



# B1L102S, U21-ch0, adc0

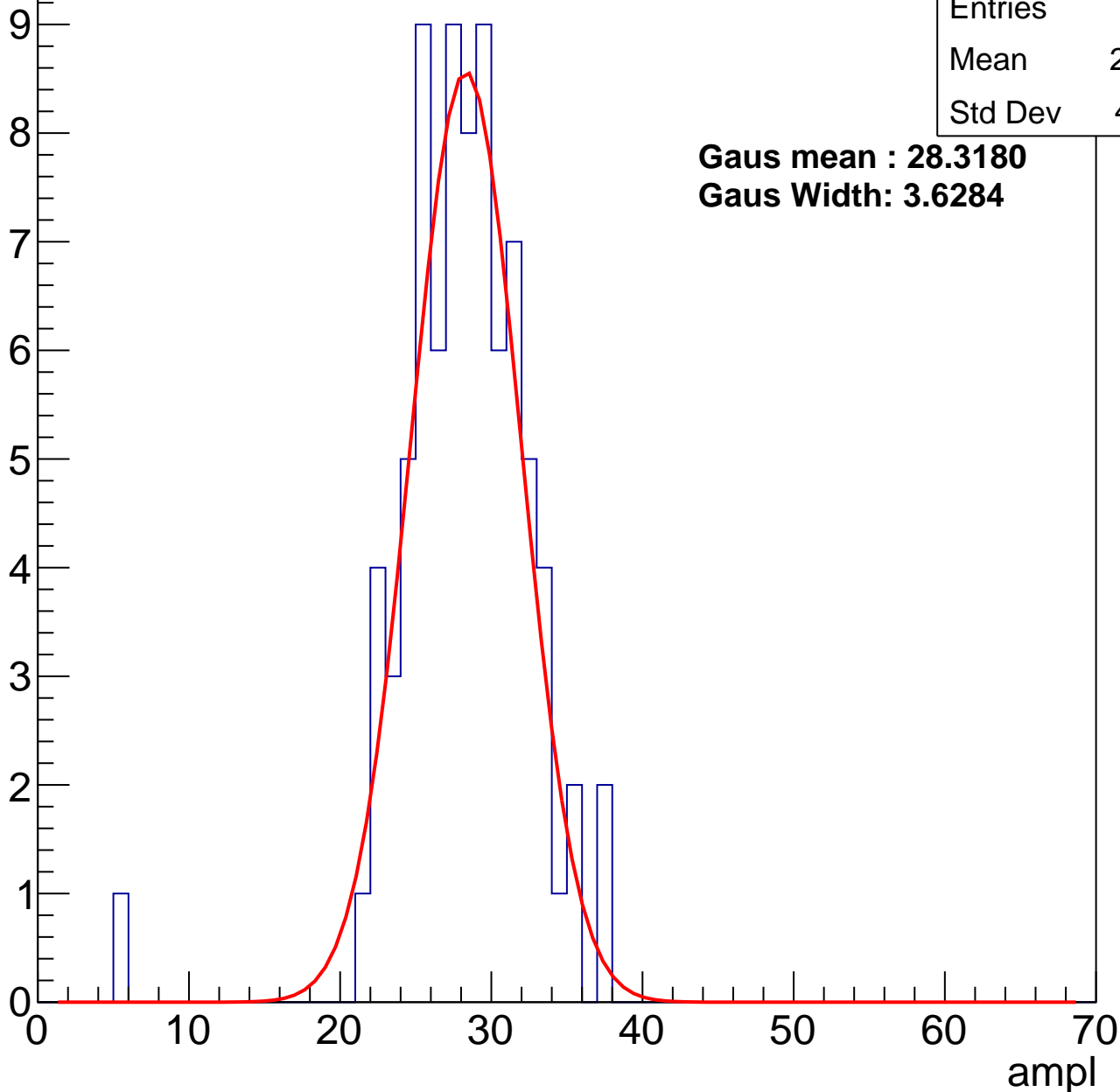
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	27.79
Std Dev	4.361

**Gaus mean : 28.3180**

**Gaus Width: 3.6284**



# B1L102S, U21-ch0, adc1

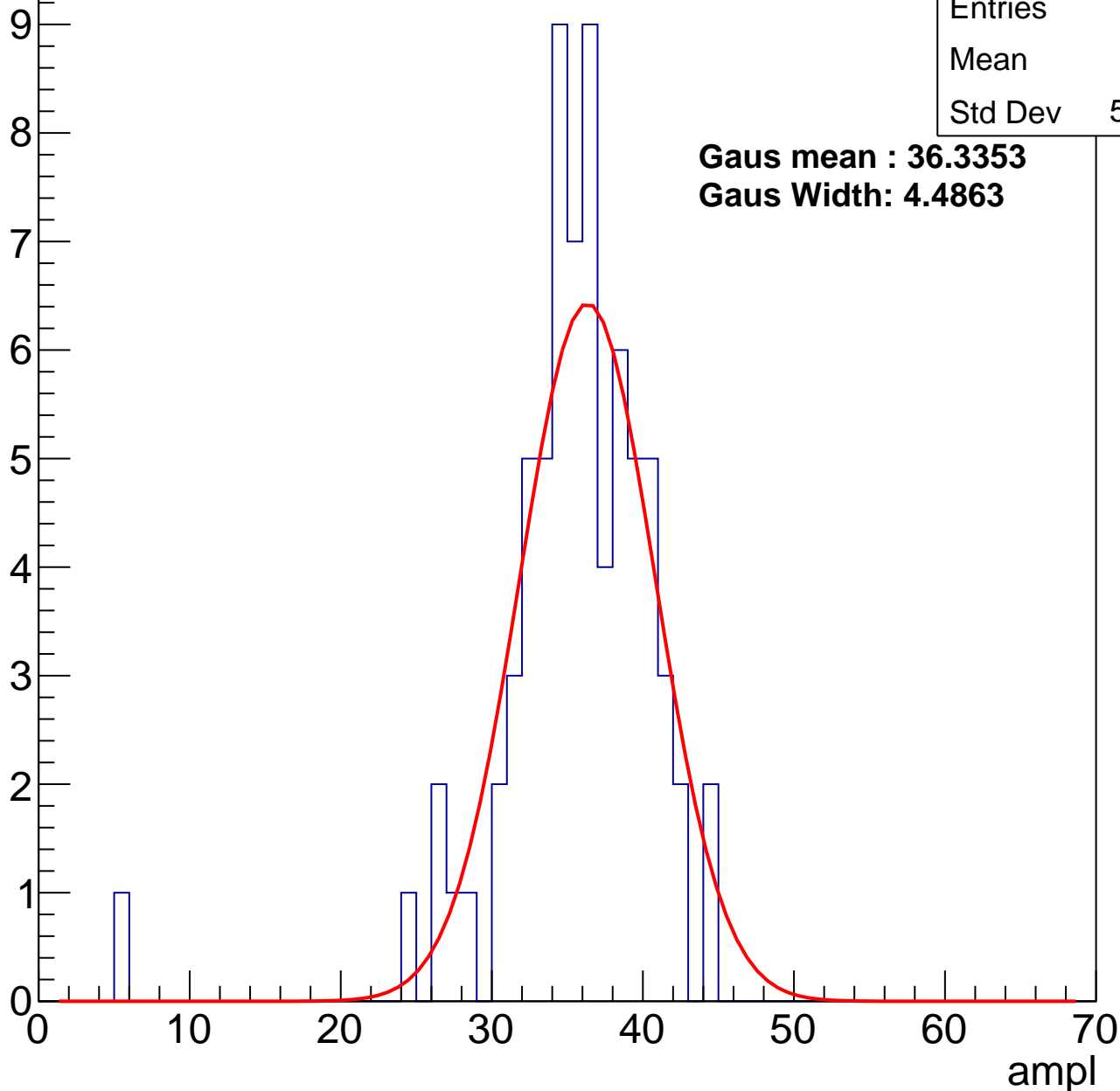
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	35
Std Dev	5.389

**Gaus mean : 36.3353**

**Gaus Width: 4.4863**



# B1L102S, U21-ch0, adc2

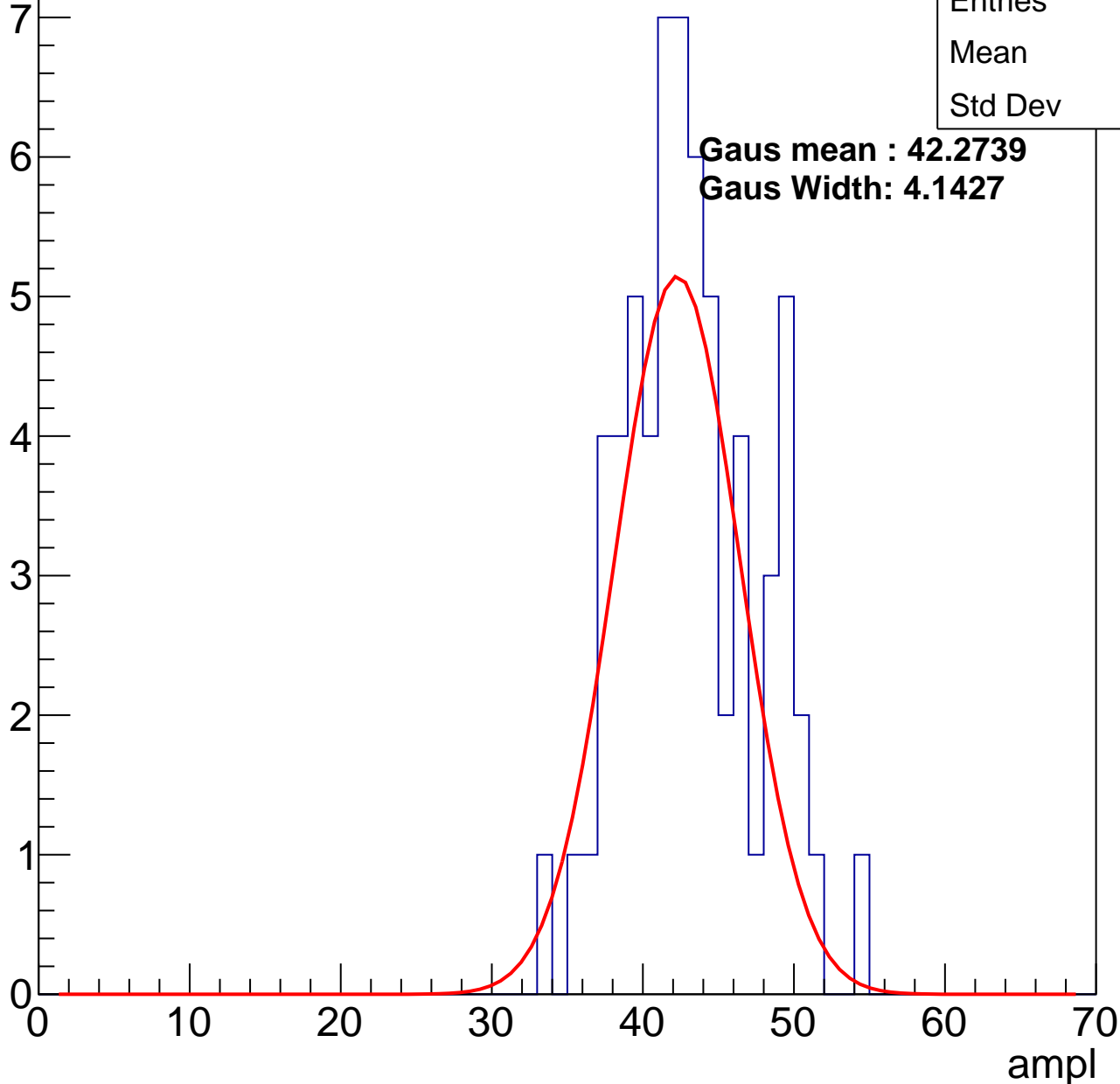
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	42.7
Std Dev	4.34

**Gaus mean : 42.2739**

**Gaus Width: 4.1427**

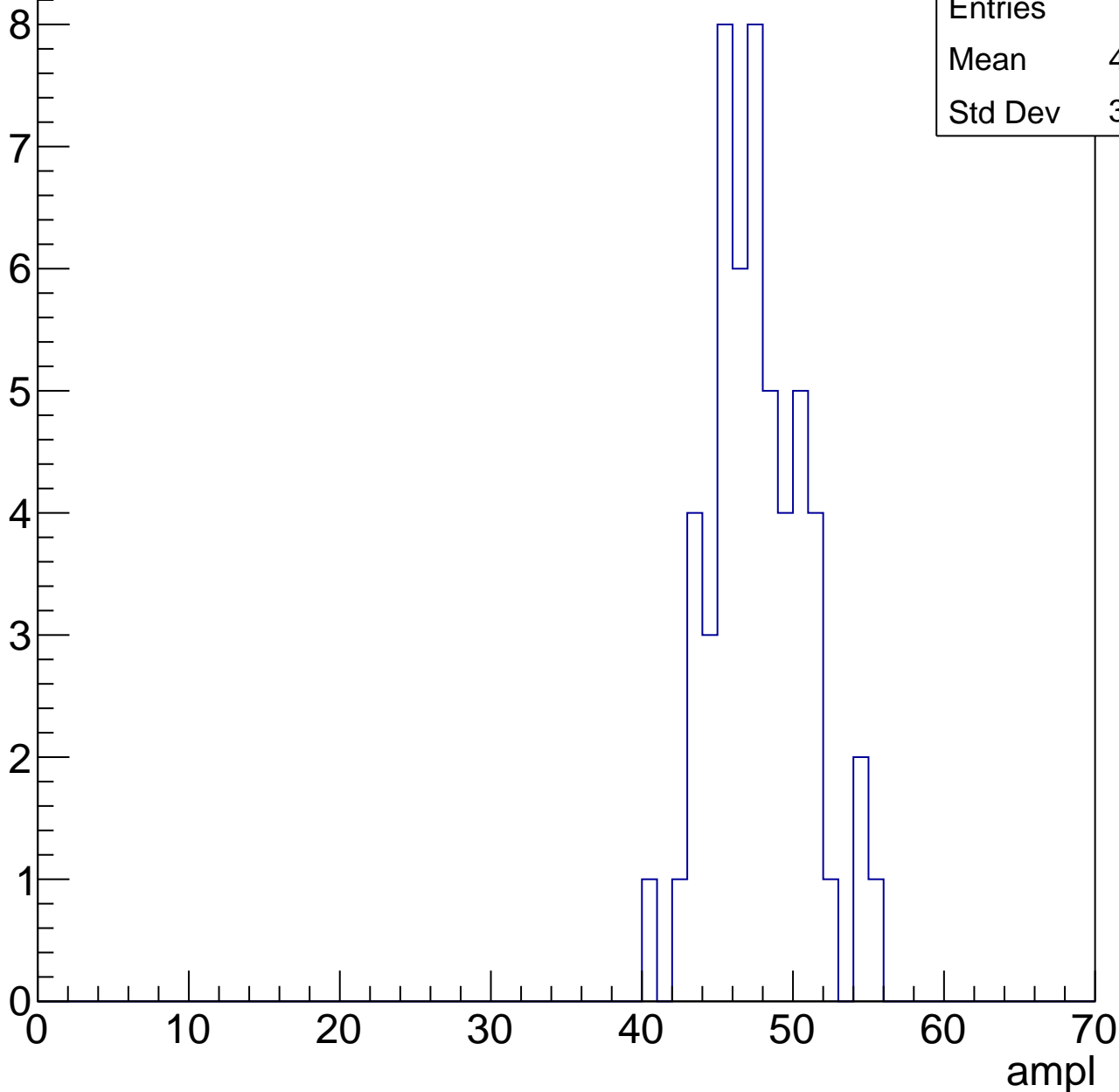


# B1L102S, U21-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	47.23
Std Dev	3.124

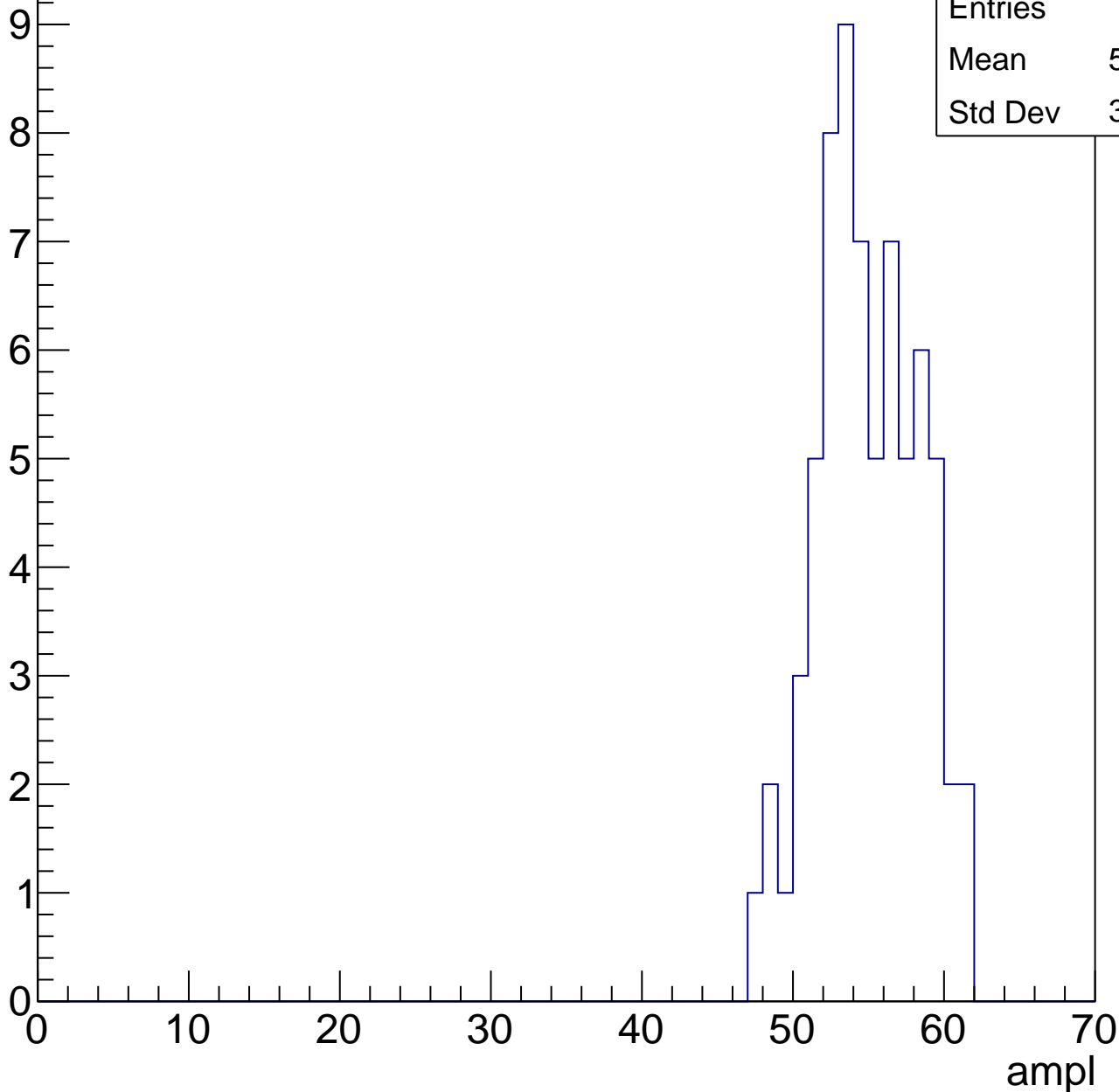


# B1L102S, U21-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	54.49
Std Dev	3.283

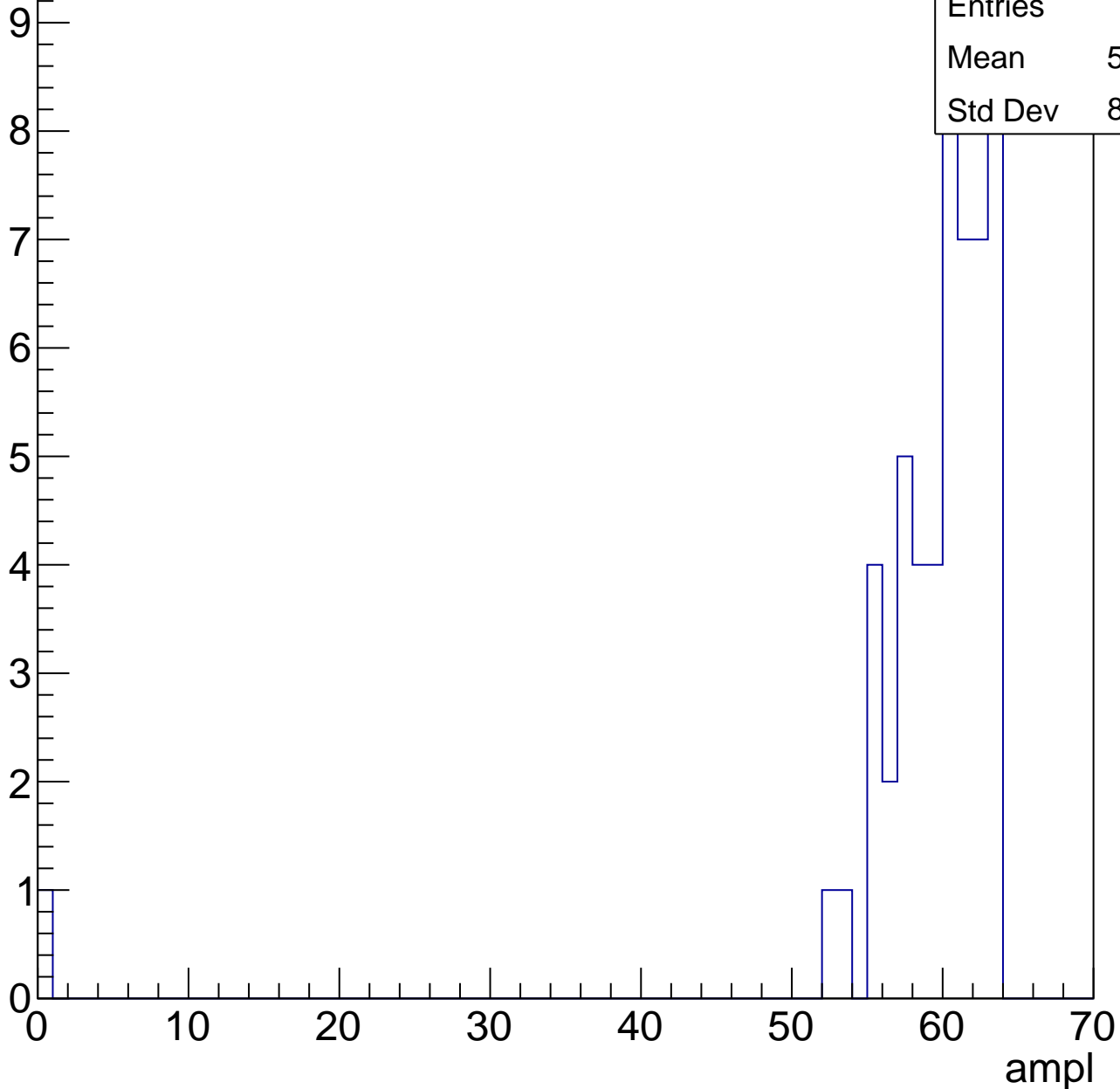


# B1L102S, U21-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

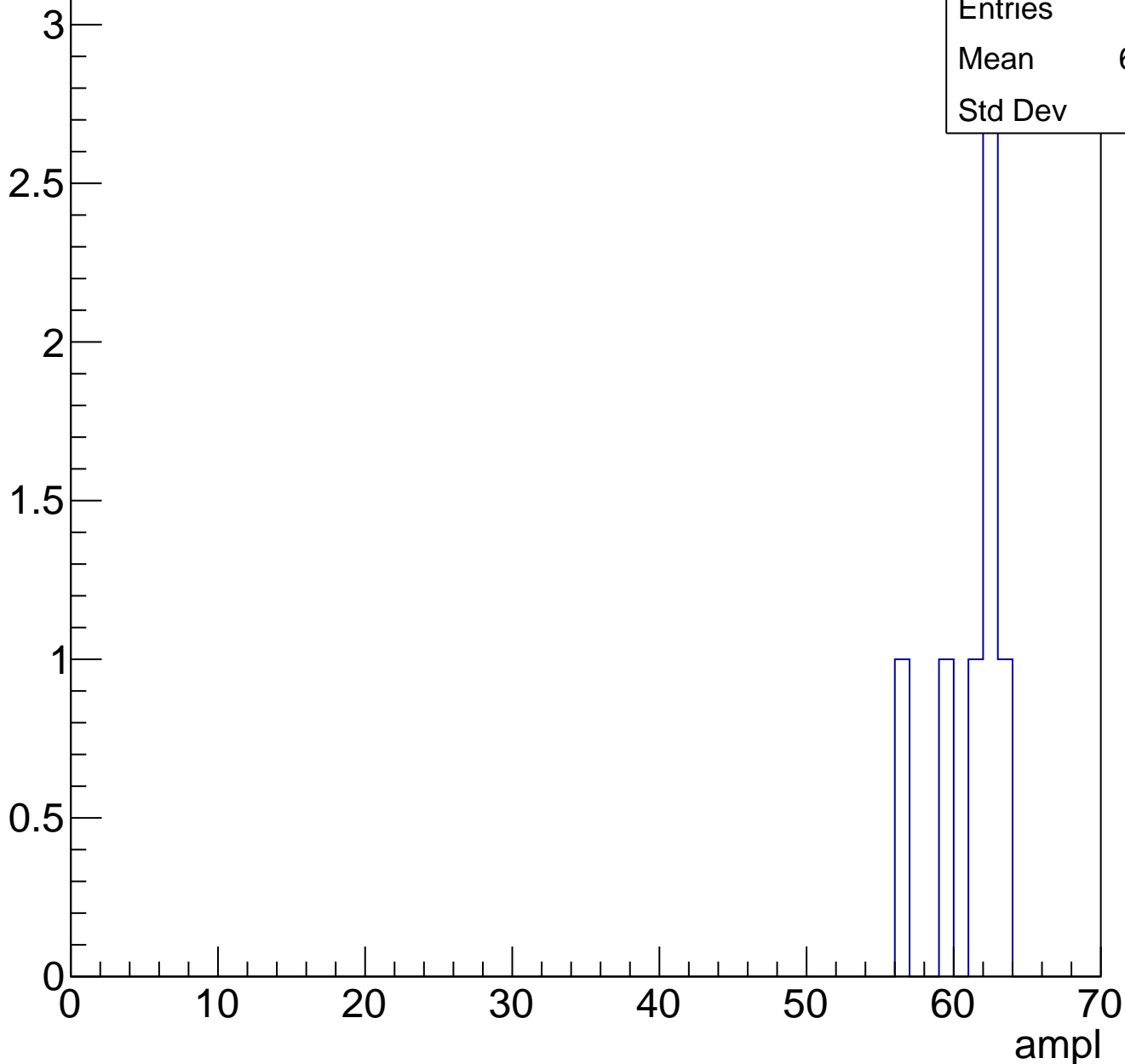
Entries	53
Mean	58.45
Std Dev	8.577



# B1L102S, U21-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	7
Mean	60.71
Std Dev	2.25



# B1L102S, U21-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U21-ch1, adc0

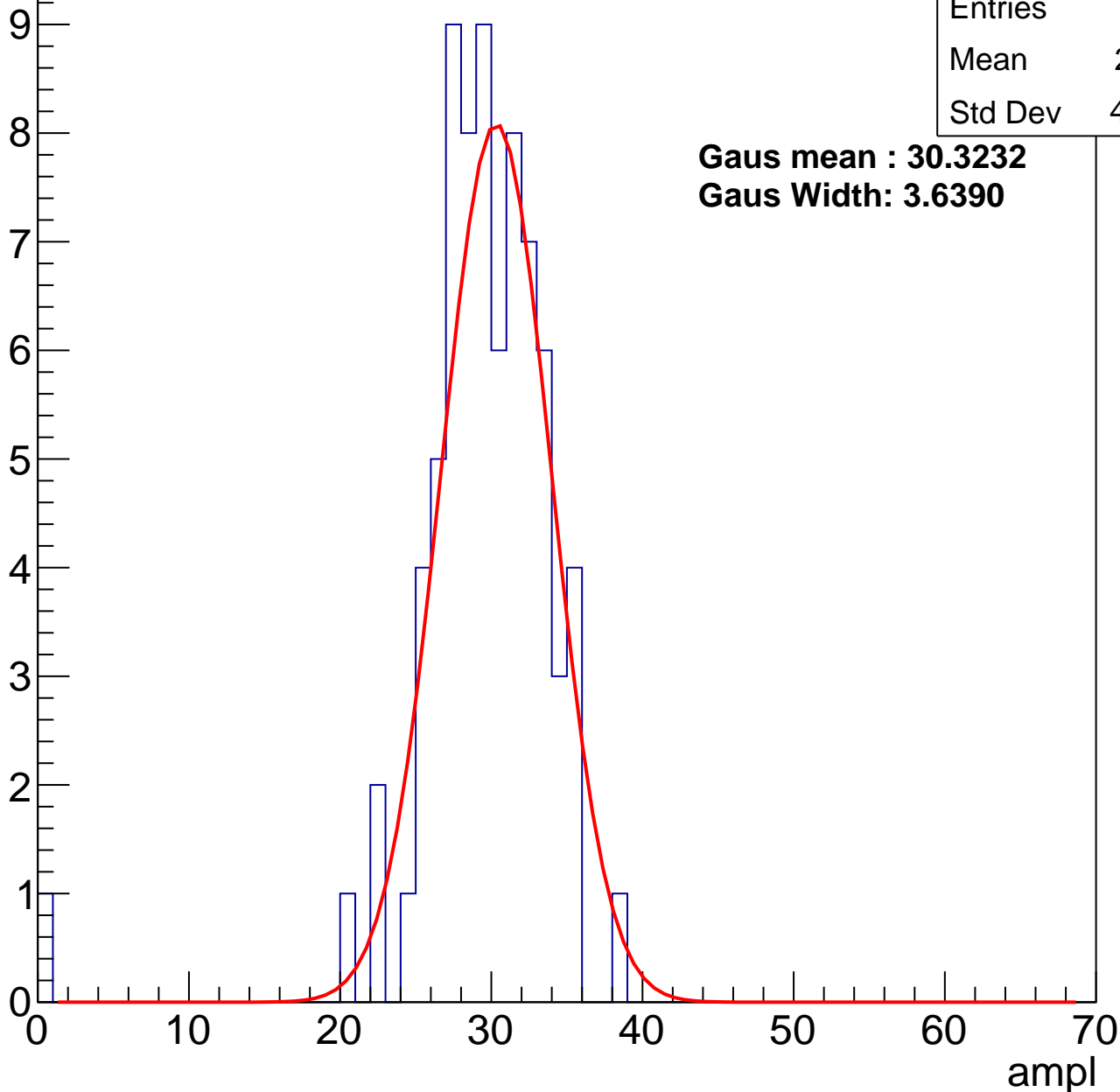
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	29.01
Std Dev	4.754

**Gaus mean : 30.3232**

**Gaus Width: 3.6390**



# B1L102S, U21-ch1, adc1

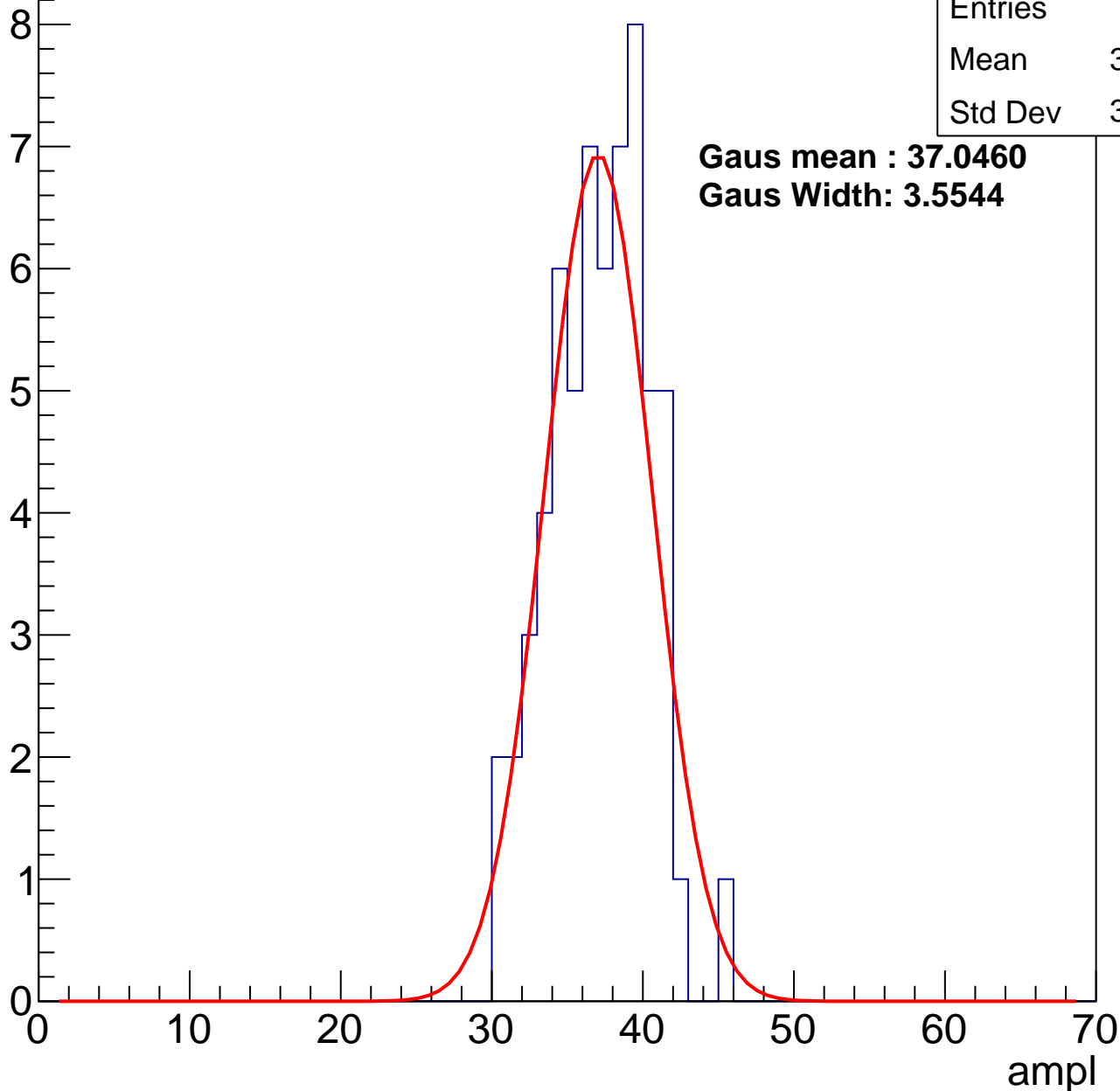
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	36.66
Std Dev	3.203

**Gaus mean : 37.0460**

**Gaus Width: 3.5544**



# B1L102S, U21-ch1, adc2

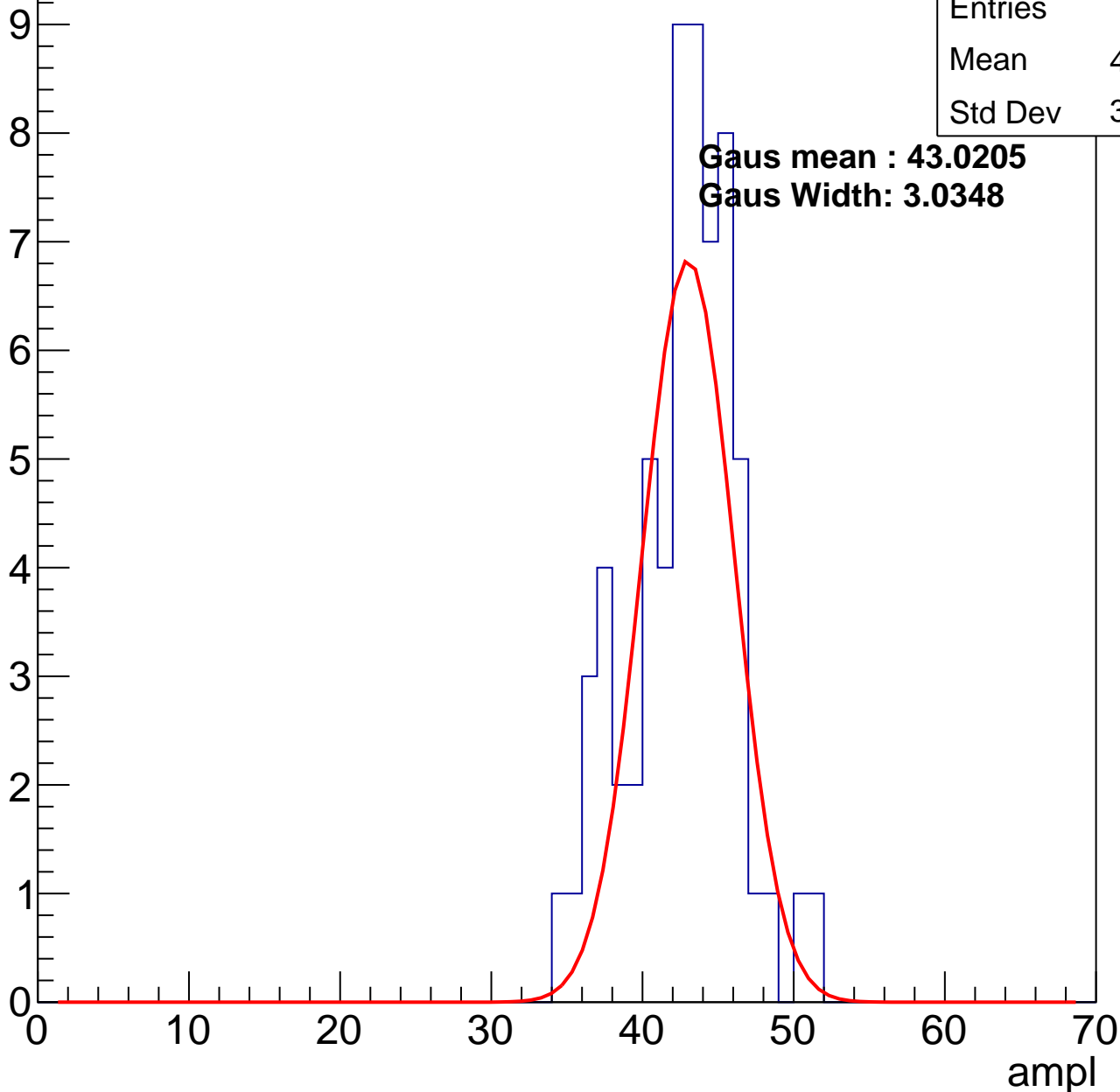
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	42.22
Std Dev	3.507

**Gaus mean : 43.0205**

**Gaus Width: 3.0348**

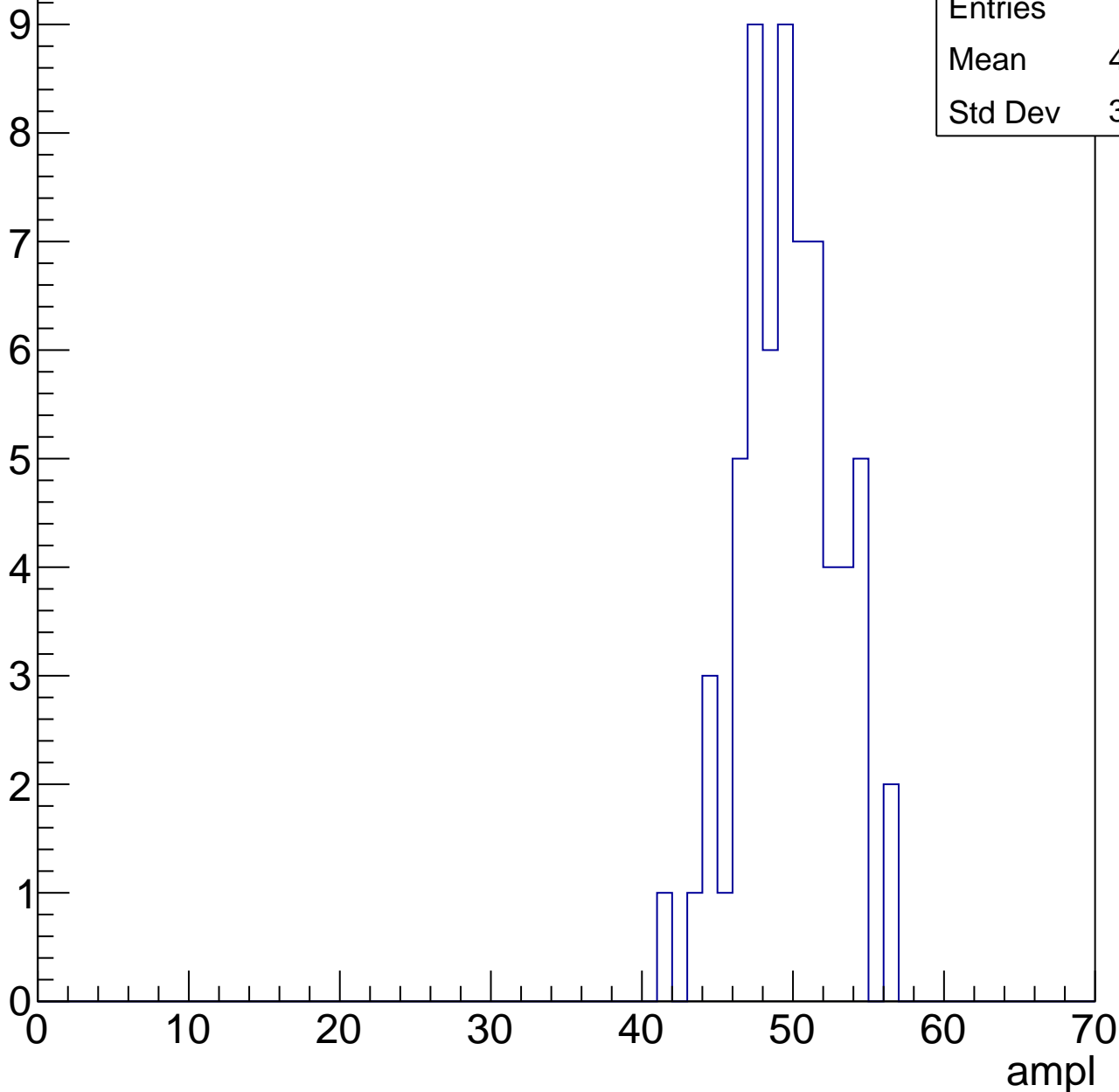


# B1L102S, U21-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	49.25
Std Dev	3.142



# B1L102S, U21-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	64
Mean	55.11
Std Dev	3.255

Entry

10

8

6

4

2

0

0

10

20

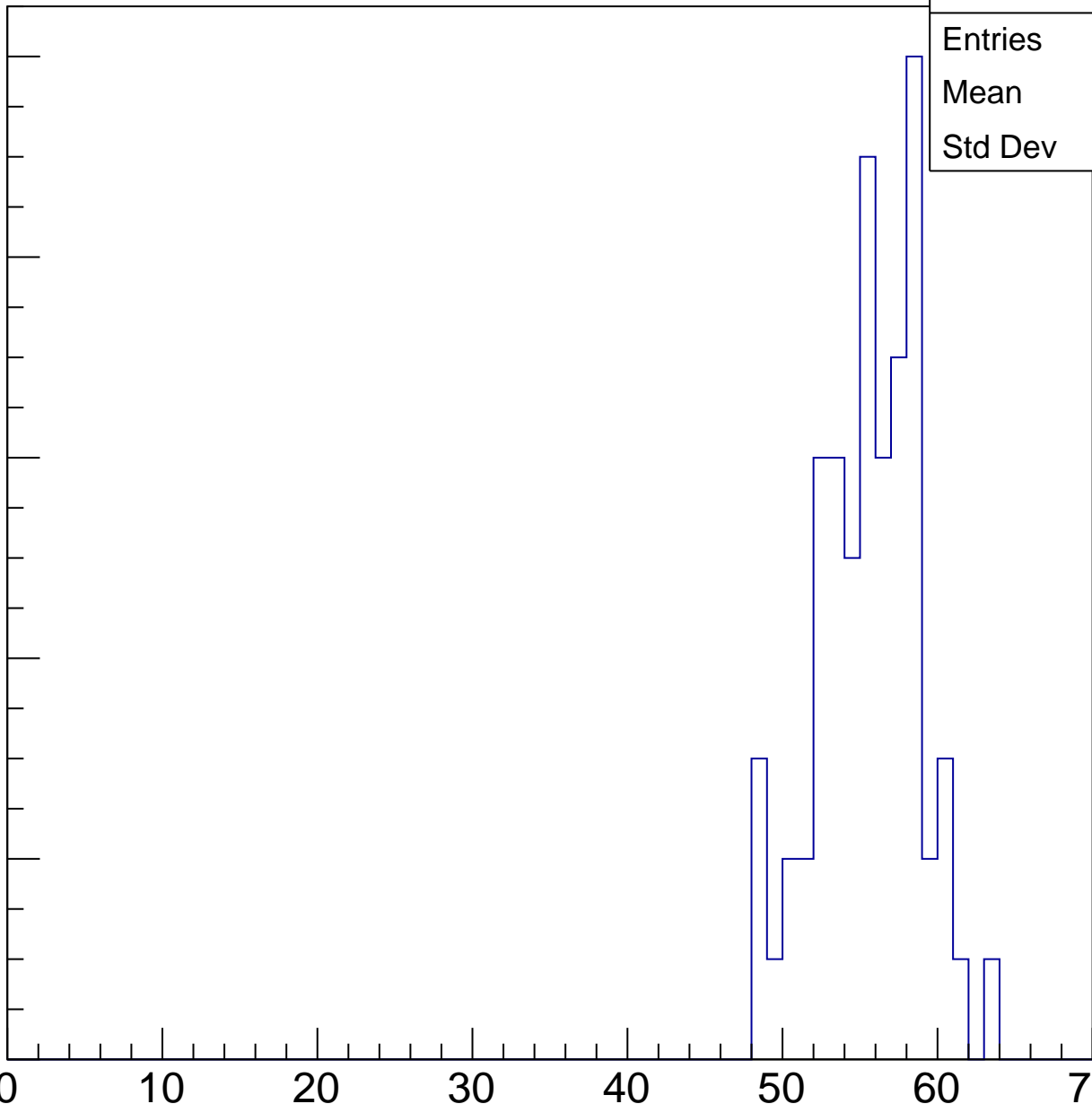
30

40

50

60

ampl



# B1L102S, U21-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	44
Mean	59.09
Std Dev	9.226

ampl

0 10 20 30 40 50 60 70

1

2

3

4

5

6

7

8

9

# B1L102S, U21-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

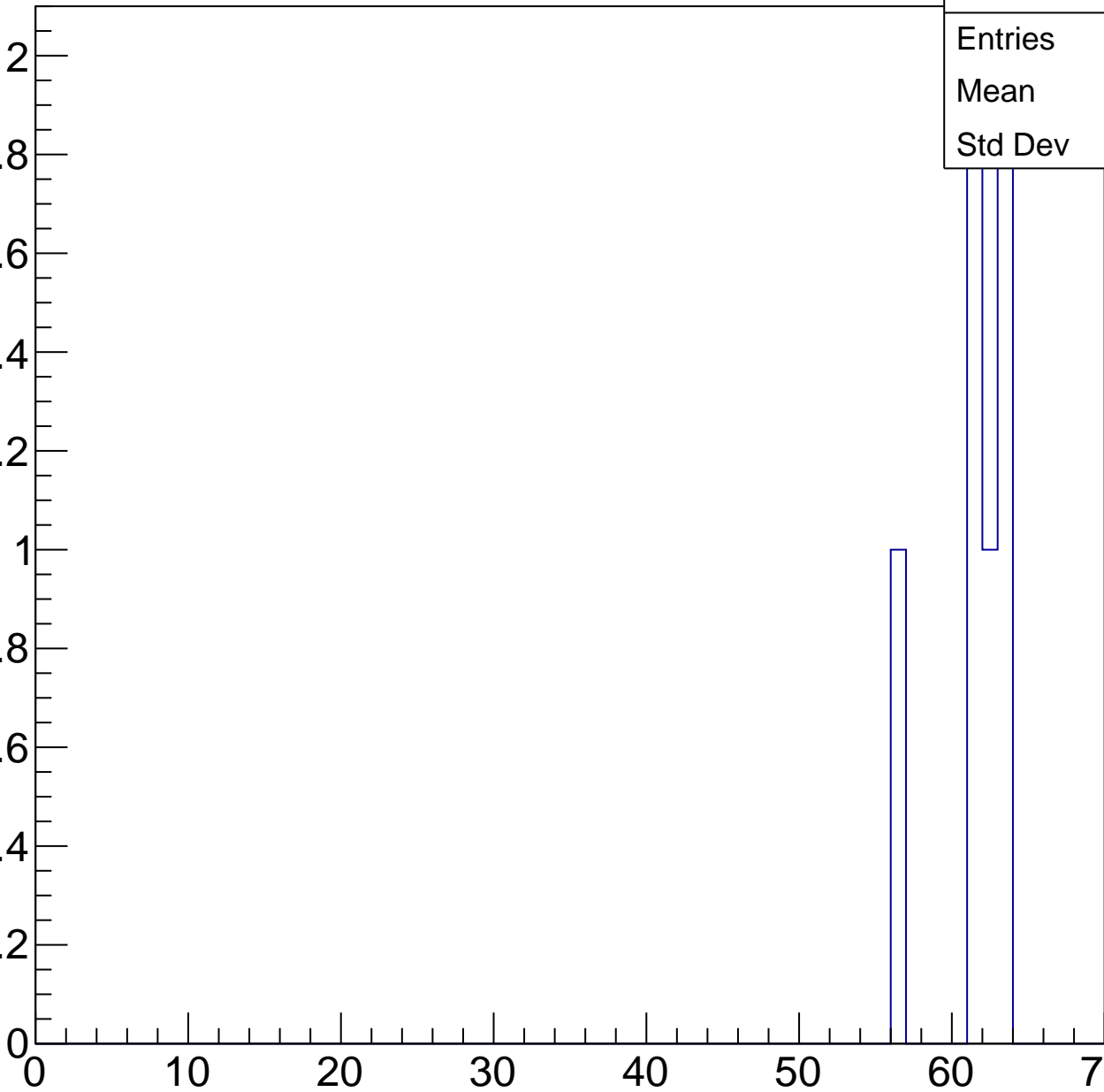
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61
Std Dev	2.38

0 10 20 30 40 50 60 70

ampl





# B1L102S, U21-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U21-ch2, adc0

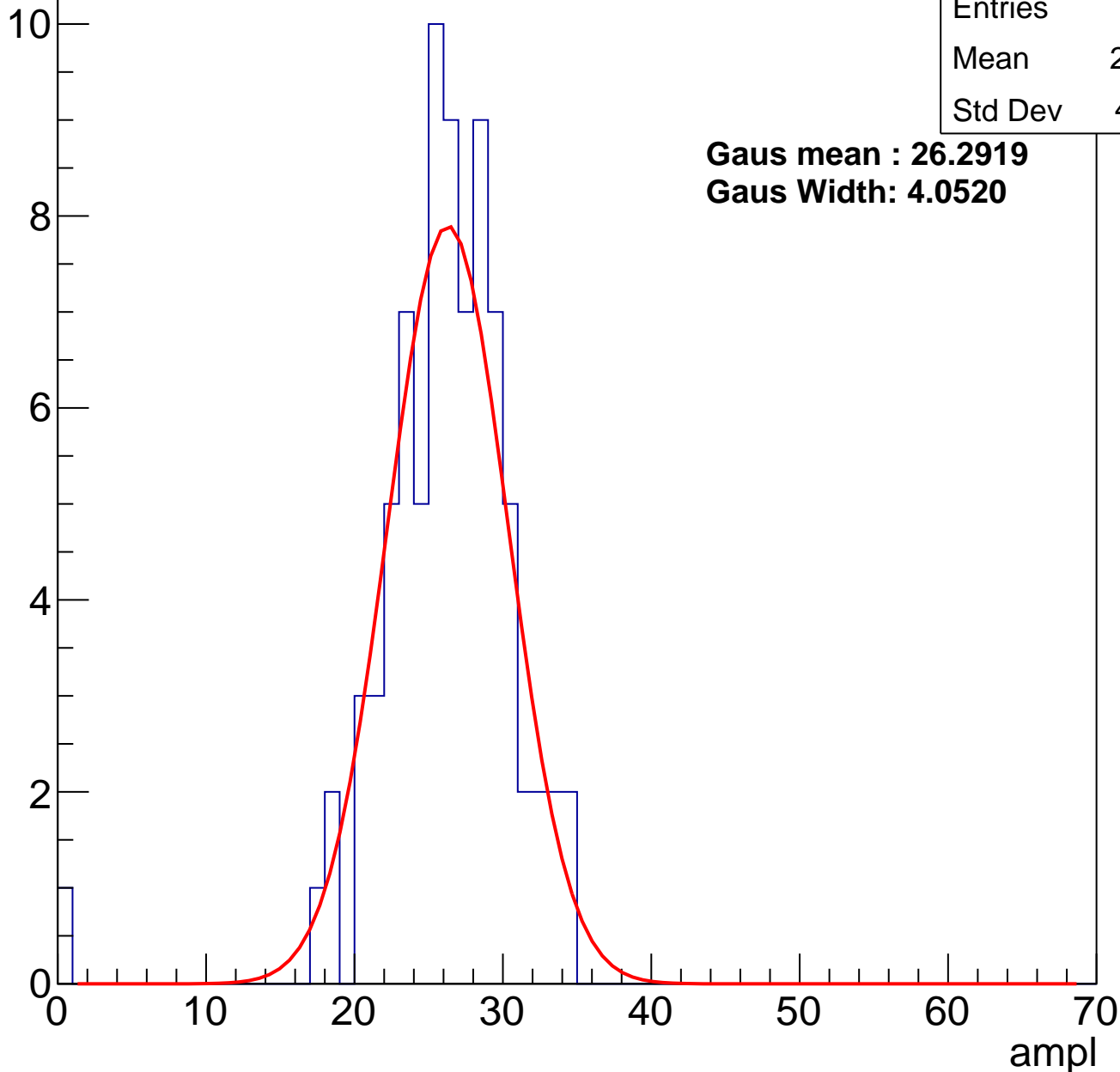
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	82
Mean	25.67
Std Dev	4.641

**Gaus mean : 26.2919**

**Gaus Width: 4.0520**

Entry



# B1L102S, U21-ch2, adc1

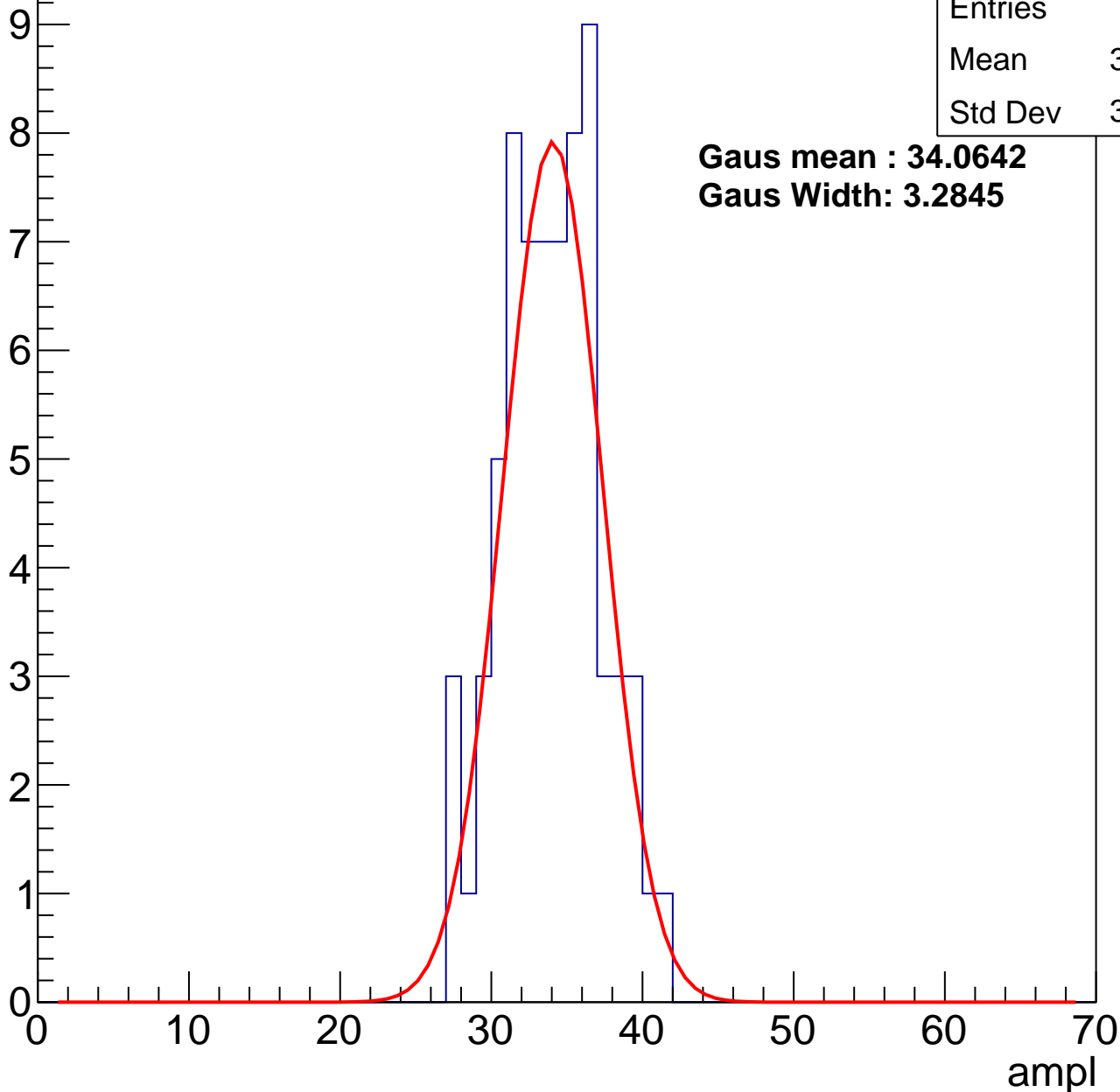
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	33.54
Std Dev	3.206

**Gaus mean : 34.0642**

**Gaus Width: 3.2845**



# B1L102S, U21-ch2, adc2

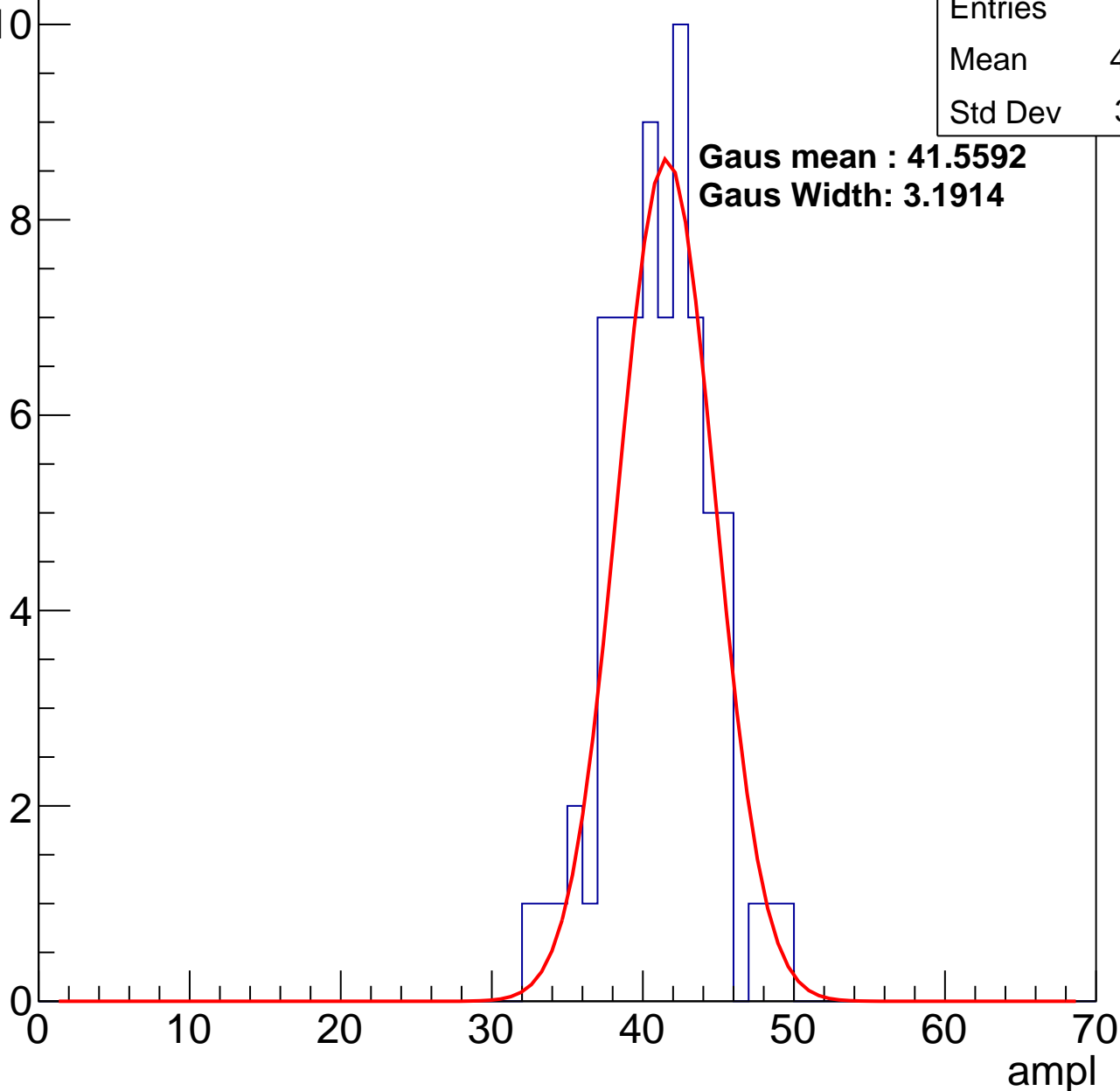
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	40.55
Std Dev	3.311

**Gaus mean : 41.5592**

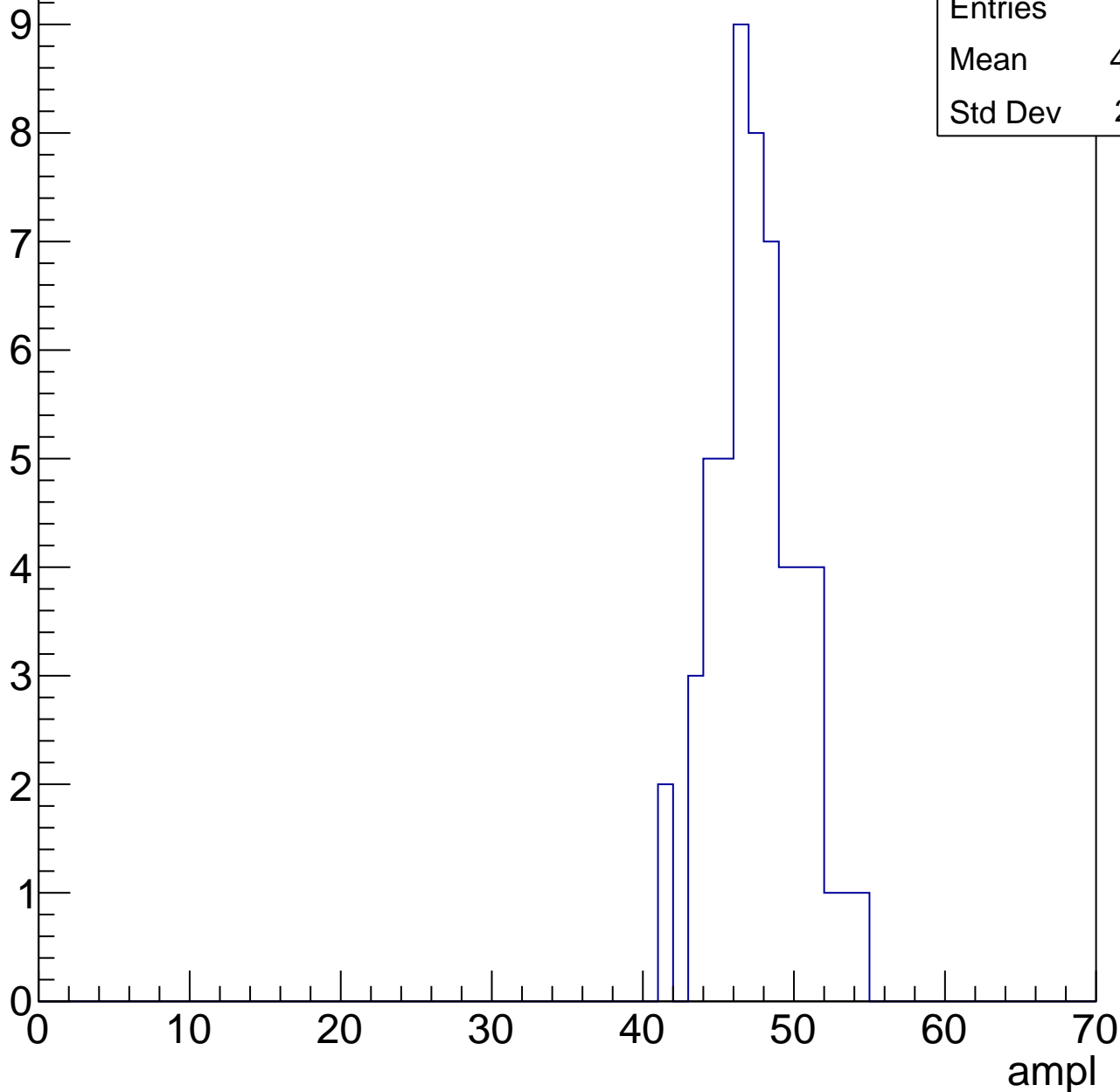
**Gaus Width: 3.1914**



# B1L102S, U21-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



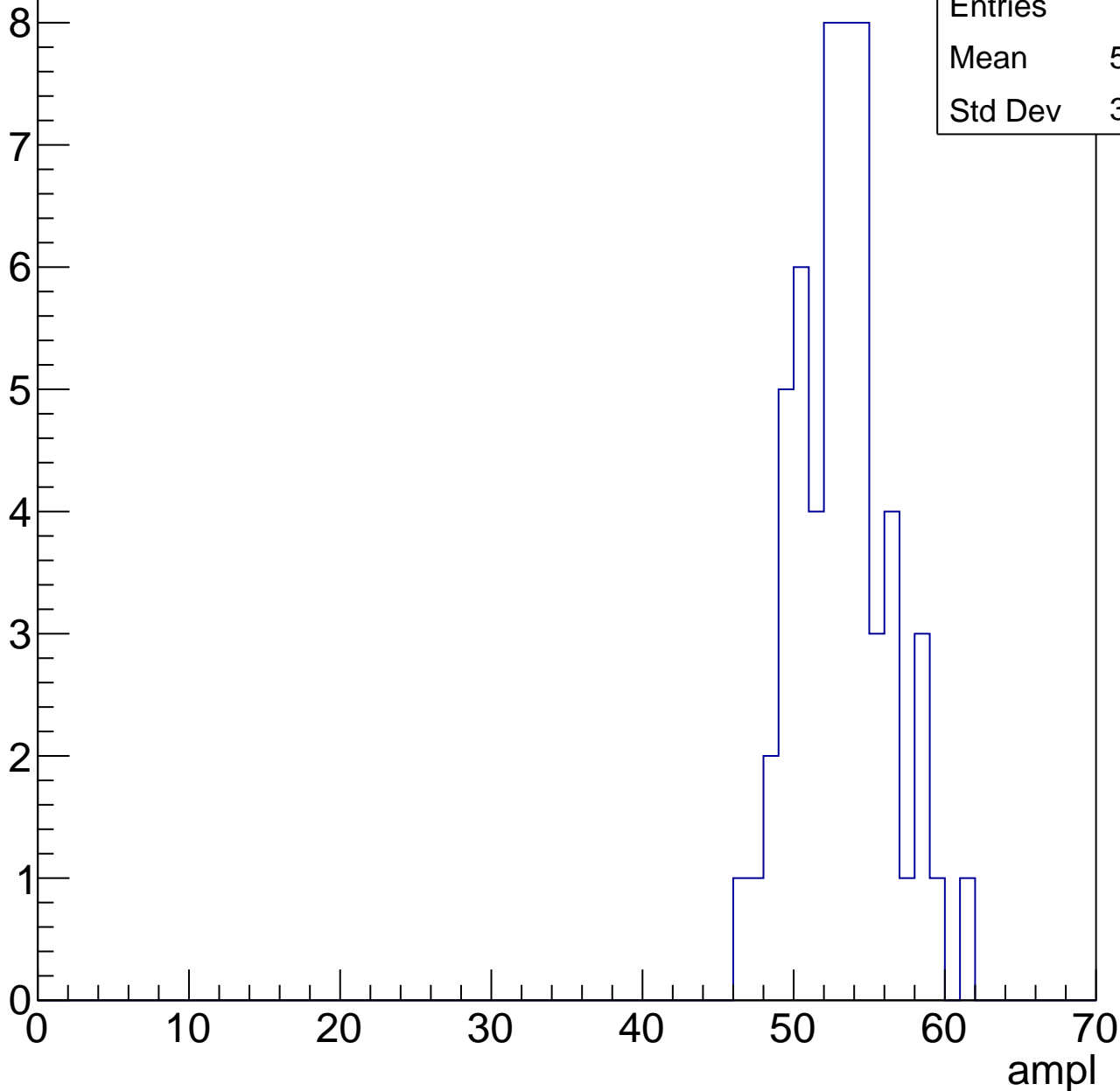
Entries	54
Mean	47.06
Std Dev	2.811

# B1L102S, U21-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	52.68
Std Dev	3.089

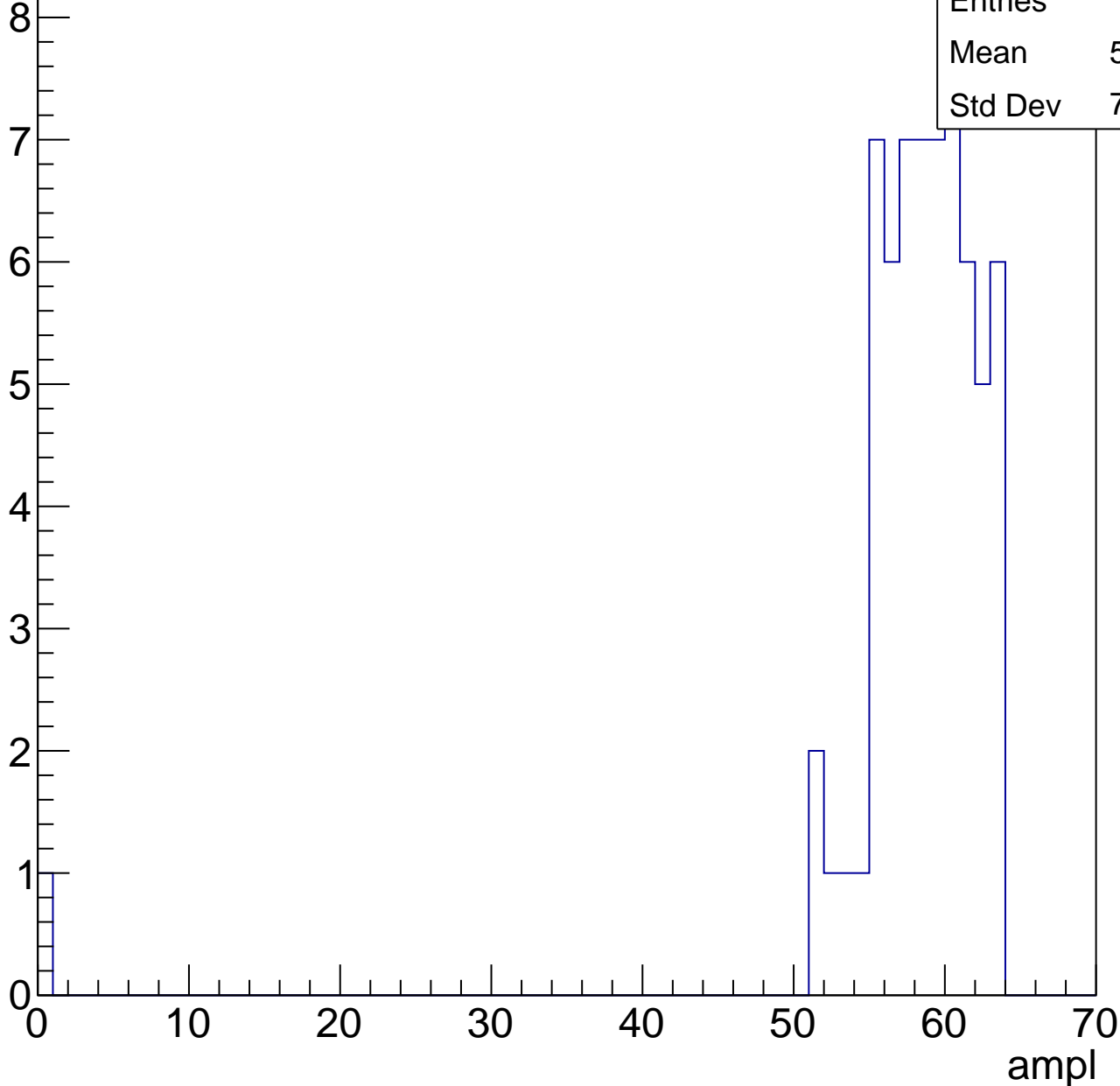


# B1L102S, U21-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	57.45
Std Dev	7.782



# B1L102S, U21-ch2, adc6

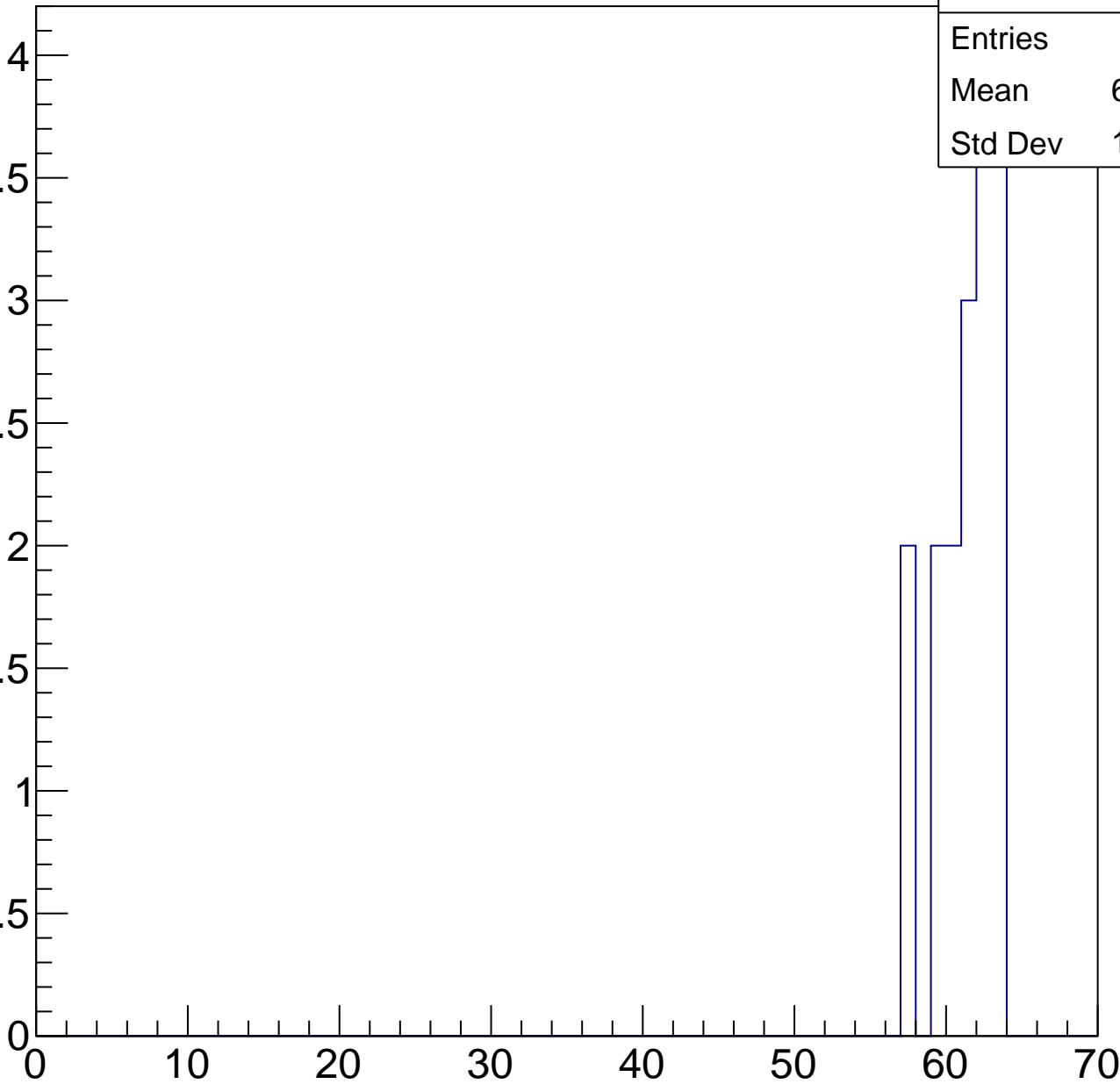
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

4  
3.5  
3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	17
Mean	60.88
Std Dev	1.906

ampl





# B1L102S, U21-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	20.67
Std Dev	29.23

# B1L102S, U21-ch3, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	79
Mean	31.08
Std Dev	3.217

**Gaus mean : 31.4190**

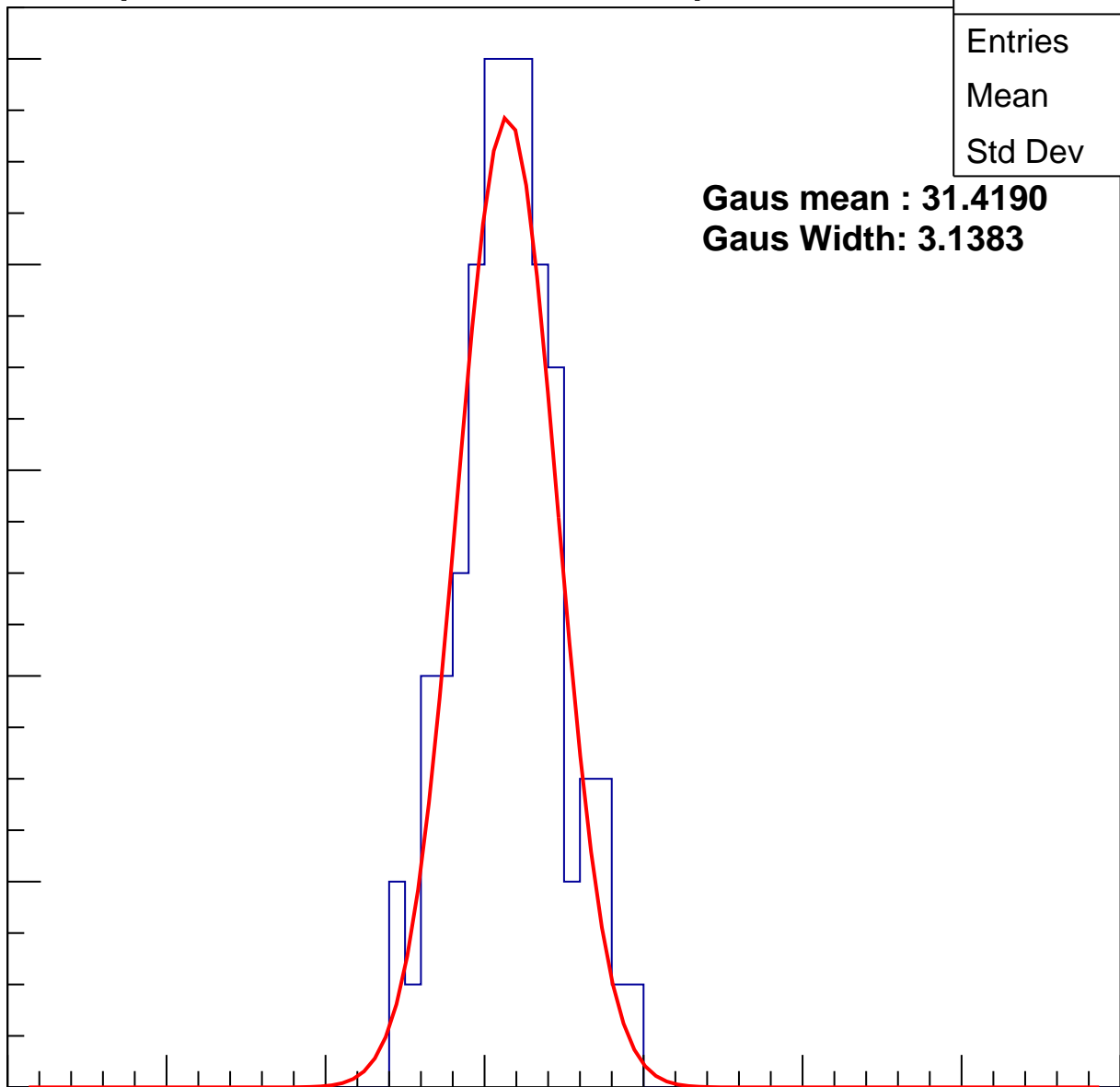
**Gaus Width: 3.1383**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U21-ch3, adc1

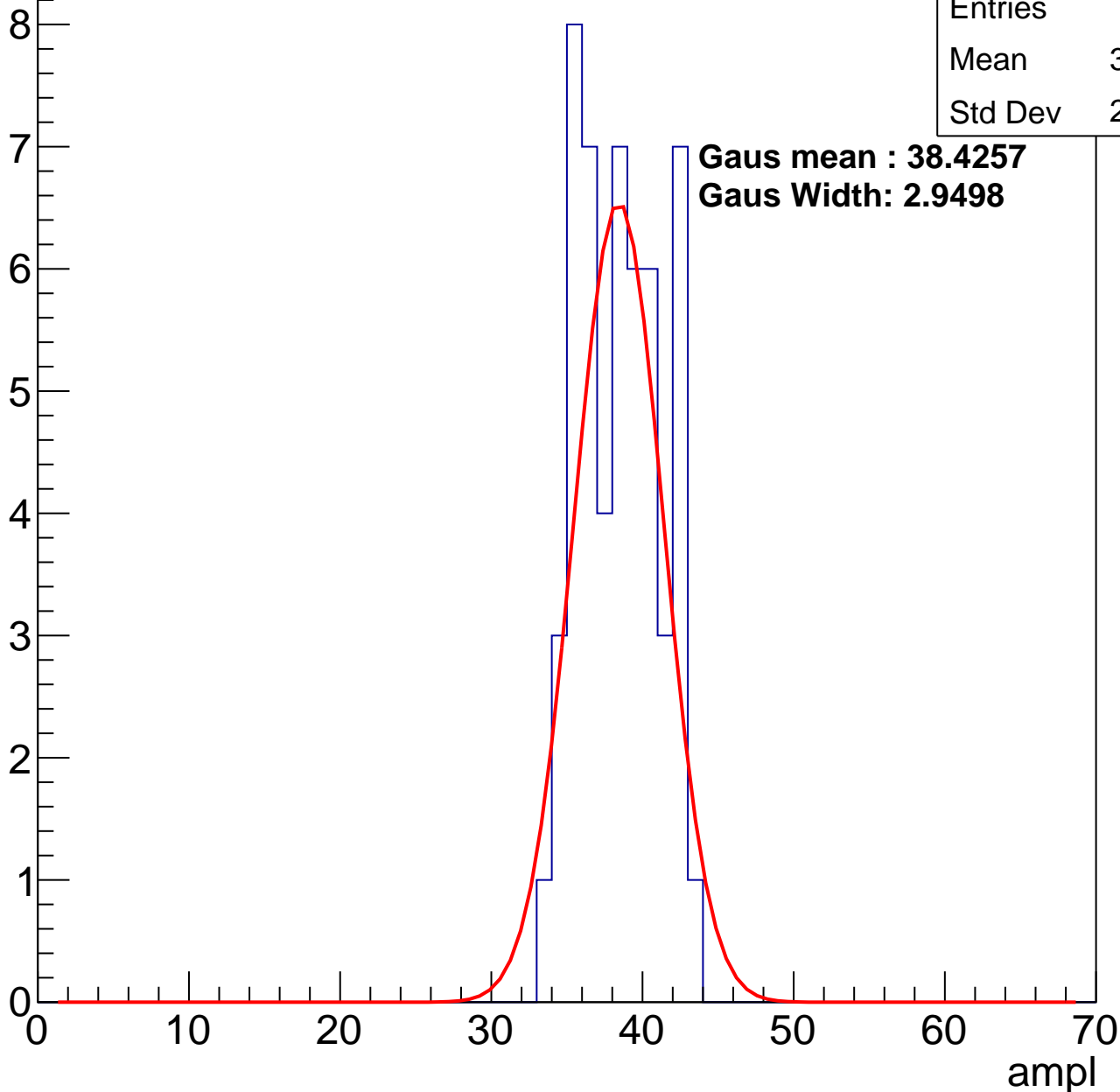
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	38.02
Std Dev	2.646

**Gaus mean : 38.4257**

**Gaus Width: 2.9498**



# B1L102S, U21-ch3, adc2

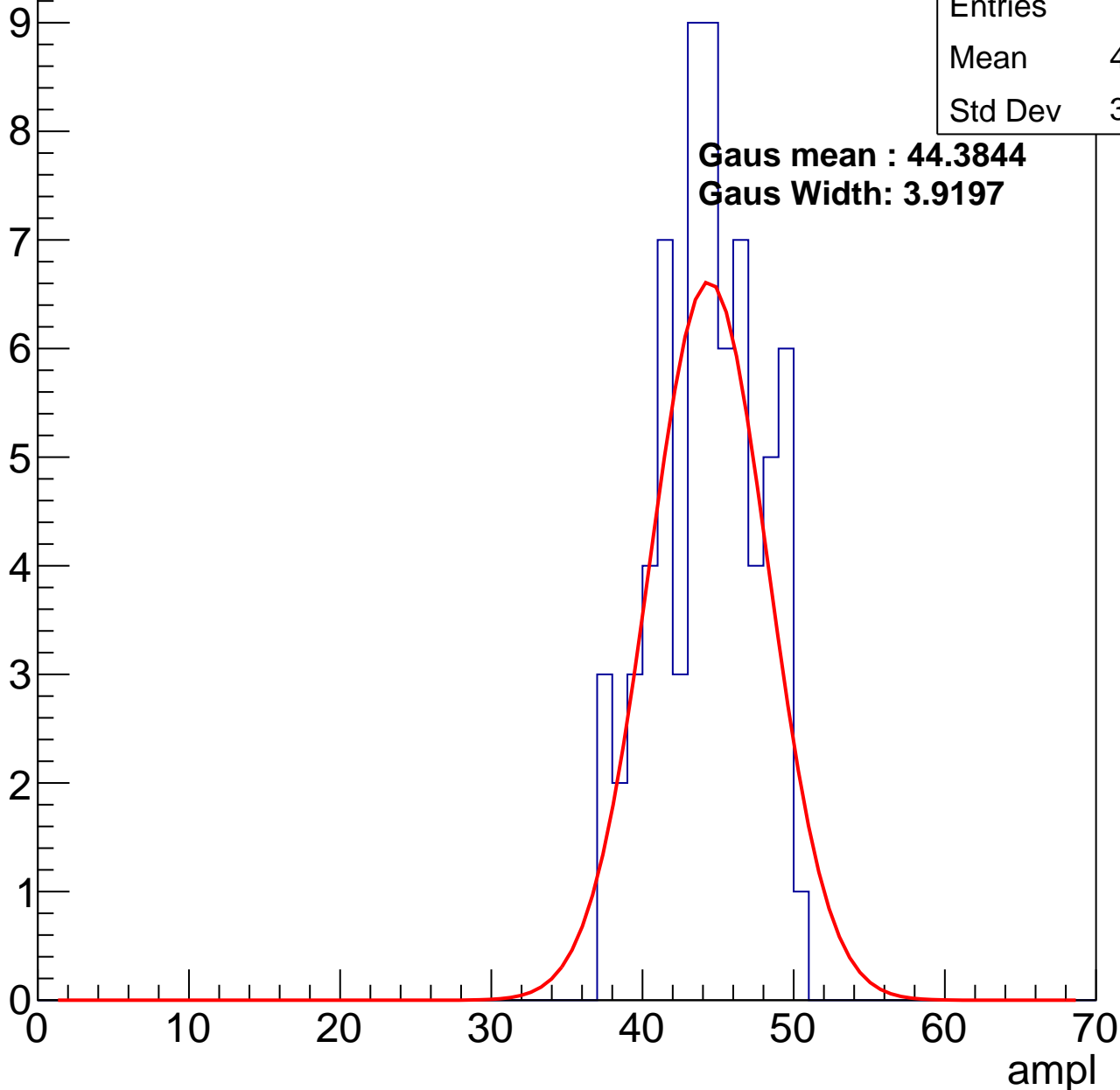
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	43.83
Std Dev	3.353

**Gaus mean : 44.3844**

**Gaus Width: 3.9197**

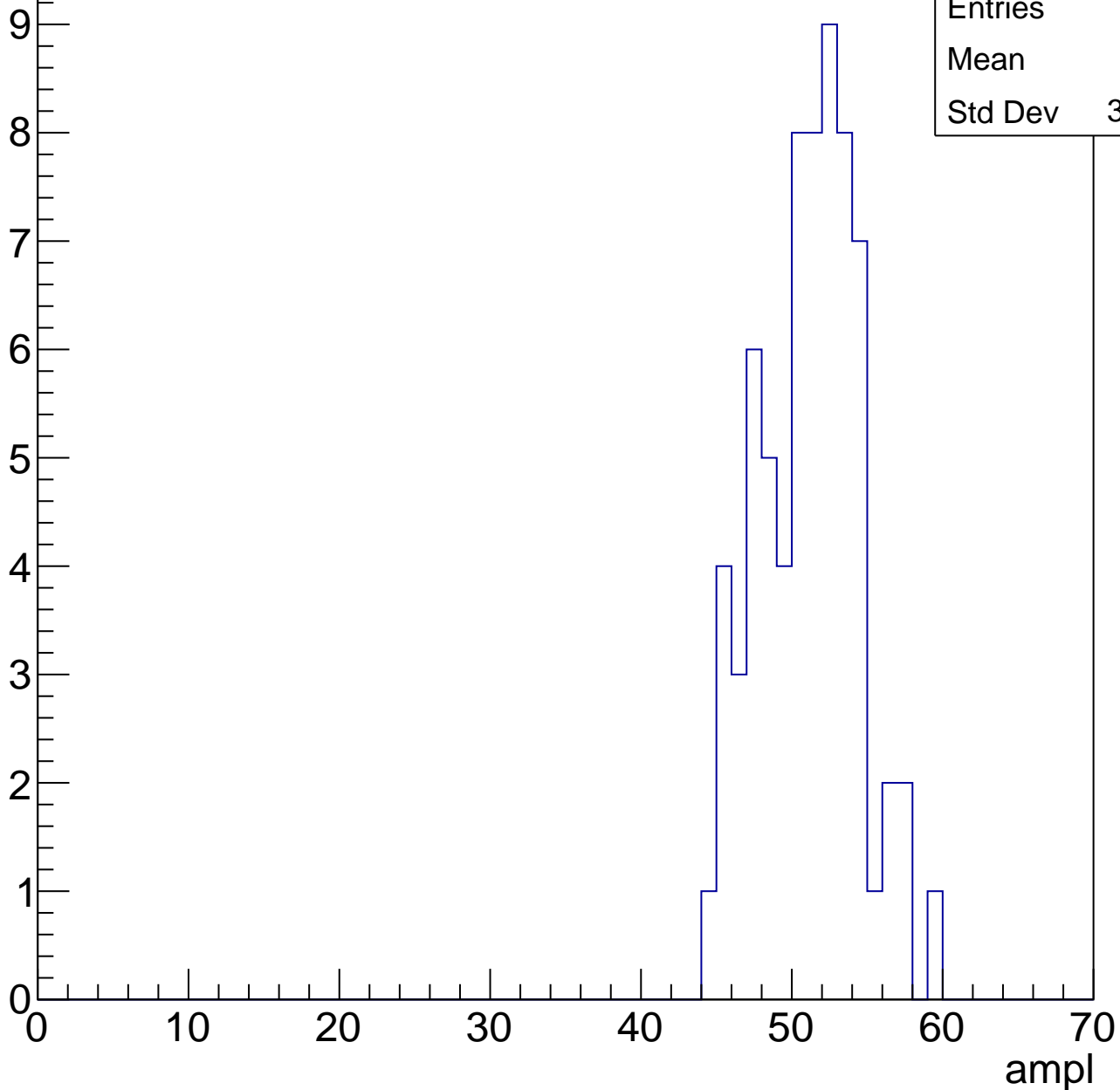


# B1L102S, U21-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	50.7
Std Dev	3.258

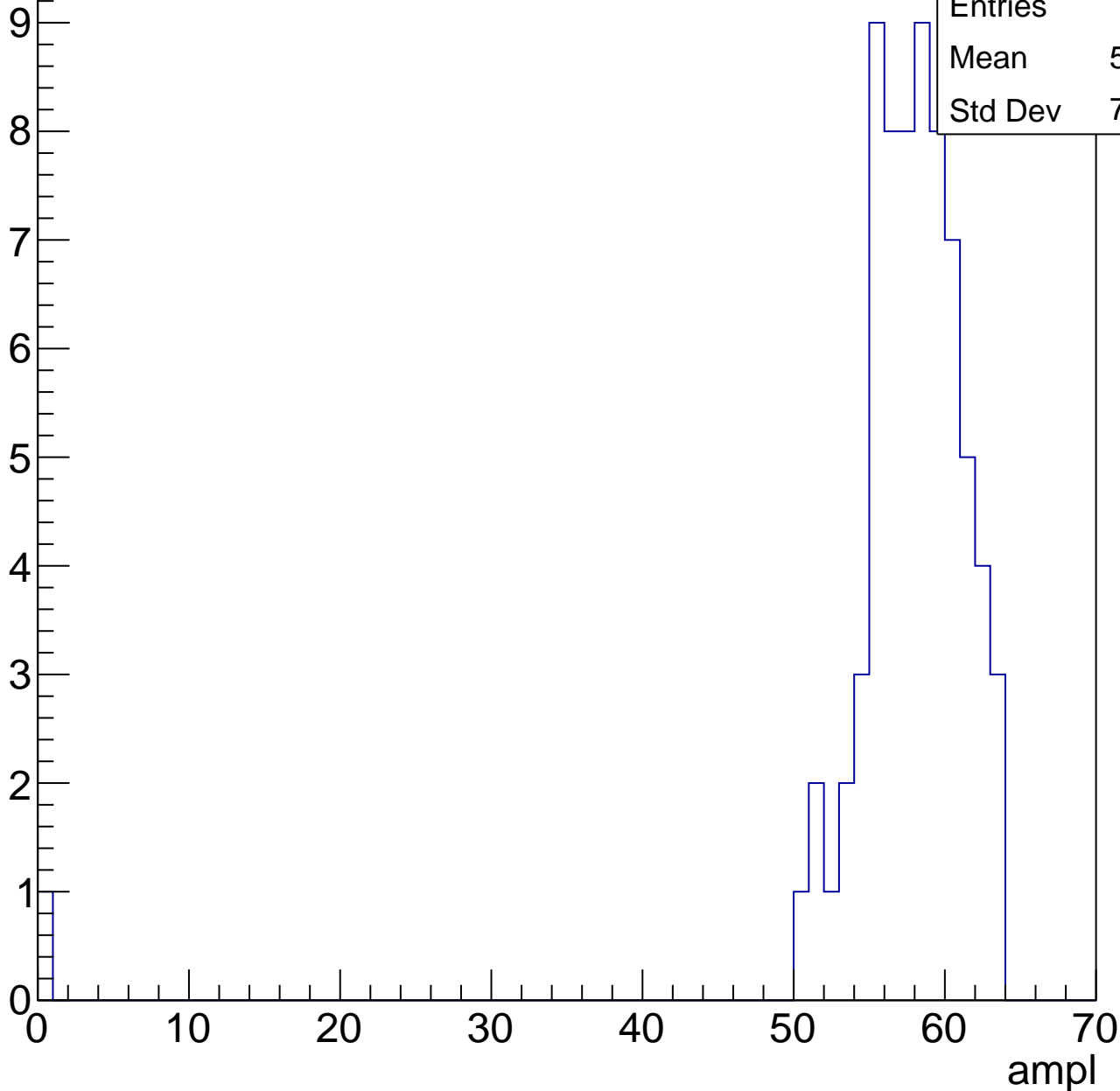


# B1L102S, U21-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	56.72
Std Dev	7.397

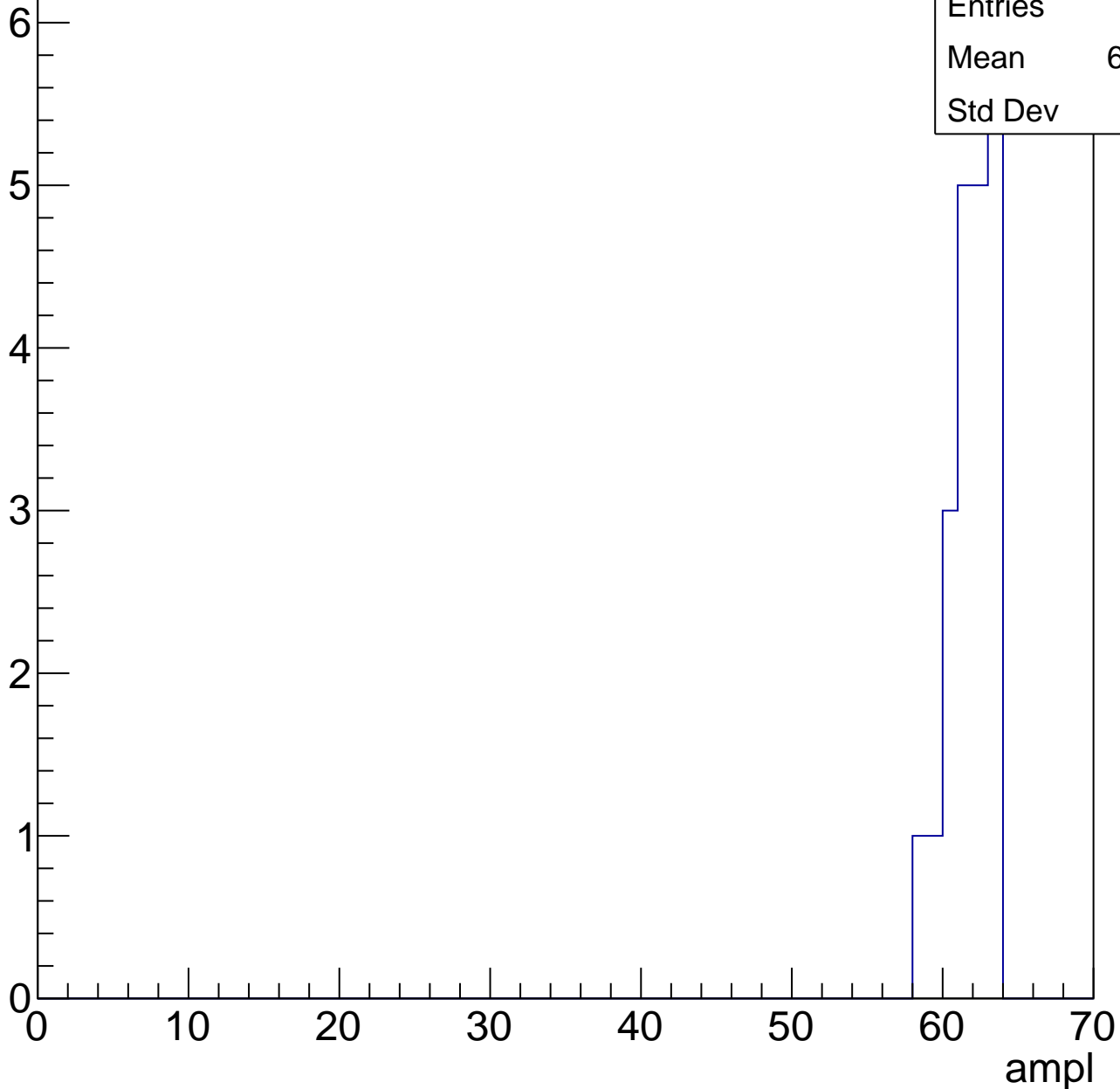


# B1L102S, U21-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	21
Mean	61.43
Std Dev	1.4



# B1L102S, U21-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch4, adc0

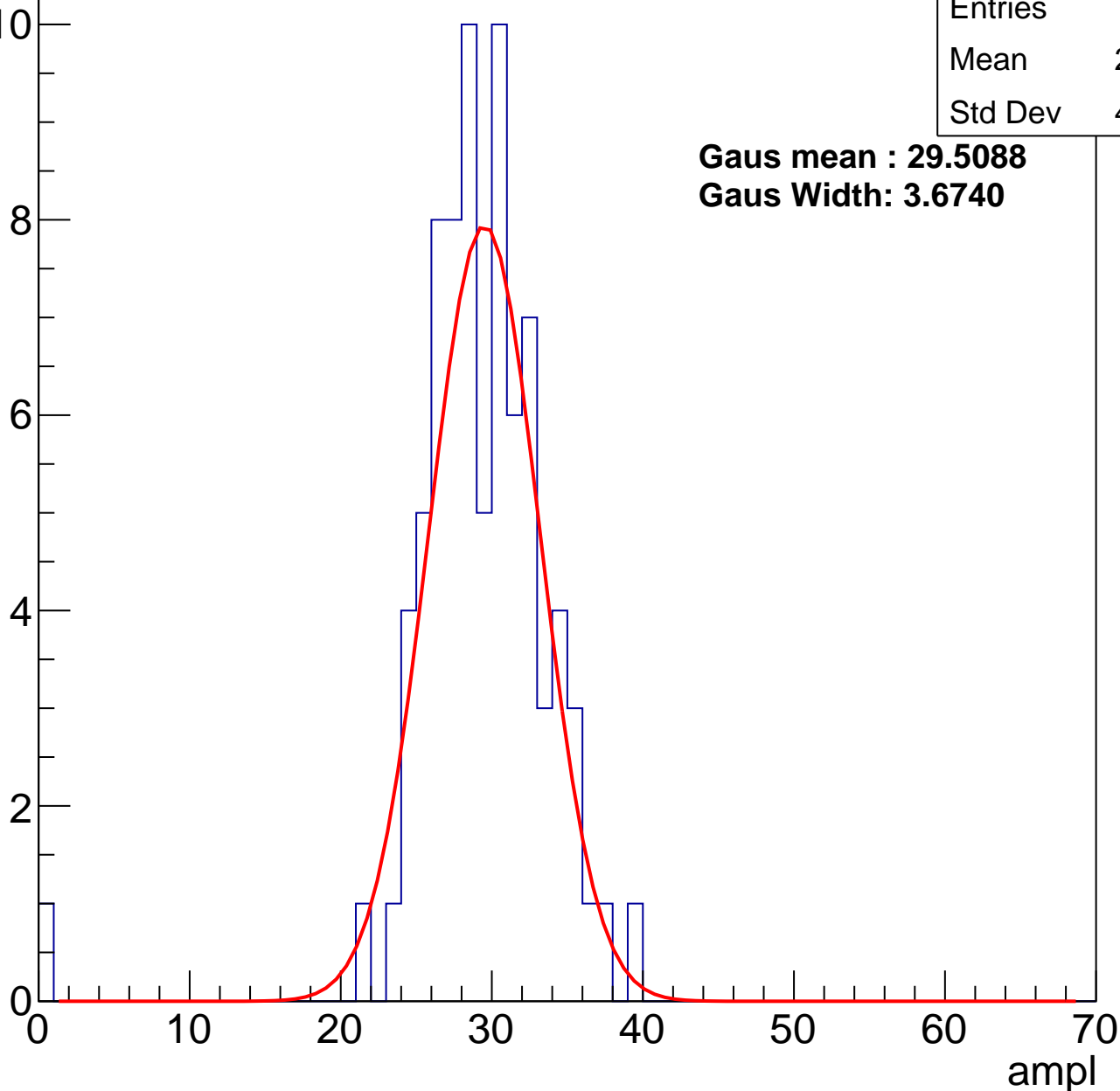
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	28.81
Std Dev	4.771

**Gaus mean : 29.5088**

**Gaus Width: 3.6740**



# B1L102S, U21-ch4, adc1

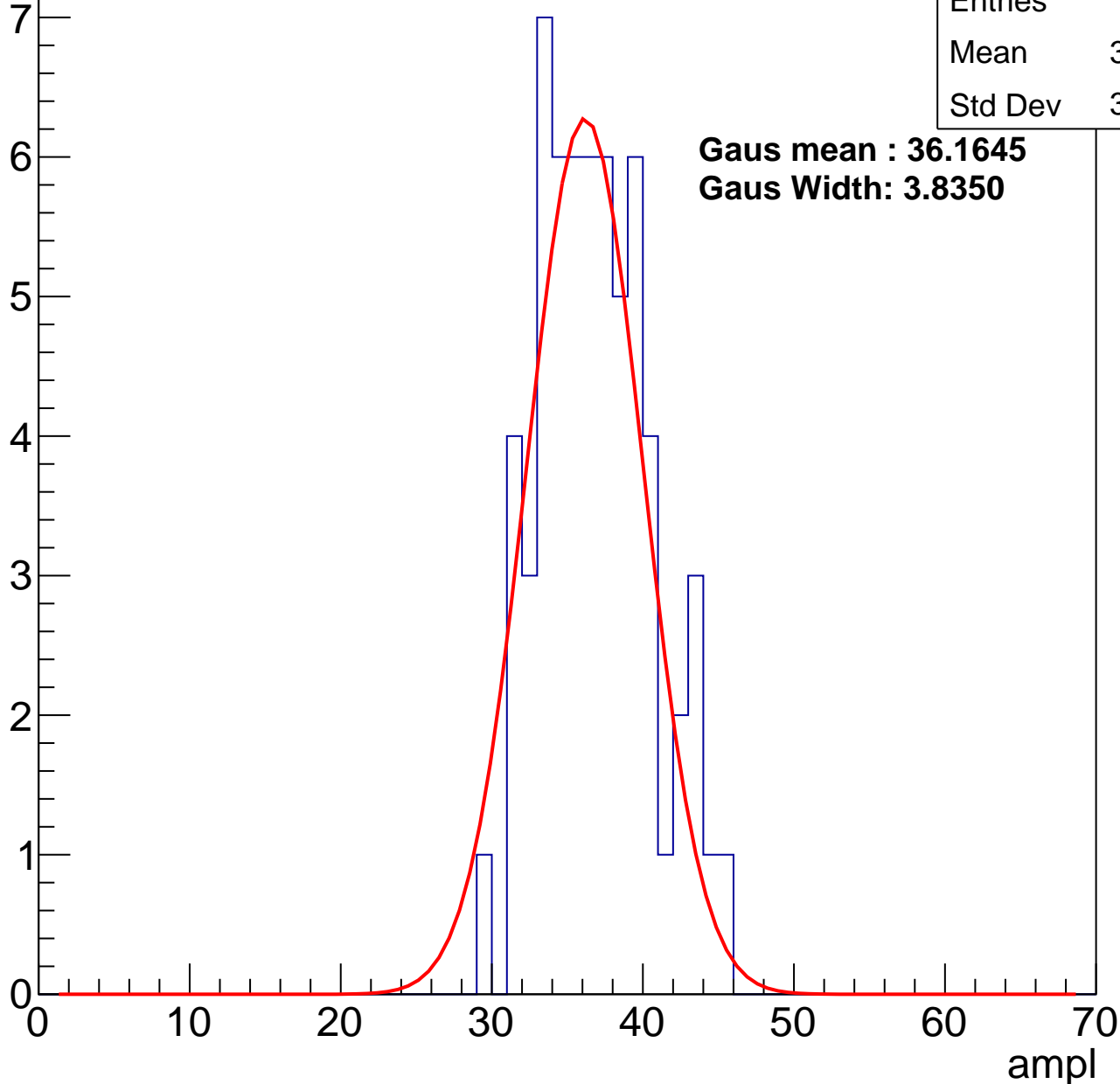
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	36.44
Std Dev	3.617

**Gaus mean : 36.1645**

**Gaus Width: 3.8350**

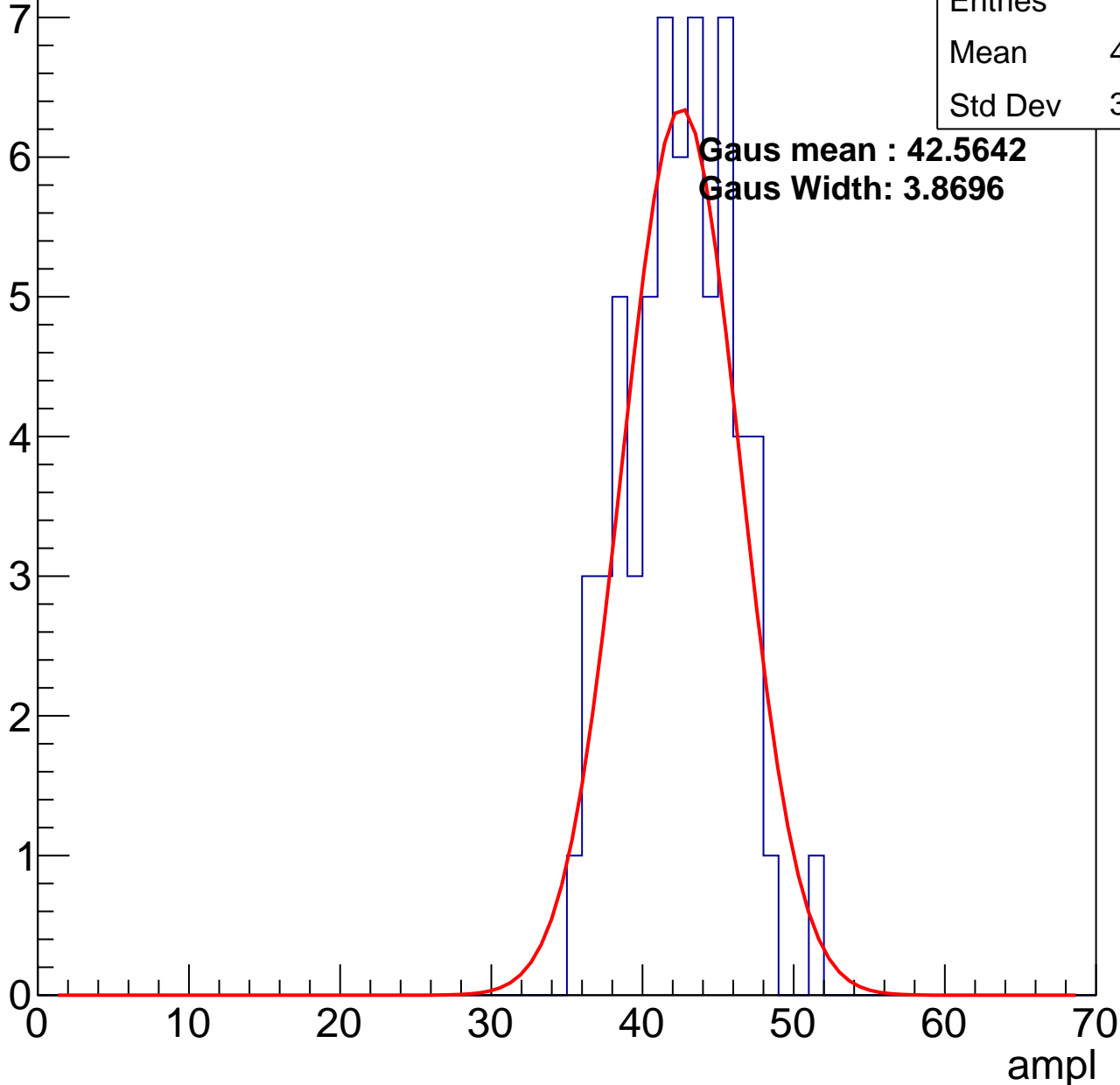


# B1L102S, U21-ch4, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

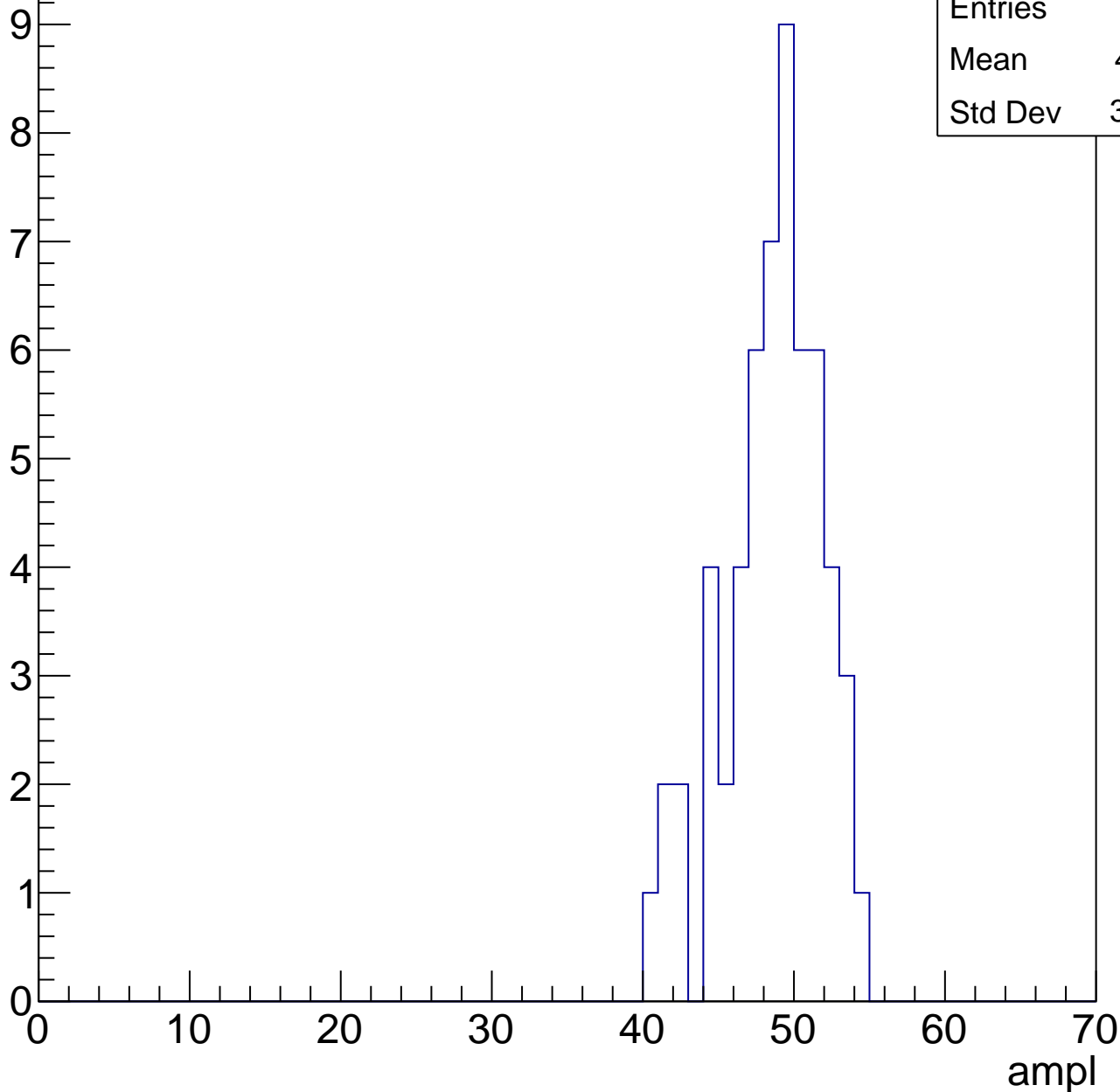
Entries	62
Mean	42.05
Std Dev	3.447



# B1L102S, U21-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



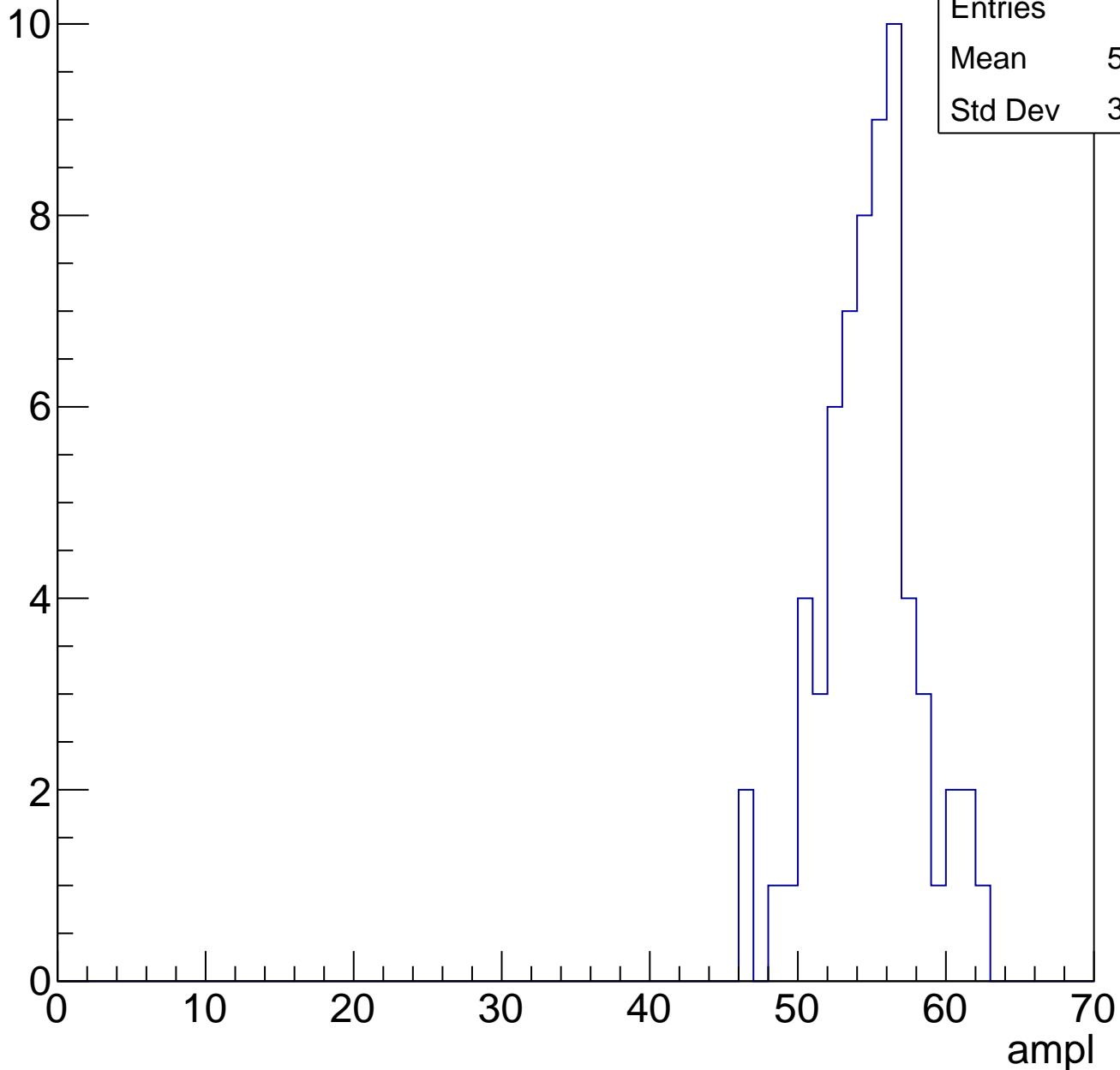
Entries	57
Mean	48.11
Std Dev	3.243

# B1L102S, U21-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	64
Mean	54.33
Std Dev	3.298

Entry

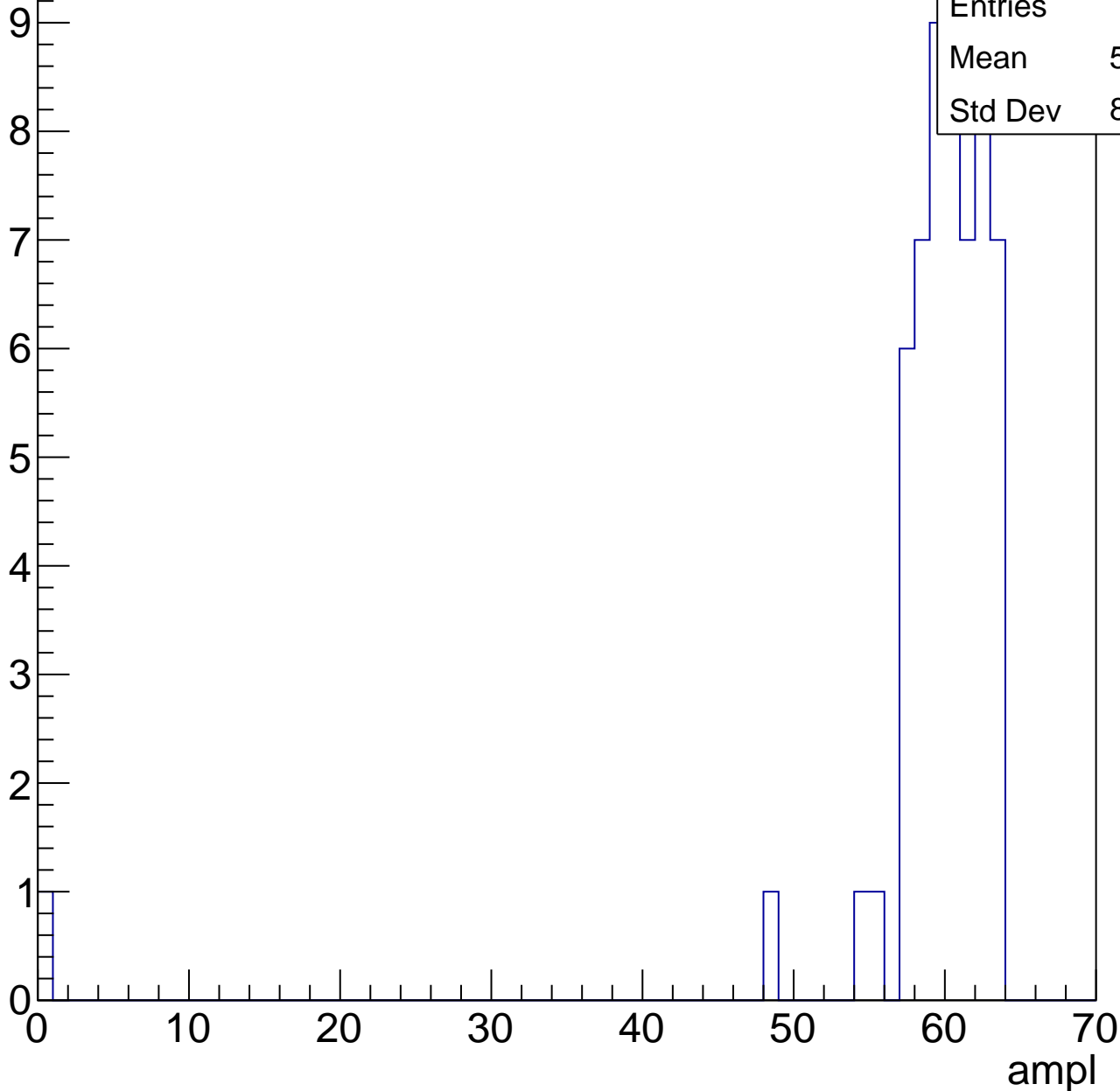


# B1L102S, U21-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	58.57
Std Dev	8.328



# B1L102S, U21-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch5, adc0

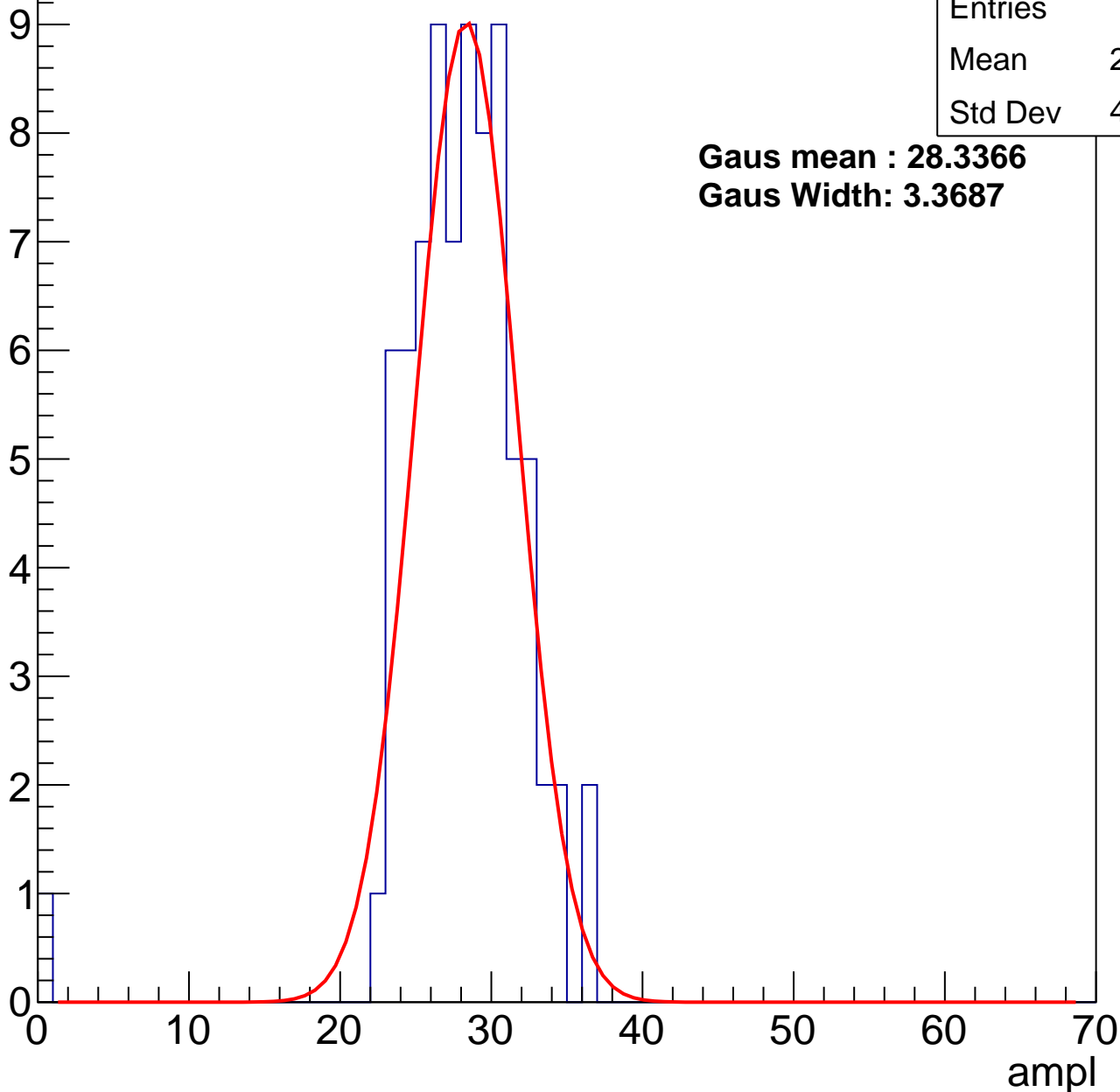
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	27.56
Std Dev	4.466

**Gaus mean : 28.3366**

**Gaus Width: 3.3687**



# B1L102S, U21-ch5, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	78
Mean	35.74
Std Dev	3.553

**Gaus mean : 36.6072**

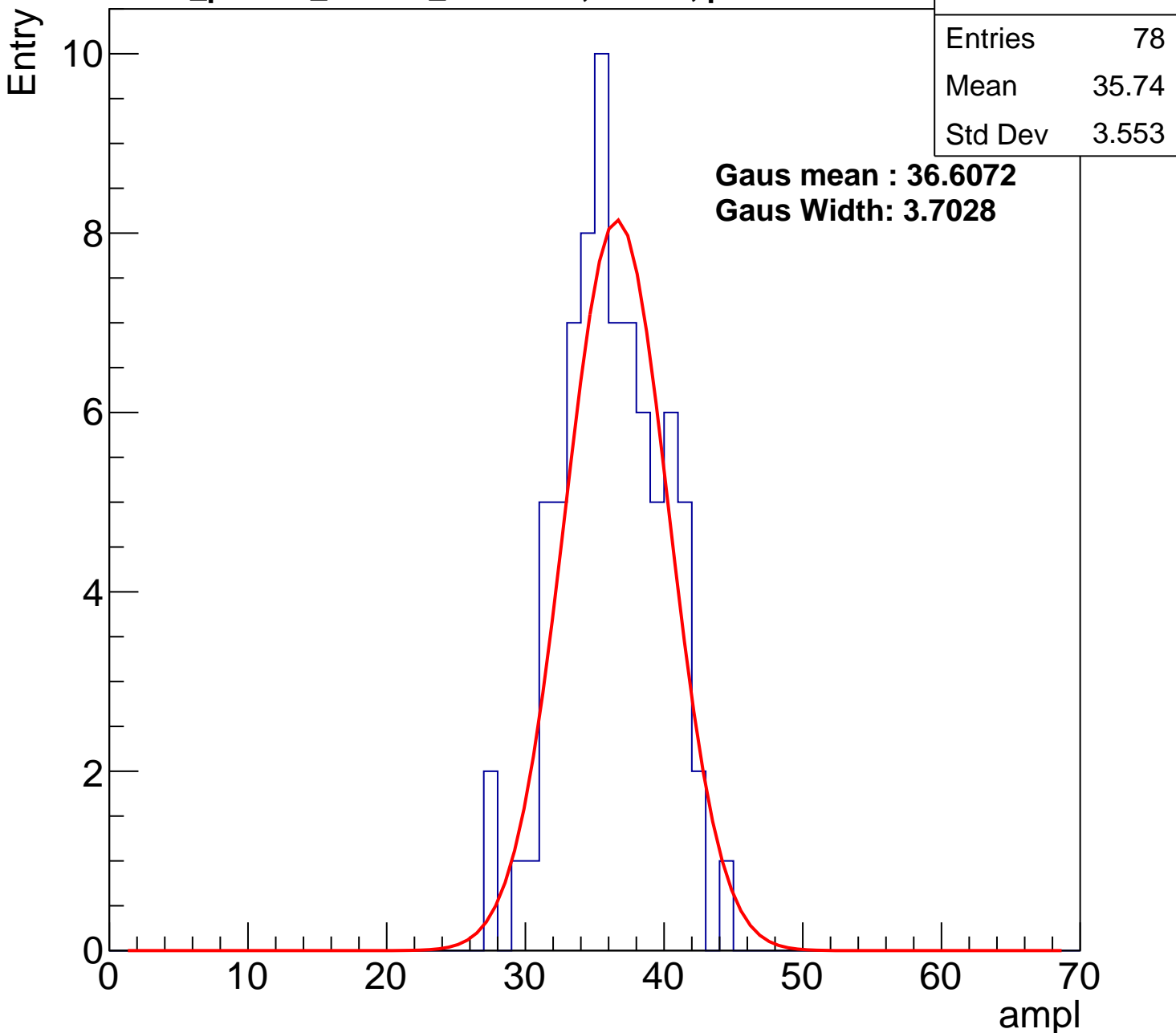
**Gaus Width: 3.7028**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U21-ch5, adc2

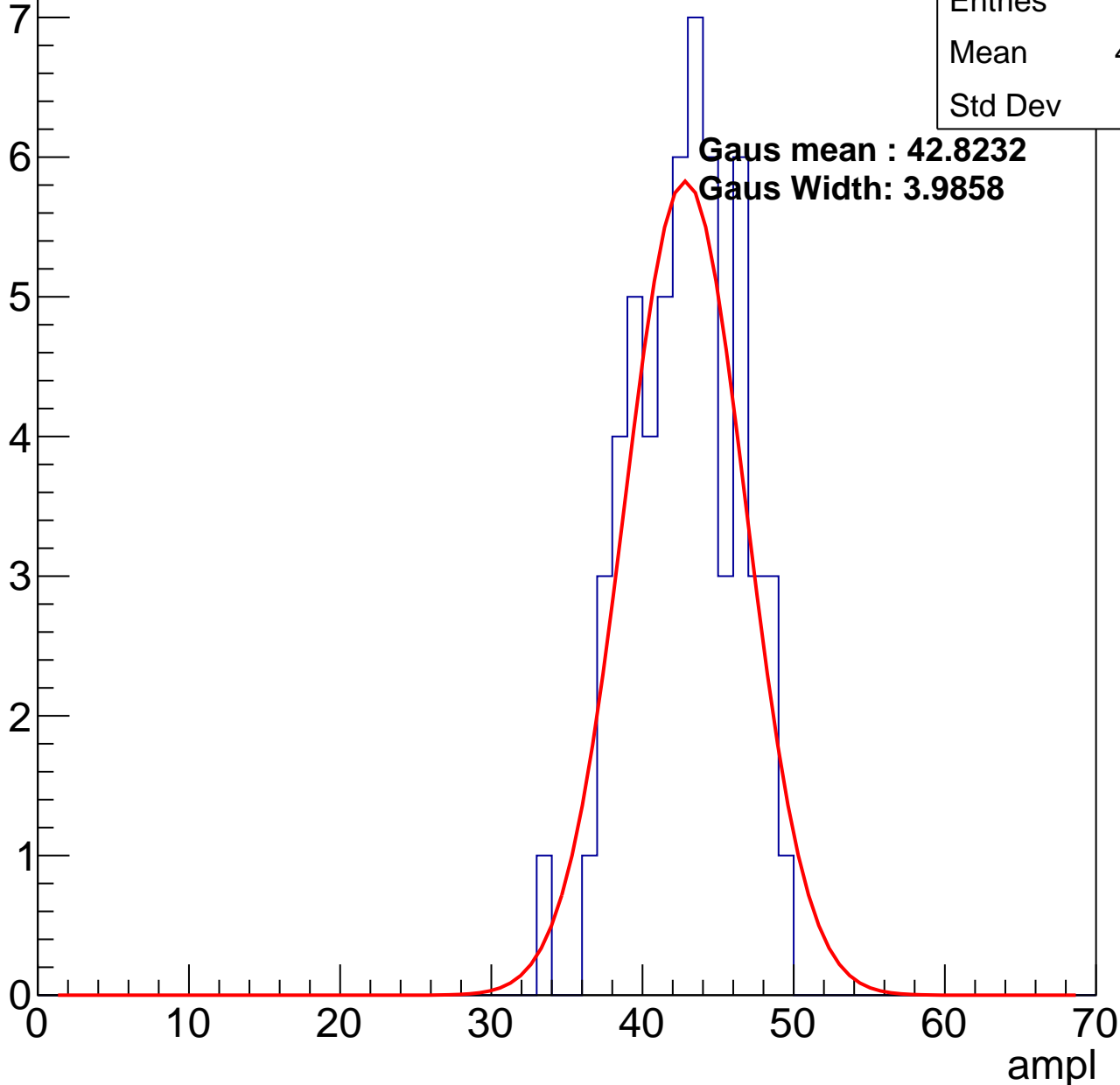
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	42.31
Std Dev	3.48

**Gaus mean : 42.8232**

**Gaus Width: 3.9858**



# B1L102S, U21-ch5, adc3

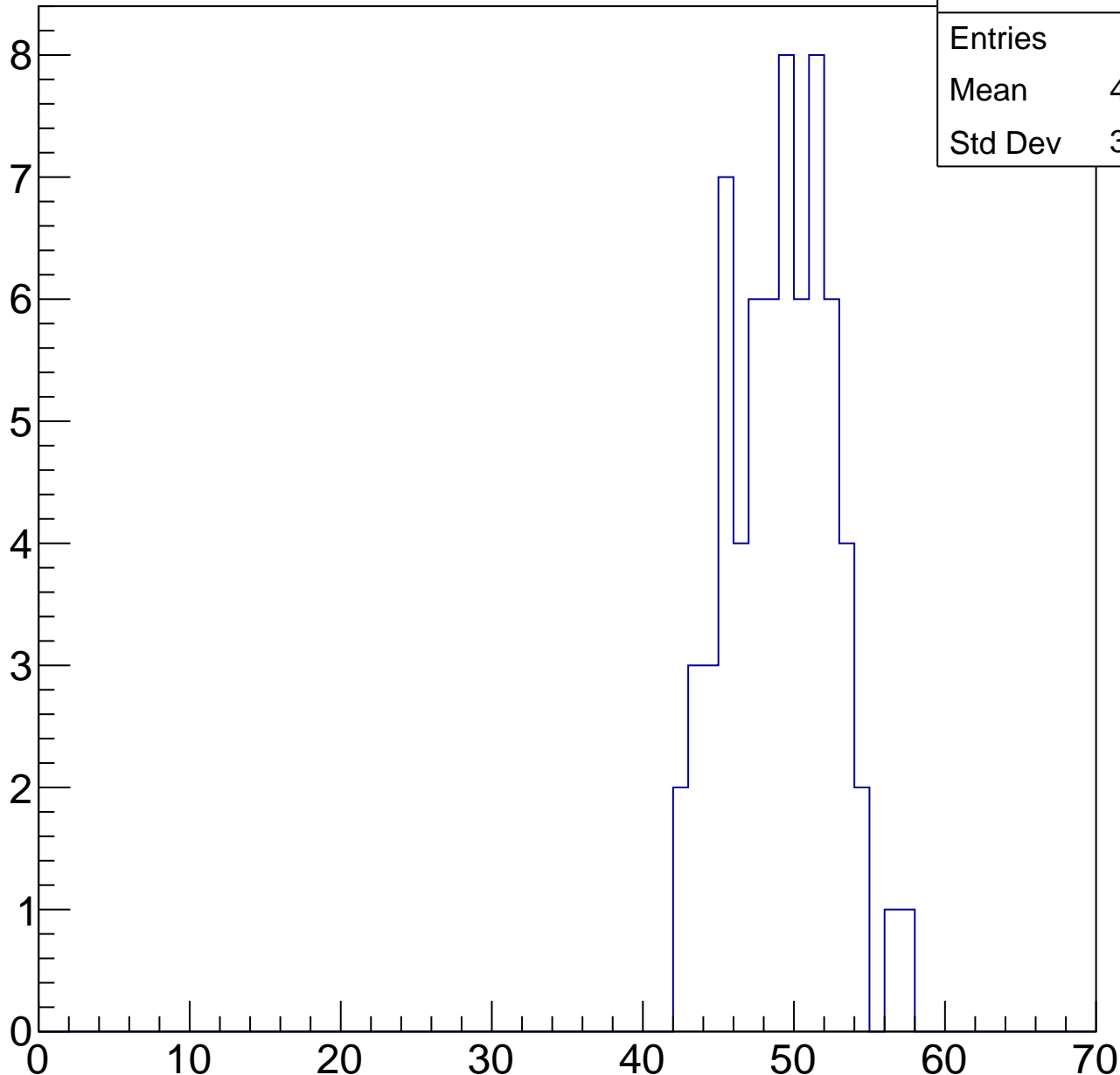
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	67
Mean	48.64
Std Dev	3.389

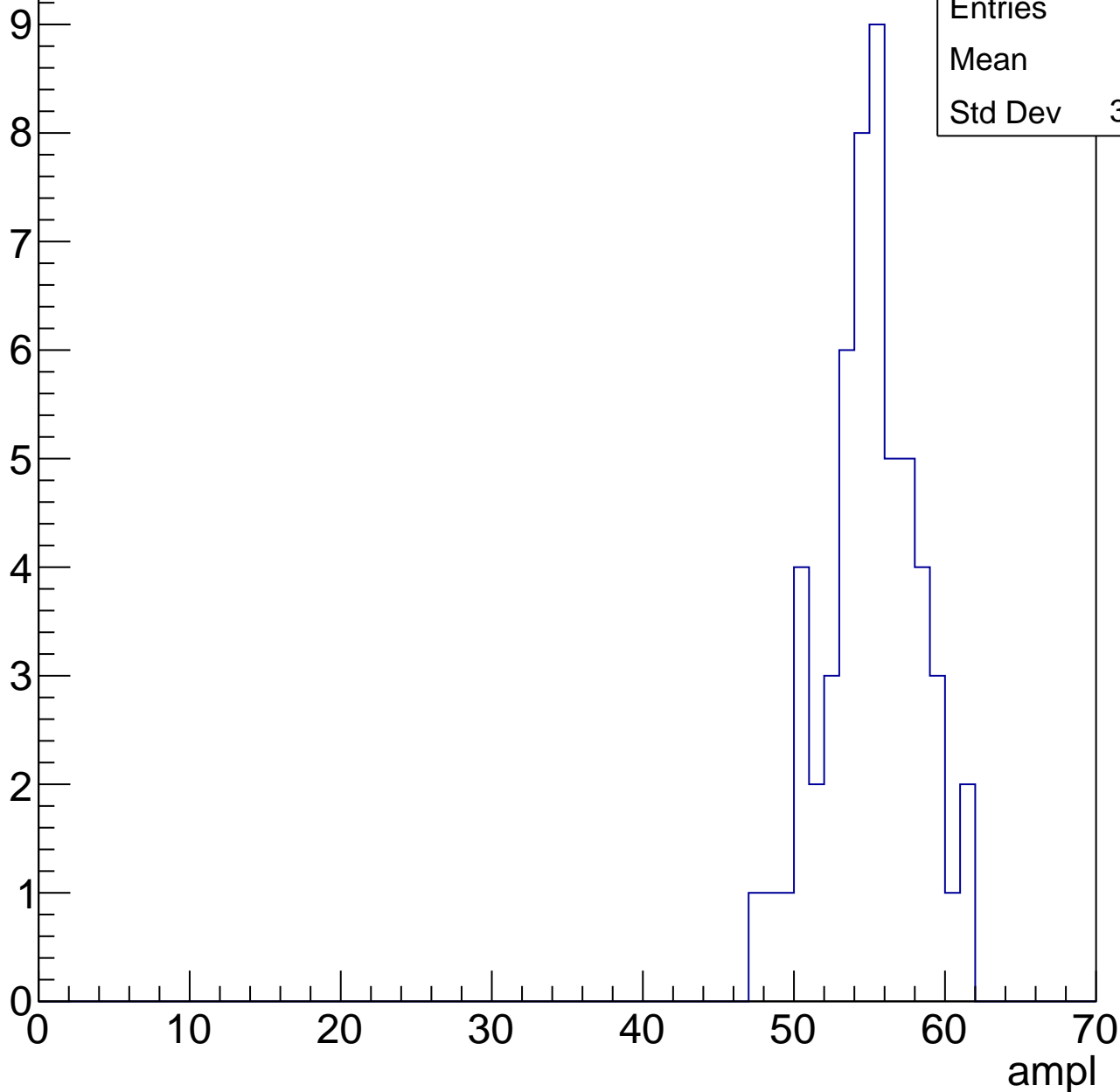
ampl



# B1L102S, U21-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

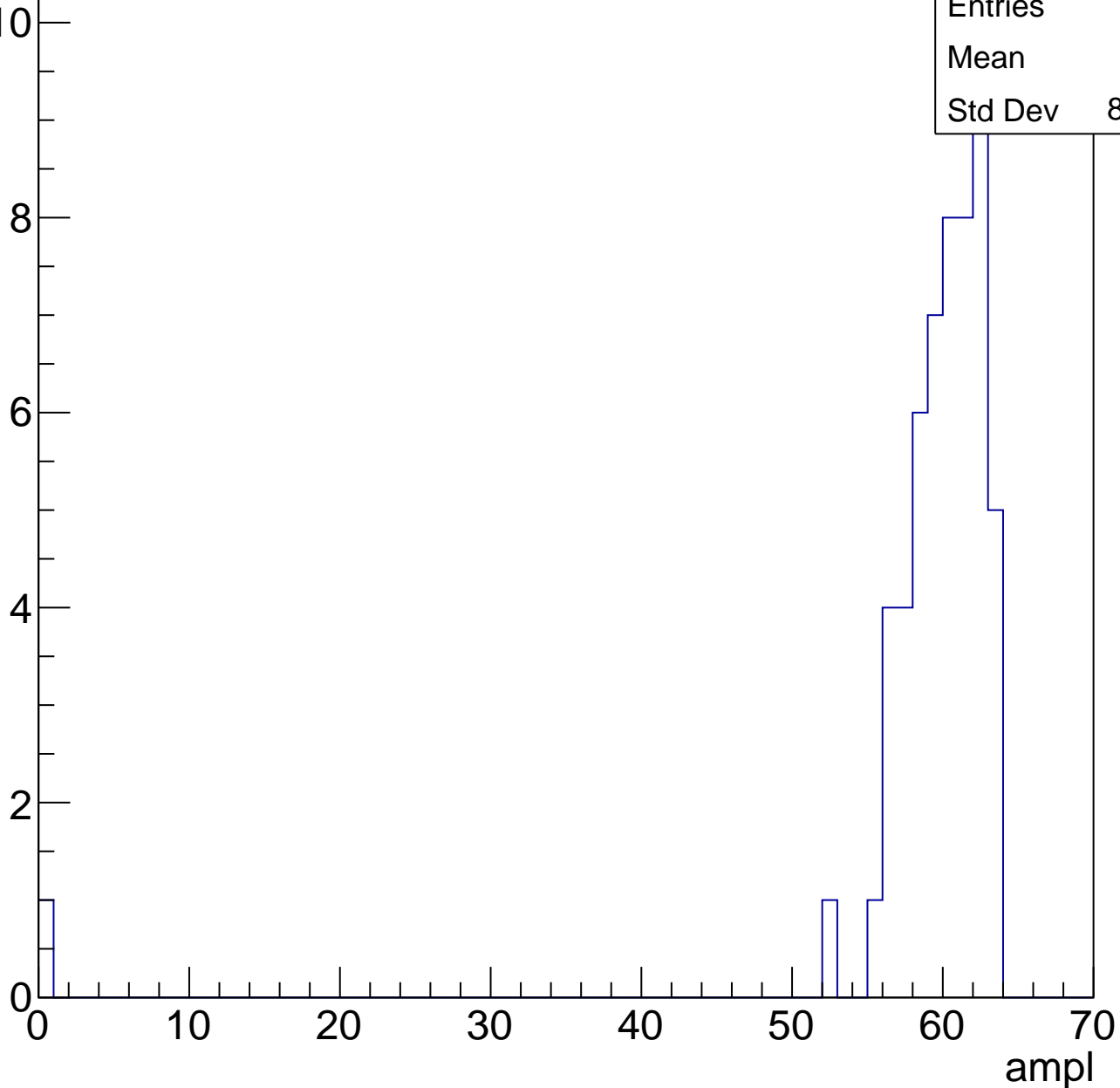


# B1L102S, U21-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	58.6
Std Dev	8.318

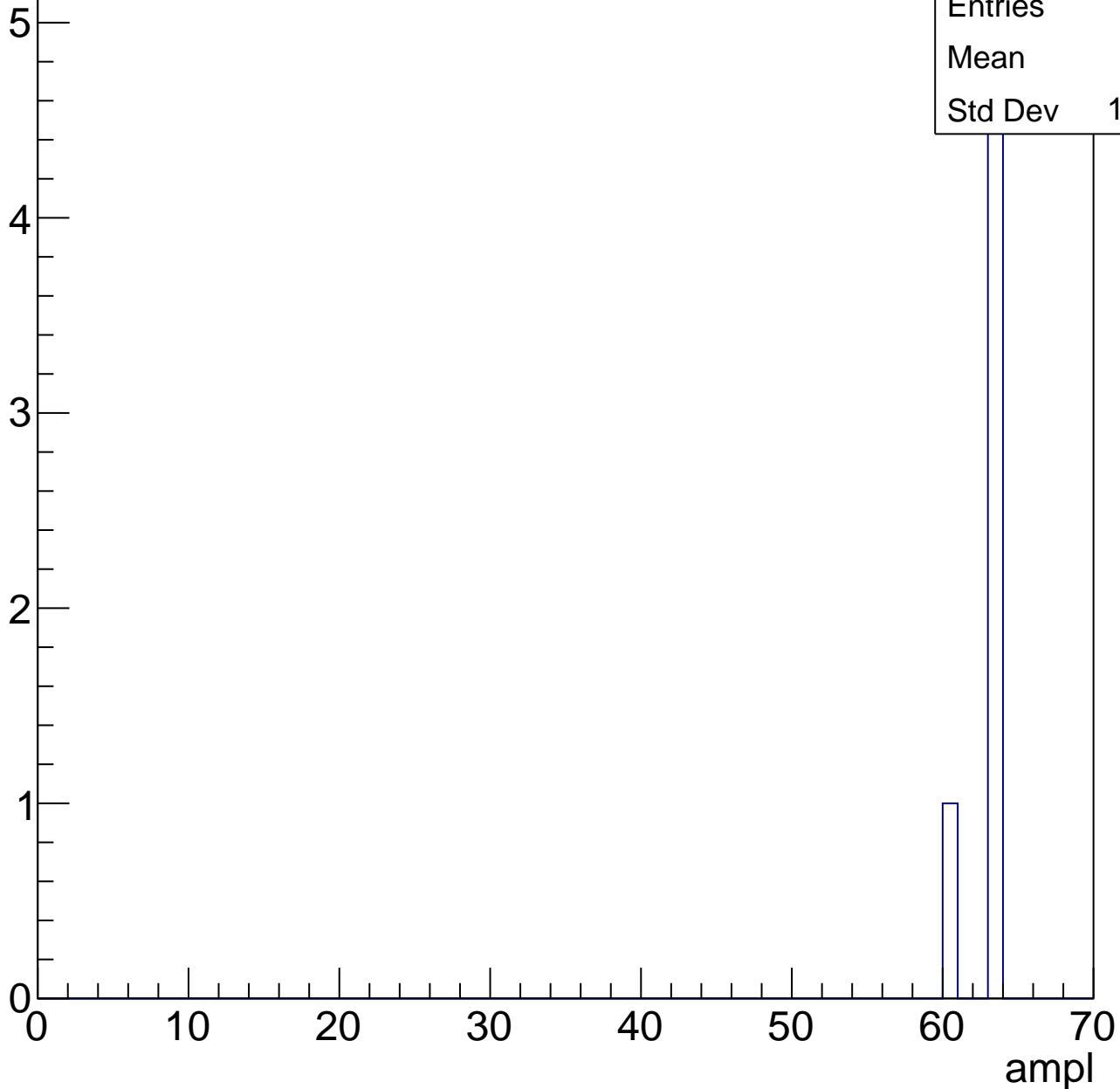


# B1L102S, U21-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	6
Mean	62.5
Std Dev	1.118





# B1L102S, U21-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch6, adc0

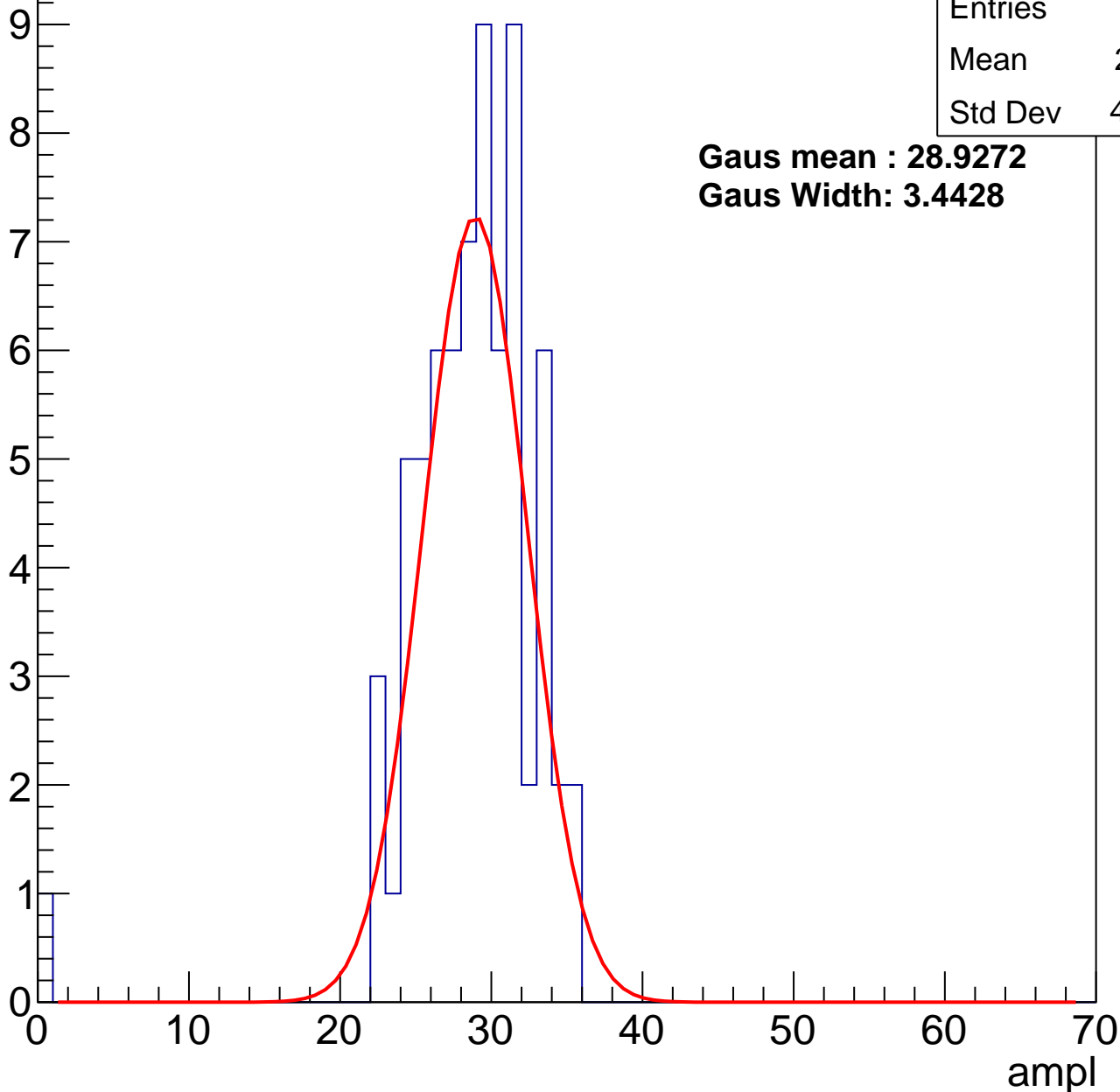
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	28.11
Std Dev	4.686

**Gaus mean : 28.9272**

**Gaus Width: 3.4428**



# B1L102S, U21-ch6, adc1

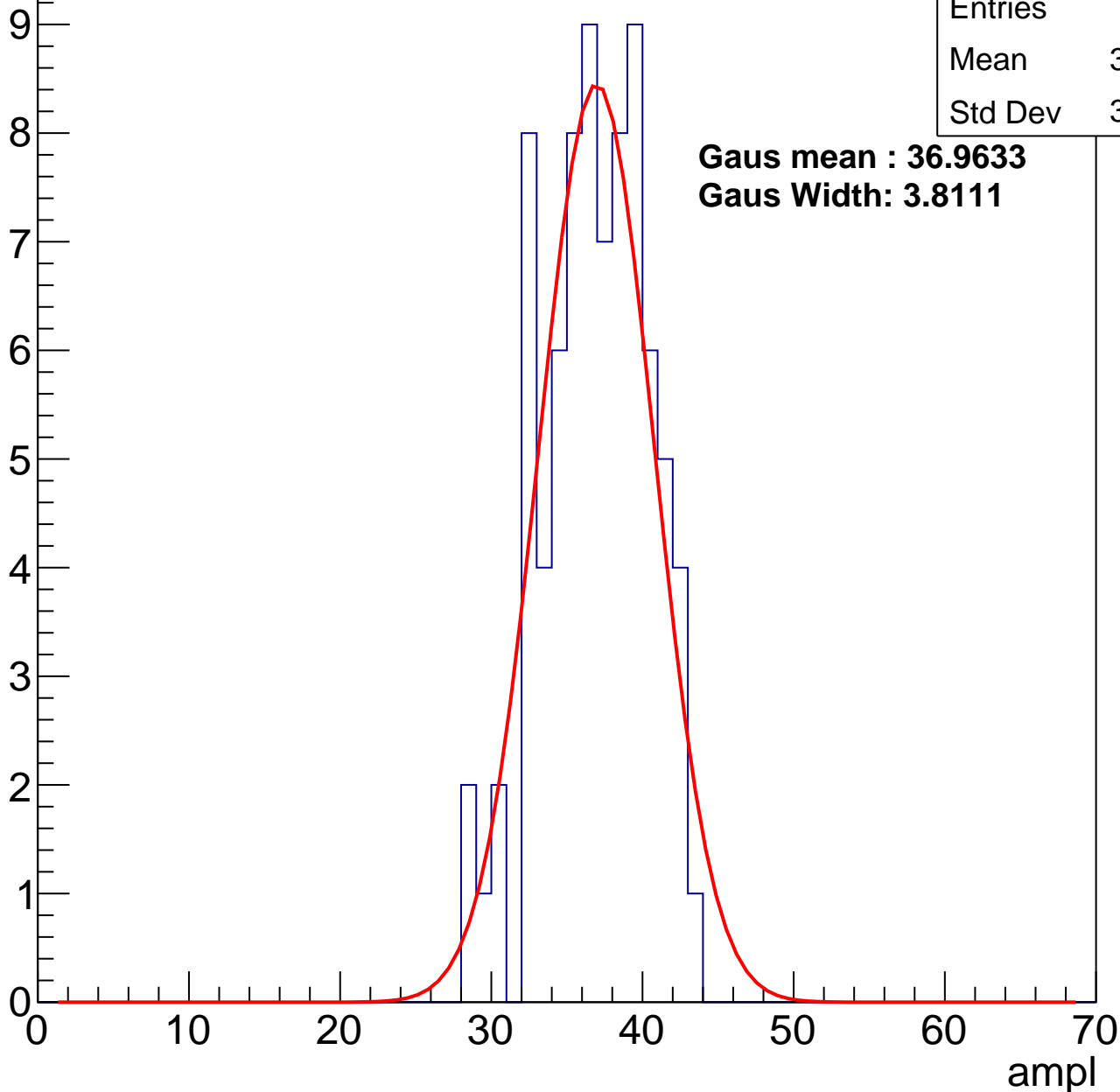
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	36.39
Std Dev	3.477

**Gaus mean : 36.9633**

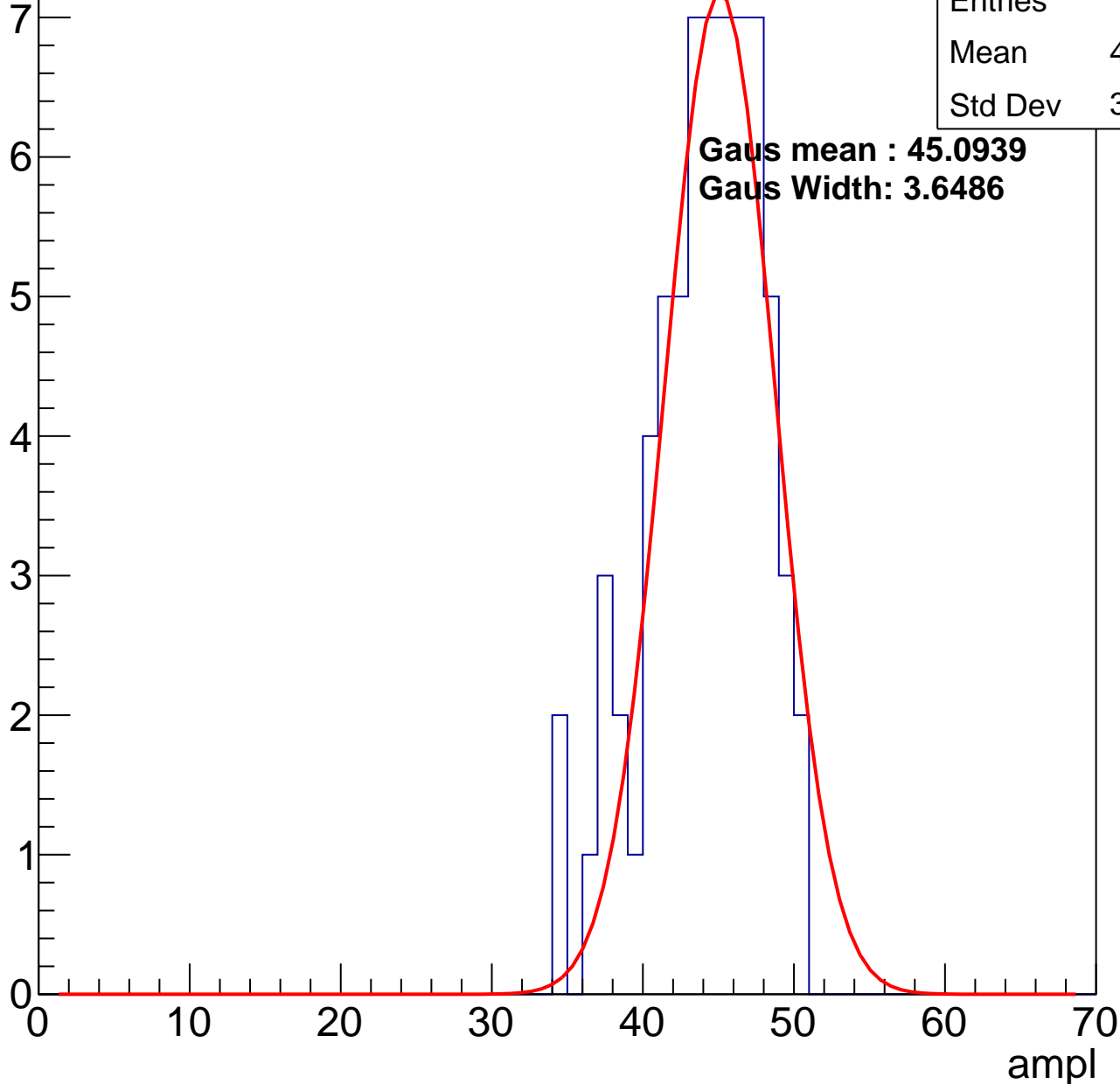
**Gaus Width: 3.8111**



# B1L102S, U21-ch6, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

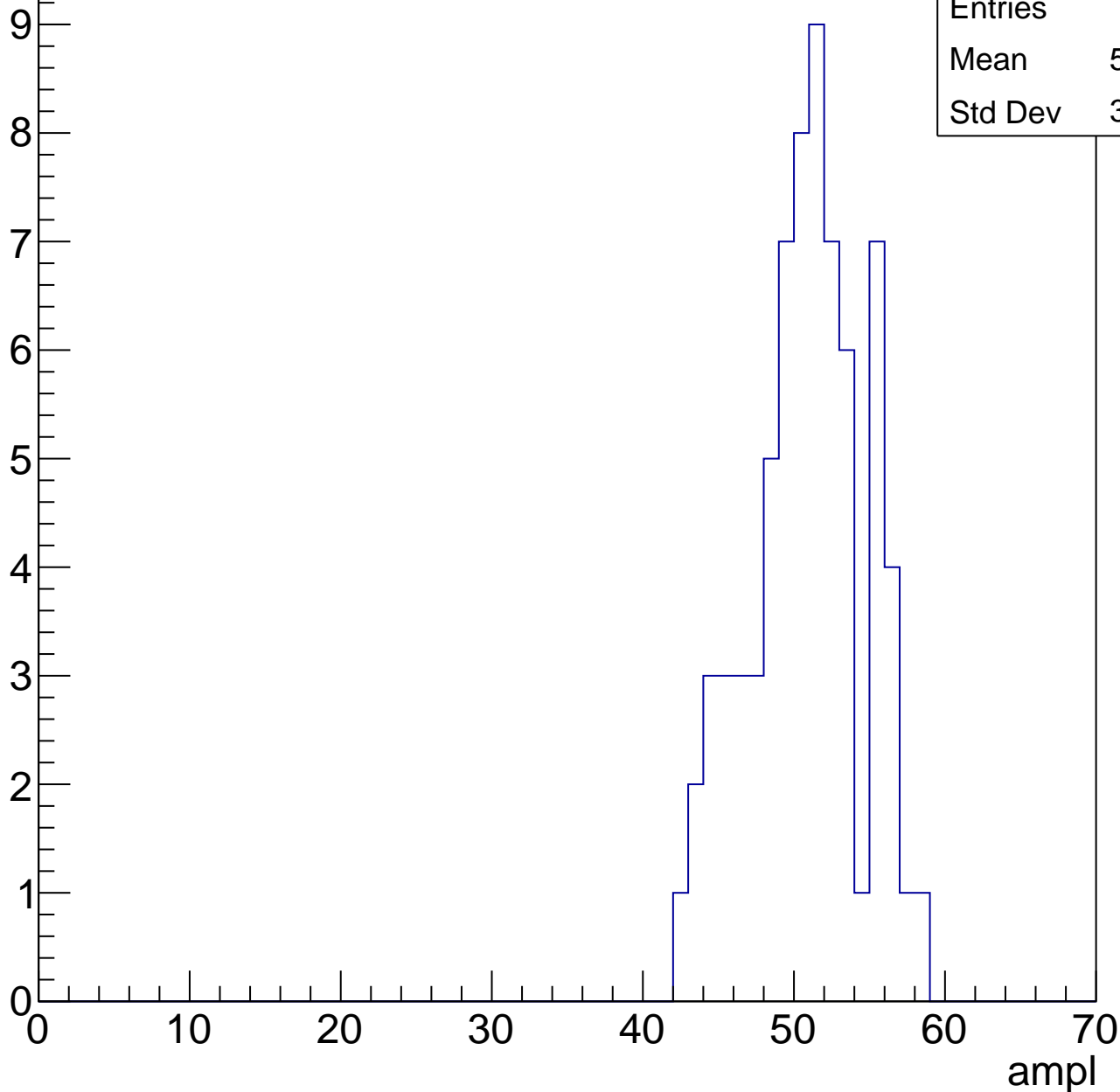
Entry



# B1L102S, U21-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



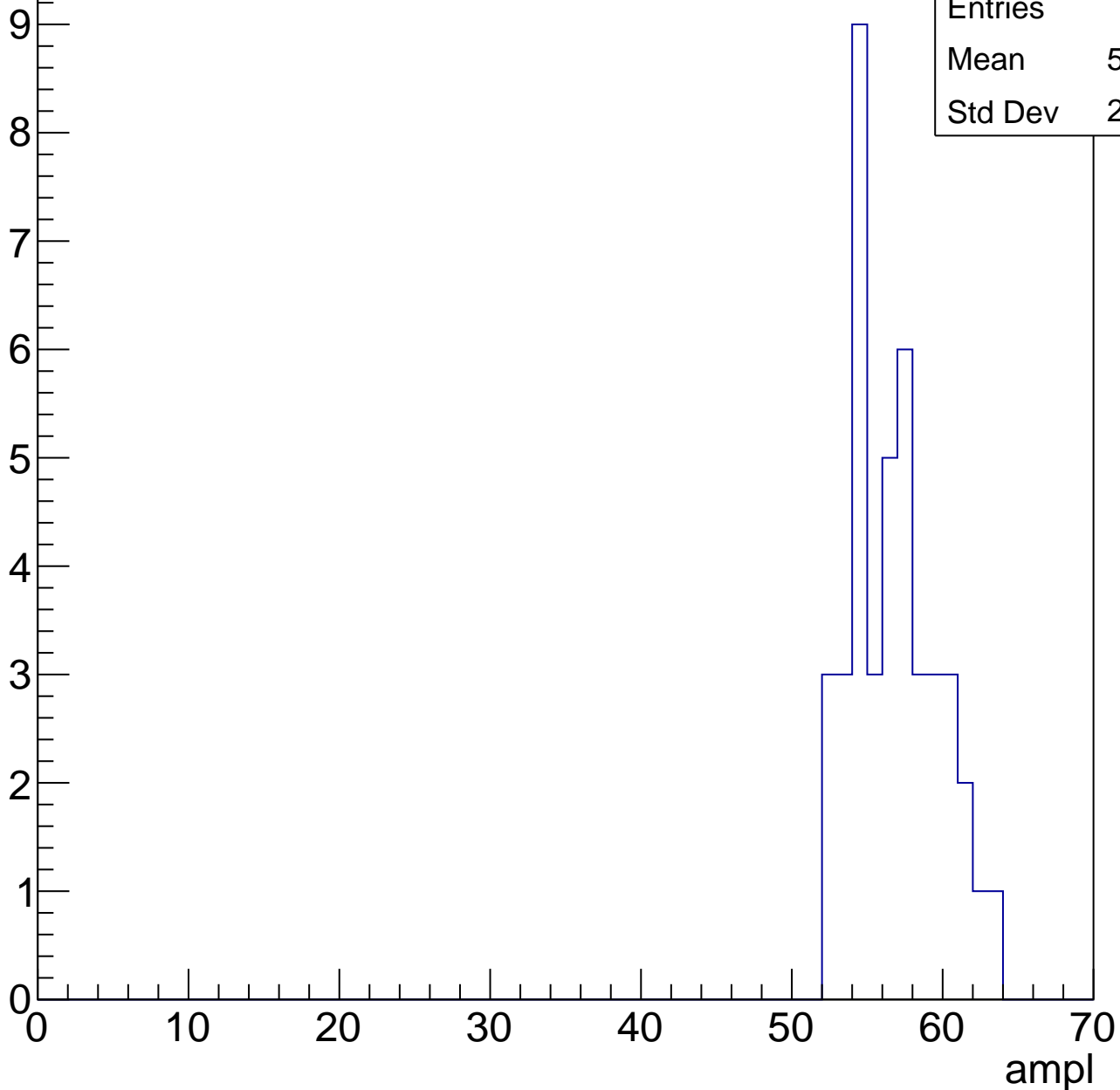
Entries	71
Mean	50.37
Std Dev	3.709

# B1L102S, U21-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	42
Mean	56.33
Std Dev	2.834

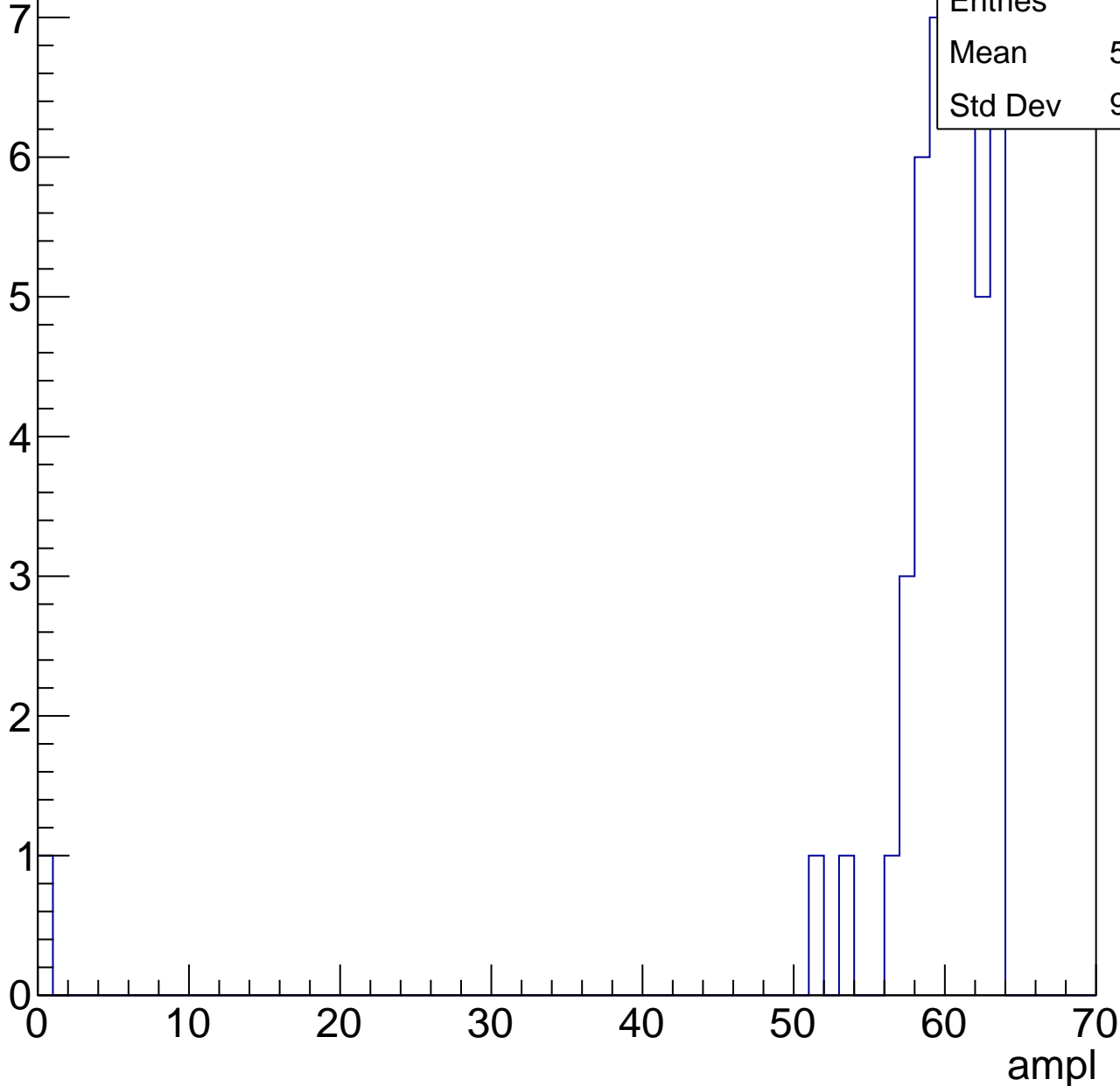


# B1L102S, U21-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

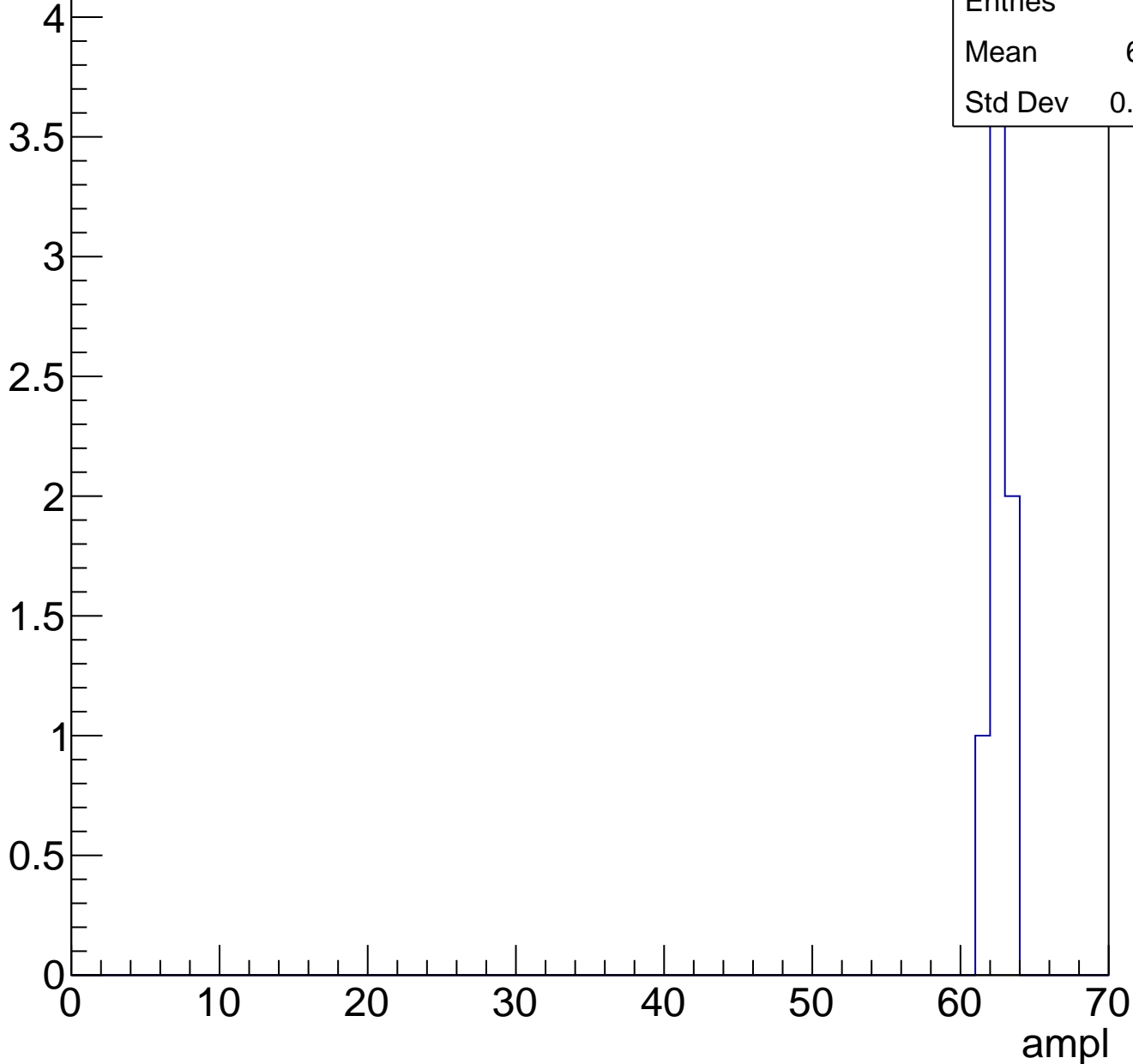
Entries	46
Mean	58.48
Std Dev	9.074



# B1L102S, U21-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	10
Std Dev	10

# B1L102S, U21-ch7, adc0

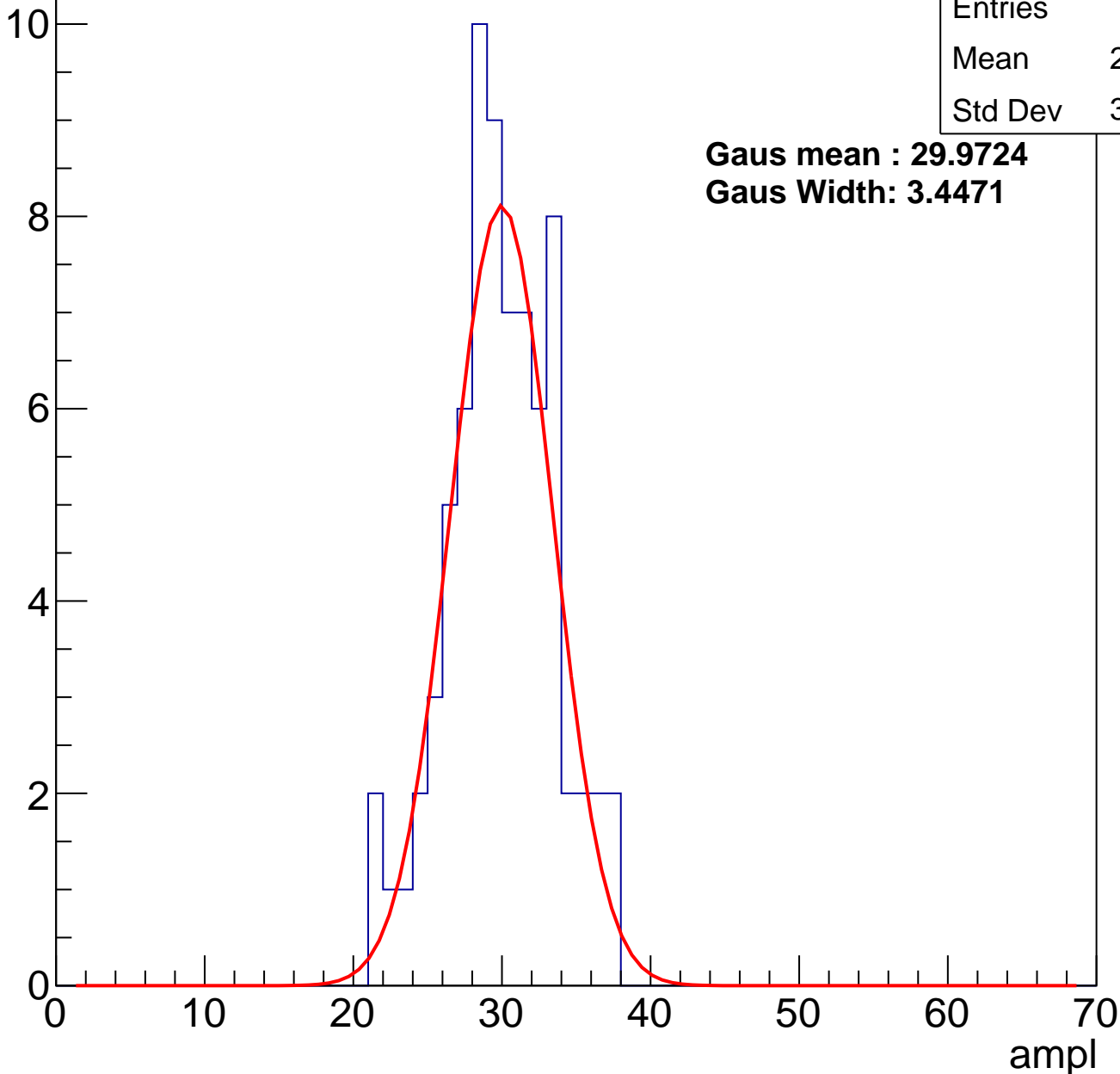
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	75
Mean	29.47
Std Dev	3.538

**Gaus mean : 29.9724**

**Gaus Width: 3.4471**

Entry



# B1L102S, U21-ch7, adc1

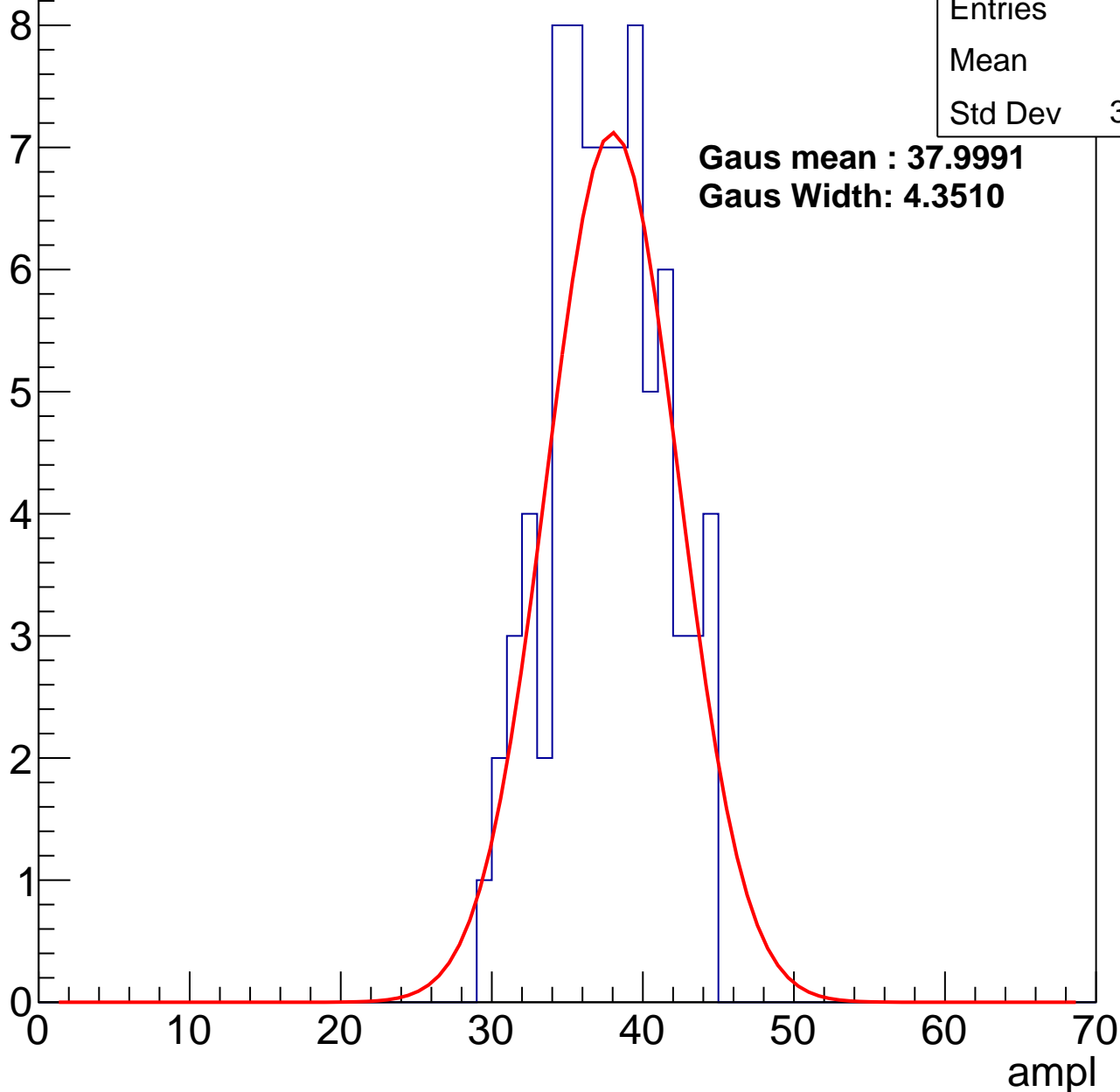
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	37.1
Std Dev	3.706

**Gaus mean : 37.9991**

**Gaus Width: 4.3510**



# B1L102S, U21-ch7, adc2

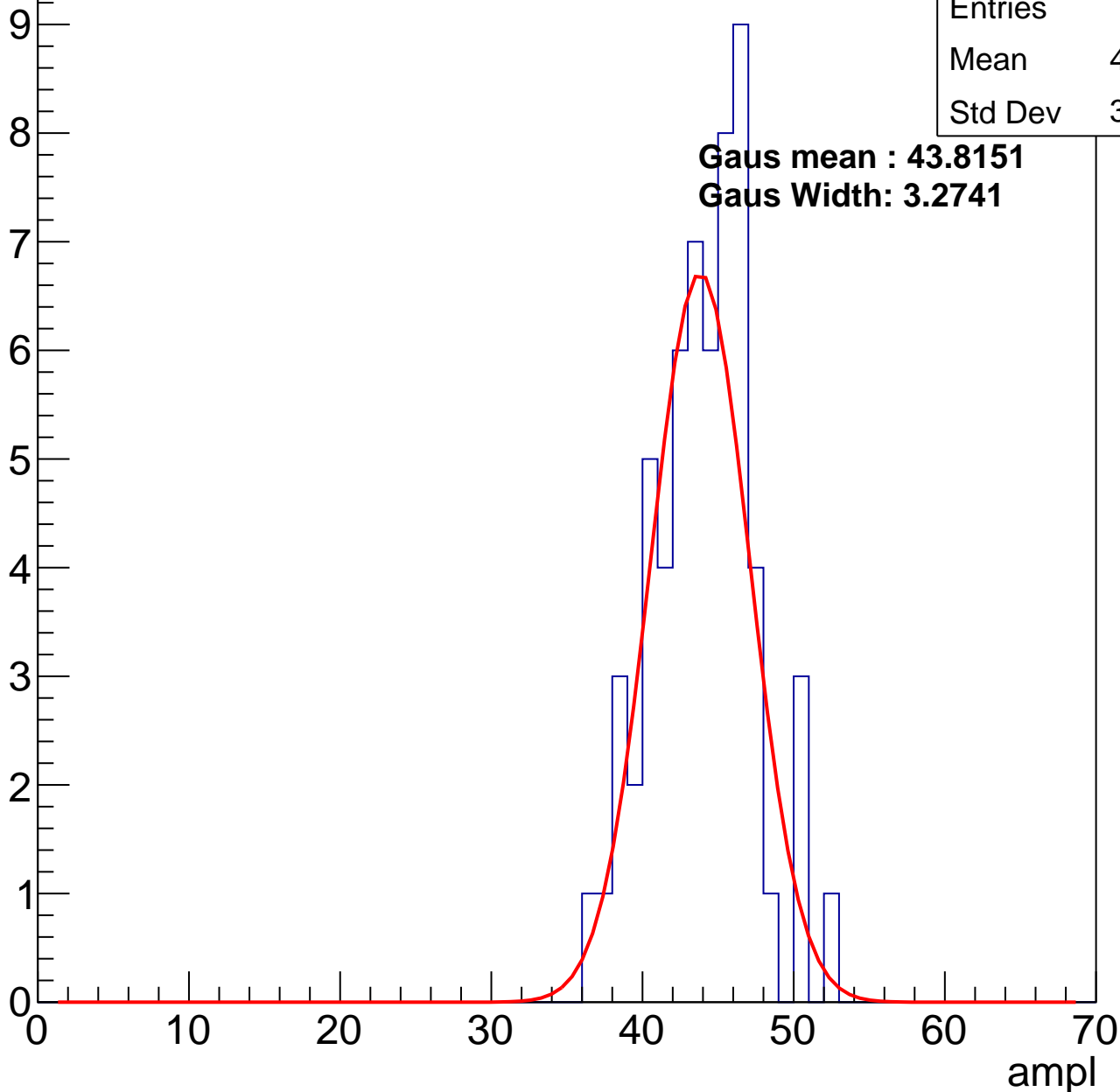
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	43.57
Std Dev	3.326

**Gaus mean : 43.8151**

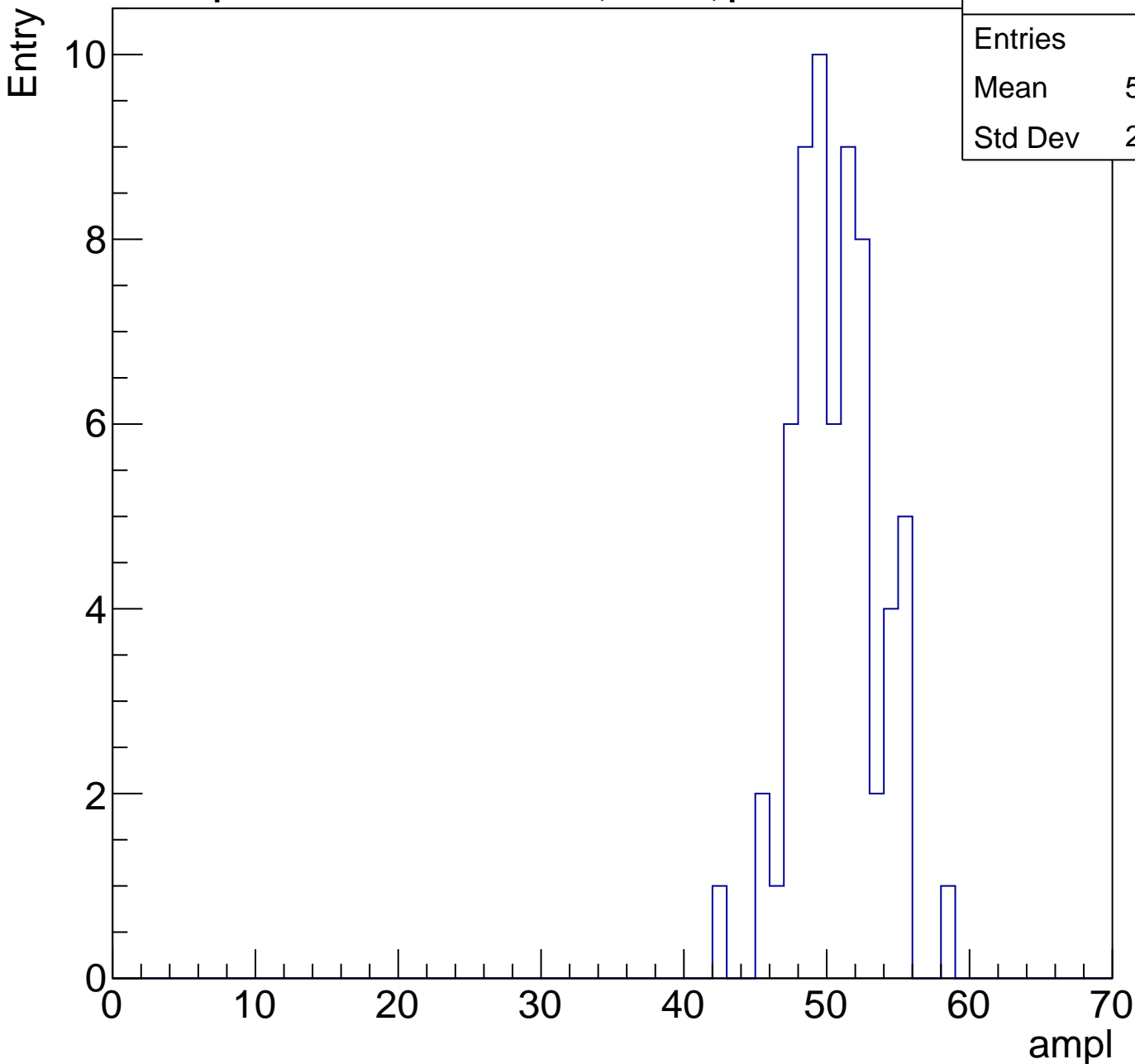
**Gaus Width: 3.2741**



# B1L102S, U21-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	64
Mean	50.19
Std Dev	2.904

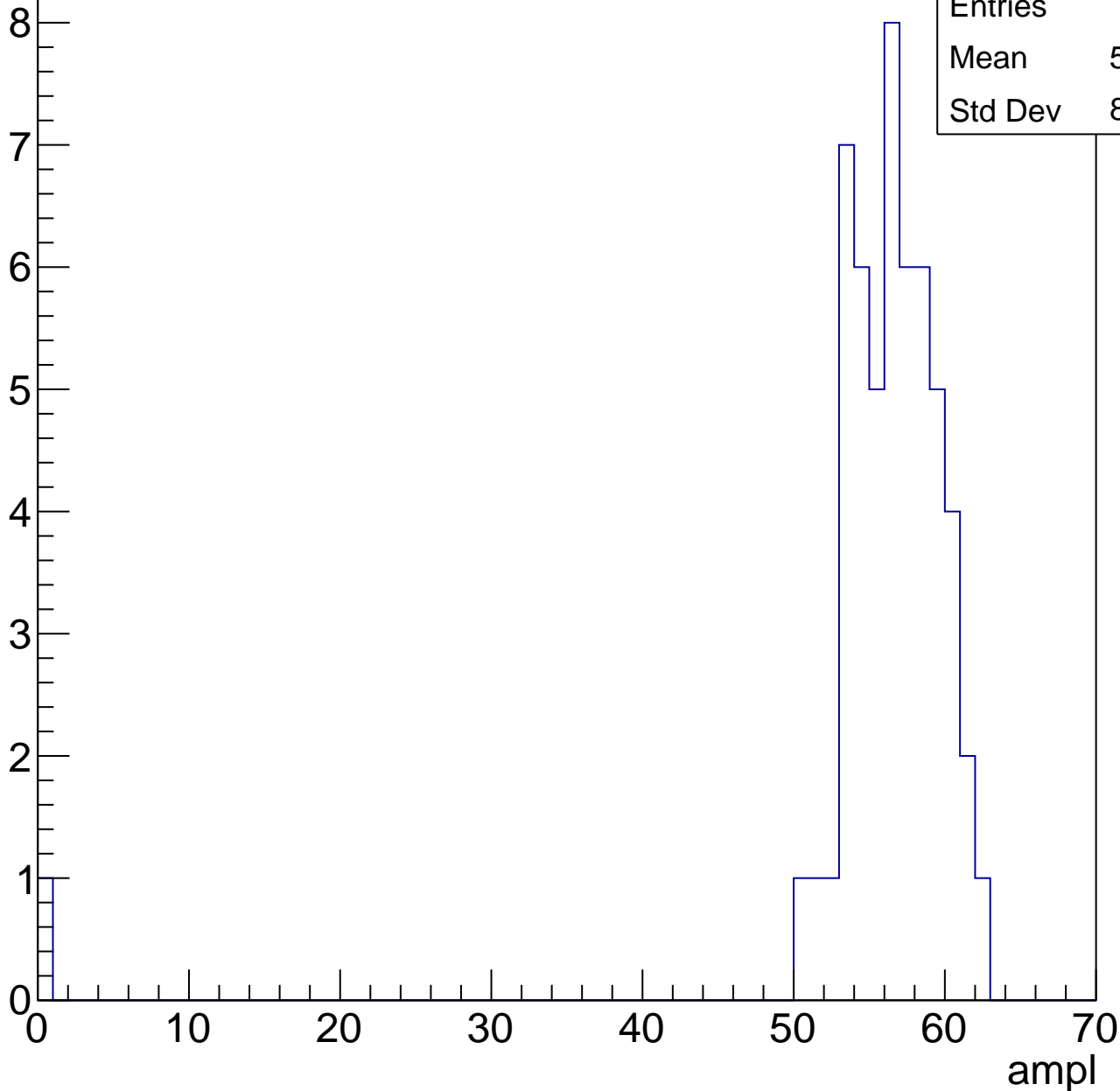


# B1L102S, U21-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	55.19
Std Dev	8.044

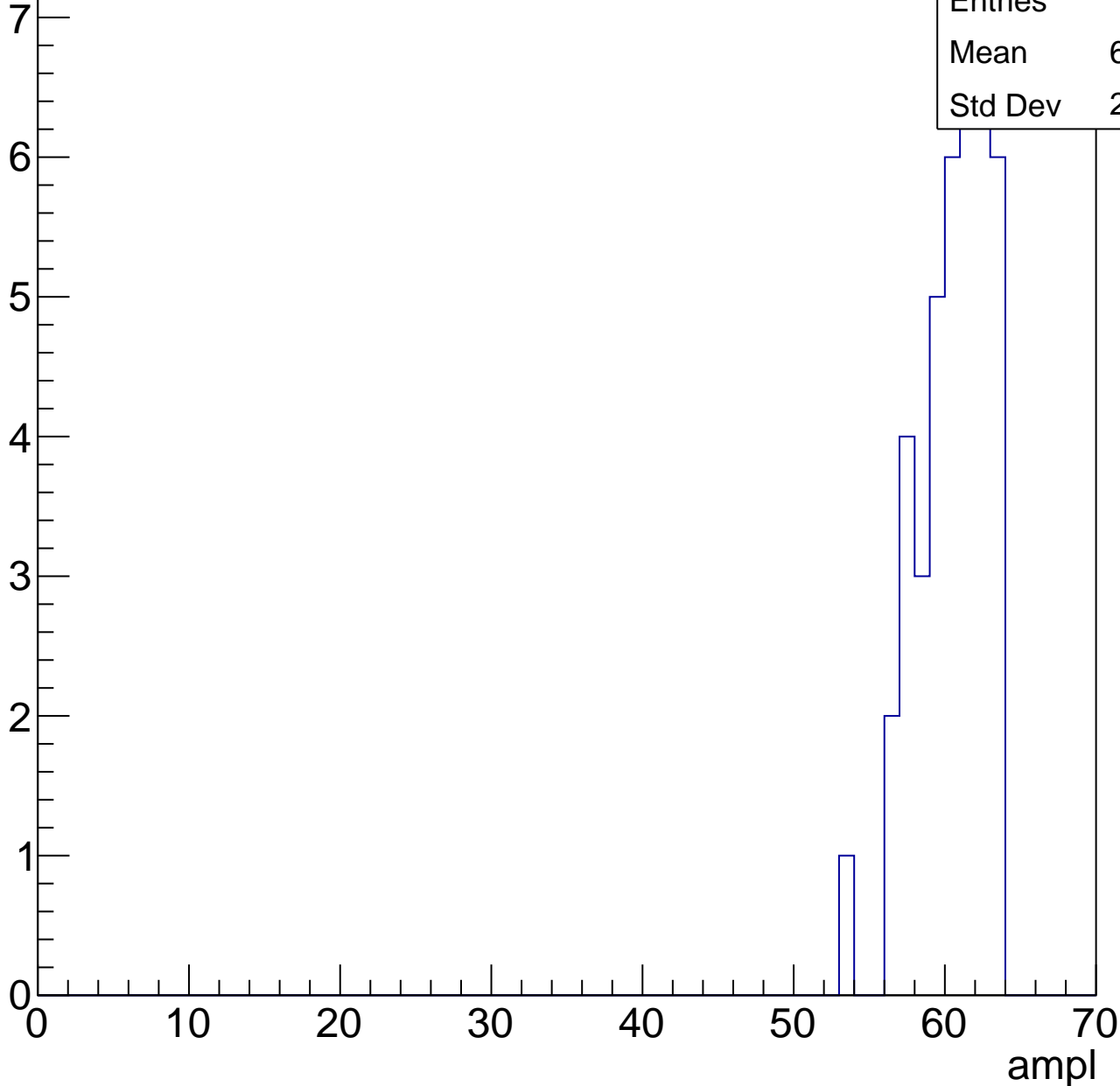


# B1L102S, U21-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	41
Mean	60.02
Std Dev	2.332



# B1L102S, U21-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U21-ch8, adc0

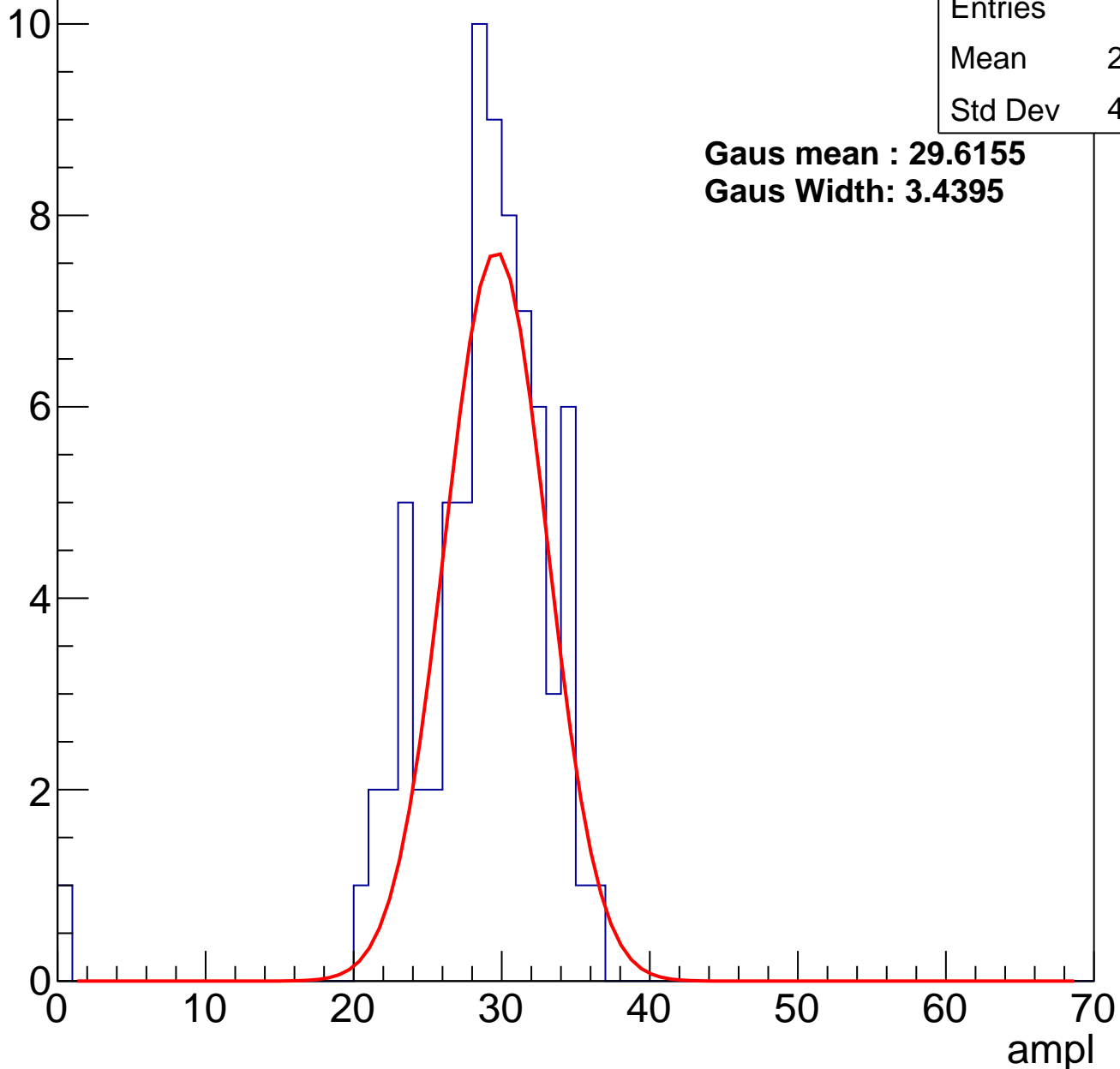
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	76
Mean	28.26
Std Dev	4.889

**Gaus mean : 29.6155**

**Gaus Width: 3.4395**

Entry



# B1L102S, U21-ch8, adc1

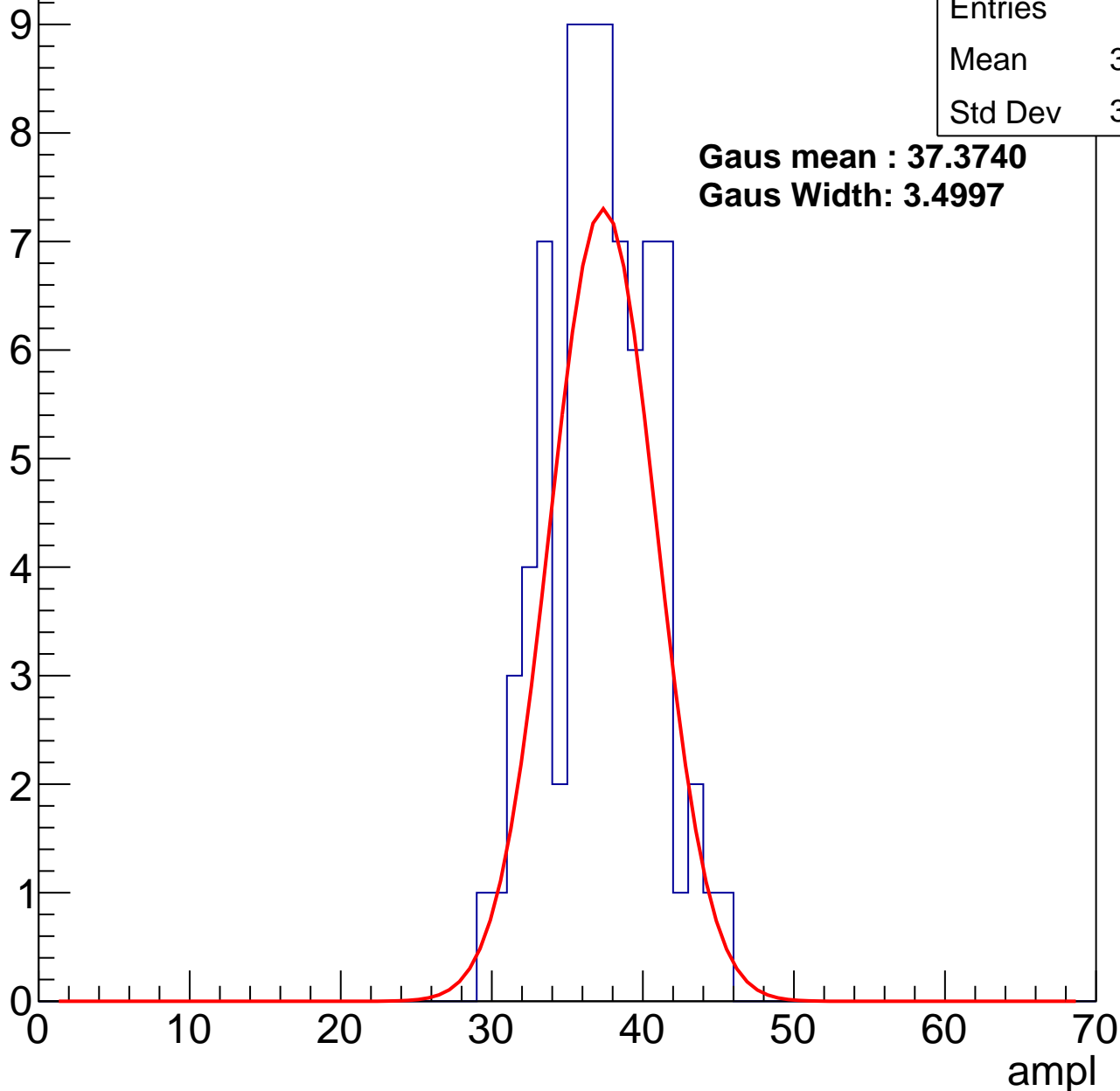
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	36.82
Std Dev	3.437

**Gaus mean : 37.3740**

**Gaus Width: 3.4997**



# B1L102S, U21-ch8, adc2

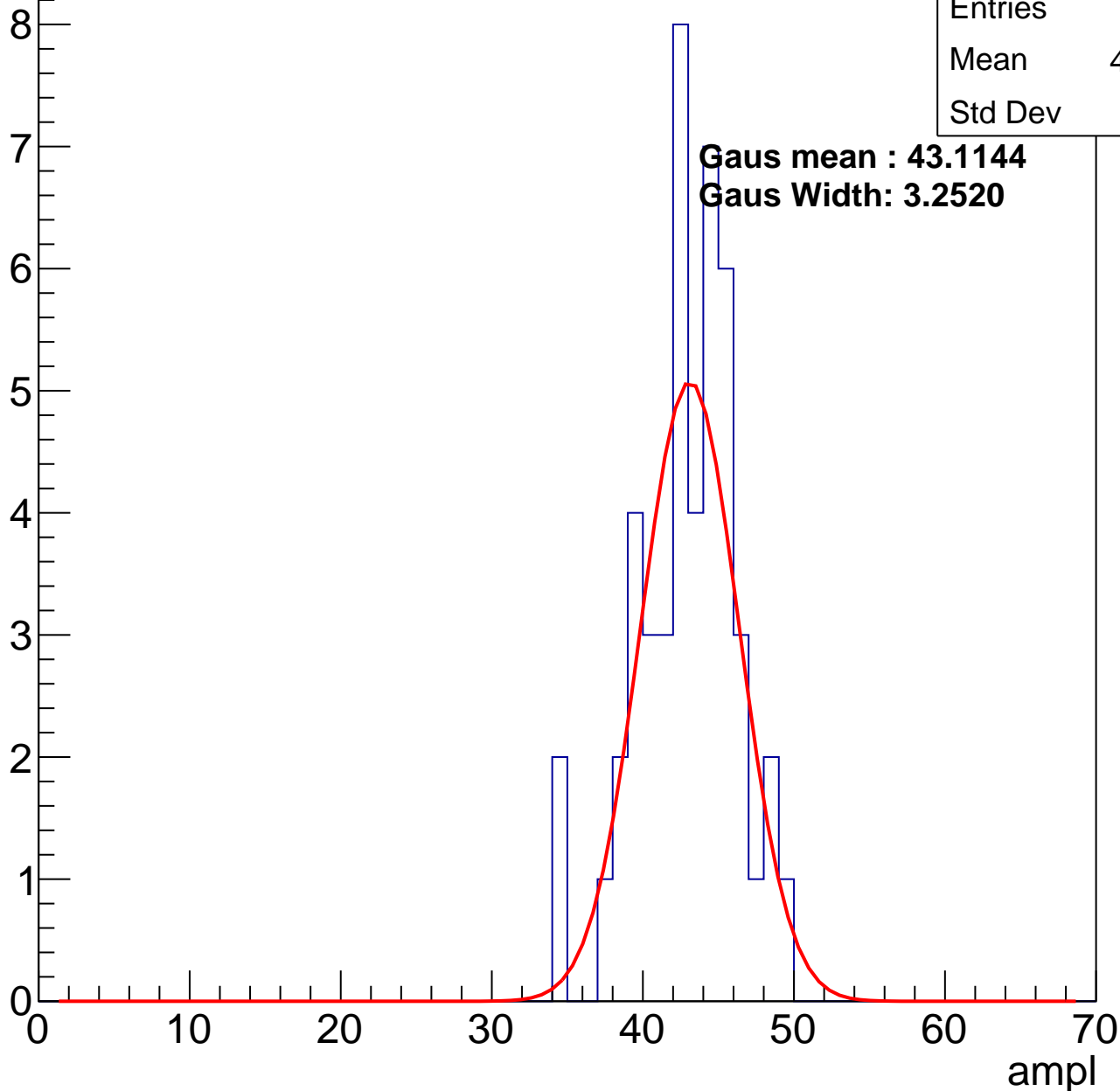
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	42.47
Std Dev	3.28

**Gaus mean : 43.1144**

**Gaus Width: 3.2520**

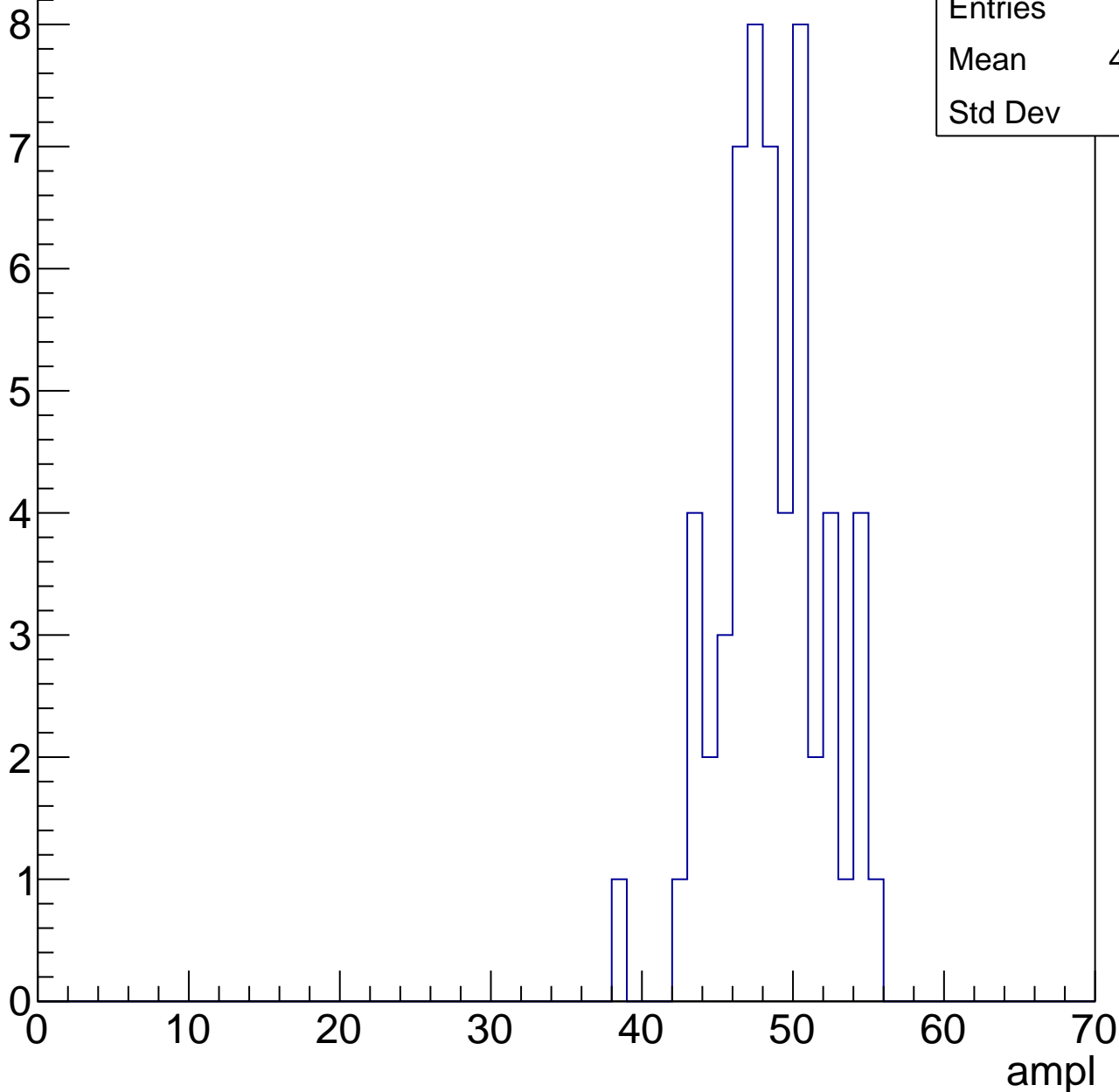


# B1L102S, U21-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	48.05
Std Dev	3.42

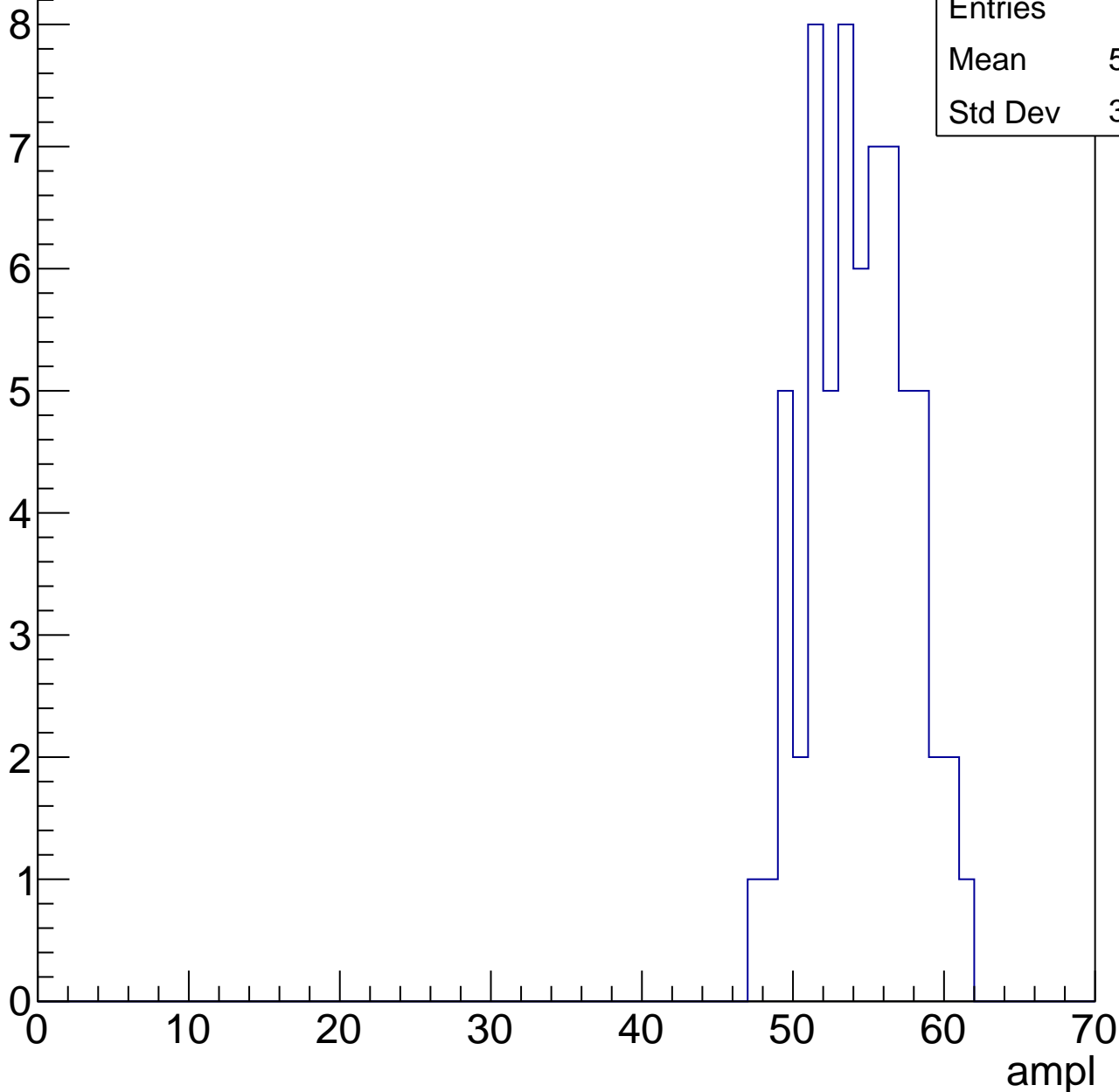


# B1L102S, U21-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	53.95
Std Dev	3.217

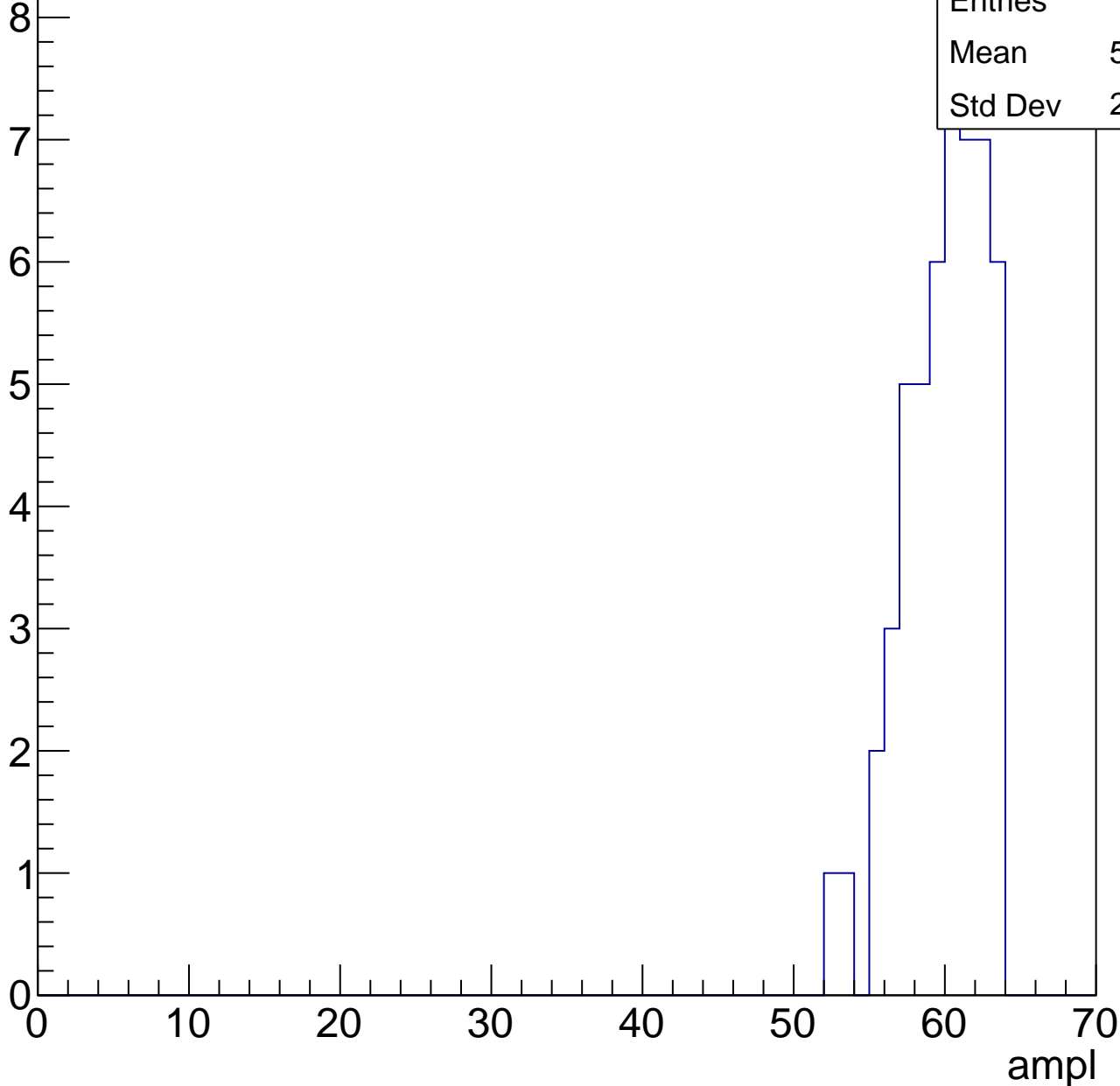


# B1L102S, U21-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

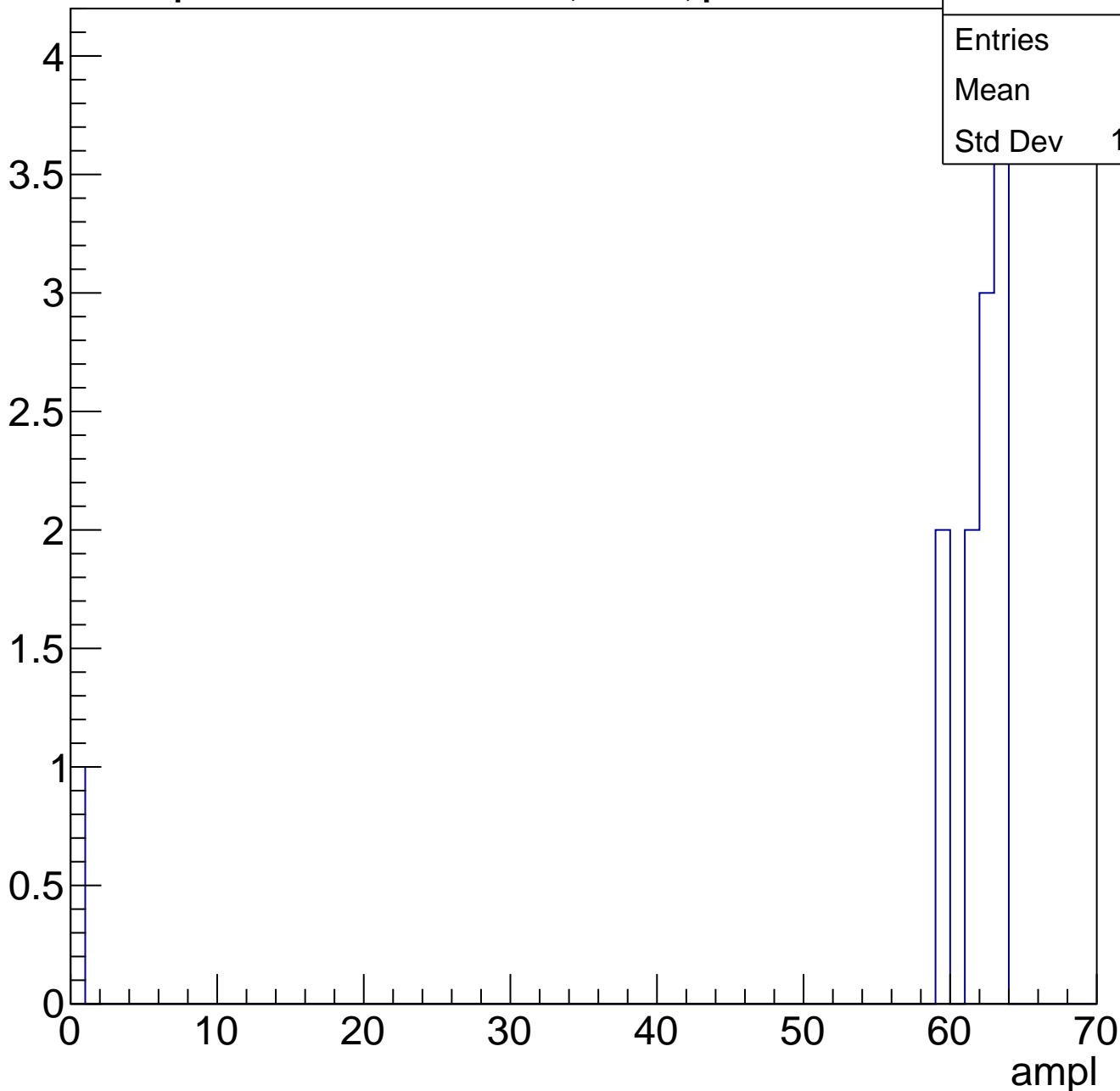
Entries	51
Mean	59.43
Std Dev	2.637



# B1L102S, U21-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

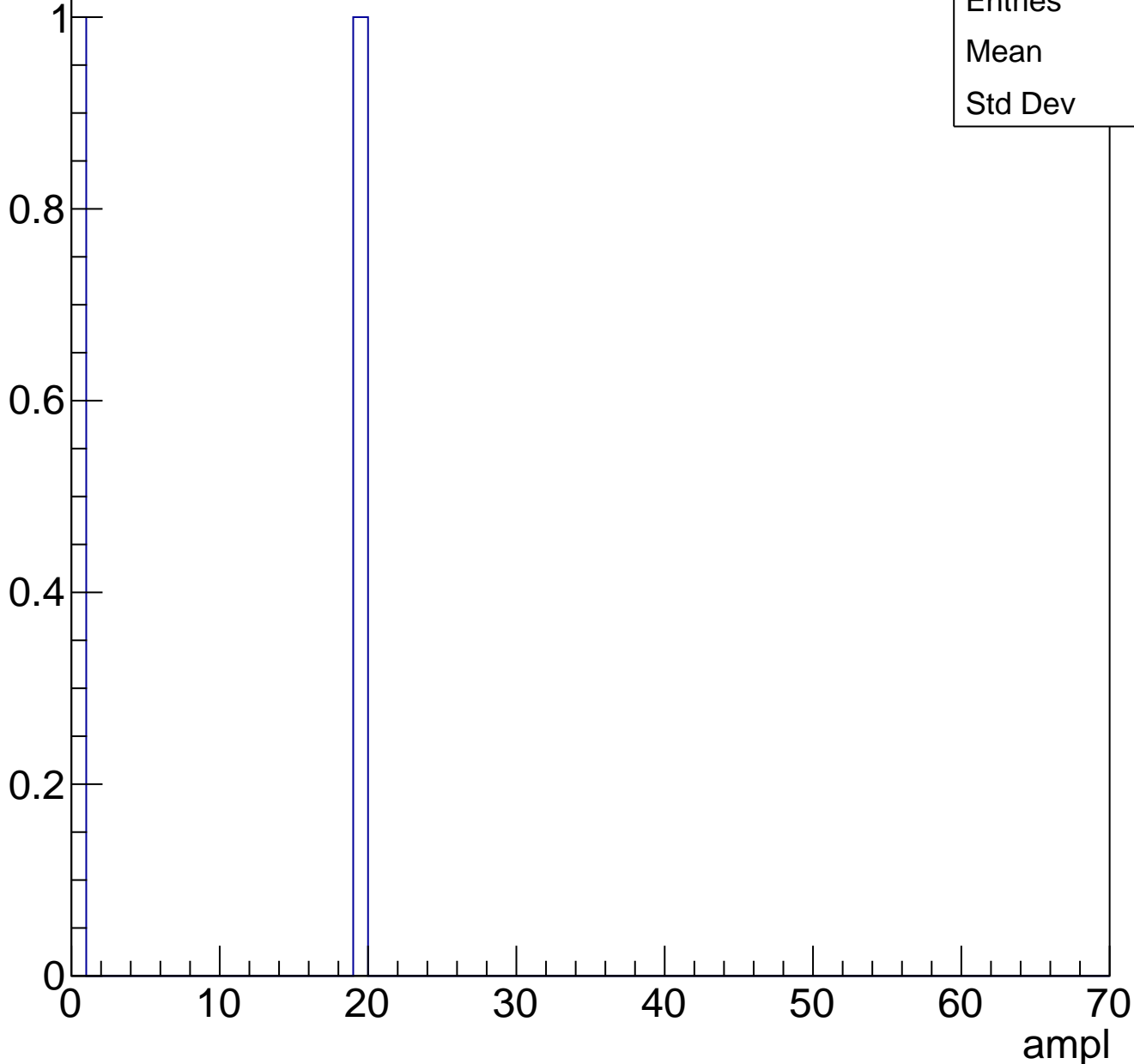




# B1L102S, U21-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch9, adc0

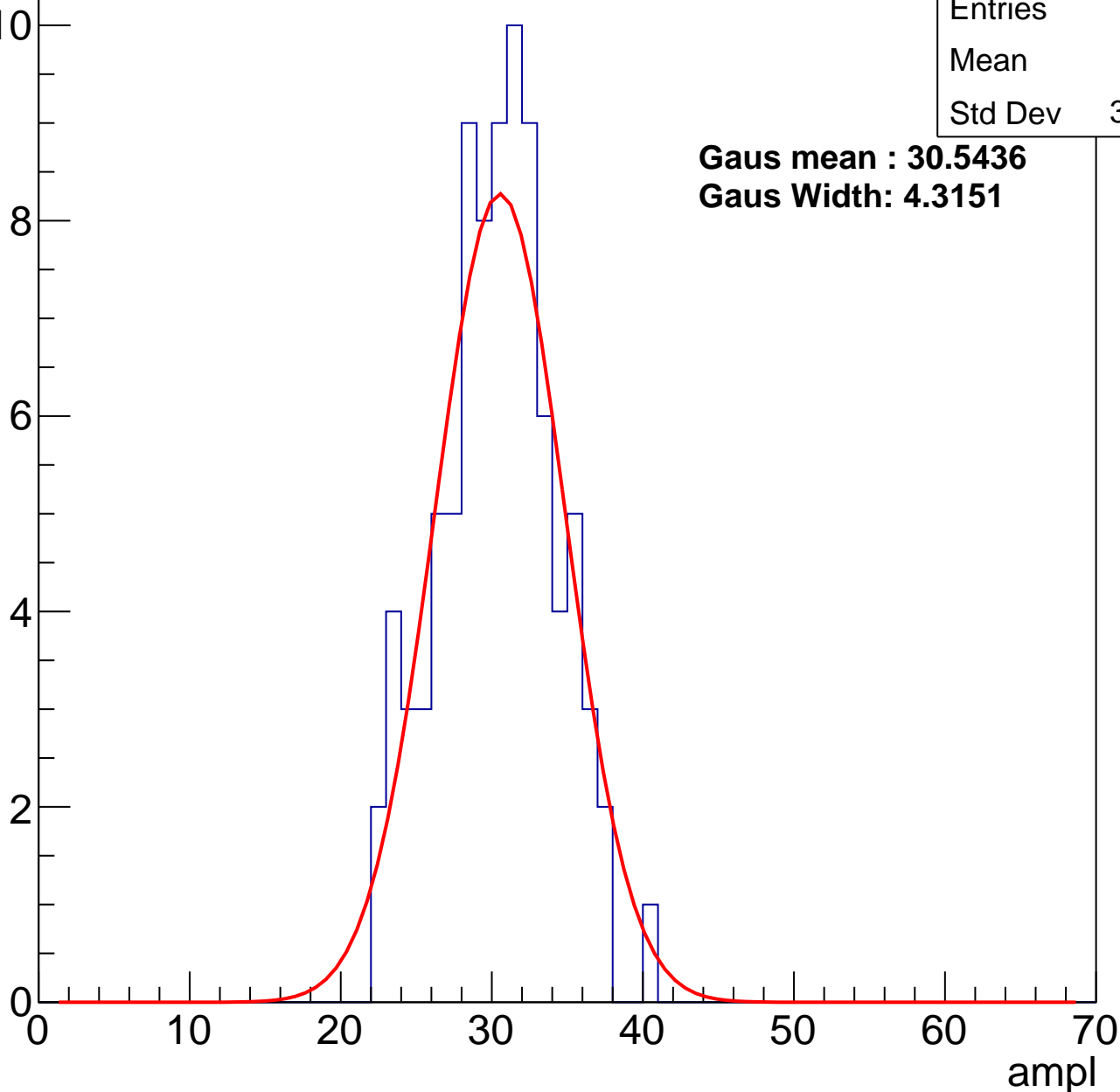
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	88
Mean	29.9
Std Dev	3.799

**Gaus mean : 30.5436**

**Gaus Width: 4.3151**



# B1L102S, U21-ch9, adc1

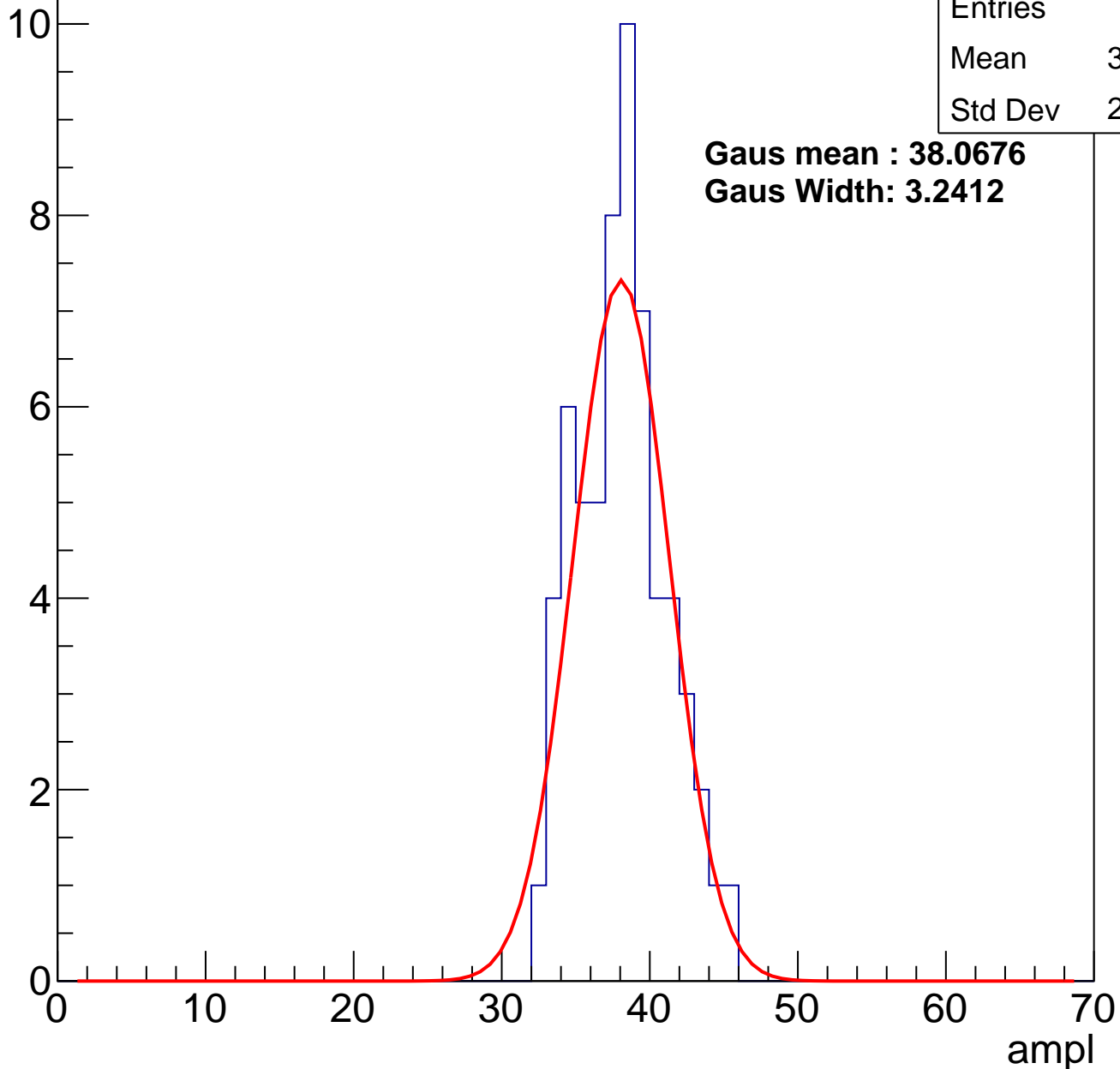
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	61
Mean	37.66
Std Dev	2.975

**Gaus mean : 38.0676**

**Gaus Width: 3.2412**

Entry



# B1L102S, U21-ch9, adc2

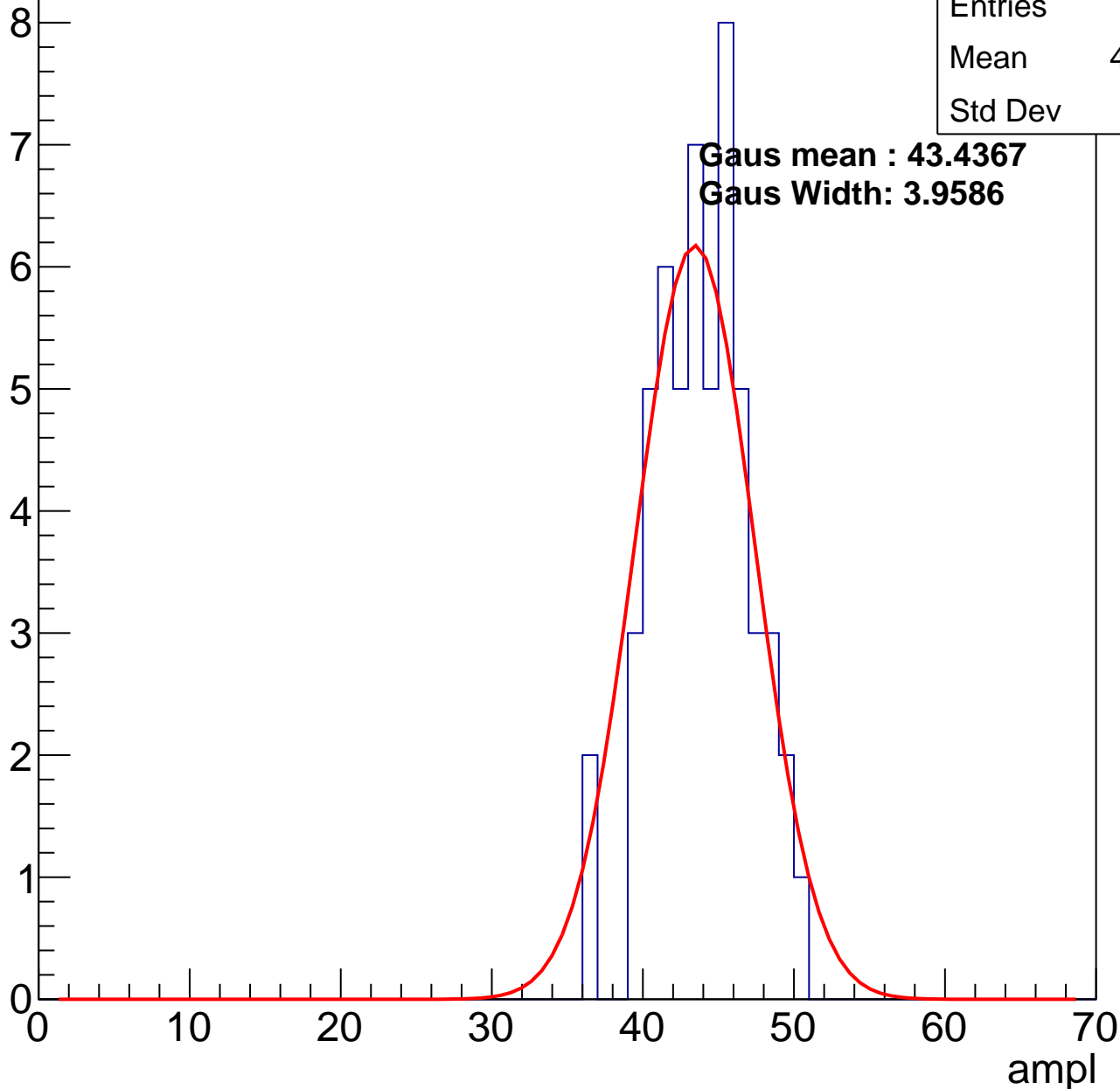
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	43.44
Std Dev	3.12

**Gaus mean : 43.4367**

**Gaus Width: 3.9586**

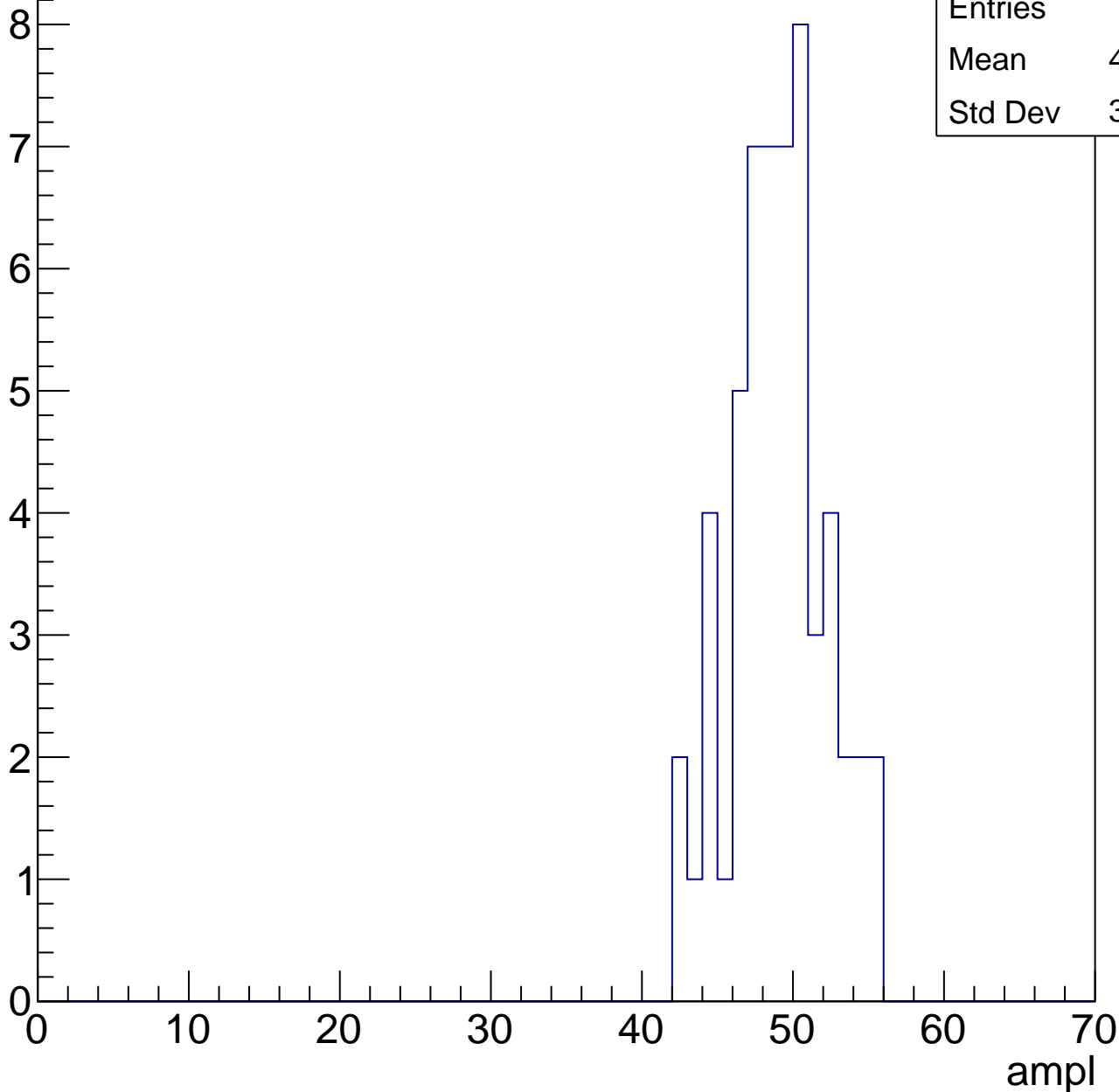


# B1L102S, U21-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	48.56
Std Dev	3.103

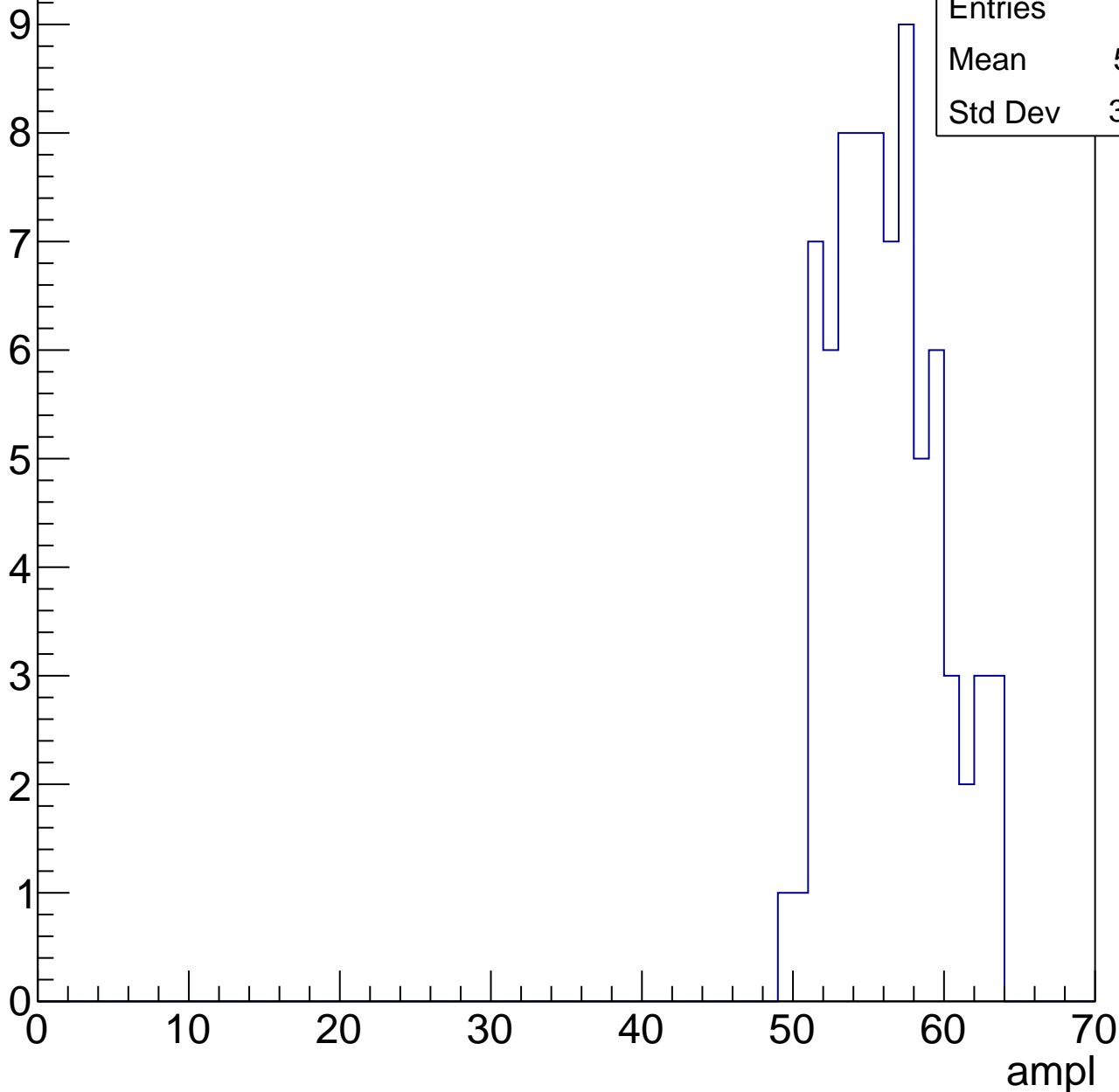


# B1L102S, U21-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	55.71
Std Dev	3.414

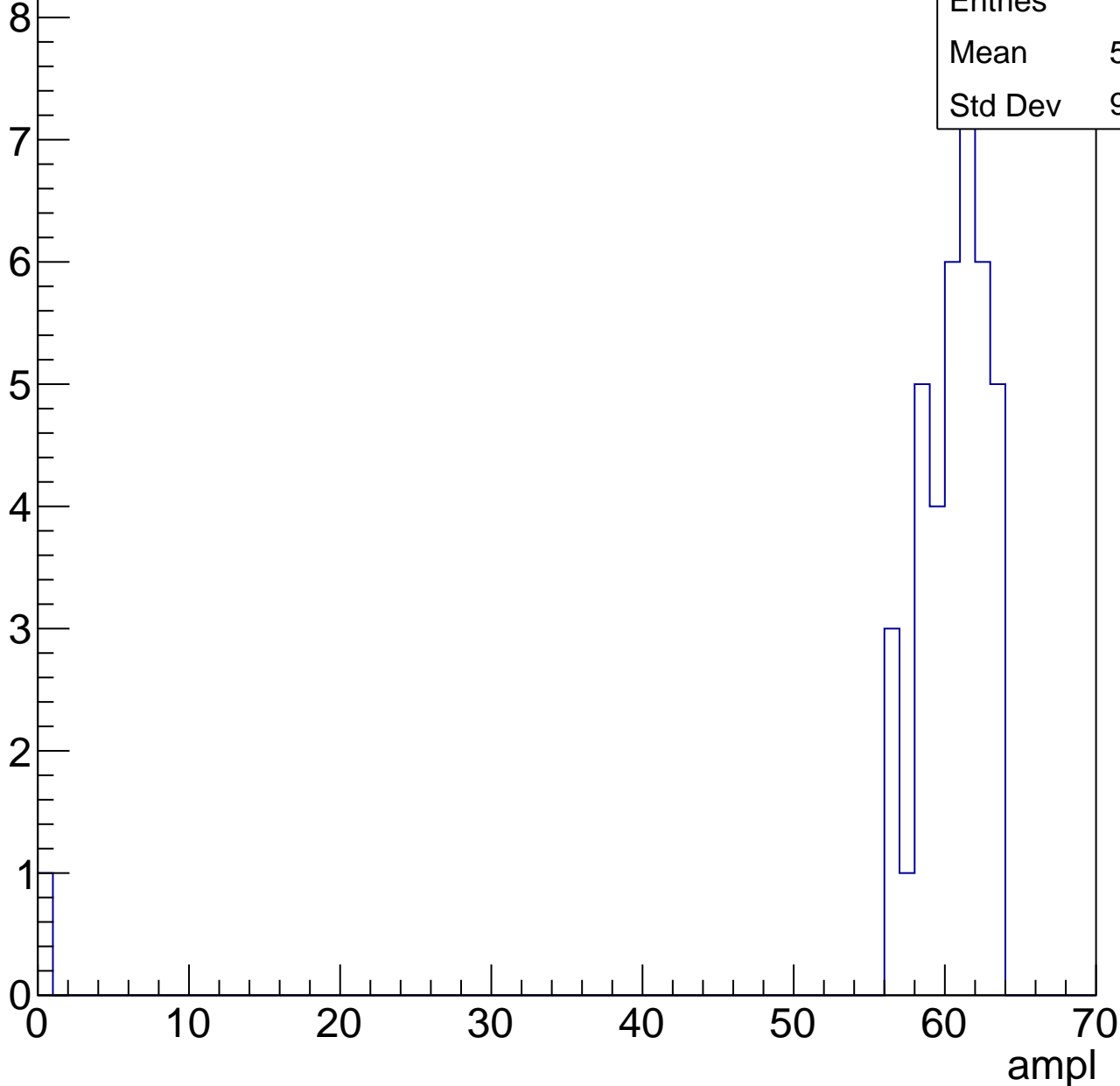


# B1L102S, U21-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

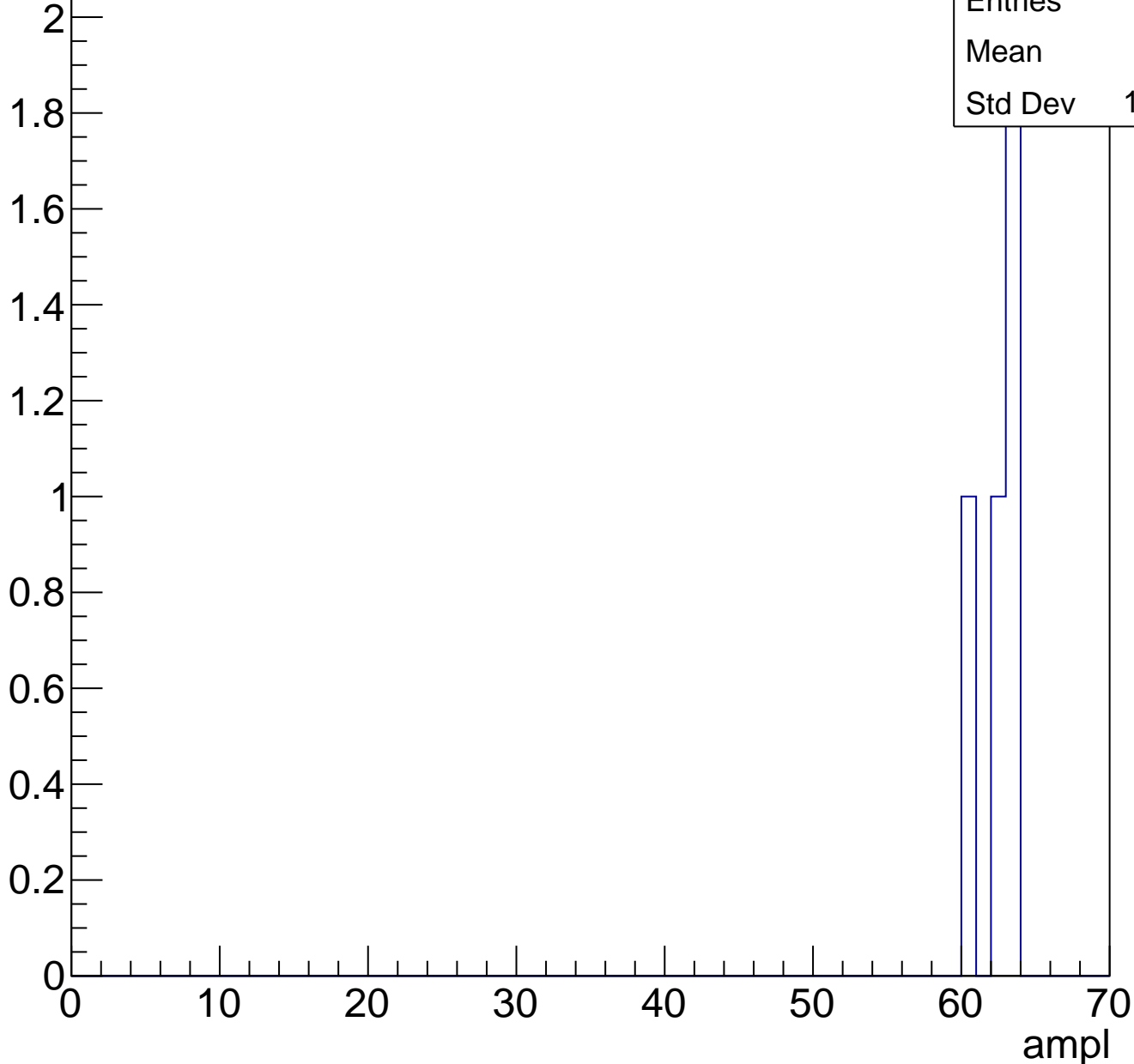
Entries	39
Mean	58.62
Std Dev	9.718



# B1L102S, U21-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch10, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	76
Mean	28.57
Std Dev	3.443

**Gaus mean : 29.4394**

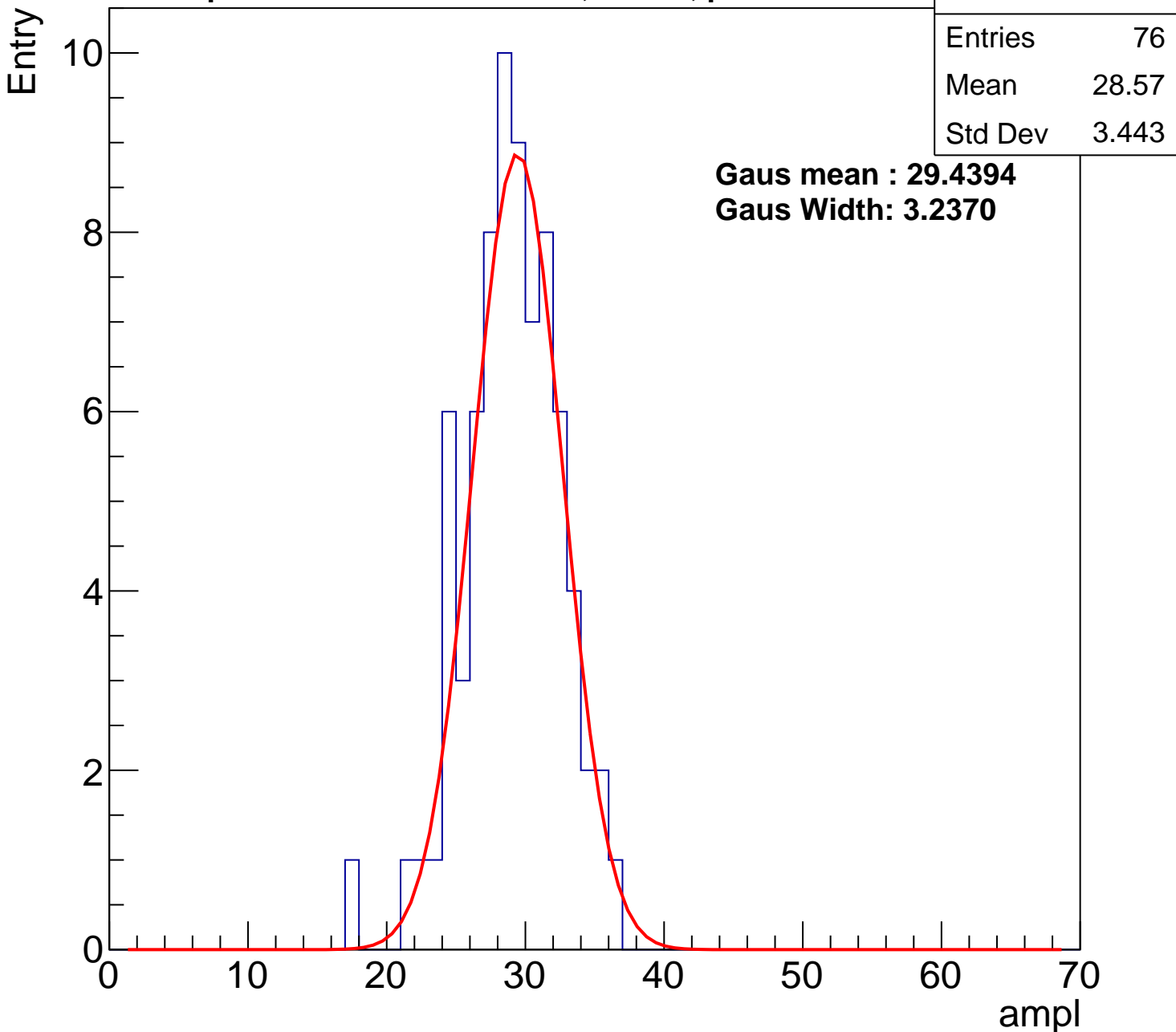
**Gaus Width: 3.2370**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U21-ch10, adc1

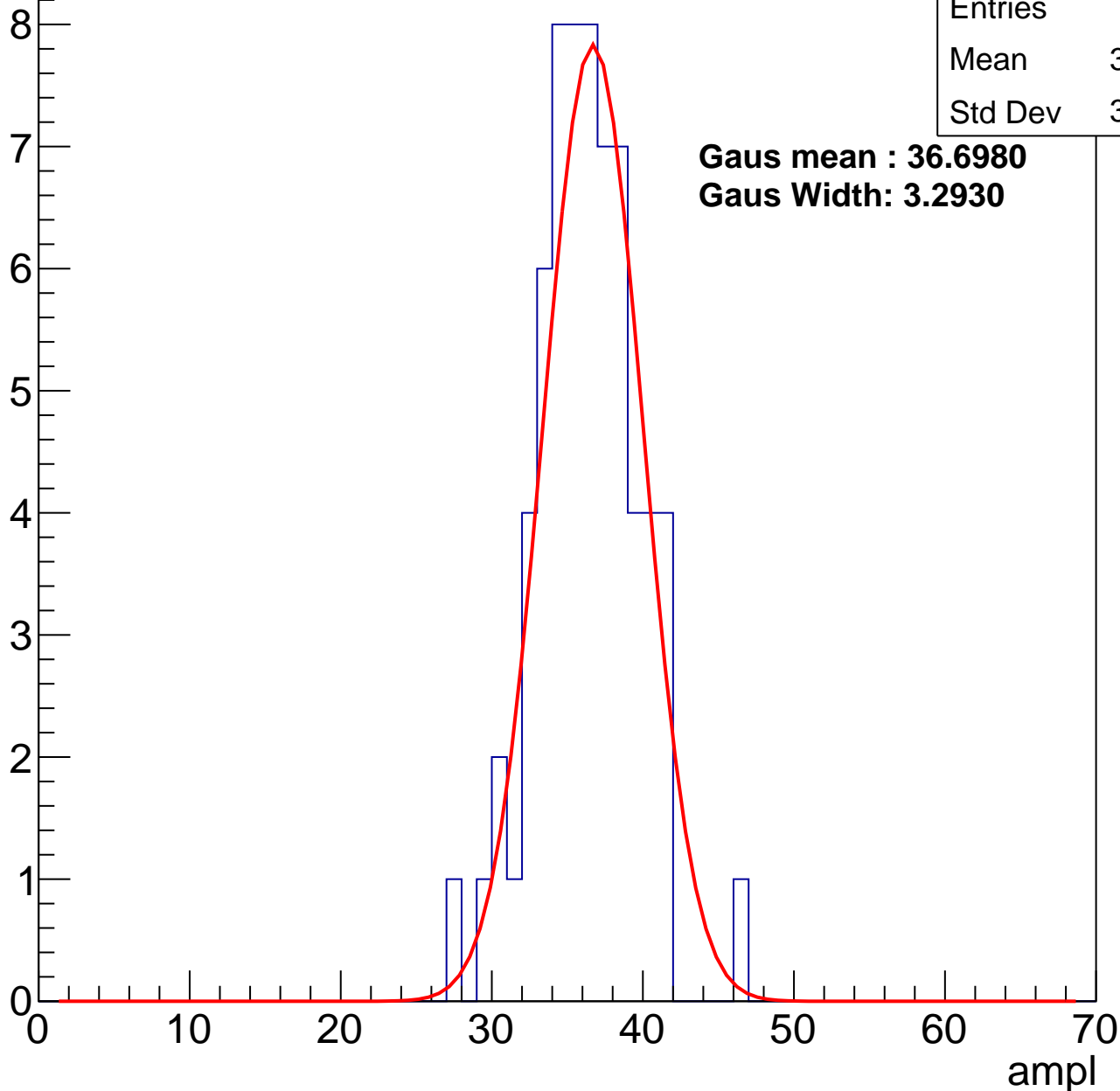
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	35.82
Std Dev	3.298

**Gaus mean : 36.6980**

**Gaus Width: 3.2930**



# B1L102S, U21-ch10, adc2

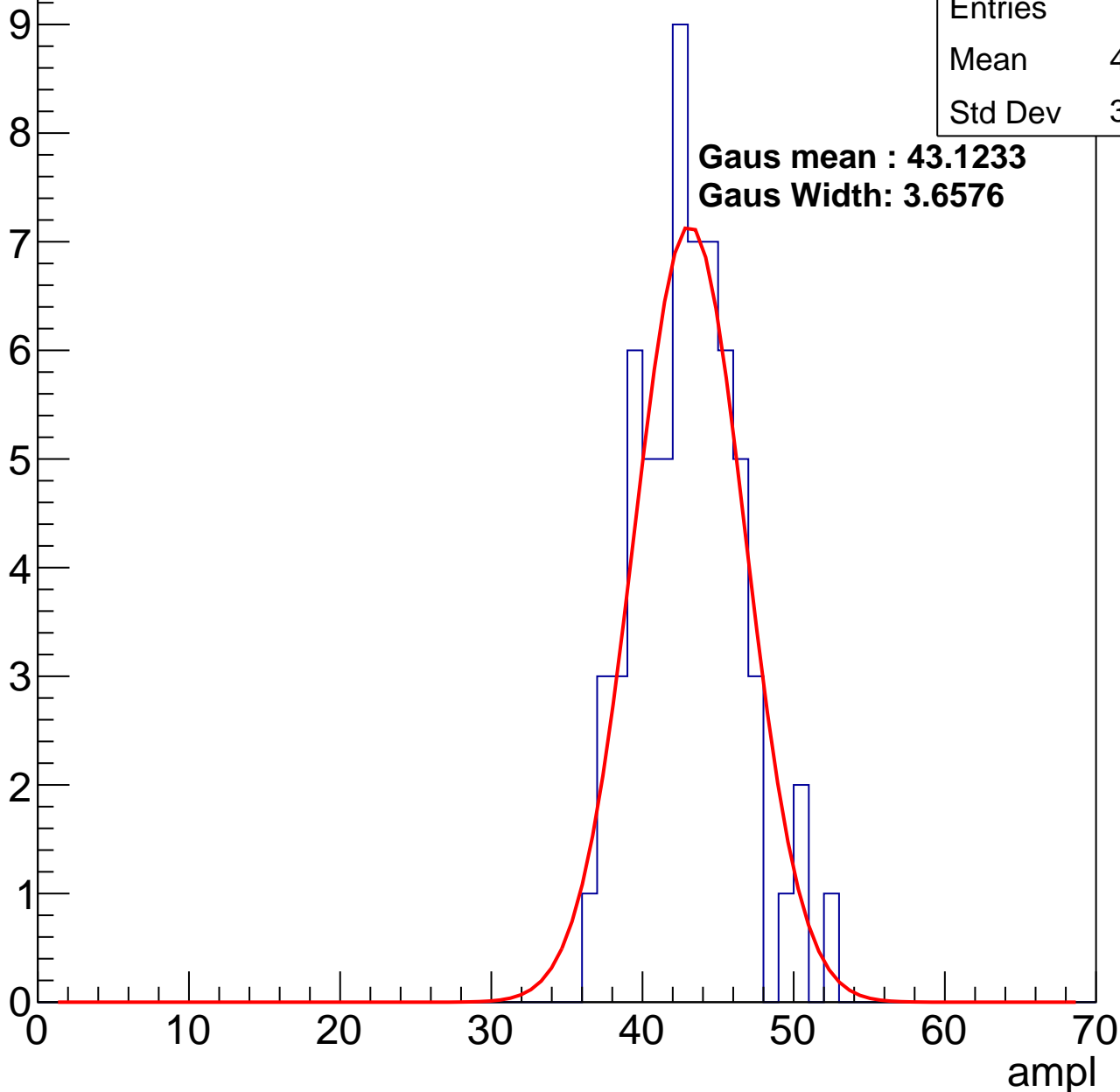
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	42.64
Std Dev	3.384

**Gaus mean : 43.1233**

**Gaus Width: 3.6576**



# B1L102S, U21-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

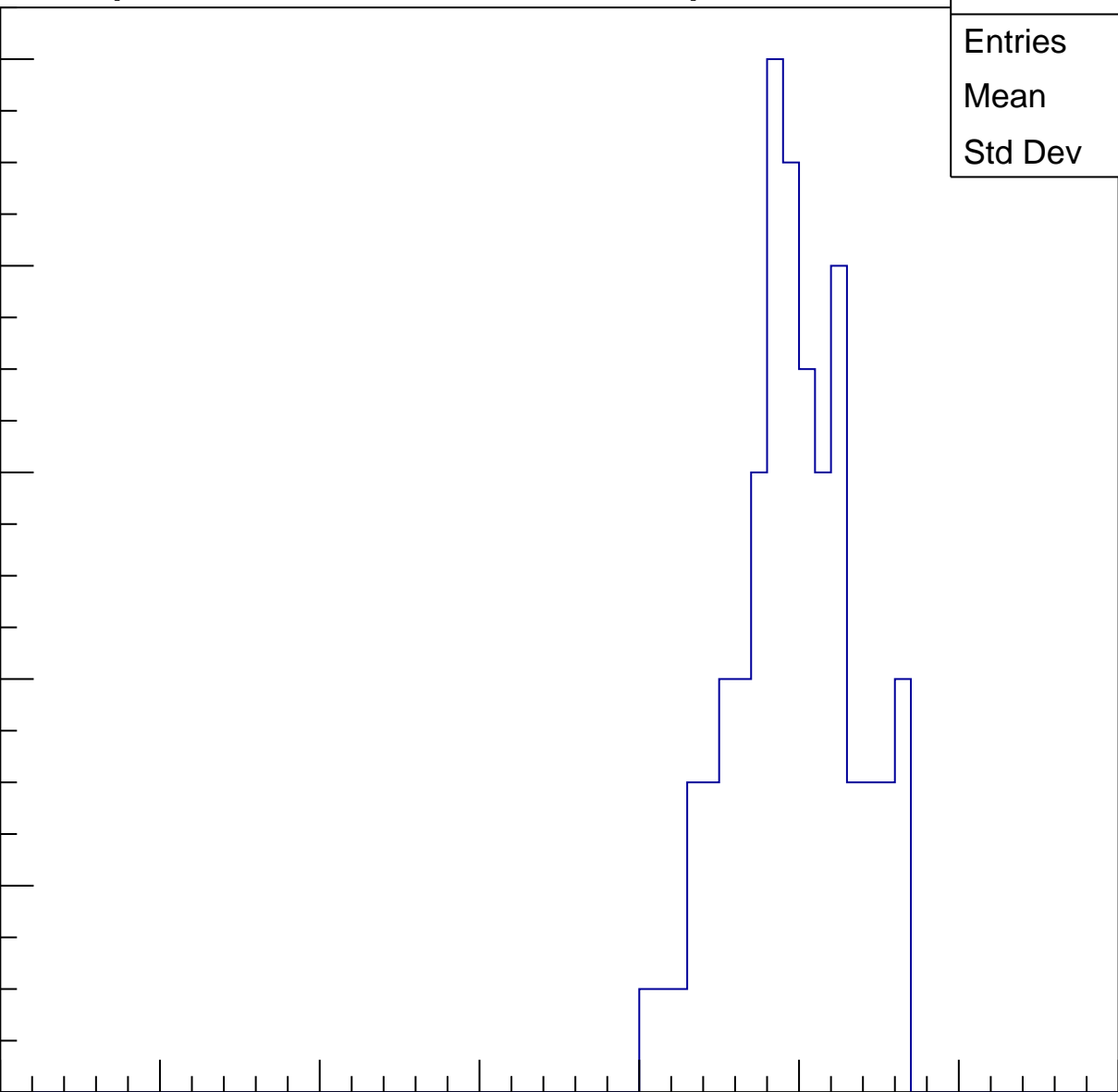
Entries	76
Mean	49.12
Std Dev	3.699

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

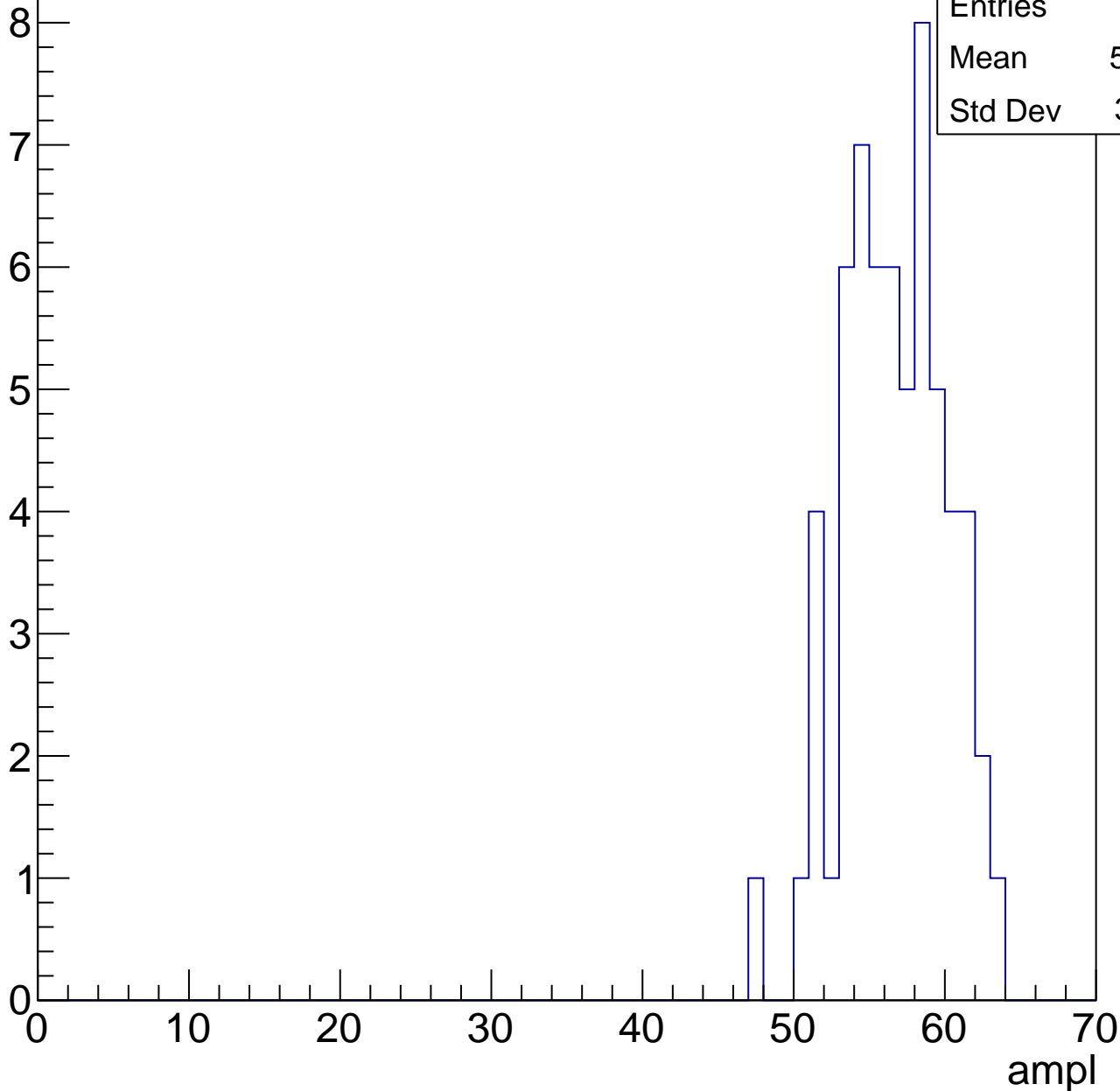


# B1L102S, U21-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	56.23
Std Dev	3.351

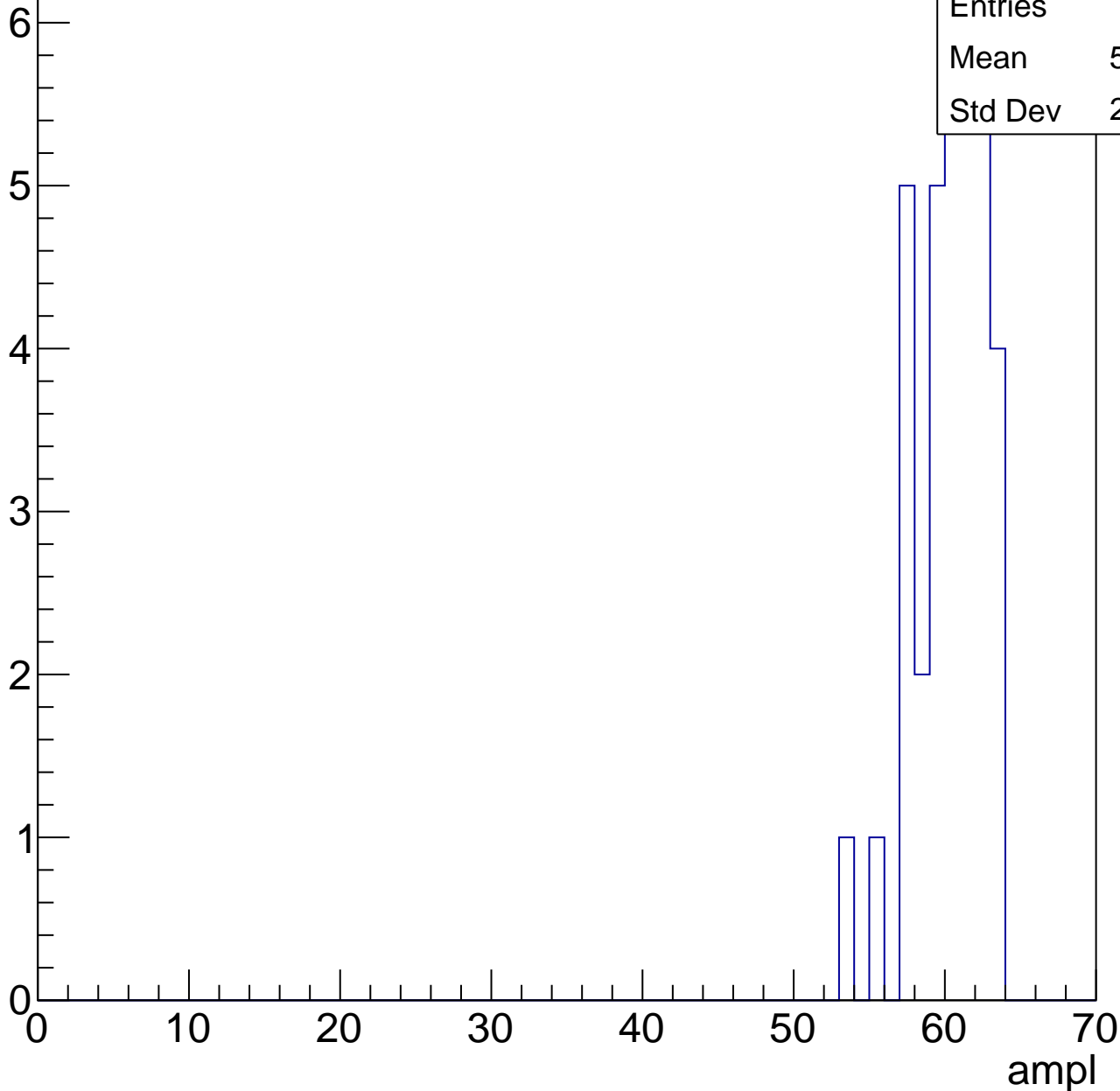


# B1L102S, U21-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	36
Mean	59.83
Std Dev	2.339

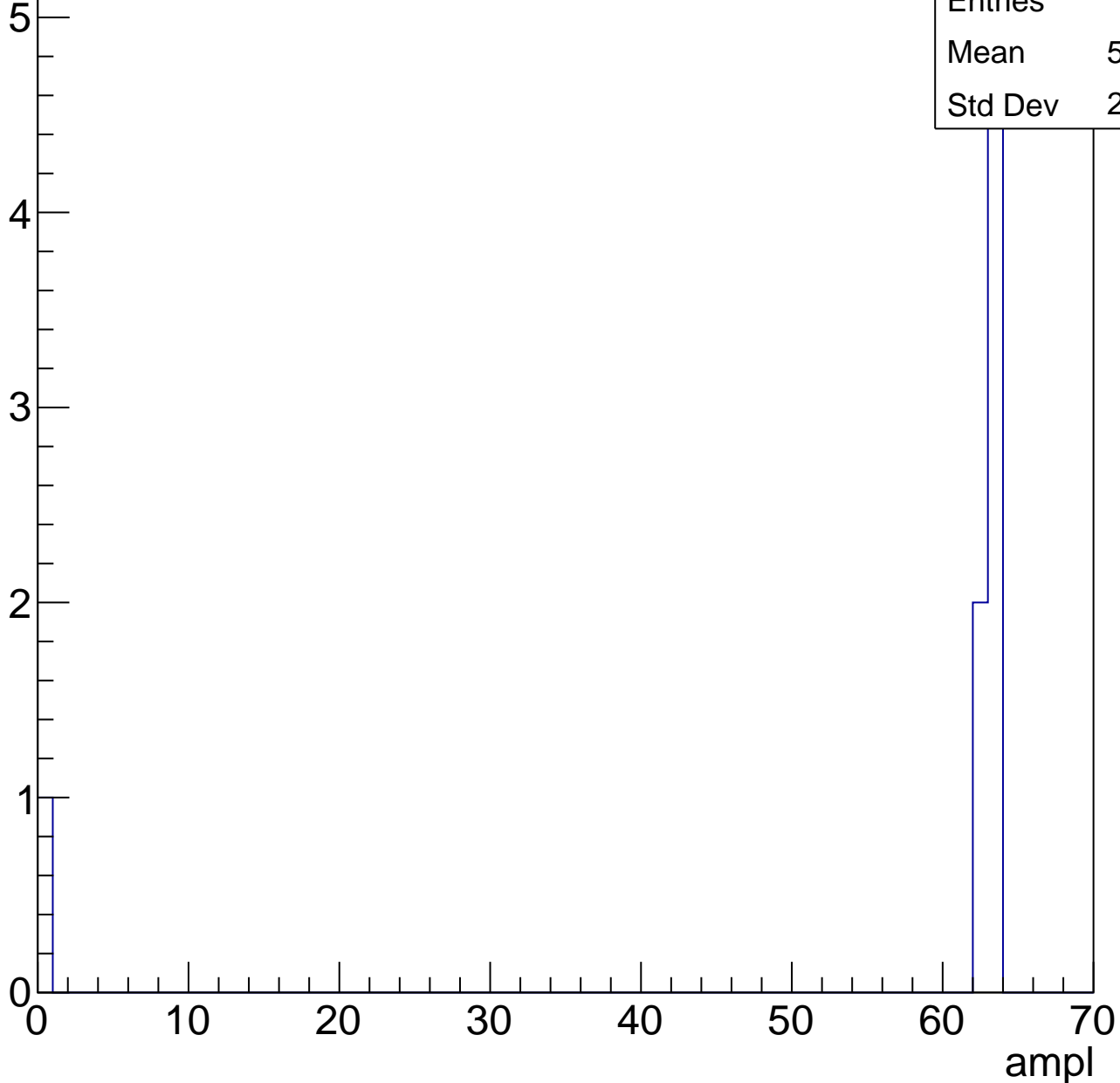


# B1L102S, U21-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	8
Mean	54.88
Std Dev	20.75





# B1L102S, U21-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch11, adc0

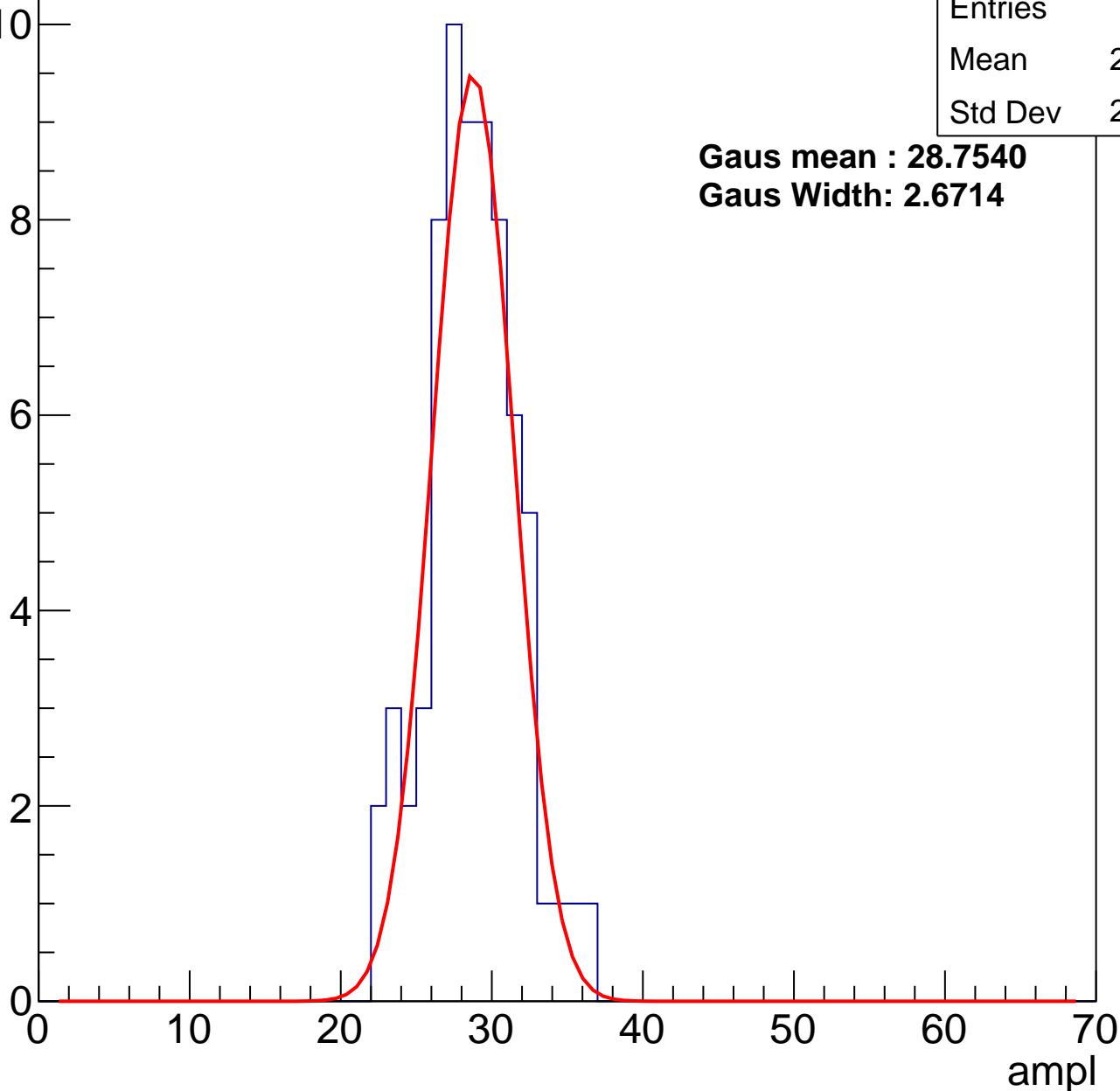
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	28.28
Std Dev	2.929

**Gaus mean : 28.7540**

**Gaus Width: 2.6714**



# B1L102S, U21-ch11, adc1

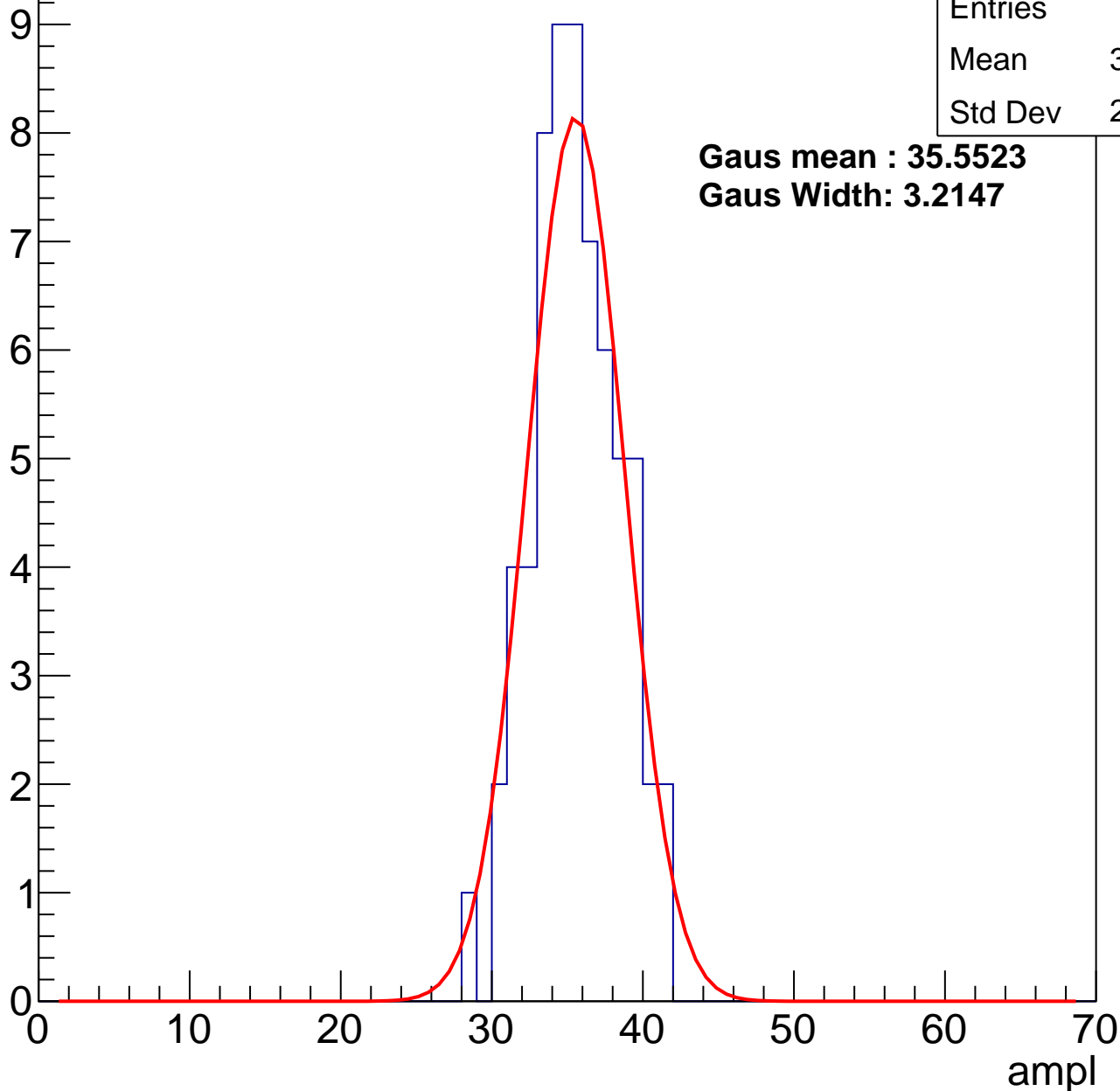
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	35.09
Std Dev	2.843

**Gaus mean : 35.5523**

**Gaus Width: 3.2147**



# B1L102S, U21-ch11, adc2

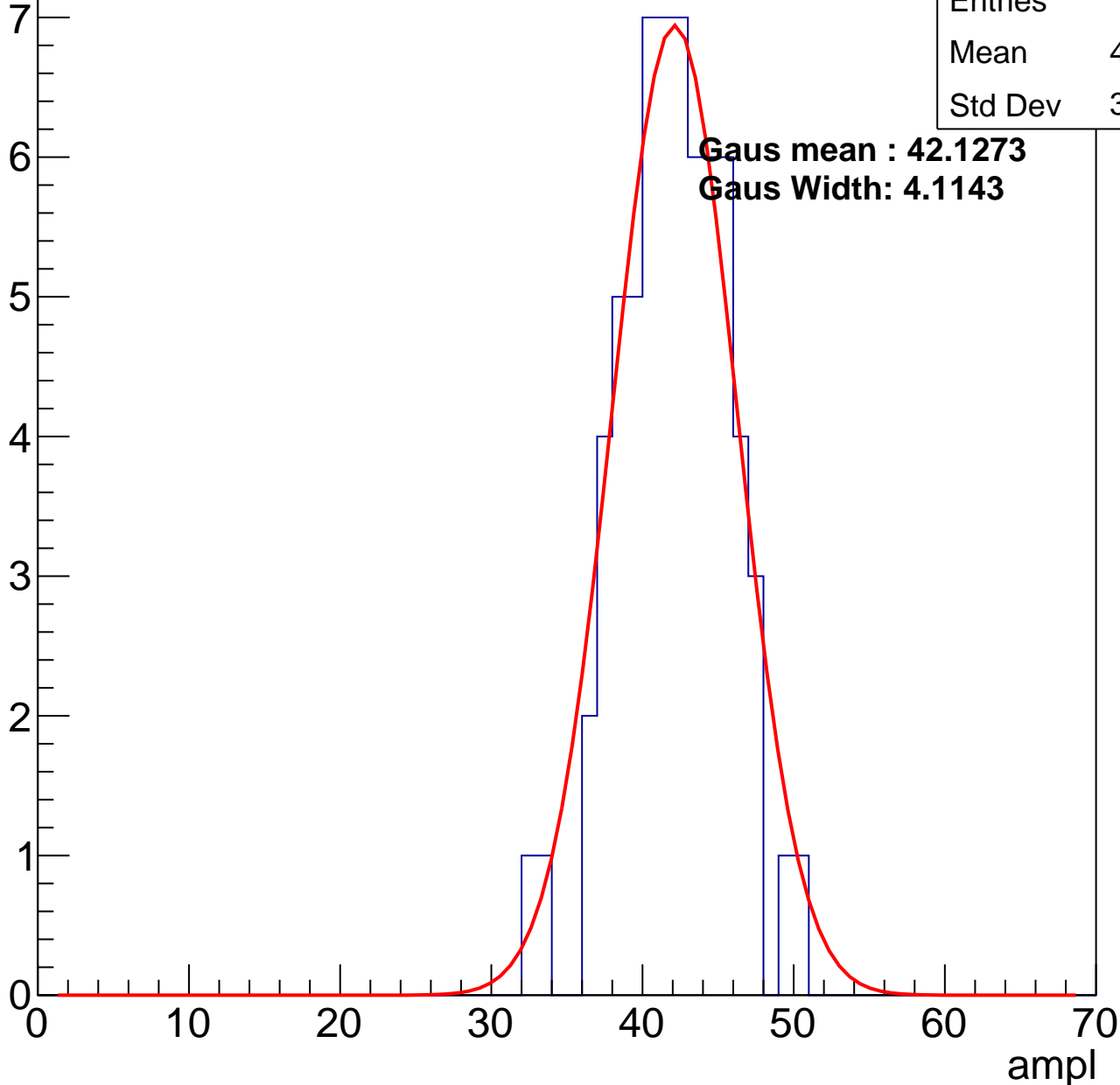
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	41.62
Std Dev	3.567

**Gaus mean : 42.1273**

**Gaus Width: 4.1143**

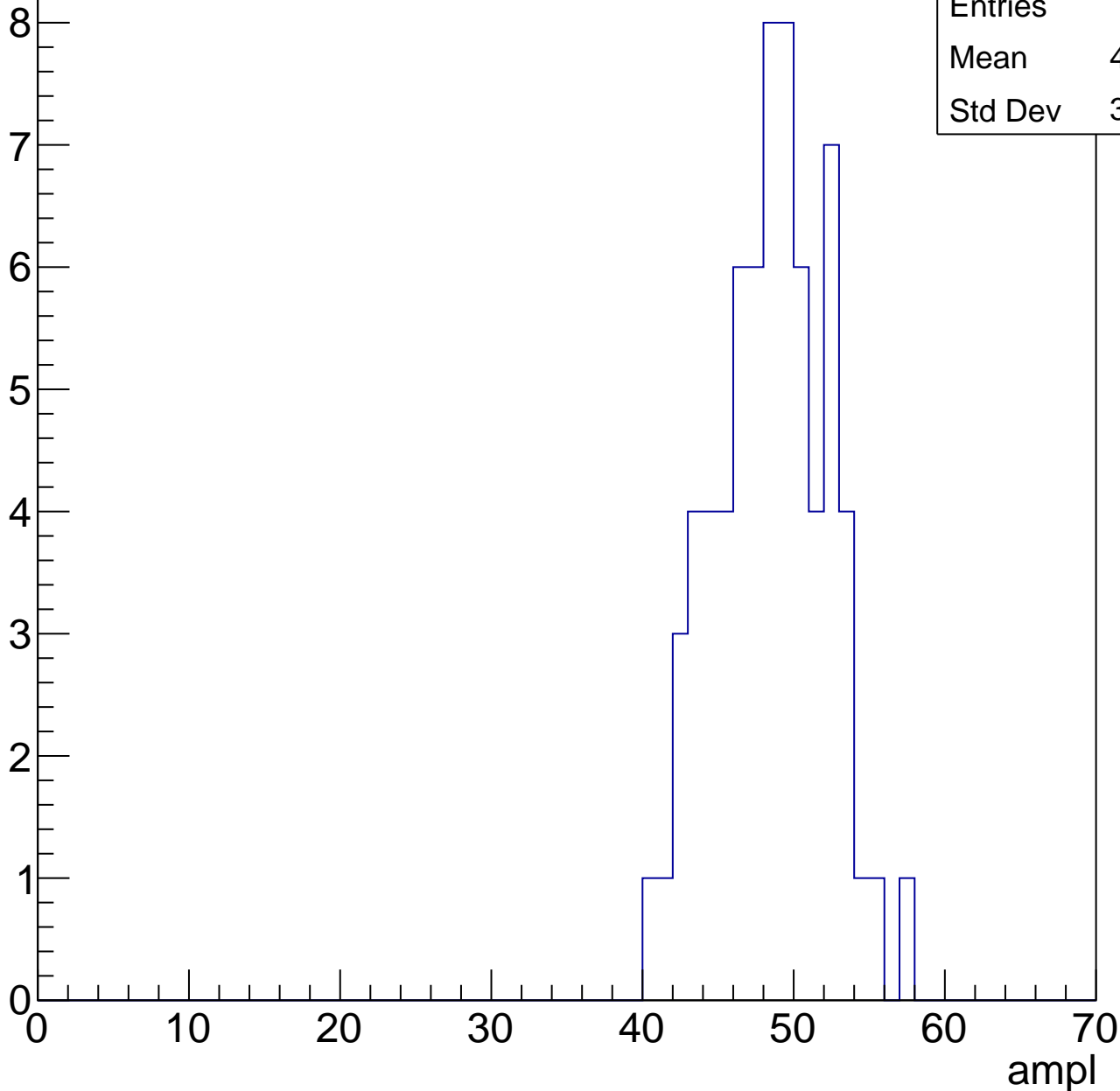


# B1L102S, U21-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	48.04
Std Dev	3.605

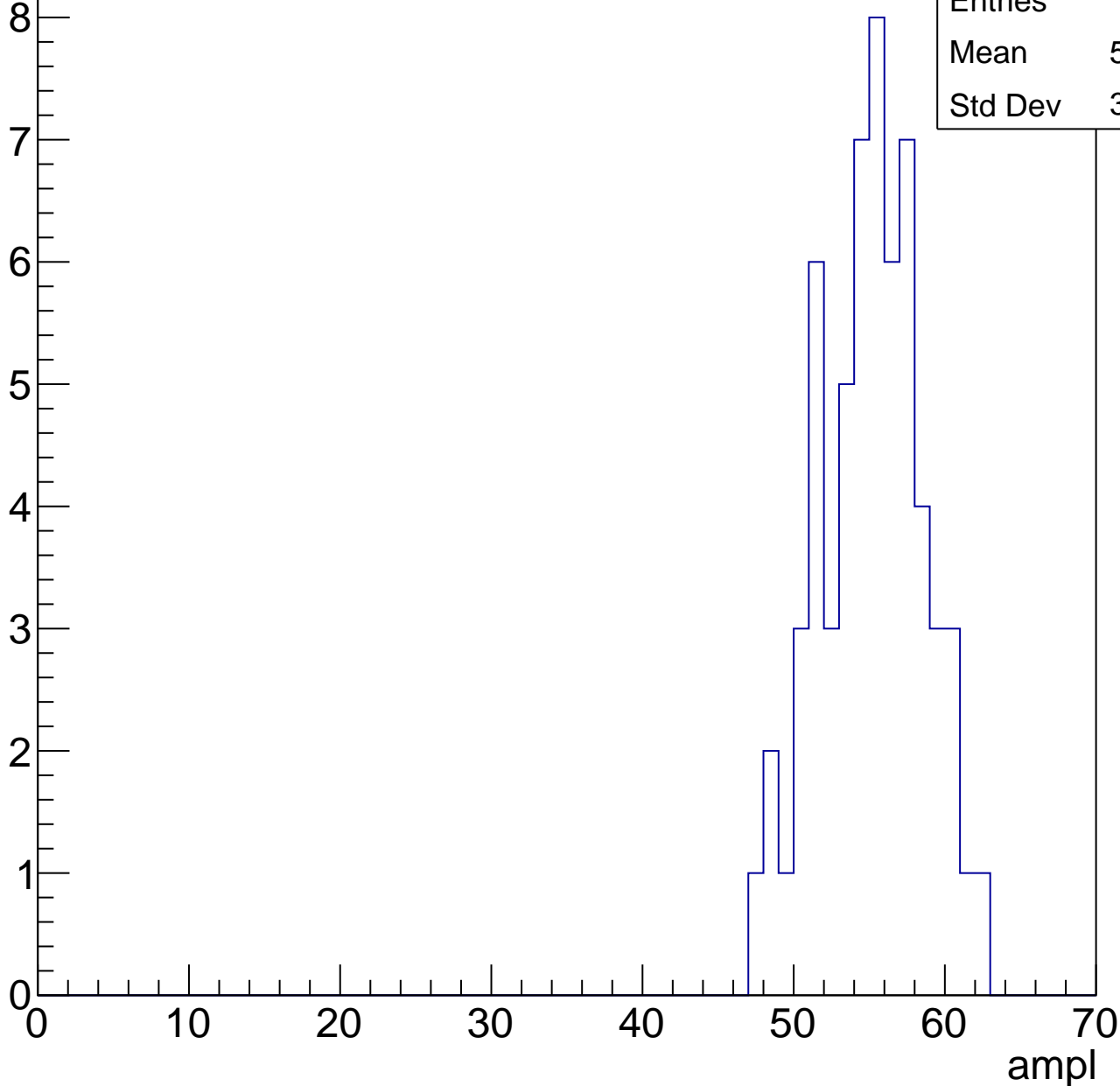


# B1L102S, U21-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	54.66
Std Dev	3.372



# B1L102S, U21-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

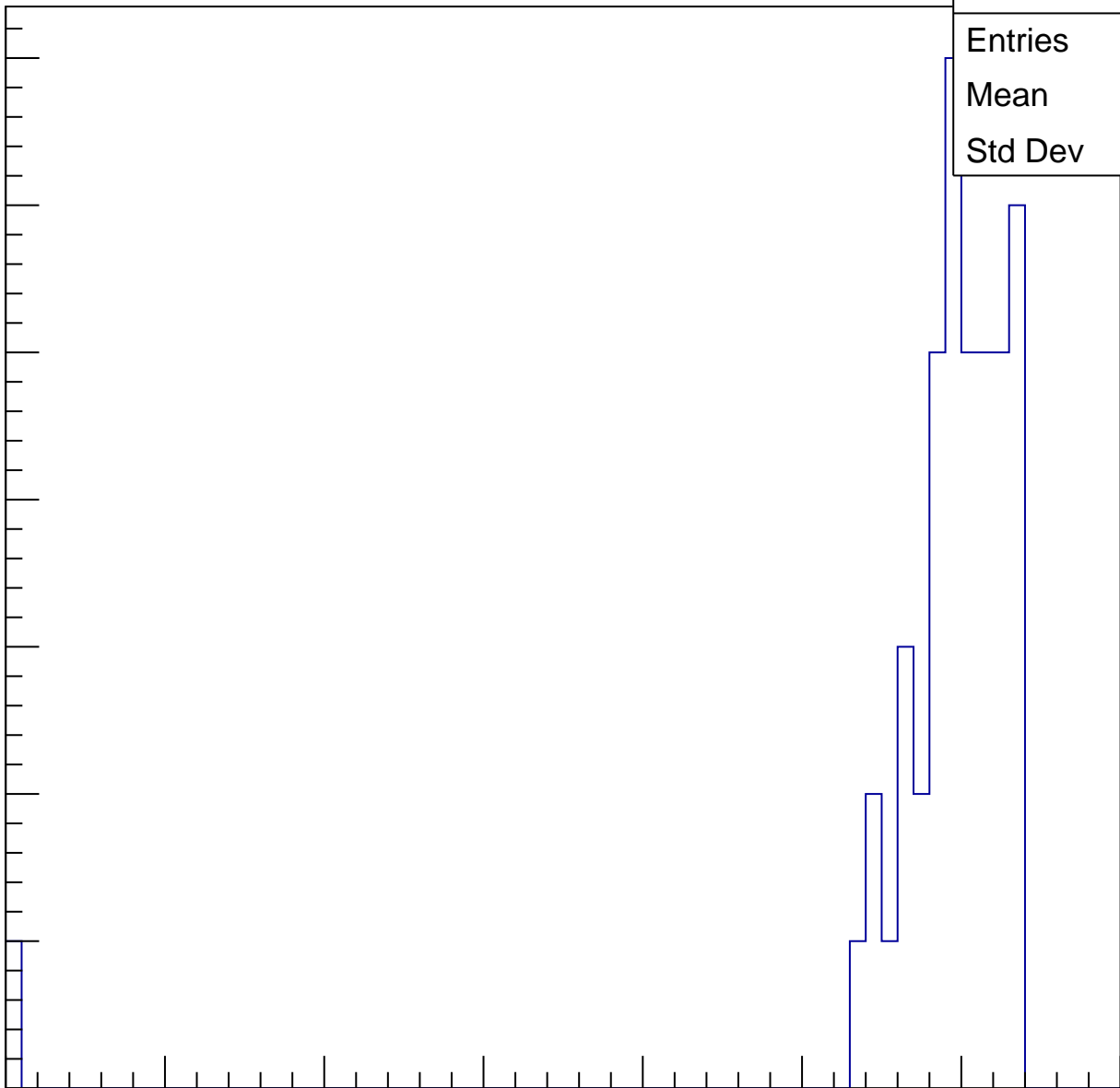
Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	43
Mean	58
Std Dev	9.334

ampl

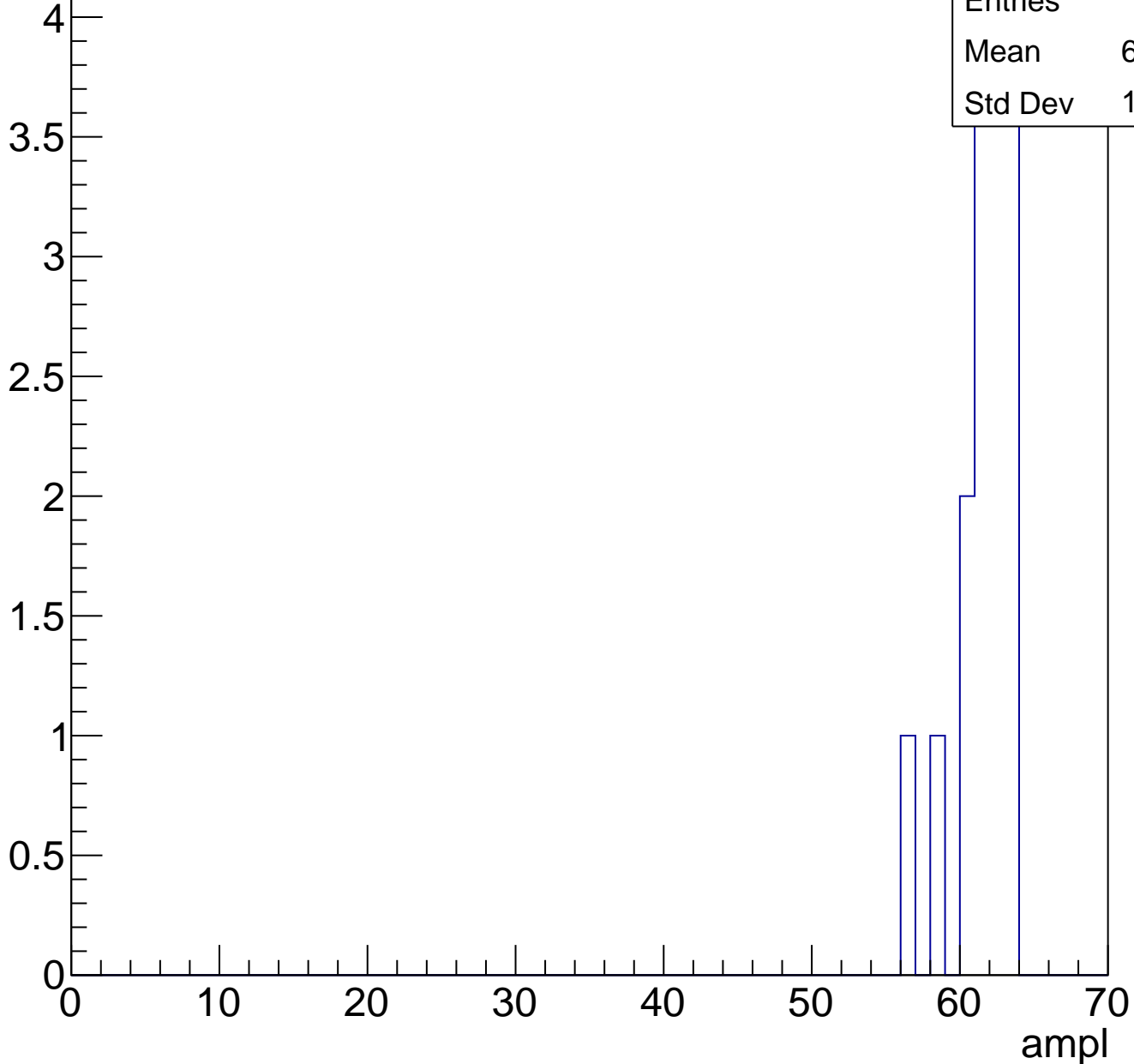
0 10 20 30 40 50 60 70



# B1L102S, U21-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	20
Std Dev	0

ampl

# B1L102S, U21-ch12, adc0

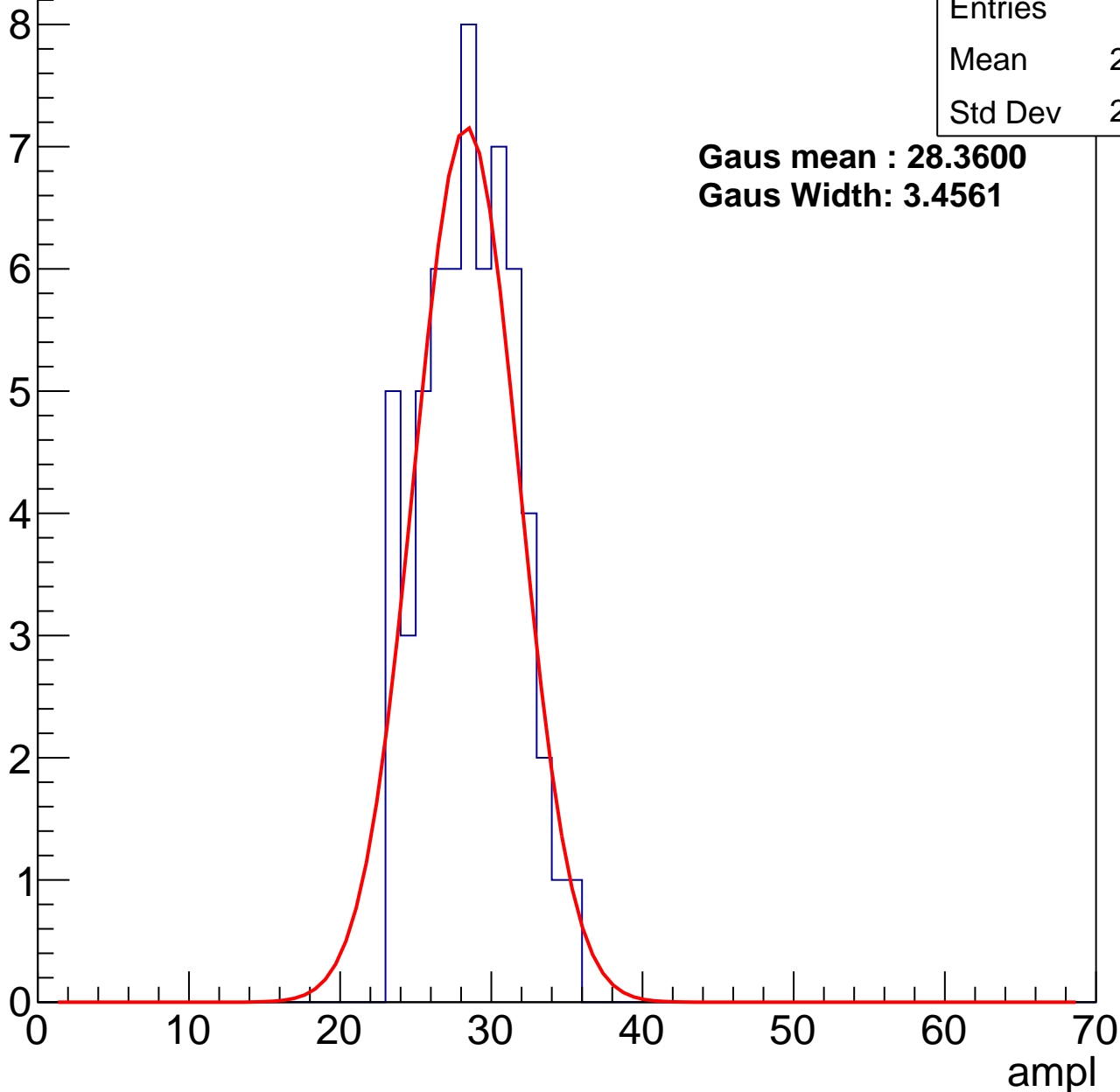
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	28.12
Std Dev	2.984

**Gaus mean : 28.3600**

**Gaus Width: 3.4561**



# B1L102S, U21-ch12, adc1

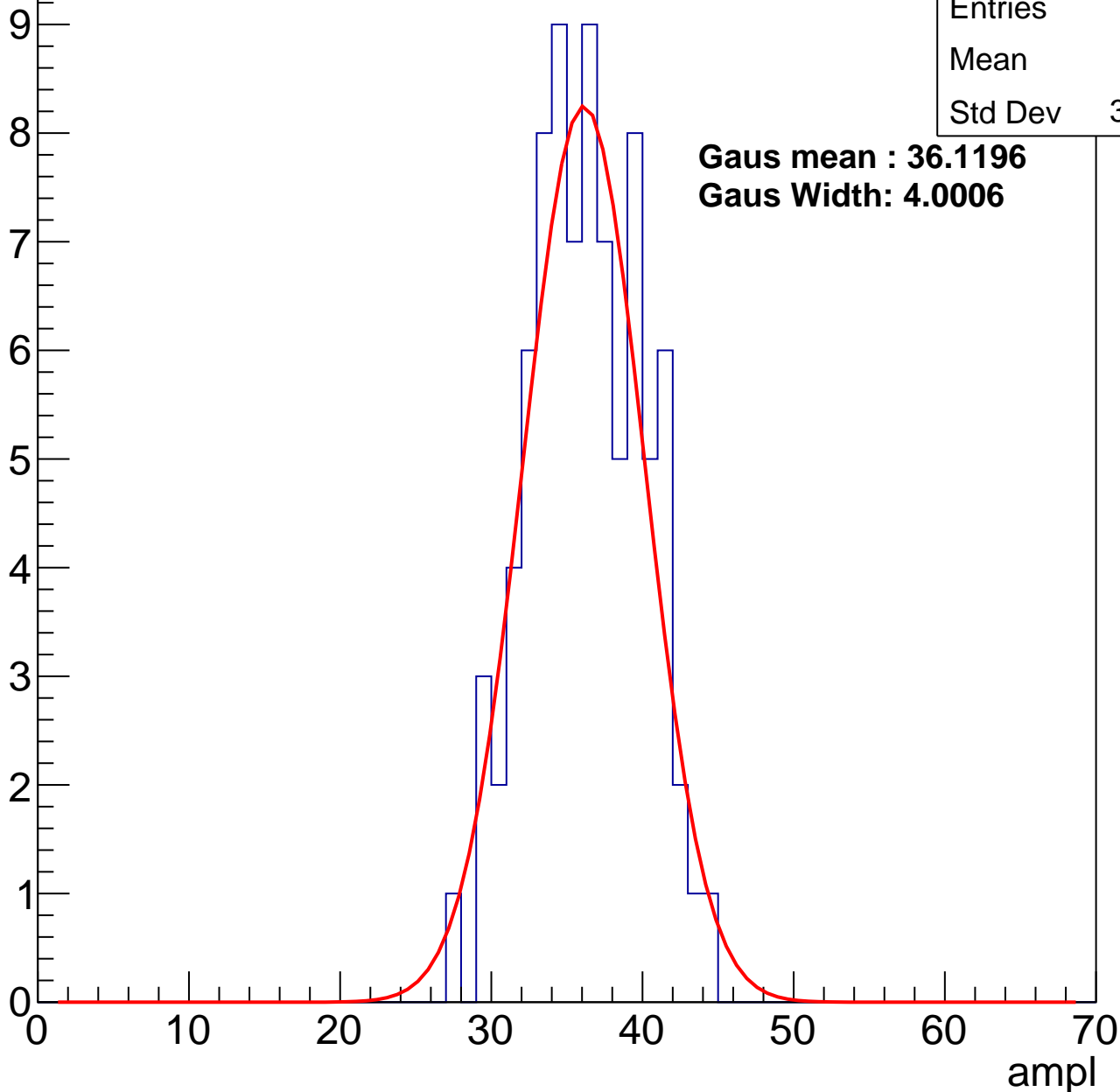
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	35.8
Std Dev	3.654

**Gaus mean : 36.1196**

**Gaus Width: 4.0006**



# B1L102S, U21-ch12, adc2

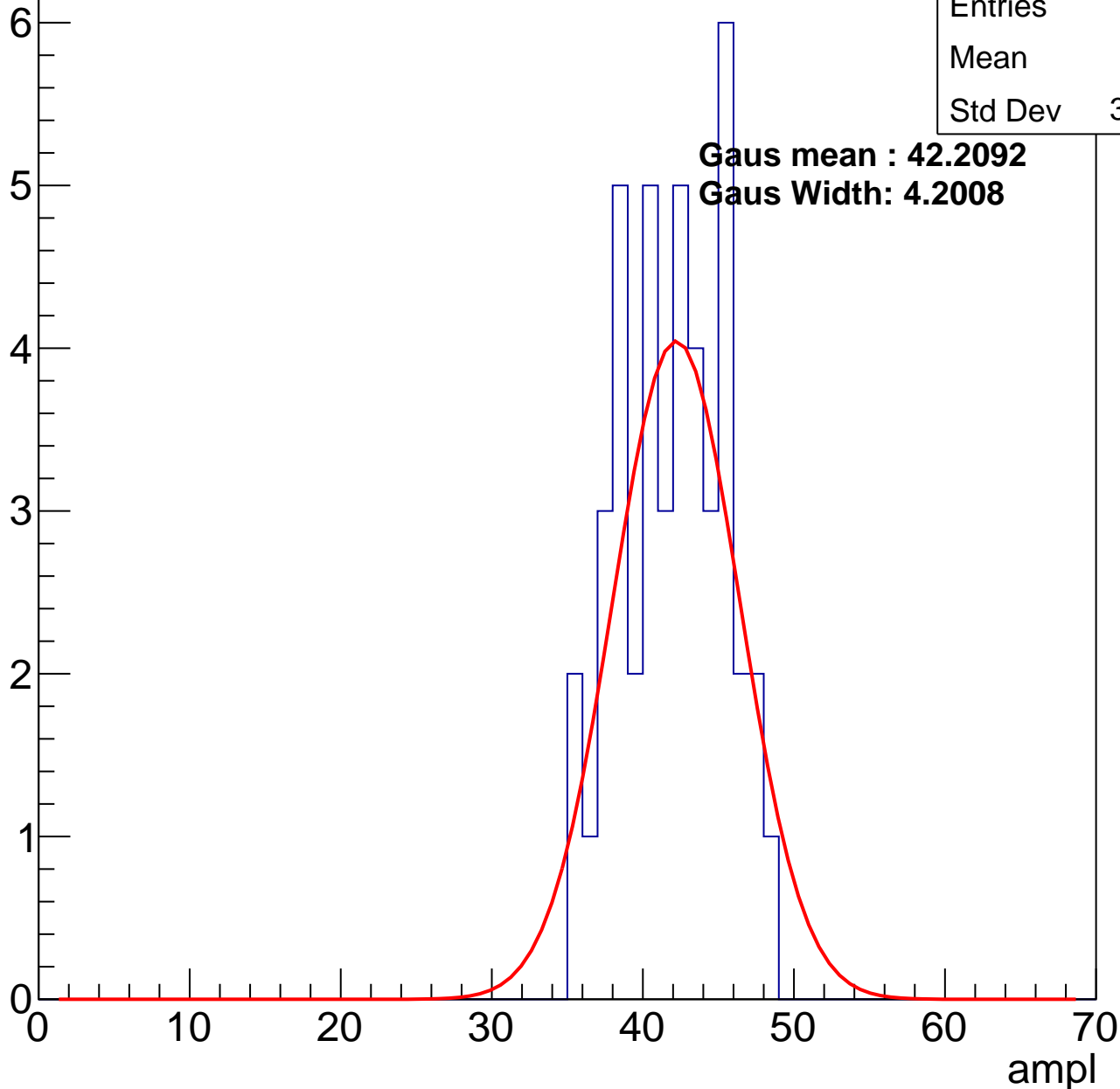
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	44
Mean	41.5
Std Dev	3.395

**Gaus mean : 42.2092**

**Gaus Width: 4.2008**

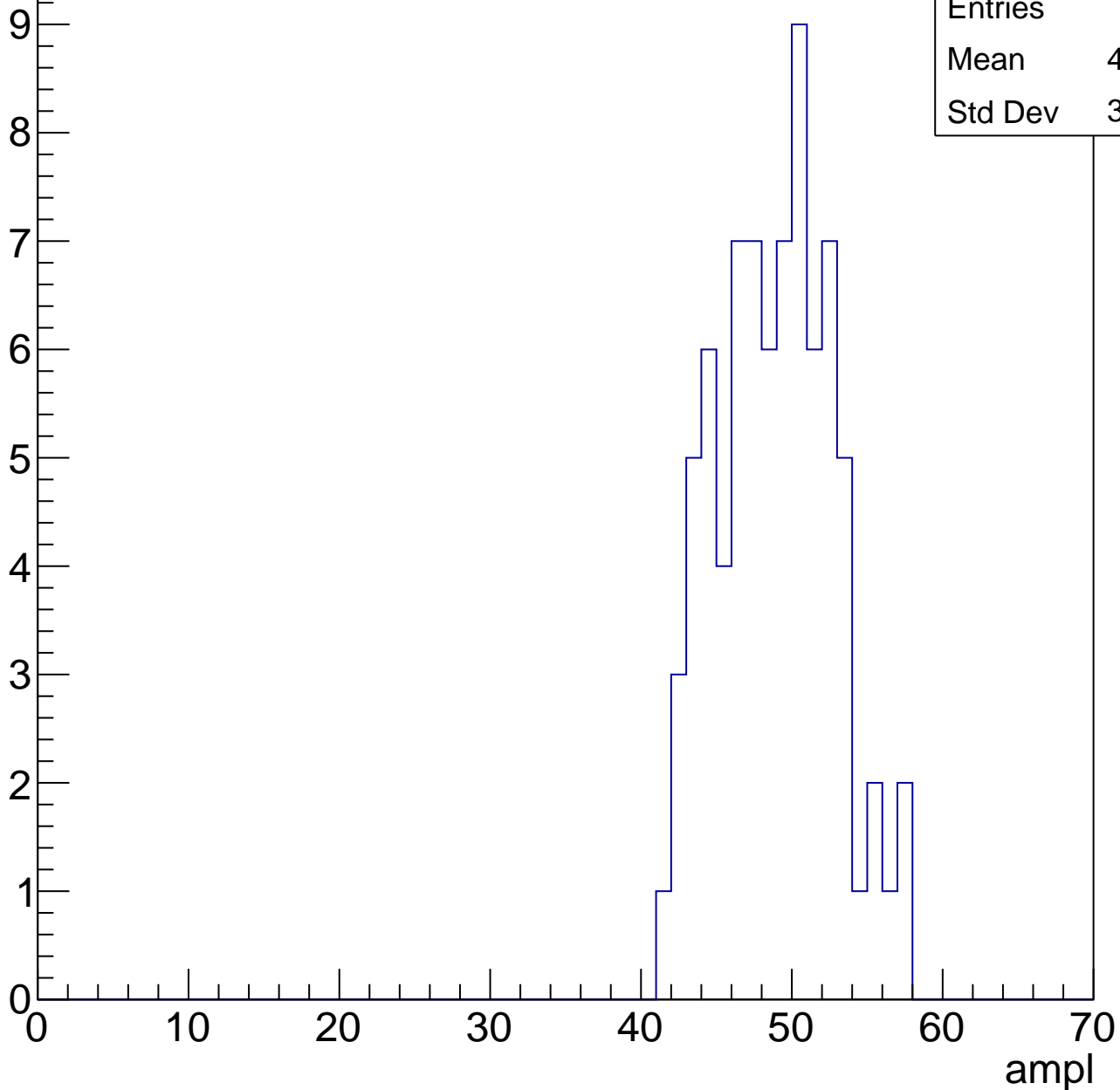


# B1L102S, U21-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	48.44
Std Dev	3.778

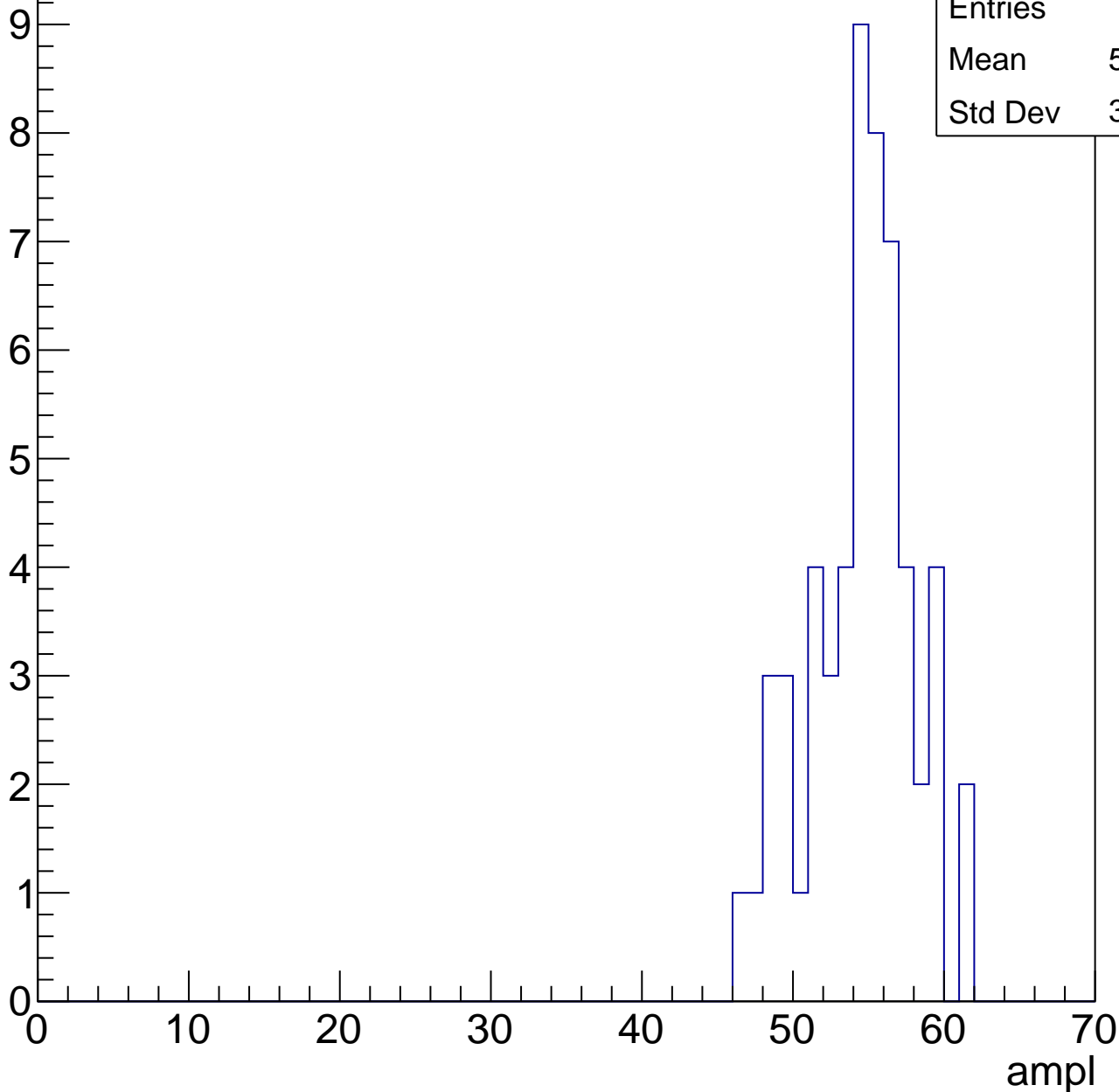


# B1L102S, U21-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	54.04
Std Dev	3.448

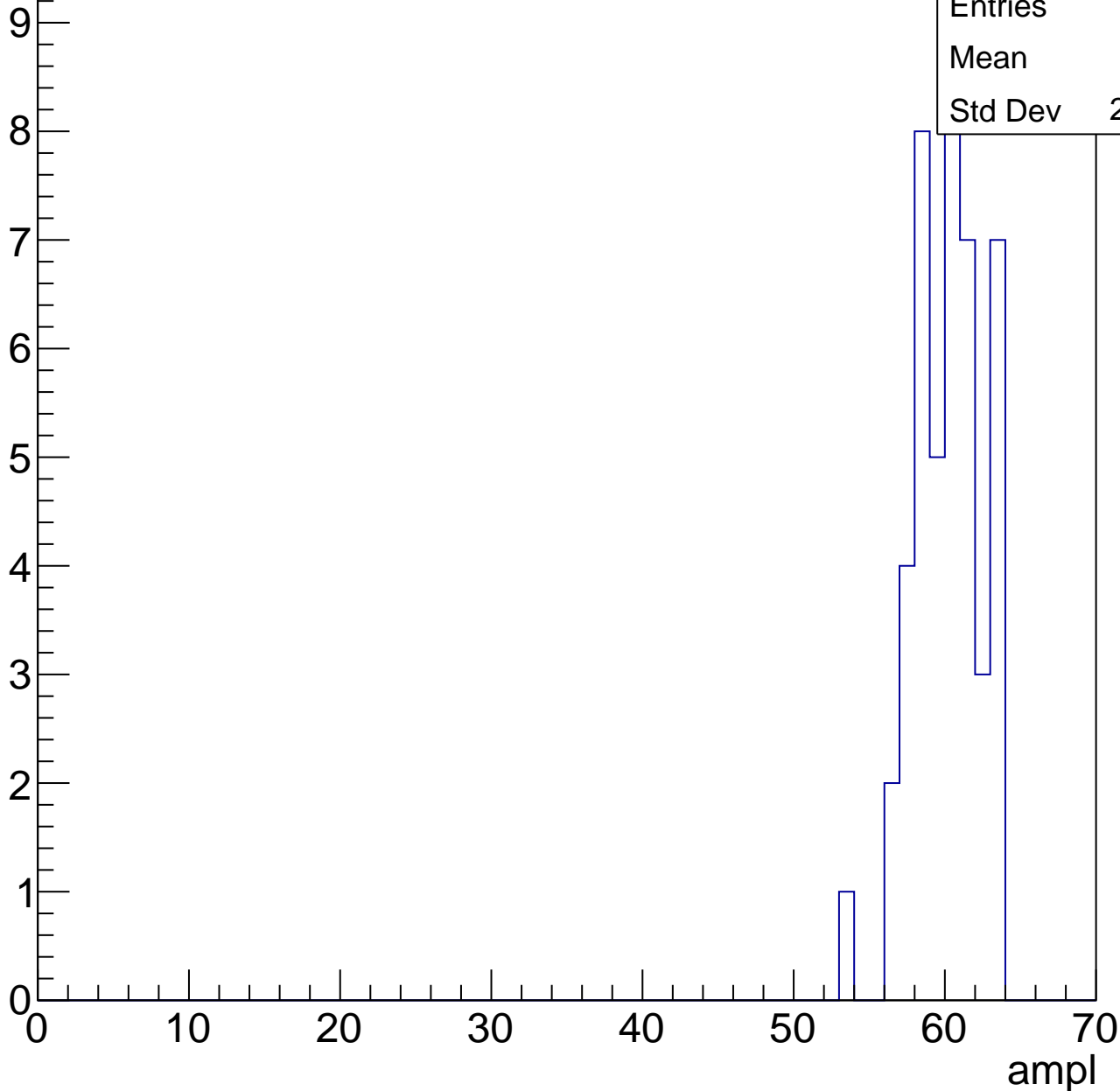


# B1L102S, U21-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	59.7
Std Dev	2.245

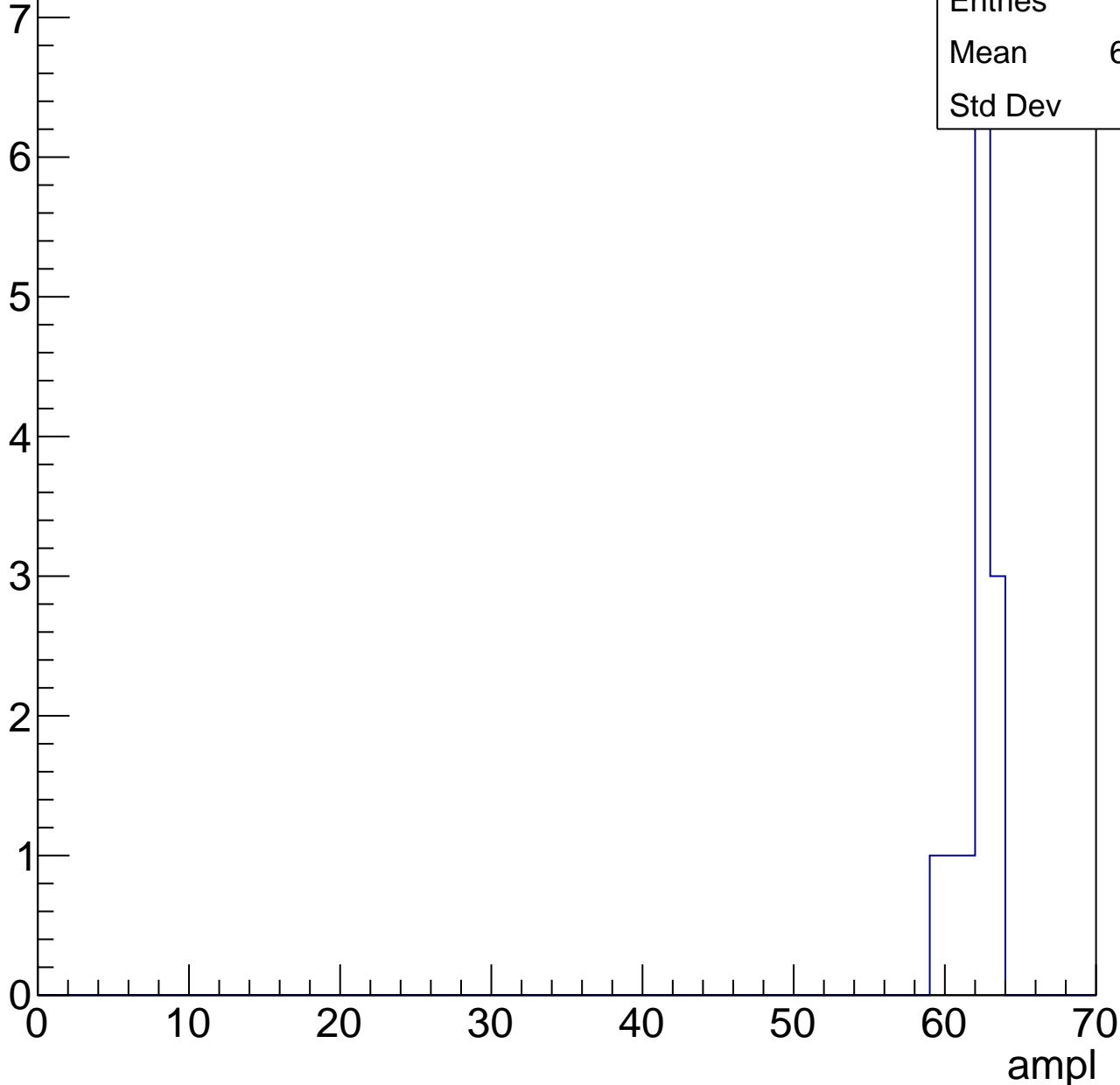


# B1L102S, U21-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	13
Mean	61.77
Std Dev	1.12





# B1L102S, U21-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U21-ch13, adc0

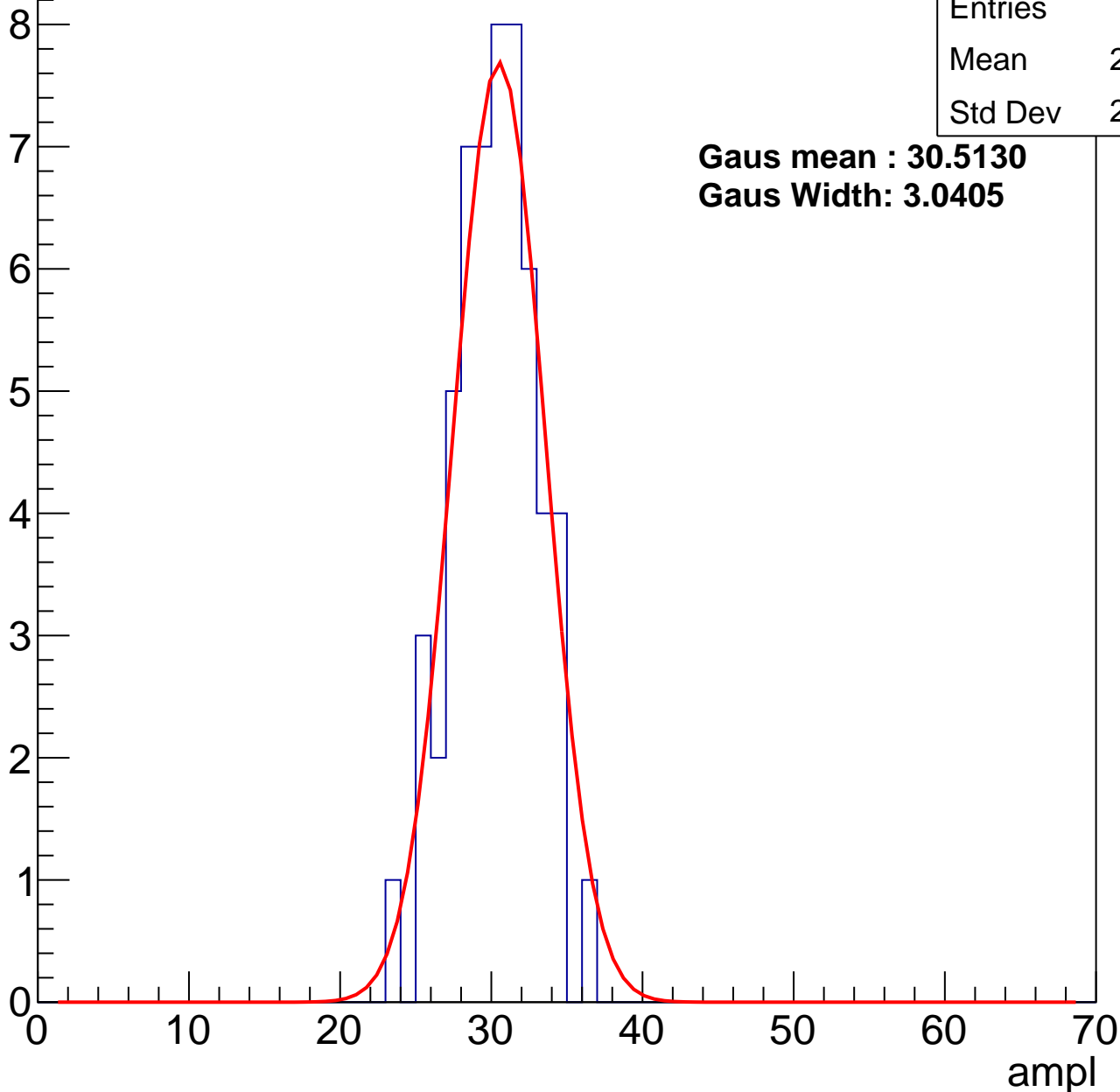
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	29.79
Std Dev	2.677

**Gaus mean : 30.5130**

**Gaus Width: 3.0405**



# B1L102S, U21-ch13, adc1

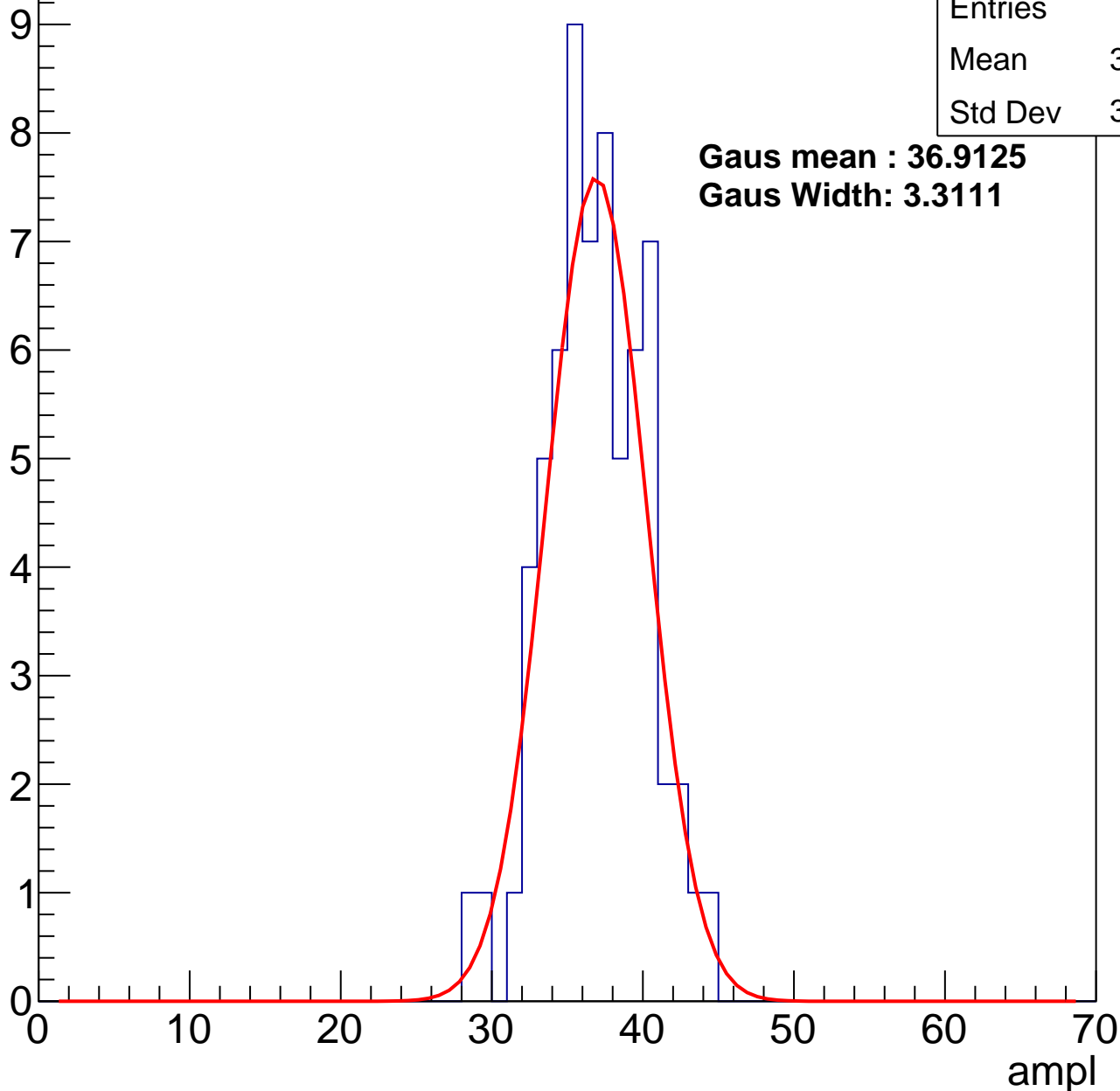
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	36.44
Std Dev	3.248

**Gaus mean : 36.9125**

**Gaus Width: 3.3111**



# B1L102S, U21-ch13, adc2

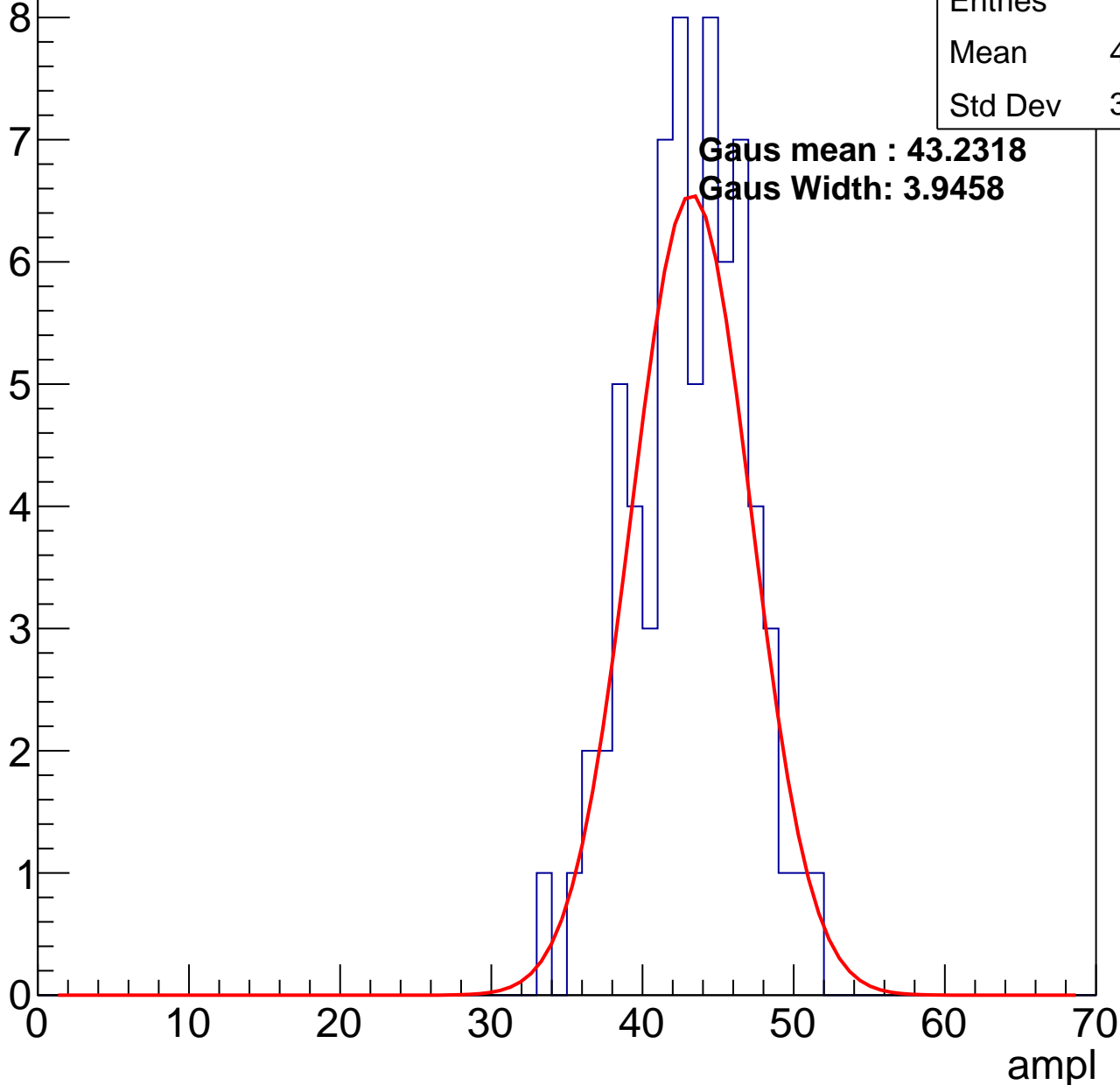
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	42.67
Std Dev	3.733

**Gaus mean : 43.2318**

**Gaus Width: 3.9458**

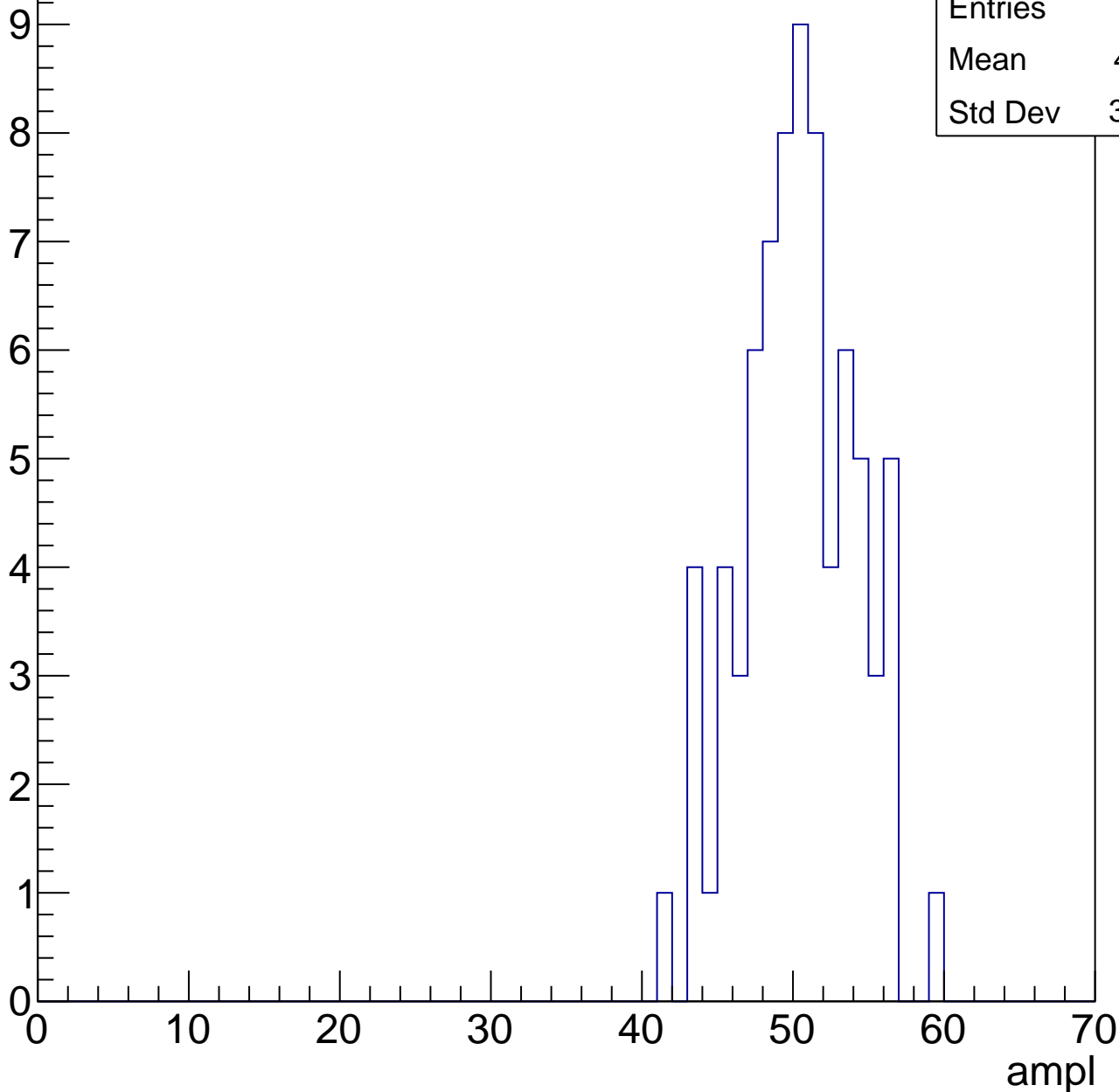


# B1L102S, U21-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	49.91
Std Dev	3.732

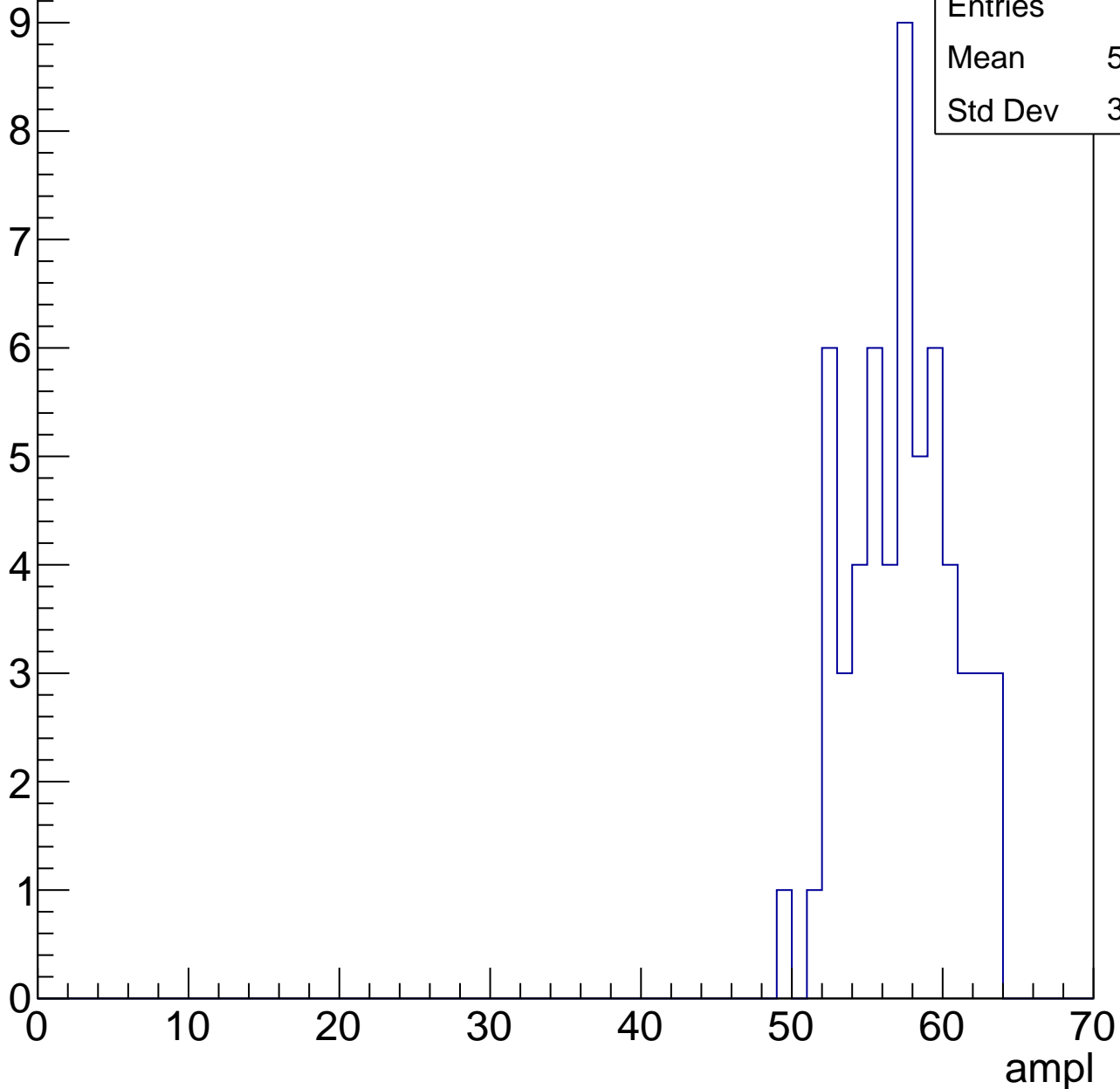


# B1L102S, U21-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	56.83
Std Dev	3.364

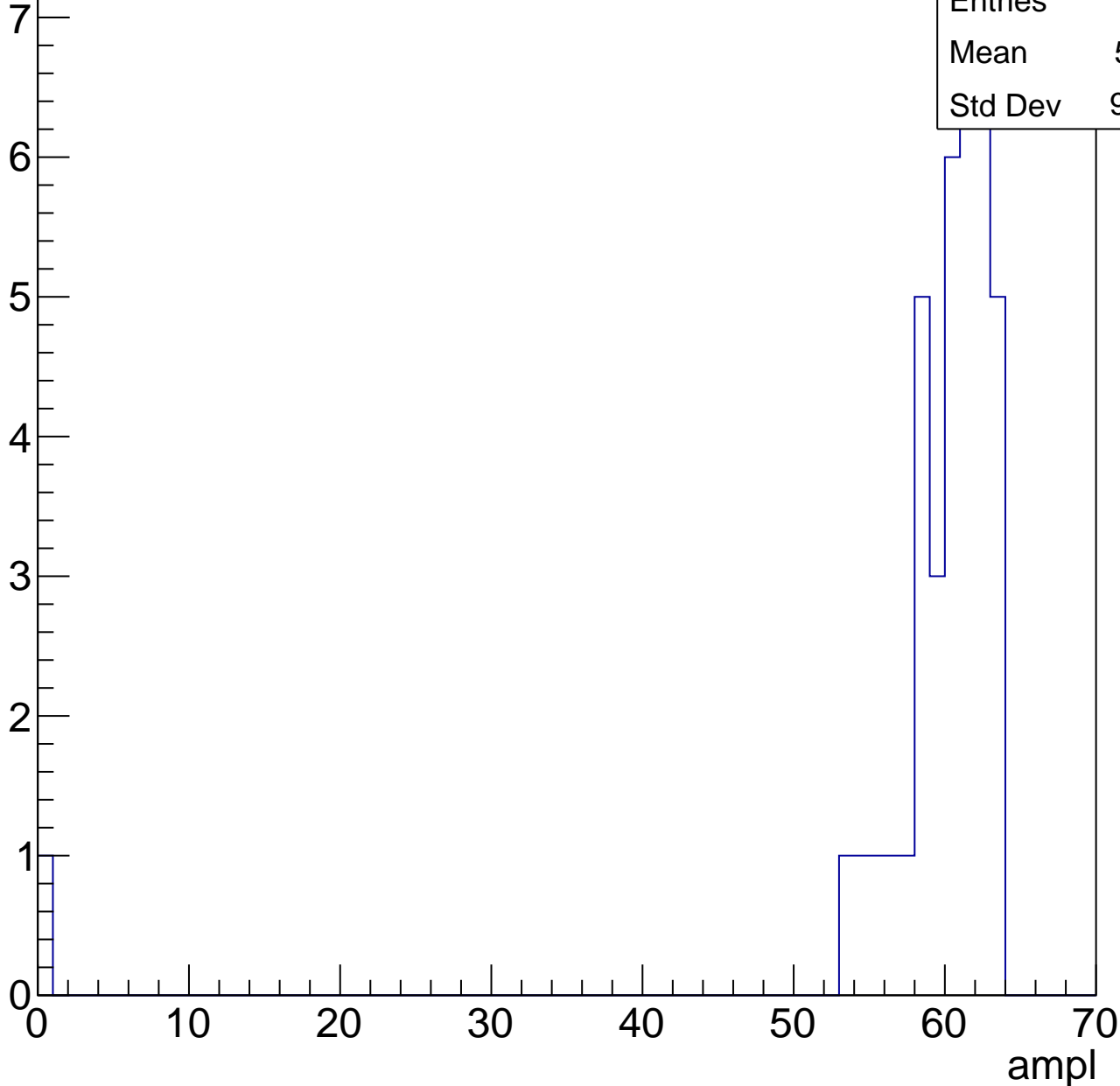


# B1L102S, U21-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	39
Mean	58.41
Std Dev	9.792



# B1L102S, U21-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U21-ch14, adc0

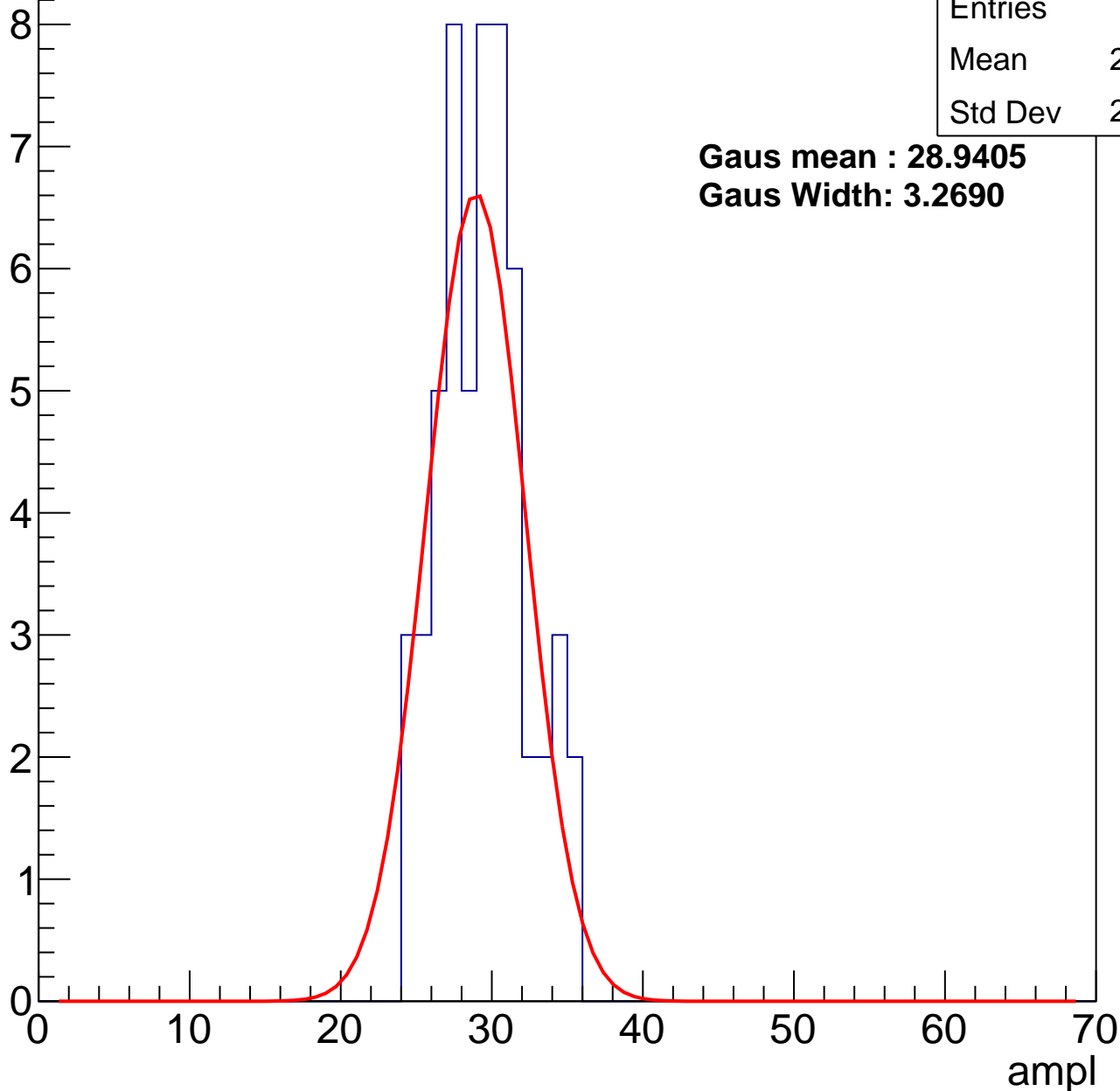
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	28.96
Std Dev	2.809

**Gaus mean : 28.9405**

**Gaus Width: 3.2690**



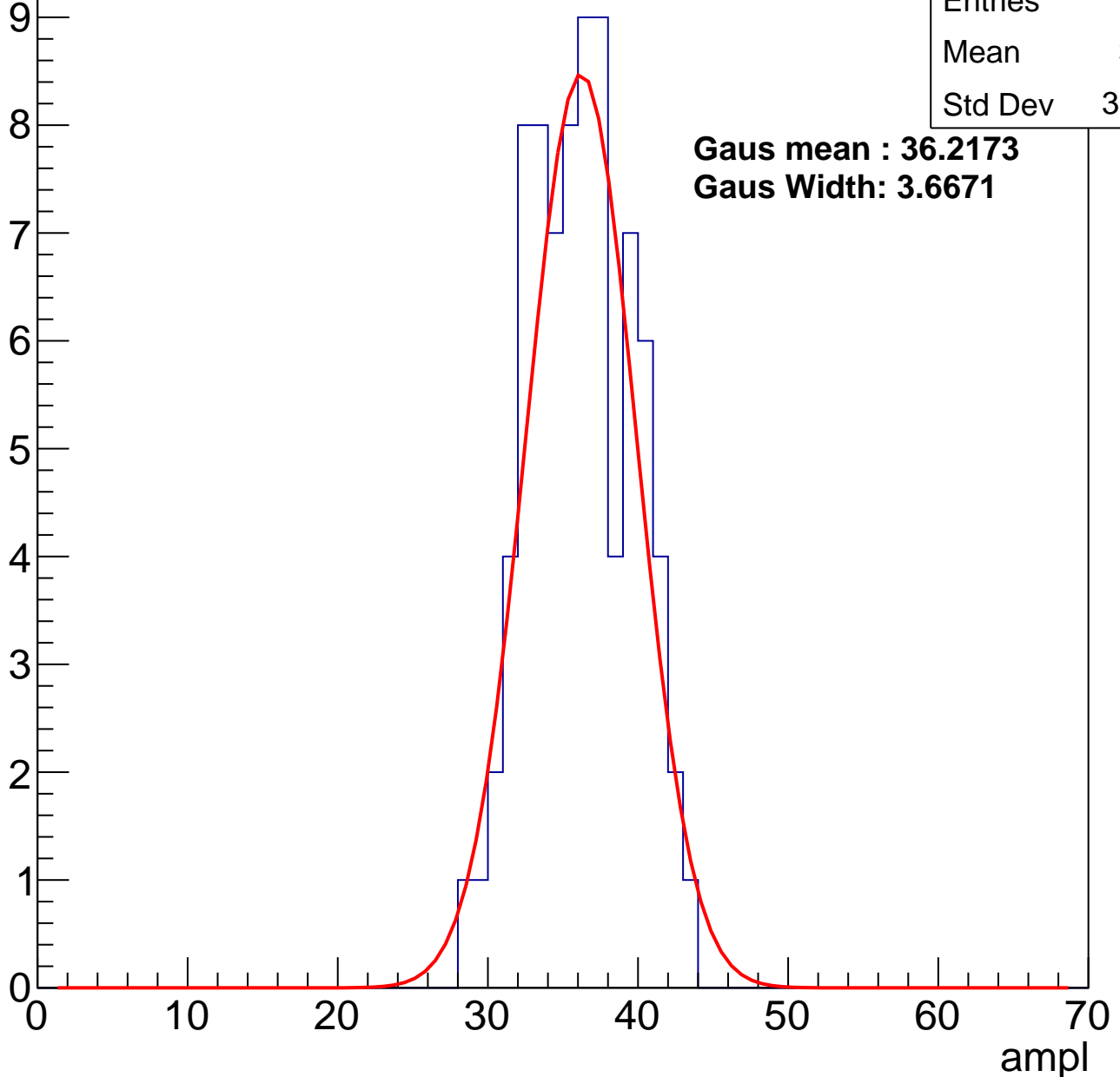
# B1L102S, U21-ch14, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	81
Mean	35.7
Std Dev	3.368

**Gaus mean : 36.2173**  
**Gaus Width: 3.6671**



# B1L102S, U21-ch14, adc2

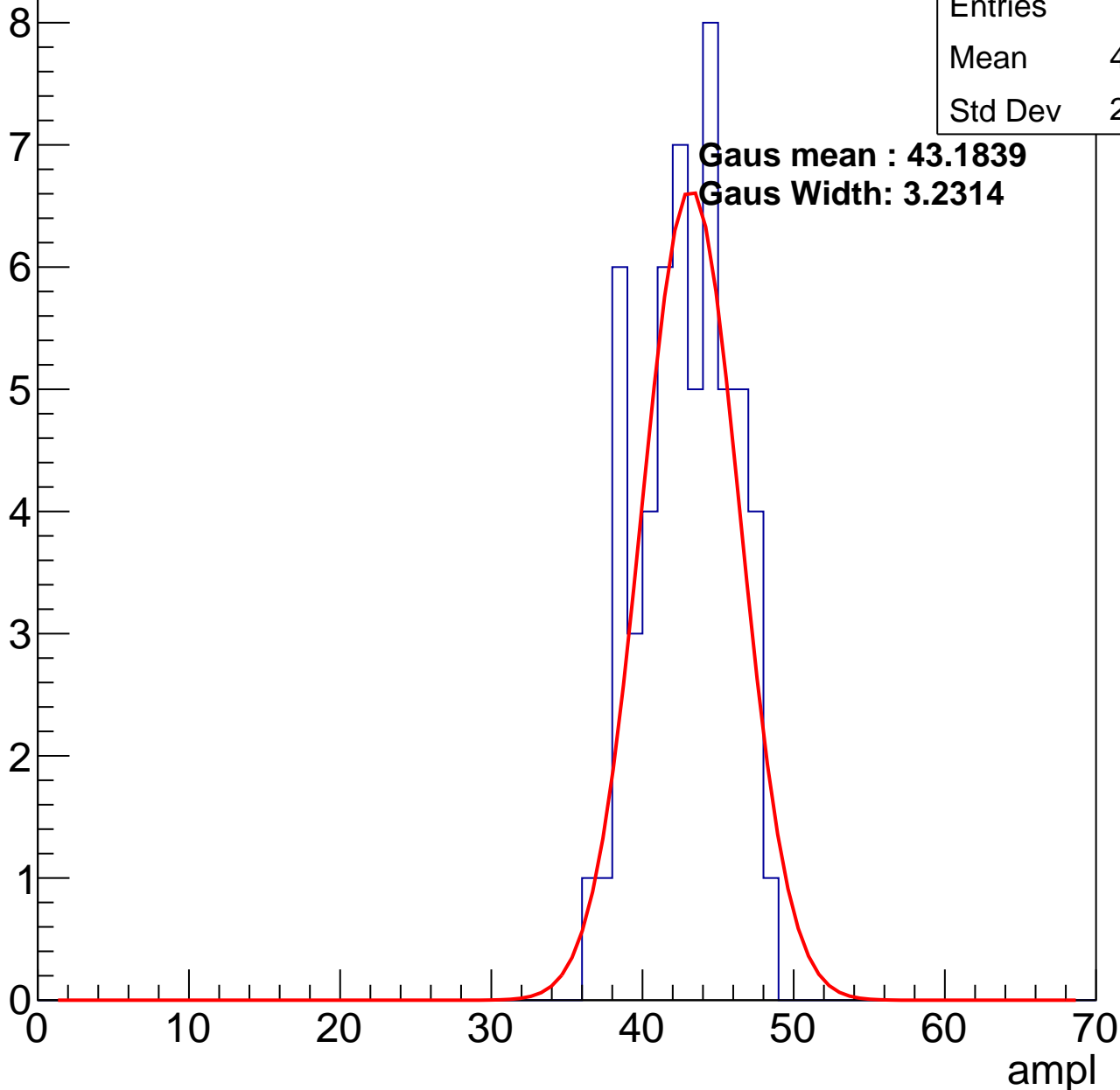
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	42.43
Std Dev	2.969

**Gaus mean : 43.1839**

**Gaus Width: 3.2314**

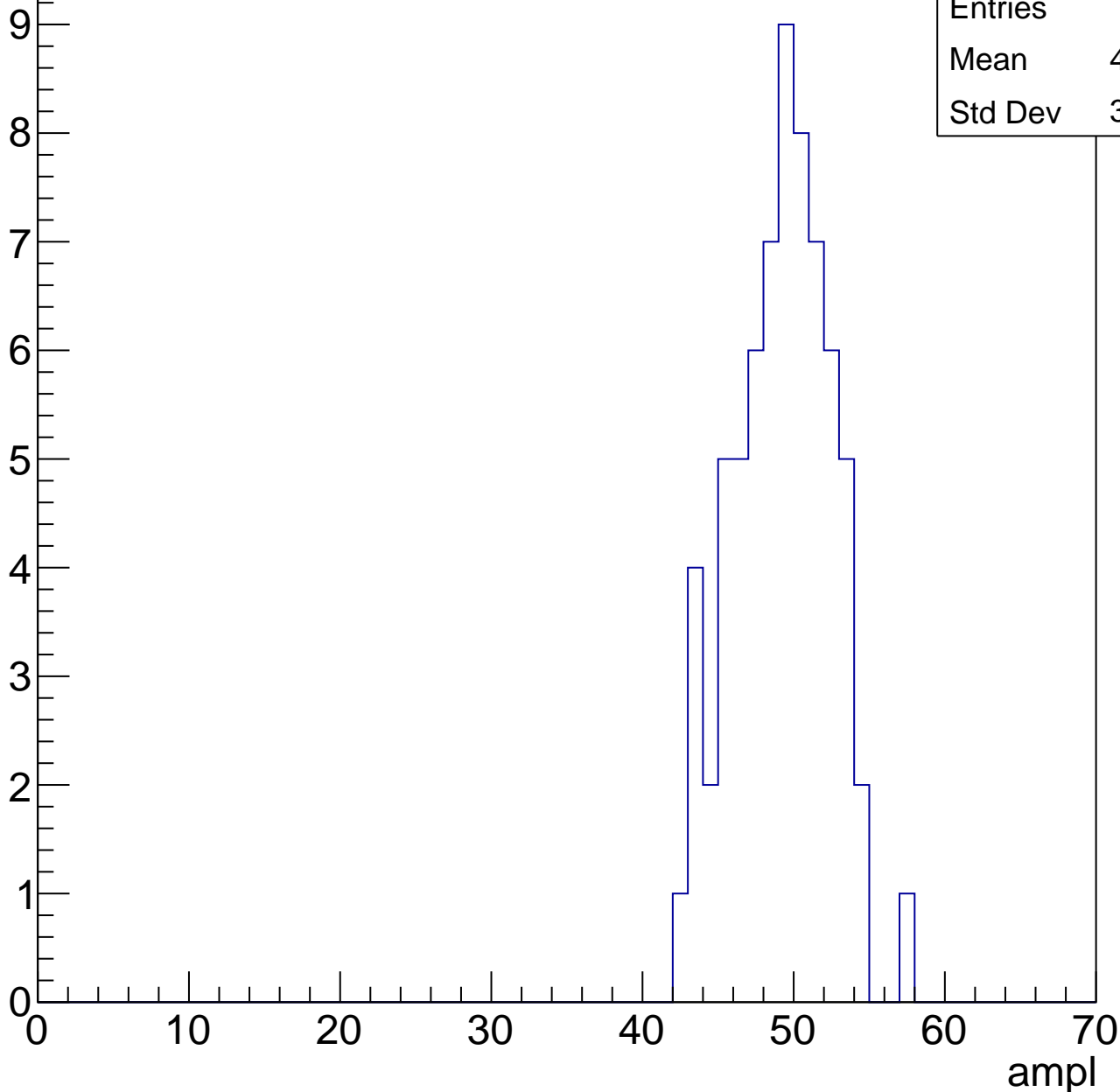


# B1L102S, U21-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	48.75
Std Dev	3.159



# B1L102S, U21-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

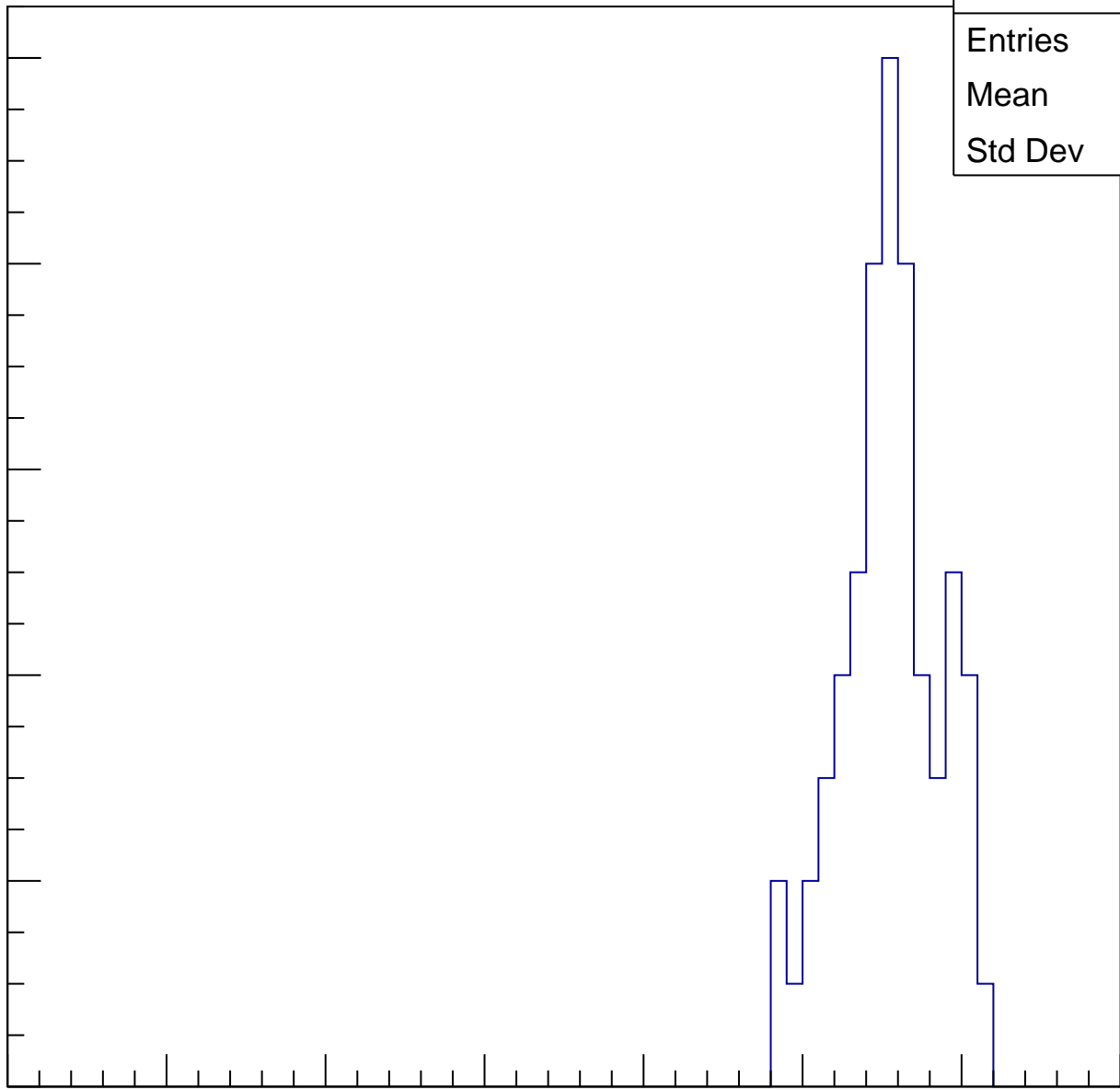
Entries	60
Mean	54.98
Std Dev	3.063

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

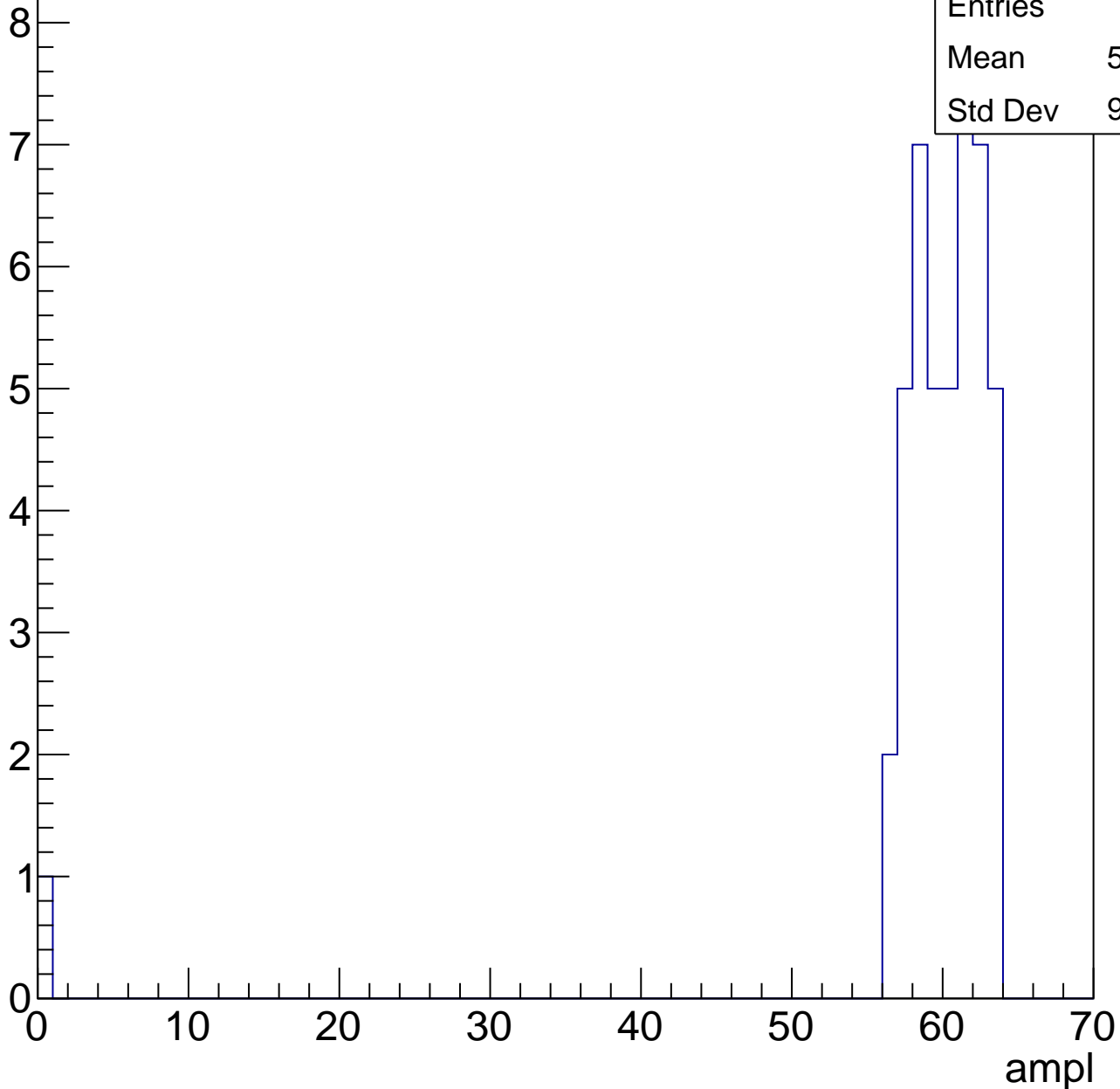


# B1L102S, U21-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	58.56
Std Dev	9.064

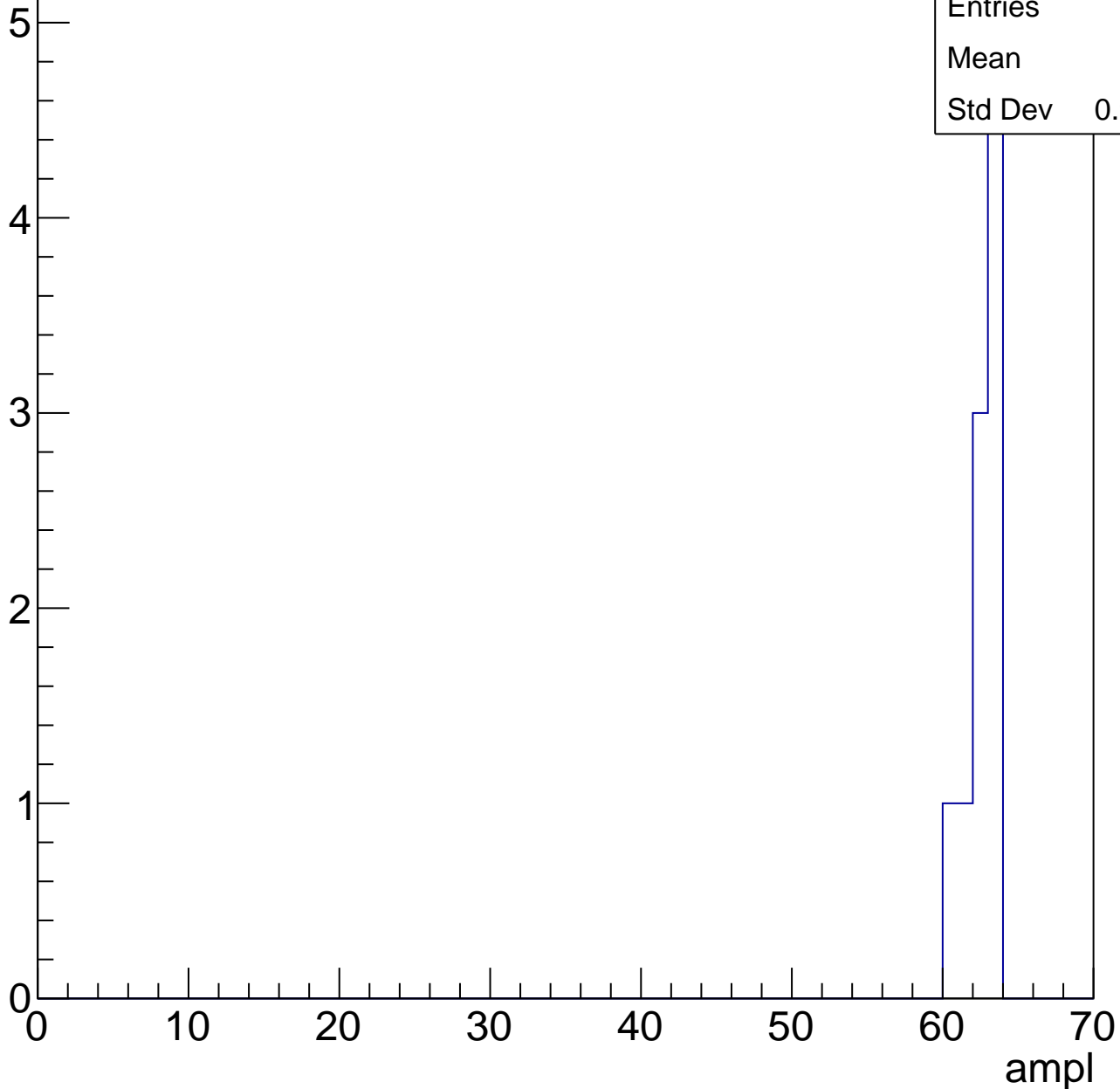


# B1L102S, U21-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	10
Mean	62.2
Std Dev	0.9798





# B1L102S, U21-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch15, adc0

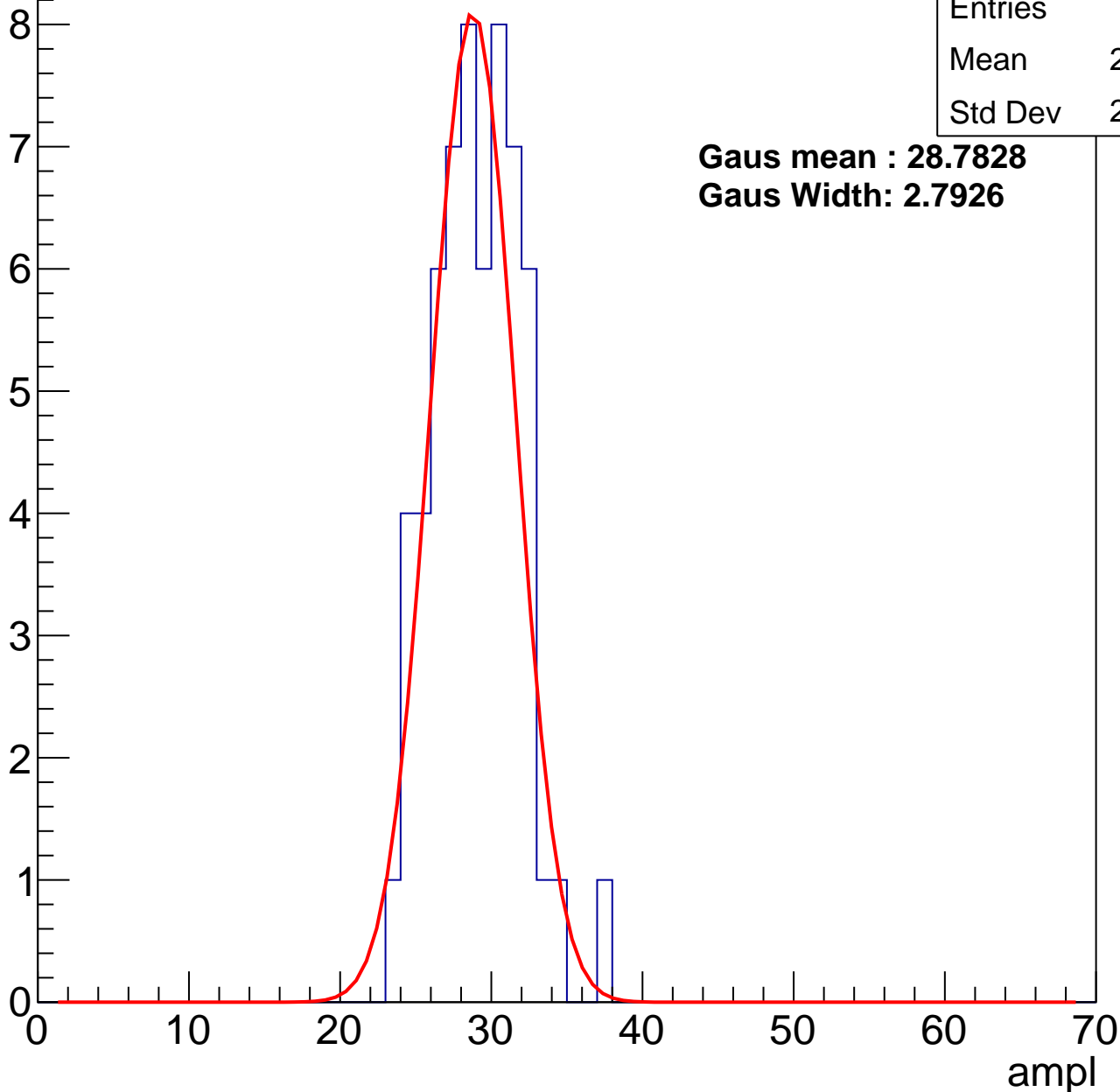
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	28.58
Std Dev	2.812

**Gaus mean : 28.7828**

**Gaus Width: 2.7926**



# B1L102S, U21-ch15, adc1

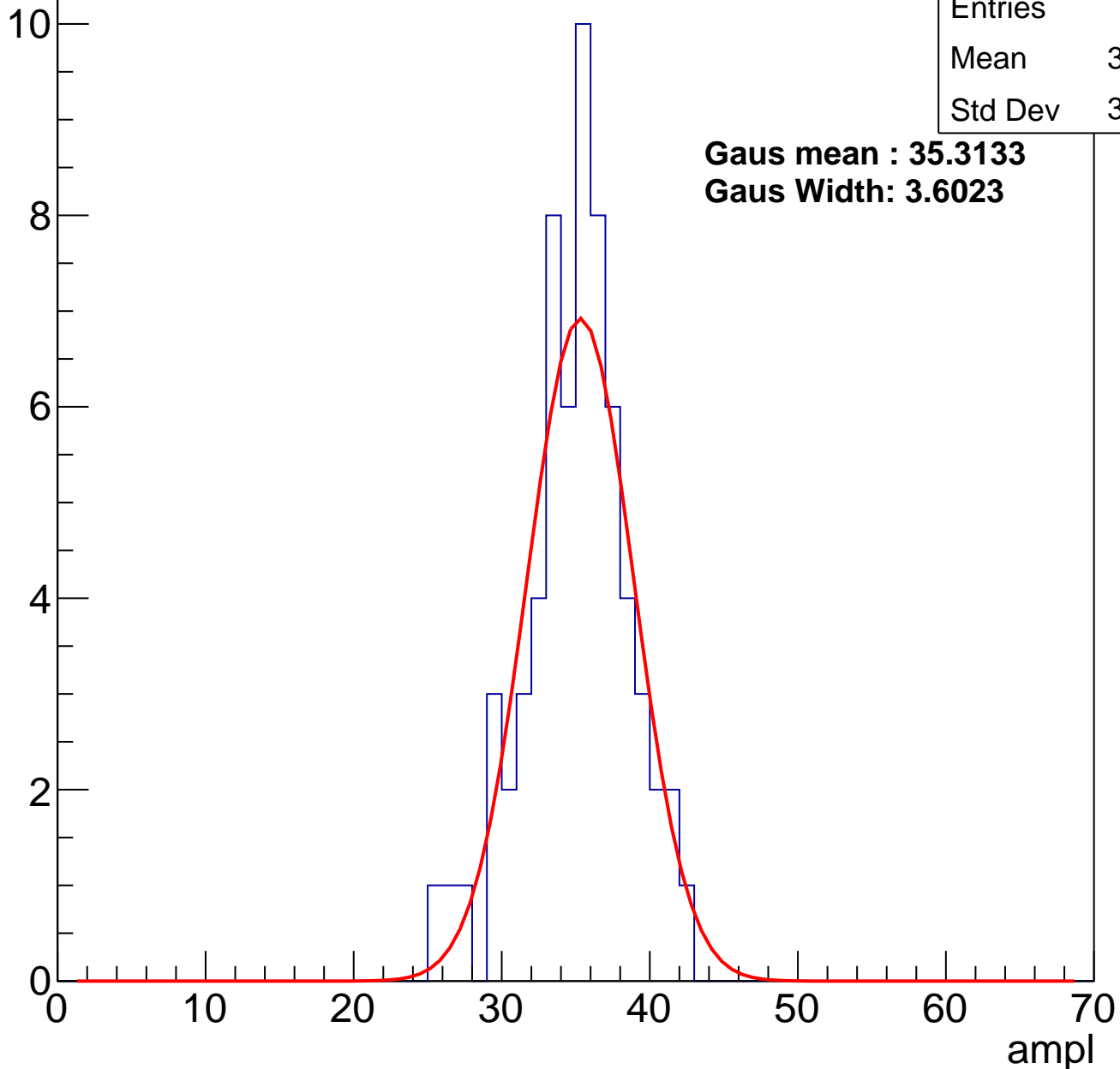
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	65
Mean	34.57
Std Dev	3.508

**Gaus mean : 35.3133**

**Gaus Width: 3.6023**

Entry



# B1L102S, U21-ch15, adc2

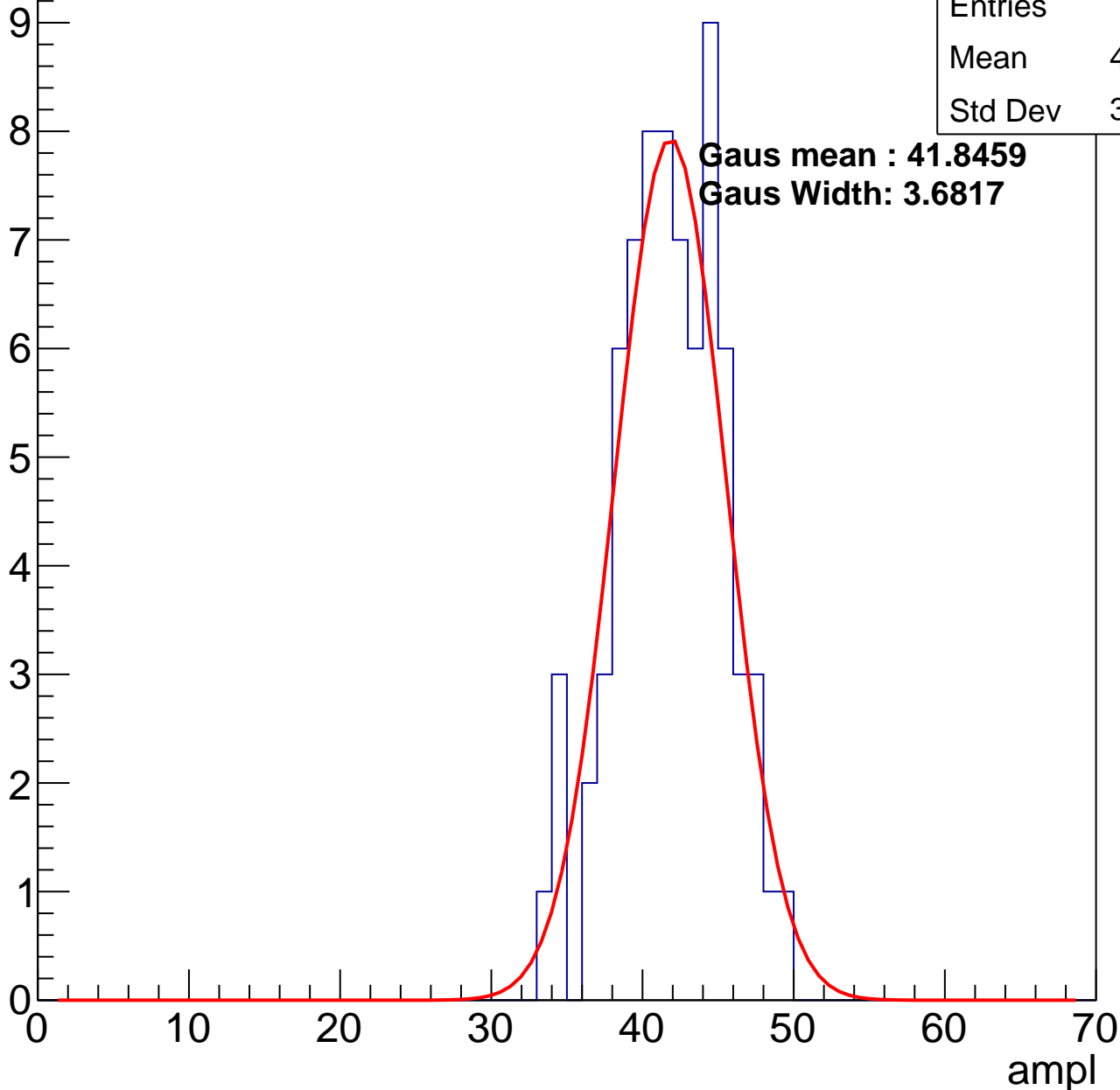
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	41.36
Std Dev	3.474

**Gaus mean : 41.8459**

**Gaus Width: 3.6817**

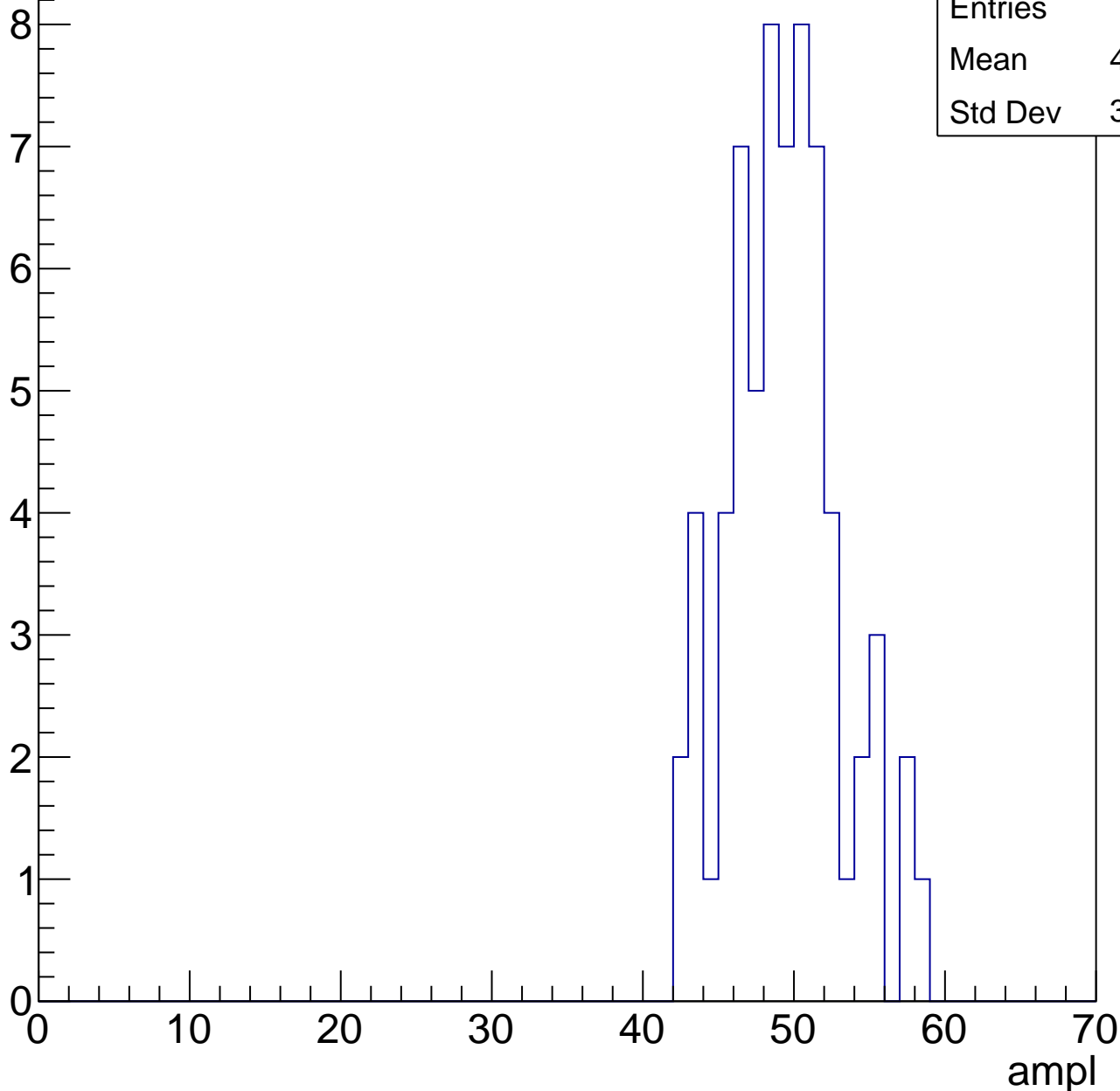


# B1L102S, U21-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	48.89
Std Dev	3.644

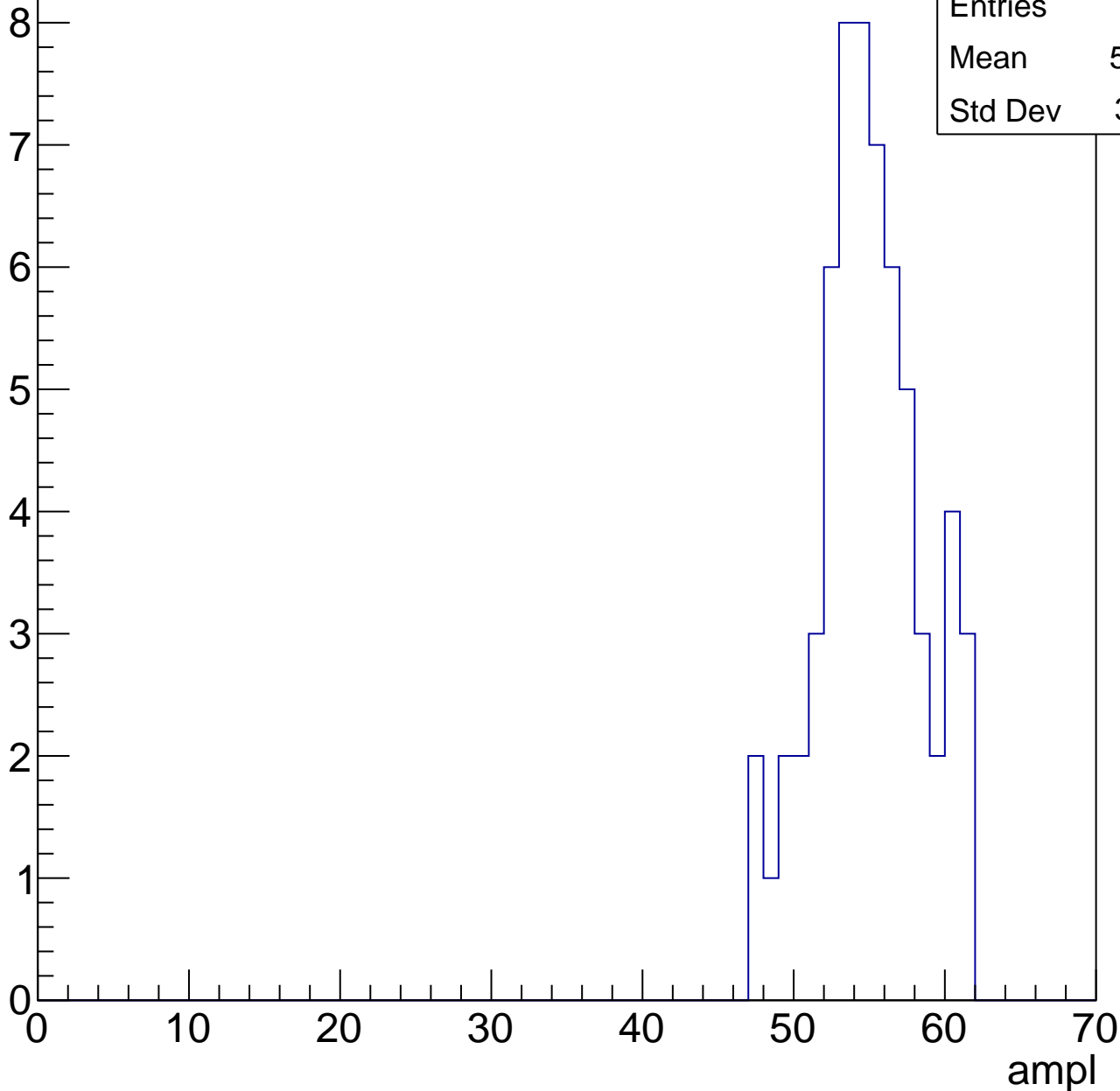


# B1L102S, U21-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	54.55
Std Dev	3.411

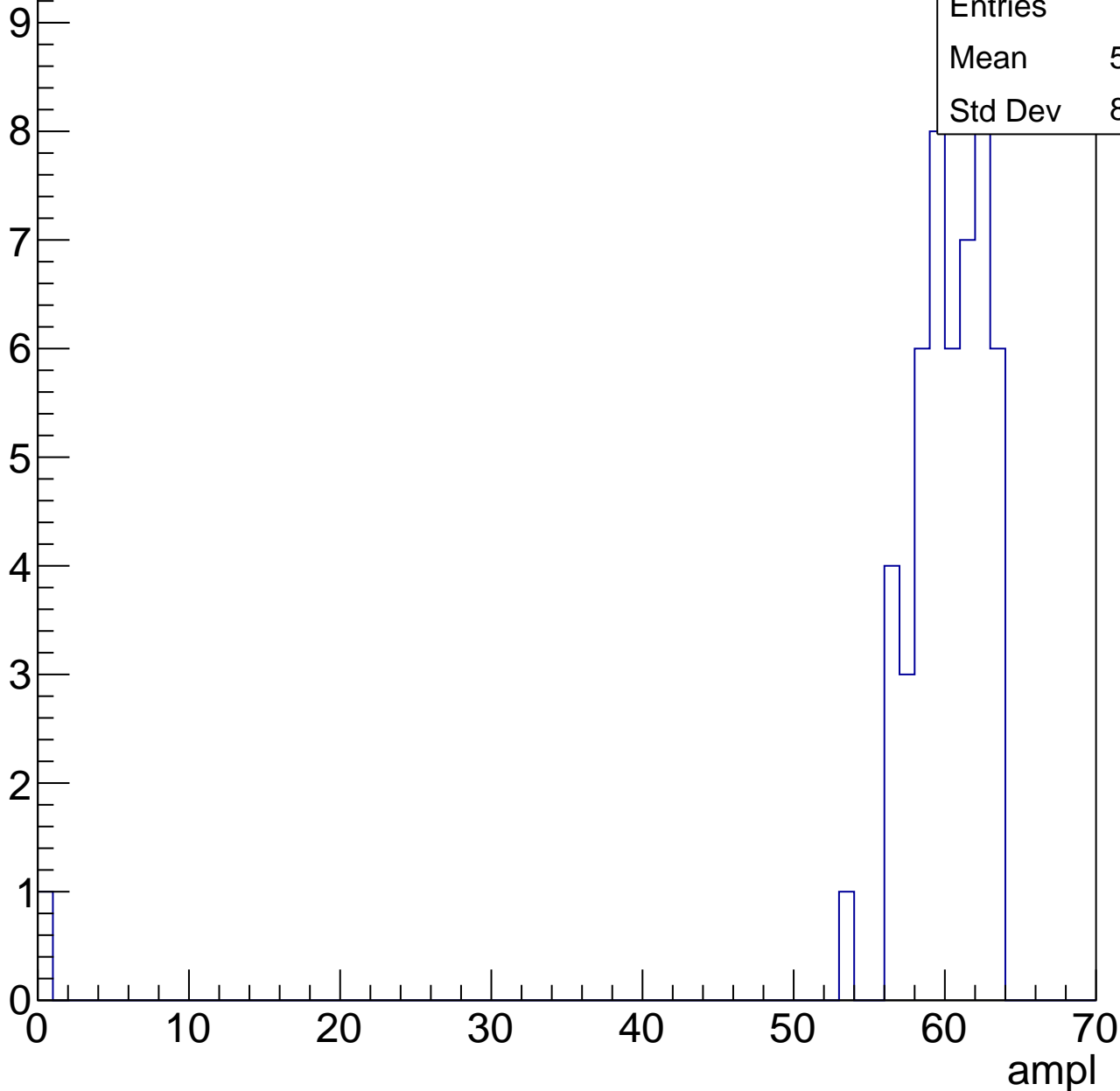


# B1L102S, U21-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	58.65
Std Dev	8.604



# B1L102S, U21-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	22
Std Dev	0

# B1L102S, U21-ch16, adc0

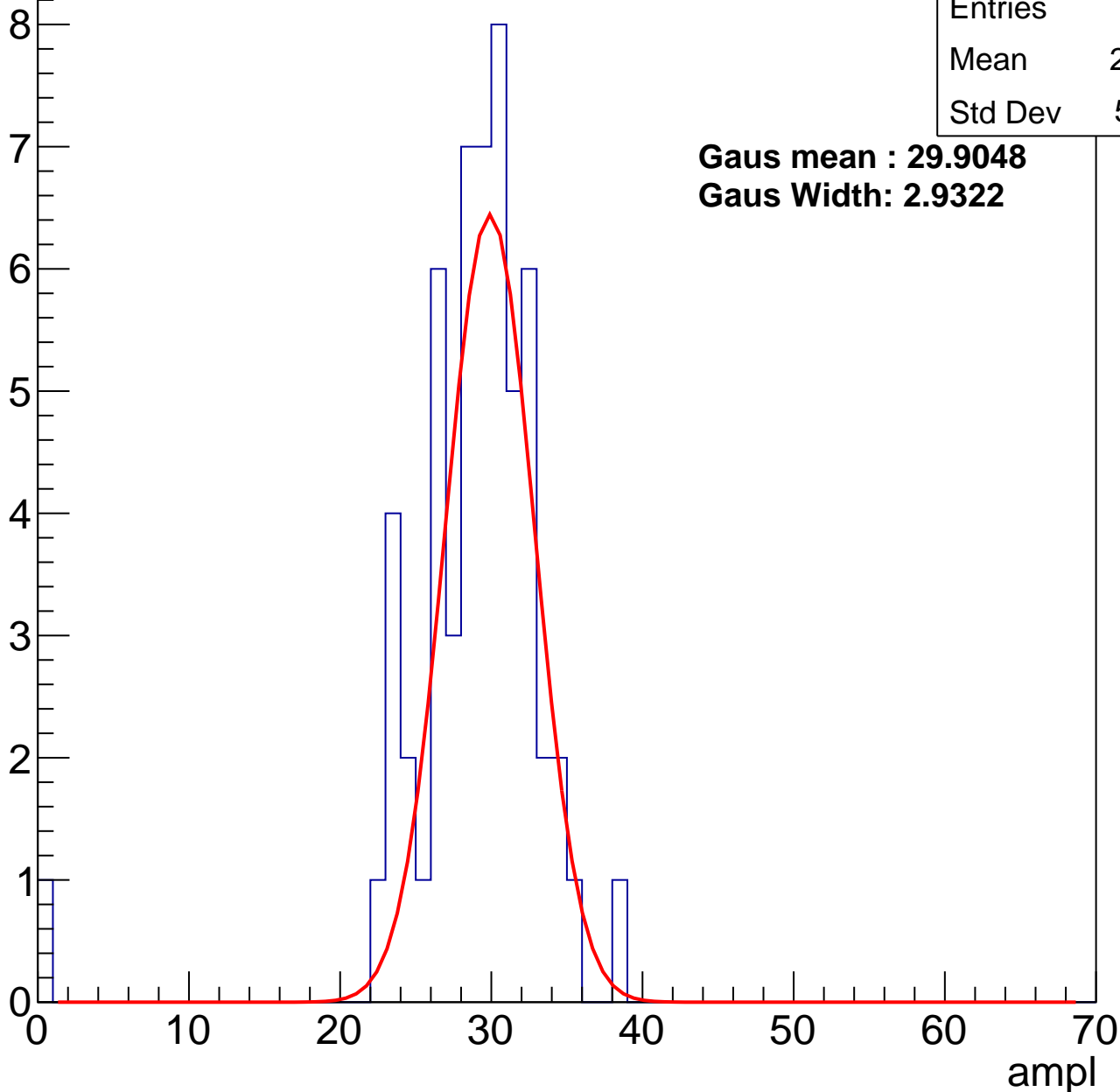
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	28.37
Std Dev	5.011

**Gaus mean : 29.9048**

**Gaus Width: 2.9322**



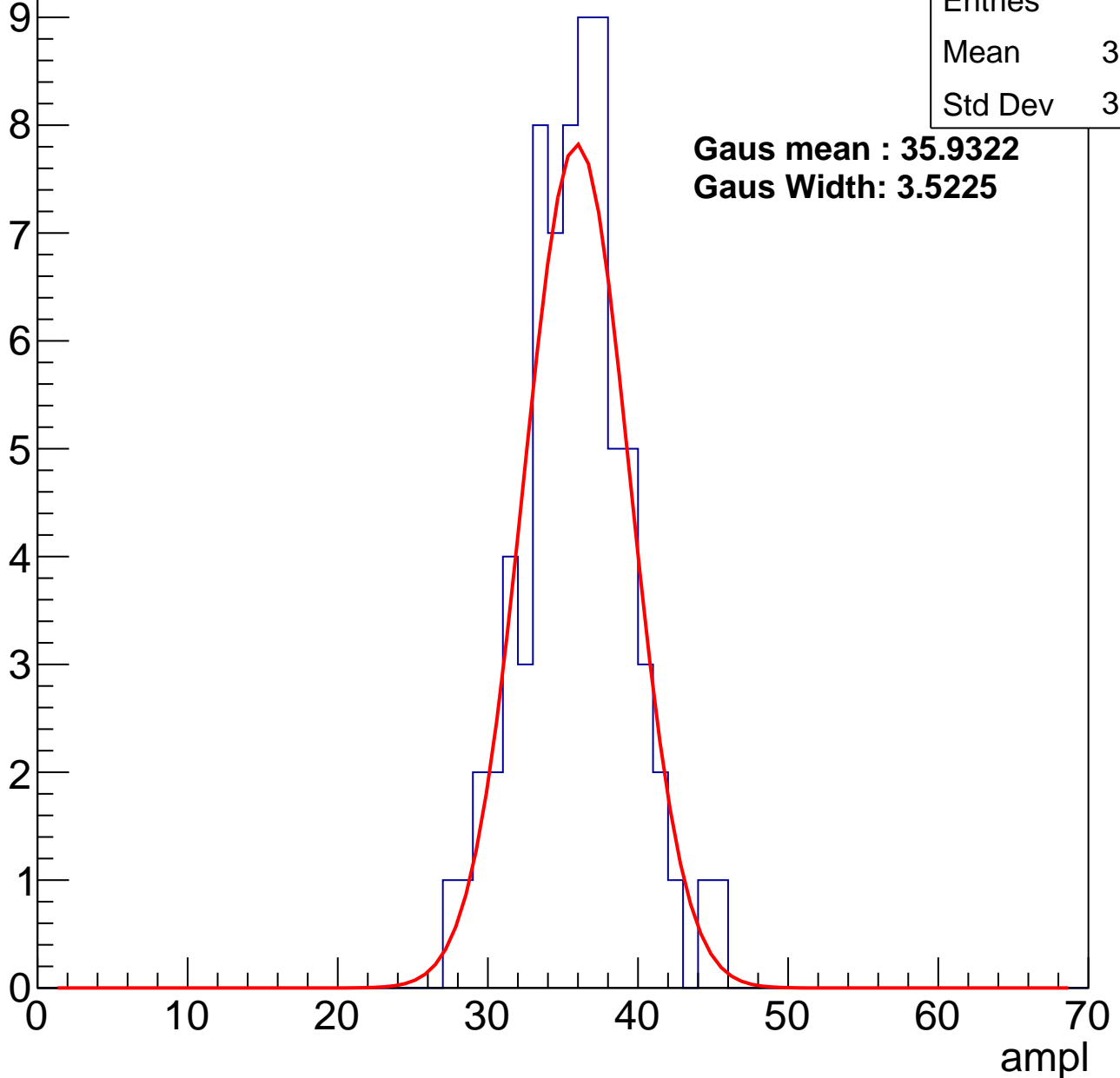
# B1L102S, U21-ch16, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	35.42
Std Dev	3.535

**Gaus mean : 35.9322**  
**Gaus Width: 3.5225**



# B1L102S, U21-ch16, adc2

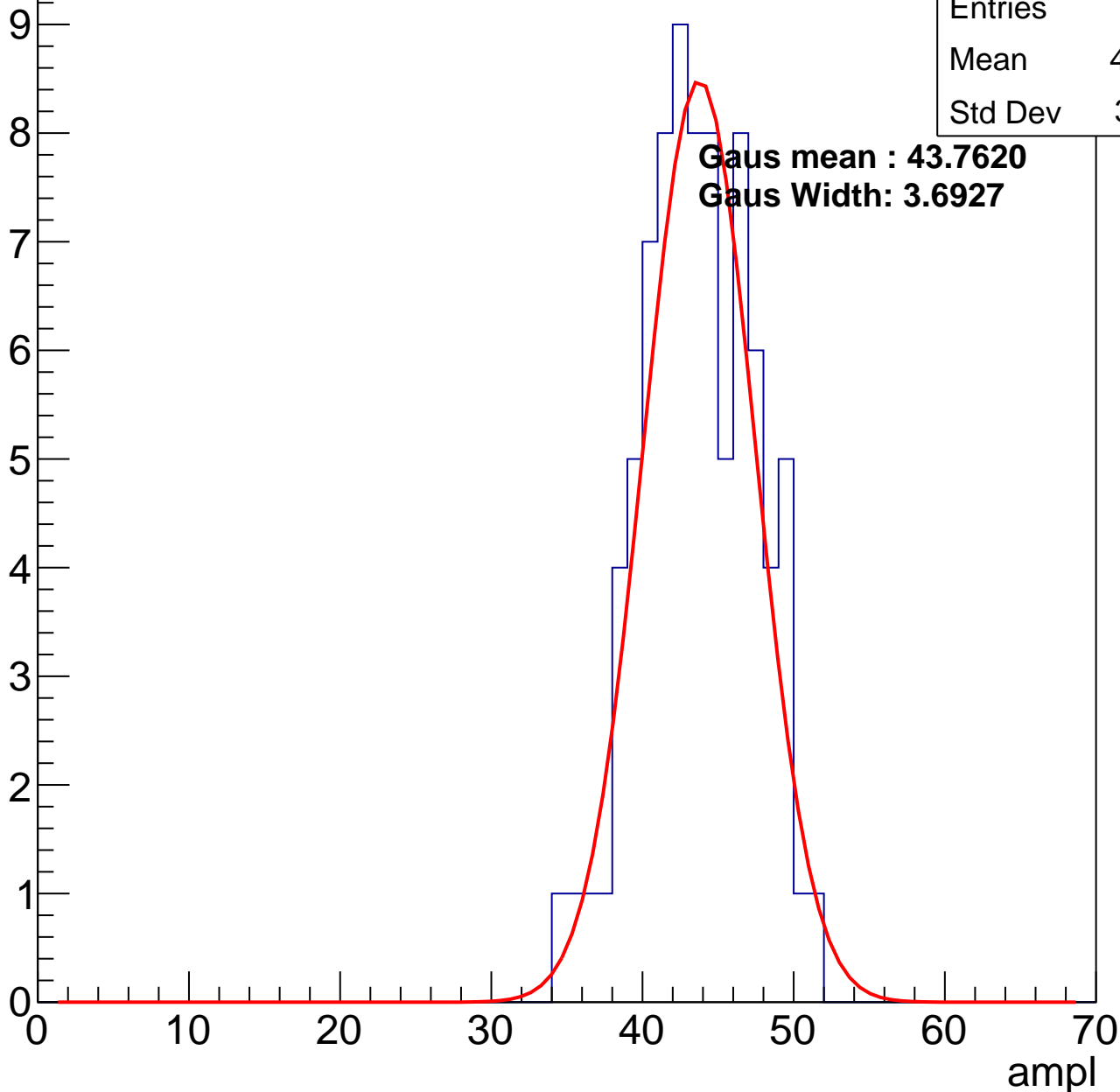
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	83
Mean	43.18
Std Dev	3.641

**Gaus mean : 43.7620**

**Gaus Width: 3.6927**

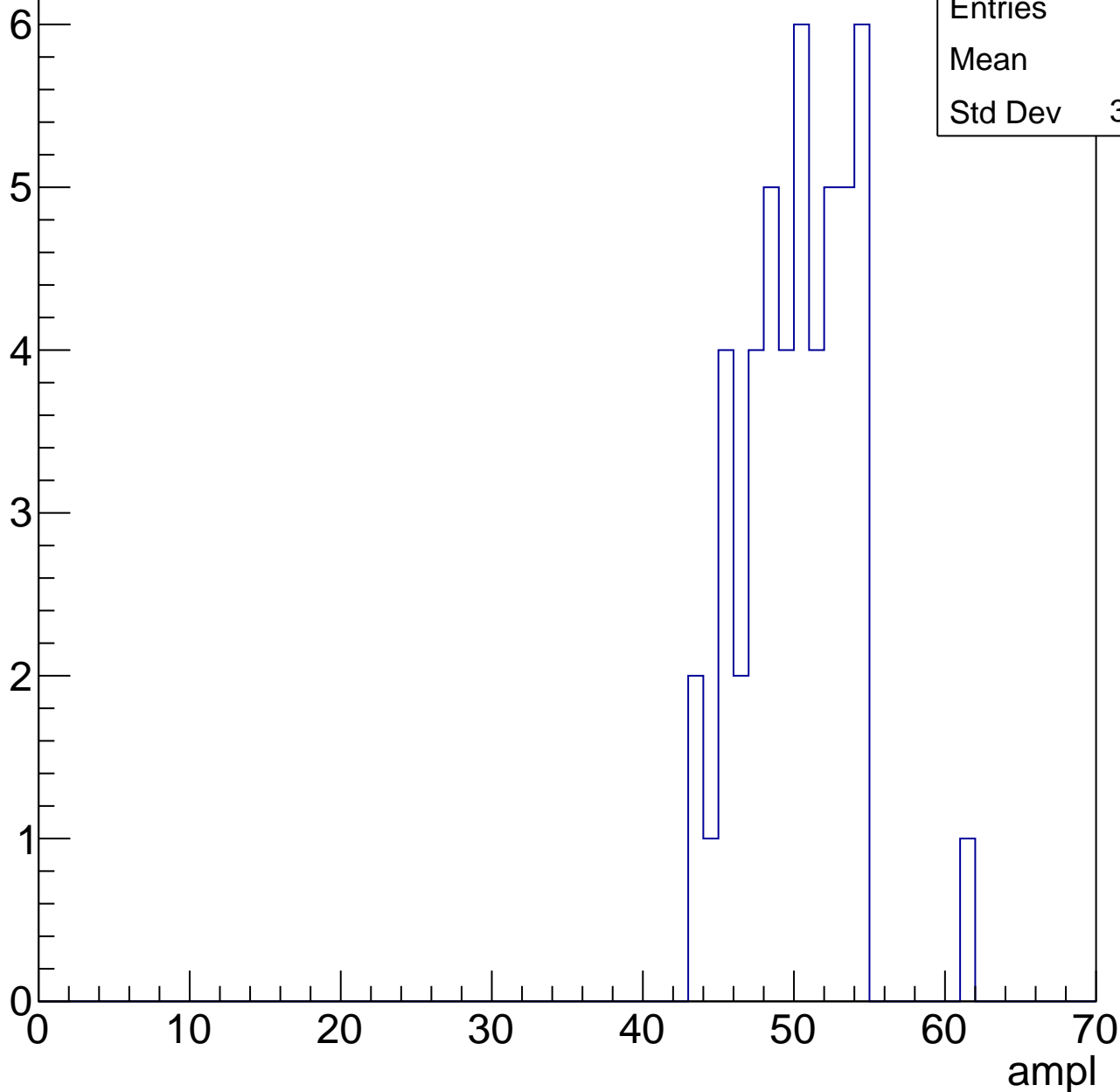


# B1L102S, U21-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	49.8
Std Dev	3.528



# B1L102S, U21-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	62
Mean	55.24
Std Dev	3.378

Entry

10

8

6

4

2

0

0

10

20

30

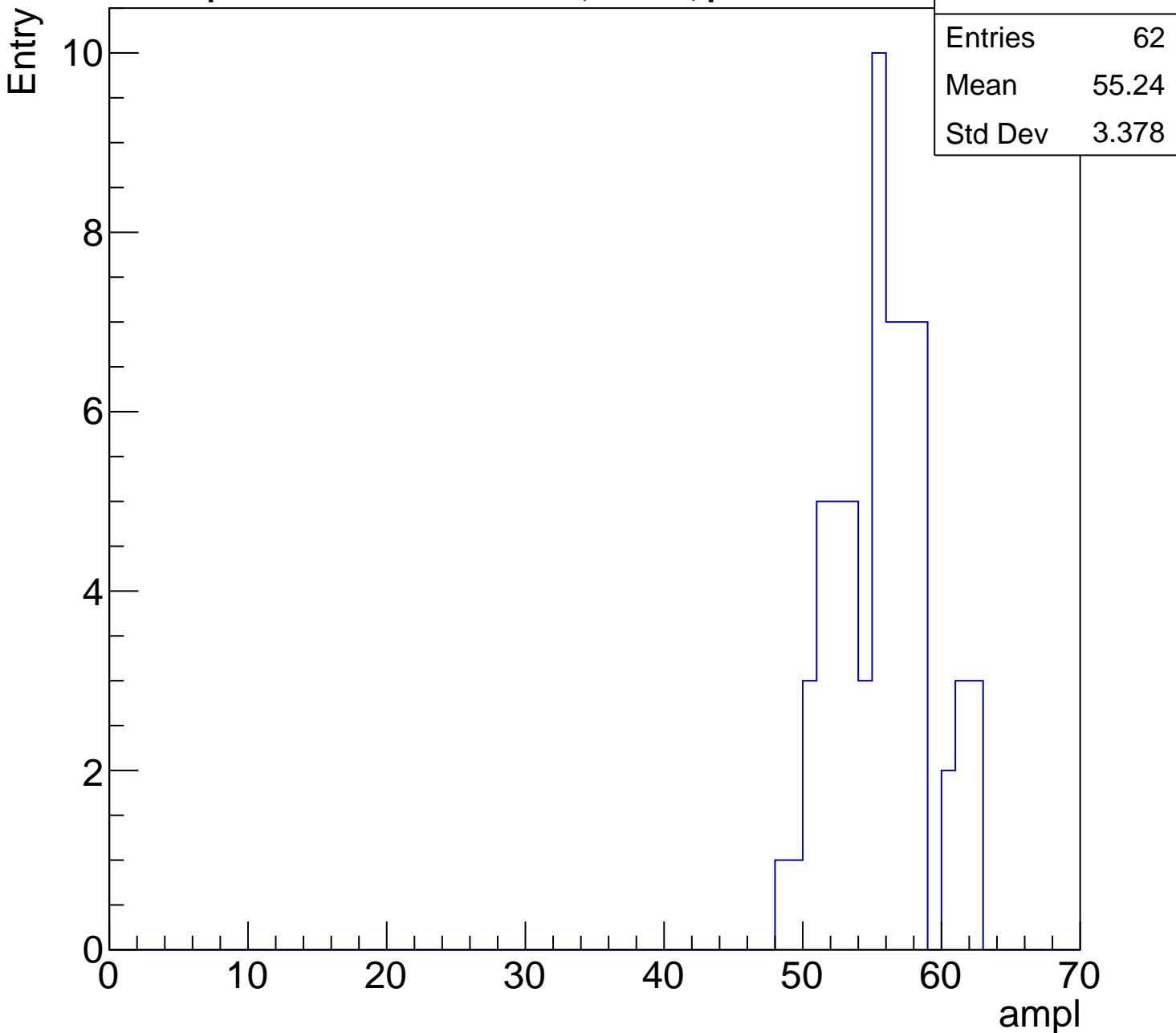
40

50

60

ampl

70

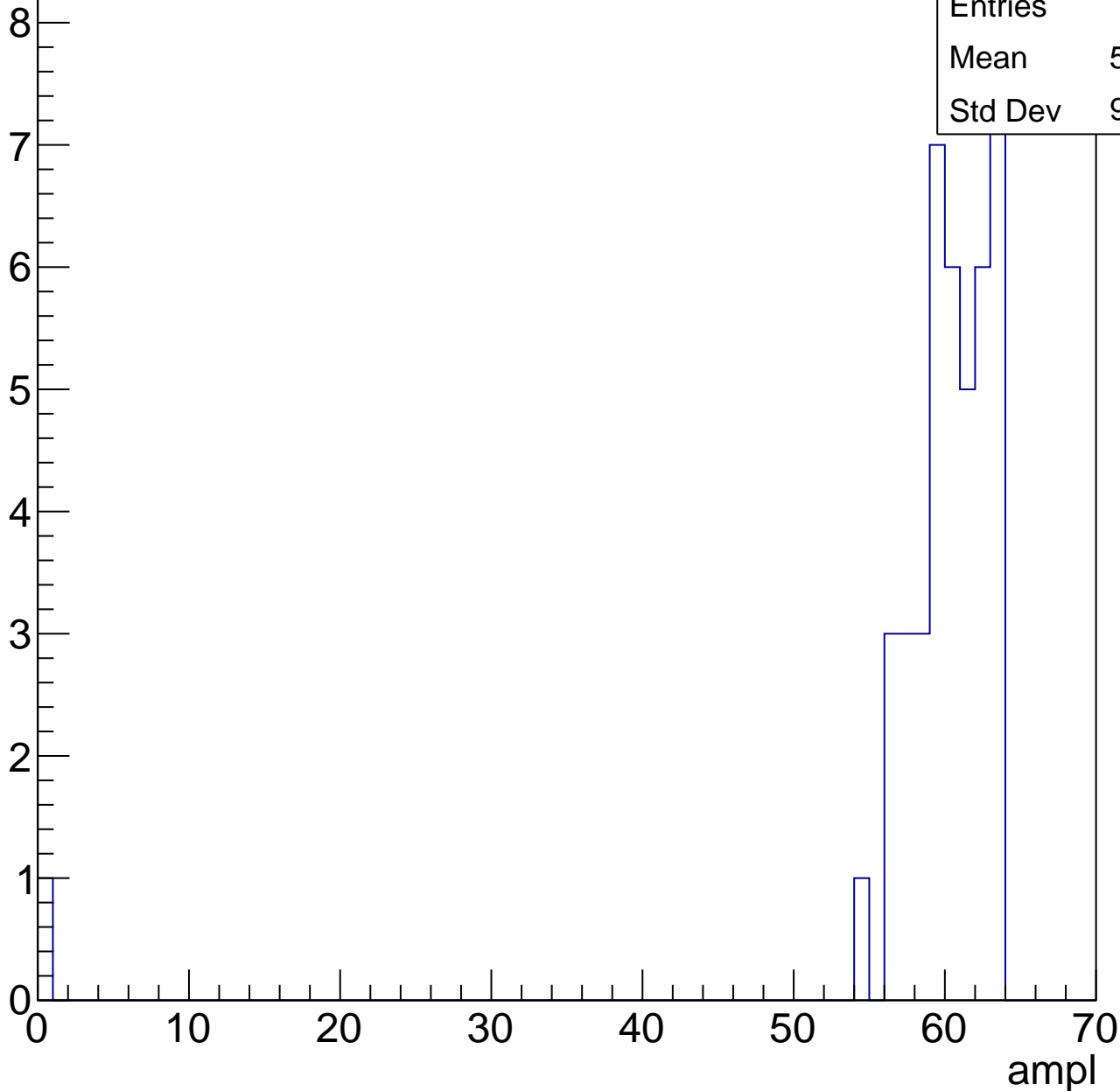


# B1L102S, U21-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	43
Mean	58.63
Std Dev	9.339



# B1L102S, U21-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

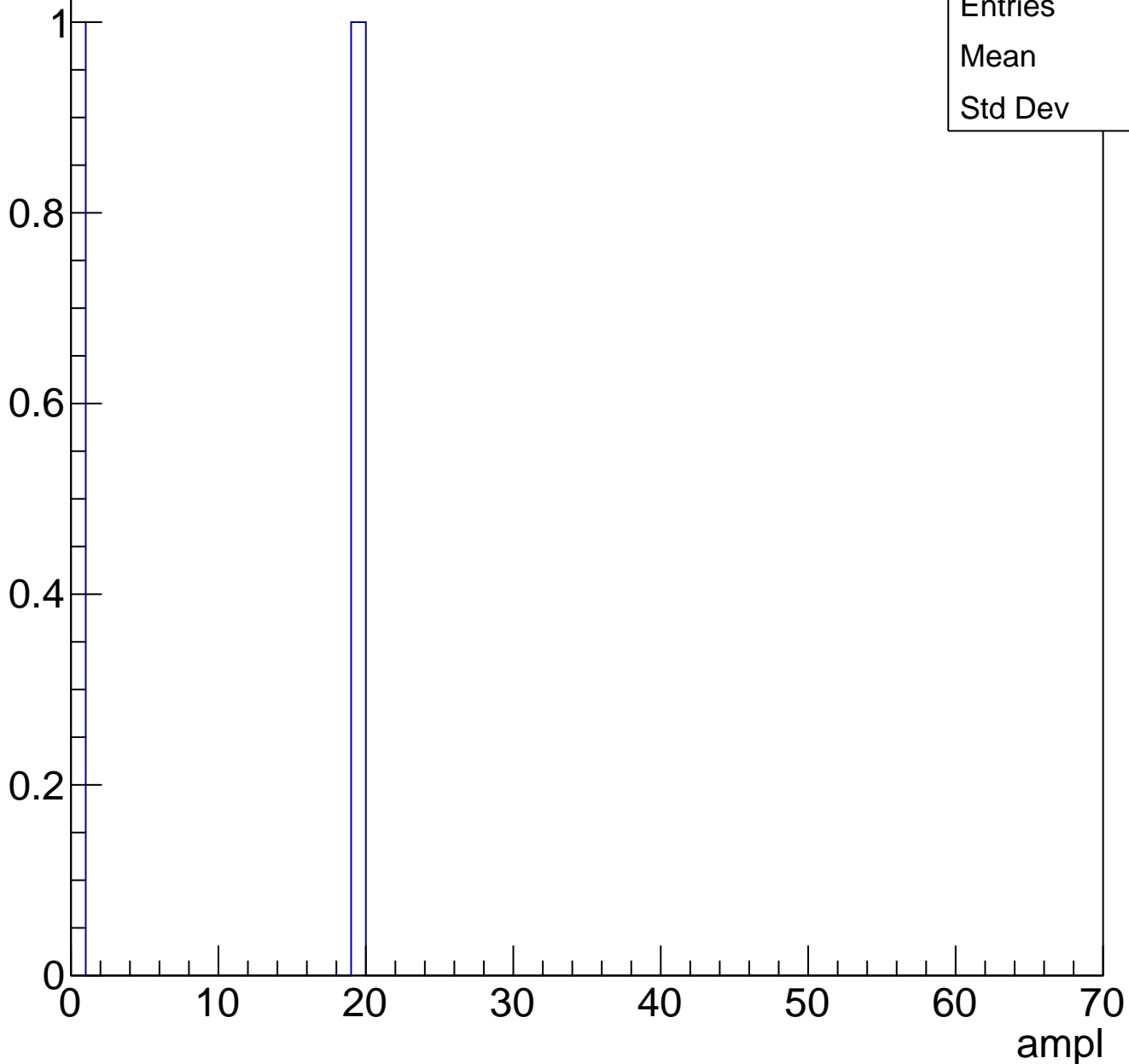
Entries	9
Mean	60.67
Std Dev	1.563



# B1L102S, U21-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch17, adc0

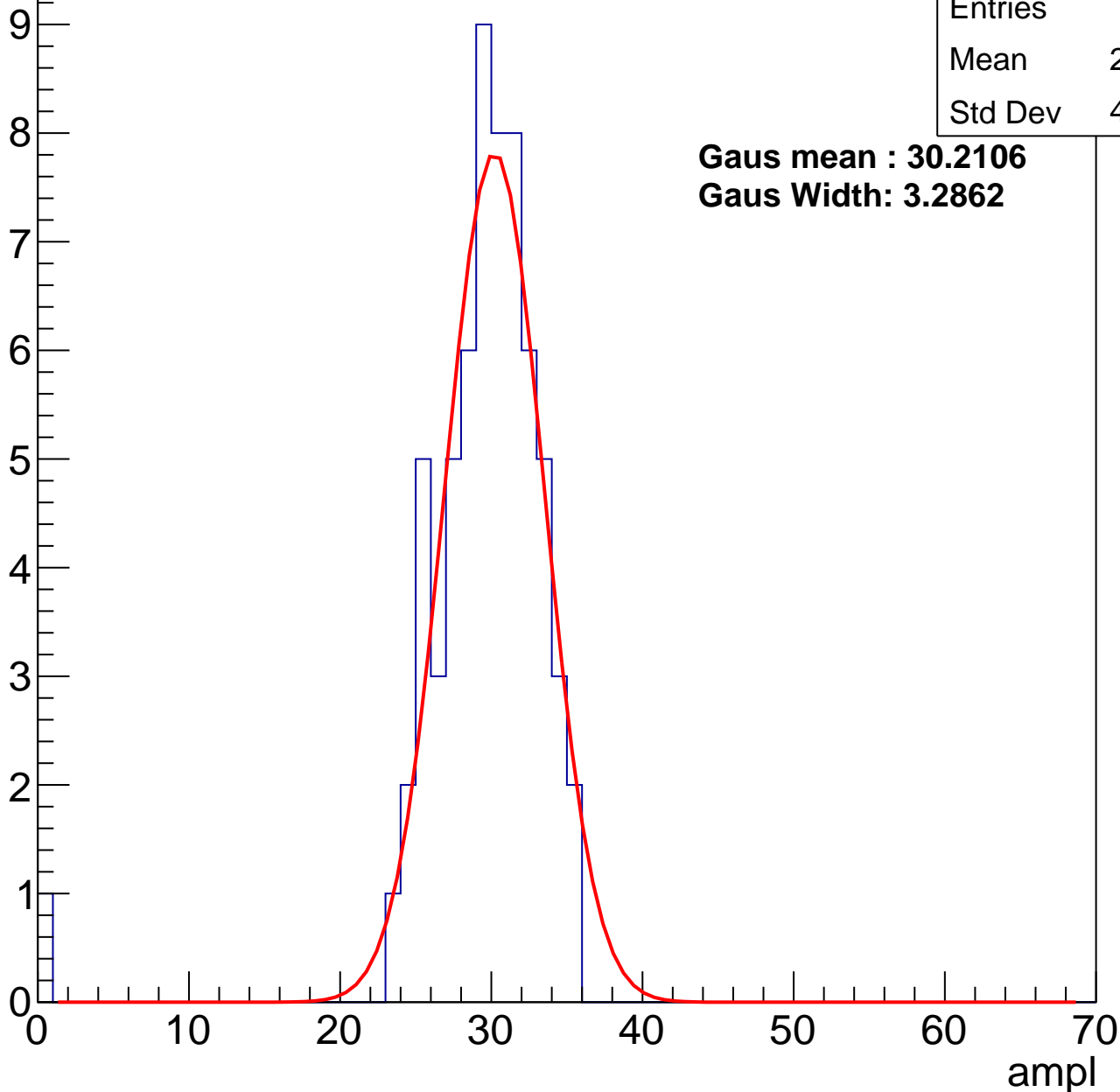
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	28.98
Std Dev	4.645

**Gaus mean : 30.2106**

**Gaus Width: 3.2862**



# B1L102S, U21-ch17, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	74
Mean	36.45
Std Dev	3.542

**Gaus mean : 37.0886**

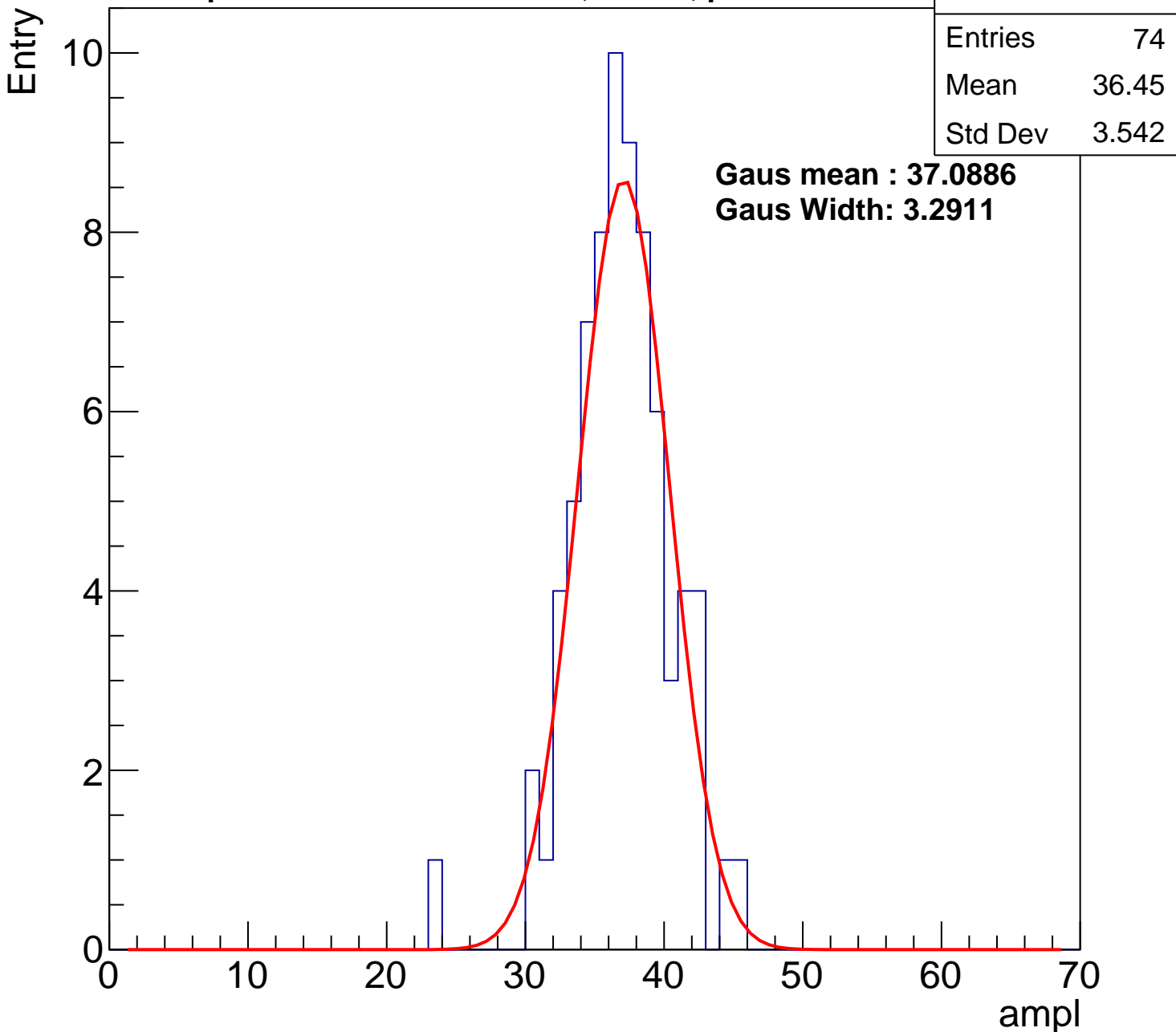
**Gaus Width: 3.2911**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U21-ch17, adc2

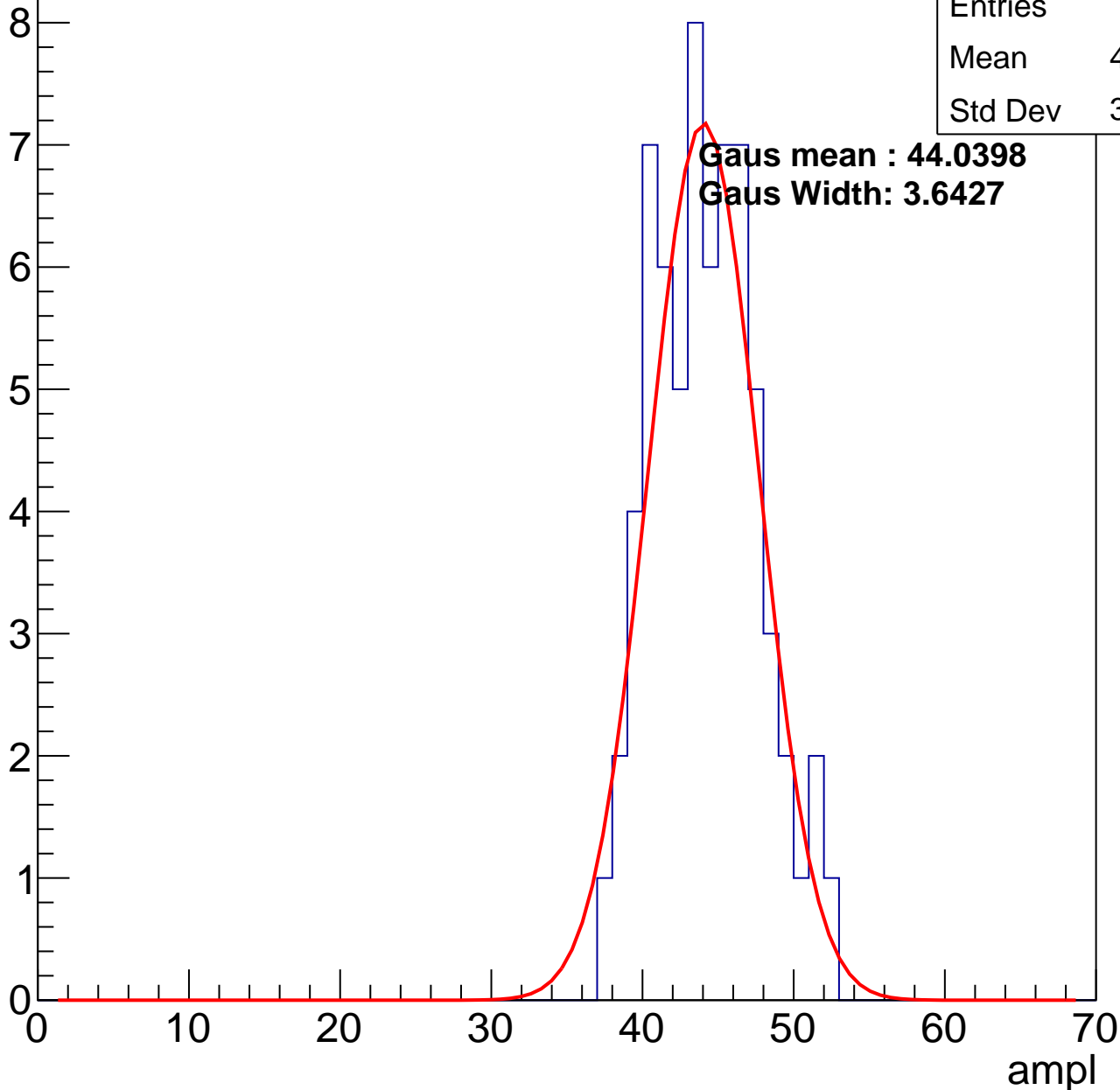
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	43.75
Std Dev	3.427

**Gaus mean : 44.0398**

**Gaus Width: 3.6427**

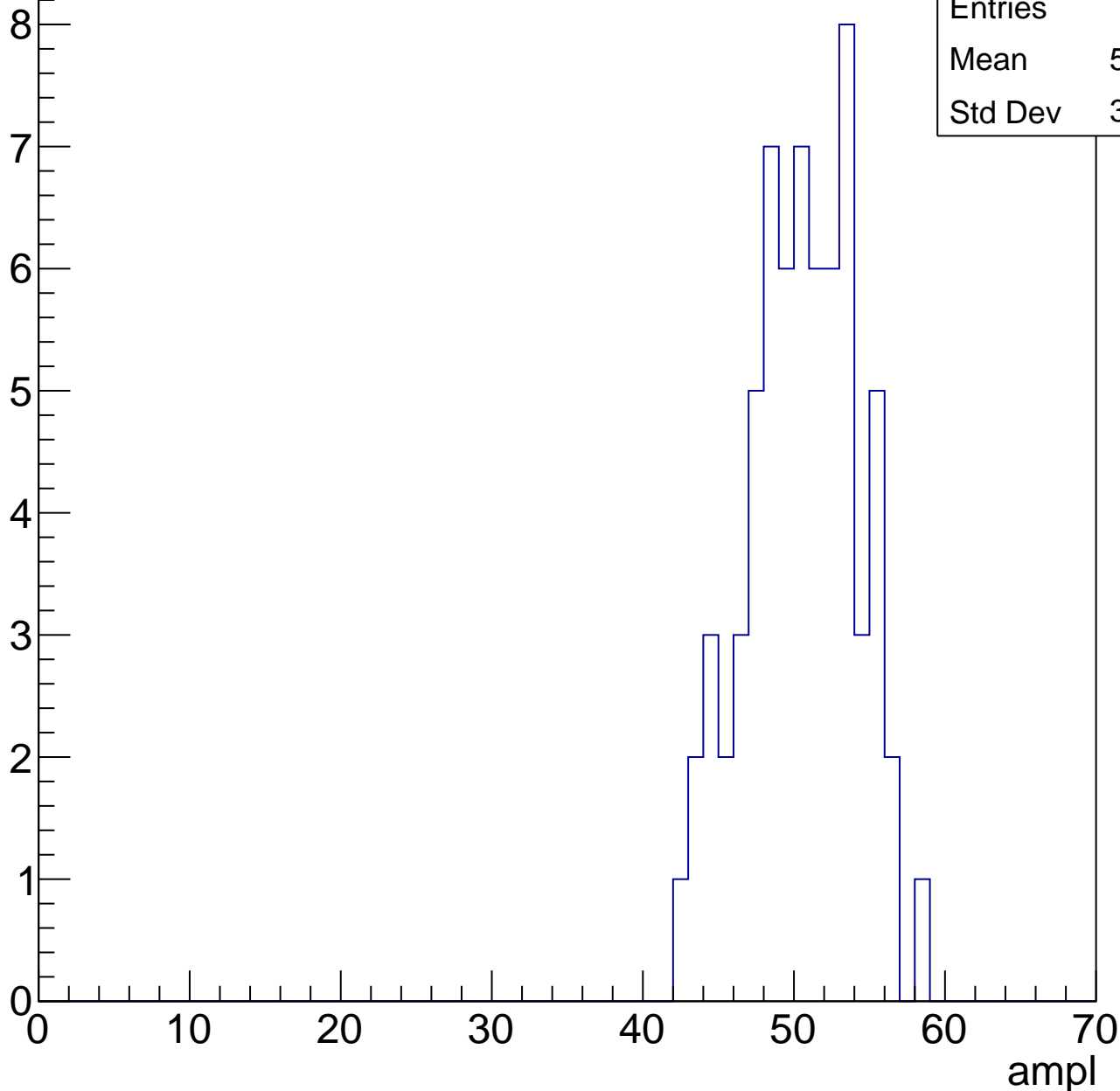


# B1L102S, U21-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	50.03
Std Dev	3.578

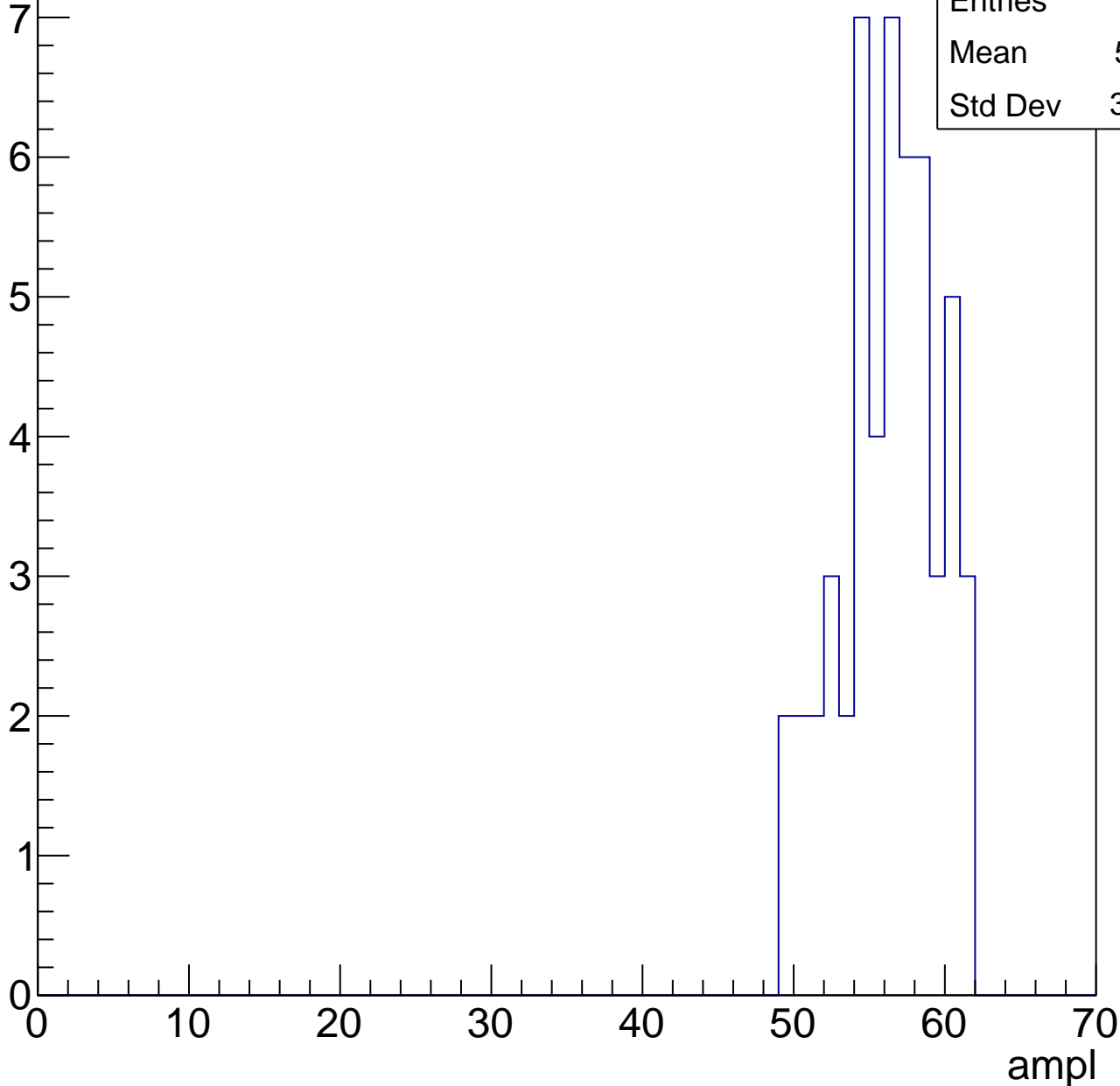


# B1L102S, U21-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	55.81
Std Dev	3.187



# B1L102S, U21-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	41
Mean	58.59
Std Dev	9.492

ampl

0 10 20 30 40 50 60 70

1

2

3

4

5

6

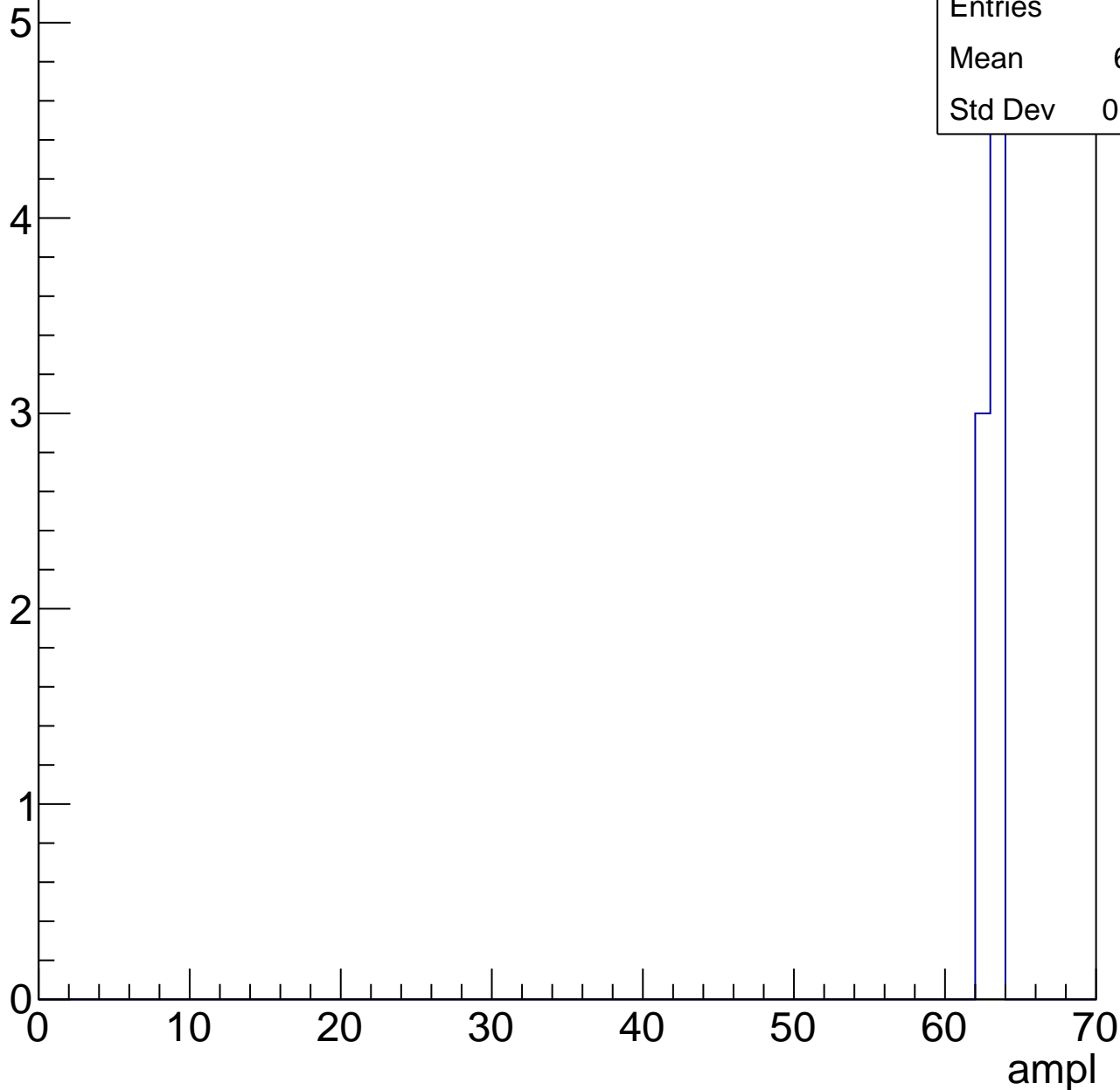
7

# B1L102S, U21-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	8
Mean	62.62
Std Dev	0.4841





# B1L102S, U21-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U21-ch18, adc0

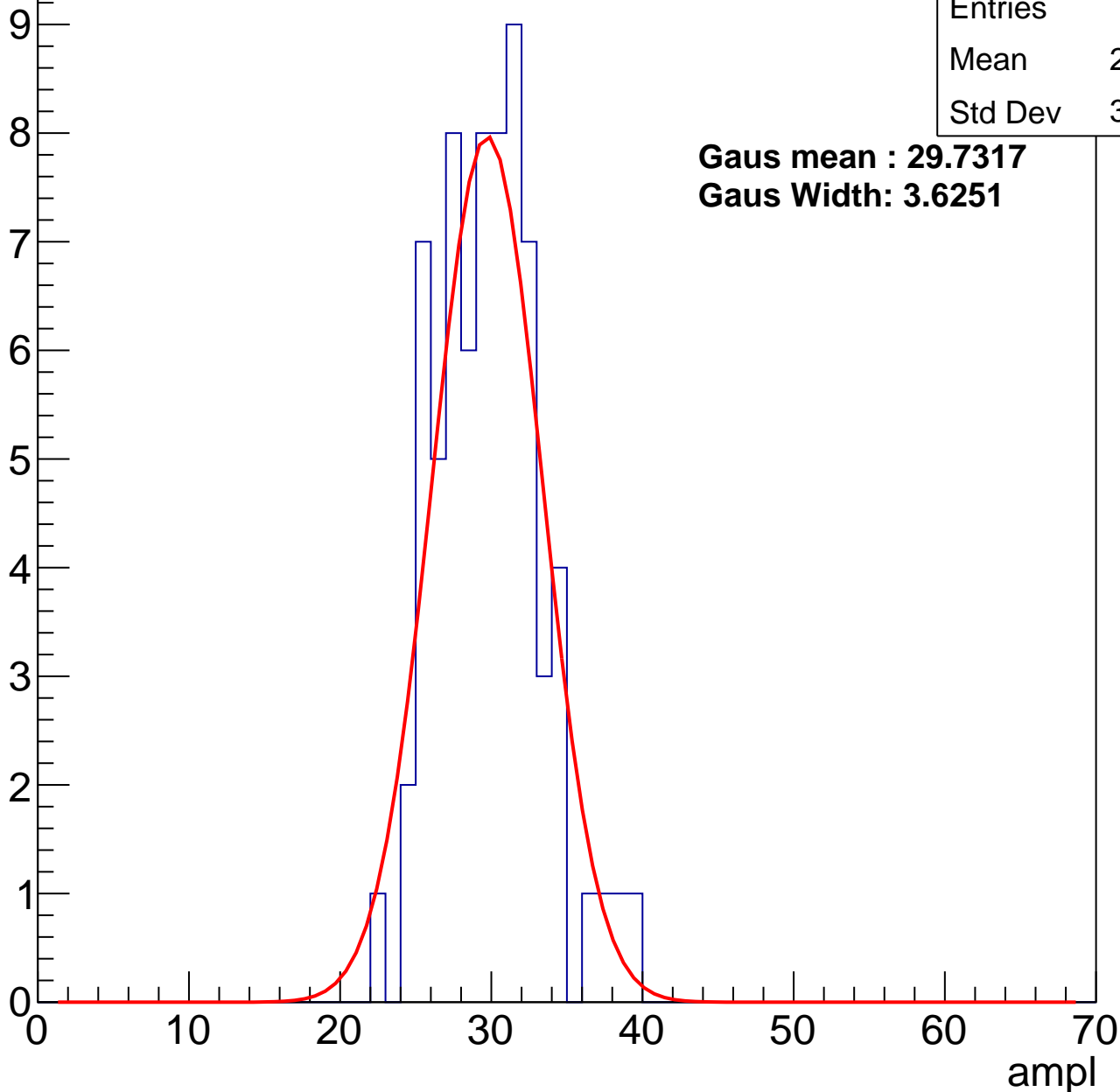
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	29.43
Std Dev	3.395

**Gaus mean : 29.7317**

**Gaus Width: 3.6251**



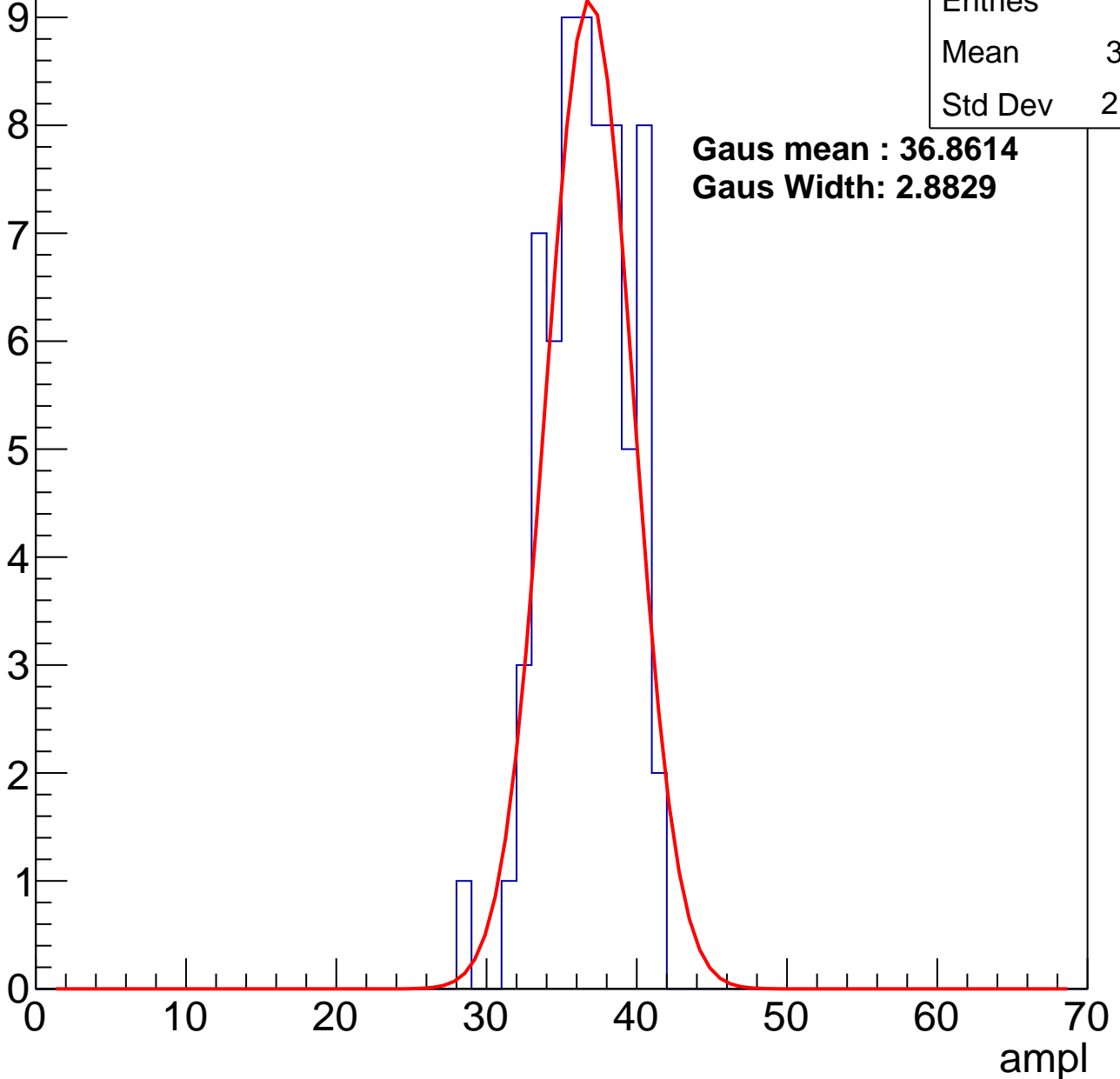
# B1L102S, U21-ch18, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	36.21
Std Dev	2.713

**Gaus mean : 36.8614**  
**Gaus Width: 2.8829**



# B1L102S, U21-ch18, adc2

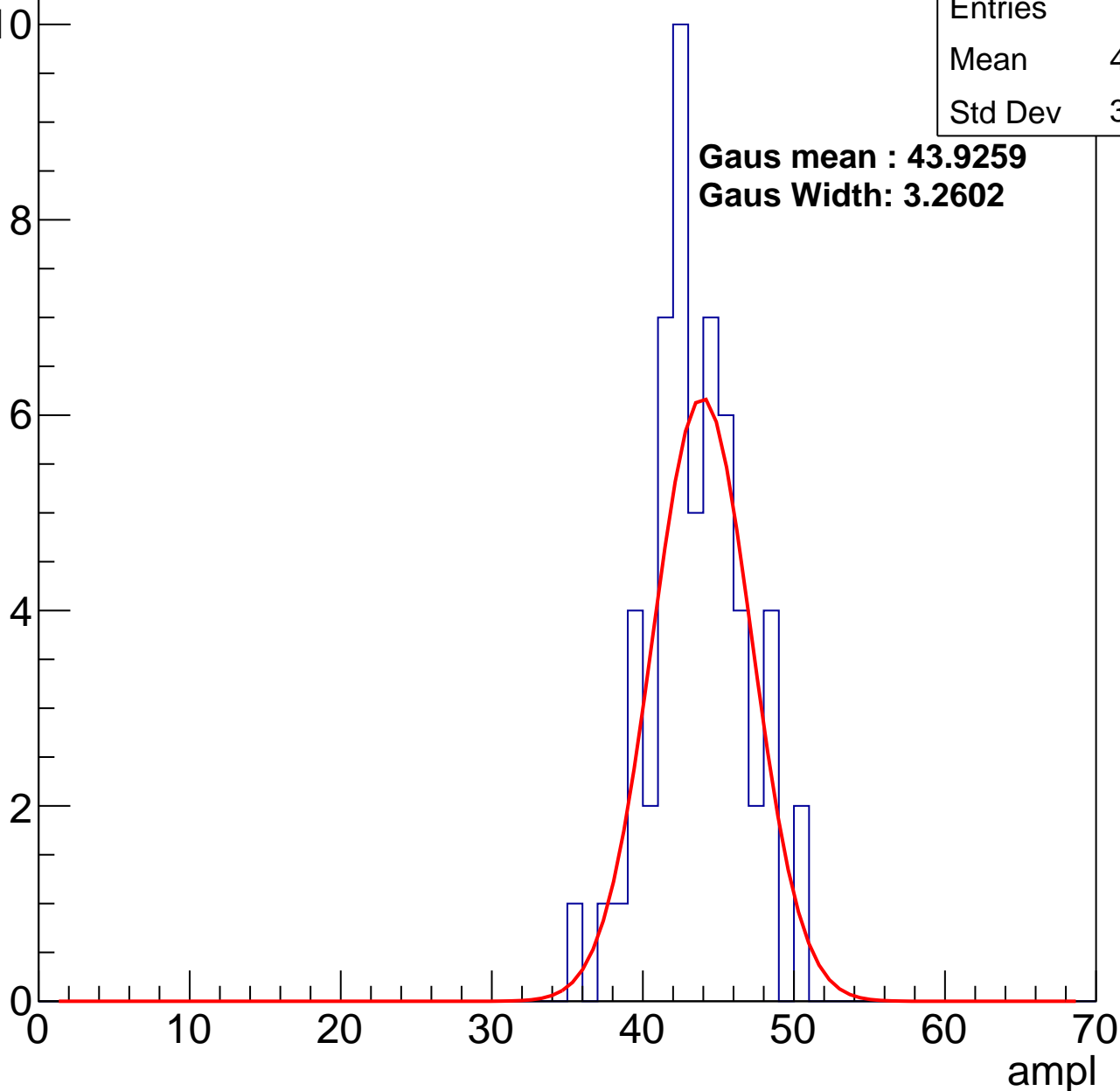
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	43.14
Std Dev	3.108

**Gaus mean : 43.9259**

**Gaus Width: 3.2602**

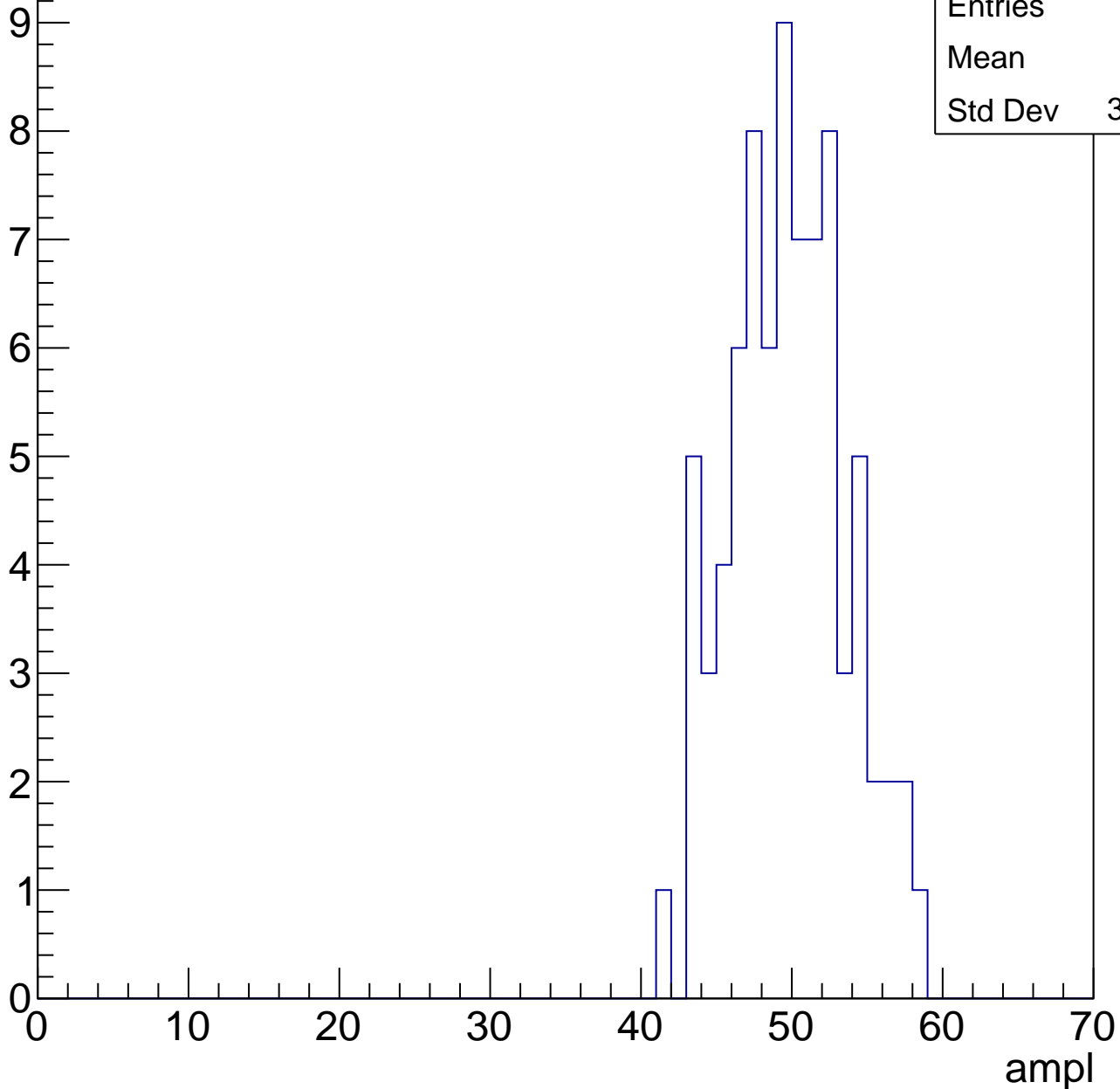


# B1L102S, U21-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

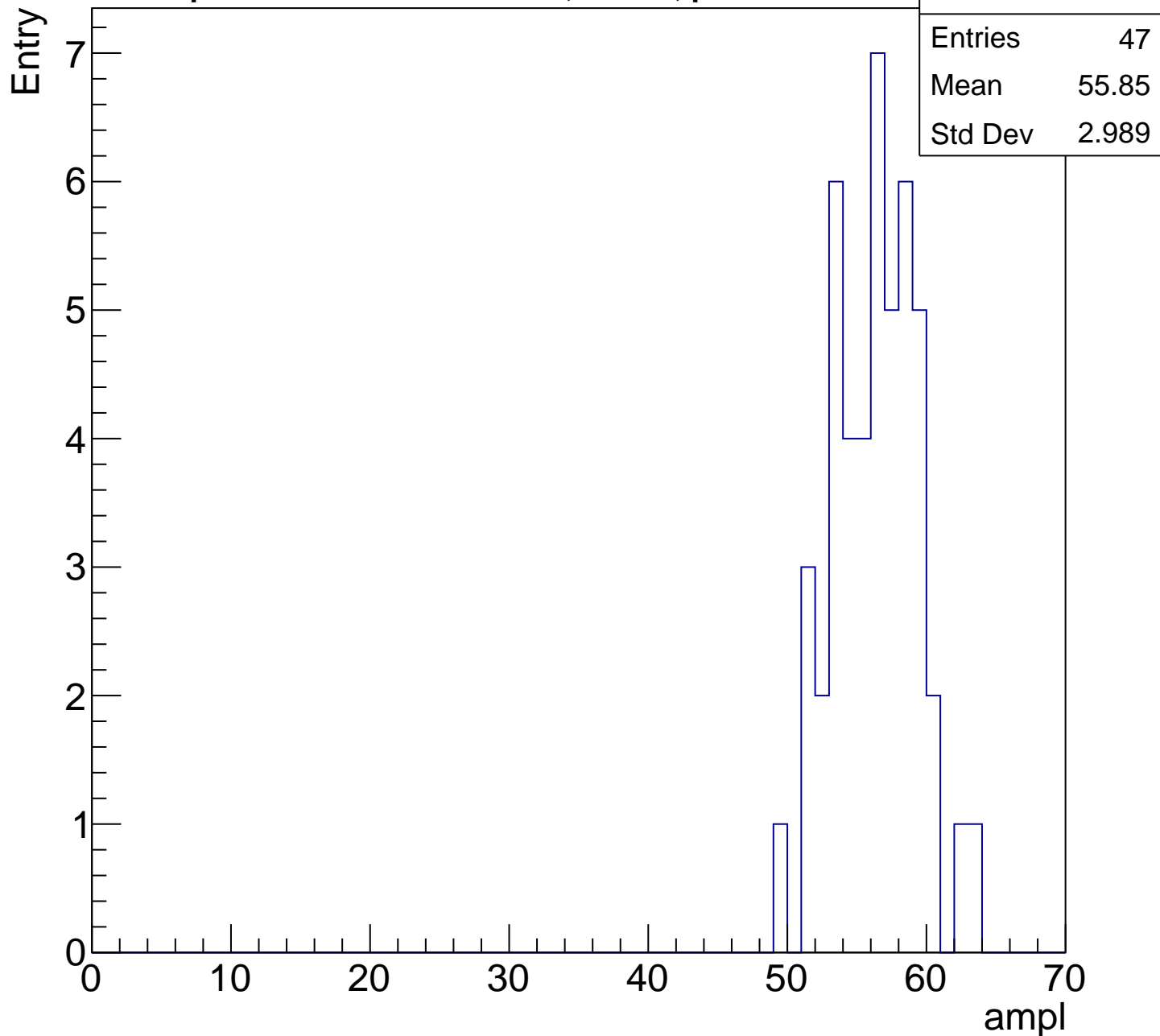
Entry

Entries	79
Mean	49.3
Std Dev	3.777



# B1L102S, U21-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

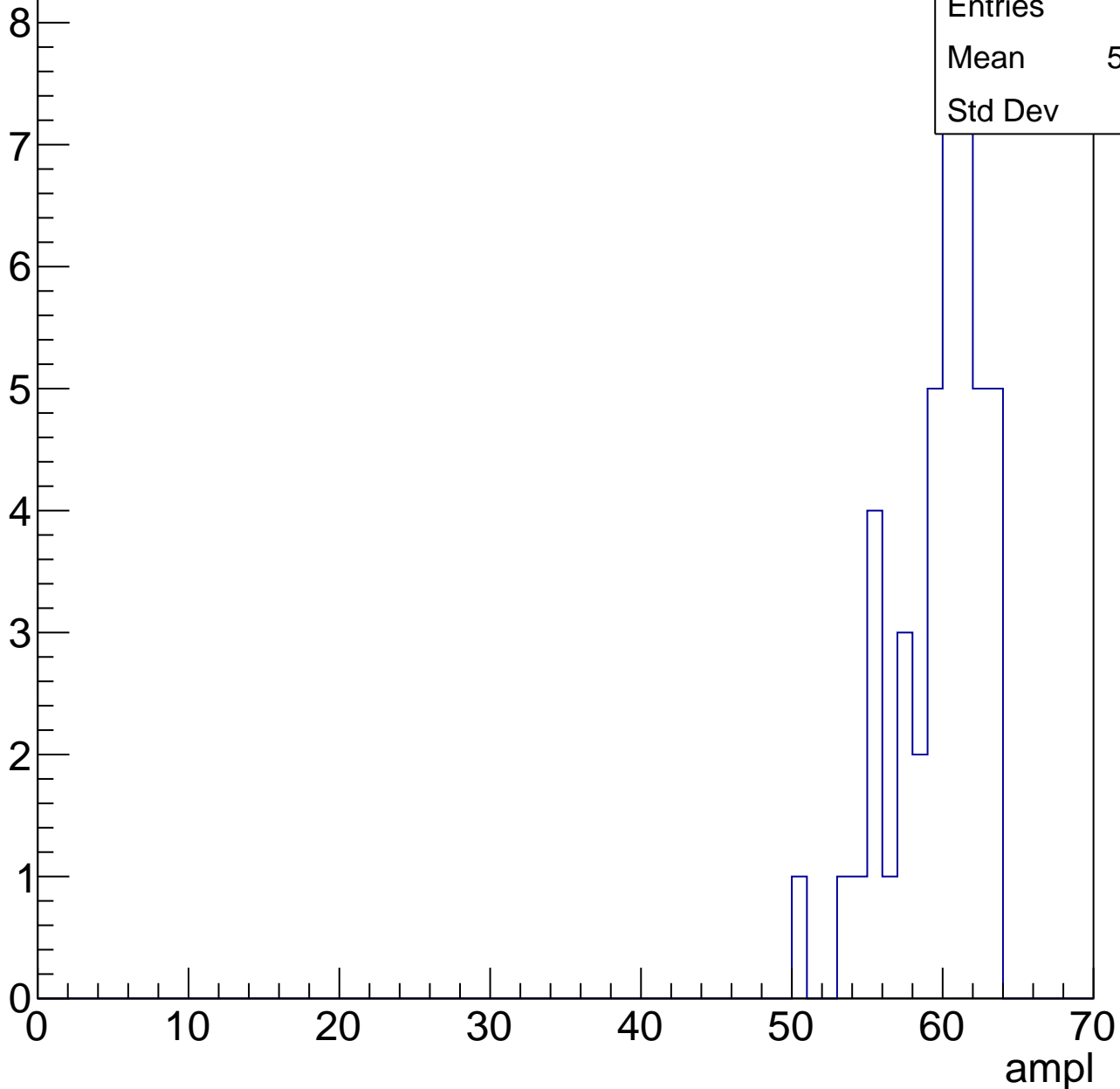


# B1L102S, U21-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

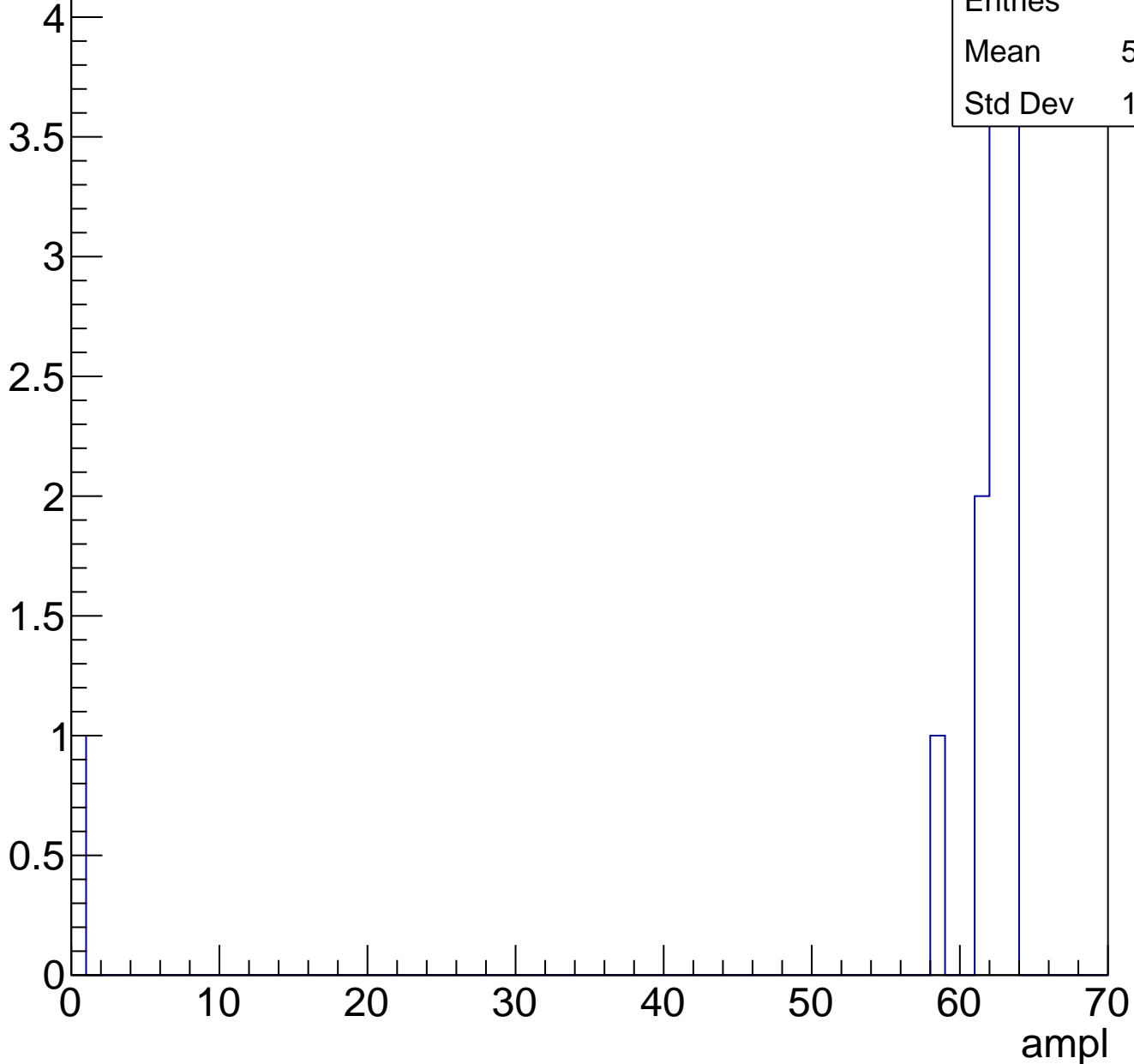
Entries	44
Mean	59.27
Std Dev	2.98



# B1L102S, U21-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch19, adc0

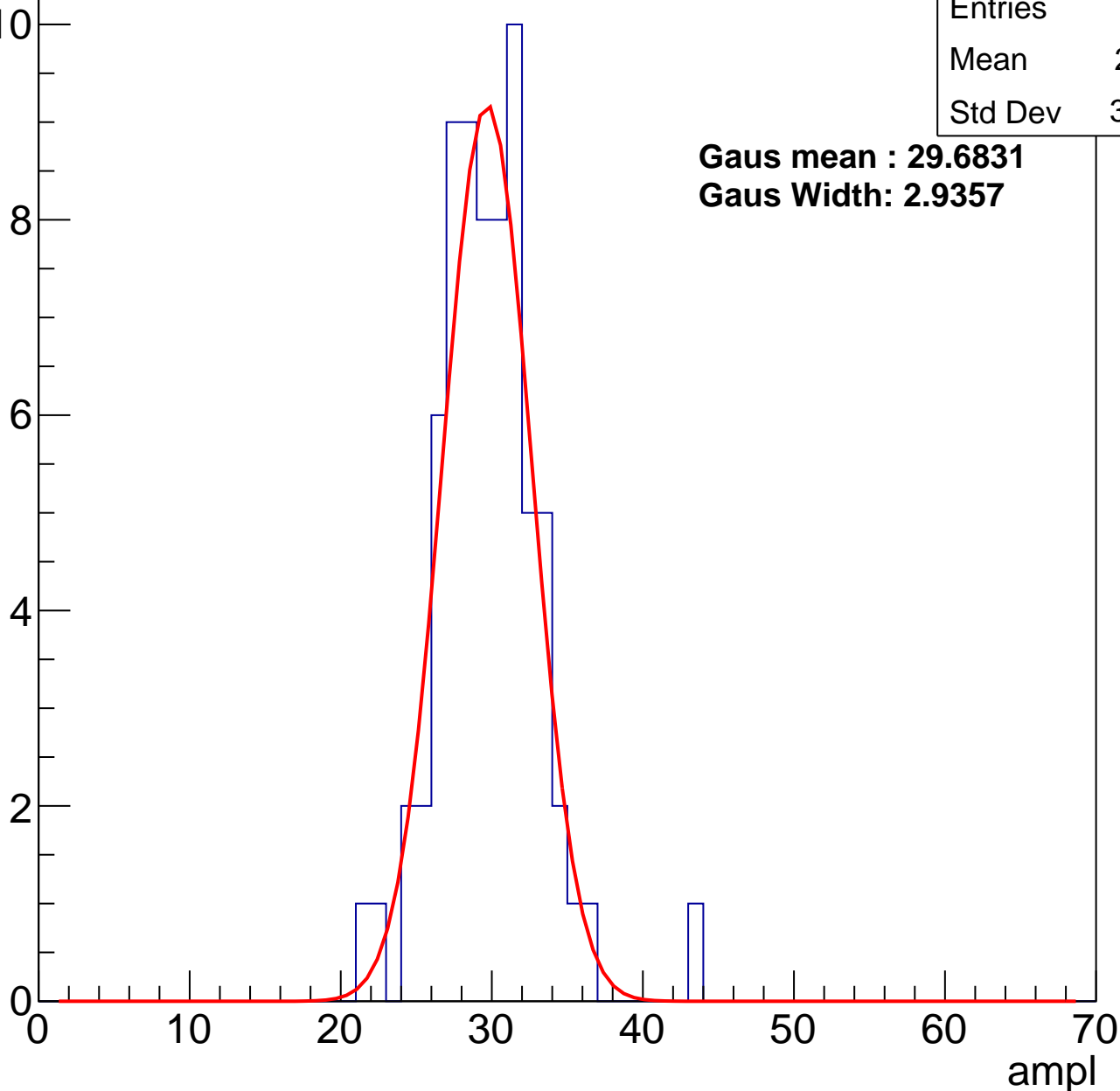
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	29.31
Std Dev	3.338

**Gaus mean : 29.6831**

**Gaus Width: 2.9357**



# B1L102S, U21-ch19, adc1

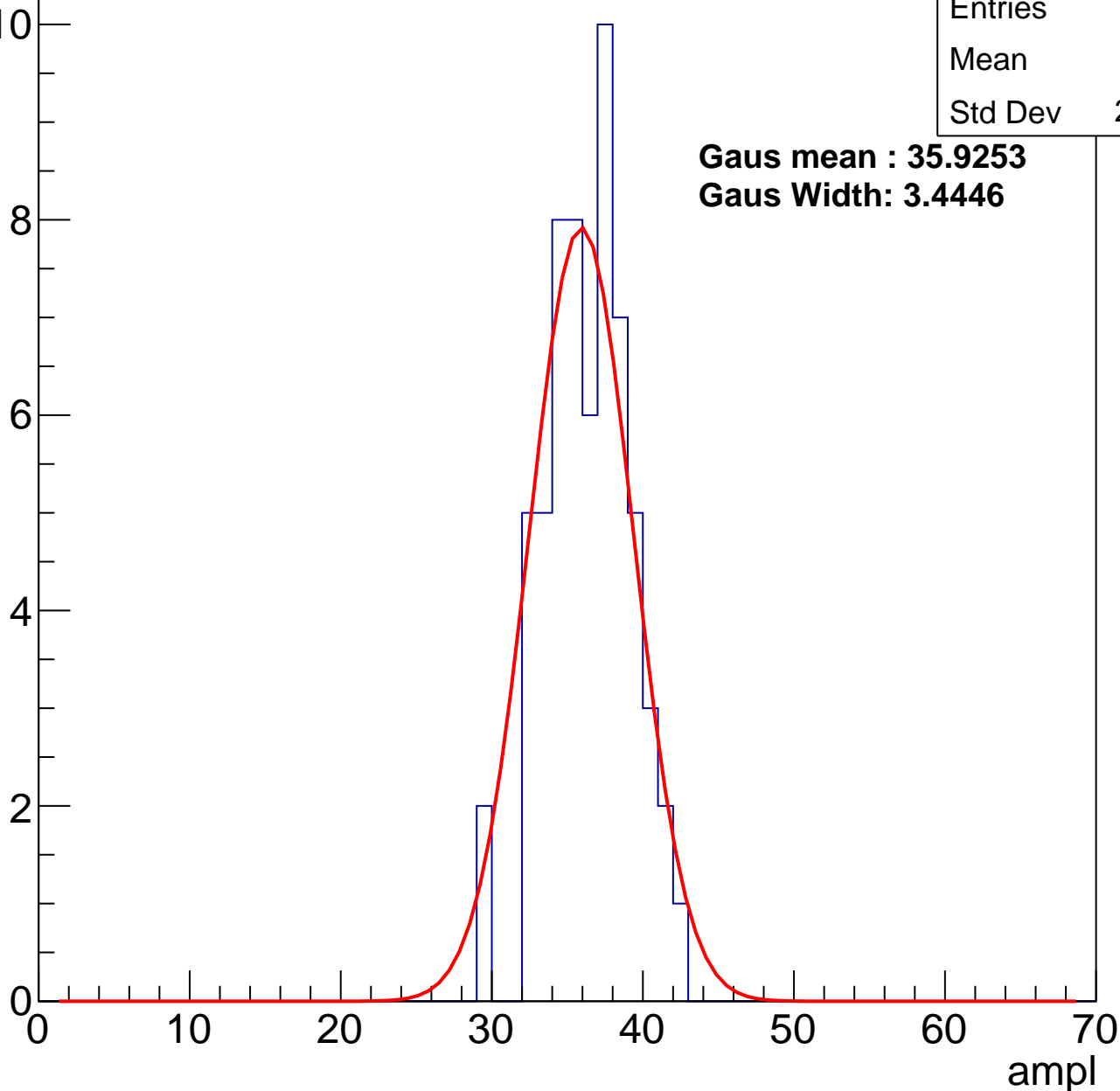
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	35.9
Std Dev	2.781

**Gaus mean : 35.9253**

**Gaus Width: 3.4446**



# B1L102S, U21-ch19, adc2

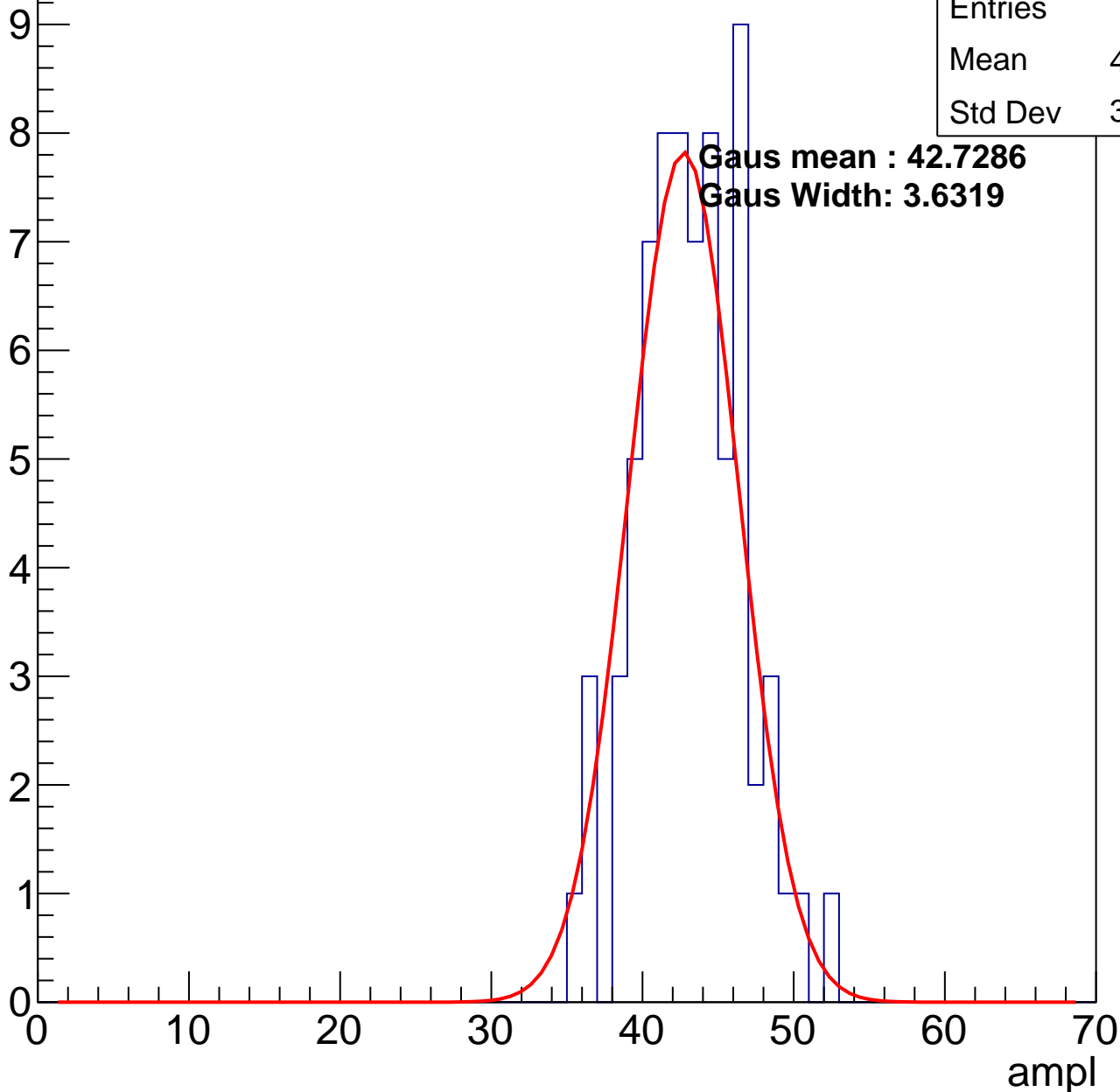
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	42.74
Std Dev	3.428

**Gaus mean : 42.7286**

**Gaus Width: 3.6319**

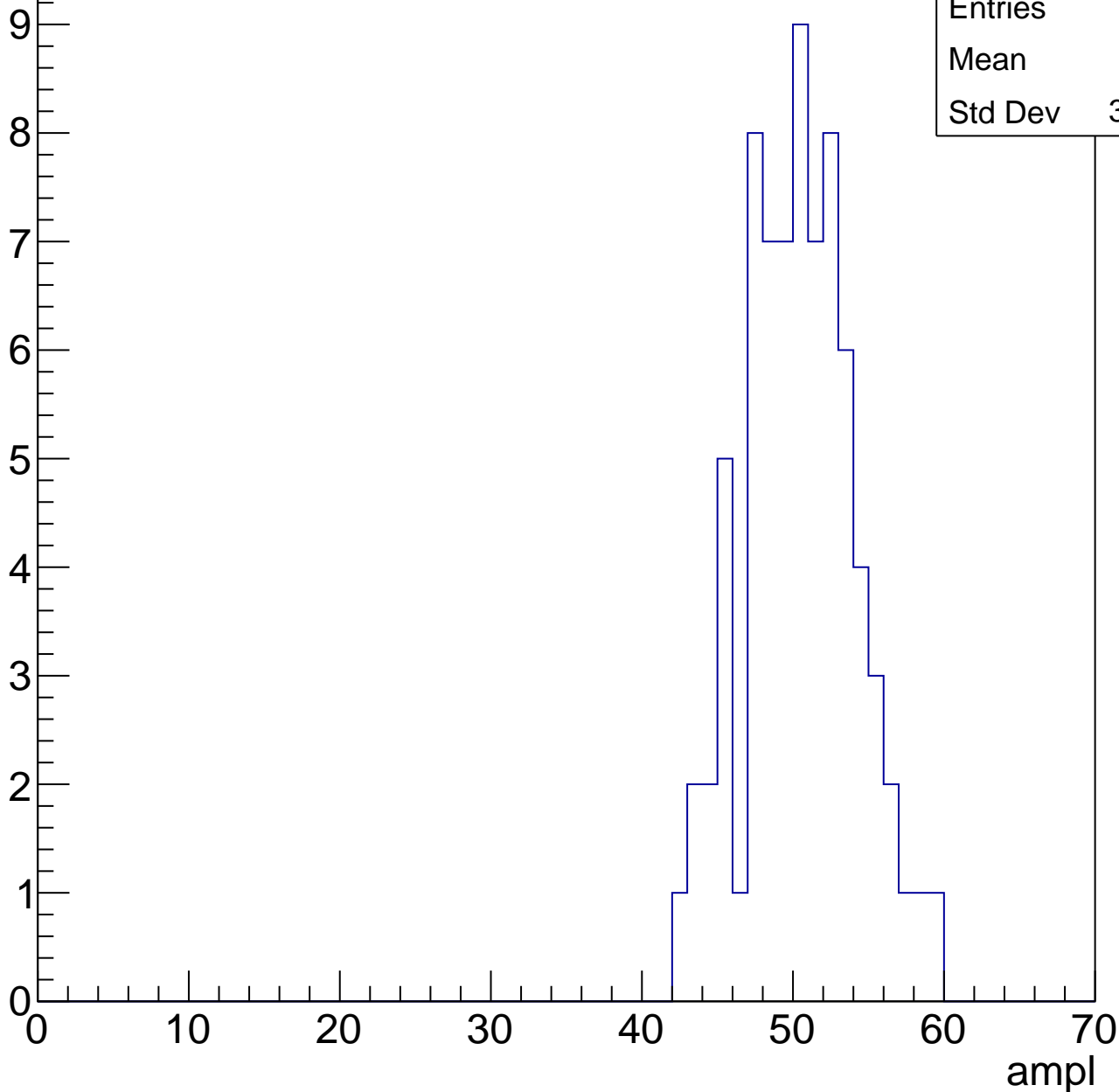


# B1L102S, U21-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	50
Std Dev	3.615

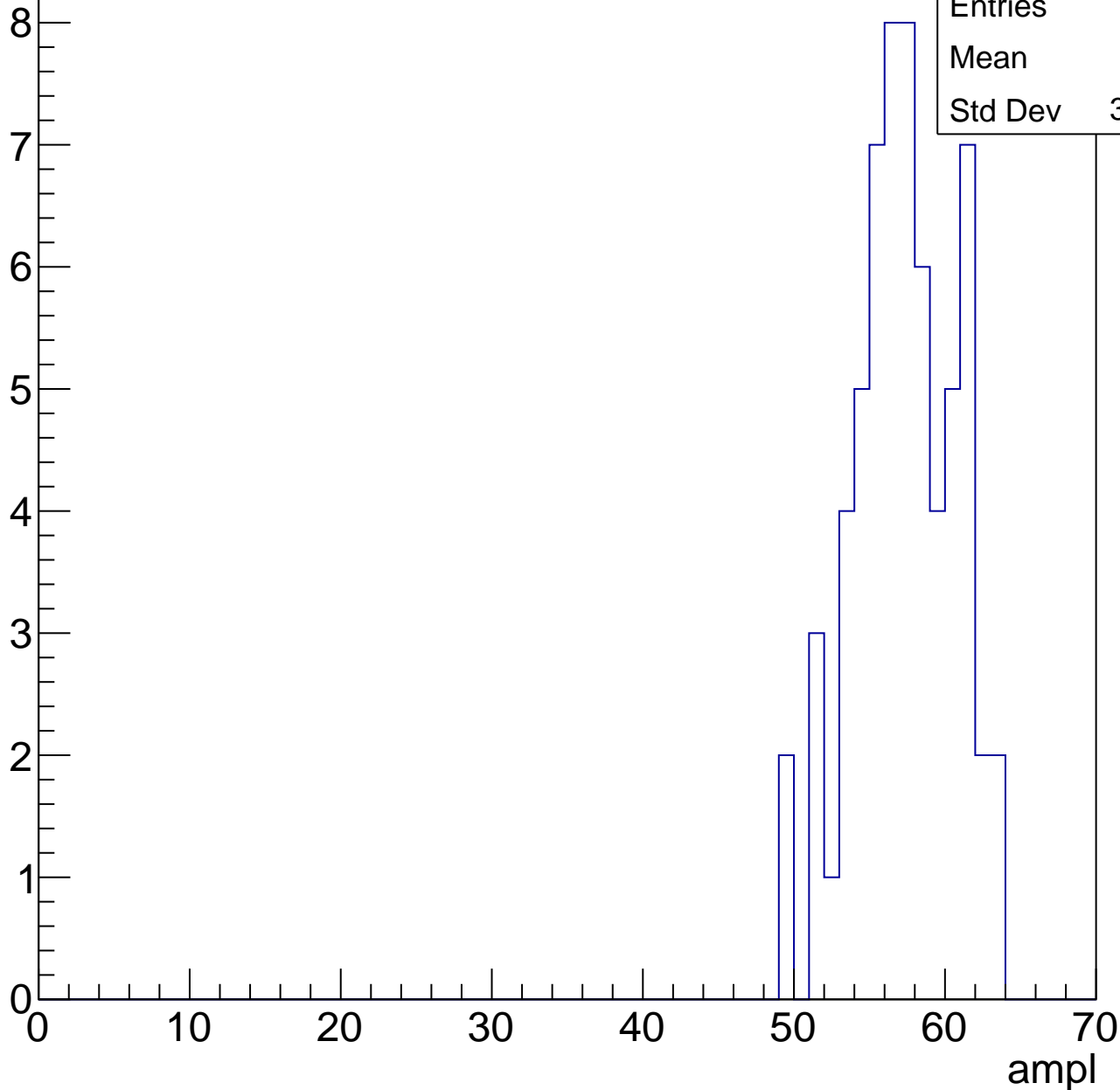


# B1L102S, U21-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	56.8
Std Dev	3.317

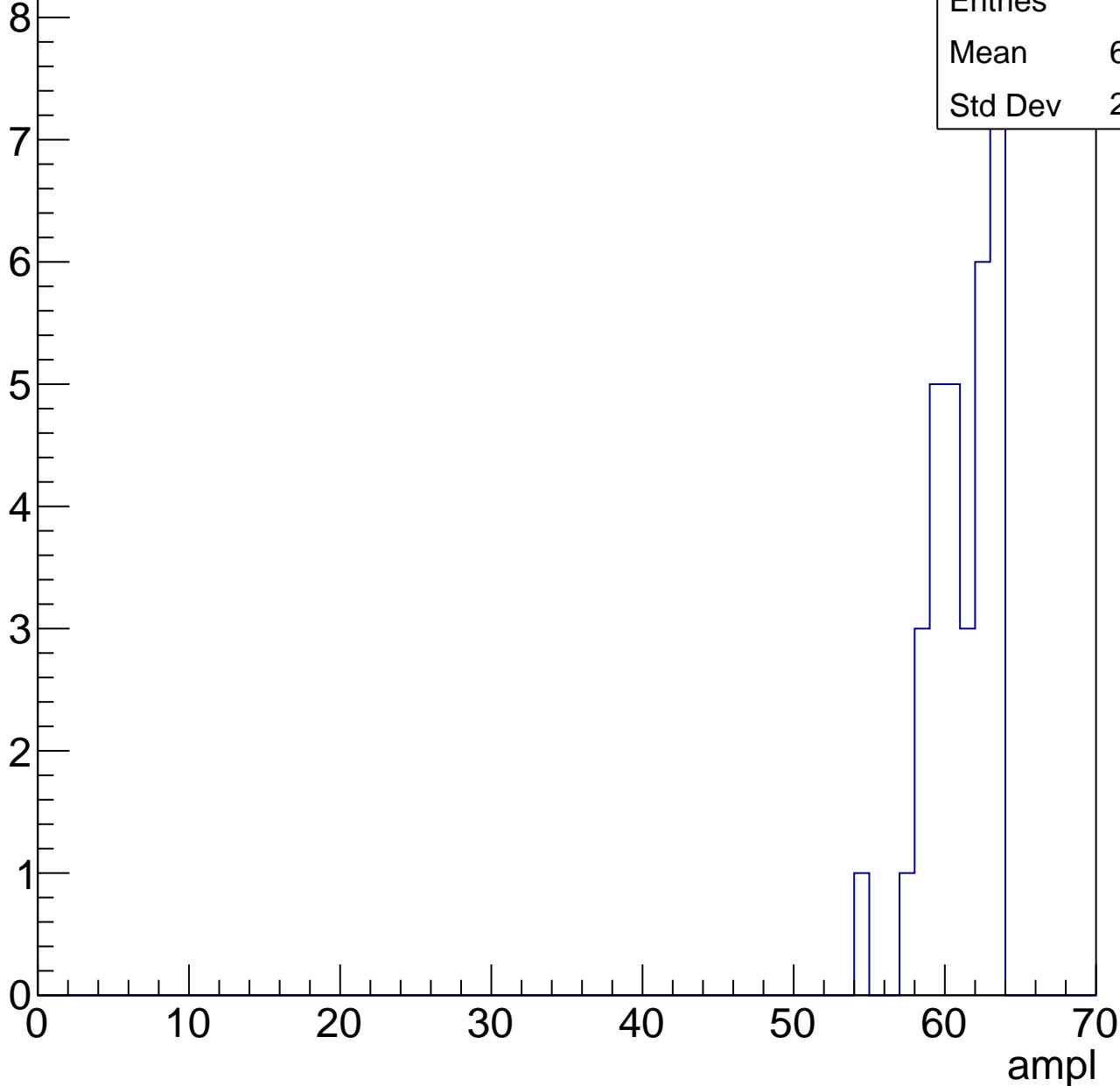


# B1L102S, U21-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

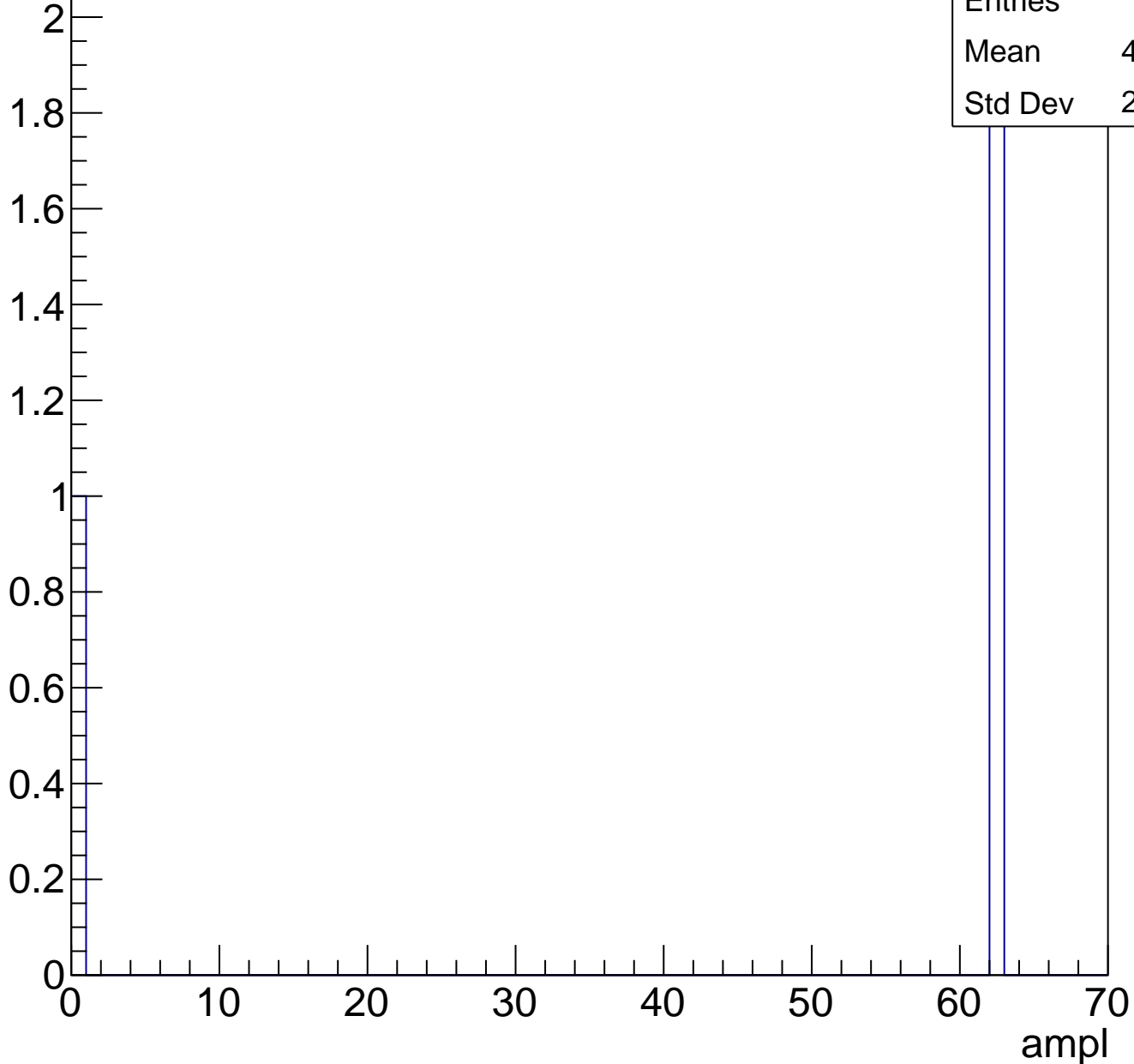
Entries	32
Mean	60.59
Std Dev	2.163



# B1L102S, U21-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch20, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	76
Mean	31.22
Std Dev	3.417

**Gaus mean : 32.2620**

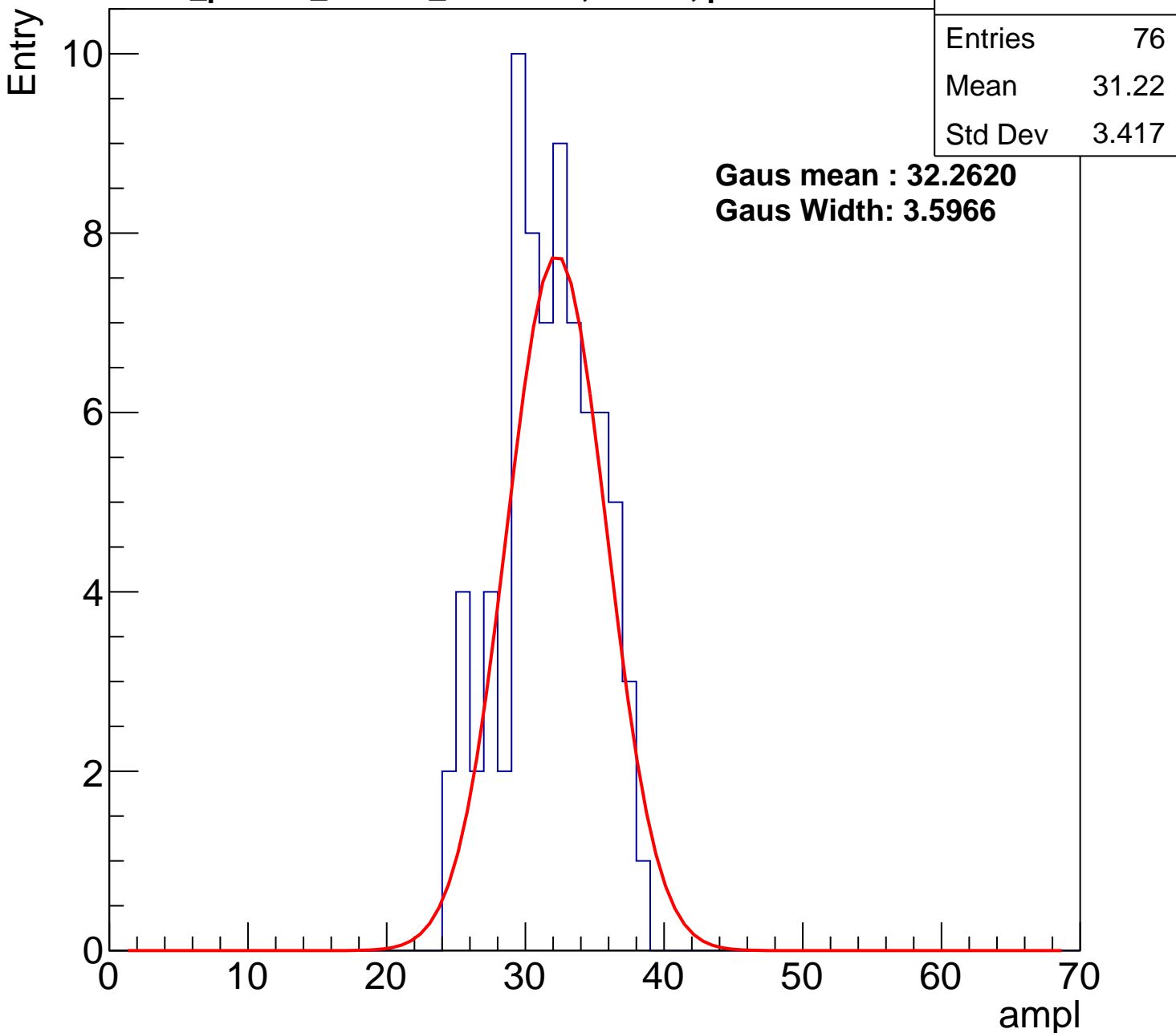
**Gaus Width: 3.5966**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U21-ch20, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	38.22
Std Dev	3.184

7

6

5

4

3

2

1

0

**Gaus mean : 39.0083**

**Gaus Width: 3.7439**

0

1

2

3

4

5

6

7

8

9

10

11

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# B1L102S, U21-ch20, adc2

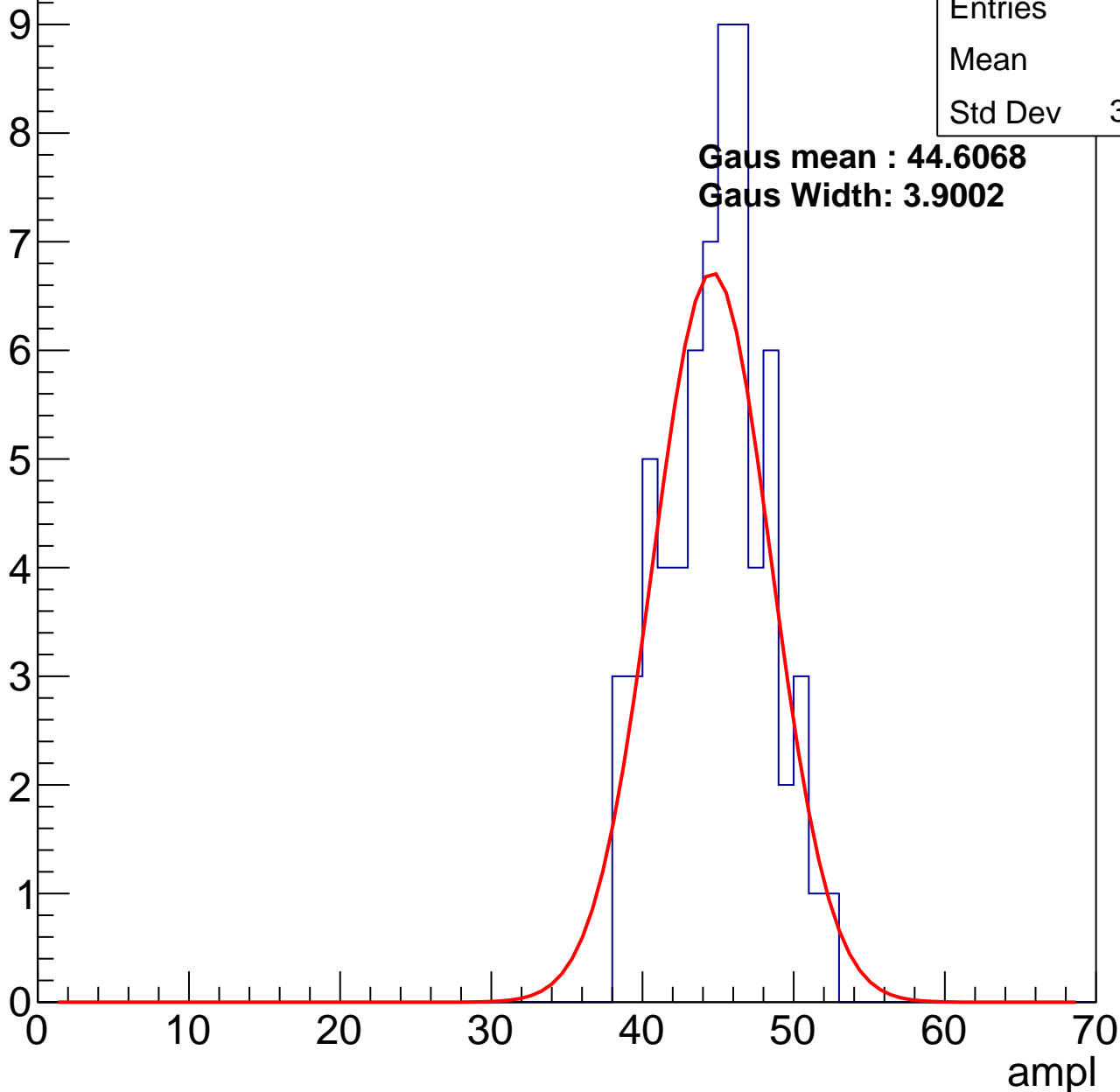
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	44.4
Std Dev	3.364

**Gaus mean : 44.6068**

**Gaus Width: 3.9002**

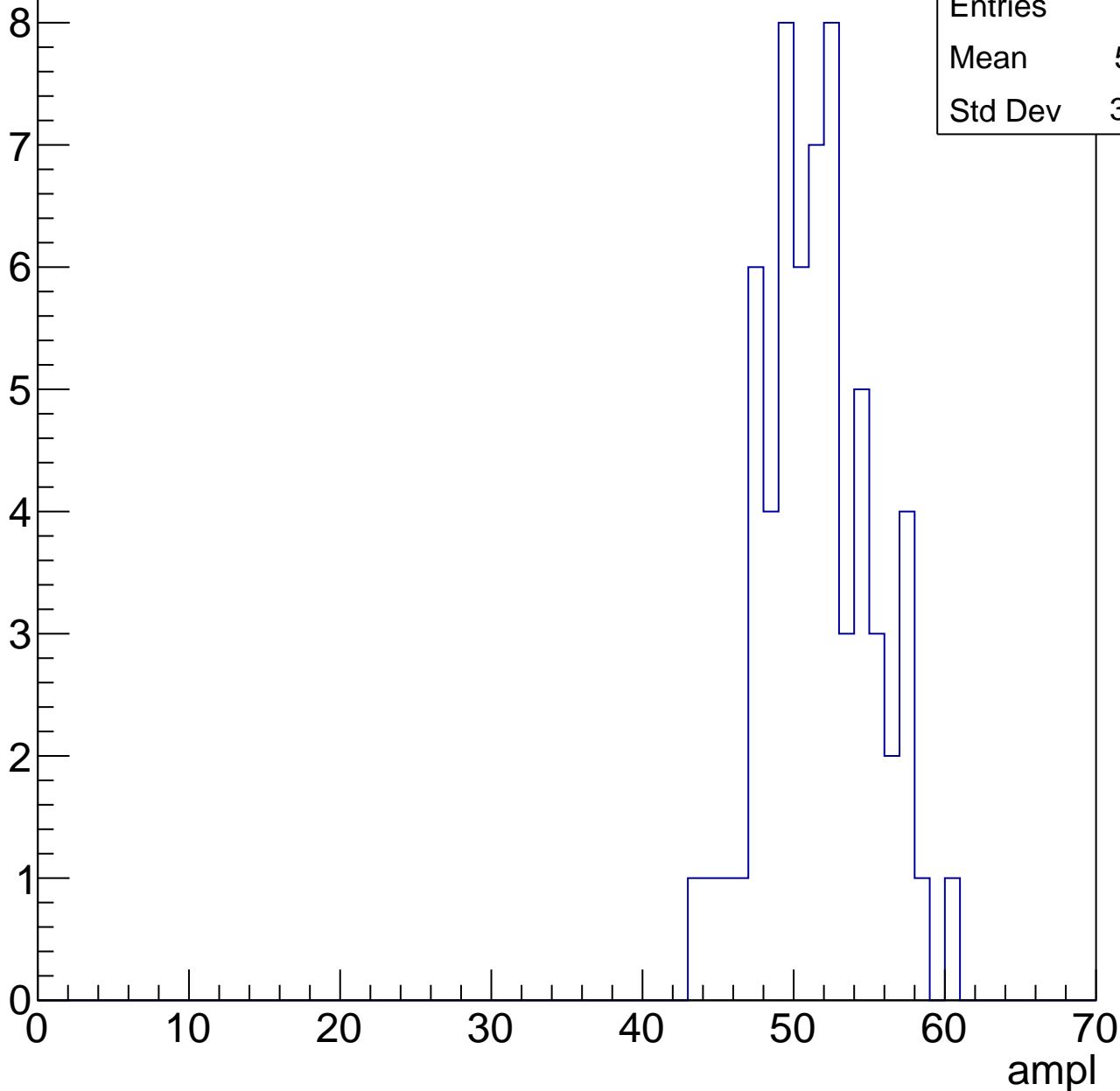


# B1L102S, U21-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	51.11
Std Dev	3.547

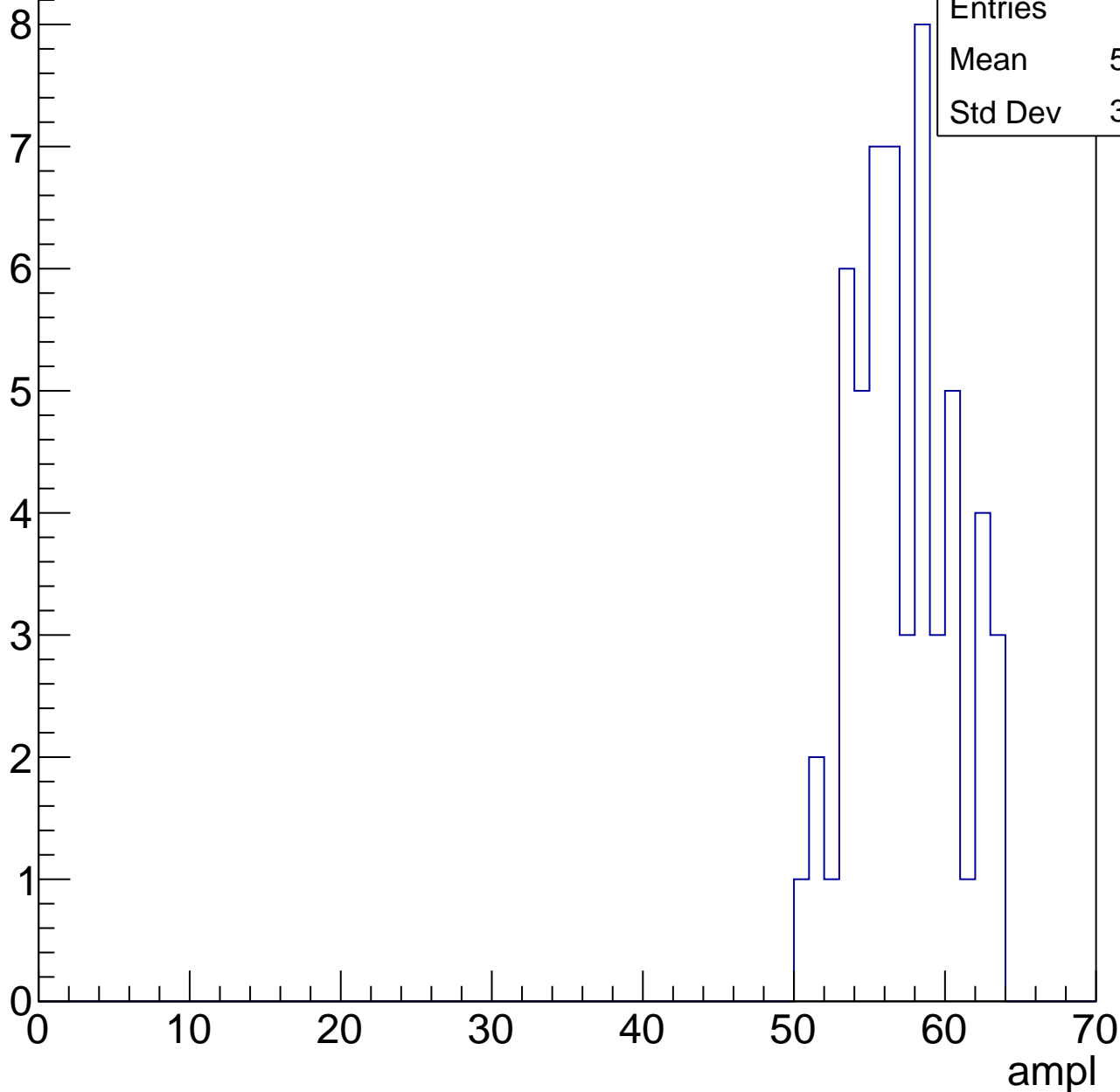


# B1L102S, U21-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	56.77
Std Dev	3.295

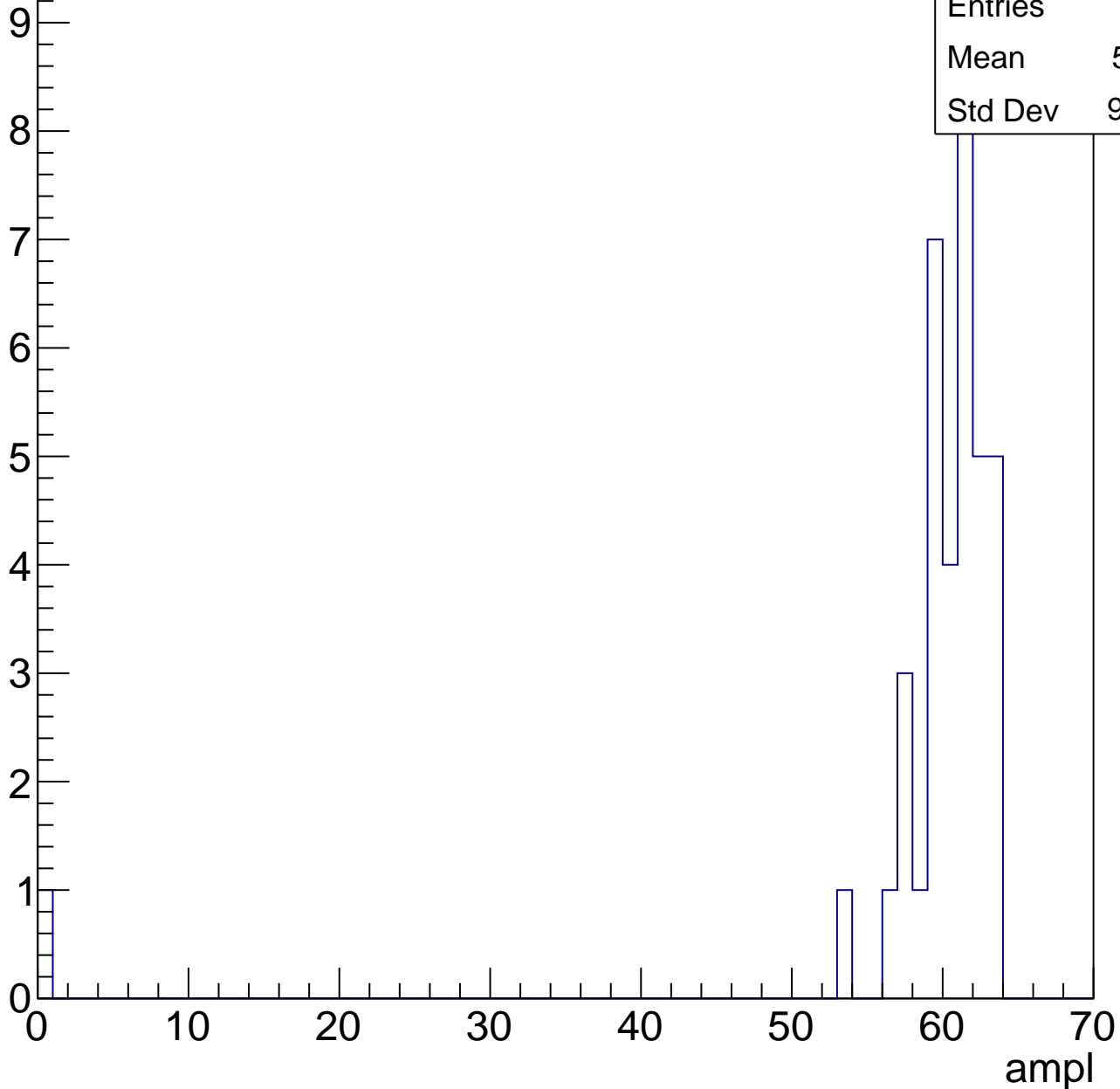


# B1L102S, U21-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

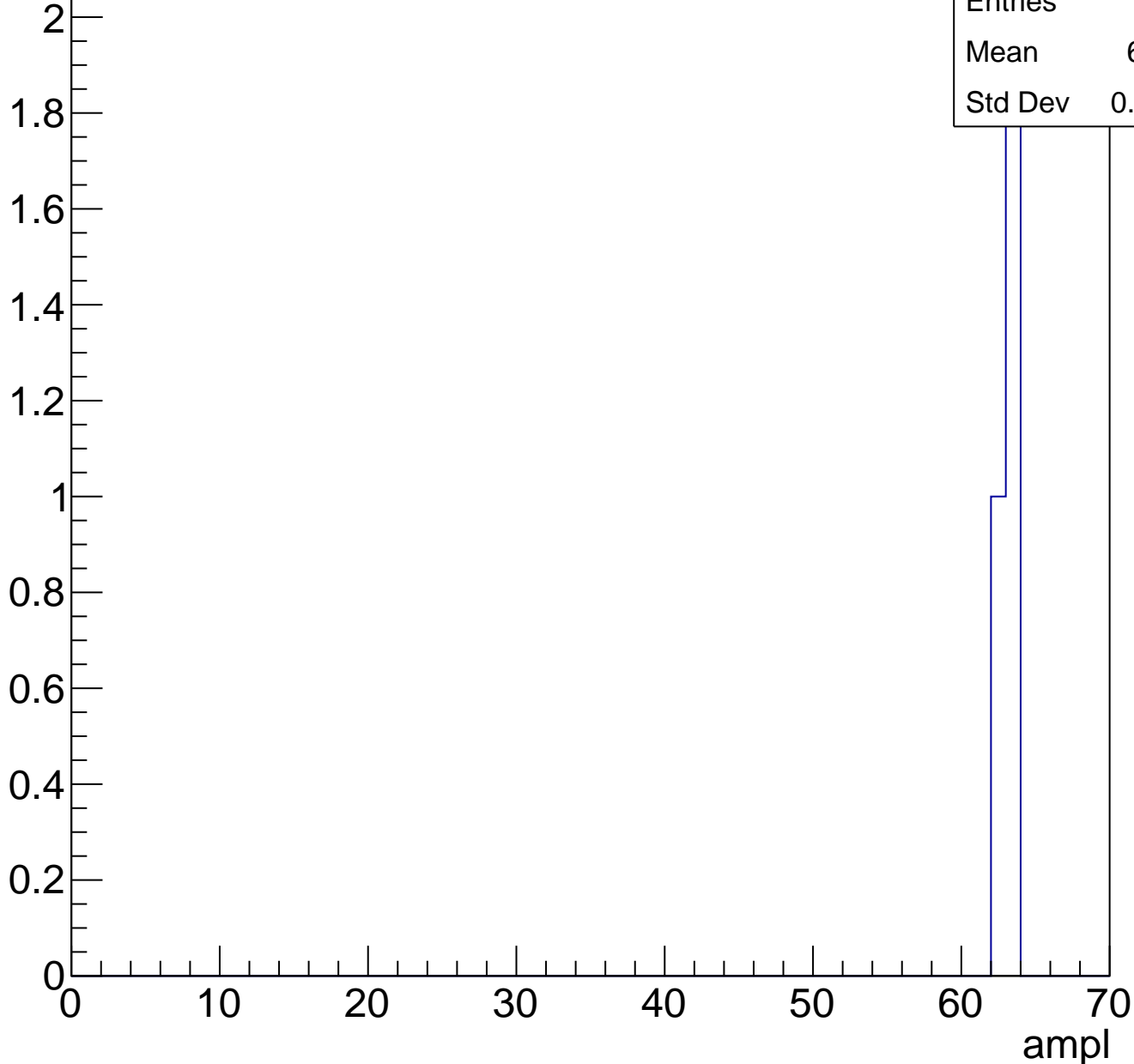
Entries	37
Mean	58.51
Std Dev	9.994



# B1L102S, U21-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U21-ch21, adc0

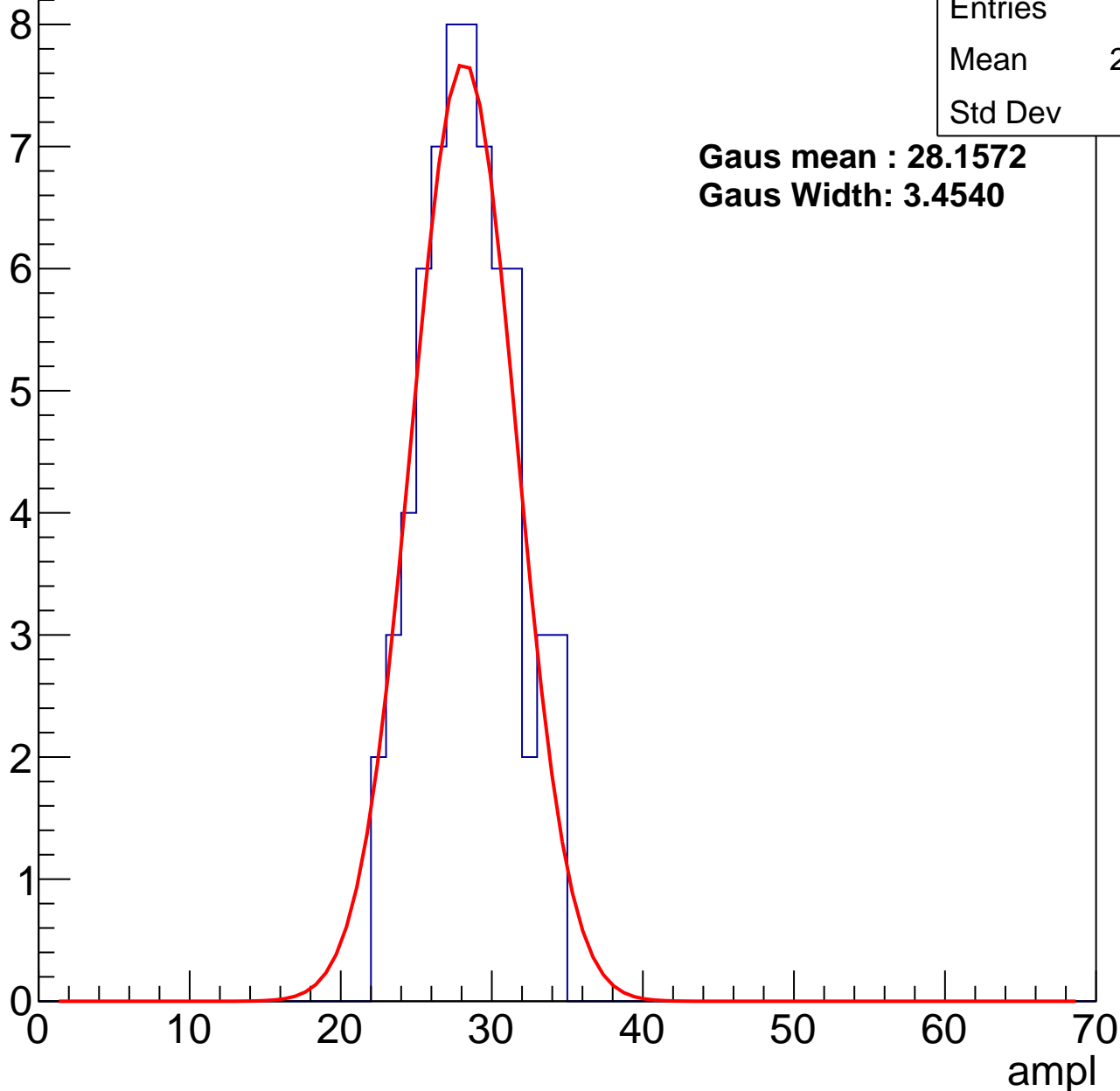
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	27.92
Std Dev	3.04

**Gaus mean : 28.1572**

**Gaus Width: 3.4540**



# B1L102S, U21-ch21, adc1

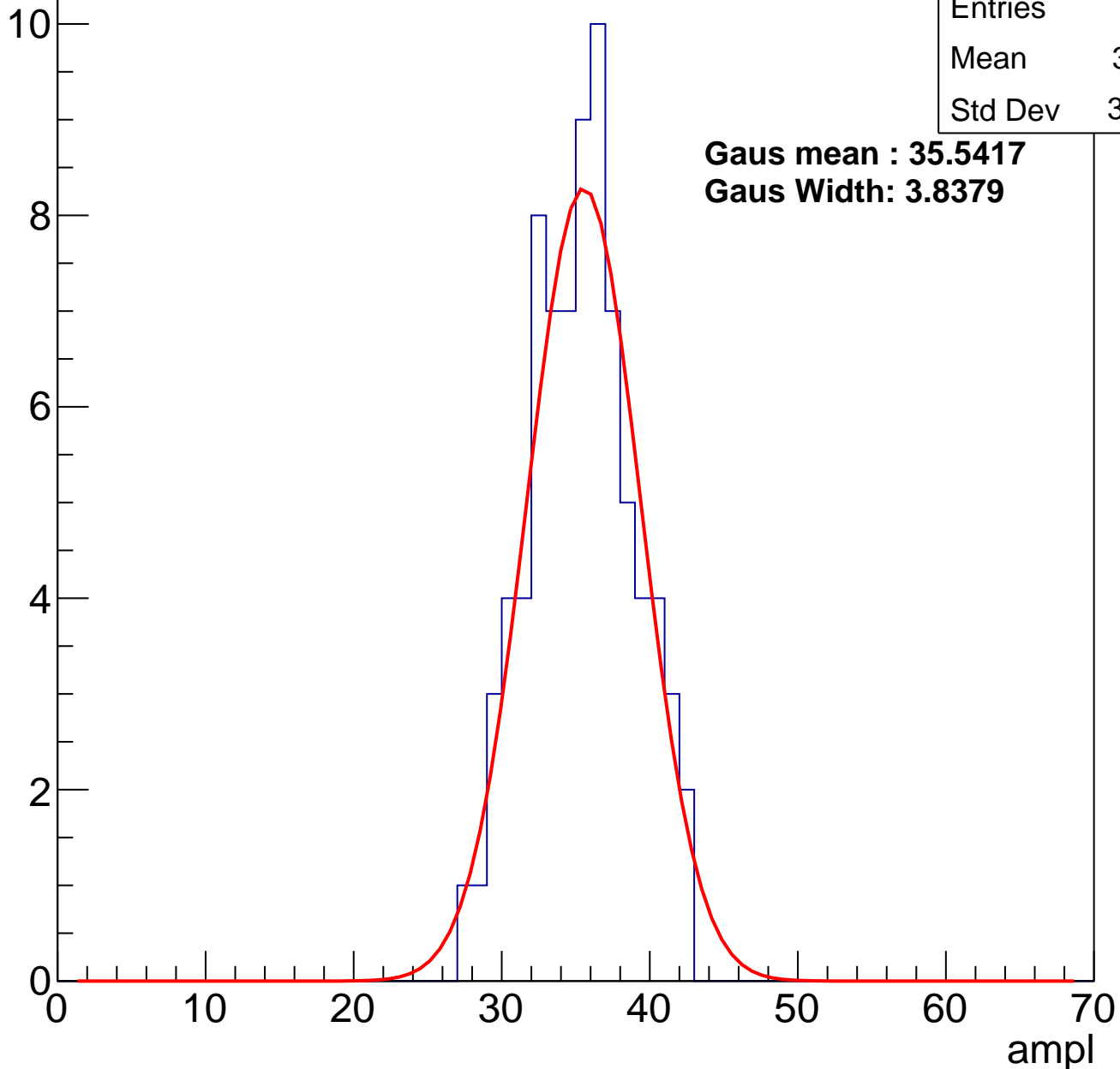
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	79
Mean	34.91
Std Dev	3.457

**Gaus mean : 35.5417**

**Gaus Width: 3.8379**

Entry



# B1L102S, U21-ch21, adc2

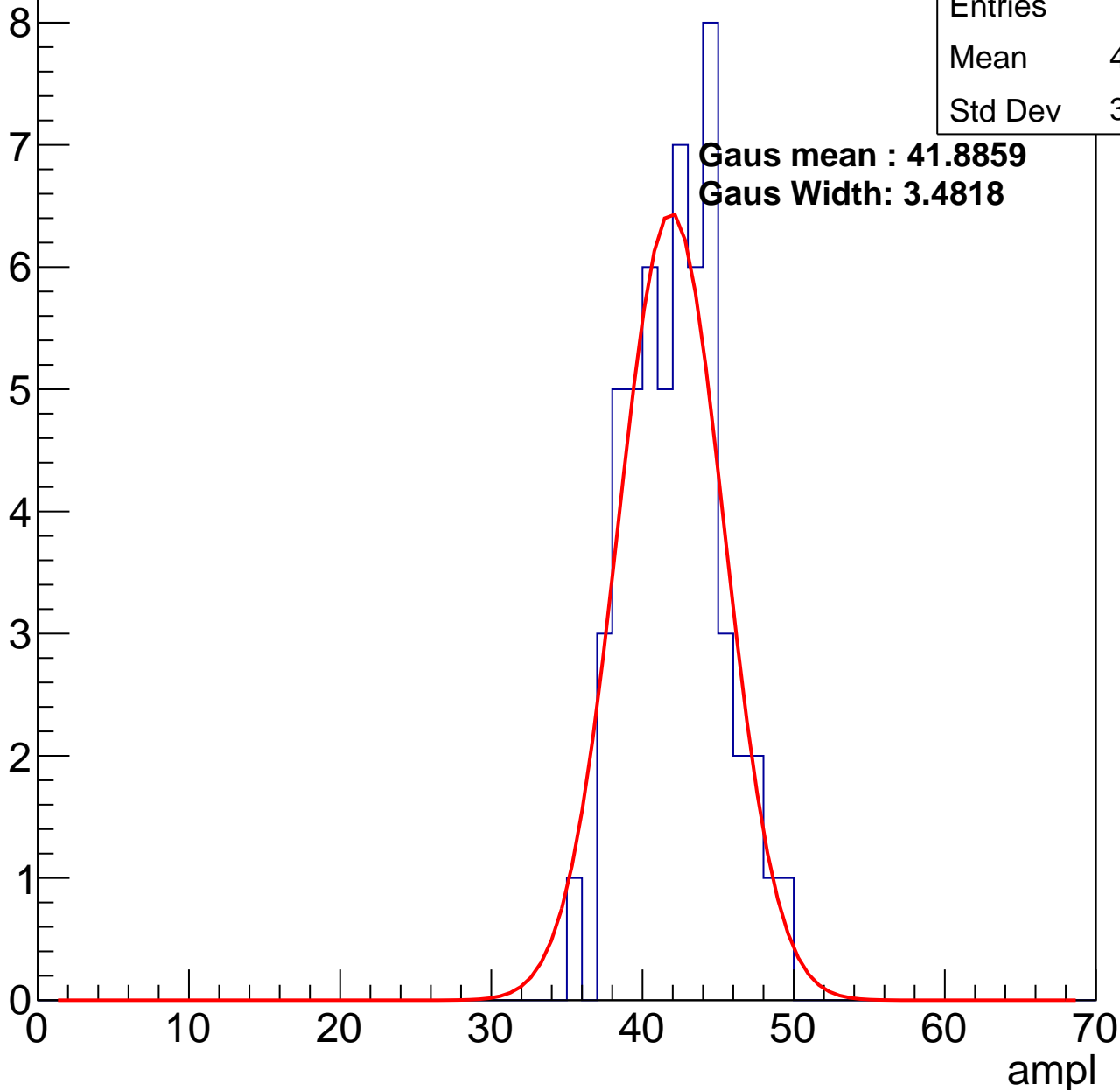
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	41.78
Std Dev	3.037

**Gaus mean : 41.8859**

**Gaus Width: 3.4818**

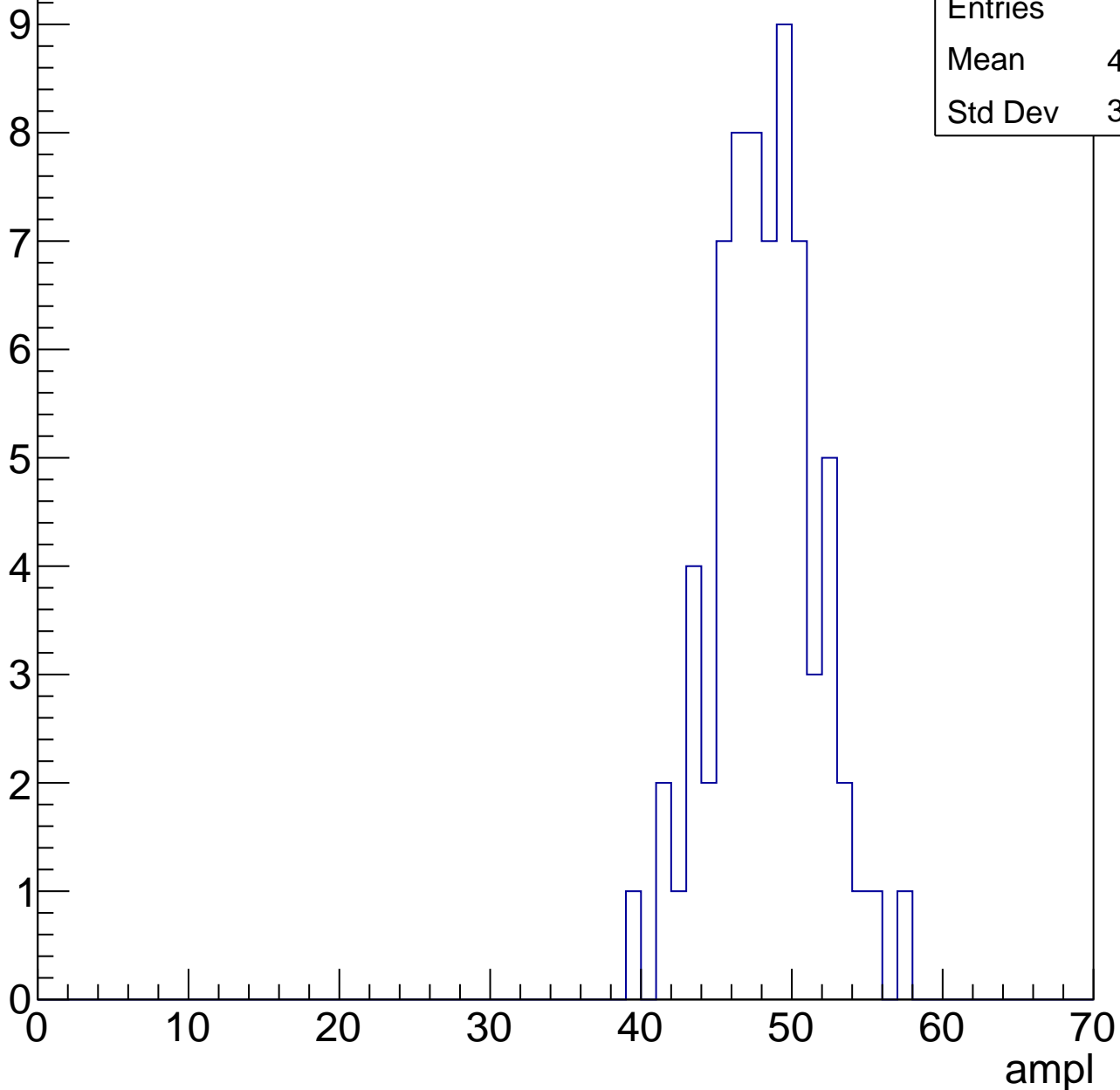


# B1L102S, U21-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

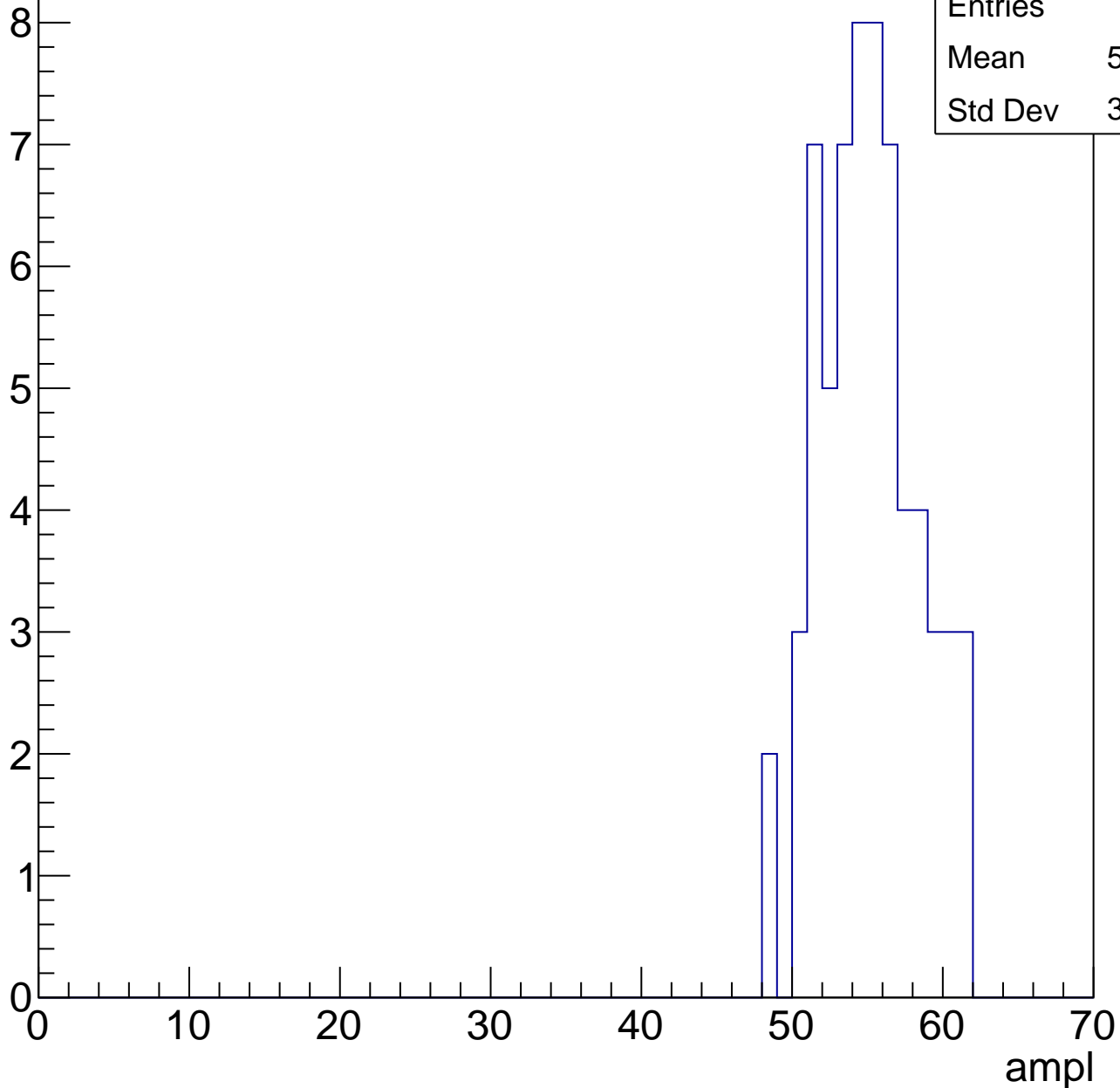
Entries	69
Mean	47.74
Std Dev	3.416



# B1L102S, U21-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

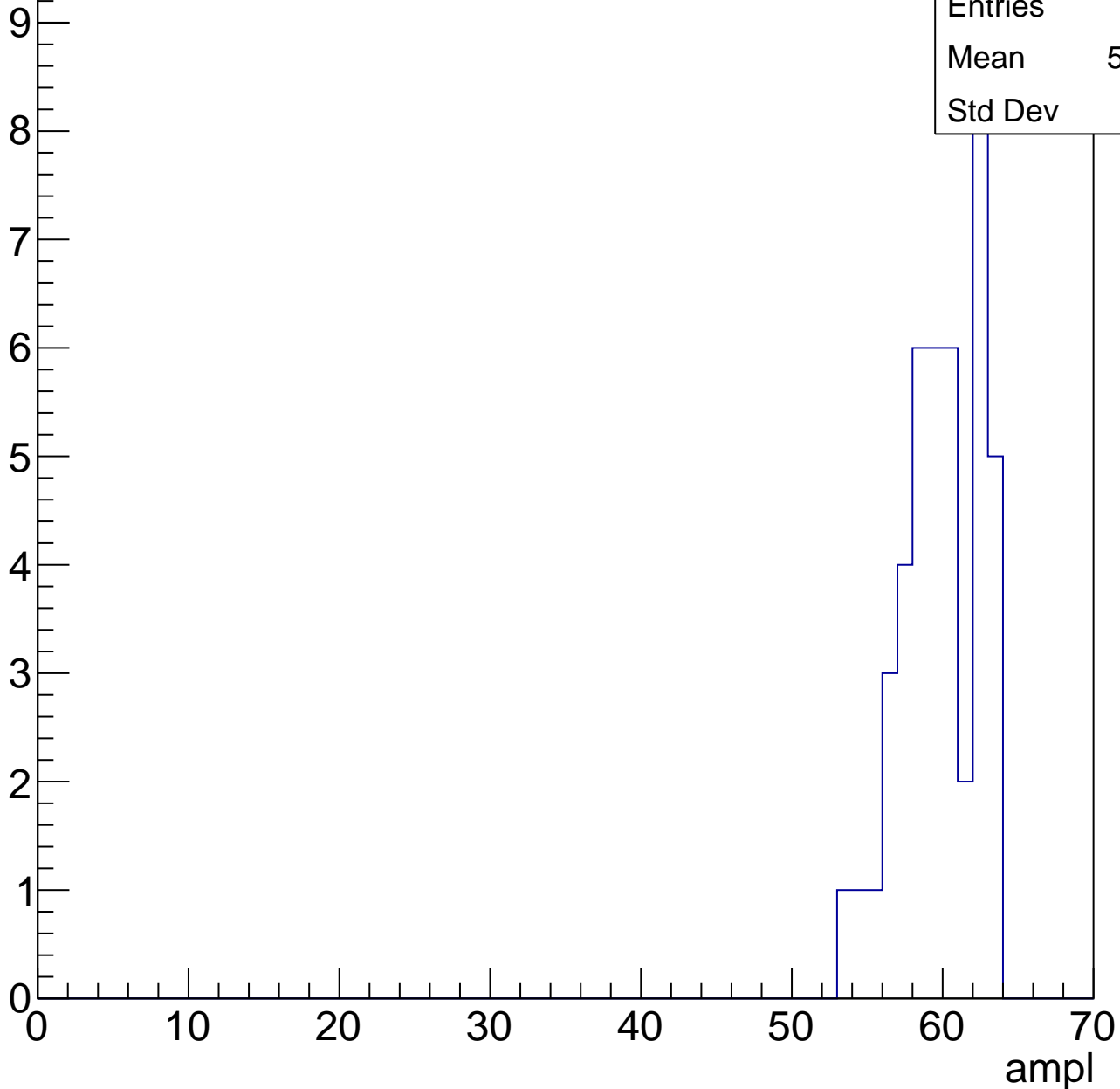


# B1L102S, U21-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	44
Mean	59.43
Std Dev	2.58

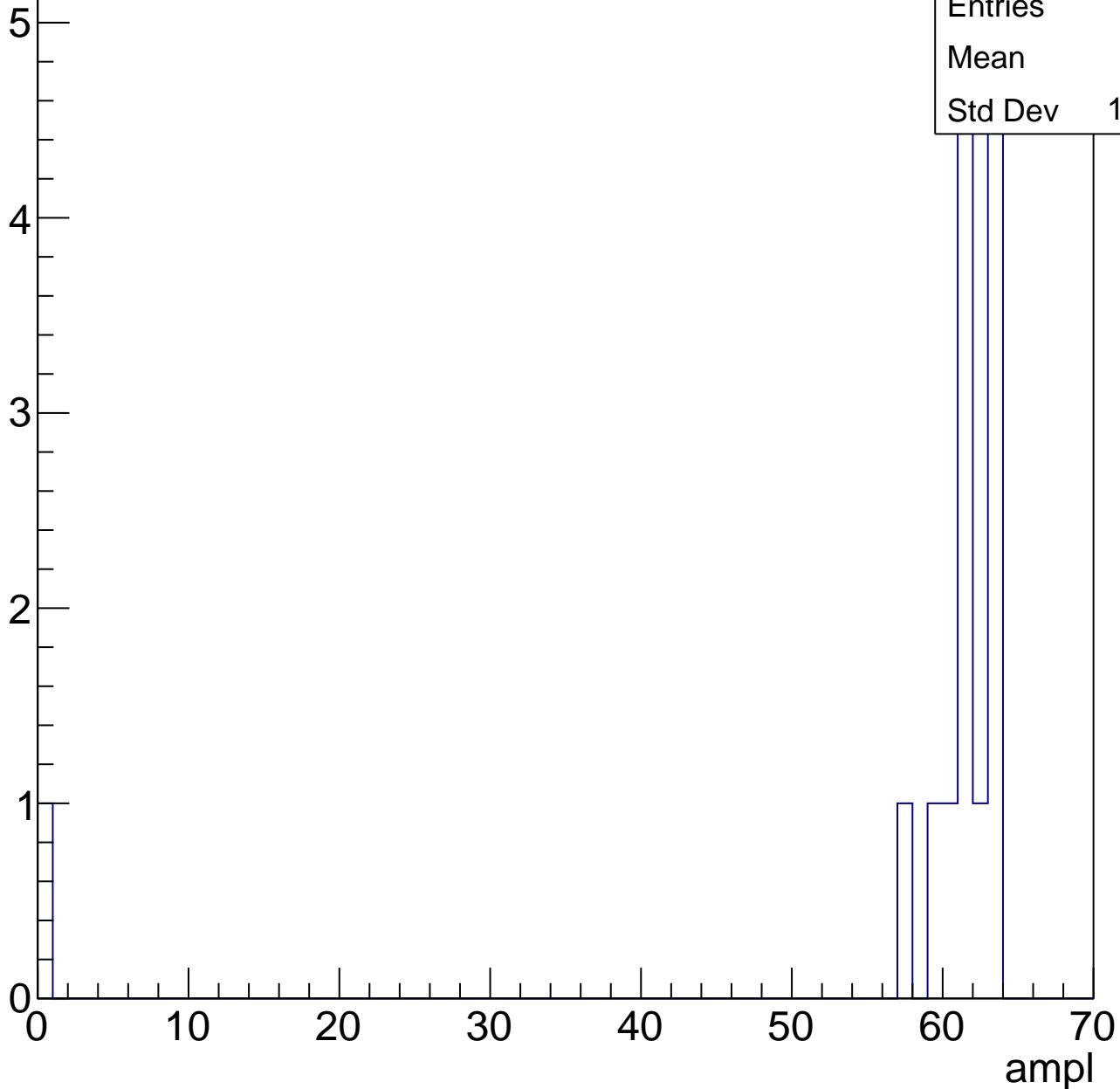


# B1L102S, U21-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	15
Mean	57.2
Std Dev	15.38





# B1L102S, U21-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U21-ch22, adc0

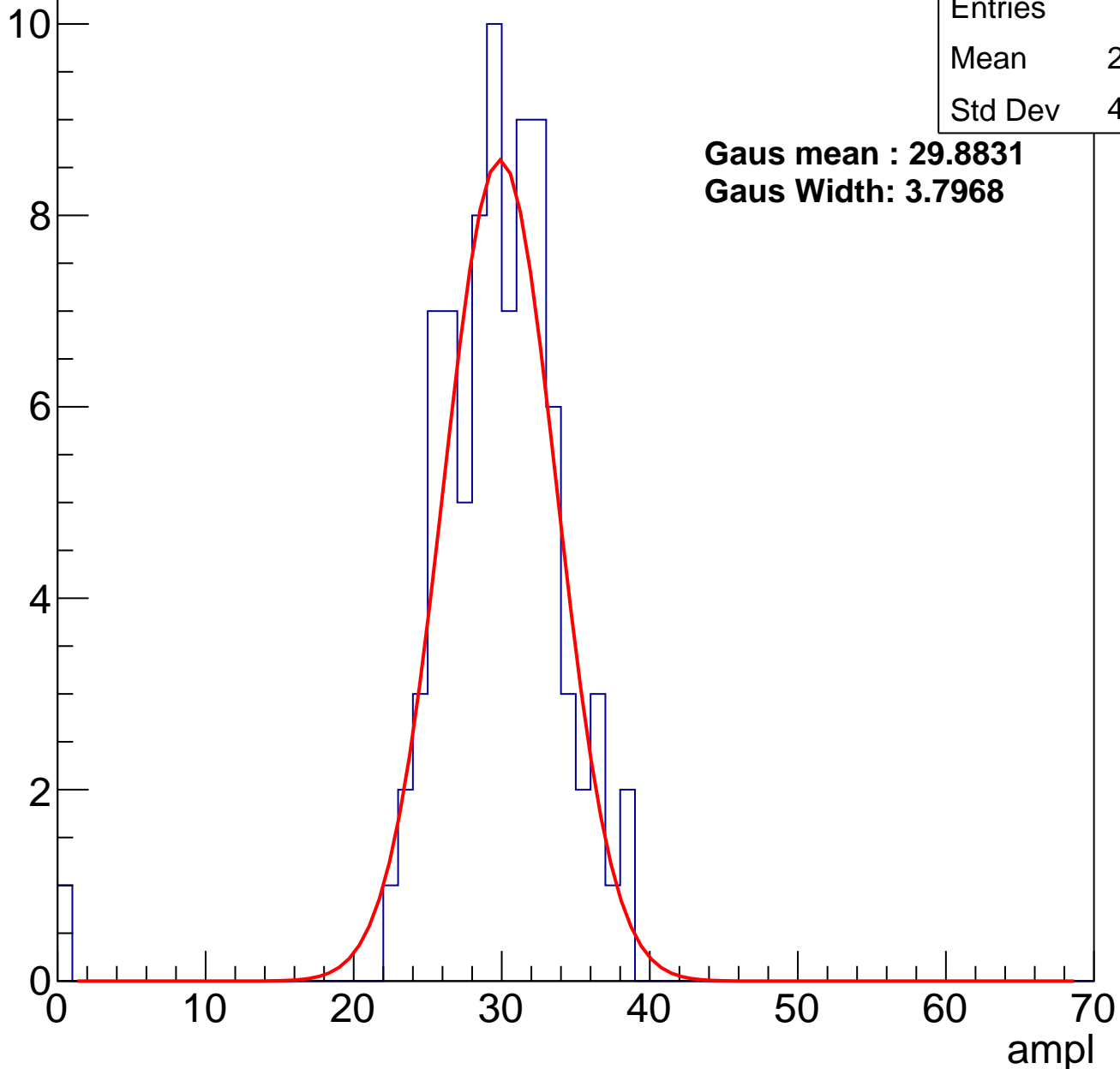
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	86
Mean	29.23
Std Dev	4.793

**Gaus mean : 29.8831**

**Gaus Width: 3.7968**

Entry



# B1L102S, U21-ch22, adc1

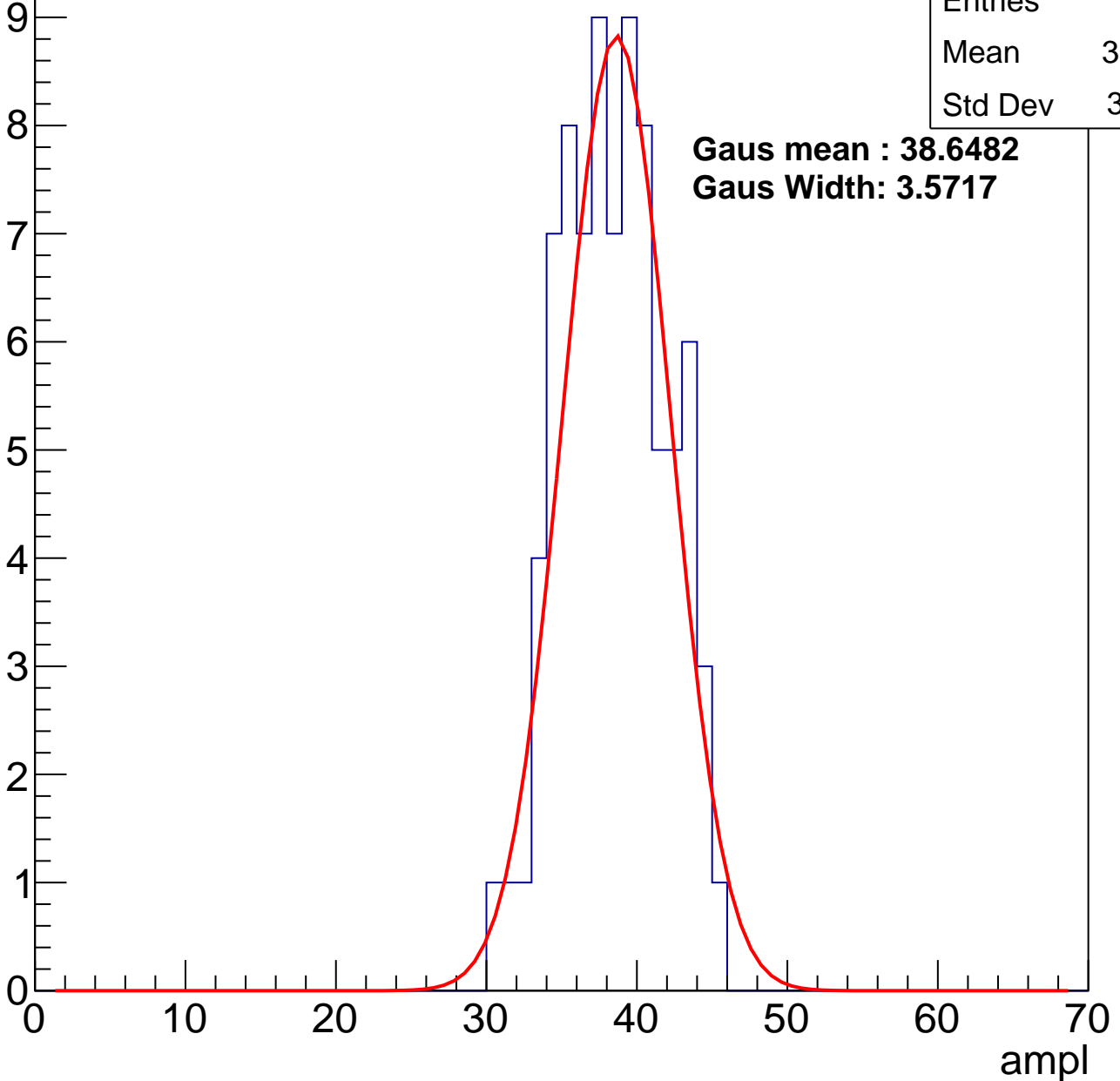
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	37.99
Std Dev	3.391

**Gaus mean : 38.6482**

**Gaus Width: 3.5717**



# B1L102S, U21-ch22, adc2

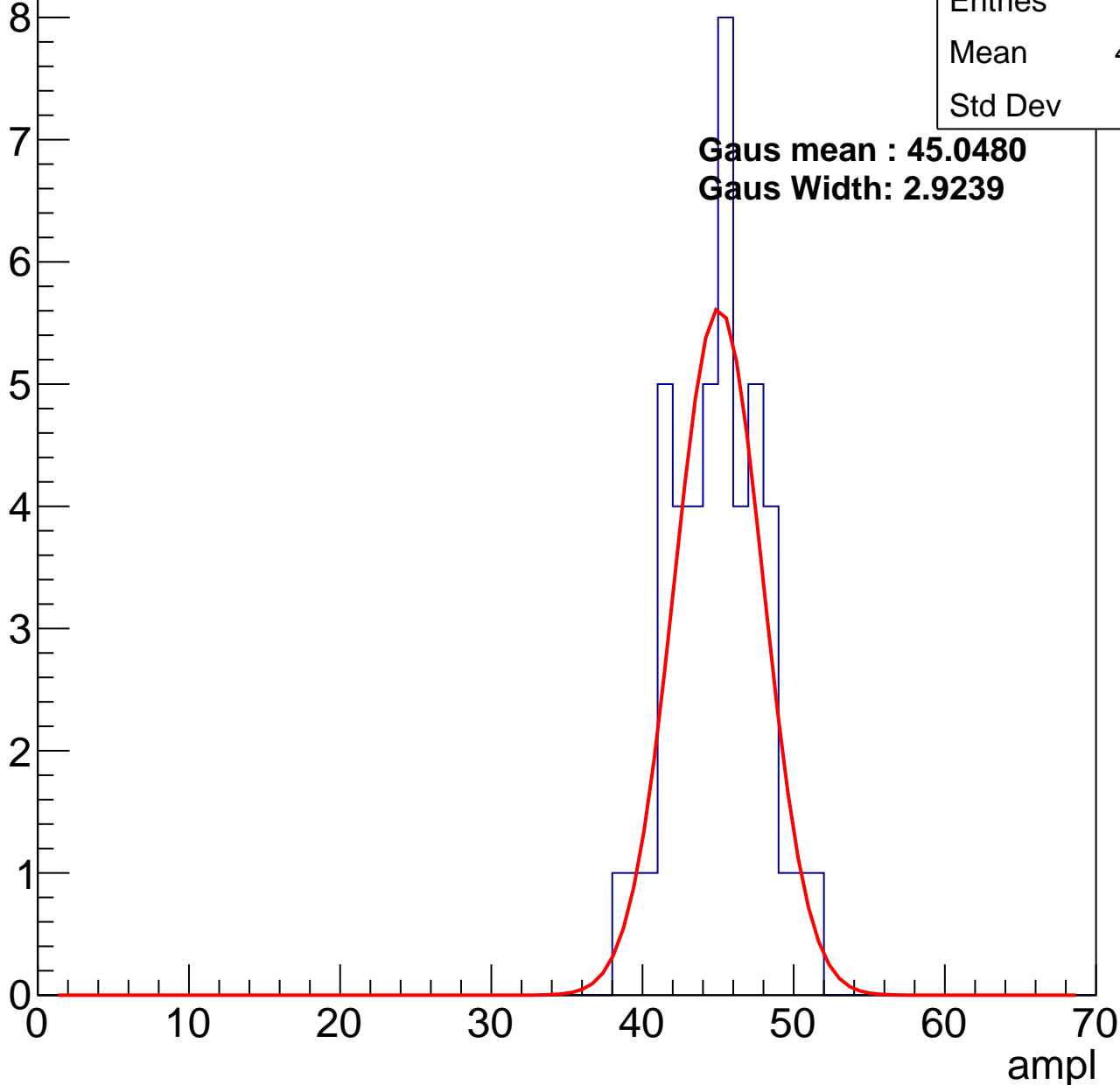
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	44.51
Std Dev	2.88

**Gaus mean : 45.0480**

**Gaus Width: 2.9239**

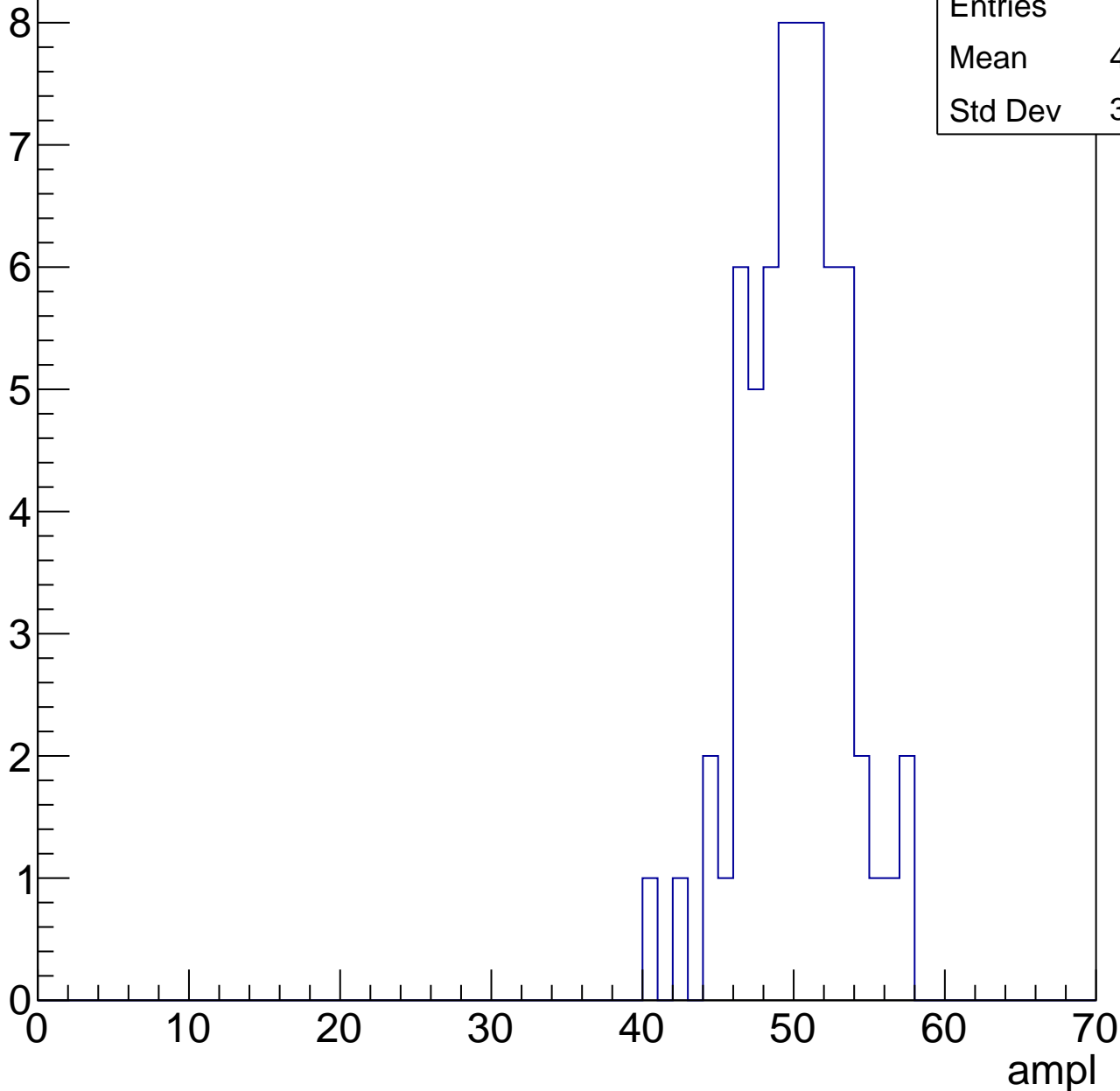


# B1L102S, U21-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	49.64
Std Dev	3.314

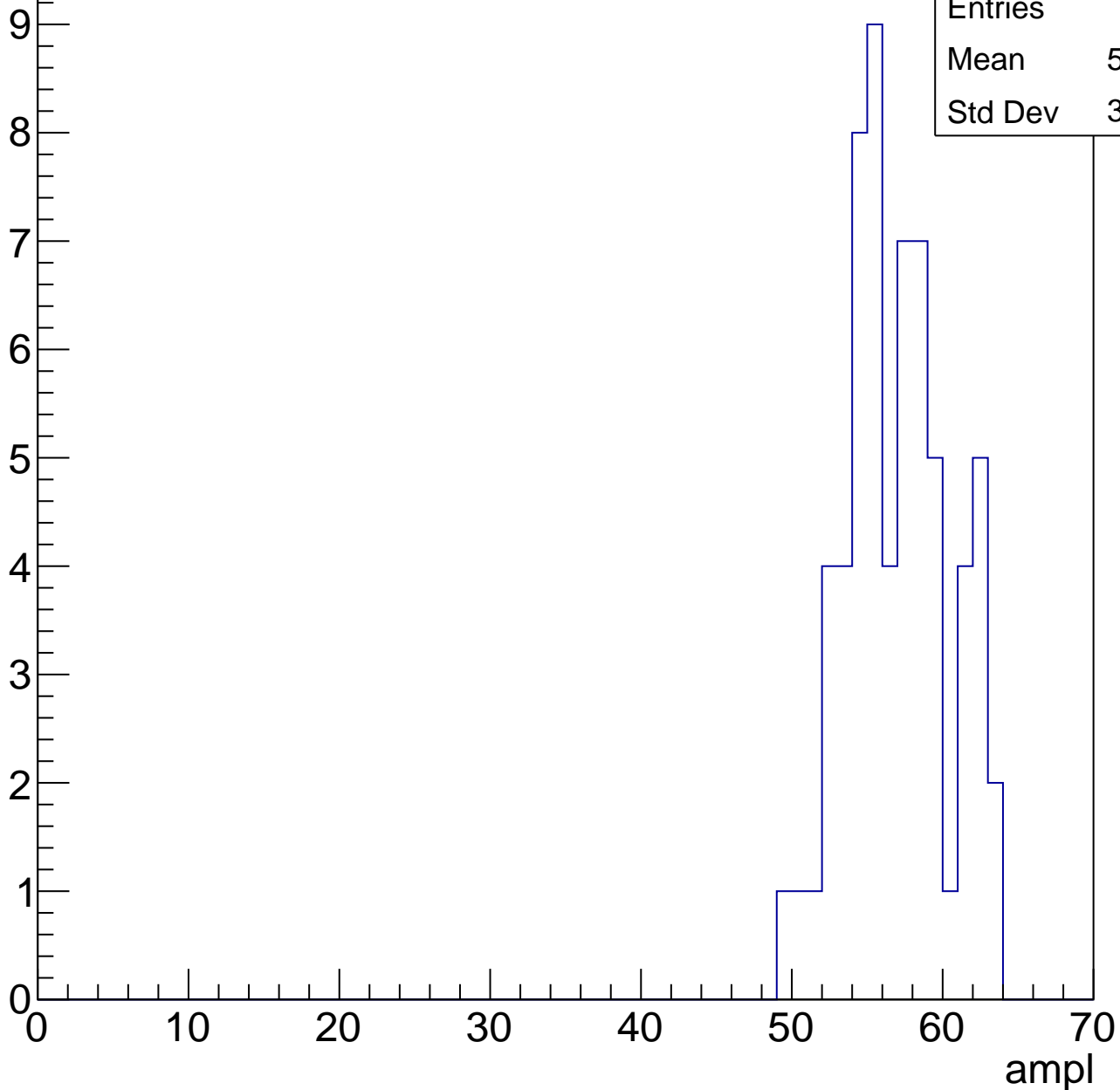


# B1L102S, U21-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	56.52
Std Dev	3.352



# B1L102S, U21-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

7

6

5

4

3

2

1

0

Entries

32

Mean

59.5

Std Dev

2.046

0

10

20

30

40

50

60

70

ampl

0

10

20

30

40

50

60

70

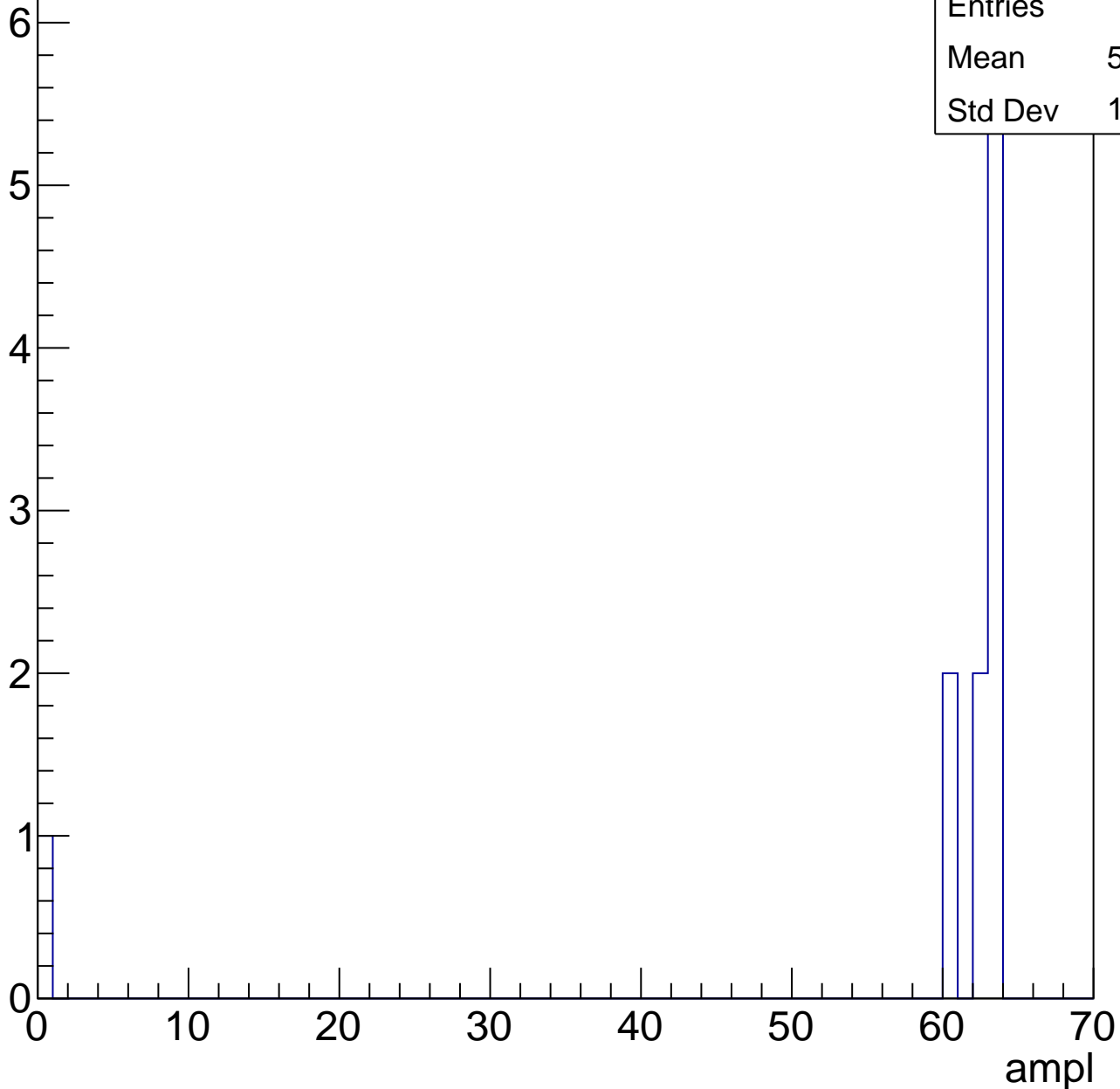
ampl

# B1L102S, U21-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	11
Mean	56.55
Std Dev	17.92





# B1L102S, U21-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U21-ch23, adc0

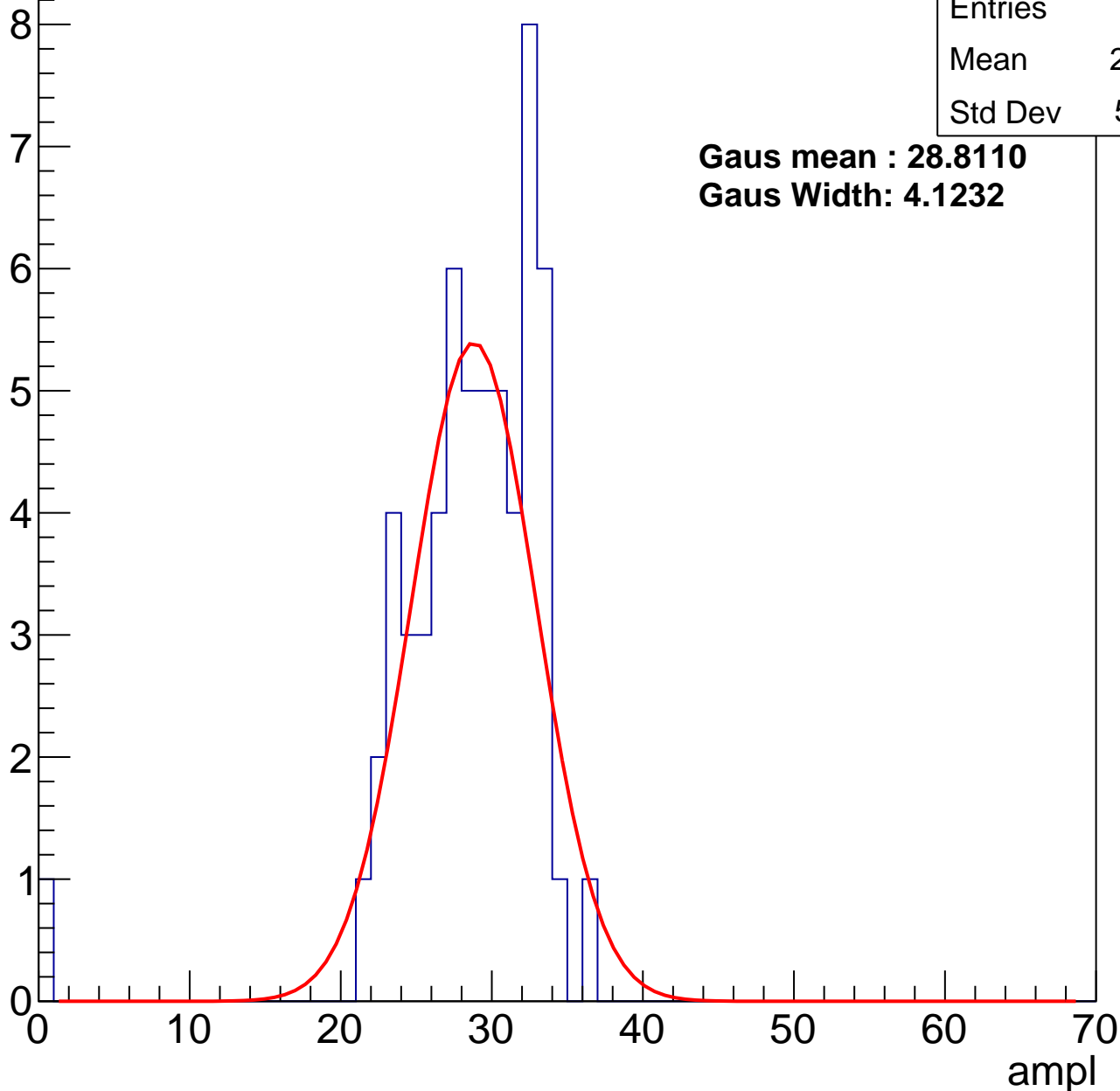
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	28.02
Std Dev	5.111

**Gaus mean : 28.8110**

**Gaus Width: 4.1232**



# B1L102S, U21-ch23, adc1

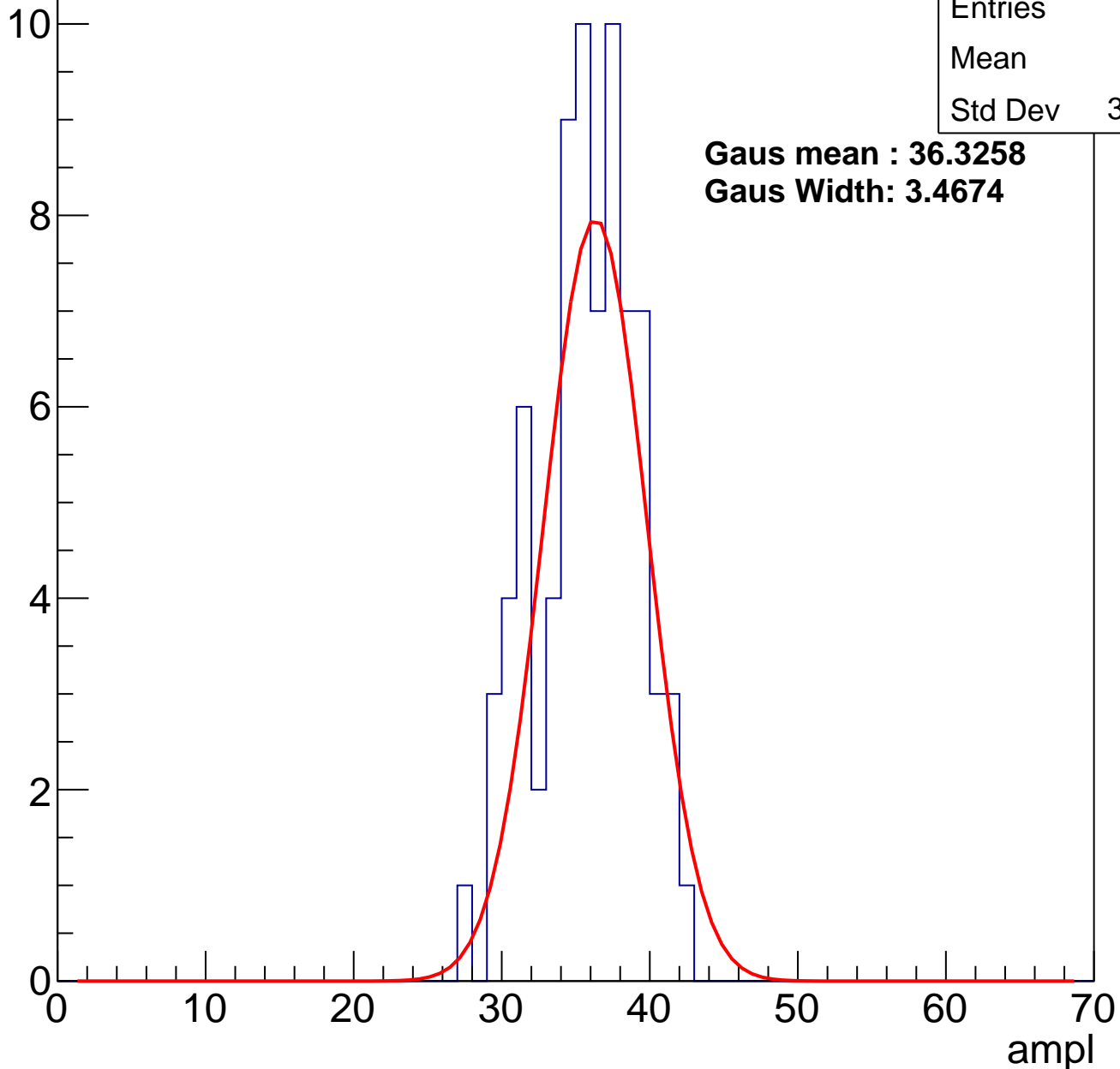
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	77
Mean	35.3
Std Dev	3.338

**Gaus mean : 36.3258**

**Gaus Width: 3.4674**

Entry



# B1L102S, U21-ch23, adc2

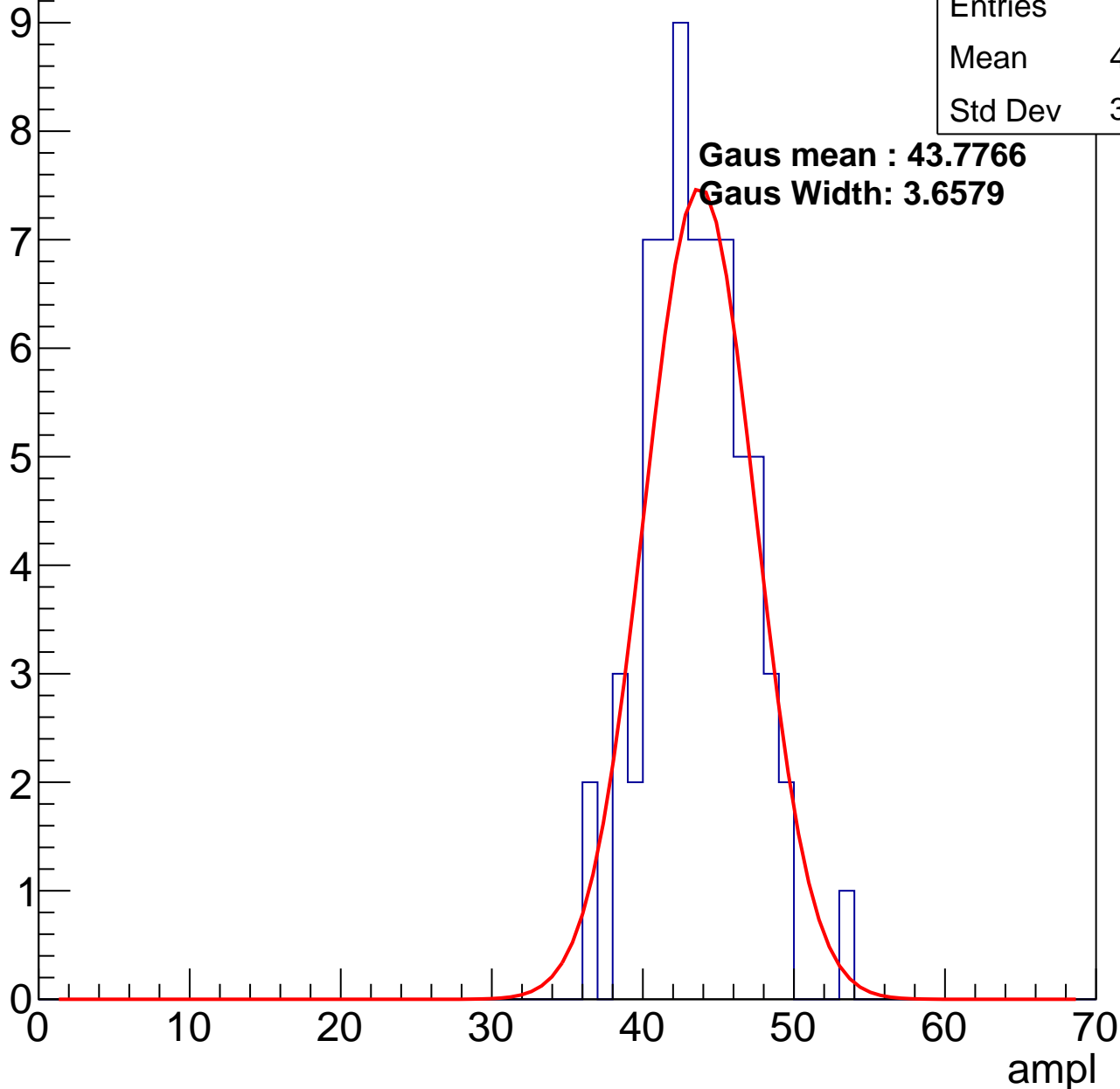
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	43.18
Std Dev	3.255

**Gaus mean : 43.7766**

**Gaus Width: 3.6579**

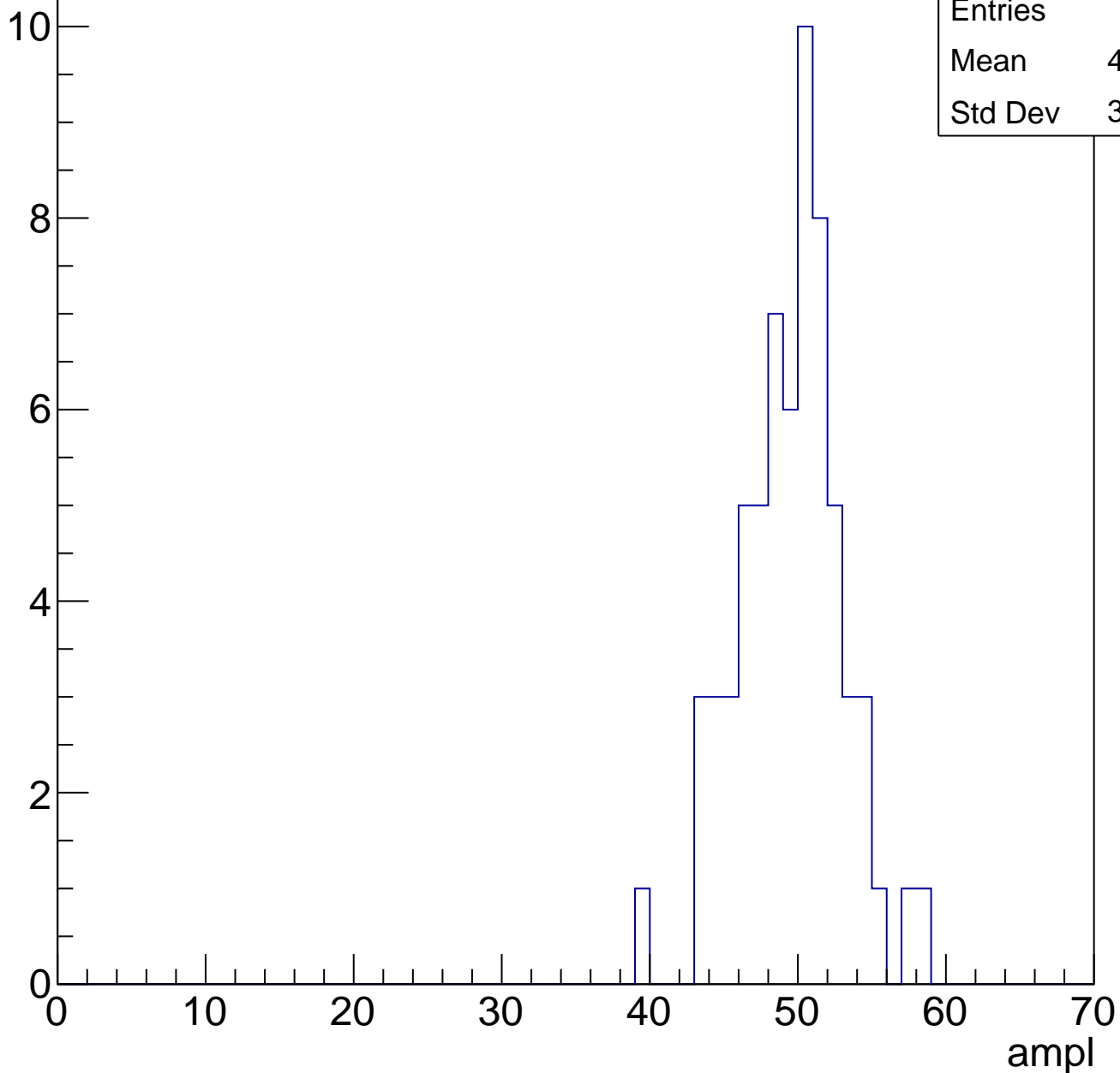


# B1L102S, U21-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	49.06
Std Dev	3.495

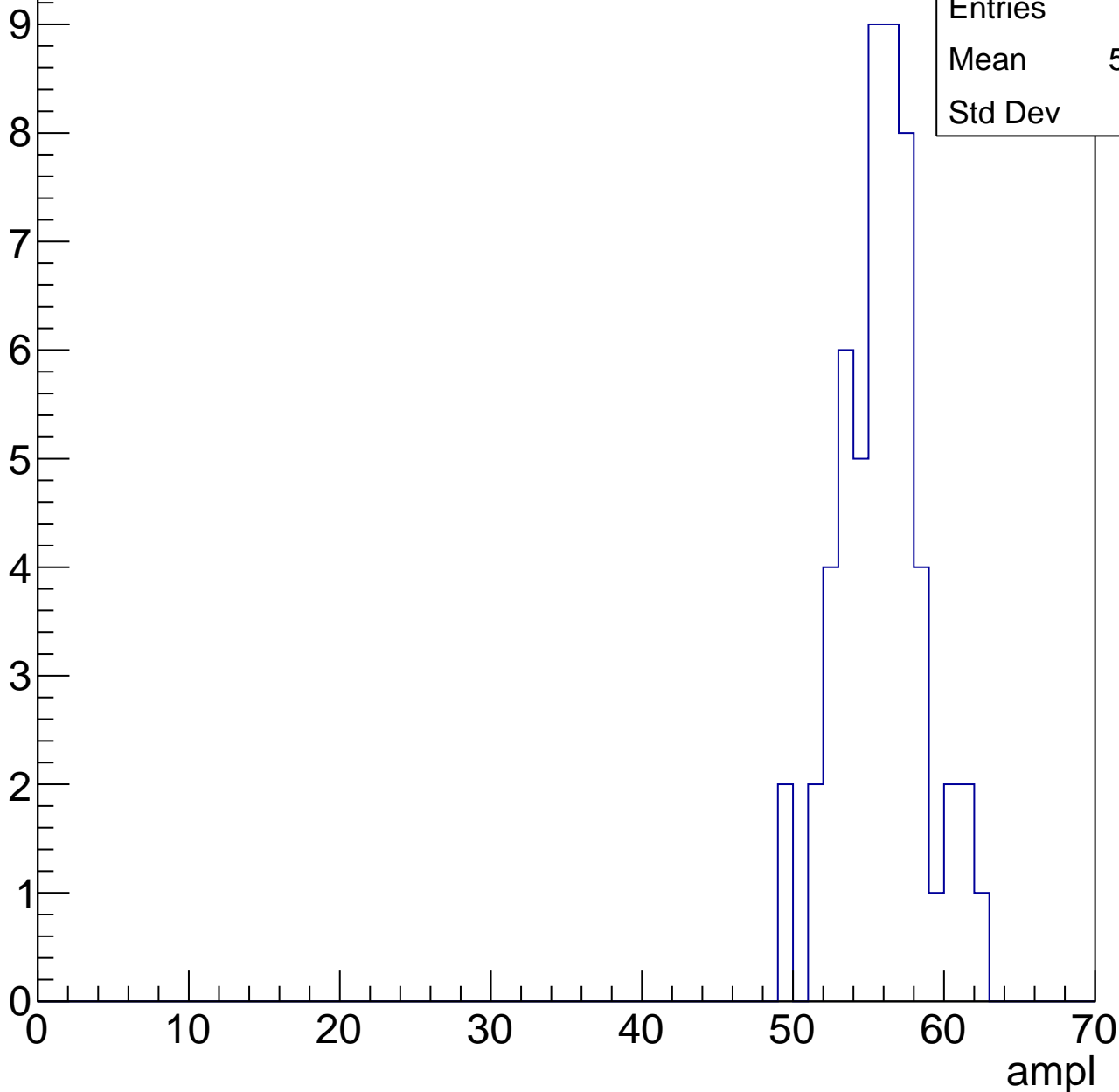


# B1L102S, U21-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	55.38
Std Dev	2.78

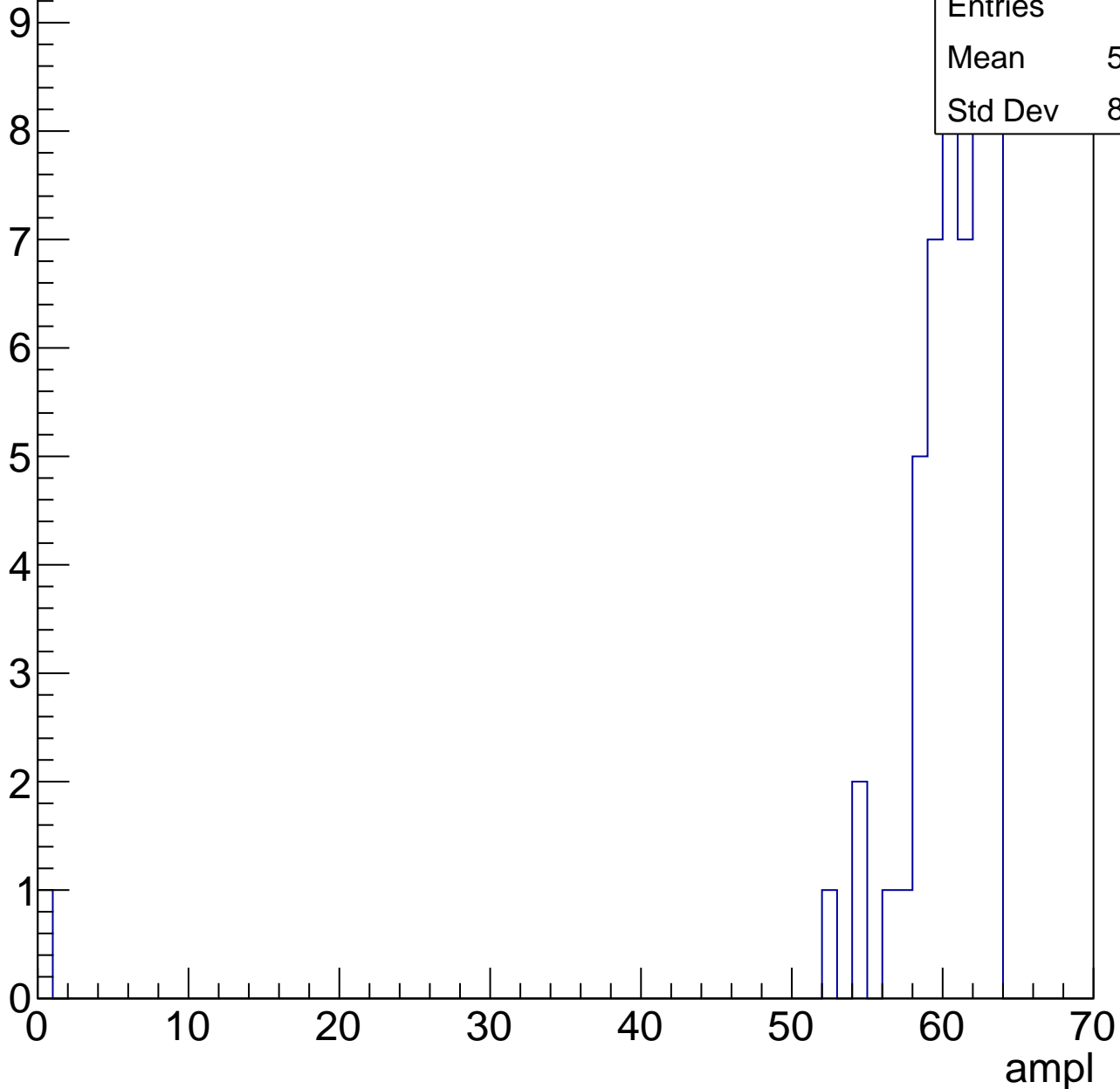


# B1L102S, U21-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

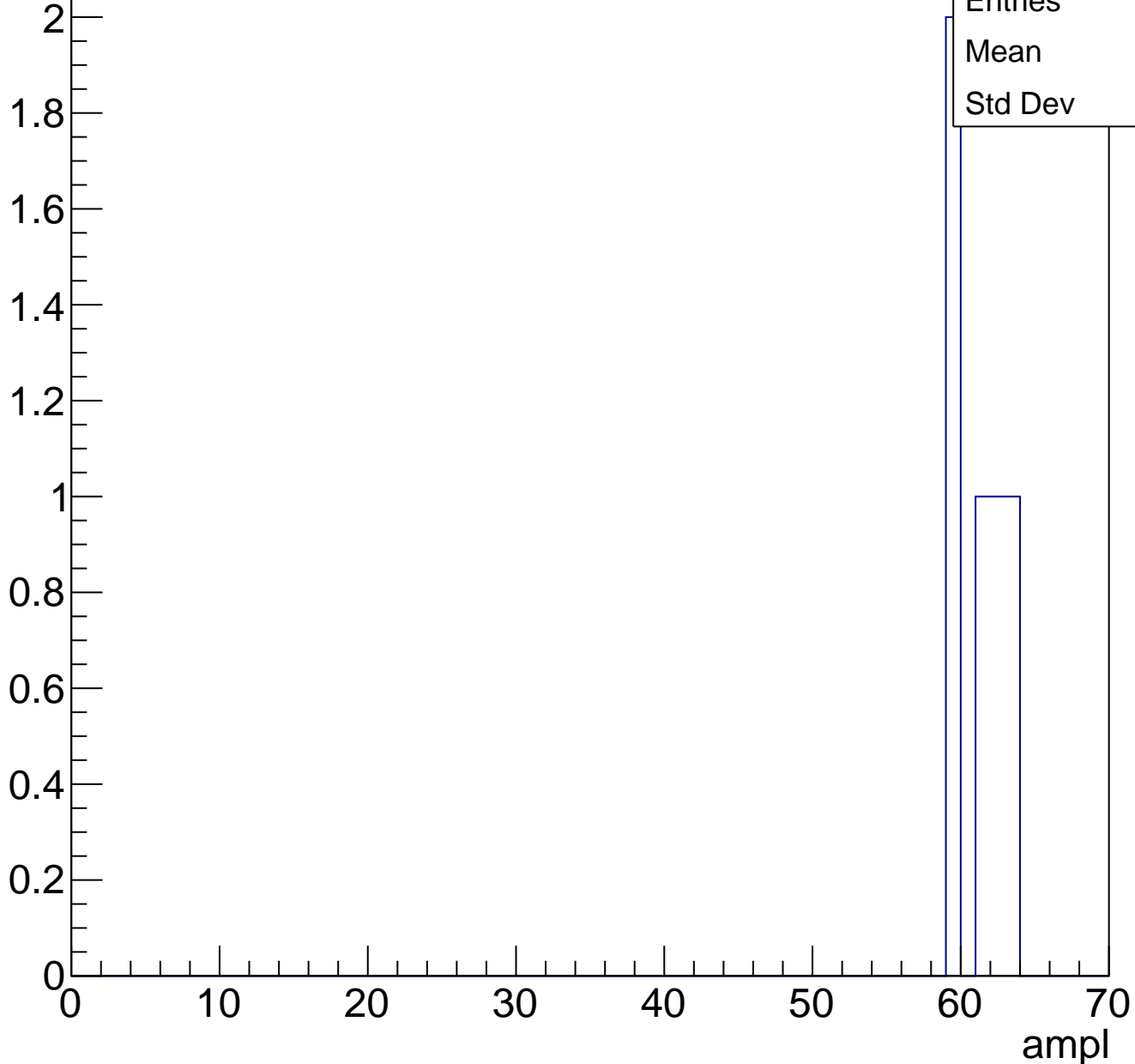
Entries	50
Mean	58.92
Std Dev	8.775



# B1L102S, U21-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch24, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	66
Mean	28.18
Std Dev	3.205

**Gaus mean : 27.9510**

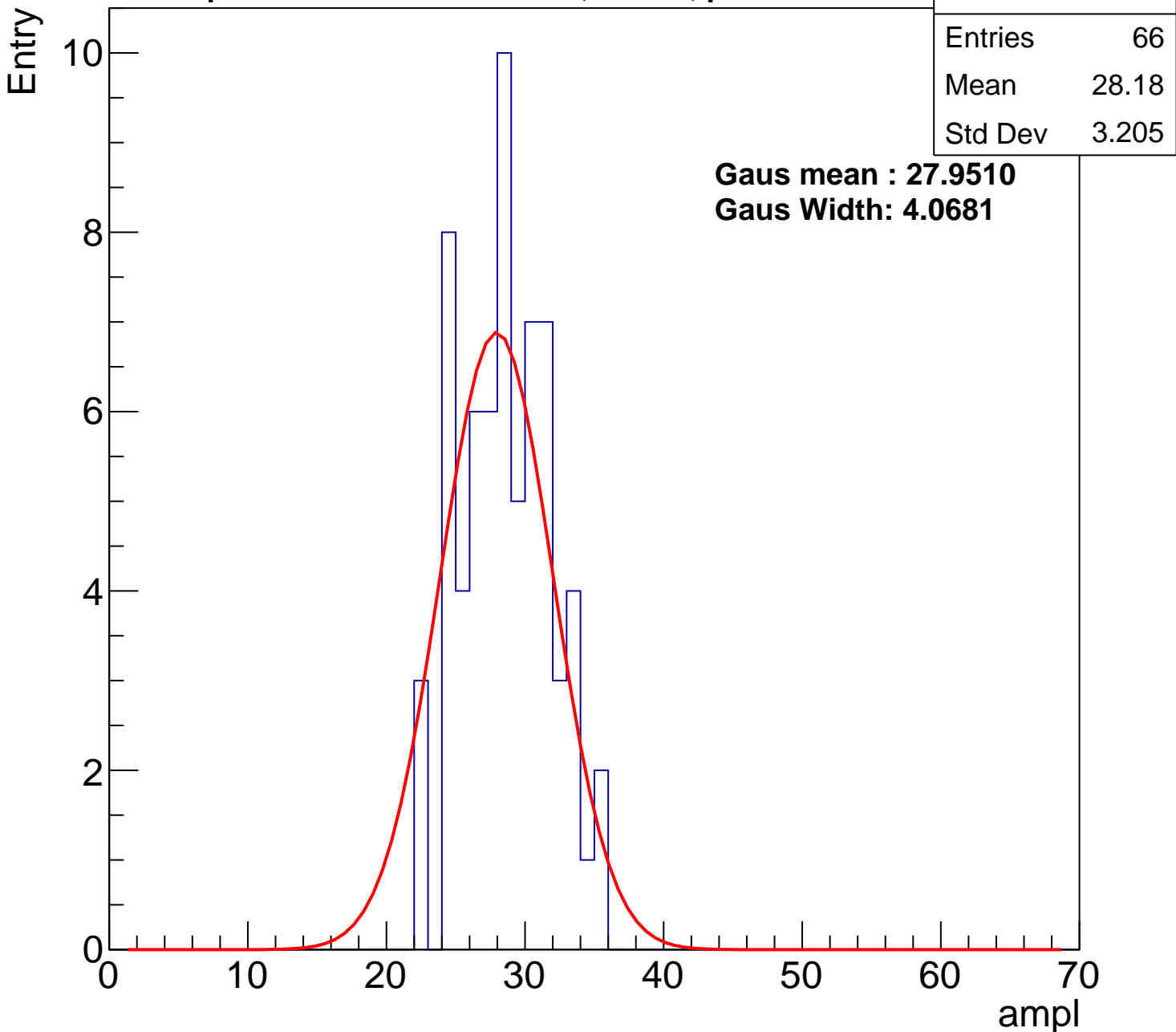
**Gaus Width: 4.0681**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U21-ch24, adc1

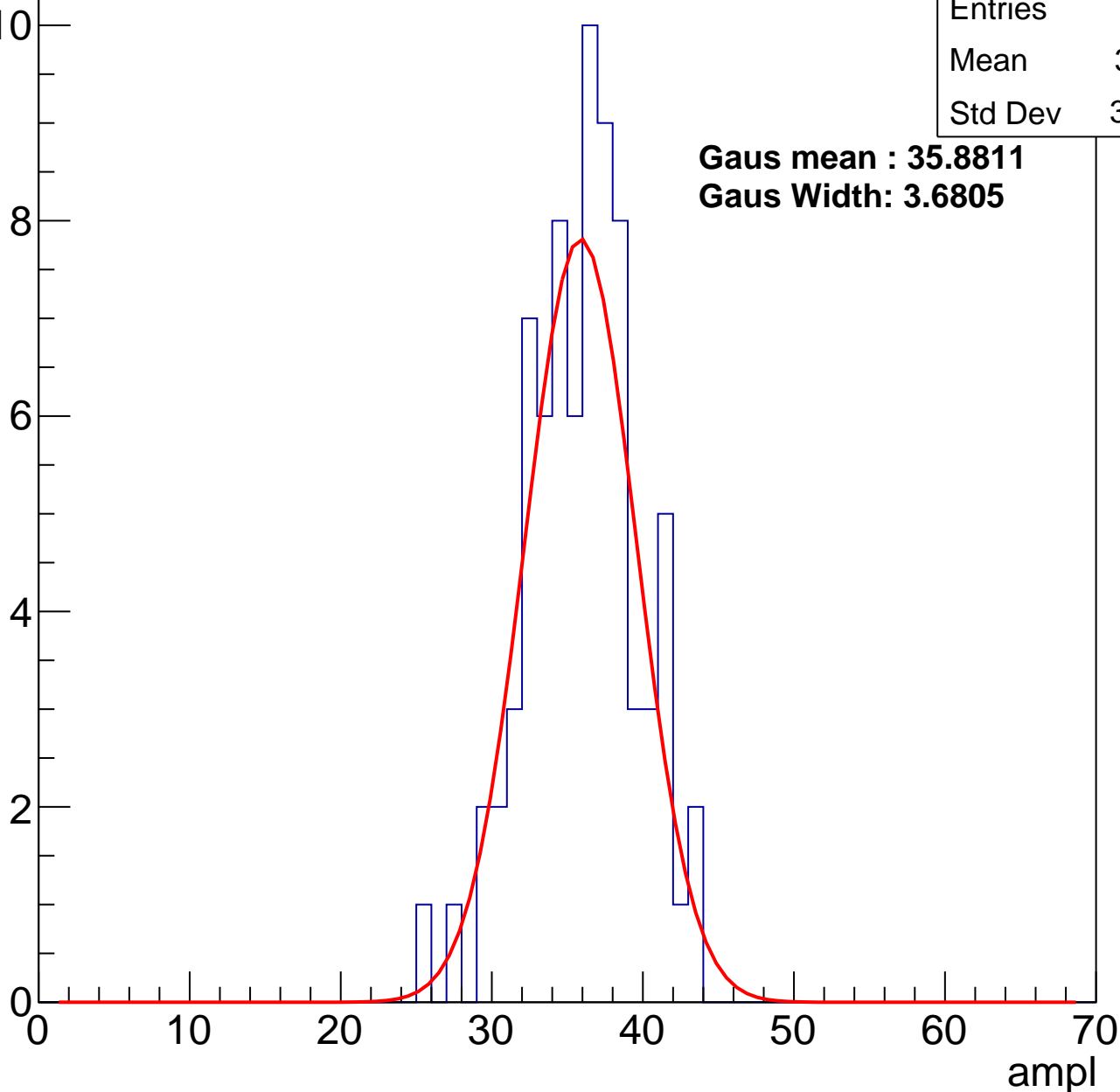
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	35.51
Std Dev	3.617

**Gaus mean : 35.8811**

**Gaus Width: 3.6805**

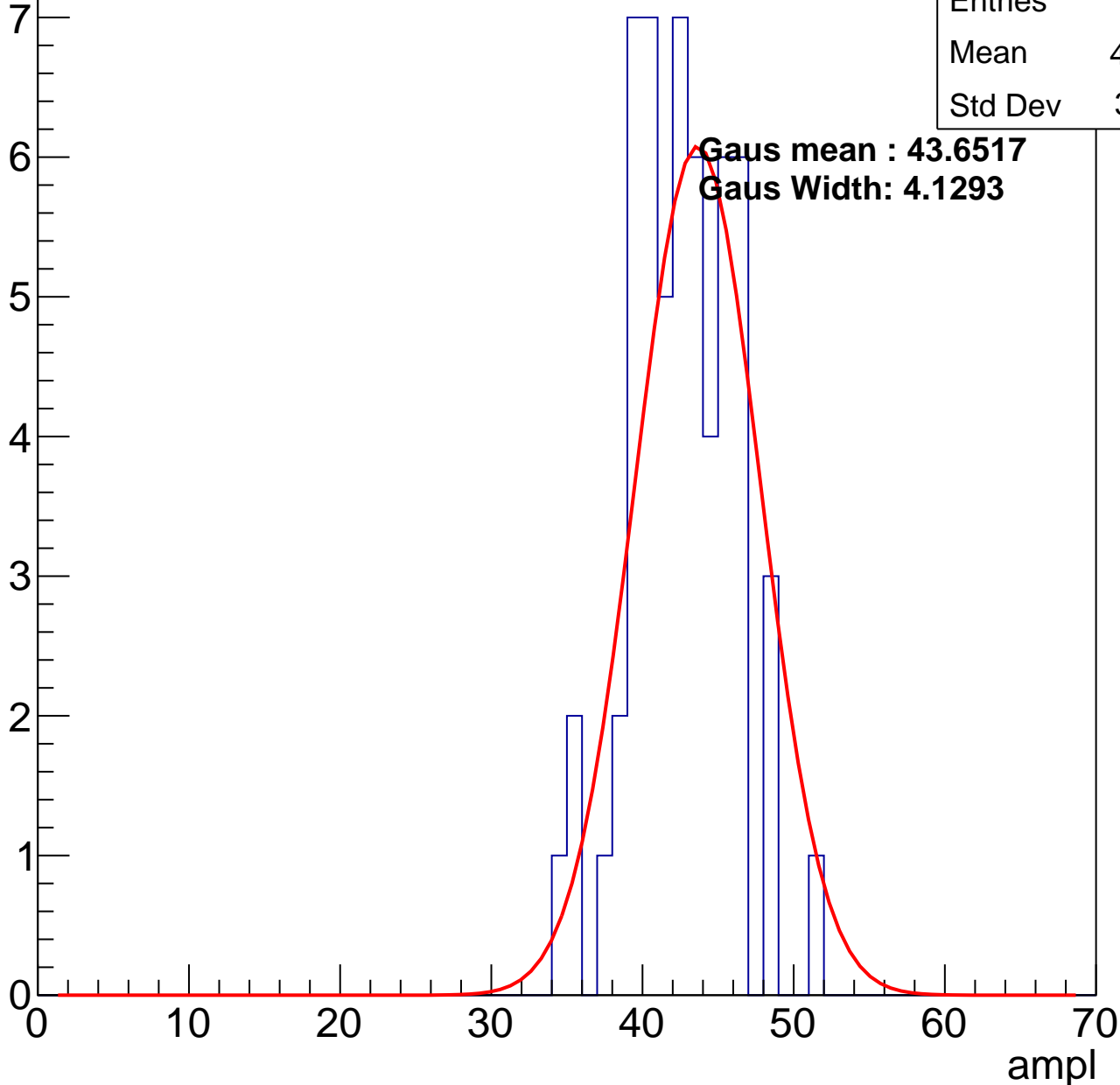


# B1L102S, U21-ch24, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	42.14
Std Dev	3.411



# B1L102S, U21-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

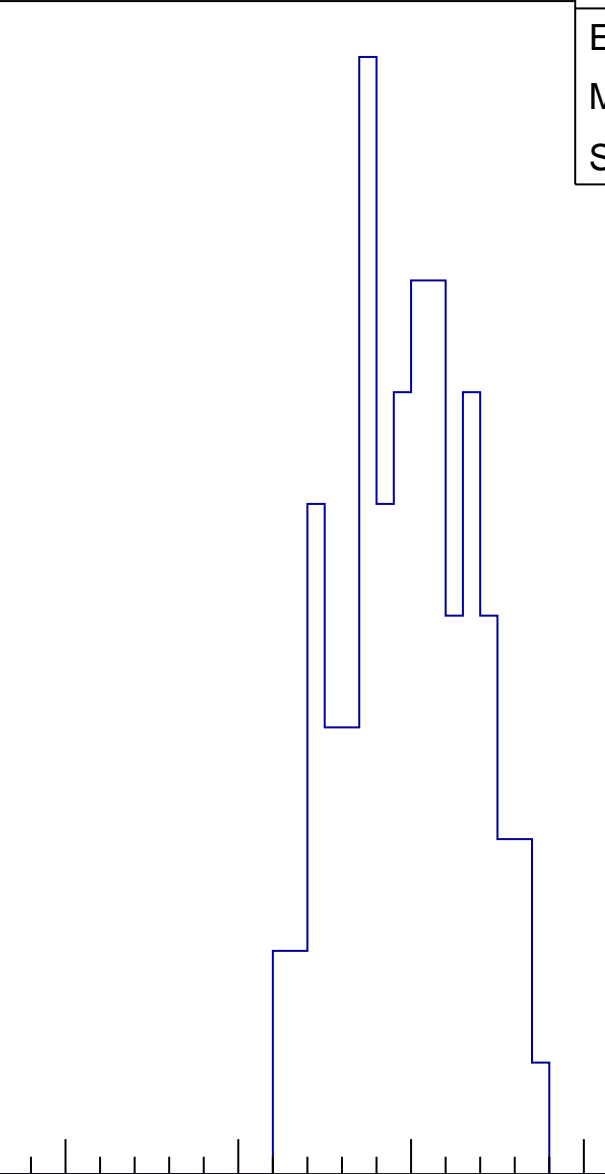
Entries	81
Mean	49.36
Std Dev	3.679

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

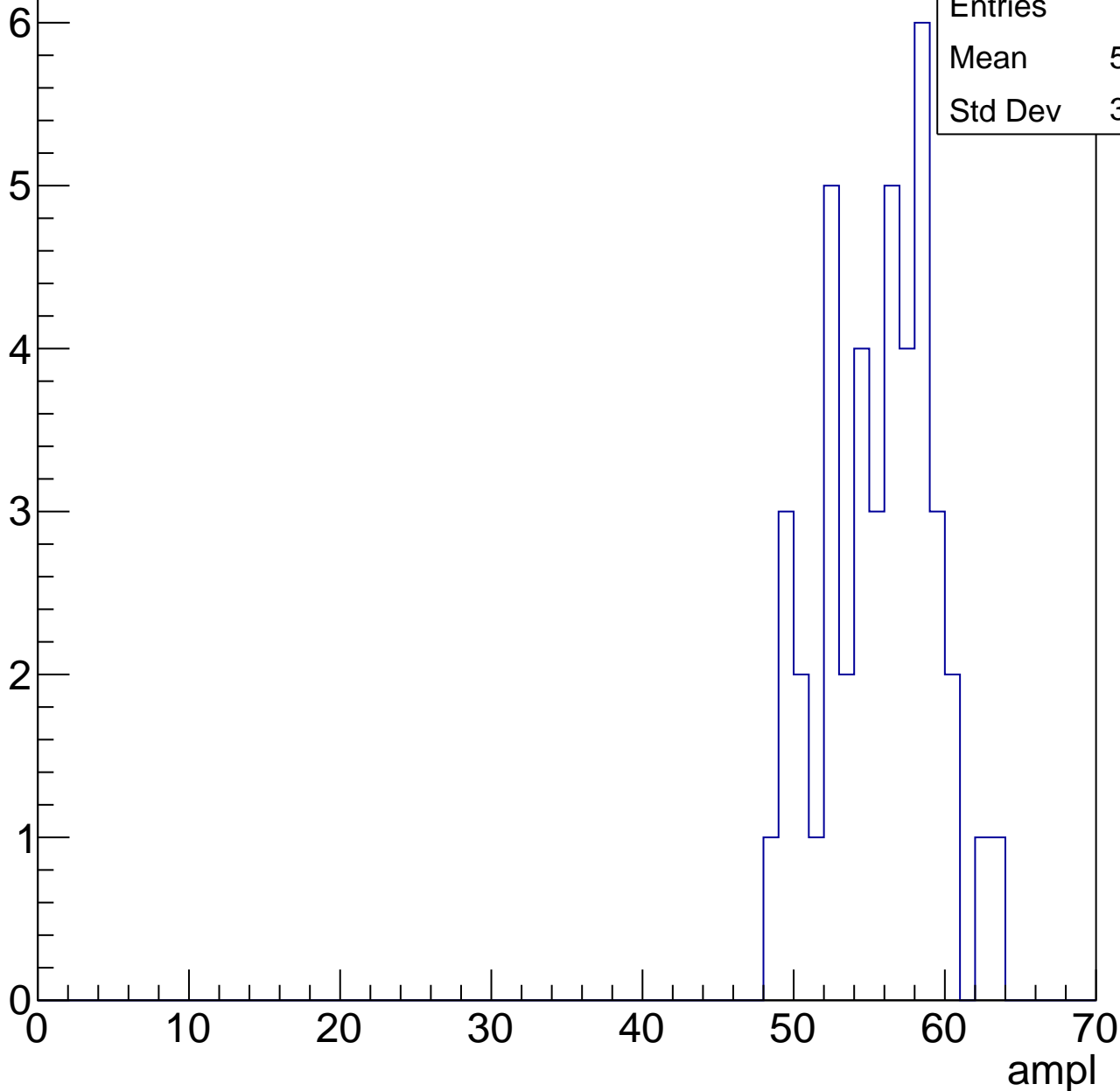


# B1L102S, U21-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	43
Mean	55.14
Std Dev	3.625

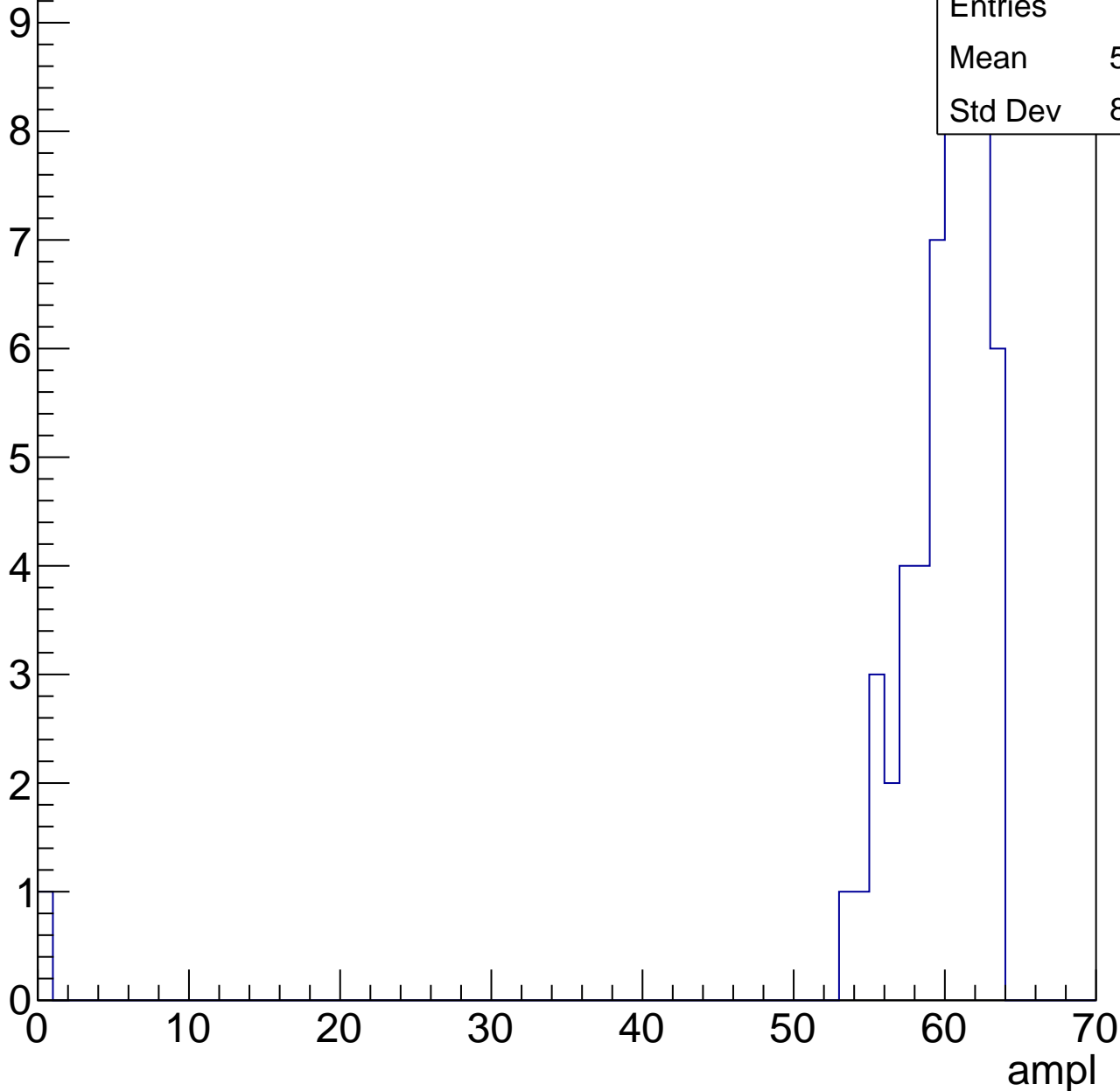


# B1L102S, U21-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

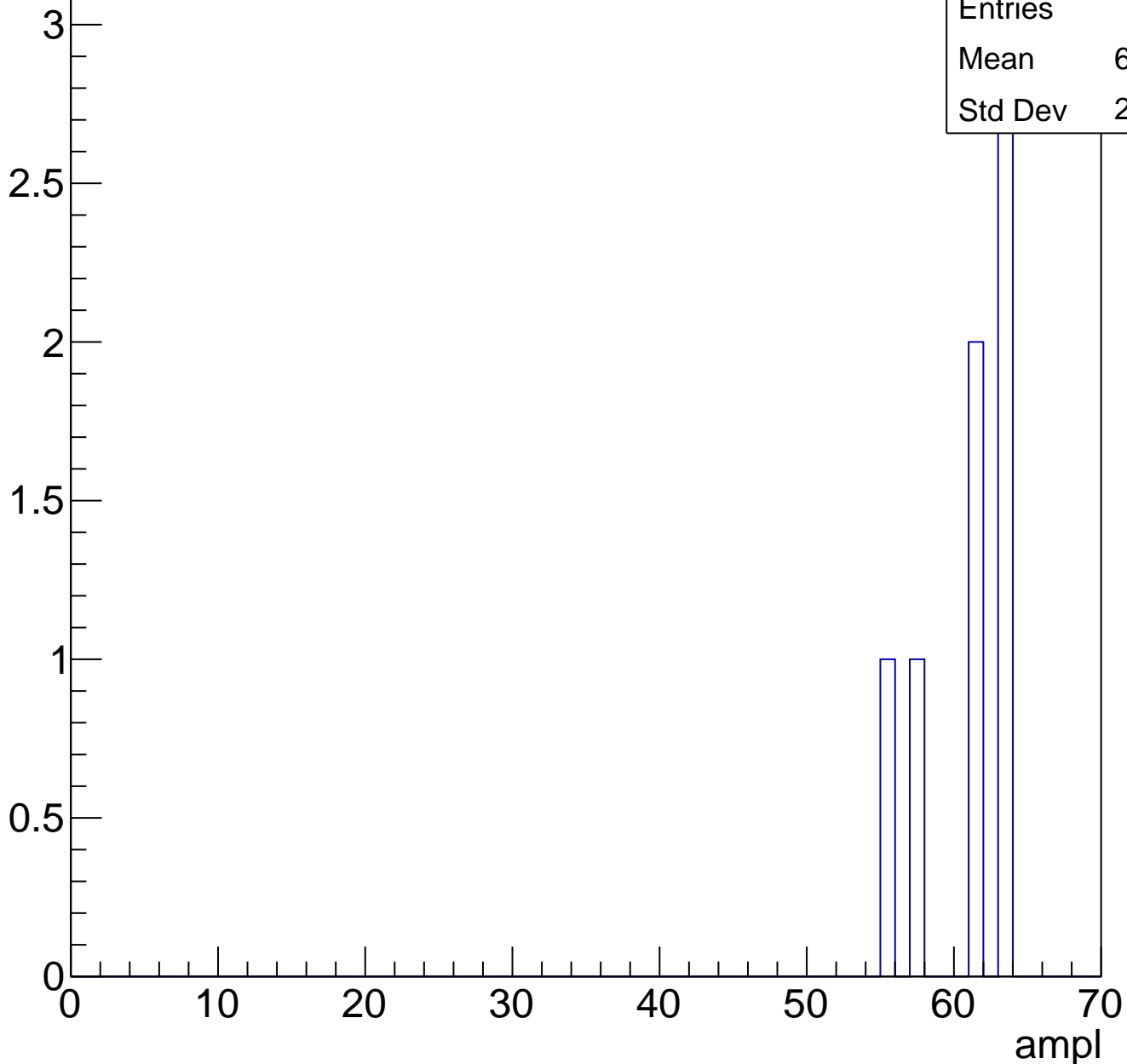
Entries	54
Mean	58.54
Std Dev	8.426



# B1L102S, U21-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	7
Mean	60.43
Std Dev	2.969



# B1L102S, U21-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch25, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	80
Mean	30.16
Std Dev	3.523

**Gaus mean : 30.9838**

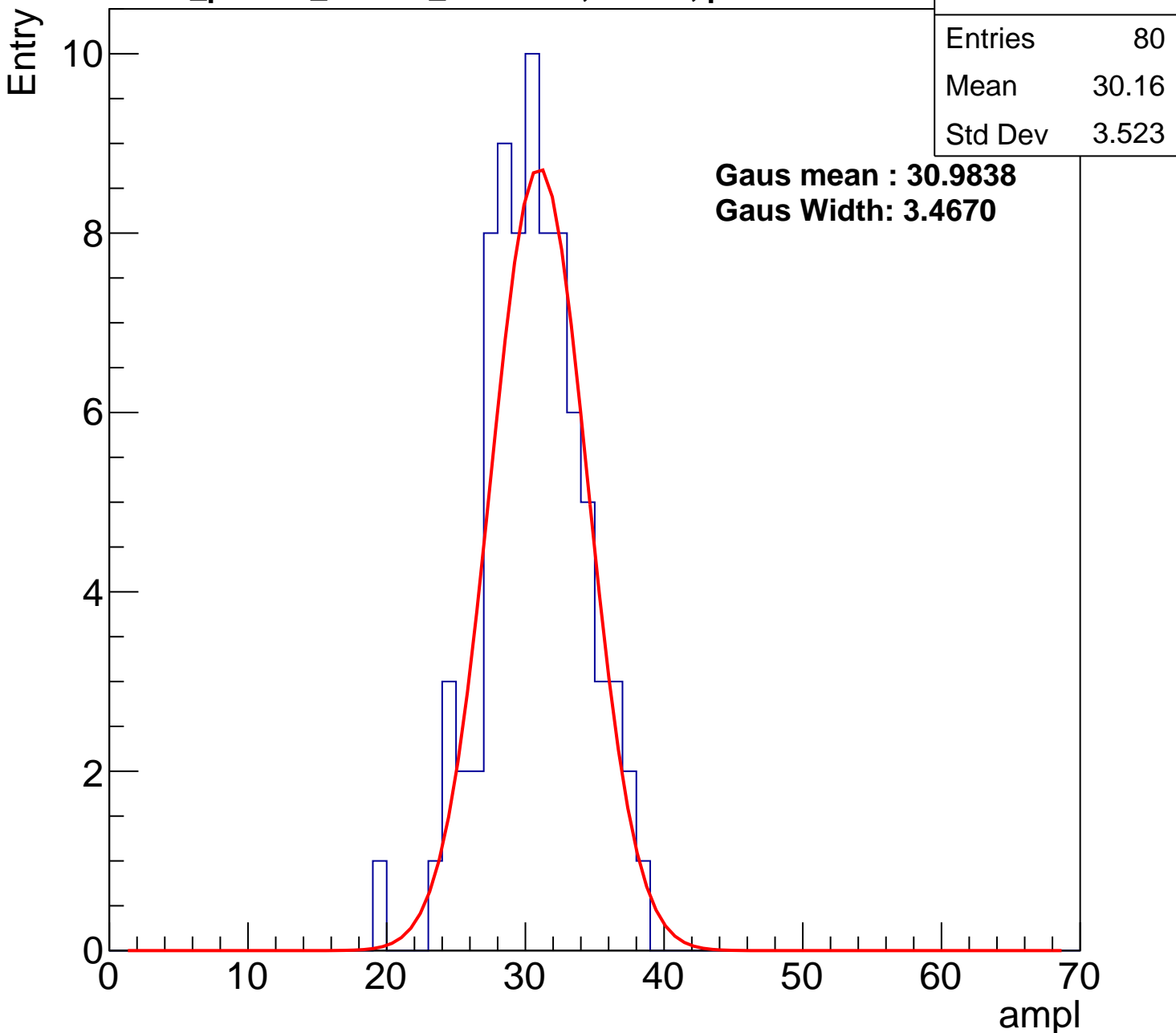
**Gaus Width: 3.4670**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



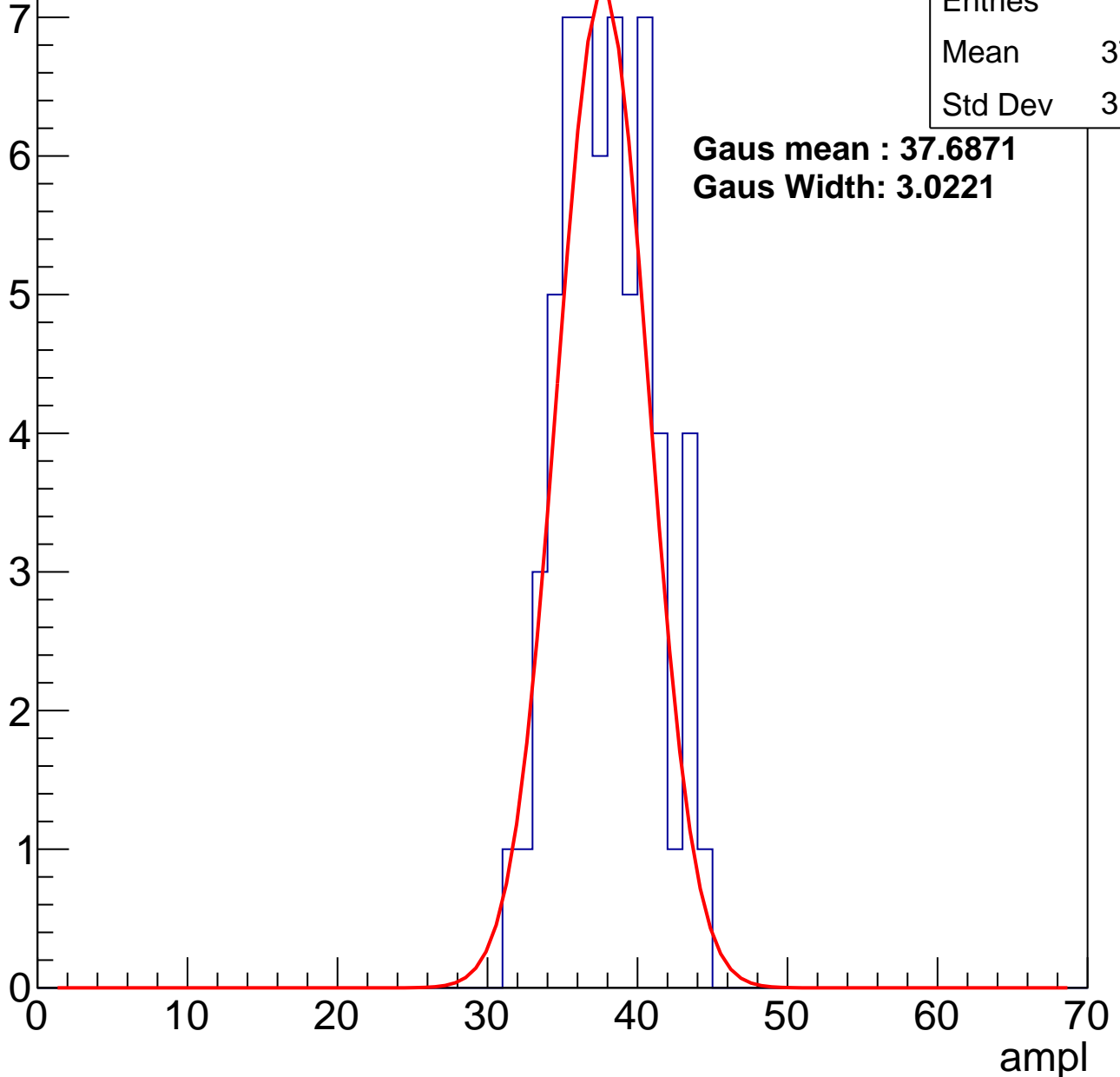
# B1L102S, U21-ch25, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	37.53
Std Dev	3.038

**Gaus mean : 37.6871**  
**Gaus Width: 3.0221**



# B1L102S, U21-ch25, adc2

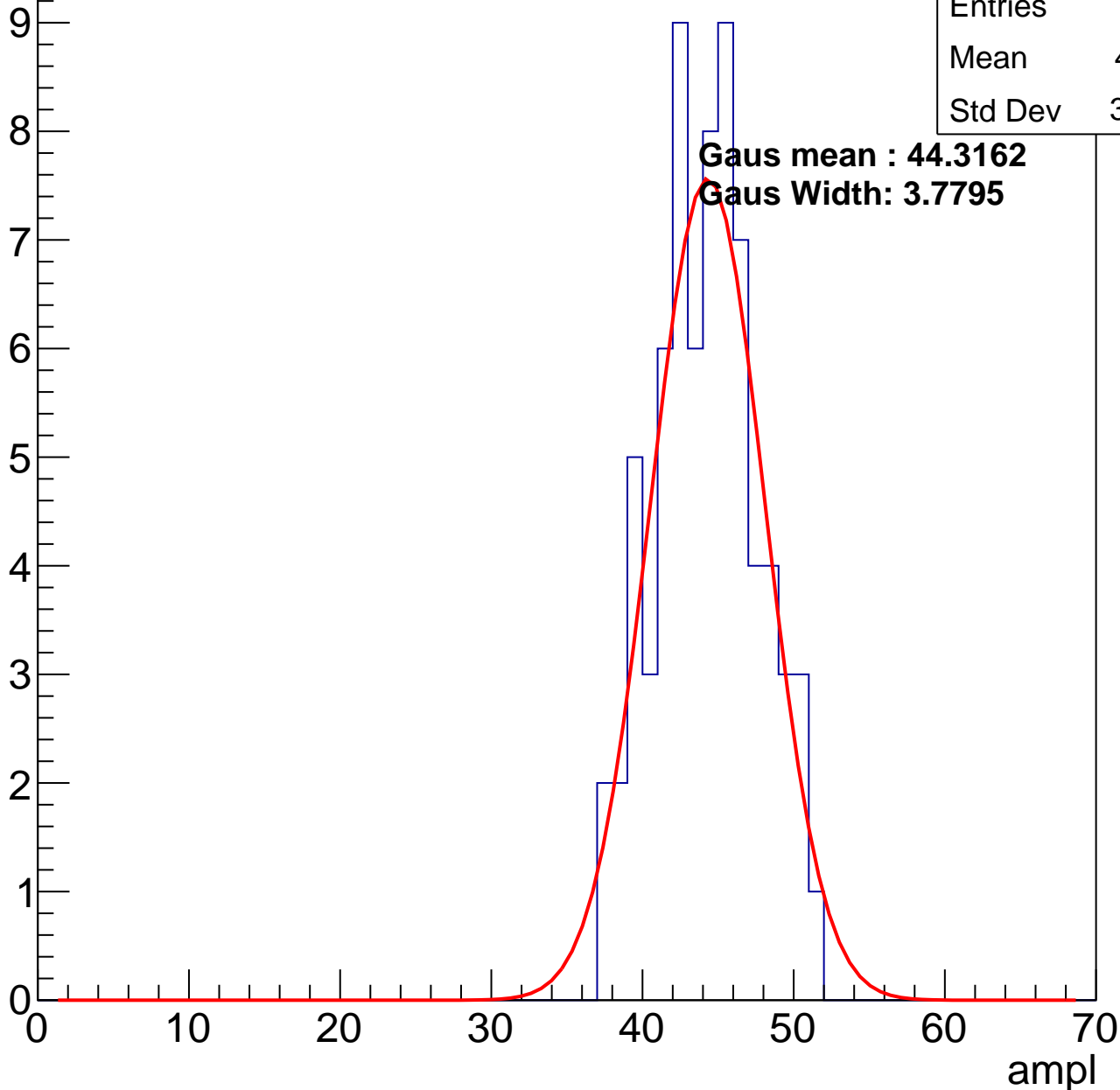
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	43.81
Std Dev	3.344

**Gaus mean : 44.3162**

**Gaus Width: 3.7795**

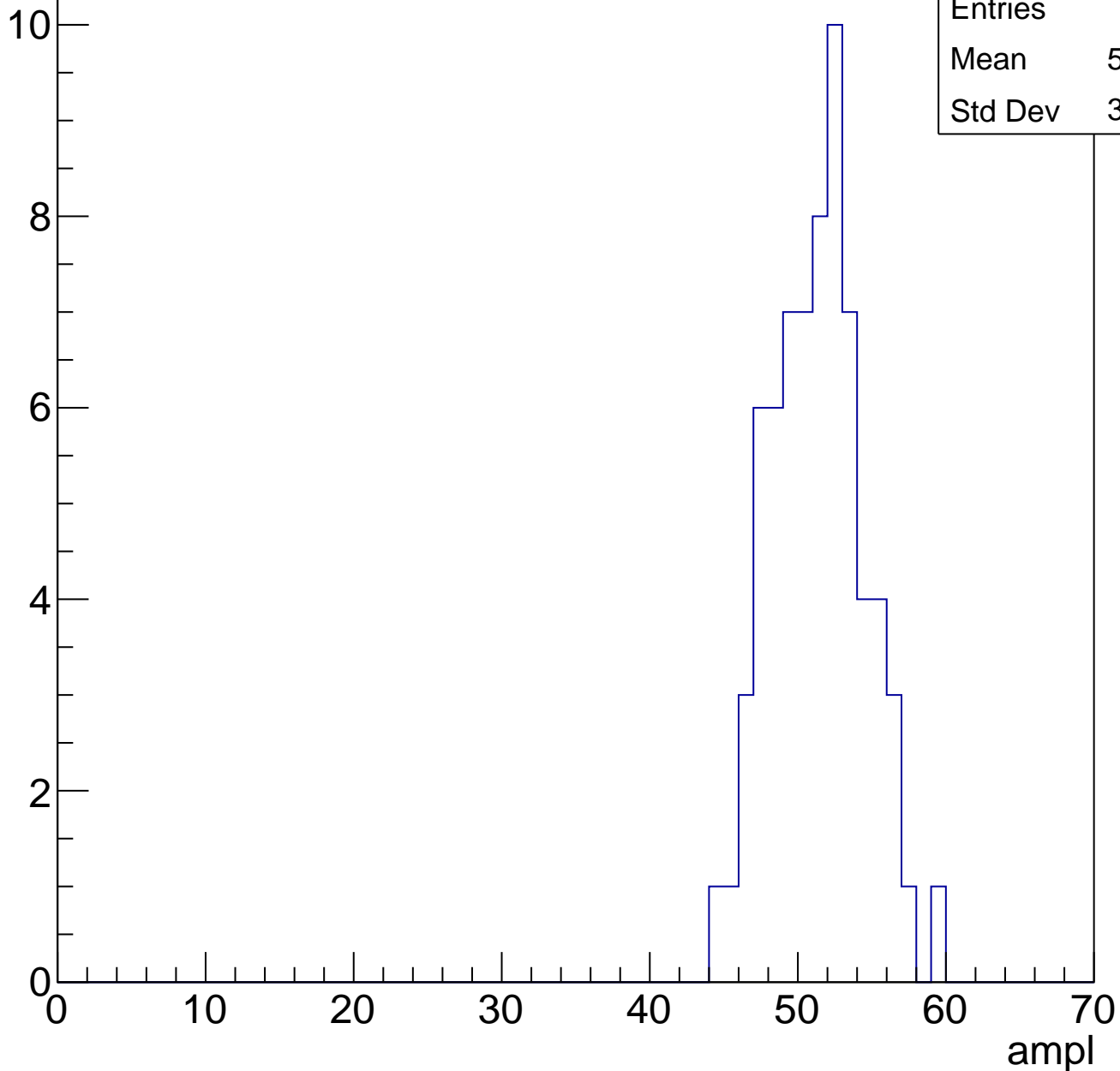


# B1L102S, U21-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	50.86
Std Dev	3.085

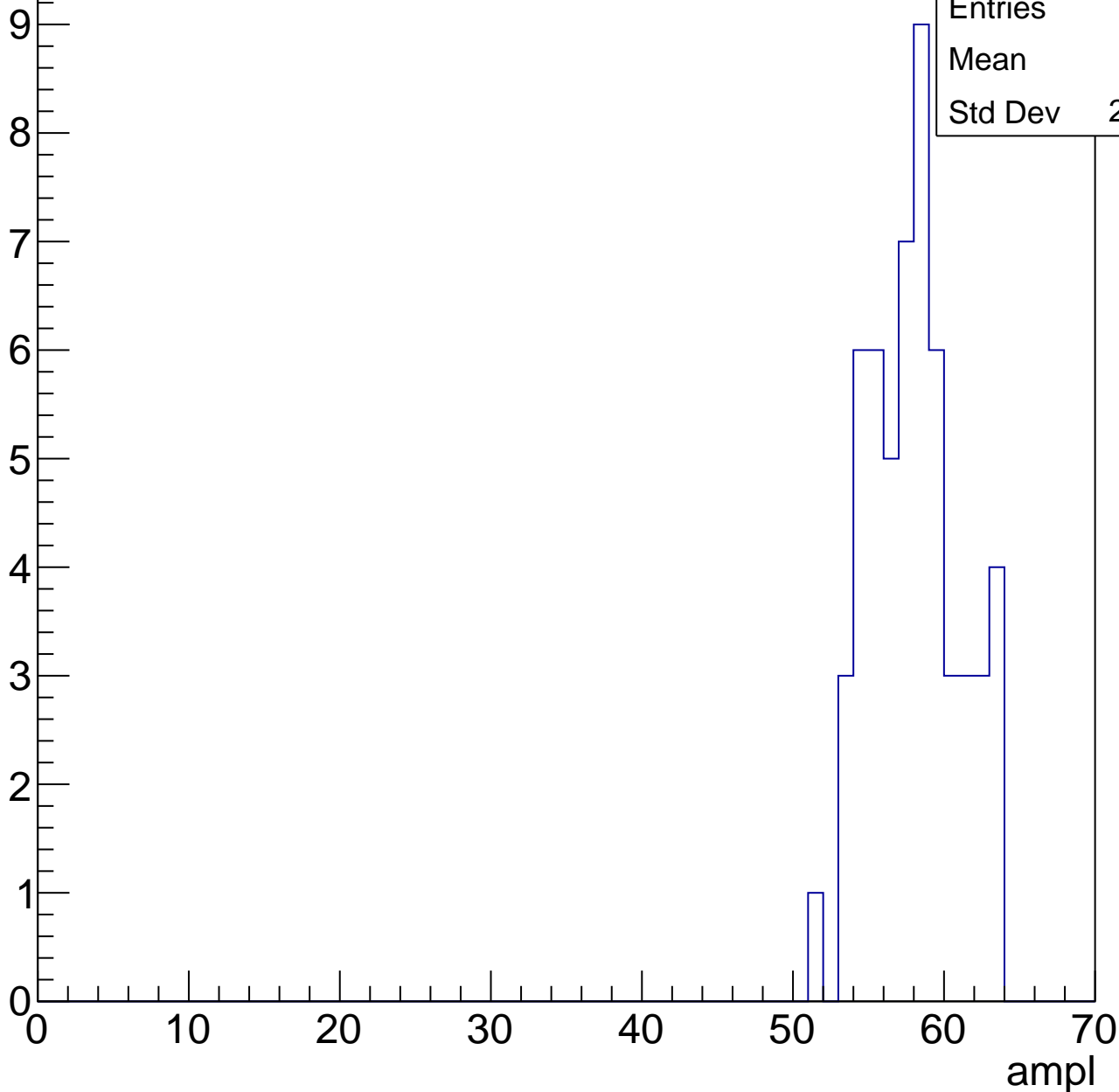


# B1L102S, U21-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	57.5
Std Dev	2.928

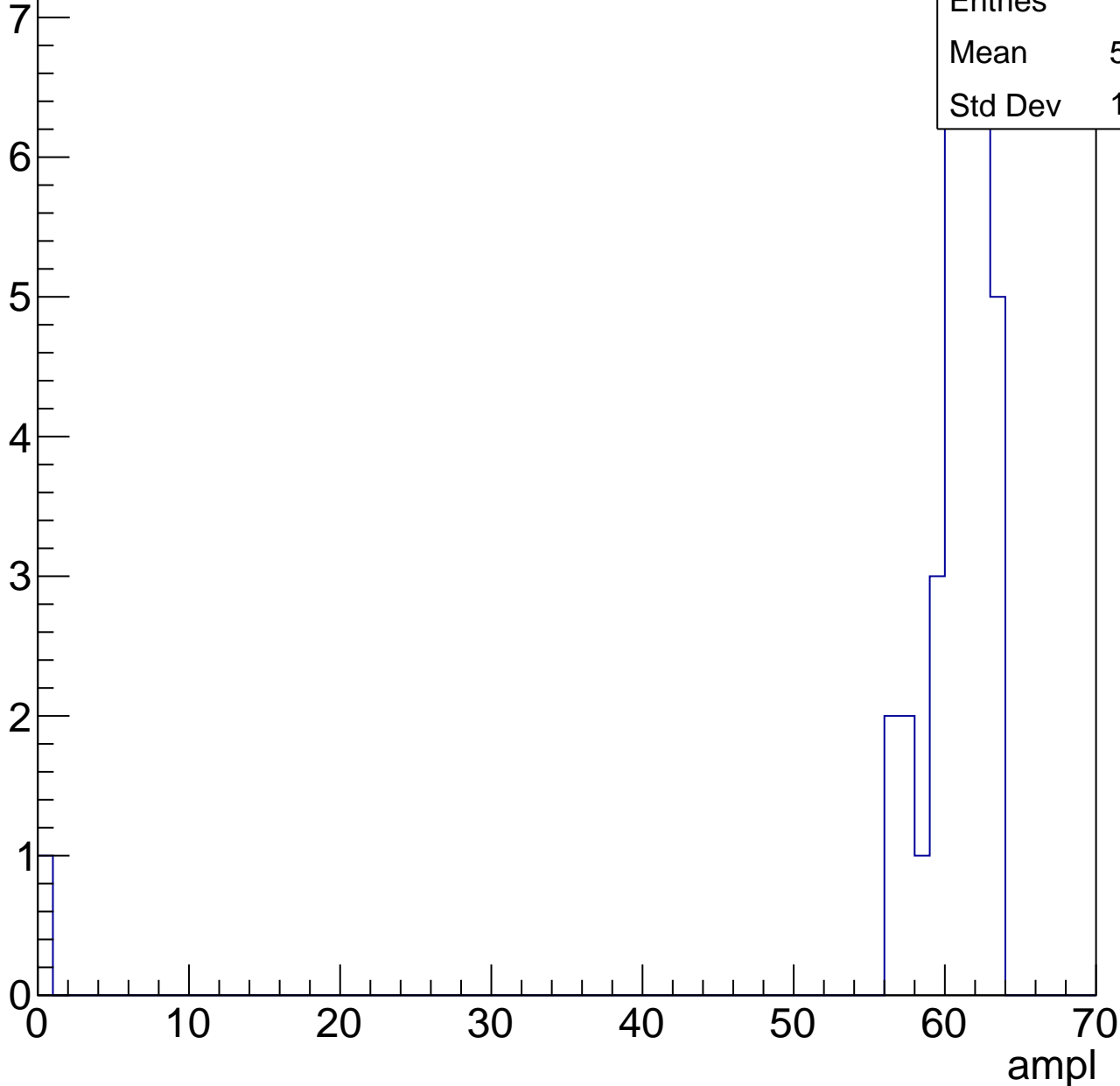


# B1L102S, U21-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	35
Mean	58.77
Std Dev	10.26



# B1L102S, U21-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch26, adc0

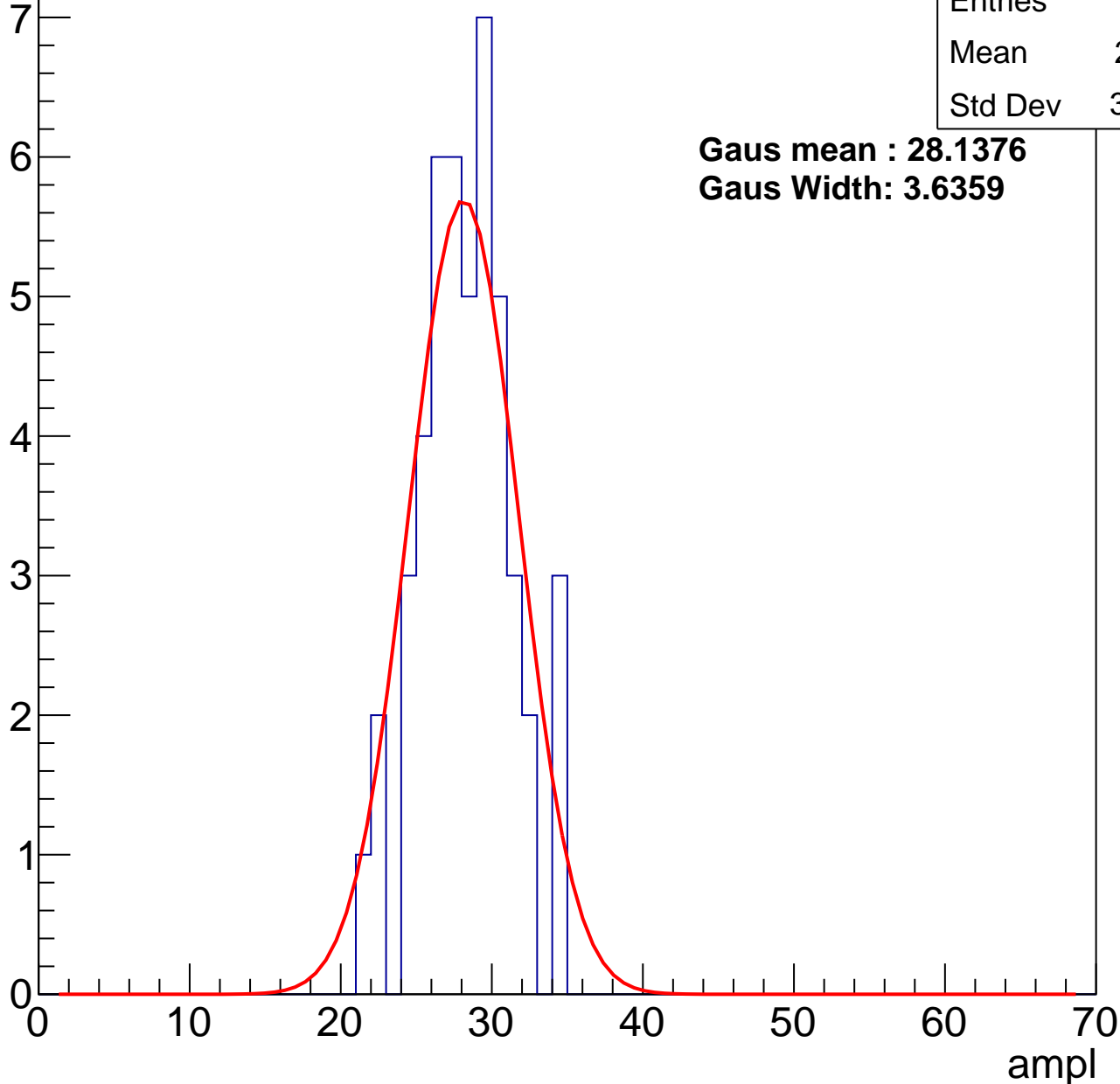
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	27.81
Std Dev	3.015

**Gaus mean : 28.1376**

**Gaus Width: 3.6359**



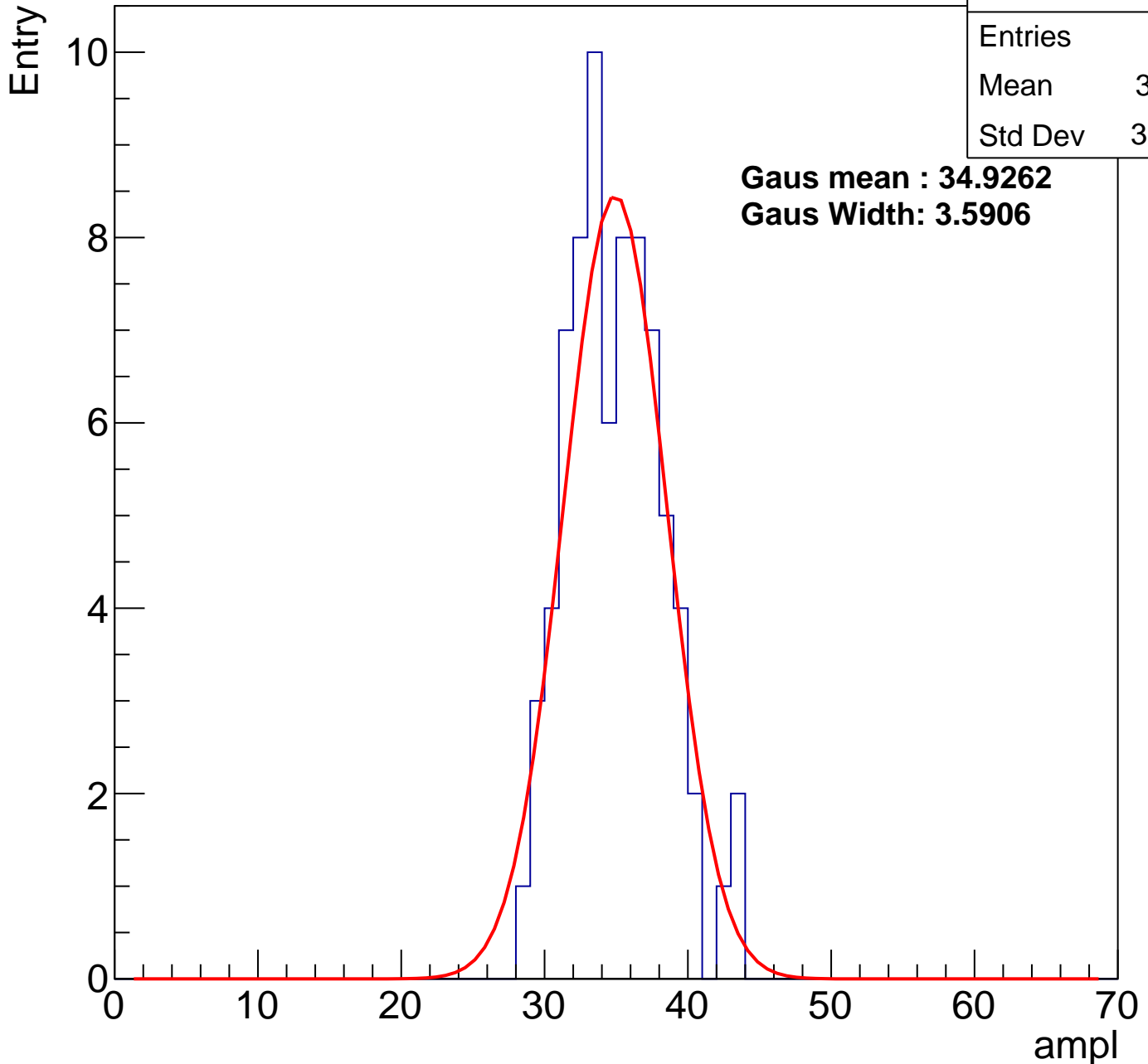
# B1L102S, U21-ch26, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	76
Mean	34.51
Std Dev	3.327

**Gaus mean : 34.9262**

**Gaus Width: 3.5906**



# B1L102S, U21-ch26, adc2

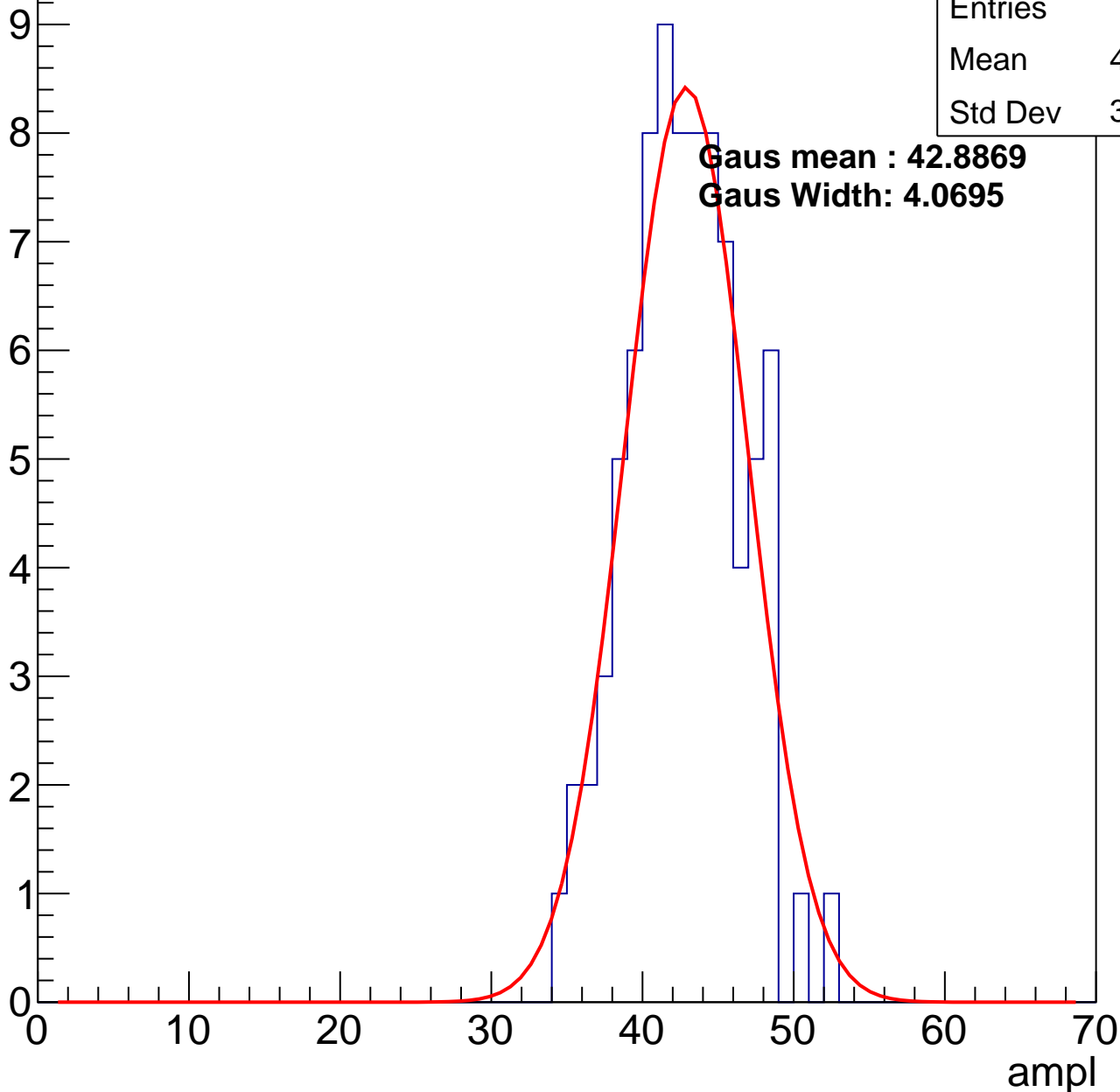
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	42.33
Std Dev	3.695

**Gaus mean : 42.8869**

**Gaus Width: 4.0695**

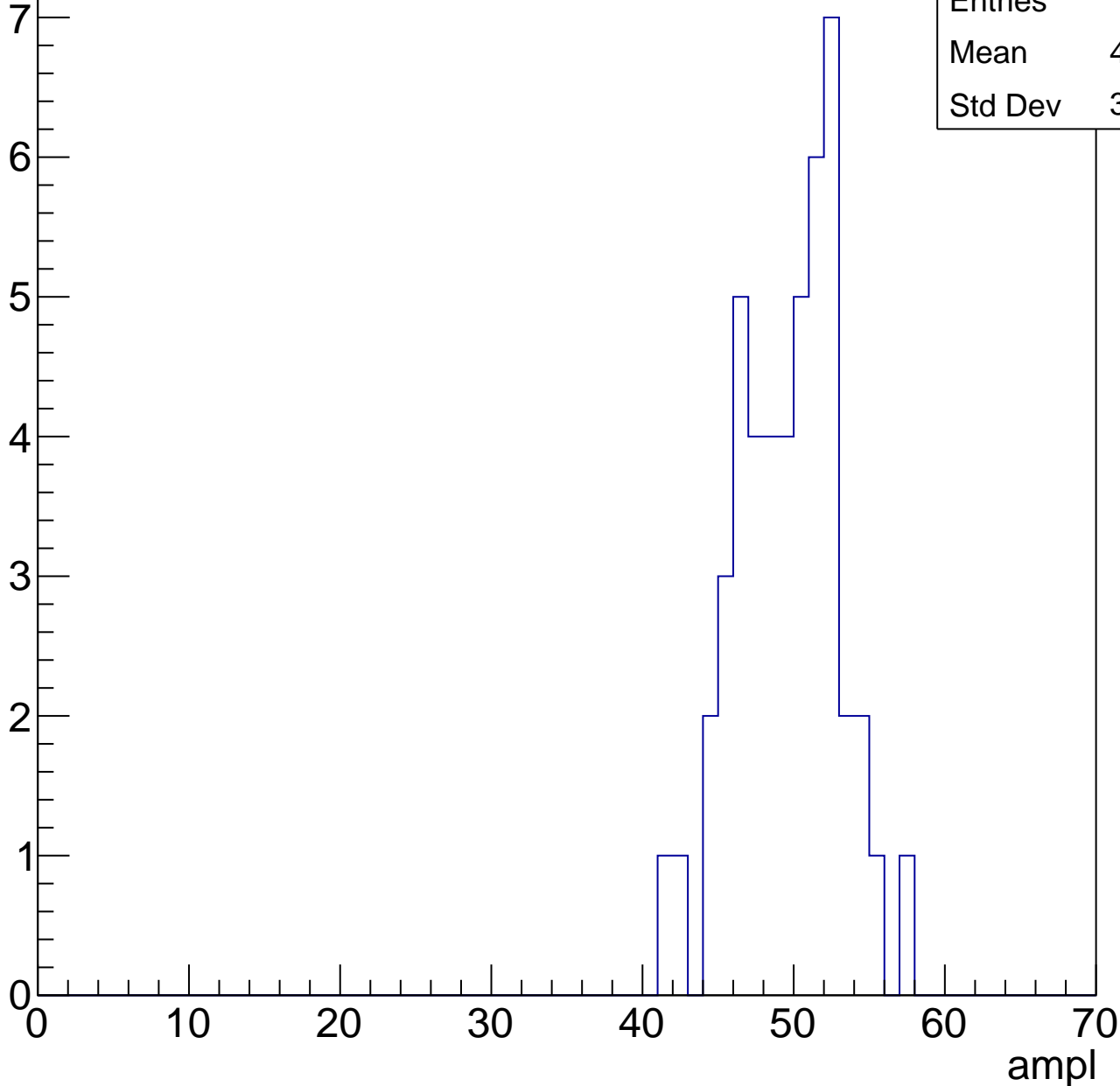


# B1L102S, U21-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	49.12
Std Dev	3.383

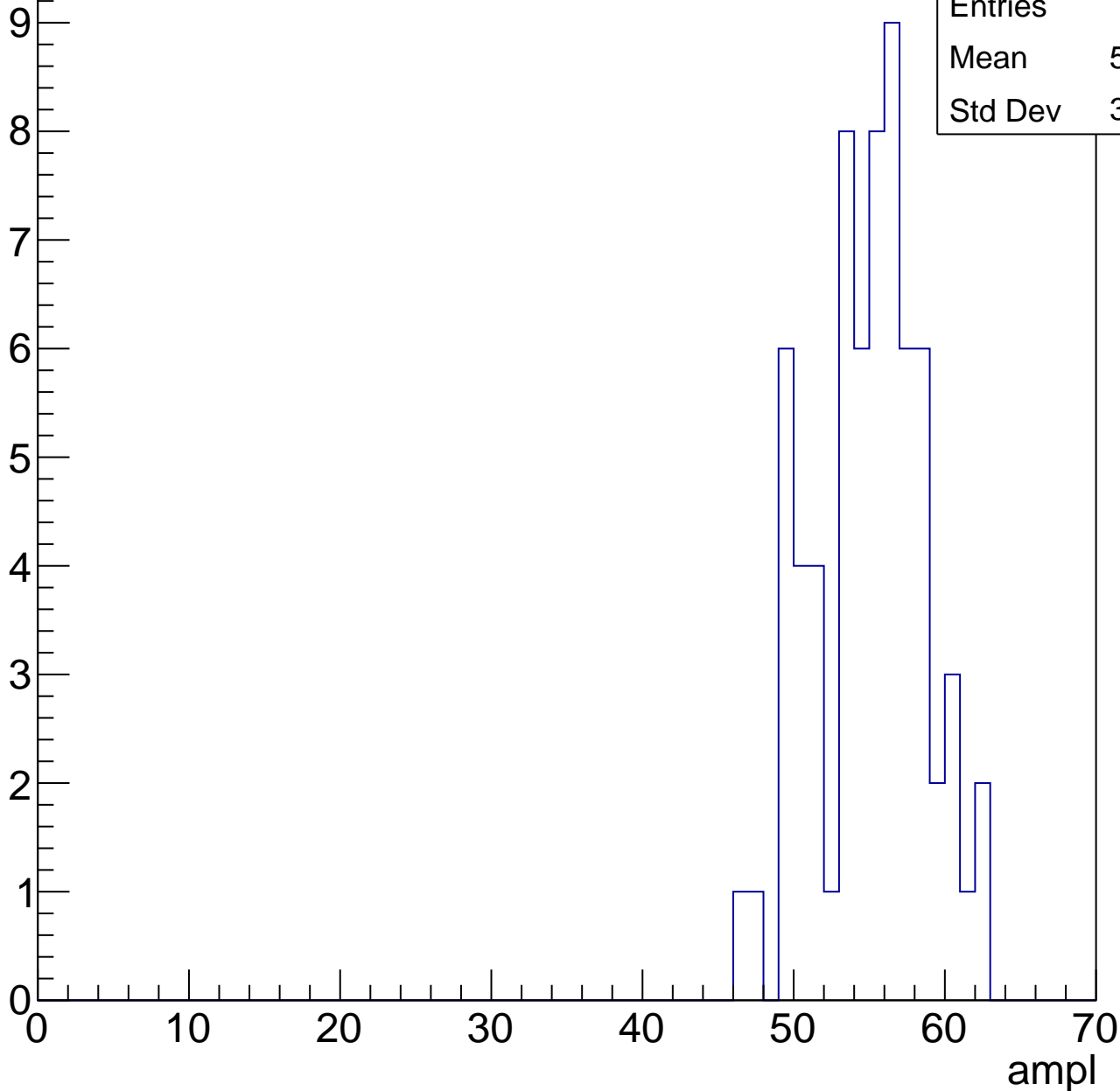


# B1L102S, U21-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	54.53
Std Dev	3.607

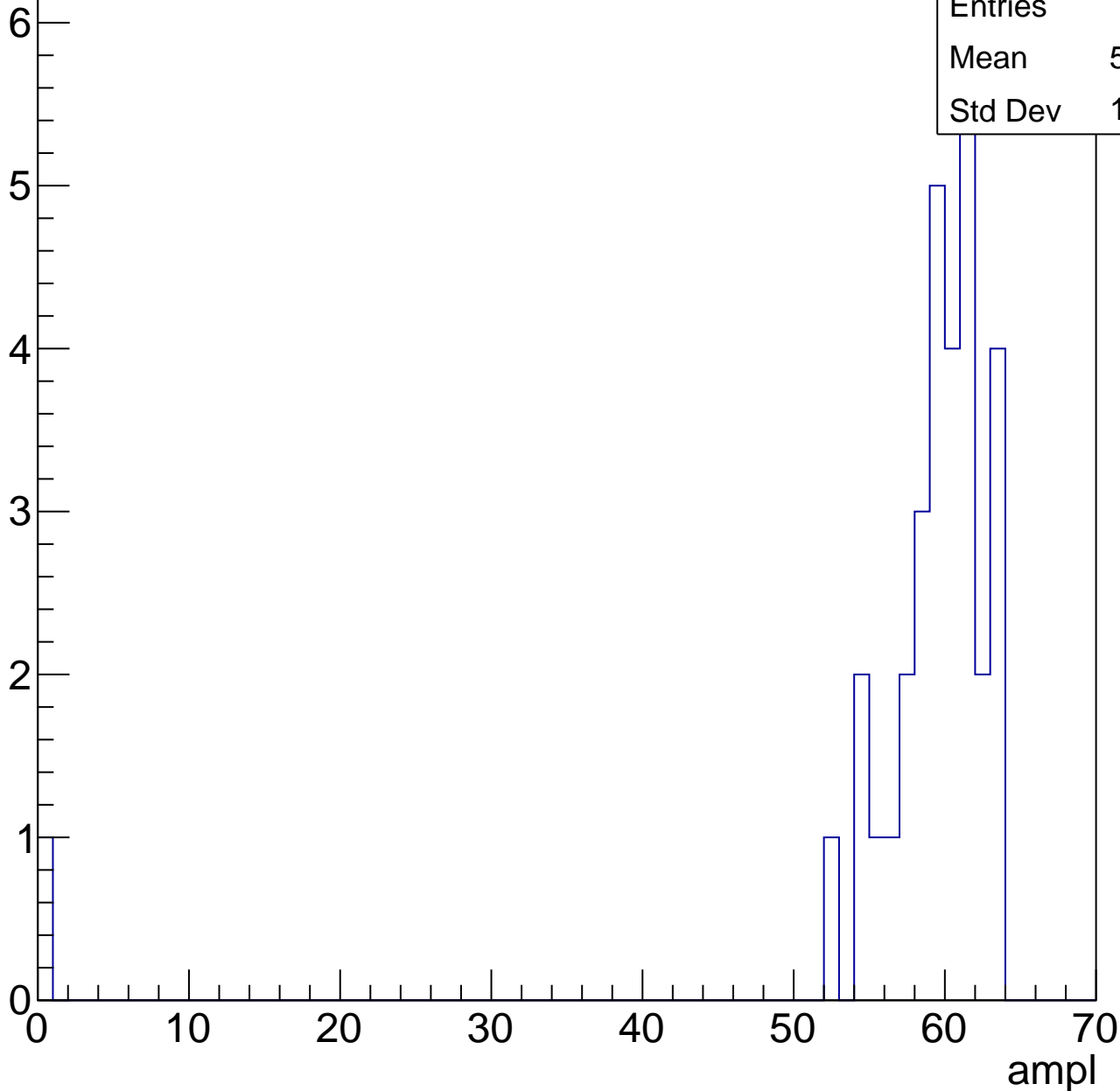


# B1L102S, U21-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

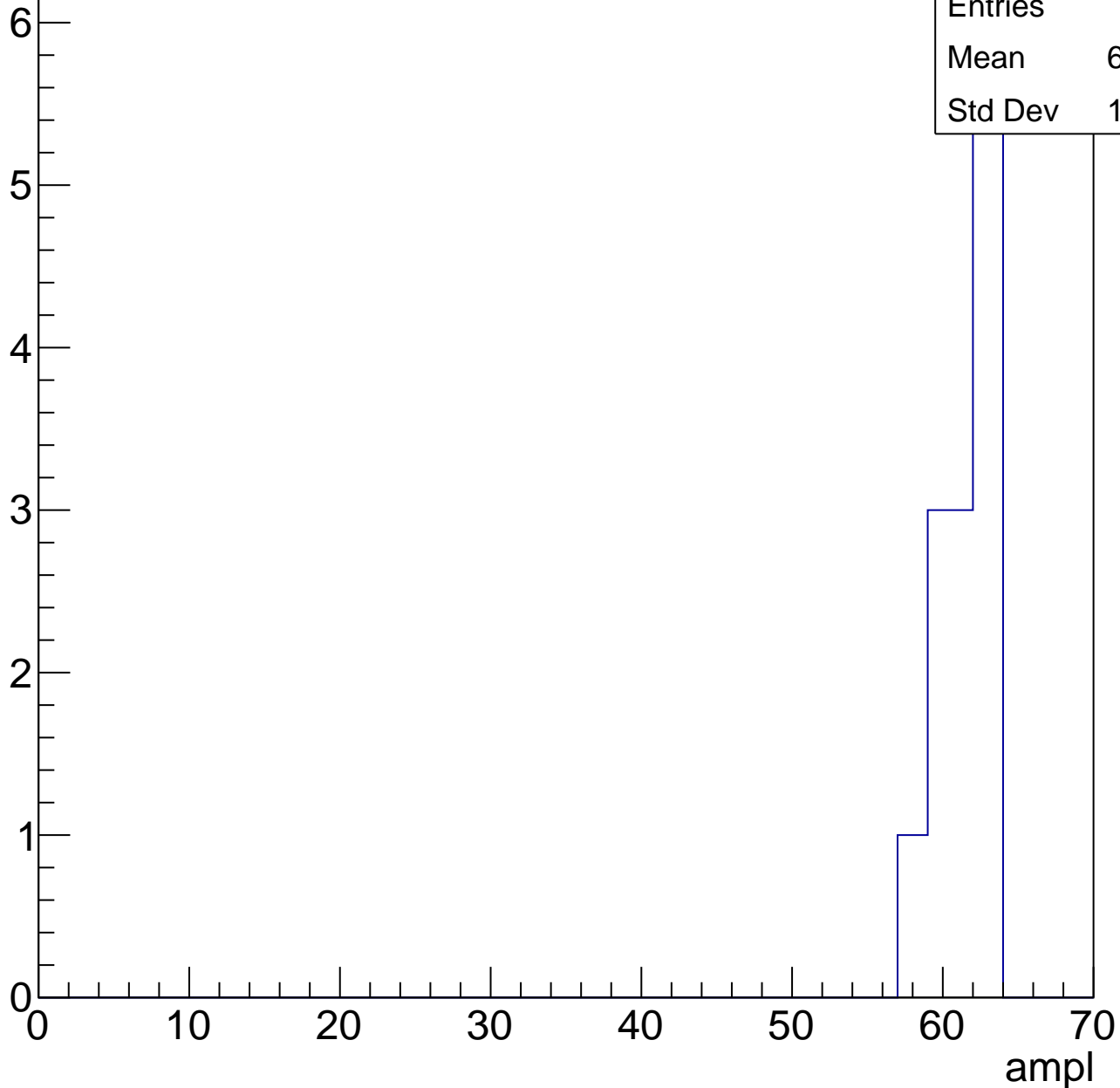
Entries	32
Mean	57.38
Std Dev	10.67



# B1L102S, U21-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch27, adc0

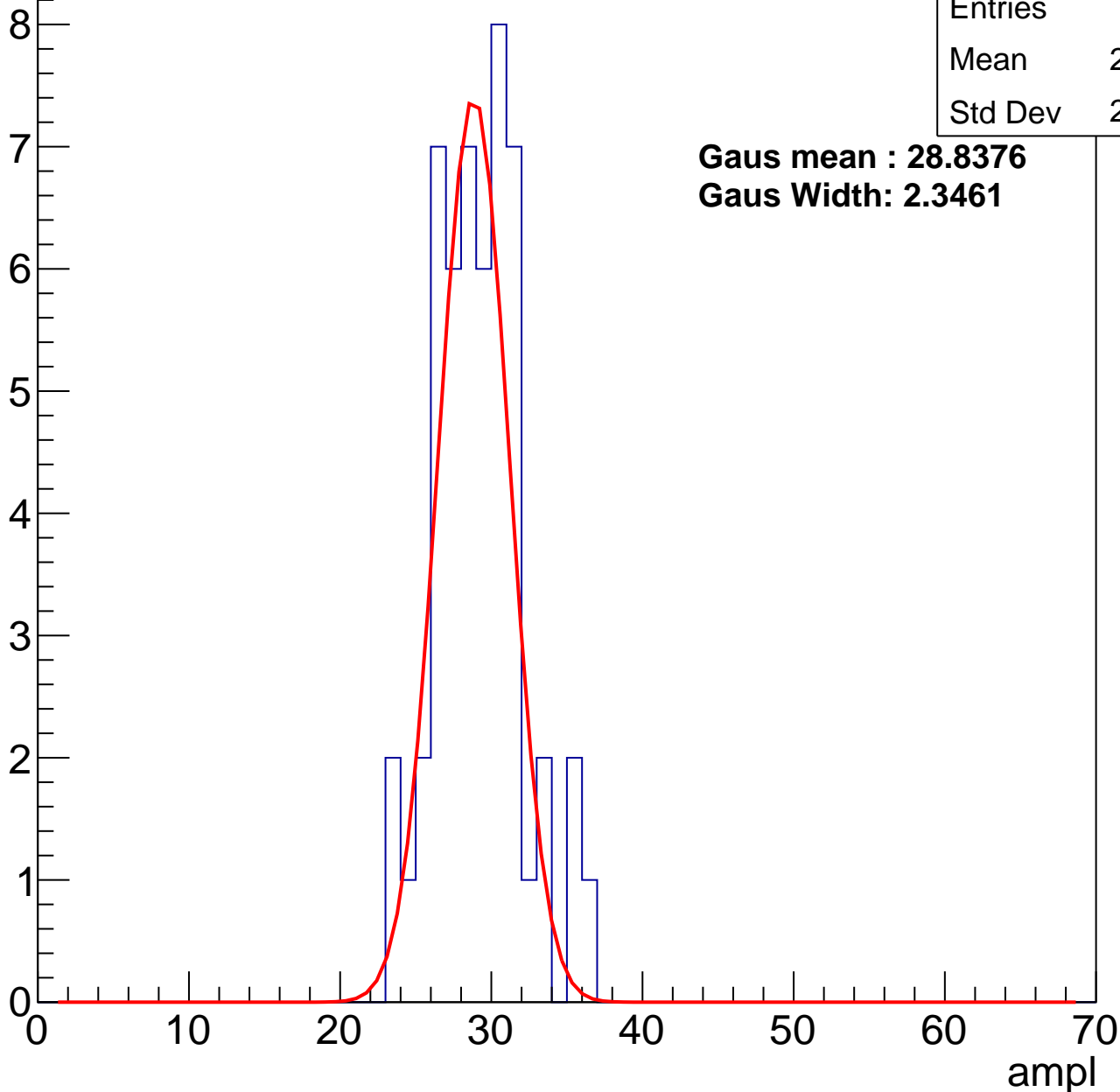
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	28.75
Std Dev	2.834

**Gaus mean : 28.8376**

**Gaus Width: 2.3461**



# B1L102S, U21-ch27, adc1

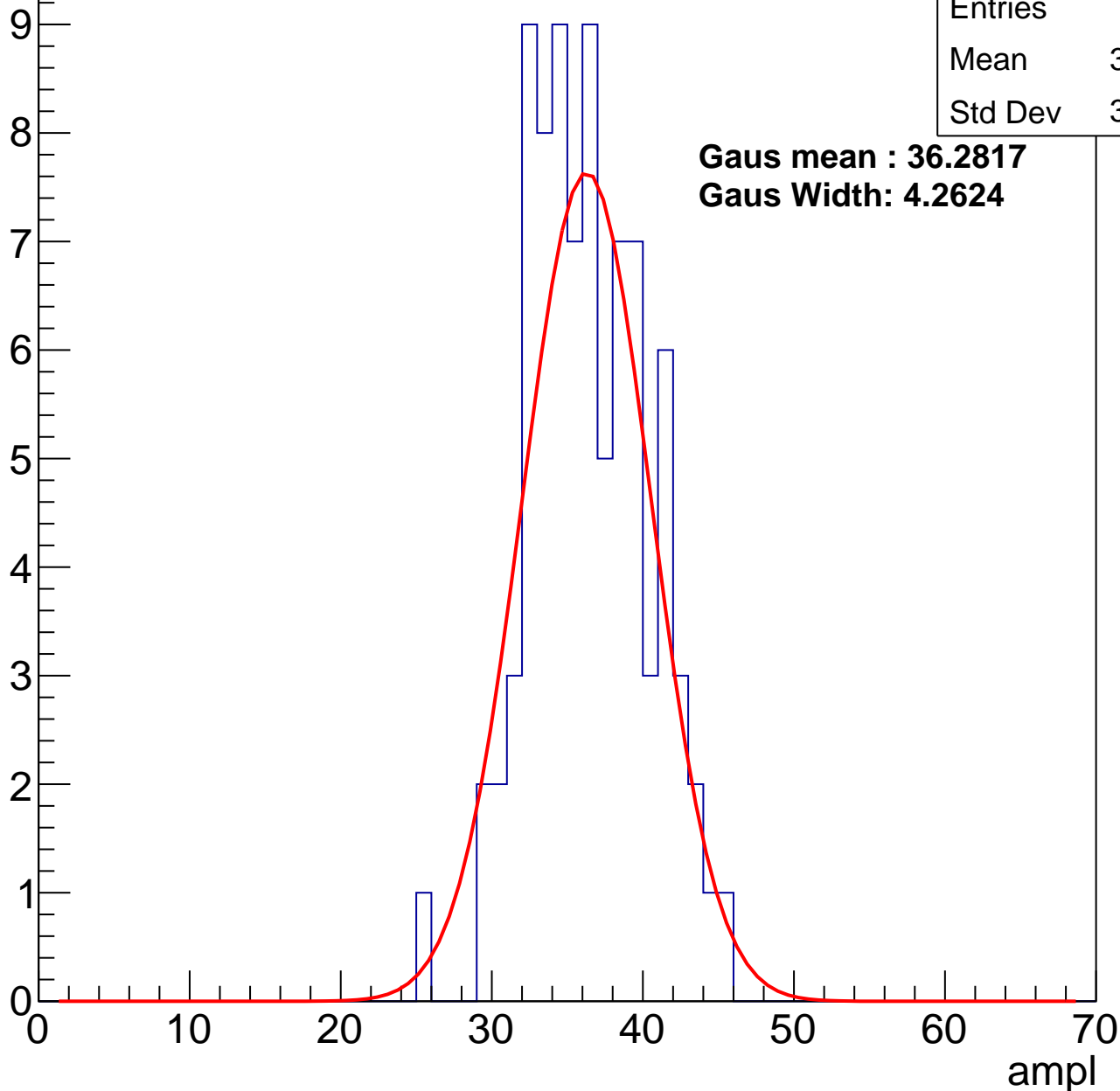
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	85
Mean	35.93
Std Dev	3.865

**Gaus mean : 36.2817**

**Gaus Width: 4.2624**



# B1L102S, U21-ch27, adc2

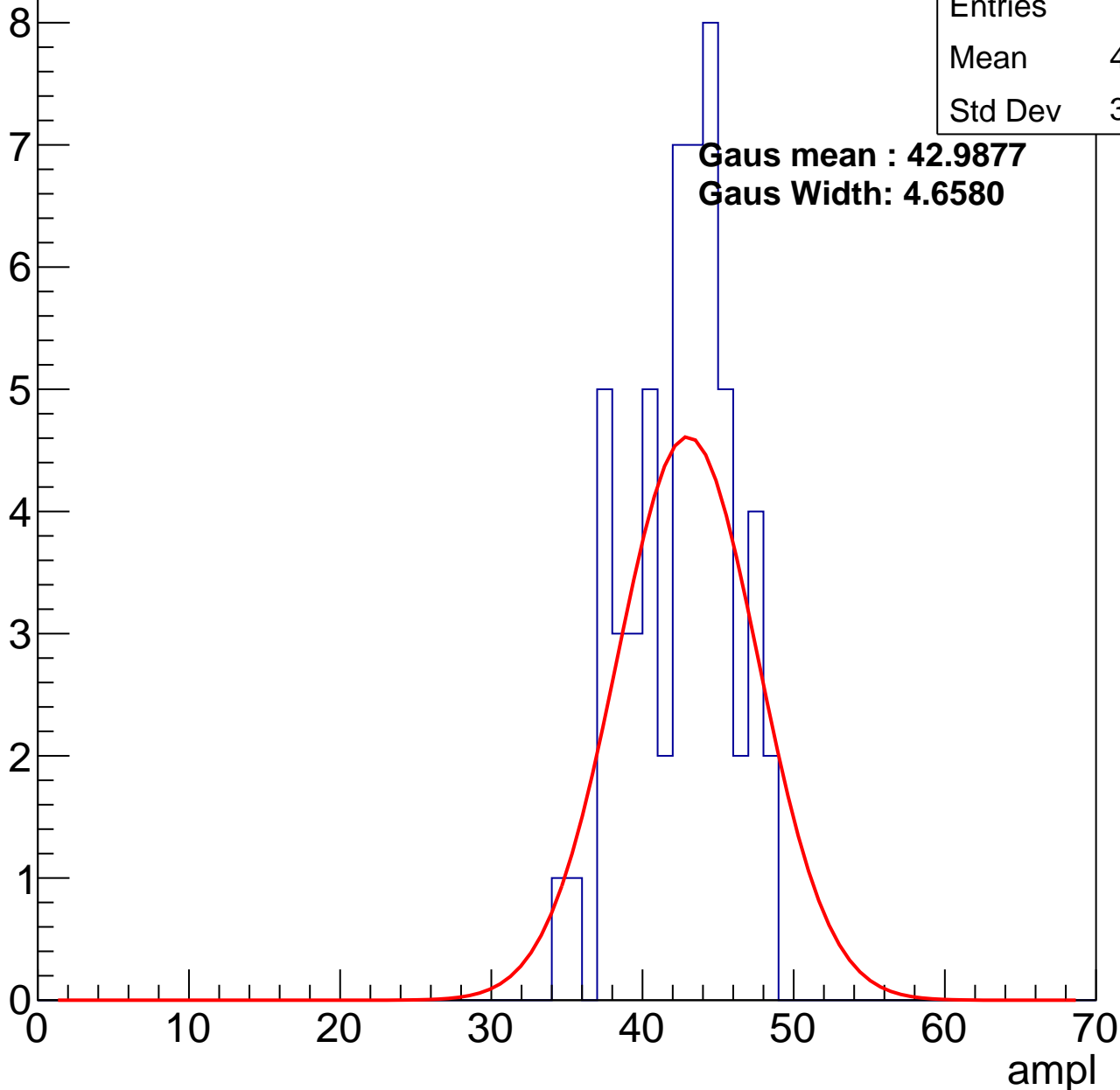
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	42.09
Std Dev	3.364

**Gaus mean : 42.9877**

**Gaus Width: 4.6580**



# B1L102S, U21-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	79
Mean	49.33
Std Dev	3.737

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

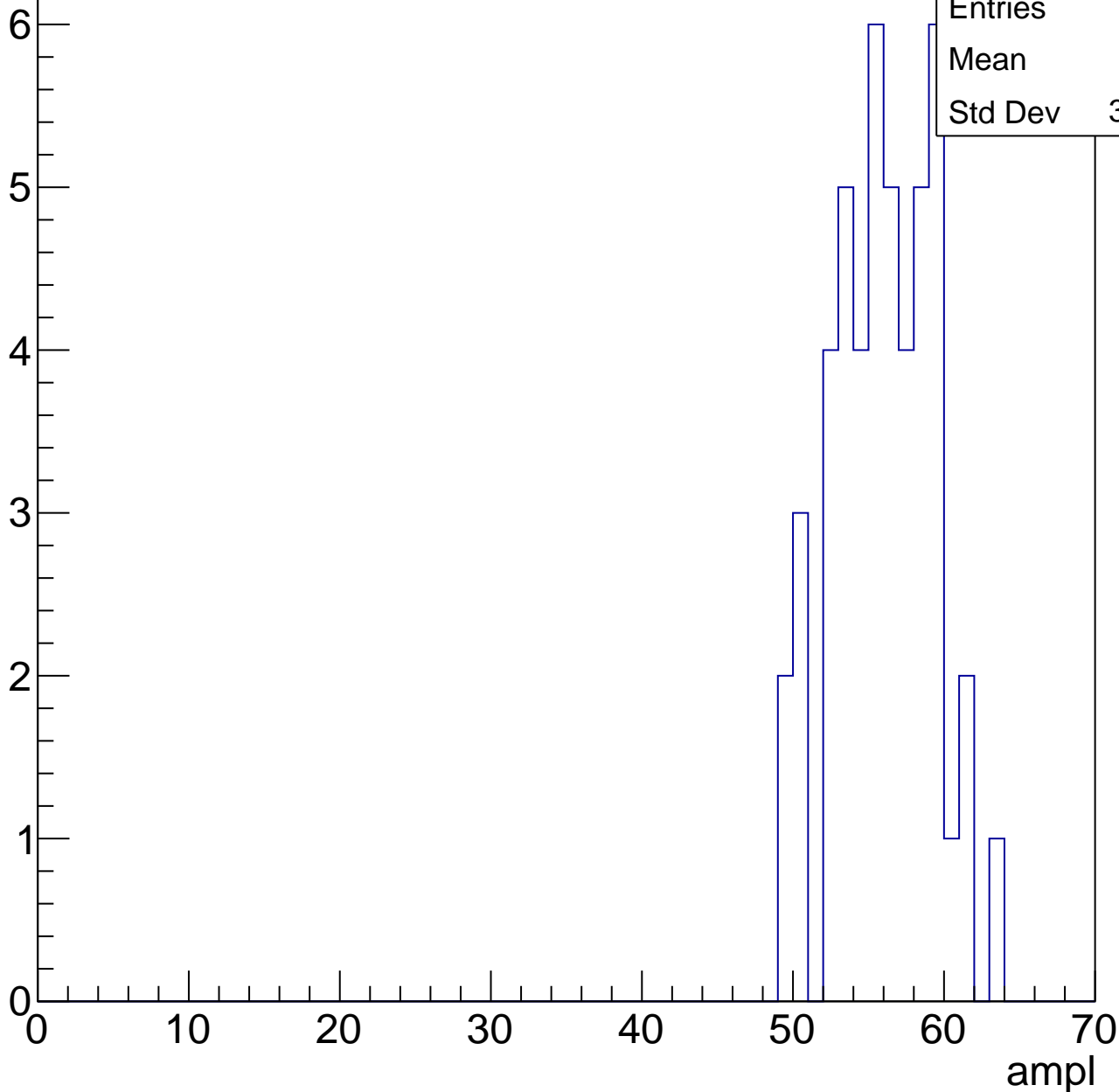
70

# B1L102S, U21-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	55.5
Std Dev	3.285

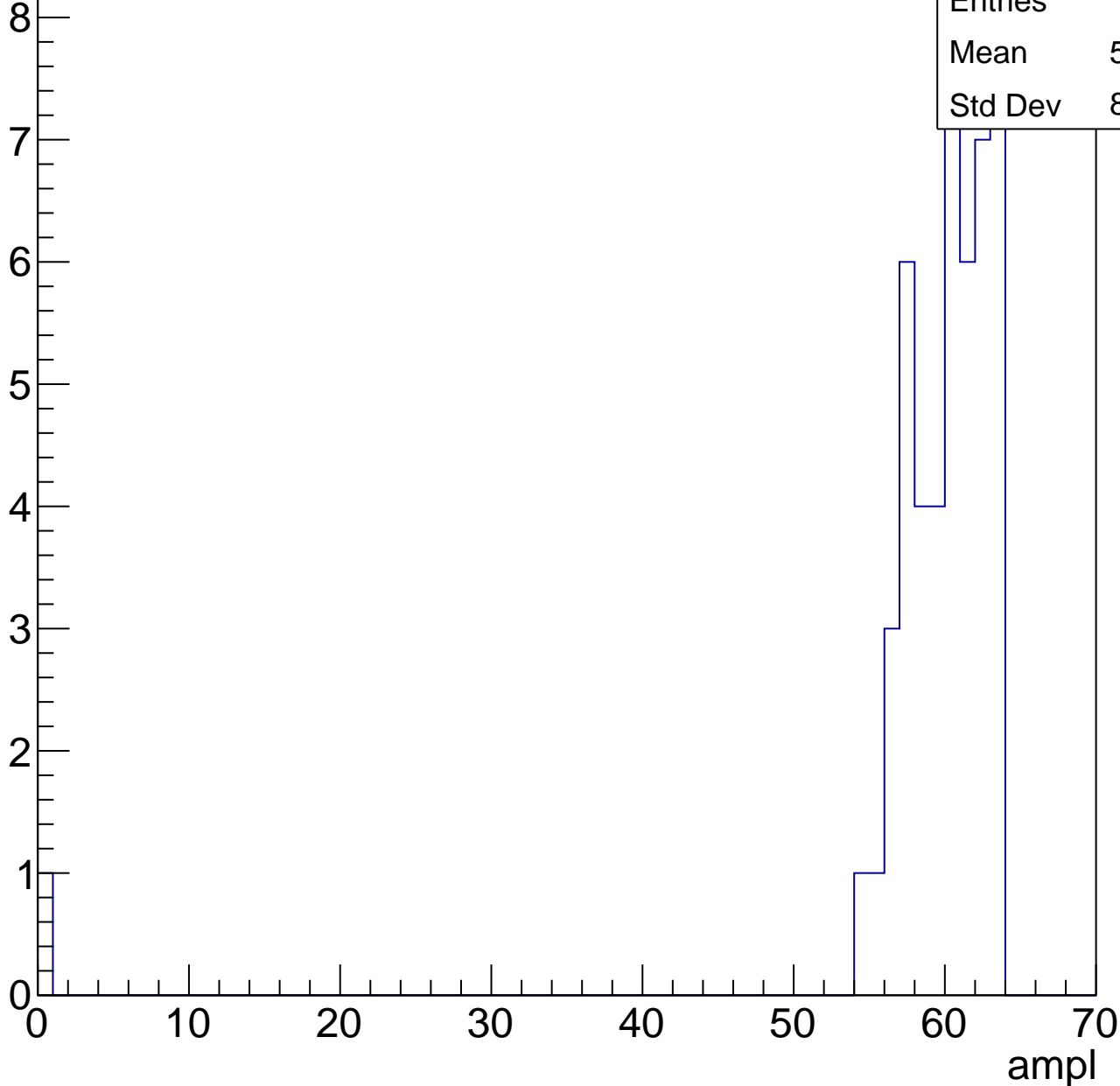


# B1L102S, U21-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

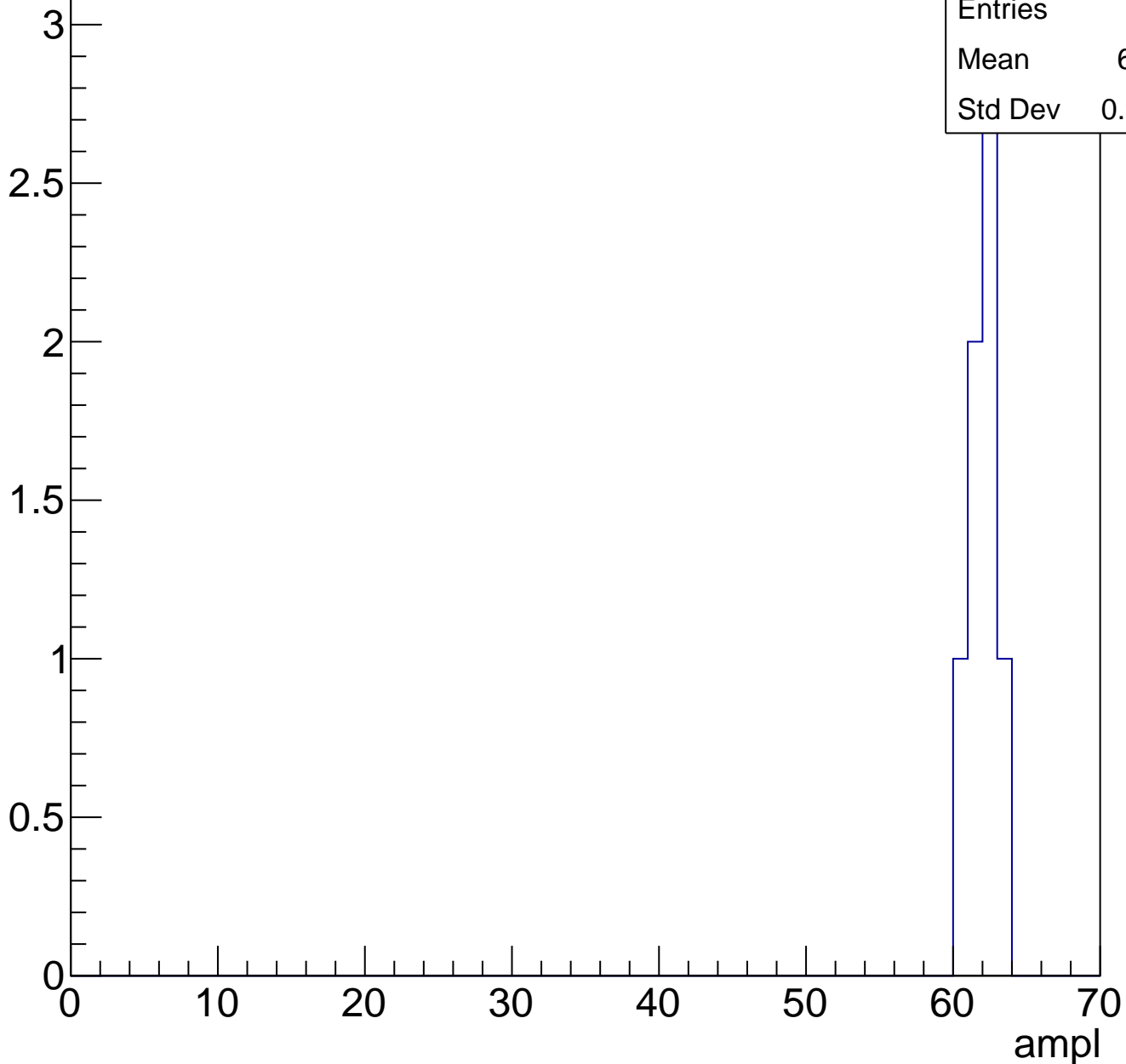
Entries	49
Mean	58.59
Std Dev	8.797



# B1L102S, U21-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

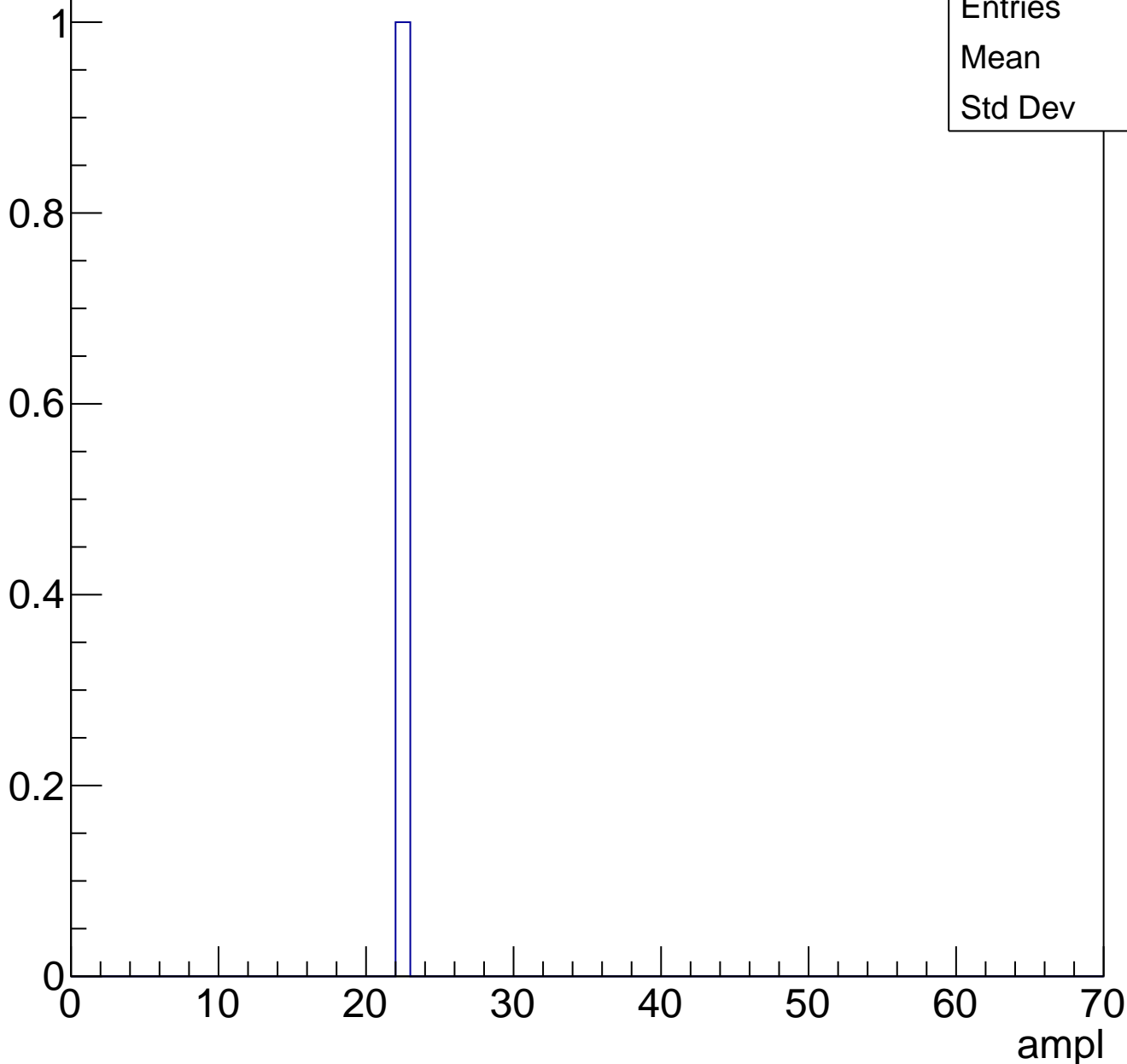




# B1L102S, U21-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



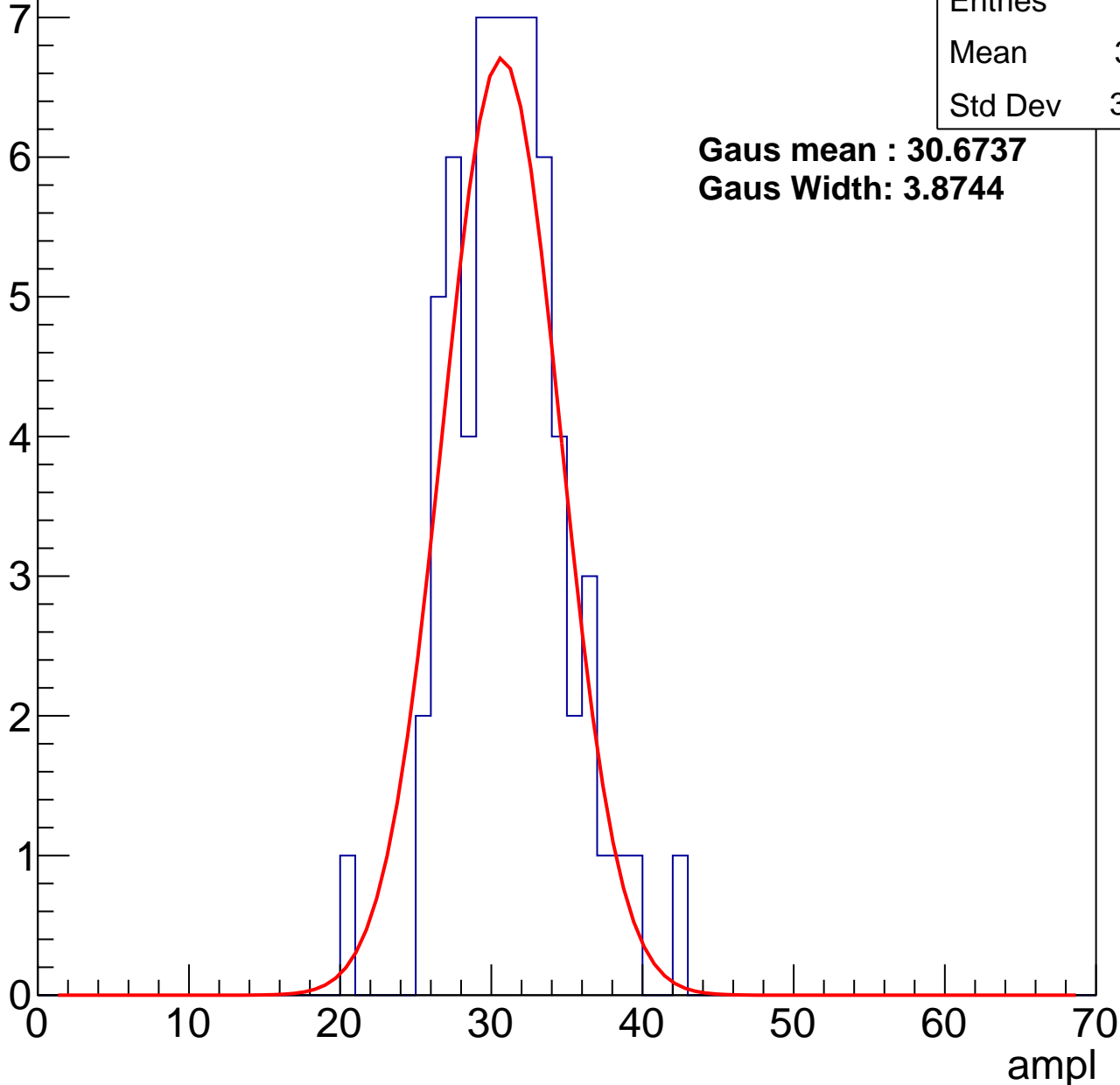
# B1L102S, U21-ch28, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	30.71
Std Dev	3.769

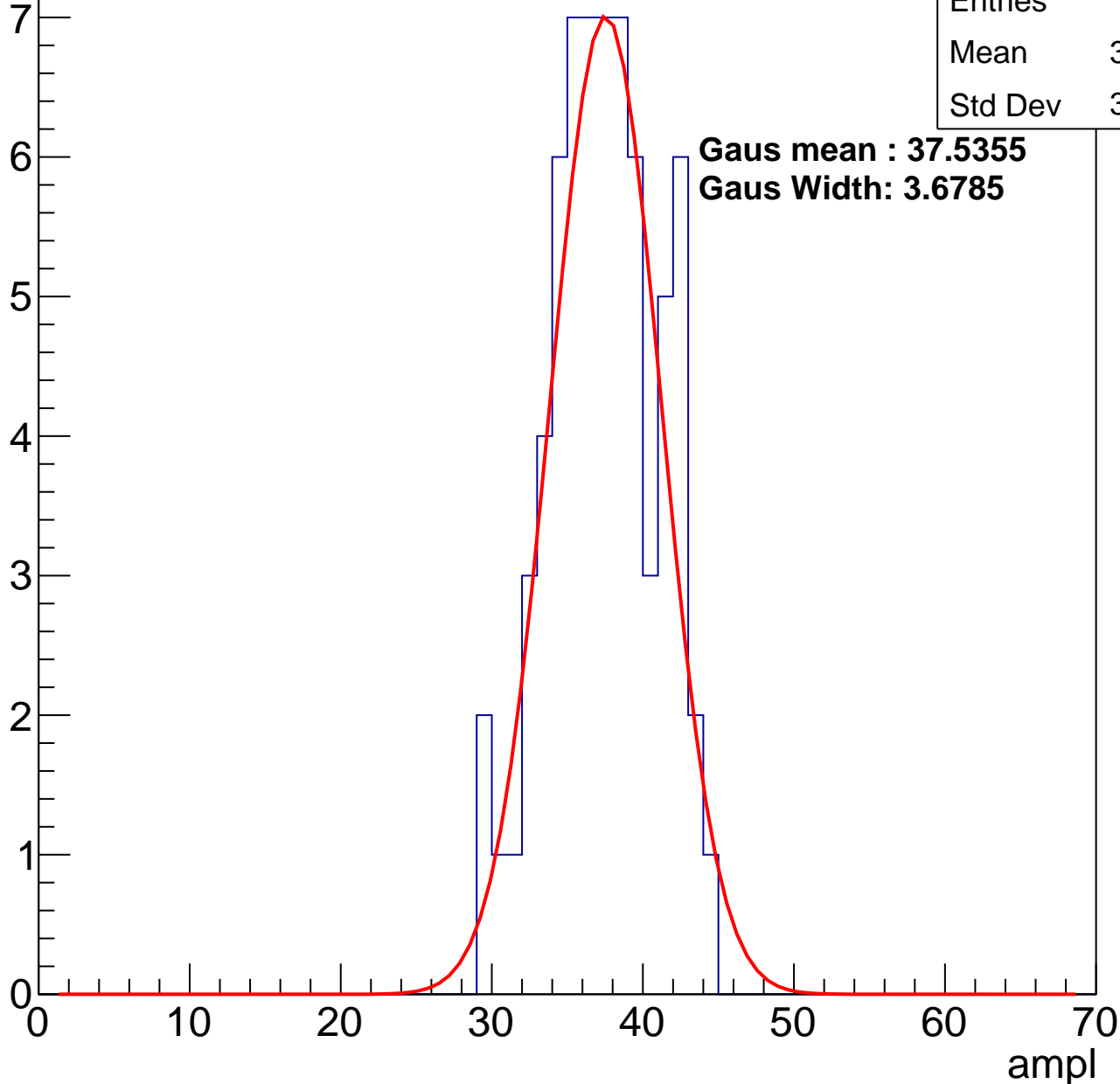
**Gaus mean : 30.6737**  
**Gaus Width: 3.8744**



# B1L102S, U21-ch28, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch28, adc2

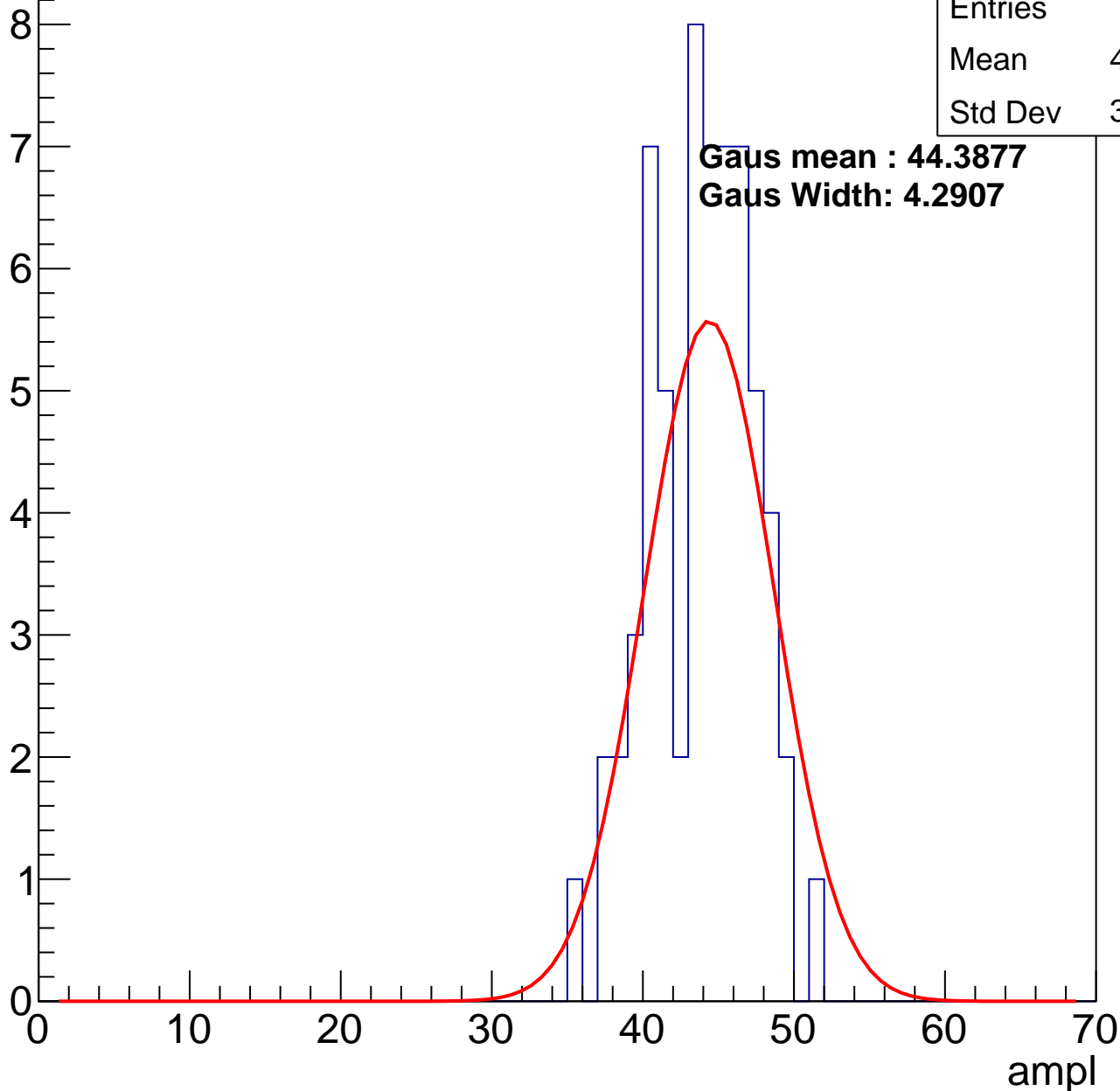
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	43.43
Std Dev	3.384

**Gaus mean : 44.3877**

**Gaus Width: 4.2907**



# B1L102S, U21-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

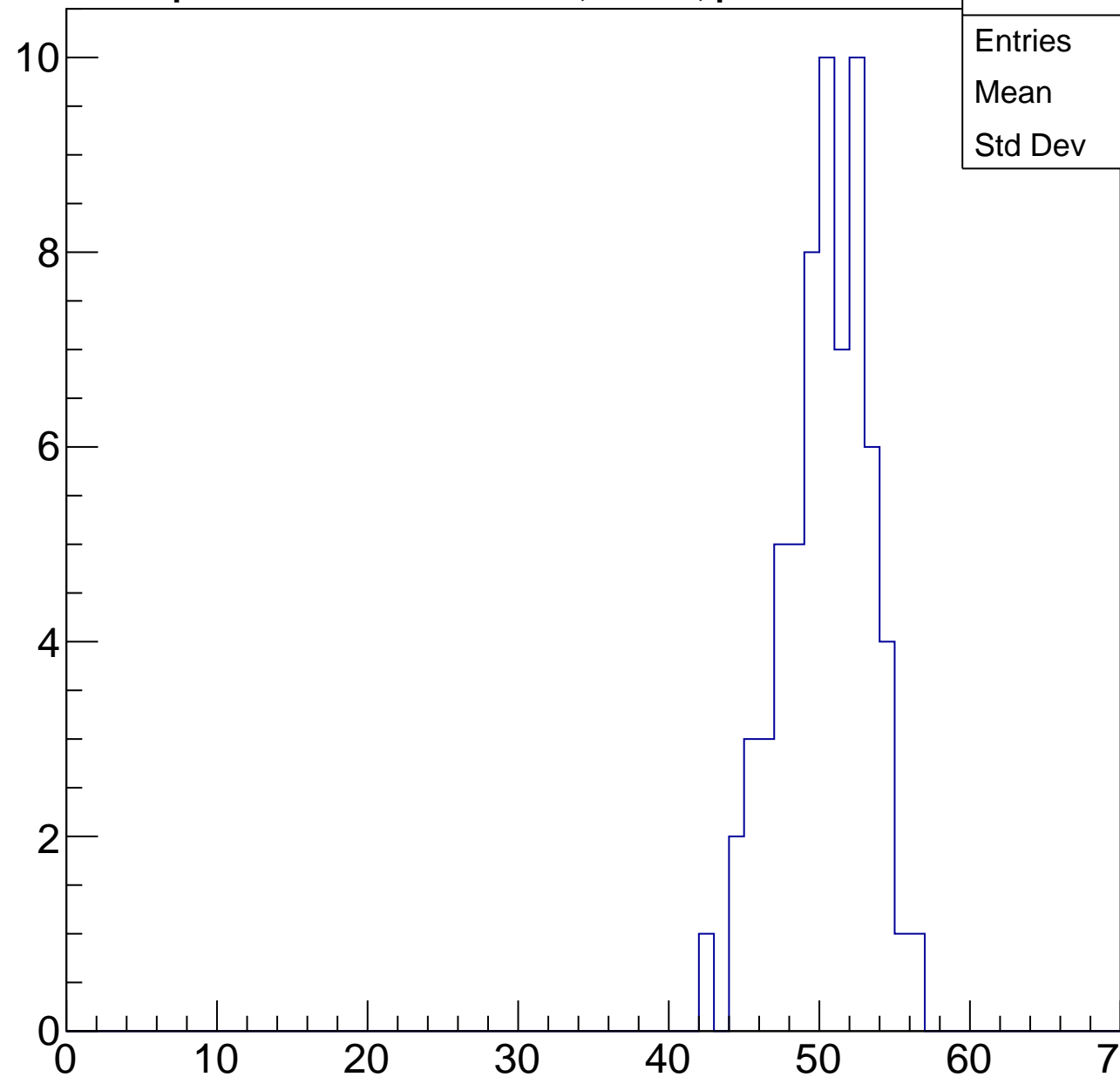
Entries	66
Mean	49.88
Std Dev	2.905

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

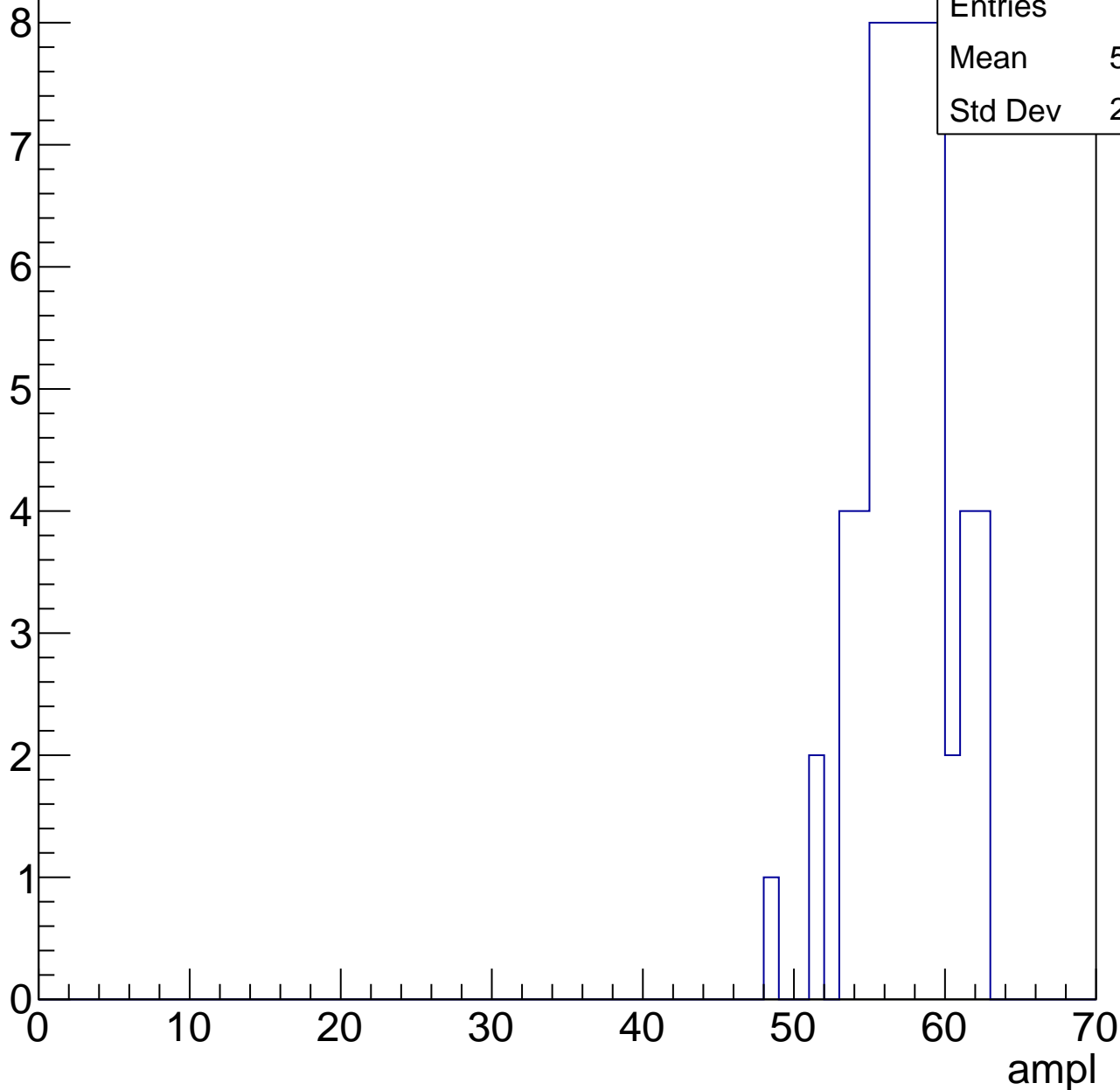


# B1L102S, U21-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	56.89
Std Dev	2.903



# B1L102S, U21-ch28, adc5

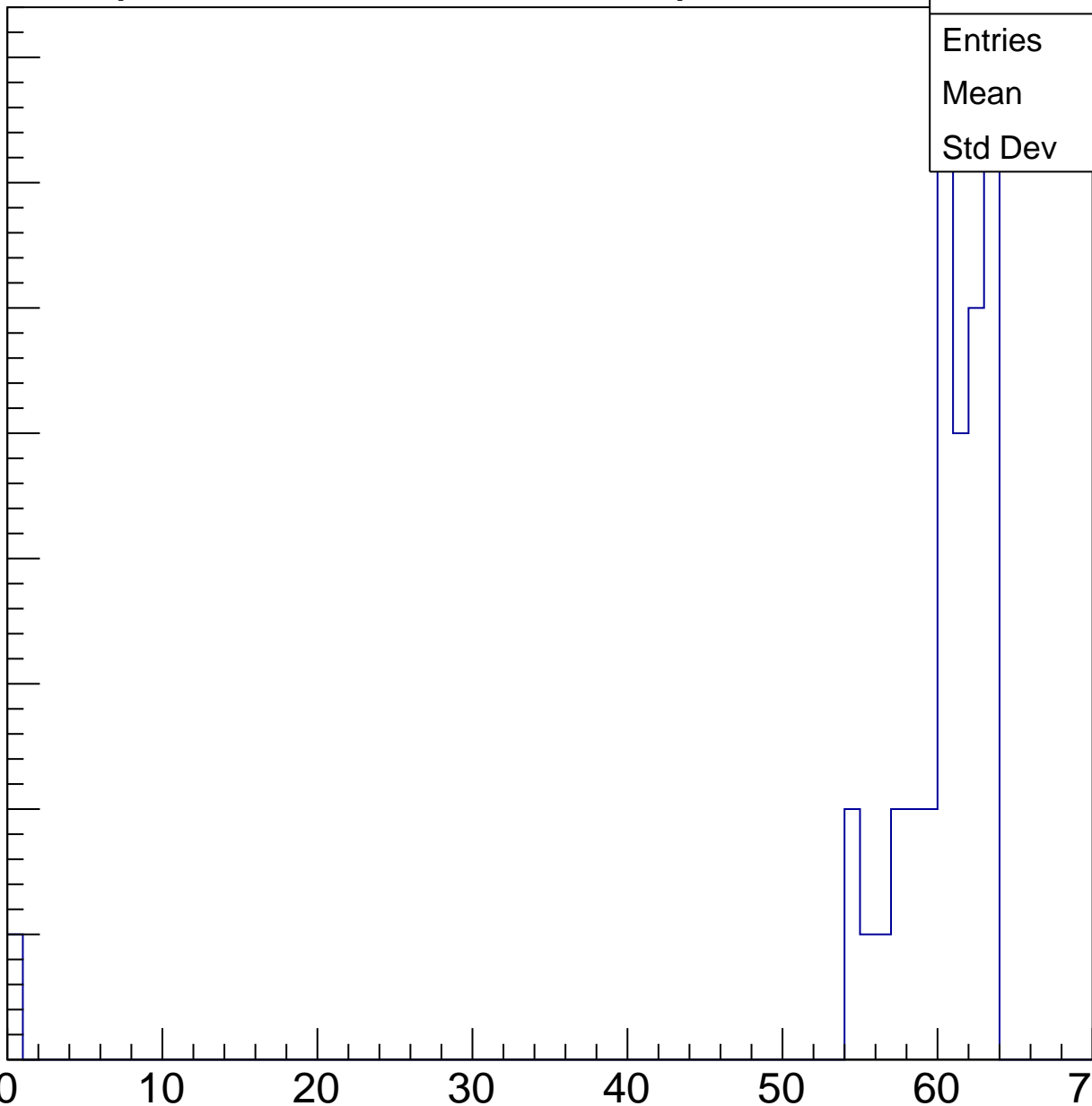
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	38
Mean	58.63
Std Dev	9.962

ampl



# B1L102S, U21-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch29, adc0

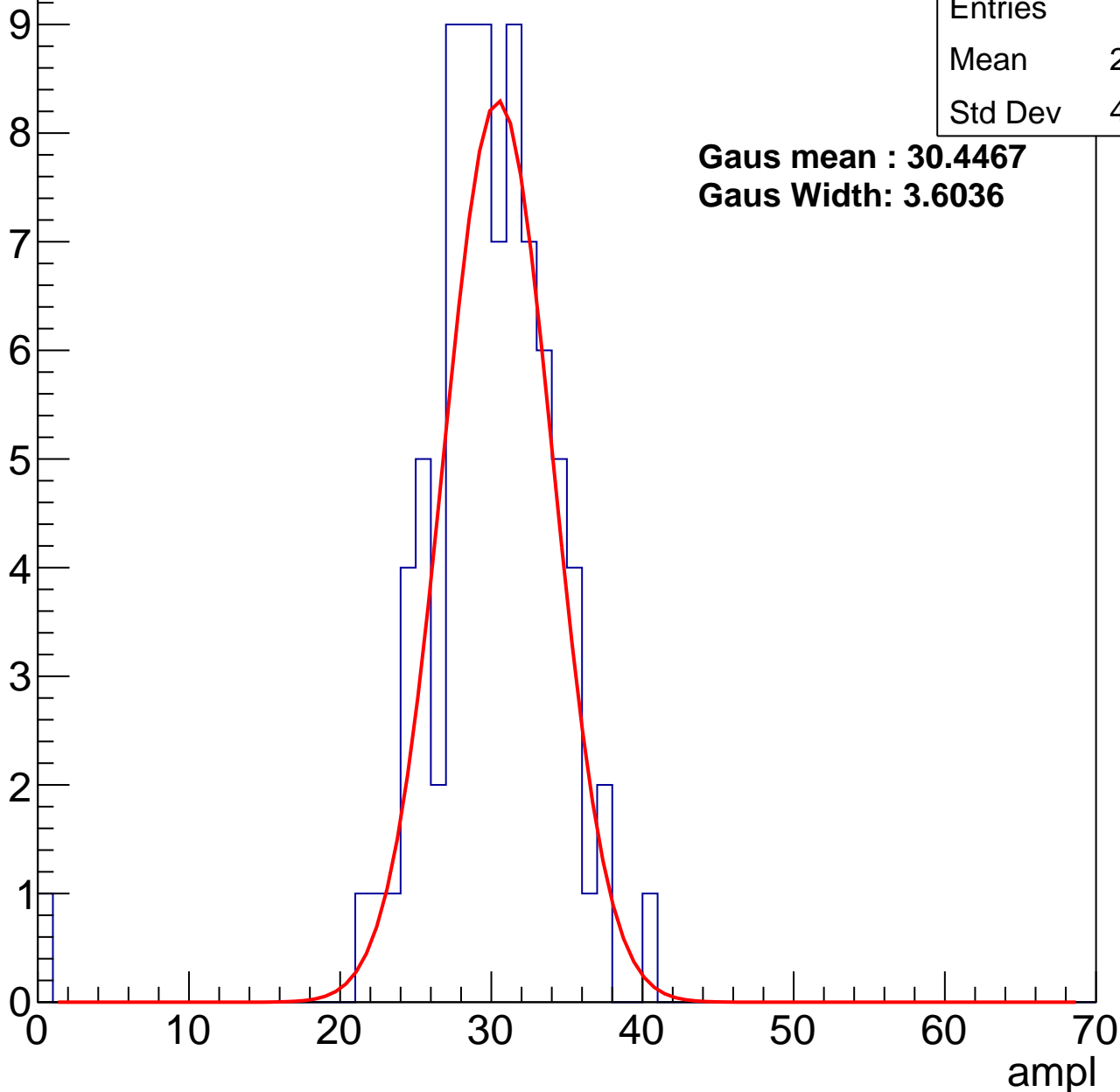
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	29.36
Std Dev	4.869

**Gaus mean : 30.4467**

**Gaus Width: 3.6036**



# B1L102S, U21-ch29, adc1

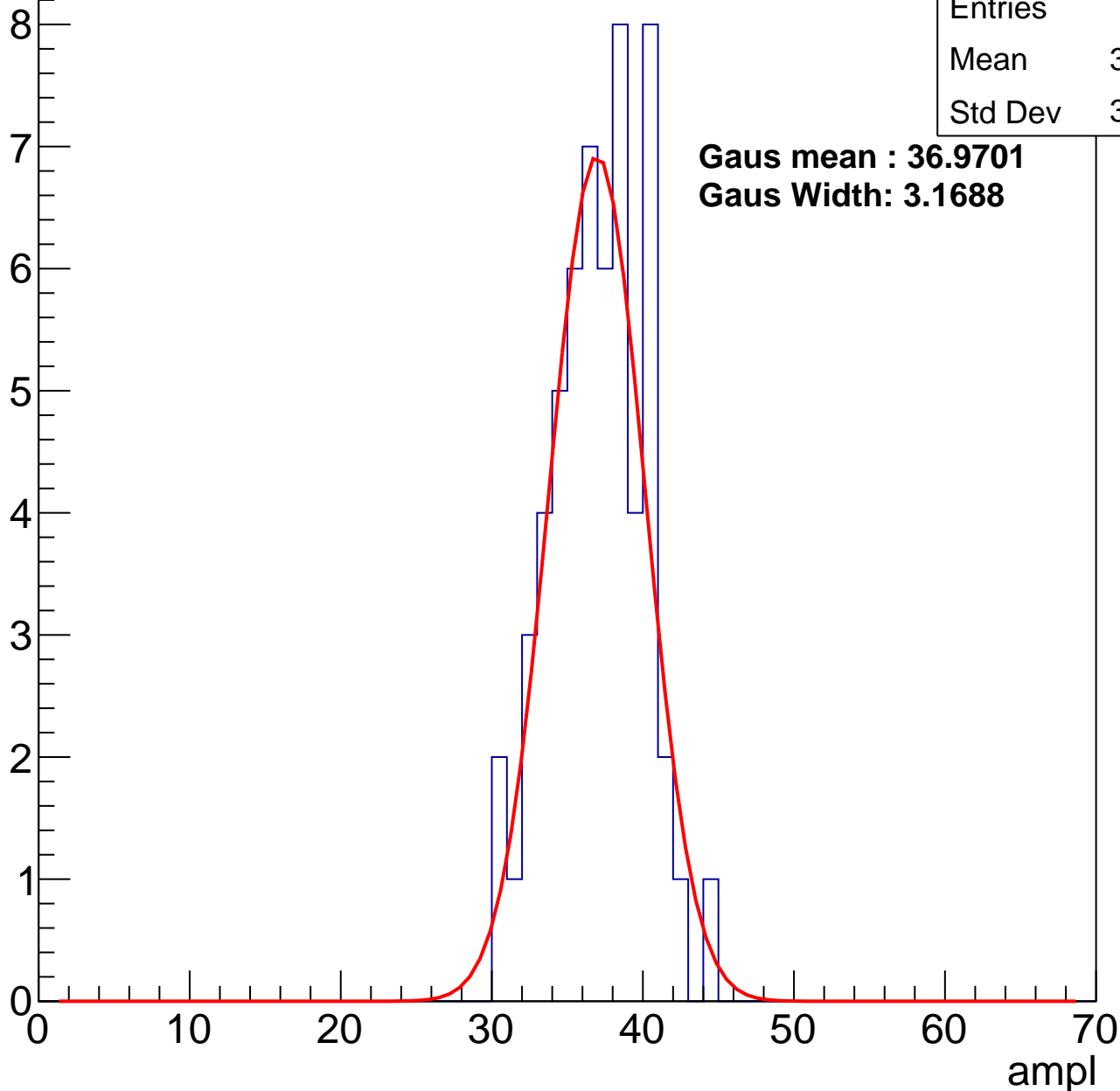
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	36.57
Std Dev	3.052

**Gaus mean : 36.9701**

**Gaus Width: 3.1688**



# B1L102S, U21-ch29, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	72
Mean	43
Std Dev	3.689

**Gaus mean : 44.4053**

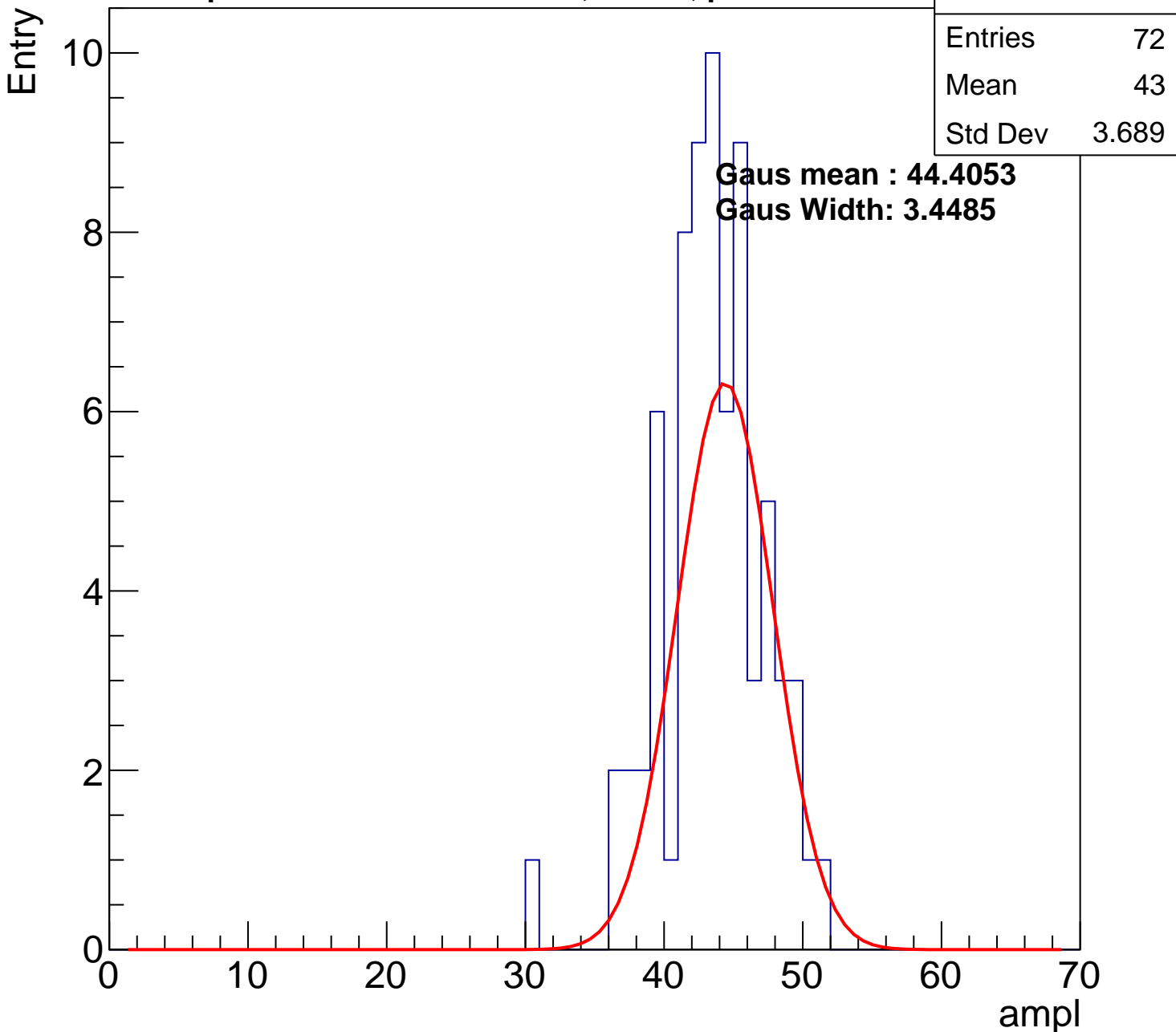
**Gaus Width: 3.4485**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

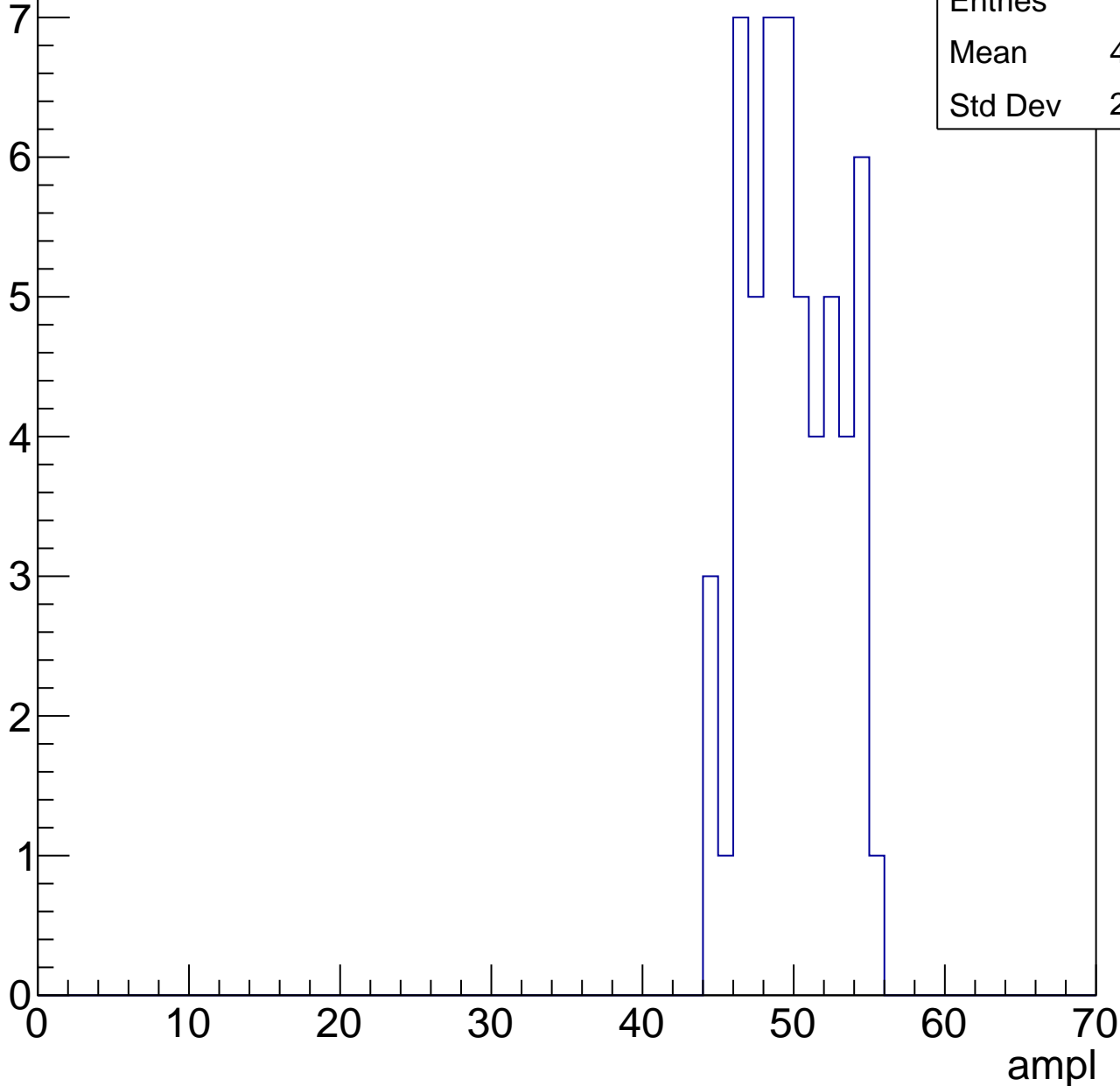


# B1L102S, U21-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

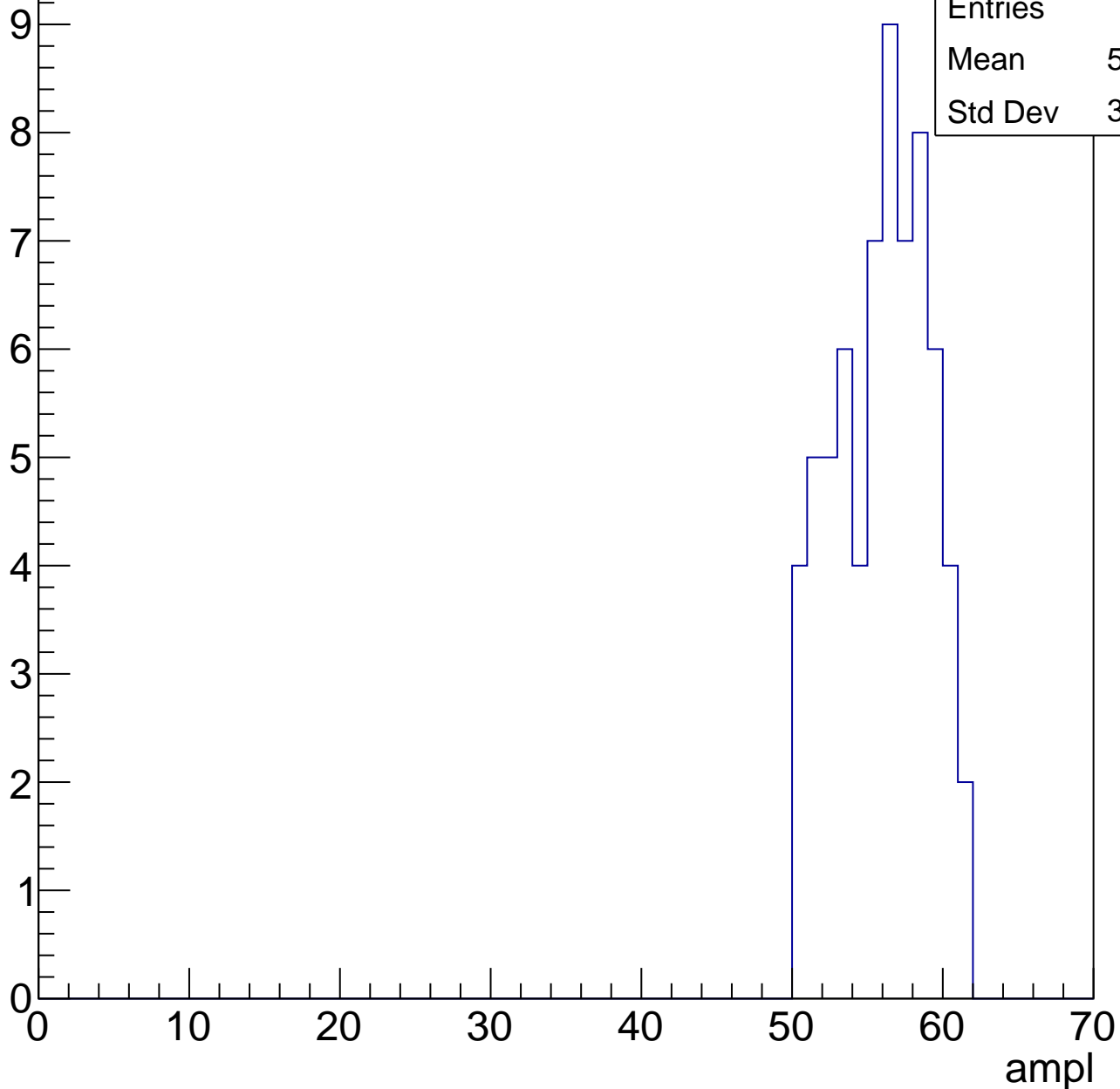
Entries	55
Mean	49.42
Std Dev	2.977



# B1L102S, U21-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

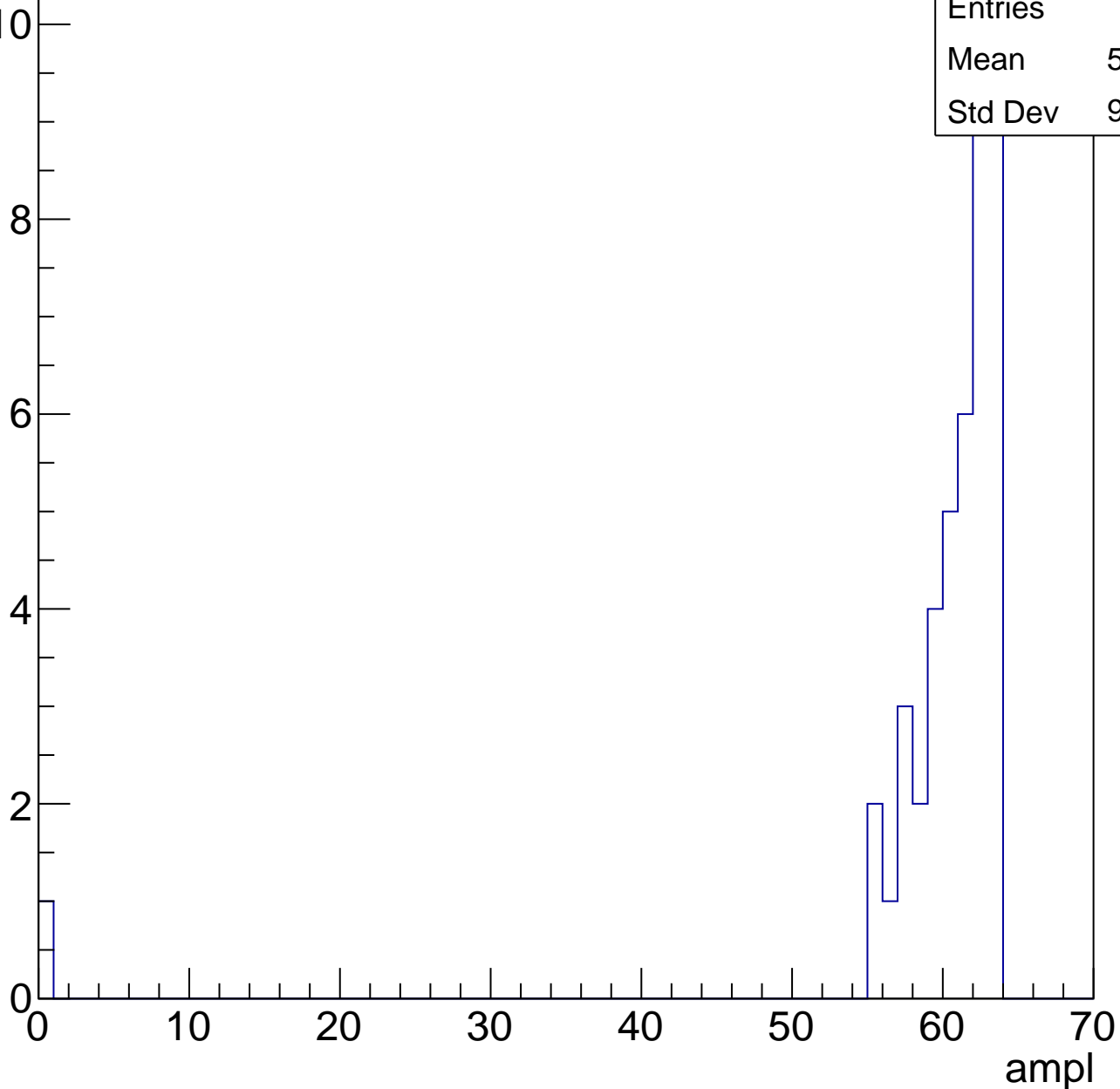


# B1L102S, U21-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

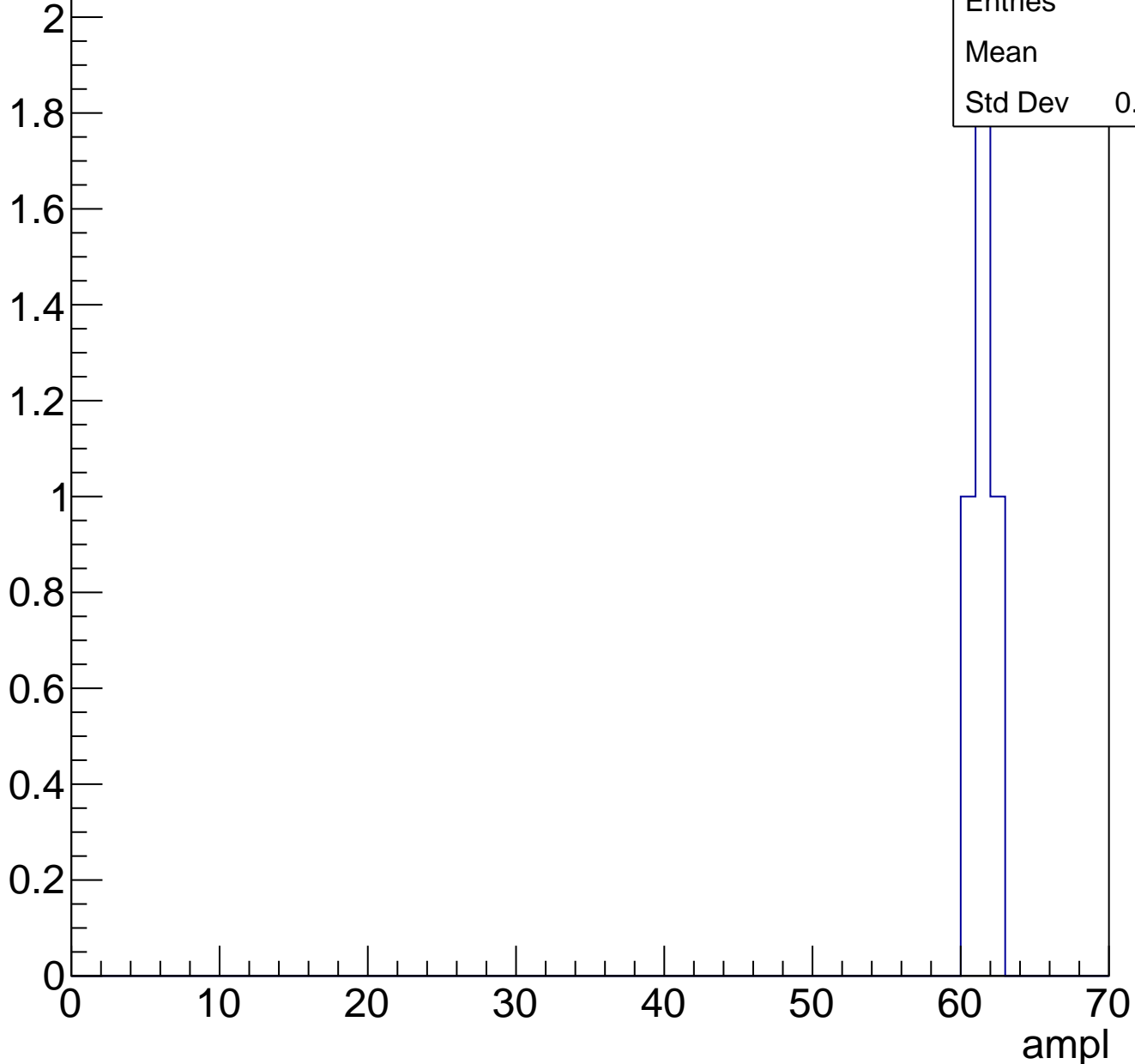
Entries	43
Mean	59.14
Std Dev	9.407



# B1L102S, U21-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U21-ch30, adc0

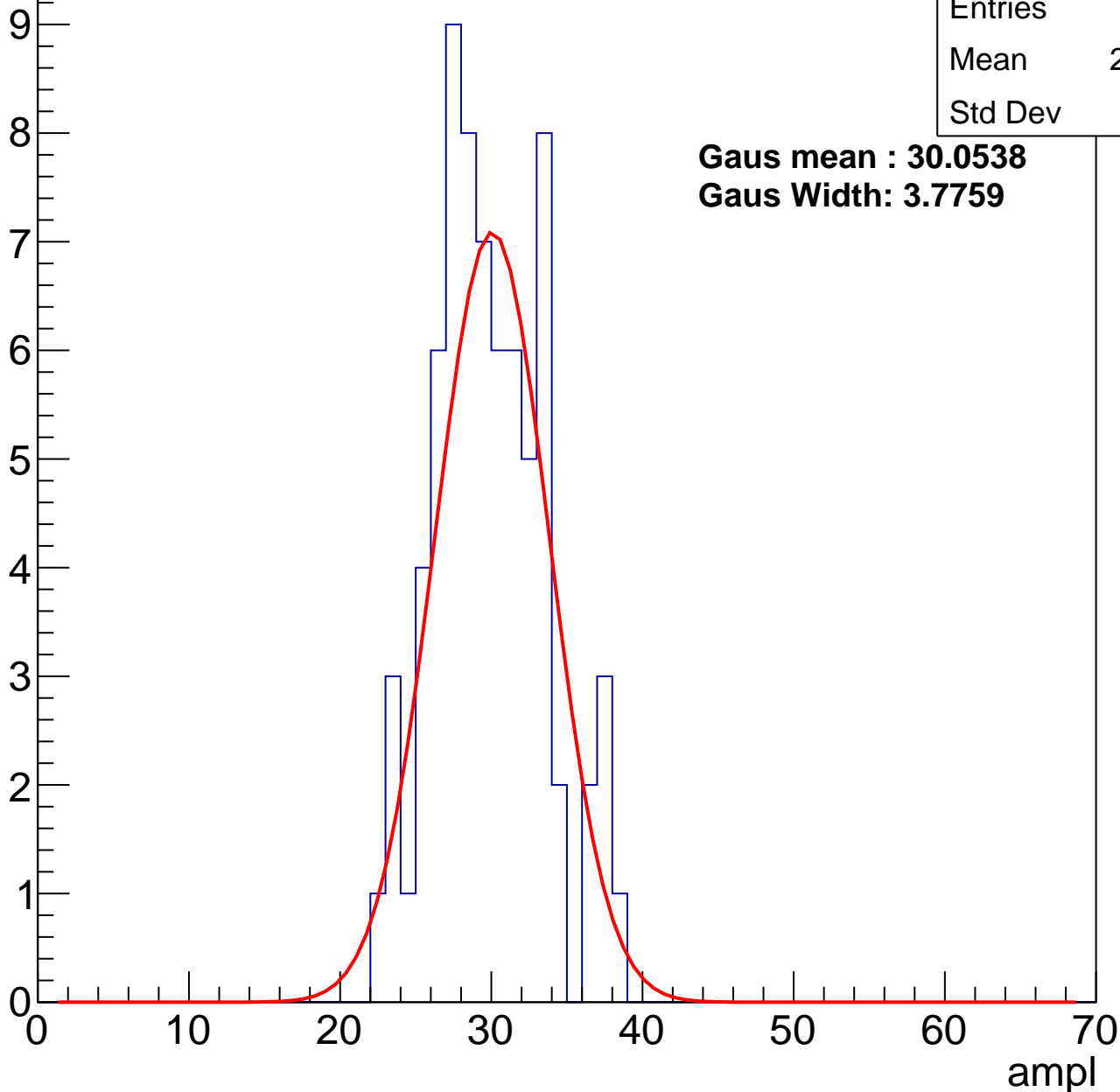
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	29.44
Std Dev	3.64

**Gaus mean : 30.0538**

**Gaus Width: 3.7759**



# B1L102S, U21-ch30, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	88
Mean	36.42
Std Dev	4.258

**Gaus mean : 37.0670**

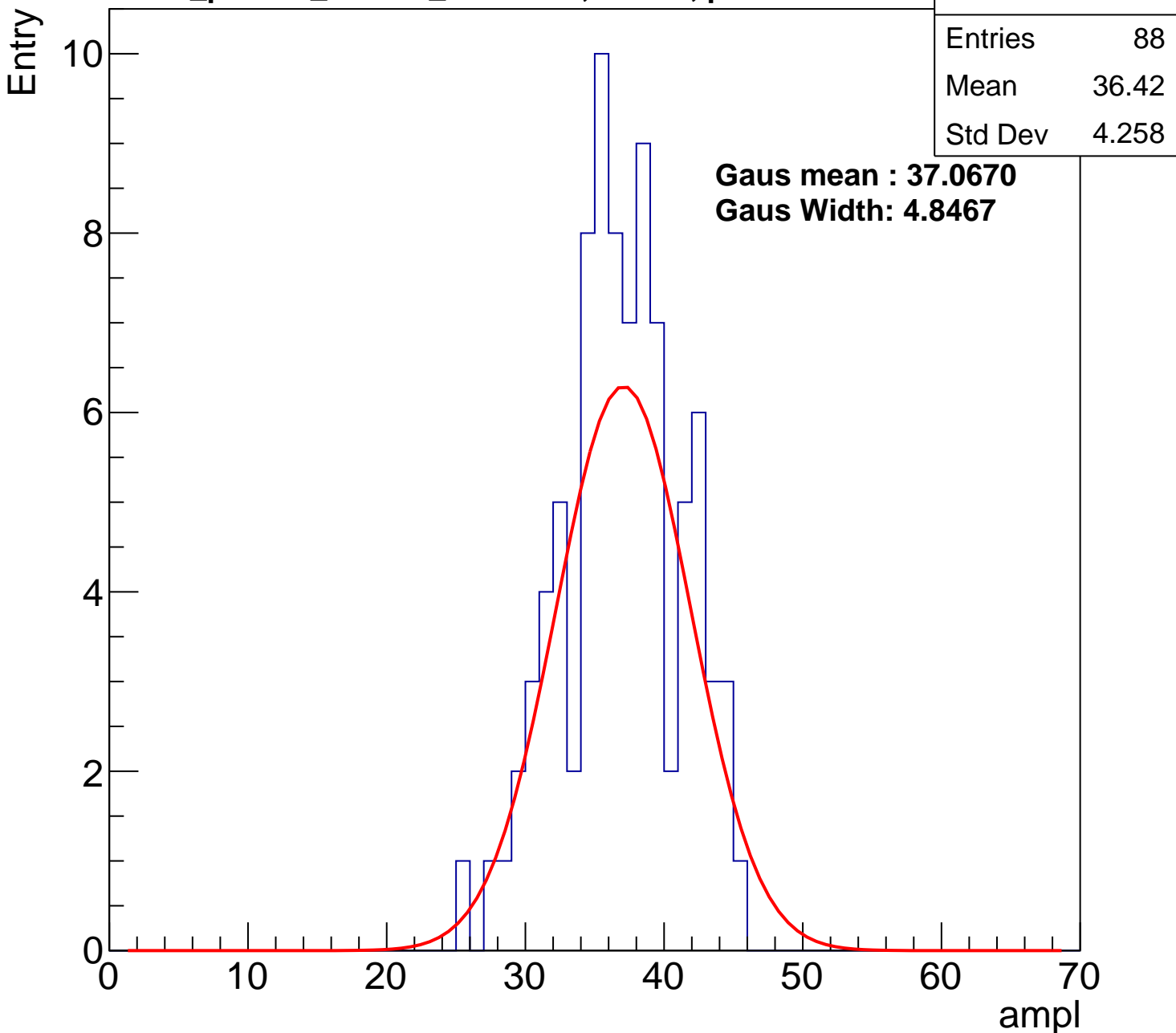
**Gaus Width: 4.8467**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U21-ch30, adc2

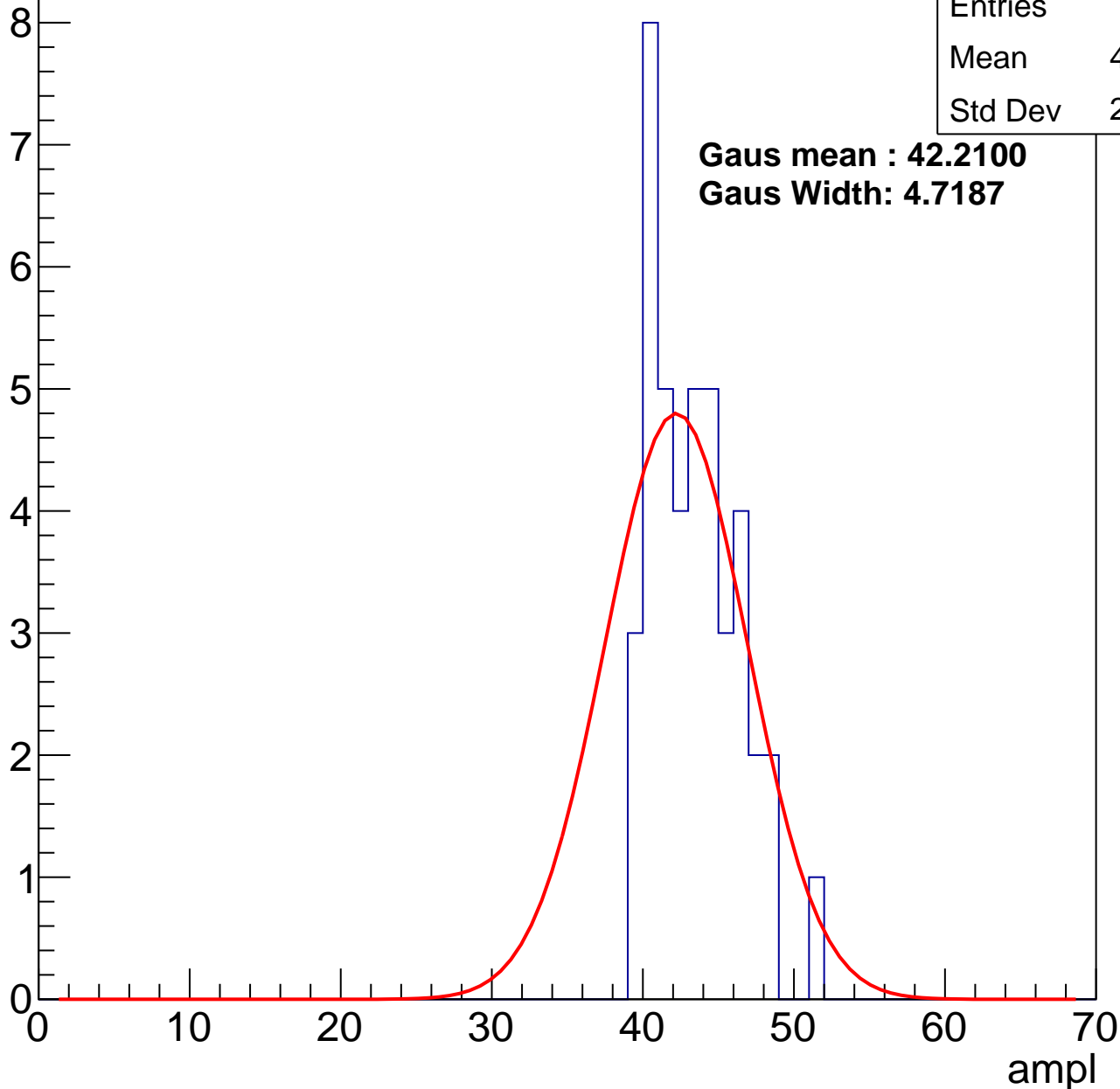
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	42
Mean	42.98
Std Dev	2.858

**Gaus mean : 42.2100**

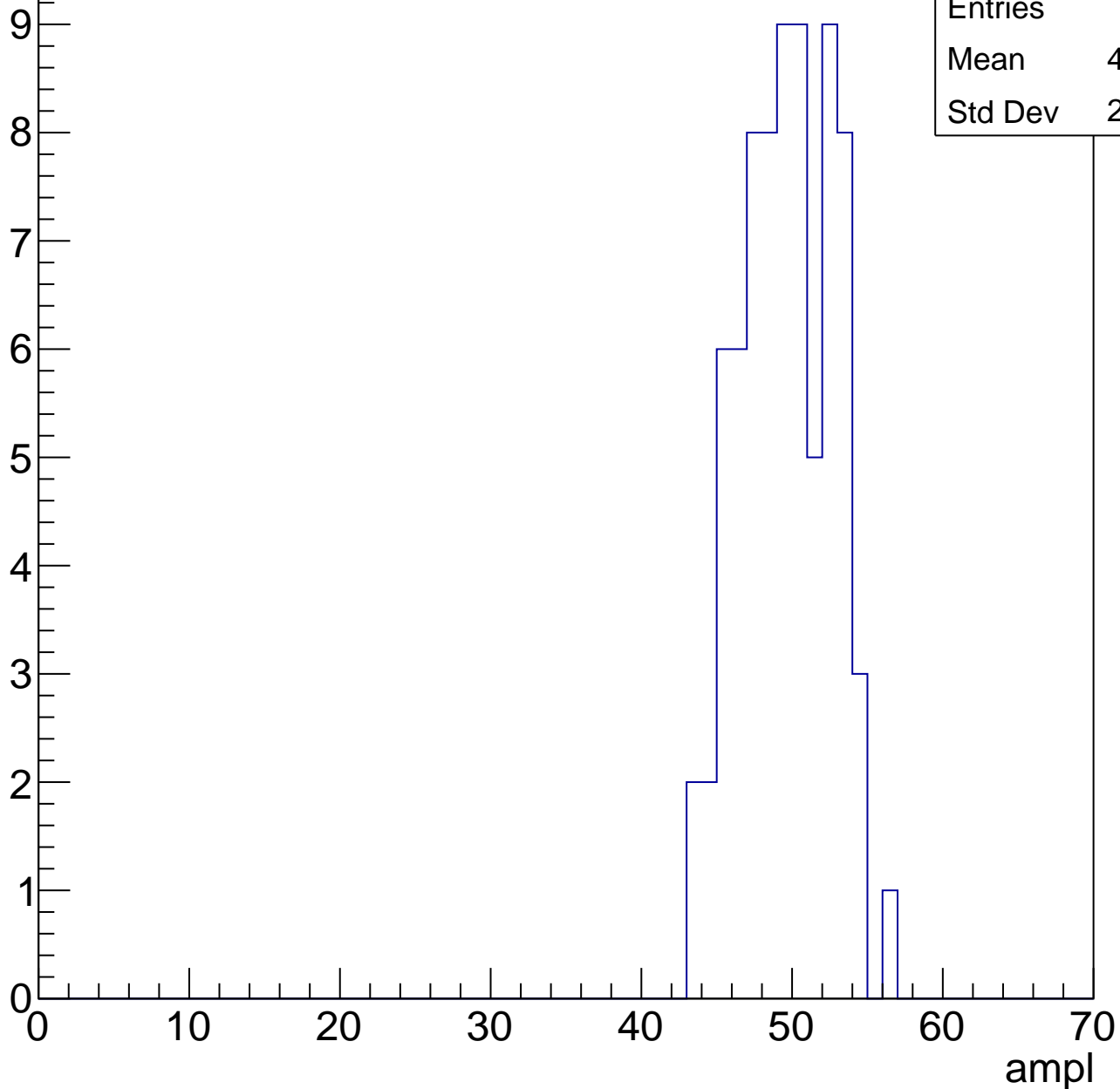
**Gaus Width: 4.7187**



# B1L102S, U21-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

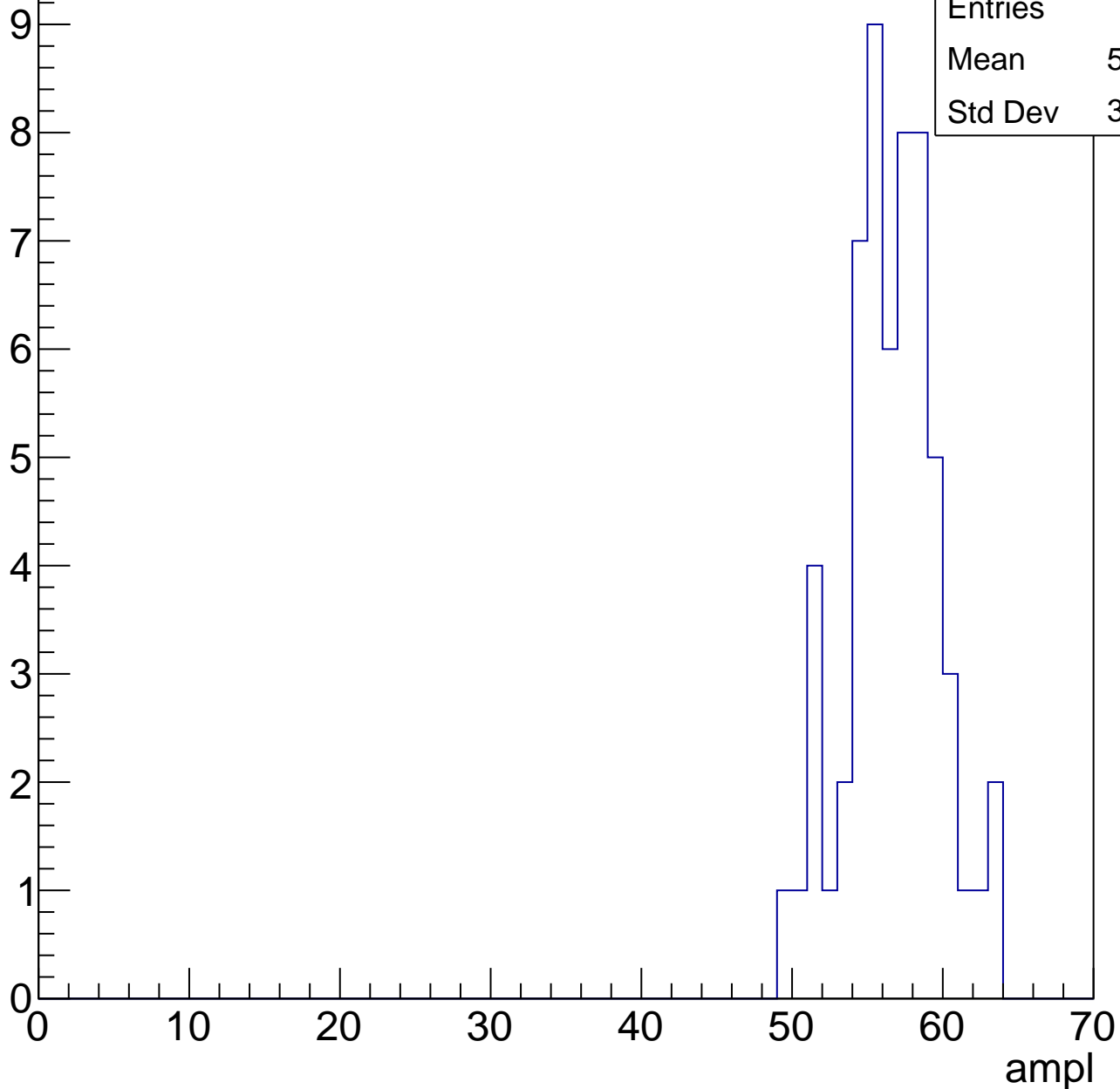
Entry



# B1L102S, U21-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

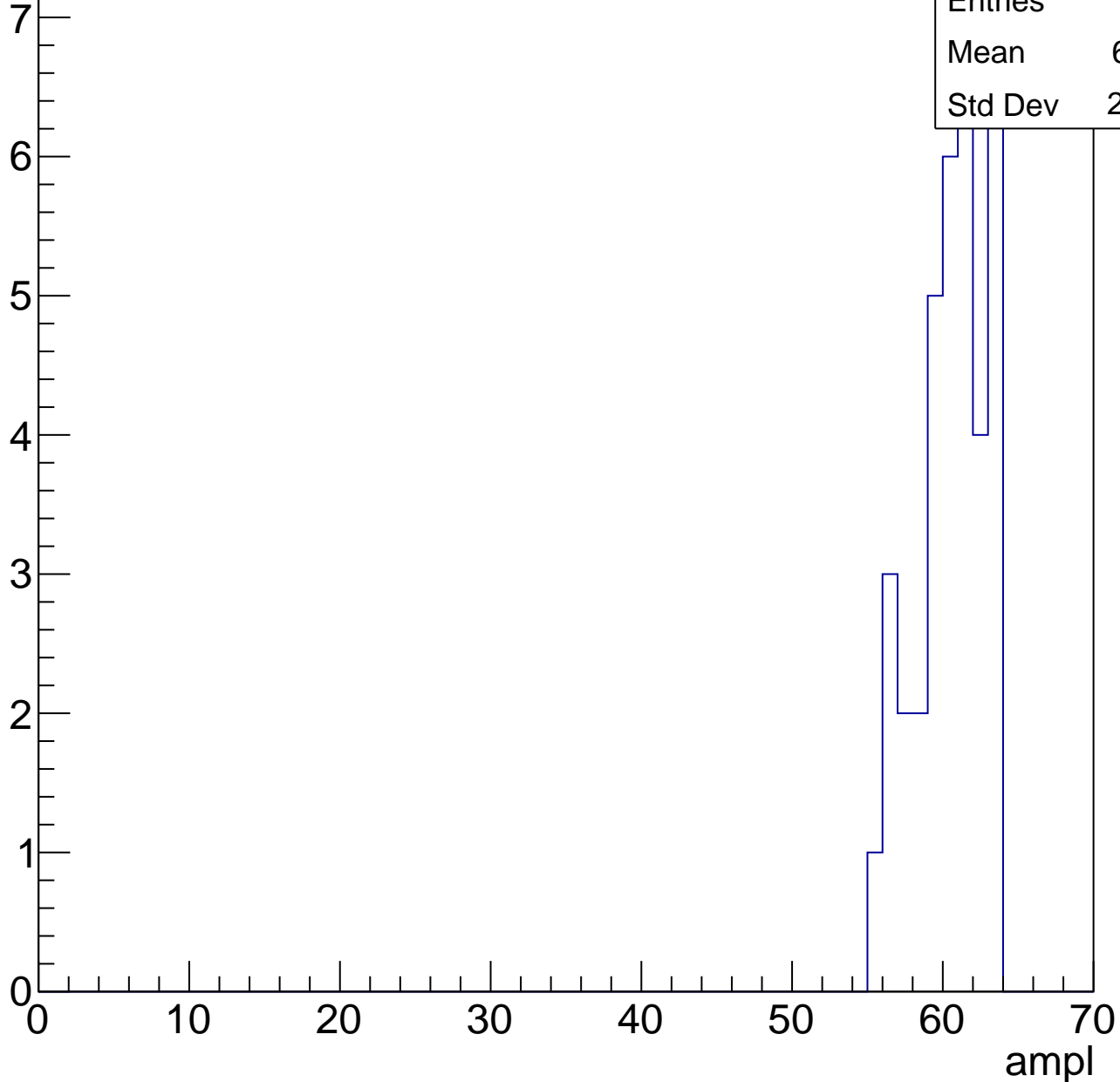
Entry



# B1L102S, U21-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

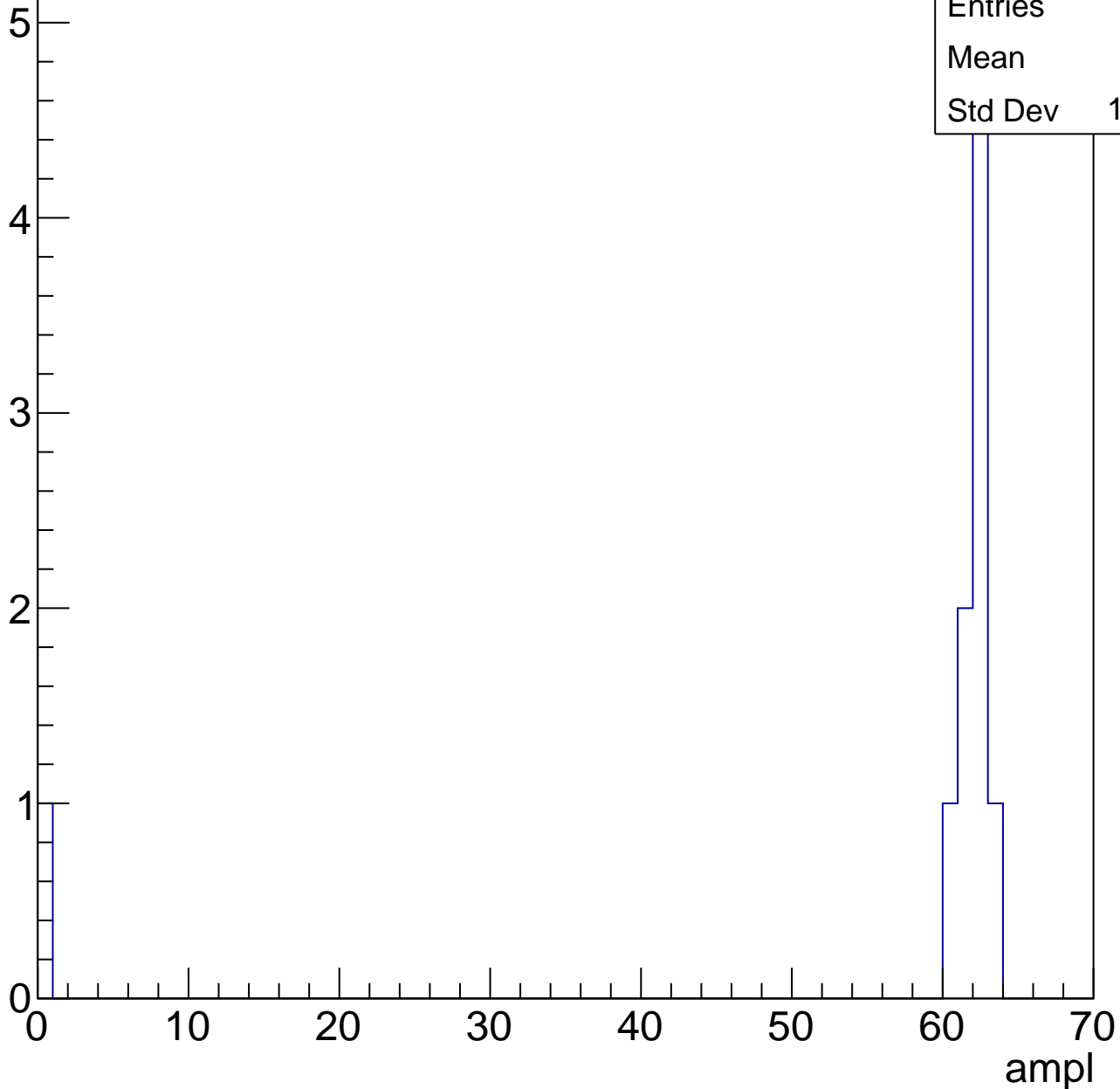


# B1L102S, U21-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	10
Mean	55.5
Std Dev	18.52





# B1L102S, U21-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U21-ch31, adc0

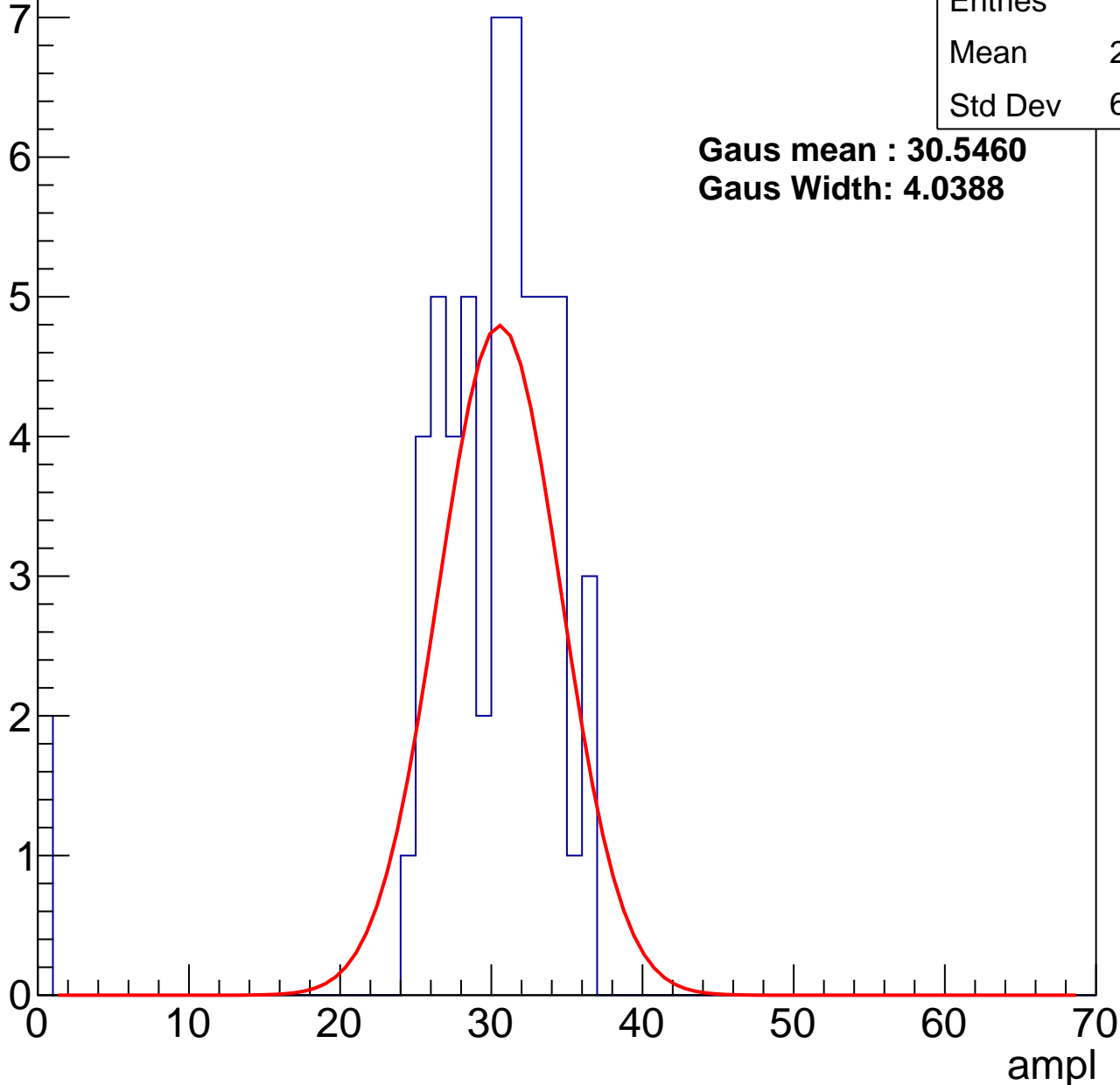
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	29.02
Std Dev	6.416

**Gaus mean : 30.5460**

**Gaus Width: 4.0388**



# B1L102S, U21-ch31, adc1

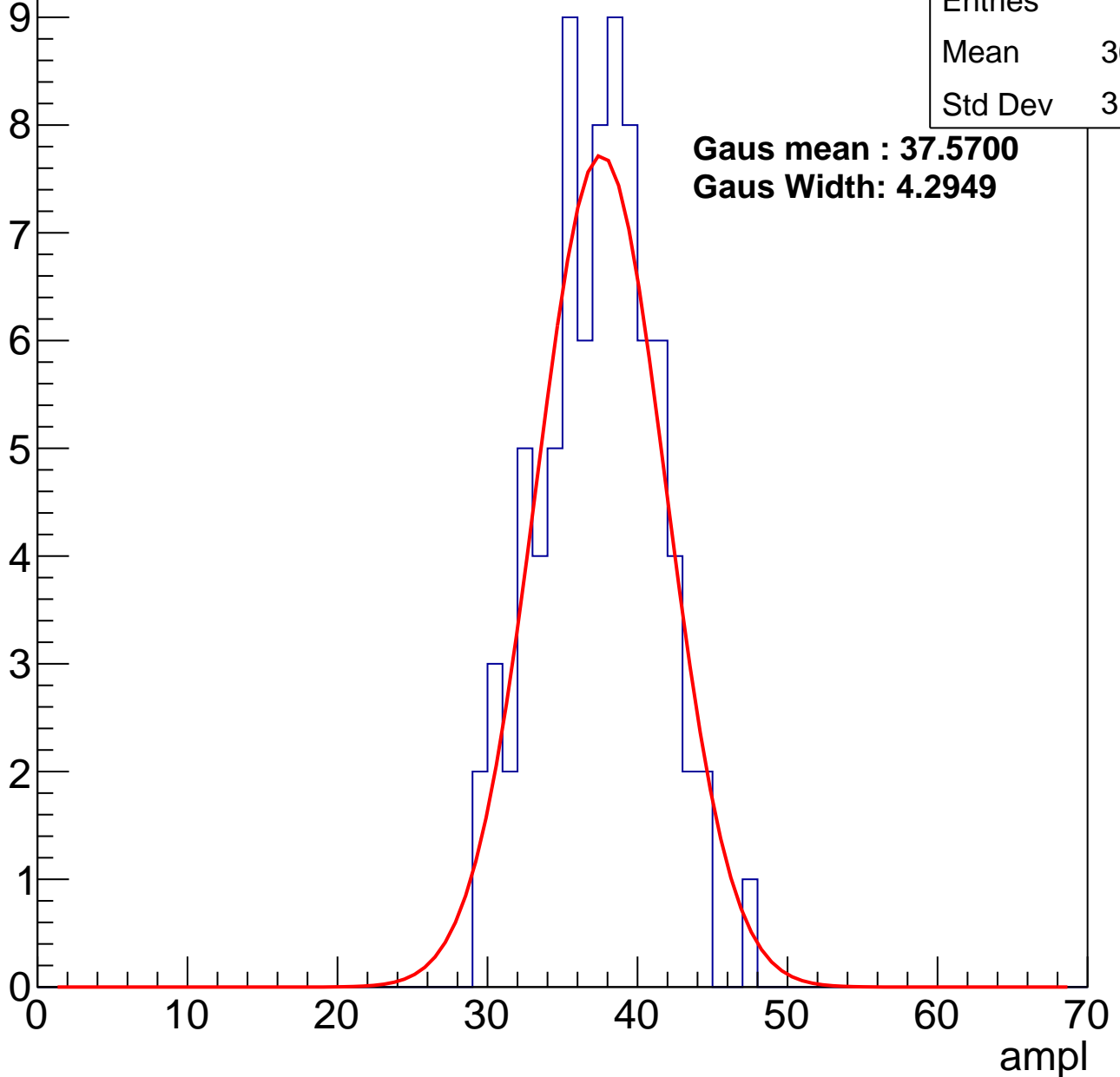
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	36.93
Std Dev	3.799

**Gaus mean : 37.5700**

**Gaus Width: 4.2949**



# B1L102S, U21-ch31, adc2

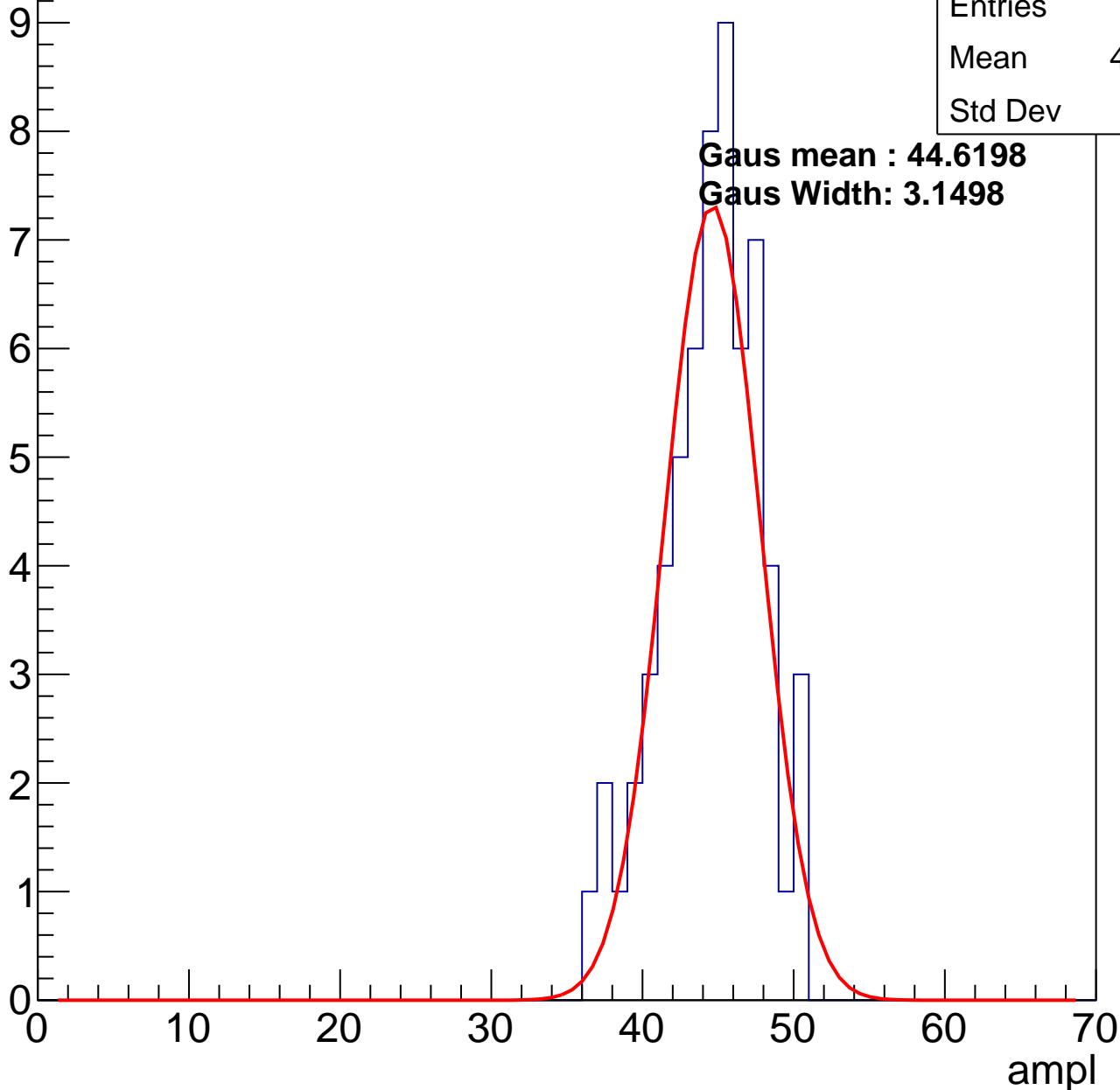
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	44.05
Std Dev	3.24

**Gaus mean : 44.6198**

**Gaus Width: 3.1498**

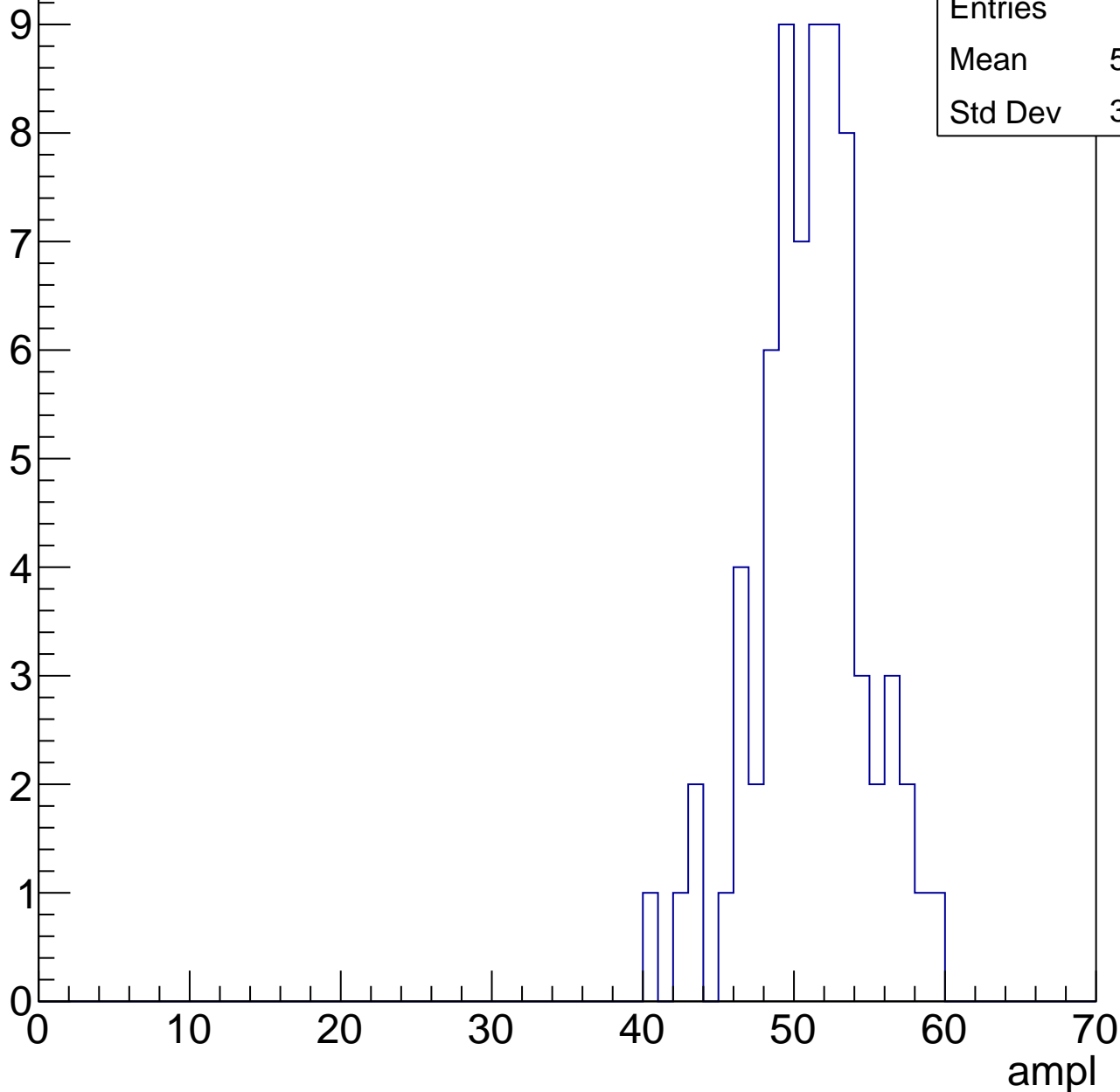


# B1L102S, U21-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	50.59
Std Dev	3.645



# B1L102S, U21-ch31, adc4

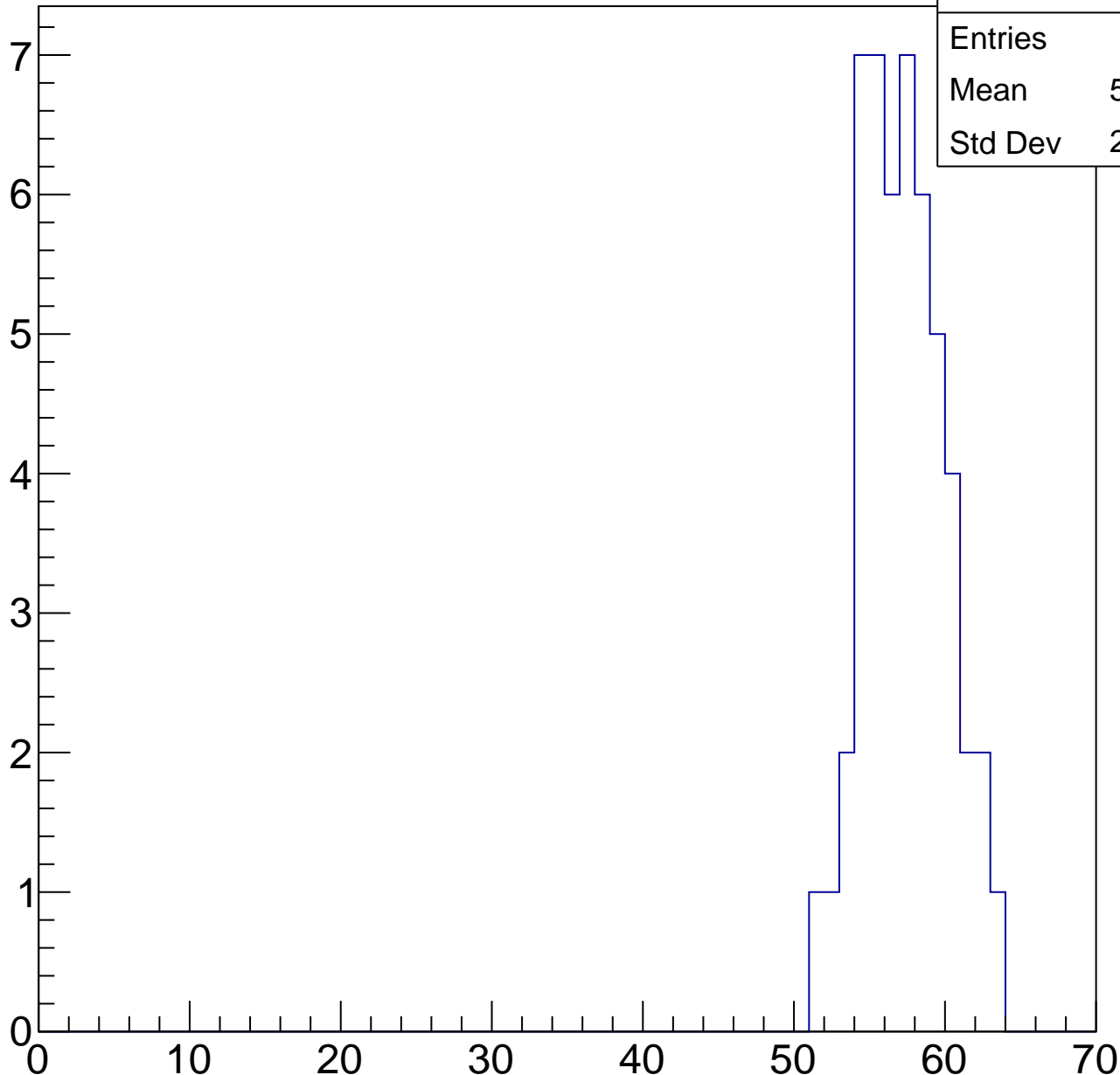
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	56.84
Std Dev	2.689

ampl

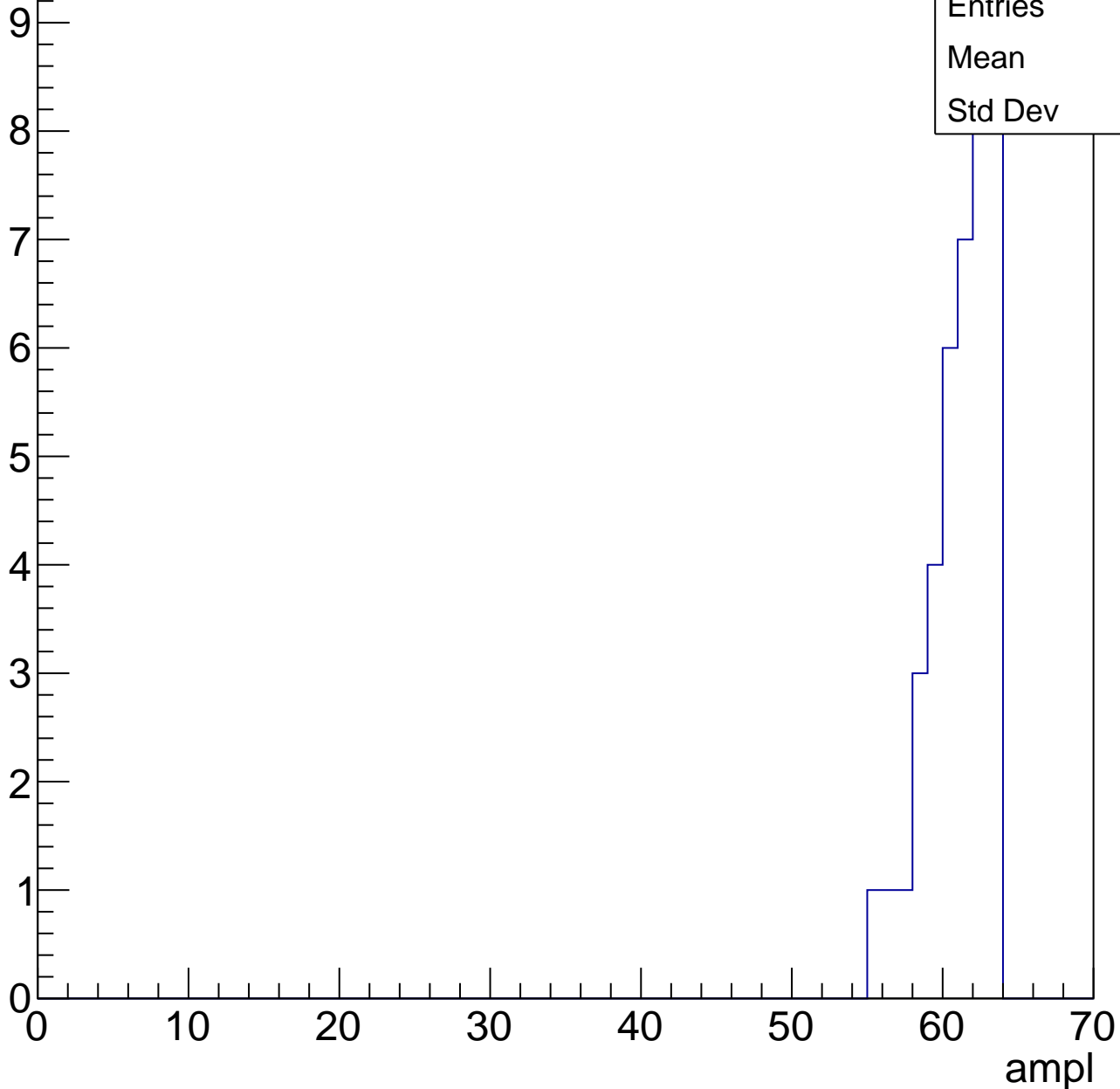


# B1L102S, U21-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

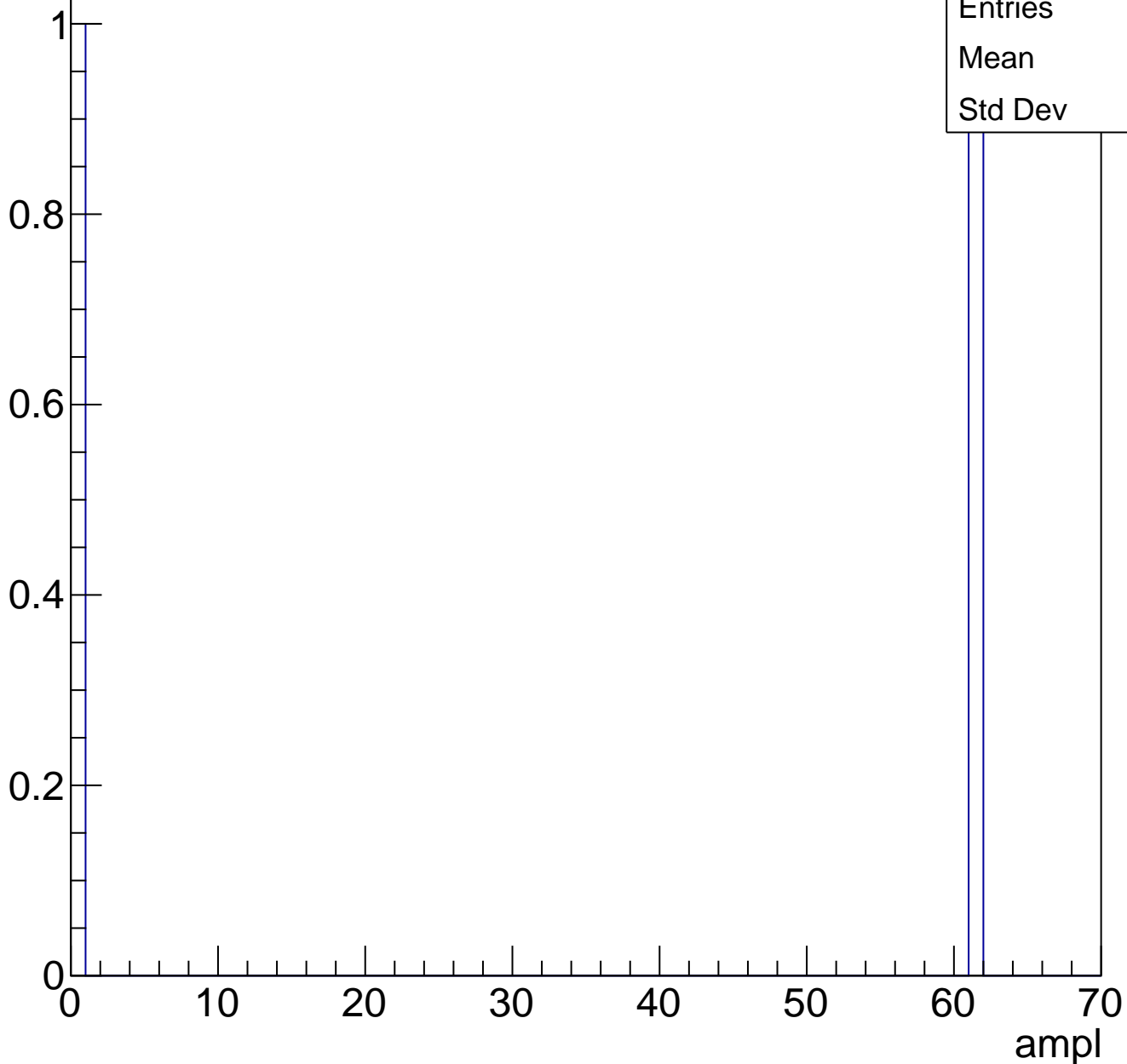
Entries	40
Mean	60.7
Std Dev	2.04



# B1L102S, U21-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch32, adc0

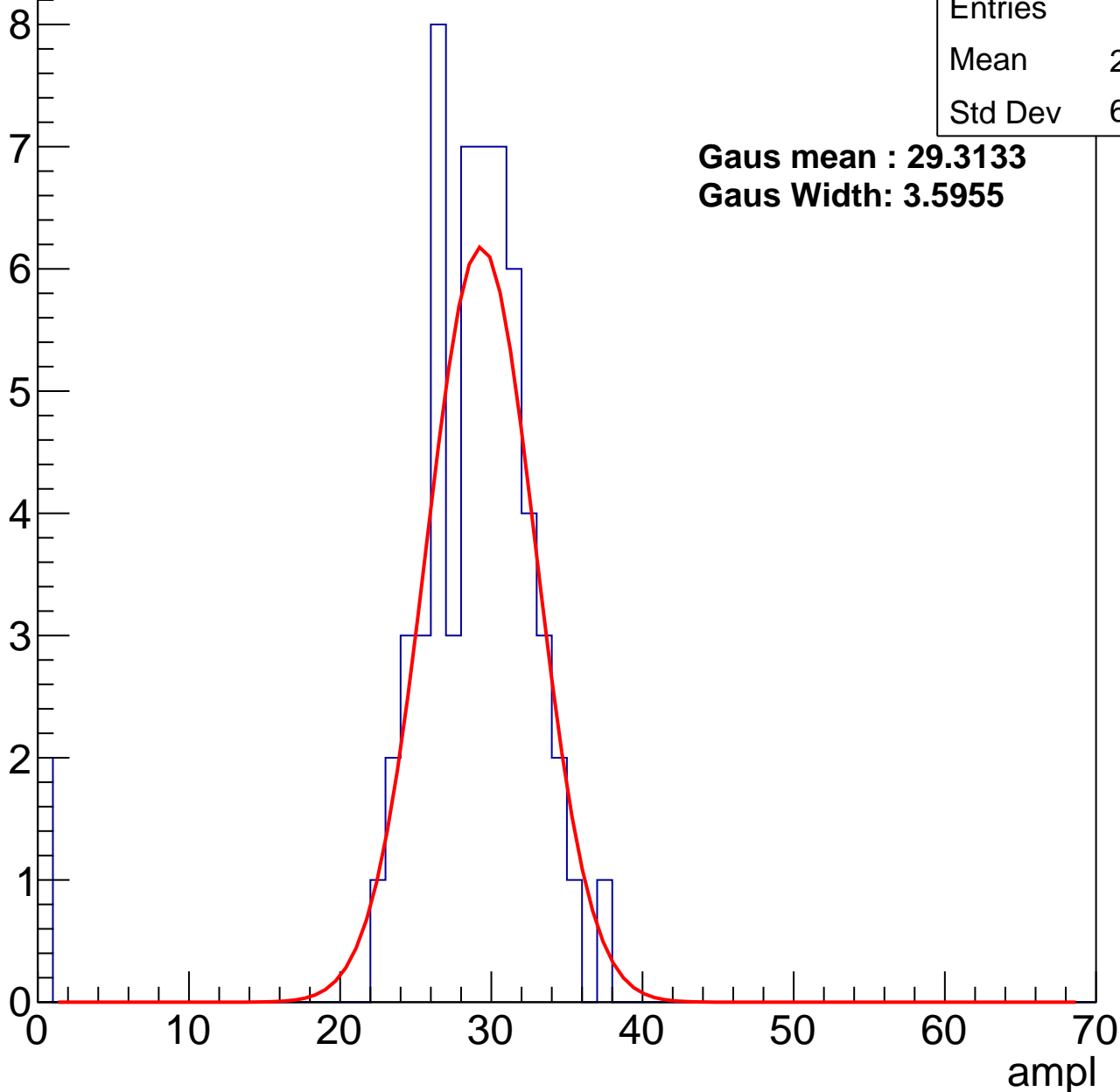
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	27.77
Std Dev	6.043

**Gaus mean : 29.3133**

**Gaus Width: 3.5955**



# B1L102S, U21-ch32, adc1

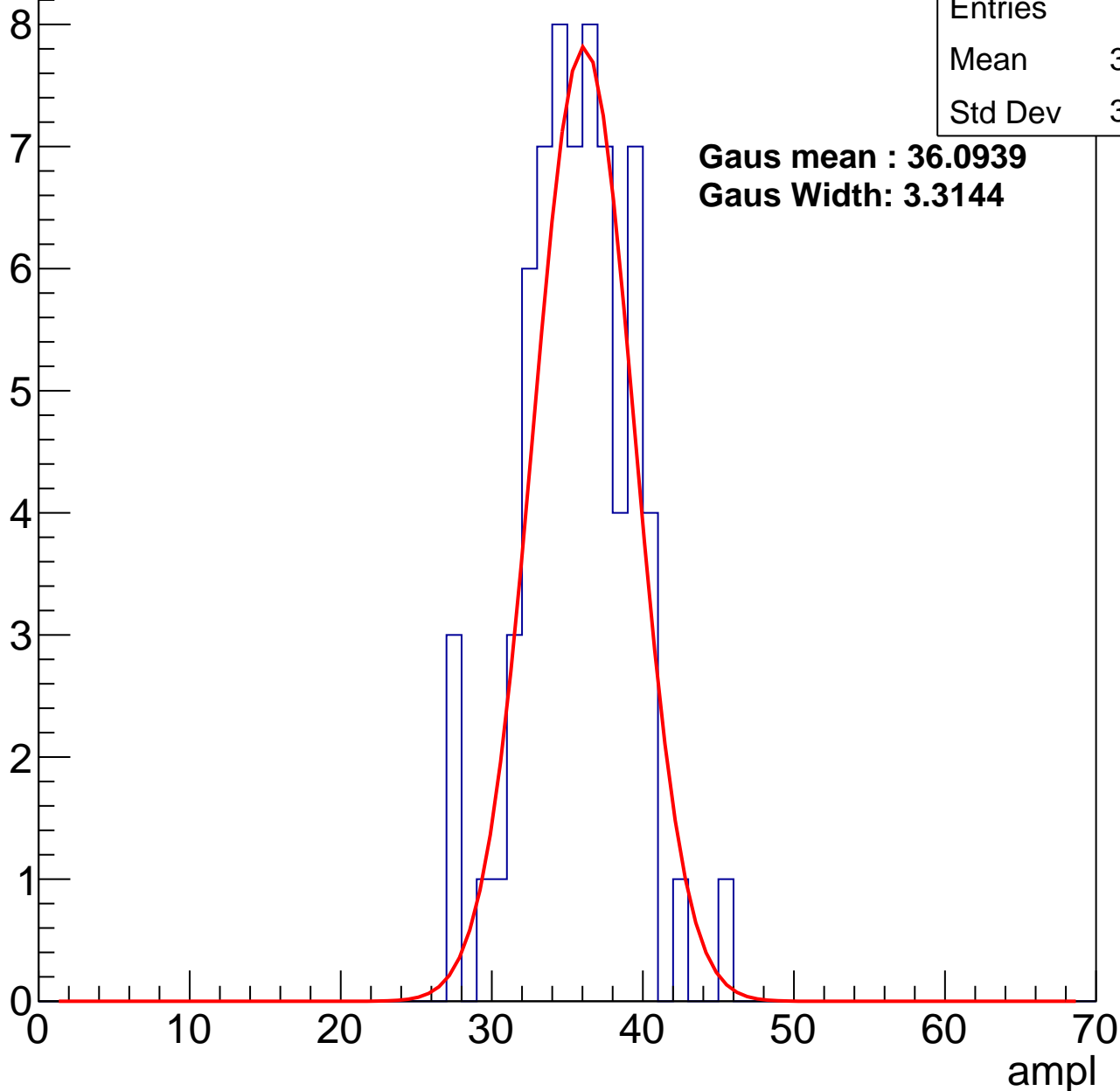
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	35.18
Std Dev	3.477

**Gaus mean : 36.0939**

**Gaus Width: 3.3144**



# B1L102S, U21-ch32, adc2

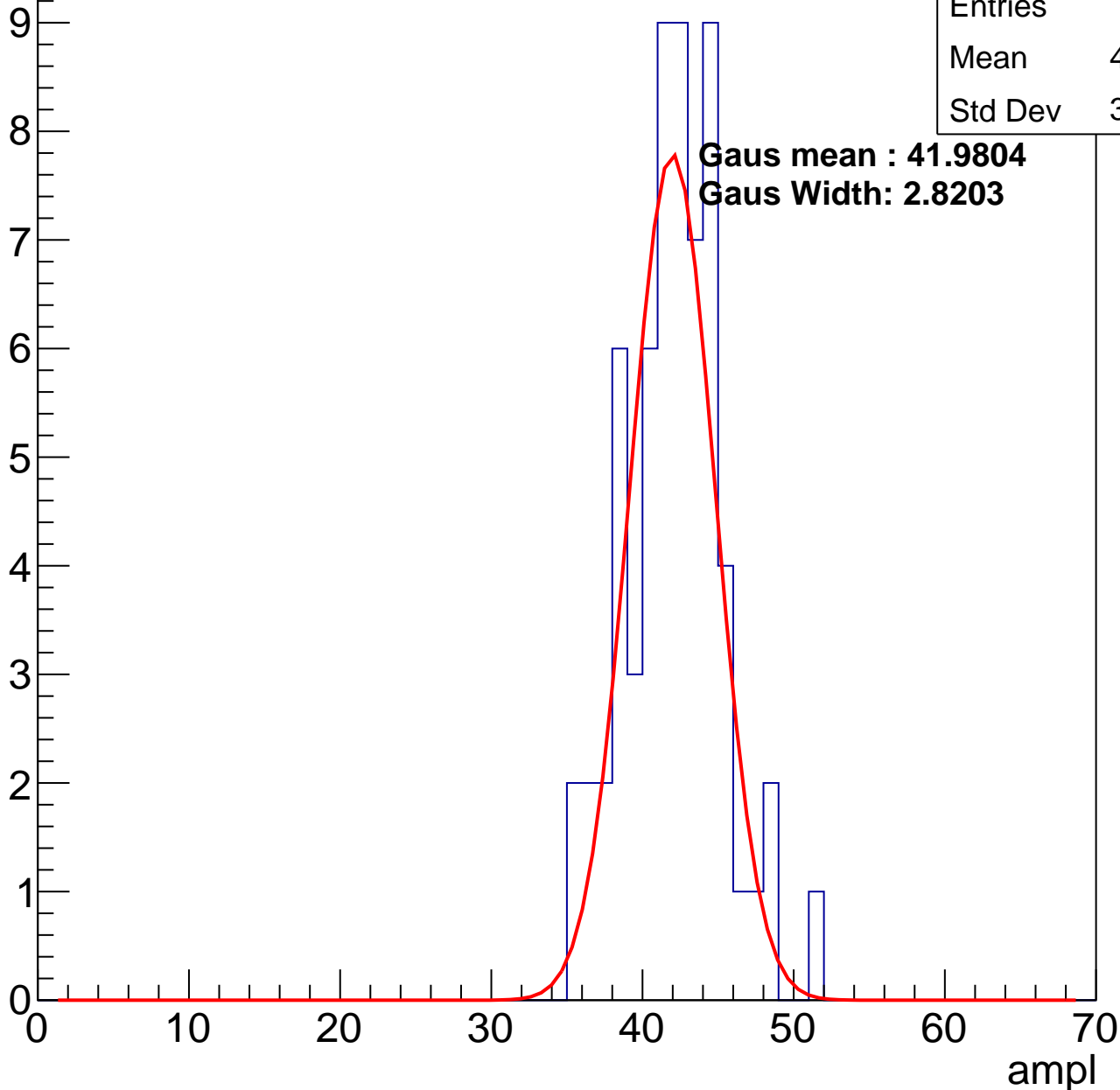
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	41.64
Std Dev	3.164

**Gaus mean : 41.9804**

**Gaus Width: 2.8203**

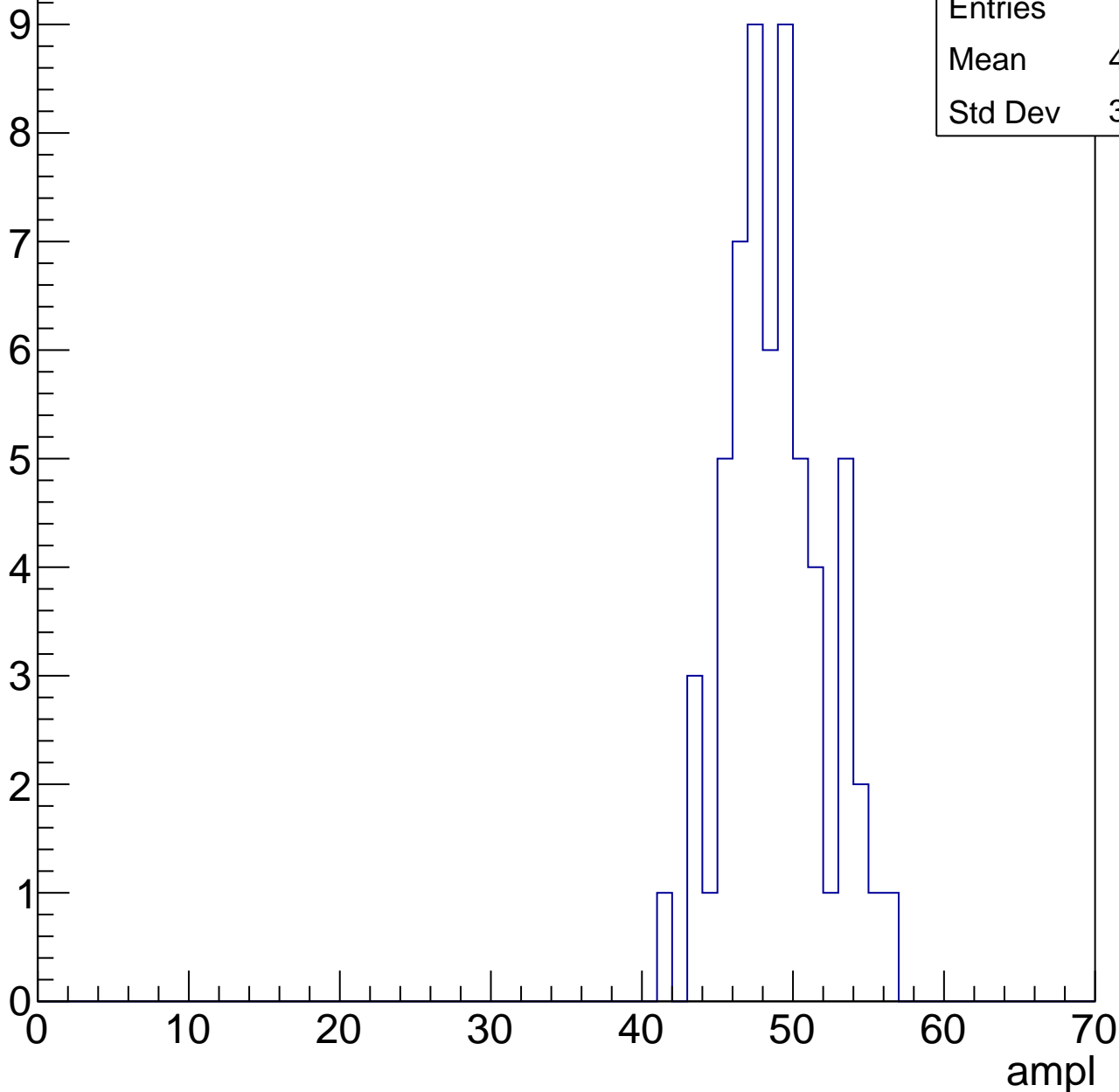


# B1L102S, U21-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	48.38
Std Dev	3.173

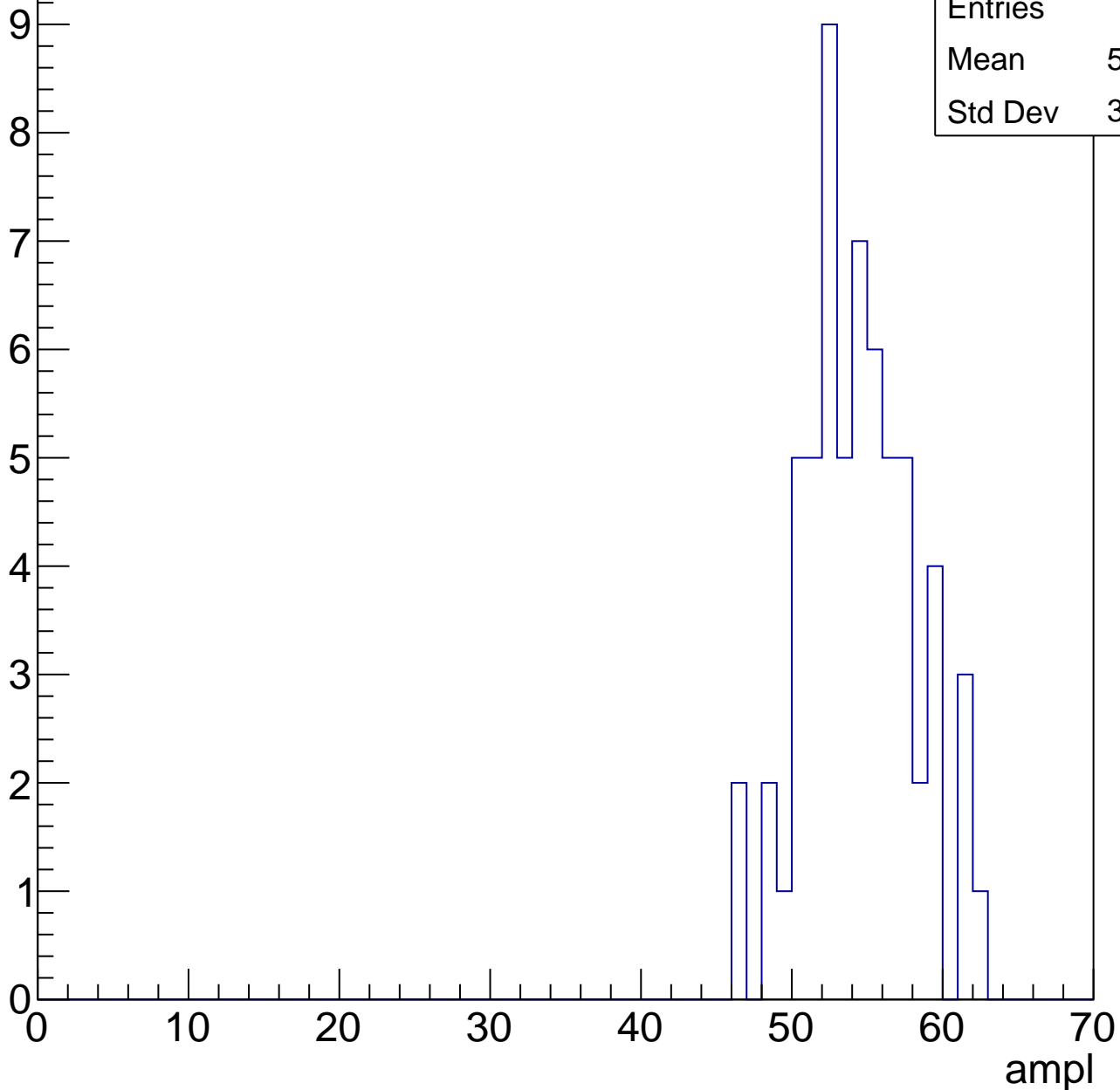


# B1L102S, U21-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	53.95
Std Dev	3.603

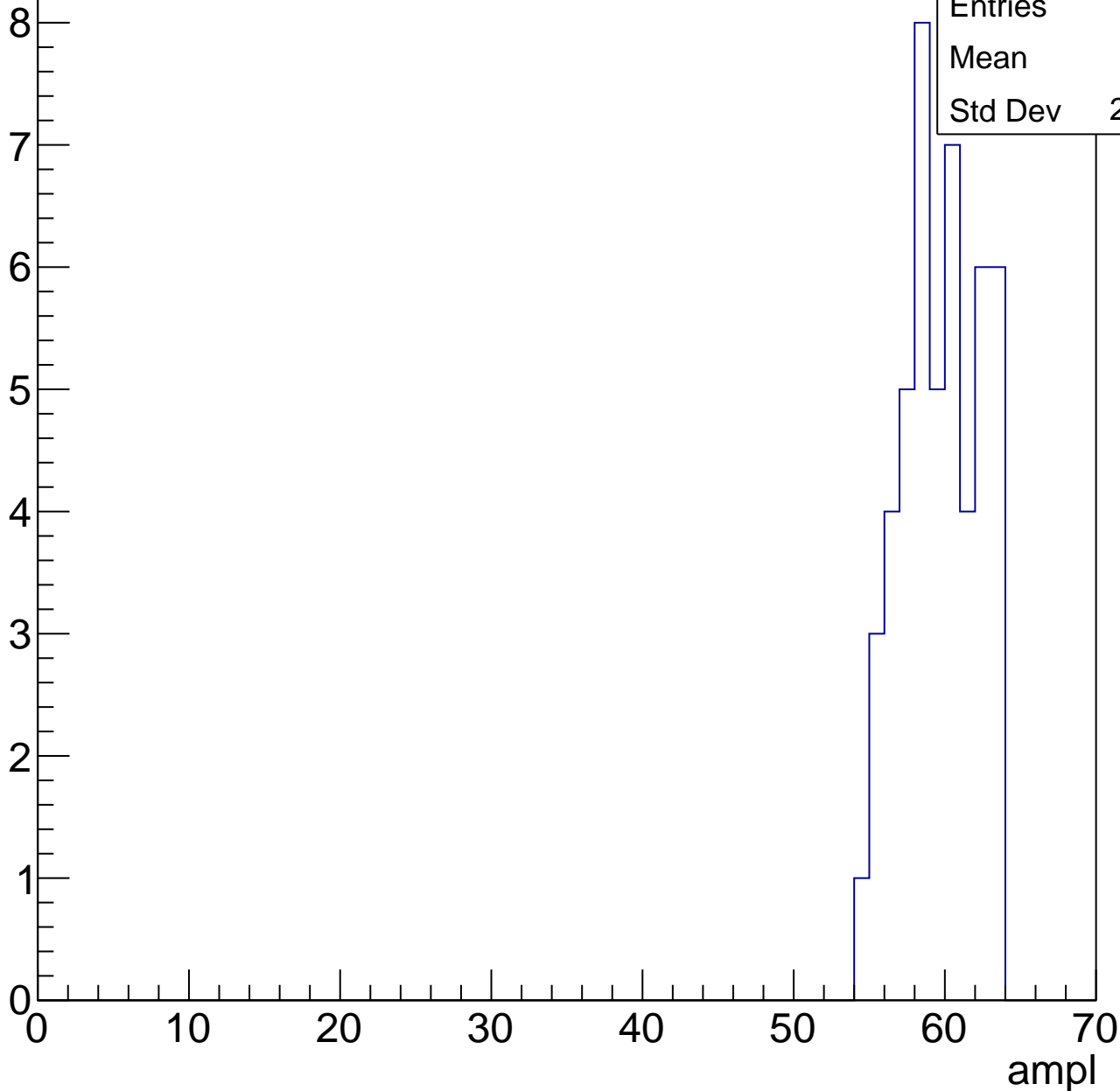


# B1L102S, U21-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	59.2
Std Dev	2.507



# B1L102S, U21-ch32, adc6

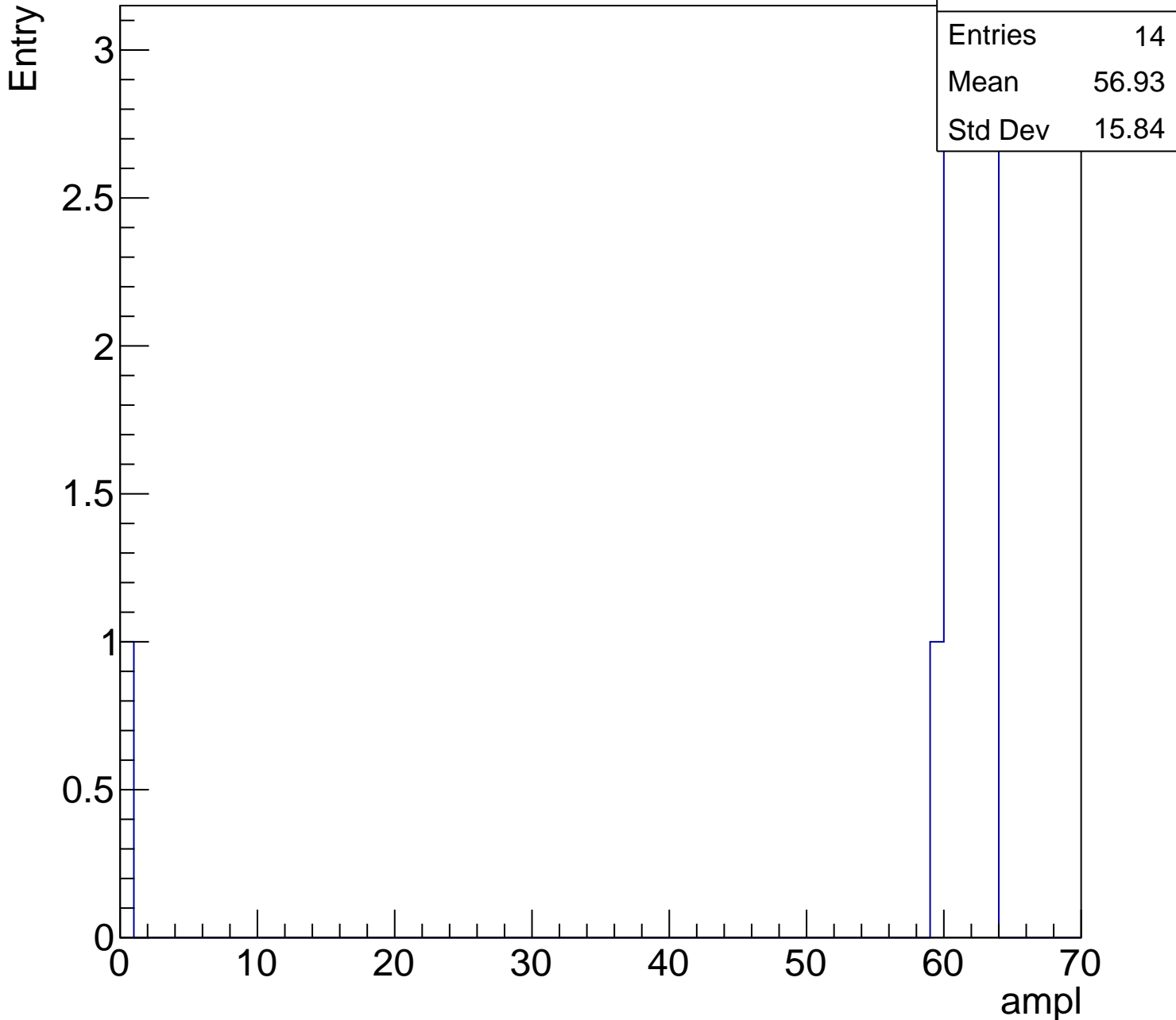
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	14
Mean	56.93
Std Dev	15.84

ampl





# B1L102S, U21-ch32, adc7

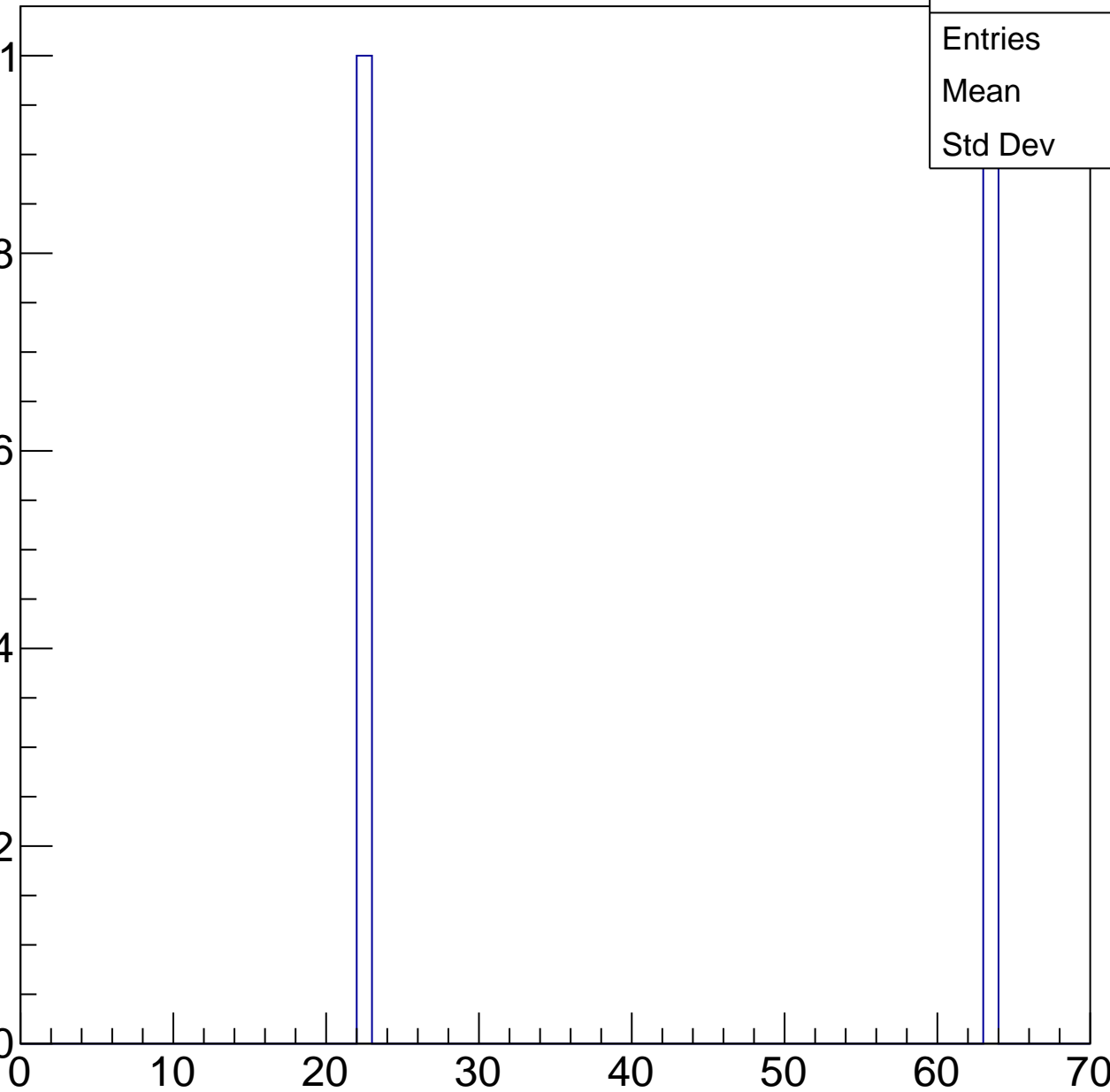
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	42.5
Std Dev	20.5

ampl



# B1L102S, U21-ch33, adc0

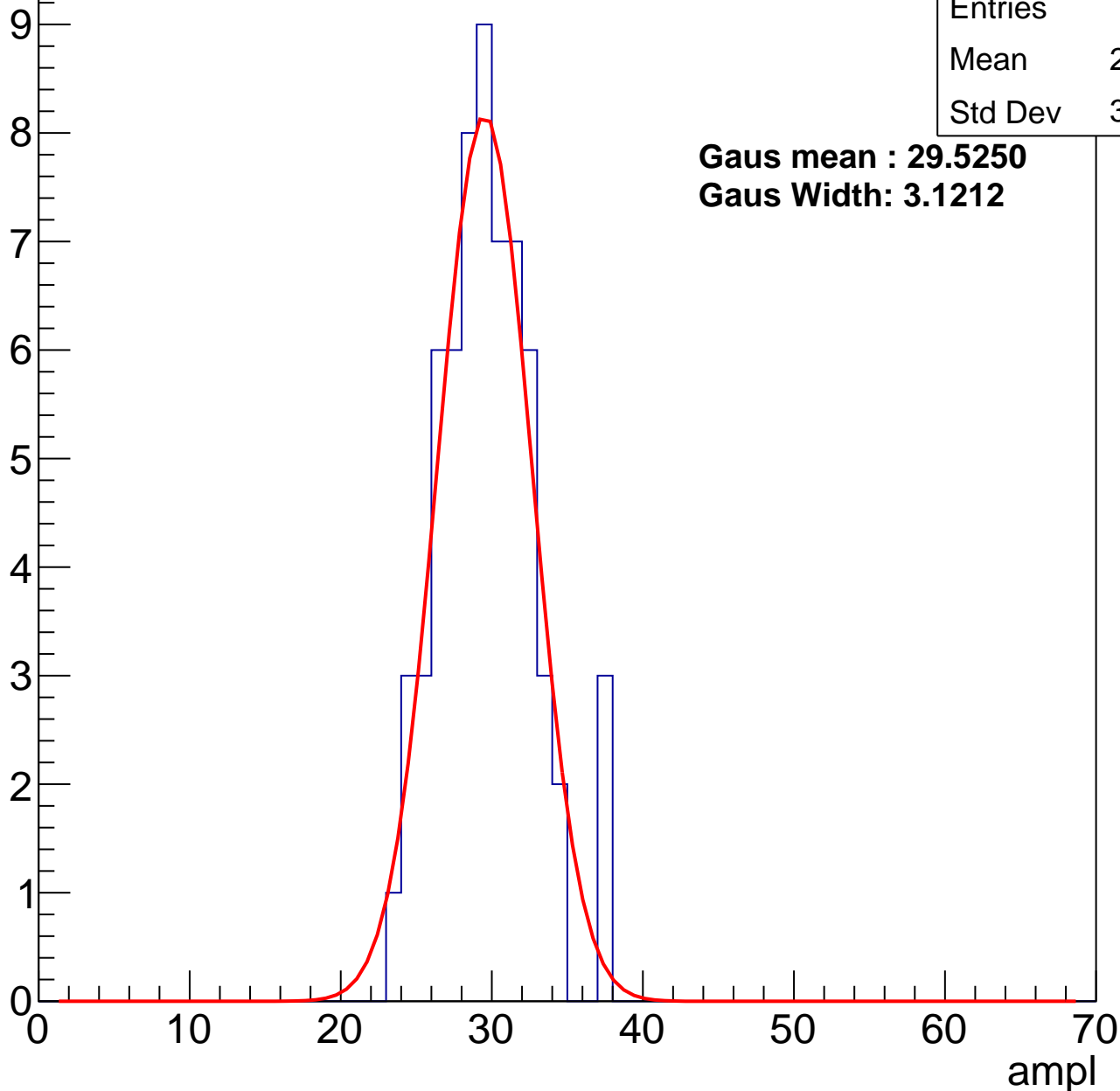
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	29.22
Std Dev	3.115

**Gaus mean : 29.5250**

**Gaus Width: 3.1212**



# B1L102S, U21-ch33, adc1

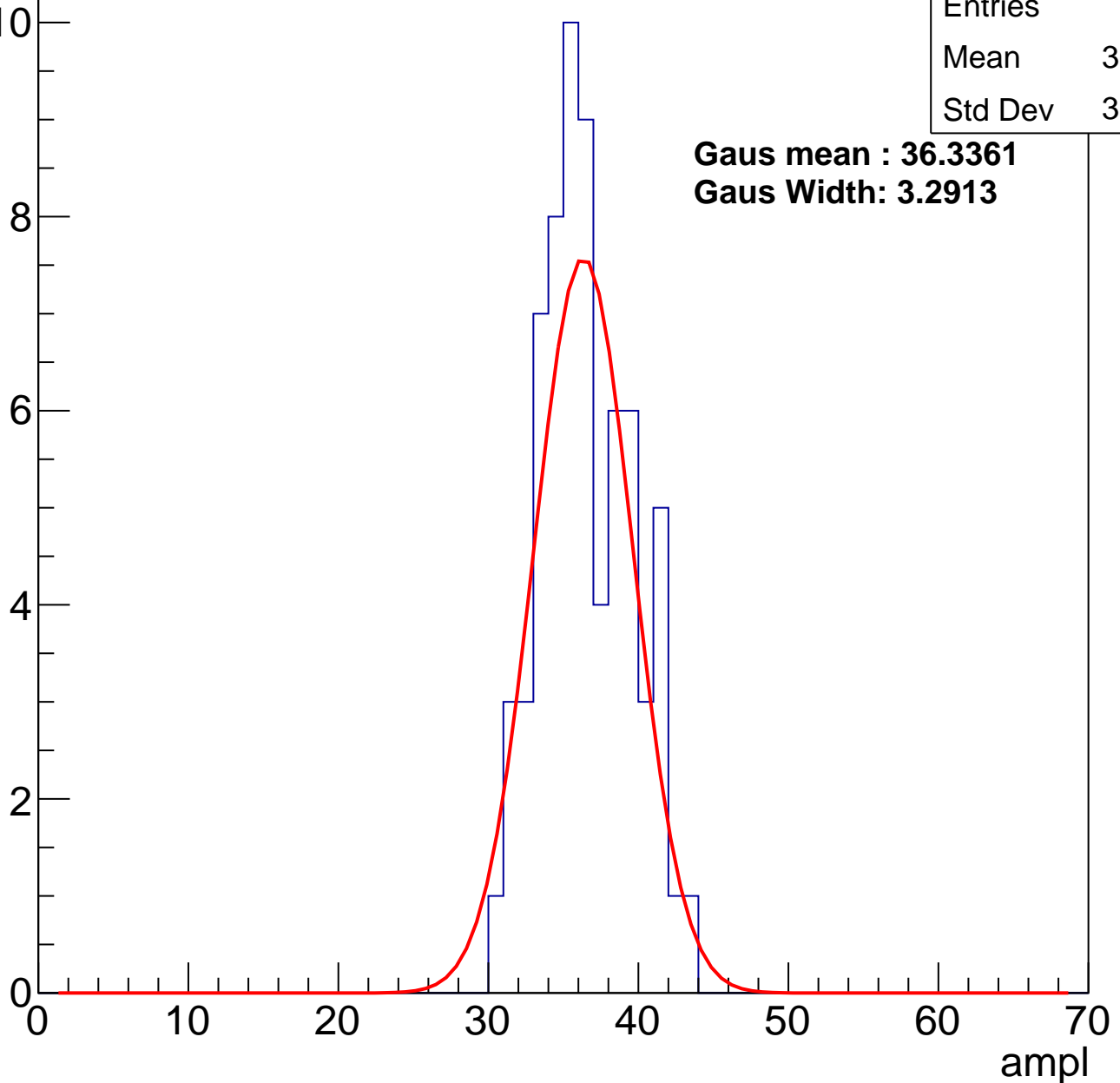
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	36.06
Std Dev	3.002

**Gaus mean : 36.3361**

**Gaus Width: 3.2913**



# B1L102S, U21-ch33, adc2

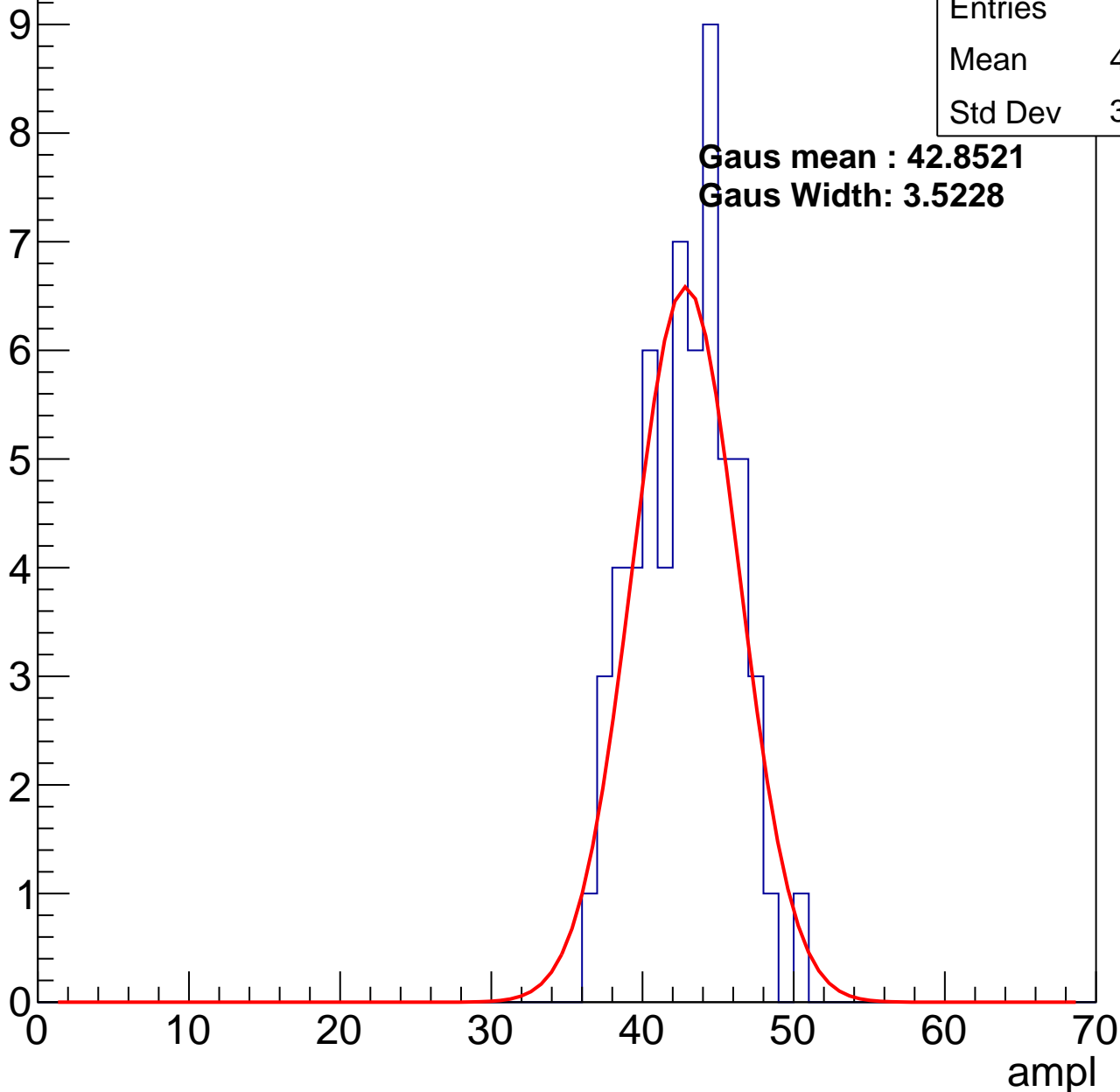
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	42.39
Std Dev	3.114

**Gaus mean : 42.8521**

**Gaus Width: 3.5228**



# B1L102S, U21-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	88
Mean	49.65
Std Dev	3.977

Entry

10

8

6

4

2

0

0

10

20

30

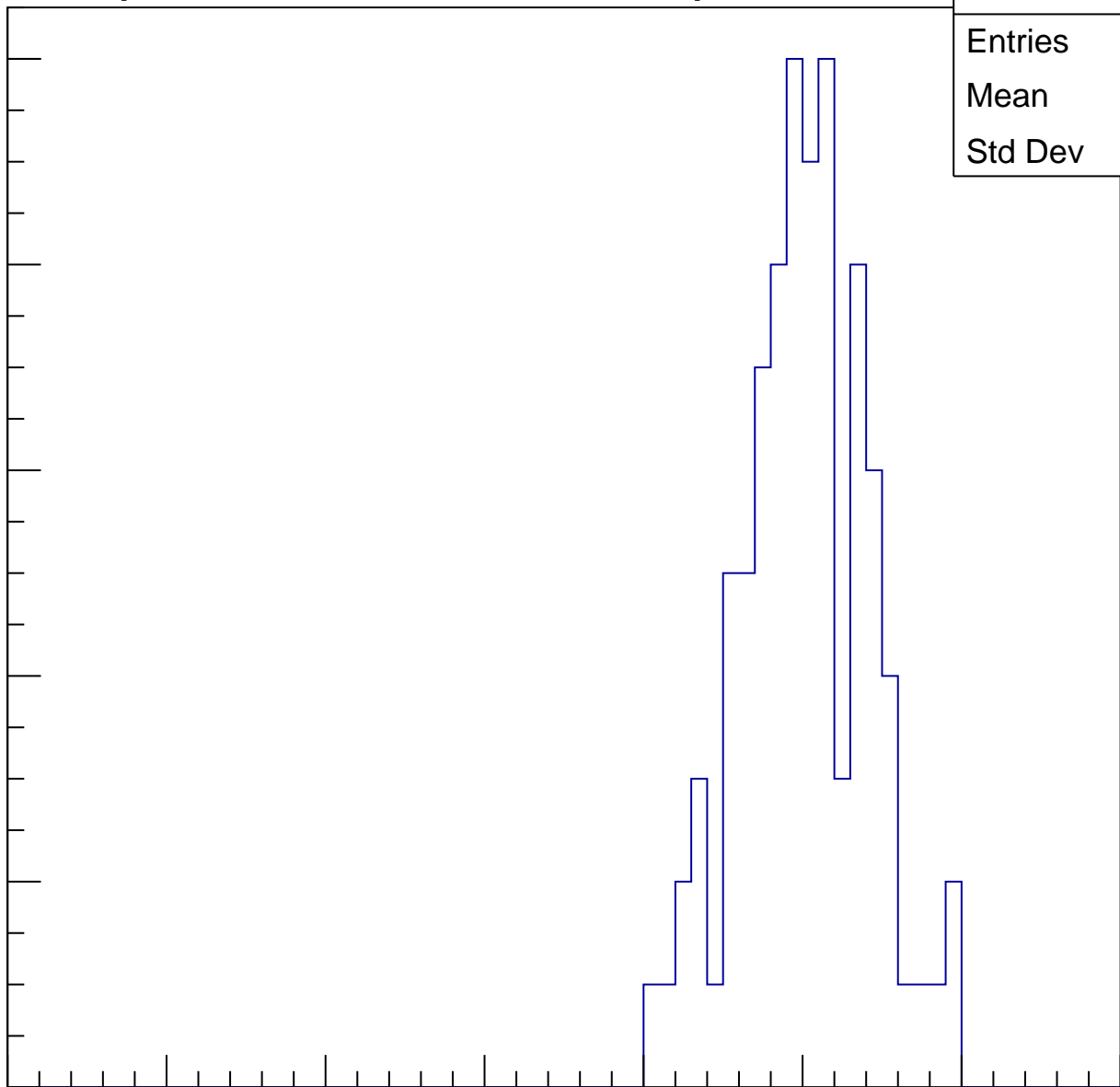
40

50

60

70

ampl

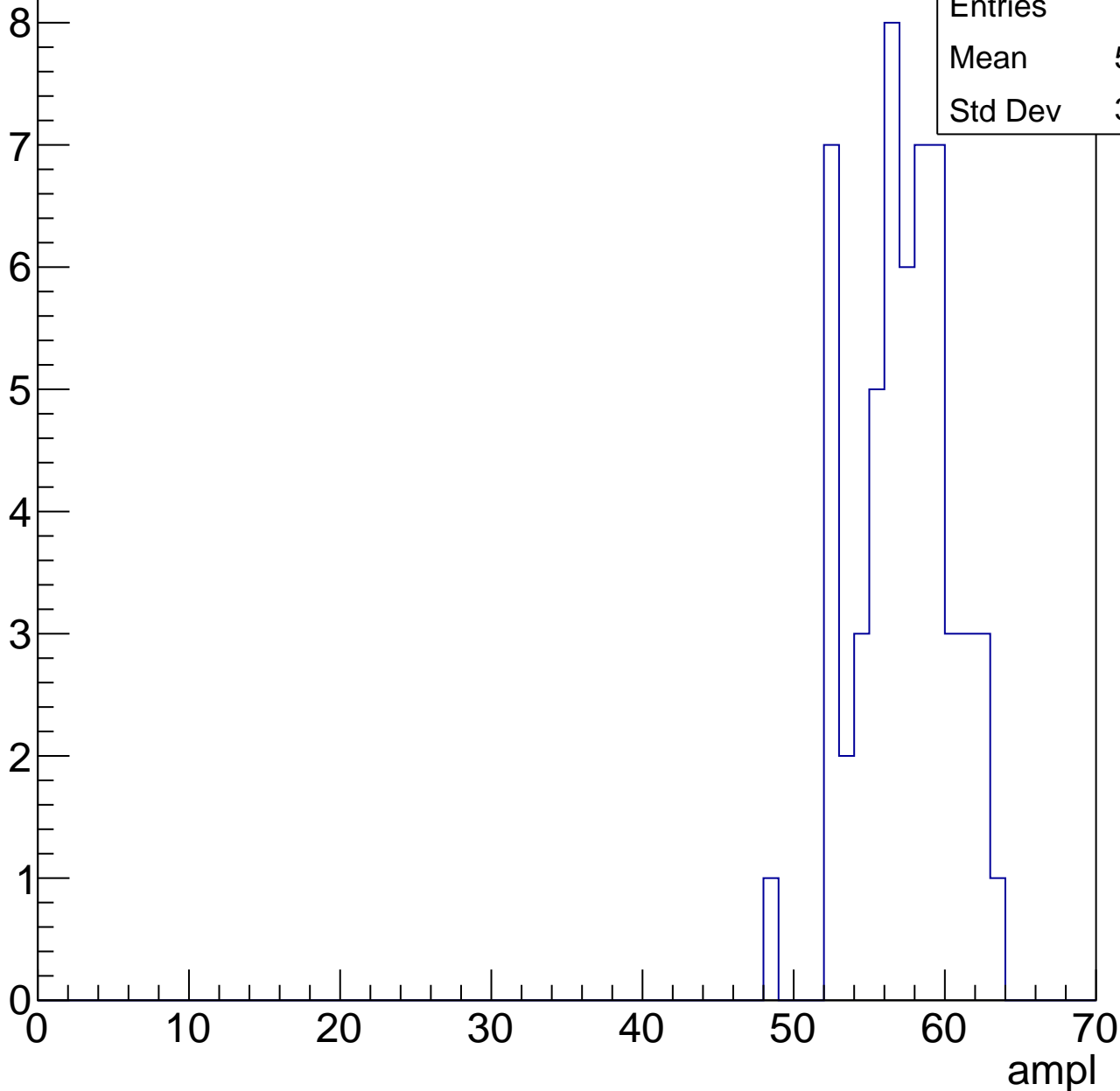


# B1L102S, U21-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	56.71
Std Dev	3.161



# B1L102S, U21-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

7

6

5

4

3

2

1

0

Entries 37

Mean 58.65

Std Dev 10.05

ampl

0

10

20

30

40

50

60

70

0

1

2

3

4

5

6

7

8

9

10

11

12

13

14

15

16

17

18

19

20

21

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# B1L102S, U21-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U21-ch34, adc0

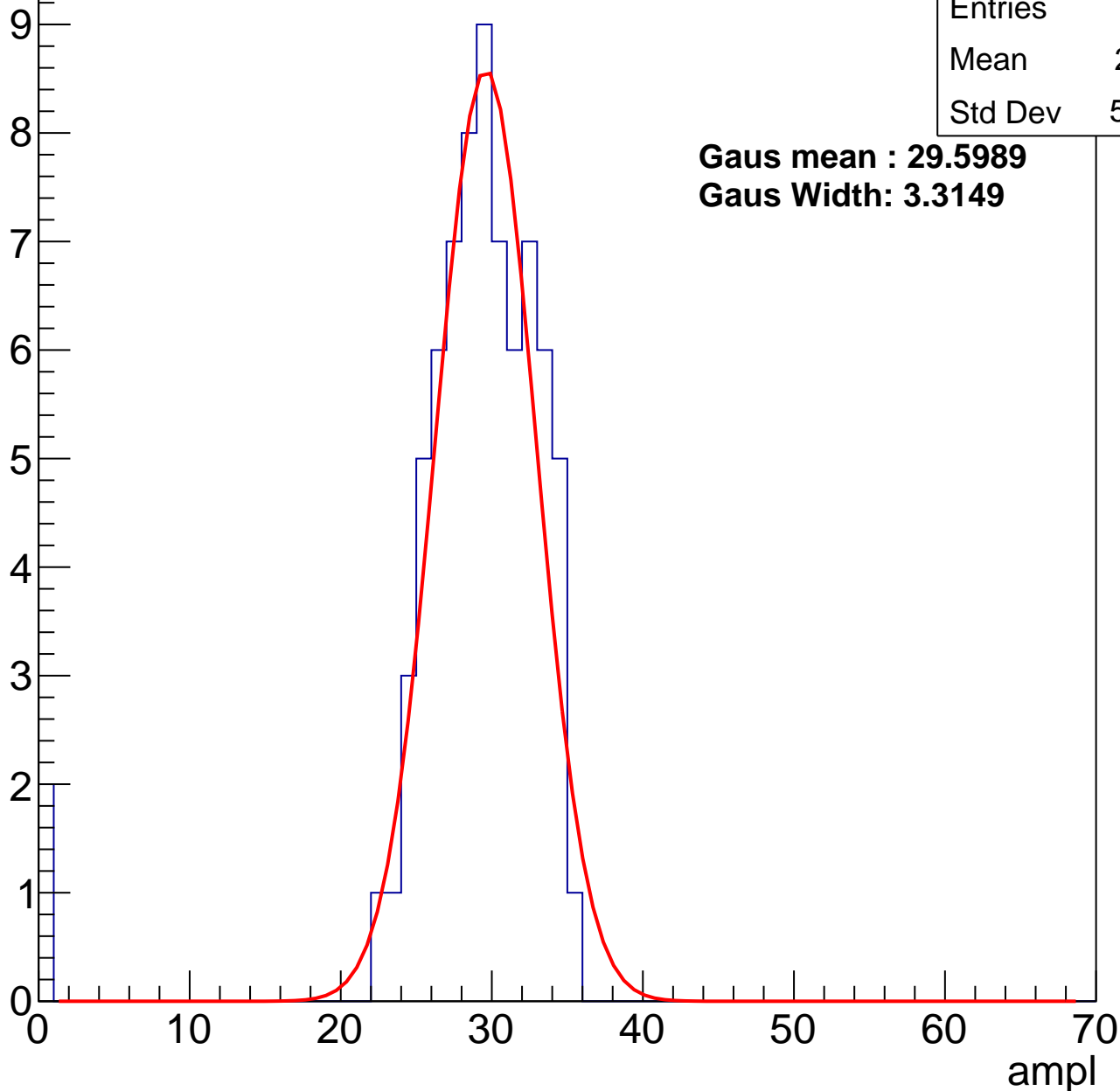
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	28.31
Std Dev	5.609

**Gaus mean : 29.5989**

**Gaus Width: 3.3149**



# B1L102S, U21-ch34, adc1

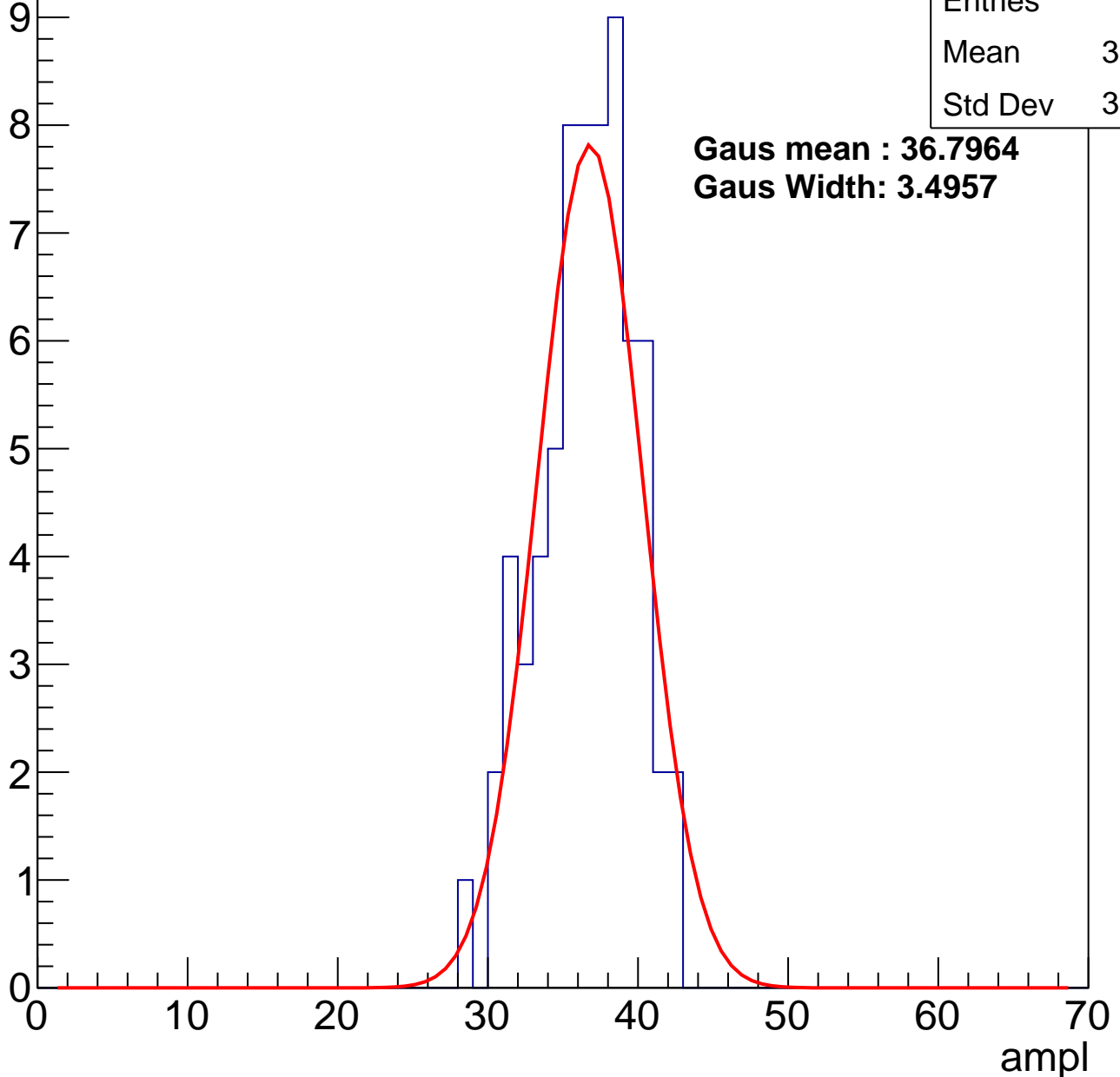
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	36.12
Std Dev	3.123

**Gaus mean : 36.7964**

**Gaus Width: 3.4957**



# B1L102S, U21-ch34, adc2

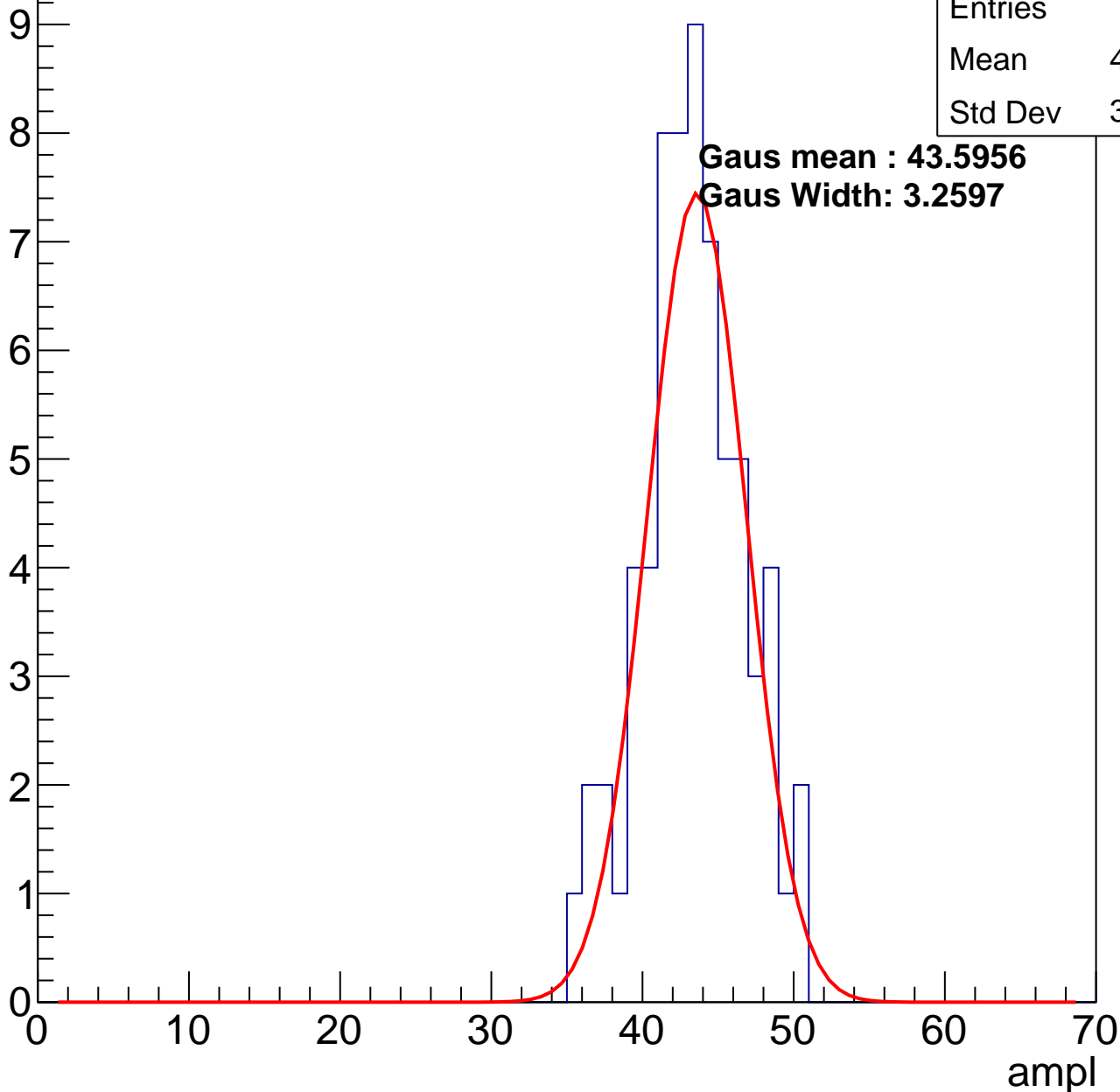
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	42.89
Std Dev	3.376

**Gaus mean : 43.5956**

**Gaus Width: 3.2597**

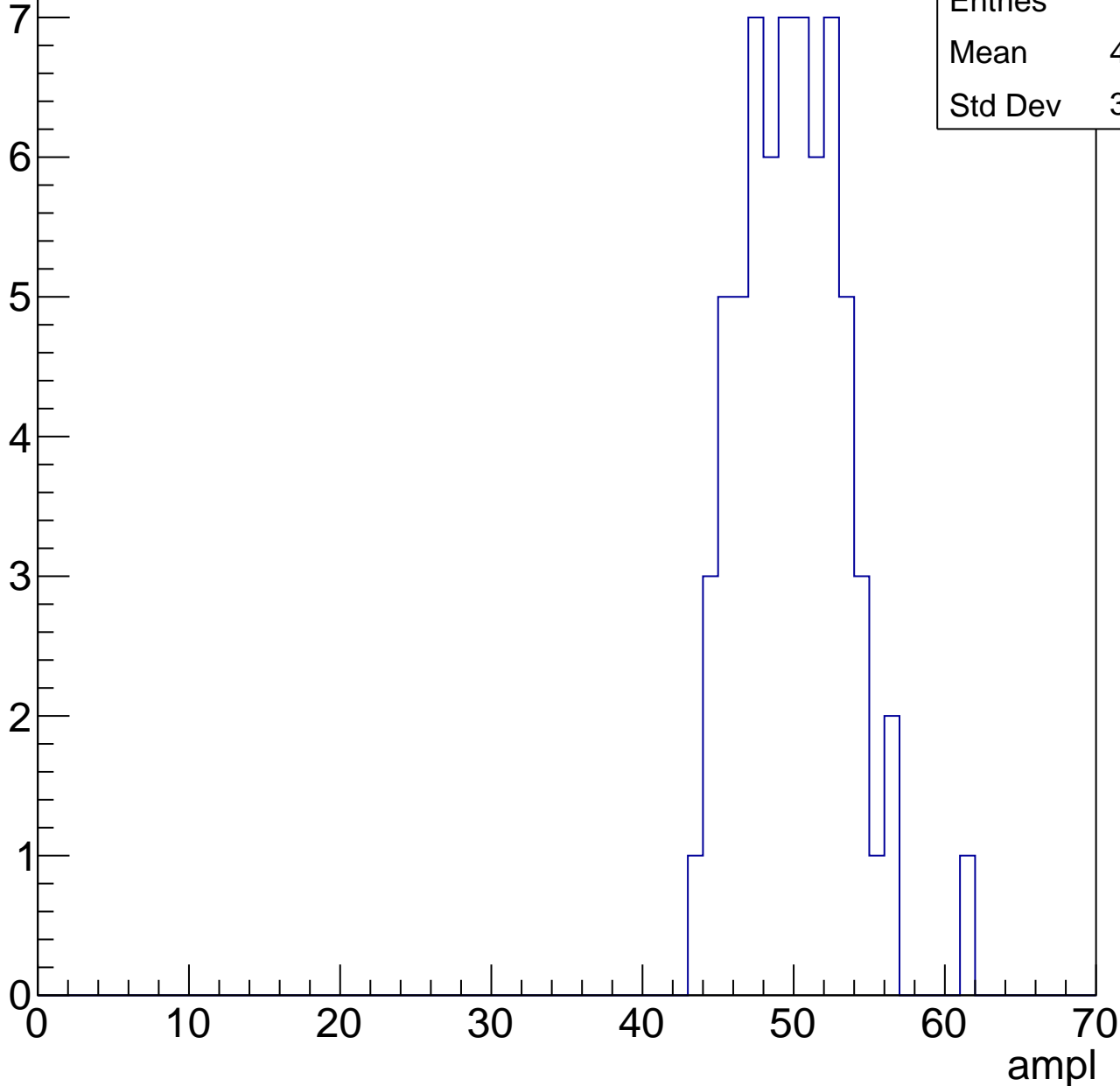


# B1L102S, U21-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	49.47
Std Dev	3.443

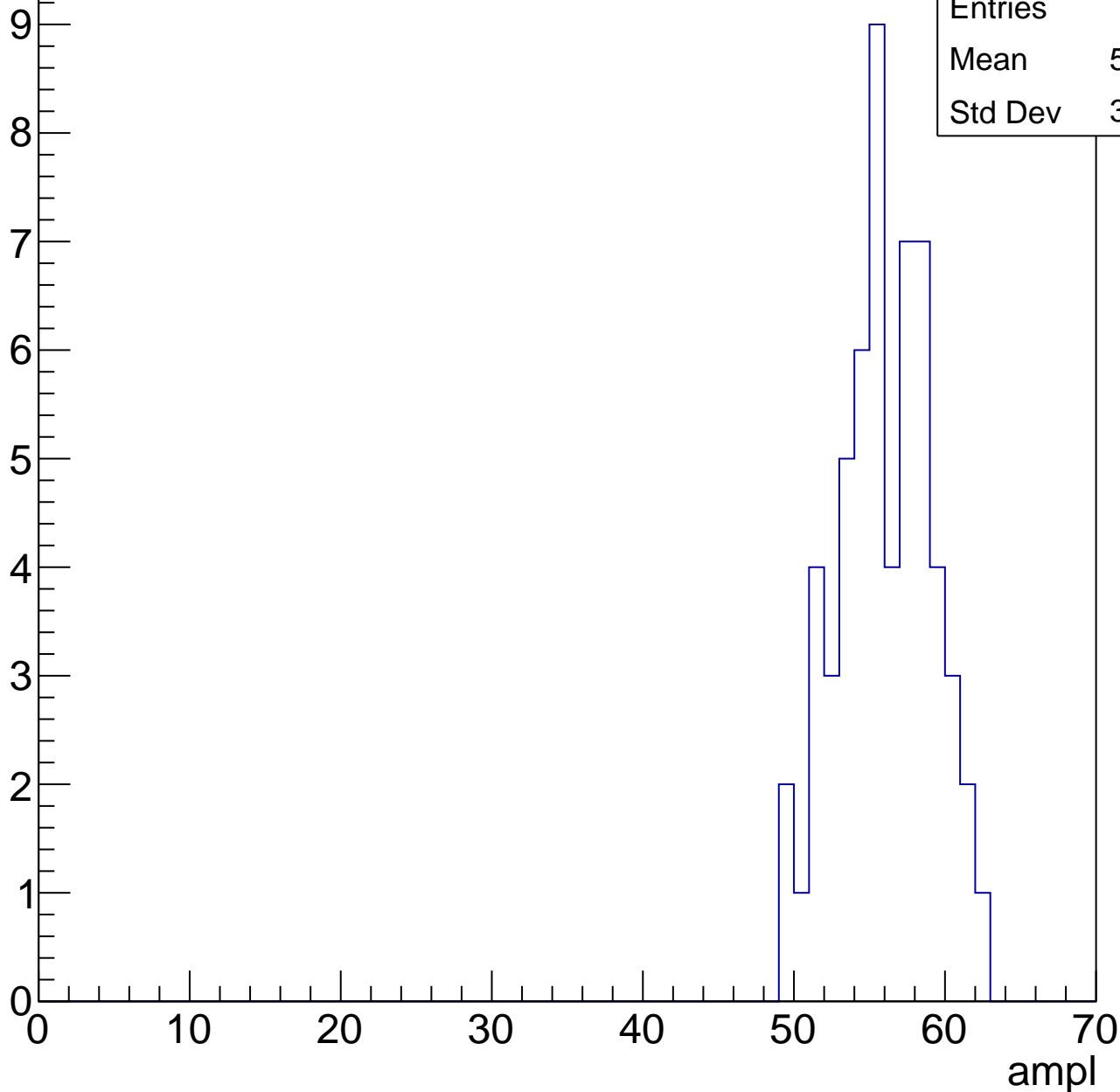


# B1L102S, U21-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	55.53
Std Dev	3.086

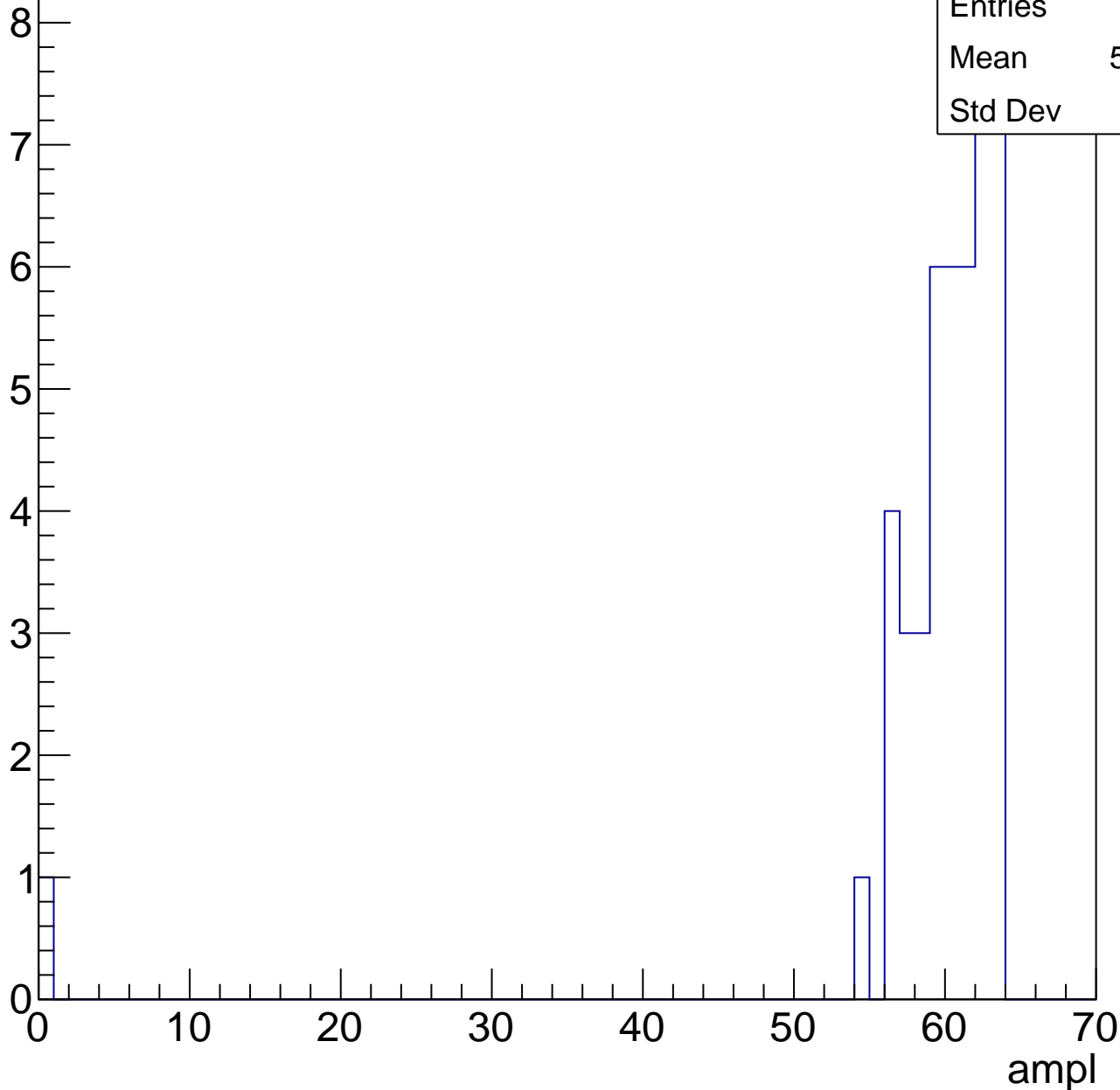


# B1L102S, U21-ch34, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	58.76
Std Dev	9.07



# B1L102S, U21-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

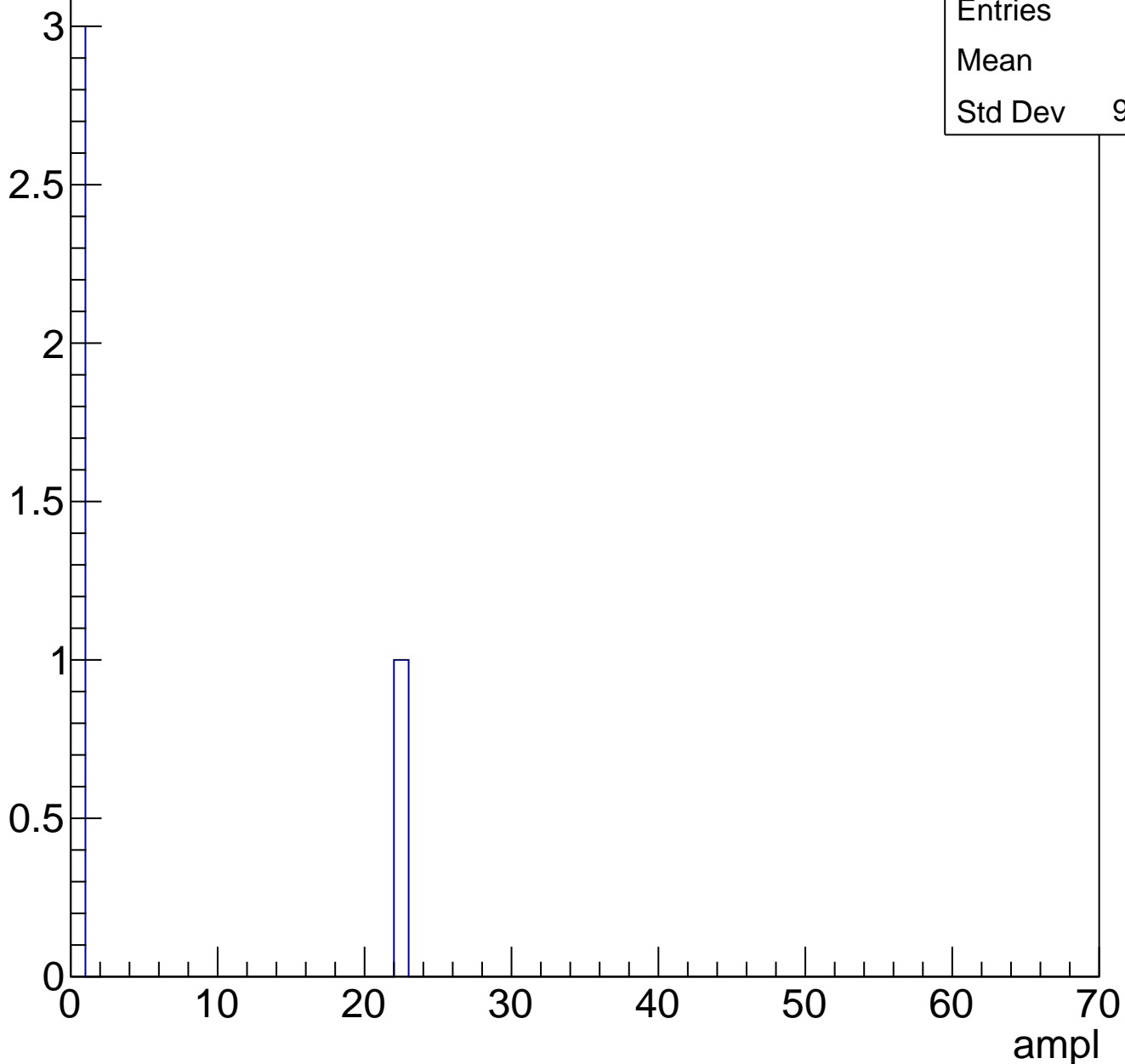




# B1L102S, U21-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	4
Mean	5.5
Std Dev	9.526

# B1L102S, U21-ch35, adc0

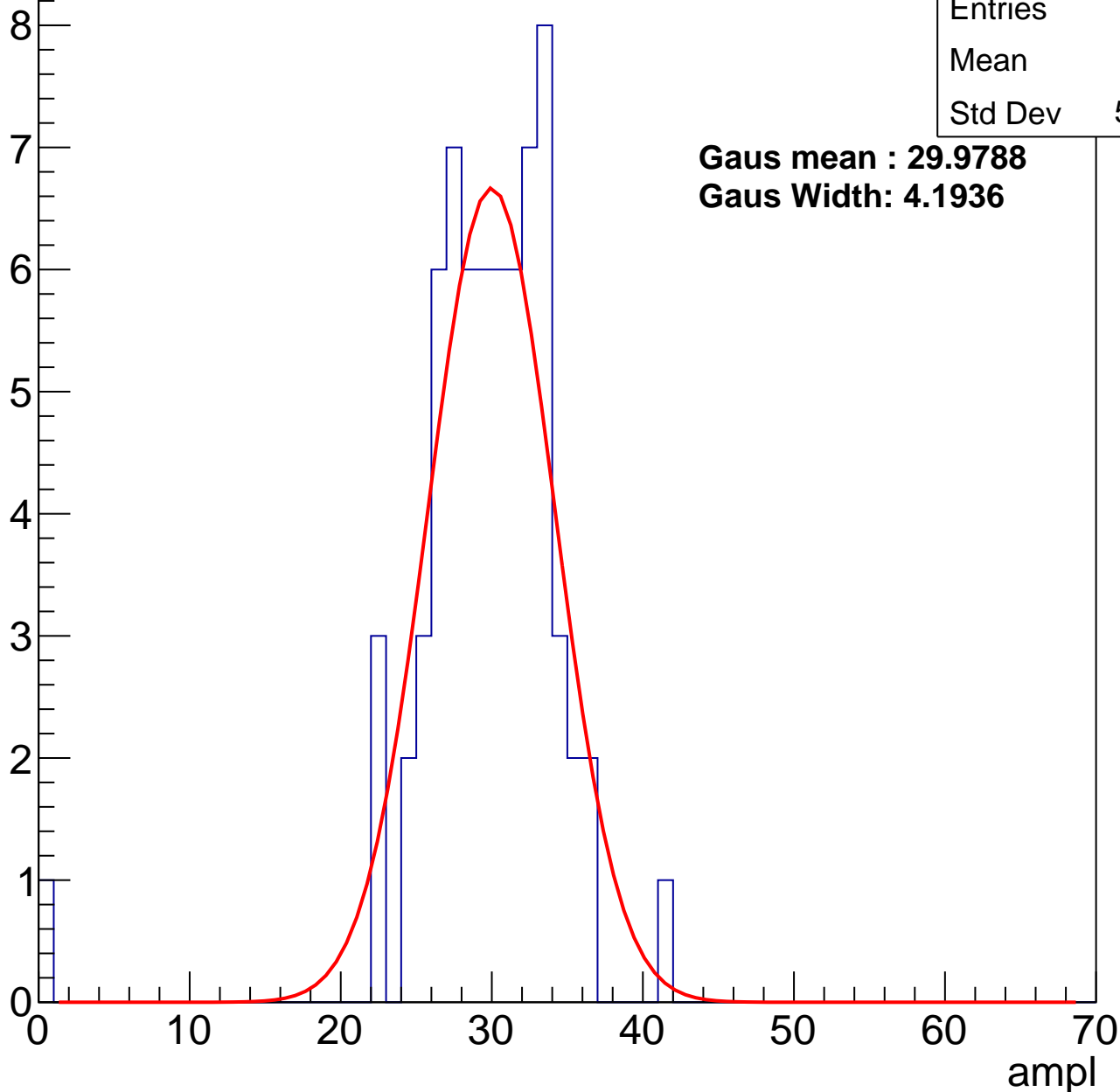
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	29.2
Std Dev	5.081

**Gaus mean : 29.9788**

**Gaus Width: 4.1936**



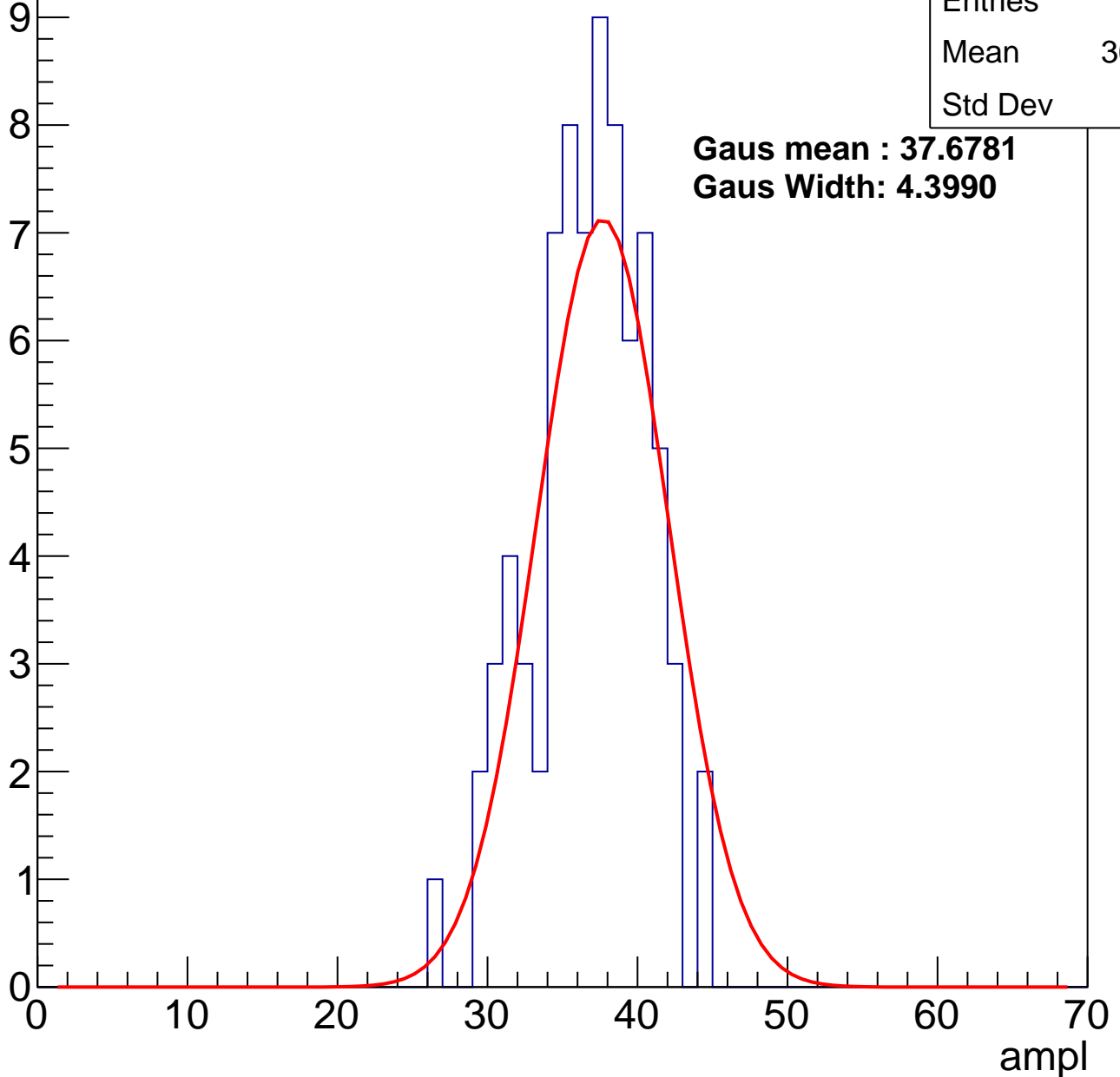
# B1L102S, U21-ch35, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	36.36
Std Dev	3.72

**Gaus mean : 37.6781**  
**Gaus Width: 4.3990**



# B1L102S, U21-ch35, adc2

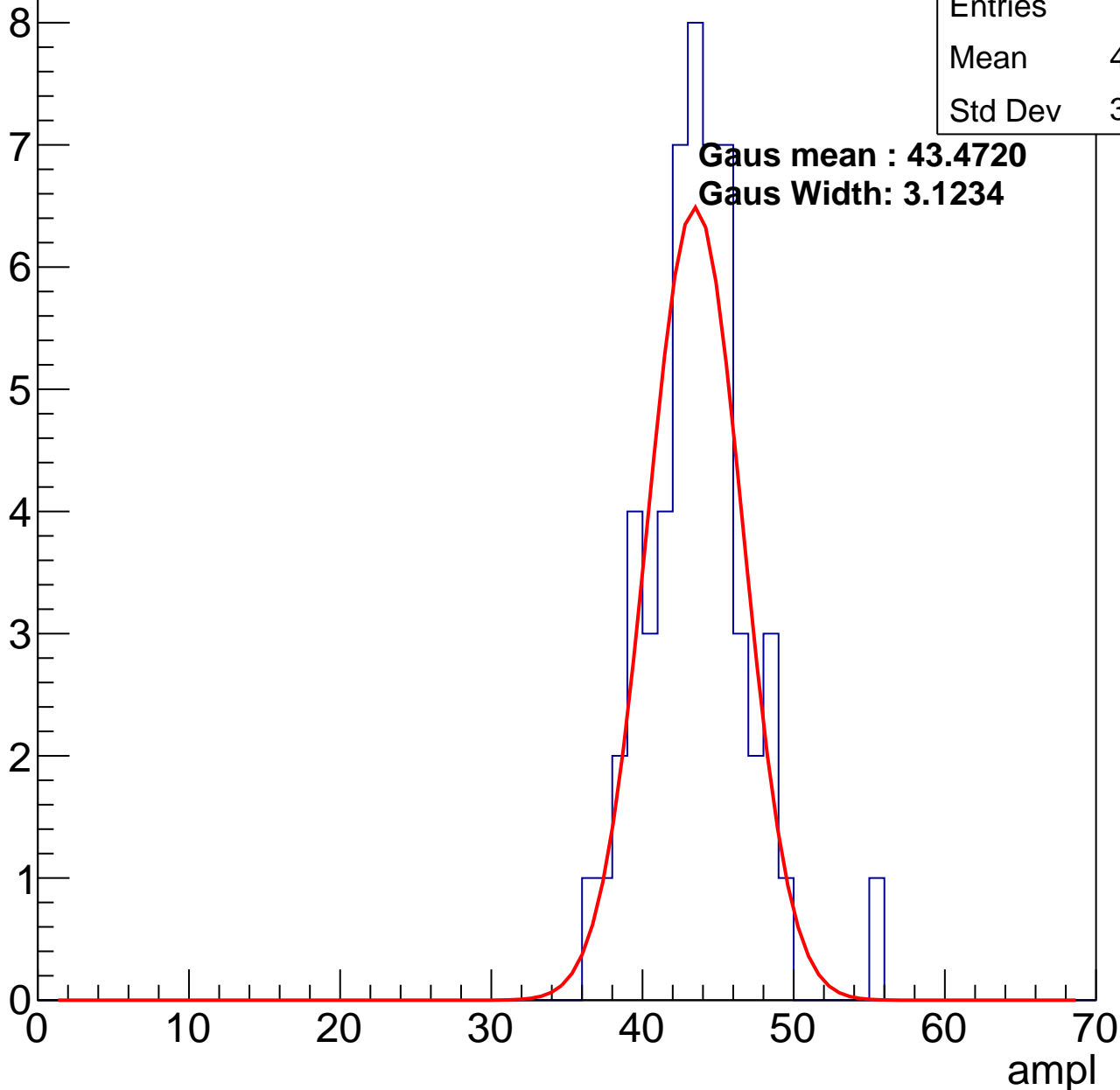
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	43.15
Std Dev	3.324

**Gaus mean : 43.4720**

**Gaus Width: 3.1234**

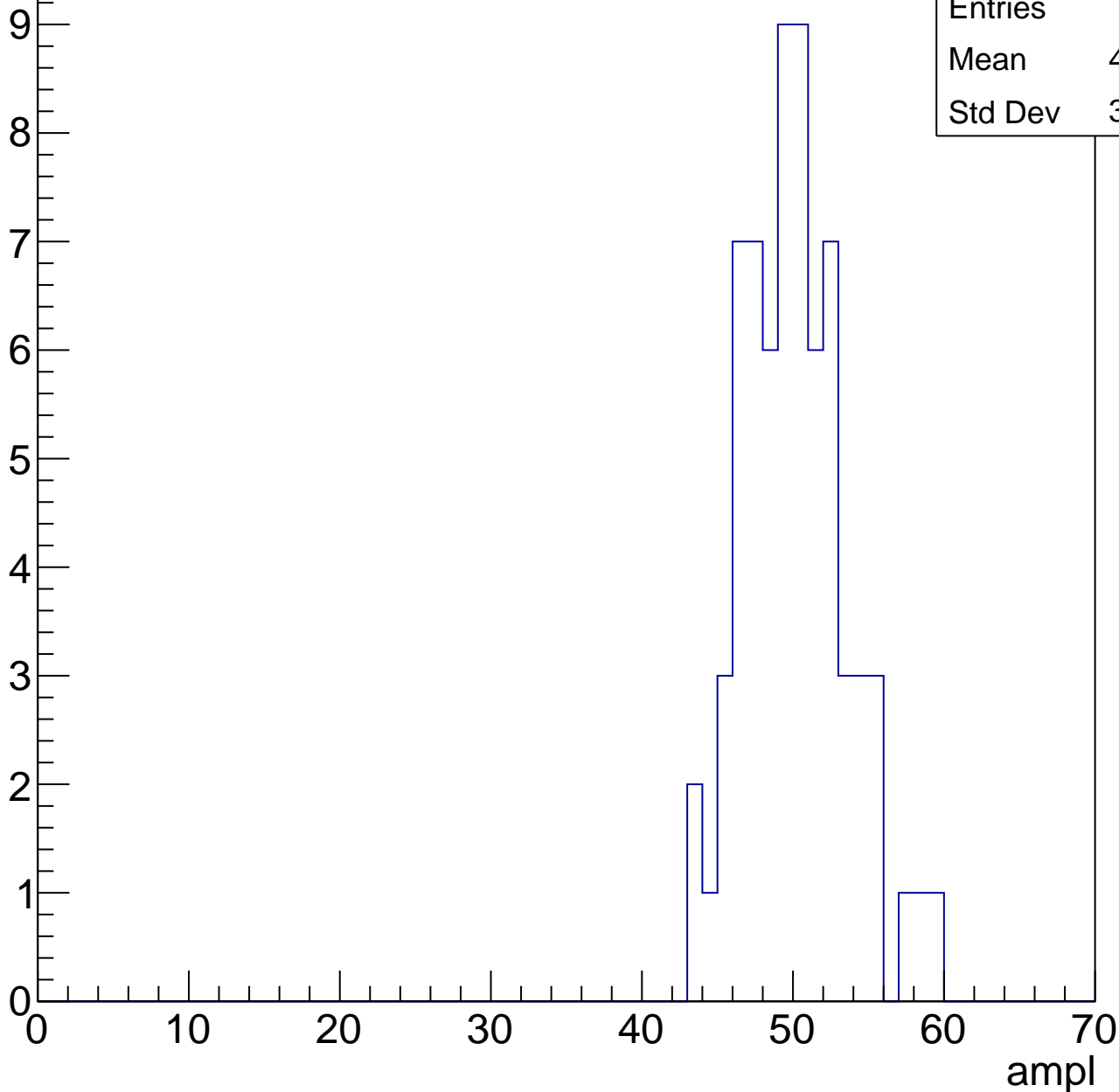


# B1L102S, U21-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	49.64
Std Dev	3.375

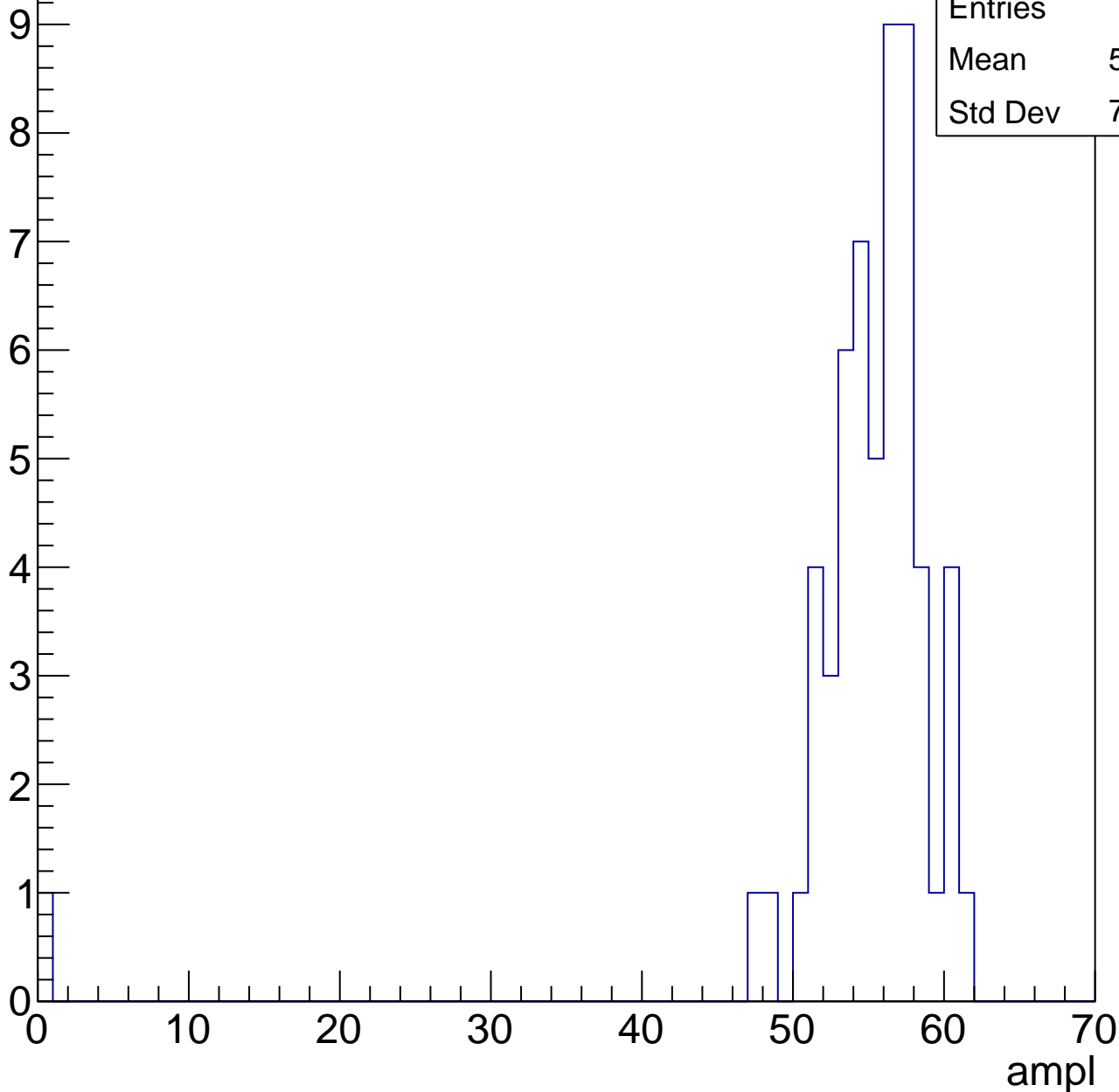


# B1L102S, U21-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

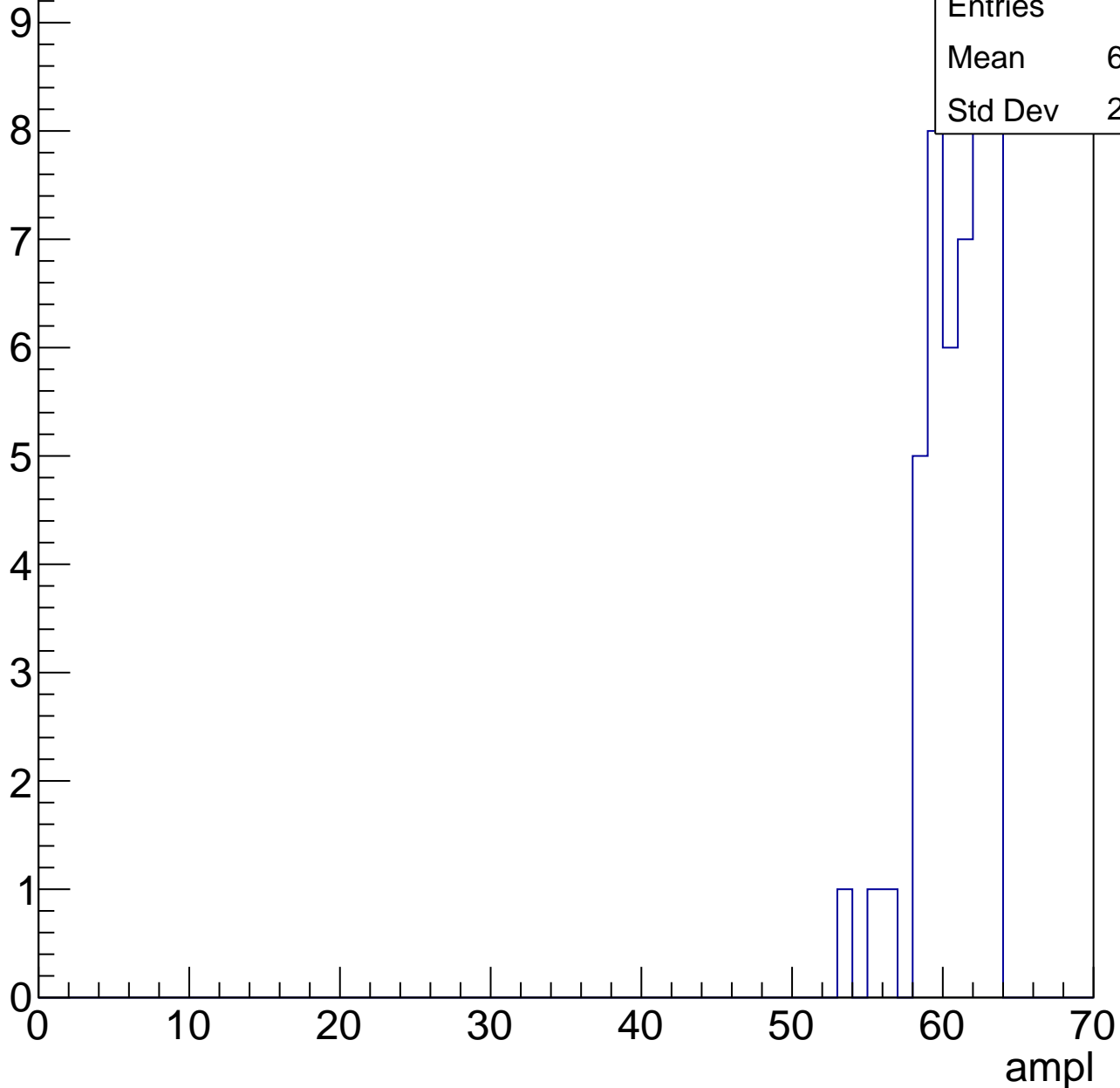
Entries	57
Mean	54.12
Std Dev	7.807



# B1L102S, U21-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	61.5
Std Dev	0.5

0 10 20 30 40 50 60 70

ampl



# B1L102S, U21-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch36, adc0

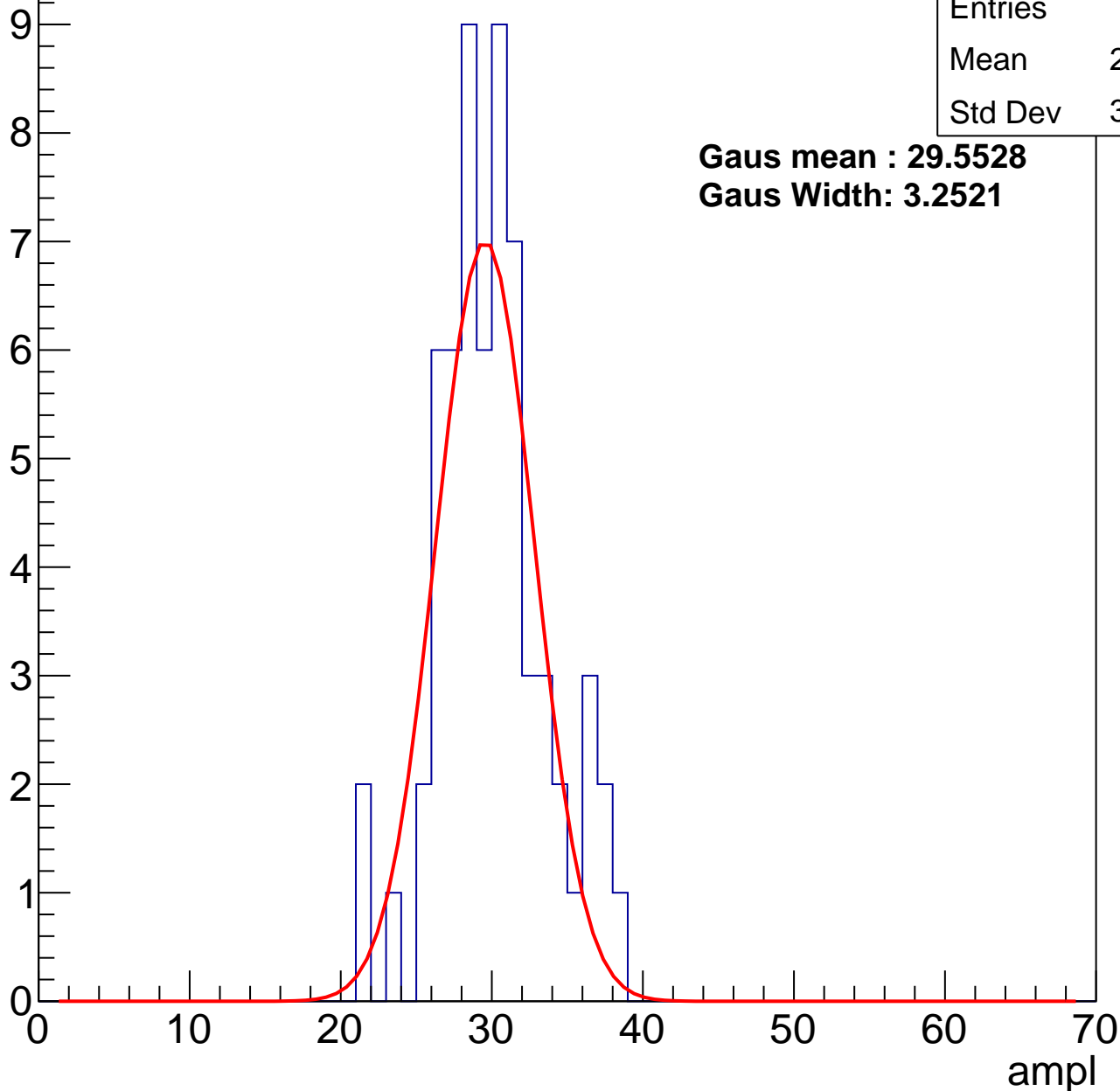
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	29.59
Std Dev	3.597

**Gaus mean : 29.5528**

**Gaus Width: 3.2521**



# B1L102S, U21-ch36, adc1

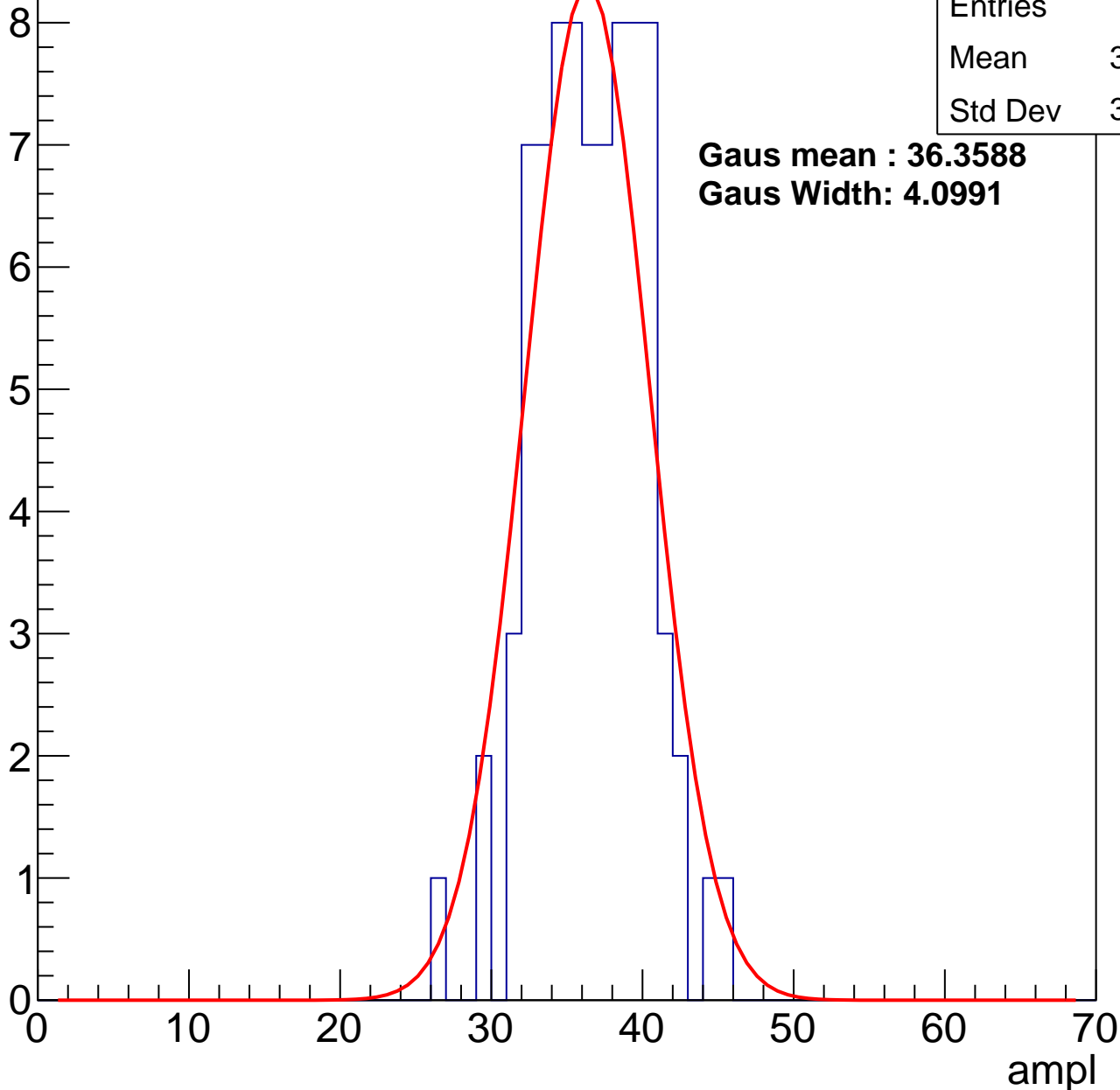
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	81
Mean	36.14
Std Dev	3.544

**Gaus mean : 36.3588**

**Gaus Width: 4.0991**



# B1L102S, U21-ch36, adc2

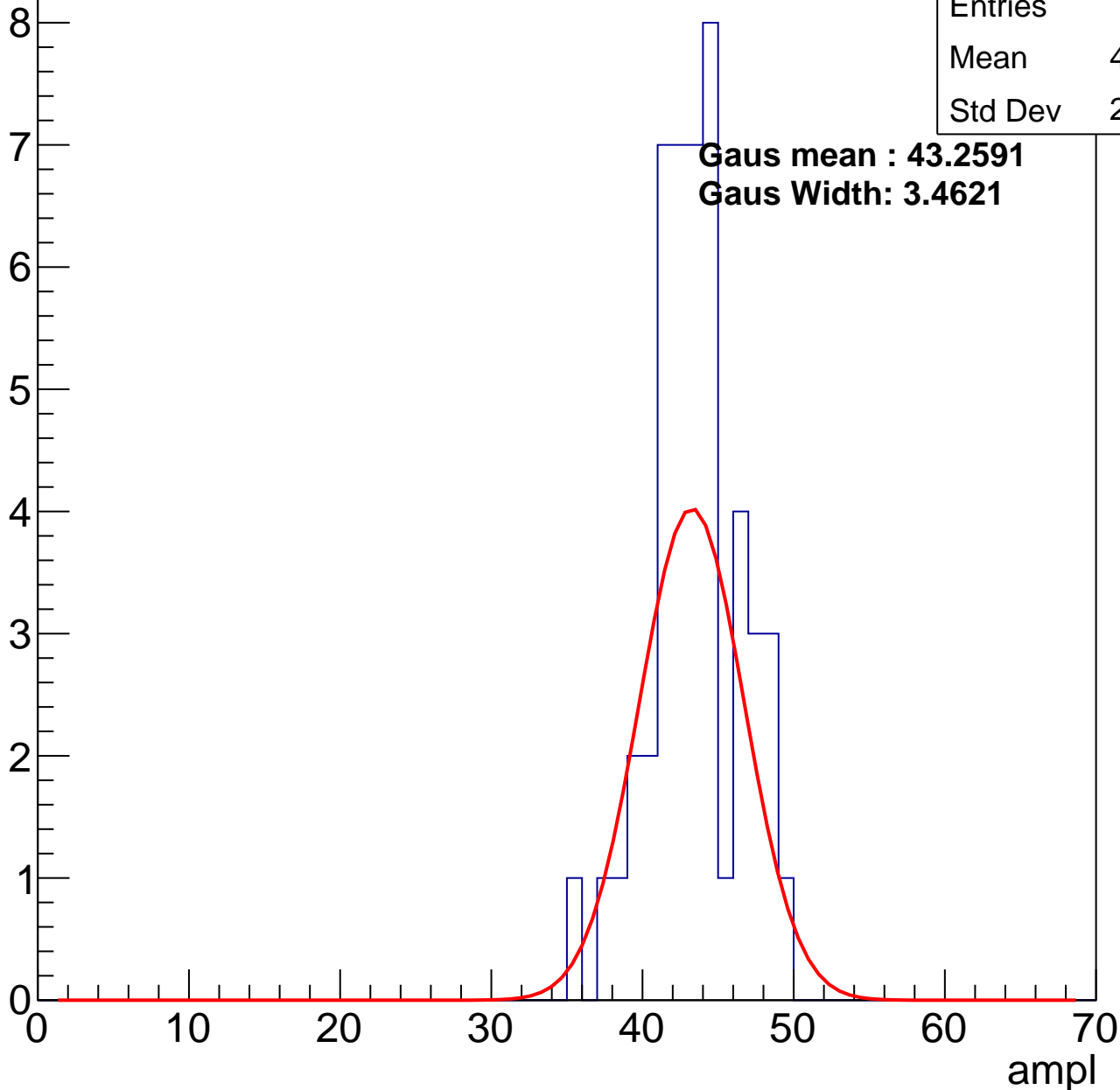
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	43.02
Std Dev	2.947

**Gaus mean : 43.2591**

**Gaus Width: 3.4621**

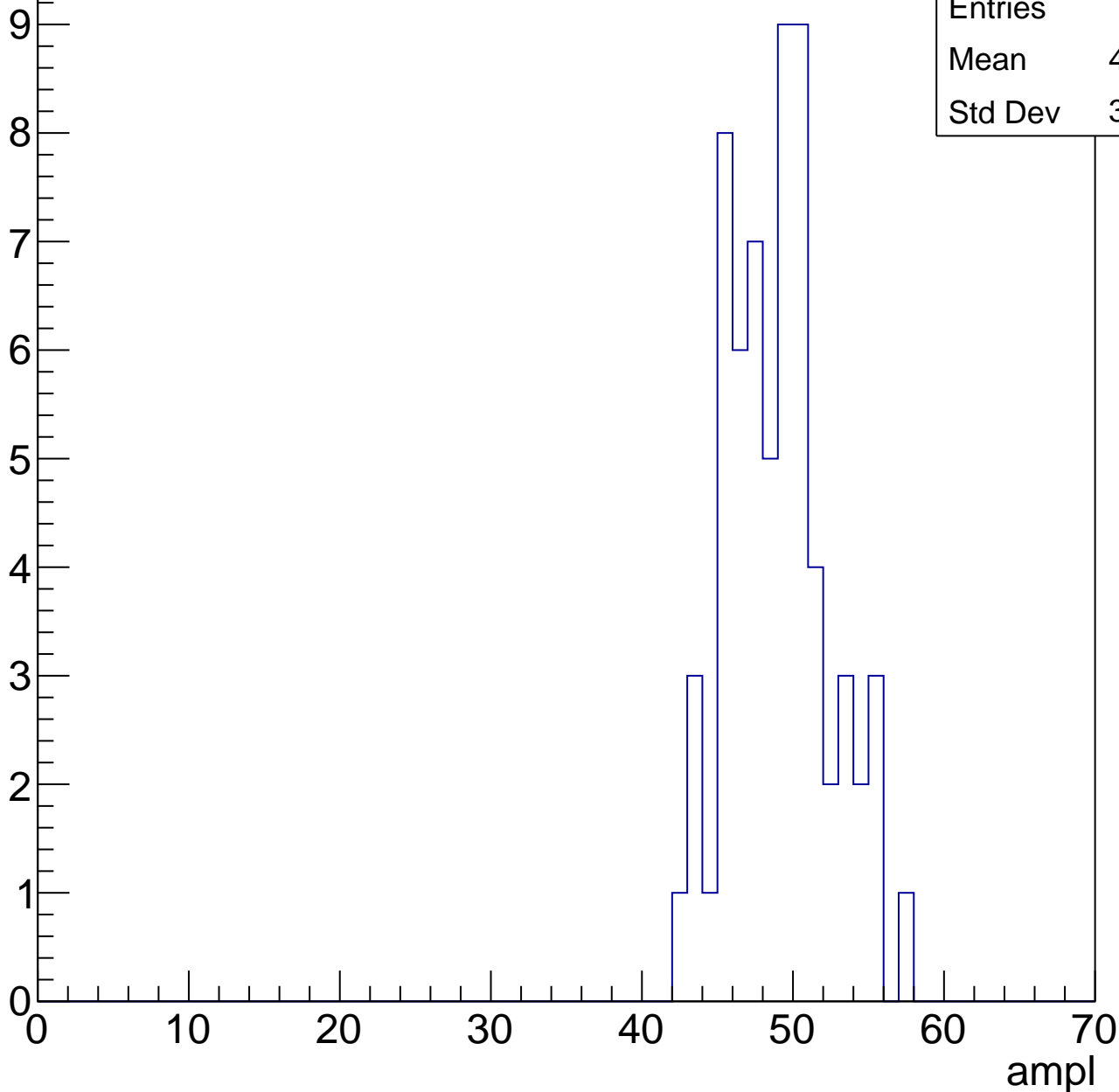


# B1L102S, U21-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	48.56
Std Dev	3.302

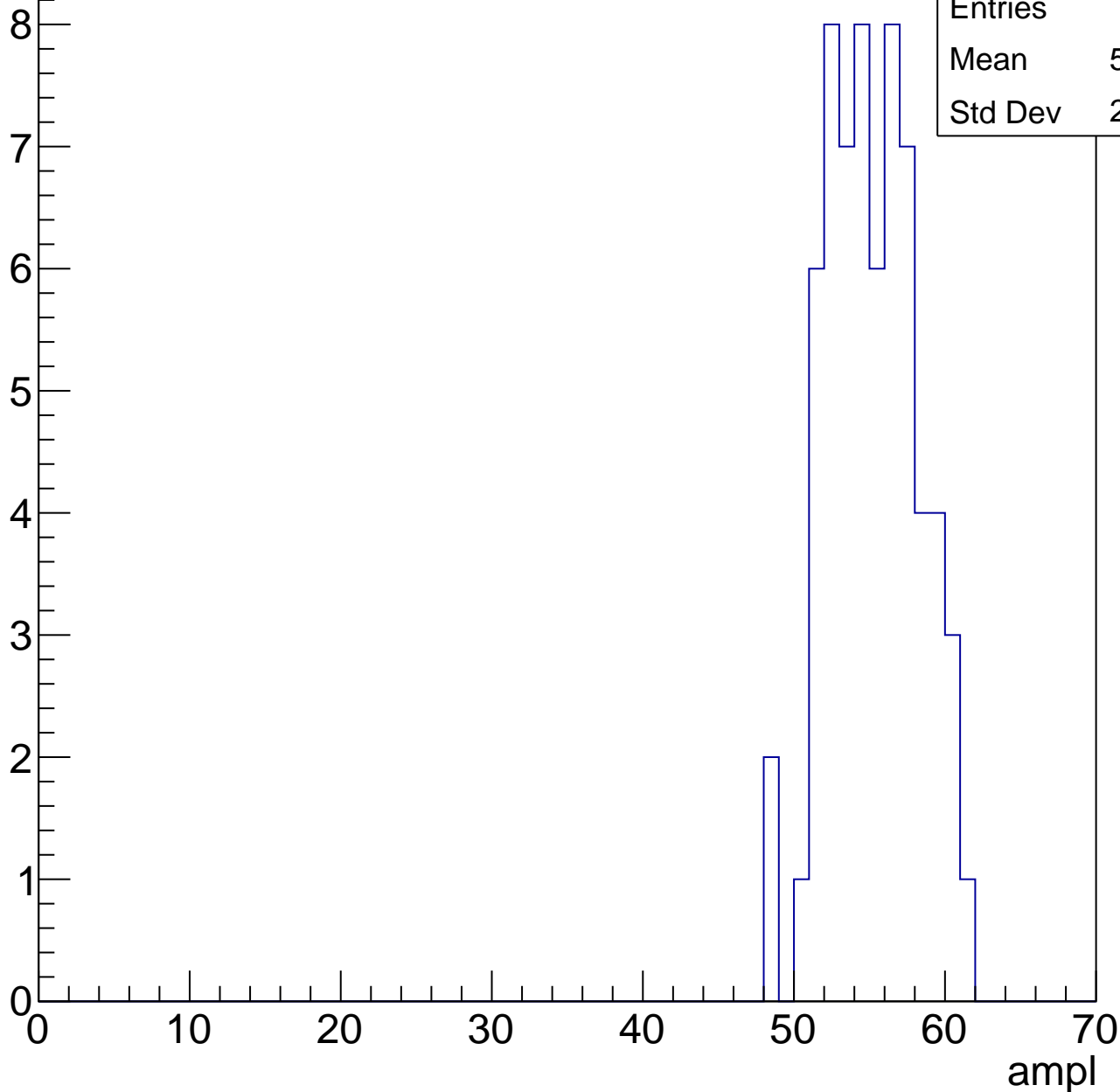


# B1L102S, U21-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	54.72
Std Dev	2.959

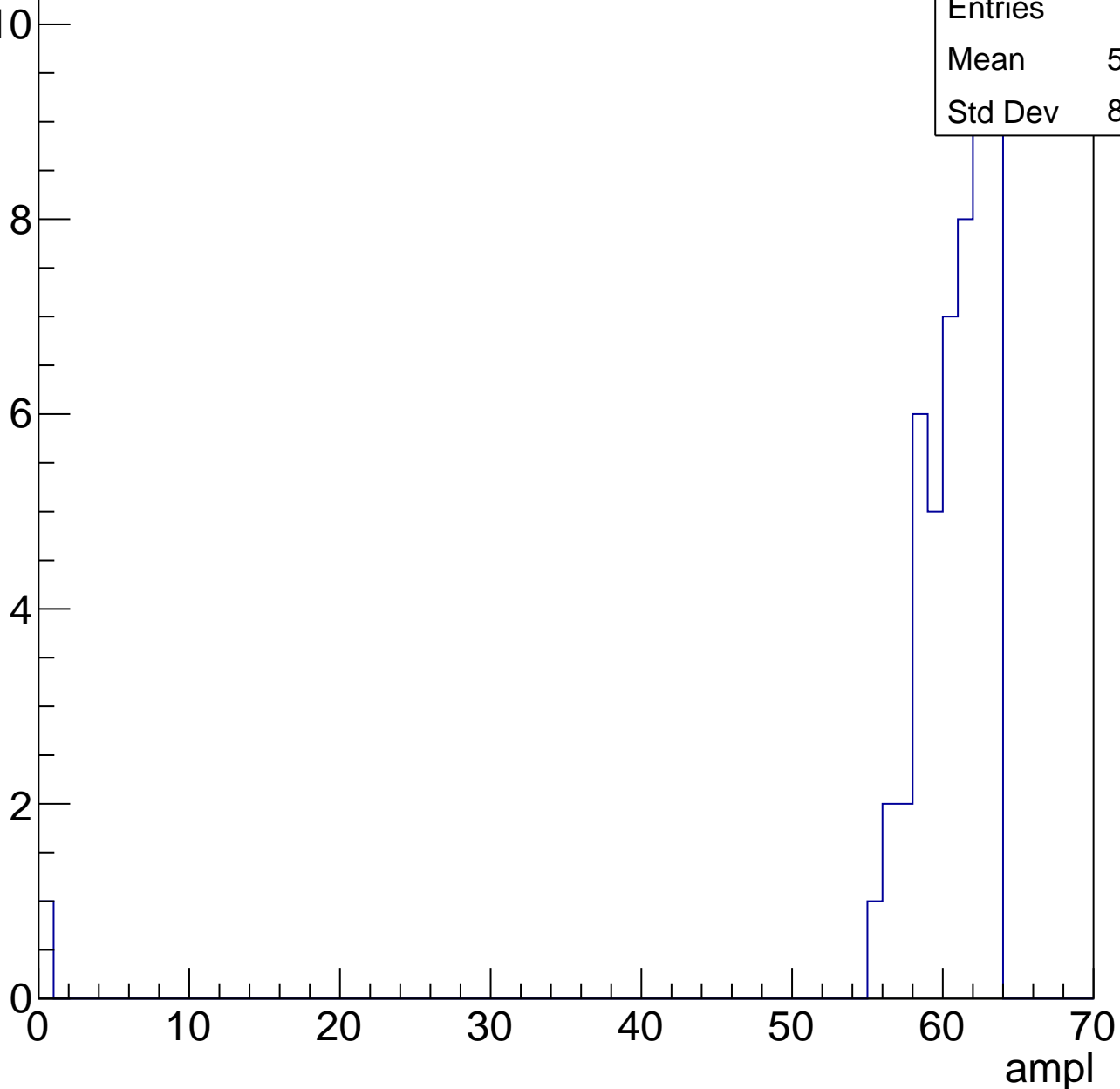


# B1L102S, U21-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

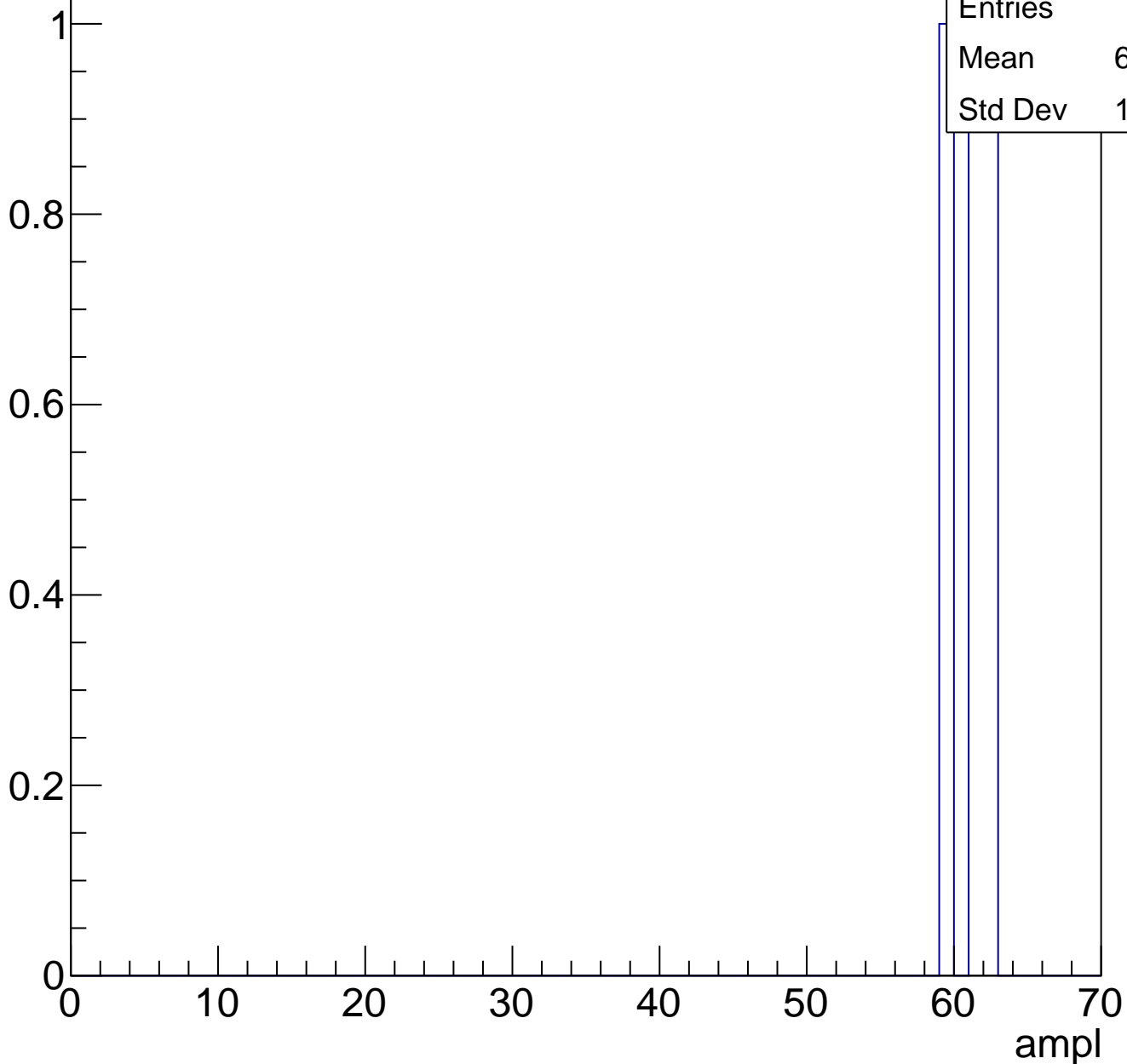
Entries	51
Mean	59.22
Std Dev	8.639



# B1L102S, U21-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U21-ch37, adc0

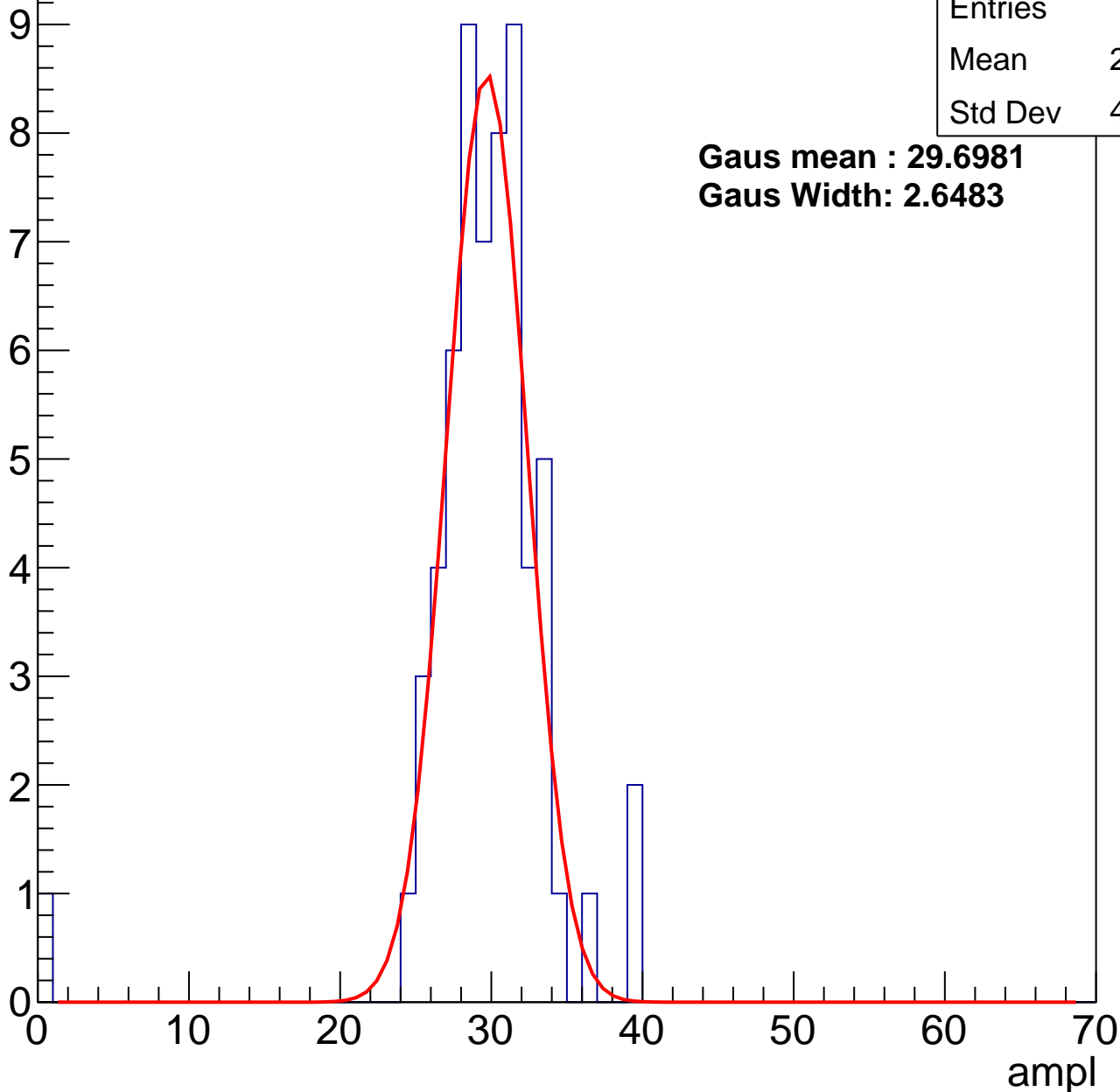
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	29.18
Std Dev	4.816

**Gaus mean : 29.6981**

**Gaus Width: 2.6483**



# B1L102S, U21-ch37, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	36.39
Std Dev	3.443

**Gaus mean : 36.6156**

**Gaus Width: 2.7967**

10

8

6

4

2

0

0

10

20

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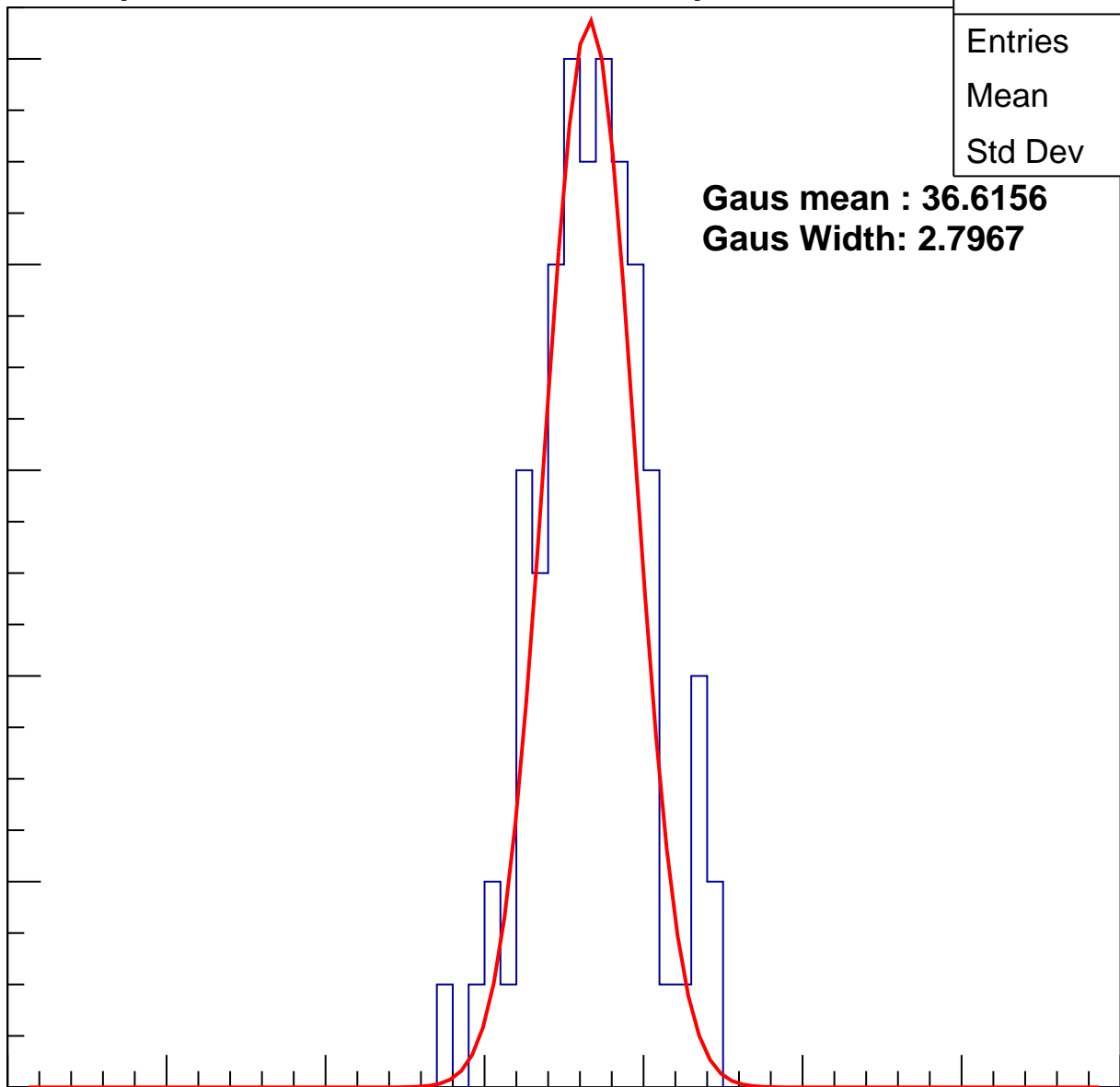
40

50

60

70

ampl



# B1L102S, U21-ch37, adc2

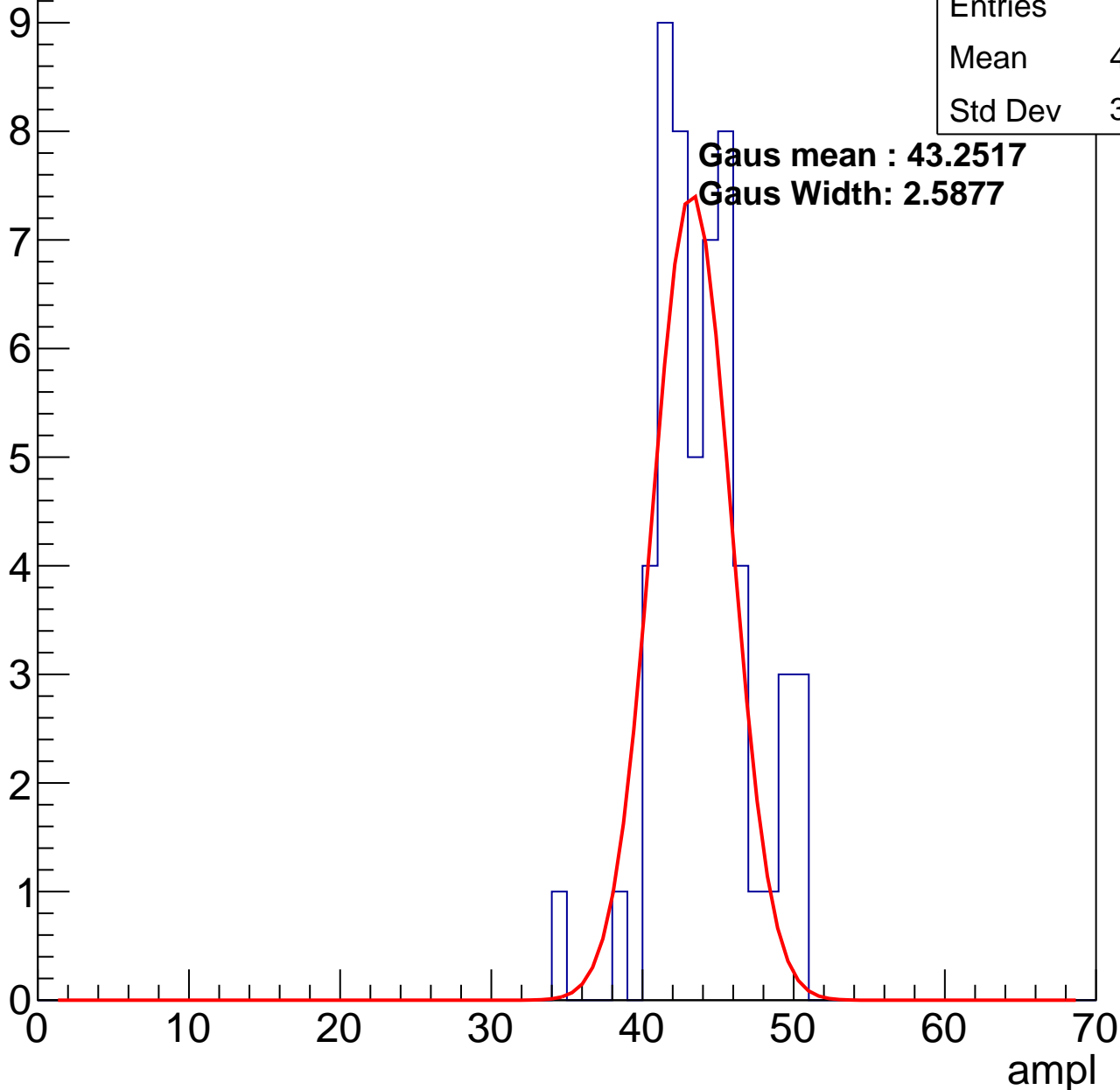
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	43.56
Std Dev	3.132

**Gaus mean : 43.2517**

**Gaus Width: 2.5877**

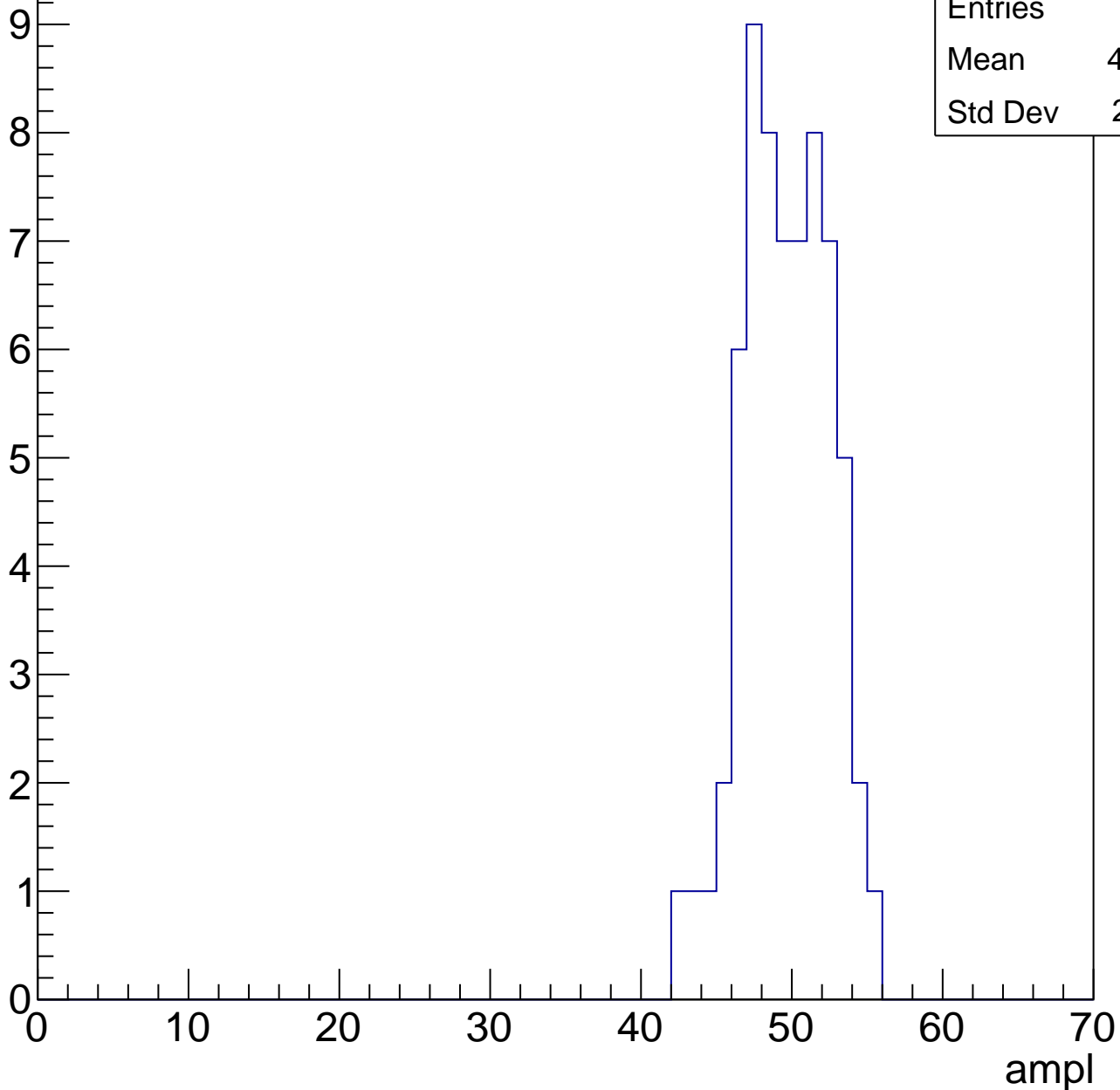


# B1L102S, U21-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	49.15
Std Dev	2.791

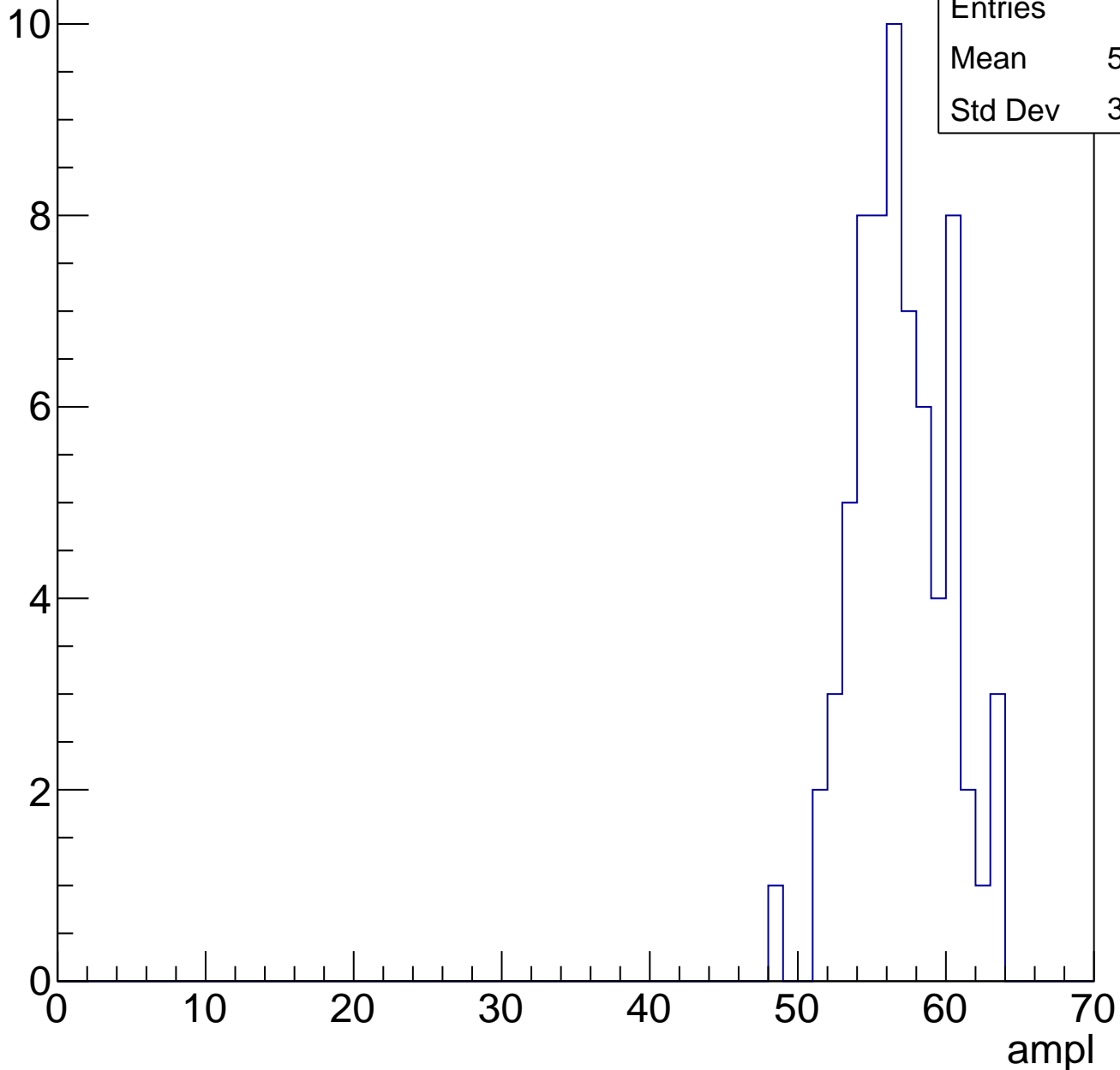


# B1L102S, U21-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	68
Mean	56.46
Std Dev	3.117

Entry

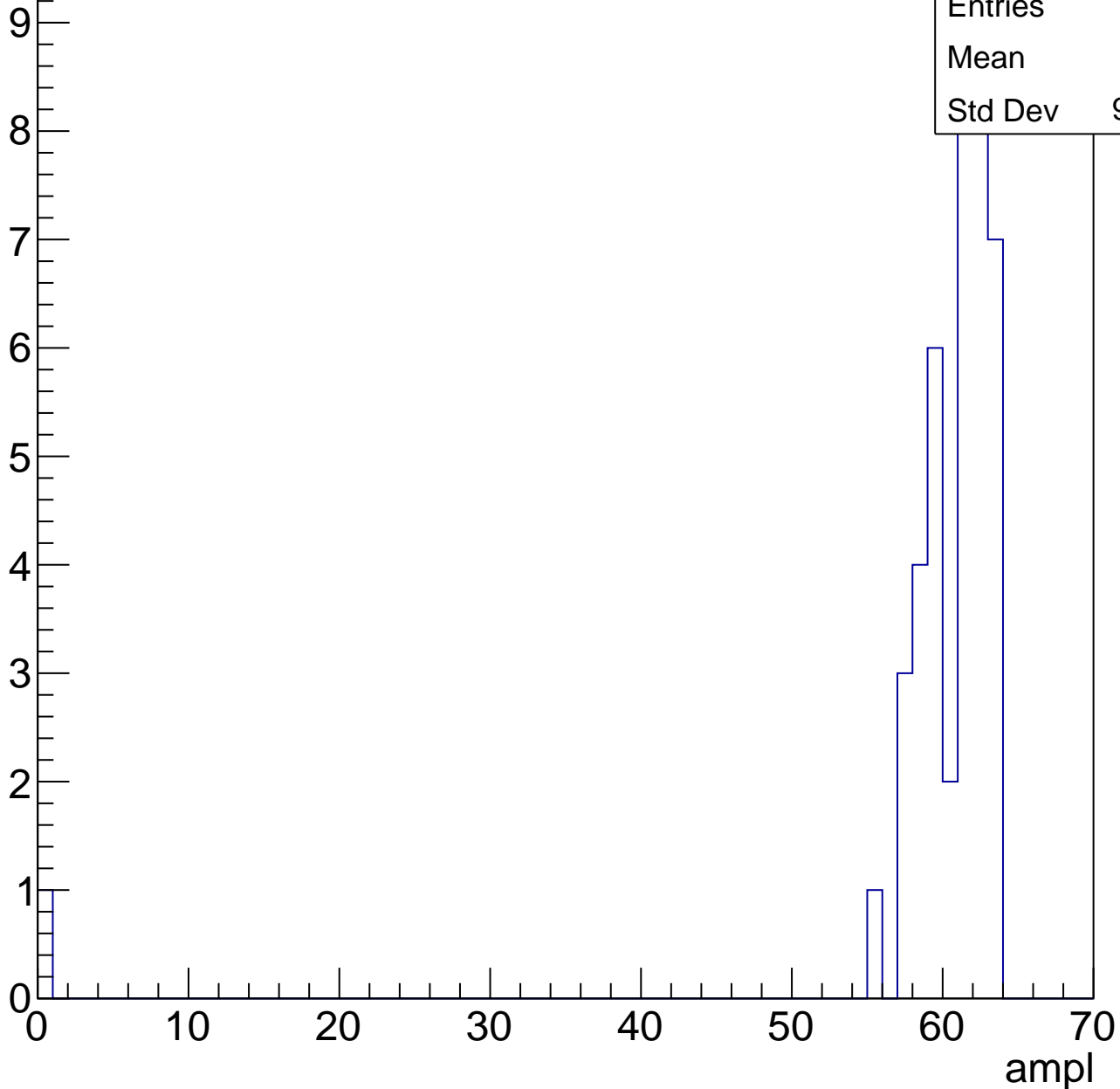


# B1L102S, U21-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	41
Mean	59
Std Dev	9.551



# B1L102S, U21-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L102S, U21-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	12
Std Dev	12

ampl

# B1L102S, U21-ch38, adc0

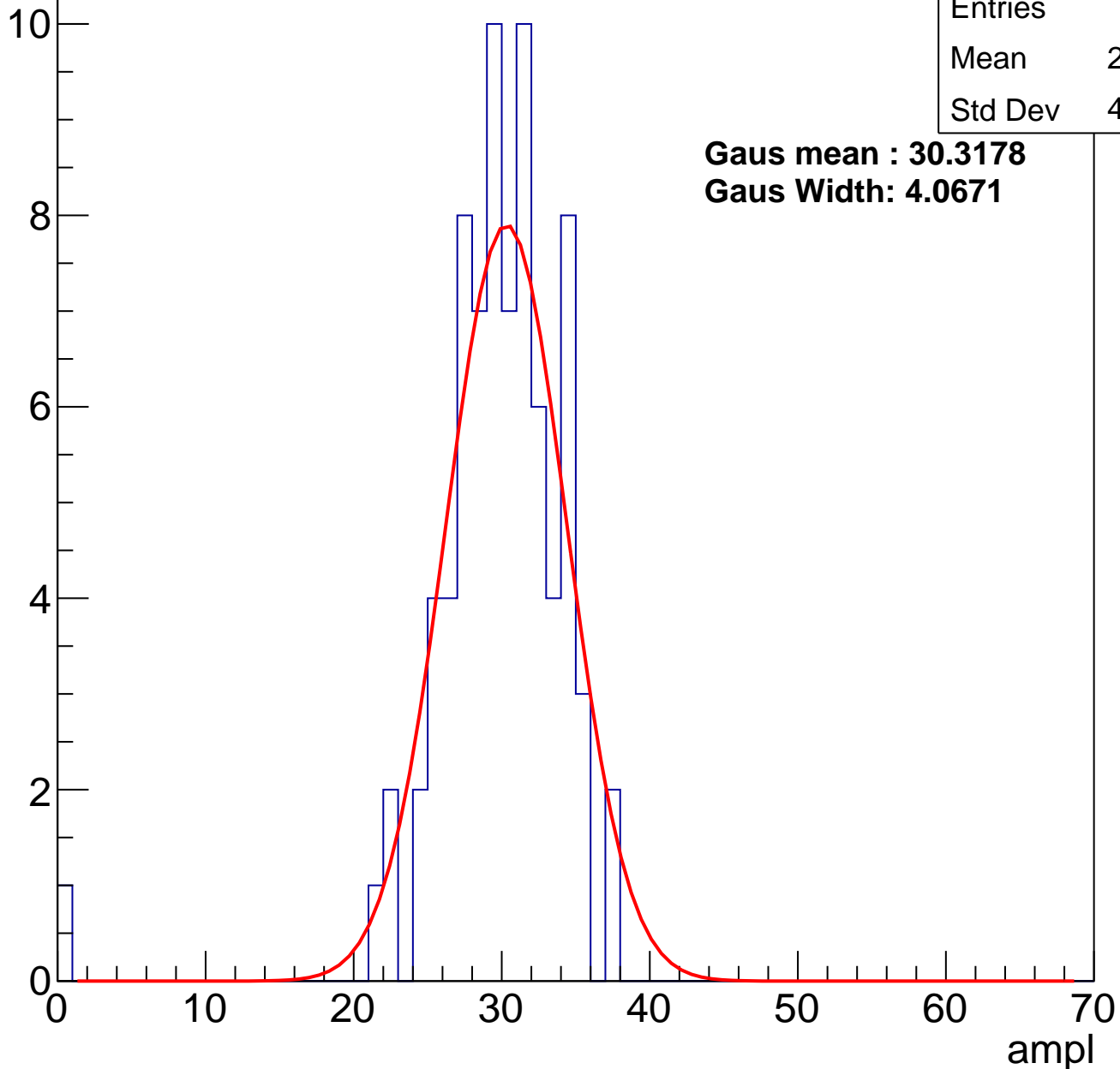
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	79
Mean	29.29
Std Dev	4.755

**Gaus mean : 30.3178**

**Gaus Width: 4.0671**

Entry



# B1L102S, U21-ch38, adc1

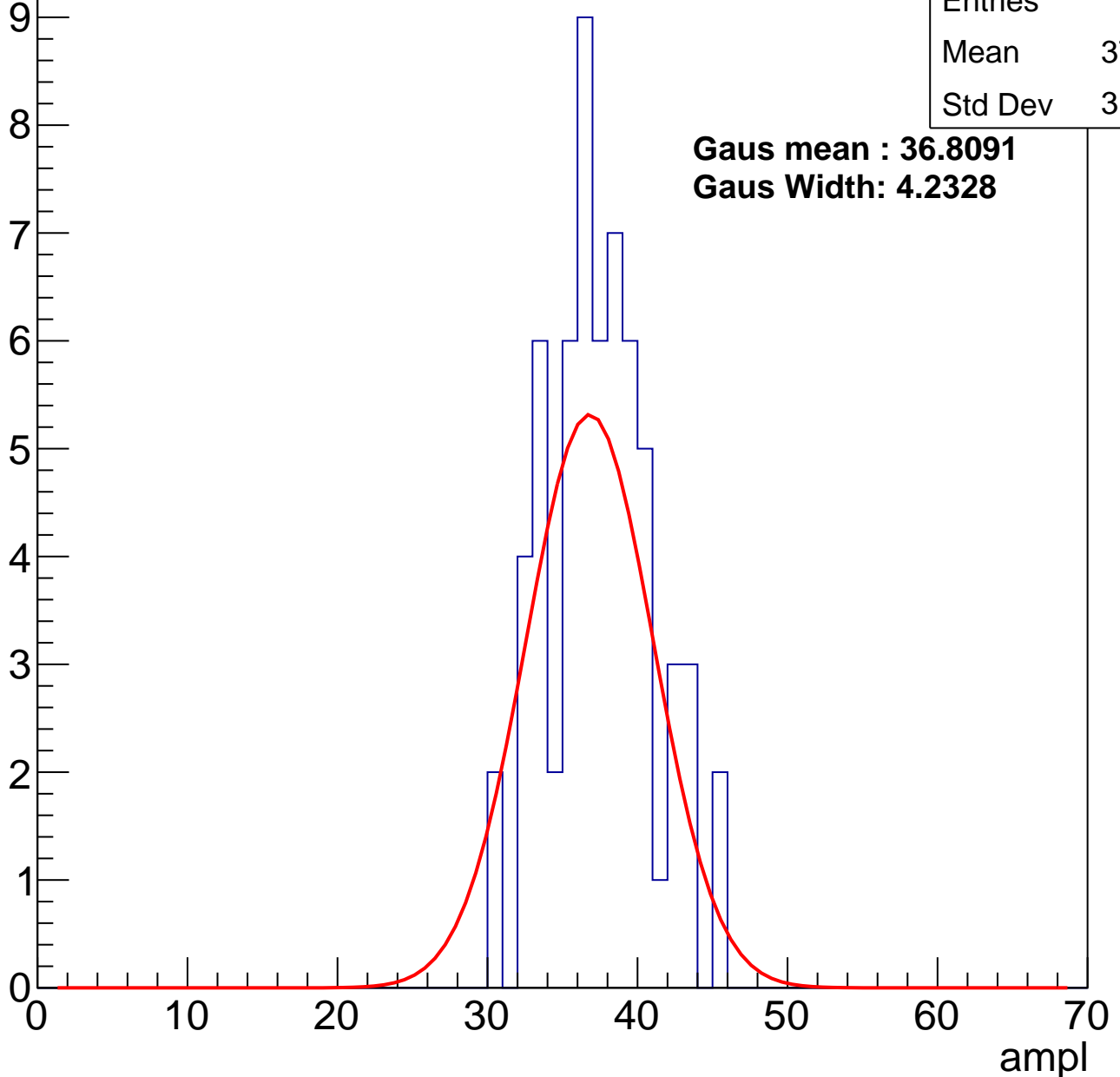
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	37.03
Std Dev	3.473

**Gaus mean : 36.8091**

**Gaus Width: 4.2328**



# B1L102S, U21-ch38, adc2

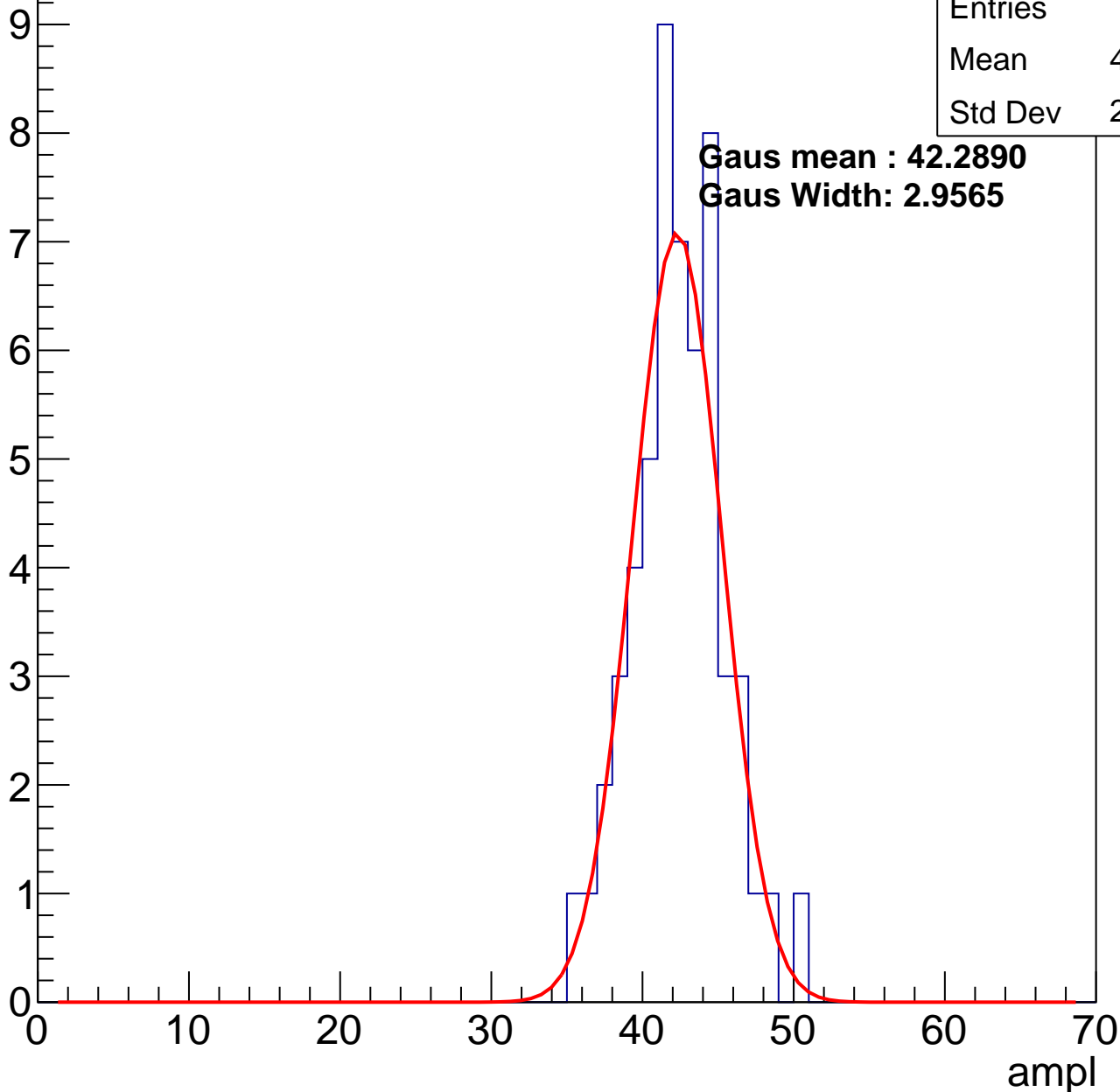
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	41.93
Std Dev	2.972

**Gaus mean : 42.2890**

**Gaus Width: 2.9565**

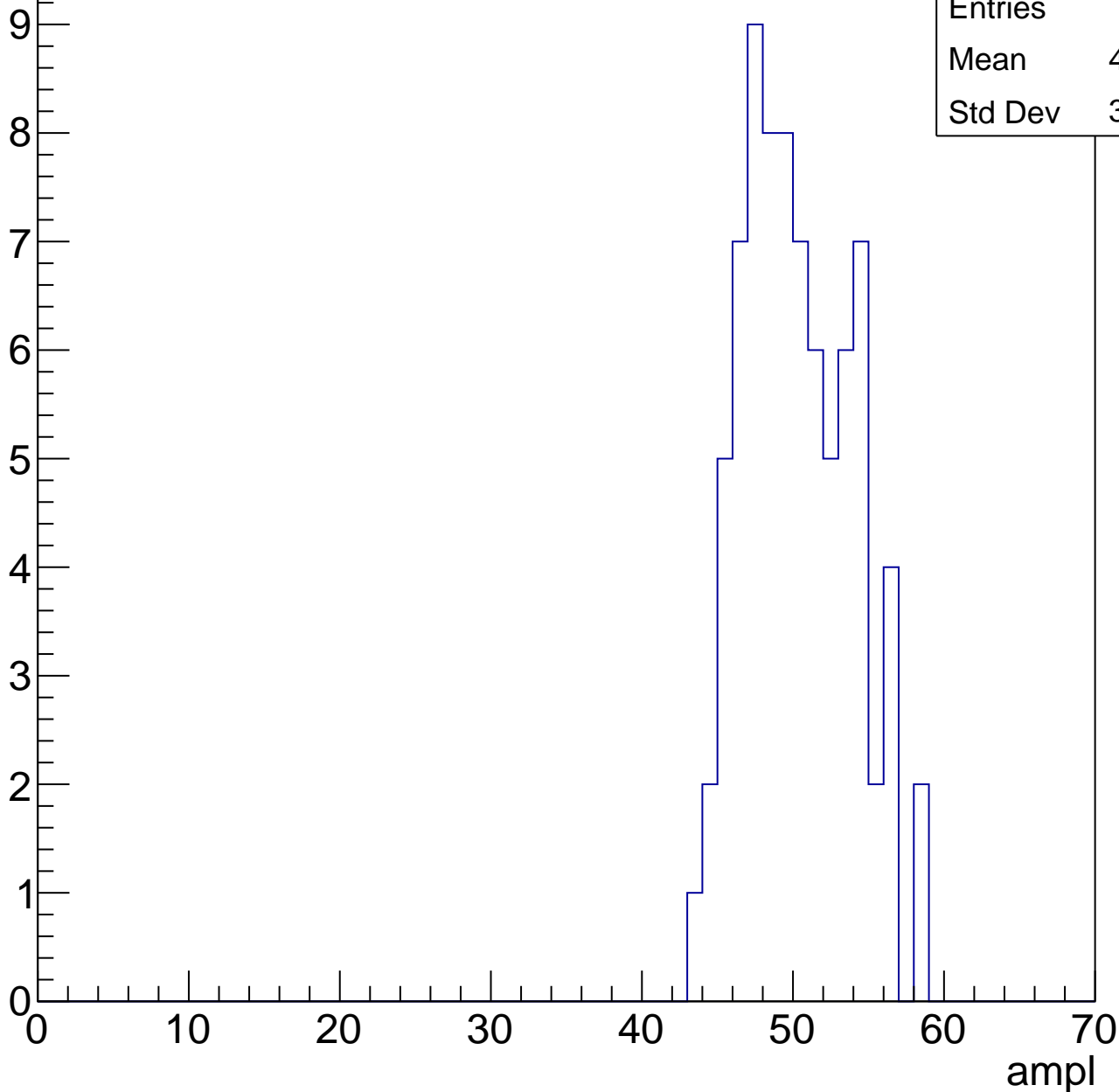


# B1L102S, U21-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	49.86
Std Dev	3.543

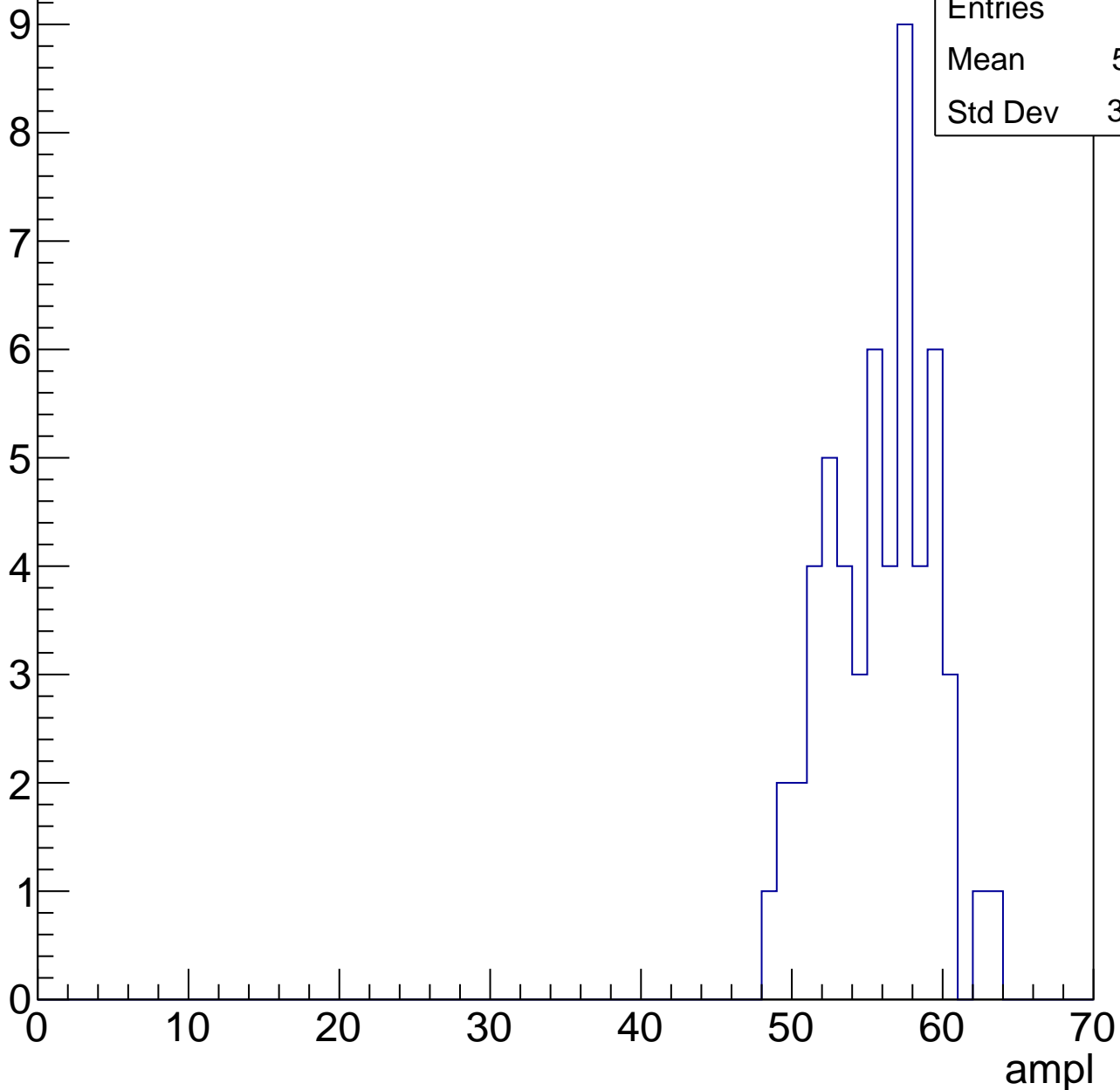


# B1L102S, U21-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	55.31
Std Dev	3.448

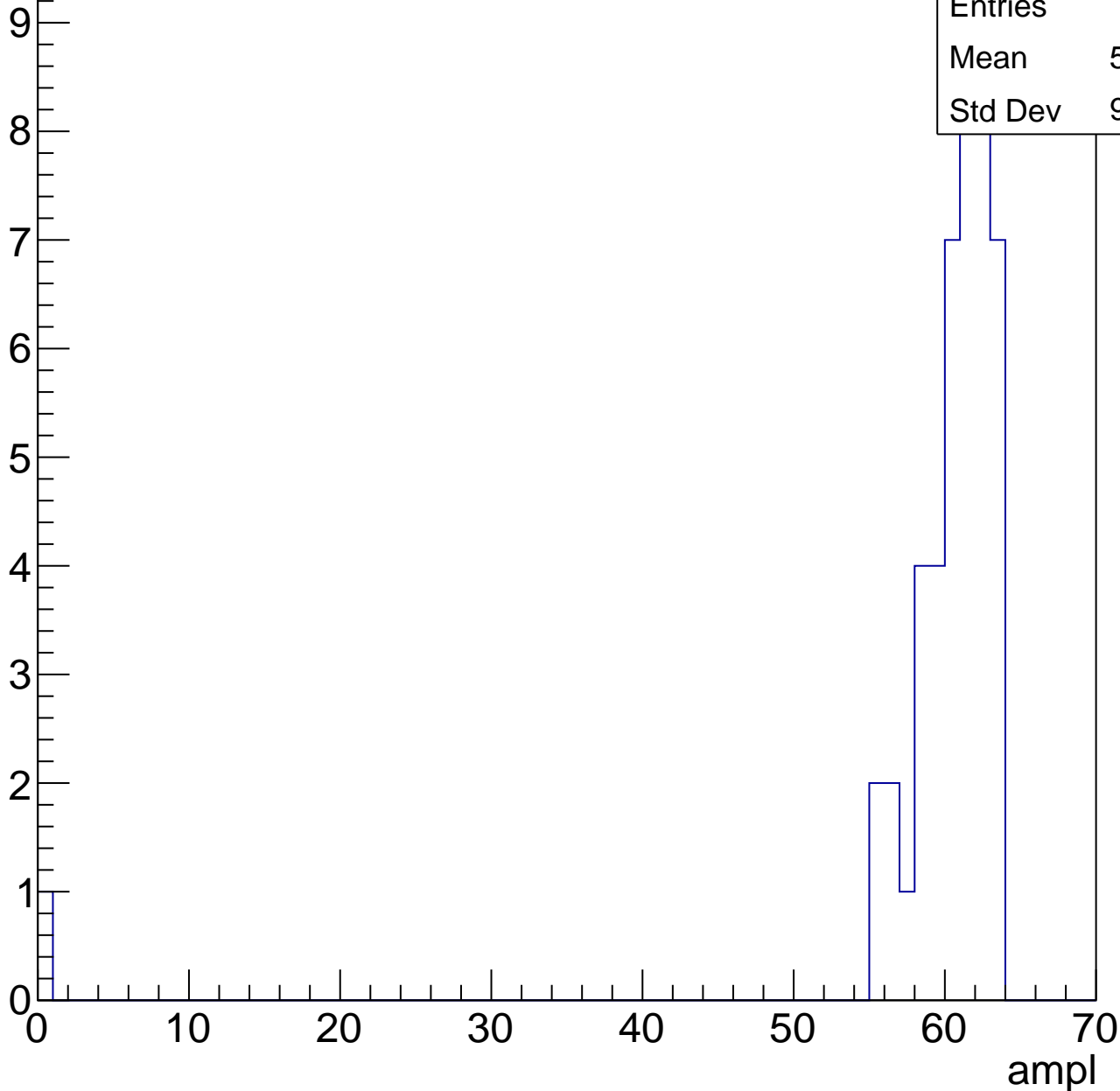


# B1L102S, U21-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	58.96
Std Dev	9.148



# B1L102S, U21-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	4
Mean	62.25
Std Dev	0.8292



# B1L102S, U21-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U21-ch39, adc0

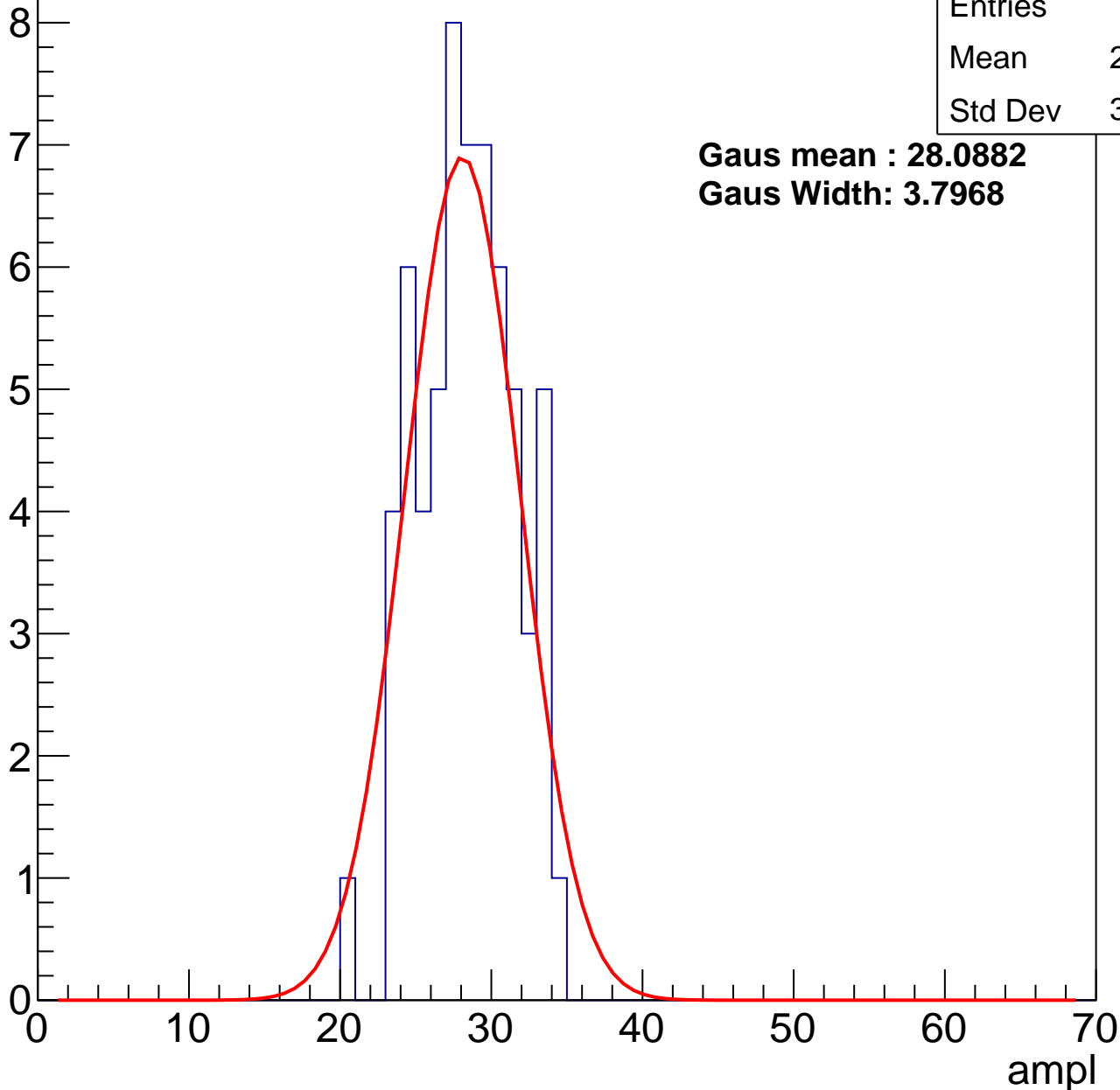
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	27.92
Std Dev	3.133

**Gaus mean : 28.0882**

**Gaus Width: 3.7968**



# B1L102S, U21-ch39, adc1

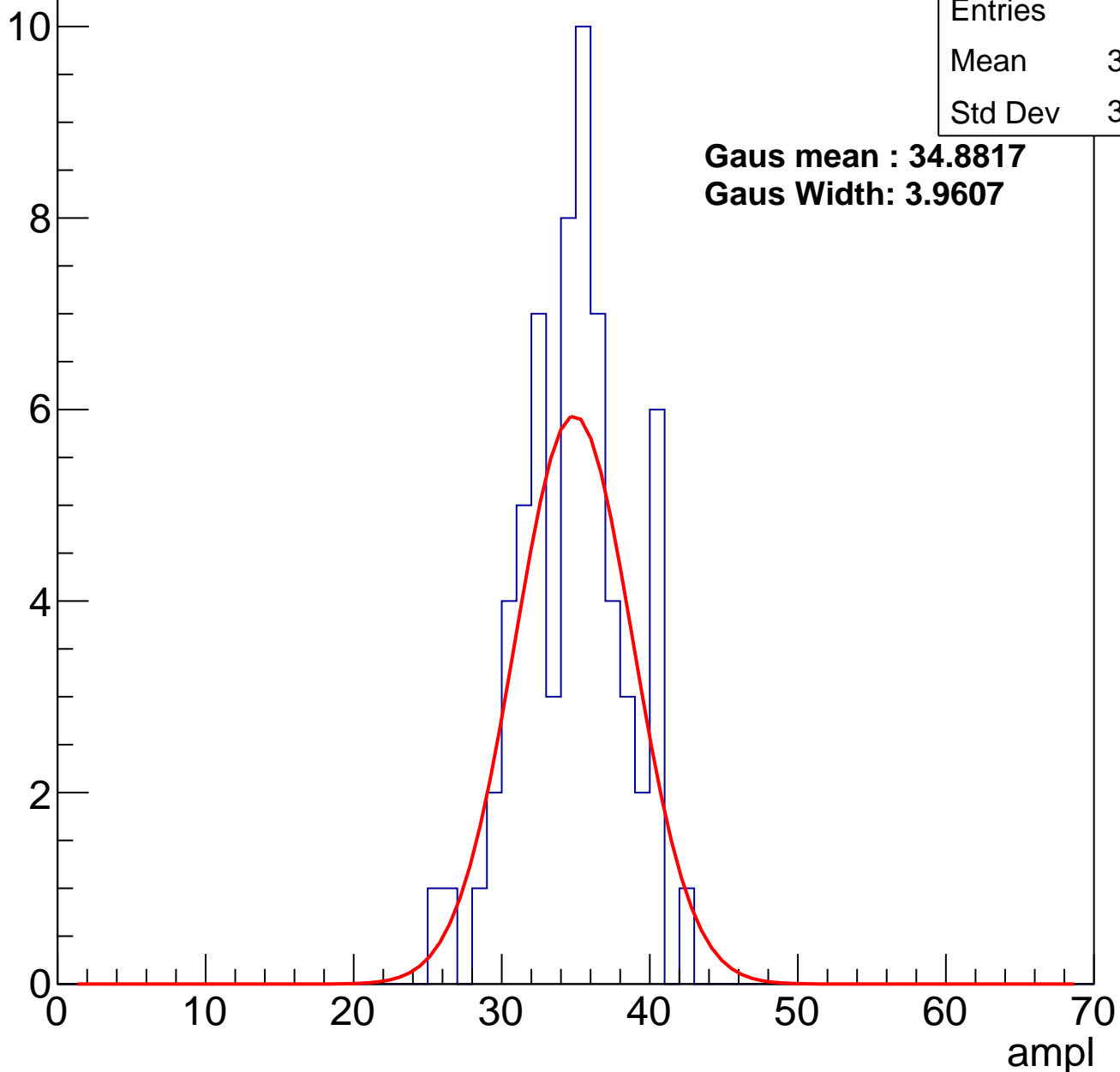
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	65
Mean	34.32
Std Dev	3.544

**Gaus mean : 34.8817**

**Gaus Width: 3.9607**

Entry



# B1L102S, U21-ch39, adc2

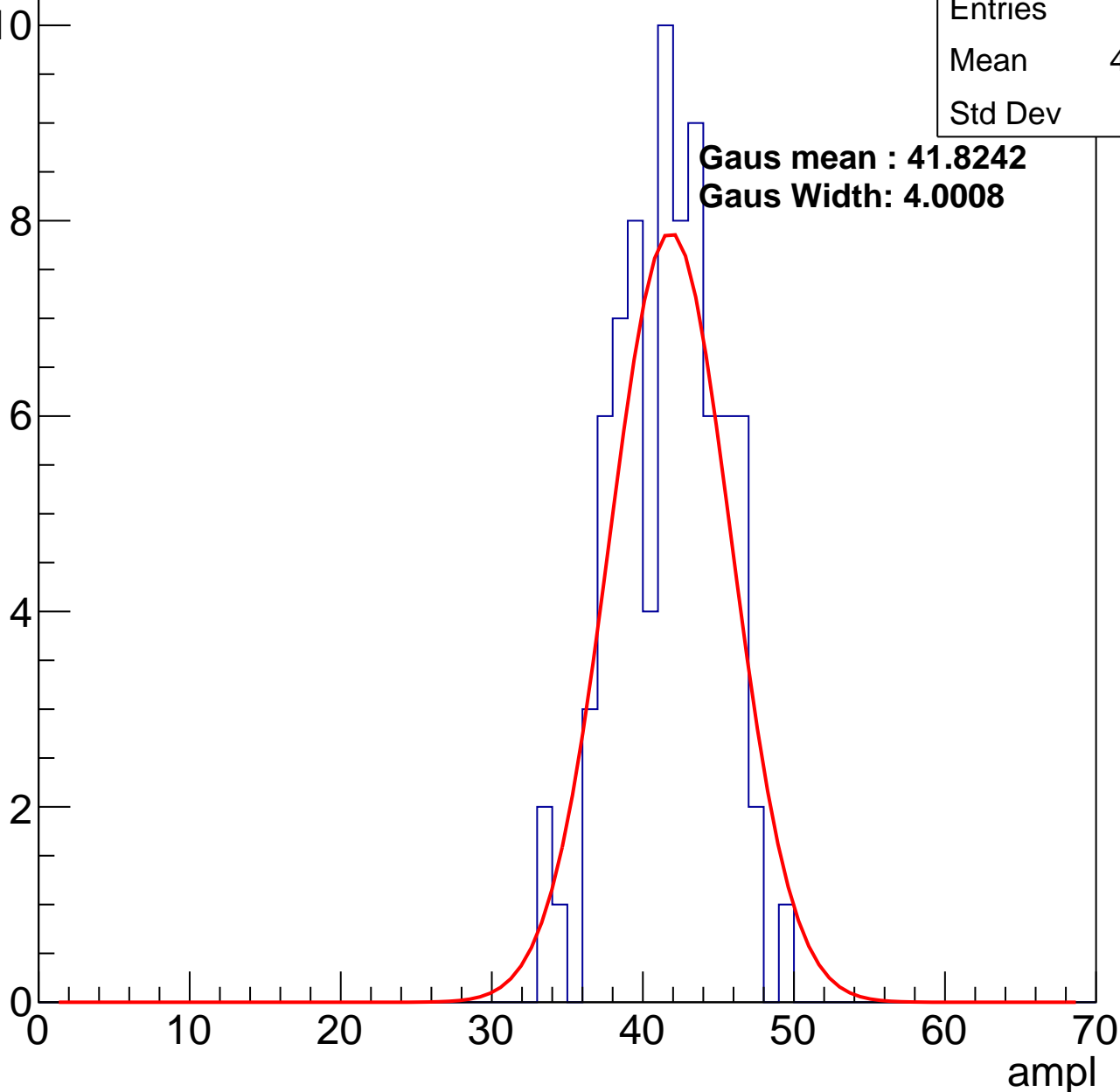
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	41.19
Std Dev	3.42

**Gaus mean : 41.8242**

**Gaus Width: 4.0008**

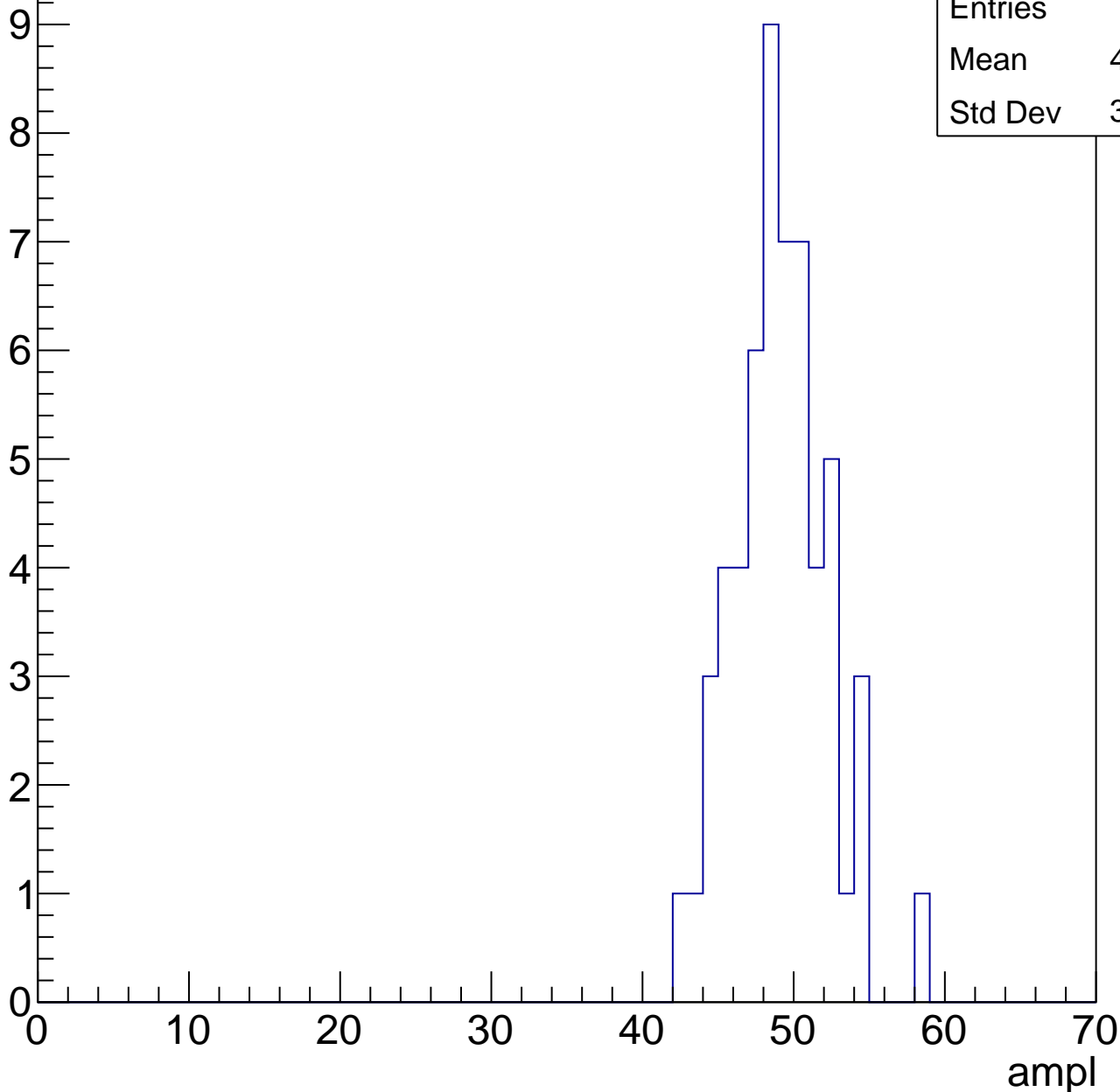


# B1L102S, U21-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	48.66
Std Dev	3.066

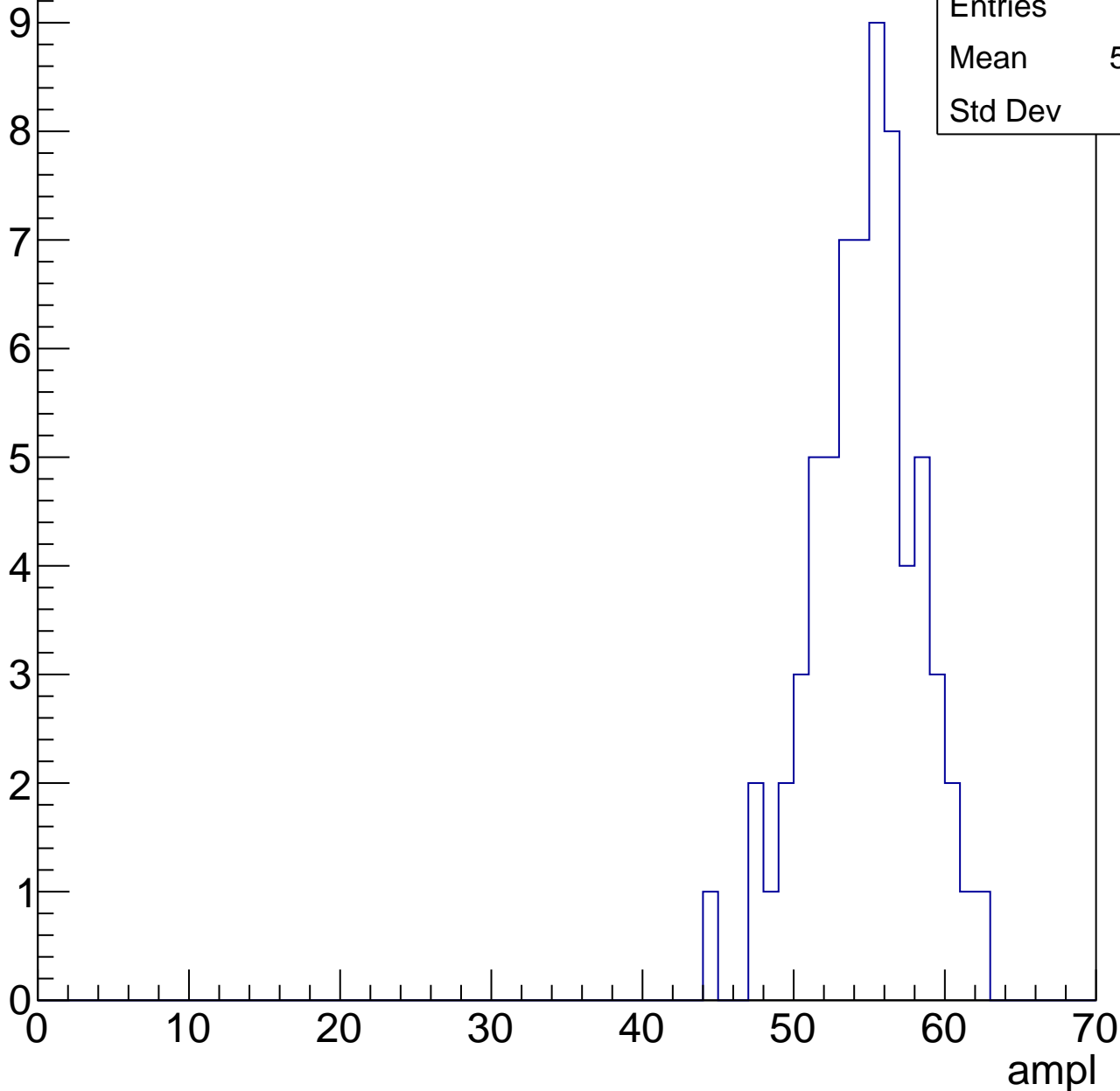


# B1L102S, U21-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	54.23
Std Dev	3.52

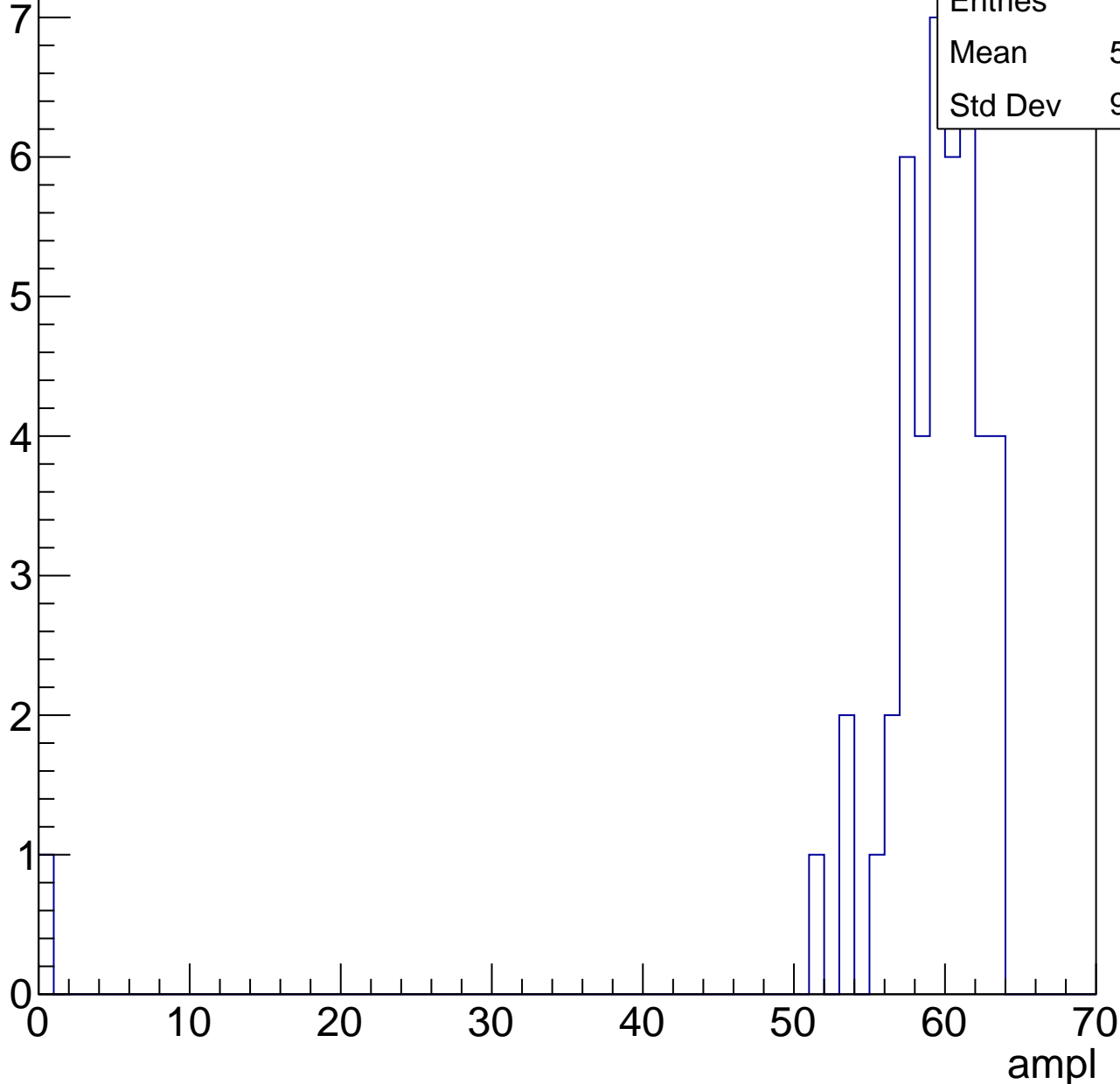


# B1L102S, U21-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	57.73
Std Dev	9.118

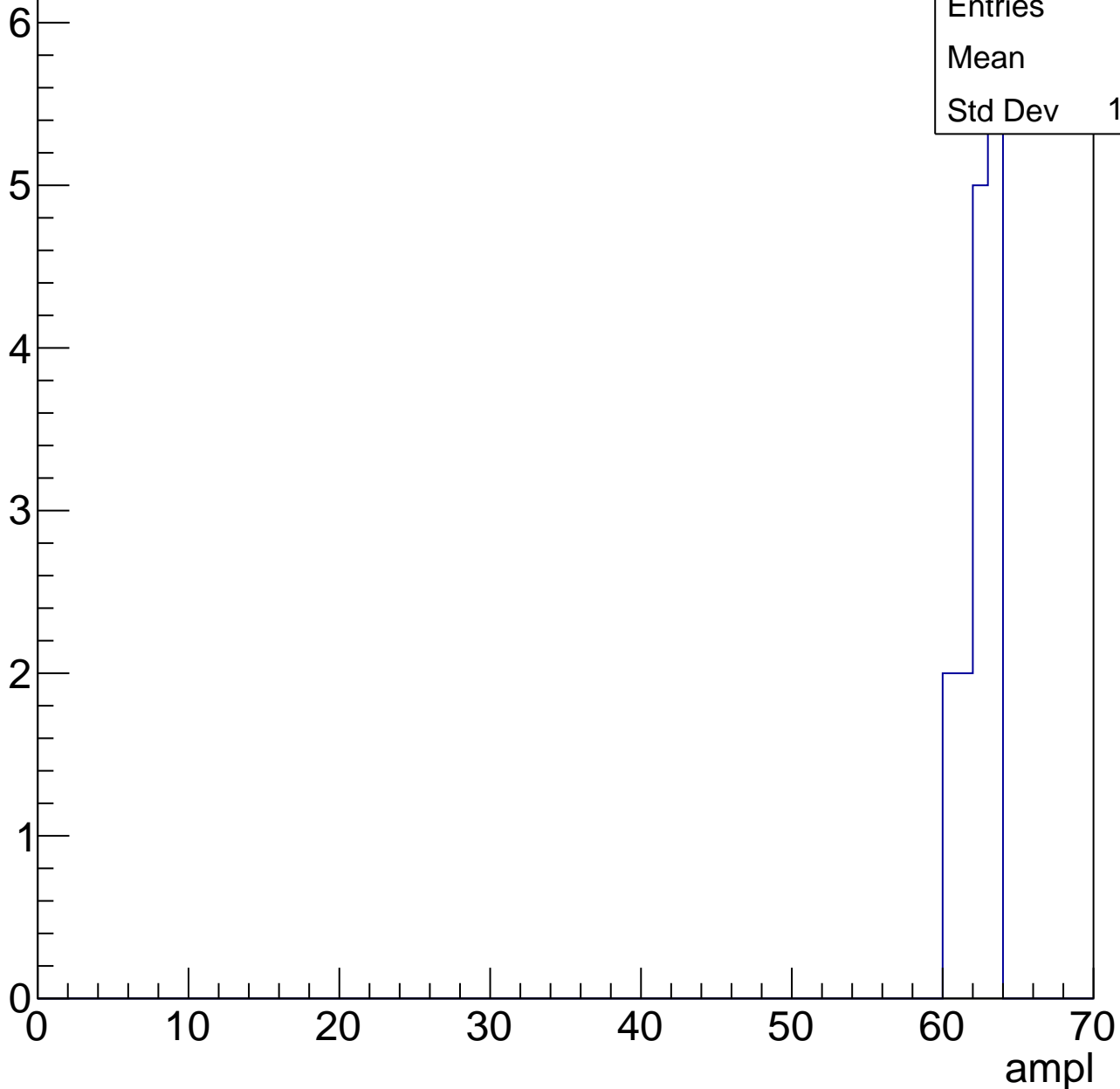


# B1L102S, U21-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	15
Mean	62
Std Dev	1.033





# B1L102S, U21-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch40, adc0

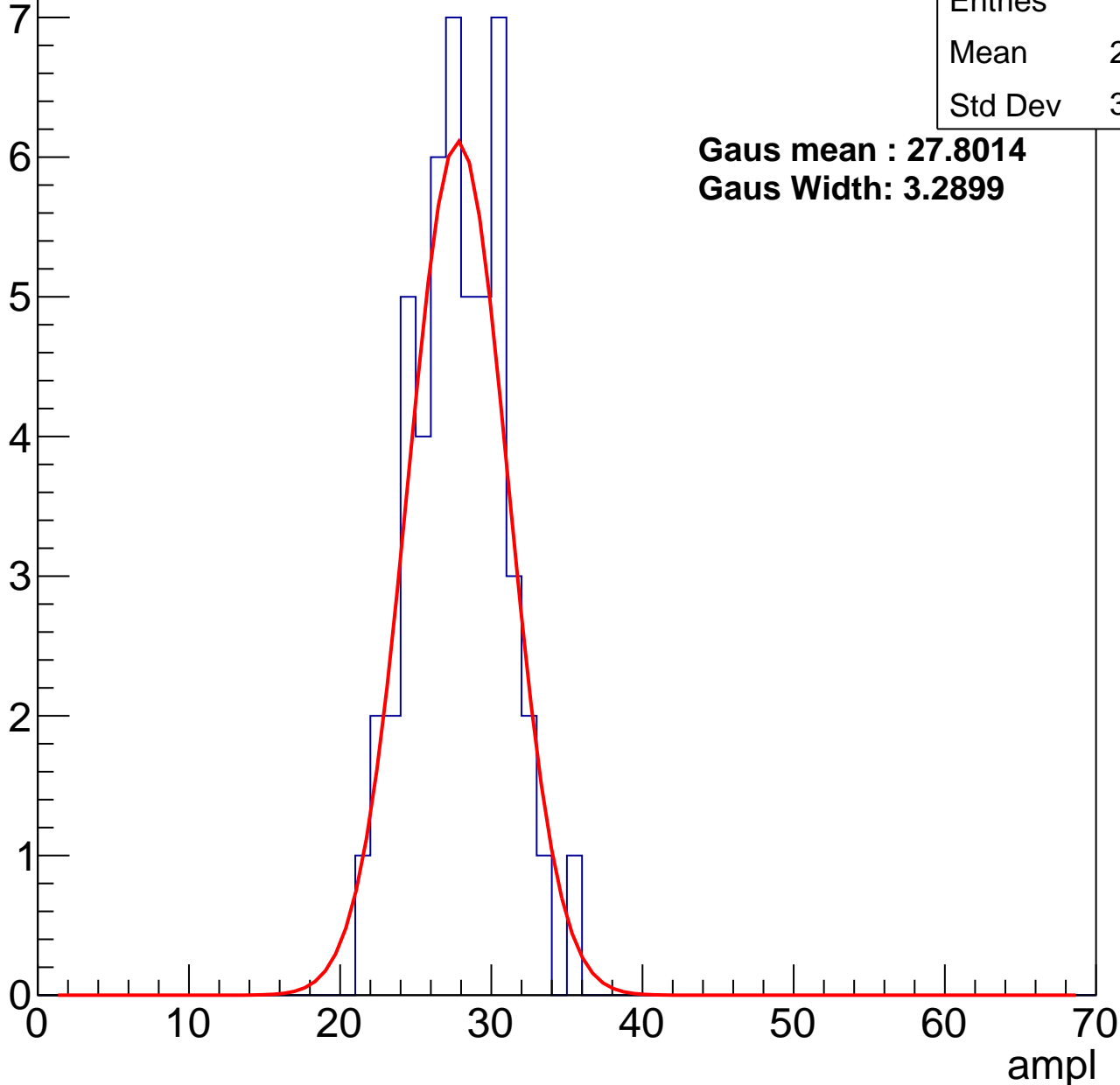
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	27.37
Std Dev	3.016

**Gaus mean : 27.8014**

**Gaus Width: 3.2899**



# B1L102S, U21-ch40, adc1

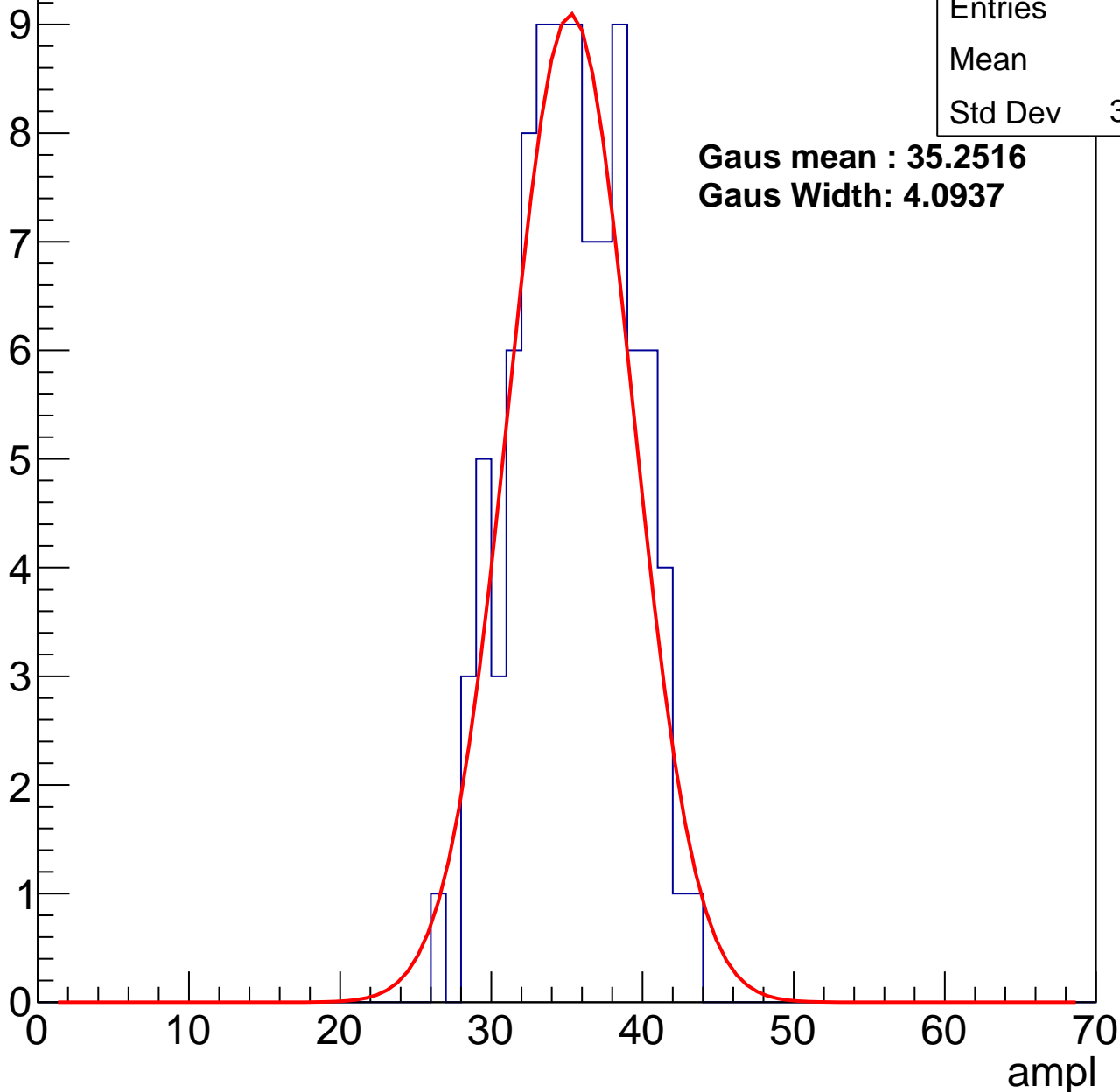
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	94
Mean	34.9
Std Dev	3.739

**Gaus mean : 35.2516**

**Gaus Width: 4.0937**



# B1L102S, U21-ch40, adc2

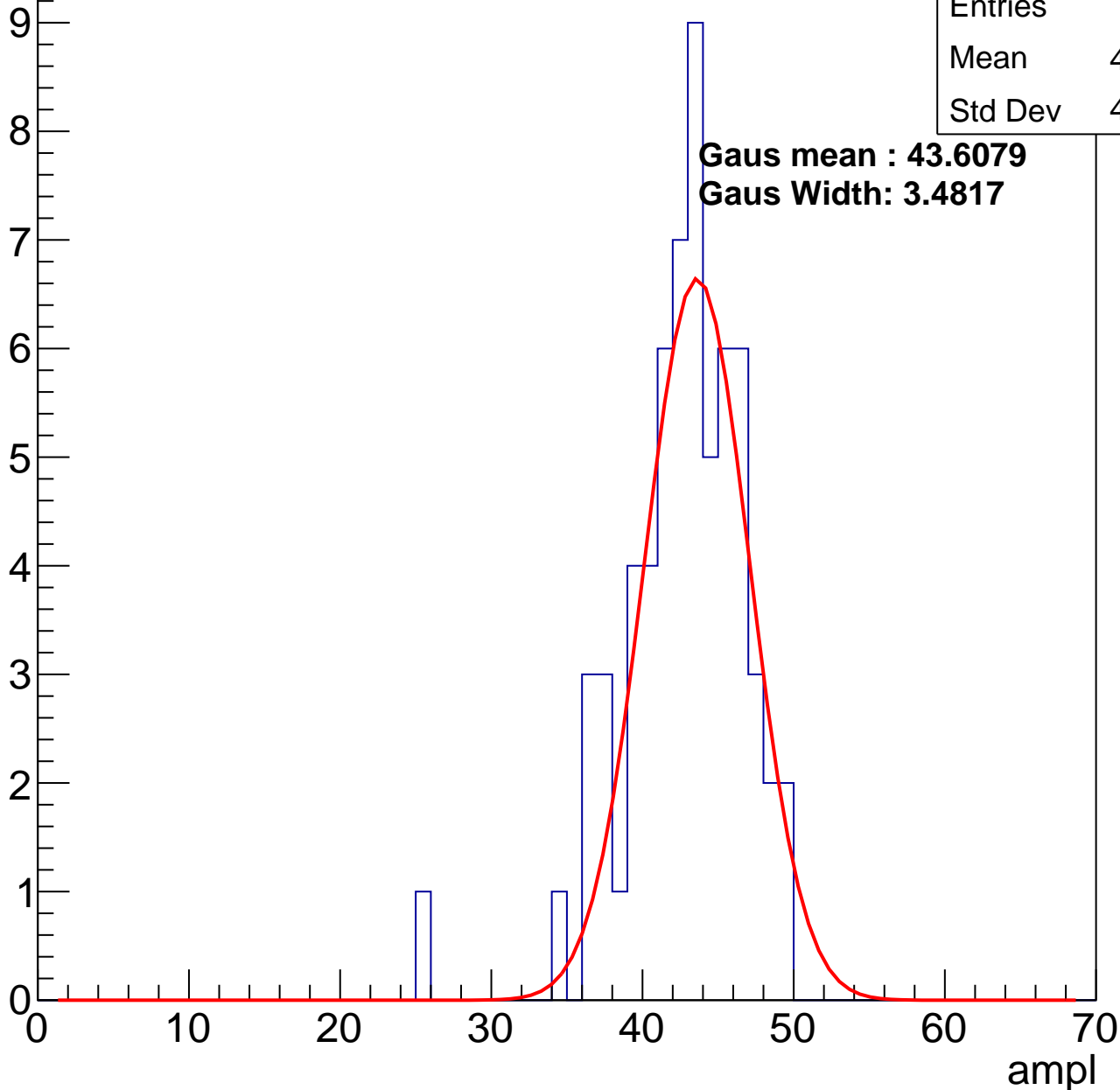
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	42.22
Std Dev	4.045

**Gaus mean : 43.6079**

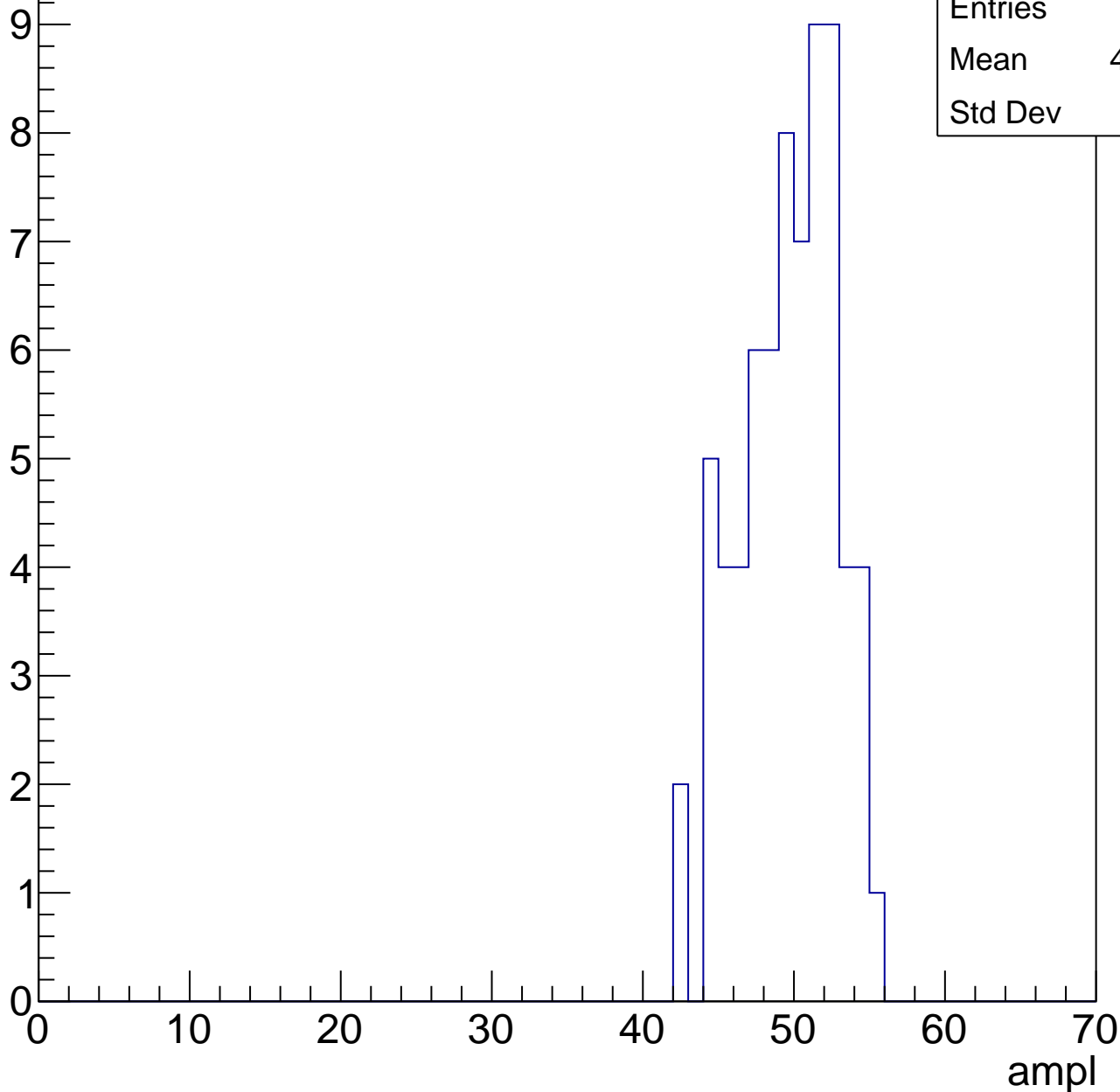
**Gaus Width: 3.4817**



# B1L102S, U21-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

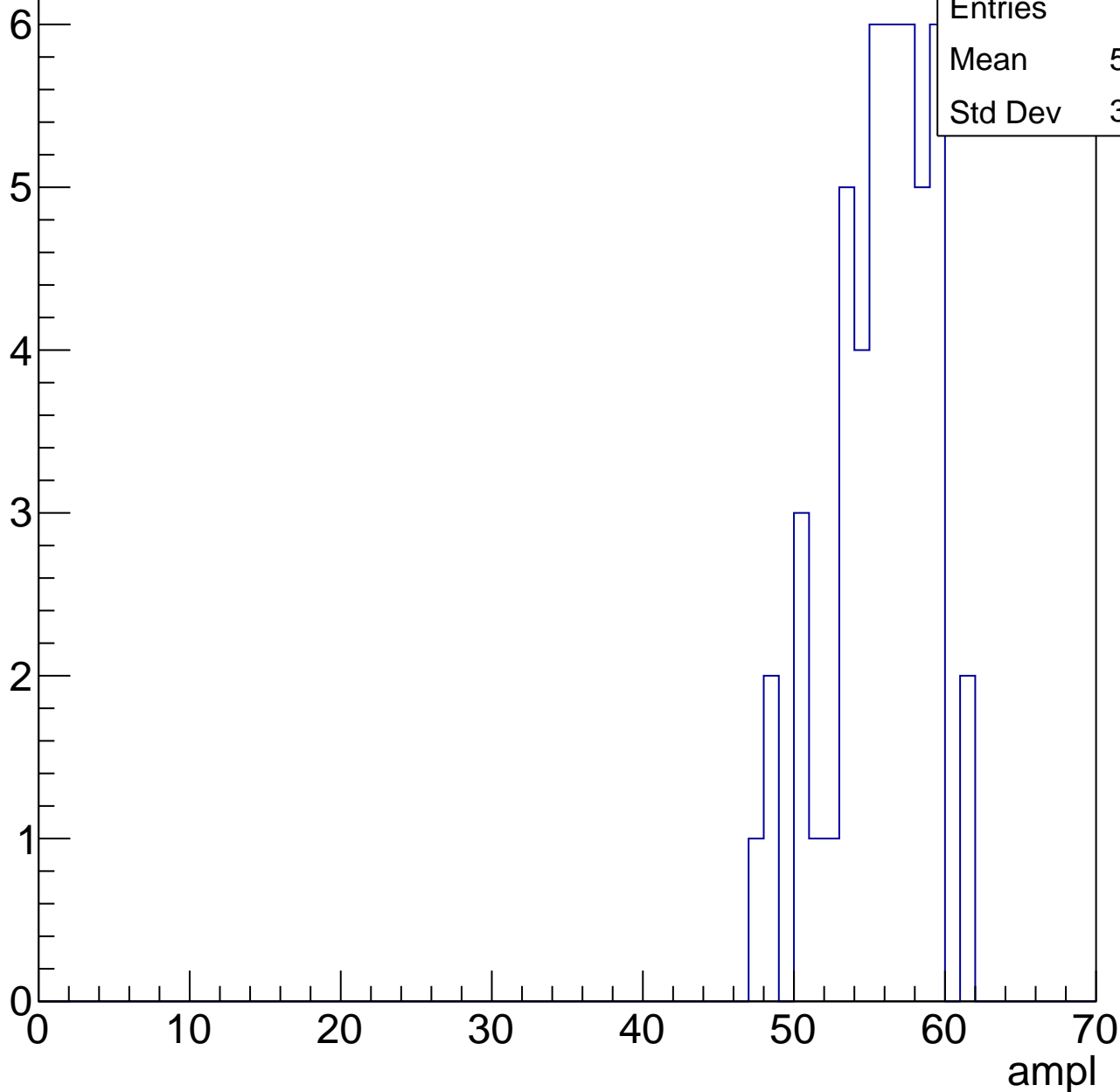


# B1L102S, U21-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	55.23
Std Dev	3.312



# B1L102S, U21-ch40, adc5

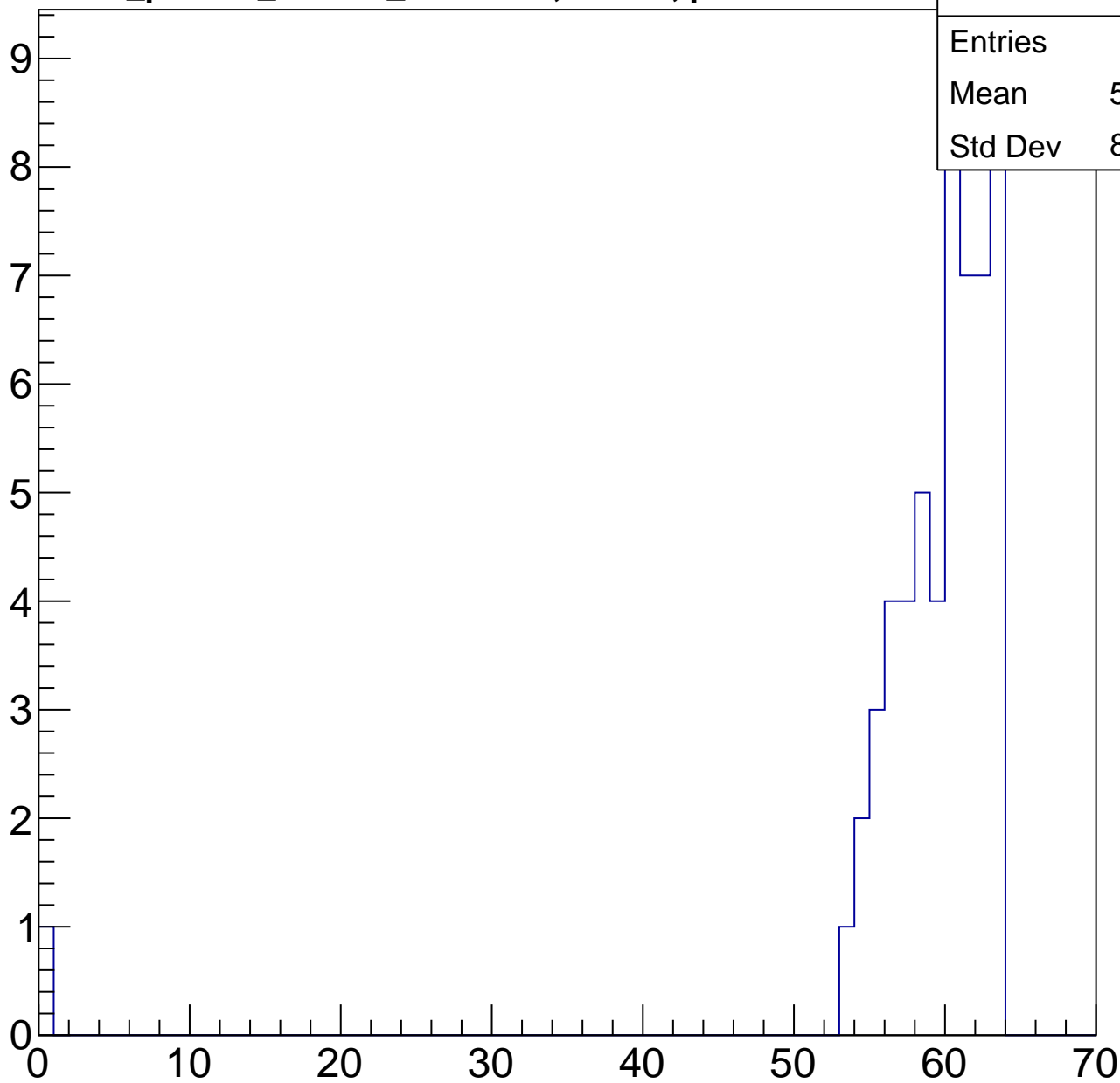
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	56
Mean	58.43
Std Dev	8.343

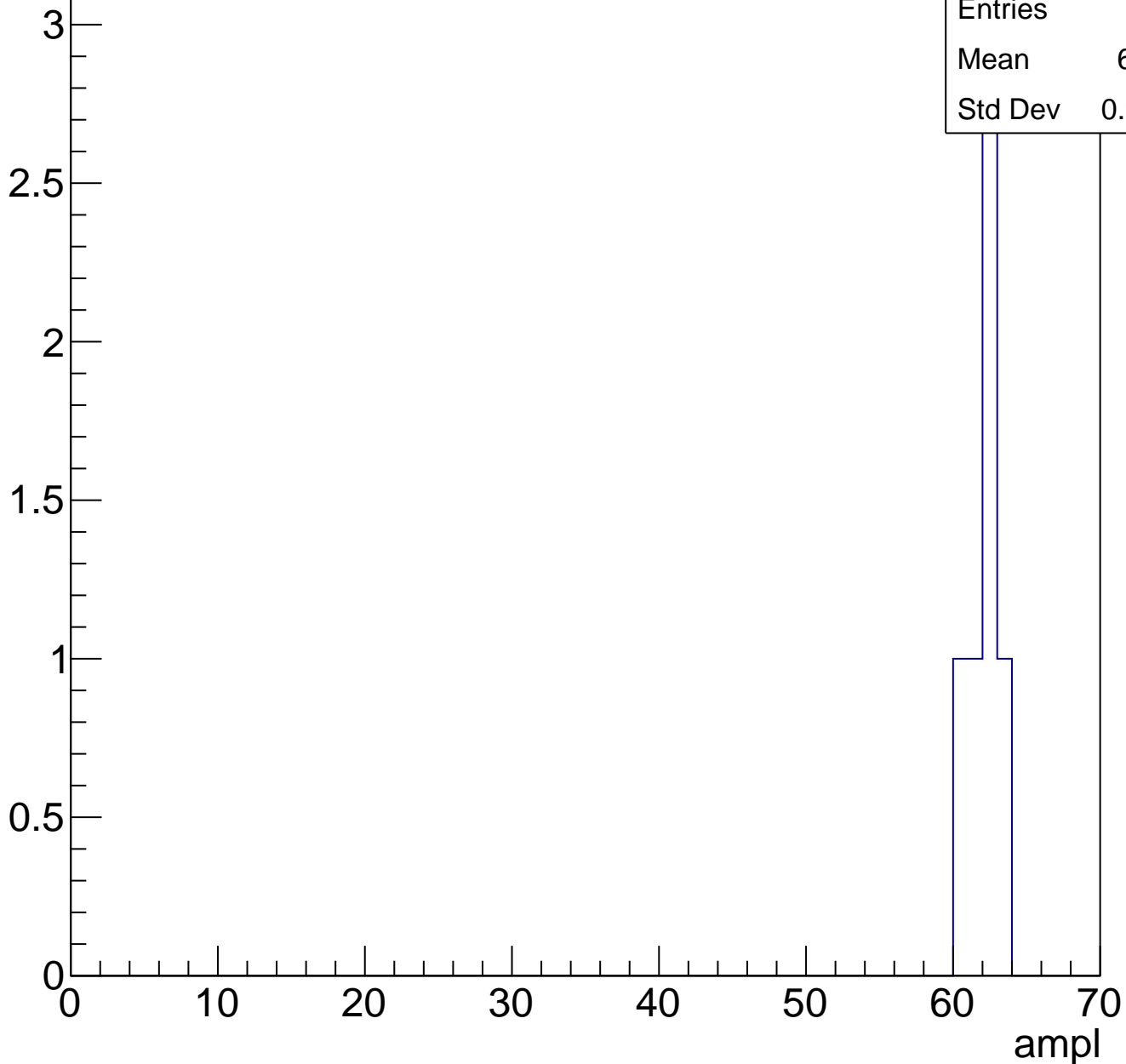
ampl



# B1L102S, U21-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

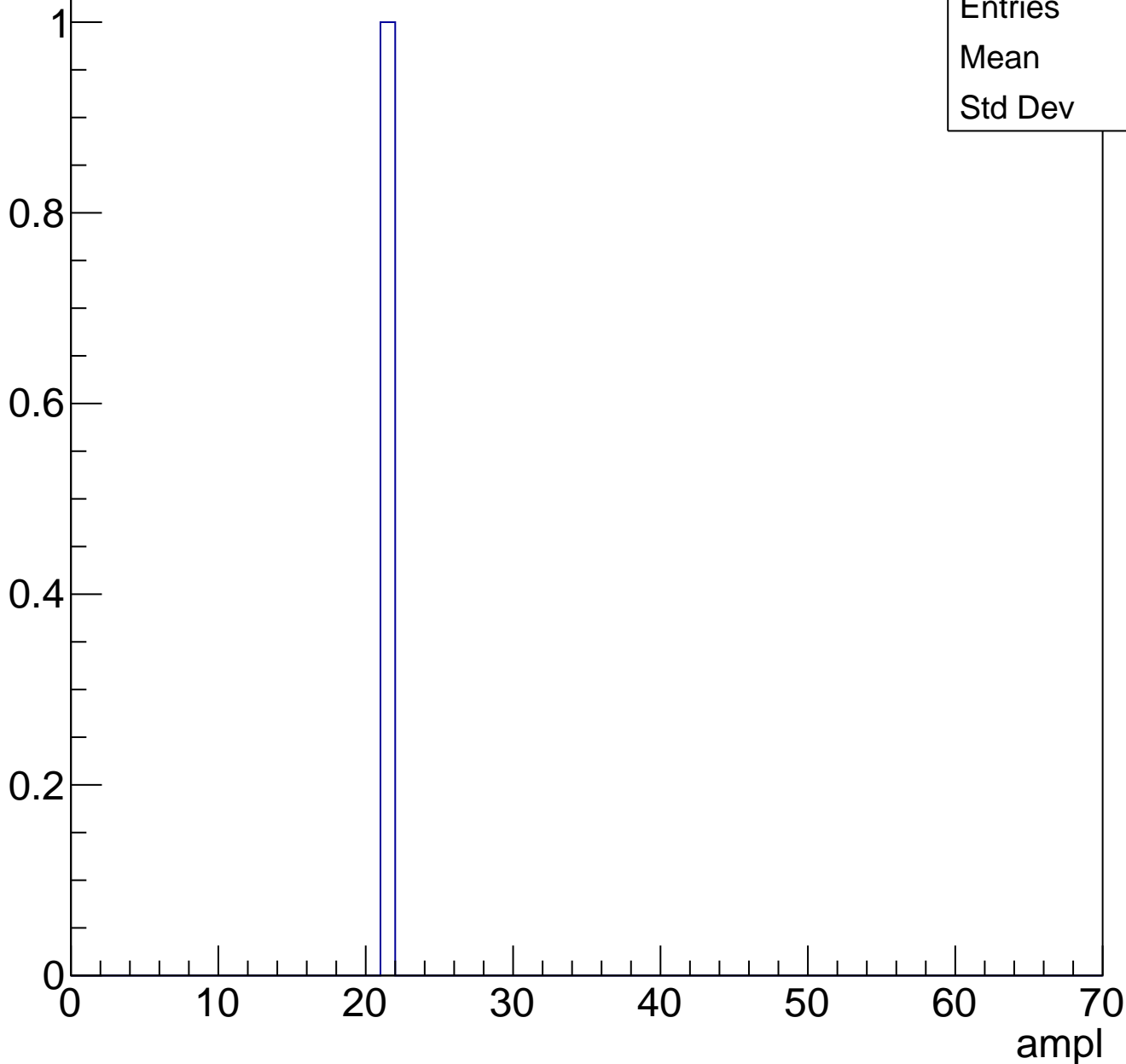




# B1L102S, U21-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch41, adc0

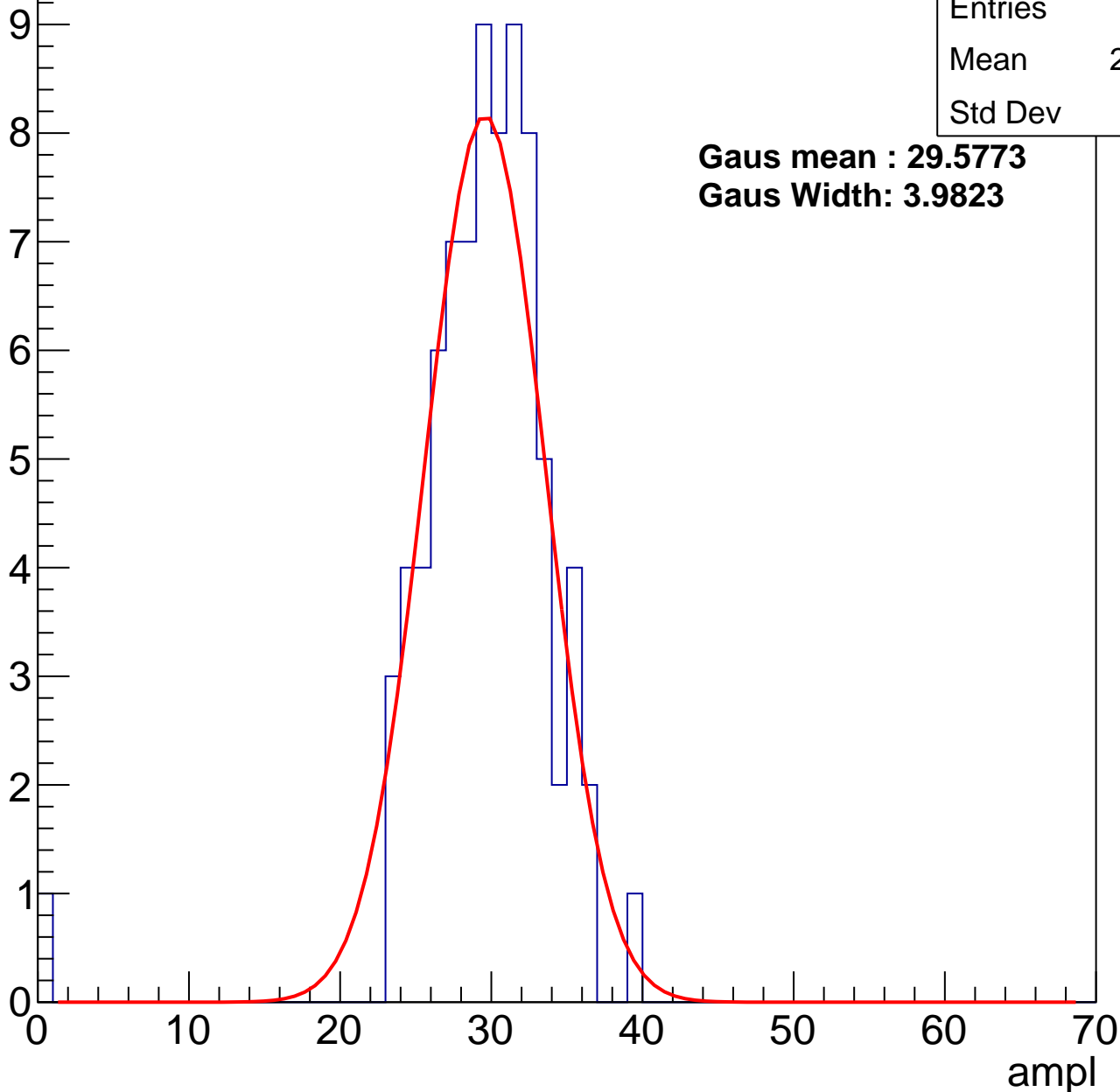
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	29.07
Std Dev	4.73

**Gaus mean : 29.5773**

**Gaus Width: 3.9823**



# B1L102S, U21-ch41, adc1

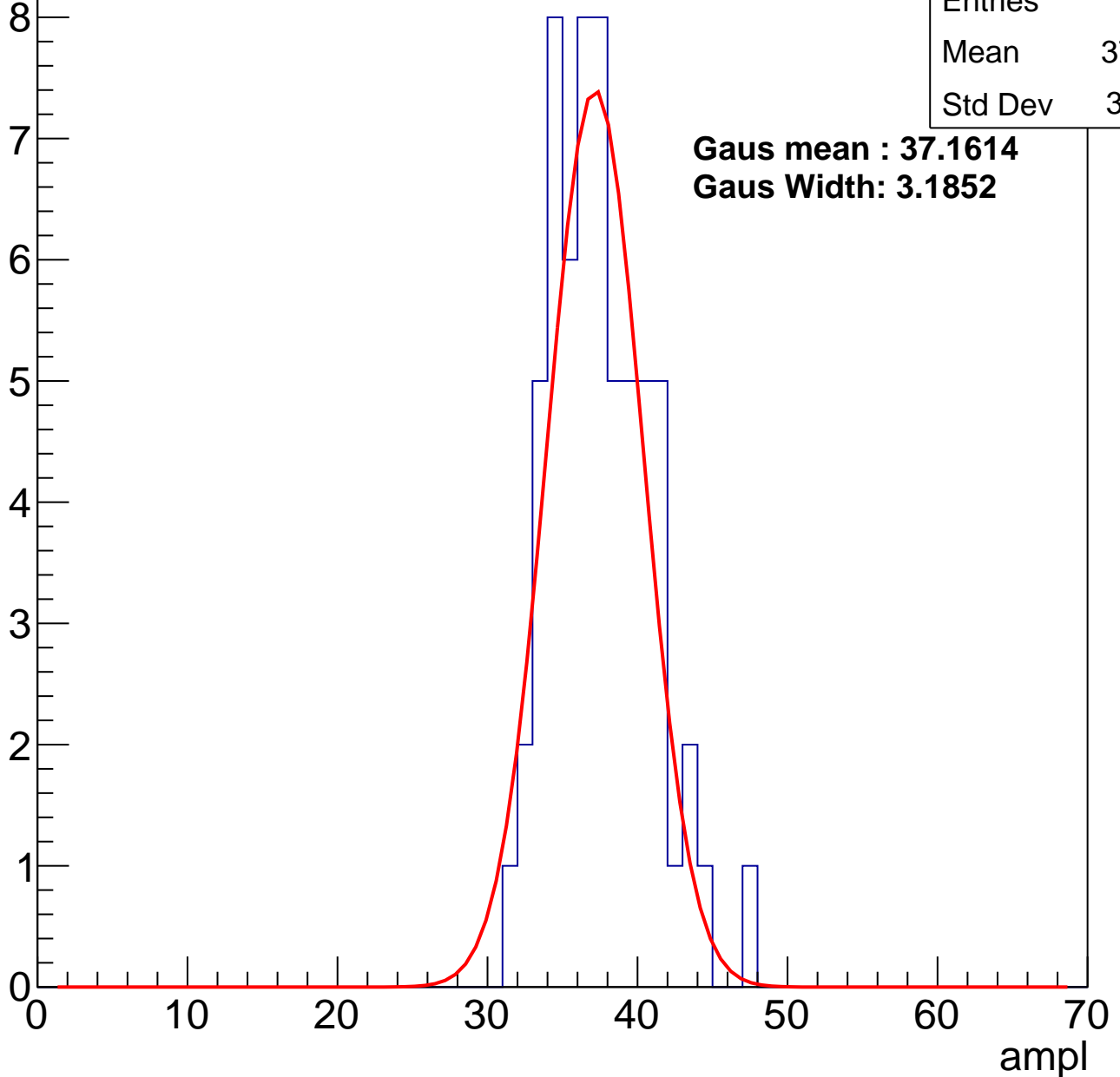
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	37.06
Std Dev	3.251

**Gaus mean : 37.1614**

**Gaus Width: 3.1852**



# B1L102S, U21-ch41, adc2

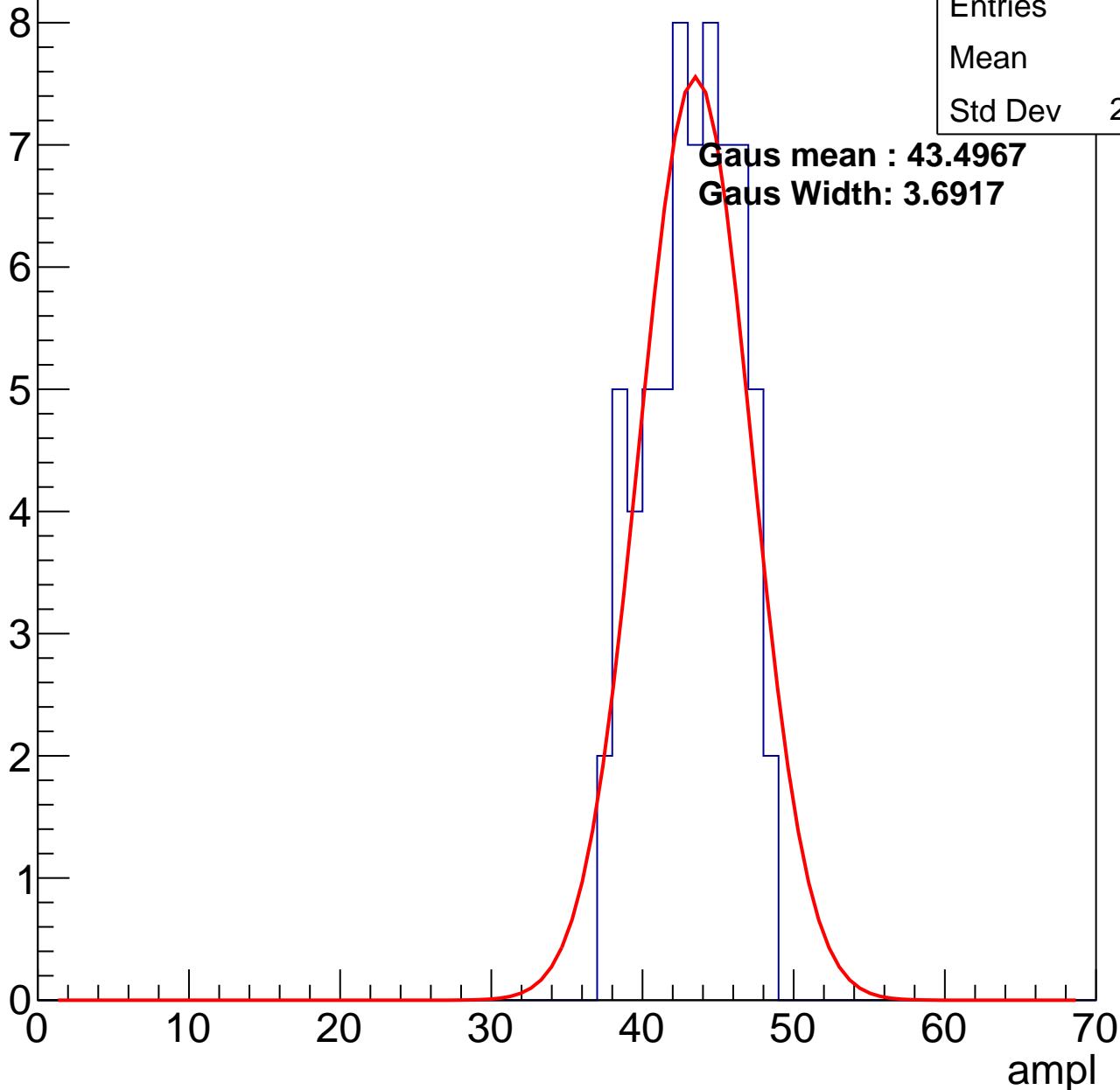
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	42.8
Std Dev	2.936

**Gaus mean : 43.4967**

**Gaus Width: 3.6917**

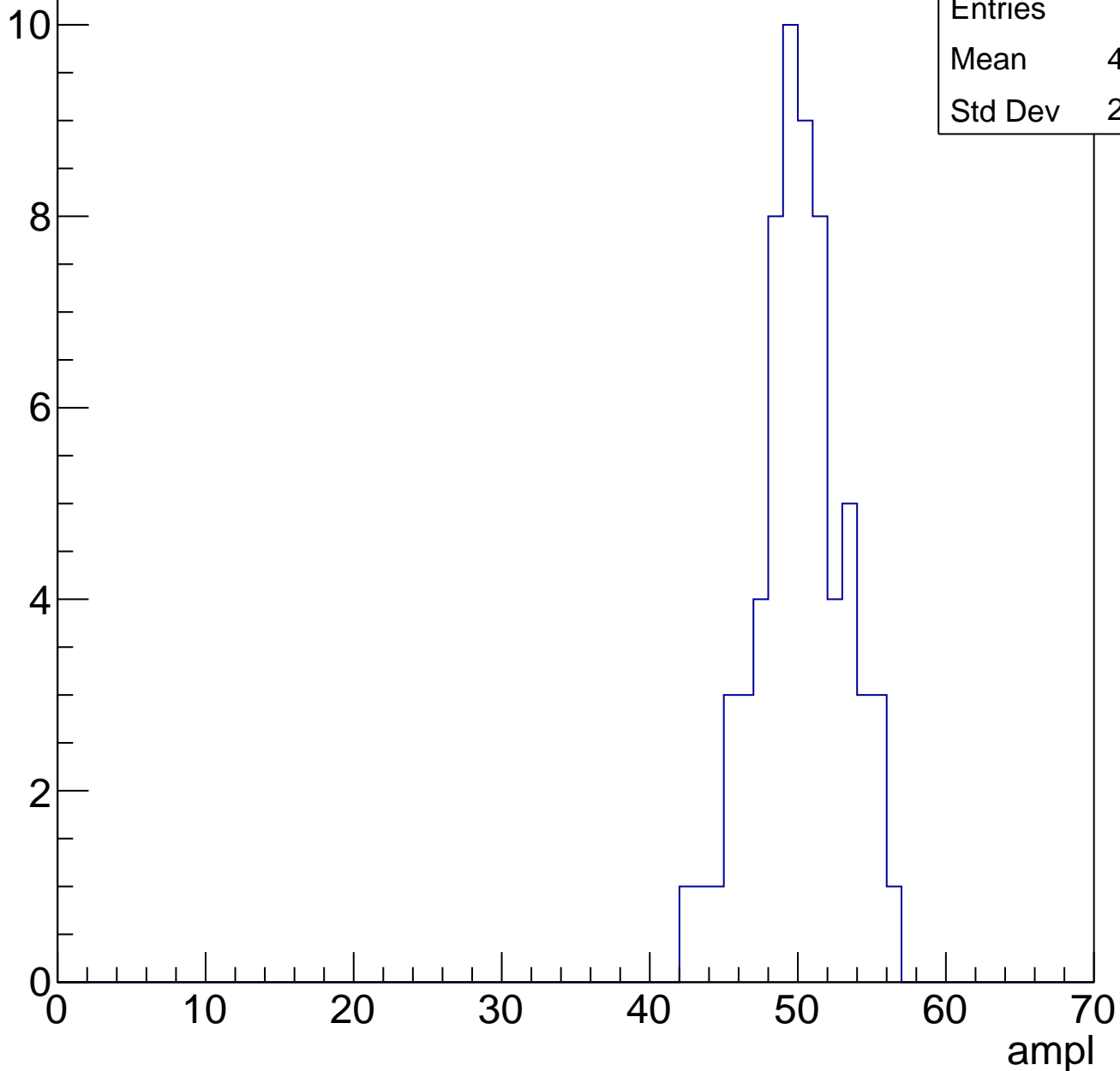


# B1L102S, U21-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

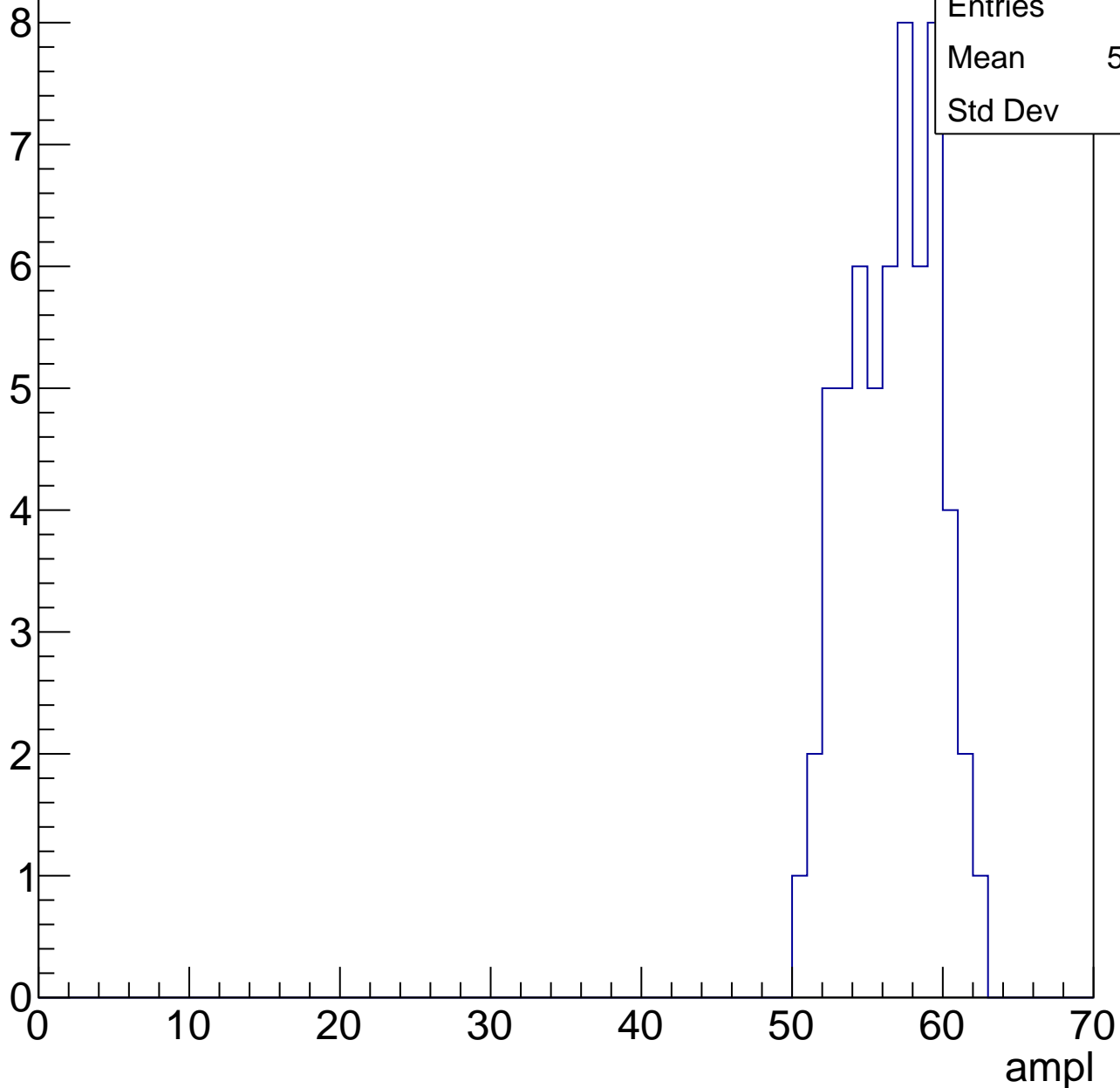
Entries	64
Mean	49.66
Std Dev	2.985



# B1L102S, U21-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

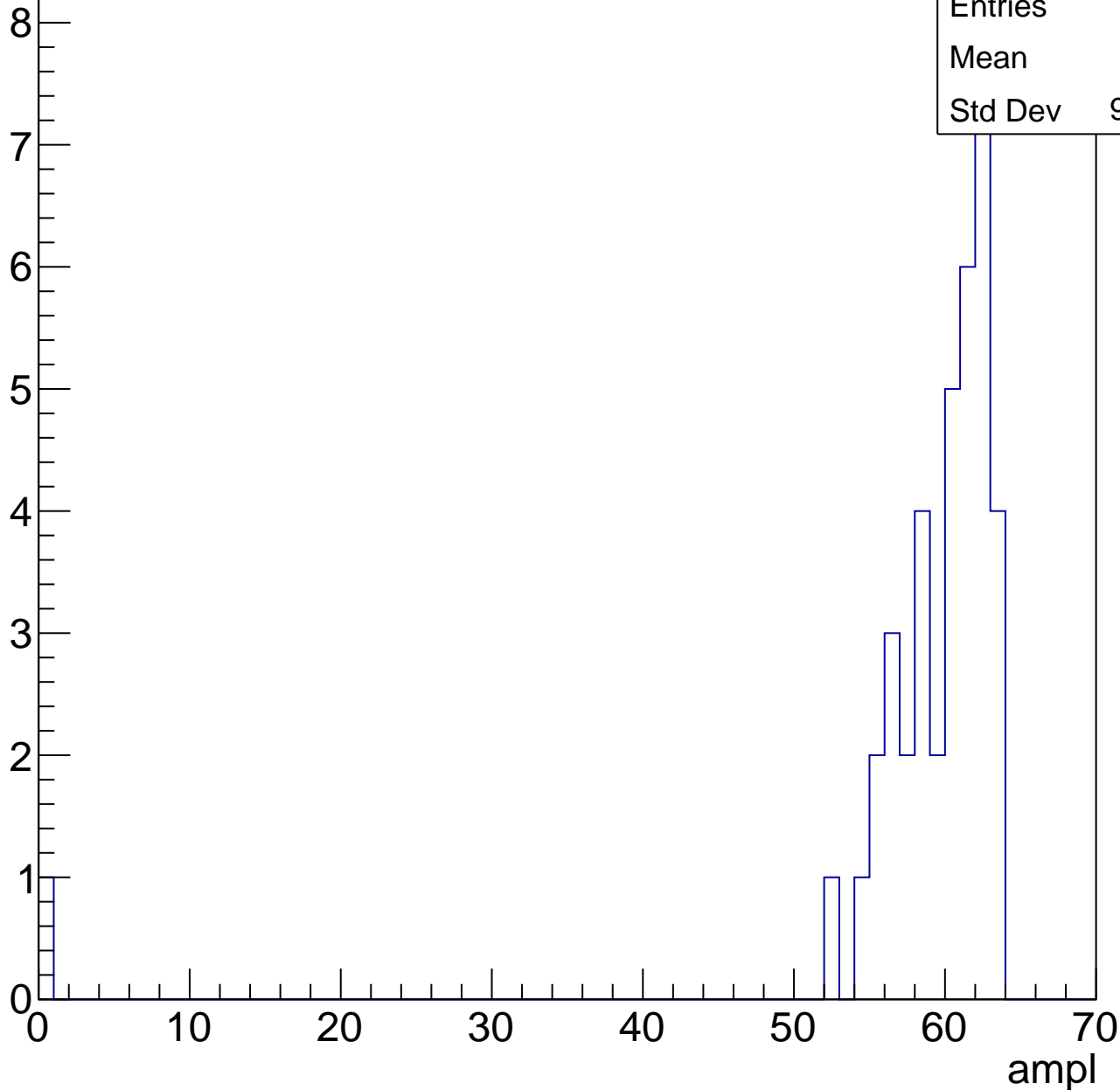


# B1L102S, U21-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	39
Mean	58
Std Dev	9.808

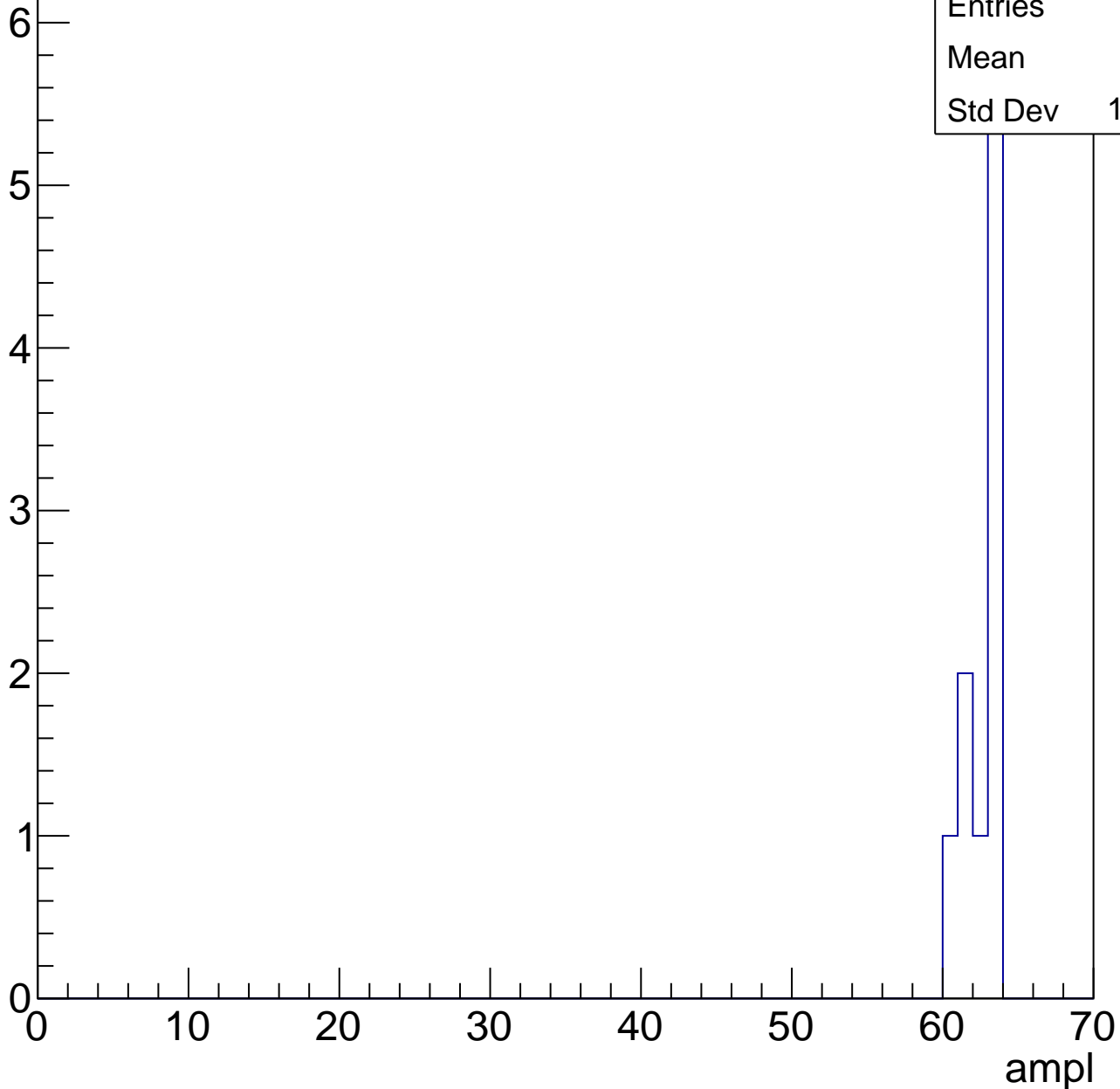


# B1L102S, U21-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	10
Mean	62.2
Std Dev	1.077





# B1L102S, U21-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch42, adc0

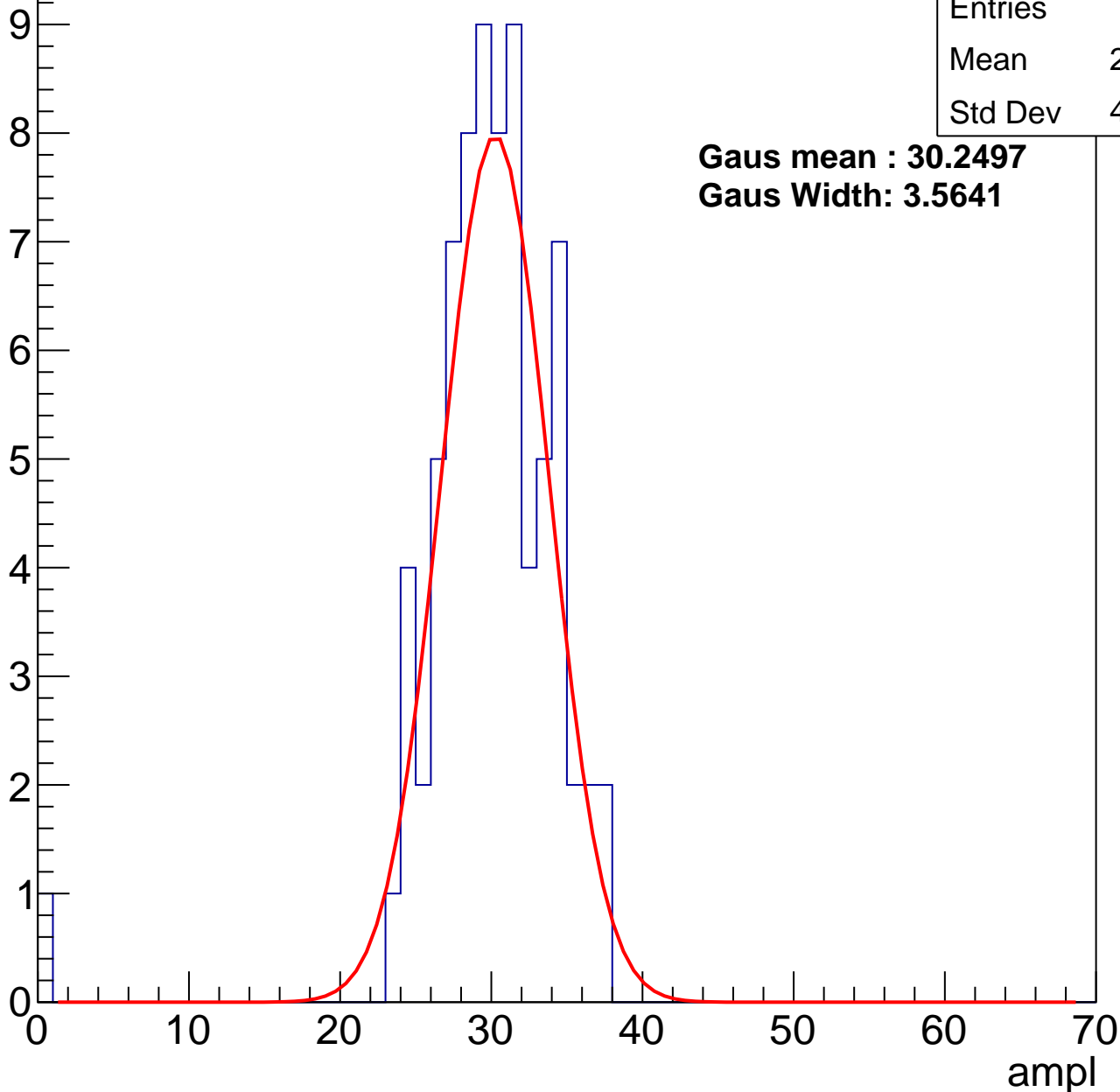
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	29.46
Std Dev	4.739

**Gaus mean : 30.2497**

**Gaus Width: 3.5641**



# B1L102S, U21-ch42, adc1

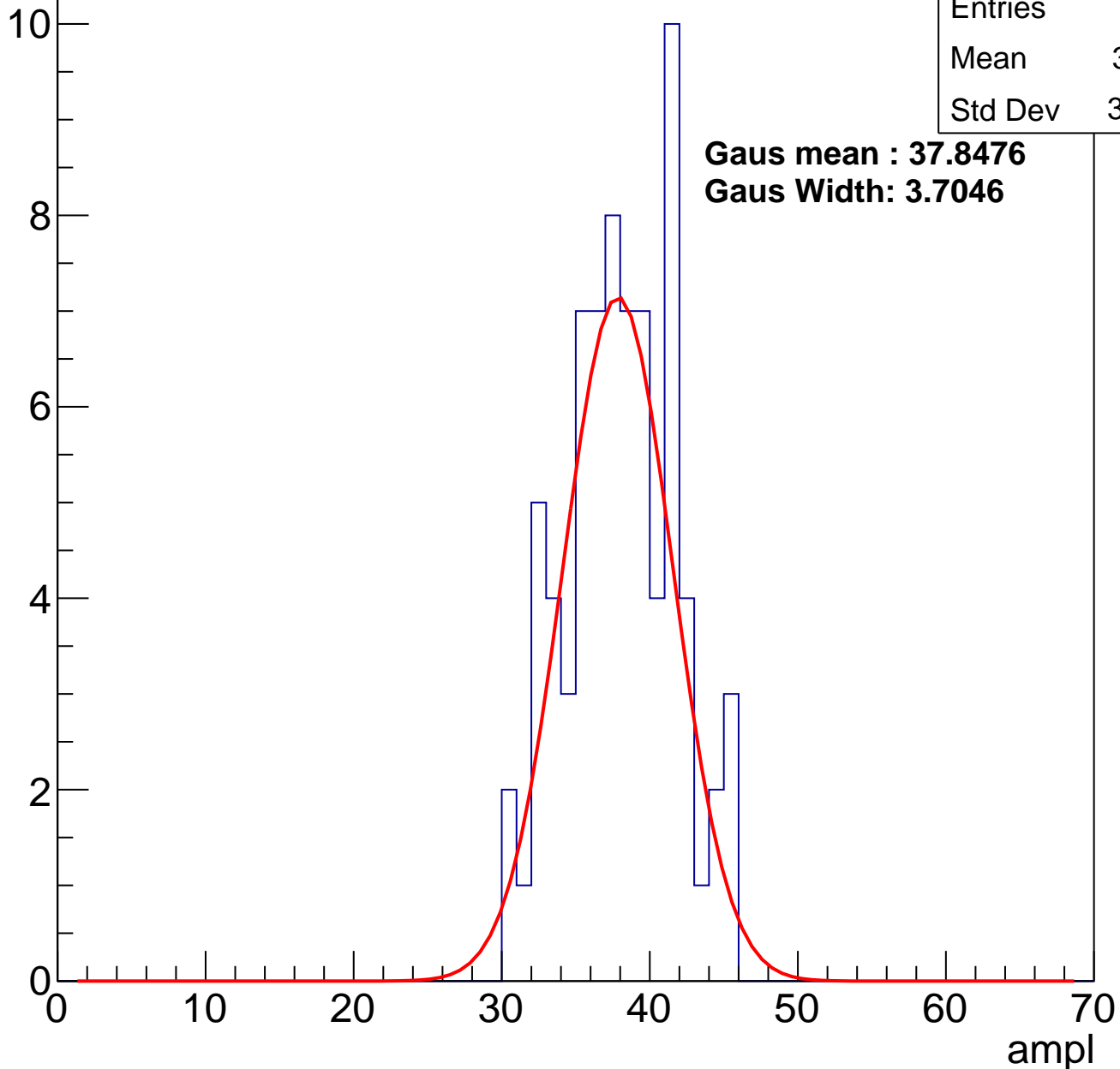
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	75
Mean	37.61
Std Dev	3.677

**Gaus mean : 37.8476**

**Gaus Width: 3.7046**

Entry



# B1L102S, U21-ch42, adc2

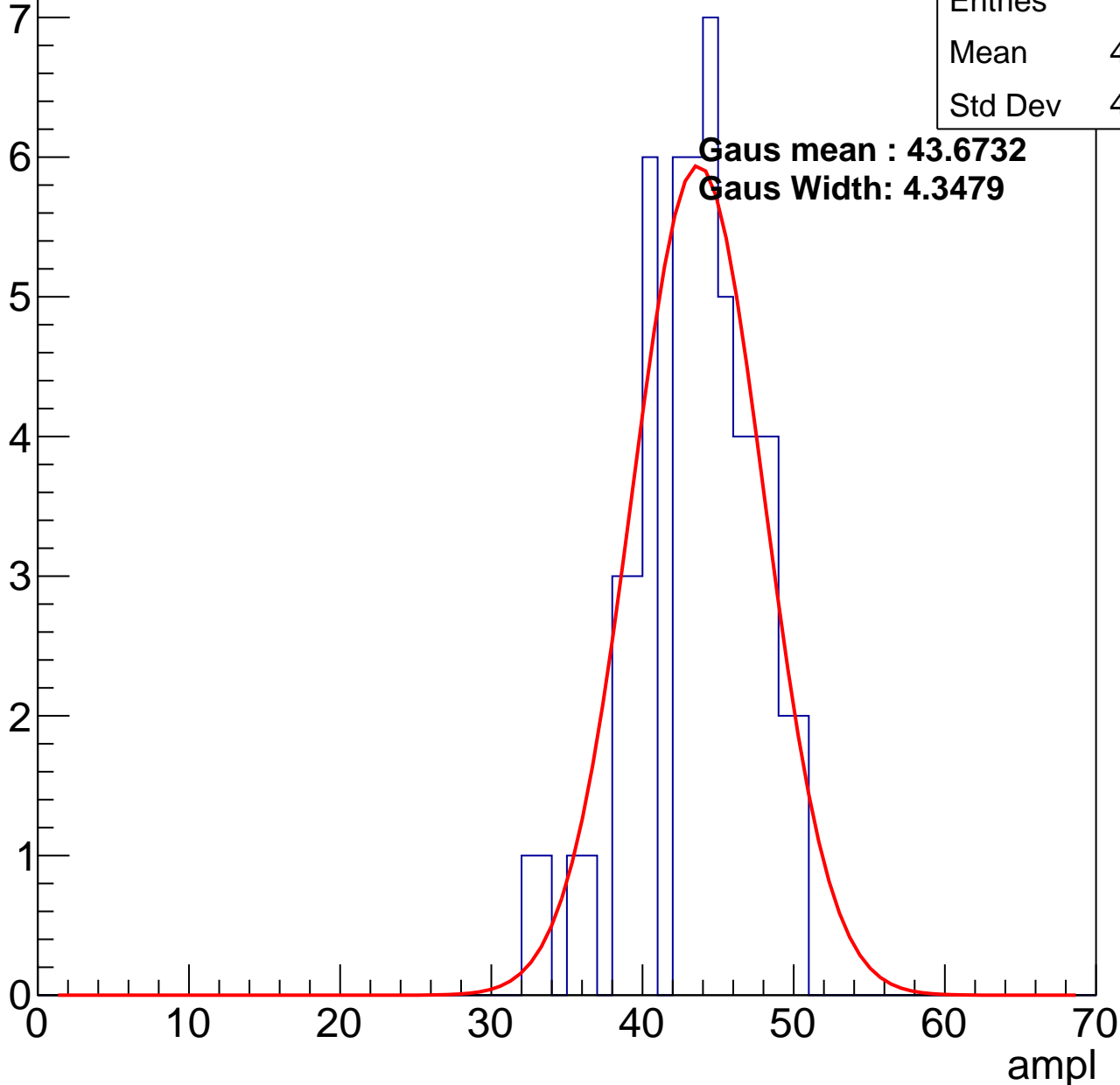
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	43.07
Std Dev	4.039

**Gaus mean : 43.6732**

**Gaus Width: 4.3479**

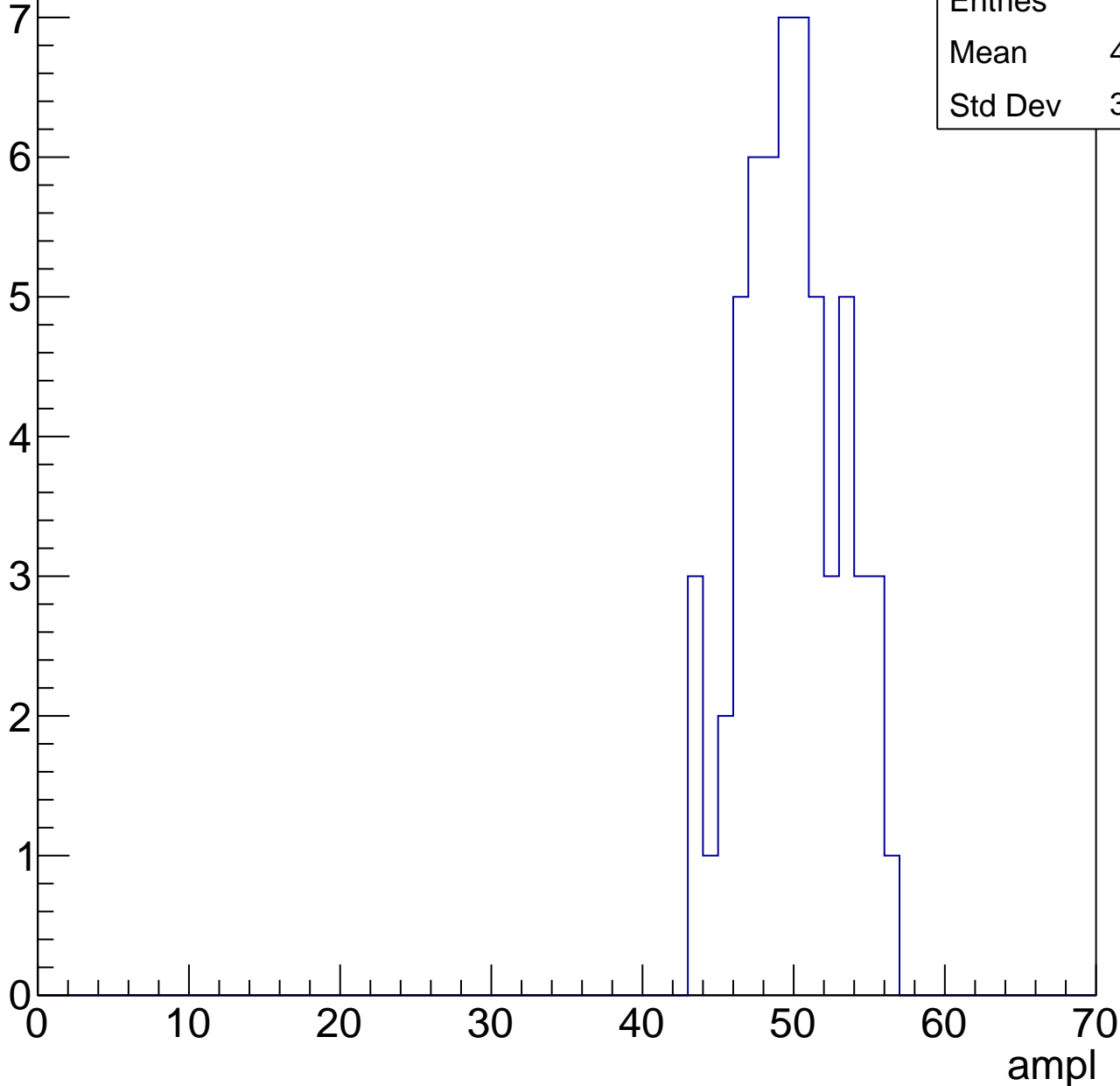


# B1L102S, U21-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	49.39
Std Dev	3.238

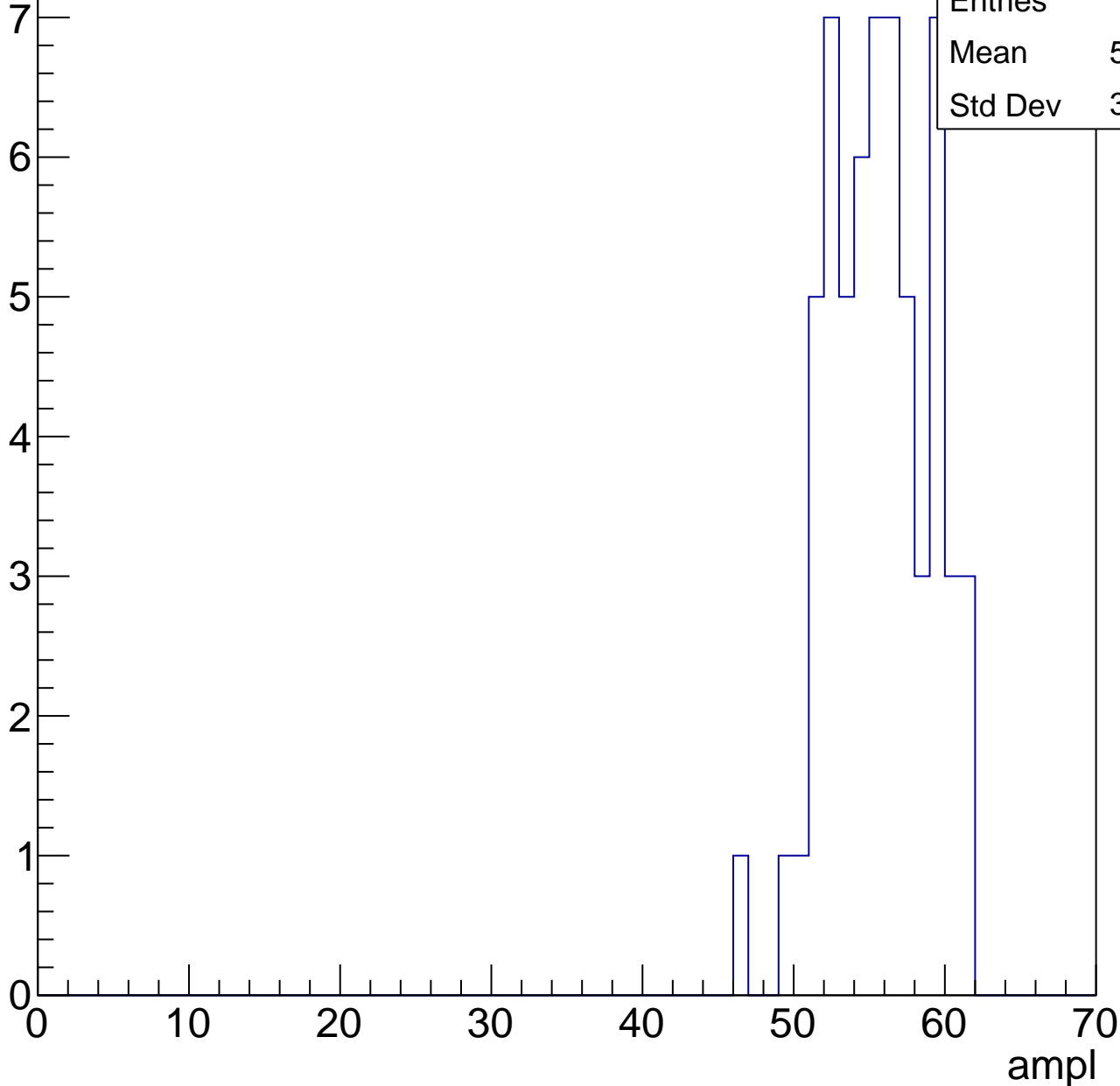


# B1L102S, U21-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	55.16
Std Dev	3.285

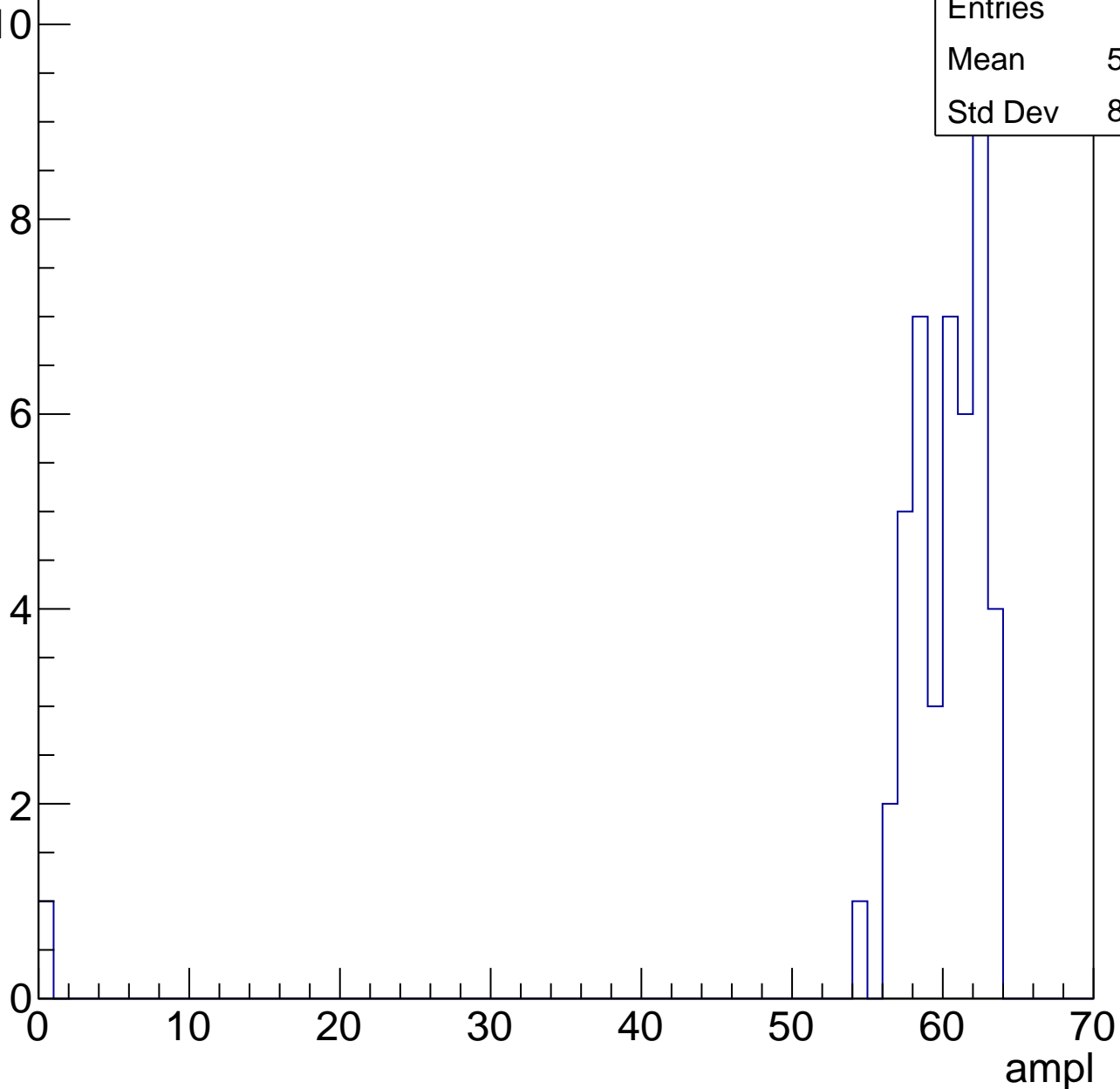


# B1L102S, U21-ch42, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	58.52
Std Dev	8.999

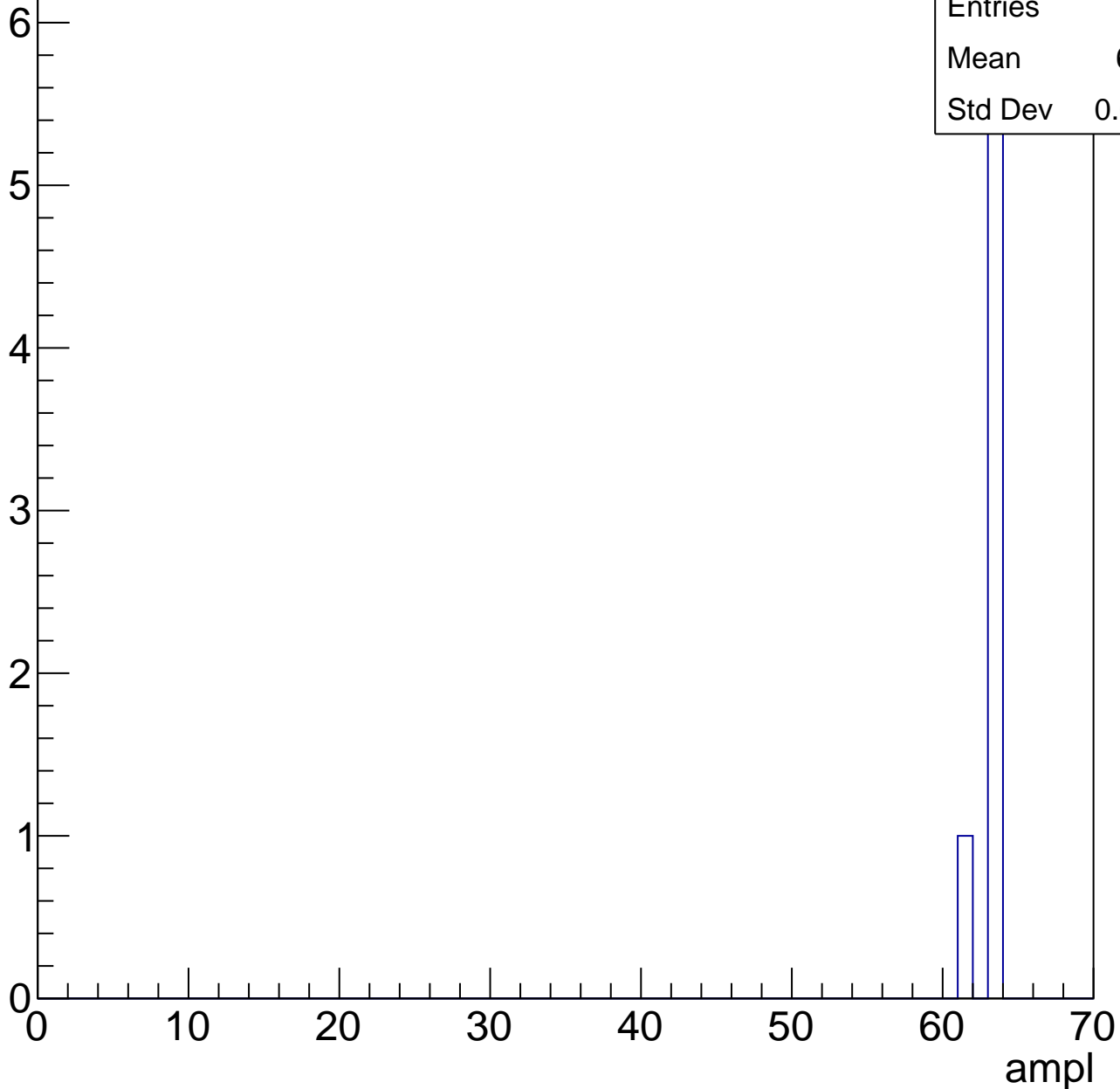


# B1L102S, U21-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	7
Mean	62.71
Std Dev	0.6999





# B1L102S, U21-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch43, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	70
Mean	28.21
Std Dev	3.589

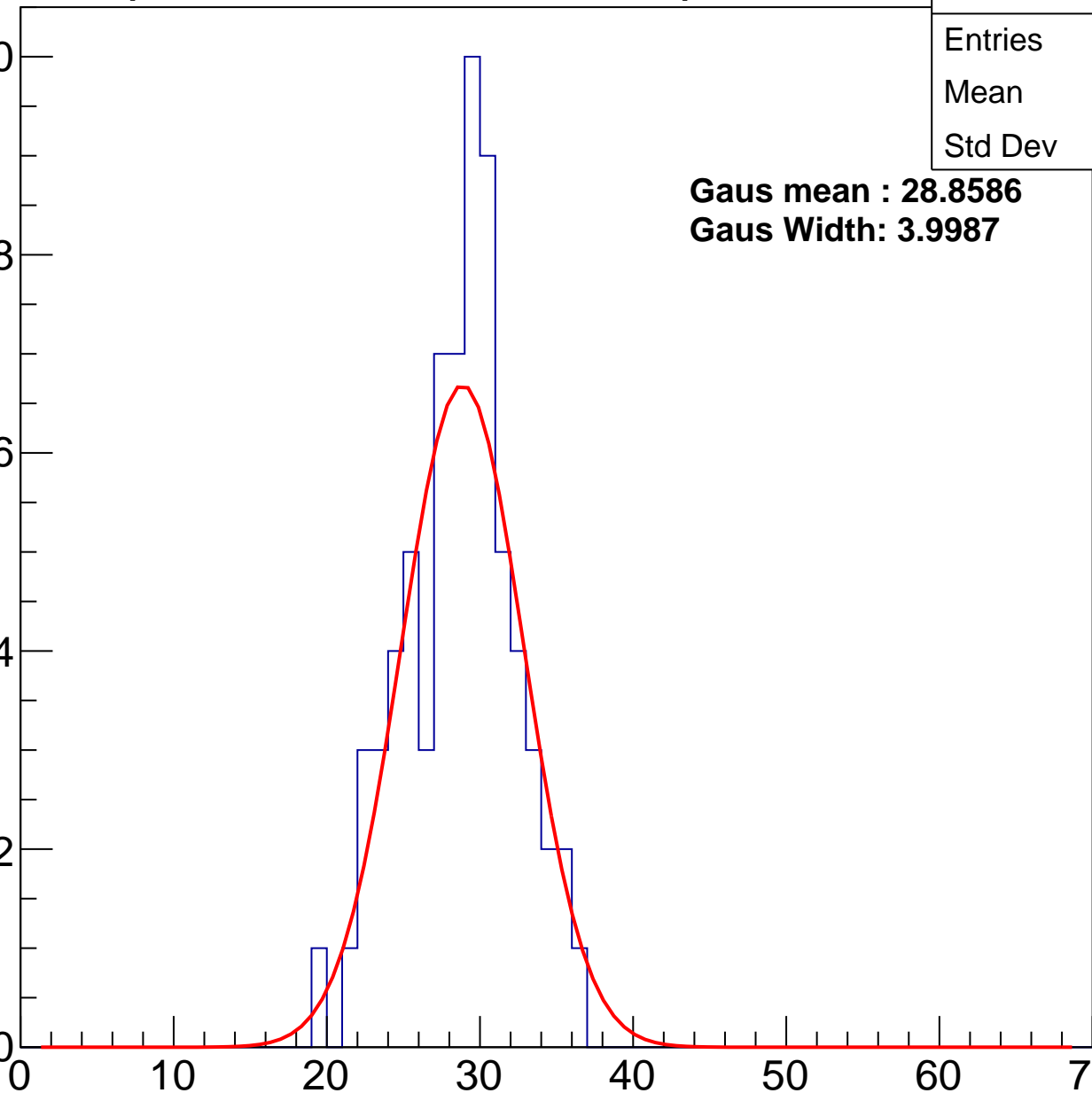
**Gaus mean : 28.8586**

**Gaus Width: 3.9987**

Entry

10  
8  
6  
4  
2  
0

ampl



# B1L102S, U21-ch43, adc1

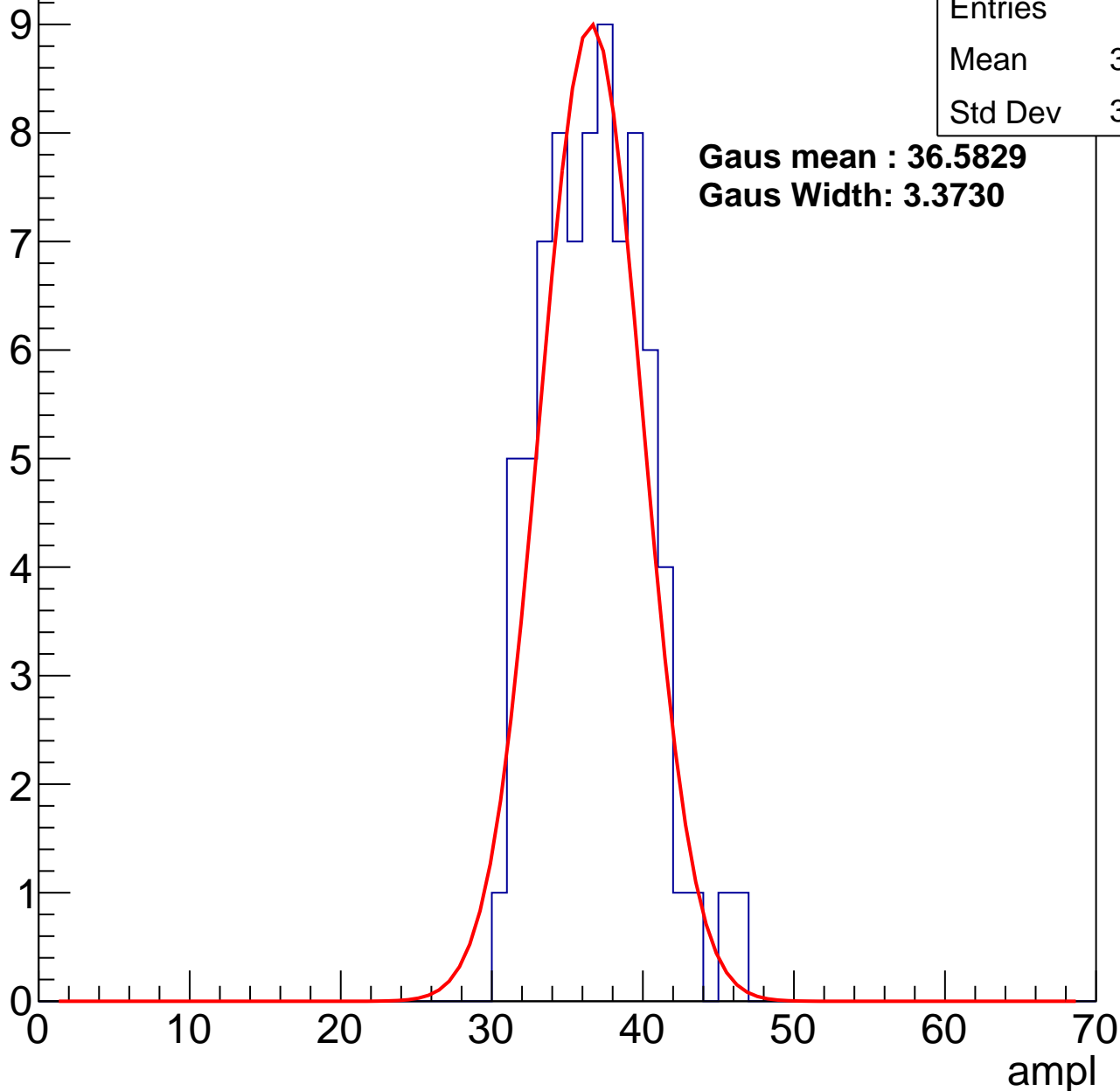
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	36.35
Std Dev	3.383

**Gaus mean : 36.5829**

**Gaus Width: 3.3730**



# B1L102S, U21-ch43, adc2

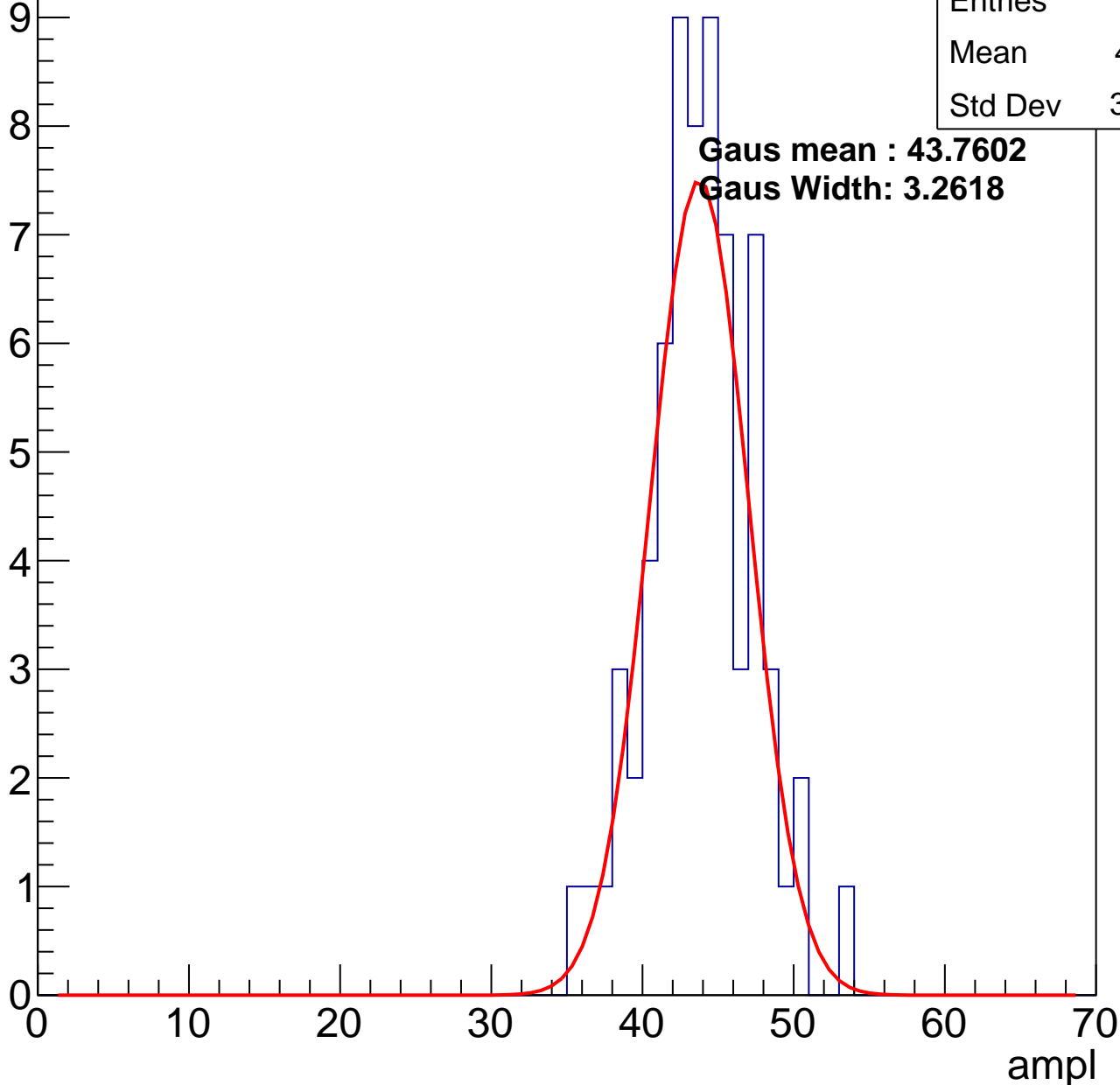
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	43.41
Std Dev	3.427

**Gaus mean : 43.7602**

**Gaus Width: 3.2618**

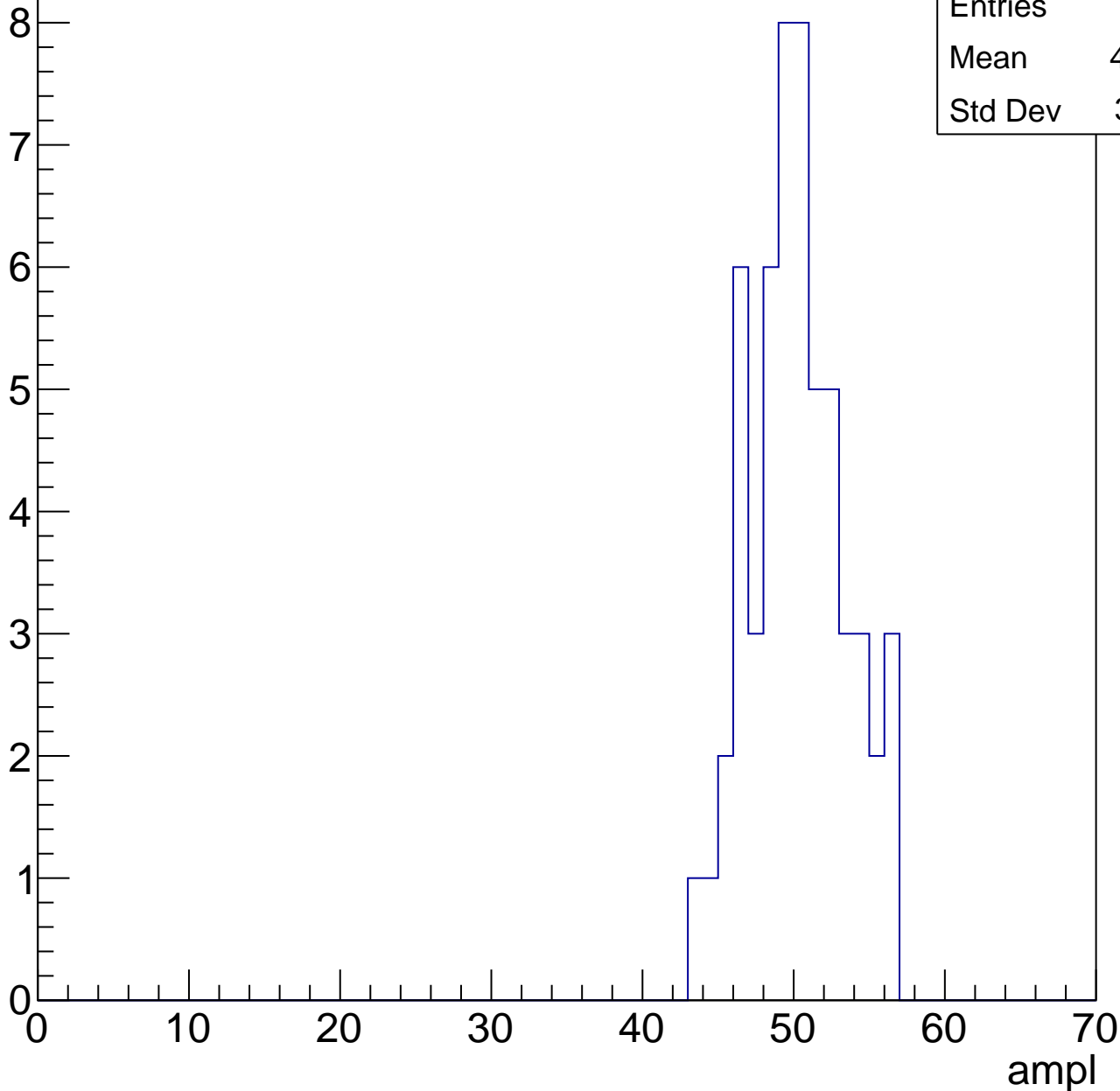


# B1L102S, U21-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

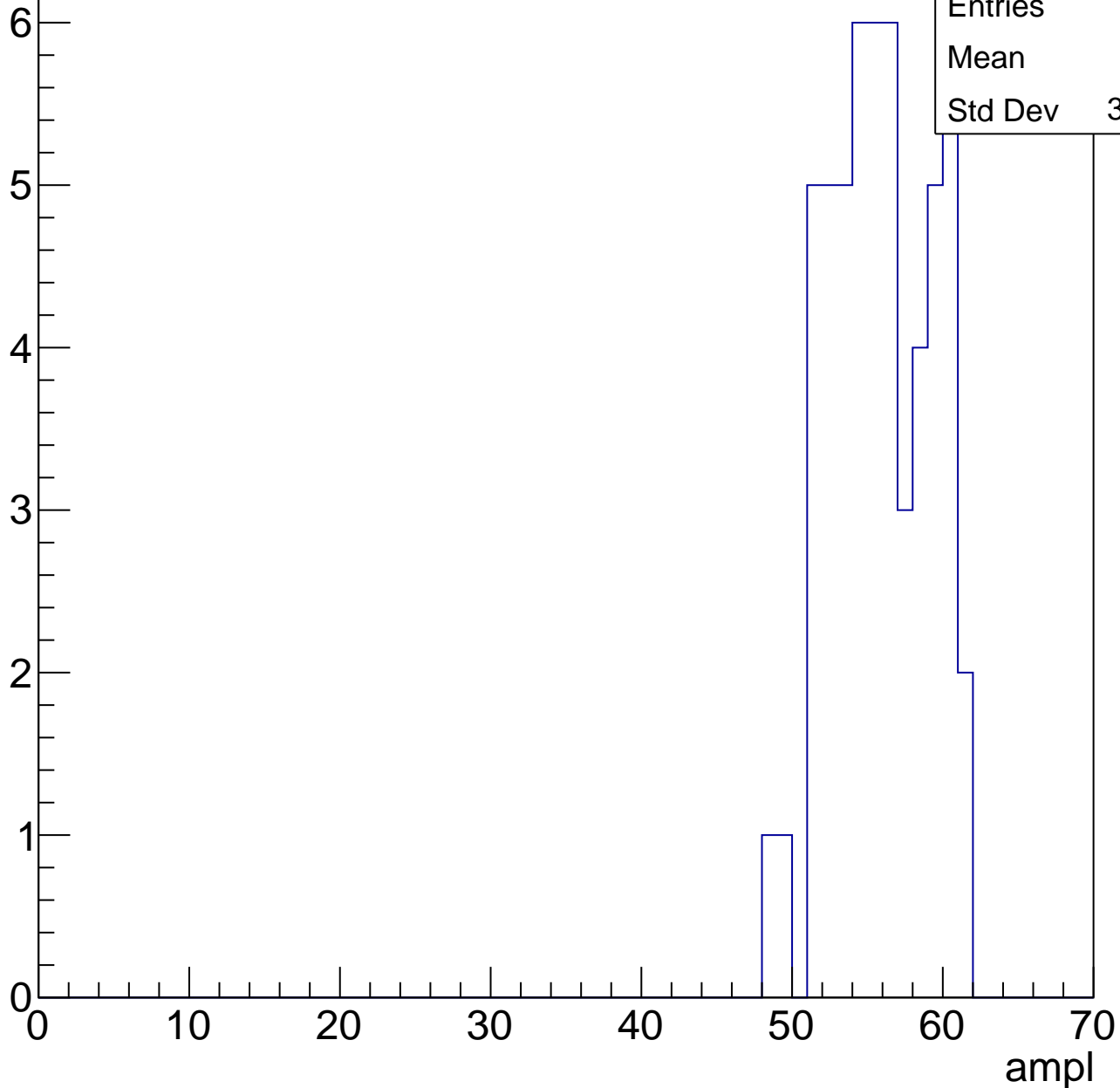
Entries	56
Mean	49.79
Std Dev	3.121



# B1L102S, U21-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



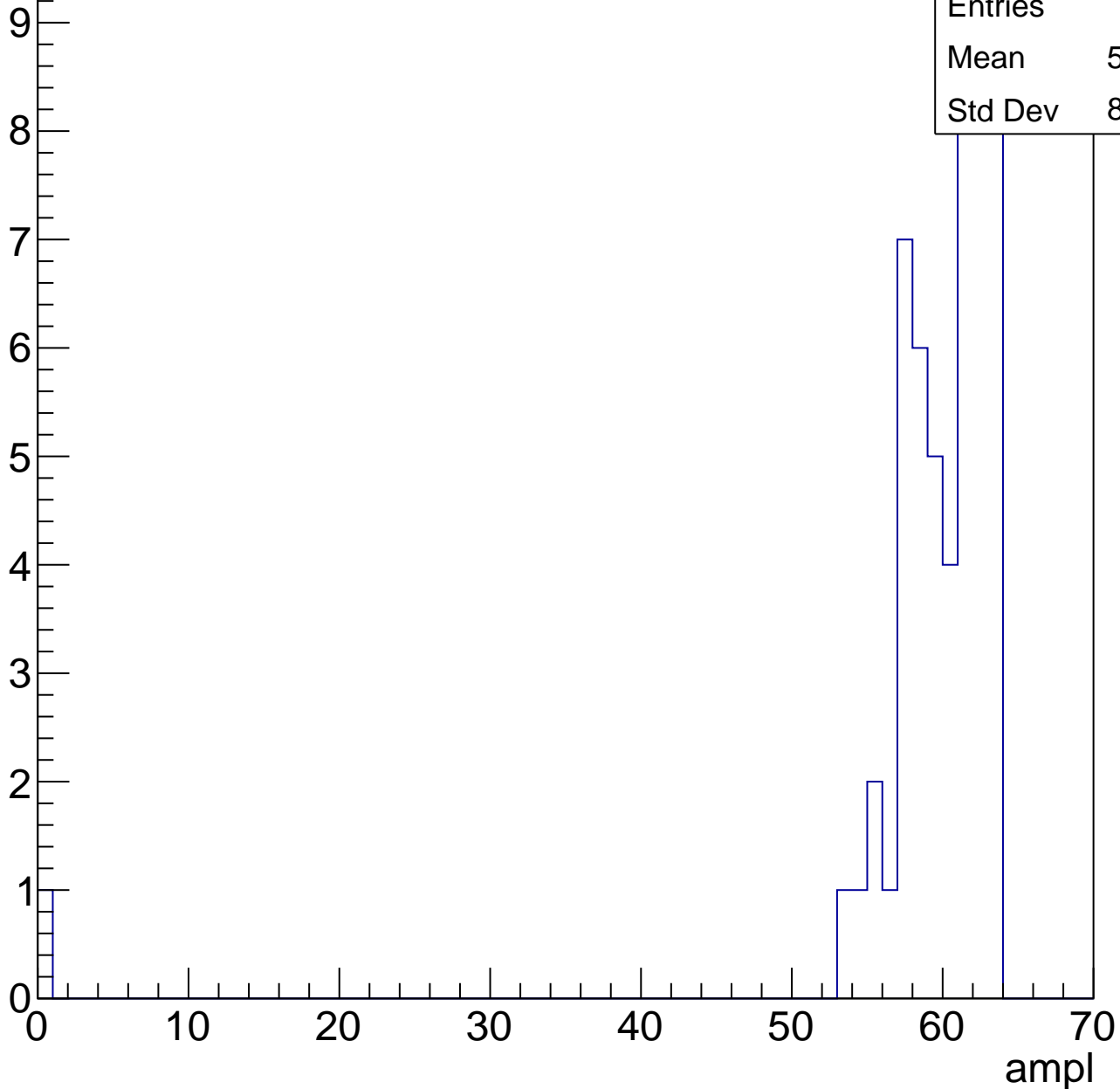
Entries	55
Mean	55.4
Std Dev	3.256

# B1L102S, U21-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	58.67
Std Dev	8.468



# B1L102S, U21-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

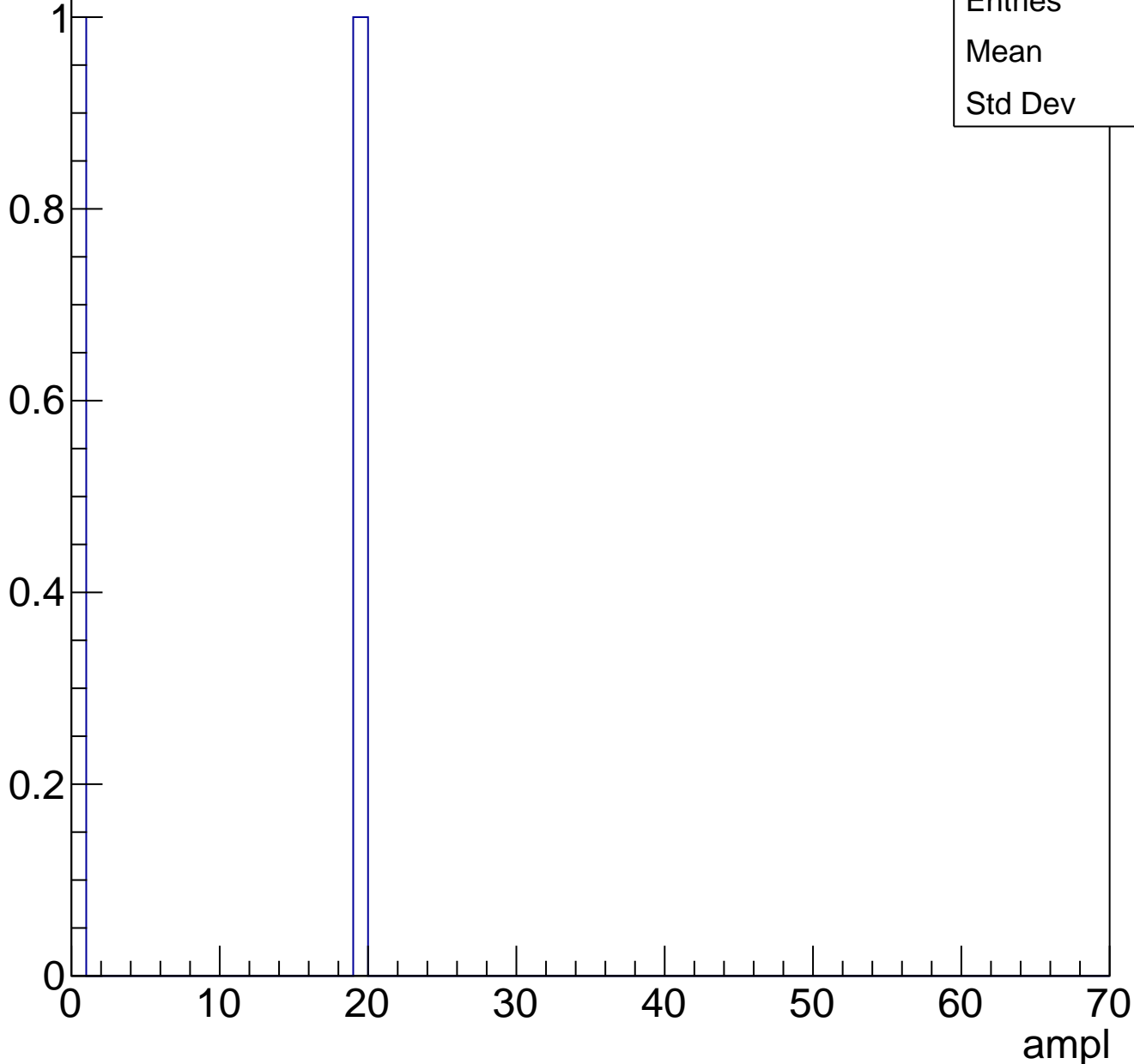




# B1L102S, U21-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	9.5
Std Dev	9.5

# B1L102S, U21-ch44, adc0

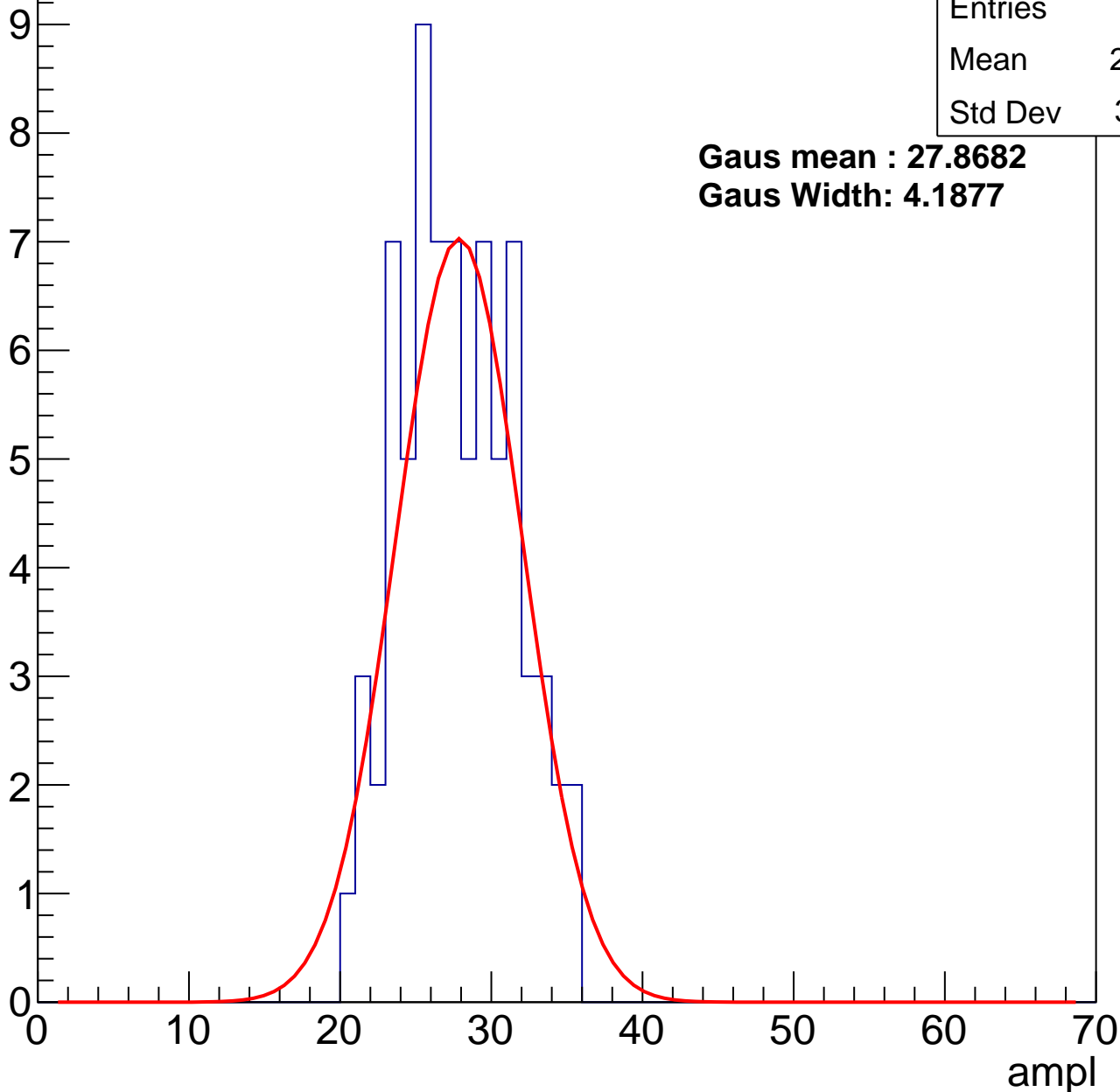
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	27.29
Std Dev	3.651

**Gaus mean : 27.8682**

**Gaus Width: 4.1877**



# B1L102S, U21-ch44, adc1

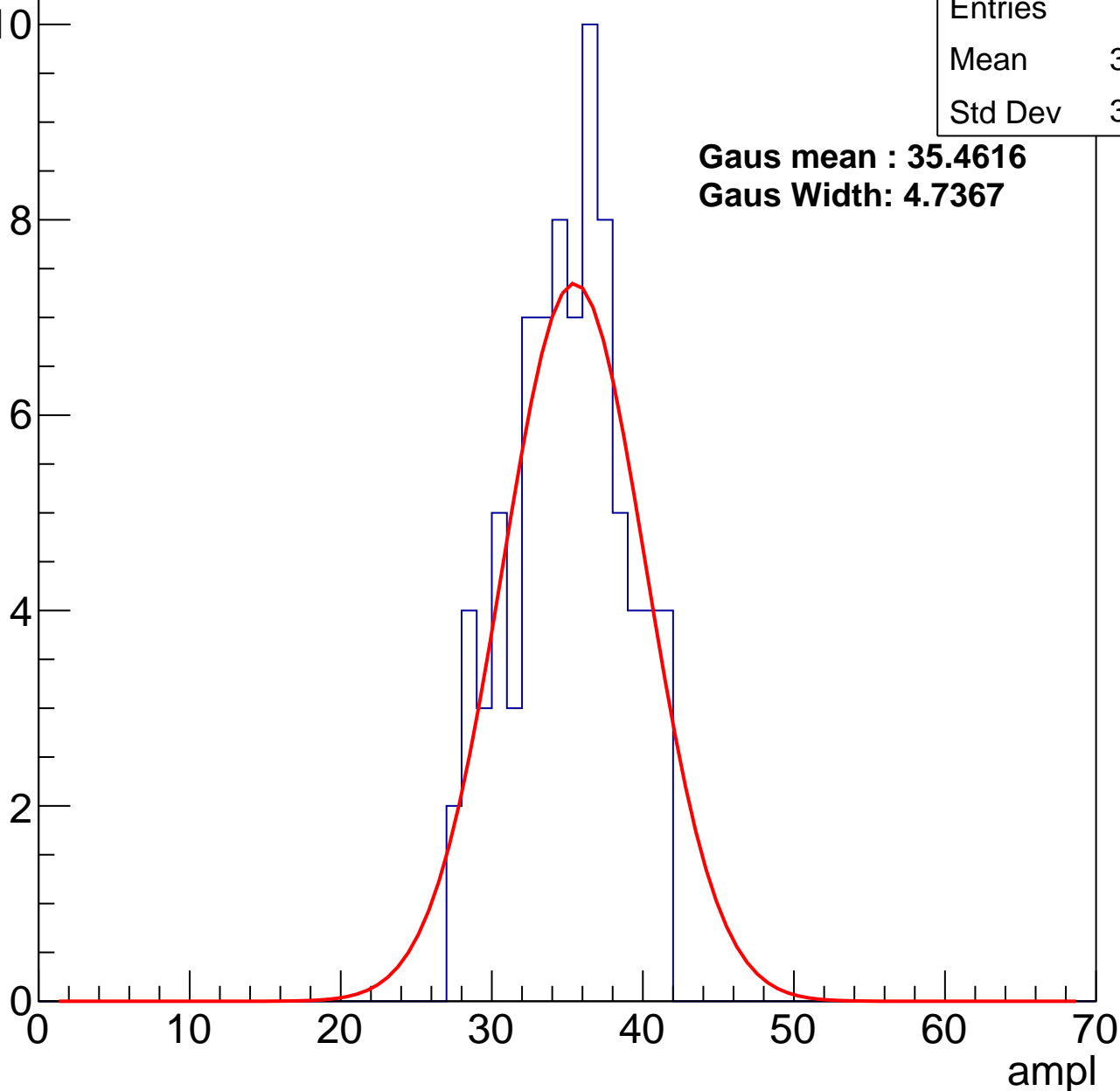
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	81
Mean	34.49
Std Dev	3.649

**Gaus mean : 35.4616**

**Gaus Width: 4.7367**



# B1L102S, U21-ch44, adc2

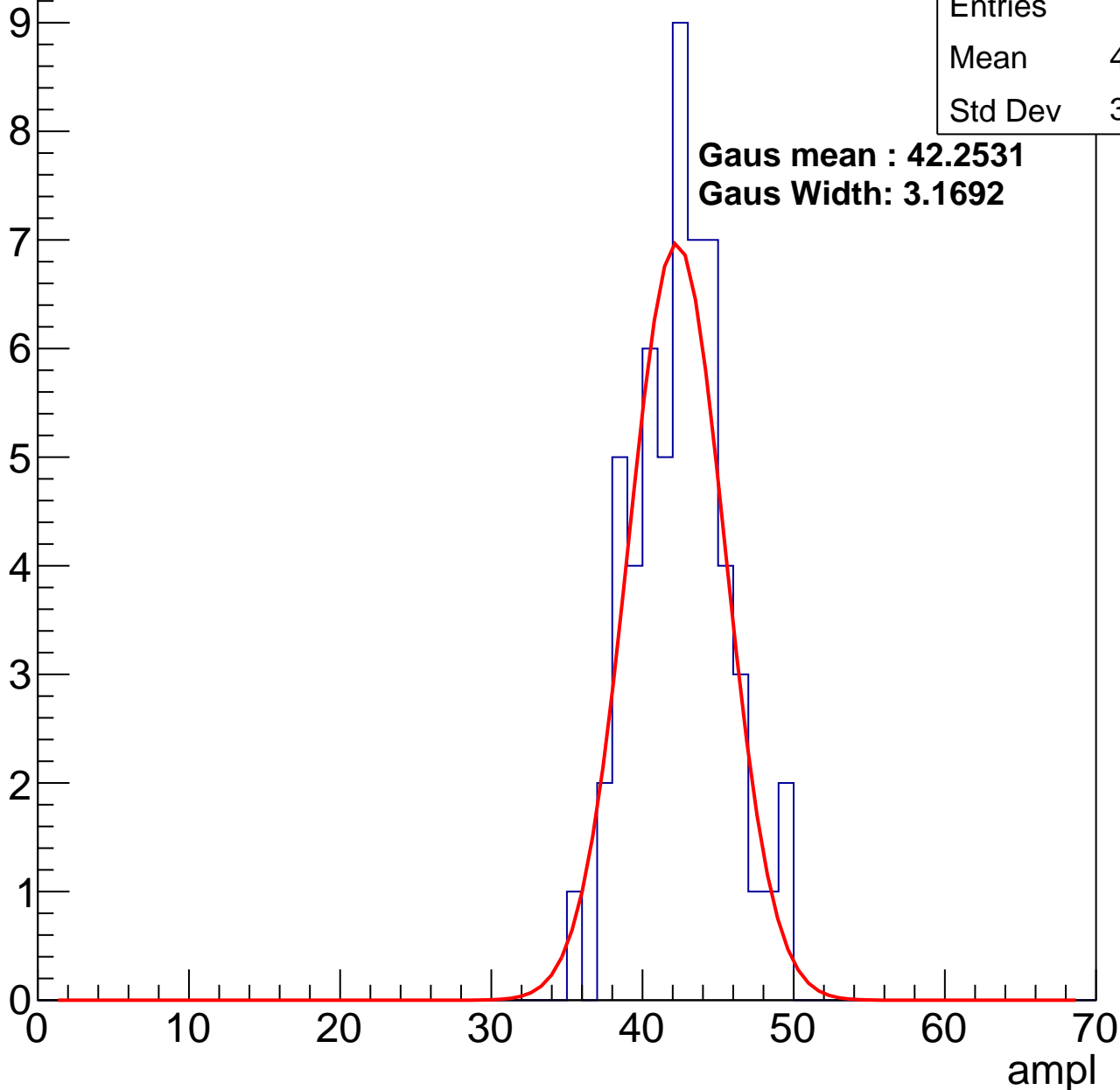
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	42.07
Std Dev	3.025

**Gaus mean : 42.2531**

**Gaus Width: 3.1692**

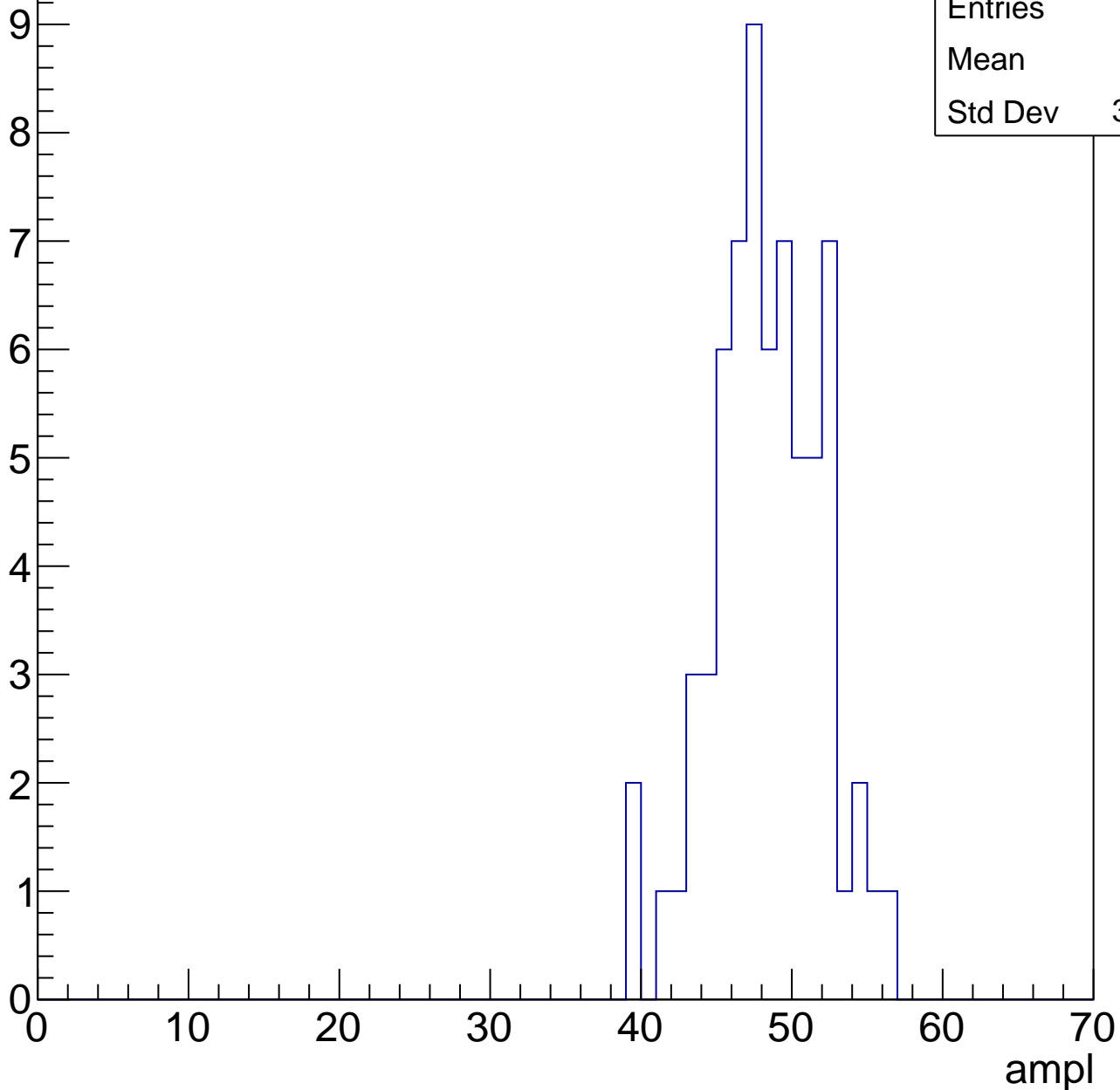


# B1L102S, U21-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	47.9
Std Dev	3.571

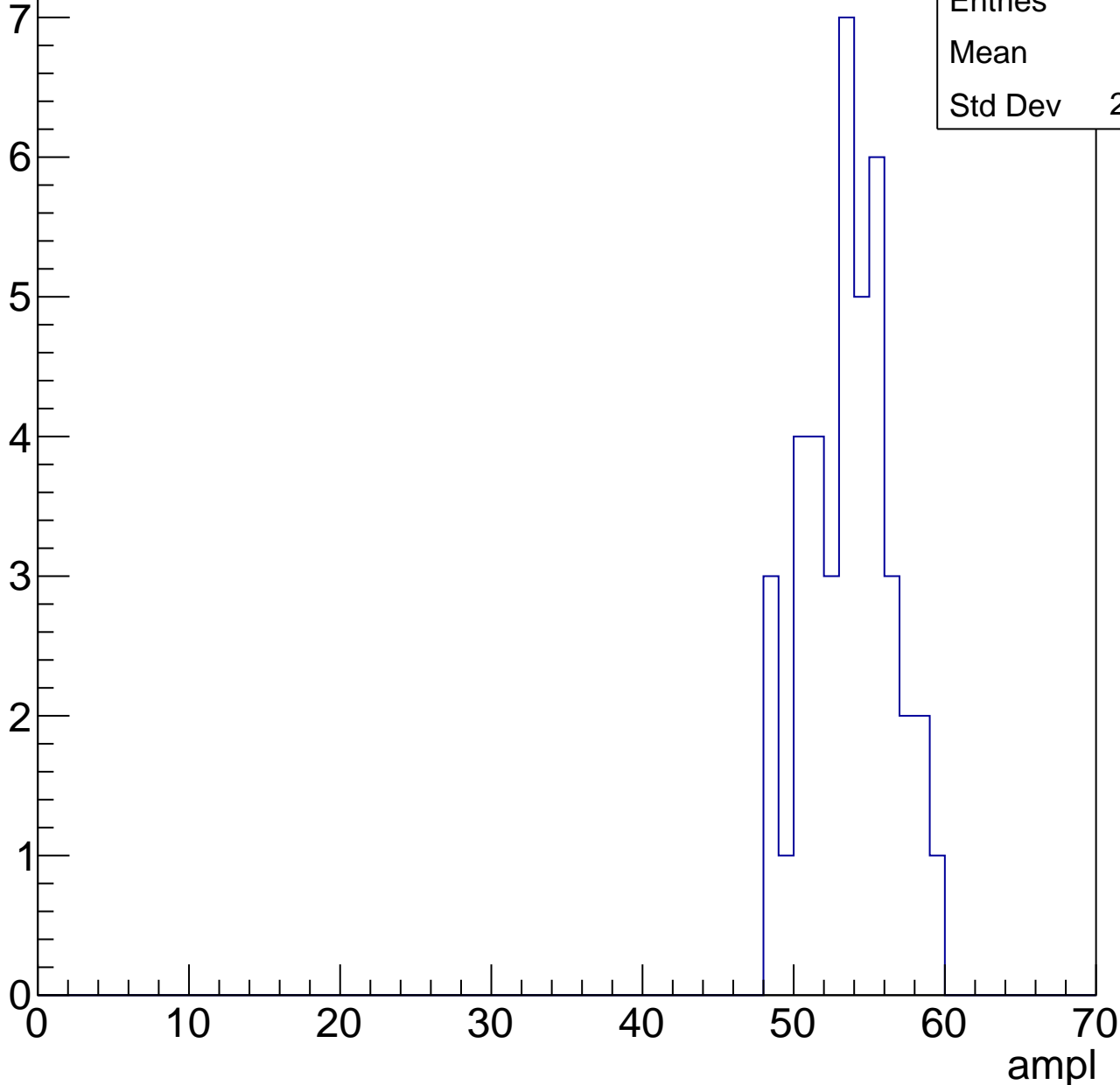


# B1L102S, U21-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	41
Mean	53.2
Std Dev	2.787

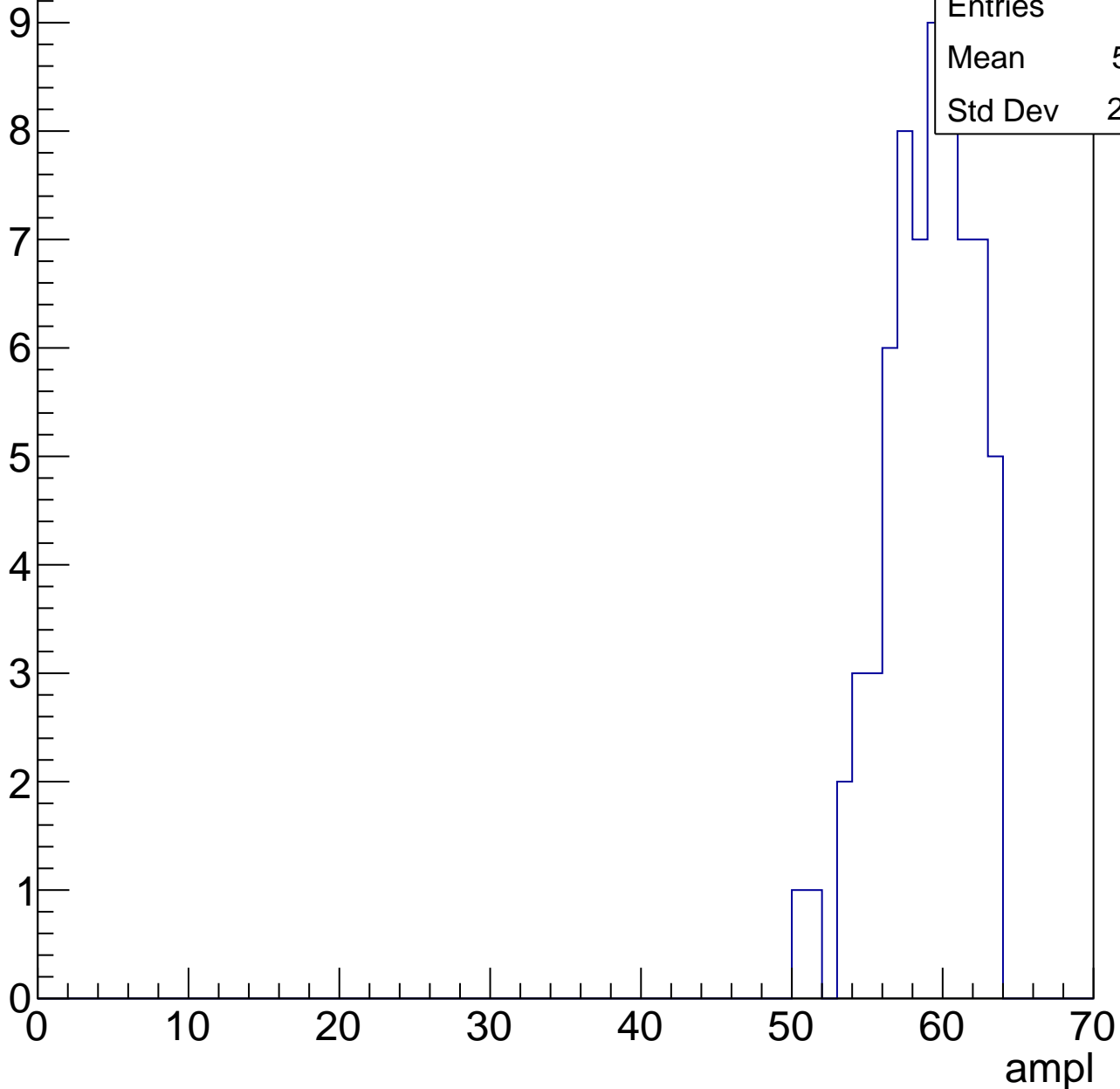


# B1L102S, U21-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	58.51
Std Dev	2.963

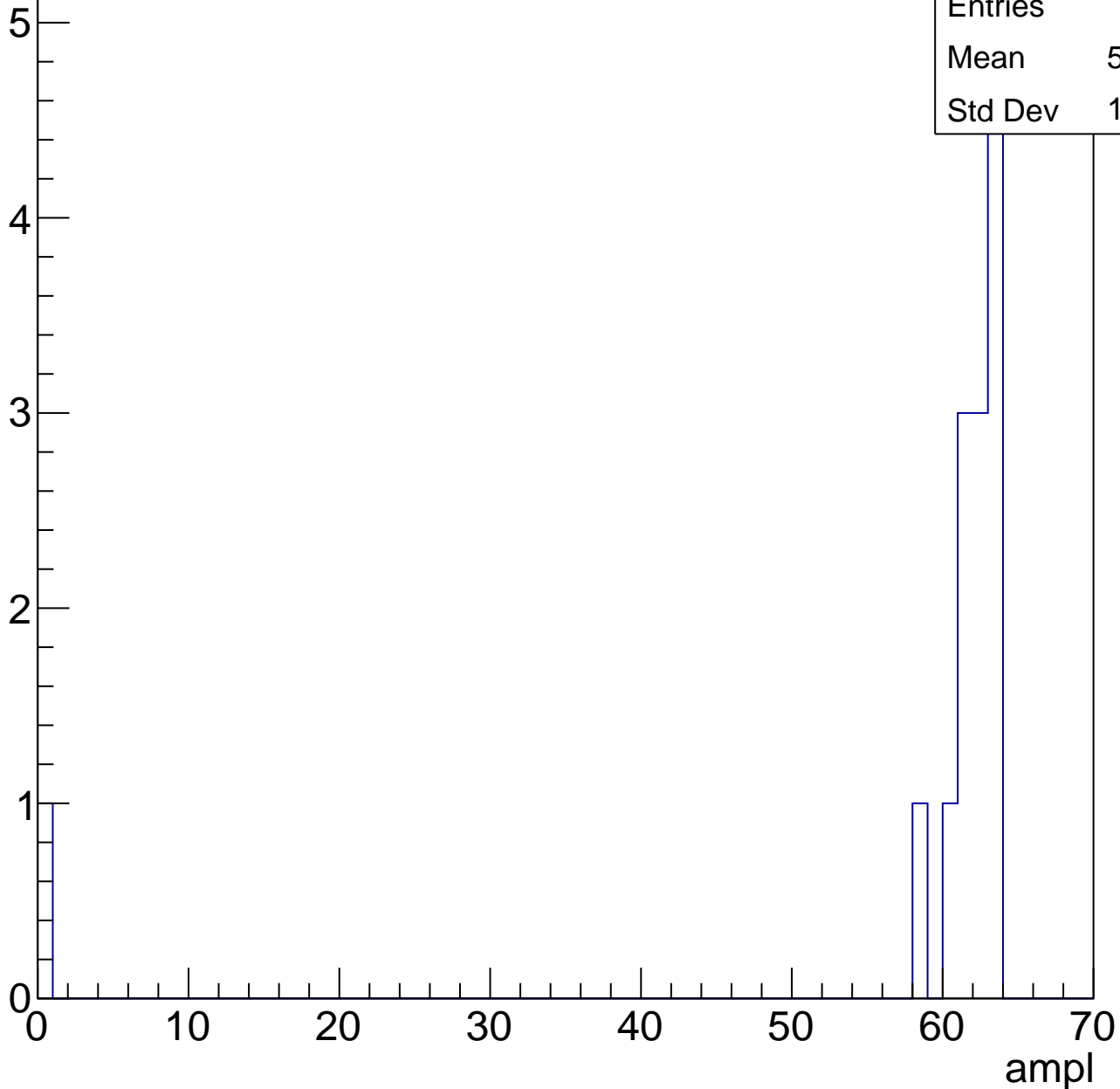


# B1L102S, U21-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	14
Mean	57.29
Std Dev	15.95





# B1L102S, U21-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch45, adc0

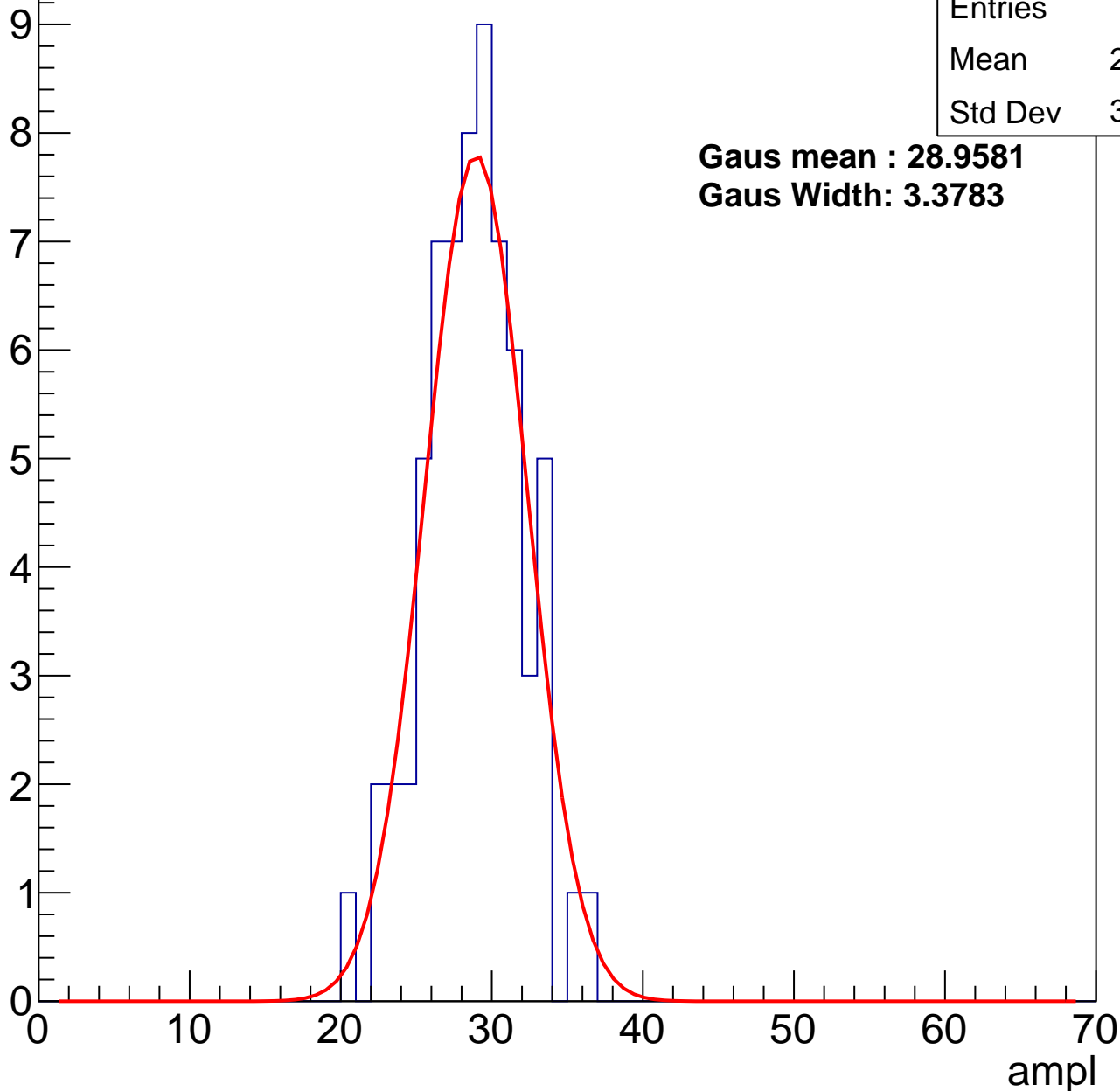
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	28.29
Std Dev	3.185

**Gaus mean : 28.9581**

**Gaus Width: 3.3783**



# B1L102S, U21-ch45, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	77
Mean	35.83
Std Dev	3.521

**Gaus mean : 35.9196**

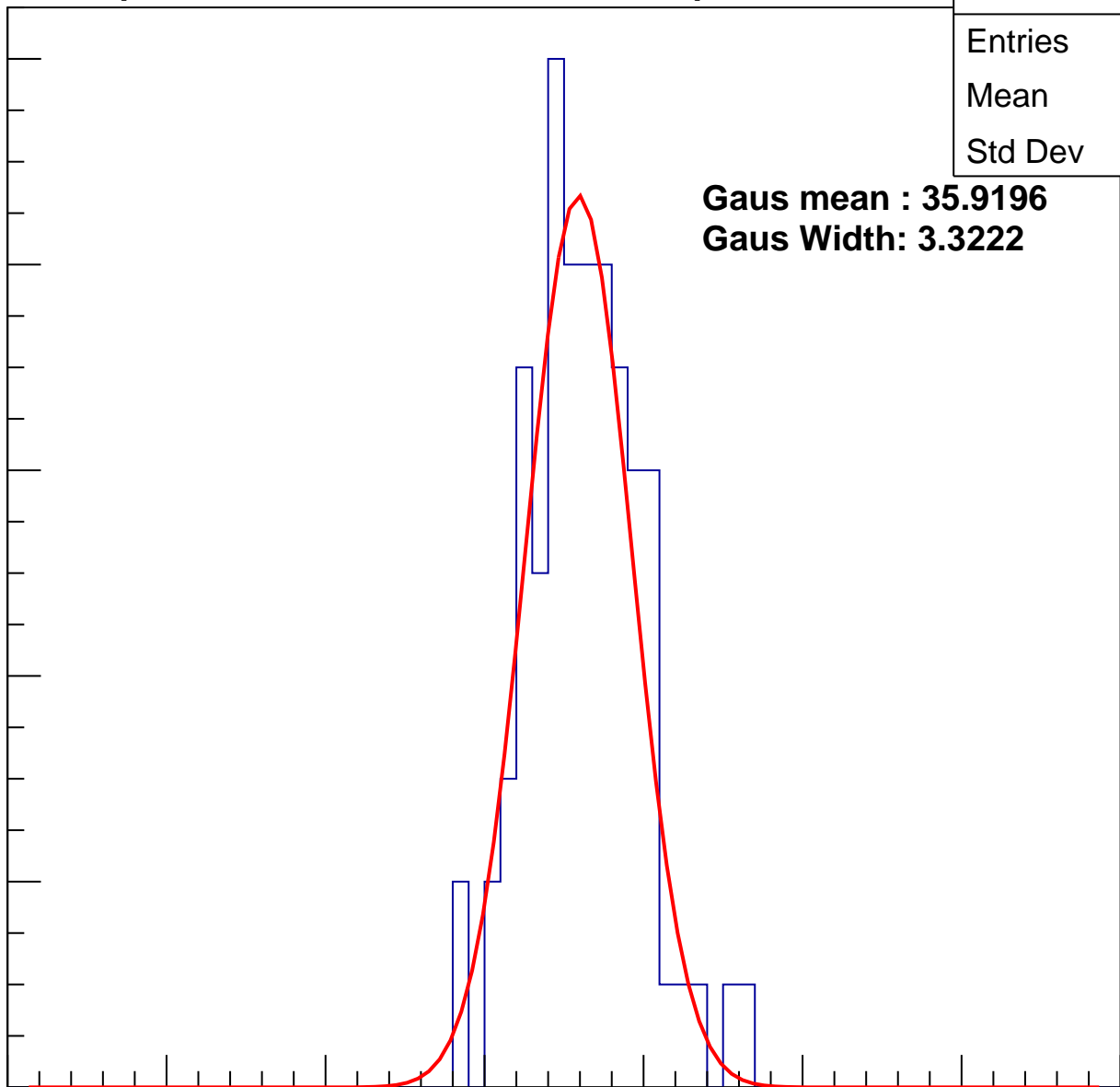
**Gaus Width: 3.3222**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U21-ch45, adc2

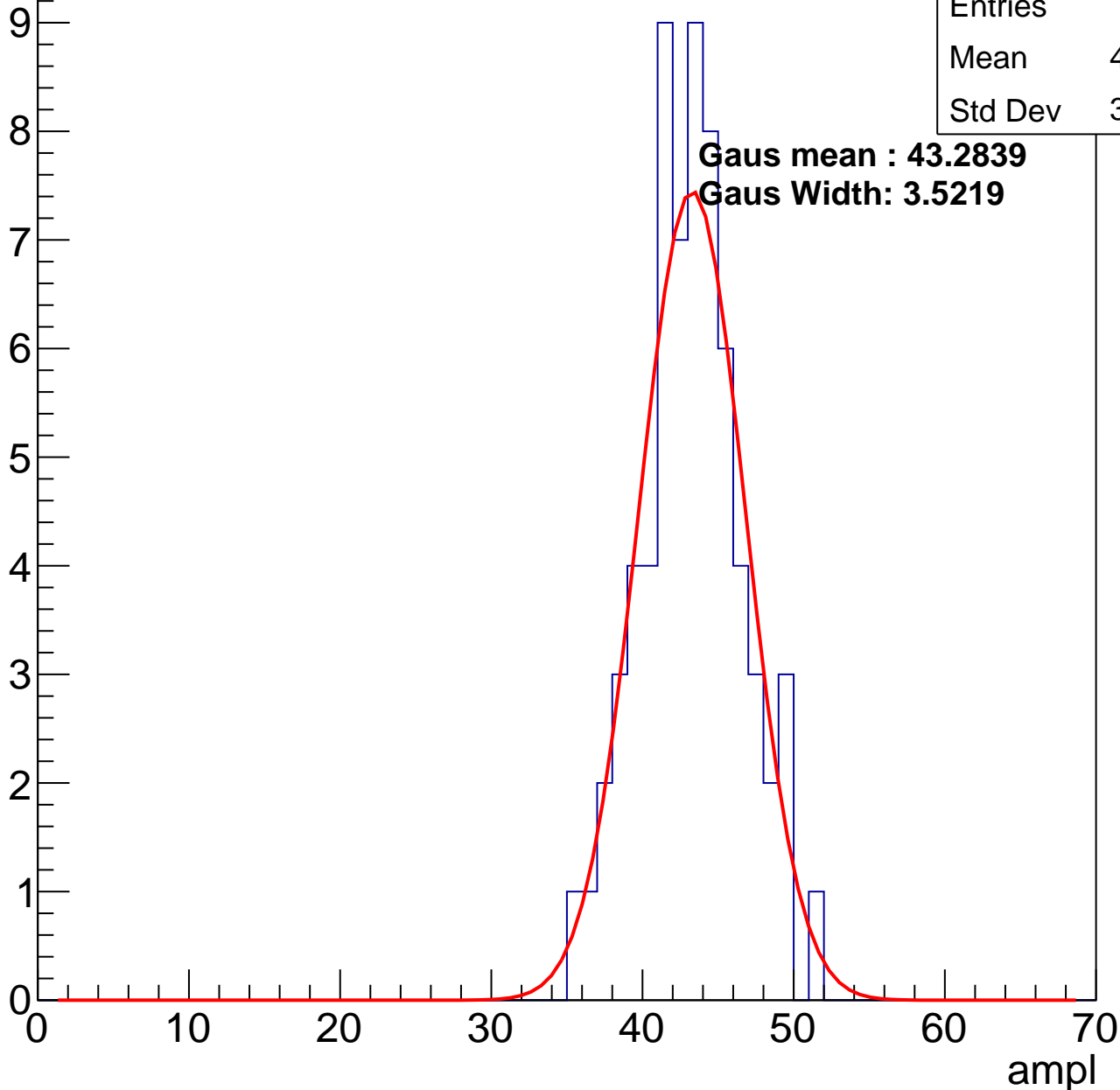
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	42.78
Std Dev	3.318

**Gaus mean : 43.2839**

**Gaus Width: 3.5219**



# B1L102S, U21-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

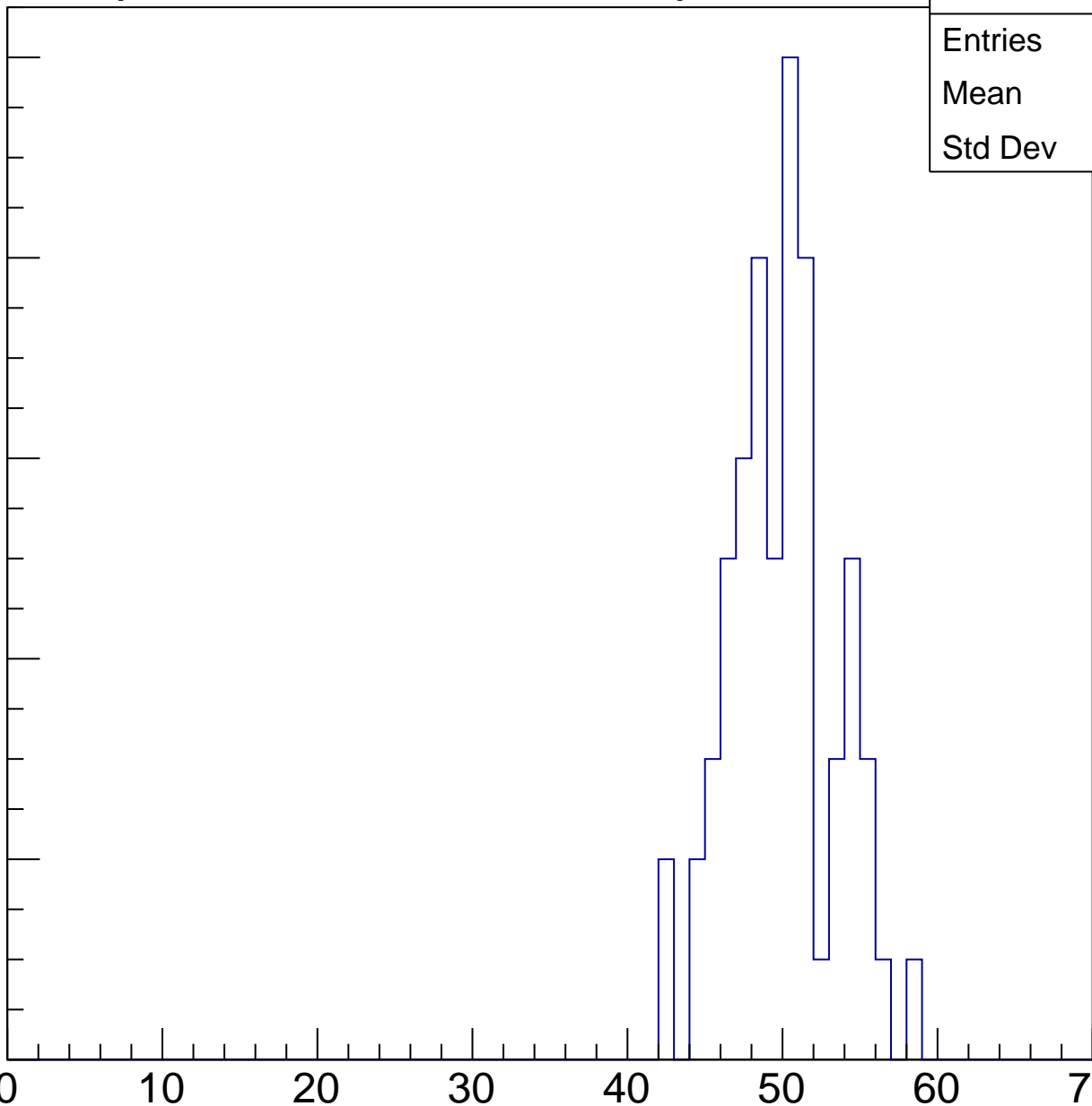
Entries	63
Mean	49.46
Std Dev	3.384

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

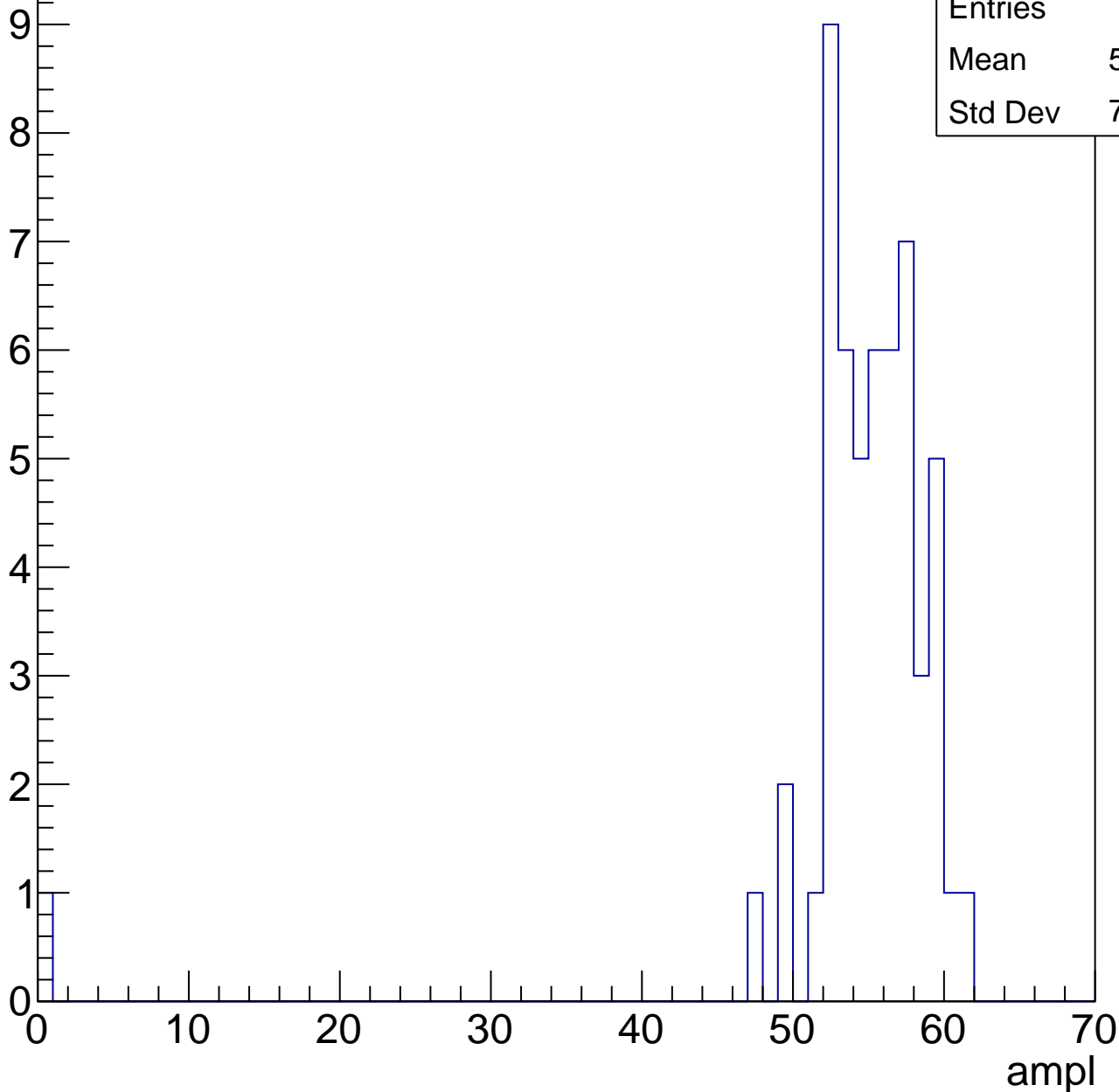


# B1L102S, U21-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	53.83
Std Dev	7.953

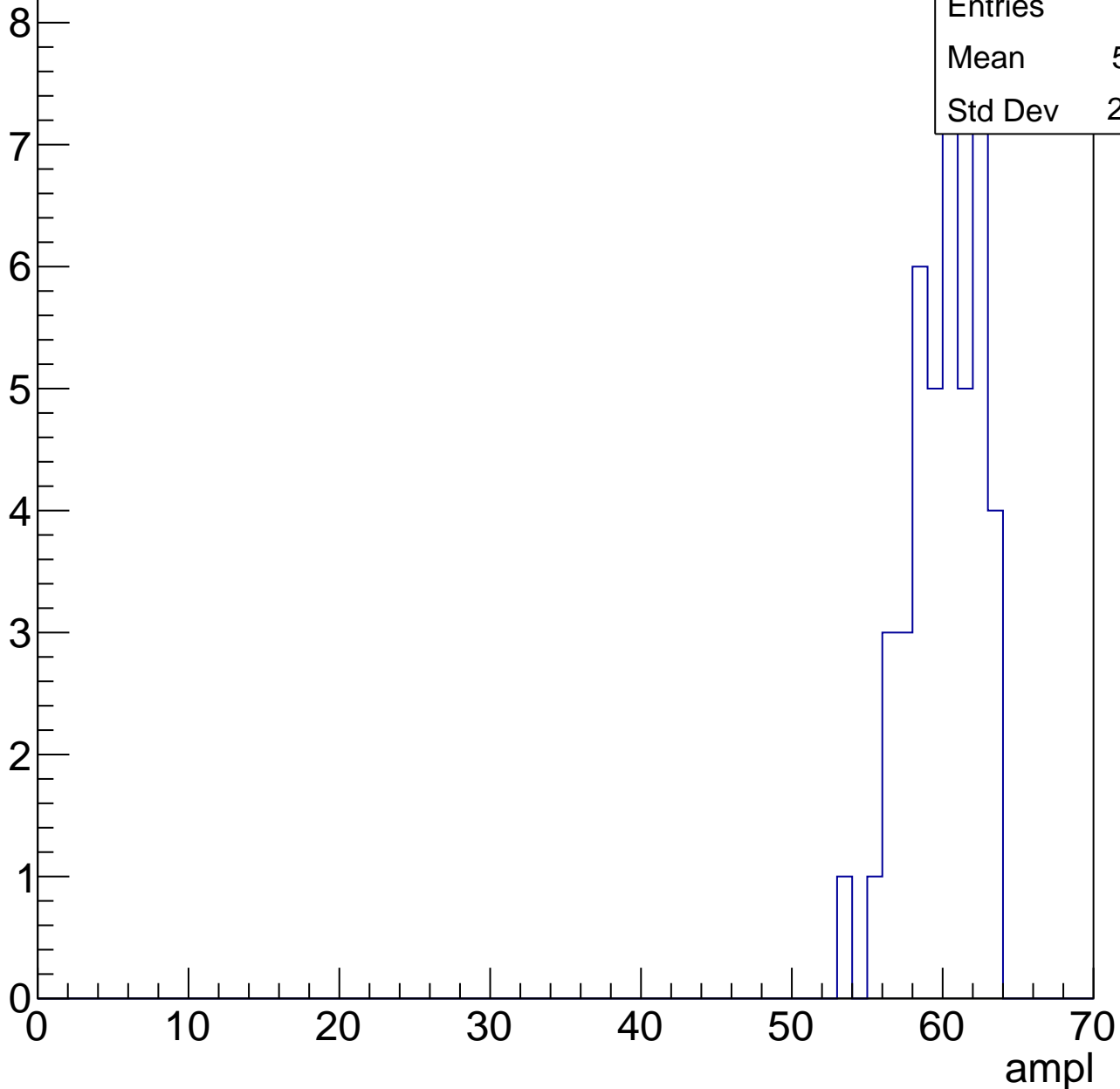


# B1L102S, U21-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	44
Mean	59.61
Std Dev	2.357

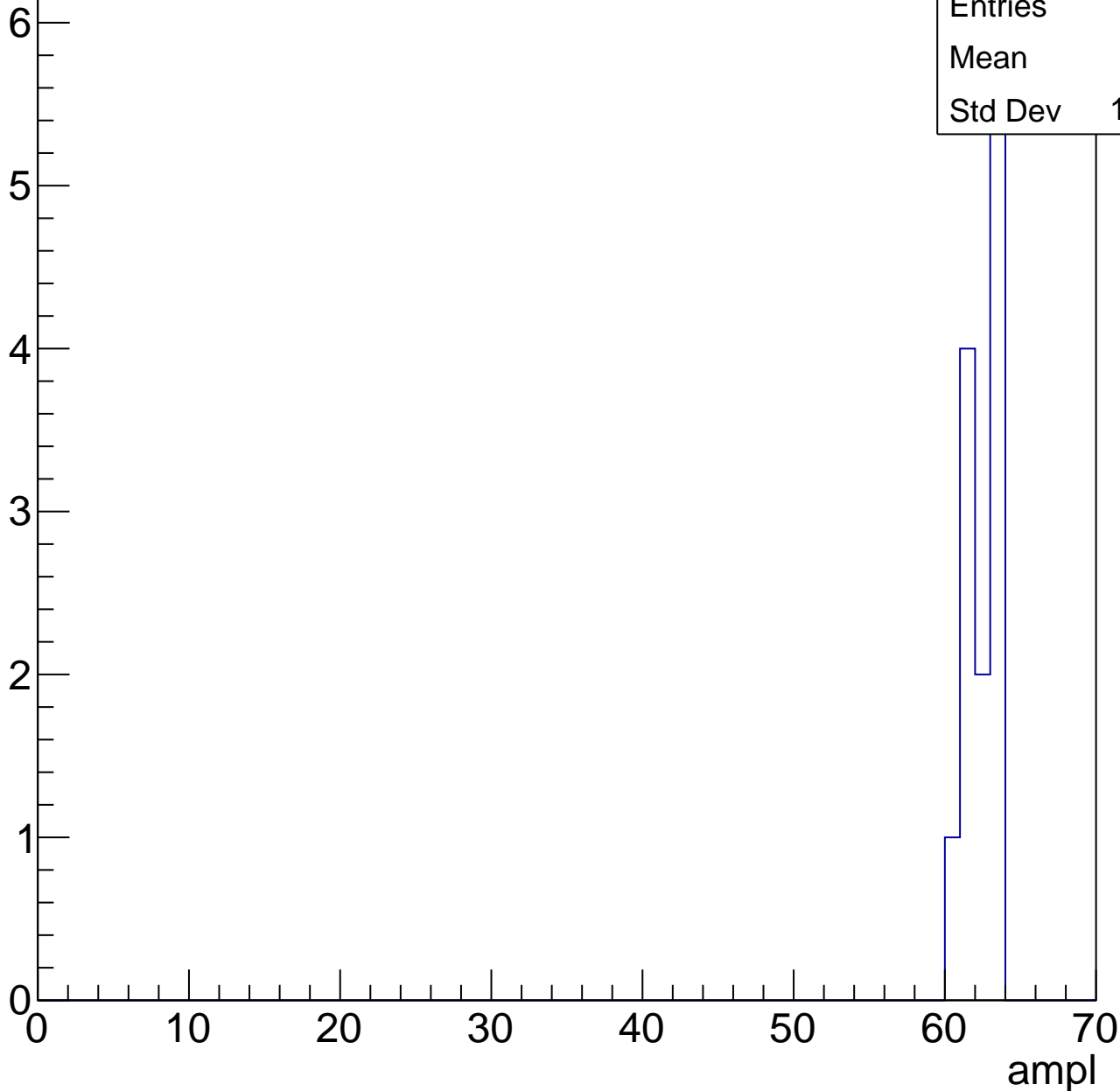


# B1L102S, U21-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	13
Mean	62
Std Dev	1.038





# B1L102S, U21-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U21-ch46, adc0

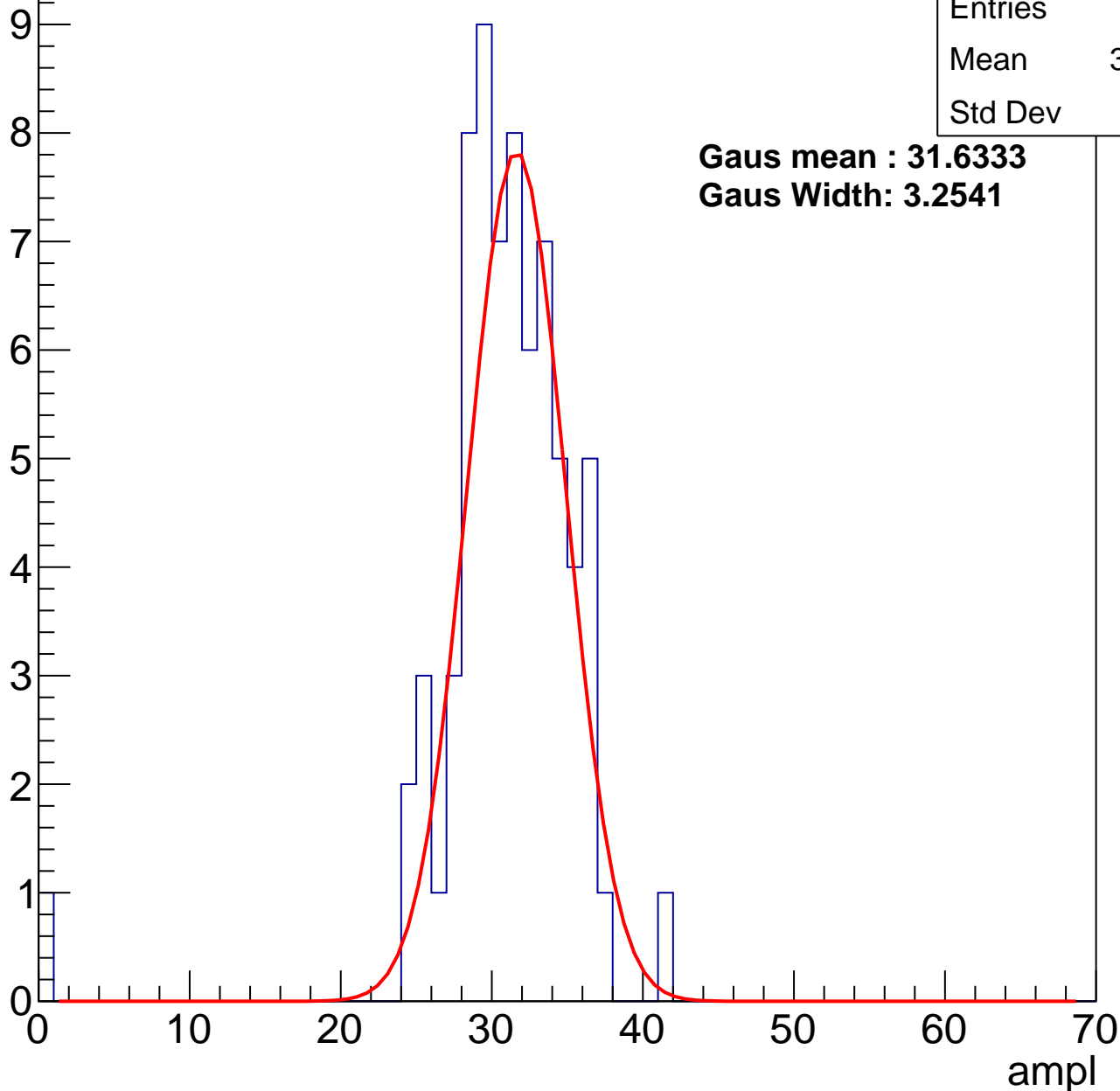
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	30.48
Std Dev	4.95

**Gaus mean : 31.6333**

**Gaus Width: 3.2541**



# B1L102S, U21-ch46, adc1

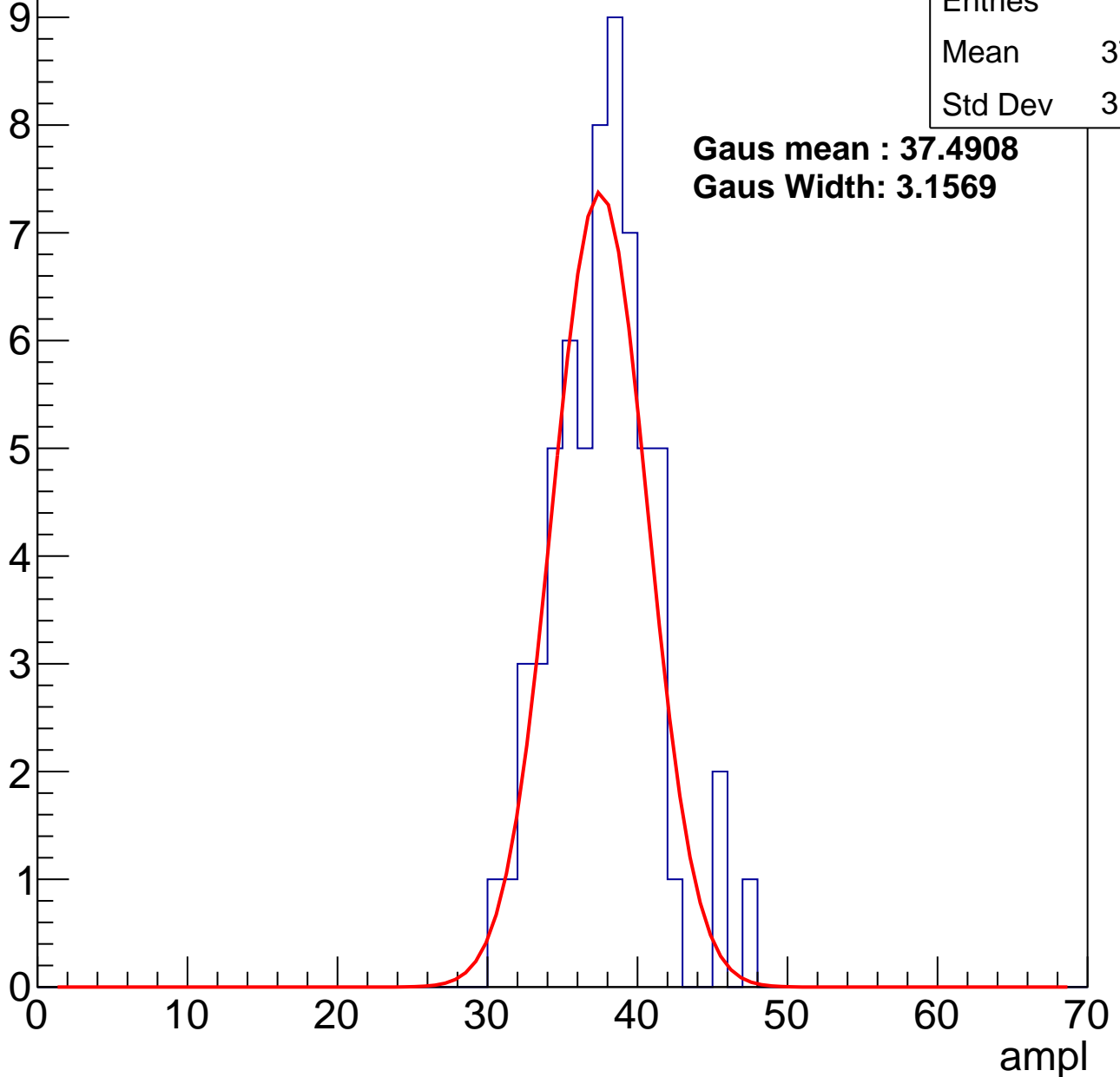
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	37.27
Std Dev	3.342

**Gaus mean : 37.4908**

**Gaus Width: 3.1569**



# B1L102S, U21-ch46, adc2

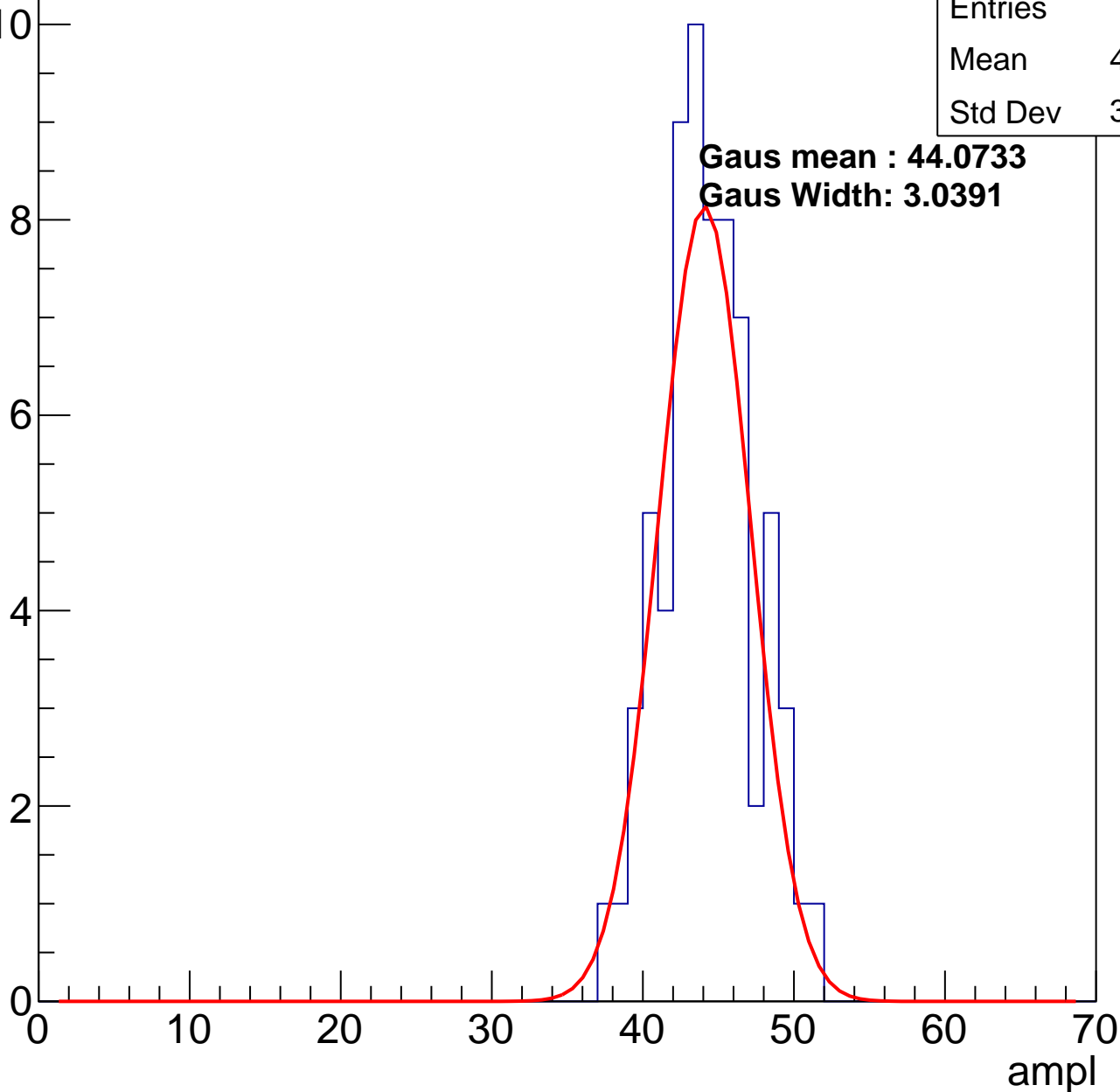
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	43.82
Std Dev	3.005

**Gaus mean : 44.0733**

**Gaus Width: 3.0391**

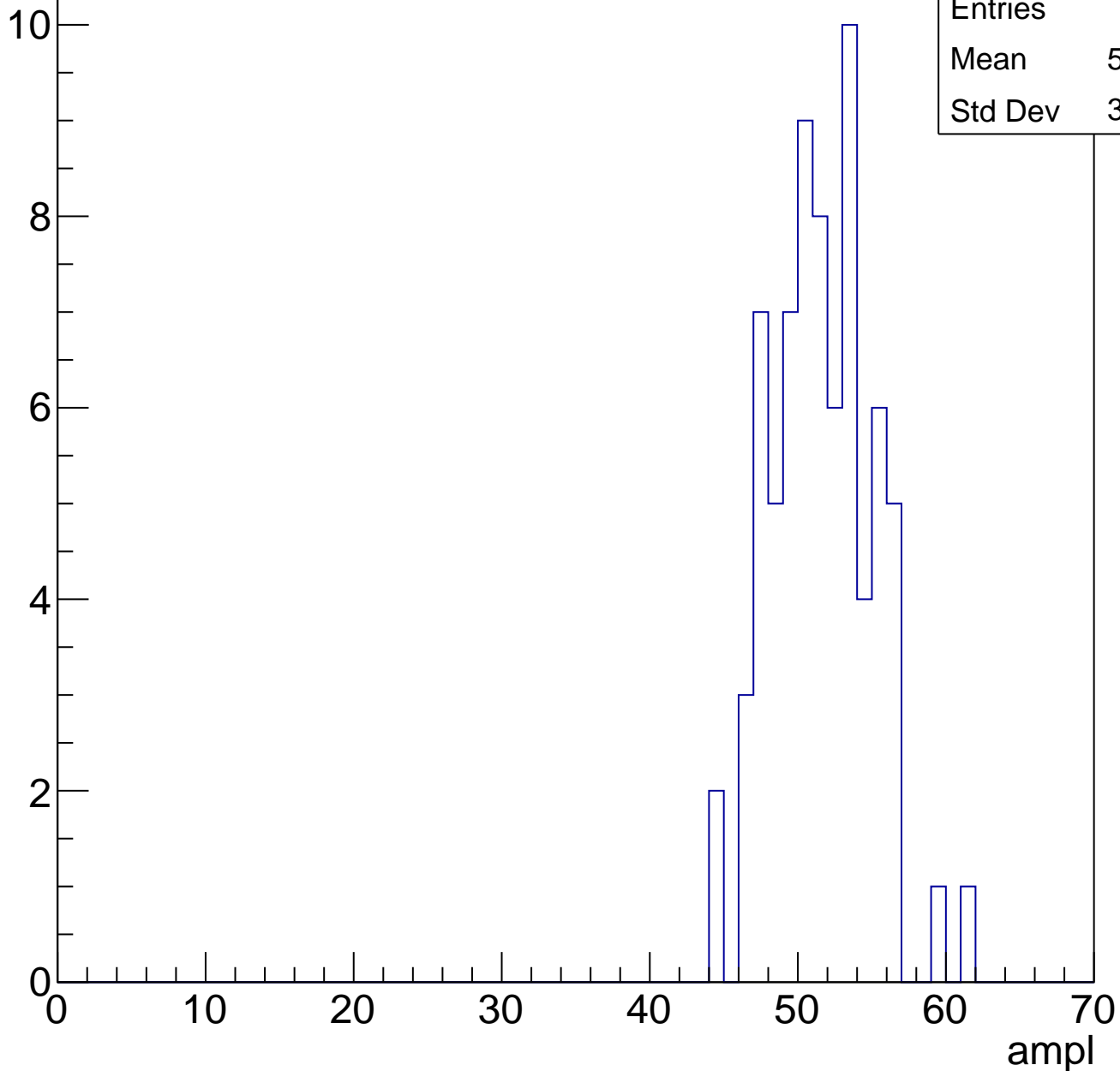


# B1L102S, U21-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	51.14
Std Dev	3.354

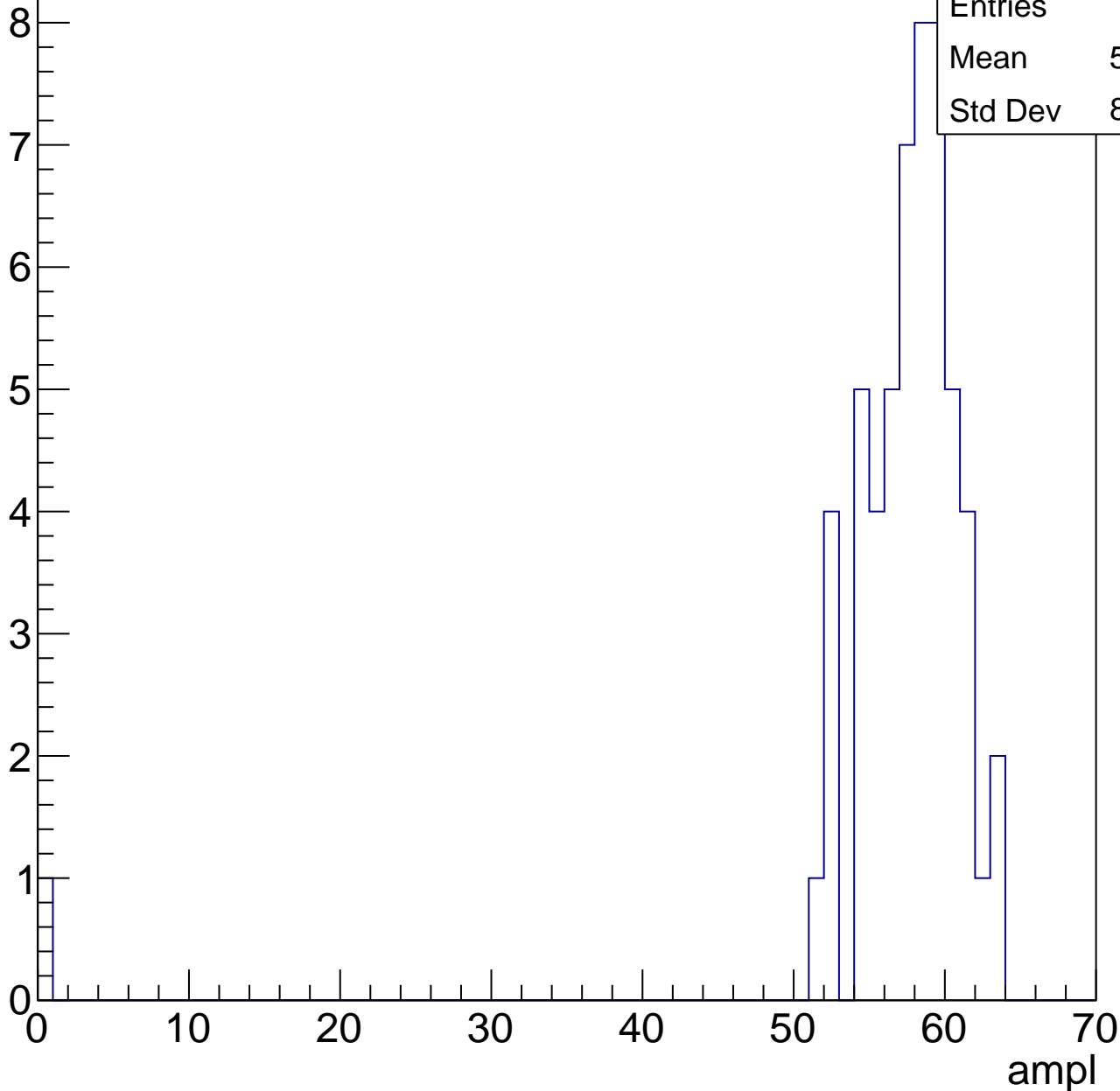


# B1L102S, U21-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	56.29
Std Dev	8.168

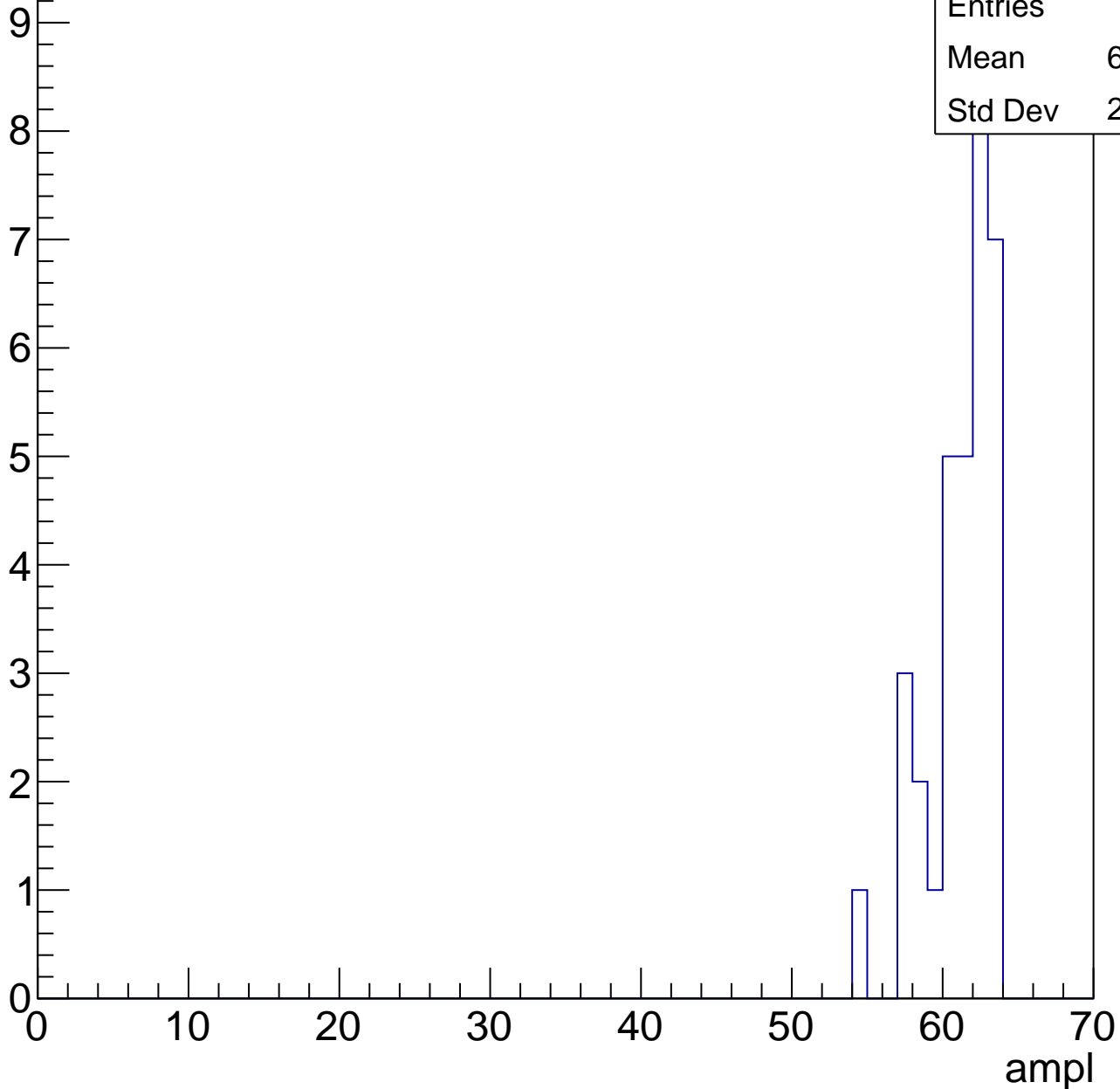


# B1L102S, U21-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	33
Mean	60.73
Std Dev	2.192



# B1L102S, U21-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

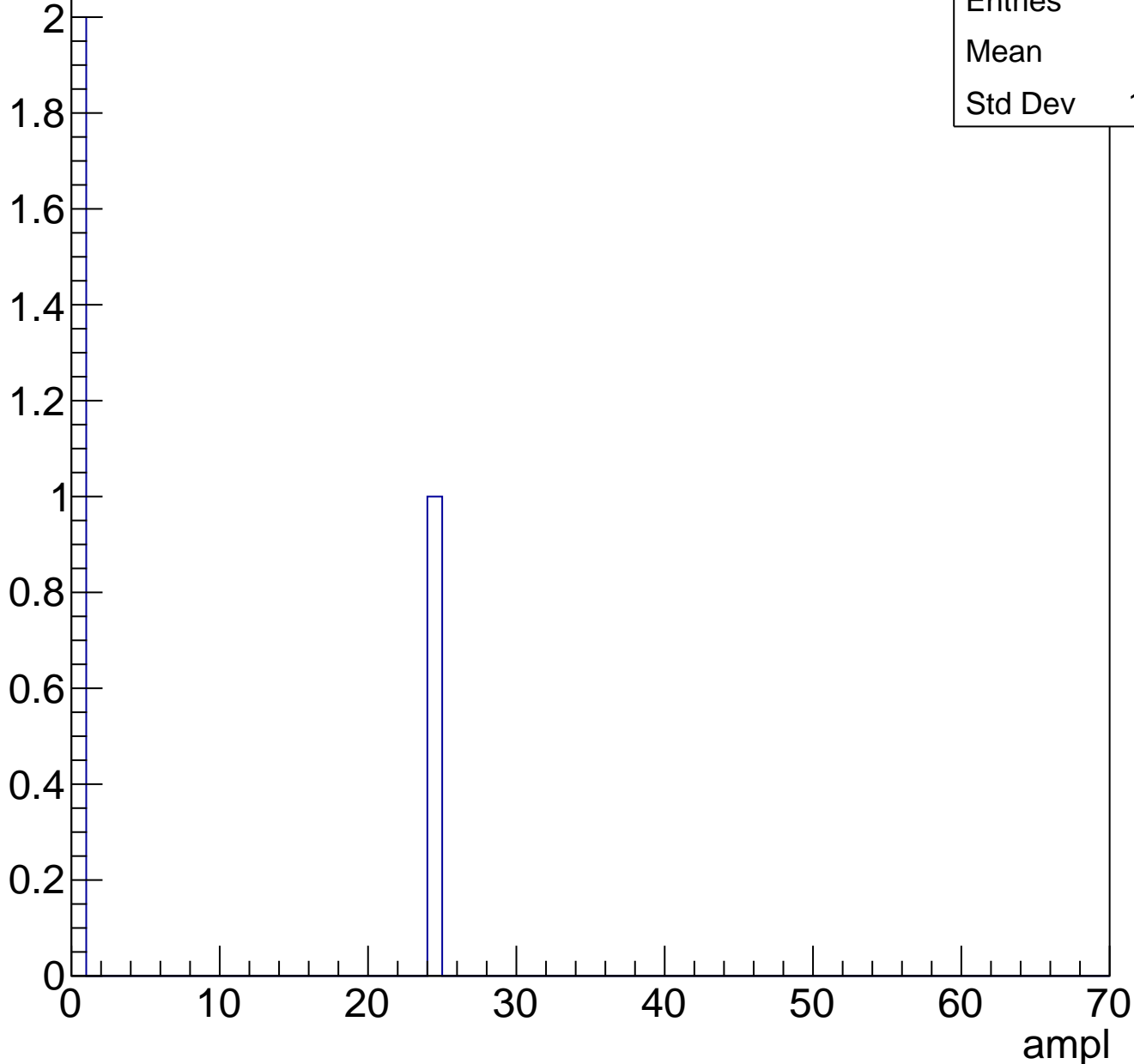




# B1L102S, U21-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch47, adc0

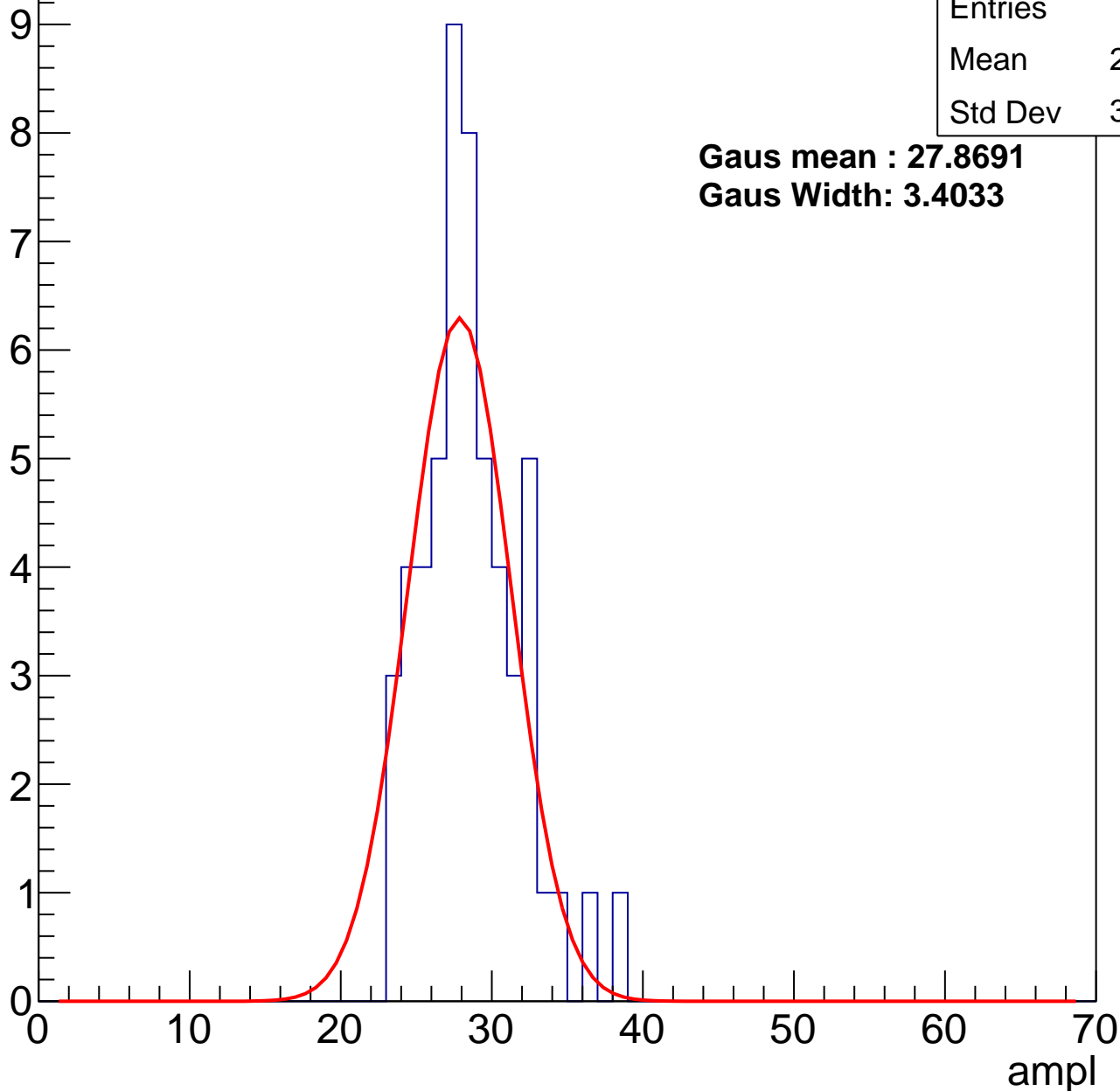
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	28.17
Std Dev	3.207

**Gaus mean : 27.8691**

**Gaus Width: 3.4033**



# B1L102S, U21-ch47, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	82
Mean	34.85
Std Dev	3.864

**Gaus mean : 34.6760**

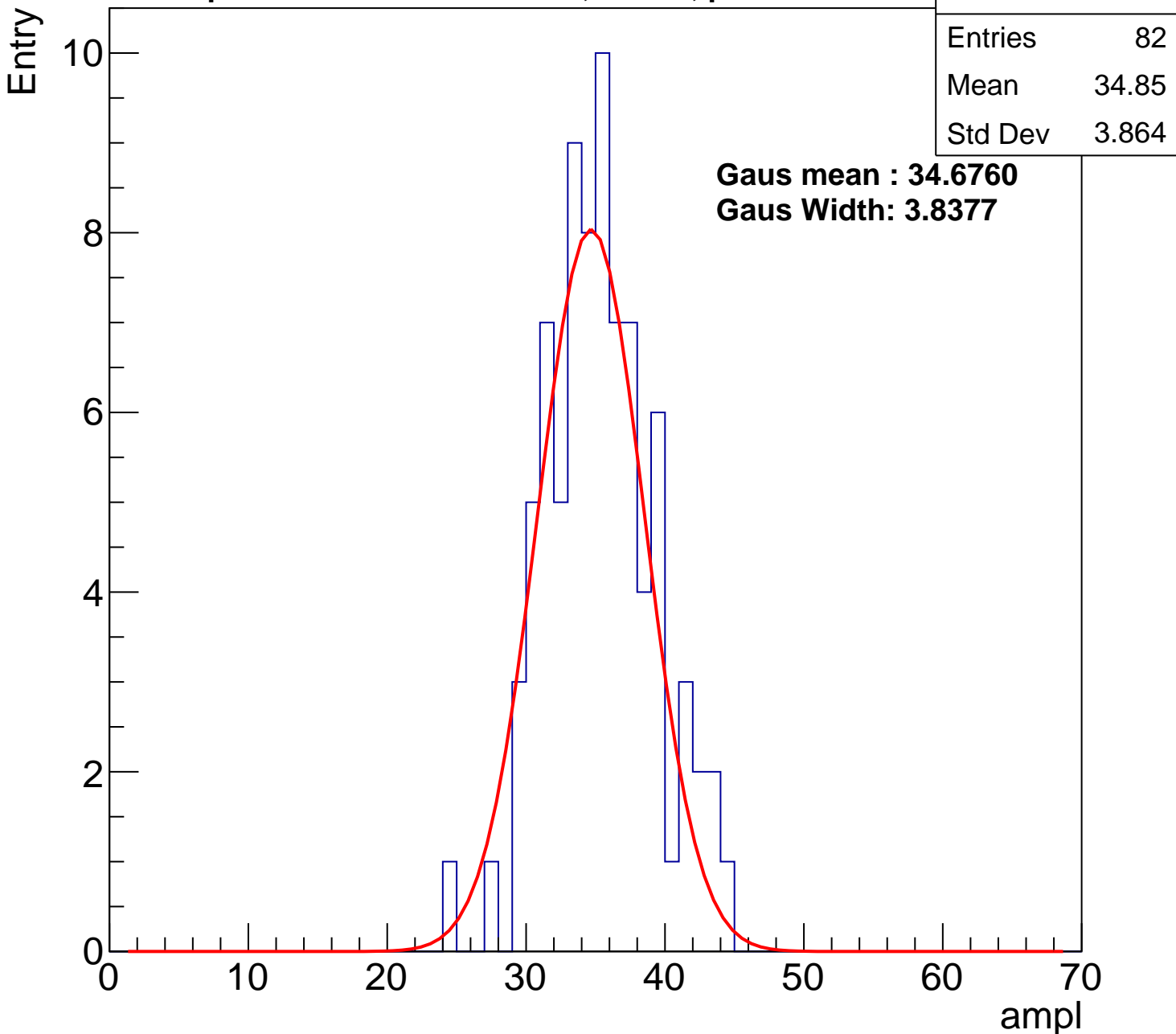
**Gaus Width: 3.8377**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U21-ch47, adc2

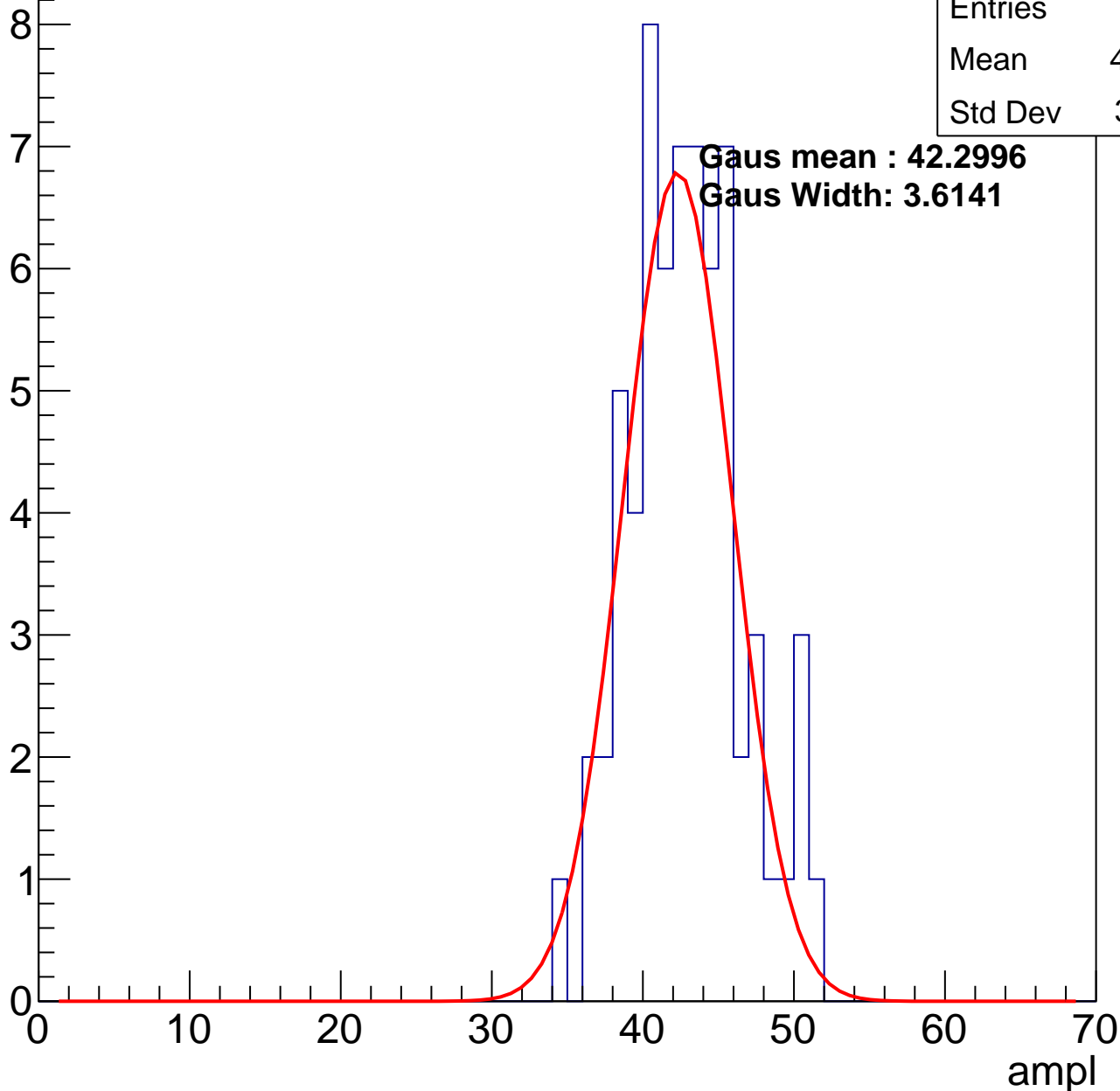
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	42.38
Std Dev	3.671

**Gaus mean : 42.2996**

**Gaus Width: 3.6141**

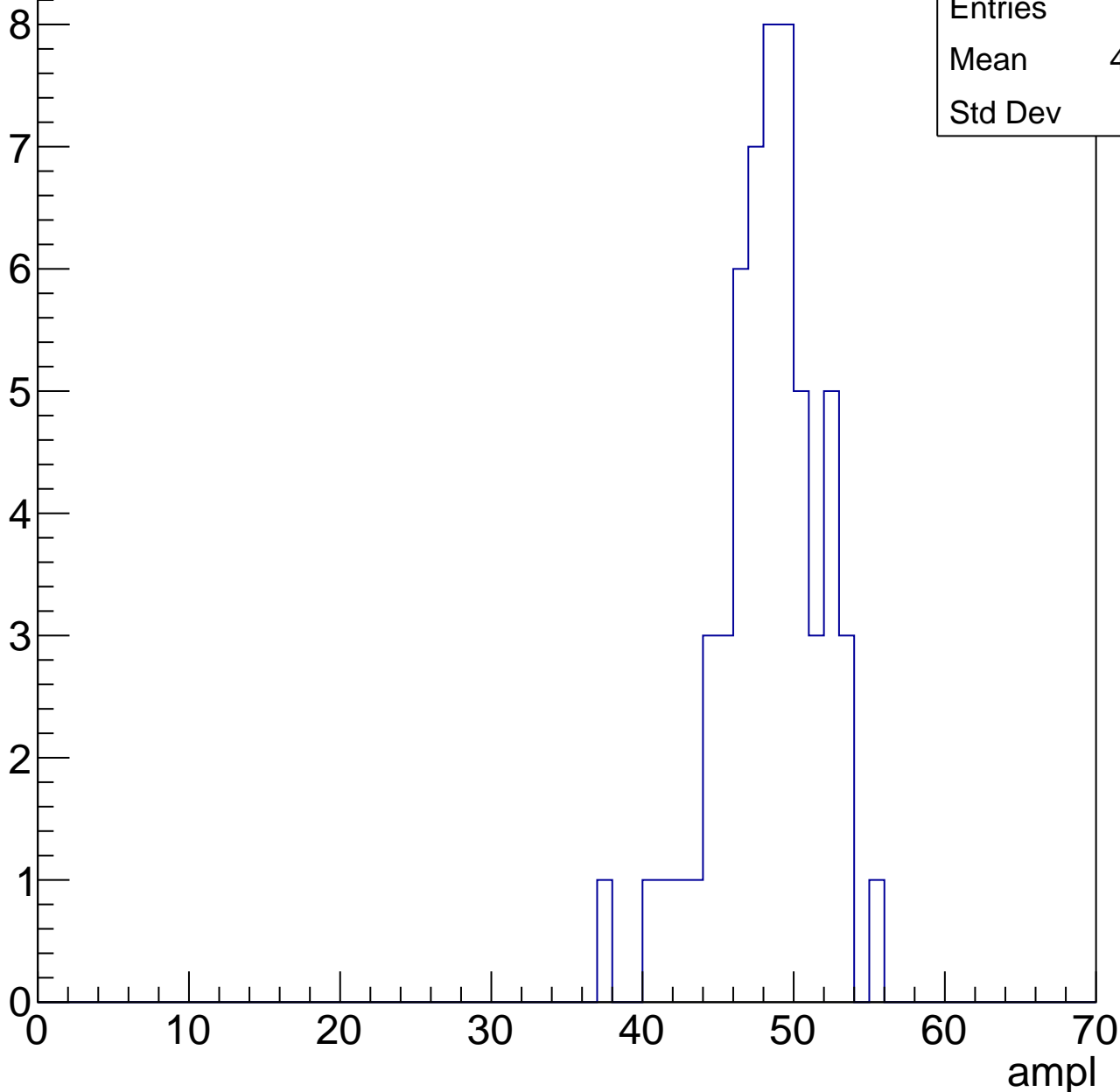


# B1L102S, U21-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	47.86
Std Dev	3.4

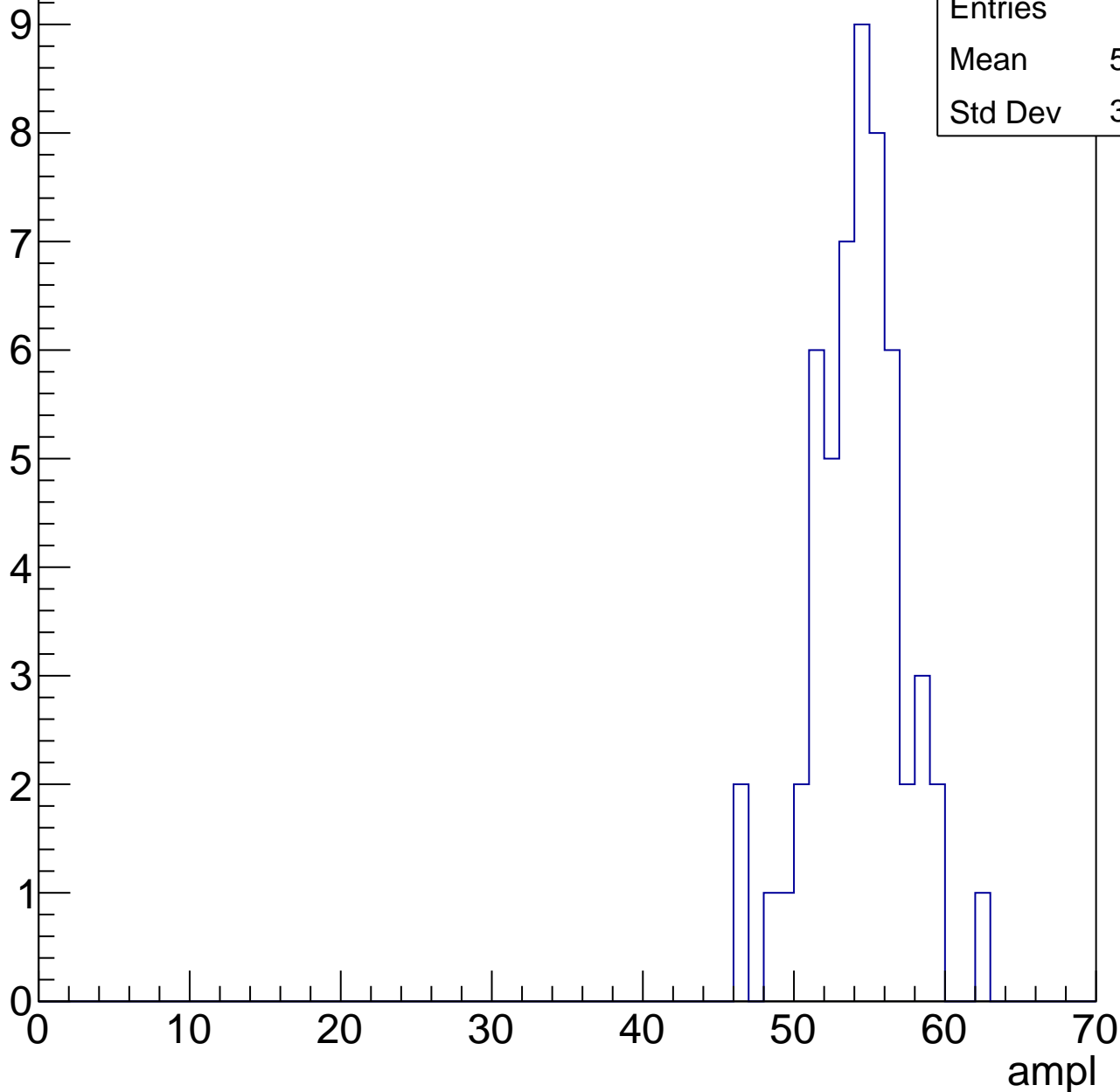


# B1L102S, U21-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

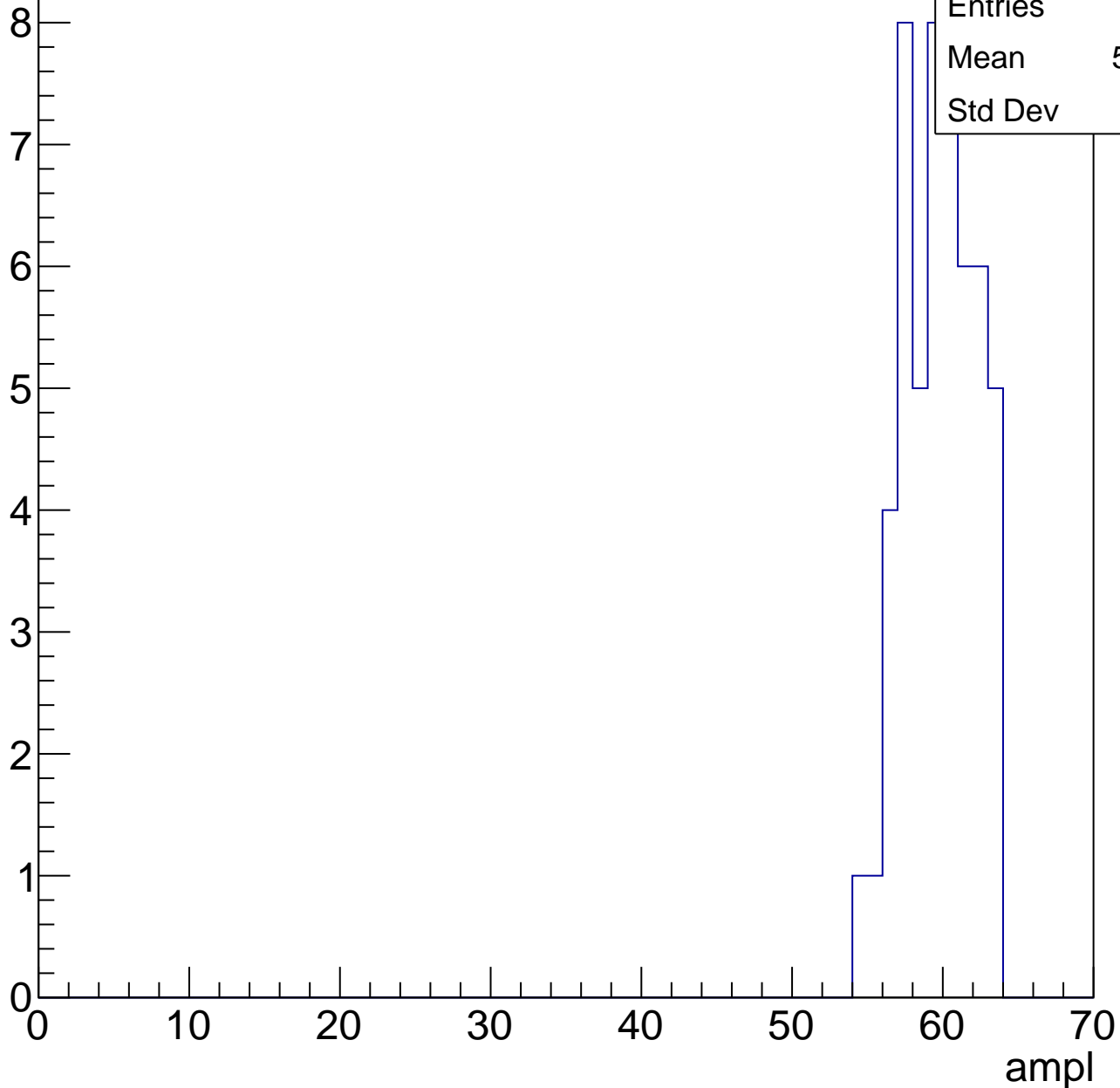
Entries	55
Mean	53.75
Std Dev	3.046



# B1L102S, U21-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

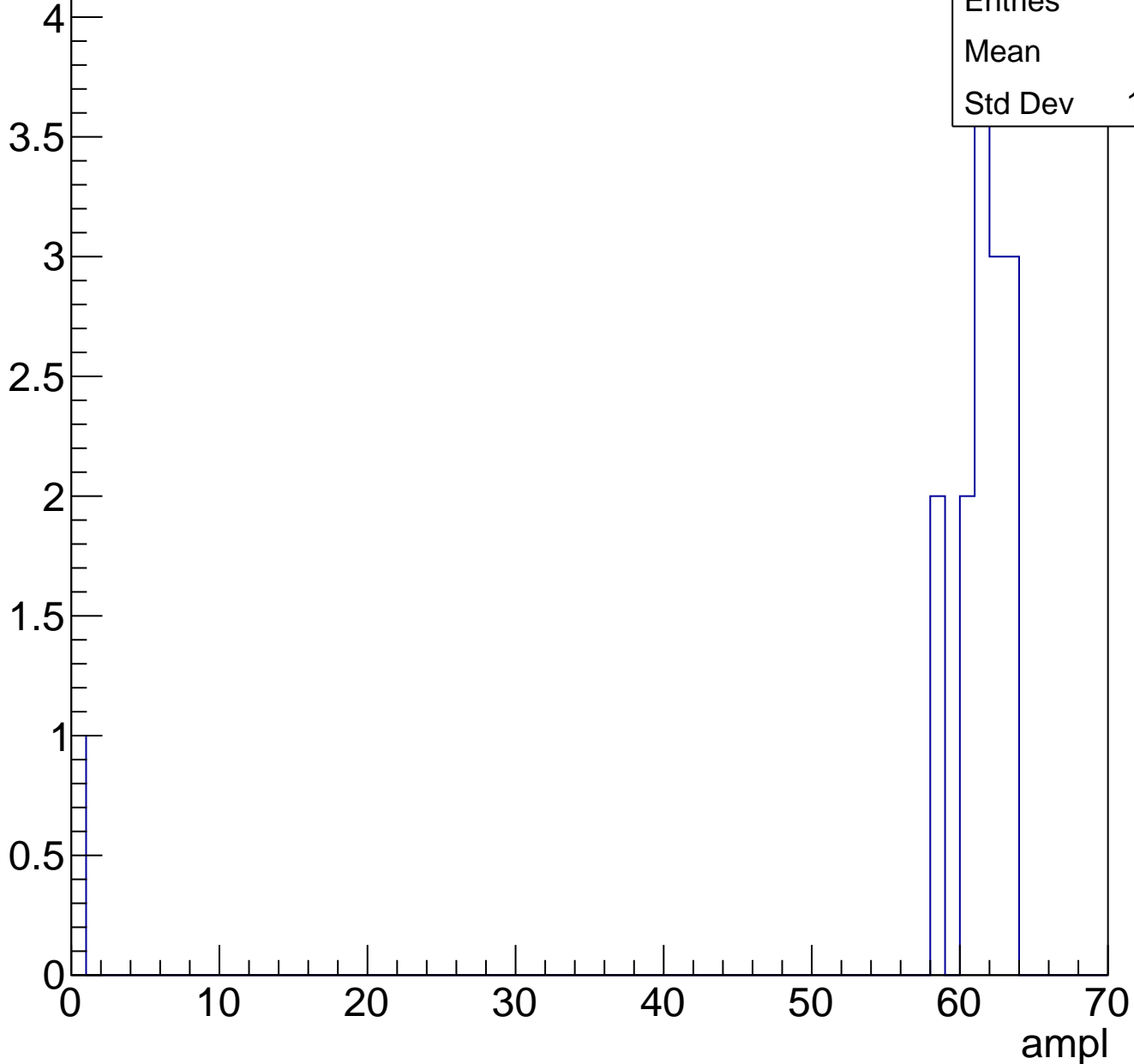


Entries	52
Mean	59.31
Std Dev	2.3

# B1L102S, U21-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	49.67
Std Dev	18.86

0 10 20 30 40 50 60 70

ampl

B1L102S, U21-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	49.67
Std Dev	18.86

0 10 20 30 40 50 60 70

ampl

# B1L102S, U21-ch48, adc0

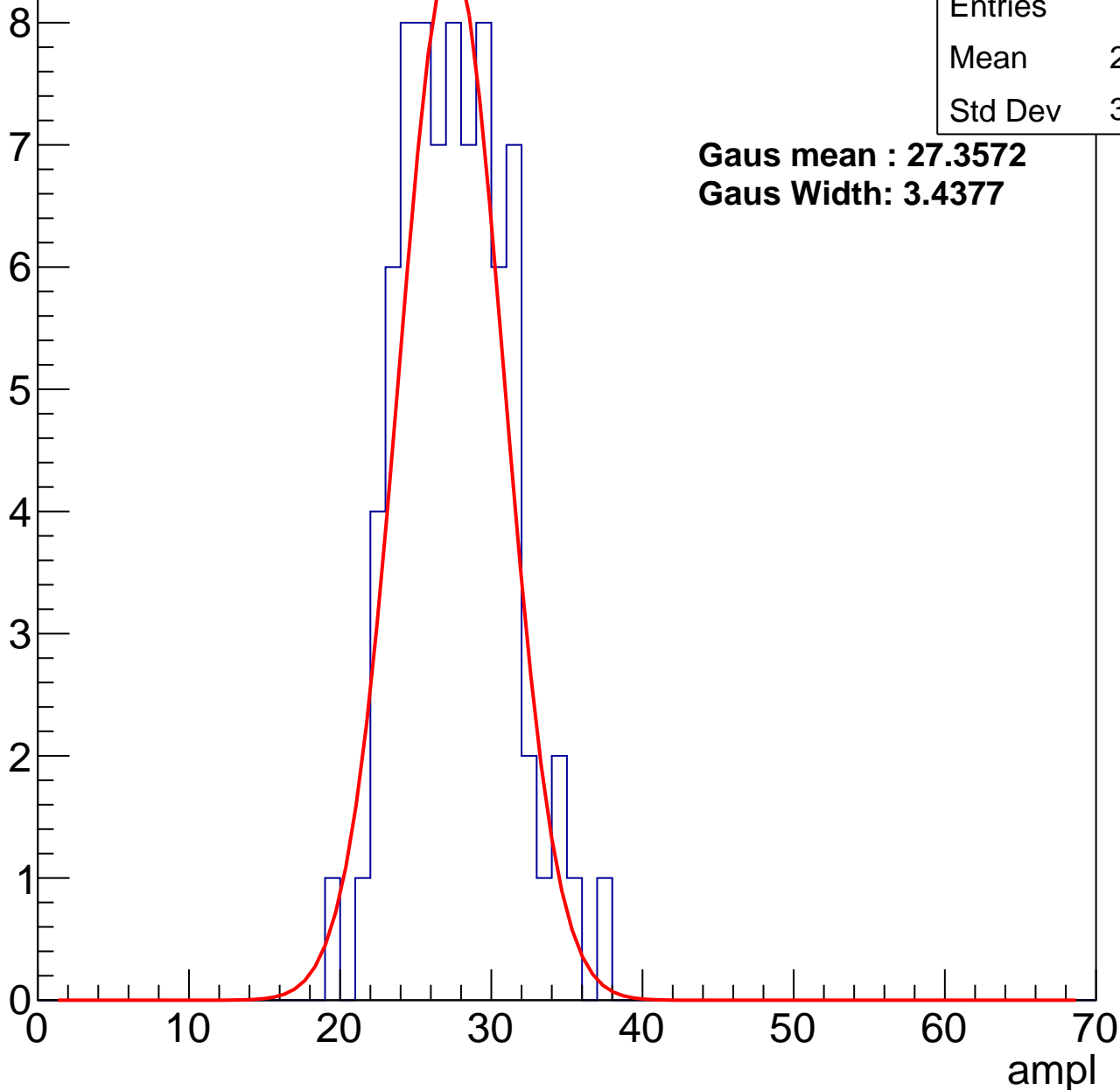
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	27.15
Std Dev	3.505

**Gaus mean : 27.3572**

**Gaus Width: 3.4377**



# B1L102S, U21-ch48, adc1

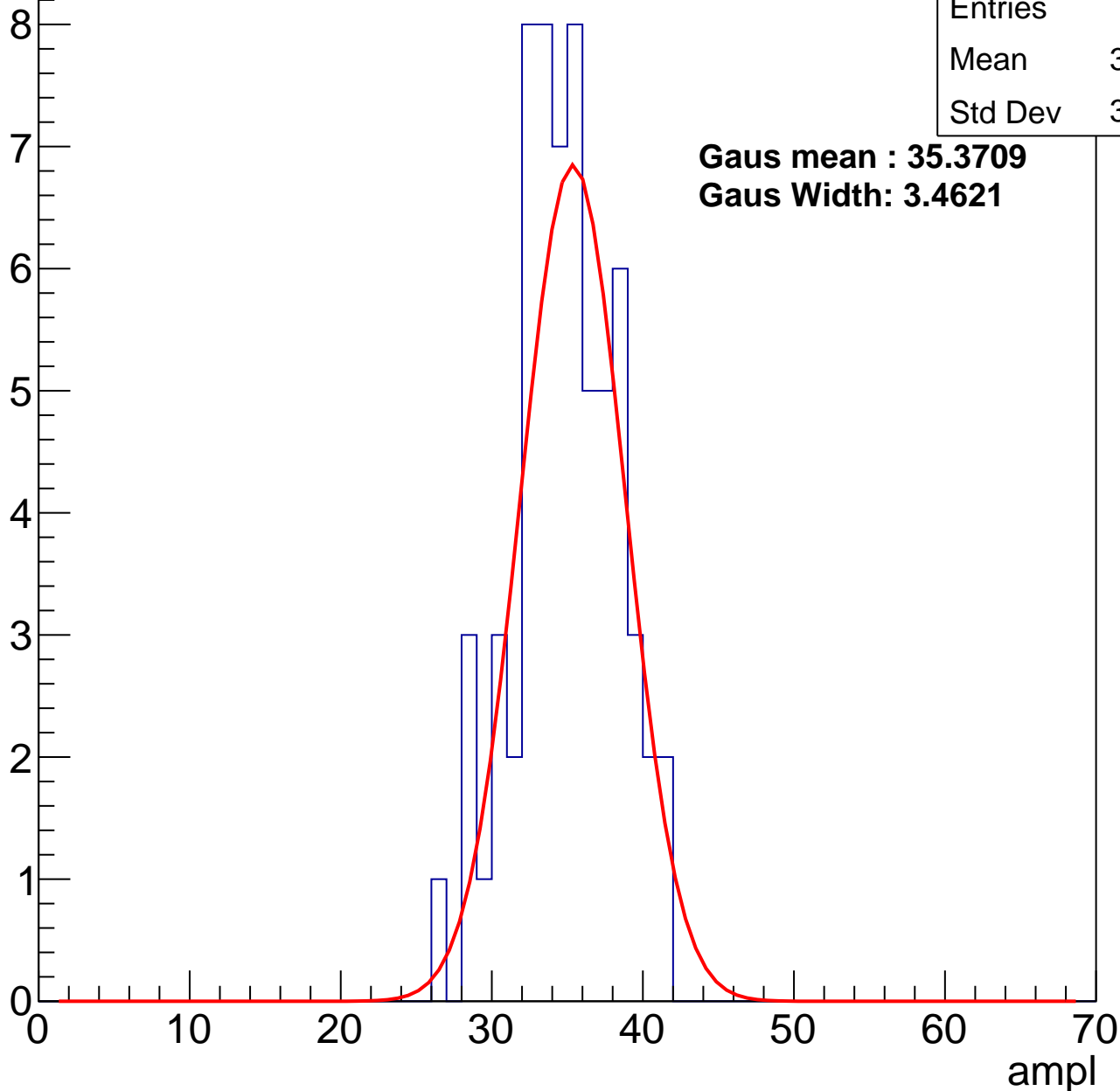
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	34.39
Std Dev	3.324

**Gaus mean : 35.3709**

**Gaus Width: 3.4621**



# B1L102S, U21-ch48, adc2

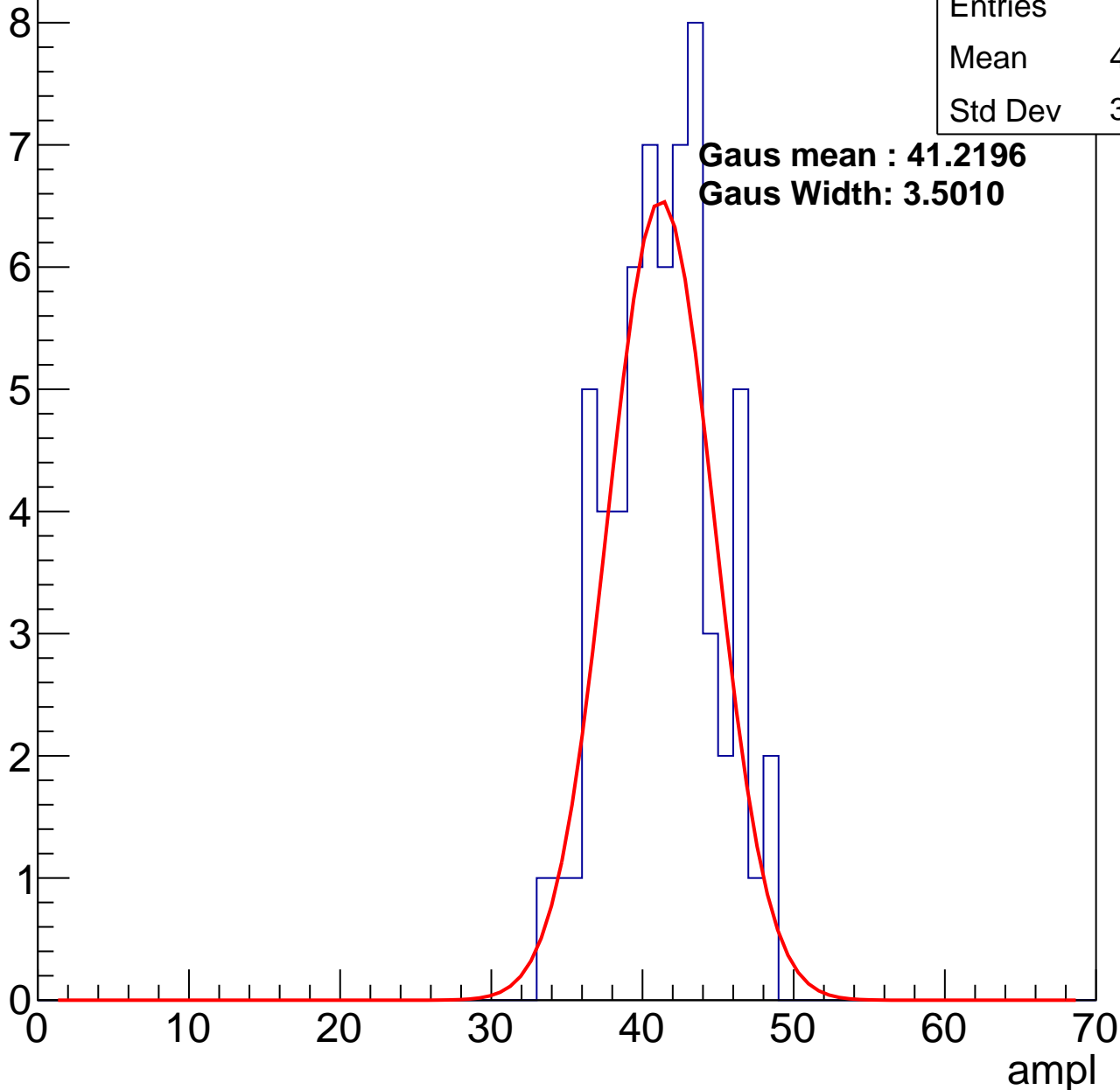
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	40.87
Std Dev	3.476

**Gaus mean : 41.2196**

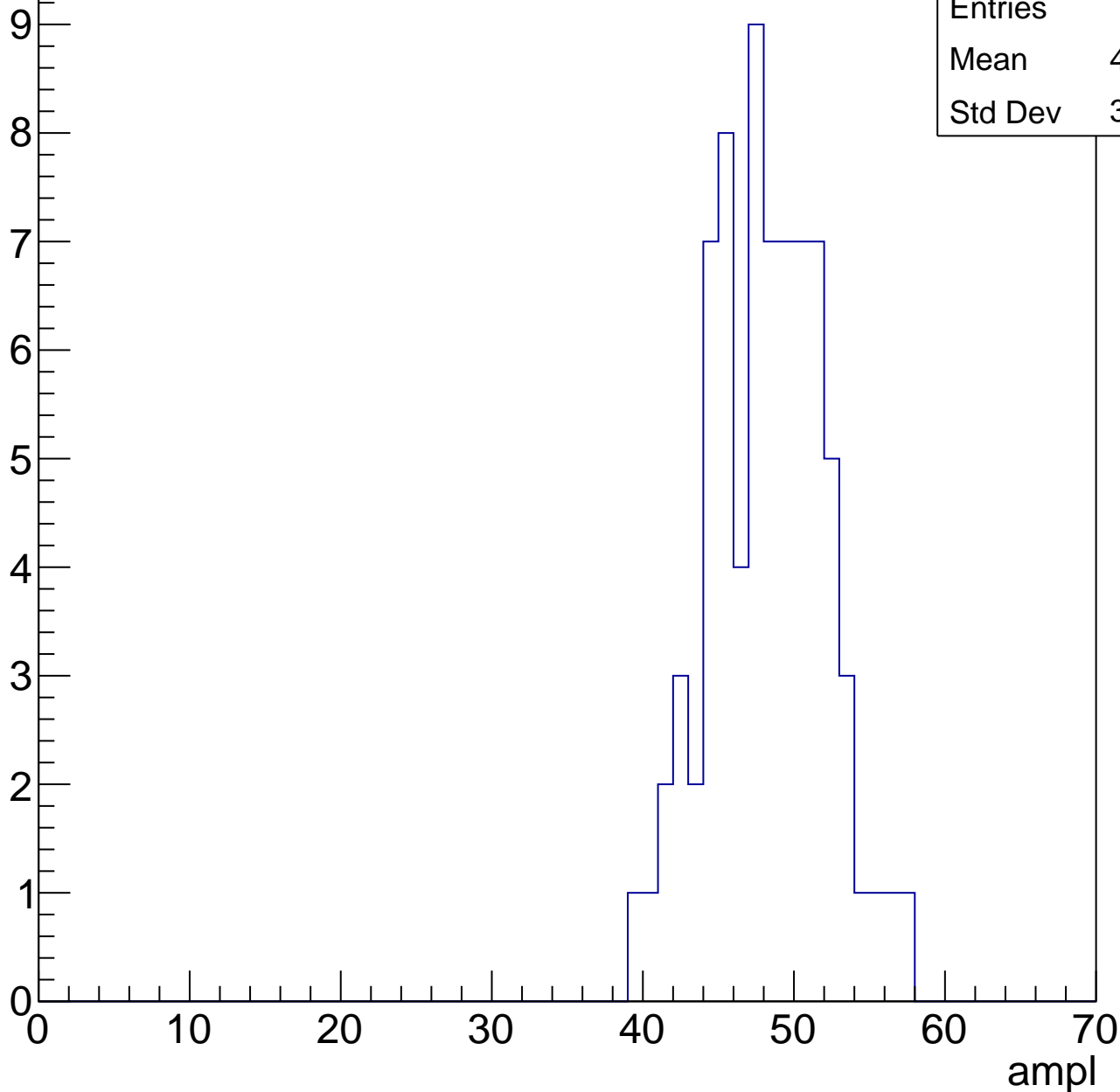
**Gaus Width: 3.5010**



# B1L102S, U21-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

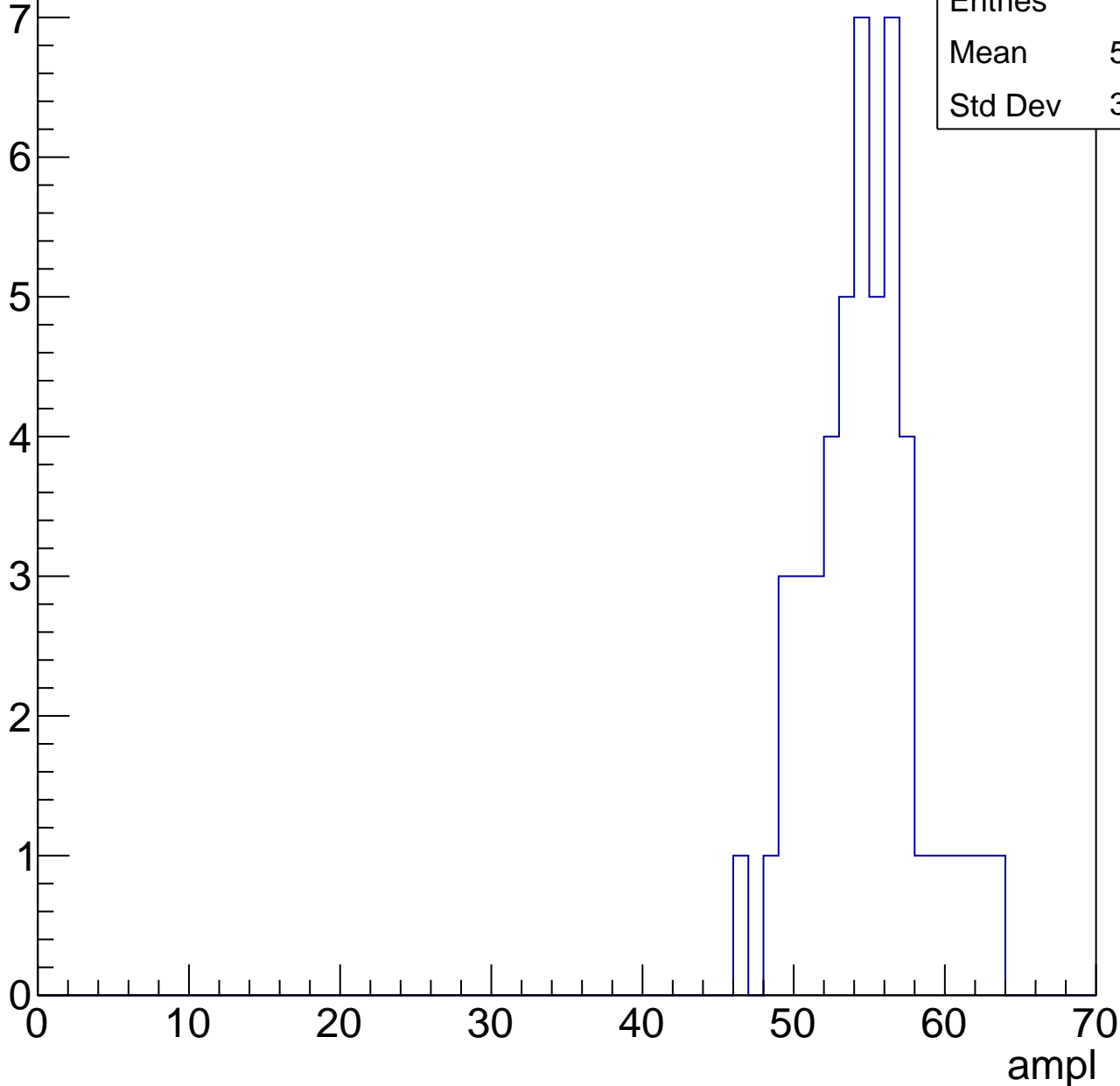


# B1L102S, U21-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

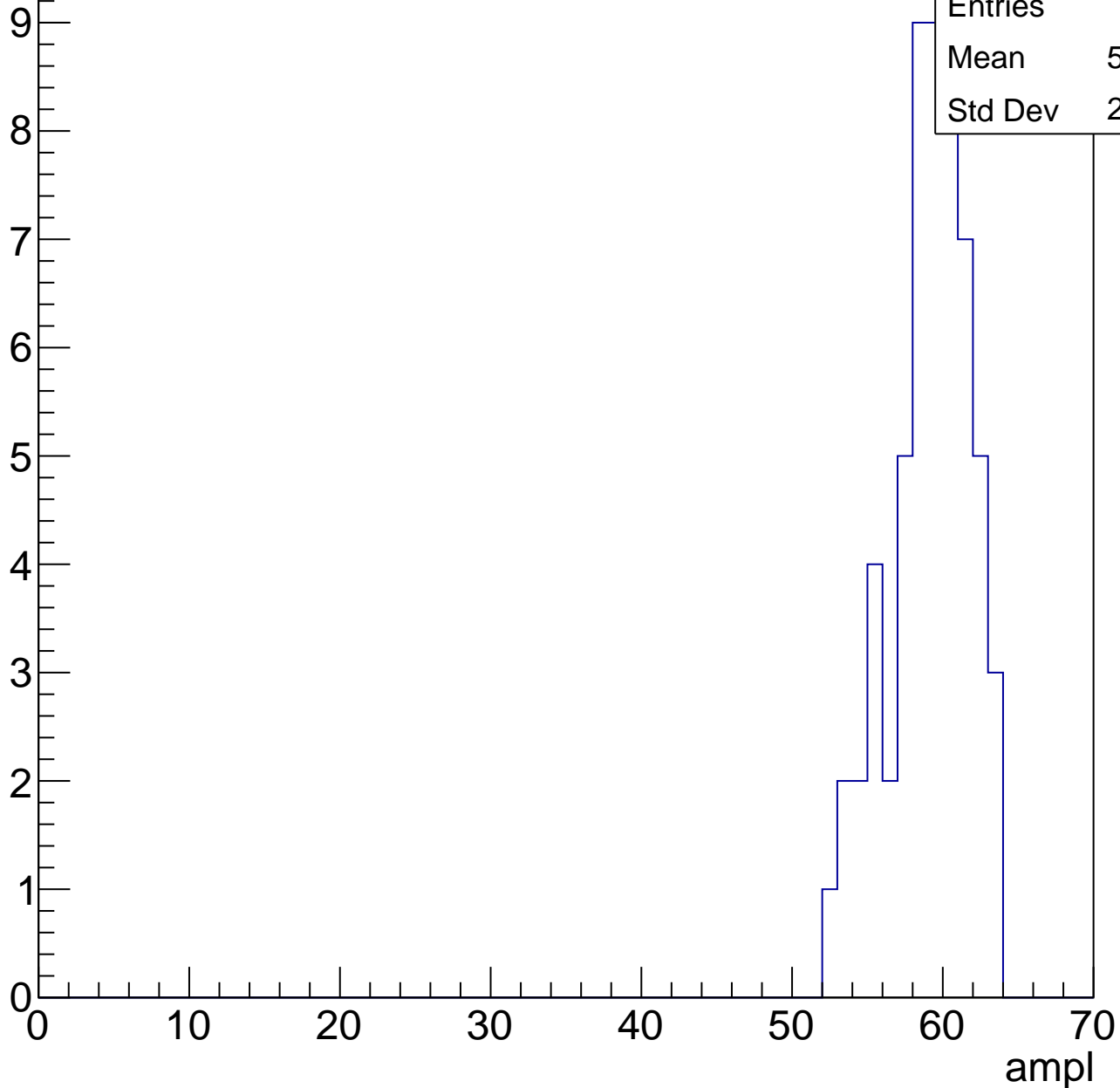
Entries	49
Mean	54.14
Std Dev	3.528



# B1L102S, U21-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

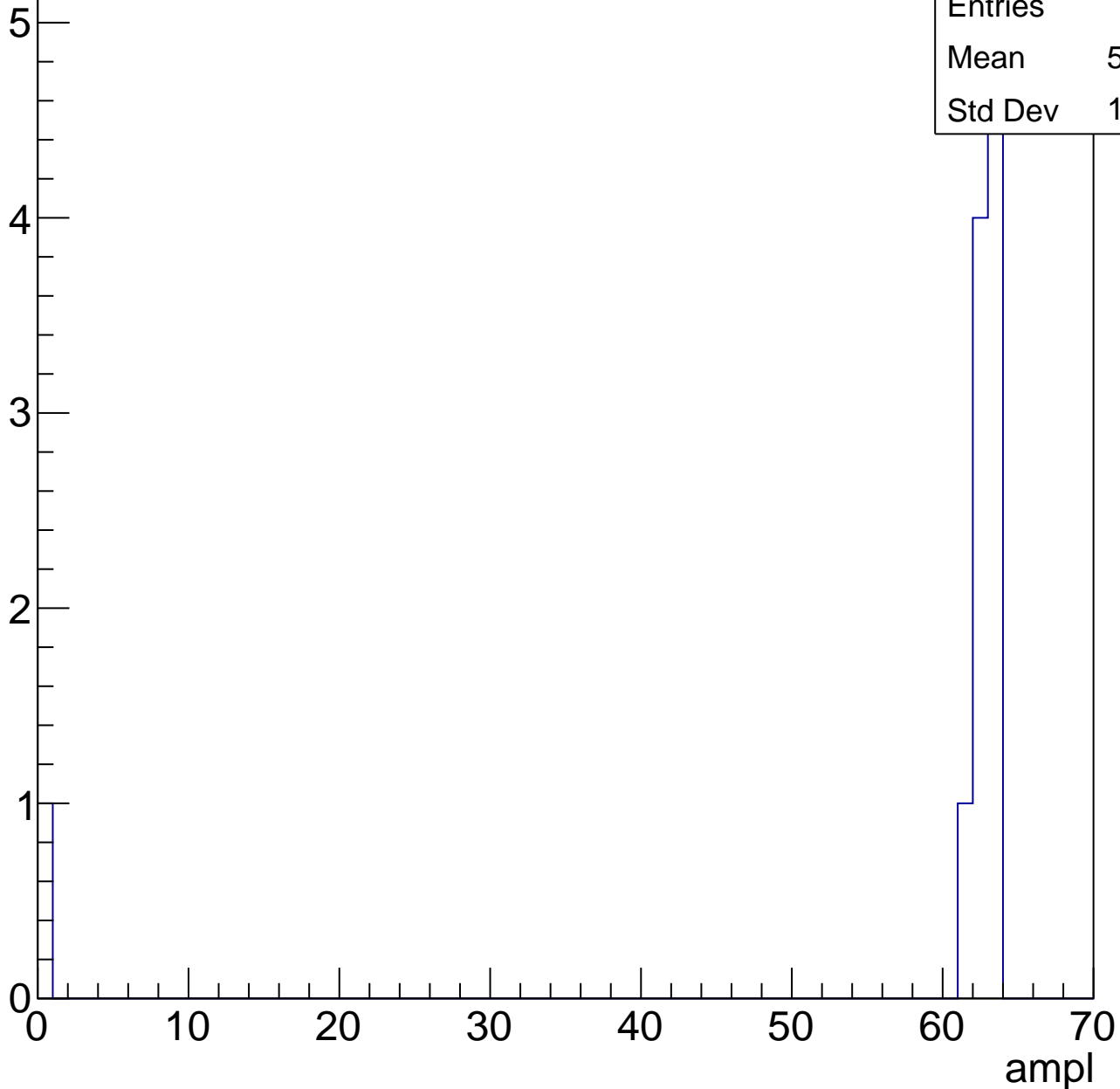


# B1L102S, U21-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	11
Mean	56.73
Std Dev	17.95

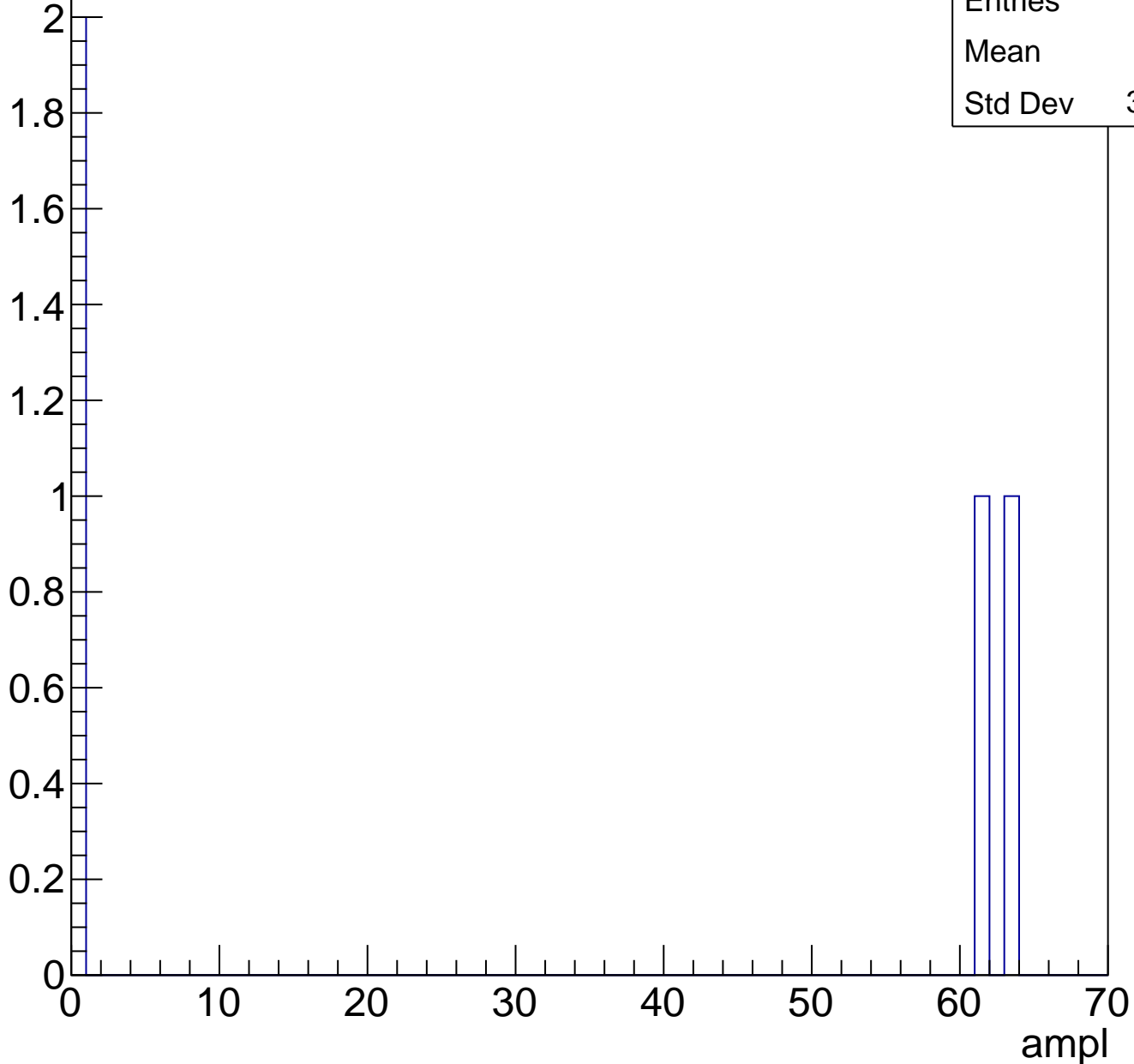




# B1L102S, U21-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch49, adc0

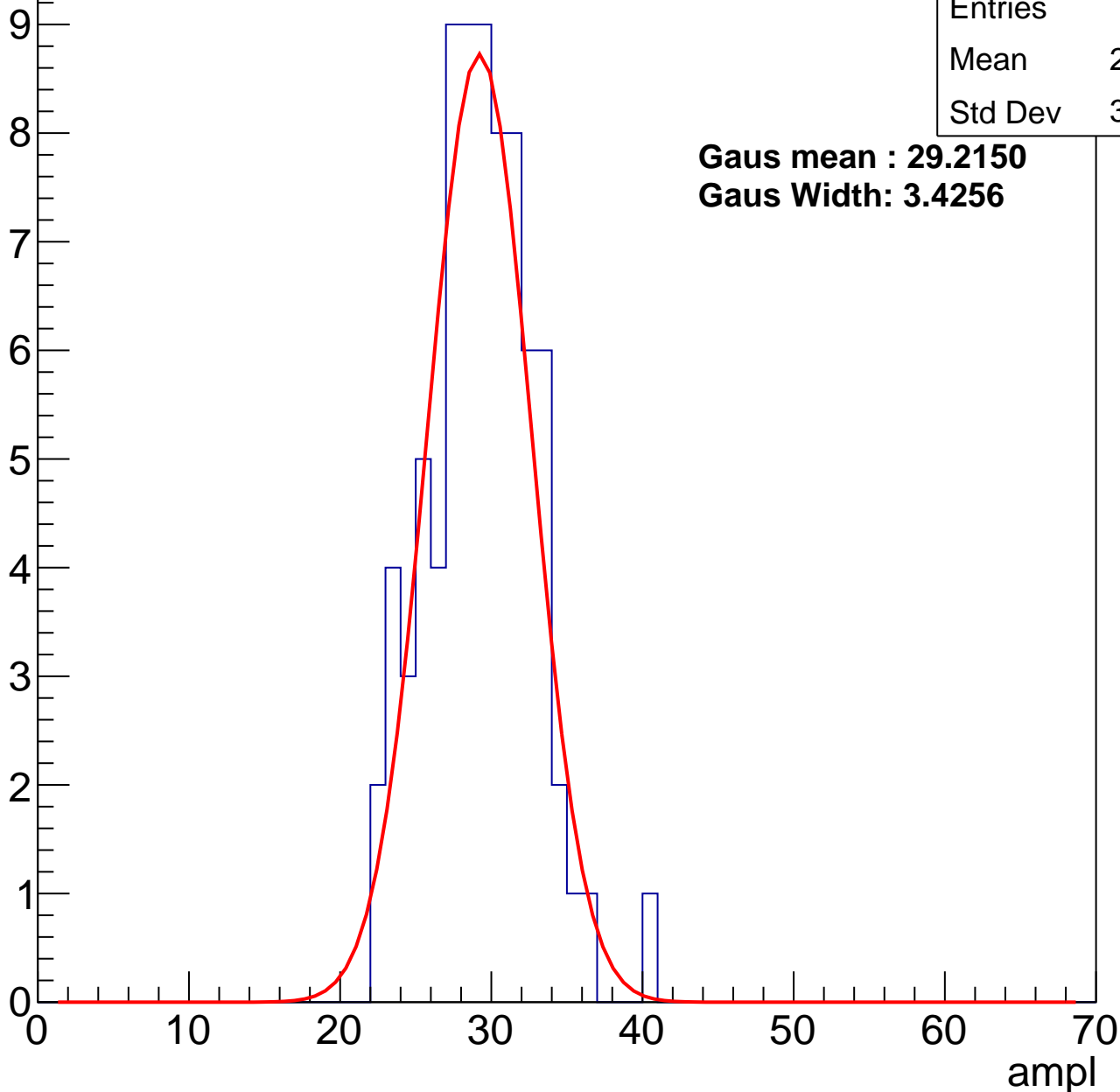
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	28.85
Std Dev	3.438

**Gaus mean : 29.2150**

**Gaus Width: 3.4256**



# B1L102S, U21-ch49, adc1

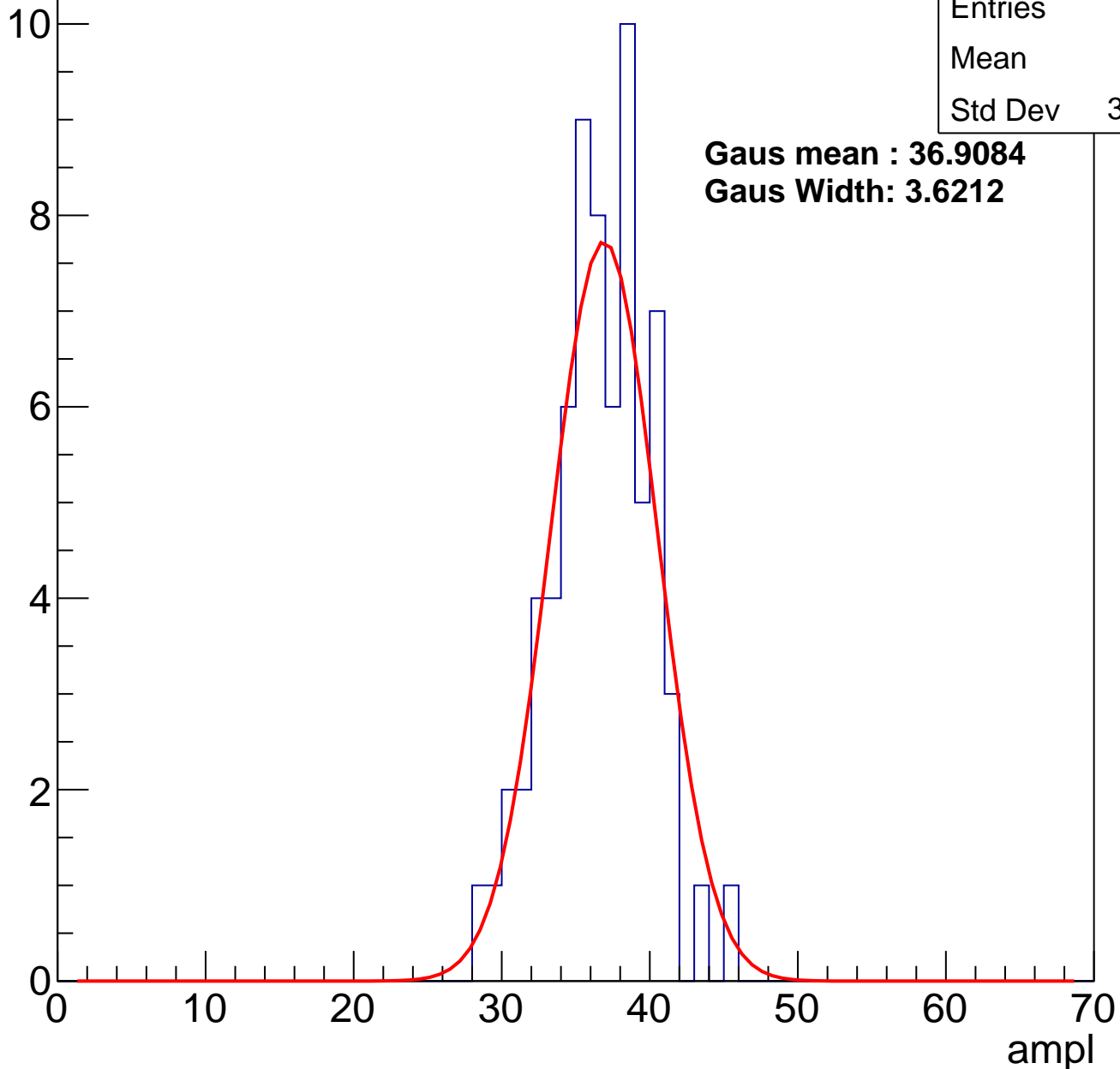
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	70
Mean	36.2
Std Dev	3.324

**Gaus mean : 36.9084**

**Gaus Width: 3.6212**

Entry



# B1L102S, U21-ch49, adc2

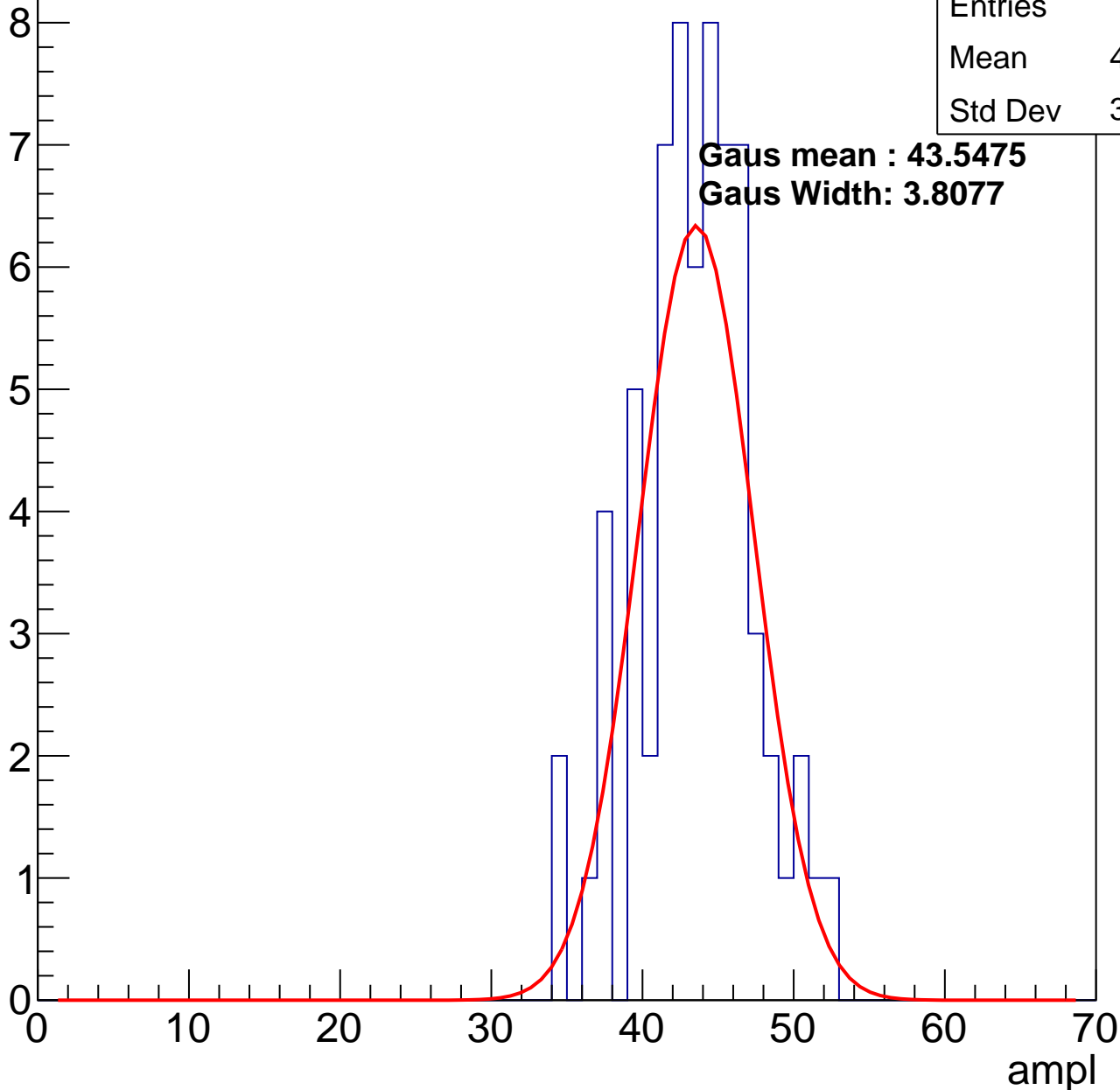
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	43.07
Std Dev	3.794

**Gaus mean : 43.5475**

**Gaus Width: 3.8077**

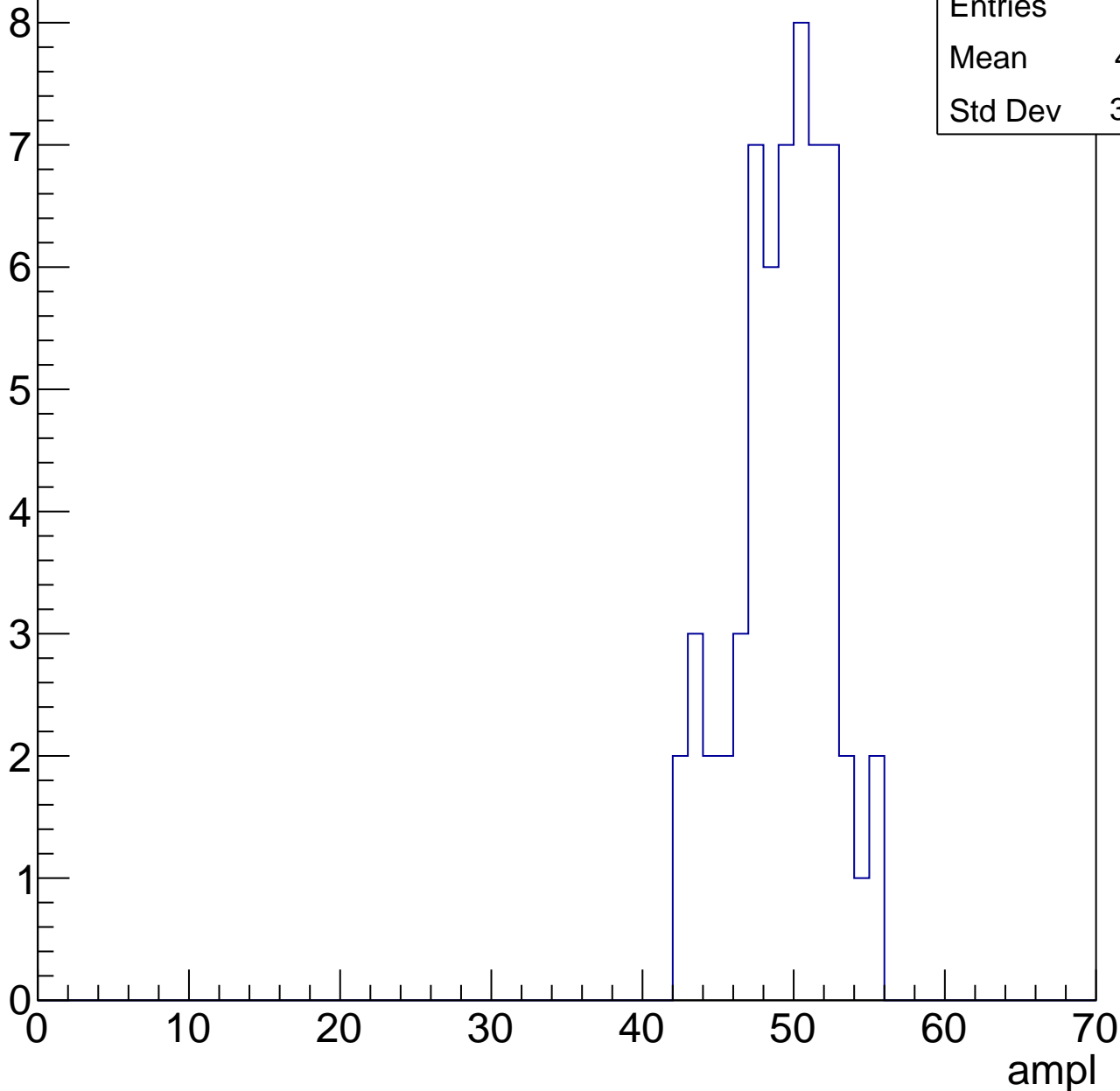


# B1L102S, U21-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

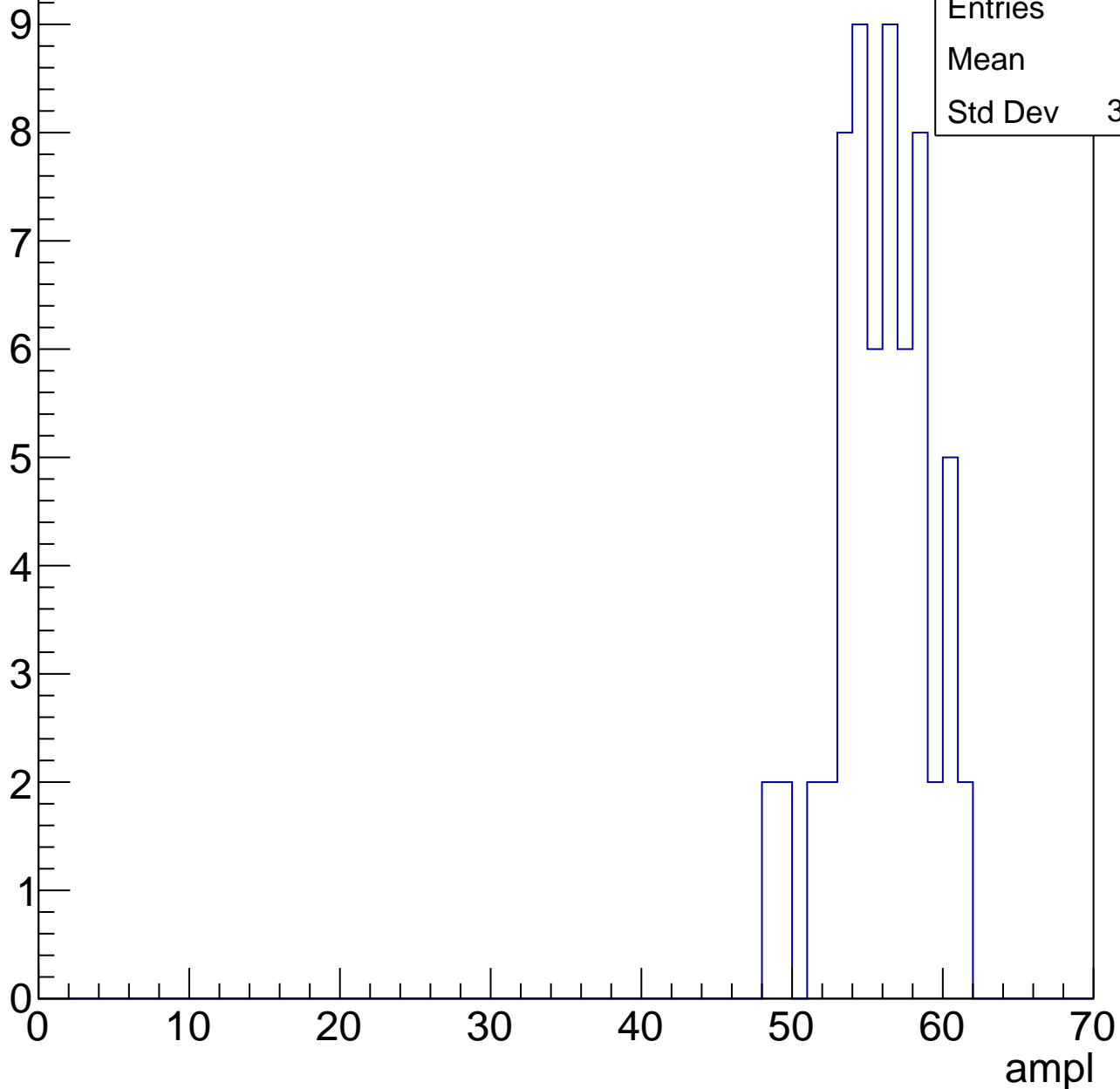
Entries	59
Mean	48.81
Std Dev	3.122



# B1L102S, U21-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	49
Mean	60.43
Std Dev	2.241

Entry

10

8

6

4

2

0

0

10

20

30

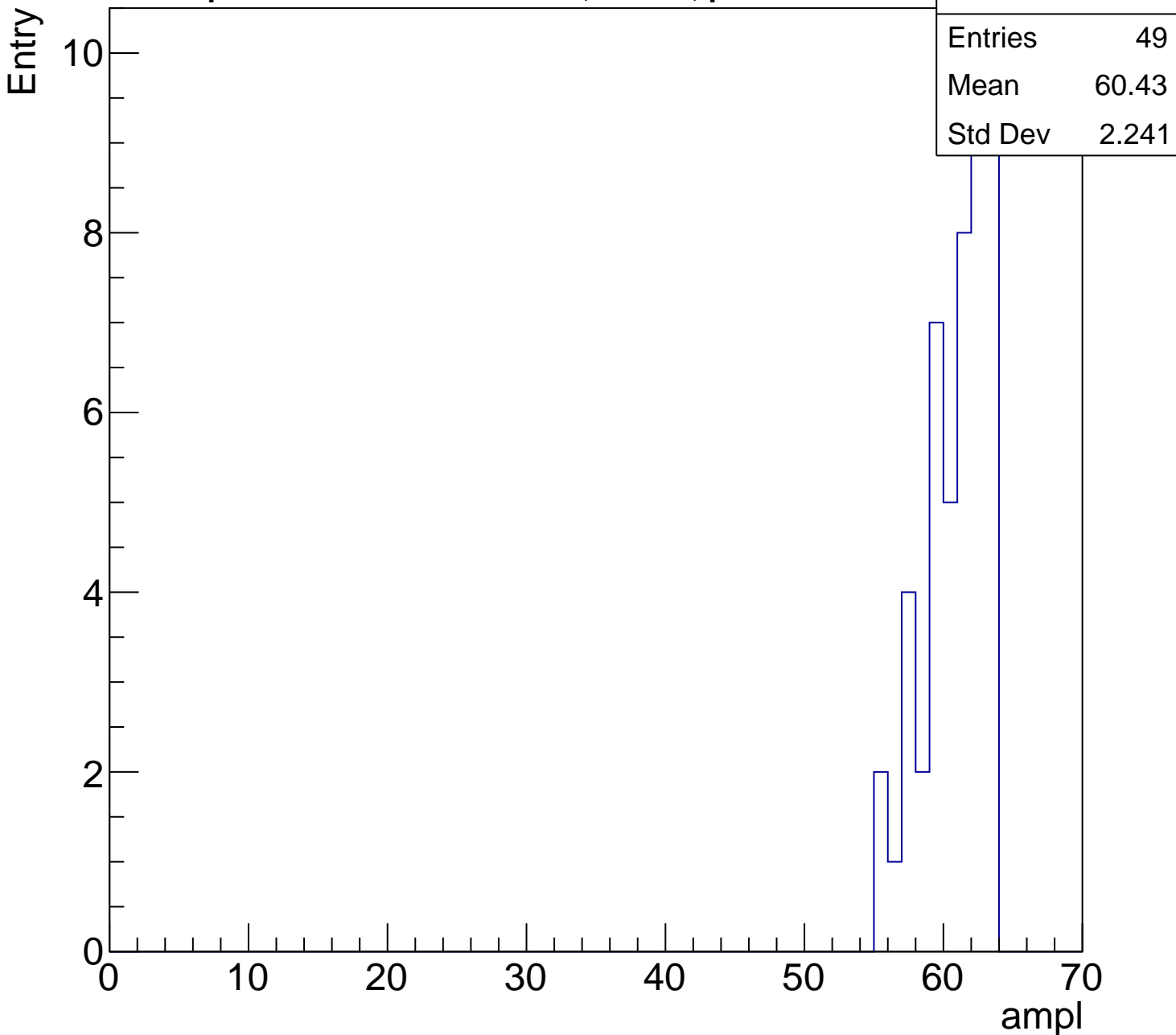
40

50

60

ampl

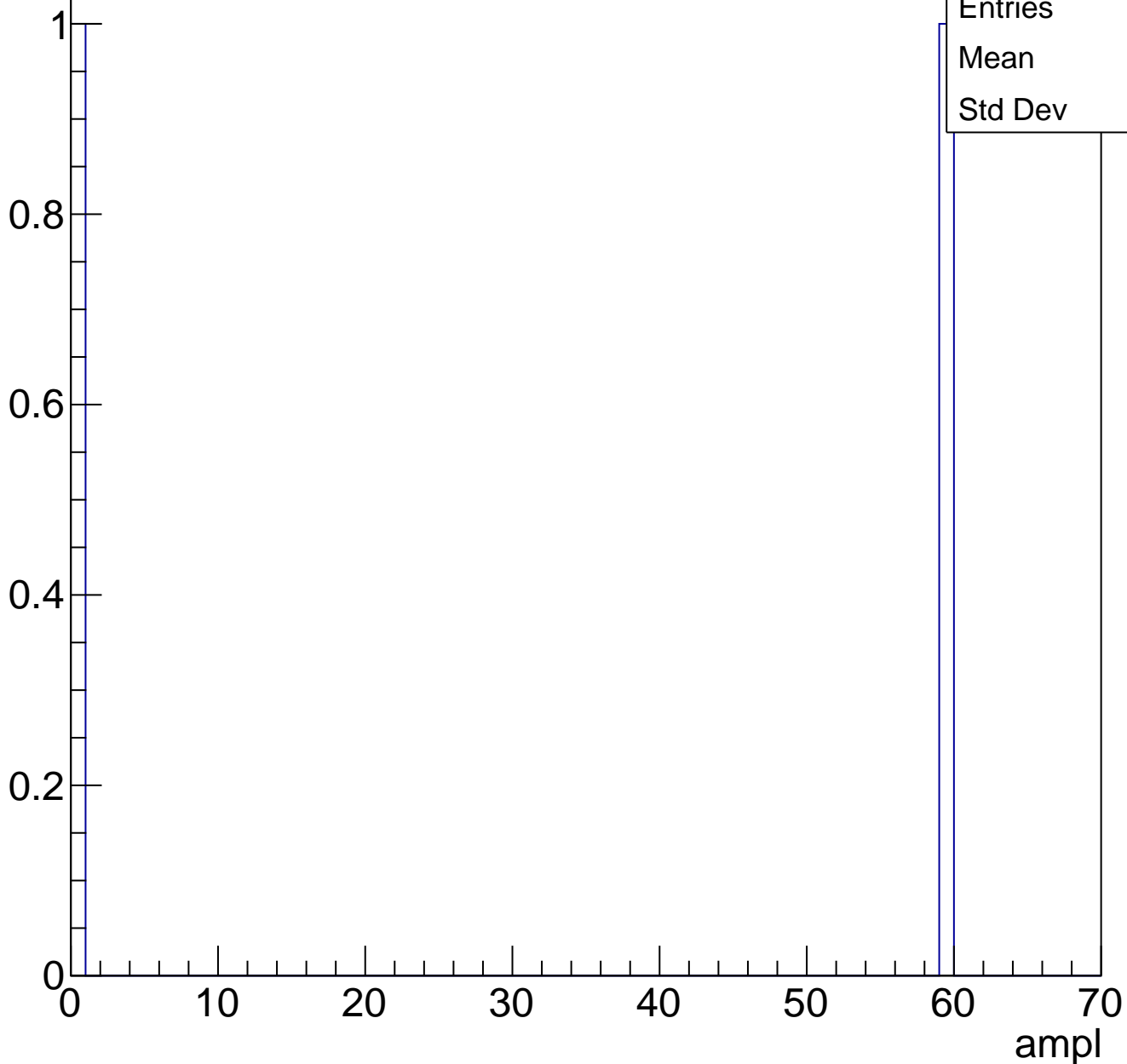
70



# B1L102S, U21-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	11
Std Dev	11

# B1L102S, U21-ch50, adc0

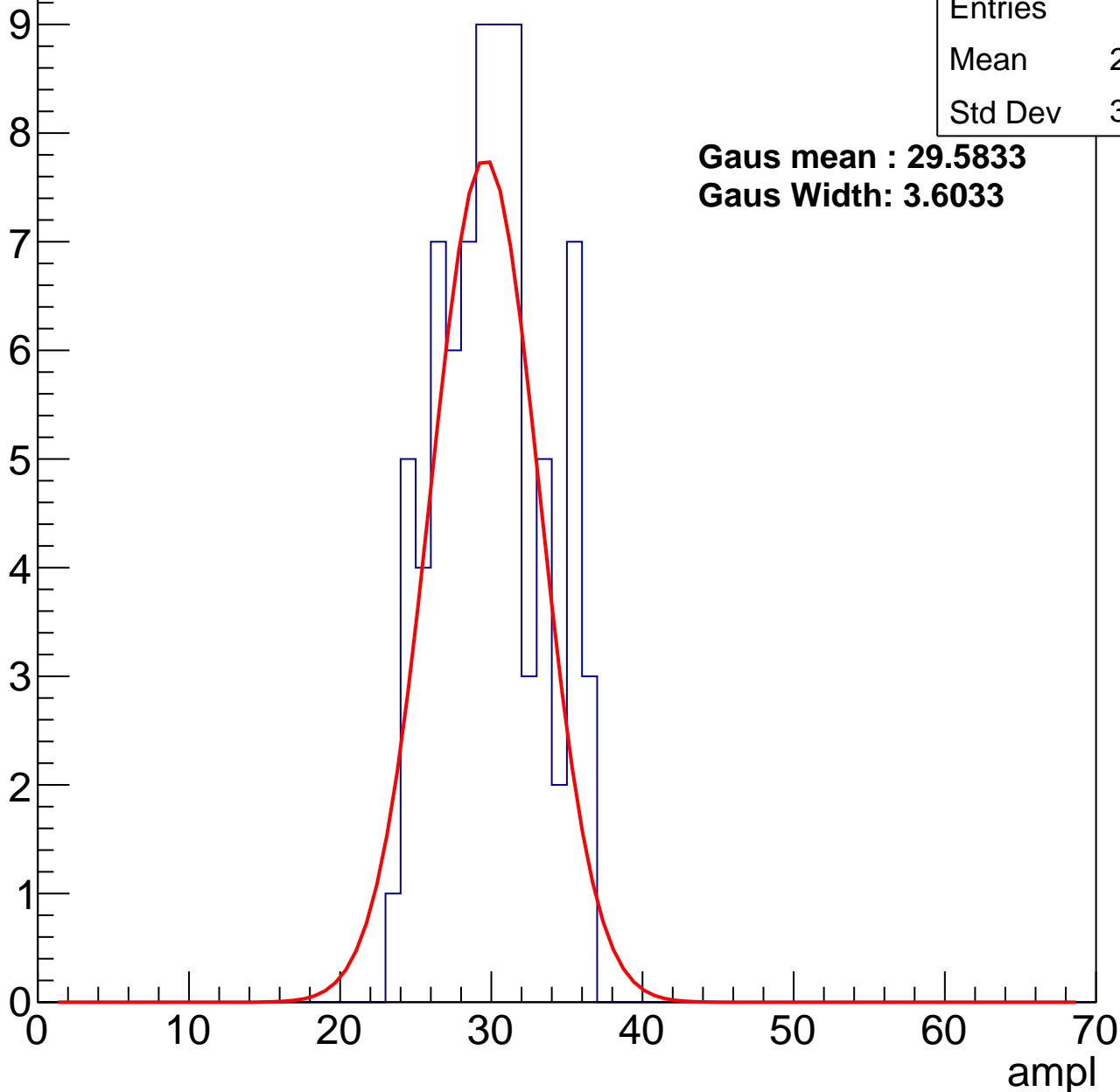
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	29.55
Std Dev	3.413

**Gaus mean : 29.5833**

**Gaus Width: 3.6033**



# B1L102S, U21-ch50, adc1

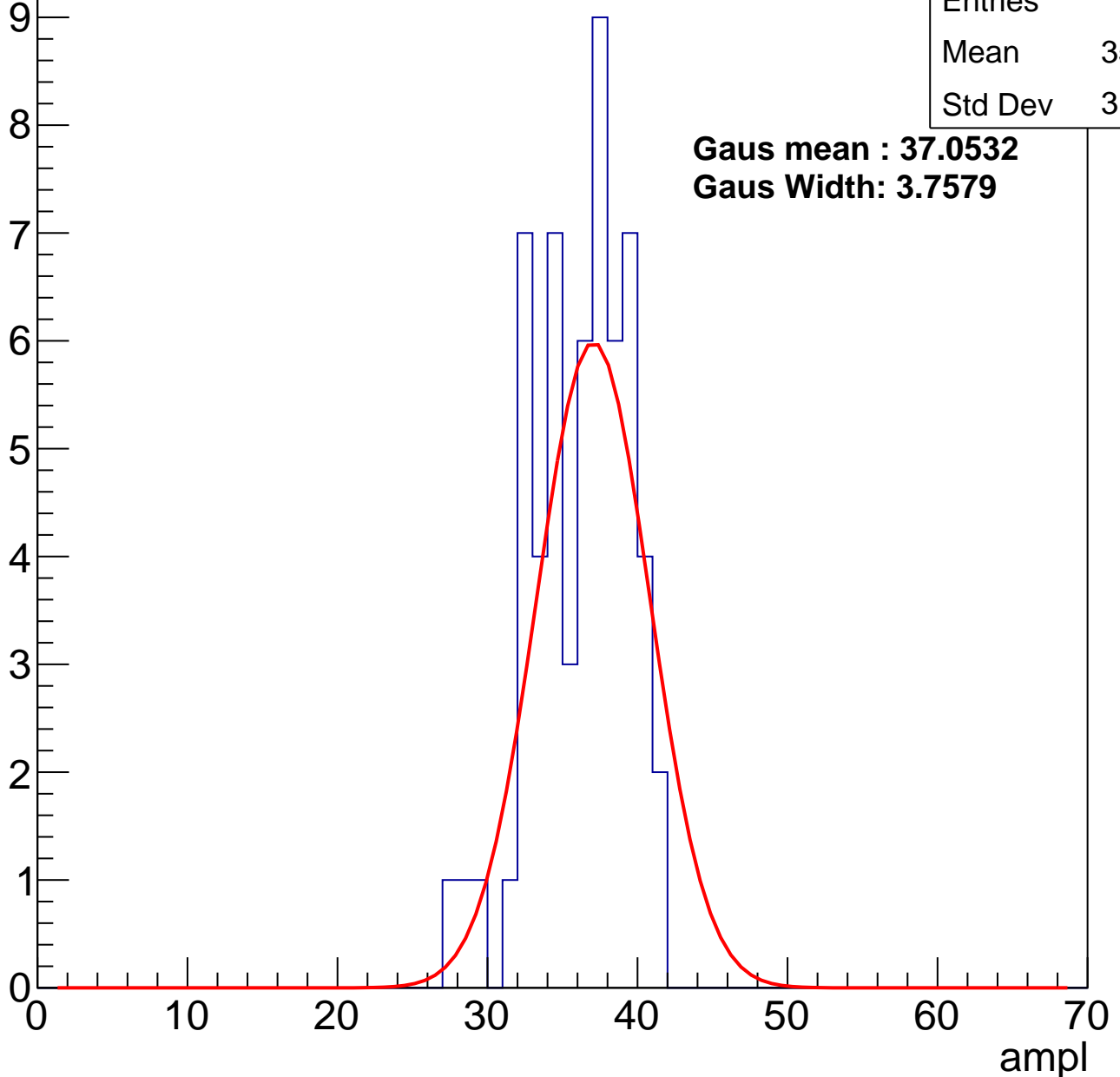
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	35.69
Std Dev	3.196

**Gaus mean : 37.0532**

**Gaus Width: 3.7579**



# B1L102S, U21-ch50, adc2

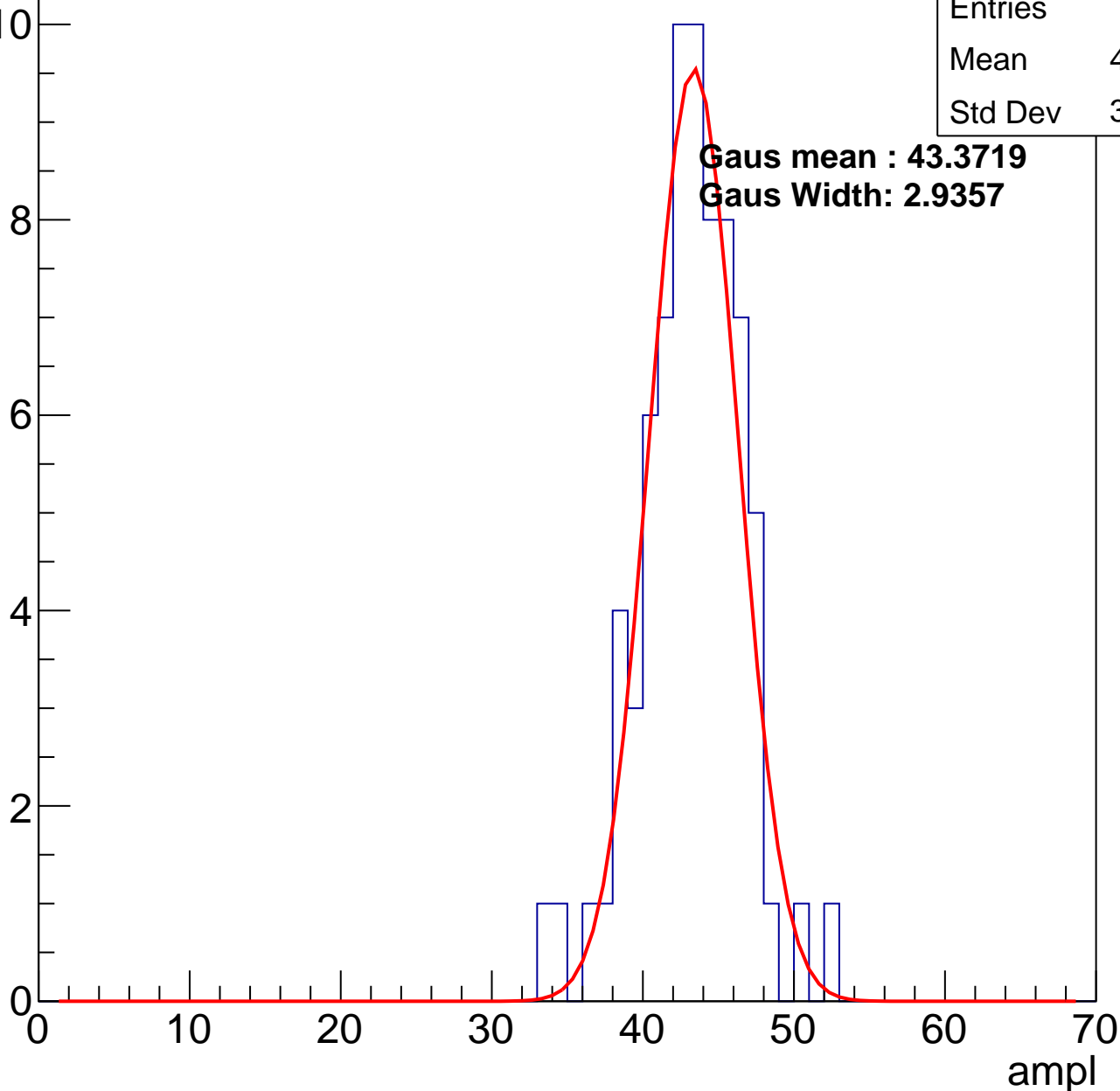
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	42.73
Std Dev	3.344

**Gaus mean : 43.3719**

**Gaus Width: 2.9357**

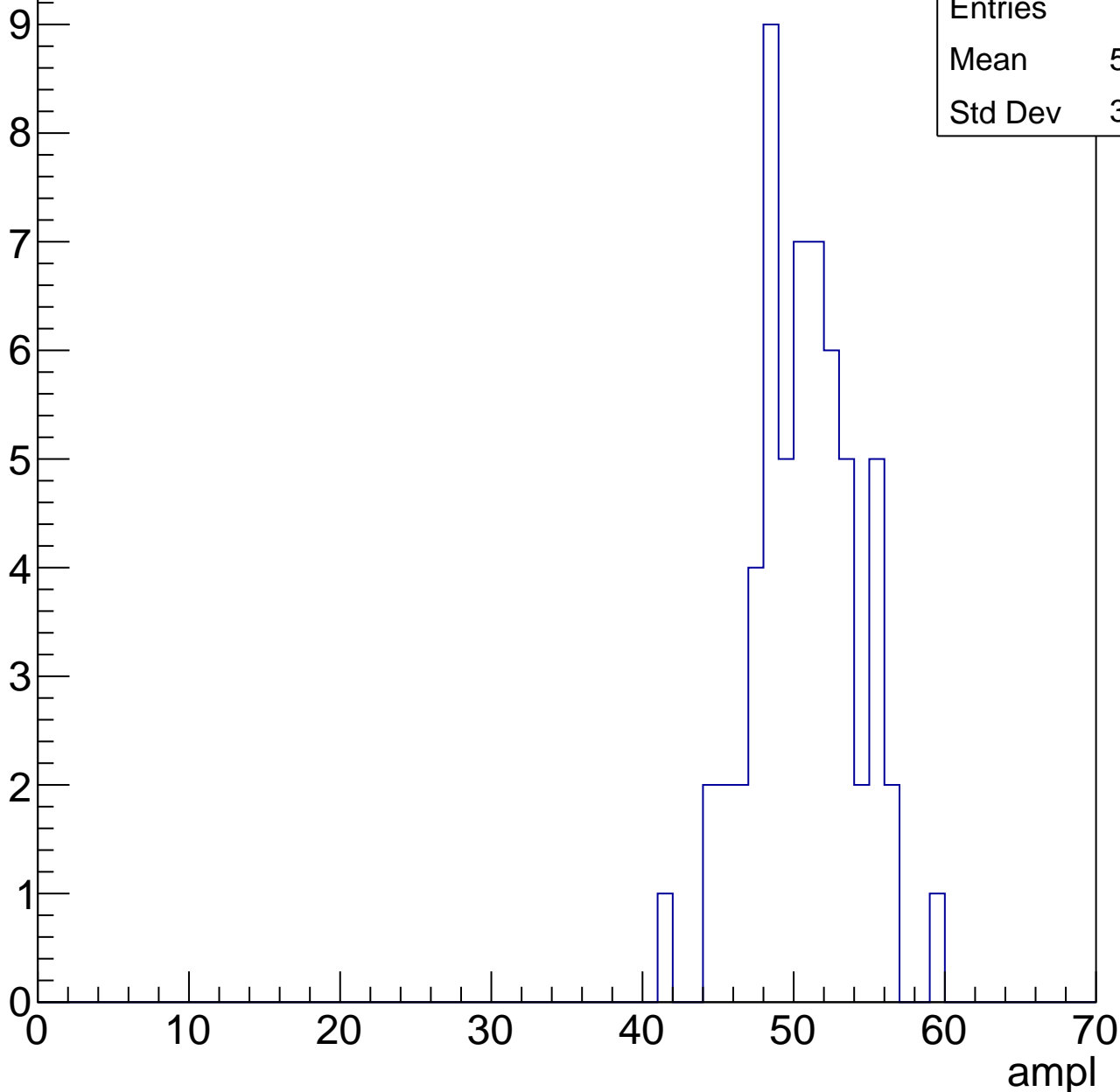


# B1L102S, U21-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	50.23
Std Dev	3.403

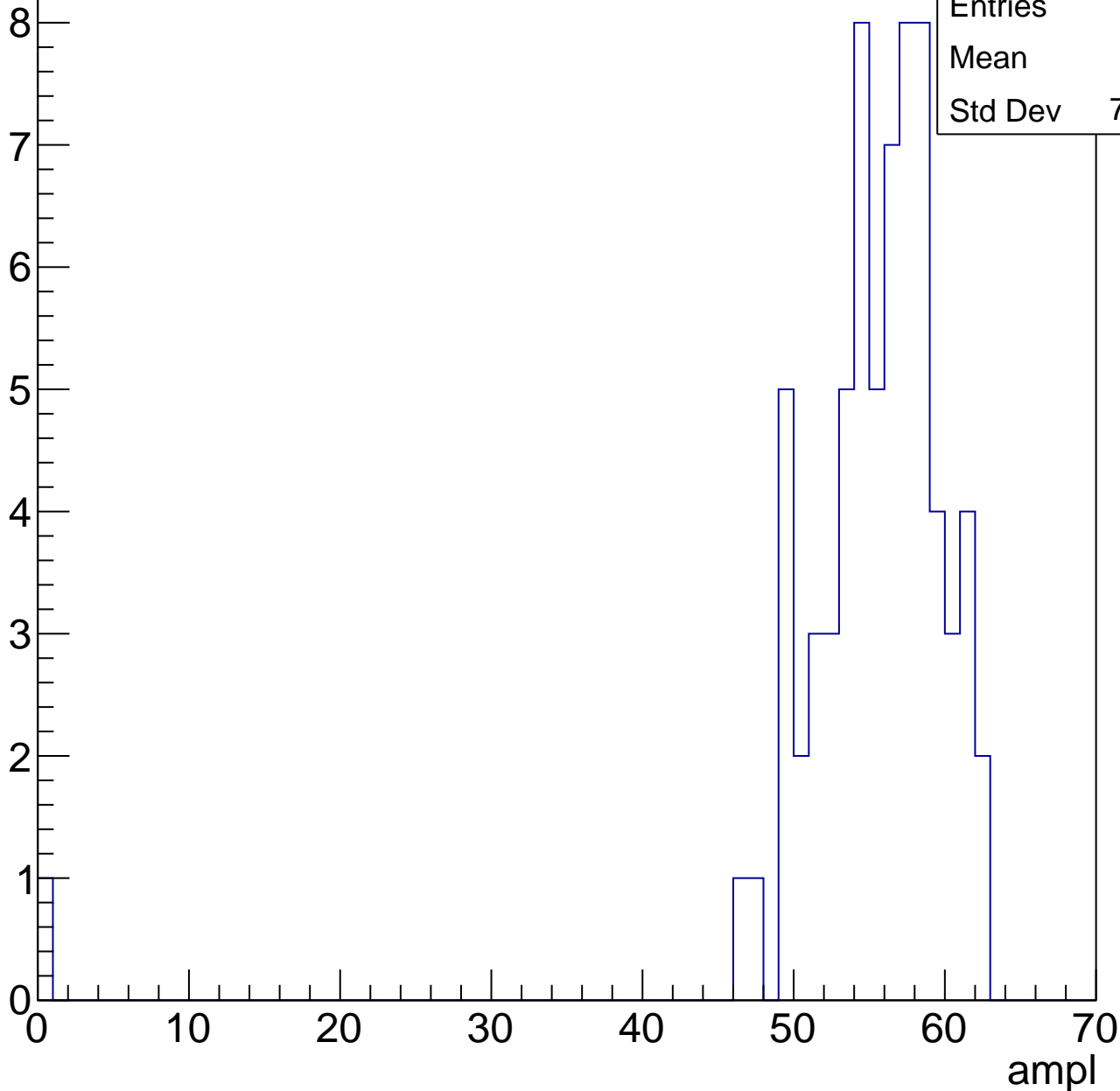


# B1L102S, U21-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	54.5
Std Dev	7.538

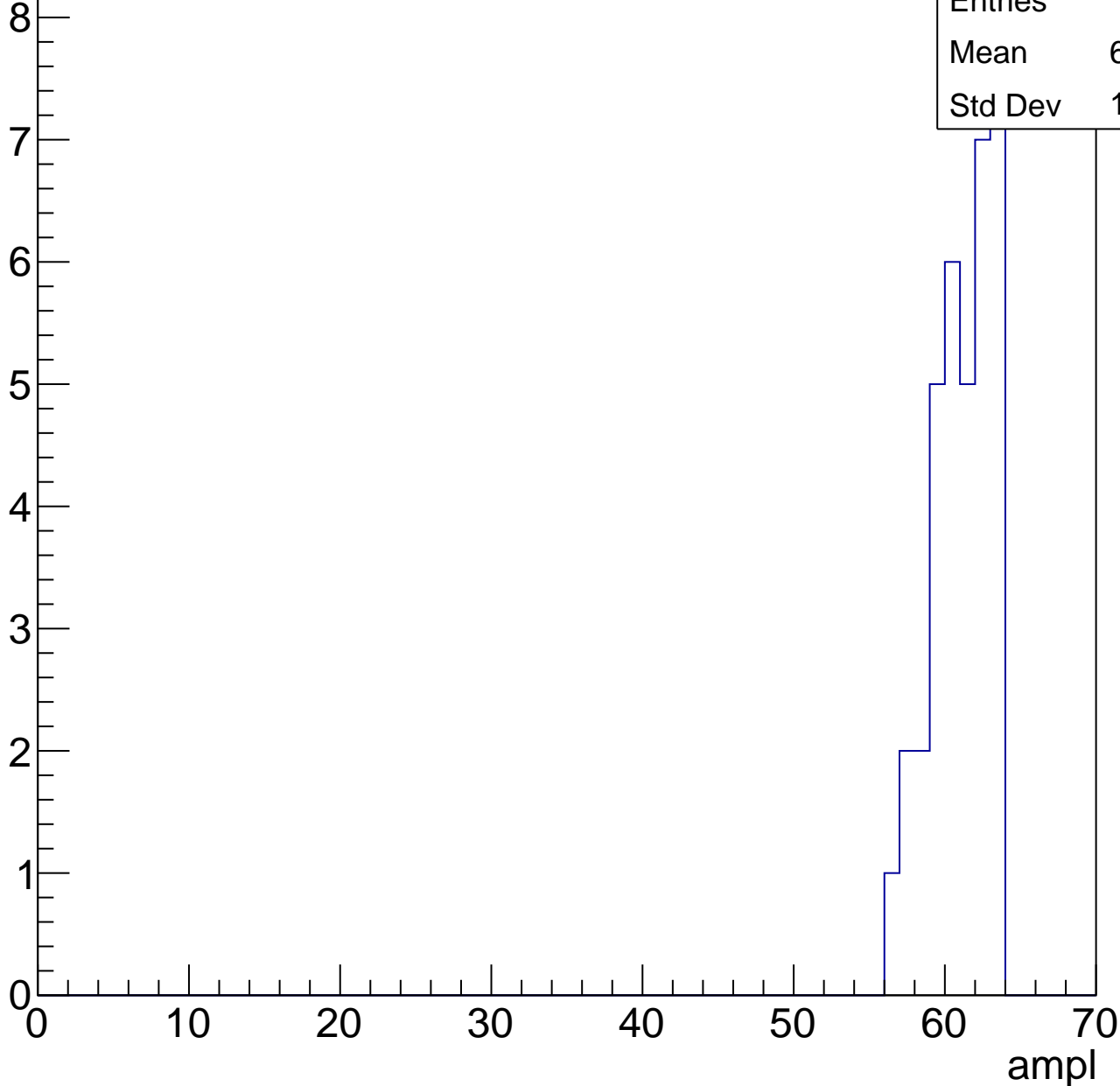


# B1L102S, U21-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	36
Mean	60.67
Std Dev	1.944



# B1L102S, U21-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	5
Mean	61.8
Std Dev	1.166



# B1L102S, U21-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	22
Std Dev	0

ampl

# B1L102S, U21-ch51, adc0

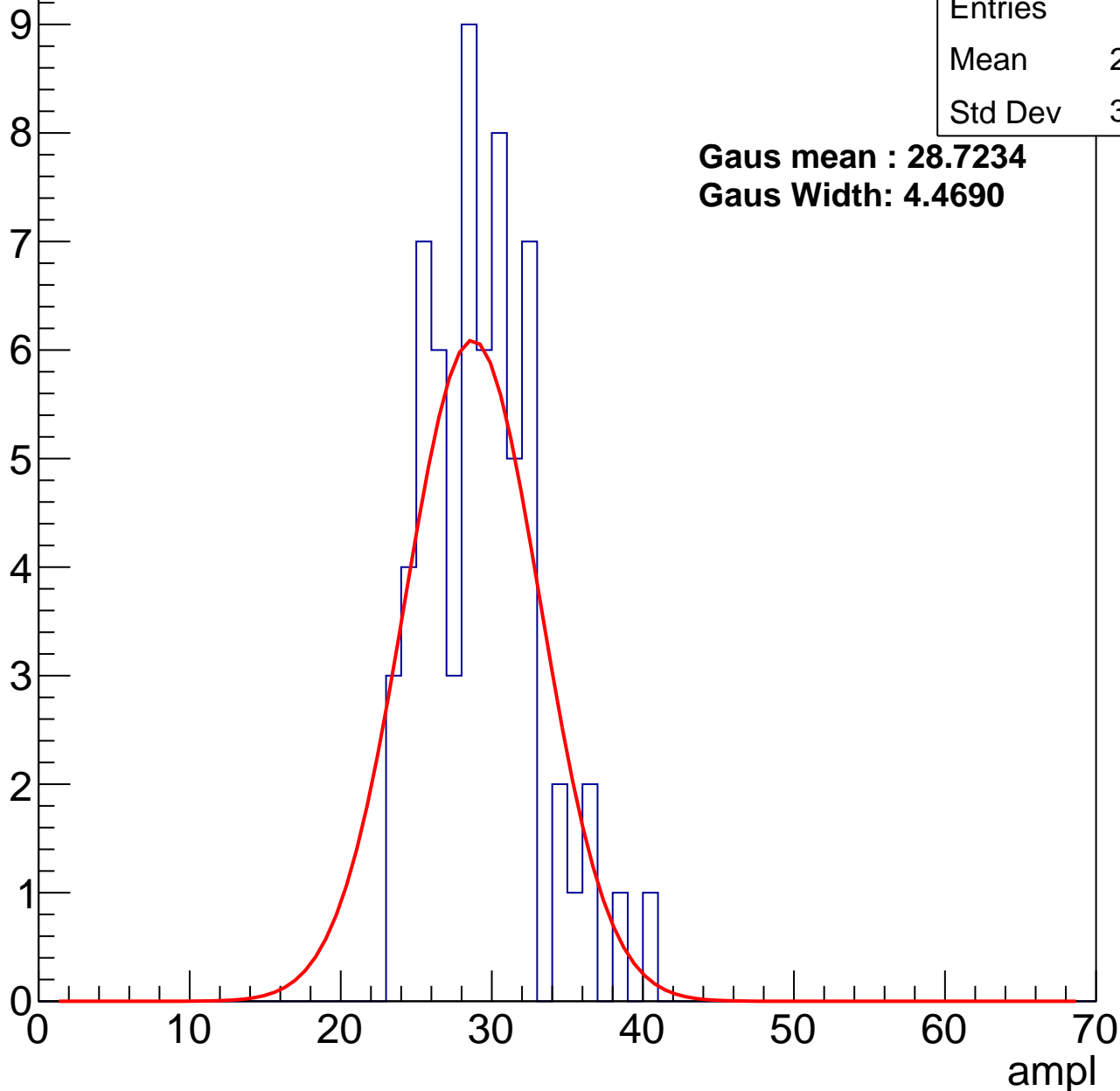
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	28.85
Std Dev	3.659

**Gaus mean : 28.7234**

**Gaus Width: 4.4690**



# B1L102S, U21-ch51, adc1

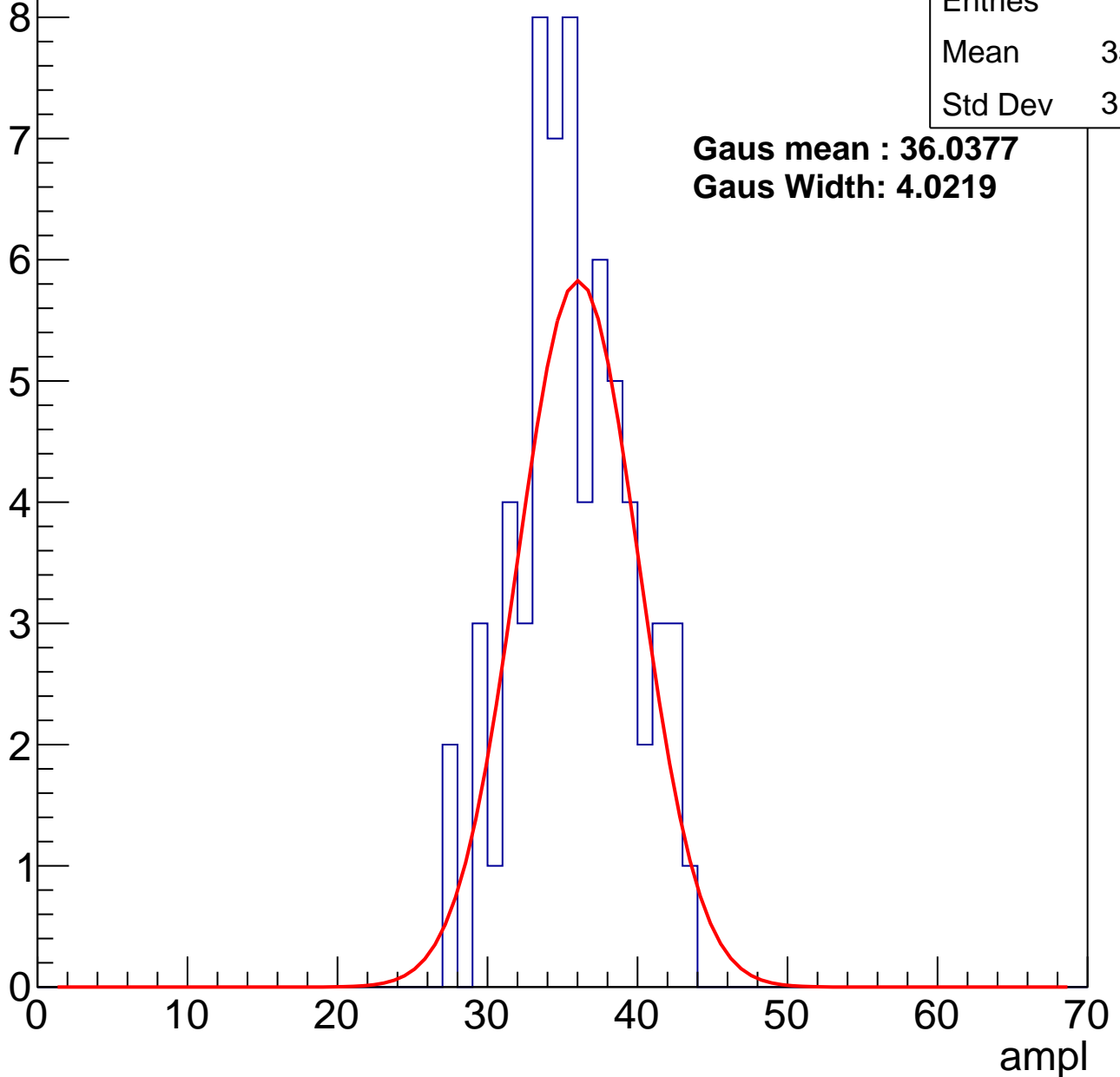
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	35.27
Std Dev	3.734

**Gaus mean : 36.0377**

**Gaus Width: 4.0219**



# B1L102S, U21-ch51, adc2

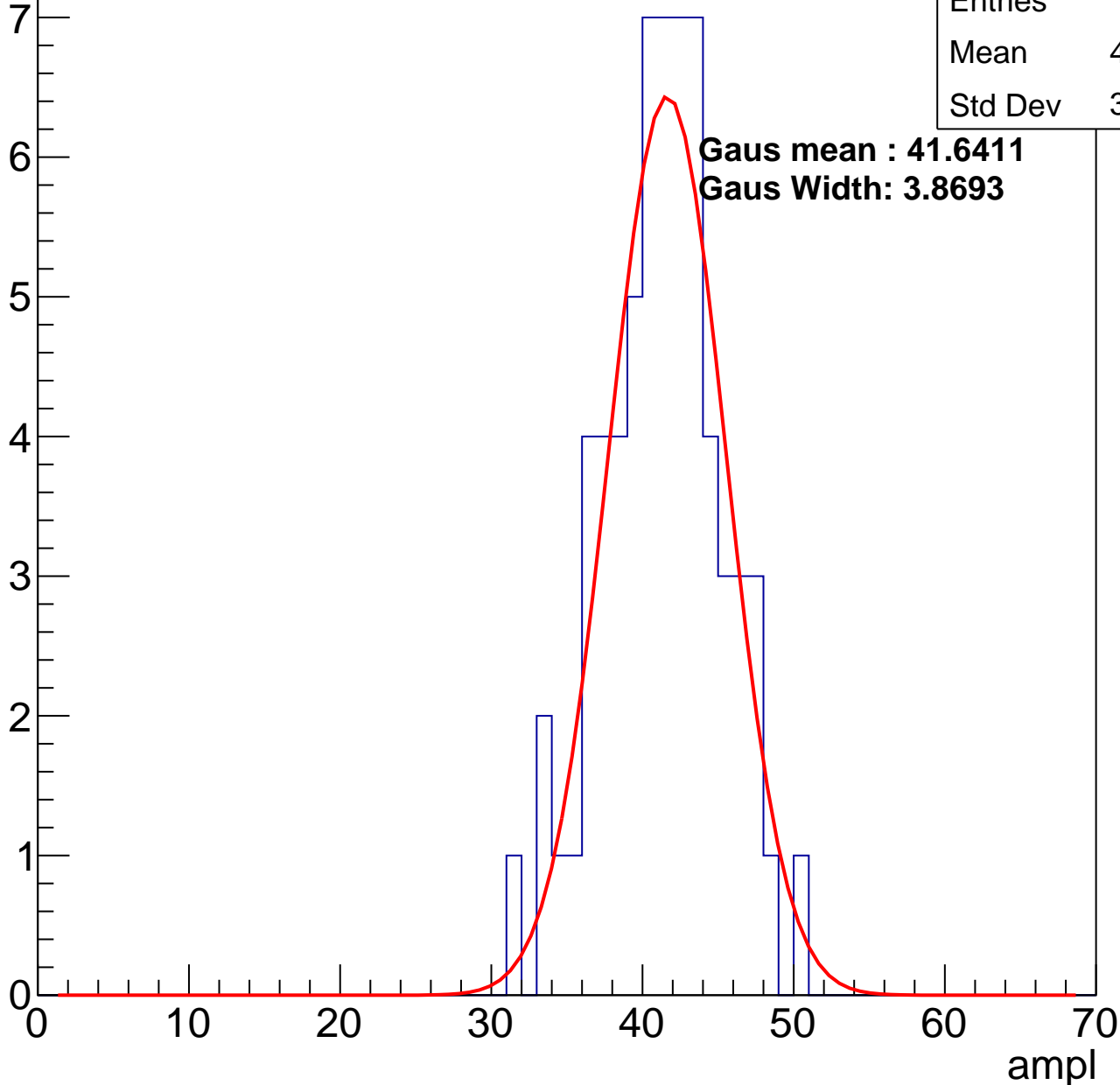
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	40.85
Std Dev	3.864

**Gaus mean : 41.6411**

**Gaus Width: 3.8693**

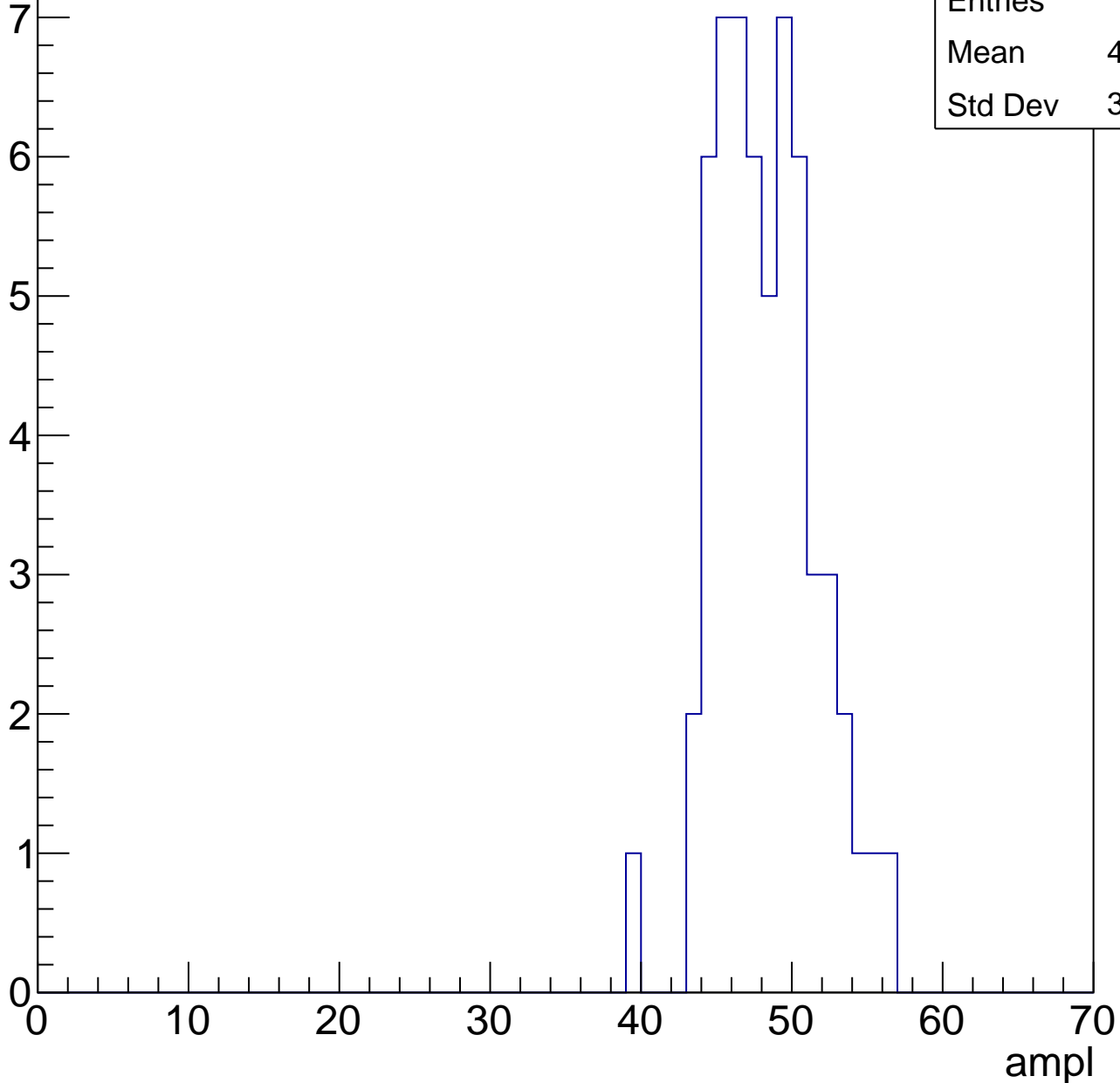


# B1L102S, U21-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	47.78
Std Dev	3.286

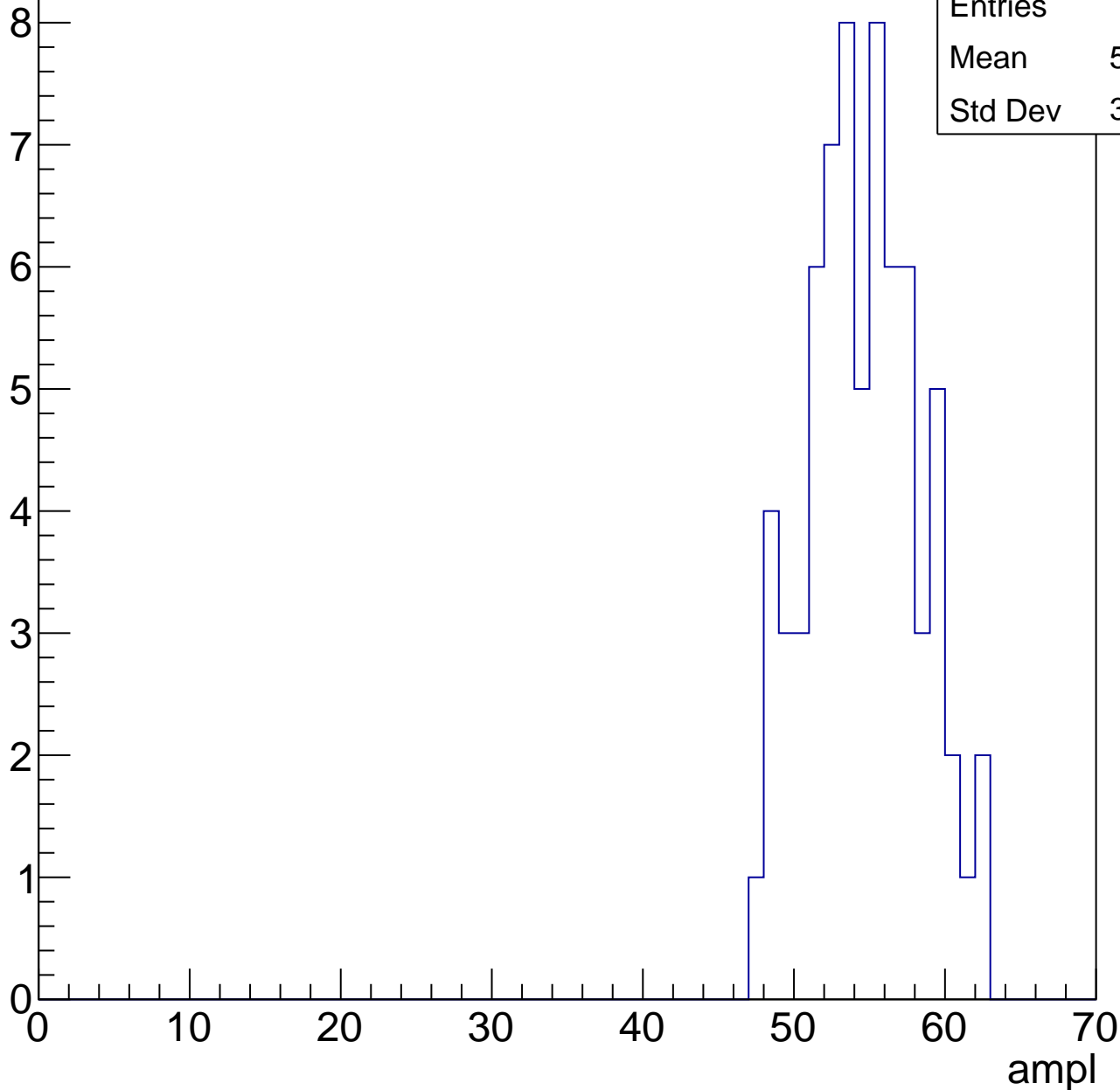


# B1L102S, U21-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	54.17
Std Dev	3.609

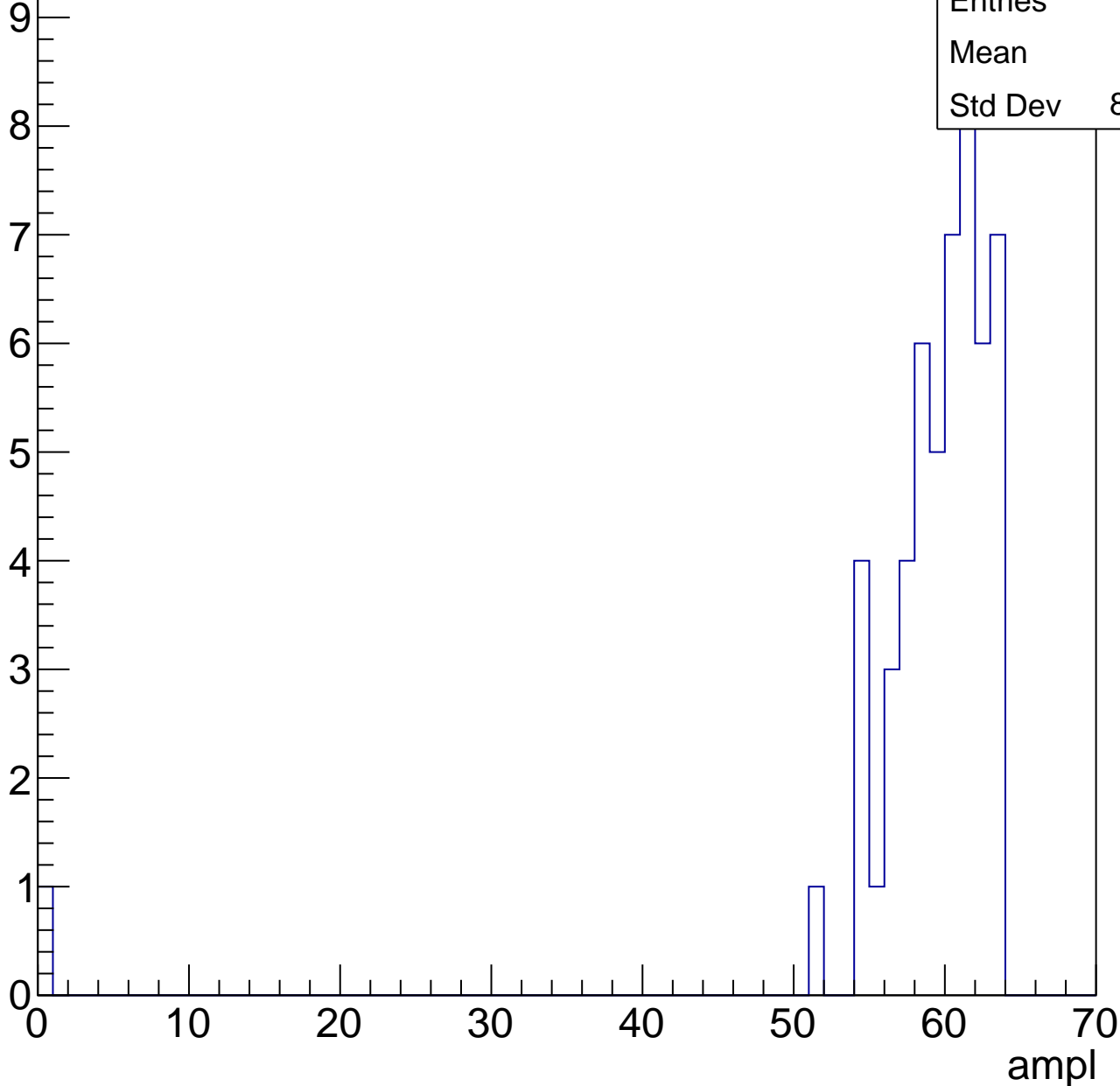


# B1L102S, U21-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

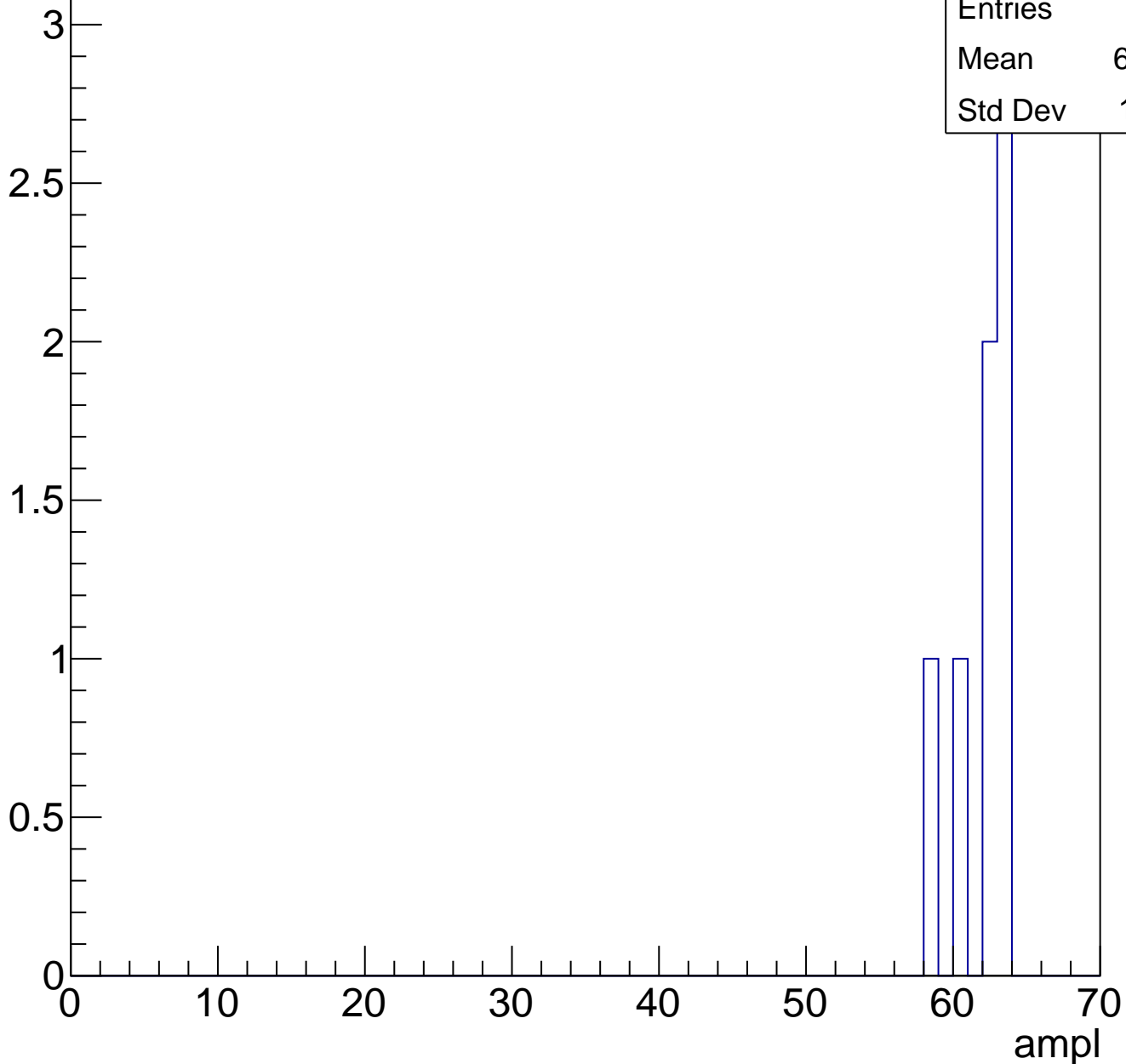
Entries	54
Mean	58.2
Std Dev	8.482



# B1L102S, U21-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch52, adc0

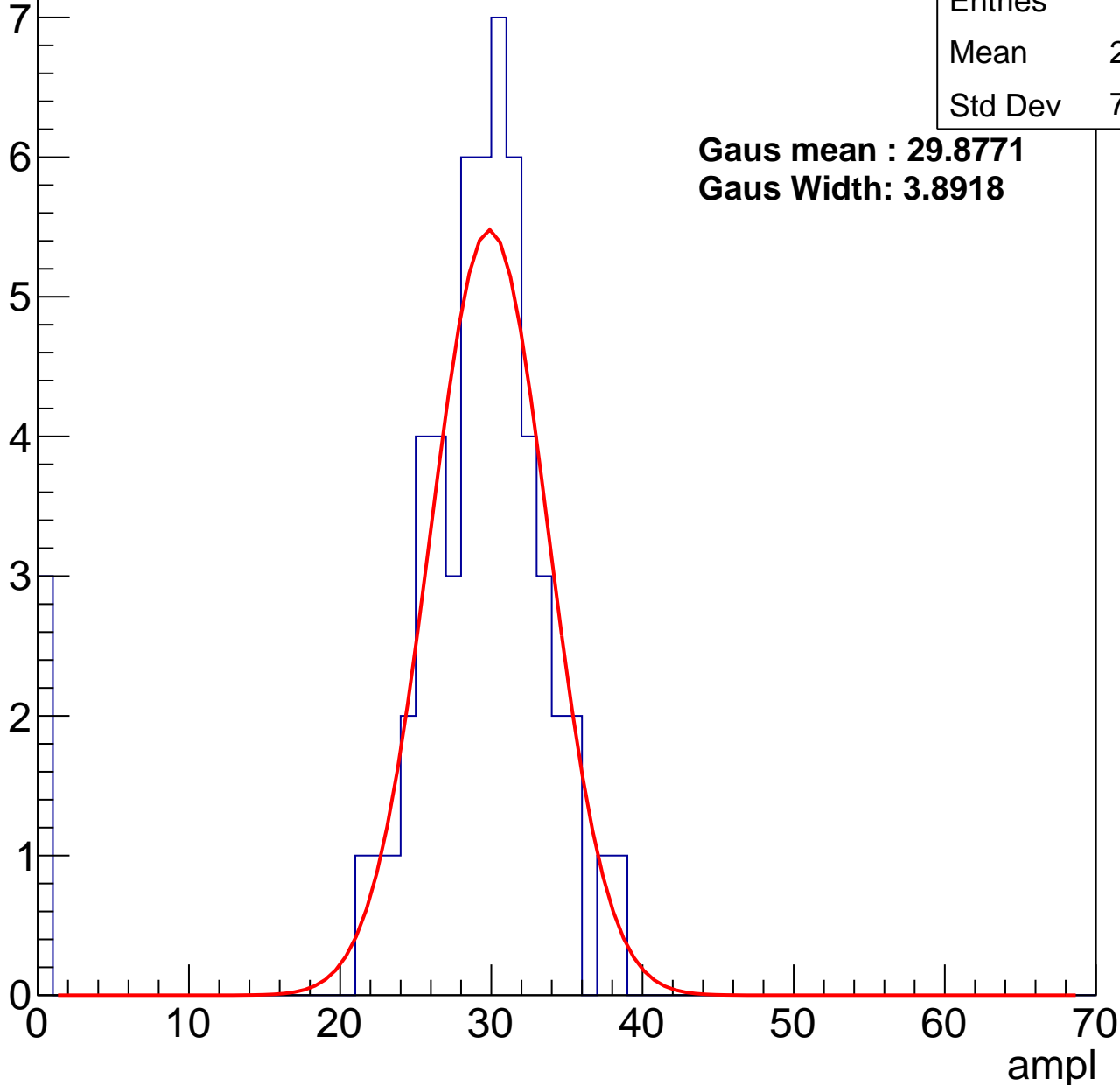
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	27.67
Std Dev	7.399

**Gaus mean : 29.8771**

**Gaus Width: 3.8918**



# B1L102S, U21-ch52, adc1

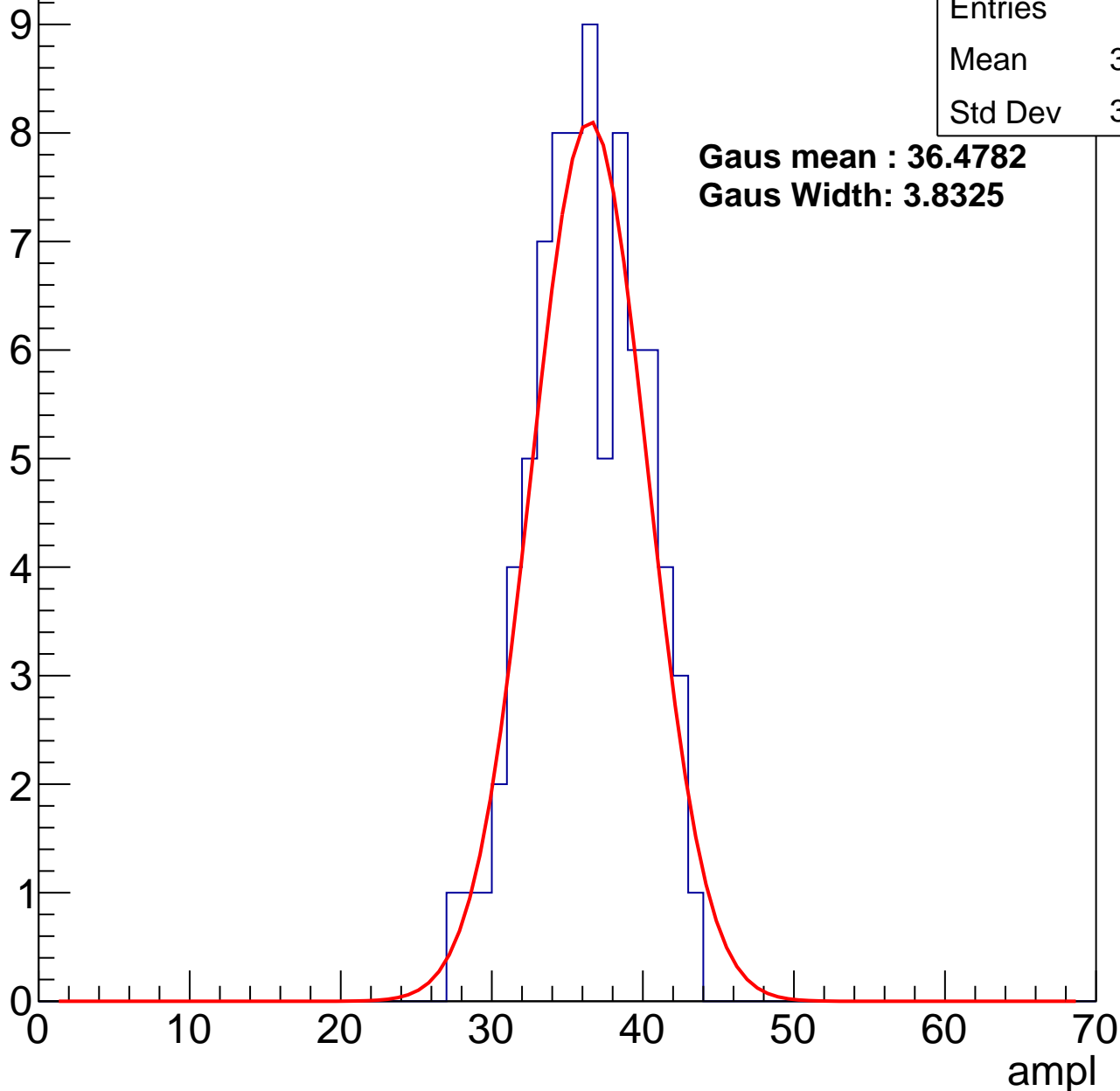
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	35.84
Std Dev	3.542

**Gaus mean : 36.4782**

**Gaus Width: 3.8325**



# B1L102S, U21-ch52, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	43.55
Std Dev	3.388

**Gaus mean : 44.1529**

**Gaus Width: 3.2788**

10

8

6

4

2

0

ampl

0

10

20

30

40

50

60

70

# B1L102S, U21-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	66
Mean	50.73
Std Dev	3.788

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

70

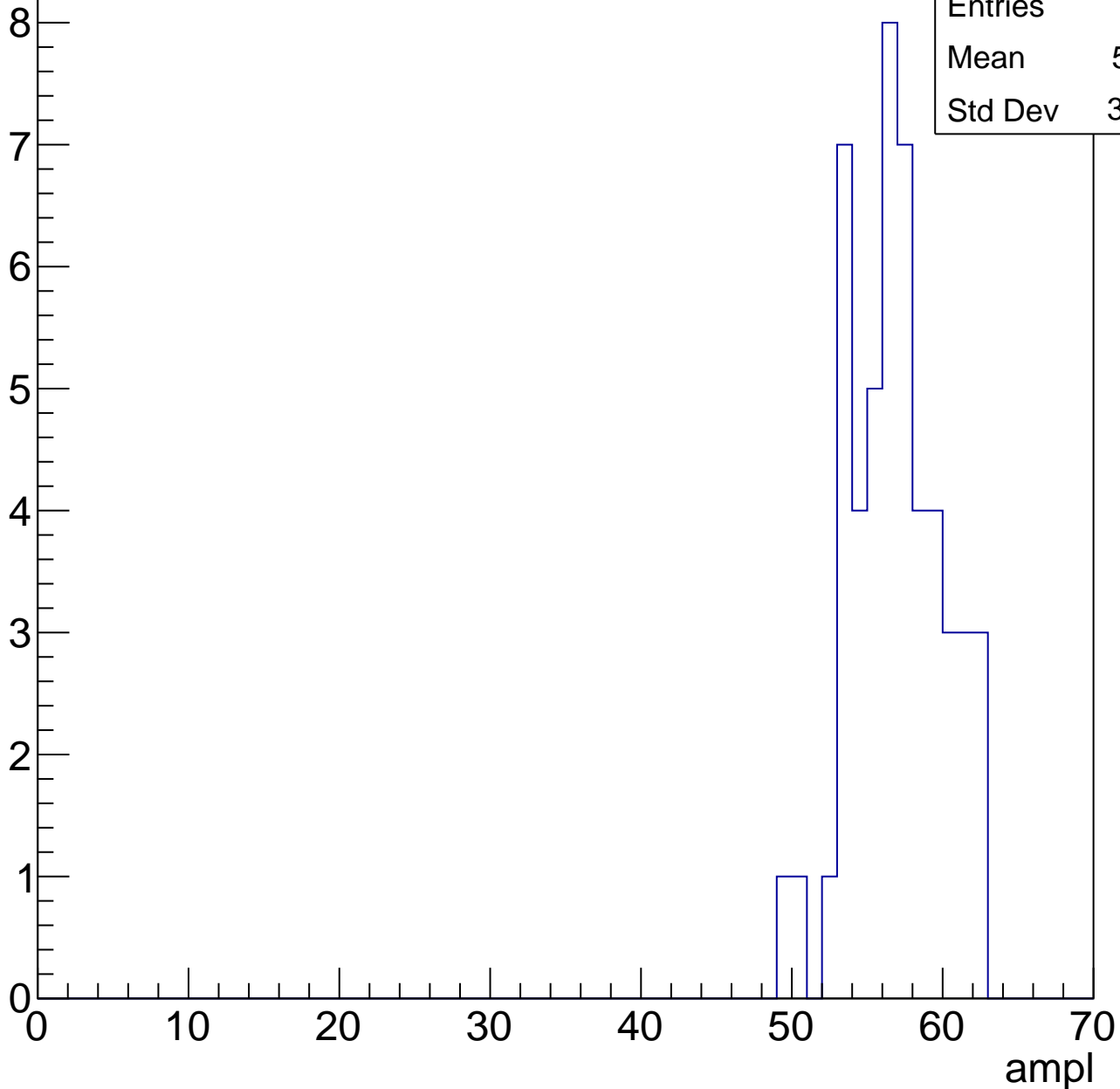


# B1L102S, U21-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	56.41
Std Dev	3.024

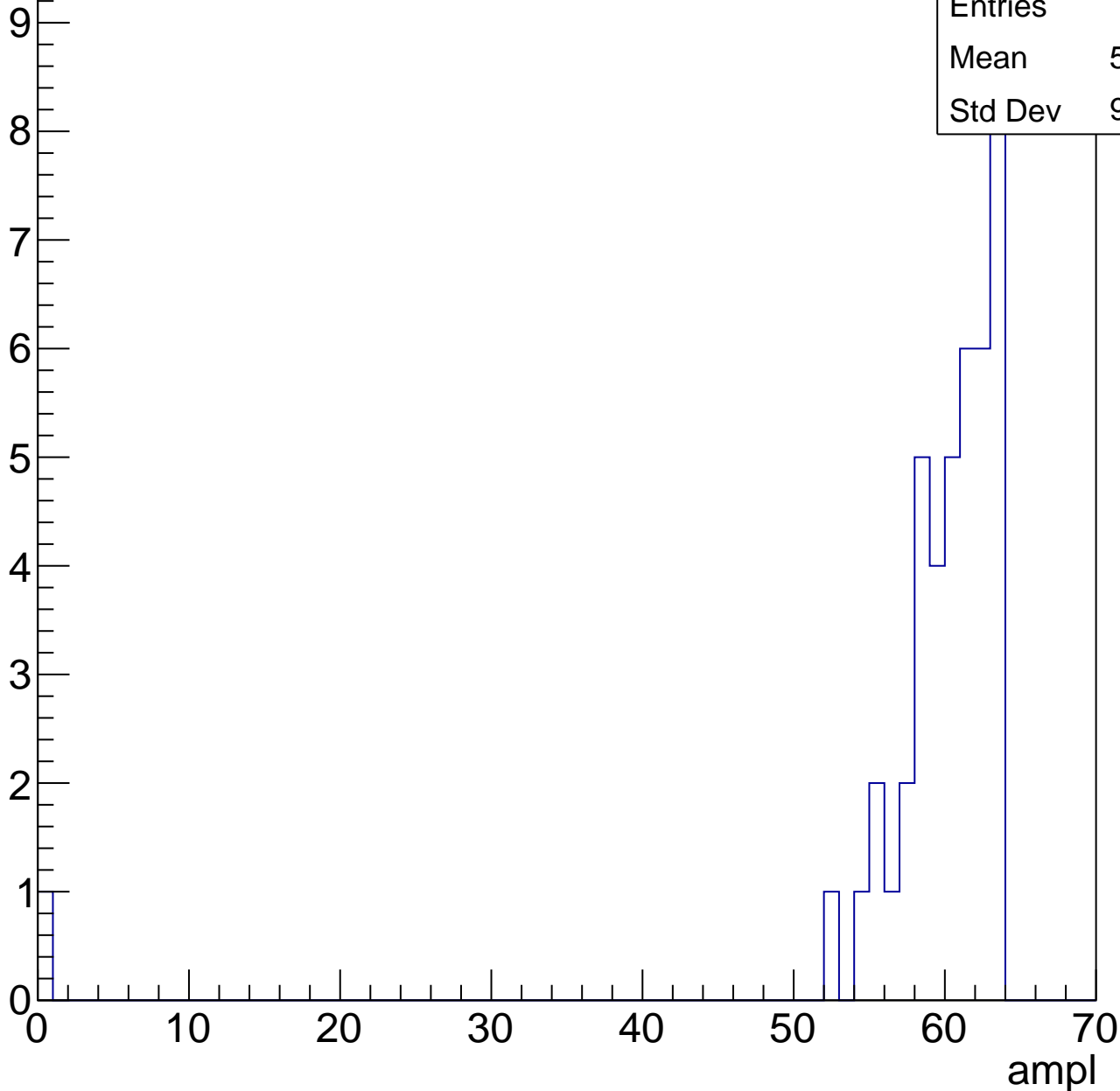


# B1L102S, U21-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

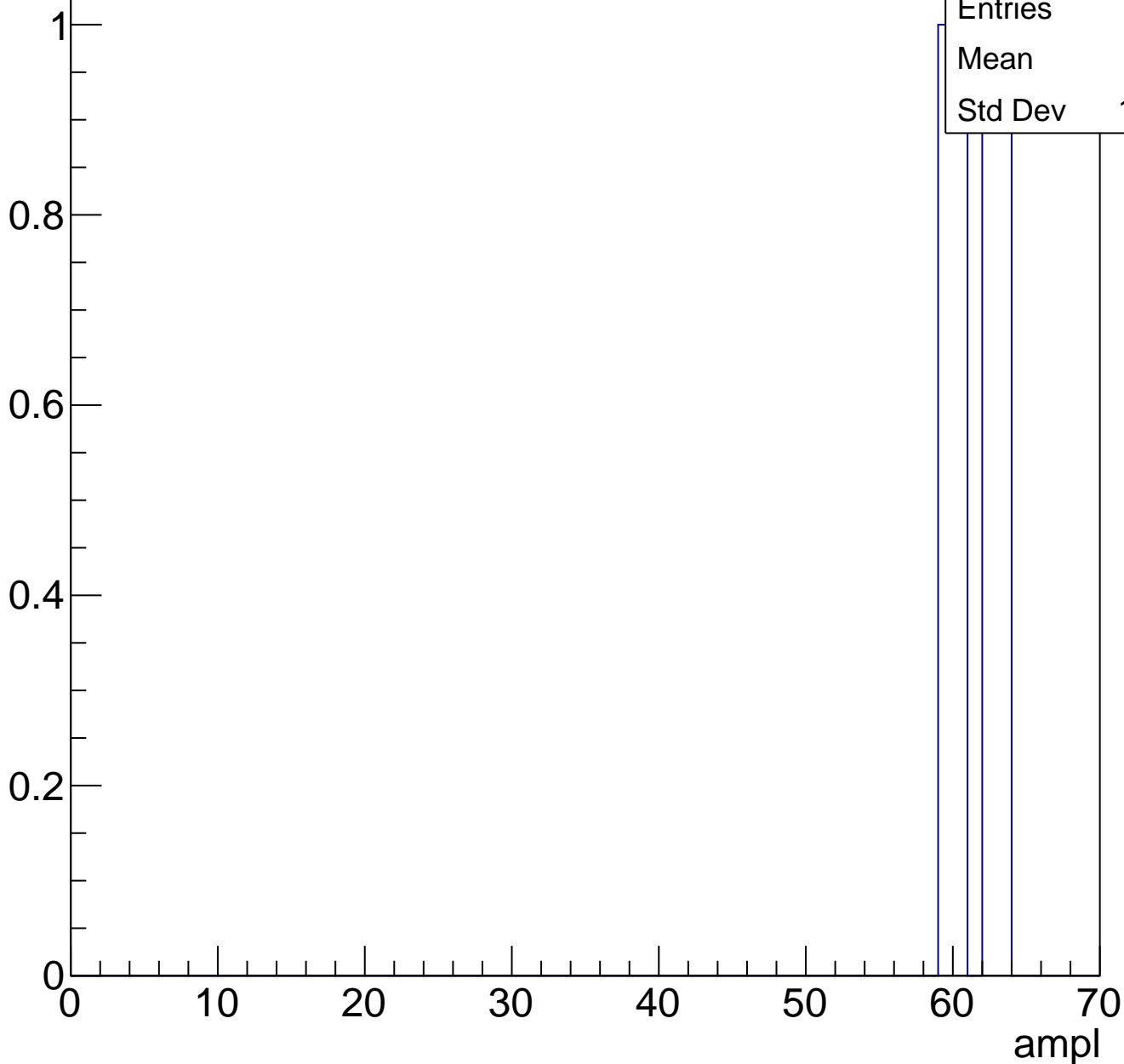
Entries	43
Mean	58.53
Std Dev	9.434



# B1L102S, U21-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U21-ch53, adc0

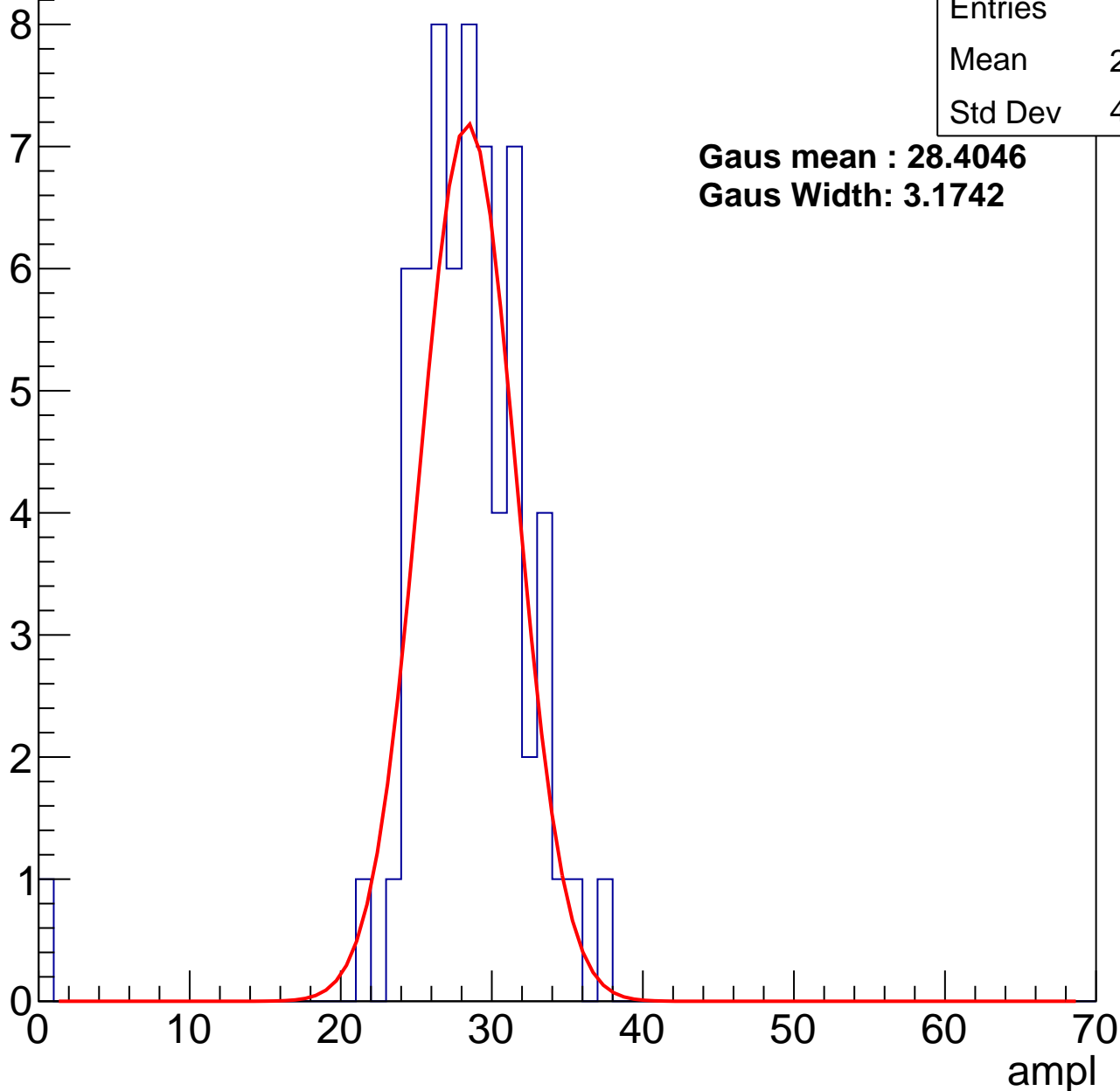
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	27.72
Std Dev	4.719

**Gaus mean : 28.4046**

**Gaus Width: 3.1742**



# B1L102S, U21-ch53, adc1

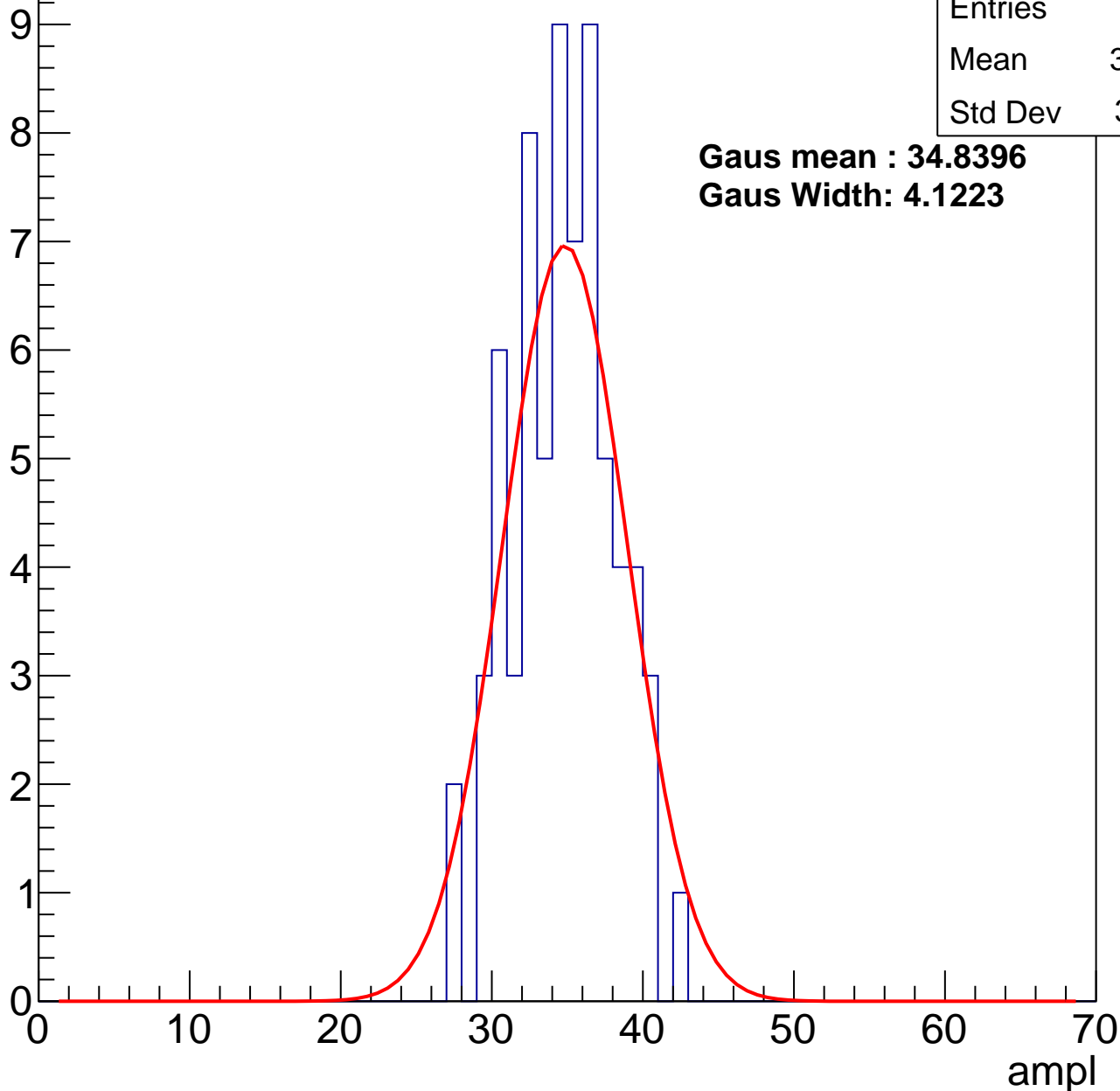
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	34.28
Std Dev	3.301

**Gaus mean : 34.8396**

**Gaus Width: 4.1223**



# B1L102S, U21-ch53, adc2

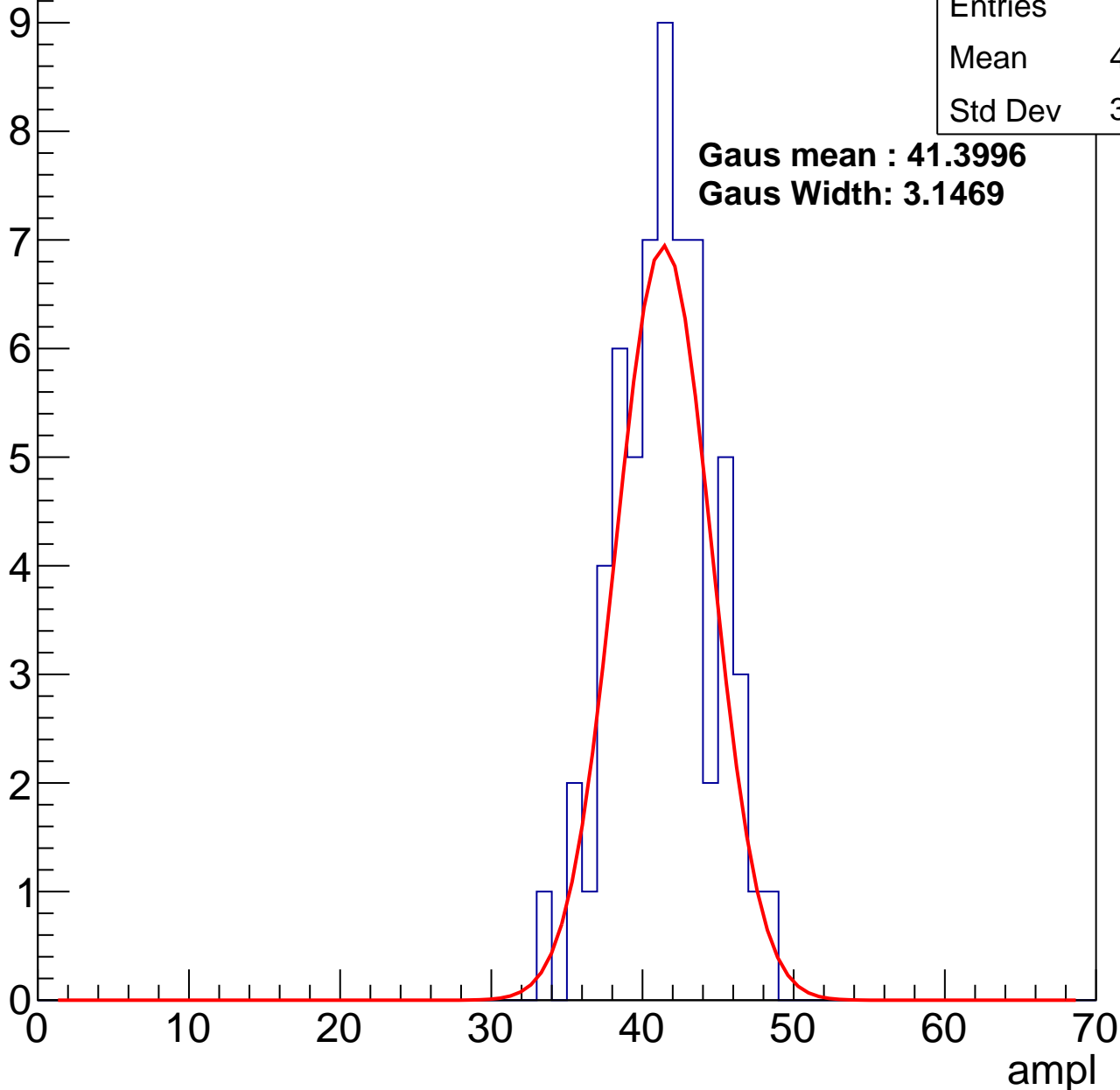
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	40.98
Std Dev	3.134

**Gaus mean : 41.3996**

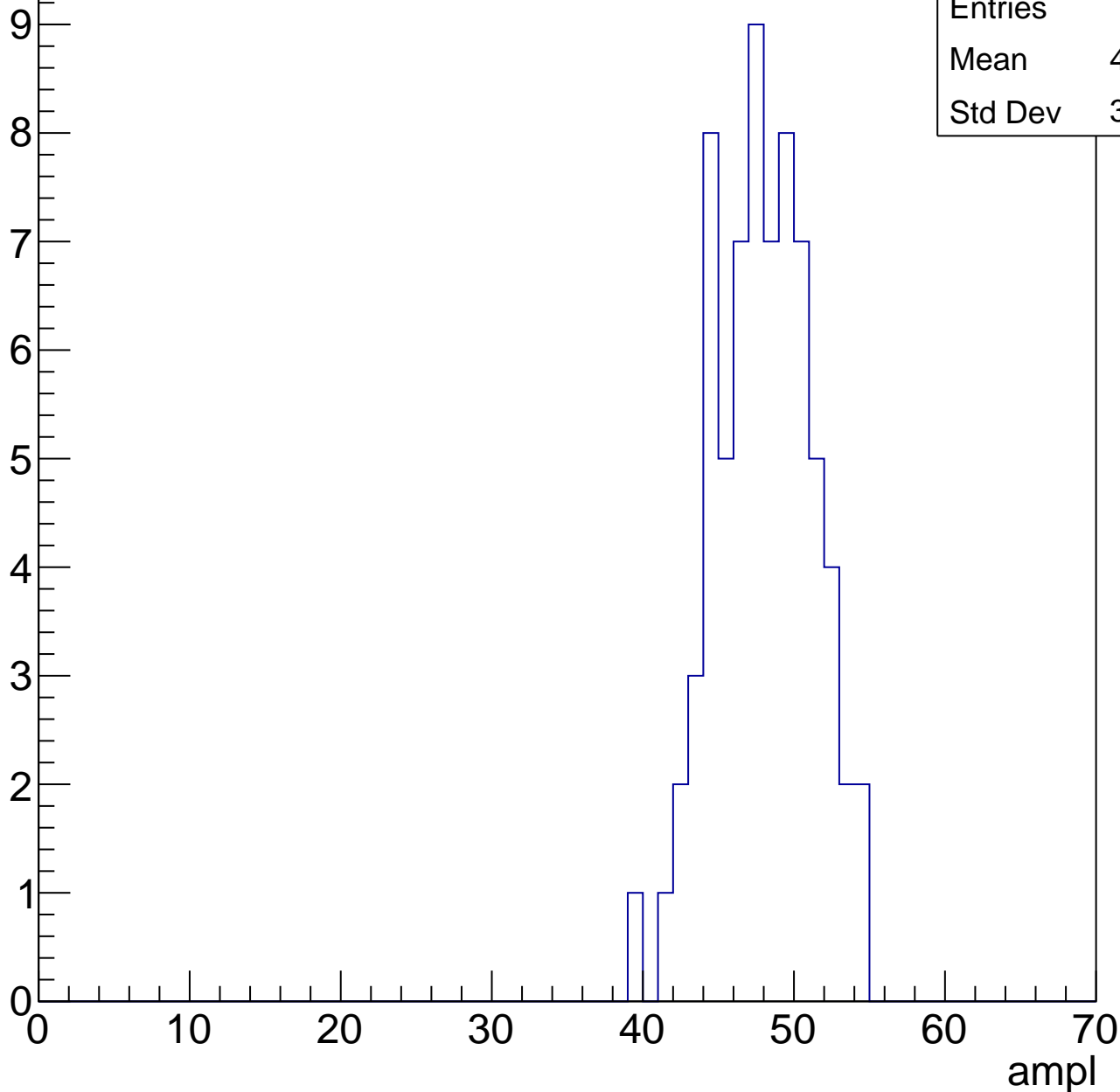
**Gaus Width: 3.1469**



# B1L102S, U21-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

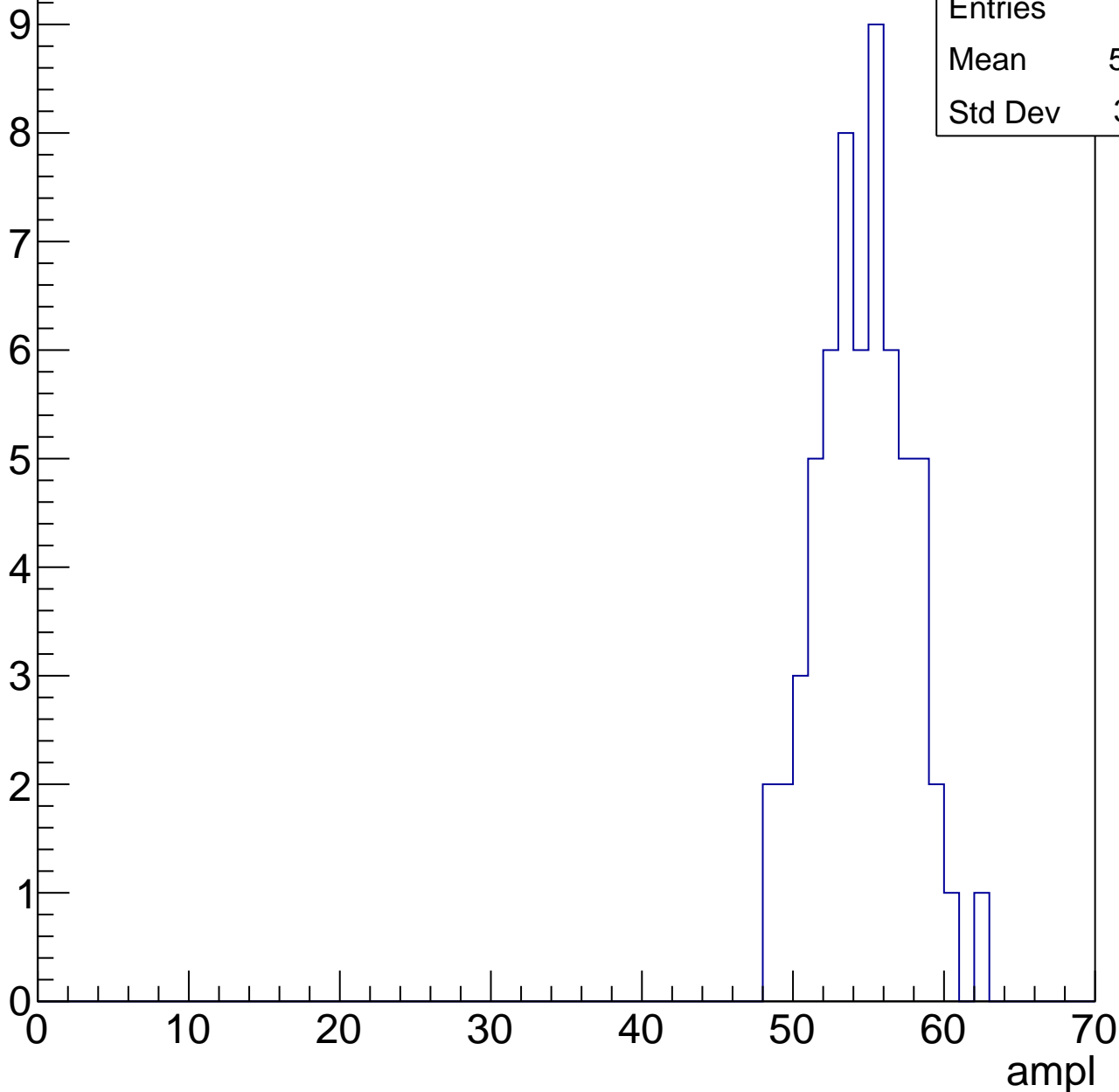


# B1L102S, U21-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	54.18
Std Dev	3.011



# B1L102S, U21-ch53, adc5

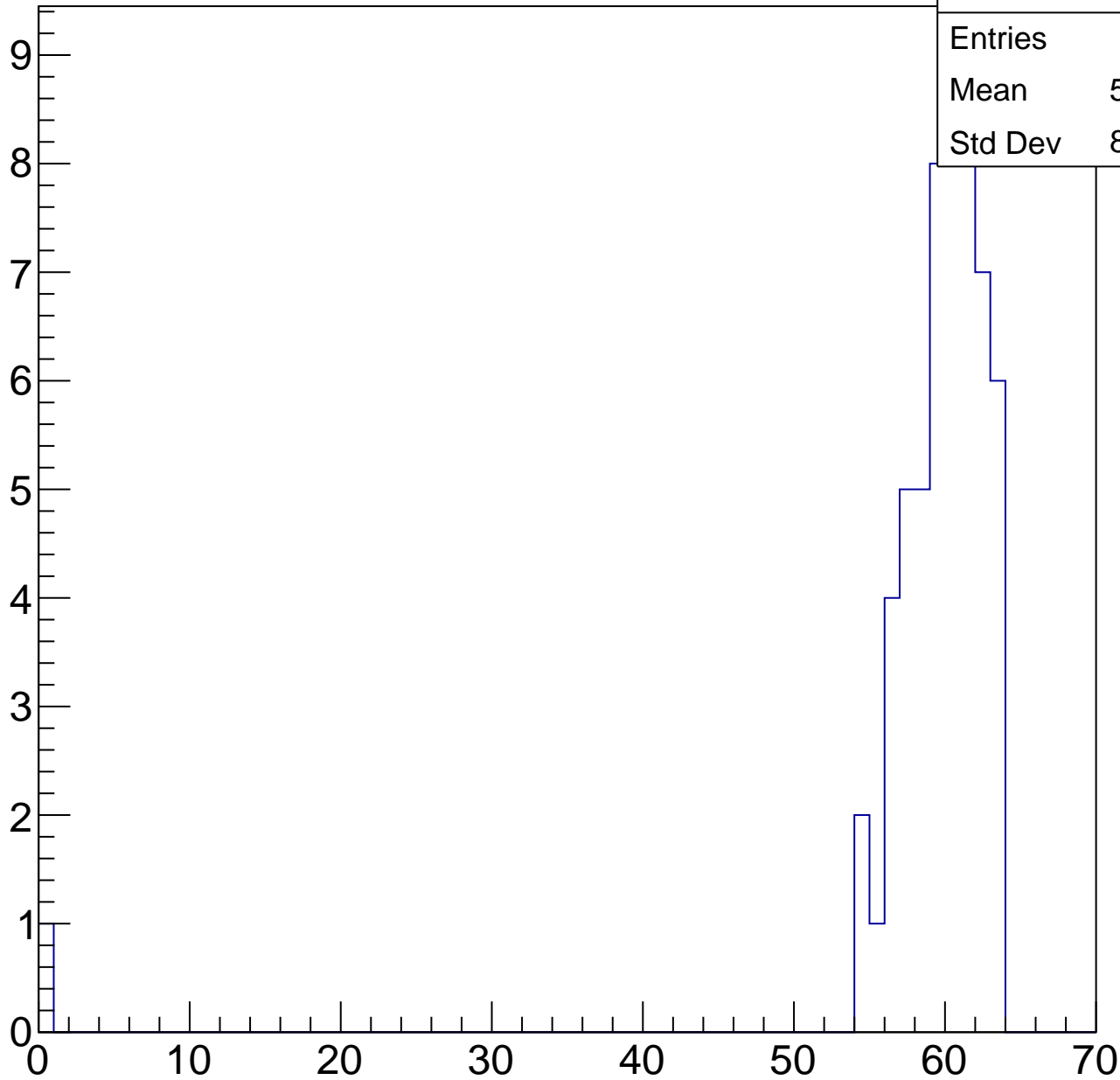
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	56
Mean	58.46
Std Dev	8.229

ampl



# B1L102S, U21-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U21-ch54, adc0

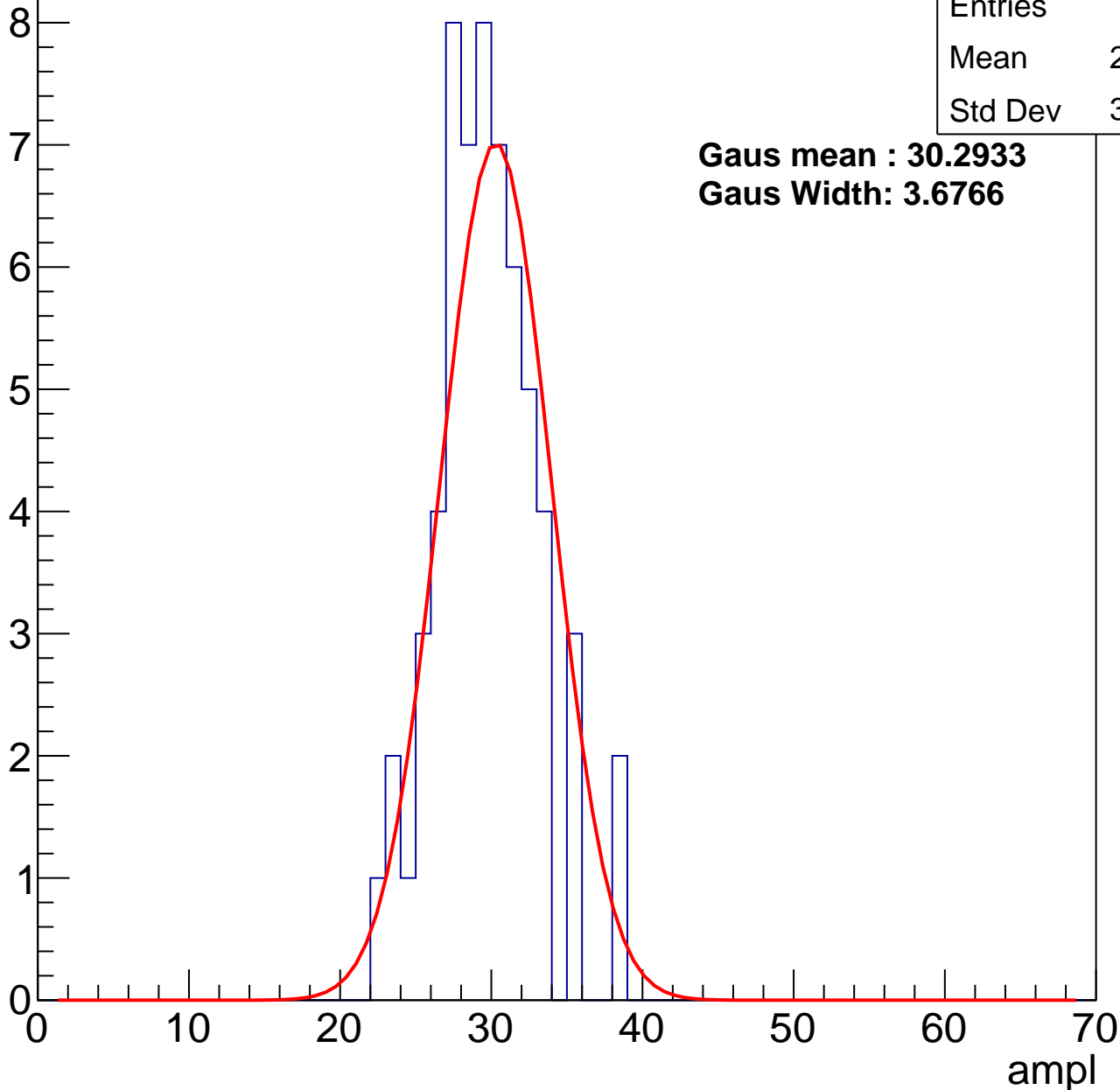
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	29.25
Std Dev	3.327

**Gaus mean : 30.2933**

**Gaus Width: 3.6766**



# B1L102S, U21-ch54, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	84
Mean	36.05
Std Dev	3.897

**Gaus mean : 36.6736**

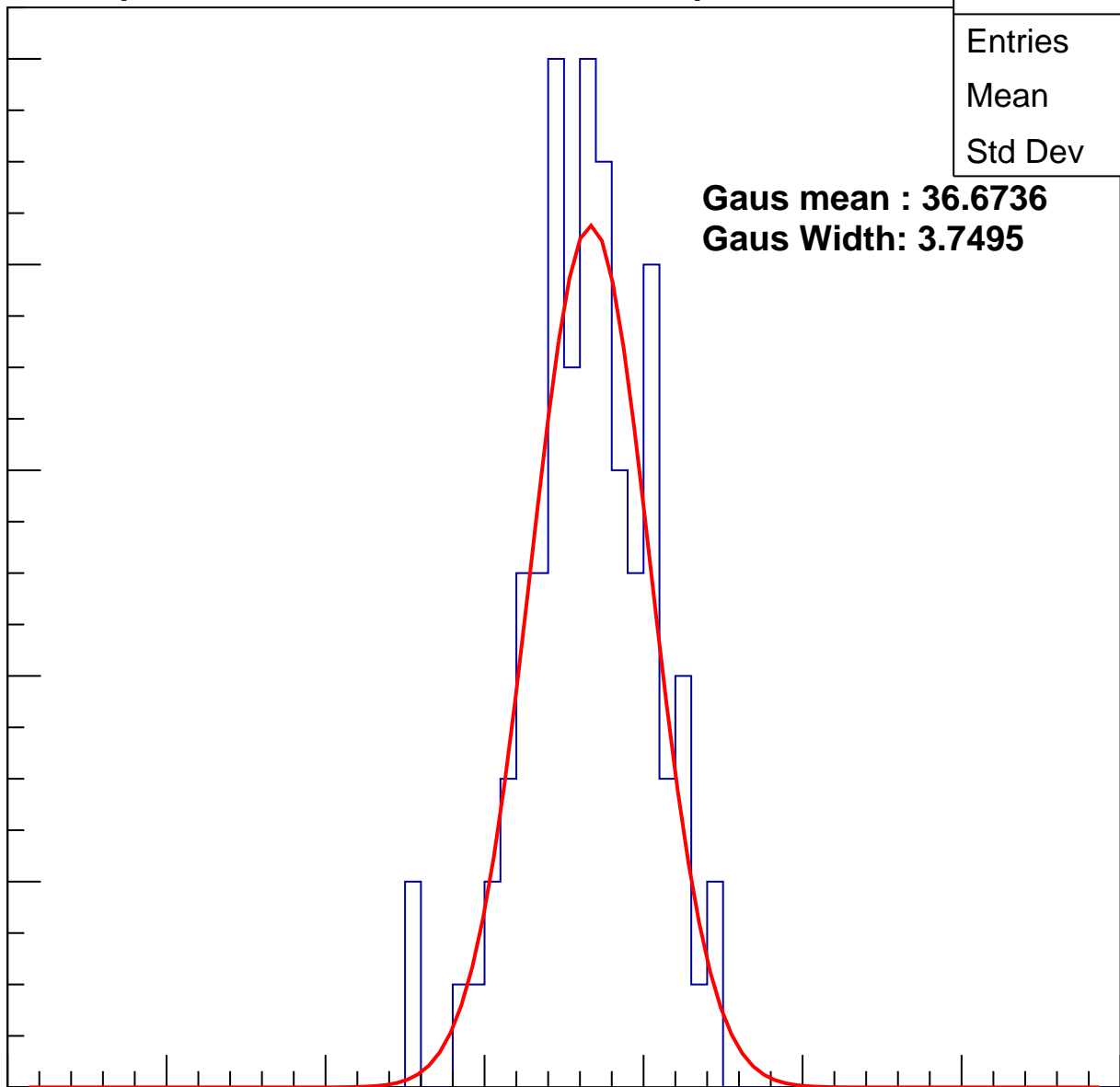
**Gaus Width: 3.7495**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U21-ch54, adc2

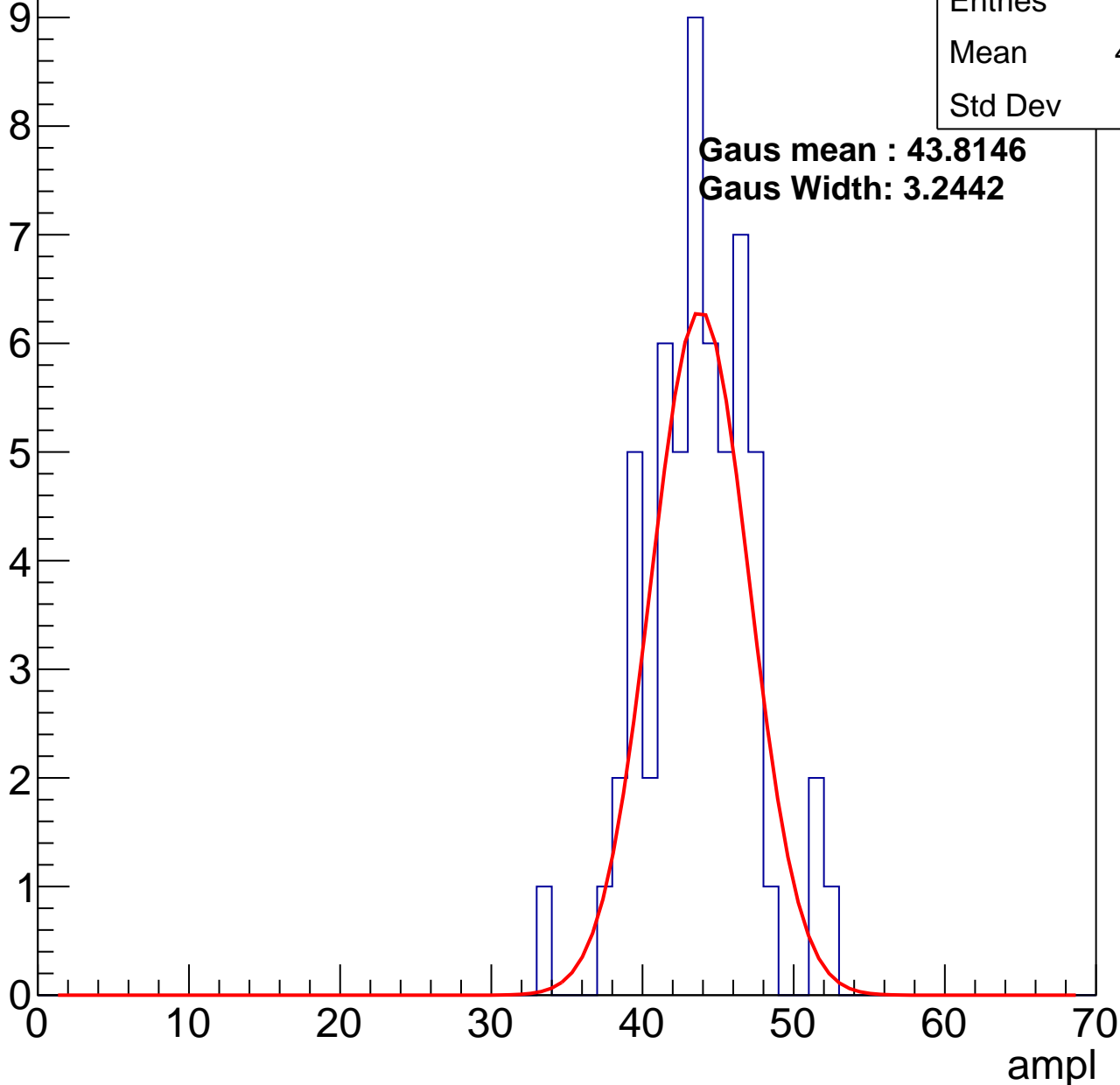
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	43.31
Std Dev	3.5

**Gaus mean : 43.8146**

**Gaus Width: 3.2442**

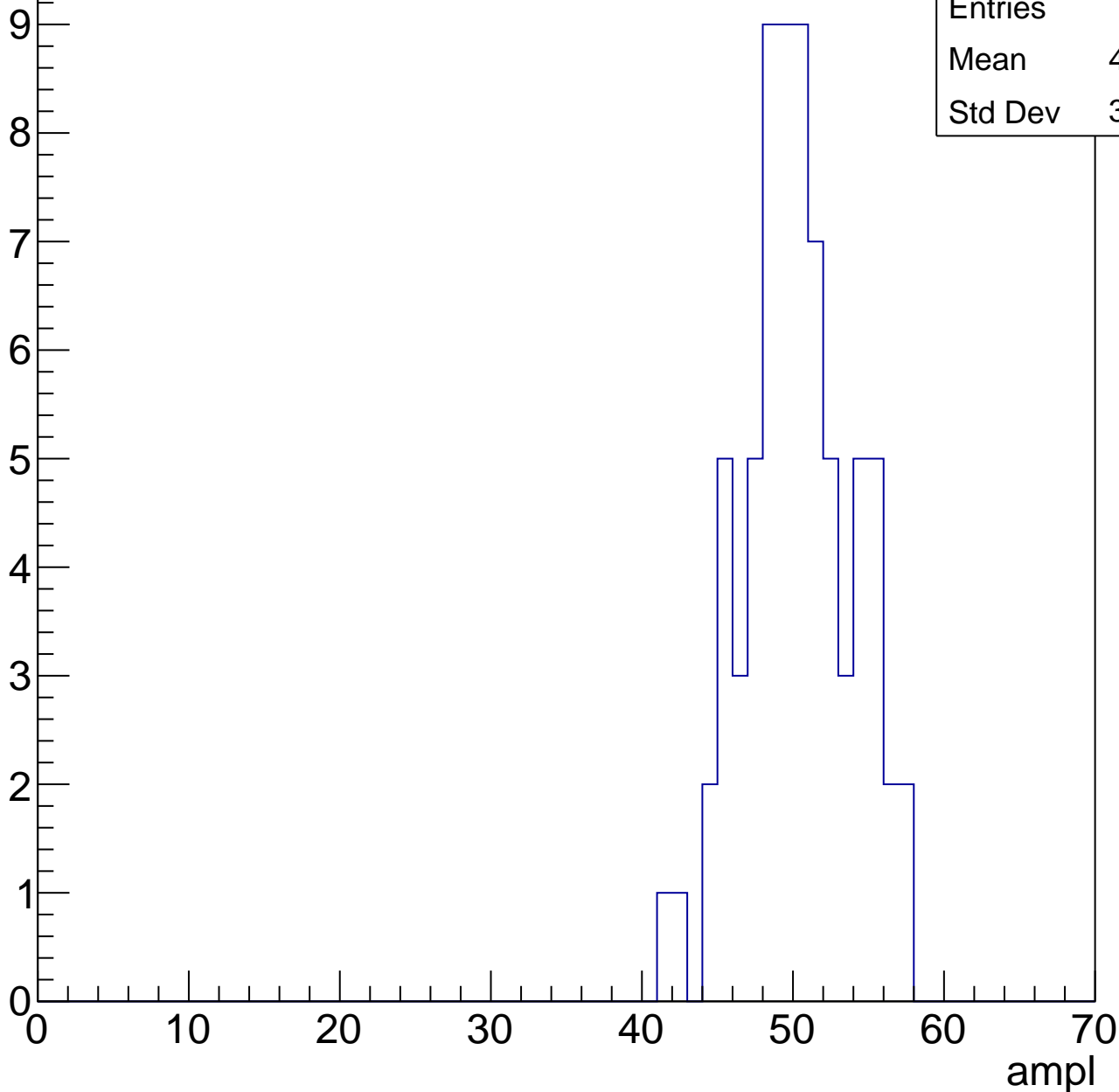


# B1L102S, U21-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	49.85
Std Dev	3.526

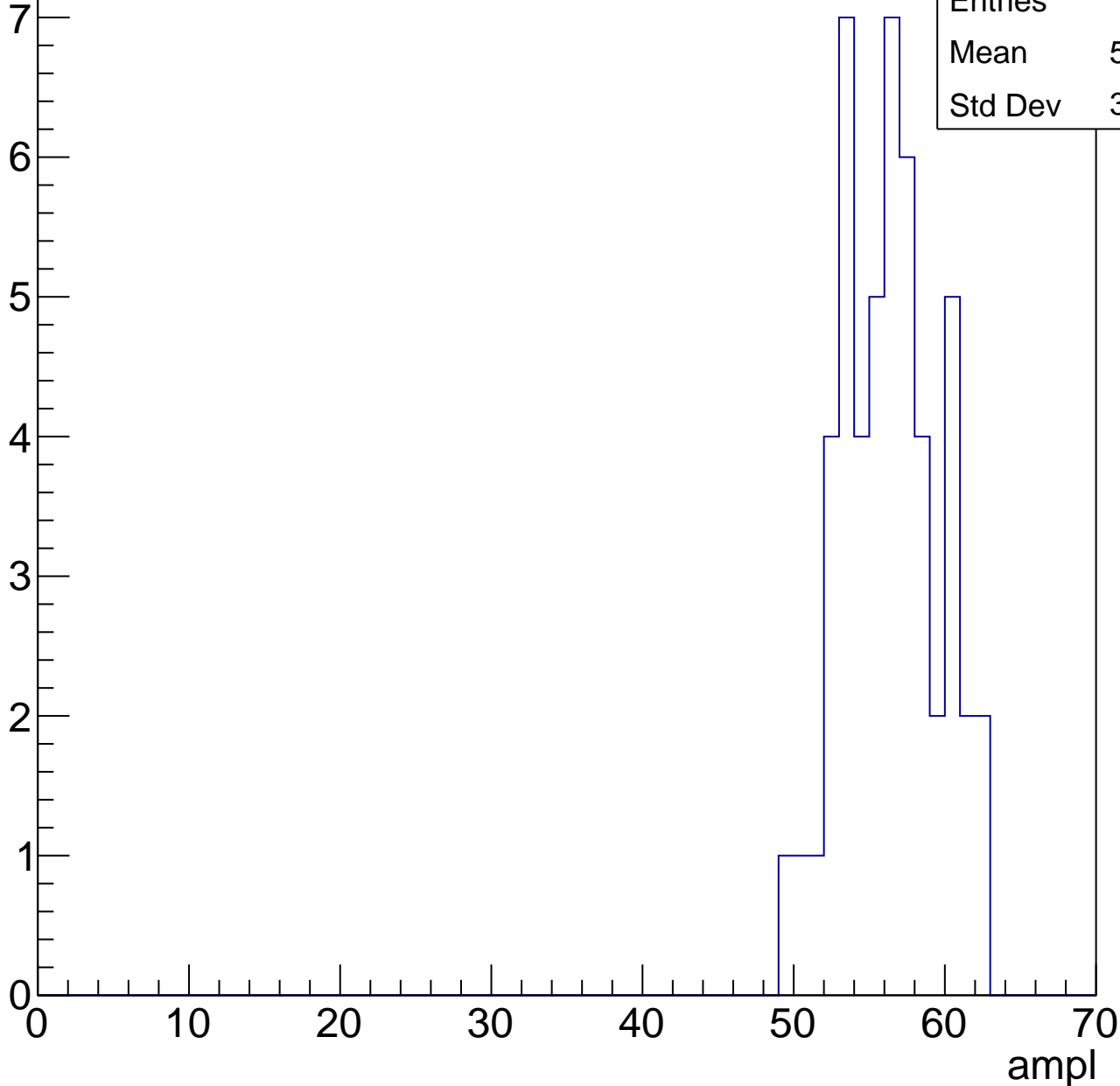


# B1L102S, U21-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

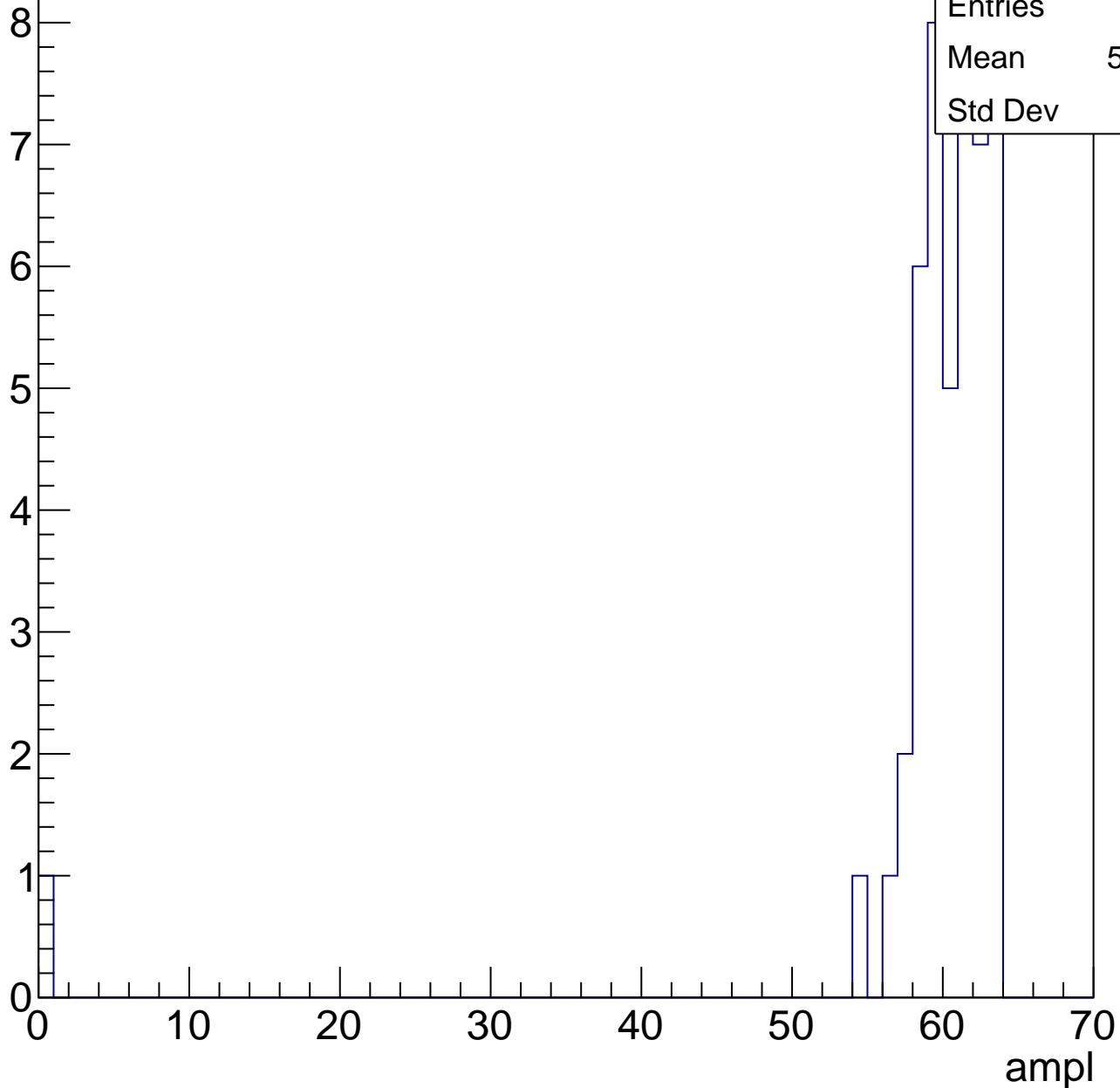
Entries	51
Mean	55.88
Std Dev	3.129



# B1L102S, U21-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch55, adc0

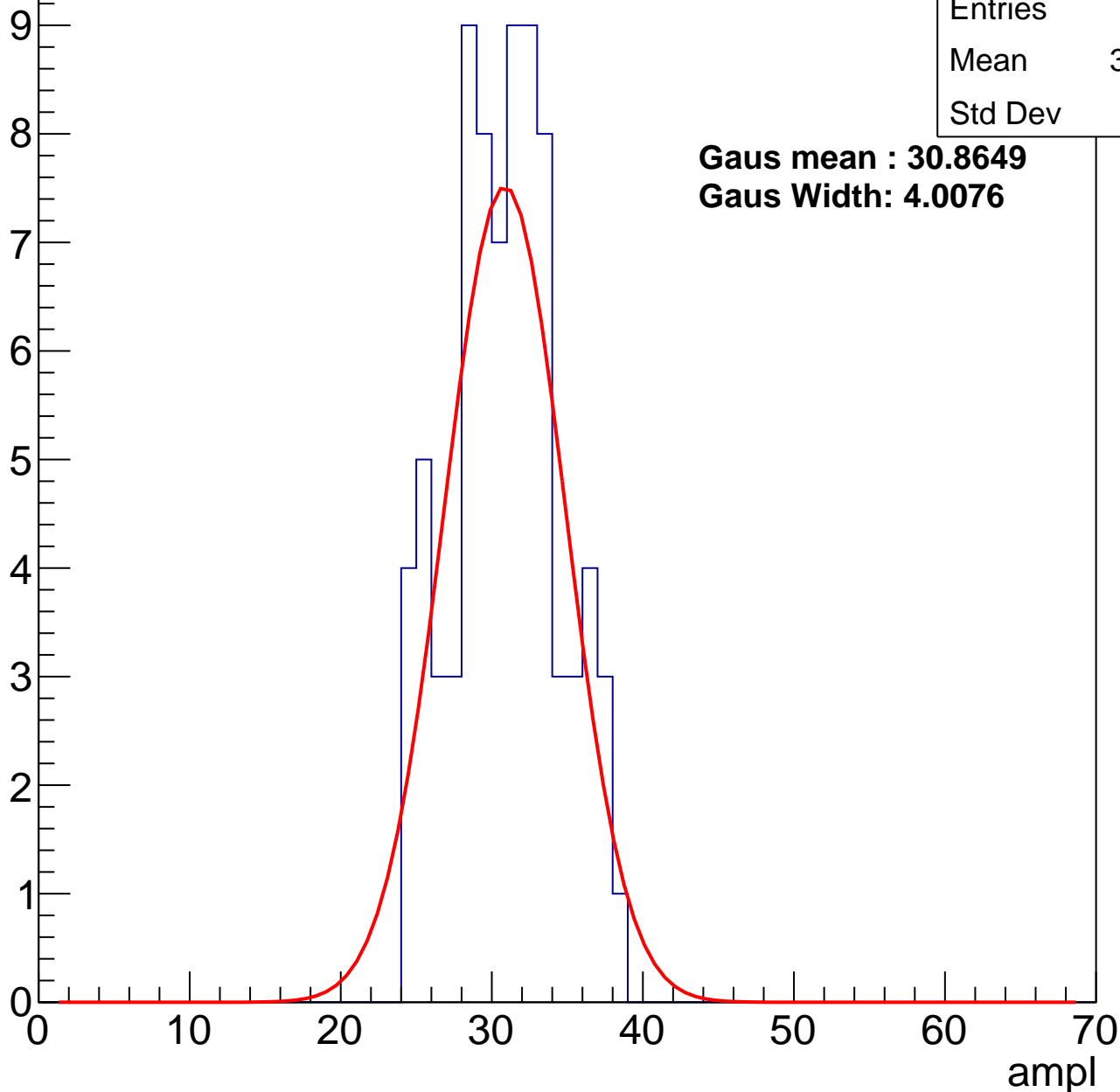
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	30.44
Std Dev	3.5

**Gaus mean : 30.8649**

**Gaus Width: 4.0076**



# B1L102S, U21-ch55, adc1

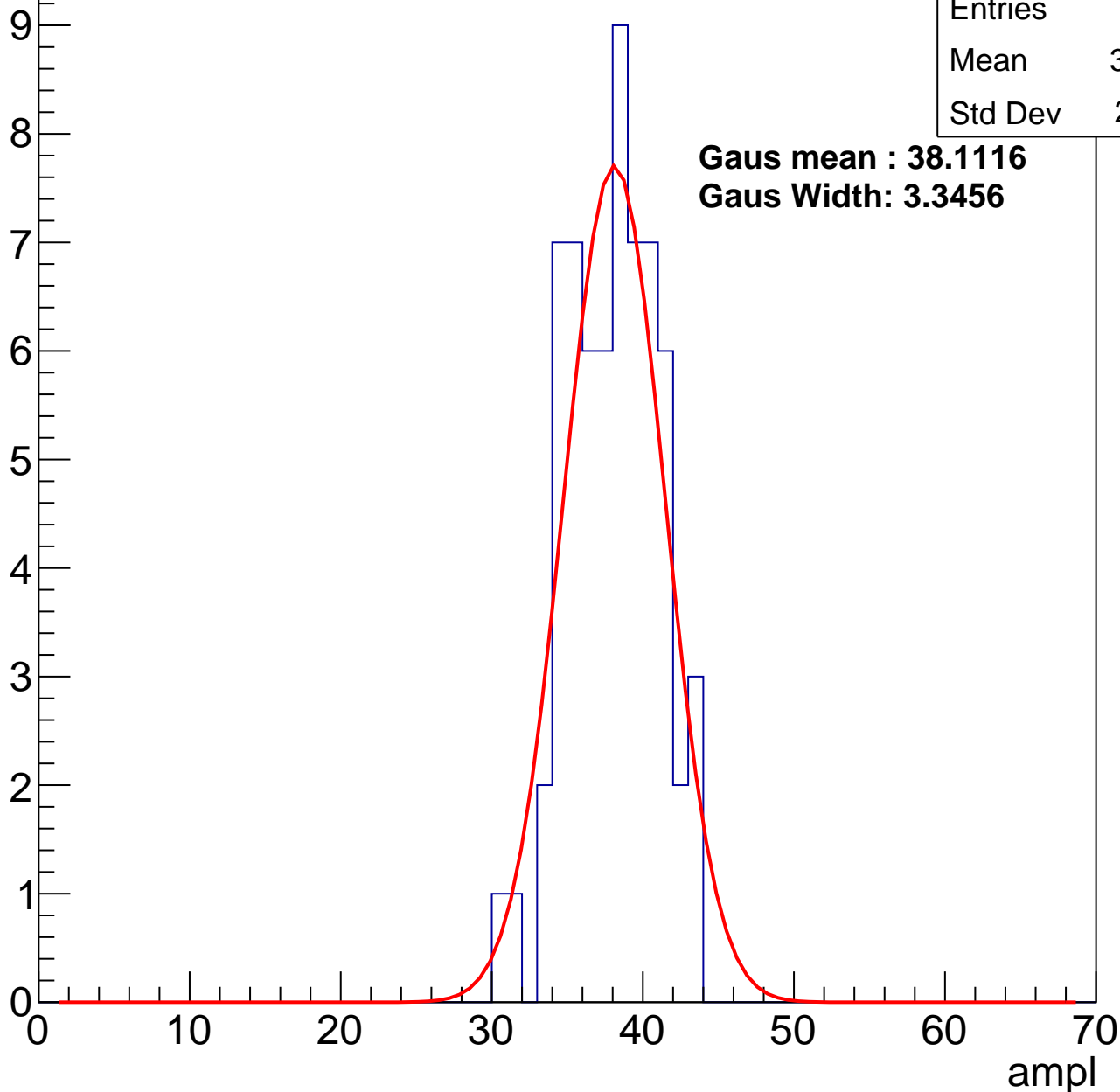
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	37.53
Std Dev	2.931

**Gaus mean : 38.1116**

**Gaus Width: 3.3456**



# B1L102S, U21-ch55, adc2

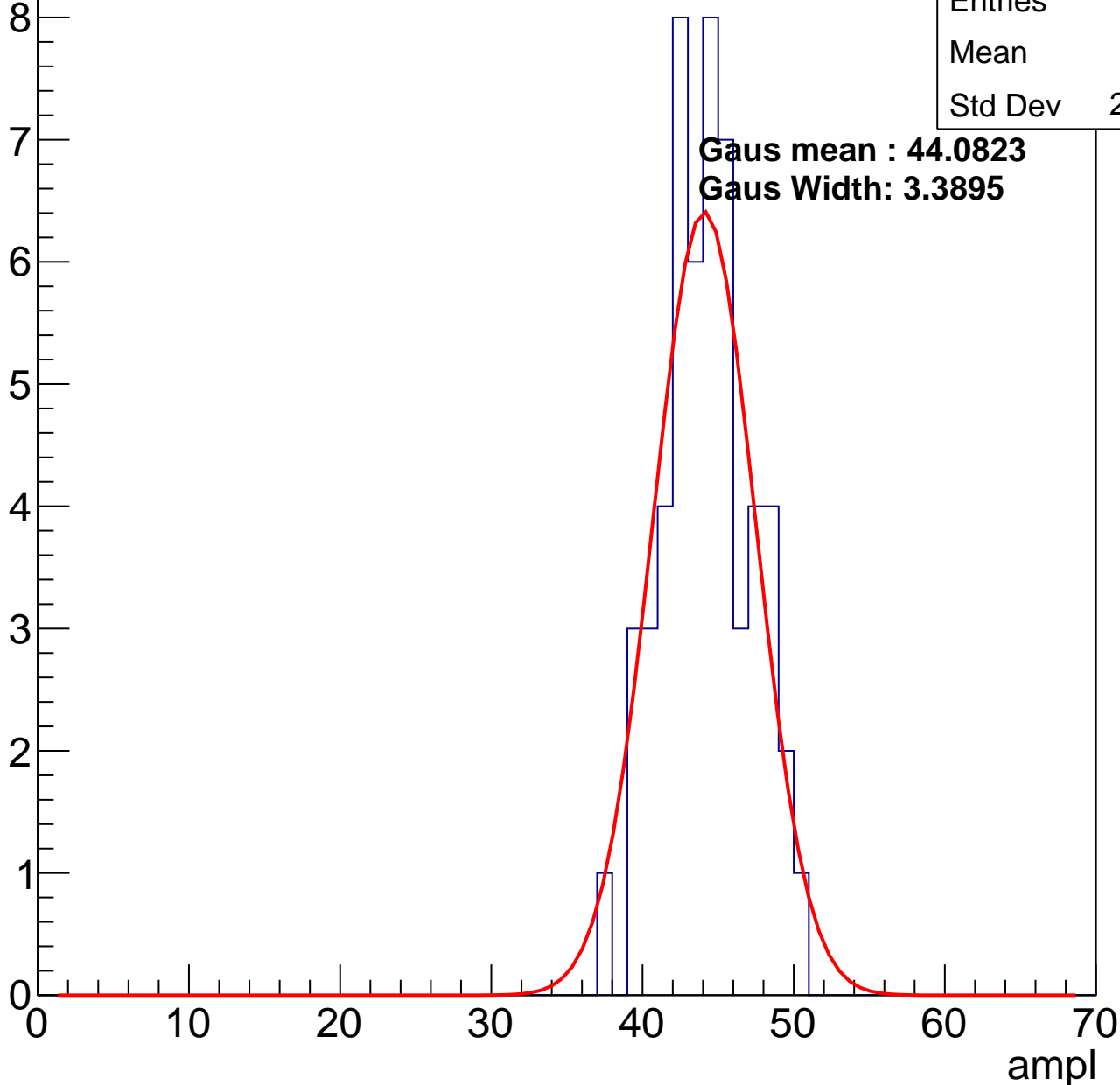
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	43.8
Std Dev	2.883

**Gaus mean : 44.0823**

**Gaus Width: 3.3895**

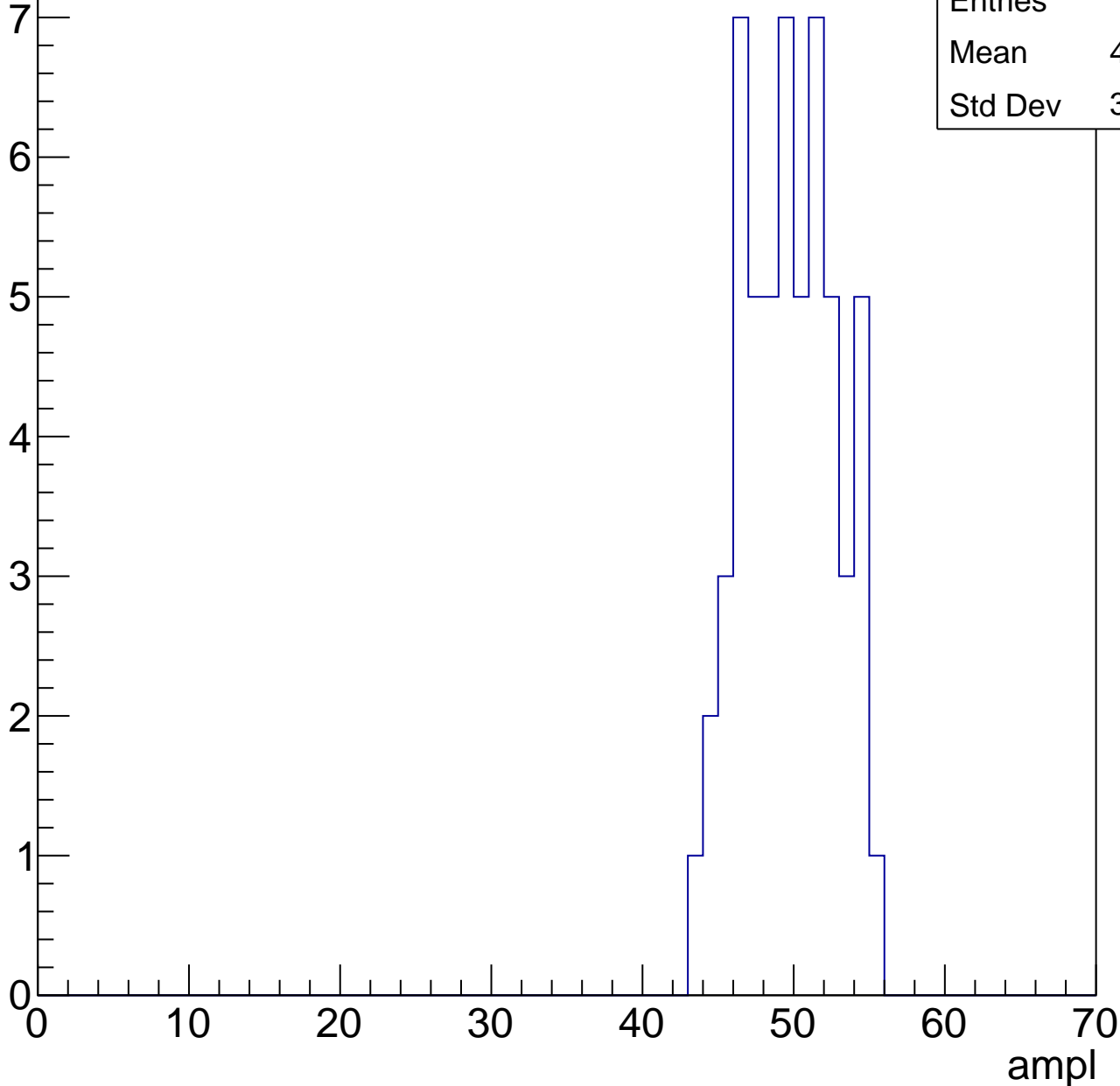


# B1L102S, U21-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	49.23
Std Dev	3.006

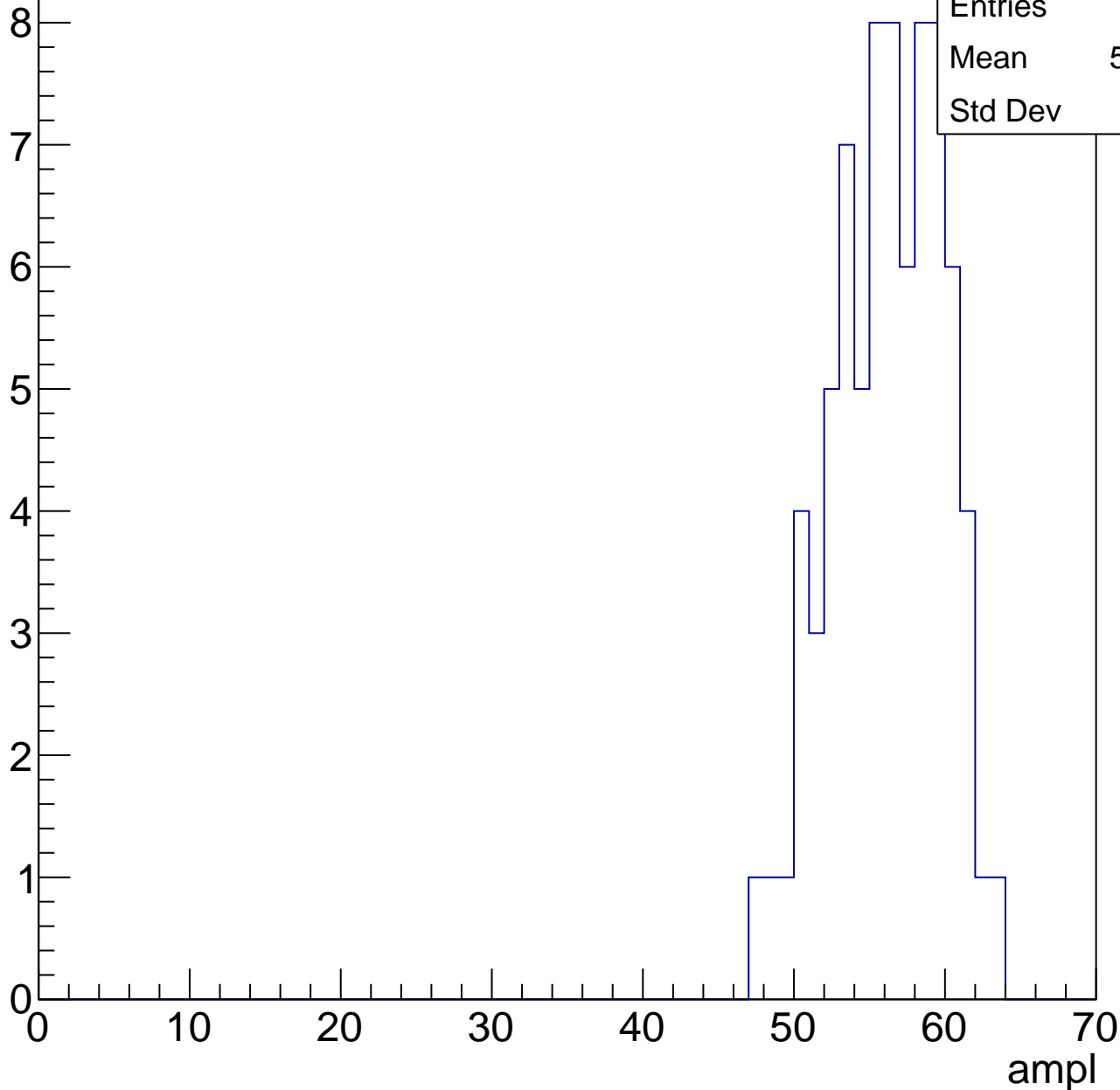


# B1L102S, U21-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	55.75
Std Dev	3.55

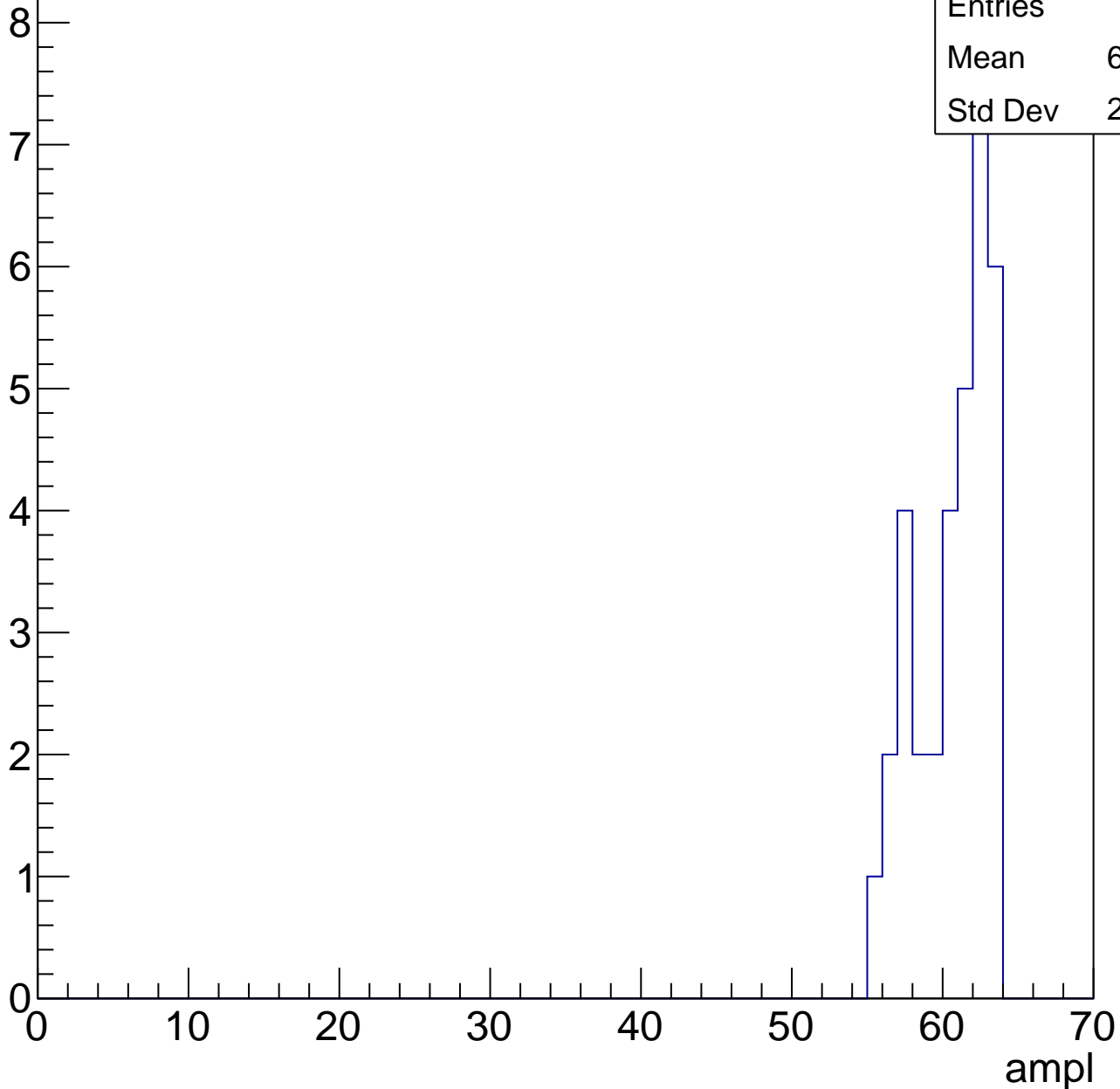


# B1L102S, U21-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

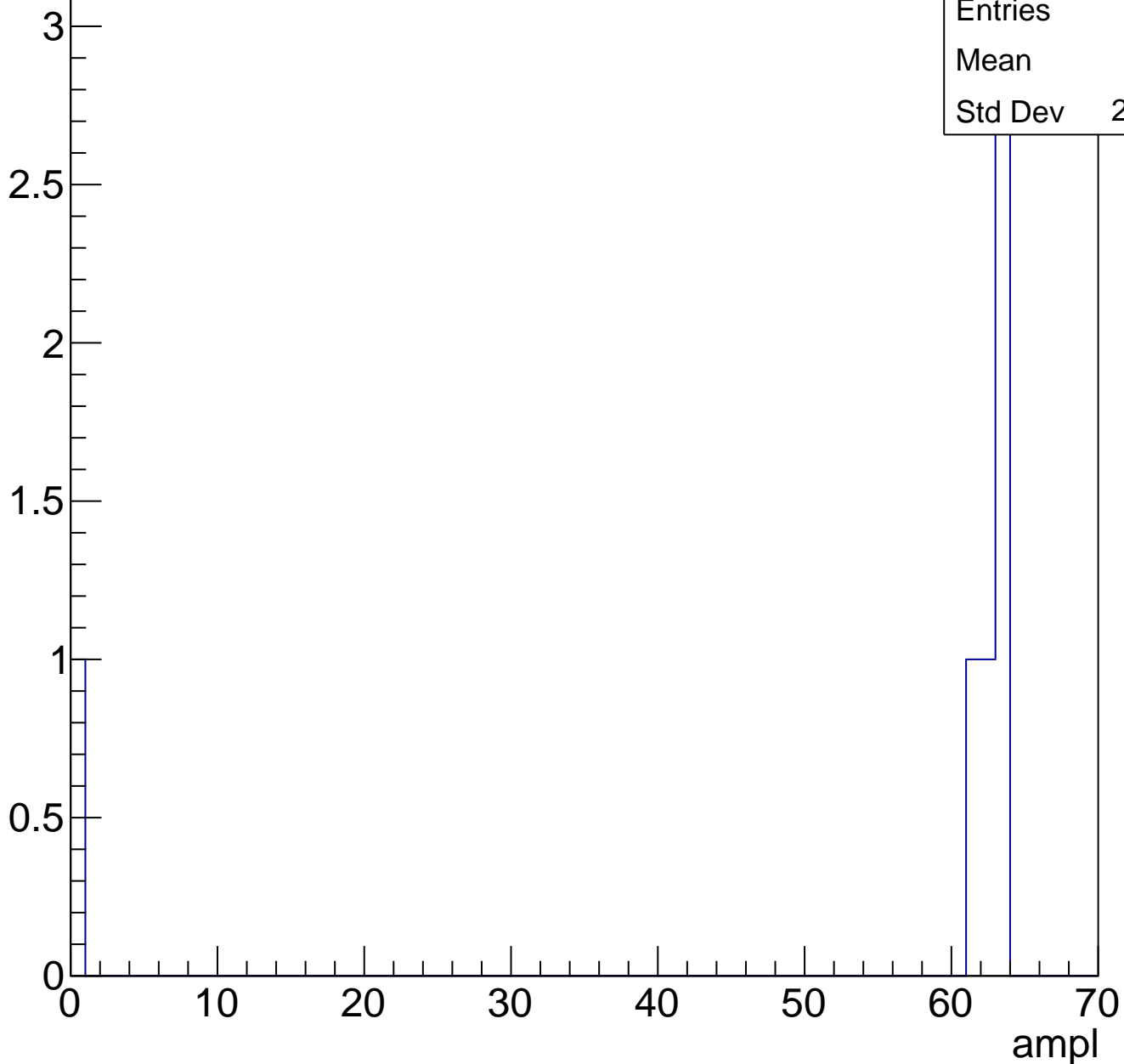
Entries	34
Mean	60.24
Std Dev	2.377



# B1L102S, U21-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	6
Mean	52
Std Dev	23.27



# B1L102S, U21-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U21-ch56, adc0

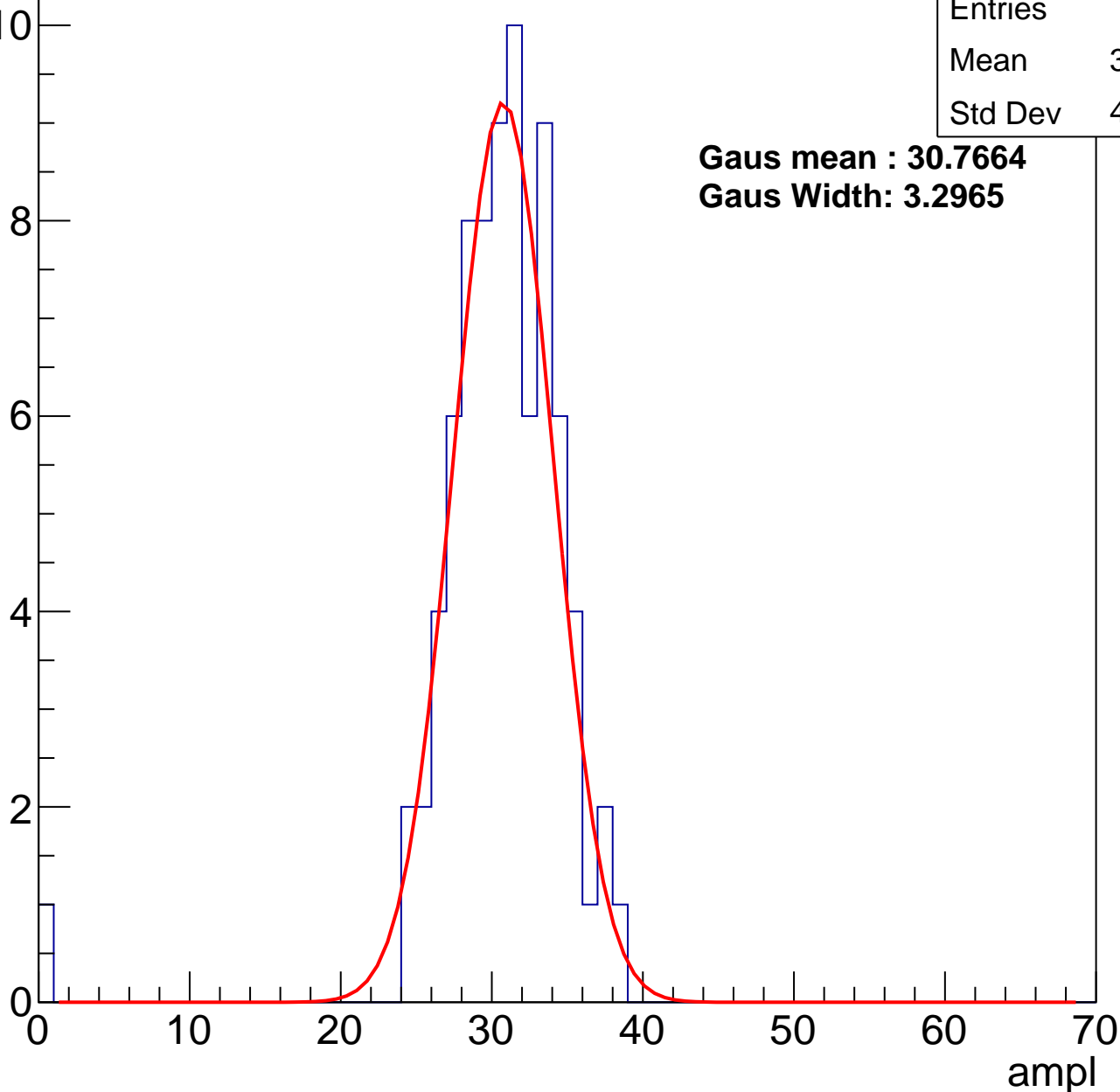
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	30.14
Std Dev	4.622

**Gaus mean : 30.7664**

**Gaus Width: 3.2965**



# B1L102S, U21-ch56, adc1

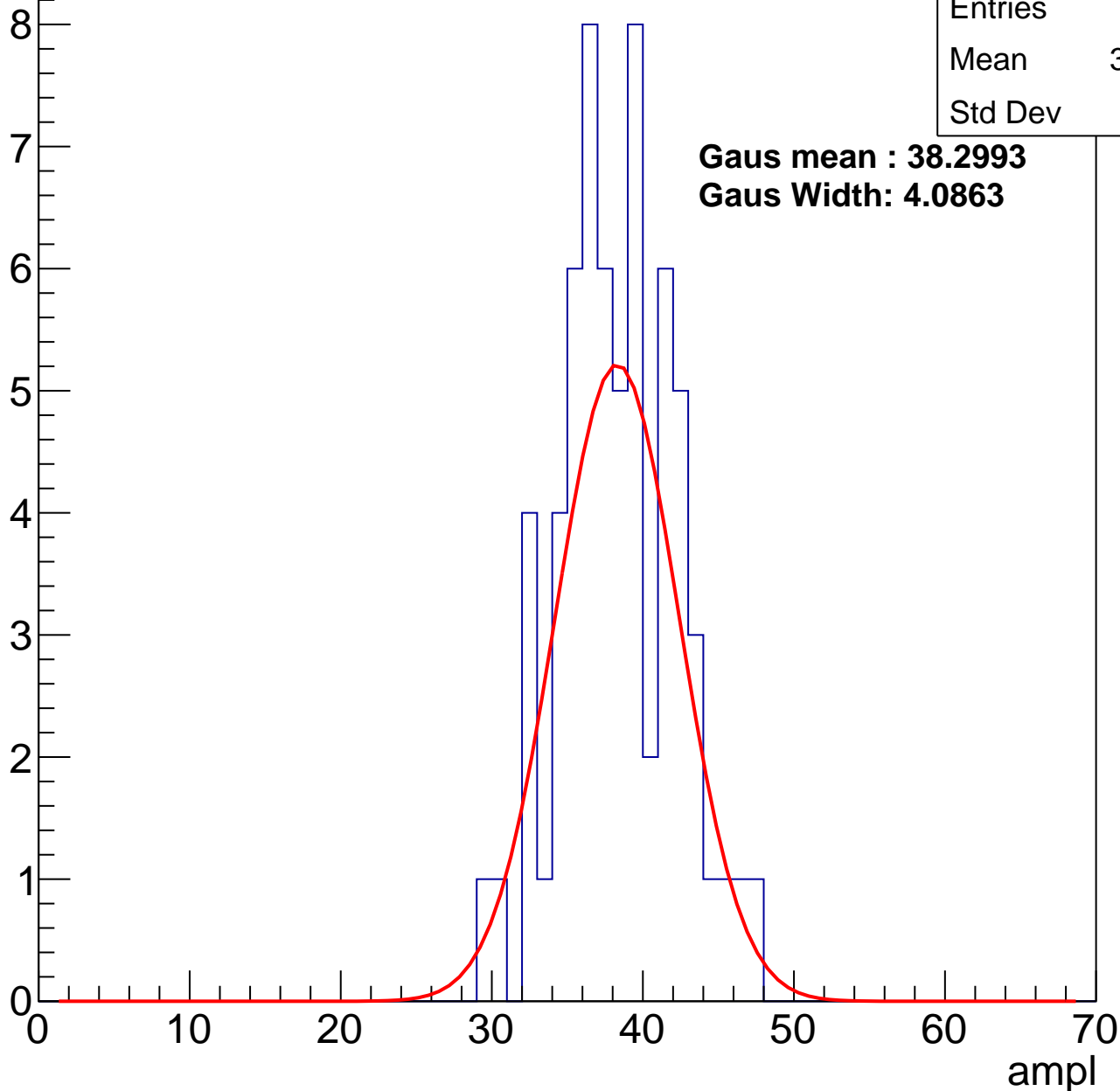
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	37.89
Std Dev	3.8

**Gaus mean : 38.2993**

**Gaus Width: 4.0863**



# B1L102S, U21-ch56, adc2

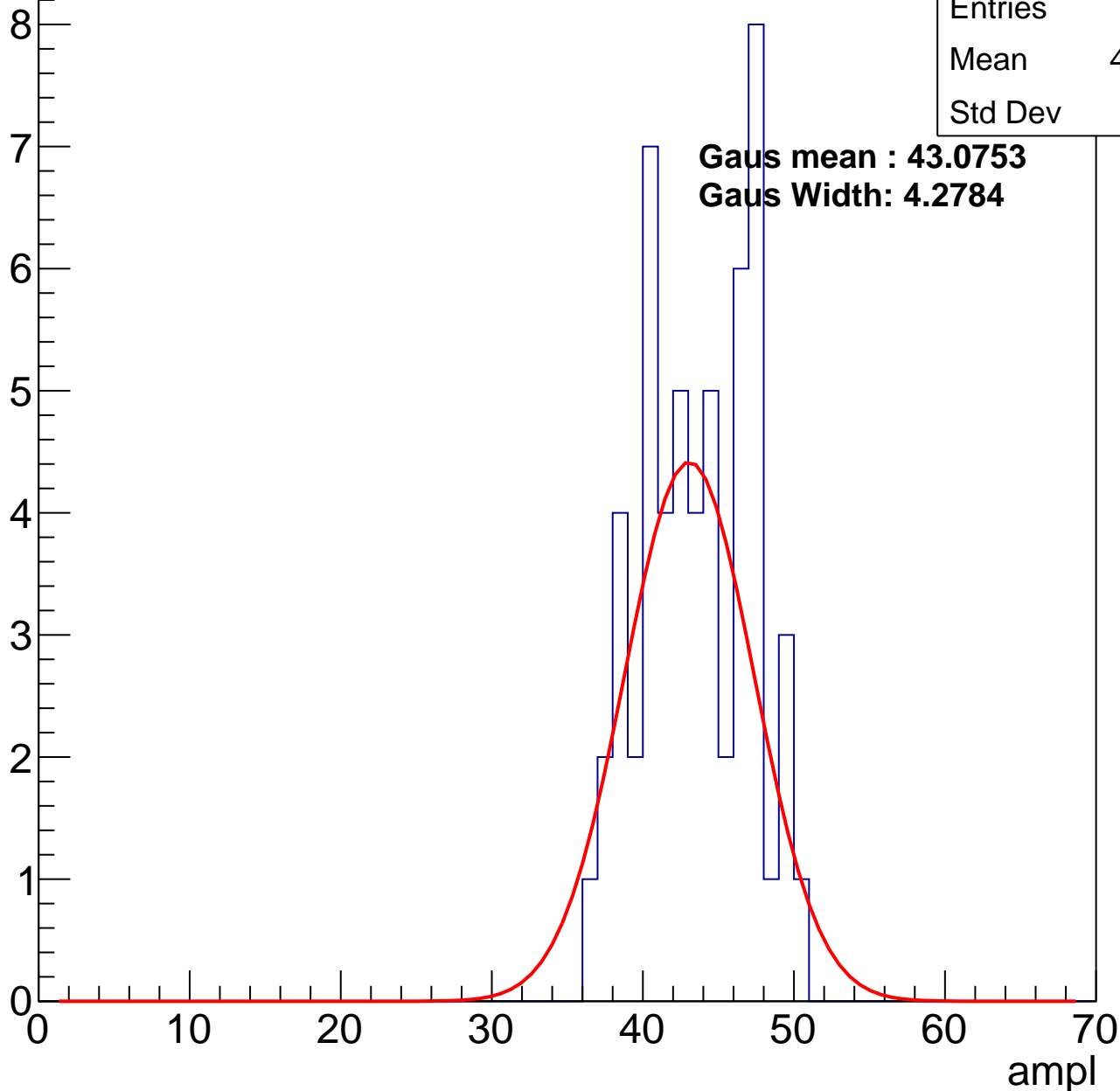
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	43.15
Std Dev	3.6

**Gaus mean : 43.0753**

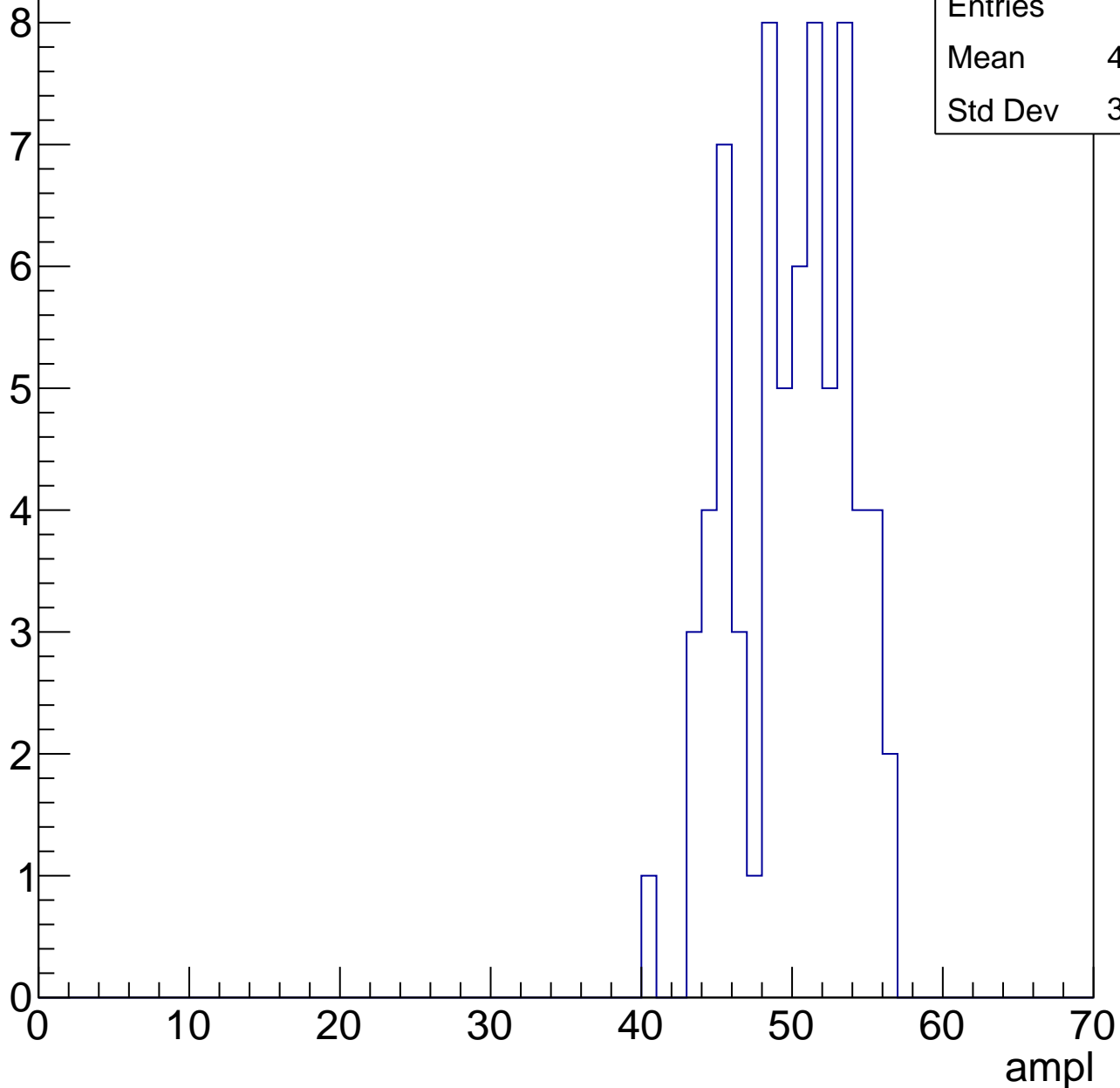
**Gaus Width: 4.2784**



# B1L102S, U21-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

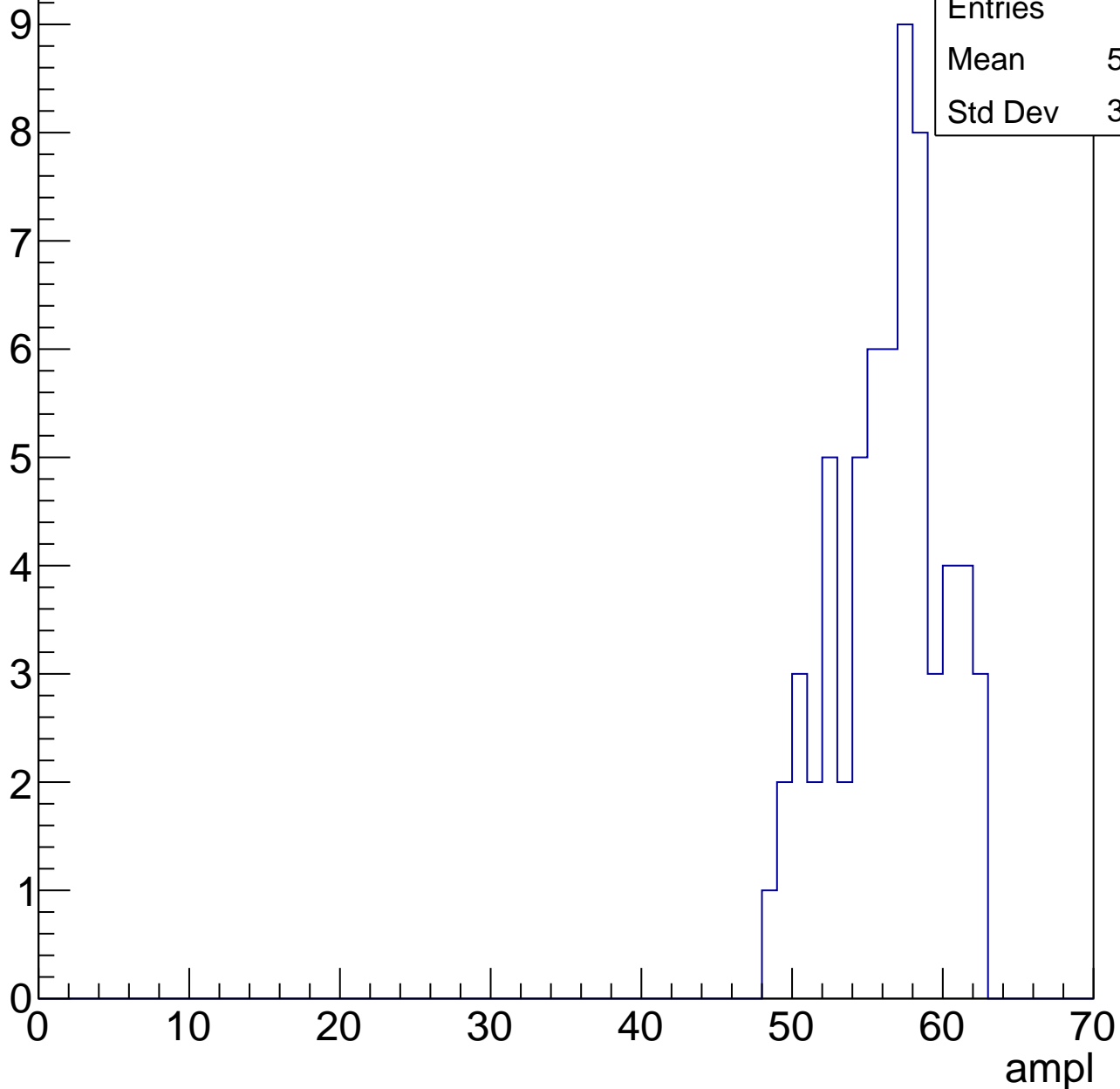
Entry



# B1L102S, U21-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



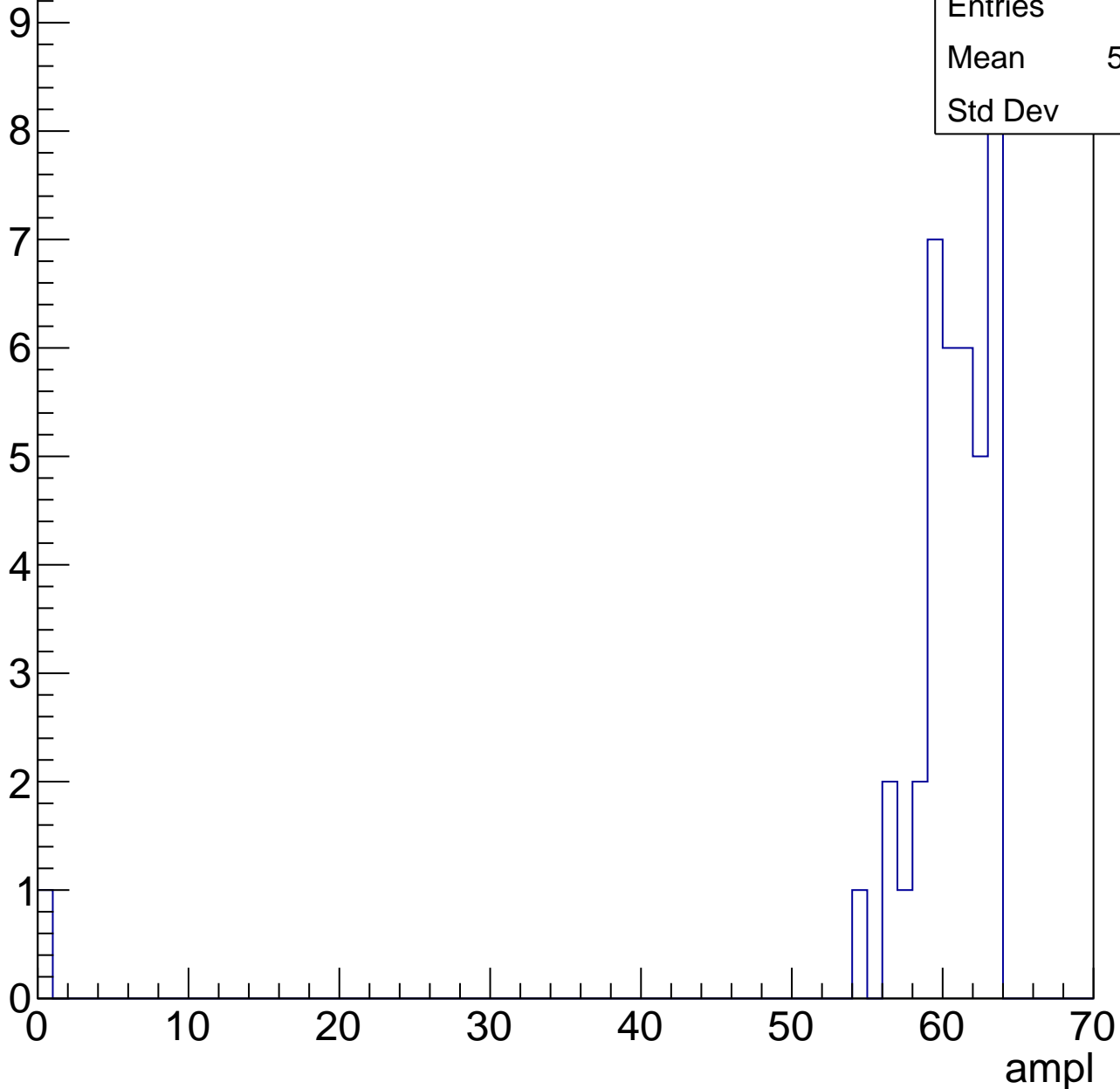
Entries	63
Mean	55.94
Std Dev	3.527

# B1L102S, U21-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	58.88
Std Dev	9.68



# B1L102S, U21-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U21-ch57, adc0

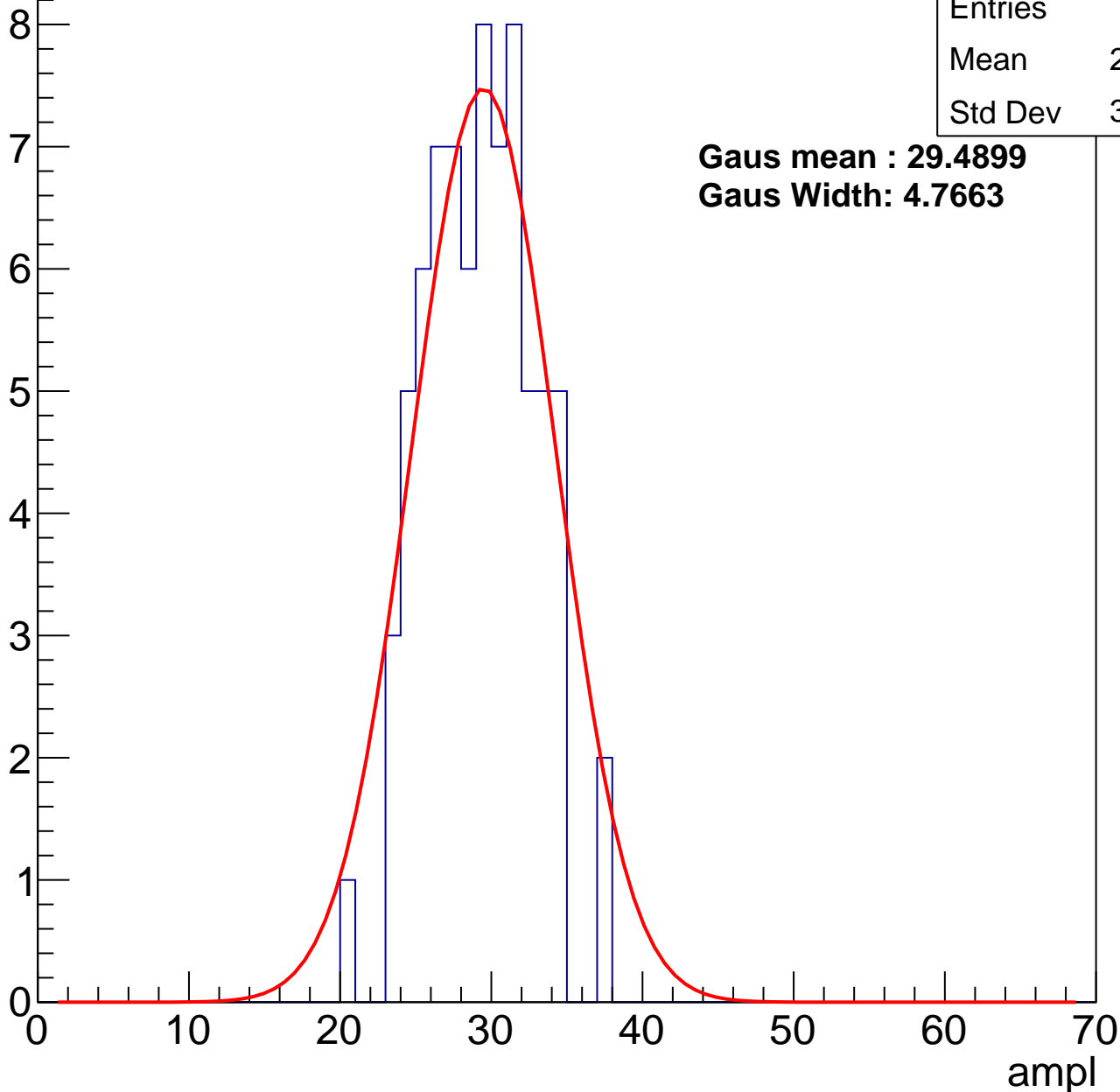
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	28.76
Std Dev	3.502

**Gaus mean : 29.4899**

**Gaus Width: 4.7663**



# B1L102S, U21-ch57, adc1

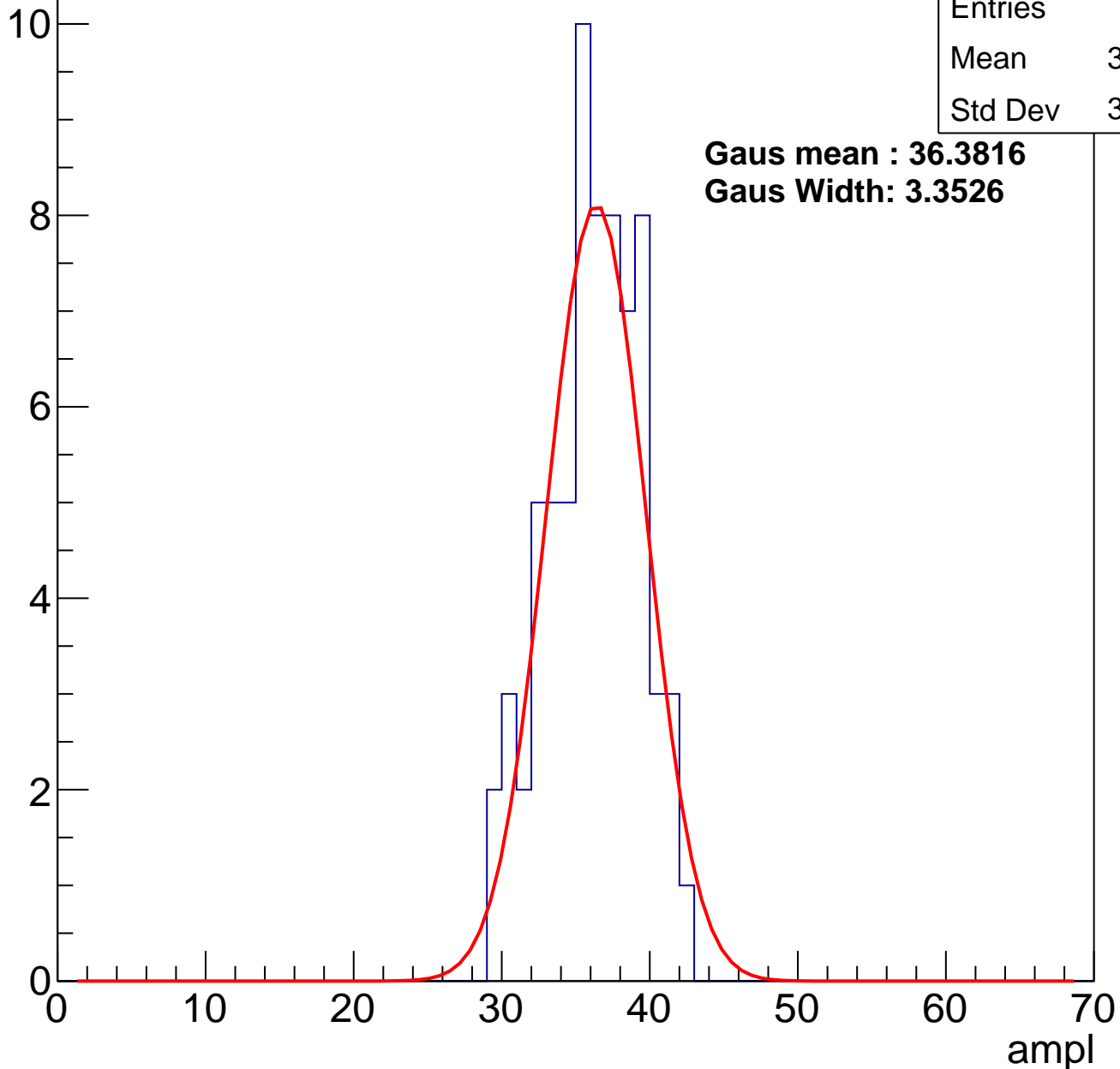
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	70
Mean	35.74
Std Dev	3.102

**Gaus mean : 36.3816**

**Gaus Width: 3.3526**

Entry



# B1L102S, U21-ch57, adc2

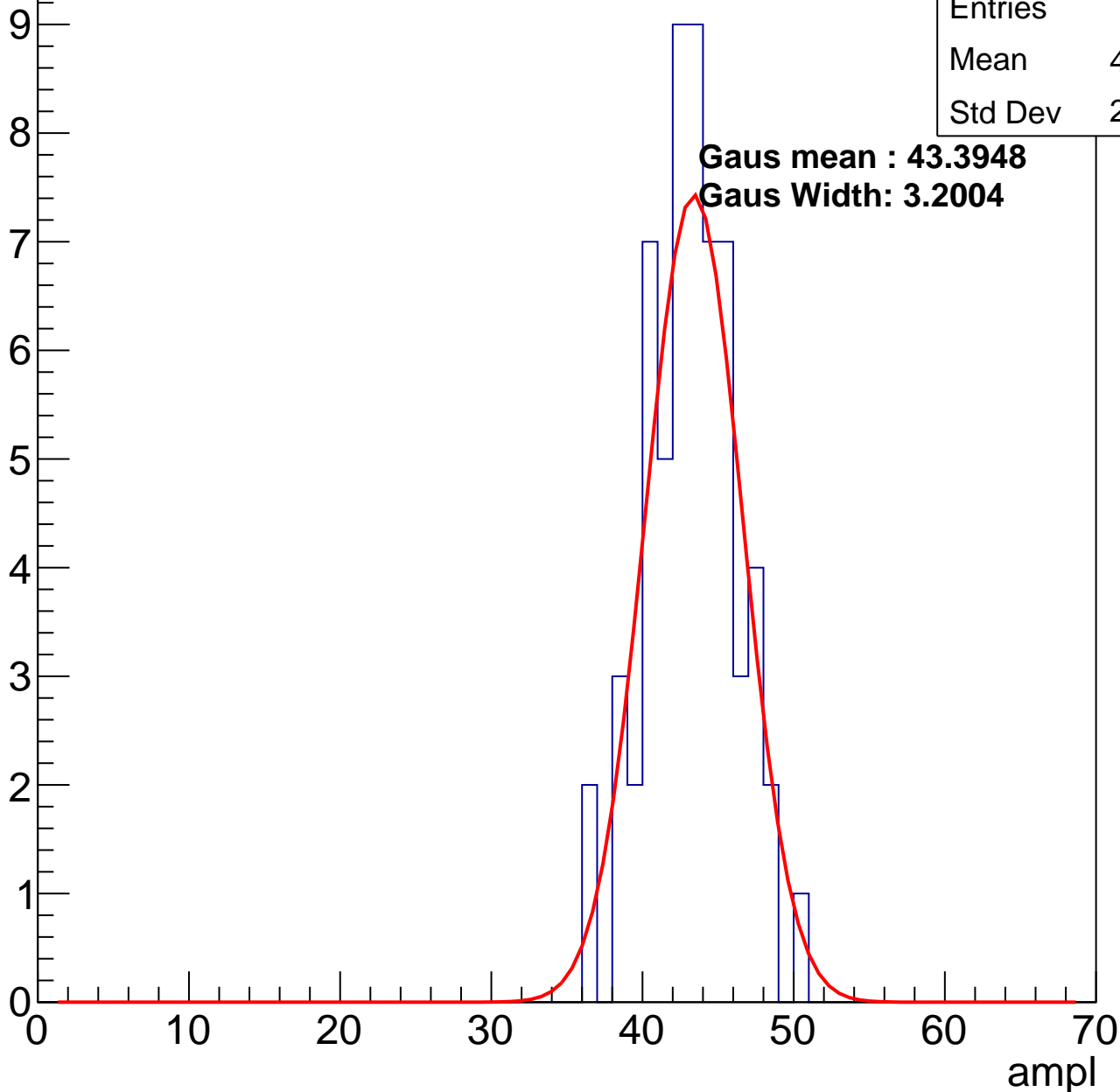
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	42.77
Std Dev	2.916

**Gaus mean : 43.3948**

**Gaus Width: 3.2004**



# B1L102S, U21-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	73
Mean	49.26
Std Dev	3.38

Entry

10

8

6

4

2

0

0

10

20

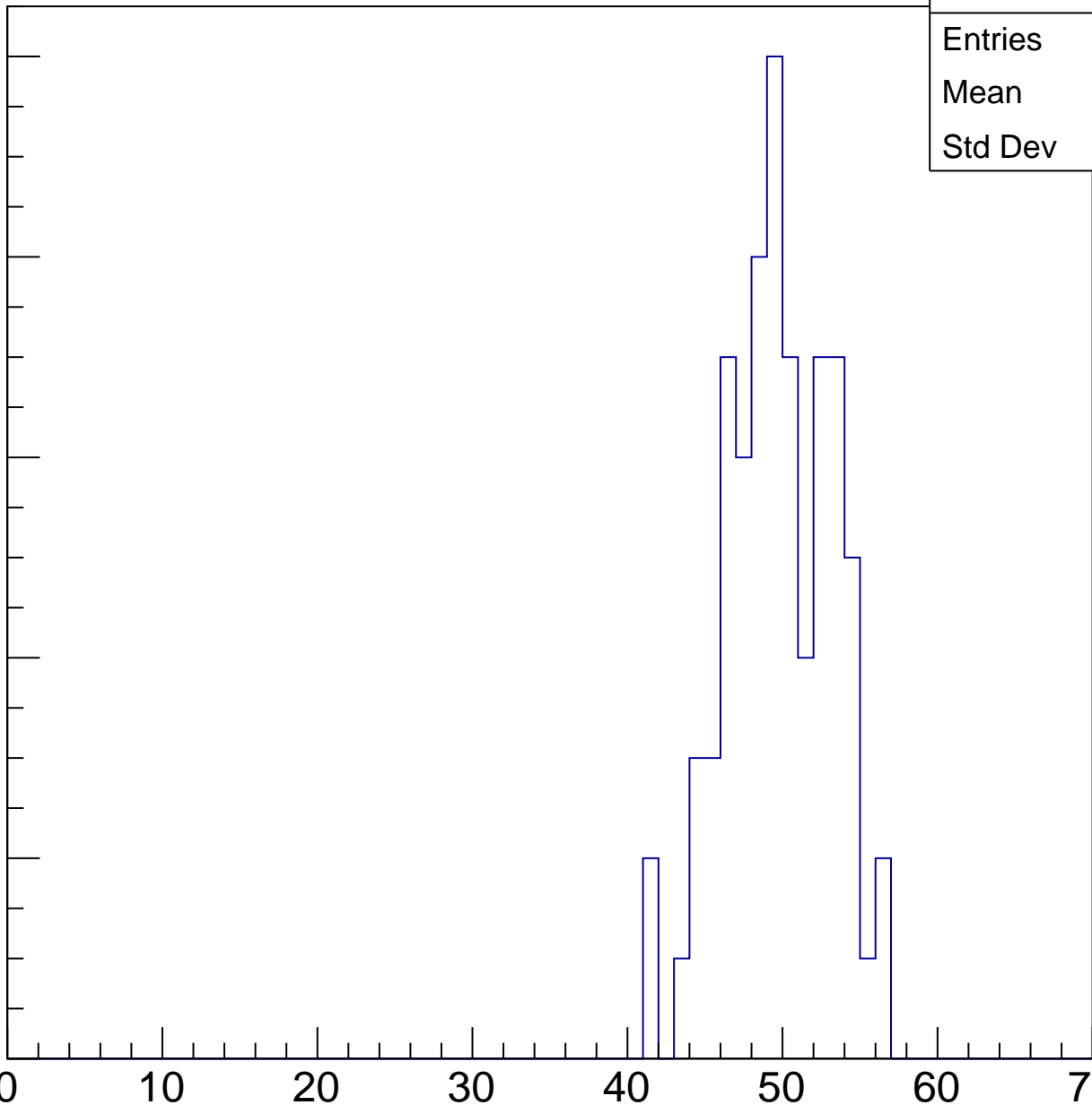
30

40

50

60

ampl

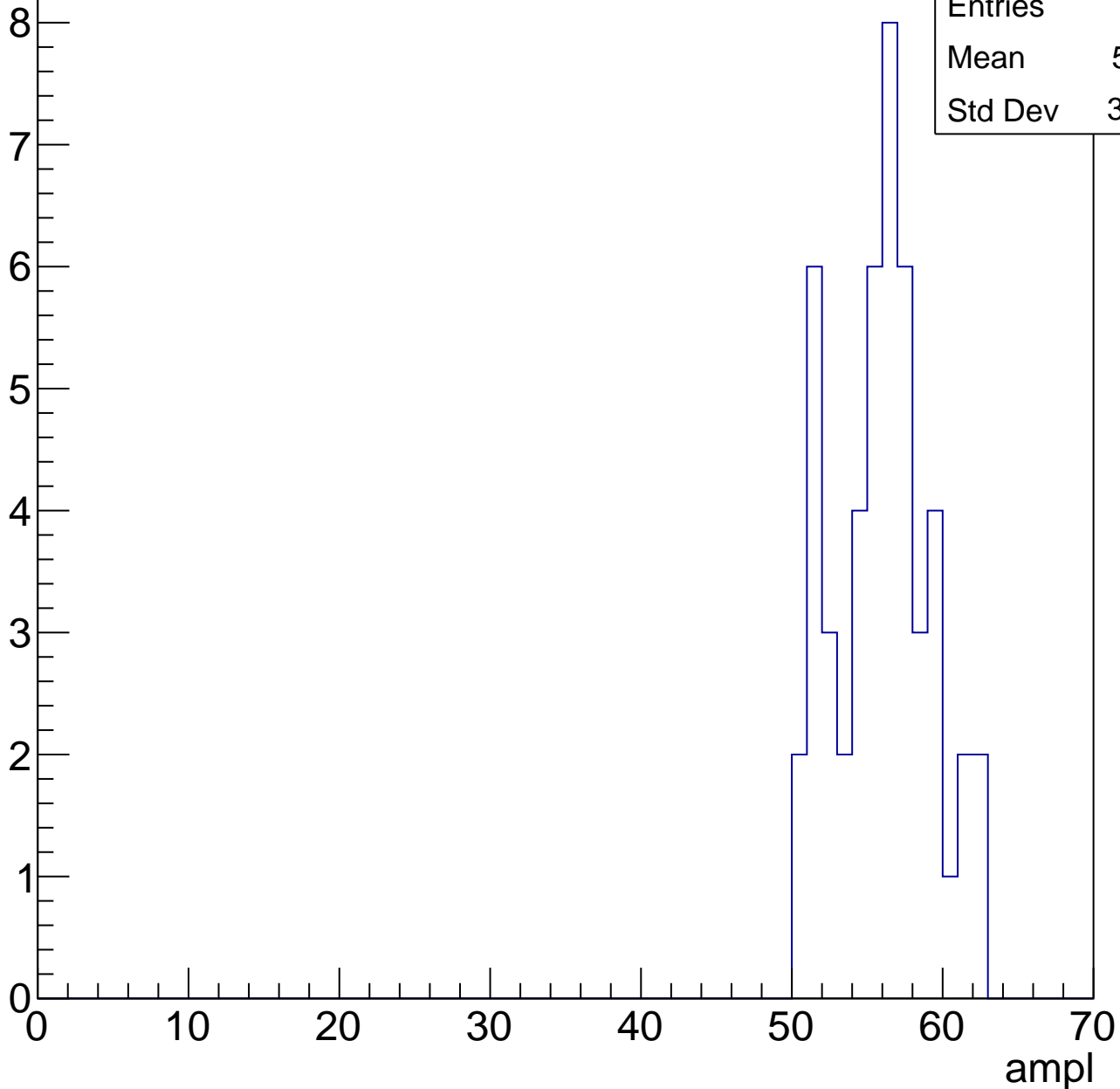


# B1L102S, U21-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	55.51
Std Dev	3.163

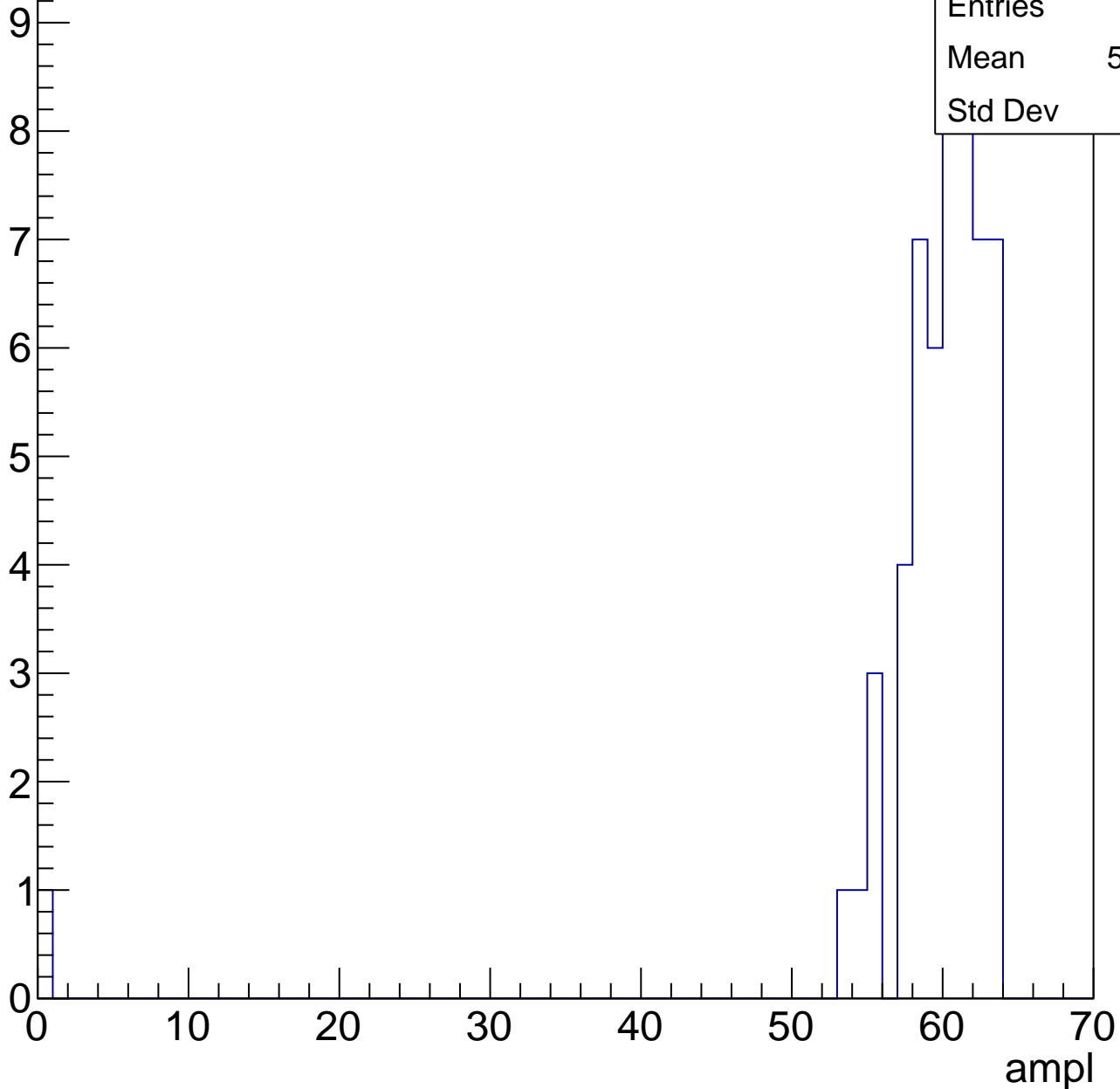


# B1L102S, U21-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	58.57
Std Dev	8.41



# B1L102S, U21-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U21-ch58, adc0

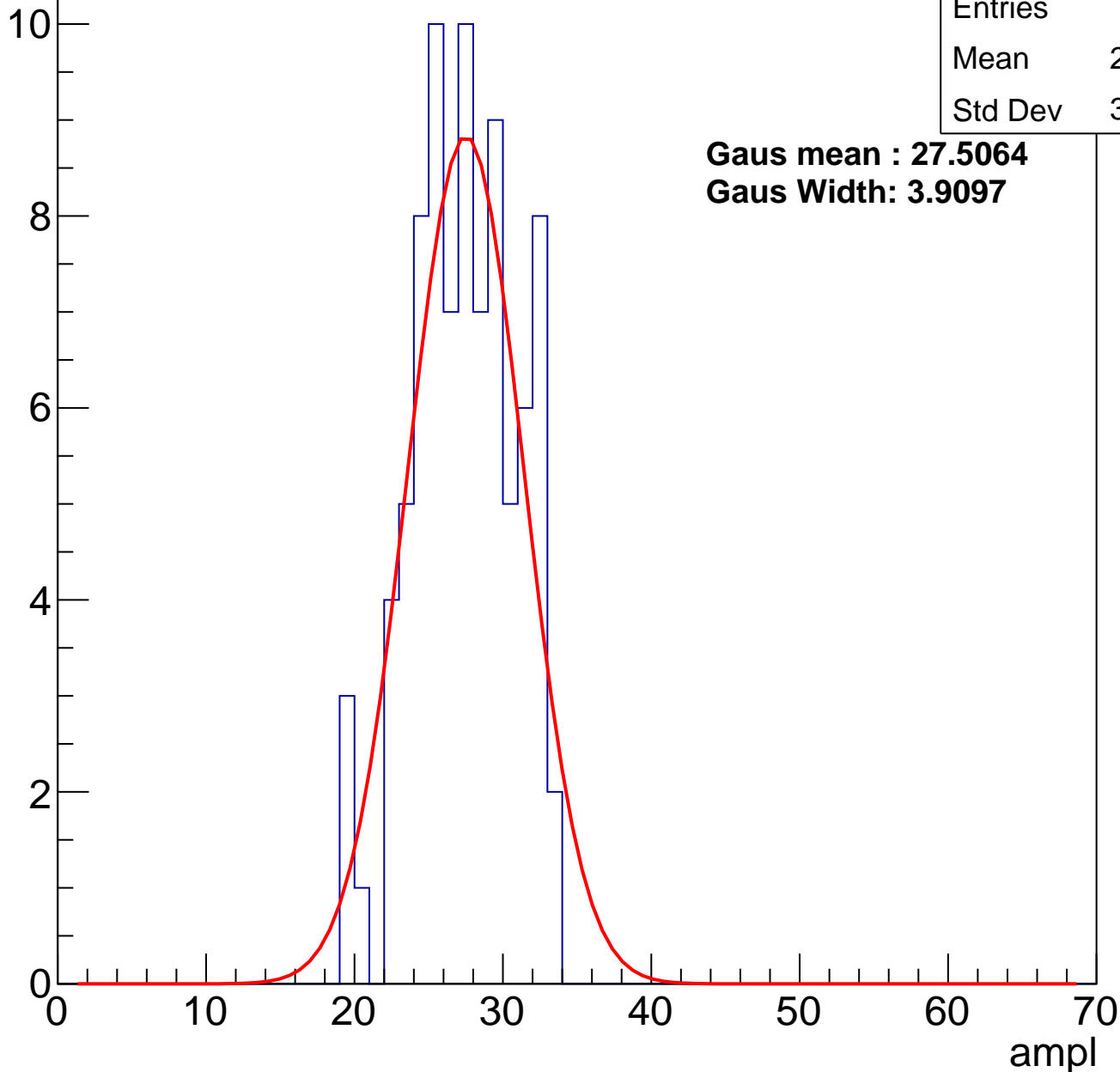
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	85
Mean	26.93
Std Dev	3.422

**Gaus mean : 27.5064**

**Gaus Width: 3.9097**

Entry



# B1L102S, U21-ch58, adc1

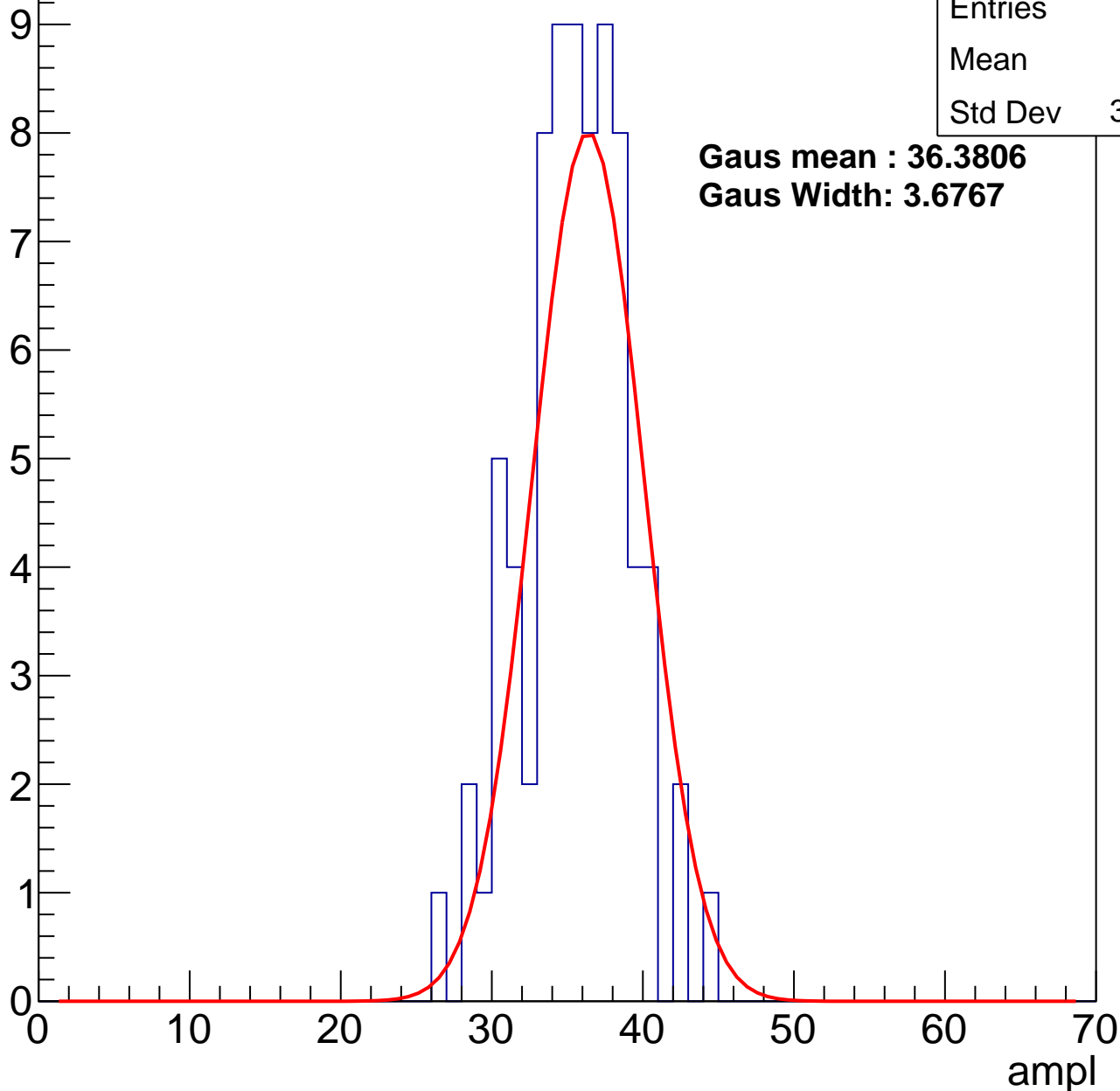
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	35.1
Std Dev	3.459

**Gaus mean : 36.3806**

**Gaus Width: 3.6767**



# B1L102S, U21-ch58, adc2

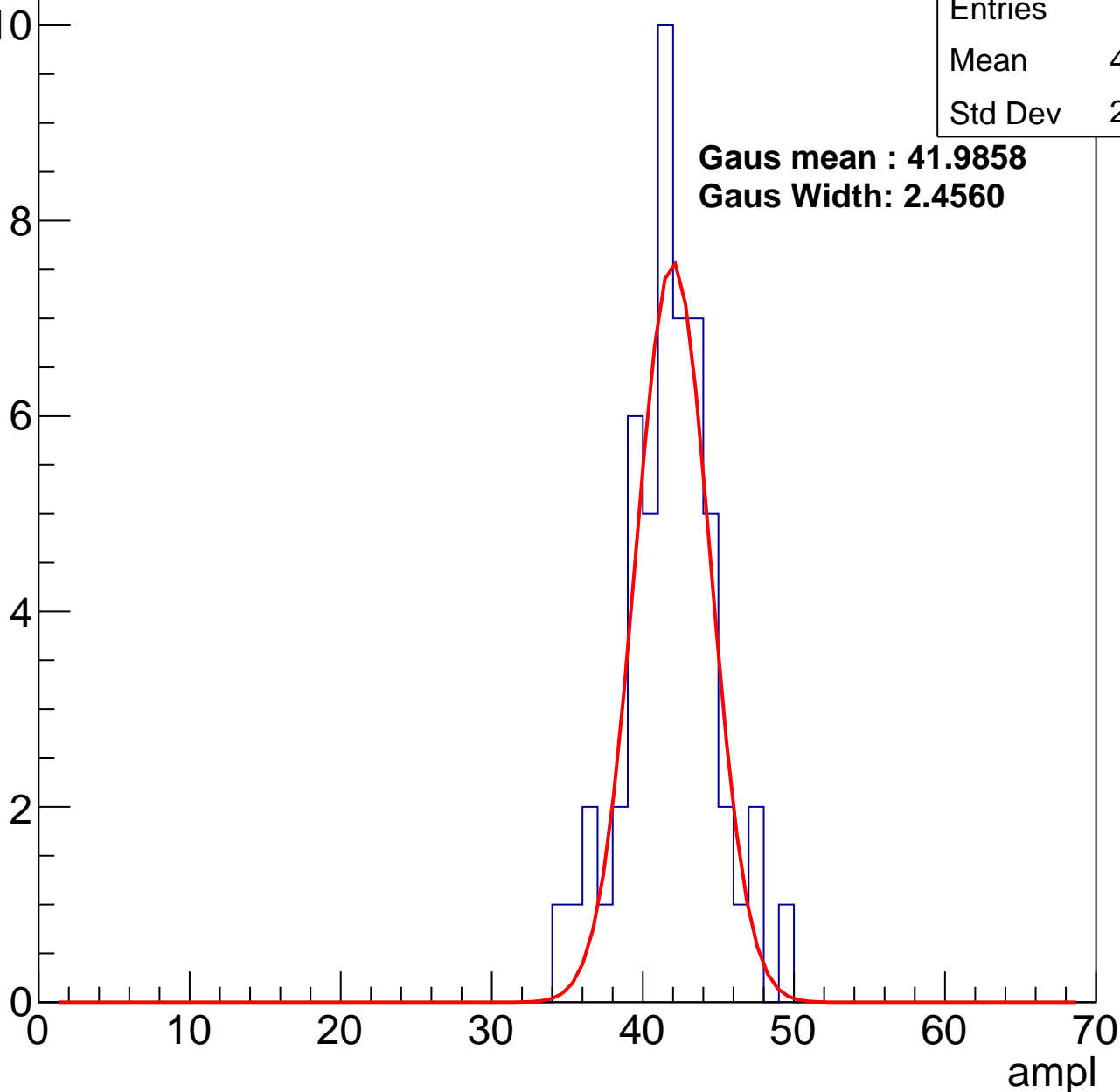
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	41.36
Std Dev	2.959

**Gaus mean : 41.9858**

**Gaus Width: 2.4560**

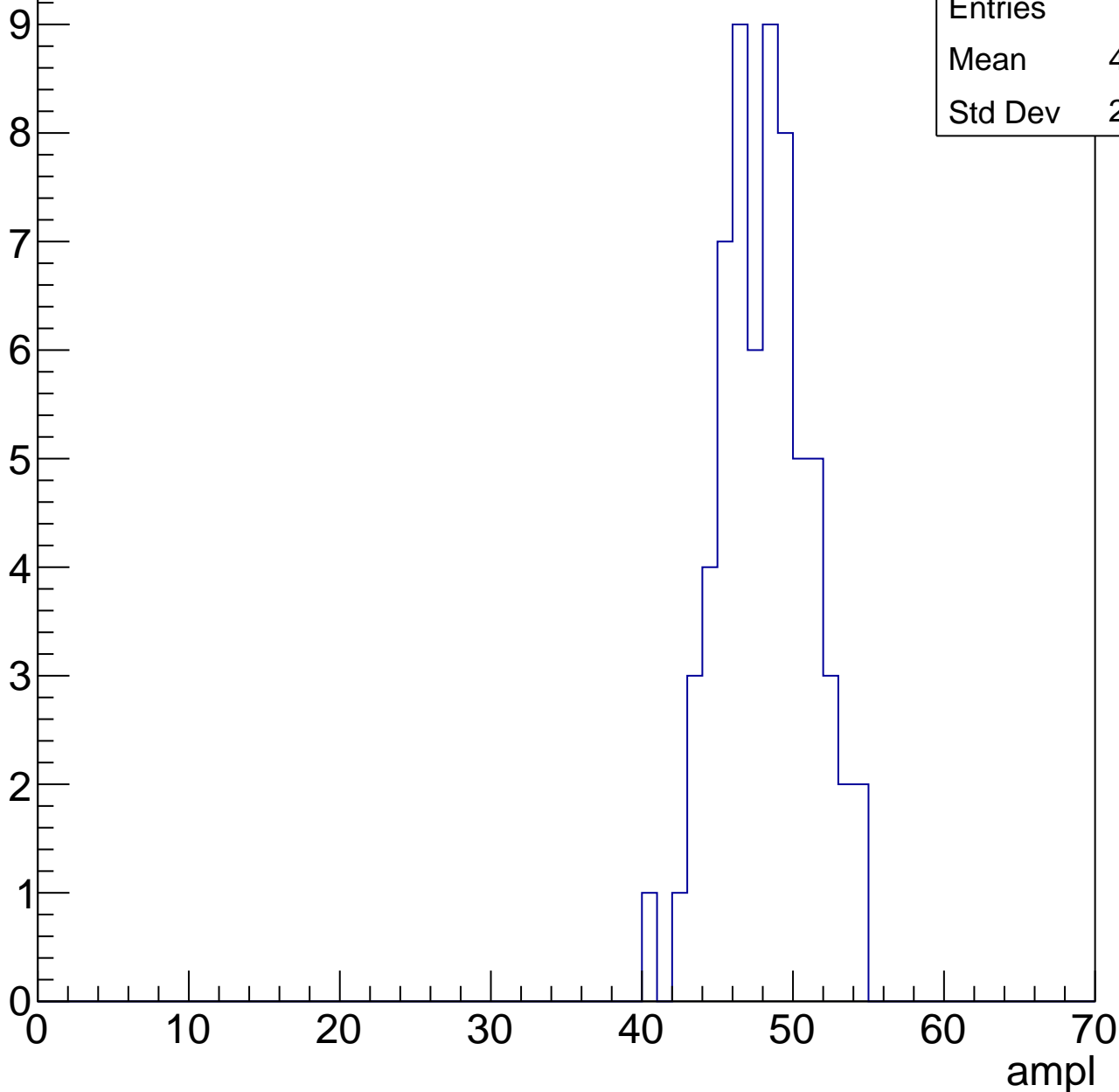


# B1L102S, U21-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	47.65
Std Dev	2.984

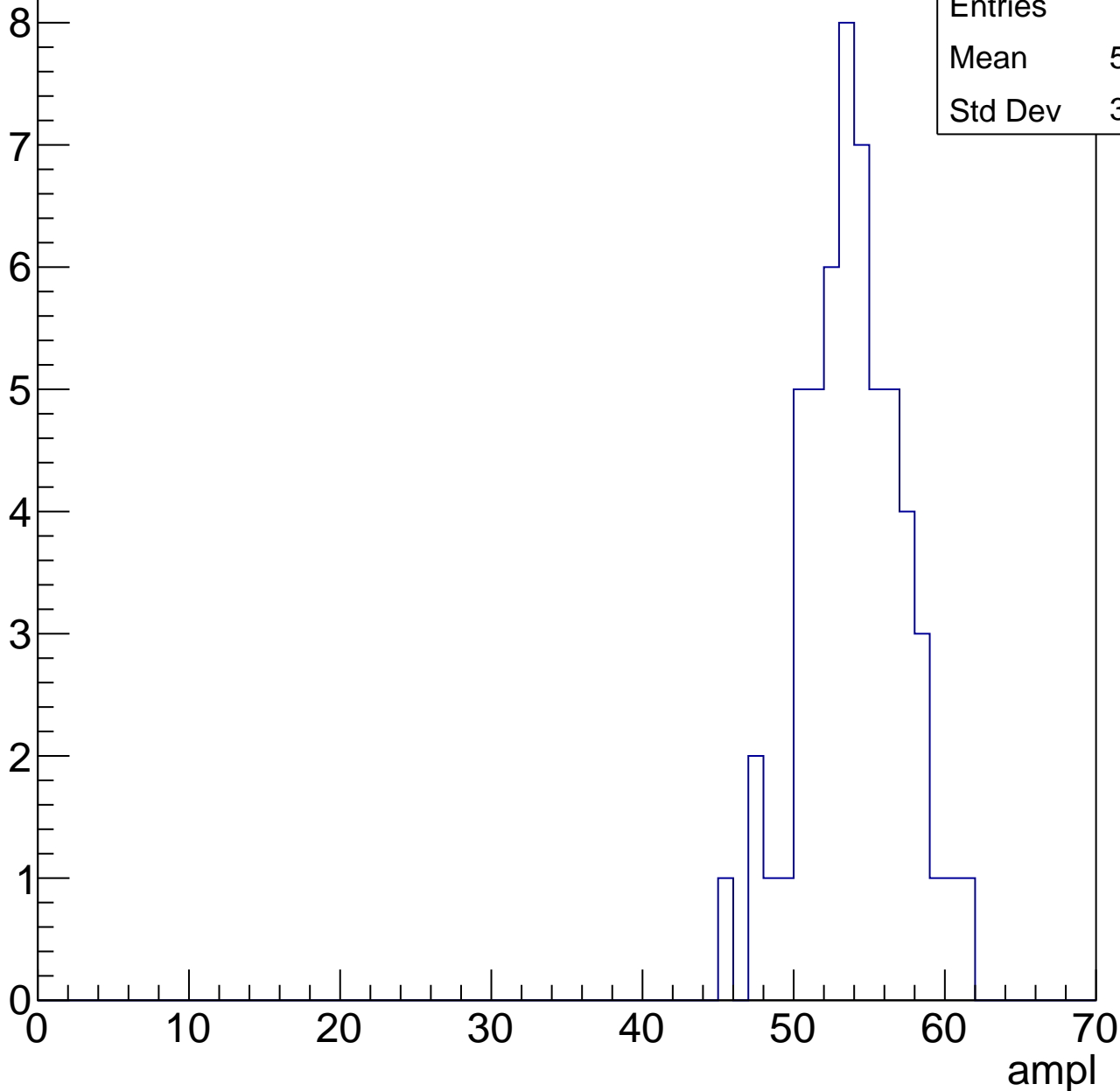


# B1L102S, U21-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	53.43
Std Dev	3.267

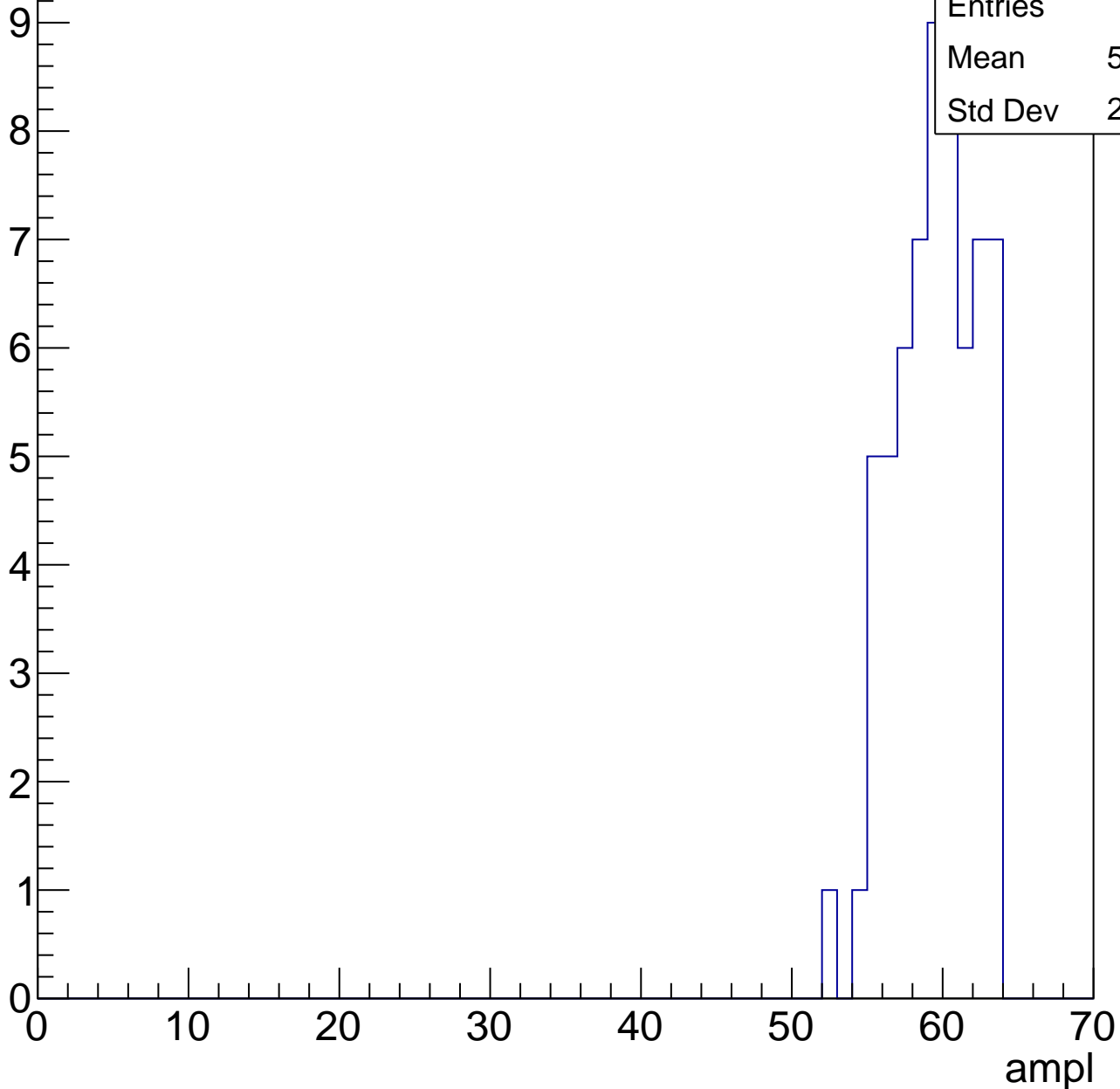


# B1L102S, U21-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

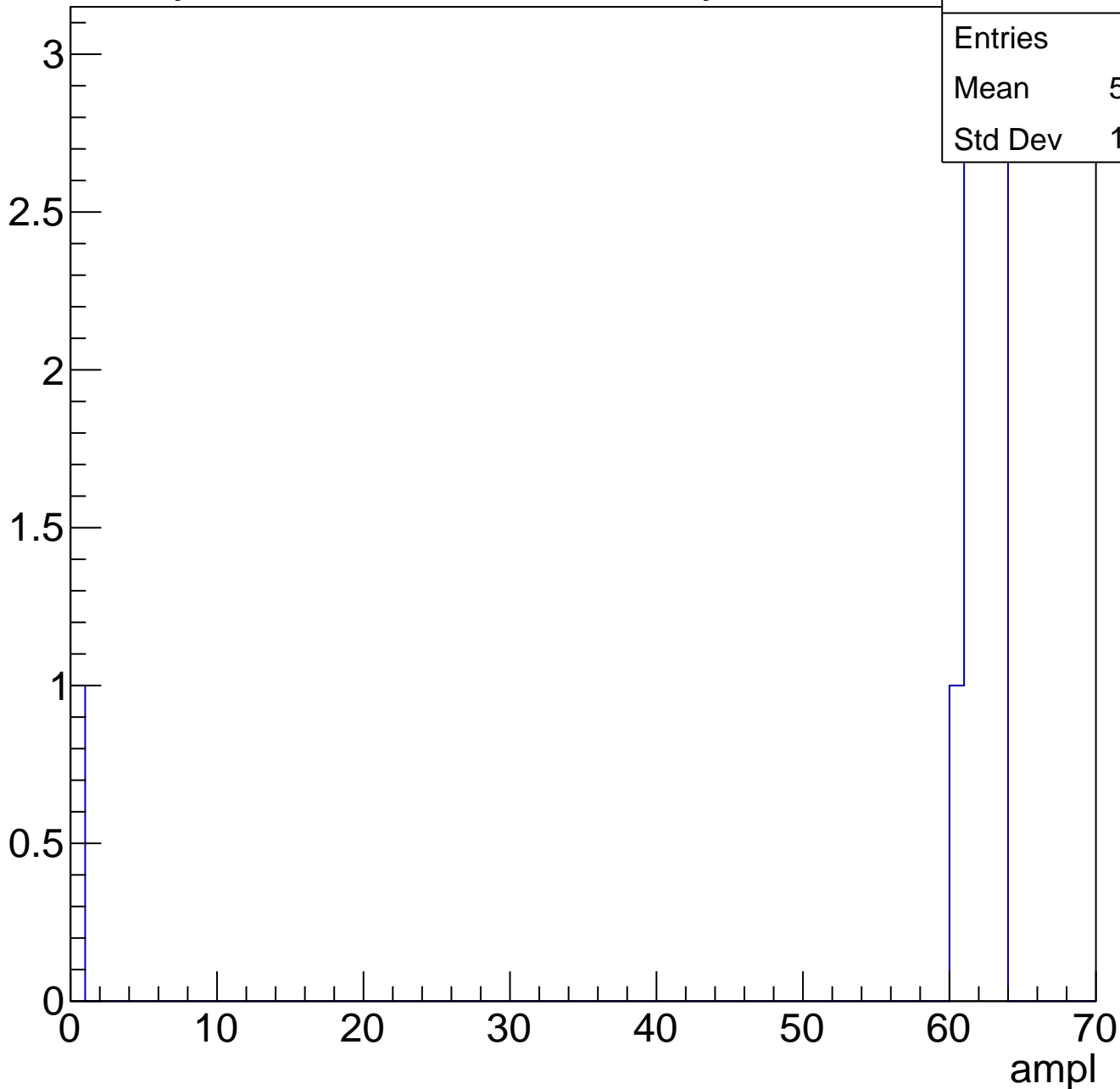
Entries	62
Mean	59.05
Std Dev	2.654



# B1L102S, U21-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U21-ch59, adc0

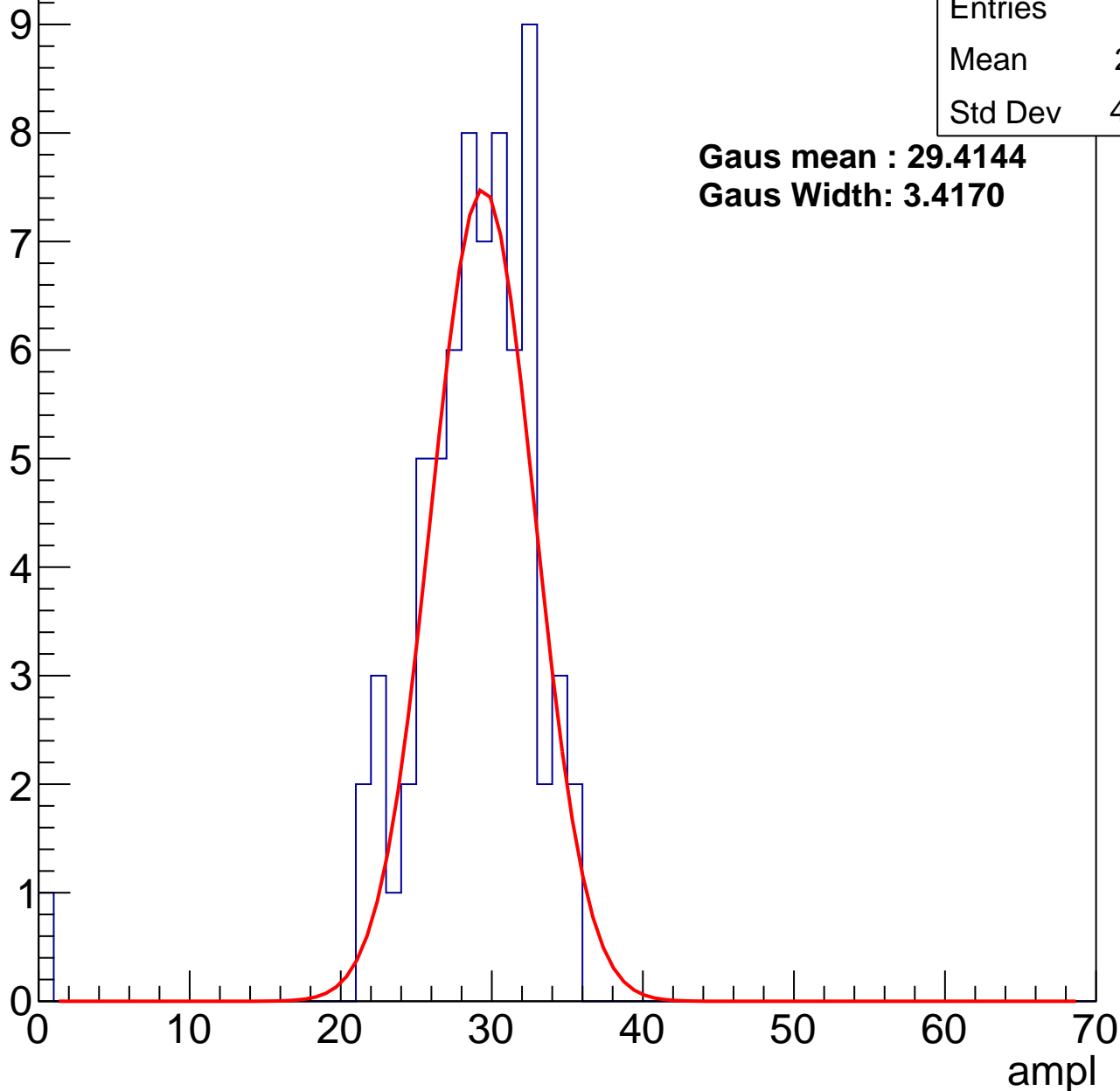
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	28.21
Std Dev	4.793

**Gaus mean : 29.4144**

**Gaus Width: 3.4170**



# B1L102S, U21-ch59, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	65
Mean	35.66
Std Dev	3.278

**Gaus mean : 36.6008**

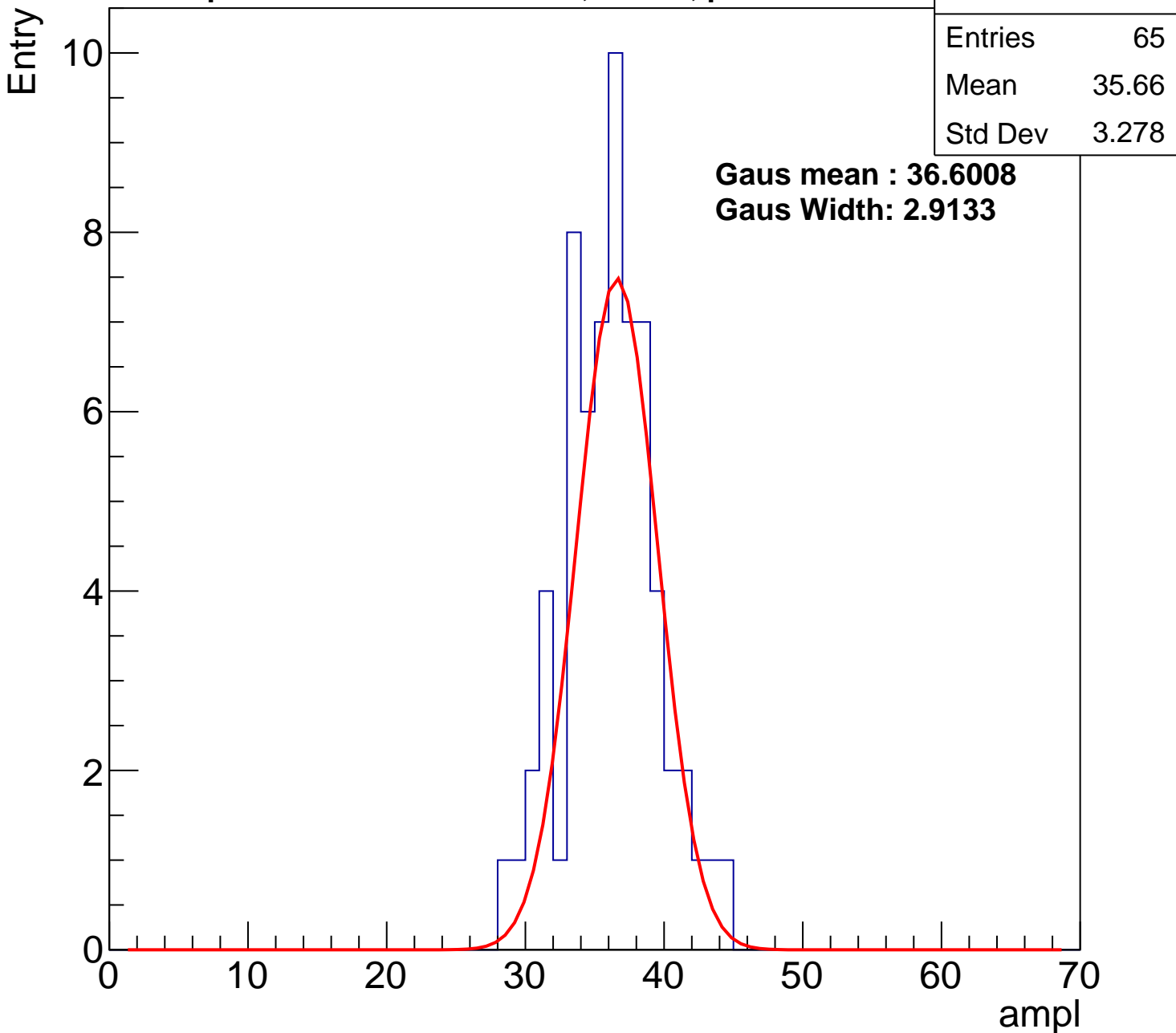
**Gaus Width: 2.9133**

Entry

10  
8  
6  
4  
2  
0

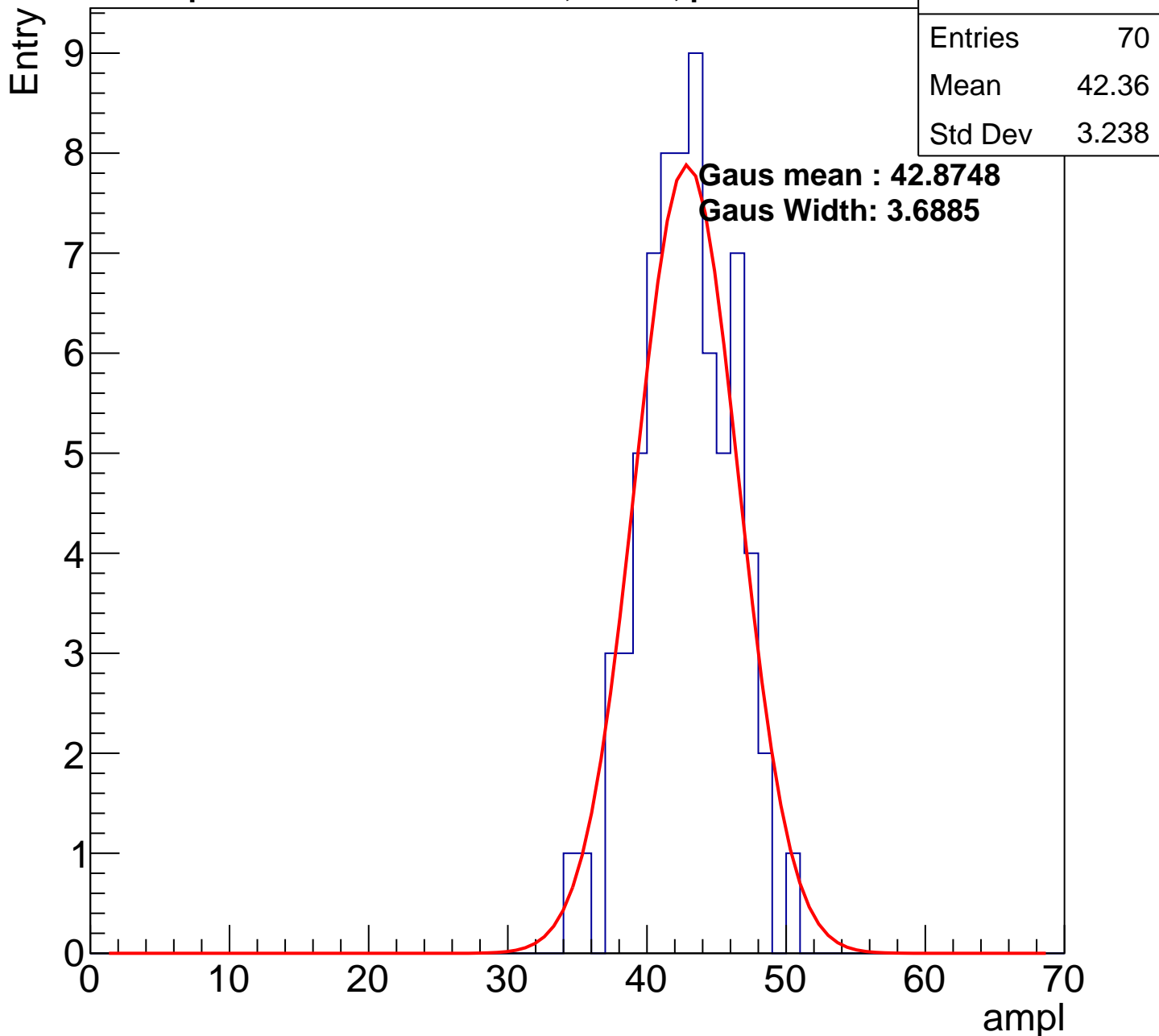
ampl

0 10 20 30 40 50 60 70



# B1L102S, U21-ch59, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

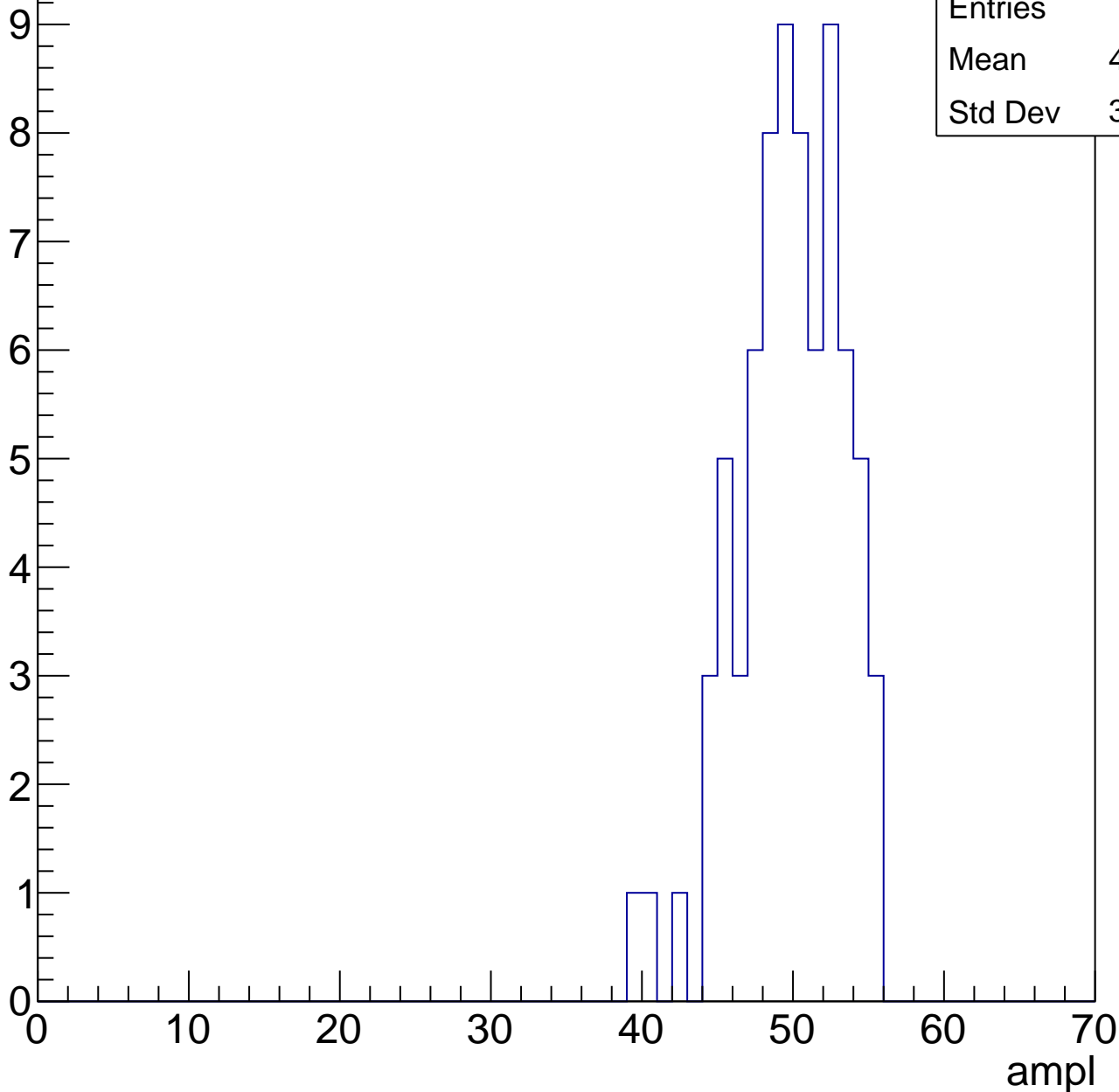


# B1L102S, U21-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	49.32
Std Dev	3.445

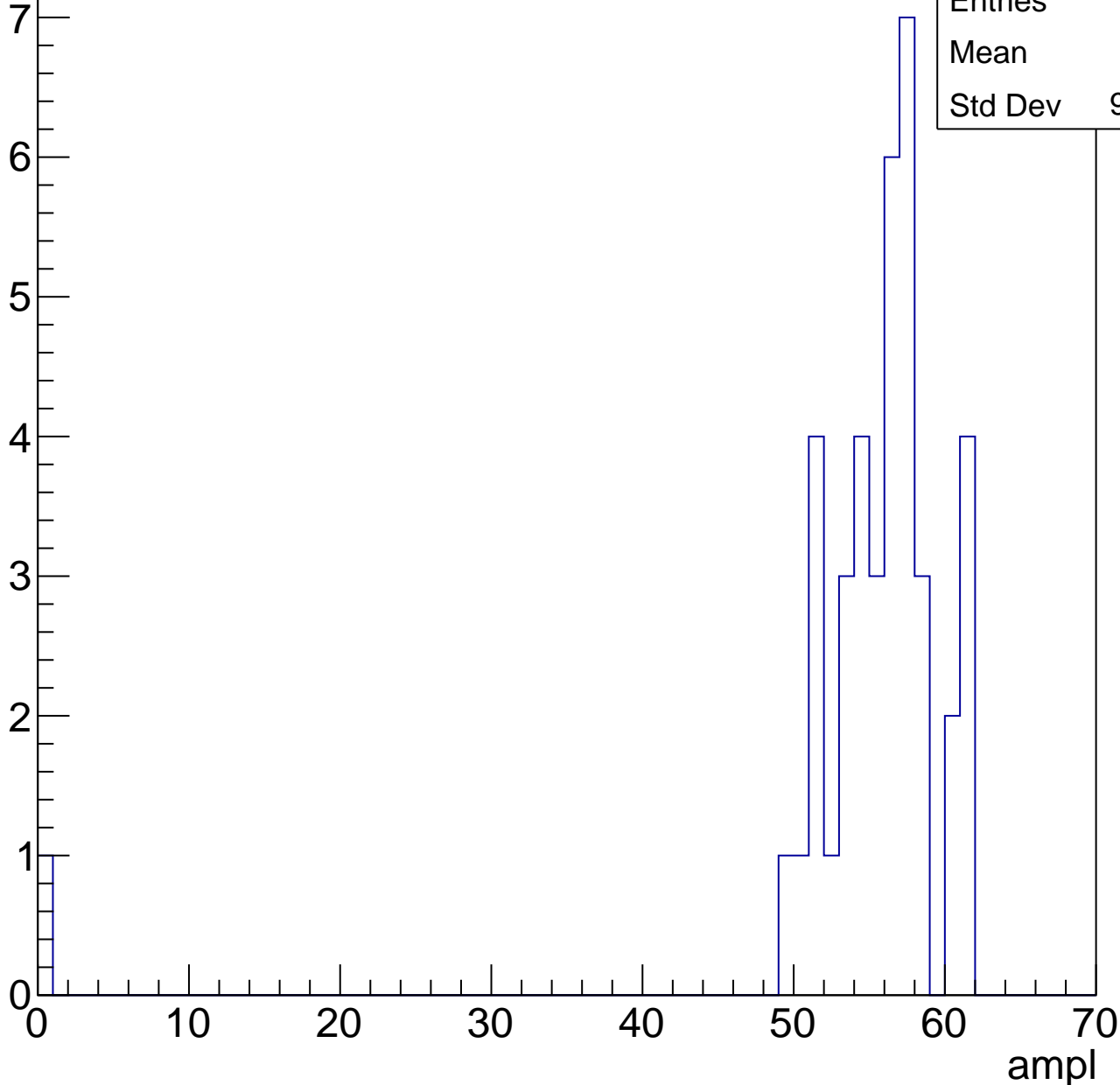


# B1L102S, U21-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	54.2
Std Dev	9.226

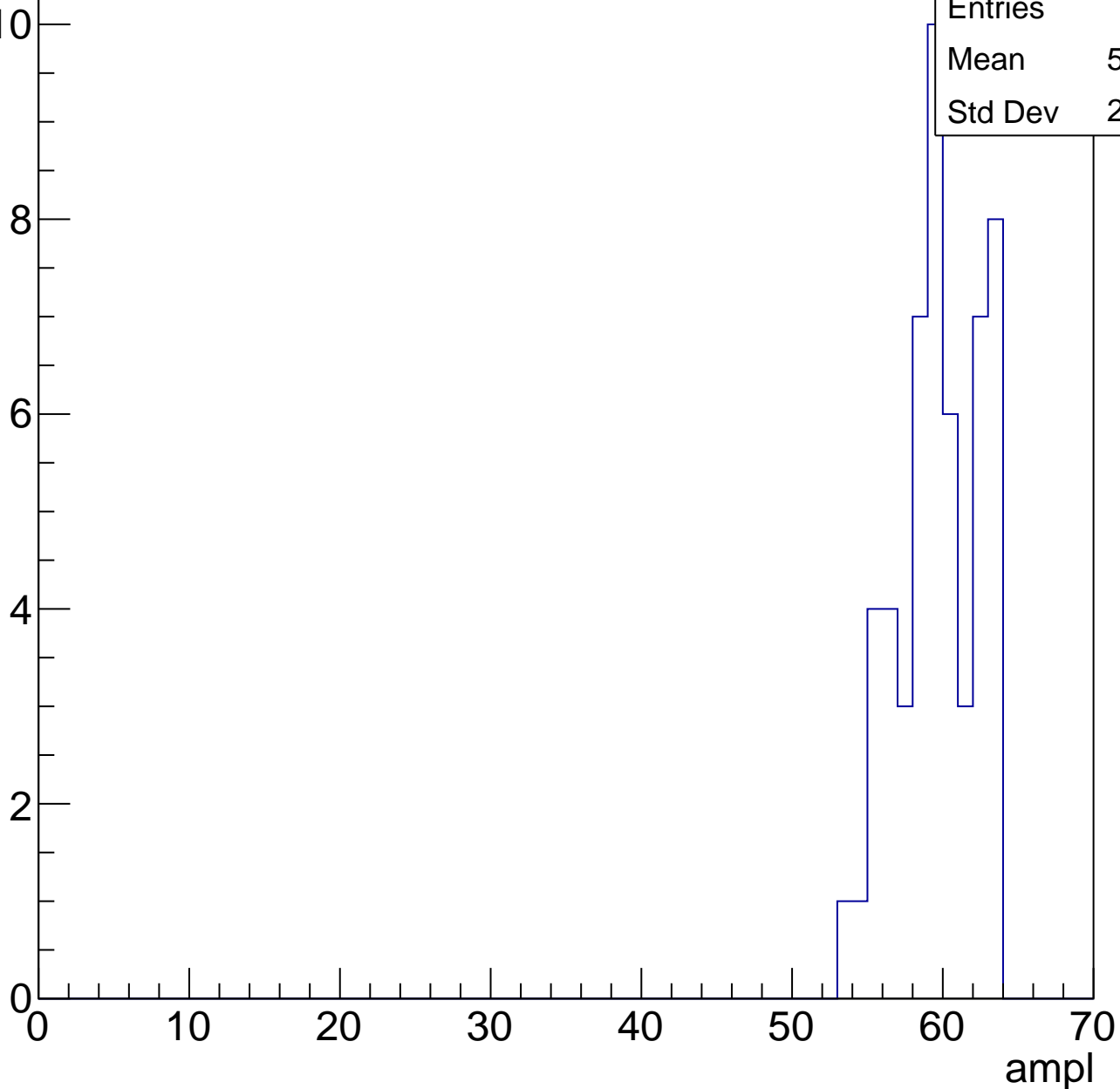


# B1L102S, U21-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

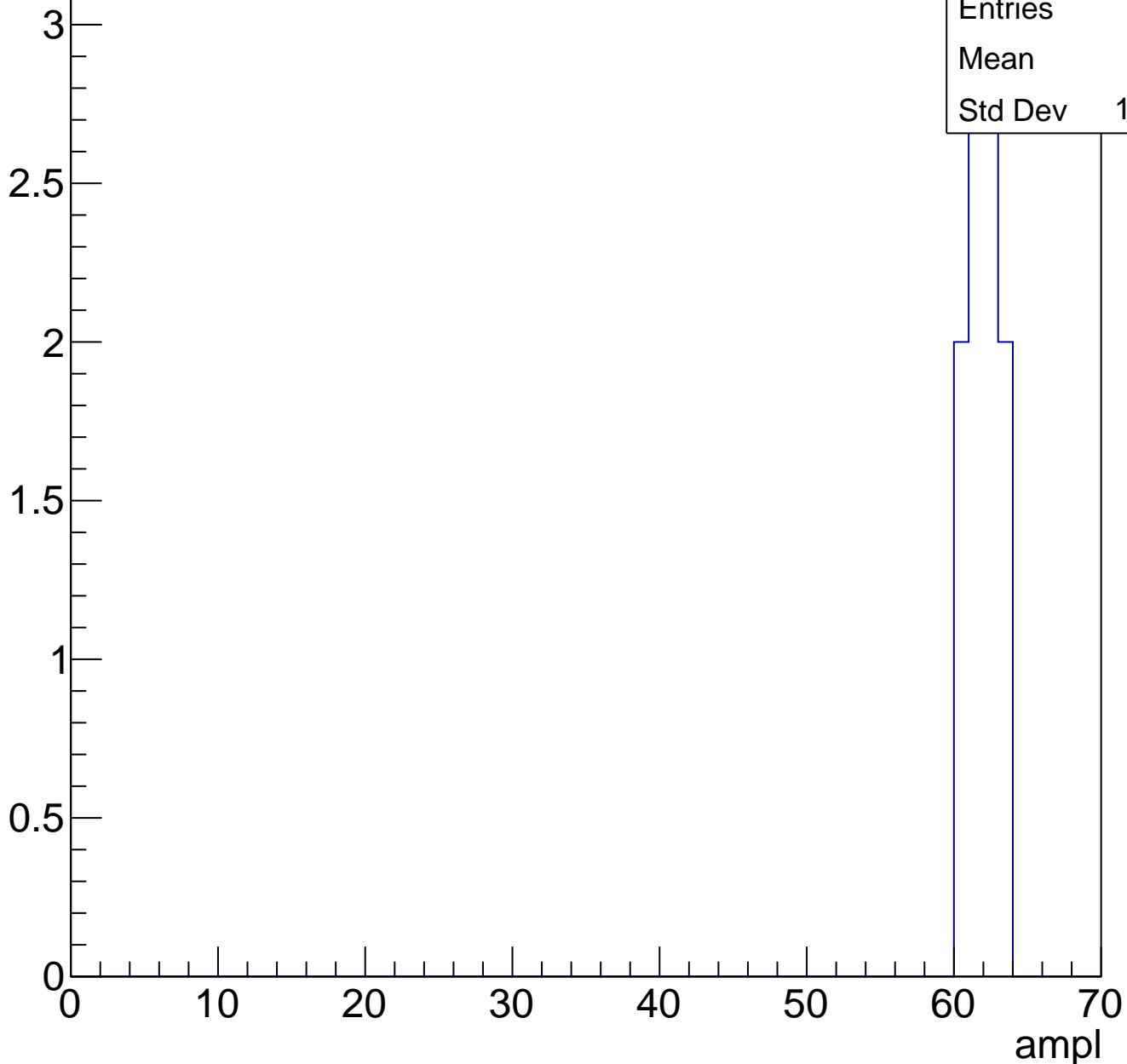
Entries	54
Mean	59.24
Std Dev	2.673



# B1L102S, U21-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

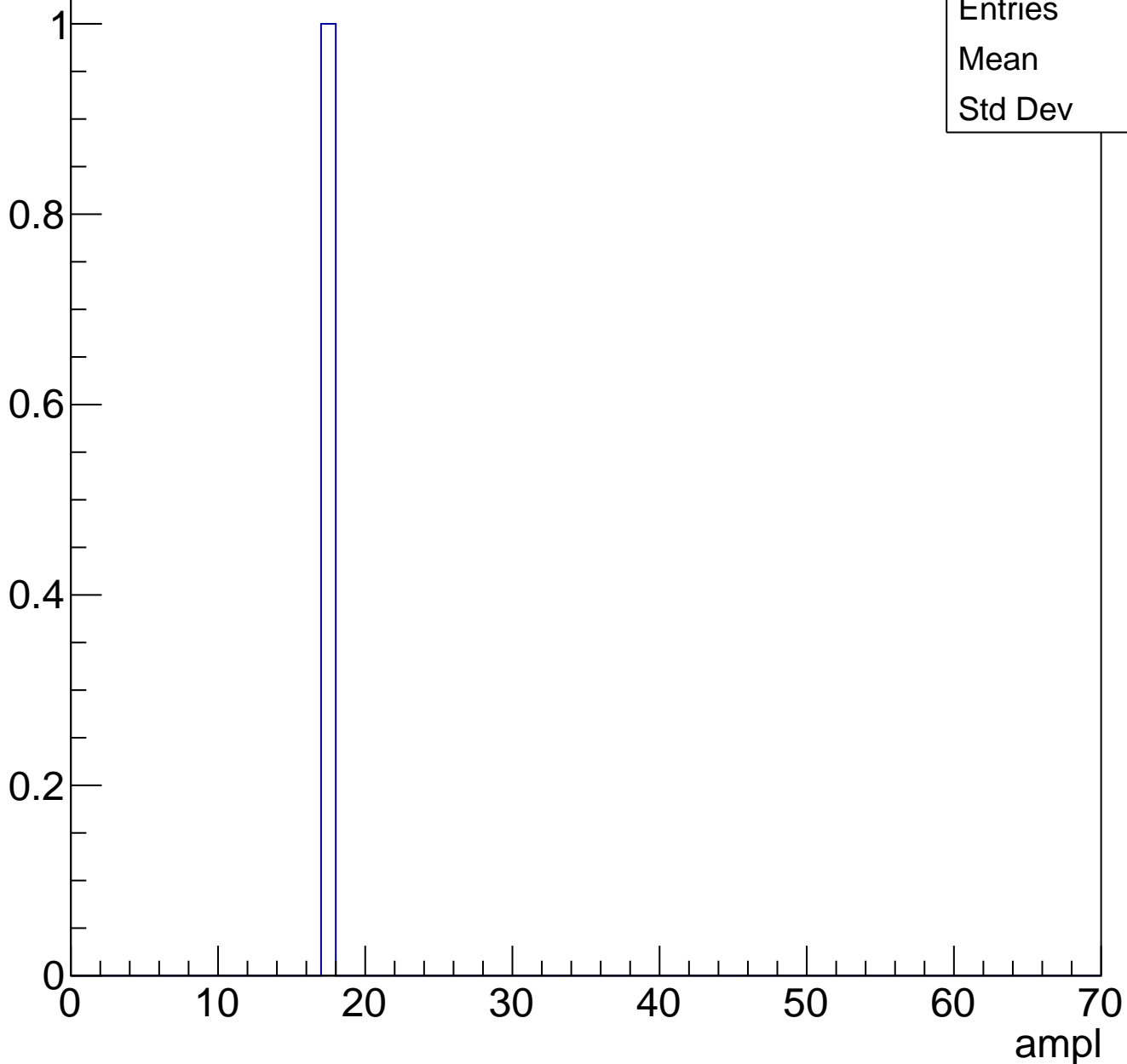




# B1L102S, U21-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch60, adc0

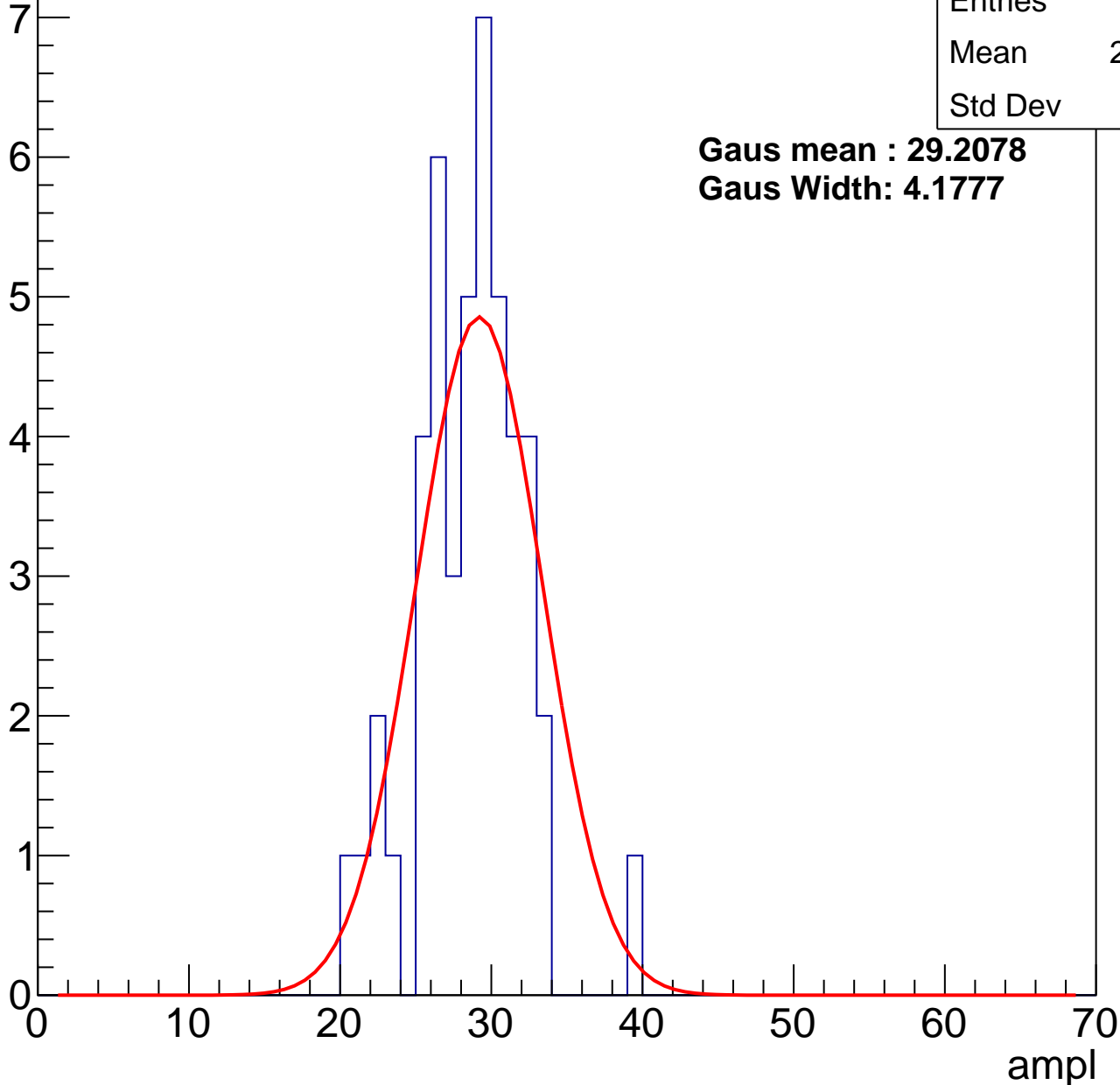
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	28.15
Std Dev	3.52

**Gaus mean : 29.2078**

**Gaus Width: 4.1777**



# B1L102S, U21-ch60, adc1

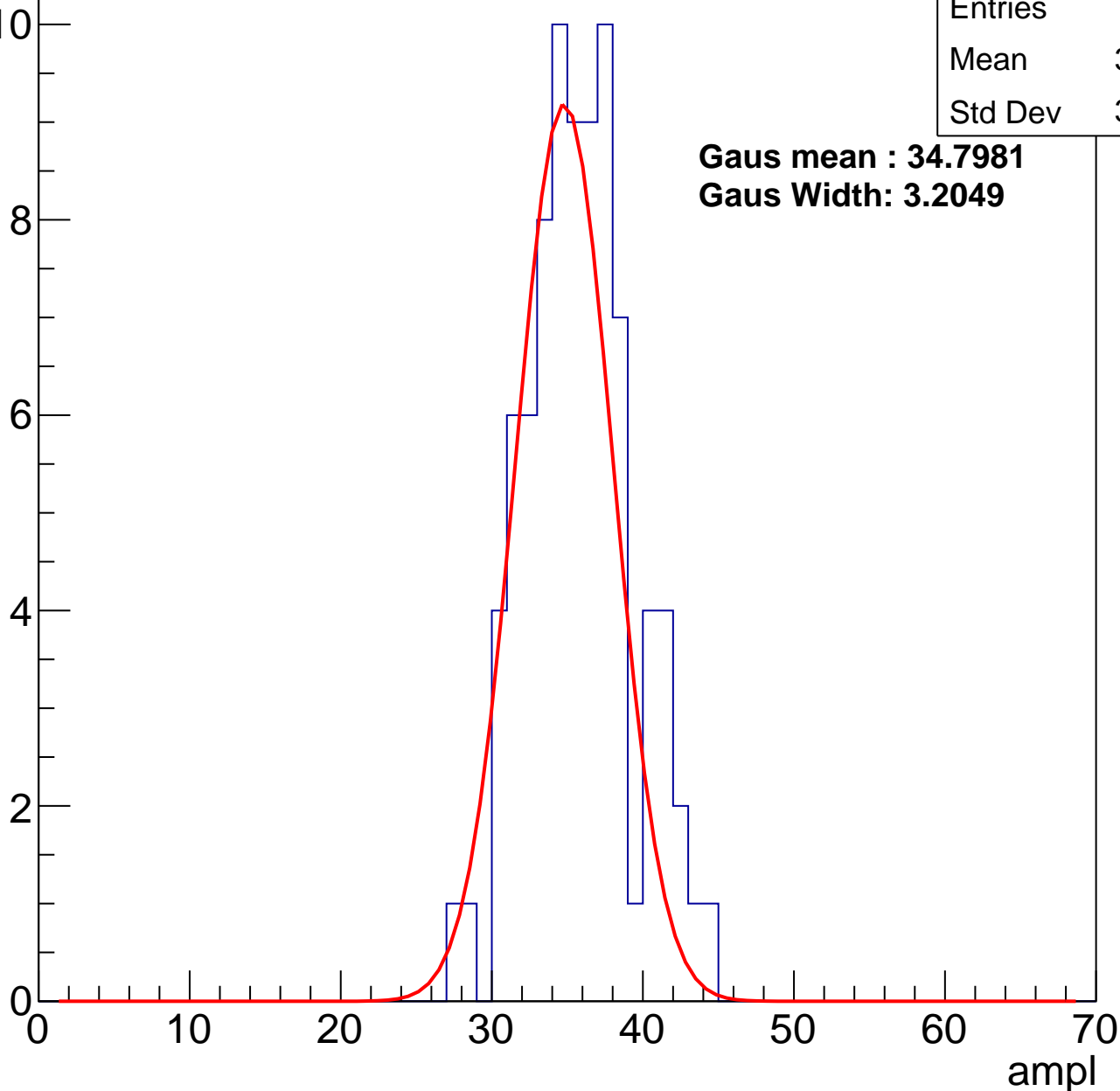
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	35.31
Std Dev	3.471

**Gaus mean : 34.7981**

**Gaus Width: 3.2049**



# B1L102S, U21-ch60, adc2

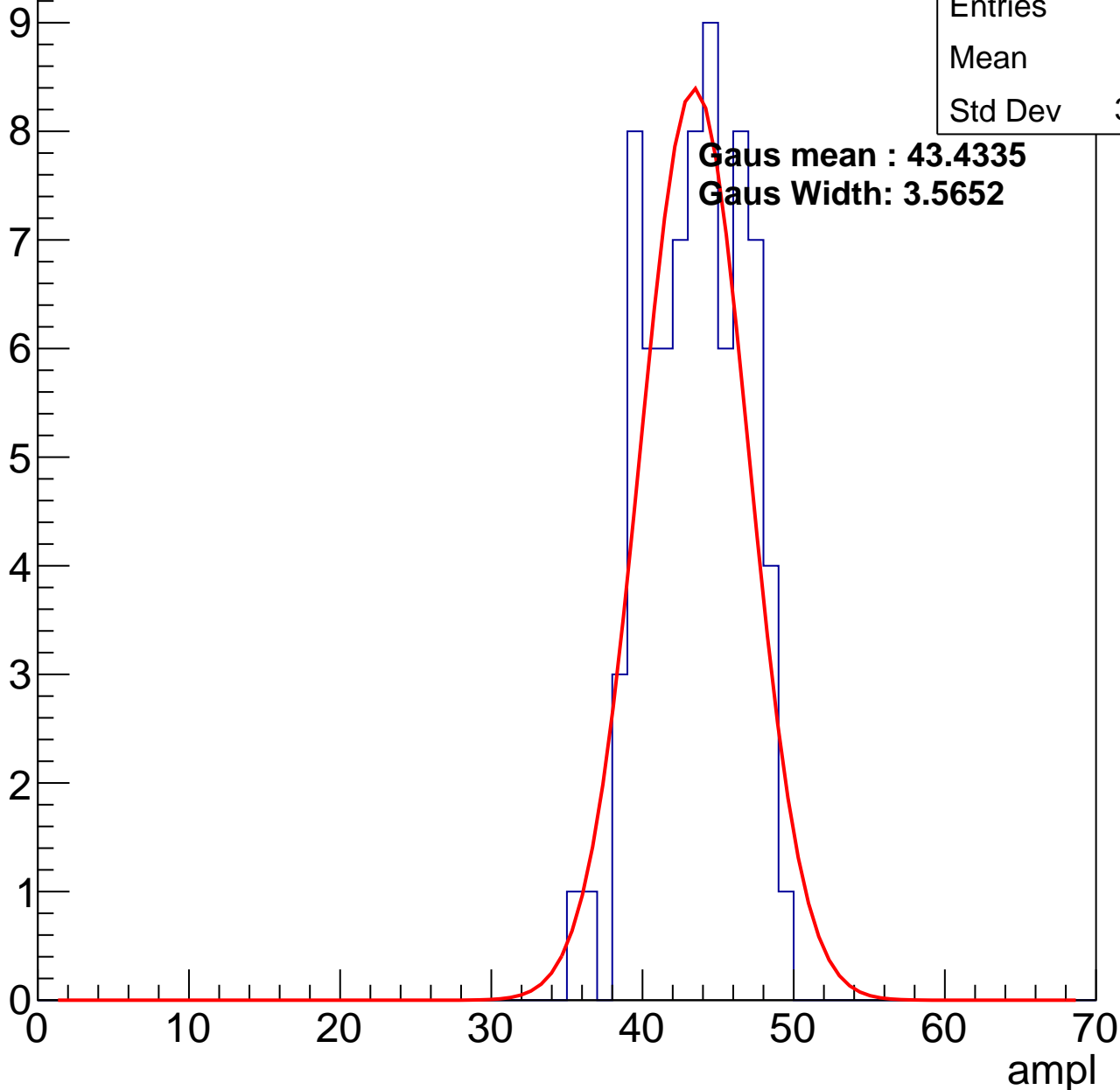
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	43
Std Dev	3.171

**Gaus mean : 43.4335**

**Gaus Width: 3.5652**

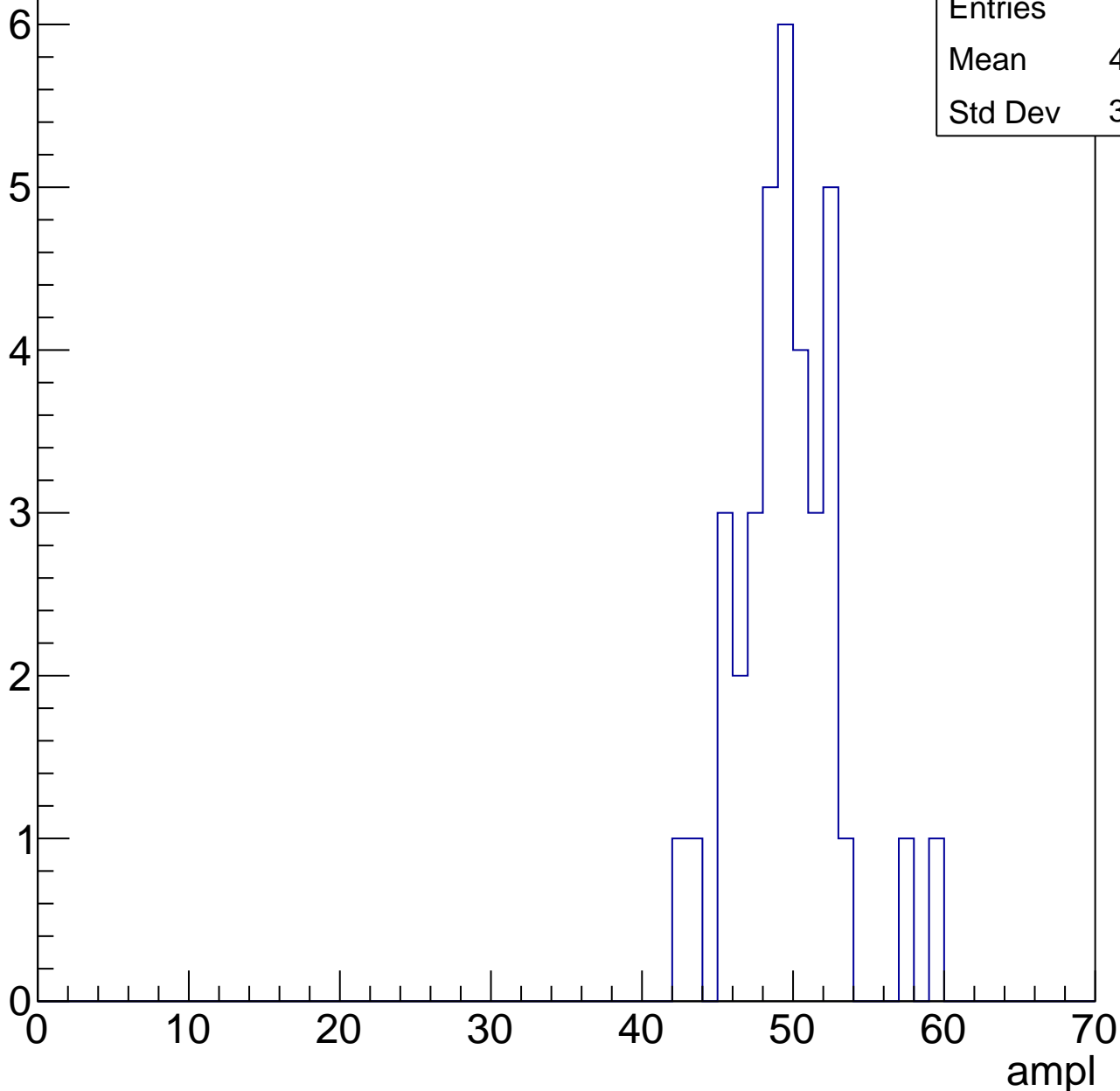


# B1L102S, U21-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	36
Mean	49.14
Std Dev	3.368

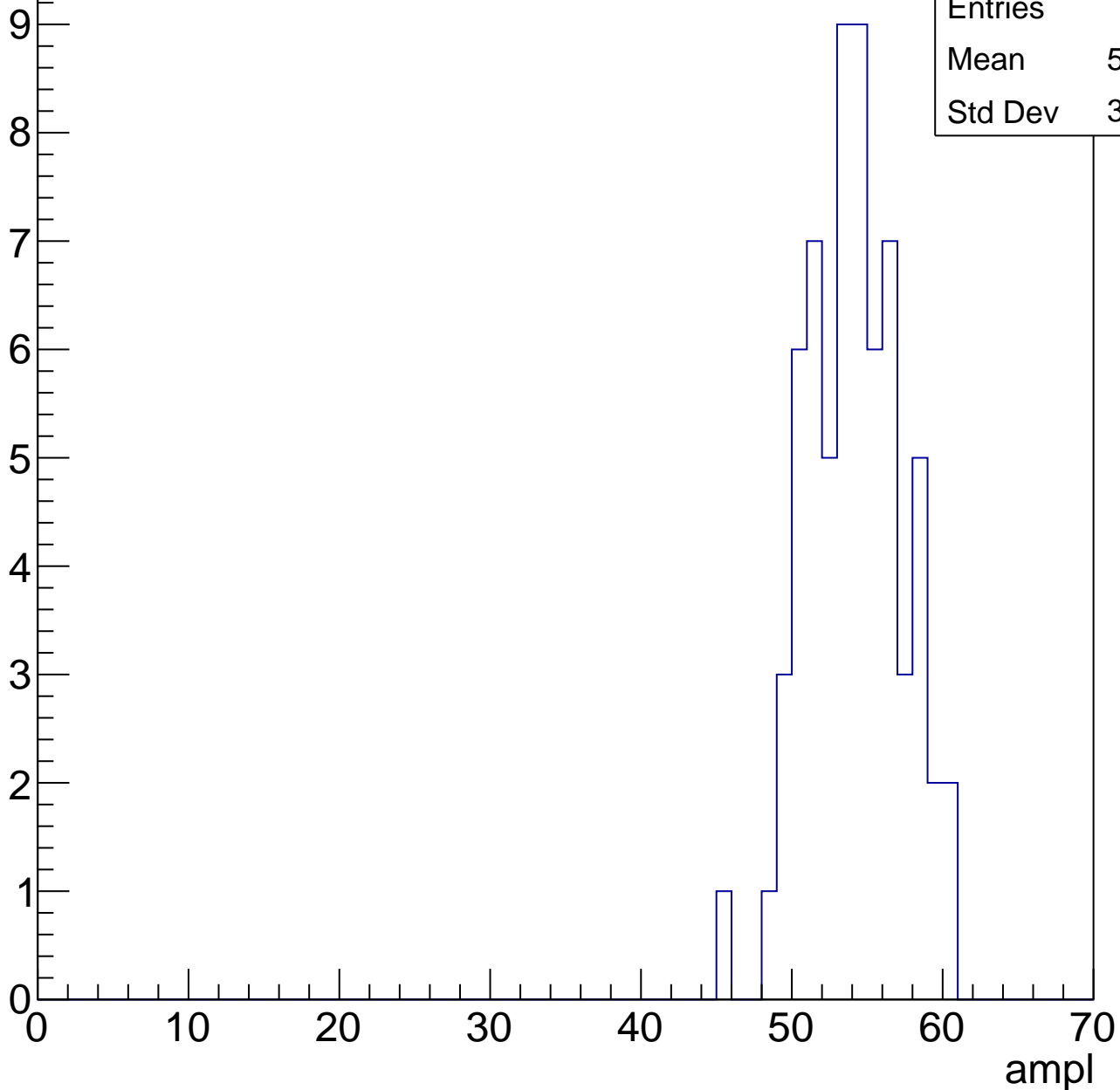


# B1L102S, U21-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	53.65
Std Dev	3.102

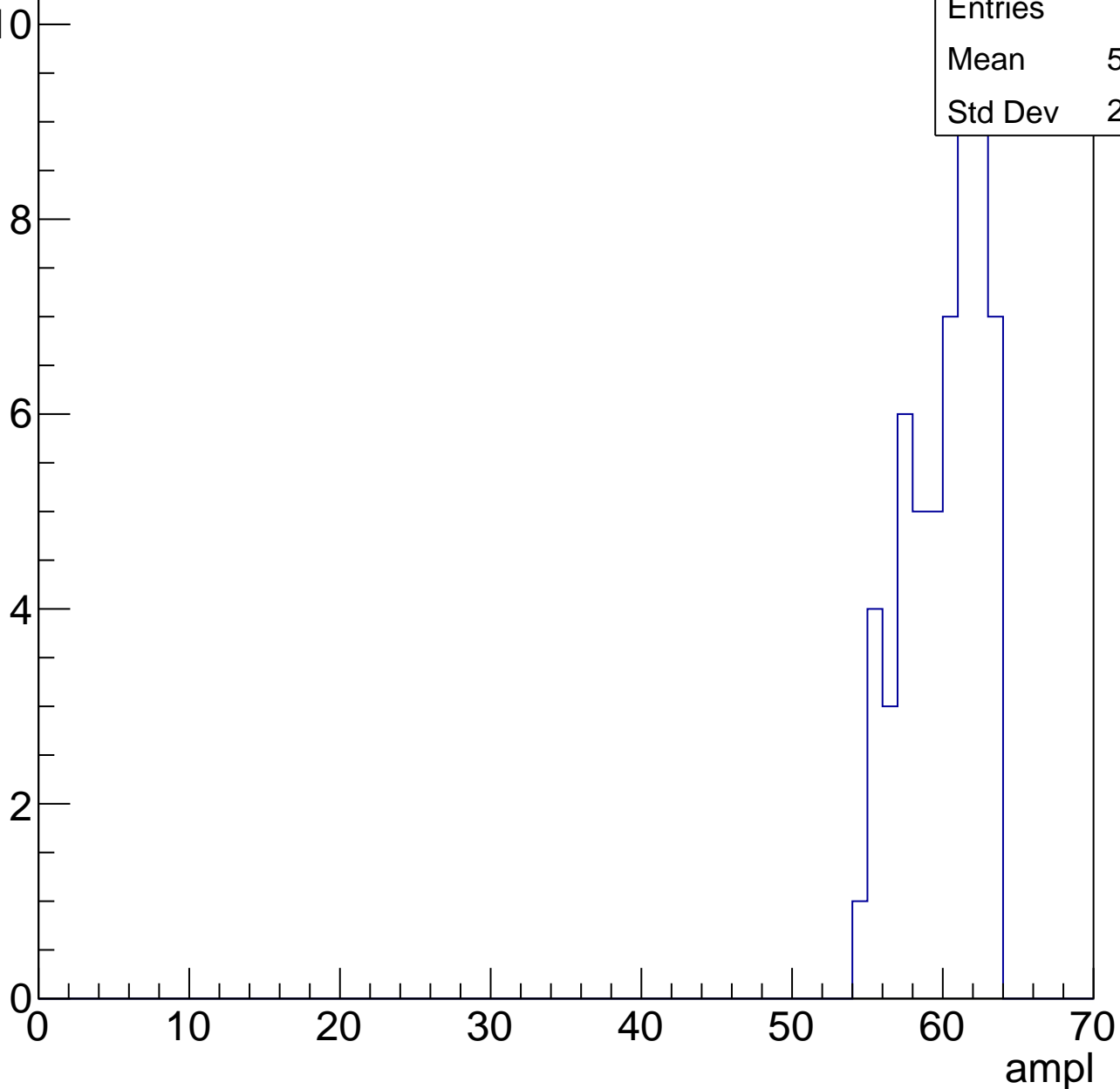


# B1L102S, U21-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	59.63
Std Dev	2.538



# B1L102S, U21-ch60, adc6

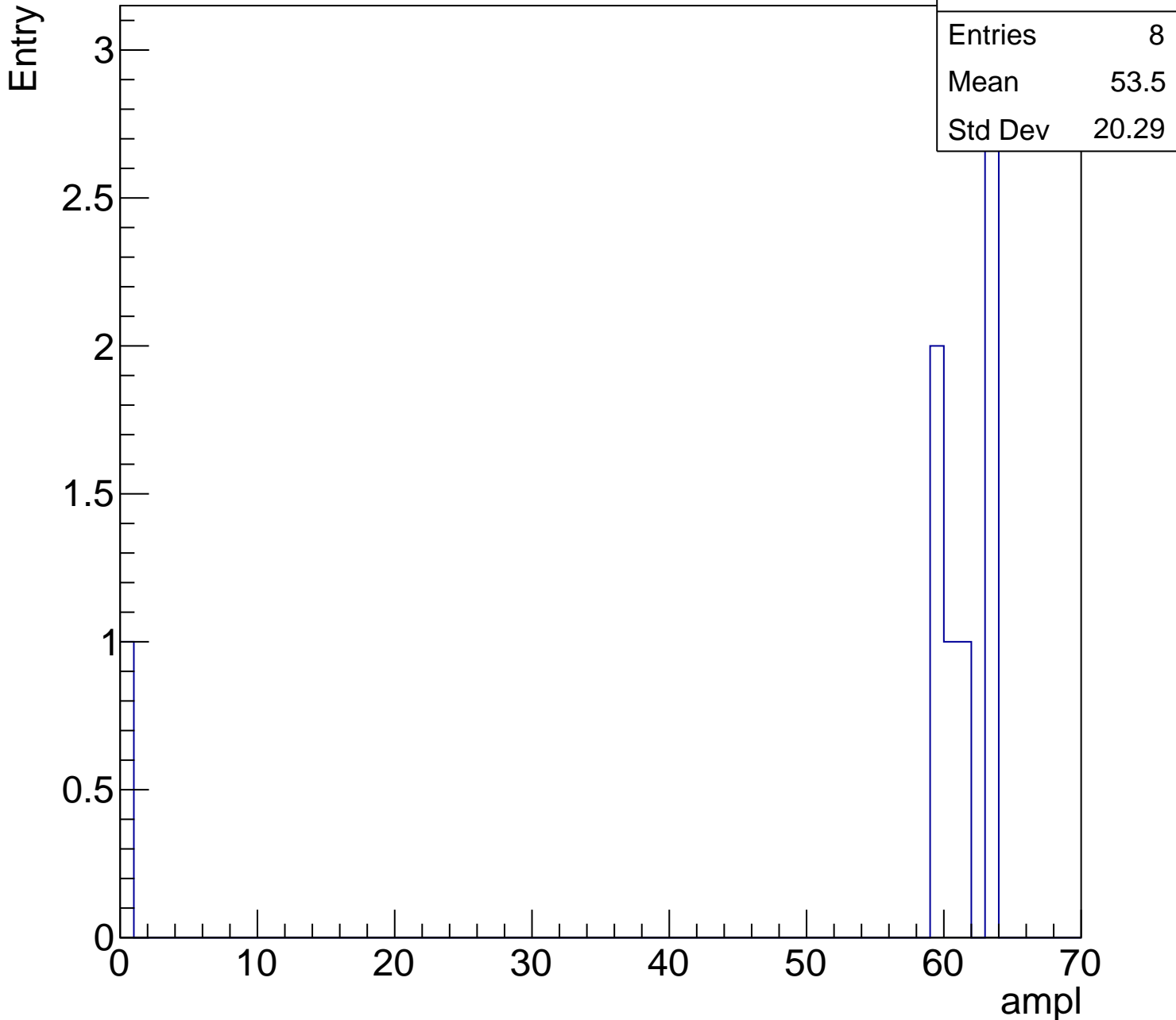
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	8
Mean	53.5
Std Dev	20.29

ampl





# B1L102S, U21-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch61, adc0

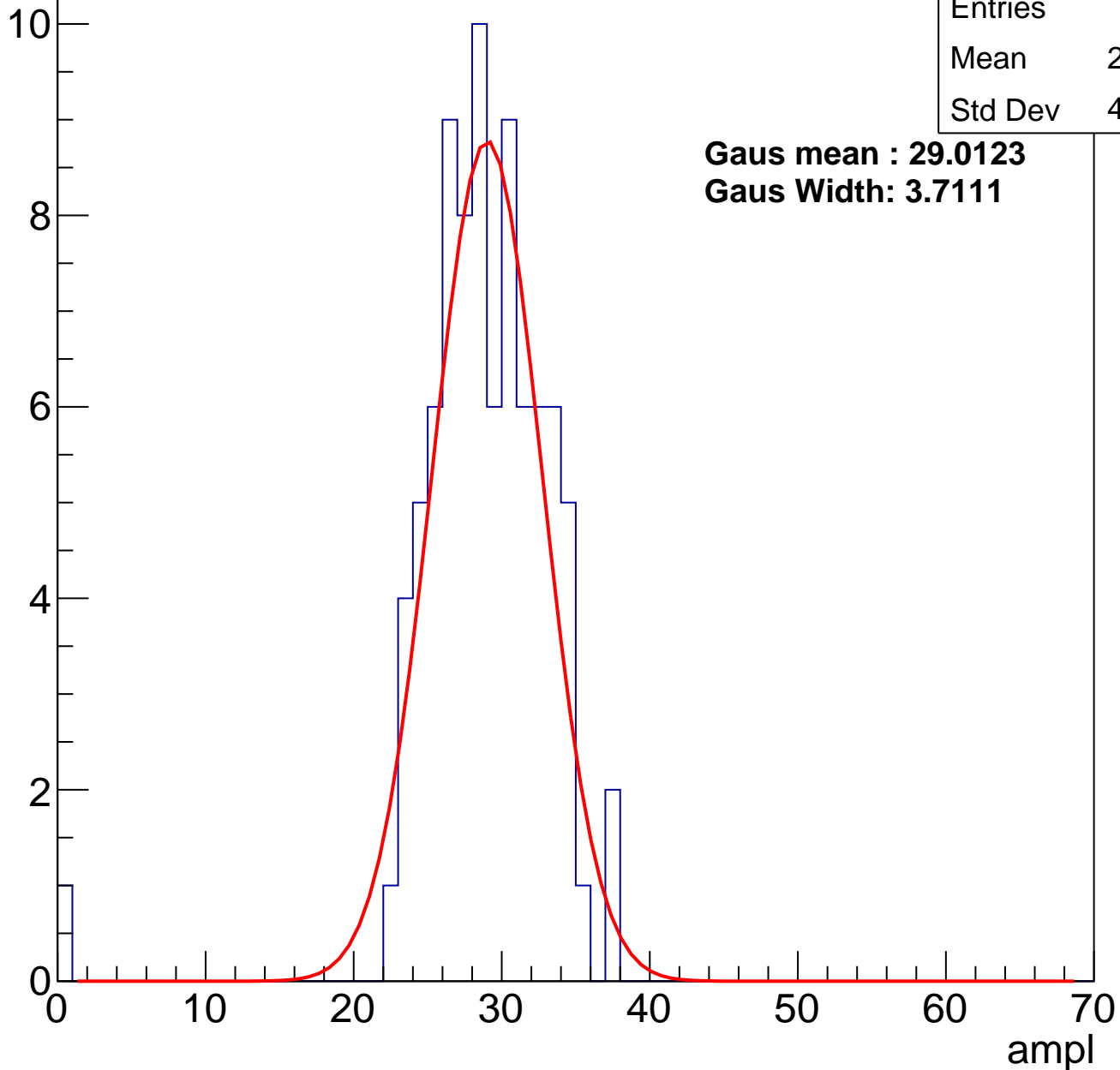
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	85
Mean	28.39
Std Dev	4.625

**Gaus mean : 29.0123**

**Gaus Width: 3.7111**

Entry



# B1L102S, U21-ch61, adc1

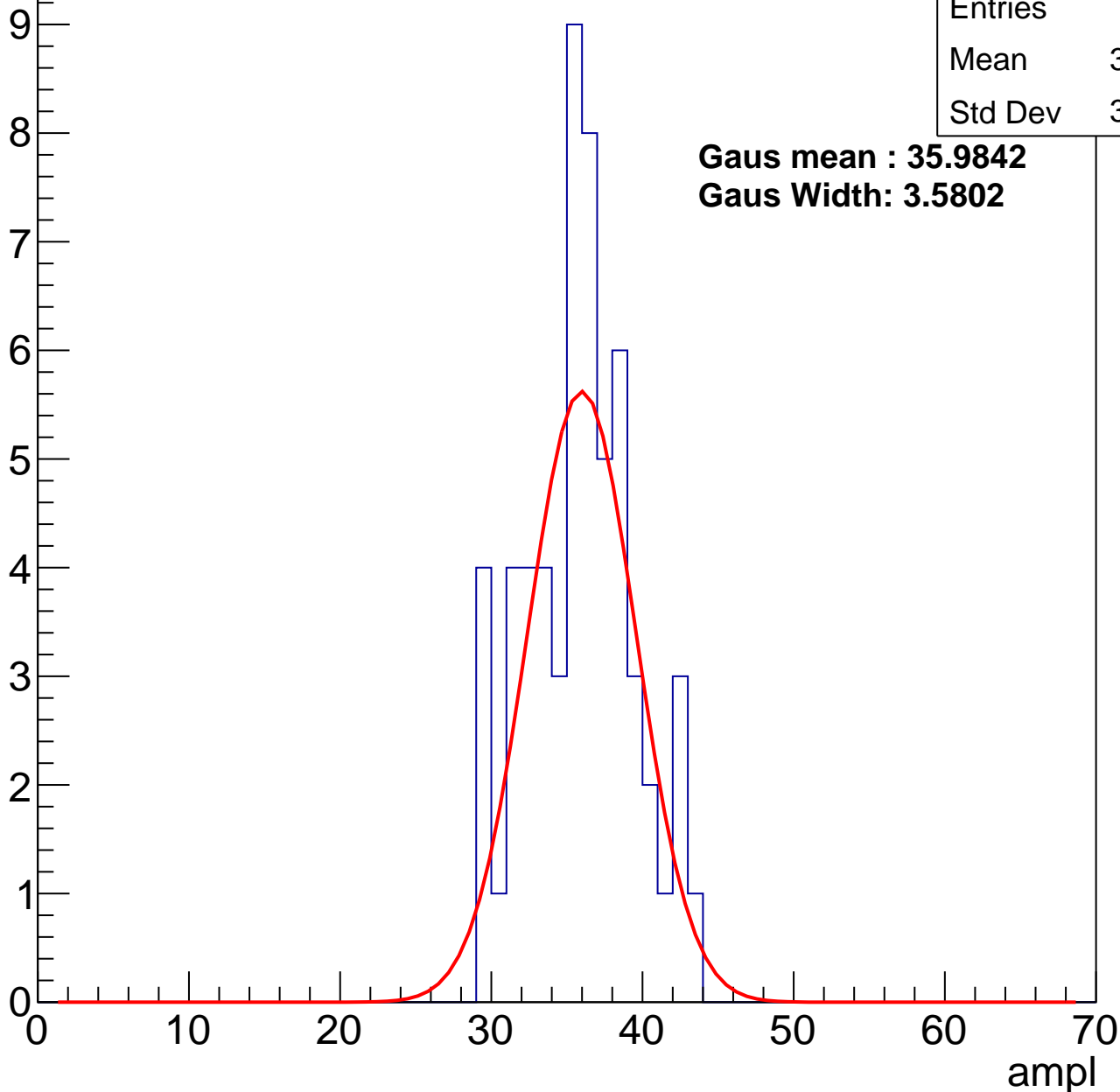
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	35.43
Std Dev	3.485

**Gaus mean : 35.9842**

**Gaus Width: 3.5802**



# B1L102S, U21-ch61, adc2

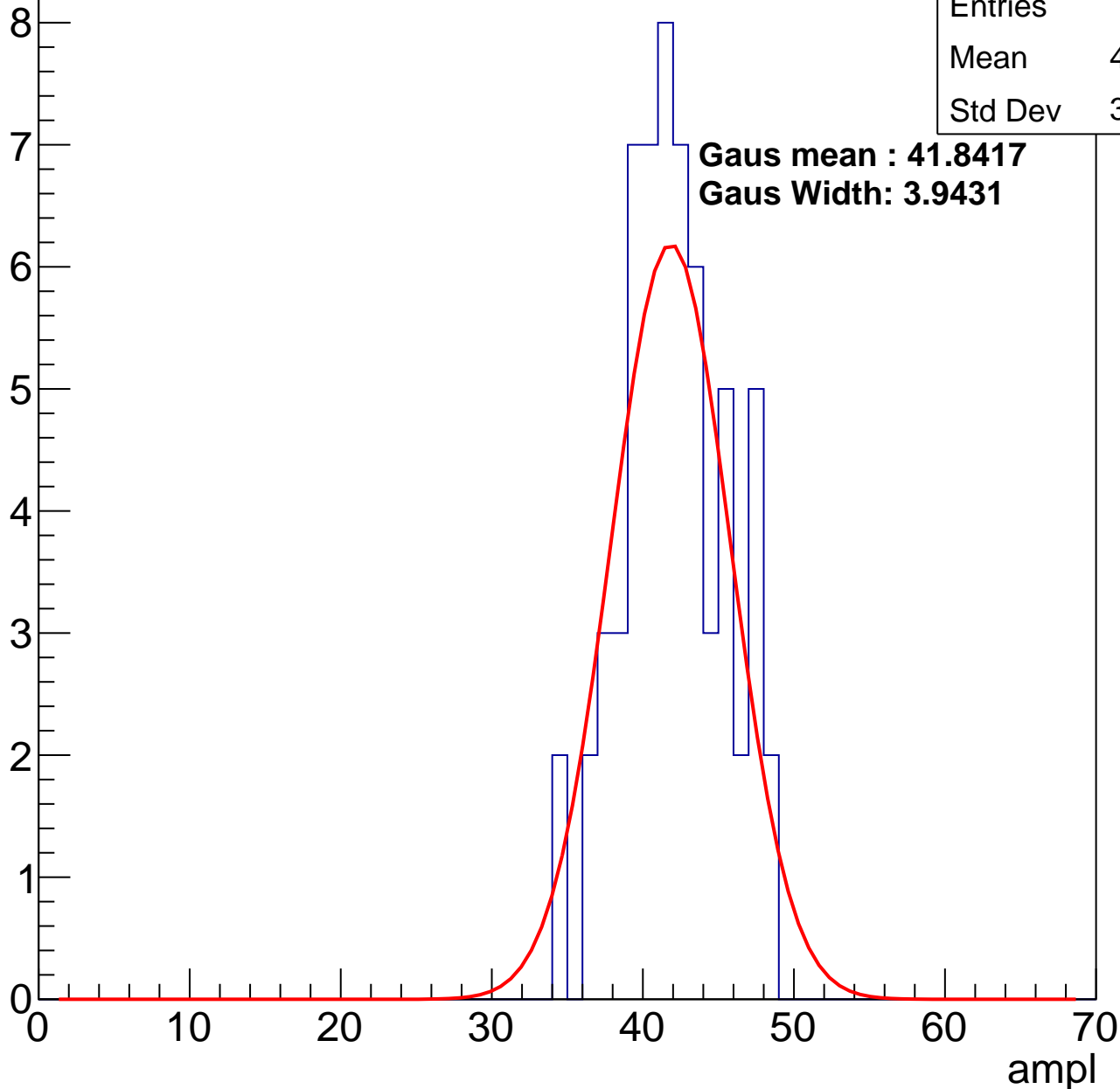
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	41.58
Std Dev	3.368

**Gaus mean : 41.8417**

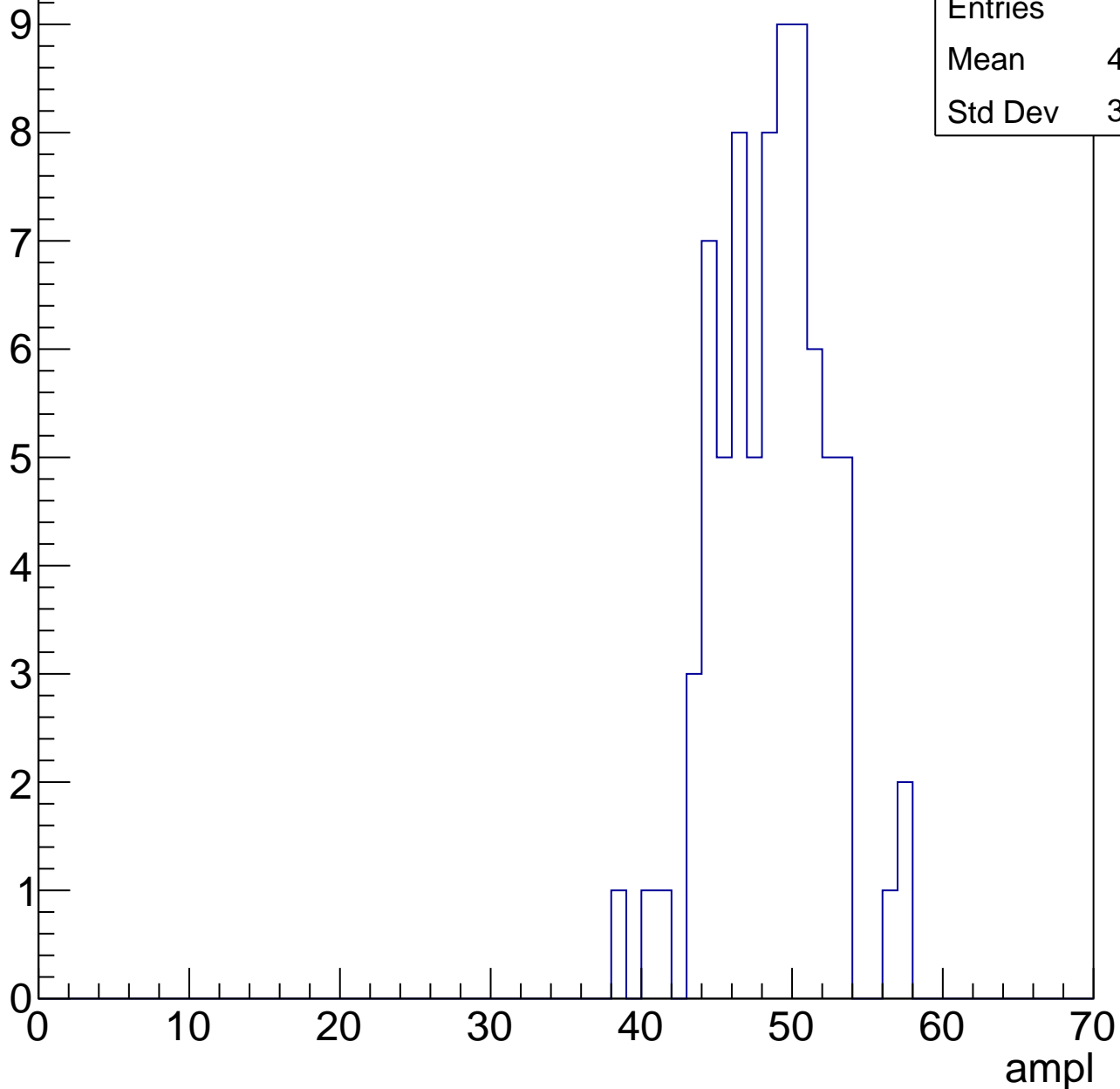
**Gaus Width: 3.9431**



# B1L102S, U21-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

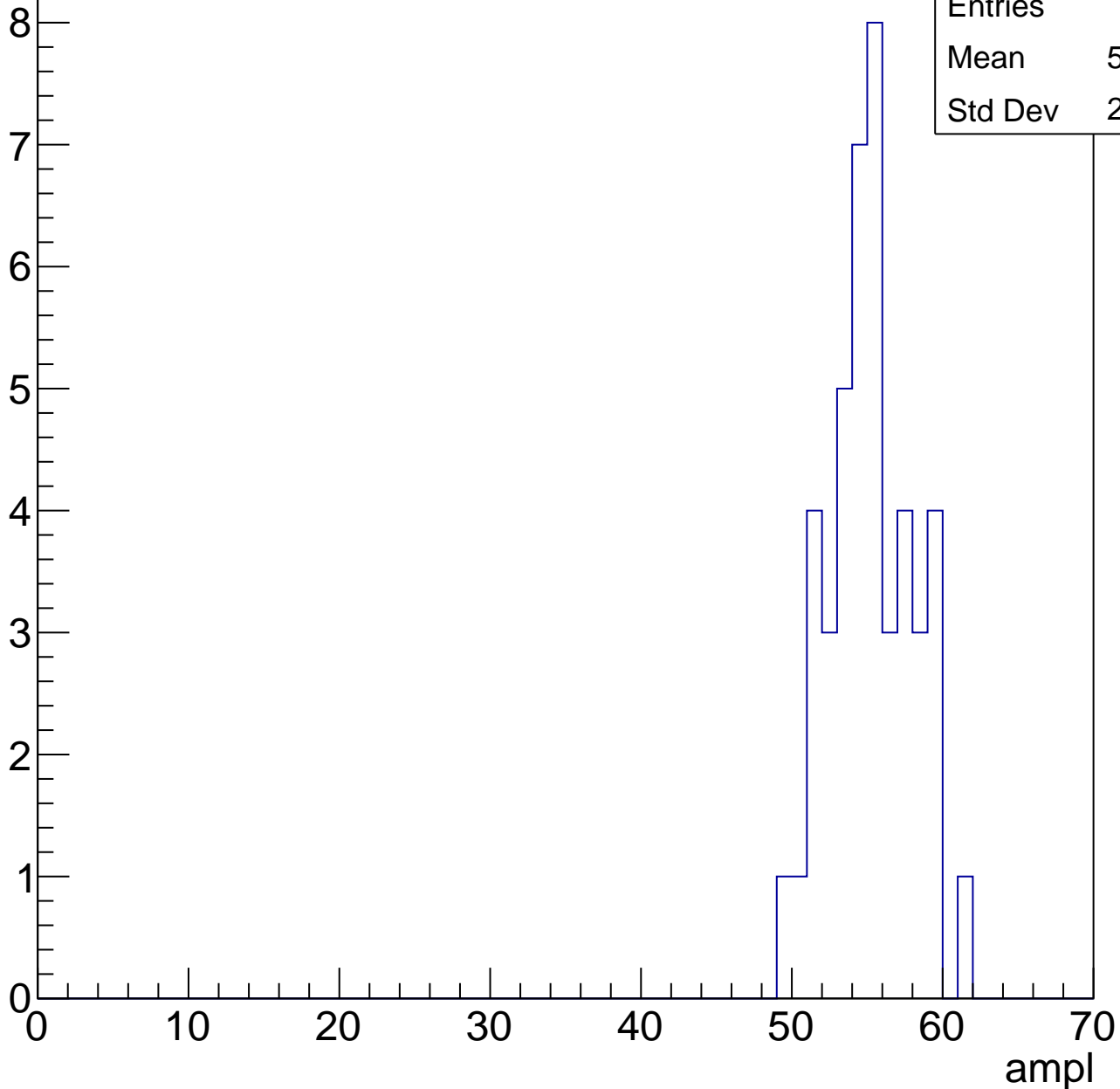


# B1L102S, U21-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	44
Mean	54.75
Std Dev	2.706

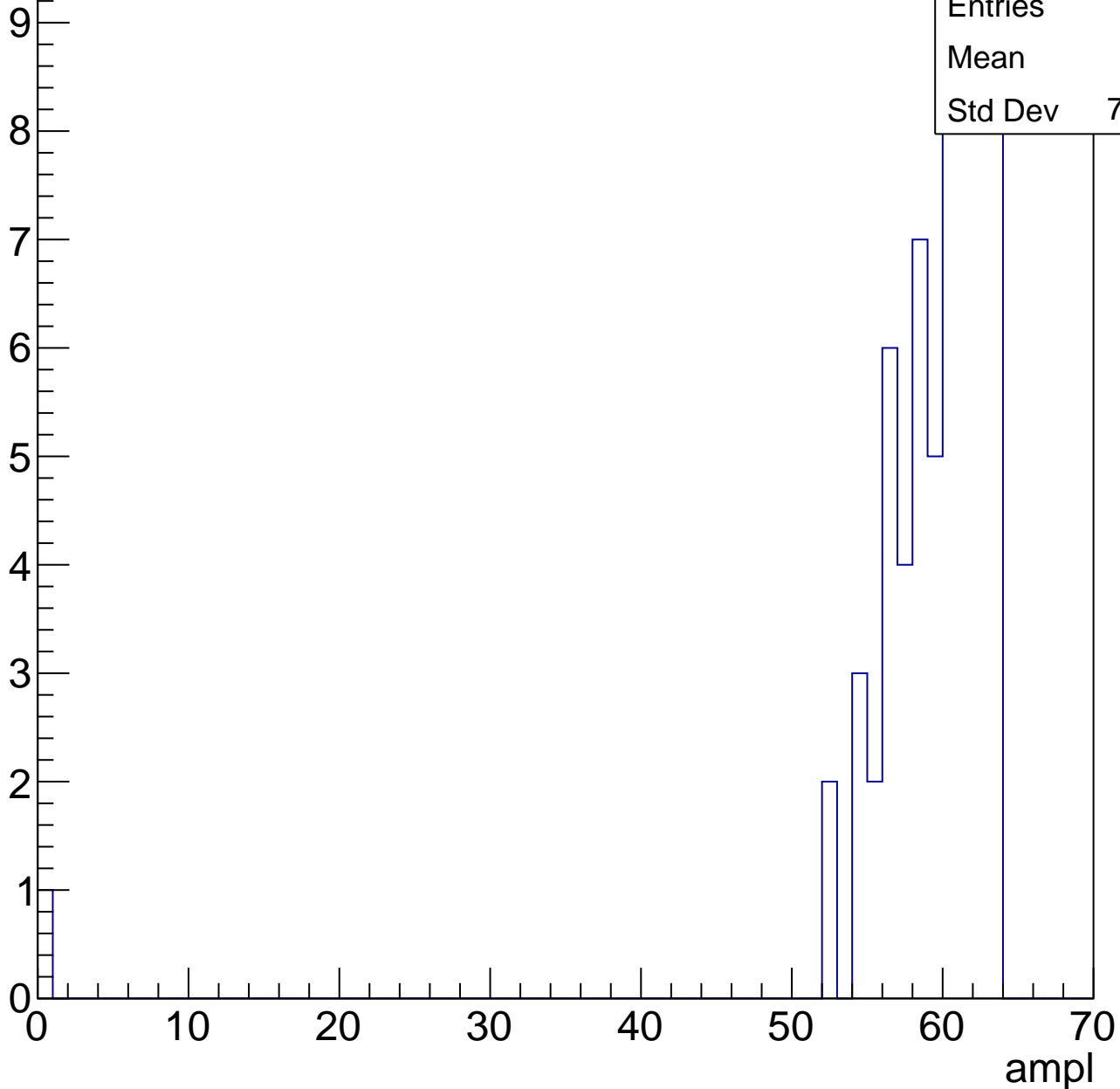


# B1L102S, U21-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

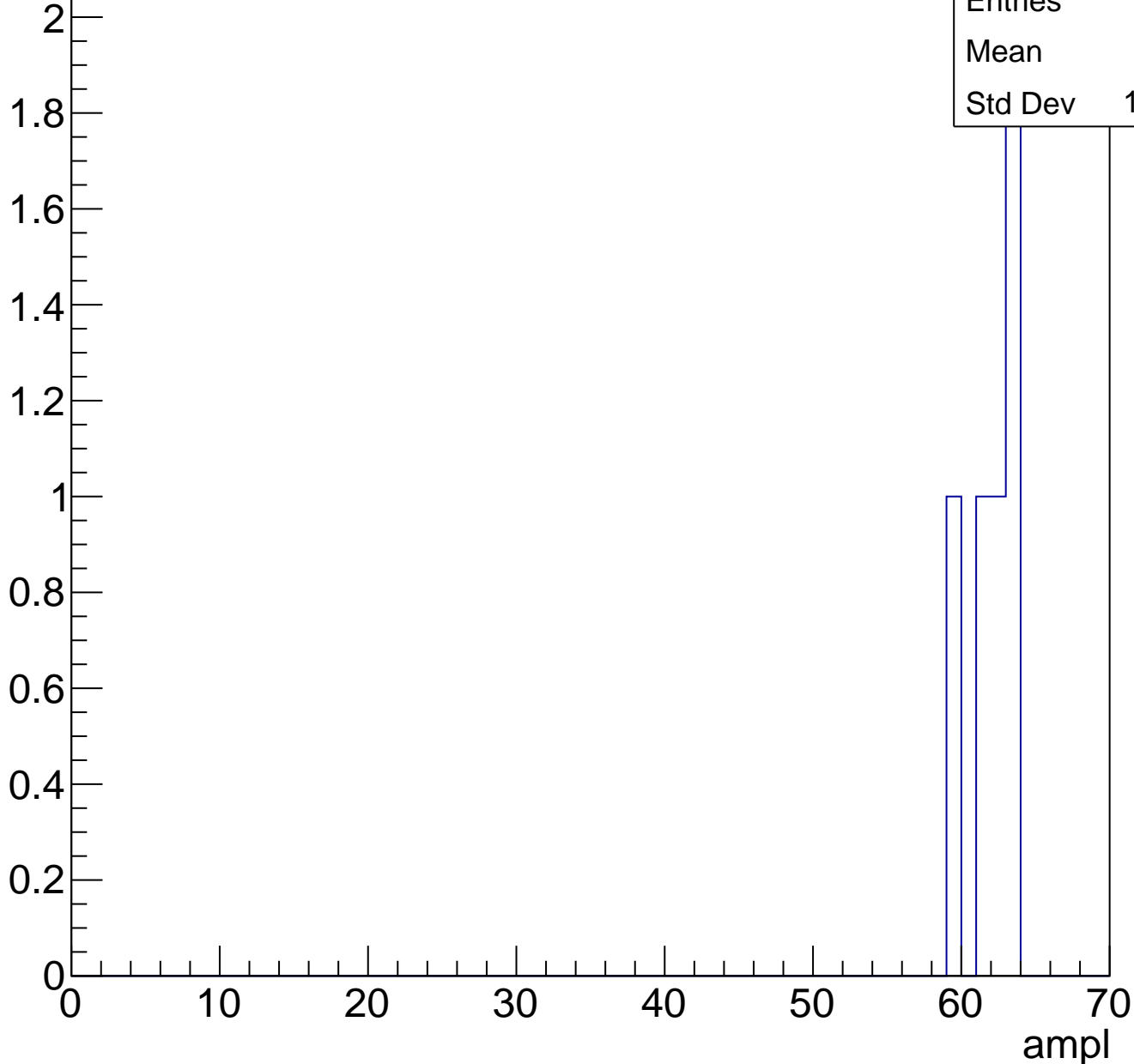
Entries	64
Mean	58.3
Std Dev	7.887



# B1L102S, U21-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

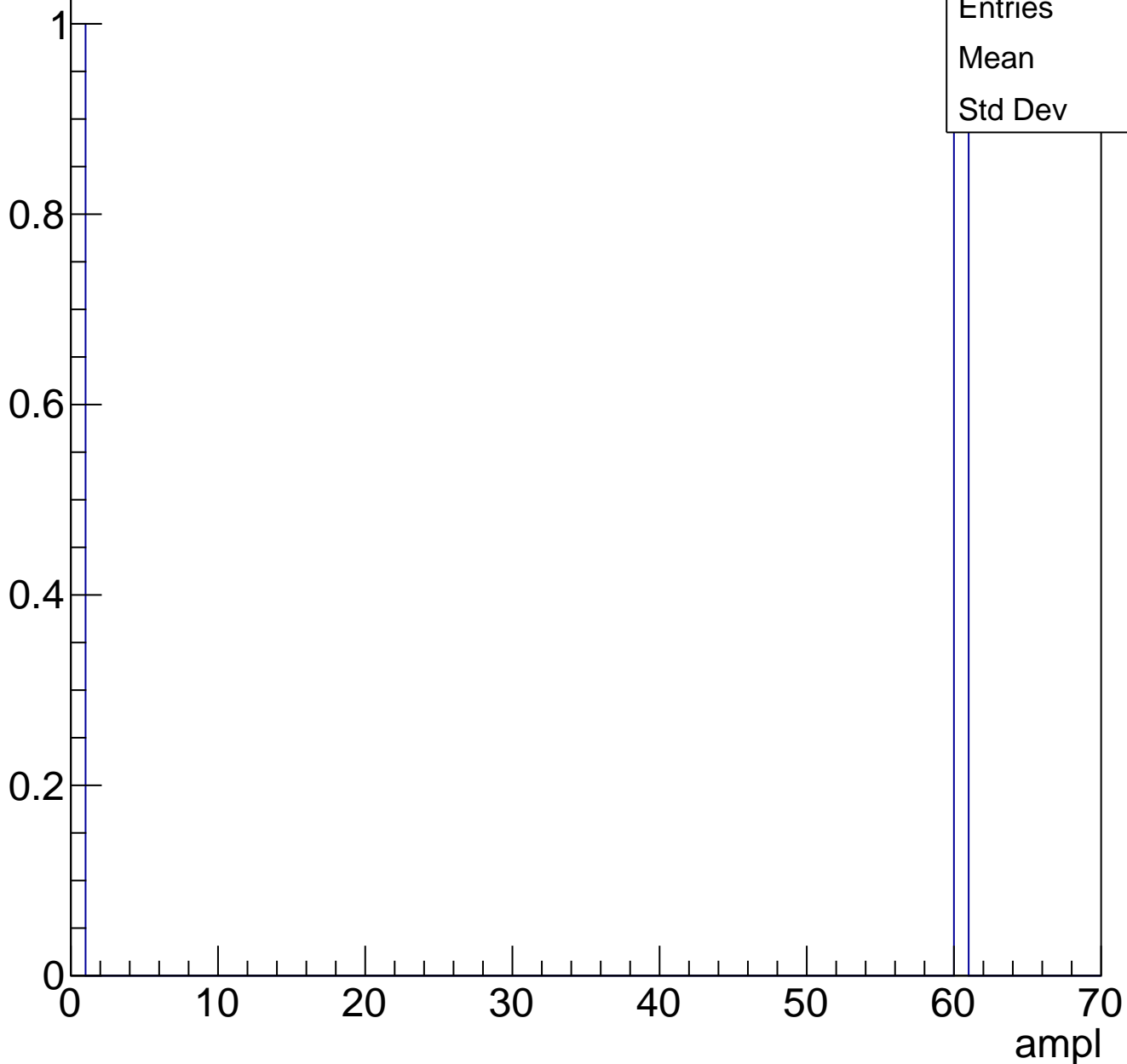




# B1L102S, U21-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch62, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	88
Mean	27.72
Std Dev	6.385

**Gaus mean : 29.1008**

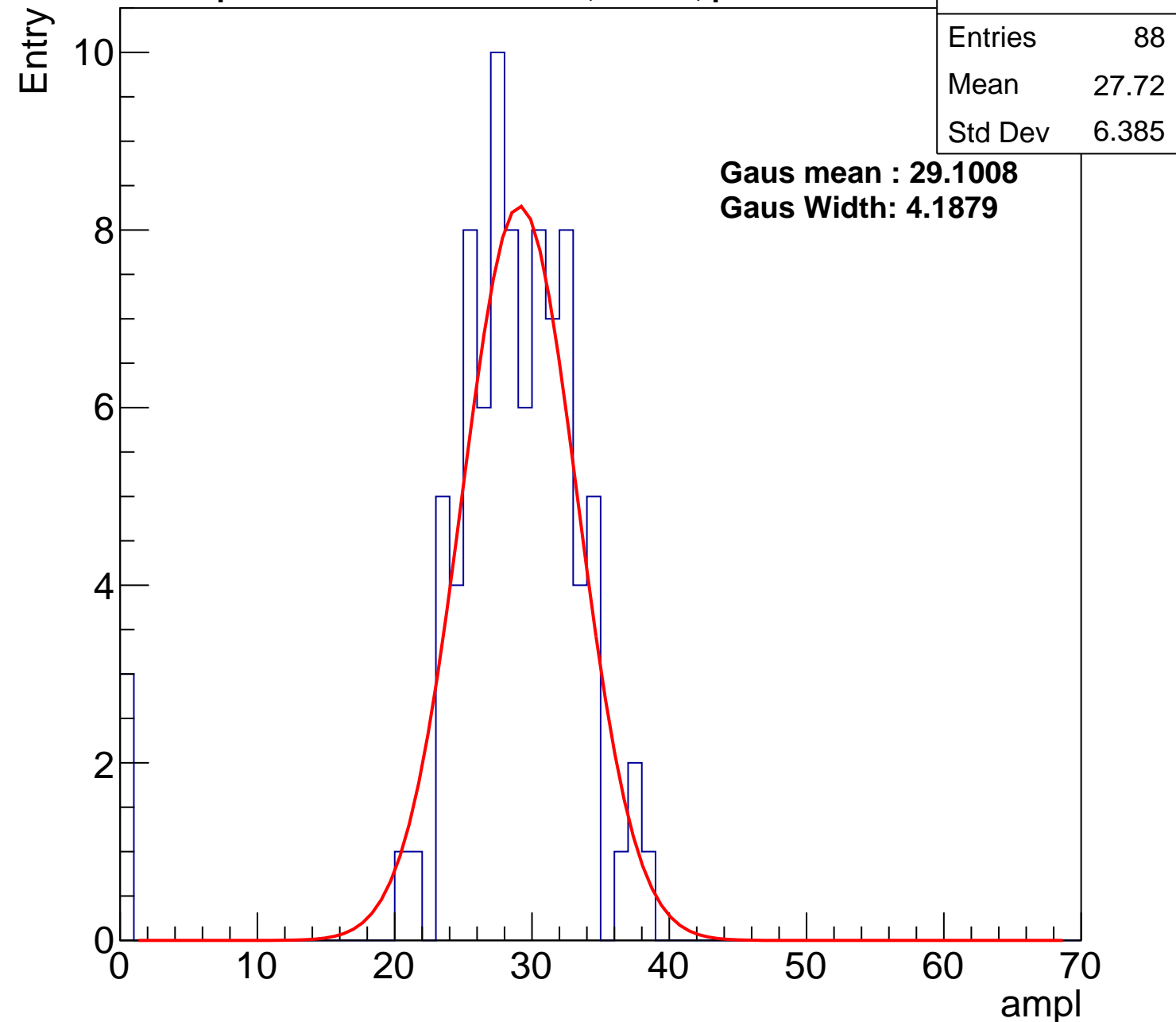
**Gaus Width: 4.1879**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U21-ch62, adc1

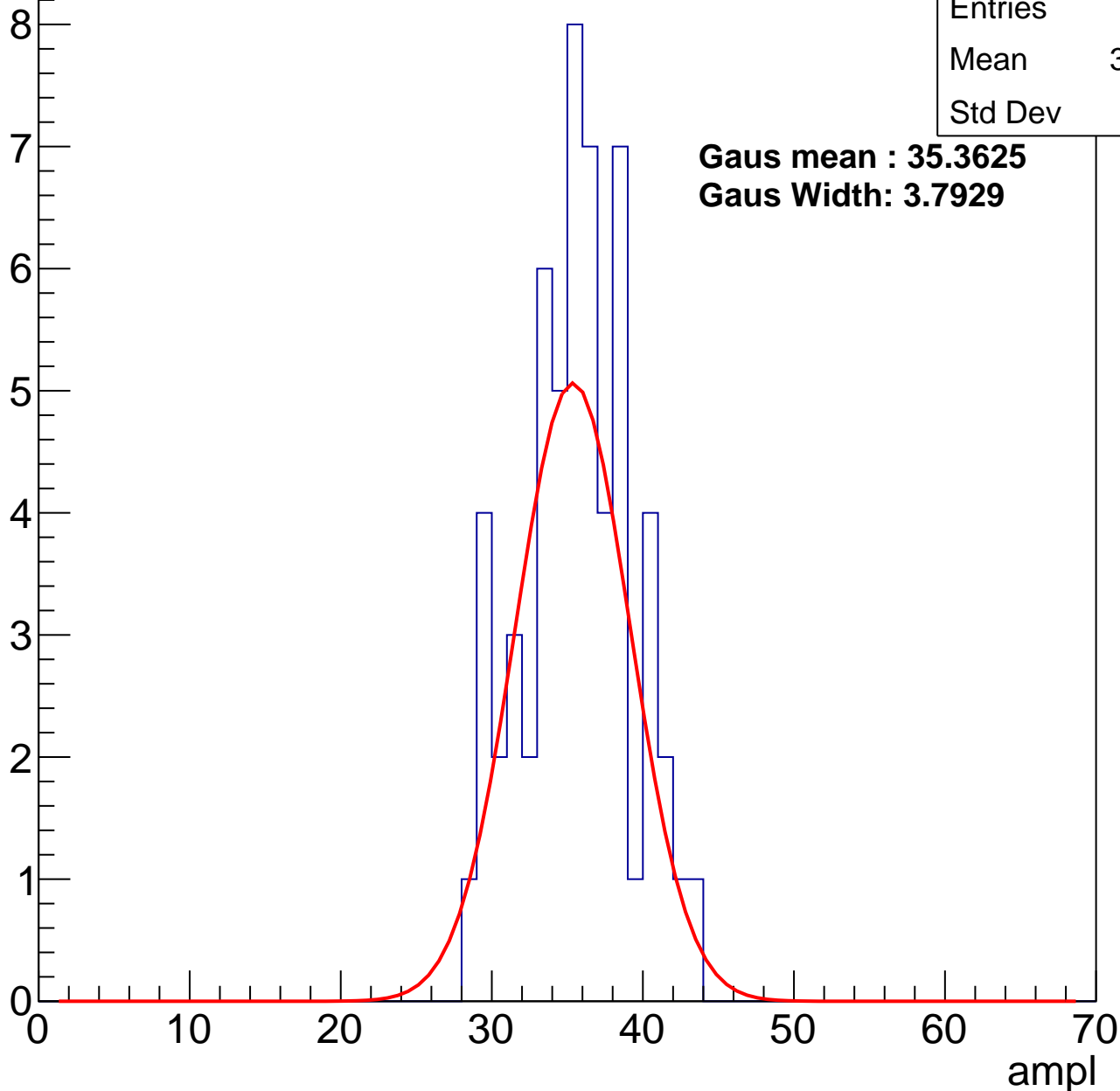
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	35.19
Std Dev	3.53

**Gaus mean : 35.3625**

**Gaus Width: 3.7929**



# B1L102S, U21-ch62, adc2

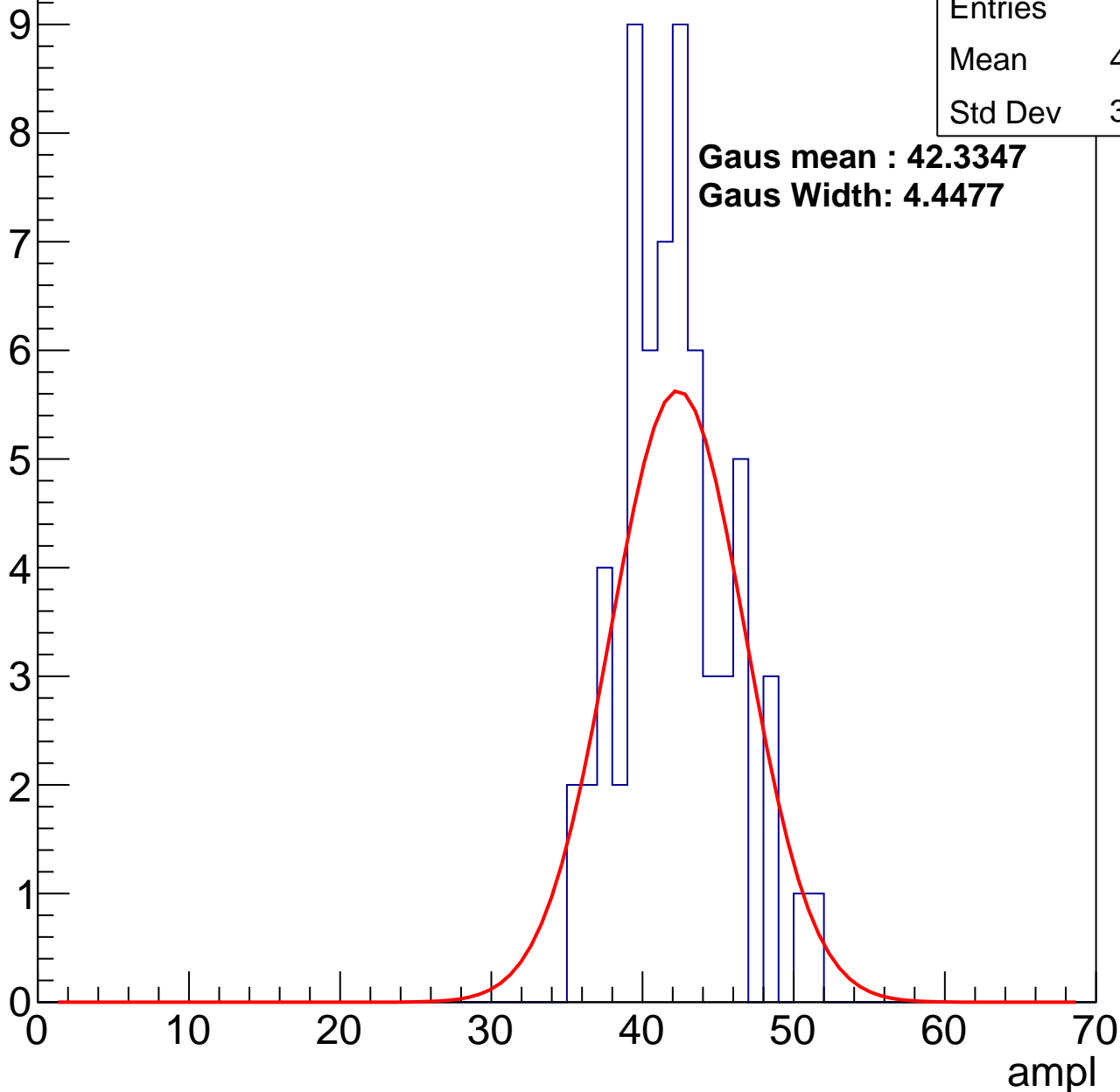
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	41.62
Std Dev	3.525

**Gaus mean : 42.3347**

**Gaus Width: 4.4477**

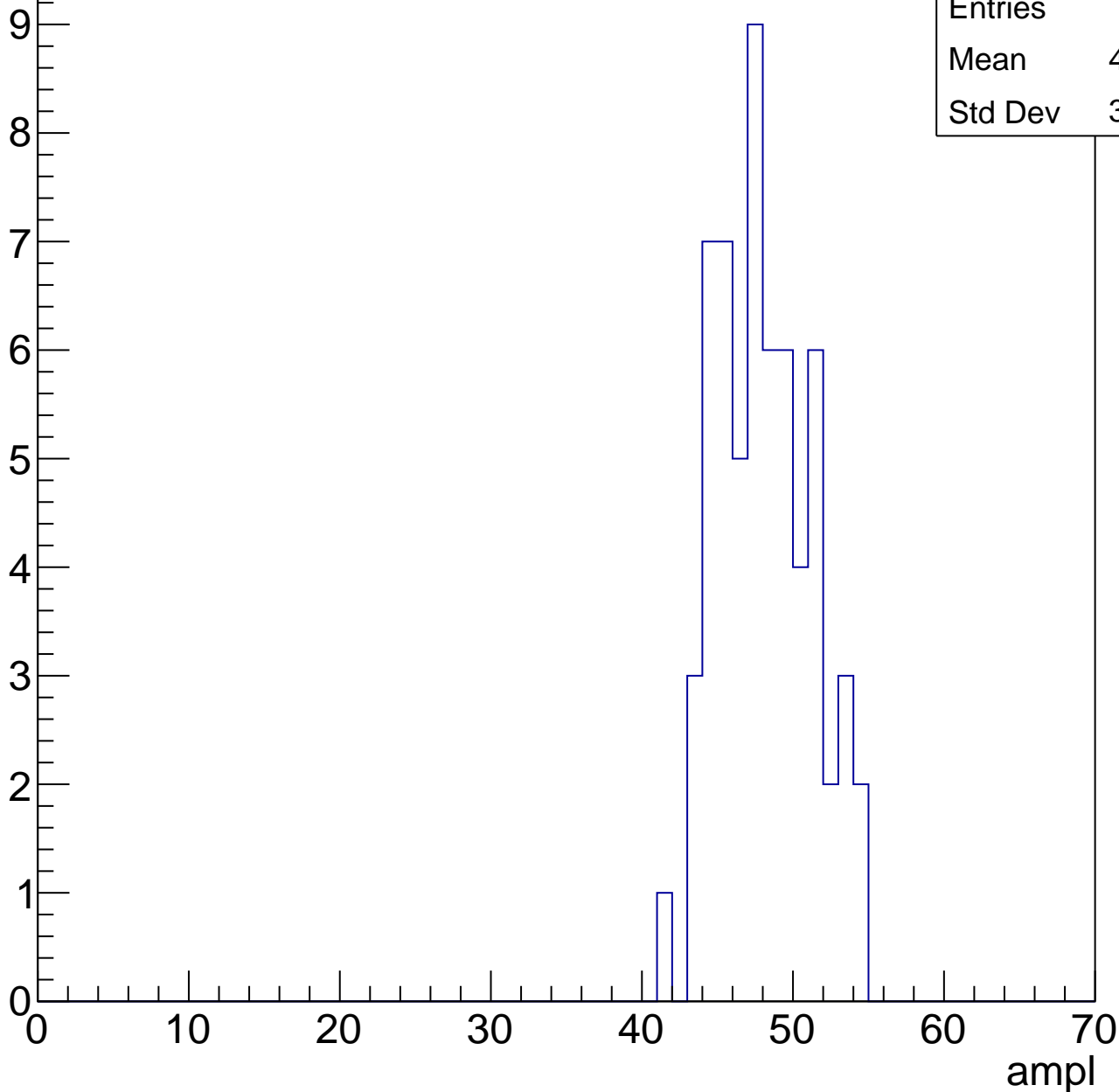


# B1L102S, U21-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	47.62
Std Dev	3.068

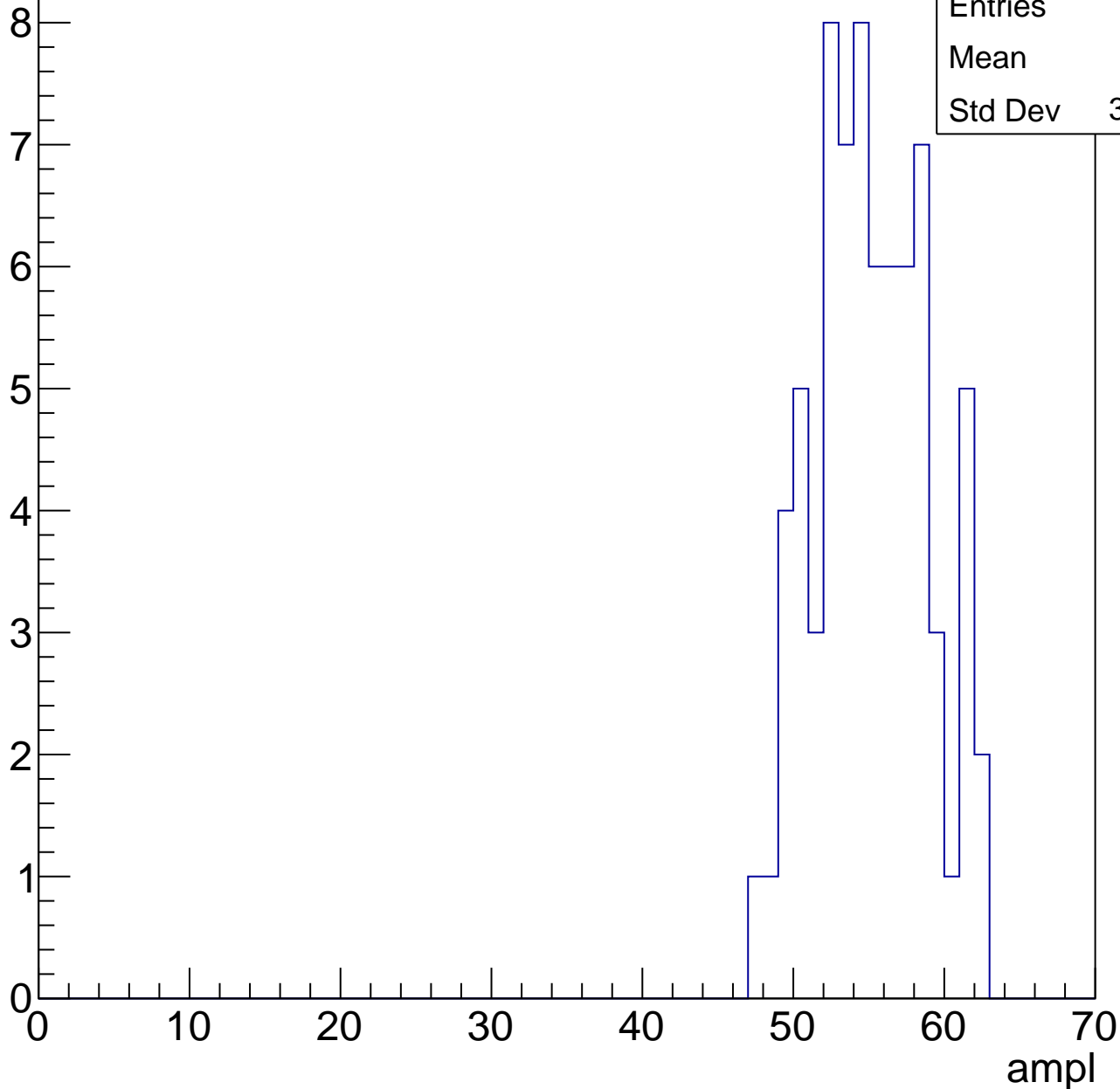


# B1L102S, U21-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	54.7
Std Dev	3.655

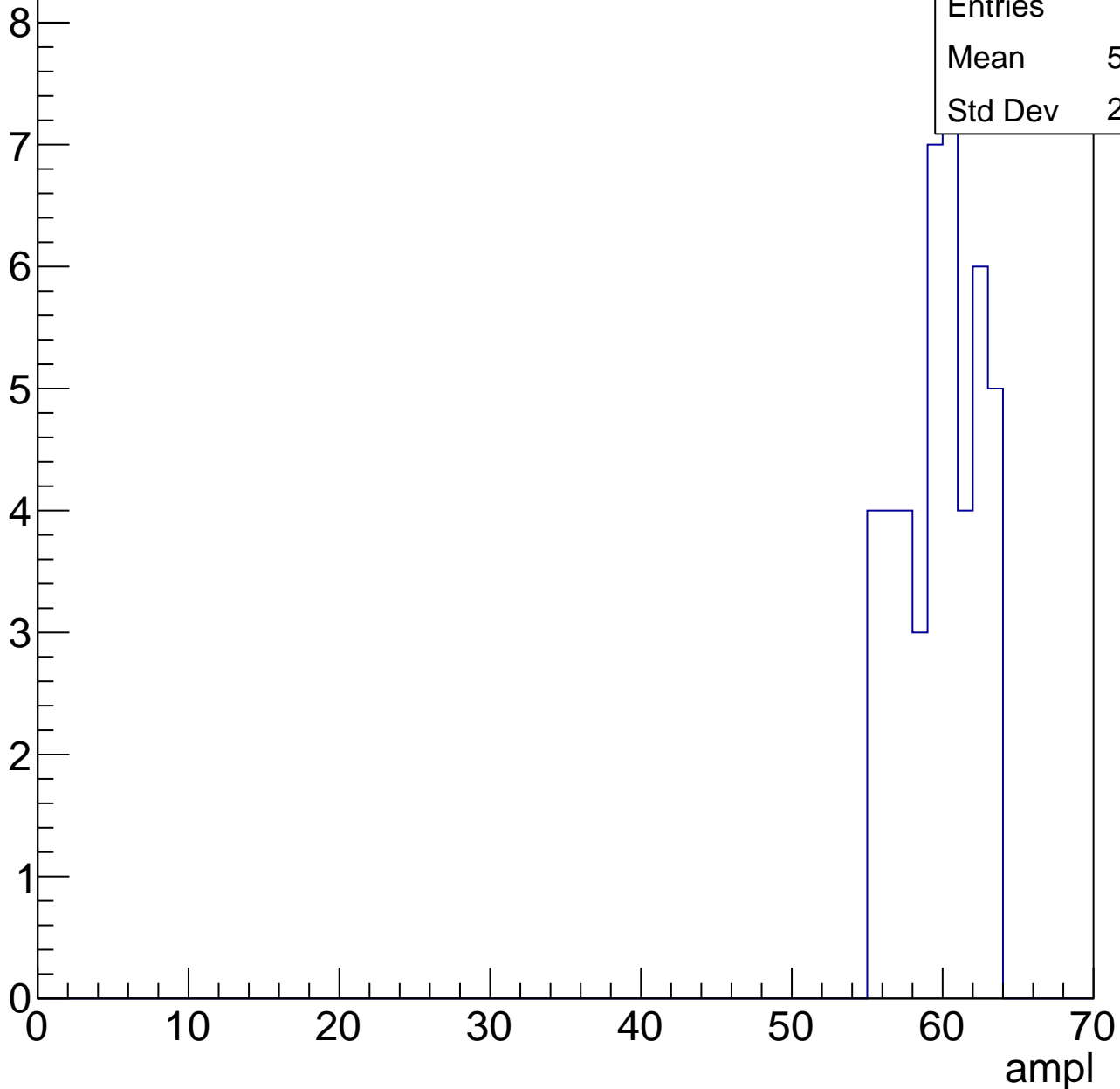


# B1L102S, U21-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	59.33
Std Dev	2.459

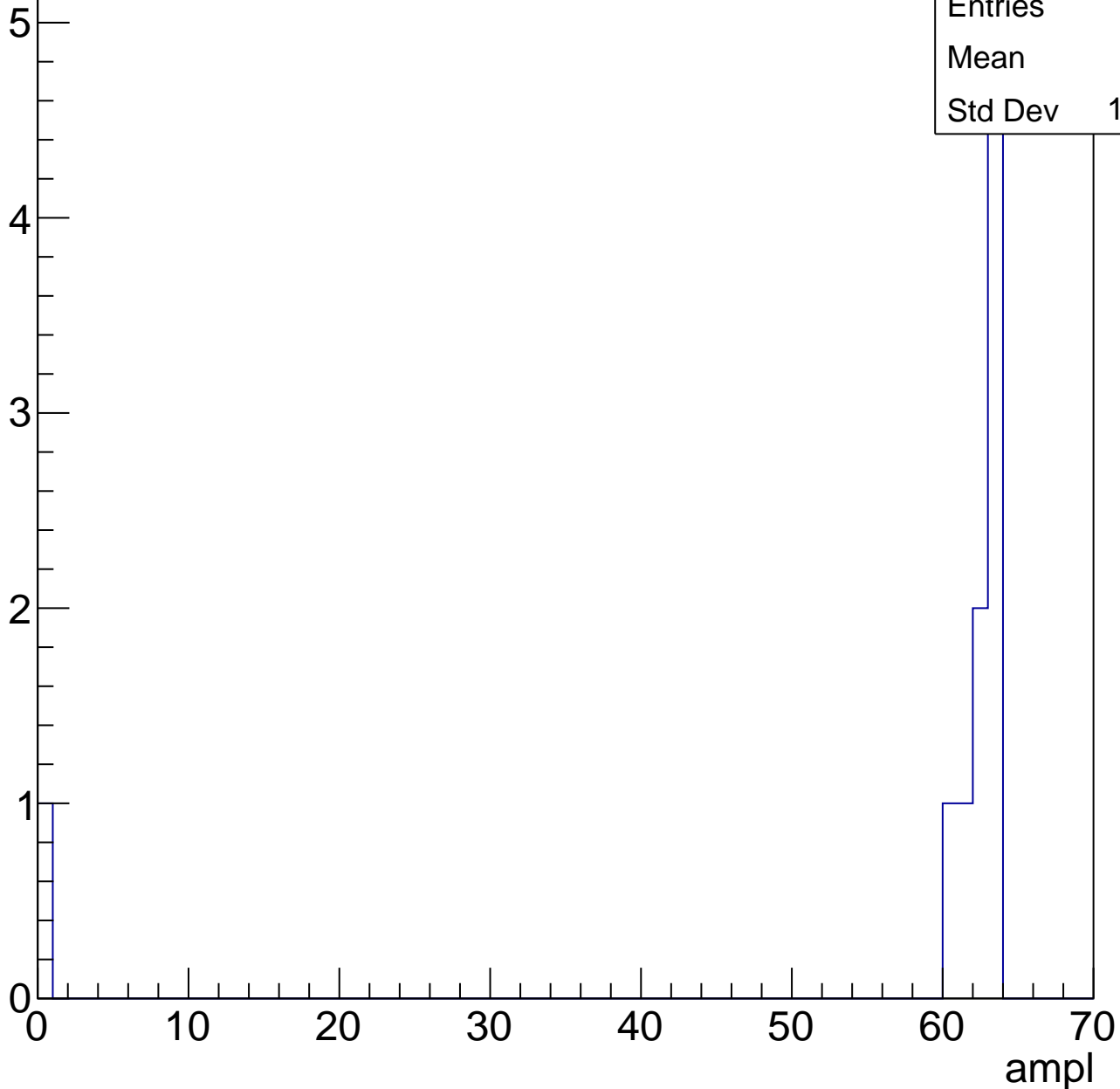


# B1L102S, U21-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	10
Mean	56
Std Dev	18.69





# B1L102S, U21-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U21-ch63, adc0

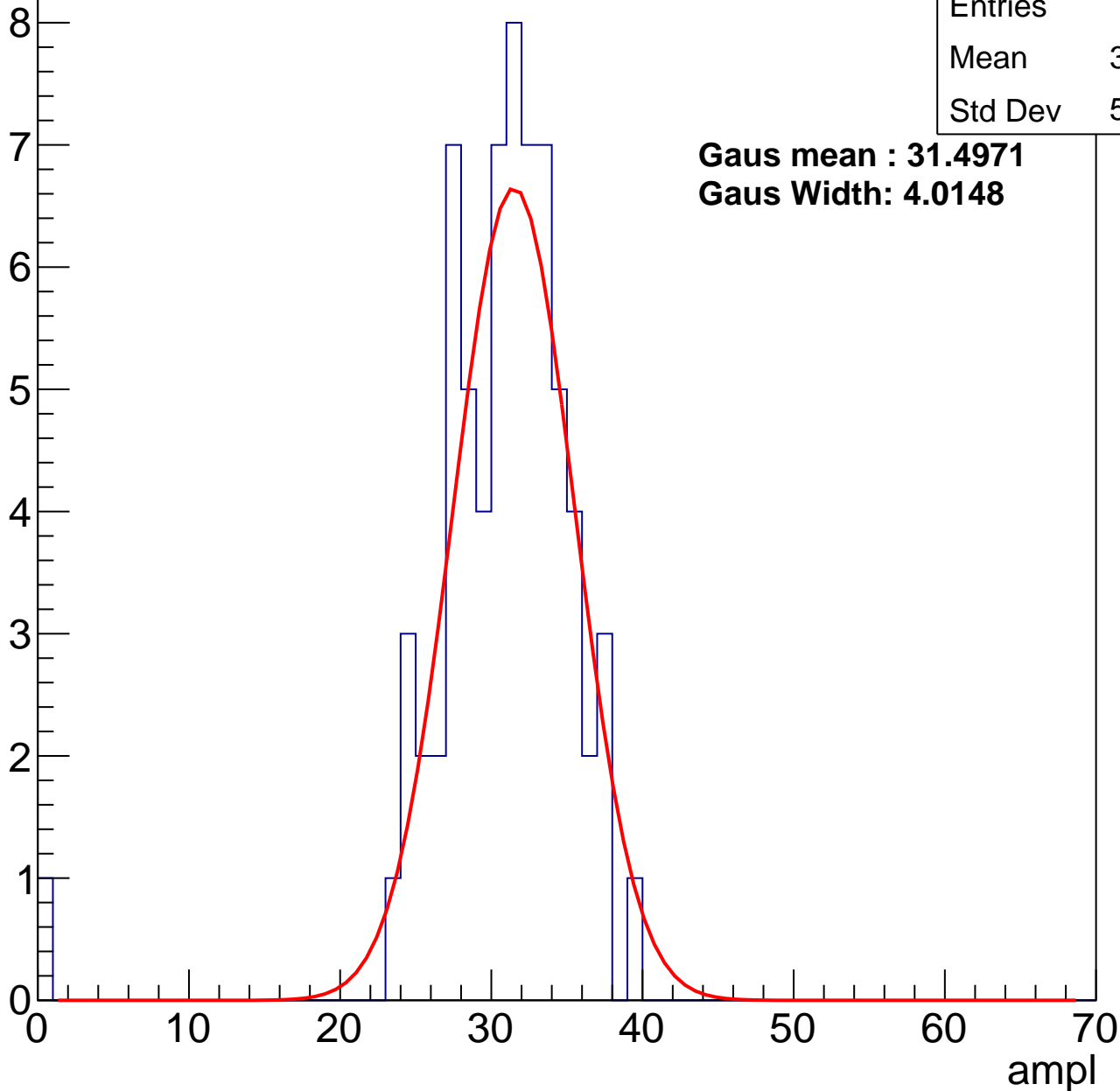
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	30.25
Std Dev	5.109

**Gaus mean : 31.4971**

**Gaus Width: 4.0148**



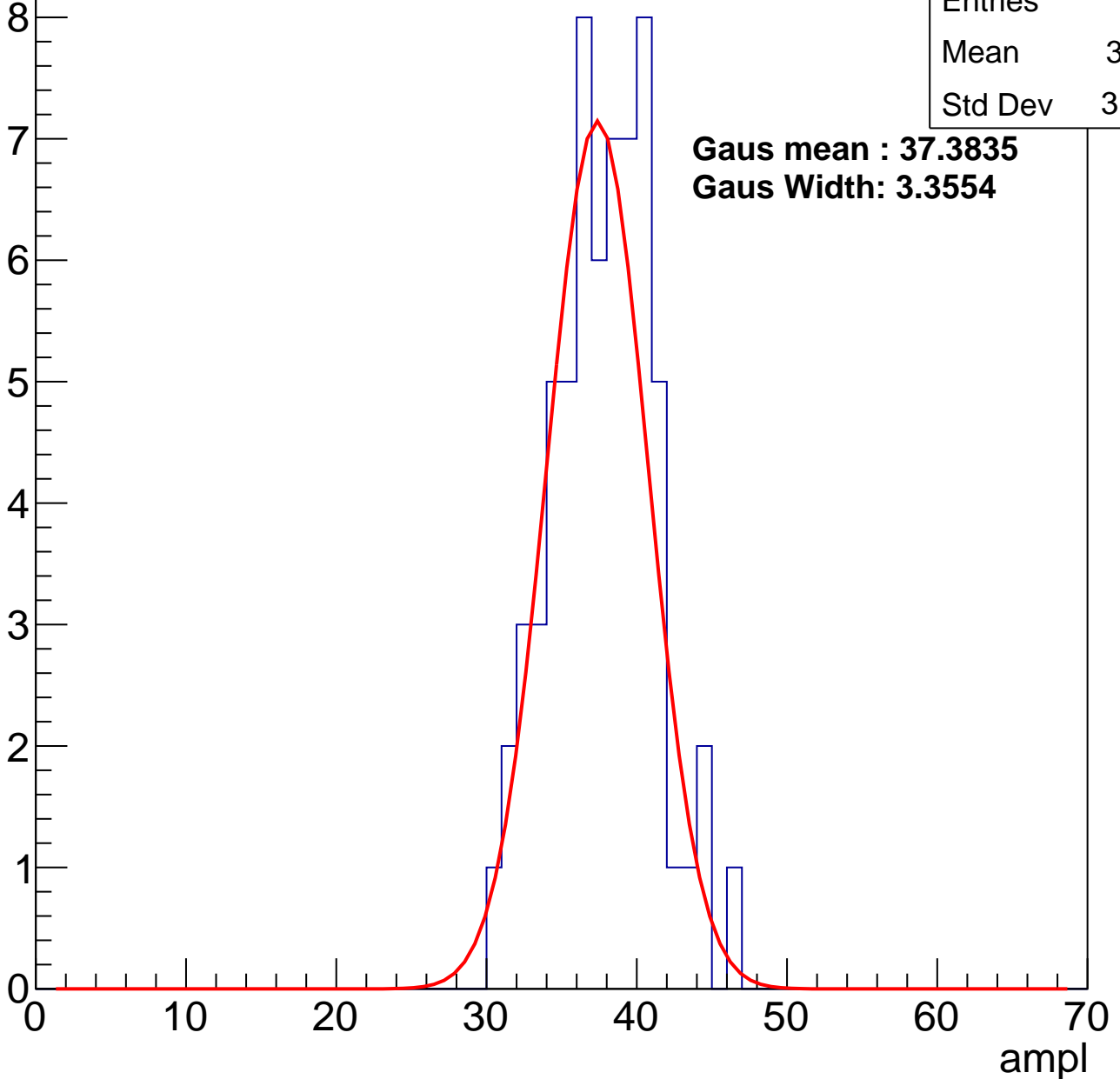
# B1L102S, U21-ch63, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	37.31
Std Dev	3.369

**Gaus mean : 37.3835**  
**Gaus Width: 3.3554**



# B1L102S, U21-ch63, adc2

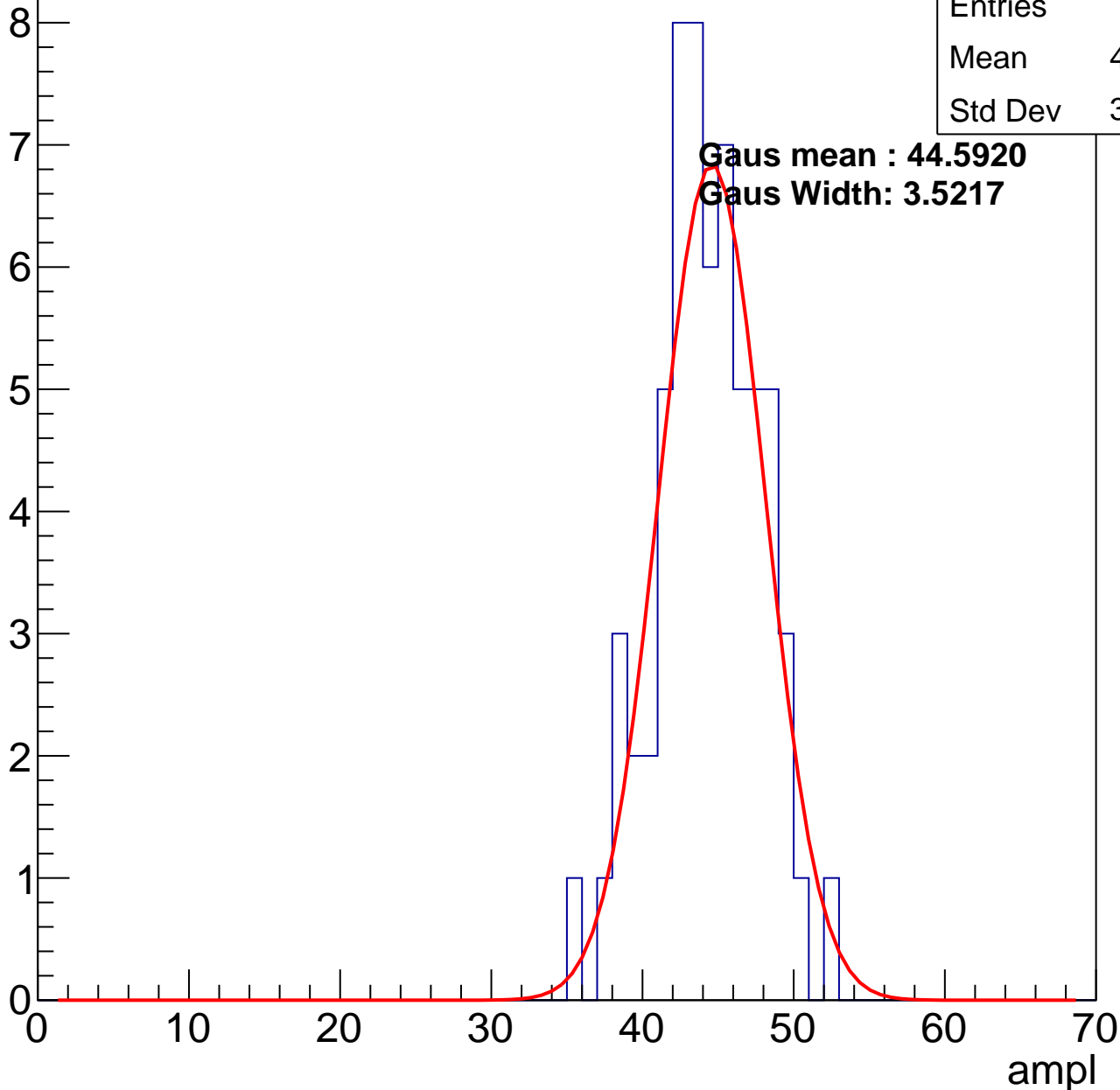
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	43.84
Std Dev	3.405

**Gaus mean : 44.5920**

**Gaus Width: 3.5217**

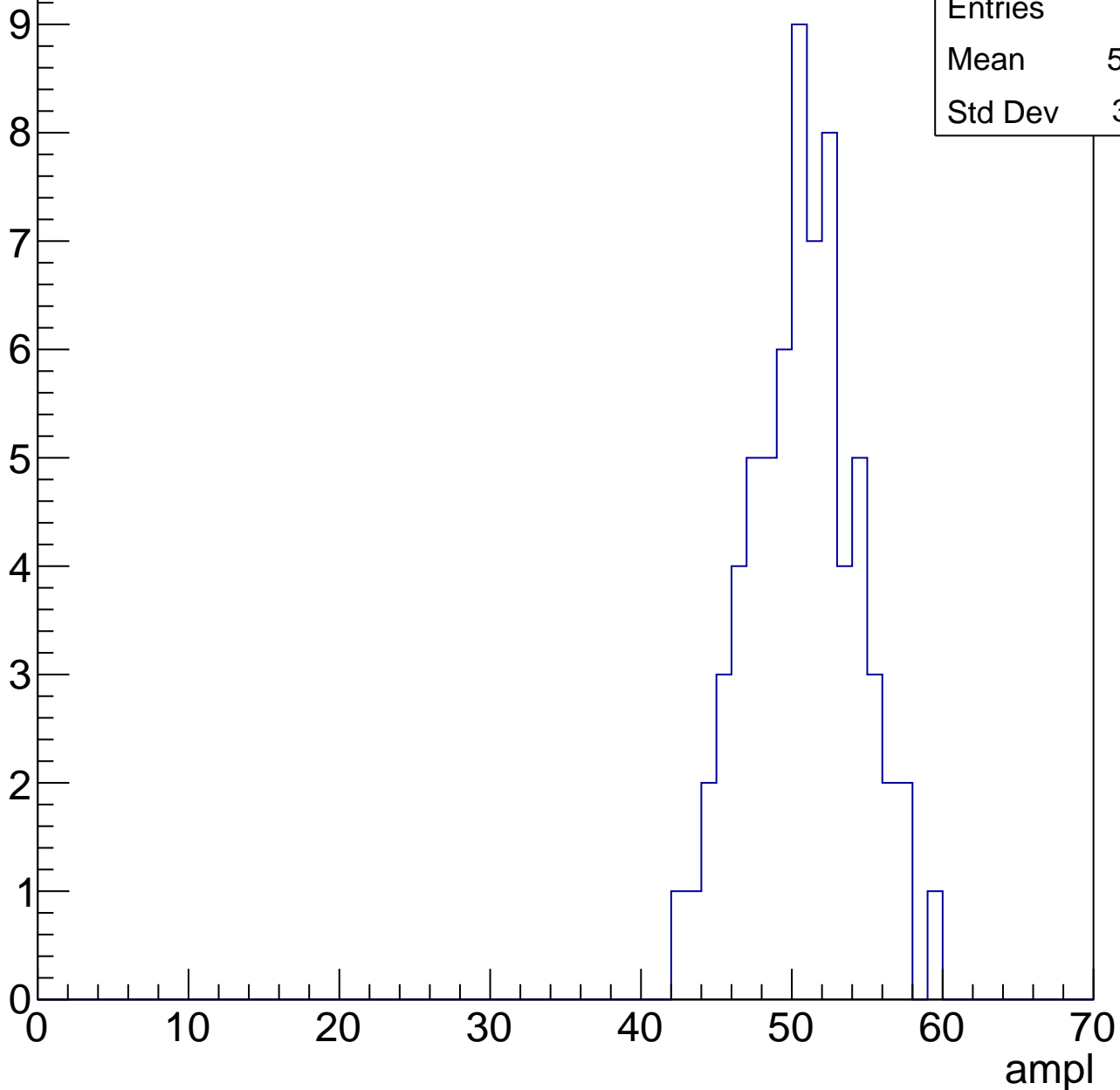


# B1L102S, U21-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	50.24
Std Dev	3.581

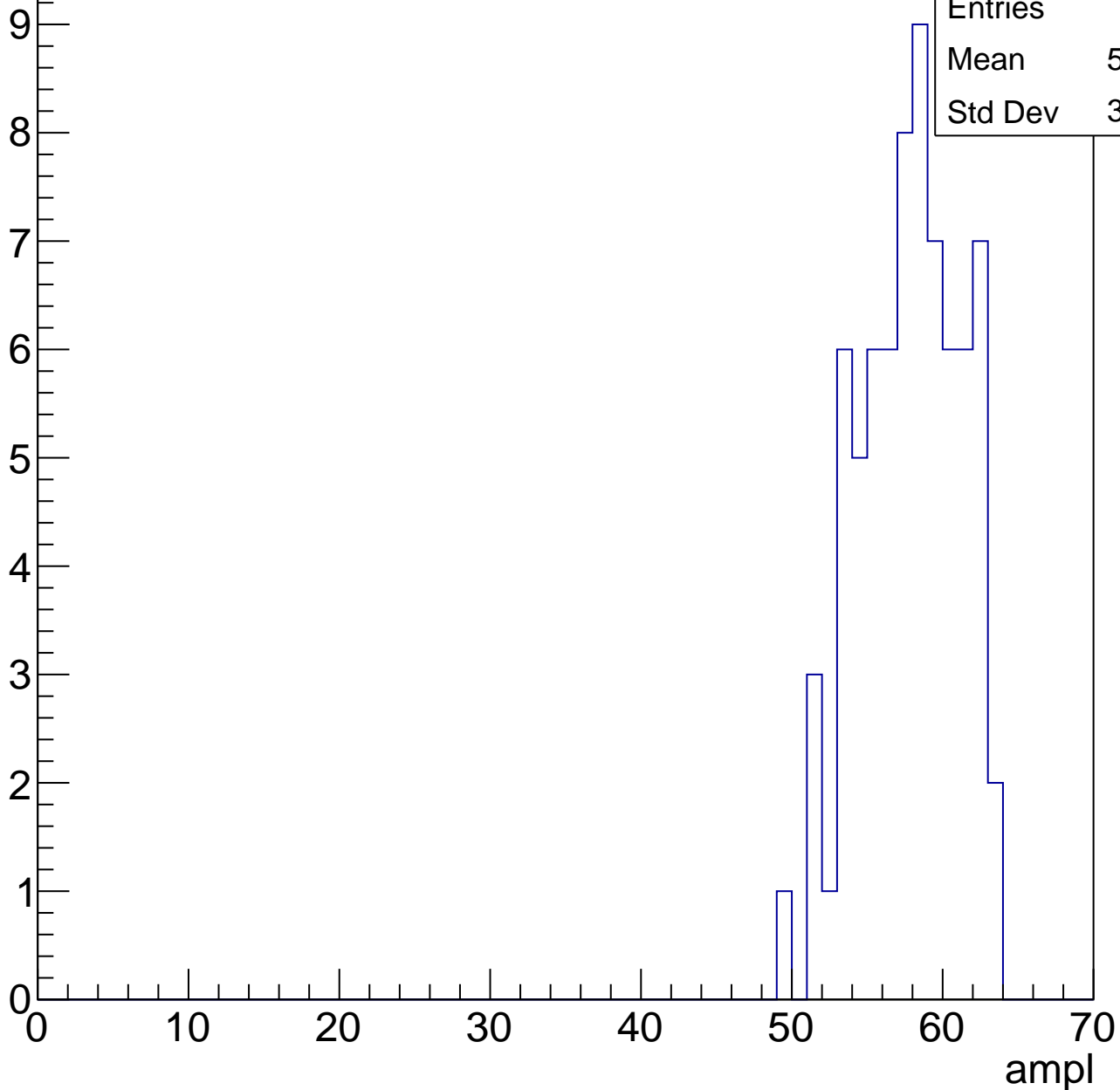


# B1L102S, U21-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	57.33
Std Dev	3.298

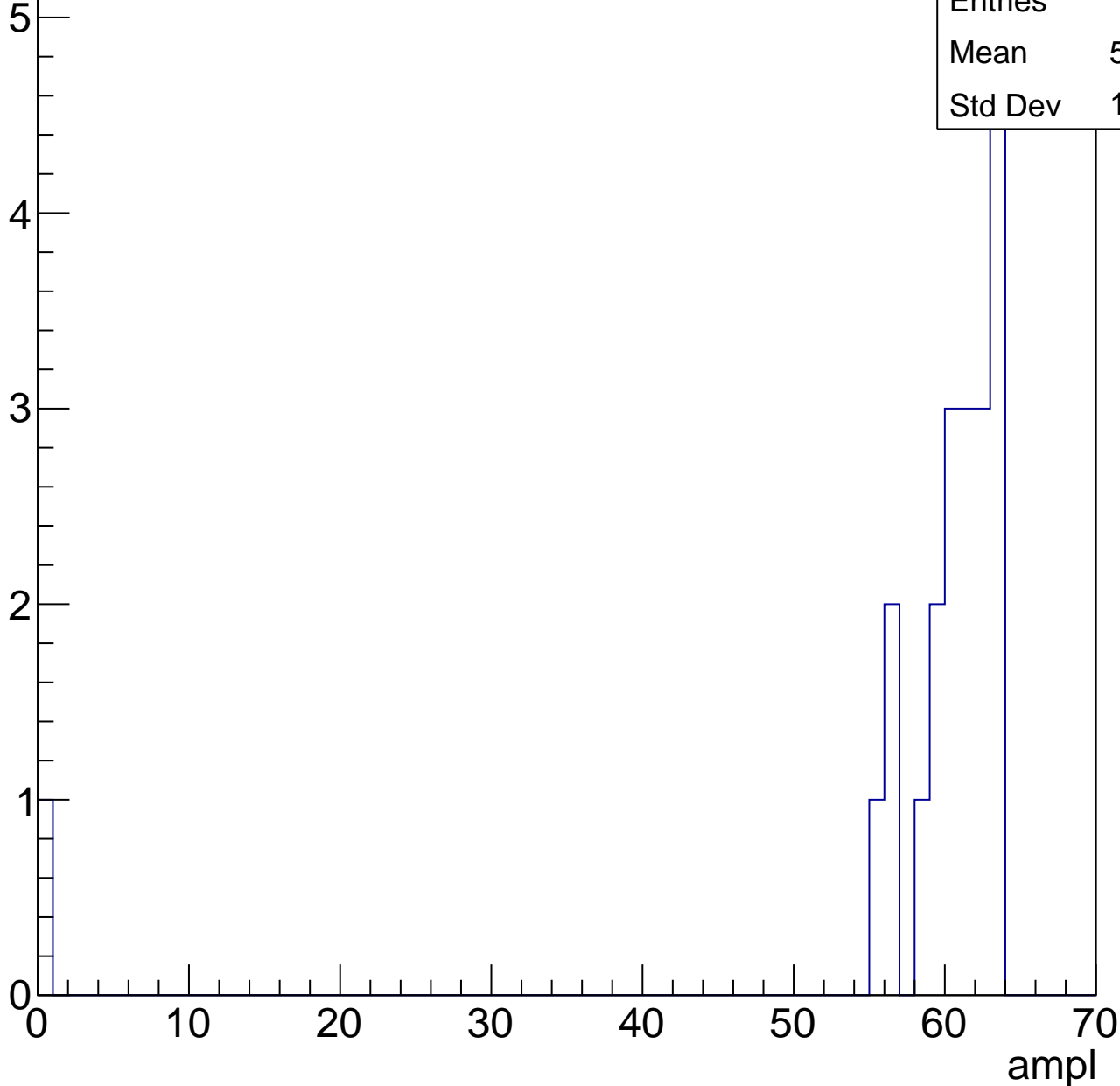


# B1L102S, U21-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	21
Mean	57.48
Std Dev	13.07



# B1L102S, U21-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U21-ch64, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	86
Mean	29.31
Std Dev	4.828

**Gaus mean : 29.6305**

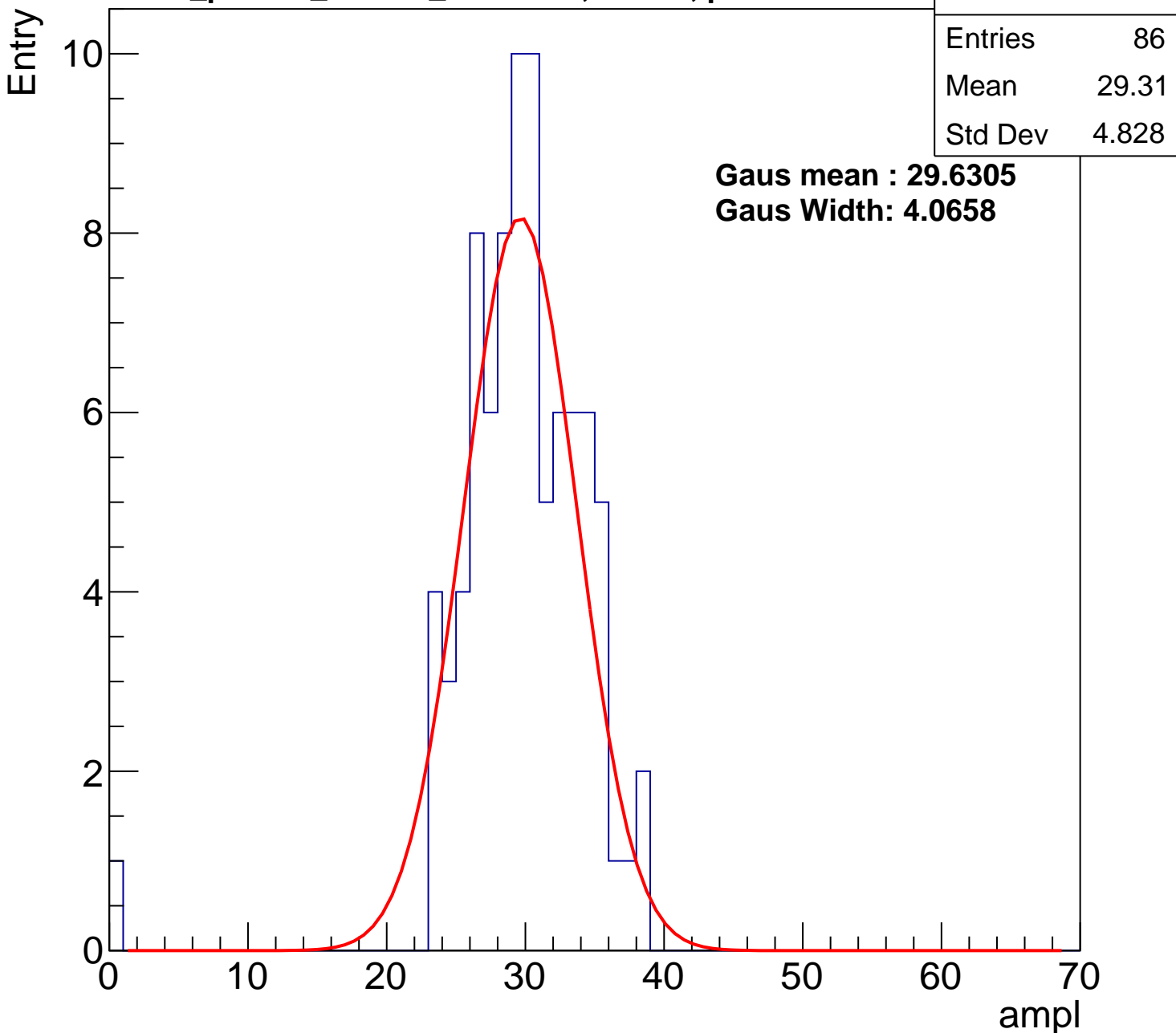
**Gaus Width: 4.0658**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U21-ch64, adc1

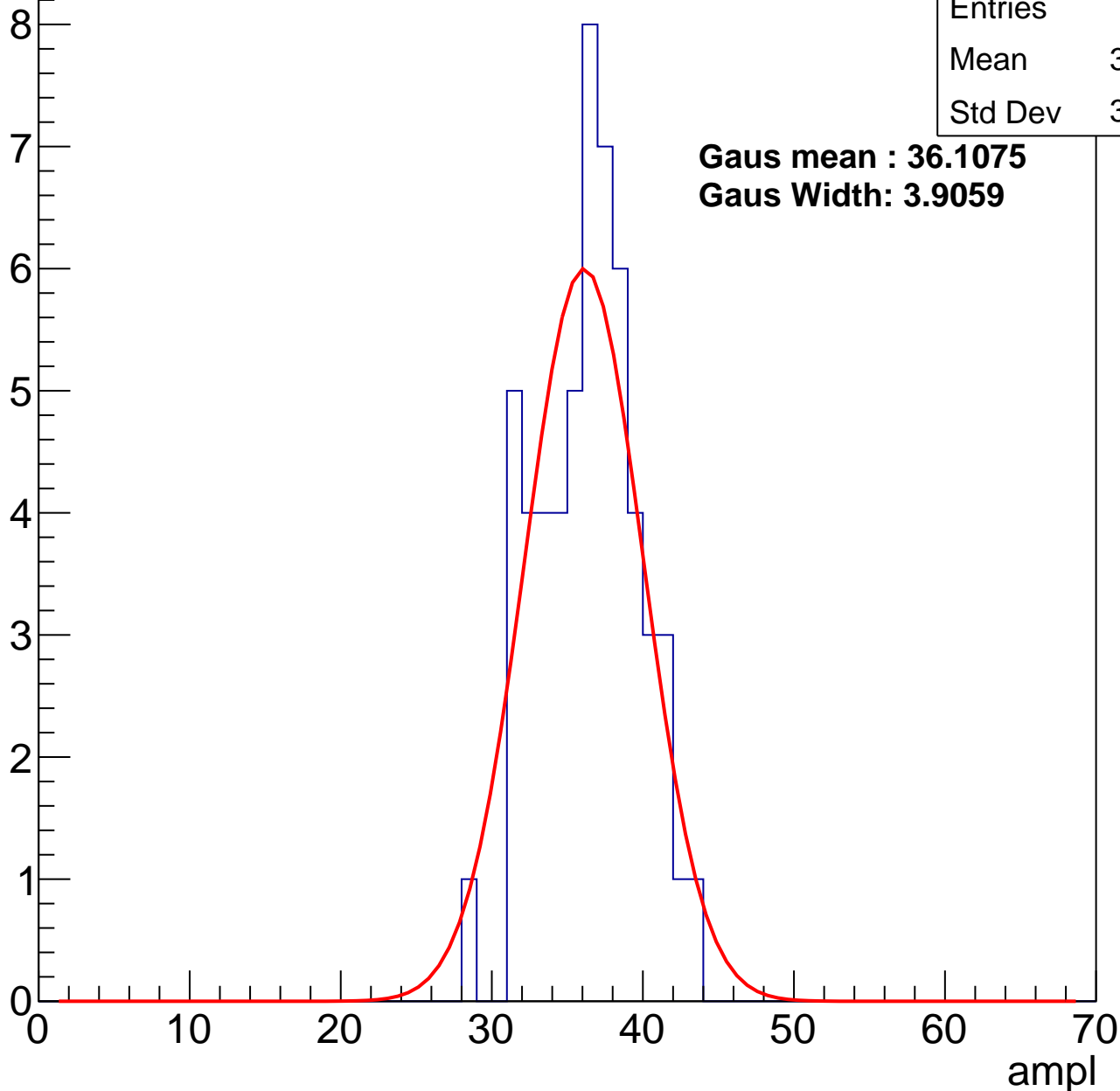
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	35.95
Std Dev	3.232

**Gaus mean : 36.1075**

**Gaus Width: 3.9059**



# B1L102S, U21-ch64, adc2

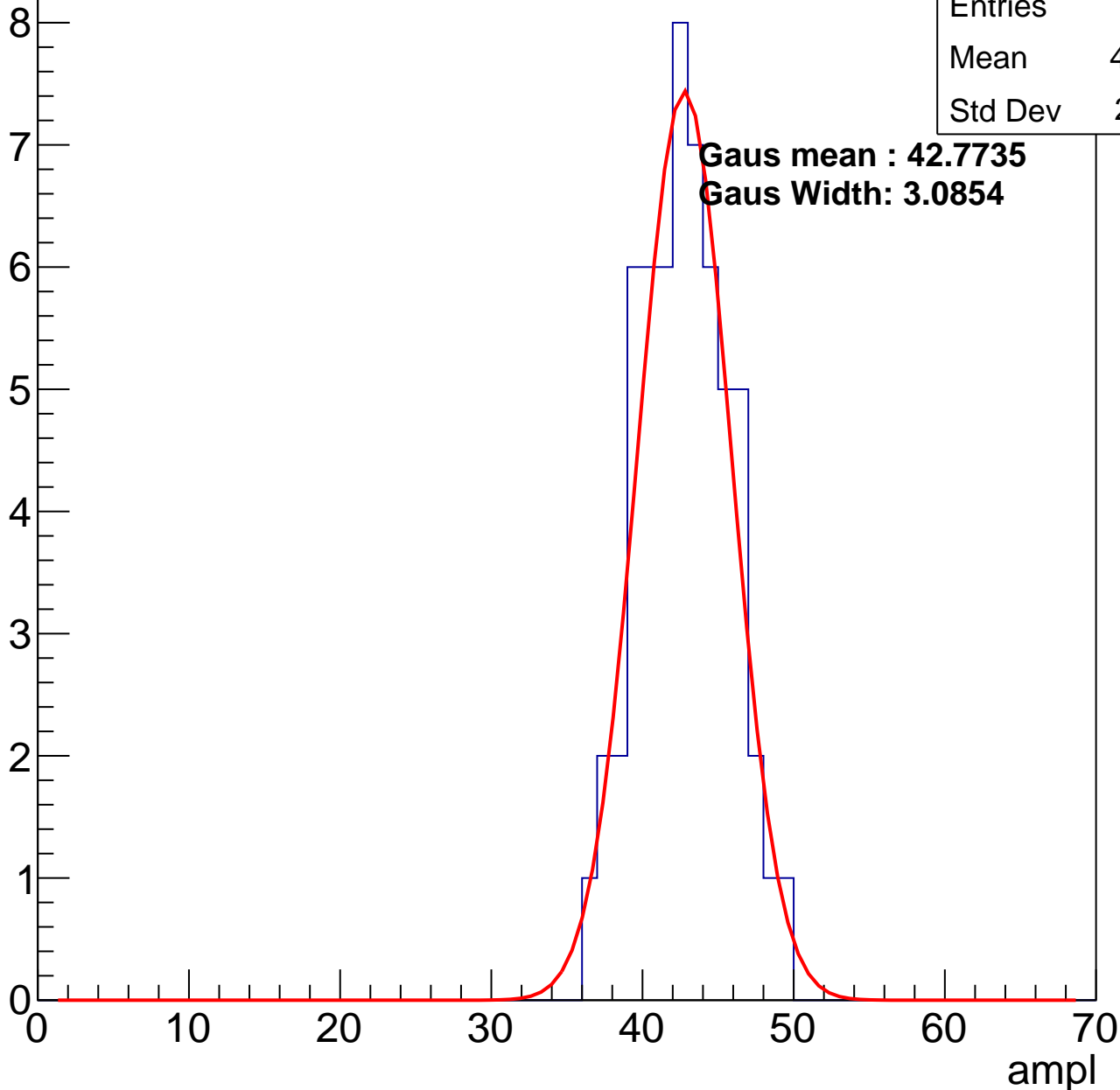
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	42.29
Std Dev	2.901

**Gaus mean : 42.7735**

**Gaus Width: 3.0854**

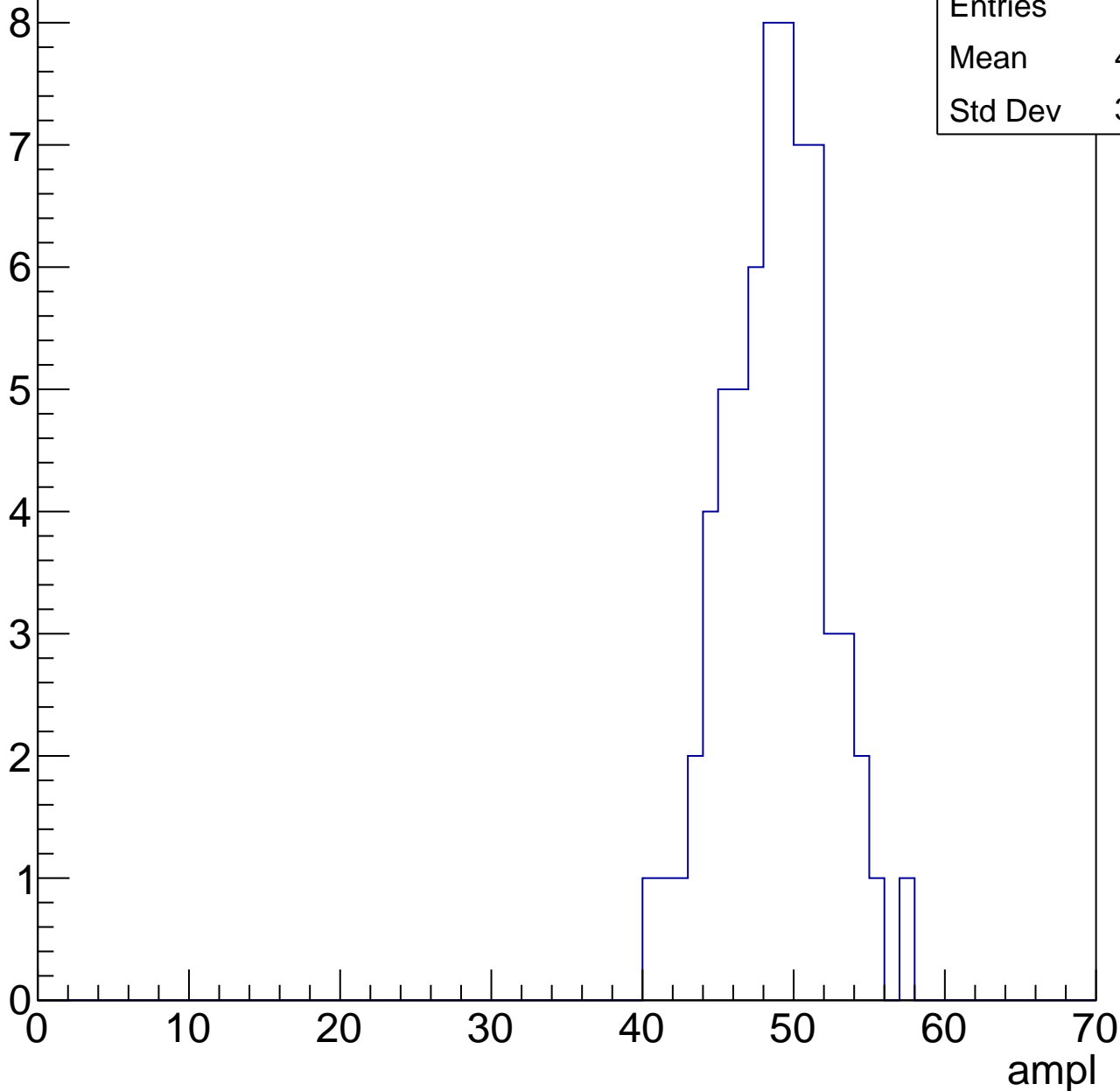


# B1L102S, U21-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	48.31
Std Dev	3.401

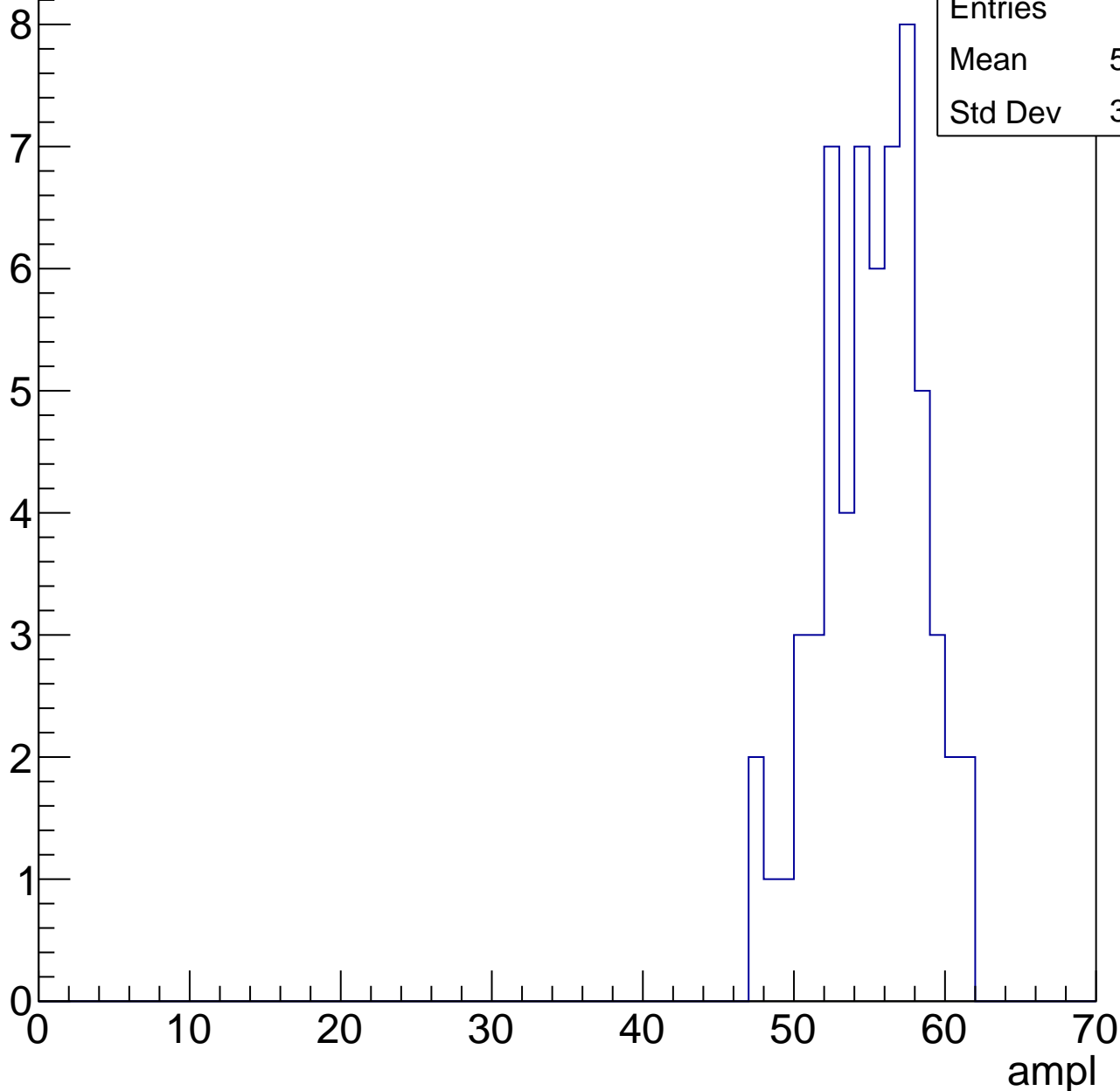


# B1L102S, U21-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	54.67
Std Dev	3.313

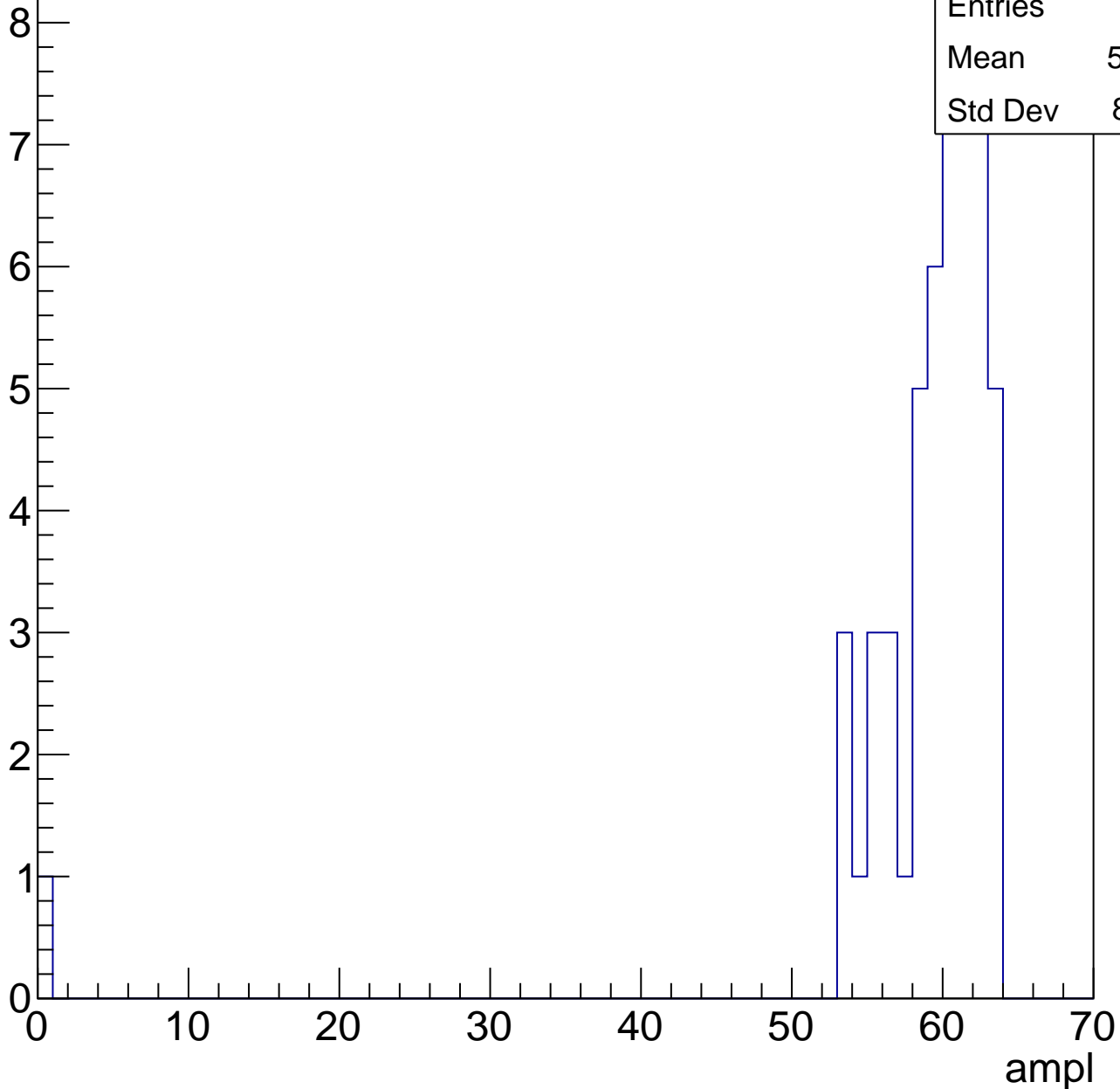


# B1L102S, U21-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	58.19
Std Dev	8.611

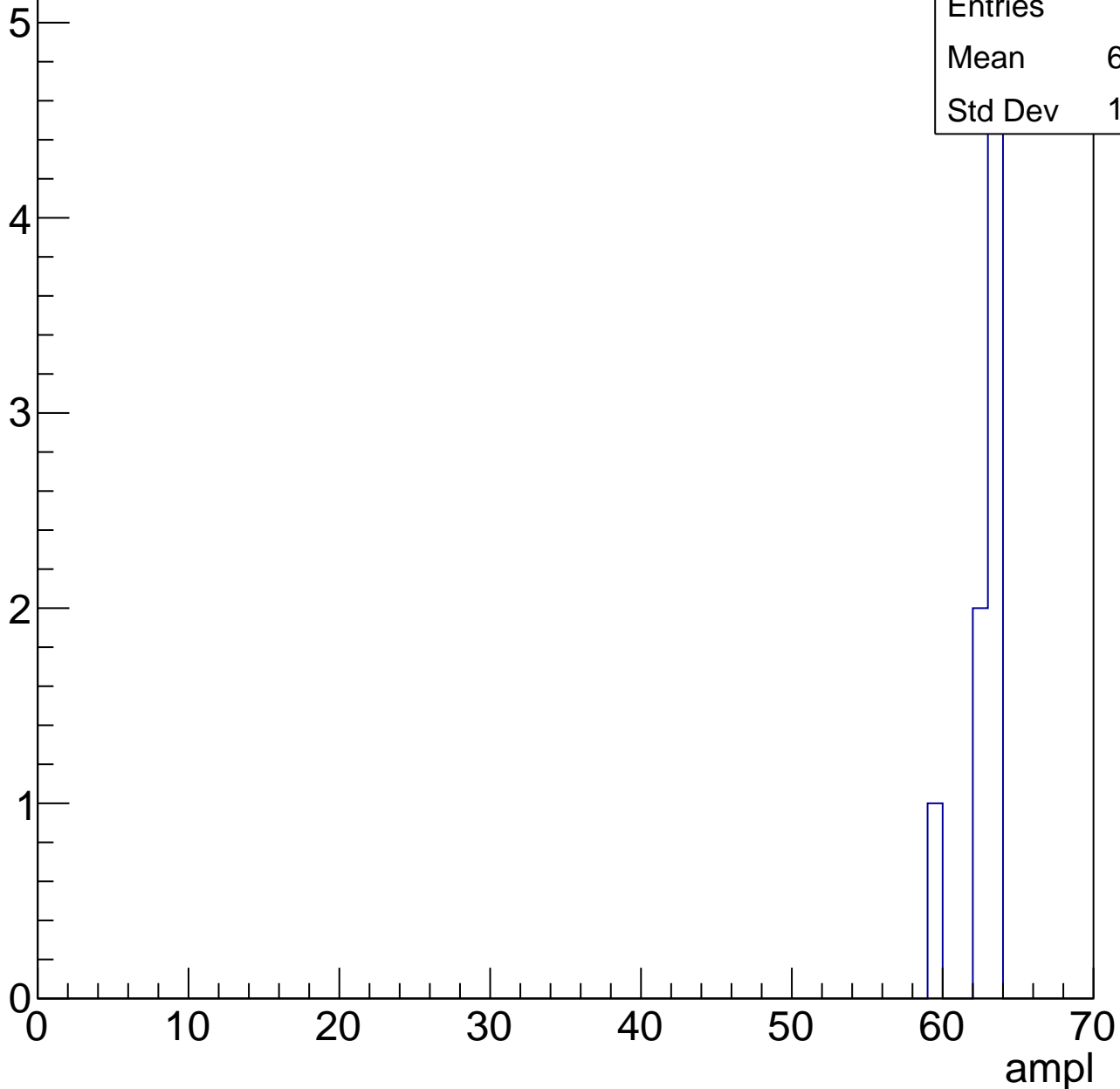


# B1L102S, U21-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	8
Mean	62.25
Std Dev	1.299





# B1L102S, U21-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U21-ch65, adc0

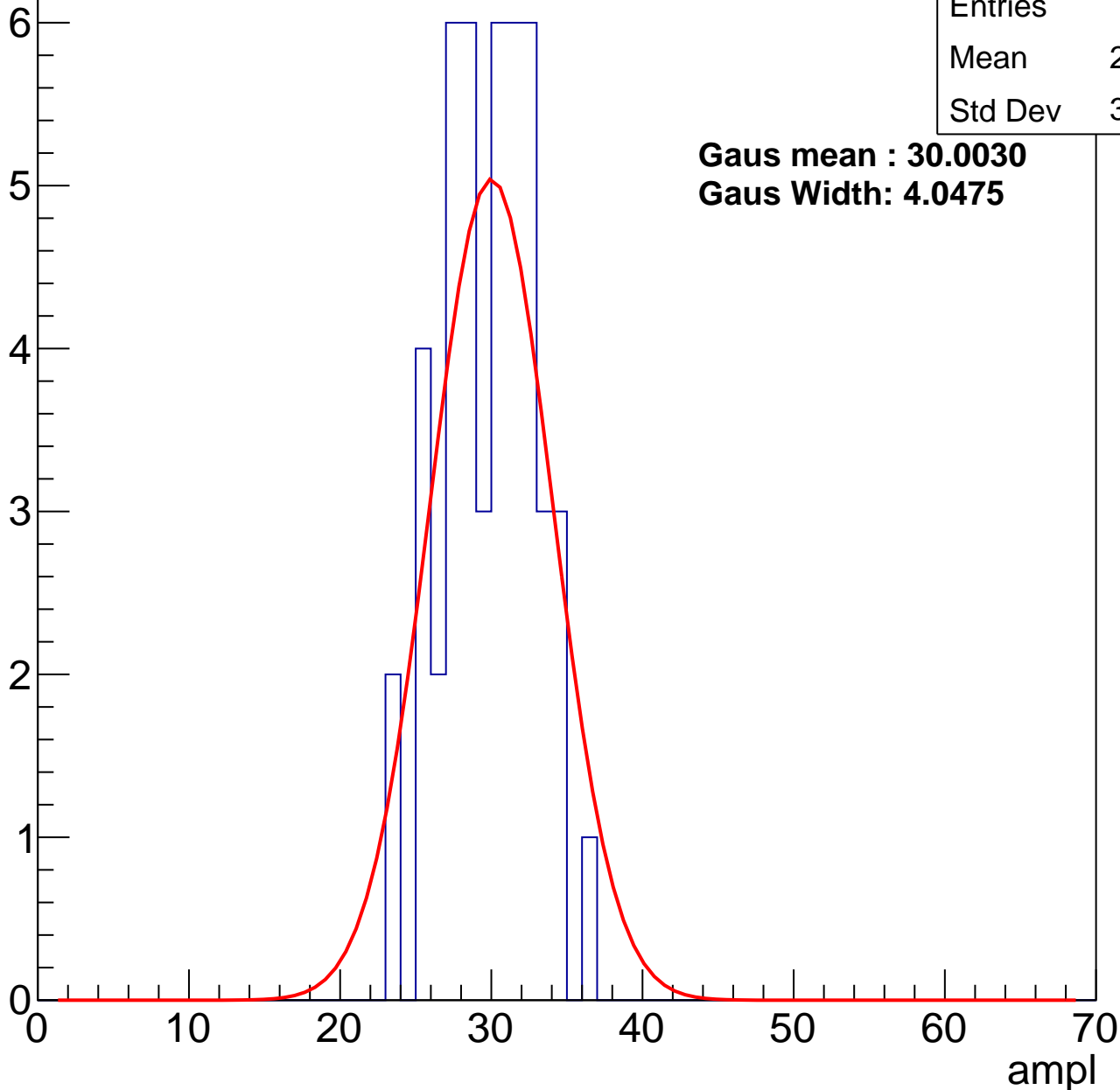
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	29.38
Std Dev	3.004

**Gaus mean : 30.0030**

**Gaus Width: 4.0475**



# B1L102S, U21-ch65, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	78
Mean	36.15
Std Dev	3.84

**Gaus mean : 36.2217**

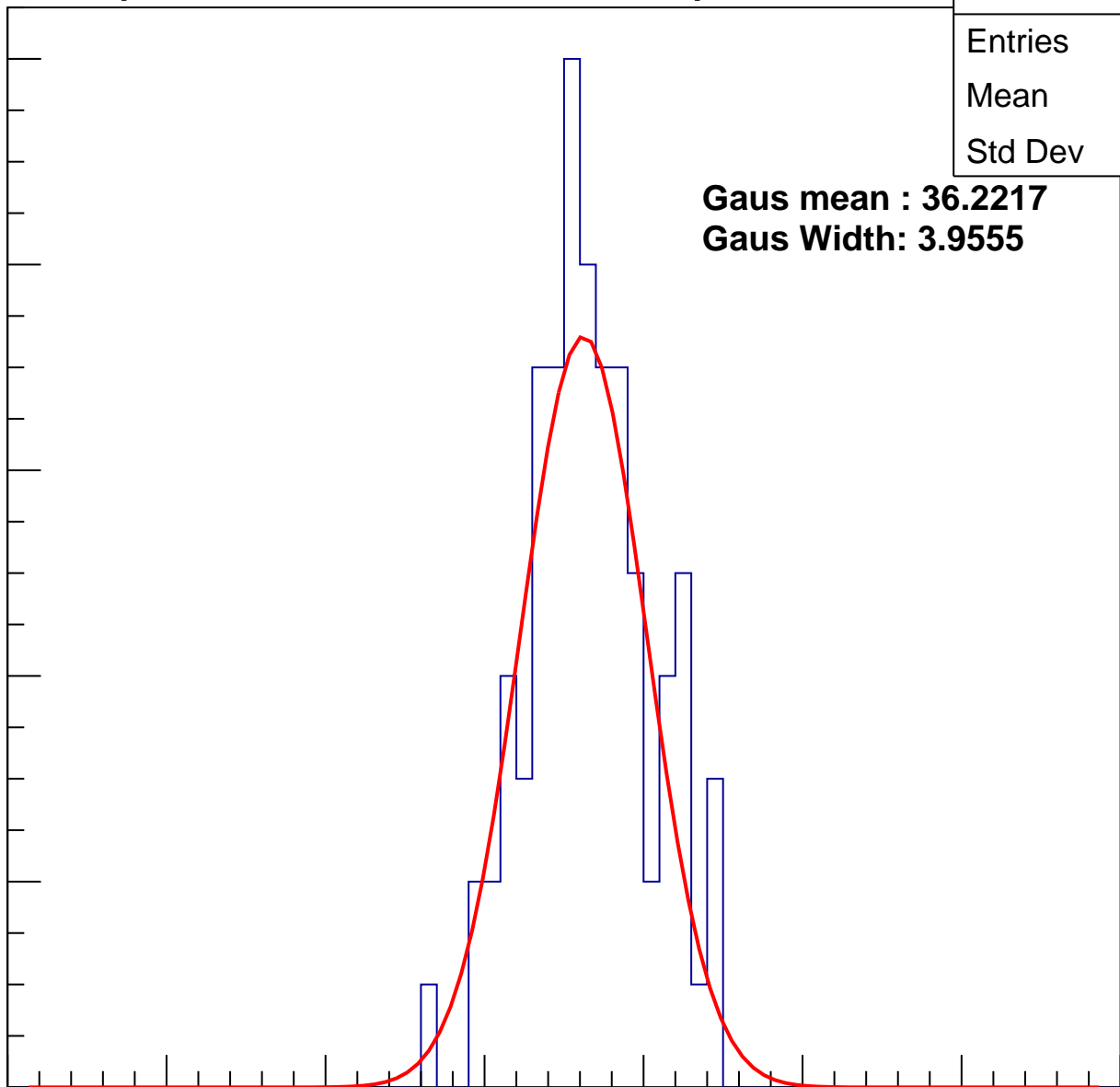
**Gaus Width: 3.9555**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U21-ch65, adc2

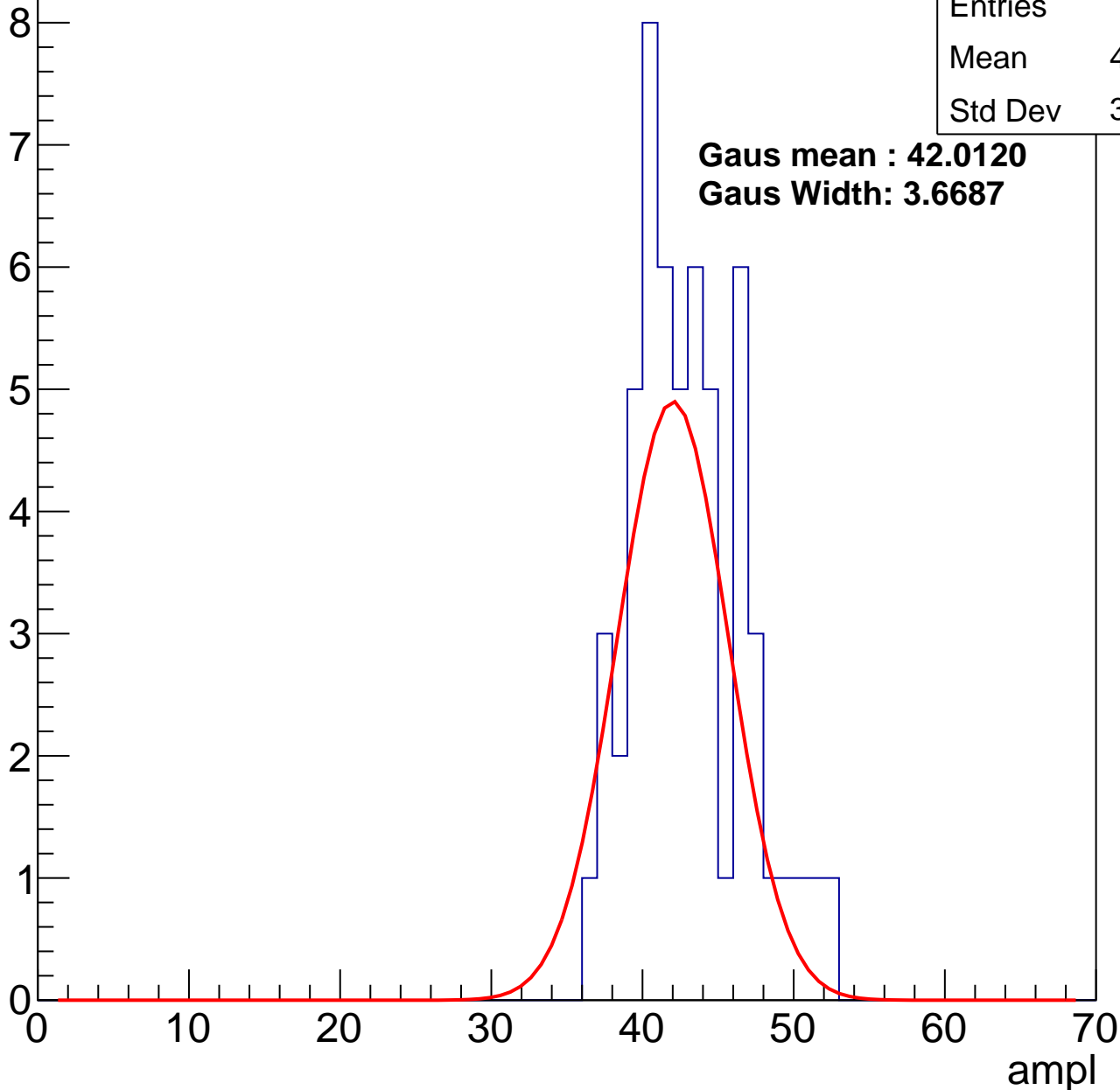
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	42.57
Std Dev	3.644

**Gaus mean : 42.0120**

**Gaus Width: 3.6687**

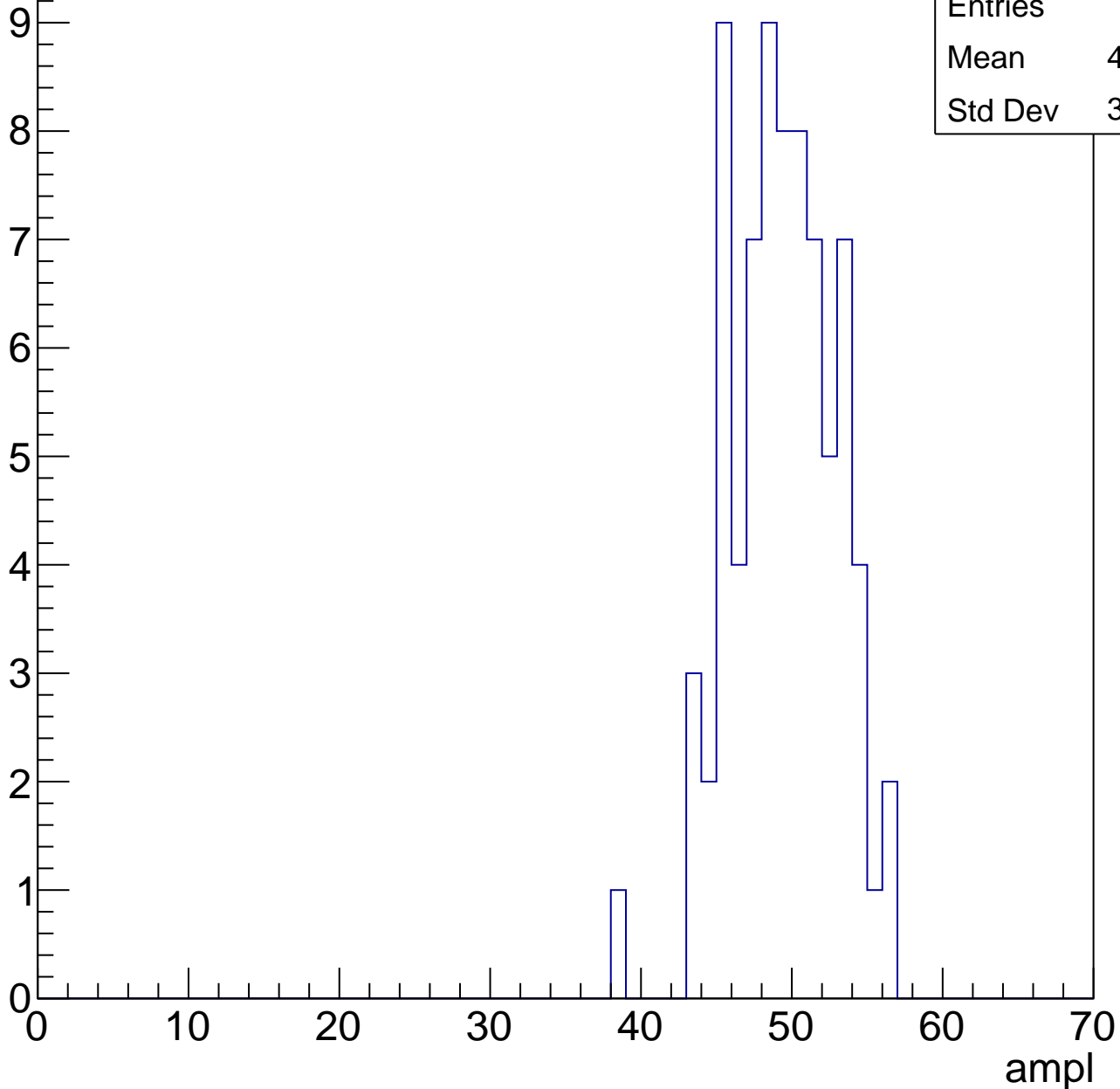


# B1L102S, U21-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	48.94
Std Dev	3.462

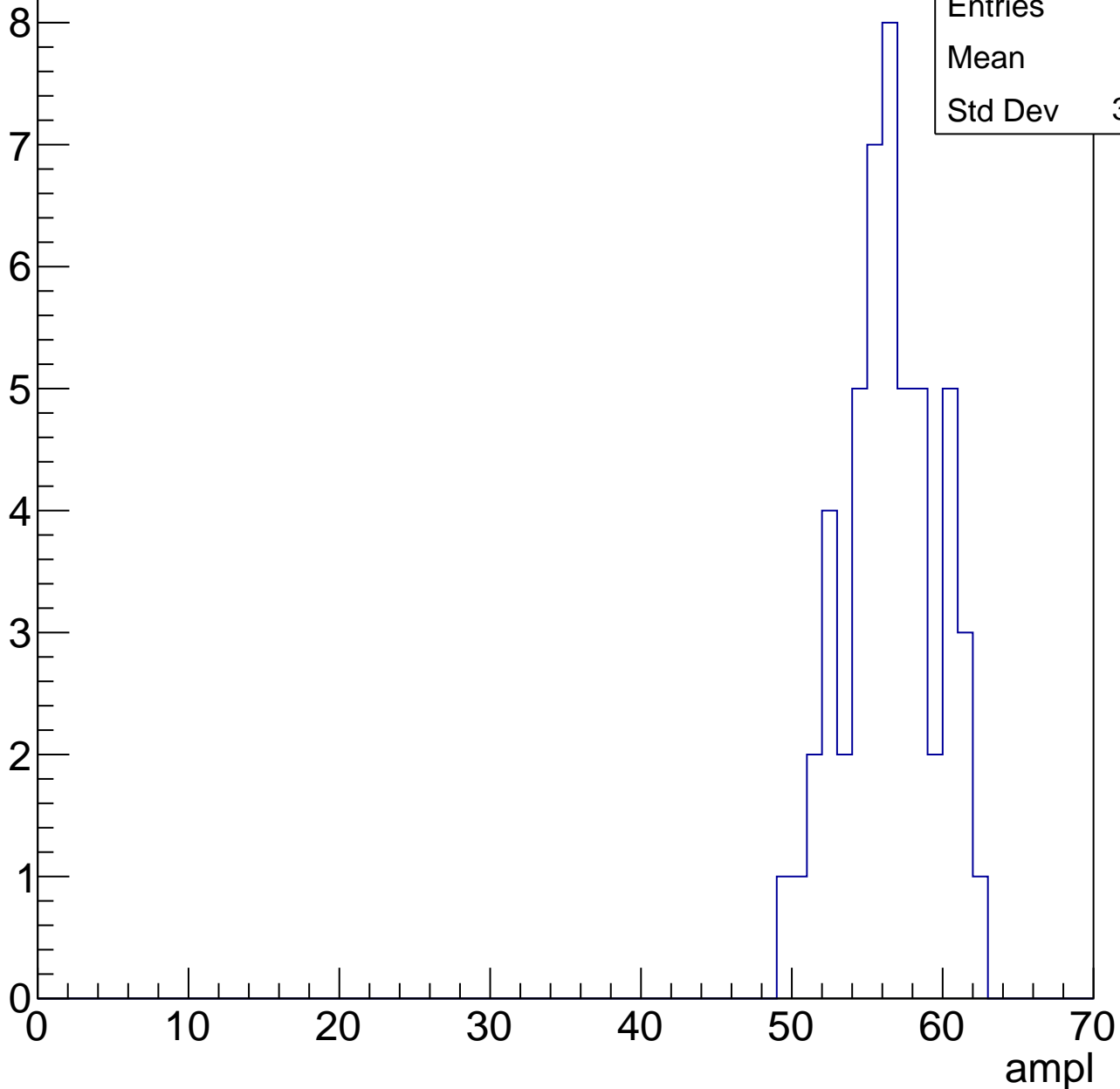


# B1L102S, U21-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	56
Std Dev	3.061



# B1L102S, U21-ch65, adc5

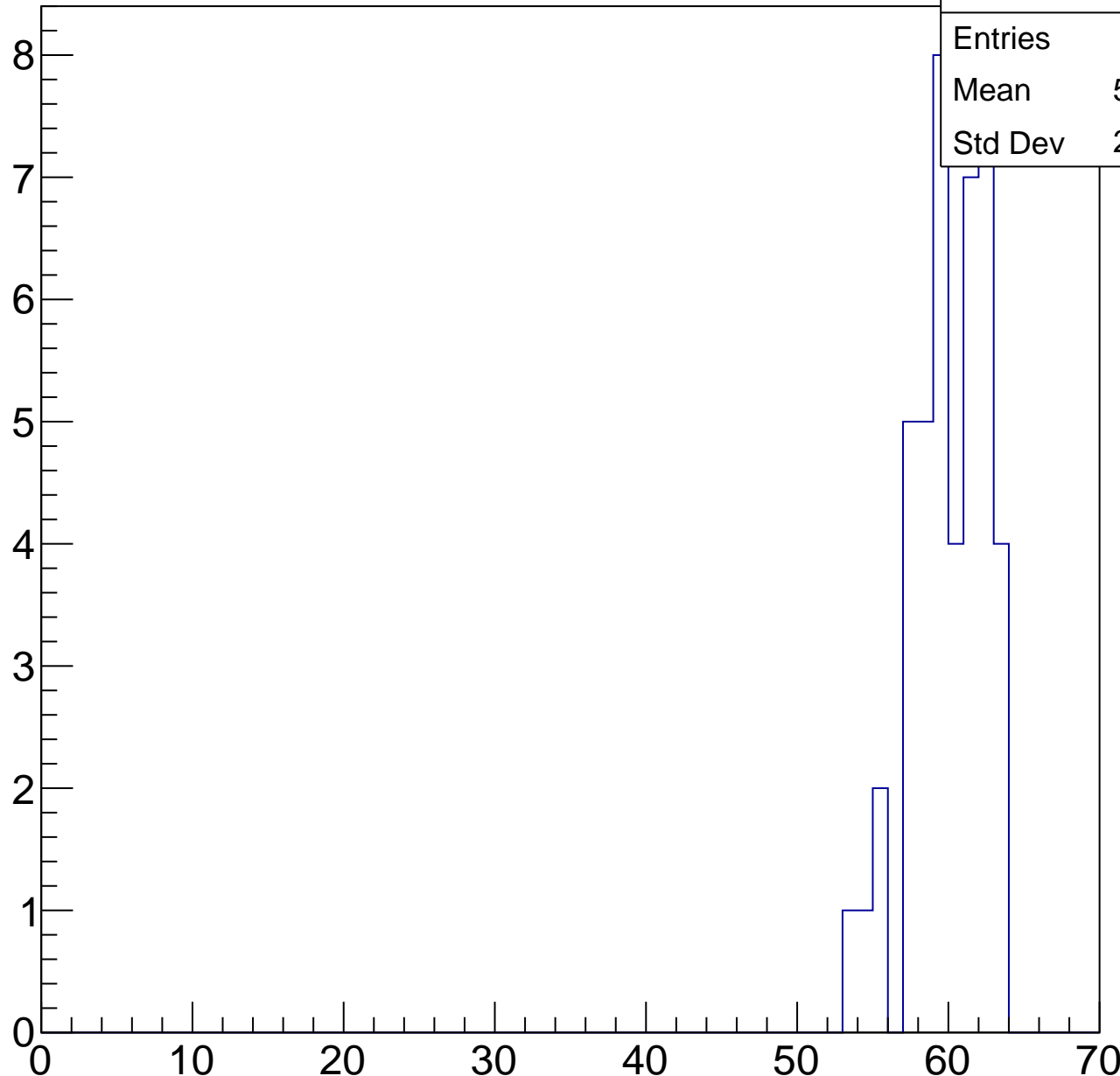
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	45
Mean	59.53
Std Dev	2.464

ampl

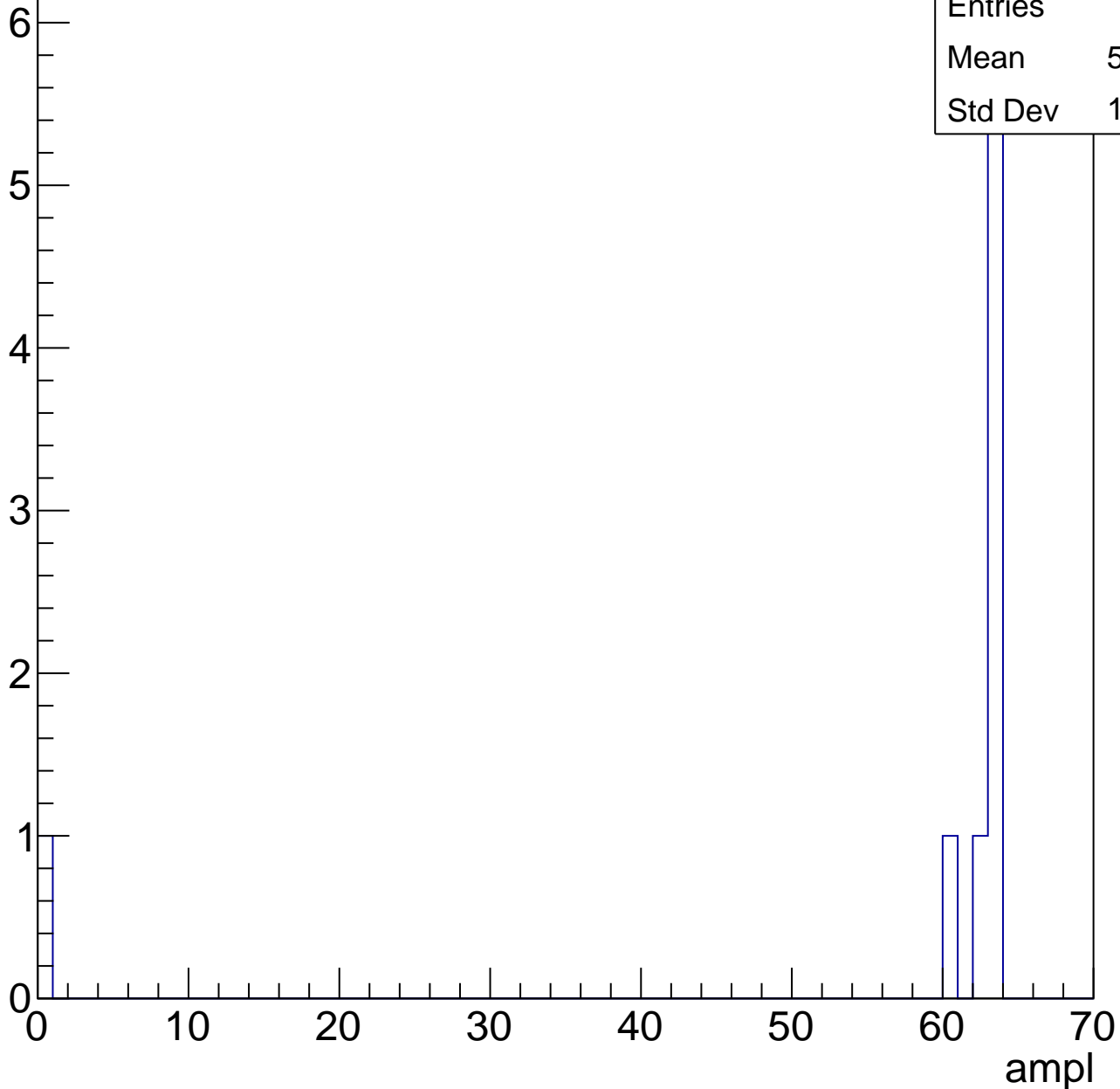


# B1L102S, U21-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	9
Mean	55.56
Std Dev	19.66





# B1L102S, U21-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U21-ch66, adc0

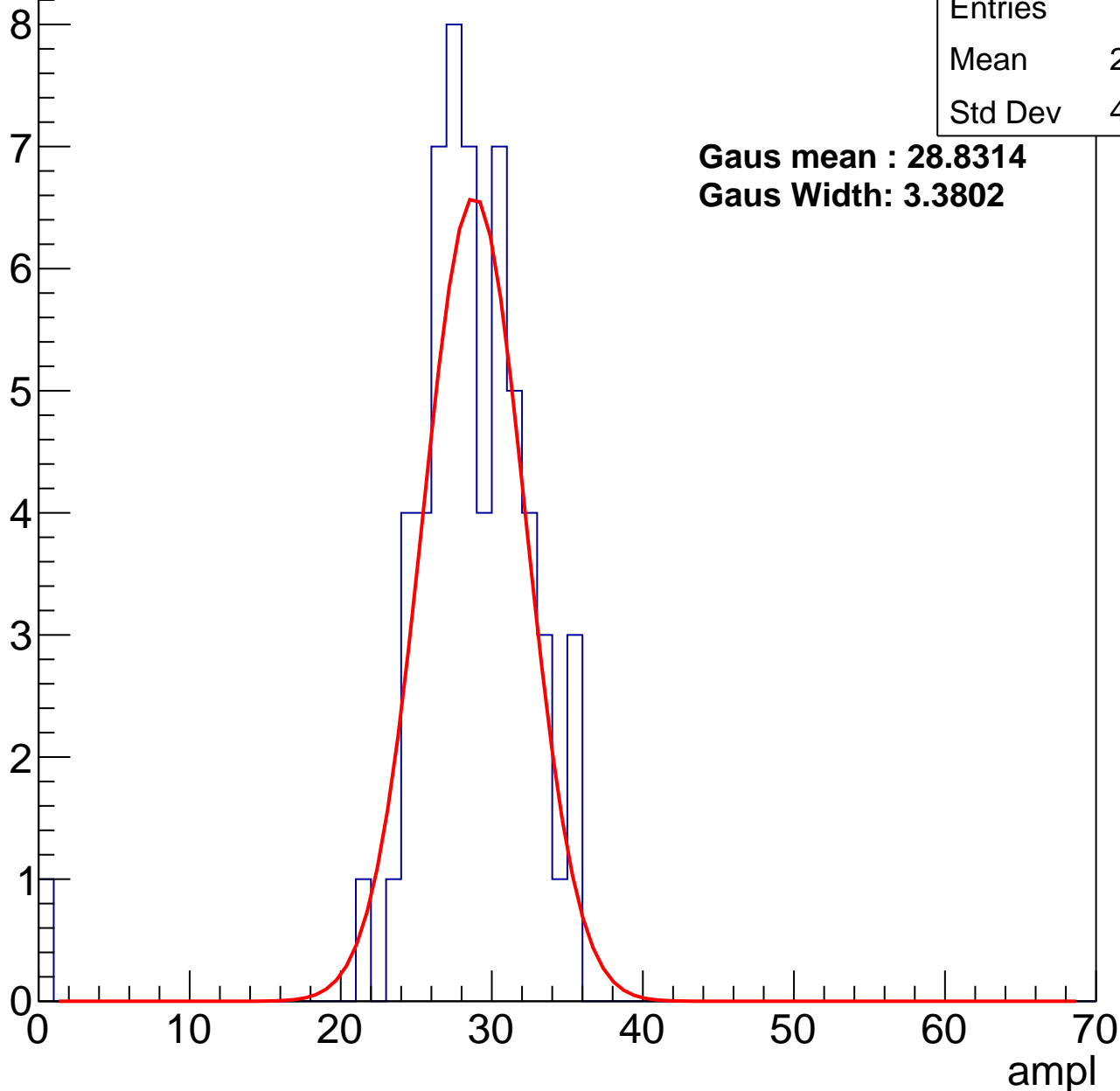
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	28.02
Std Dev	4.818

**Gaus mean : 28.8314**

**Gaus Width: 3.3802**



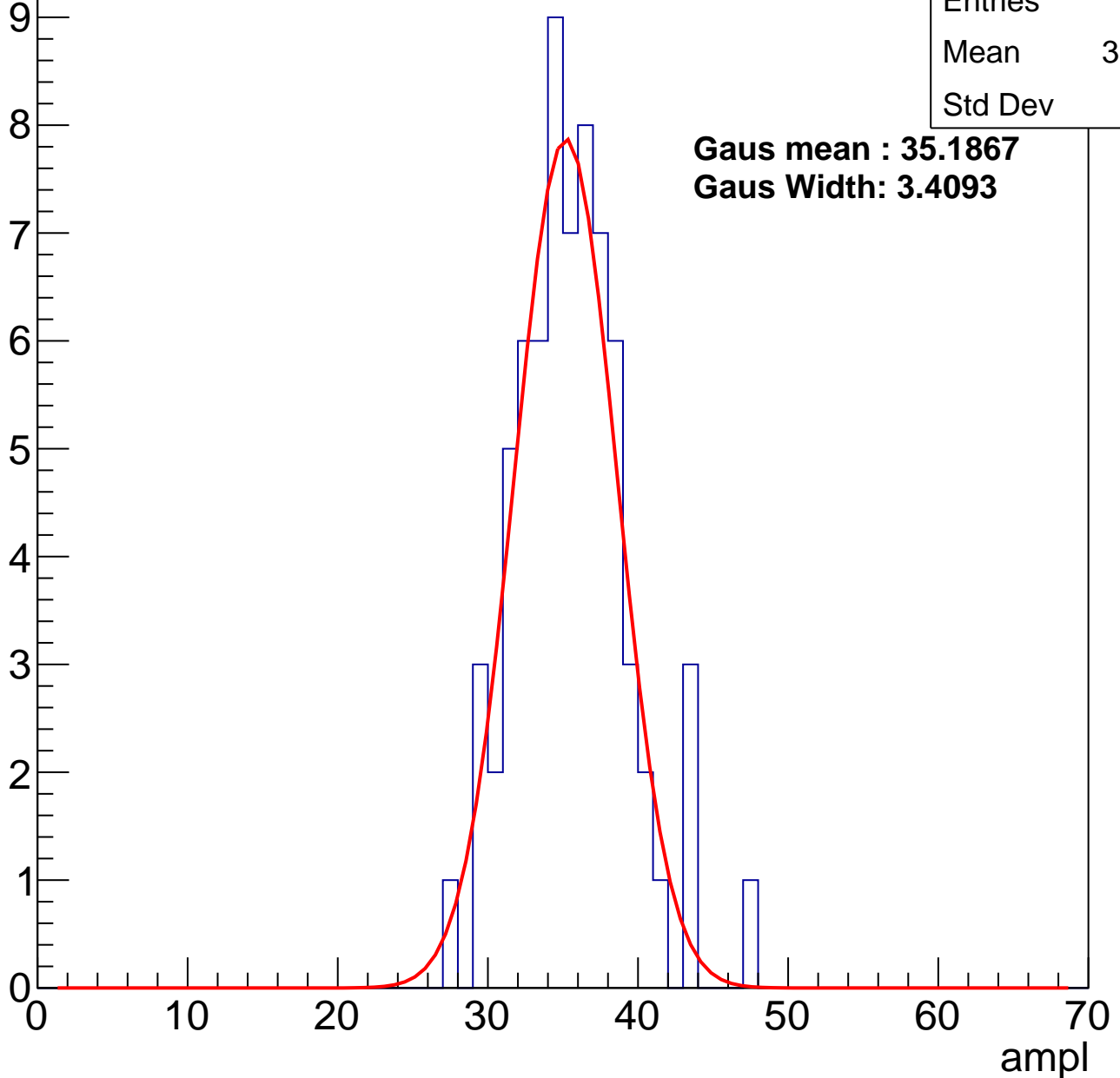
# B1L102S, U21-ch66, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	35.13
Std Dev	3.68

**Gaus mean : 35.1867**  
**Gaus Width: 3.4093**



# B1L102S, U21-ch66, adc2

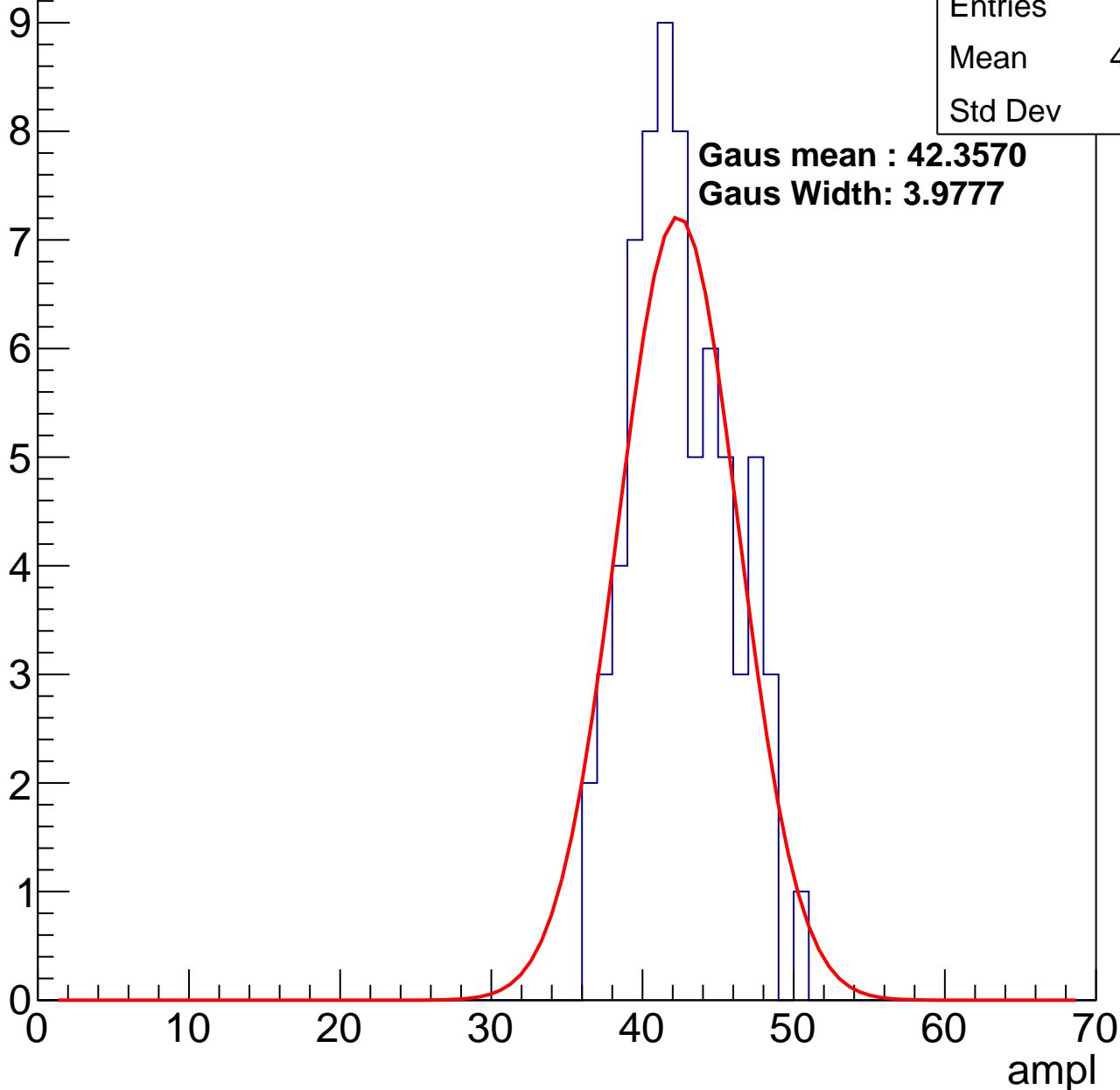
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	42.09
Std Dev	3.26

**Gaus mean : 42.3570**

**Gaus Width: 3.9777**

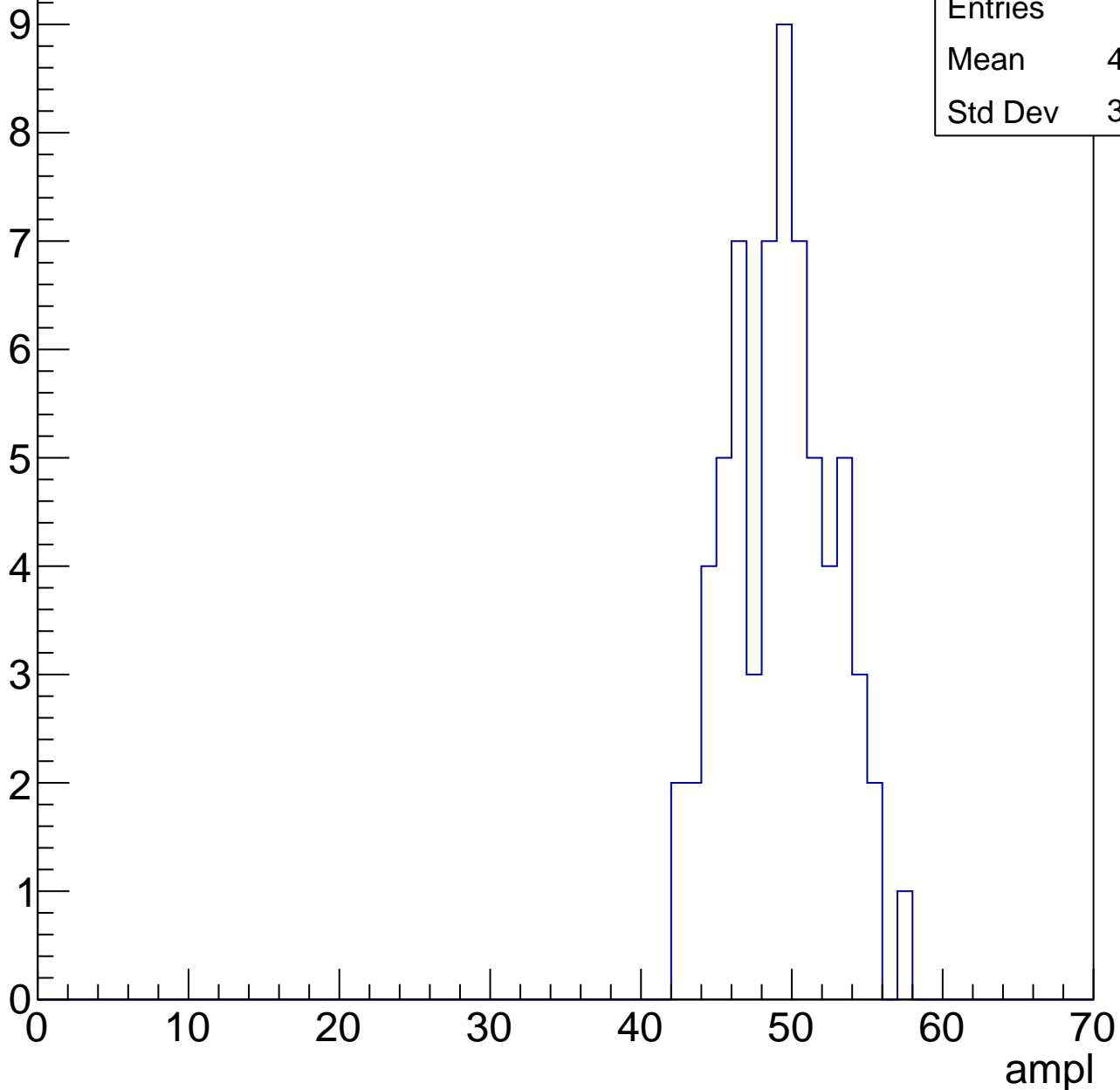


# B1L102S, U21-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	48.76
Std Dev	3.442

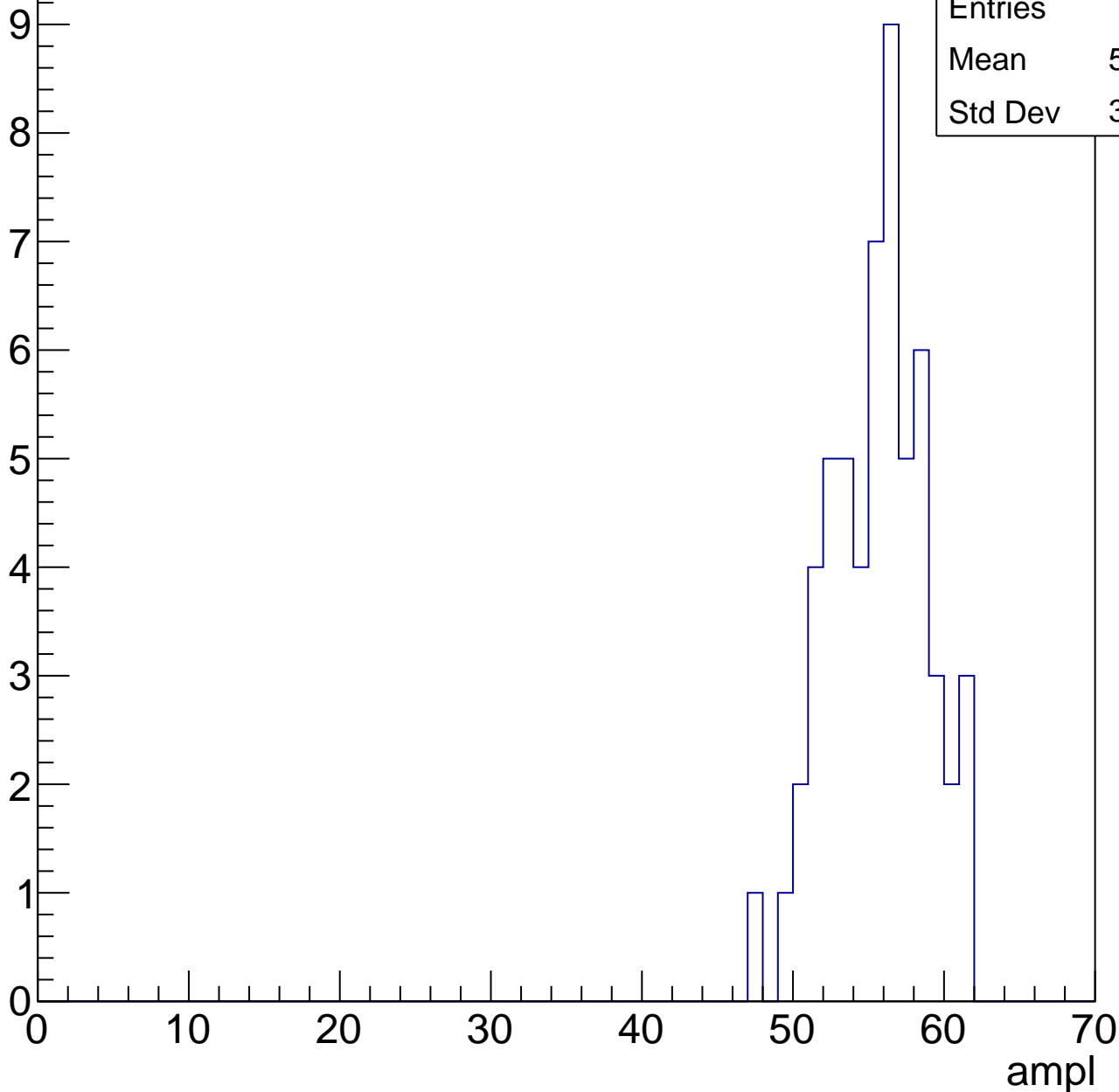


# B1L102S, U21-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	55.14
Std Dev	3.165

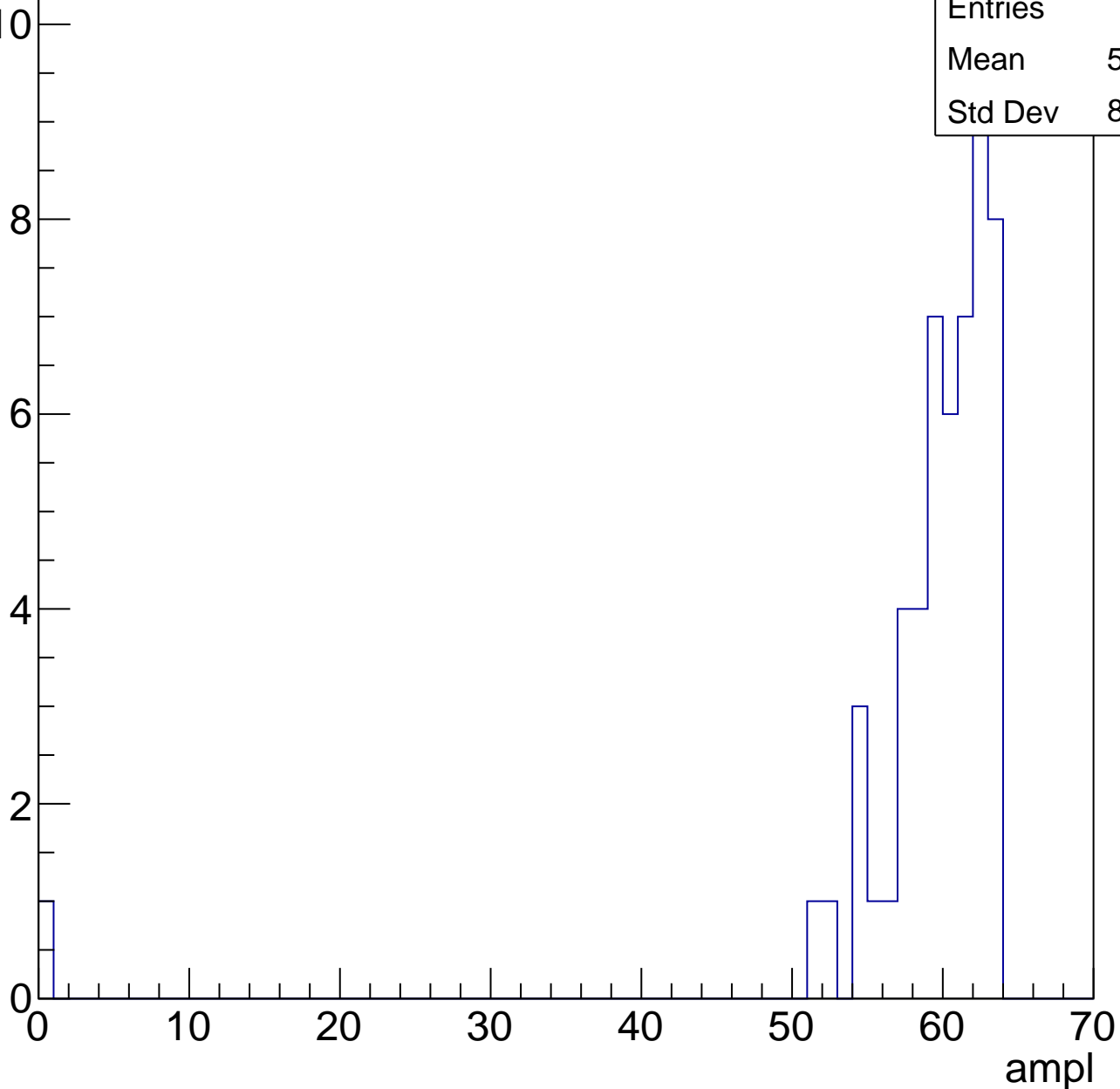


# B1L102S, U21-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	58.52
Std Dev	8.556



# B1L102S, U21-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	61.5
Std Dev	1.5

0 10 20 30 40 50 60 70

ampl



# B1L102S, U21-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U21-ch67, adc0

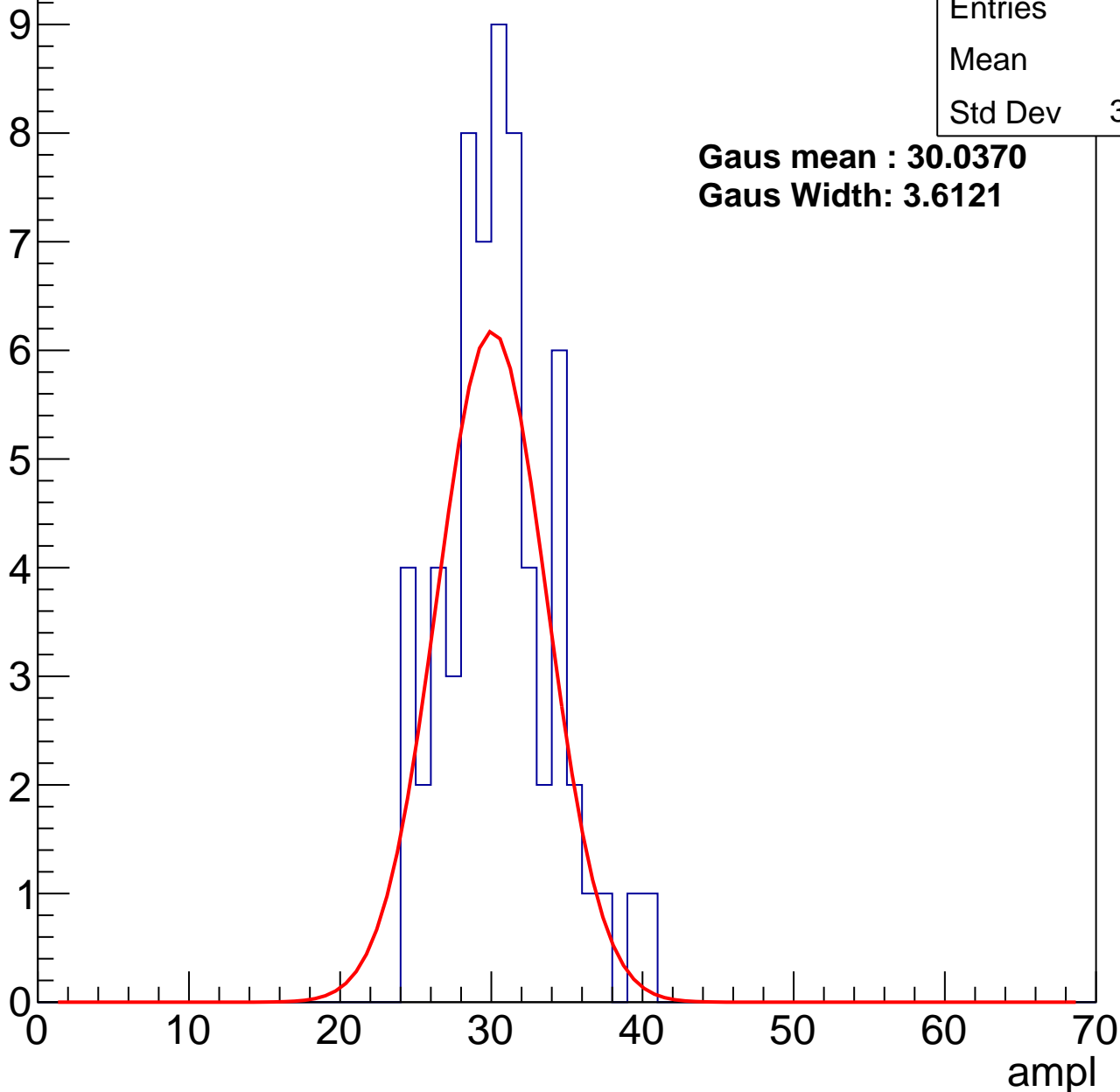
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	30.1
Std Dev	3.513

**Gaus mean : 30.0370**

**Gaus Width: 3.6121**



# B1L102S, U21-ch67, adc1

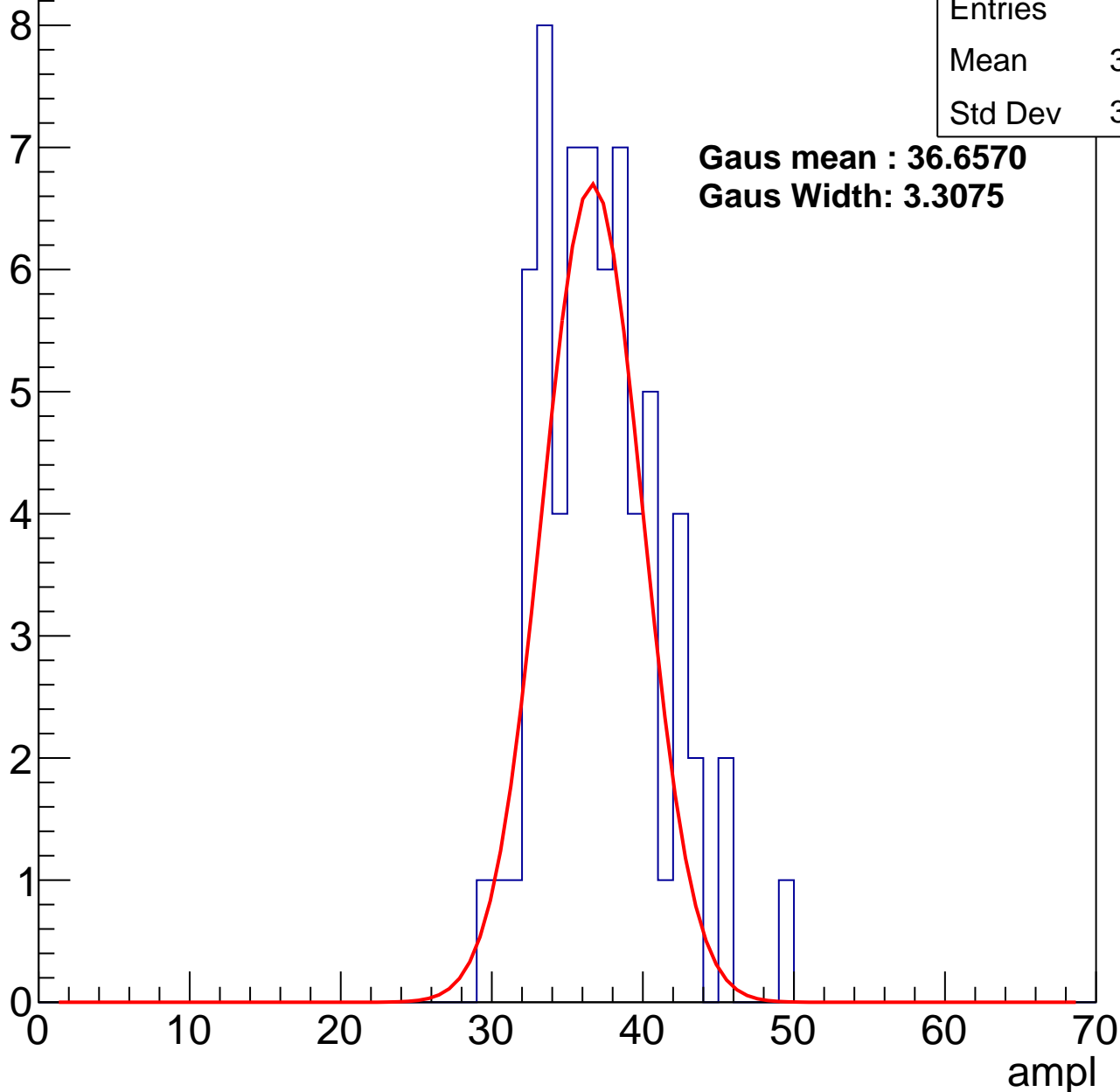
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	36.67
Std Dev	3.899

**Gaus mean : 36.6570**

**Gaus Width: 3.3075**



# B1L102S, U21-ch67, adc2

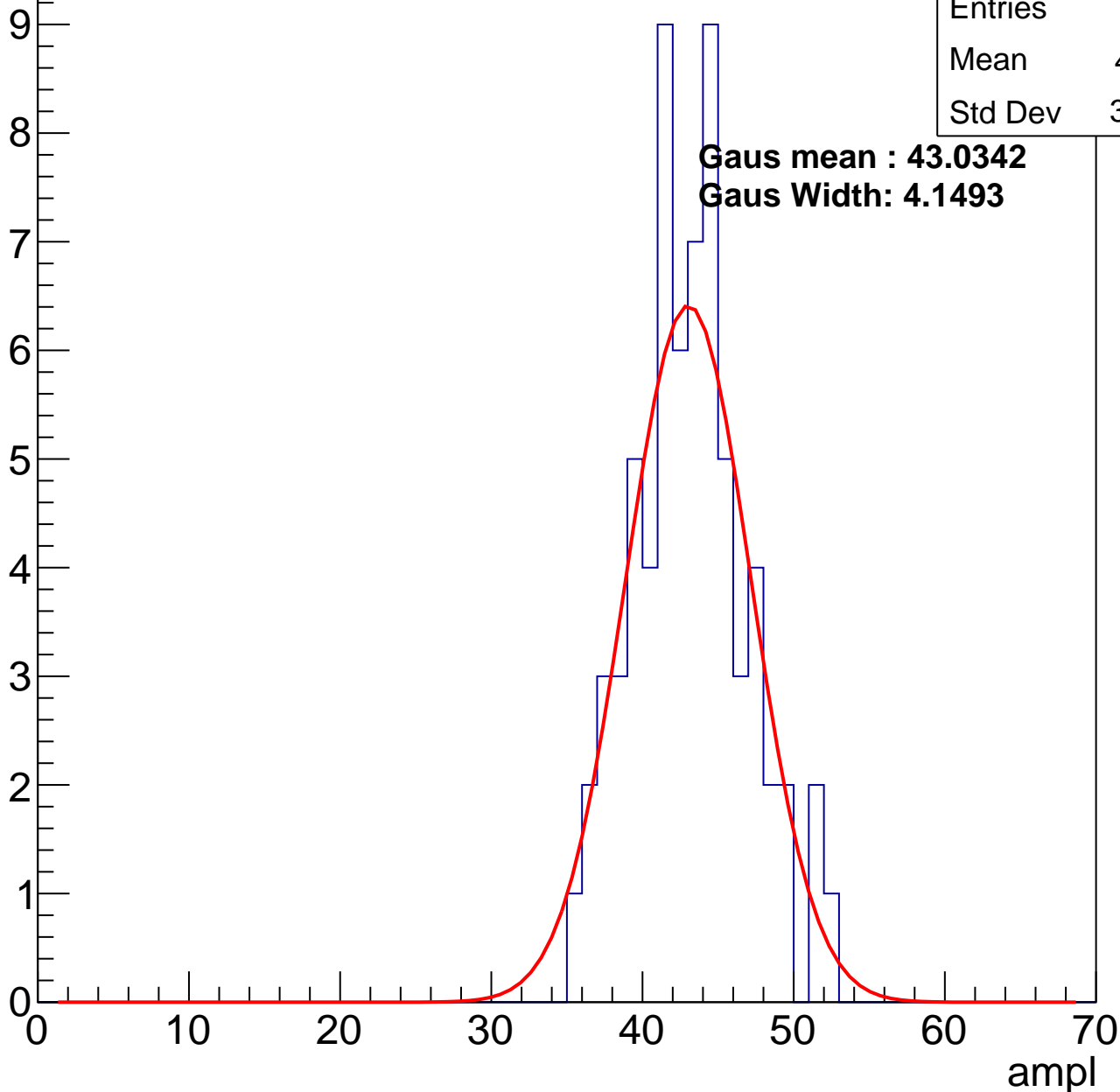
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	42.71
Std Dev	3.734

**Gaus mean : 43.0342**

**Gaus Width: 4.1493**

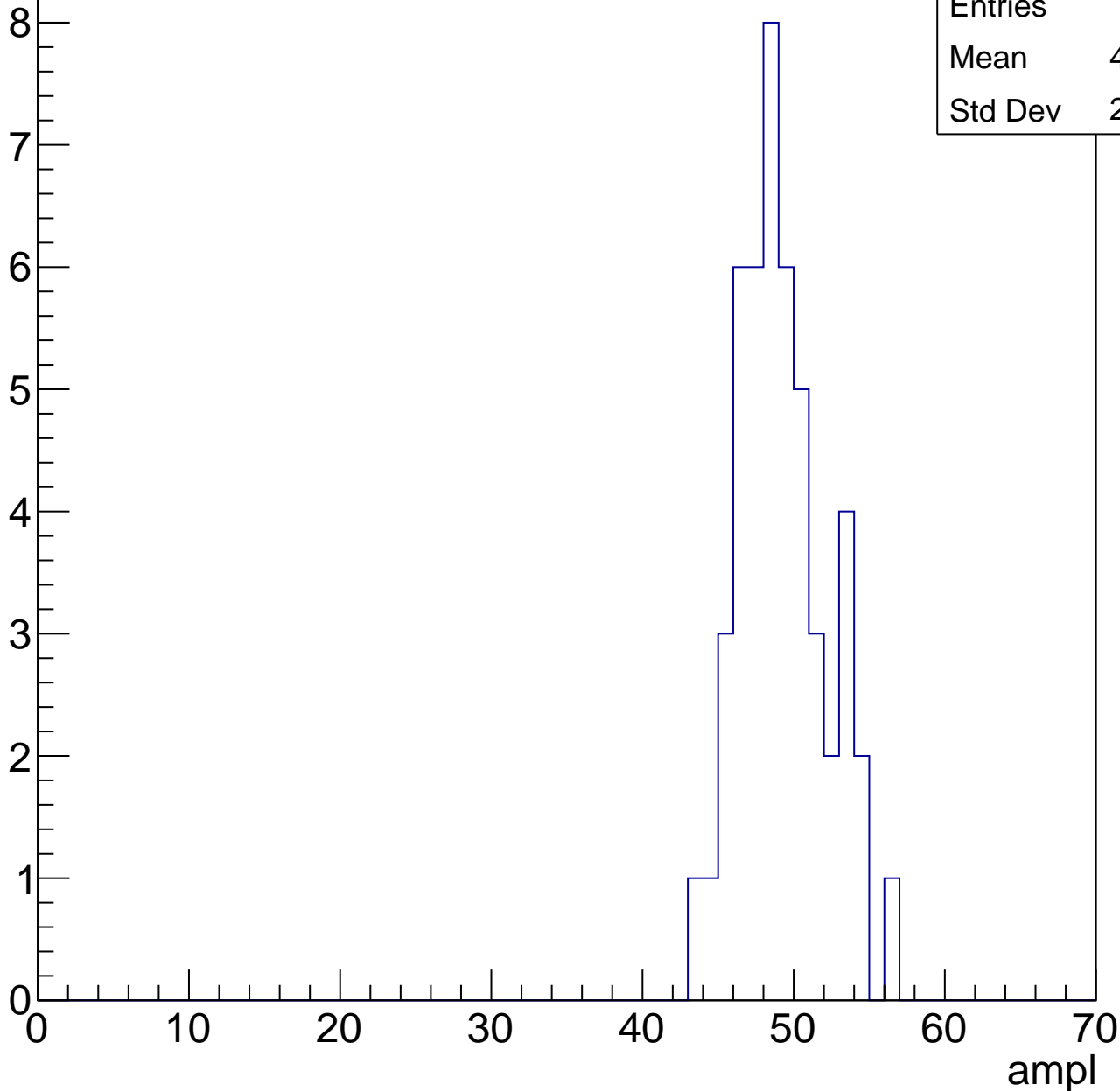


# B1L102S, U21-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	48.77
Std Dev	2.852

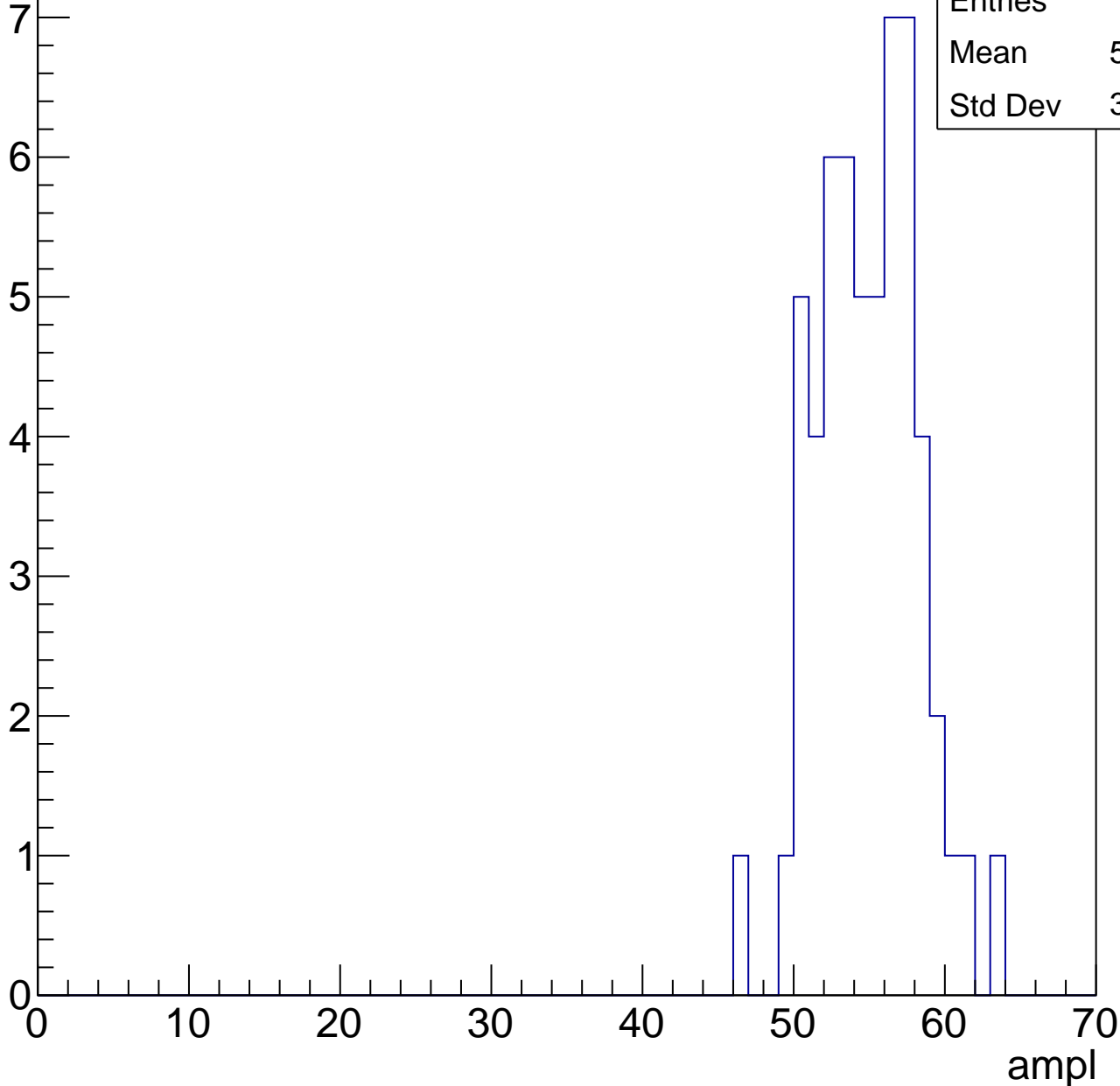


# B1L102S, U21-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	54.45
Std Dev	3.273

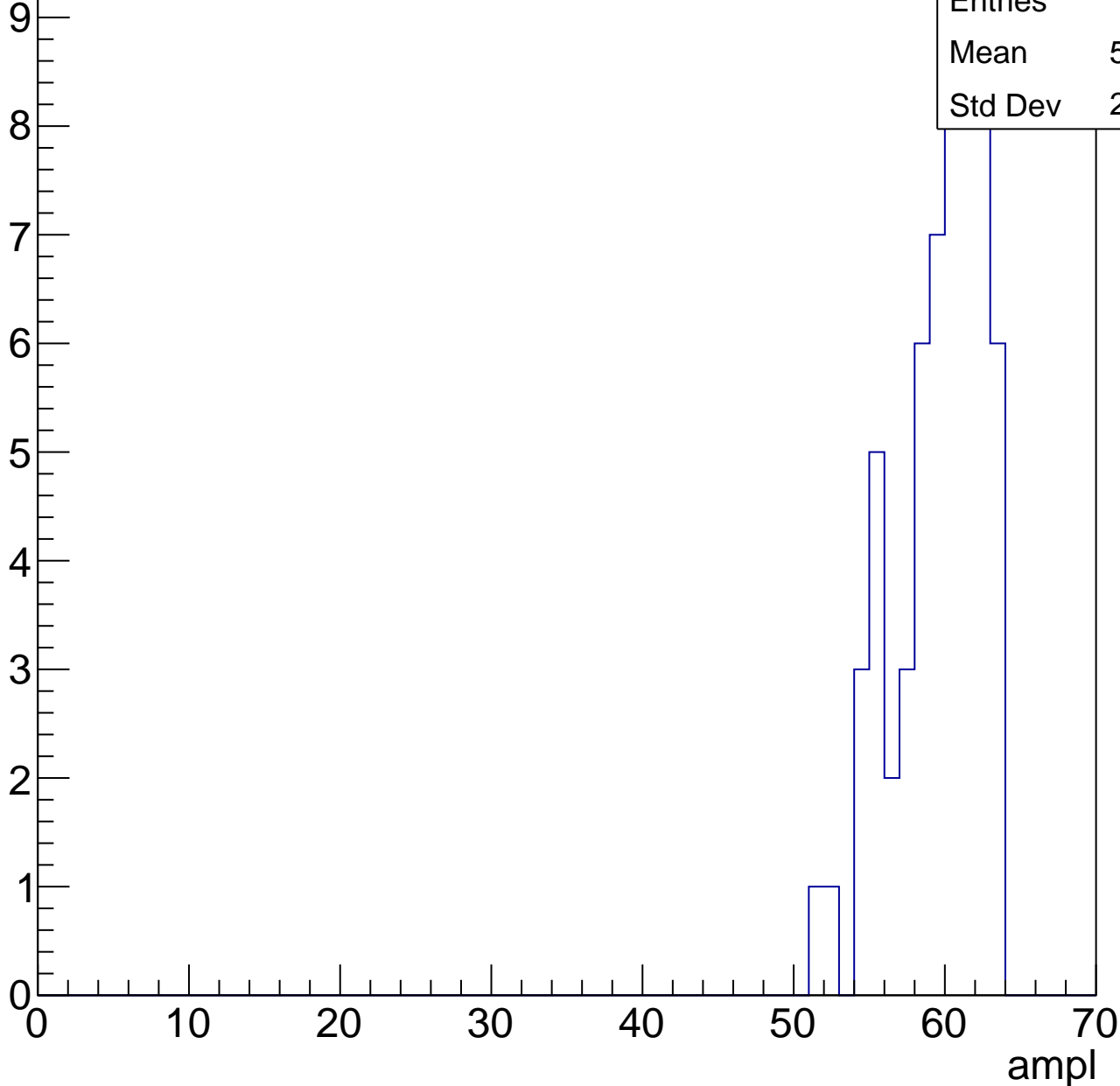


# B1L102S, U21-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

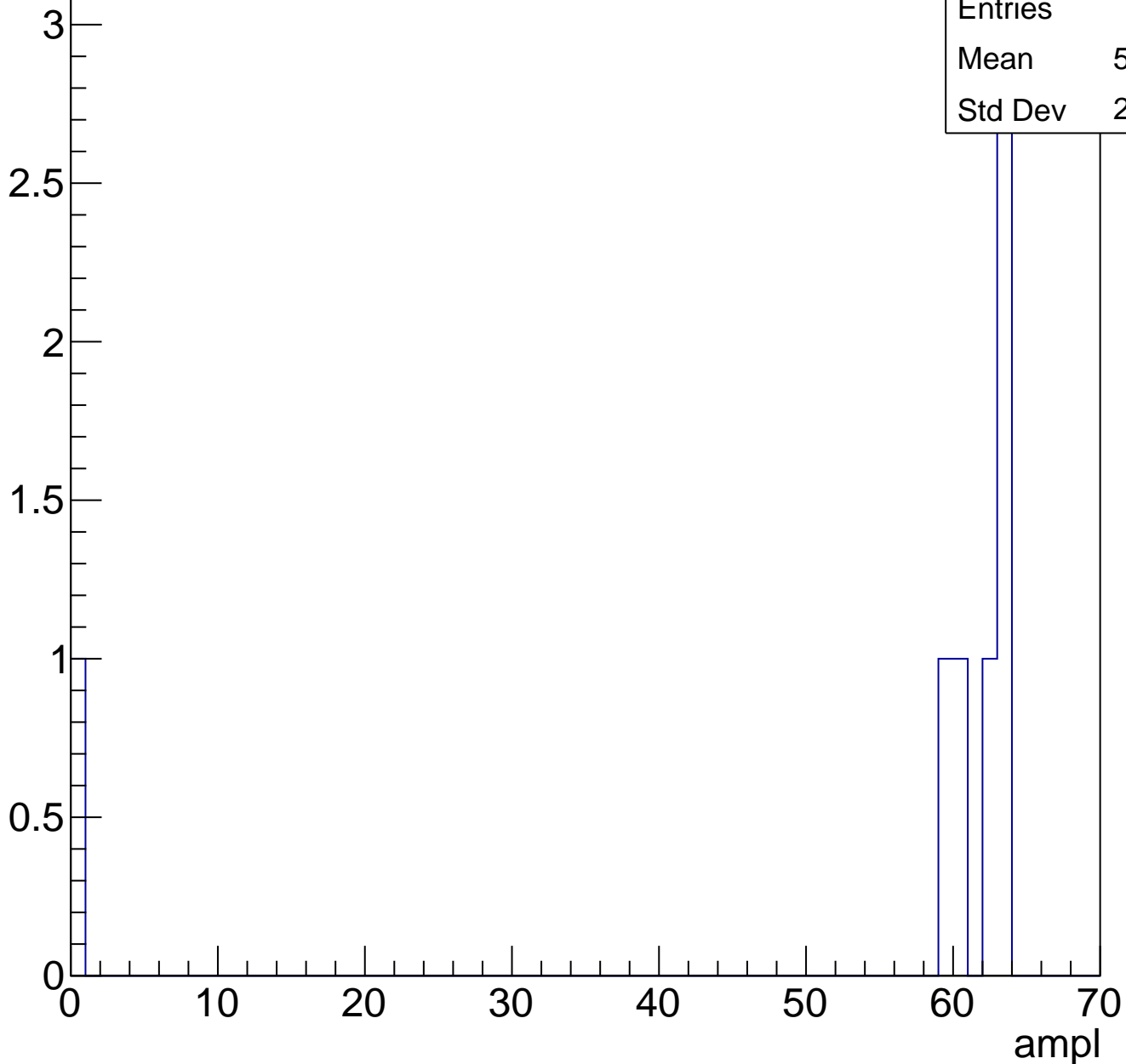
Entries	60
Mean	59.15
Std Dev	2.954



# B1L102S, U21-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch68, adc0

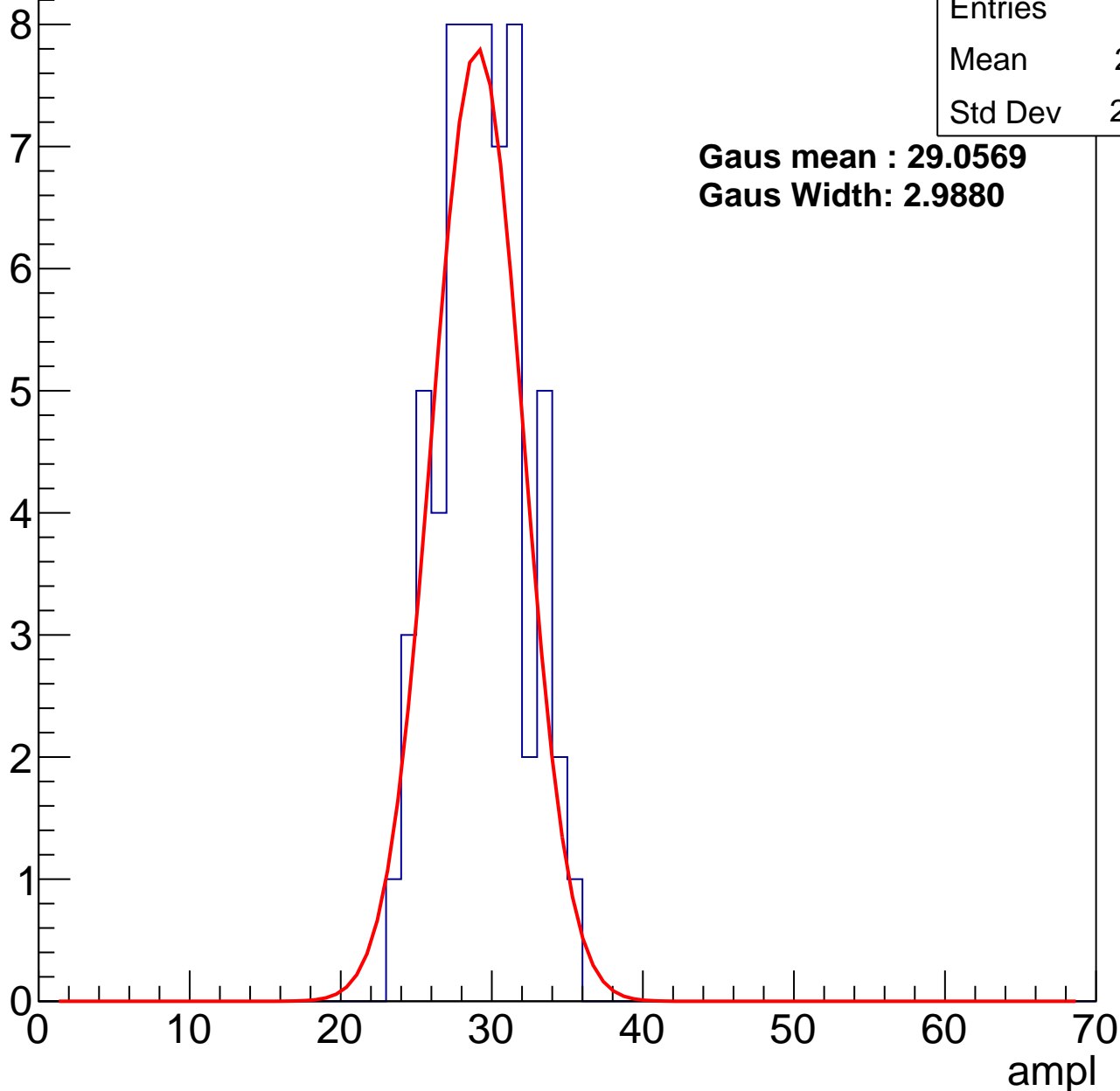
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	28.81
Std Dev	2.805

**Gaus mean : 29.0569**

**Gaus Width: 2.9880**



# B1L102S, U21-ch68, adc1

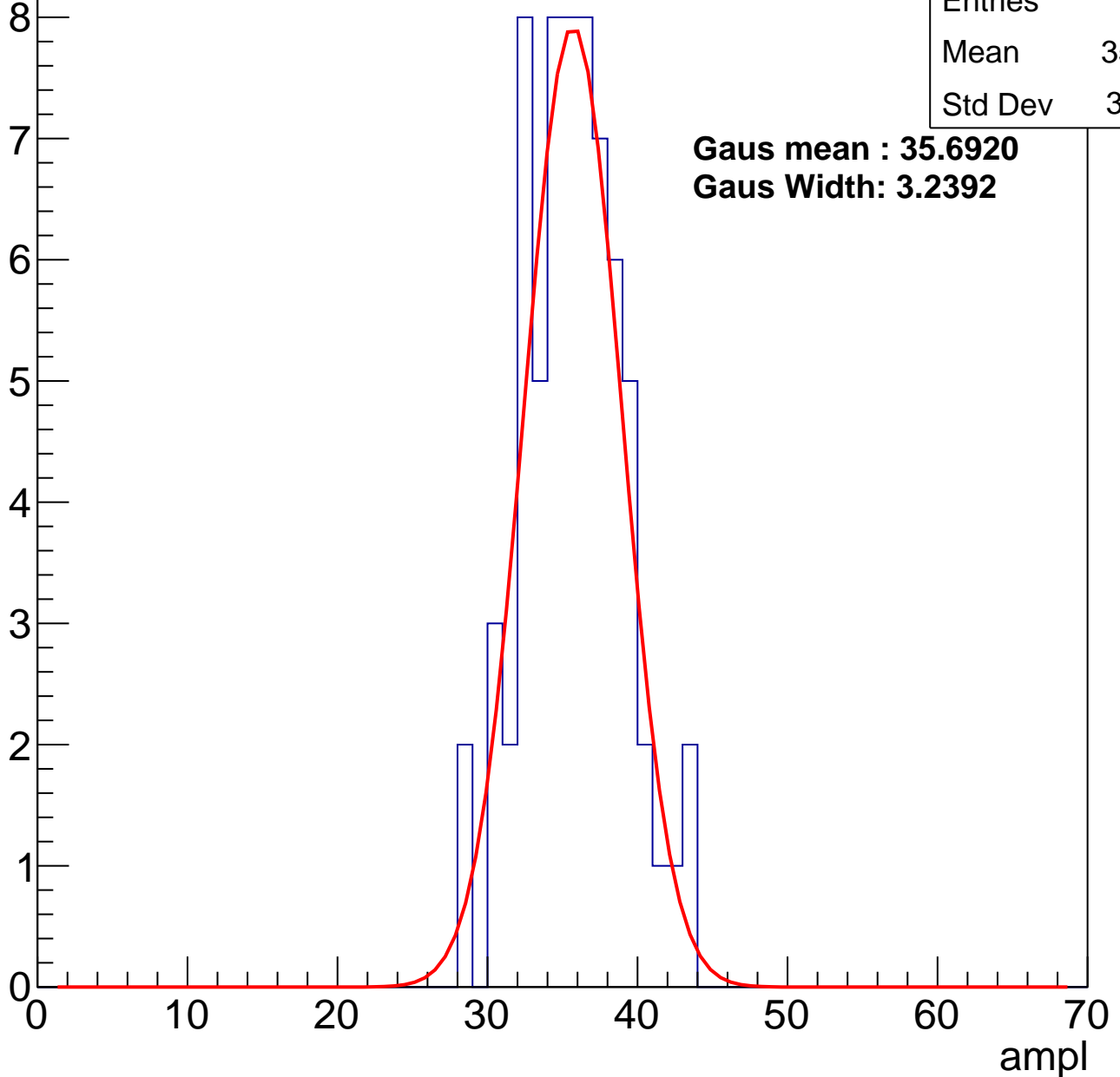
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	35.29
Std Dev	3.281

**Gaus mean : 35.6920**

**Gaus Width: 3.2392**



# B1L102S, U21-ch68, adc2

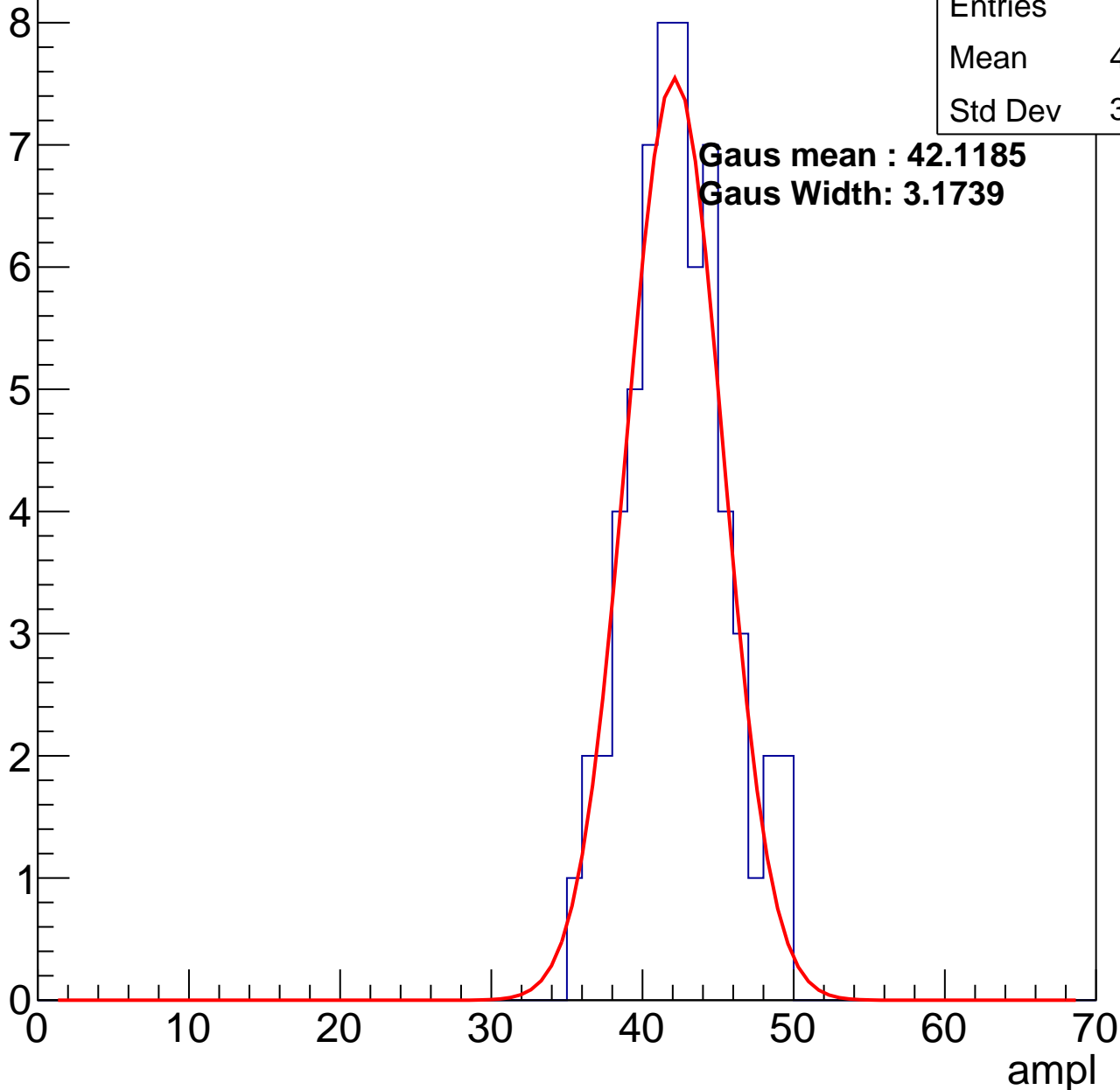
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	41.89
Std Dev	3.183

**Gaus mean : 42.1185**

**Gaus Width: 3.1739**

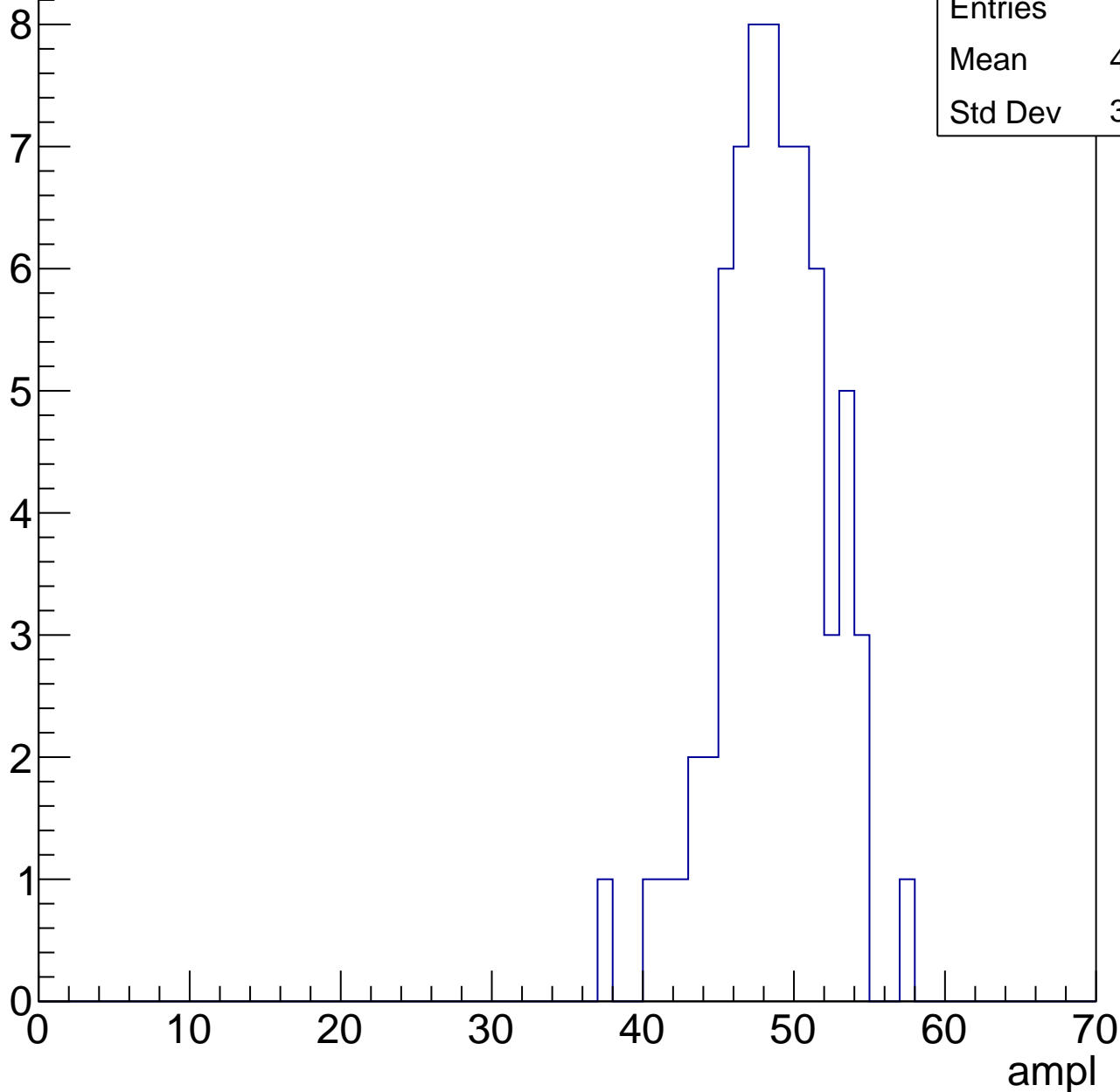


# B1L102S, U21-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	48.19
Std Dev	3.593

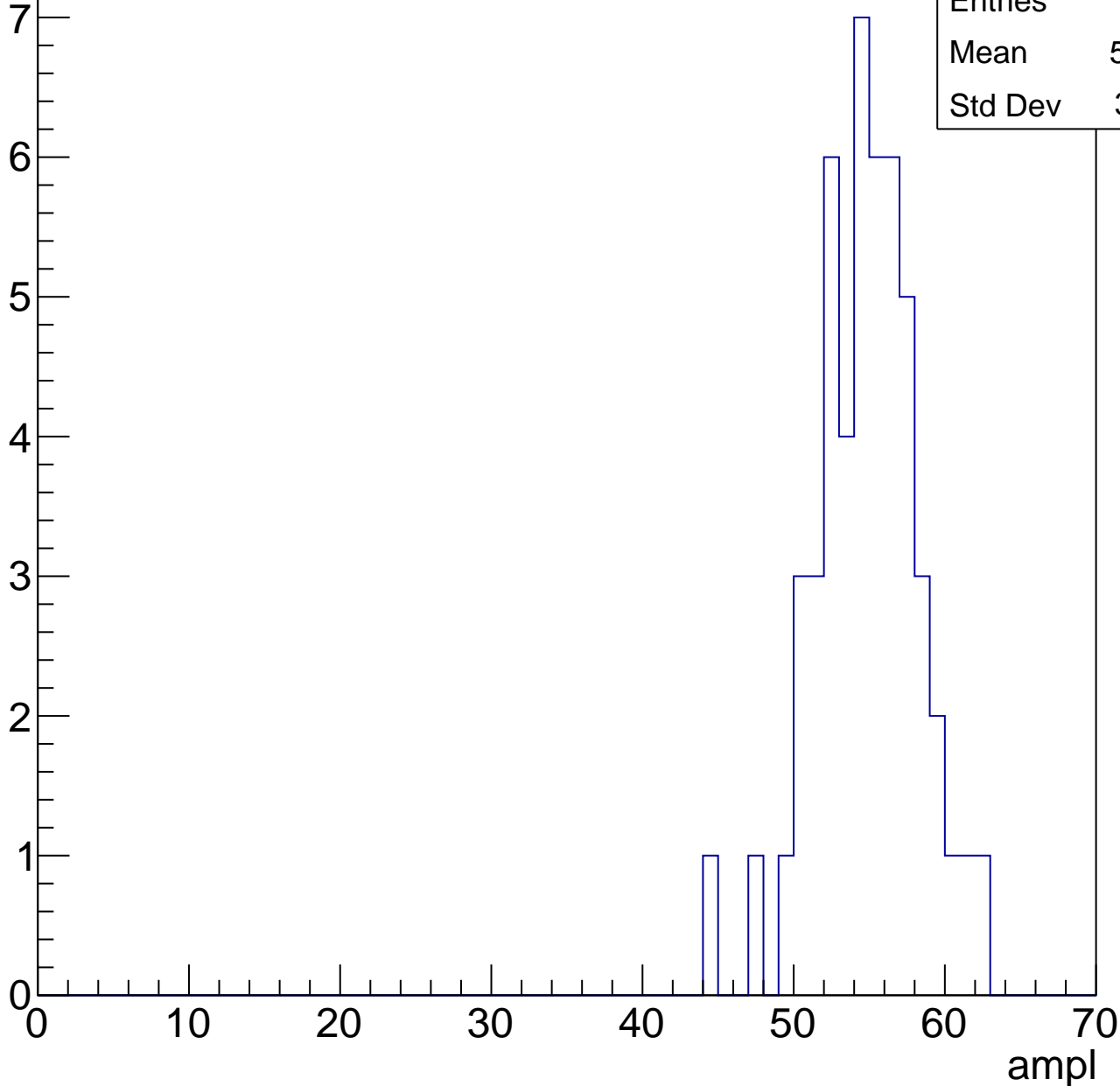


# B1L102S, U21-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	54.33
Std Dev	3.411

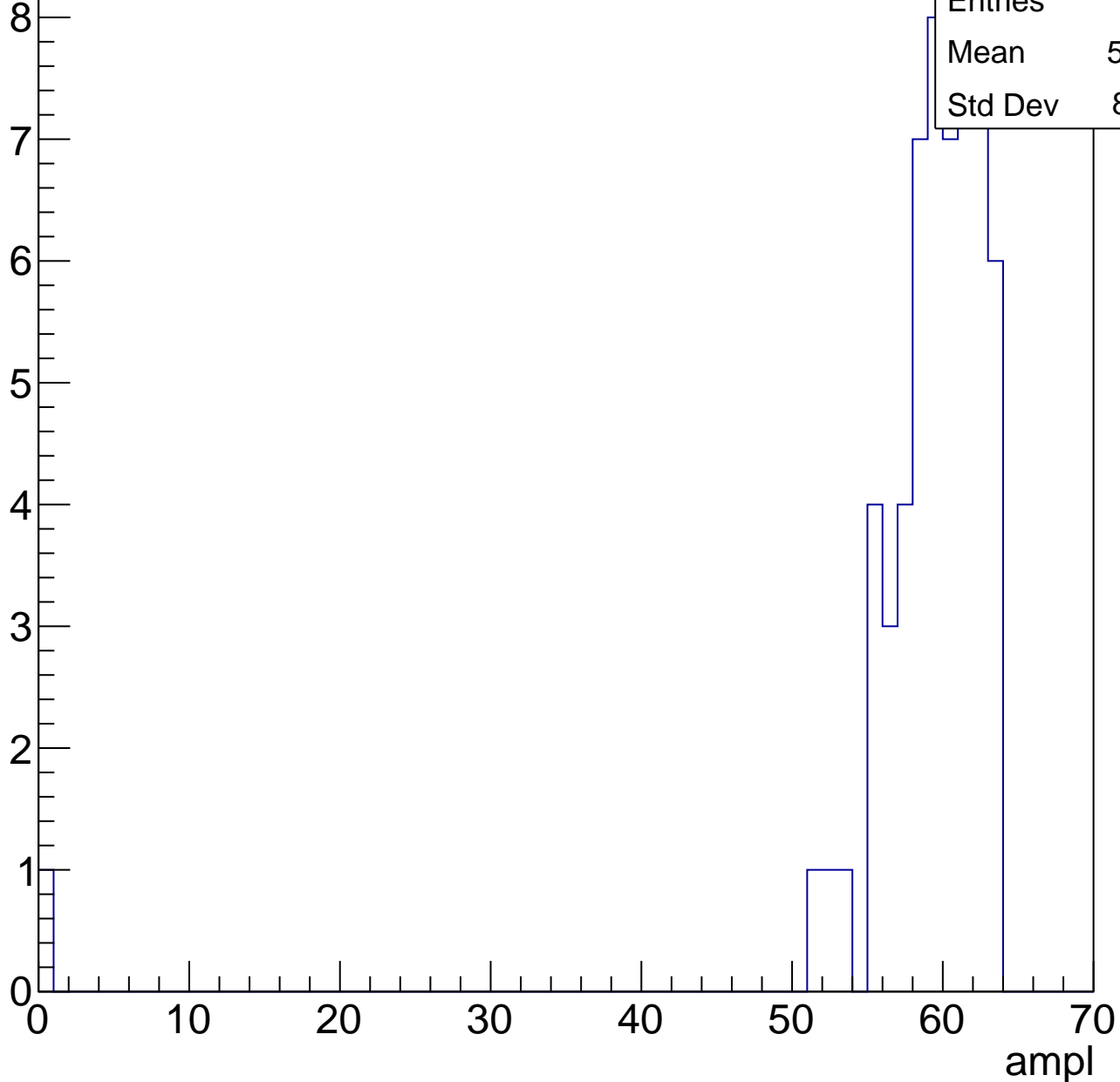


# B1L102S, U21-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	58.17
Std Dev	8.141



# B1L102S, U21-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

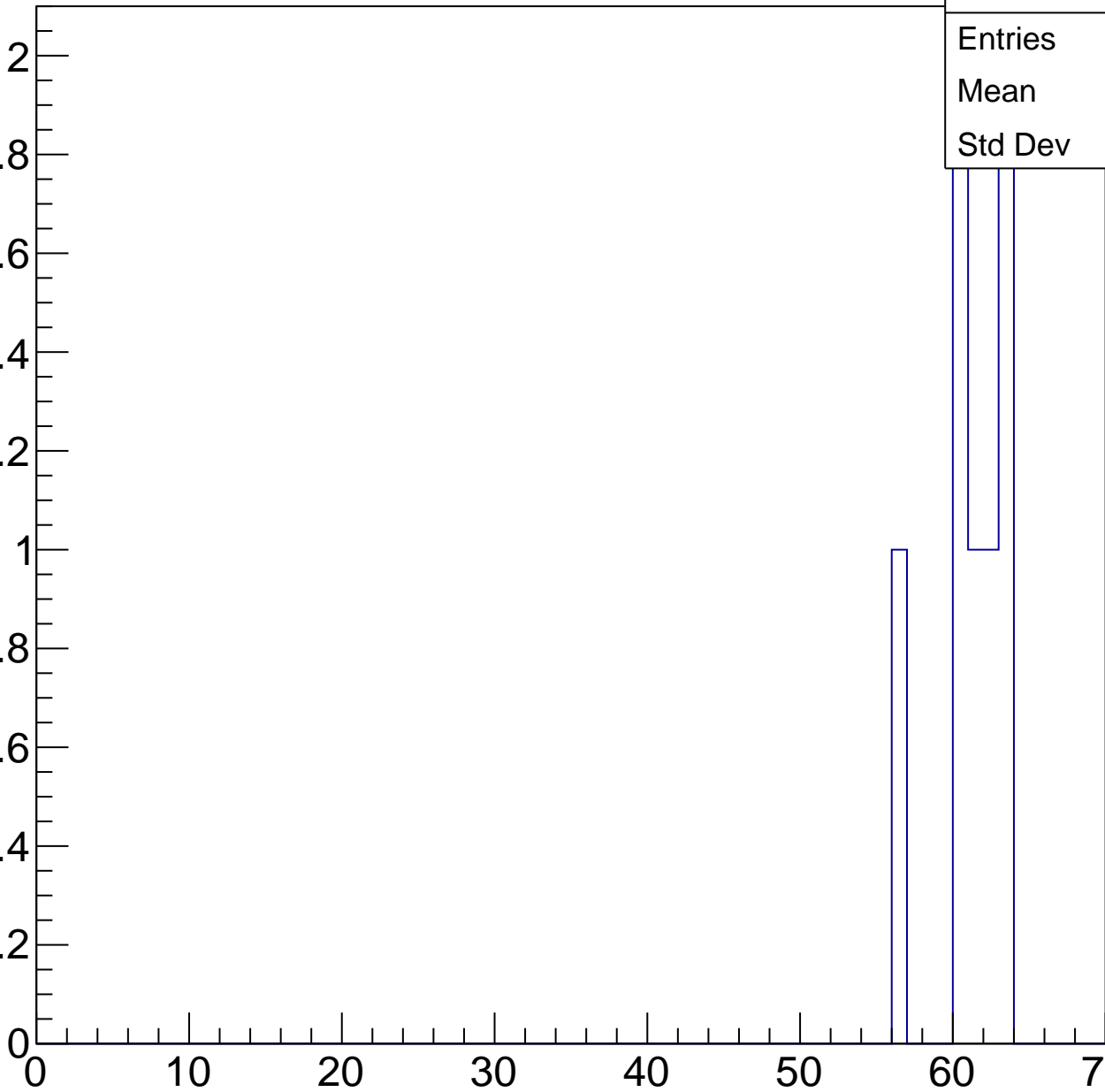
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	60.71
Std Dev	2.25

0 10 20 30 40 50 60 70

ampl

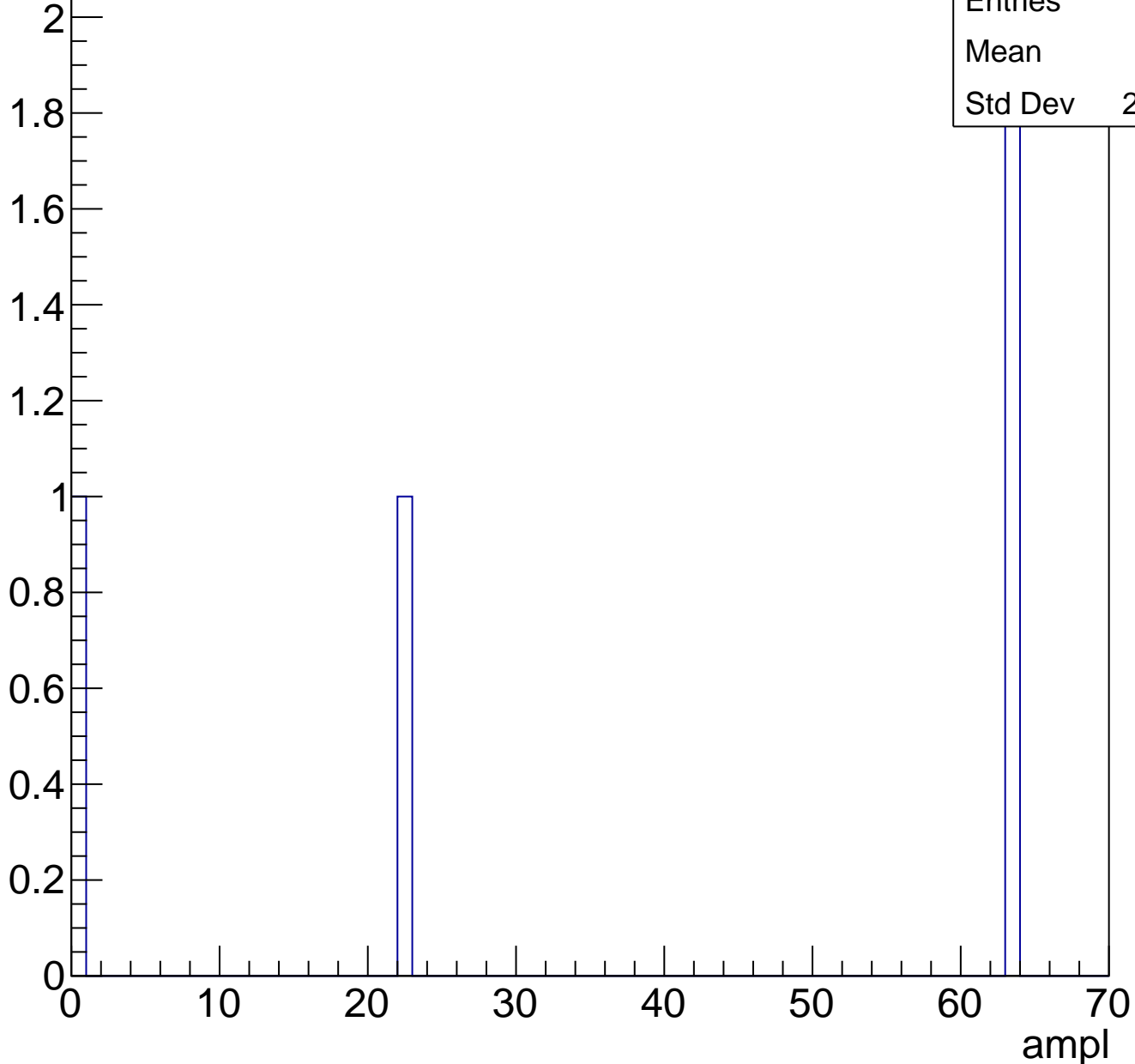




# B1L102S, U21-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	4
Mean	37
Std Dev	27.14

# B1L102S, U21-ch69, adc0

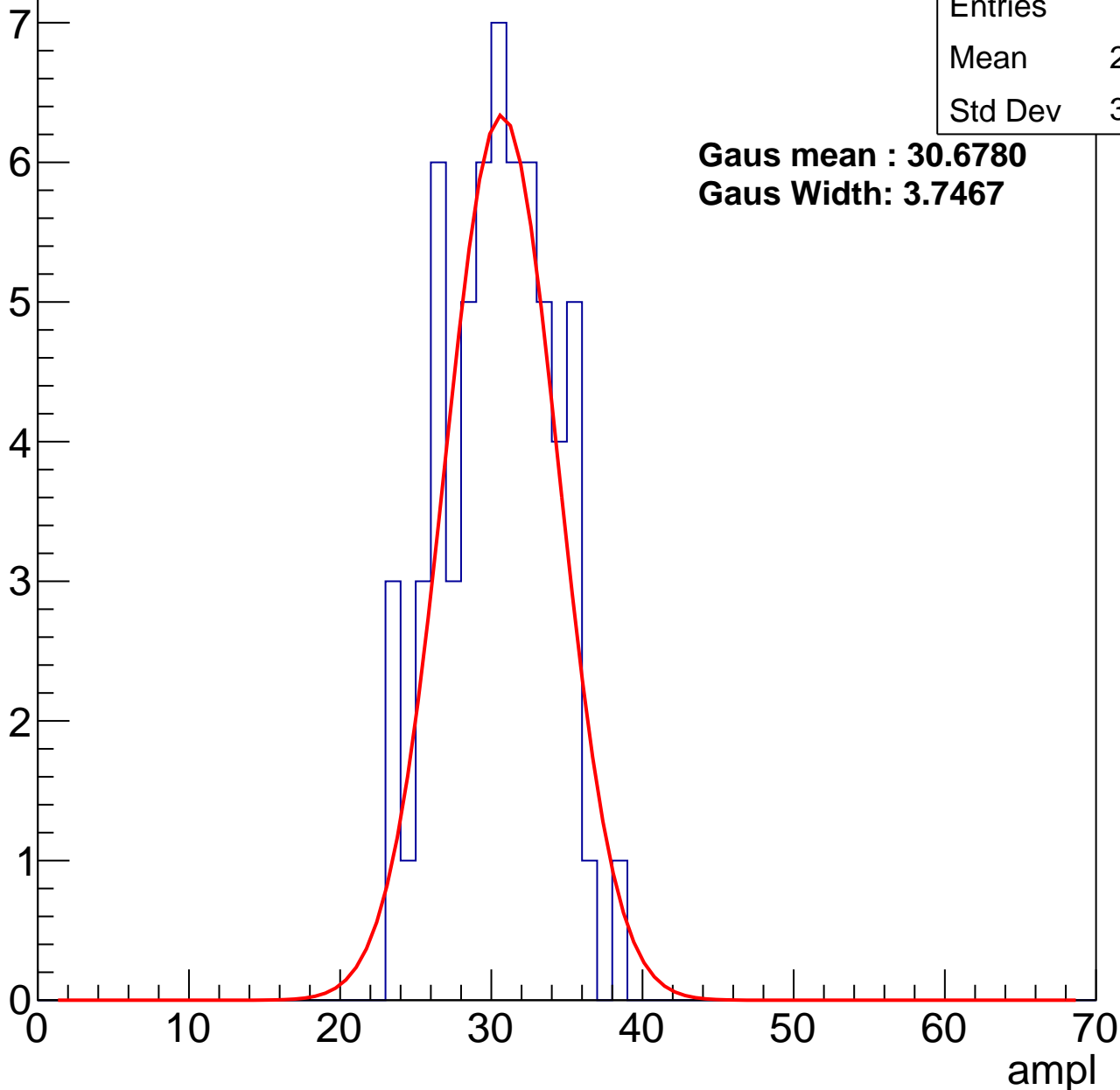
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	29.95
Std Dev	3.526

**Gaus mean : 30.6780**

**Gaus Width: 3.7467**



# B1L102S, U21-ch69, adc1

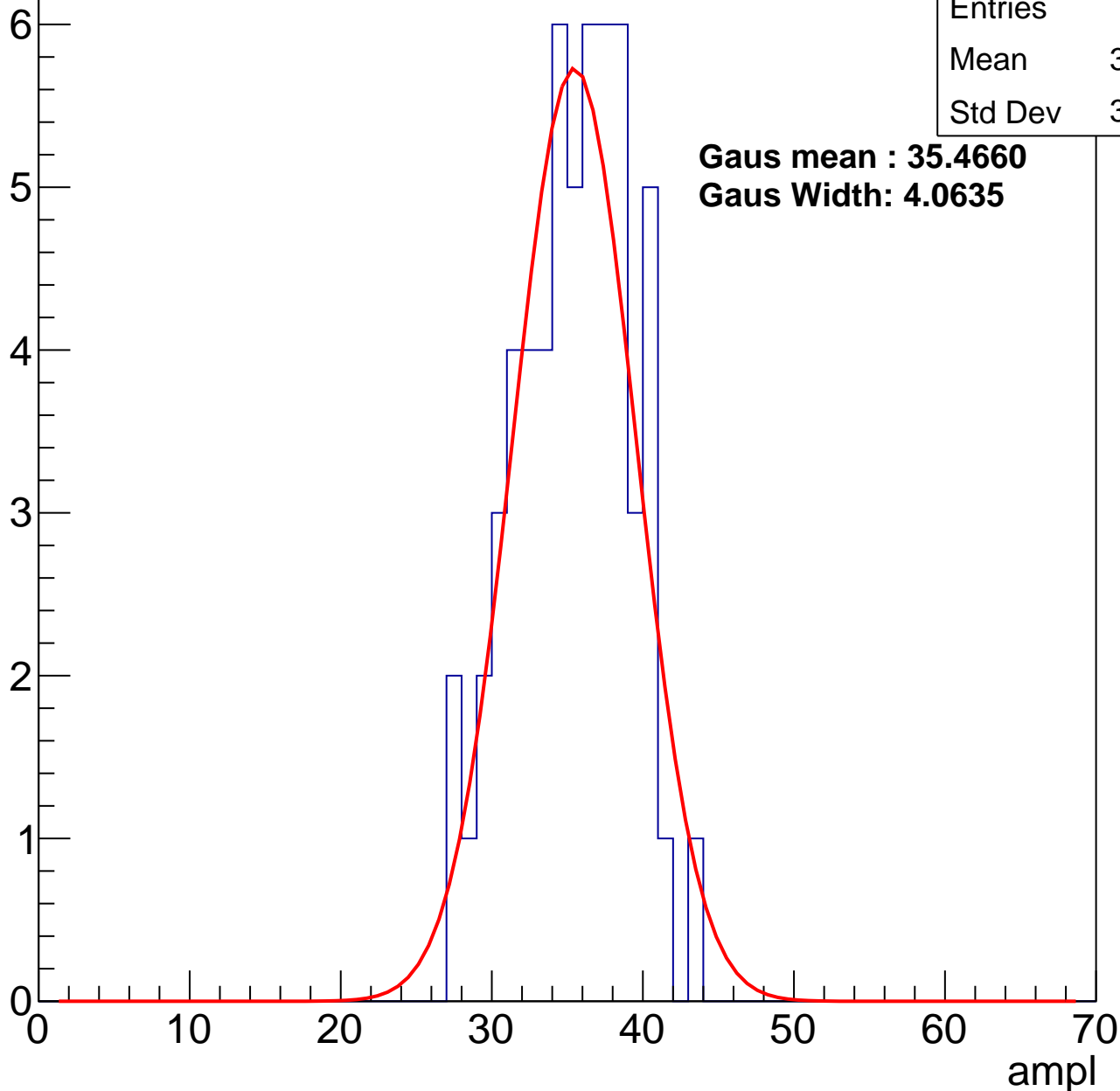
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	34.92
Std Dev	3.688

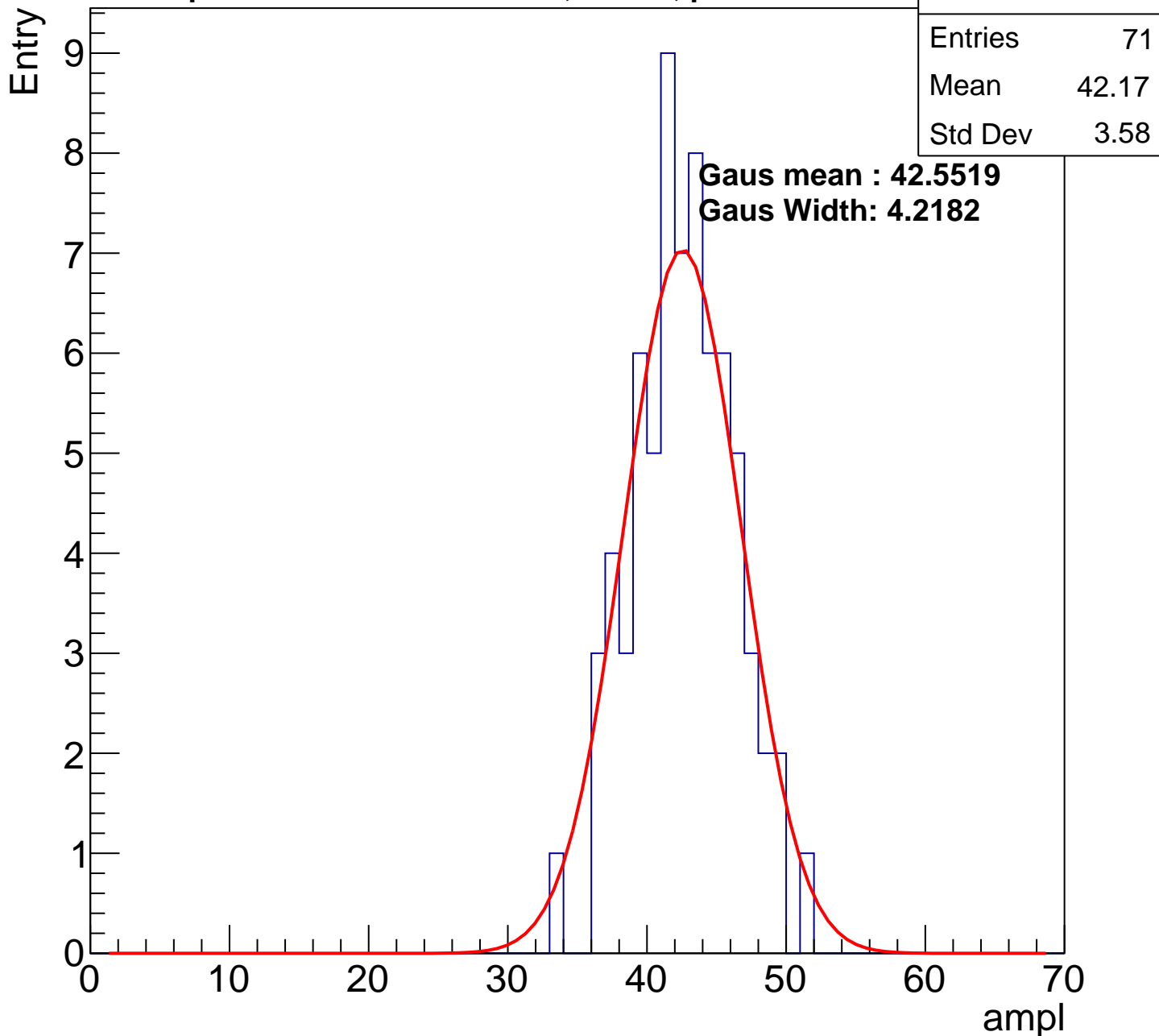
**Gaus mean : 35.4660**

**Gaus Width: 4.0635**



# B1L102S, U21-ch69, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

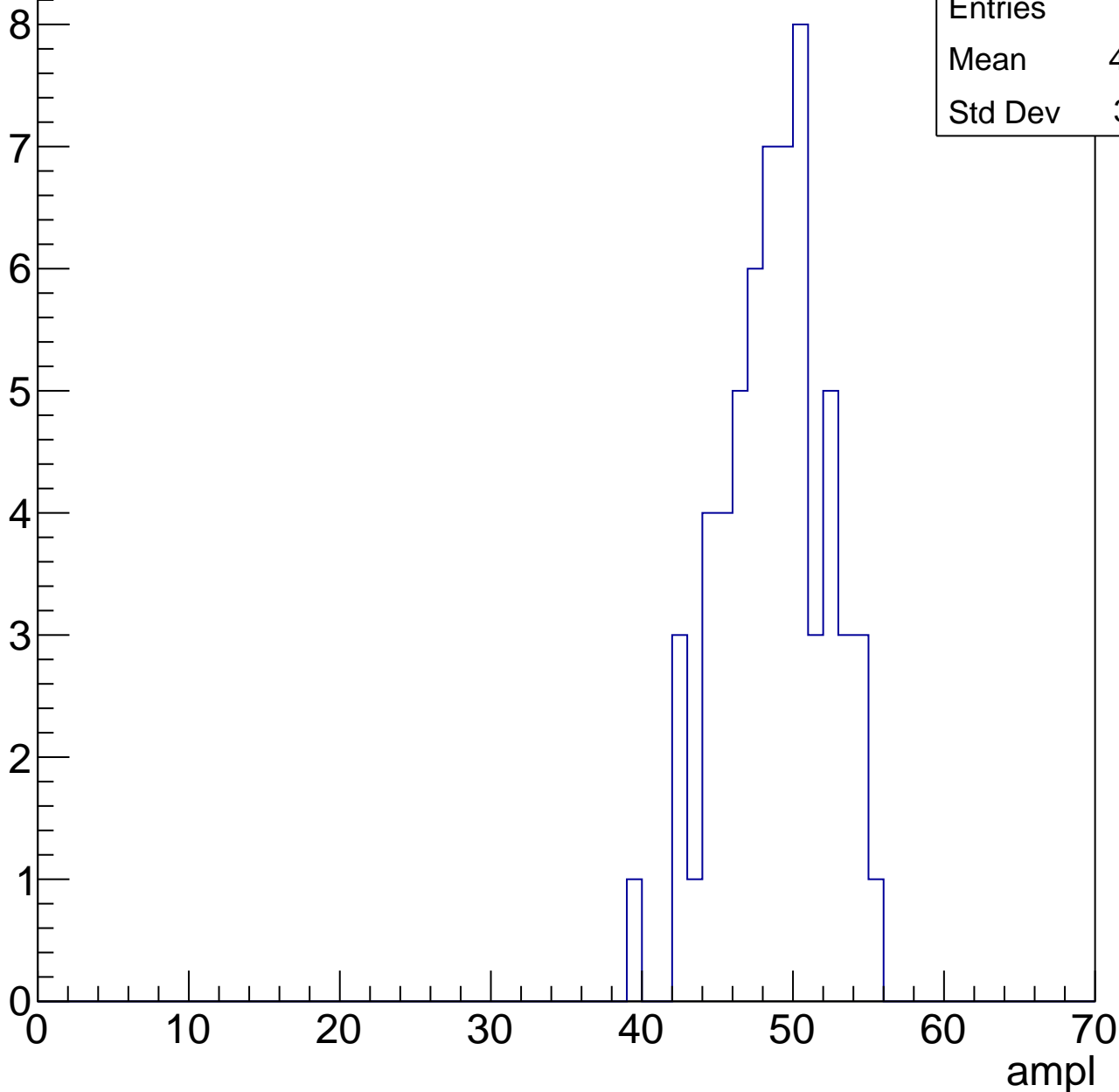


# B1L102S, U21-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	48.26
Std Dev	3.421

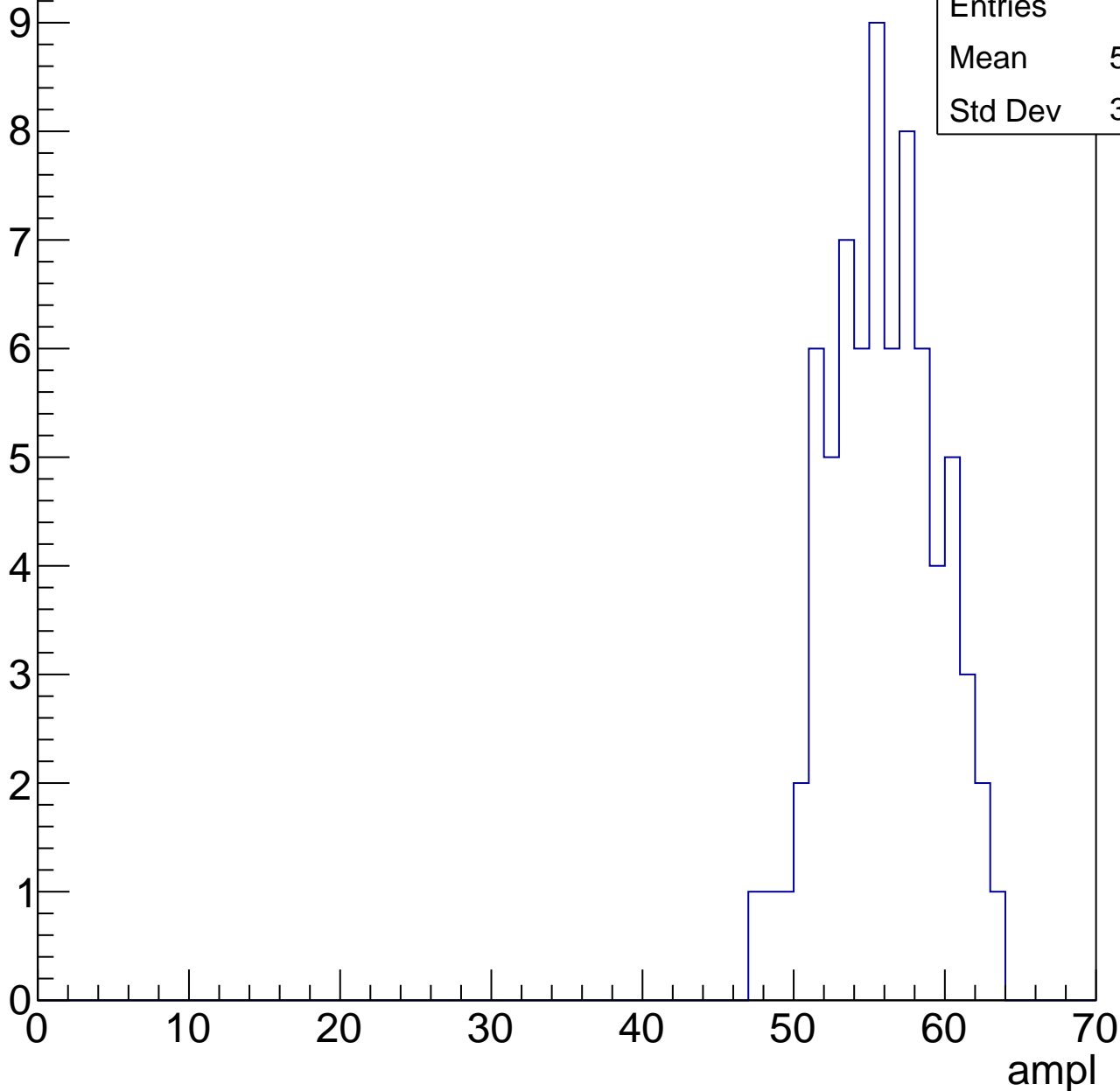


# B1L102S, U21-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	55.42
Std Dev	3.534

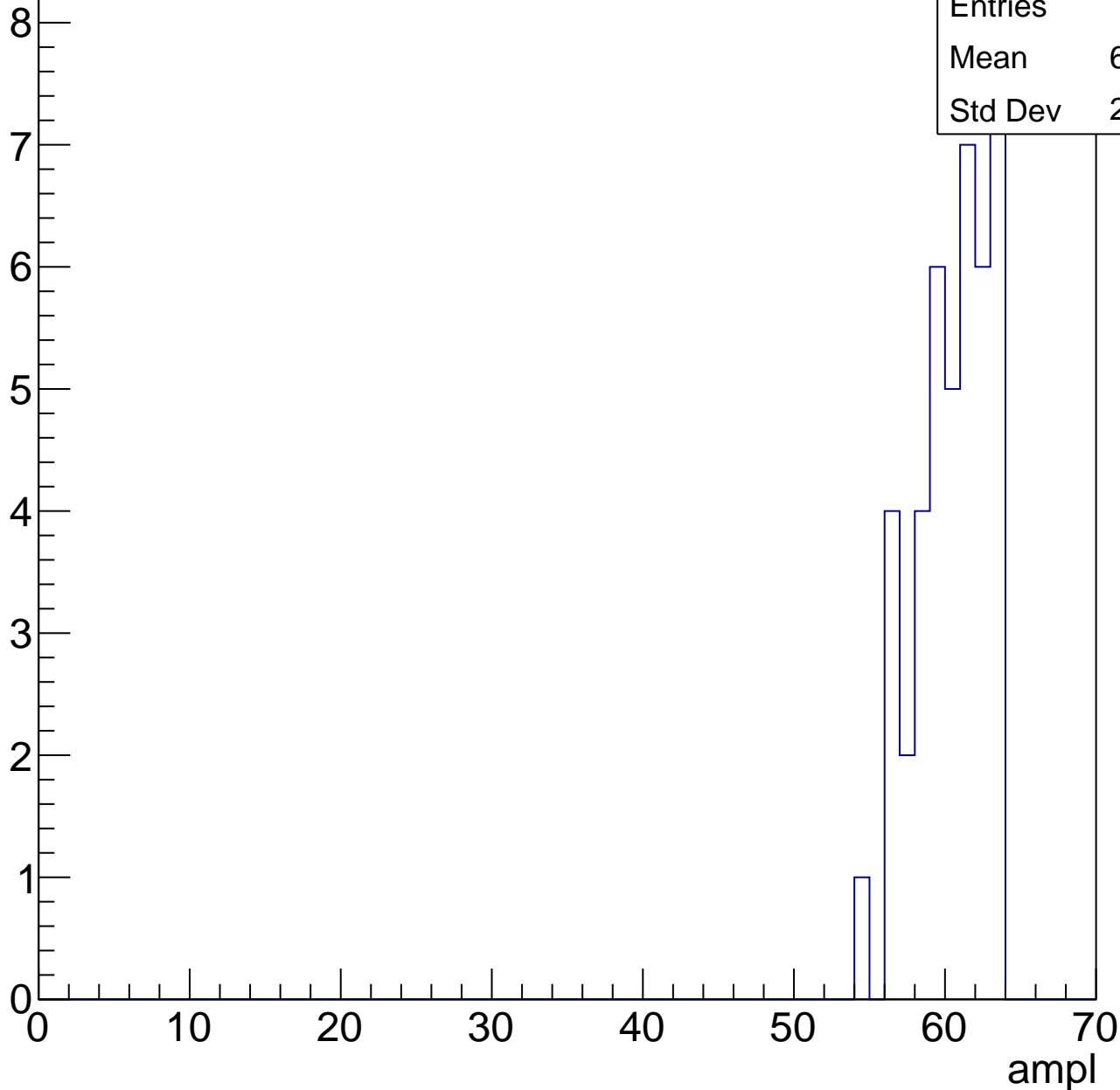


# B1L102S, U21-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	43
Mean	60.02
Std Dev	2.377



# B1L102S, U21-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	22
Std Dev	0

# B1L102S, U21-ch70, adc0

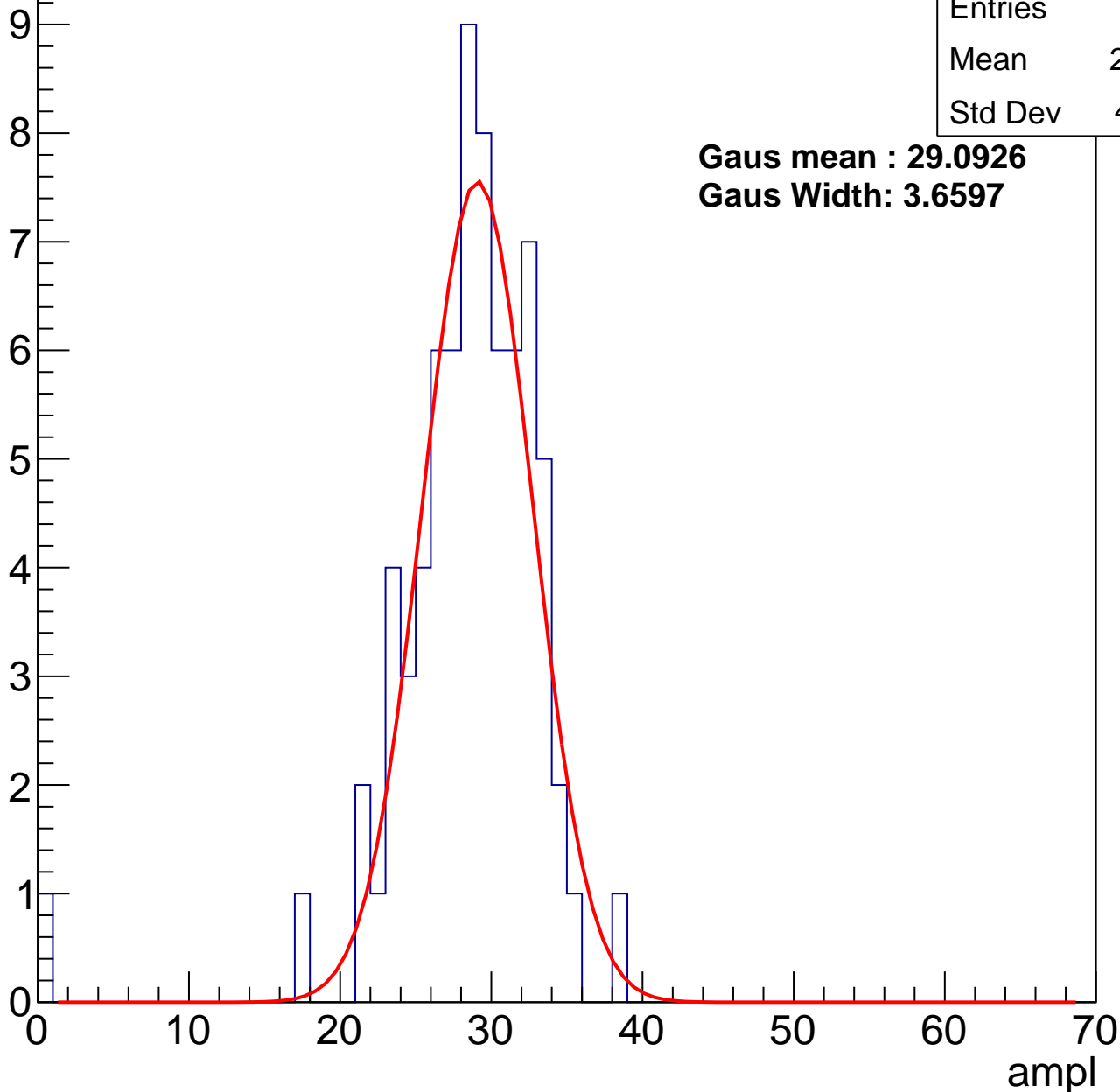
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	27.99
Std Dev	4.961

**Gaus mean : 29.0926**

**Gaus Width: 3.6597**



# B1L102S, U21-ch70, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	77
Mean	36.26
Std Dev	3.551

**Gaus mean : 36.5439**

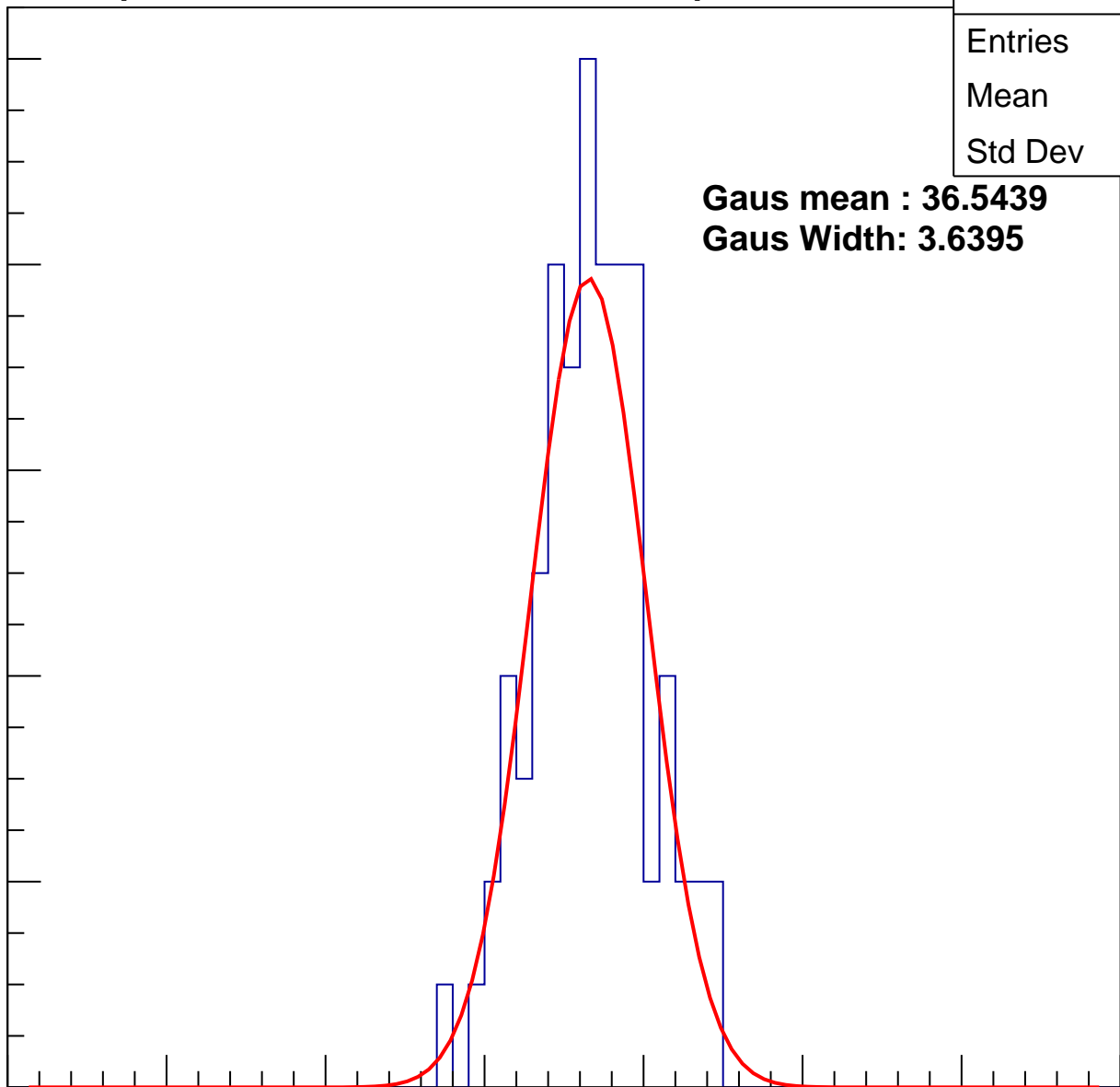
**Gaus Width: 3.6395**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U21-ch70, adc2

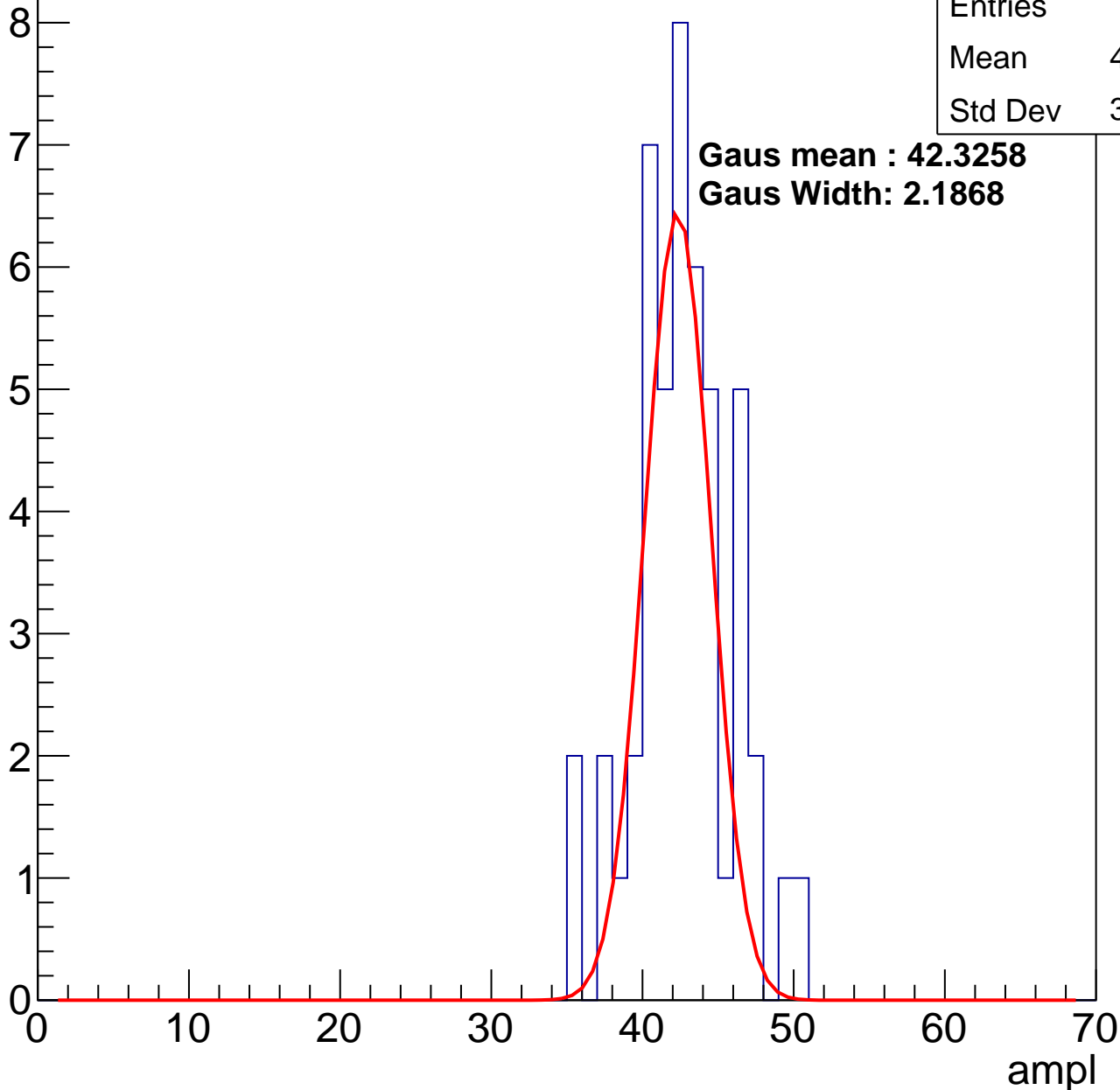
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	42.23
Std Dev	3.197

**Gaus mean : 42.3258**

**Gaus Width: 2.1868**

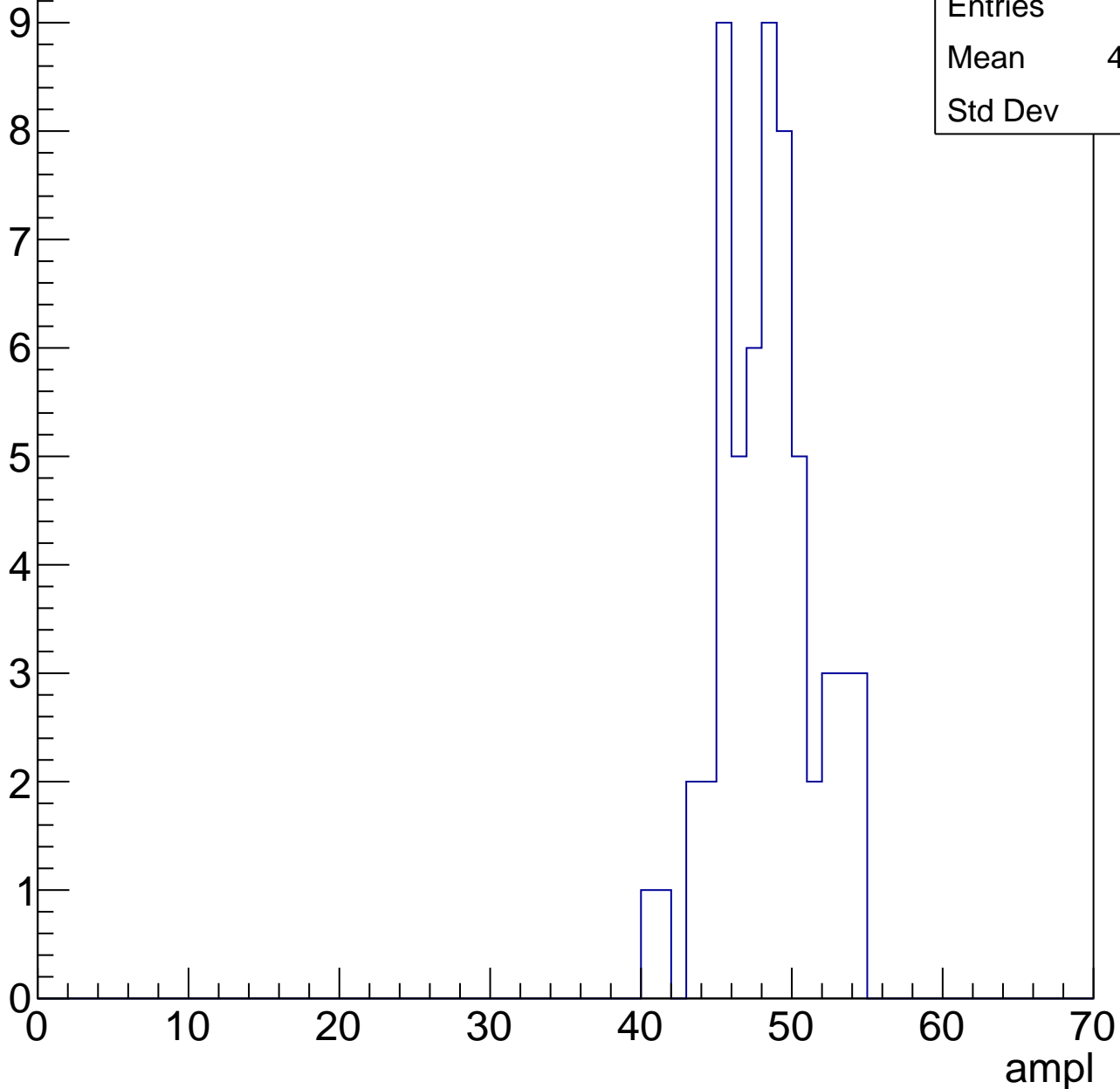


# B1L102S, U21-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	47.88
Std Dev	3.13

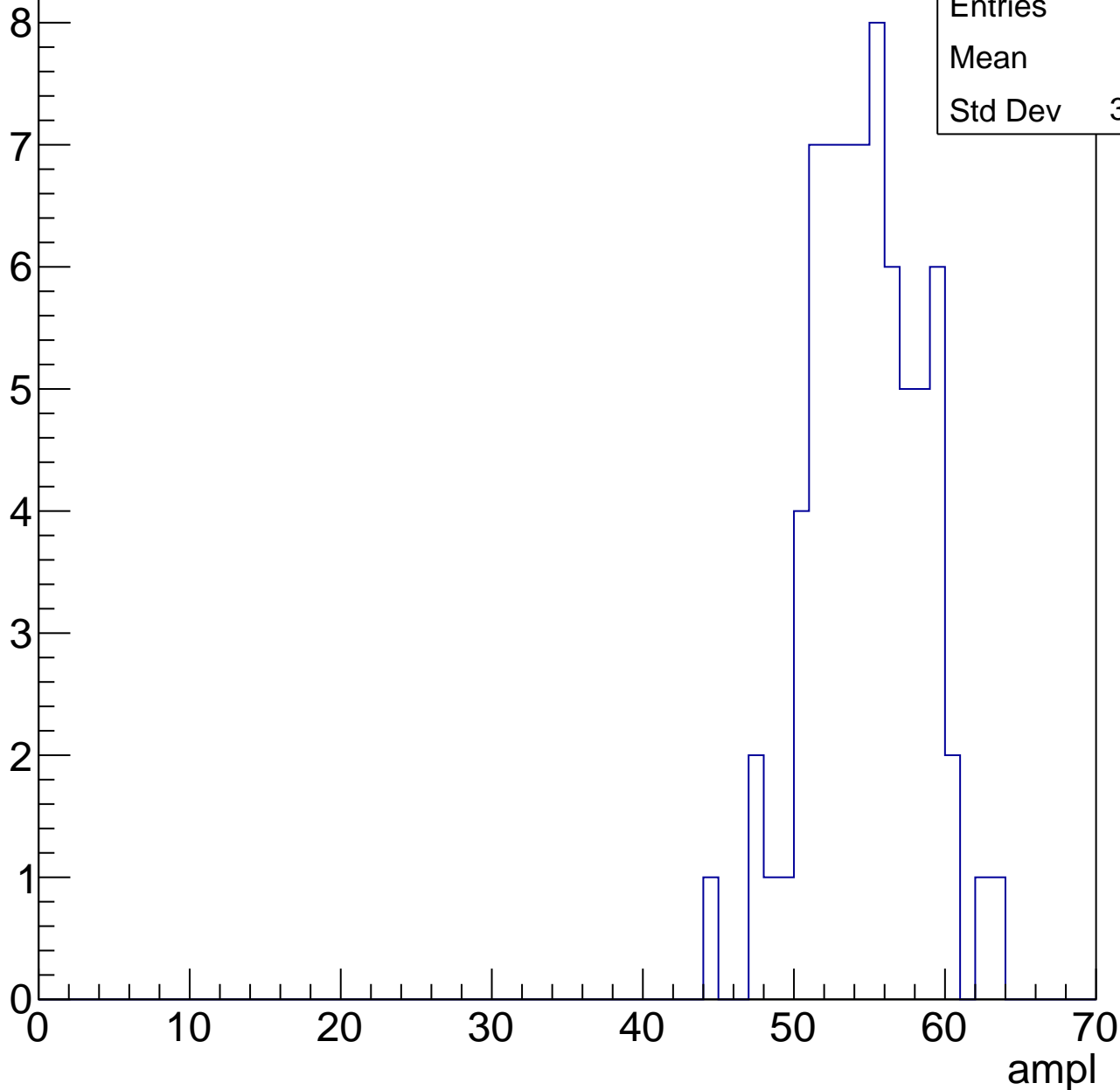


# B1L102S, U21-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	54.3
Std Dev	3.636

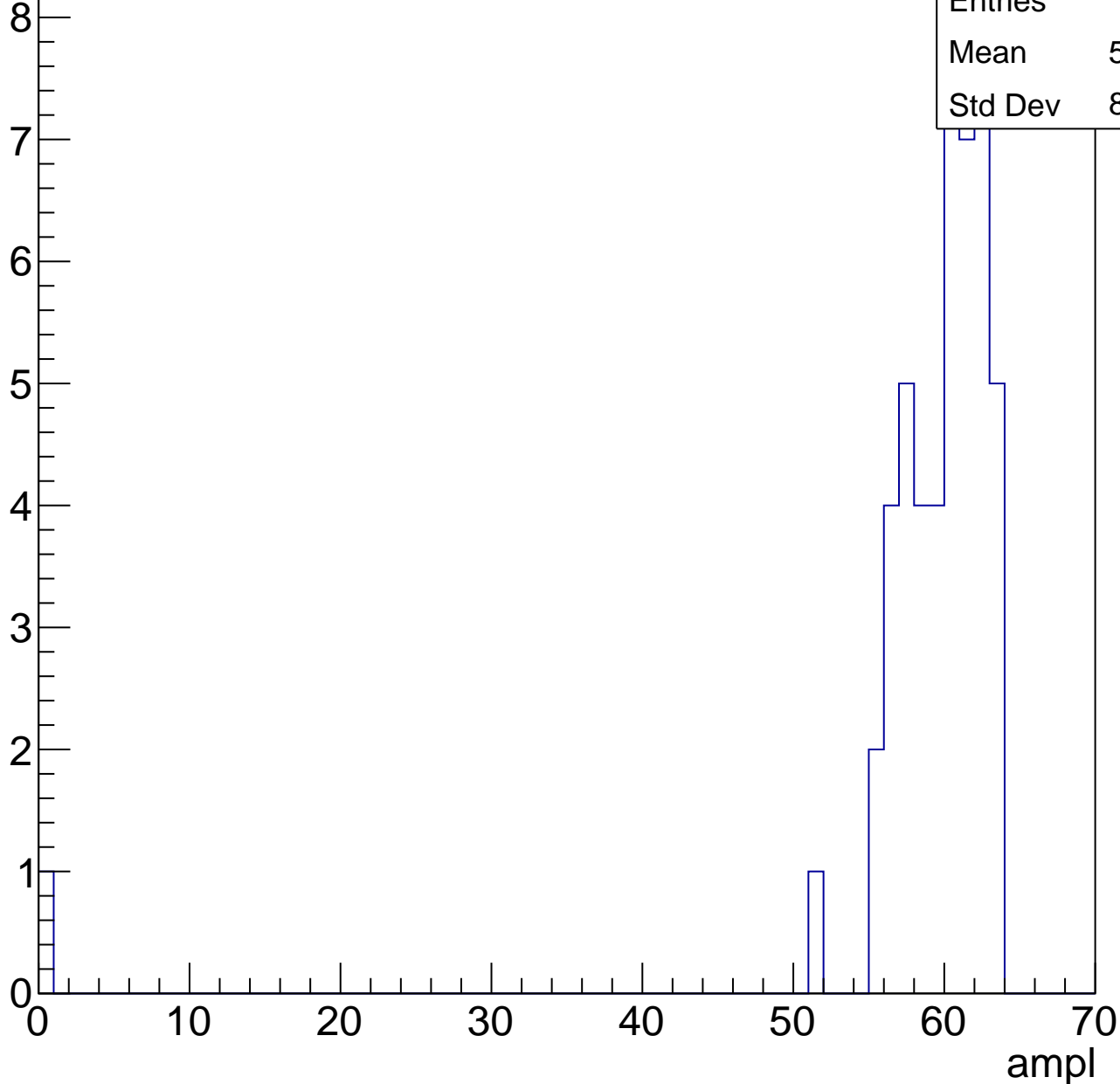


# B1L102S, U21-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	58.29
Std Dev	8.806



# B1L102S, U21-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

8

Mean

61.5

Std Dev

1.581

Entries	8
Mean	61.5
Std Dev	1.581



# B1L102S, U21-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch71, adc0

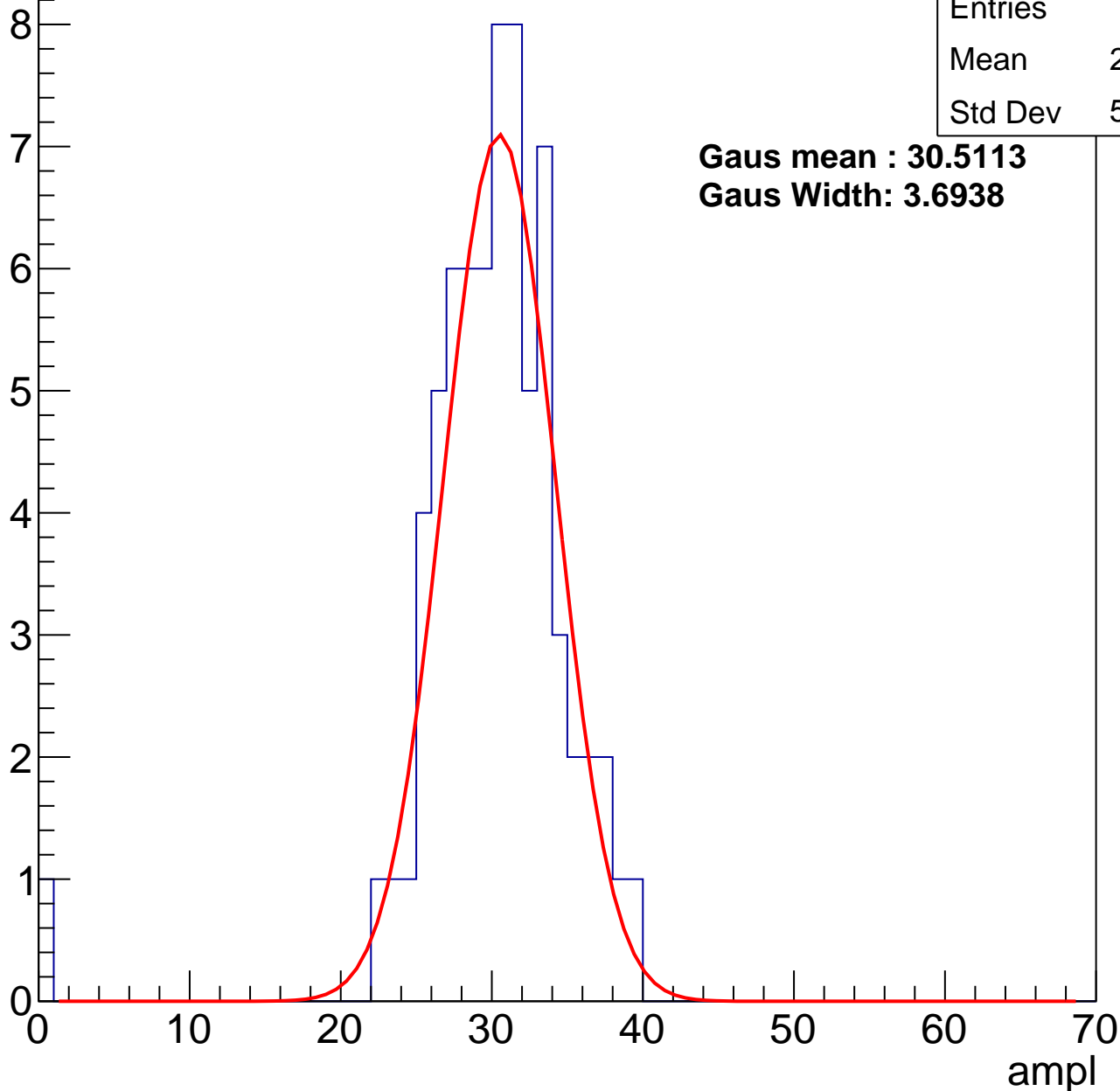
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	29.67
Std Dev	5.084

**Gaus mean : 30.5113**

**Gaus Width: 3.6938**



# B1L102S, U21-ch71, adc1

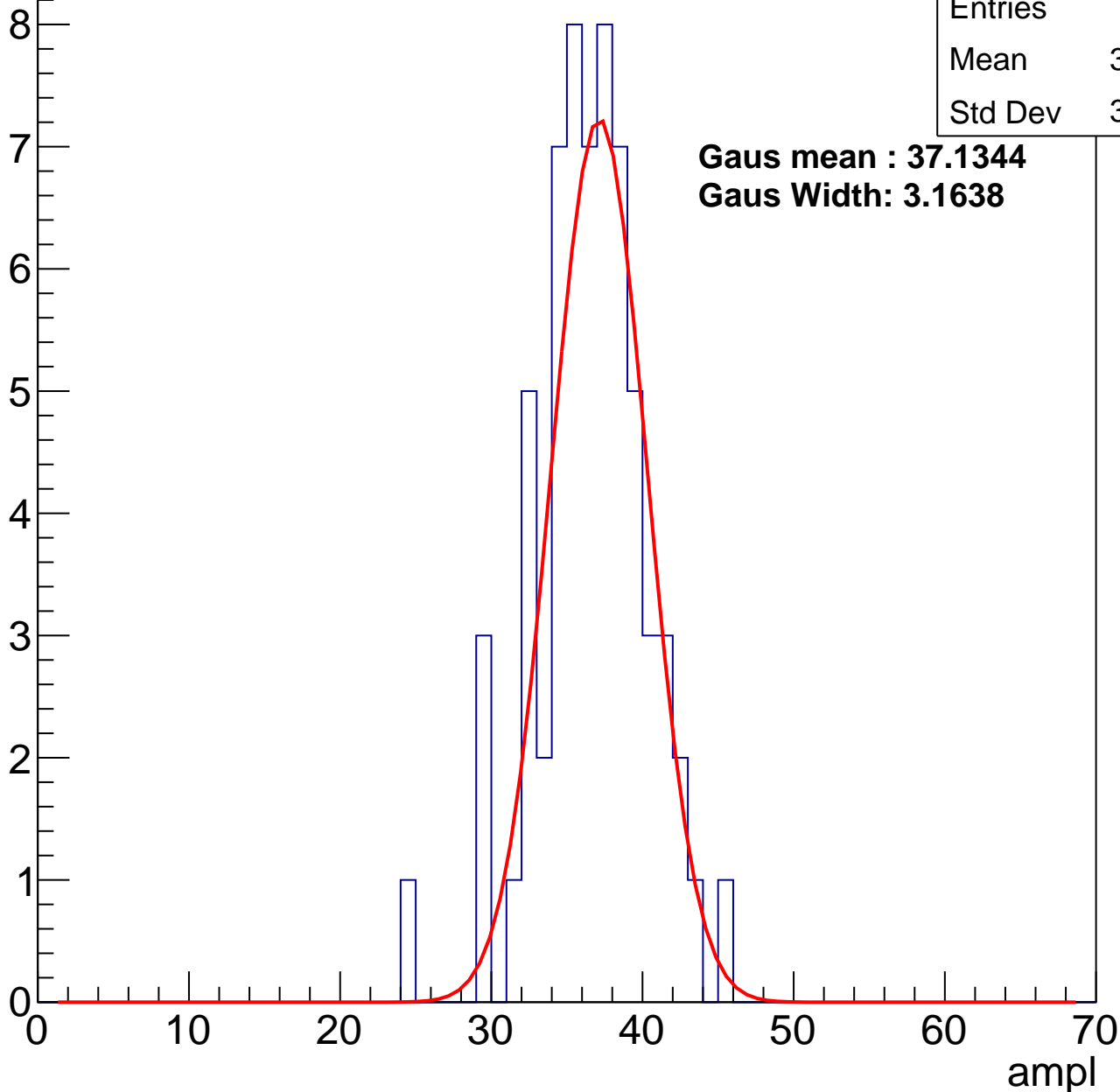
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	36.09
Std Dev	3.656

**Gaus mean : 37.1344**

**Gaus Width: 3.1638**



# B1L102S, U21-ch71, adc2

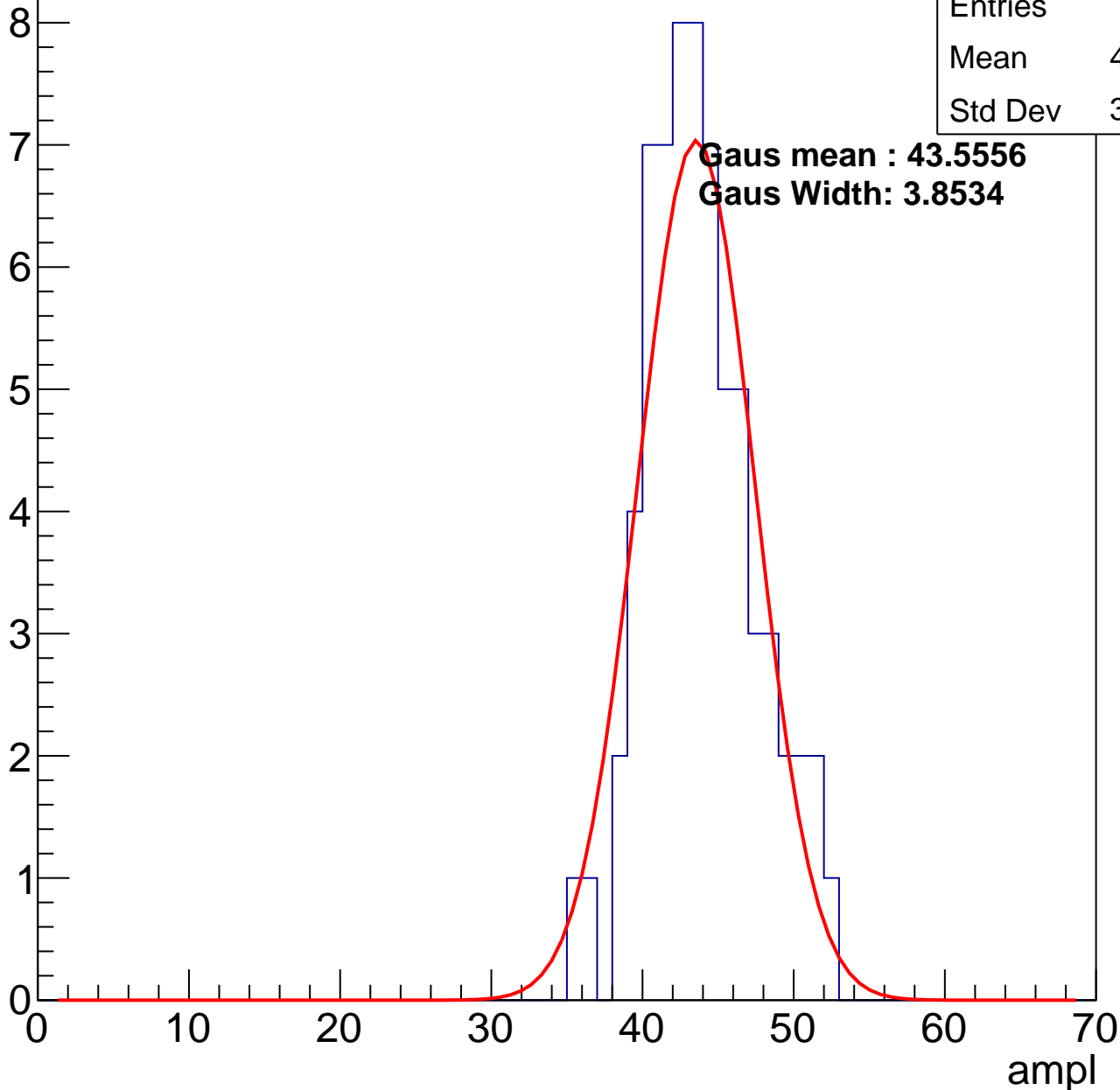
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	43.38
Std Dev	3.618

**Gaus mean : 43.5556**

**Gaus Width: 3.8534**

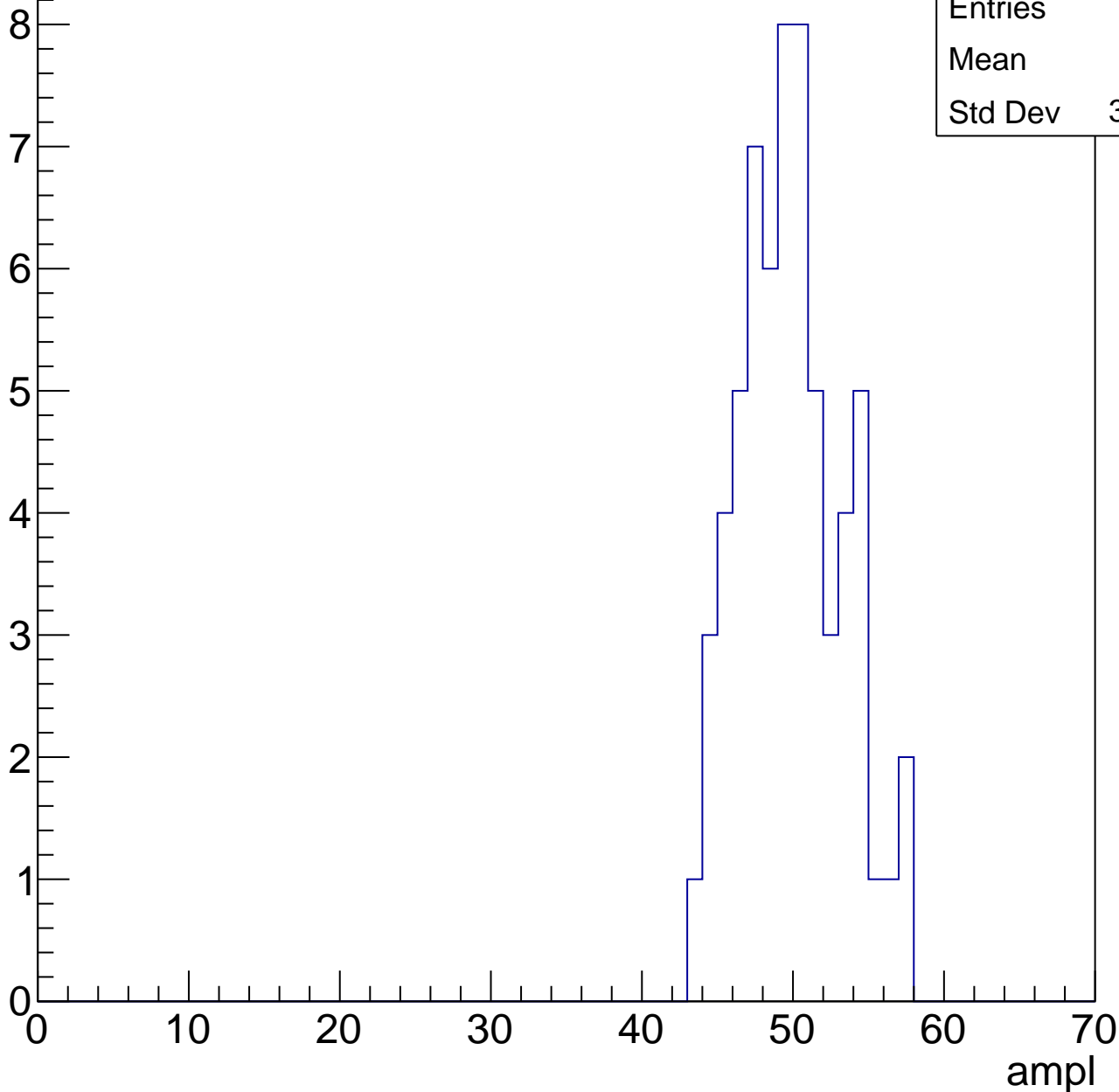


# B1L102S, U21-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	49.4
Std Dev	3.336

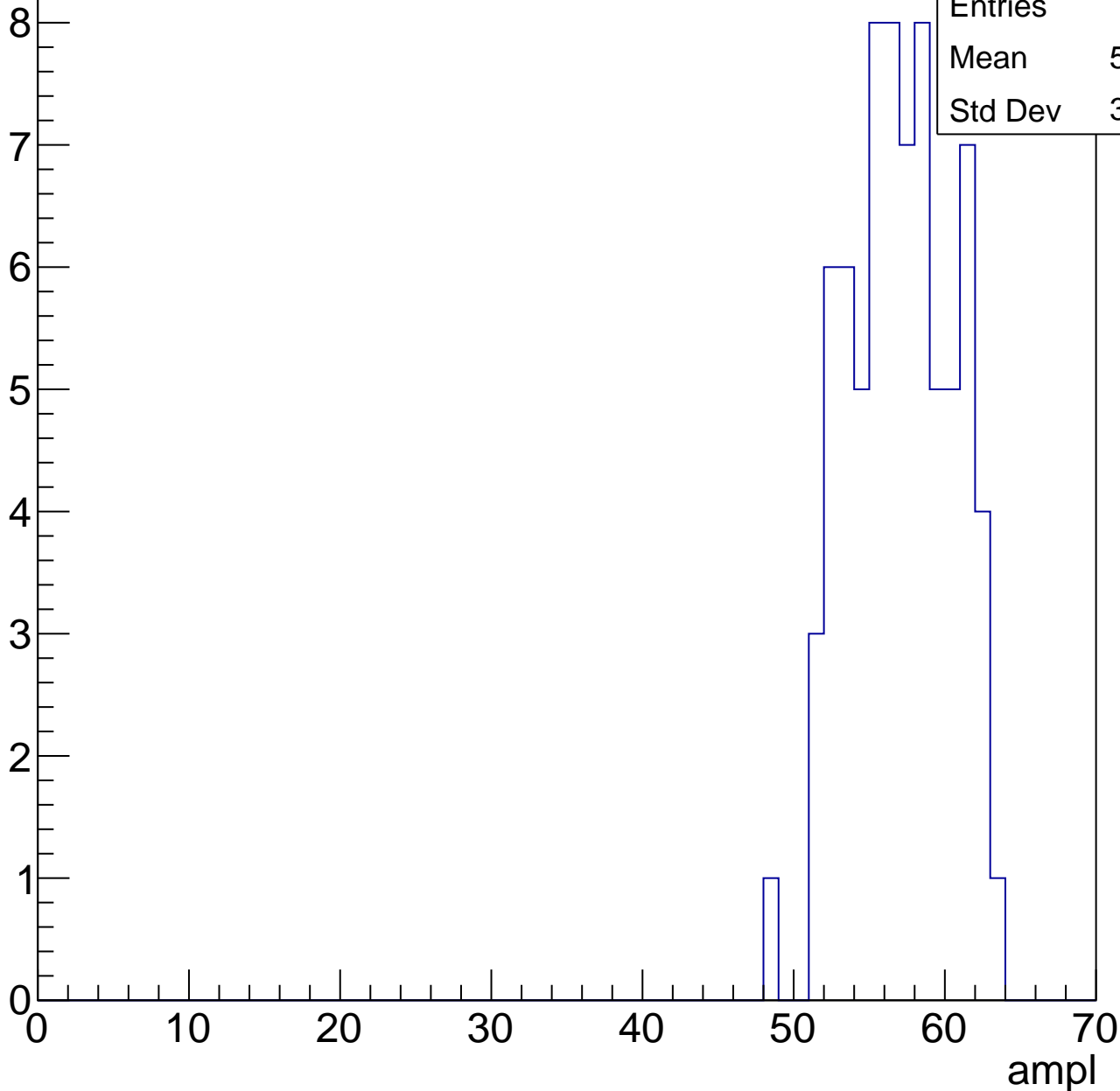


# B1L102S, U21-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	56.55
Std Dev	3.342

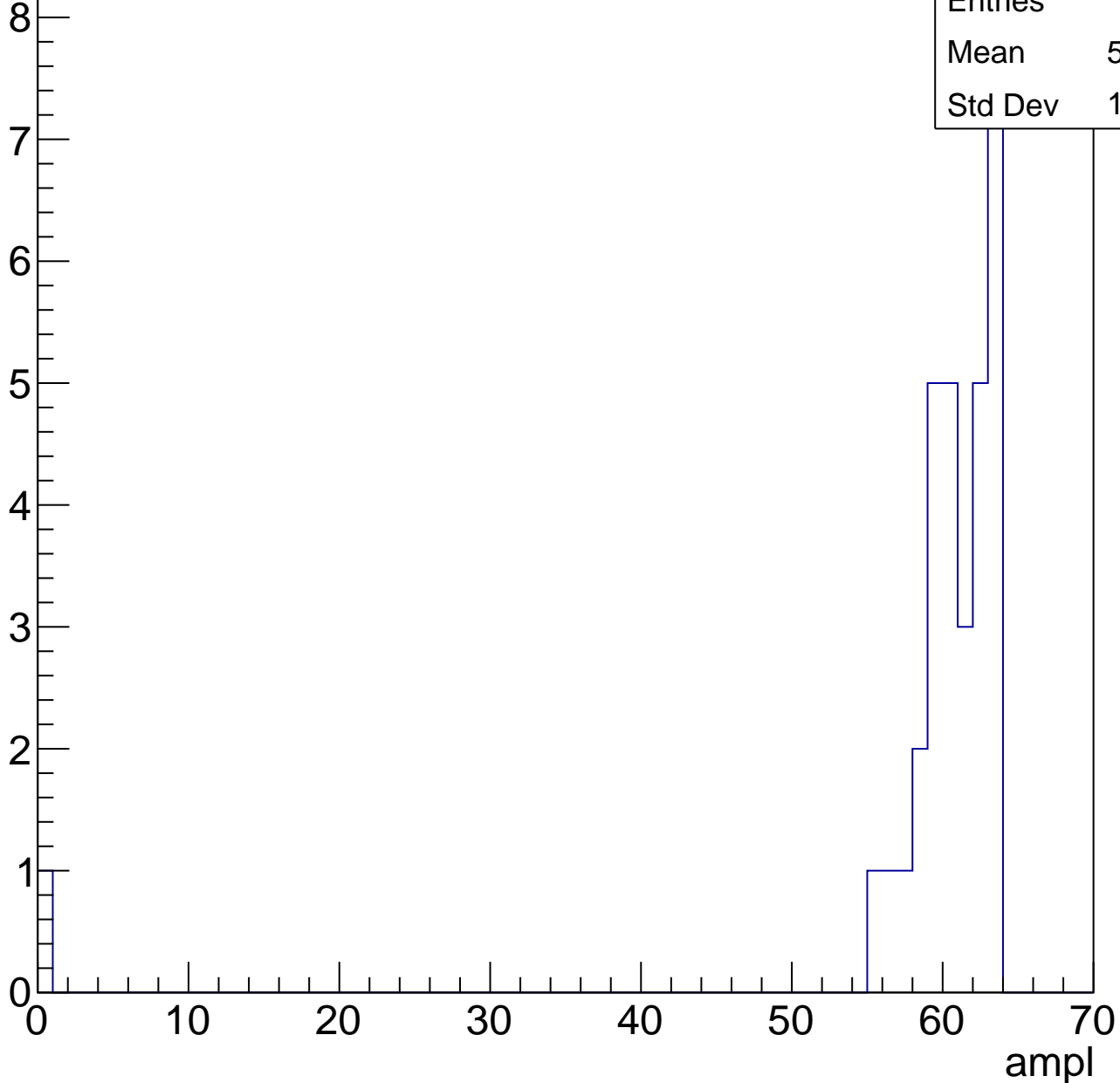


# B1L102S, U21-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	32
Mean	58.62
Std Dev	10.75



# B1L102S, U21-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch72, adc0

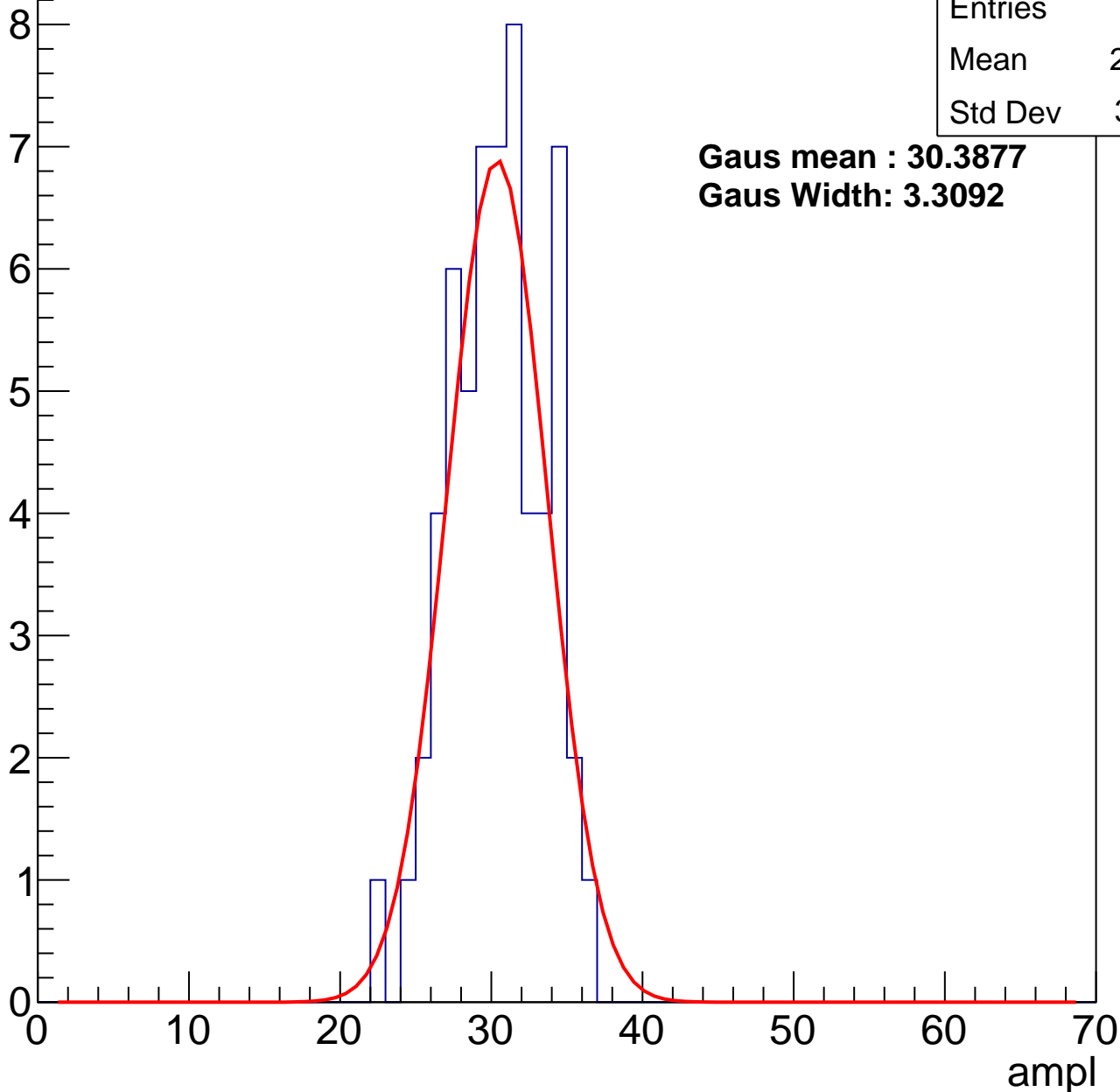
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	29.95
Std Dev	3.061

**Gaus mean : 30.3877**

**Gaus Width: 3.3092**



# B1L102S, U21-ch72, adc1

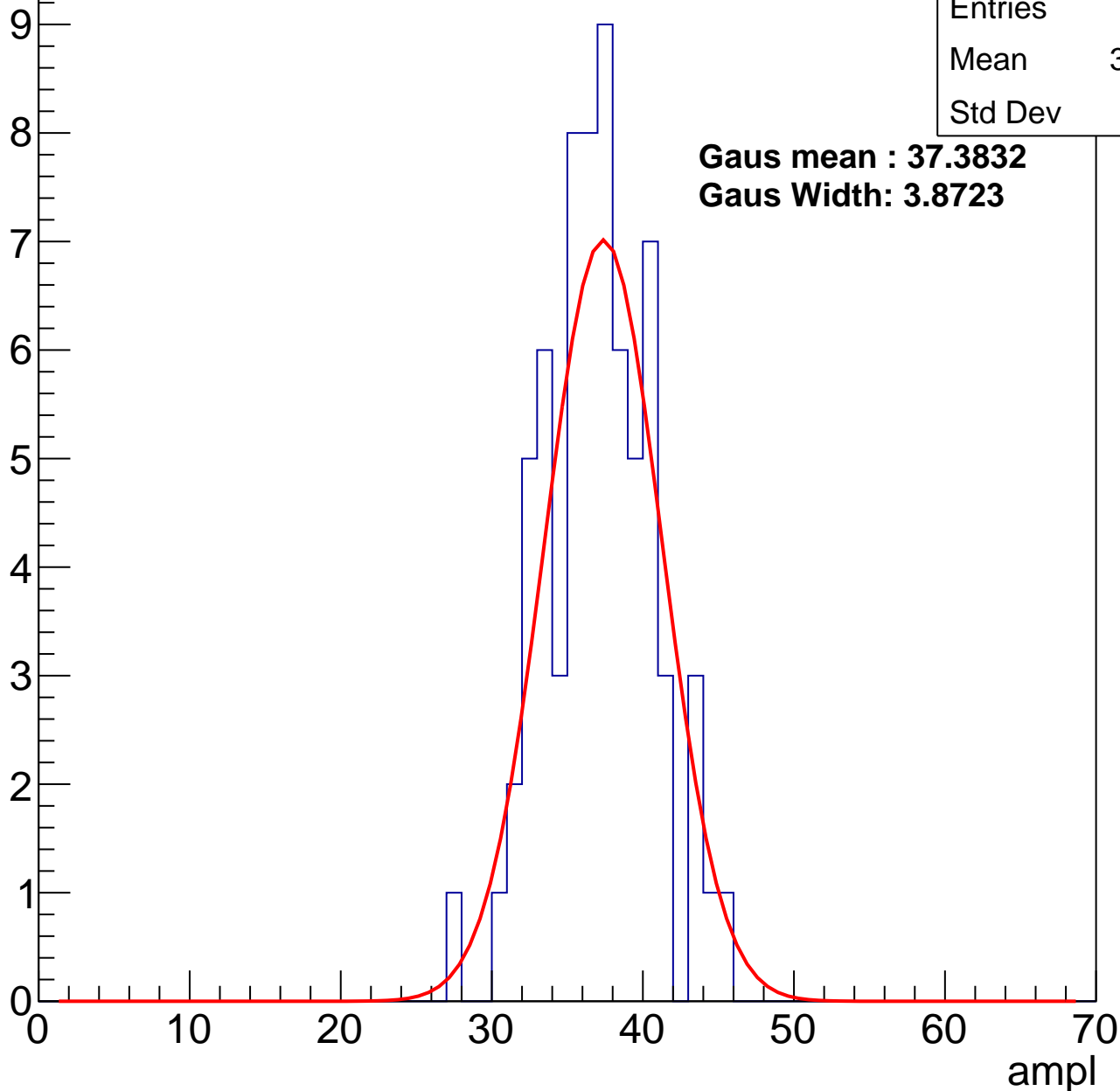
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	36.58
Std Dev	3.52

**Gaus mean : 37.3832**

**Gaus Width: 3.8723**



# B1L102S, U21-ch72, adc2

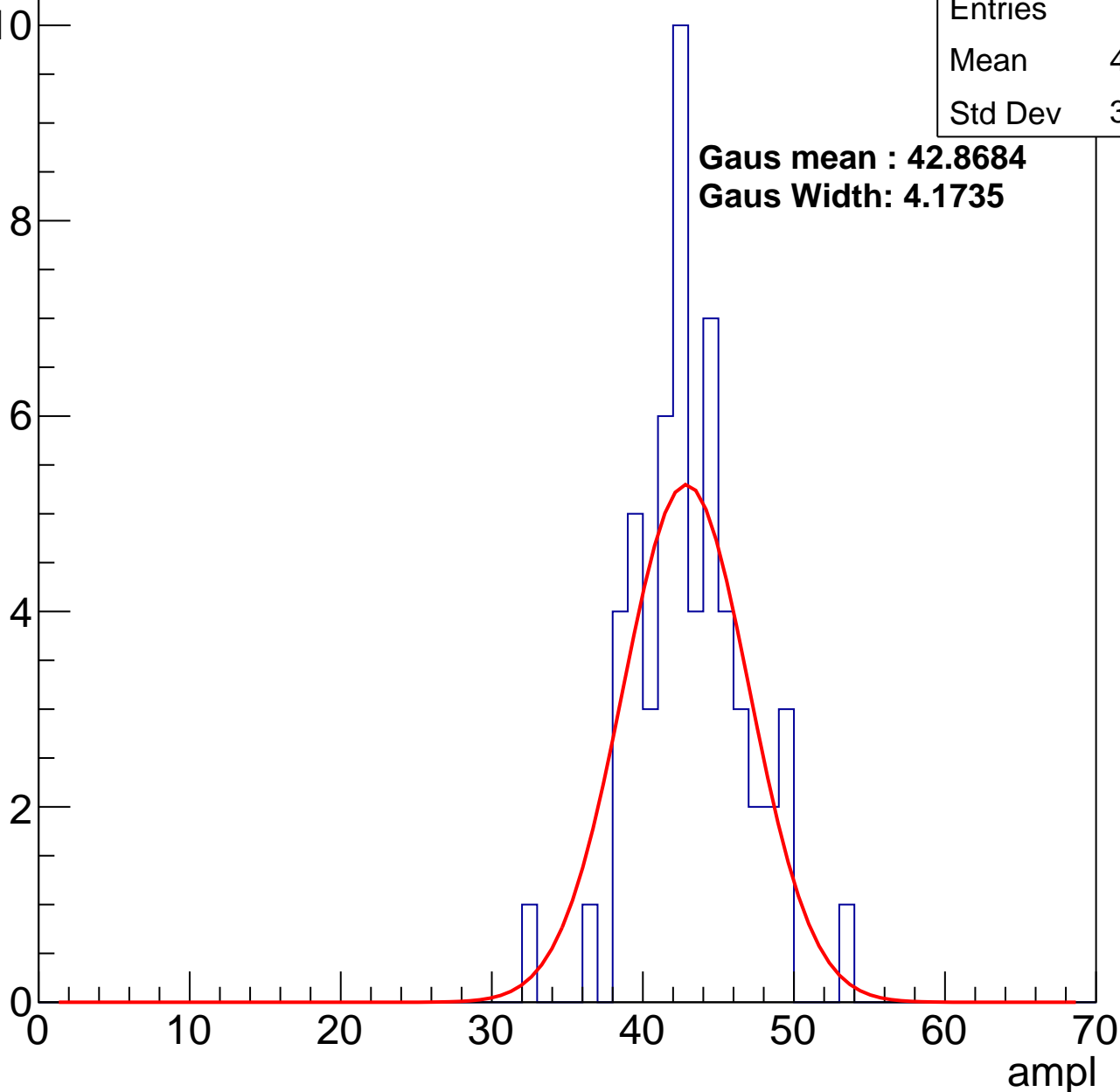
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	42.66
Std Dev	3.646

**Gaus mean : 42.8684**

**Gaus Width: 4.1735**

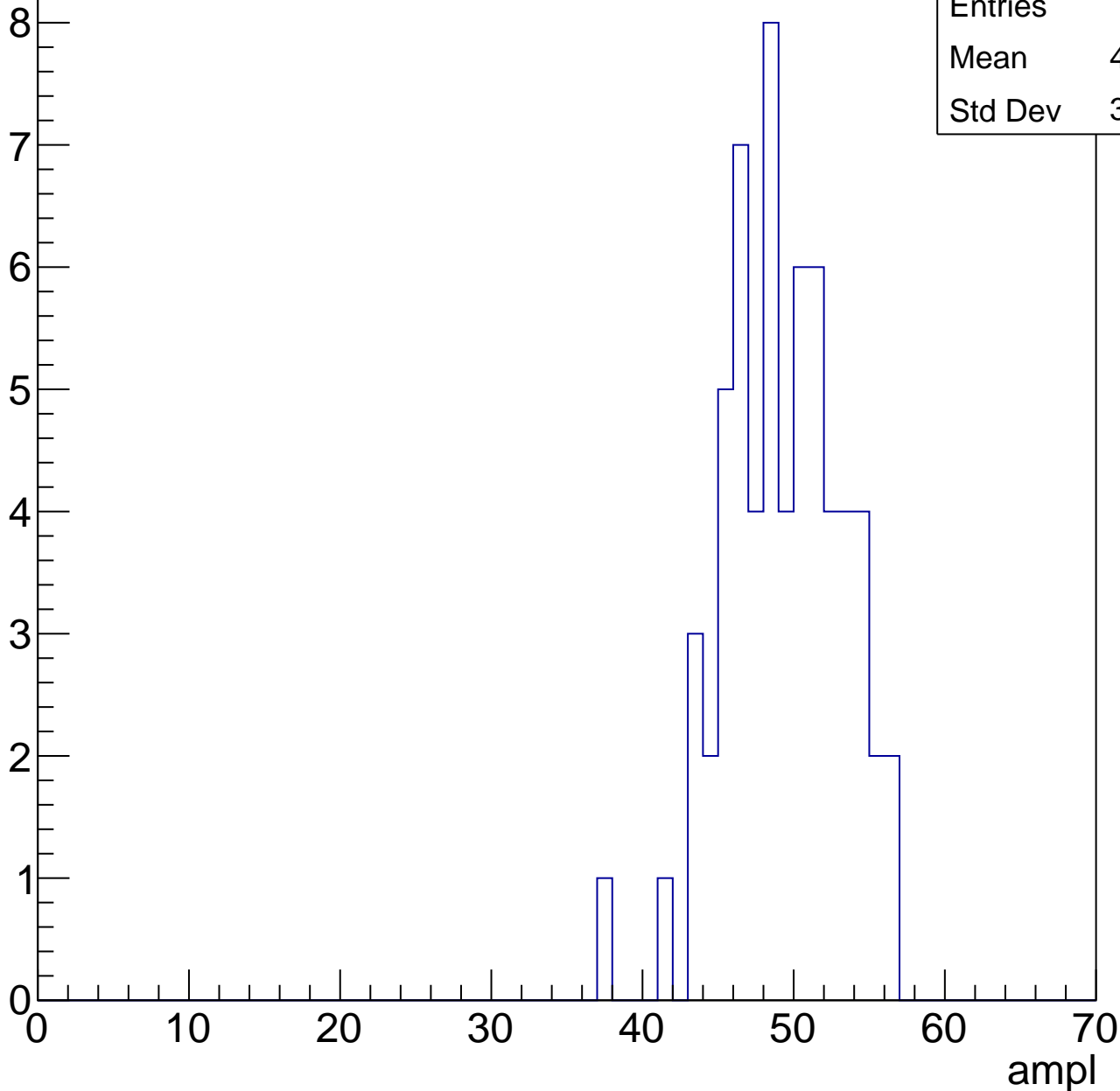


# B1L102S, U21-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	48.79
Std Dev	3.843

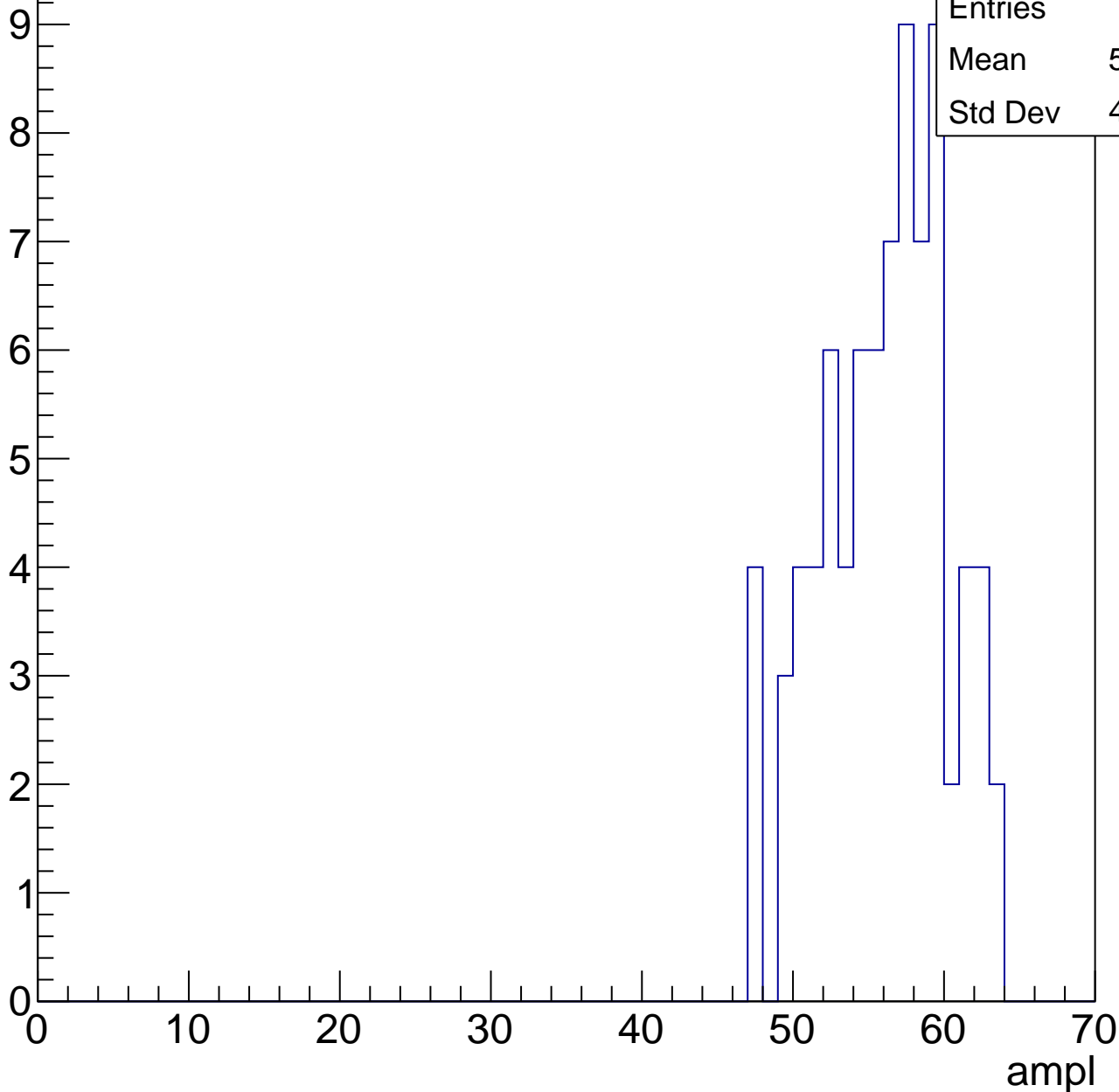


# B1L102S, U21-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	81
Mean	55.52
Std Dev	4.083

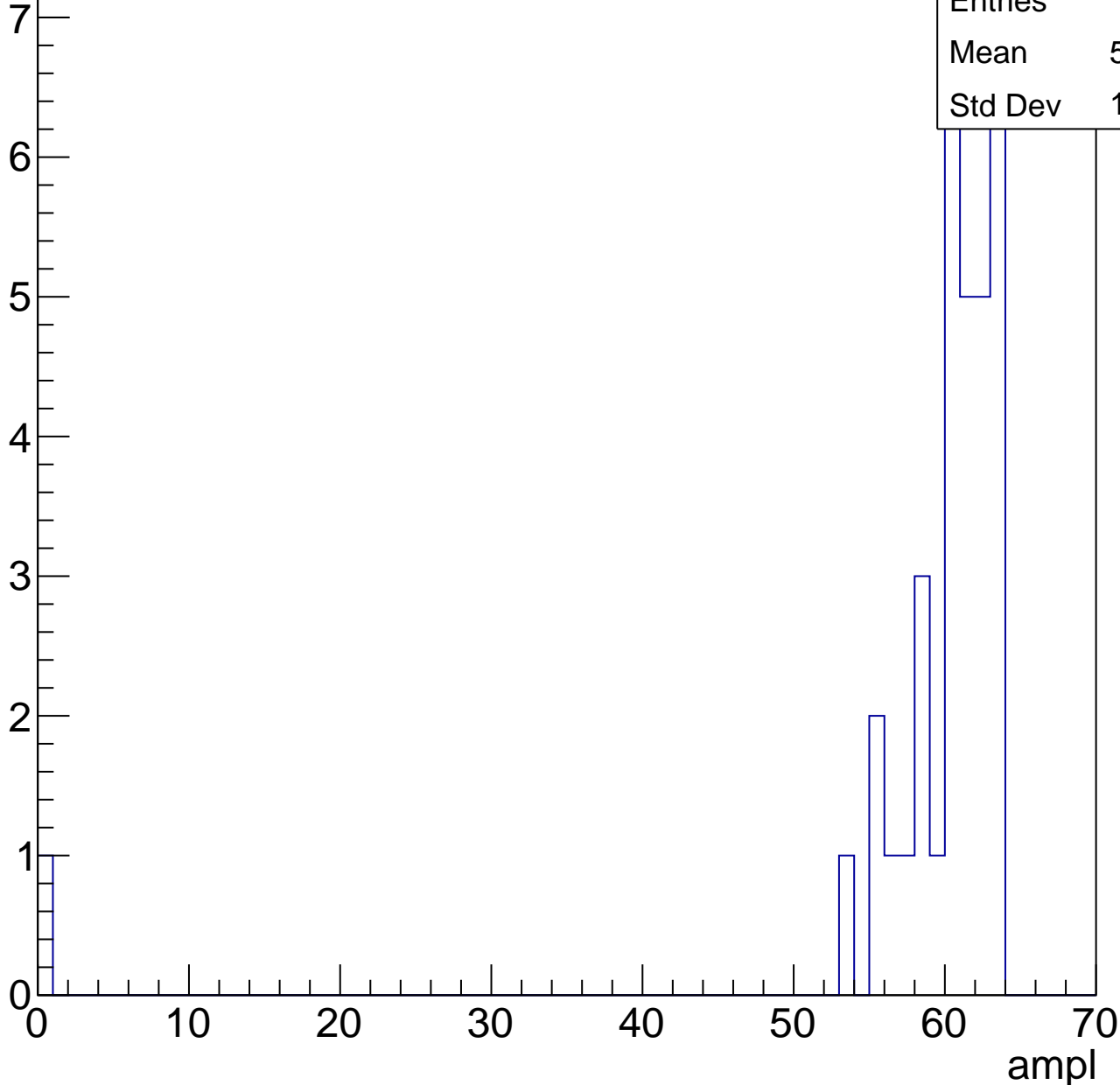


# B1L102S, U21-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	34
Mean	58.38
Std Dev	10.48



# B1L102S, U21-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

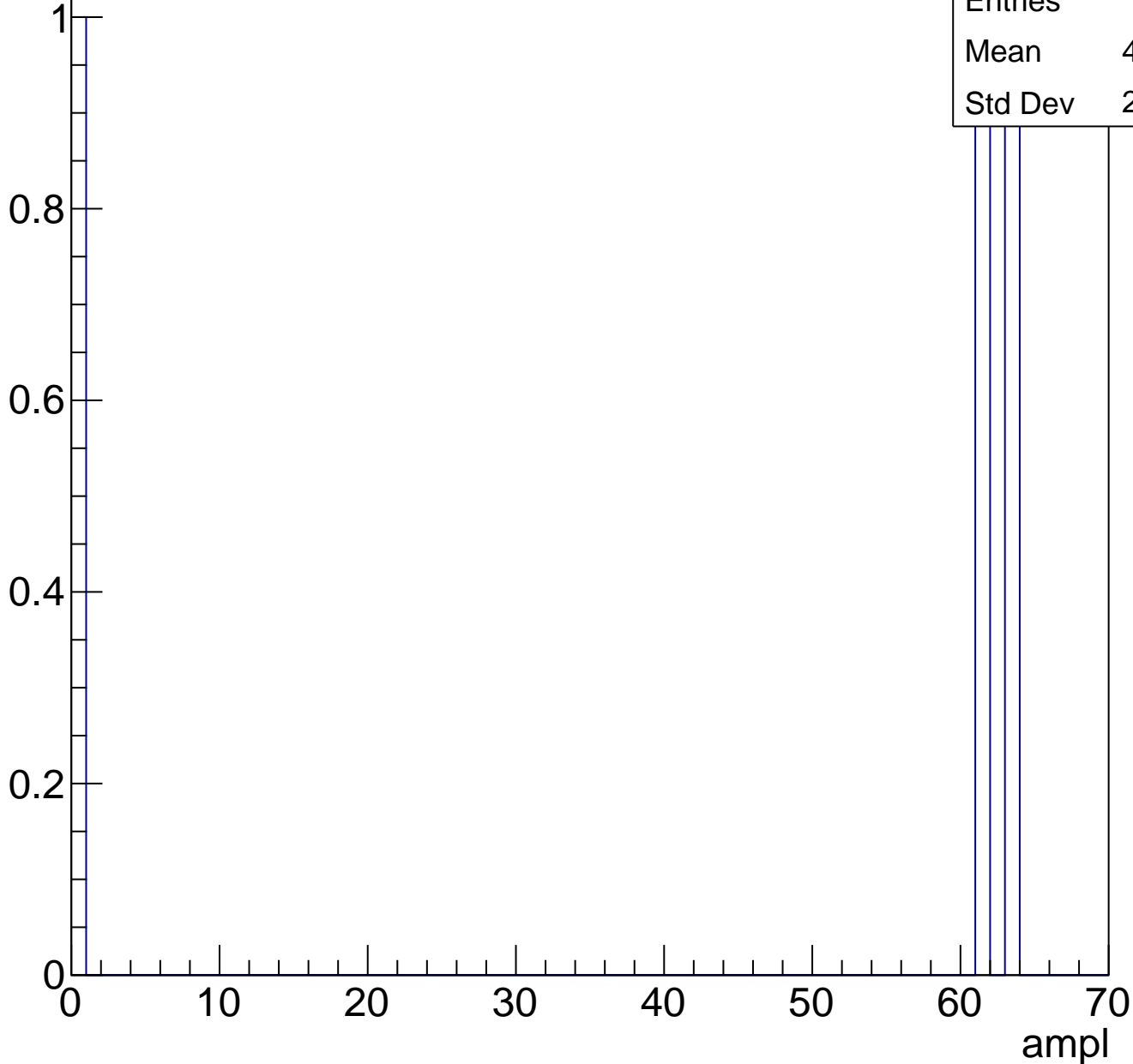




# B1L102S, U21-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch73, adc0

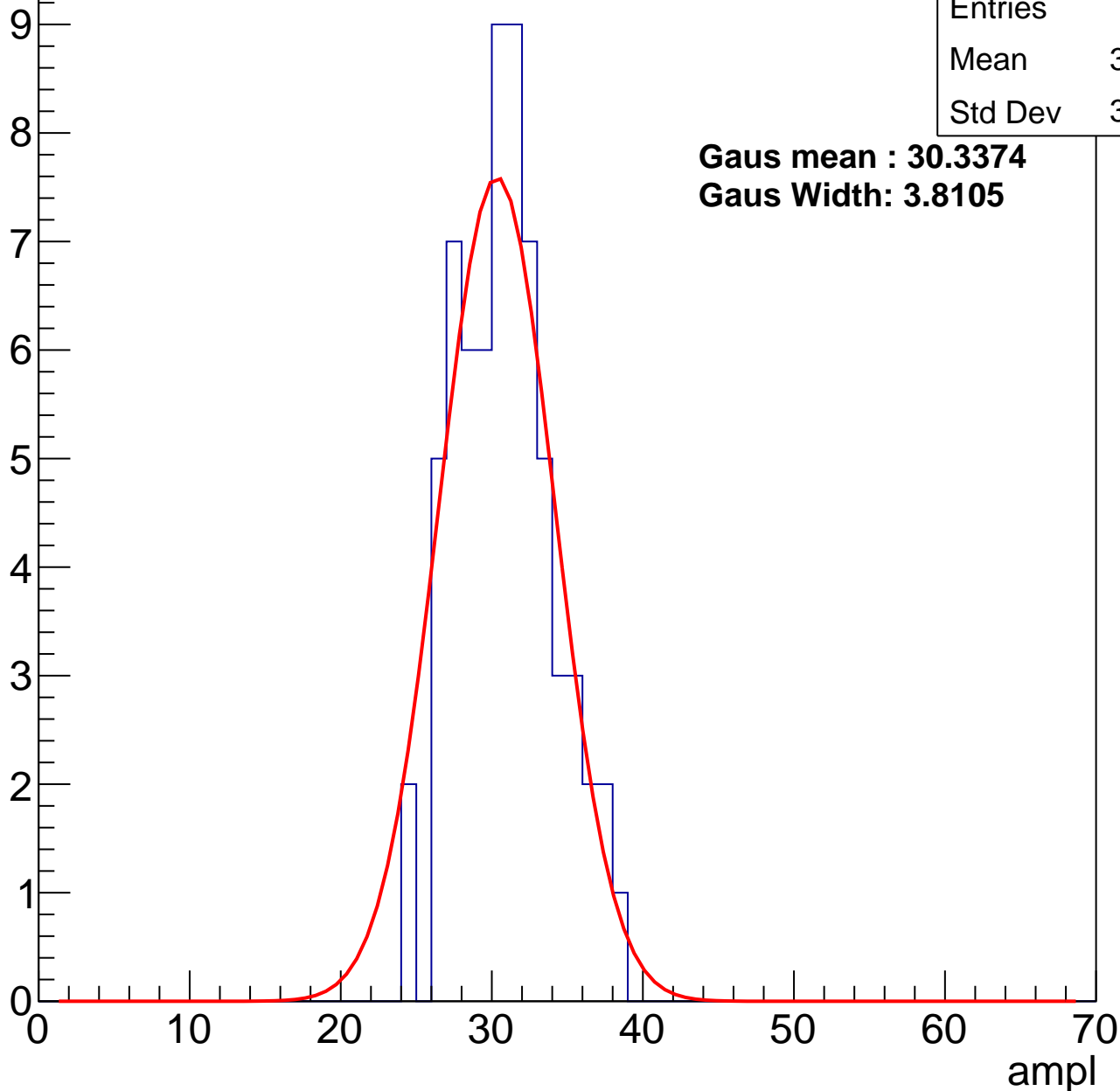
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	30.42
Std Dev	3.168

**Gaus mean : 30.3374**

**Gaus Width: 3.8105**



# B1L102S, U21-ch73, adc1

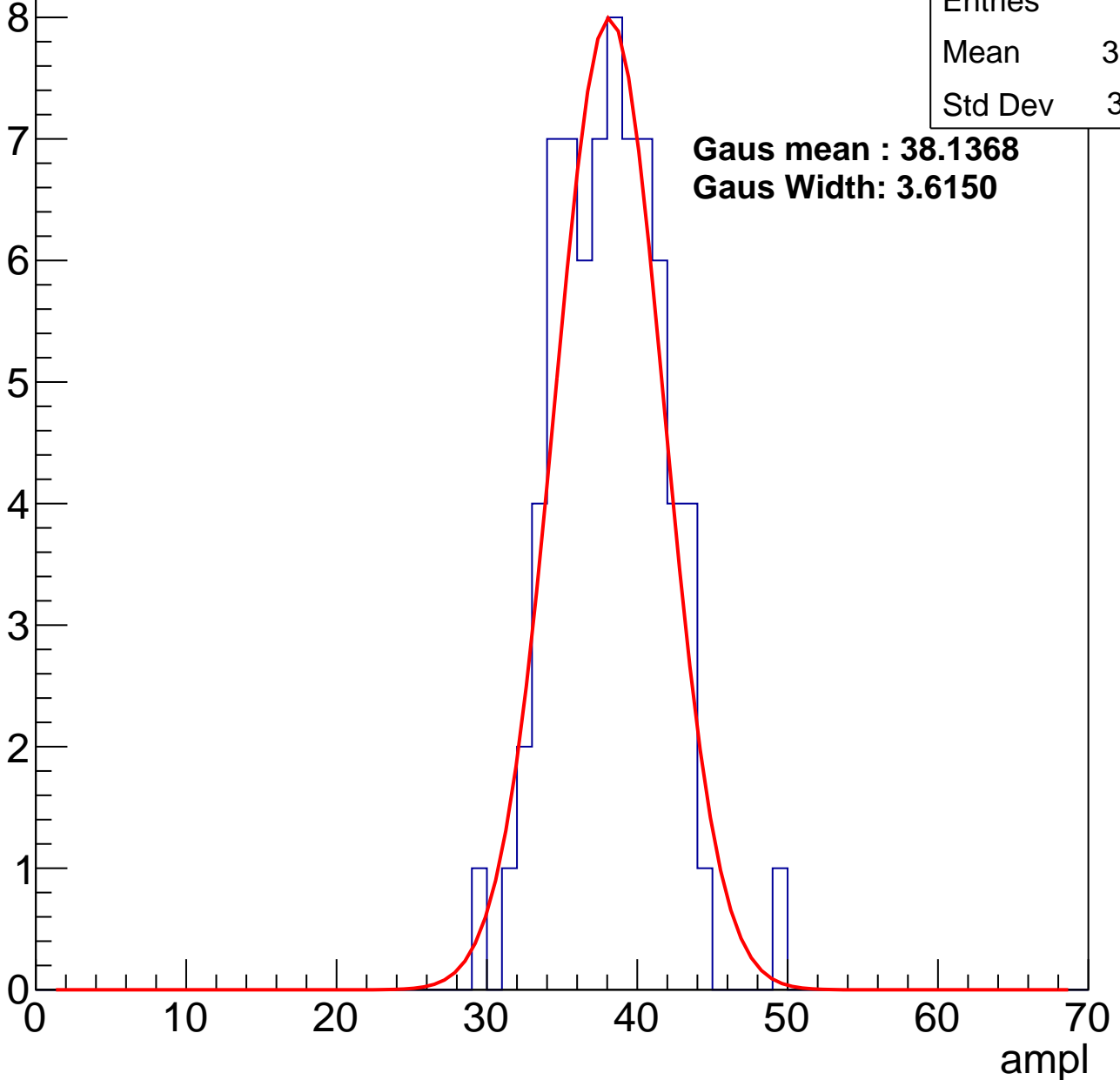
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	37.67
Std Dev	3.531

**Gaus mean : 38.1368**

**Gaus Width: 3.6150**



# B1L102S, U21-ch73, adc2

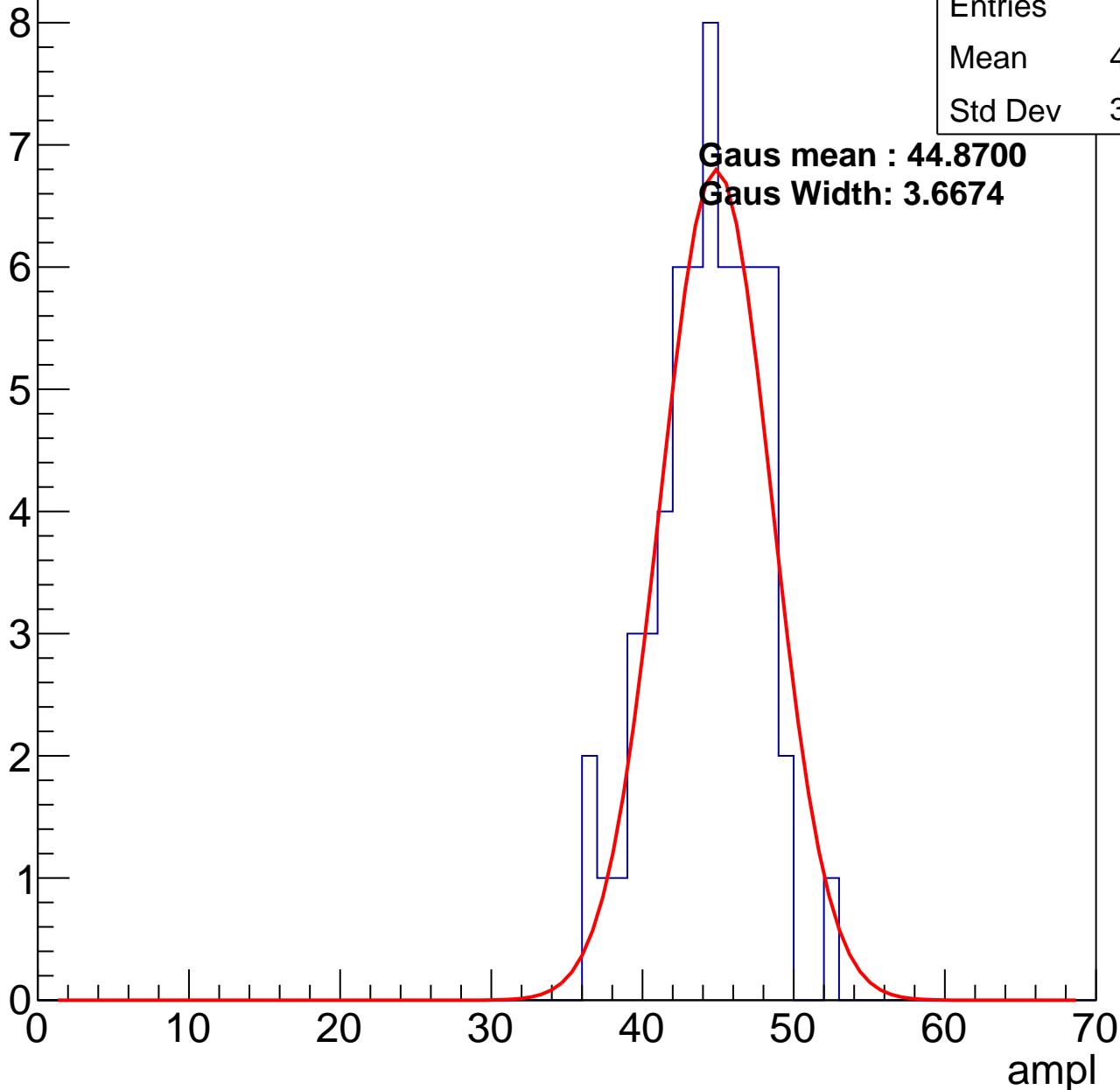
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	43.87
Std Dev	3.375

**Gaus mean : 44.8700**

**Gaus Width: 3.6674**

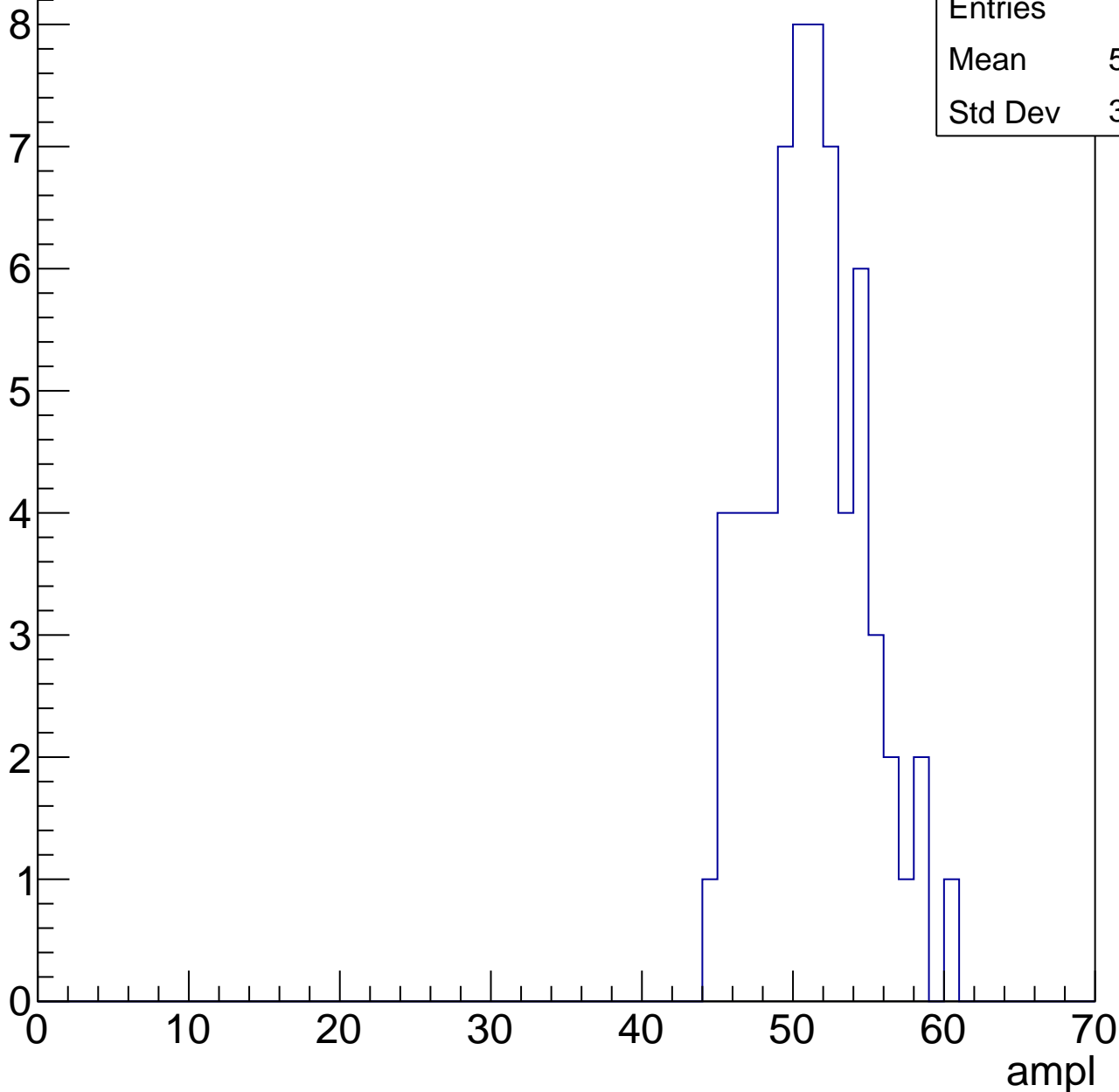


# B1L102S, U21-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

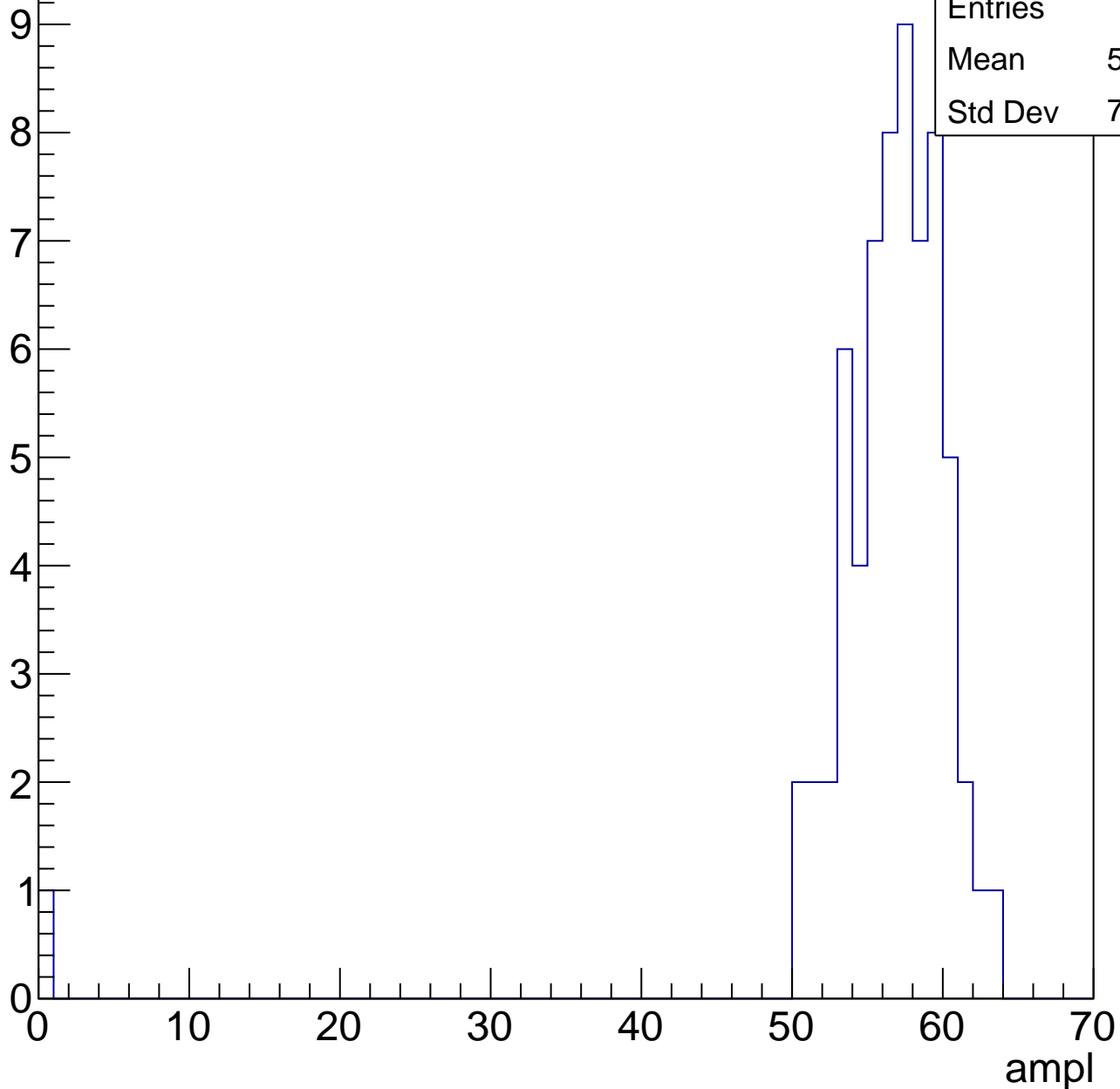
Entries	66
Mean	50.74
Std Dev	3.513



# B1L102S, U21-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	65
Mean	55.55
Std Dev	7.522

# B1L102S, U21-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

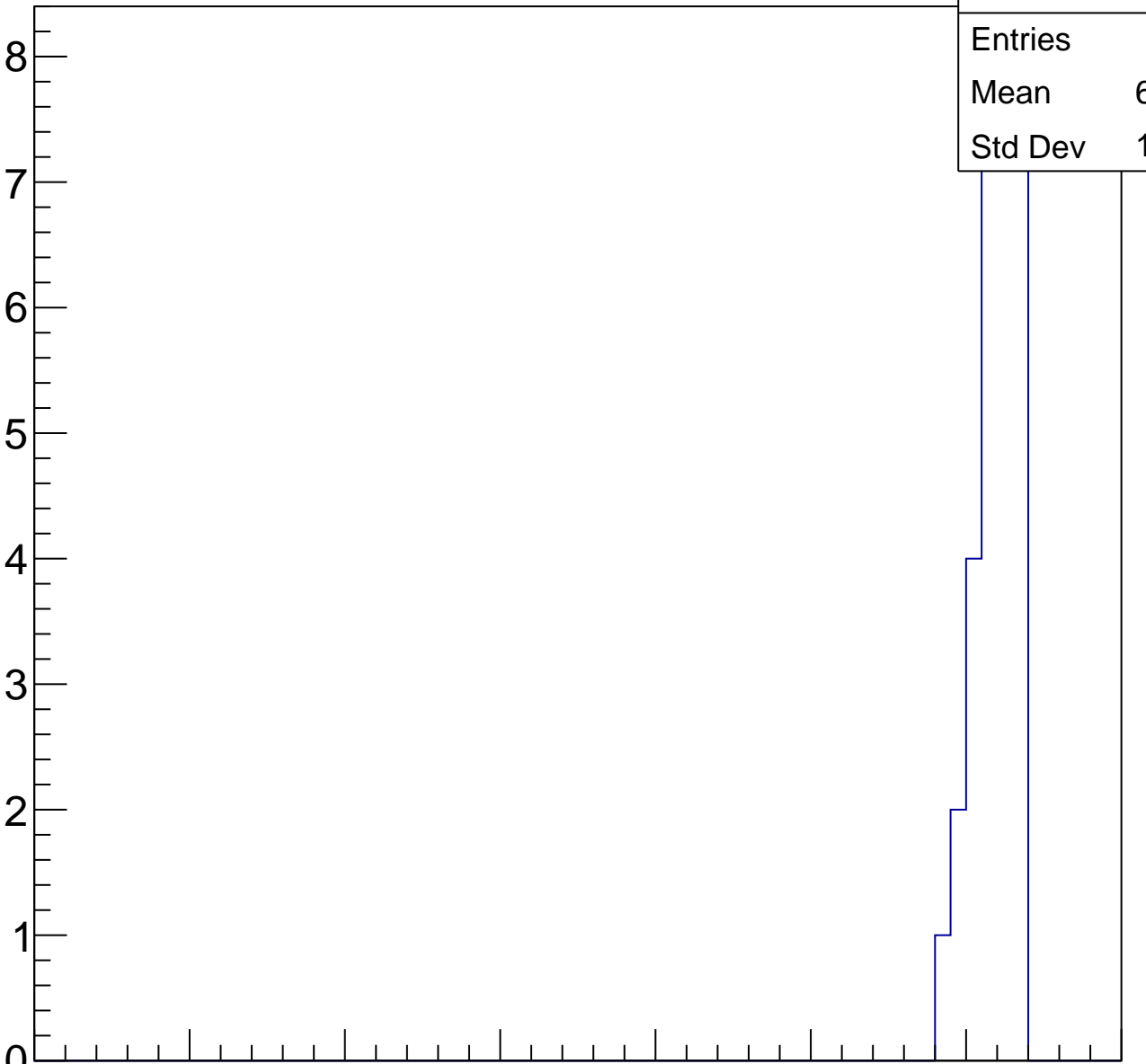
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	31
Mean	61.42
Std Dev	1.339

ampl

0 10 20 30 40 50 60 70



# B1L102S, U21-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch74, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	74
Mean	29.18
Std Dev	5.767

**Gaus mean : 30.1580**

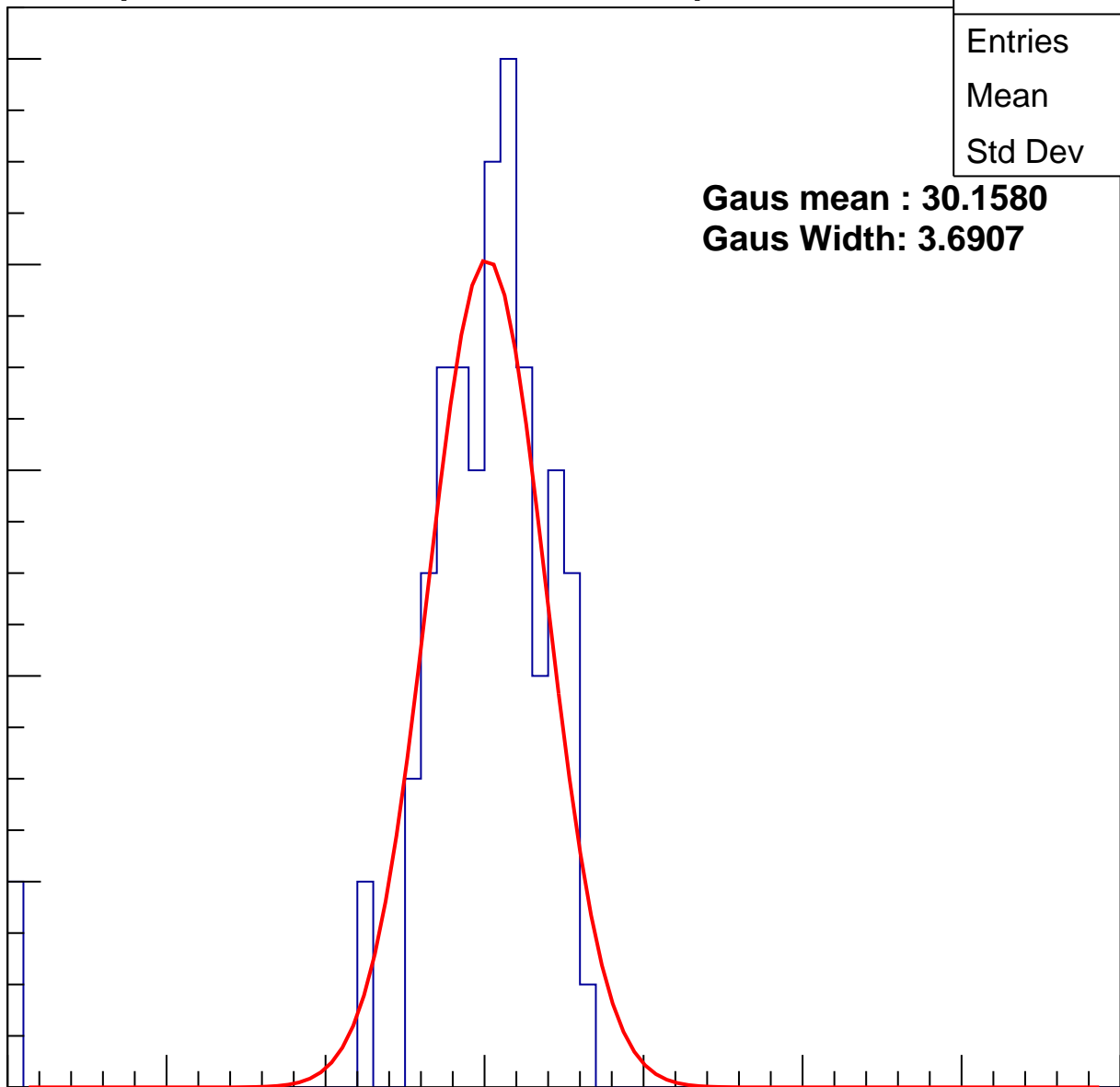
**Gaus Width: 3.6907**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U21-ch74, adc1

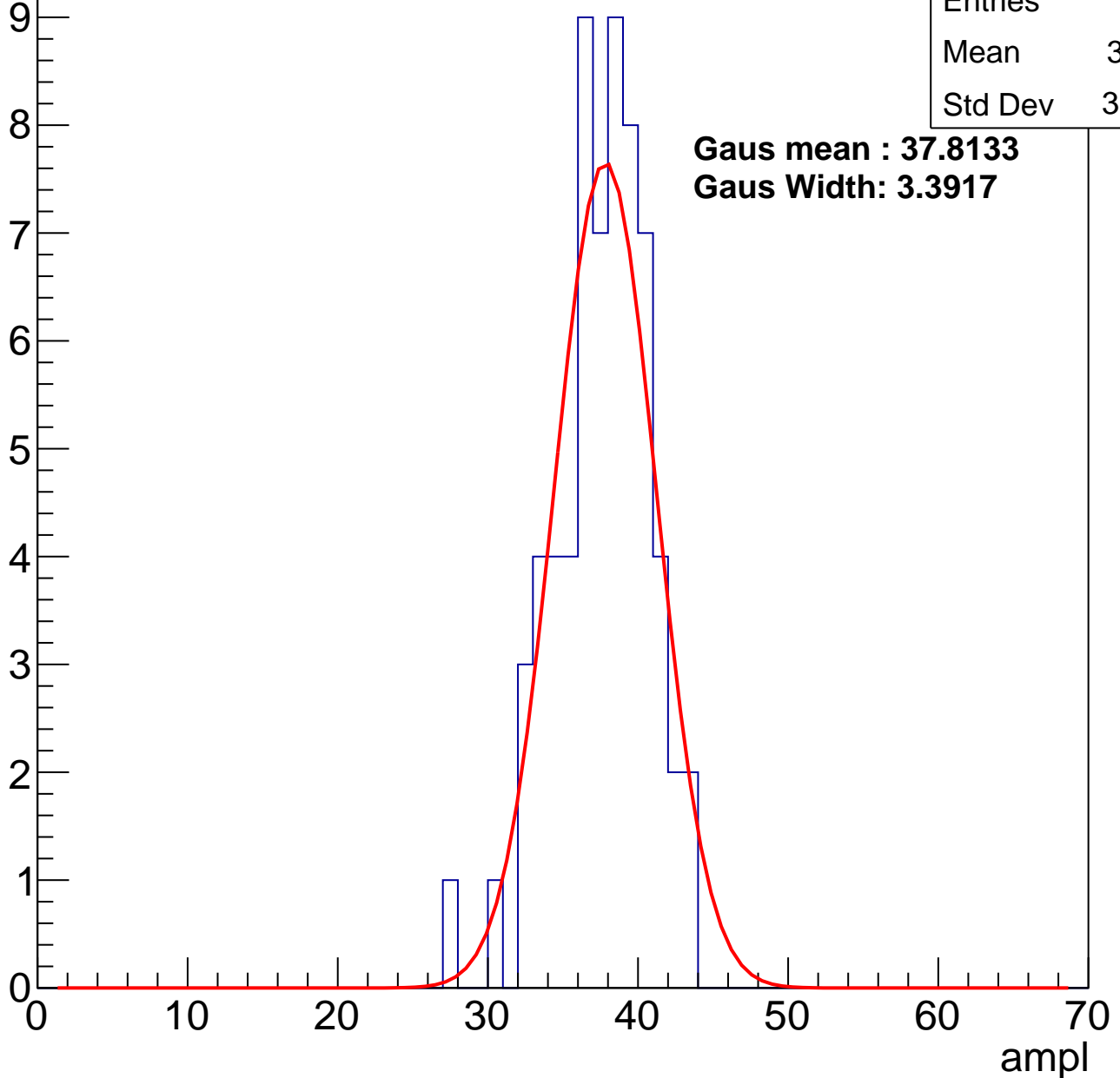
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	37.11
Std Dev	3.134

**Gaus mean : 37.8133**

**Gaus Width: 3.3917**



# B1L102S, U21-ch74, adc2

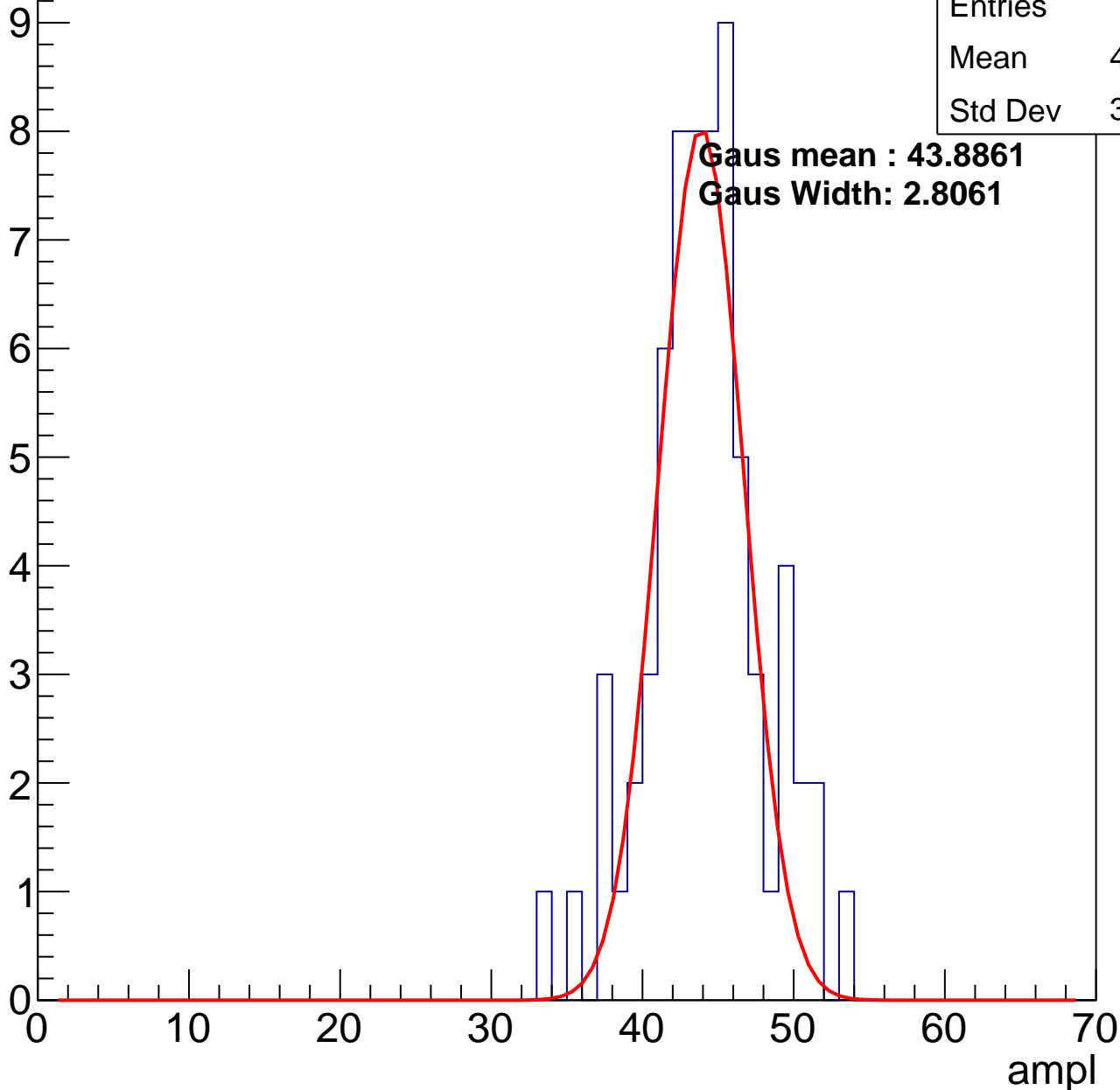
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	43.65
Std Dev	3.819

**Gaus mean : 43.8861**

**Gaus Width: 2.8061**

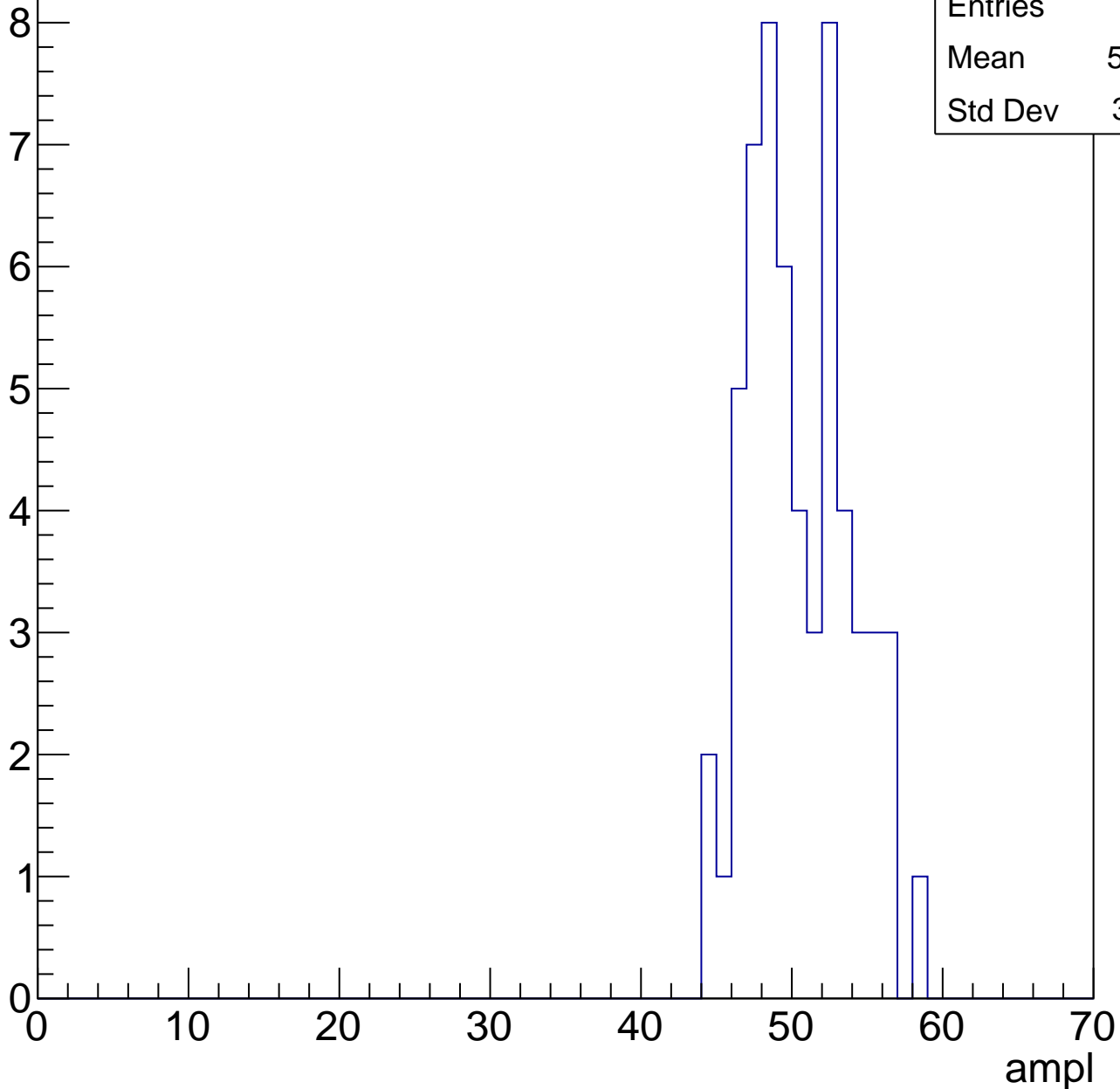


# B1L102S, U21-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	50.07
Std Dev	3.331

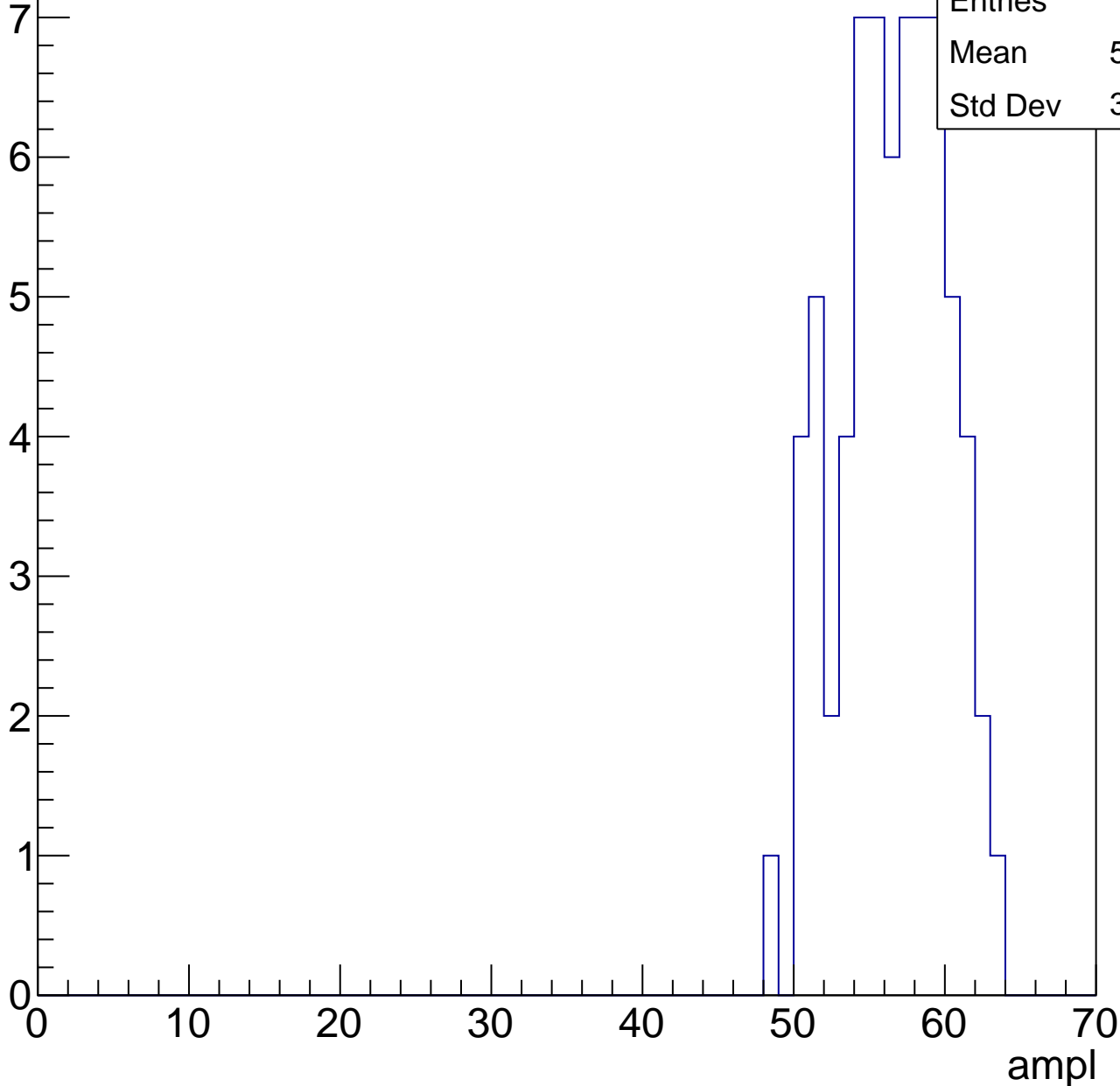


# B1L102S, U21-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	56.04
Std Dev	3.478

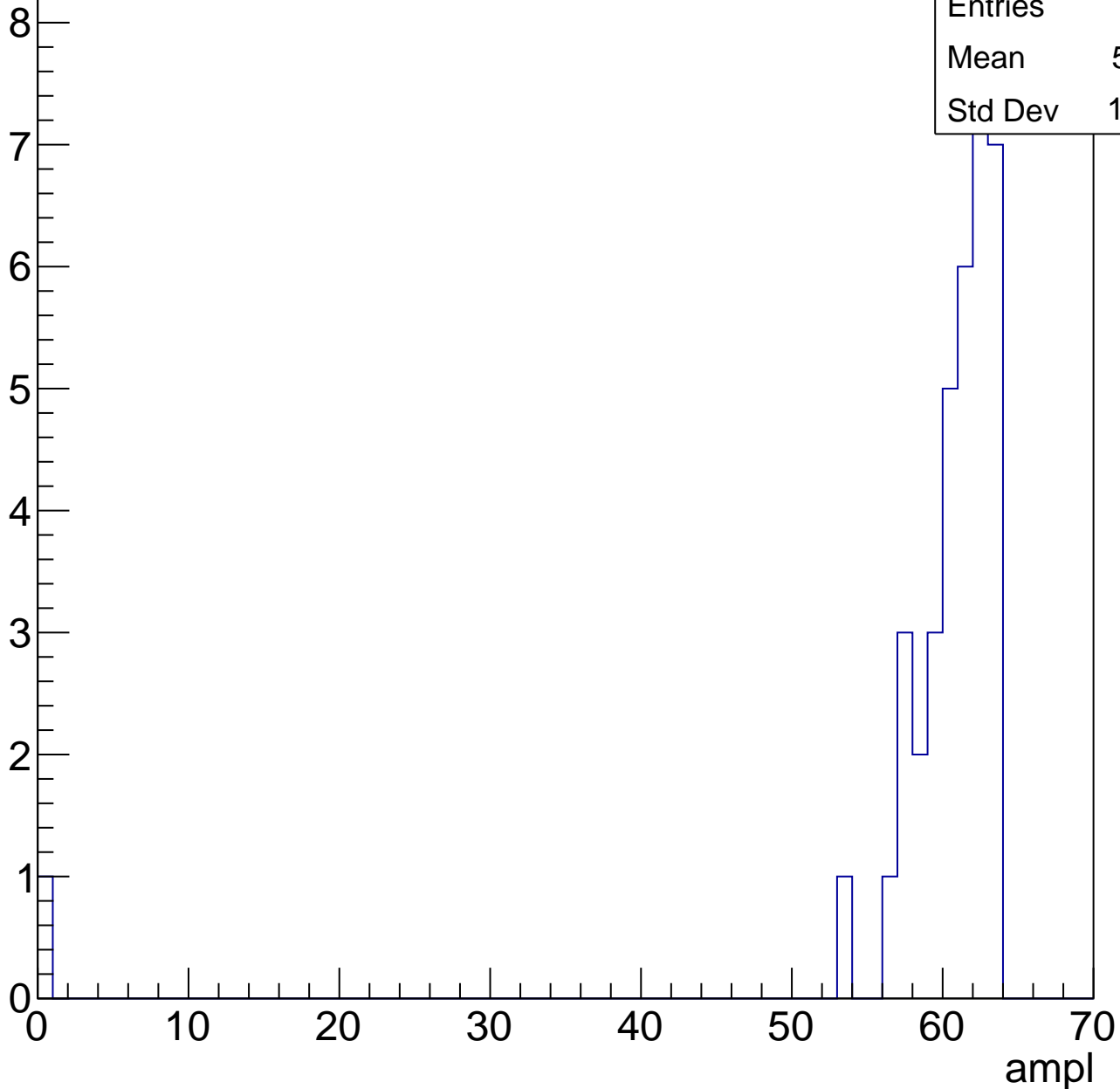


# B1L102S, U21-ch74, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	37
Mean	58.81
Std Dev	10.07



# B1L102S, U21-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U21-ch75, adc0

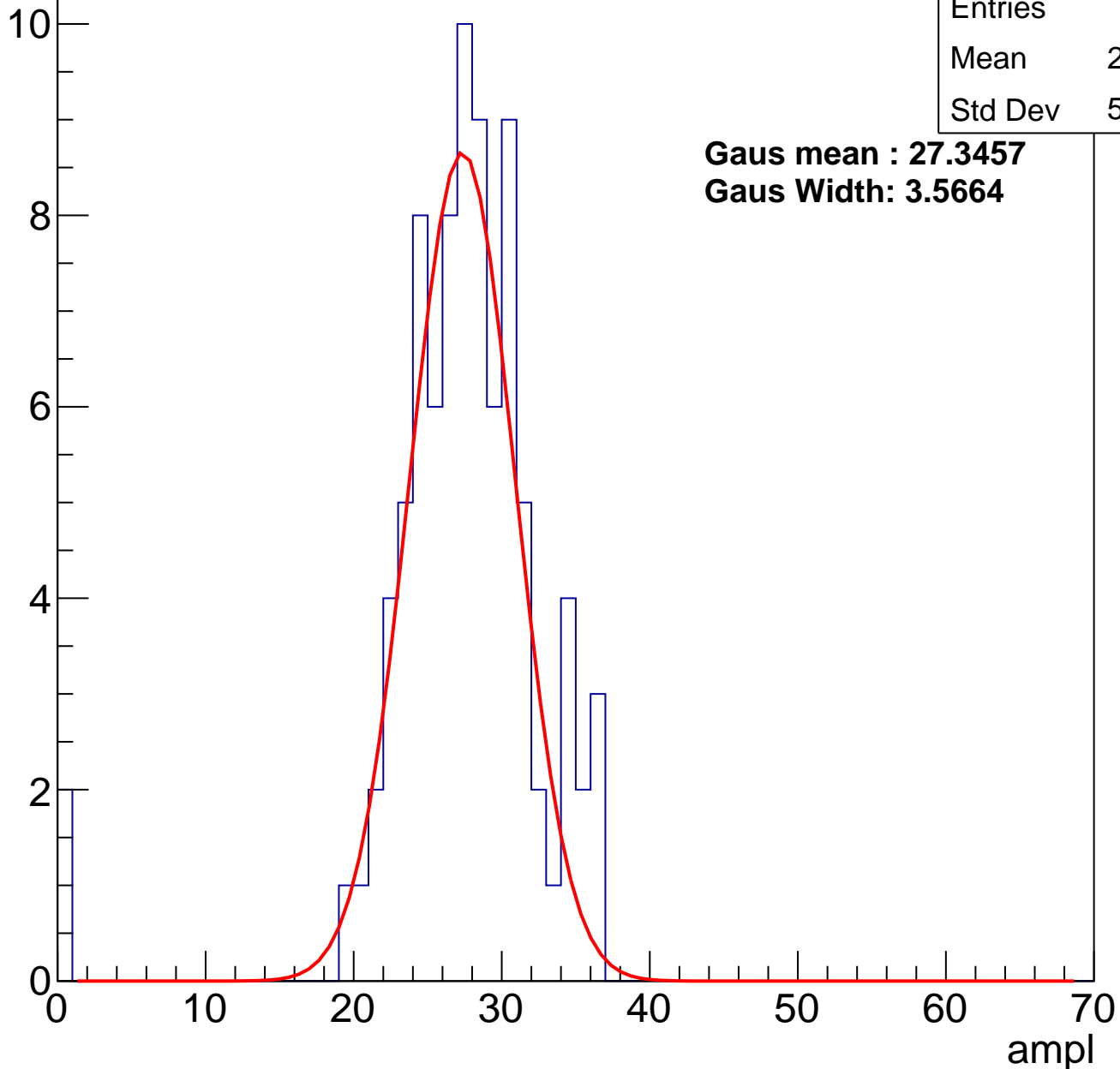
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	88
Mean	26.89
Std Dev	5.613

**Gaus mean : 27.3457**

**Gaus Width: 3.5664**

Entry



# B1L102S, U21-ch75, adc1

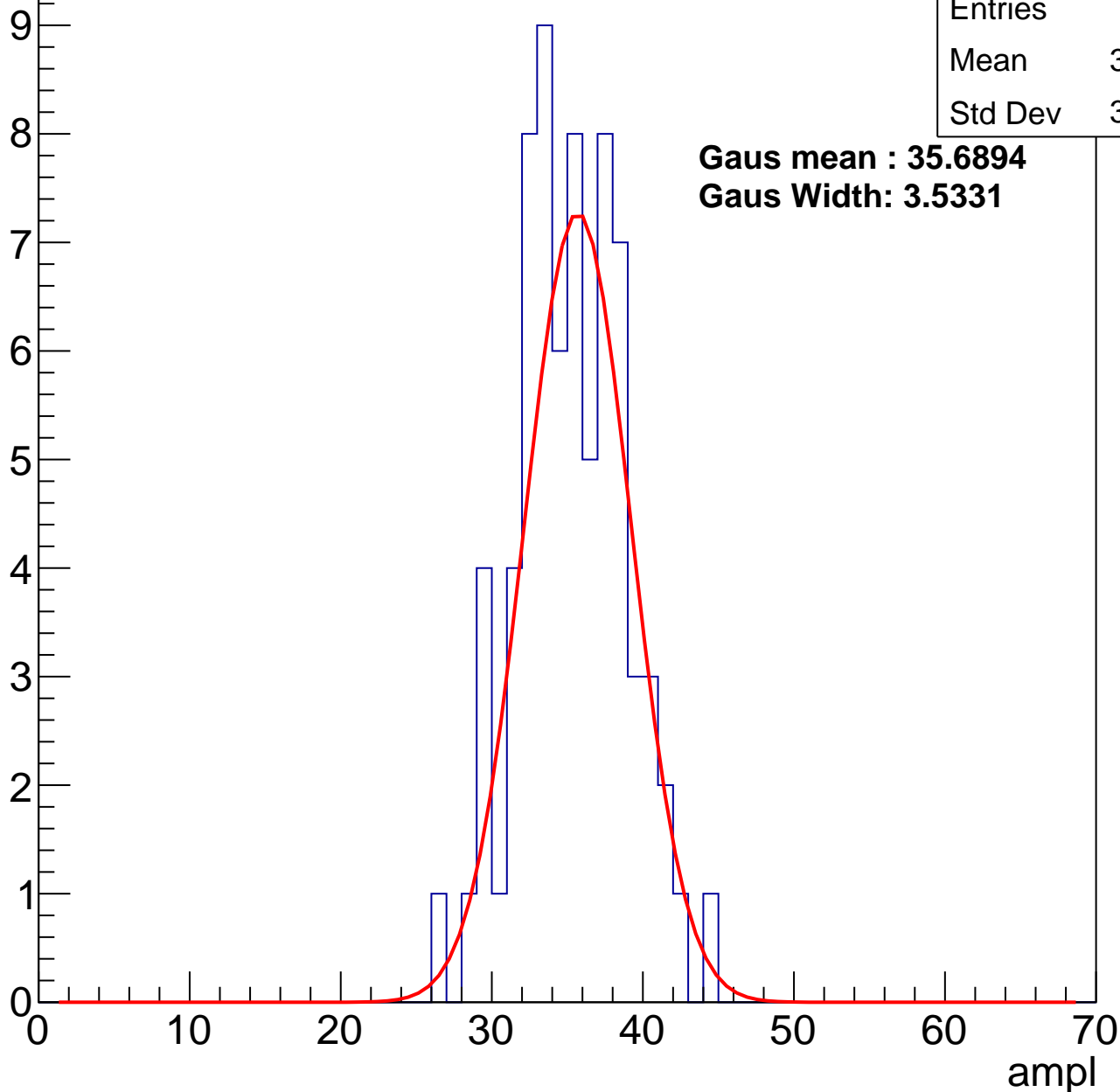
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	34.83
Std Dev	3.536

**Gaus mean : 35.6894**

**Gaus Width: 3.5331**



# B1L102S, U21-ch75, adc2

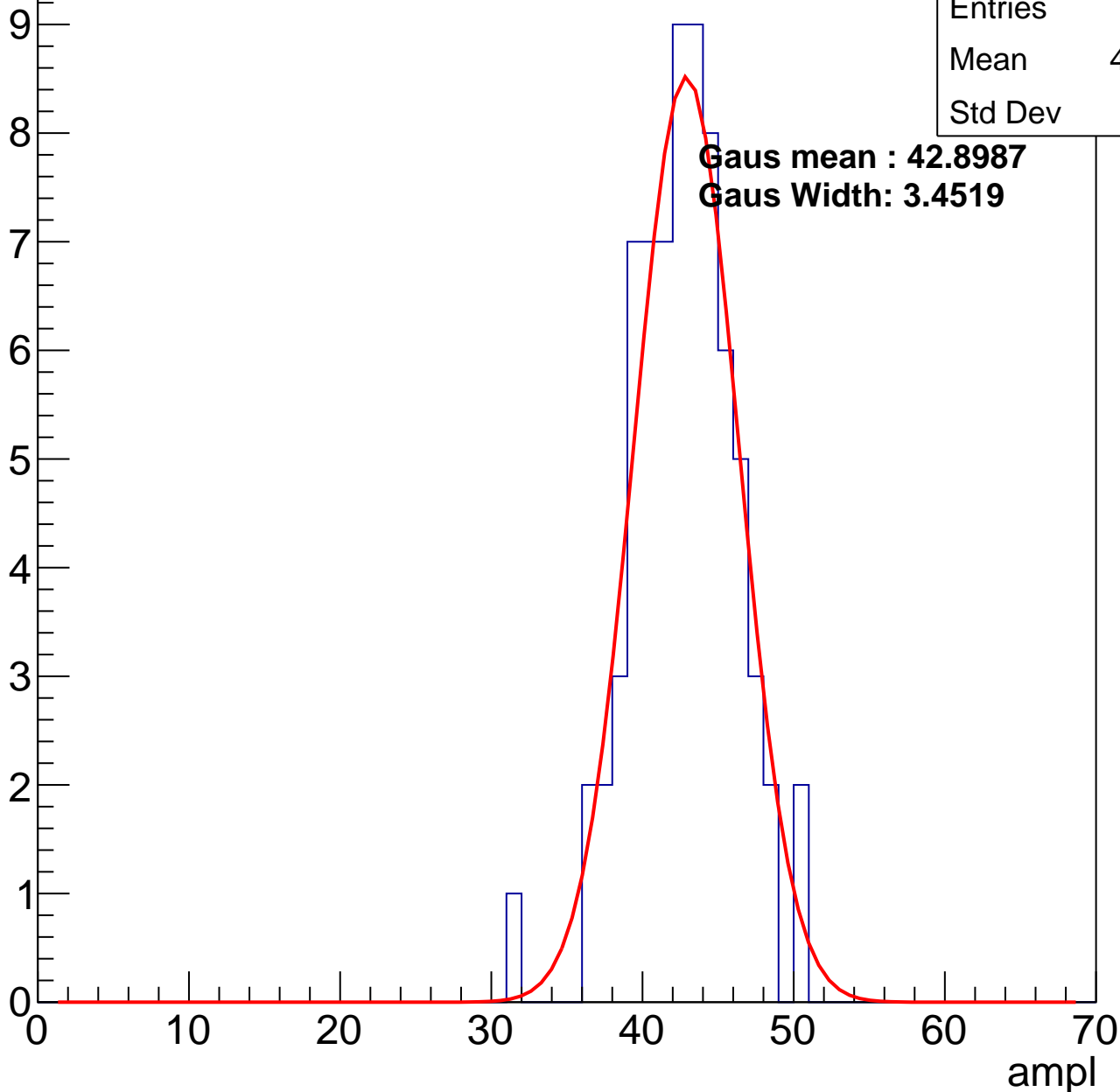
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	42.26
Std Dev	3.38

**Gaus mean : 42.8987**

**Gaus Width: 3.4519**

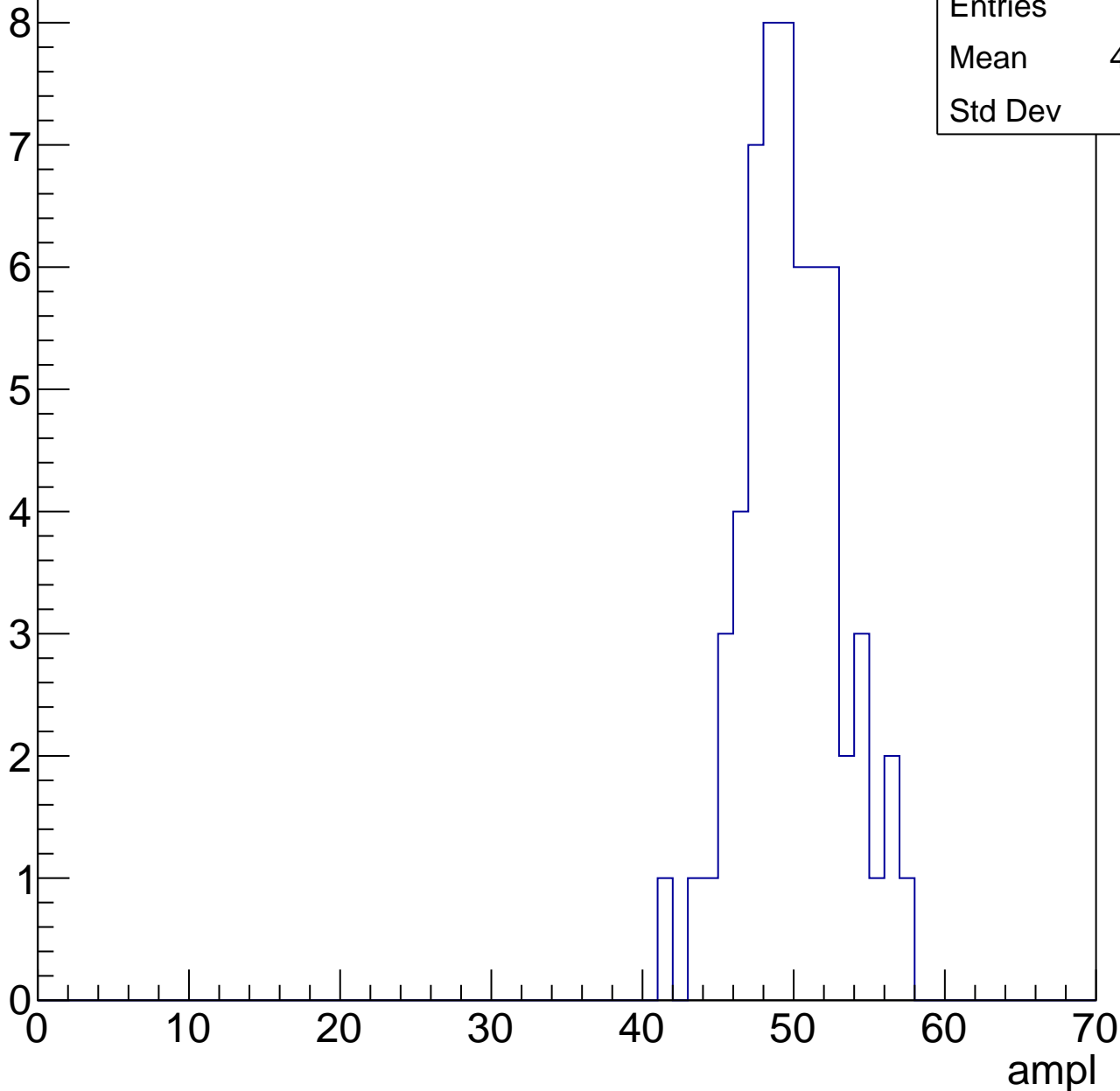


# B1L102S, U21-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	49.37
Std Dev	3.23

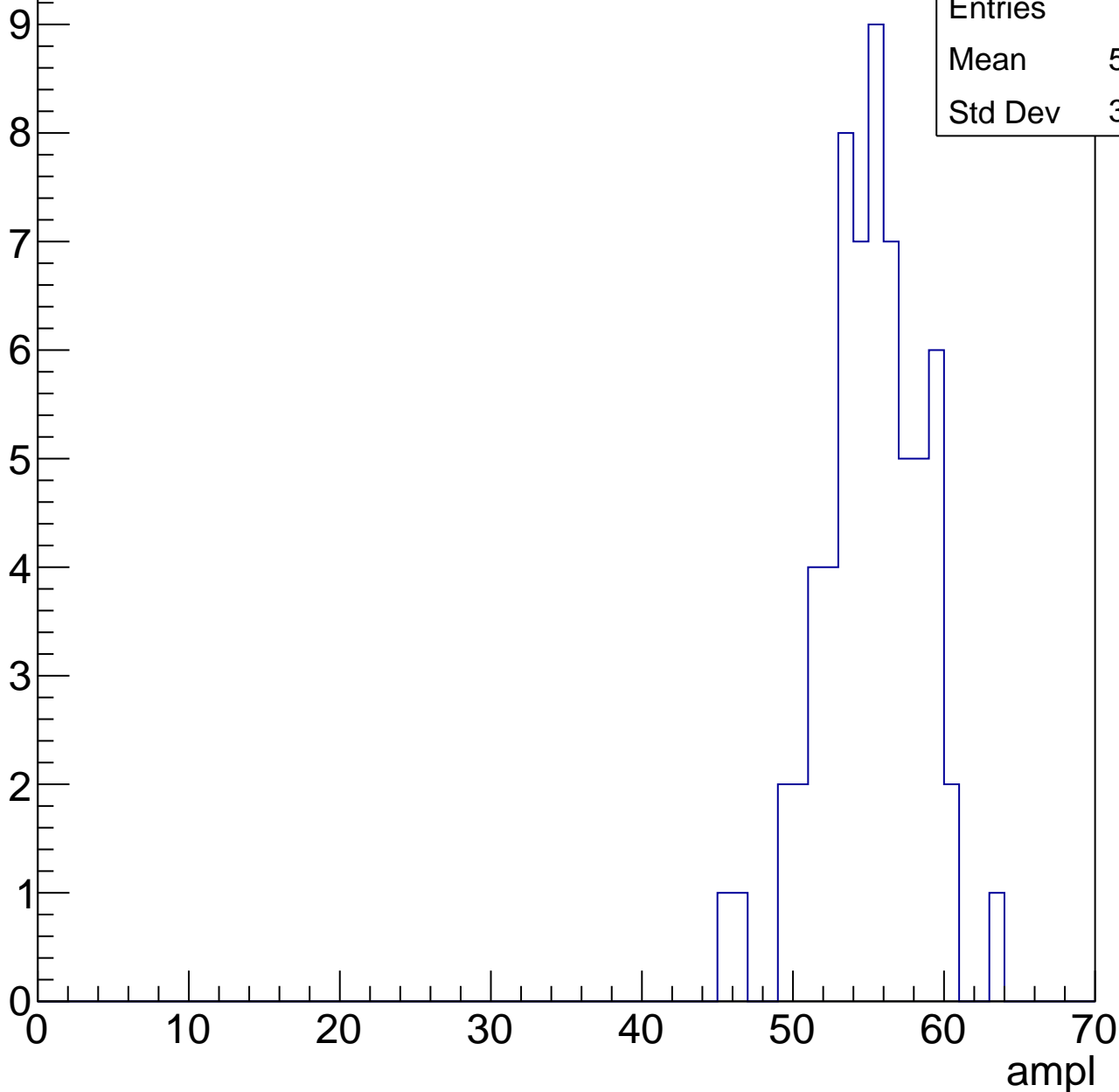


# B1L102S, U21-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	54.72
Std Dev	3.352

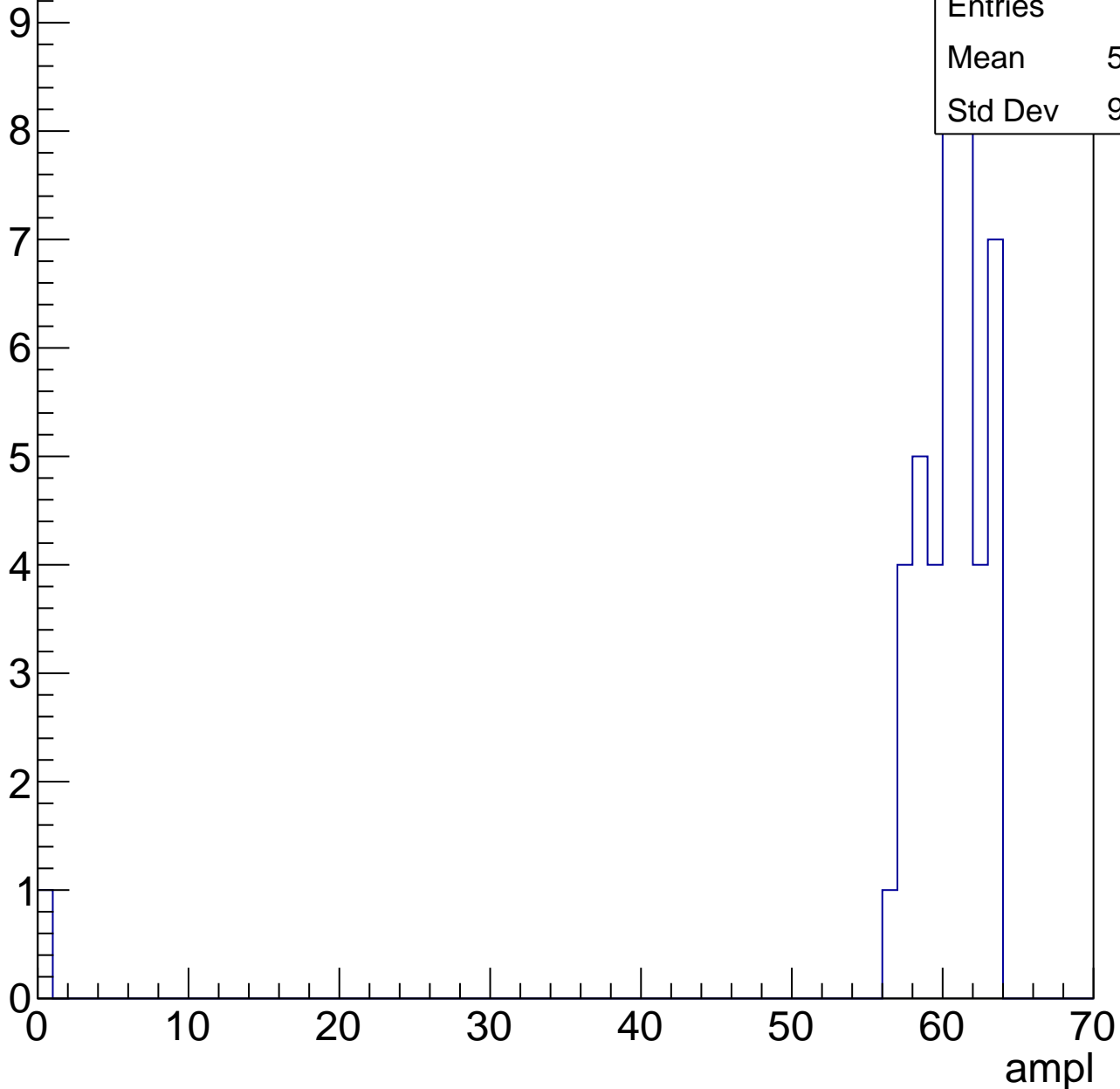


# B1L102S, U21-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	43
Mean	58.79
Std Dev	9.278

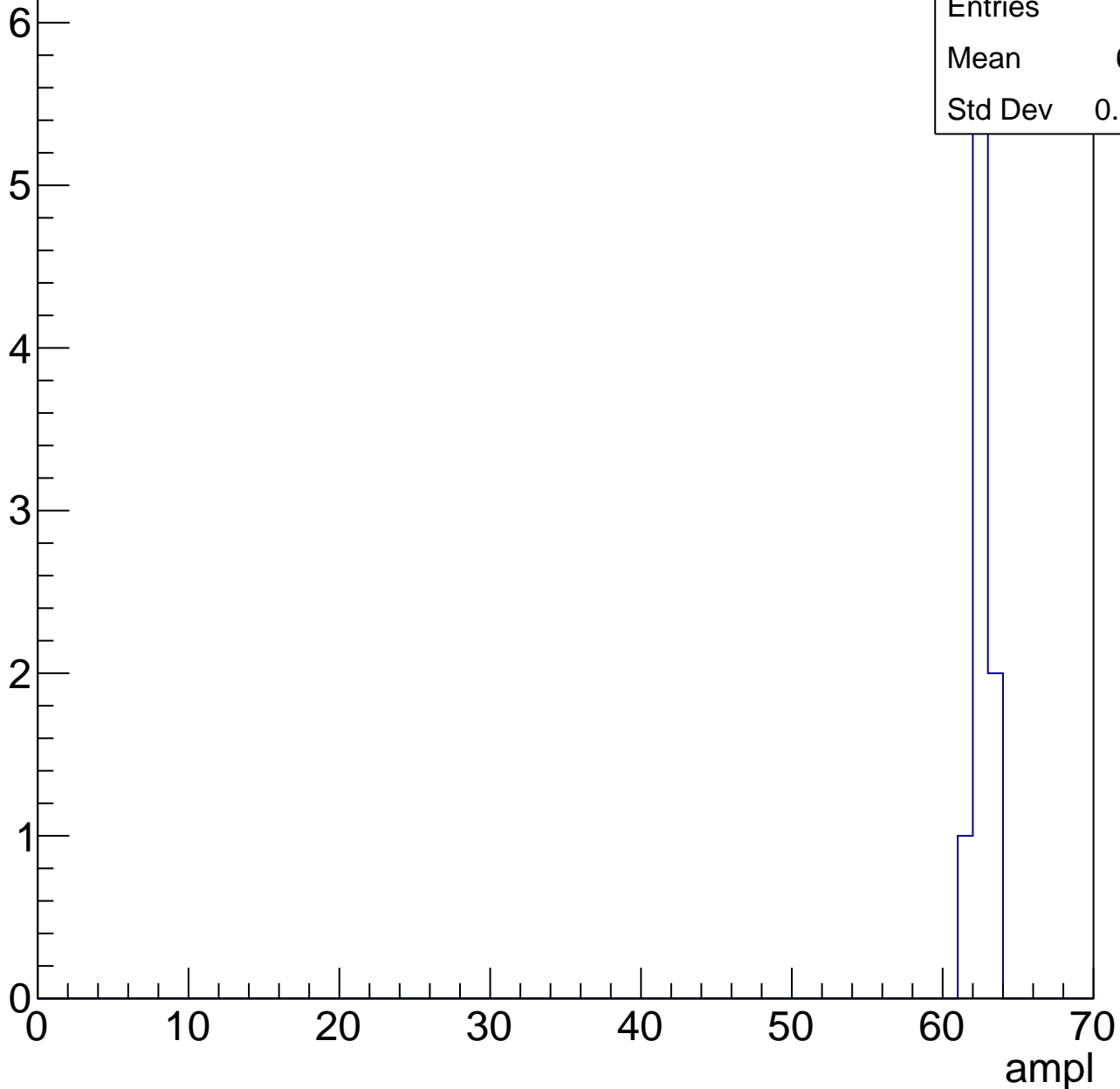


# B1L102S, U21-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	9
Mean	62.11
Std Dev	0.5666





# B1L102S, U21-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch76, adc0

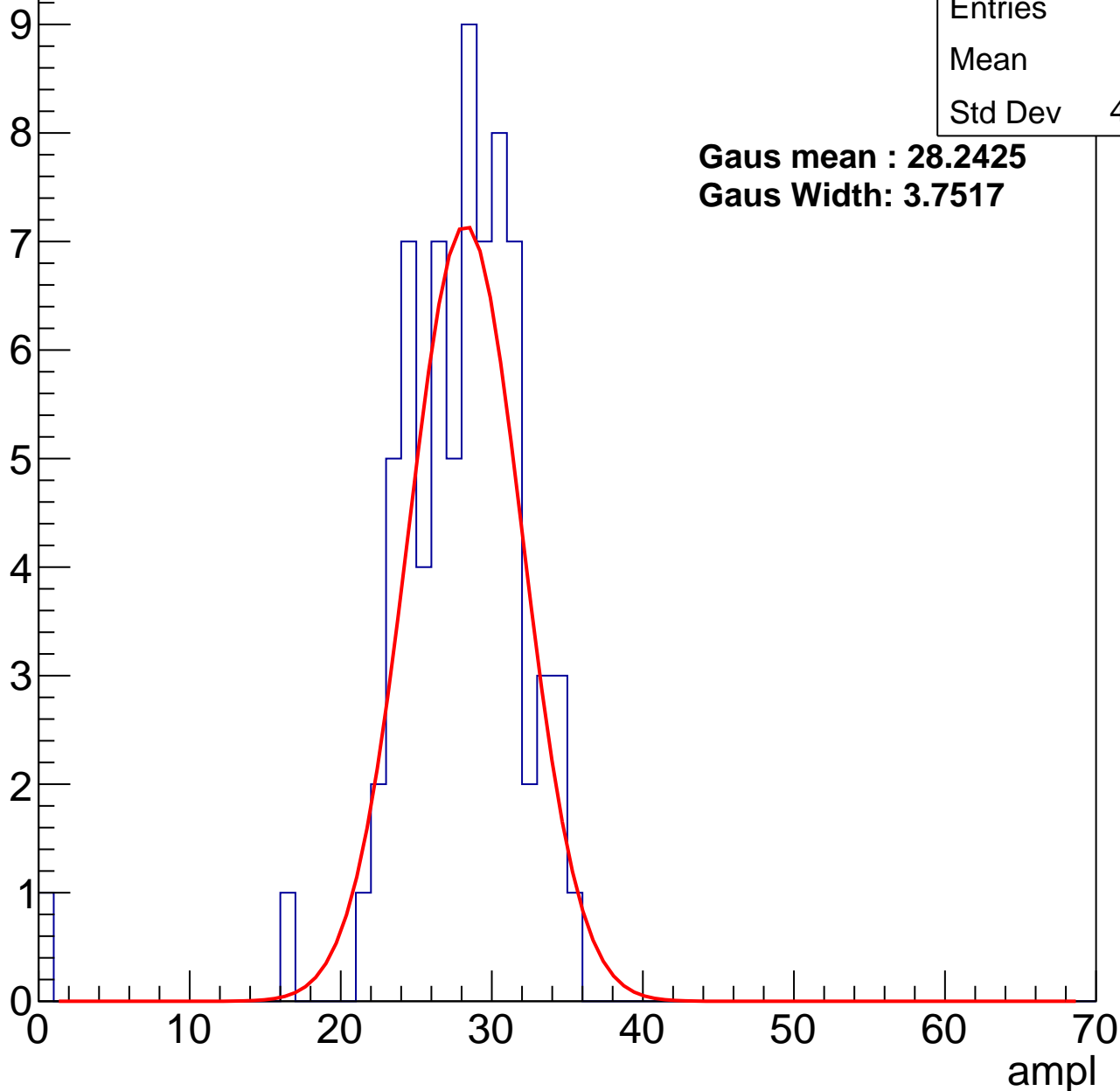
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	27.3
Std Dev	4.805

**Gaus mean : 28.2425**

**Gaus Width: 3.7517**



# B1L102S, U21-ch76, adc1

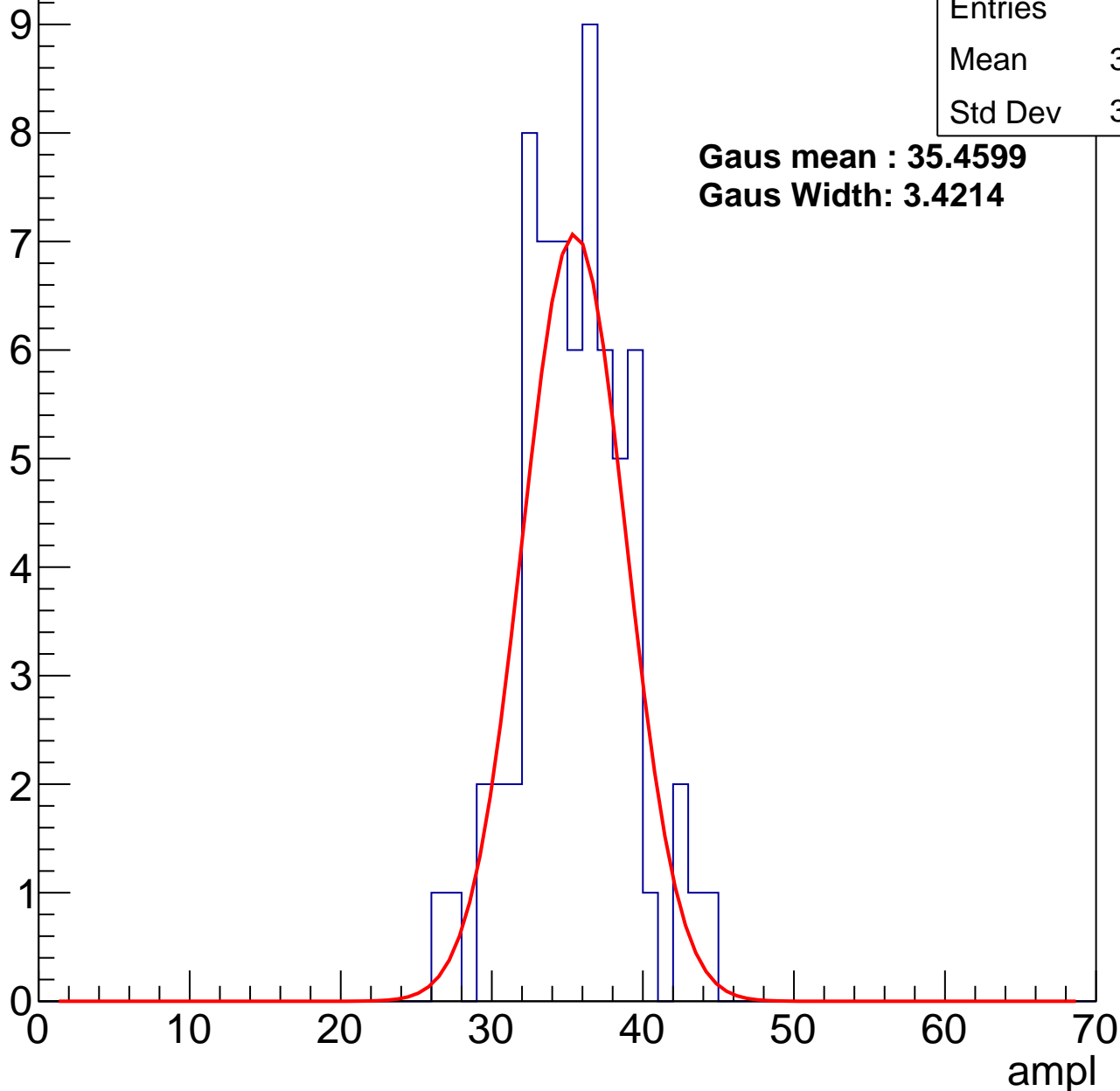
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	35.06
Std Dev	3.557

**Gaus mean : 35.4599**

**Gaus Width: 3.4214**



# B1L102S, U21-ch76, adc2

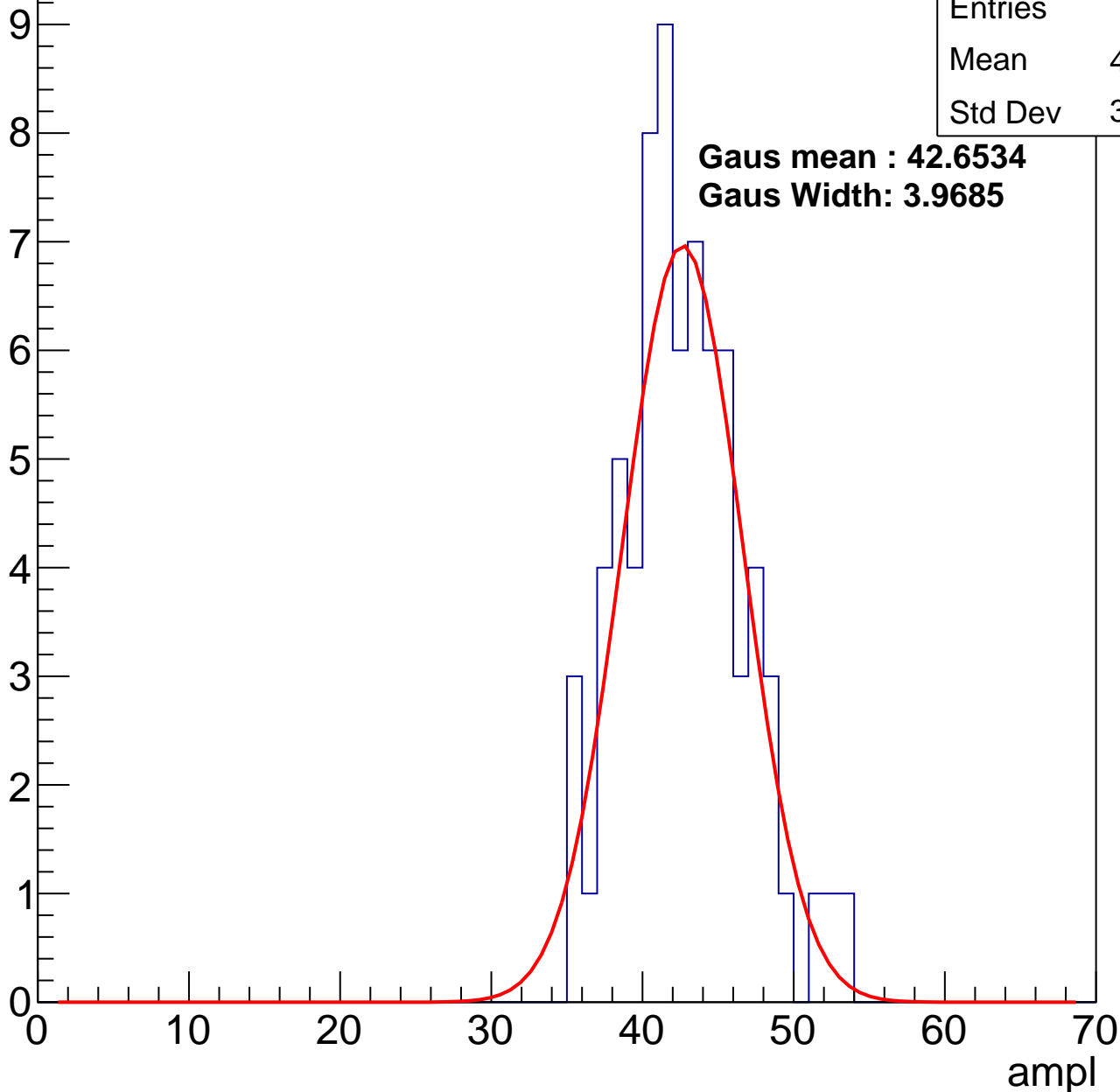
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	42.27
Std Dev	3.928

**Gaus mean : 42.6534**

**Gaus Width: 3.9685**

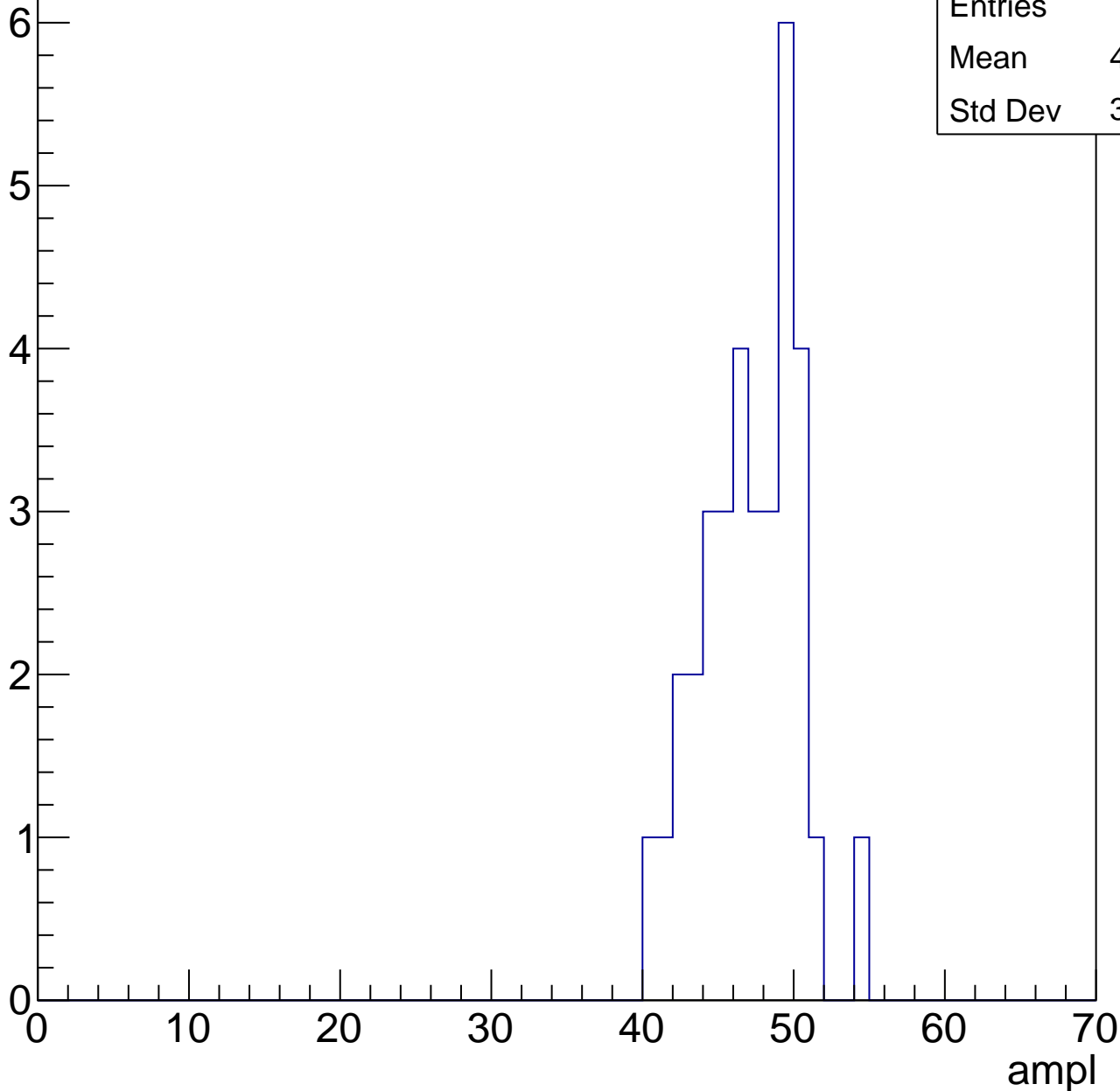


# B1L102S, U21-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	34
Mean	46.65
Std Dev	3.133

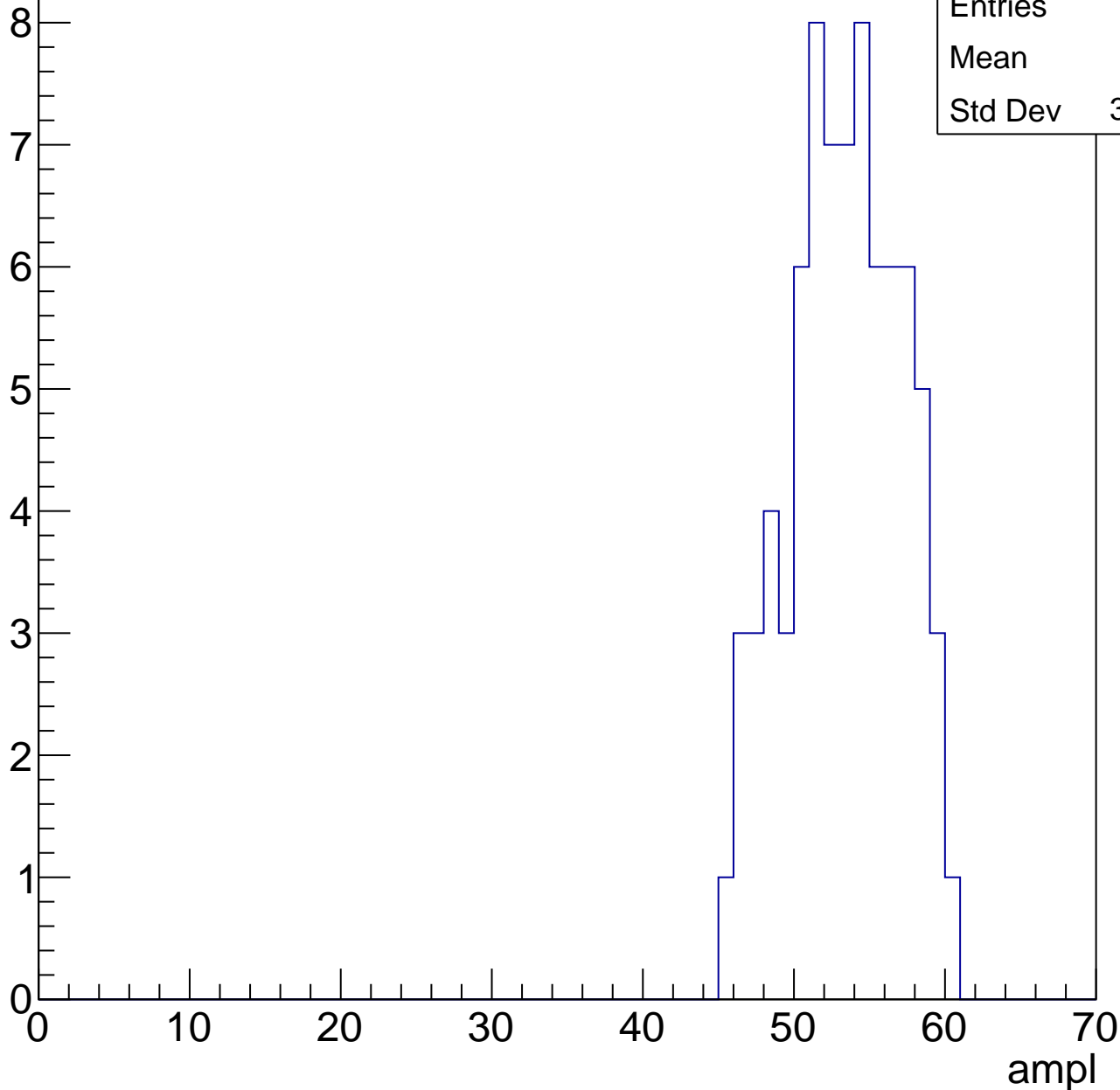


# B1L102S, U21-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

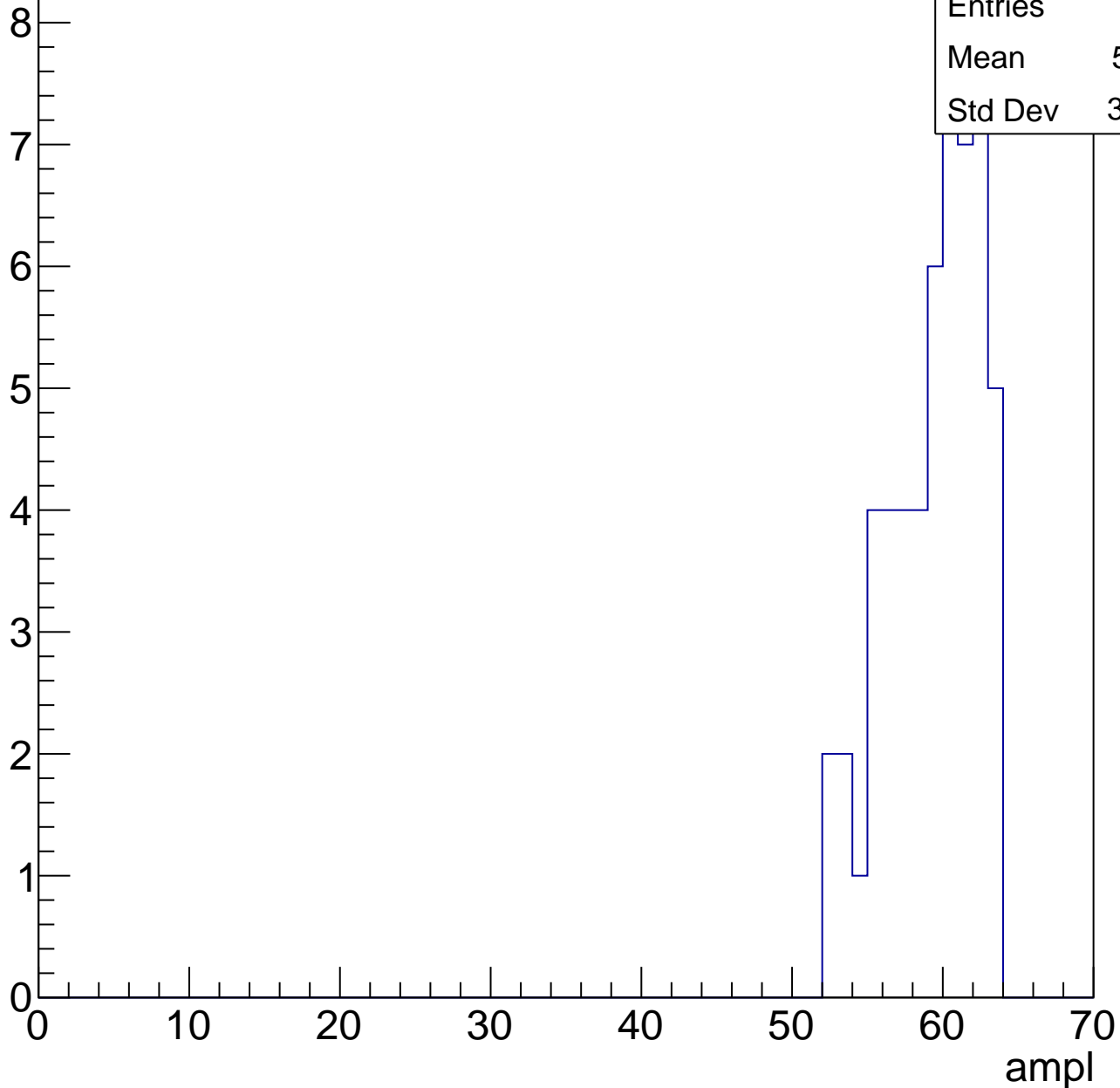
Entries	77
Mean	52.9
Std Dev	3.645



# B1L102S, U21-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3

2.5

2

1.5

1

0.5

0

ampl

Entries	12
Mean	56.08
Std Dev	16.98

0 10 20 30 40 50 60 70



# B1L102S, U21-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch77, adc0

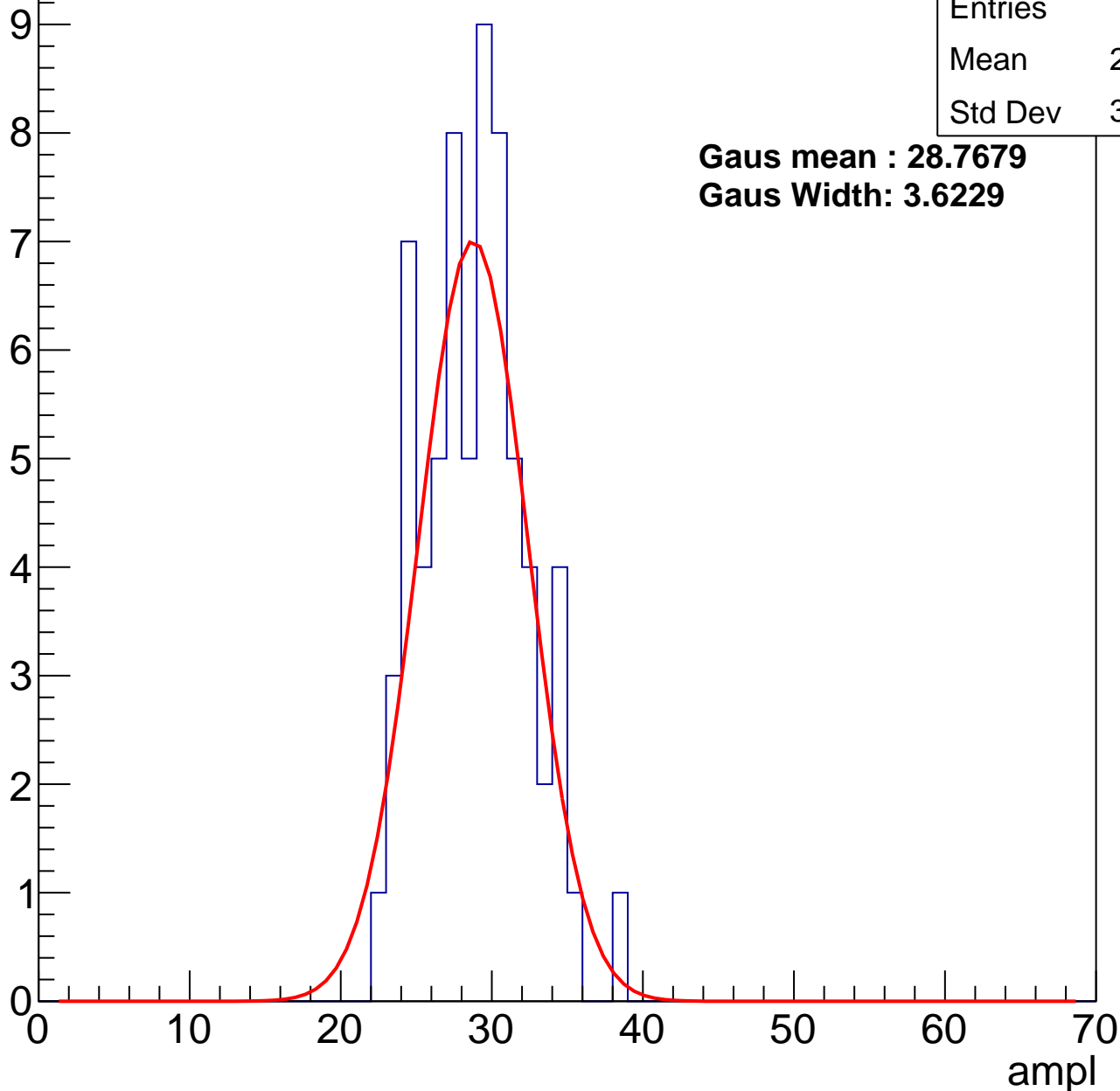
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	28.42
Std Dev	3.386

**Gaus mean : 28.7679**

**Gaus Width: 3.6229**



# B1L102S, U21-ch77, adc1

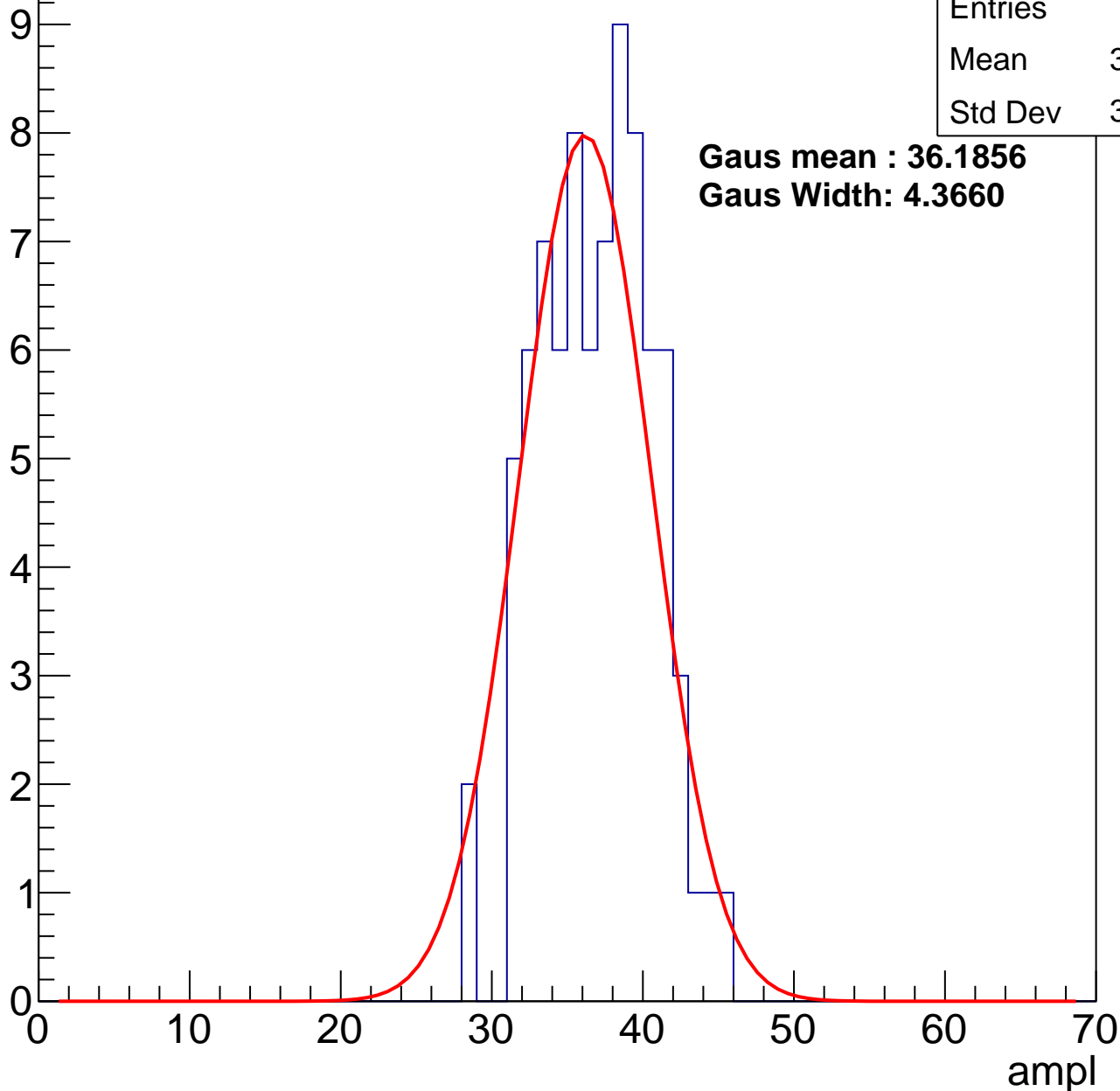
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	36.48
Std Dev	3.643

**Gaus mean : 36.1856**

**Gaus Width: 4.3660**



# B1L102S, U21-ch77, adc2

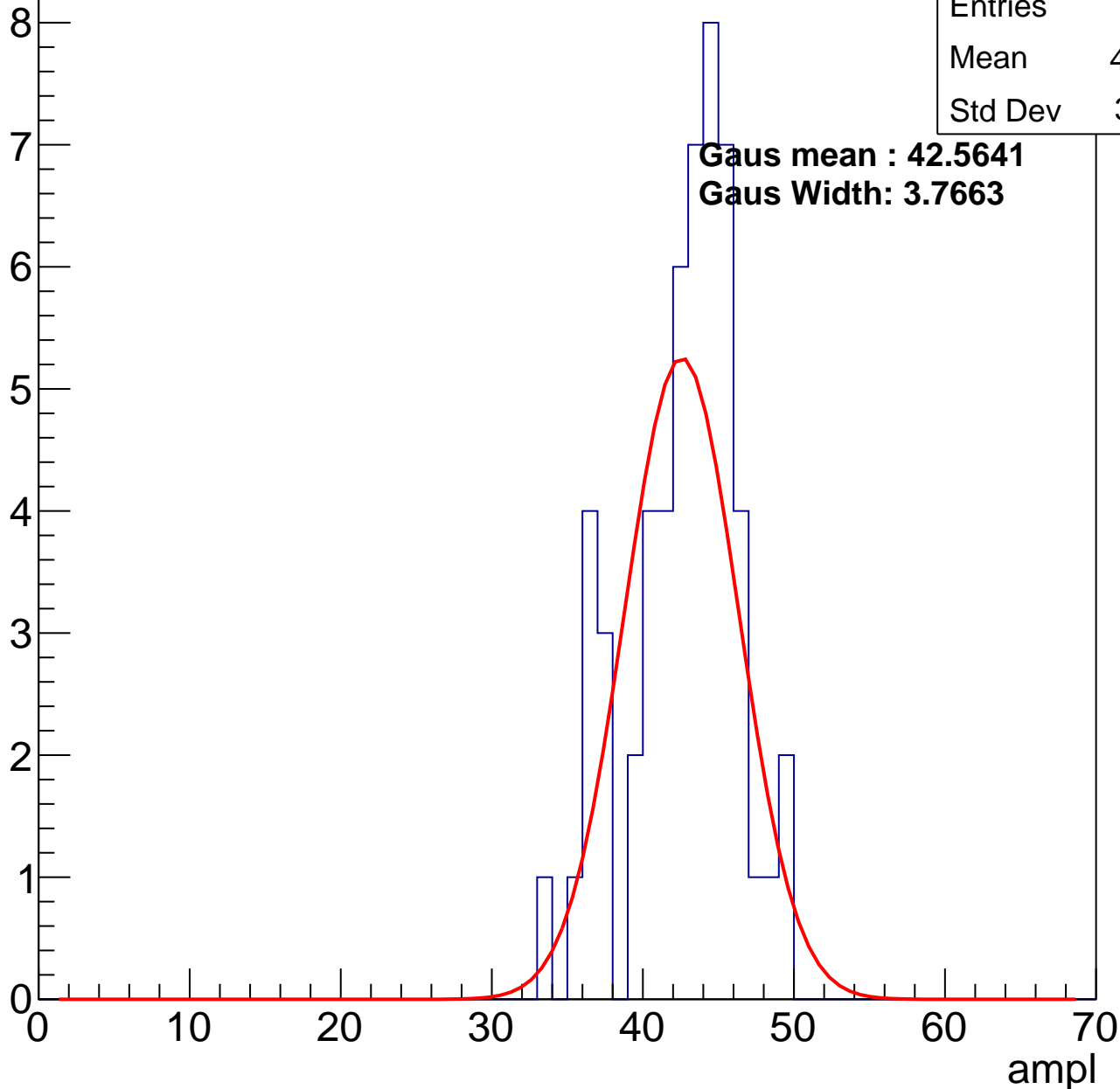
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	42.22
Std Dev	3.591

**Gaus mean : 42.5641**

**Gaus Width: 3.7663**

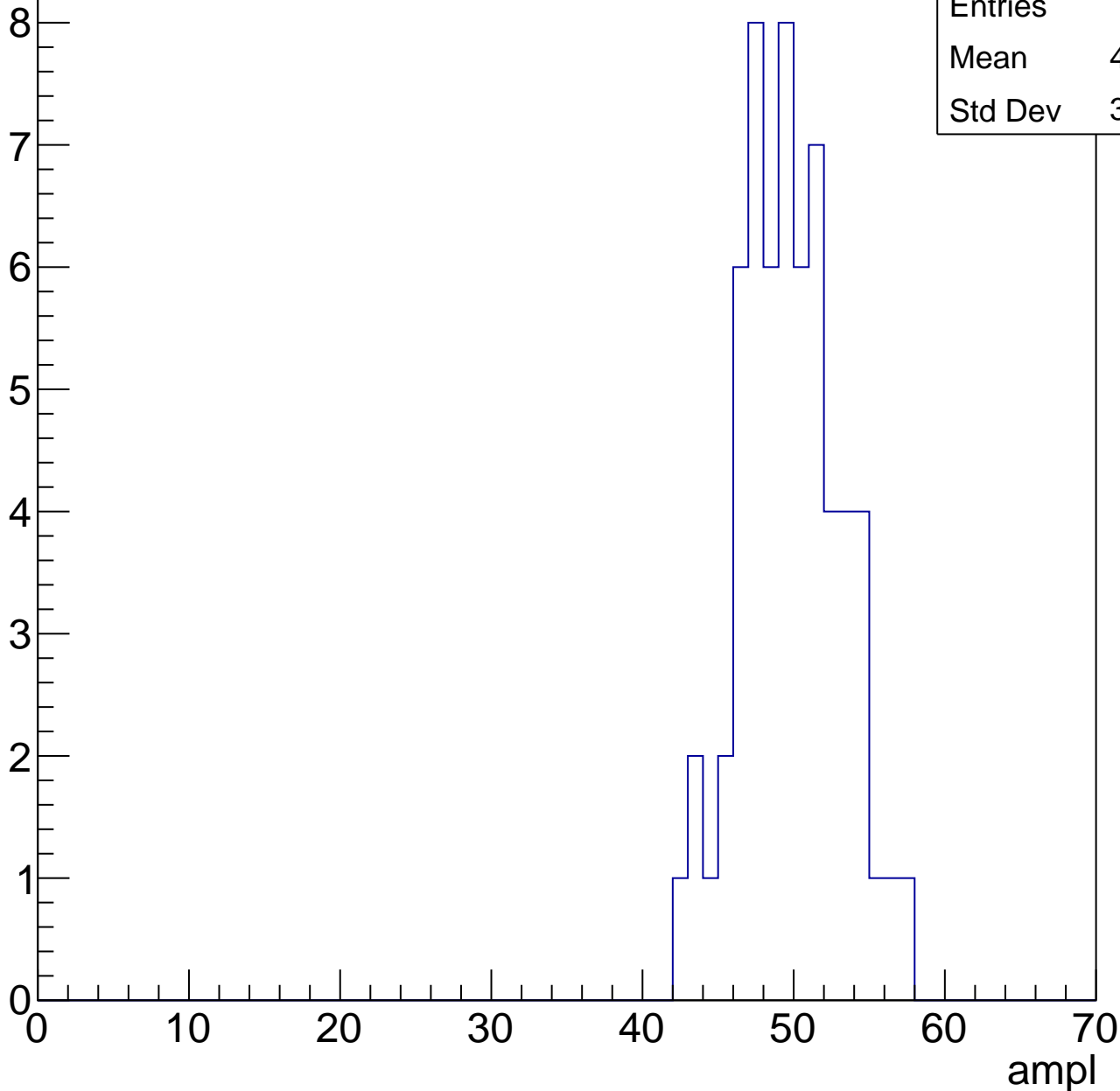


# B1L102S, U21-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	49.27
Std Dev	3.234

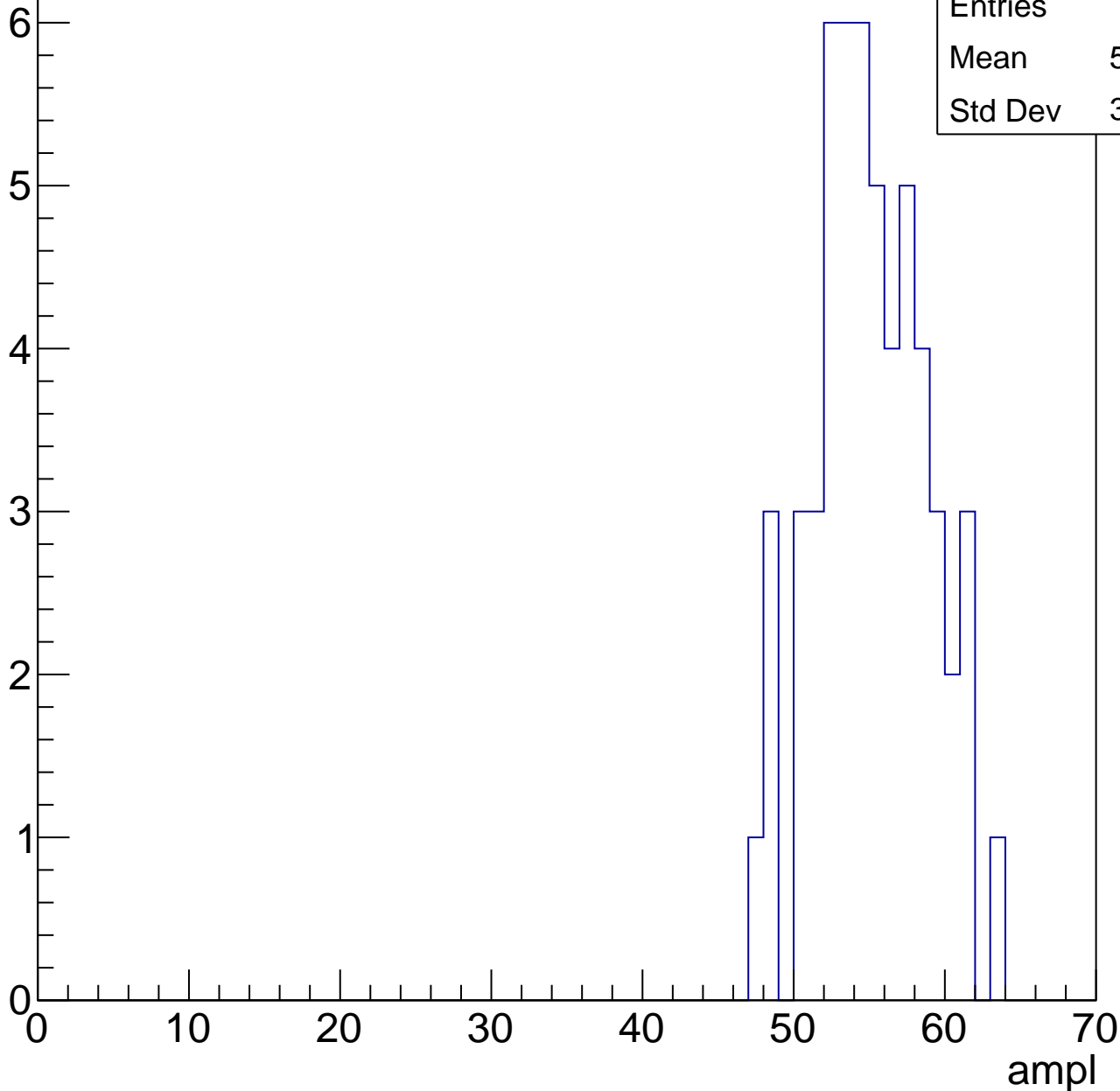


# B1L102S, U21-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	54.67
Std Dev	3.673

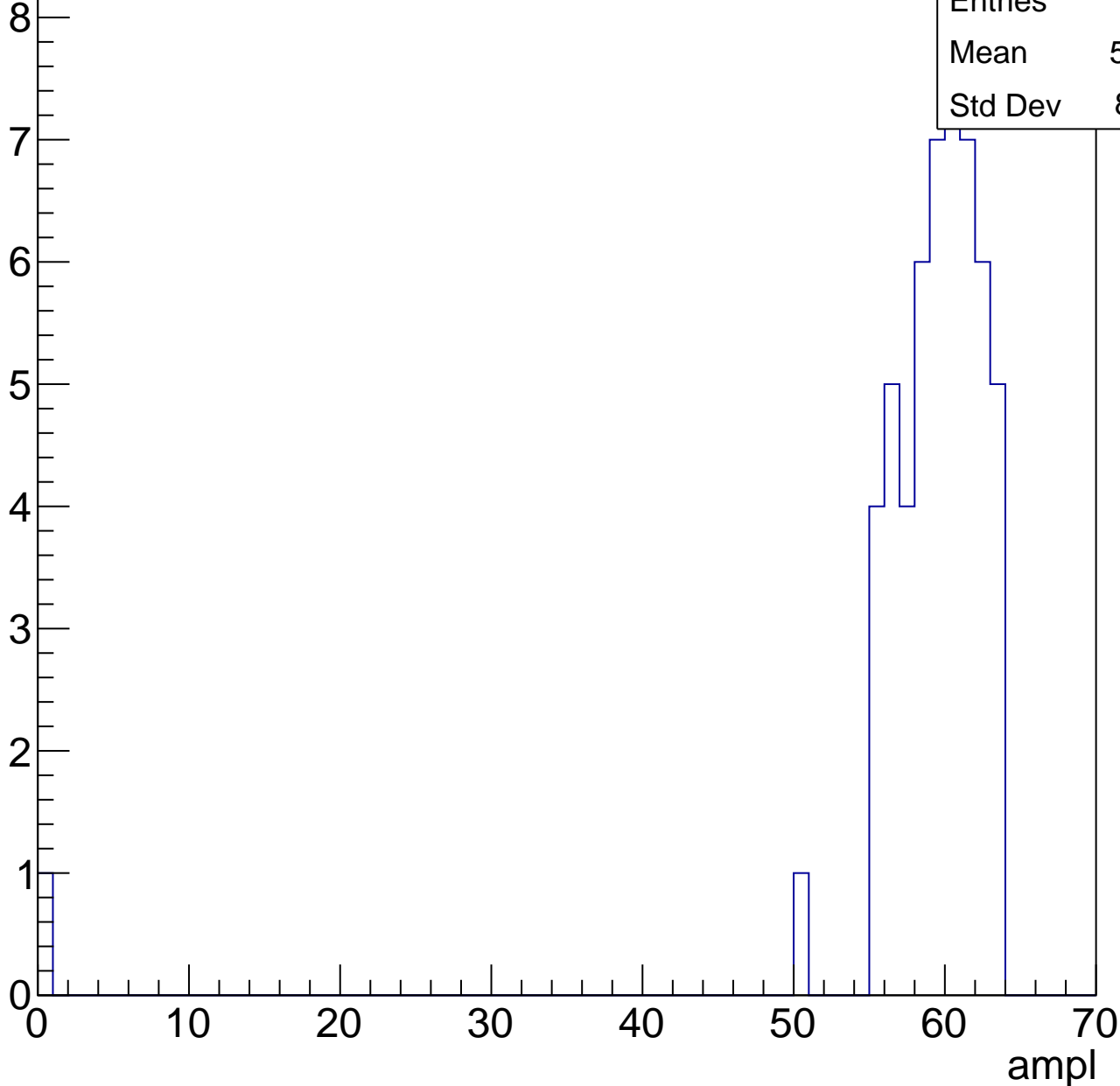


# B1L102S, U21-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

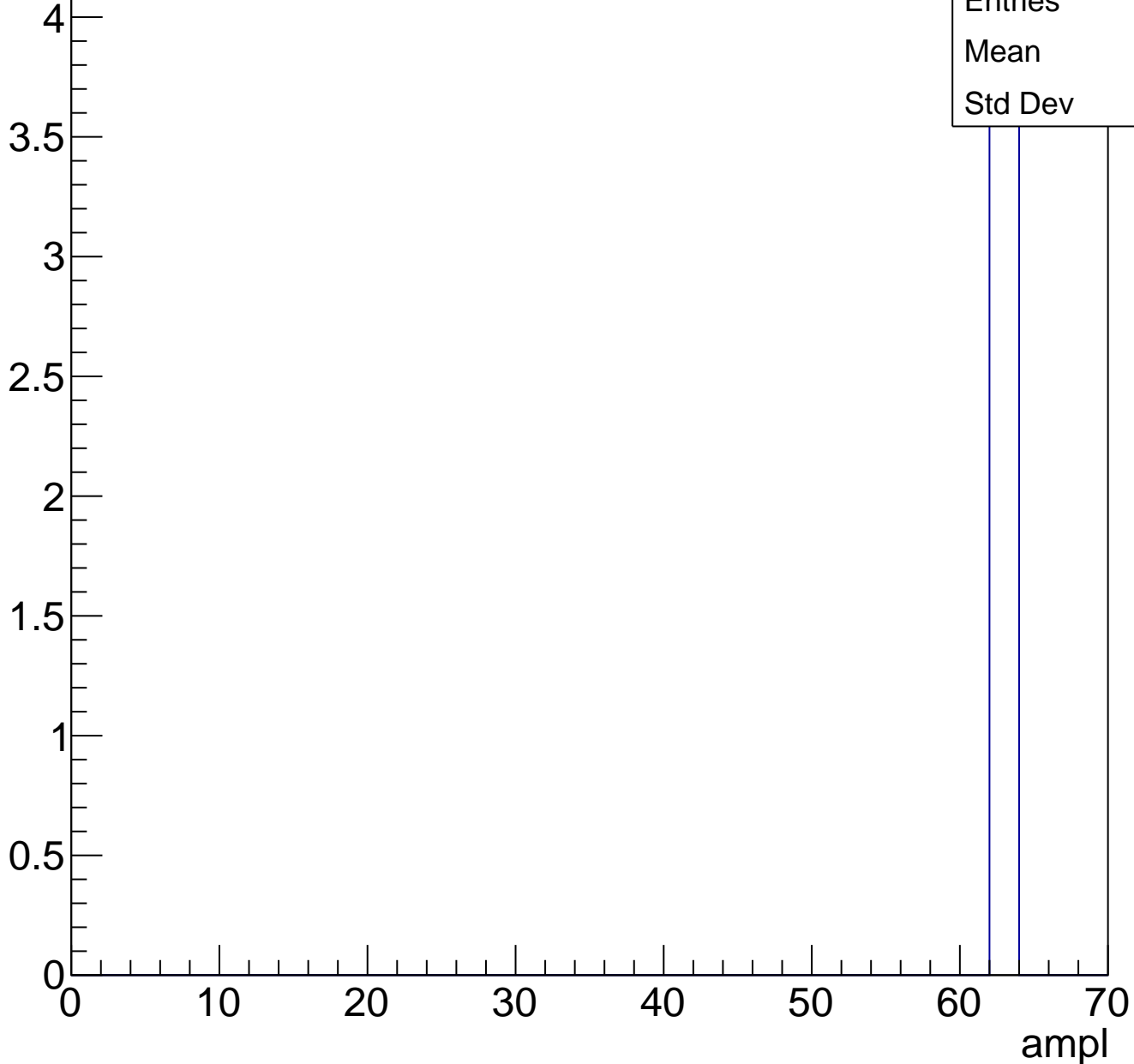
Entries	54
Mean	58.02
Std Dev	8.401



# B1L102S, U21-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	8
Mean	62.5
Std Dev	0.5



# B1L102S, U21-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	7
Std Dev	9.899

# B1L102S, U21-ch78, adc0

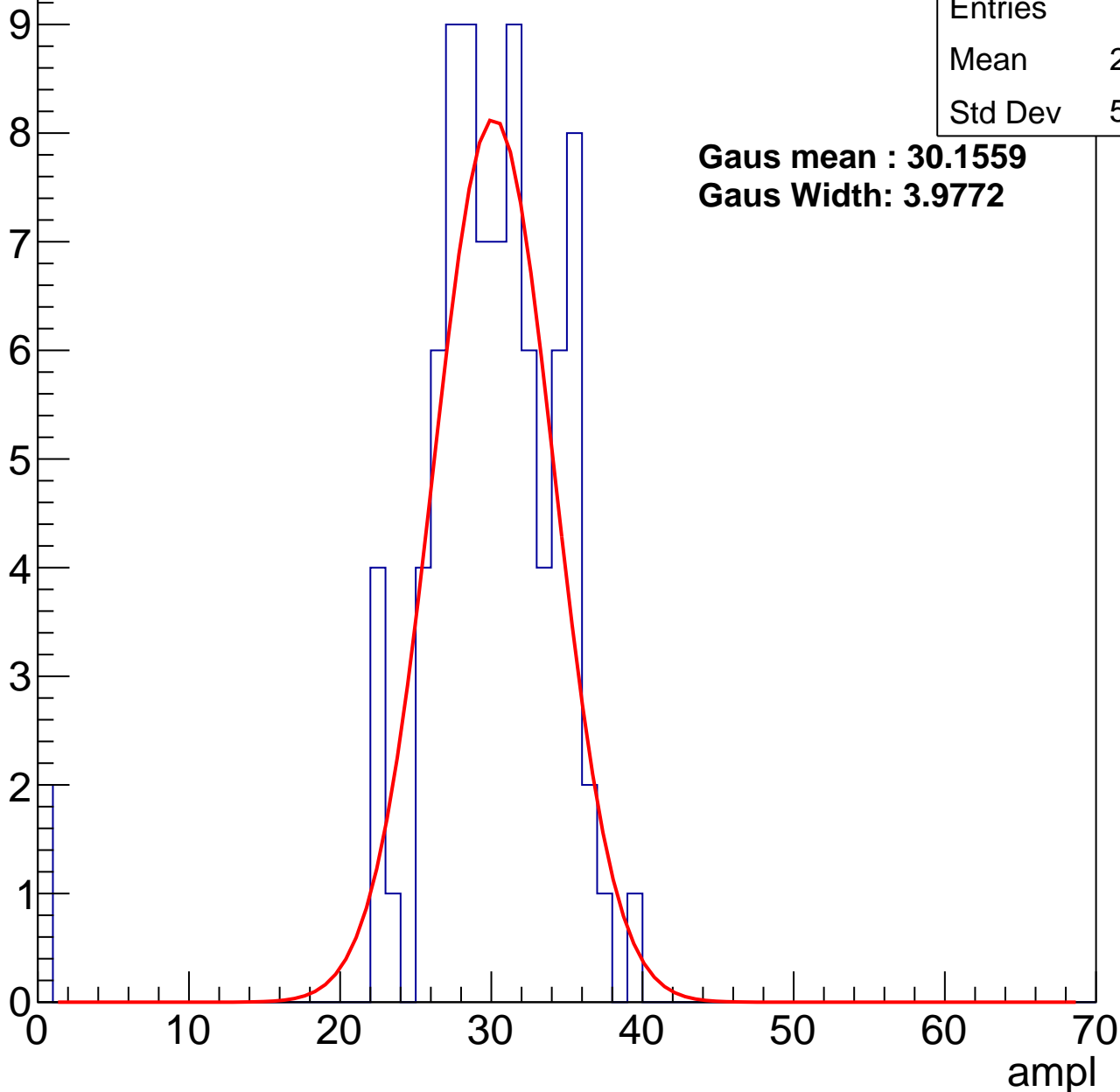
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	86
Mean	29.19
Std Dev	5.842

**Gaus mean : 30.1559**

**Gaus Width: 3.9772**



# B1L102S, U21-ch78, adc1

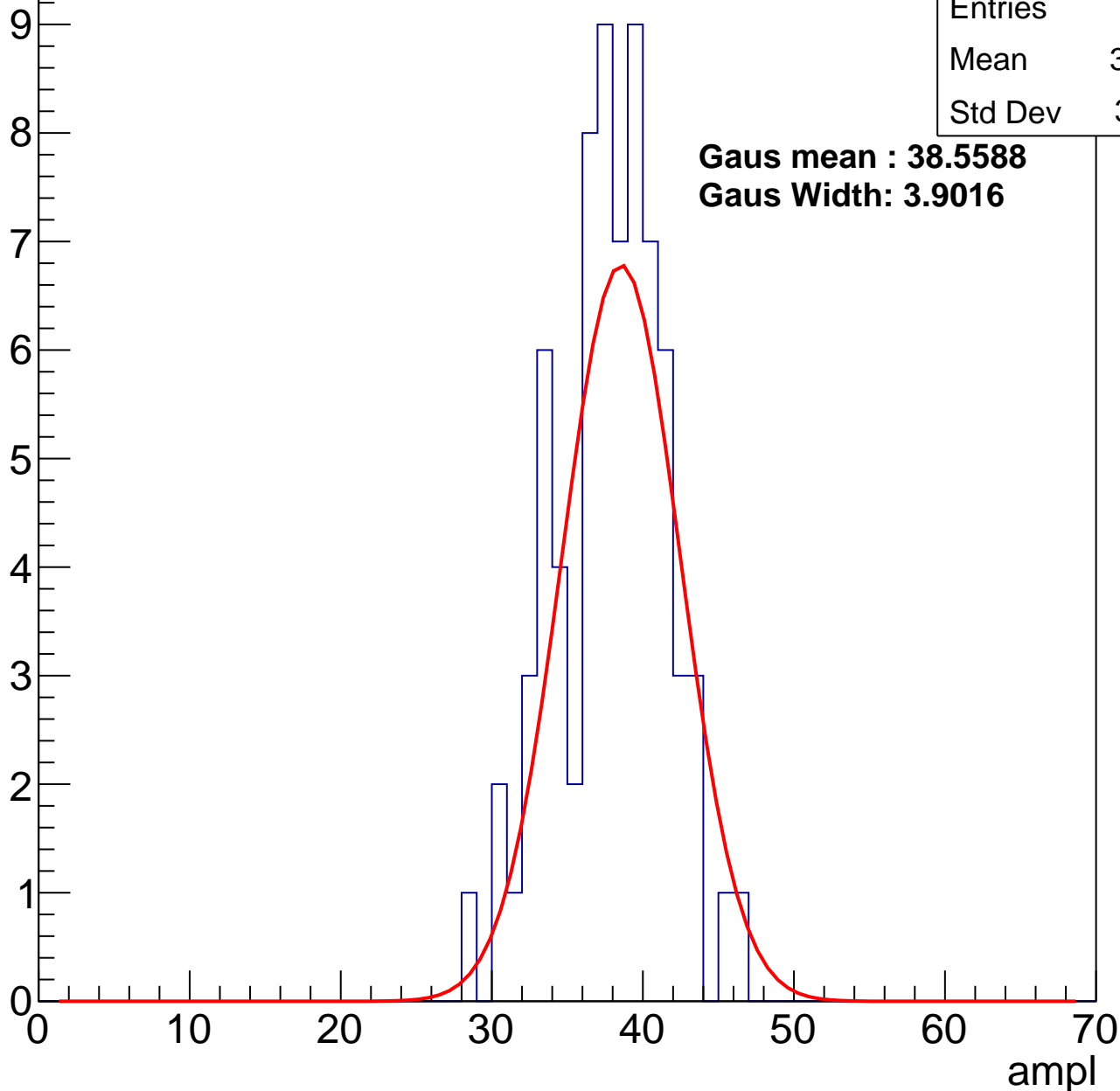
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	37.38
Std Dev	3.621

**Gaus mean : 38.5588**

**Gaus Width: 3.9016**



# B1L102S, U21-ch78, adc2

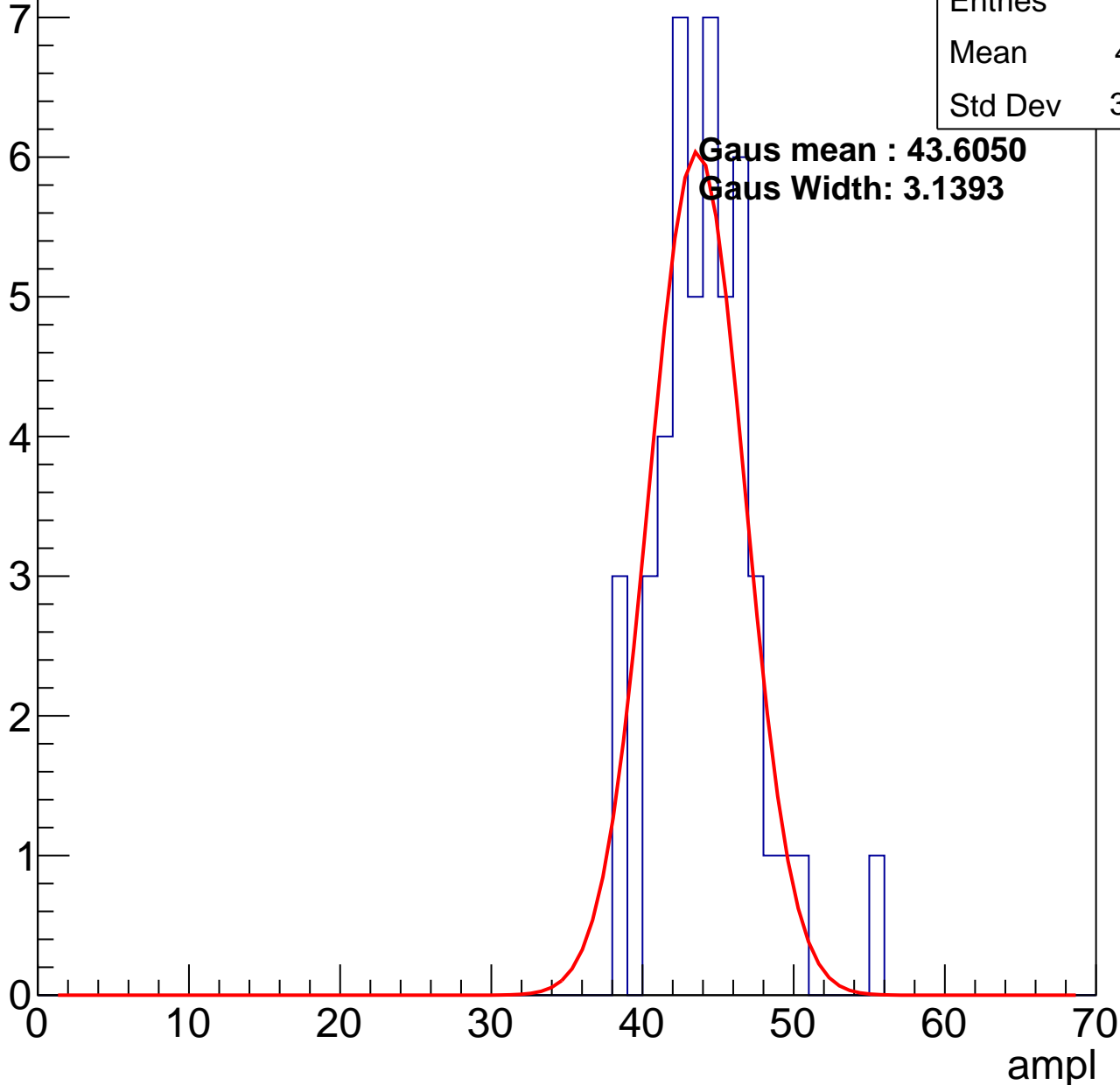
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	43.81
Std Dev	3.187

**Gaus mean : 43.6050**

**Gaus Width: 3.1393**

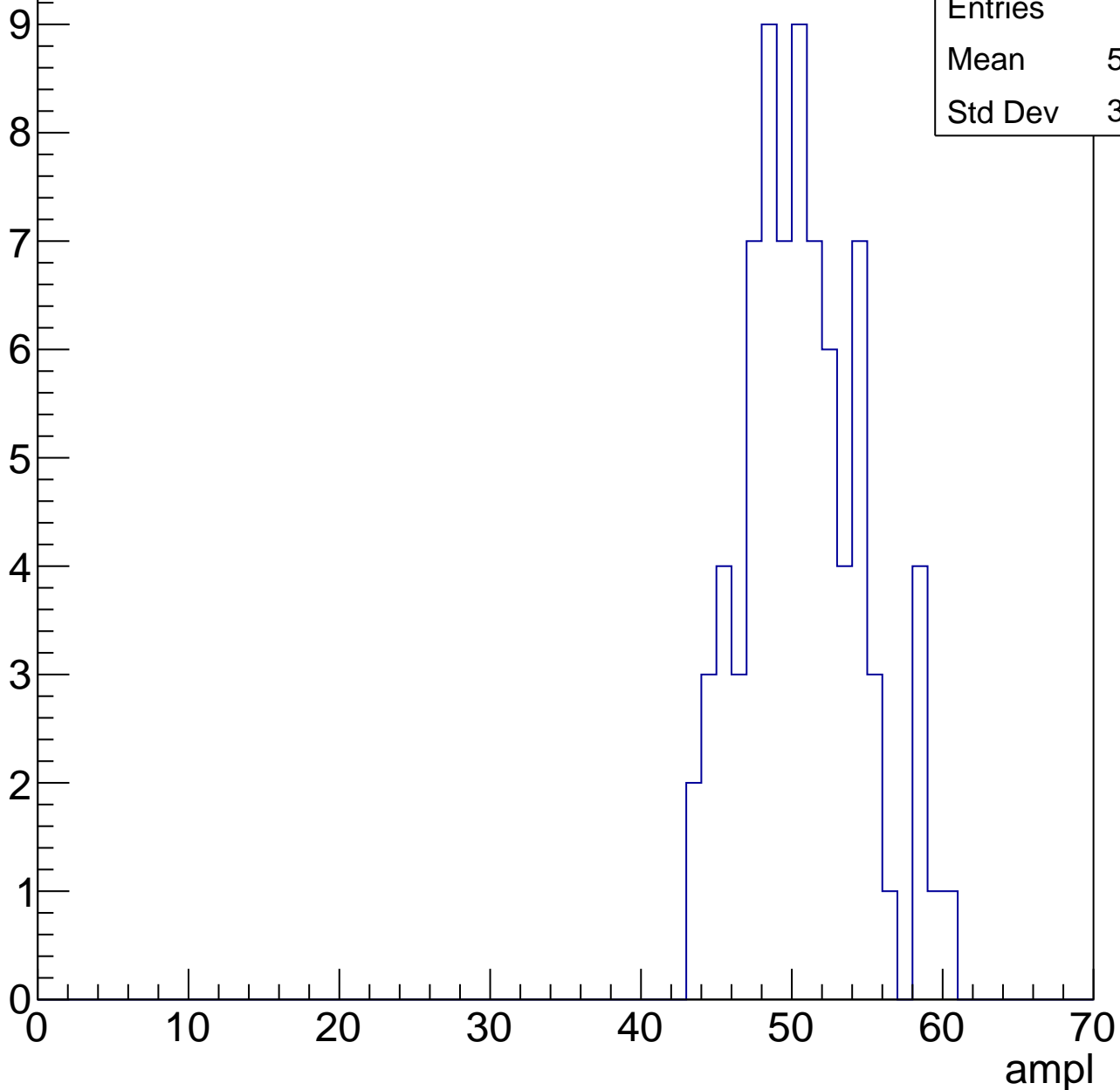


# B1L102S, U21-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	50.27
Std Dev	3.892

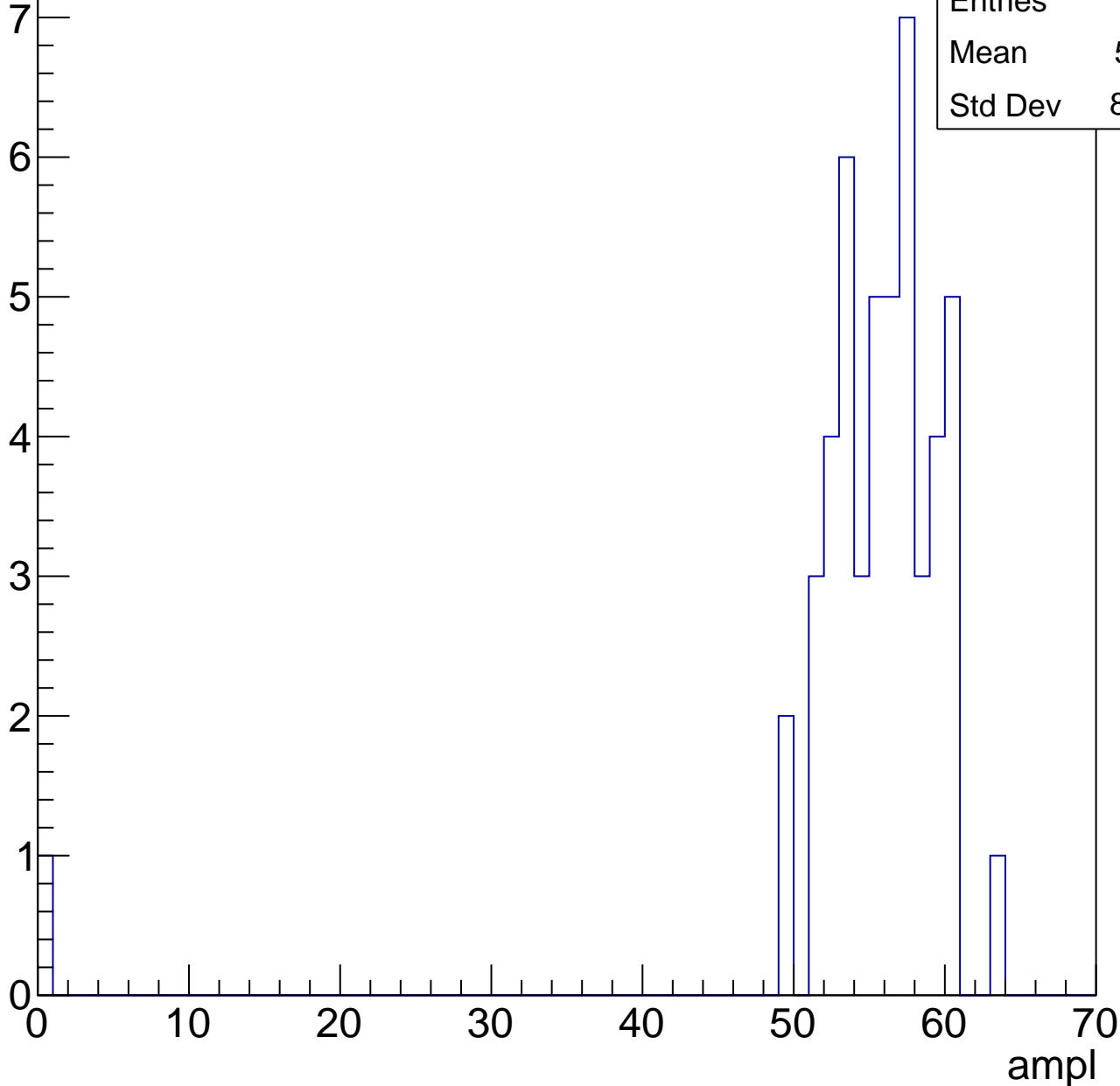


# B1L102S, U21-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	54.41
Std Dev	8.456

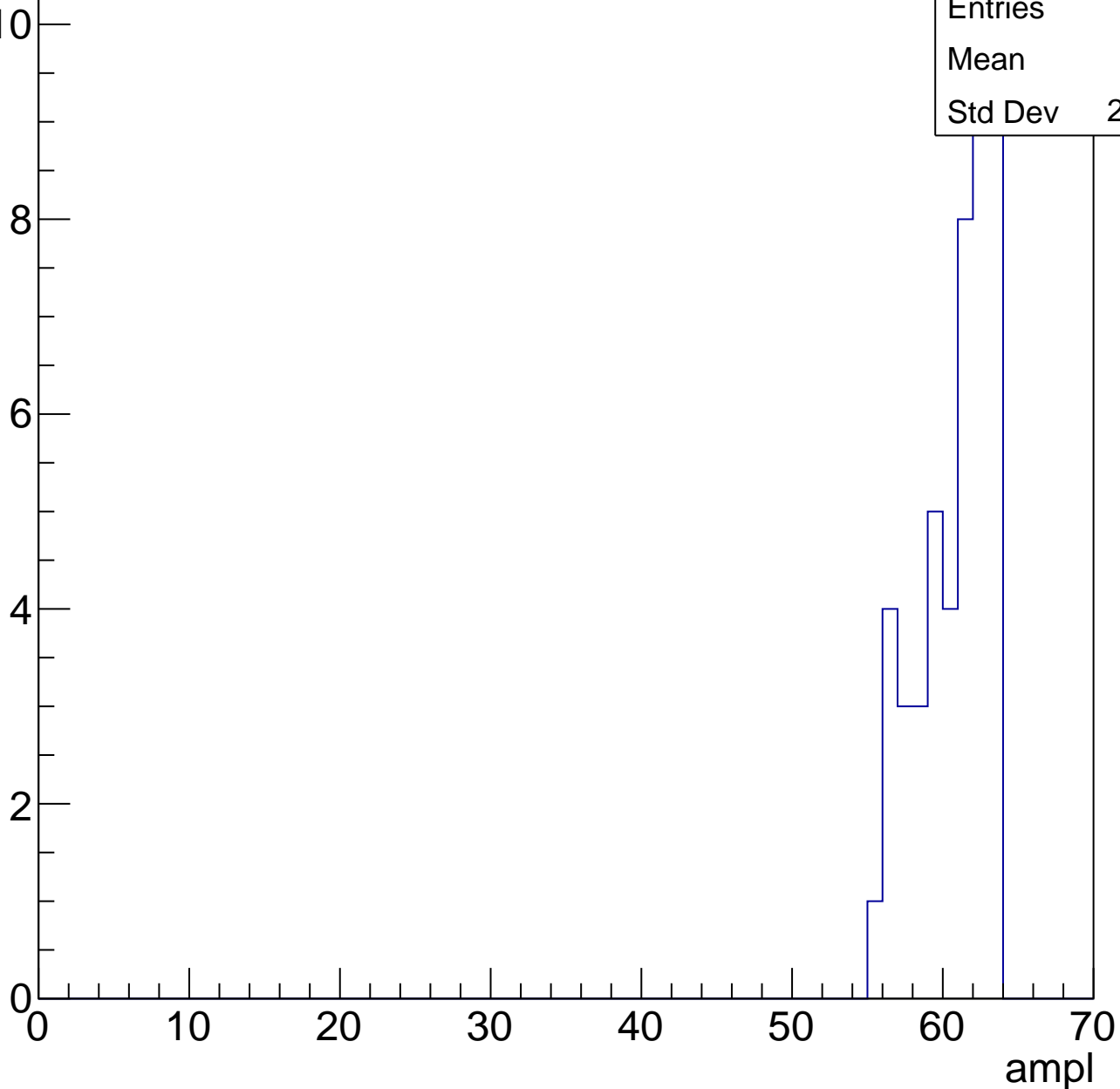


# B1L102S, U21-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

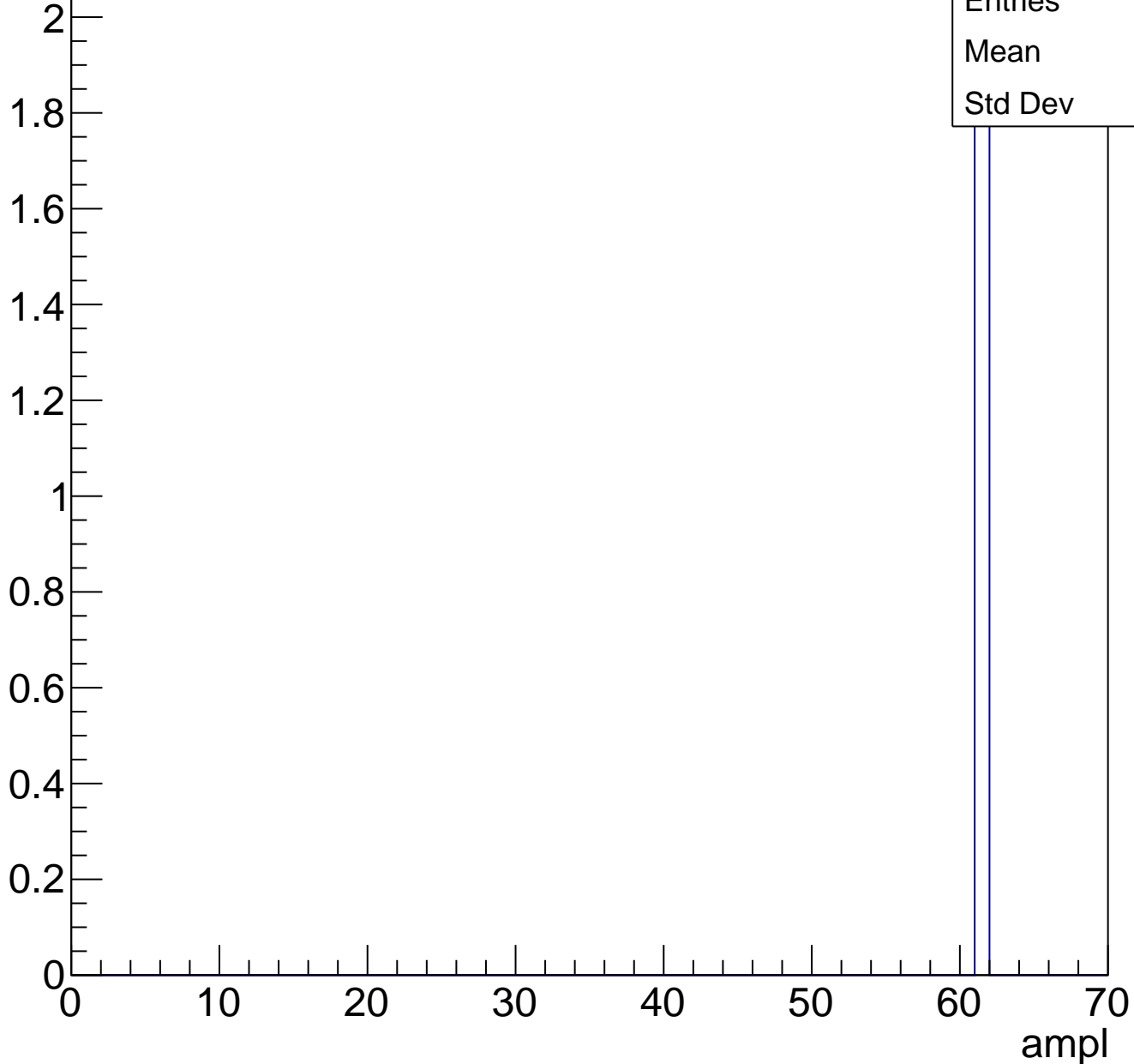
Entries	47
Mean	60.3
Std Dev	2.342



# B1L102S, U21-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	11
Std Dev	11

# B1L102S, U21-ch79, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	76
Mean	28.16
Std Dev	3.449

**Gaus mean : 28.7271**

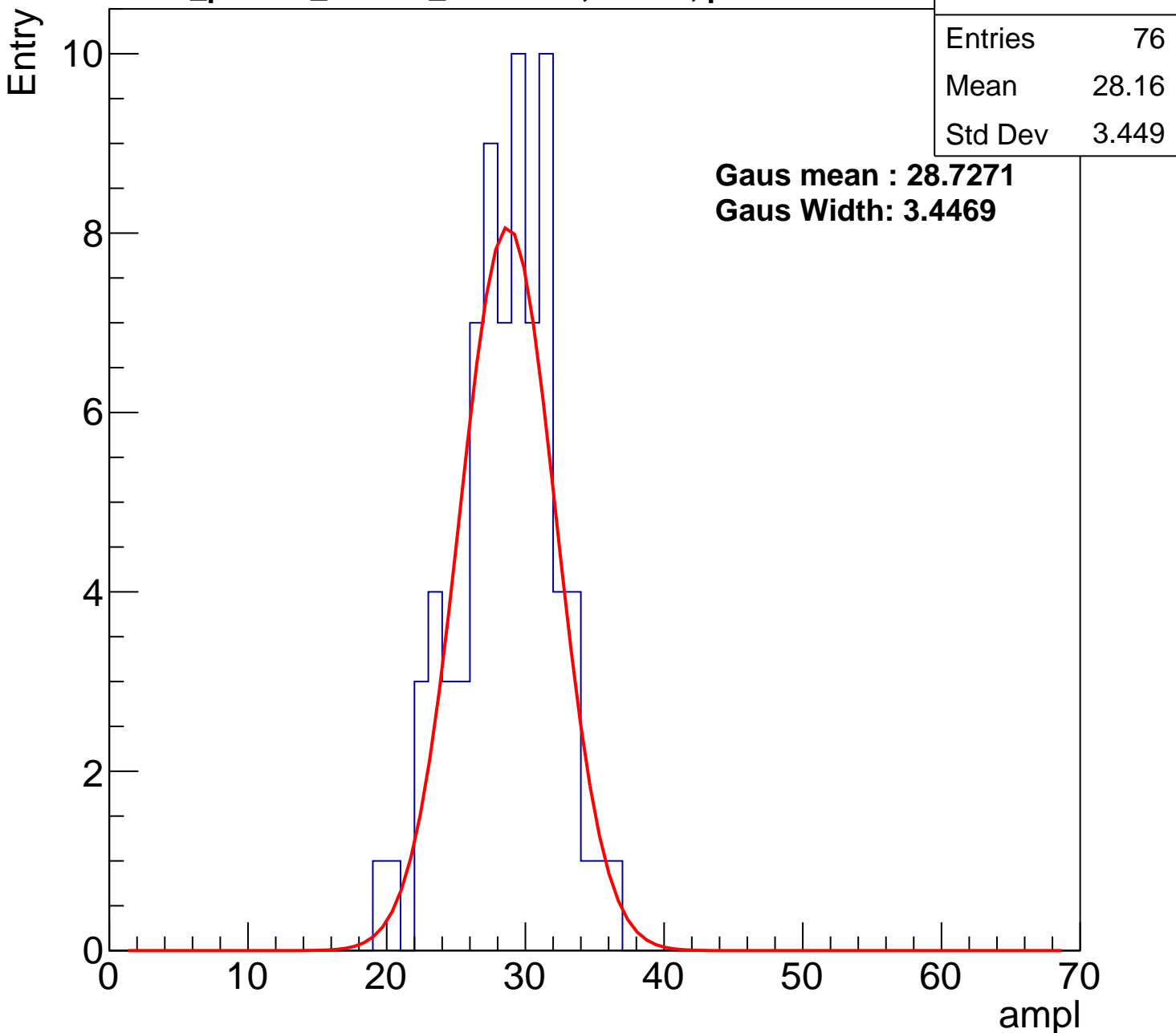
**Gaus Width: 3.4469**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U21-ch79, adc1

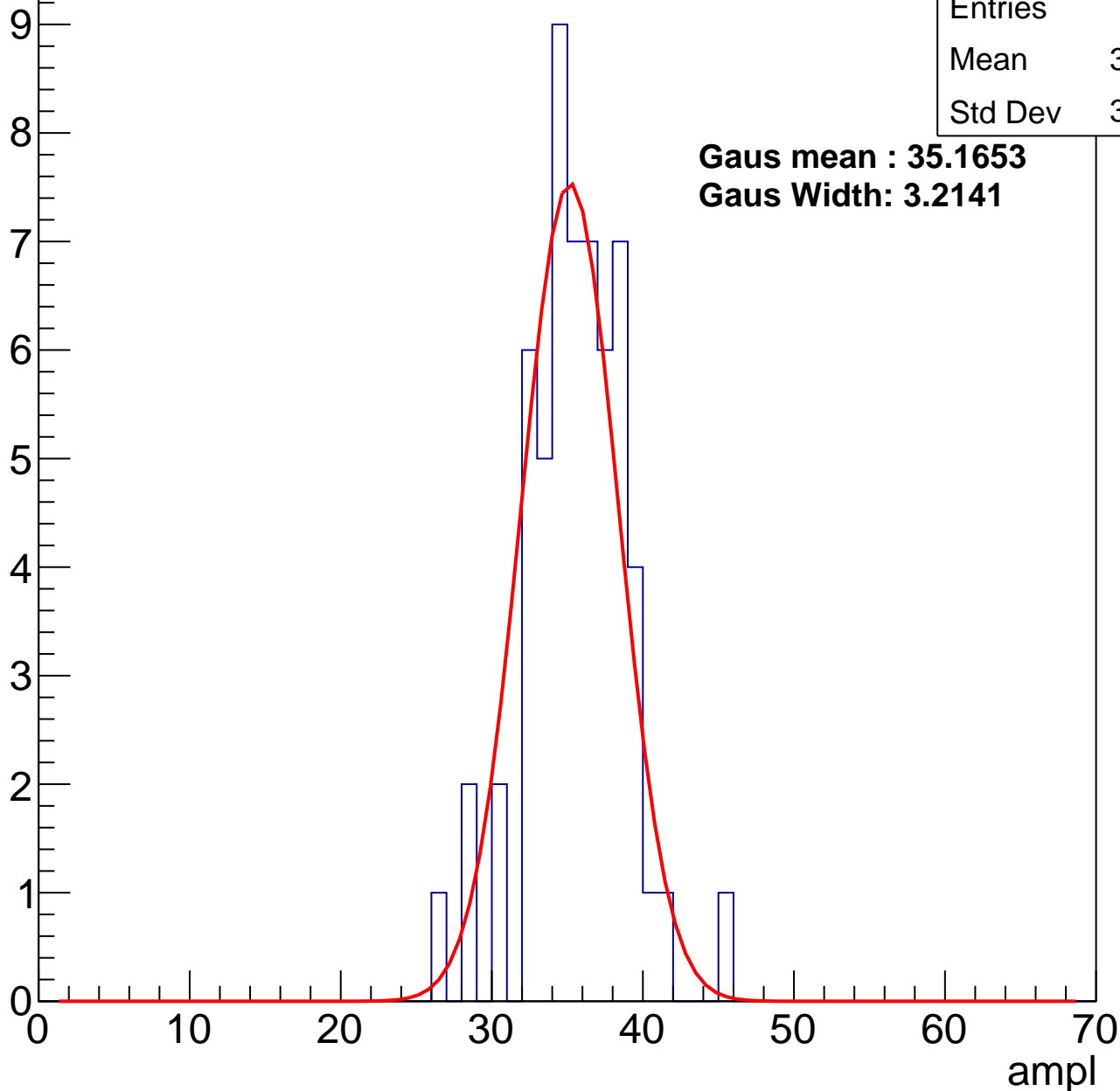
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	35.12
Std Dev	3.268

**Gaus mean : 35.1653**

**Gaus Width: 3.2141**



# B1L102S, U21-ch79, adc2

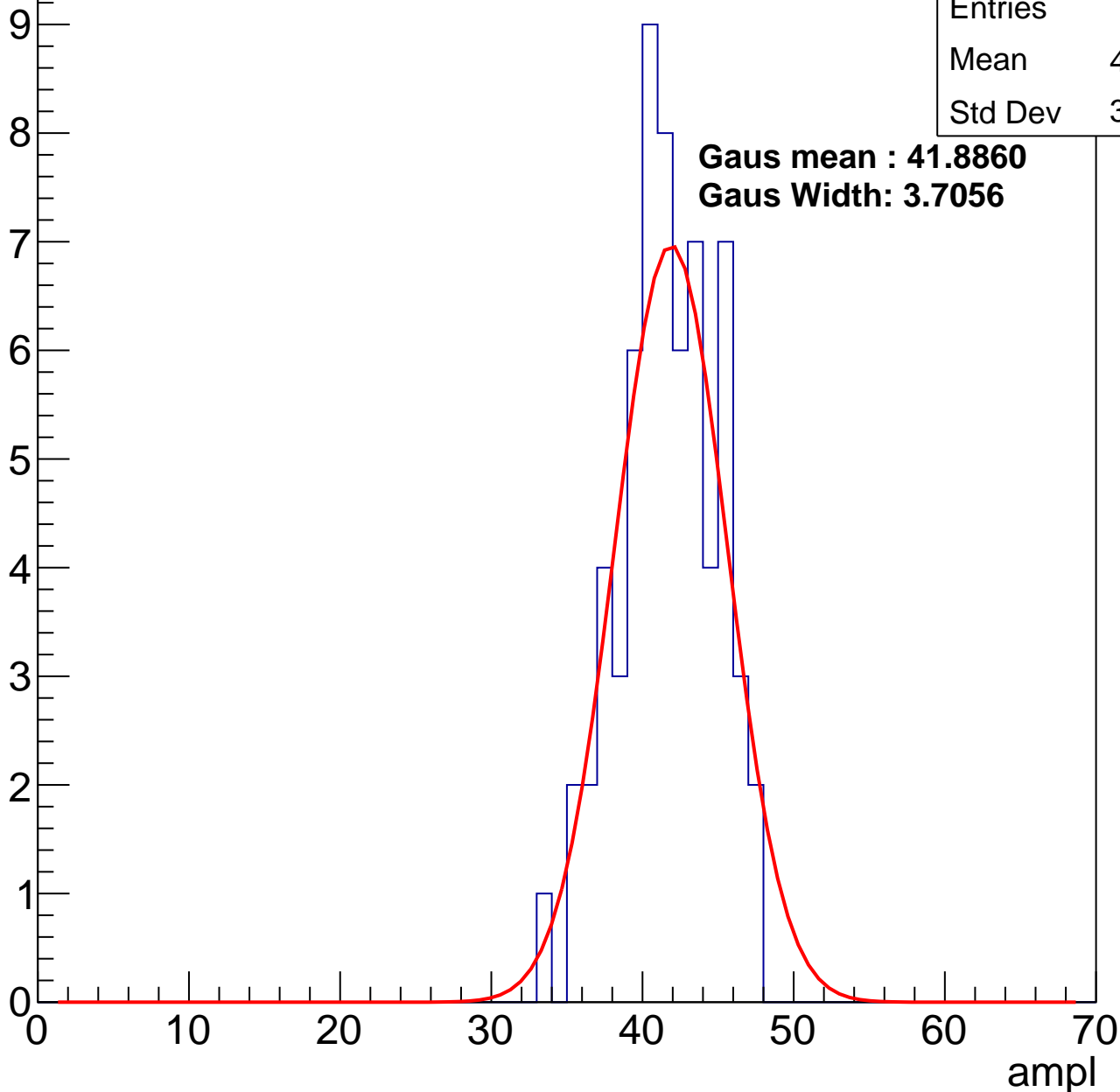
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	41.17
Std Dev	3.155

**Gaus mean : 41.8860**

**Gaus Width: 3.7056**

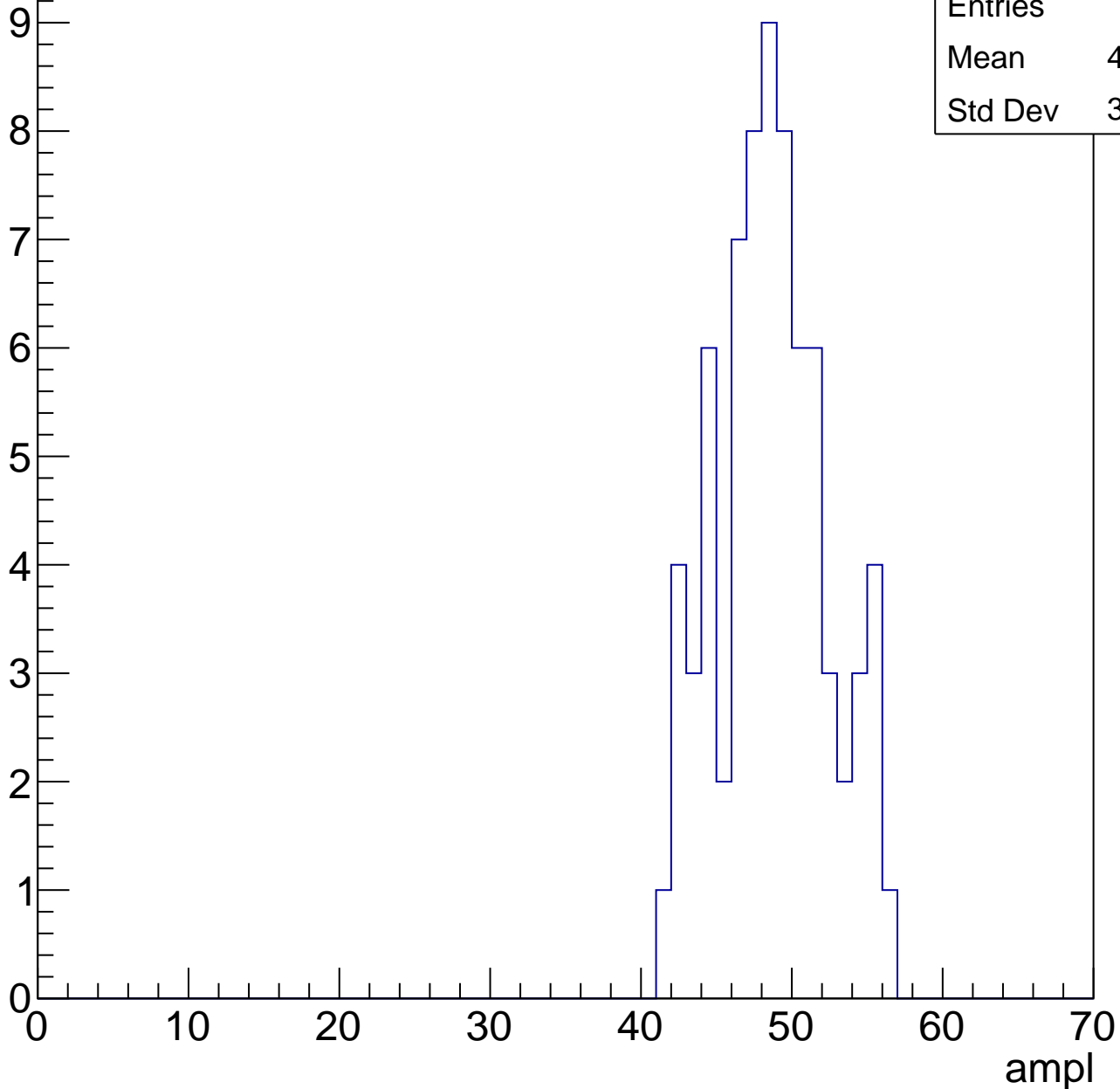


# B1L102S, U21-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	48.22
Std Dev	3.639

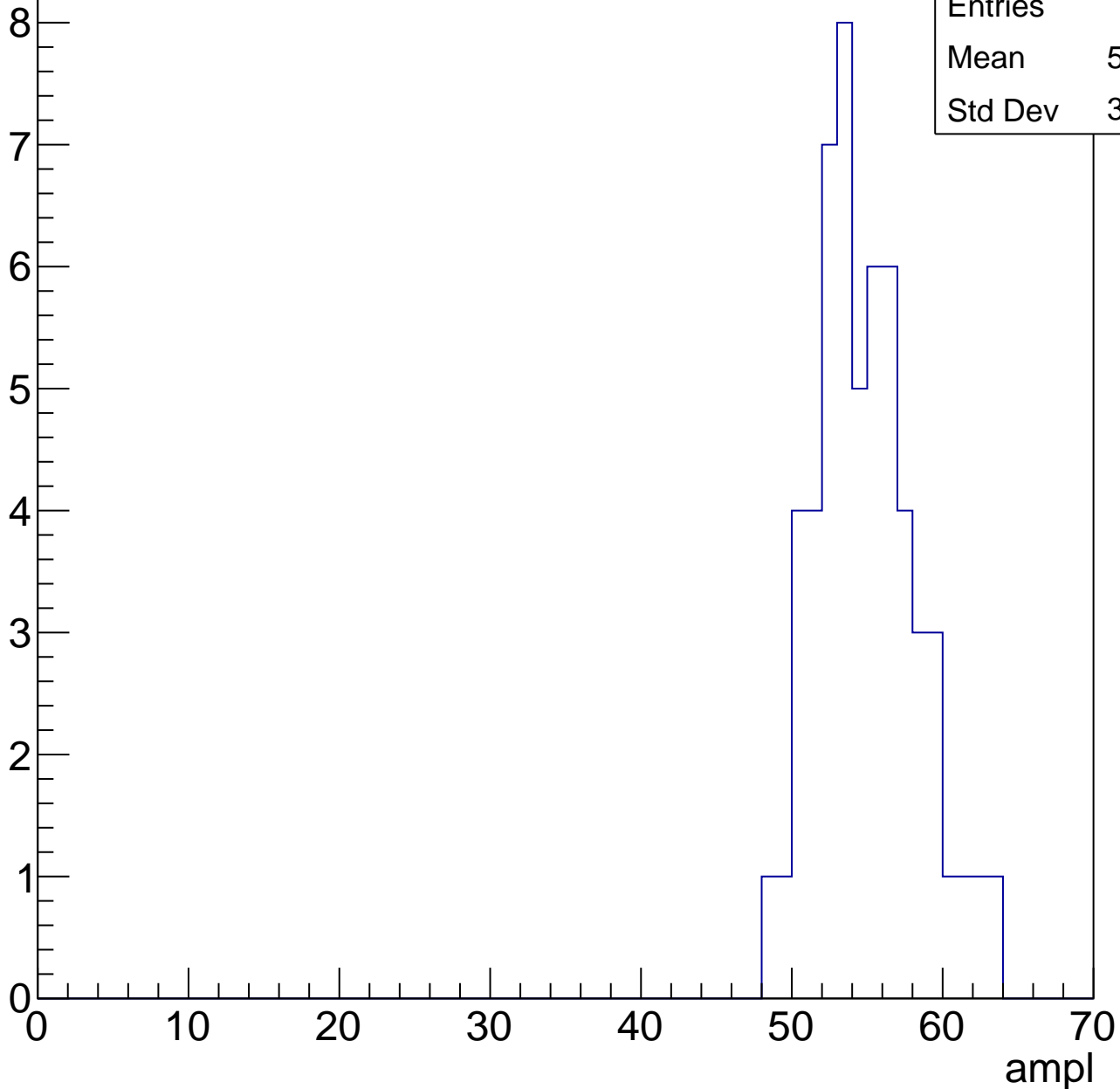


# B1L102S, U21-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	54.46
Std Dev	3.284

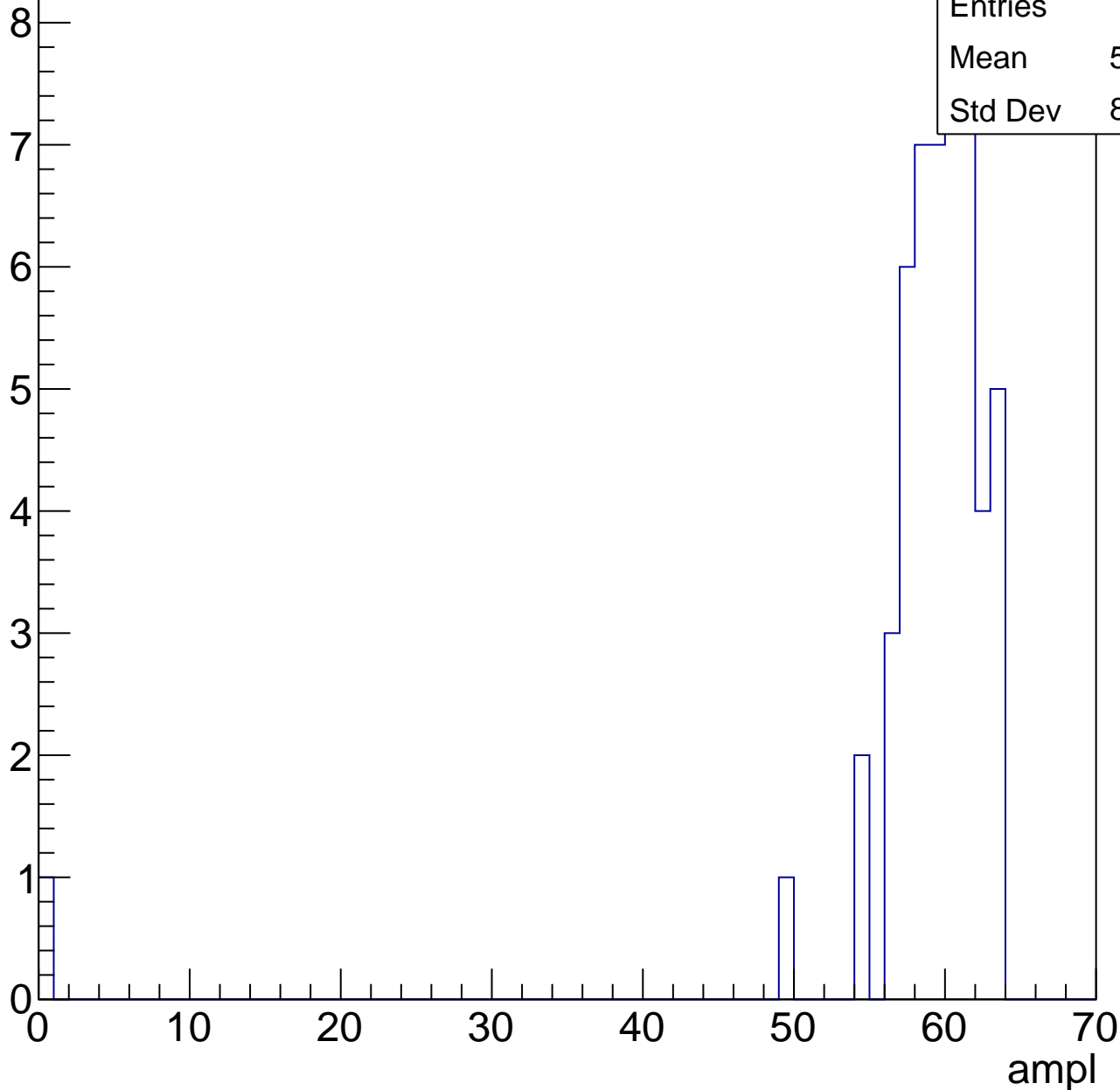


# B1L102S, U21-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	58.02
Std Dev	8.543

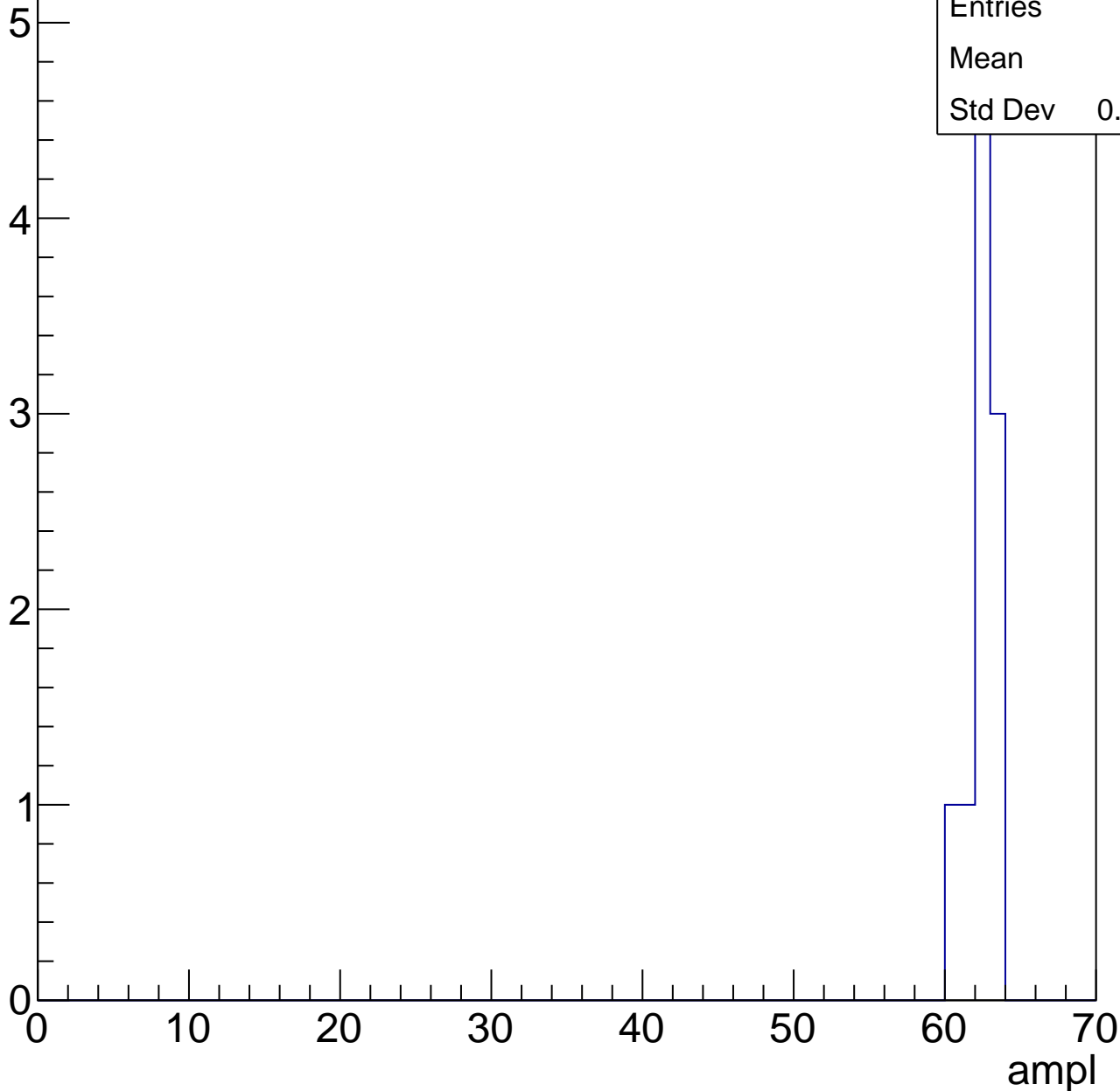


# B1L102S, U21-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	10
Mean	62
Std Dev	0.8944





# B1L102S, U21-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch80, adc0

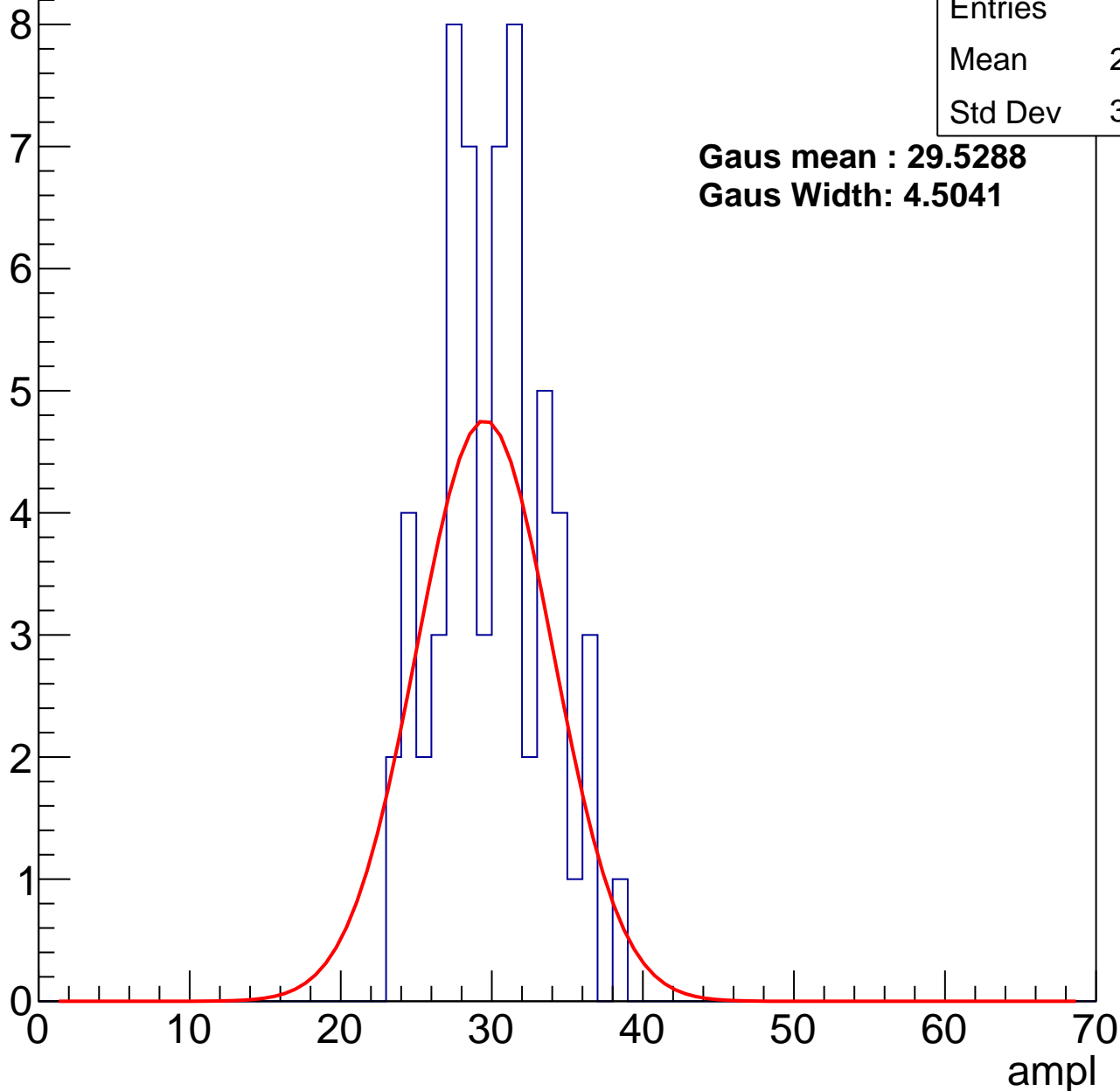
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	29.55
Std Dev	3.542

**Gaus mean : 29.5288**

**Gaus Width: 4.5041**



# B1L102S, U21-ch80, adc1

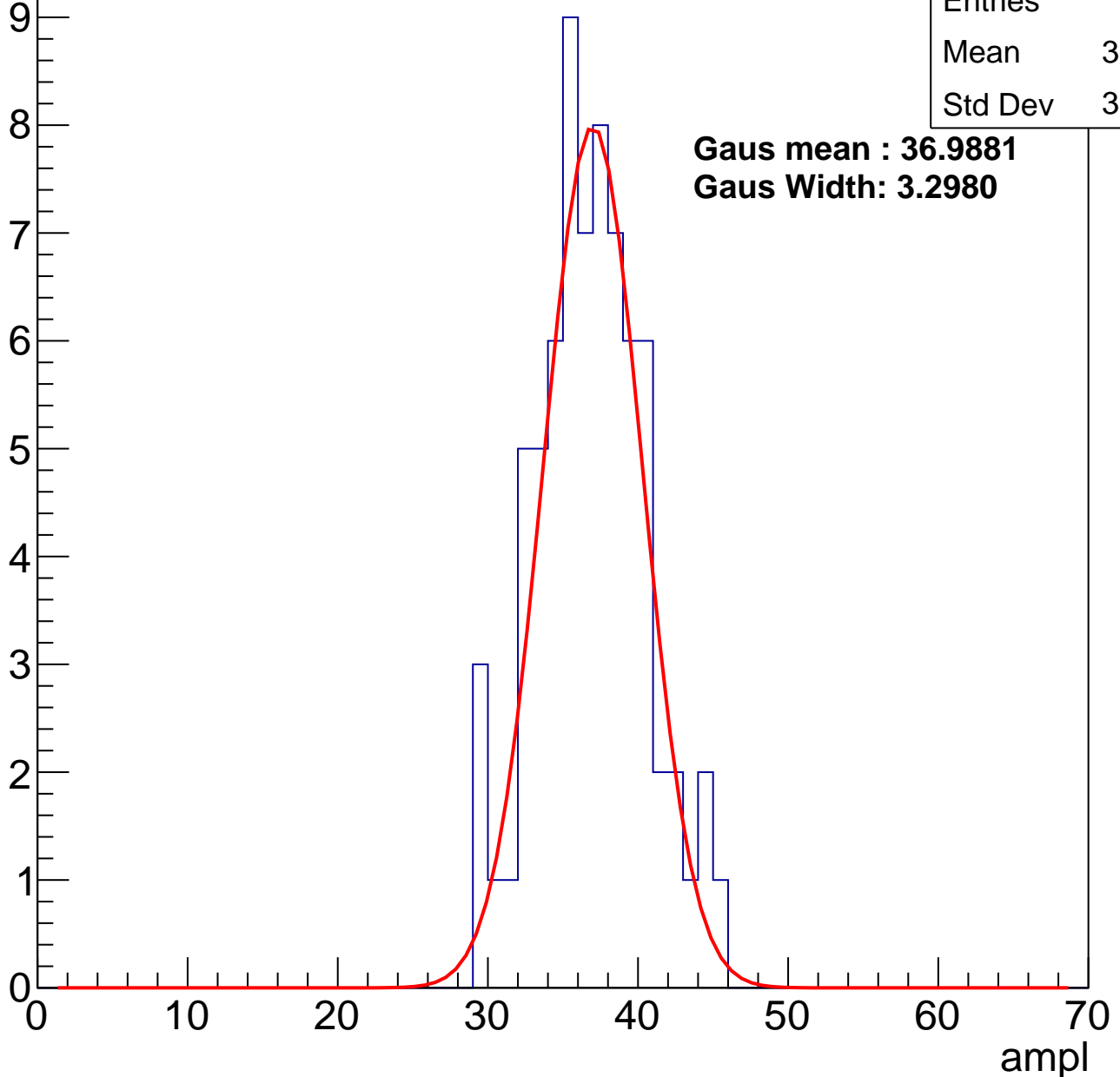
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	36.42
Std Dev	3.574

**Gaus mean : 36.9881**

**Gaus Width: 3.2980**



# B1L102S, U21-ch80, adc2

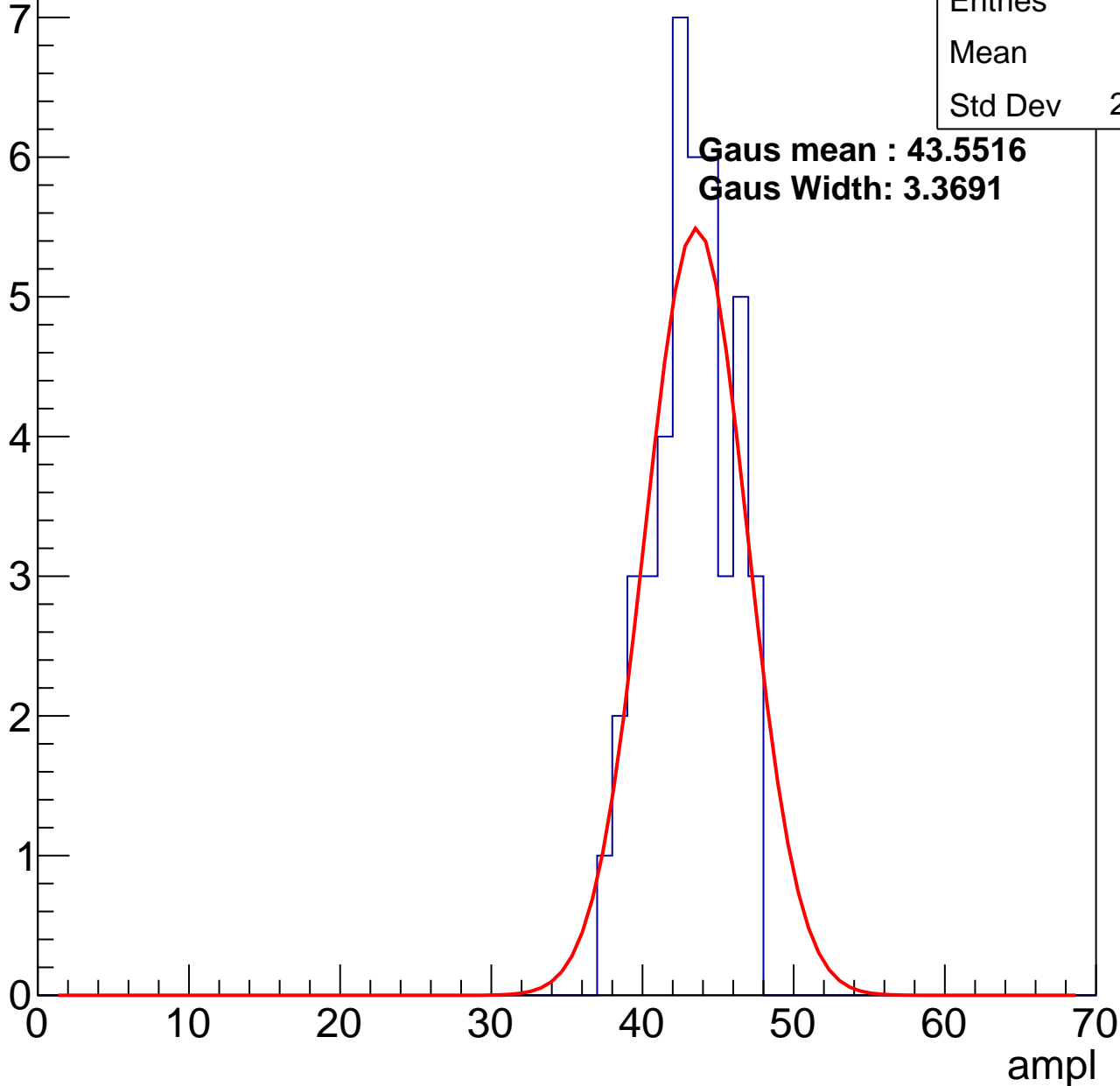
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	43
Mean	42.7
Std Dev	2.602

**Gaus mean : 43.5516**

**Gaus Width: 3.3691**



# B1L102S, U21-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	93
Mean	48.9
Std Dev	4.281

Entry

10

8

6

4

2

0

0

10

20

30

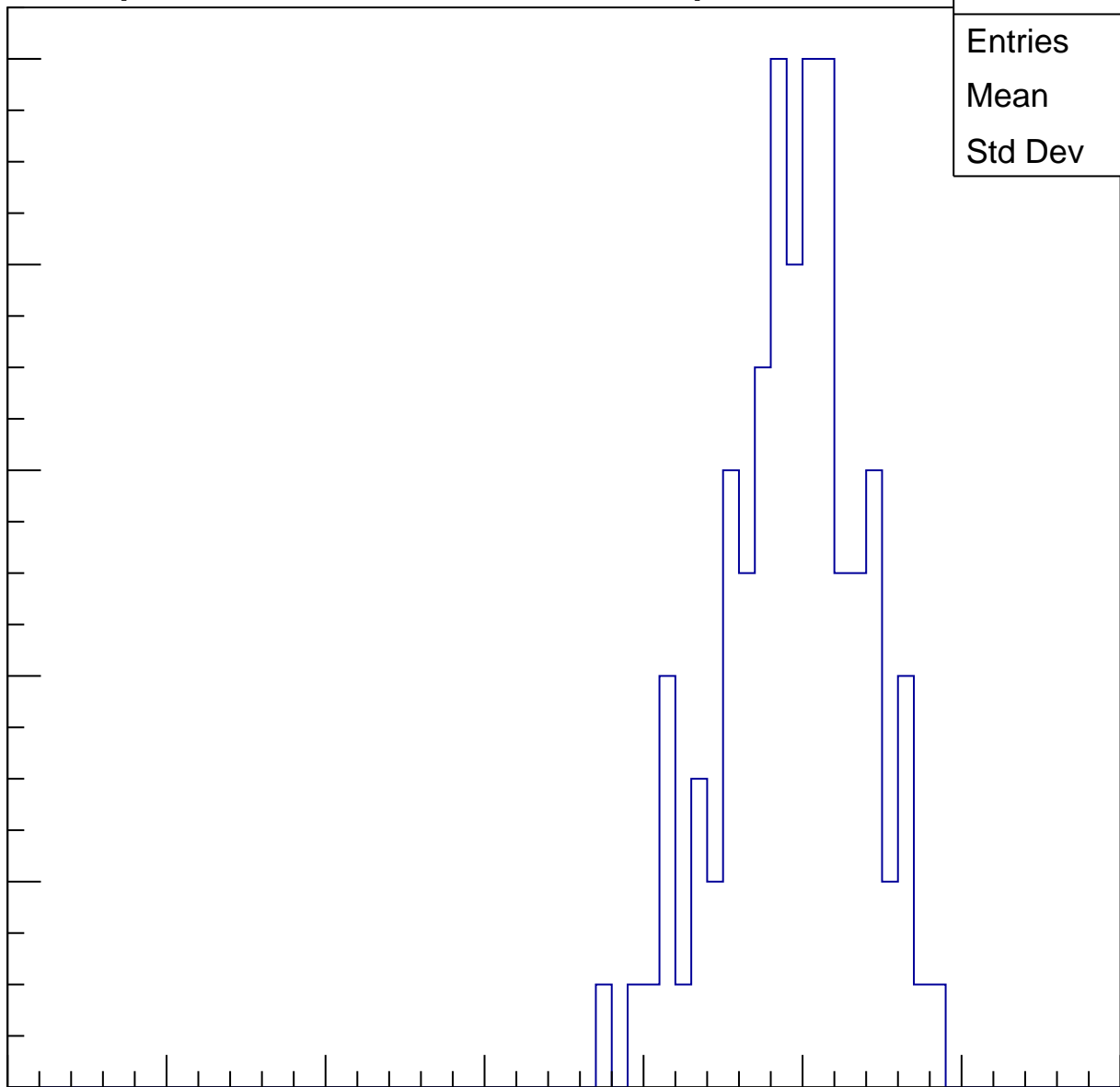
40

50

60

70

ampl

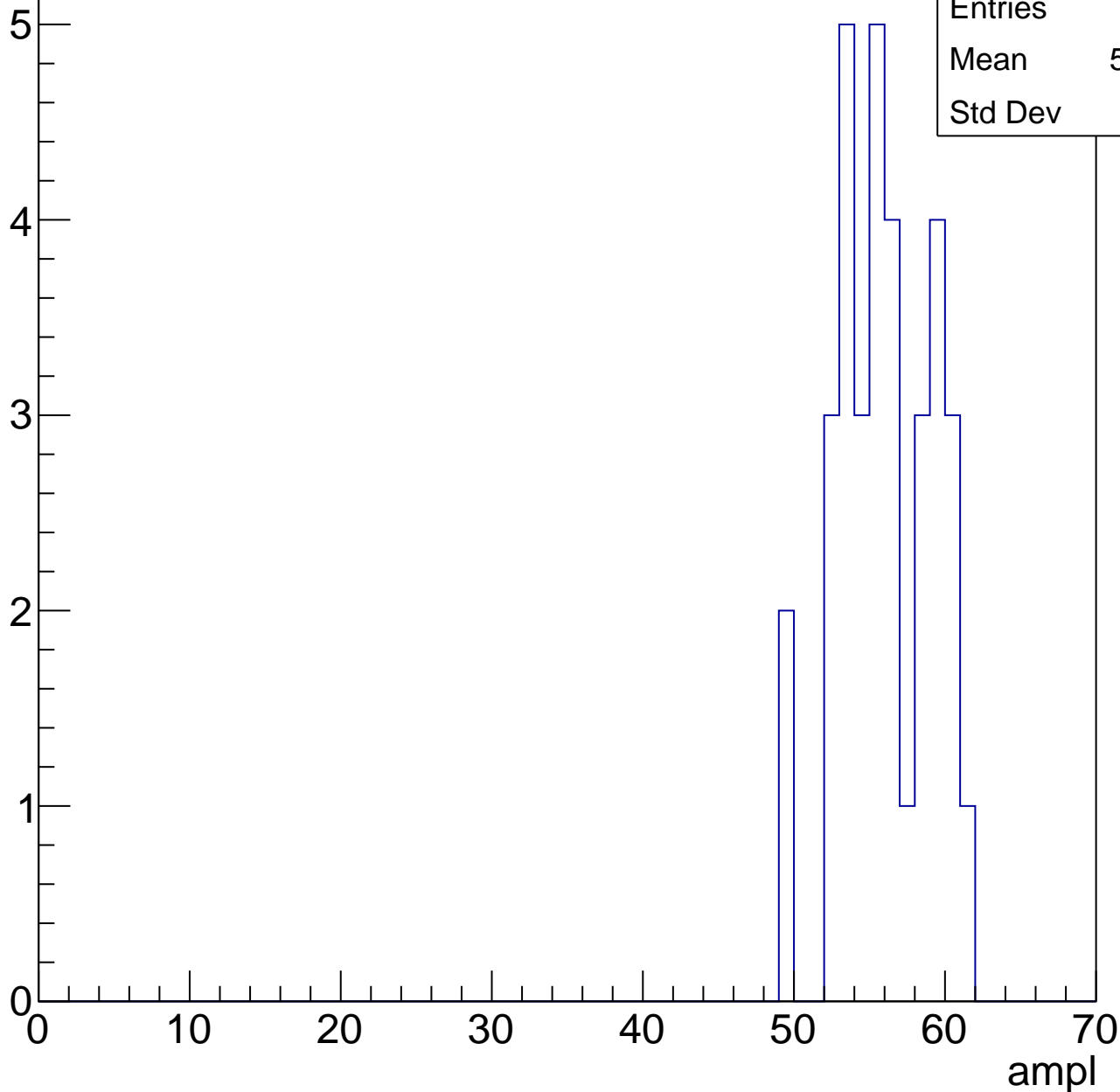


# B1L102S, U21-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	34
Mean	55.53
Std Dev	3.08

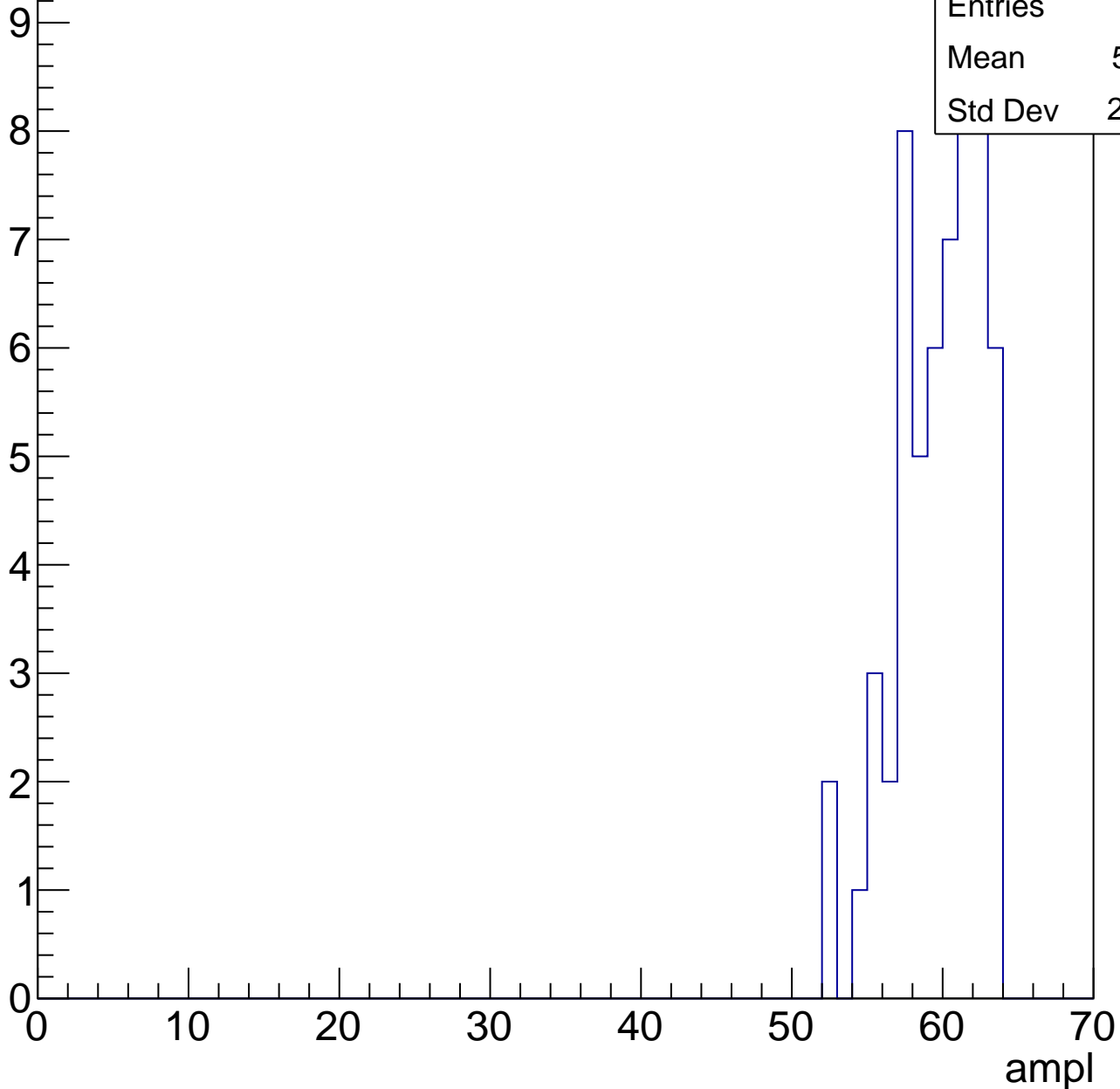


# B1L102S, U21-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

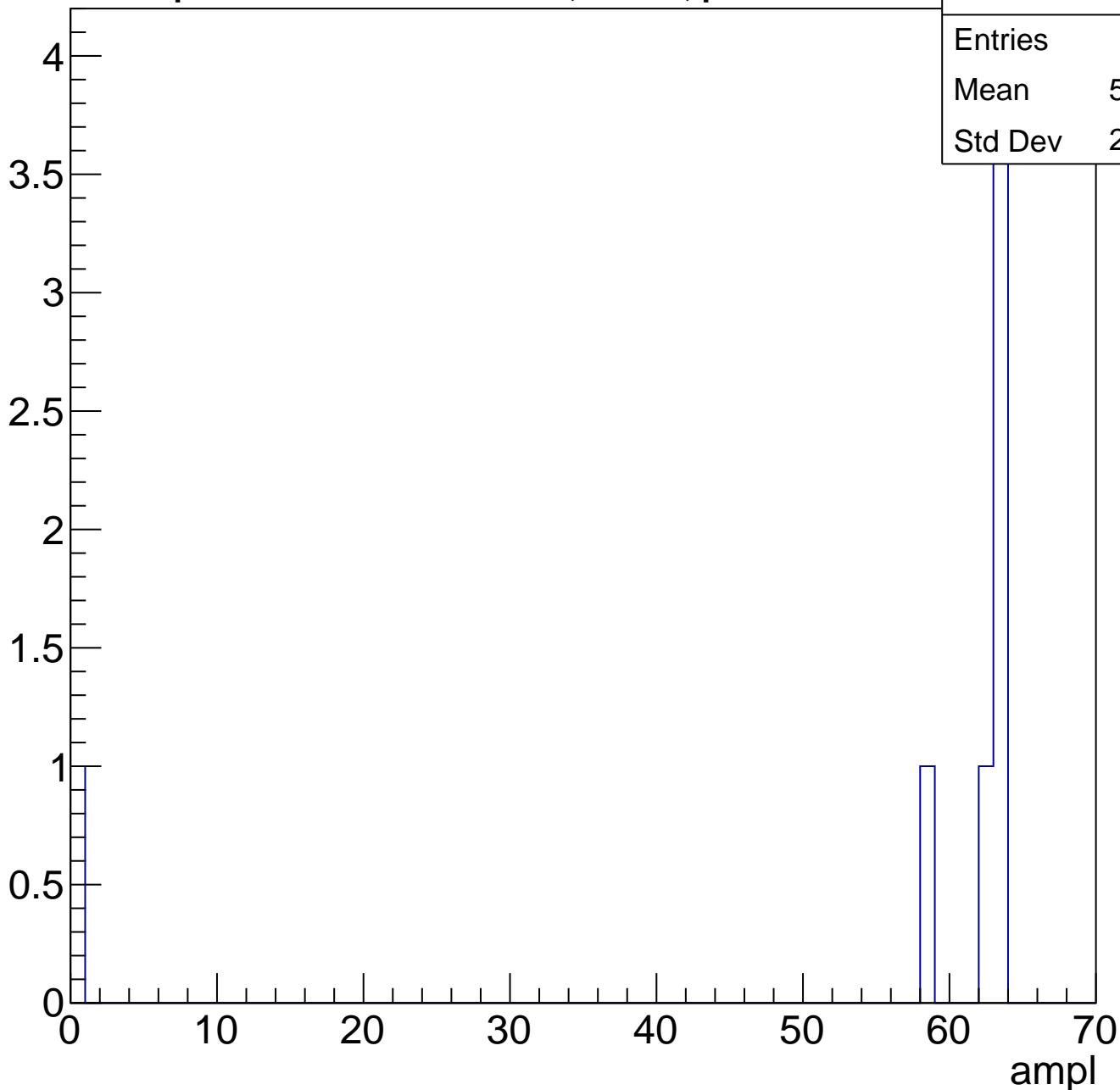
Entries	58
Mean	59.31
Std Dev	2.756



# B1L102S, U21-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	11.5
Std Dev	11.5

# B1L102S, U21-ch81, adc0

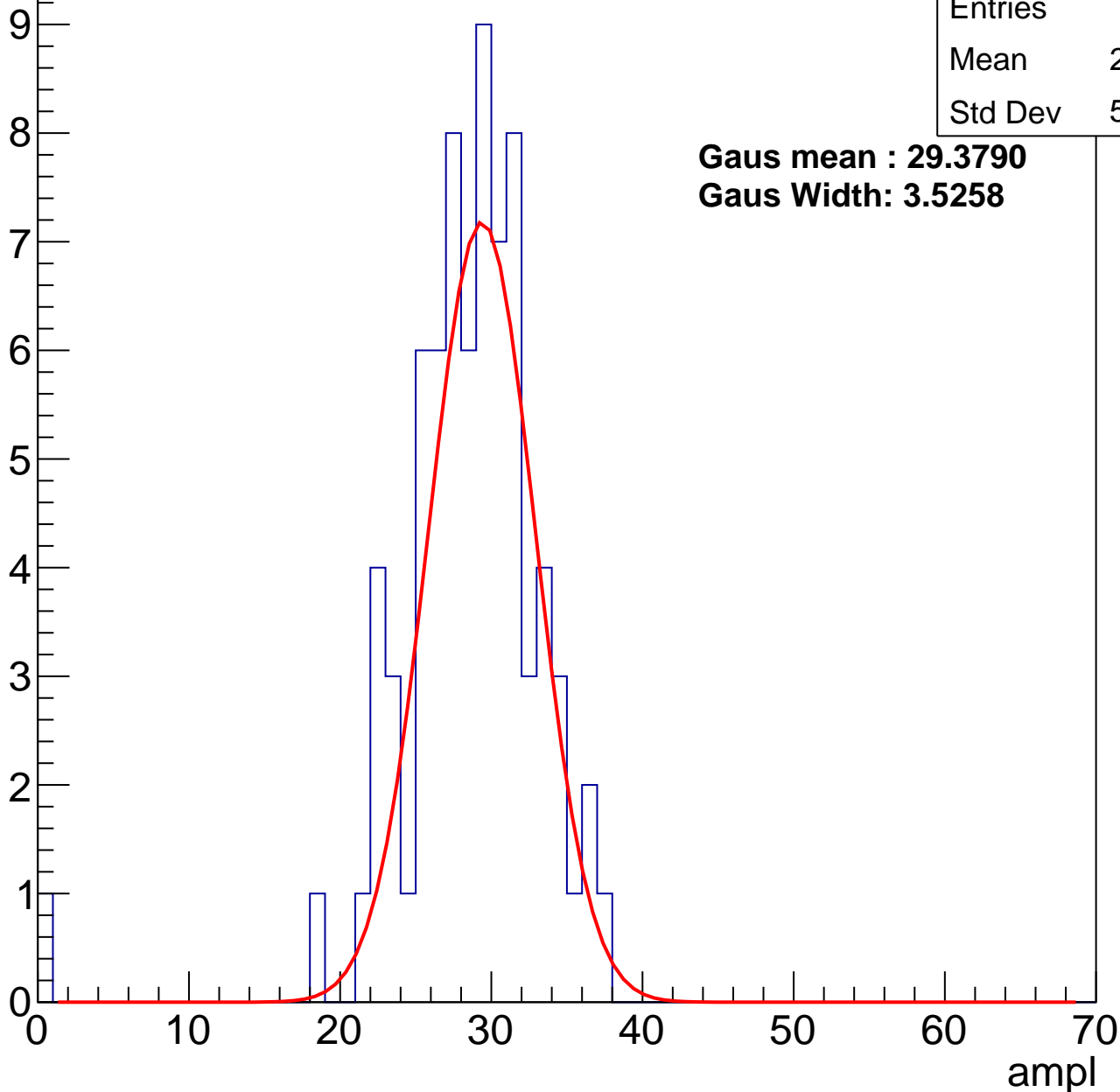
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	28.04
Std Dev	5.003

**Gaus mean : 29.3790**

**Gaus Width: 3.5258**



# B1L102S, U21-ch81, adc1

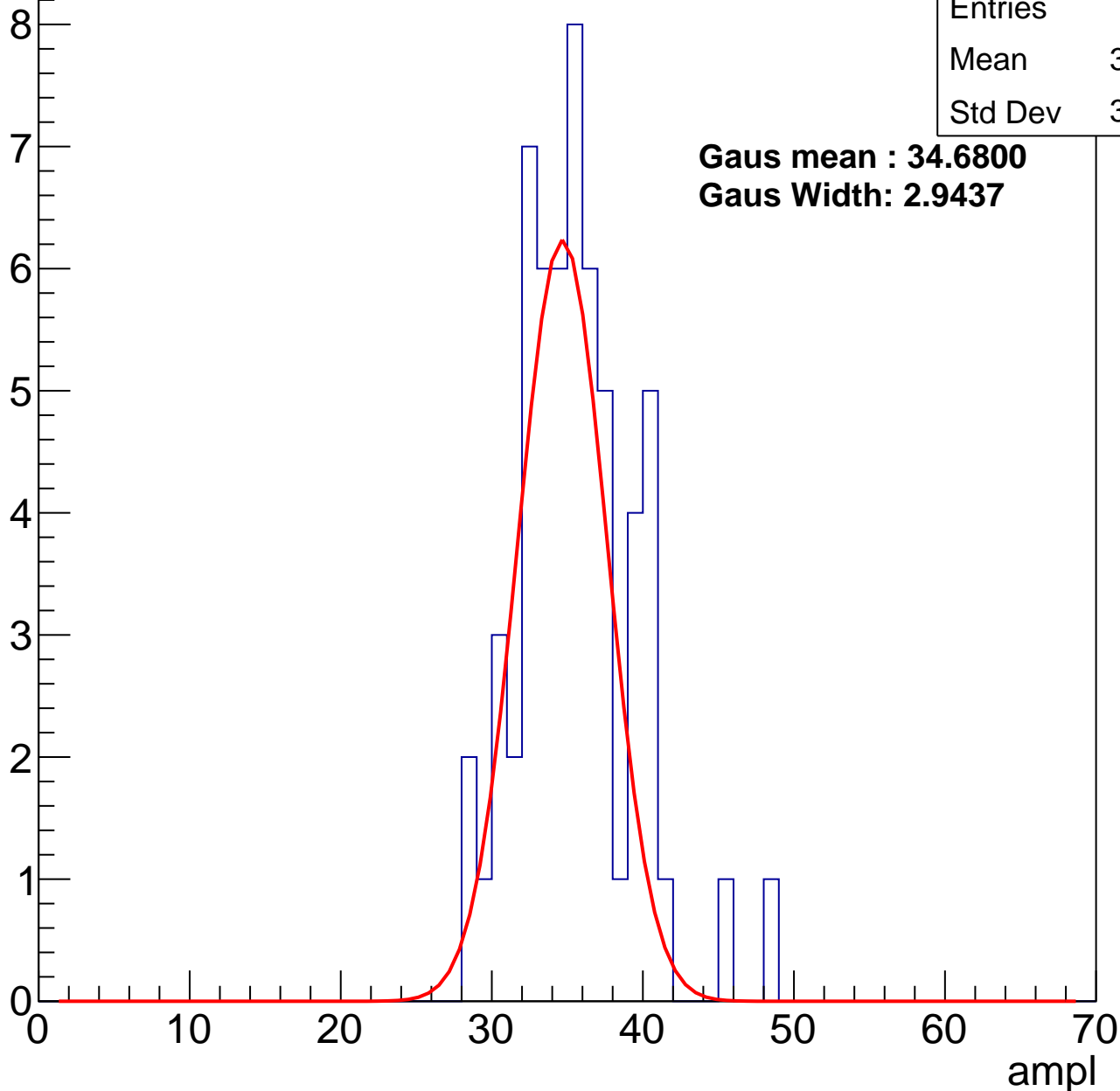
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	35.12
Std Dev	3.823

**Gaus mean : 34.6800**

**Gaus Width: 2.9437**



# B1L102S, U21-ch81, adc2

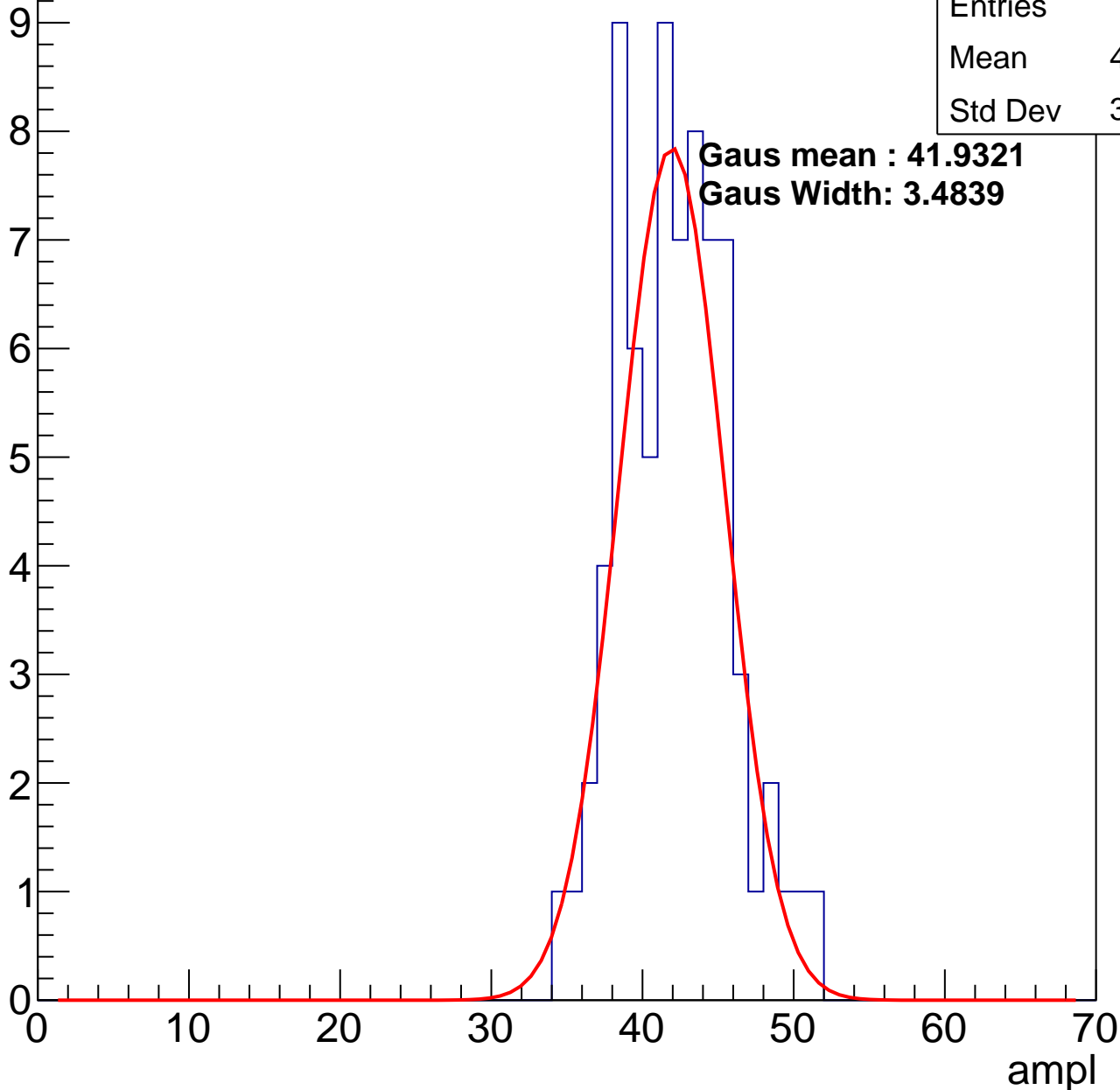
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	41.68
Std Dev	3.545

**Gaus mean : 41.9321**

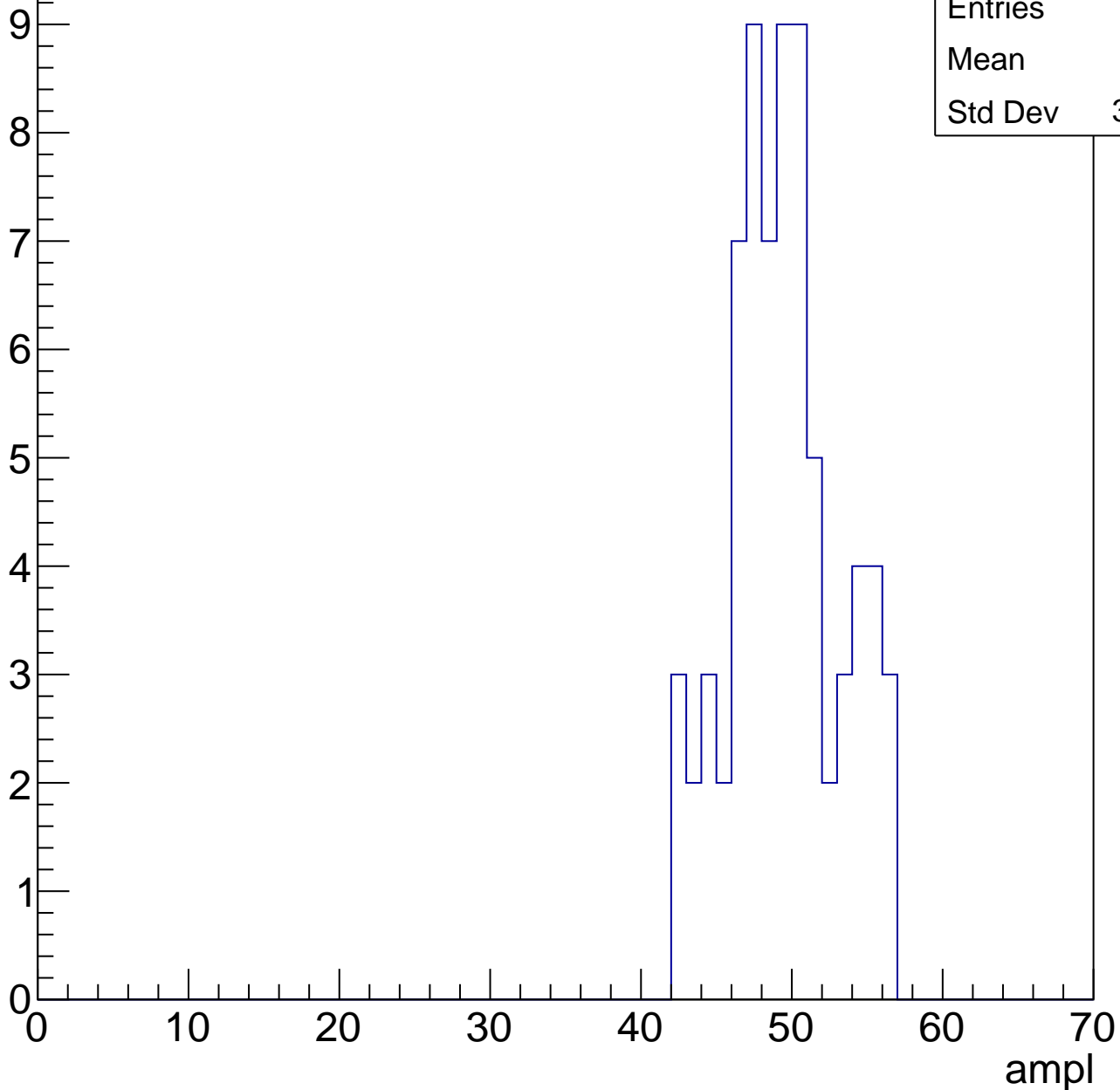
**Gaus Width: 3.4839**



# B1L102S, U21-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



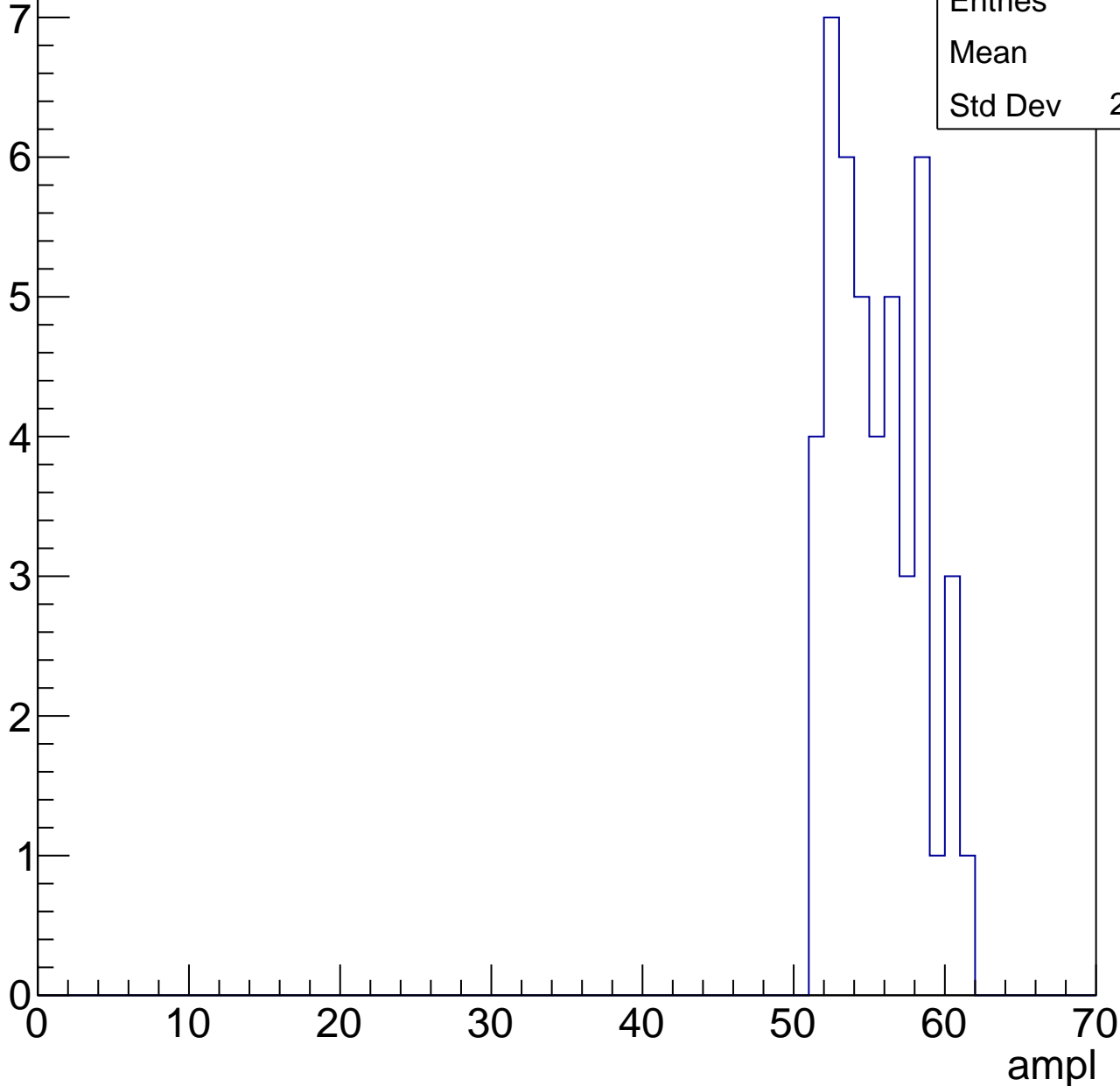
Entries	72
Mean	49
Std Dev	3.571

# B1L102S, U21-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

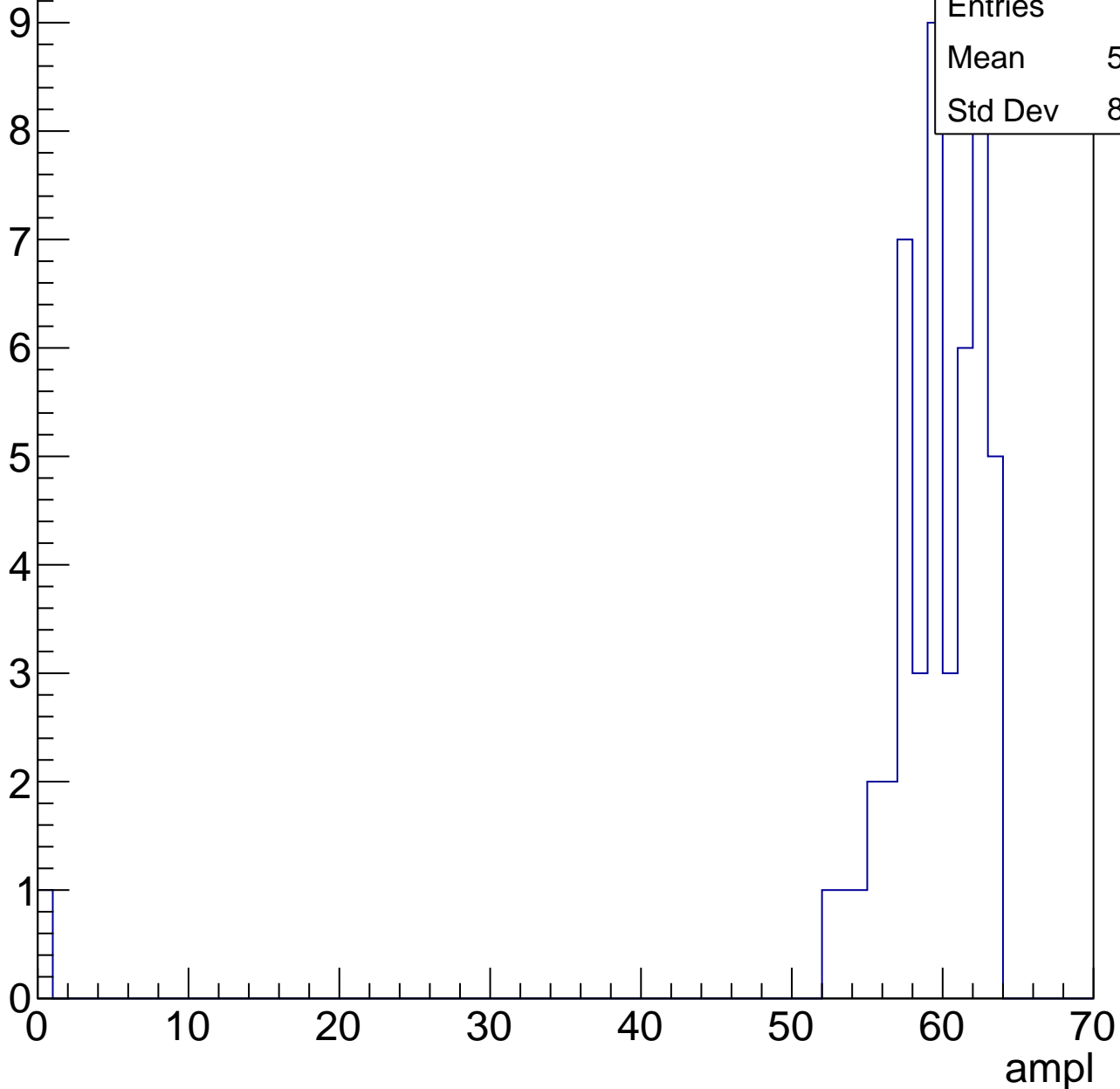
Entries	45
Mean	55
Std Dev	2.805



# B1L102S, U21-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

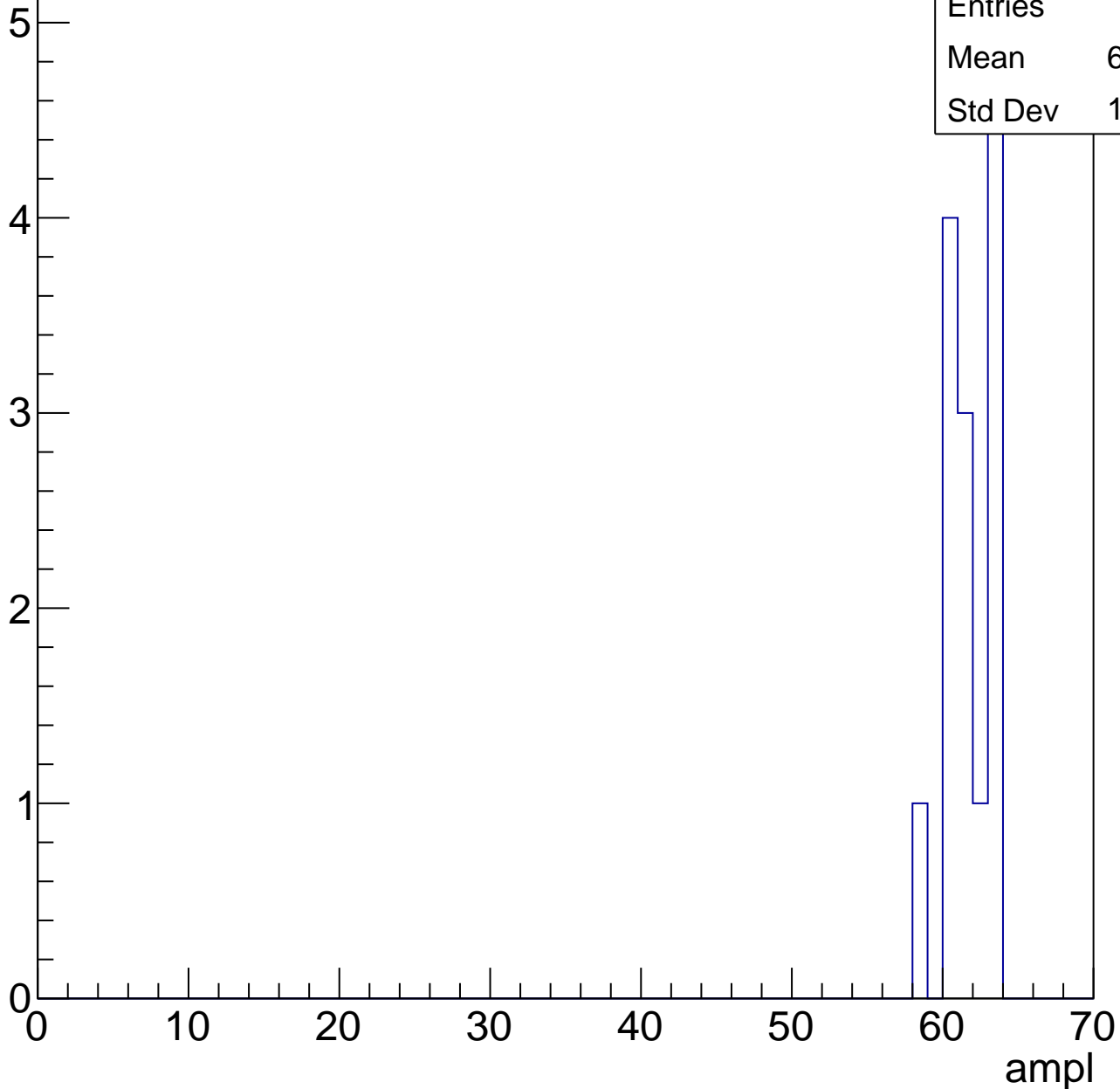


# B1L102S, U21-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	14
Mean	61.29
Std Dev	1.532

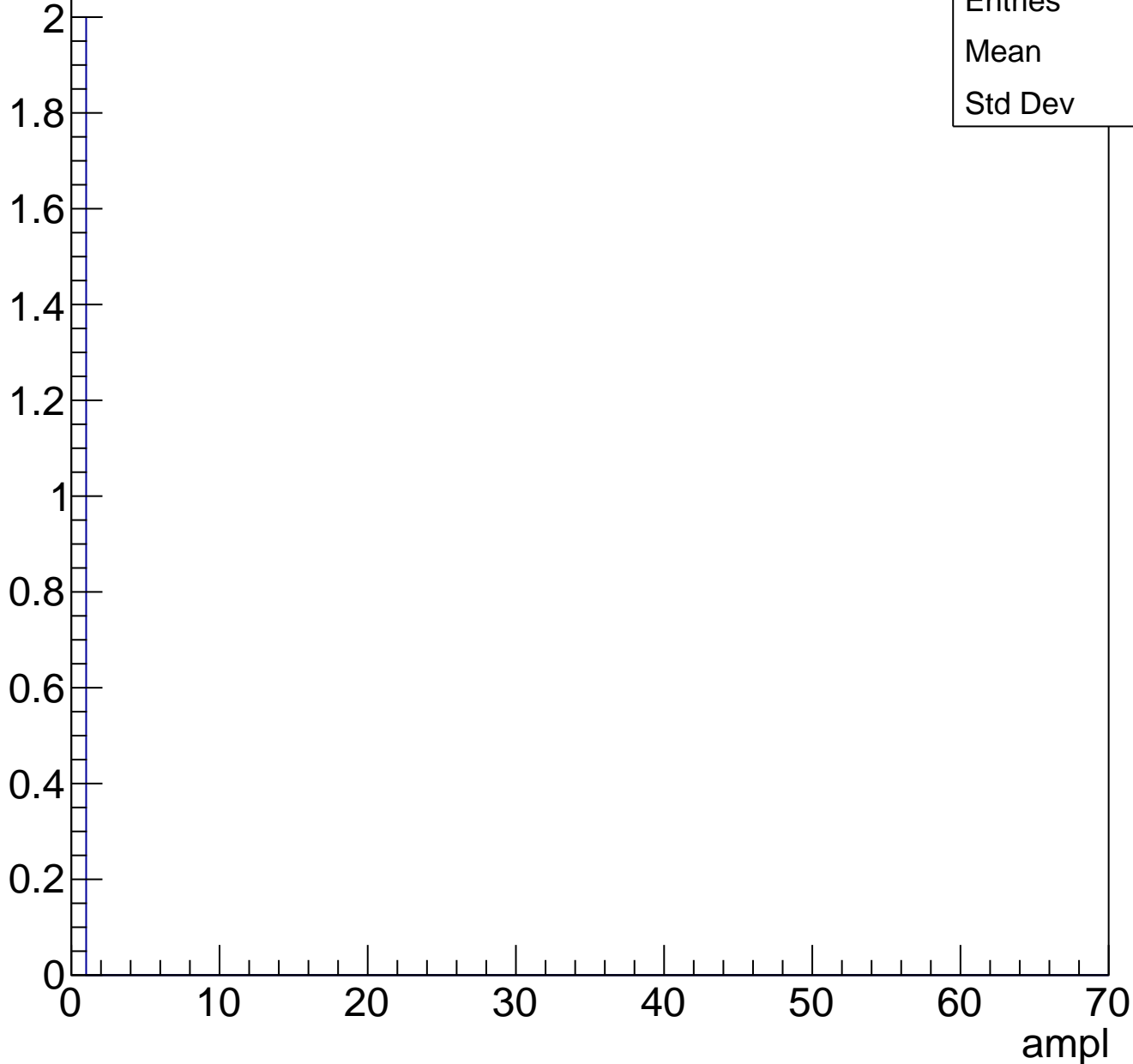




# B1L102S, U21-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch82, adc0

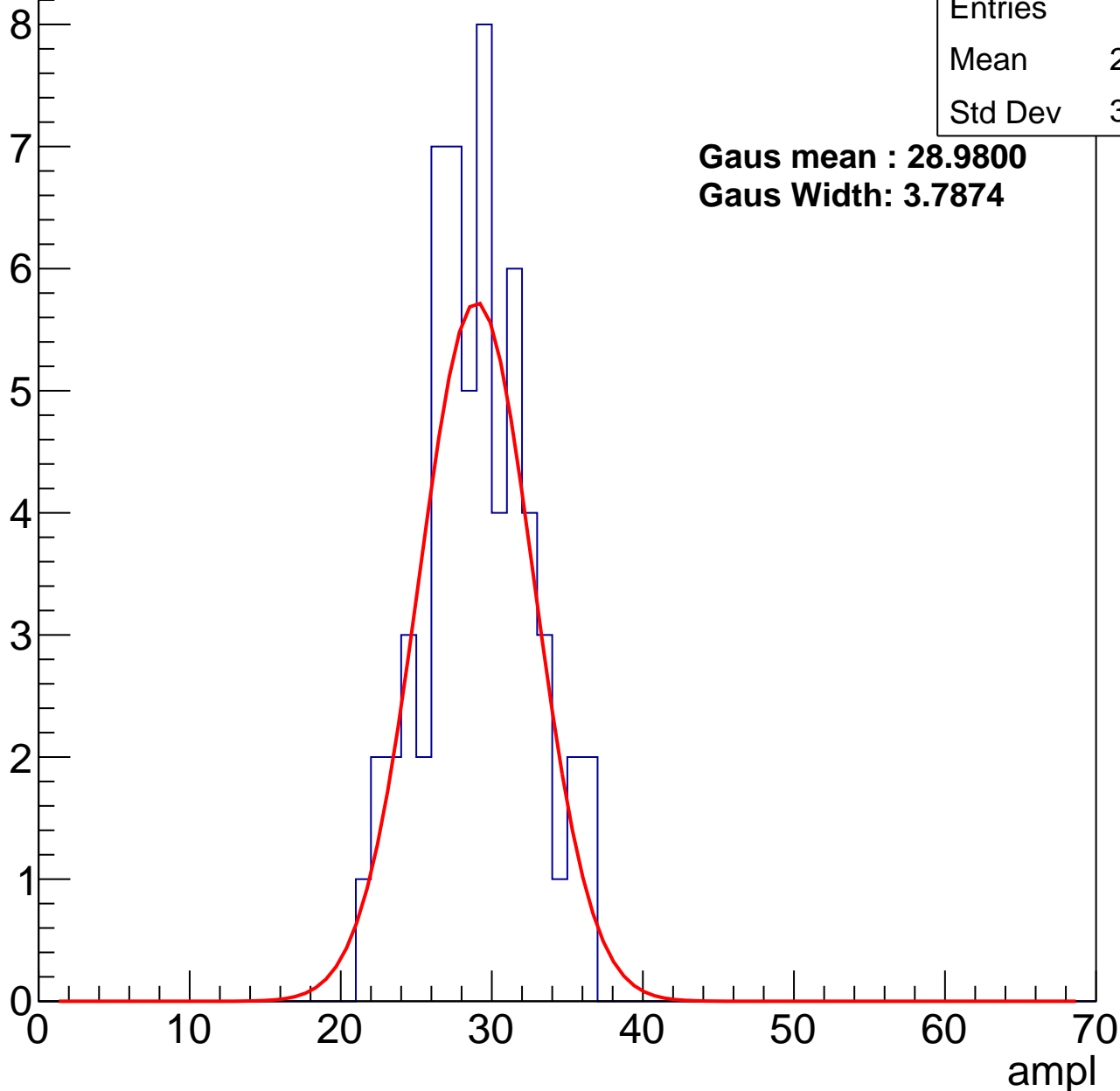
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	28.56
Std Dev	3.524

**Gaus mean : 28.9800**

**Gaus Width: 3.7874**



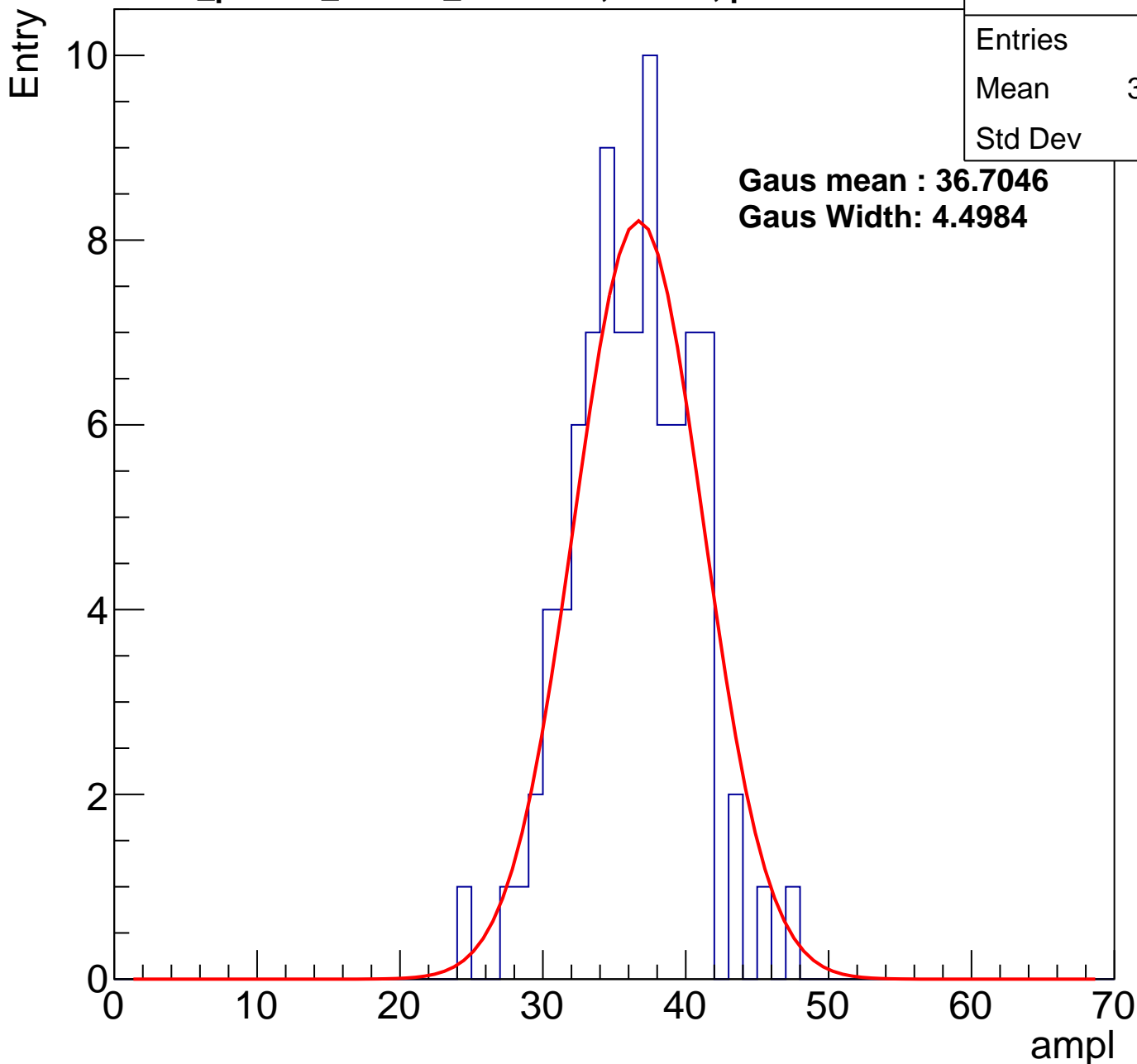
# B1L102S, U21-ch82, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	89
Mean	35.78
Std Dev	4.11

**Gaus mean : 36.7046**

**Gaus Width: 4.4984**



# B1L102S, U21-ch82, adc2

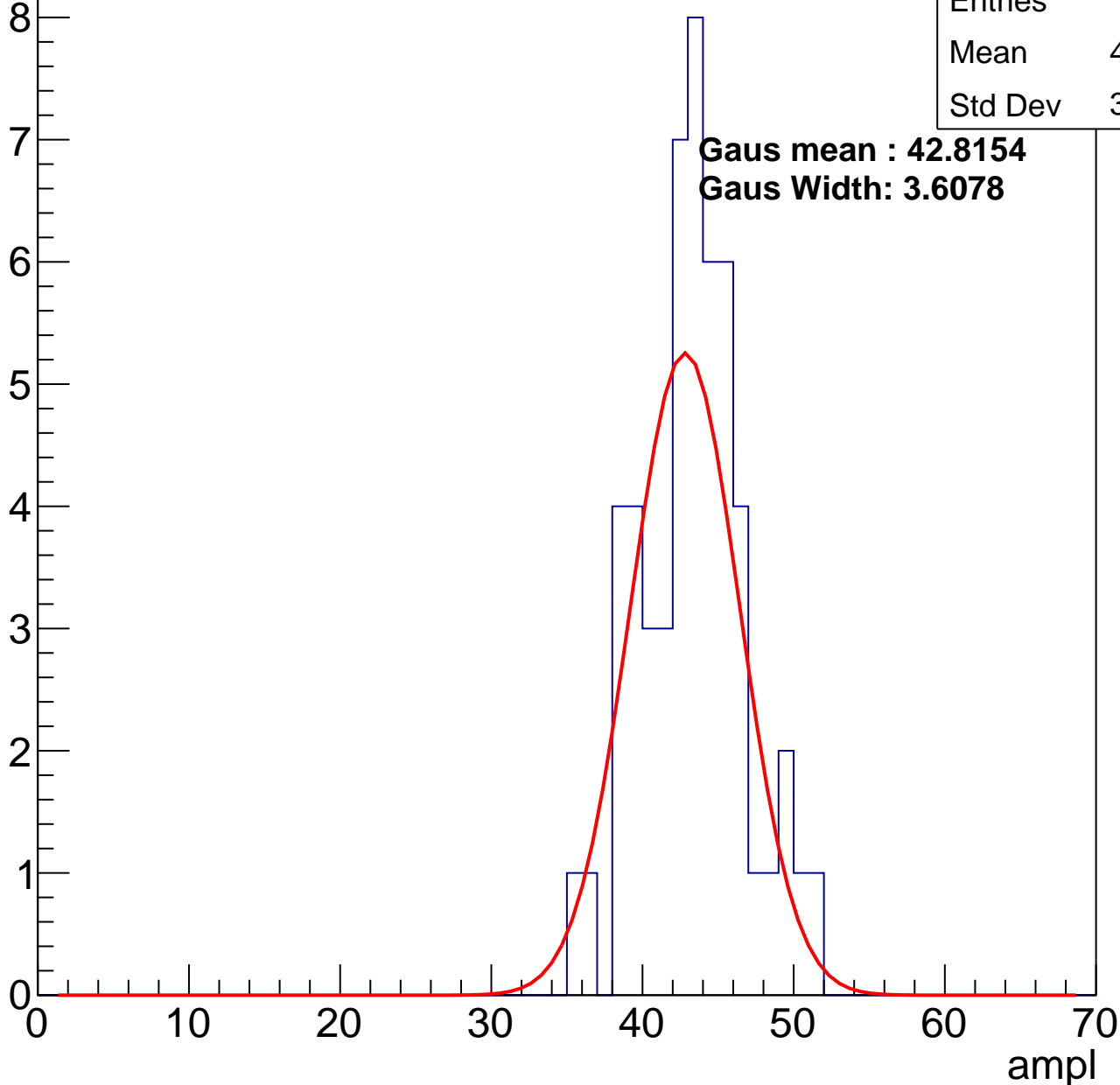
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	42.87
Std Dev	3.404

**Gaus mean : 42.8154**

**Gaus Width: 3.6078**

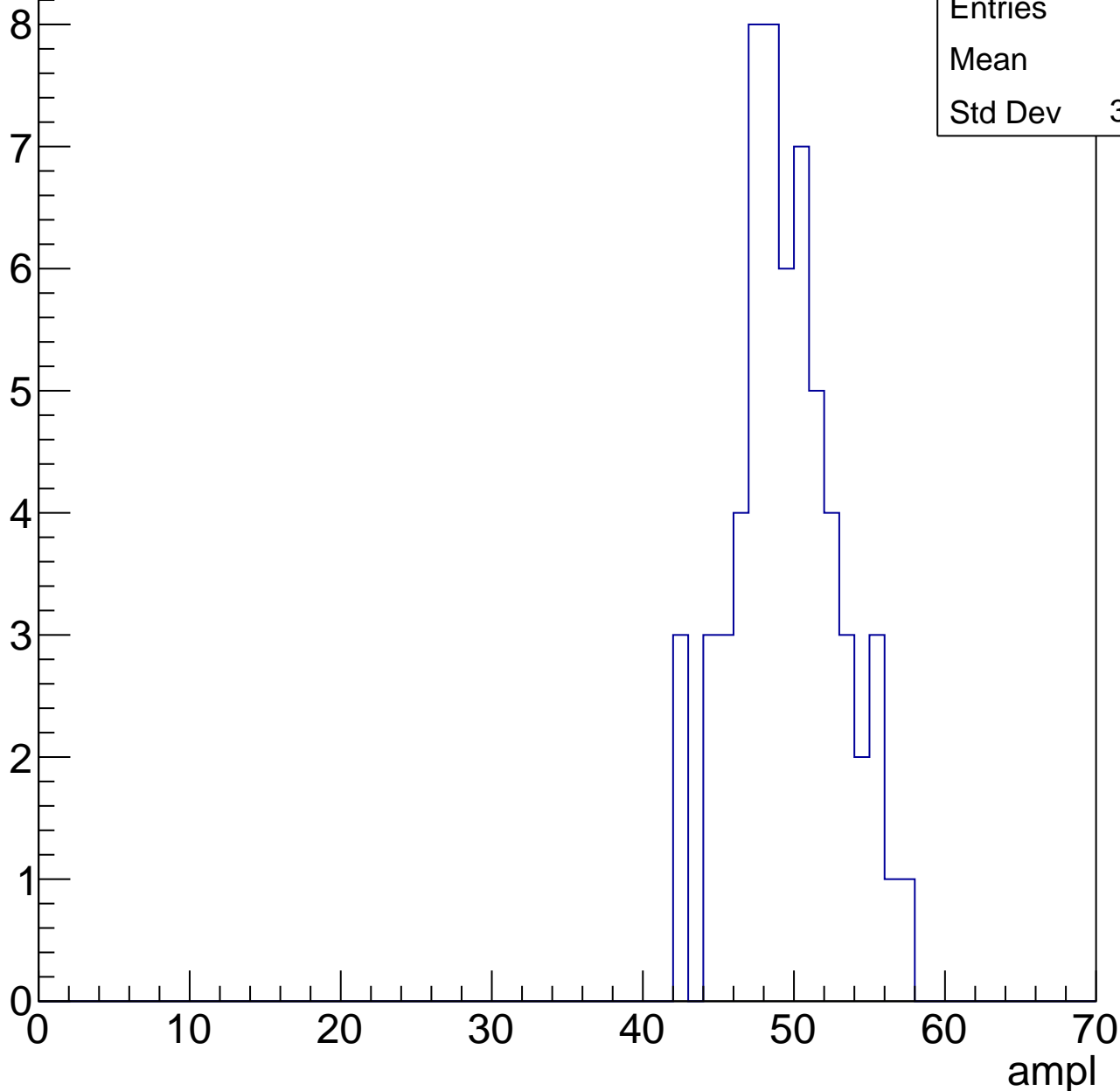


# B1L102S, U21-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	49
Std Dev	3.455

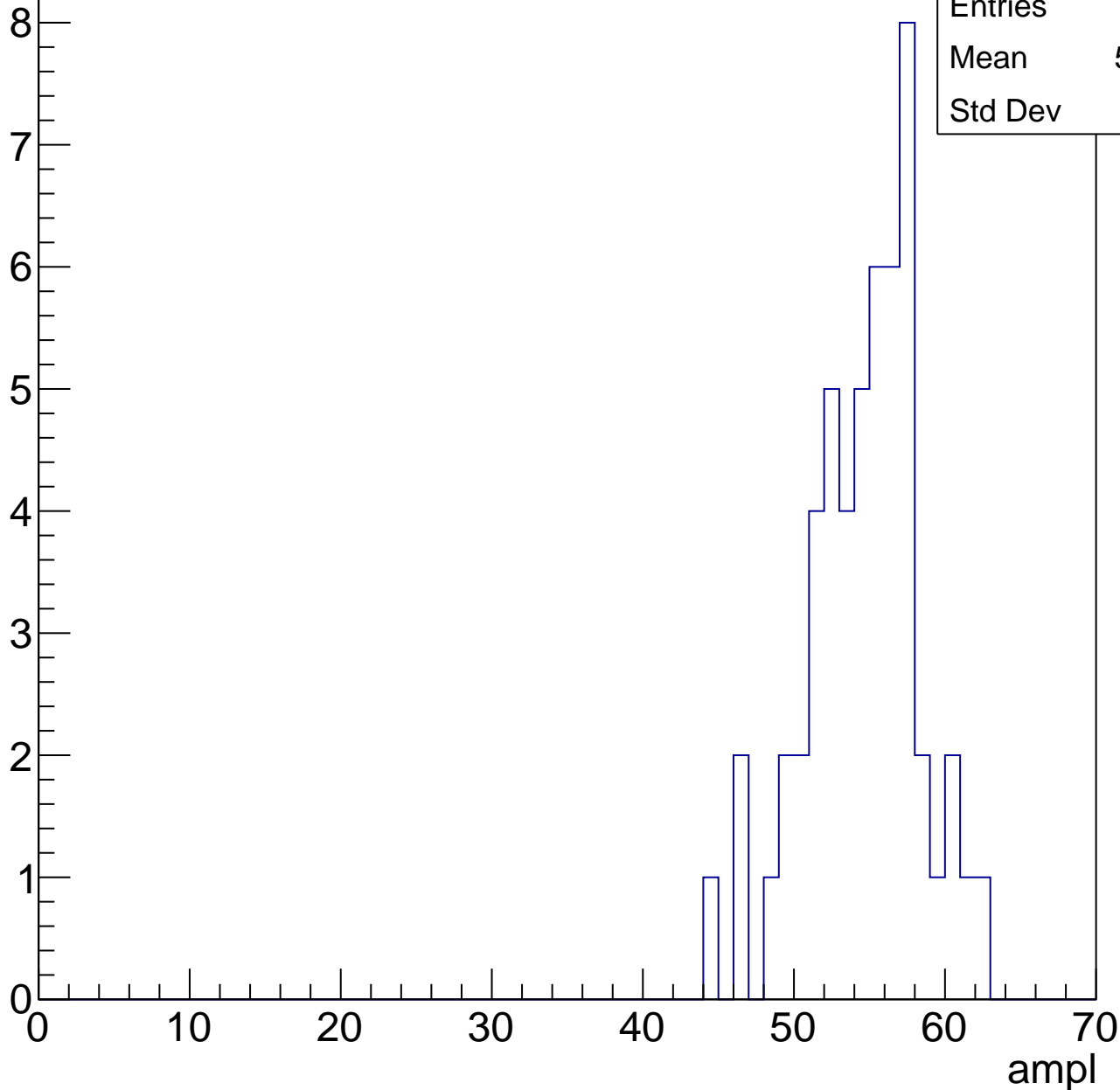


# B1L102S, U21-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	54.11
Std Dev	3.76

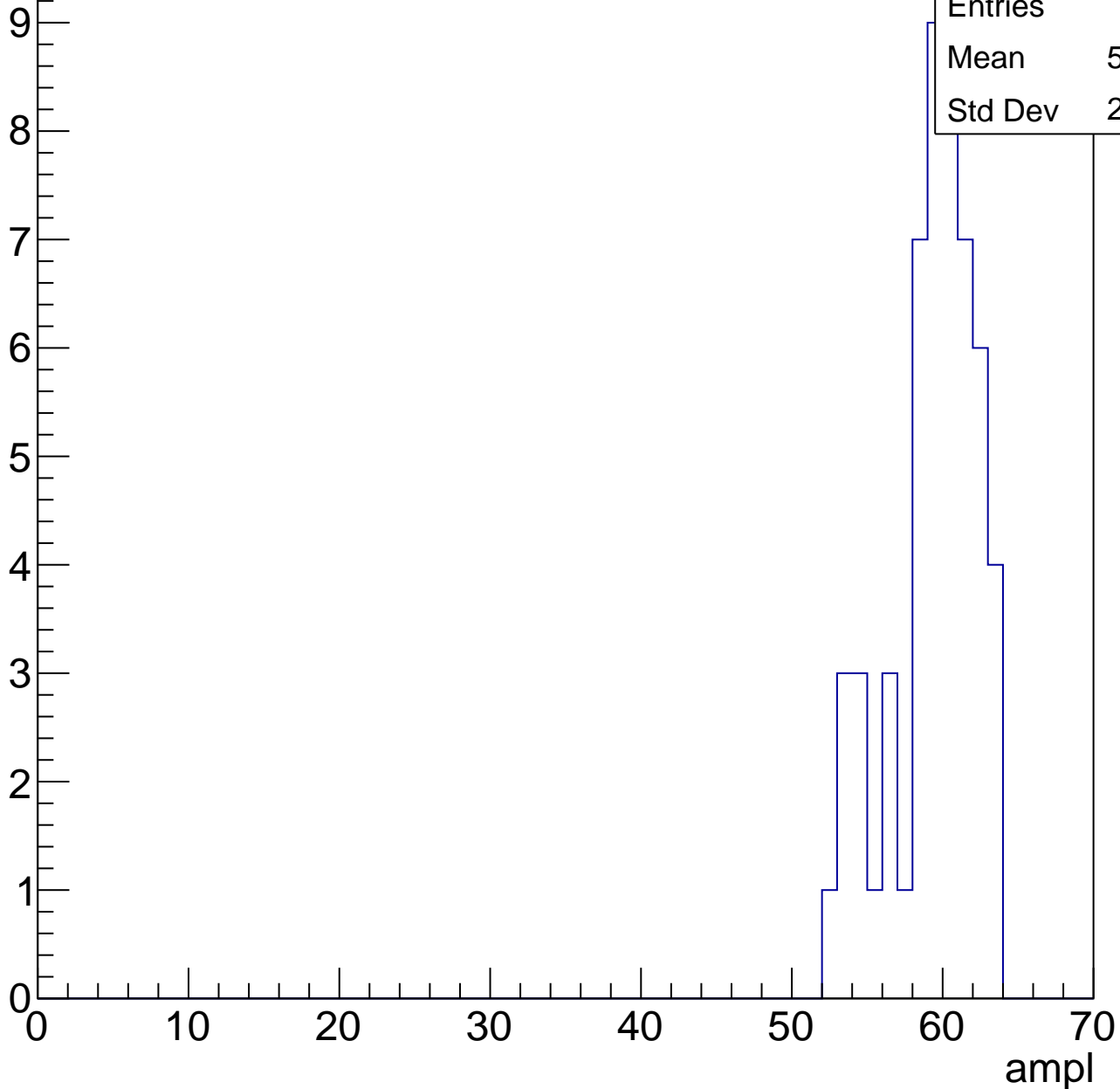


# B1L102S, U21-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	58.89
Std Dev	2.879

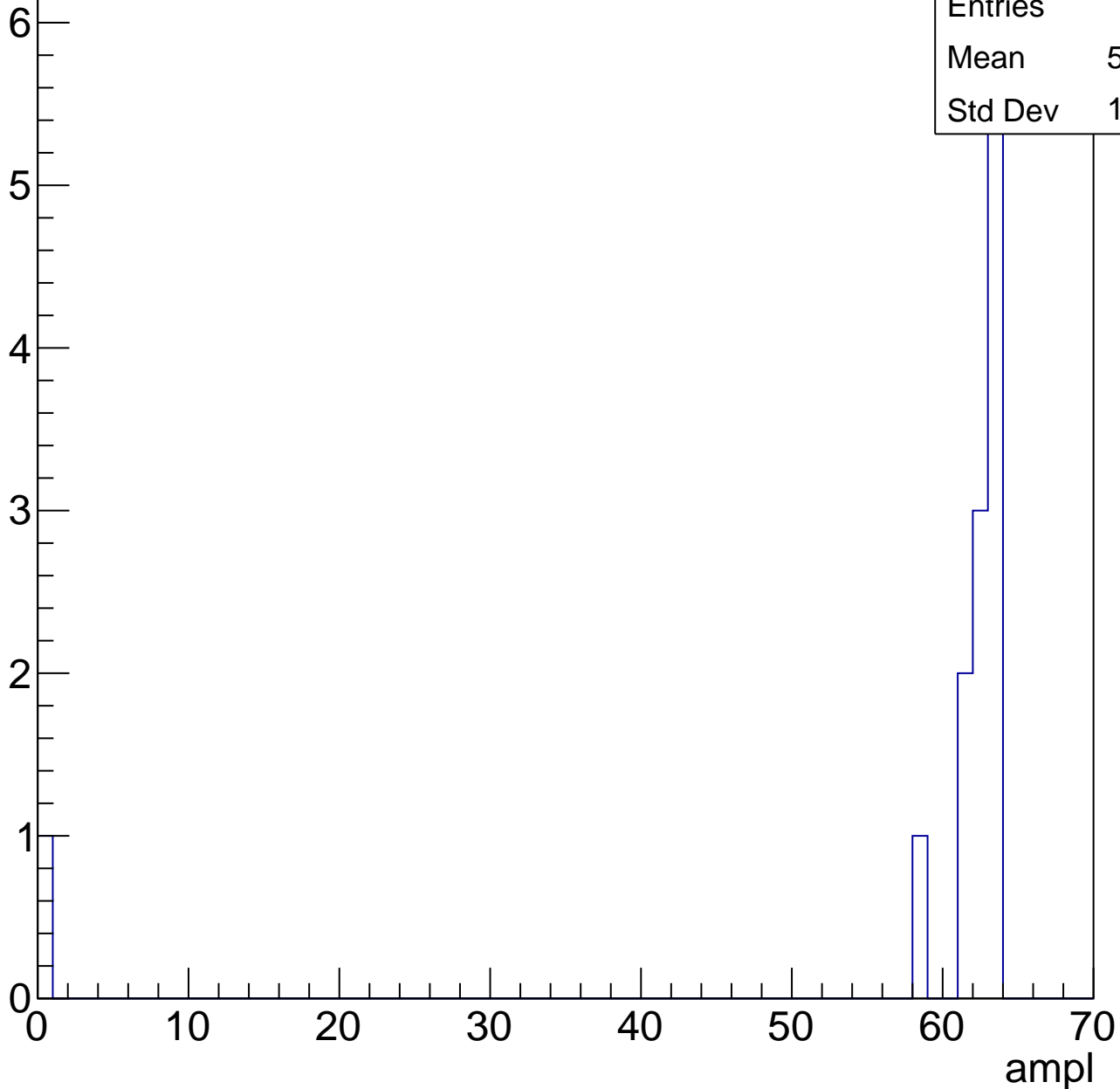


# B1L102S, U21-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	13
Mean	57.23
Std Dev	16.58





# B1L102S, U21-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	4
Mean	0
Std Dev	0

# B1L102S, U21-ch83, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	87
Mean	28.52
Std Dev	5.795

**Gaus mean : 29.8231**

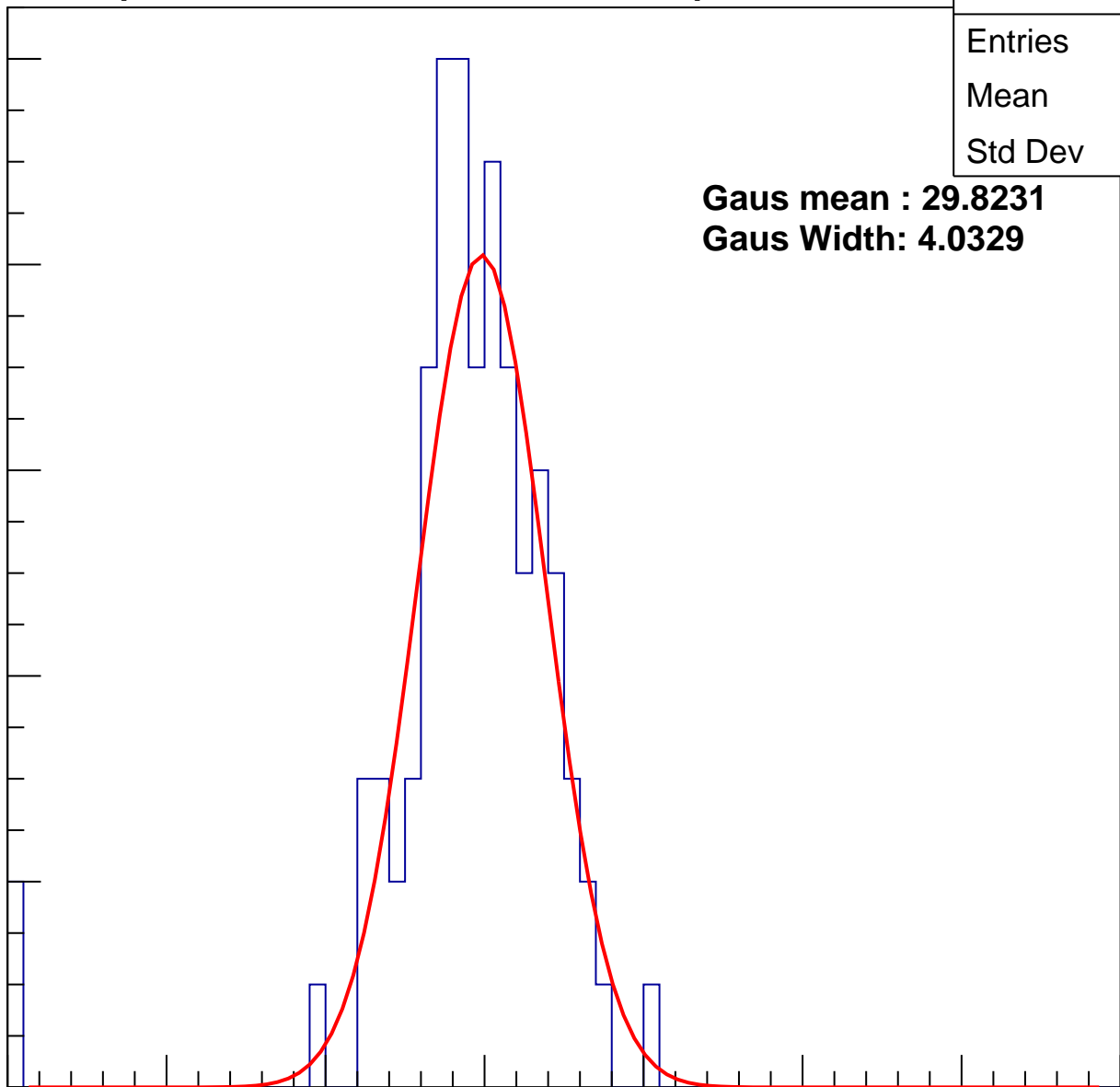
**Gaus Width: 4.0329**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U21-ch83, adc1

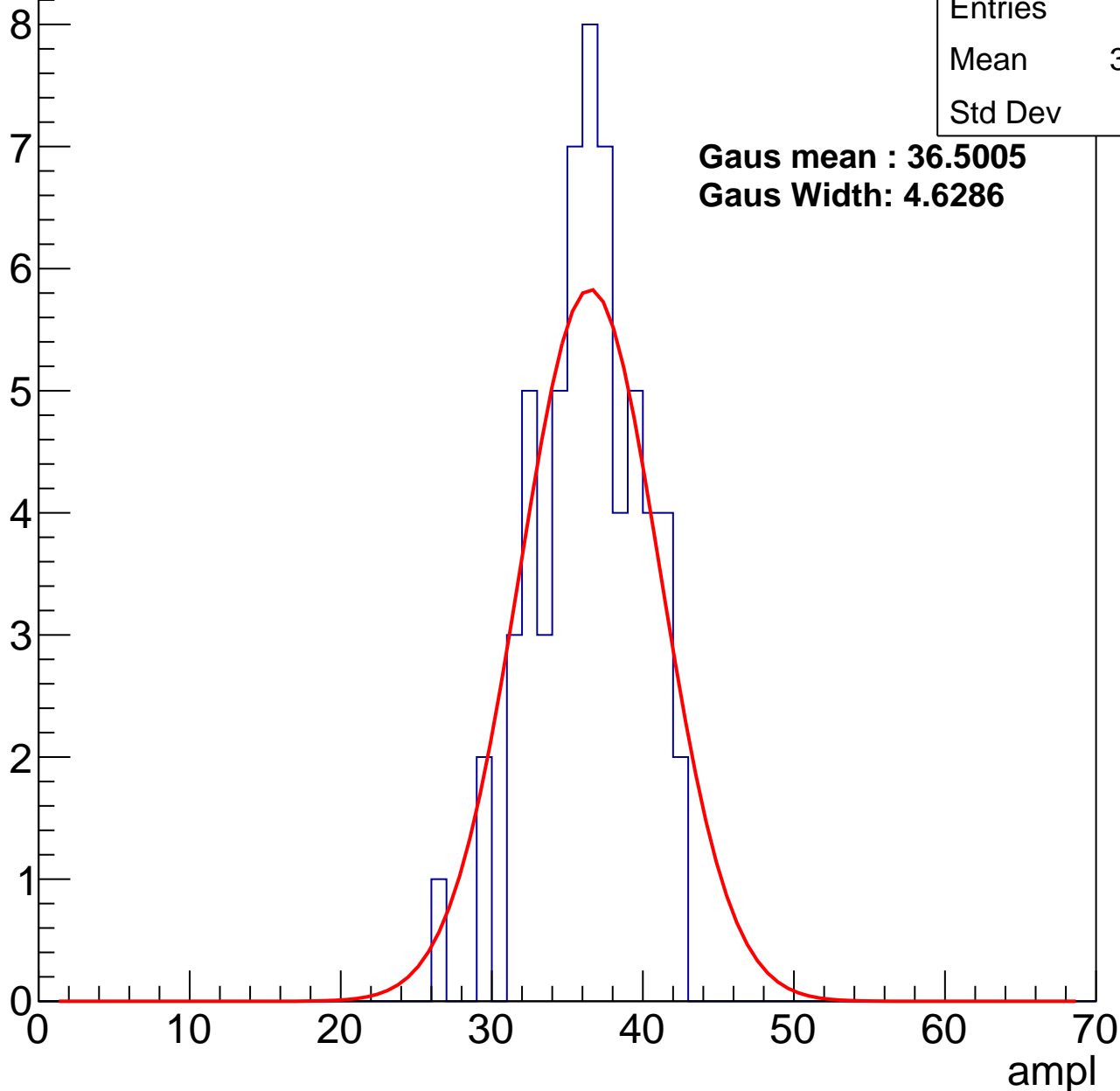
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	35.88
Std Dev	3.44

**Gaus mean : 36.5005**

**Gaus Width: 4.6286**



# B1L102S, U21-ch83, adc2

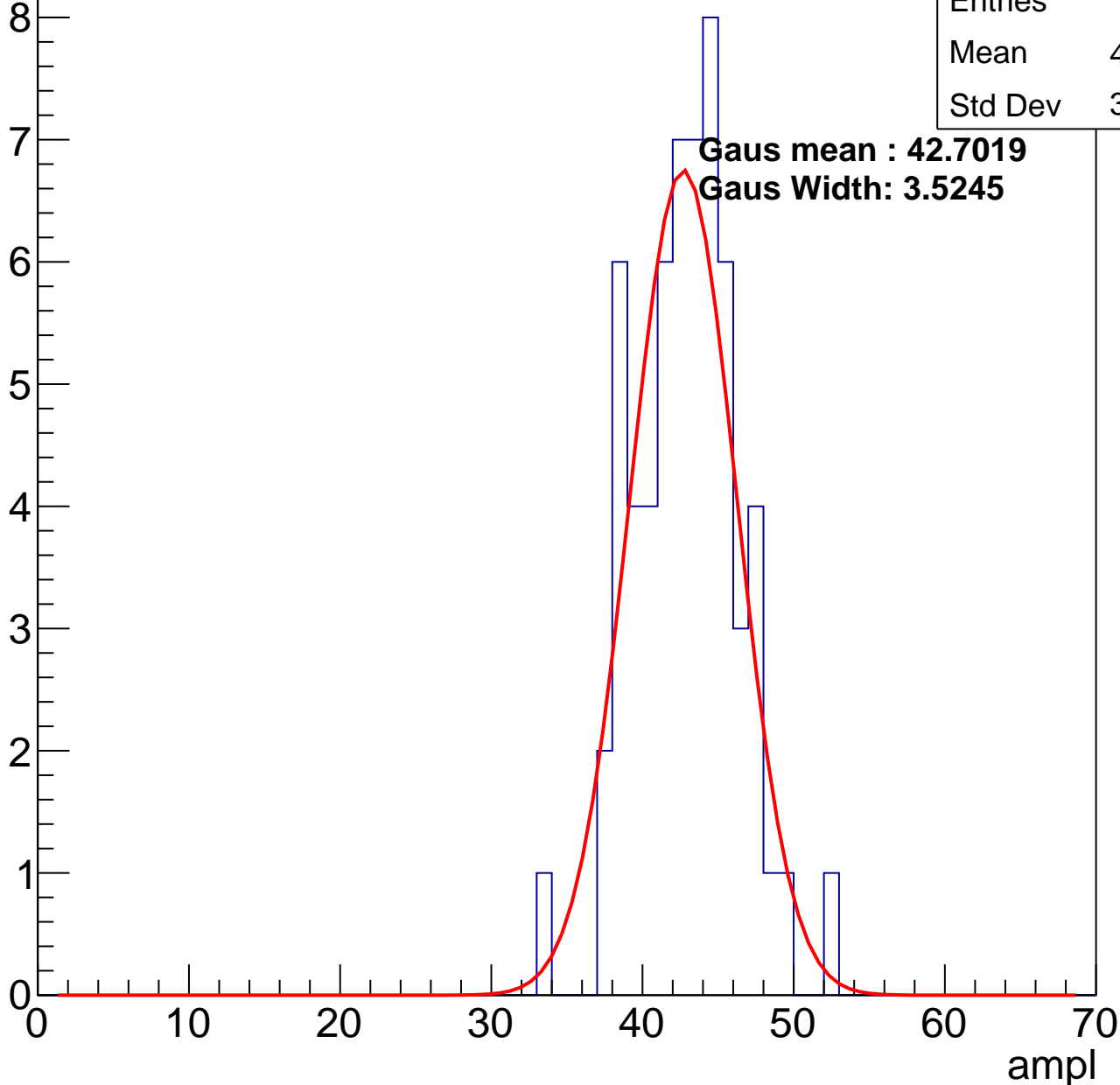
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	42.44
Std Dev	3.385

**Gaus mean : 42.7019**

**Gaus Width: 3.5245**

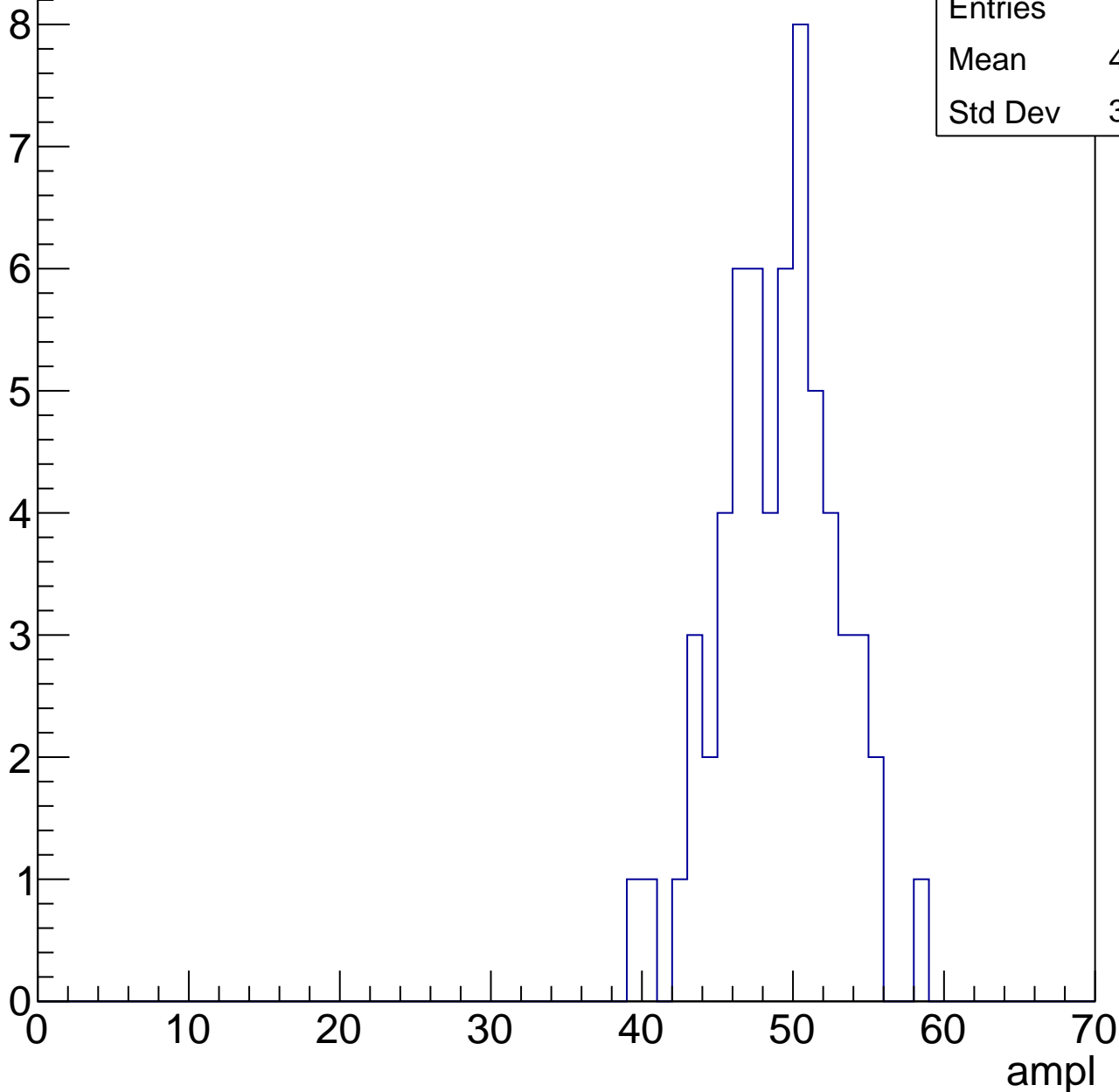


# B1L102S, U21-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

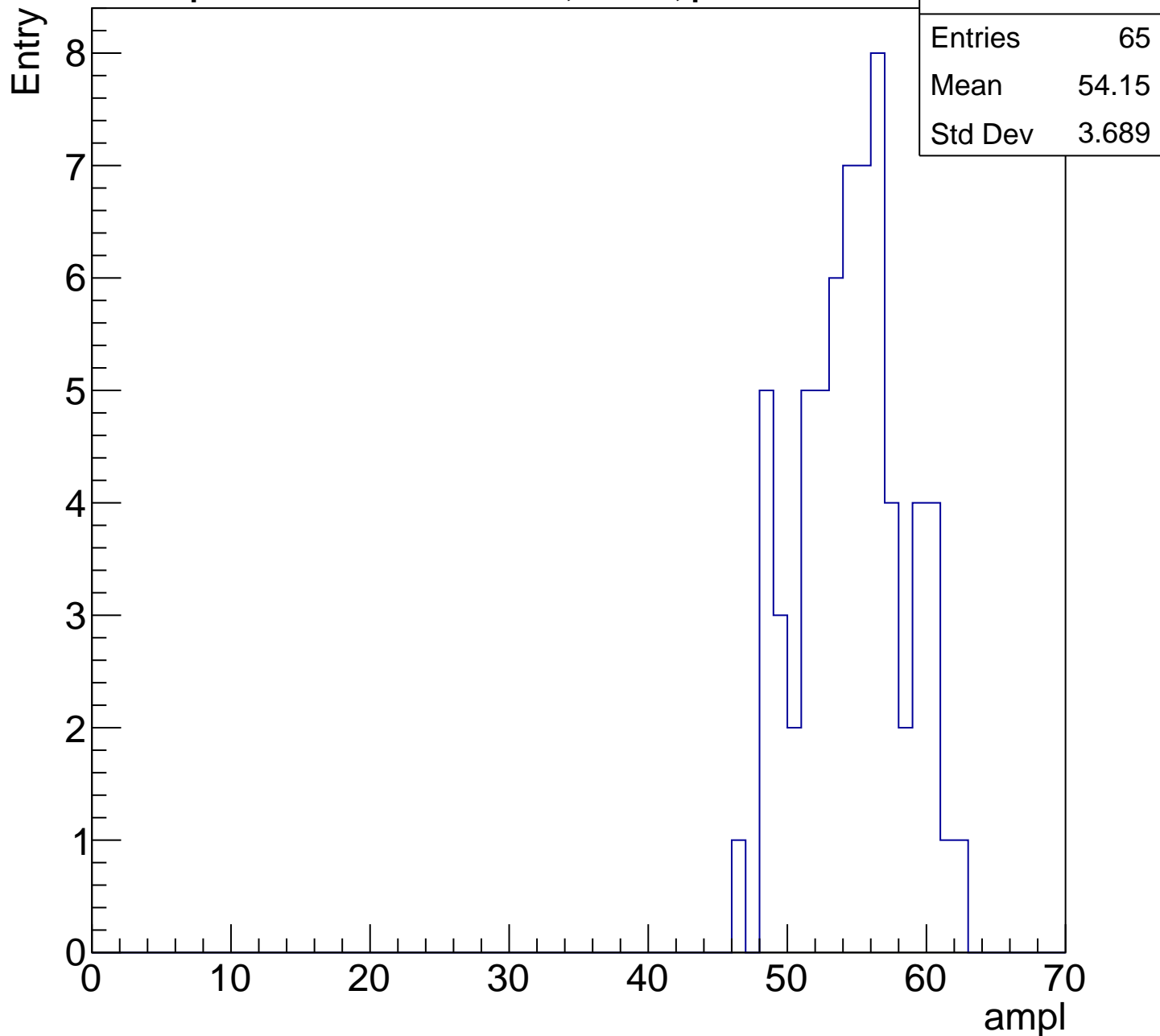
Entry

Entries	60
Mean	48.57
Std Dev	3.792



# B1L102S, U21-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

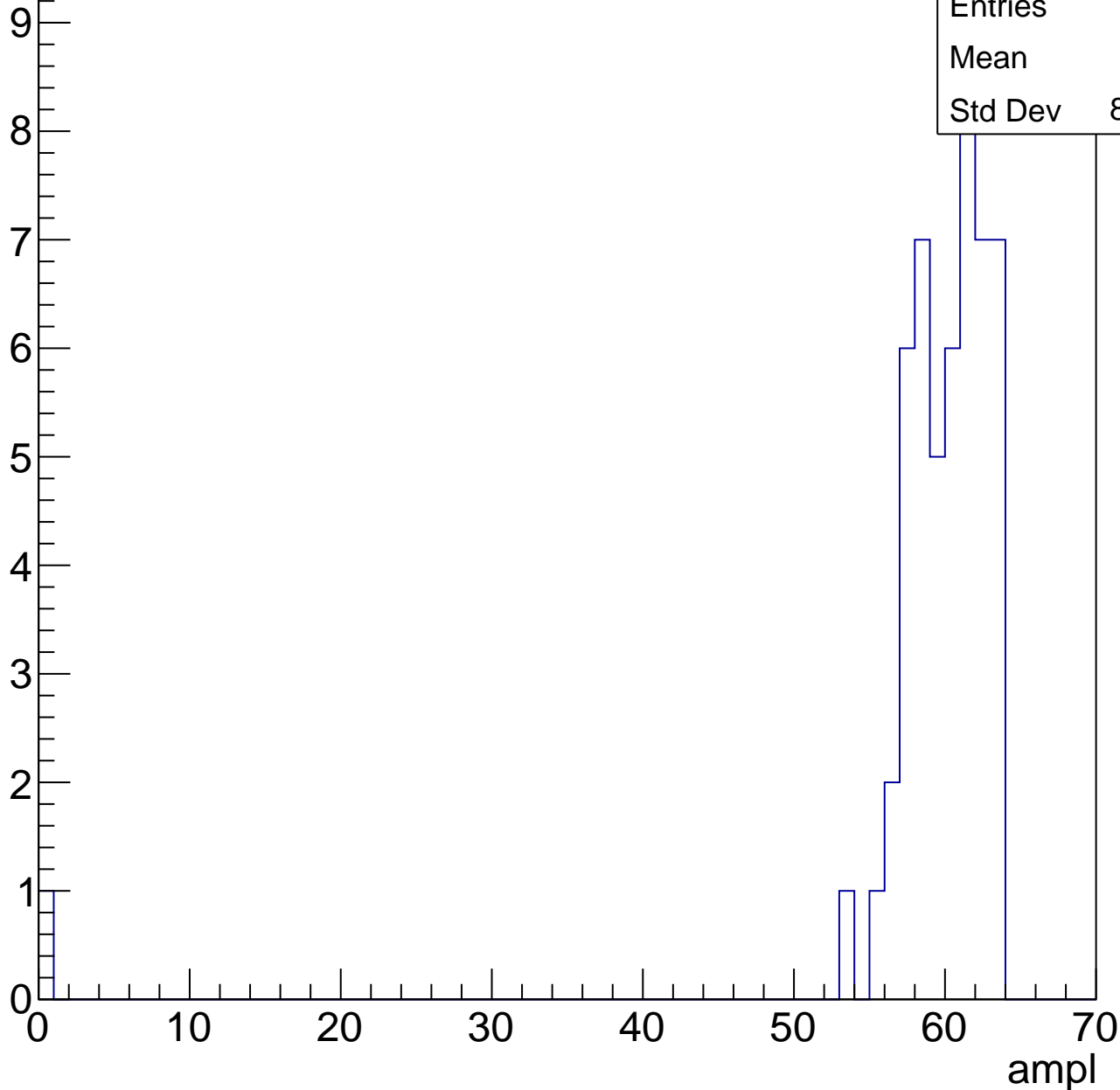


# B1L102S, U21-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	58.6
Std Dev	8.538



# B1L102S, U21-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U21-ch84, adc0

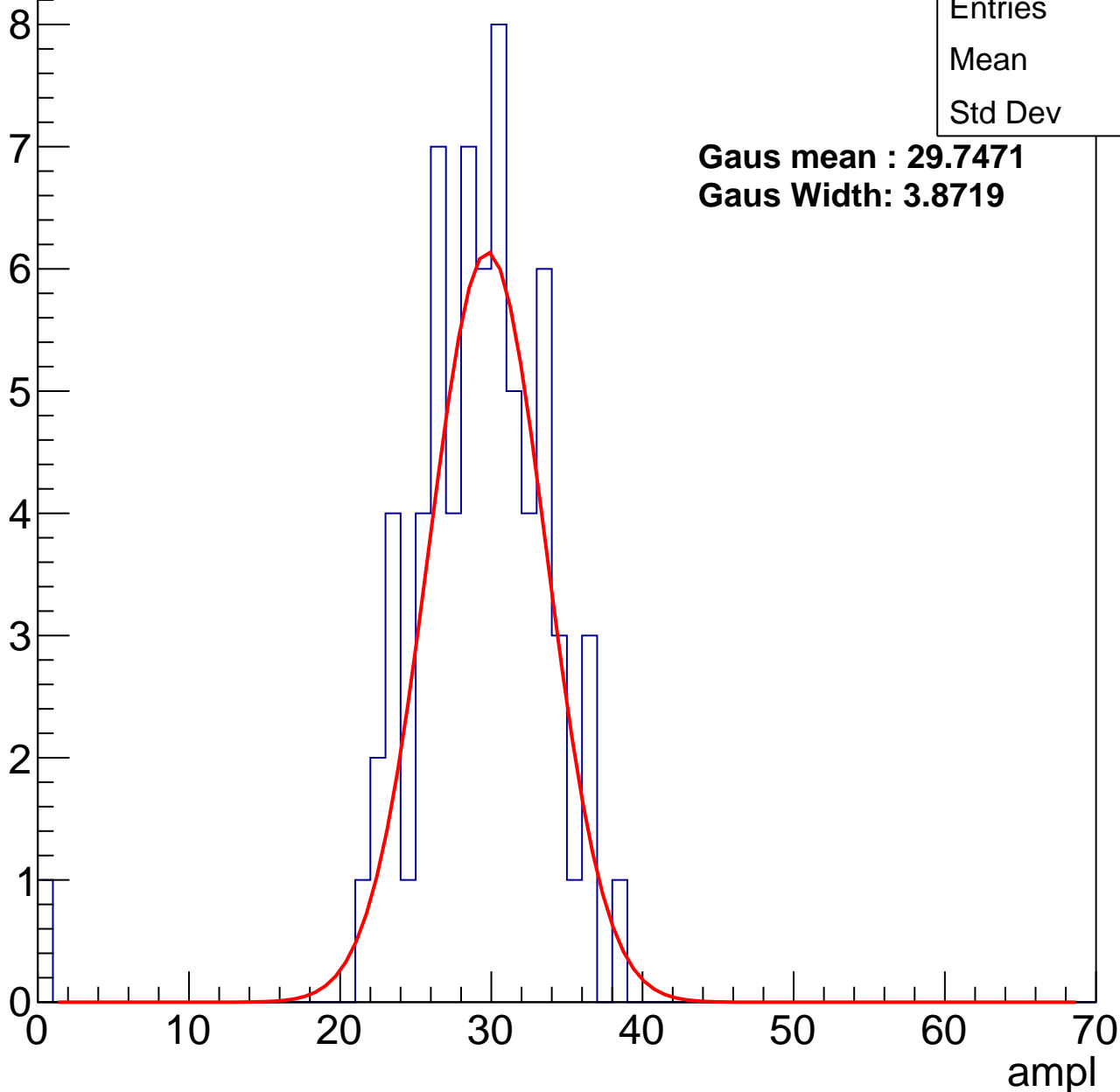
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	28.6
Std Dev	5.16

**Gaus mean : 29.7471**

**Gaus Width: 3.8719**



# B1L102S, U21-ch84, adc1

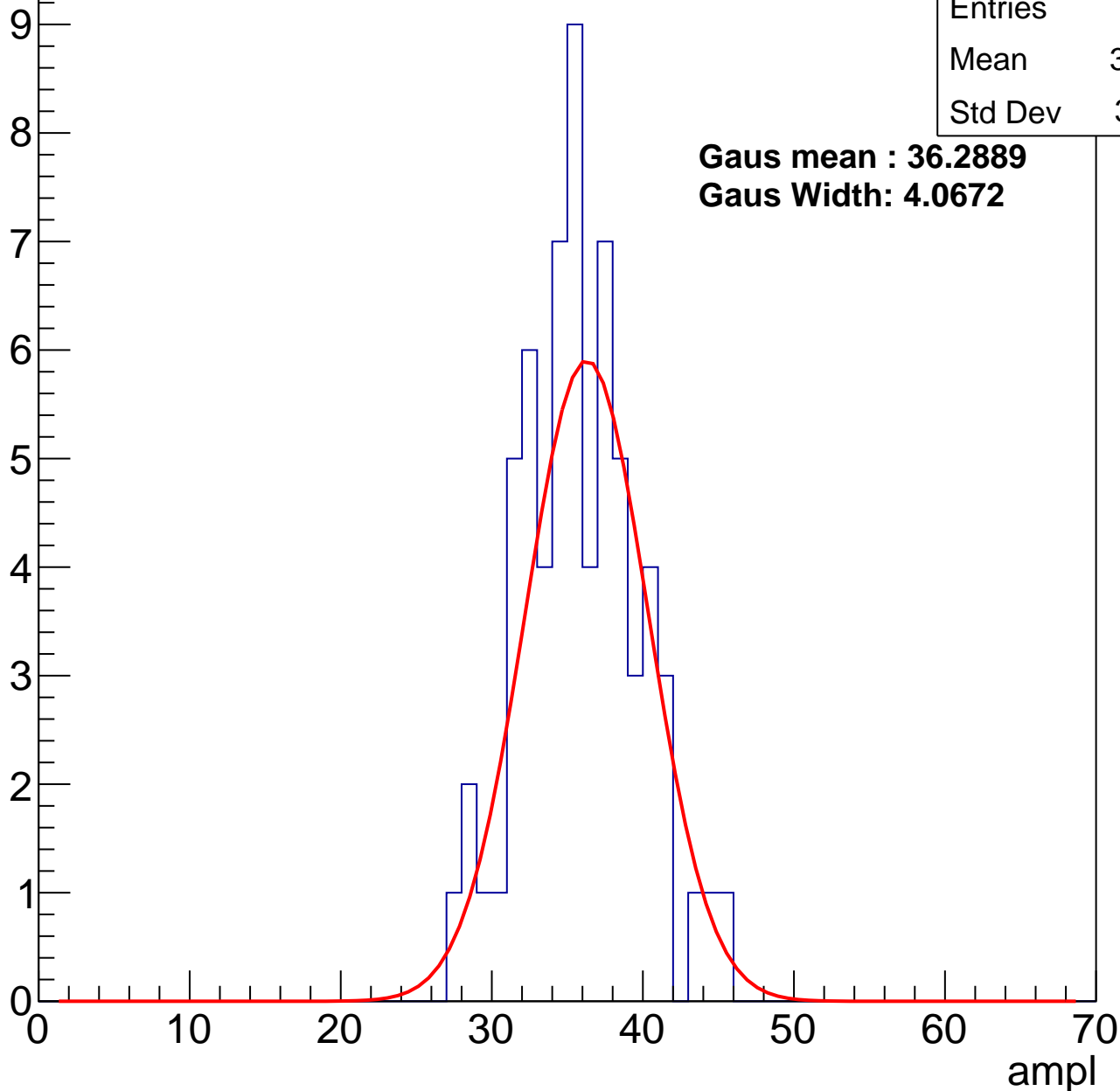
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	35.37
Std Dev	3.821

**Gaus mean : 36.2889**

**Gaus Width: 4.0672**



# B1L102S, U21-ch84, adc2

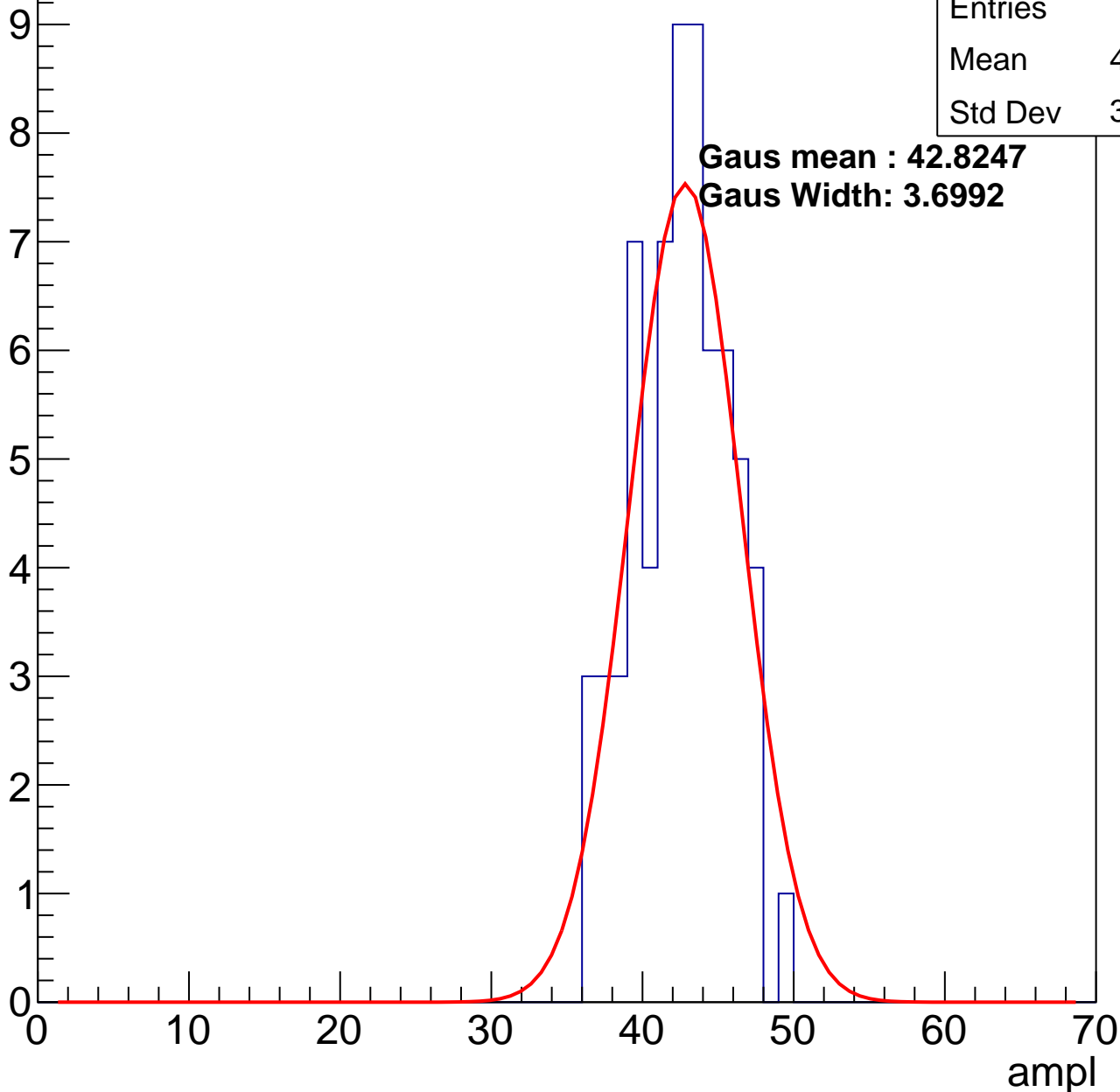
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	42.07
Std Dev	3.073

**Gaus mean : 42.8247**

**Gaus Width: 3.6992**

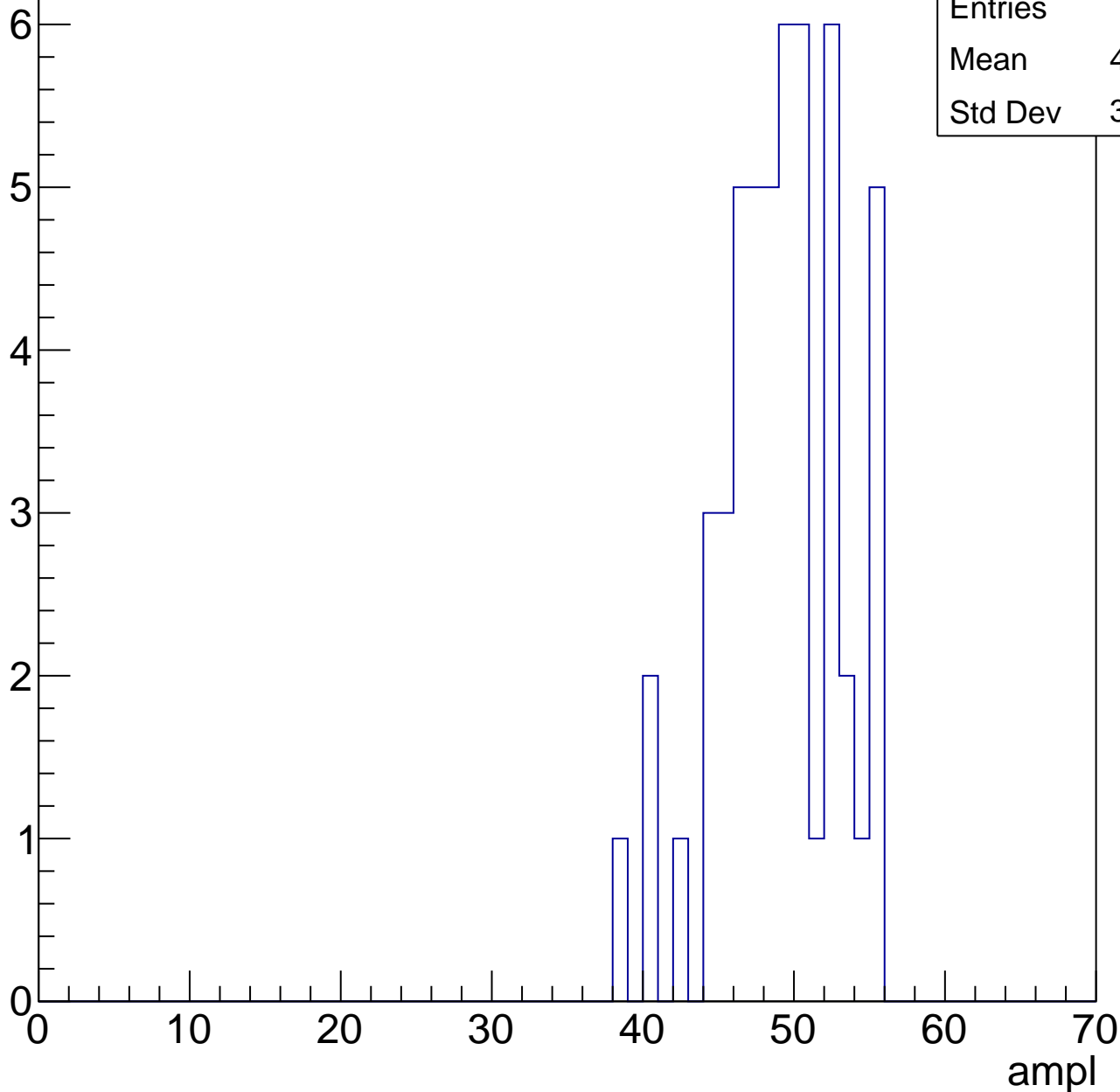


# B1L102S, U21-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	48.54
Std Dev	3.959

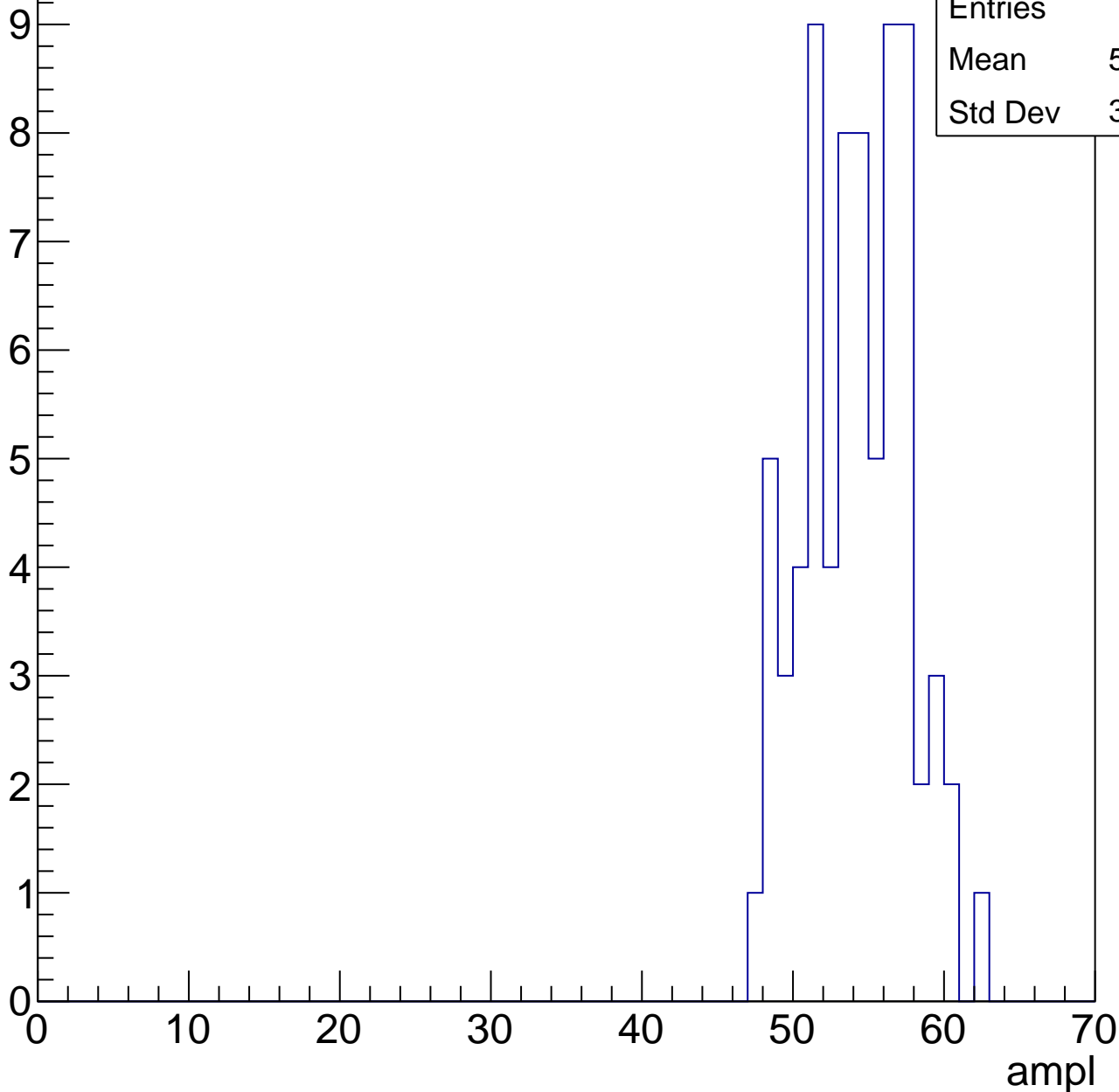


# B1L102S, U21-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	53.75
Std Dev	3.379

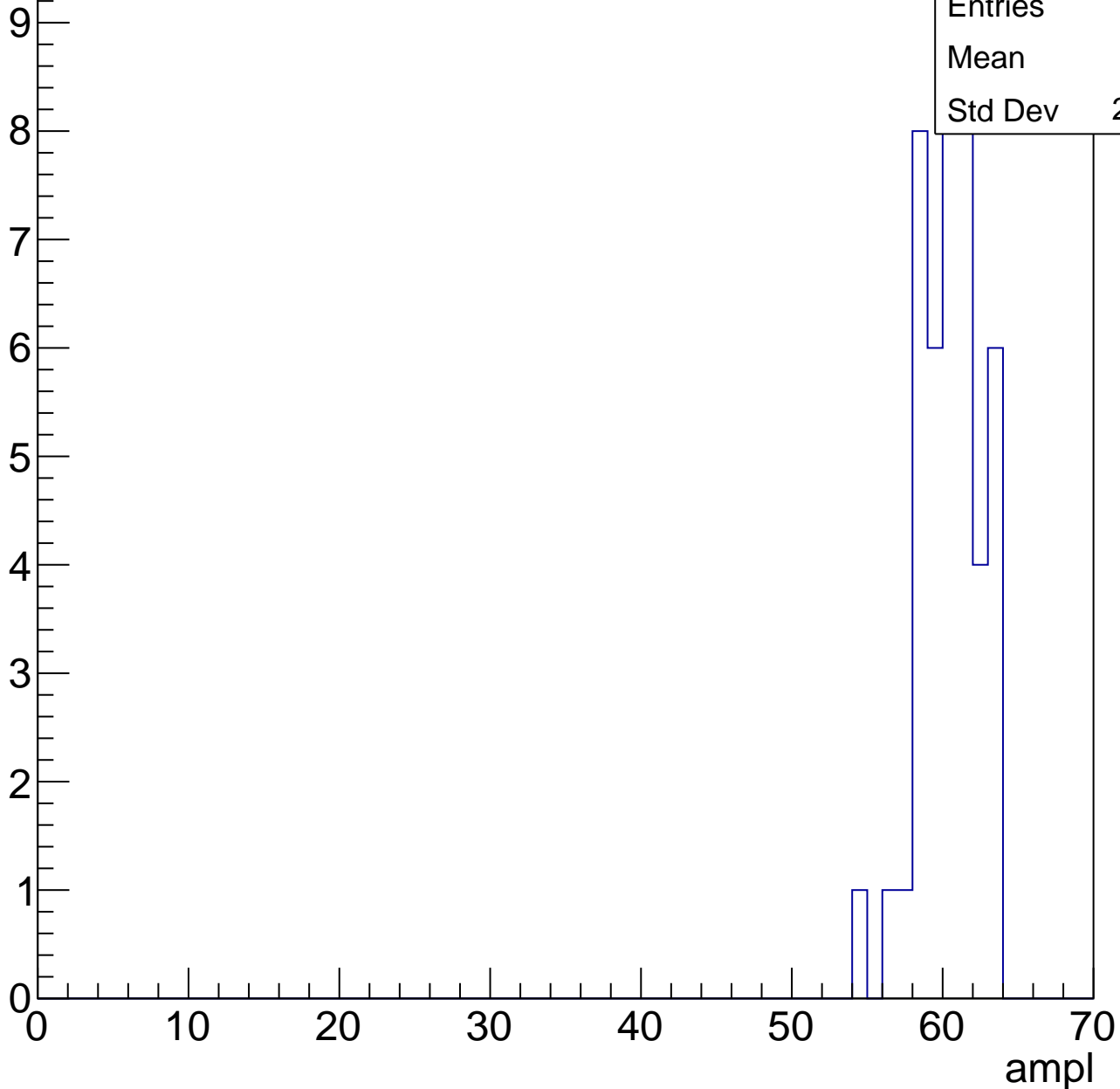


# B1L102S, U21-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	44
Mean	60
Std Dev	2.011

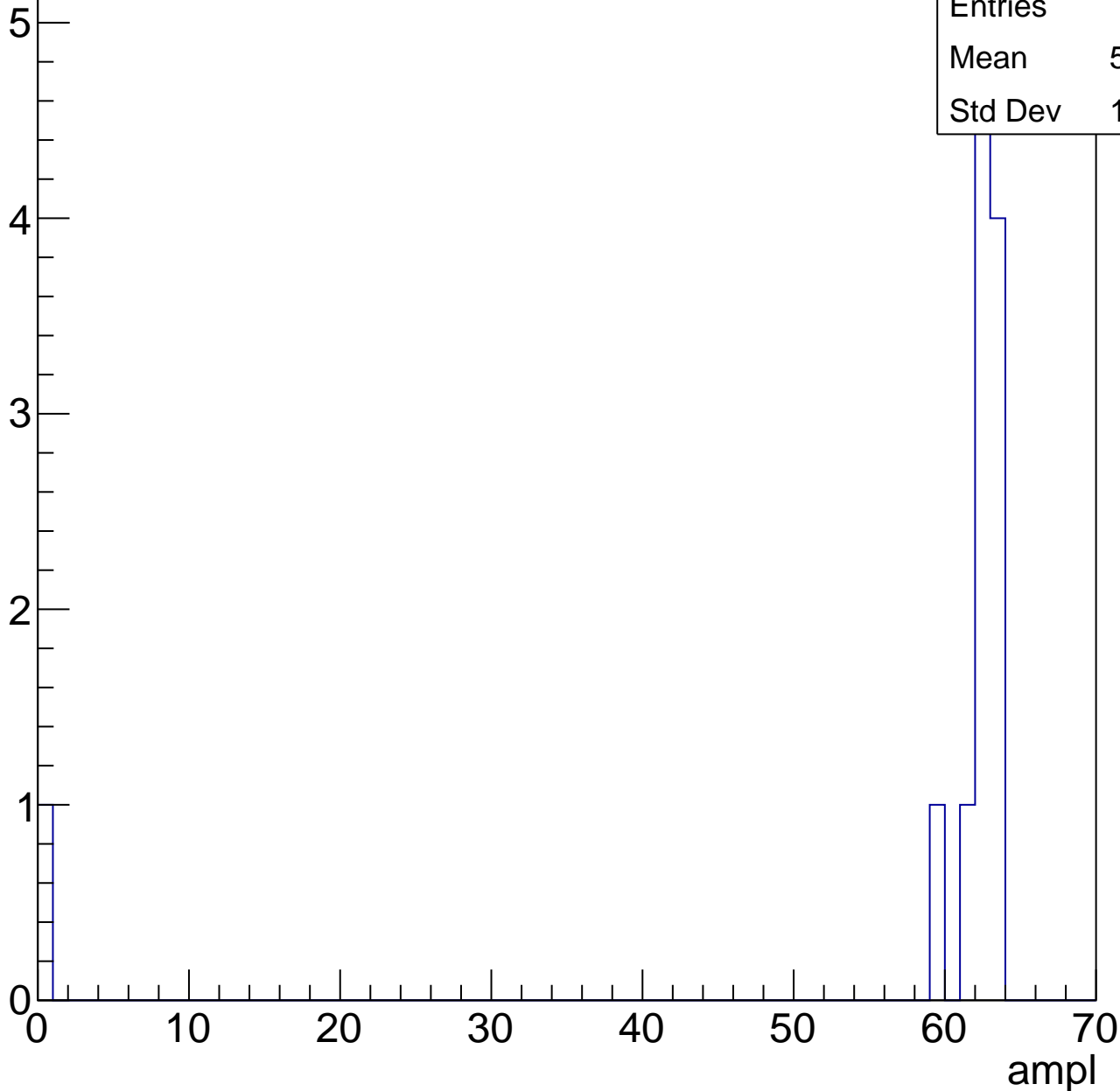


# B1L102S, U21-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	12
Mean	56.83
Std Dev	17.17





# B1L102S, U21-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	9.5
Std Dev	9.5

# B1L102S, U21-ch85, adc0

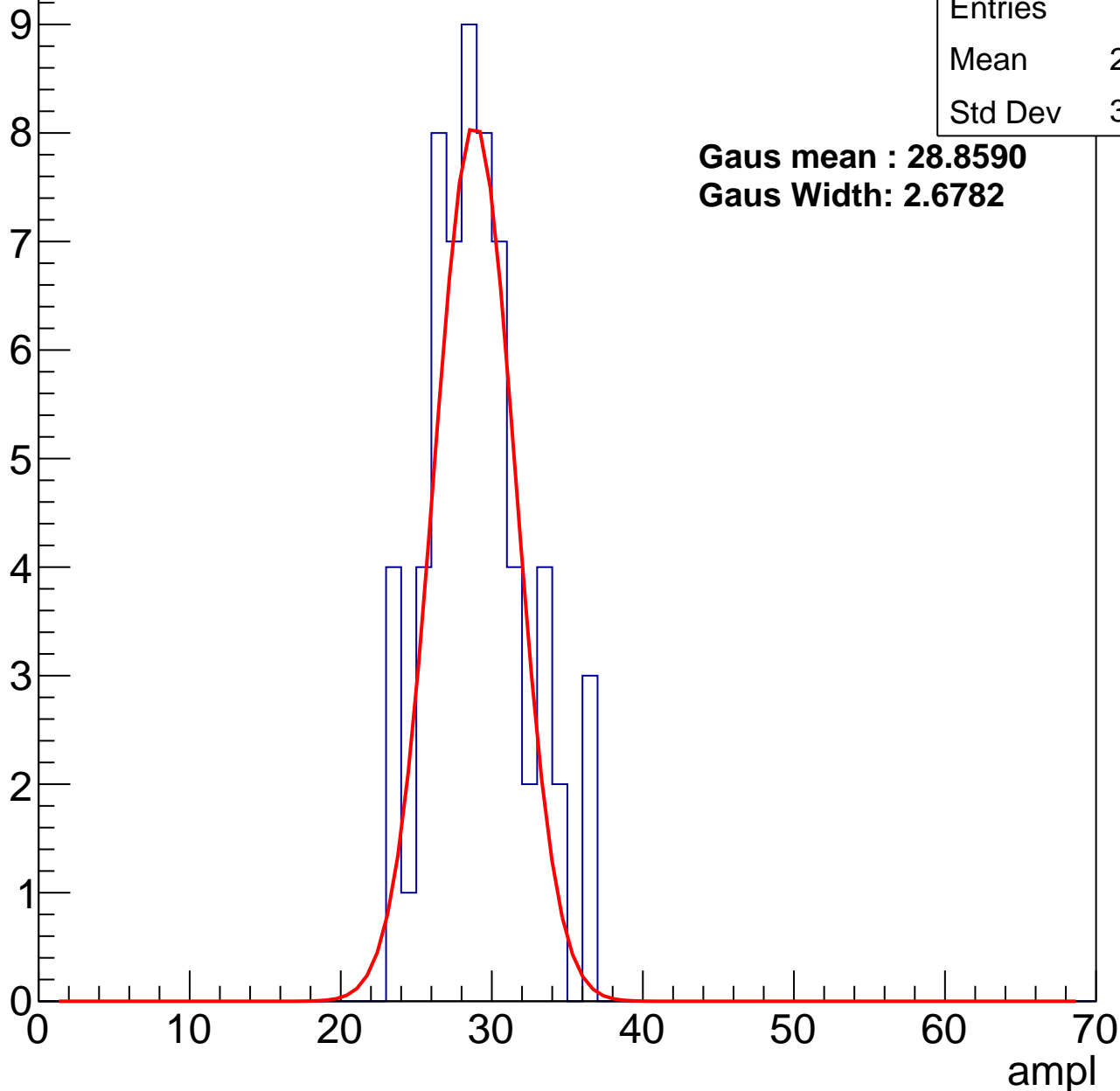
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	28.62
Std Dev	3.174

**Gaus mean : 28.8590**

**Gaus Width: 2.6782**



# B1L102S, U21-ch85, adc1

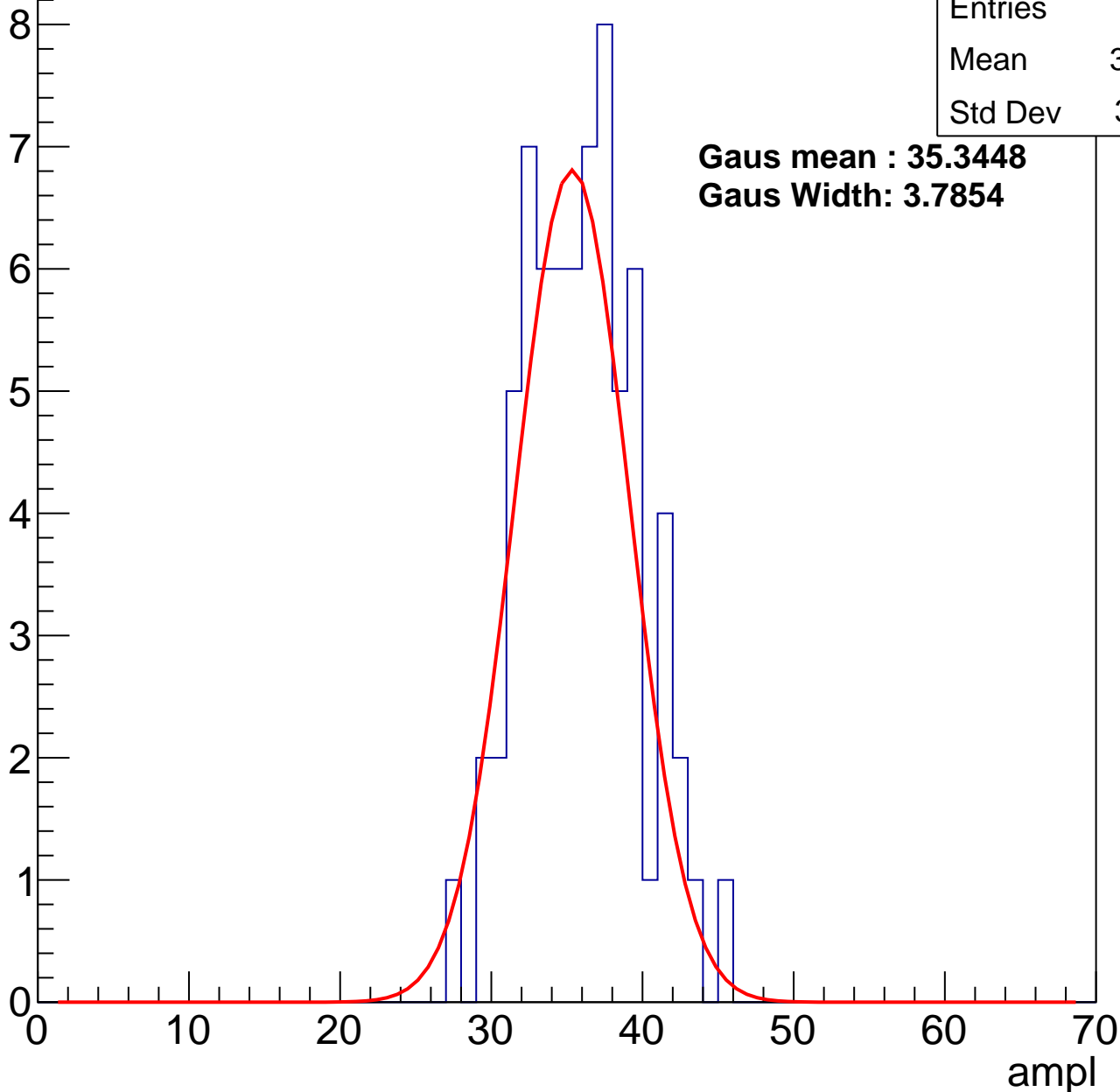
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	35.49
Std Dev	3.691

**Gaus mean : 35.3448**

**Gaus Width: 3.7854**



# B1L102S, U21-ch85, adc2

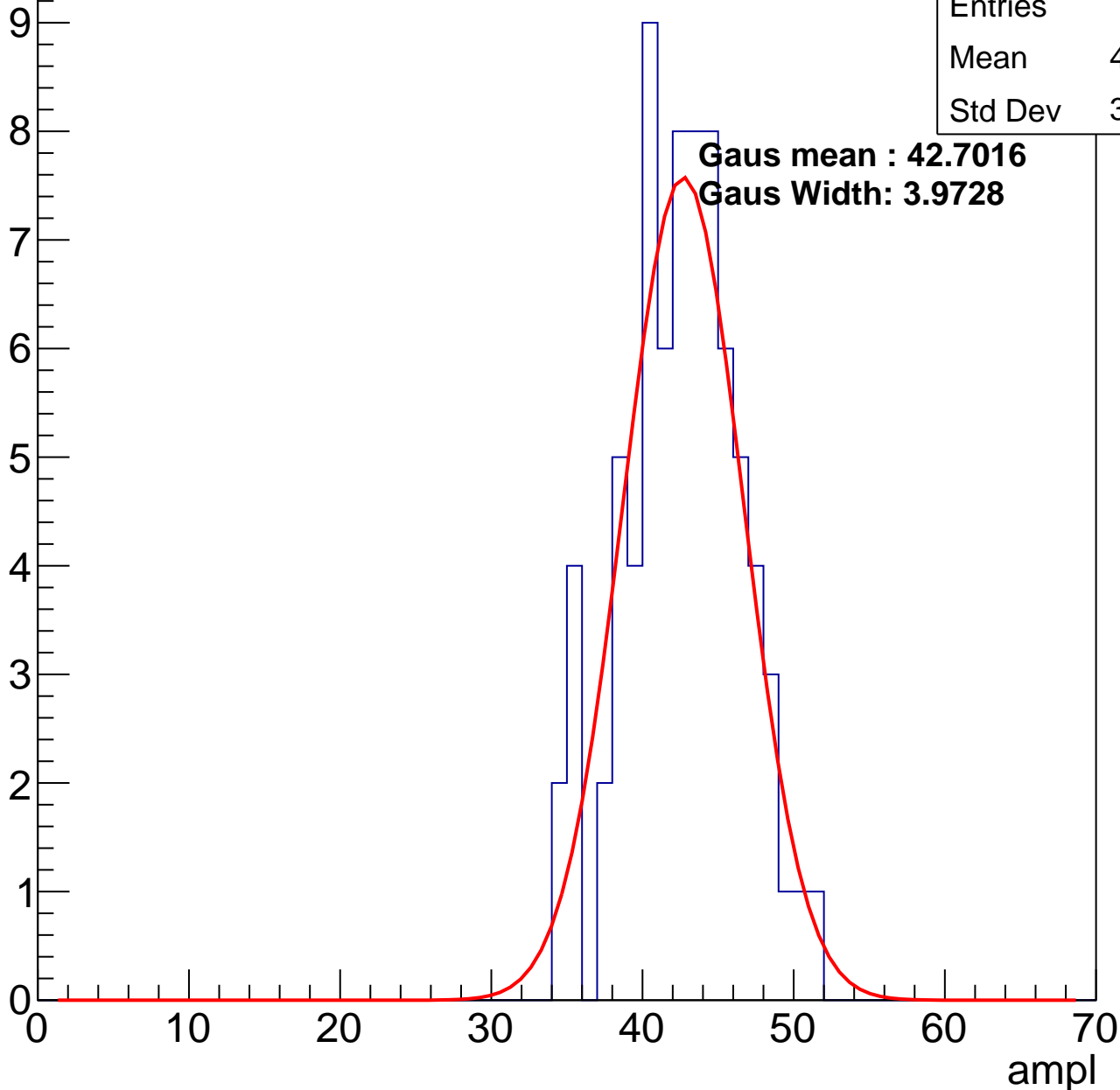
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	42.18
Std Dev	3.789

**Gaus mean : 42.7016**

**Gaus Width: 3.9728**

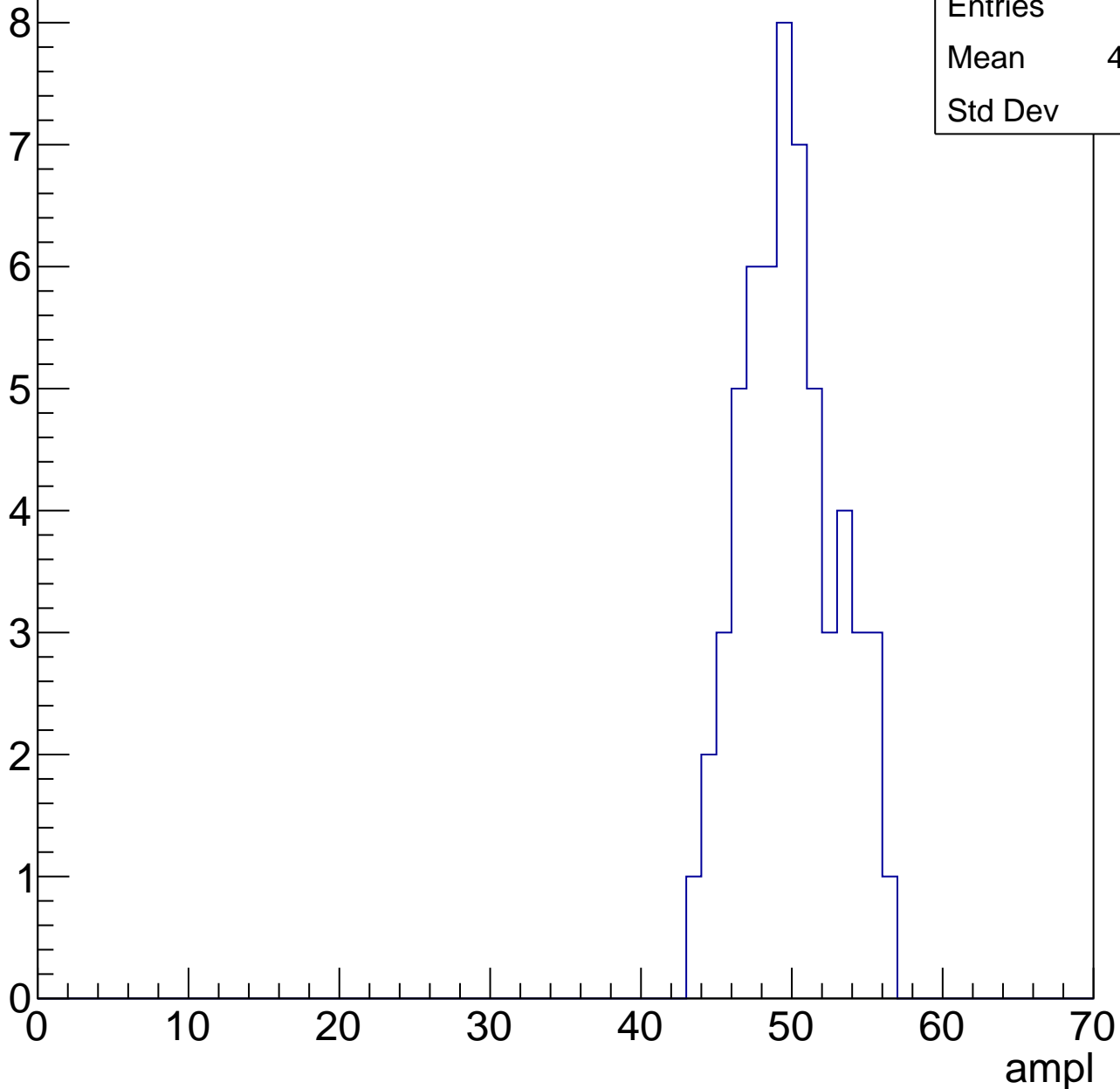


# B1L102S, U21-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	49.37
Std Dev	3.11

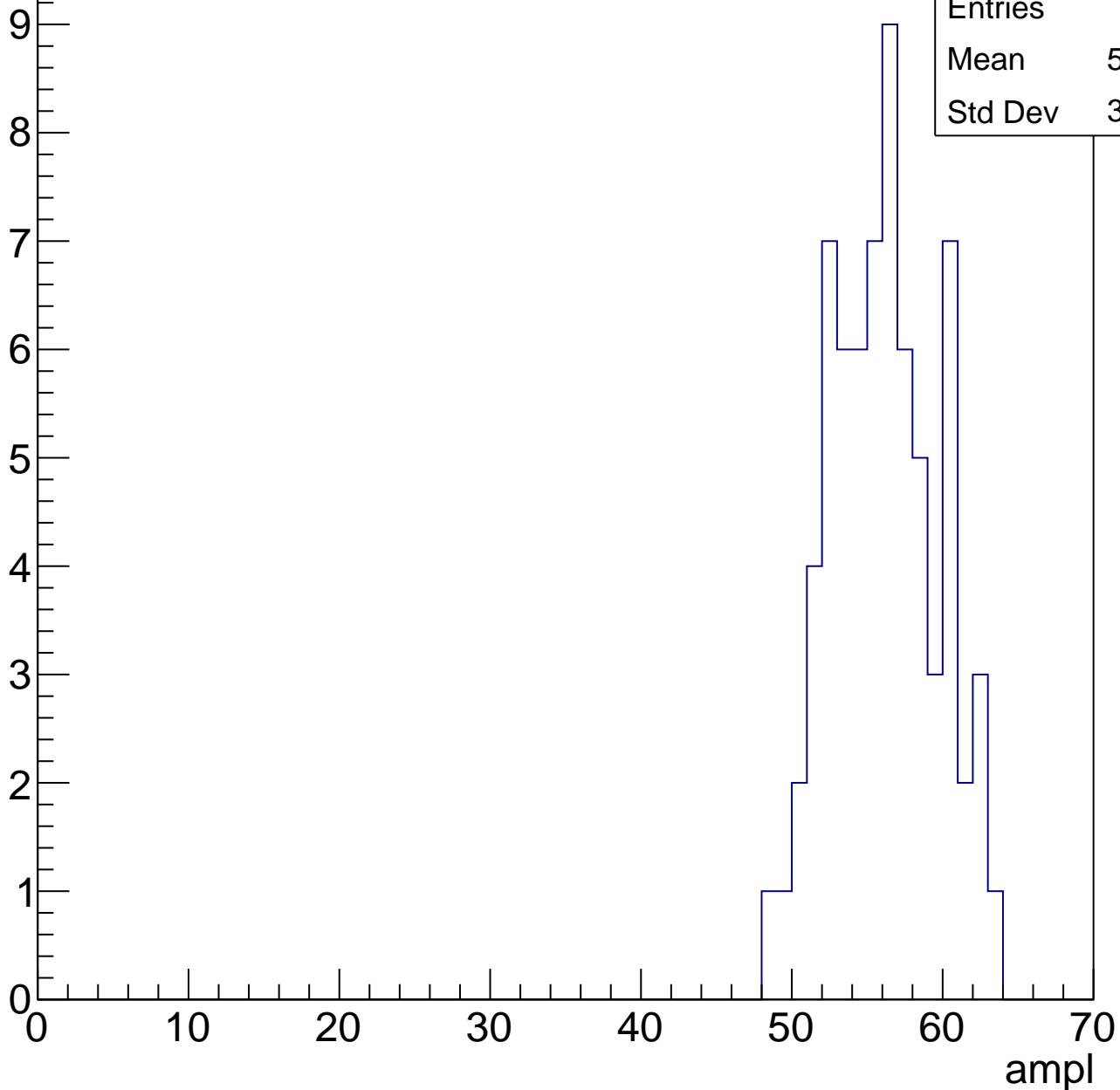


# B1L102S, U21-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	55.66
Std Dev	3.476

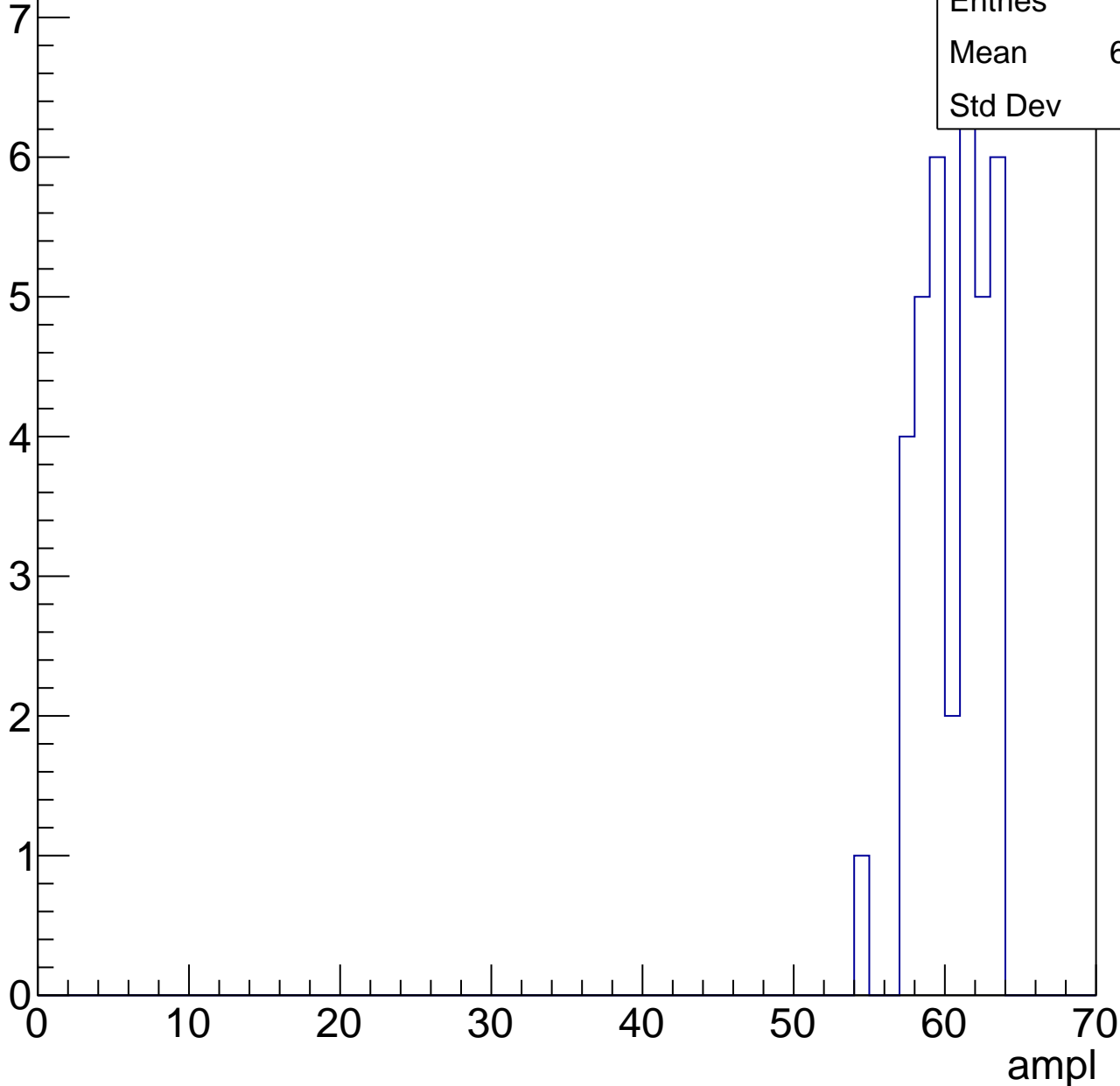


# B1L102S, U21-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

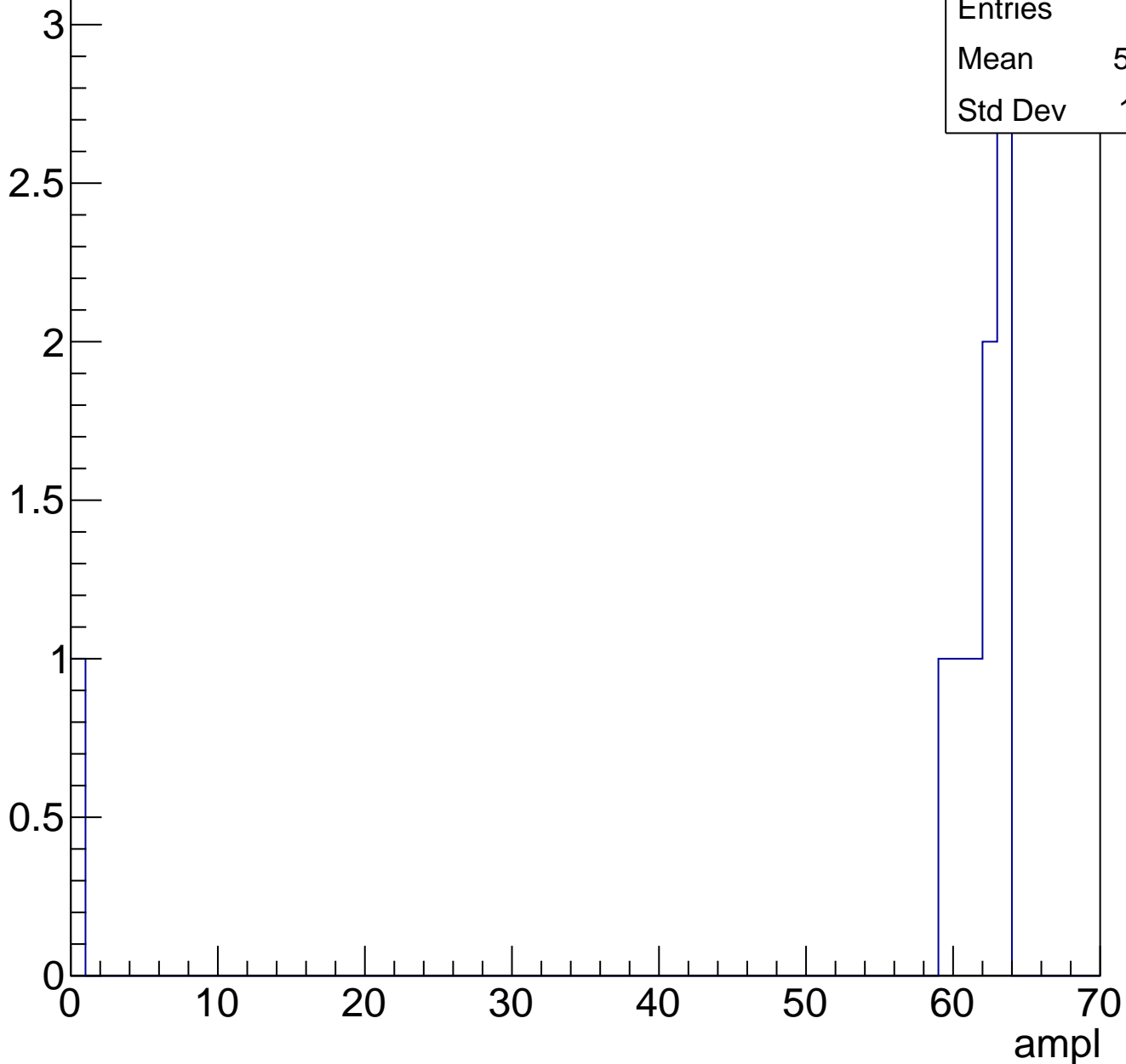
Entries	36
Mean	60.03
Std Dev	2.23



# B1L102S, U21-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U21-ch86, adc0

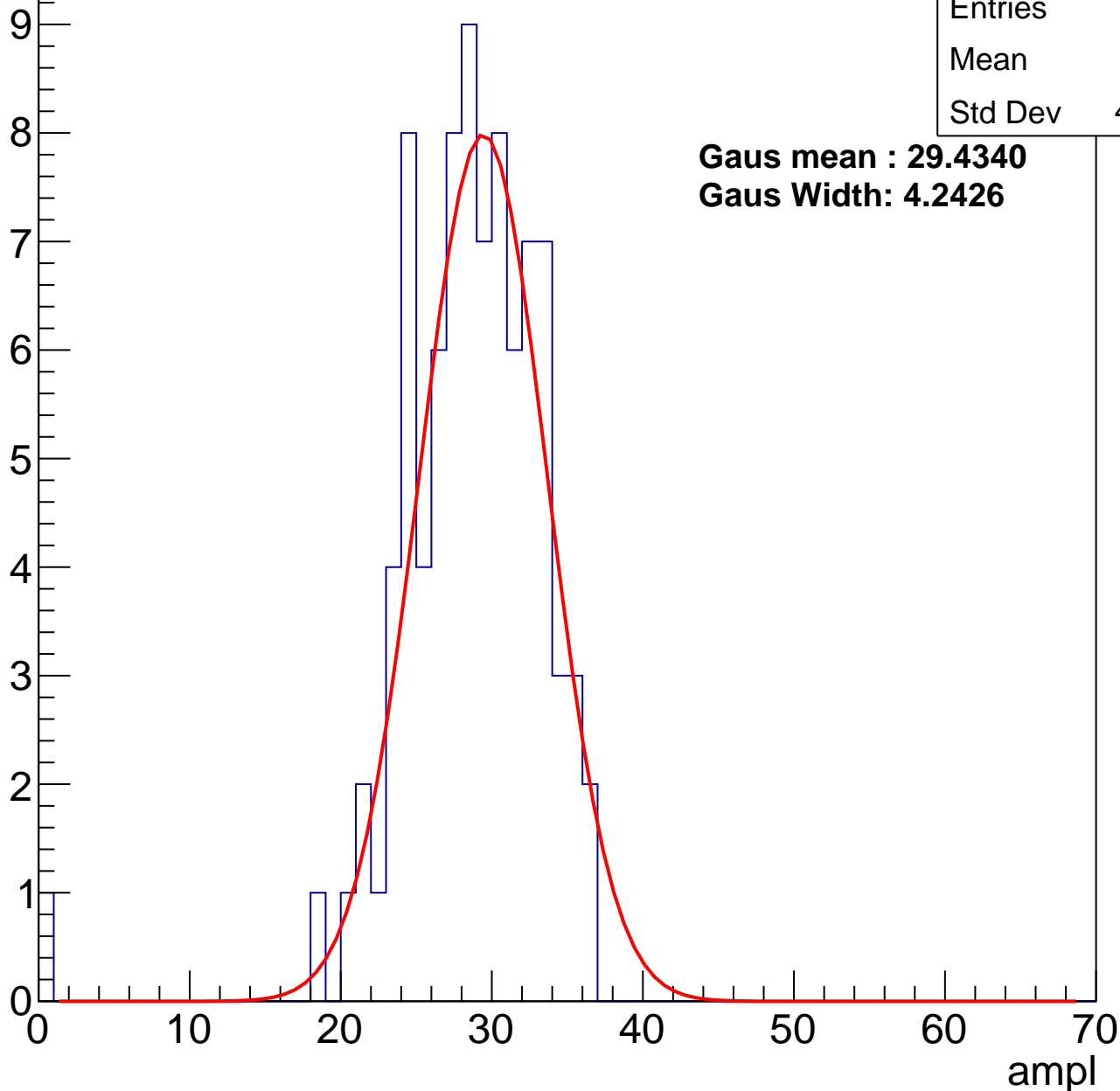
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	88
Mean	28.1
Std Dev	4.931

**Gaus mean : 29.4340**

**Gaus Width: 4.2426**



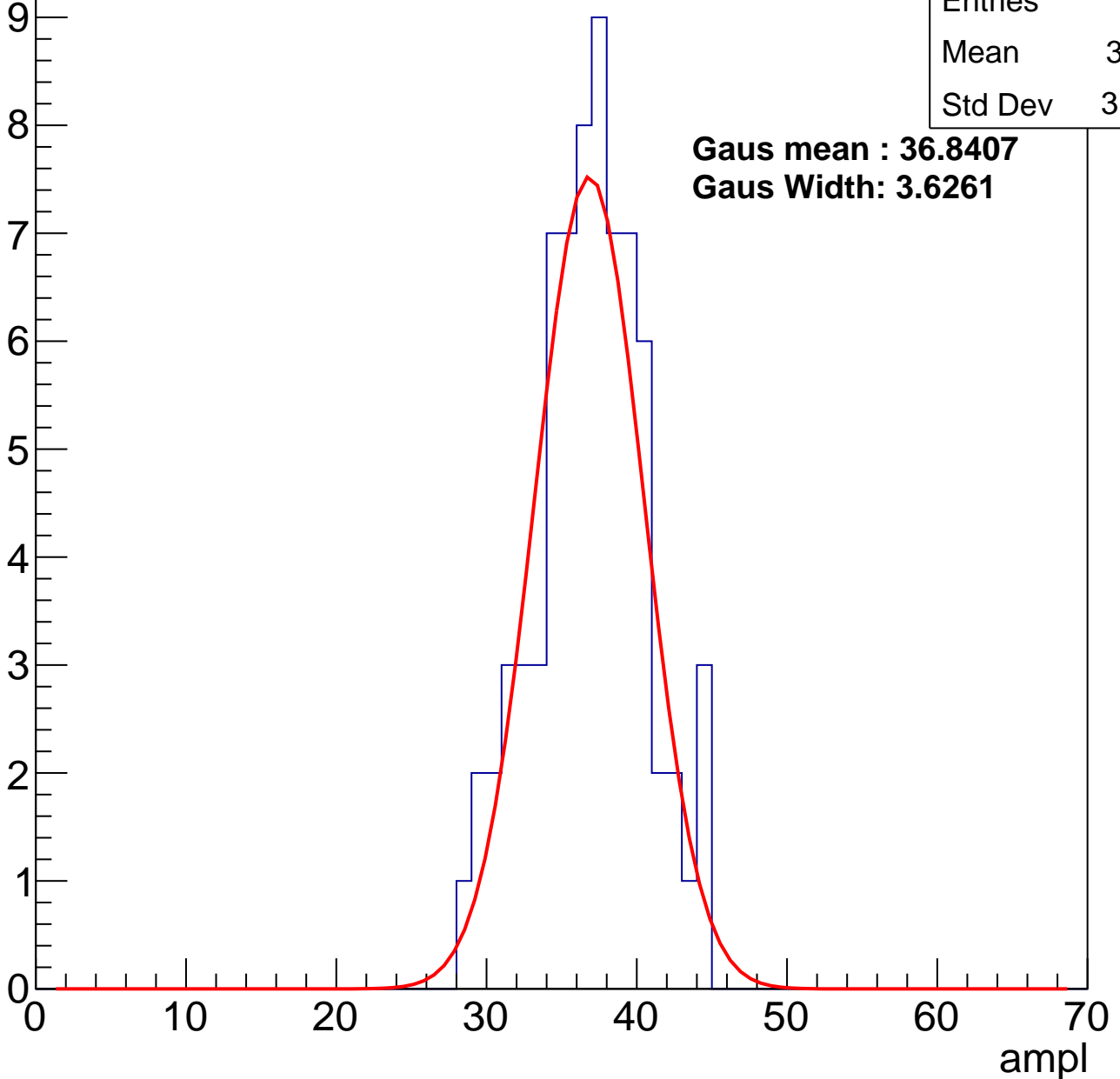
# B1L102S, U21-ch86, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	36.41
Std Dev	3.637

**Gaus mean : 36.8407**  
**Gaus Width: 3.6261**



# B1L102S, U21-ch86, adc2

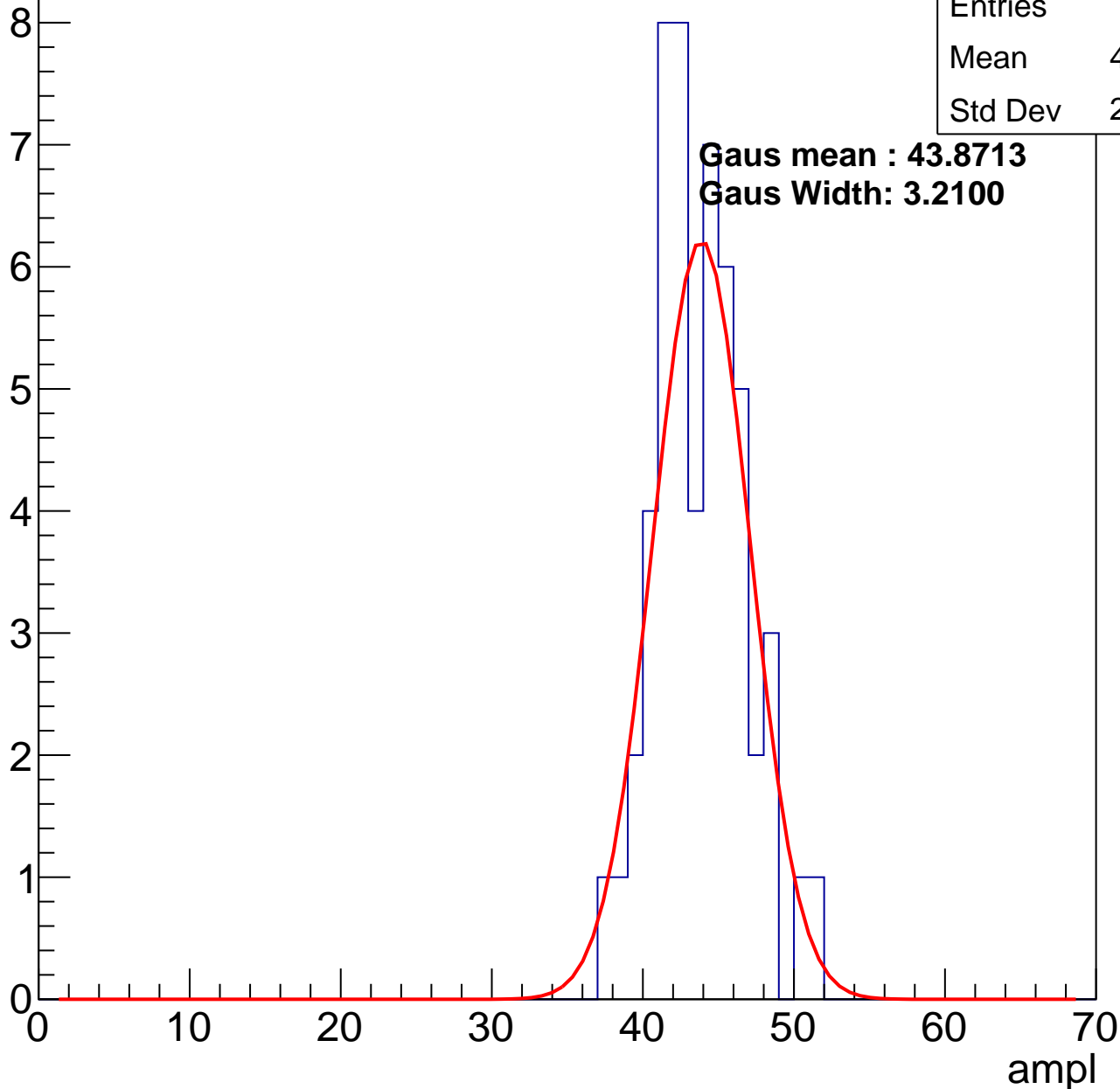
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	43.32
Std Dev	2.945

**Gaus mean : 43.8713**

**Gaus Width: 3.2100**

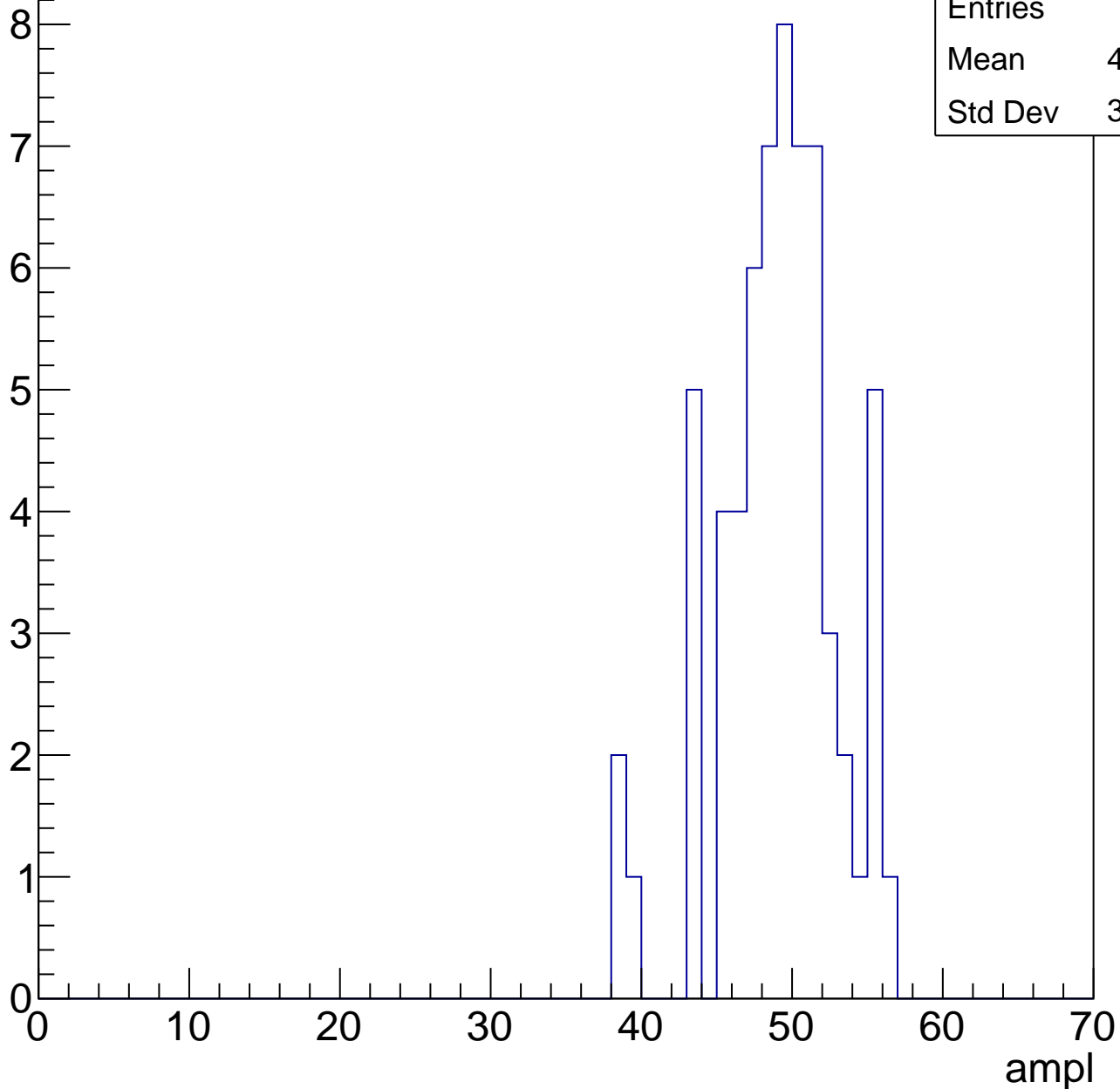


# B1L102S, U21-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	48.54
Std Dev	3.959

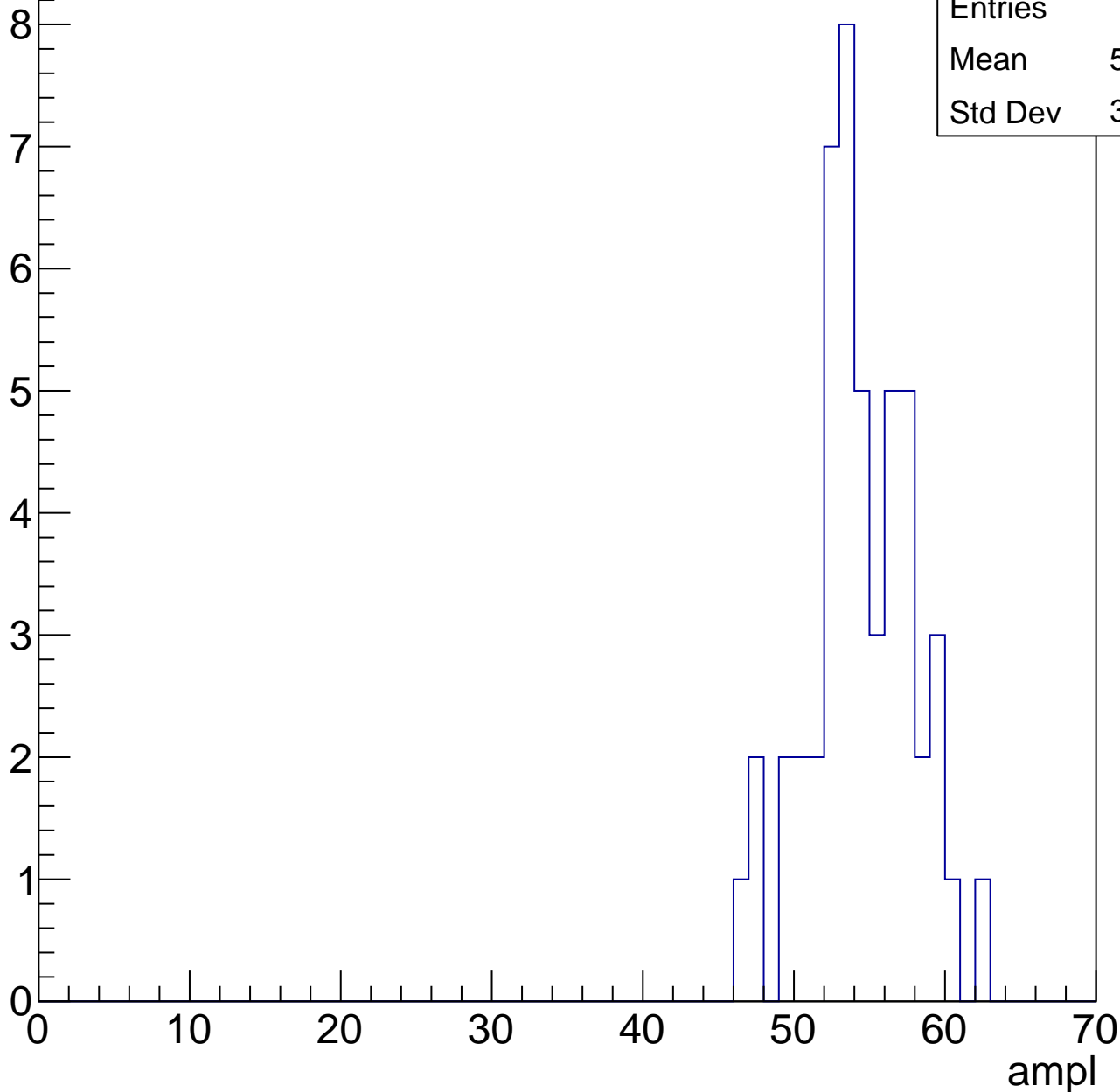


# B1L102S, U21-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	53.94
Std Dev	3.419

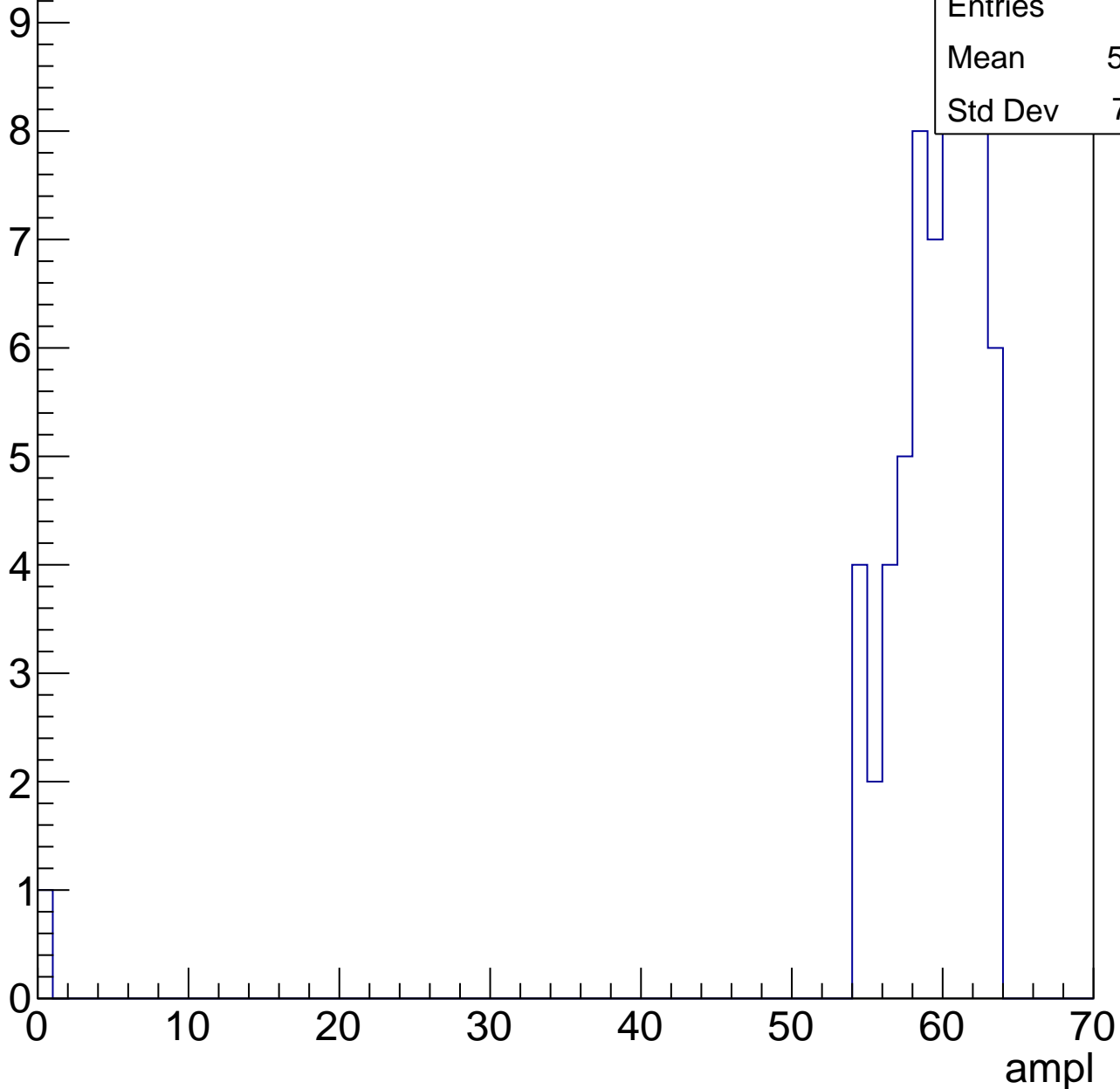


# B1L102S, U21-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	58.39
Std Dev	7.781



# B1L102S, U21-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L102S, U21-ch87, adc0

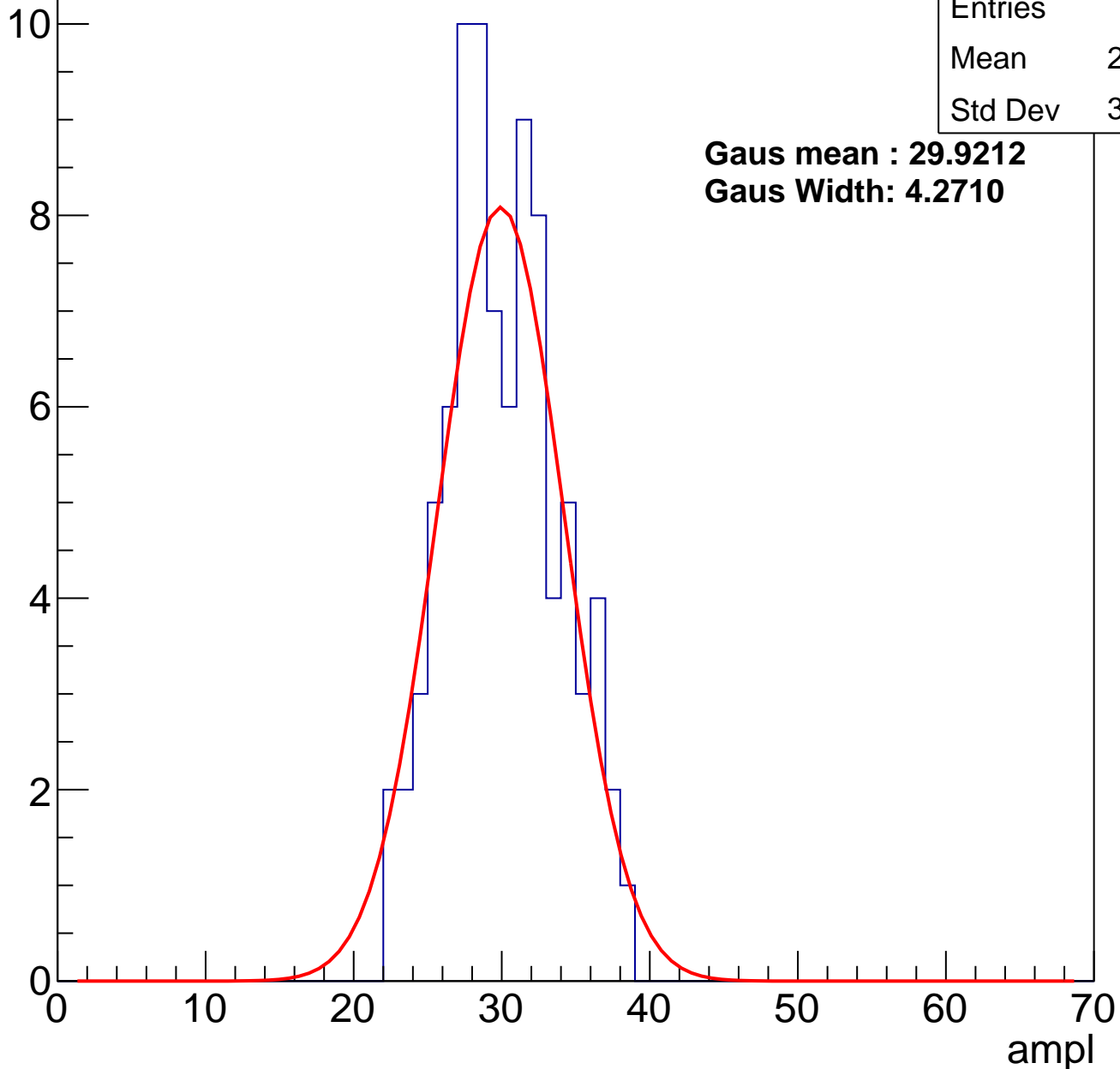
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	87
Mean	29.59
Std Dev	3.737

**Gaus mean : 29.9212**

**Gaus Width: 4.2710**

Entry



# B1L102S, U21-ch87, adc1

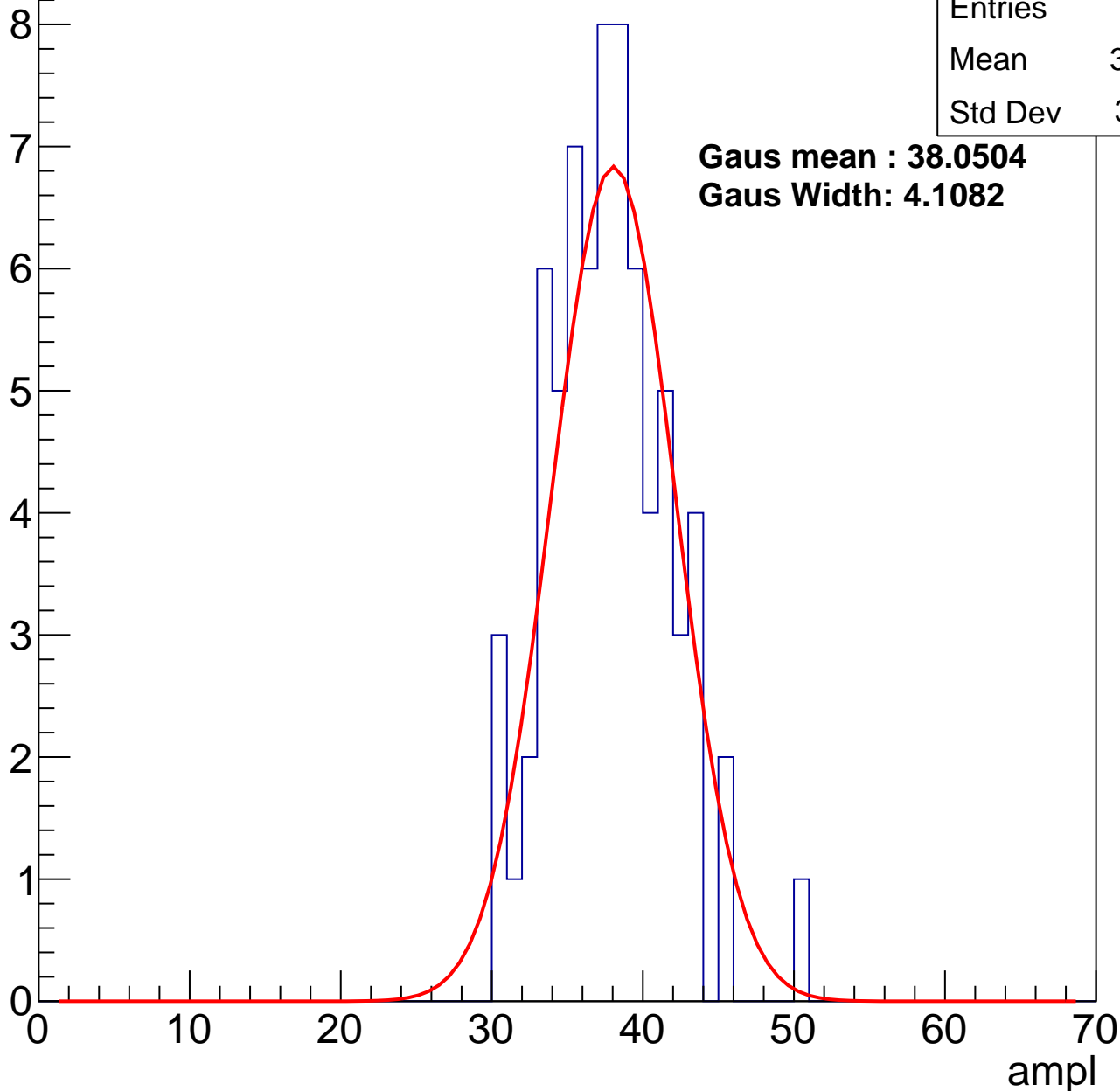
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	37.34
Std Dev	3.871

**Gaus mean : 38.0504**

**Gaus Width: 4.1082**



# B1L102S, U21-ch87, adc2

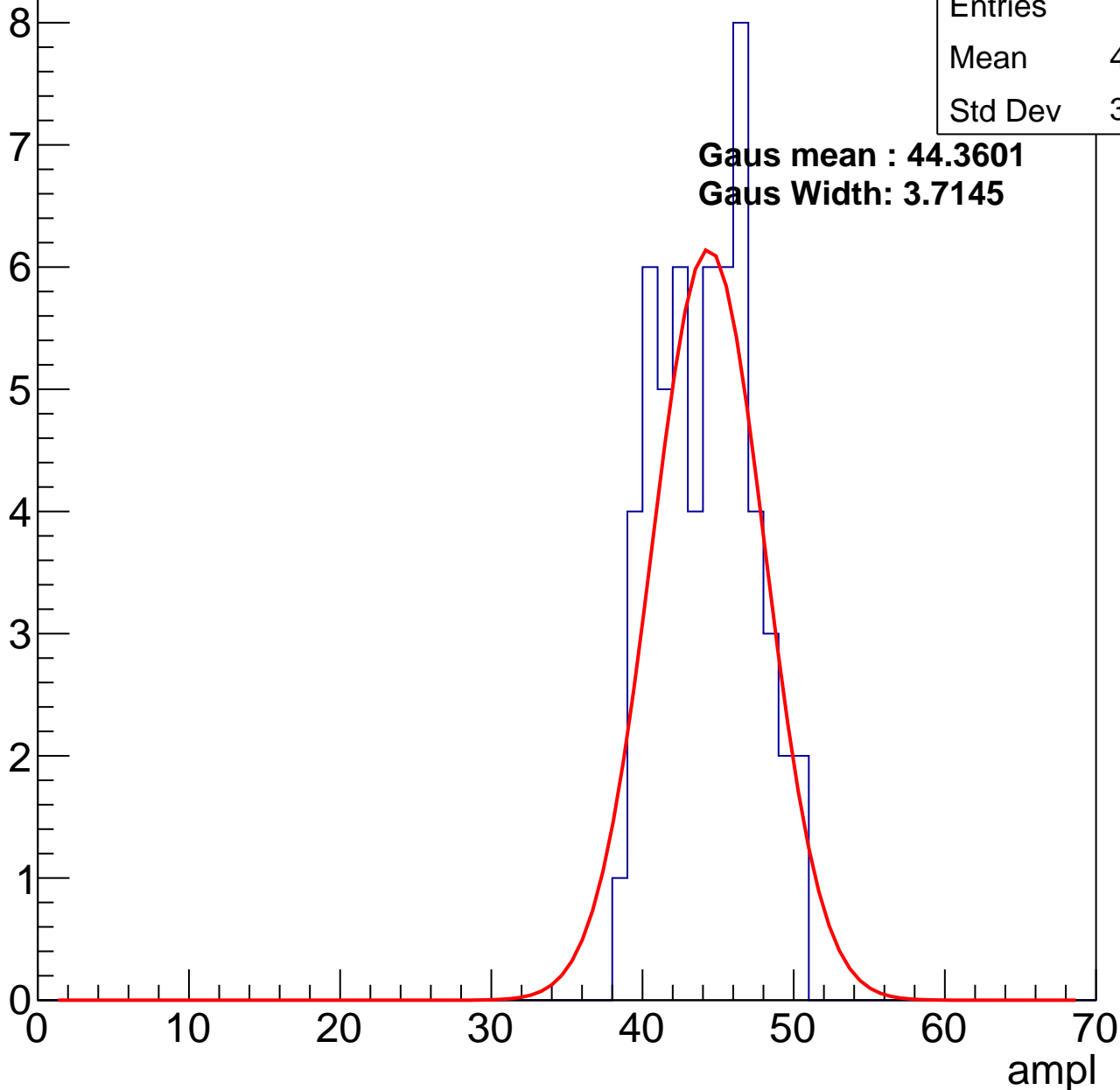
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	43.77
Std Dev	3.095

**Gaus mean : 44.3601**

**Gaus Width: 3.7145**

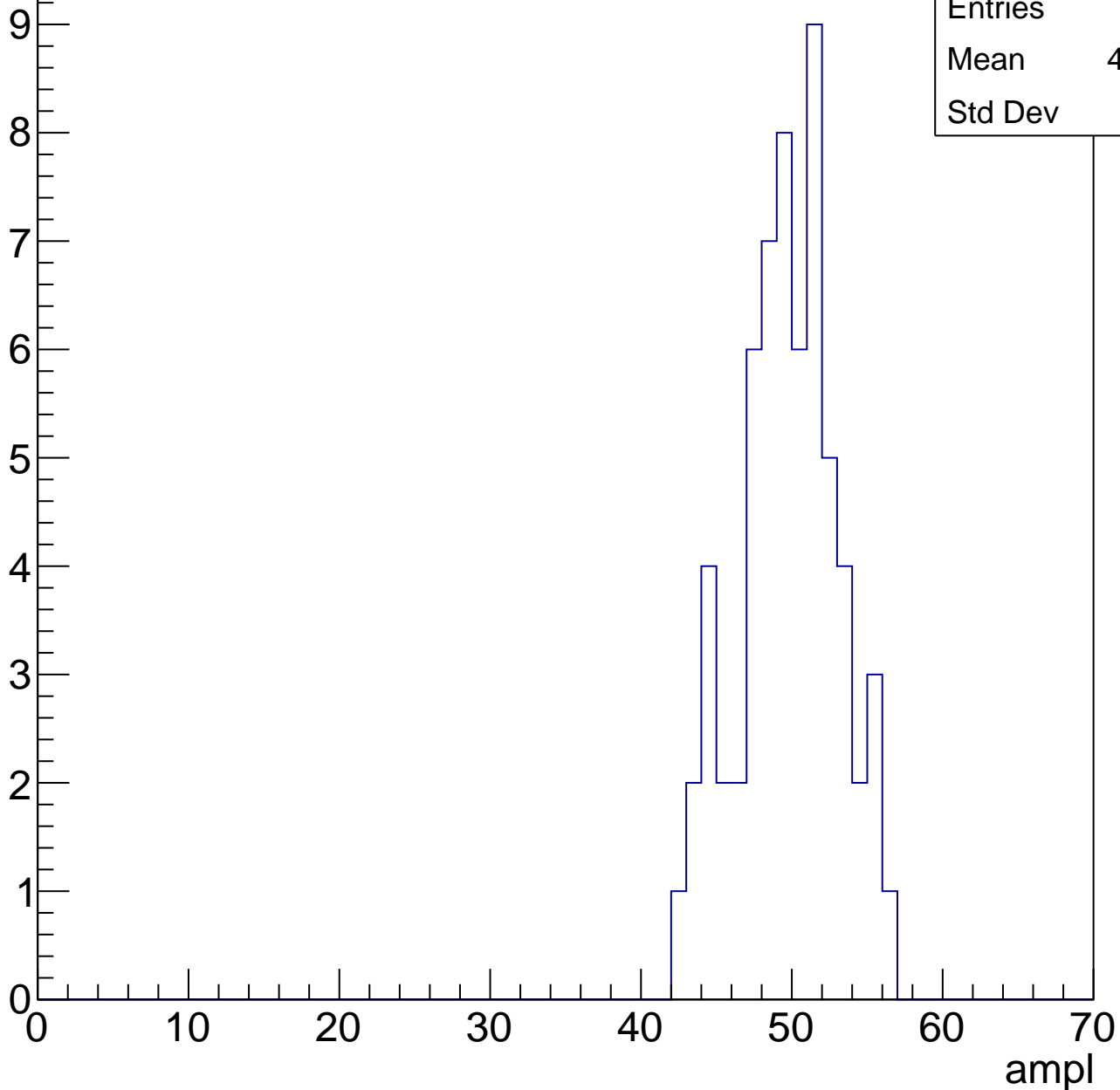


# B1L102S, U21-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	49.29
Std Dev	3.25

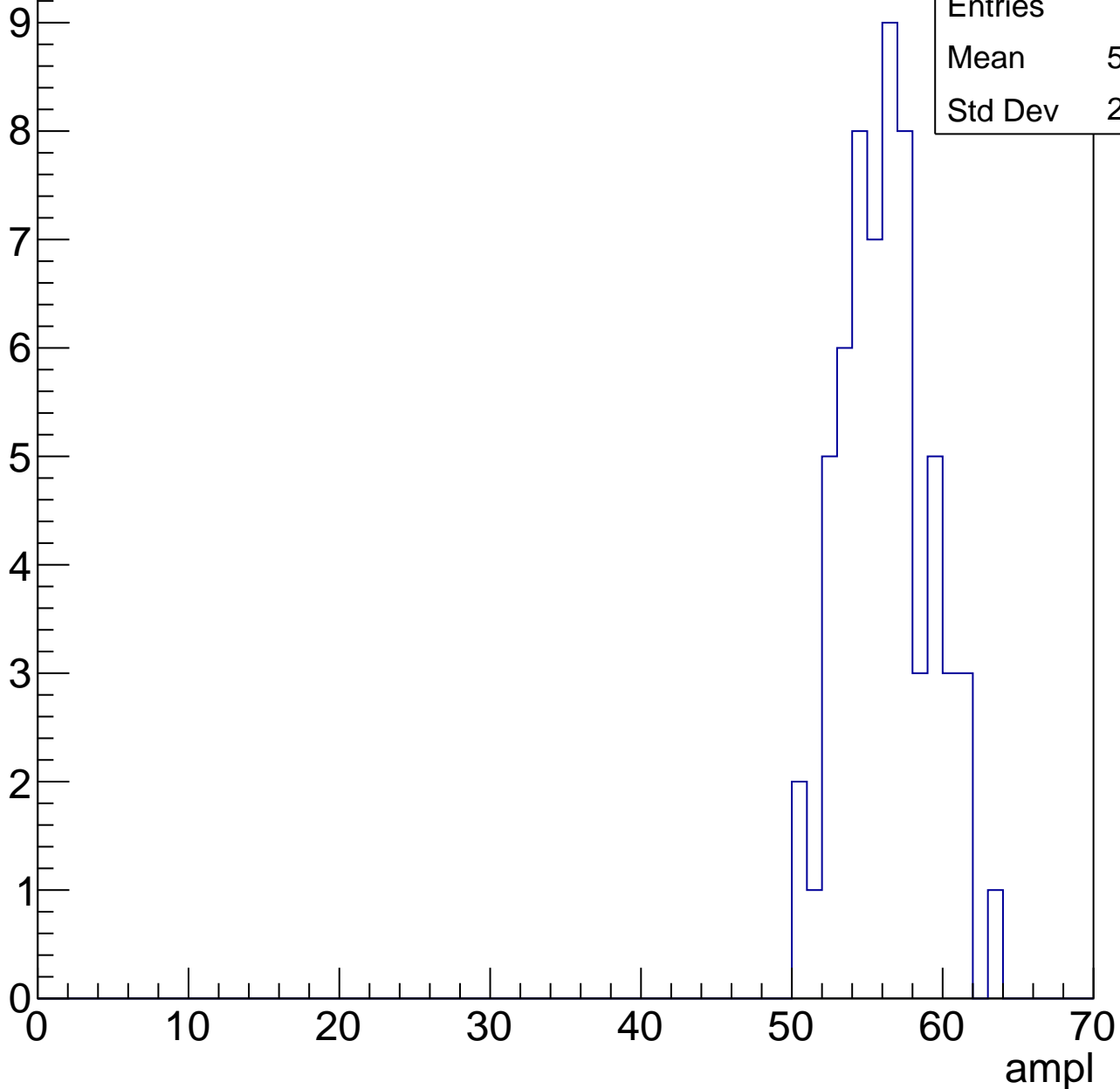


# B1L102S, U21-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	55.75
Std Dev	2.872

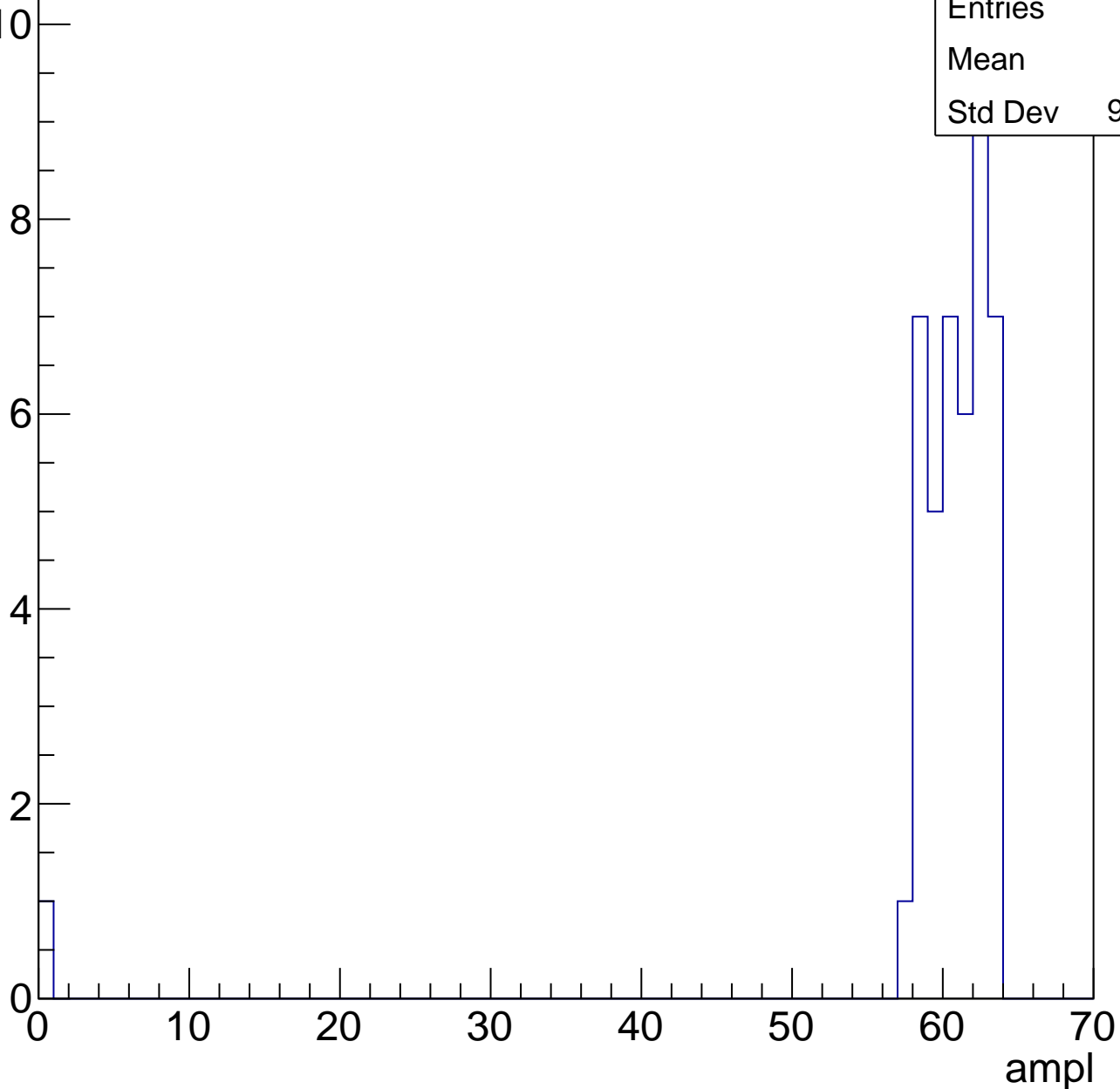


# B1L102S, U21-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

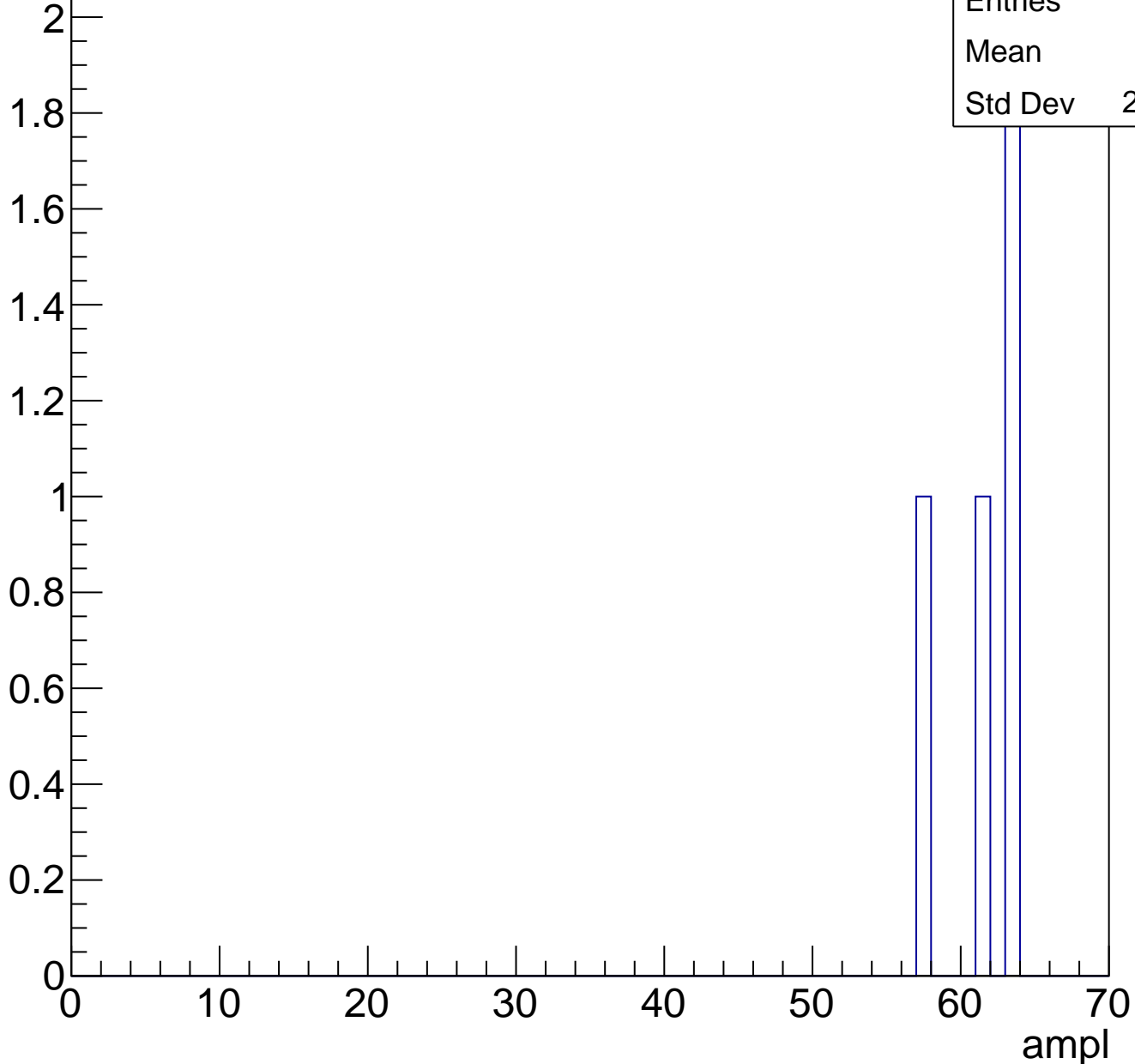
Entries	44
Mean	59.2
Std Dev	9.199



# B1L102S, U21-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	22
Std Dev	0

ampl

# B1L102S, U21-ch88, adc0

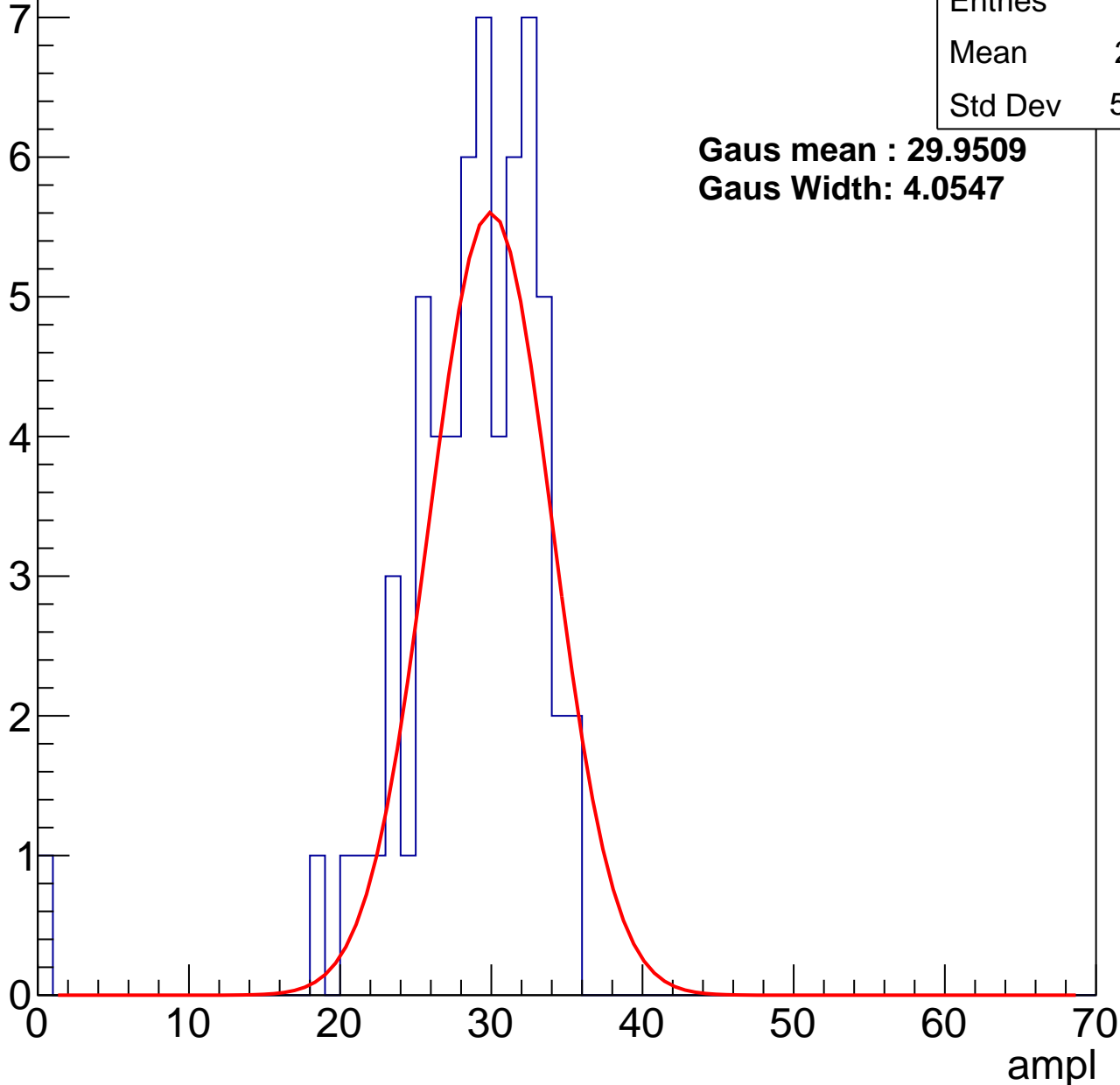
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	28.11
Std Dev	5.236

**Gaus mean : 29.9509**

**Gaus Width: 4.0547**



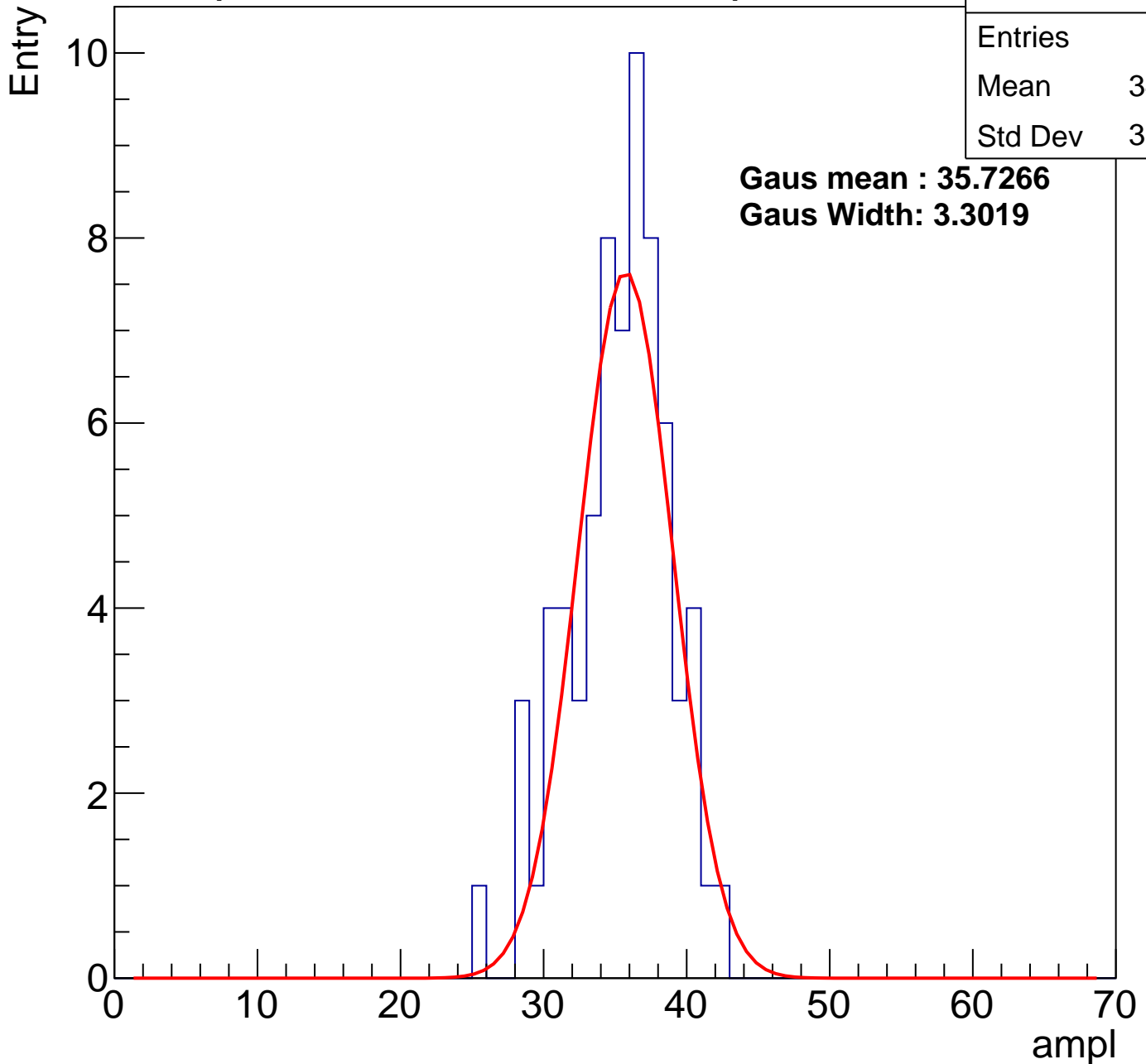
# B1L102S, U21-ch88, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	69
Mean	34.84
Std Dev	3.467

**Gaus mean : 35.7266**

**Gaus Width: 3.3019**



# B1L102S, U21-ch88, adc2

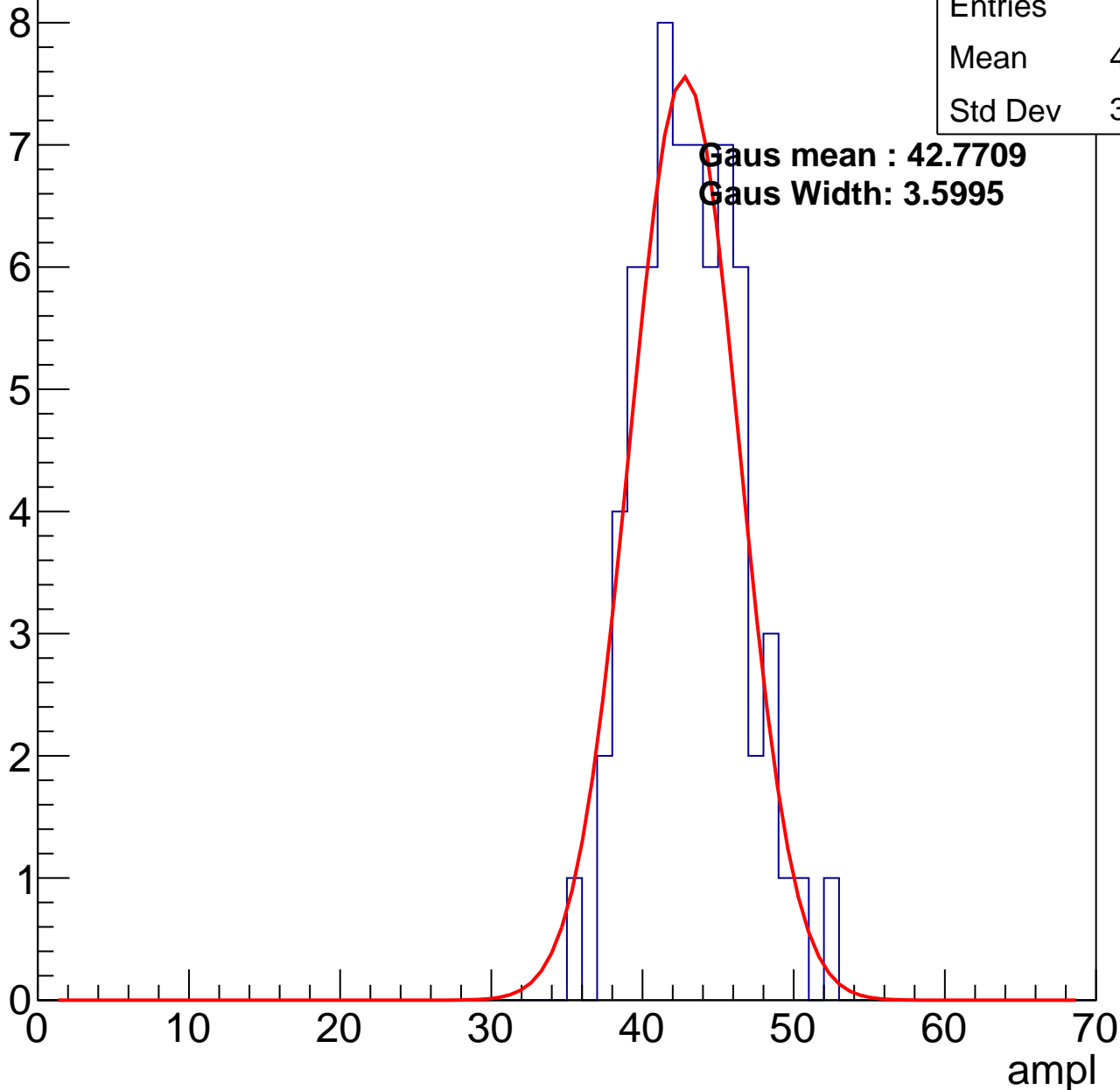
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	42.68
Std Dev	3.384

**Gaus mean : 42.7709**

**Gaus Width: 3.5995**

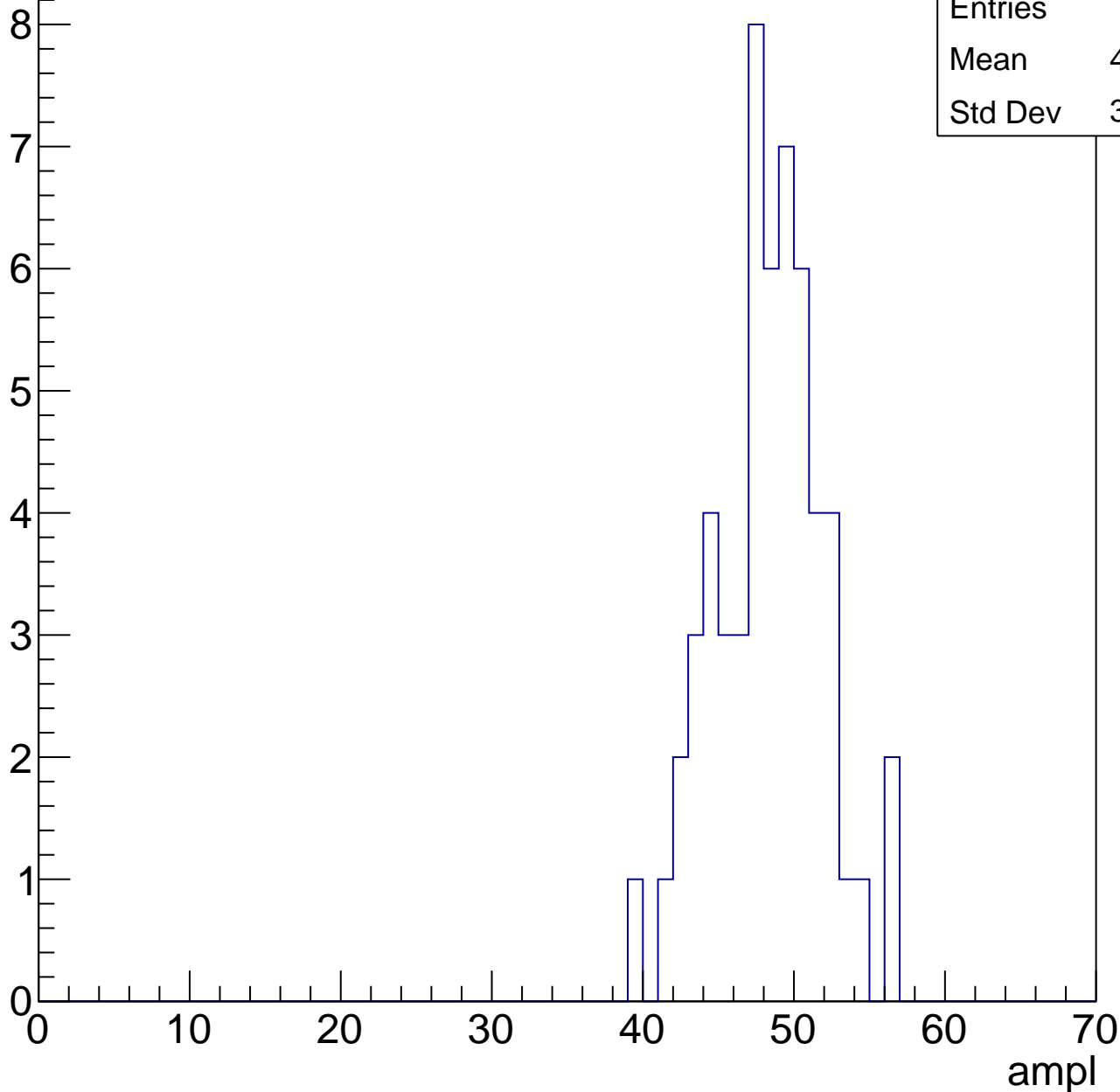


# B1L102S, U21-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	47.86
Std Dev	3.553

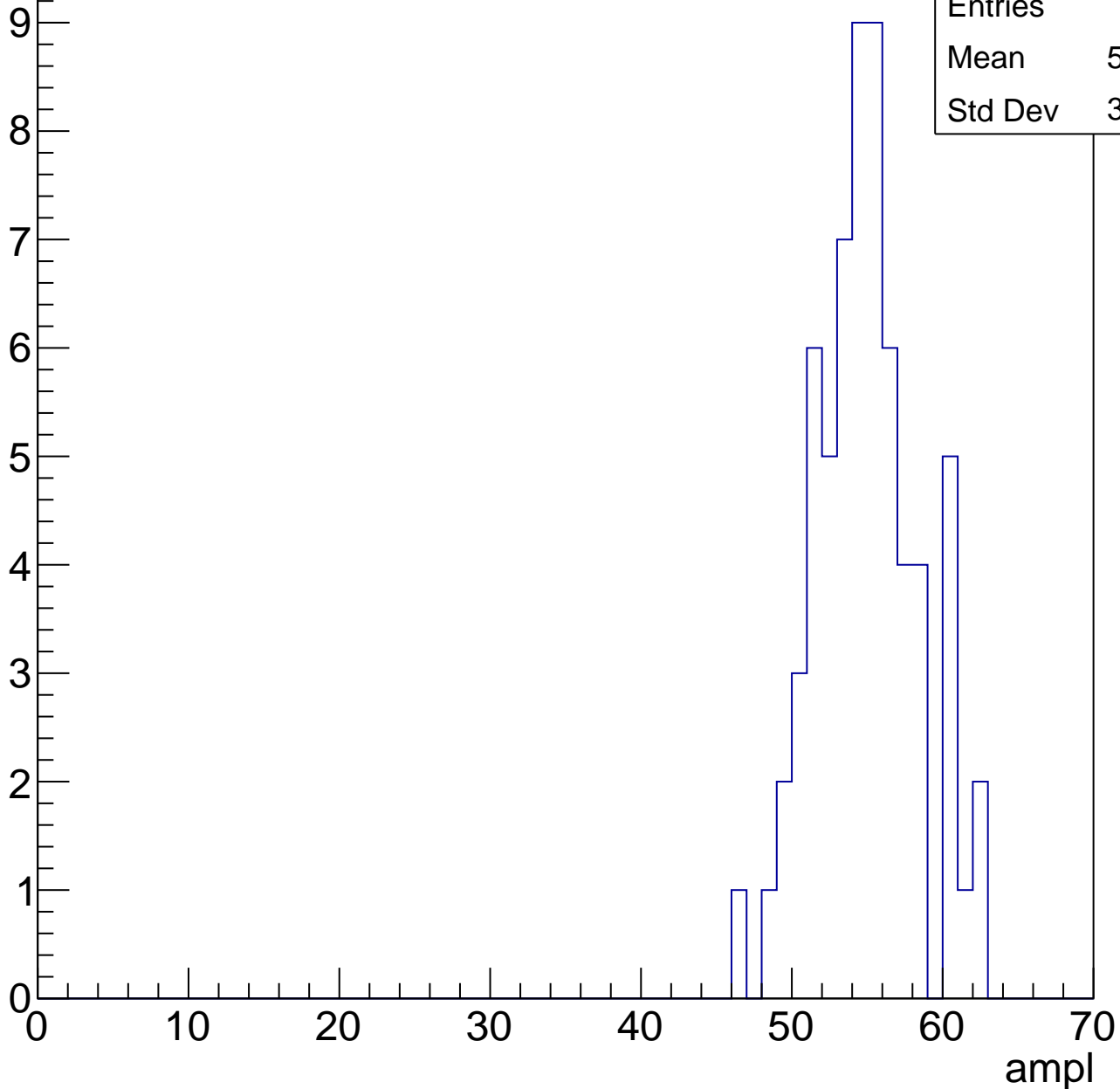


# B1L102S, U21-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	54.48
Std Dev	3.406



# B1L102S, U21-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	45
Mean	57.8
Std Dev	9.042

Entry

10

8

6

4

2

0

0

10

20

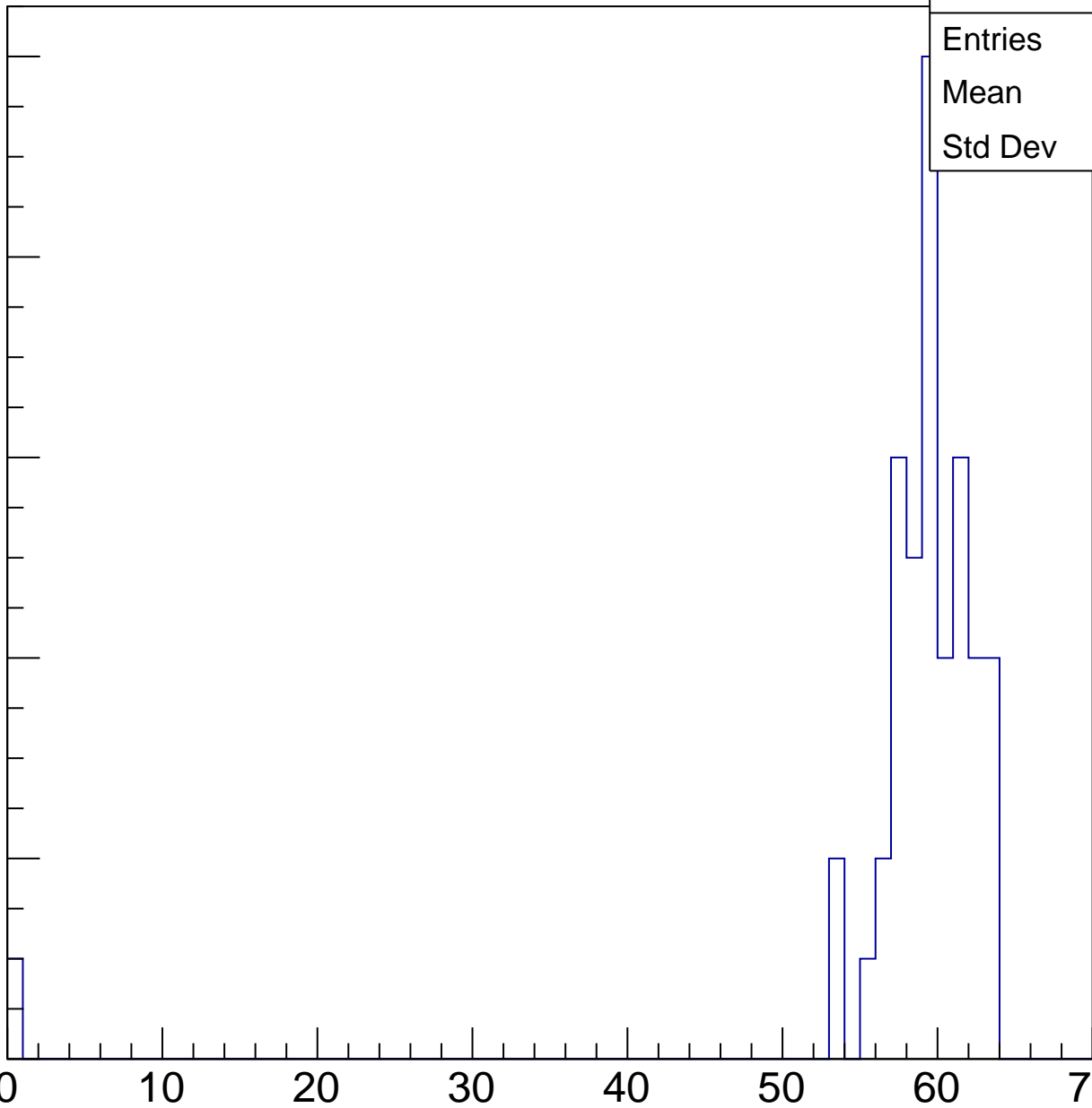
30

40

50

60

ampl

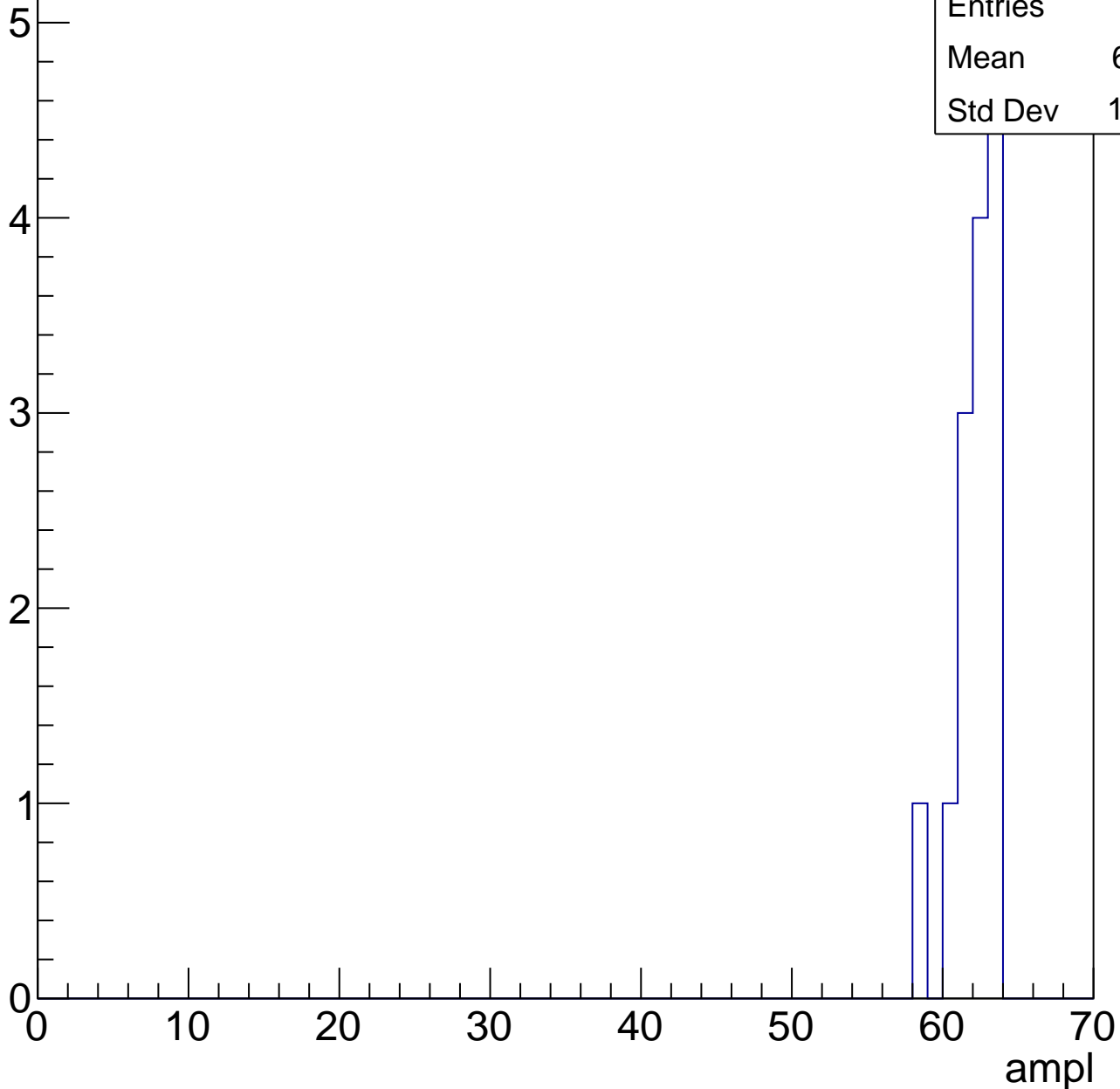


# B1L102S, U21-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	14
Mean	61.71
Std Dev	1.385





# B1L102S, U21-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch89, adc0

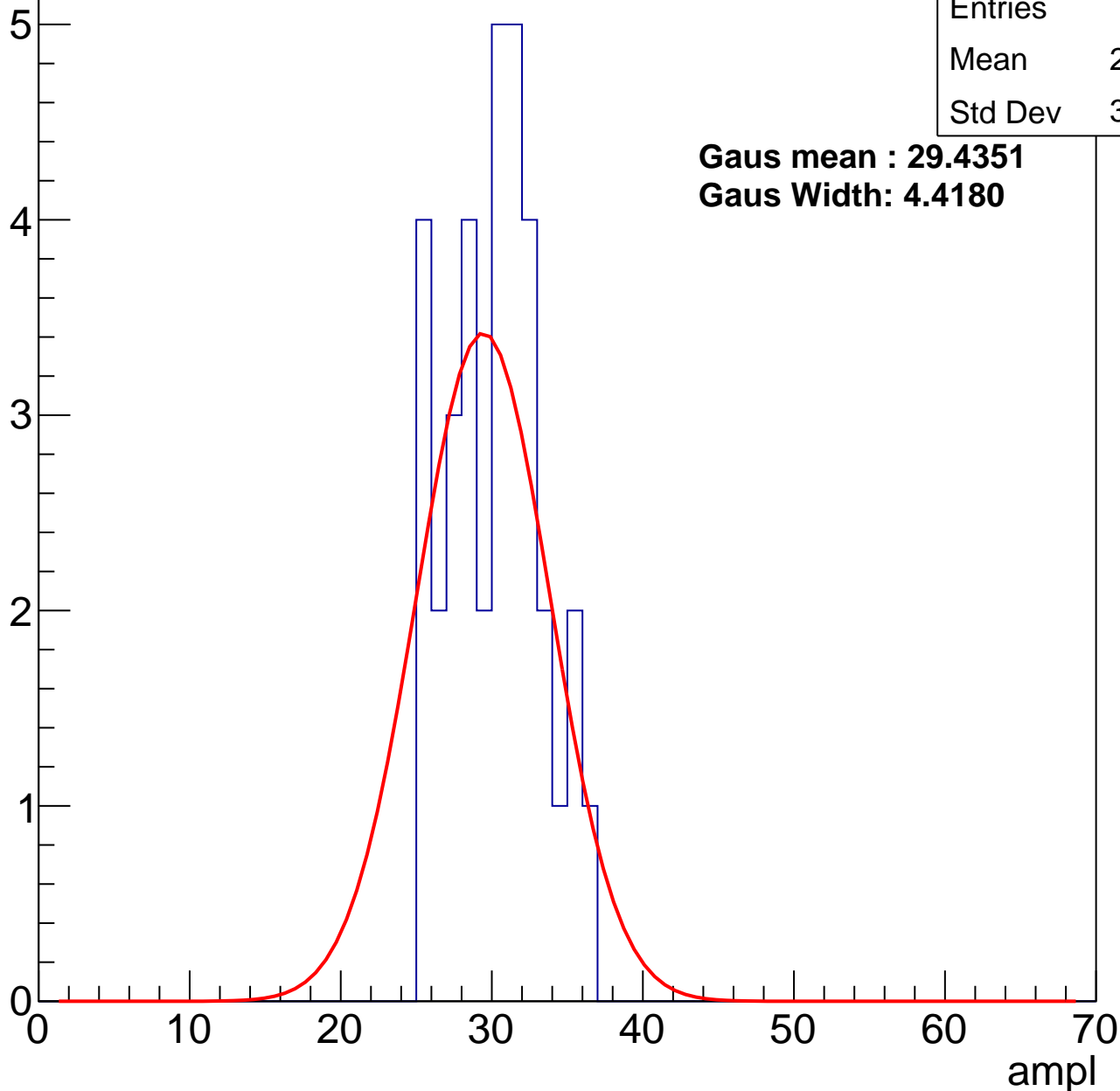
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	35
Mean	29.77
Std Dev	3.006

**Gaus mean : 29.4351**

**Gaus Width: 4.4180**



# B1L102S, U21-ch89, adc1

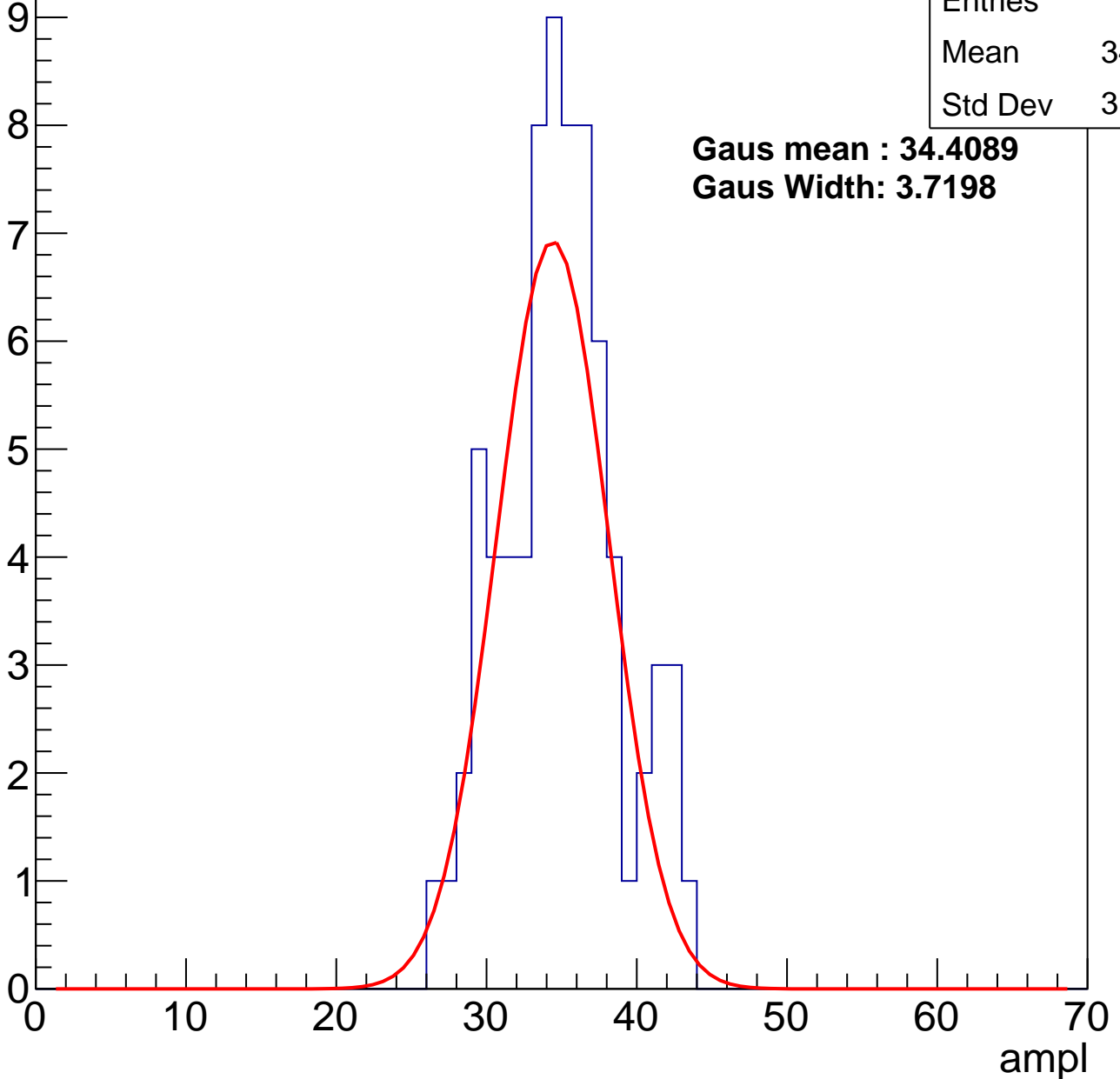
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	34.45
Std Dev	3.845

**Gaus mean : 34.4089**

**Gaus Width: 3.7198**



# B1L102S, U21-ch89, adc2

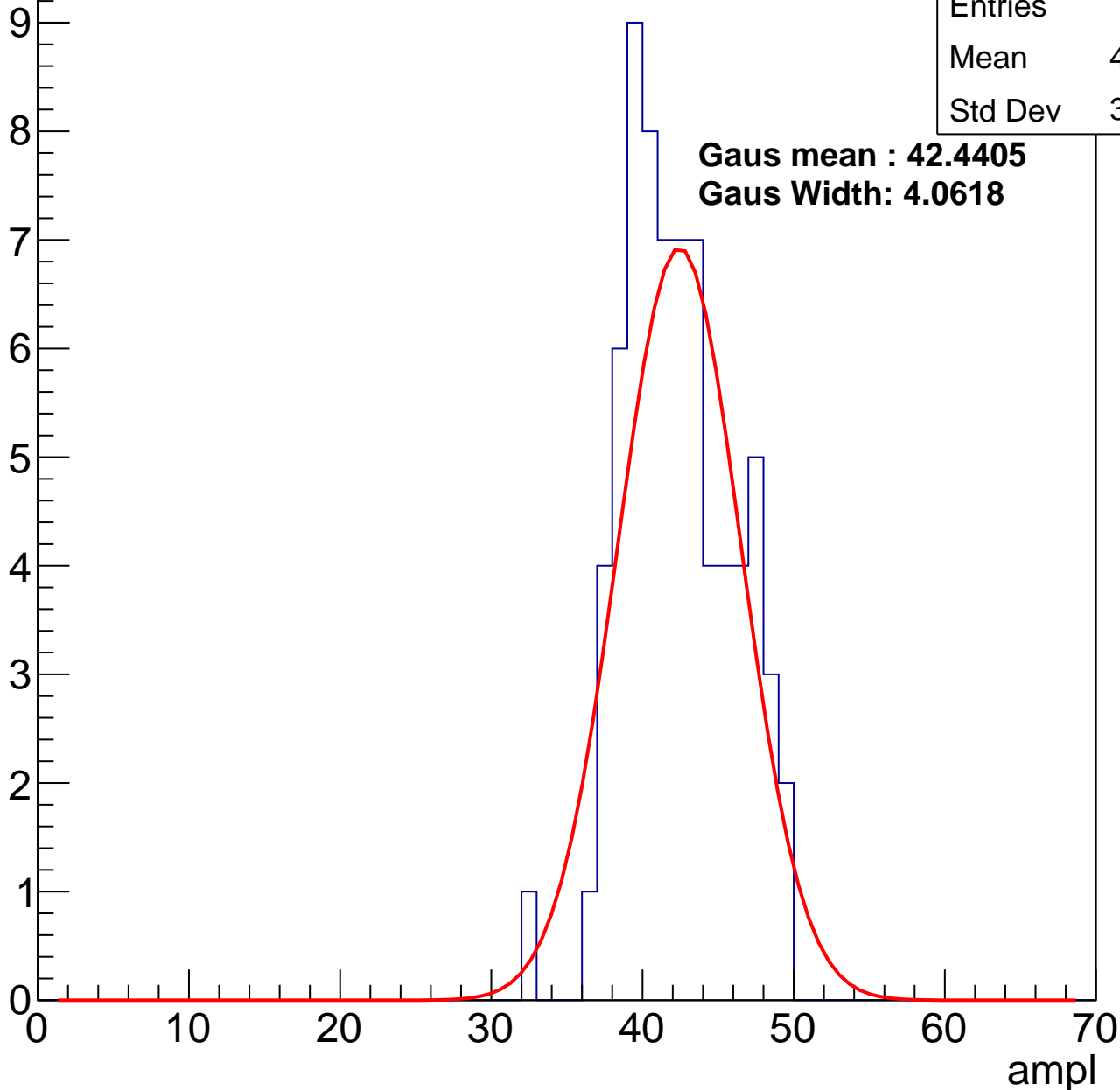
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	41.86
Std Dev	3.545

**Gaus mean : 42.4405**

**Gaus Width: 4.0618**

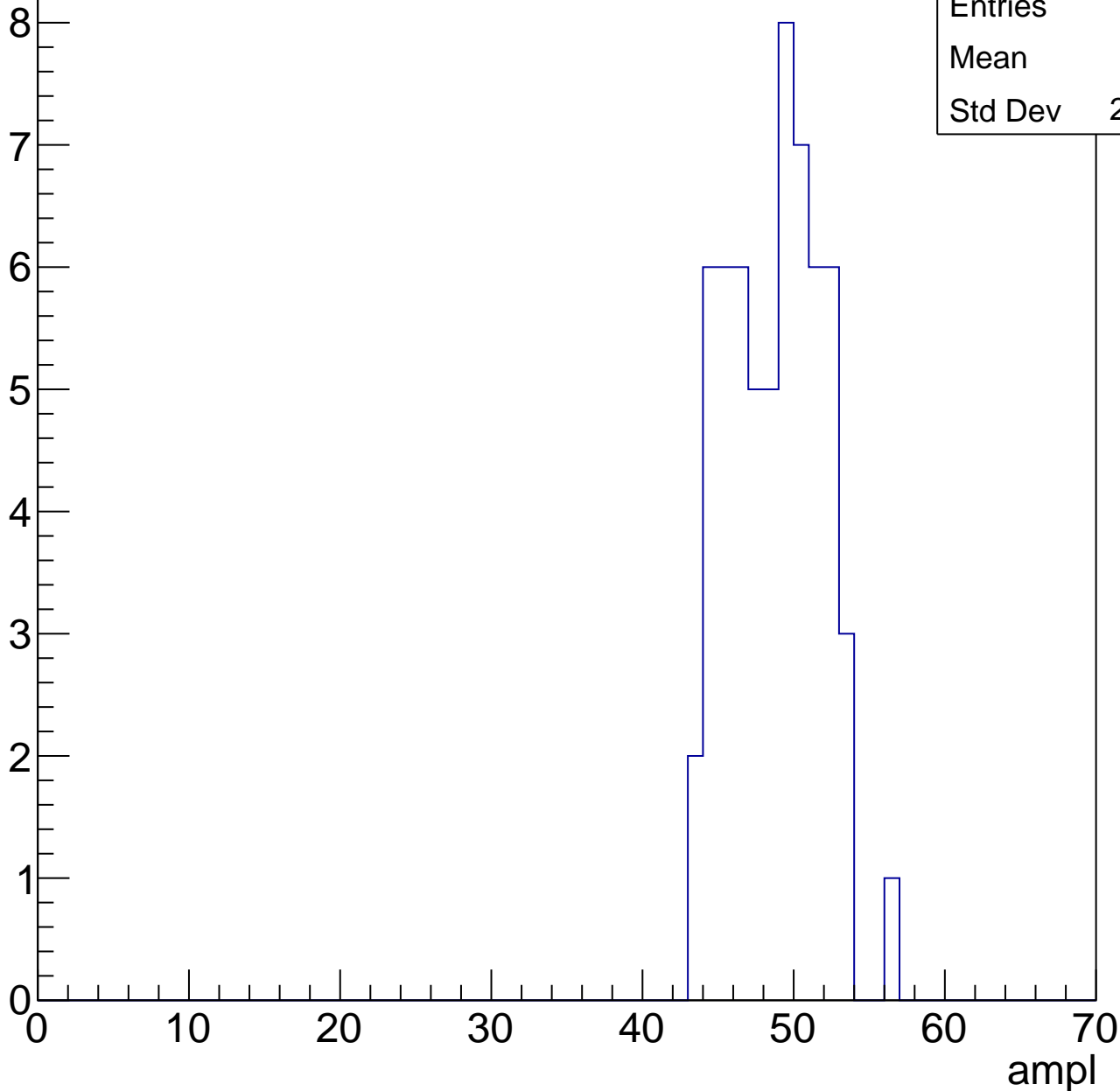


# B1L102S, U21-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	48.3
Std Dev	2.999

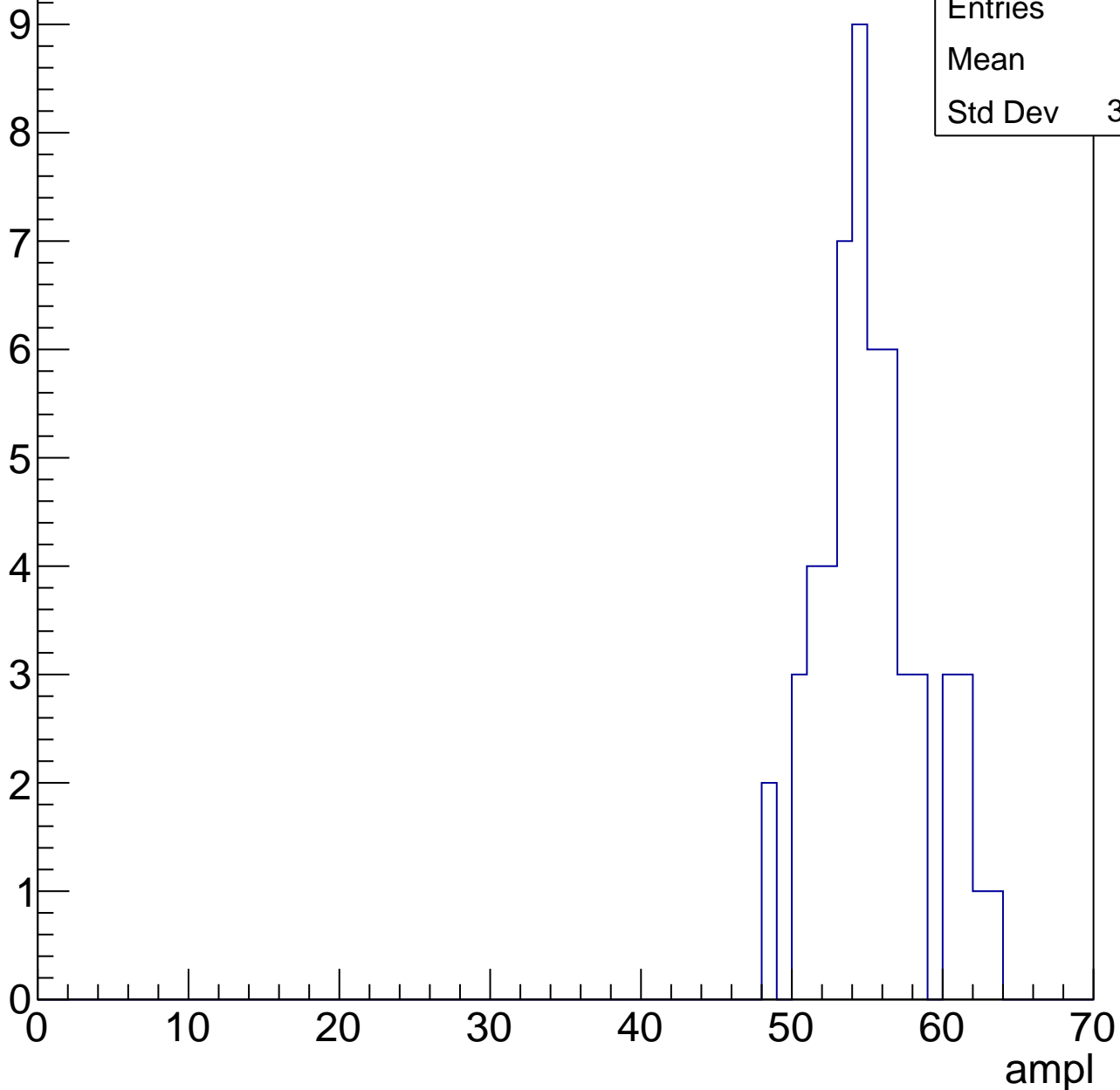


# B1L102S, U21-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	54.8
Std Dev	3.435



# B1L102S, U21-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

10

8

6

4

2

0

0

10

20

30

40

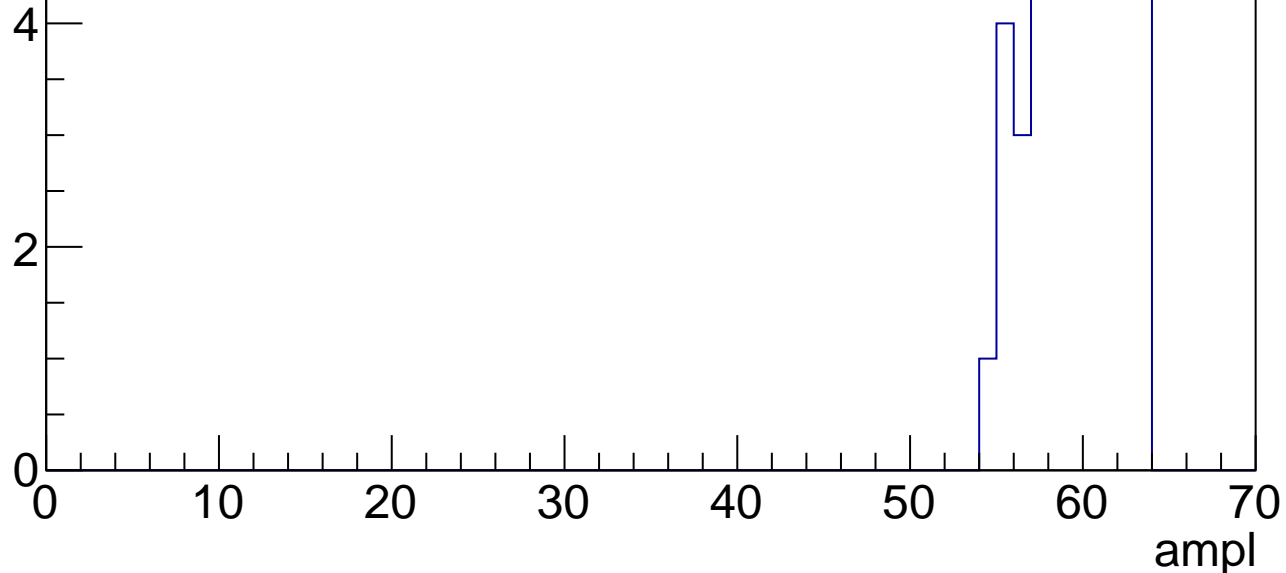
50

60

70

ampl

Entries	53
Mean	59.09
Std Dev	2.428



# B1L102S, U21-ch89, adc6

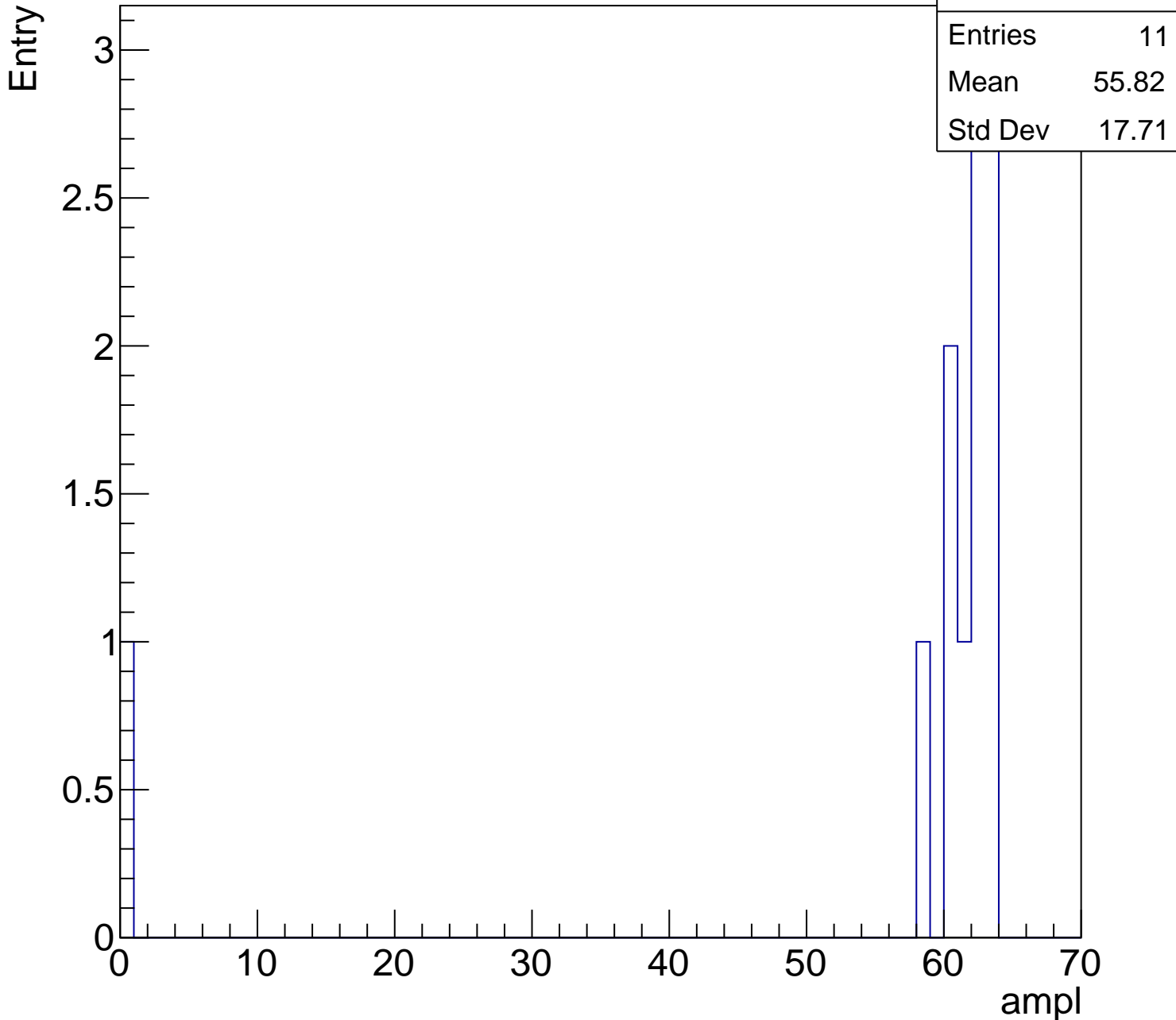
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	11
Mean	55.82
Std Dev	17.71

ampl





# B1L102S, U21-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch90, adc0

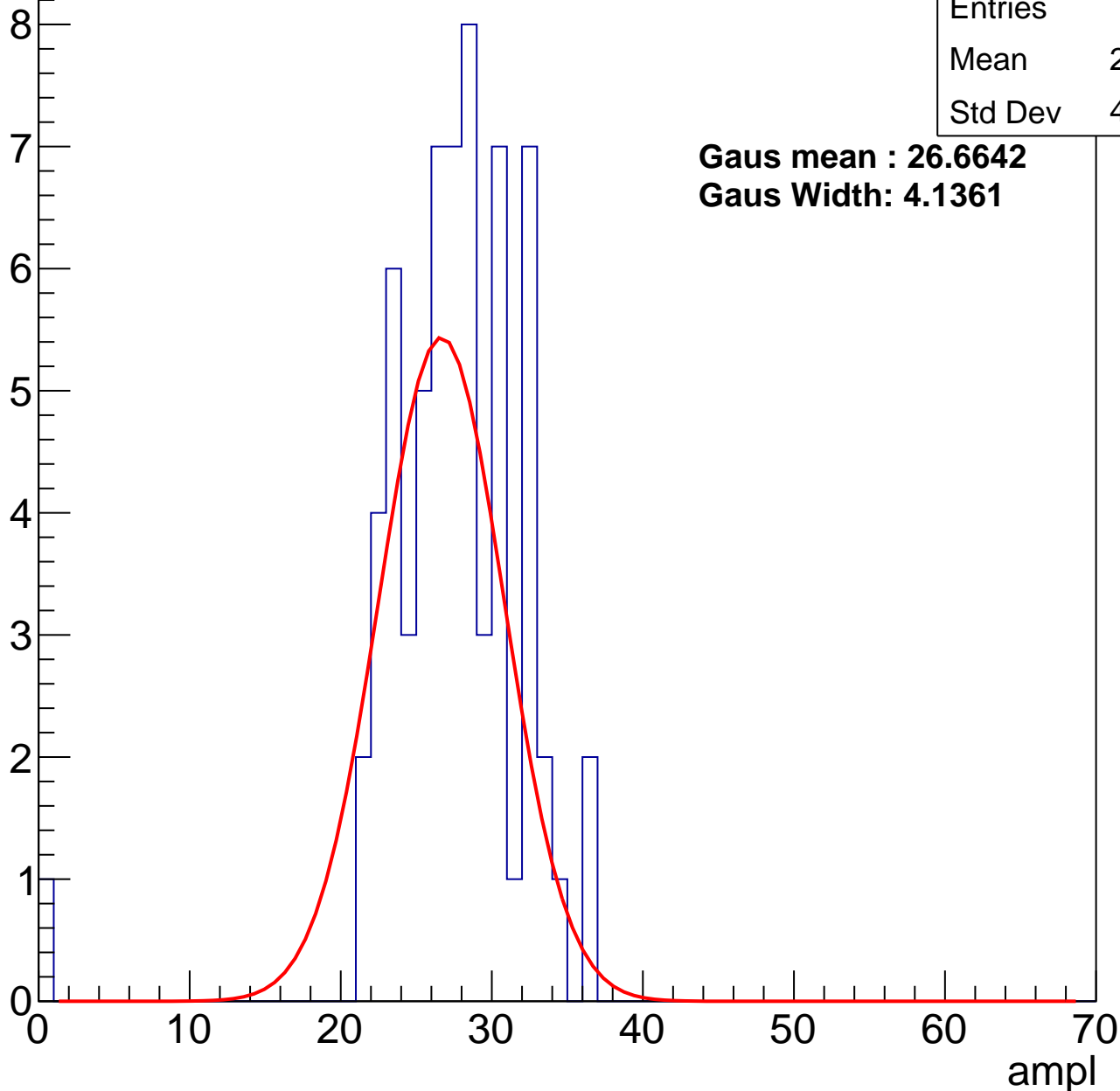
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	27.03
Std Dev	4.936

**Gaus mean : 26.6642**

**Gaus Width: 4.1361**



# B1L102S, U21-ch90, adc1

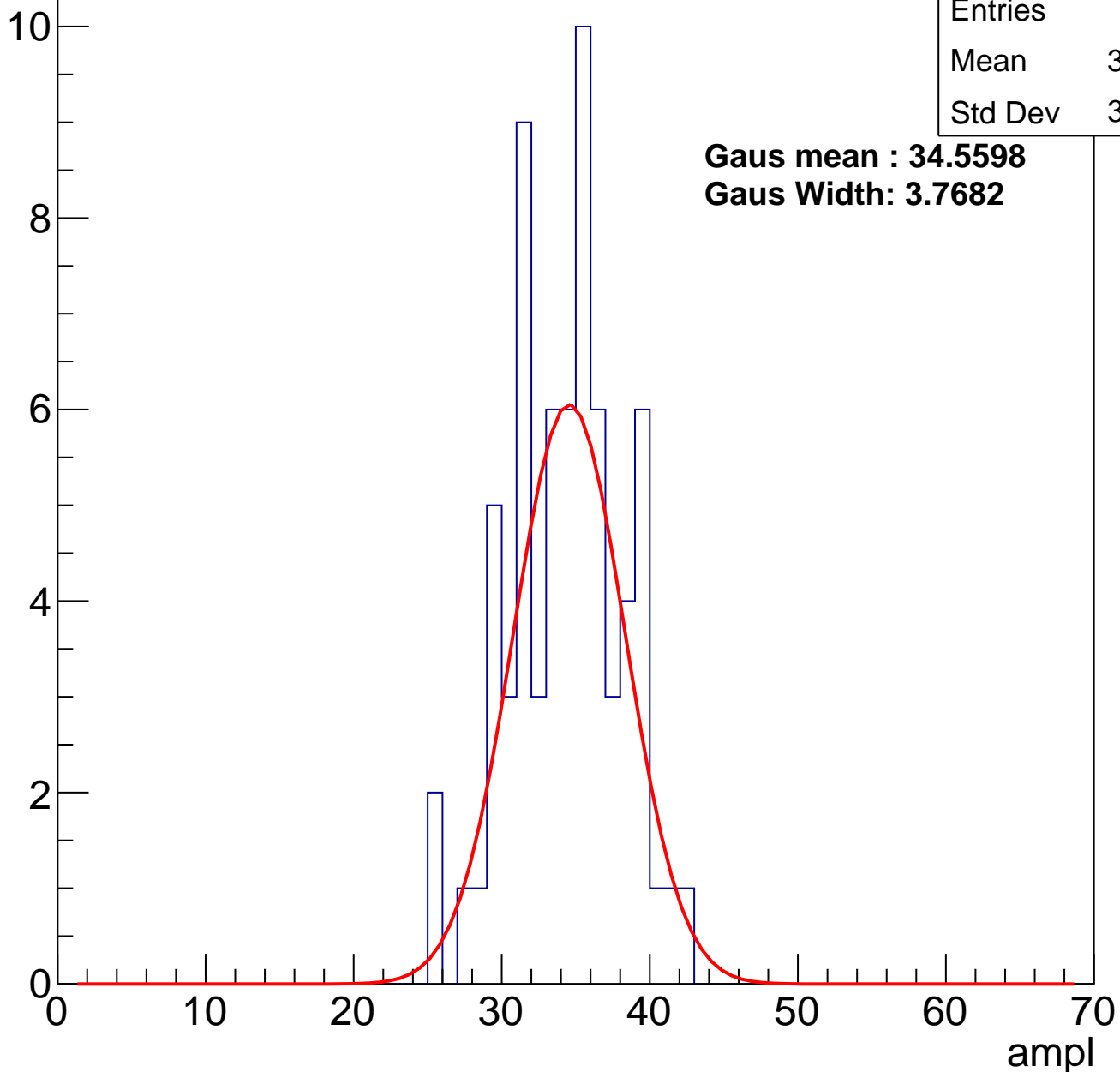
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	68
Mean	33.87
Std Dev	3.722

**Gaus mean : 34.5598**

**Gaus Width: 3.7682**

Entry



# B1L102S, U21-ch90, adc2

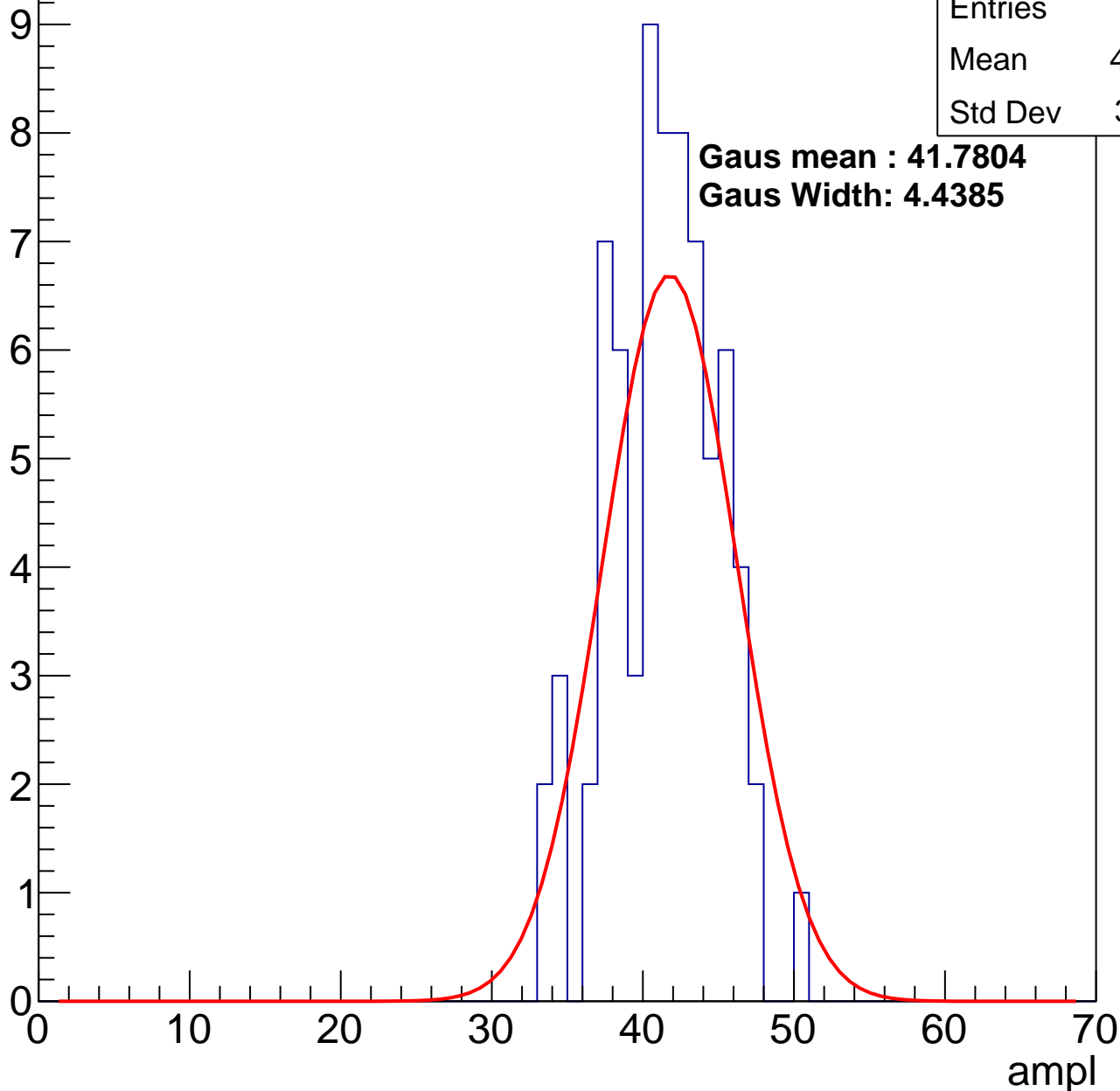
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	40.92
Std Dev	3.591

**Gaus mean : 41.7804**

**Gaus Width: 4.4385**

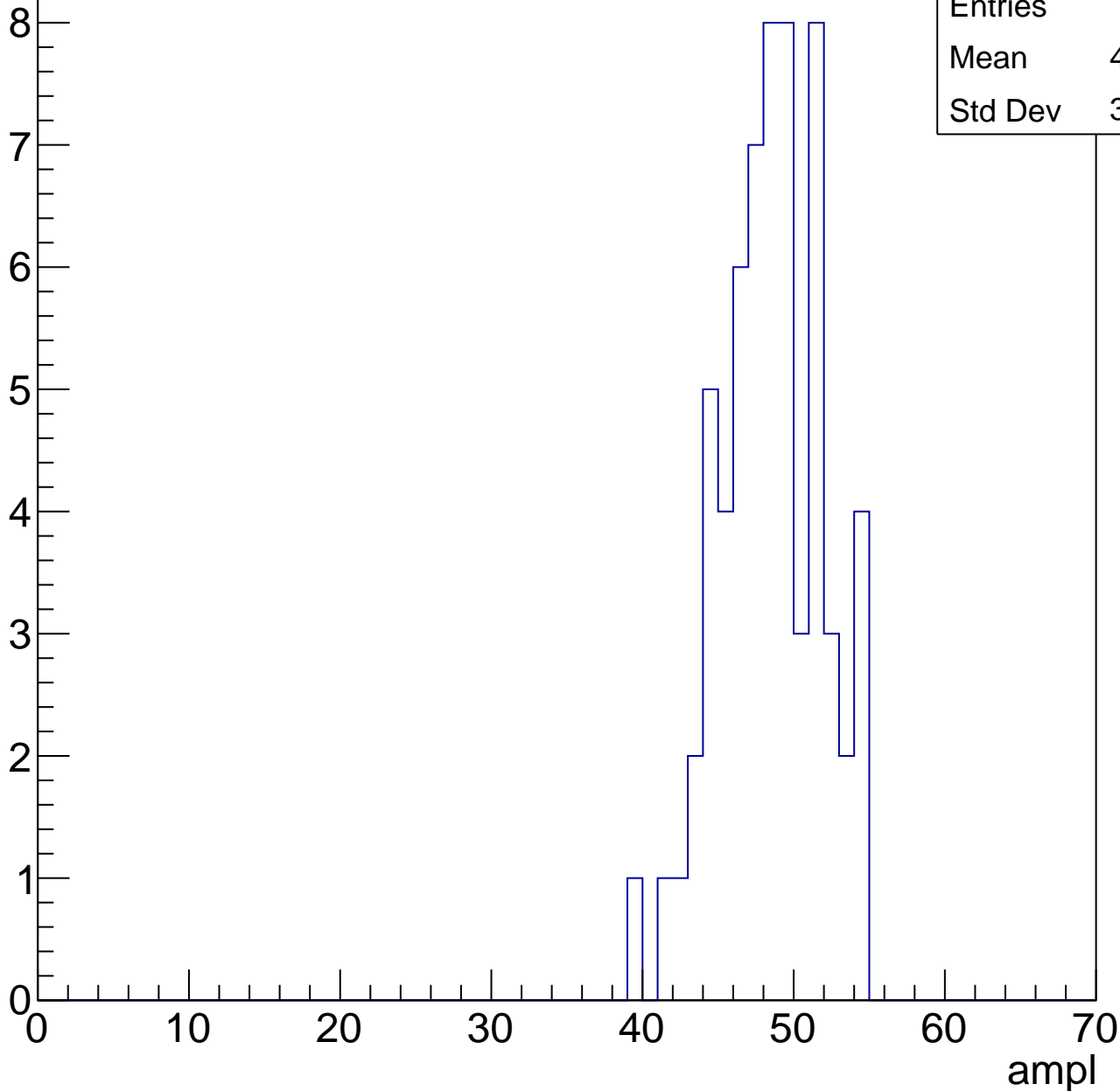


# B1L102S, U21-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	48.02
Std Dev	3.326

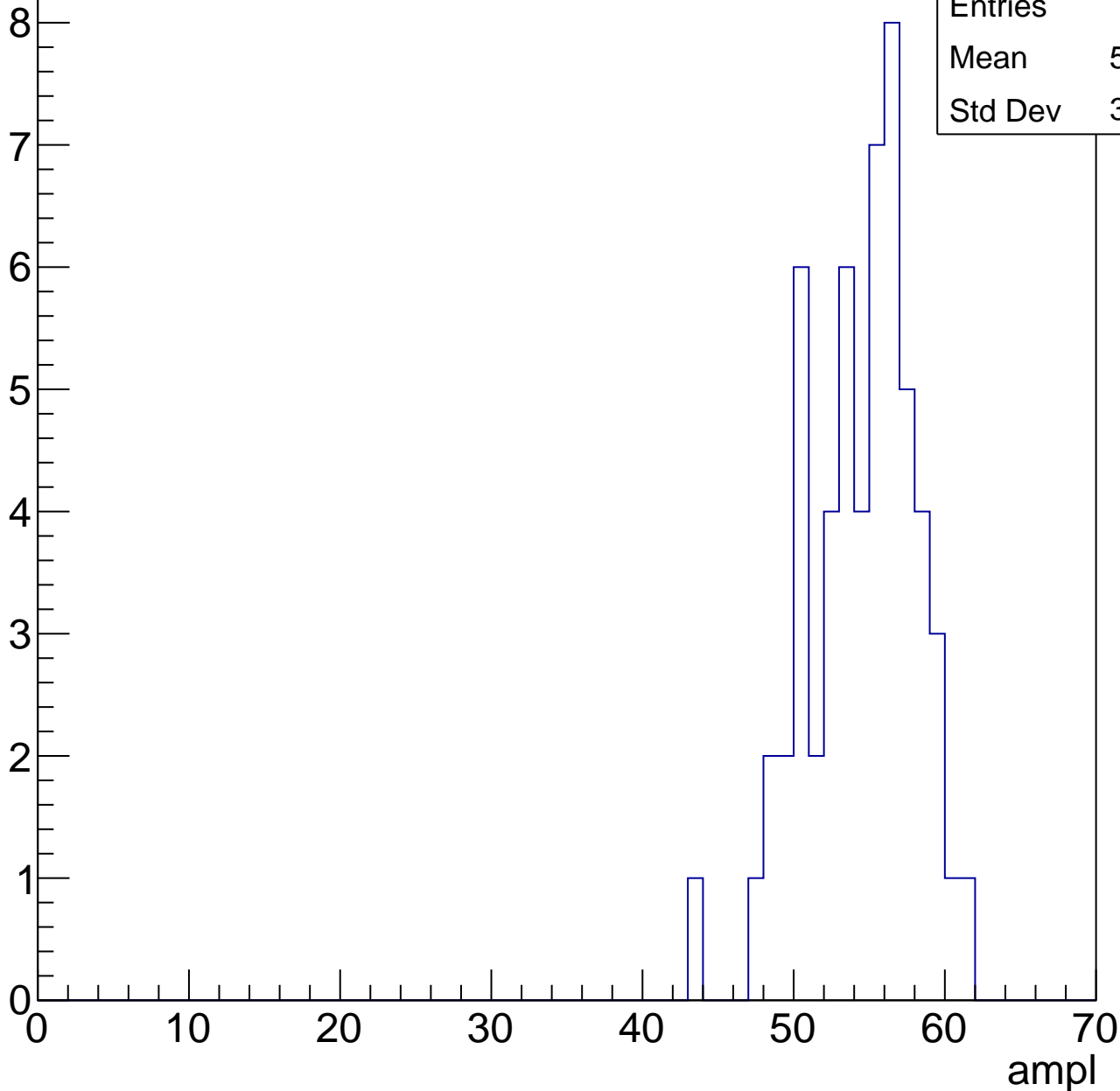


# B1L102S, U21-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

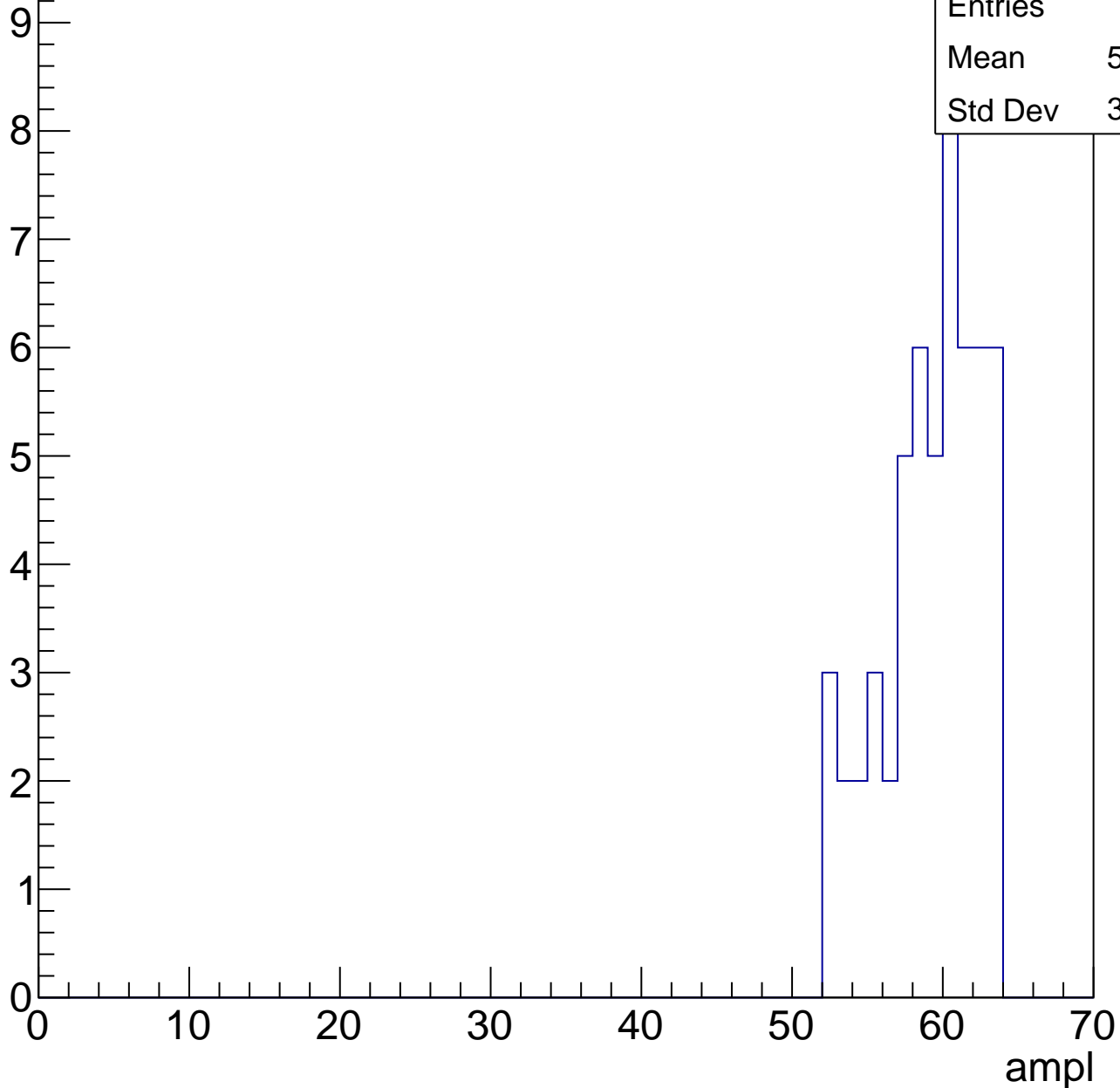
Entries	57
Mean	53.96
Std Dev	3.593



# B1L102S, U21-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

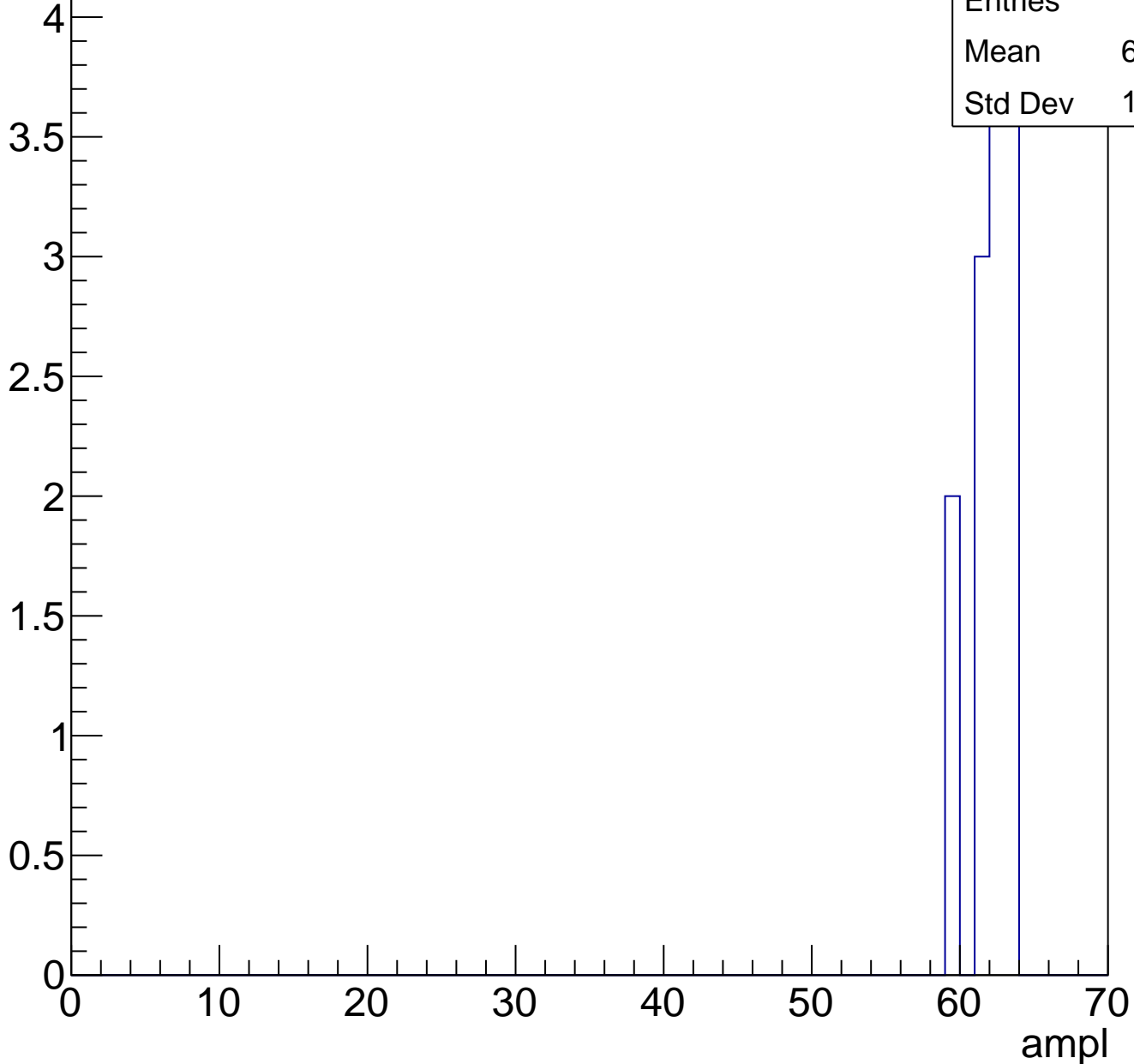
Entry



# B1L102S, U21-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U21-ch91, adc0

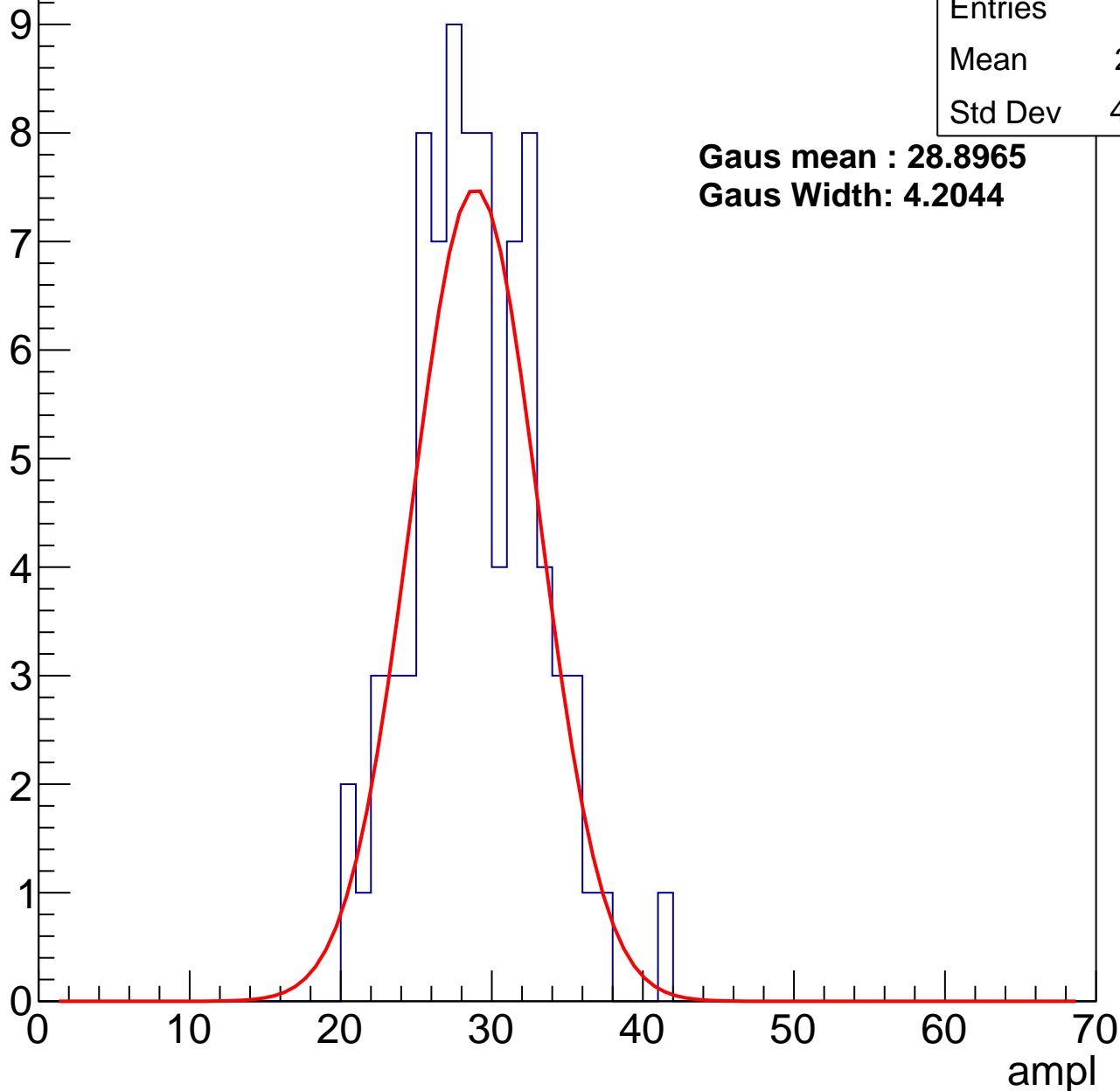
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	28.51
Std Dev	4.052

**Gaus mean : 28.8965**

**Gaus Width: 4.2044**



# B1L102S, U21-ch91, adc1

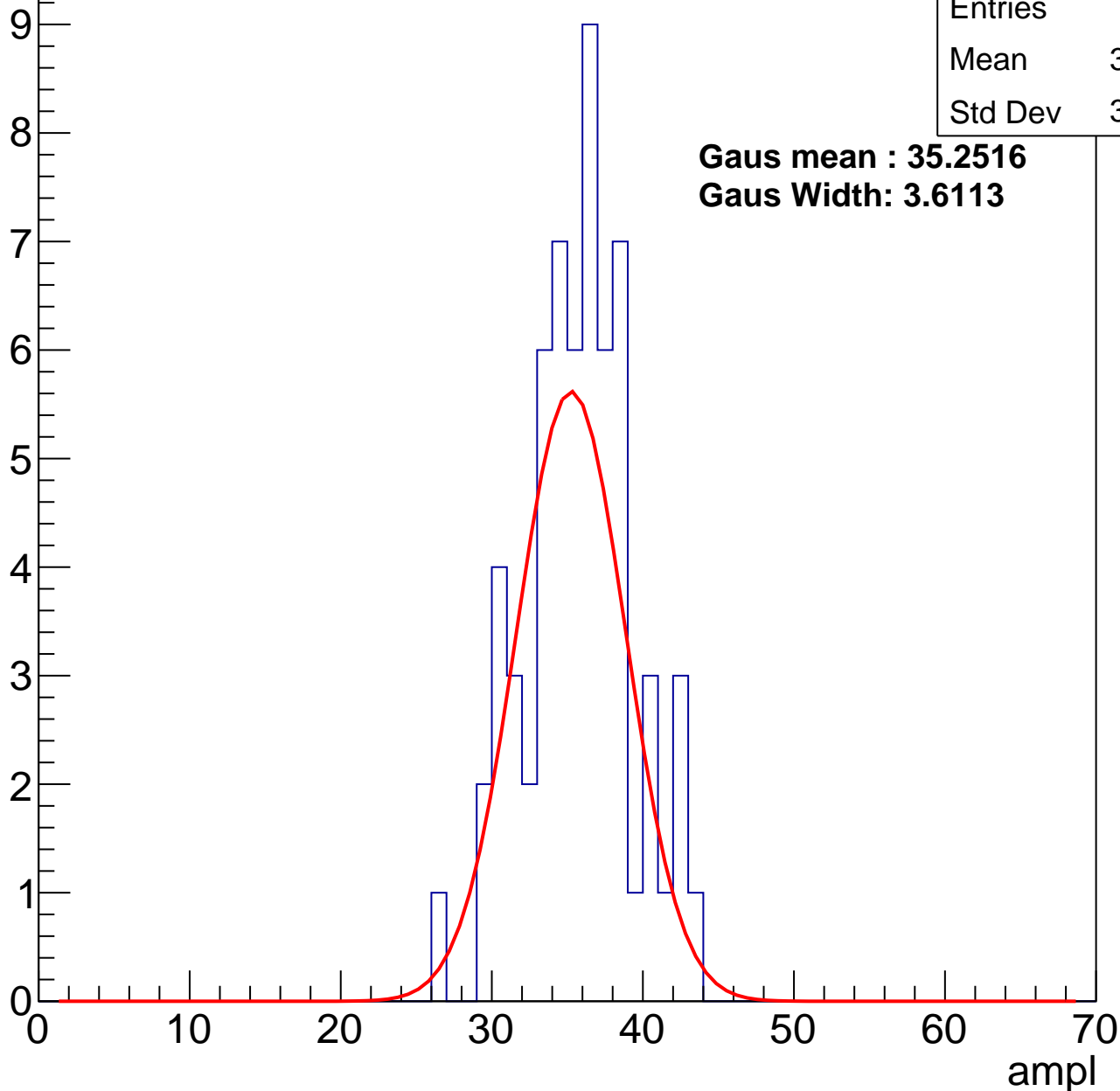
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	35.29
Std Dev	3.544

**Gaus mean : 35.2516**

**Gaus Width: 3.6113**



# B1L102S, U21-ch91, adc2

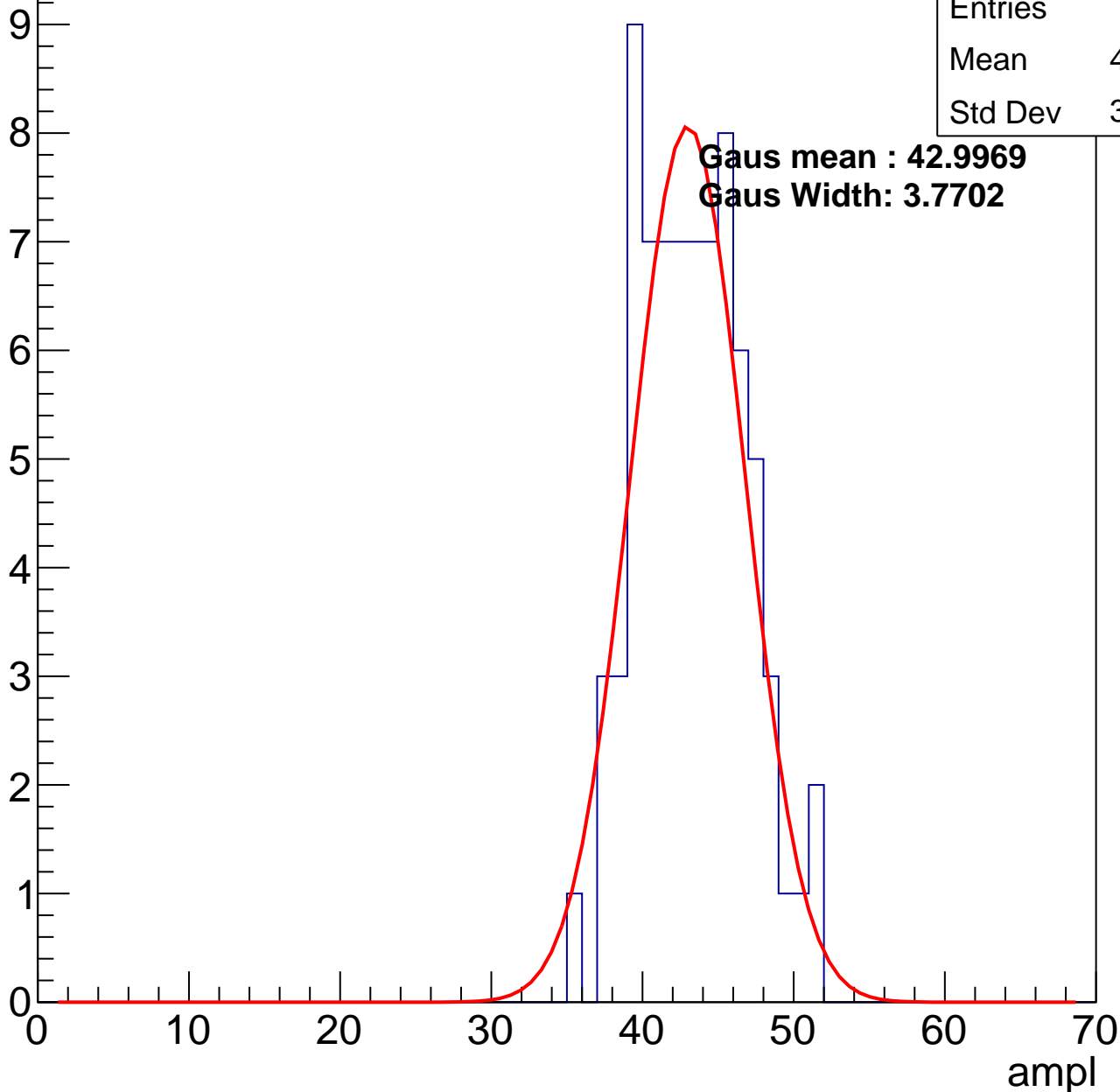
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	42.82
Std Dev	3.508

**Gaus mean : 42.9969**

**Gaus Width: 3.7702**

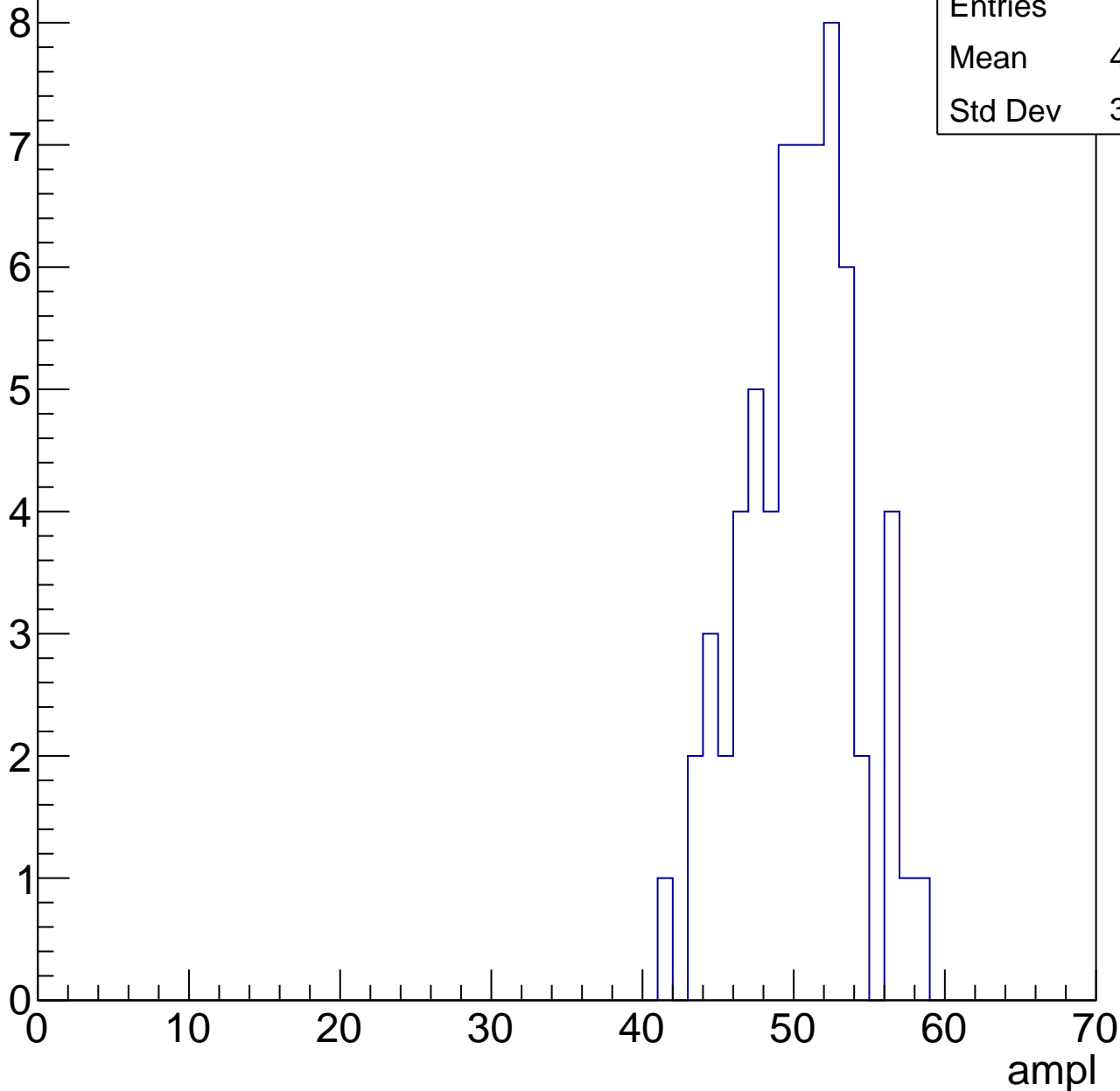


# B1L102S, U21-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	49.86
Std Dev	3.644



# B1L102S, U21-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	57
Mean	55.35
Std Dev	3.517

Entry

10

8

6

4

2

0

0

10

20

30

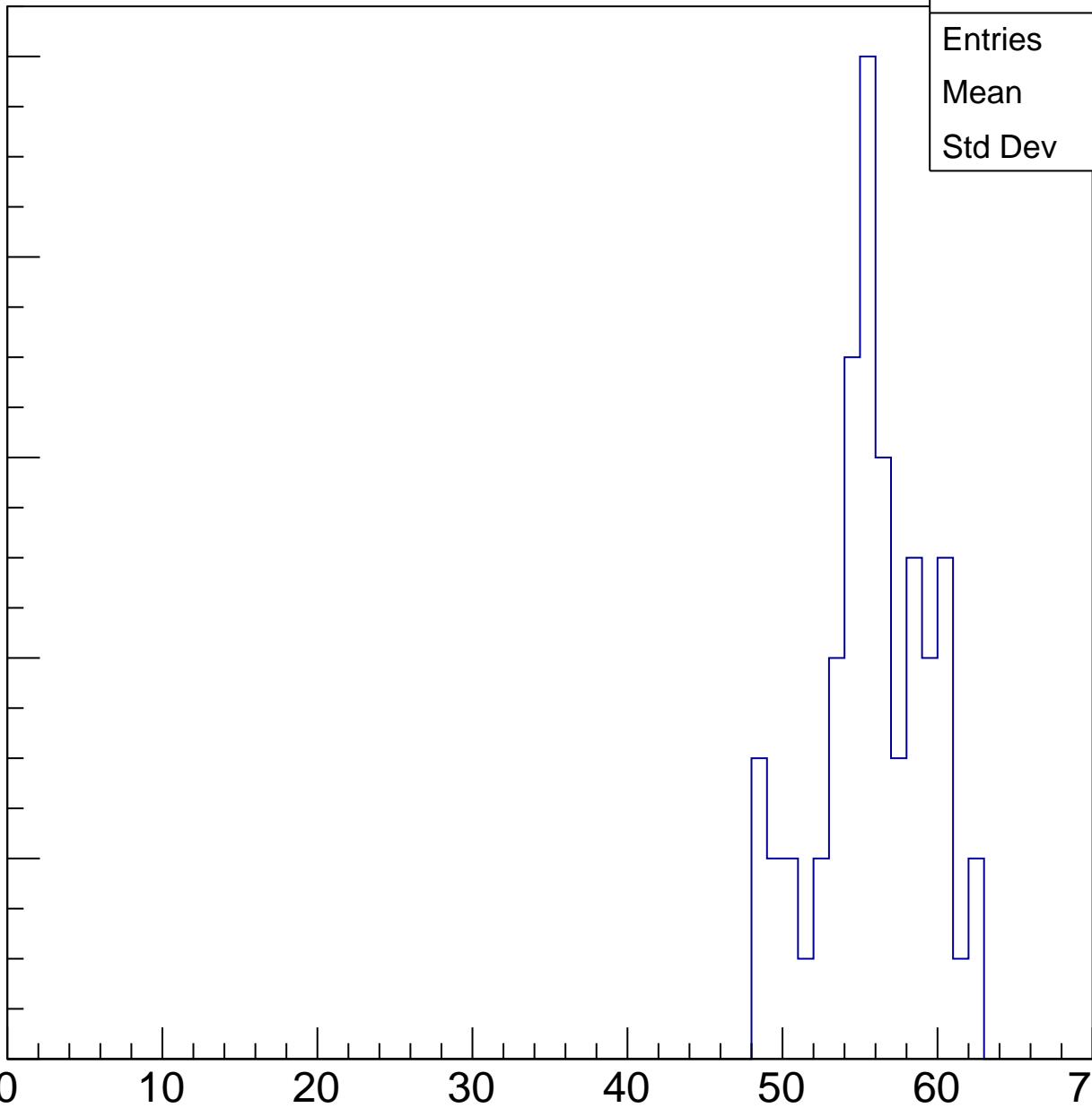
40

50

60

70

ampl

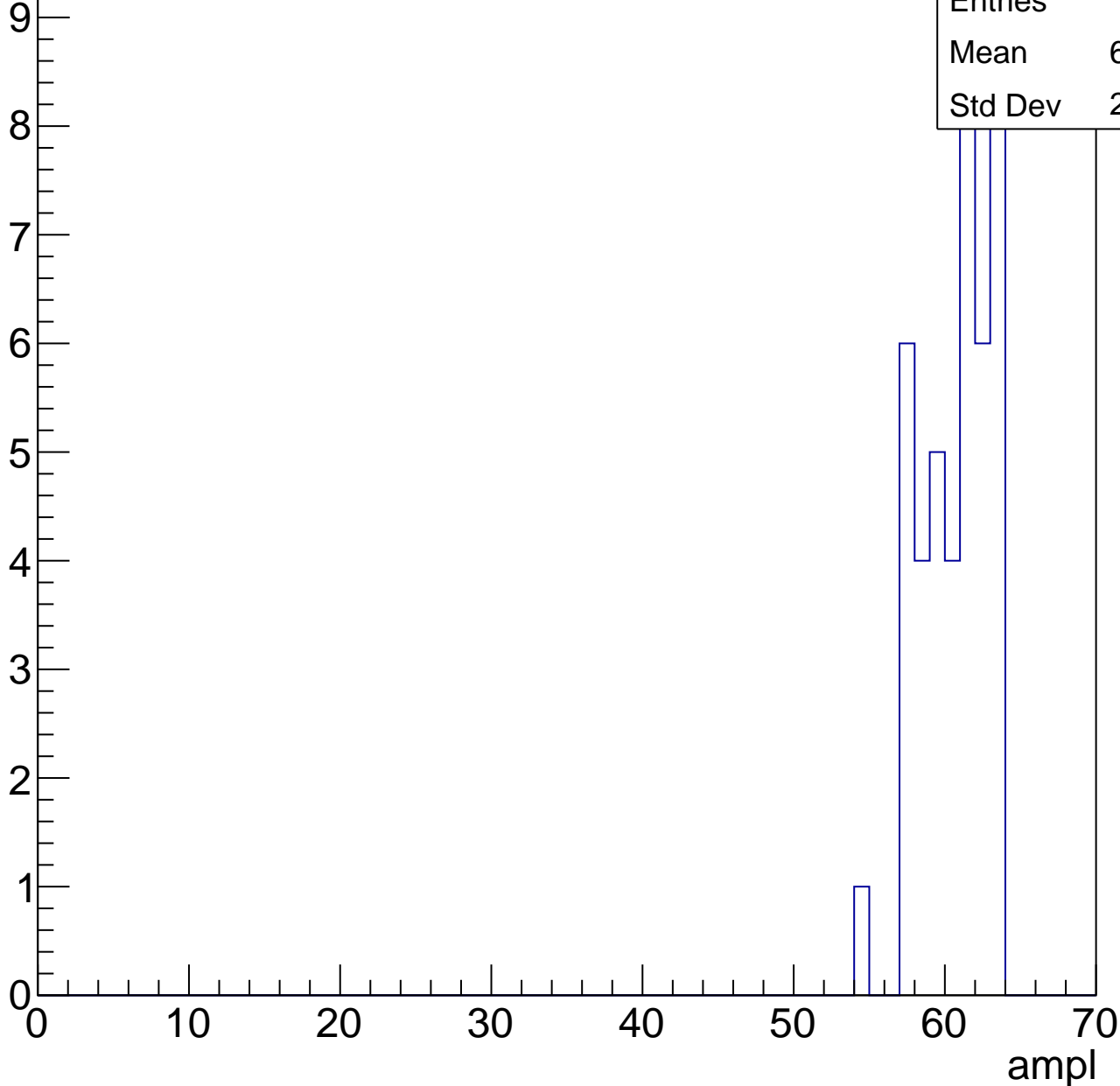


# B1L102S, U21-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	43
Mean	60.19
Std Dev	2.234



# B1L102S, U21-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

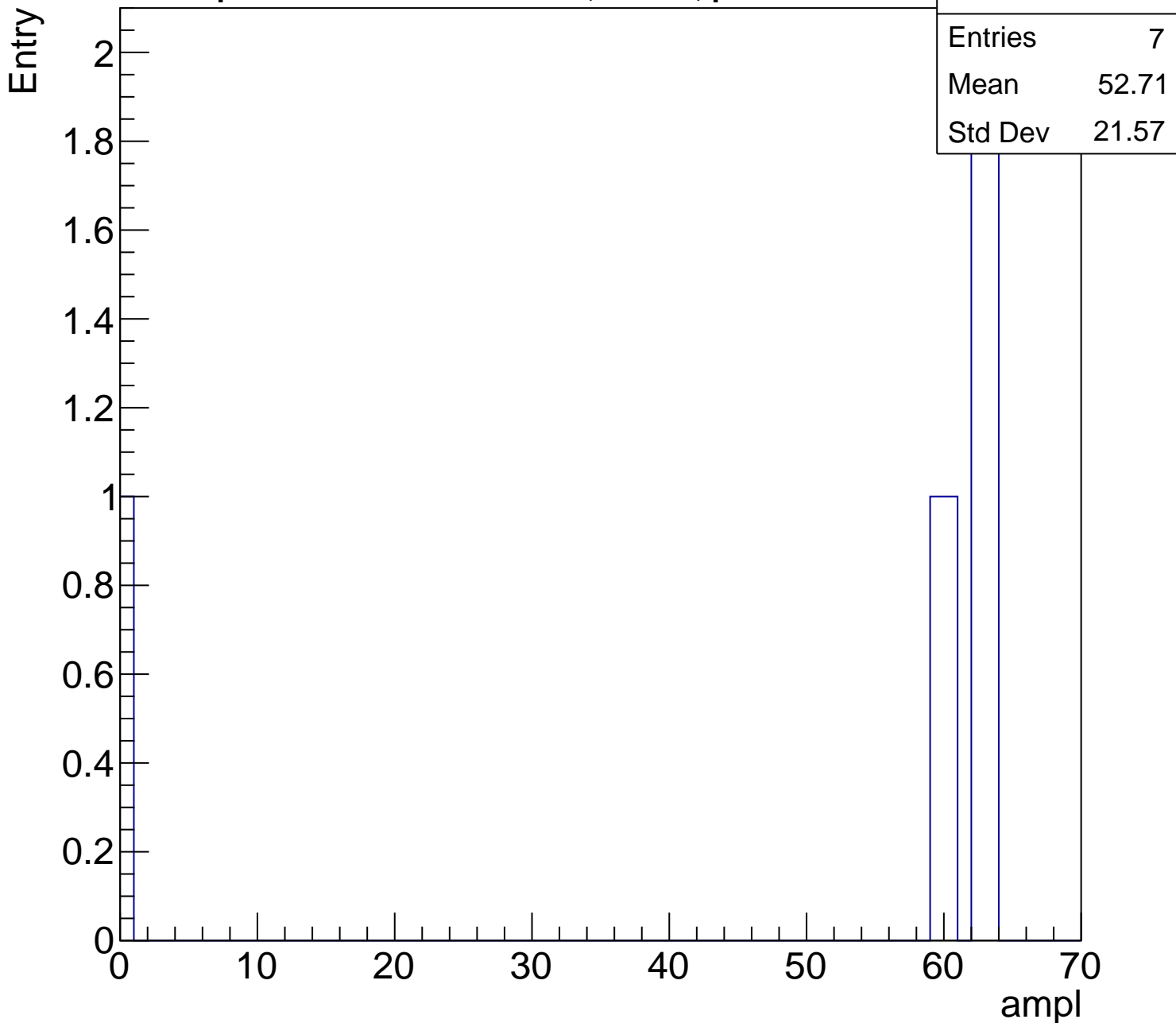
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	52.71
Std Dev	21.57

0 10 20 30 40 50 60 70

ampl





# B1L102S, U21-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch92, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	84
Mean	27.4
Std Dev	3.461

**Gaus mean : 27.9809**

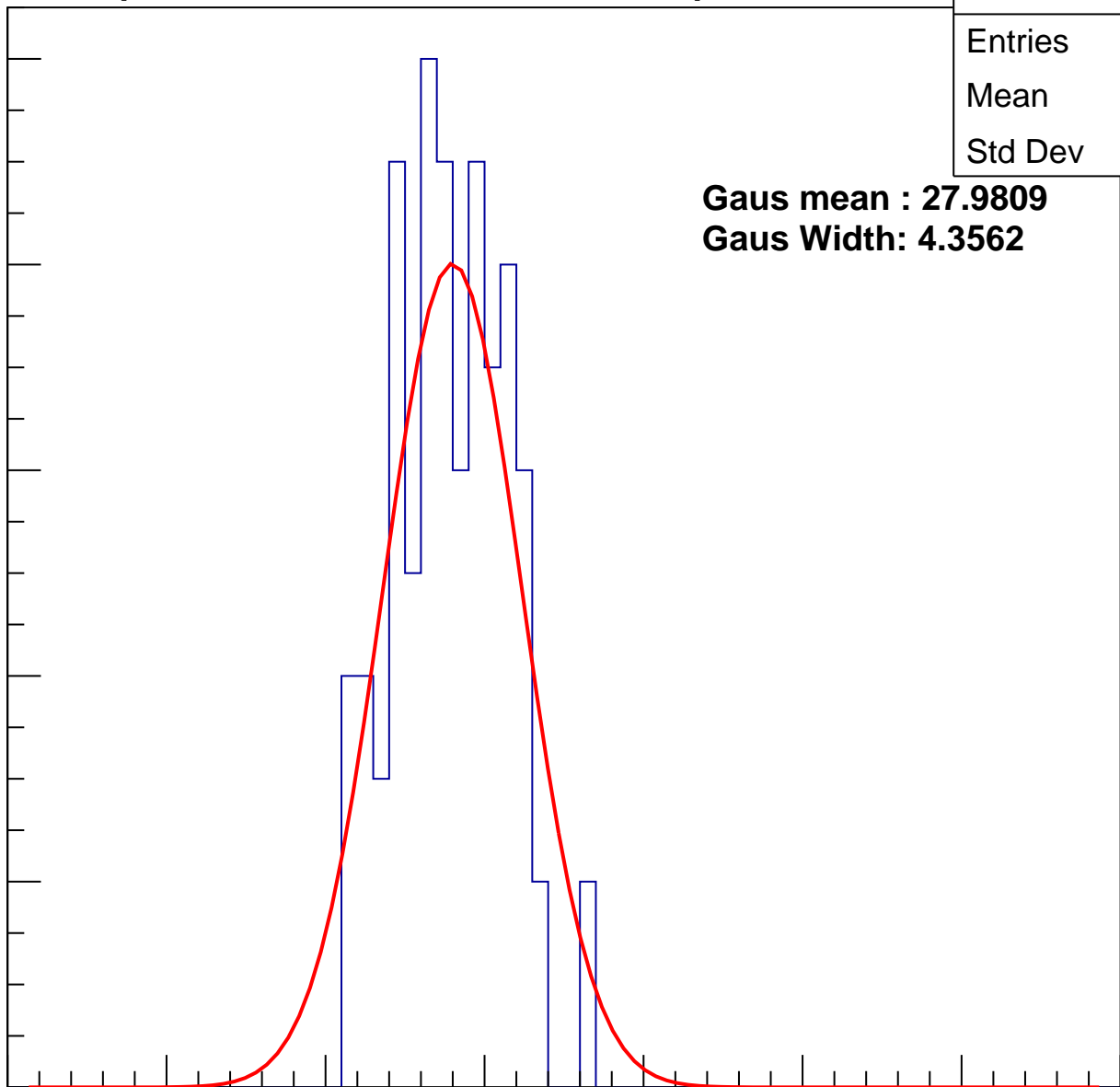
**Gaus Width: 4.3562**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U21-ch92, adc1

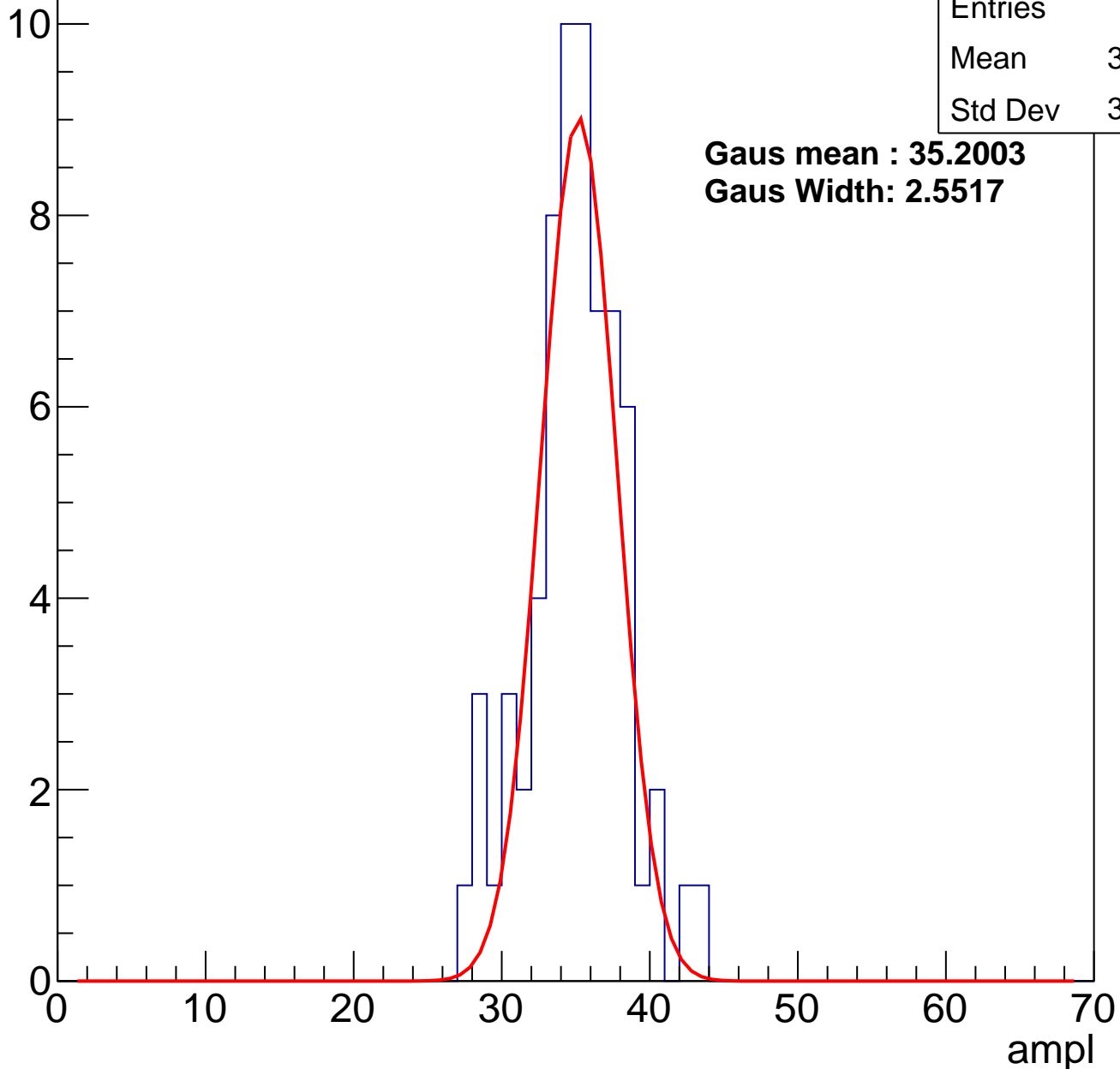
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	67
Mean	34.58
Std Dev	3.205

**Gaus mean : 35.2003**

**Gaus Width: 2.5517**

Entry



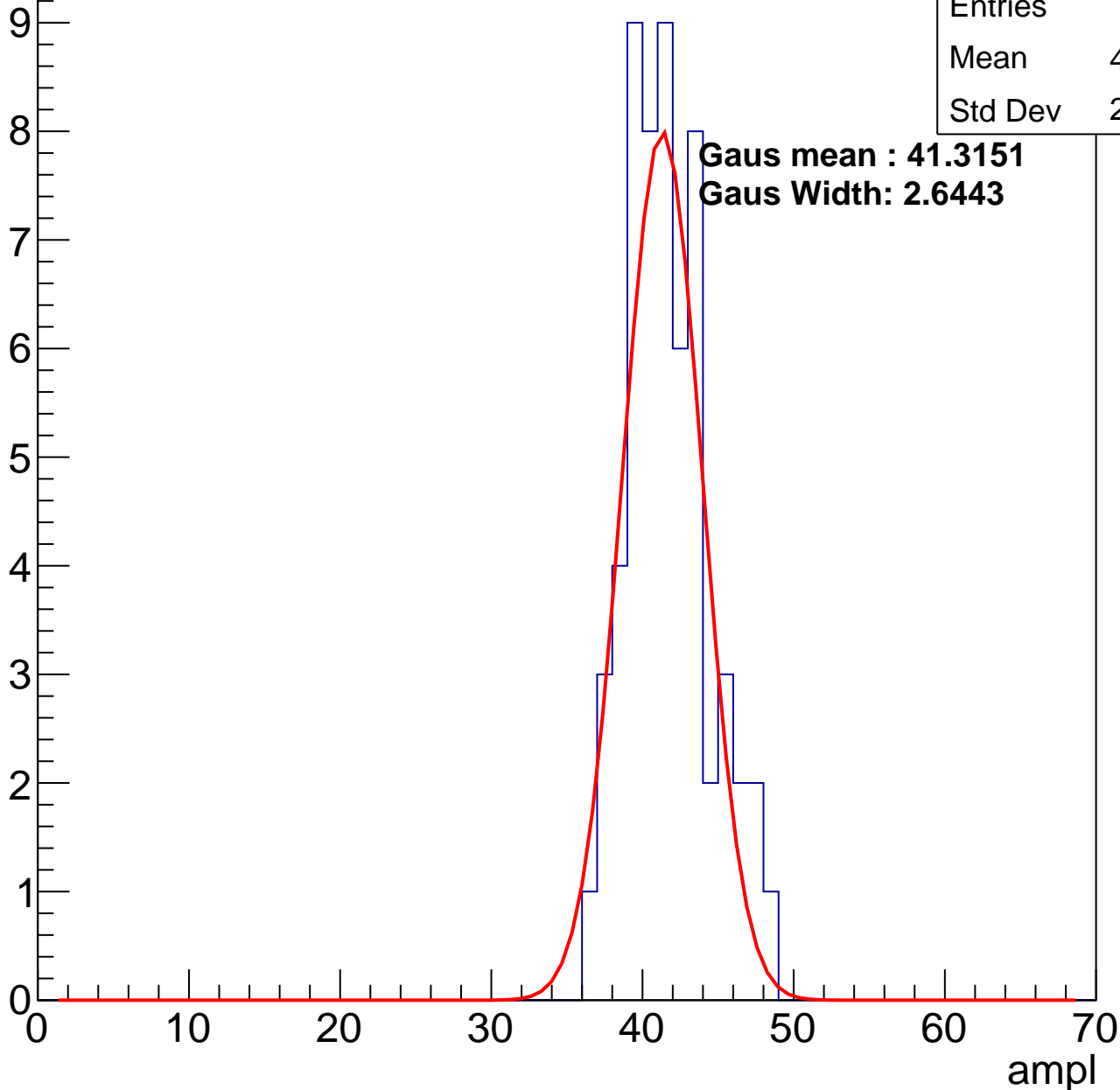
# B1L102S, U21-ch92, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	41.24
Std Dev	2.706

**Gaus mean : 41.3151**  
**Gaus Width: 2.6443**

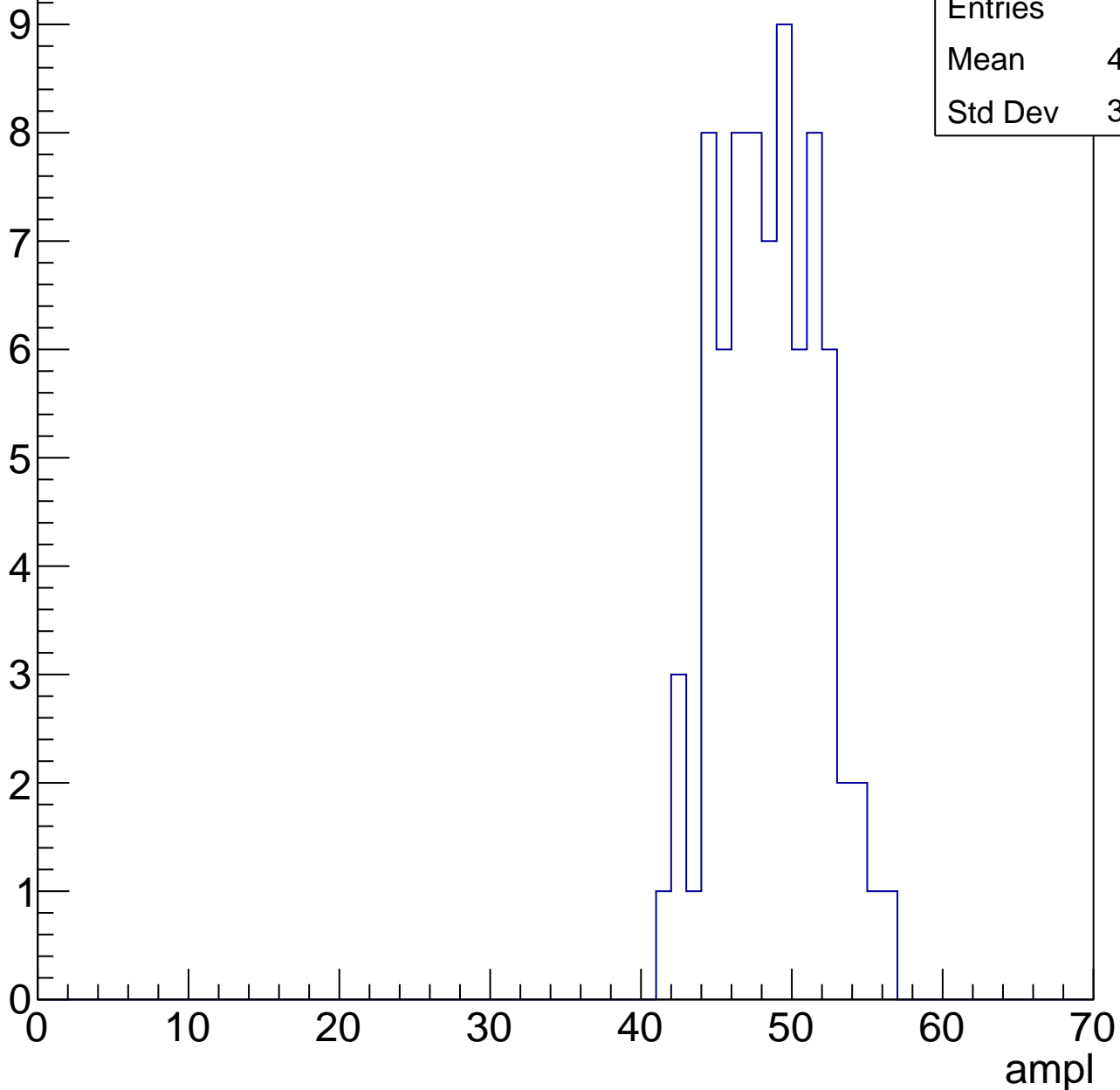


# B1L102S, U21-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	48.03
Std Dev	3.303

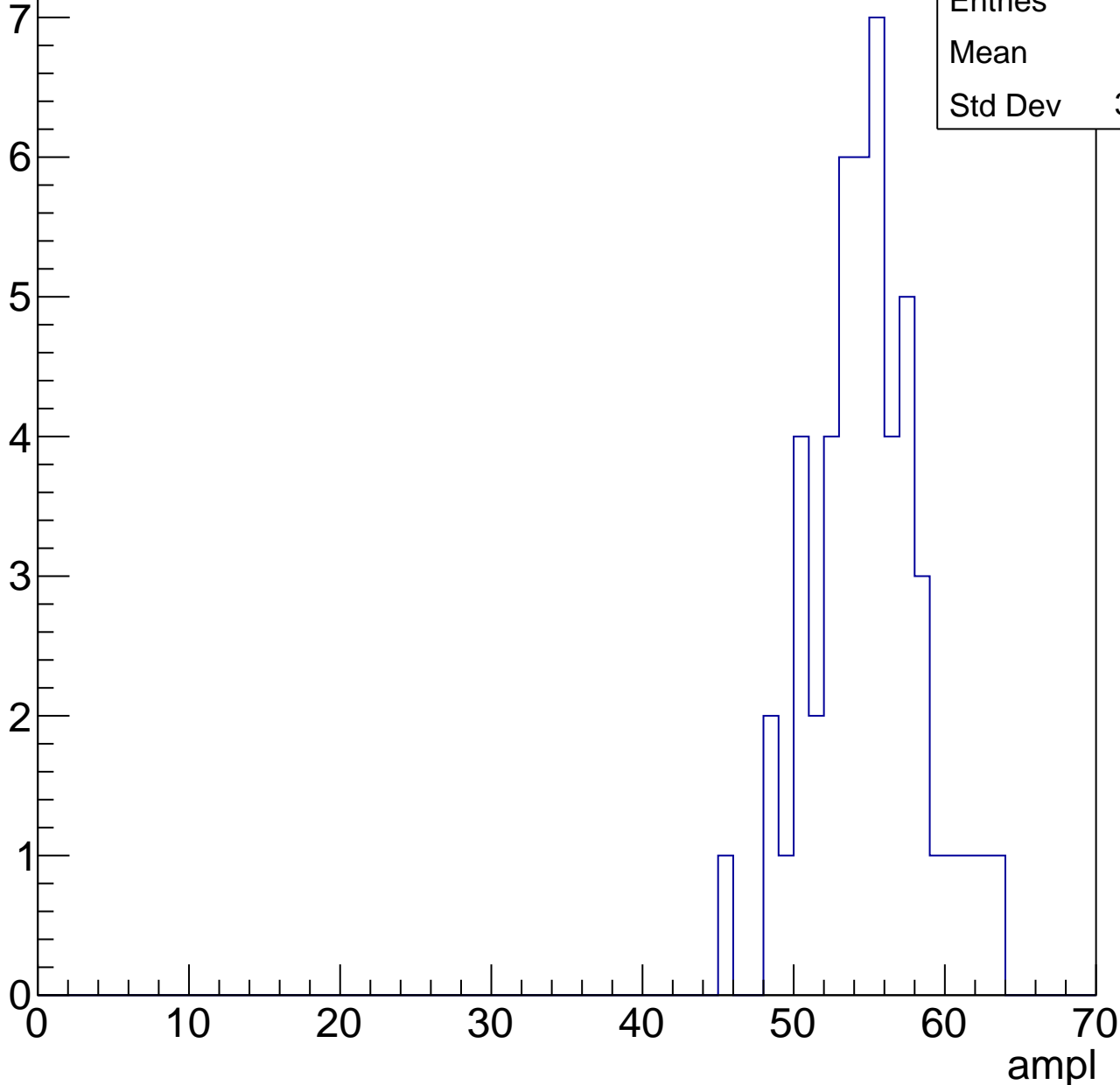


# B1L102S, U21-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

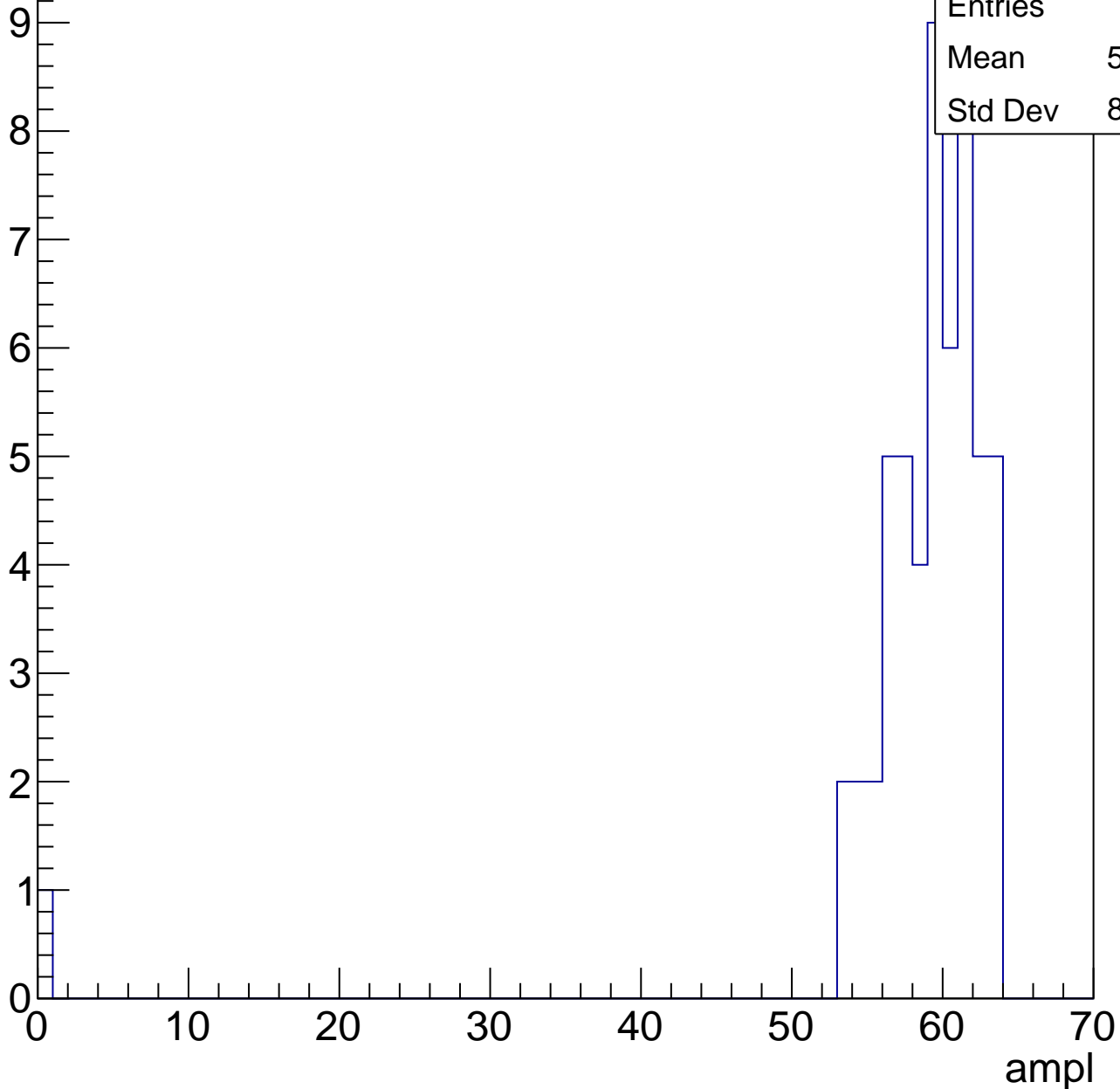
Entries	50
Mean	54.3
Std Dev	3.601



# B1L102S, U21-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

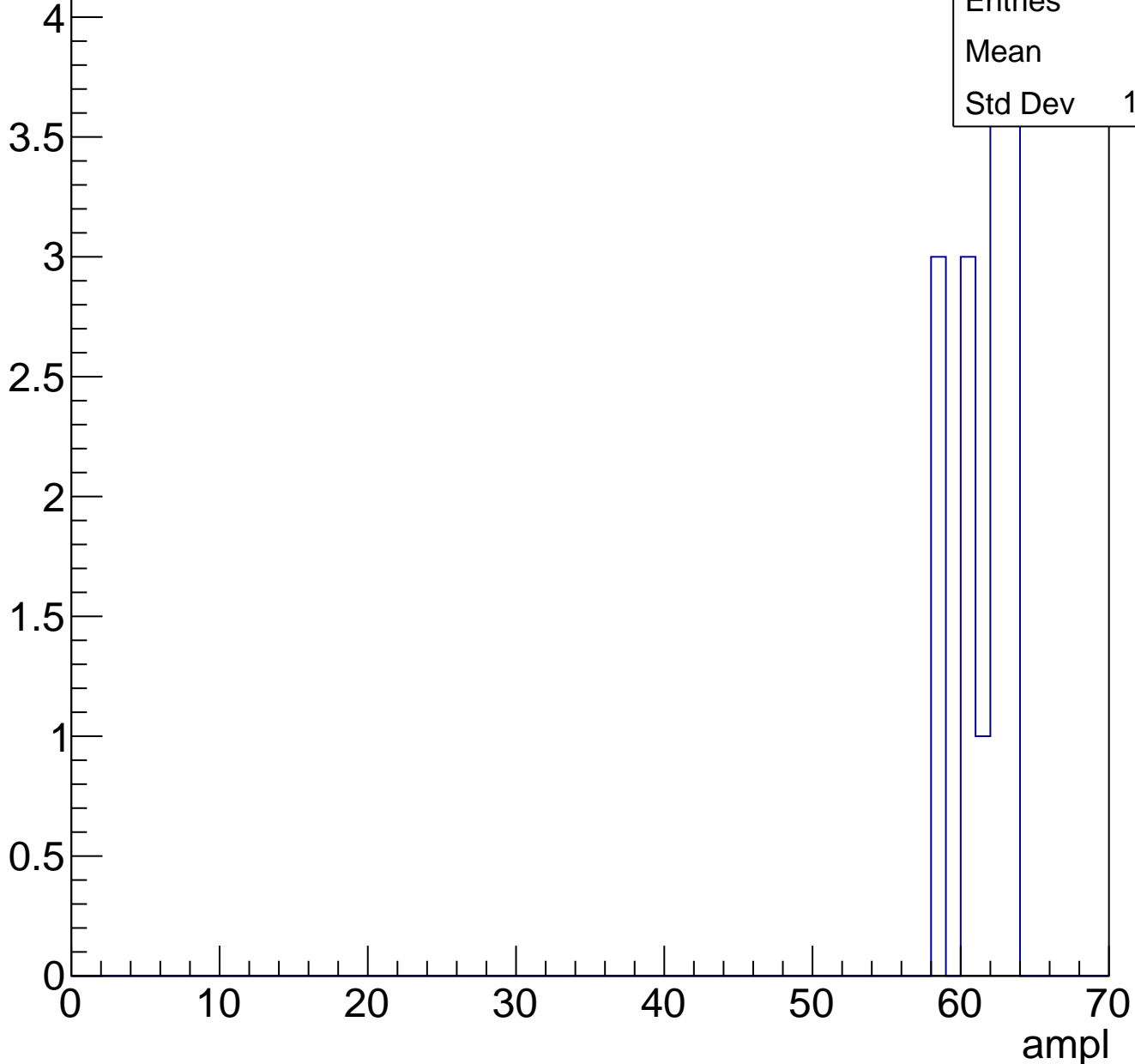
Entry



# B1L102S, U21-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch93, adc0

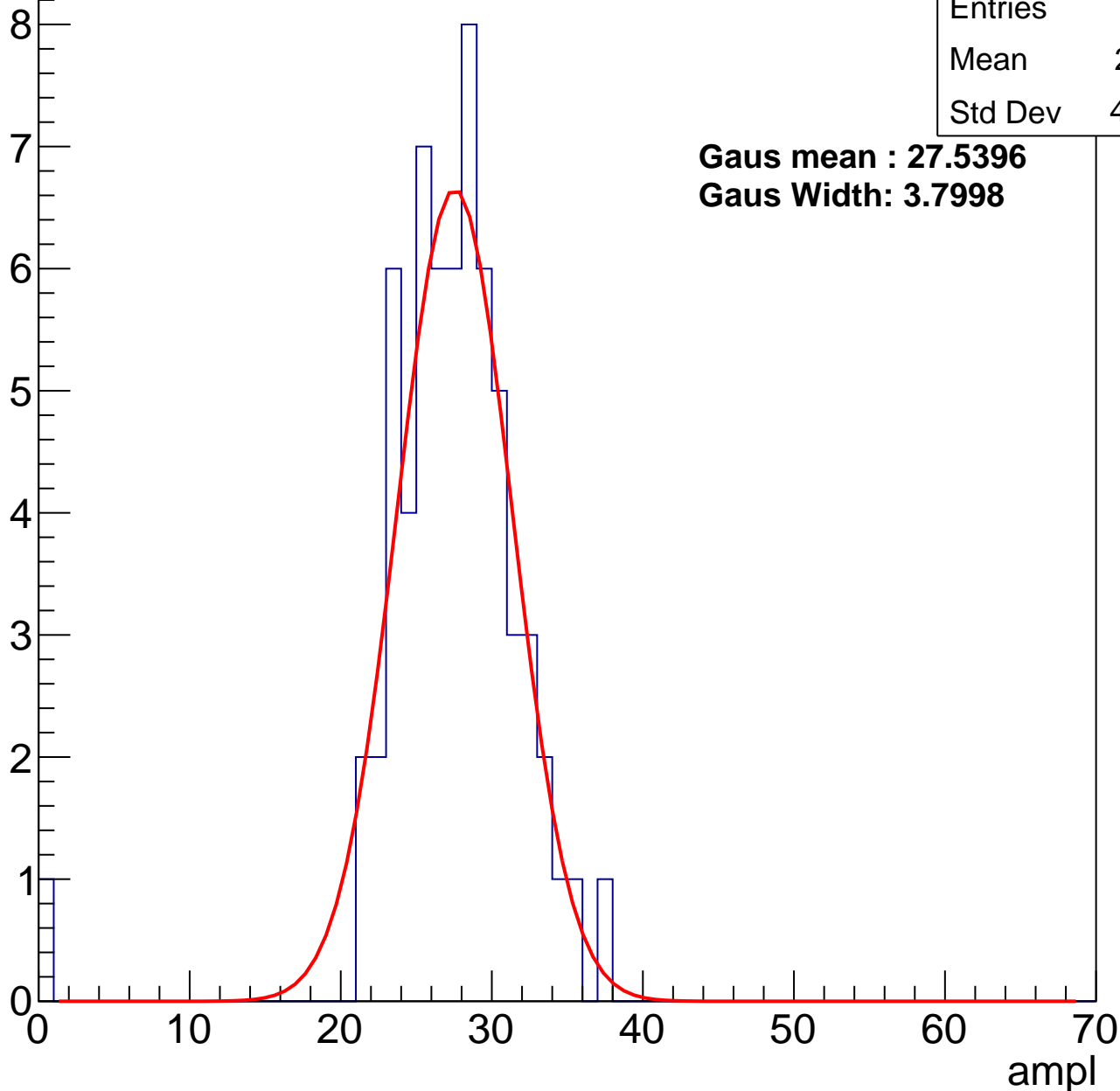
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	26.91
Std Dev	4.844

**Gaus mean : 27.5396**

**Gaus Width: 3.7998**



# B1L102S, U21-ch93, adc1

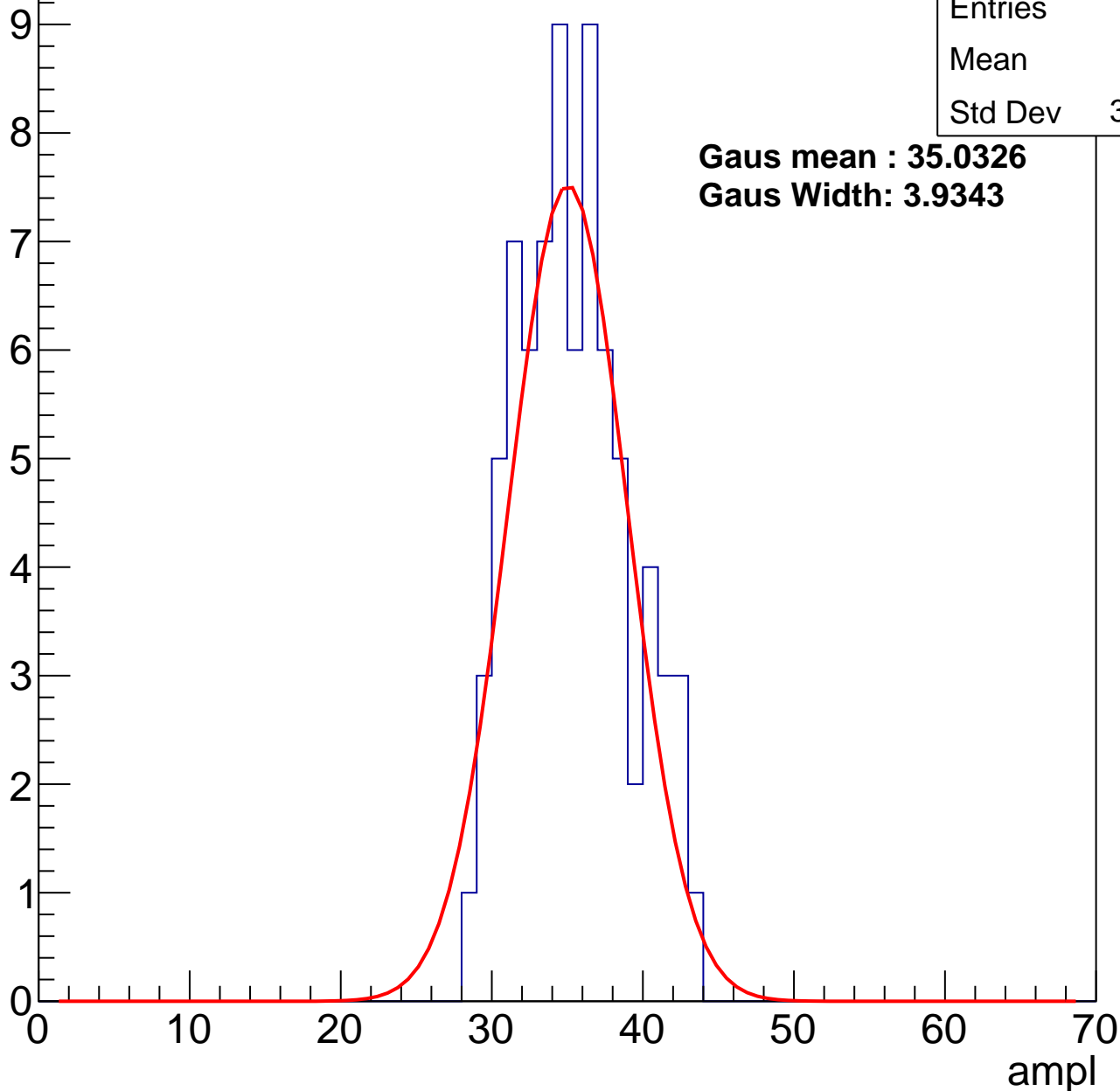
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	34.9
Std Dev	3.627

**Gaus mean : 35.0326**

**Gaus Width: 3.9343**



# B1L102S, U21-ch93, adc2

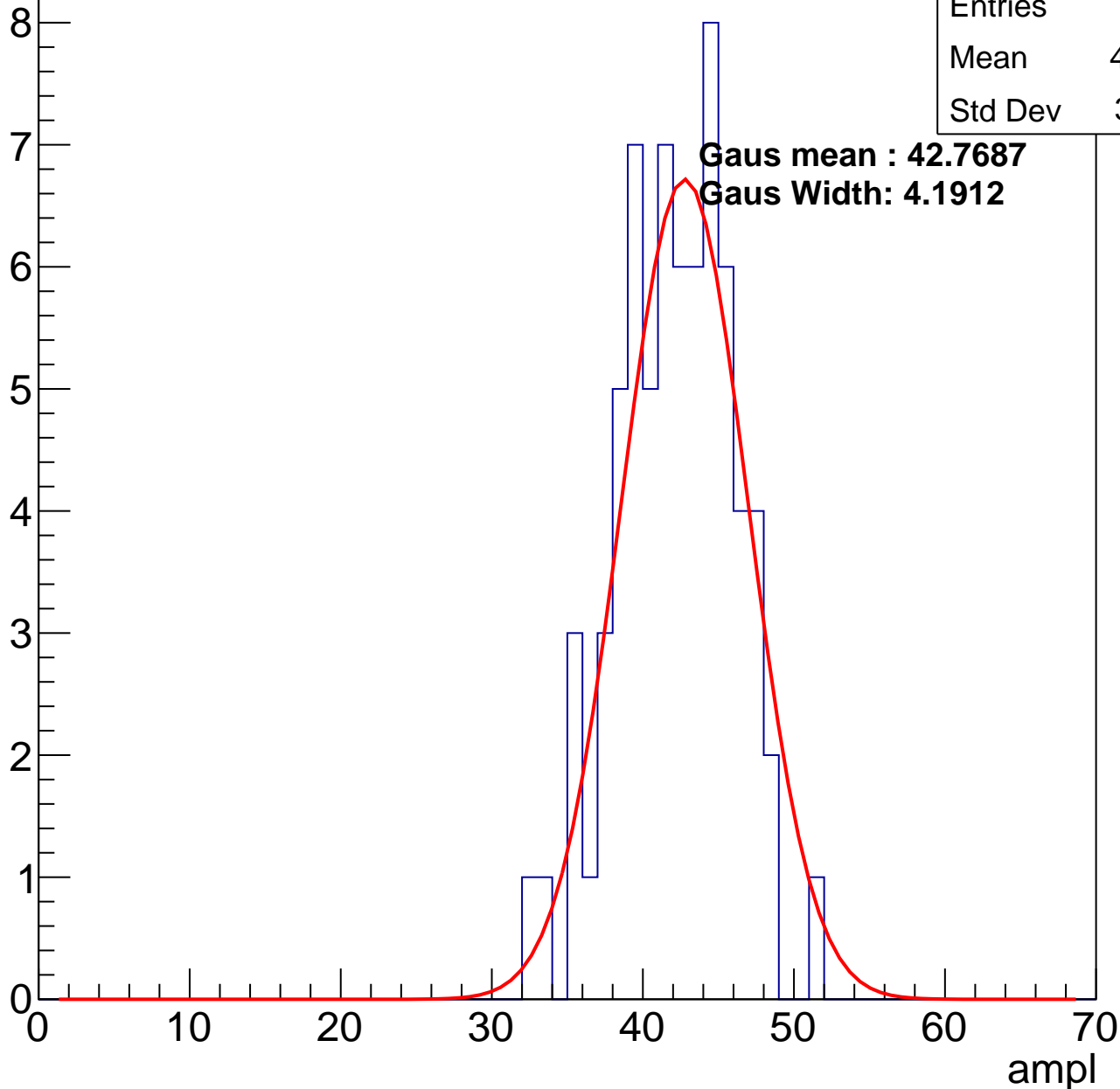
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	41.69
Std Dev	3.801

**Gaus mean : 42.7687**

**Gaus Width: 4.1912**

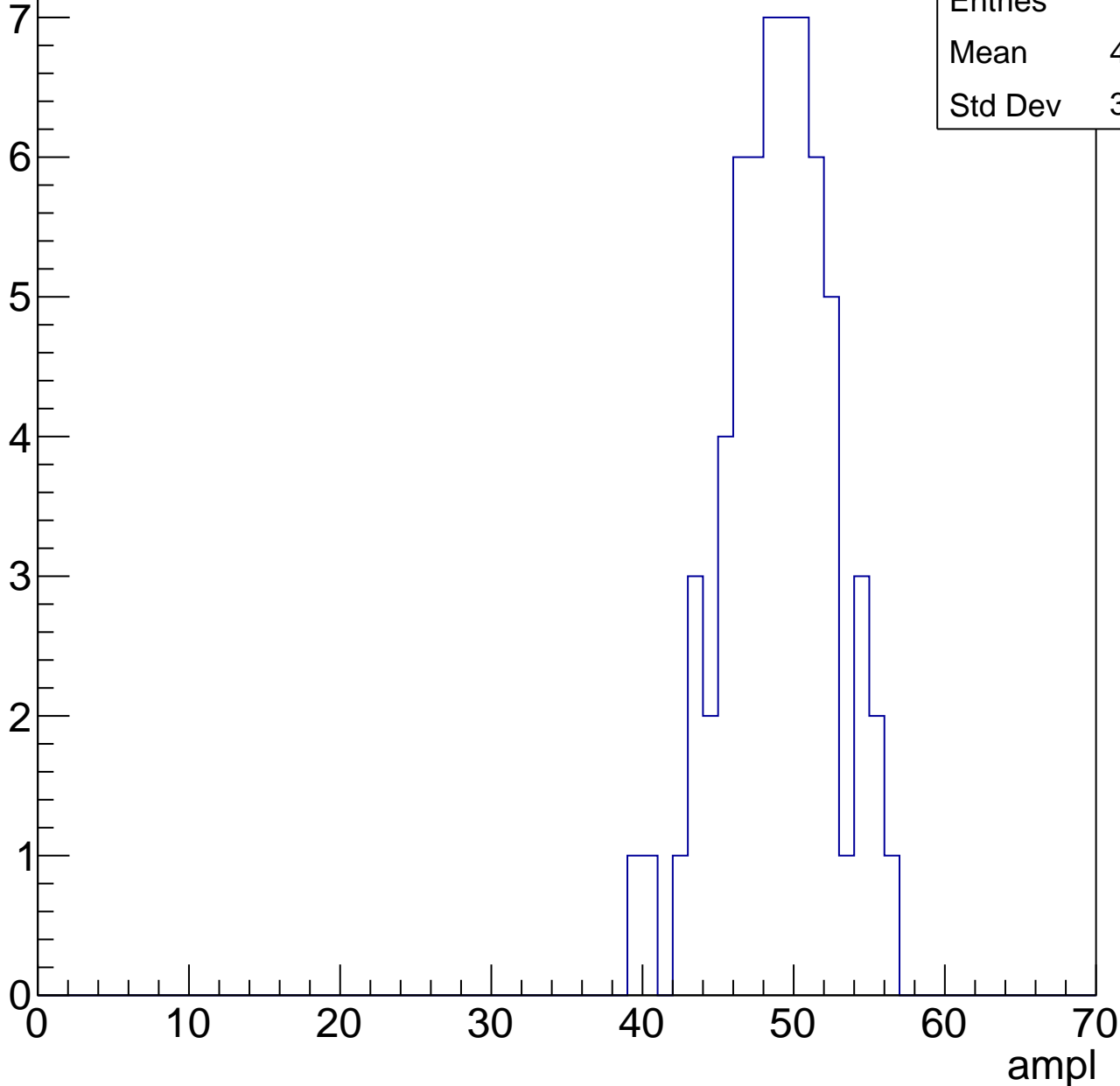


# B1L102S, U21-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	48.44
Std Dev	3.576

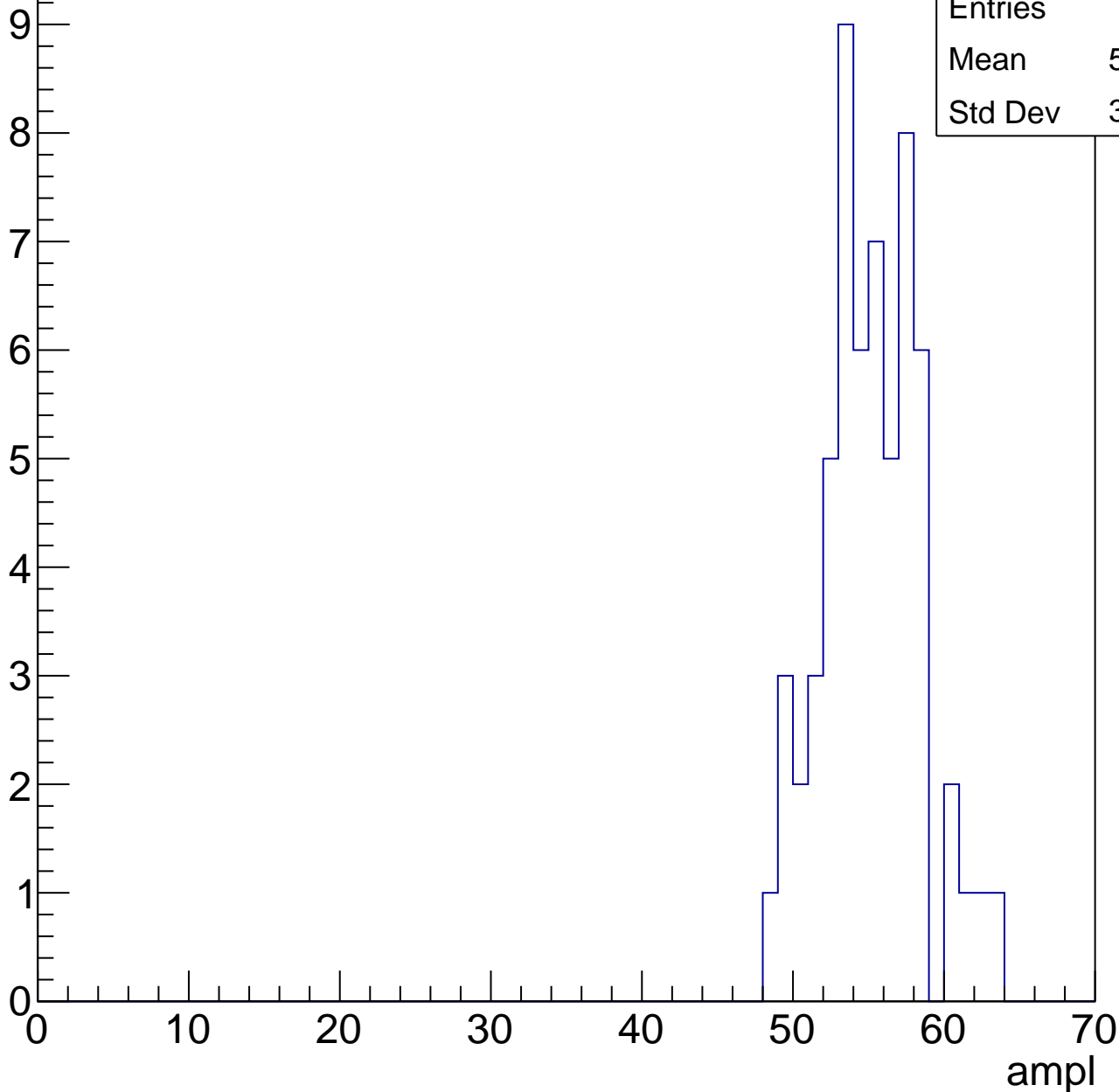


# B1L102S, U21-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	54.73
Std Dev	3.235

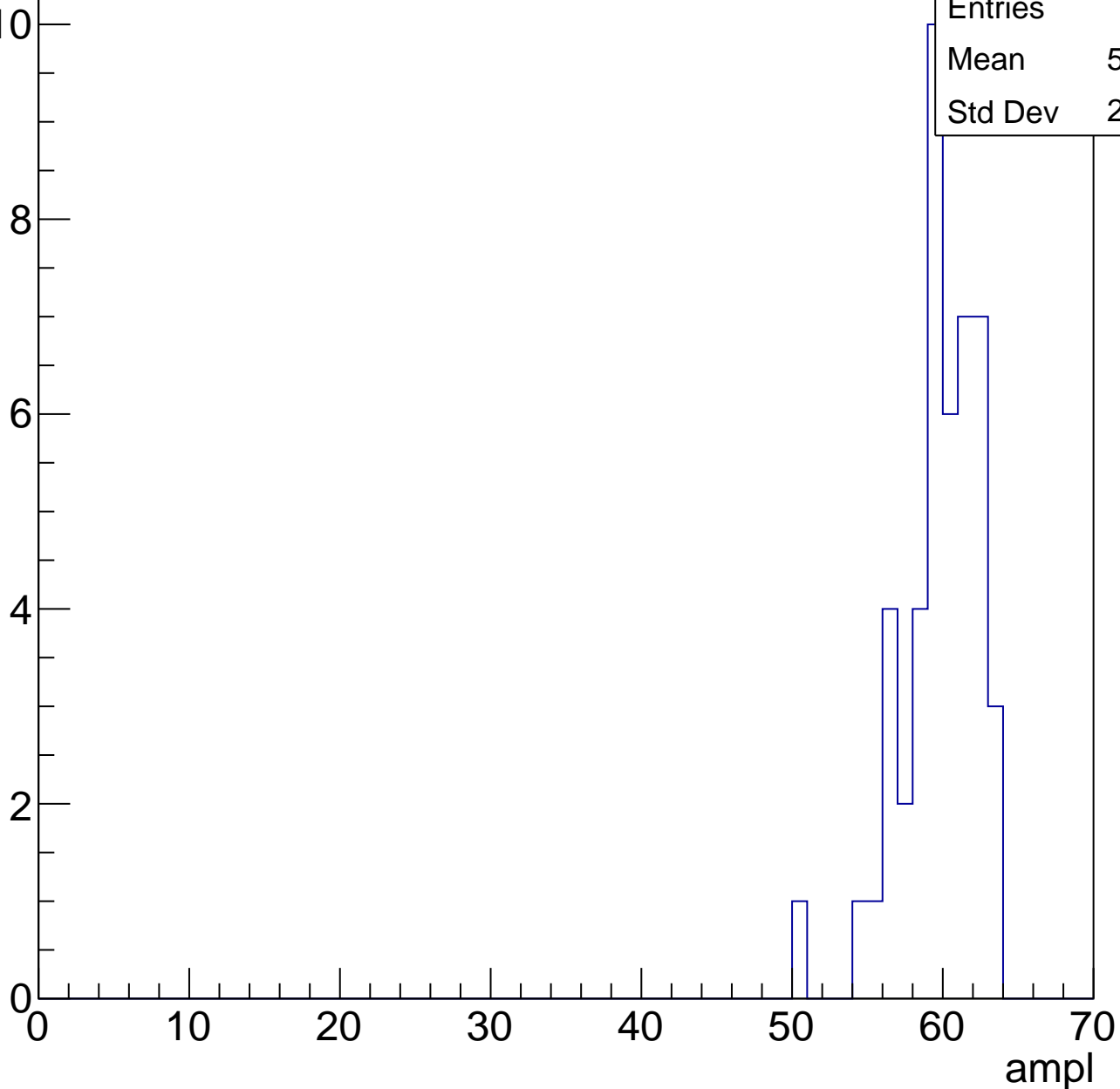


# B1L102S, U21-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	59.33
Std Dev	2.596

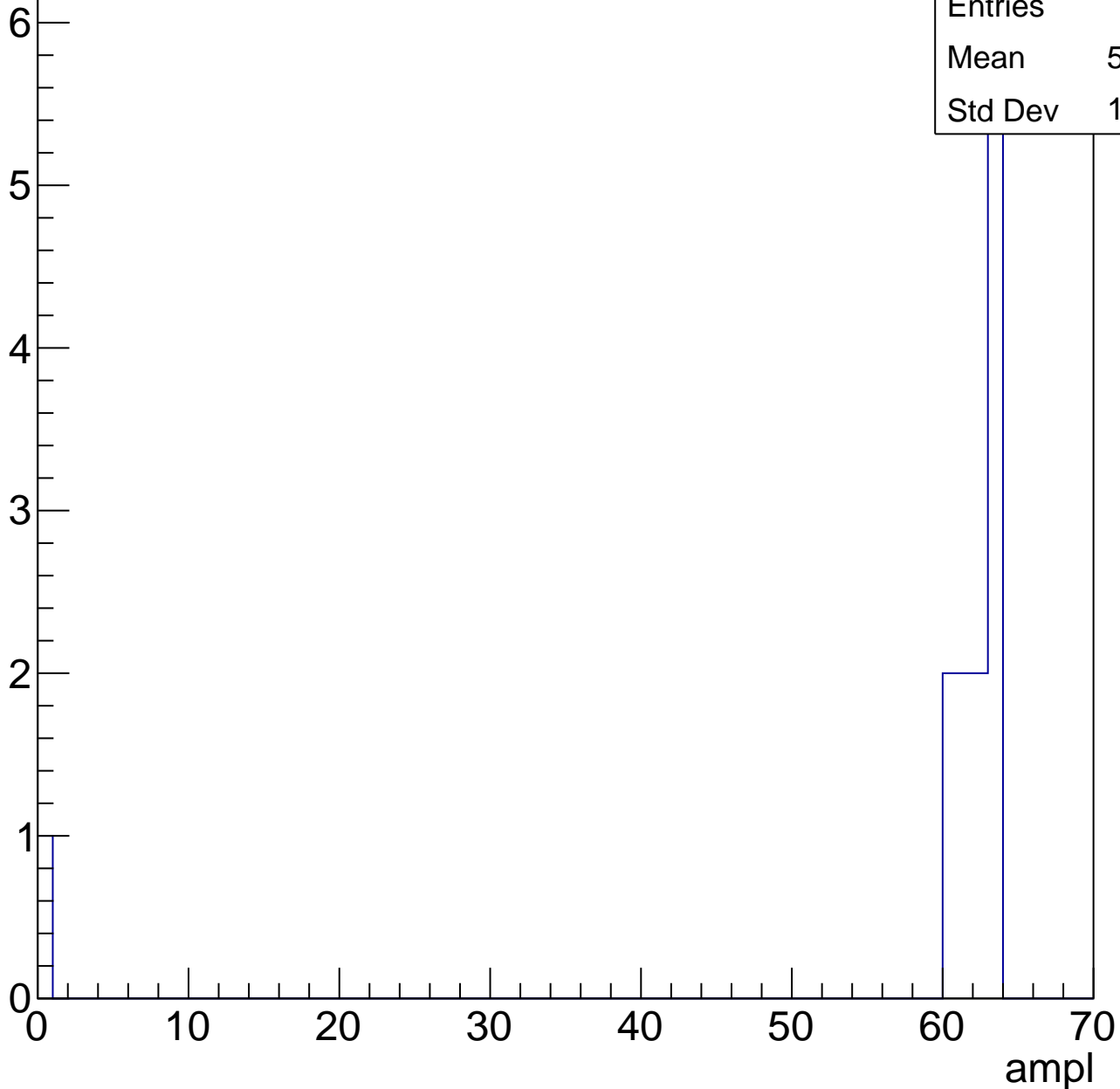


# B1L102S, U21-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	13
Mean	57.23
Std Dev	16.56





# B1L102S, U21-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U21-ch94, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	71
Mean	29.31
Std Dev	5.205

**Gaus mean : 30.0621**

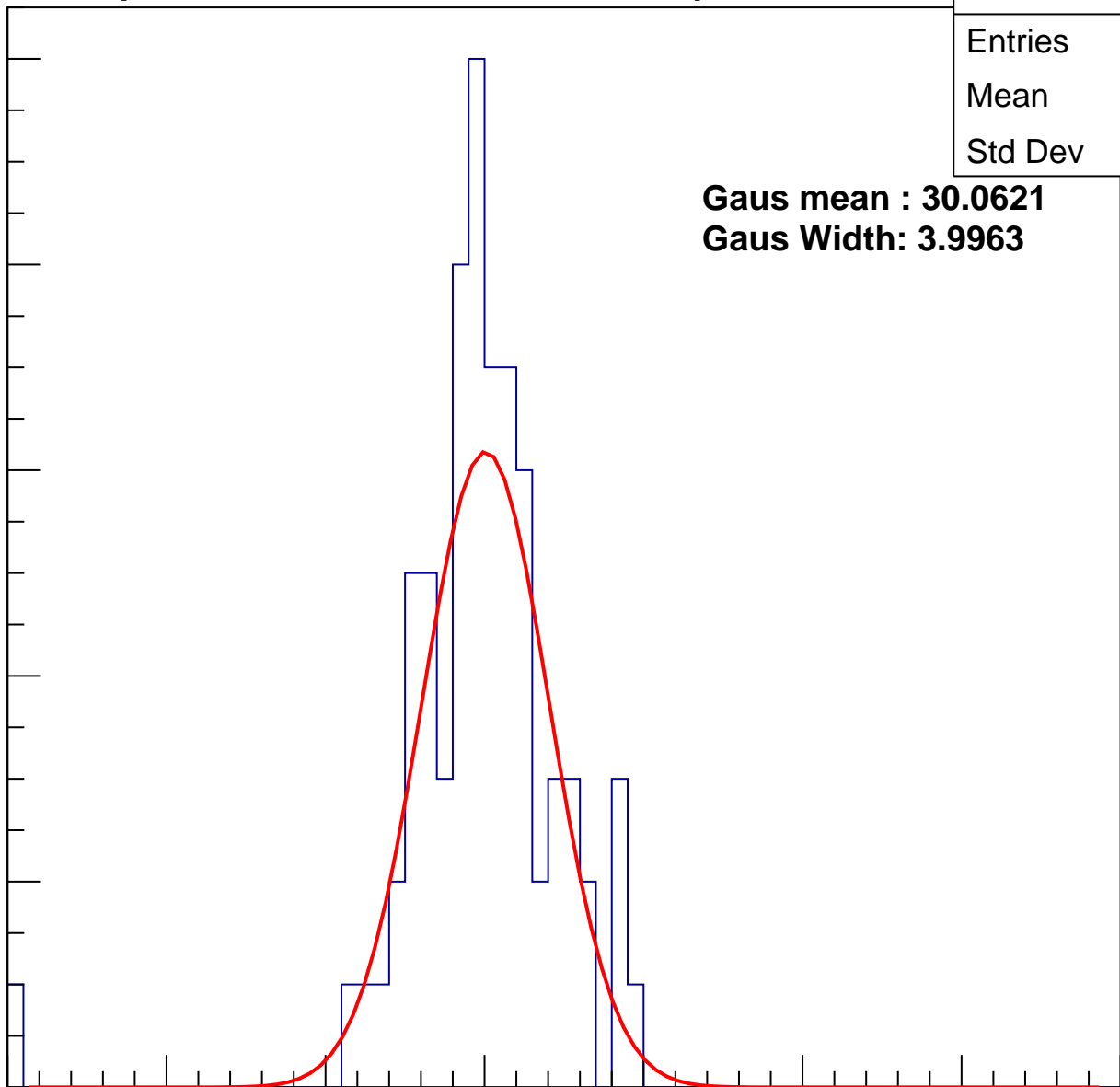
**Gaus Width: 3.9963**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U21-ch94, adc1

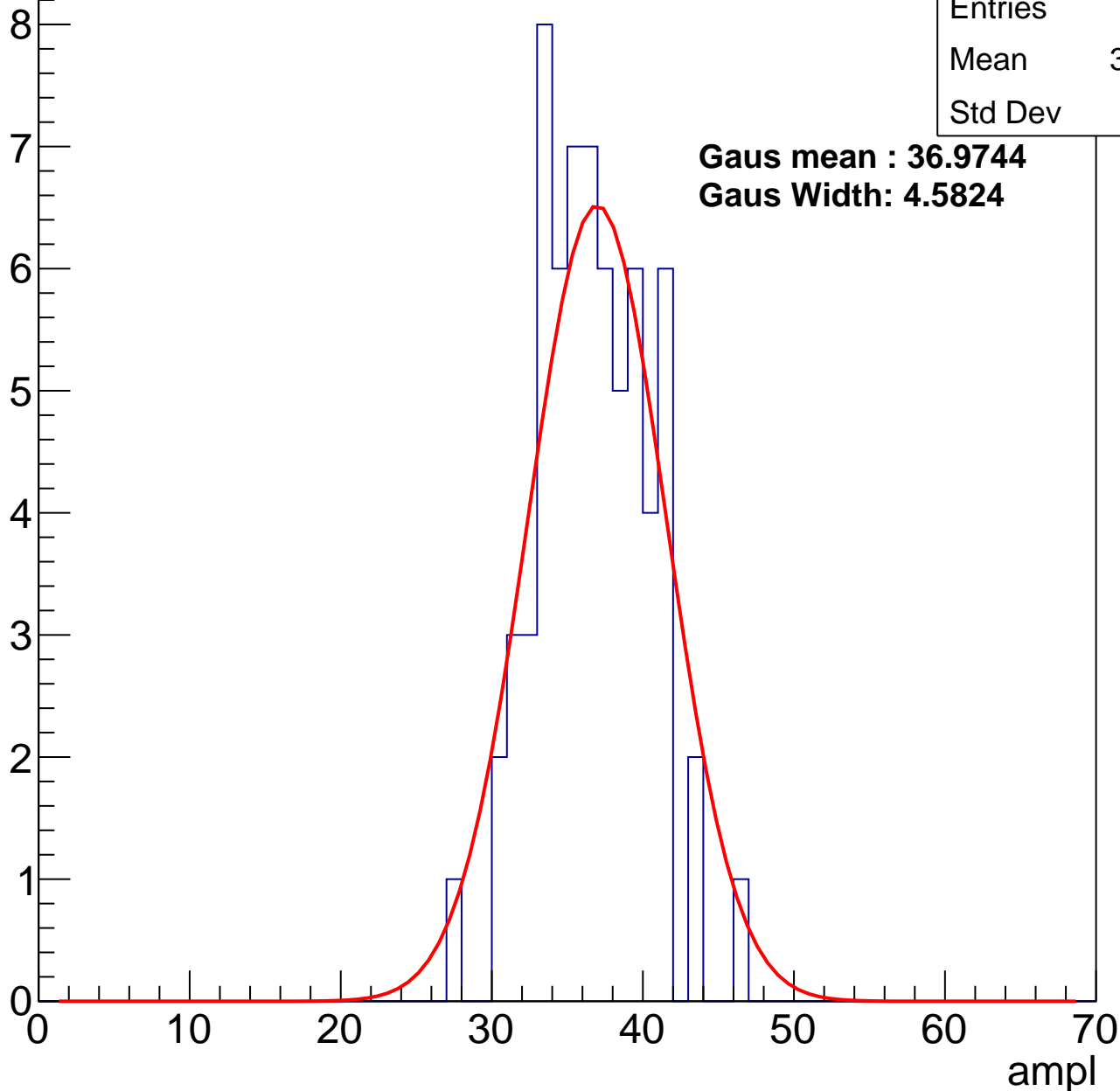
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	36.19
Std Dev	3.6

**Gaus mean : 36.9744**

**Gaus Width: 4.5824**



# B1L102S, U21-ch94, adc2

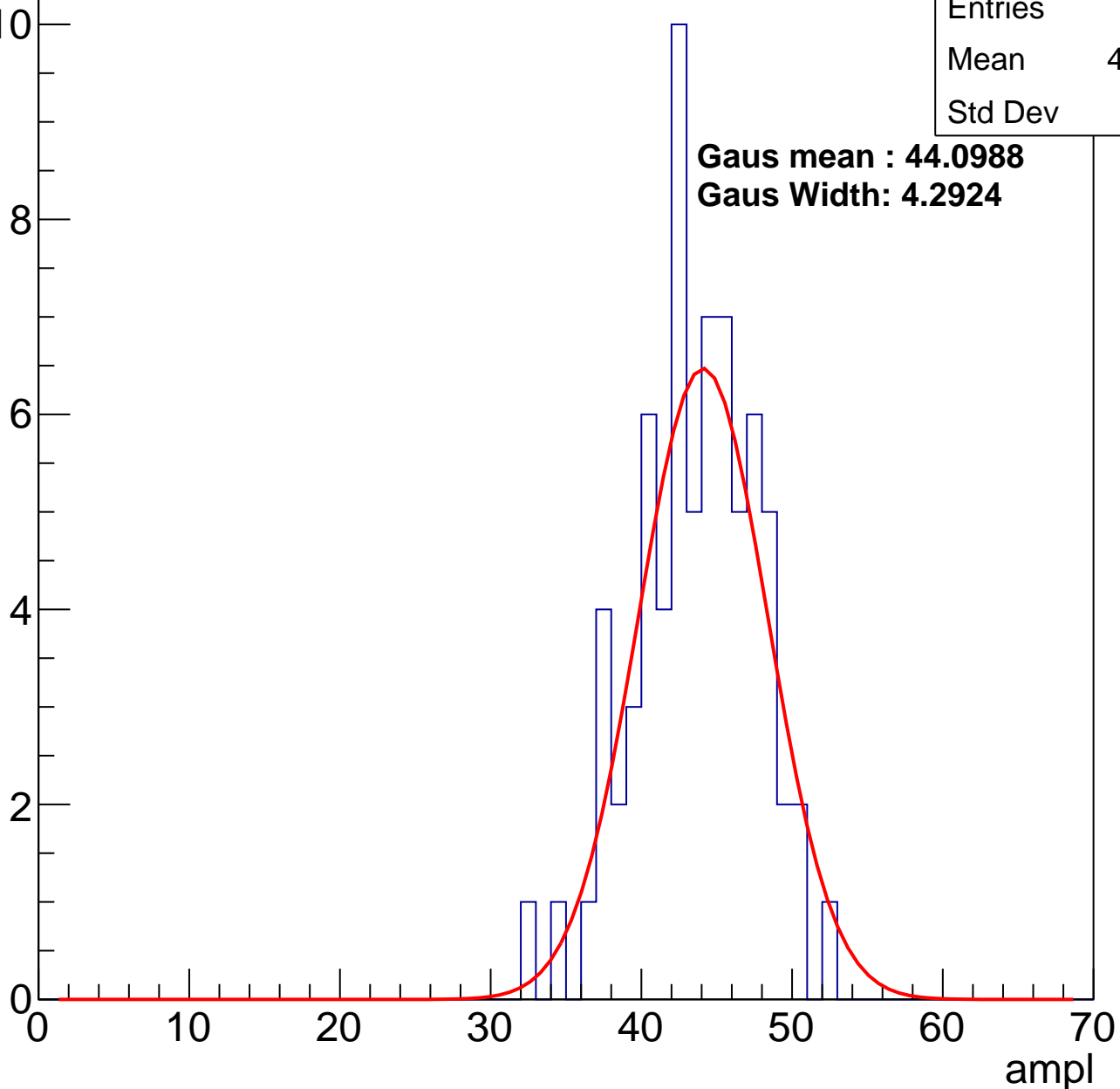
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	43.15
Std Dev	3.95

**Gaus mean : 44.0988**

**Gaus Width: 4.2924**

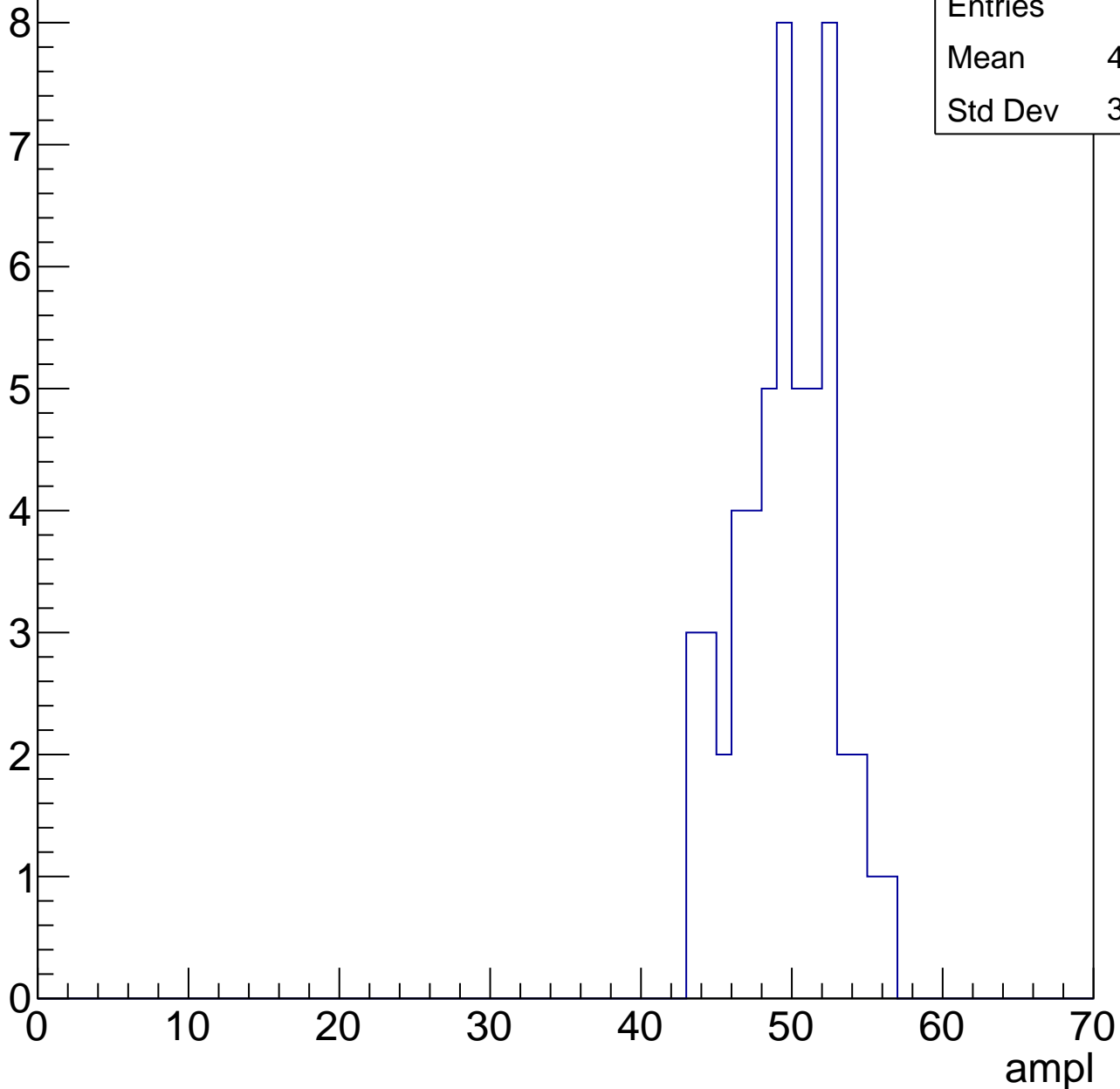


# B1L102S, U21-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

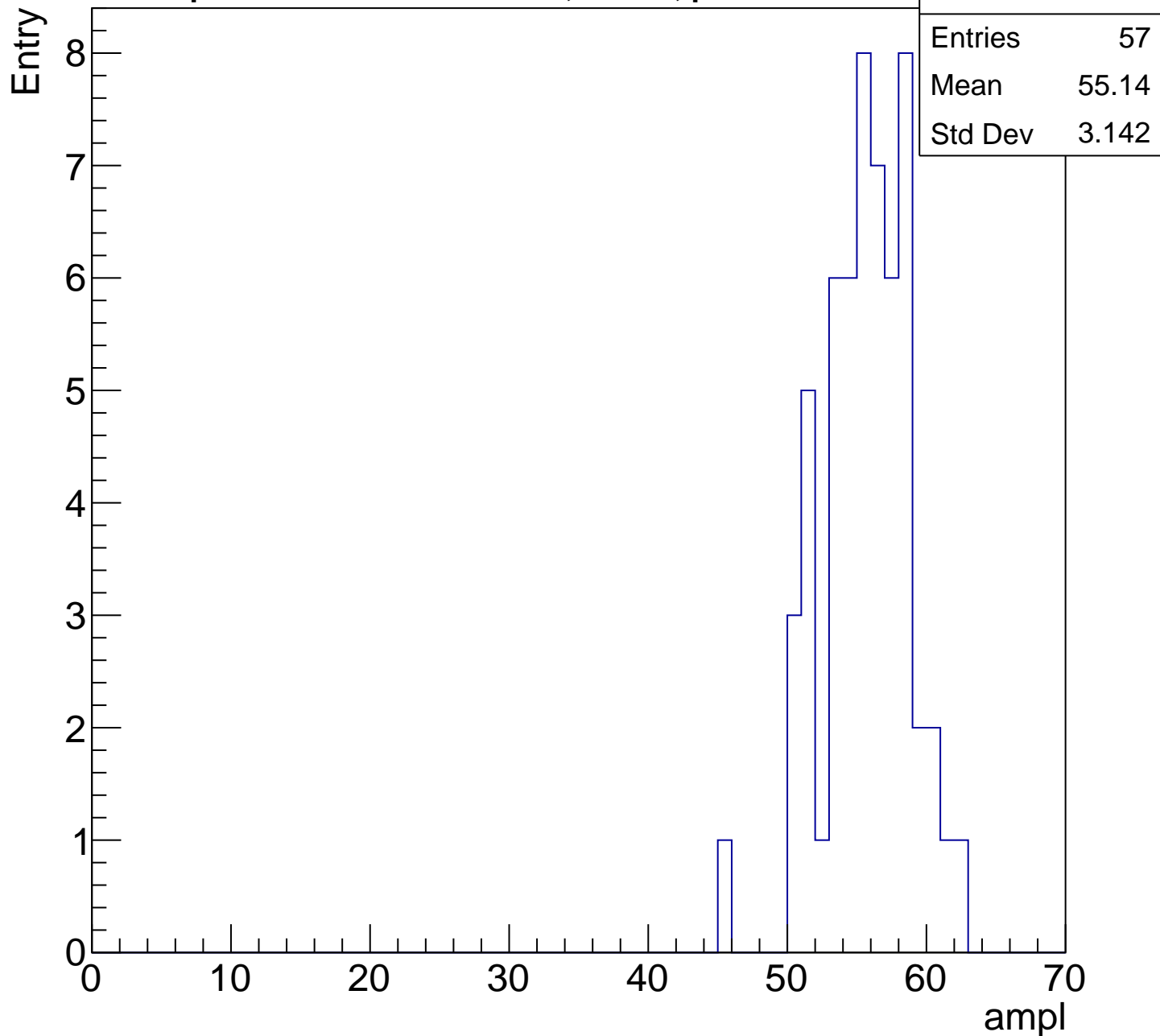
Entry

Entries	53
Mean	49.08
Std Dev	3.179



# B1L102S, U21-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

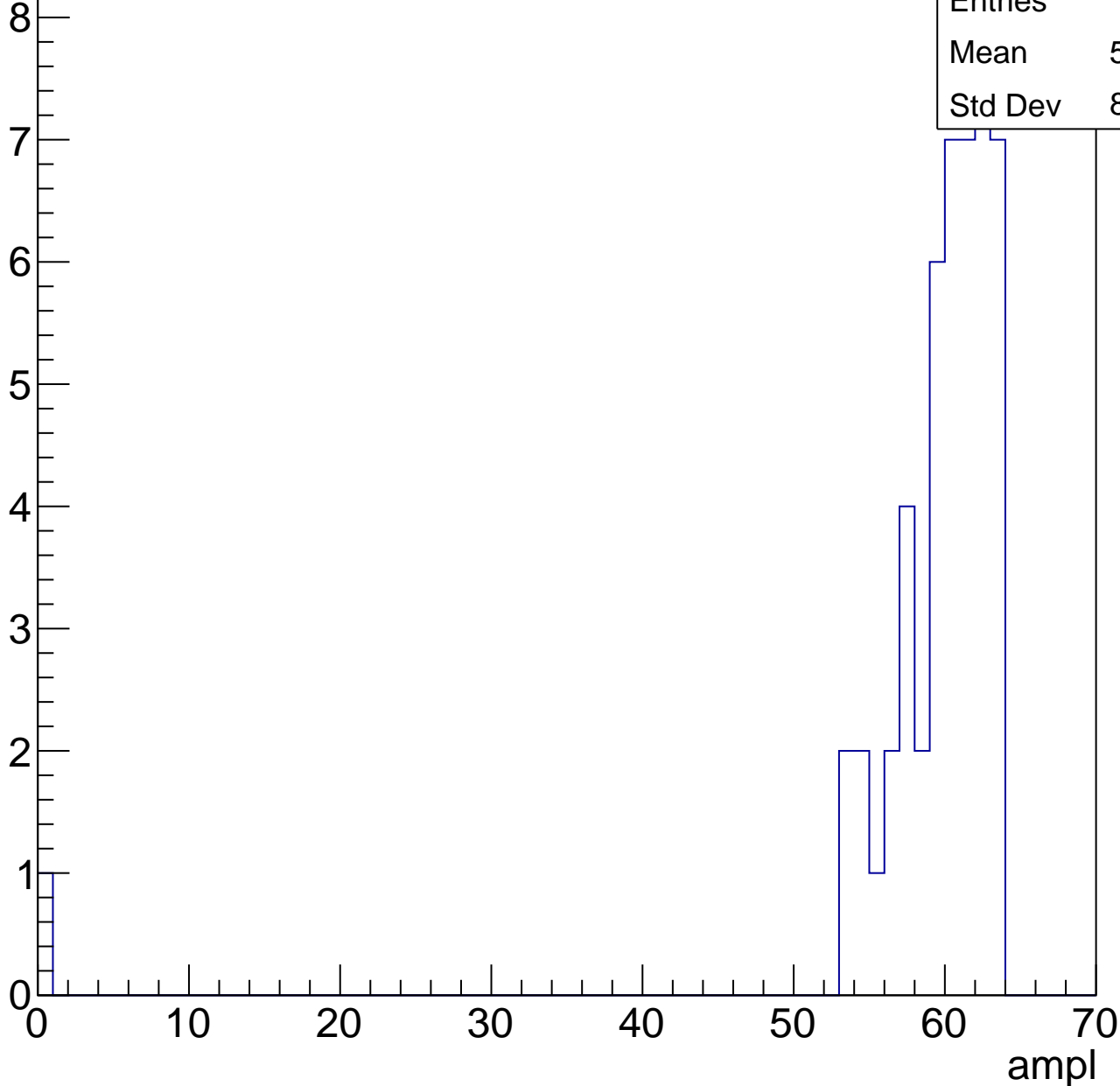


# B1L102S, U21-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

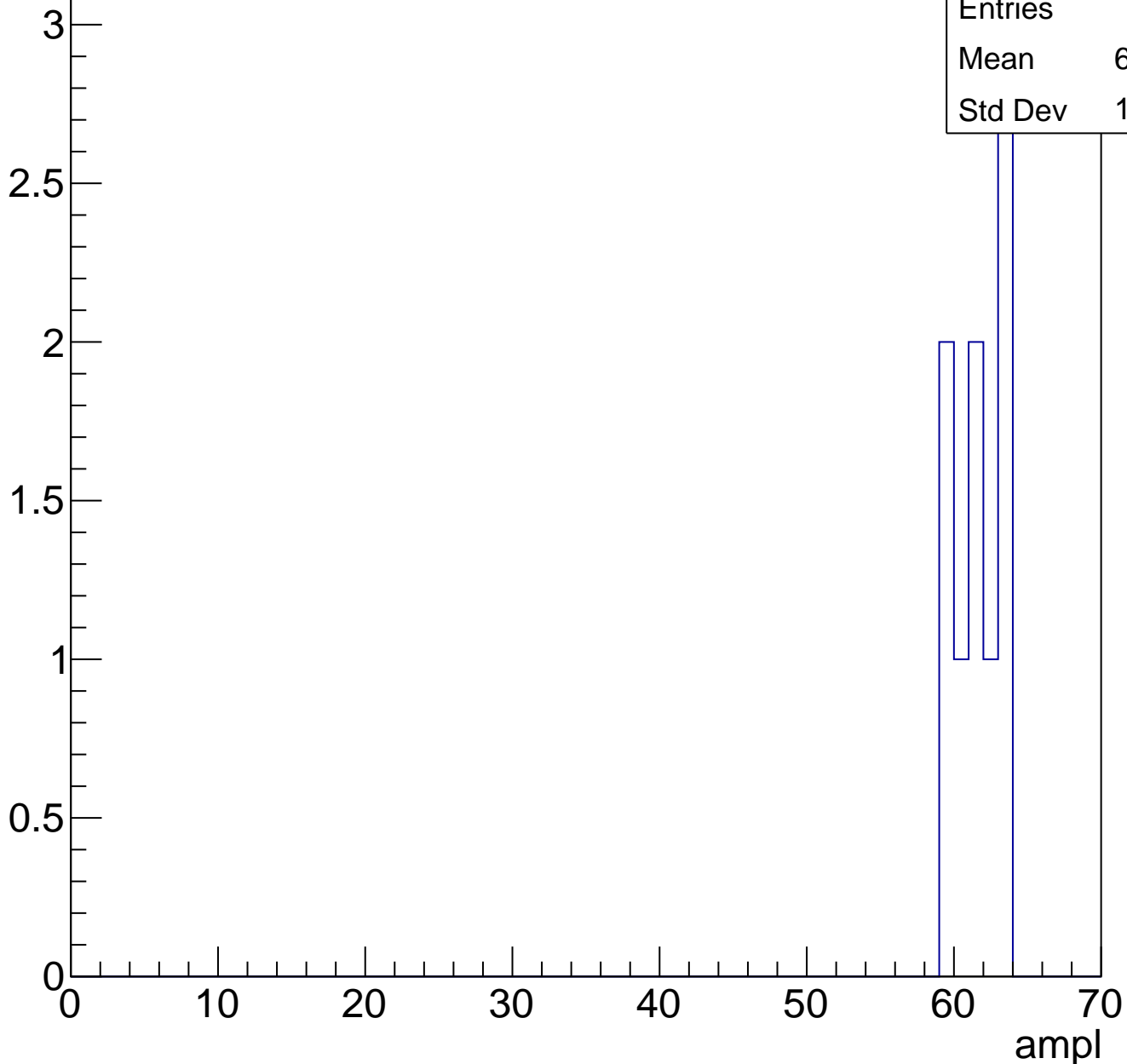
Entries	49
Mean	58.43
Std Dev	8.873



# B1L102S, U21-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	9
Mean	61.22
Std Dev	1.548



# B1L102S, U21-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U21-ch95, adc0

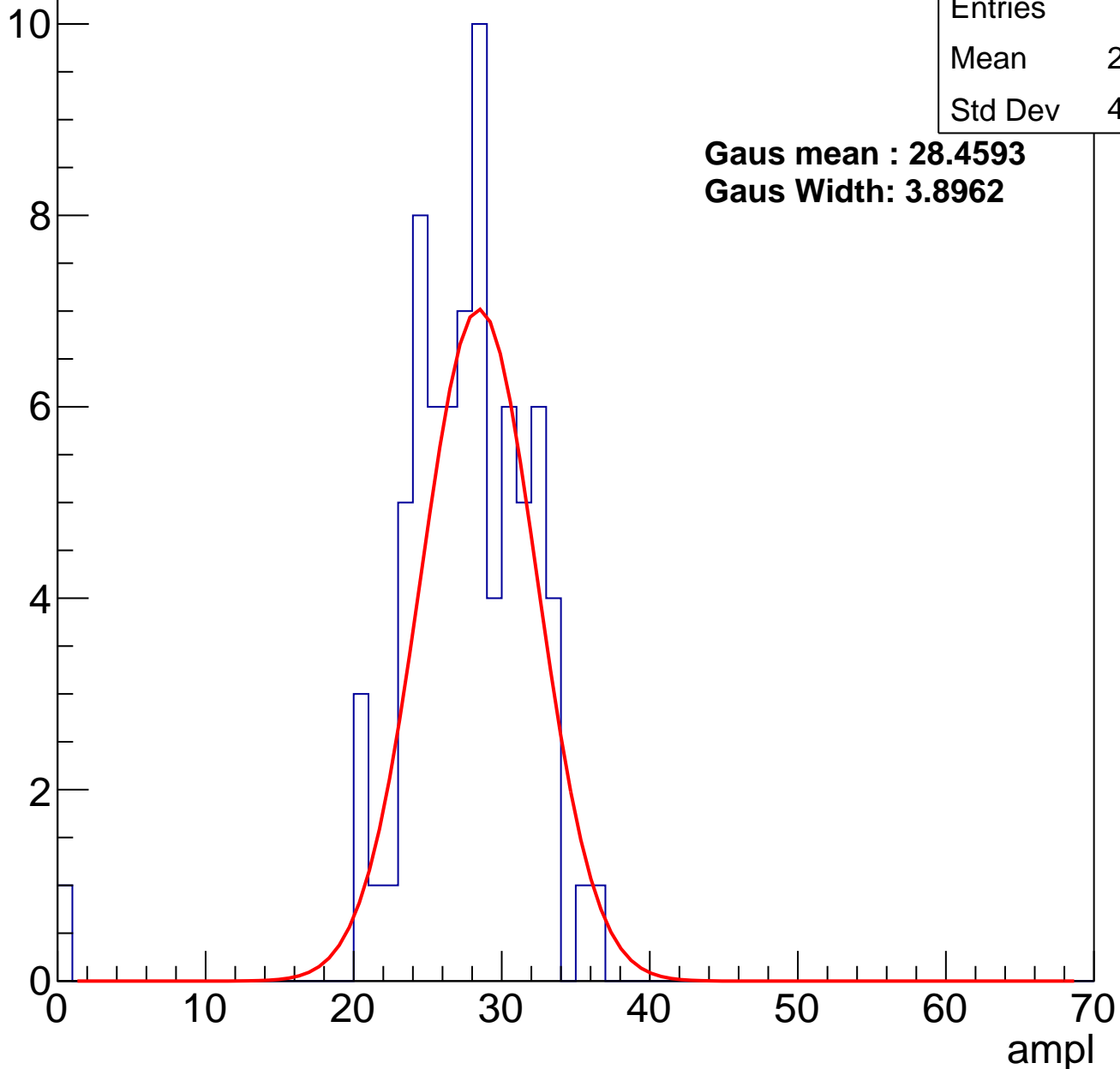
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	75
Mean	27.08
Std Dev	4.785

**Gaus mean : 28.4593**

**Gaus Width: 3.8962**

Entry



# B1L102S, U21-ch95, adc1

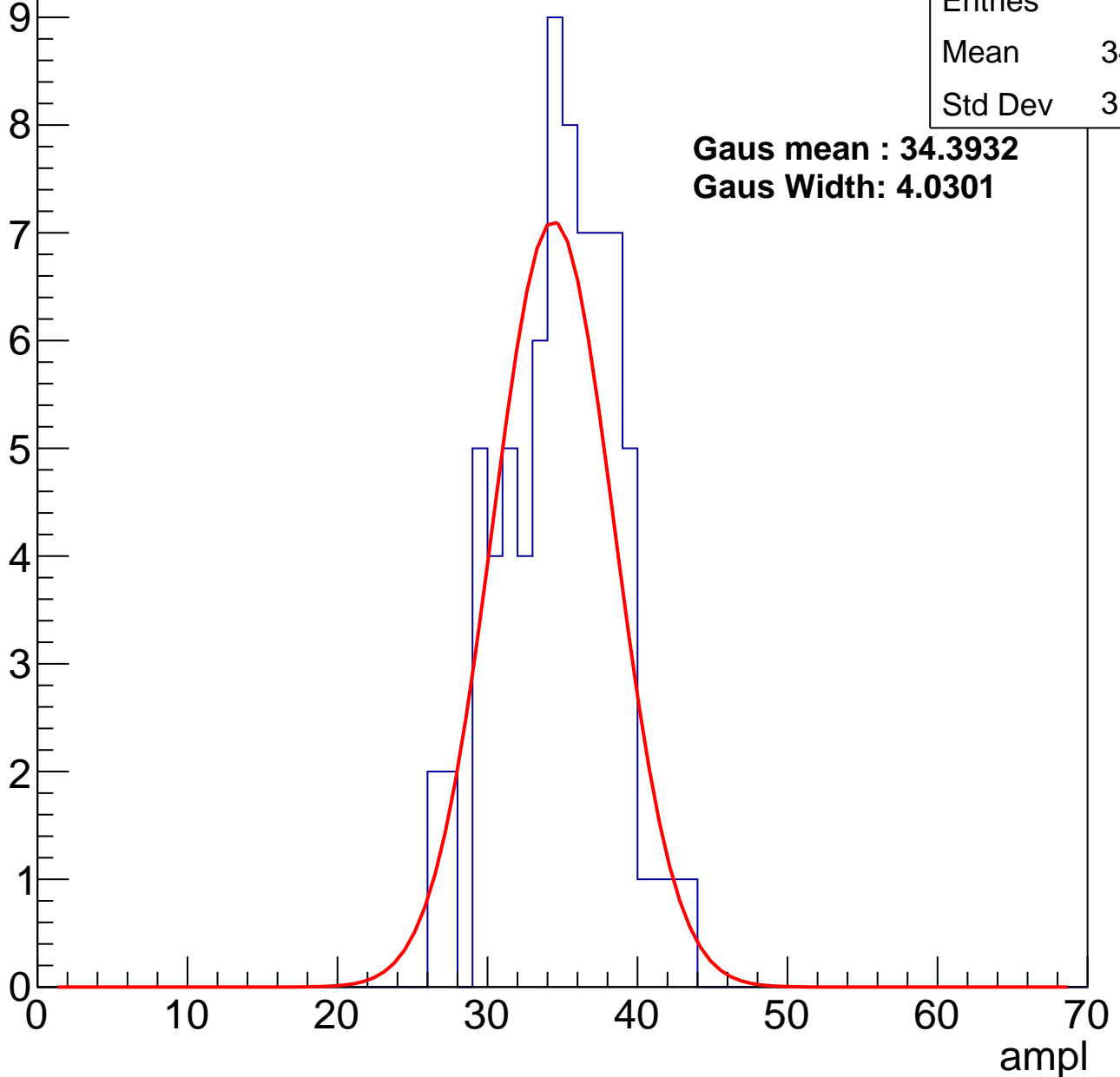
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	34.35
Std Dev	3.722

**Gaus mean : 34.3932**

**Gaus Width: 4.0301**



# B1L102S, U21-ch95, adc2

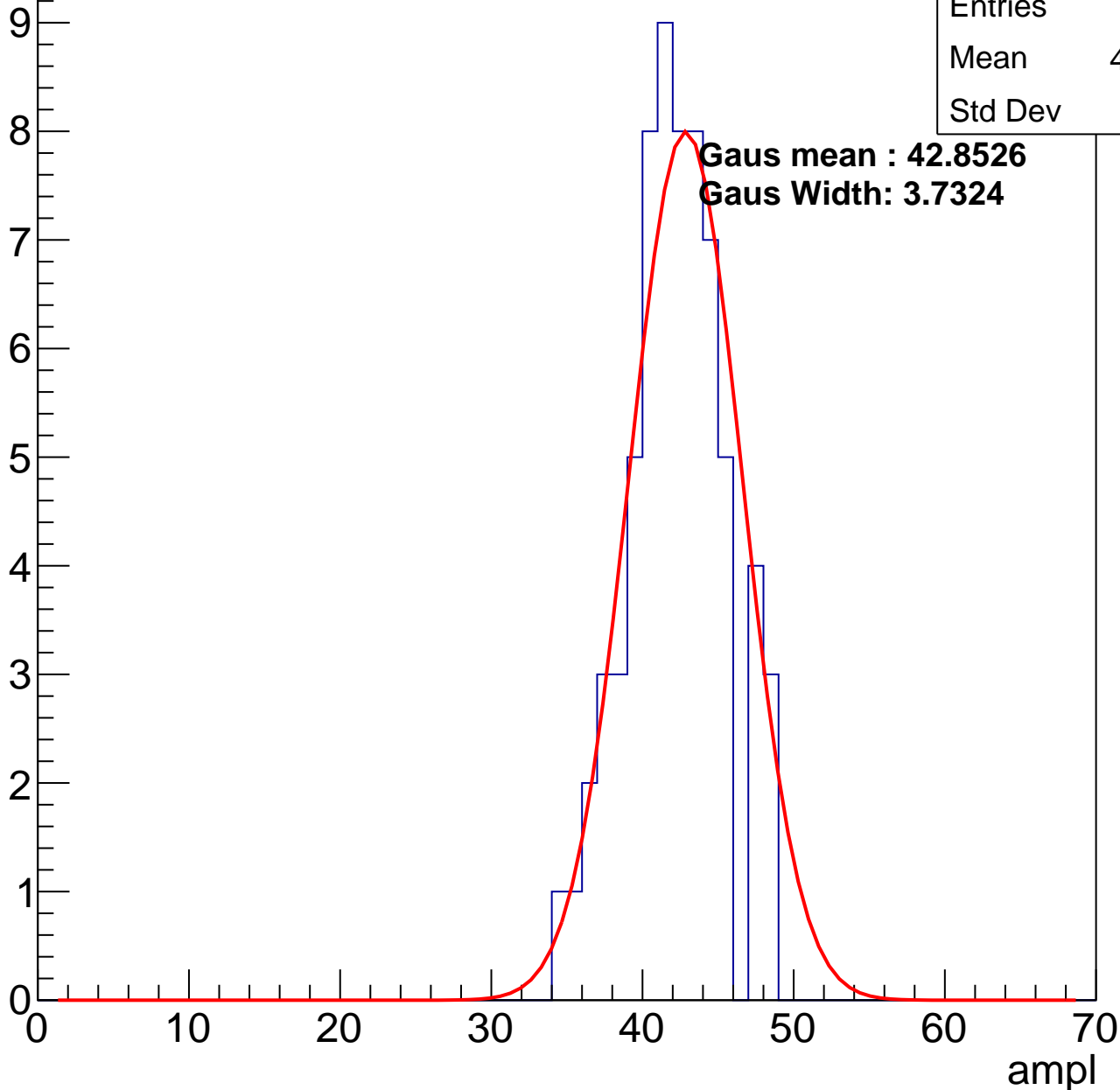
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	41.72
Std Dev	3.18

**Gaus mean : 42.8526**

**Gaus Width: 3.7324**



# B1L102S, U21-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

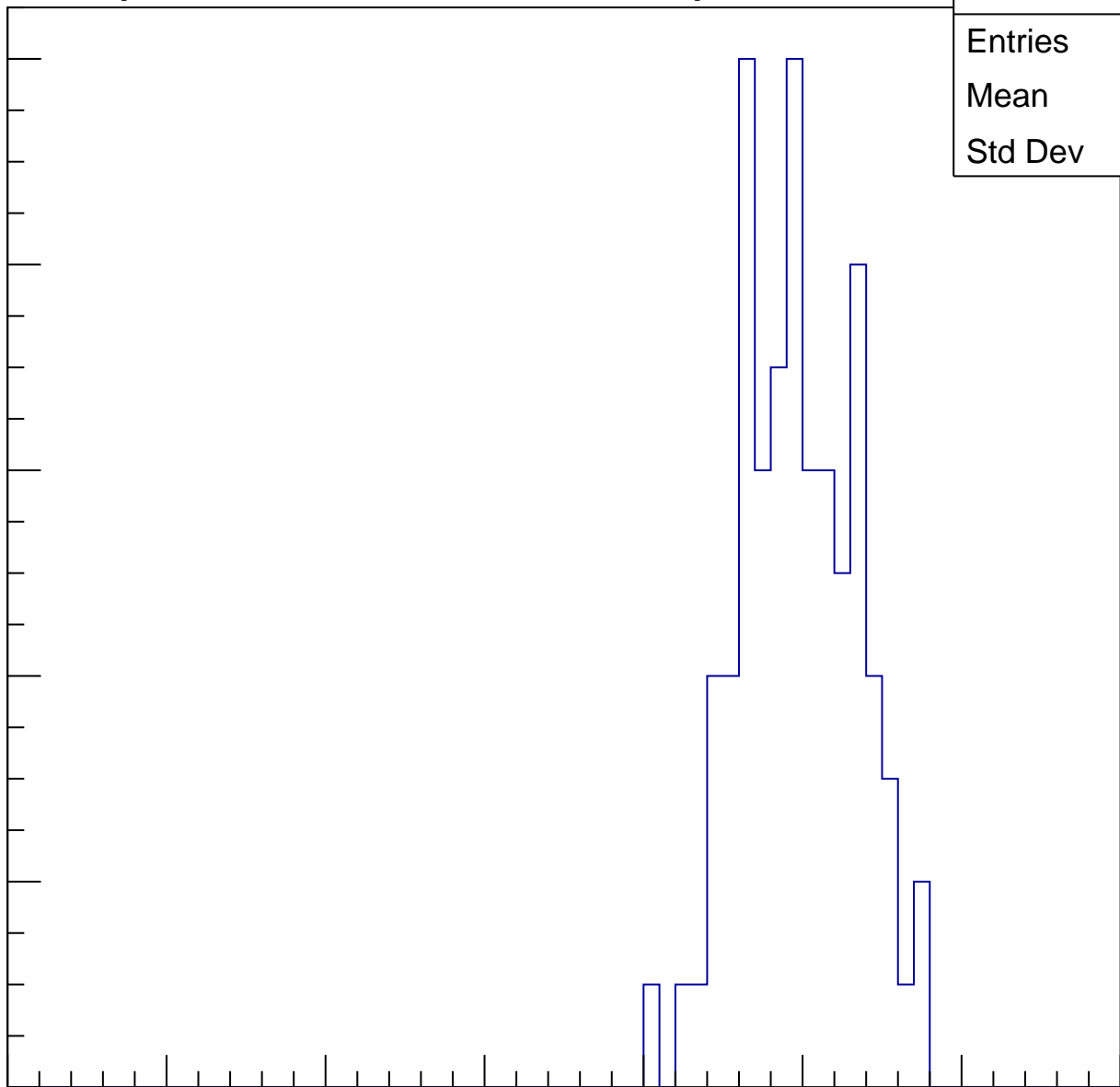
Entries	79
Mean	49.24
Std Dev	3.619

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

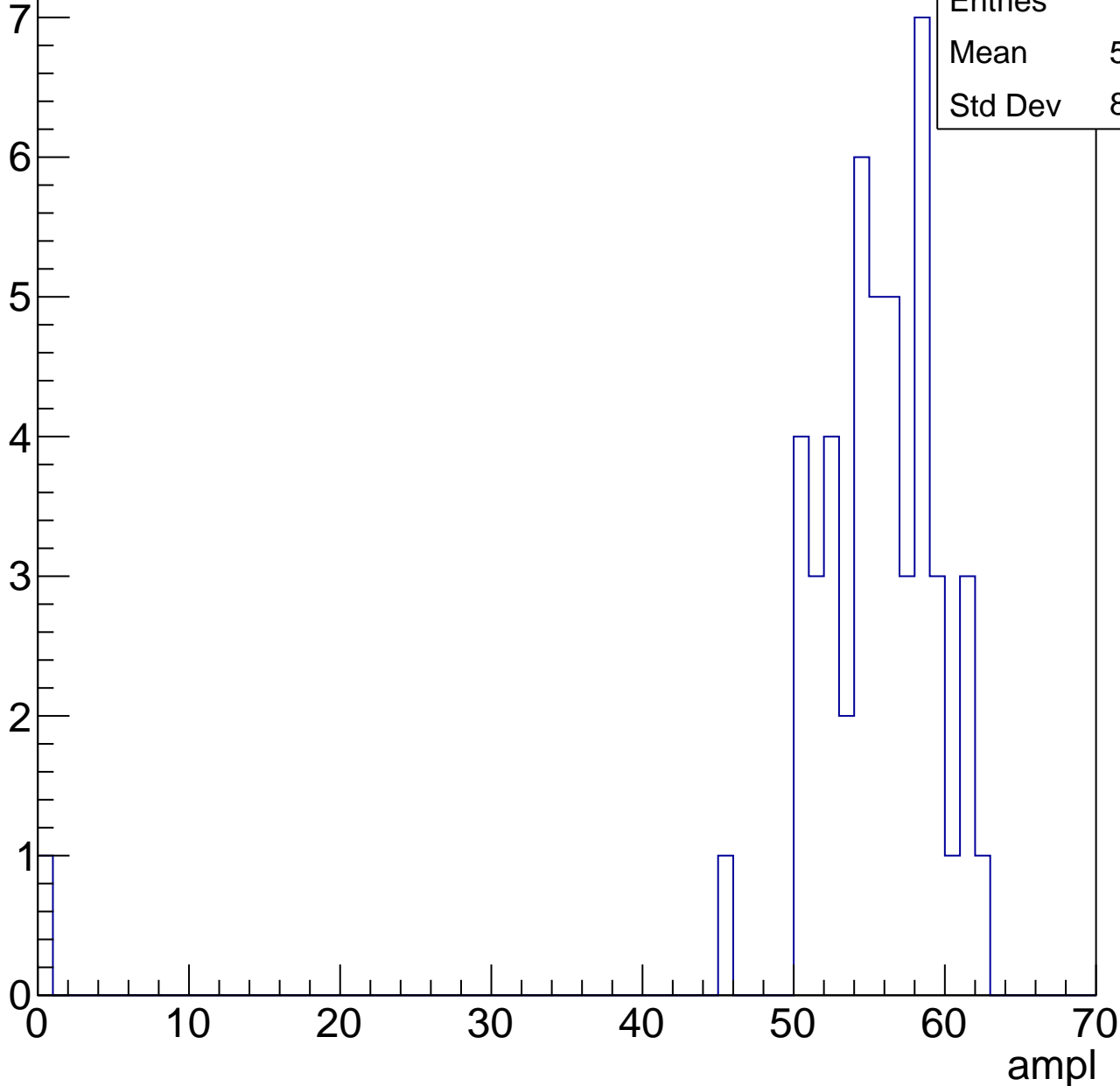


# B1L102S, U21-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	54.08
Std Dev	8.562



# B1L102S, U21-ch95, adc5

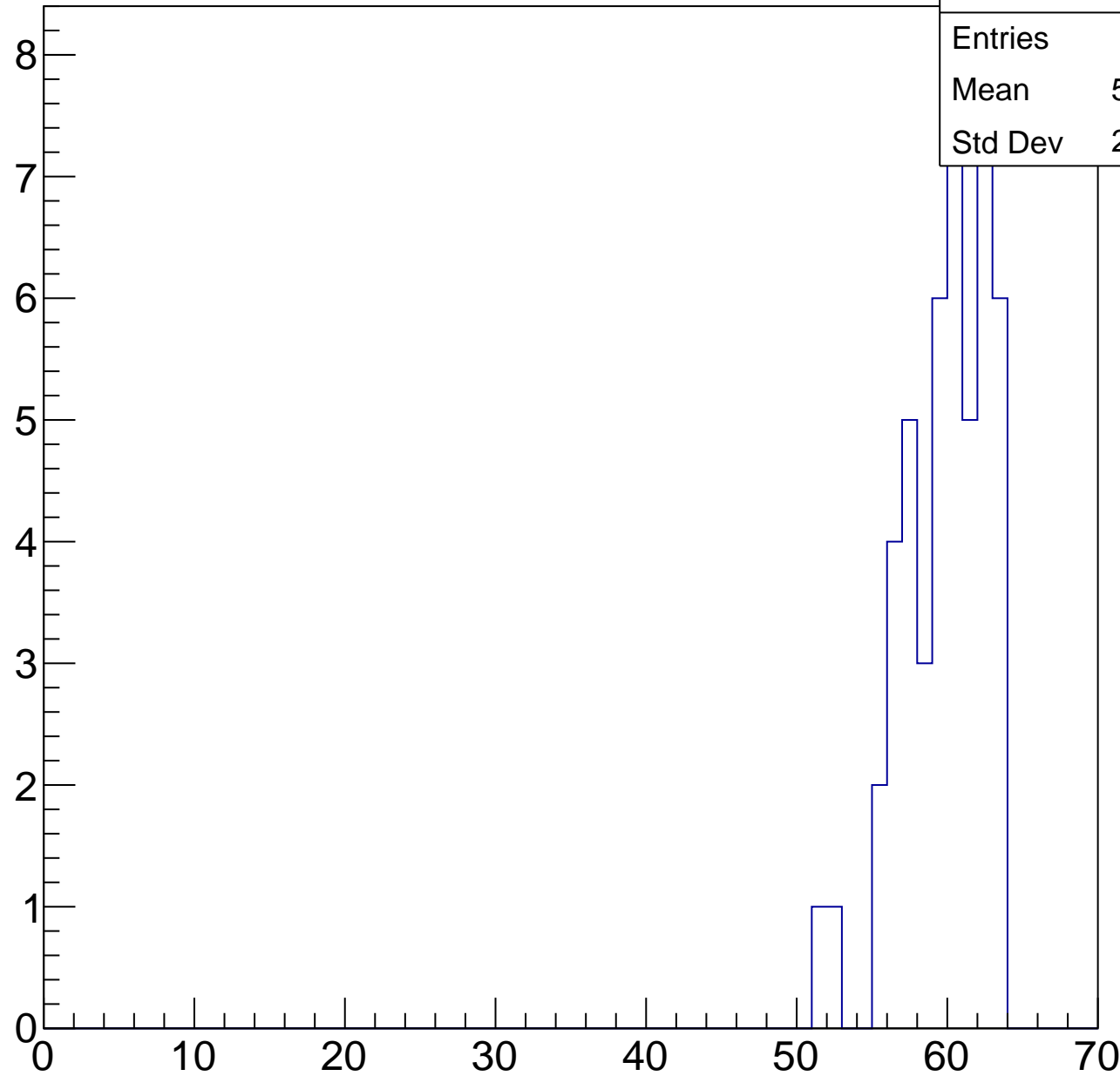
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	59.37
Std Dev	2.833

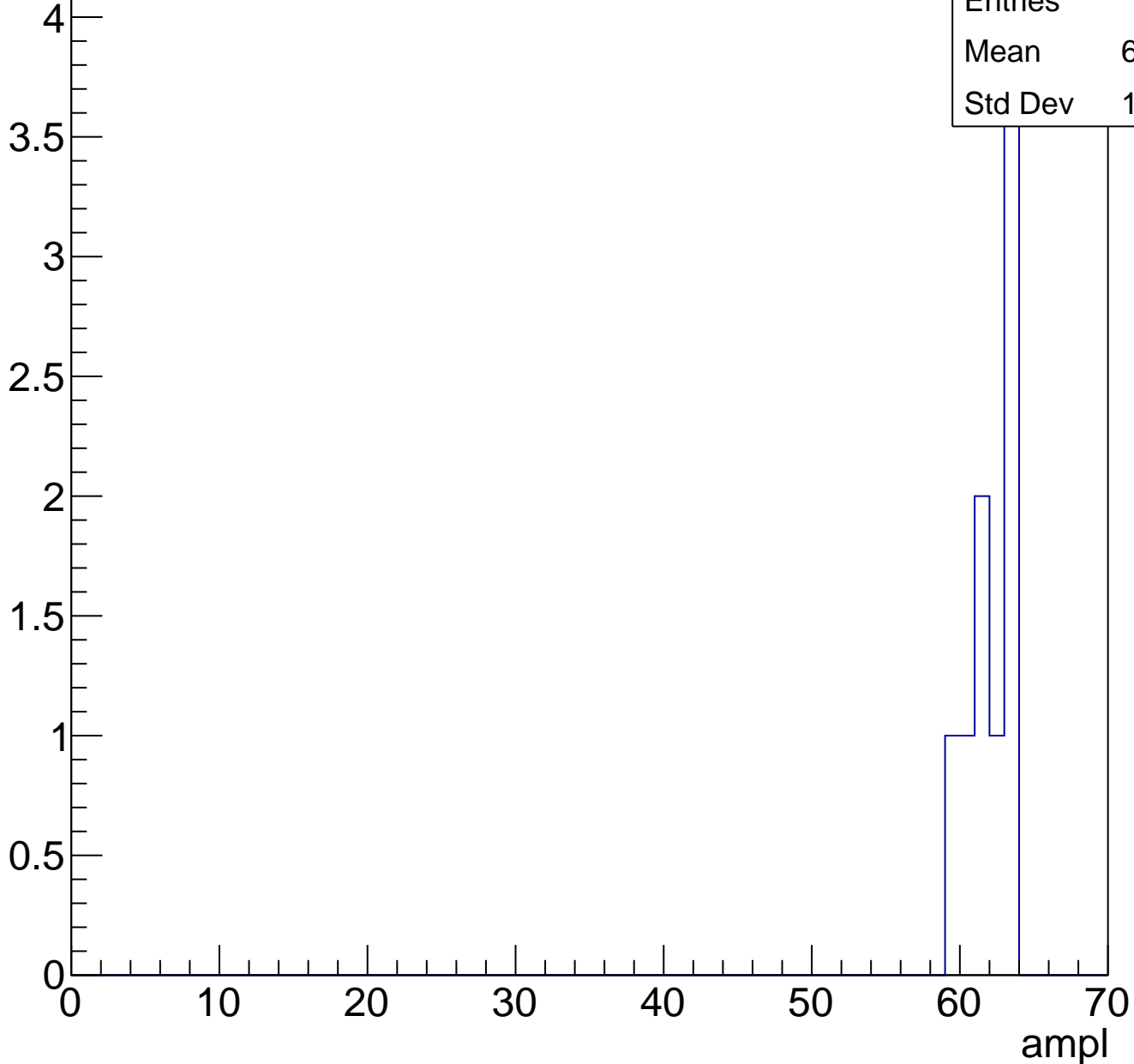
ampl



# B1L102S, U21-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U21-ch96, adc0

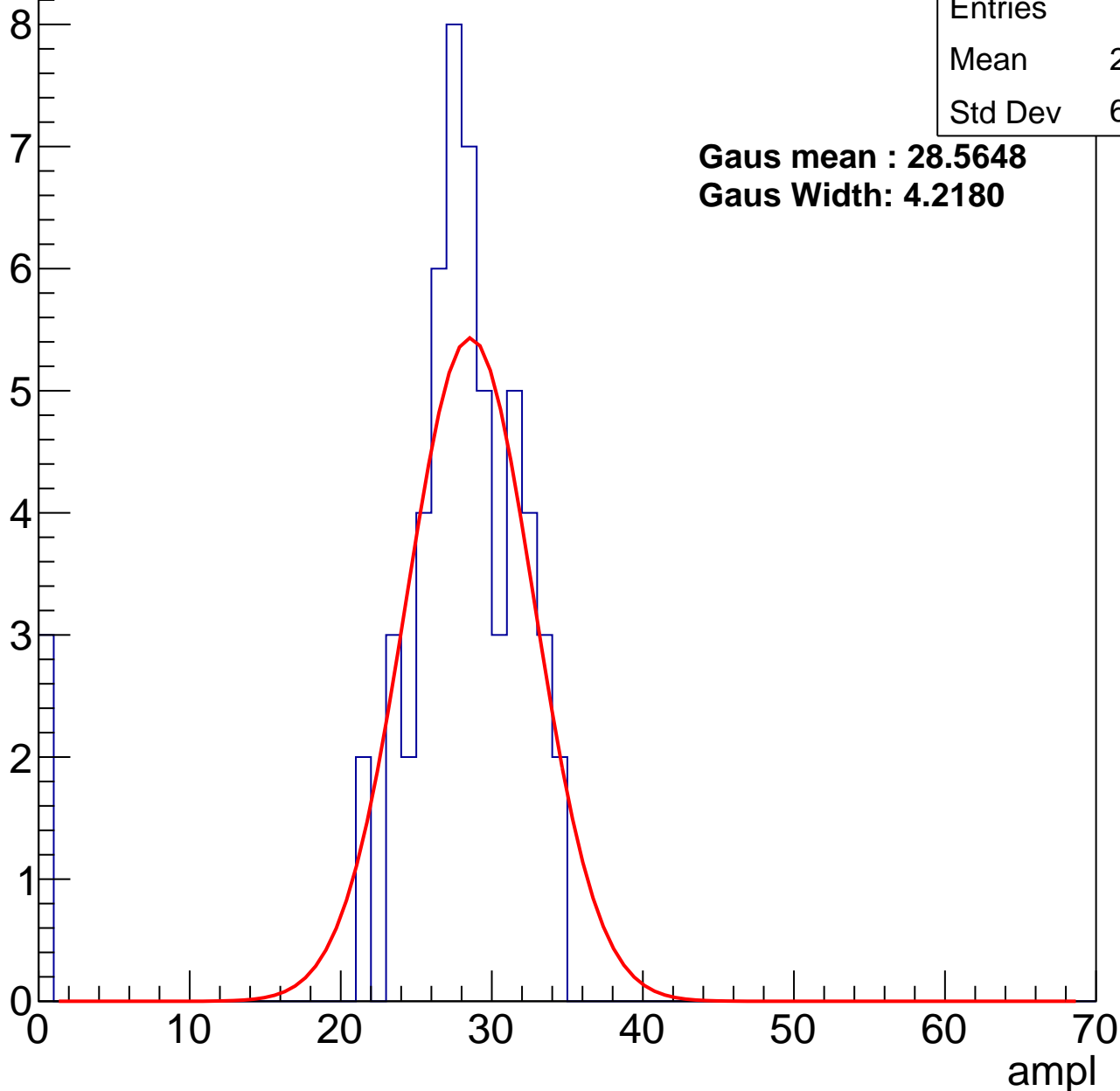
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	26.53
Std Dev	6.976

**Gaus mean : 28.5648**

**Gaus Width: 4.2180**



# B1L102S, U21-ch96, adc1

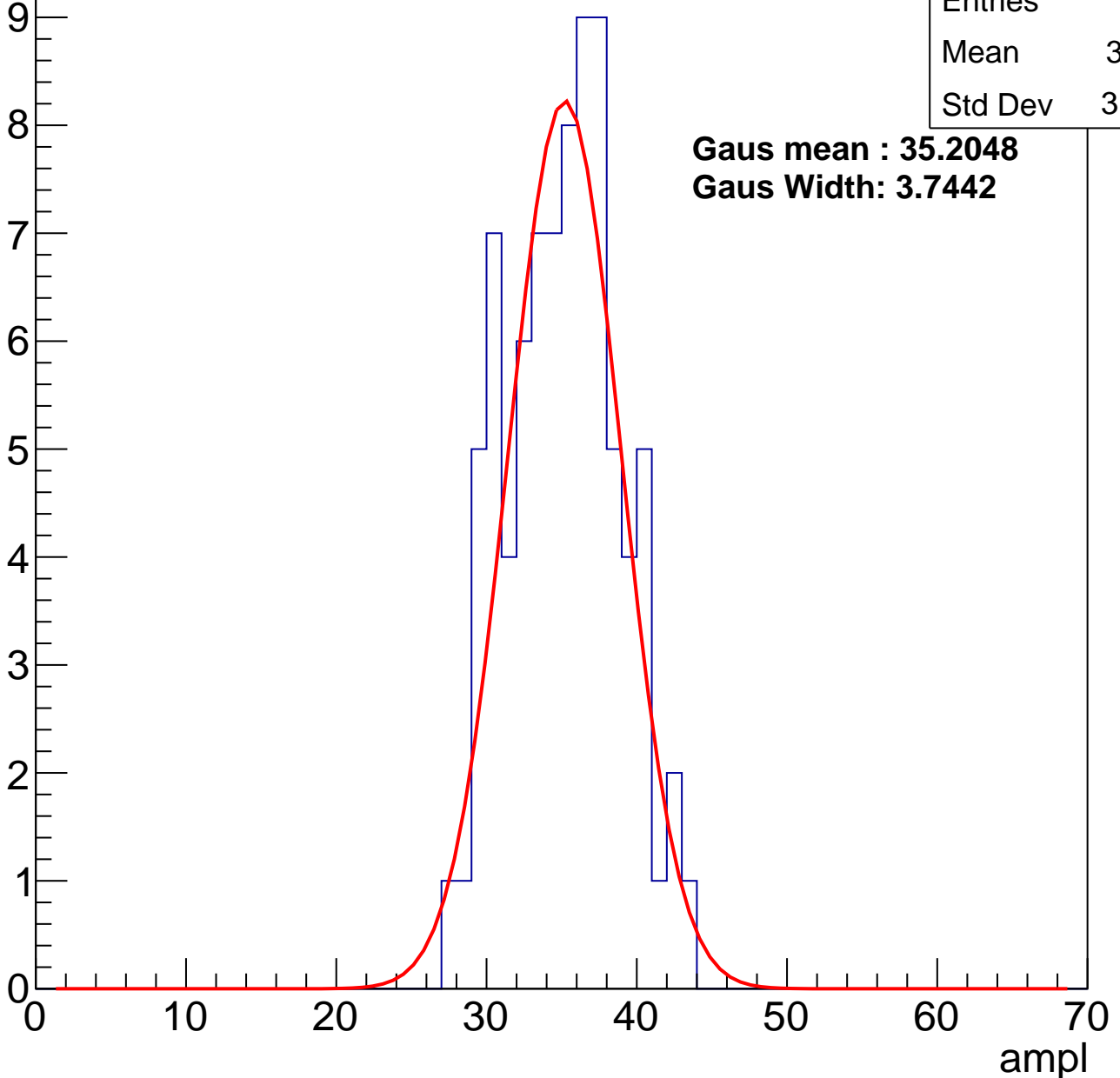
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	34.71
Std Dev	3.648

**Gaus mean : 35.2048**

**Gaus Width: 3.7442**



# B1L102S, U21-ch96, adc2

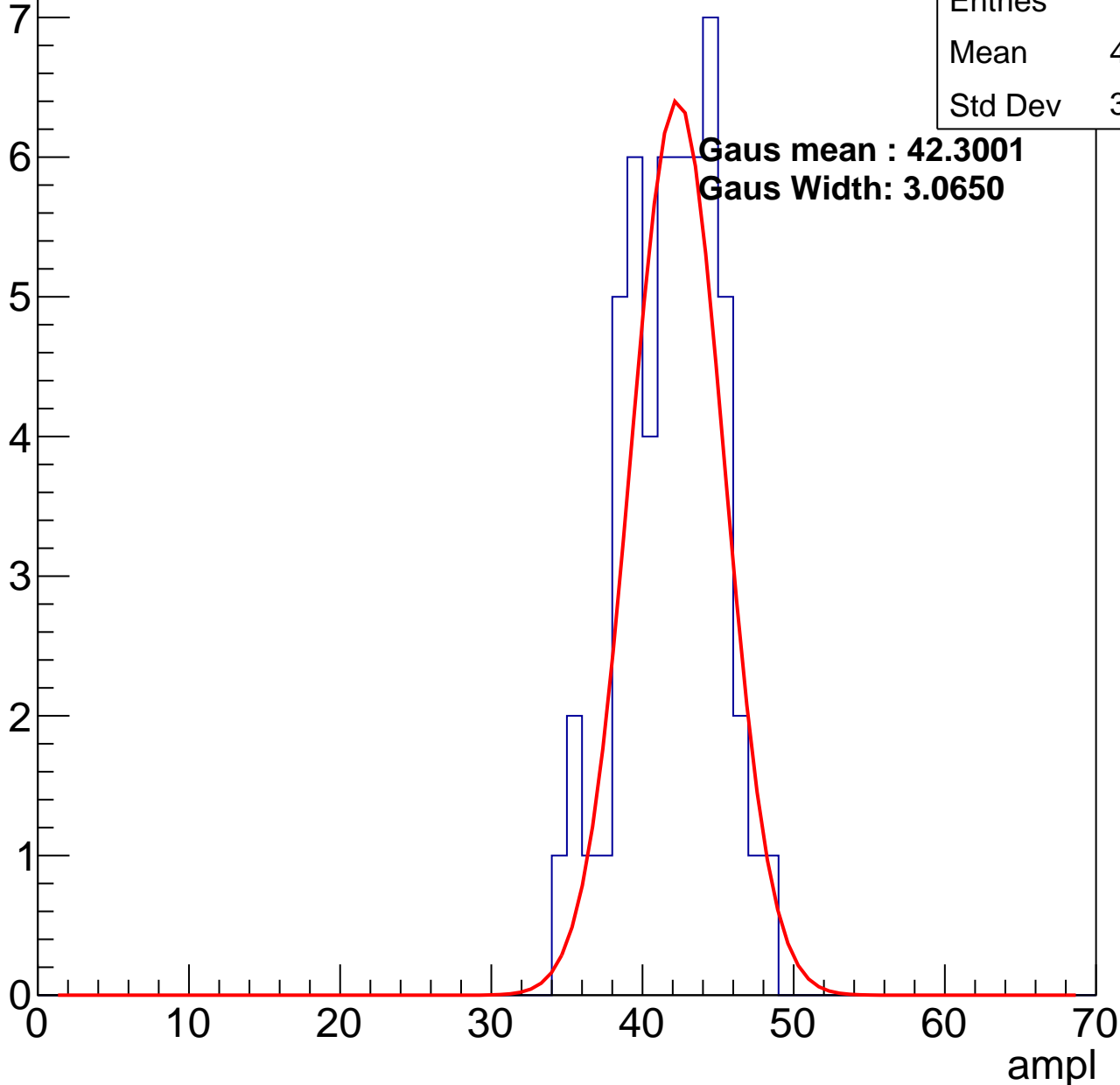
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	41.43
Std Dev	3.142

**Gaus mean : 42.3001**

**Gaus Width: 3.0650**

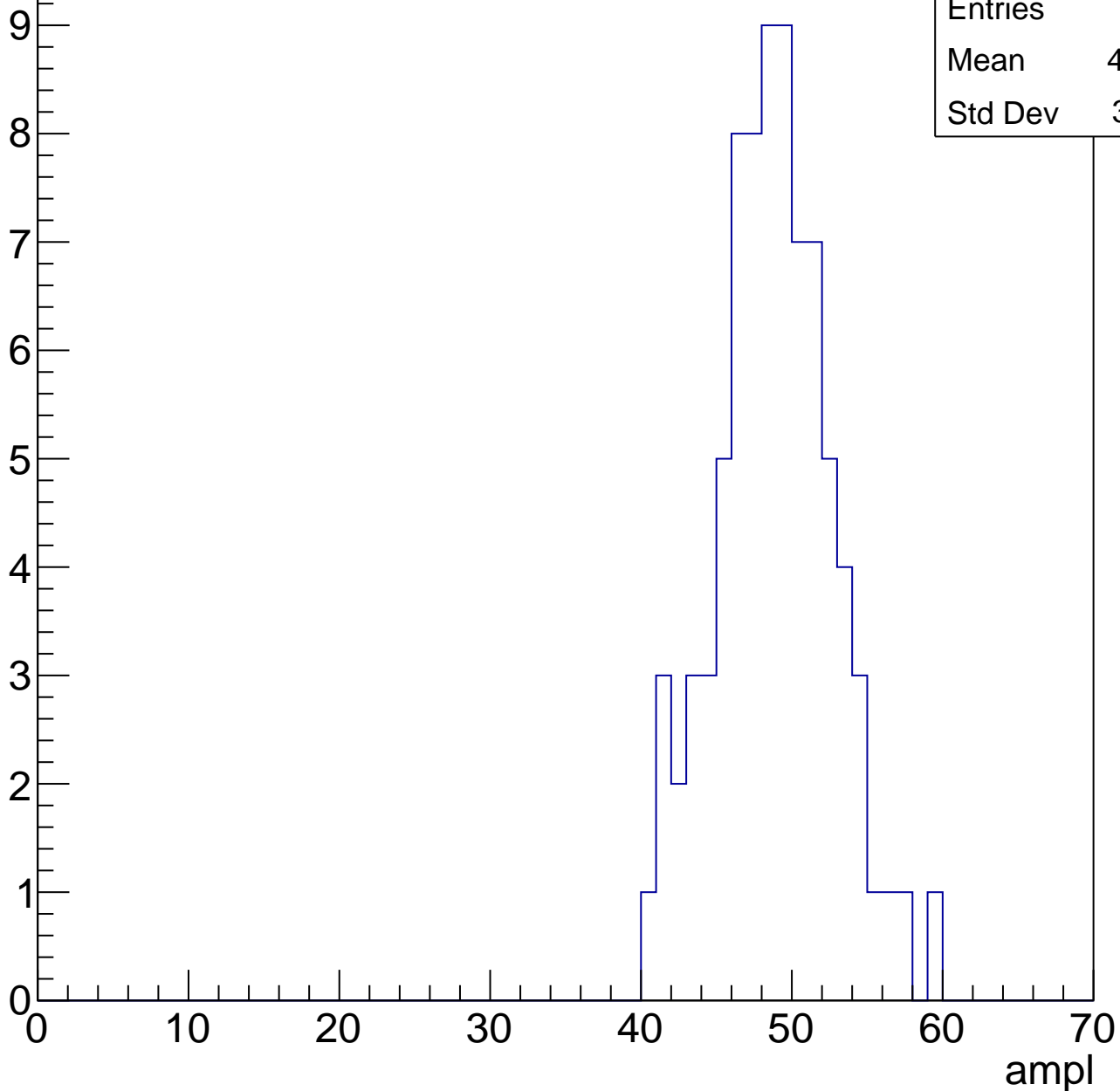


# B1L102S, U21-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	81
Mean	48.37
Std Dev	3.821

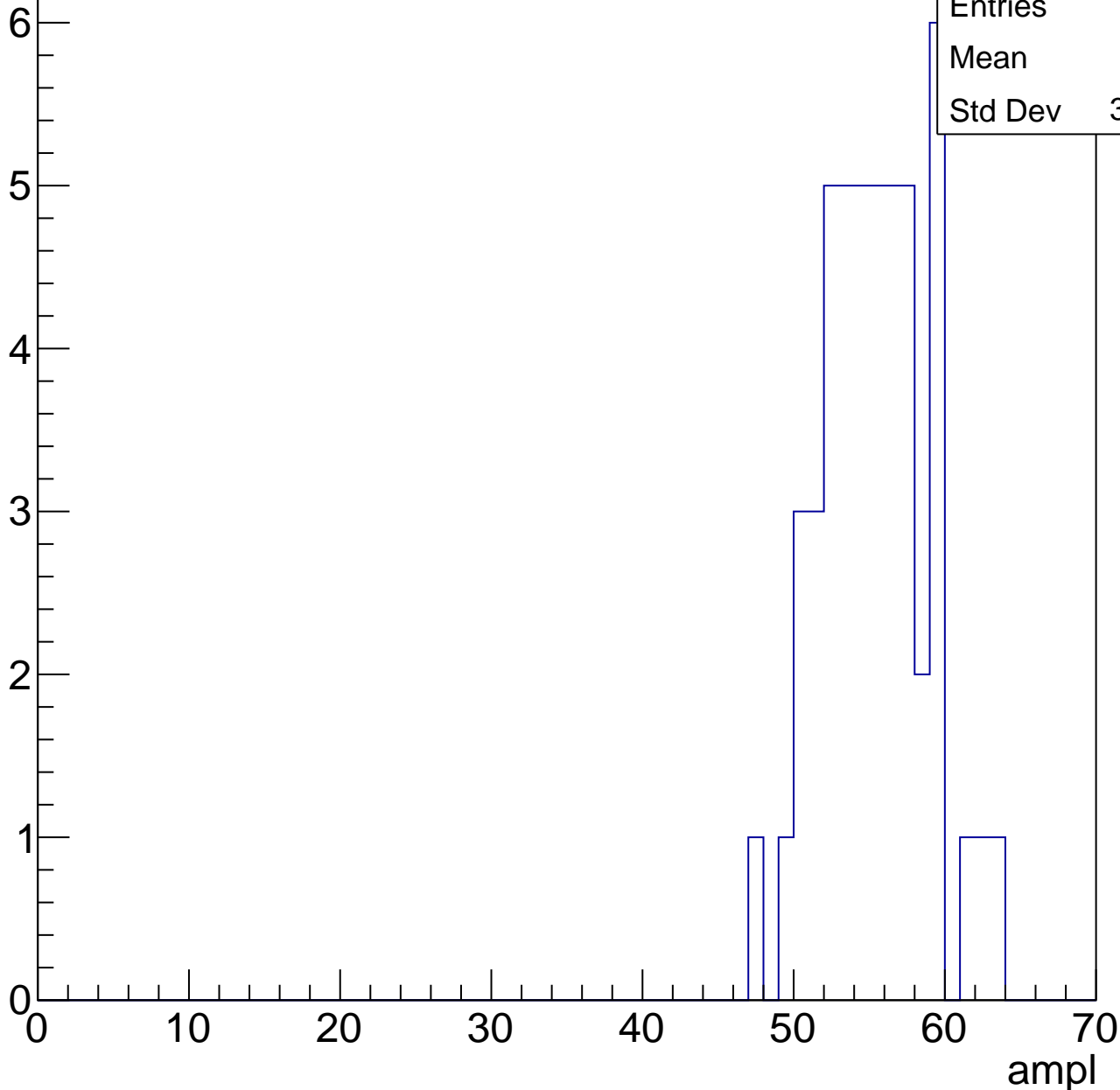


# B1L102S, U21-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

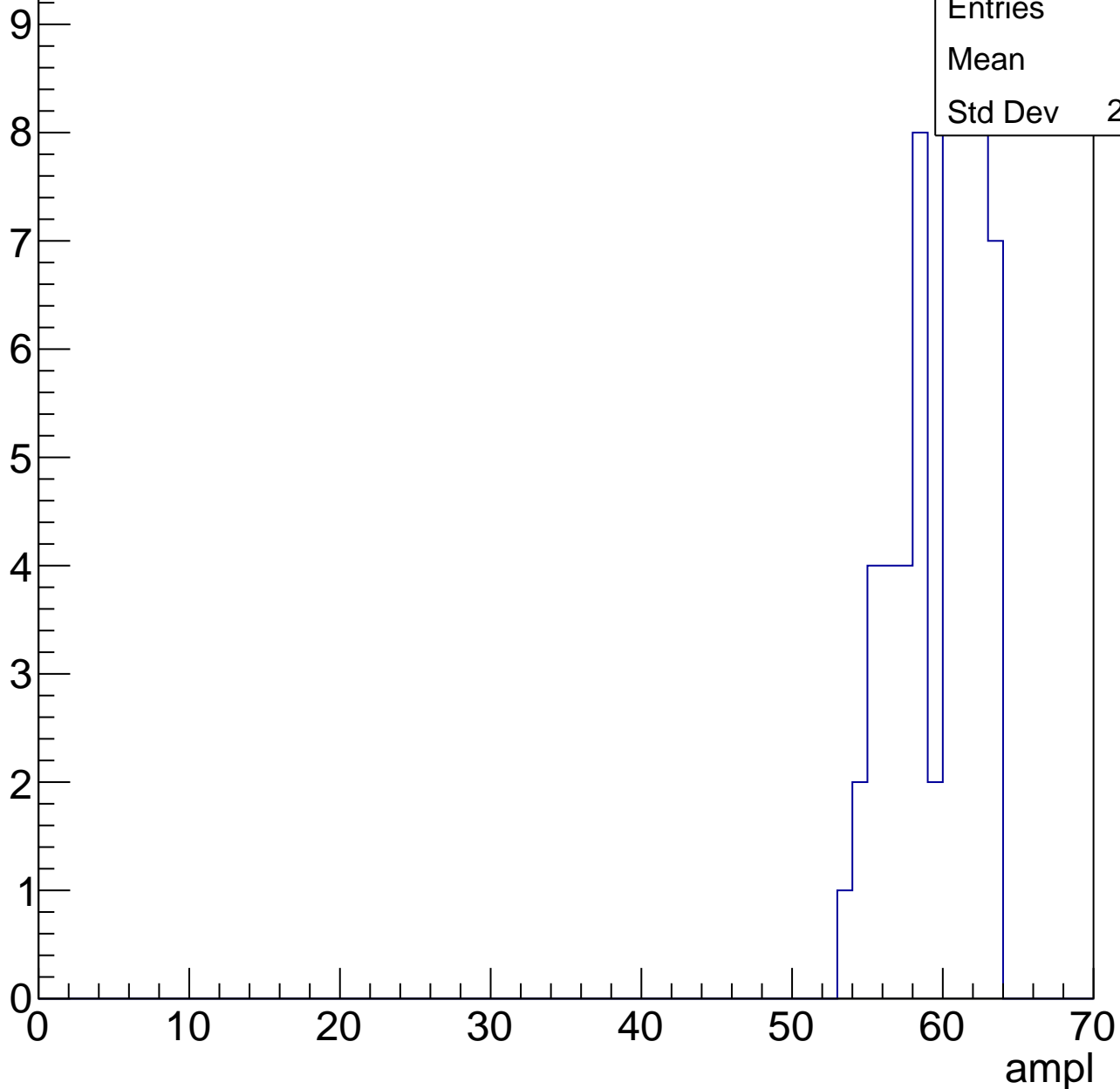
Entries	49
Mean	54.9
Std Dev	3.442



# B1L102S, U21-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	57
Mean	59.3
Std Dev	2.746

# B1L102S, U21-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

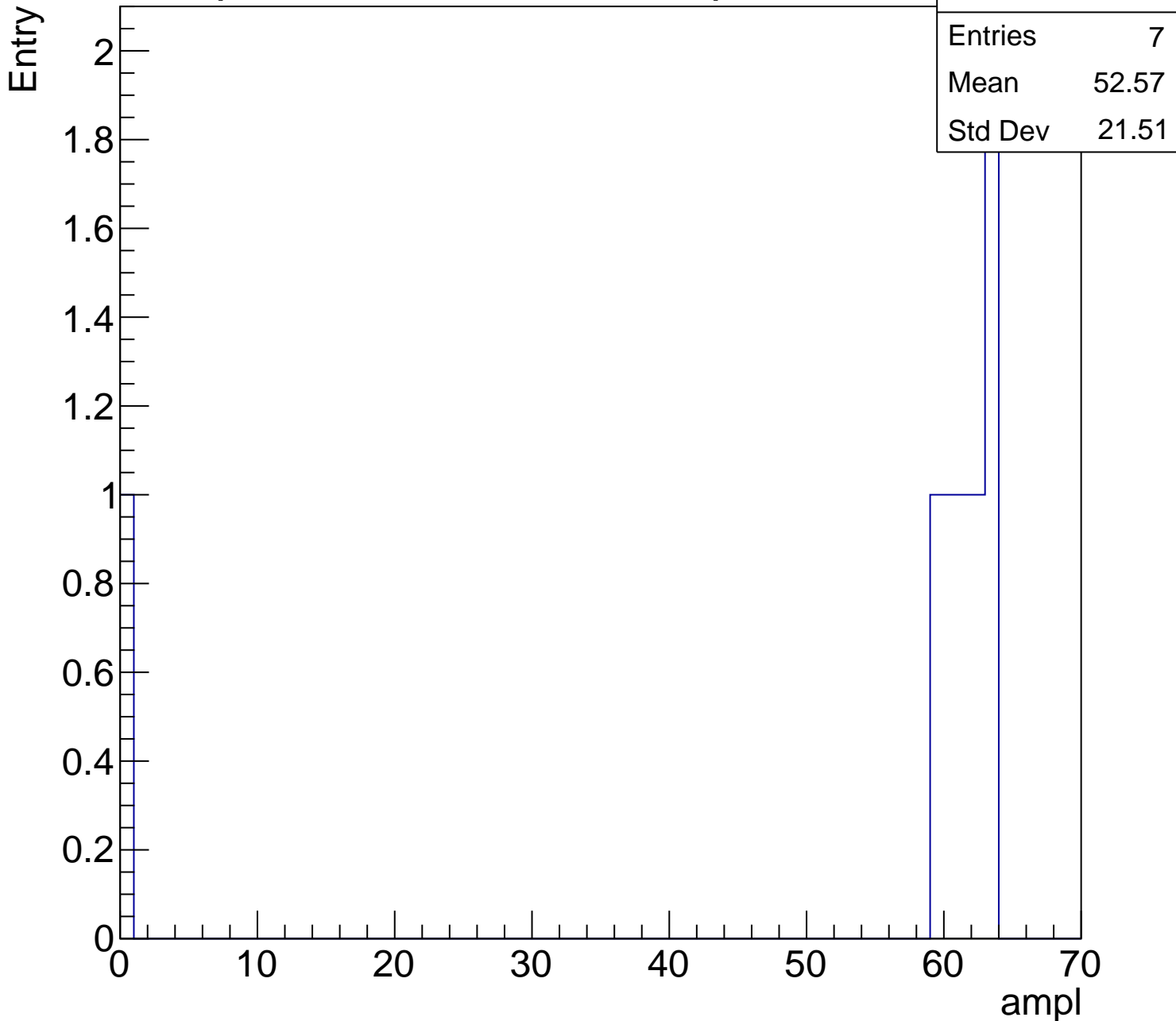
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	52.57
Std Dev	21.51

ampl

0 10 20 30 40 50 60 70





# B1L102S, U21-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U21-ch97, adc0

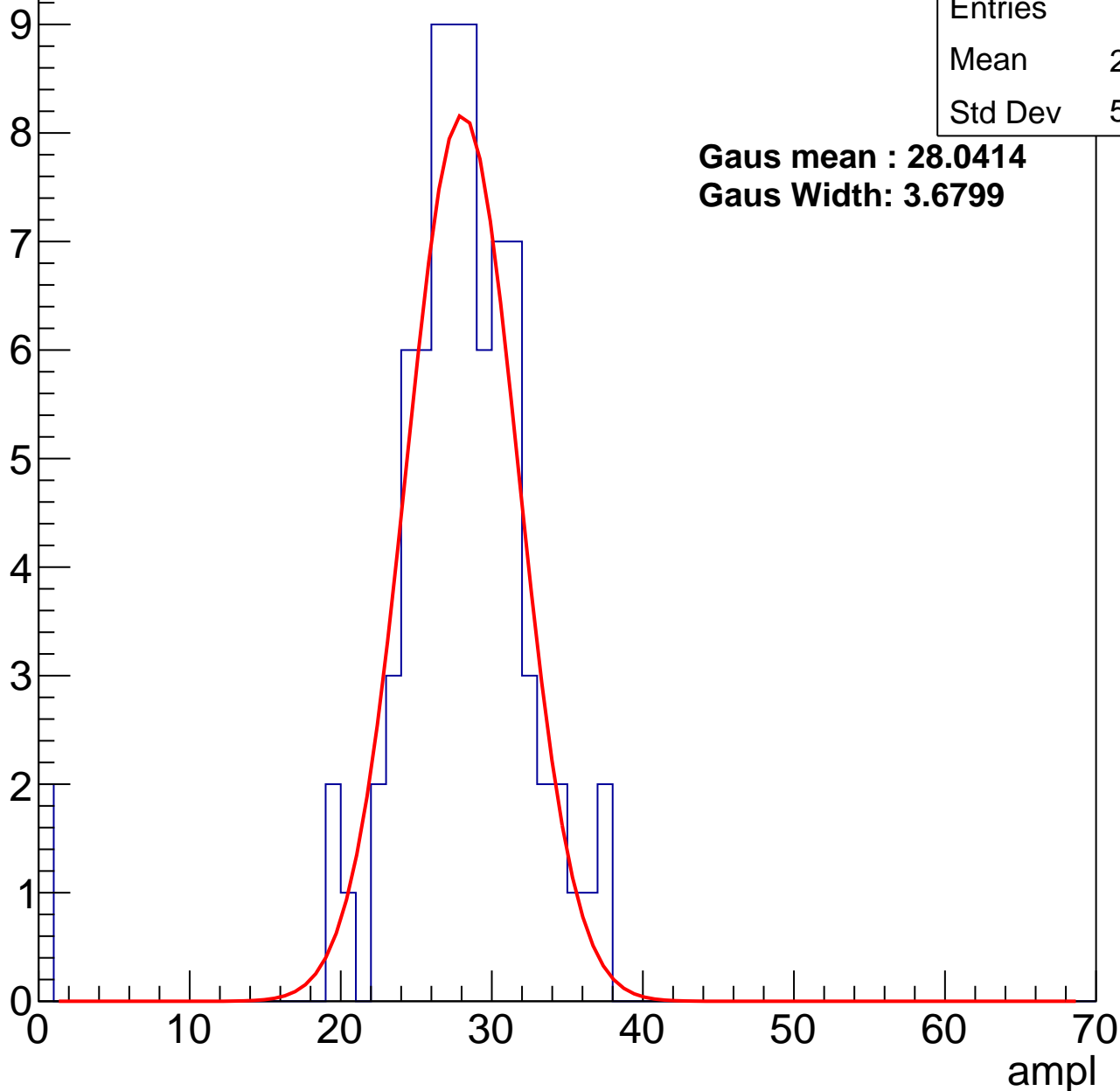
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	27.12
Std Dev	5.719

**Gaus mean : 28.0414**

**Gaus Width: 3.6799**



# B1L102S, U21-ch97, adc1

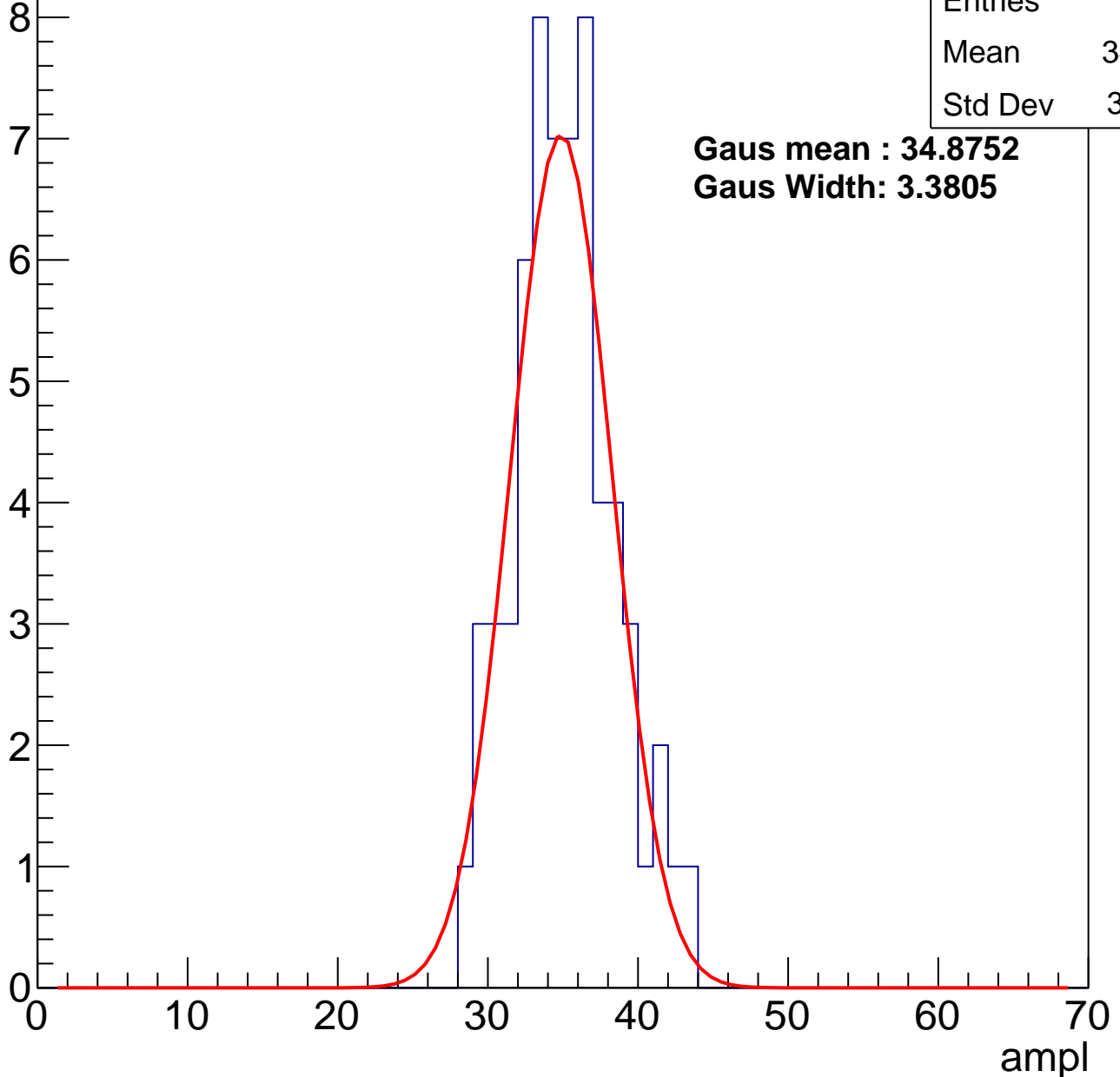
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	34.66
Std Dev	3.321

**Gaus mean : 34.8752**

**Gaus Width: 3.3805**



# B1L102S, U21-ch97, adc2

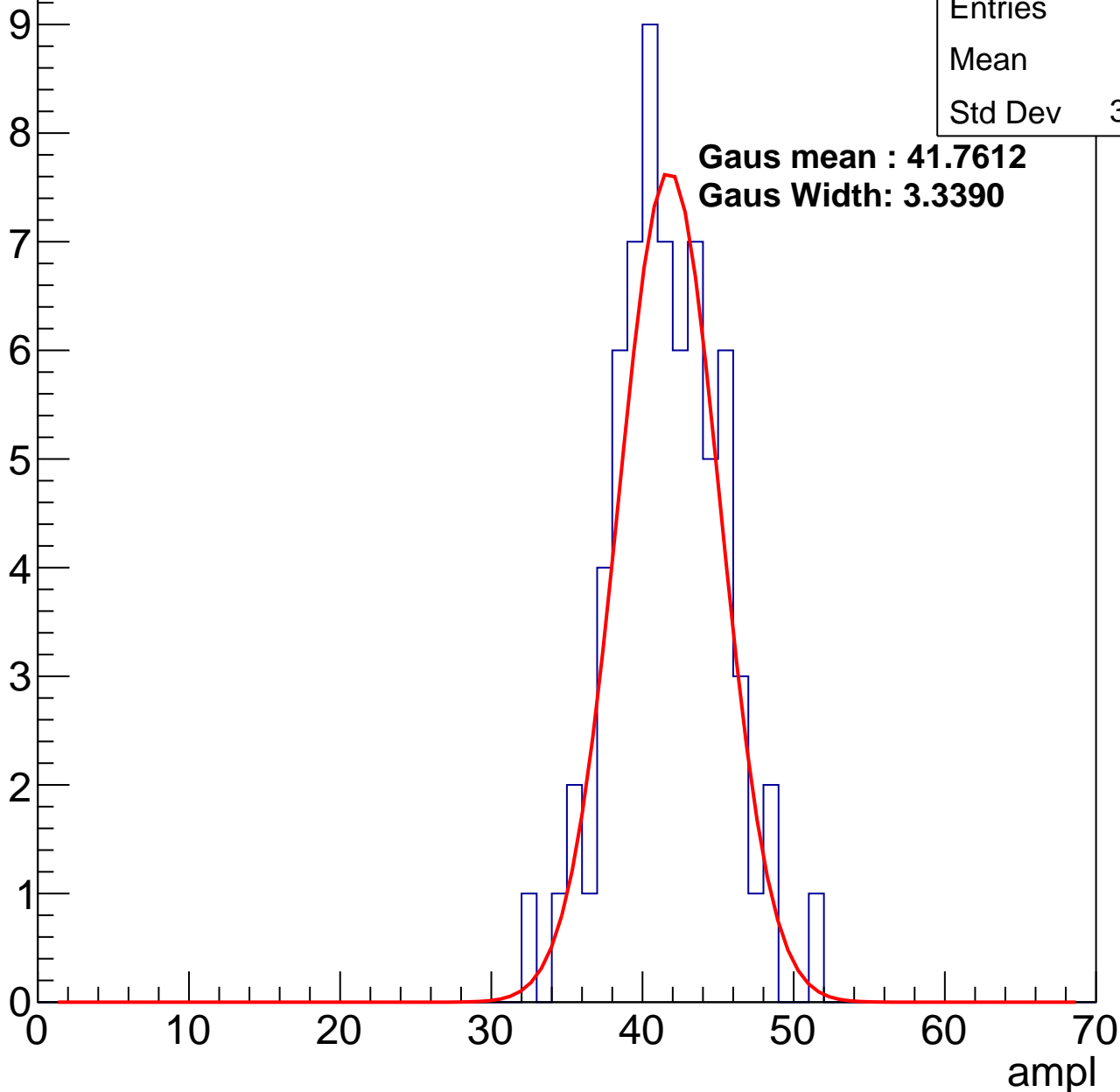
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	41.2
Std Dev	3.537

**Gaus mean : 41.7612**

**Gaus Width: 3.3390**

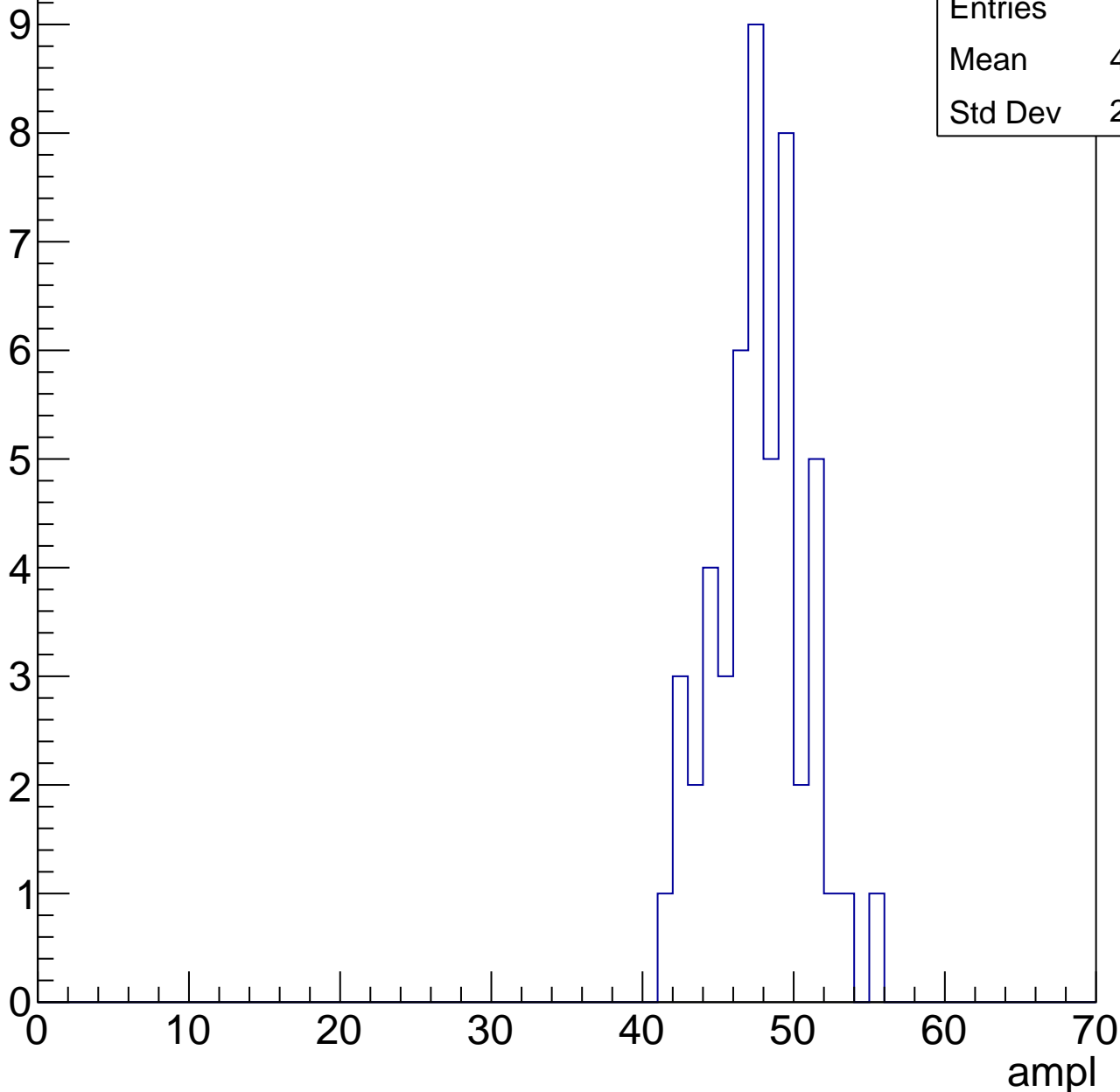


# B1L102S, U21-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	47.25
Std Dev	2.983

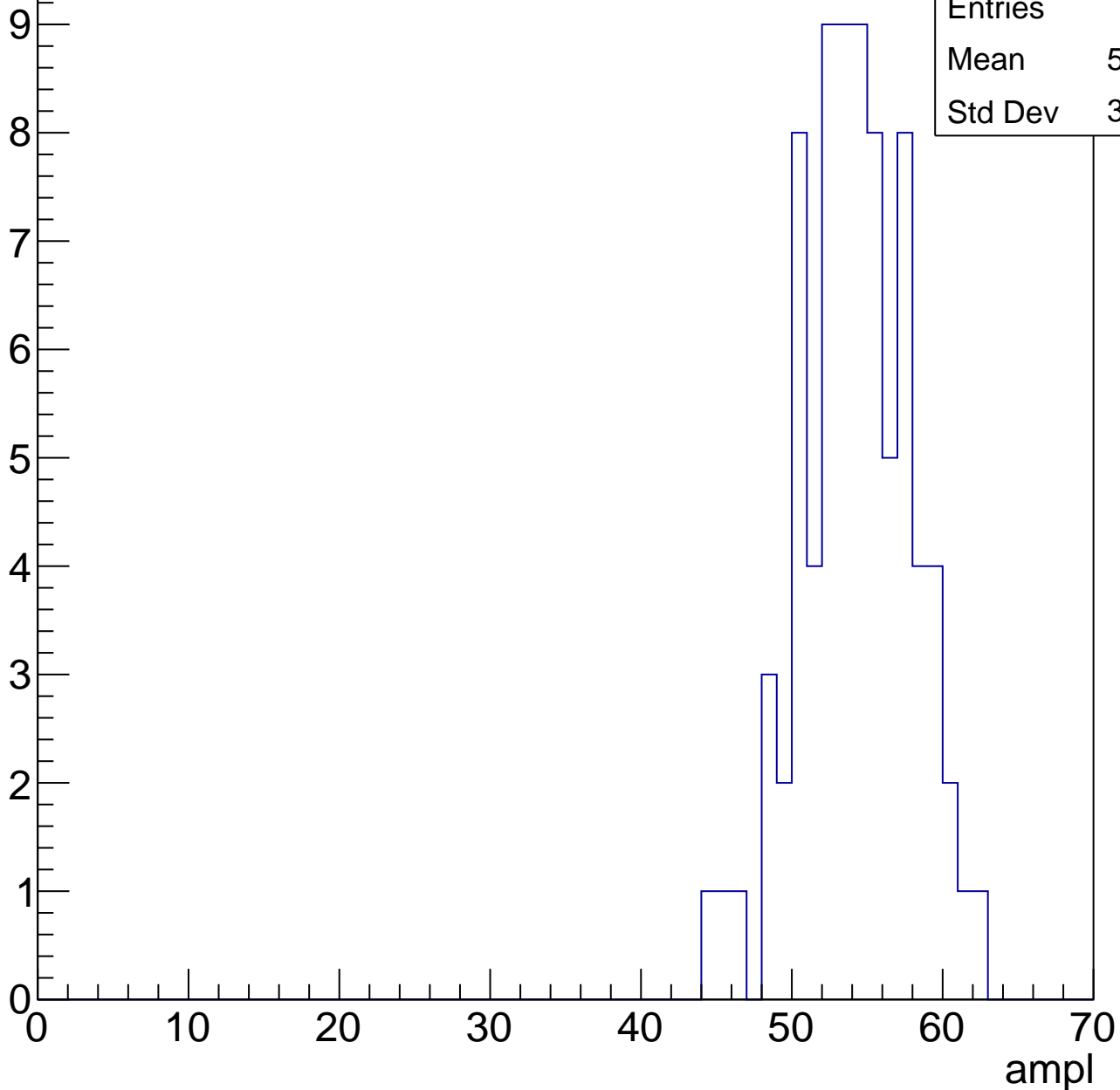


# B1L102S, U21-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	53.74
Std Dev	3.632



# B1L102S, U21-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	59.84
Std Dev	2.444

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

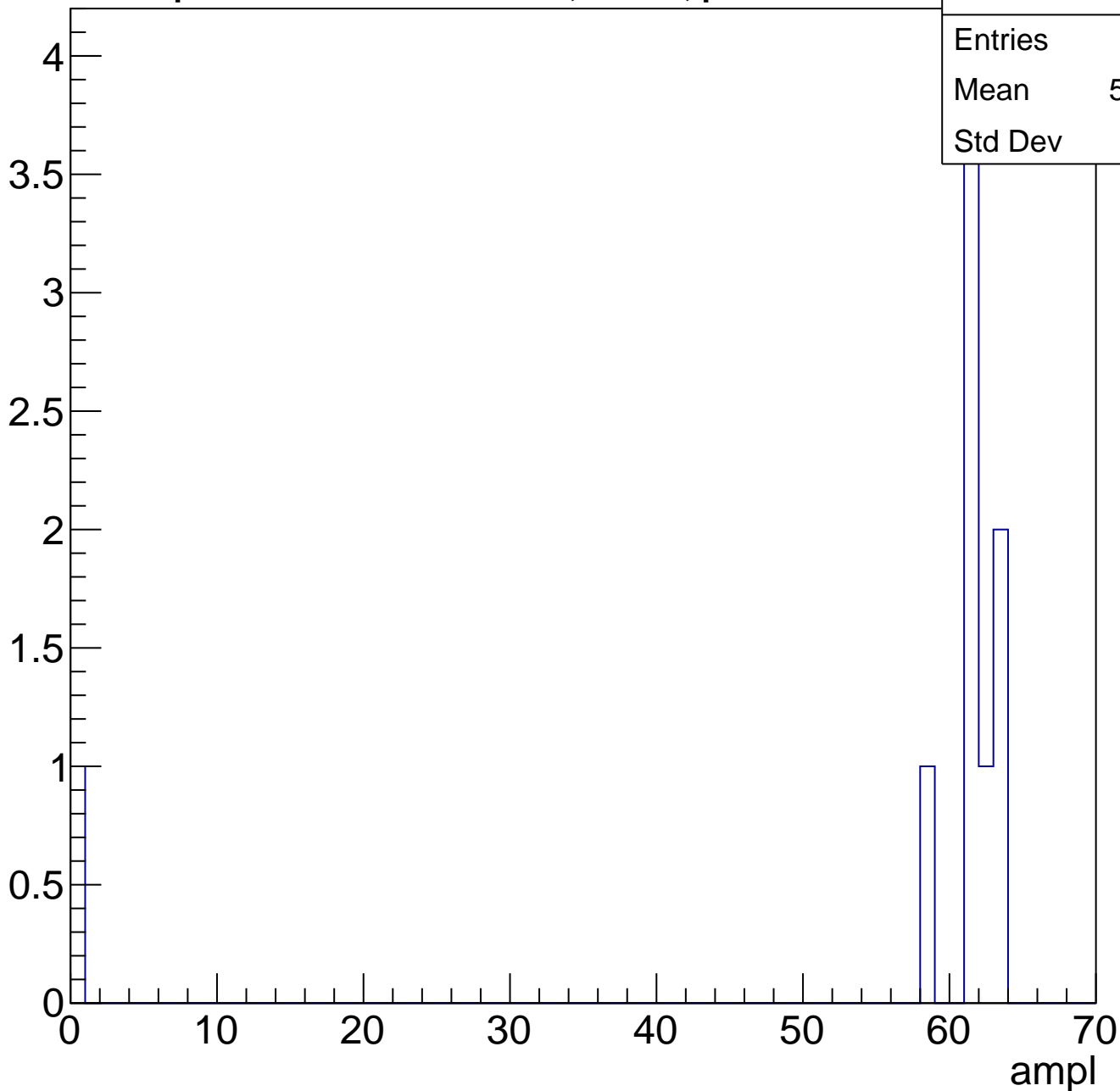
7

8

# B1L102S, U21-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U21-ch98, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	82
Mean	27.99
Std Dev	3.621

**Gaus mean : 28.7254**

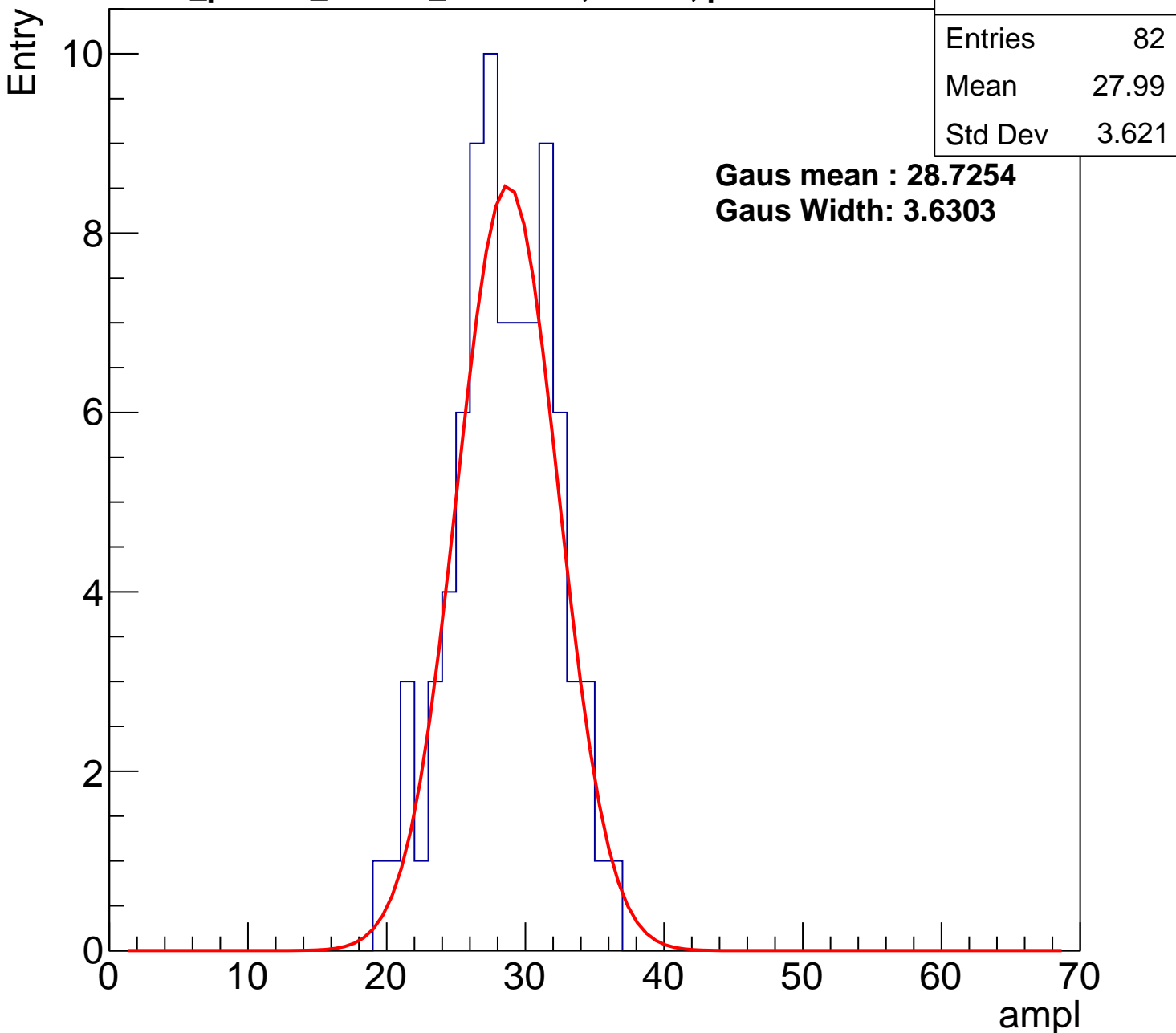
**Gaus Width: 3.6303**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U21-ch98, adc1

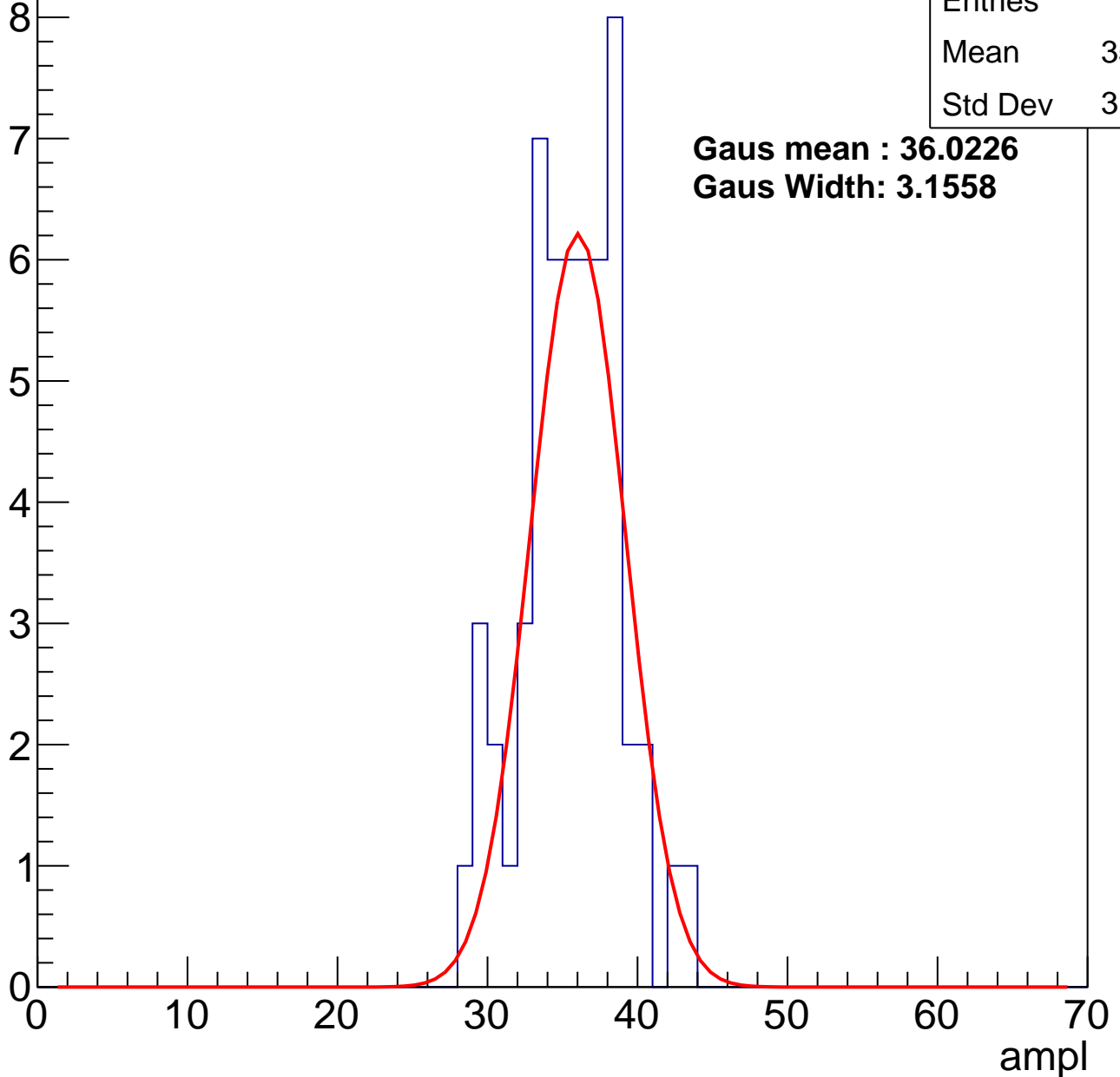
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	35.13
Std Dev	3.248

**Gaus mean : 36.0226**

**Gaus Width: 3.1558**



# B1L102S, U21-ch98, adc2

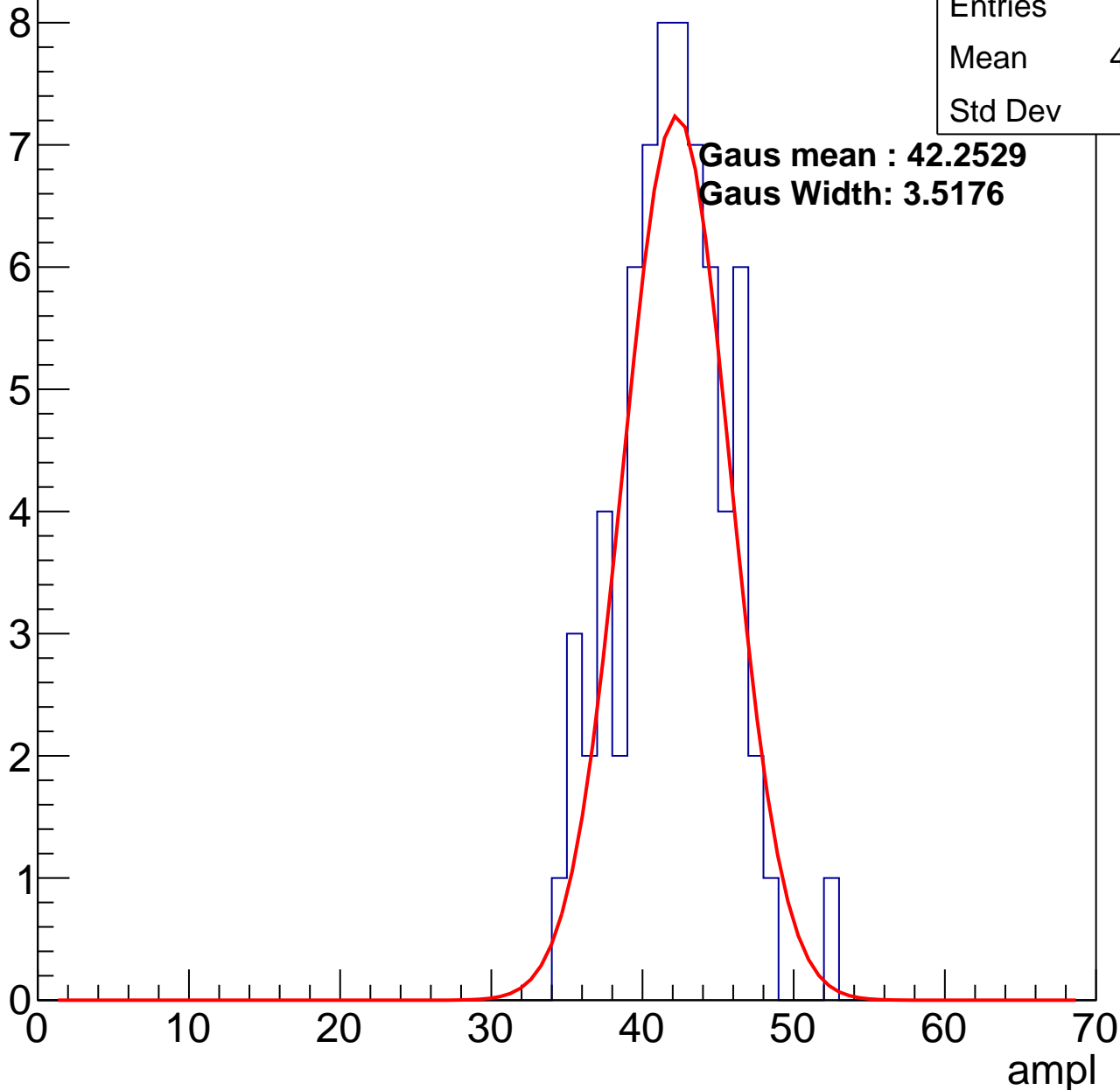
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	41.59
Std Dev	3.52

**Gaus mean : 42.2529**

**Gaus Width: 3.5176**

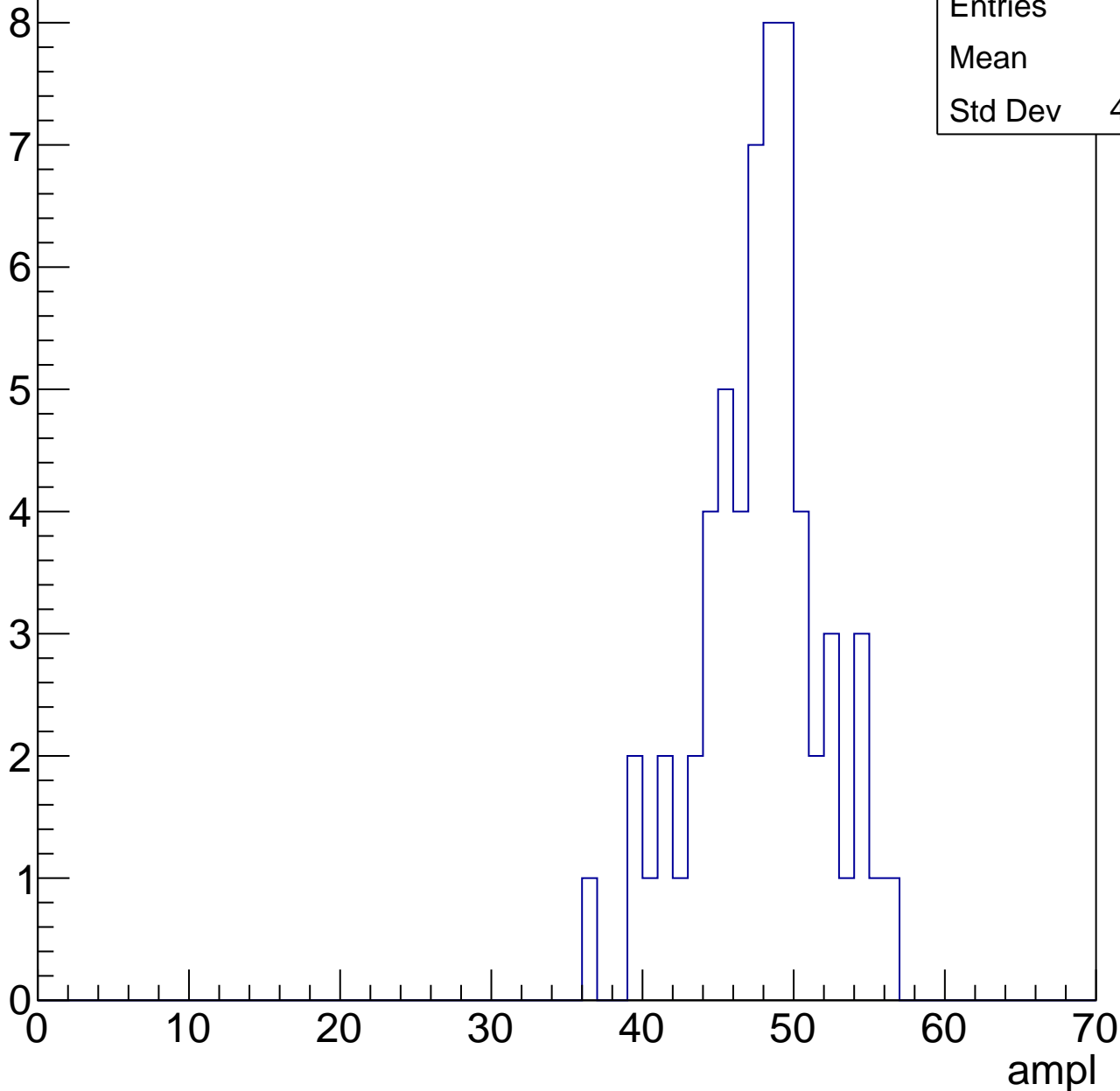


# B1L102S, U21-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	47.3
Std Dev	4.067

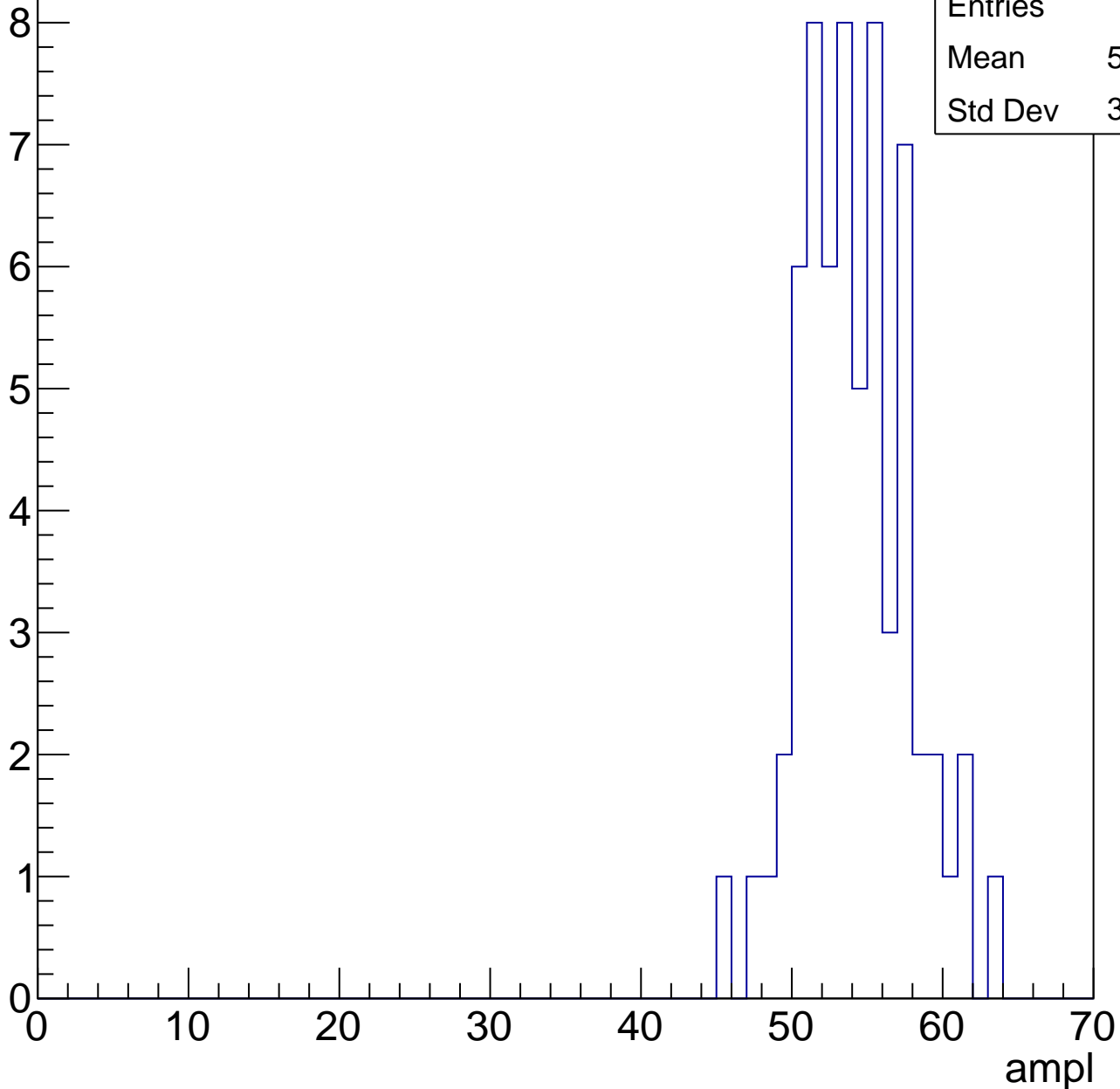


# B1L102S, U21-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	53.72
Std Dev	3.515

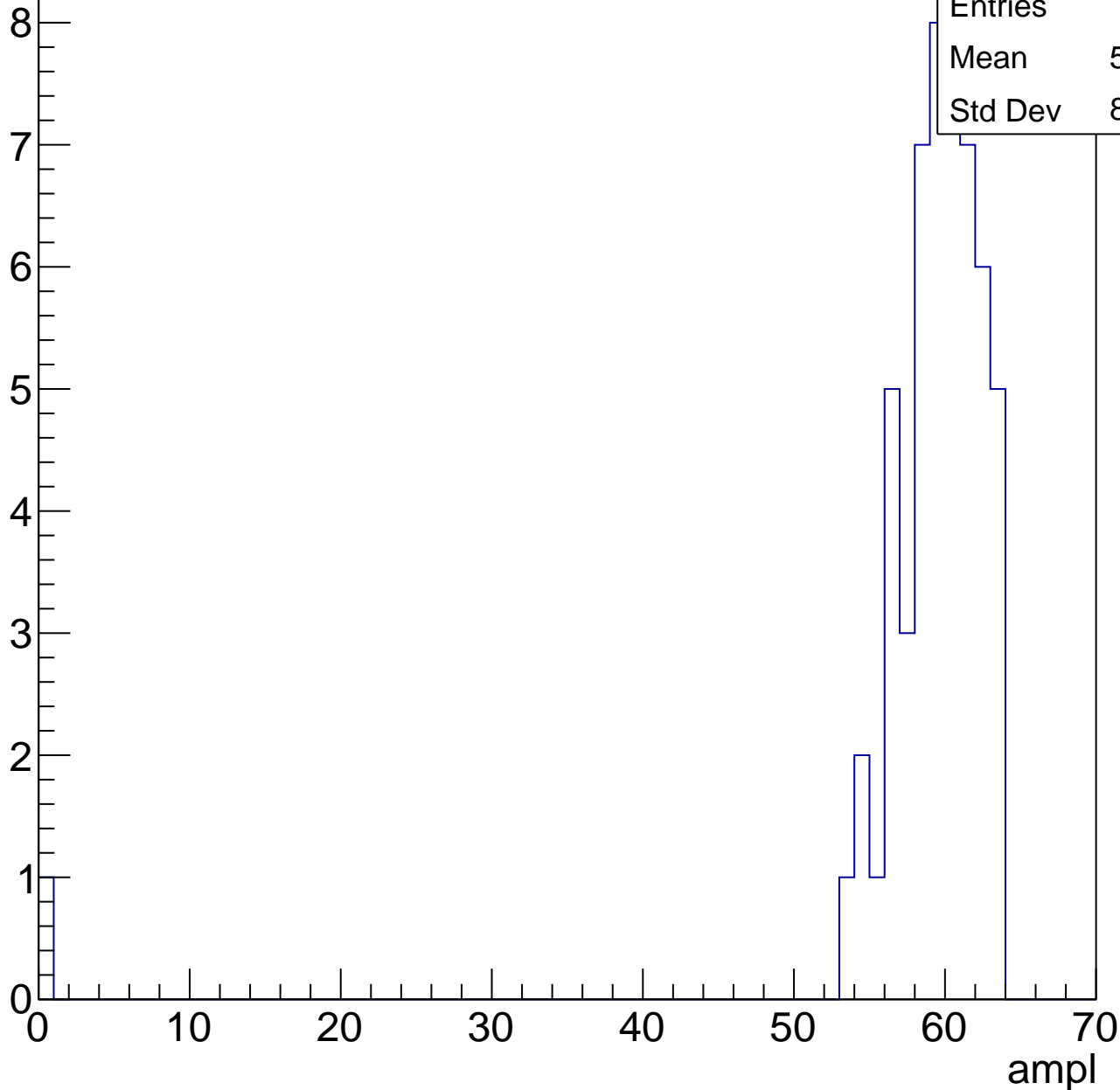


# B1L102S, U21-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

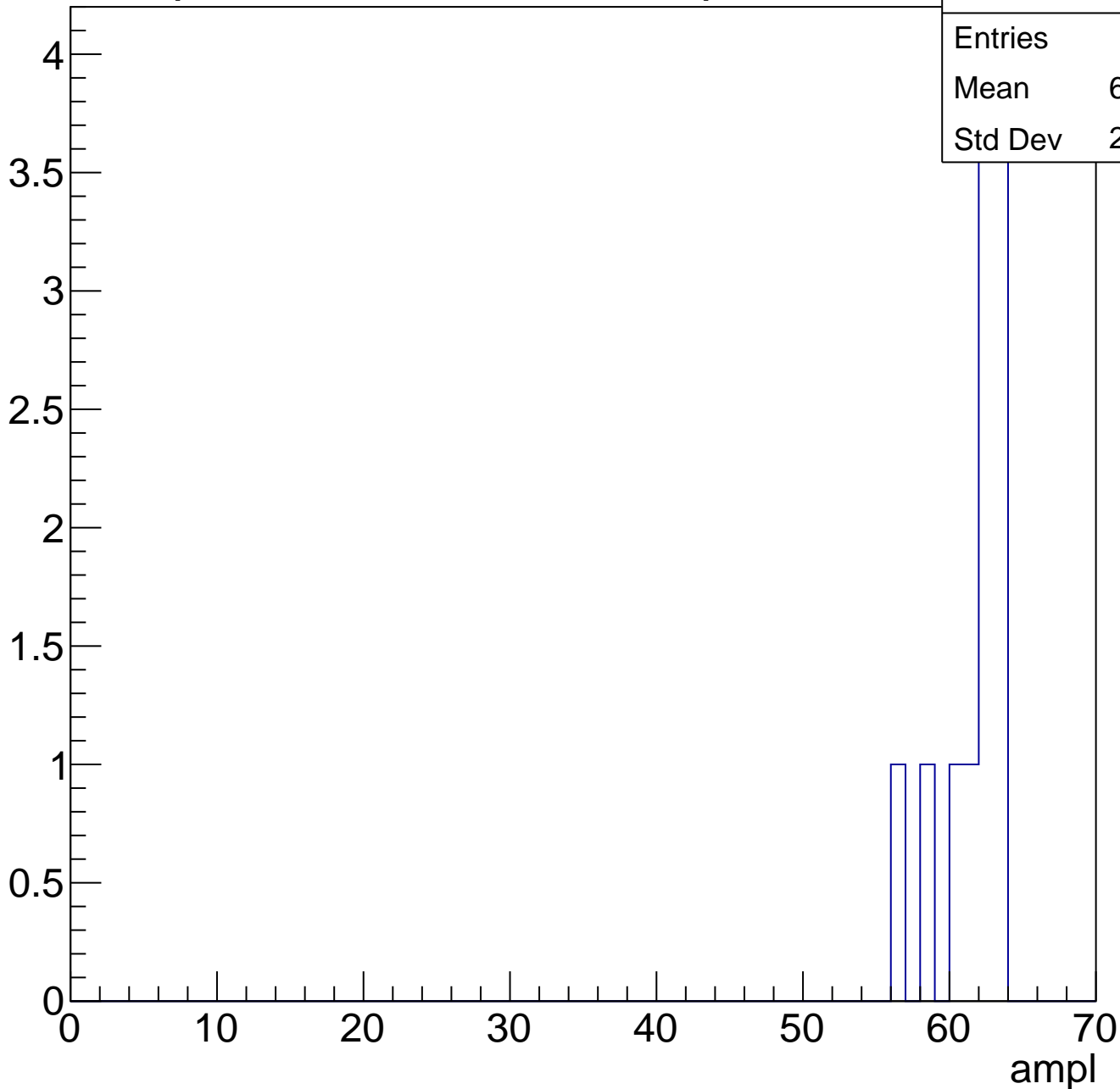
Entries	54
Mean	58.13
Std Dev	8.362



# B1L102S, U21-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

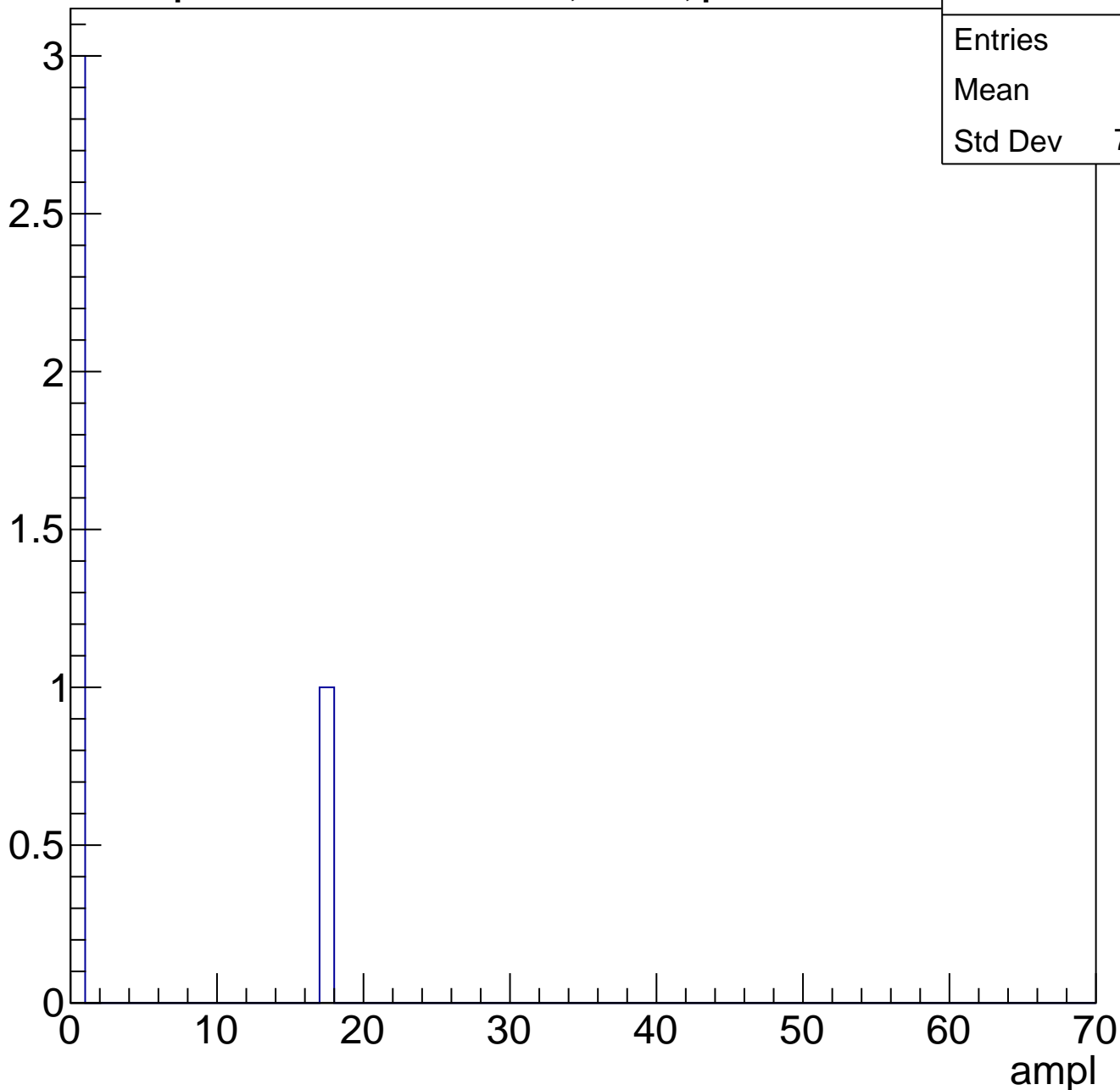




# B1L102S, U21-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	4
Mean	4.25
Std Dev	7.361

# B1L102S, U21-ch99, adc0

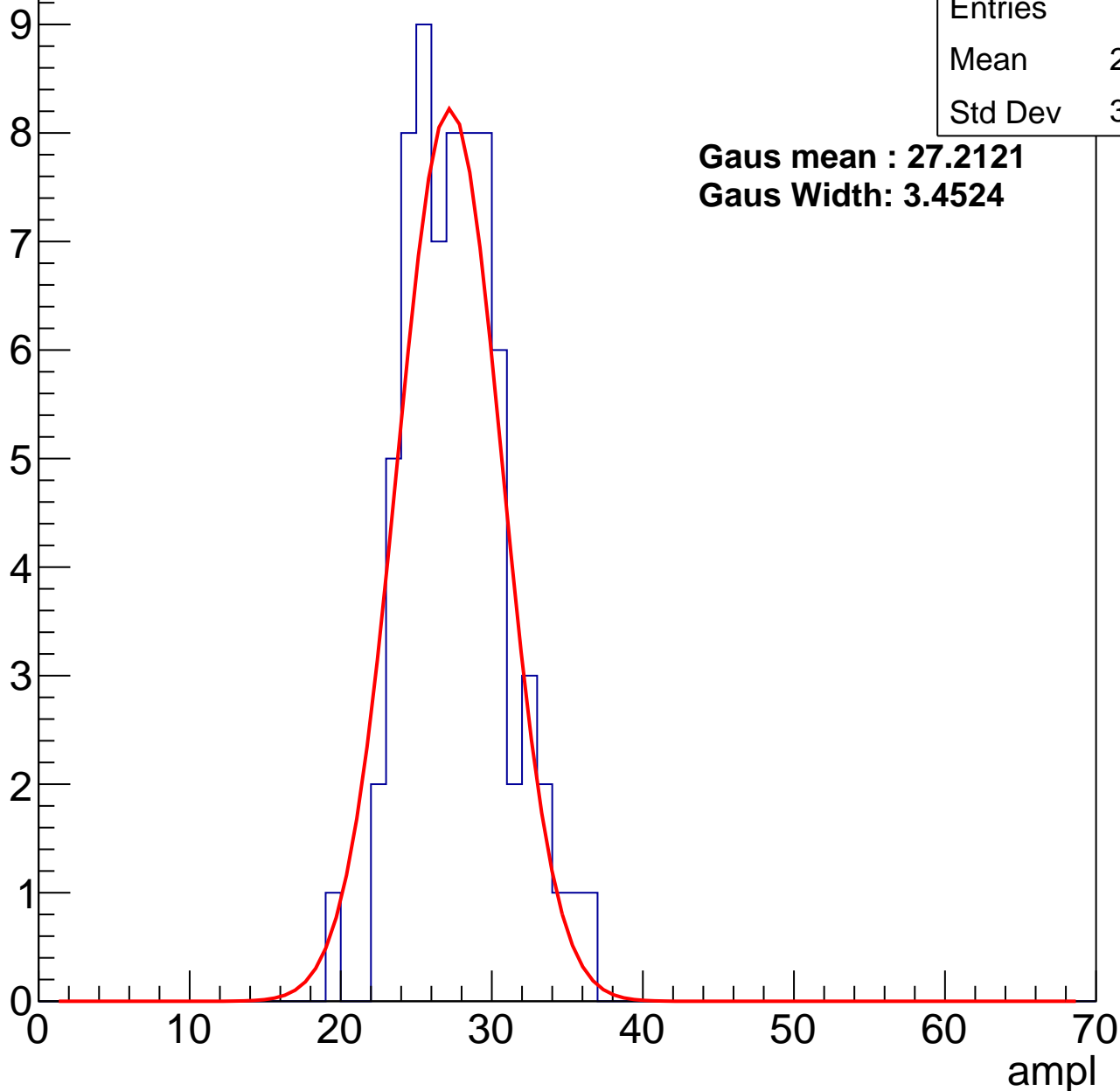
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	27.19
Std Dev	3.277

**Gaus mean : 27.2121**

**Gaus Width: 3.4524**



# B1L102S, U21-ch99, adc1

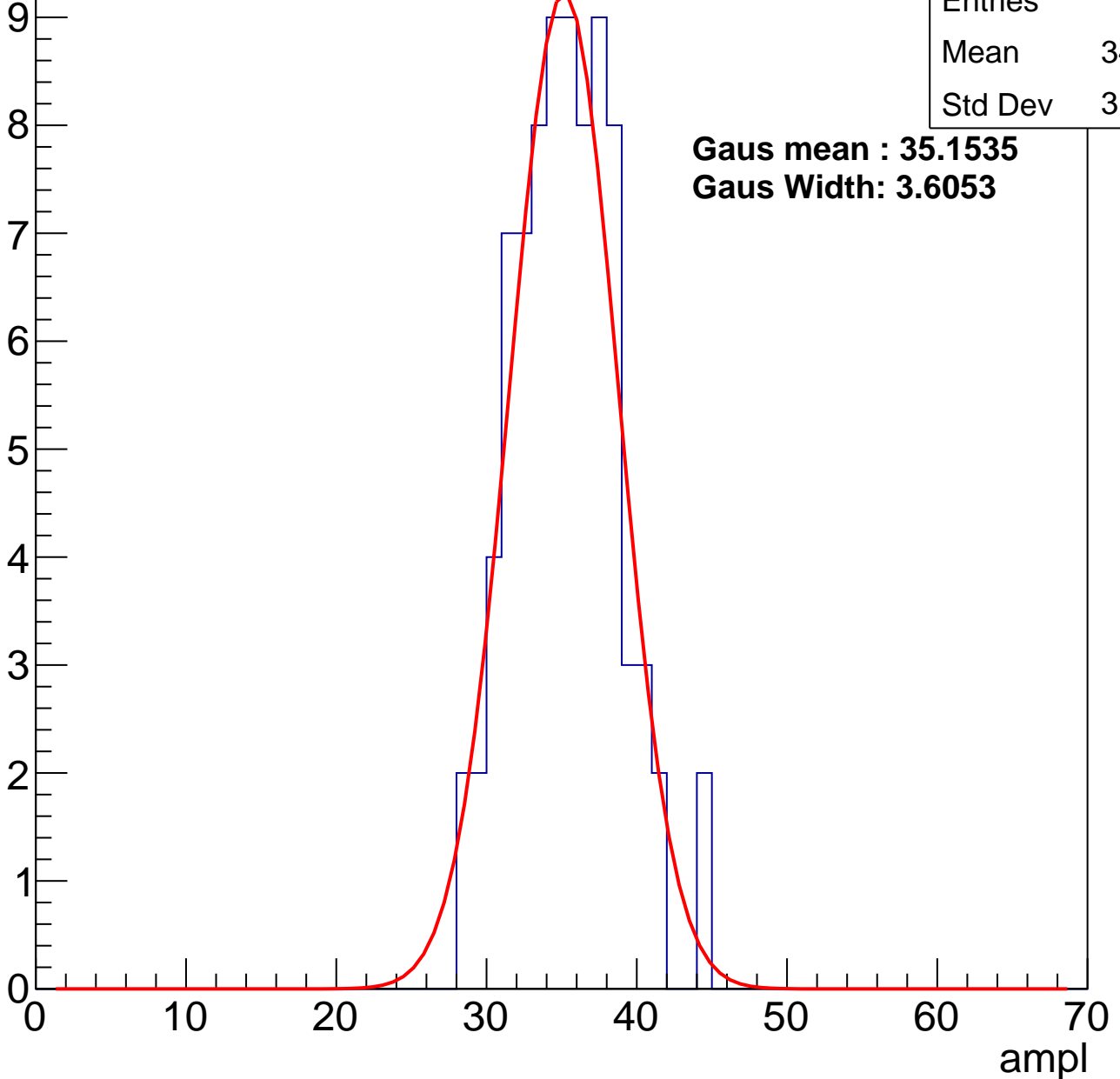
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	83
Mean	34.84
Std Dev	3.396

**Gaus mean : 35.1535**

**Gaus Width: 3.6053**



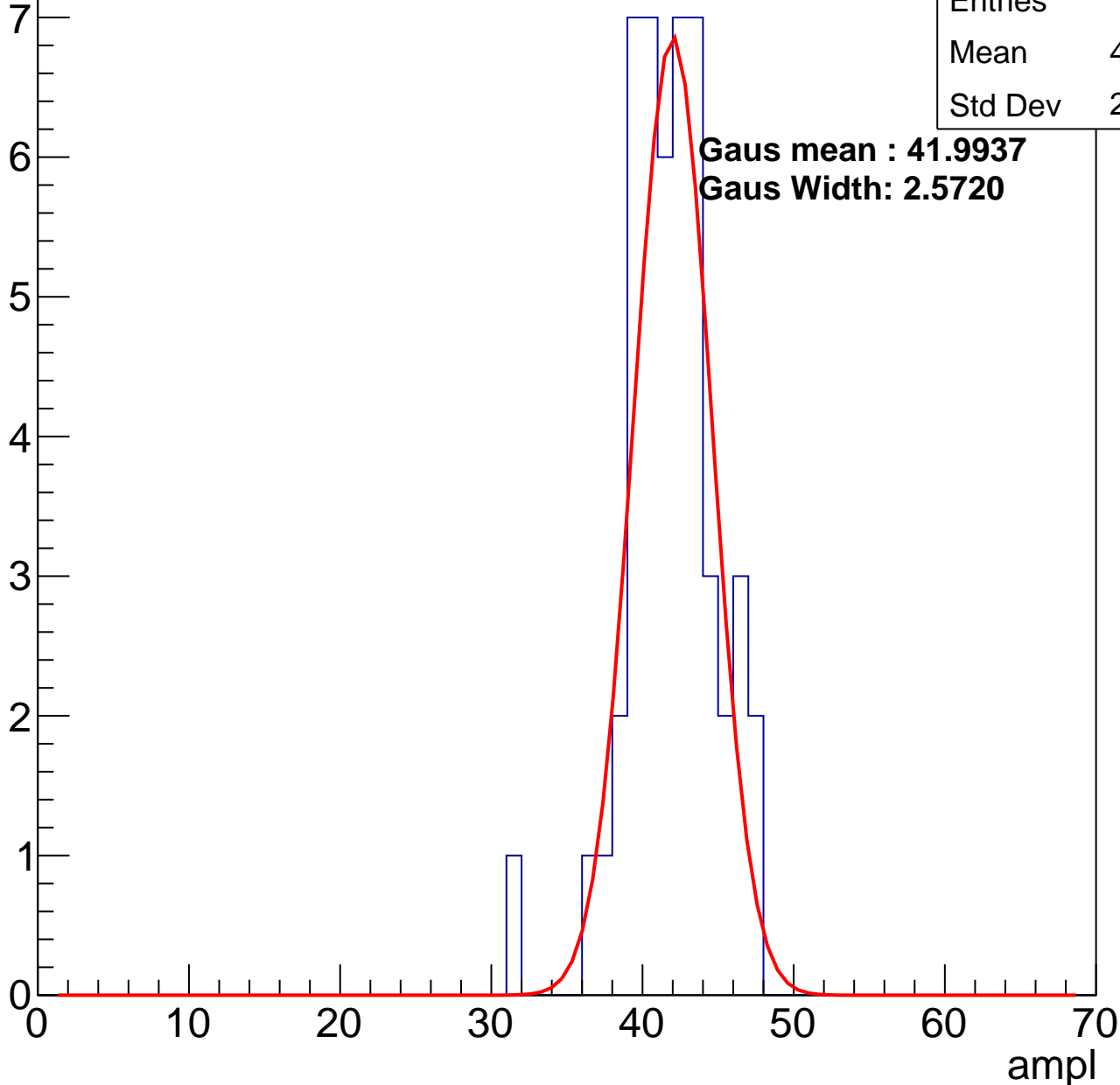
# B1L102S, U21-ch99, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	41.39
Std Dev	2.954

**Gaus mean : 41.9937**  
**Gaus Width: 2.5720**

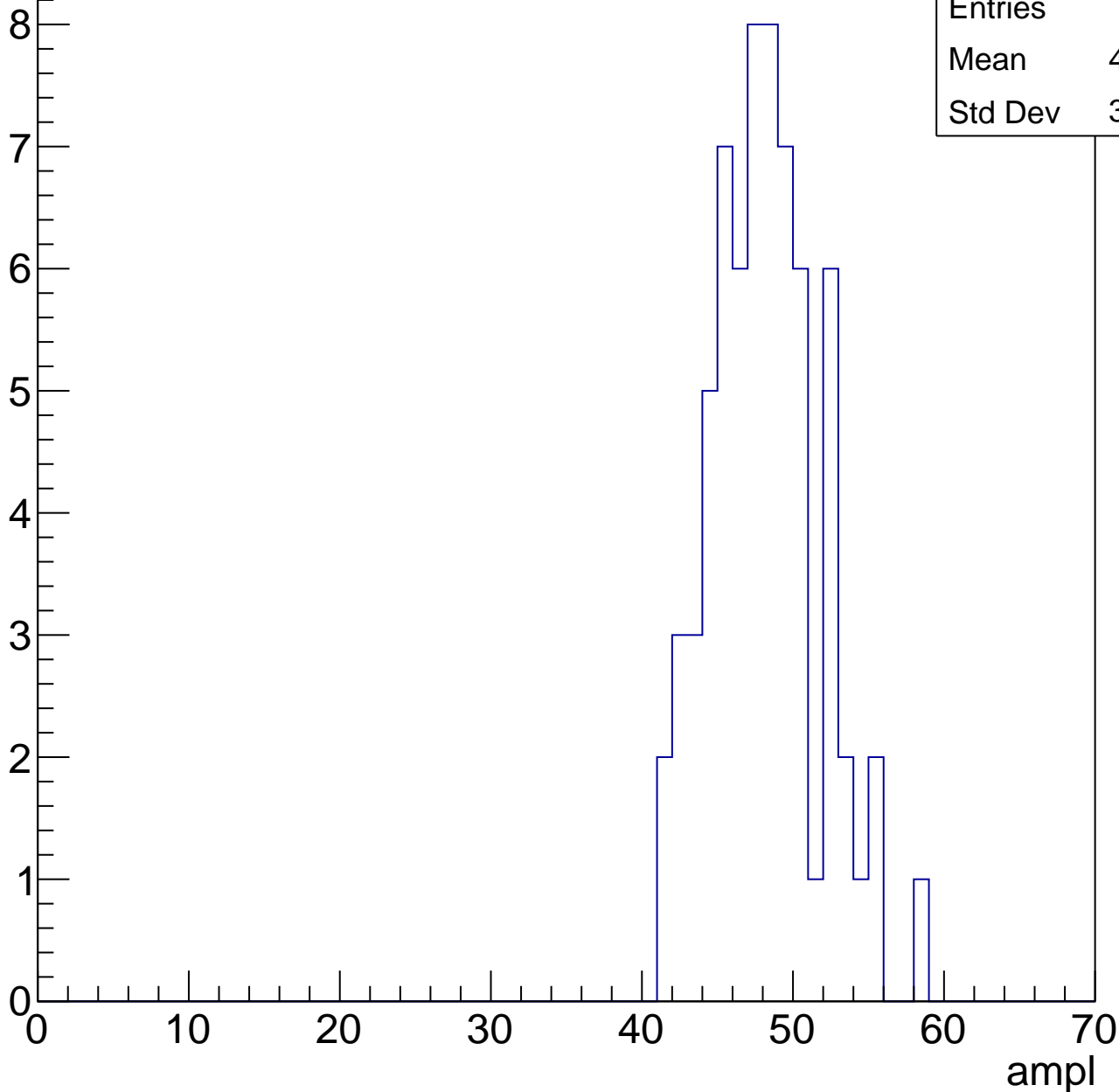


# B1L102S, U21-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	47.68
Std Dev	3.575

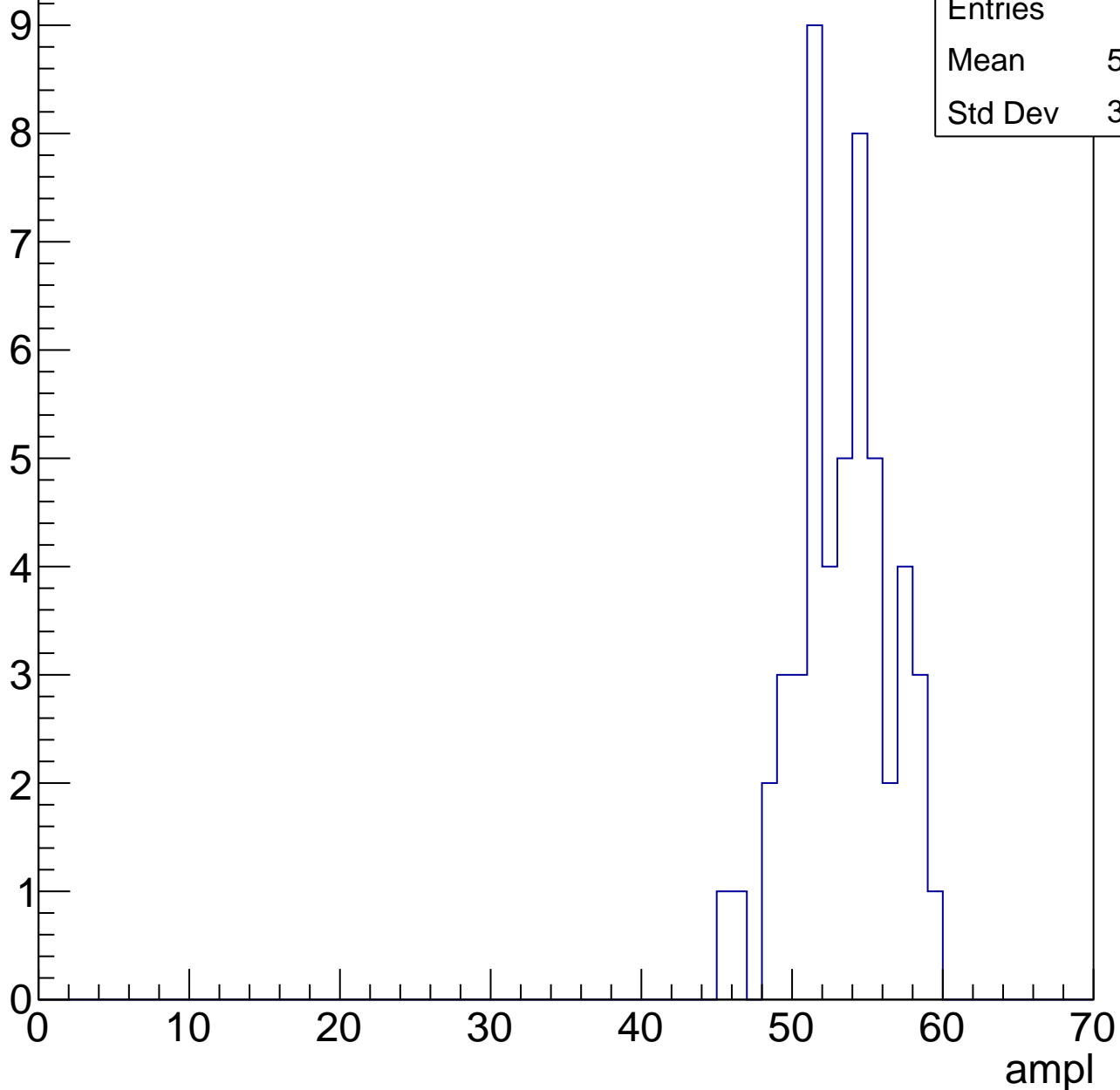


# B1L102S, U21-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	52.86
Std Dev	3.125

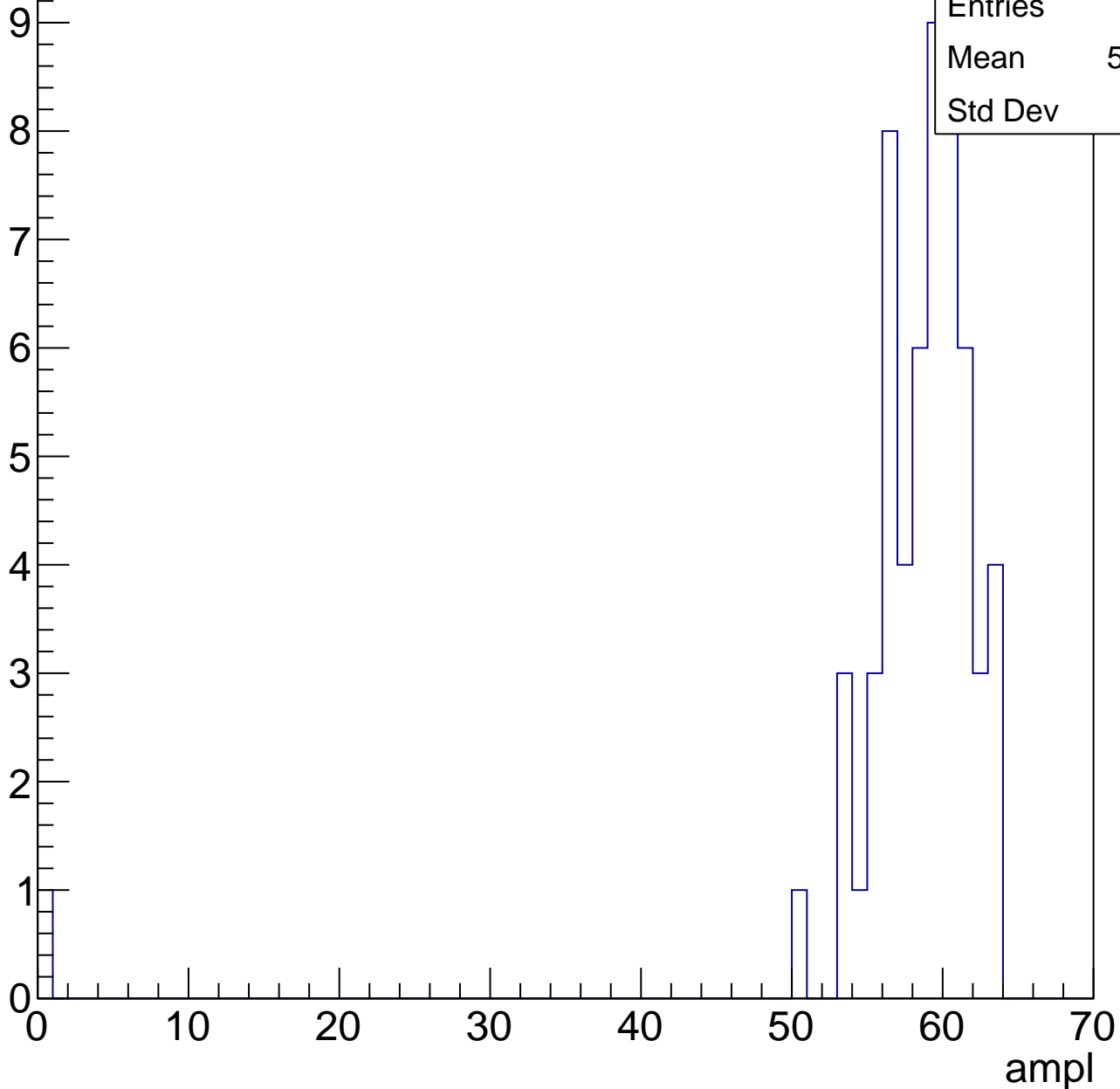


# B1L102S, U21-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	57.36
Std Dev	8.1

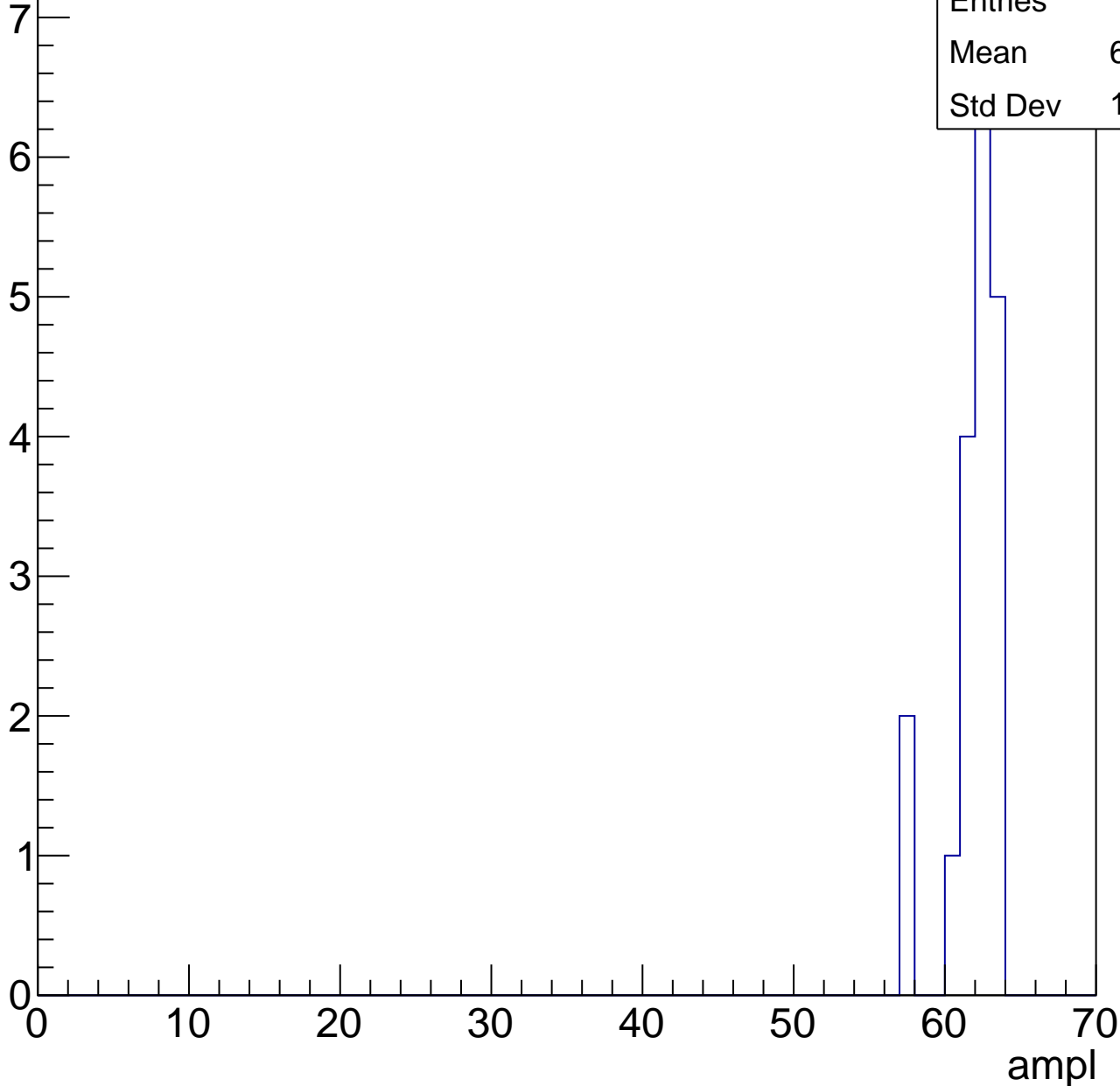


# B1L102S, U21-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	19
Mean	61.42
Std Dev	1.726





# B1L102S, U21-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch100, adc0

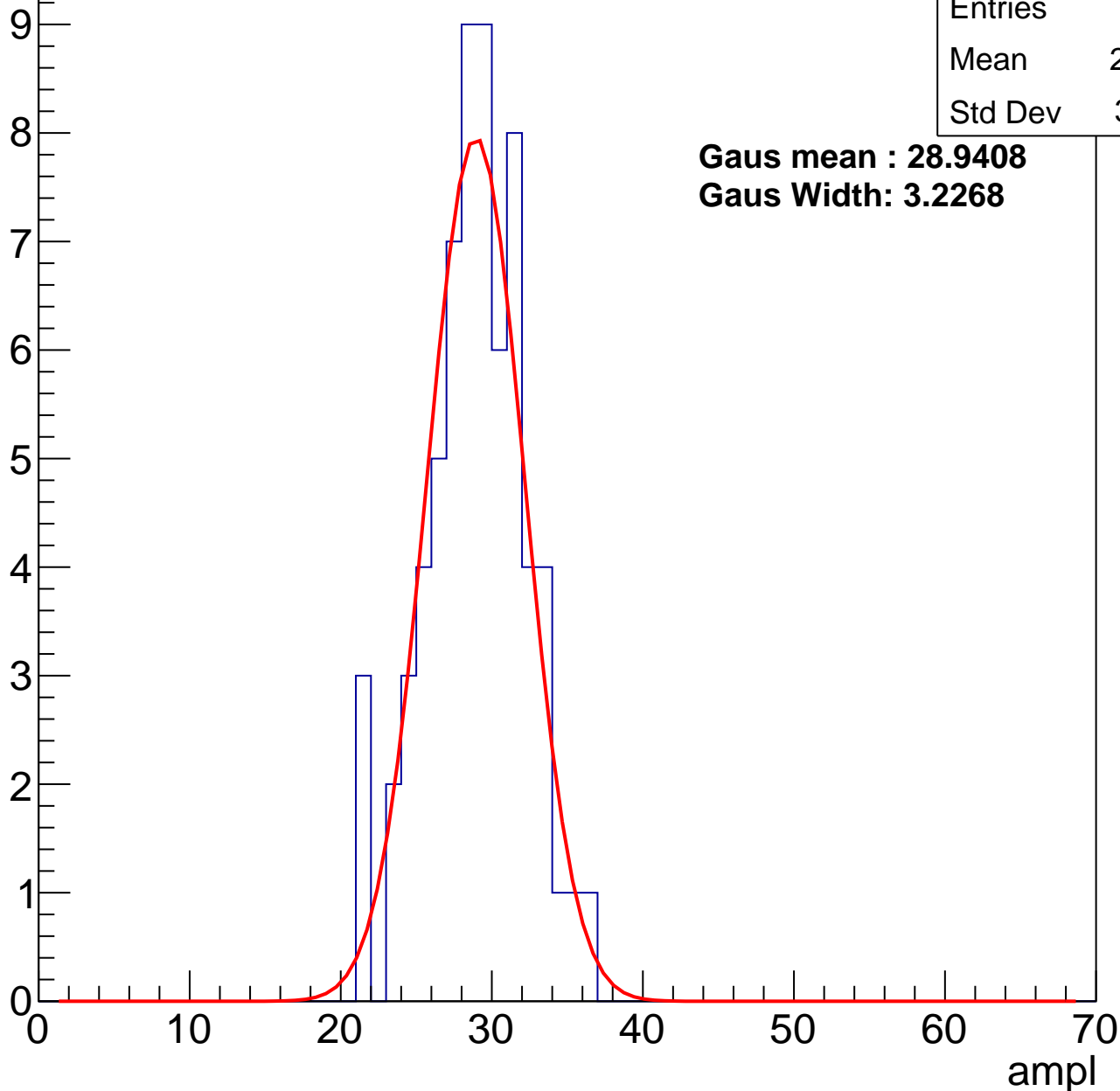
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	28.45
Std Dev	3.261

**Gaus mean : 28.9408**

**Gaus Width: 3.2268**



# B1L102S, U21-ch100, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	84
Mean	36.27
Std Dev	3.821

**Gaus mean : 36.7765**

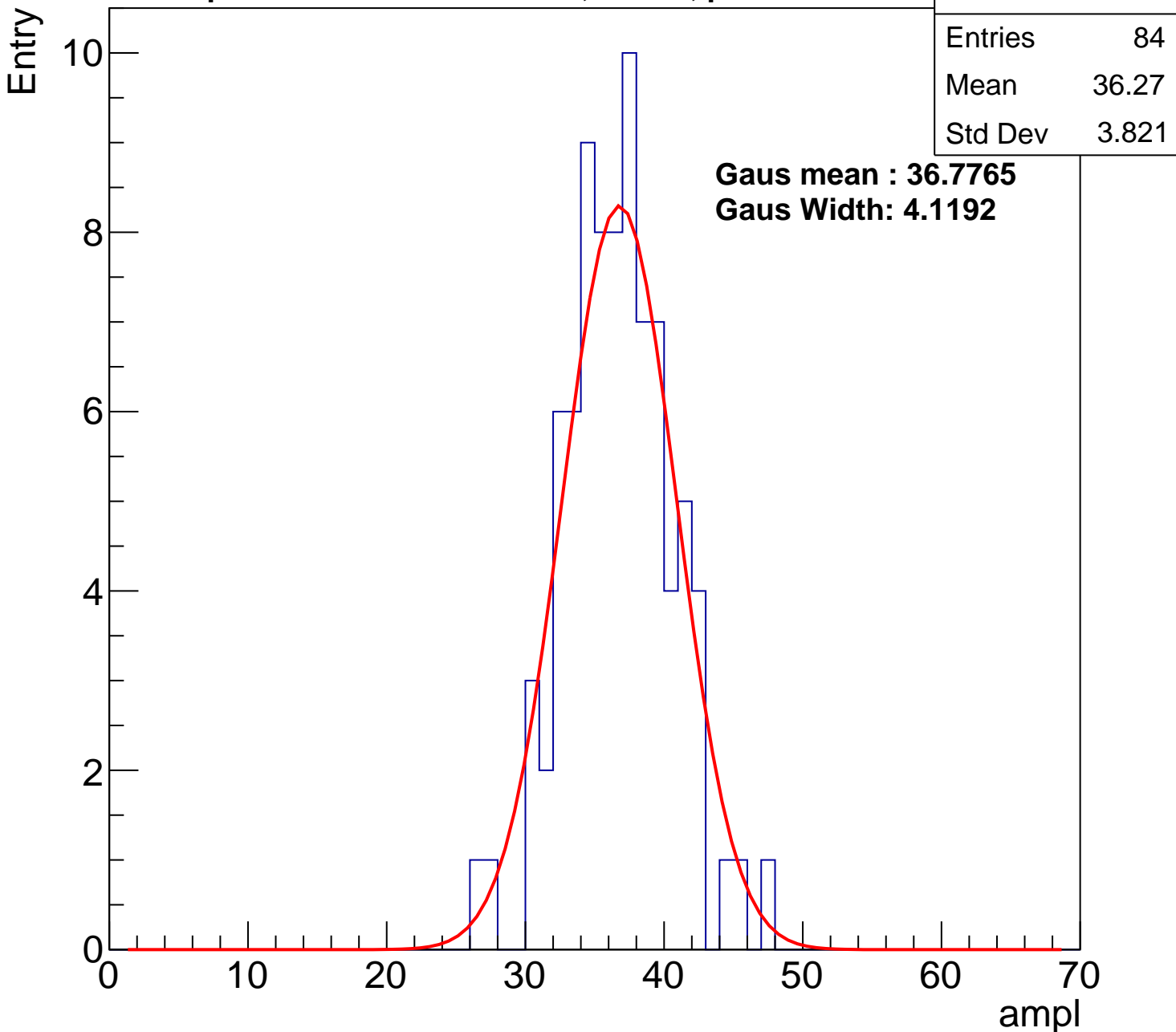
**Gaus Width: 4.1192**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L102S, U21-ch100, adc2

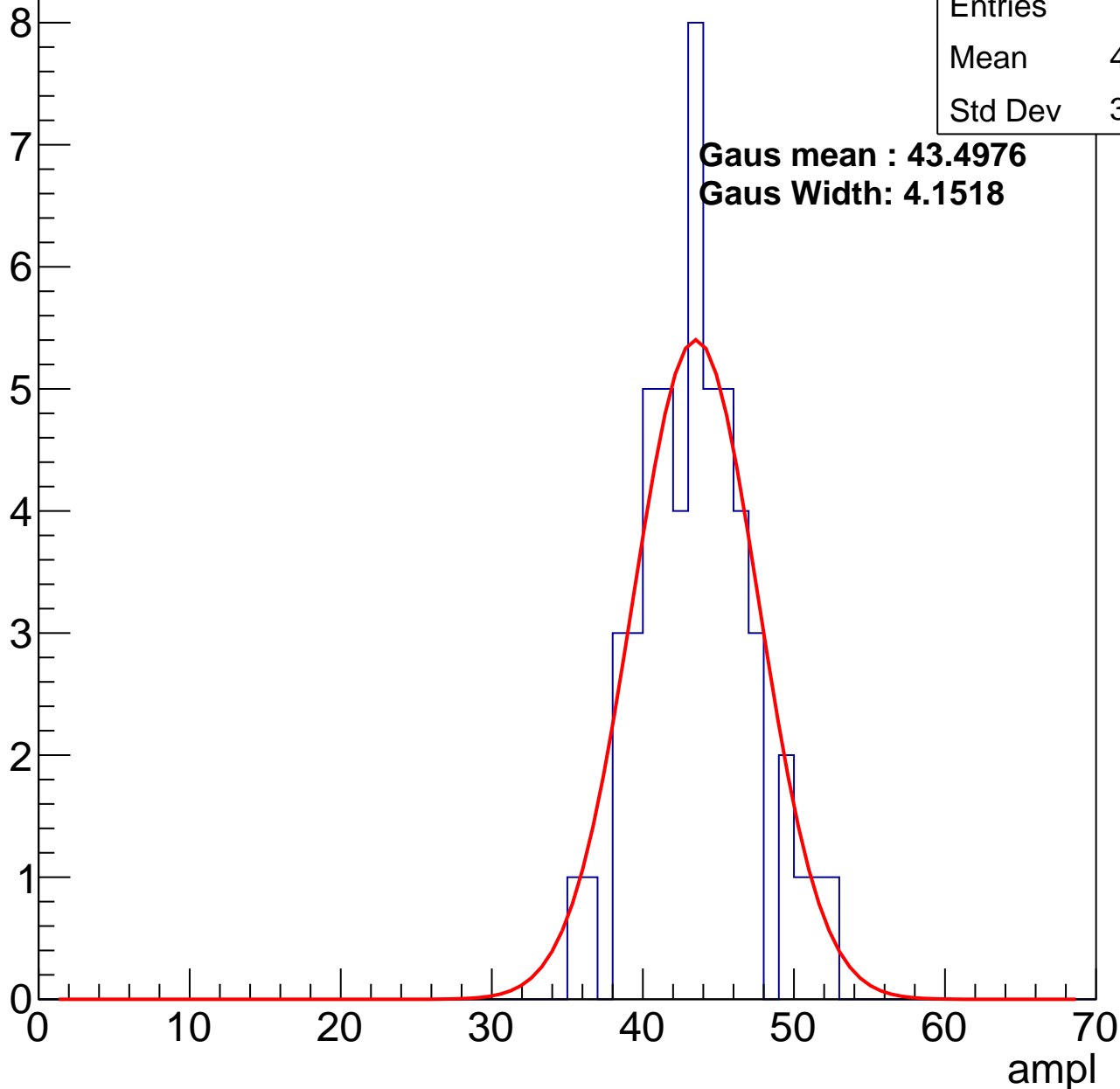
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	43.08
Std Dev	3.615

**Gaus mean : 43.4976**

**Gaus Width: 4.1518**

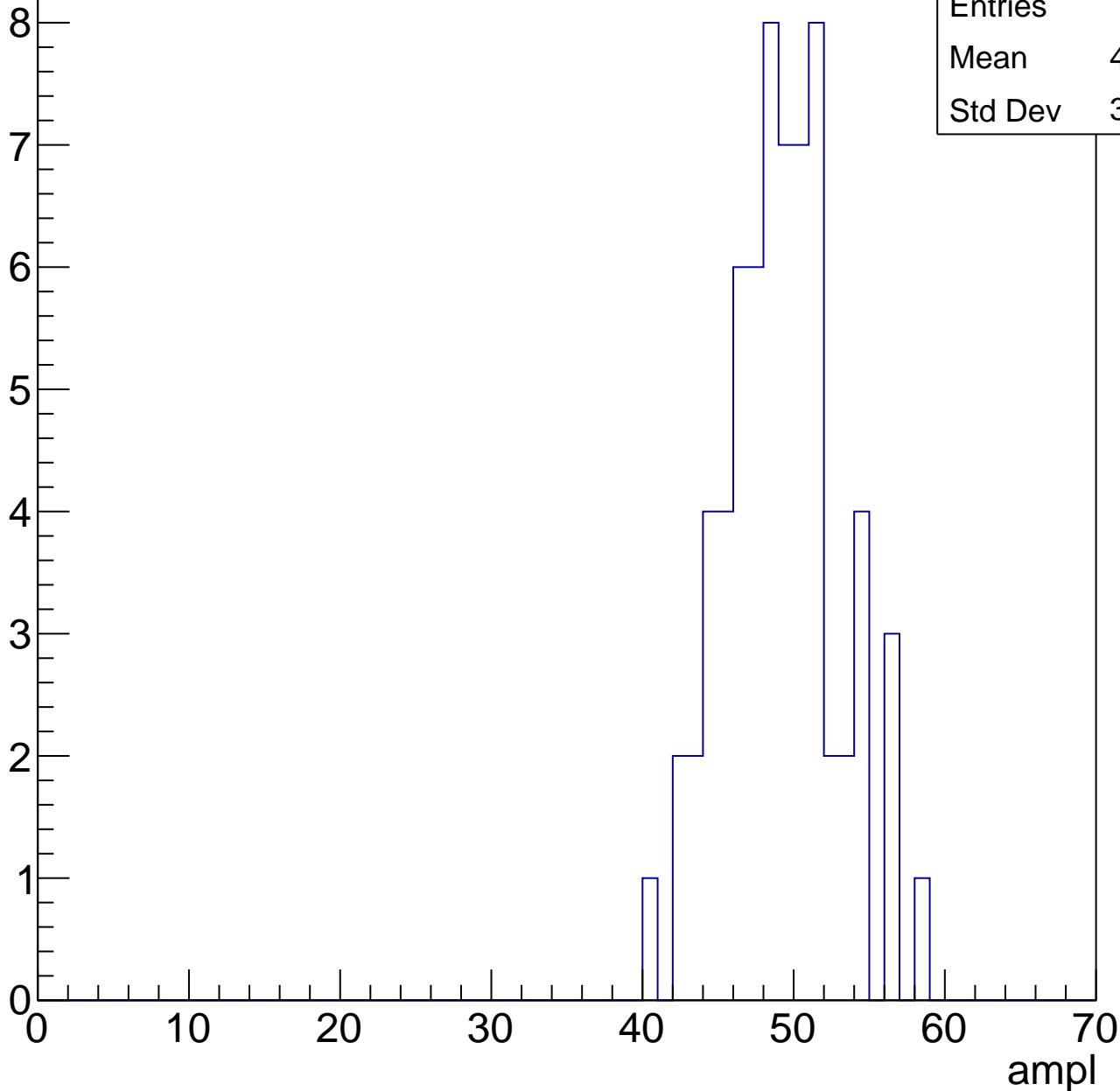


# B1L102S, U21-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	48.67
Std Dev	3.687

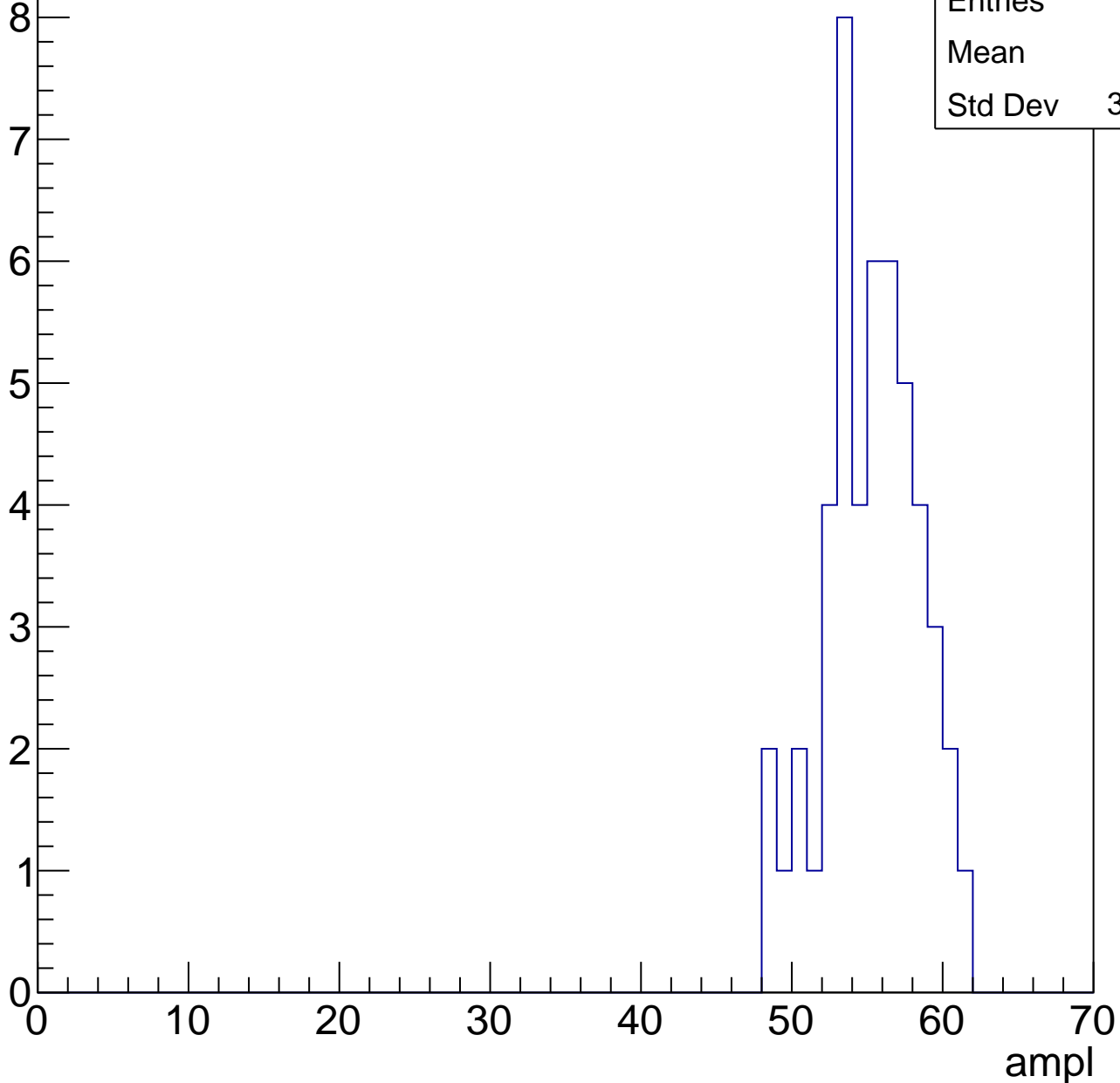


# B1L102S, U21-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	54.8
Std Dev	3.084

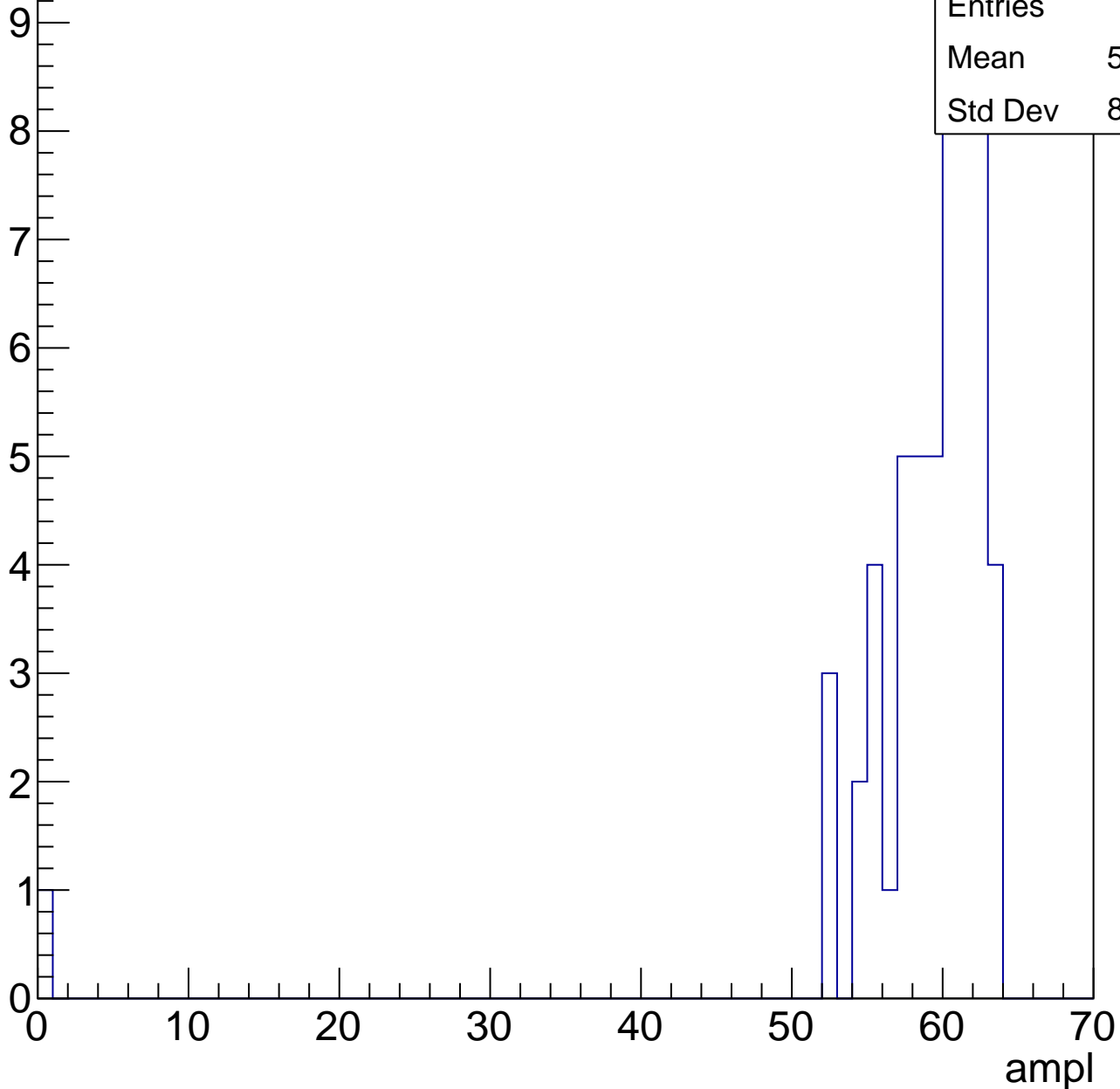


# B1L102S, U21-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	57.96
Std Dev	8.423

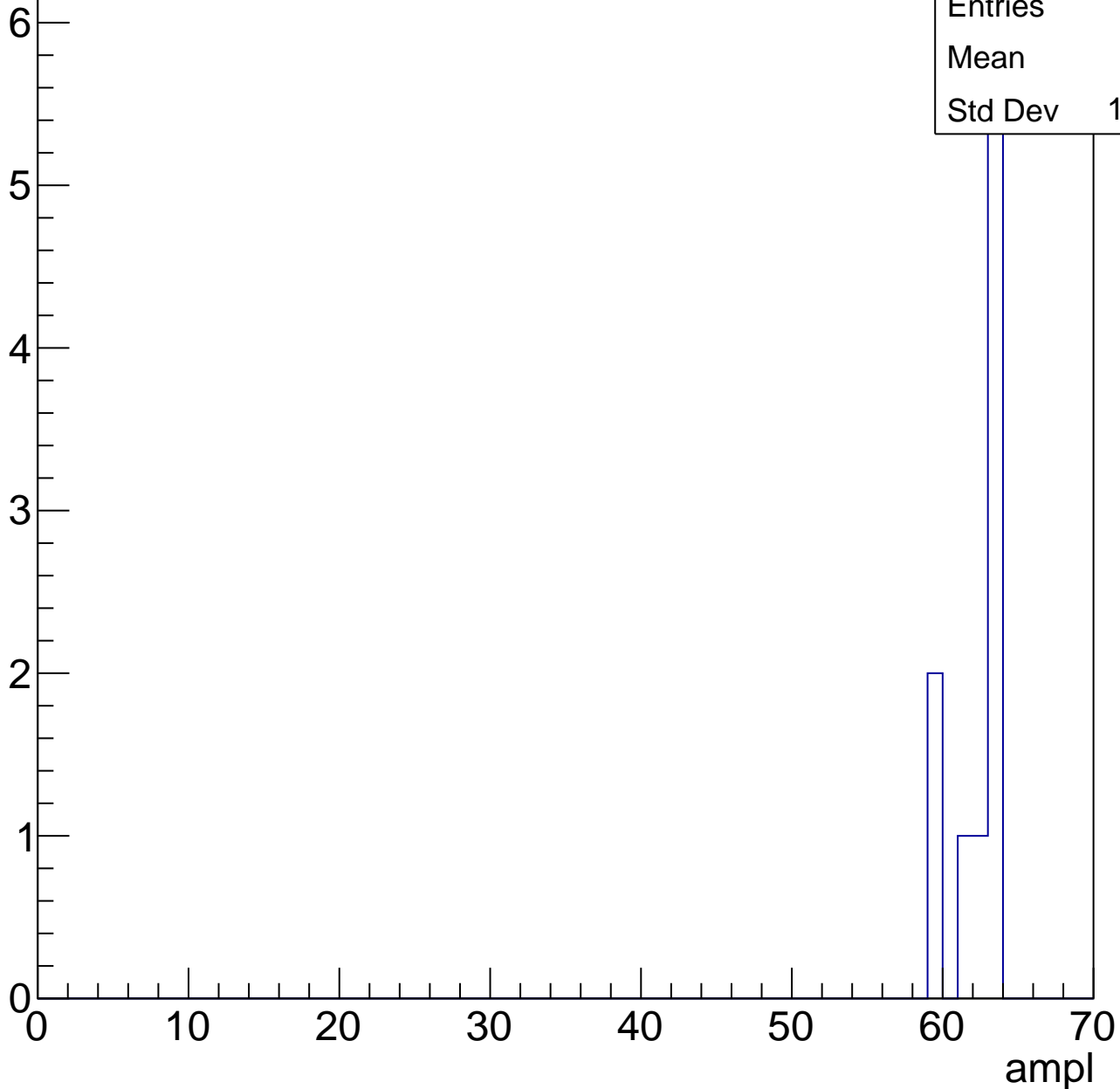


# B1L102S, U21-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	10
Mean	61.9
Std Dev	1.578





# B1L102S, U21-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

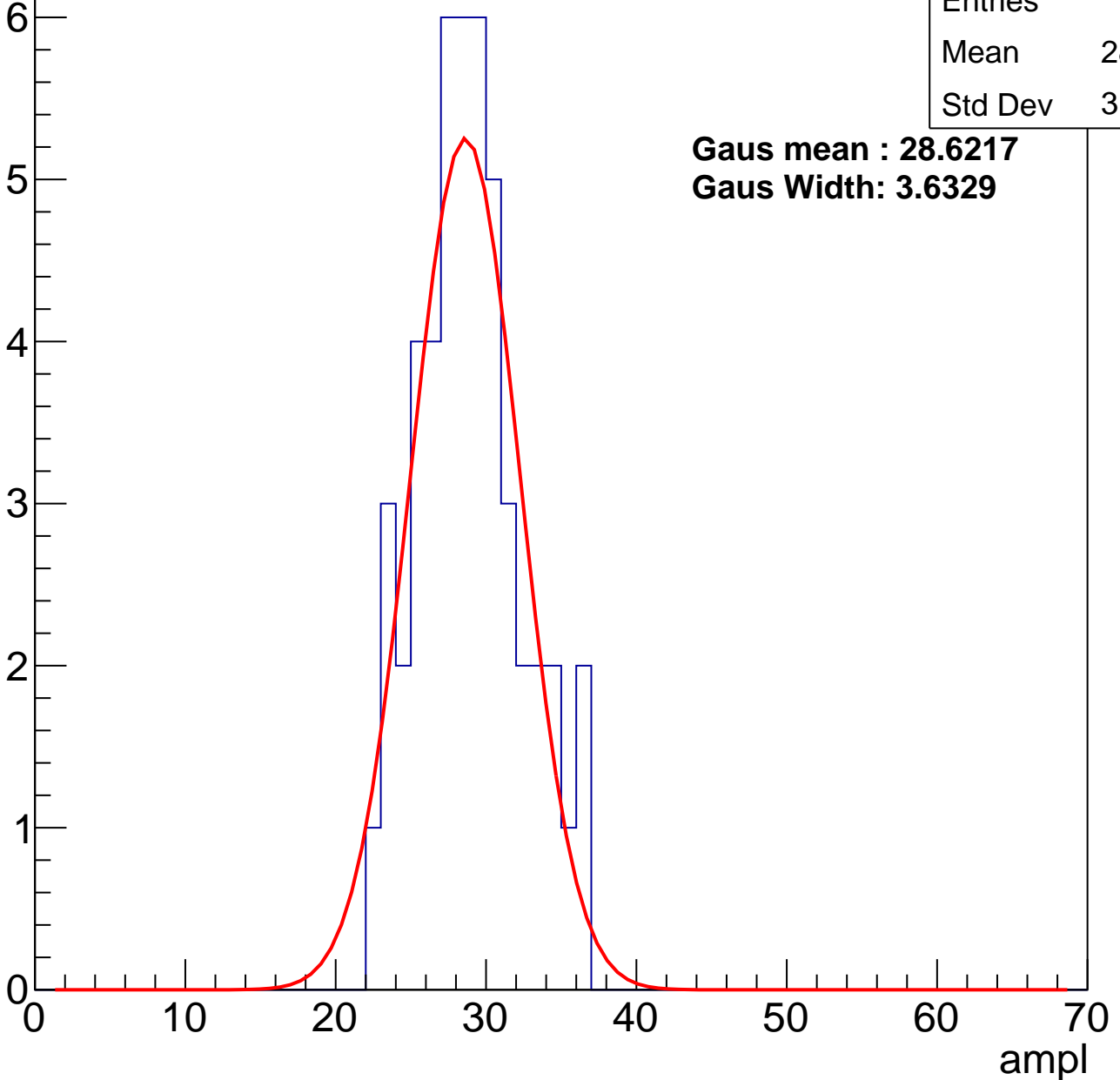
# B1L102S, U21-ch101, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	28.47
Std Dev	3.423

**Gaus mean : 28.6217**  
**Gaus Width: 3.6329**



# B1L102S, U21-ch101, adc1

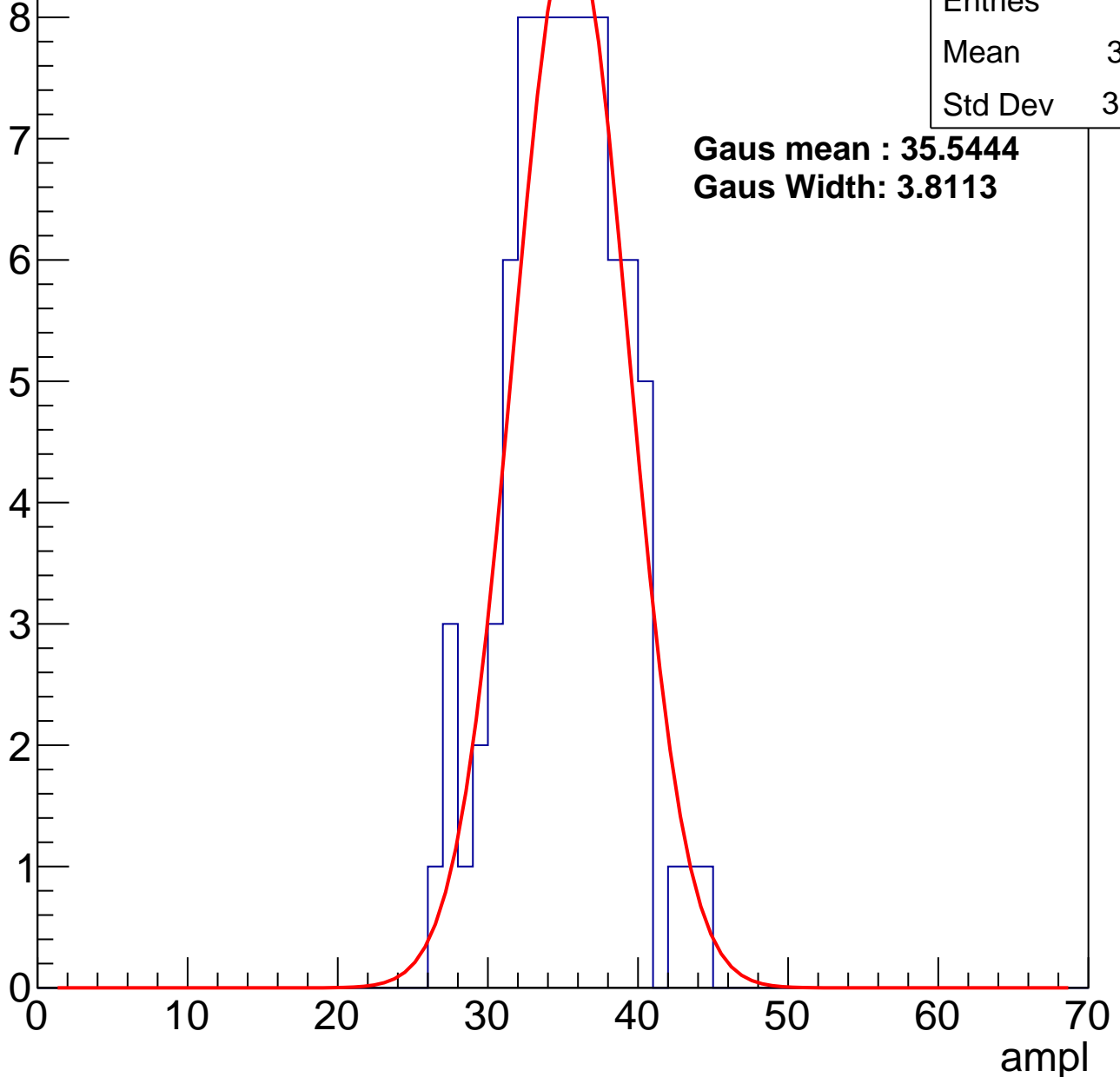
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	34.71
Std Dev	3.747

**Gaus mean : 35.5444**

**Gaus Width: 3.8113**



# B1L102S, U21-ch101, adc2

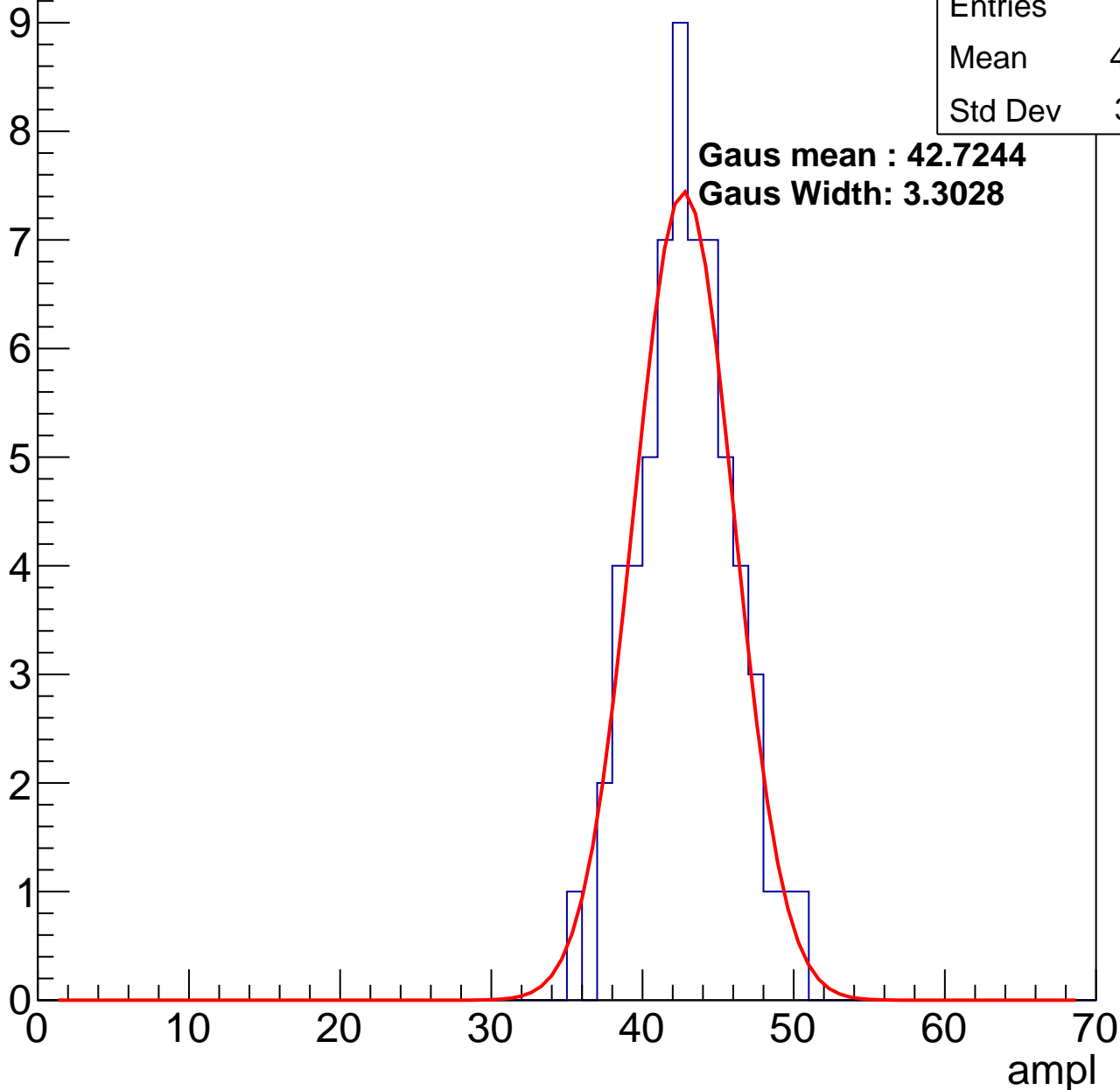
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	42.43
Std Dev	3.091

**Gaus mean : 42.7244**

**Gaus Width: 3.3028**

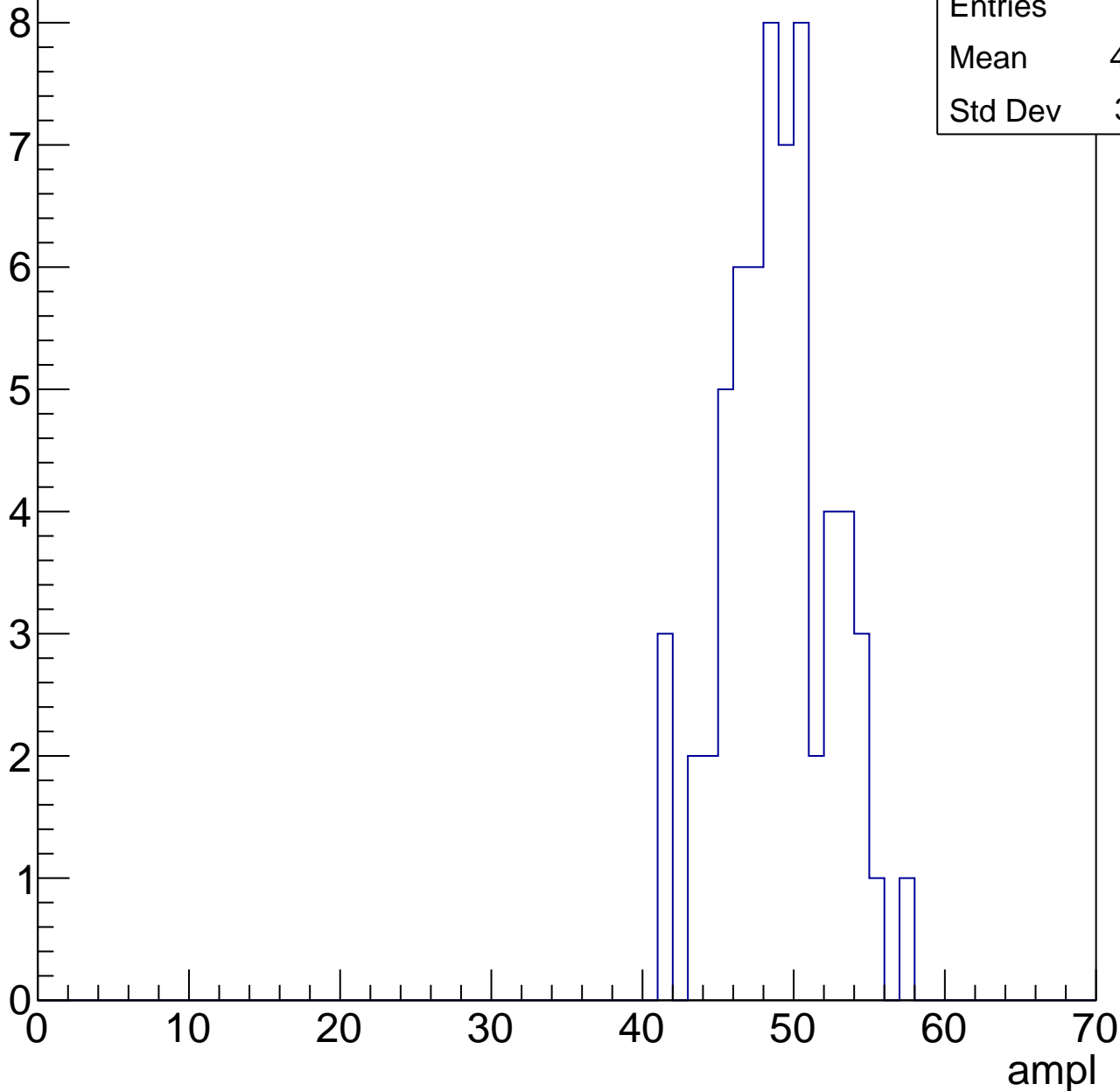


# B1L102S, U21-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	48.44
Std Dev	3.481

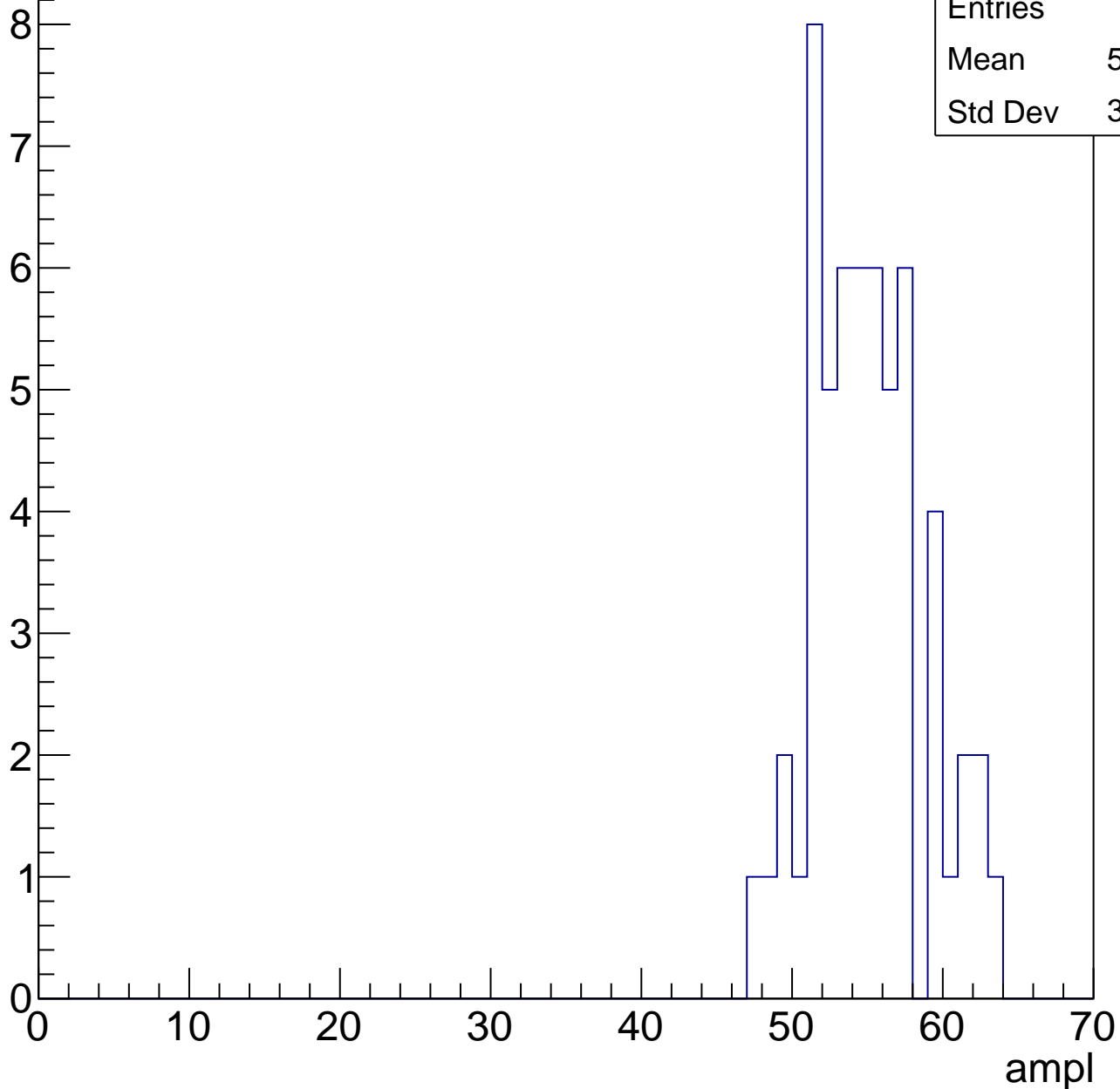


# B1L102S, U21-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	54.56
Std Dev	3.637



# B1L102S, U21-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	58
Mean	58.14
Std Dev	8.102

Entry

10

8

6

4

2

0

0

10

20

30

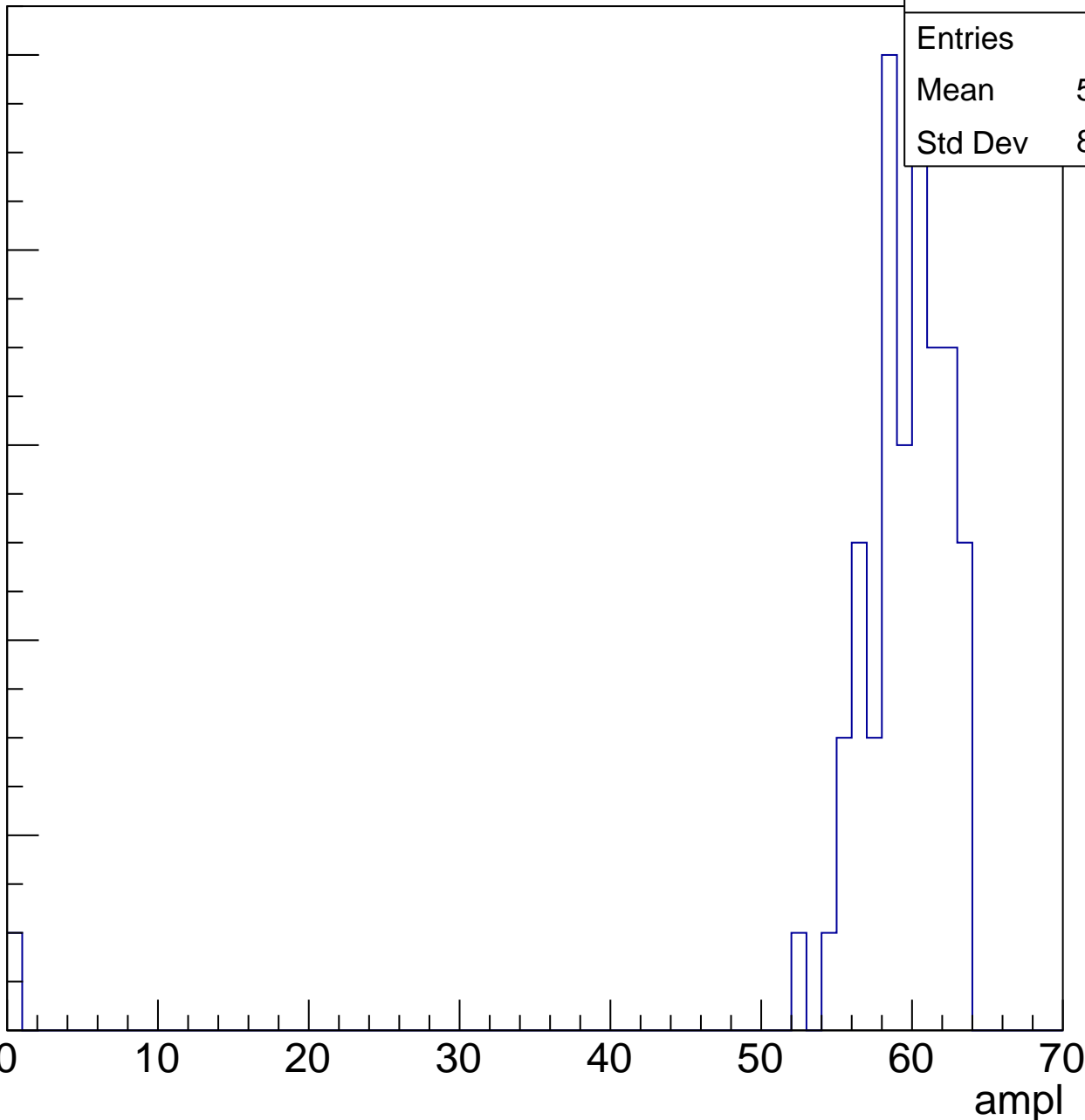
40

50

60

70

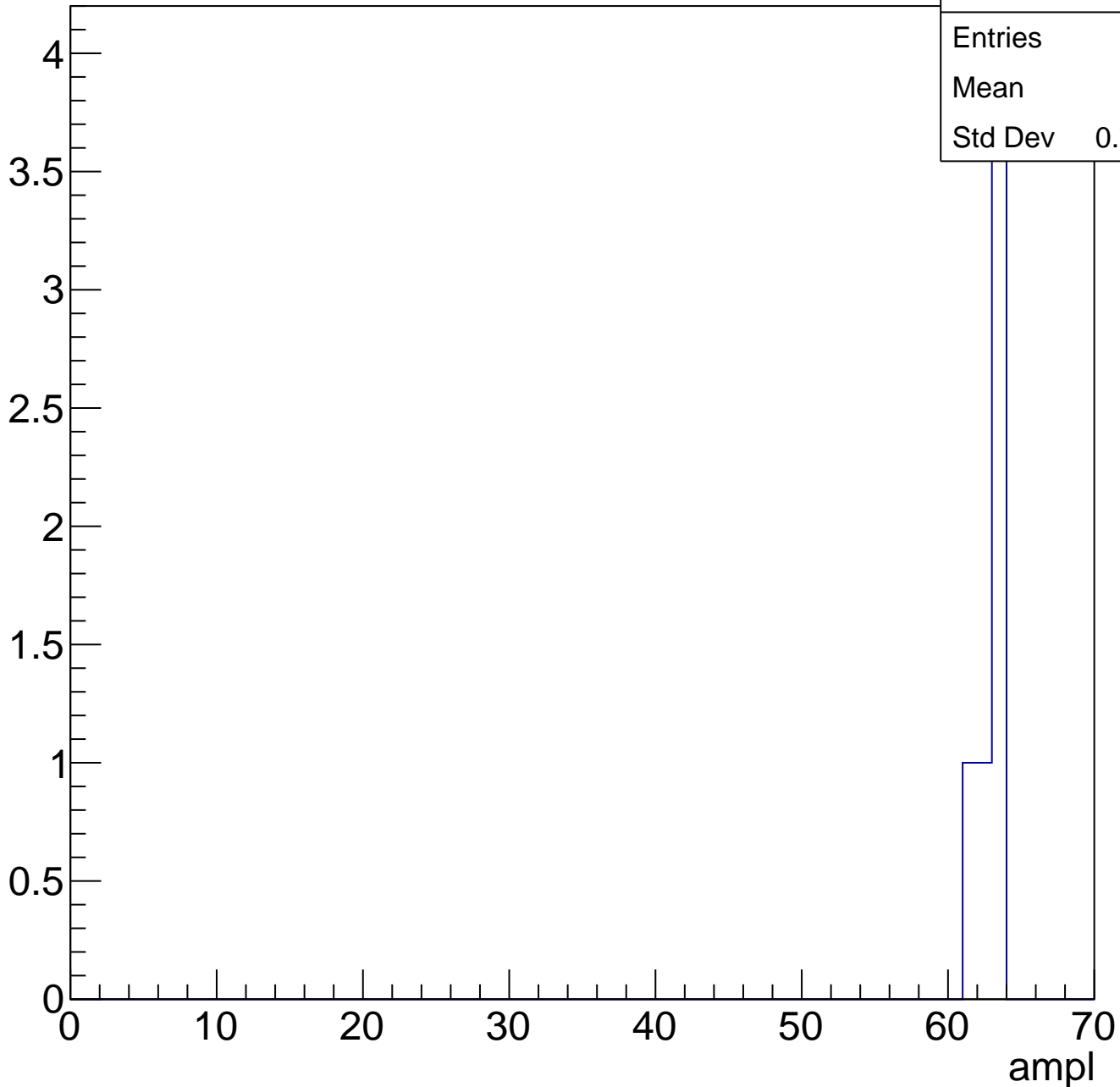
ampl



# B1L102S, U21-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U21-ch102, adc0

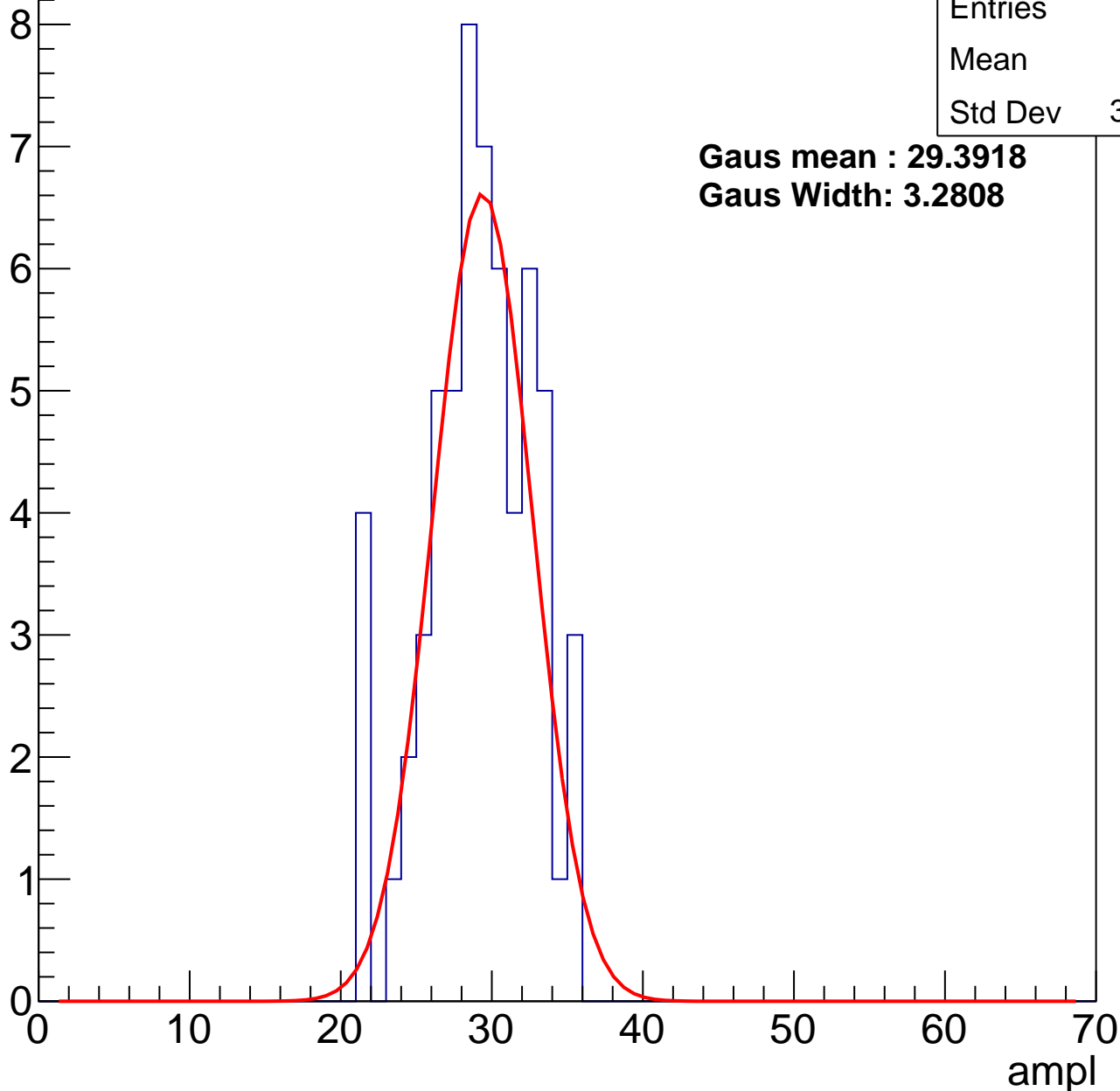
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	28.7
Std Dev	3.528

**Gaus mean : 29.3918**

**Gaus Width: 3.2808**



# B1L102S, U21-ch102, adc1

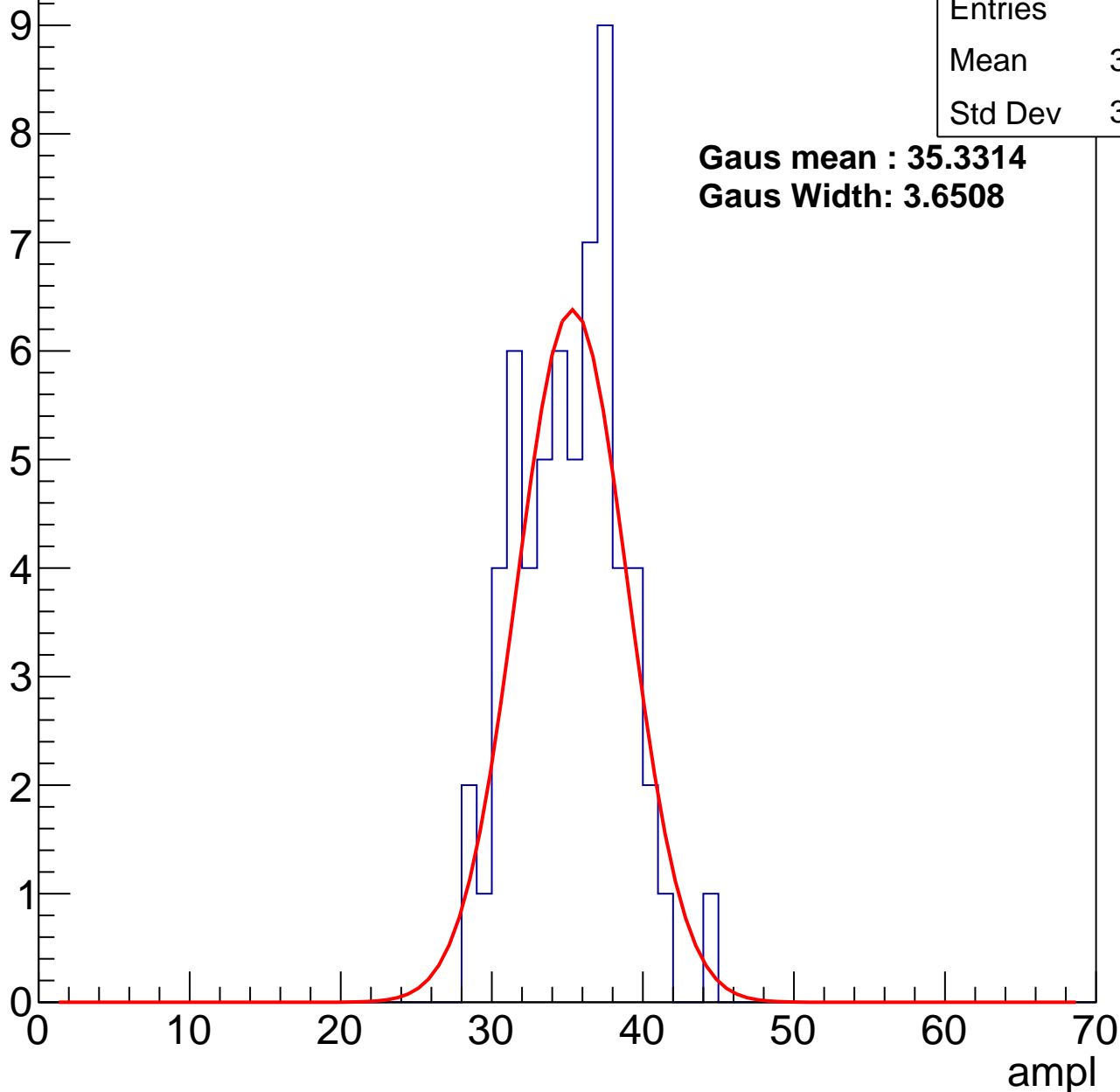
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	34.77
Std Dev	3.385

**Gaus mean : 35.3314**

**Gaus Width: 3.6508**



# B1L102S, U21-ch102, adc2

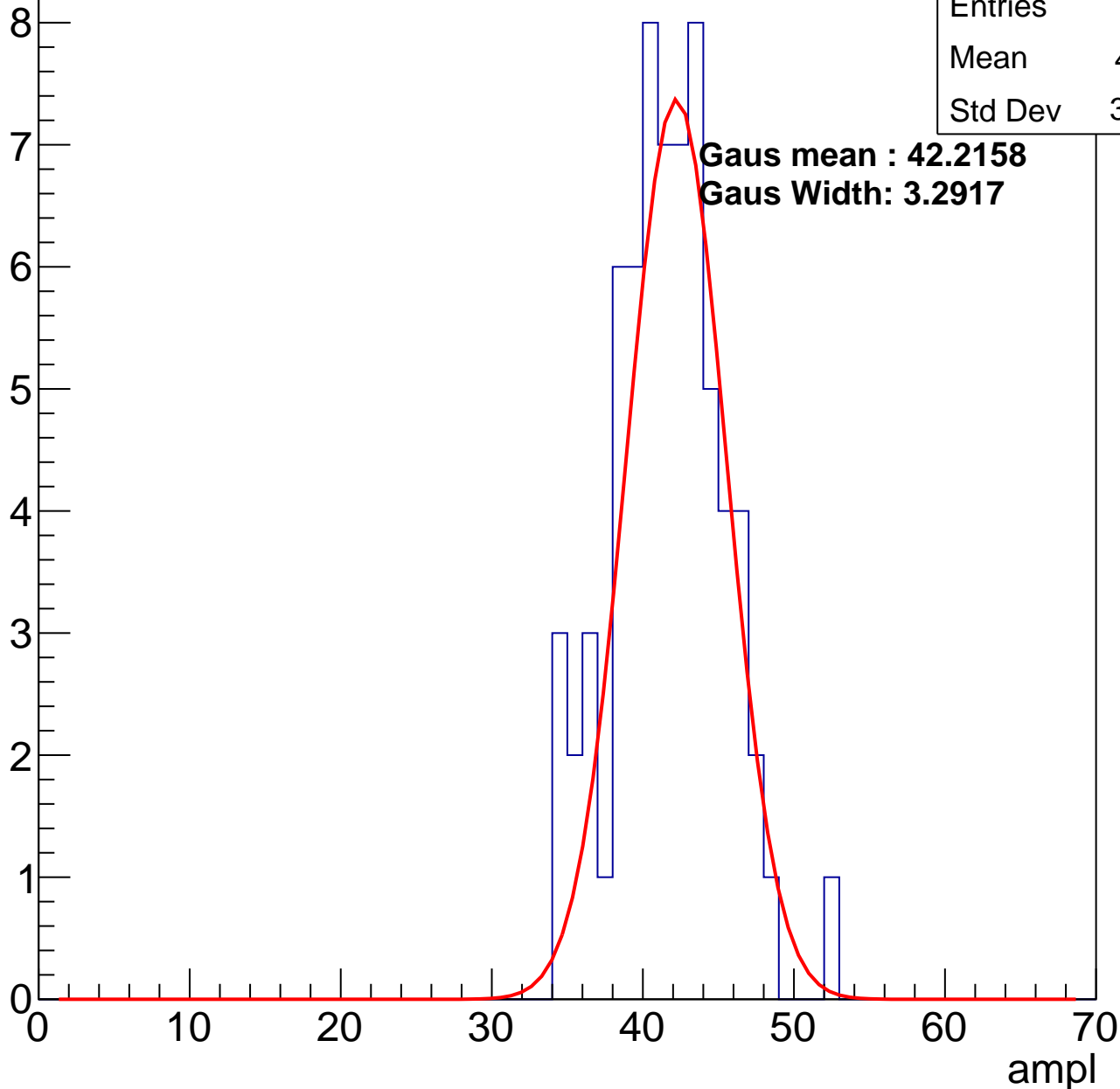
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	41.21
Std Dev	3.604

**Gaus mean : 42.2158**

**Gaus Width: 3.2917**

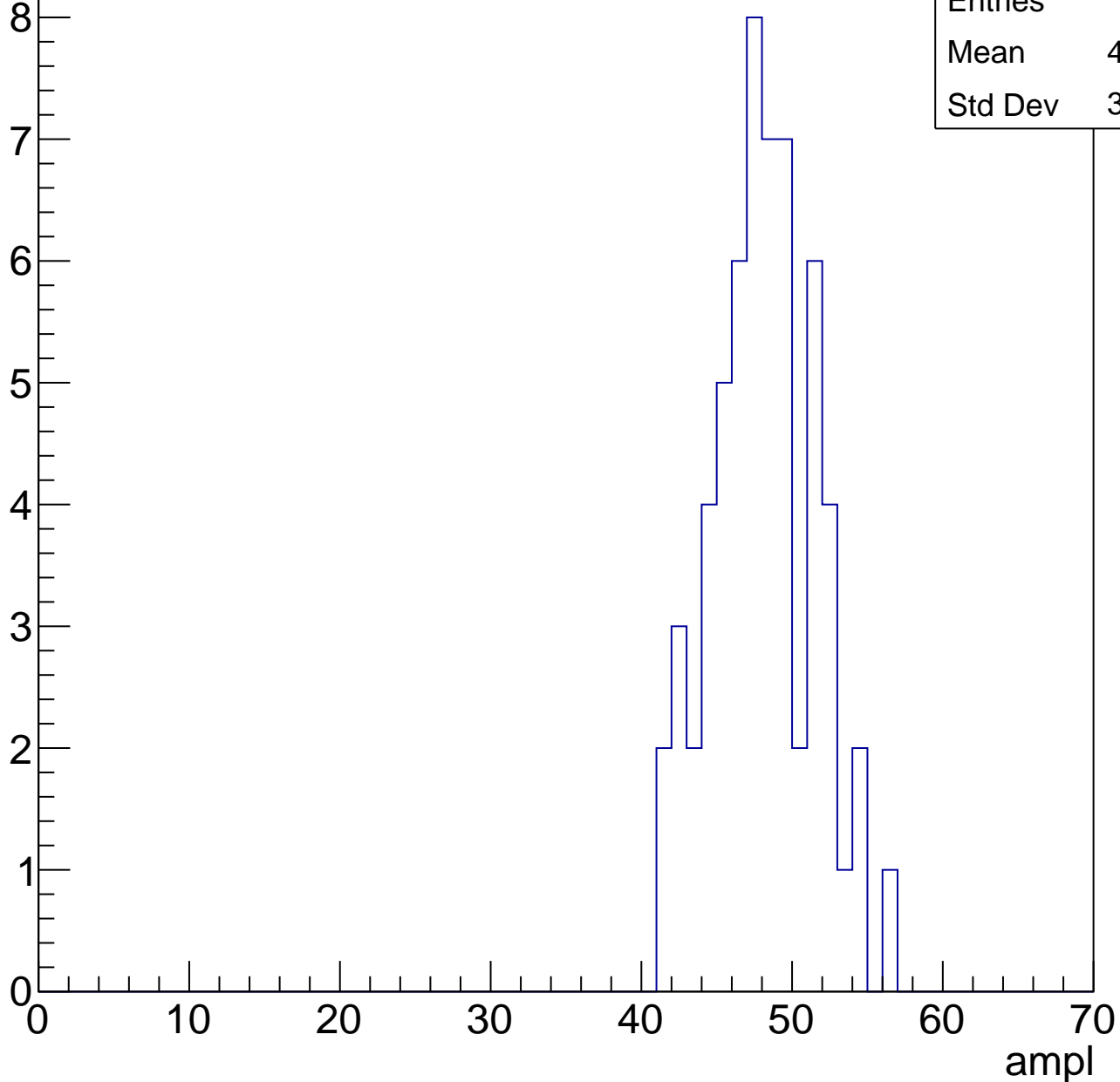


# B1L102S, U21-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	47.62
Std Dev	3.372

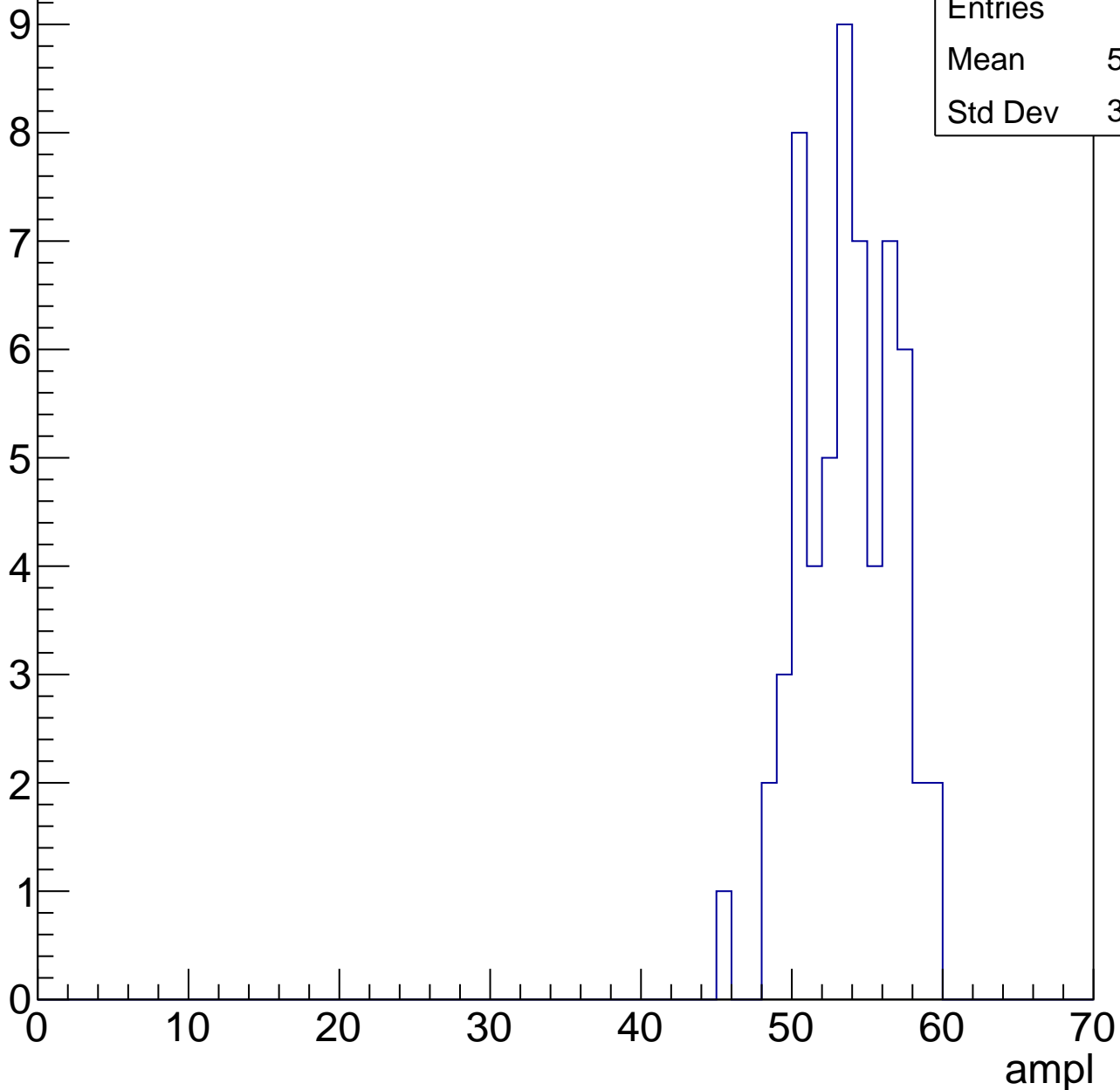


# B1L102S, U21-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	53.25
Std Dev	3.042

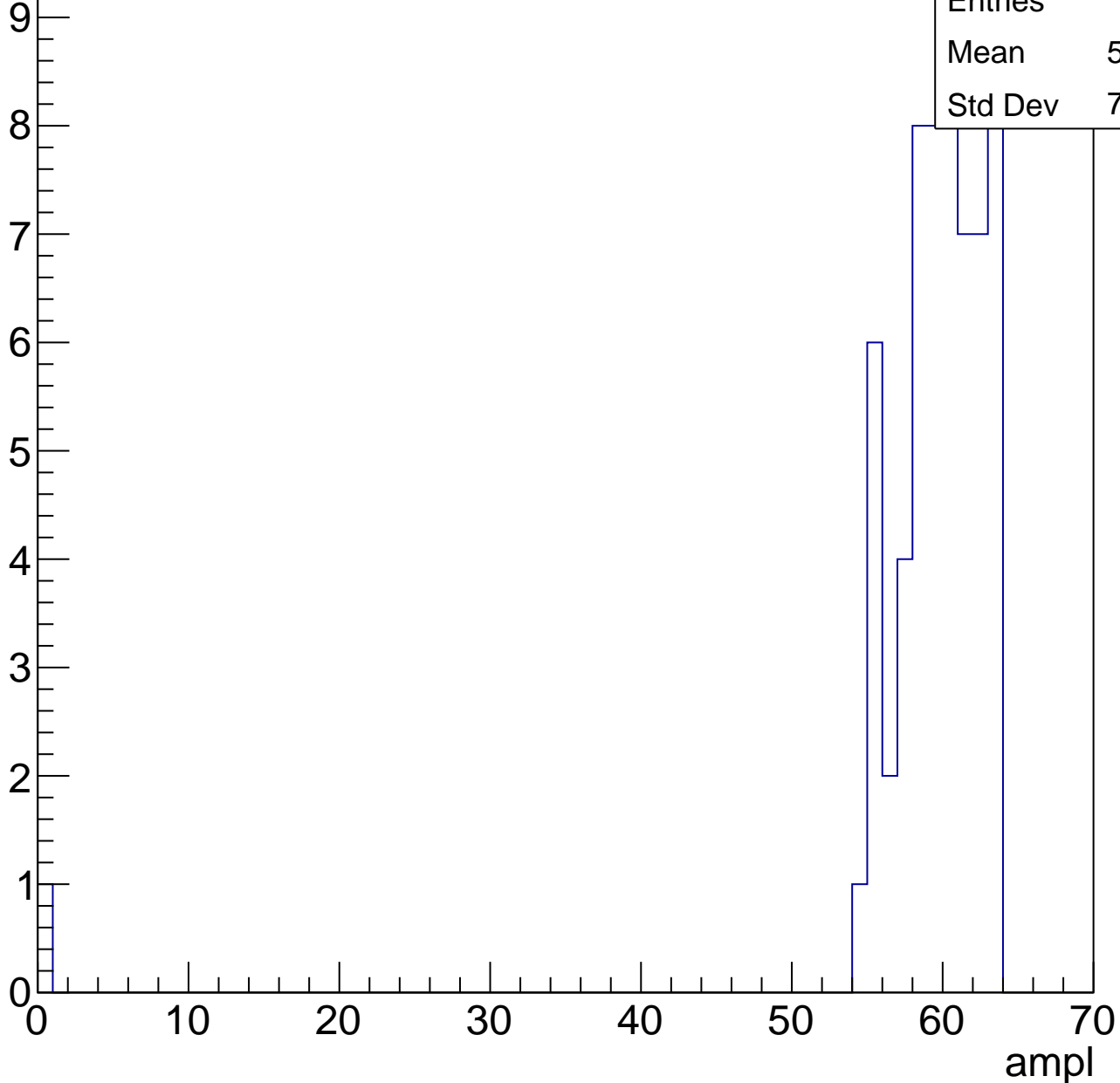


# B1L102S, U21-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

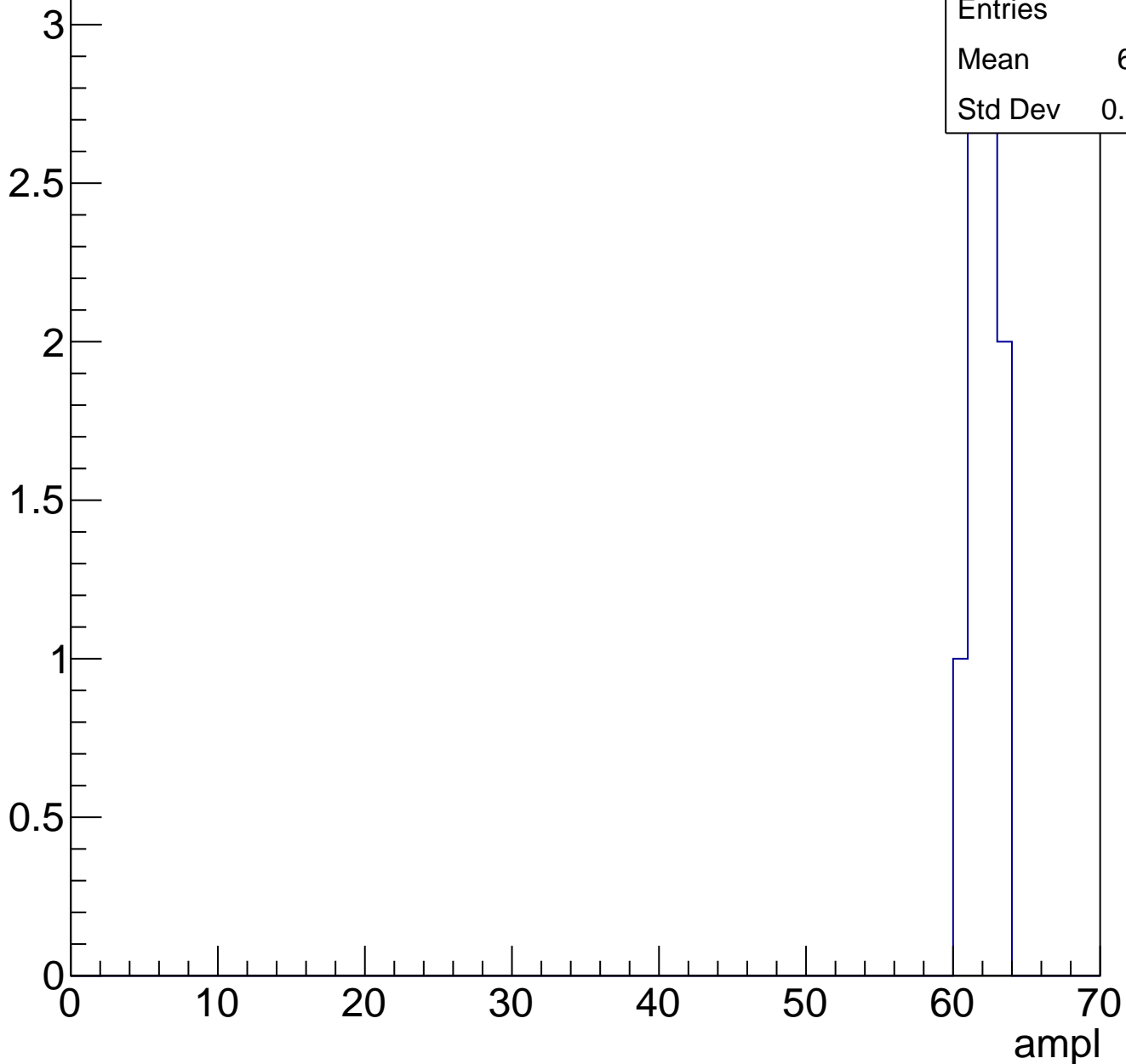
Entries	61
Mean	58.44
Std Dev	7.948



# B1L102S, U21-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

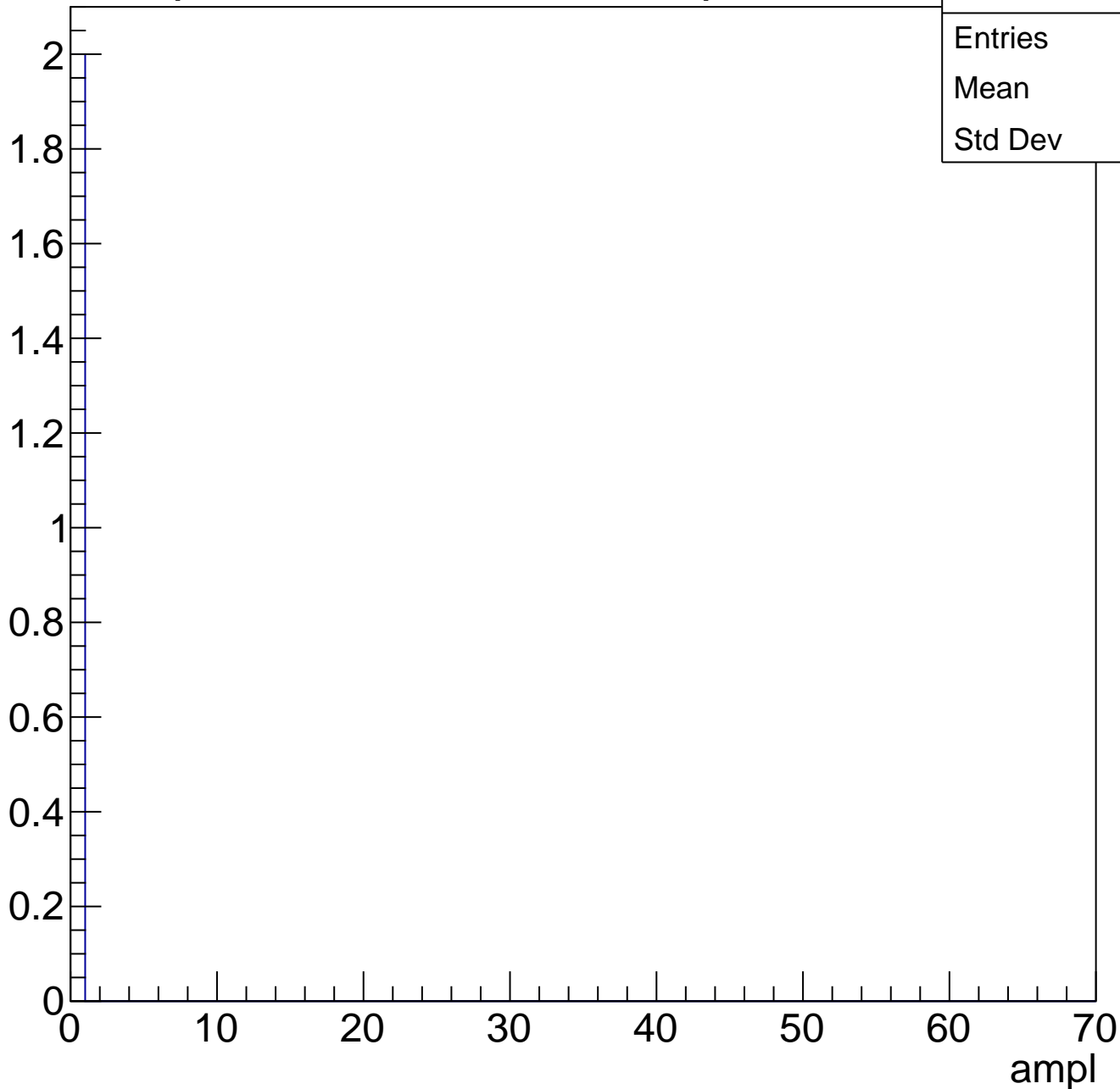




# B1L102S, U21-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch103, adc0

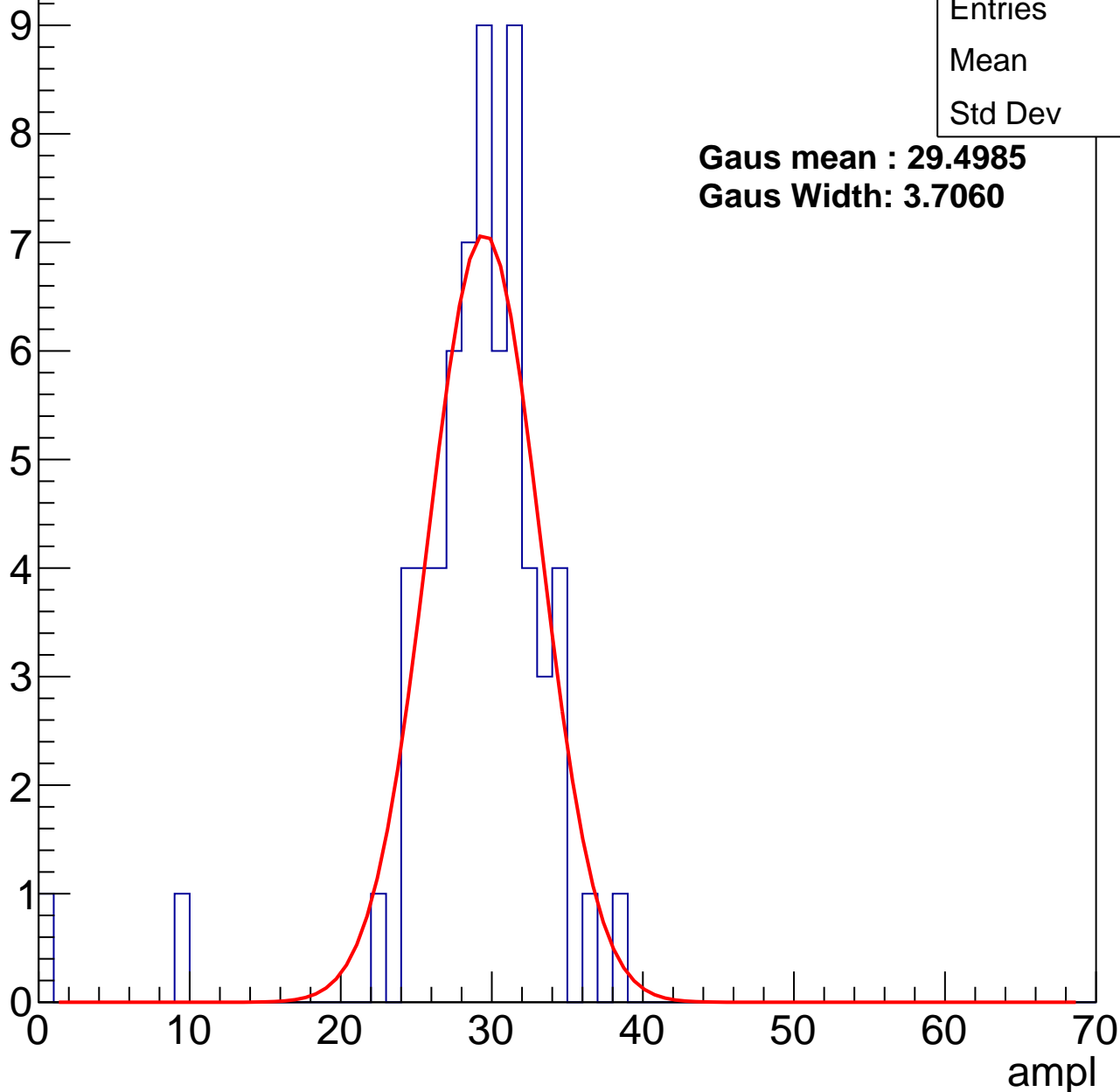
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	28.4
Std Dev	5.34

**Gaus mean : 29.4985**

**Gaus Width: 3.7060**



# B1L102S, U21-ch103, adc1

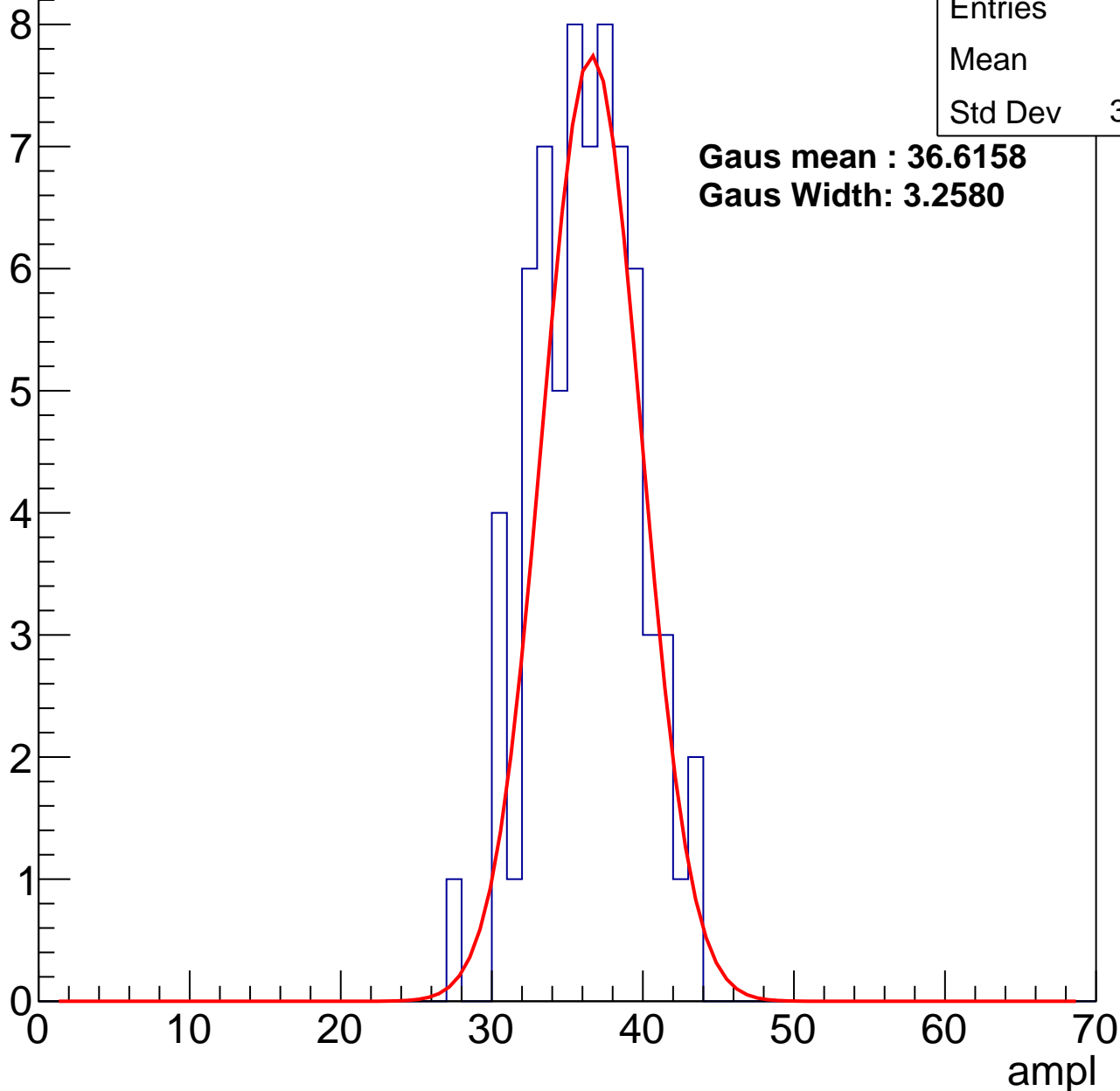
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	35.8
Std Dev	3.365

**Gaus mean : 36.6158**

**Gaus Width: 3.2580**



# B1L102S, U21-ch103, adc2

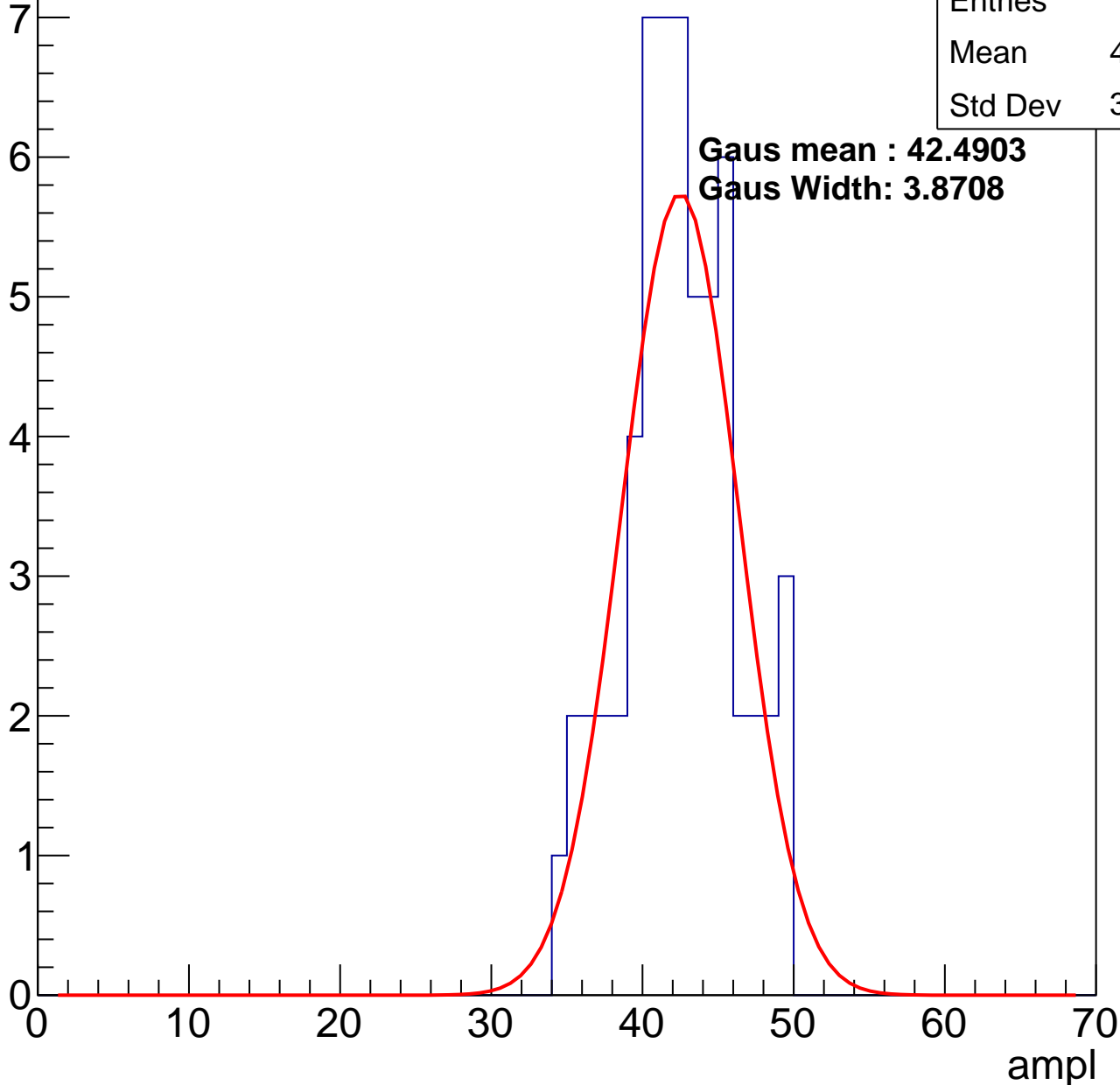
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	41.98
Std Dev	3.606

**Gaus mean : 42.4903**

**Gaus Width: 3.8708**

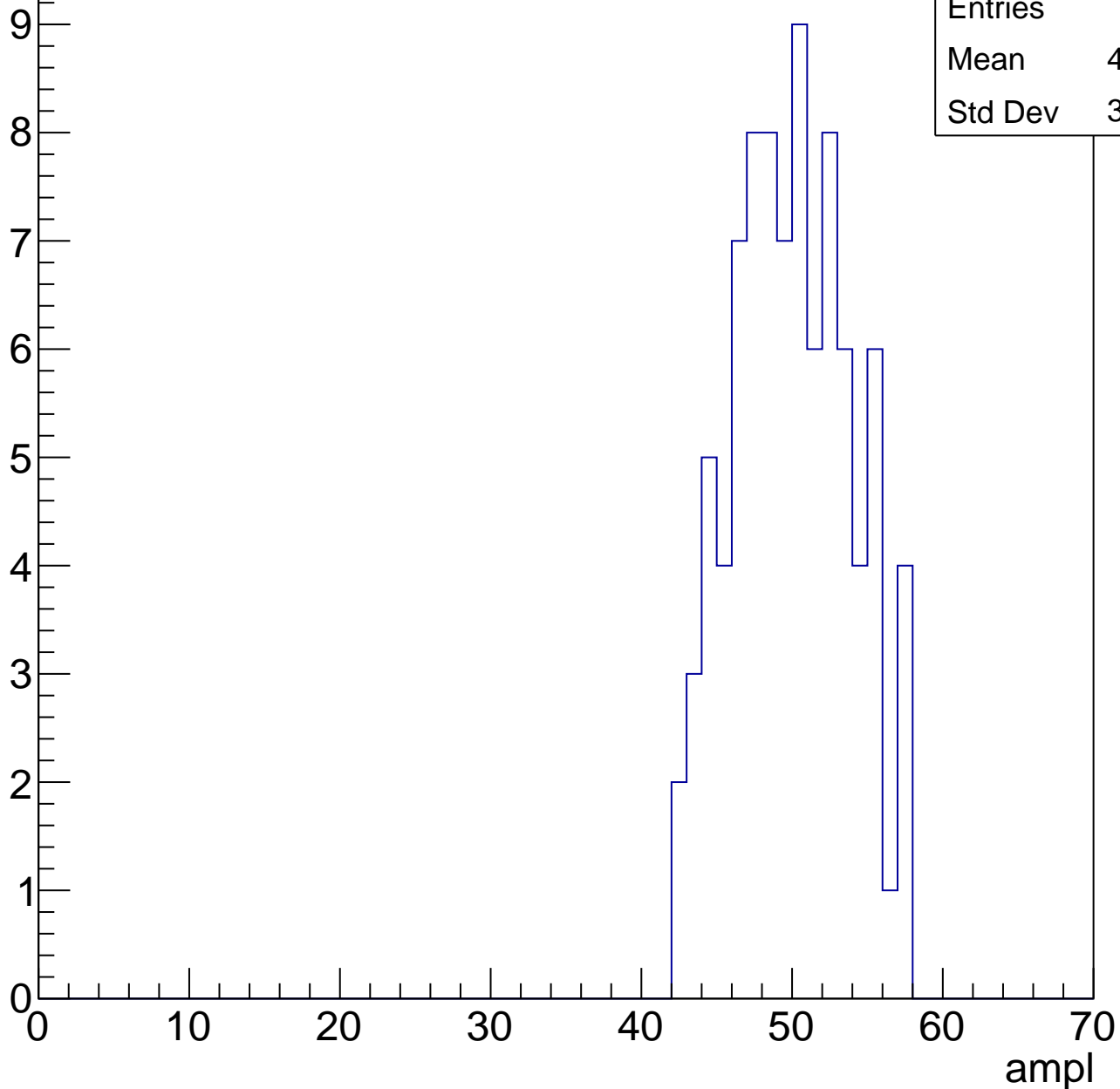


# B1L102S, U21-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	88
Mean	49.52
Std Dev	3.838

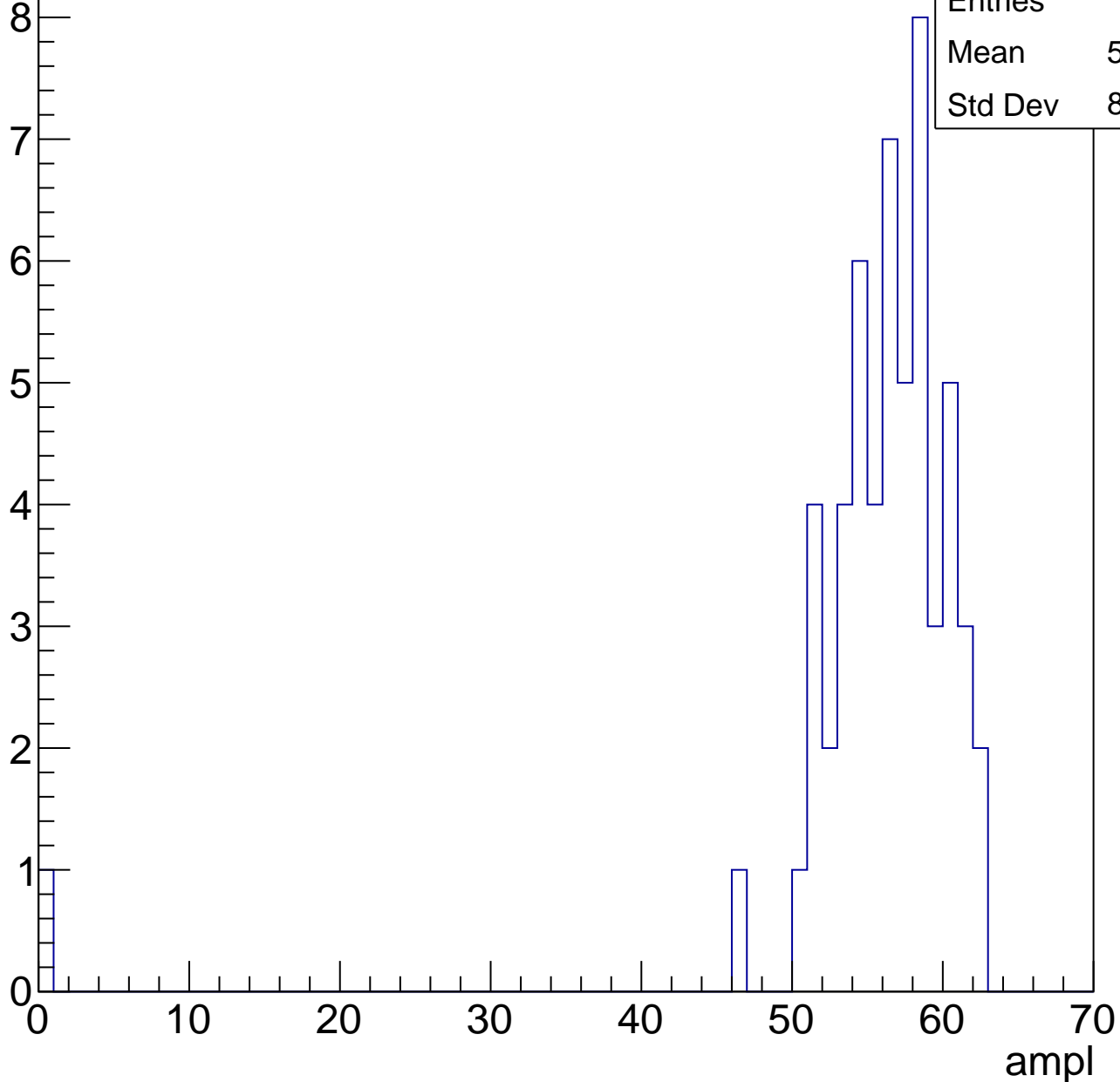


# B1L102S, U21-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	55.09
Std Dev	8.142

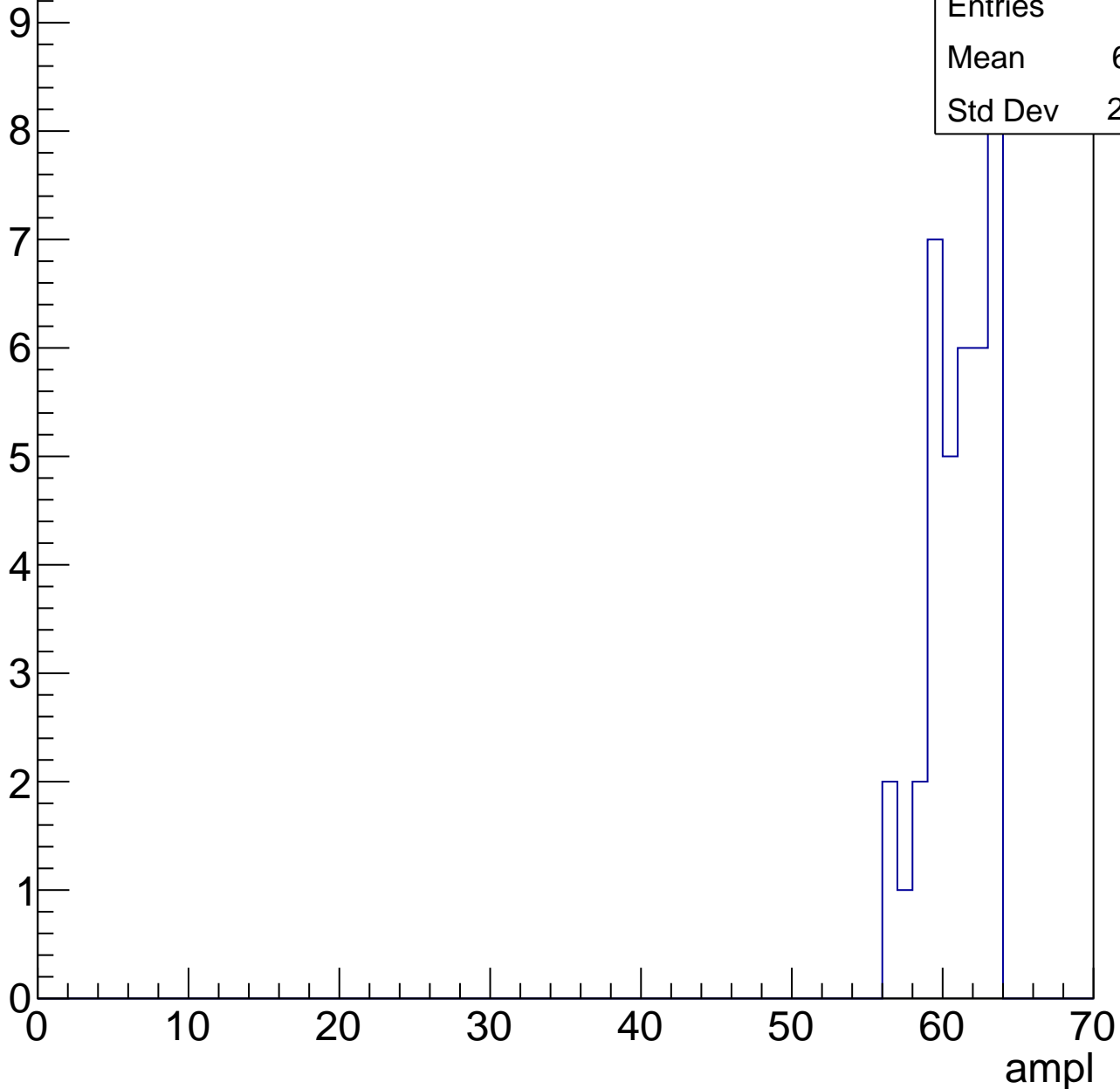


# B1L102S, U21-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	38
Mean	60.61
Std Dev	2.007



# B1L102S, U21-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U21-ch104, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	77
Mean	27.92
Std Dev	5.659

**Gaus mean : 29.9146**

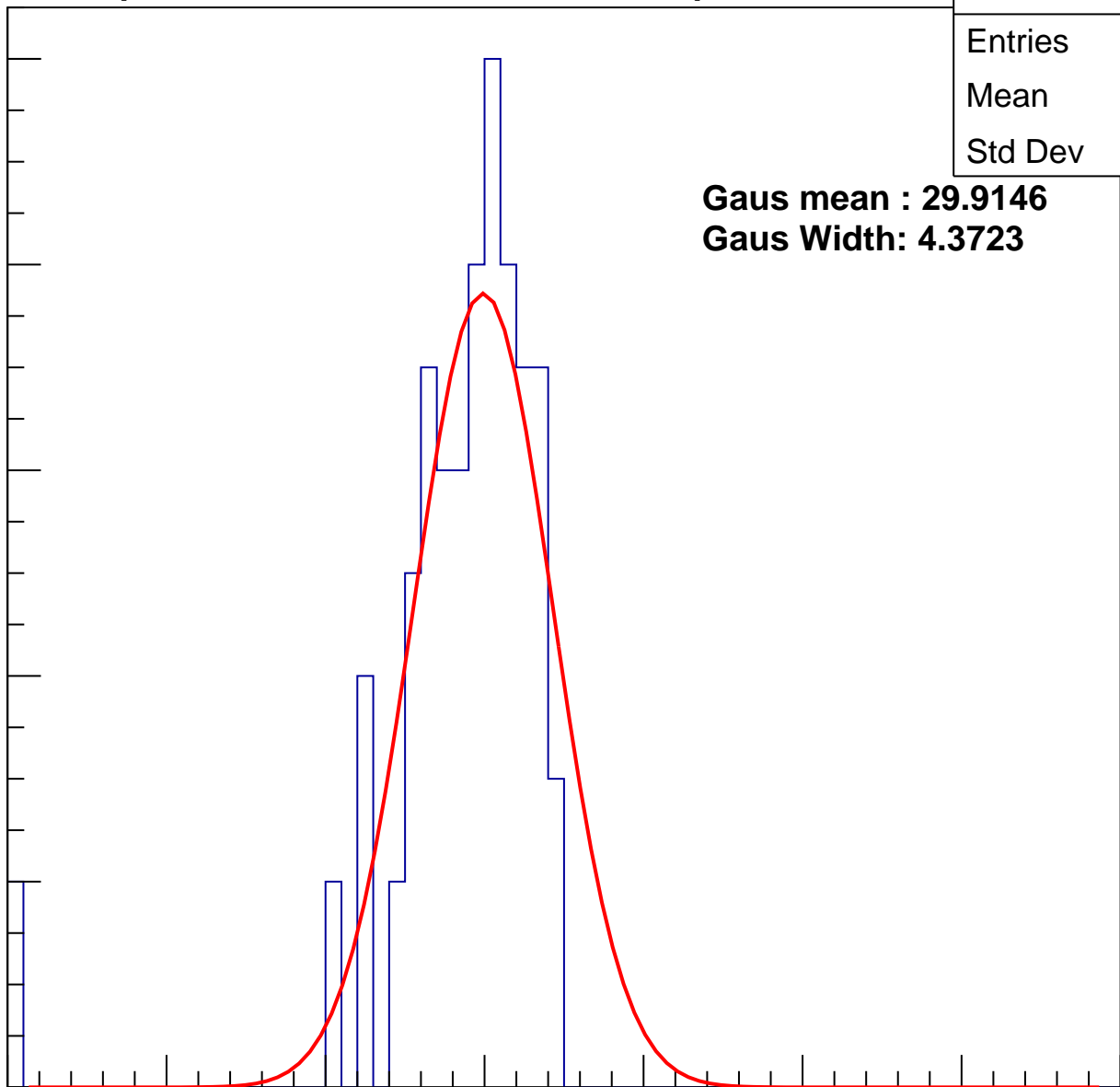
**Gaus Width: 4.3723**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U21-ch104, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	70
Mean	37.07
Std Dev	3.217

**Gaus mean : 37.5041**

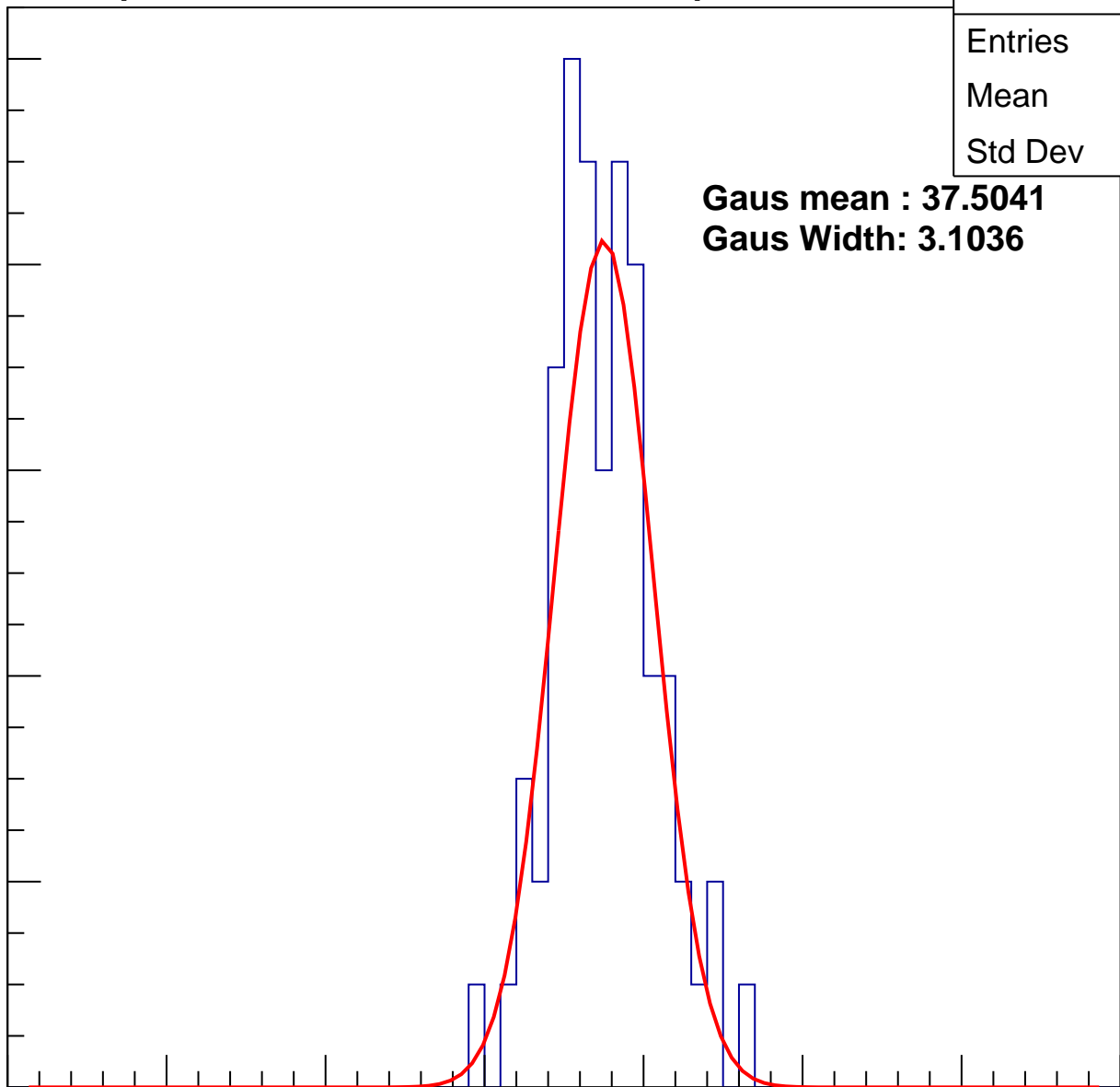
**Gaus Width: 3.1036**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L102S, U21-ch104, adc2

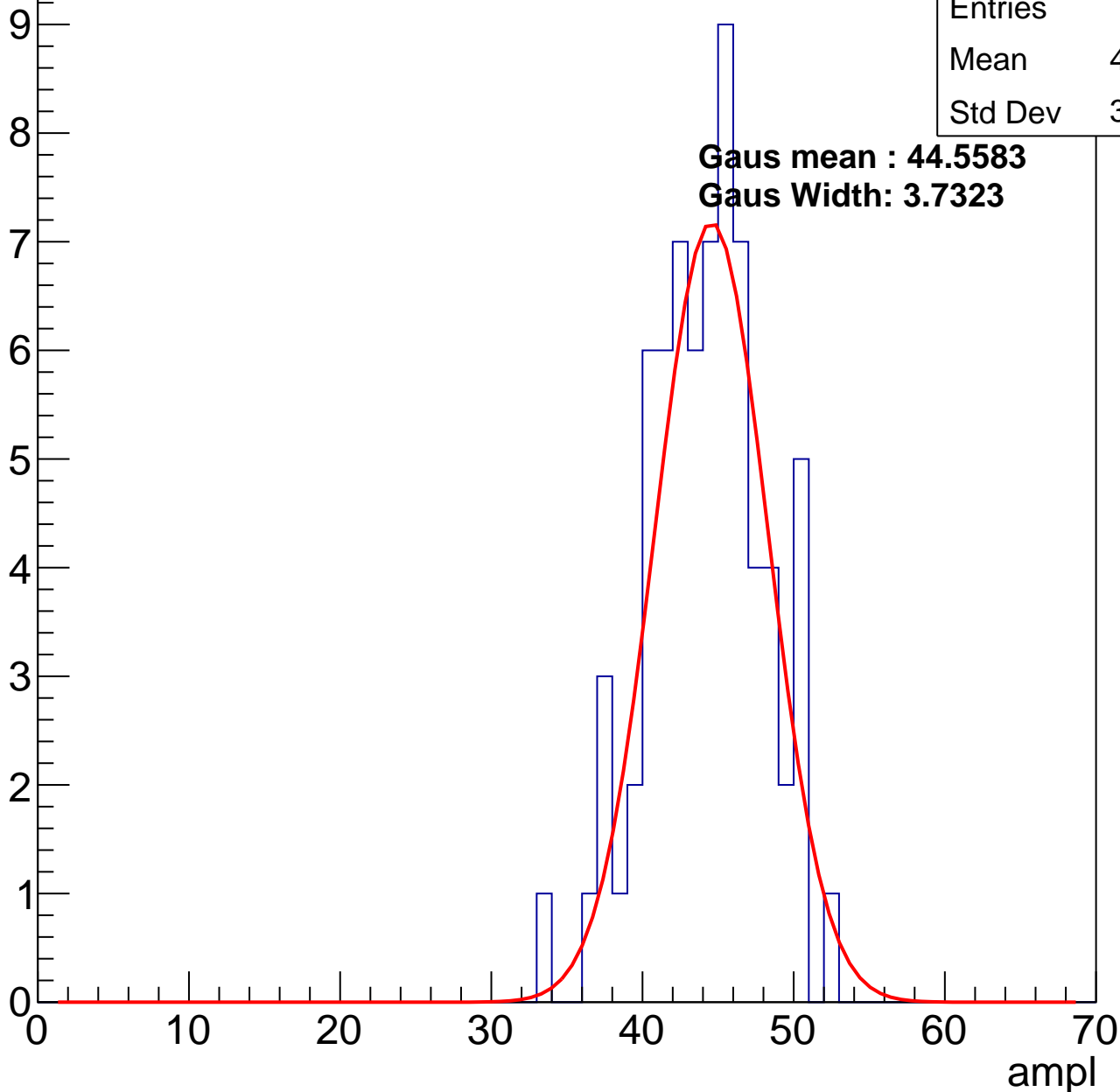
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	43.74
Std Dev	3.779

**Gaus mean : 44.5583**

**Gaus Width: 3.7323**

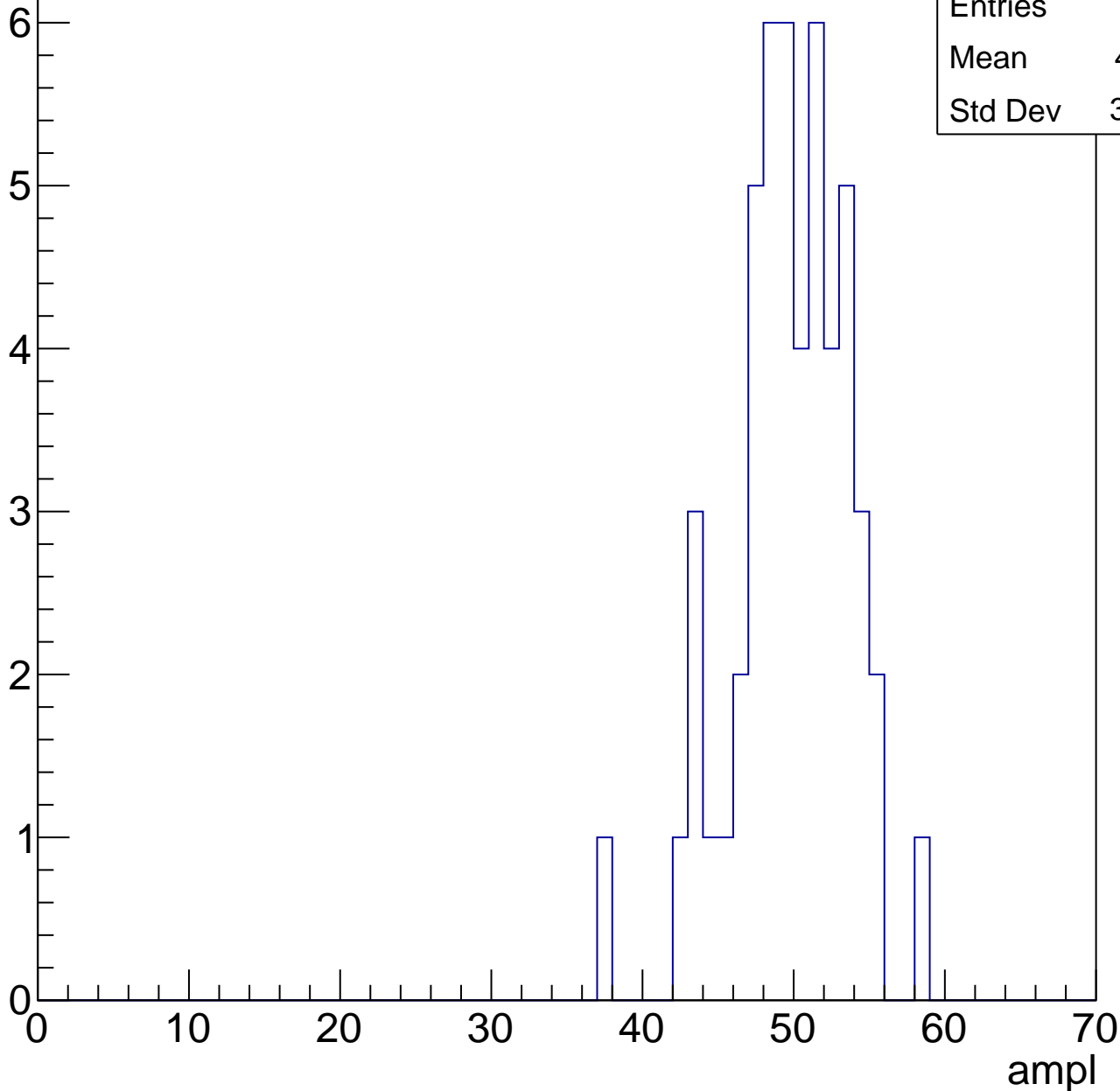


# B1L102S, U21-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	49.31
Std Dev	3.842

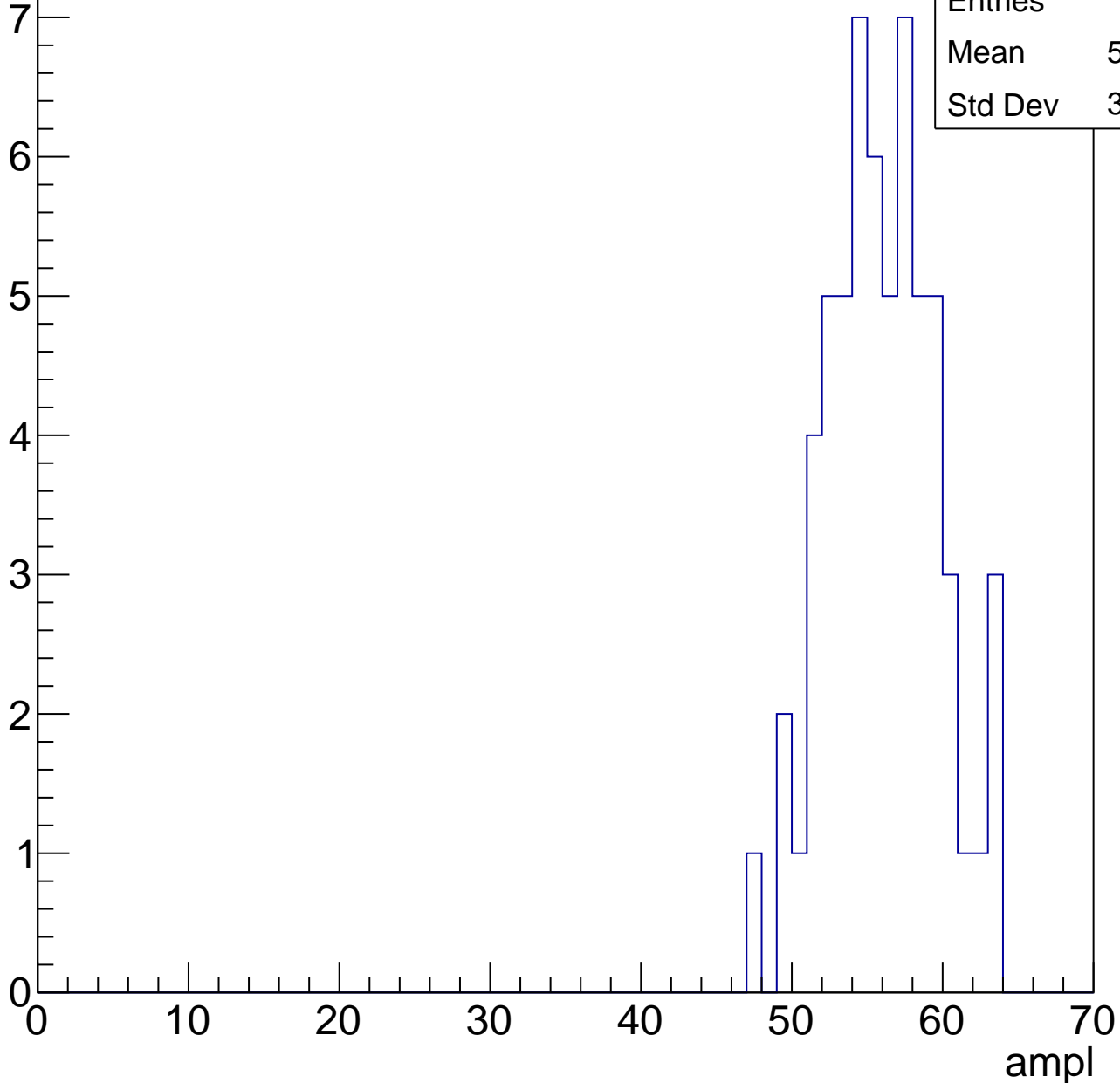


# B1L102S, U21-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	55.54
Std Dev	3.597

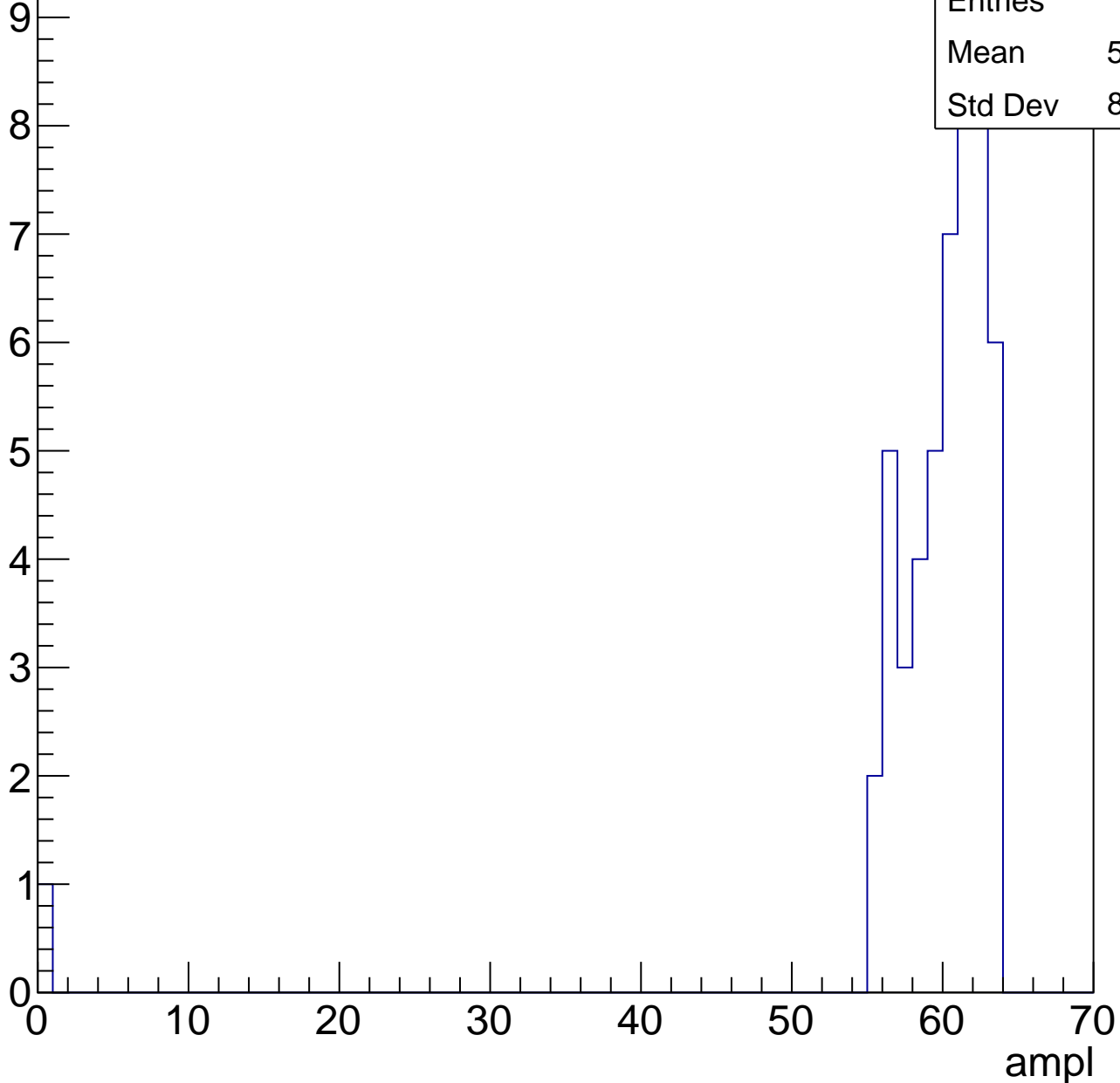


# B1L102S, U21-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	58.64
Std Dev	8.699



# B1L102S, U21-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

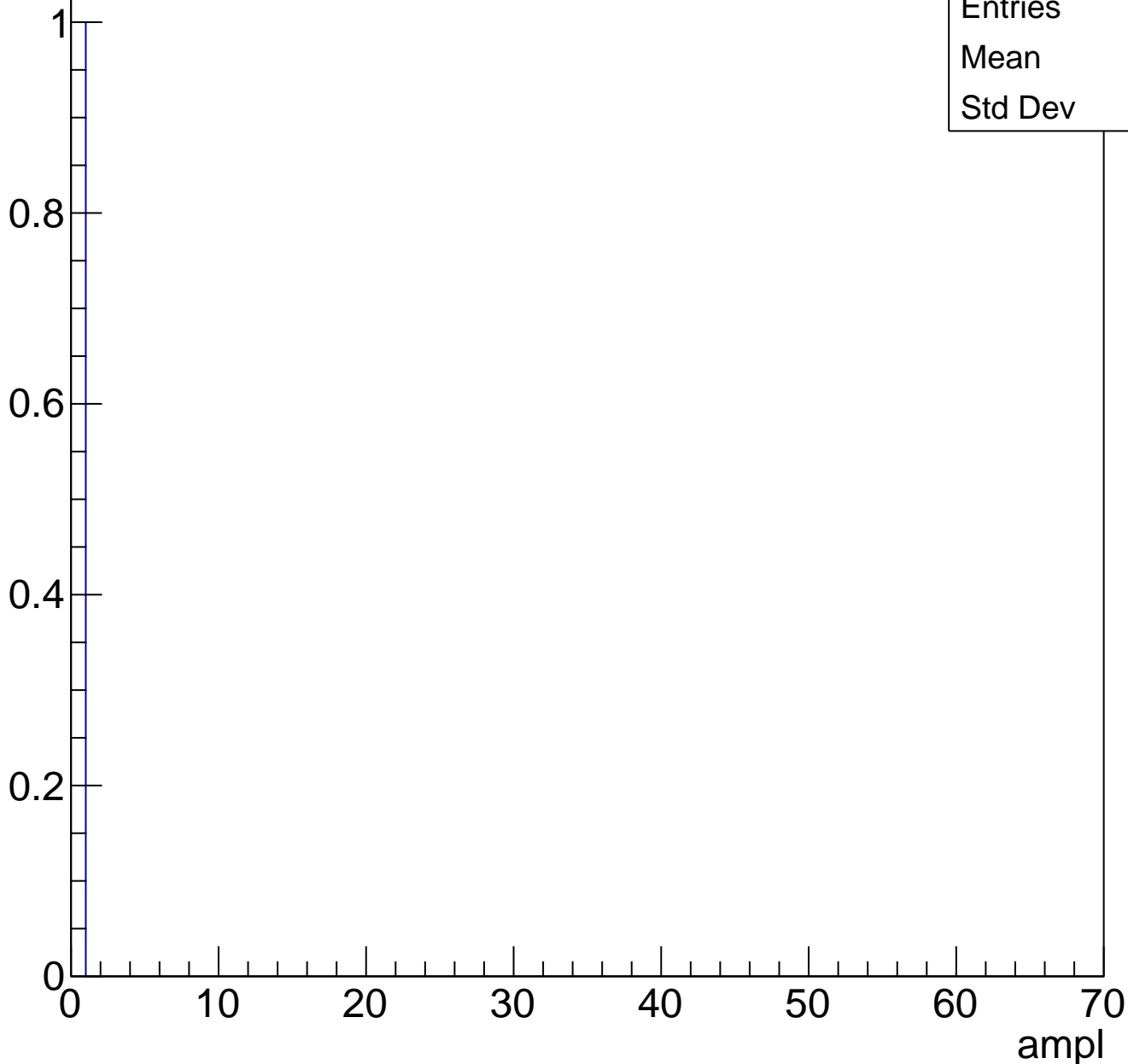




# B1L102S, U21-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch105, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	85
Mean	29.44
Std Dev	4.922

**Gaus mean : 30.4600**

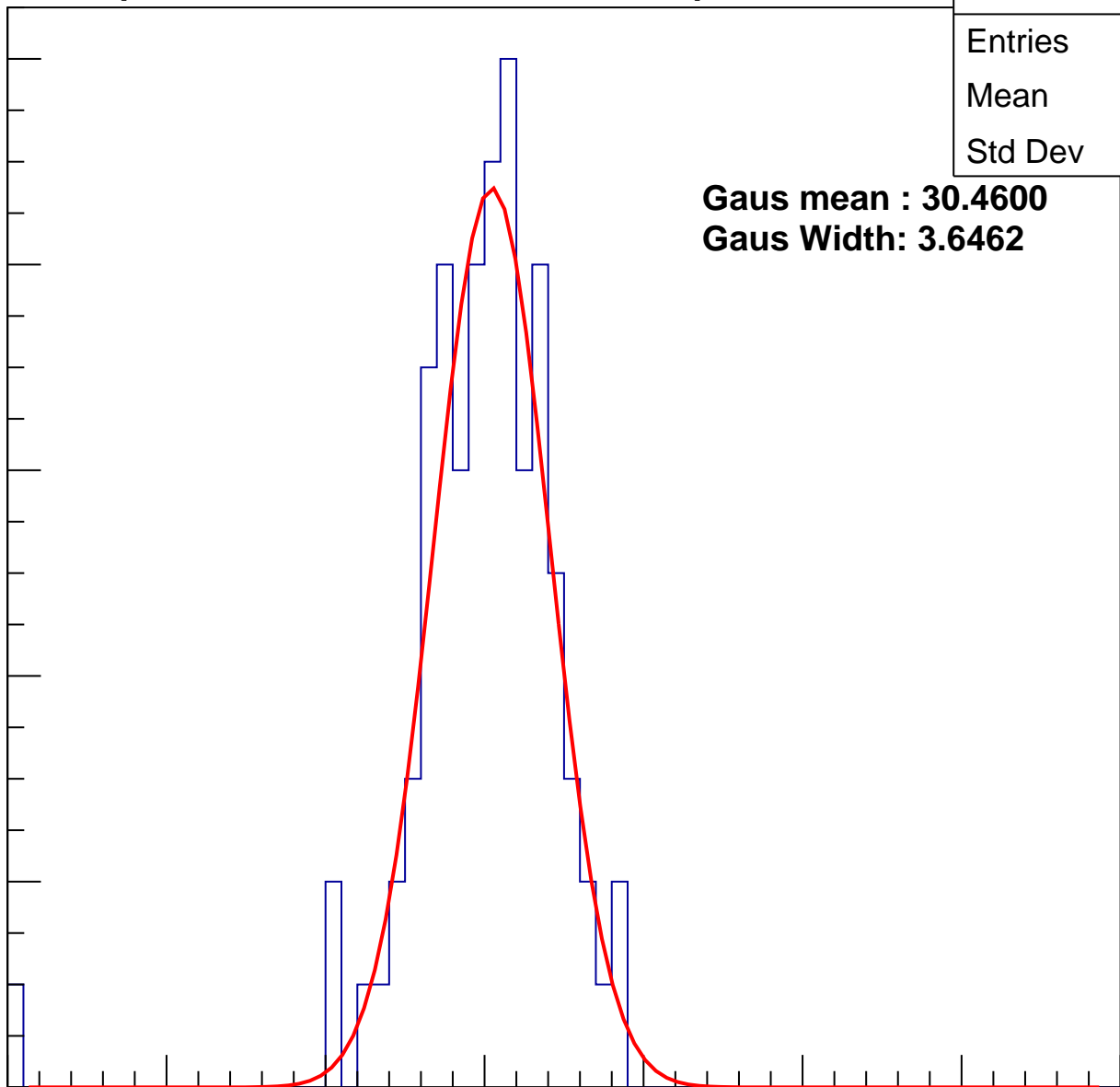
**Gaus Width: 3.6462**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U21-ch105, adc1

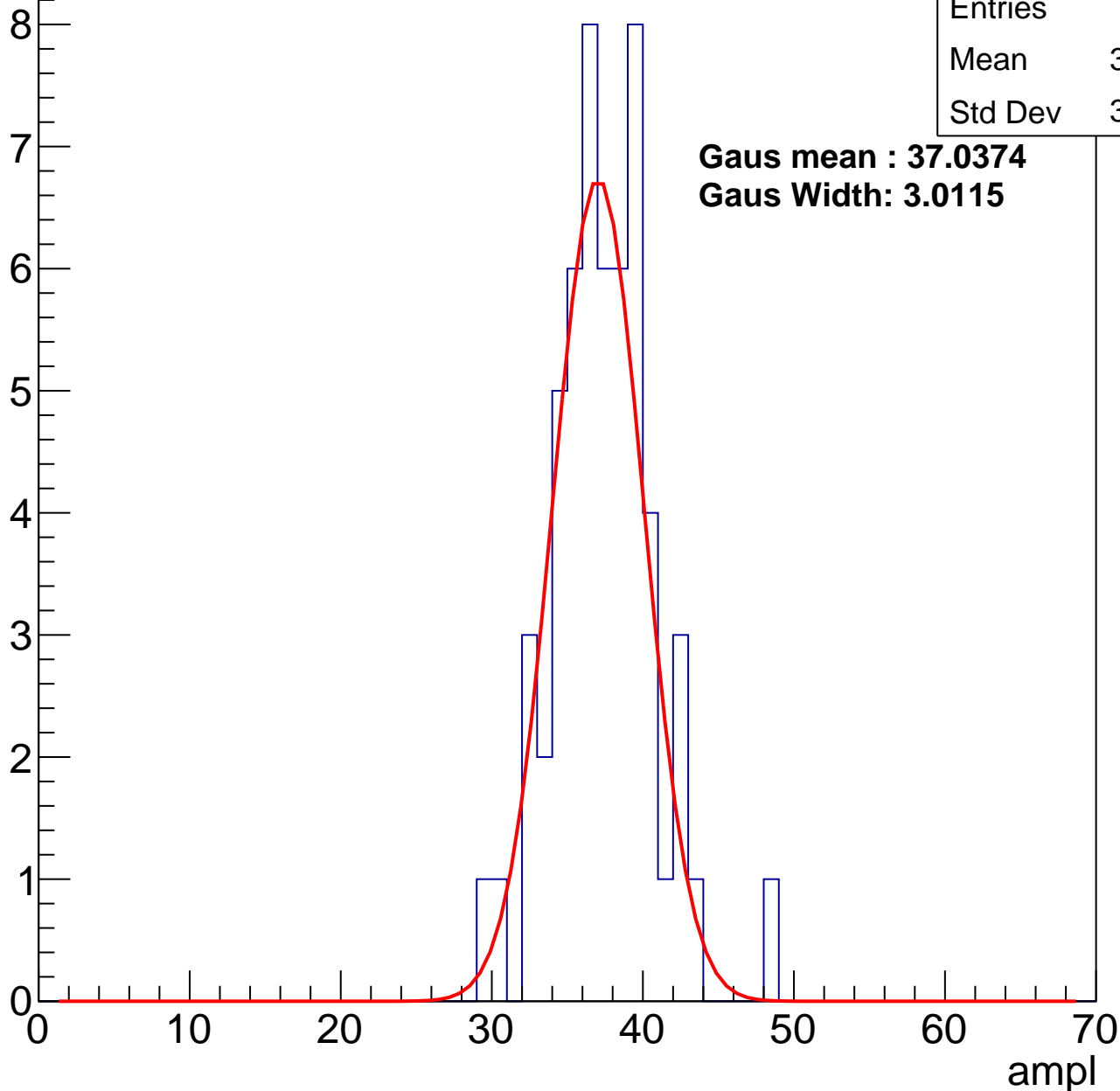
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	36.95
Std Dev	3.324

**Gaus mean : 37.0374**

**Gaus Width: 3.0115**



# B1L102S, U21-ch105, adc2

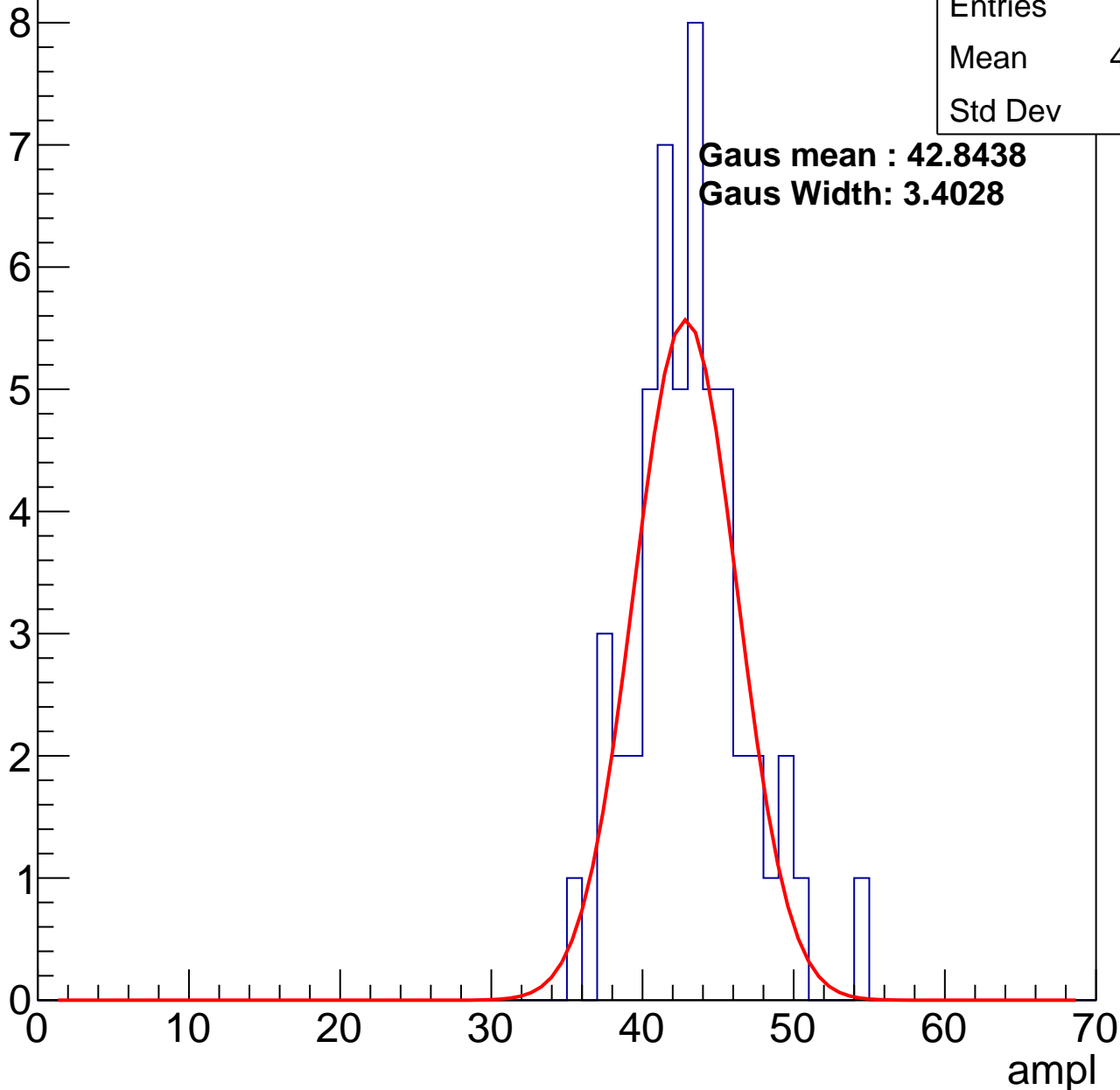
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	42.73
Std Dev	3.59

**Gaus mean : 42.8438**

**Gaus Width: 3.4028**

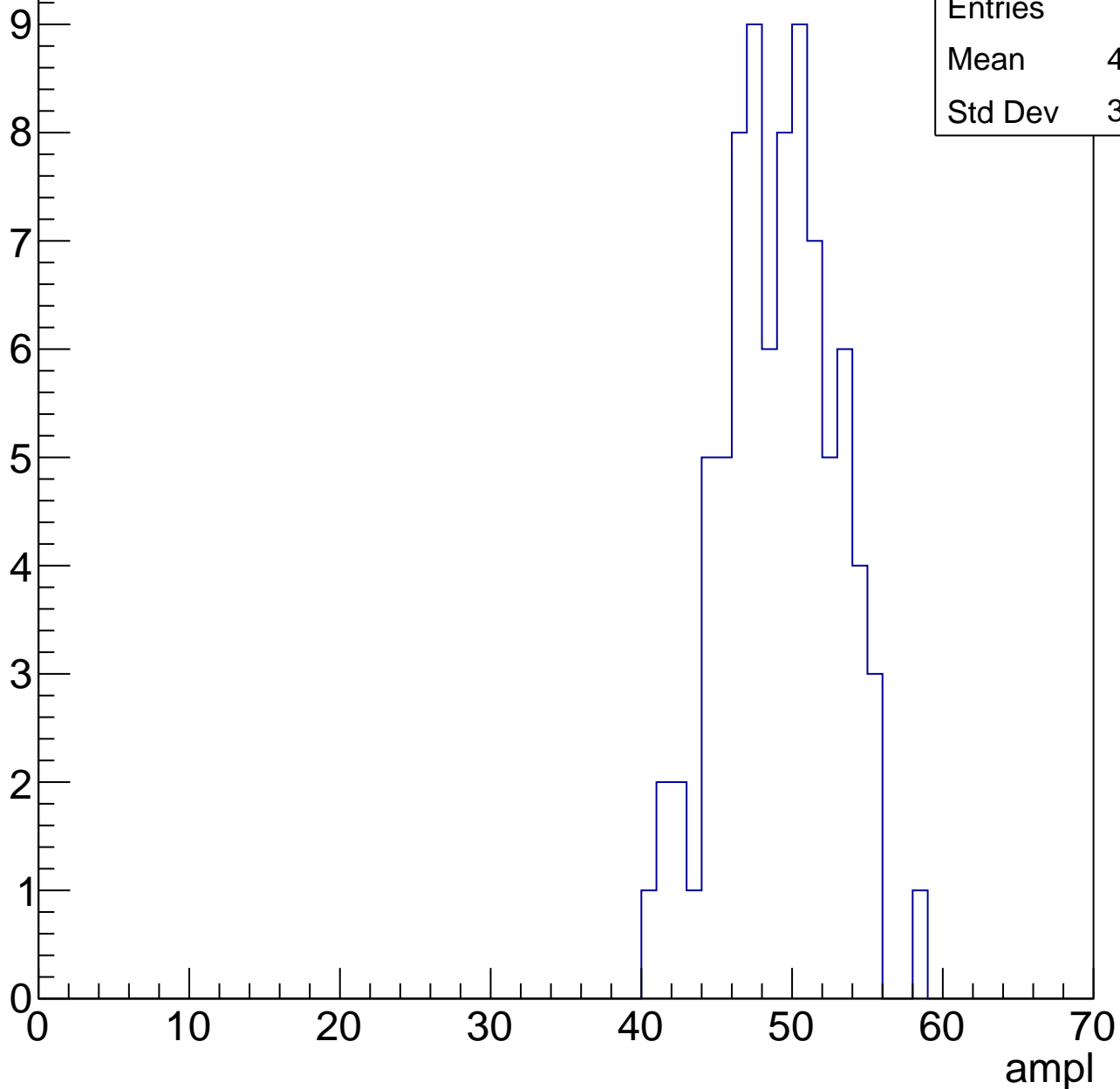


# B1L102S, U21-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	48.65
Std Dev	3.694

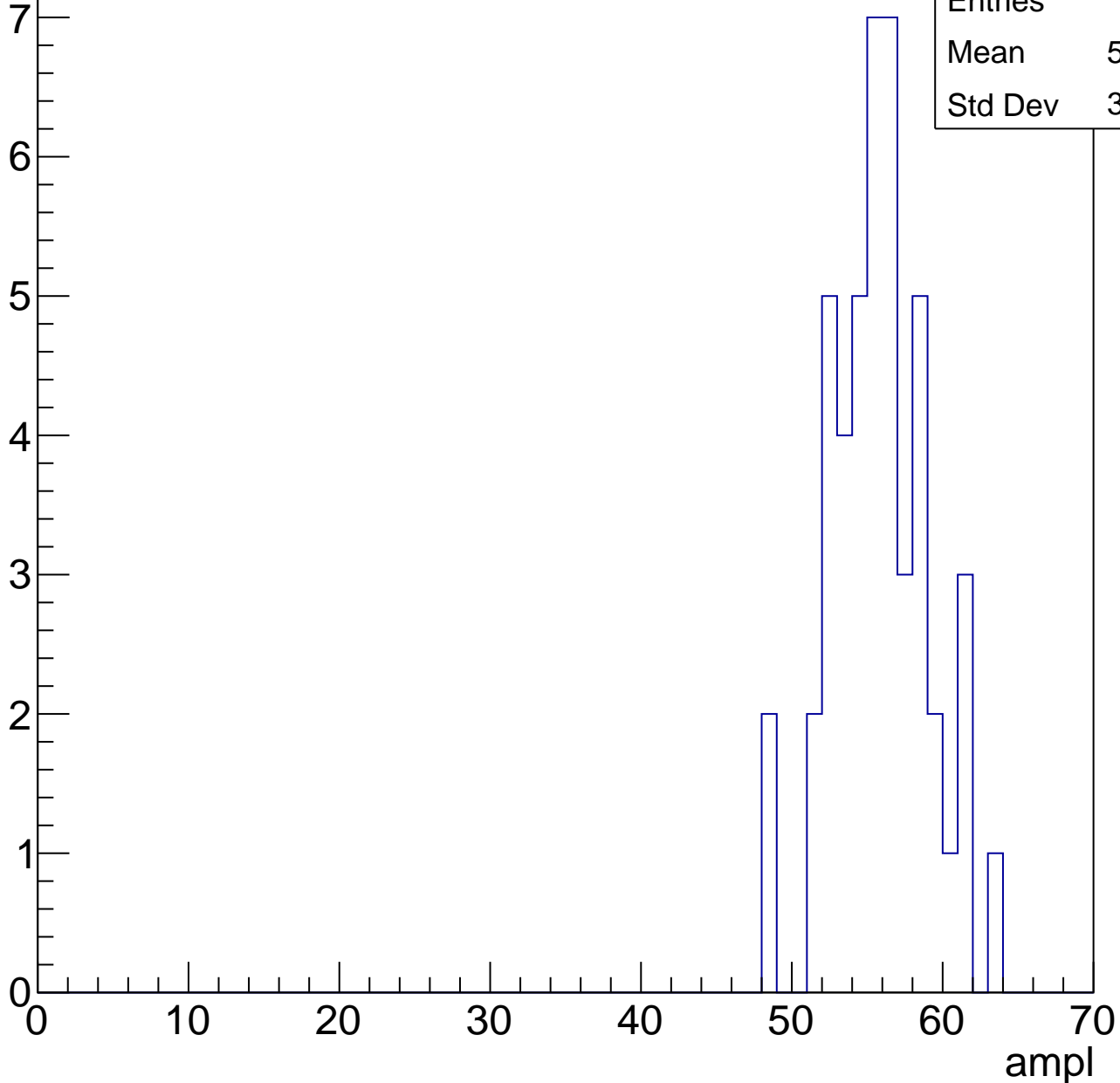


# B1L102S, U21-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

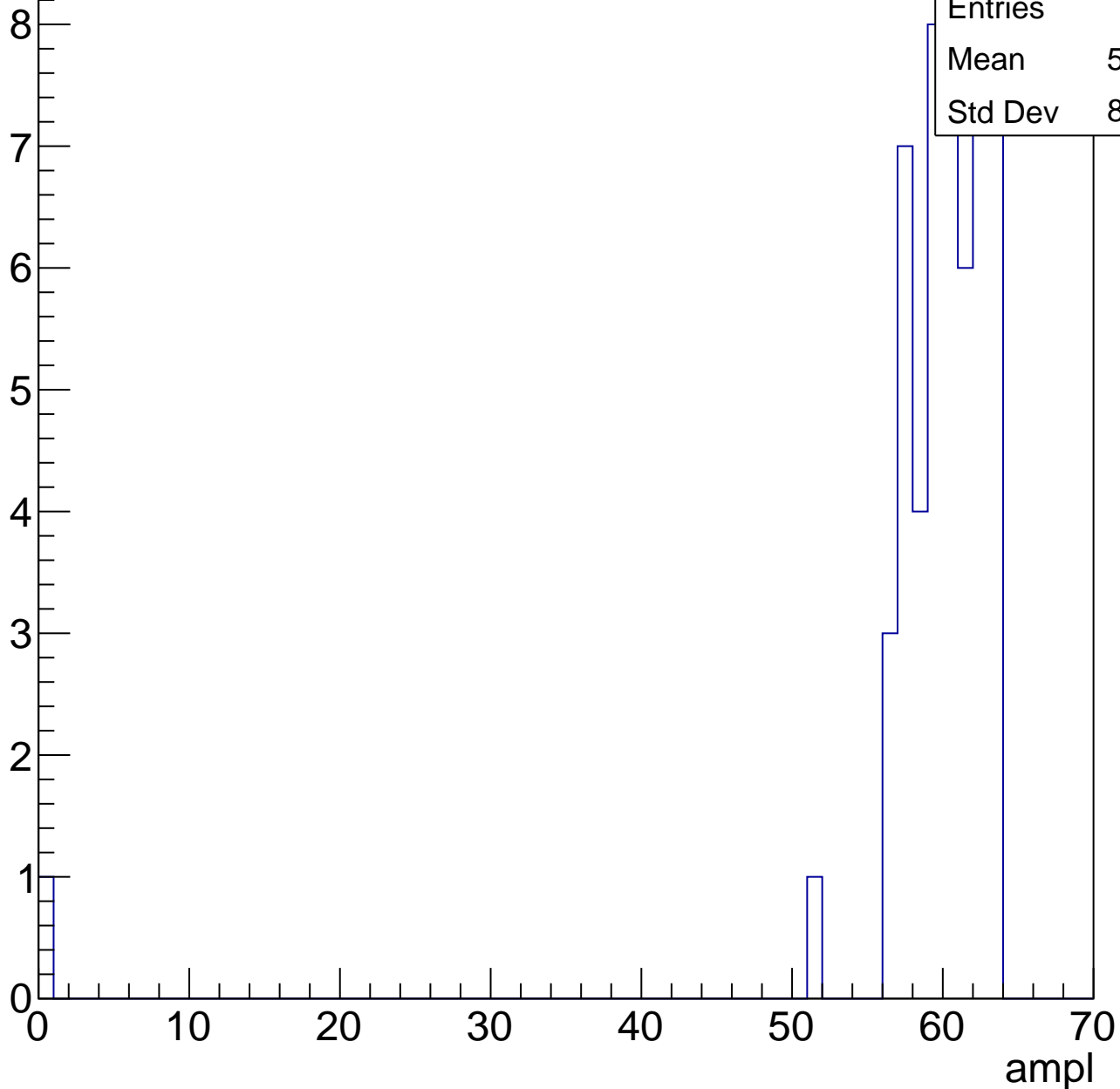
Entries	47
Mean	55.36
Std Dev	3.205



# B1L102S, U21-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	5
Mean	61.6
Std Dev	1.02



# B1L102S, U21-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U21-ch106, adc0

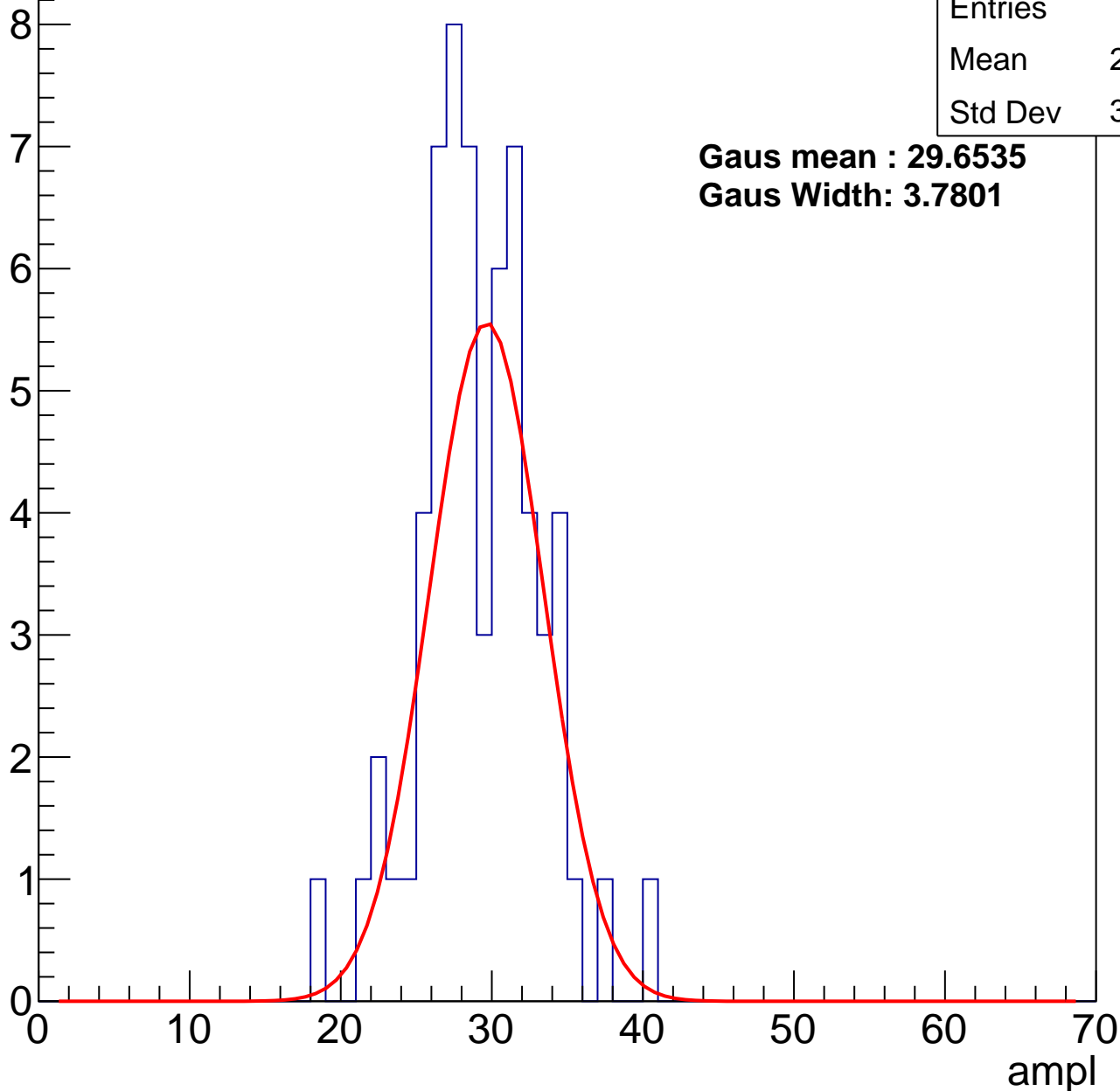
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	28.76
Std Dev	3.905

**Gaus mean : 29.6535**

**Gaus Width: 3.7801**



# B1L102S, U21-ch106, adc1

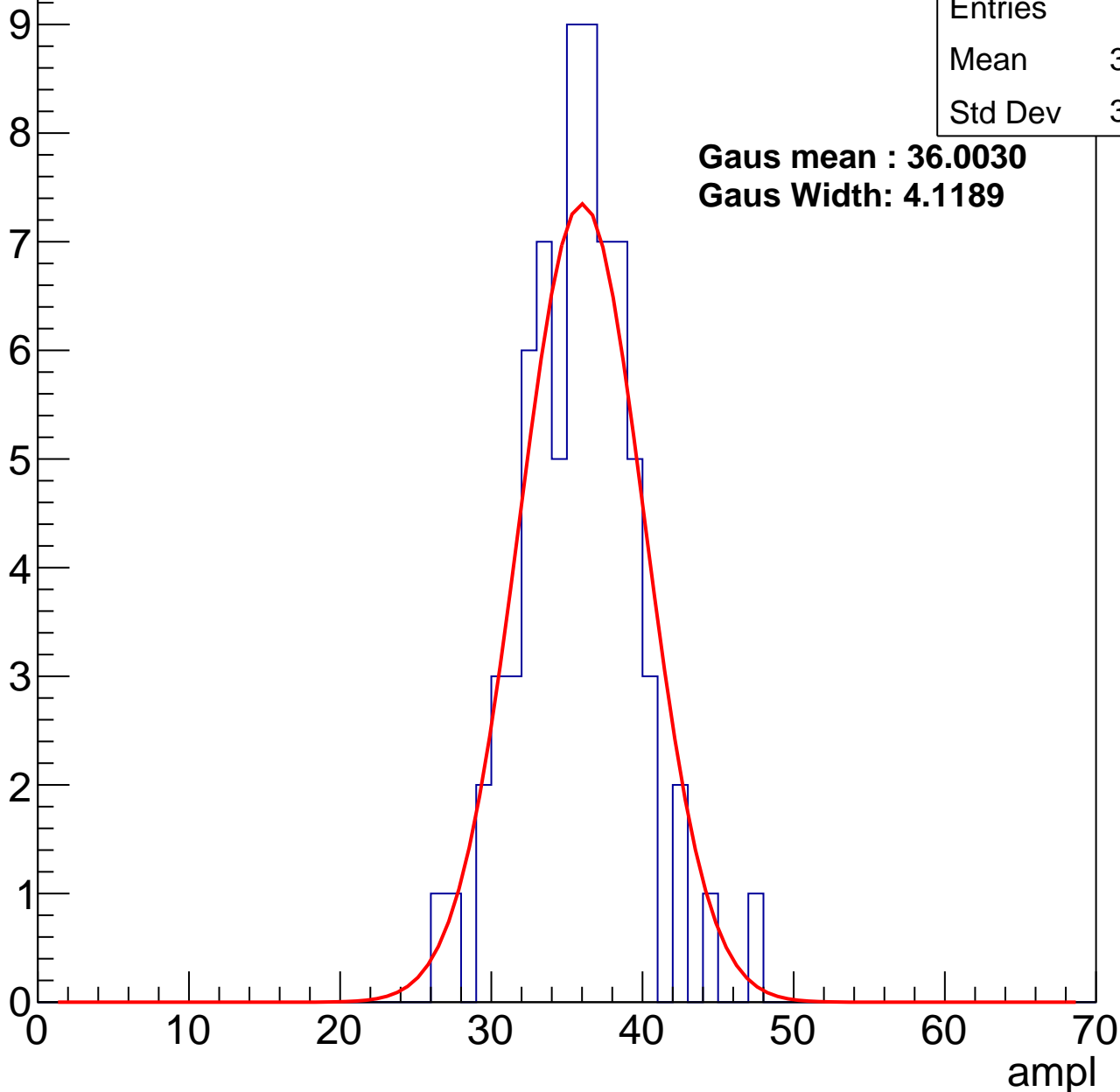
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	35.29
Std Dev	3.725

**Gaus mean : 36.0030**

**Gaus Width: 4.1189**



# B1L102S, U21-ch106, adc2

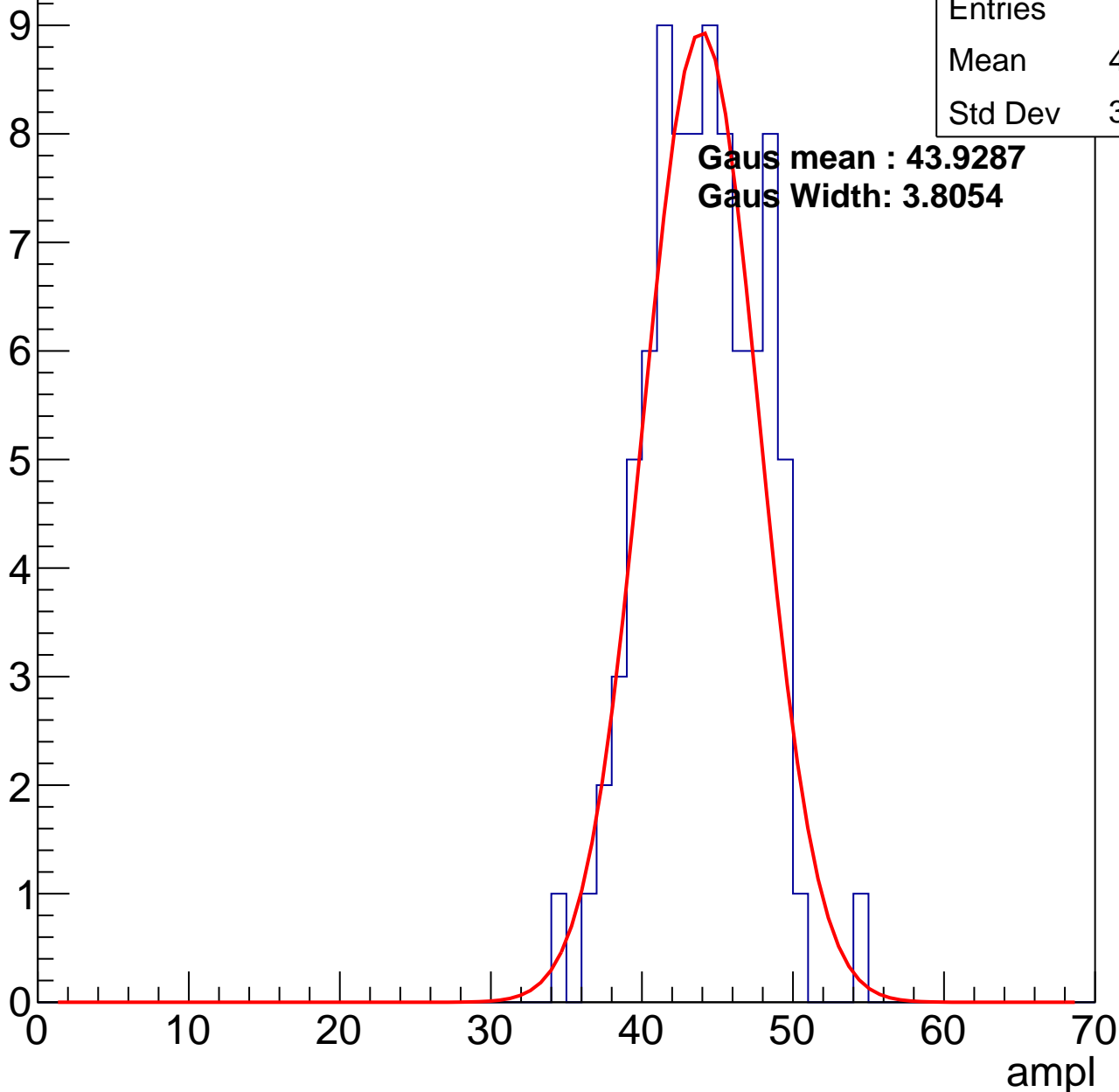
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	87
Mean	43.55
Std Dev	3.666

**Gaus mean : 43.9287**

**Gaus Width: 3.8054**

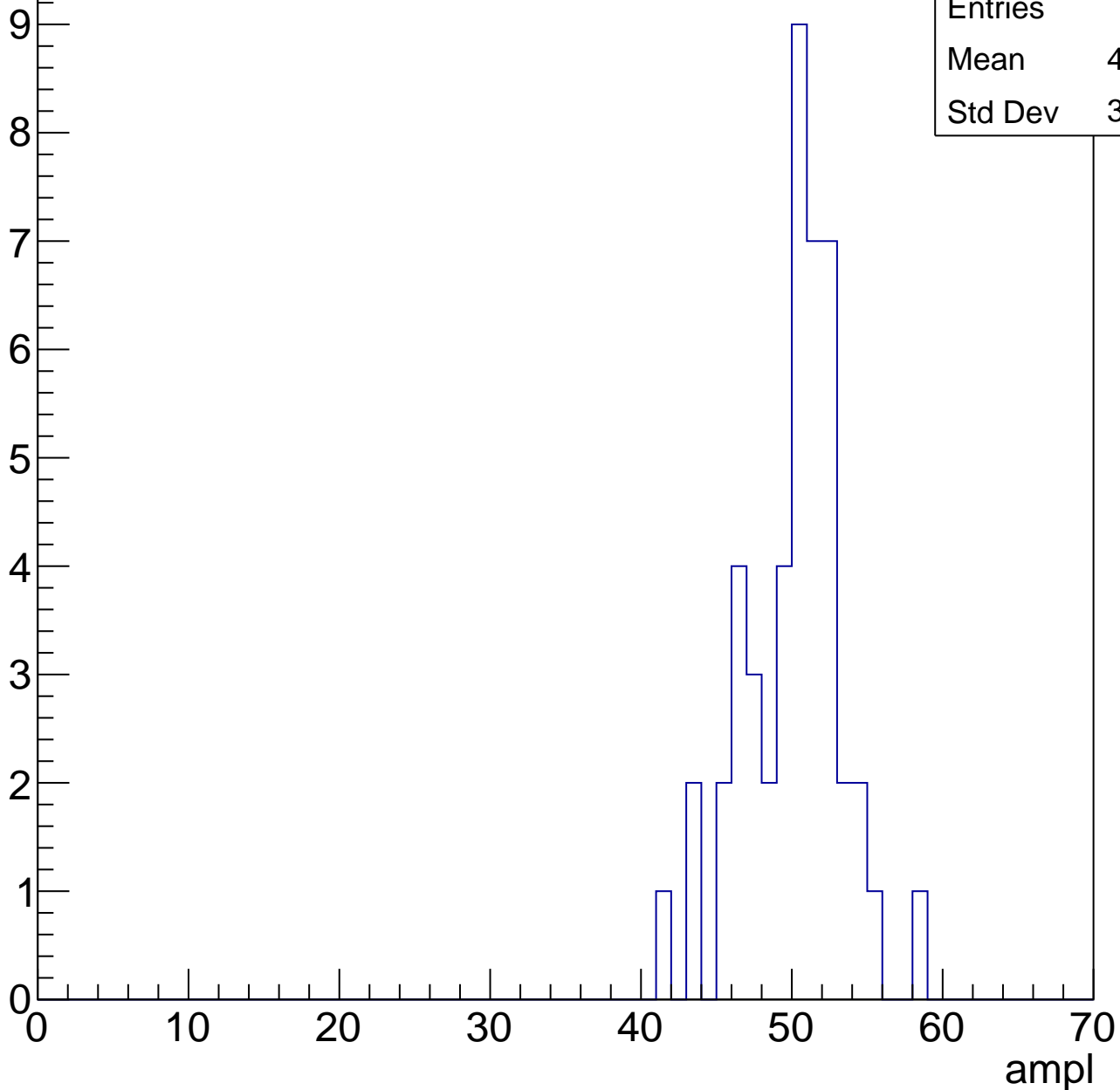


# B1L102S, U21-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	49.62
Std Dev	3.259

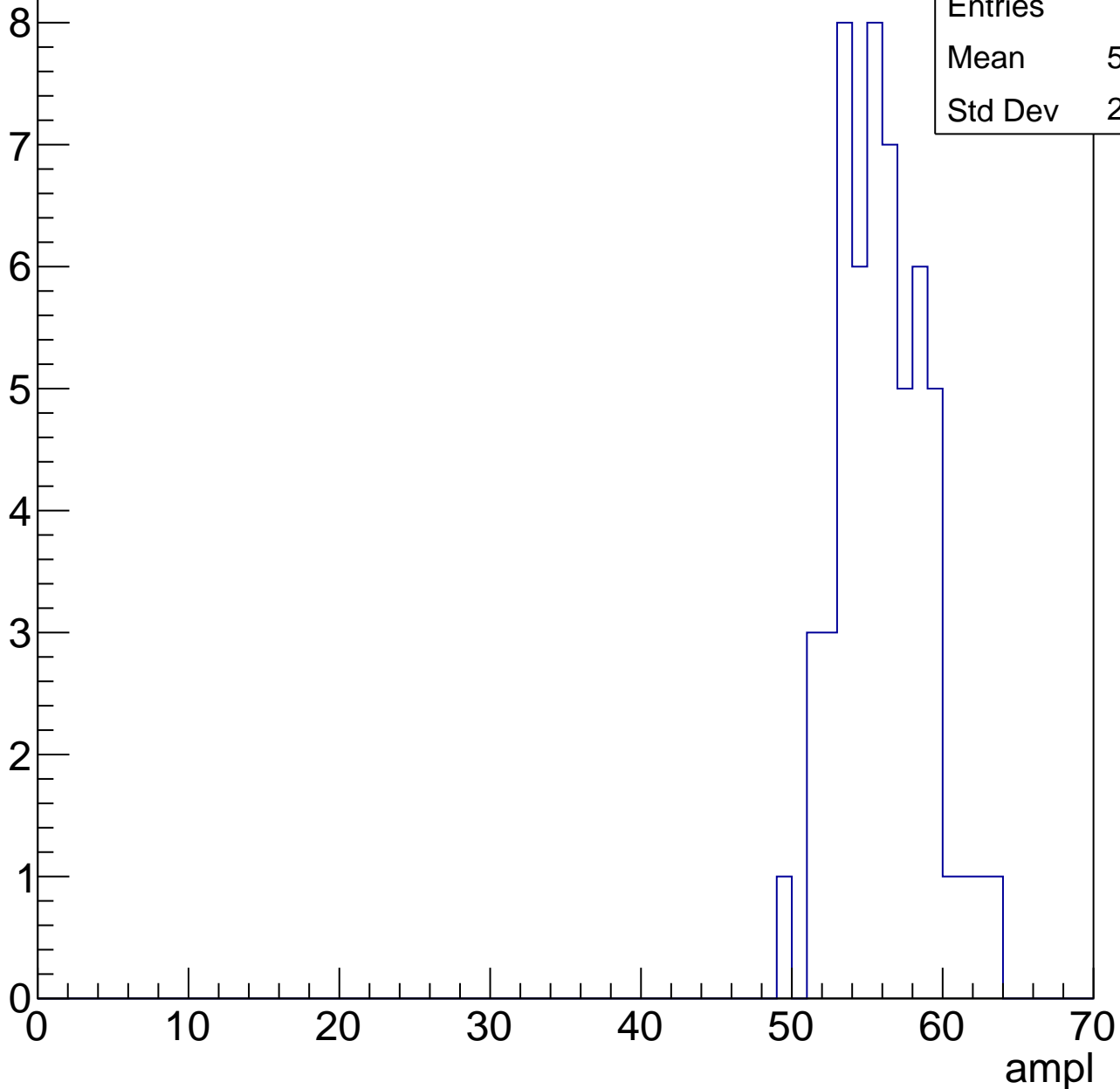


# B1L102S, U21-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

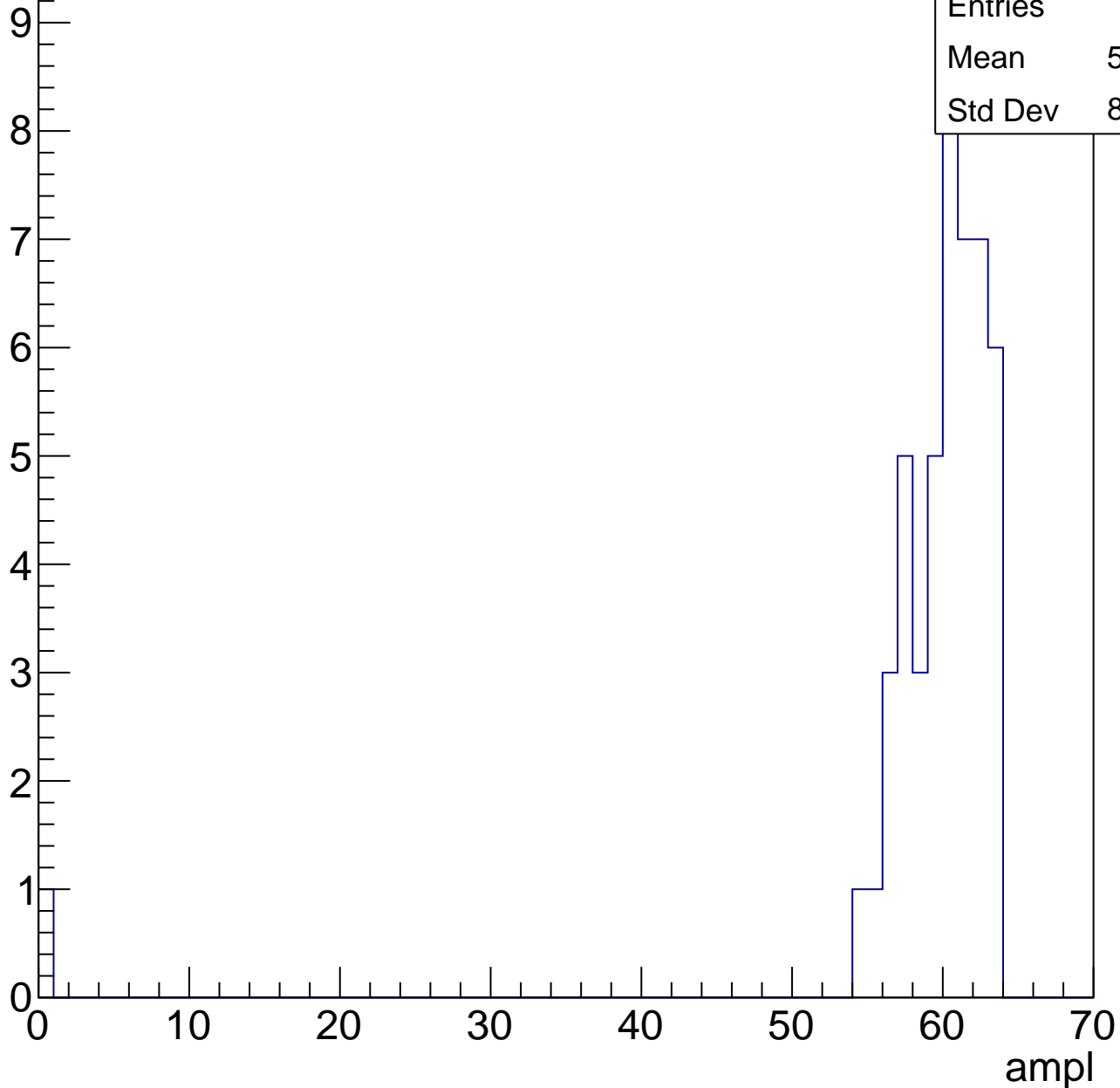
Entries	56
Mean	55.57
Std Dev	2.884



# B1L102S, U21-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U21-ch107, adc0

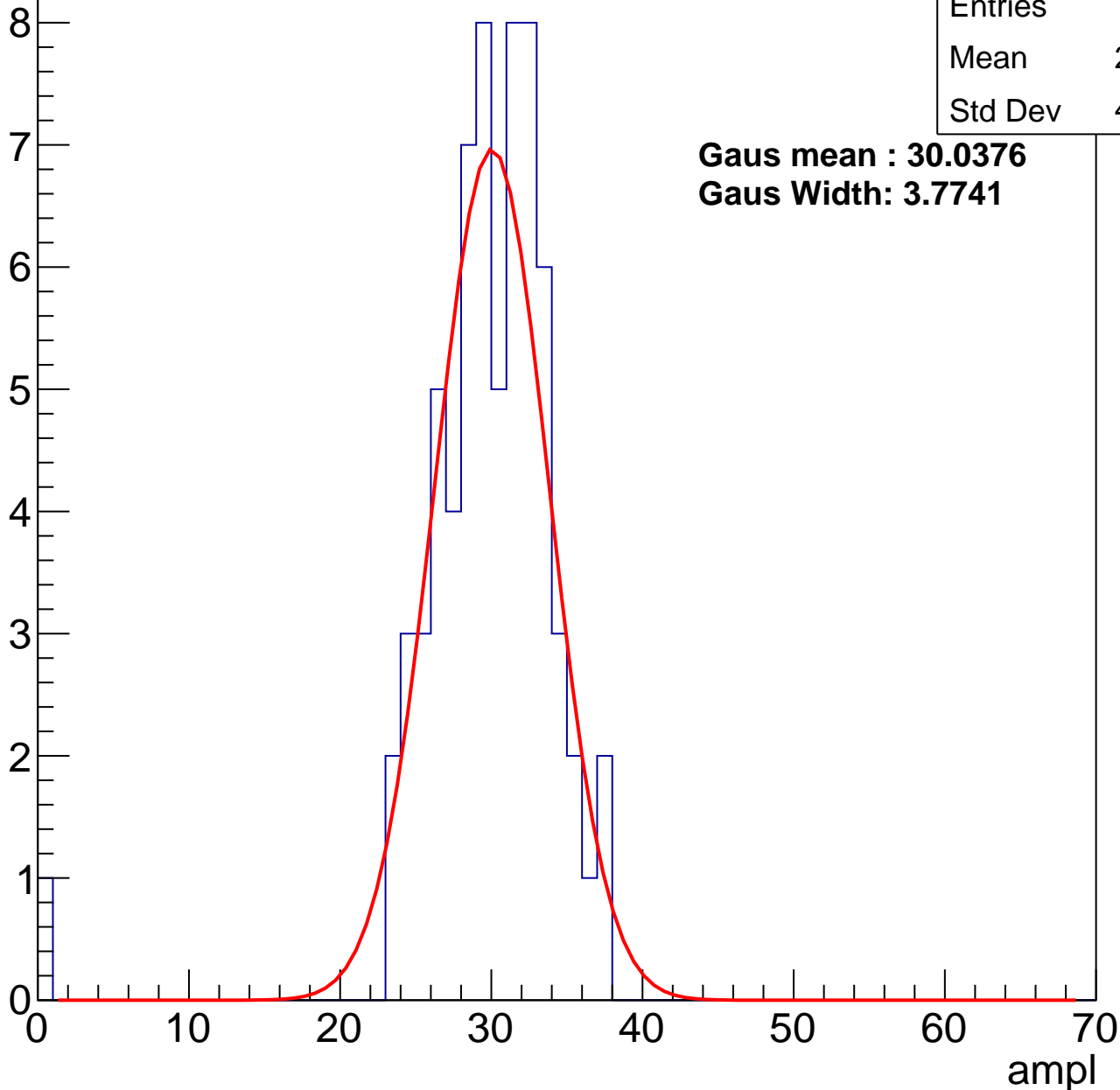
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	29.31
Std Dev	4.891

**Gaus mean : 30.0376**

**Gaus Width: 3.7741**



# B1L102S, U21-ch107, adc1

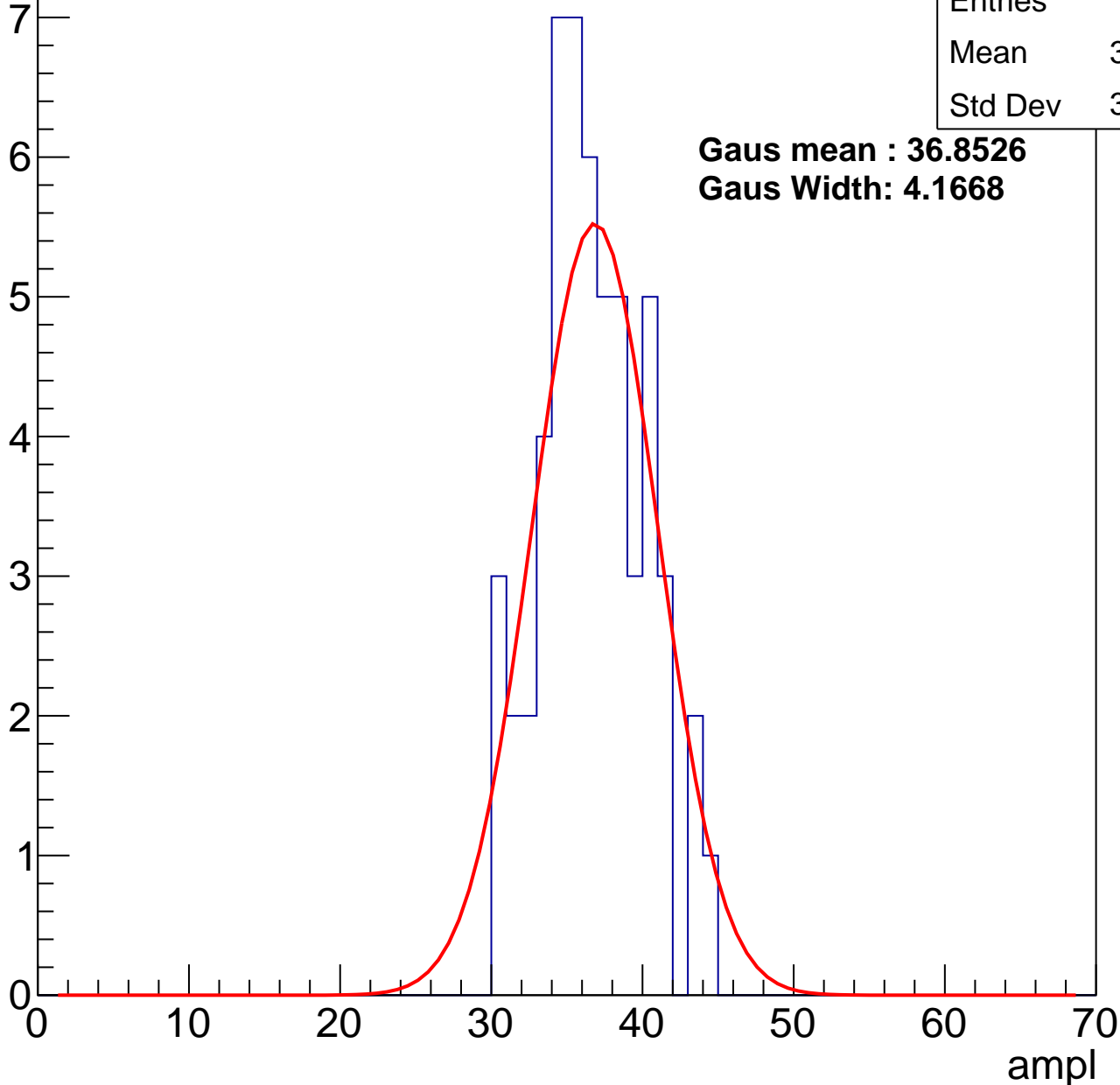
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	36.22
Std Dev	3.377

**Gaus mean : 36.8526**

**Gaus Width: 4.1668**



# B1L102S, U21-ch107, adc2

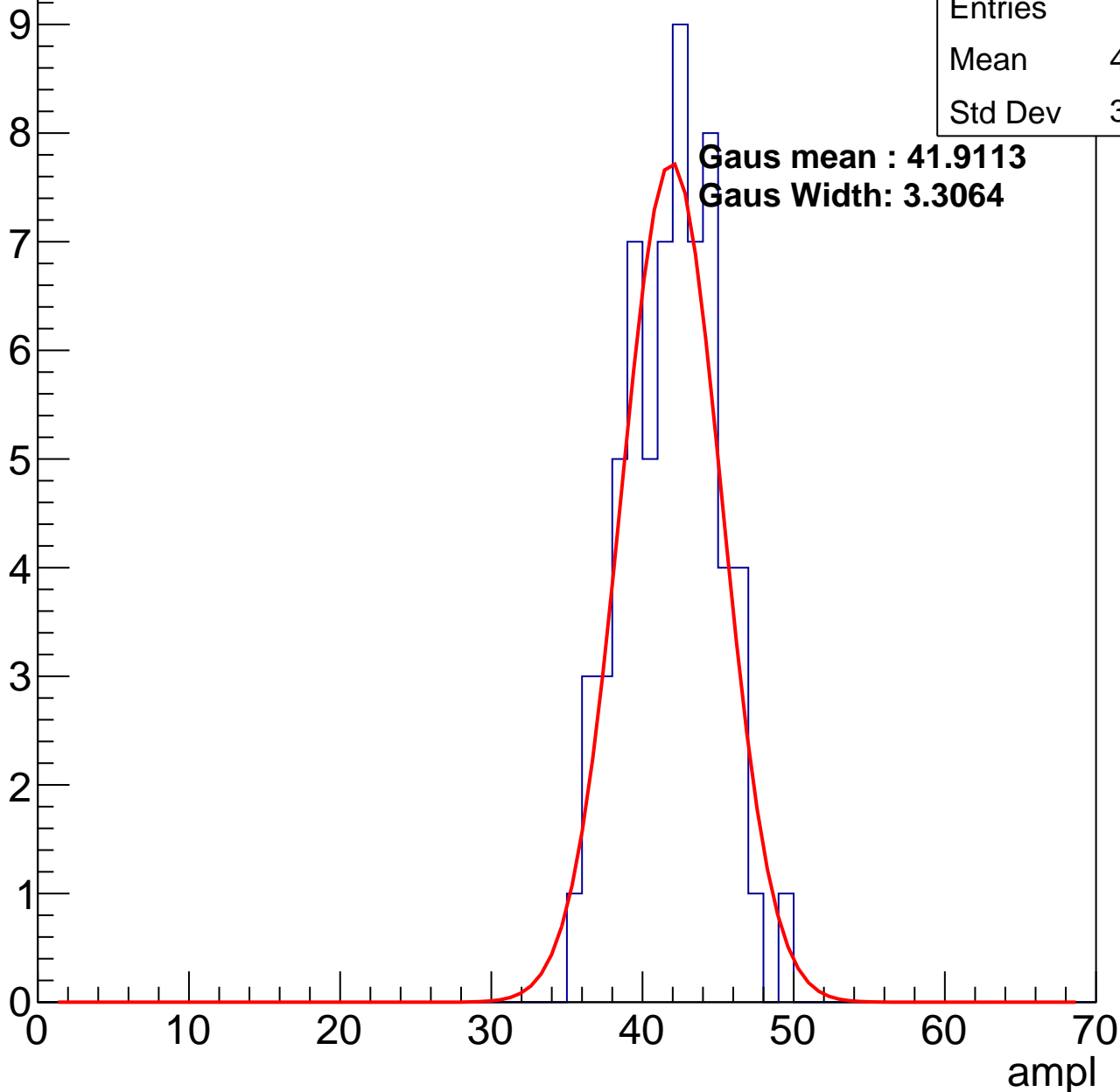
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	41.46
Std Dev	3.028

**Gaus mean : 41.9113**

**Gaus Width: 3.3064**



# B1L102S, U21-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	73
Mean	49.11
Std Dev	2.954

Entry

10

8

6

4

2

0

0

10

20

30

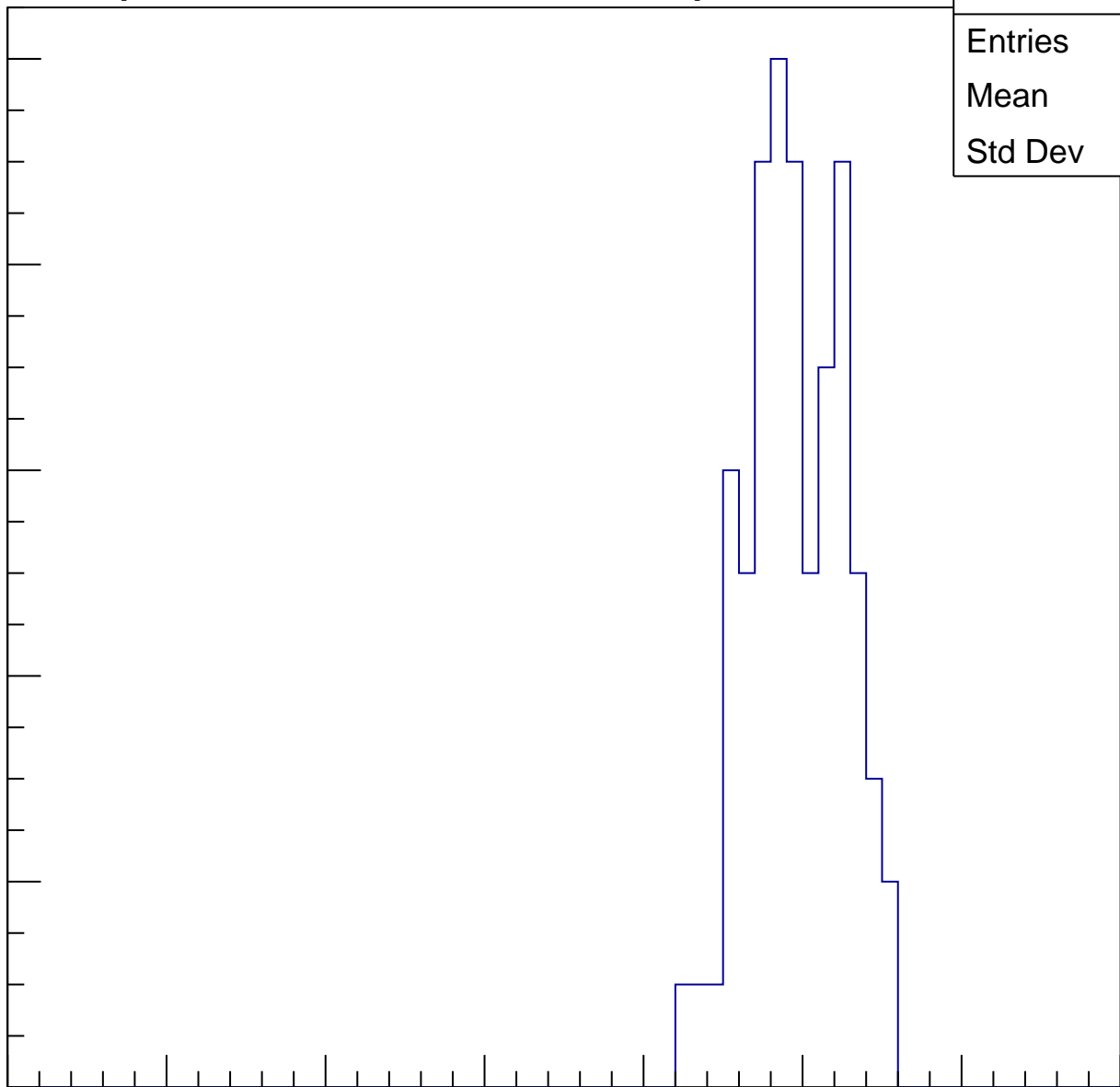
40

50

60

70

ampl

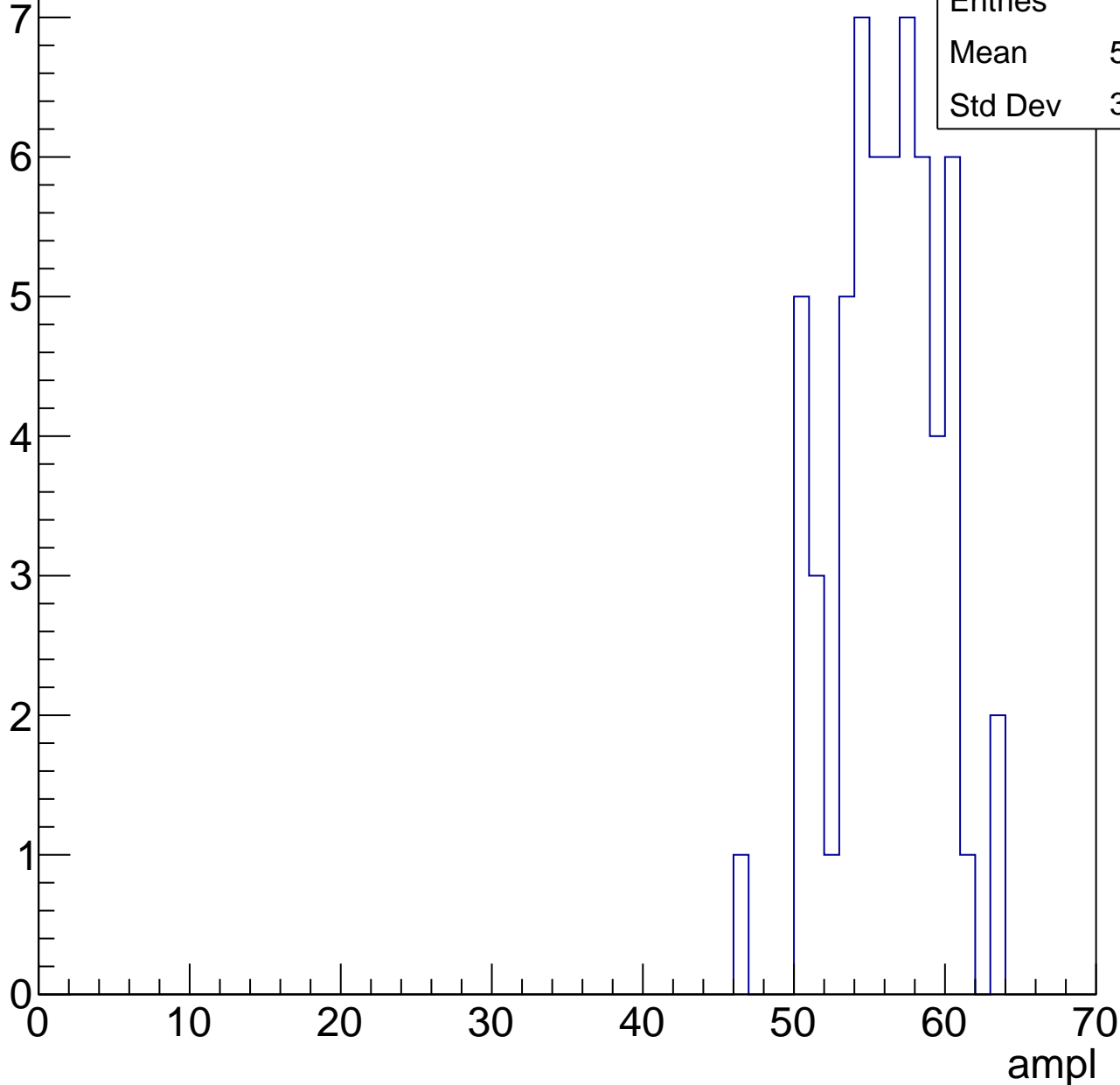


# B1L102S, U21-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	55.67
Std Dev	3.486

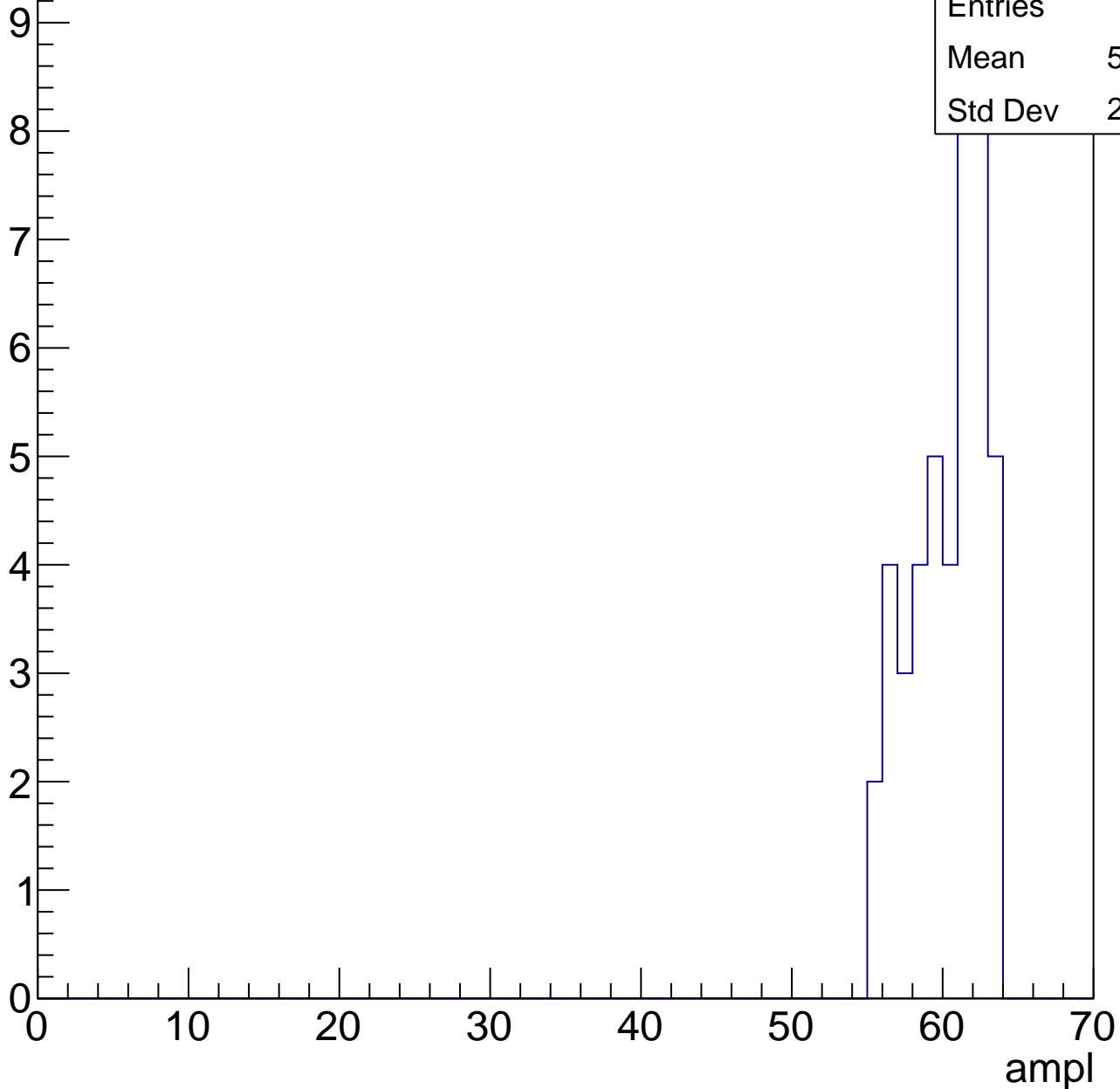


# B1L102S, U21-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	59.87
Std Dev	2.363



# B1L102S, U21-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

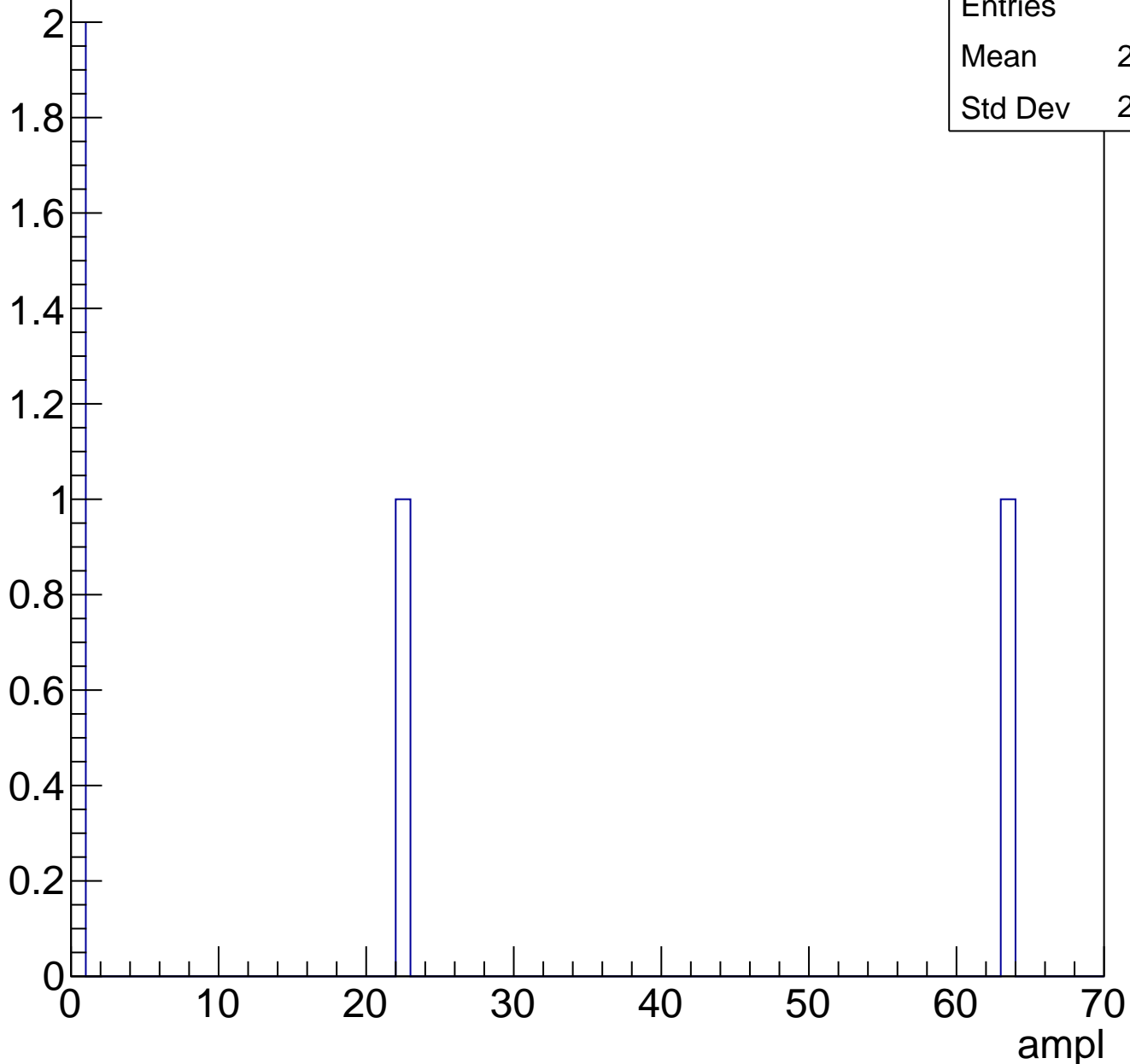




# B1L102S, U21-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	4
Mean	21.25
Std Dev	25.72

# B1L102S, U21-ch108, adc0

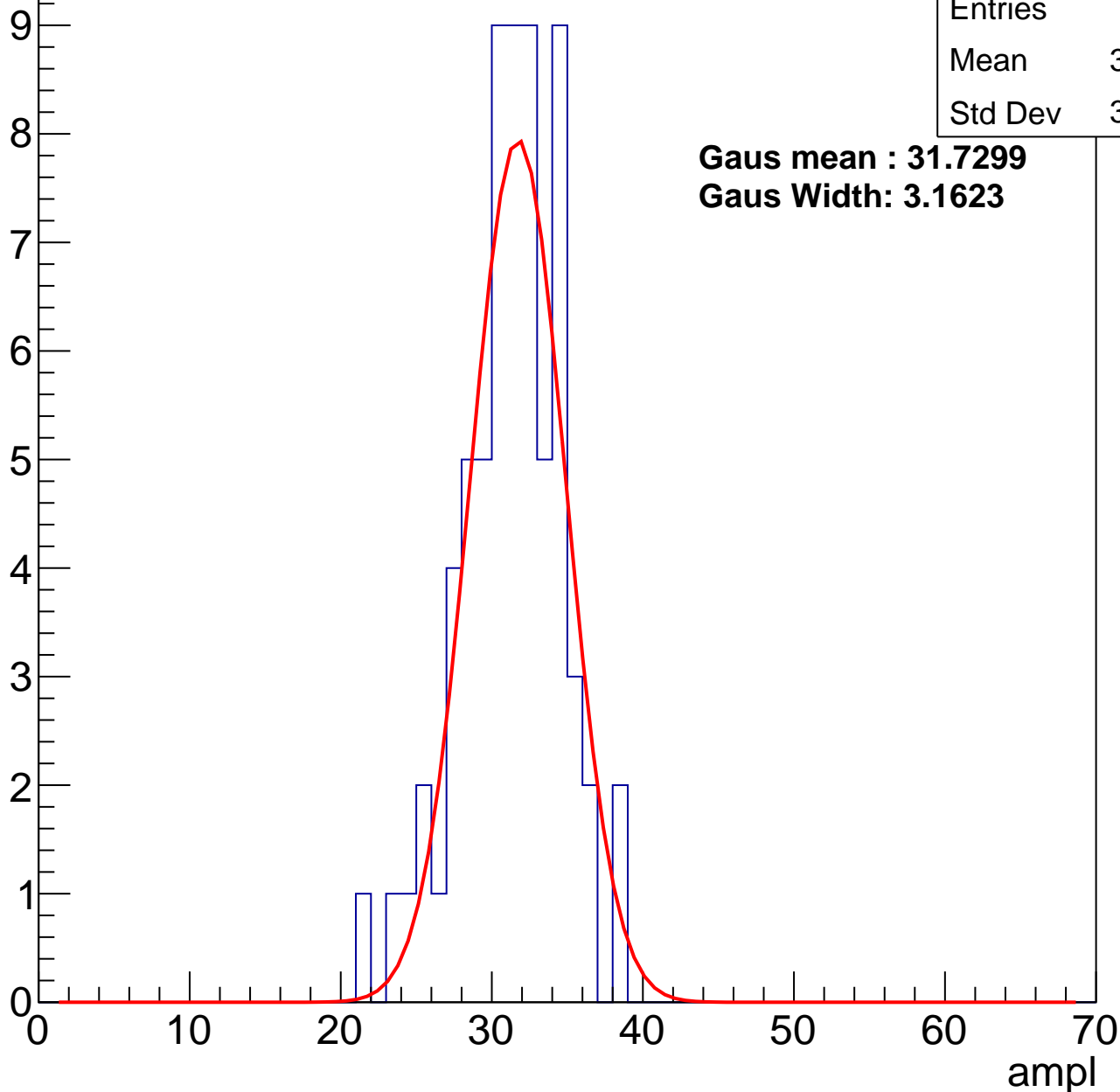
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	30.85
Std Dev	3.327

**Gaus mean : 31.7299**

**Gaus Width: 3.1623**



# B1L102S, U21-ch108, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	70
Mean	38.27
Std Dev	3.277

**Gaus mean : 39.3932**

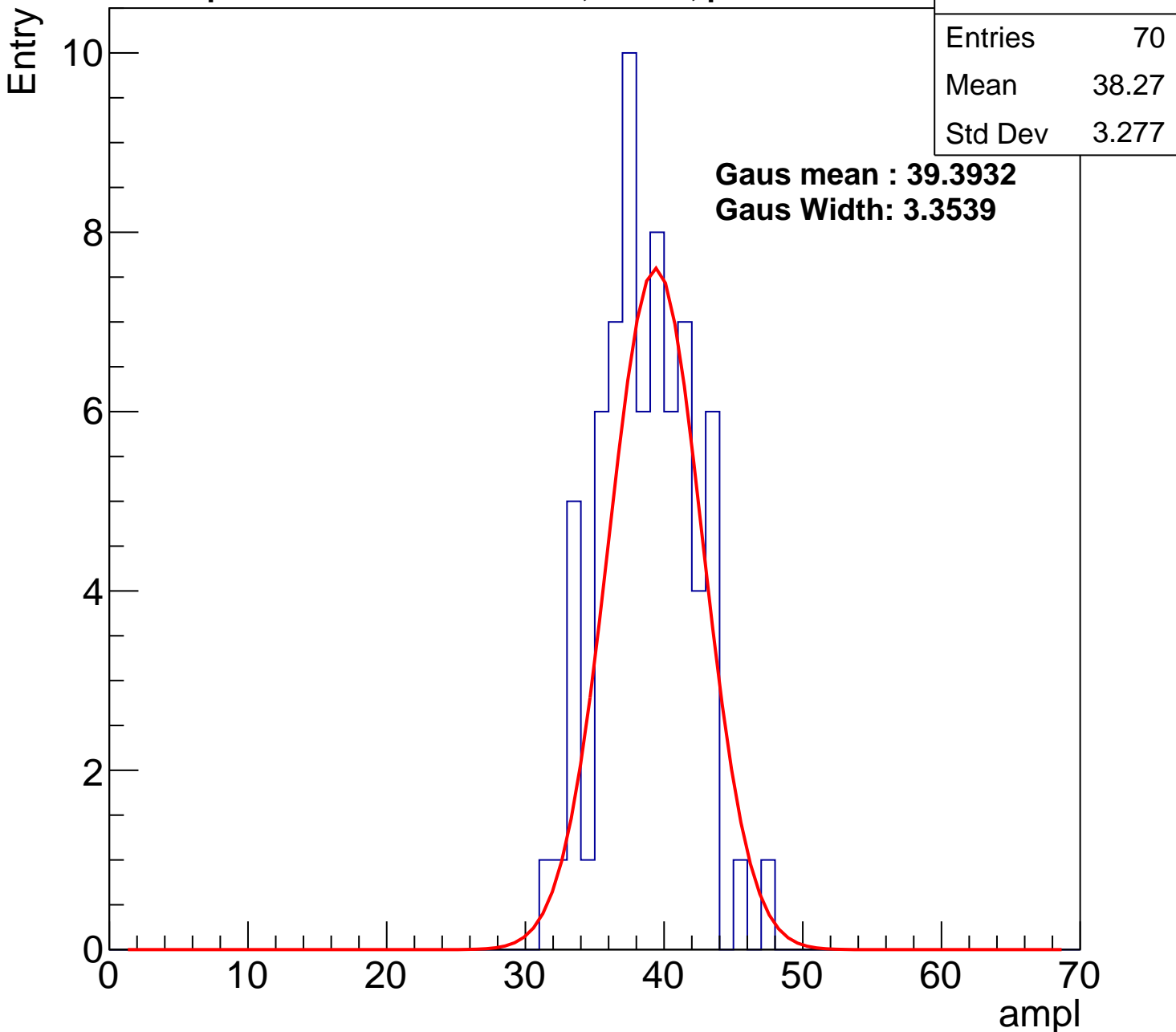
**Gaus Width: 3.3539**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L102S, U21-ch108, adc2

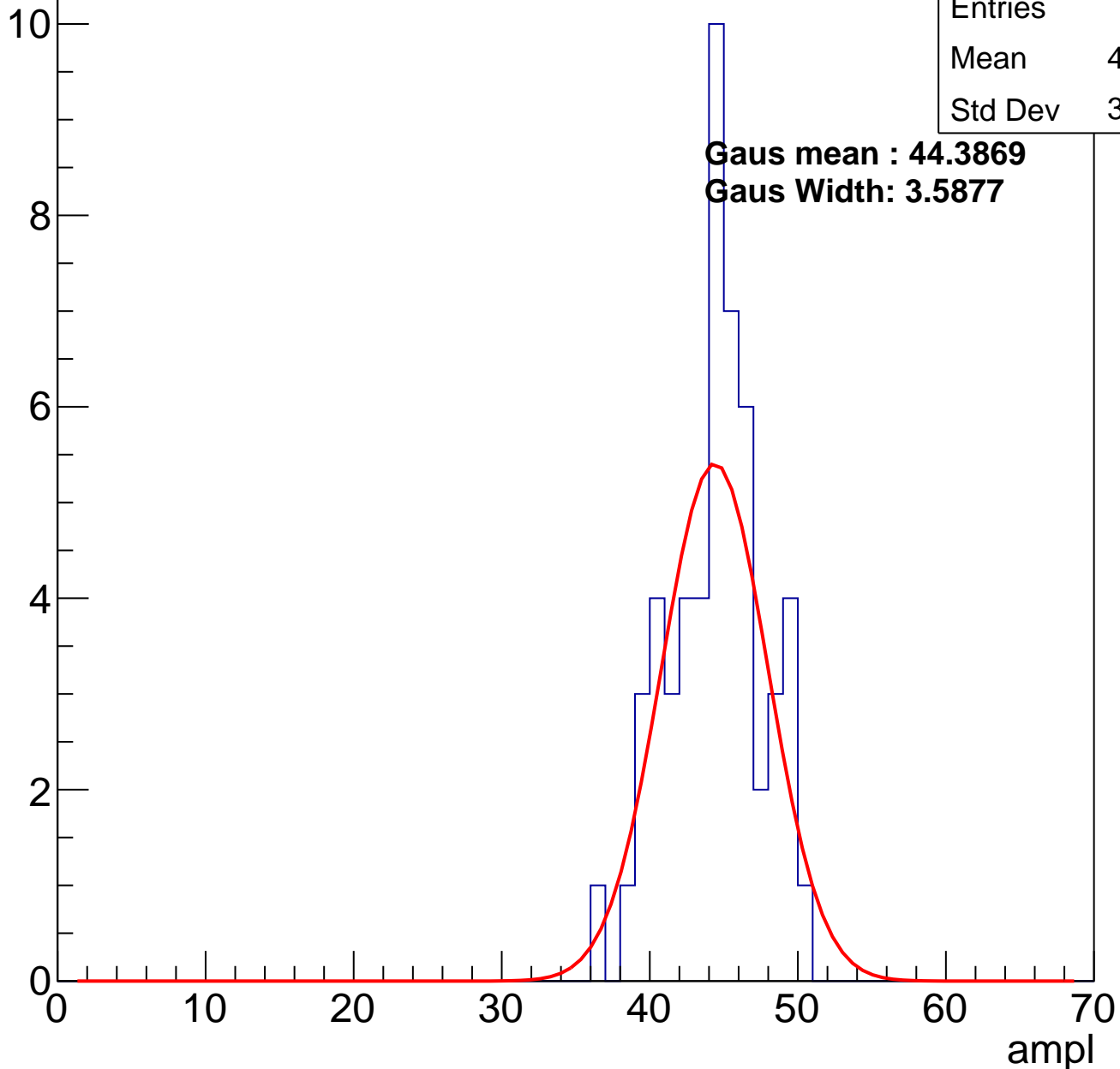
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	53
Mean	43.94
Std Dev	3.129

**Gaus mean : 44.3869**

**Gaus Width: 3.5877**

Entry

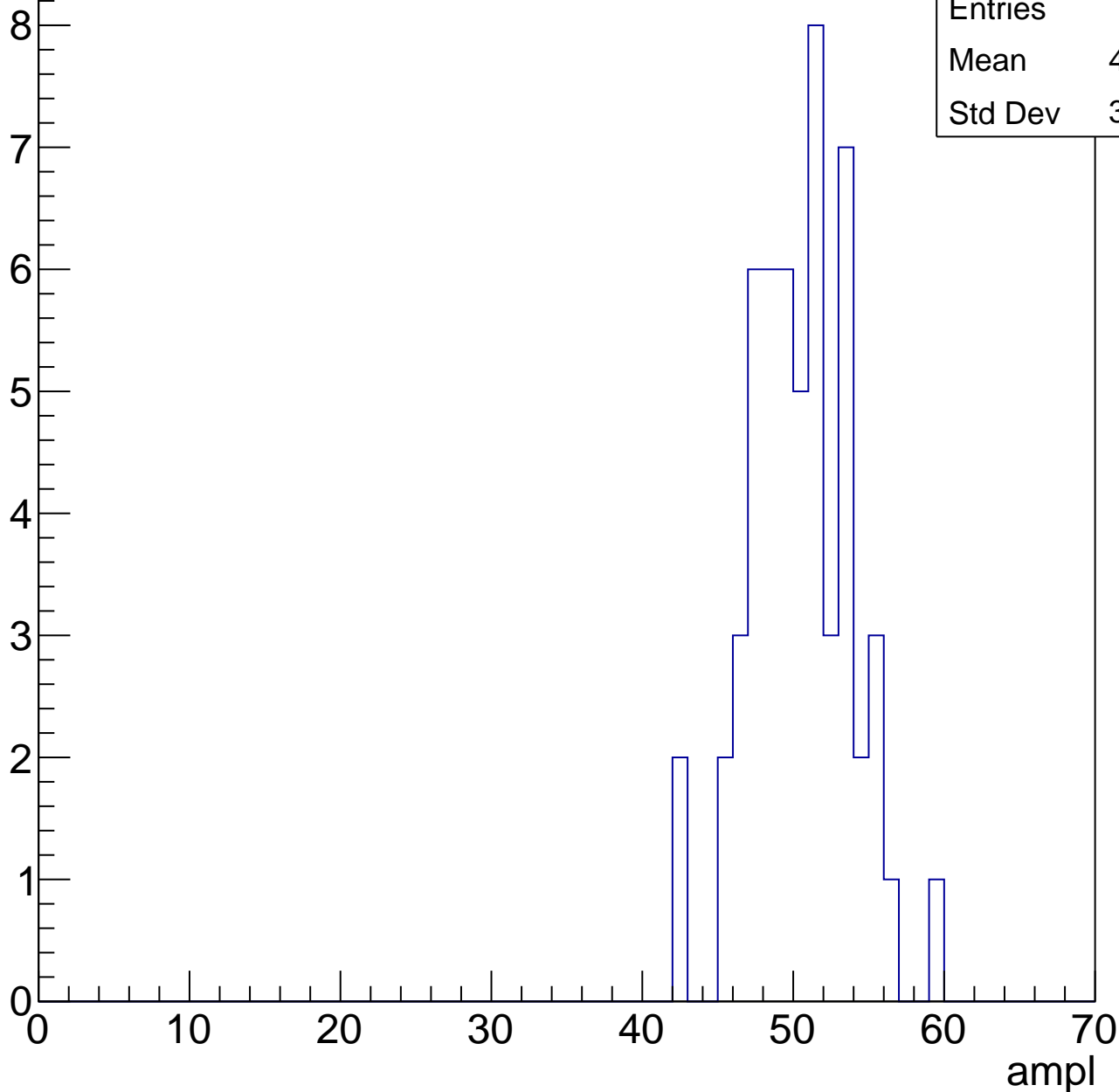


# B1L102S, U21-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	49.98
Std Dev	3.349

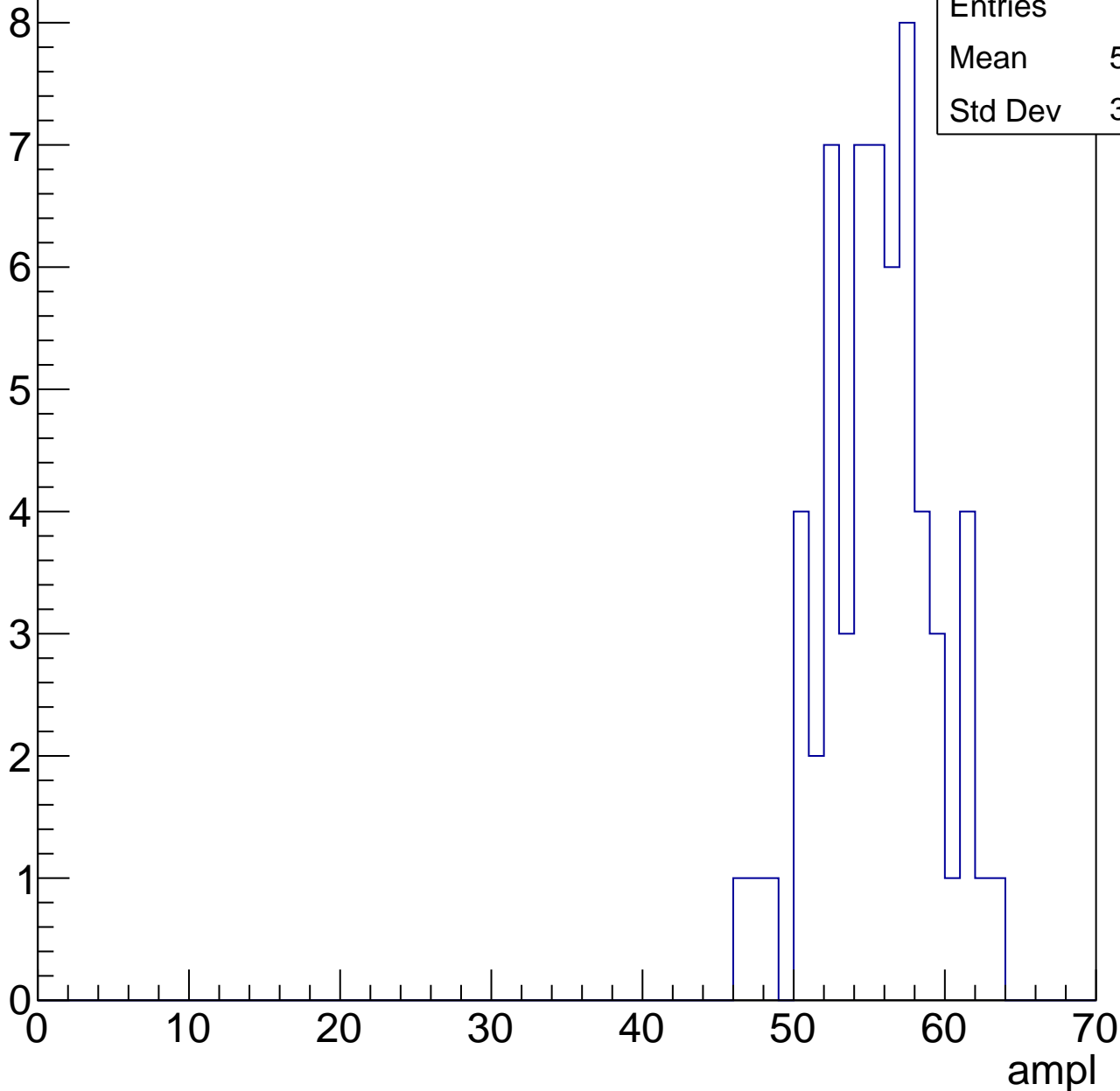


# B1L102S, U21-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	55.07
Std Dev	3.648

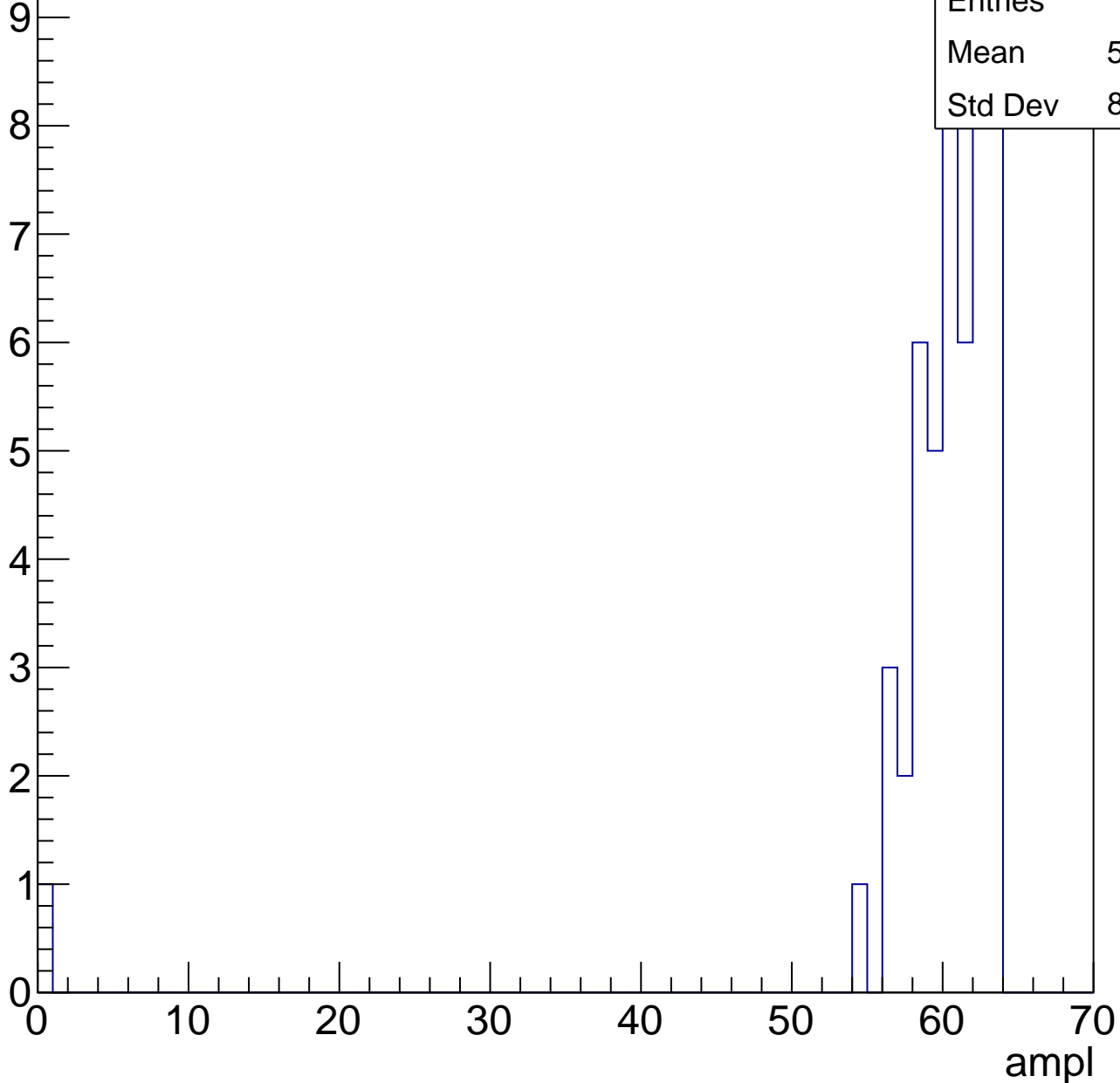


# B1L102S, U21-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

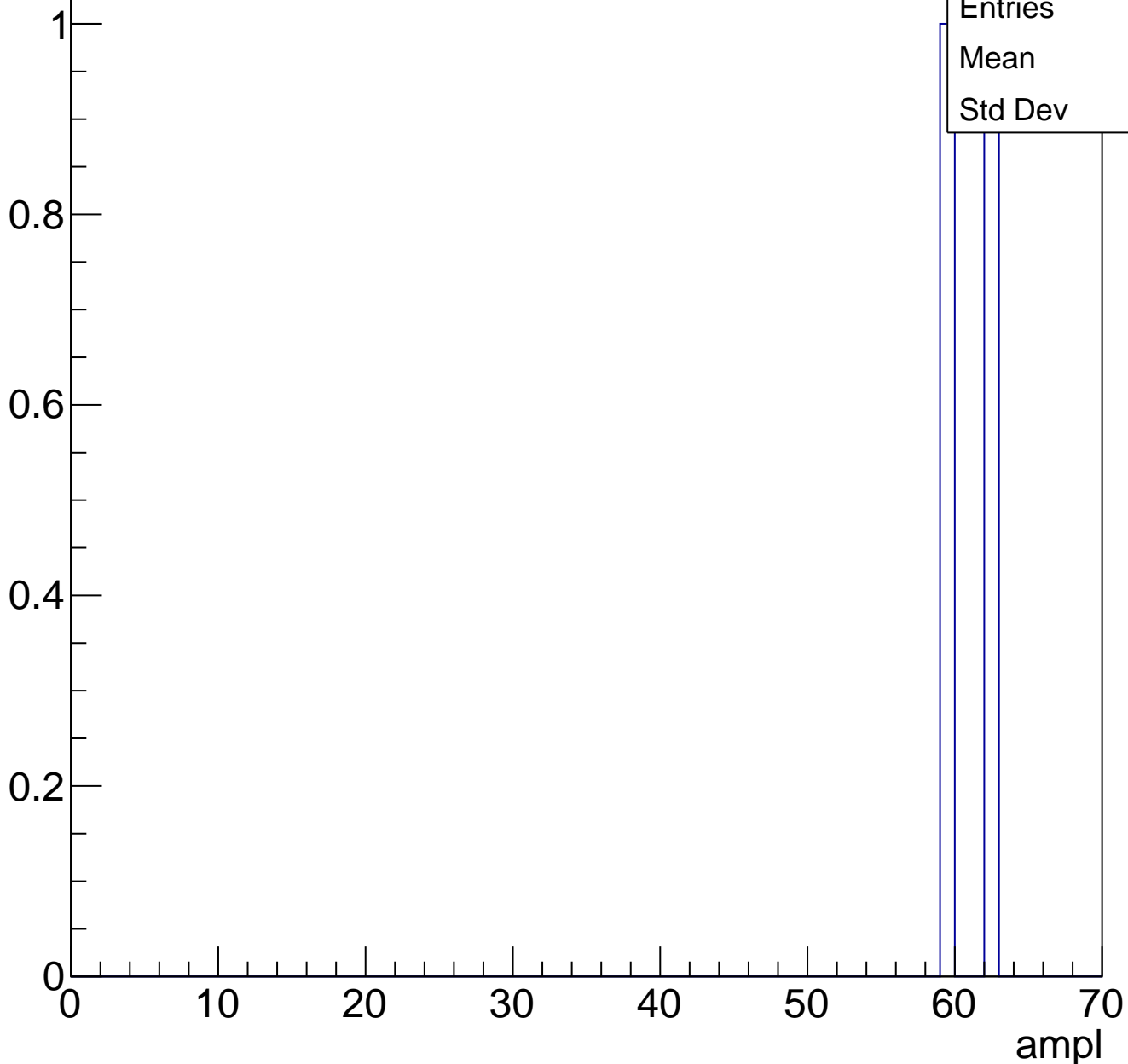
Entries	50
Mean	58.96
Std Dev	8.713



# B1L102S, U21-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	60.5
Std Dev	1.5



# B1L102S, U21-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch109, adc0

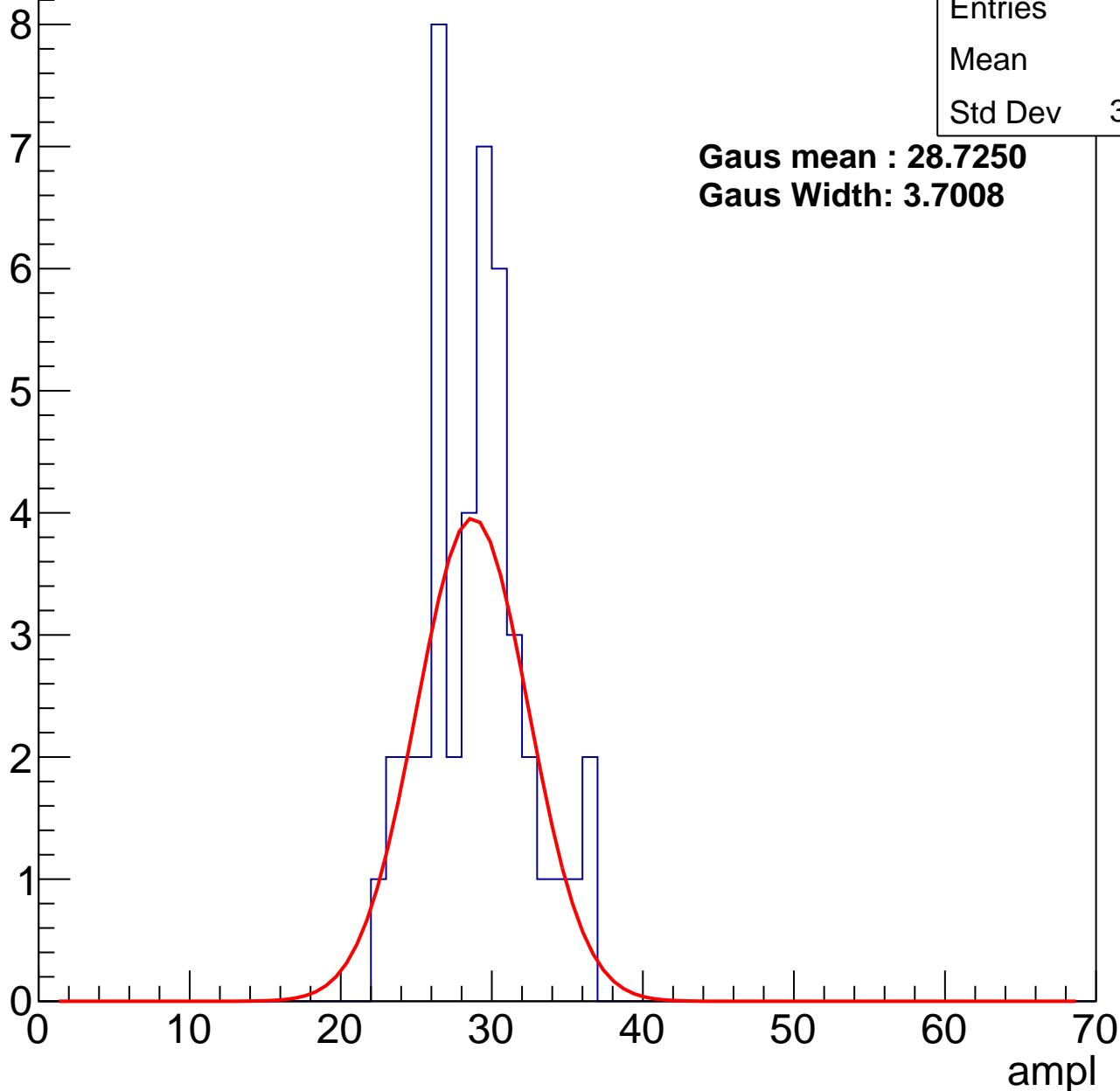
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	44
Mean	28.5
Std Dev	3.327

**Gaus mean : 28.7250**

**Gaus Width: 3.7008**



# B1L102S, U21-ch109, adc1

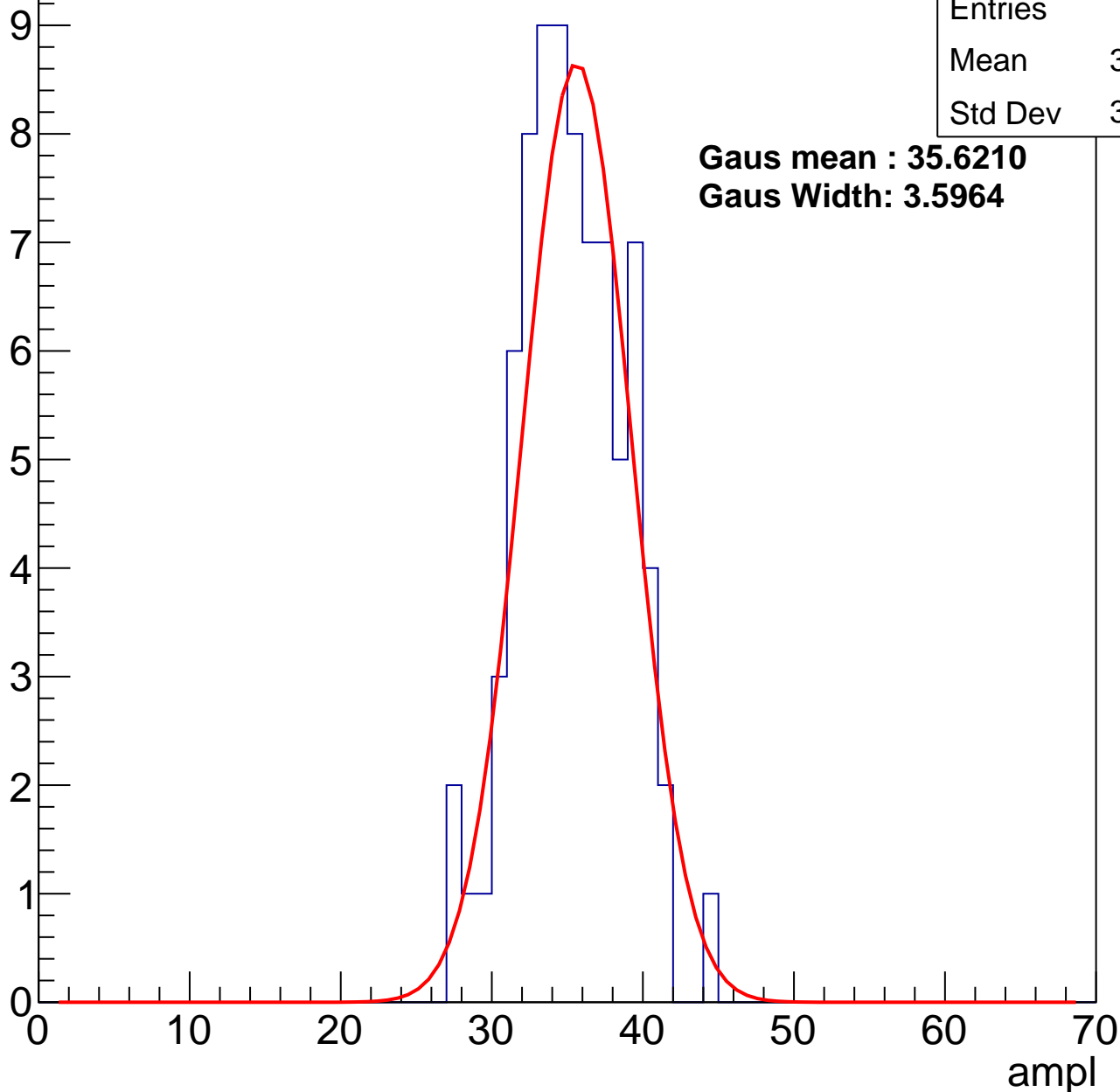
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	34.83
Std Dev	3.434

**Gaus mean : 35.6210**

**Gaus Width: 3.5964**



# B1L102S, U21-ch109, adc2

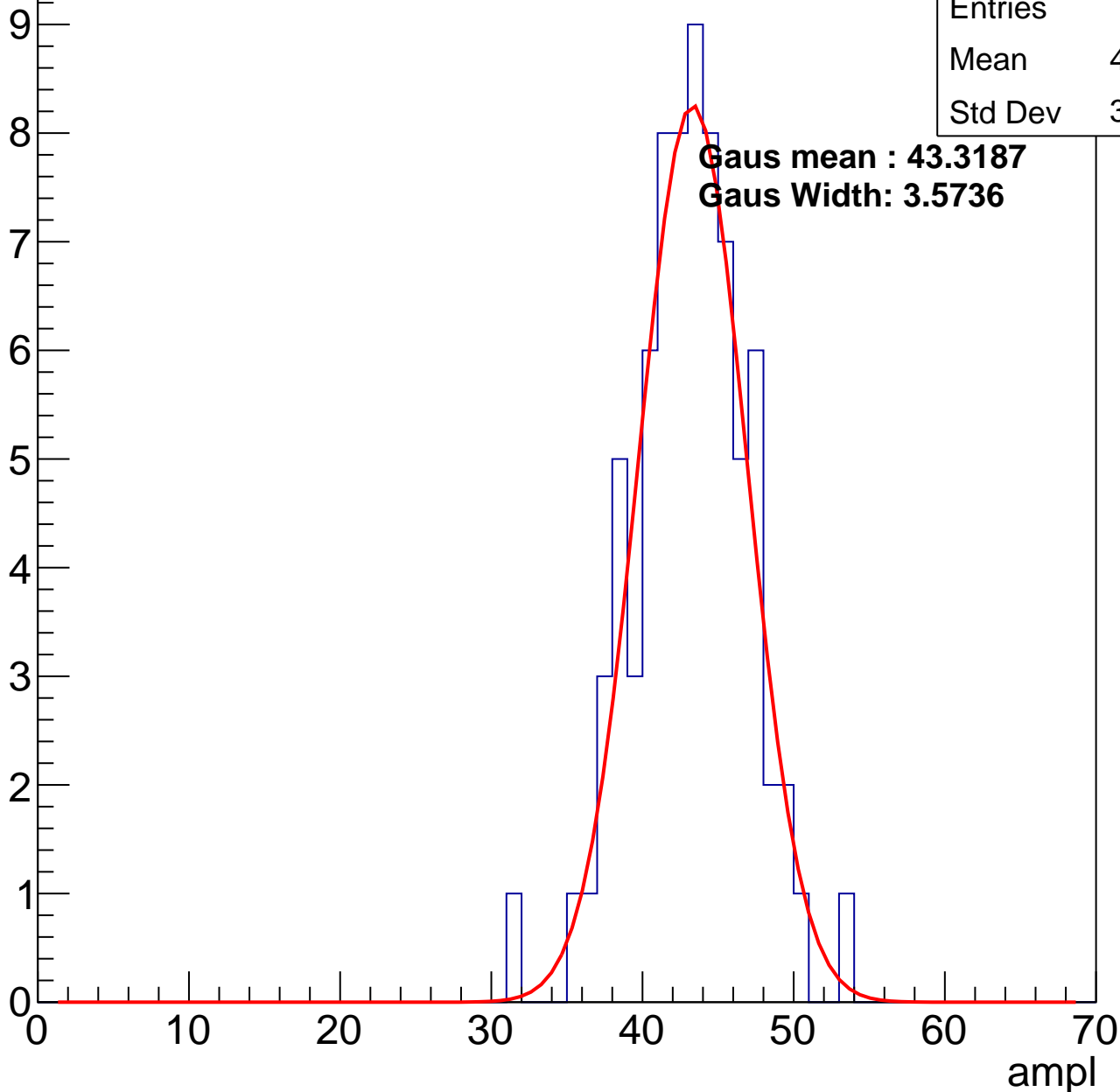
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	42.69
Std Dev	3.732

**Gaus mean : 43.3187**

**Gaus Width: 3.5736**

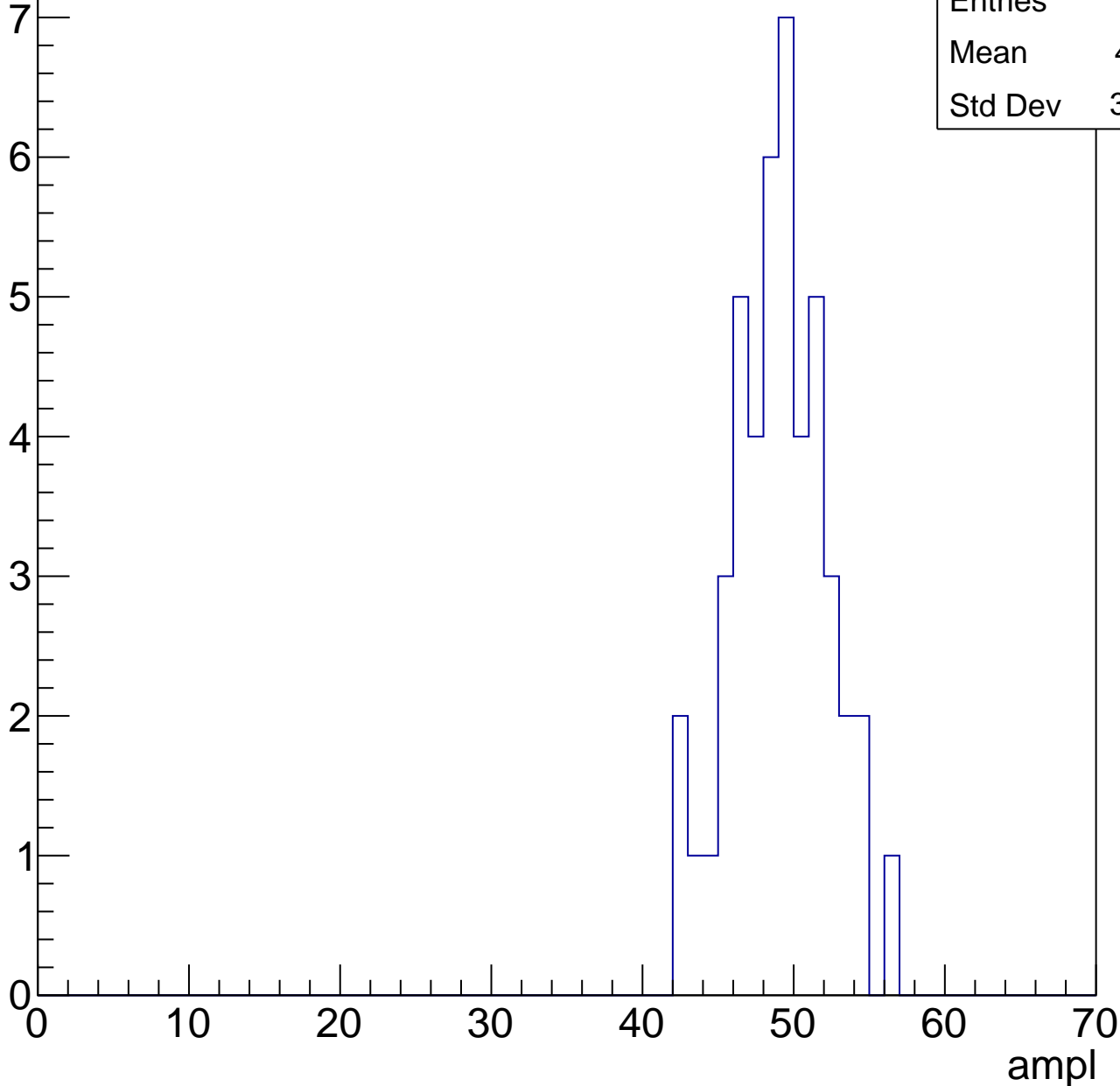


# B1L102S, U21-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	48.61
Std Dev	3.124

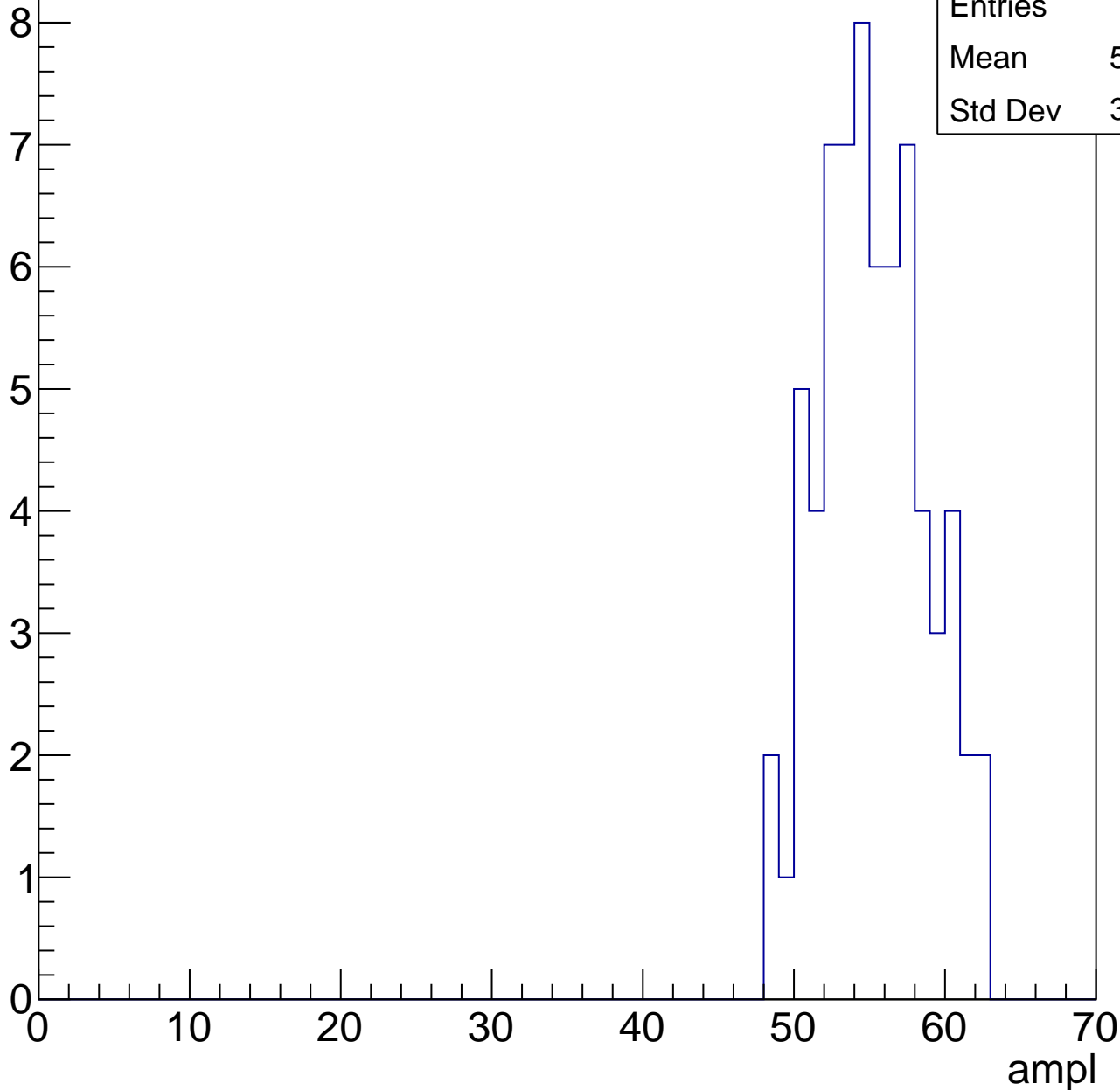


# B1L102S, U21-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	54.79
Std Dev	3.445

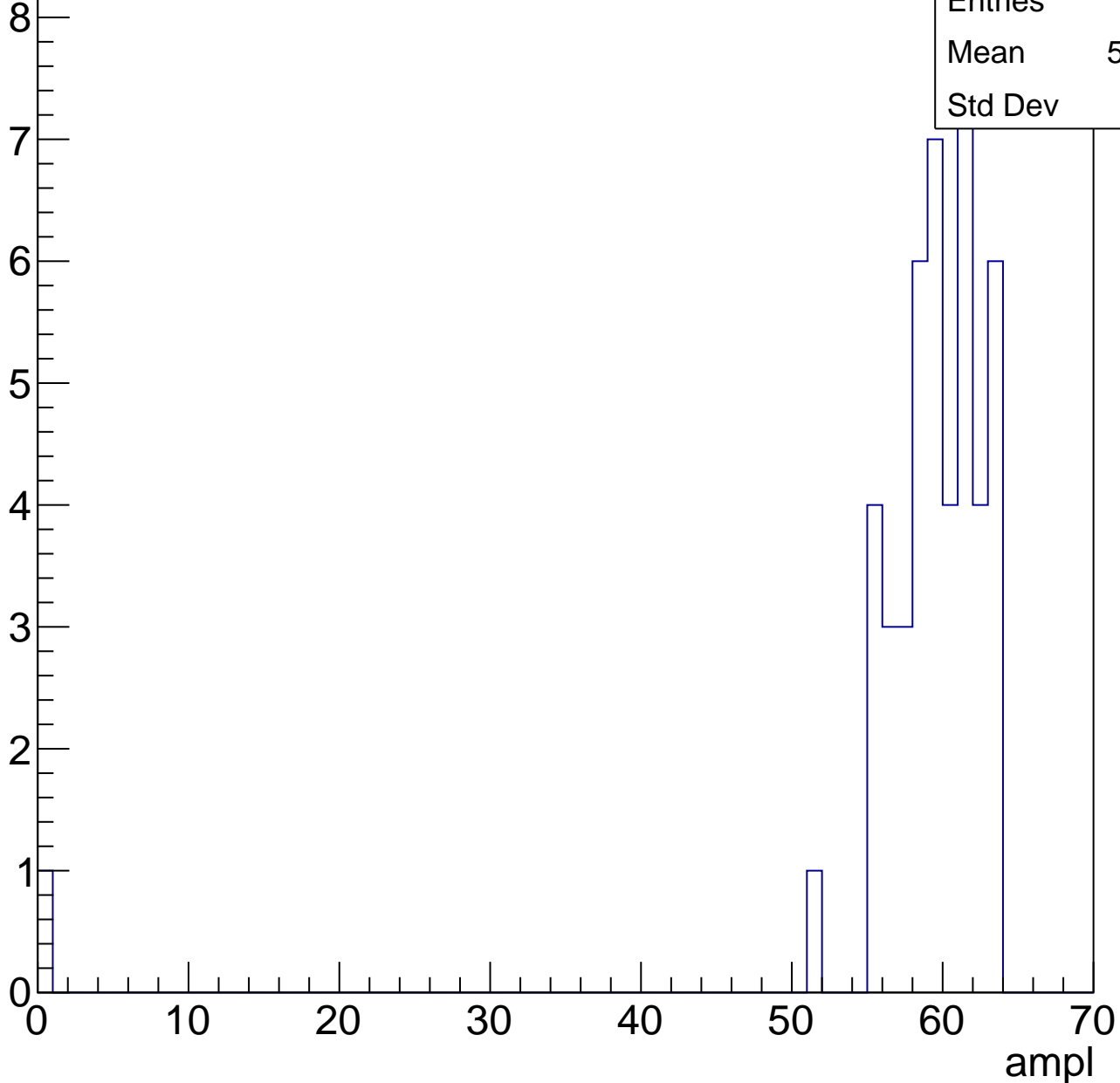


# B1L102S, U21-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

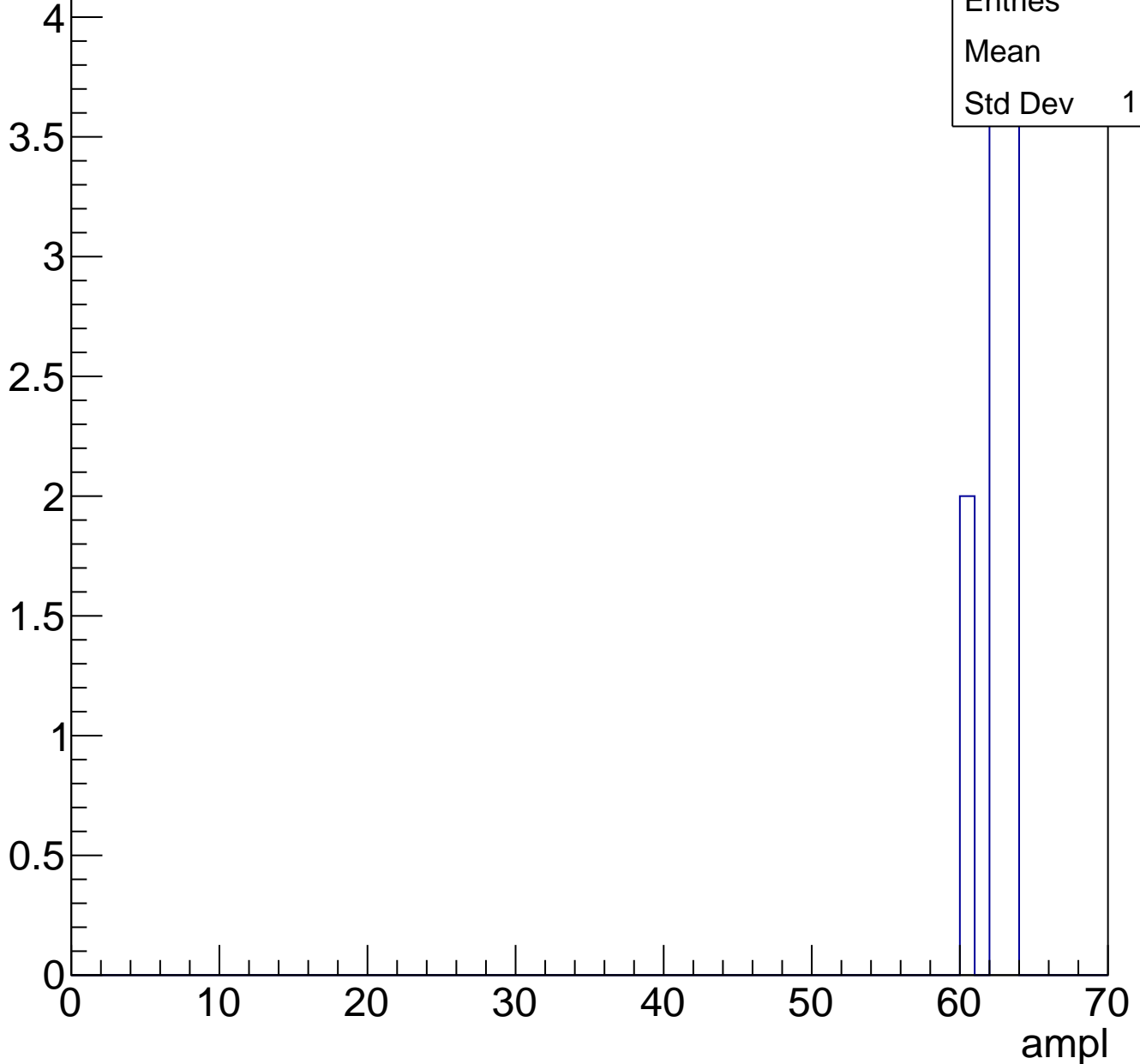
Entries	47
Mean	57.98
Std Dev	8.96



# B1L102S, U21-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

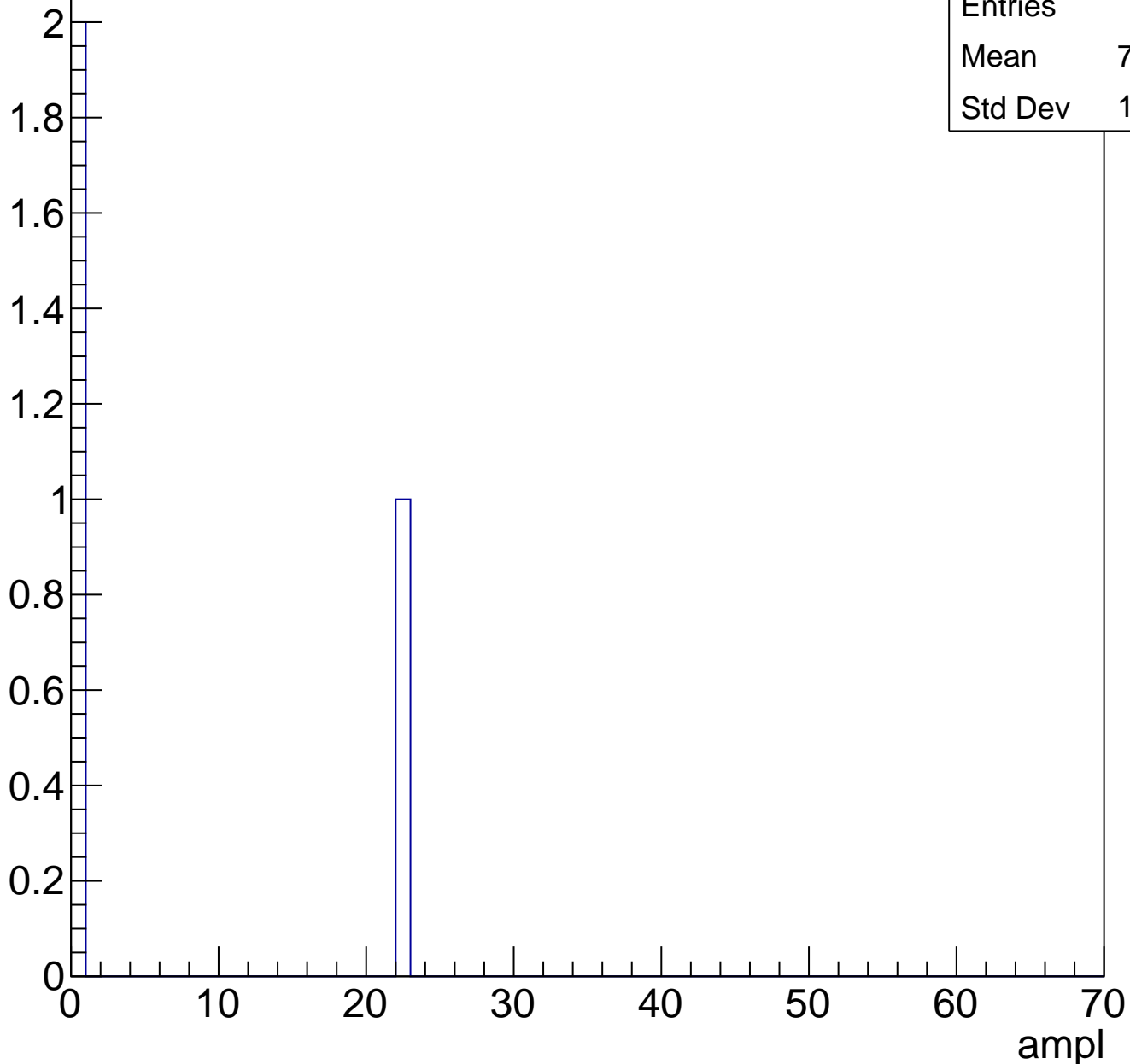




# B1L102S, U21-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	7.333
Std Dev	10.37

# B1L102S, U21-ch110, adc0

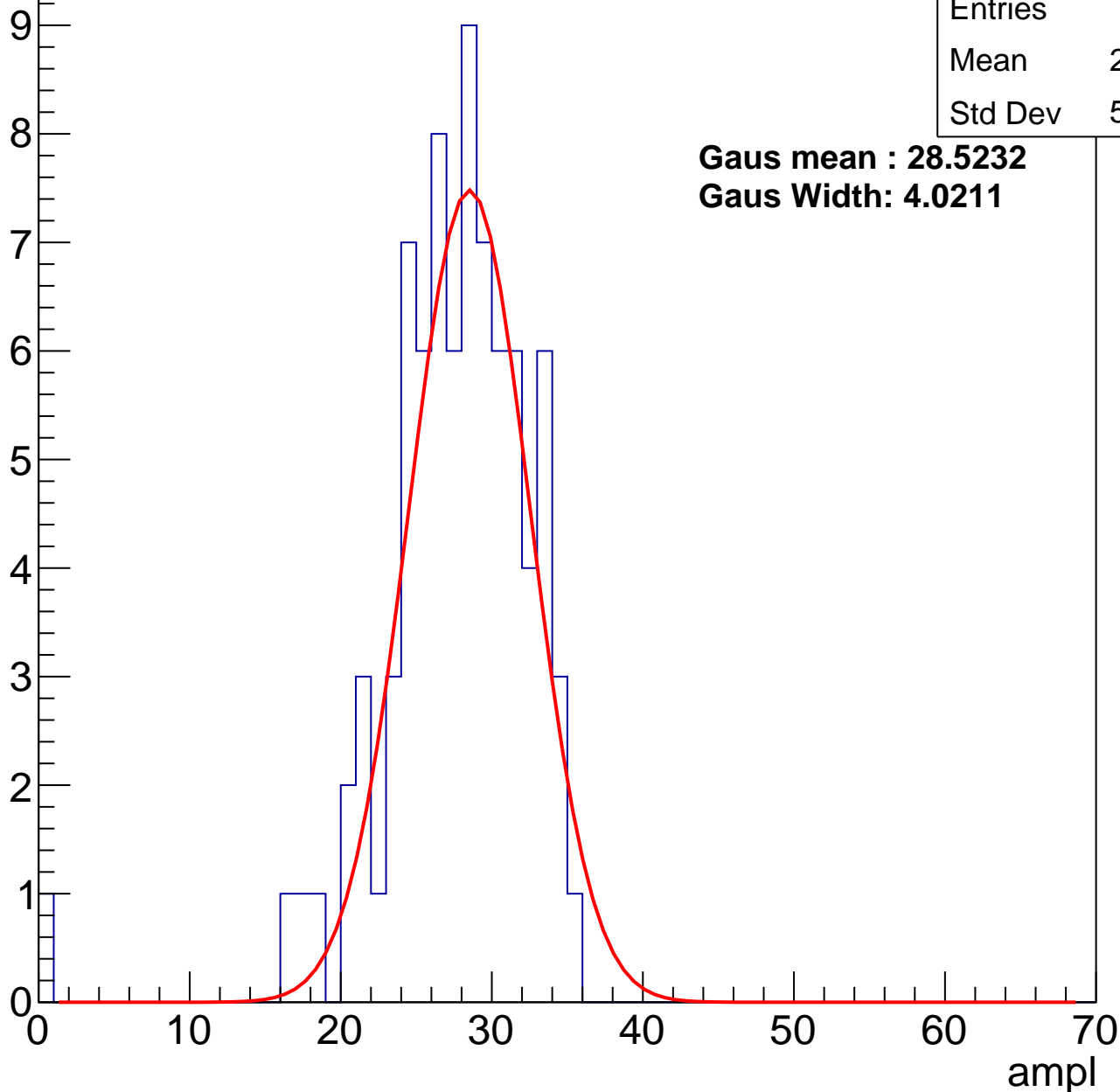
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	27.04
Std Dev	5.083

**Gaus mean : 28.5232**

**Gaus Width: 4.0211**



# B1L102S, U21-ch110, adc1

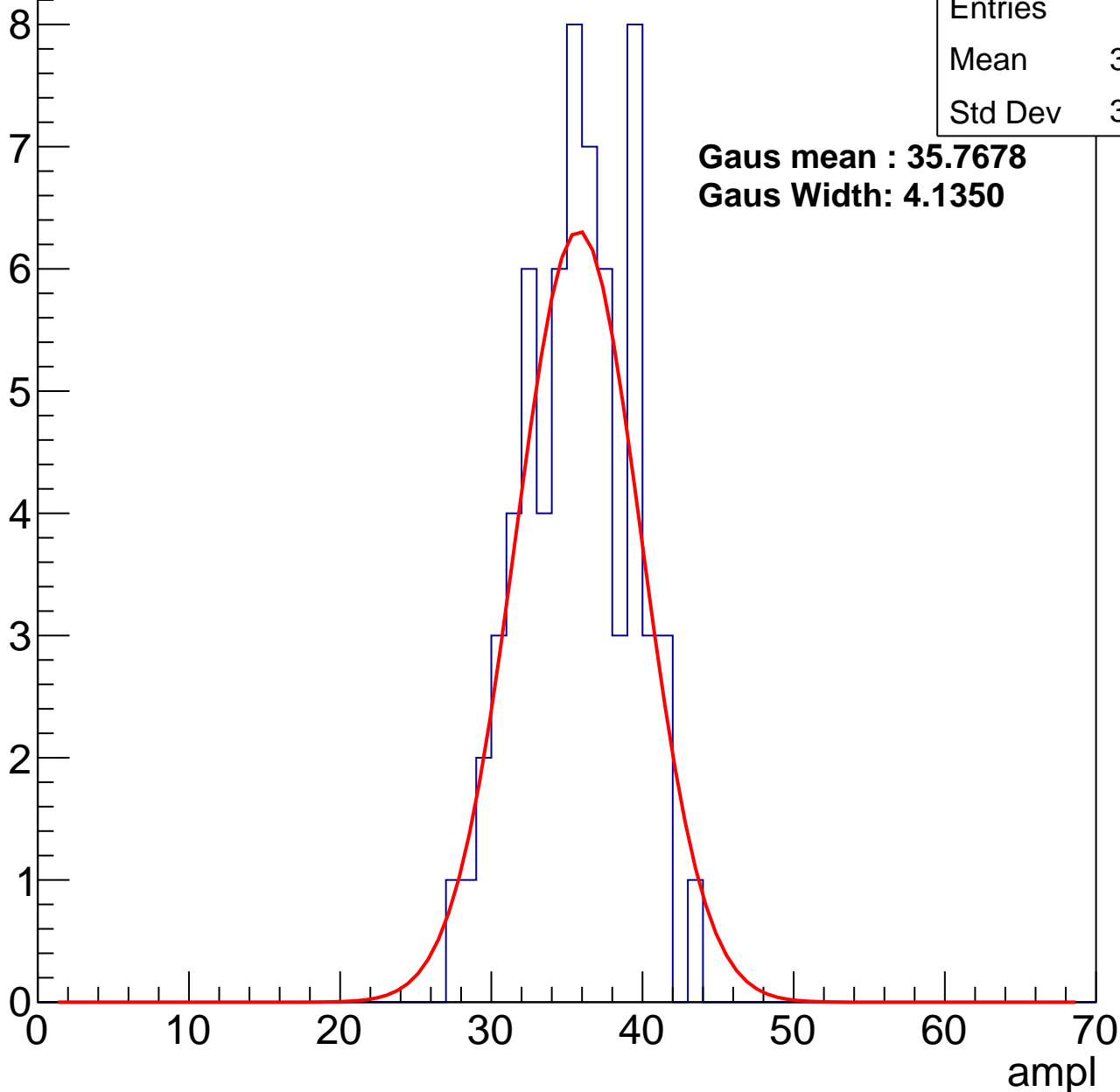
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	35.17
Std Dev	3.549

**Gaus mean : 35.7678**

**Gaus Width: 4.1350**



# B1L102S, U21-ch110, adc2

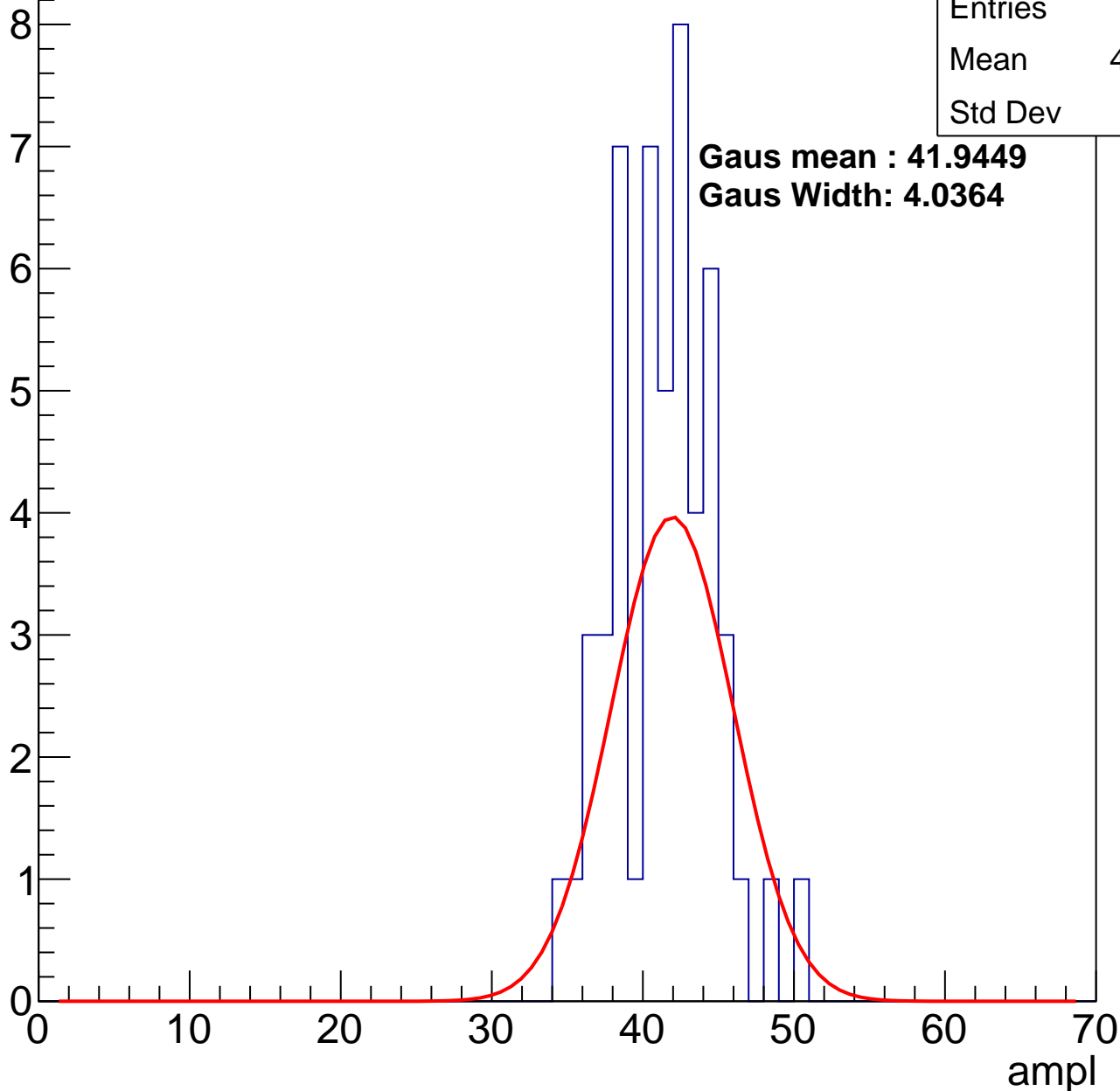
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	40.94
Std Dev	3.29

**Gaus mean : 41.9449**

**Gaus Width: 4.0364**

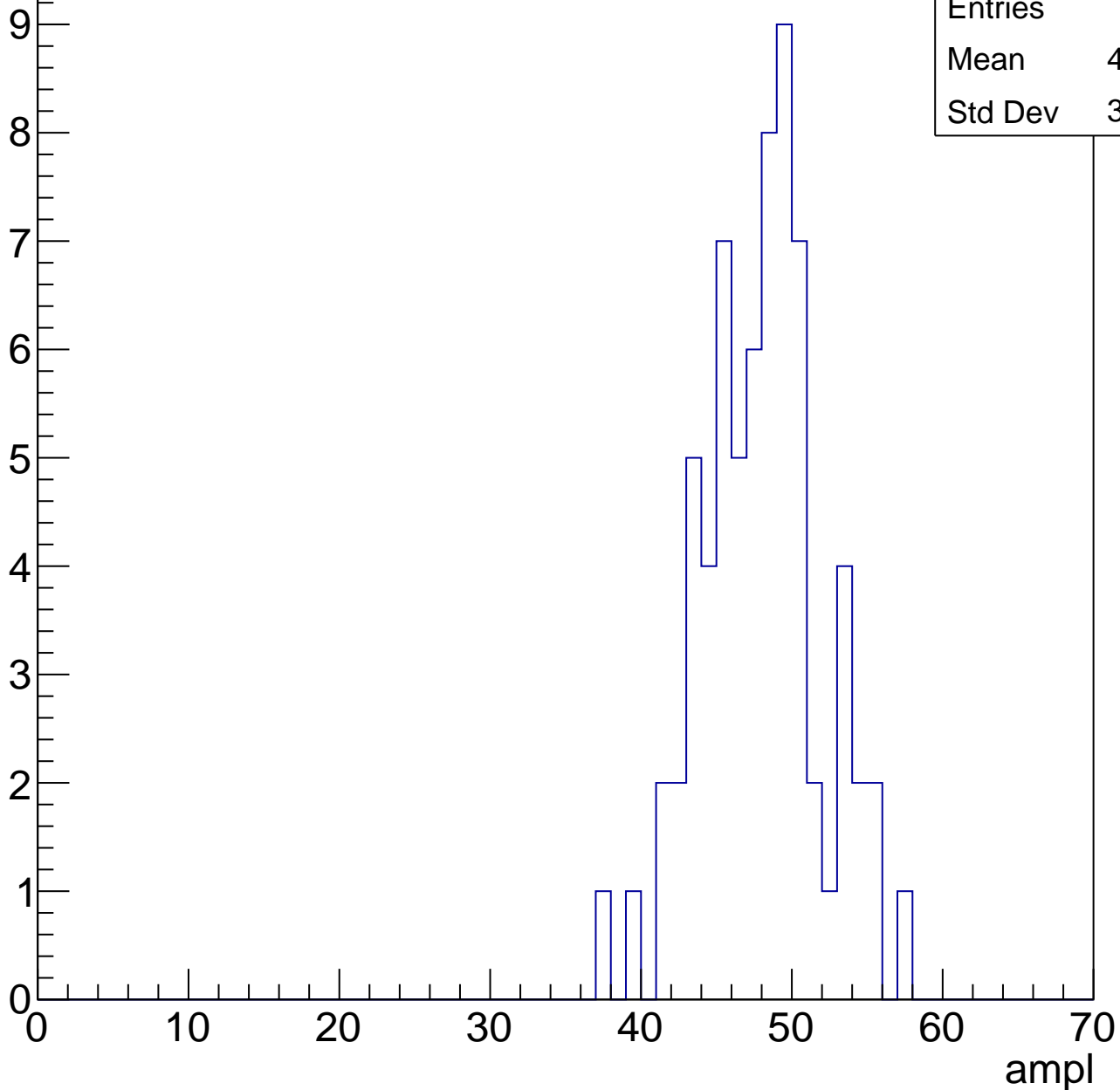


# B1L102S, U21-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	47.48
Std Dev	3.907

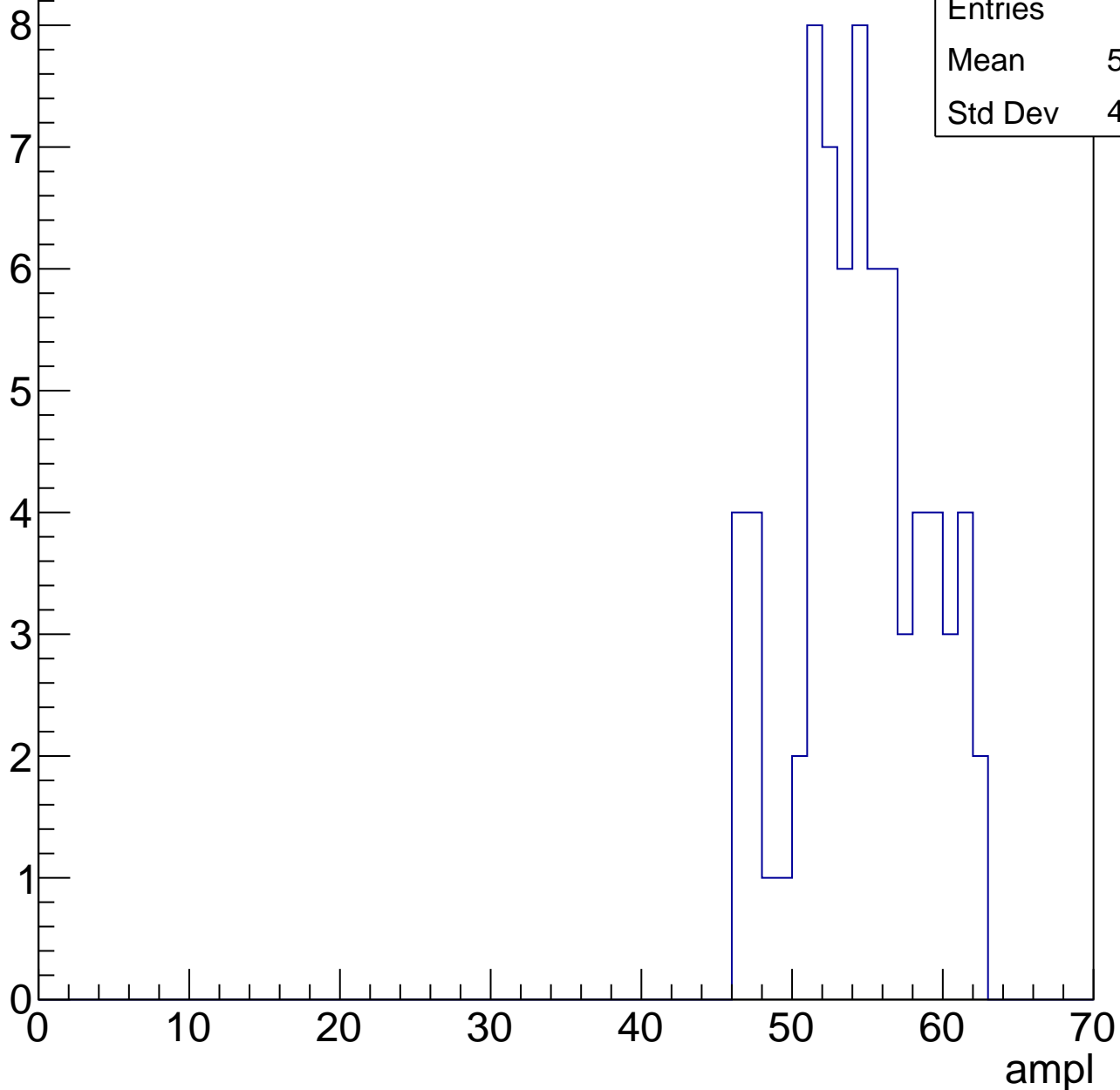


# B1L102S, U21-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	54.03
Std Dev	4.226

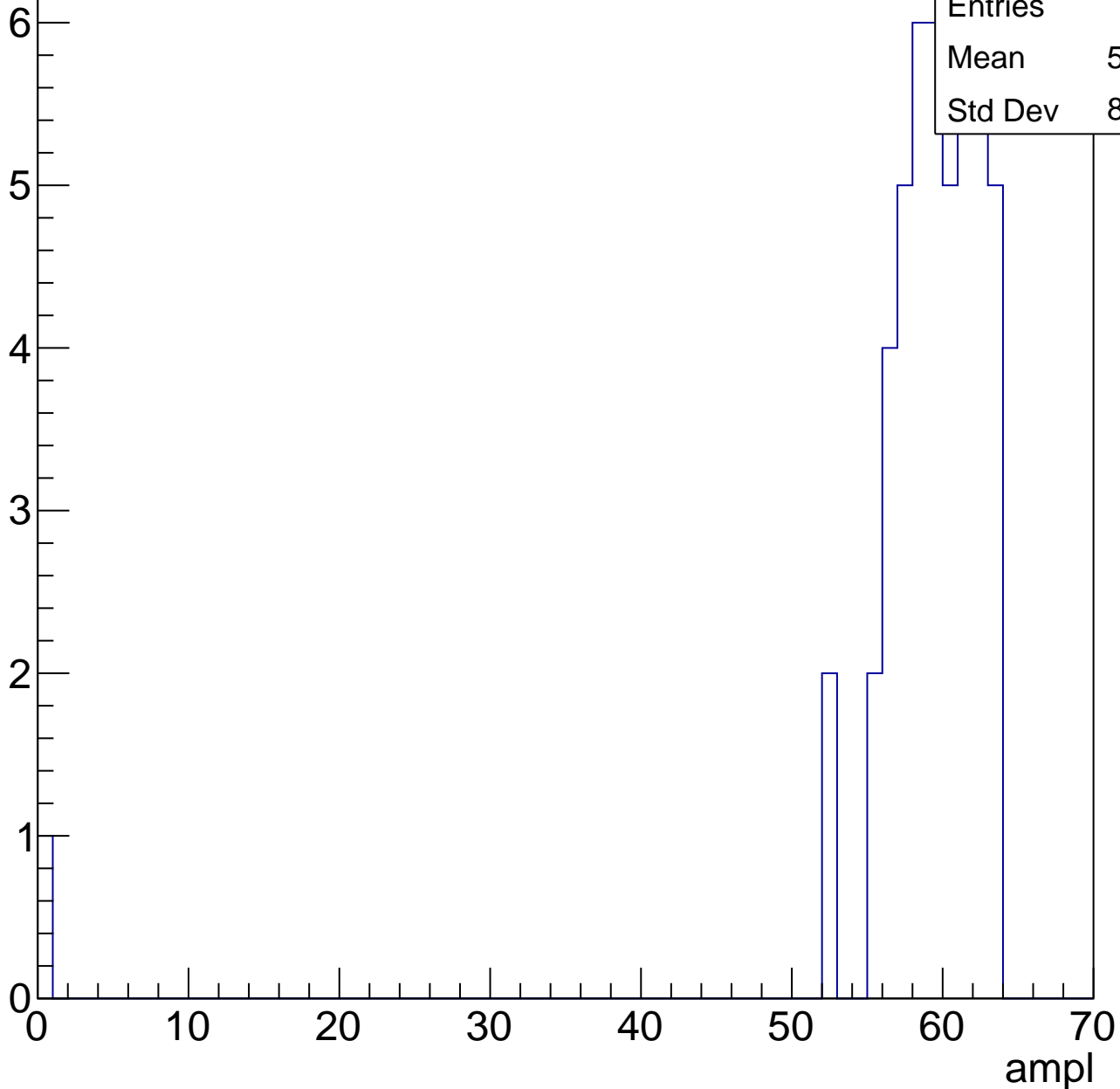


# B1L102S, U21-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	57.88
Std Dev	8.869

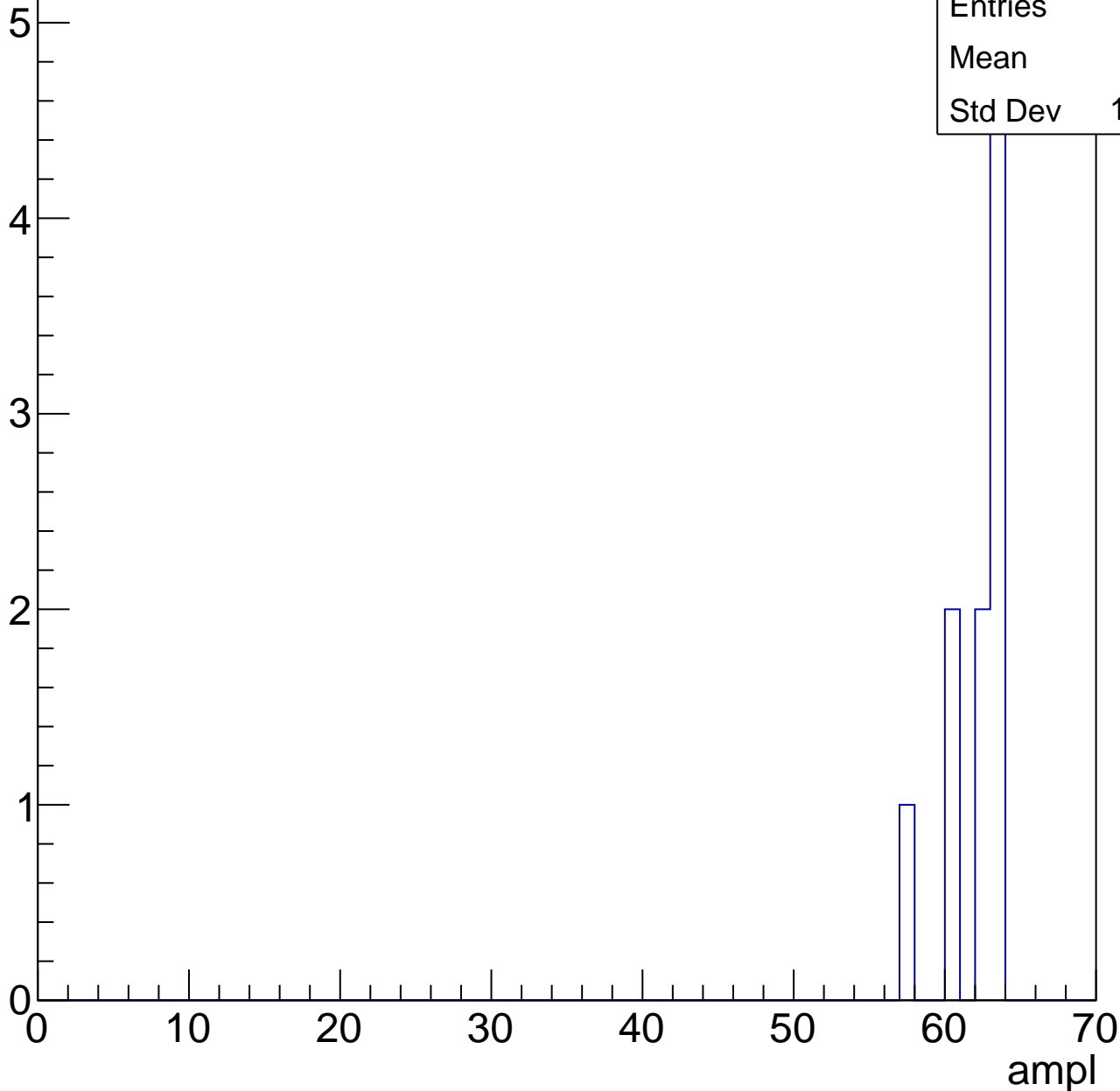


# B1L102S, U21-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	10
Mean	61.6
Std Dev	1.908





# B1L102S, U21-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch111, adc0

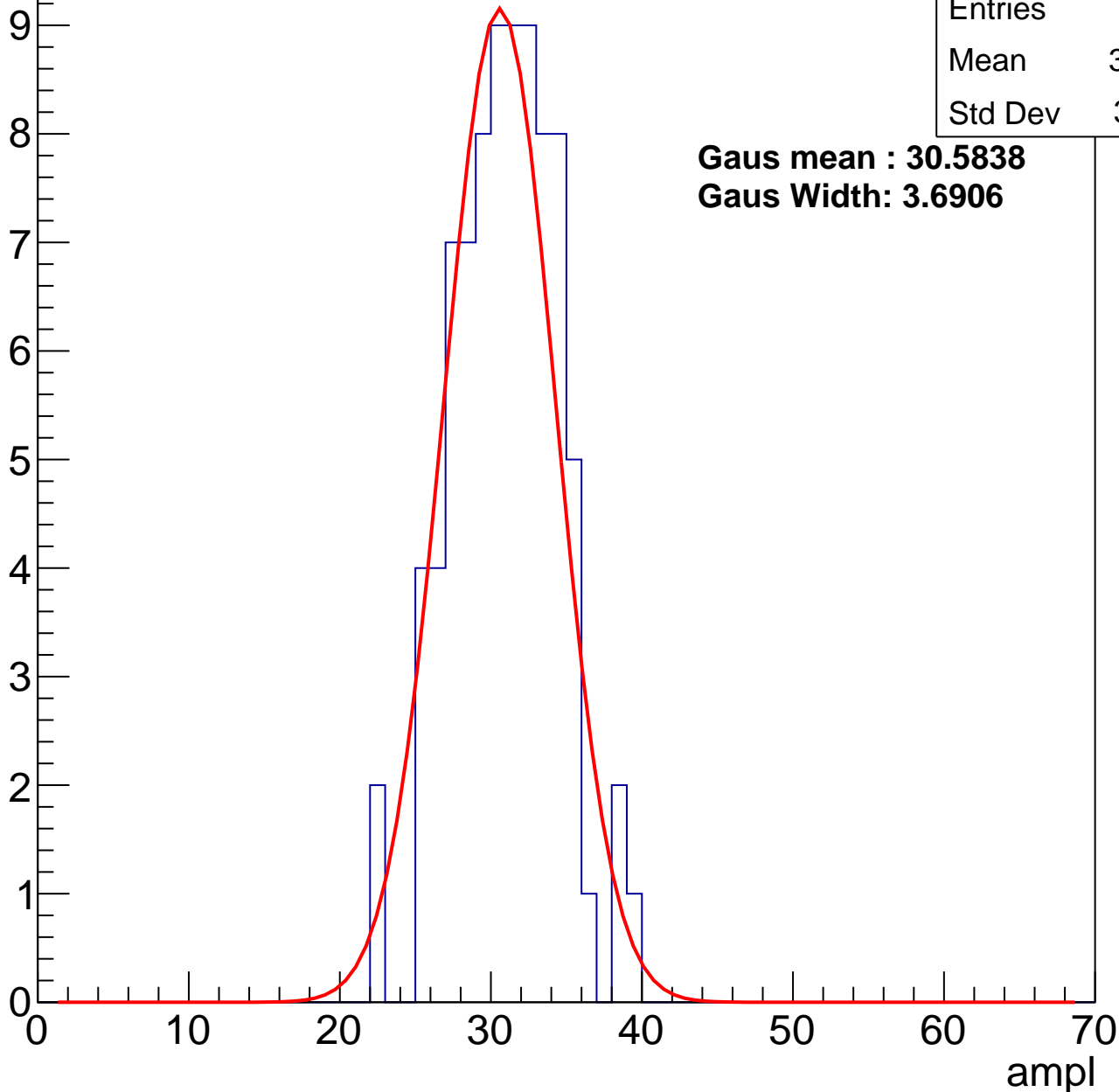
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	30.52
Std Dev	3.421

**Gaus mean : 30.5838**

**Gaus Width: 3.6906**



# B1L102S, U21-ch111, adc1

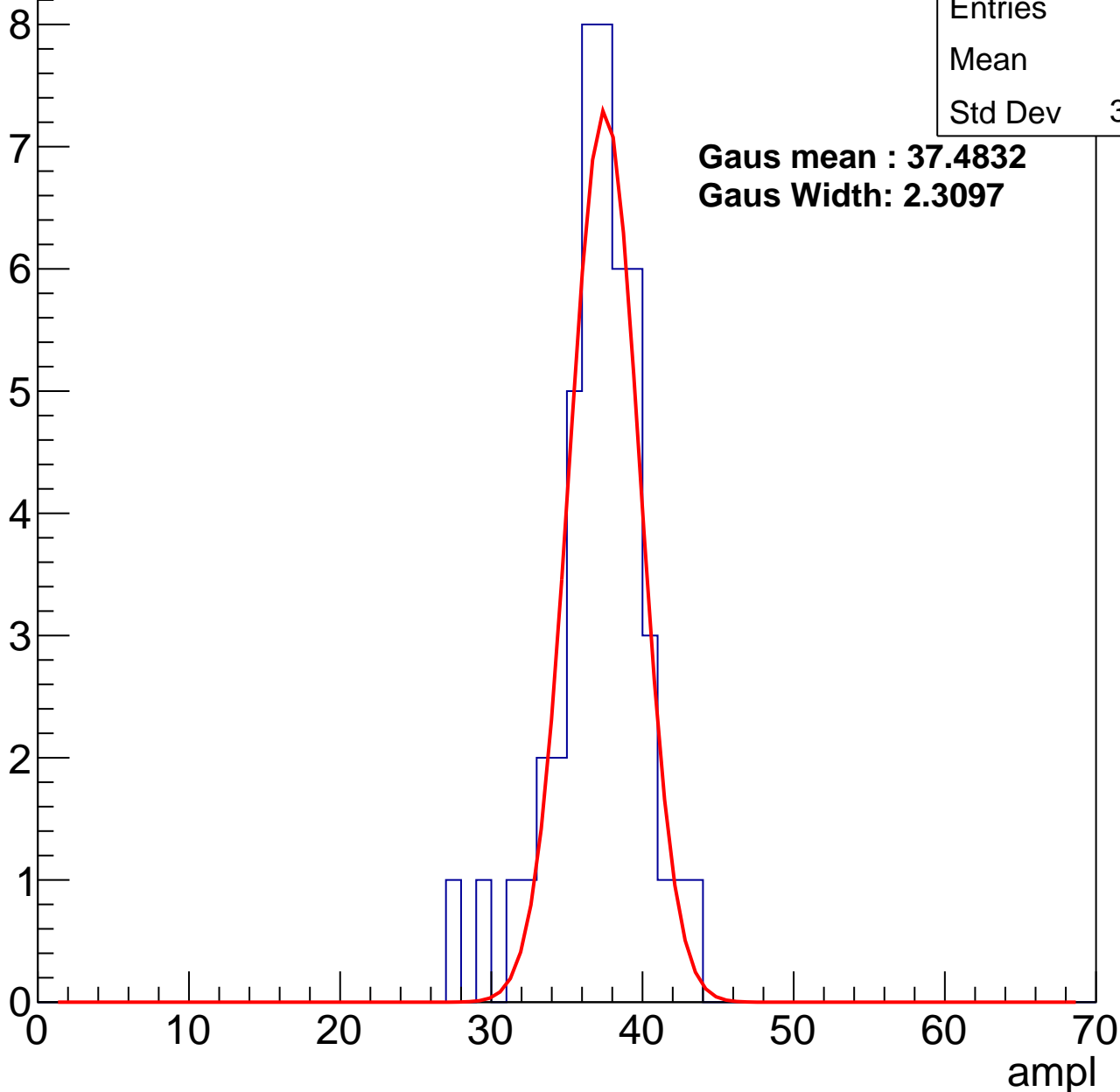
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	36.6
Std Dev	3.022

**Gaus mean : 37.4832**

**Gaus Width: 2.3097**



# B1L102S, U21-ch111, adc2

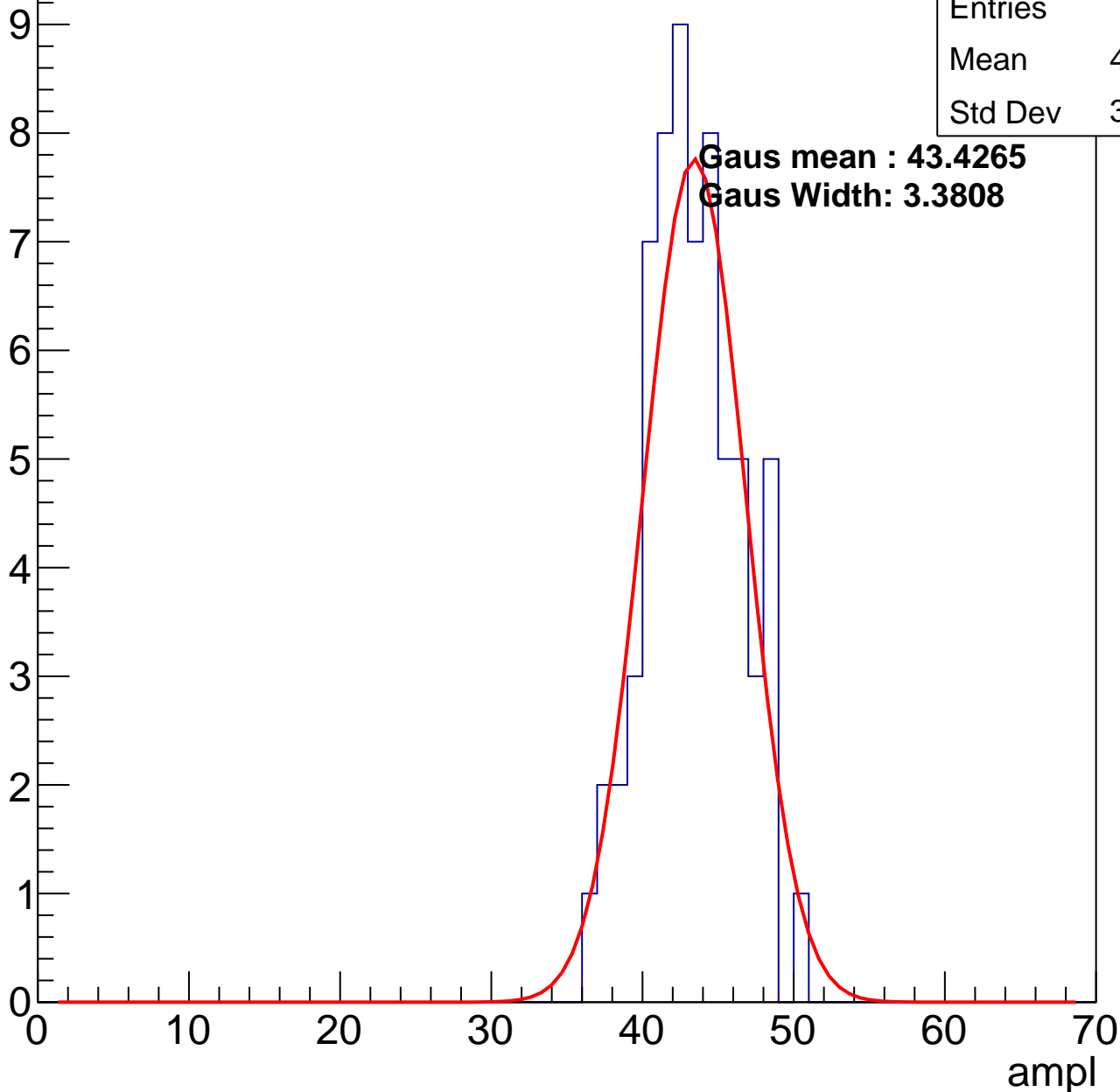
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	42.85
Std Dev	3.056

**Gaus mean : 43.4265**

**Gaus Width: 3.3808**

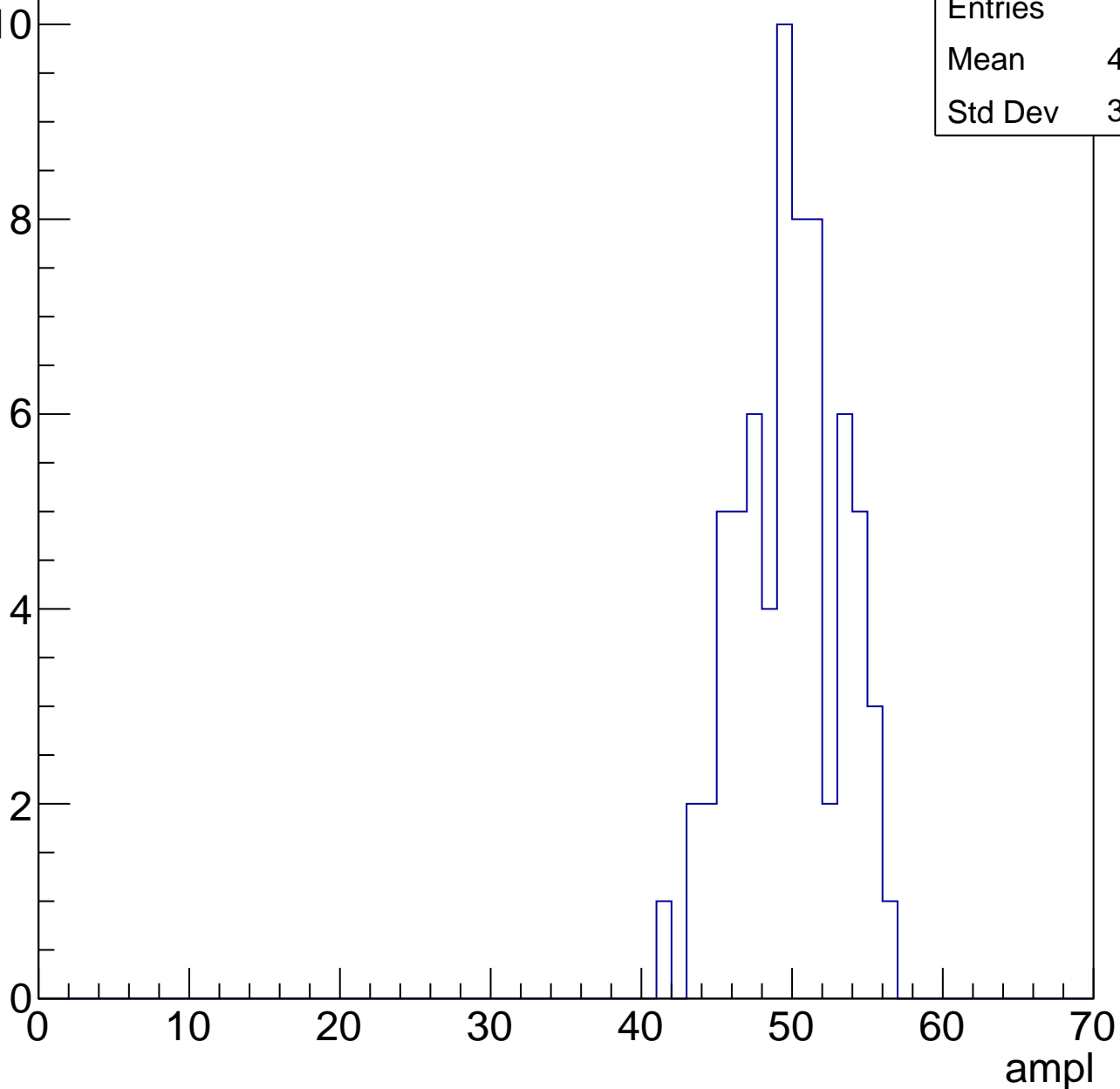


# B1L102S, U21-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	49.34
Std Dev	3.359

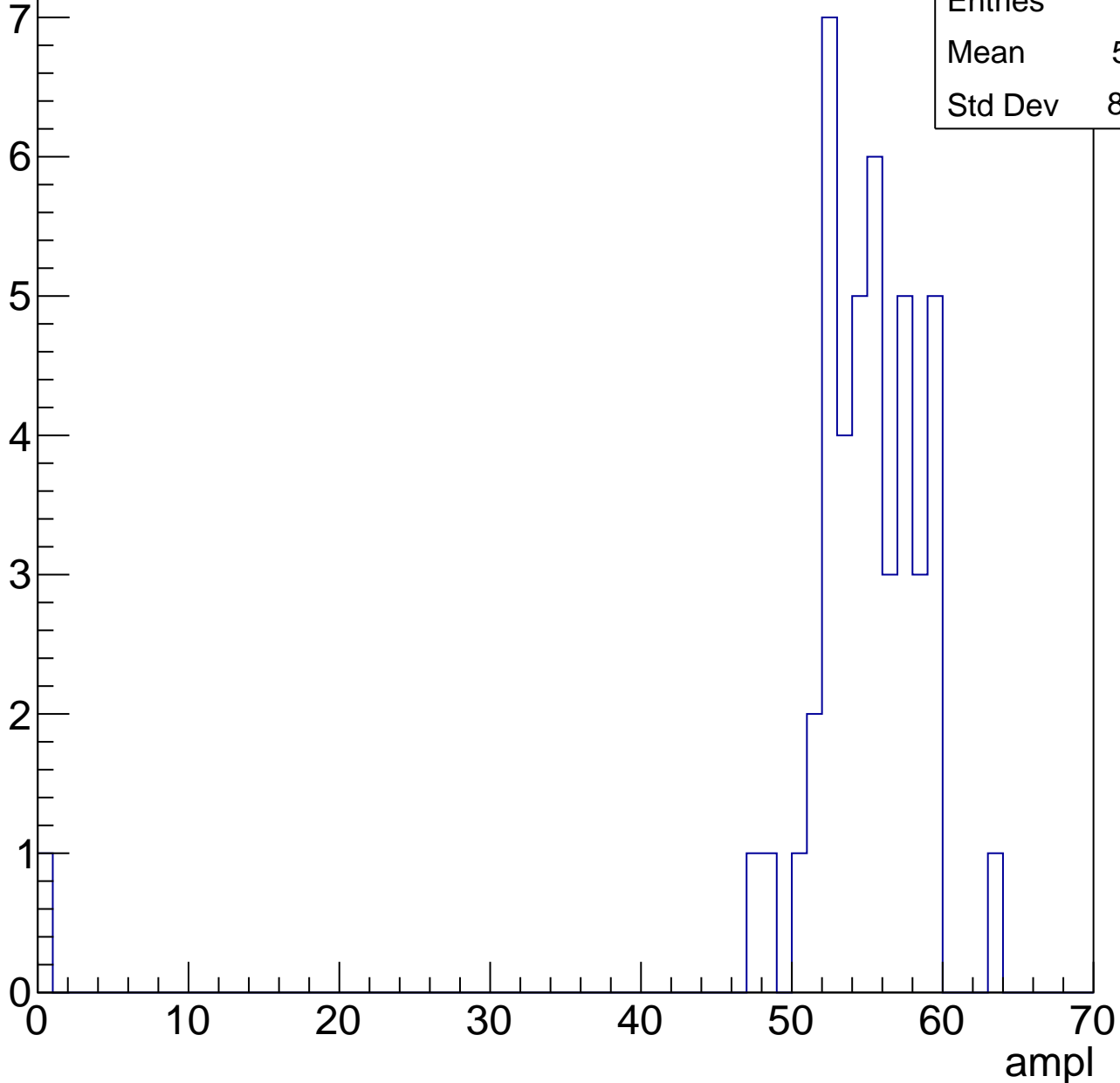


# B1L102S, U21-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	53.51
Std Dev	8.658

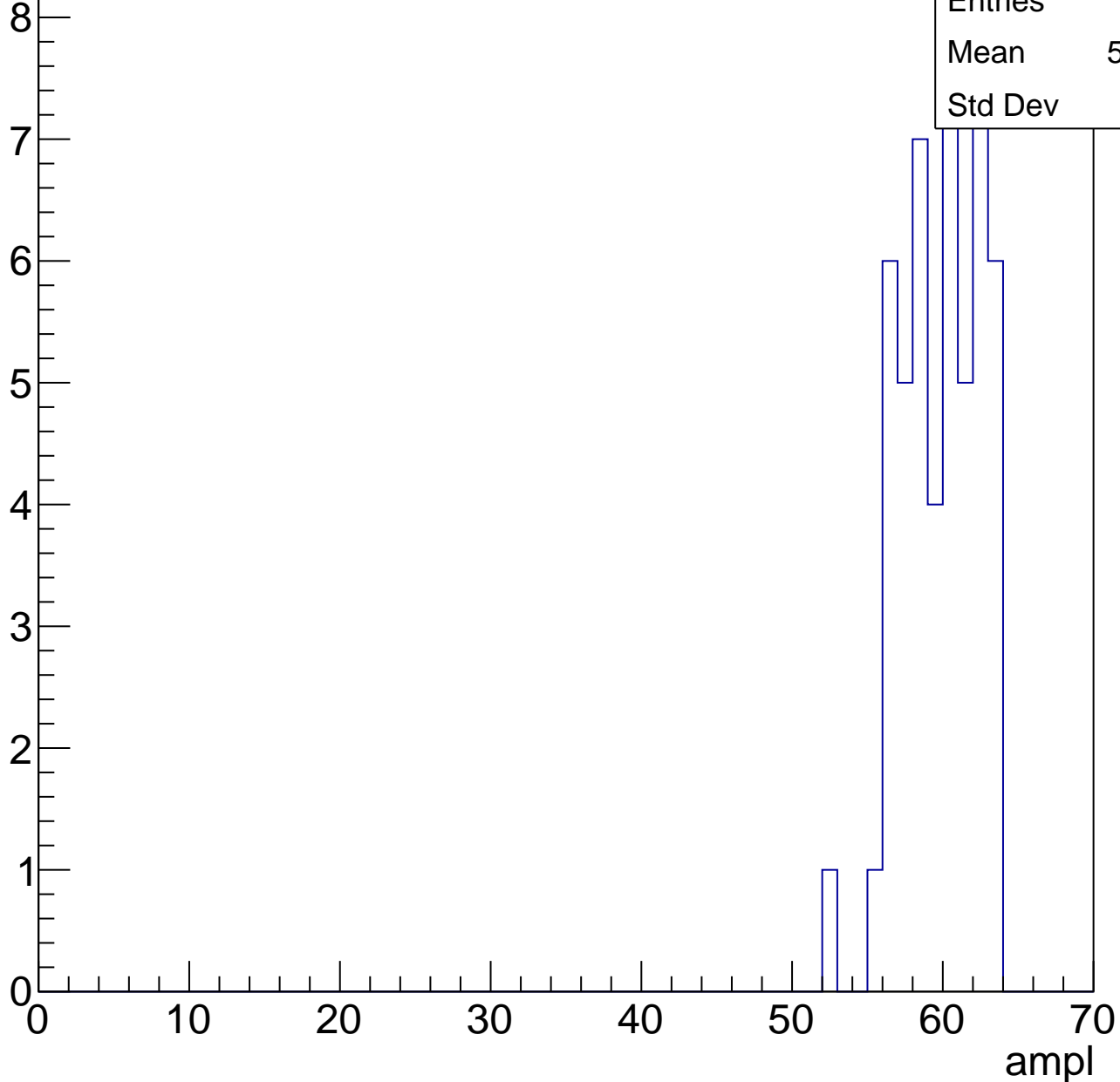


# B1L102S, U21-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

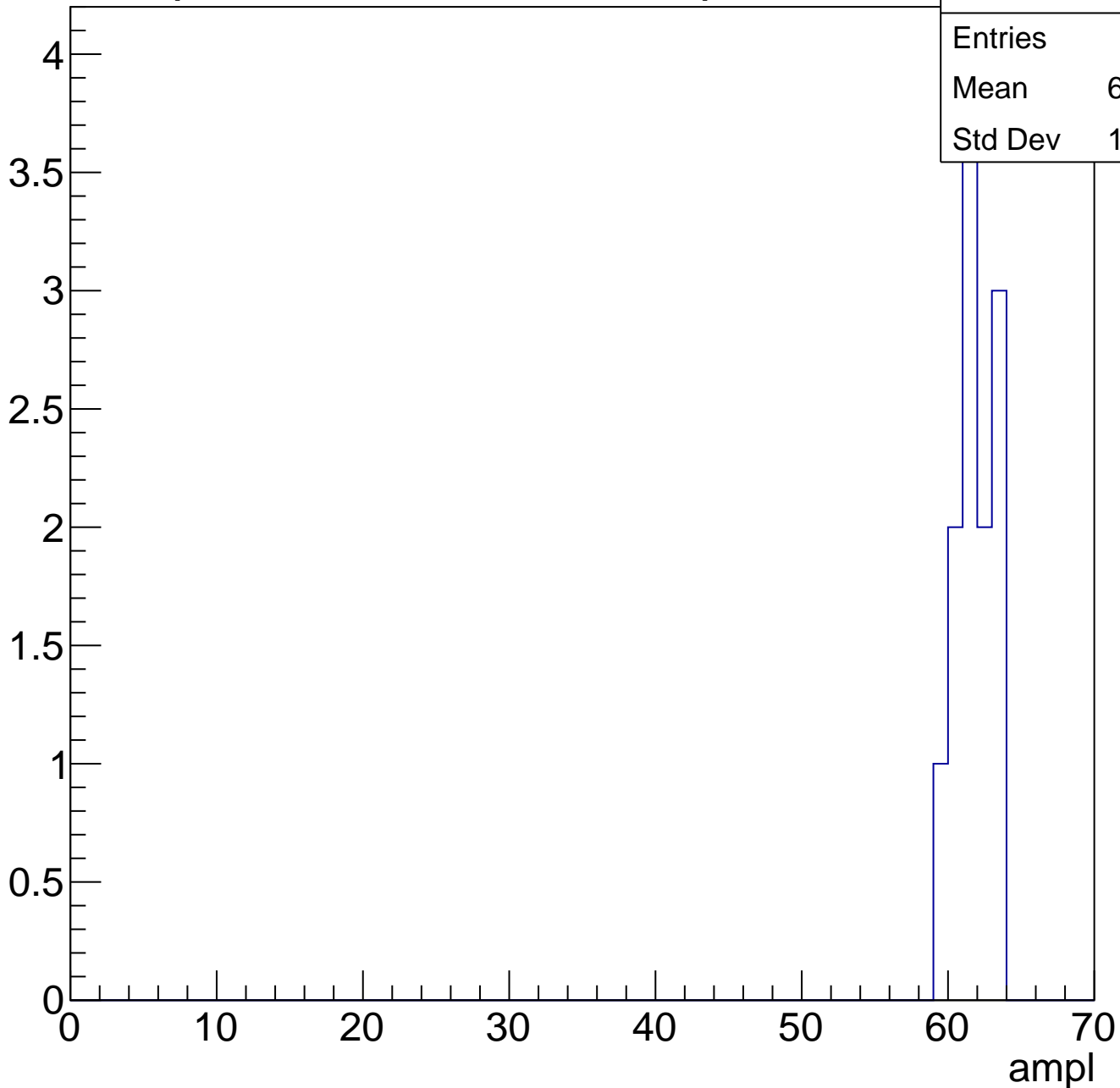
Entries	51
Mean	59.39
Std Dev	2.56



# B1L102S, U21-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

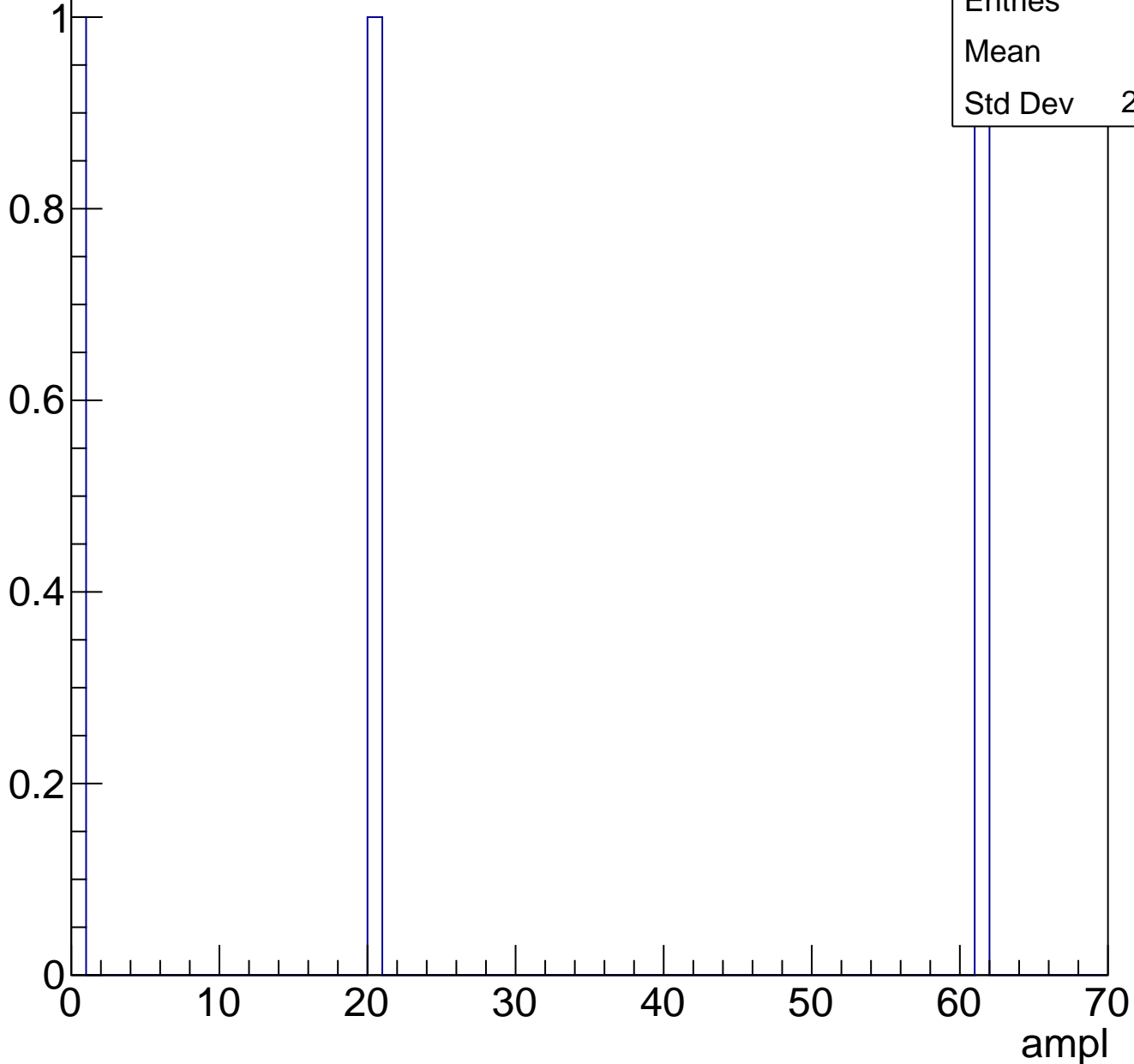




# B1L102S, U21-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	27
Std Dev	25.39

# B1L102S, U21-ch112, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	76
Mean	28.39
Std Dev	3.849

**Gaus mean : 28.4608**

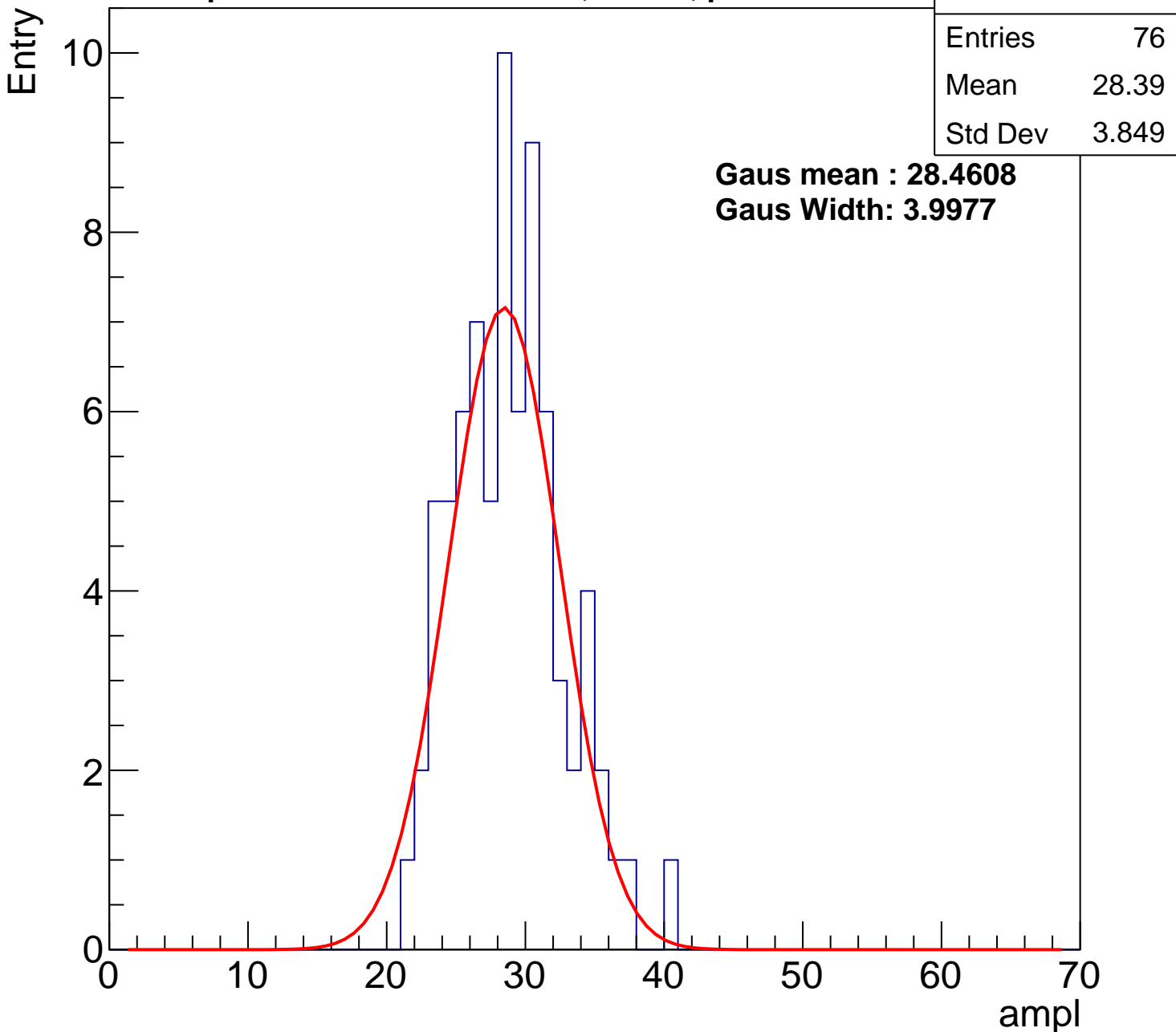
**Gaus Width: 3.9977**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U21-ch112, adc1

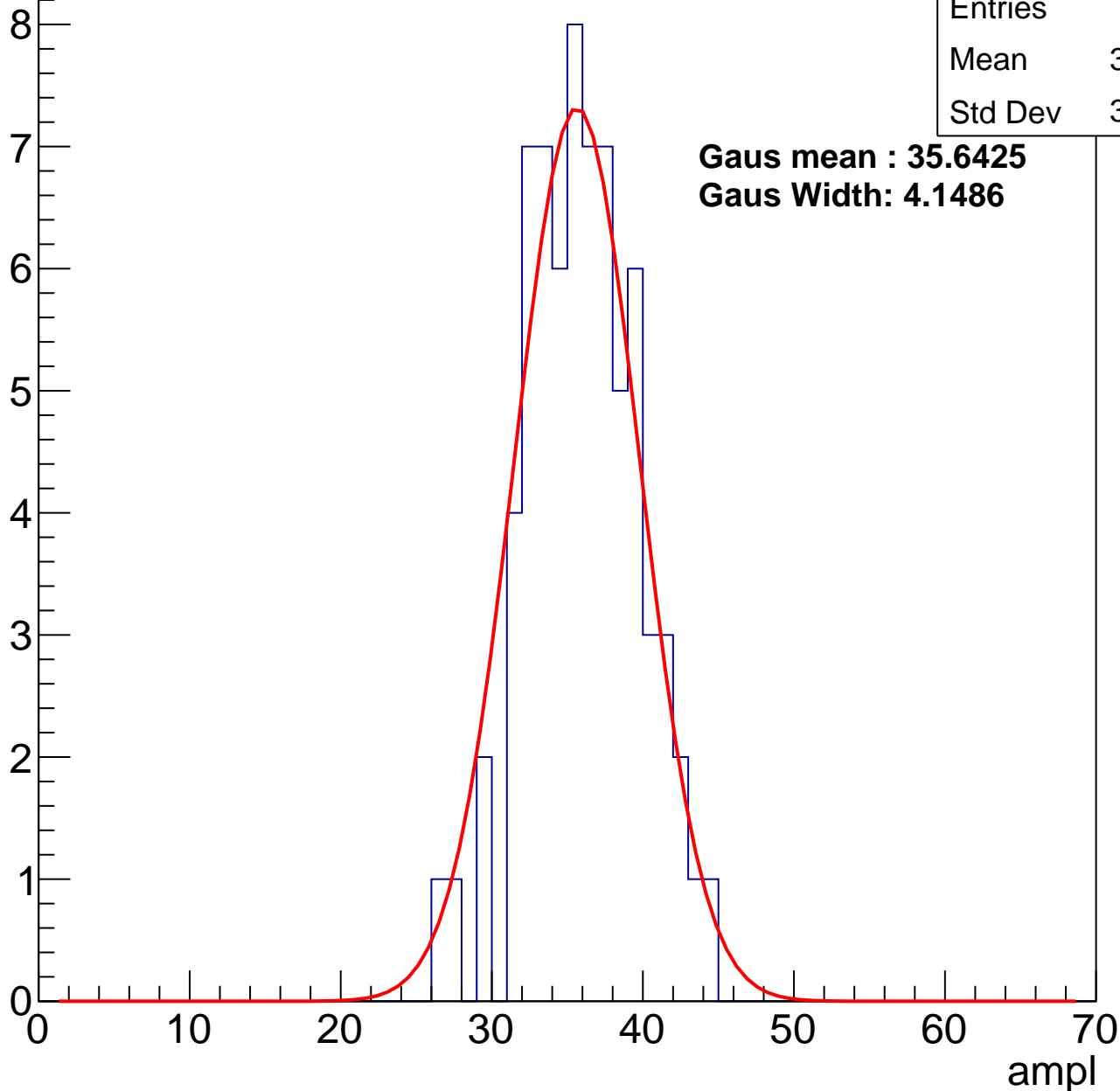
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	35.54
Std Dev	3.676

**Gaus mean : 35.6425**

**Gaus Width: 4.1486**



# B1L102S, U21-ch112, adc2

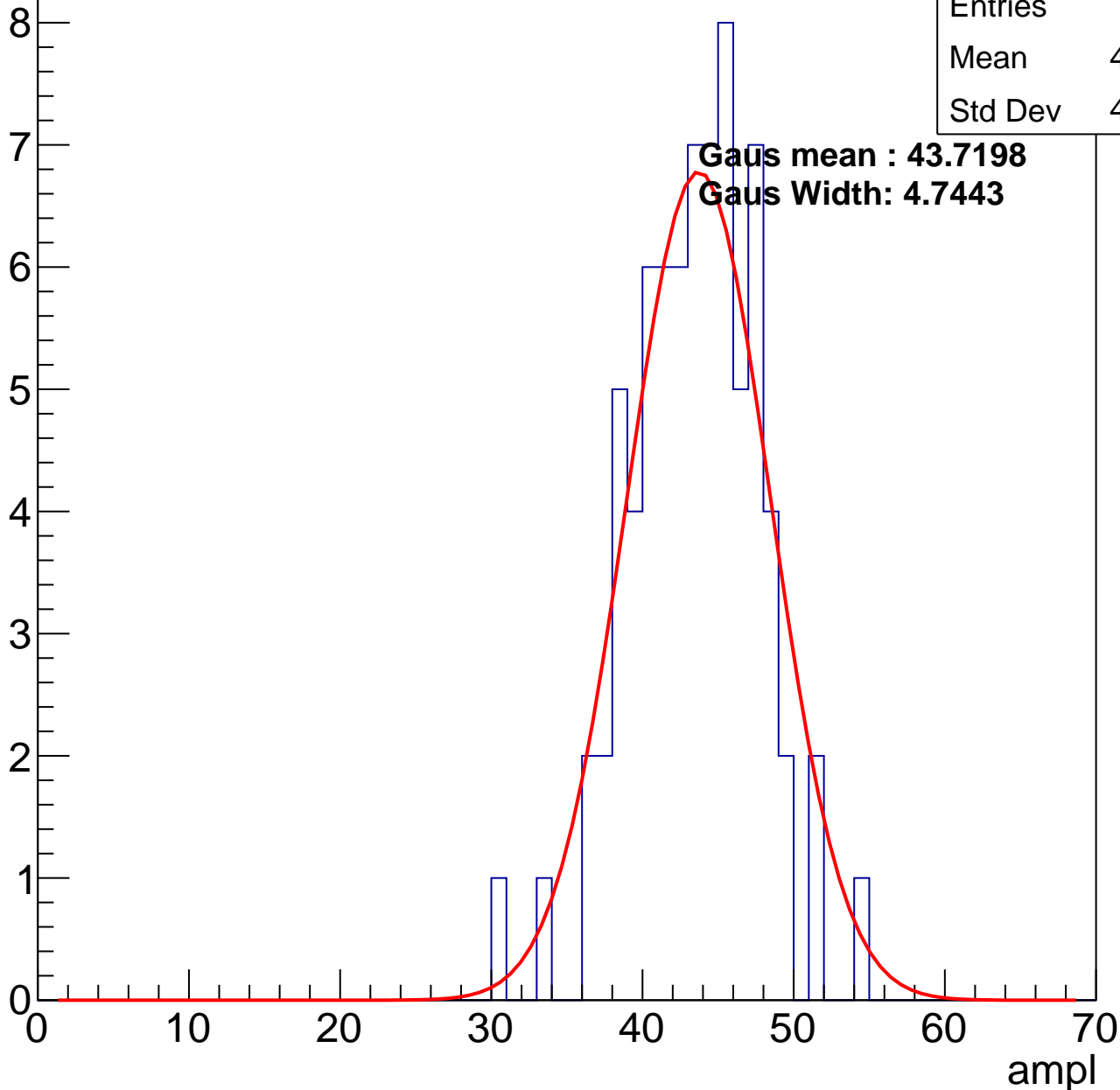
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	42.99
Std Dev	4.182

**Gaus mean : 43.7198**

**Gaus Width: 4.7443**

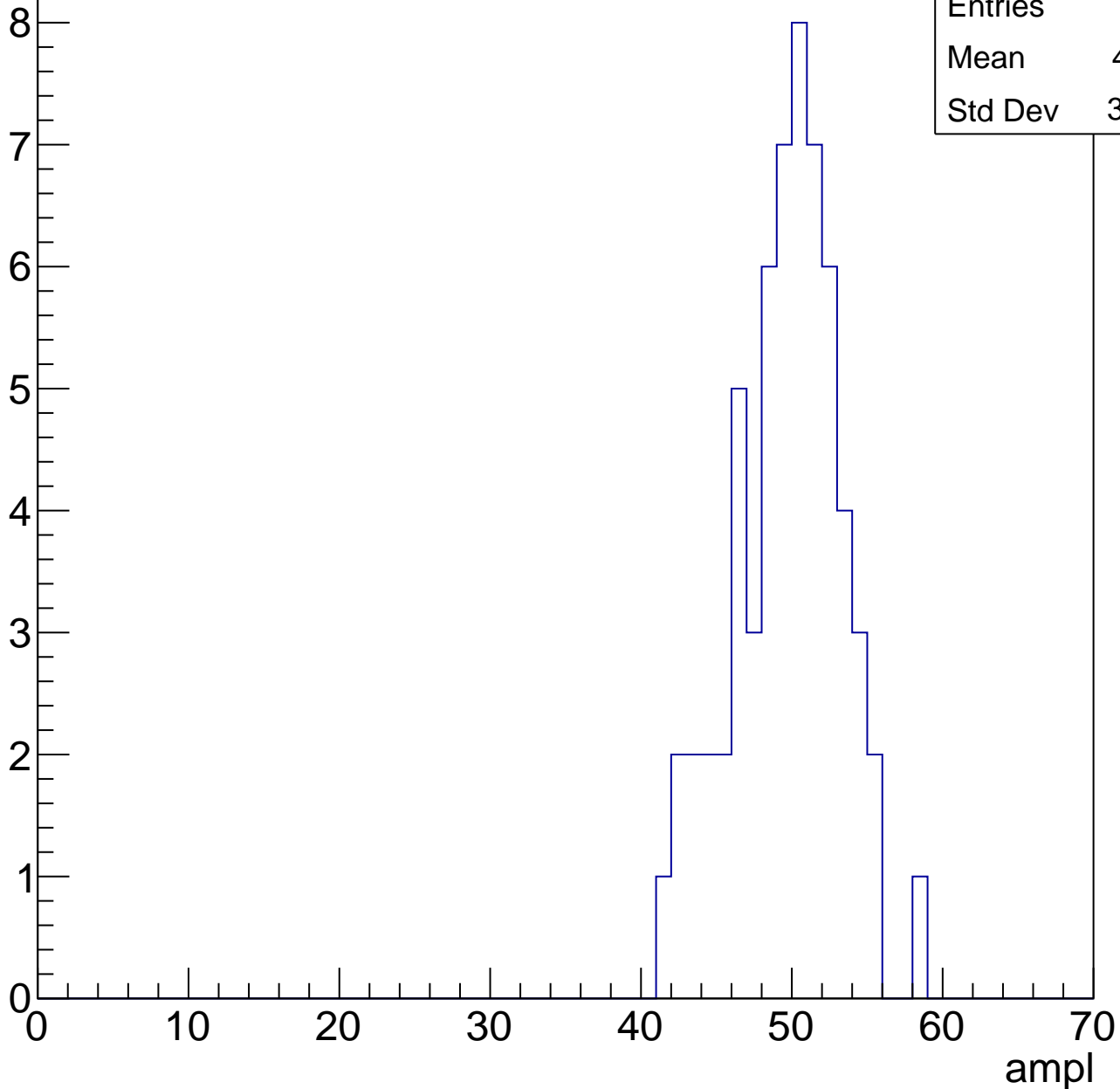


# B1L102S, U21-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	49.21
Std Dev	3.526

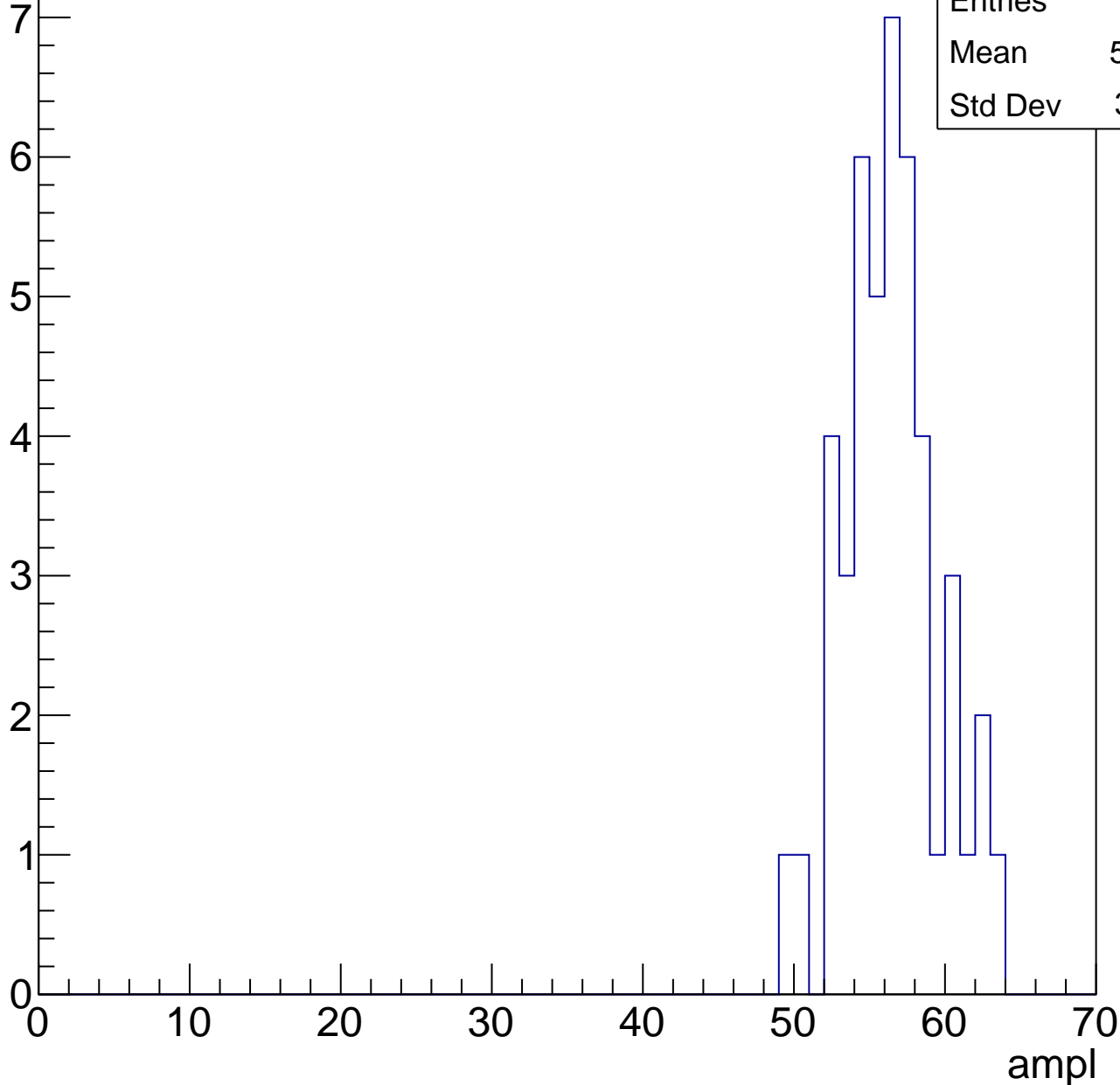


# B1L102S, U21-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	55.96
Std Dev	3.091

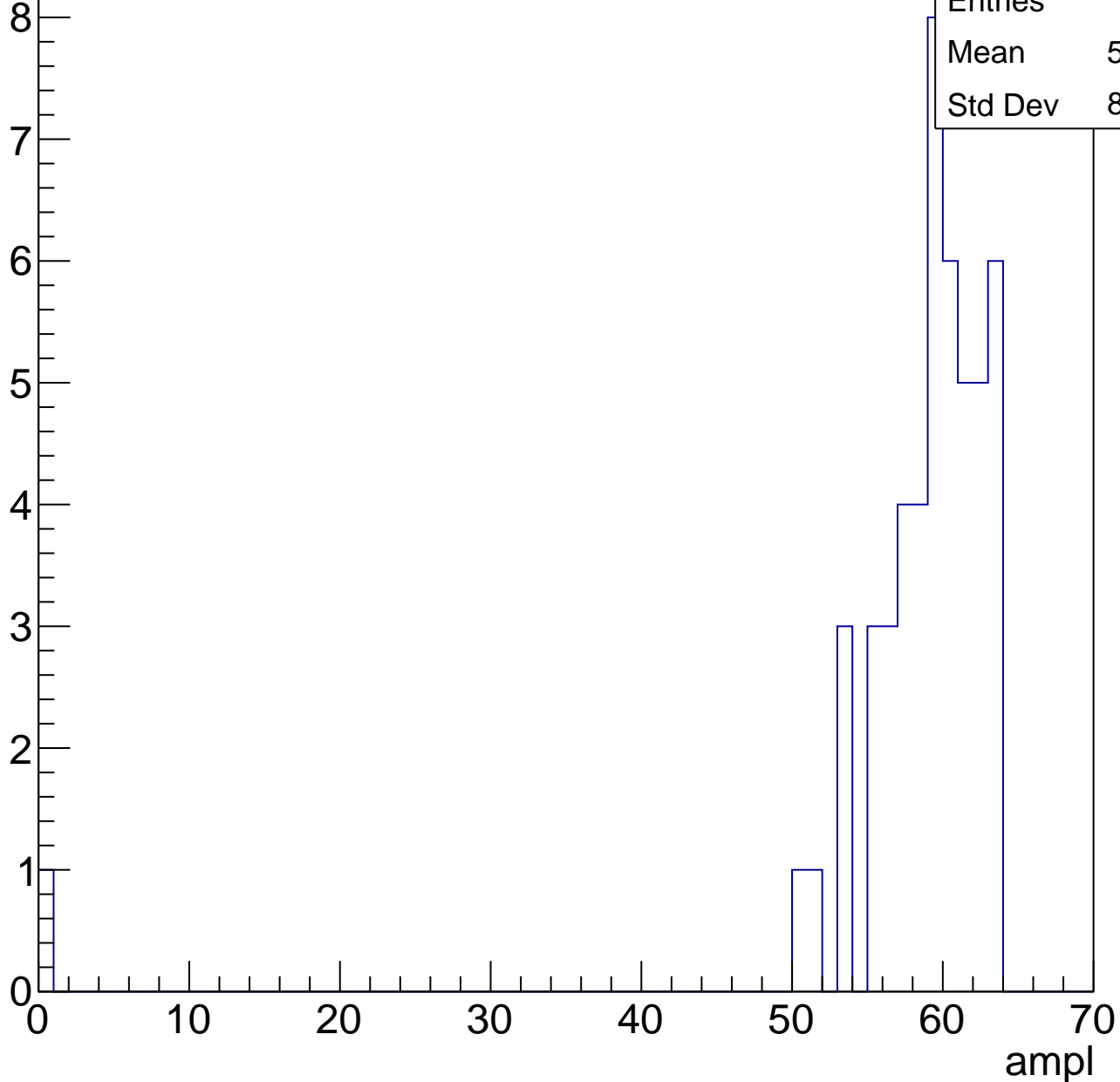


# B1L102S, U21-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

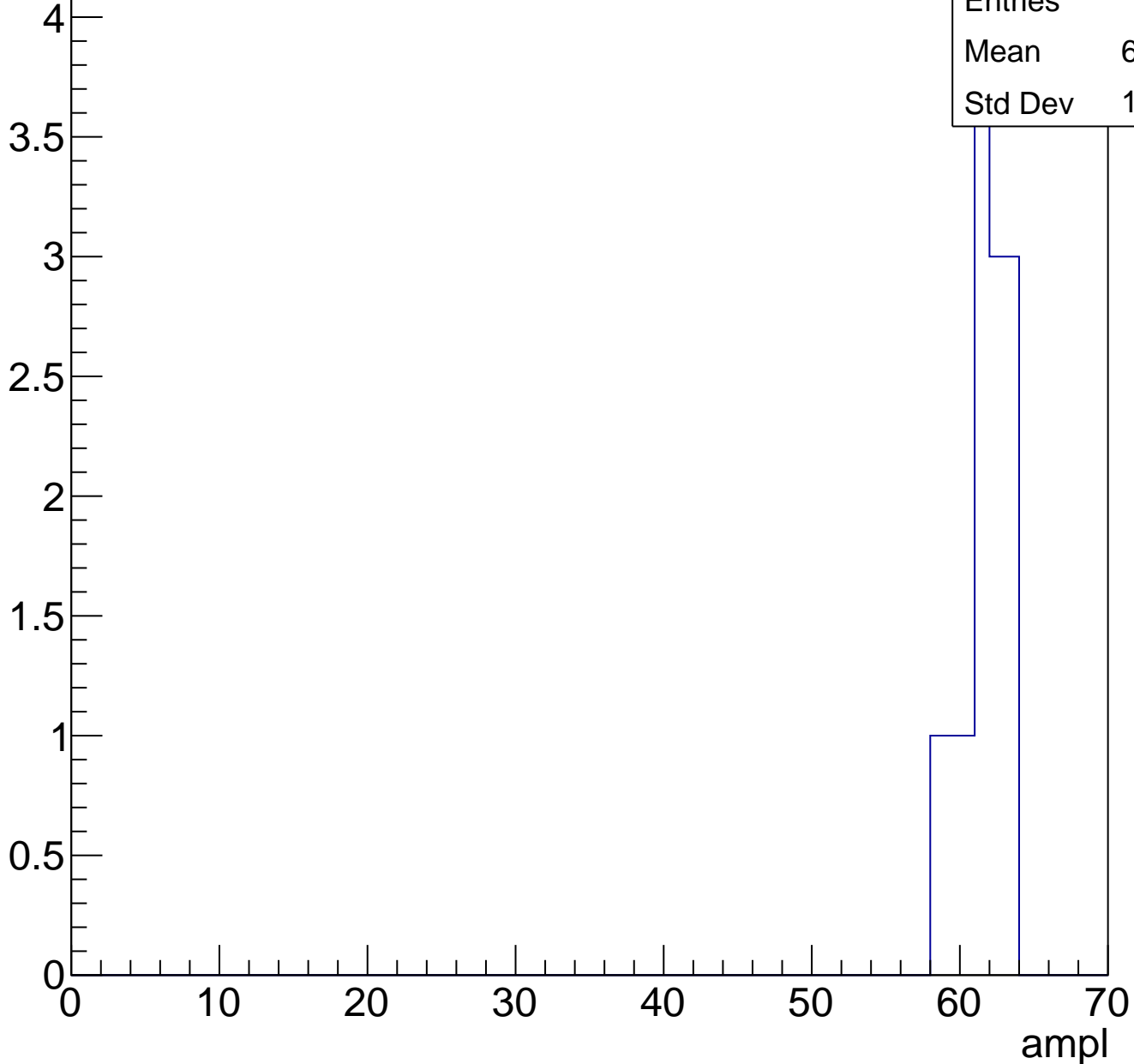
Entries	50
Mean	57.56
Std Dev	8.823



# B1L102S, U21-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U21-ch113, adc0

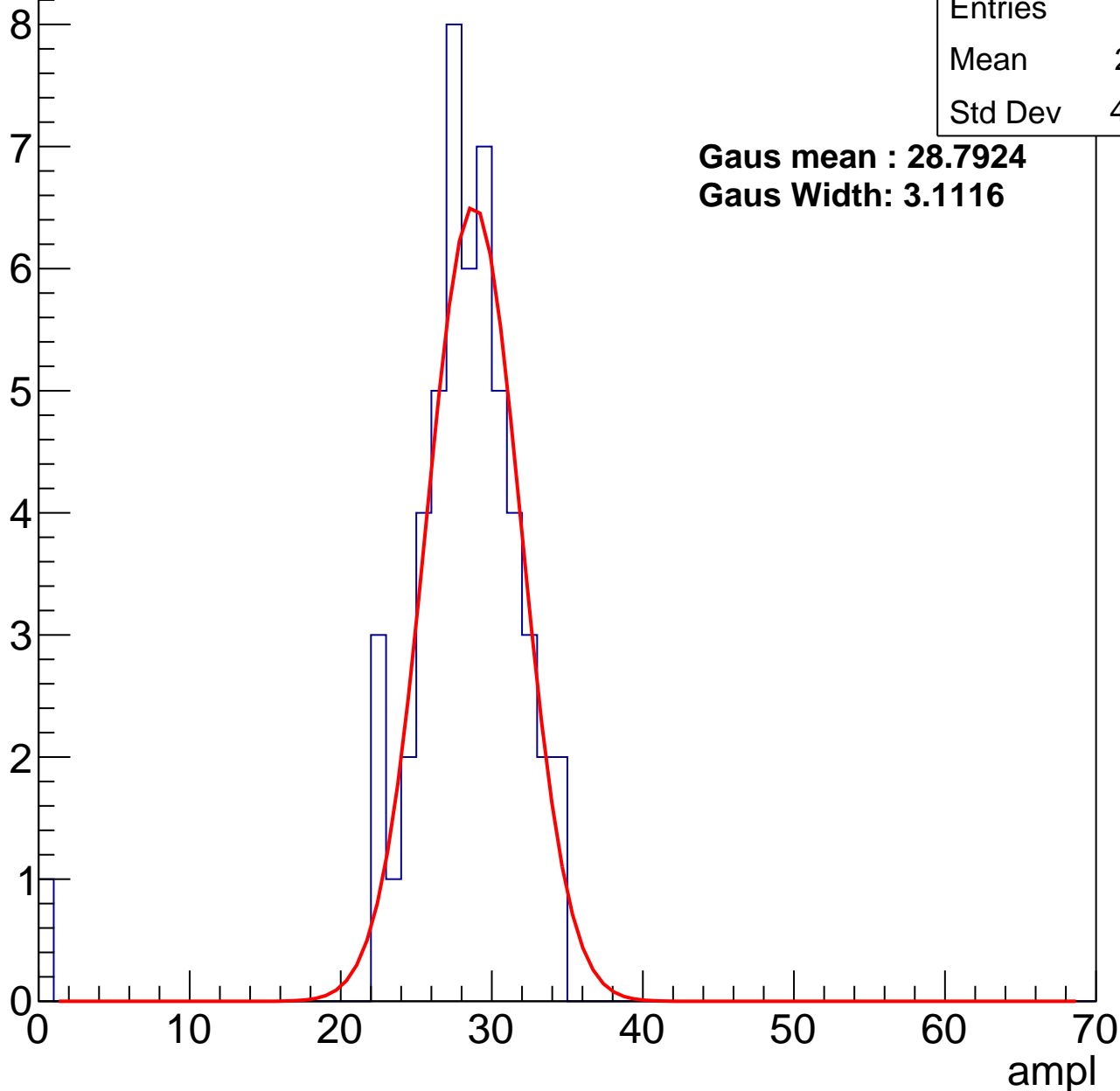
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	27.51
Std Dev	4.824

**Gaus mean : 28.7924**

**Gaus Width: 3.1116**



# B1L102S, U21-ch113, adc1

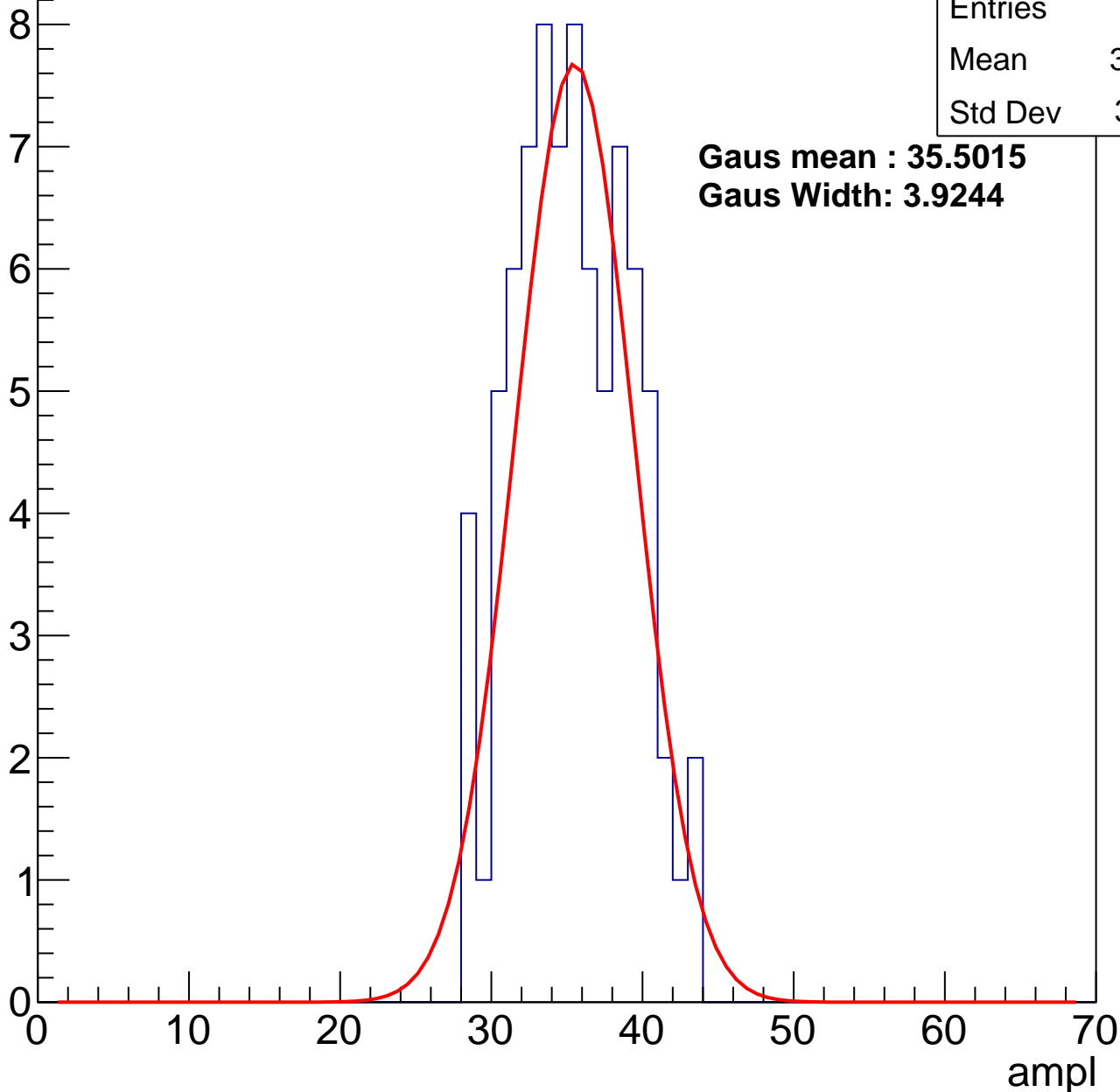
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	34.92
Std Dev	3.731

**Gaus mean : 35.5015**

**Gaus Width: 3.9244**



# B1L102S, U21-ch113, adc2

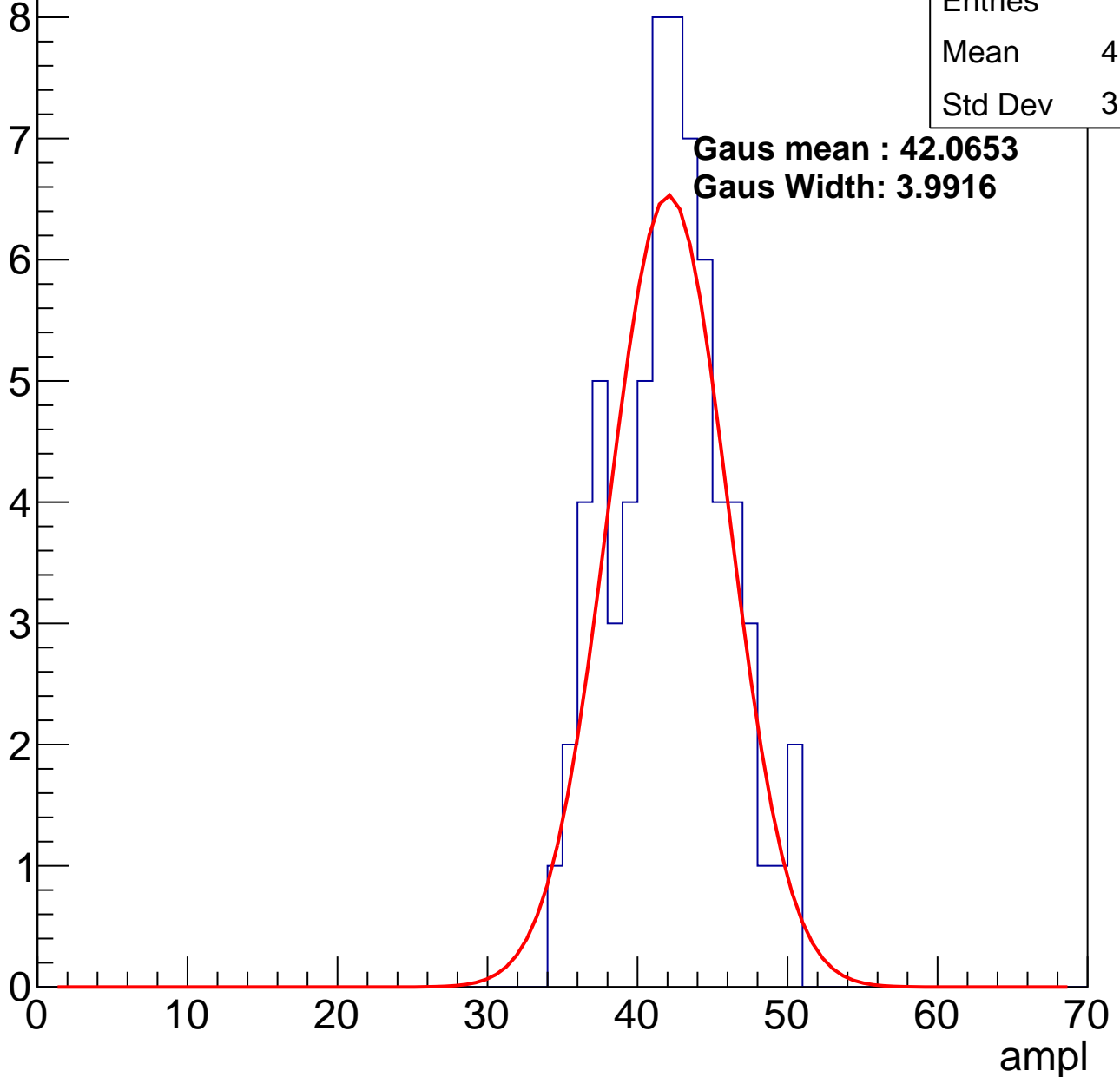
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	41.68
Std Dev	3.747

**Gaus mean : 42.0653**

**Gaus Width: 3.9916**

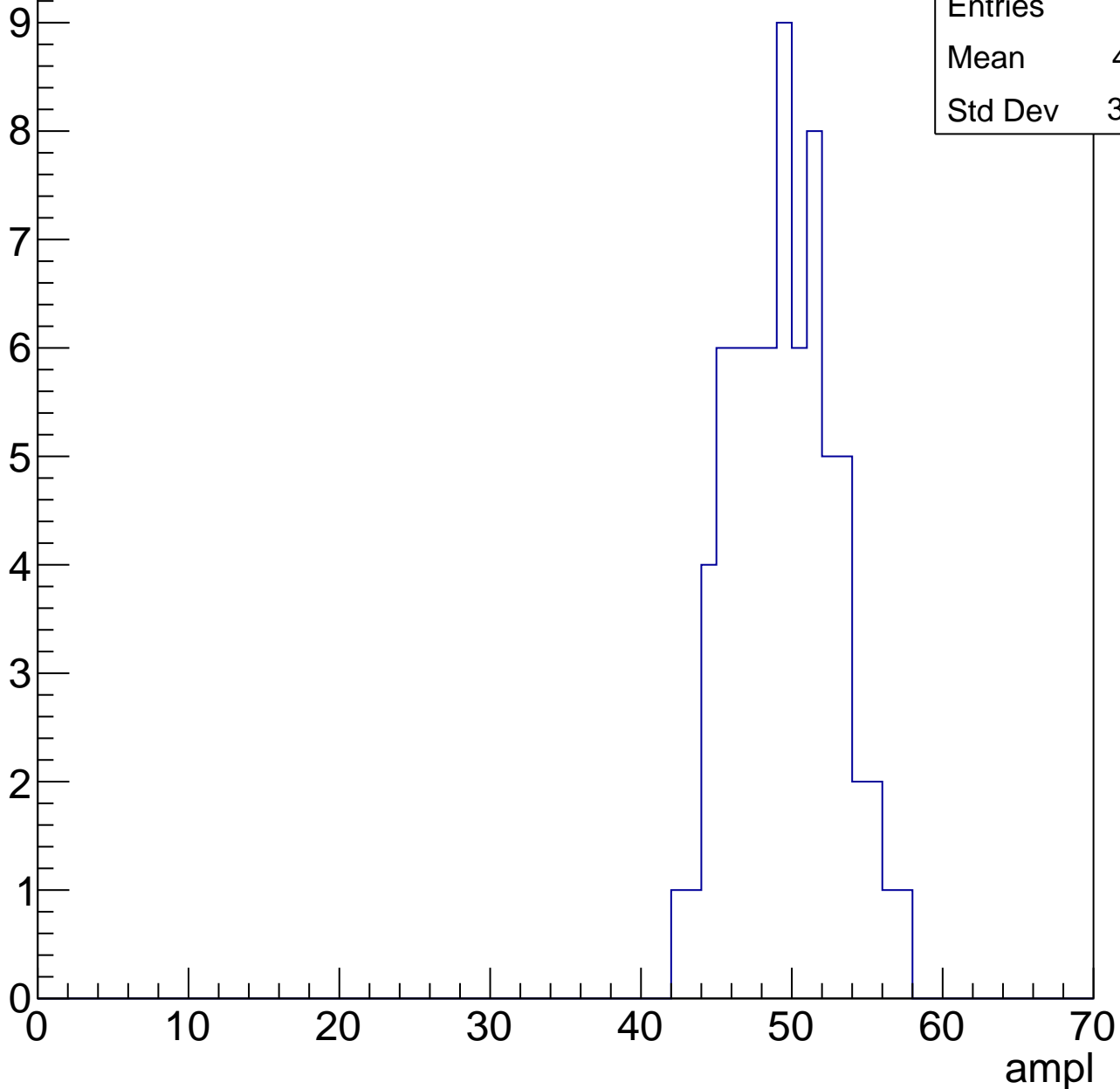


# B1L102S, U21-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	49.01
Std Dev	3.325

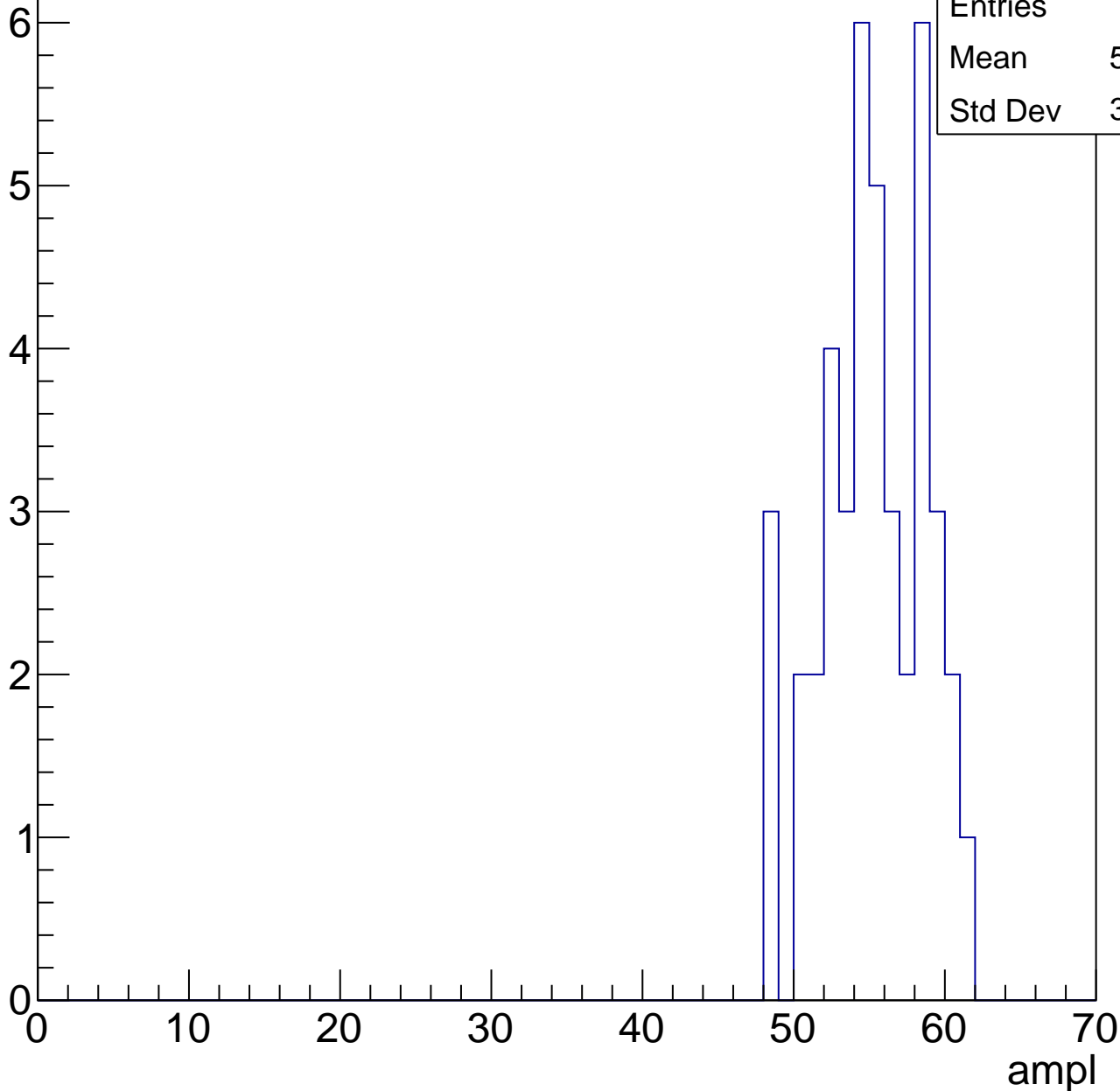


# B1L102S, U21-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	42
Mean	54.76
Std Dev	3.379

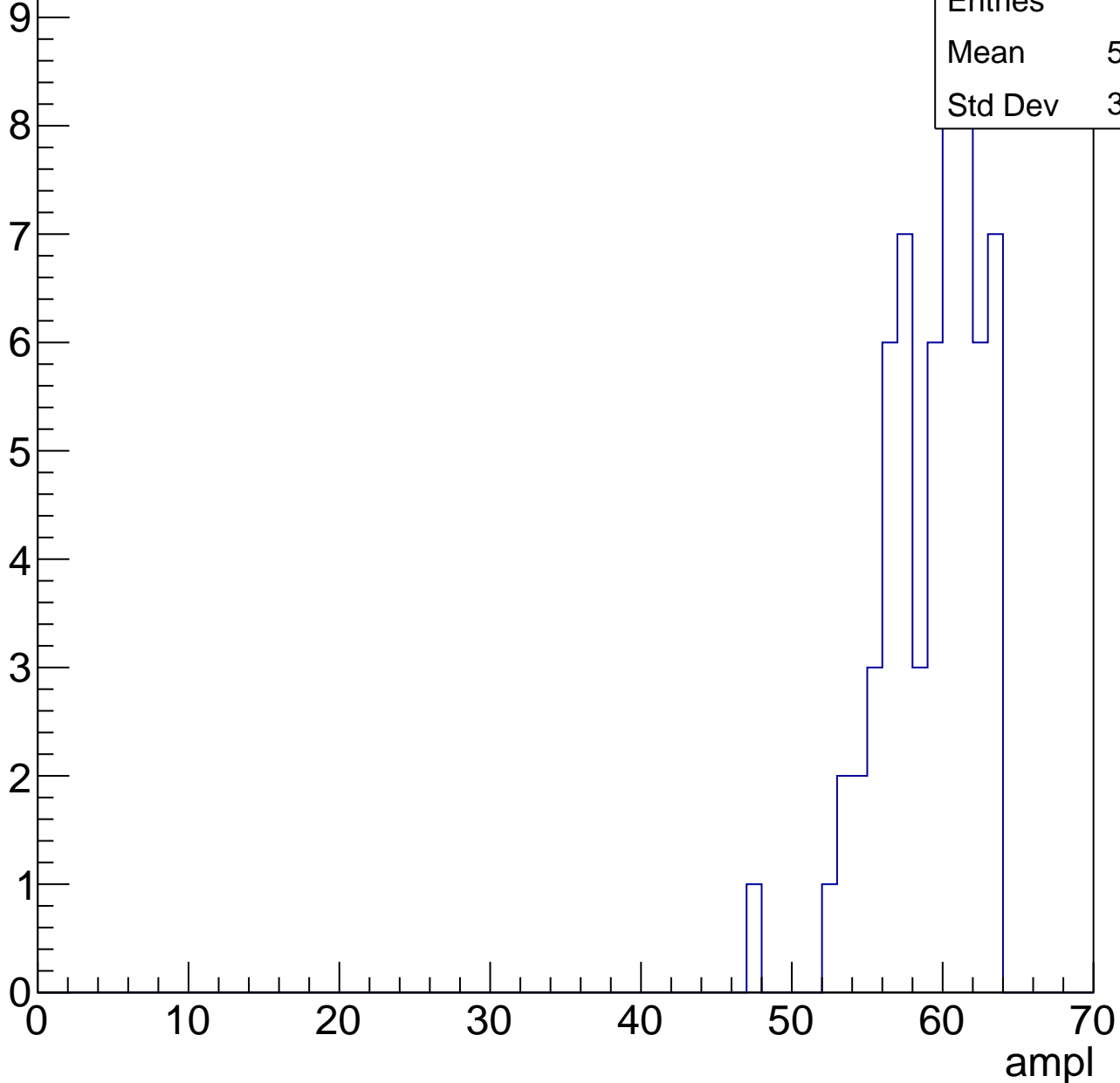


# B1L102S, U21-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

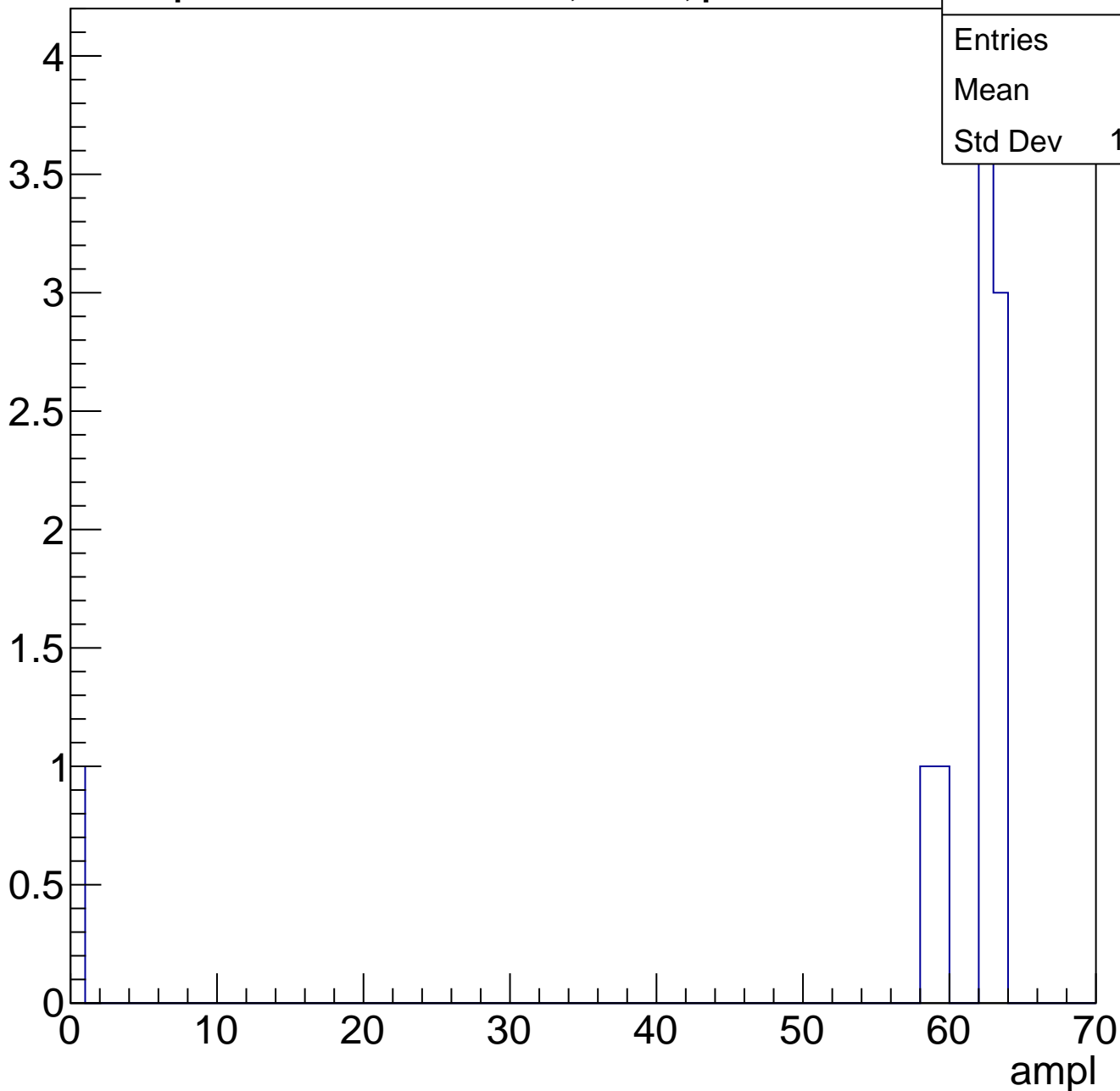
Entries	61
Mean	58.74
Std Dev	3.274



# B1L102S, U21-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	10
Mean	55.4
Std Dev	18.54



# B1L102S, U21-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch114, adc0

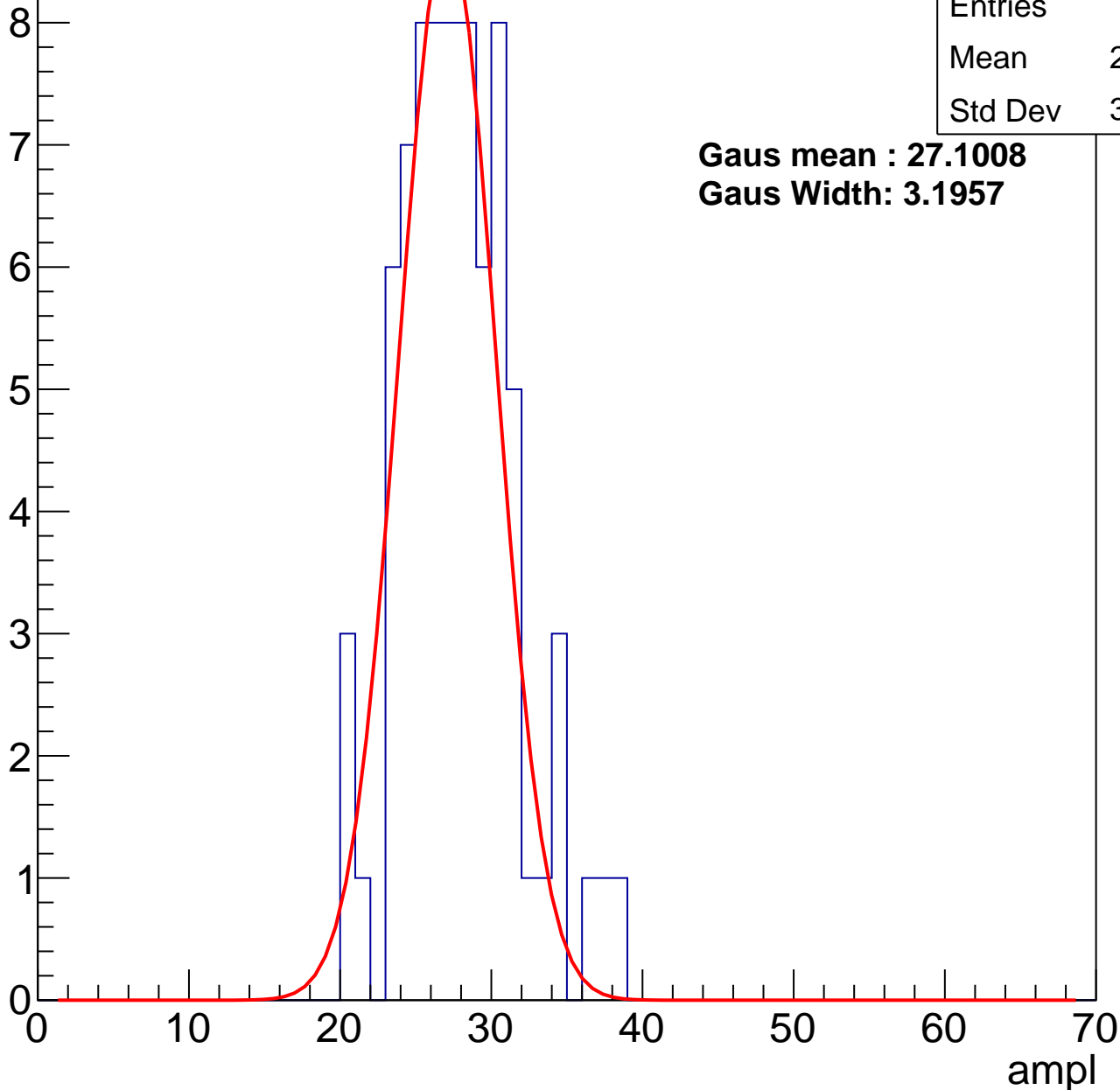
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	27.39
Std Dev	3.742

**Gaus mean : 27.1008**

**Gaus Width: 3.1957**



# B1L102S, U21-ch114, adc1

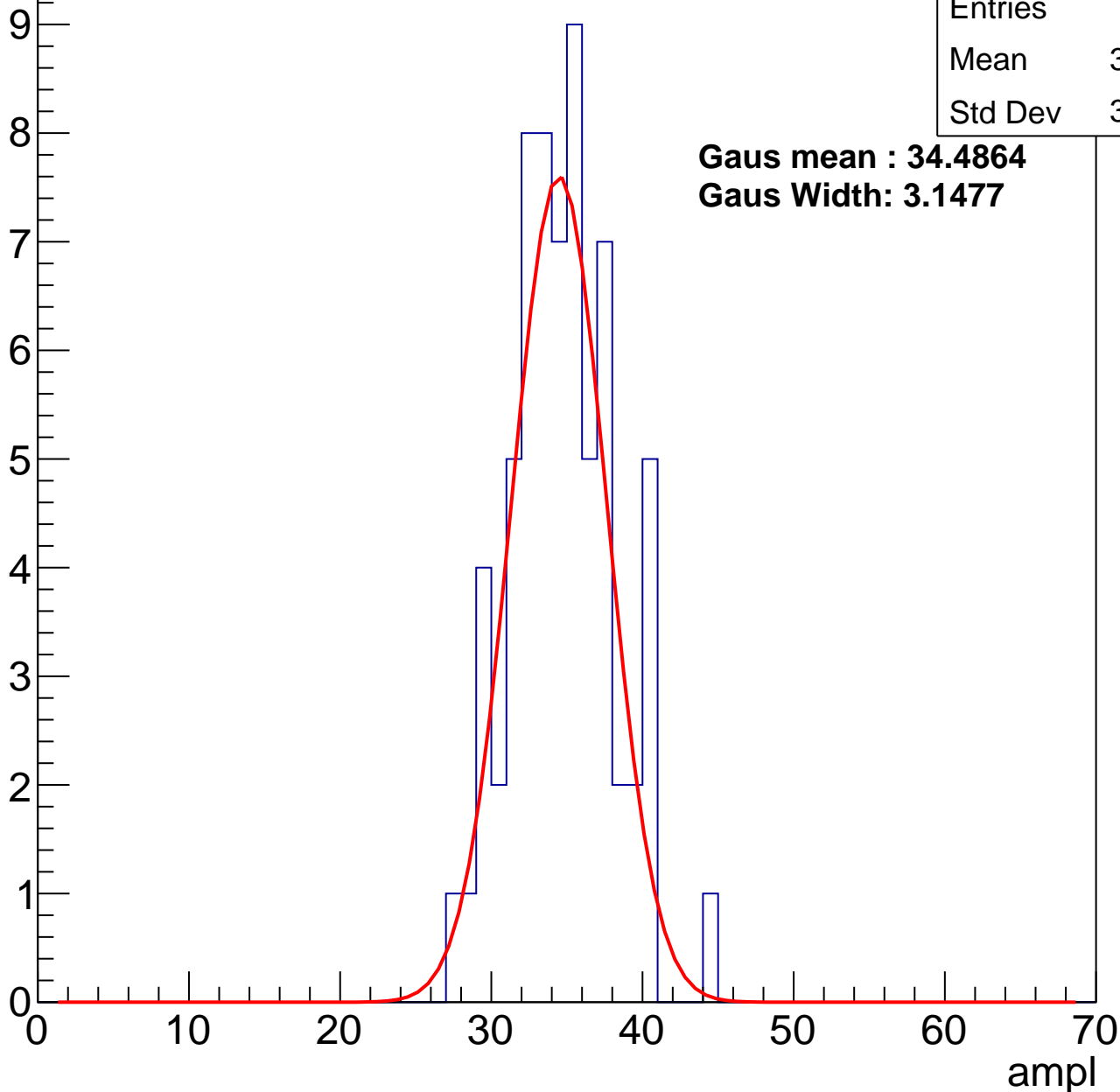
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	34.27
Std Dev	3.348

**Gaus mean : 34.4864**

**Gaus Width: 3.1477**



# B1L102S, U21-ch114, adc2

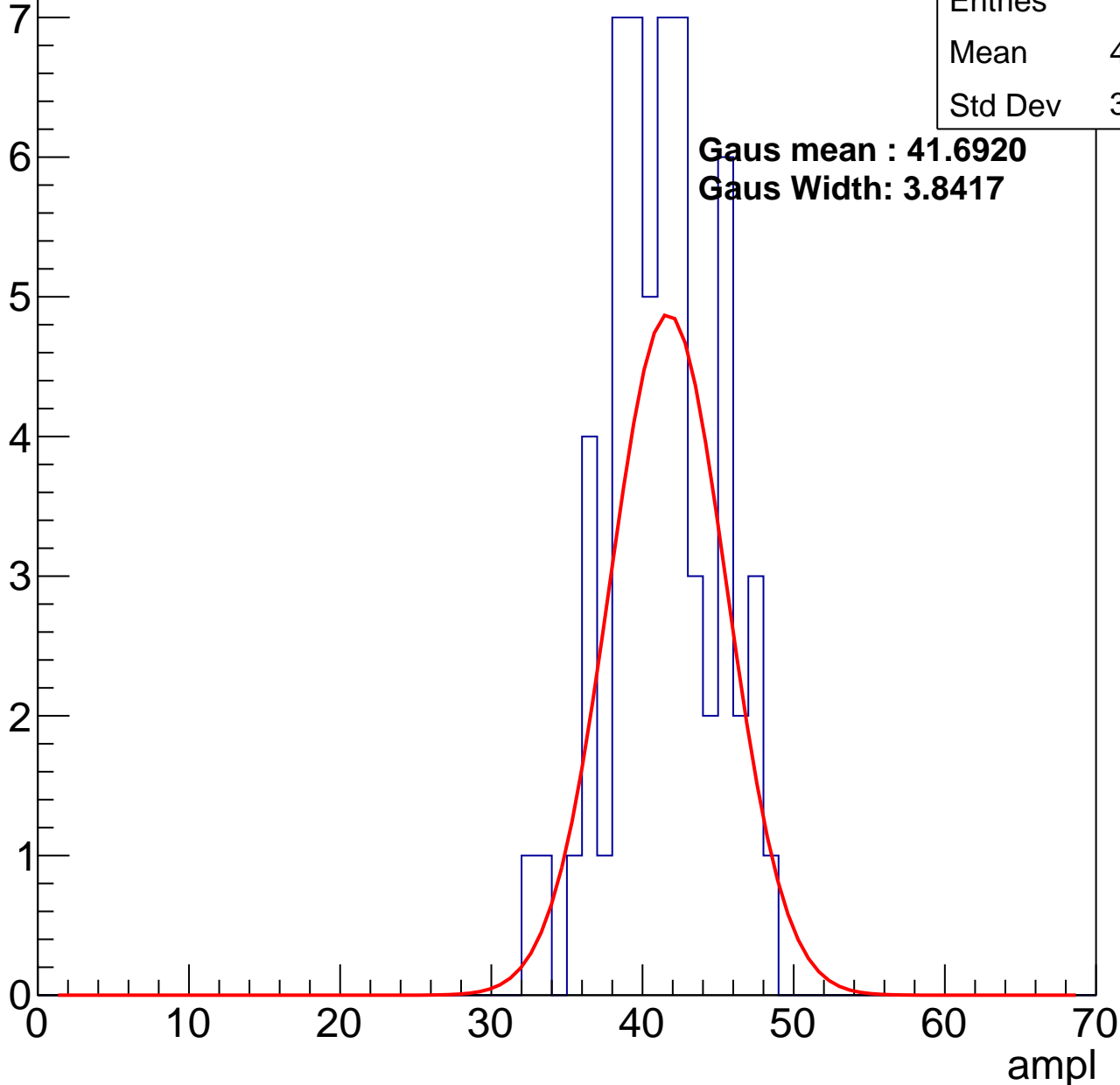
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	40.84
Std Dev	3.552

**Gaus mean : 41.6920**

**Gaus Width: 3.8417**

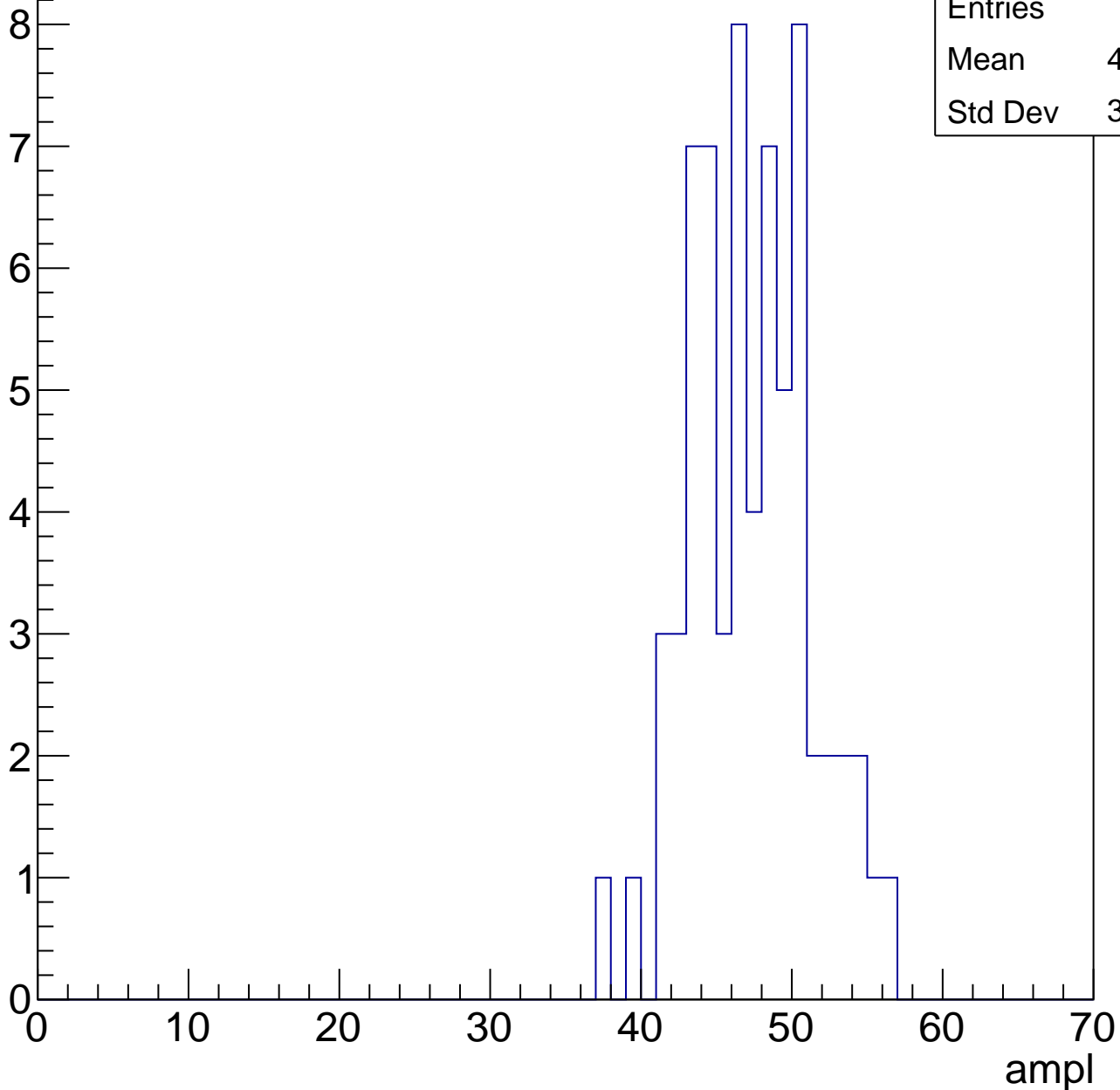


# B1L102S, U21-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	46.82
Std Dev	3.932

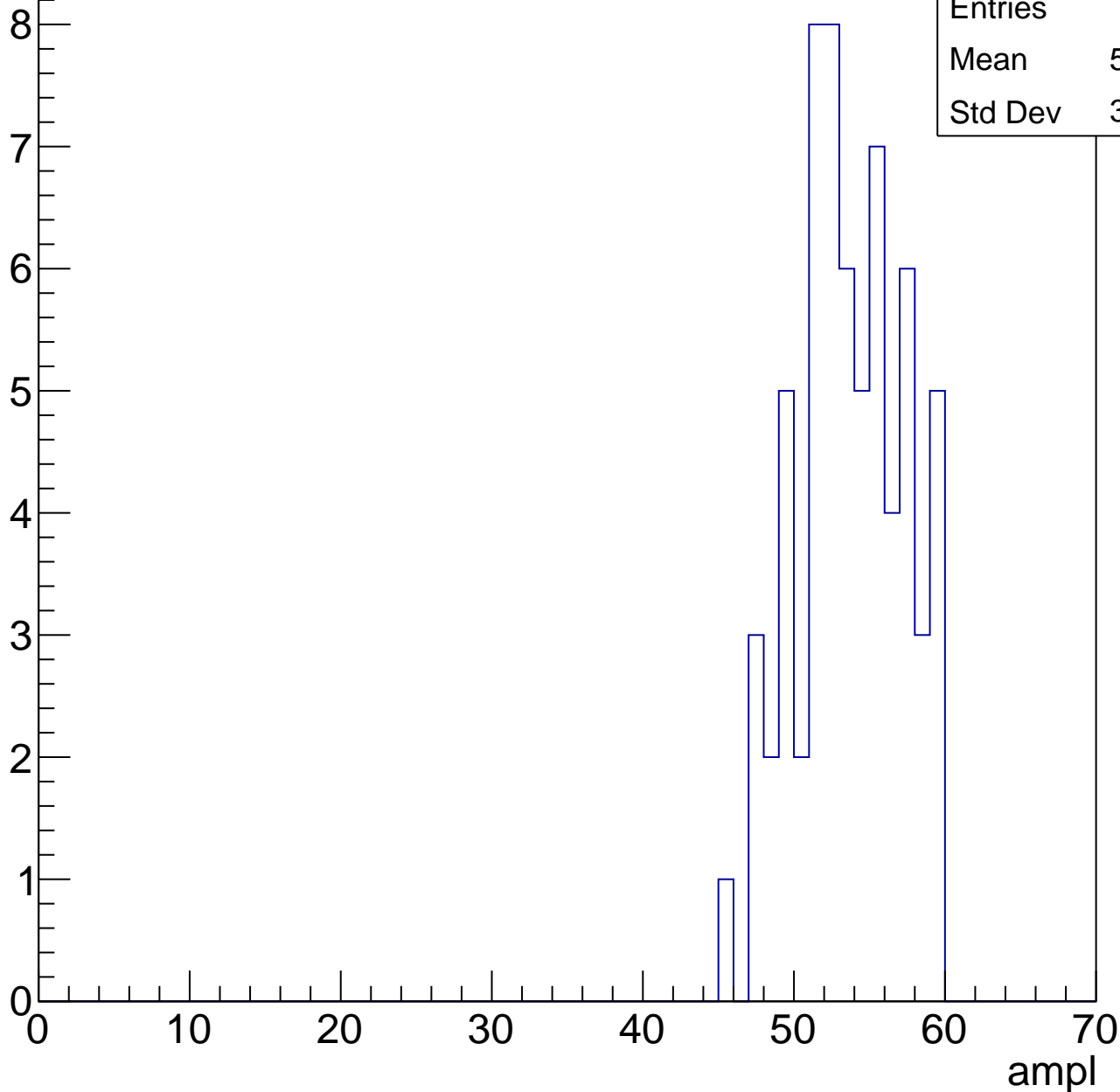


# B1L102S, U21-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	53.22
Std Dev	3.457



# B1L102S, U21-ch114, adc5

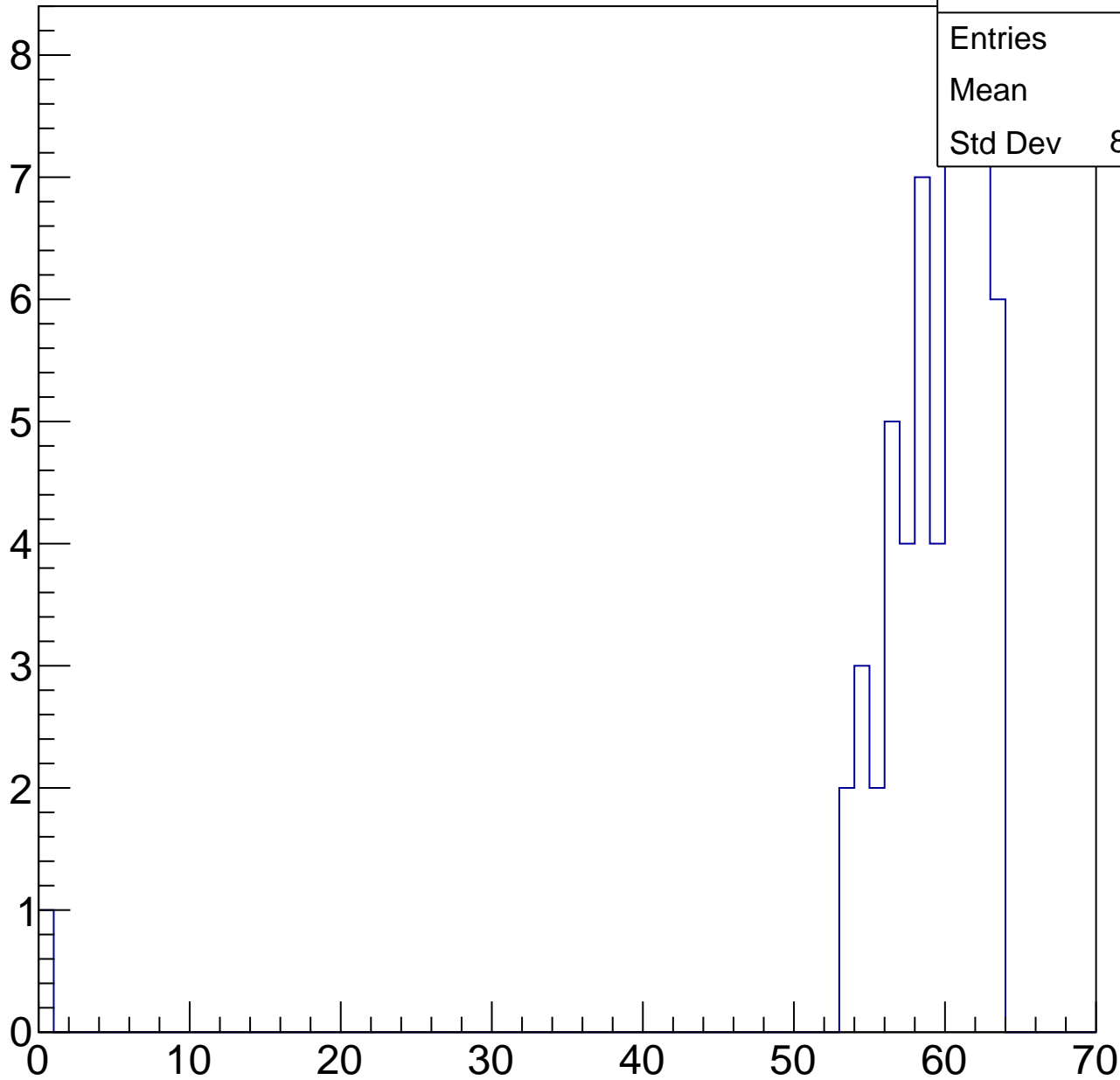
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	58
Mean	58.1
Std Dev	8.189

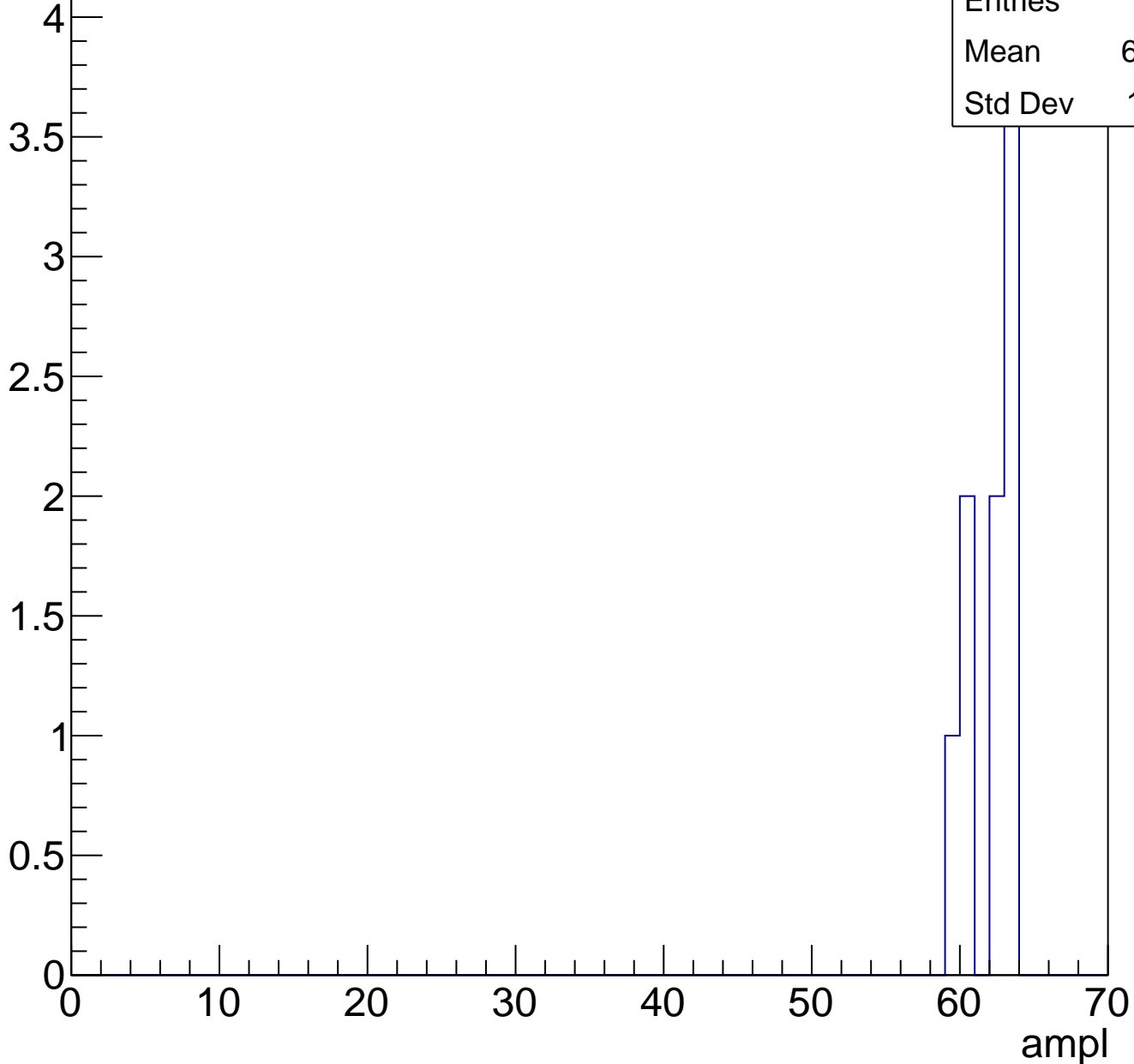
ampl



# B1L102S, U21-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

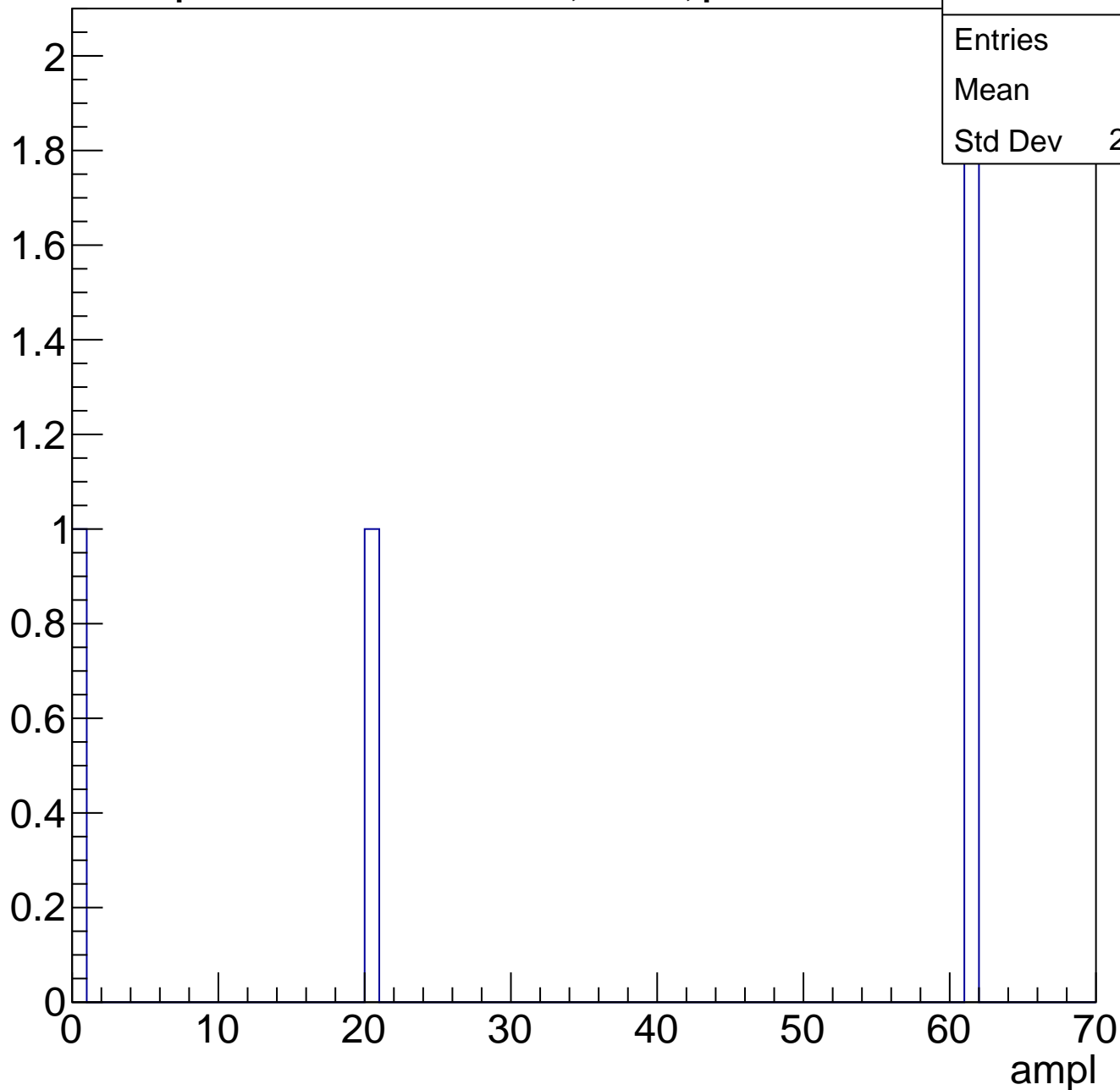




# B1L102S, U21-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch115, adc0

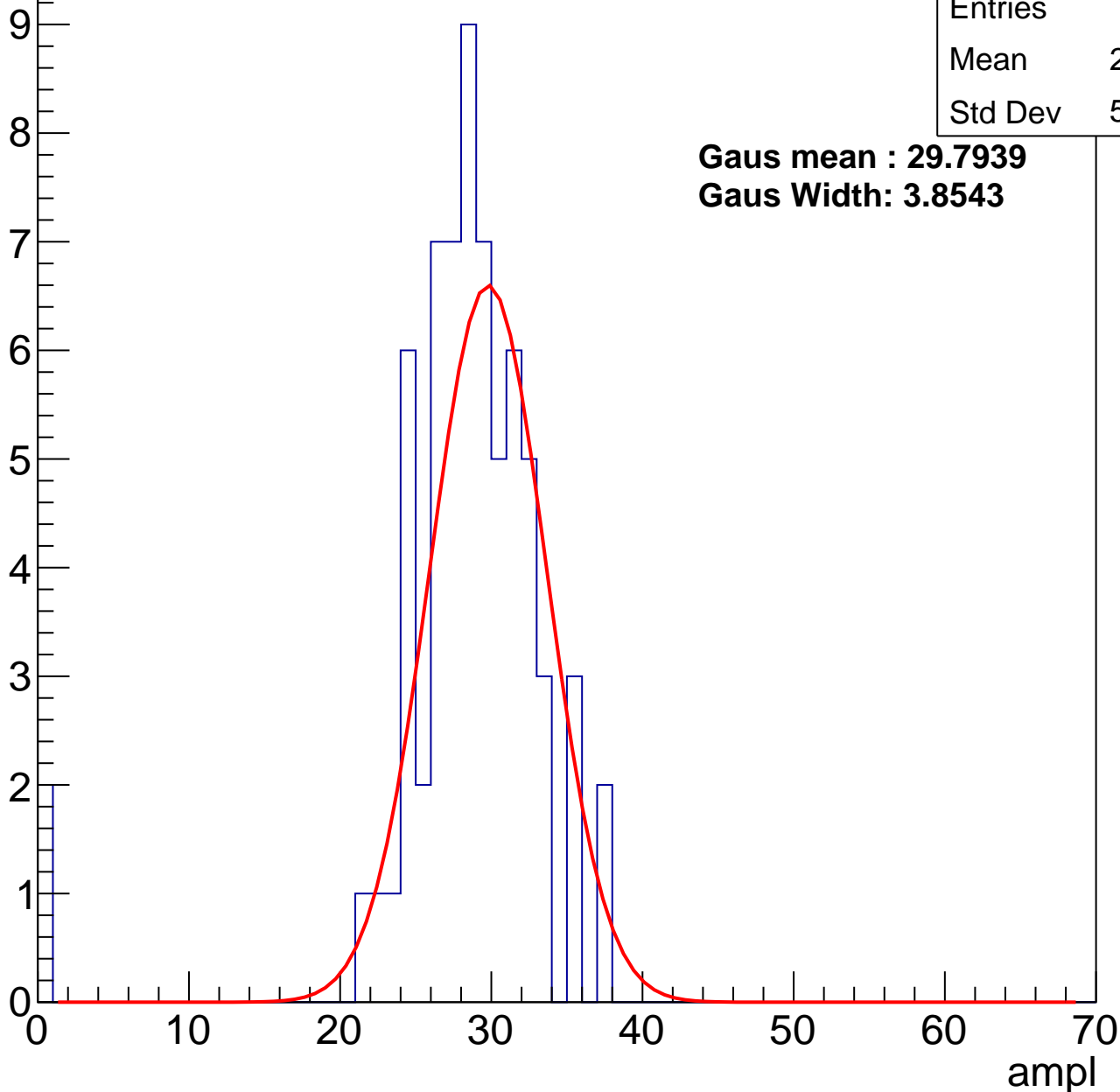
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	27.76
Std Dev	5.945

**Gaus mean : 29.7939**

**Gaus Width: 3.8543**



# B1L102S, U21-ch115, adc1

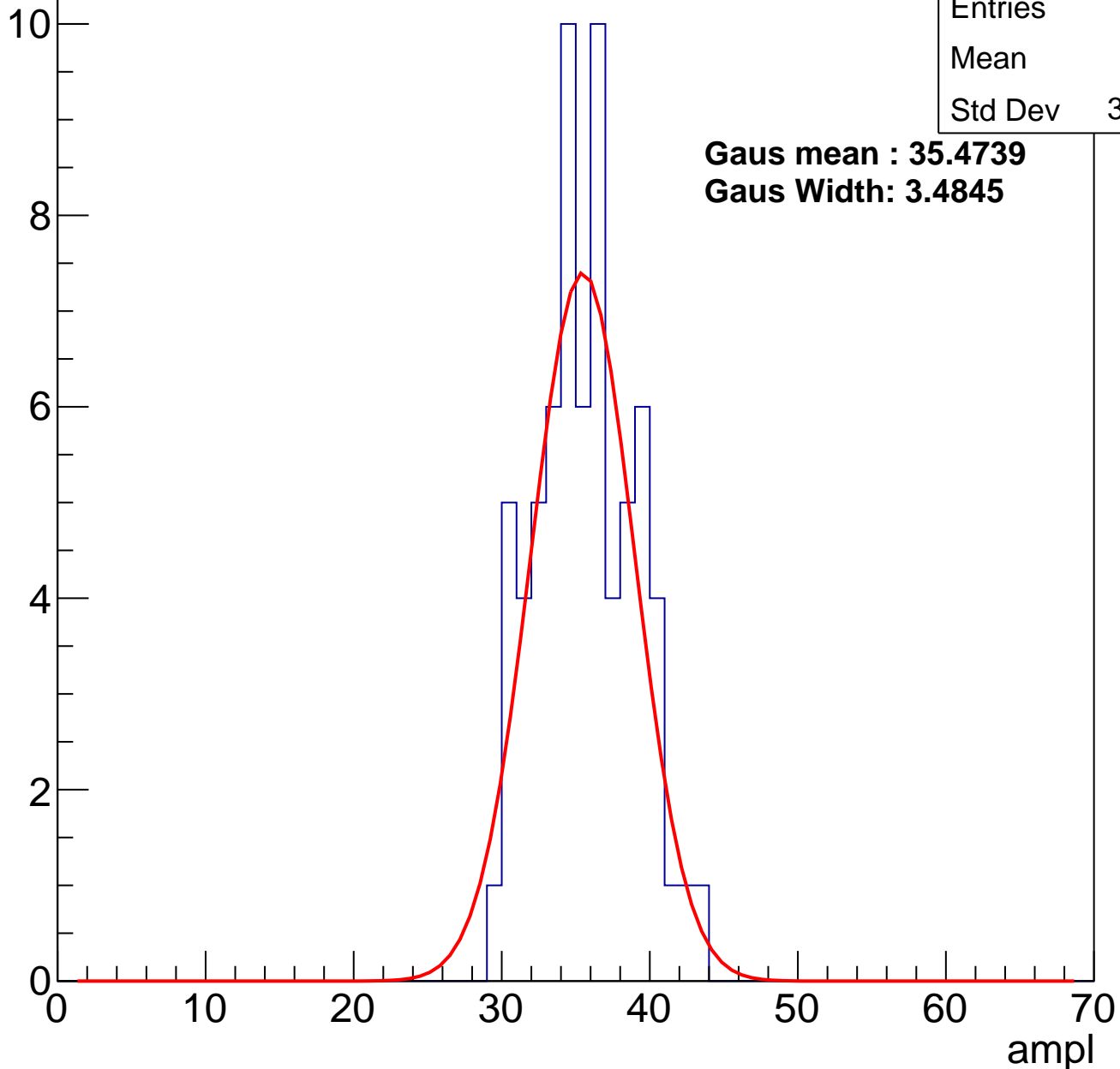
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	69
Mean	35.2
Std Dev	3.224

**Gaus mean : 35.4739**

**Gaus Width: 3.4845**

Entry



# B1L102S, U21-ch115, adc2

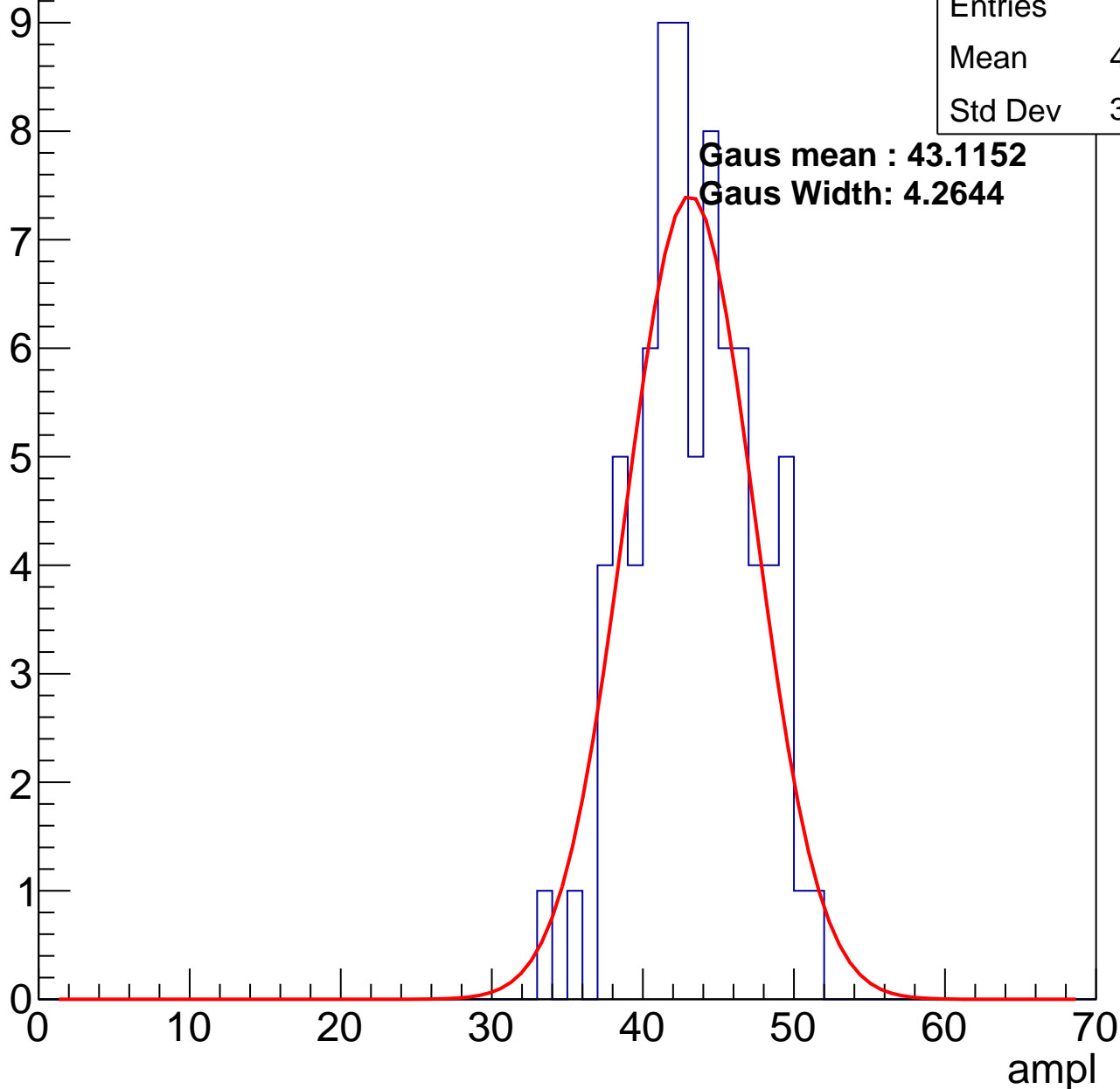
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	42.89
Std Dev	3.795

**Gaus mean : 43.1152**

**Gaus Width: 4.2644**

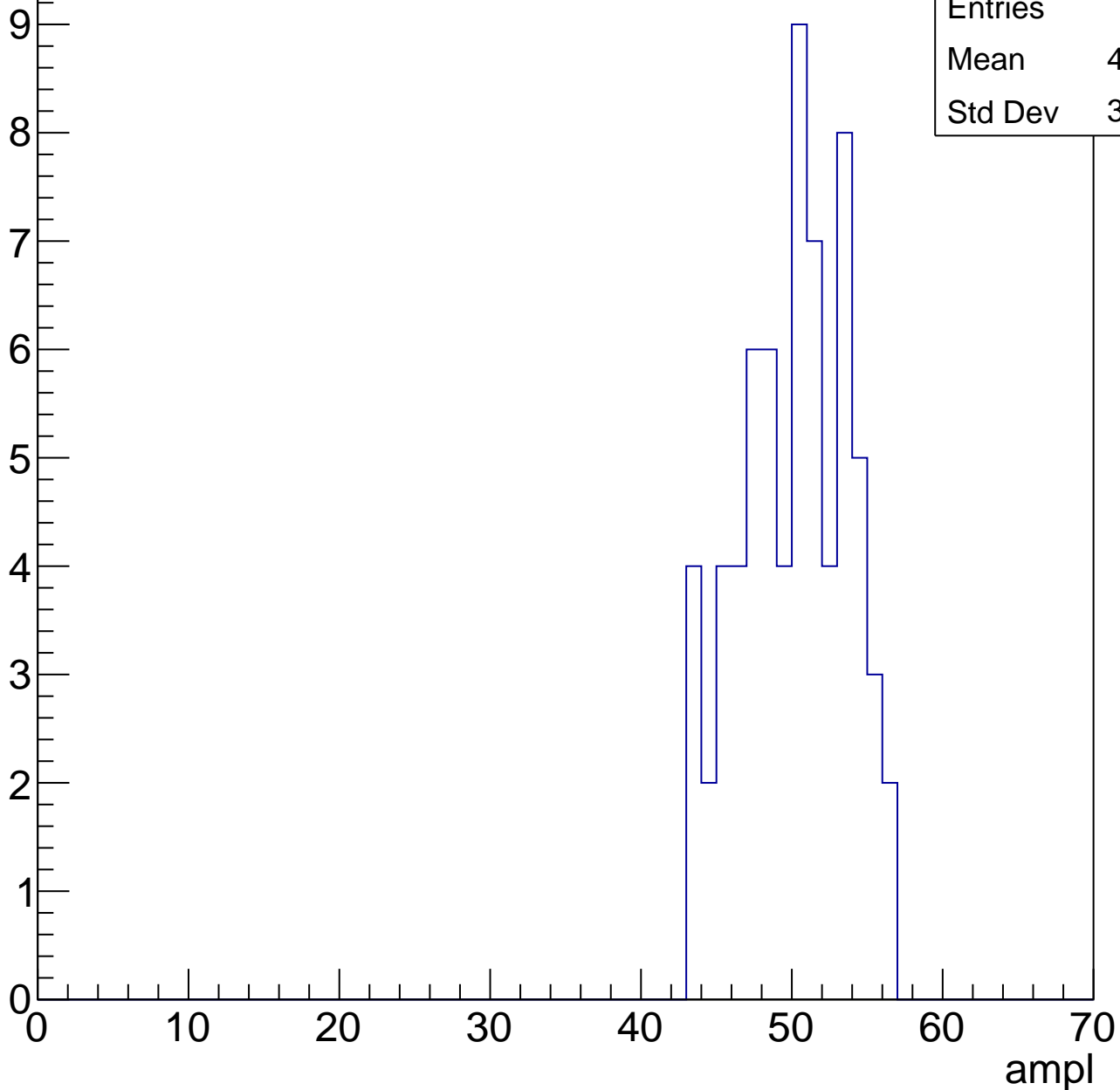


# B1L102S, U21-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	49.65
Std Dev	3.488

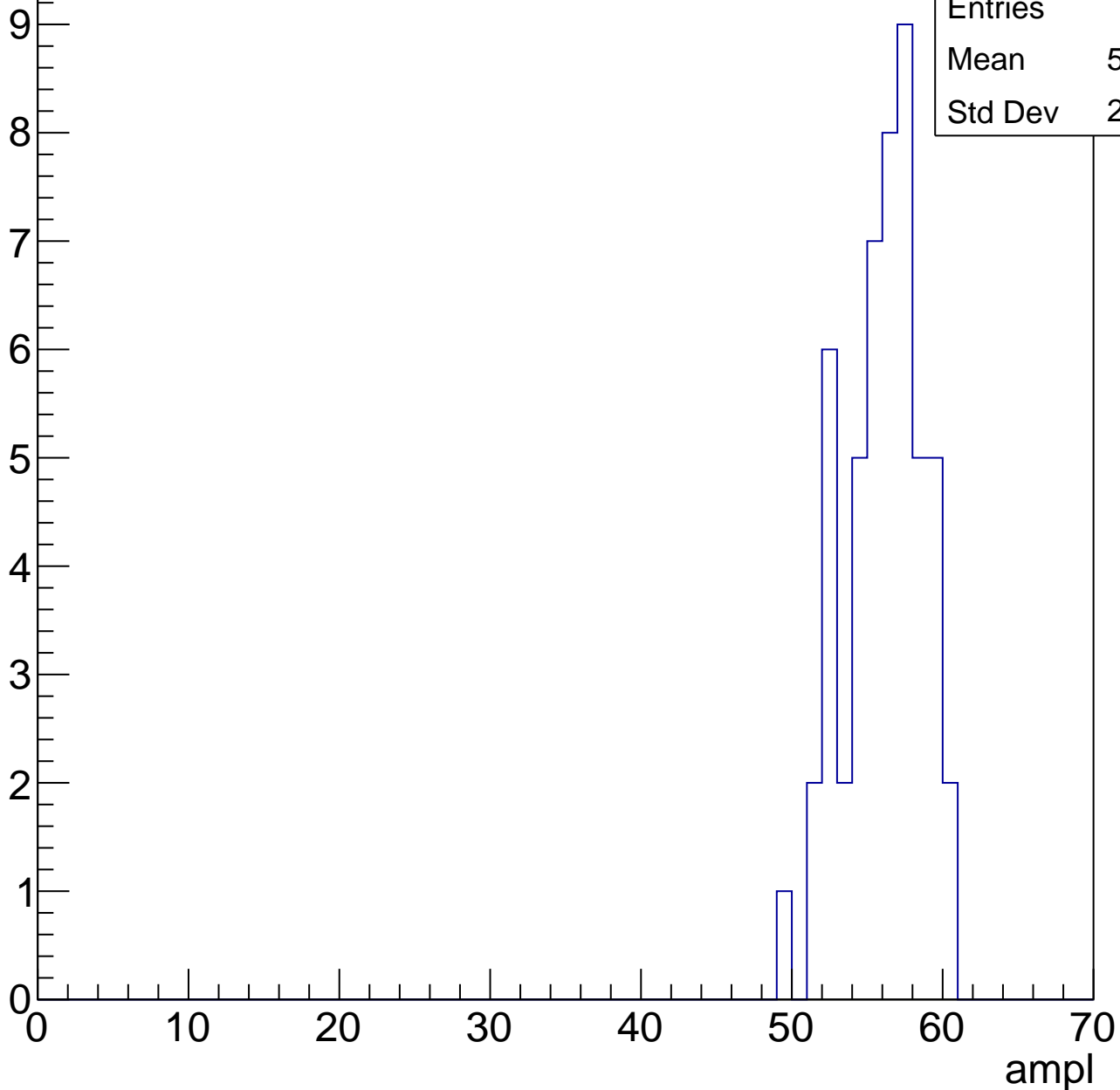


# B1L102S, U21-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	55.58
Std Dev	2.545

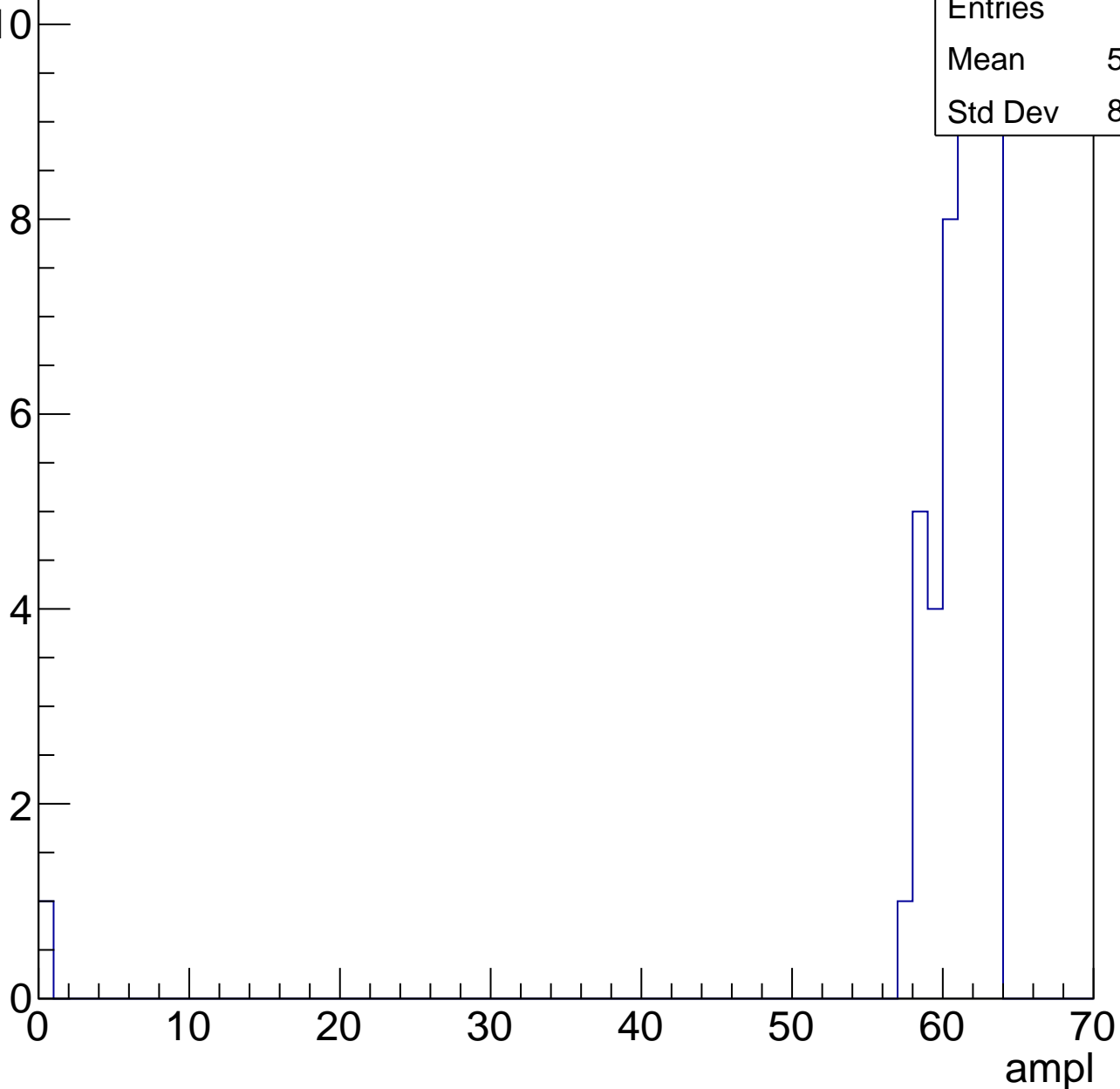


# B1L102S, U21-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

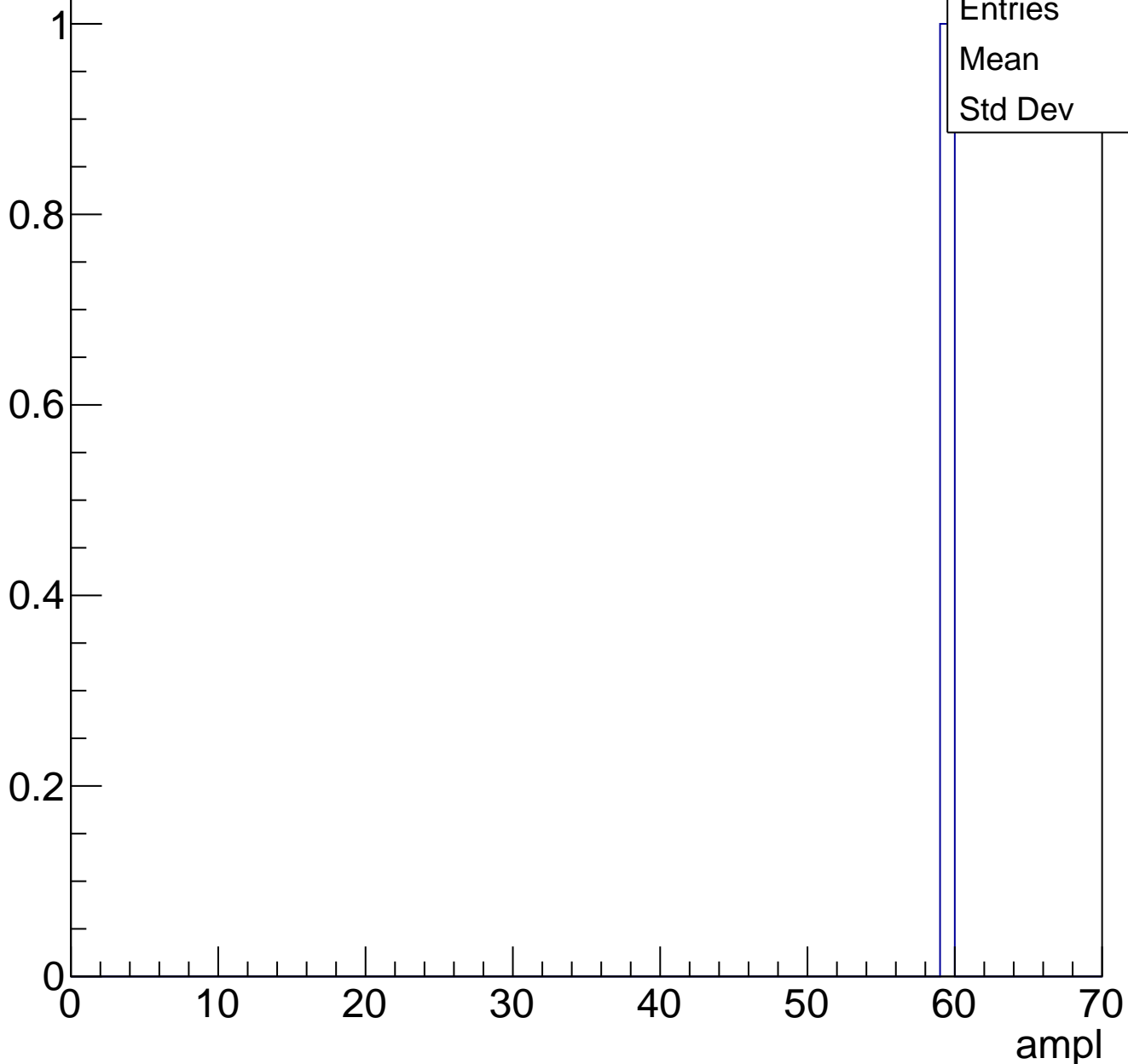
Entries	49
Mean	59.65
Std Dev	8.768



# B1L102S, U21-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	59
Std Dev	0



# B1L102S, U21-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U21-ch116, adc0

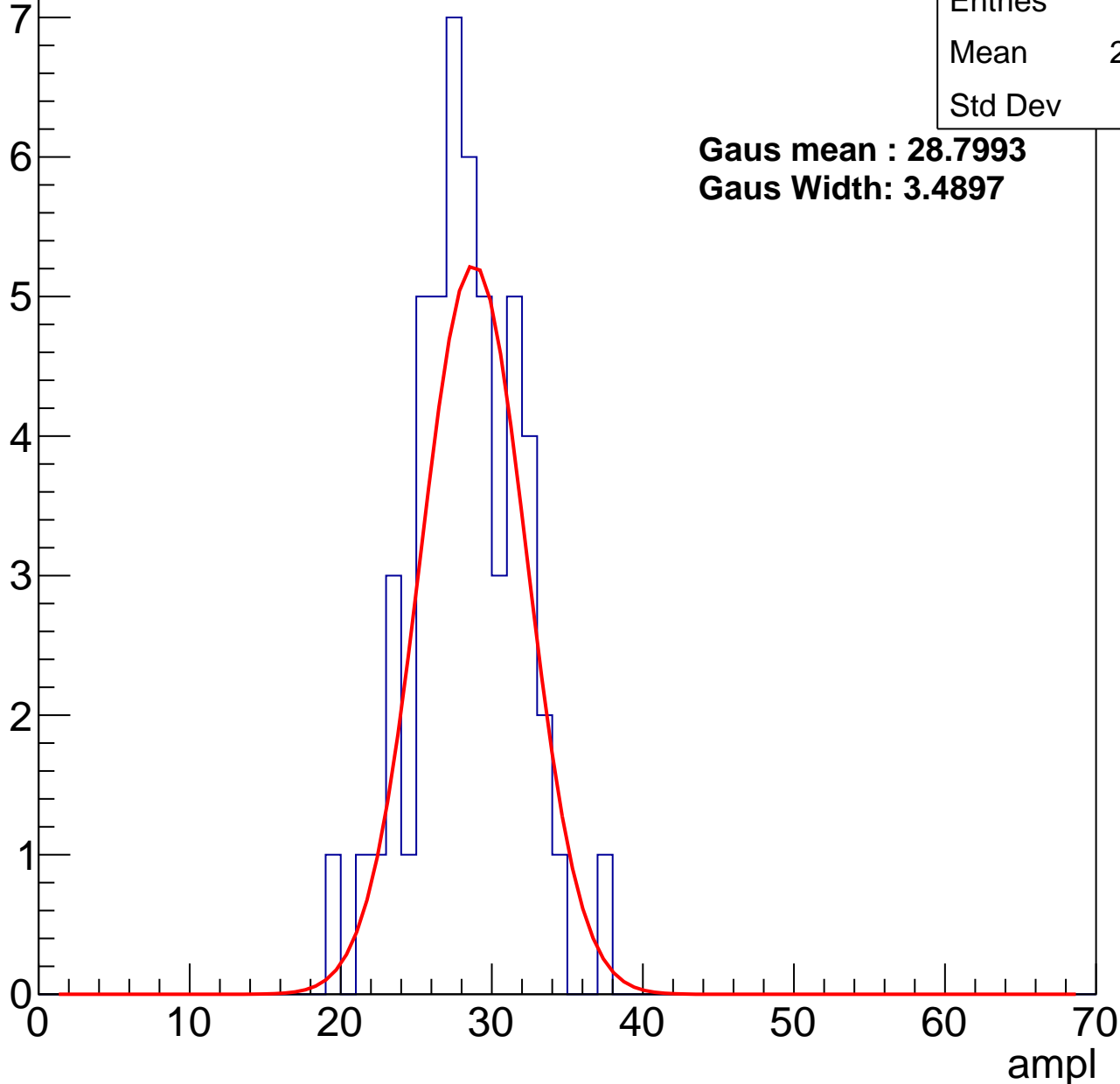
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	27.88
Std Dev	3.49

**Gaus mean : 28.7993**

**Gaus Width: 3.4897**



# B1L102S, U21-ch116, adc1

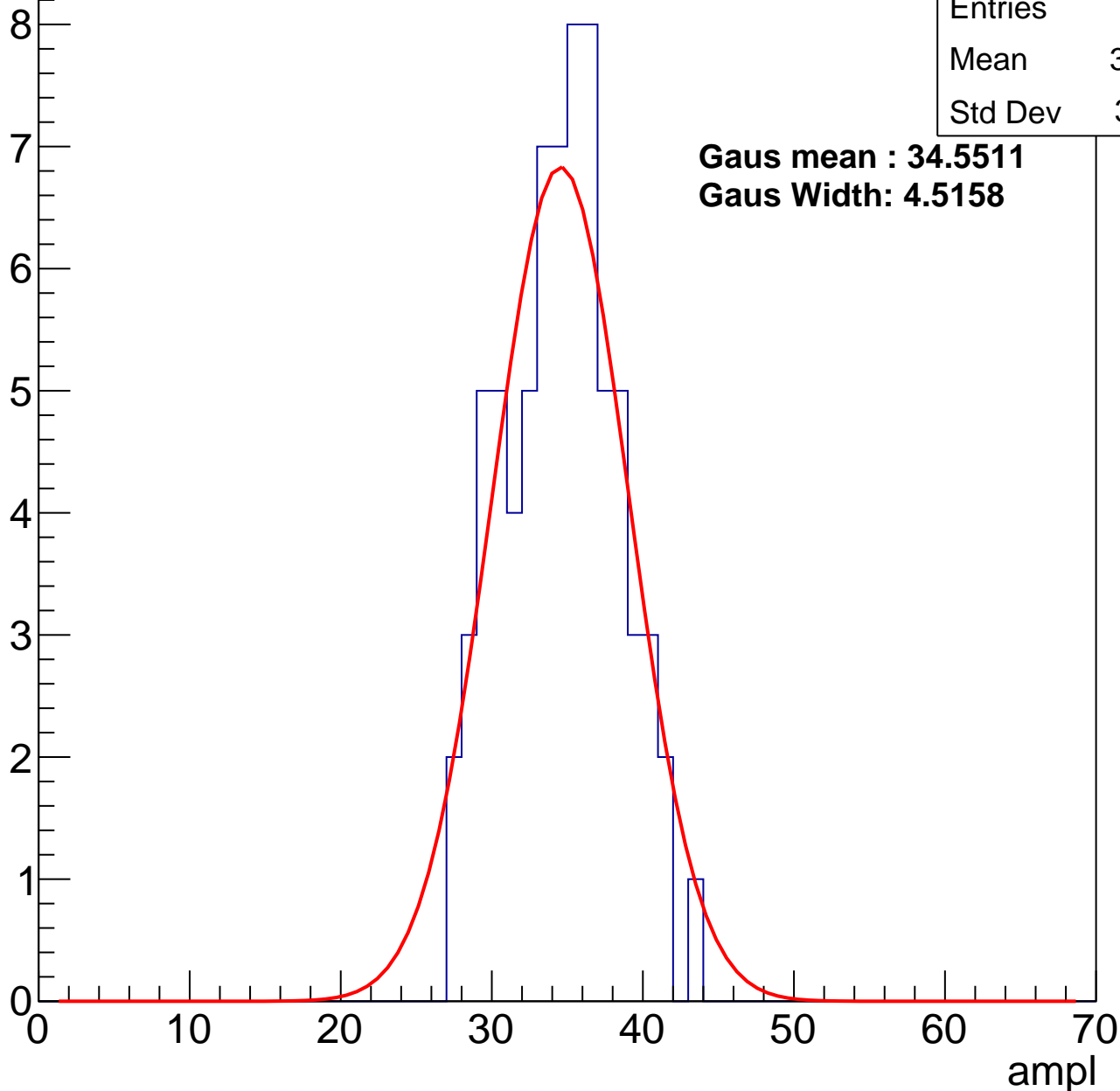
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	34.12
Std Dev	3.701

**Gaus mean : 34.5511**

**Gaus Width: 4.5158**



# B1L102S, U21-ch116, adc2

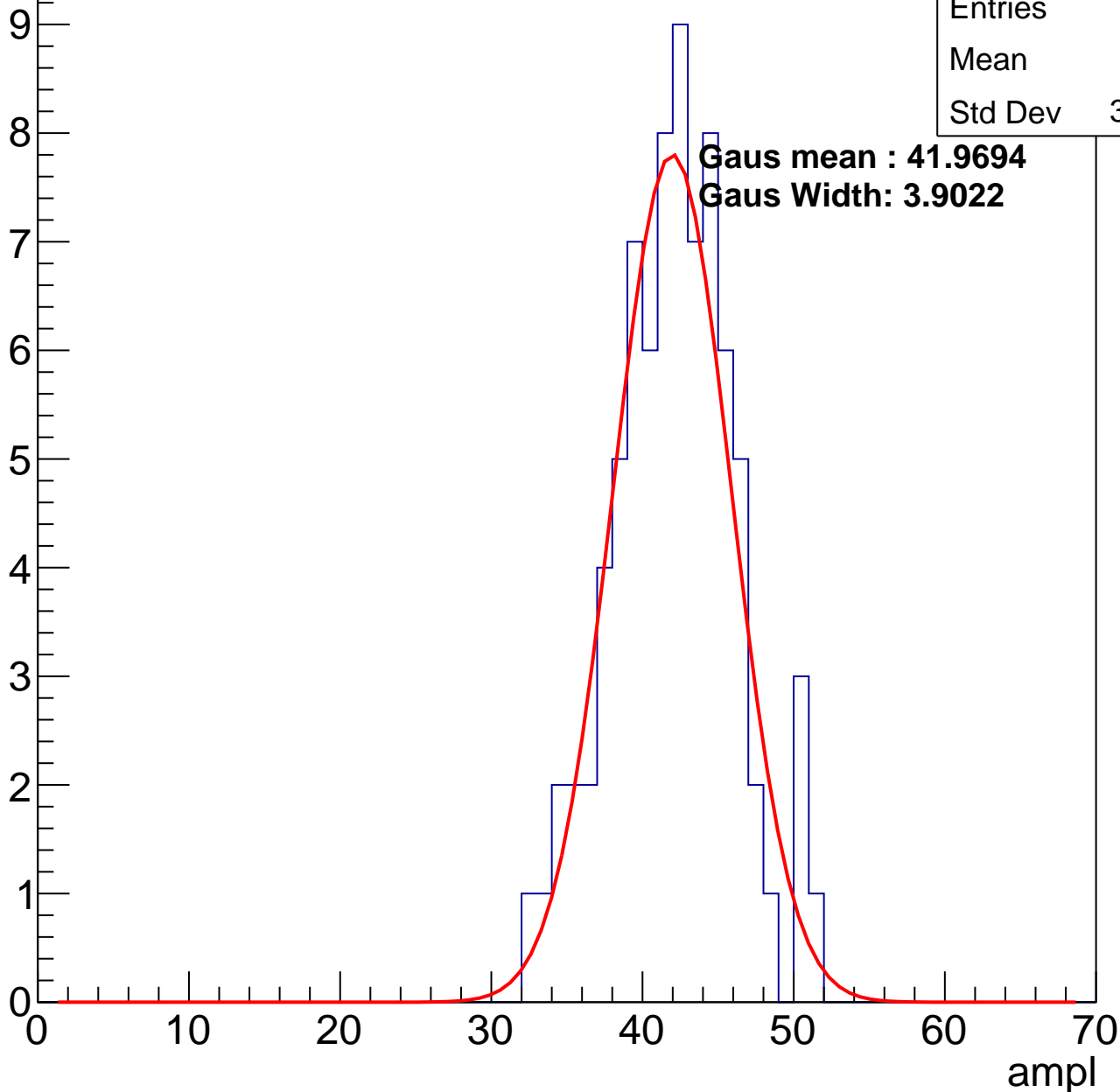
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	41.6
Std Dev	3.989

**Gaus mean : 41.9694**

**Gaus Width: 3.9022**

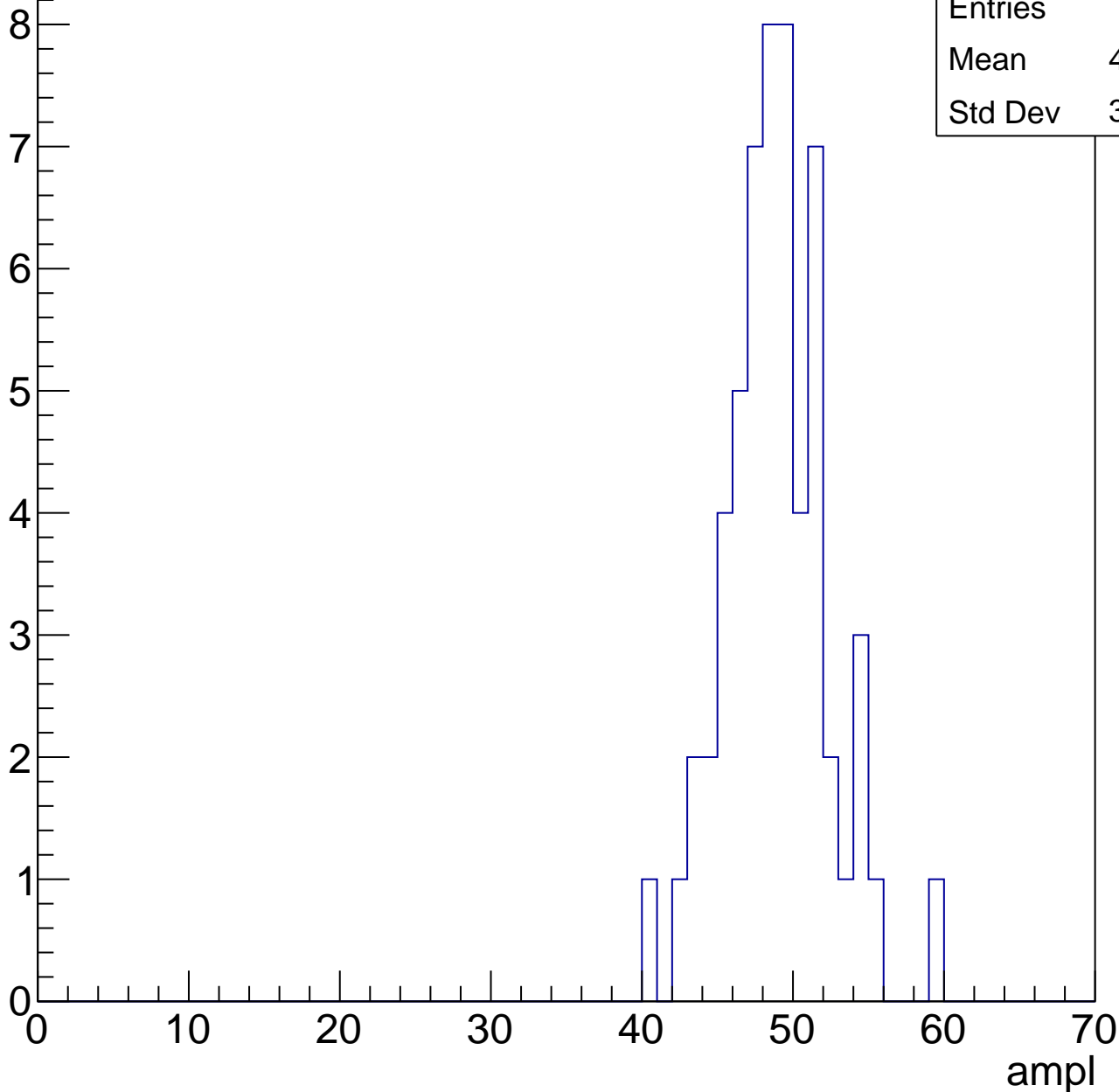


# B1L102S, U21-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	48.44
Std Dev	3.393

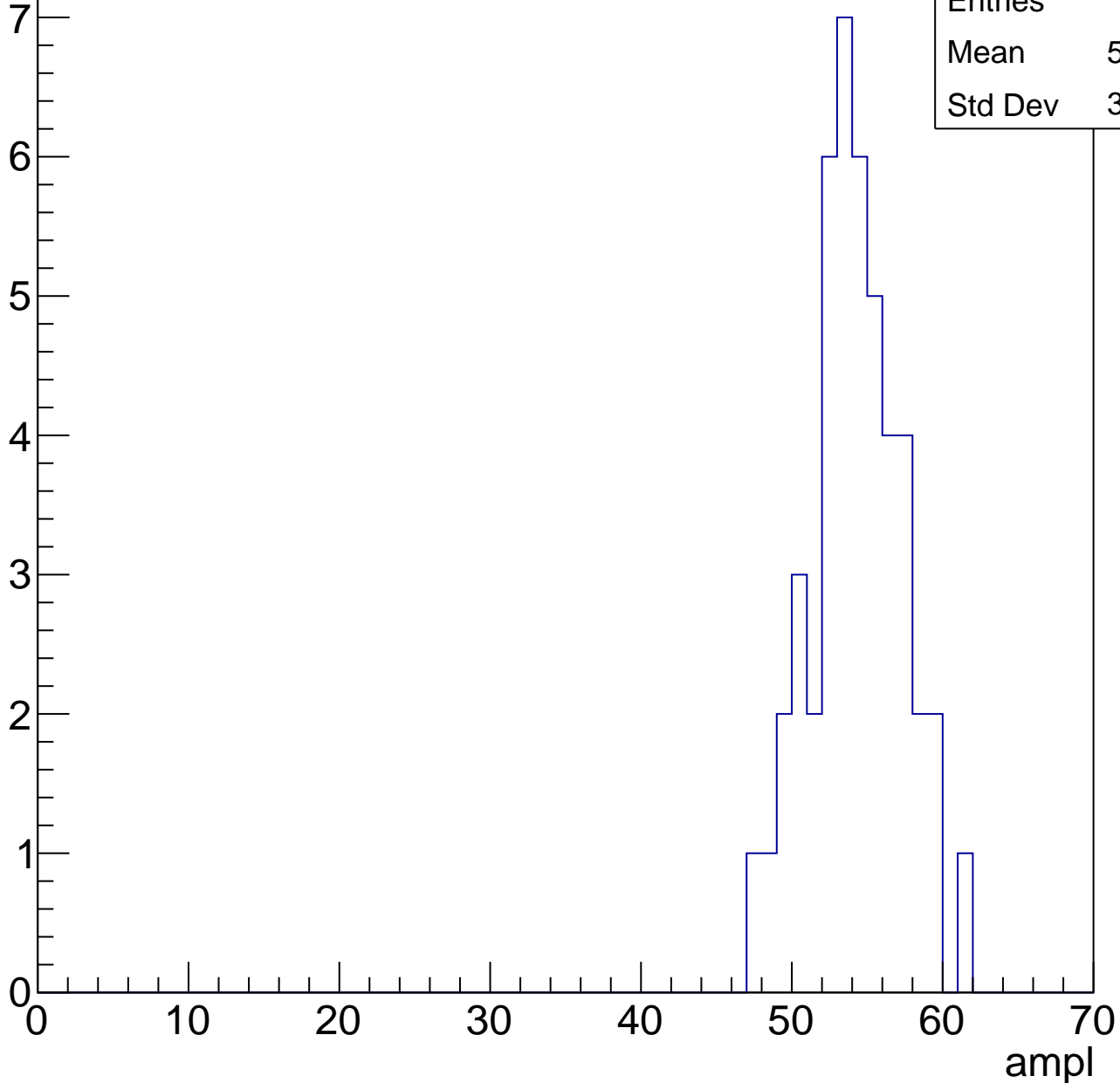


# B1L102S, U21-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	53.78
Std Dev	3.014

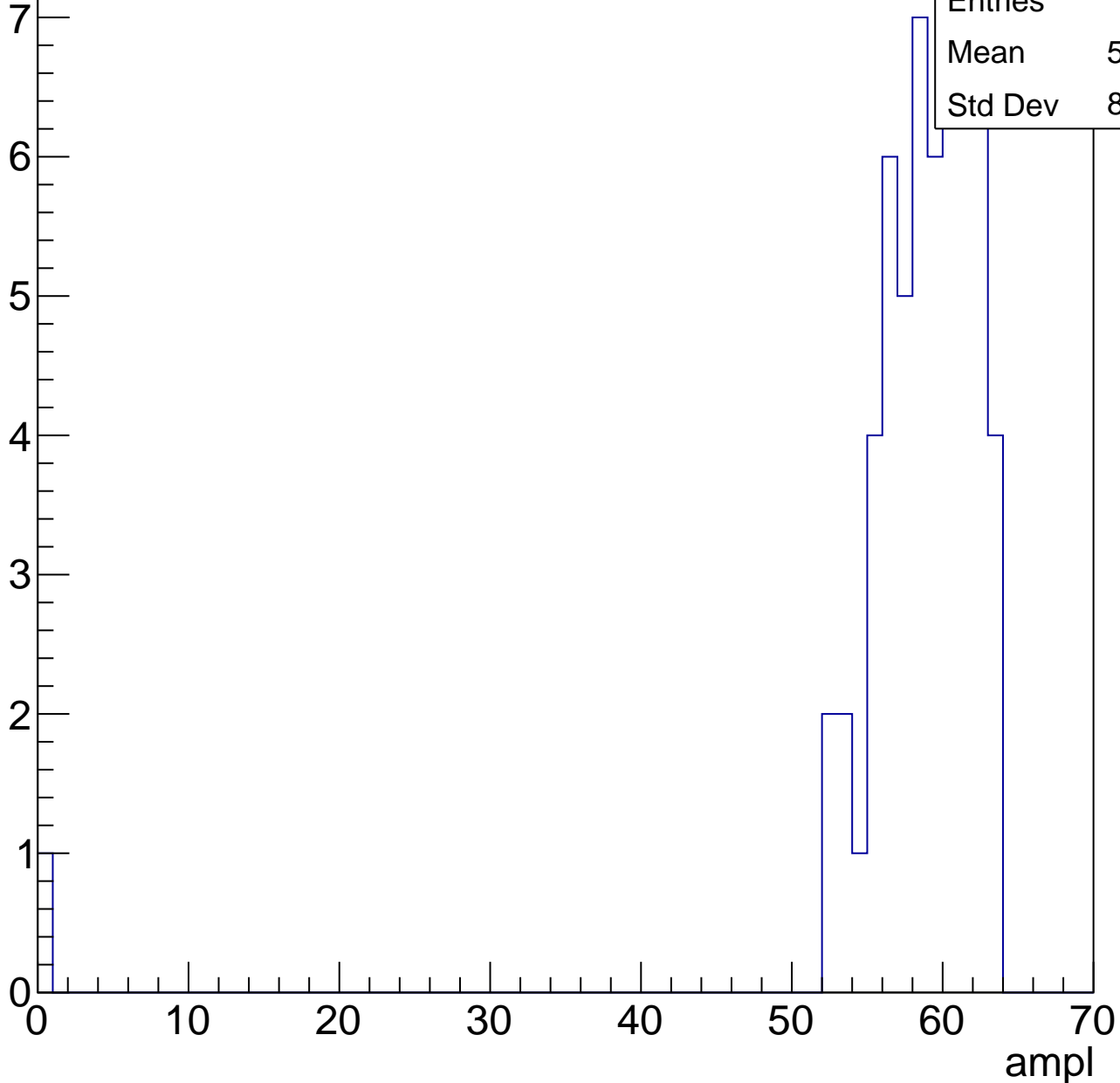


# B1L102S, U21-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	57.59
Std Dev	8.095

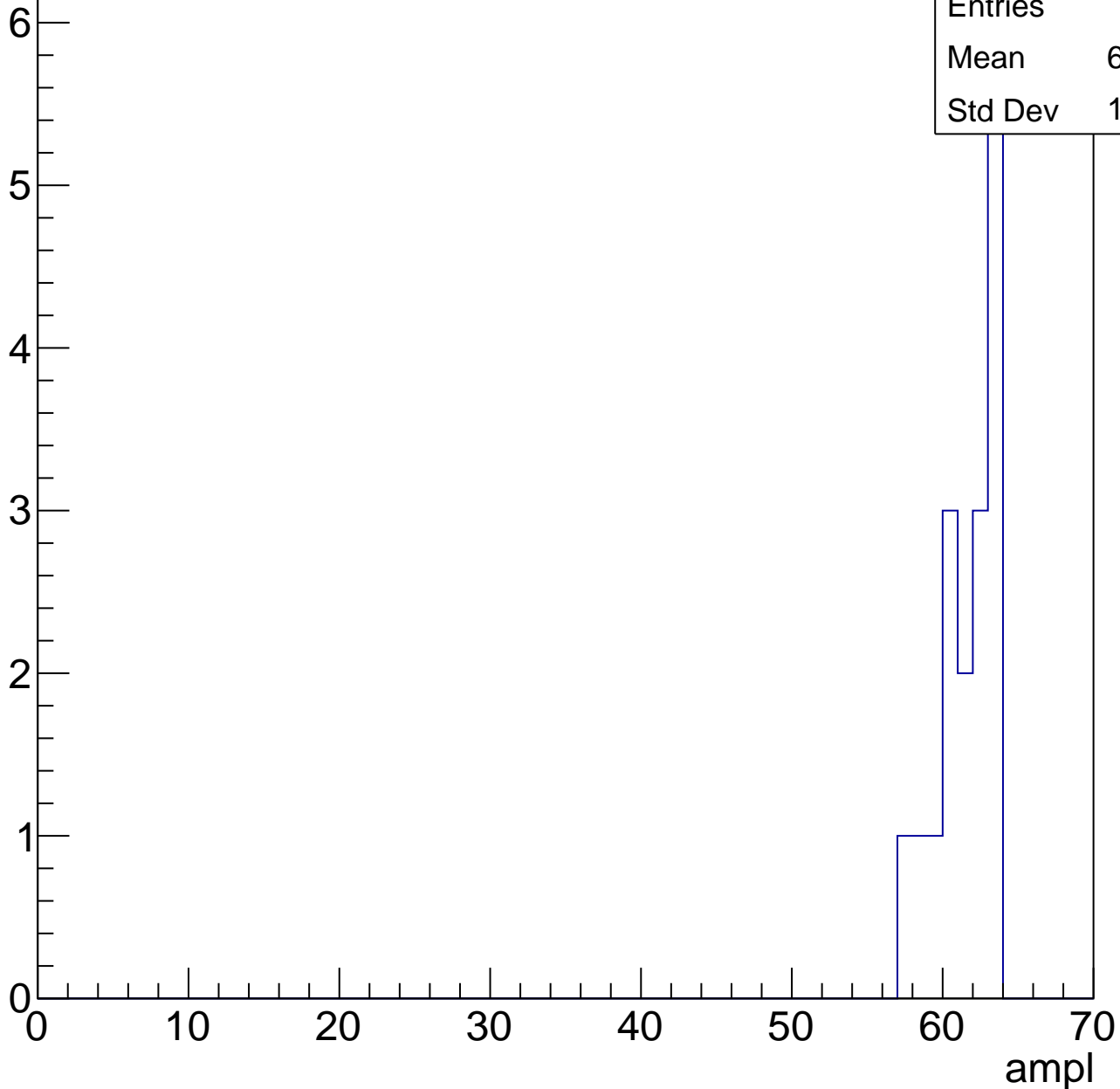


# B1L102S, U21-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	17
Mean	61.18
Std Dev	1.855





# B1L102S, U21-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U21-ch117, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	81
Mean	31.47
Std Dev	4.756

**Gaus mean : 32.3406**

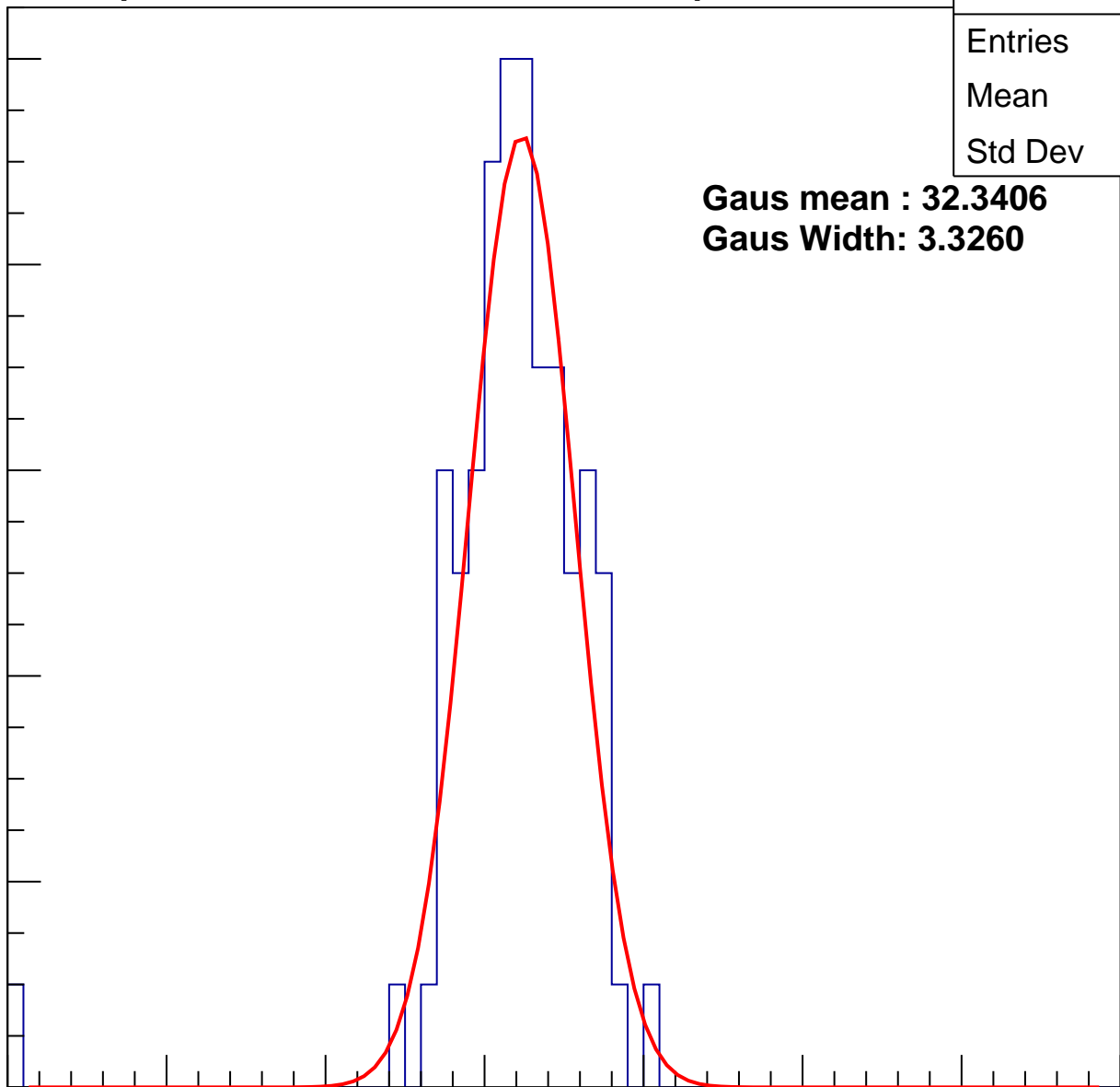
**Gaus Width: 3.3260**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U21-ch117, adc1

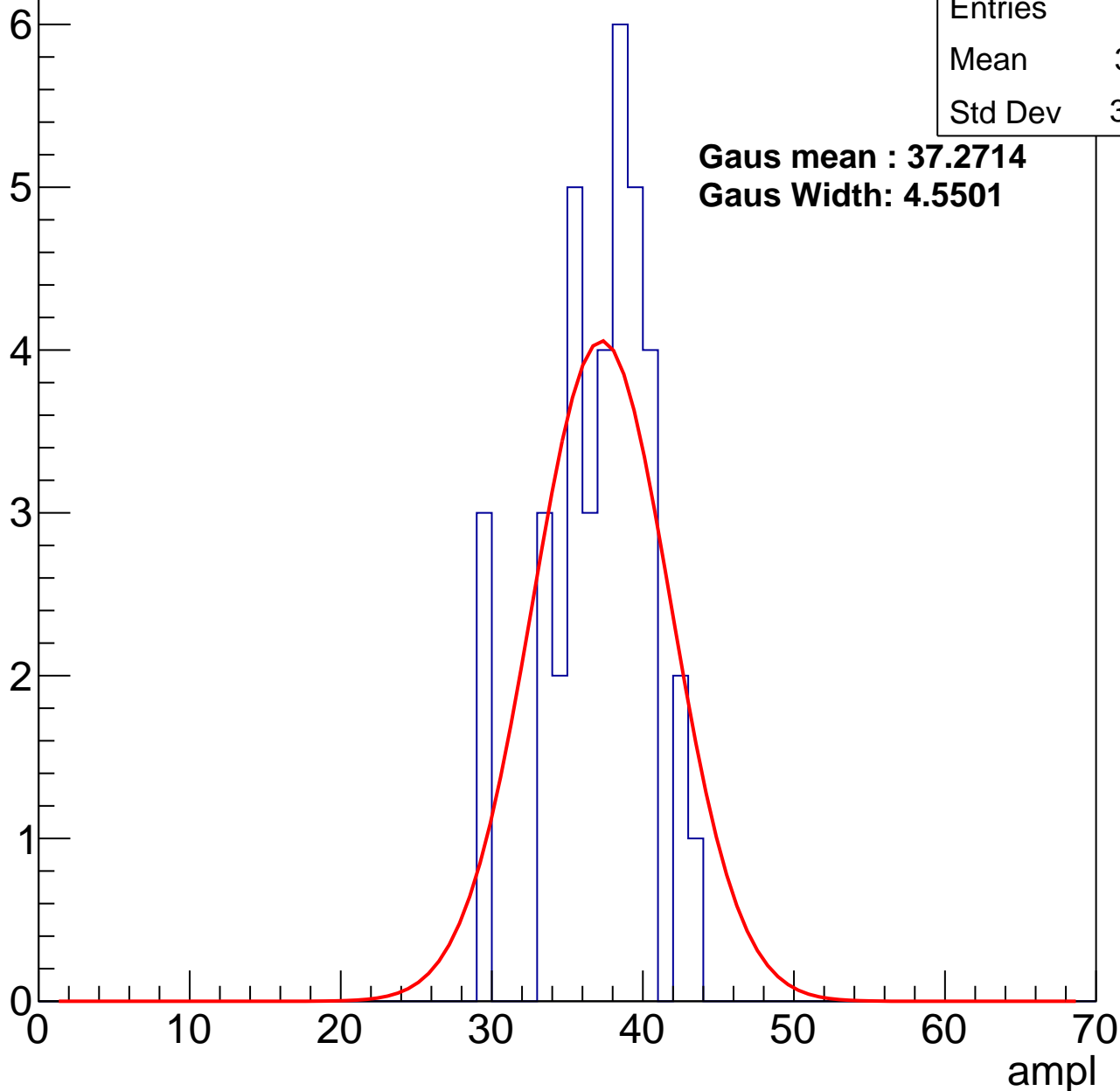
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	38
Mean	36.71
Std Dev	3.347

**Gaus mean : 37.2714**

**Gaus Width: 4.5501**



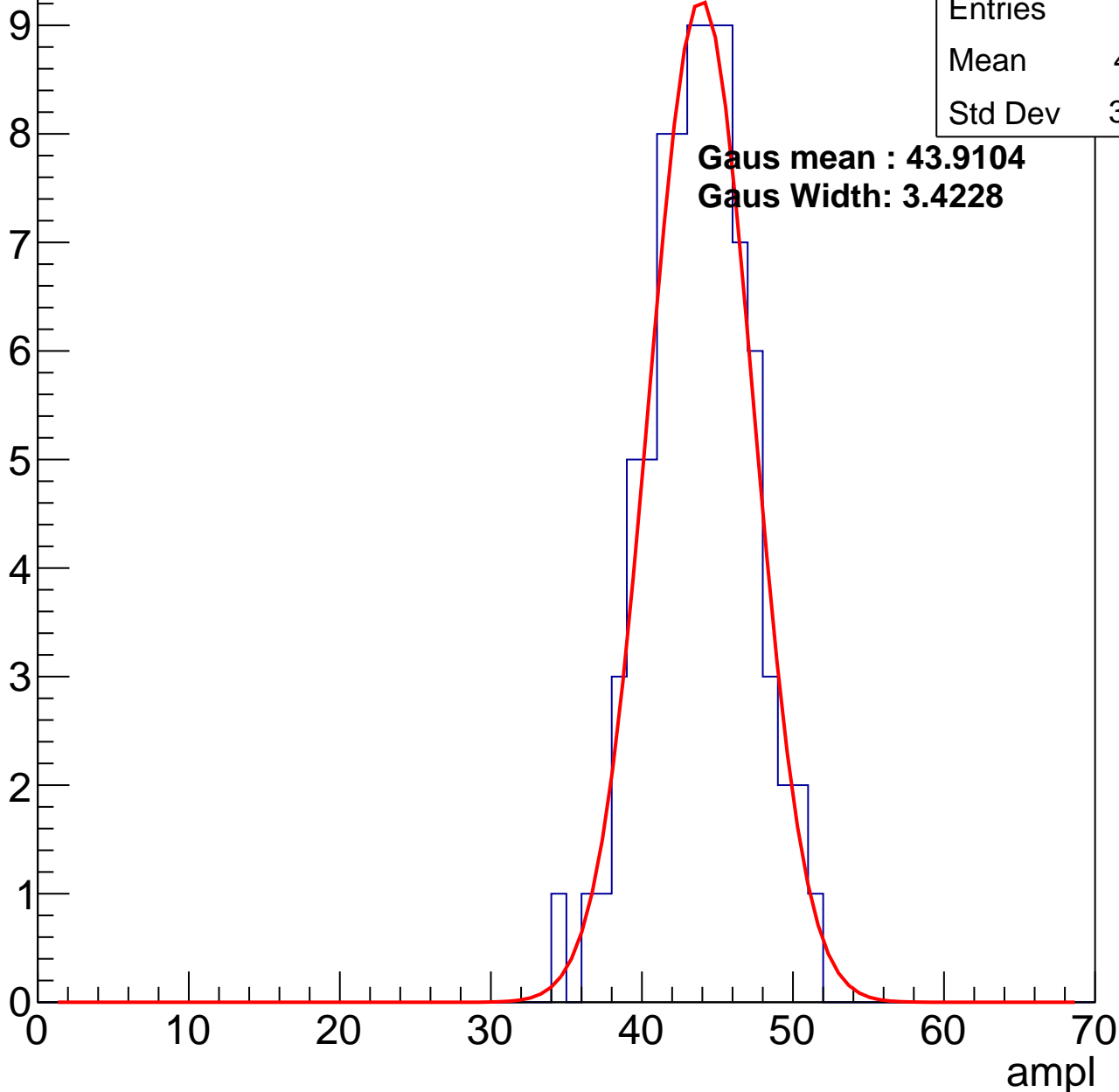
# B1L102S, U21-ch117, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	43.31
Std Dev	3.375

**Gaus mean : 43.9104**  
**Gaus Width: 3.4228**

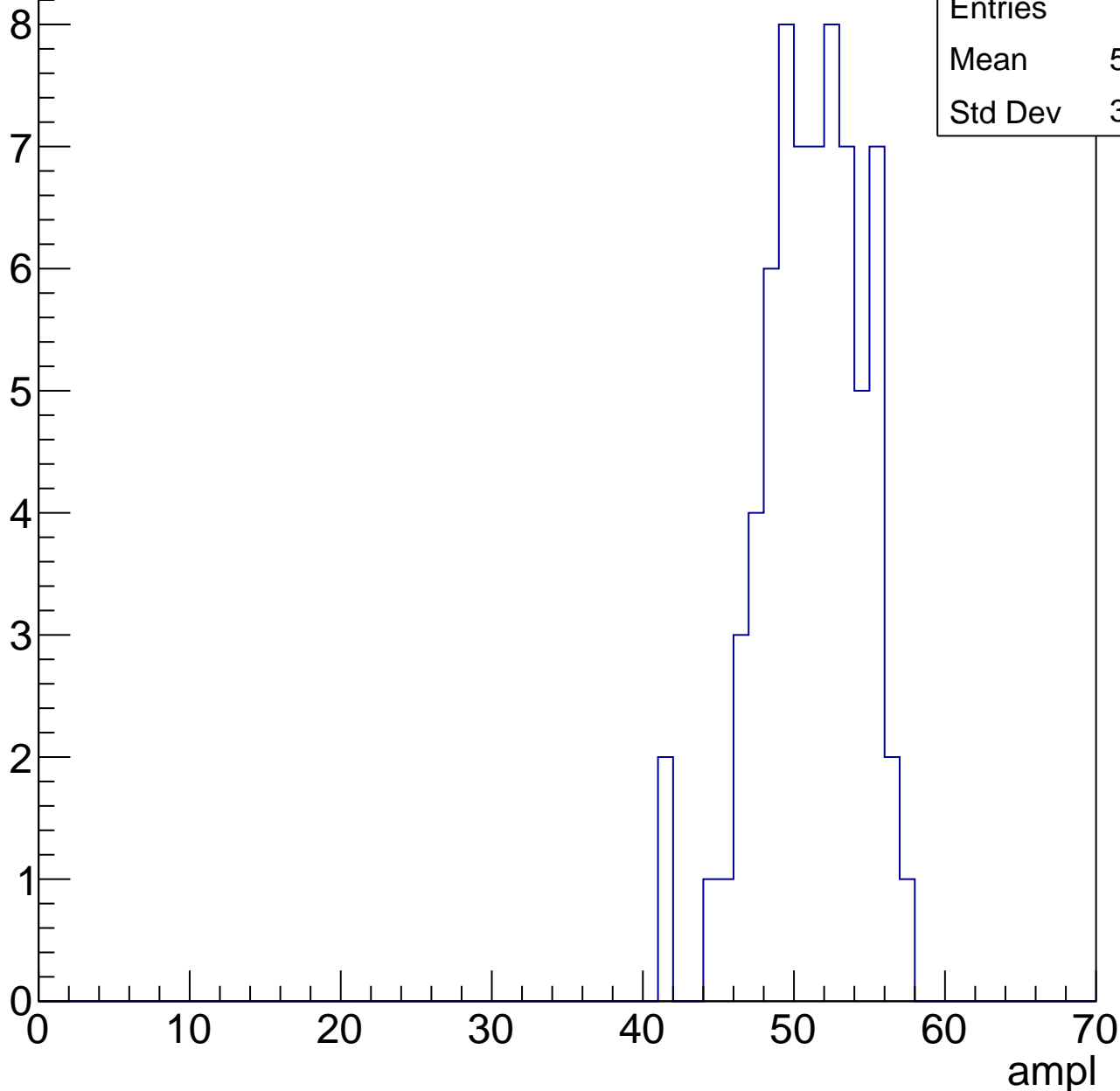


# B1L102S, U21-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	50.65
Std Dev	3.379



# B1L102S, U21-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	65
Mean	56.45
Std Dev	7.79

Entry

10

8

6

4

2

0

0

10

20

30

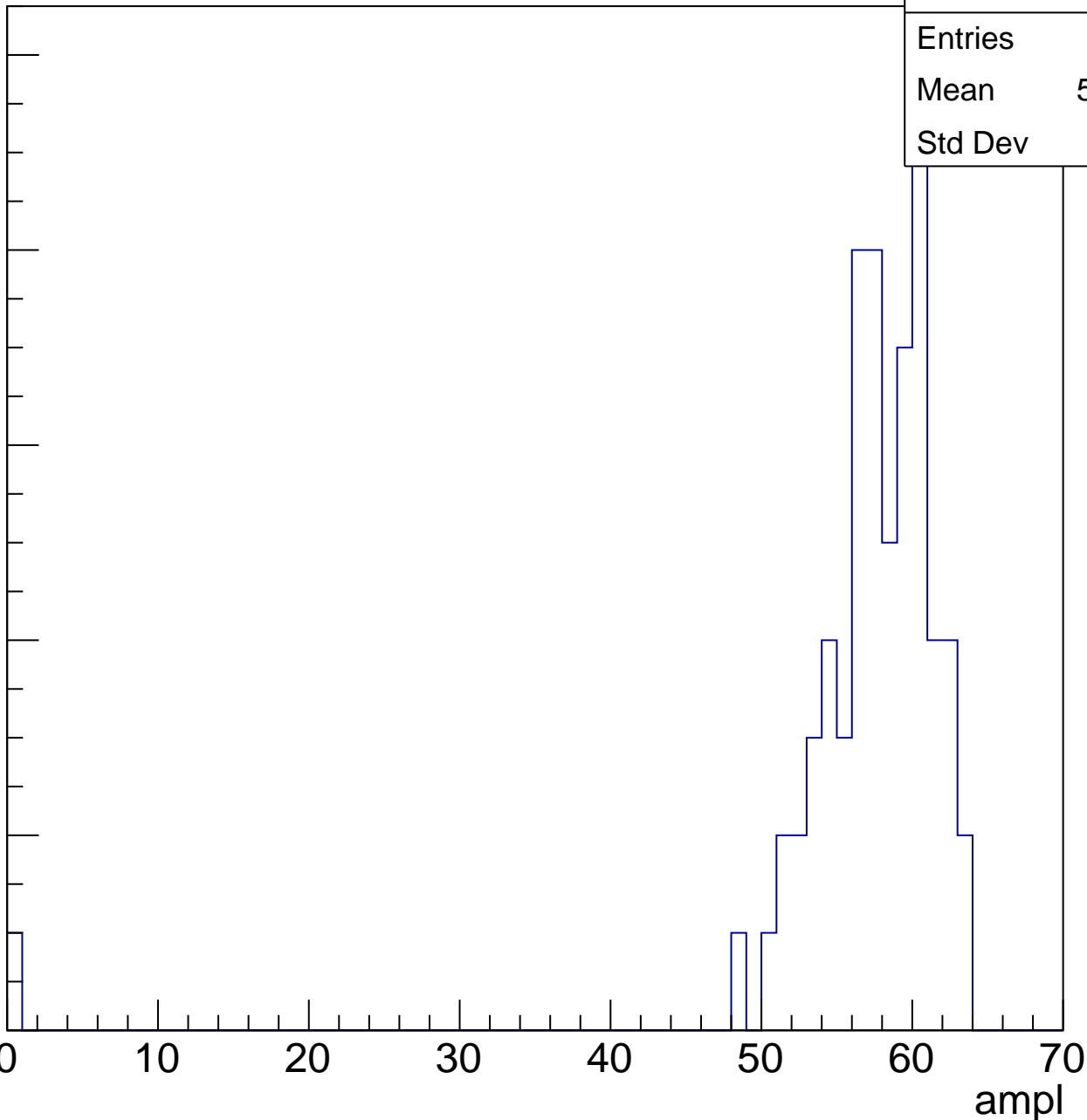
40

50

60

70

ampl

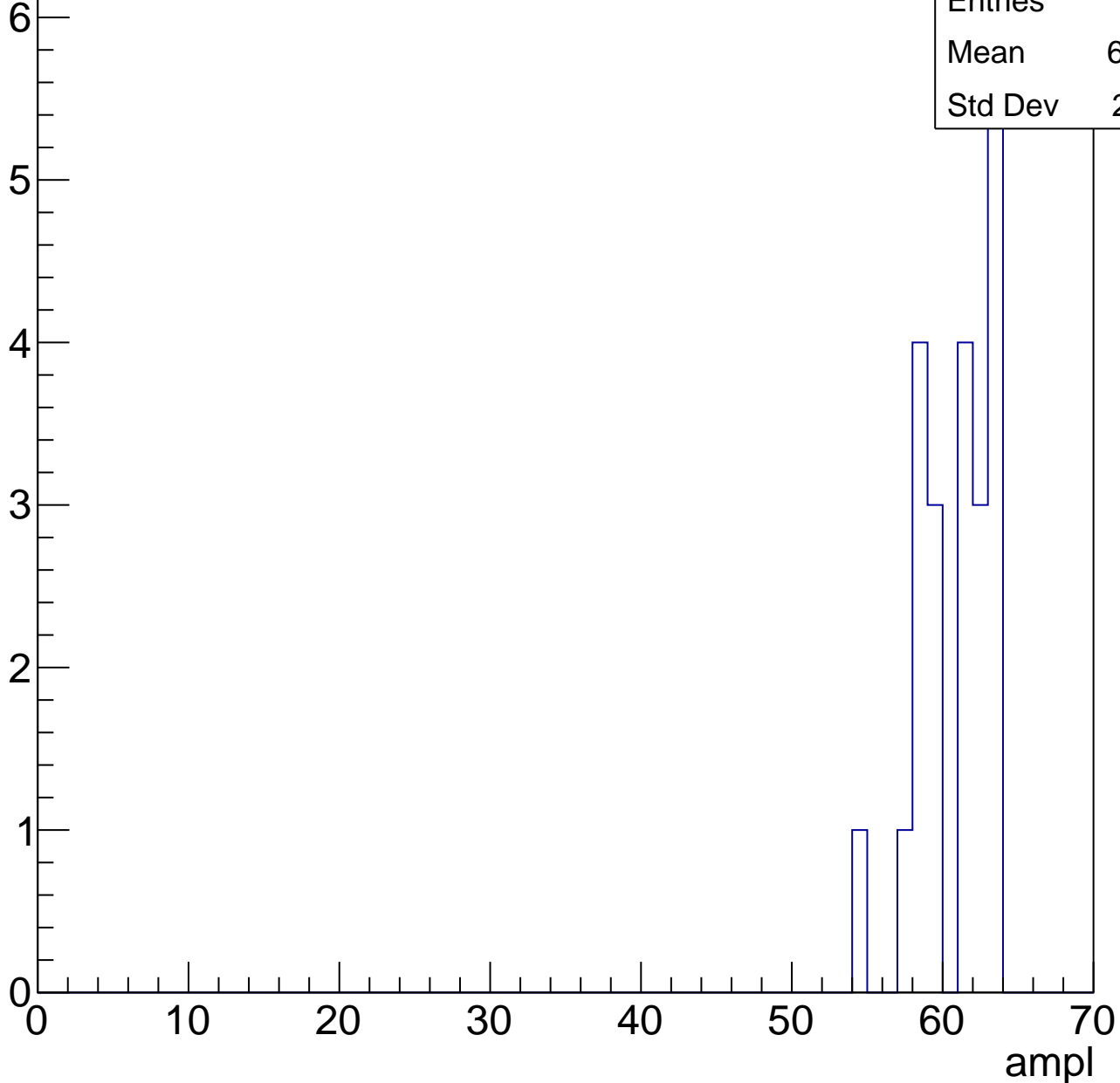


# B1L102S, U21-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

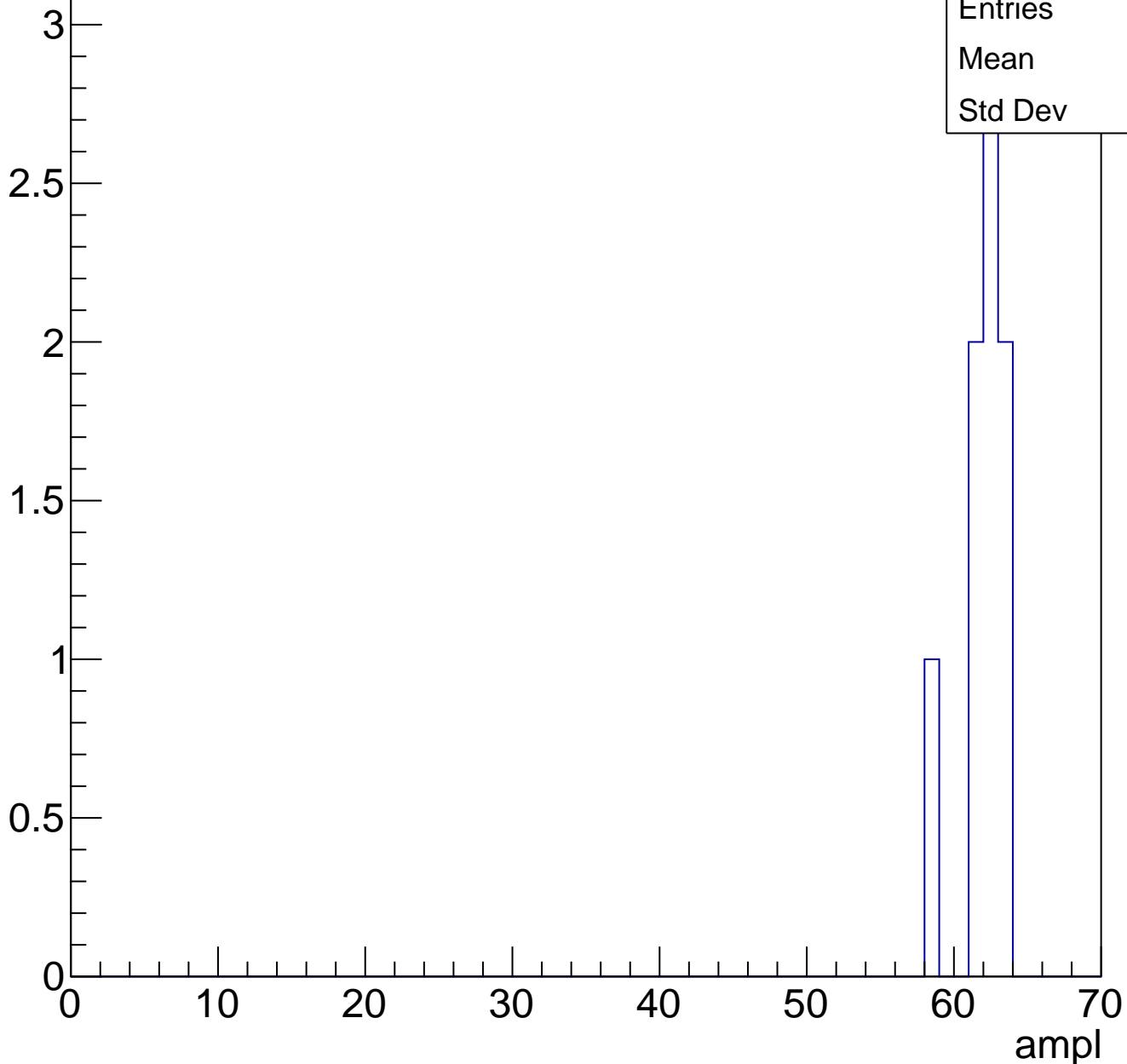
Entries	22
Mean	60.36
Std Dev	2.441



# B1L102S, U21-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch118, adc0

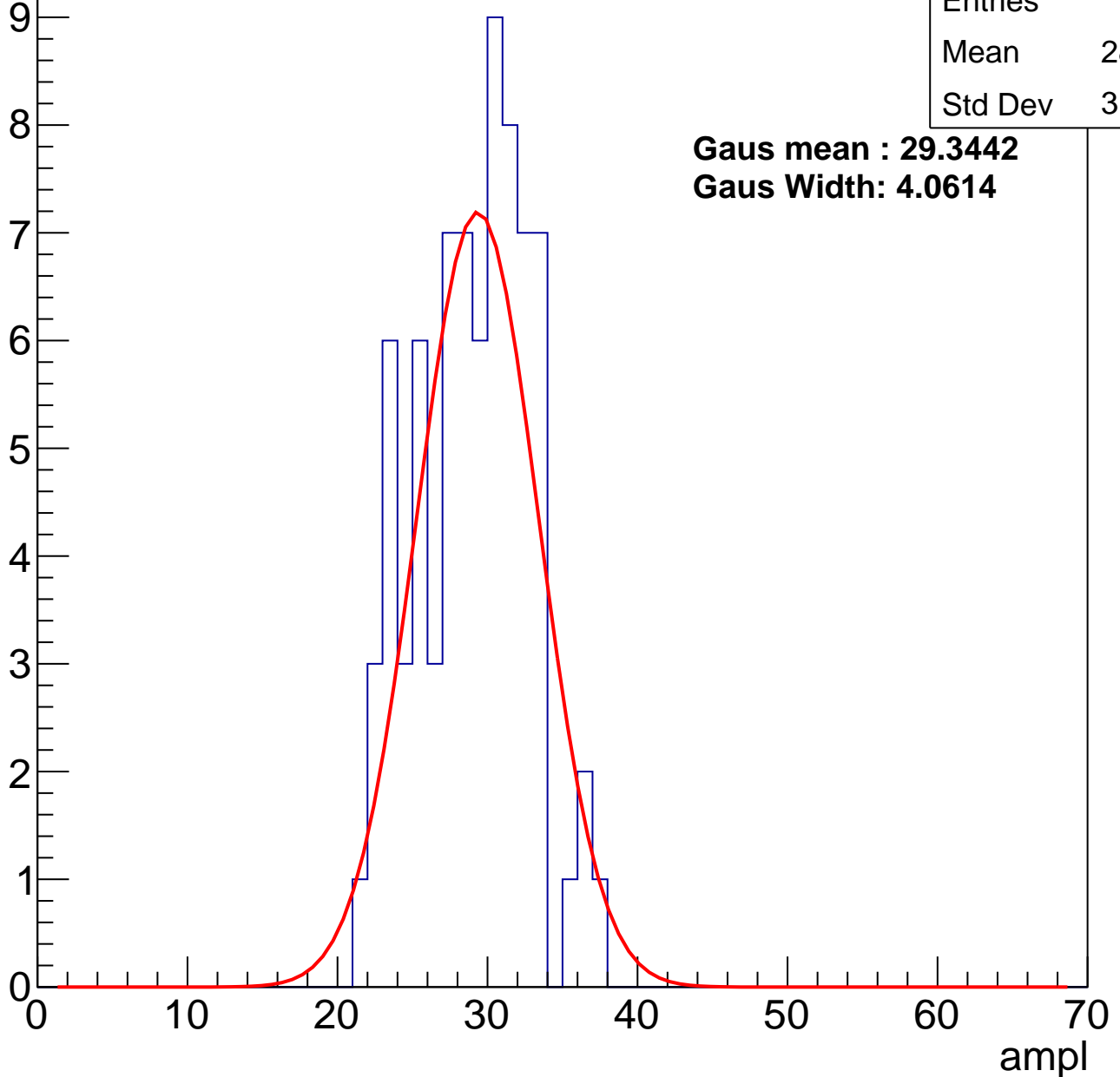
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	28.58
Std Dev	3.712

**Gaus mean : 29.3442**

**Gaus Width: 4.0614**



# B1L102S, U21-ch118, adc1

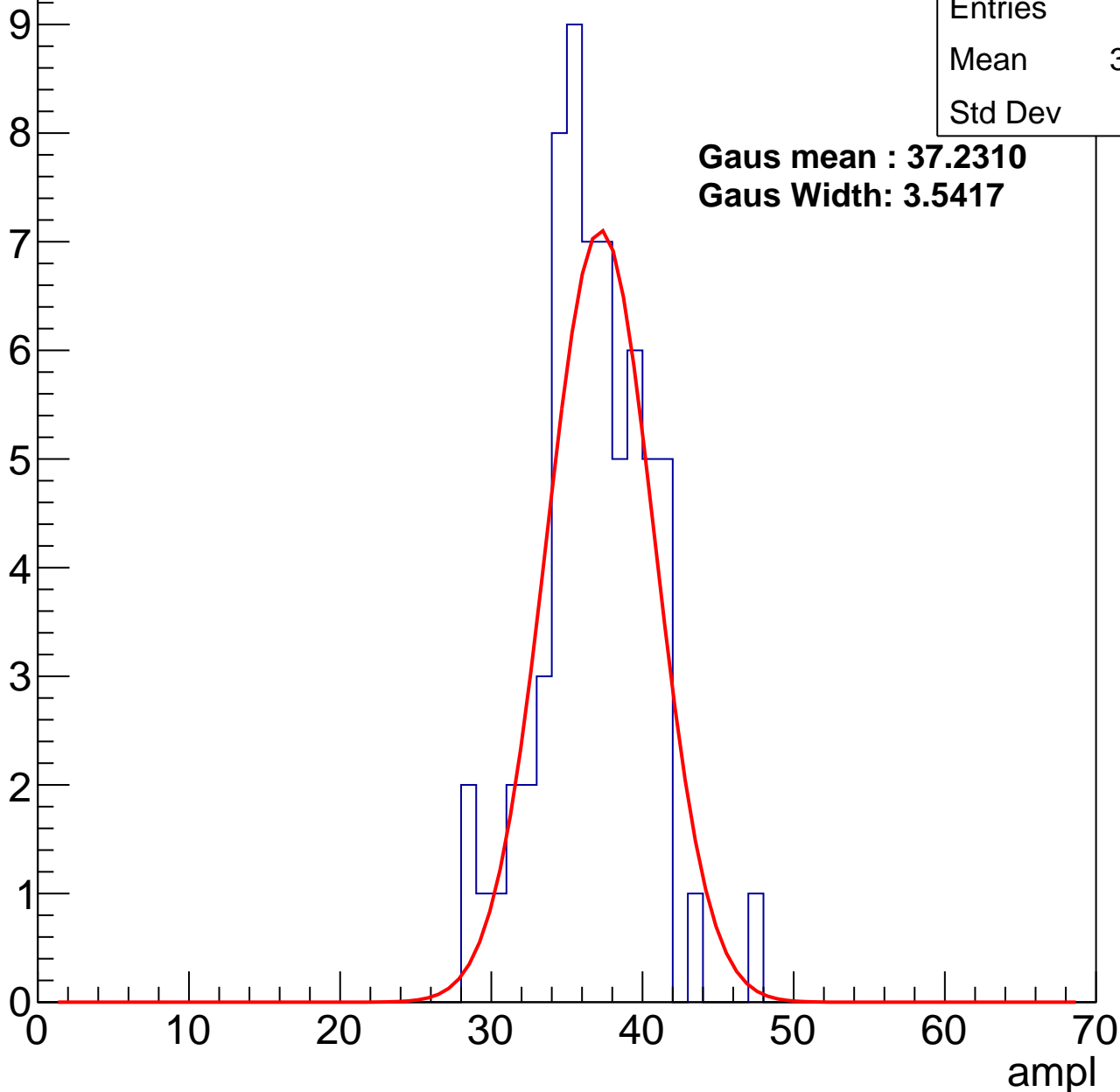
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	36.26
Std Dev	3.54

**Gaus mean : 37.2310**

**Gaus Width: 3.5417**



# B1L102S, U21-ch118, adc2

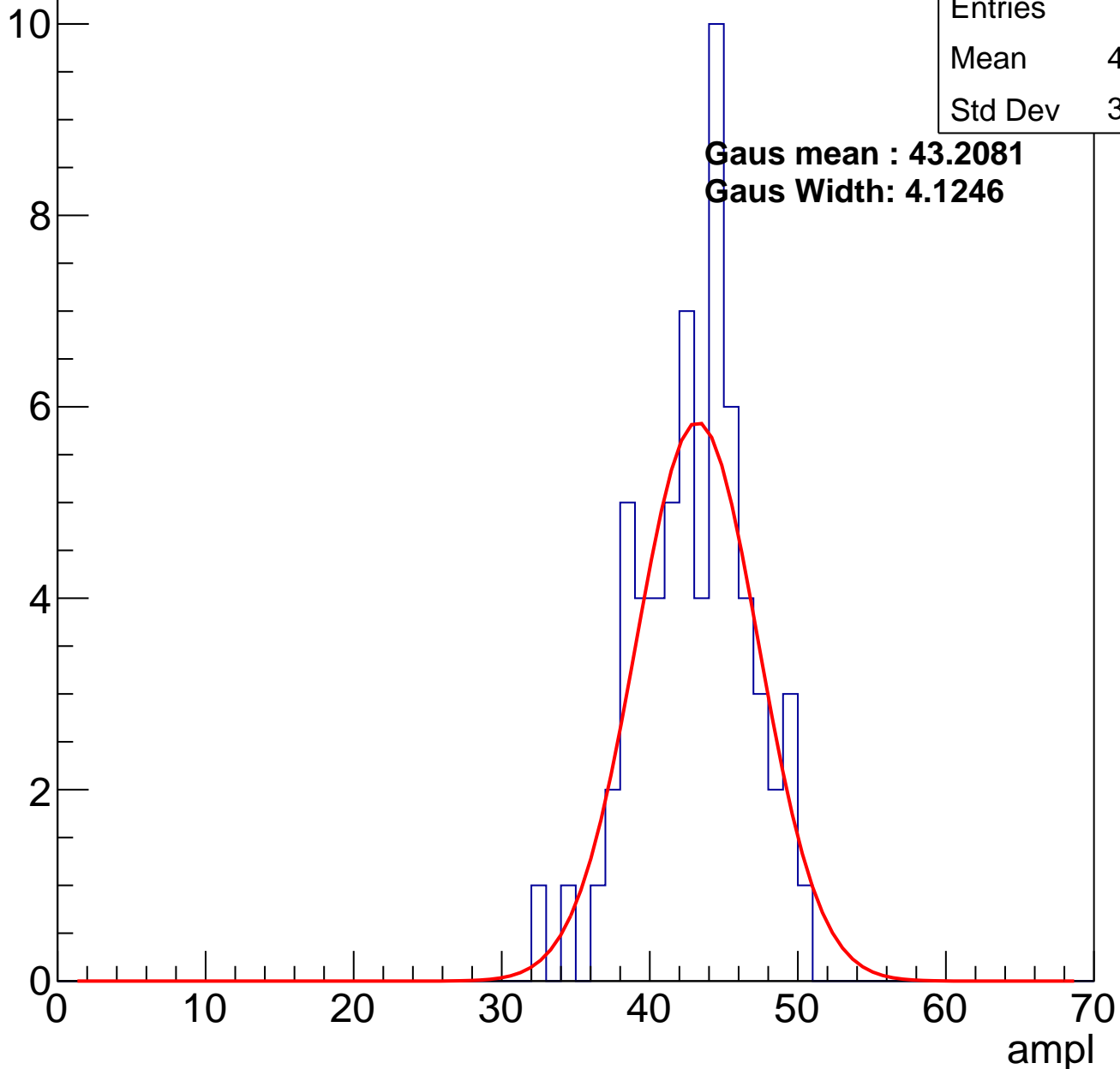
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	63
Mean	42.56
Std Dev	3.753

**Gaus mean : 43.2081**

**Gaus Width: 4.1246**

Entry

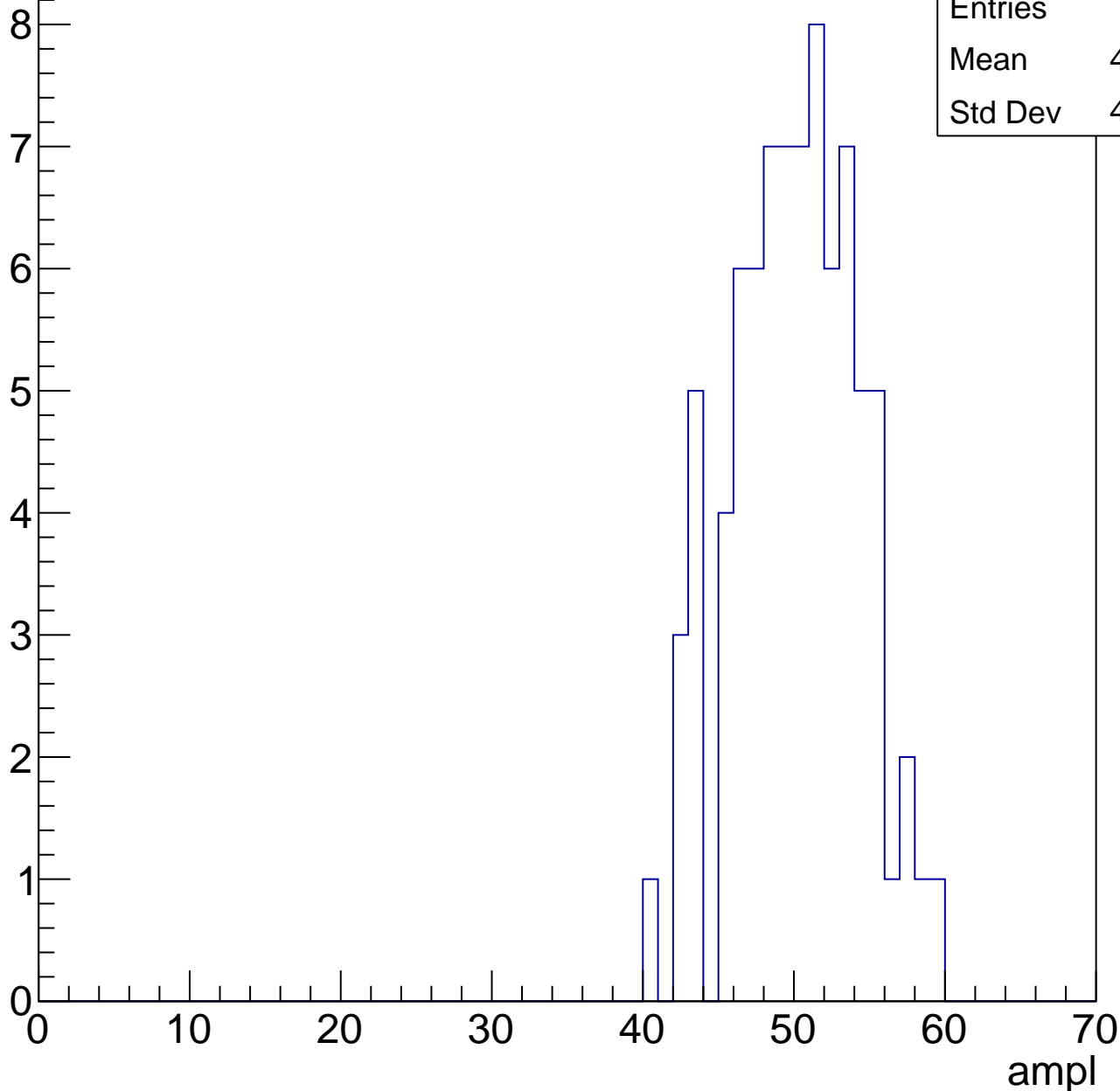


# B1L102S, U21-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	49.65
Std Dev	4.118

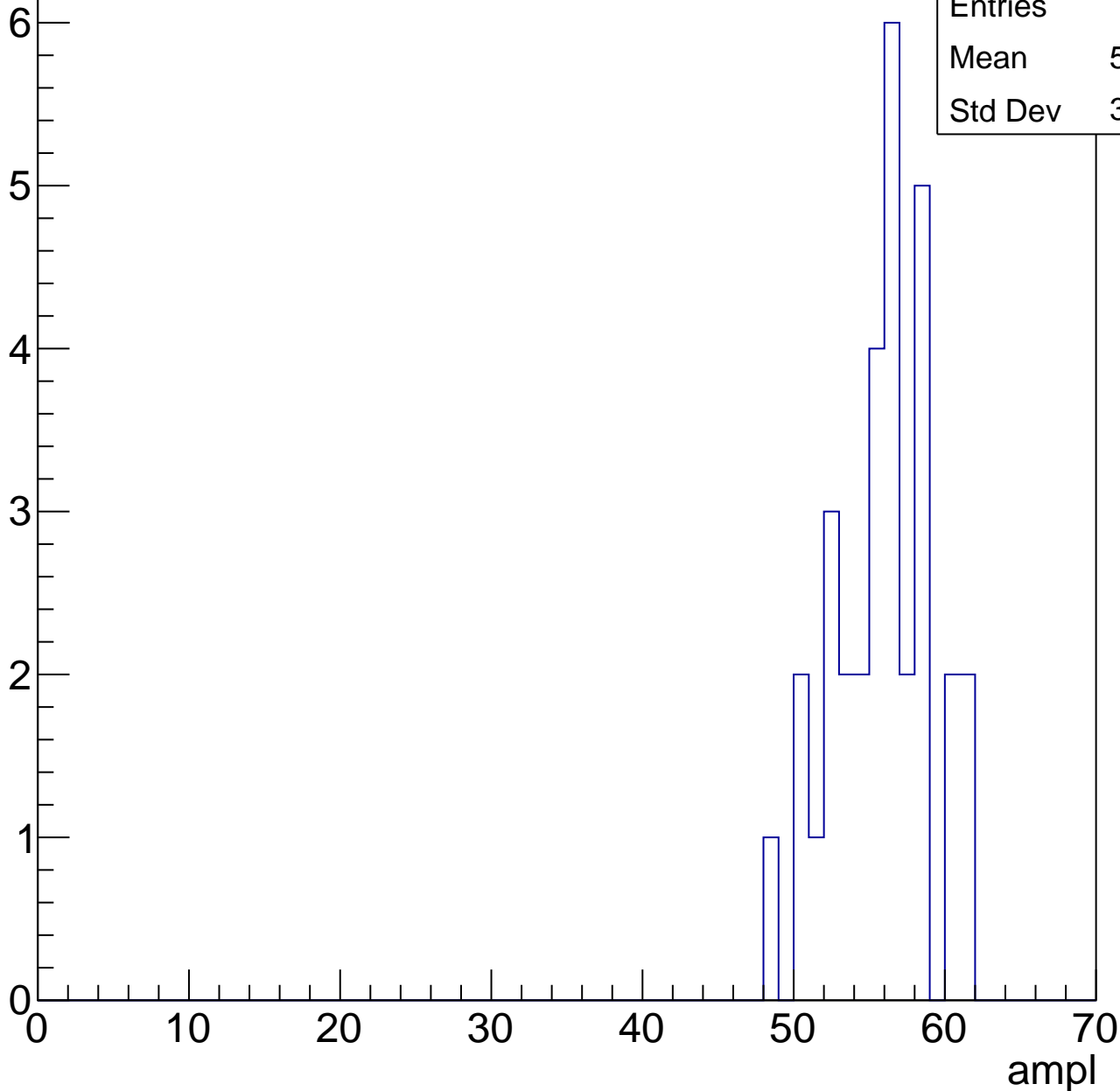


# B1L102S, U21-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	32
Mean	55.34
Std Dev	3.208

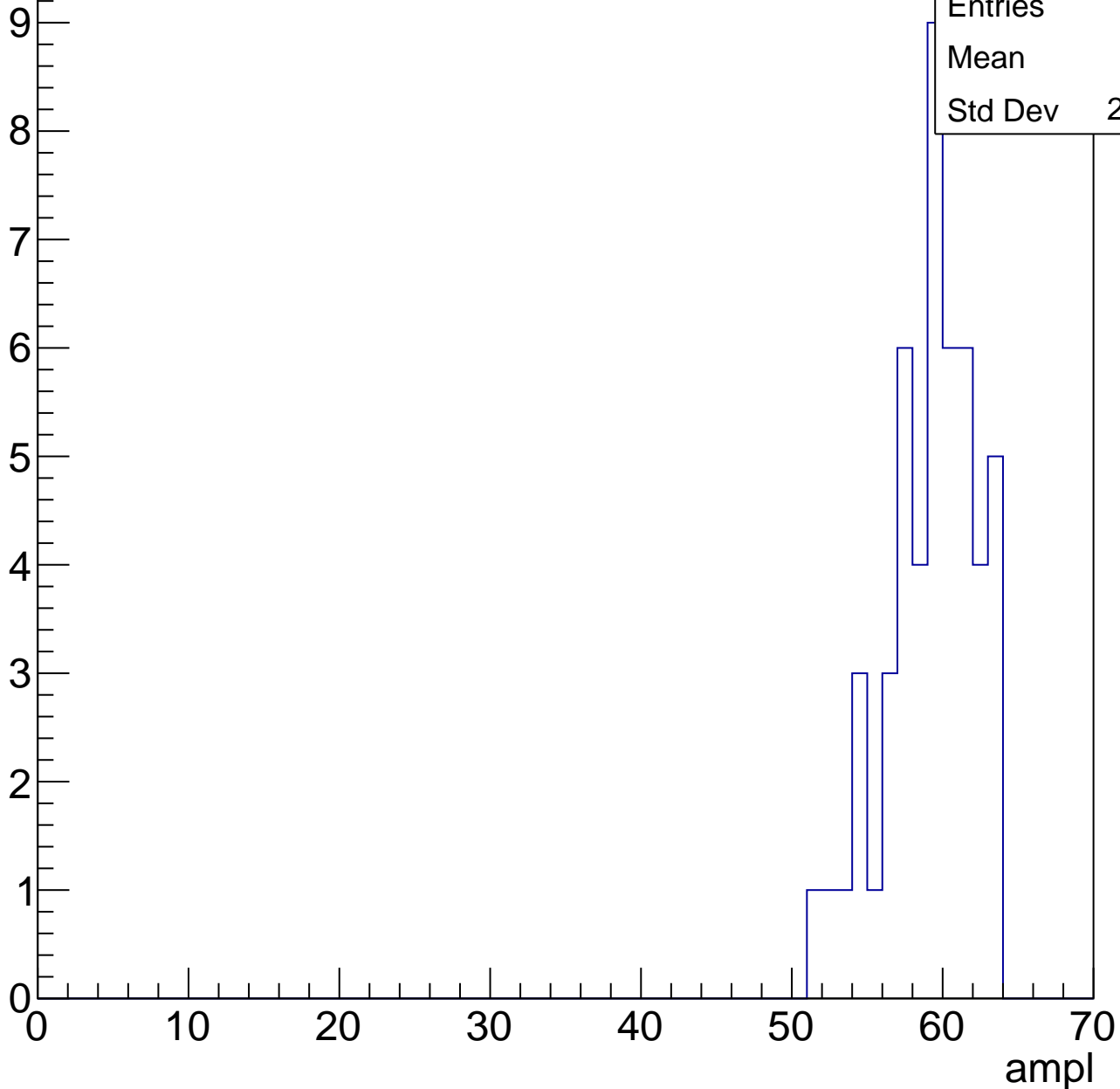


# B1L102S, U21-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	58.7
Std Dev	2.955

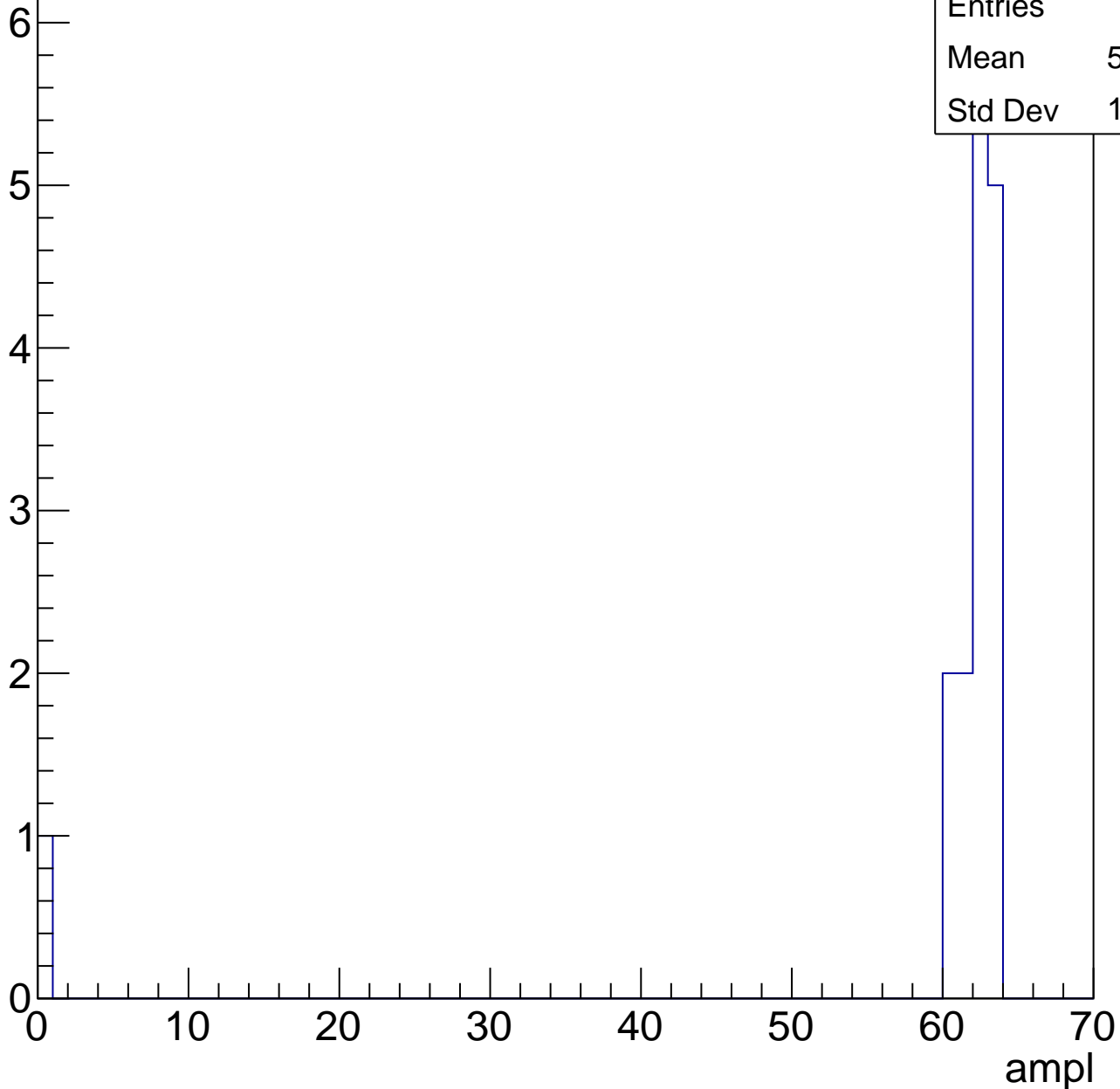


# B1L102S, U21-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	16
Mean	58.06
Std Dev	15.02





# B1L102S, U21-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U21-ch119, adc0

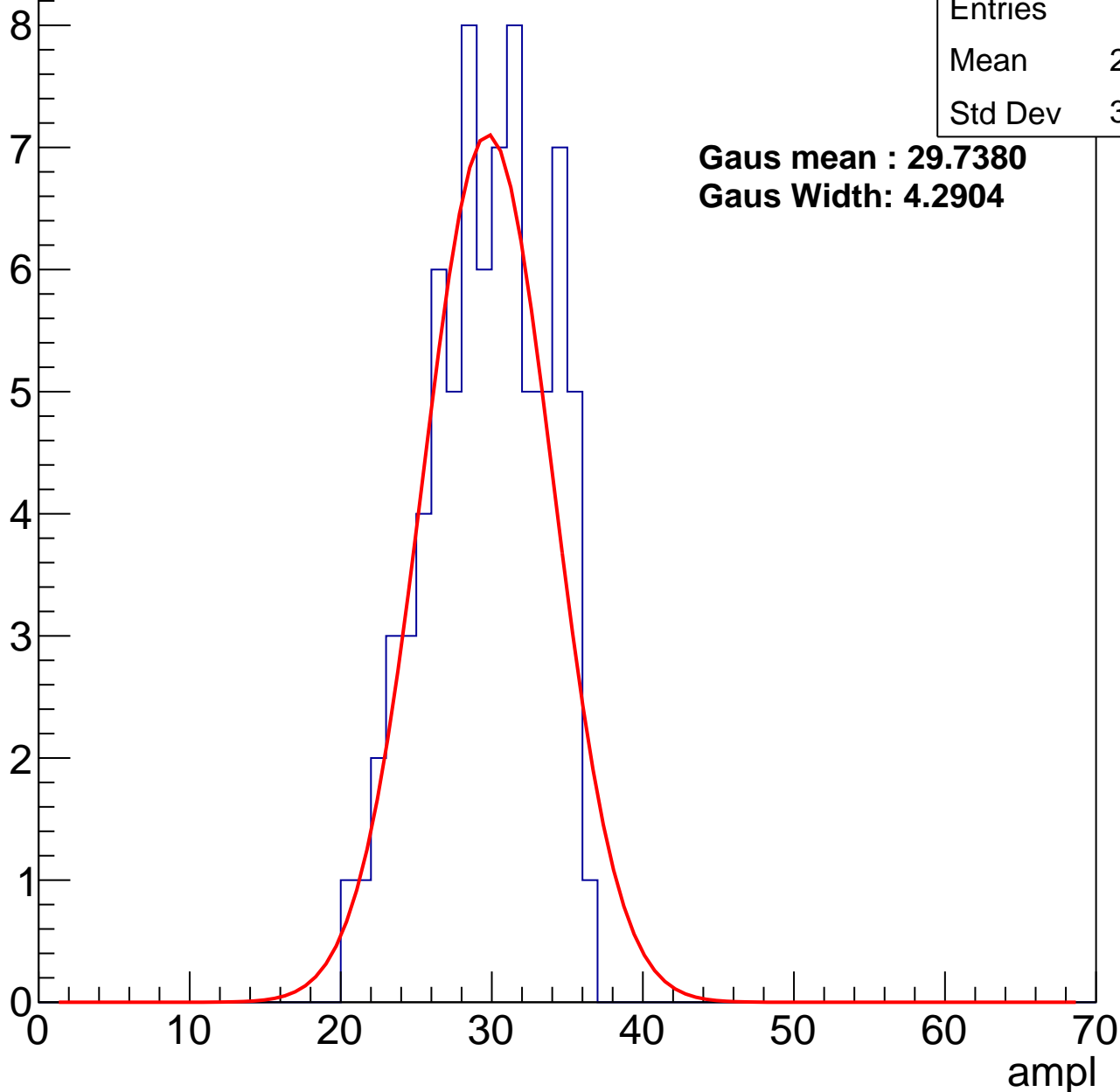
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	29.18
Std Dev	3.843

**Gaus mean : 29.7380**

**Gaus Width: 4.2904**



# B1L102S, U21-ch119, adc1

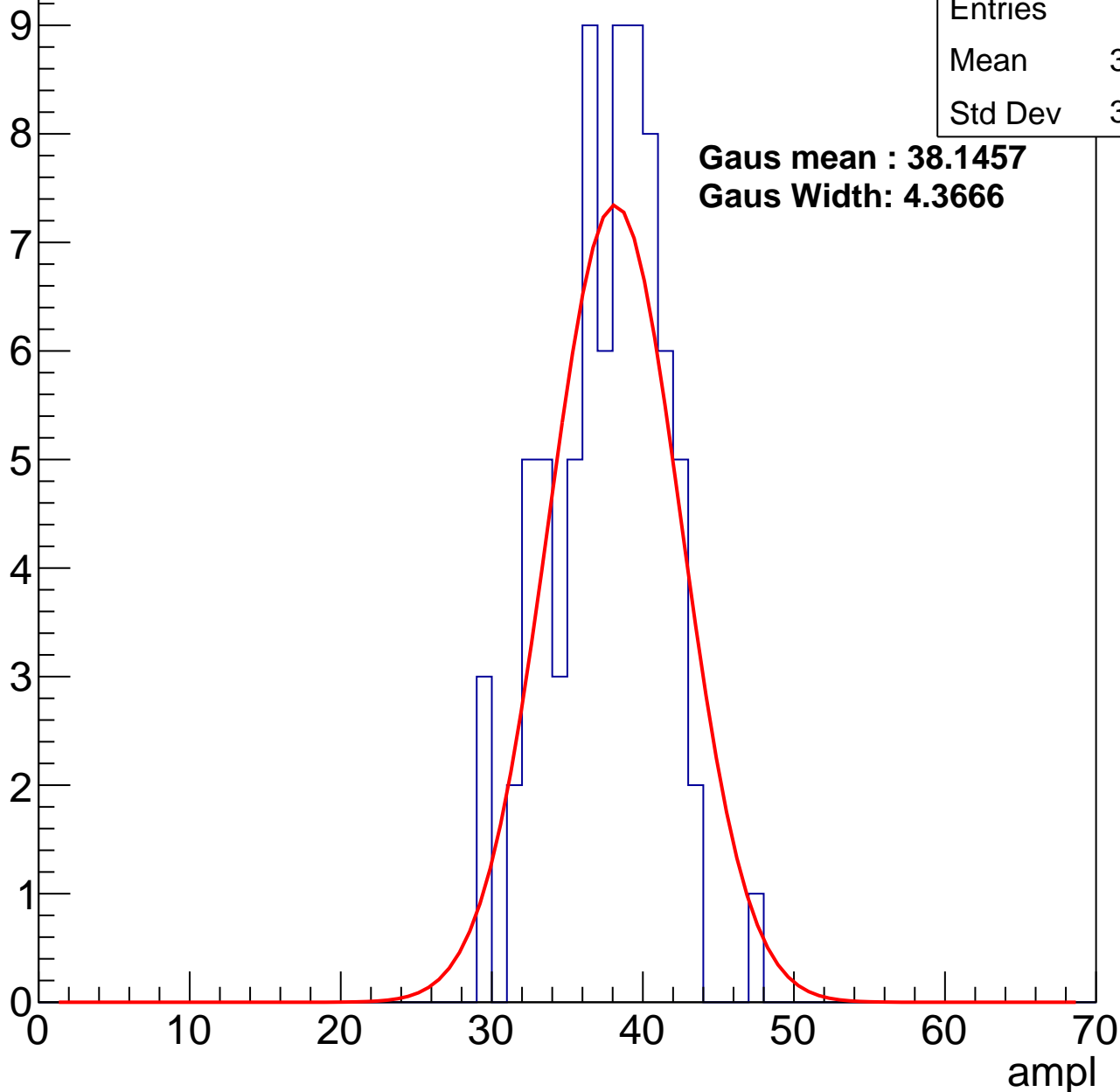
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	37.17
Std Dev	3.639

**Gaus mean : 38.1457**

**Gaus Width: 4.3666**



# B1L102S, U21-ch119, adc2

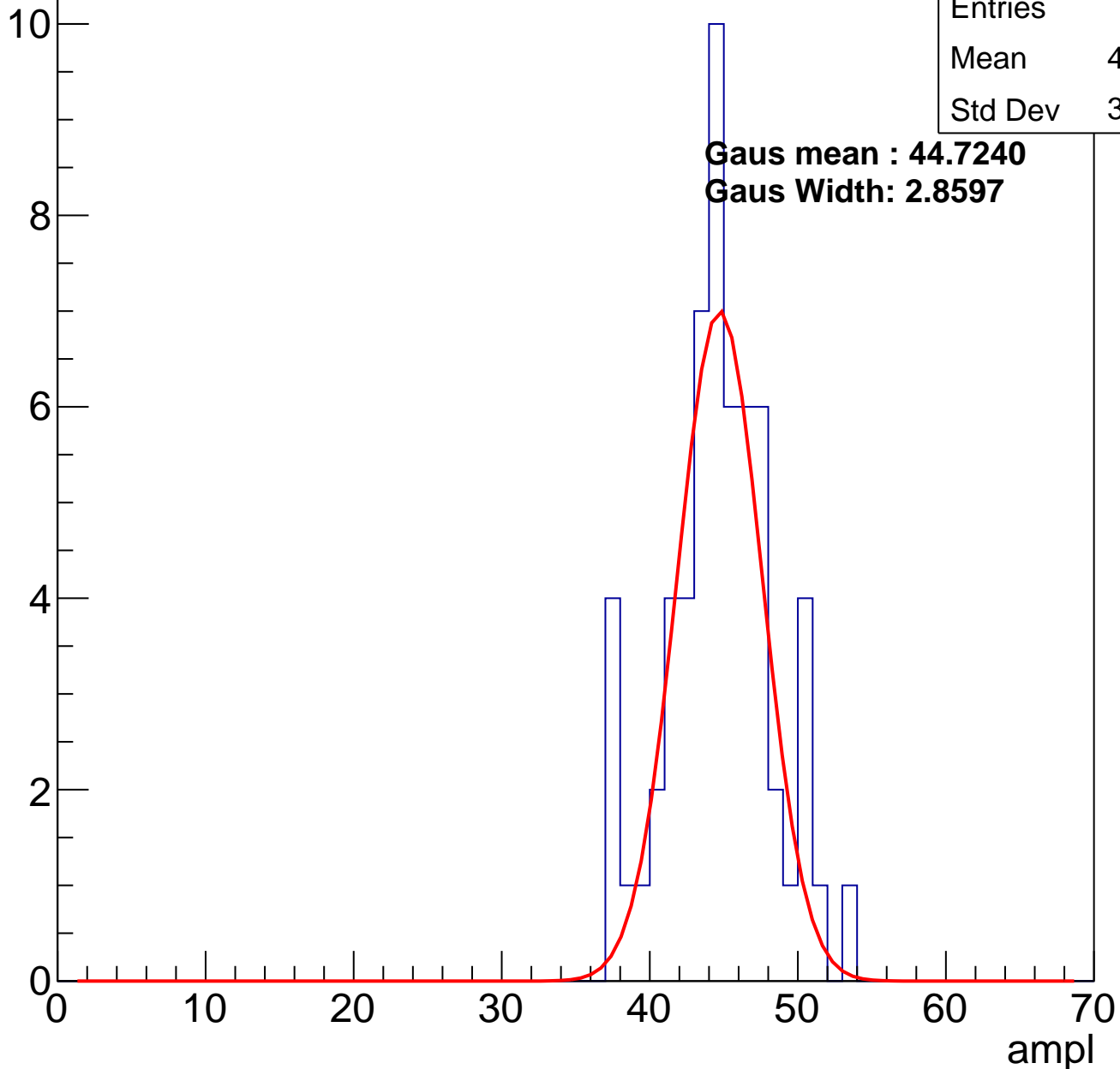
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	60
Mean	44.25
Std Dev	3.557

**Gaus mean : 44.7240**

**Gaus Width: 2.8597**

Entry

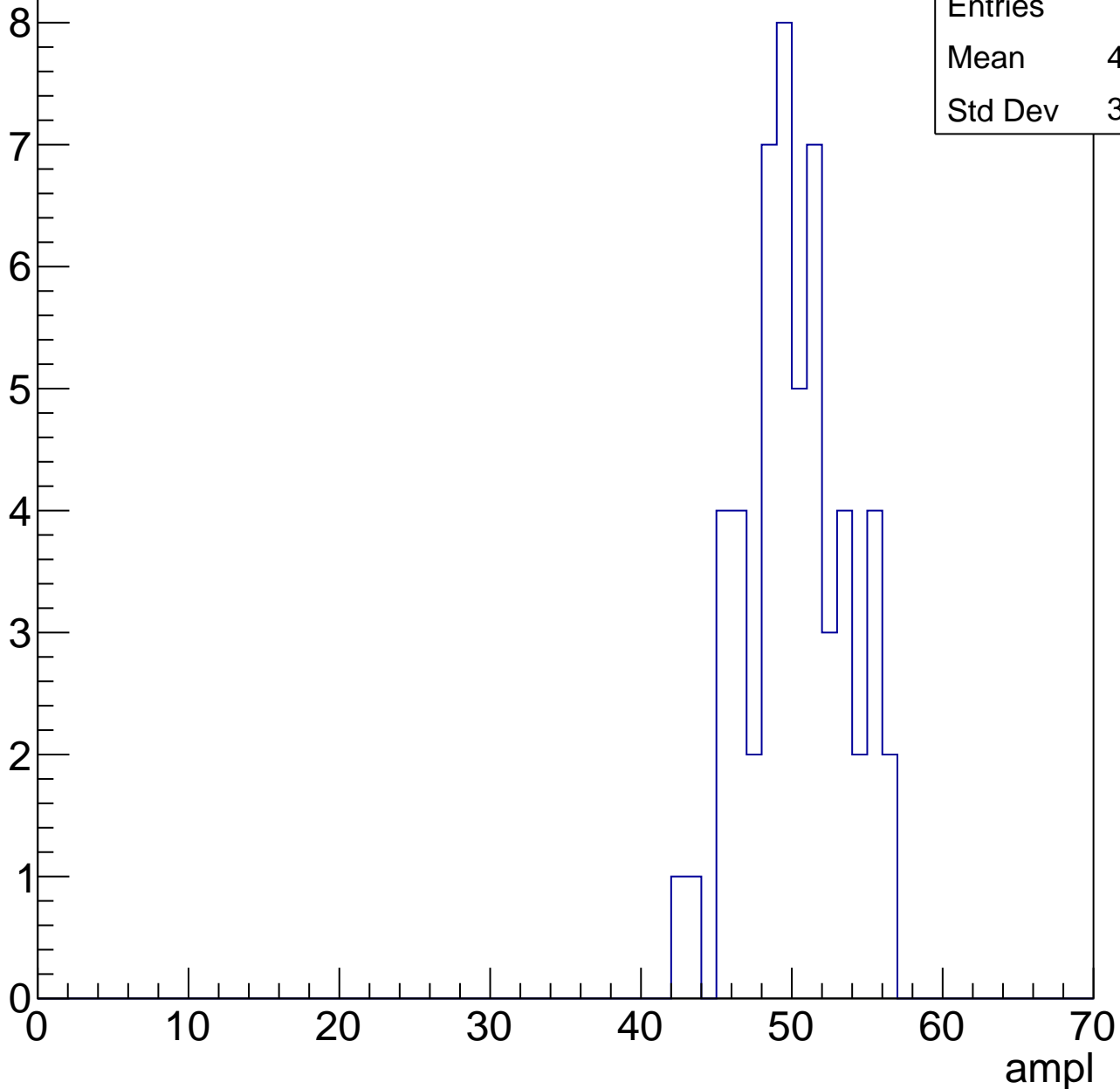


# B1L102S, U21-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	49.74
Std Dev	3.295

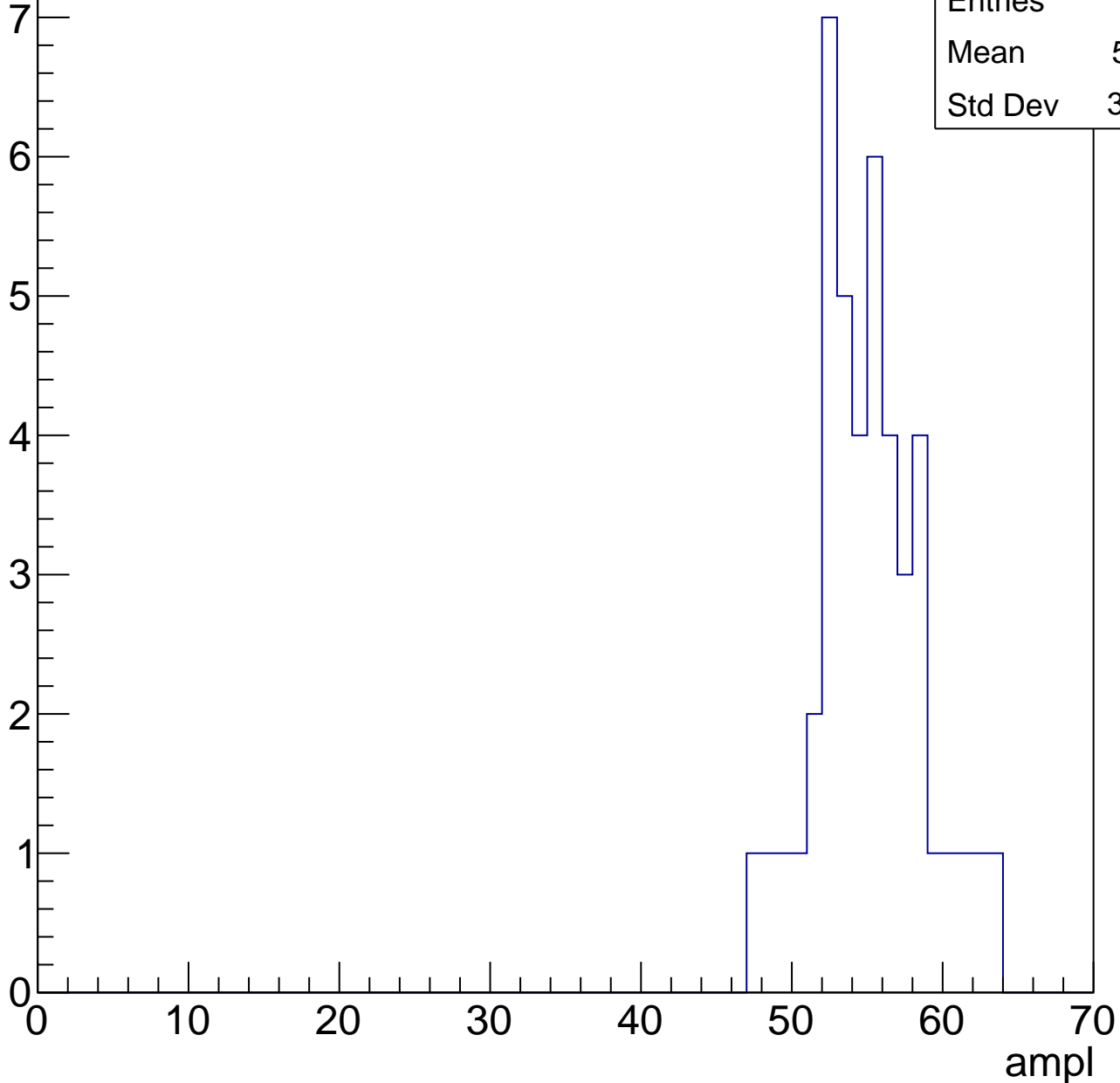


# B1L102S, U21-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	44
Mean	54.61
Std Dev	3.466

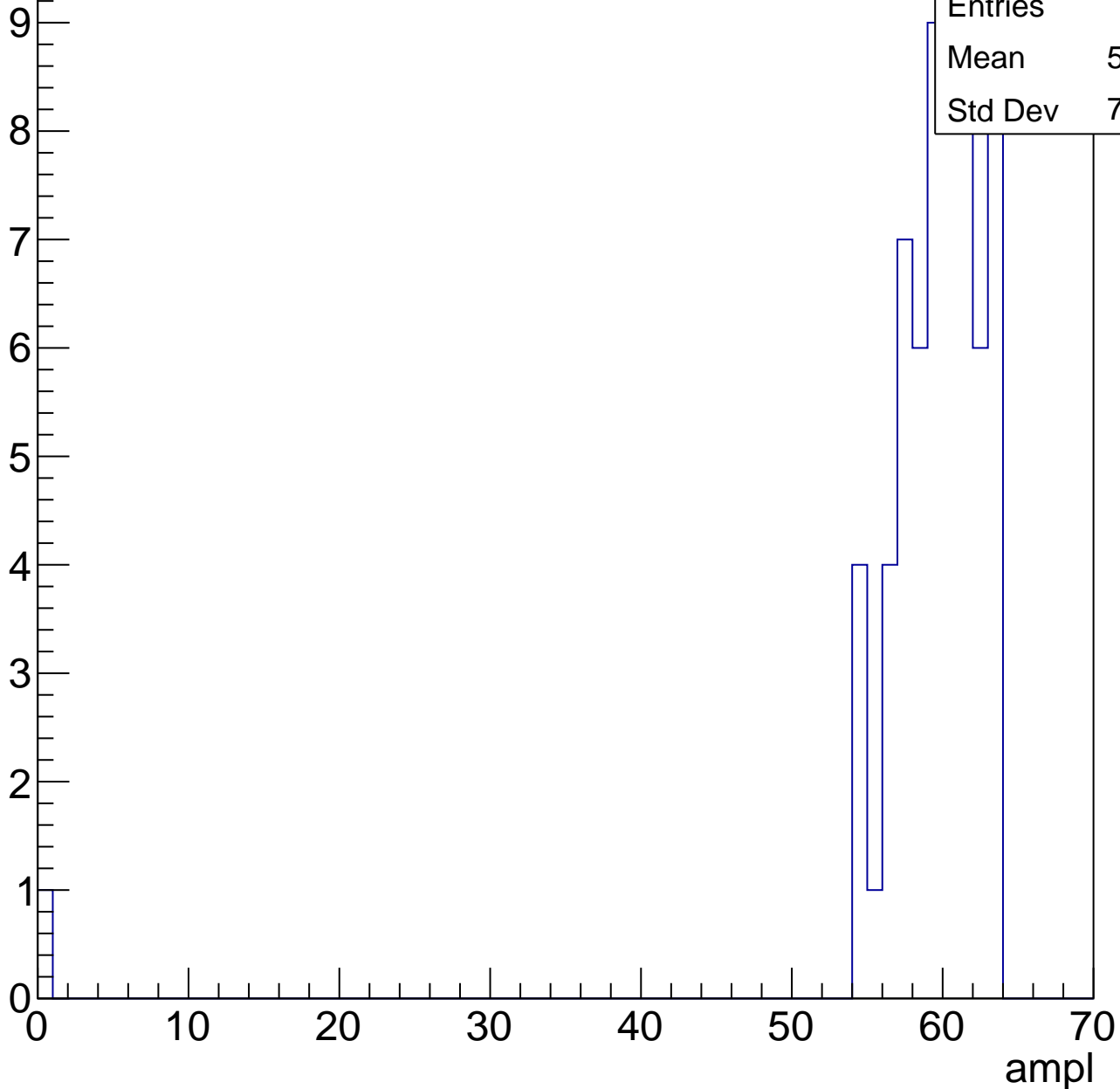


# B1L102S, U21-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	58.48
Std Dev	7.738



# B1L102S, U21-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U21-ch120, adc0

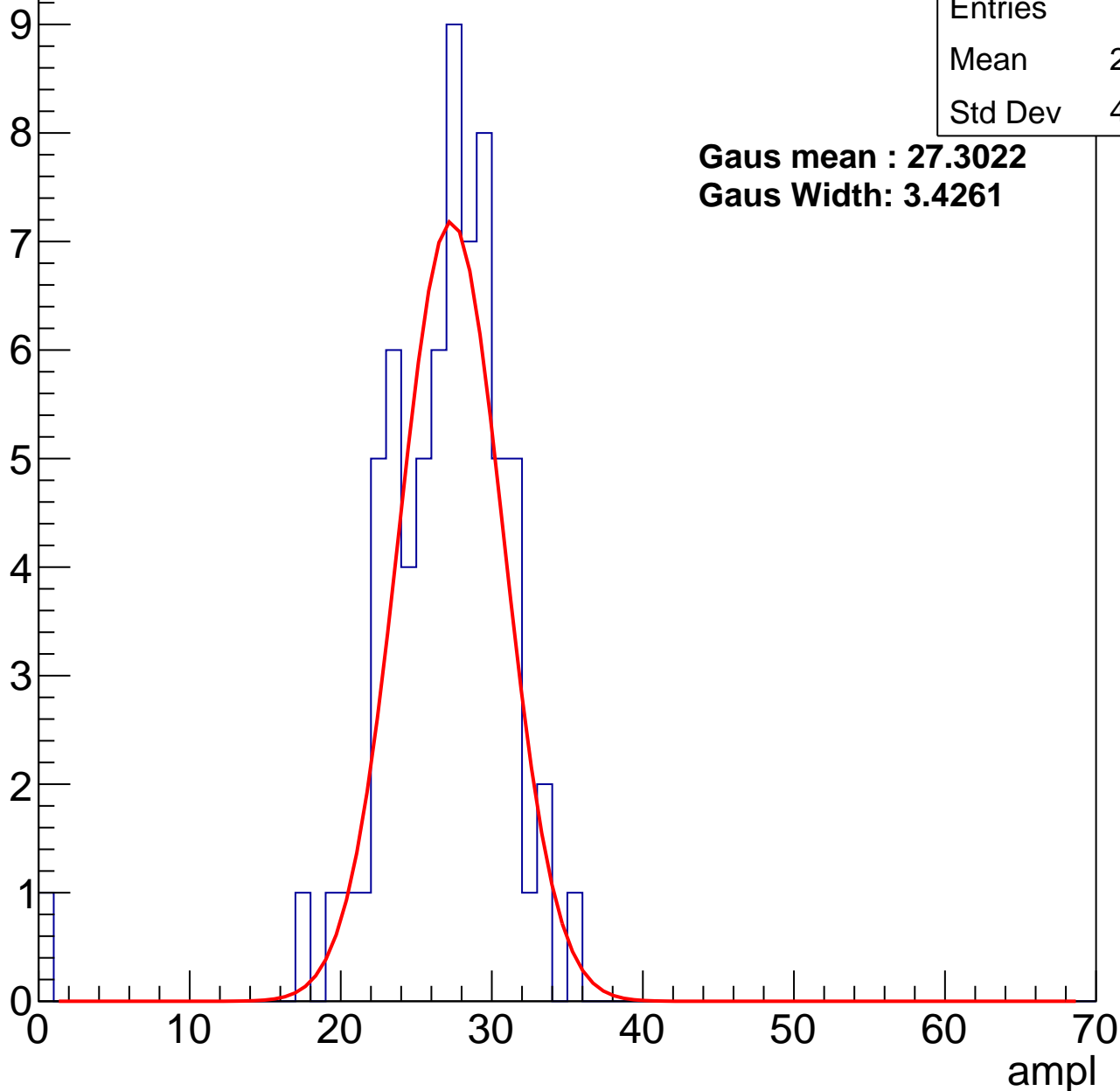
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	26.25
Std Dev	4.735

**Gaus mean : 27.3022**

**Gaus Width: 3.4261**



# B1L102S, U21-ch120, adc1

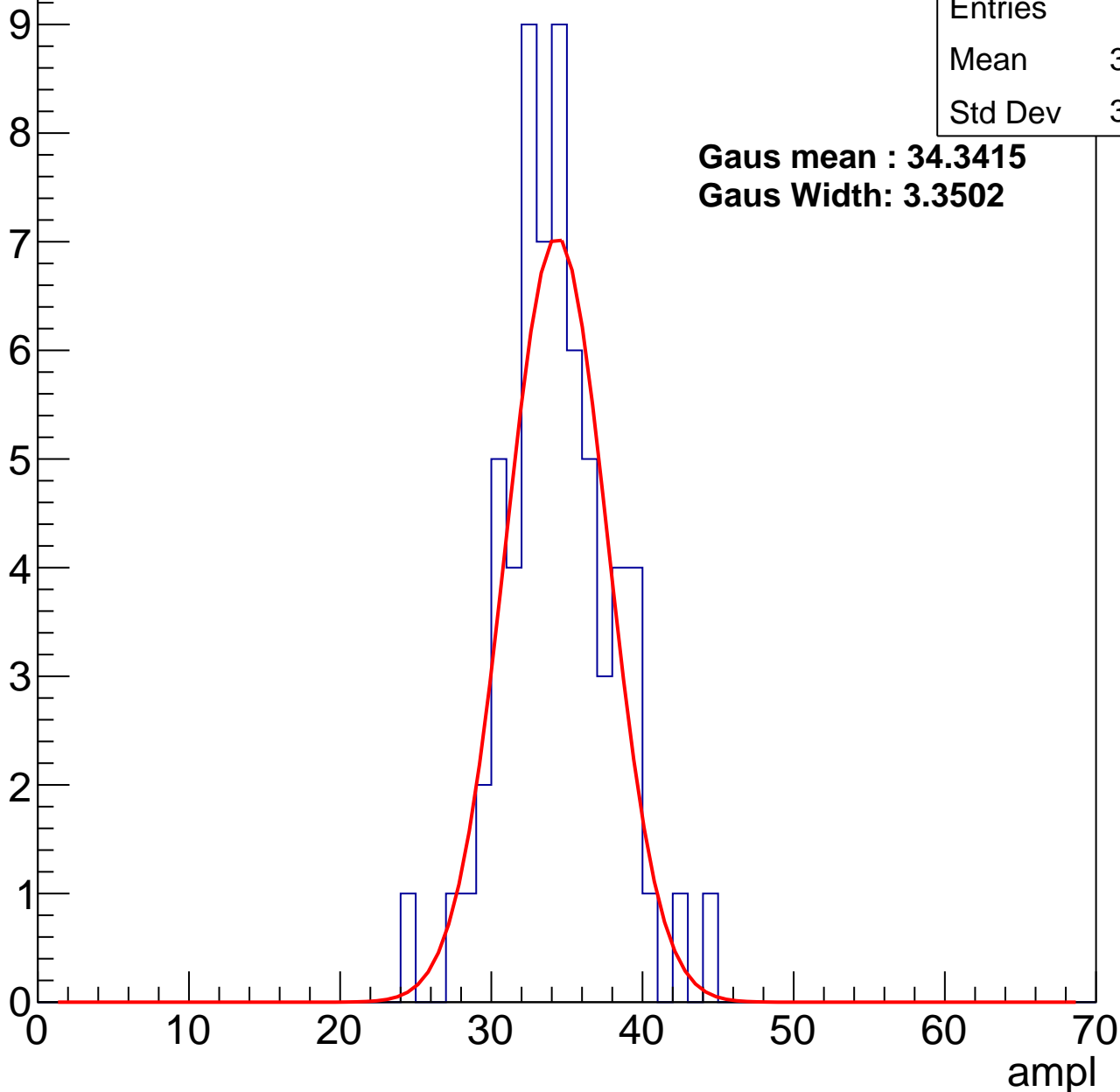
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	33.92
Std Dev	3.559

**Gaus mean : 34.3415**

**Gaus Width: 3.3502**



# B1L102S, U21-ch120, adc2

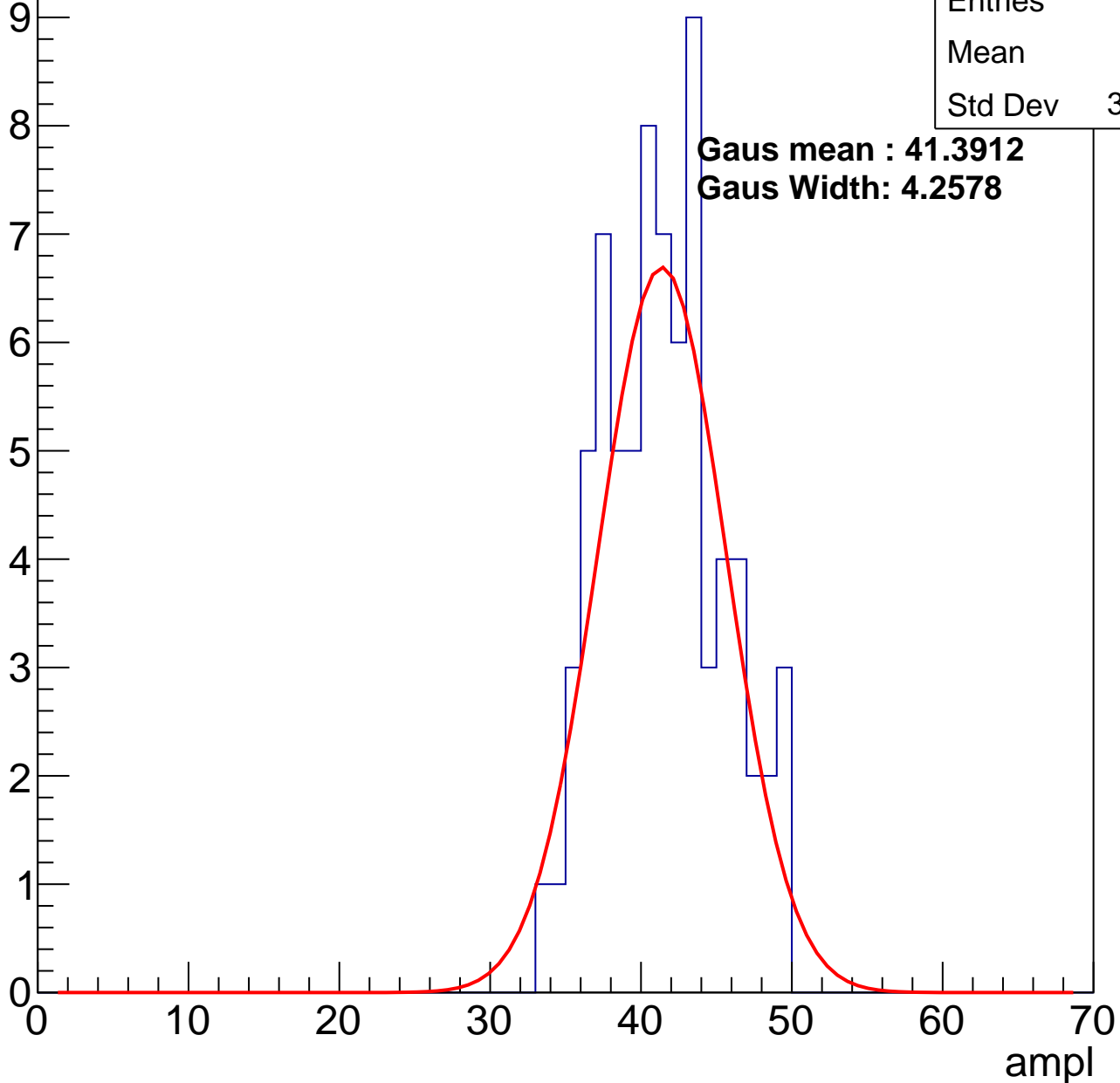
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	41
Std Dev	3.875

**Gaus mean : 41.3912**

**Gaus Width: 4.2578**

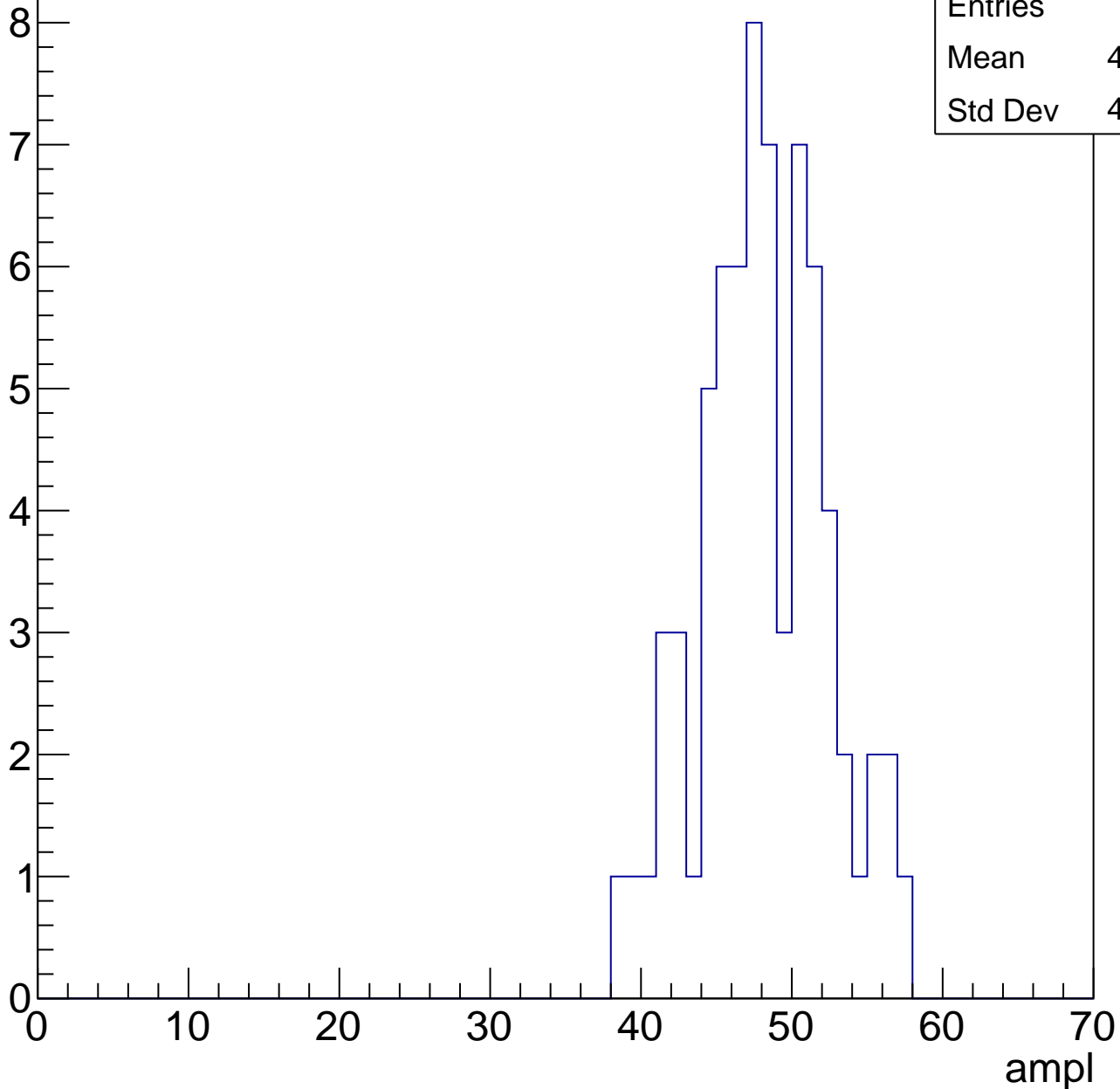


# B1L102S, U21-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	47.67
Std Dev	4.184

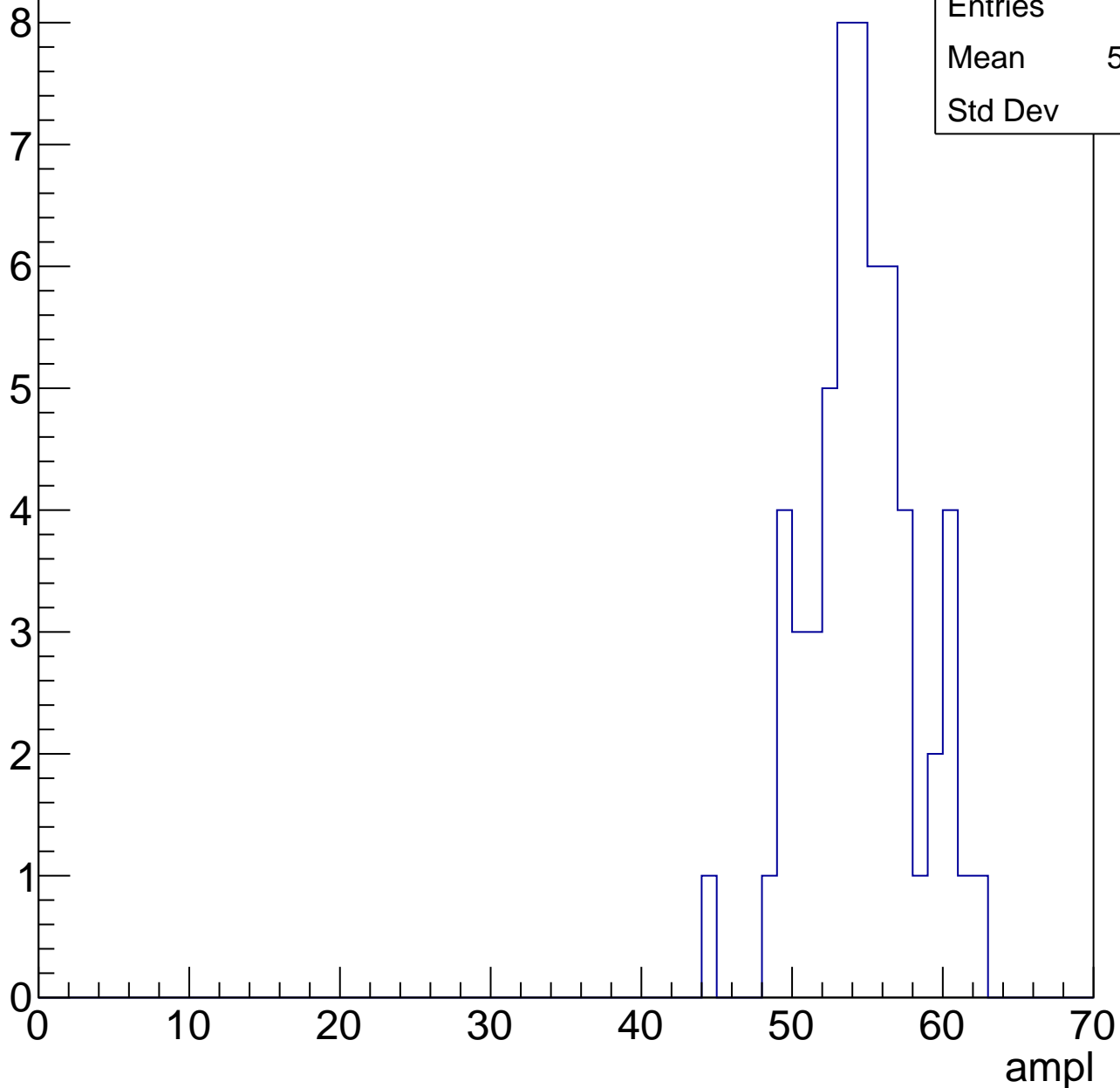


# B1L102S, U21-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	54.14
Std Dev	3.54

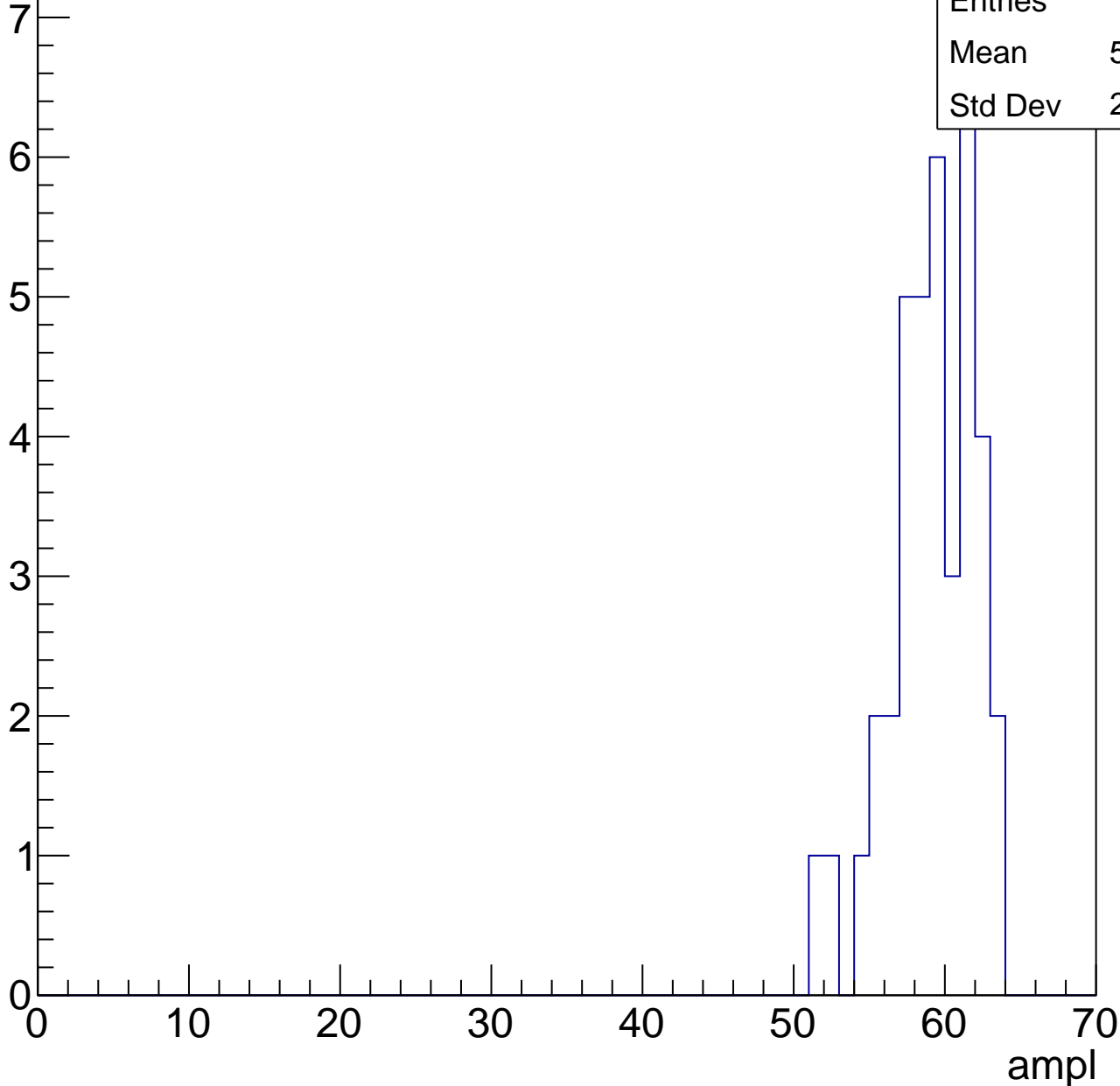


# B1L102S, U21-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	39
Mean	58.69
Std Dev	2.812

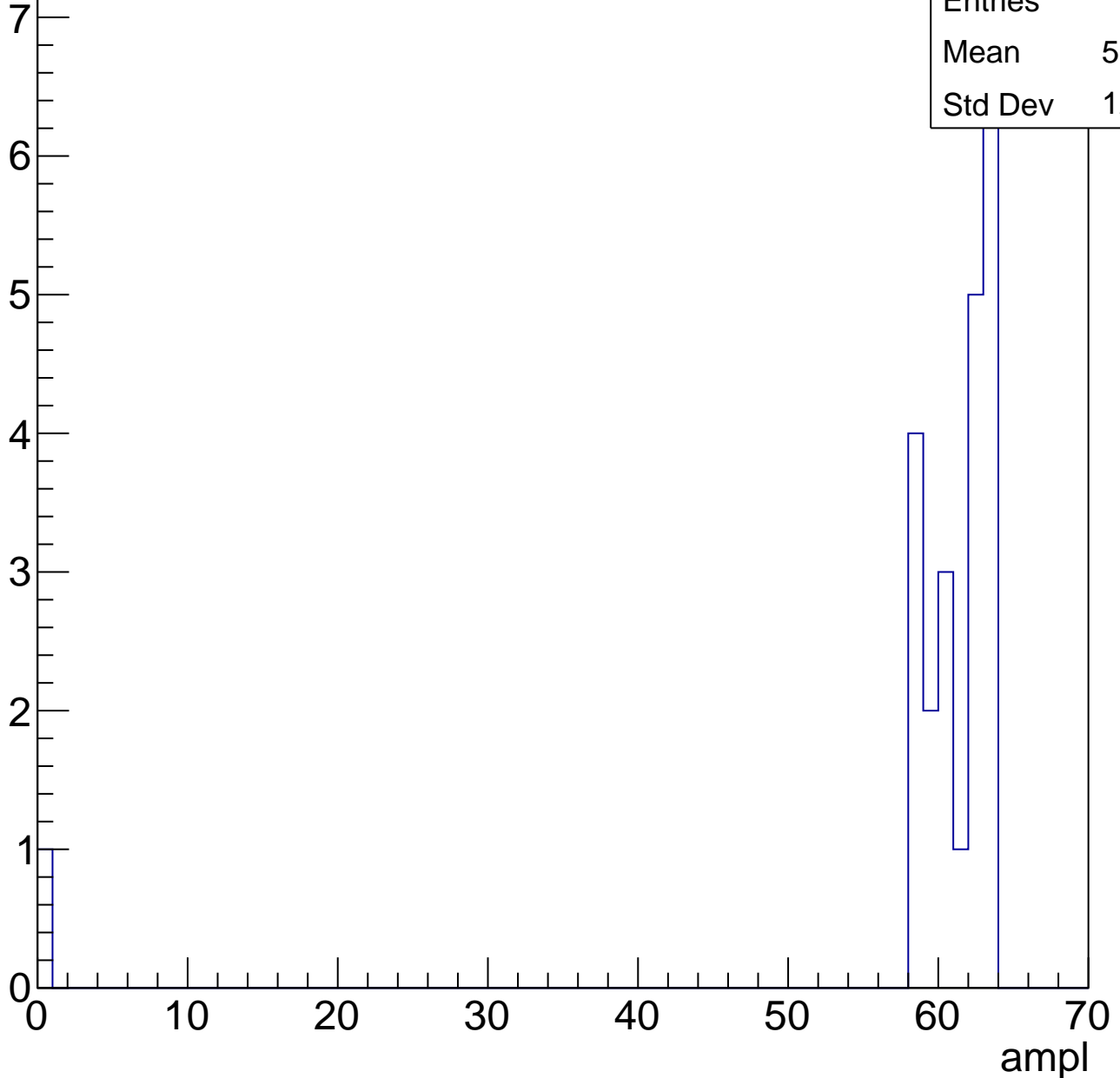


# B1L102S, U21-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	23
Mean	58.35
Std Dev	12.58

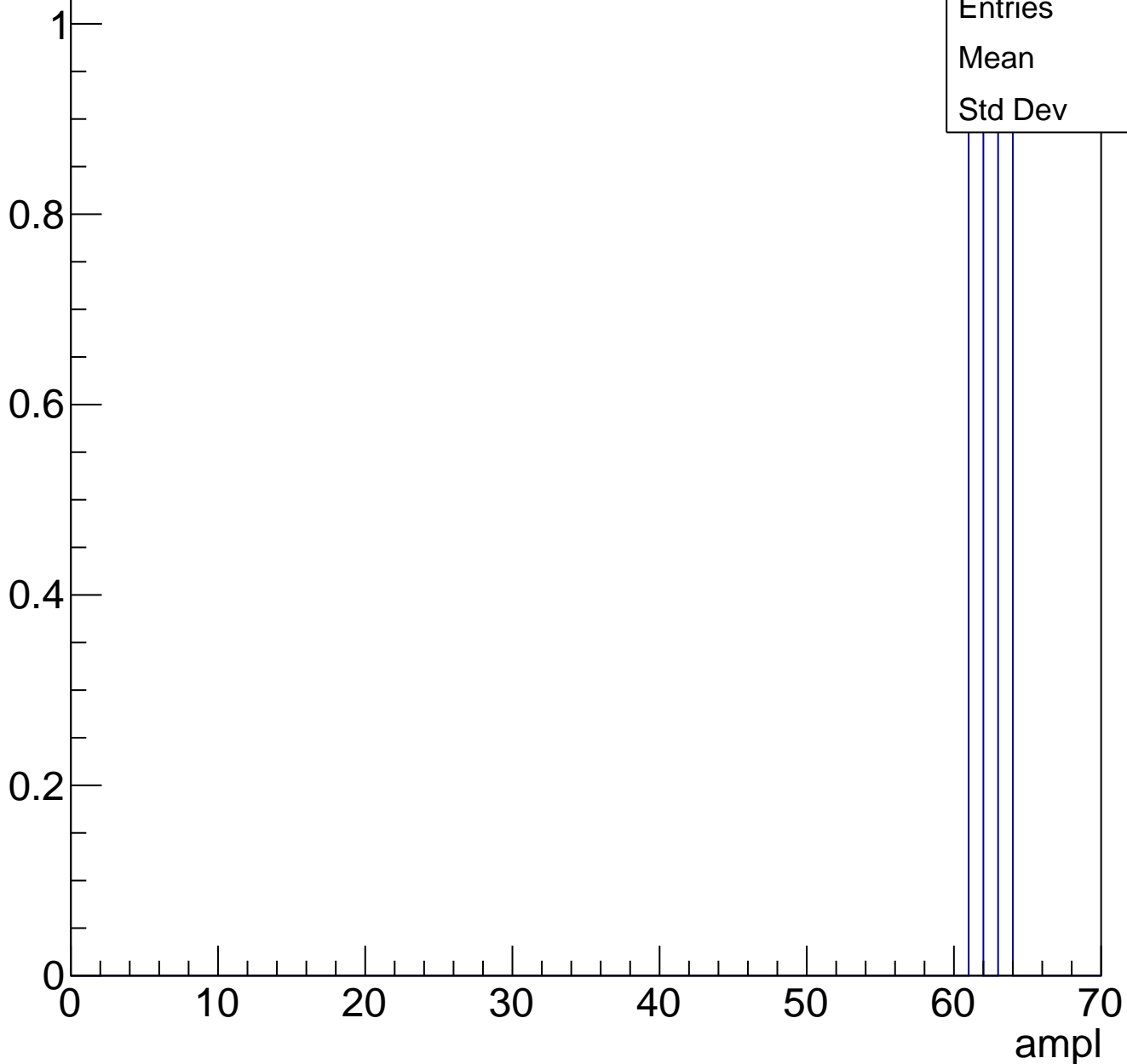




# B1L102S, U21-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch121, adc0

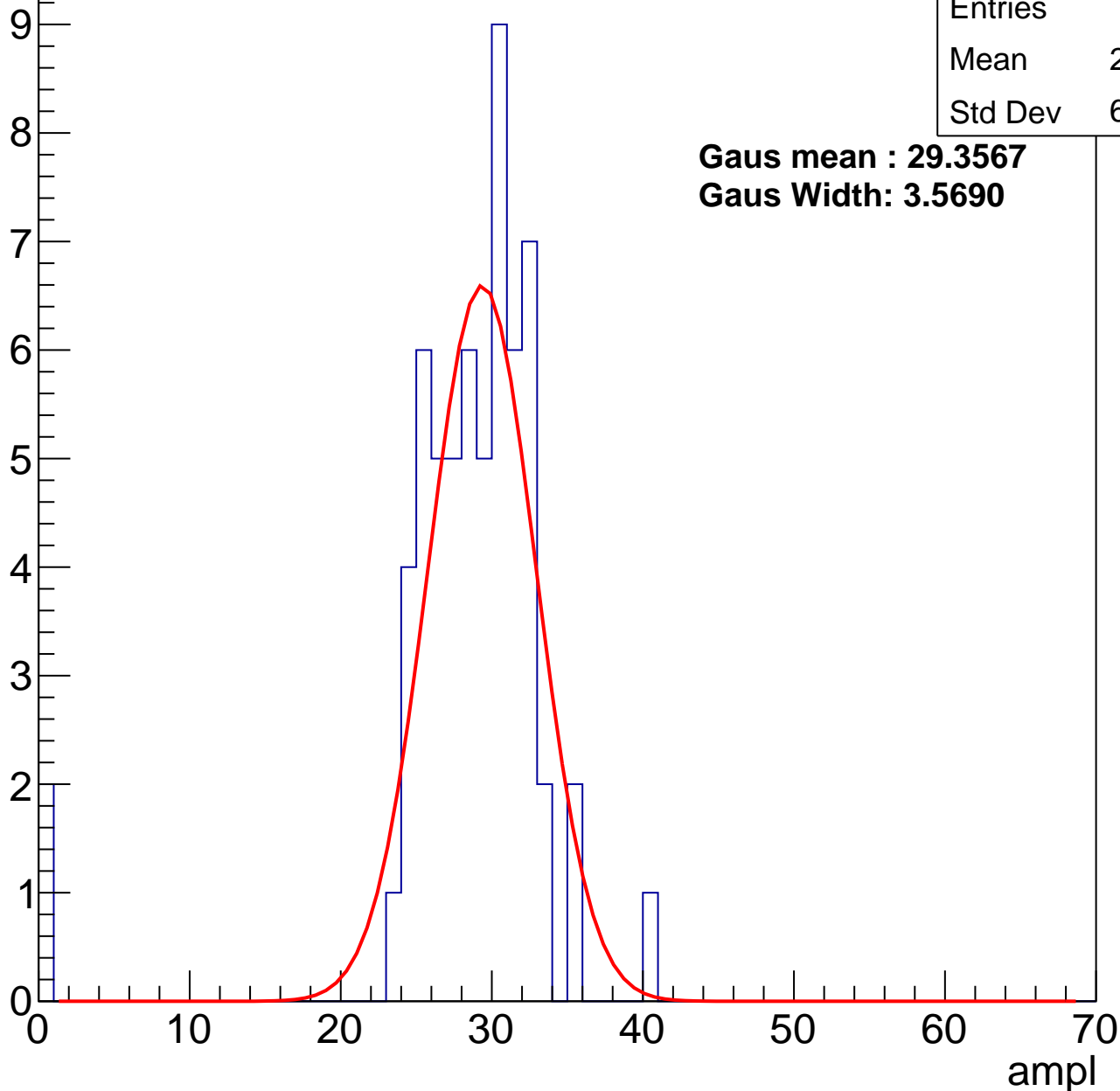
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	27.92
Std Dev	6.052

**Gaus mean : 29.3567**

**Gaus Width: 3.5690**



# B1L102S, U21-ch121, adc1

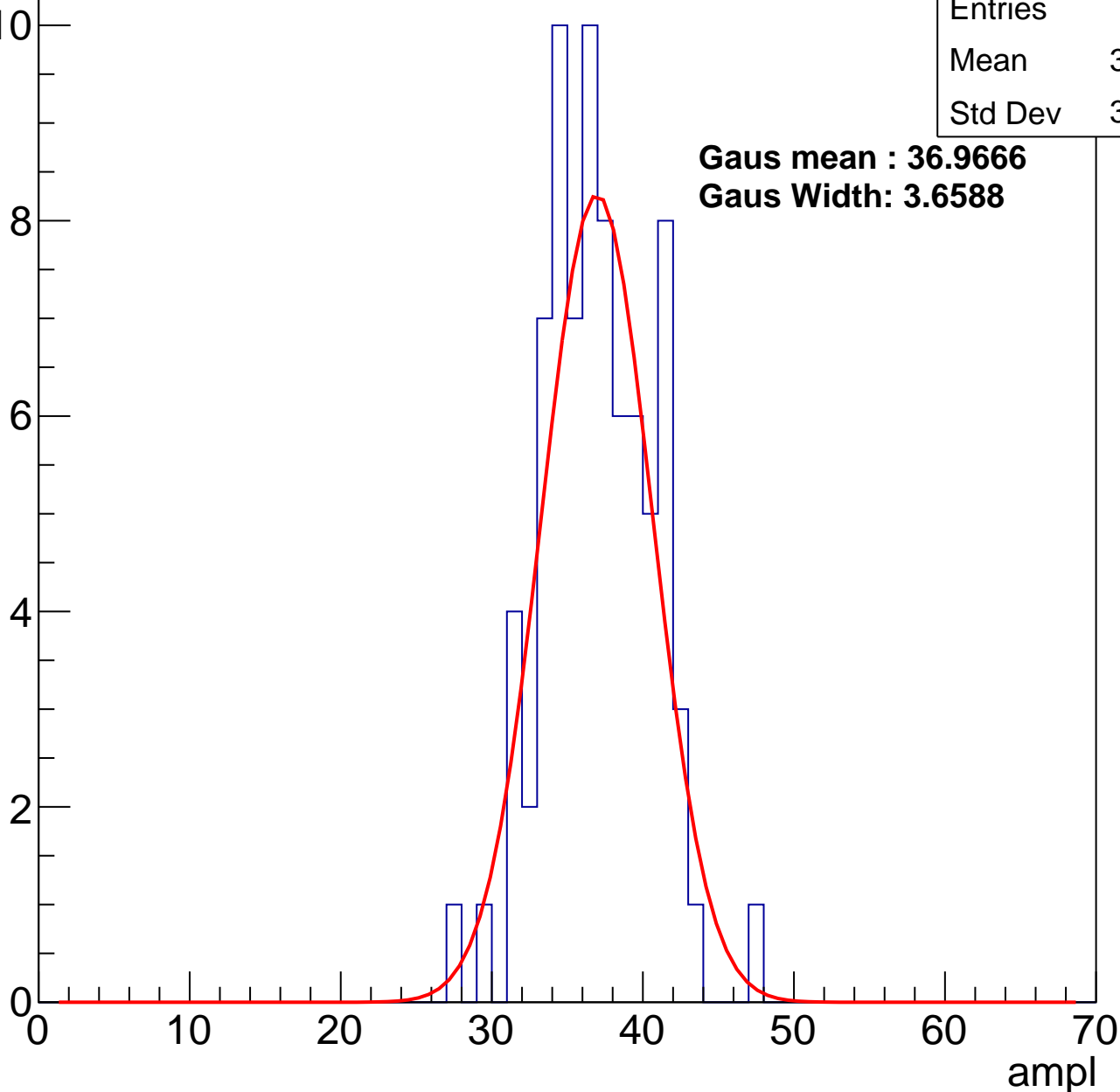
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	36.52
Std Dev	3.525

**Gaus mean : 36.9666**

**Gaus Width: 3.6588**



# B1L102S, U21-ch121, adc2

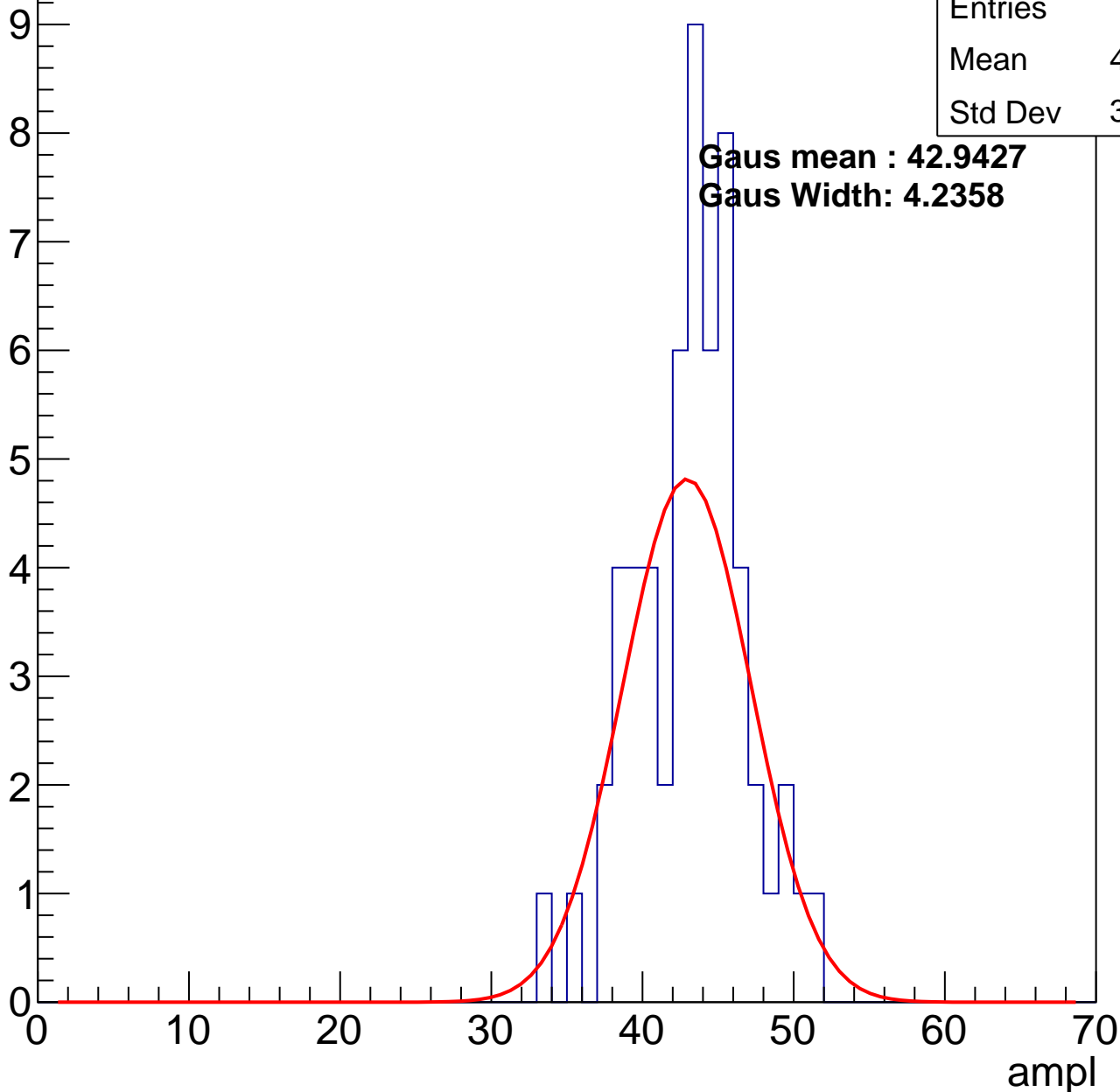
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	42.76
Std Dev	3.626

**Gaus mean : 42.9427**

**Gaus Width: 4.2358**

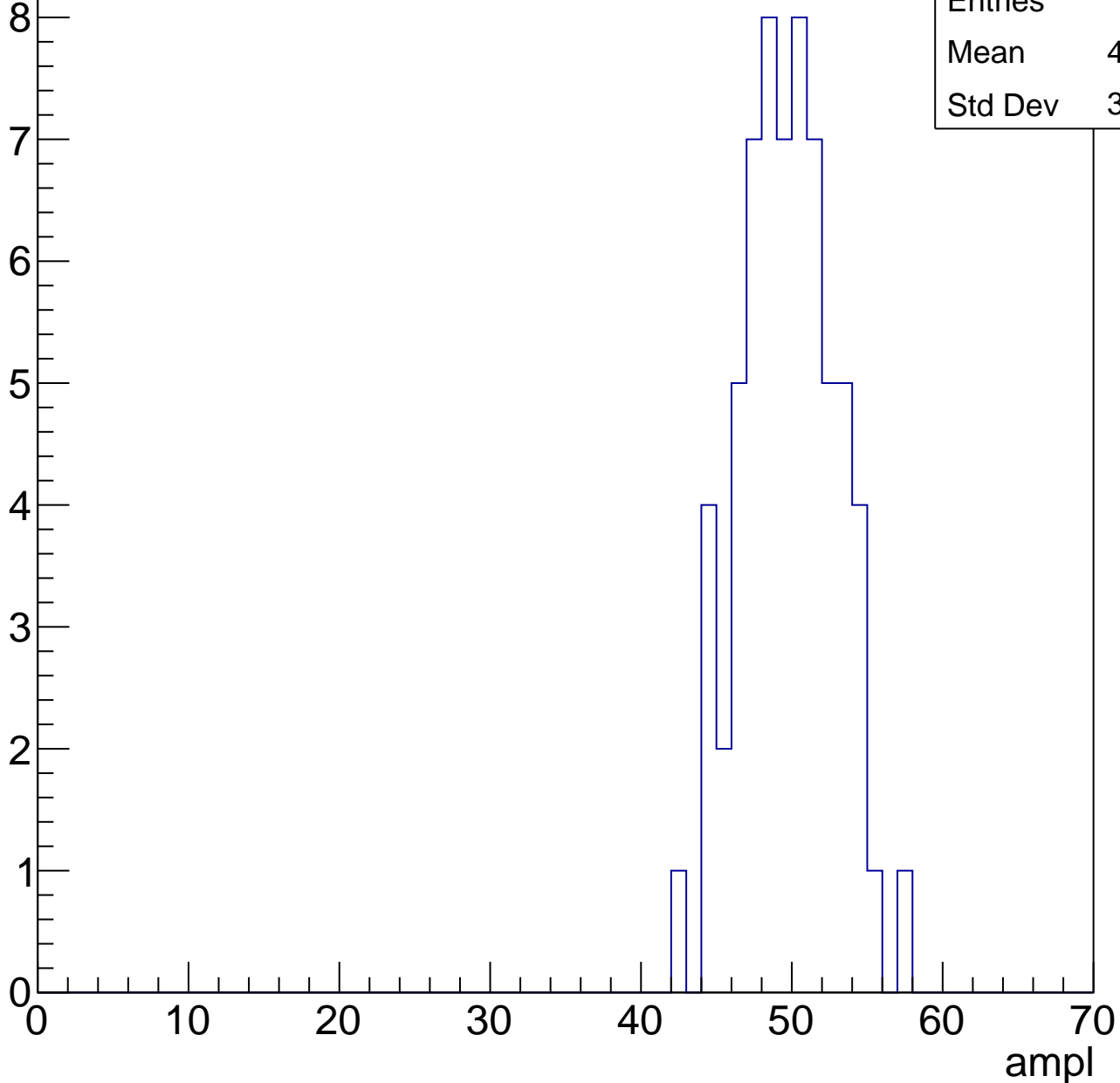


# B1L102S, U21-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	49.29
Std Dev	3.082

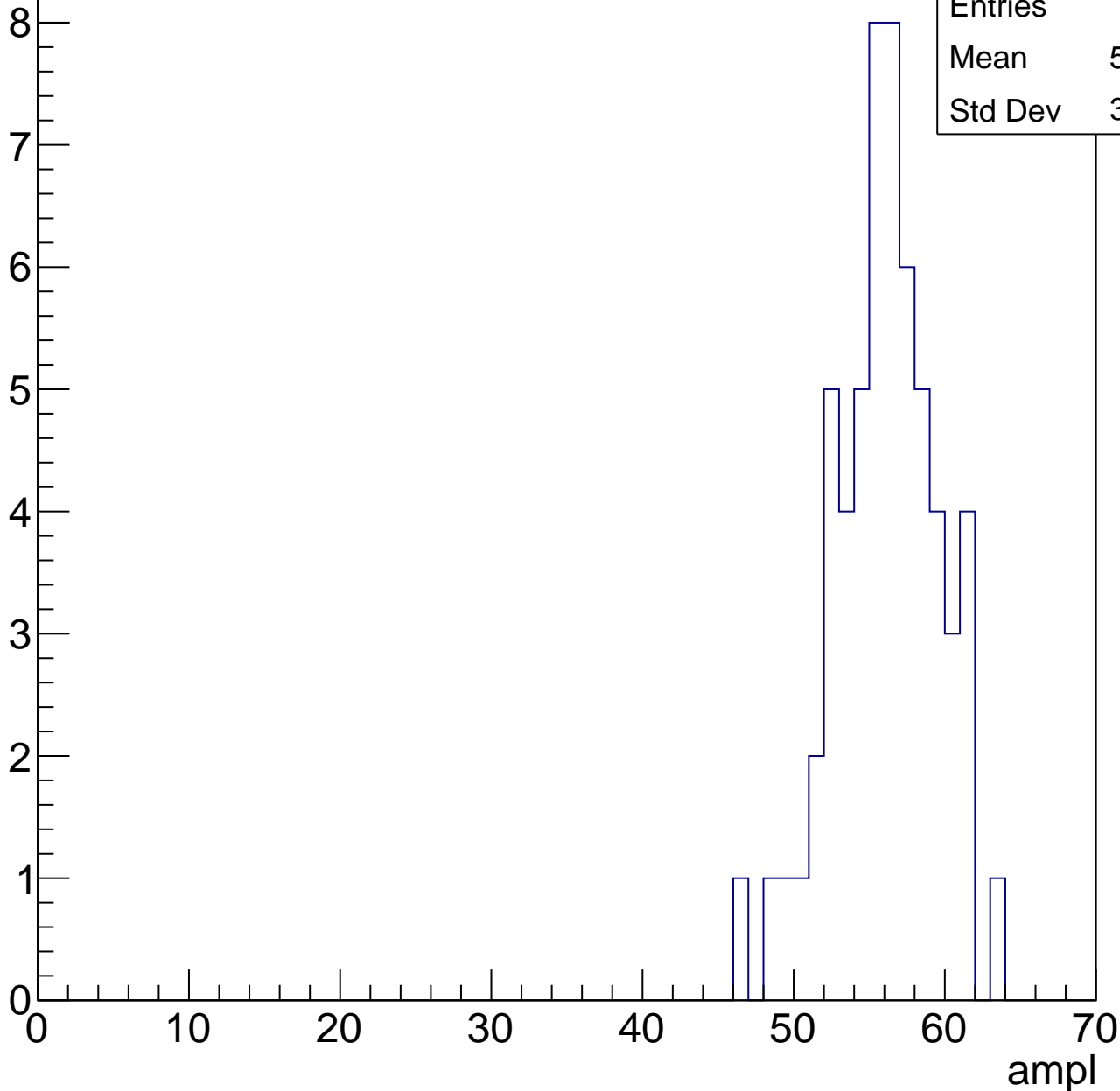


# B1L102S, U21-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	55.59
Std Dev	3.425

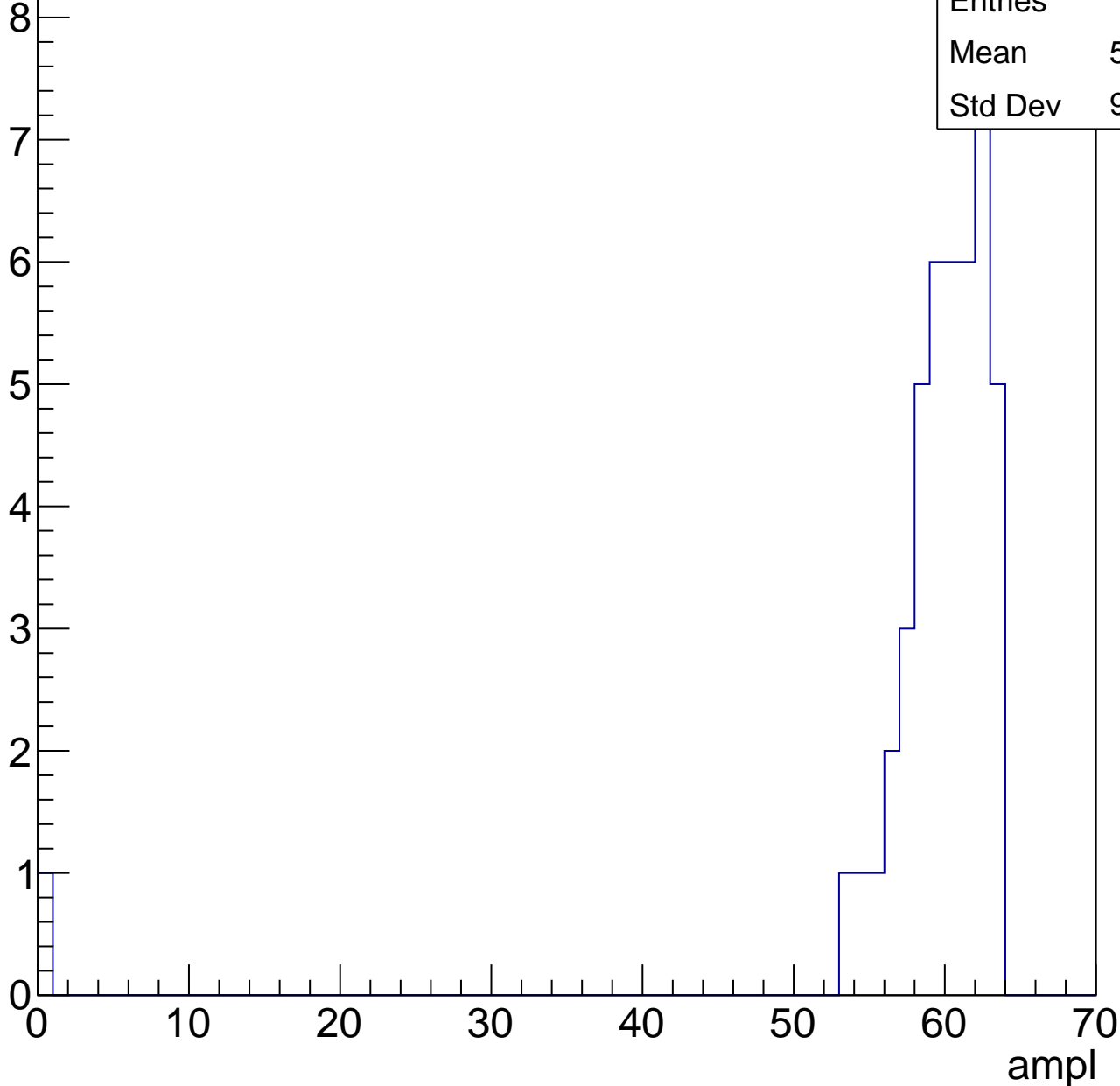


# B1L102S, U21-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	58.36
Std Dev	9.136



# B1L102S, U21-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L102S, U21-ch122, adc0

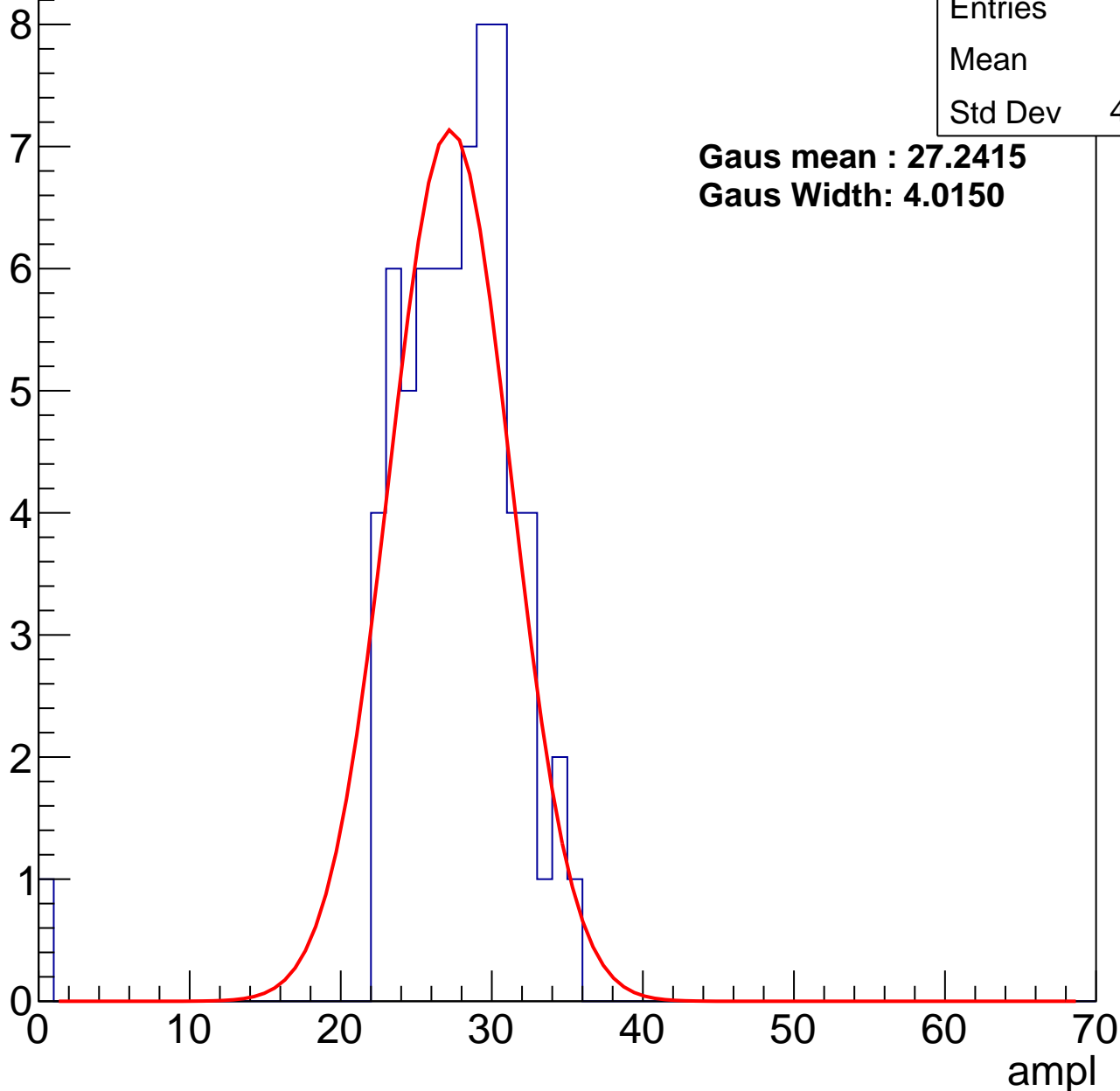
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	27.1
Std Dev	4.619

**Gaus mean : 27.2415**

**Gaus Width: 4.0150**



# B1L102S, U21-ch122, adc1

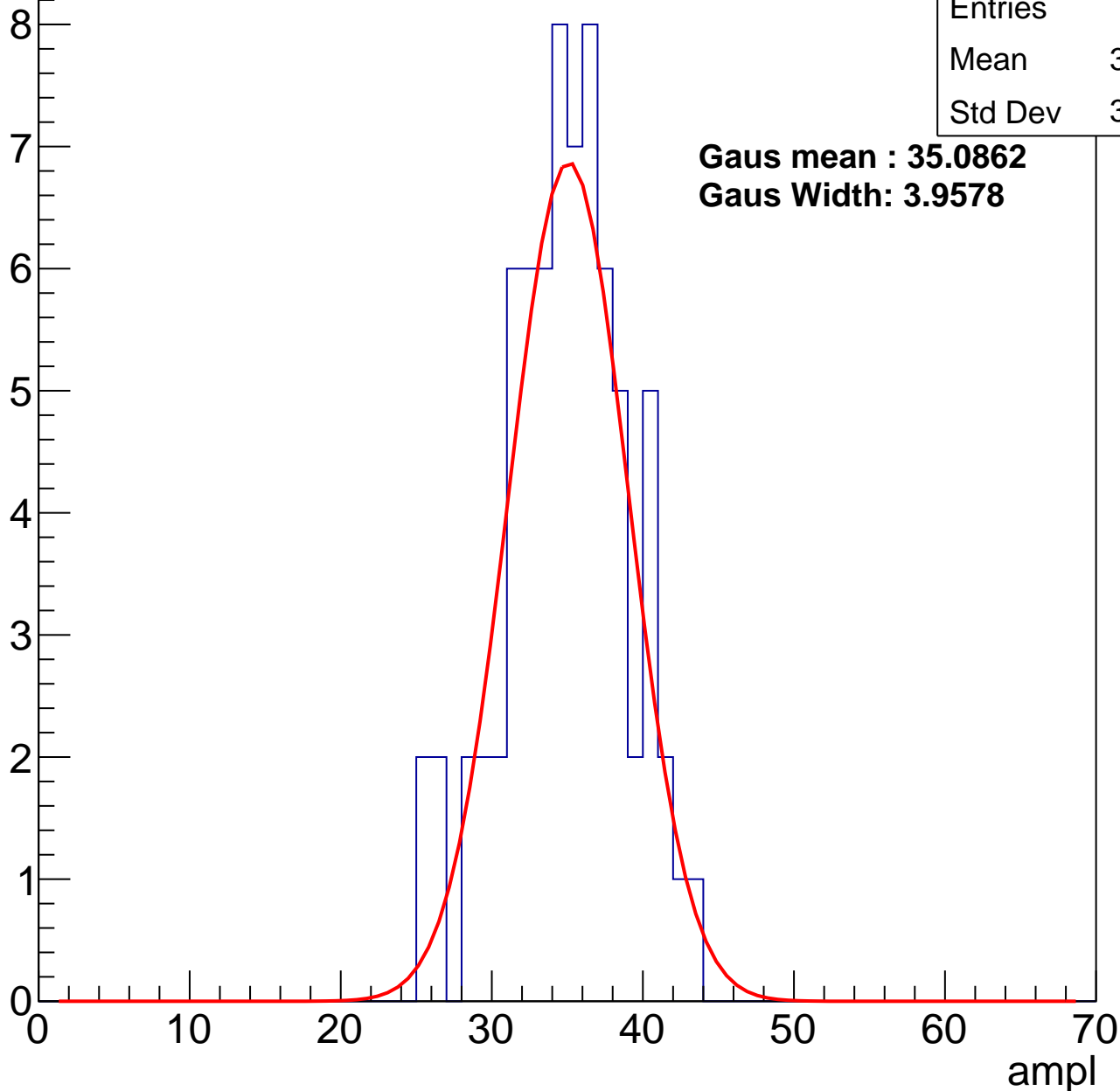
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	34.44
Std Dev	3.986

**Gaus mean : 35.0862**

**Gaus Width: 3.9578**



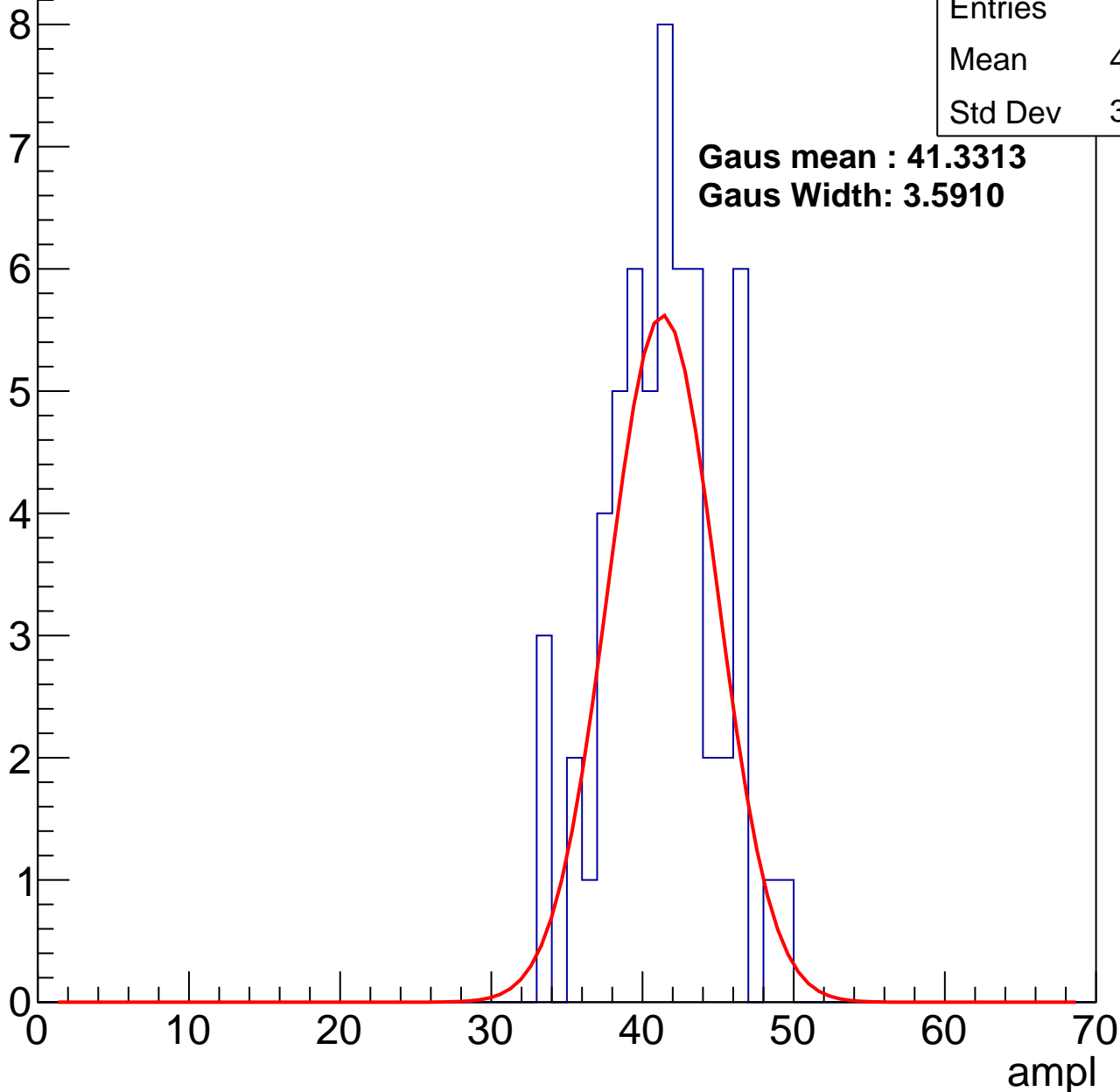
# B1L102S, U21-ch122, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	40.79
Std Dev	3.638

**Gaus mean : 41.3313**  
**Gaus Width: 3.5910**

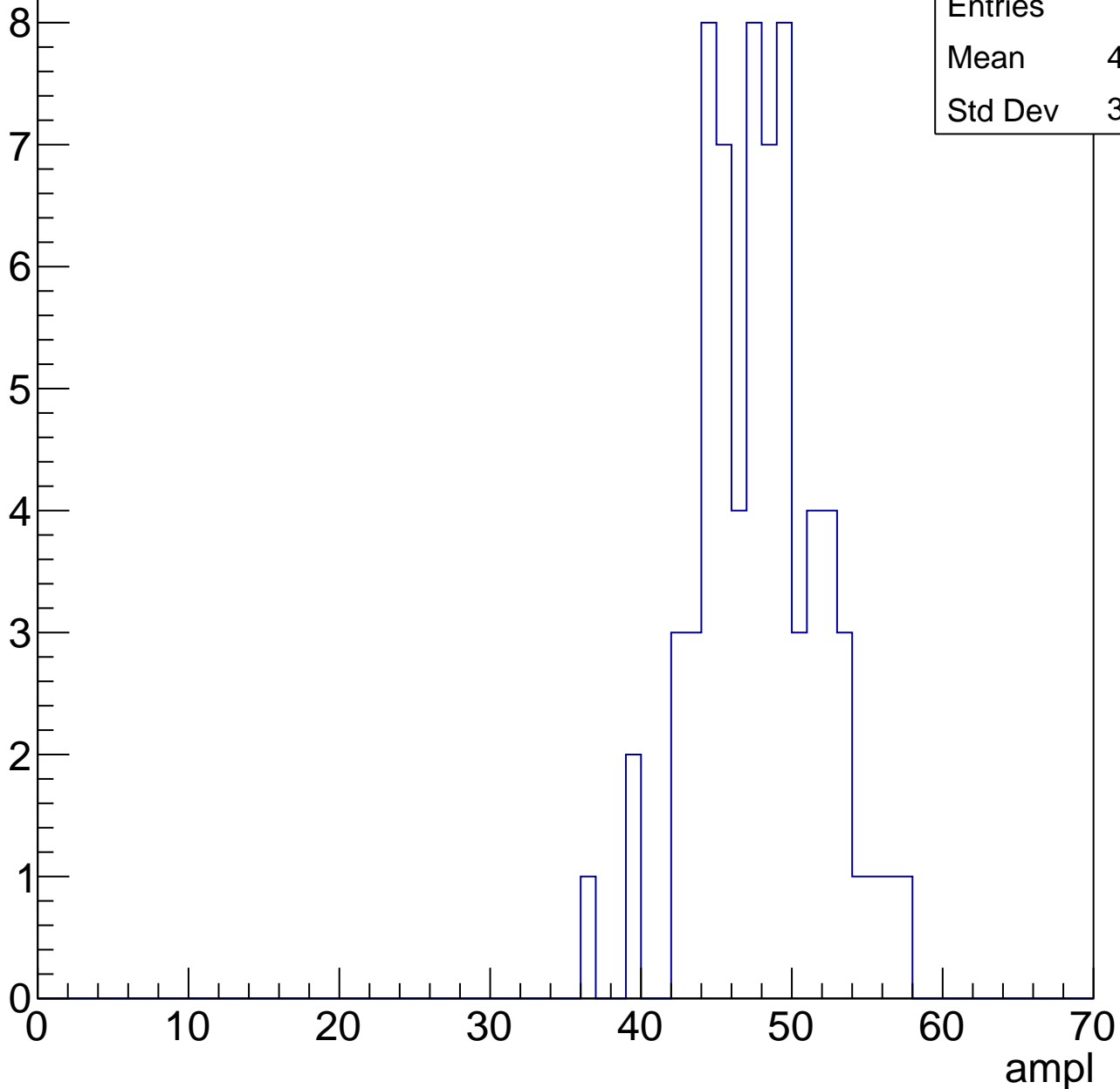


# B1L102S, U21-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	47.35
Std Dev	3.992

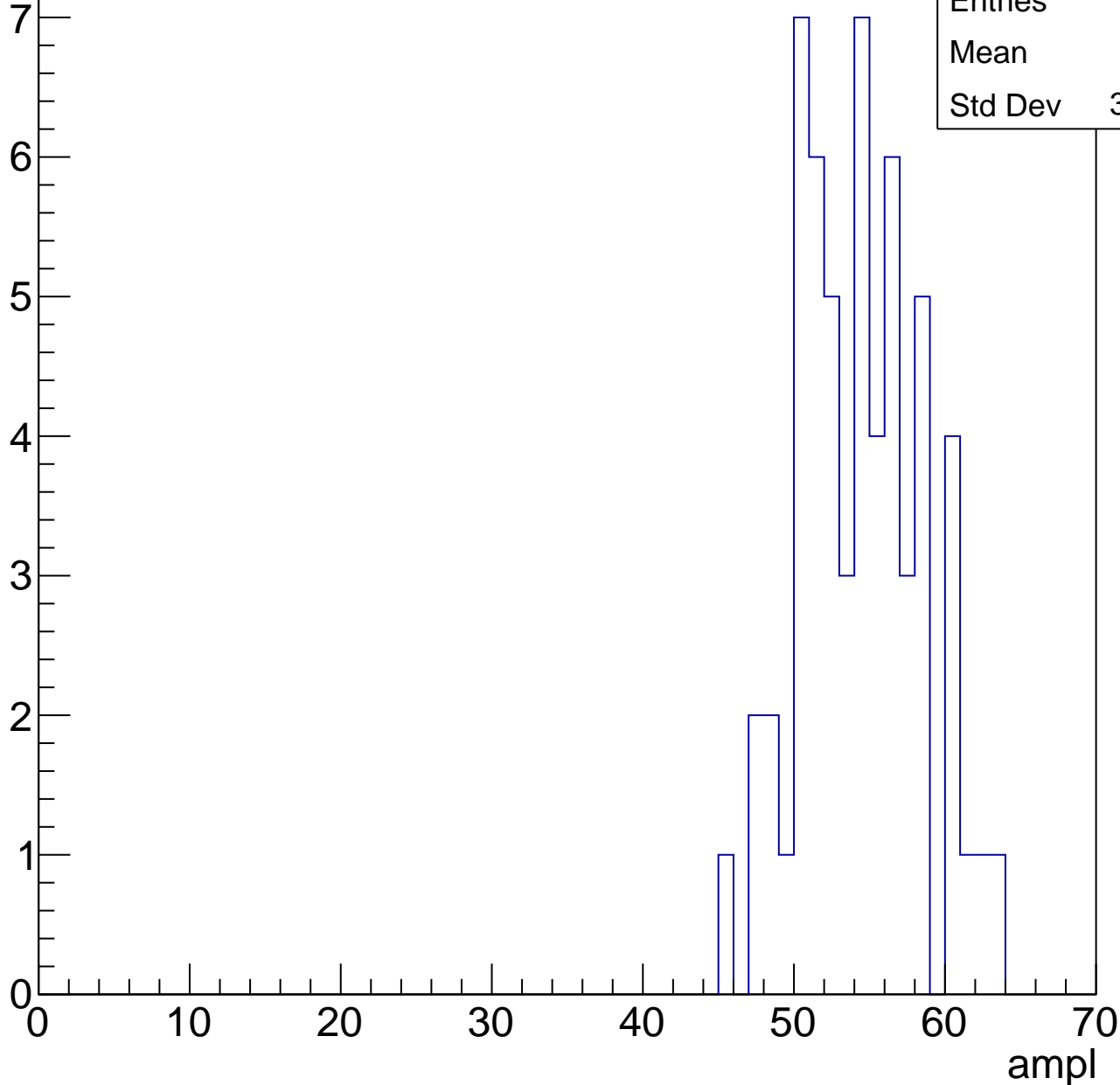


# B1L102S, U21-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

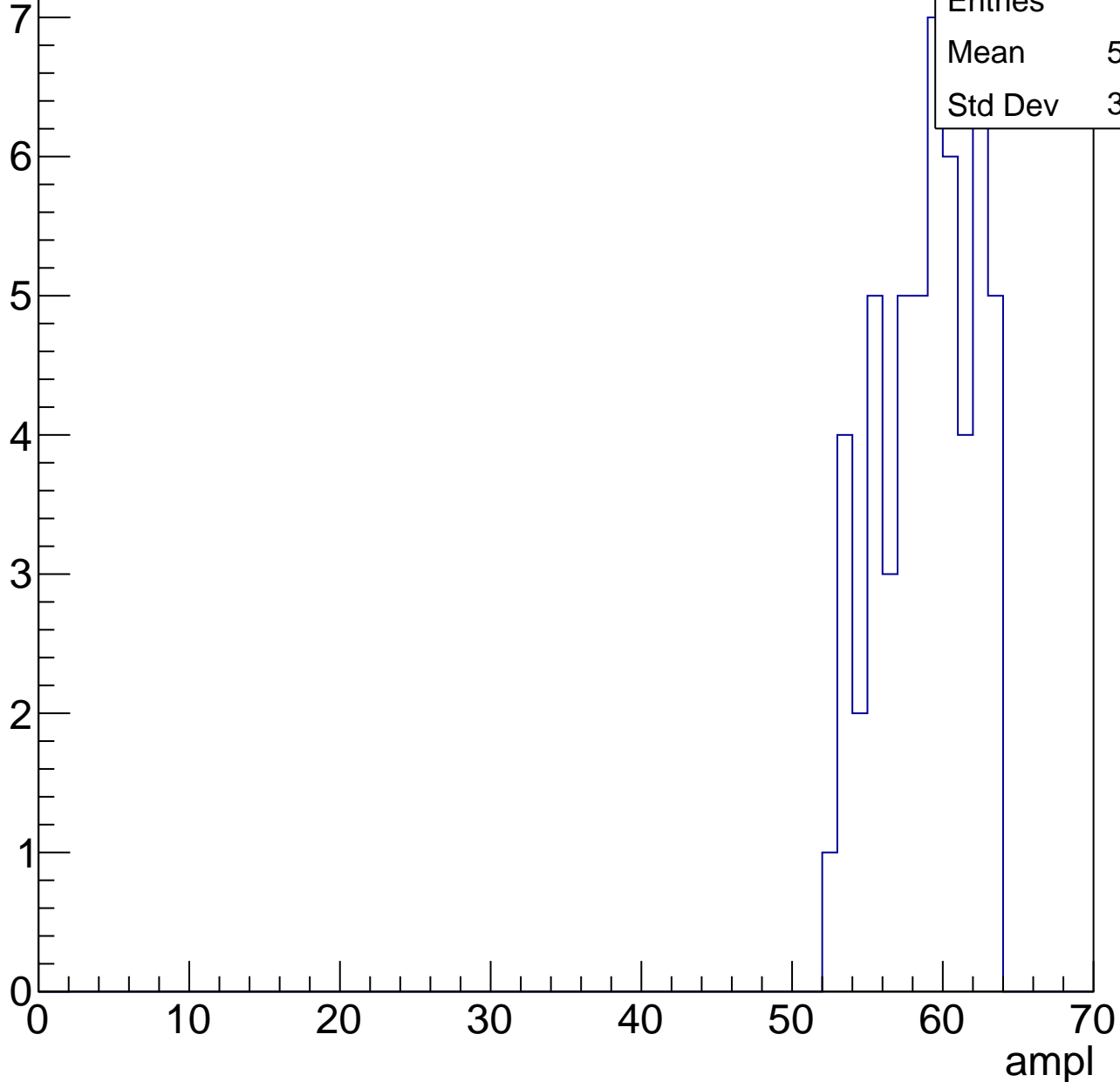
Entries	59
Mean	53.9
Std Dev	3.986



# B1L102S, U21-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



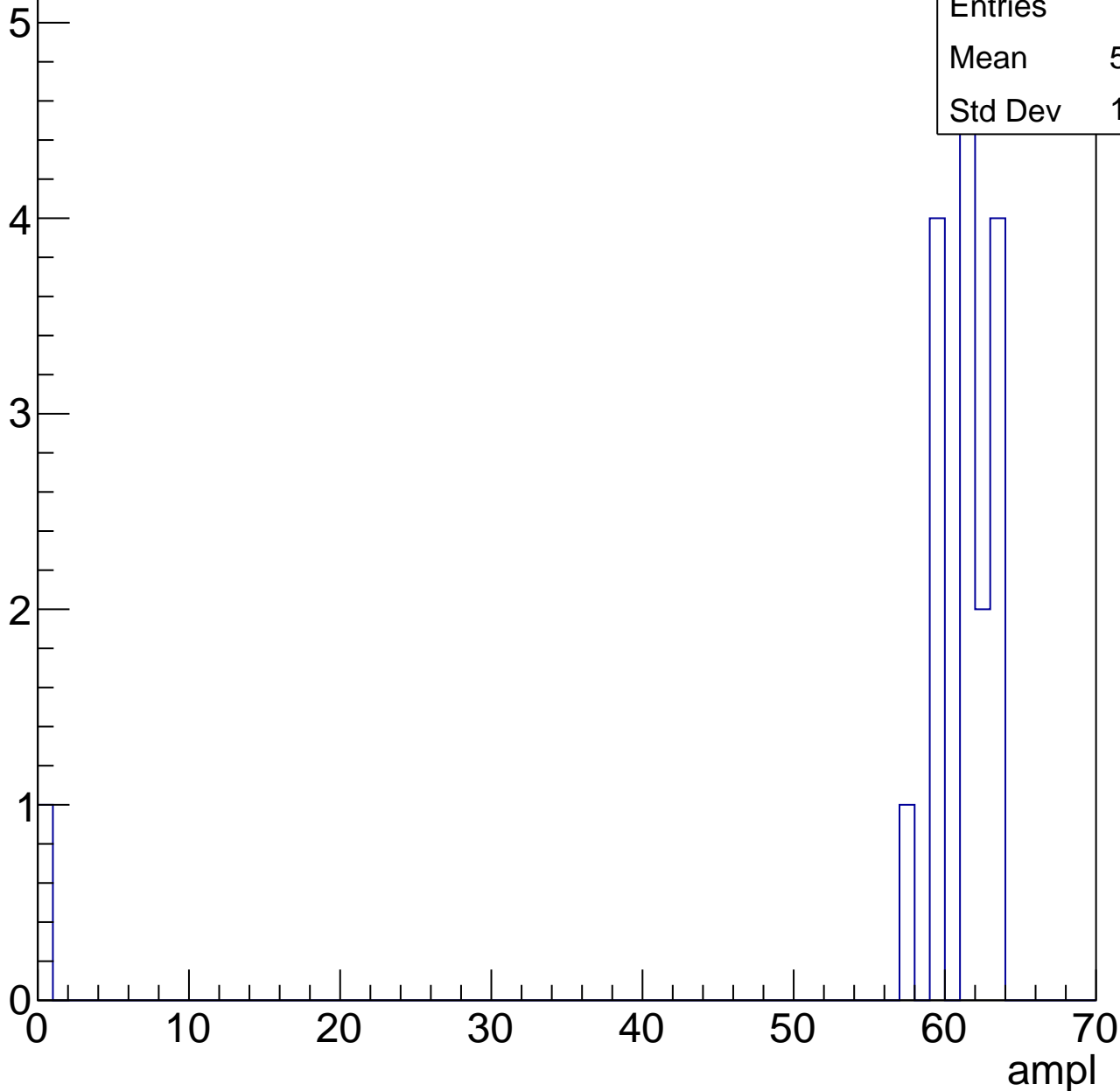
Entries	54
Mean	58.44
Std Dev	3.113

# B1L102S, U21-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	17
Mean	57.29
Std Dev	14.43





# B1L102S, U21-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	6
Std Dev	8.485

# B1L102S, U21-ch123, adc0

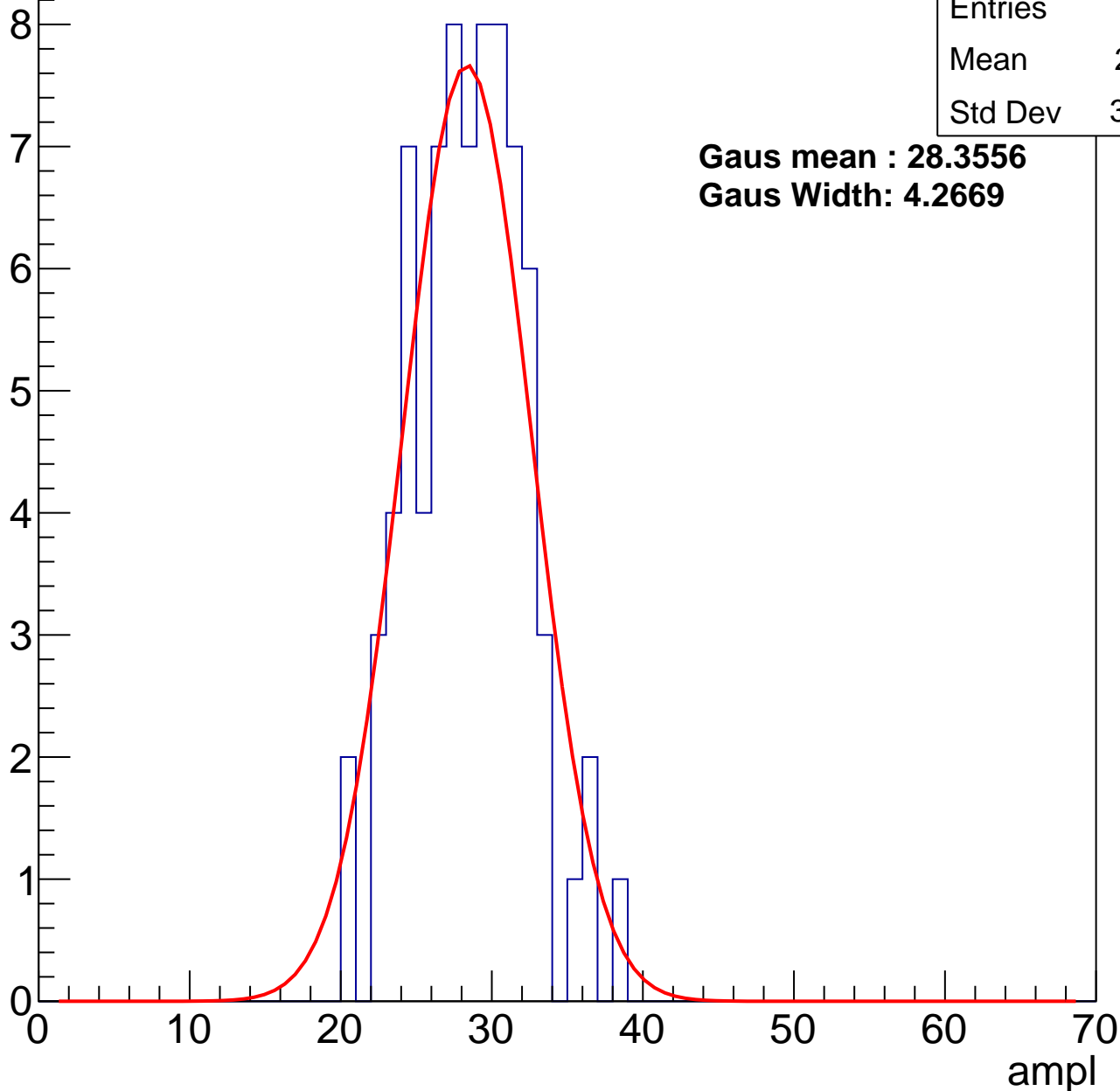
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	28.01
Std Dev	3.705

**Gaus mean : 28.3556**

**Gaus Width: 4.2669**



# B1L102S, U21-ch123, adc1

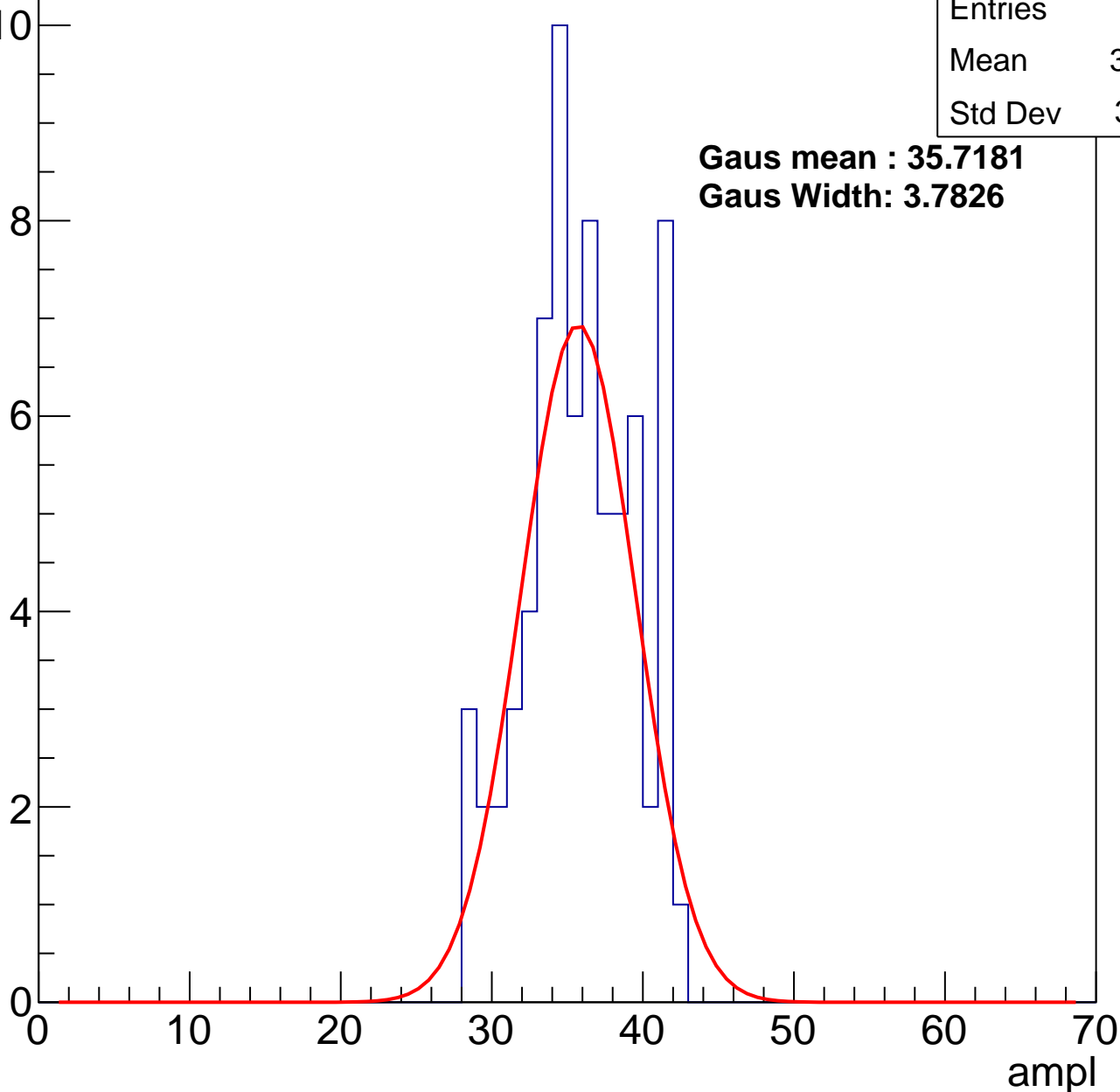
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	35.43
Std Dev	3.601

**Gaus mean : 35.7181**

**Gaus Width: 3.7826**



# B1L102S, U21-ch123, adc2

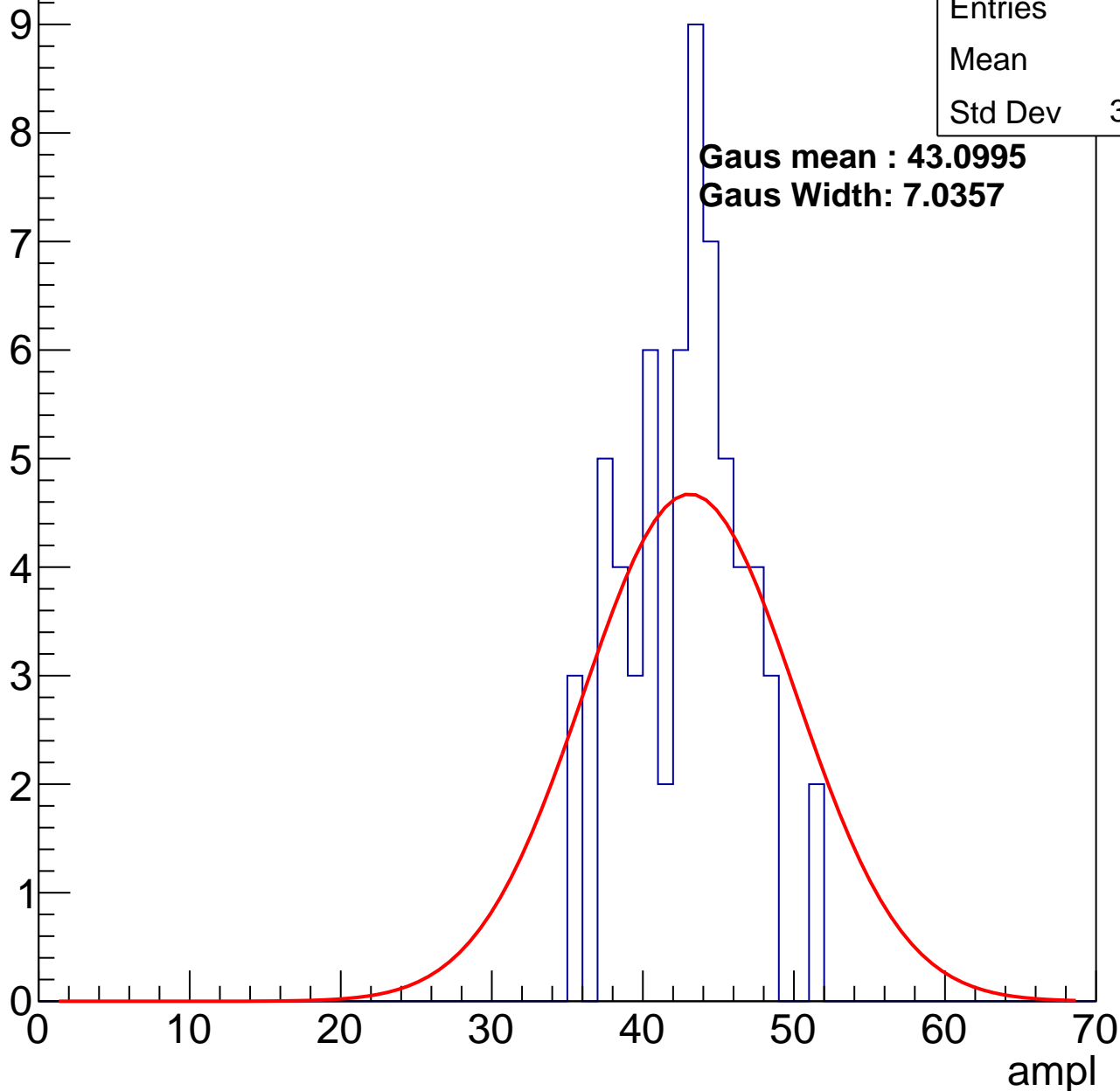
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	42.4
Std Dev	3.769

**Gaus mean : 43.0995**

**Gaus Width: 7.0357**

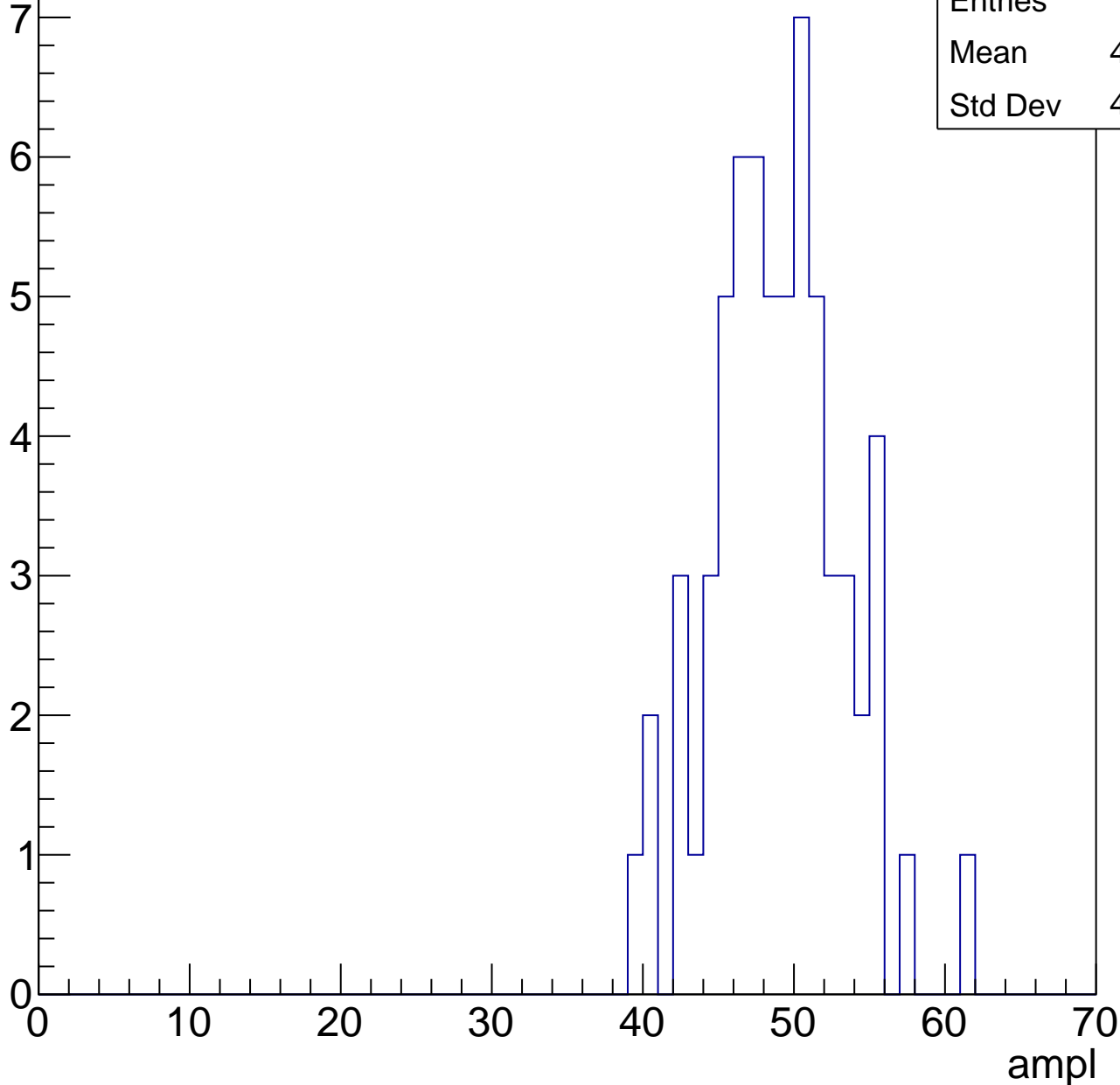


# B1L102S, U21-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

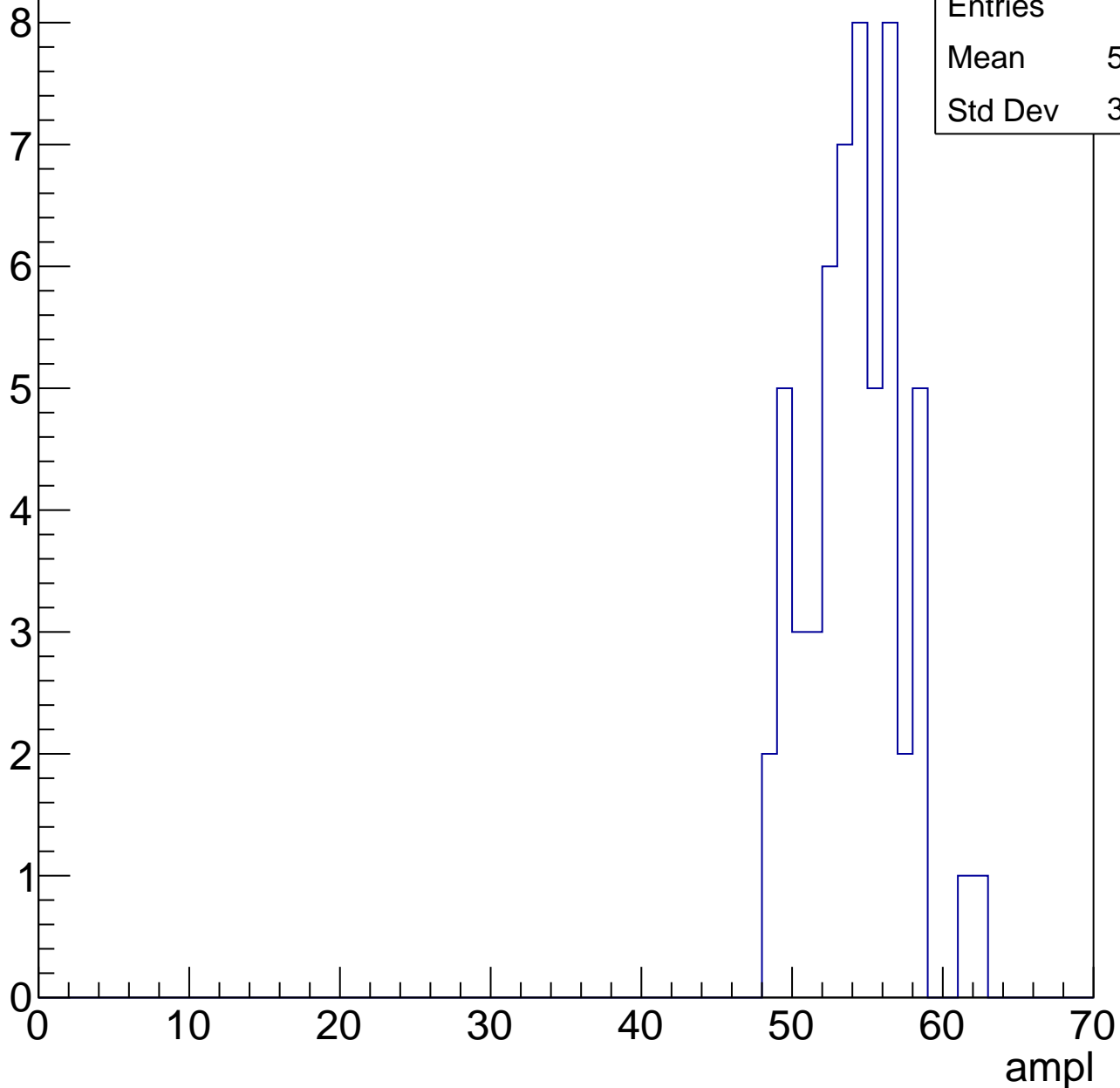
Entries	63
Mean	48.48
Std Dev	4.309



# B1L102S, U21-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	53
Mean	58.32
Std Dev	8.384

Entry

10

8

6

4

2

0

0

10

20

30

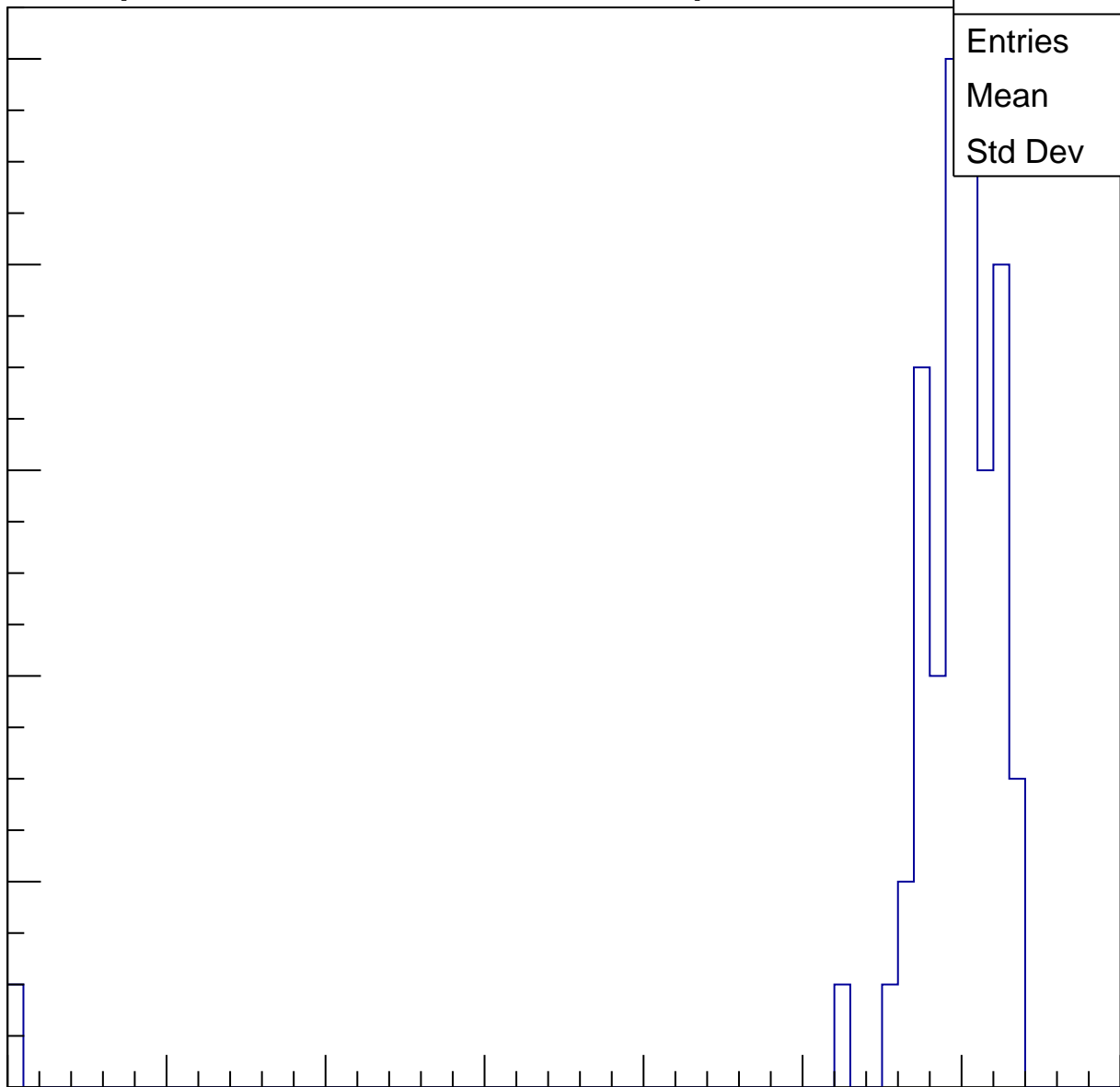
40

50

60

70

ampl

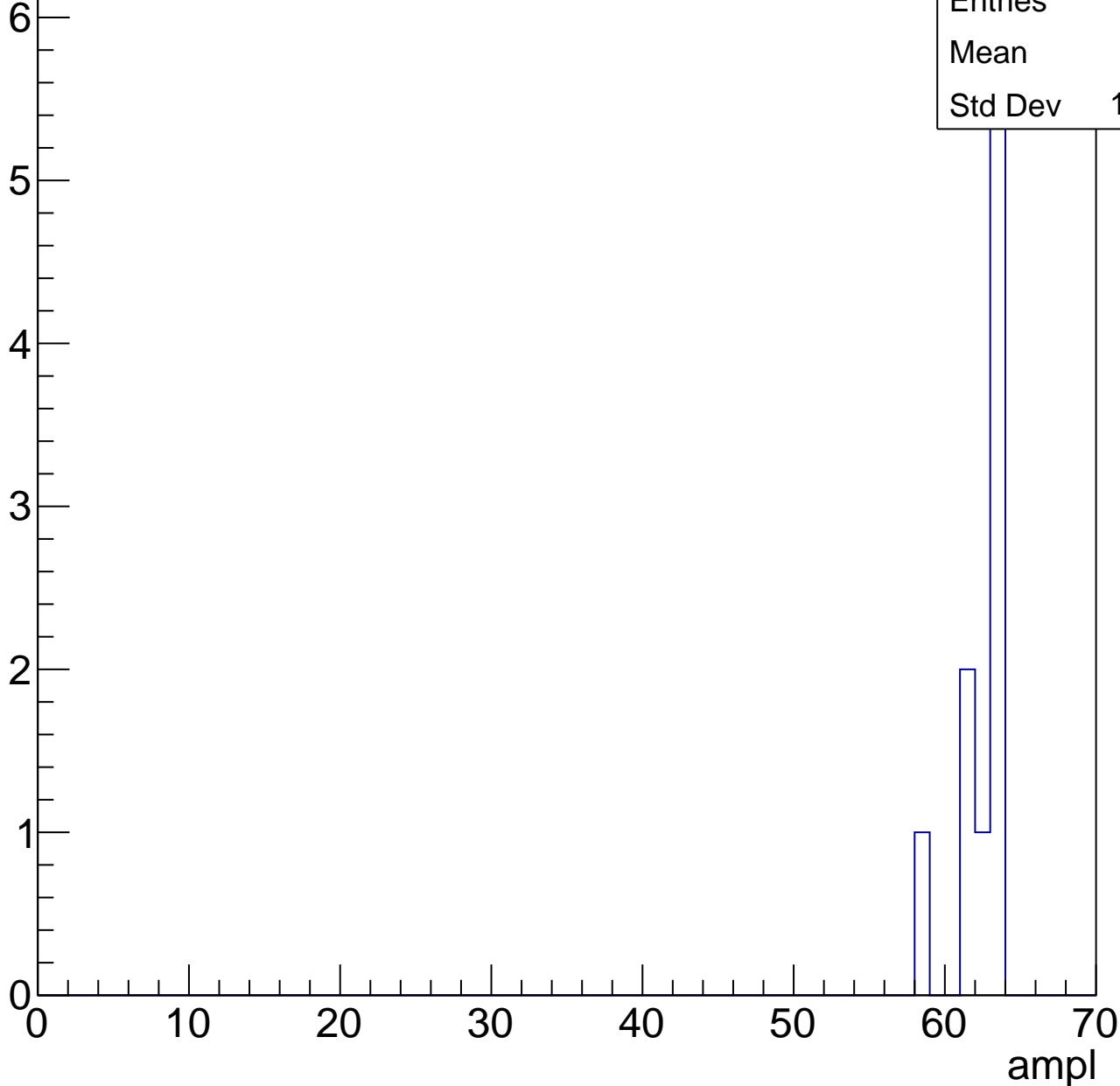


# B1L102S, U21-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	10
Mean	62
Std Dev	1.549

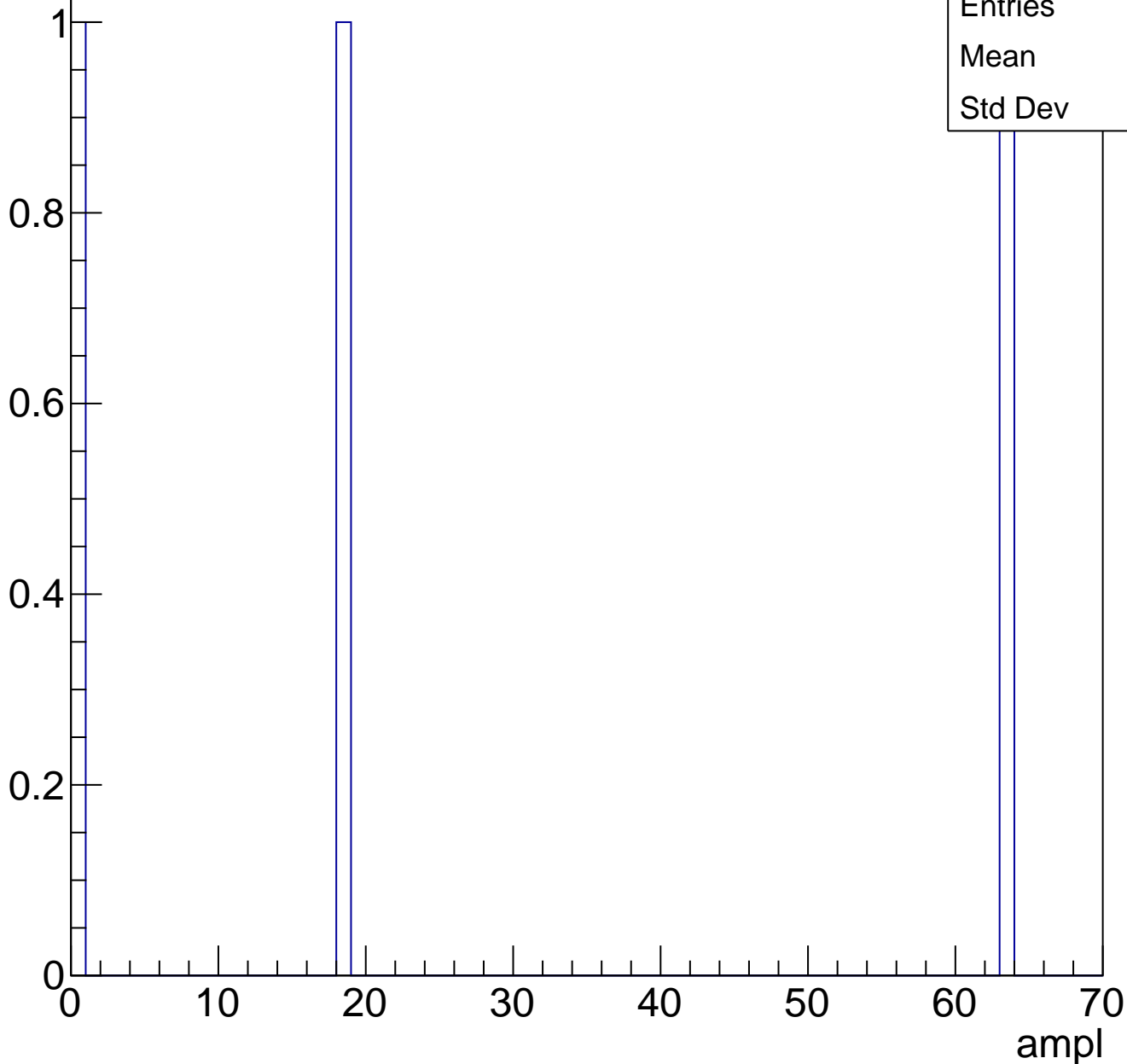




# B1L102S, U21-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch124, adc0

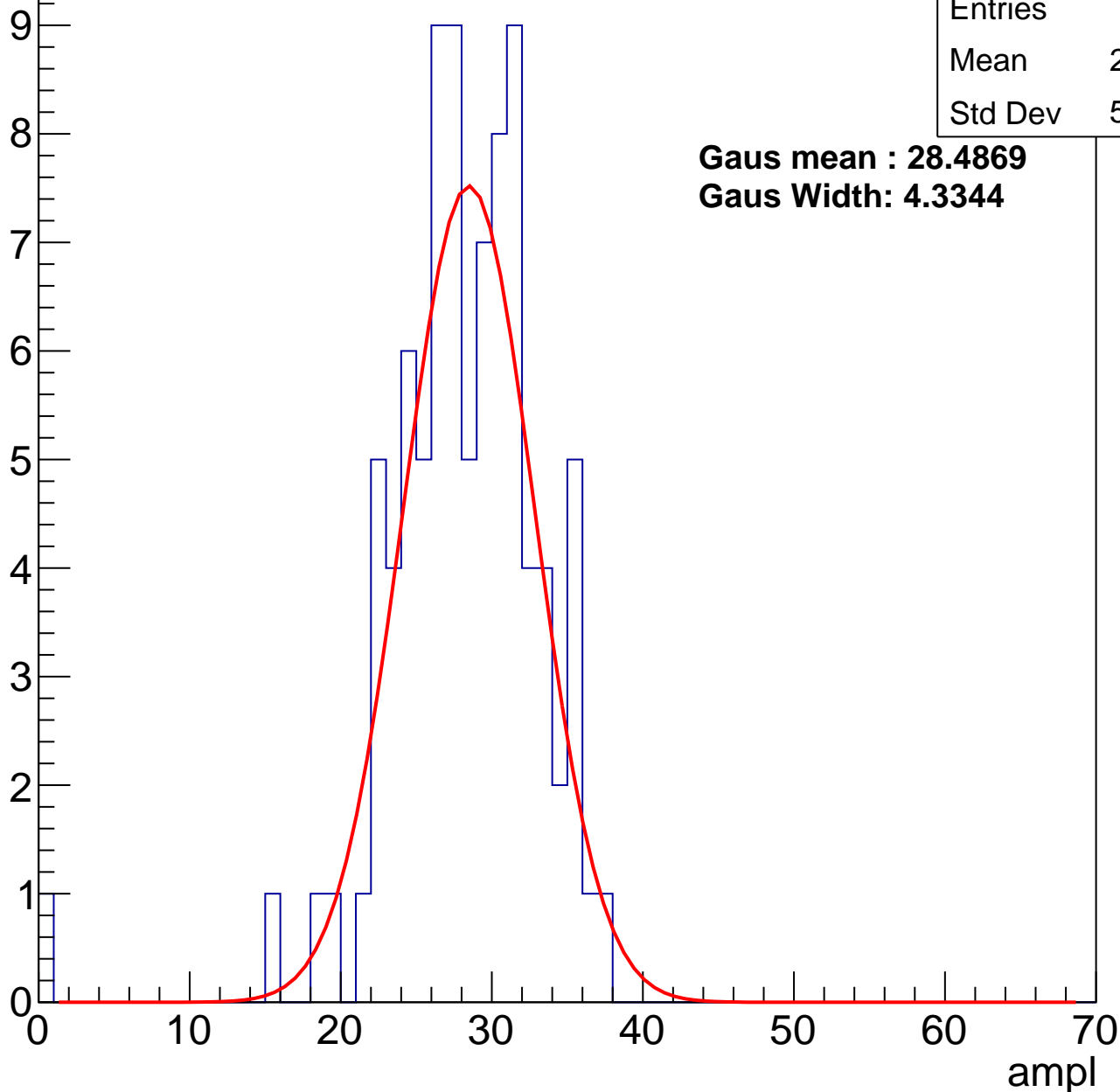
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	89
Mean	27.63
Std Dev	5.174

**Gaus mean : 28.4869**

**Gaus Width: 4.3344**



# B1L102S, U21-ch124, adc1

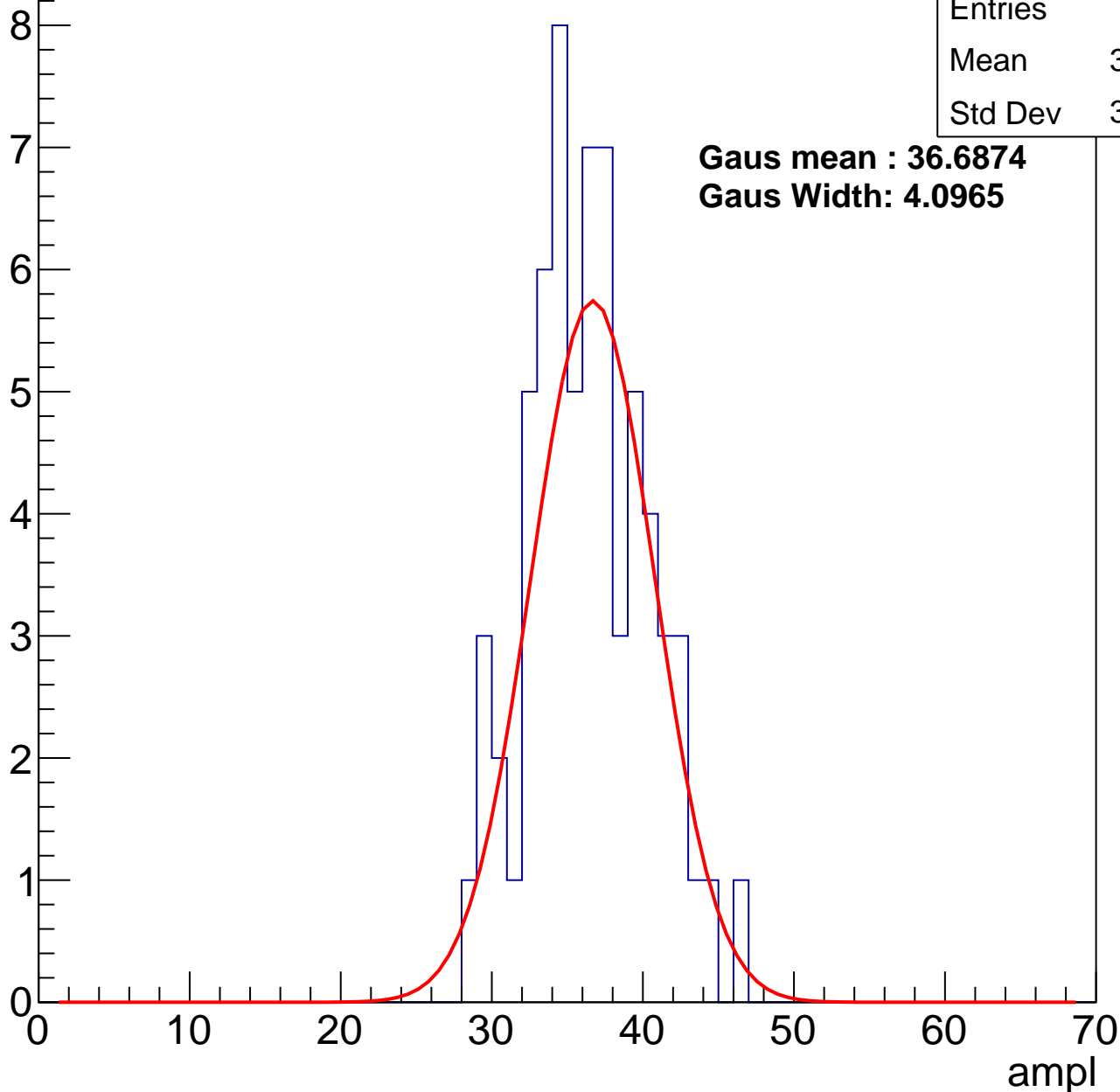
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	35.95
Std Dev	3.898

**Gaus mean : 36.6874**

**Gaus Width: 4.0965**

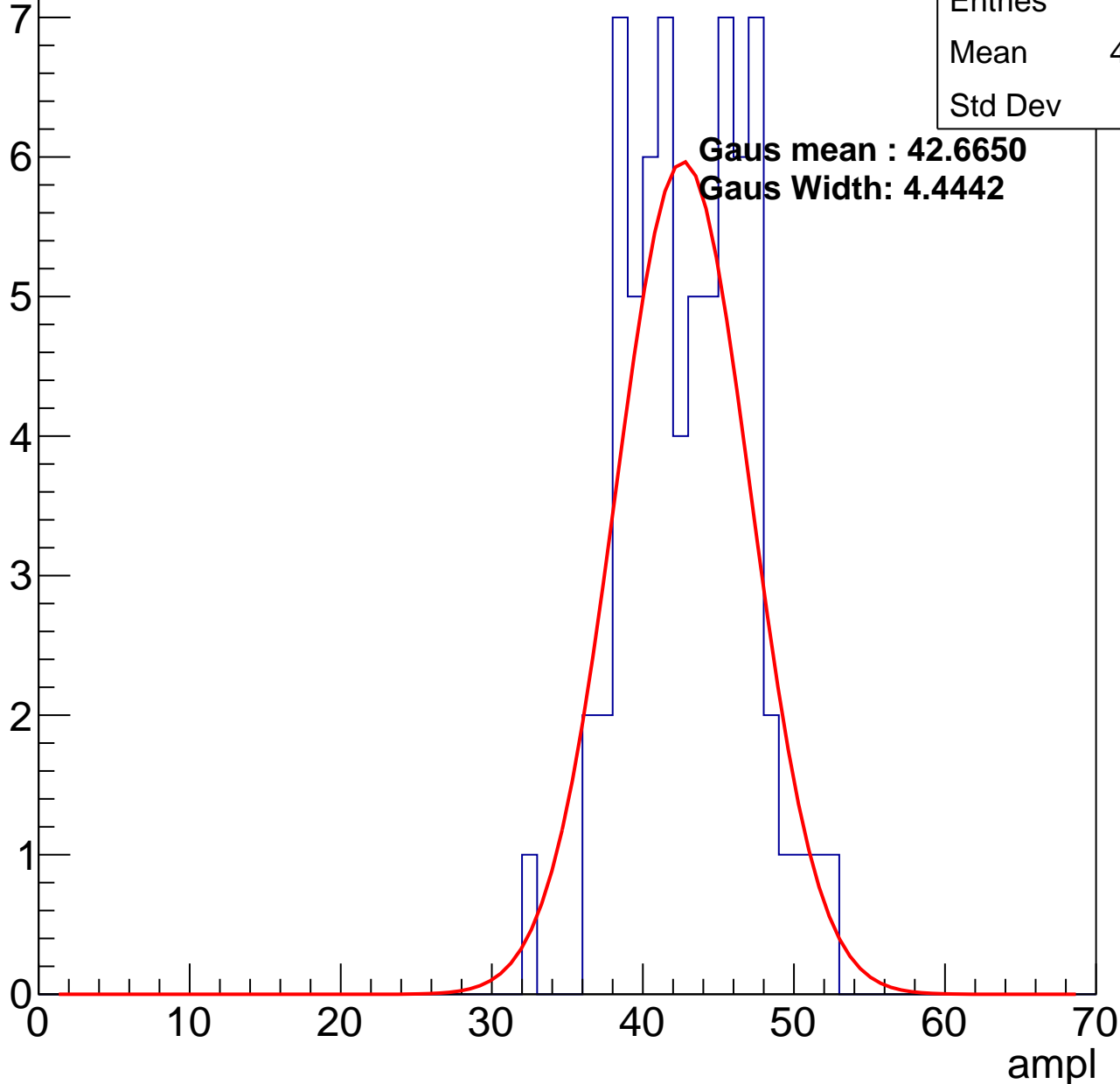


# B1L102S, U21-ch124, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	42.67
Std Dev	3.97

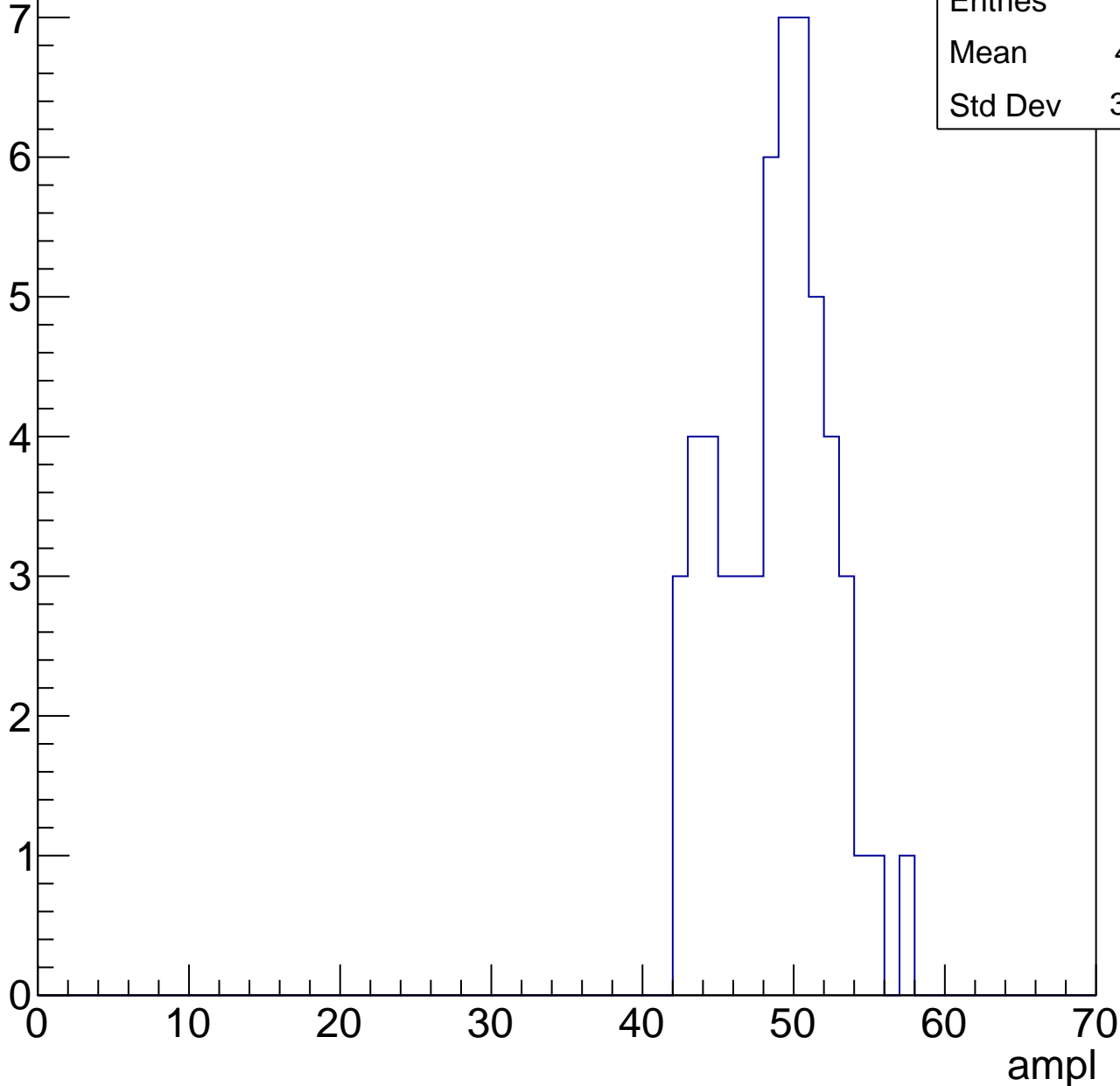


# B1L102S, U21-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	48.31
Std Dev	3.552

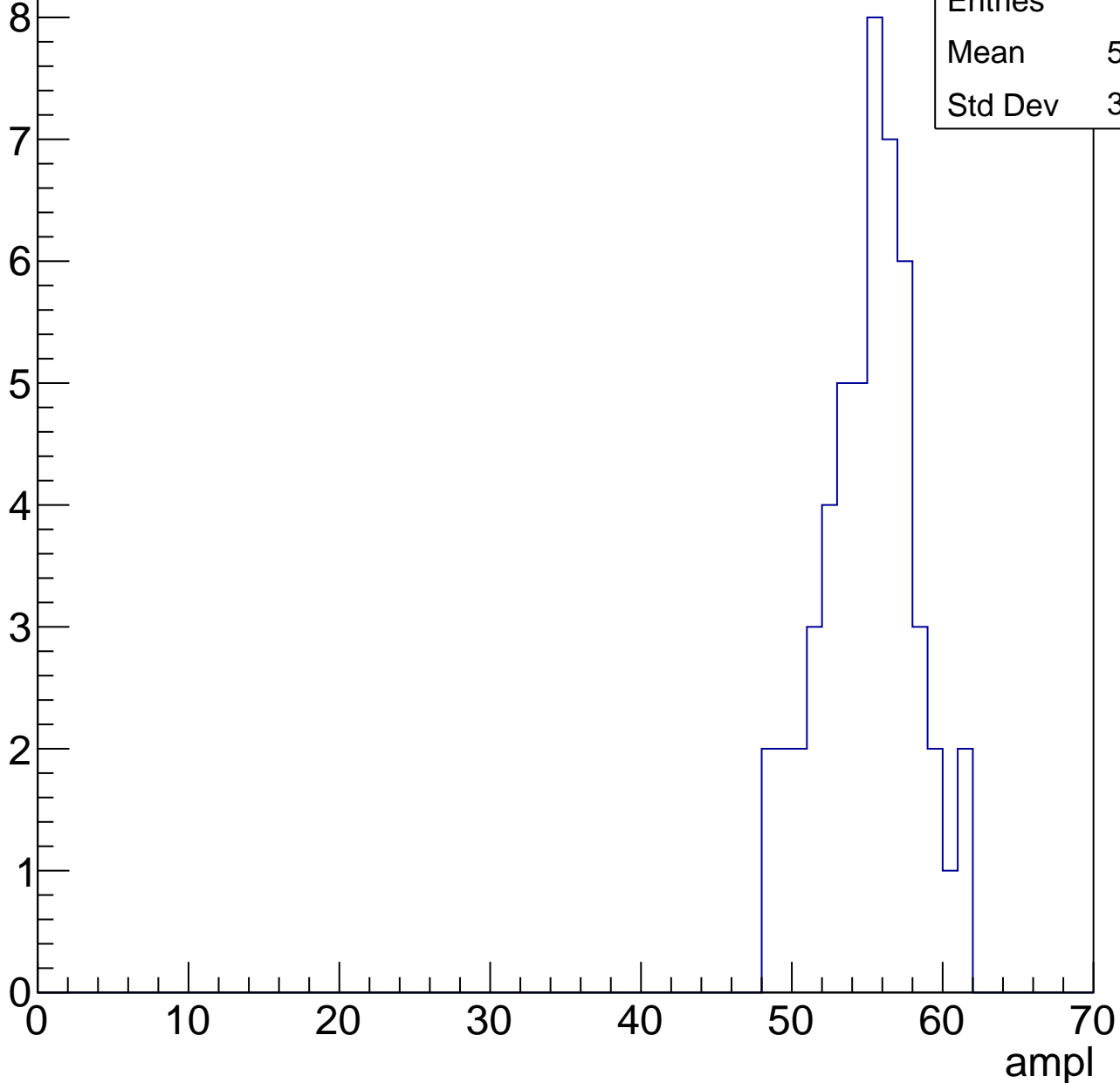


# B1L102S, U21-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	54.58
Std Dev	3.122

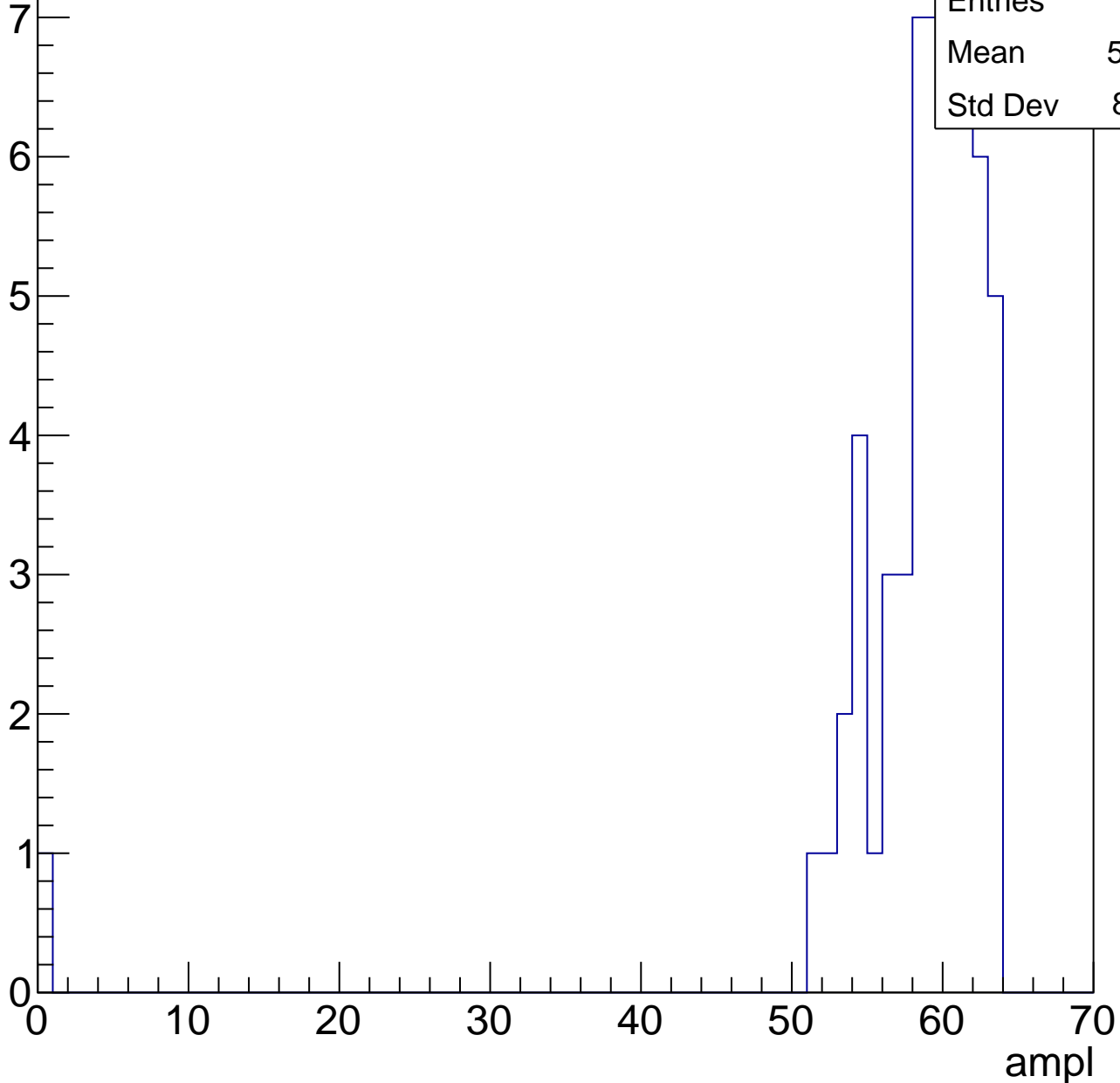


# B1L102S, U21-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

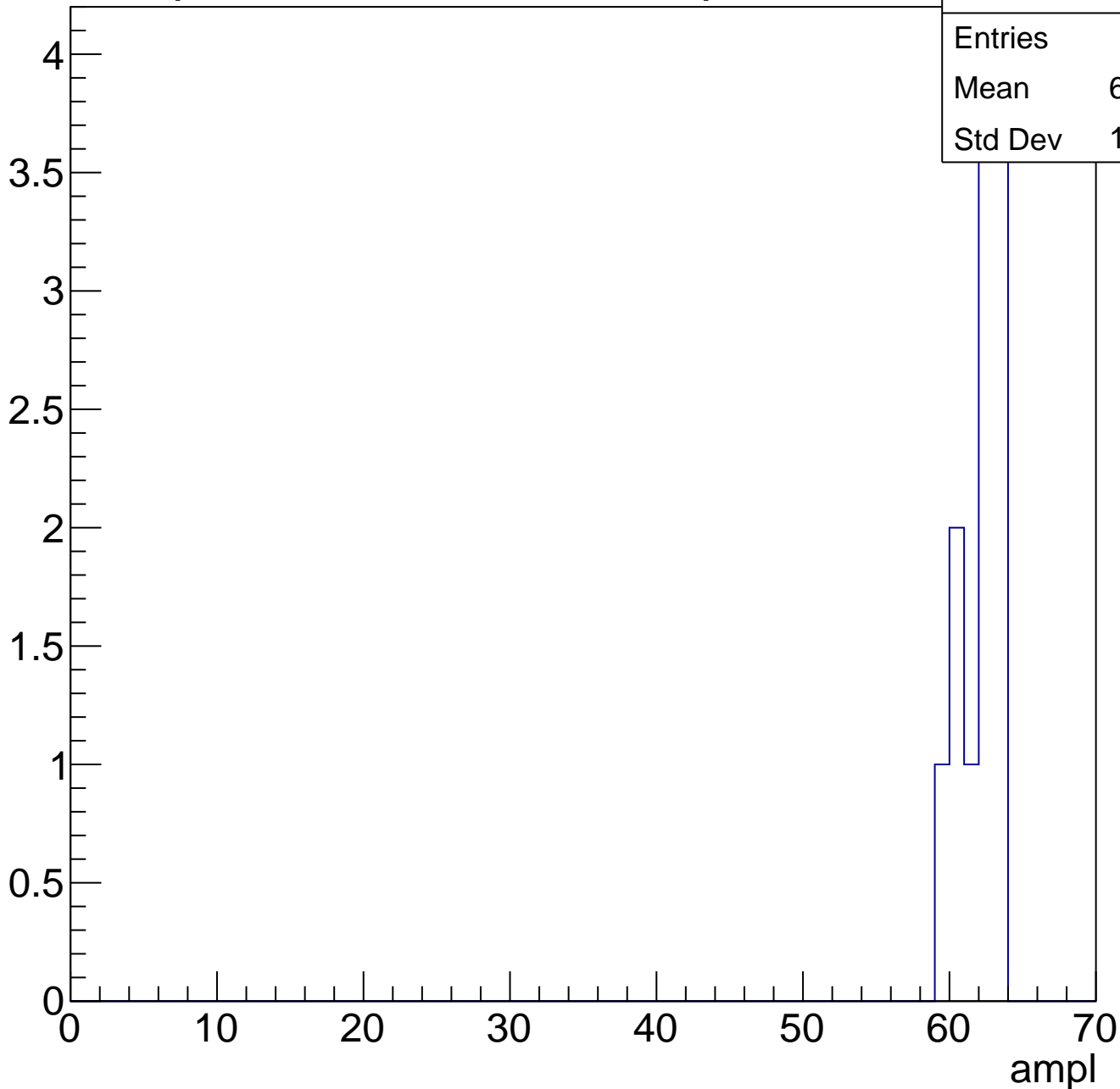
Entries	55
Mean	57.67
Std Dev	8.421



# B1L102S, U21-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U21-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch125, adc0

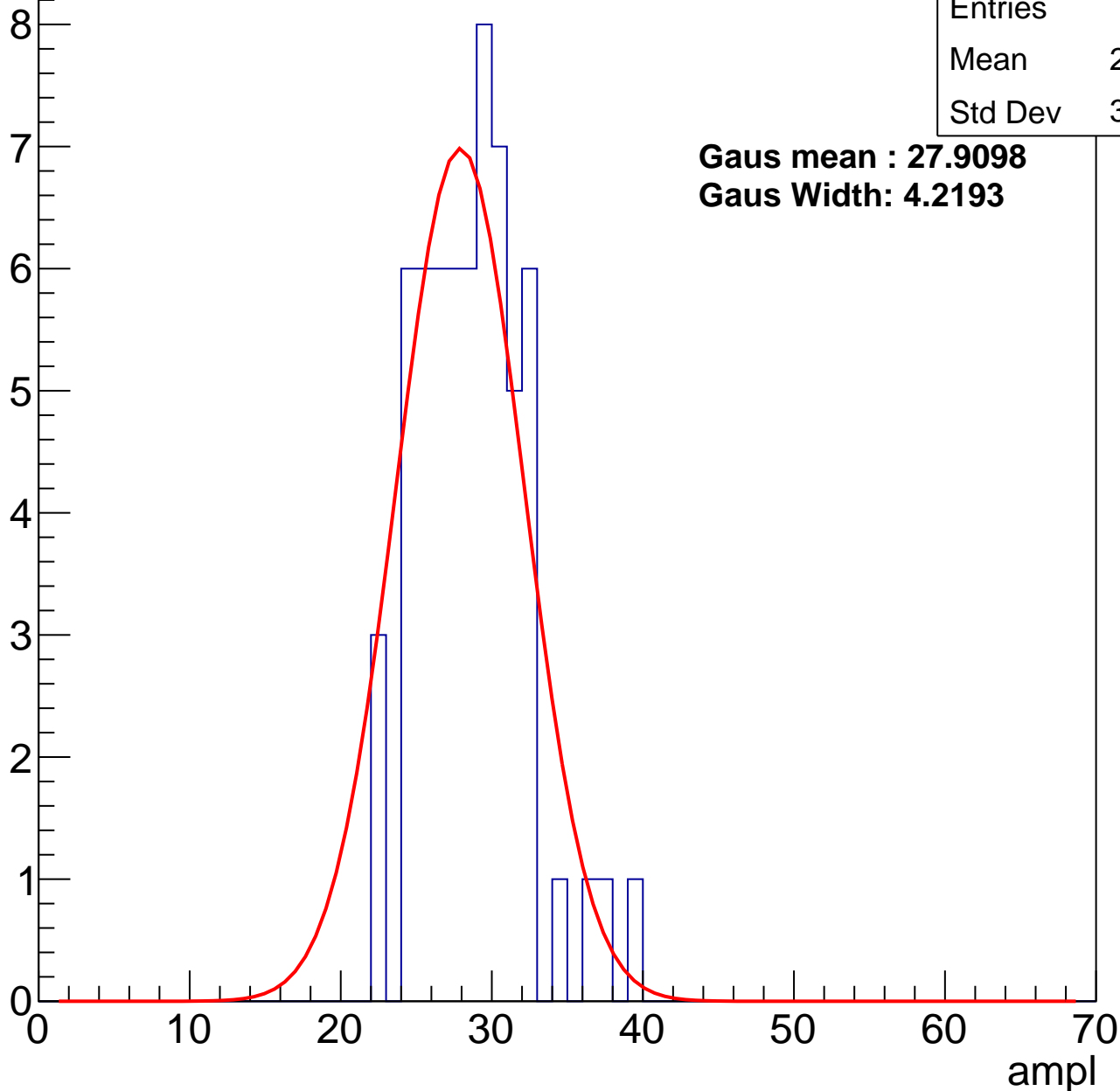
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	28.27
Std Dev	3.479

**Gaus mean : 27.9098**

**Gaus Width: 4.2193**



# B1L102S, U21-ch125, adc1

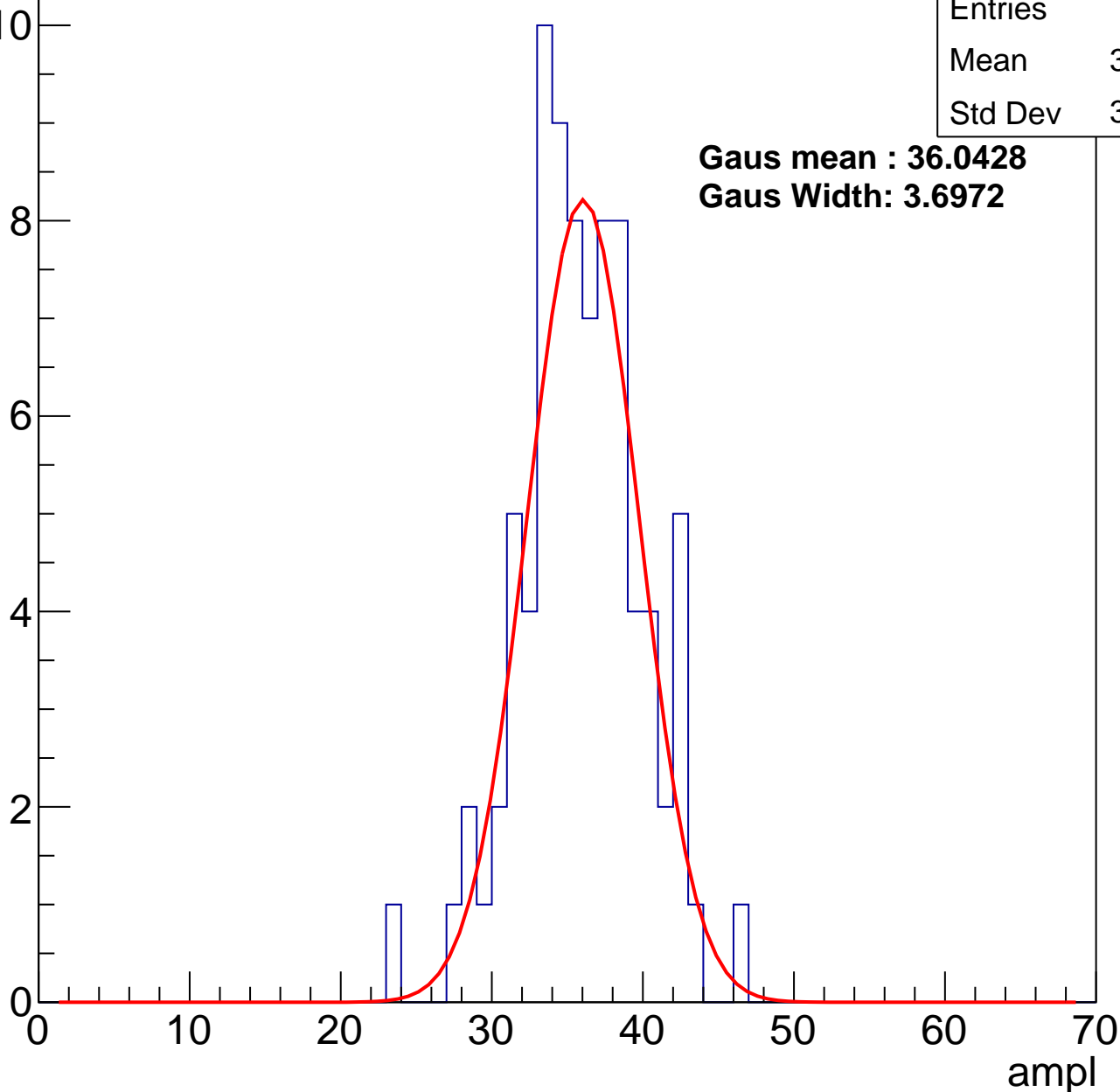
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	83
Mean	35.46
Std Dev	3.983

**Gaus mean : 36.0428**

**Gaus Width: 3.6972**



# B1L102S, U21-ch125, adc2

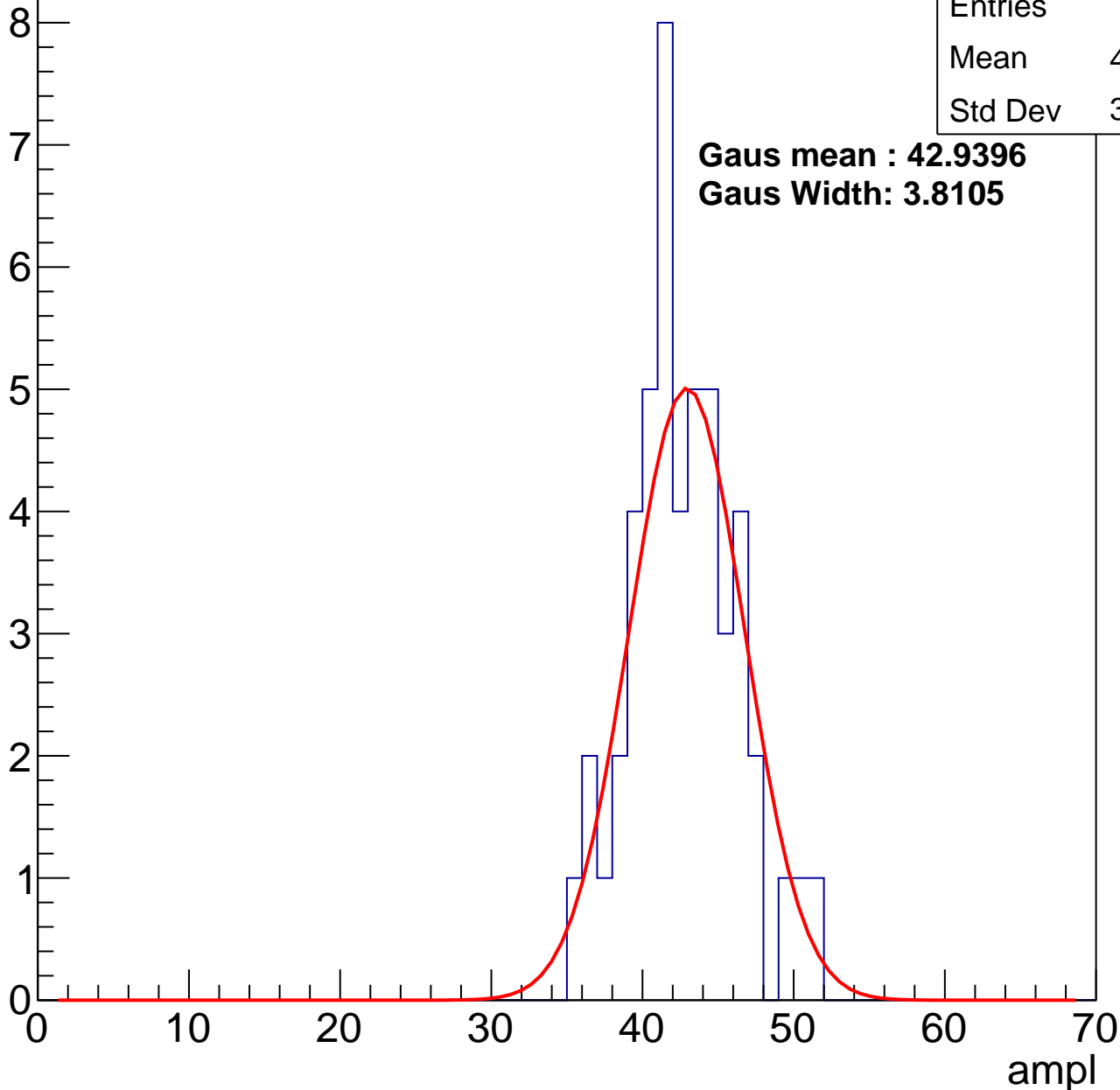
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	42.24
Std Dev	3.497

**Gaus mean : 42.9396**

**Gaus Width: 3.8105**

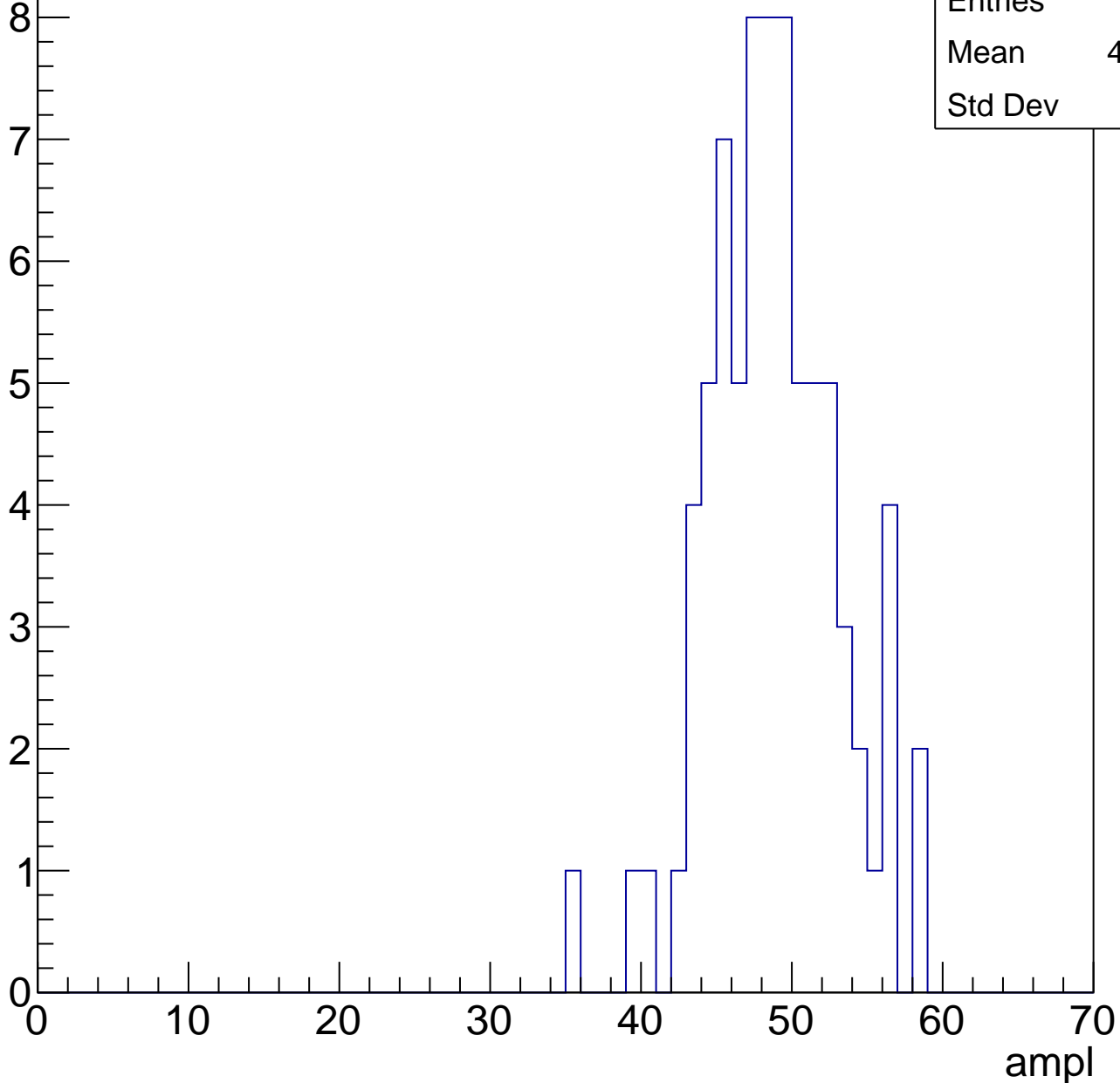


# B1L102S, U21-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	48.32
Std Dev	4.32

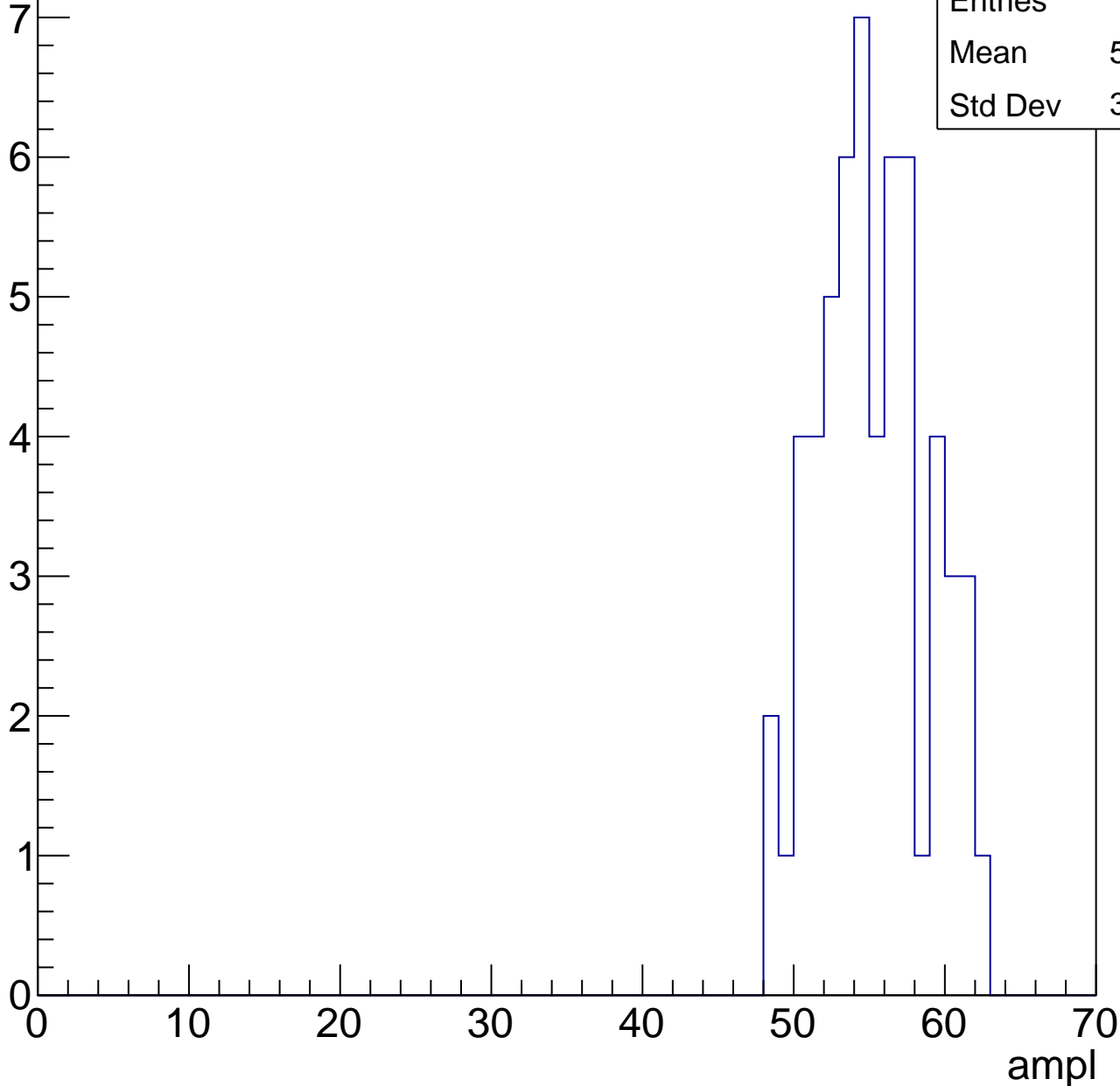


# B1L102S, U21-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

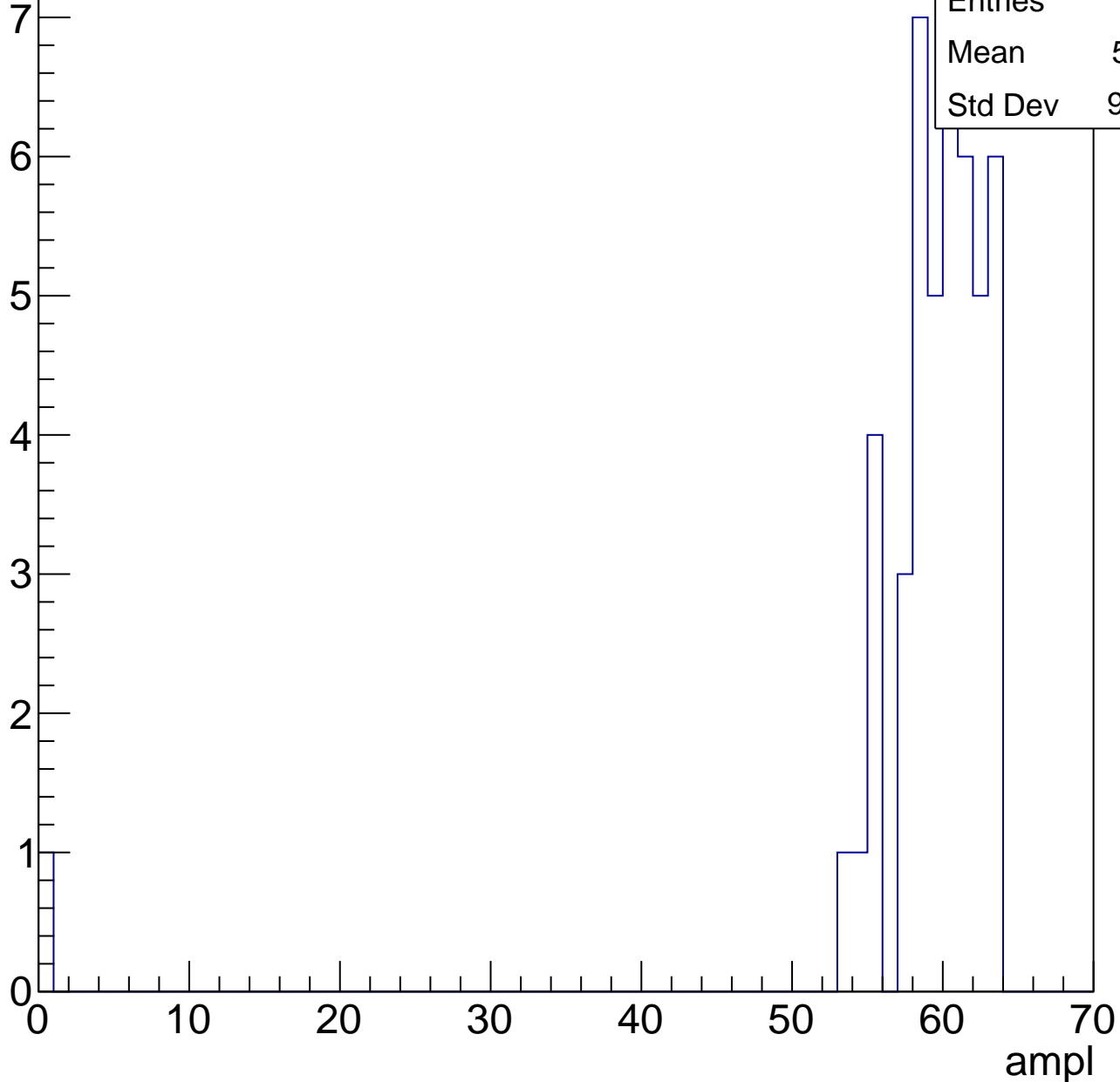
Entries	57
Mean	54.77
Std Dev	3.519



# B1L102S, U21-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

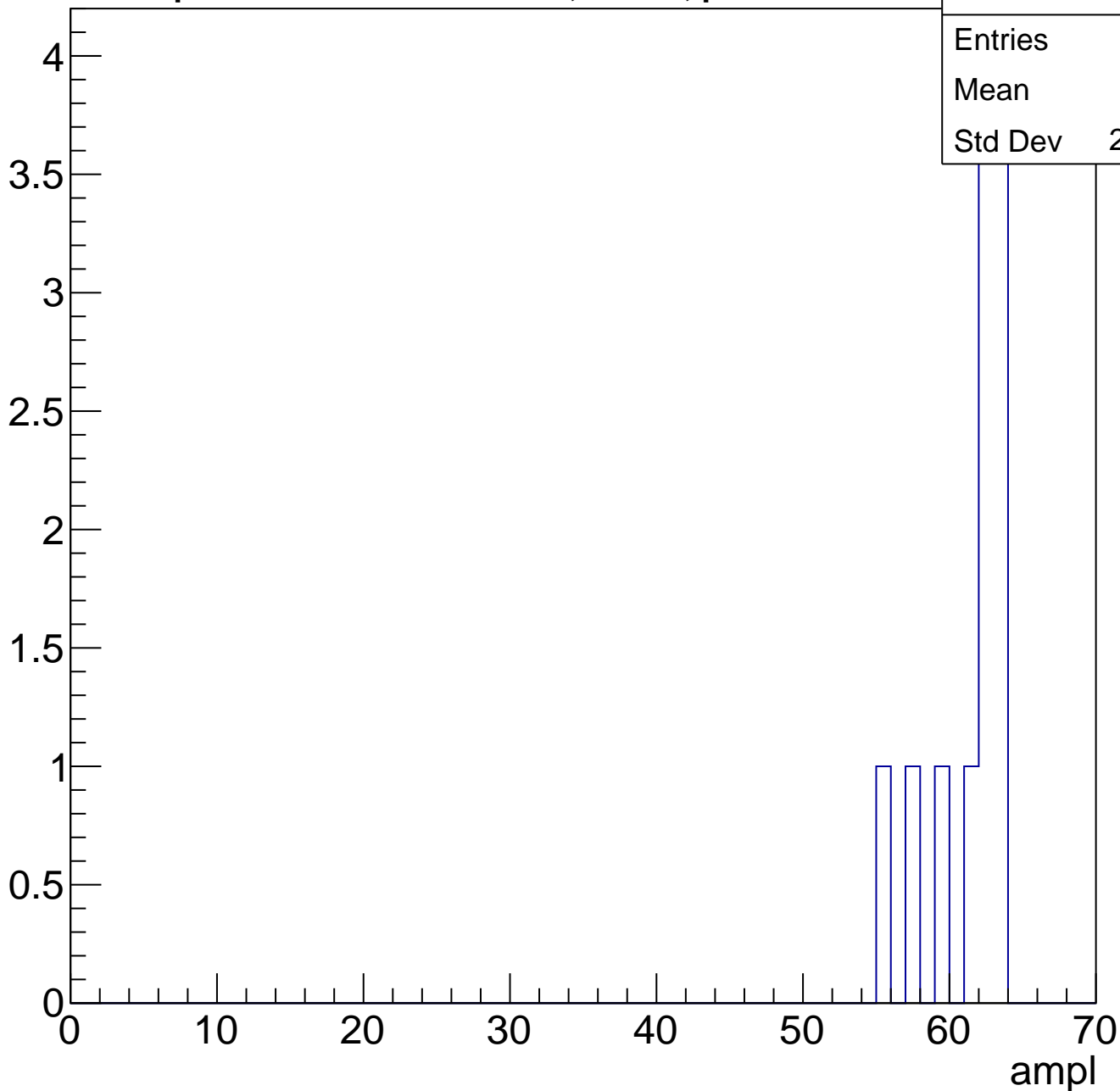
Entry



# B1L102S, U21-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



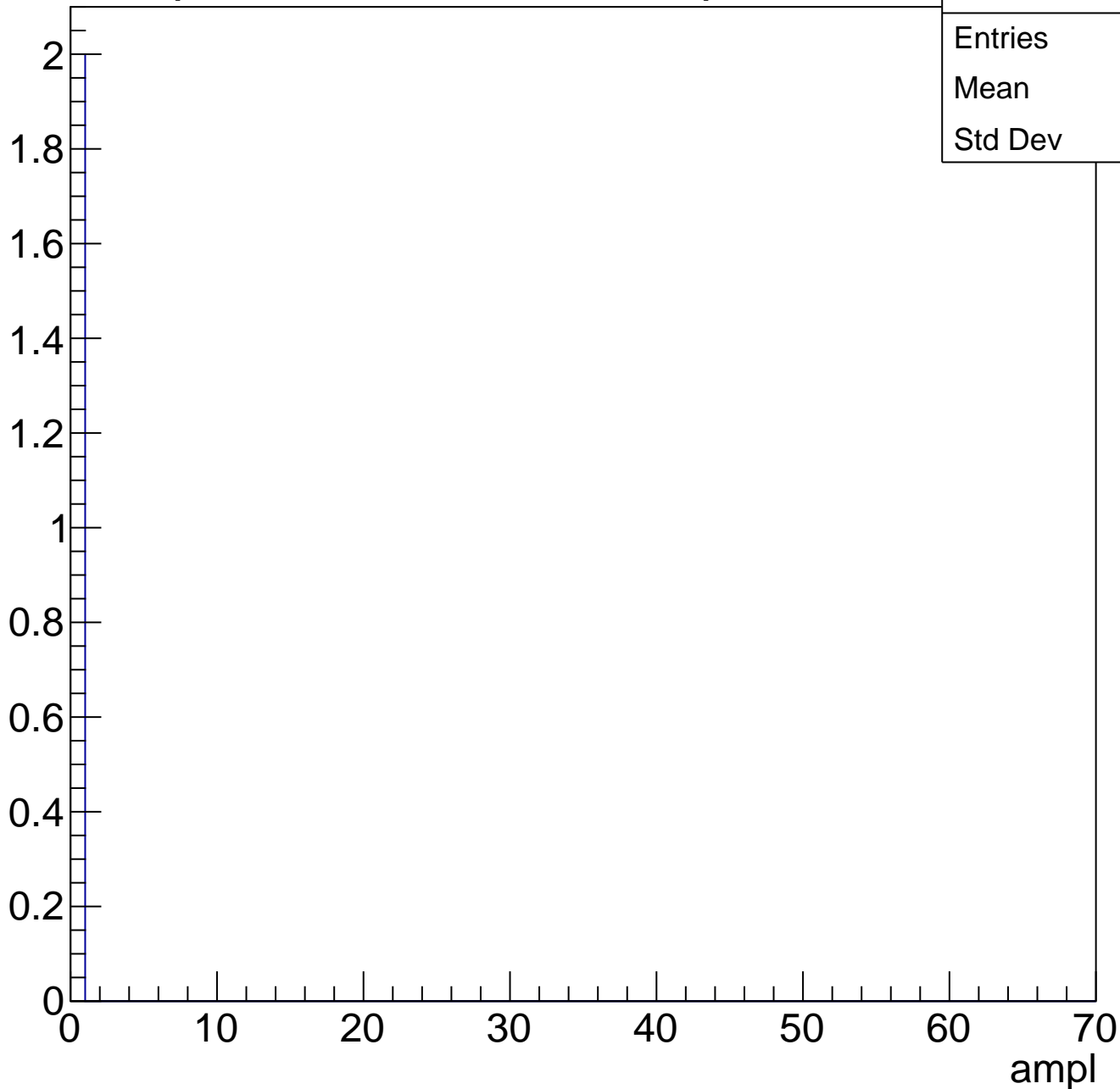
Entries	12
Mean	61
Std Dev	2.517



# B1L102S, U21-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U21-ch126, adc0

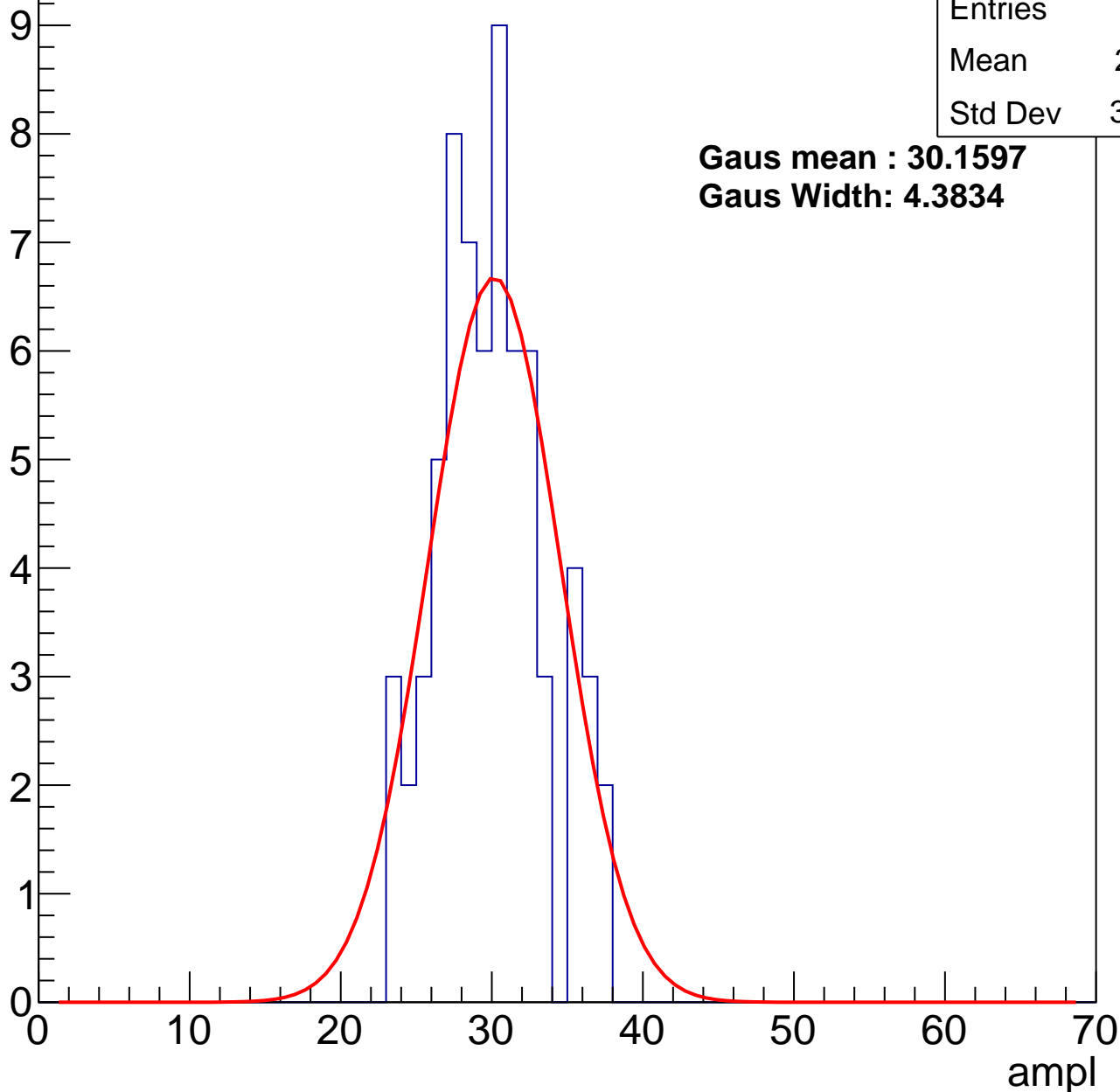
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	29.51
Std Dev	3.513

**Gaus mean : 30.1597**

**Gaus Width: 4.3834**



# B1L102S, U21-ch126, adc1

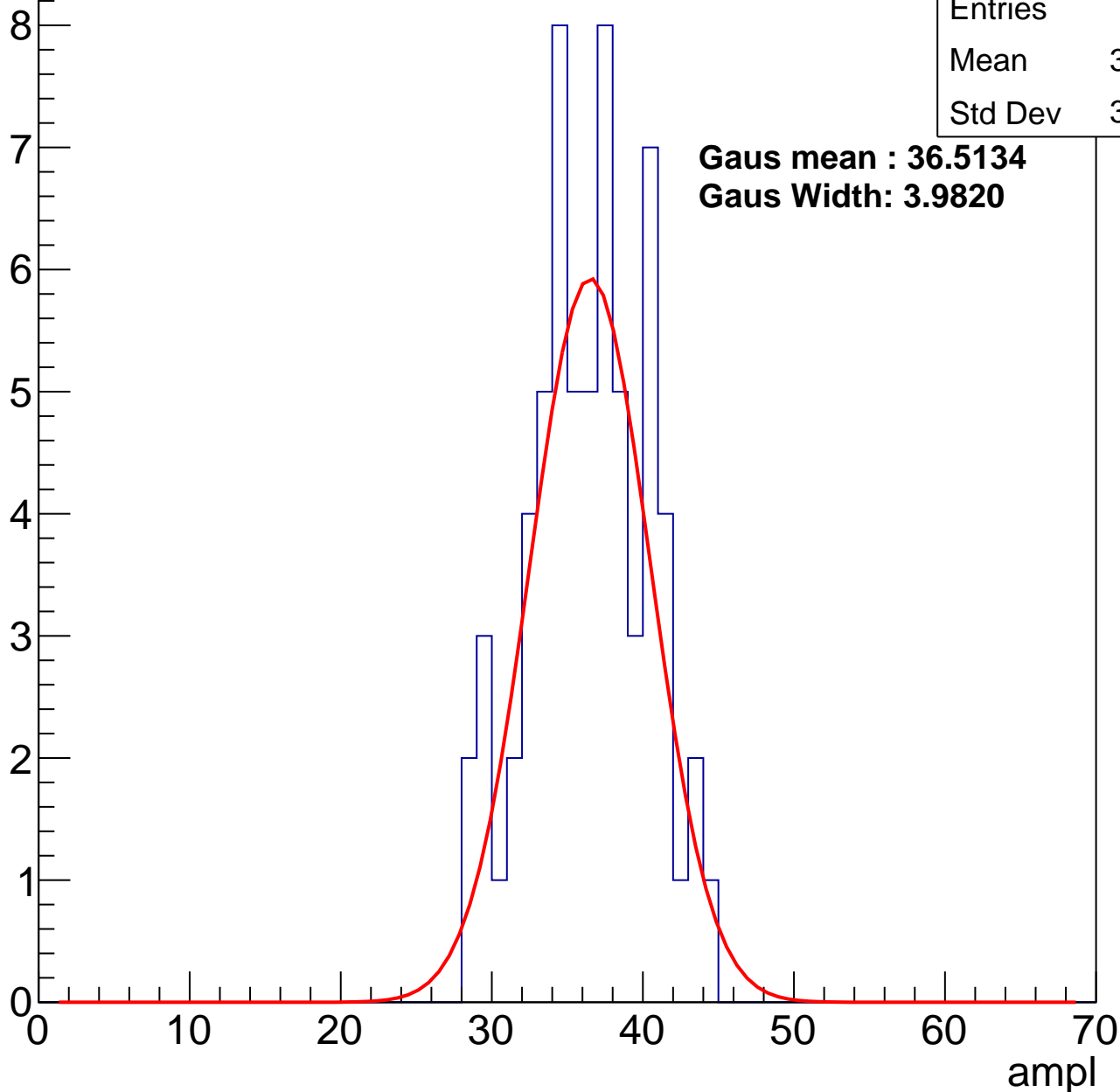
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	35.97
Std Dev	3.837

**Gaus mean : 36.5134**

**Gaus Width: 3.9820**



# B1L102S, U21-ch126, adc2

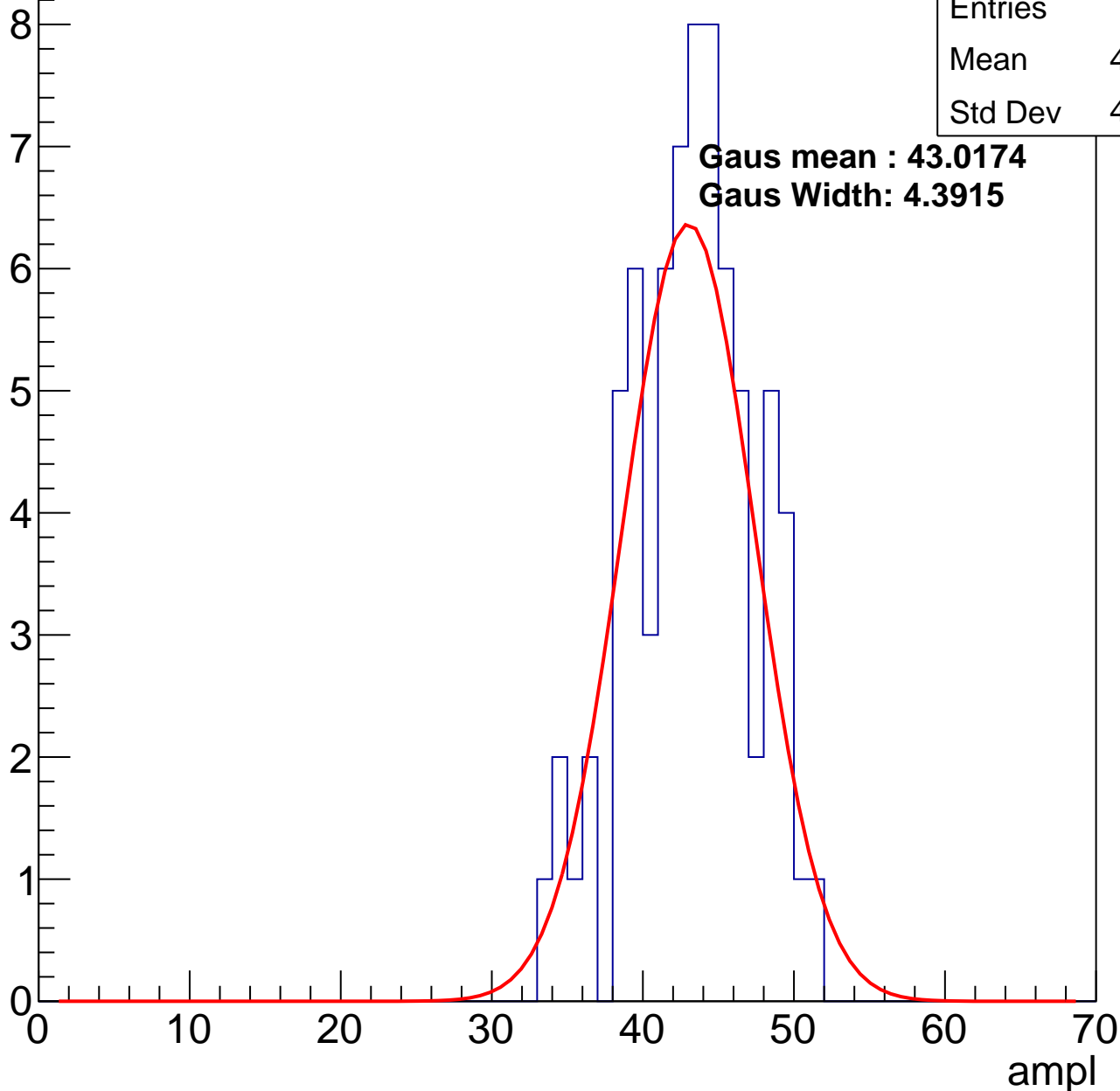
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	42.73
Std Dev	4.035

**Gaus mean : 43.0174**

**Gaus Width: 4.3915**

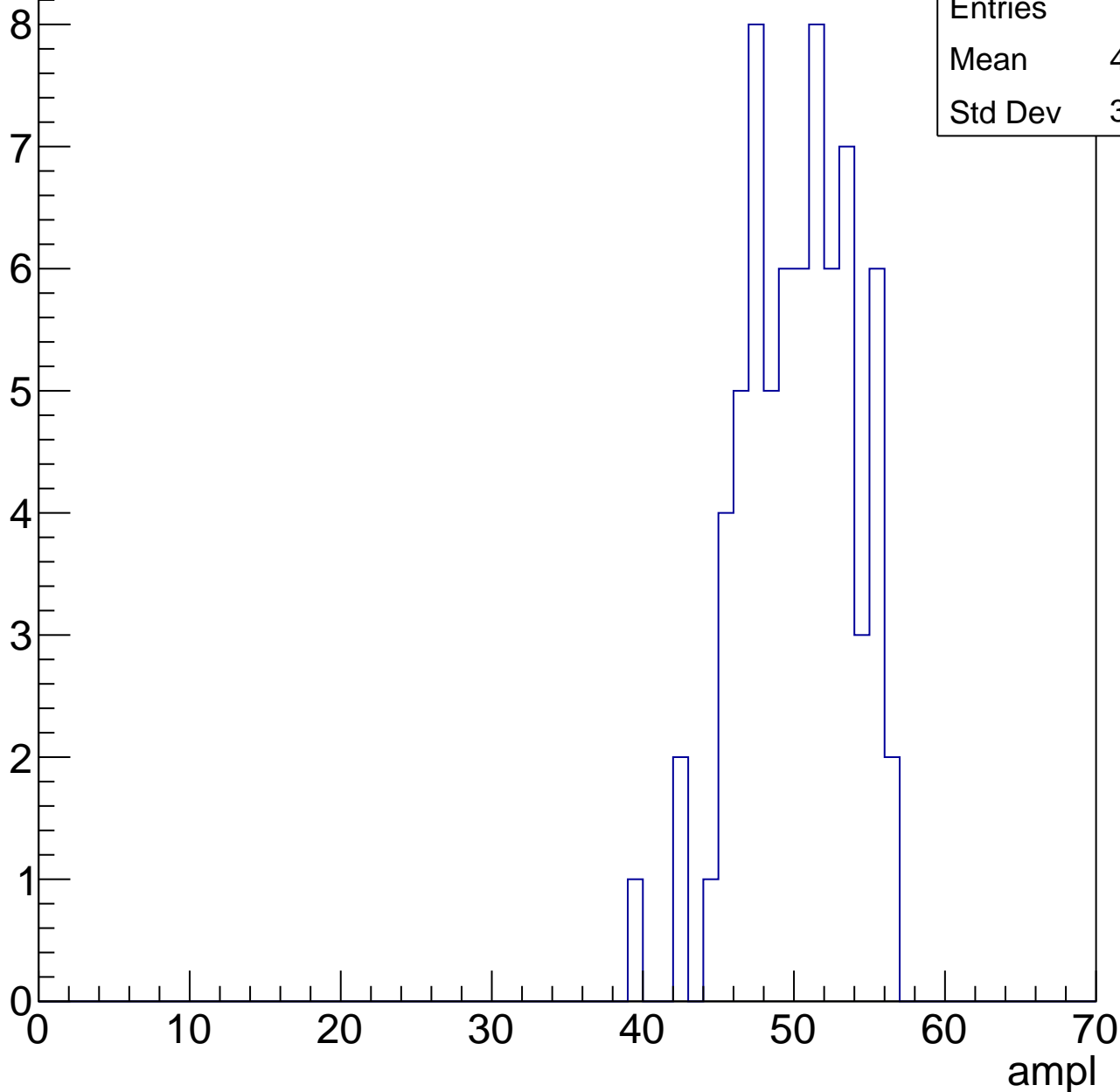


# B1L102S, U21-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	49.74
Std Dev	3.632

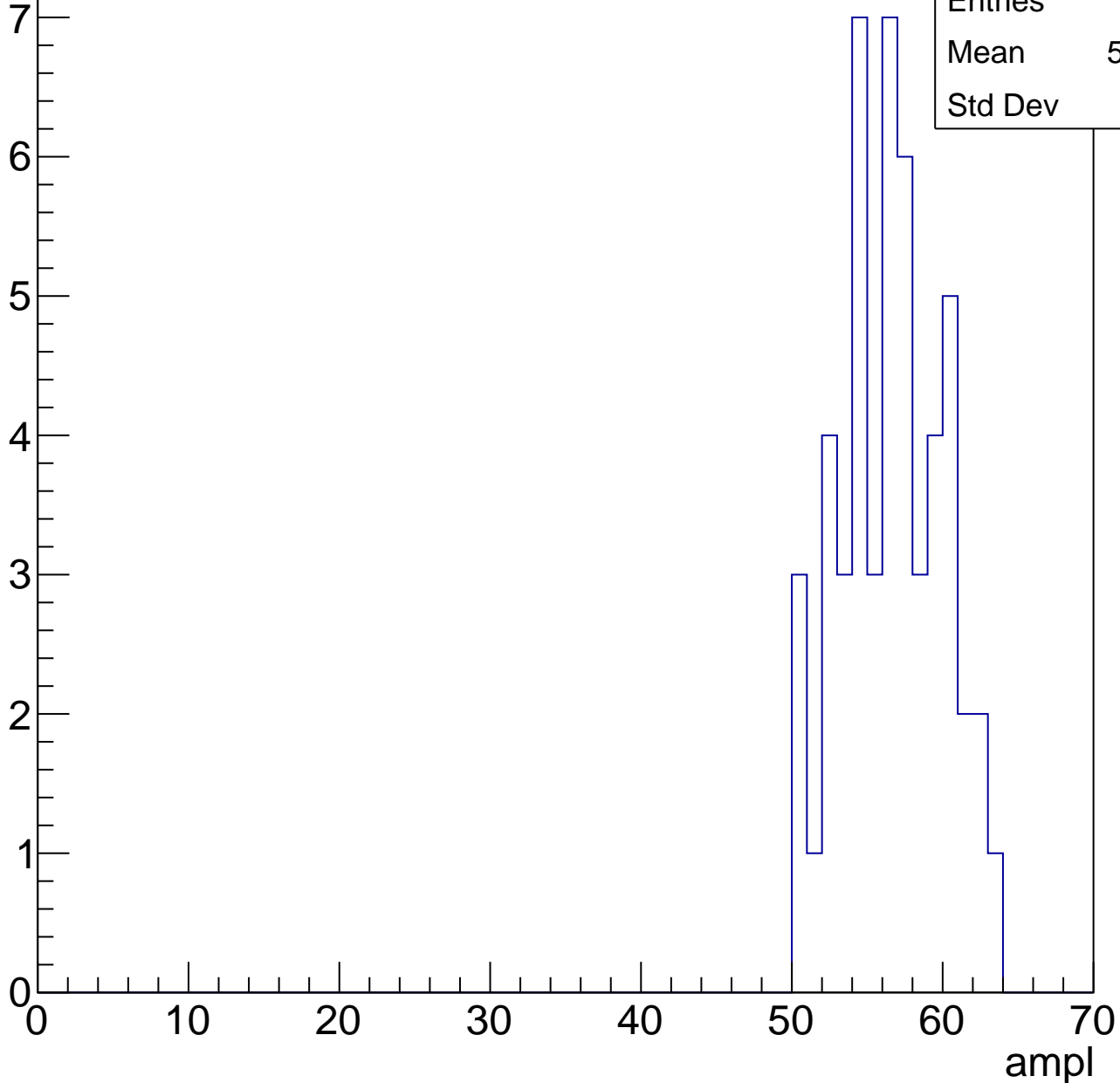


# B1L102S, U21-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

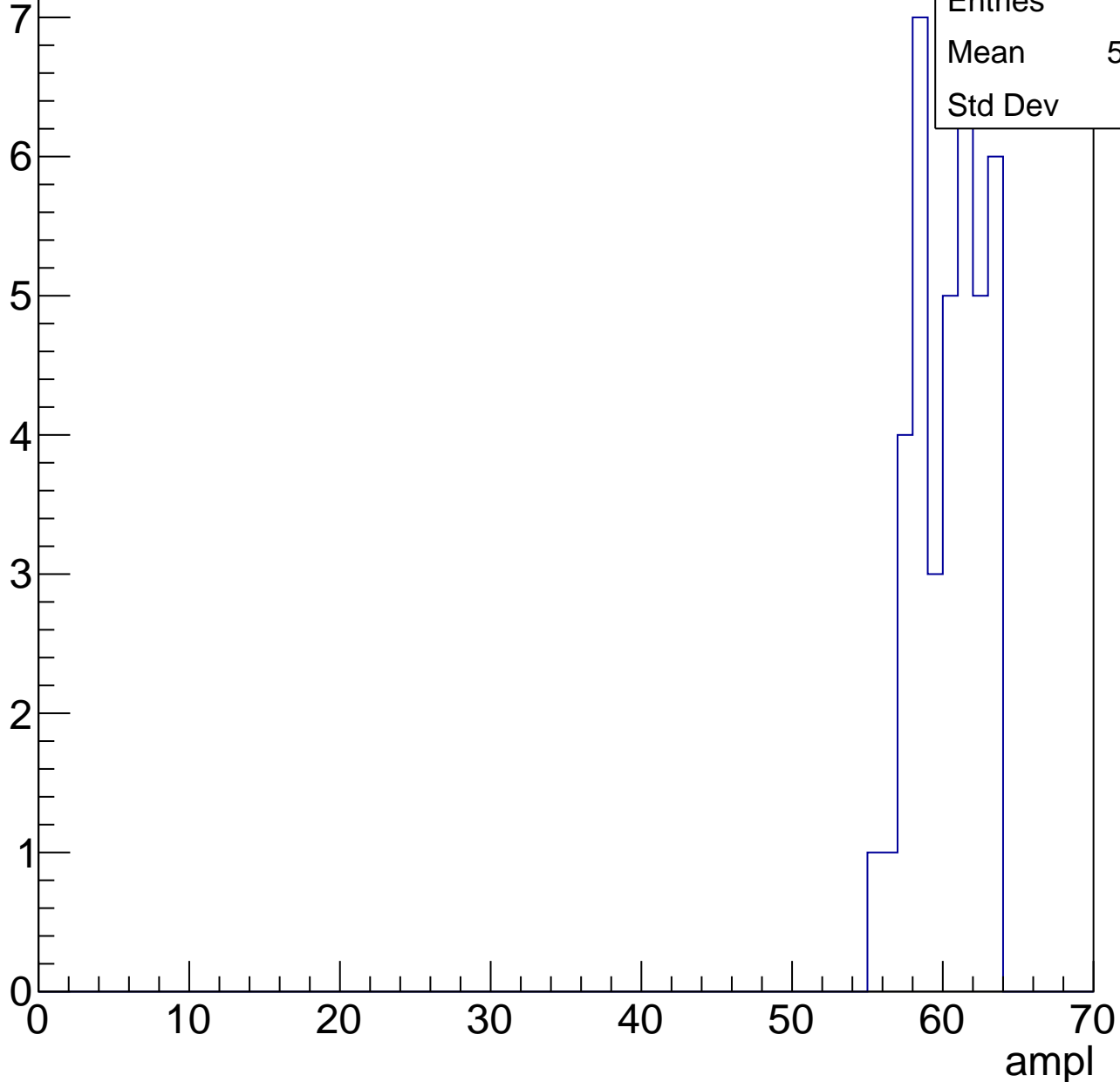
Entries	51
Mean	56.16
Std Dev	3.31



# B1L102S, U21-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	39
Mean	59.92
Std Dev	2.2

# B1L102S, U21-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries	11
Mean	55.73
Std Dev	17.69



# B1L102S, U21-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U21-ch127, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	89
Mean	26.38
Std Dev	6.341

**Gaus mean : 28.1734**

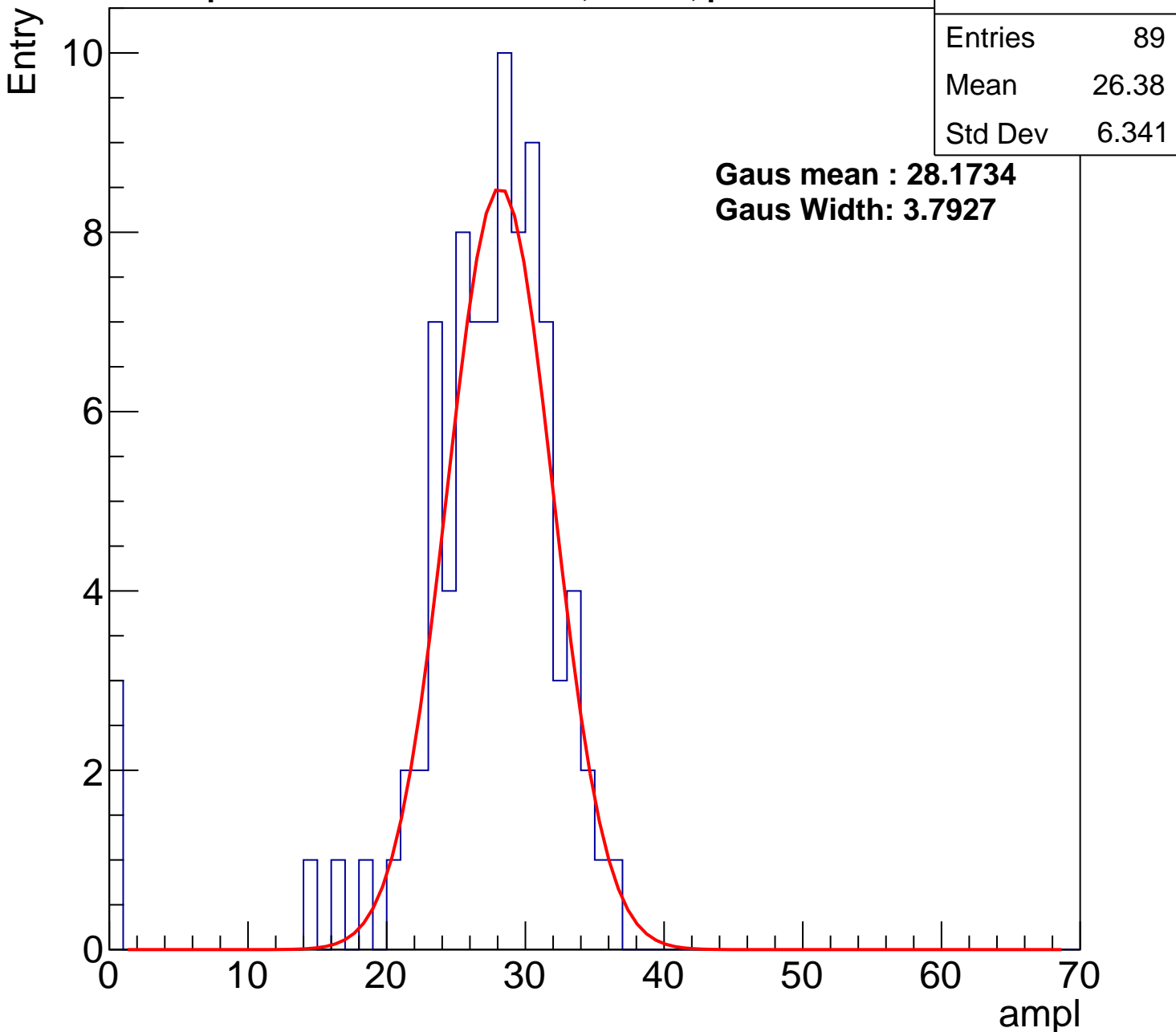
**Gaus Width: 3.7927**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U21-ch127, adc1

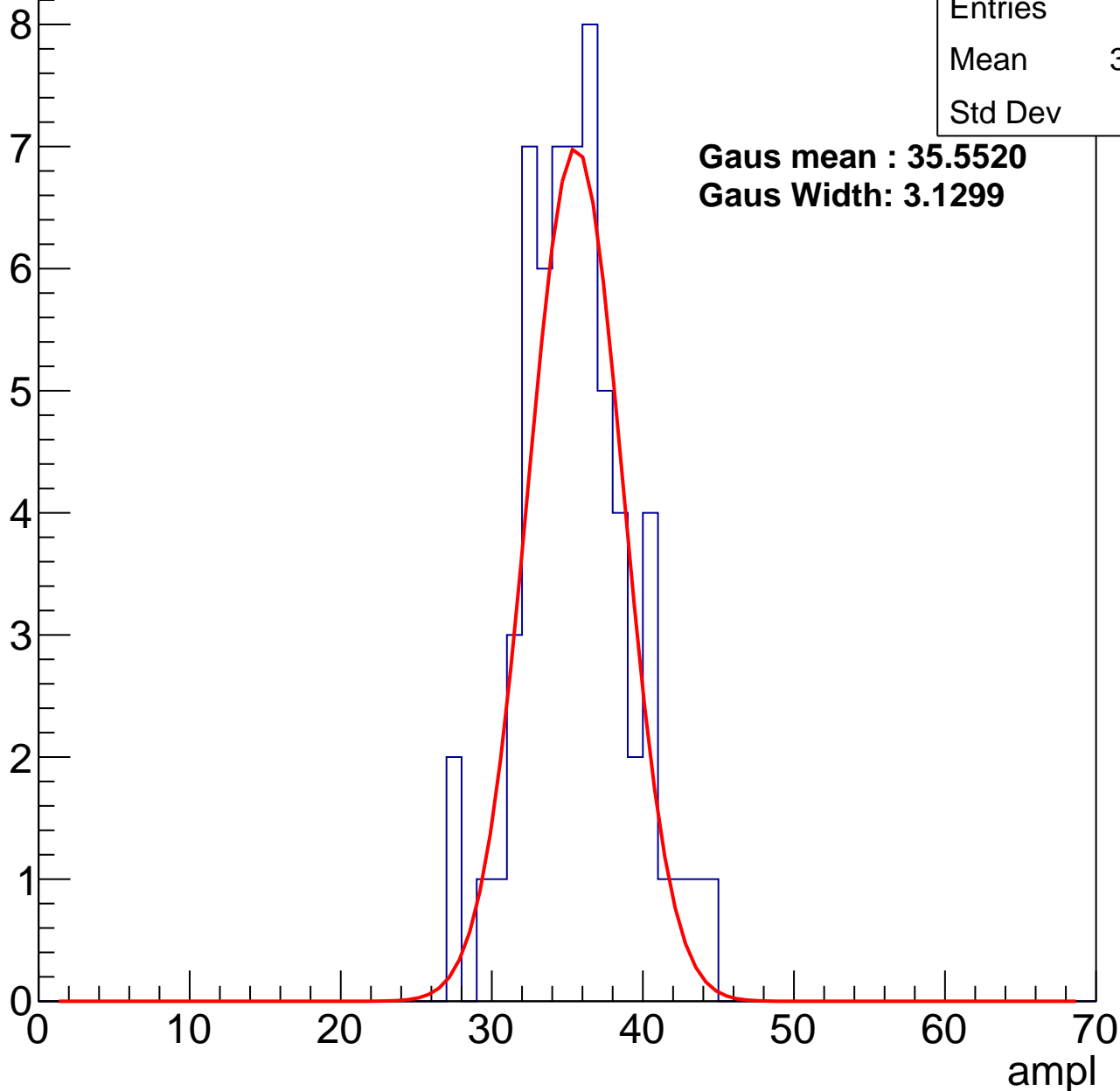
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	35.15
Std Dev	3.52

**Gaus mean : 35.5520**

**Gaus Width: 3.1299**



# B1L102S, U21-ch127, adc2

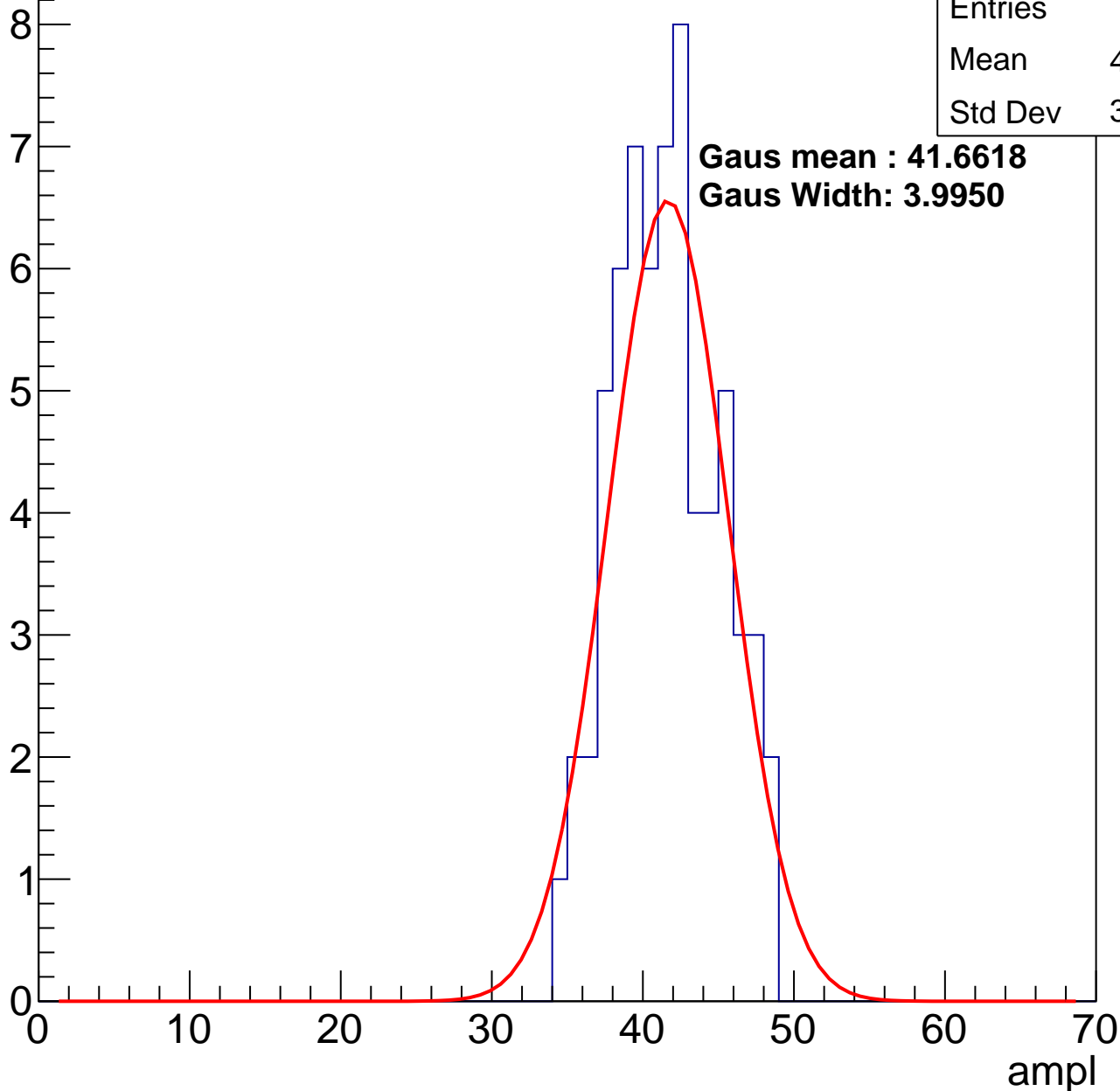
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	41.12
Std Dev	3.417

**Gaus mean : 41.6618**

**Gaus Width: 3.9950**

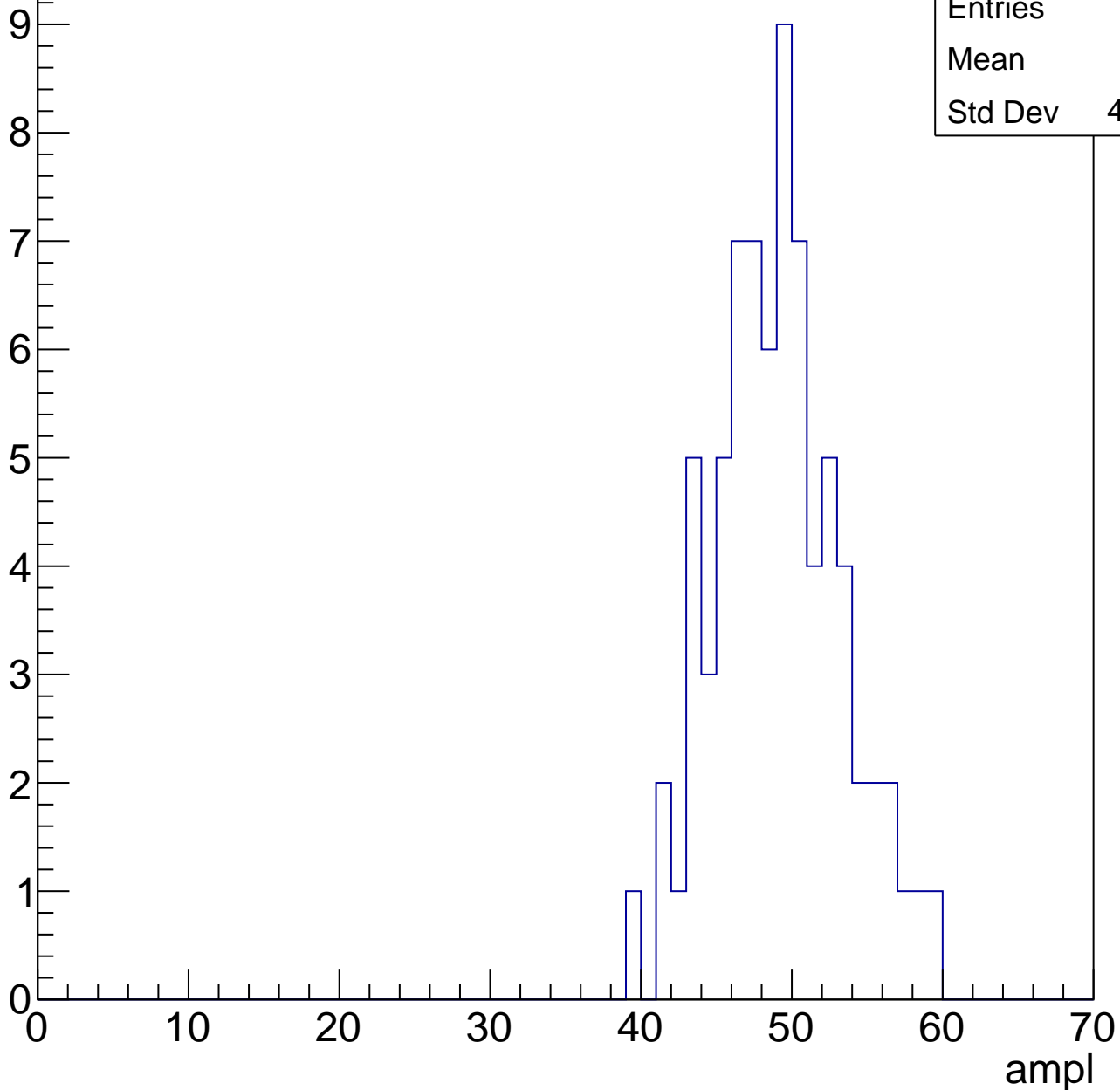


# B1L102S, U21-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	48.6
Std Dev	4.154

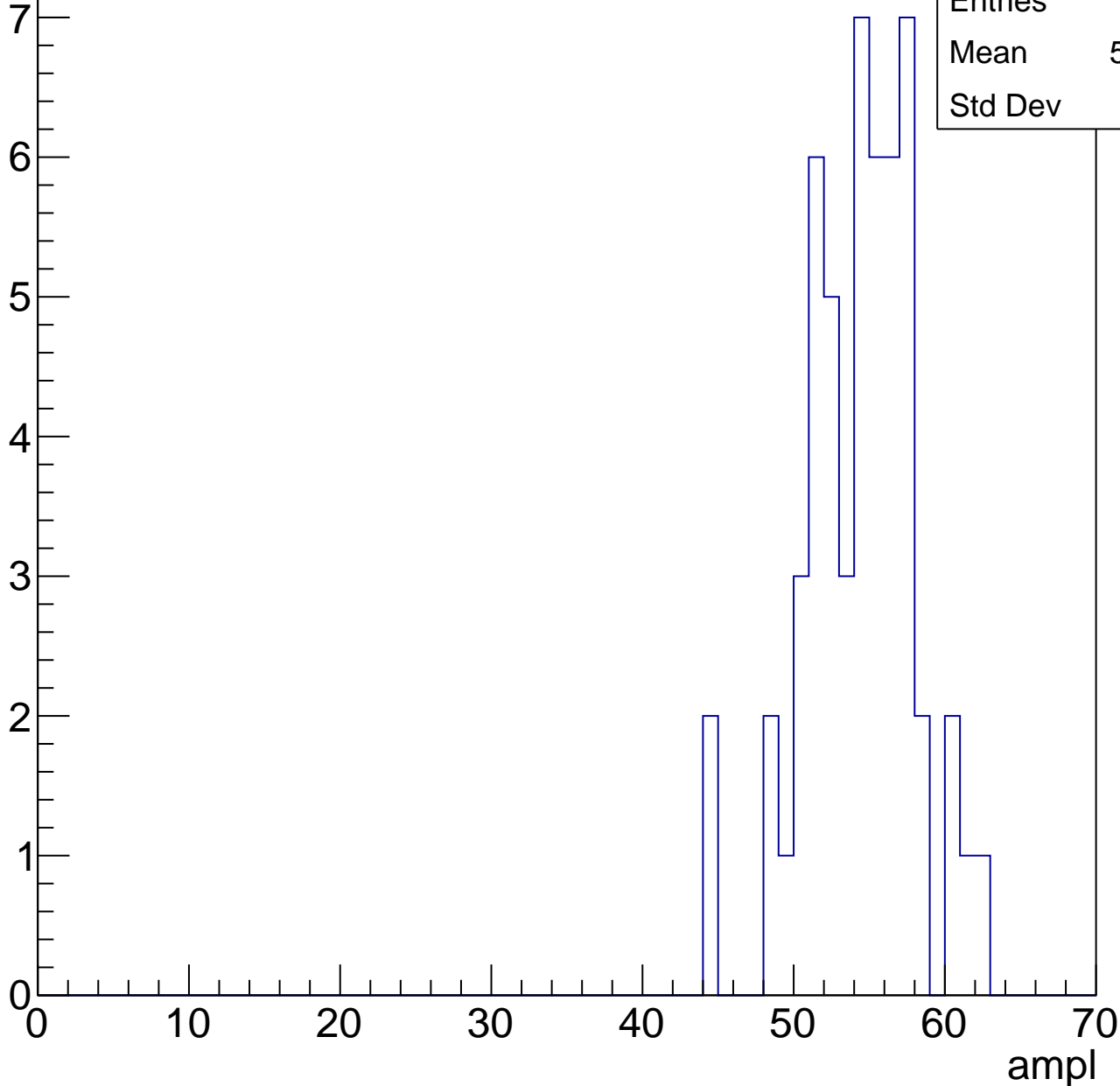


# B1L102S, U21-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	53.89
Std Dev	3.68

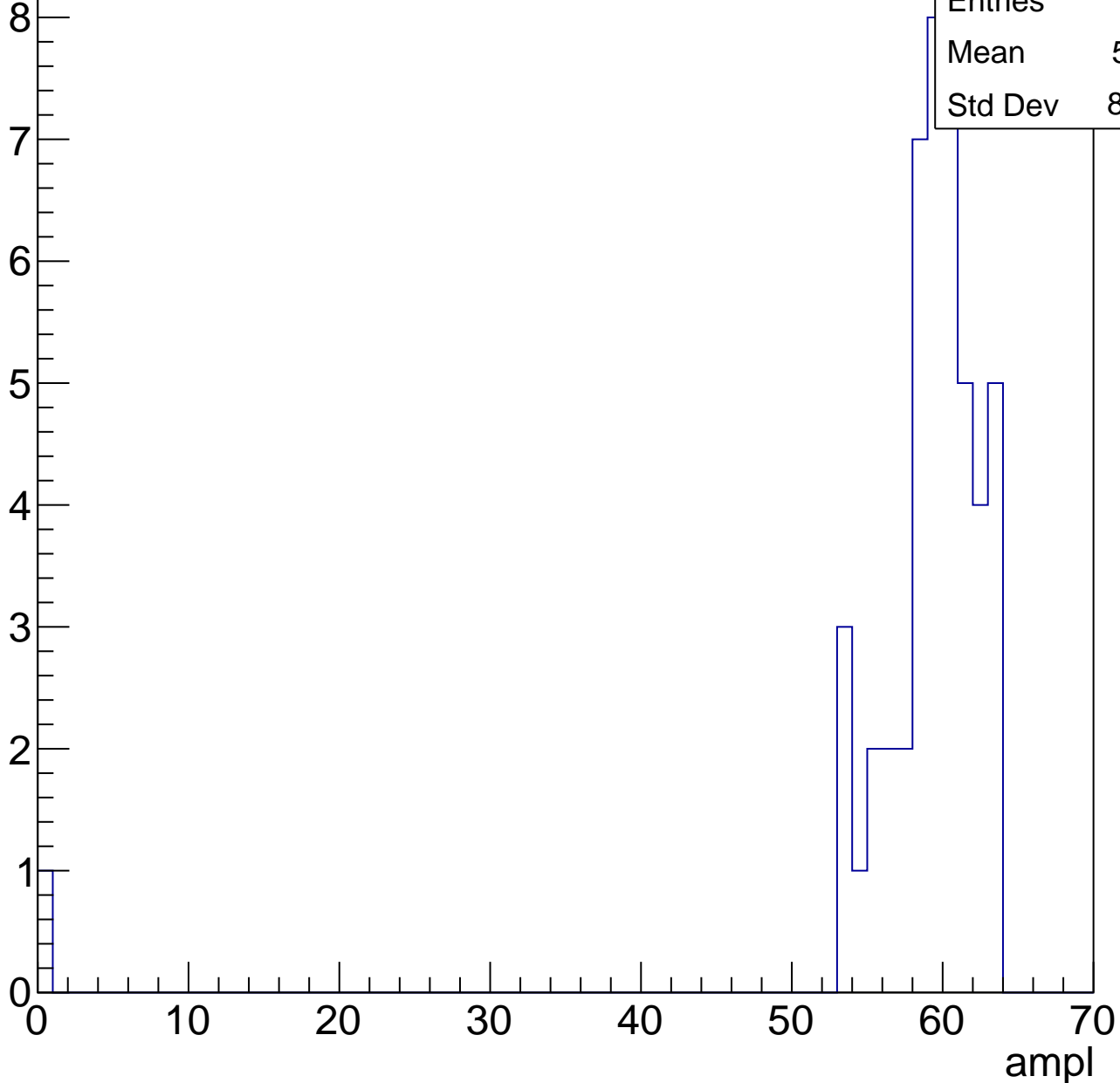


# B1L102S, U21-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	57.81
Std Dev	8.845

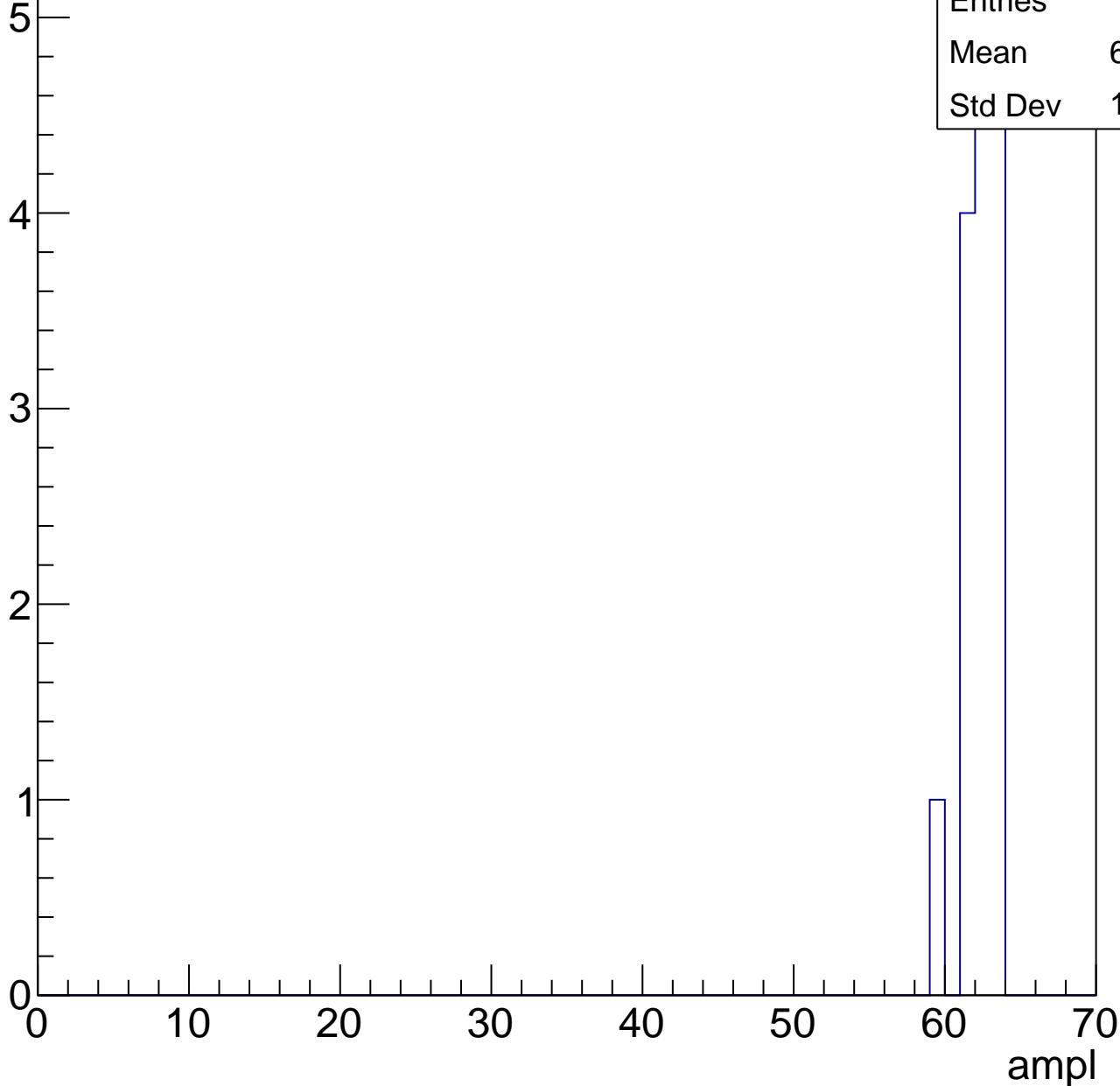


# B1L102S, U21-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	15
Mean	61.87
Std Dev	1.087





# B1L102S, U21-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U21-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0