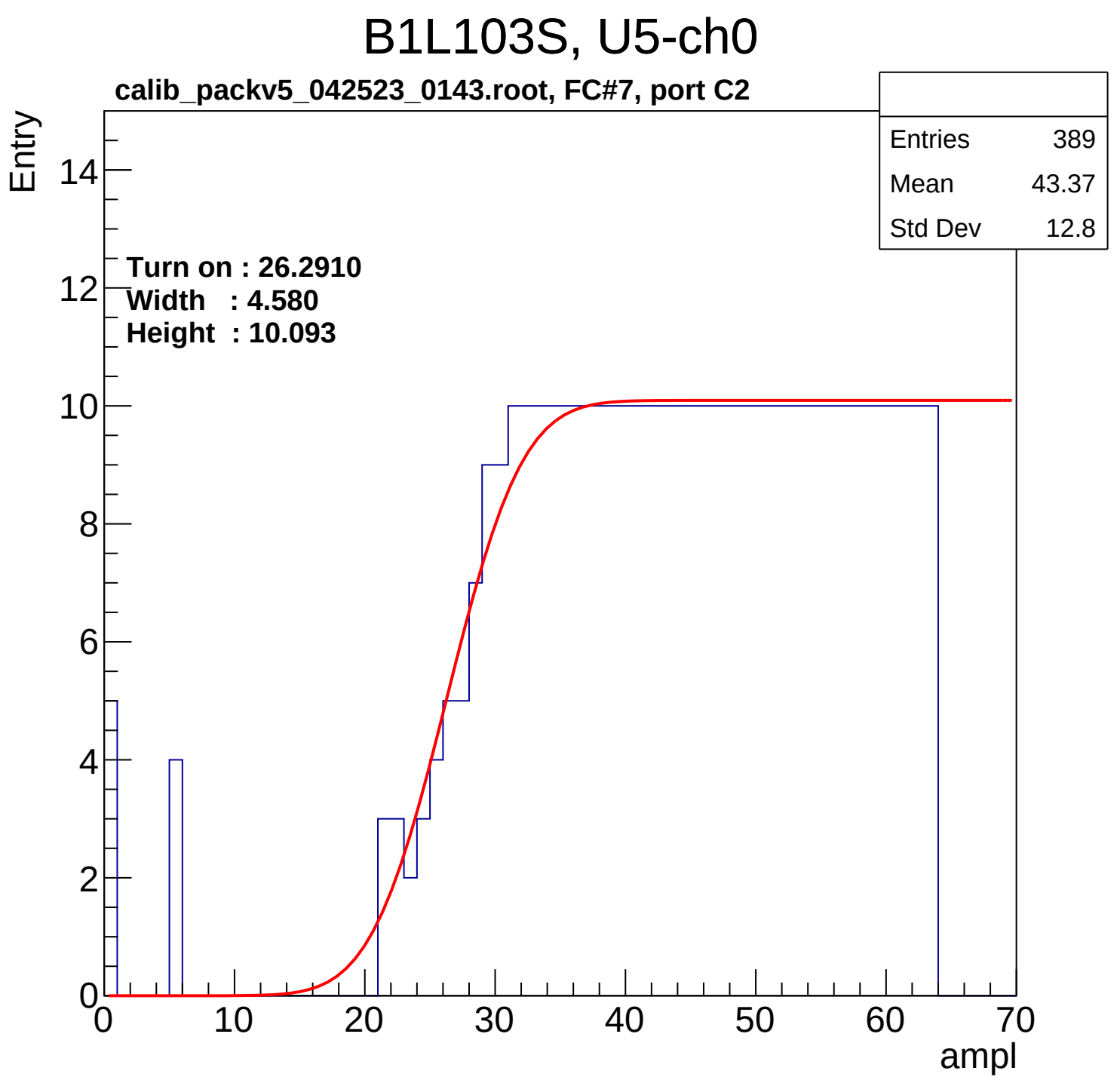
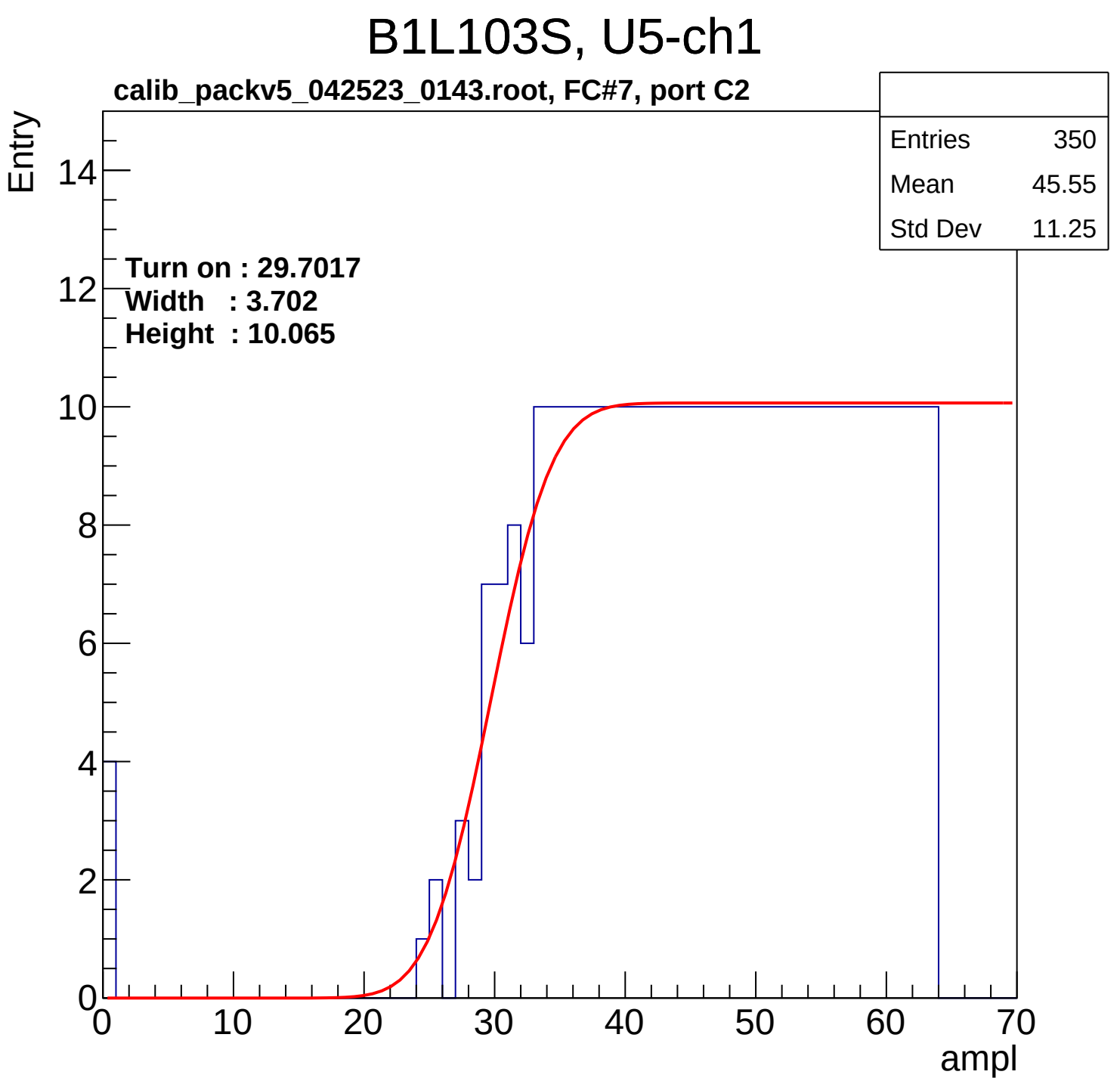
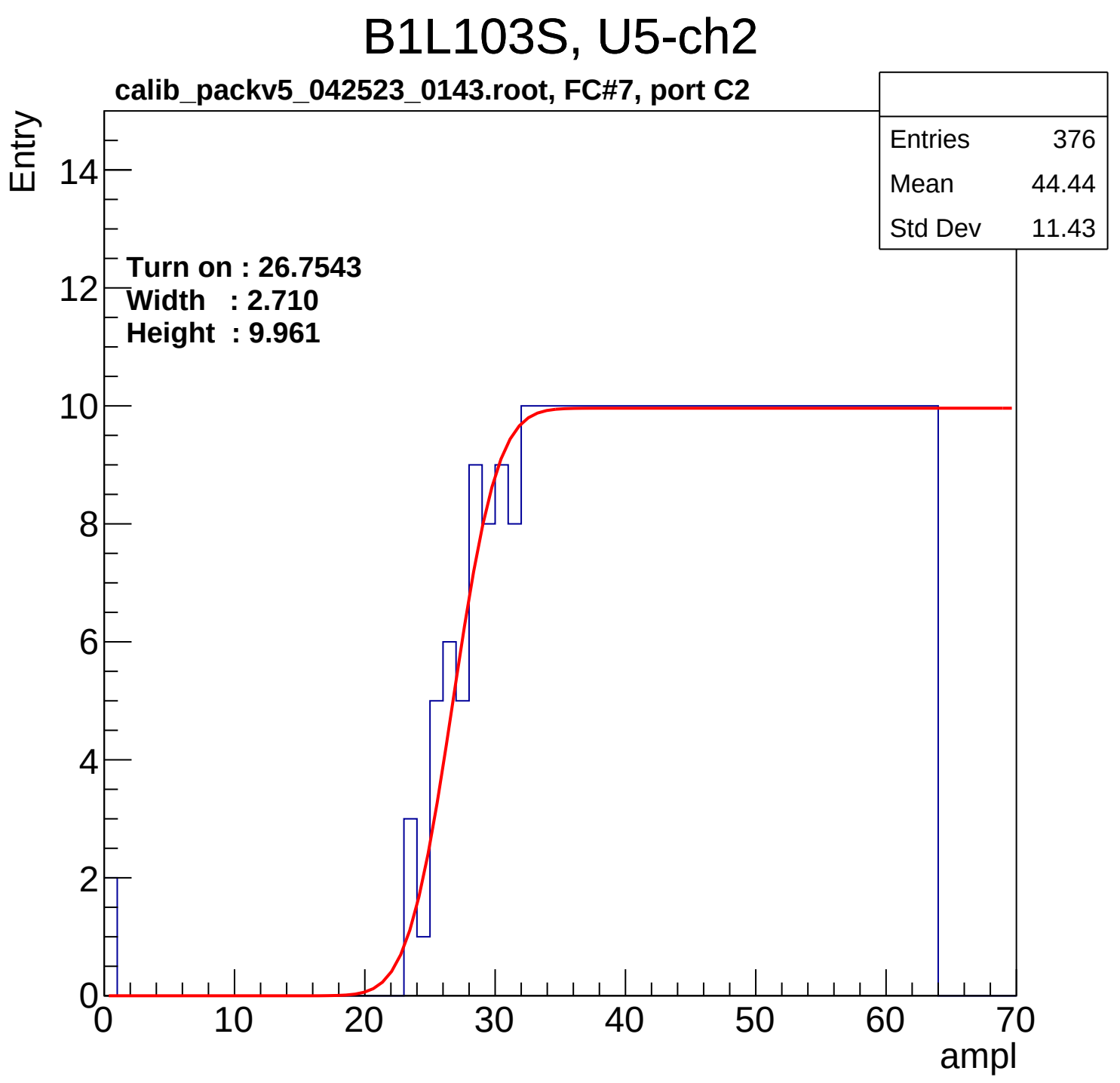
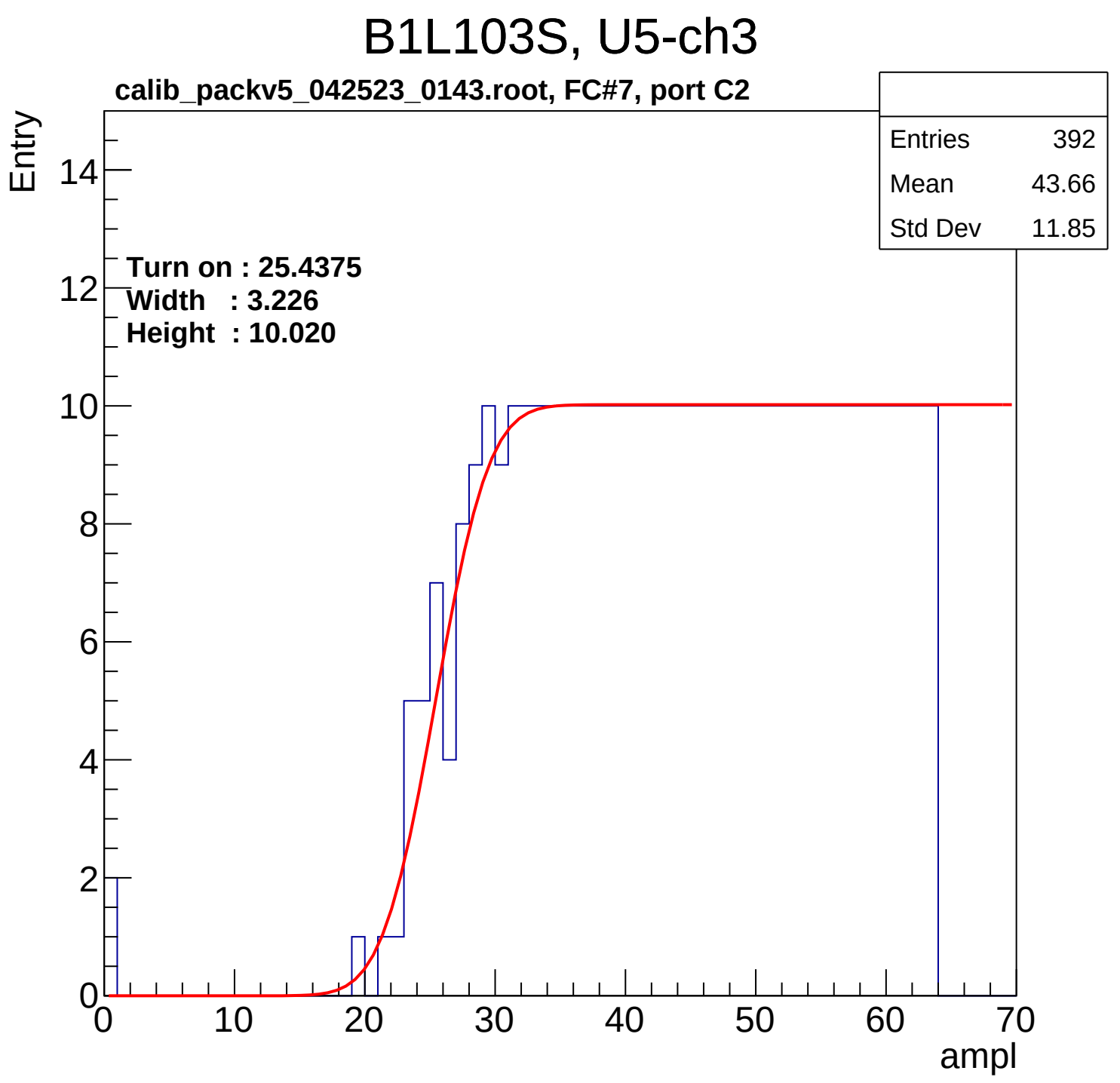
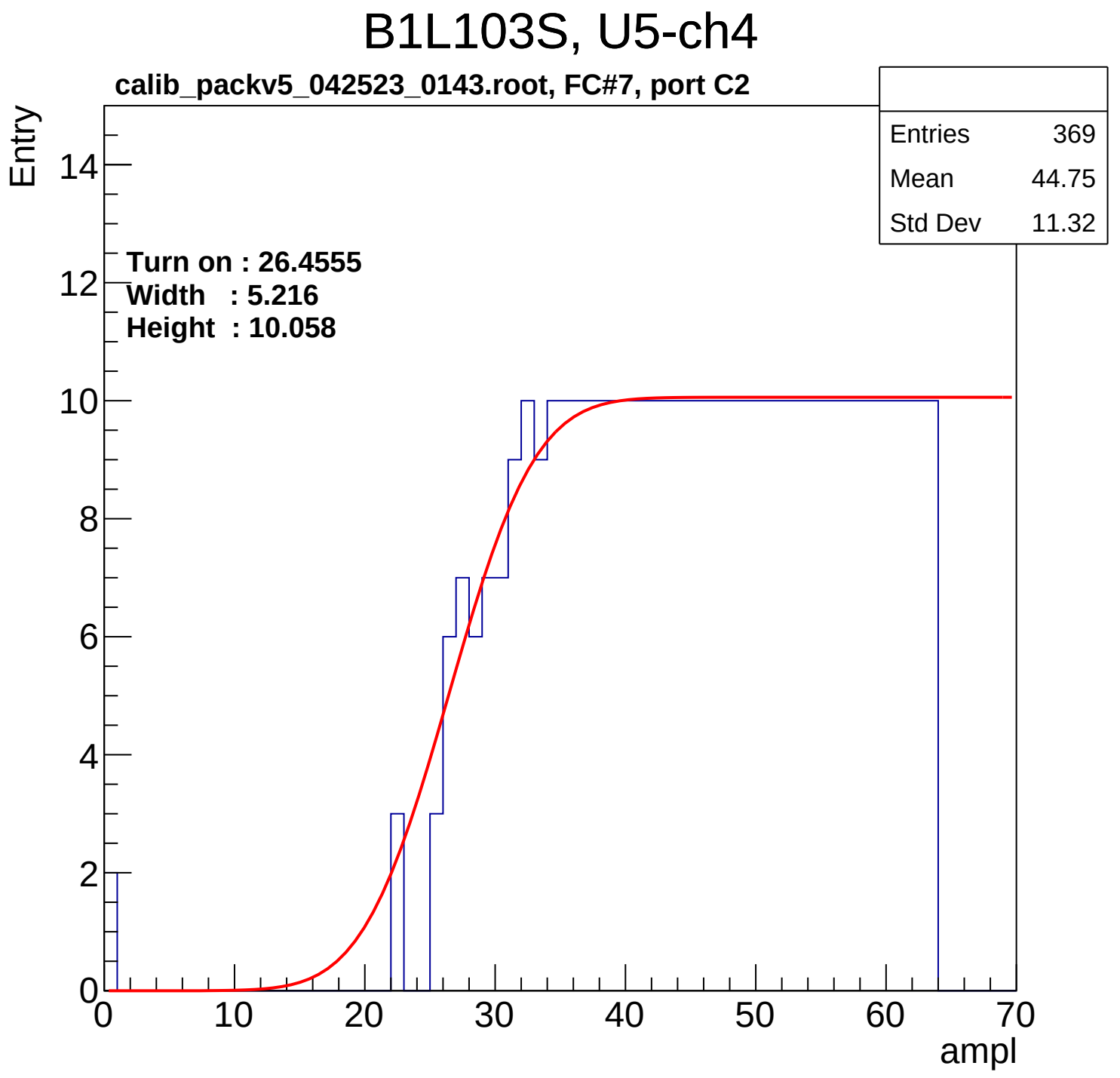
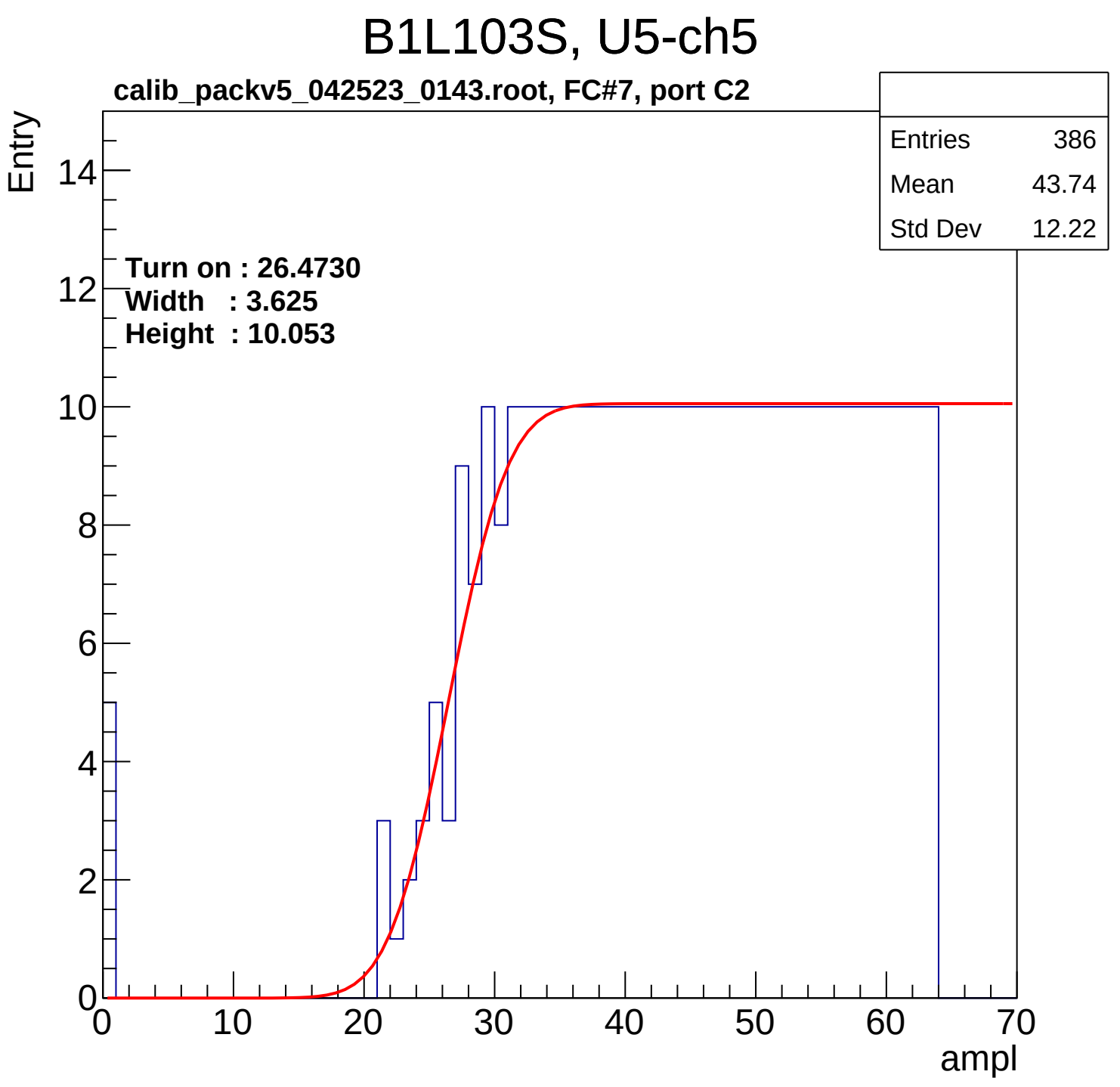

B1L103S, U5-ch0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 389
Mean 43.37
Std Dev 12.8
Turn on : 26.2910
Width : 4.580
Height : 10.093
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

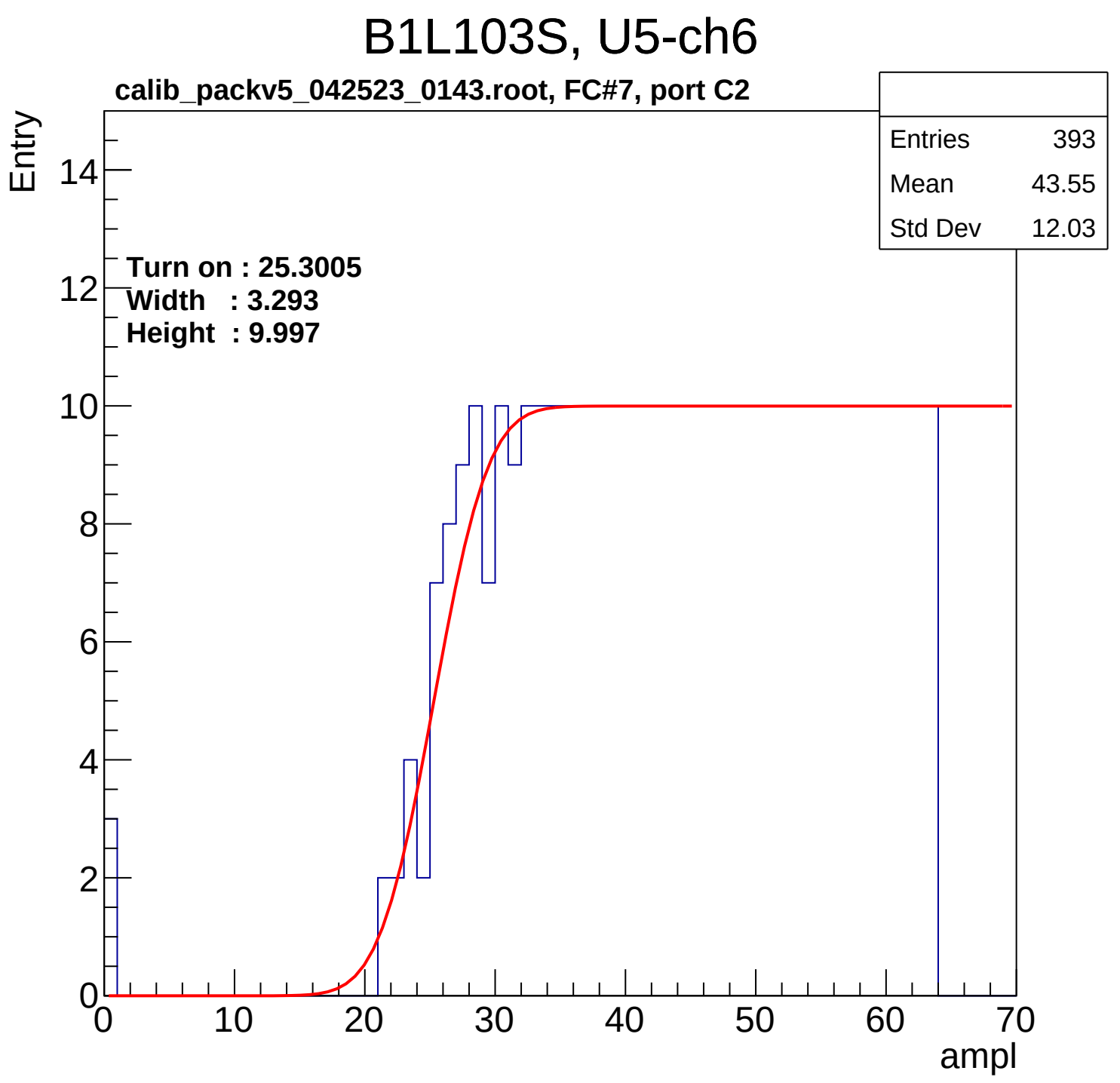

B1L103S, U5-ch1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 350
Mean 45.55
Std Dev 11.25
Turn on : 29.7017
Width : 3.702
Height : 10.065
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

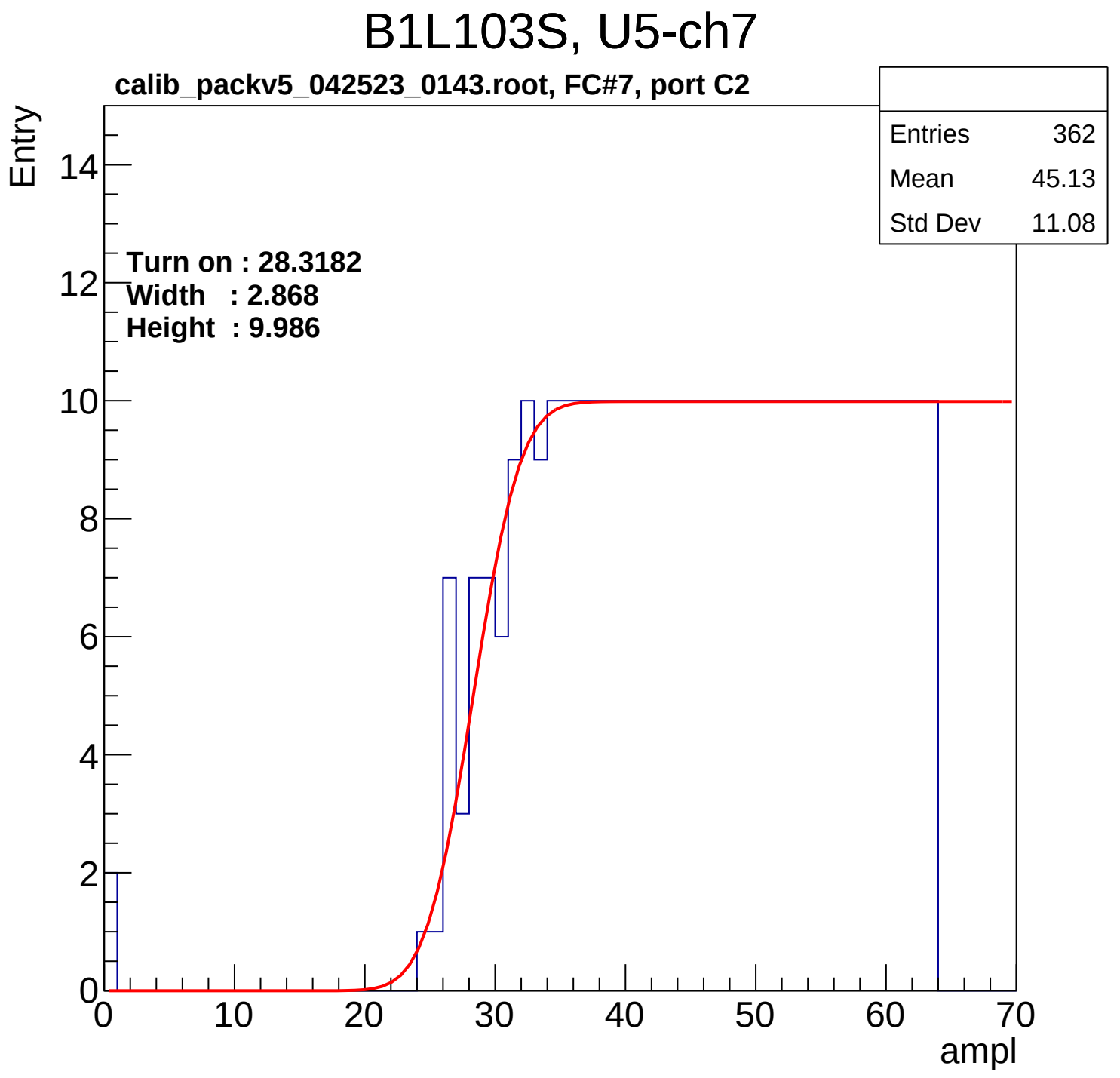

B1L103S, U5-ch2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 376
Mean 44.44
Std Dev 11.43
Turn on : 26.7543
Width : 2.710
Height : 9.961
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

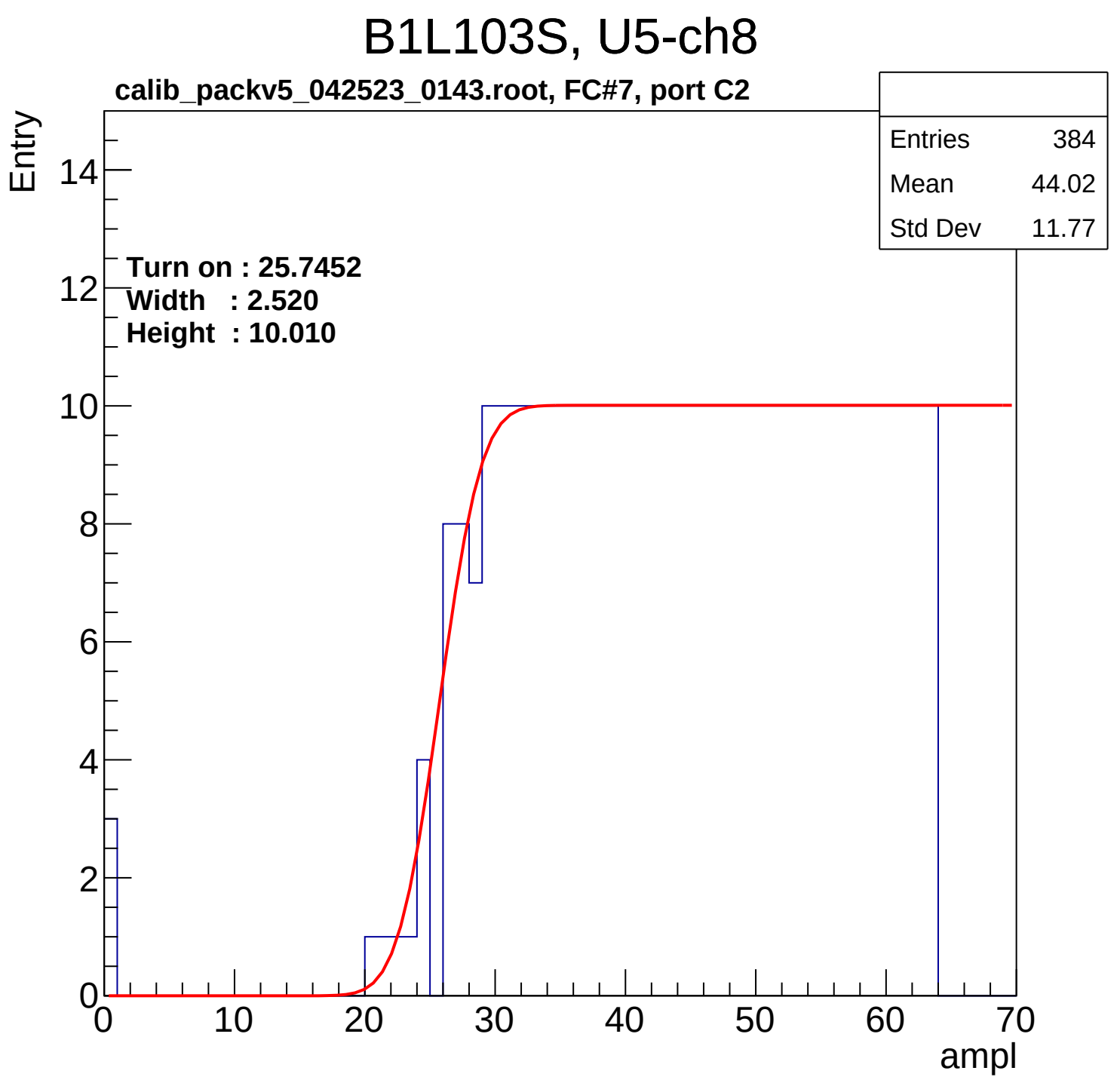

B1L103S, U5-ch3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 392
Mean 43.66
Std Dev 11.85
Turn on : 25.4375
Width : 3.226
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

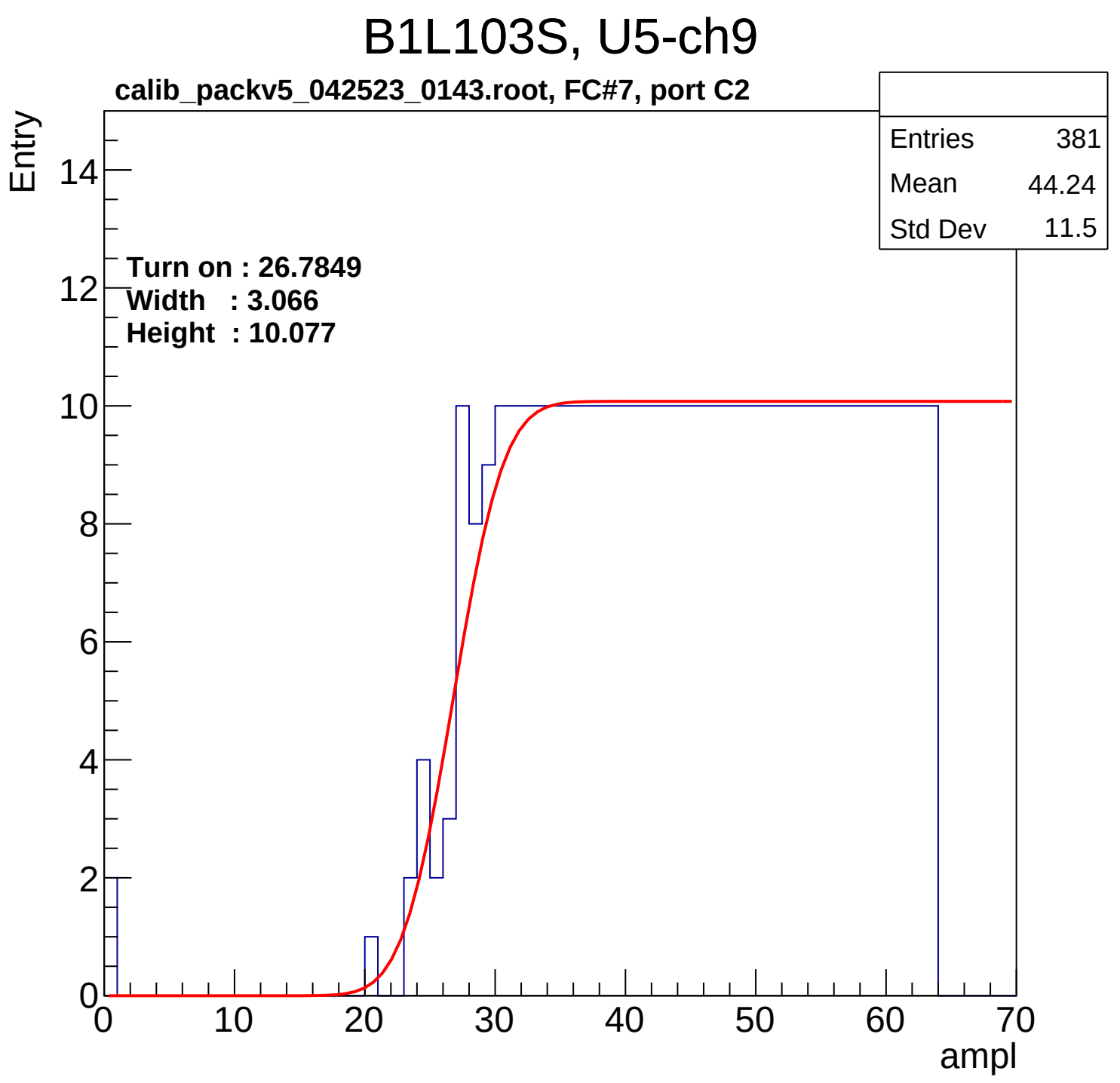

B1L103S, U5-ch4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.75
Std Dev 11.32
Turn on : 26.4555
Width : 5.216
Height : 10.058
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

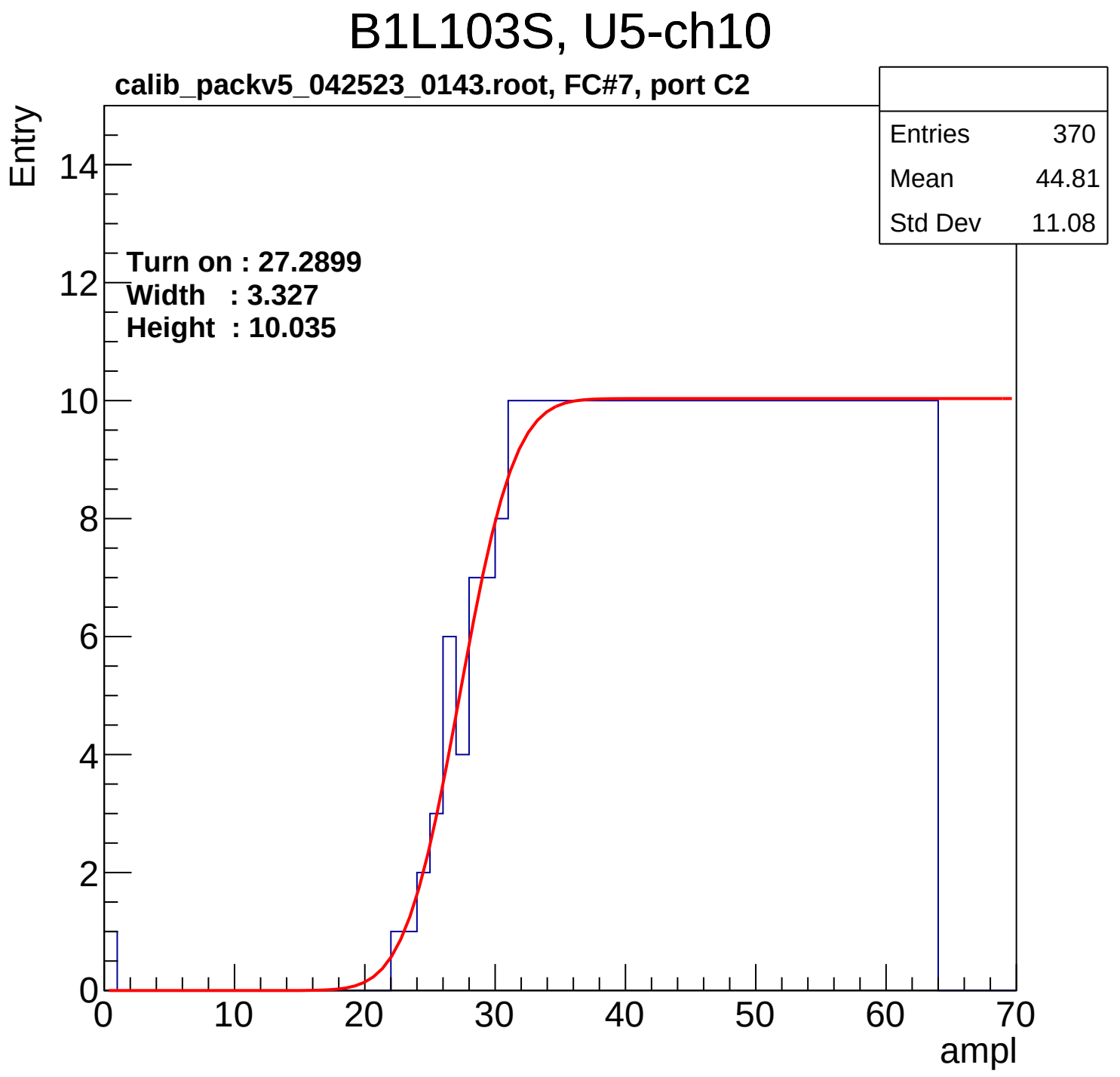

B1L103S, U5-ch5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 386
Mean 43.74
Std Dev 12.22
Turn on : 26.4730
Width : 3.625
Height : 10.053
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

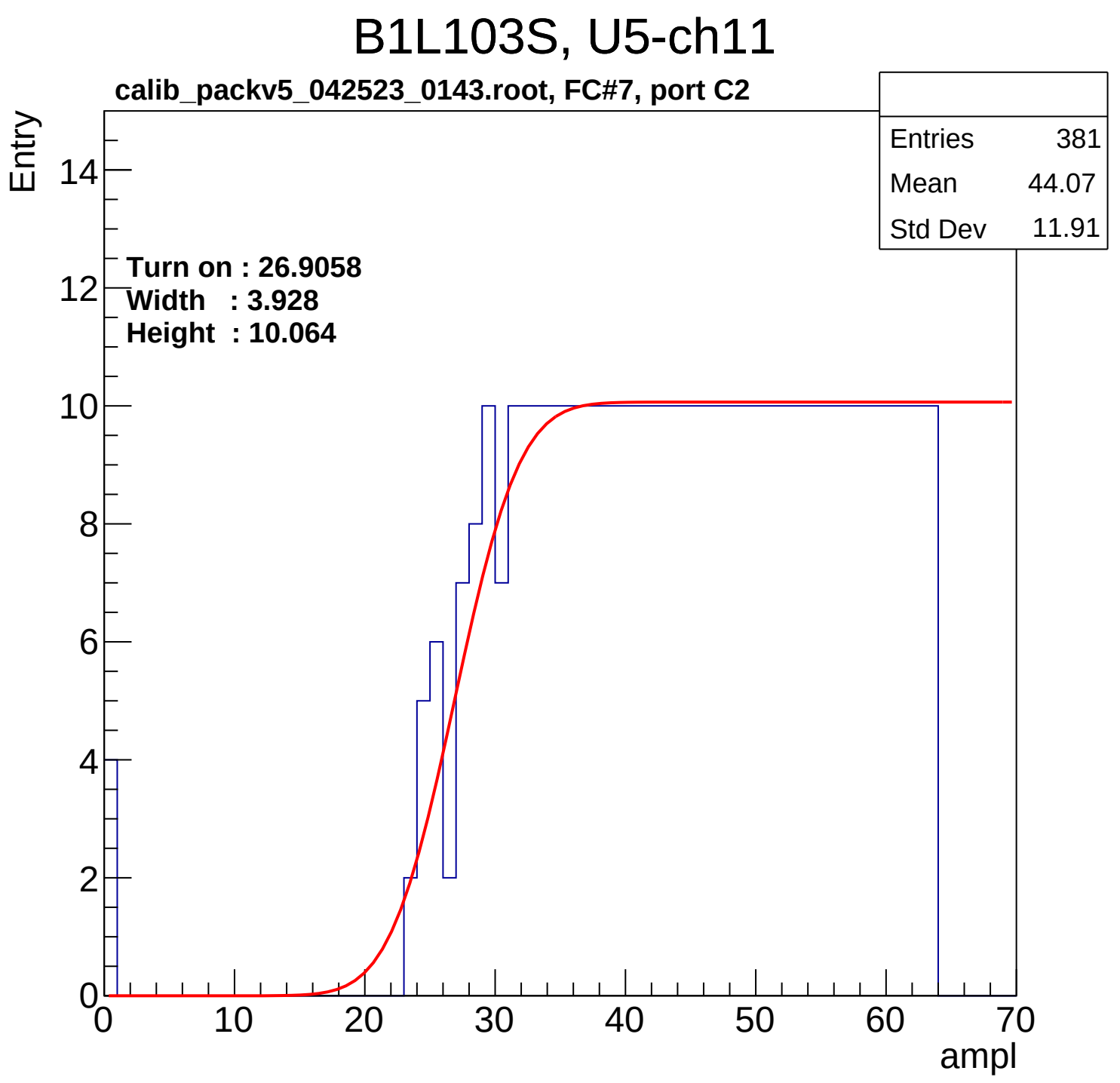

B1L103S, U5-ch6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 393
Mean 43.55
Std Dev 12.03
Turn on : 25.3005
Width : 3.293
Height : 9.997
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

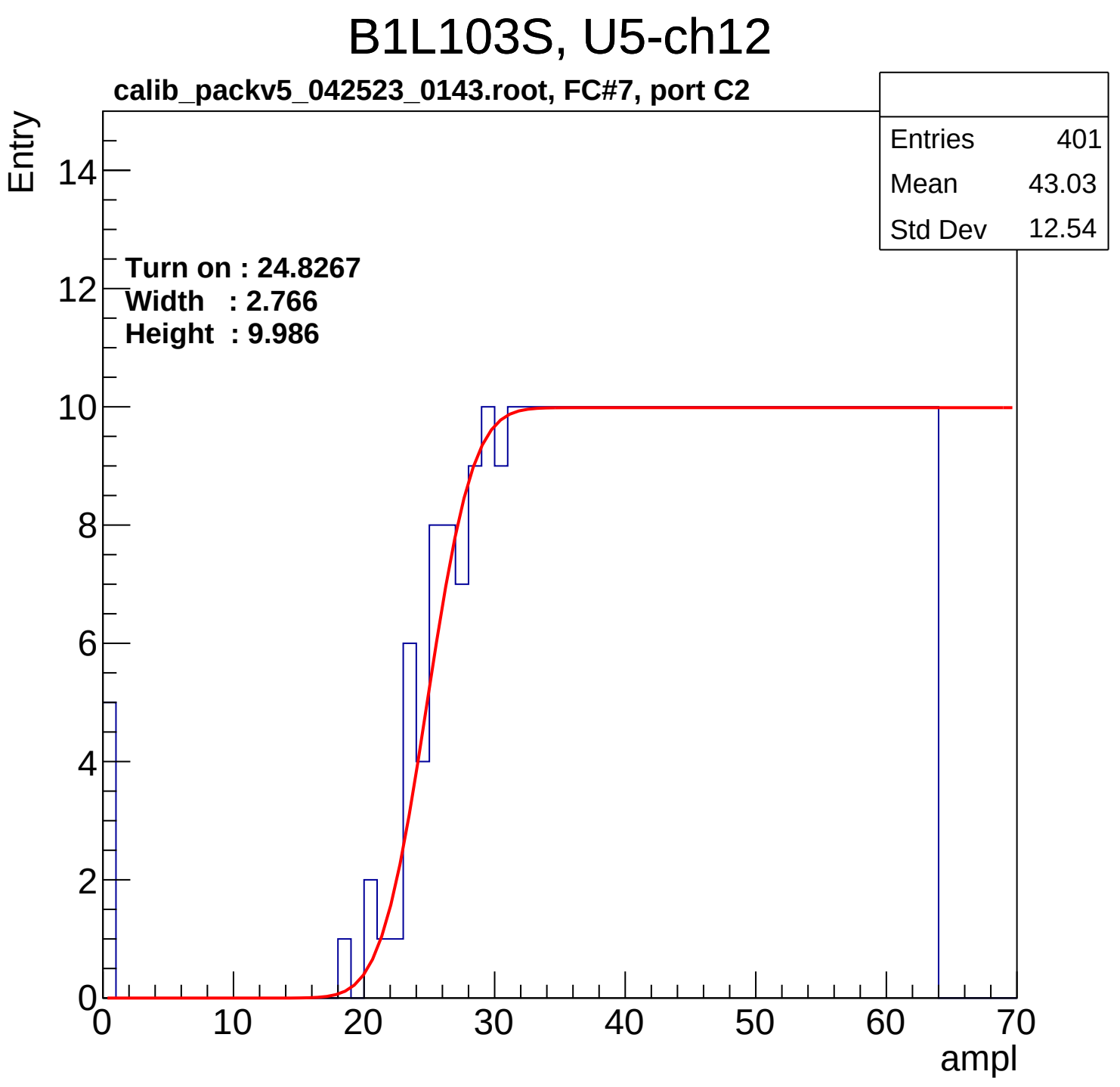

B1L103S, U5-ch7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 362
Mean 45.13
Std Dev 11.08
Turn on : 28.3182
Width : 2.868
Height : 9.986
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

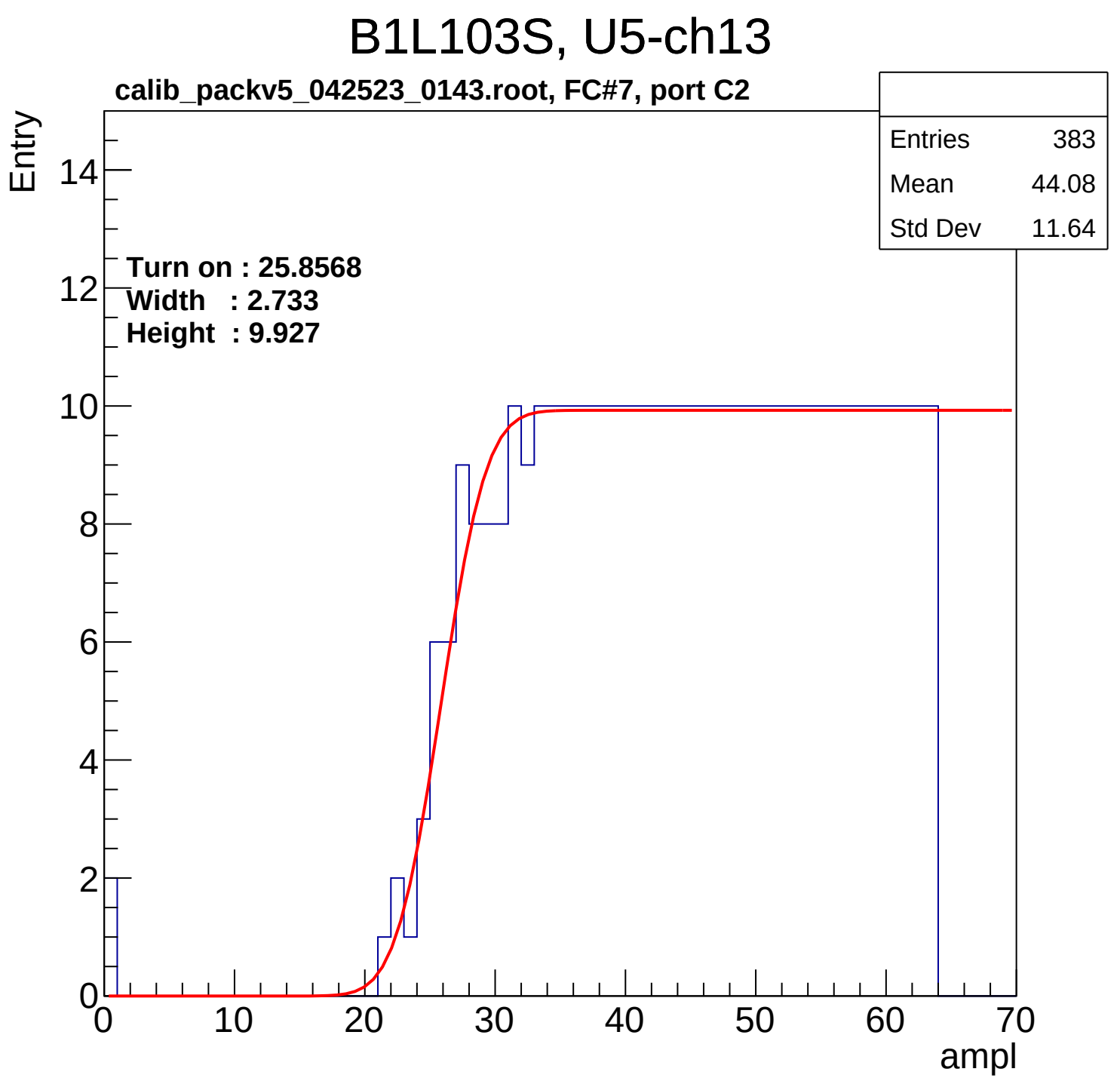

B1L103S, U5-ch8
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 44.02
Std Dev 11.77
Turn on : 25.7452
Width : 2.520
Height : 10.010
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

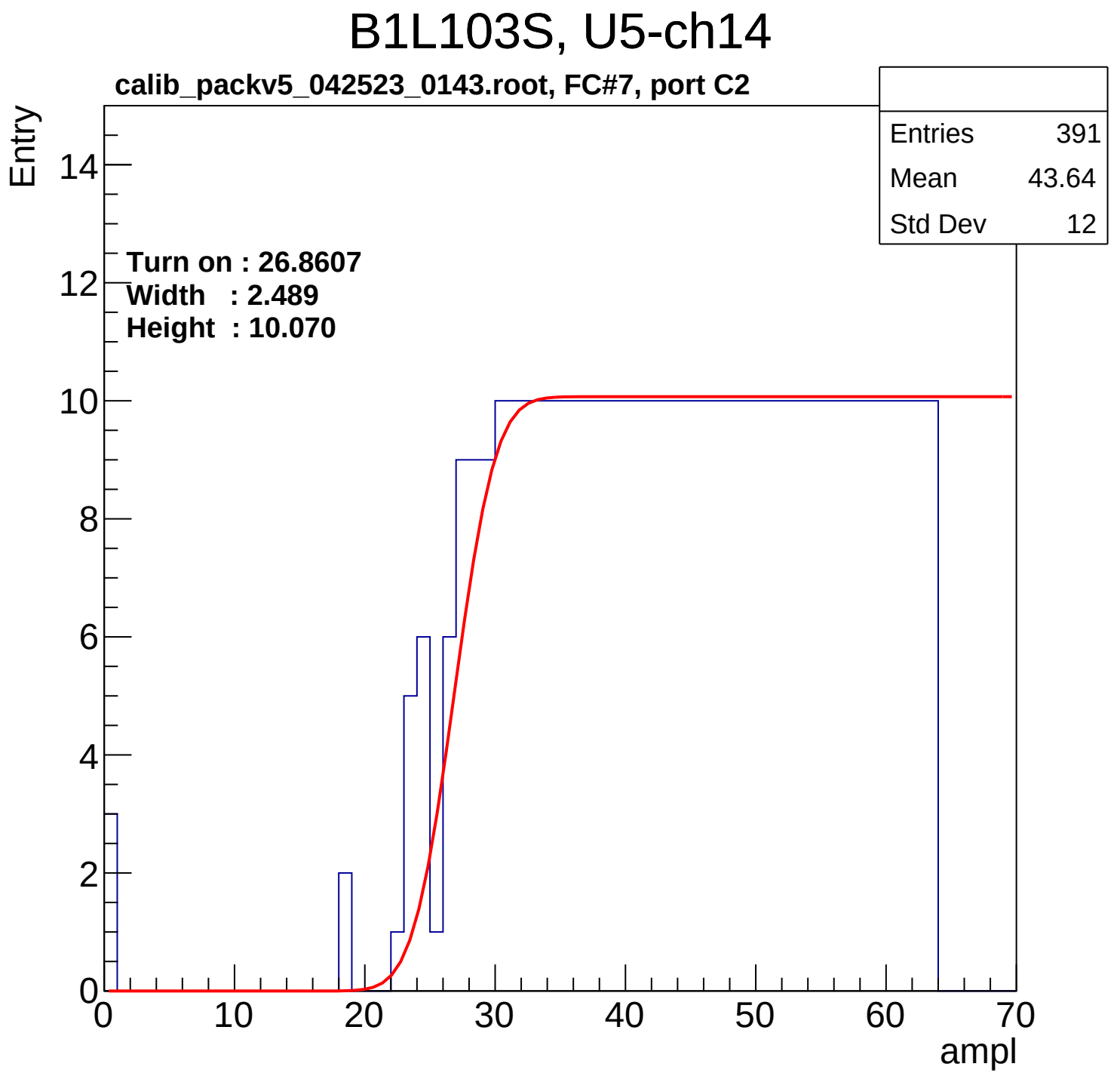

B1L103S, U5-ch9
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.24
Std Dev 11.5
Turn on : 26.7849
Width : 3.066
Height : 10.077
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

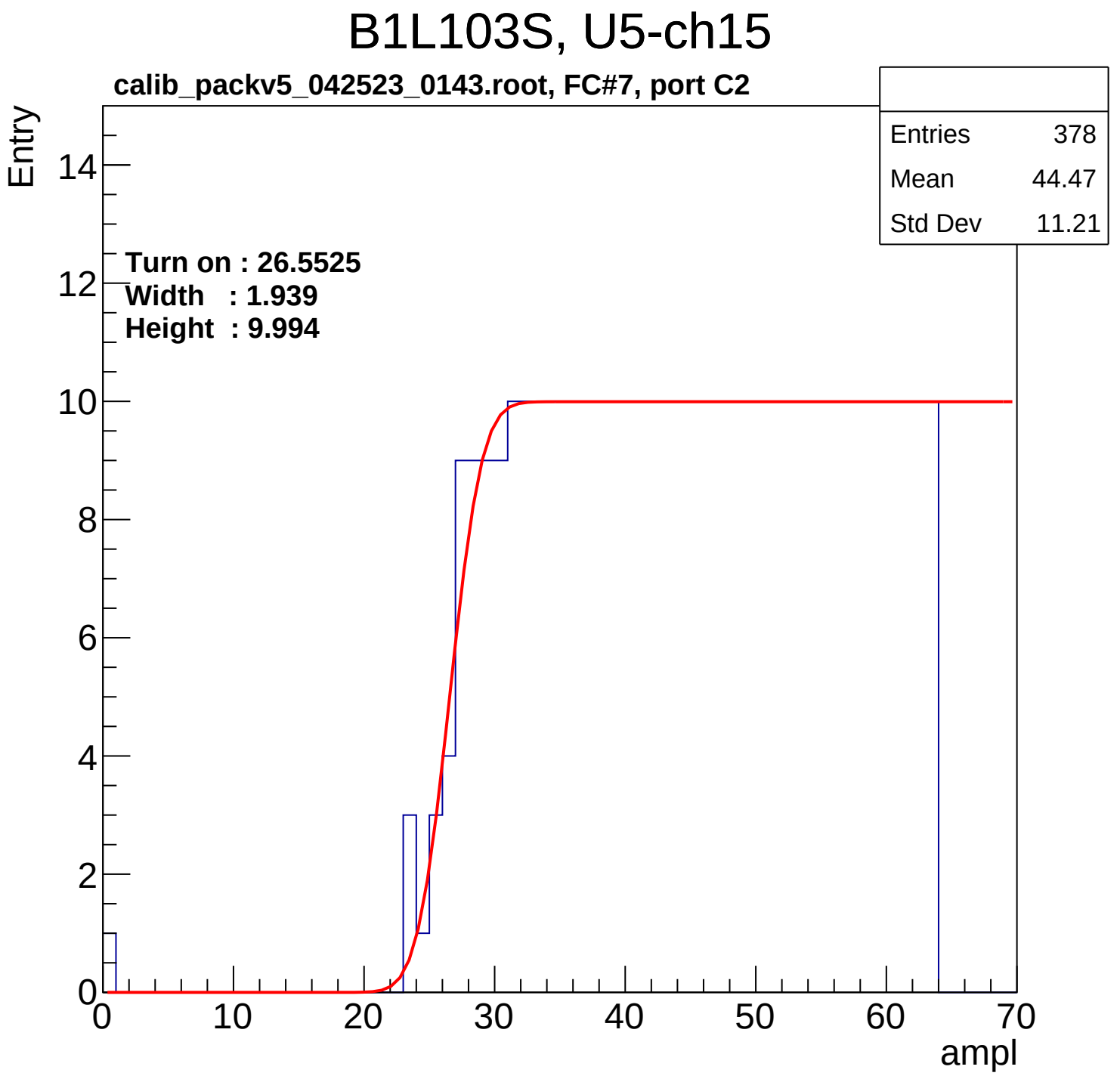

B1L103S, U5-ch10
calib_packv5_042523_0143.root, FC#7, port C2
Entries 370
Mean 44.81
Std Dev 11.08
Turn on : 27.2899
Width : 3.327
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

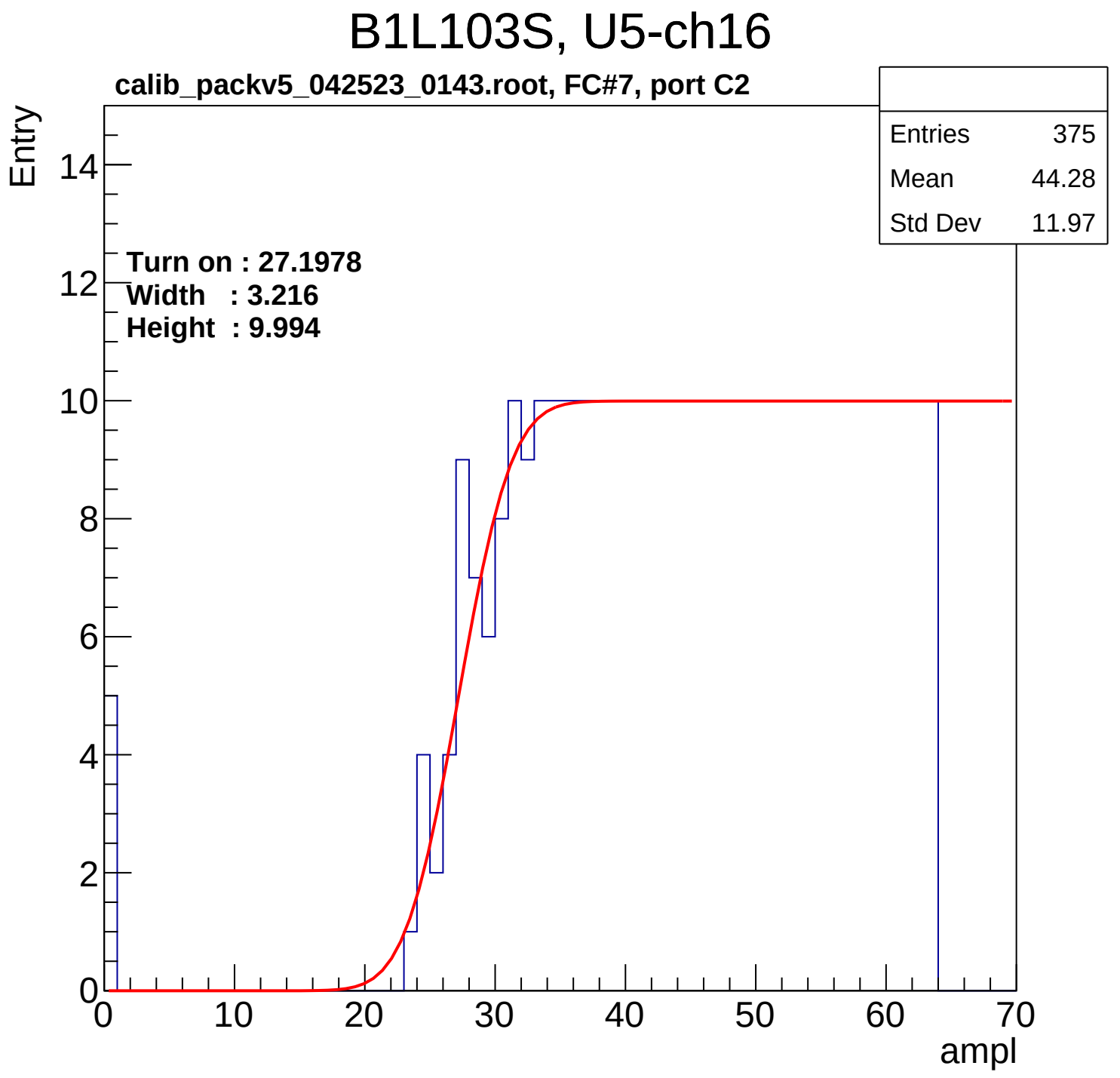

B1L103S, U5-ch11
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.07
Std Dev 11.91
Turn on : 26.9058
Width : 3.928
Height : 10.064
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

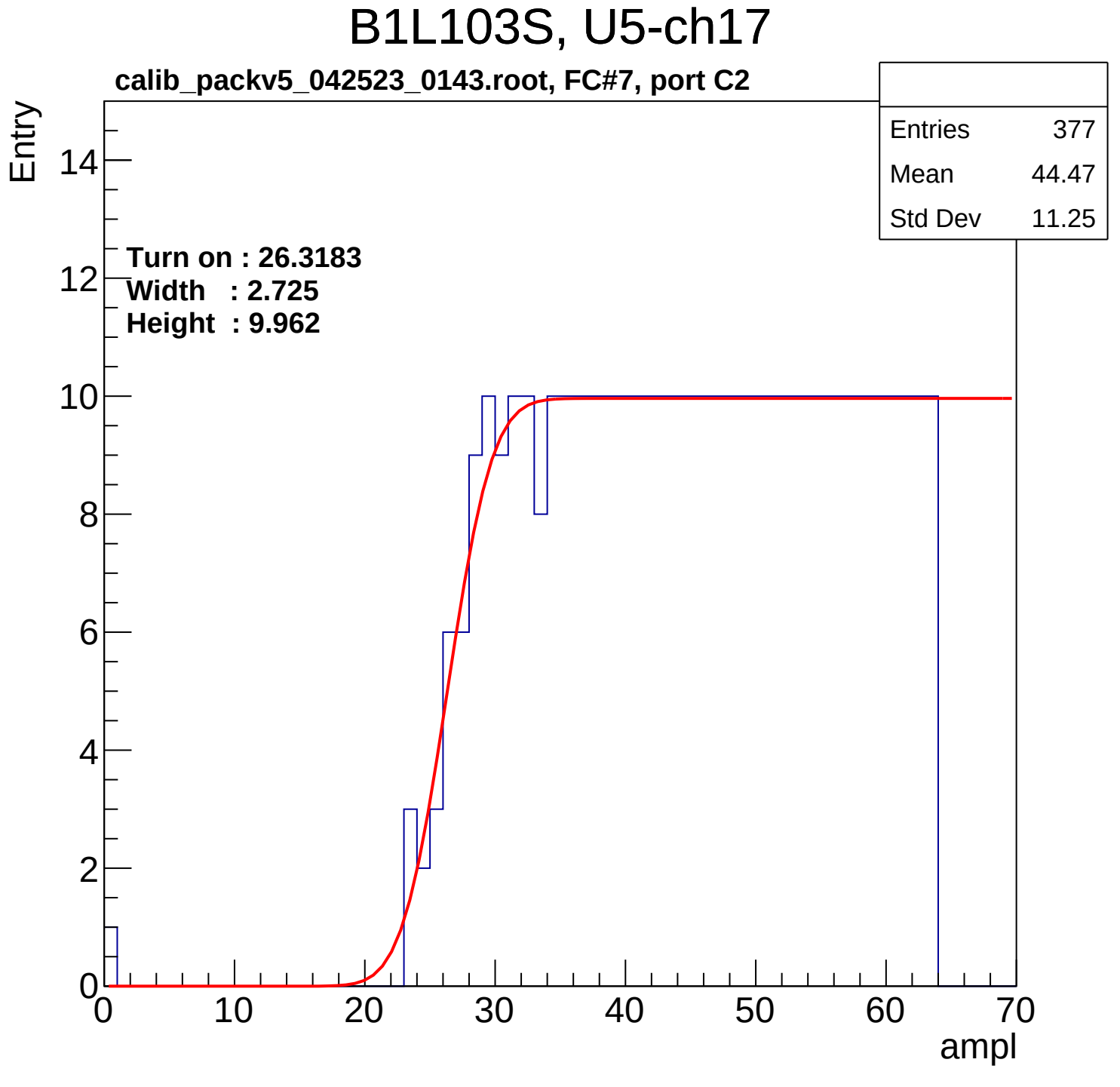

B1L103S, U5-ch12
calib_packv5_042523_0143.root, FC#7, port C2
Entries 401
Mean 43.03
Std Dev 12.54
Turn on : 24.8267
Width : 2.766
Height : 9.986
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

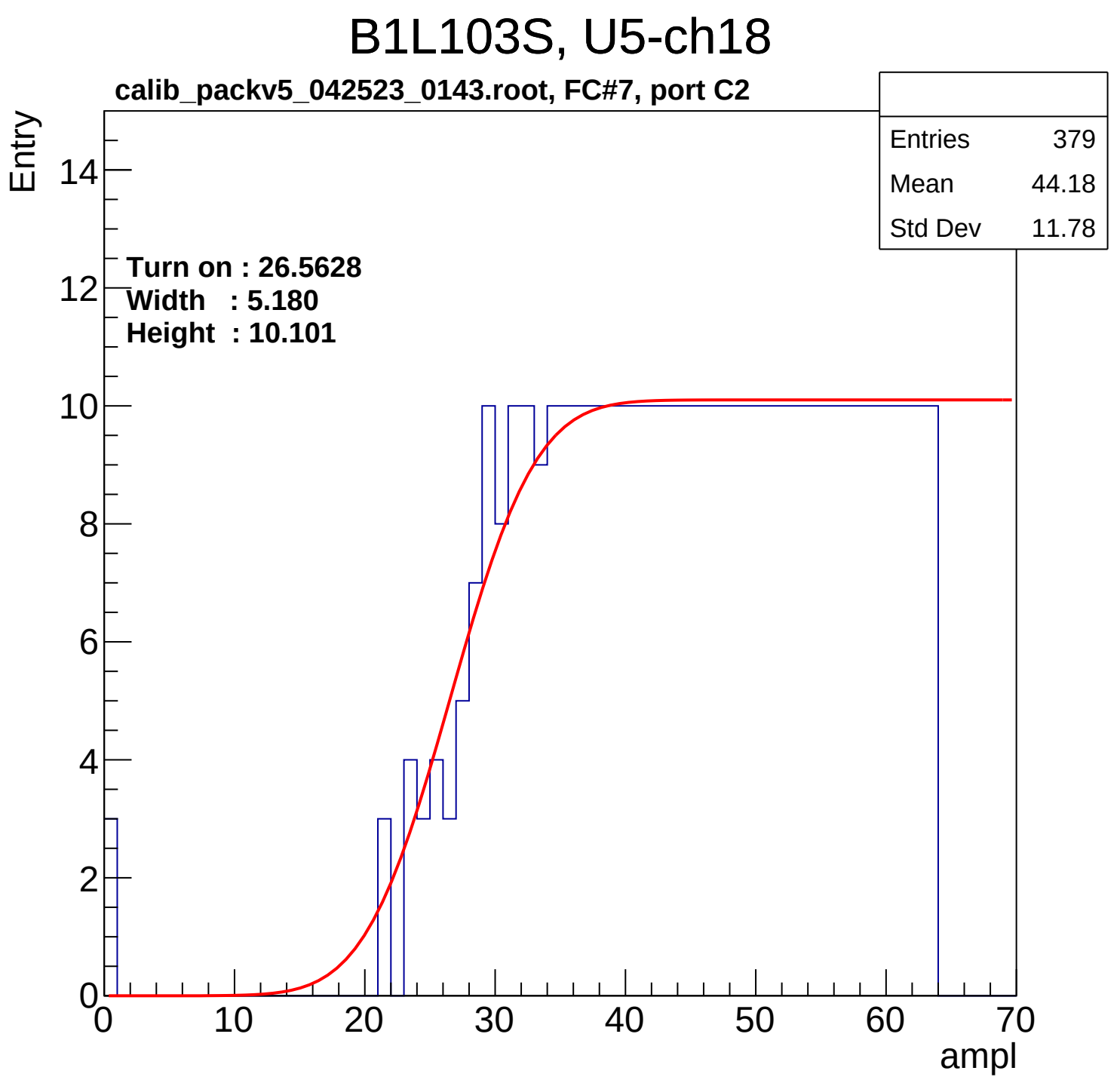

B1L103S, U5-ch13
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 44.08
Std Dev 11.64
Turn on : 25.8568
Width : 2.733
Height : 9.927
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

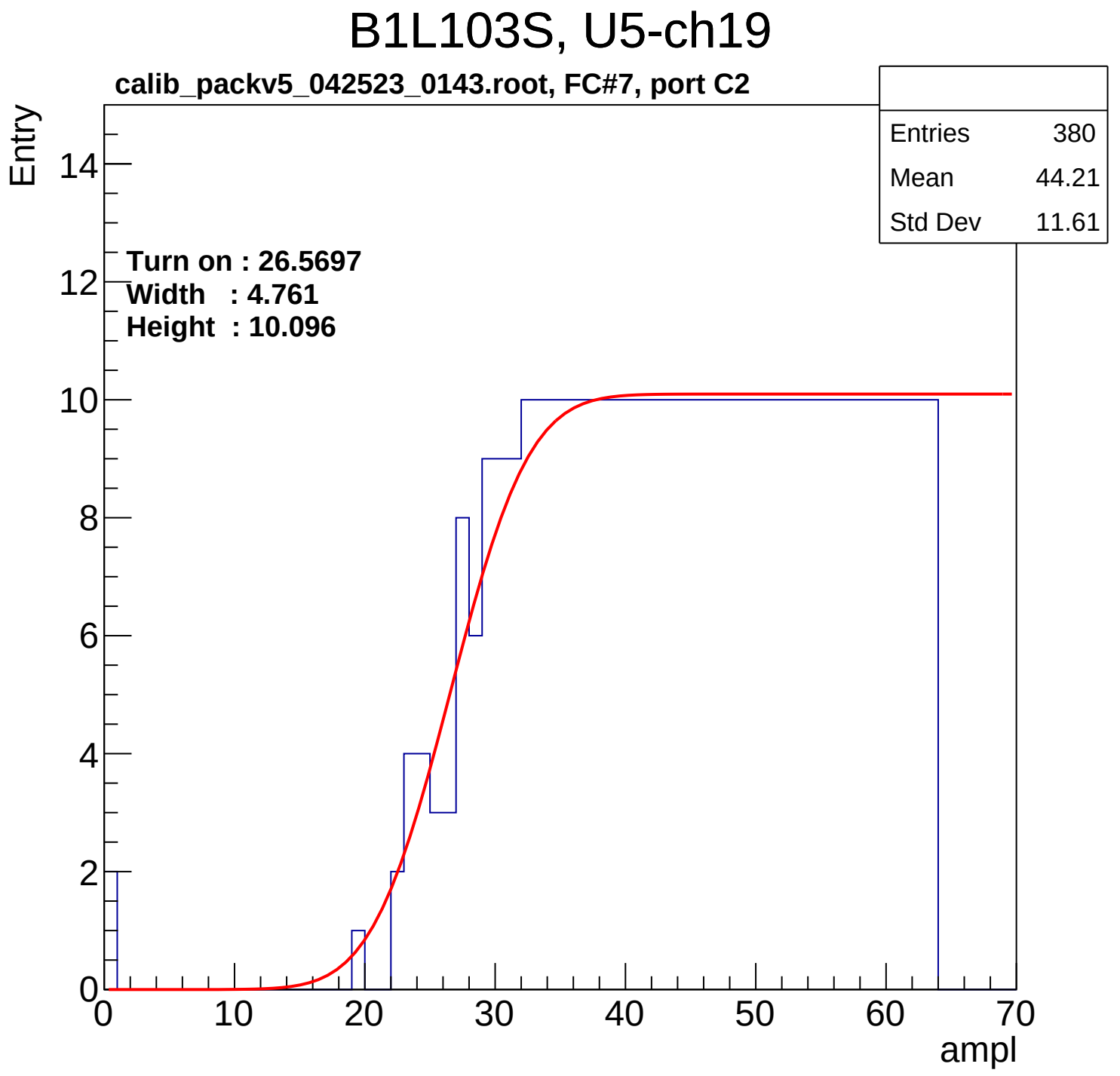

B1L103S, U5-ch14
calib_packv5_042523_0143.root, FC#7, port C2
Entries 391
Mean 43.64
Std Dev 12
Turn on : 26.8607
Width : 2.489
Height : 10.070
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

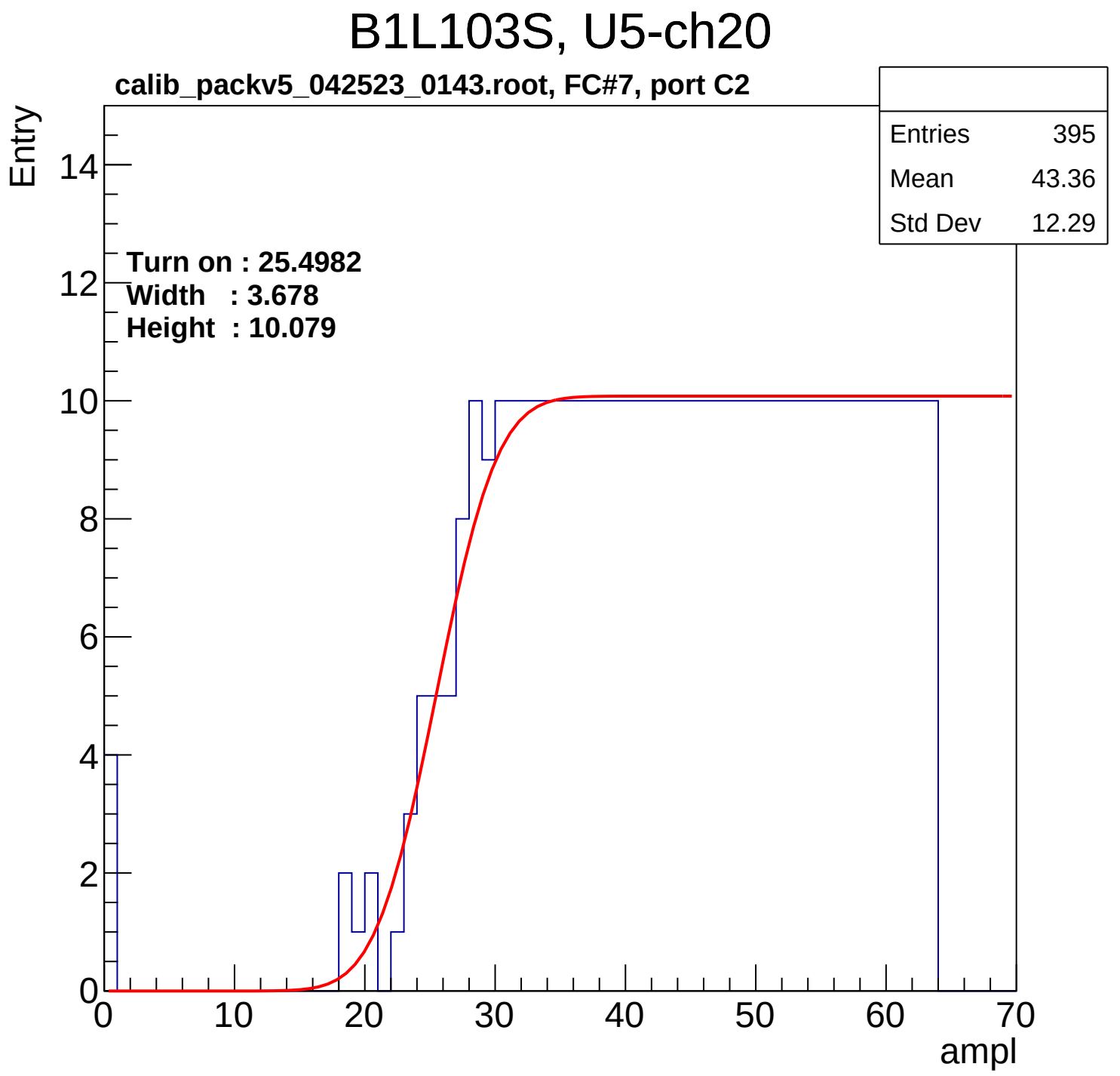

B1L103S, U5-ch15
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.47
Std Dev 11.21
Turn on : 26.5525
Width : 1.939
Height : 9.994
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

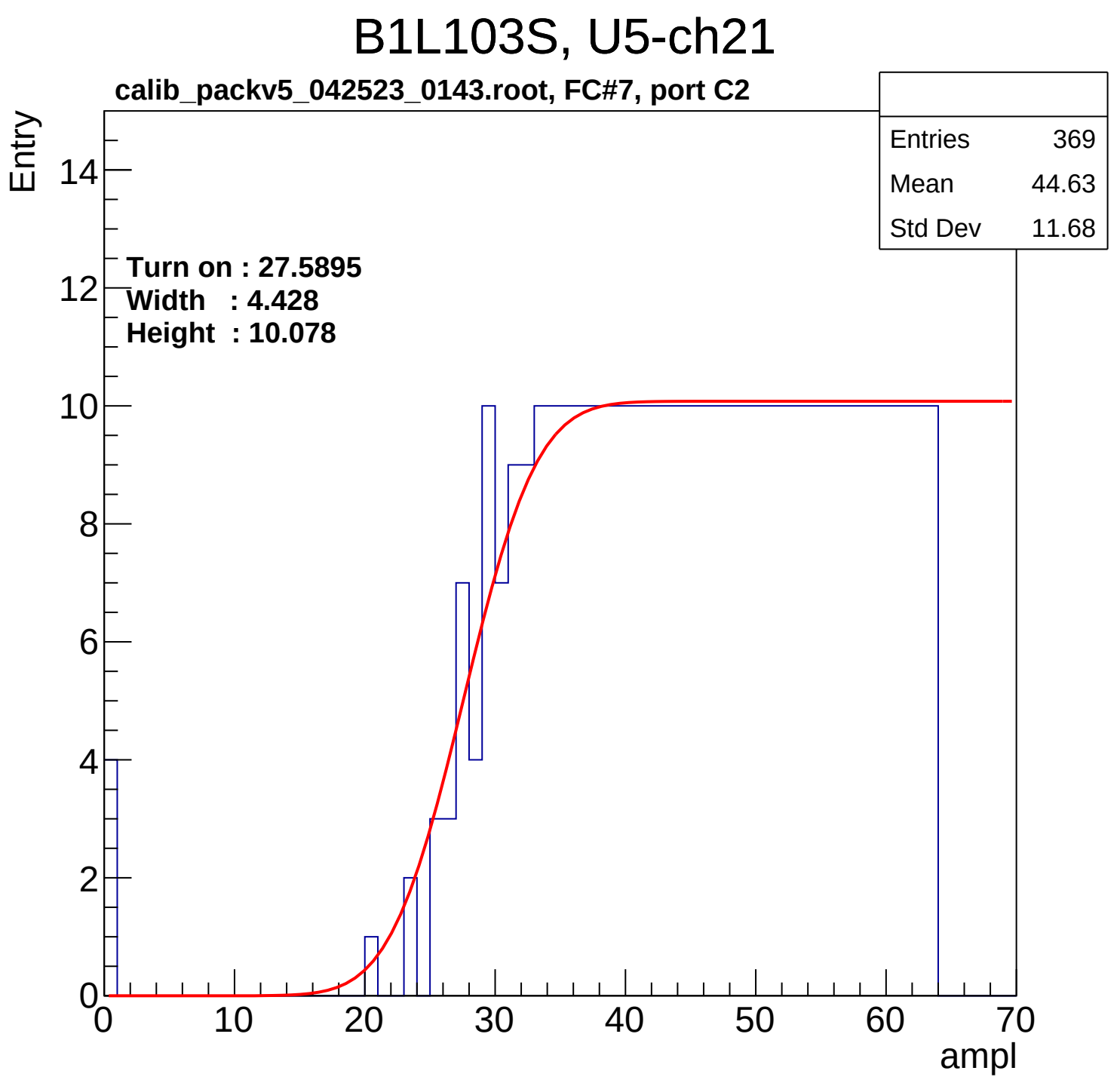

B1L103S, U5-ch16
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.28
Std Dev 11.97
Turn on : 27.1978
Width : 3.216
Height : 9.994
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

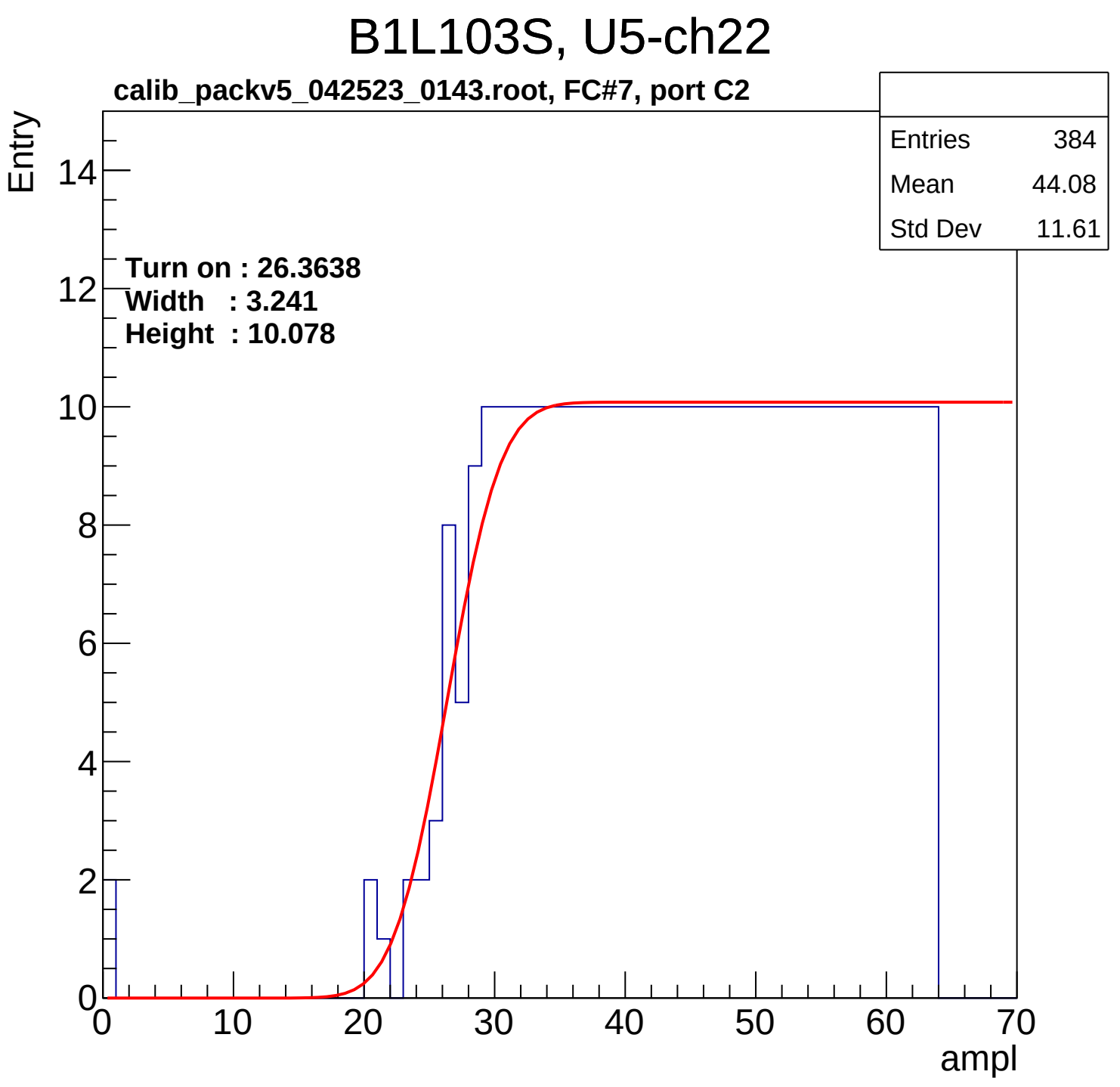

B1L103S, U5-ch17
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.47
Std Dev 11.25
Turn on : 26.3183
Width : 2.725
Height : 9.962
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

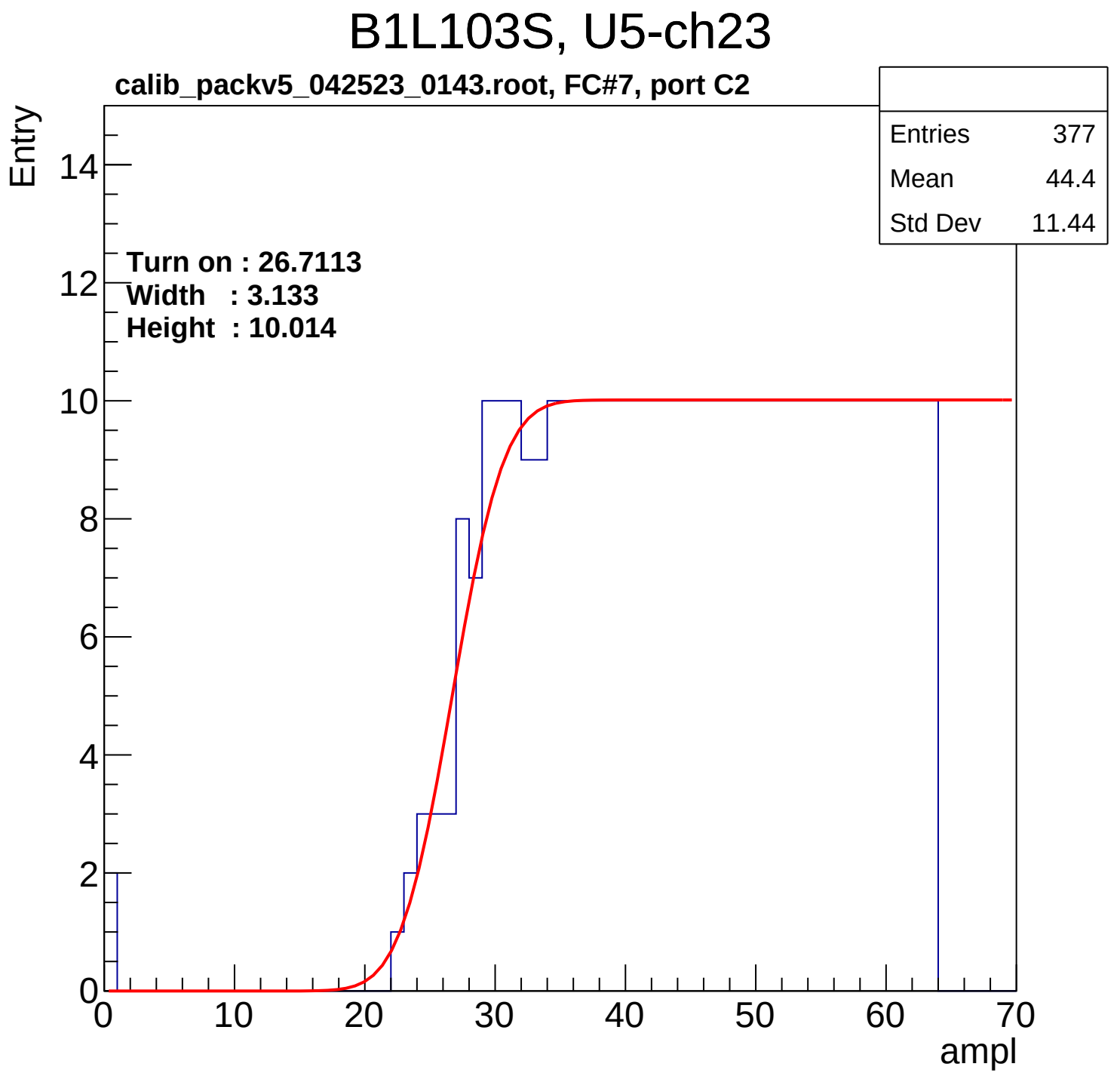

B1L103S, U5-ch18
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.18
Std Dev 11.78
Turn on : 26.5628
Width : 5.180
Height : 10.101
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

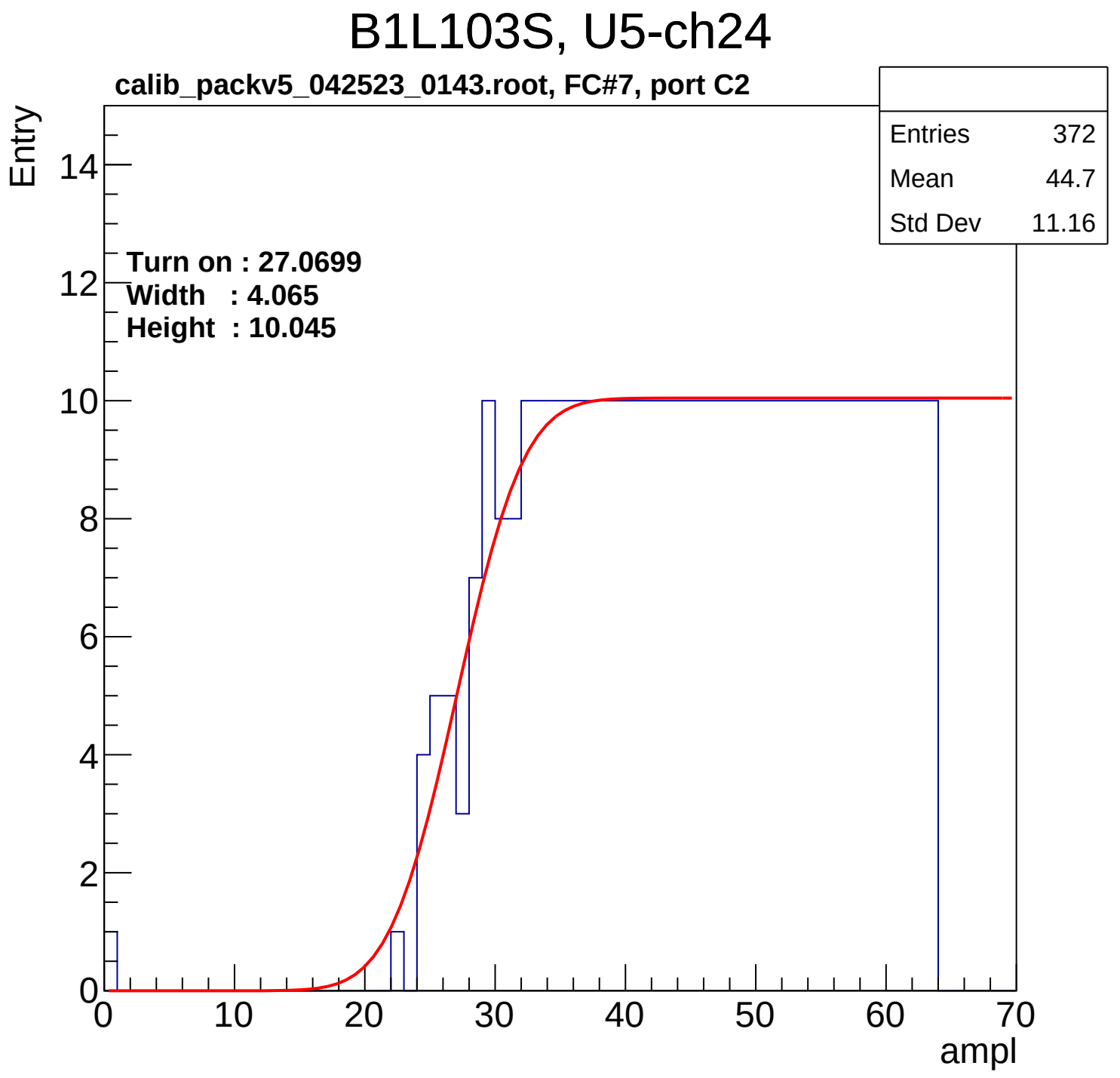

B1L103S, U5-ch19
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.21
Std Dev 11.61
Turn on : 26.5697
Width : 4.761
Height : 10.096
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

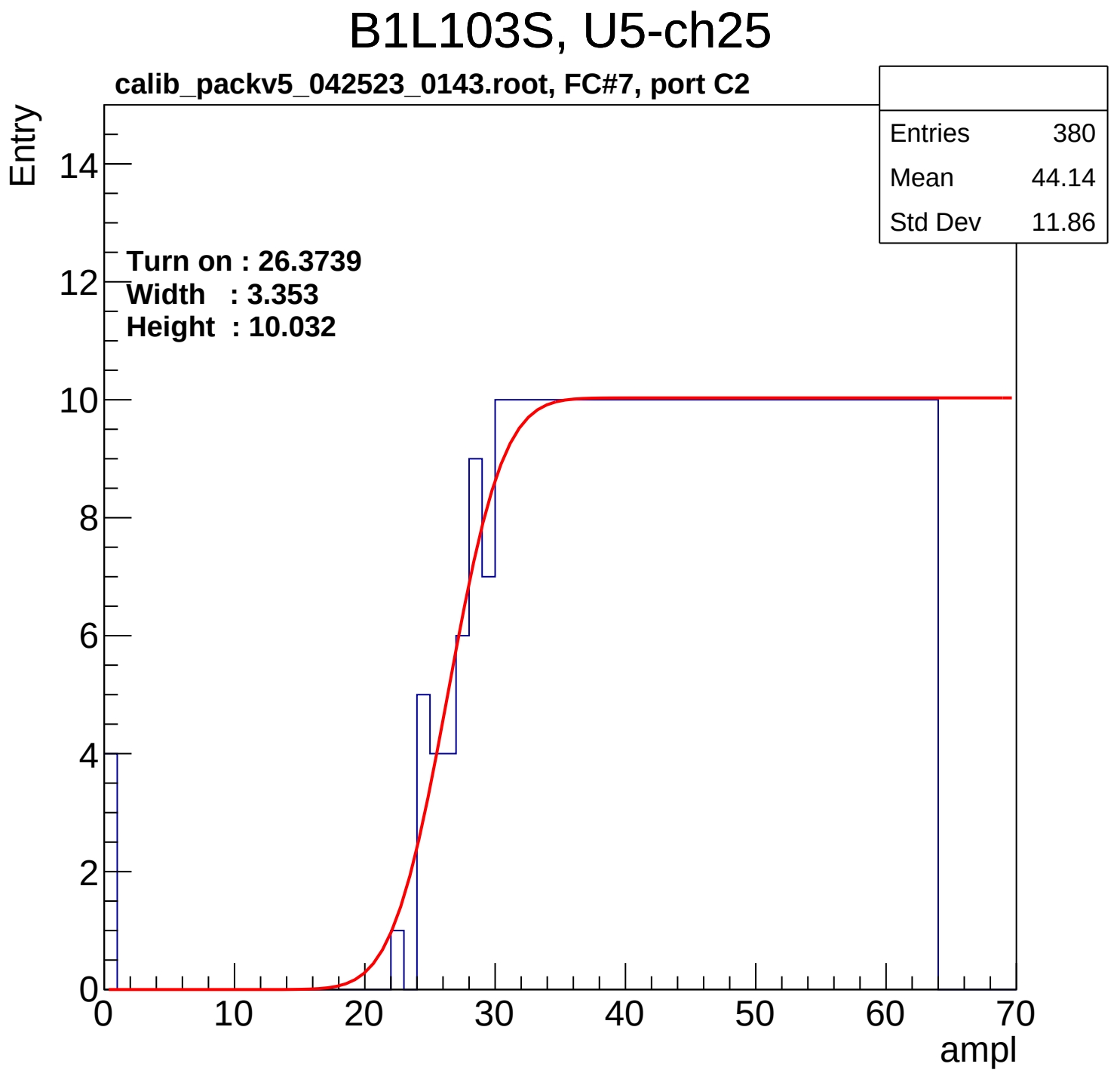

B1L103S, U5-ch20
calib_packv5_042523_0143.root, FC#7, port C2
Entries 395
Mean 43.36
Std Dev 12.29
Turn on : 25.4982
Width : 3.678
Height : 10.079
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

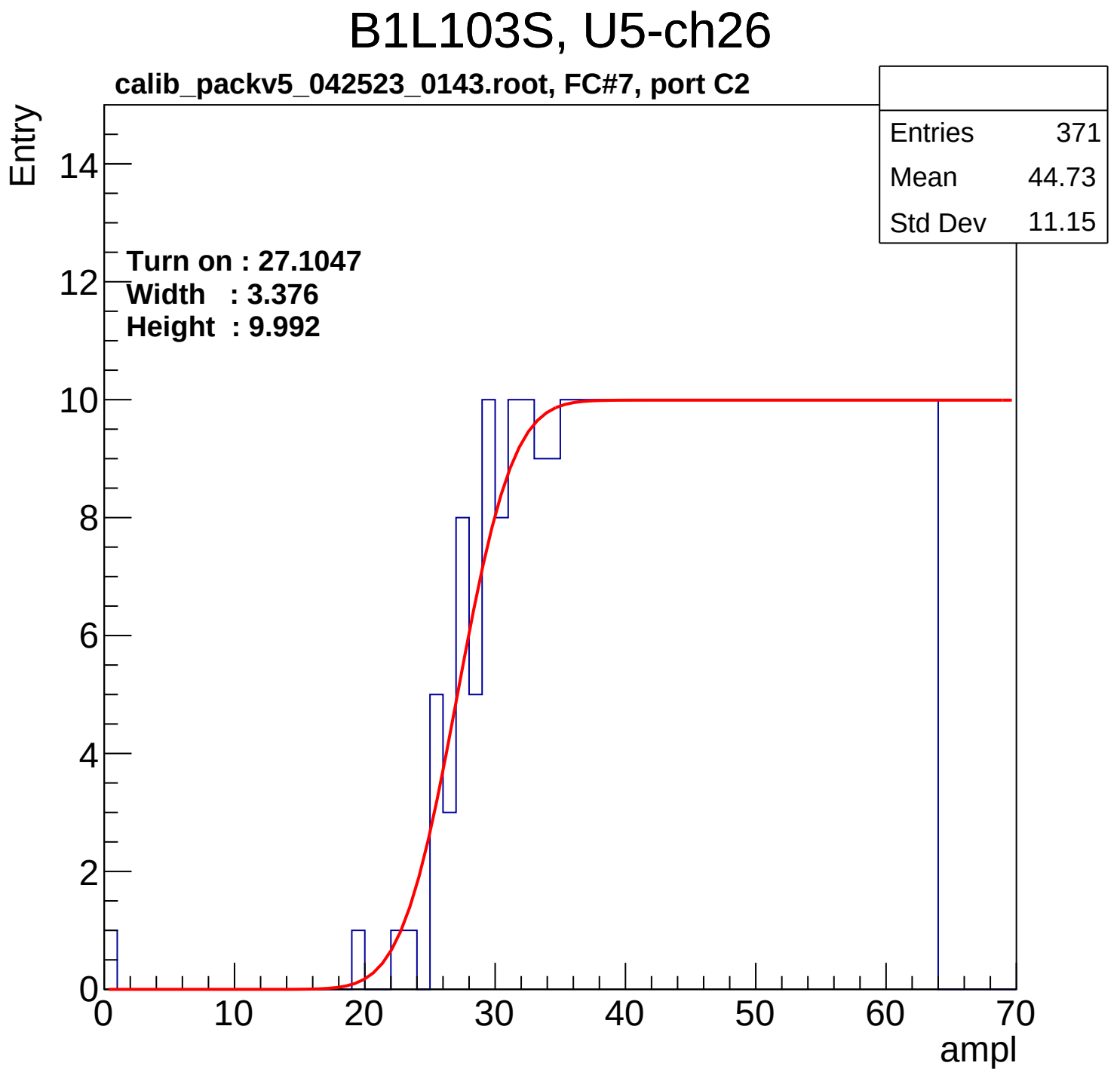

B1L103S, U5-ch21
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.63
Std Dev 11.68
Turn on : 27.5895
Width : 4.428
Height : 10.078
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

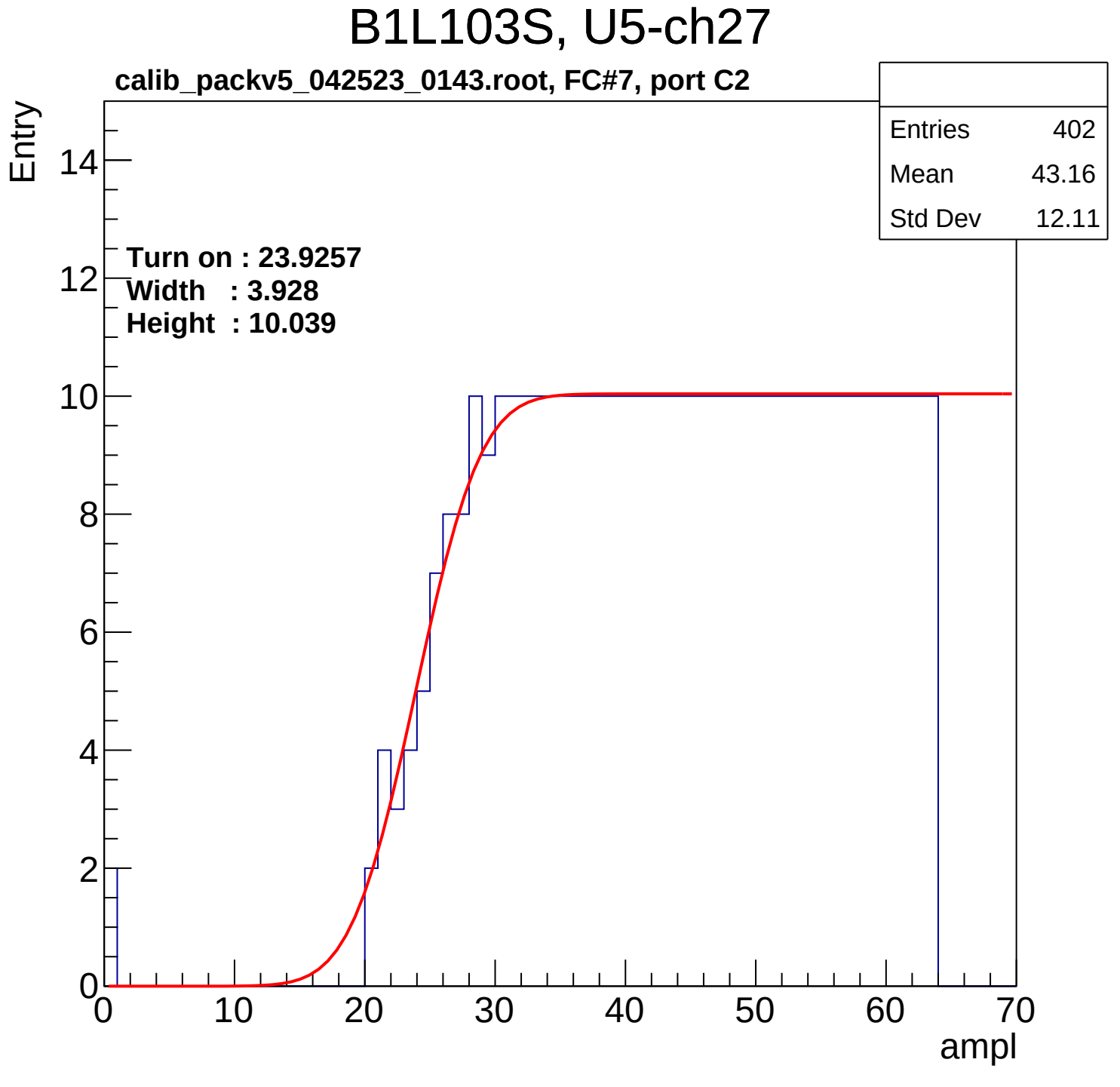

B1L103S, U5-ch22
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 44.08
Std Dev 11.61
Turn on : 26.3638
Width : 3.241
Height : 10.078
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

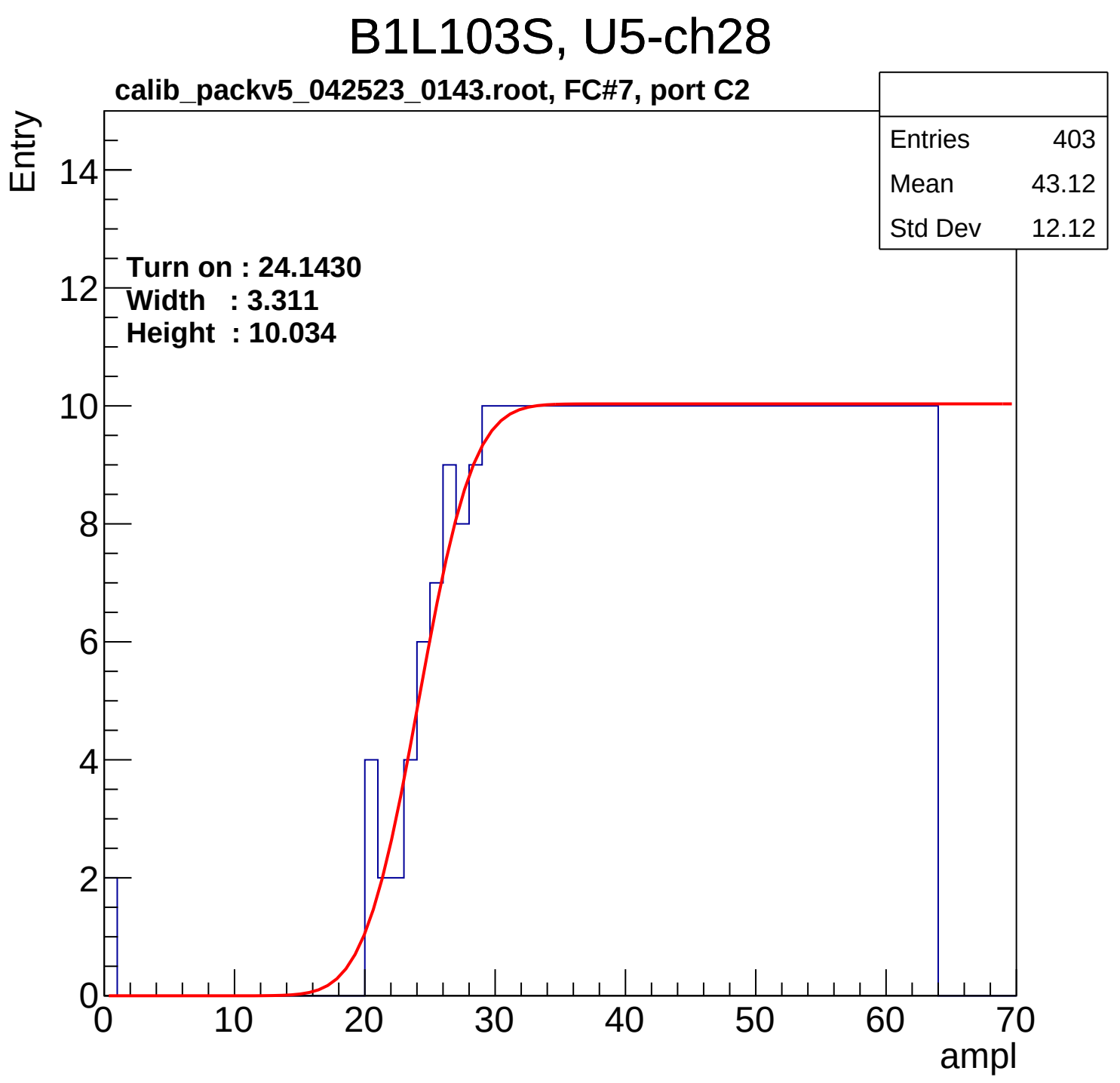

B1L103S, U5-ch23
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.4
Std Dev 11.44
Turn on : 26.7113
Width : 3.133
Height : 10.014
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

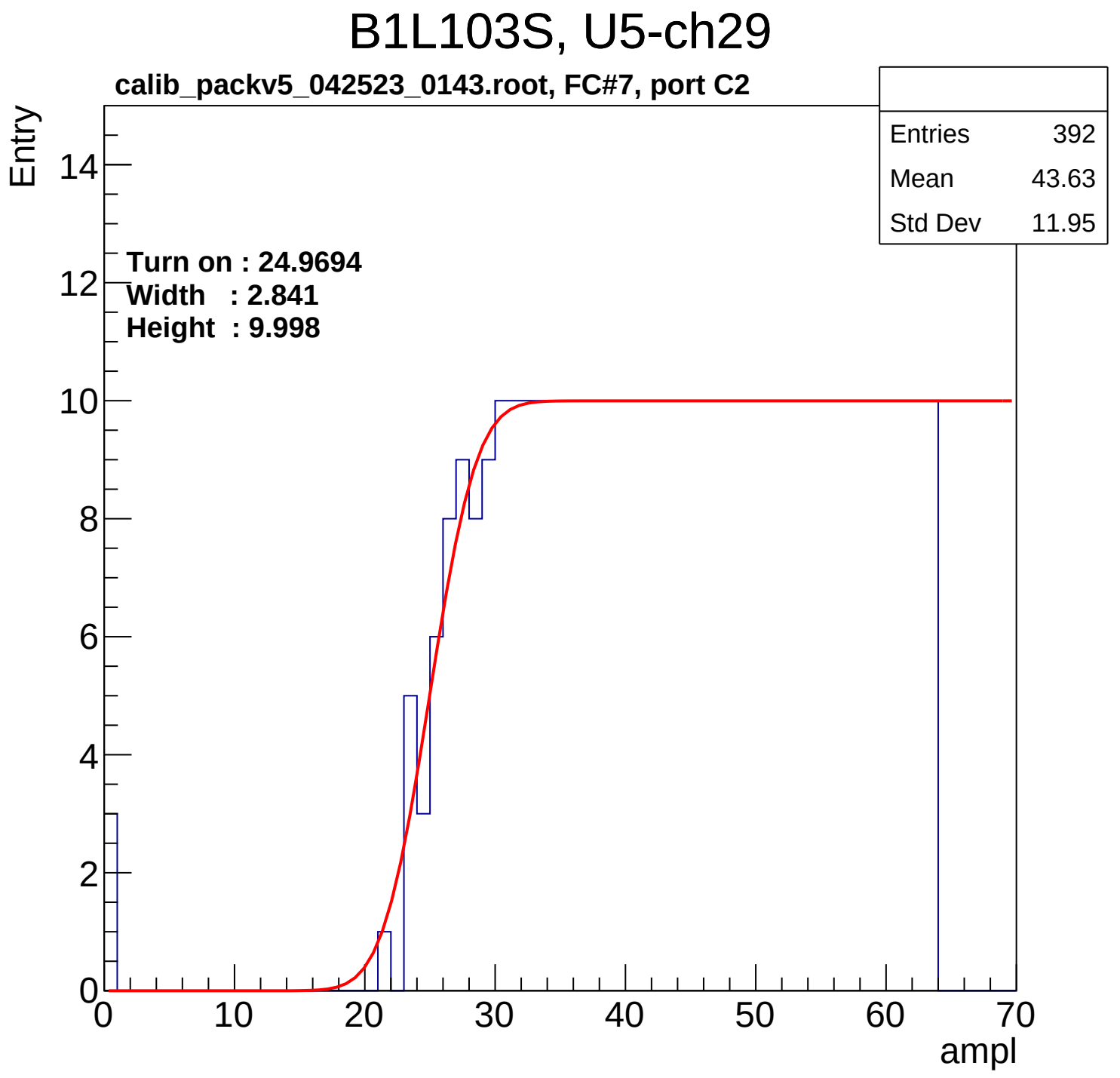

B1L103S, U5-ch24
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.7
Std Dev 11.16
Turn on : 27.0699
Width : 4.065
Height : 10.045
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

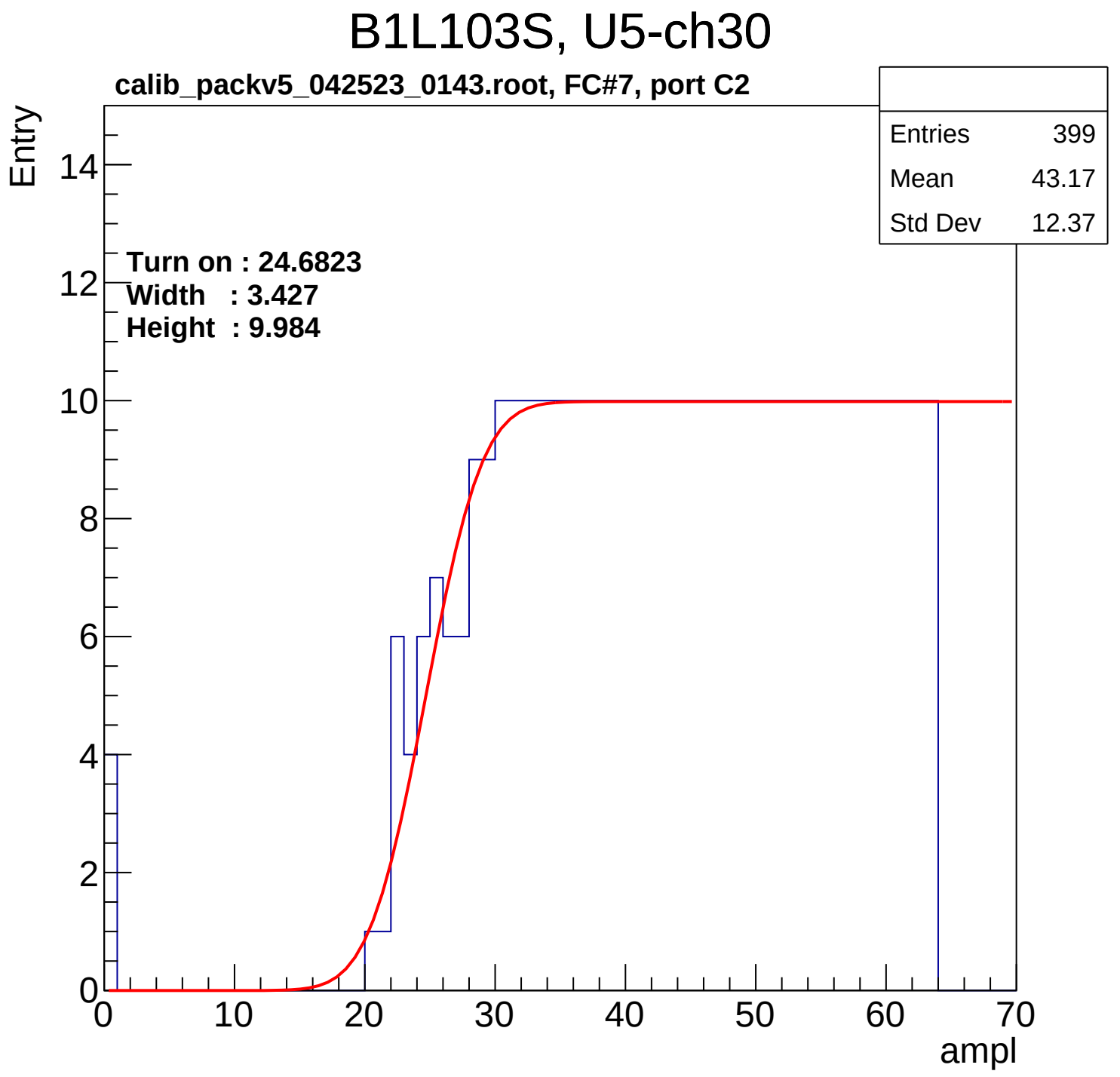

B1L103S, U5-ch25
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.14
Std Dev 11.86
Turn on : 26.3739
Width : 3.353
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

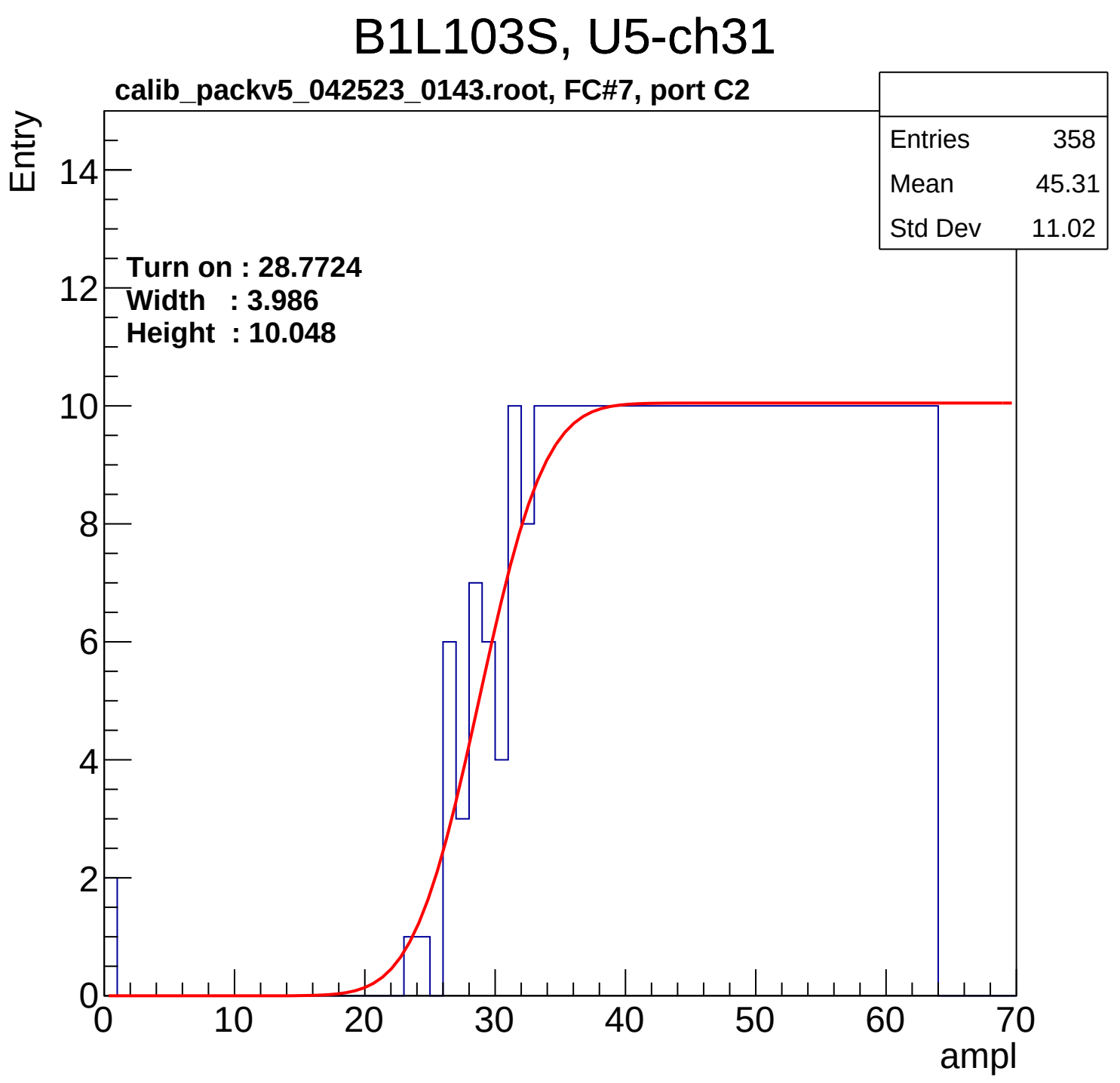

B1L103S, U5-ch26
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.73
Std Dev 11.15
Turn on : 27.1047
Width : 3.376
Height : 9.992
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

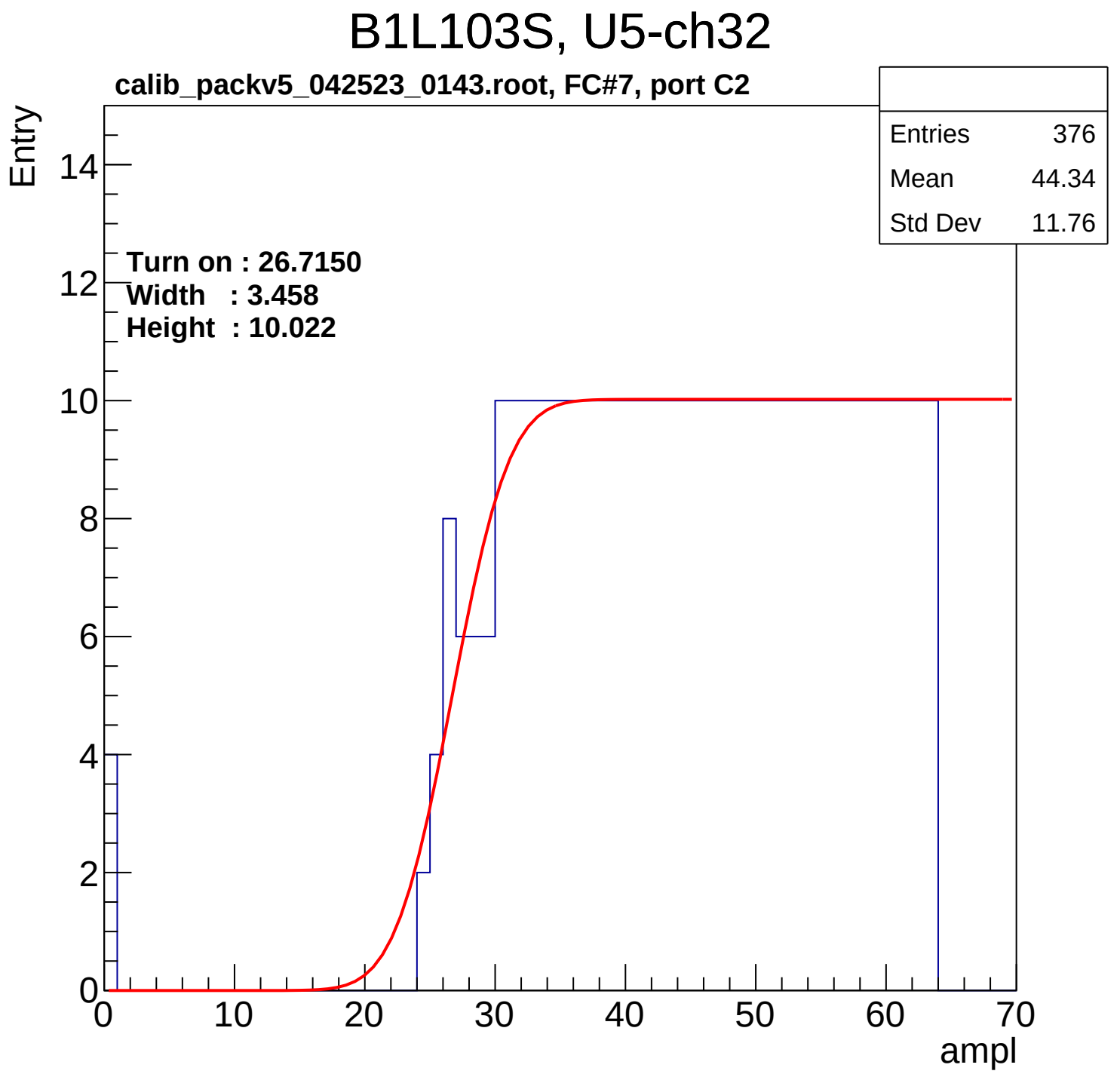

B1L103S, U5-ch27
calib_packv5_042523_0143.root, FC#7, port C2
Entries 402
Mean 43.16
Std Dev 12.11
Turn on : 23.9257
Width : 3.928
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

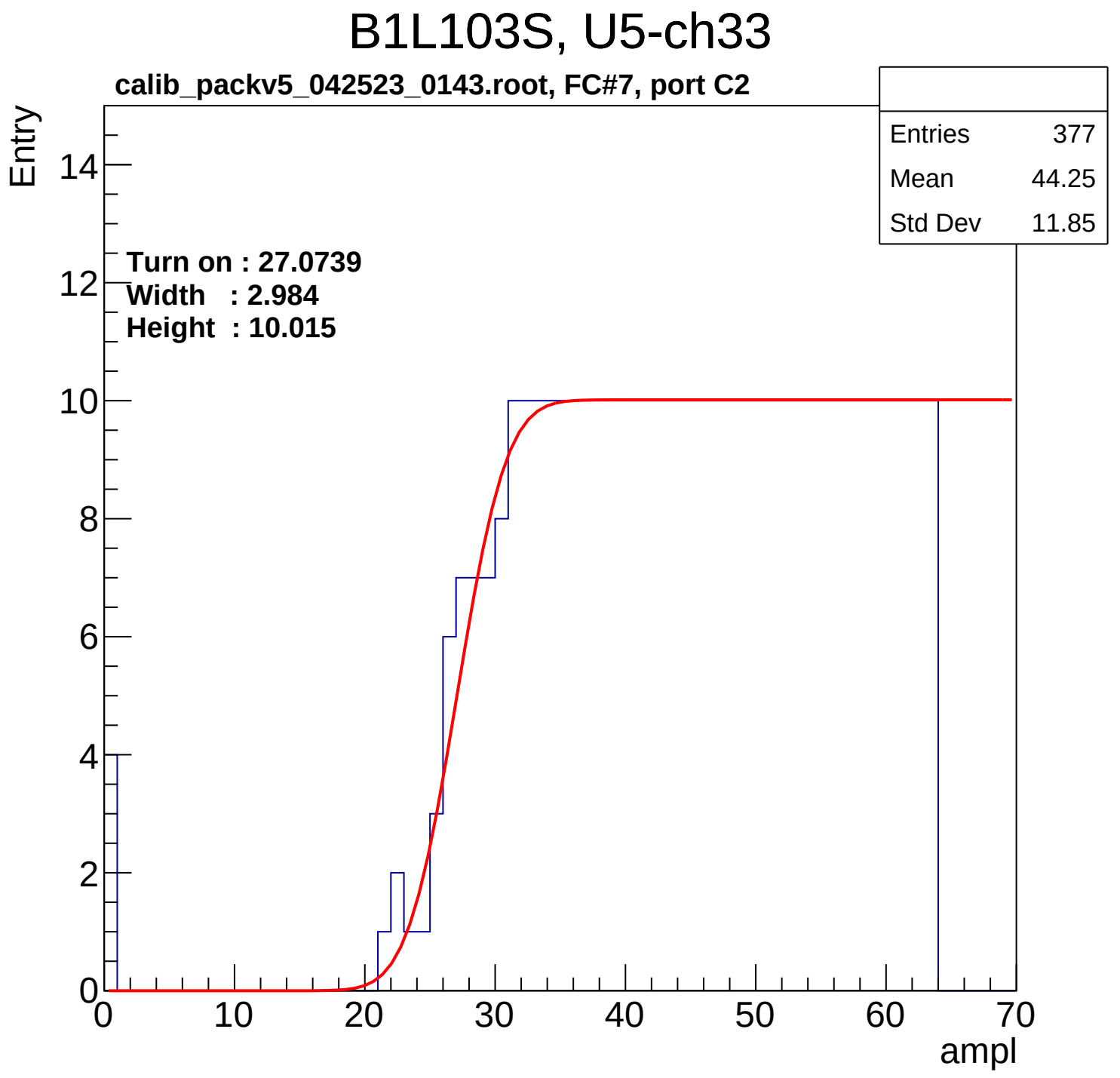

B1L103S, U5-ch28
calib_packv5_042523_0143.root, FC#7, port C2
Entries 403
Mean 43.12
Std Dev 12.12
Turn on : 24.1430
Width : 3.311
Height : 10.034
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

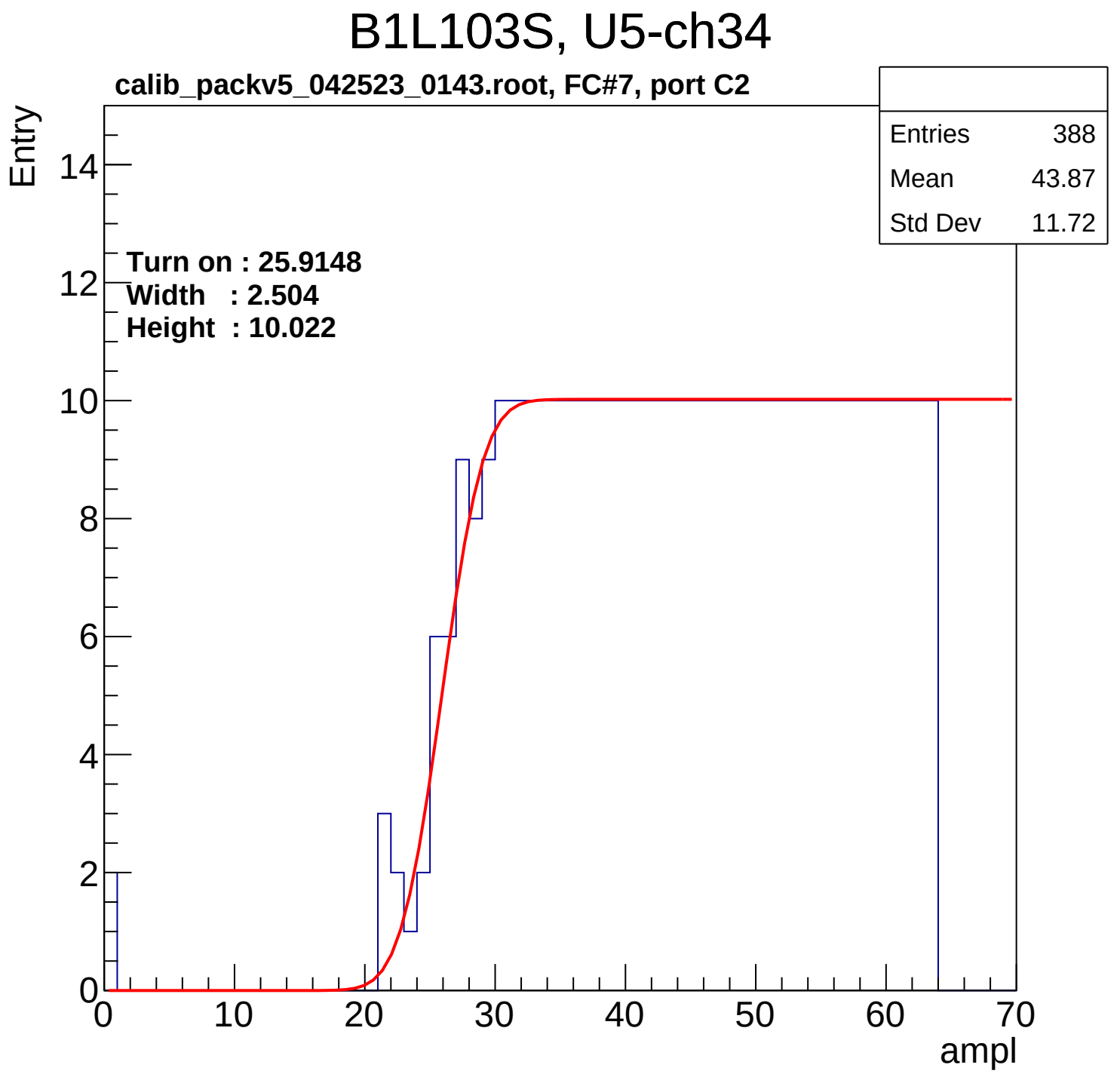

B1L103S, U5-ch29
calib_packv5_042523_0143.root, FC#7, port C2
Entries 392
Mean 43.63
Std Dev 11.95
Turn on : 24.9694
Width : 2.841
Height : 9.998
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

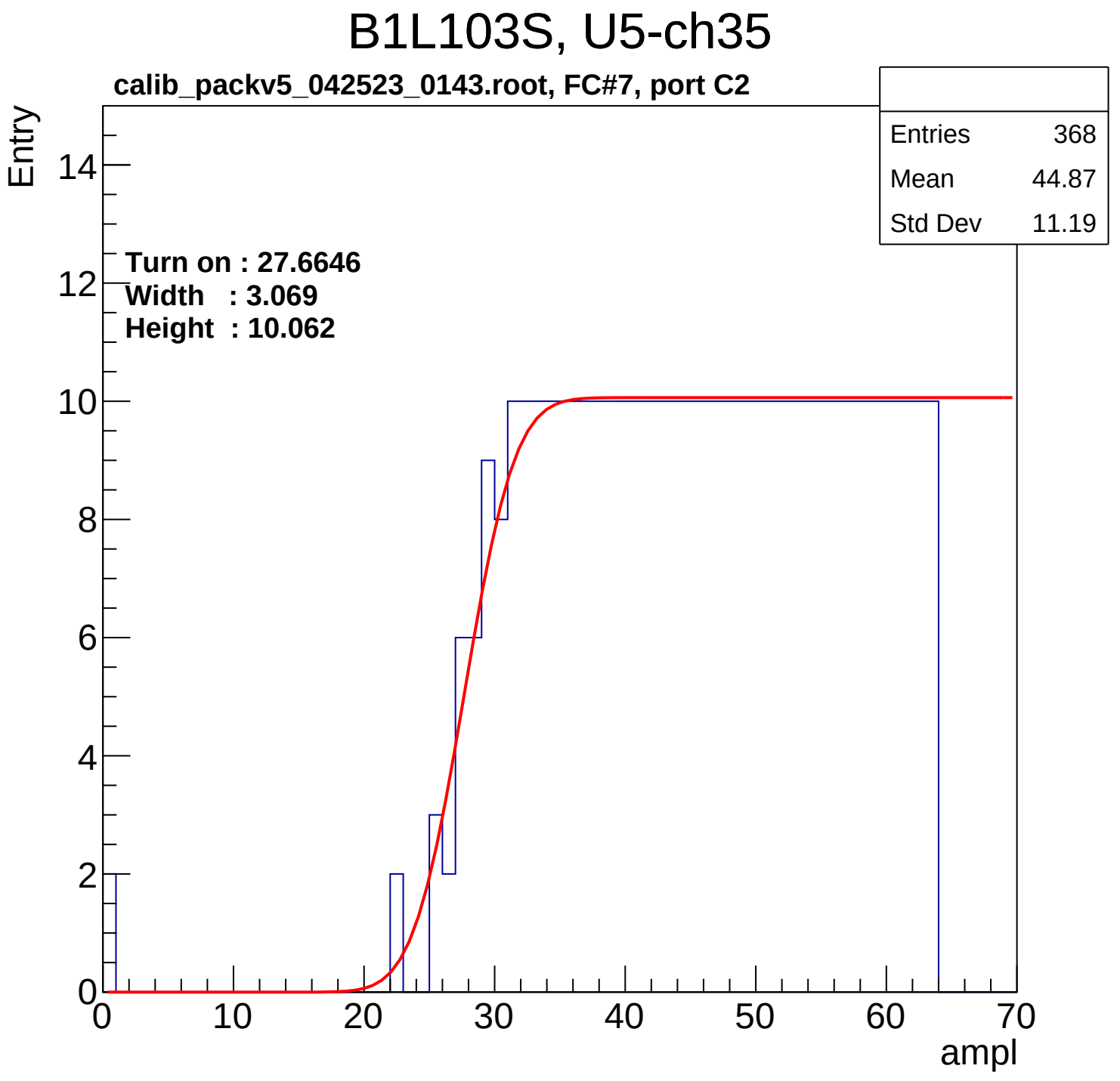

B1L103S, U5-ch30
calib_packv5_042523_0143.root, FC#7, port C2
Entries 399
Mean 43.17
Std Dev 12.37
Turn on : 24.6823
Width : 3.427
Height : 9.984
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

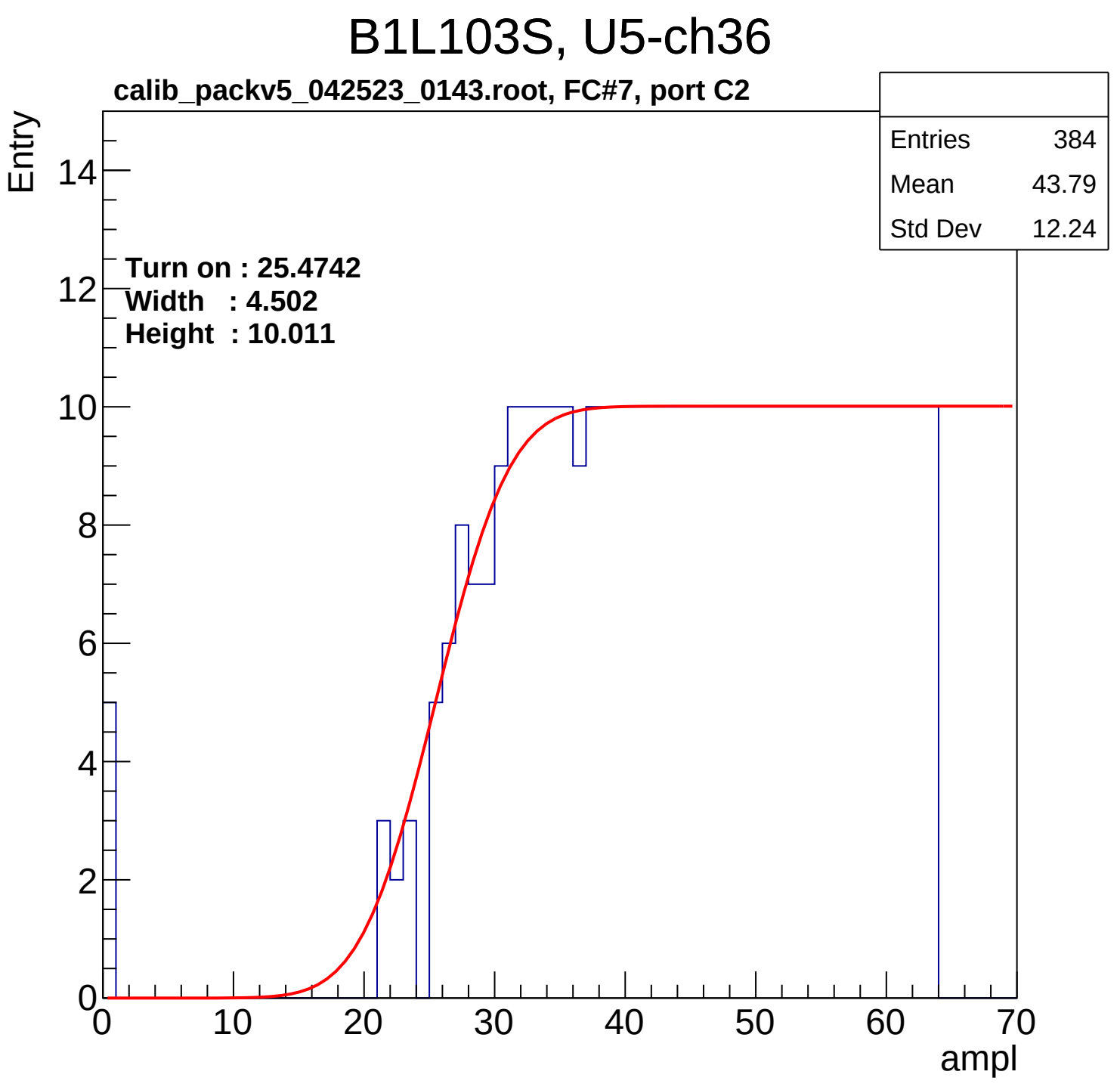

B1L103S, U5-ch31
calib_packv5_042523_0143.root, FC#7, port C2
Entries 358
Mean 45.31
Std Dev 11.02
Turn on : 28.7724
Width : 3.986
Height : 10.048
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

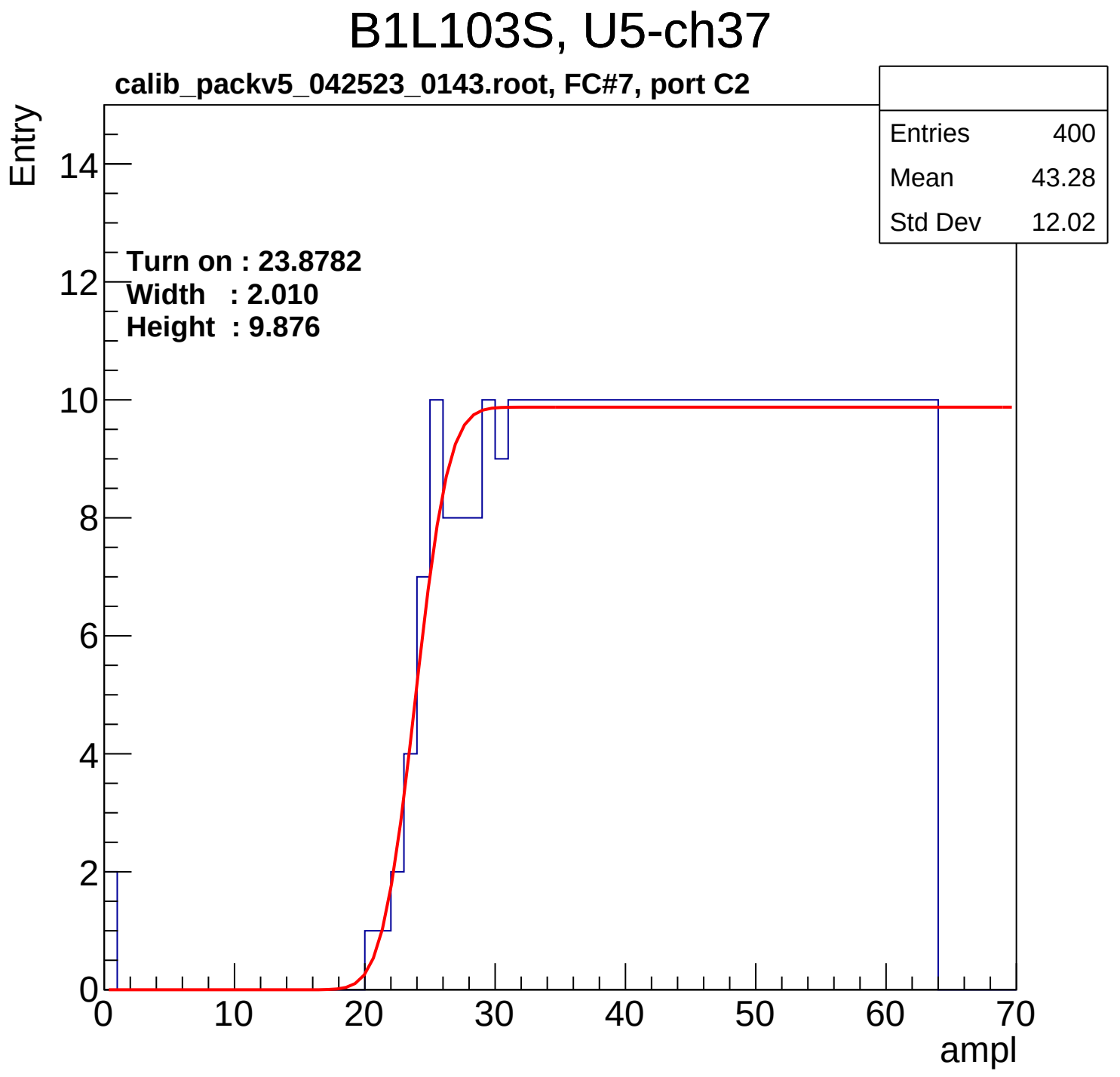

B1L103S, U5-ch32
calib_packv5_042523_0143.root, FC#7, port C2
Entries 376
Mean 44.34
Std Dev 11.76
Turn on : 26.7150
Width : 3.458
Height : 10.022
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

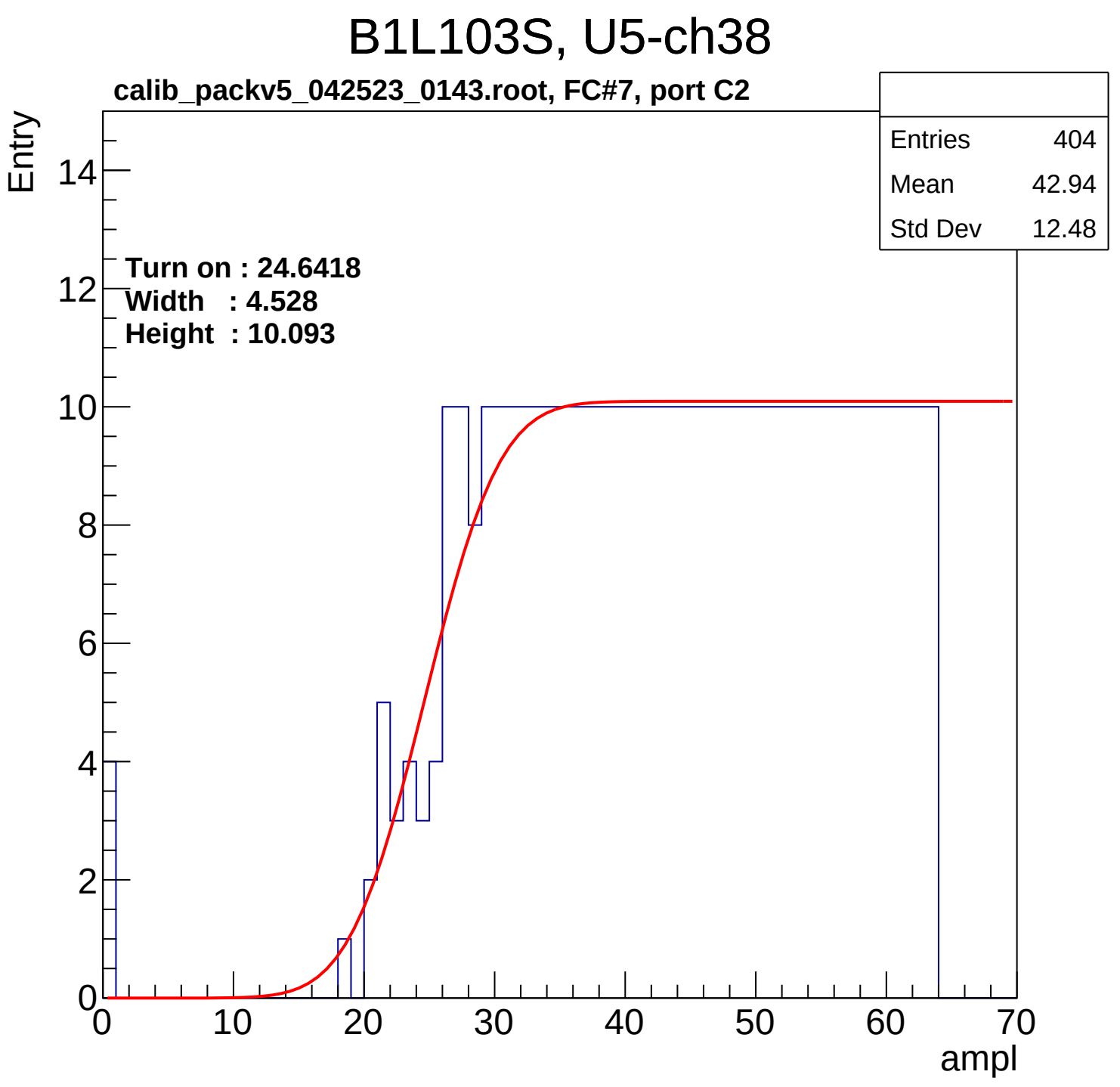

B1L103S, U5-ch33
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.25
Std Dev 11.85
Turn on : 27.0739
Width : 2.984
Height : 10.015
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

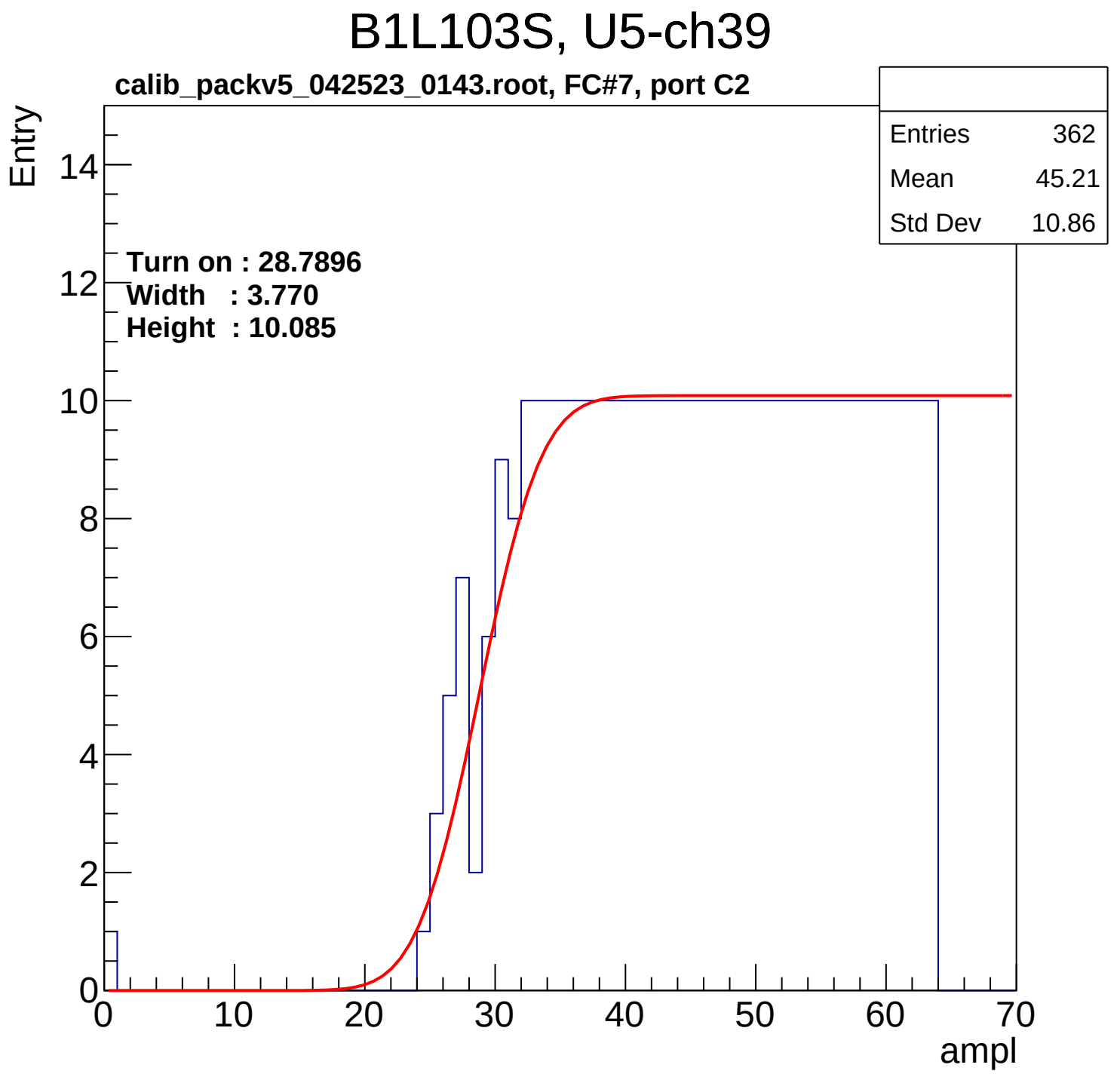

B1L103S, U5-ch34
calib_packv5_042523_0143.root, FC#7, port C2
Entries 388
Mean 43.87
Std Dev 11.72
Turn on : 25.9148
Width : 2.504
Height : 10.022
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

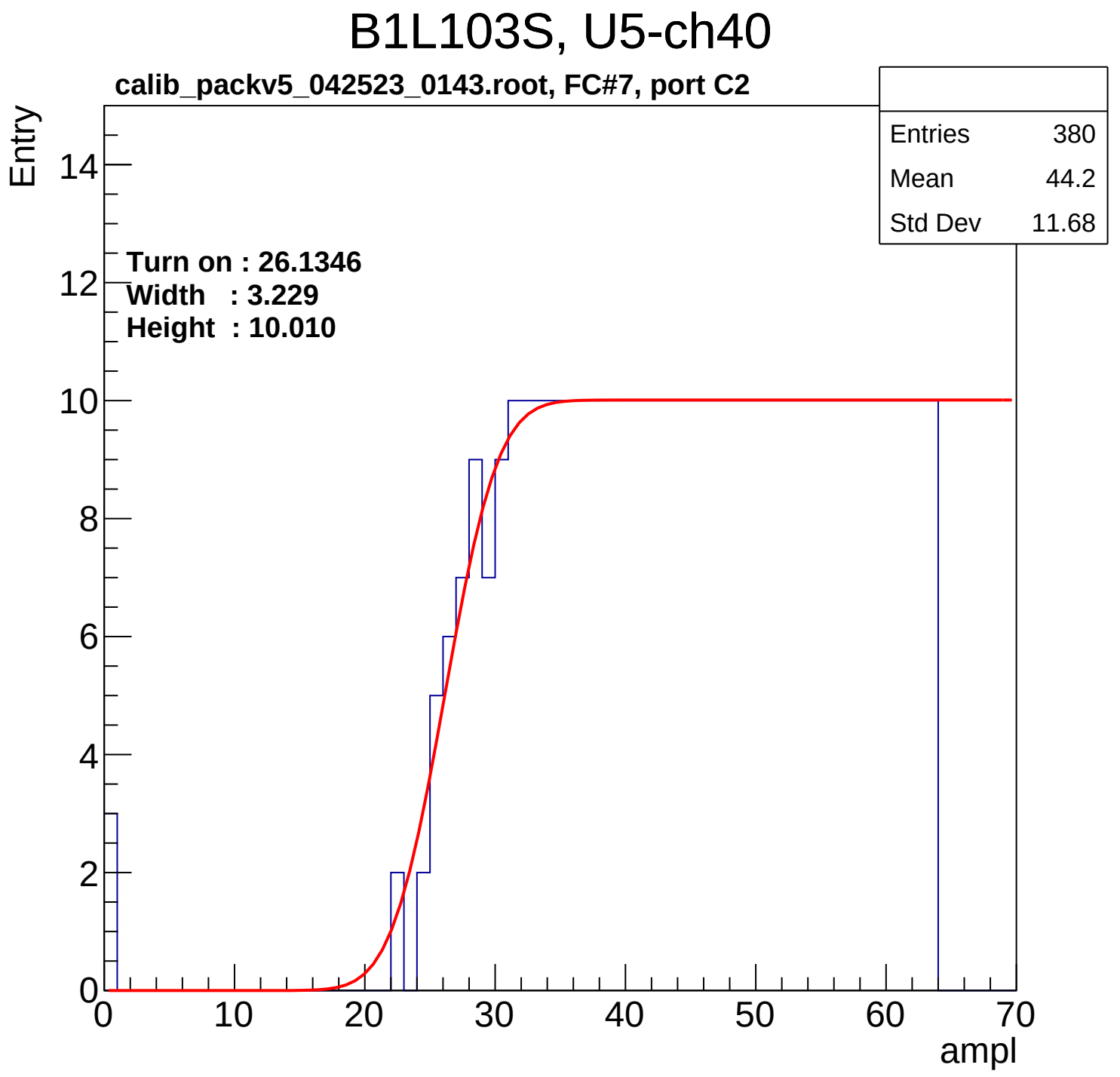

B1L103S, U5-ch35
calib_packv5_042523_0143.root, FC#7, port C2
Entries 368
Mean 44.87
Std Dev 11.19
Turn on : 27.6646
Width : 3.069
Height : 10.062
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

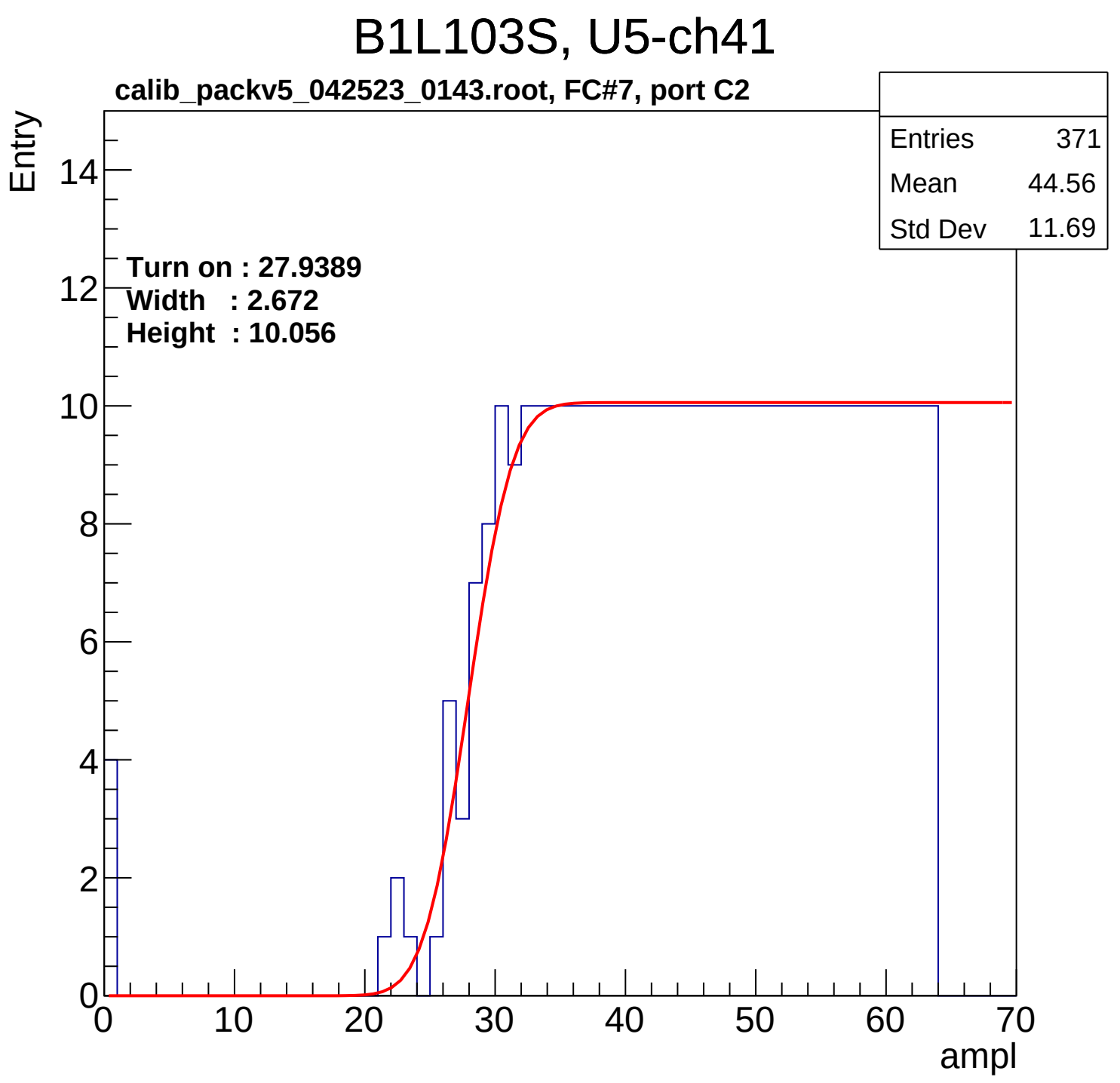

B1L103S, U5-ch36
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 43.79
Std Dev 12.24
Turn on : 25.4742
Width : 4.502
Height : 10.011
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

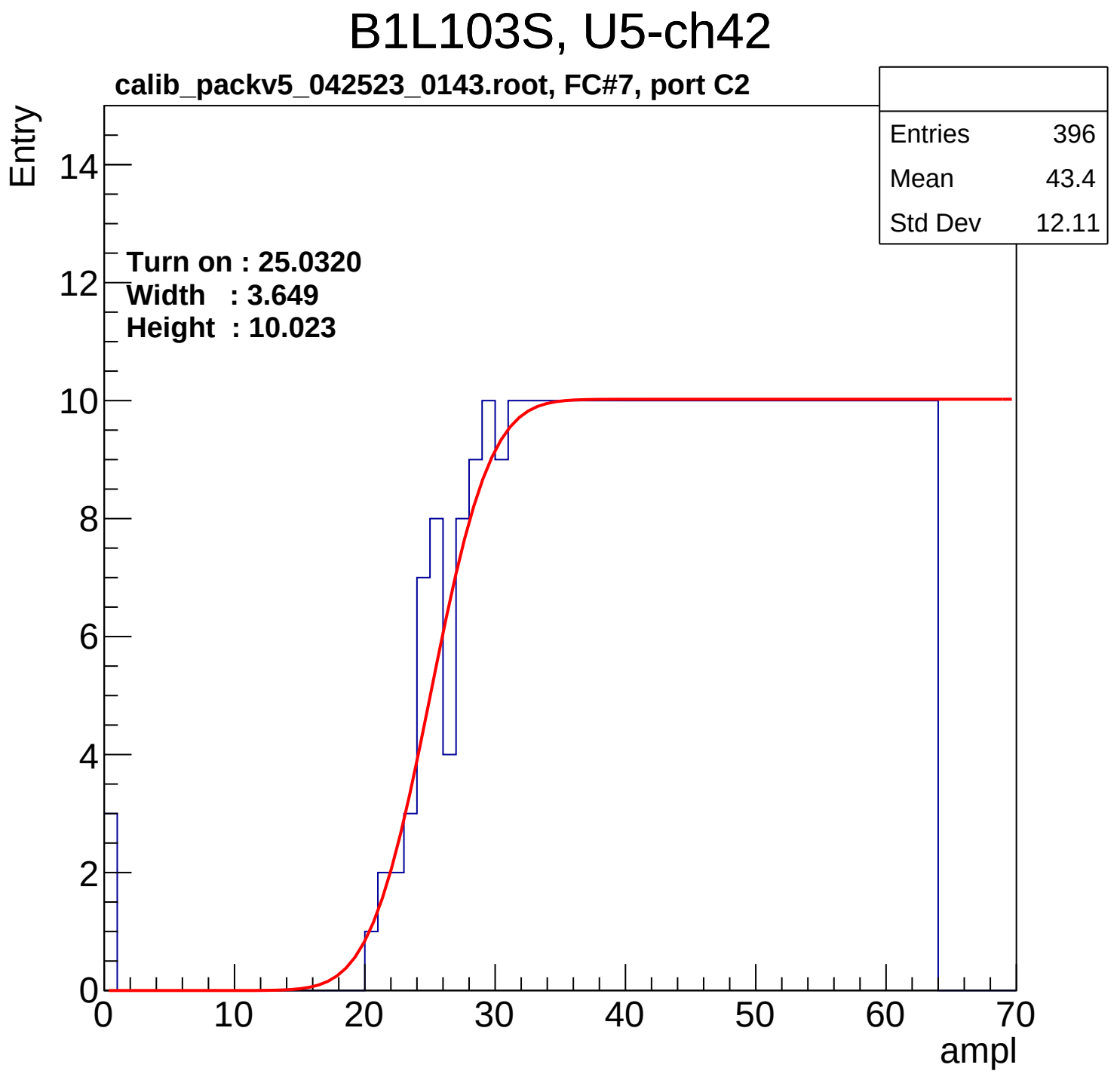

B1L103S, U5-ch37
calib_packv5_042523_0143.root, FC#7, port C2
Entries 400
Mean 43.28
Std Dev 12.02
Turn on : 23.8782
Width : 2.010
Height : 9.876
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

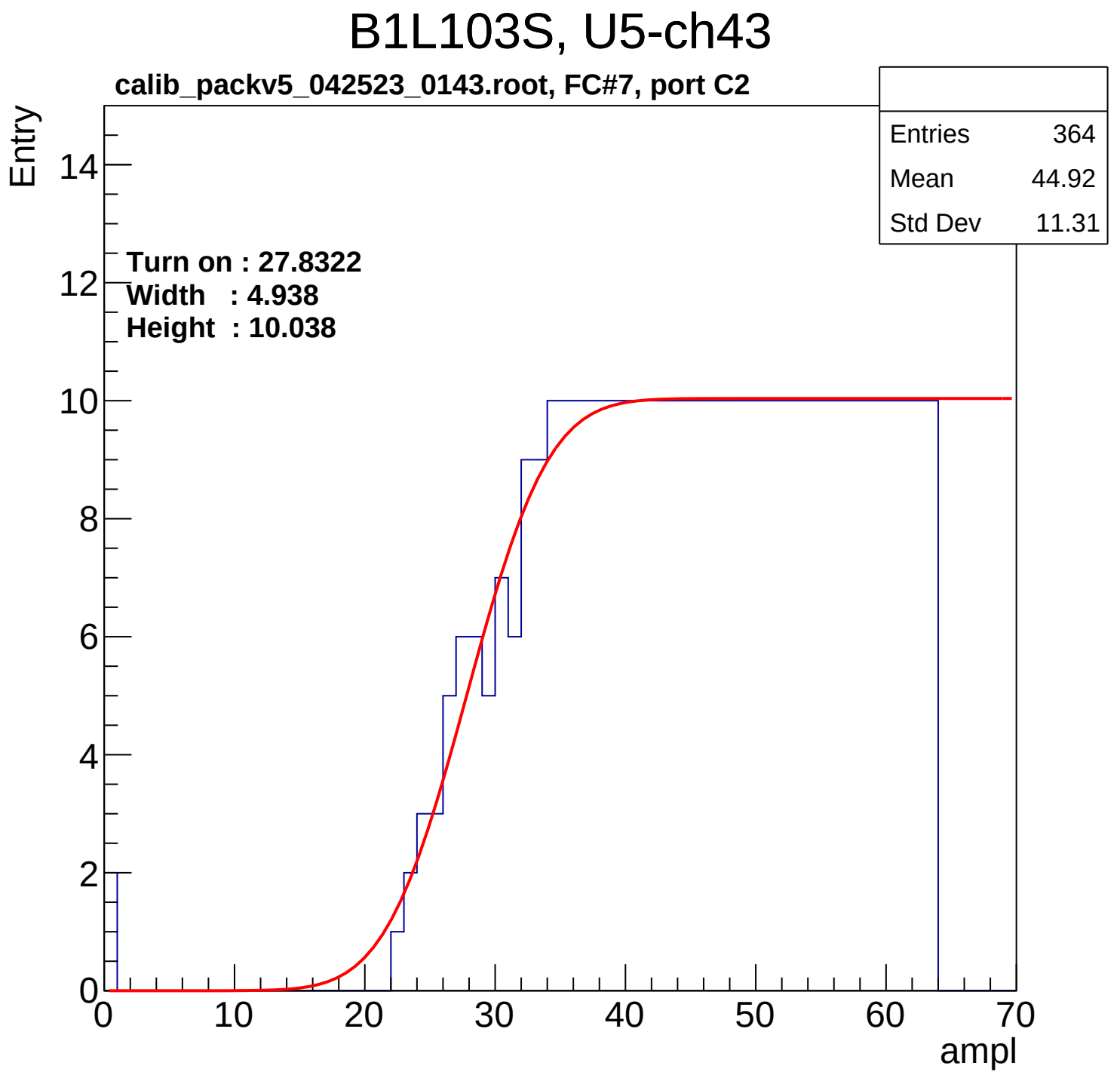

B1L103S, U5-ch38
calib_packv5_042523_0143.root, FC#7, port C2
Entries 404
Mean 42.94
Std Dev 12.48
Turn on : 24.6418
Width : 4.528
Height : 10.093
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

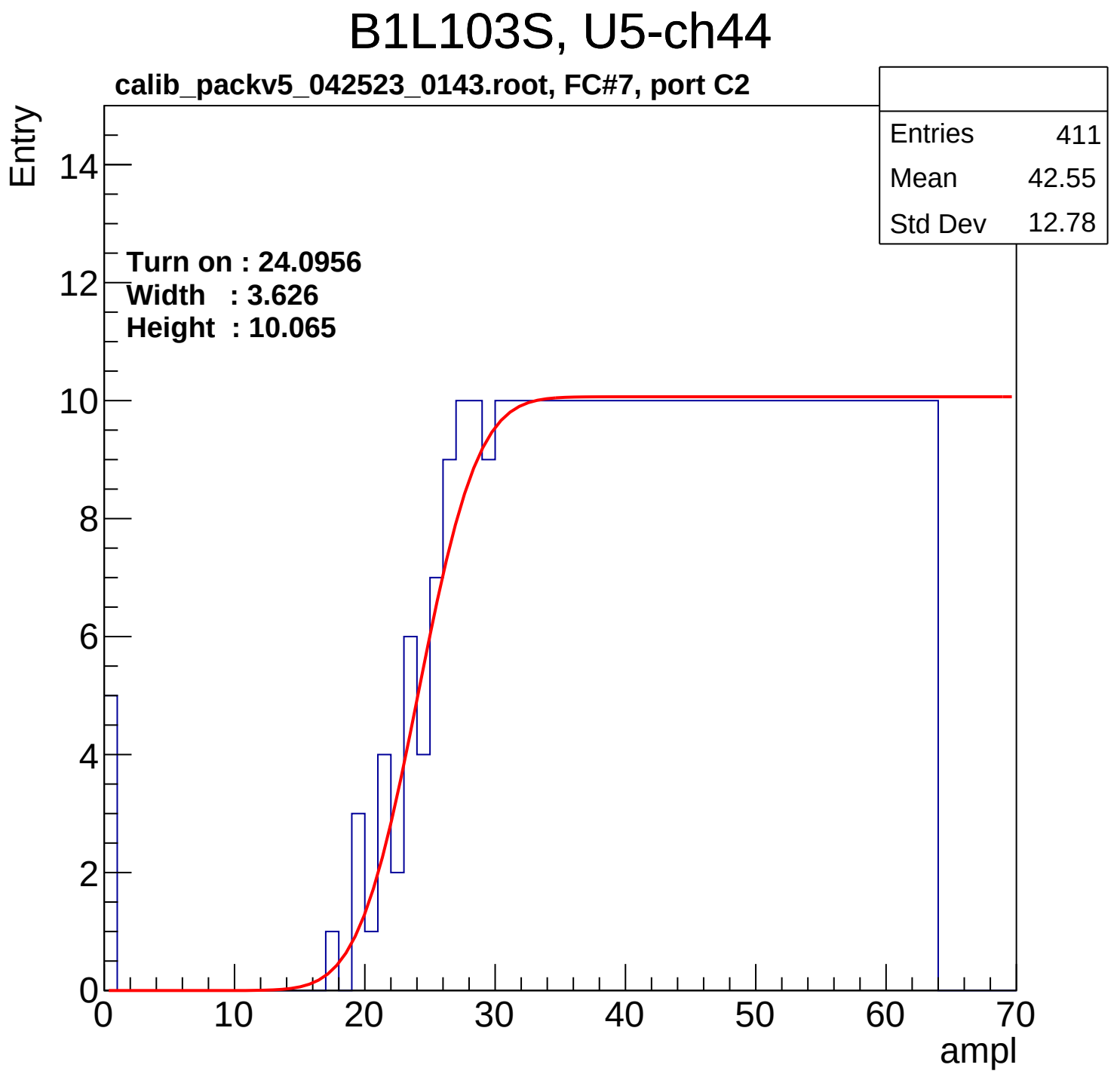

B1L103S, U5-ch39
calib_packv5_042523_0143.root, FC#7, port C2
Entries 362
Mean 45.21
Std Dev 10.86
Turn on : 28.7896
Width : 3.770
Height : 10.085
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

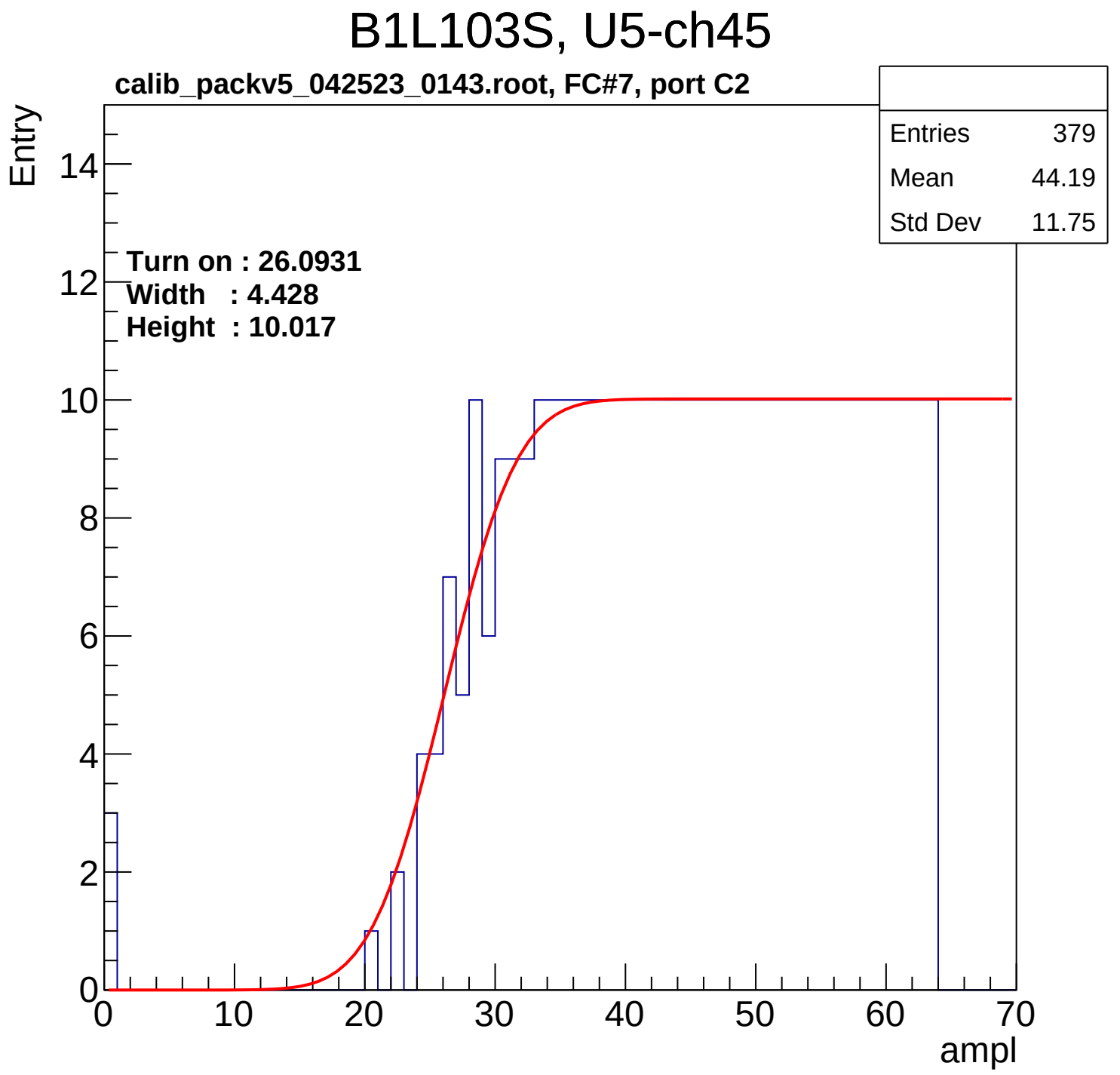

B1L103S, U5-ch40
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.2
Std Dev 11.68
Turn on : 26.1346
Width : 3.229
Height : 10.010
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

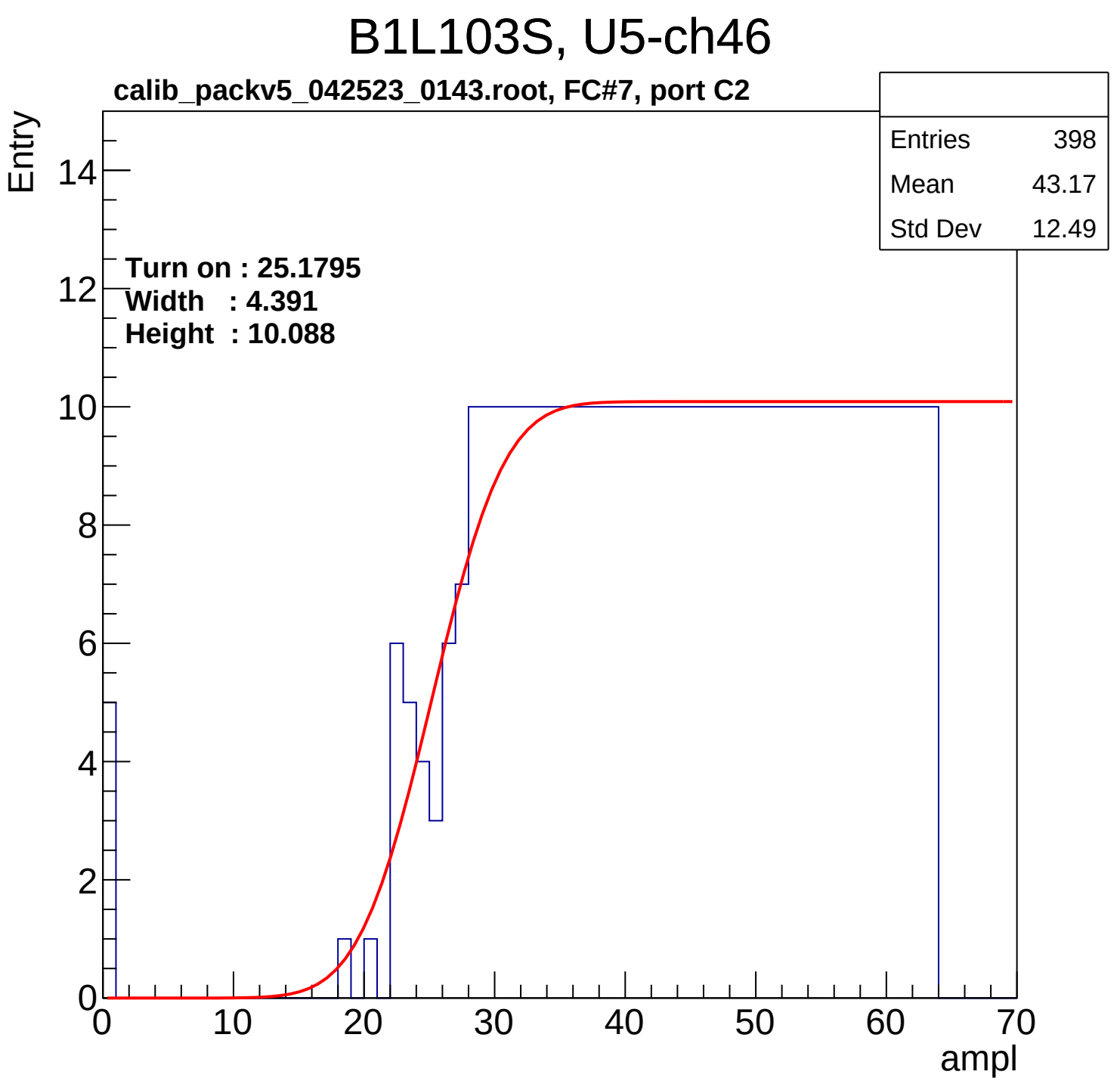

B1L103S, U5-ch41
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.56
Std Dev 11.69
Turn on : 27.9389
Width : 2.672
Height : 10.056
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

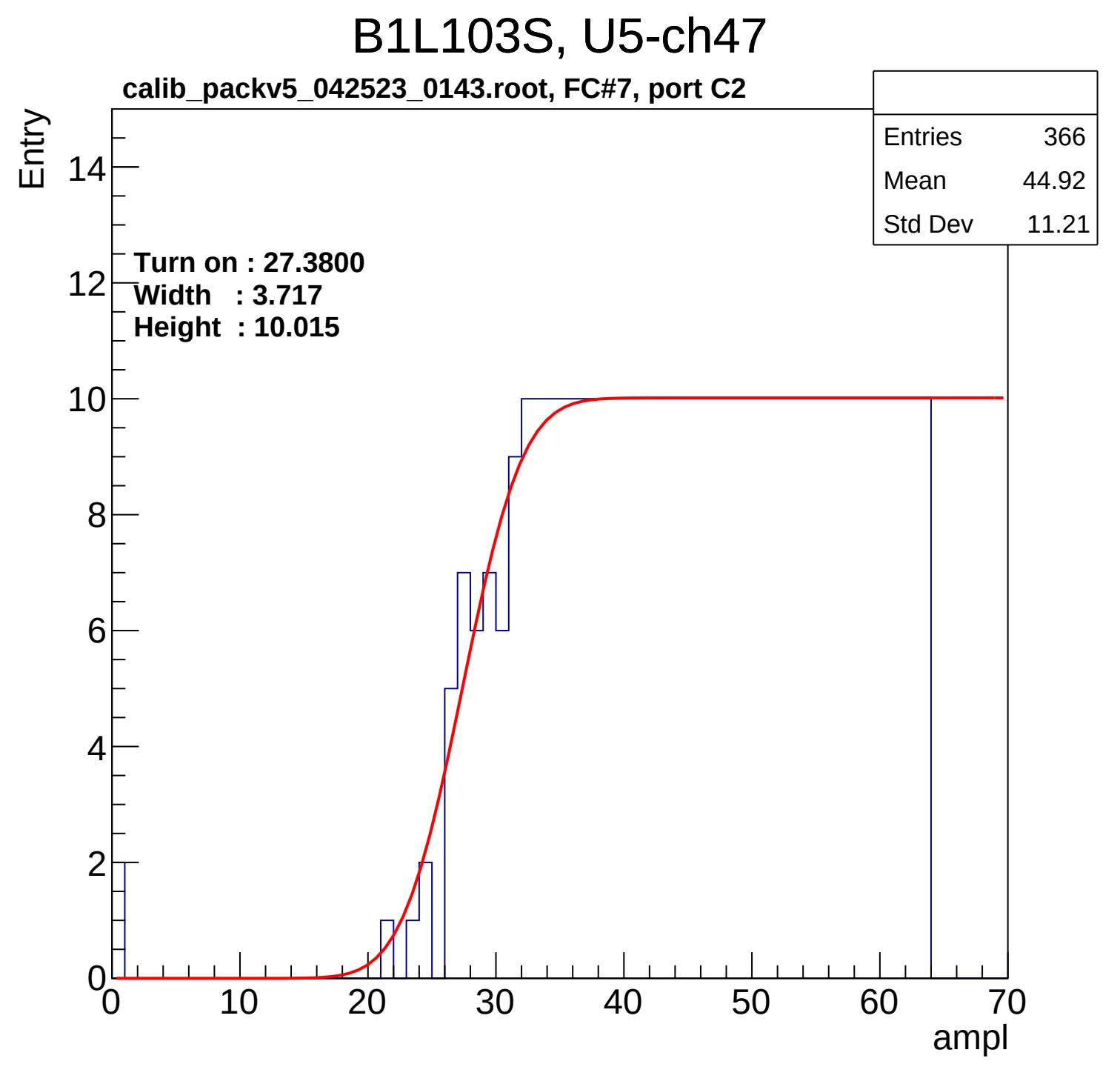

B1L103S, U5-ch42
calib_packv5_042523_0143.root, FC#7, port C2
Entries 396
Mean 43.4
Std Dev 12.11
Turn on : 25.0320
Width : 3.649
Height : 10.023
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

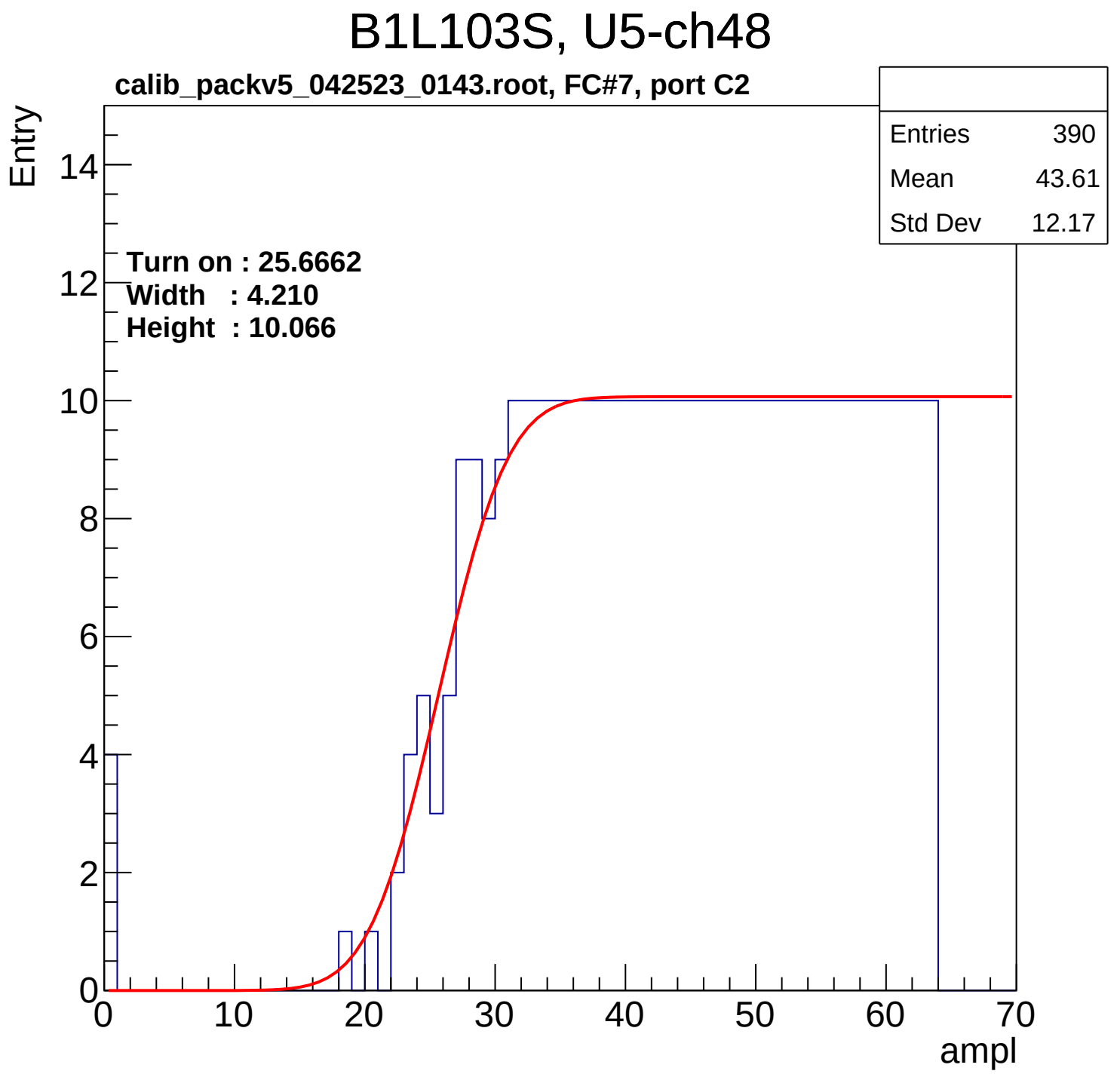

B1L103S, U5-ch43
calib_packv5_042523_0143.root, FC#7, port C2
Entries 364
Mean 44.92
Std Dev 11.31
Turn on : 27.8322
Width : 4.938
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

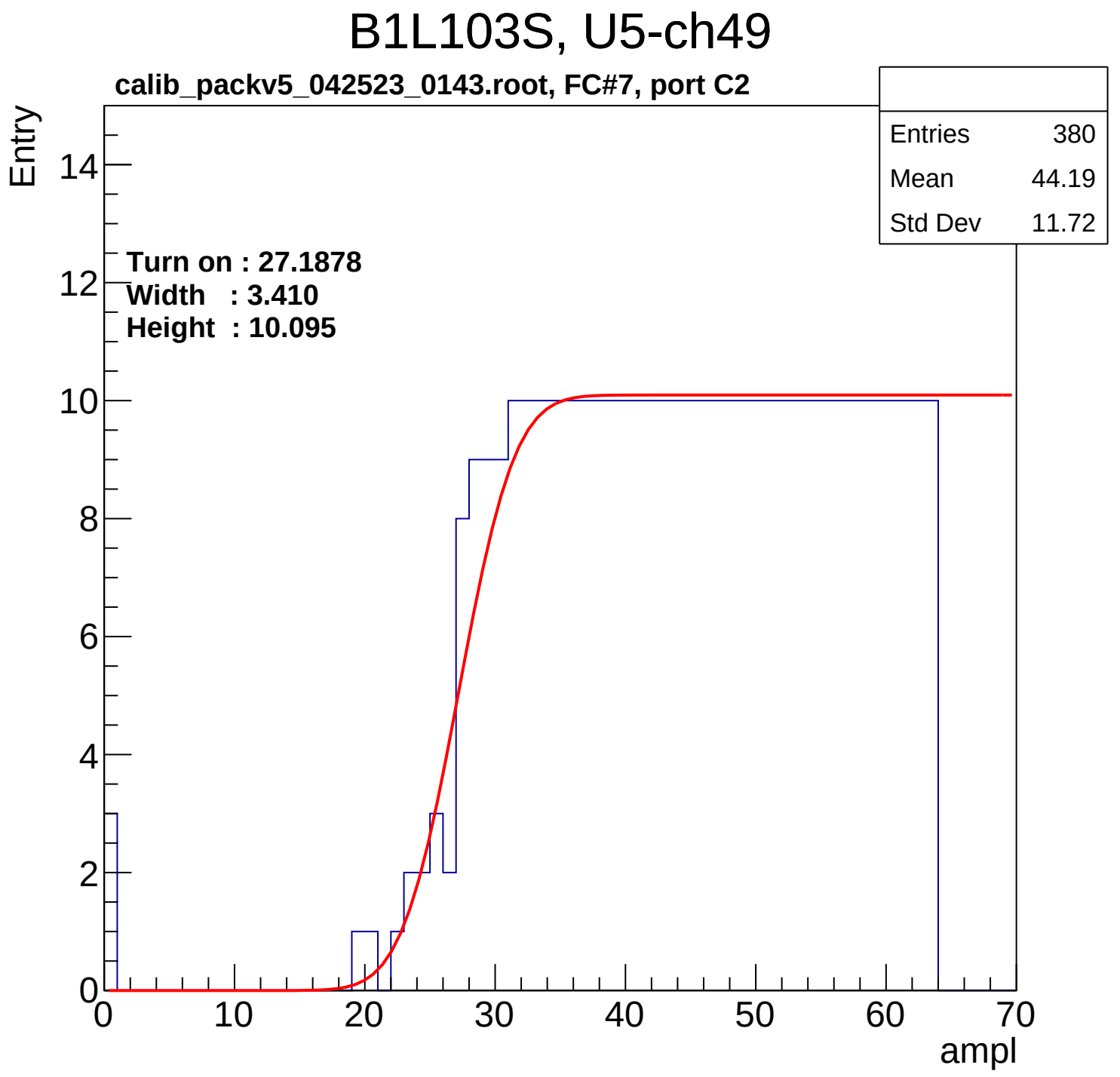

B1L103S, U5-ch44
calib_packv5_042523_0143.root, FC#7, port C2
Entries 411
Mean 42.55
Std Dev 12.78
Turn on : 24.0956
Width : 3.626
Height : 10.065
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

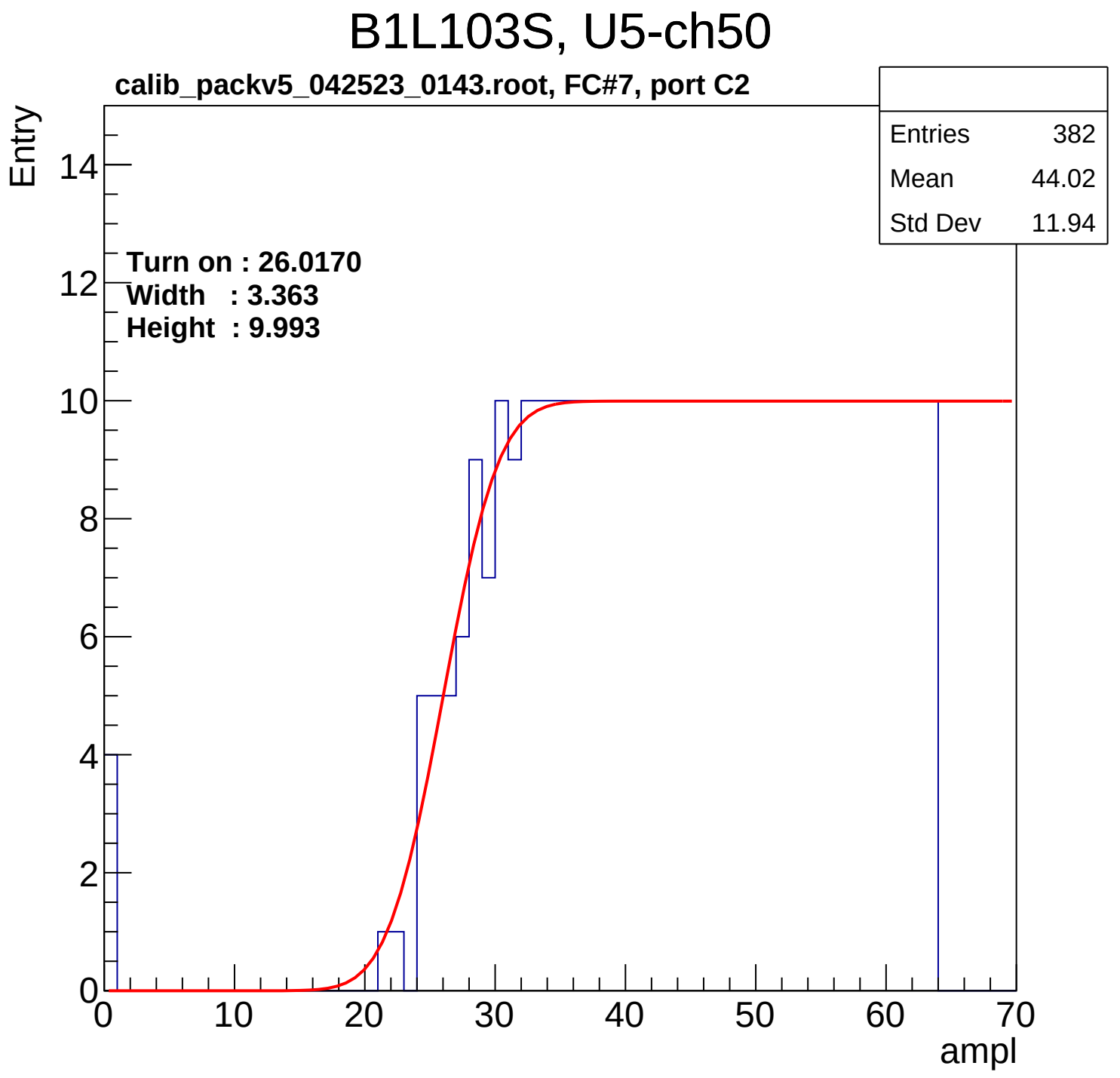

B1L103S, U5-ch45
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.19
Std Dev 11.75
Turn on : 26.0931
Width : 4.428
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

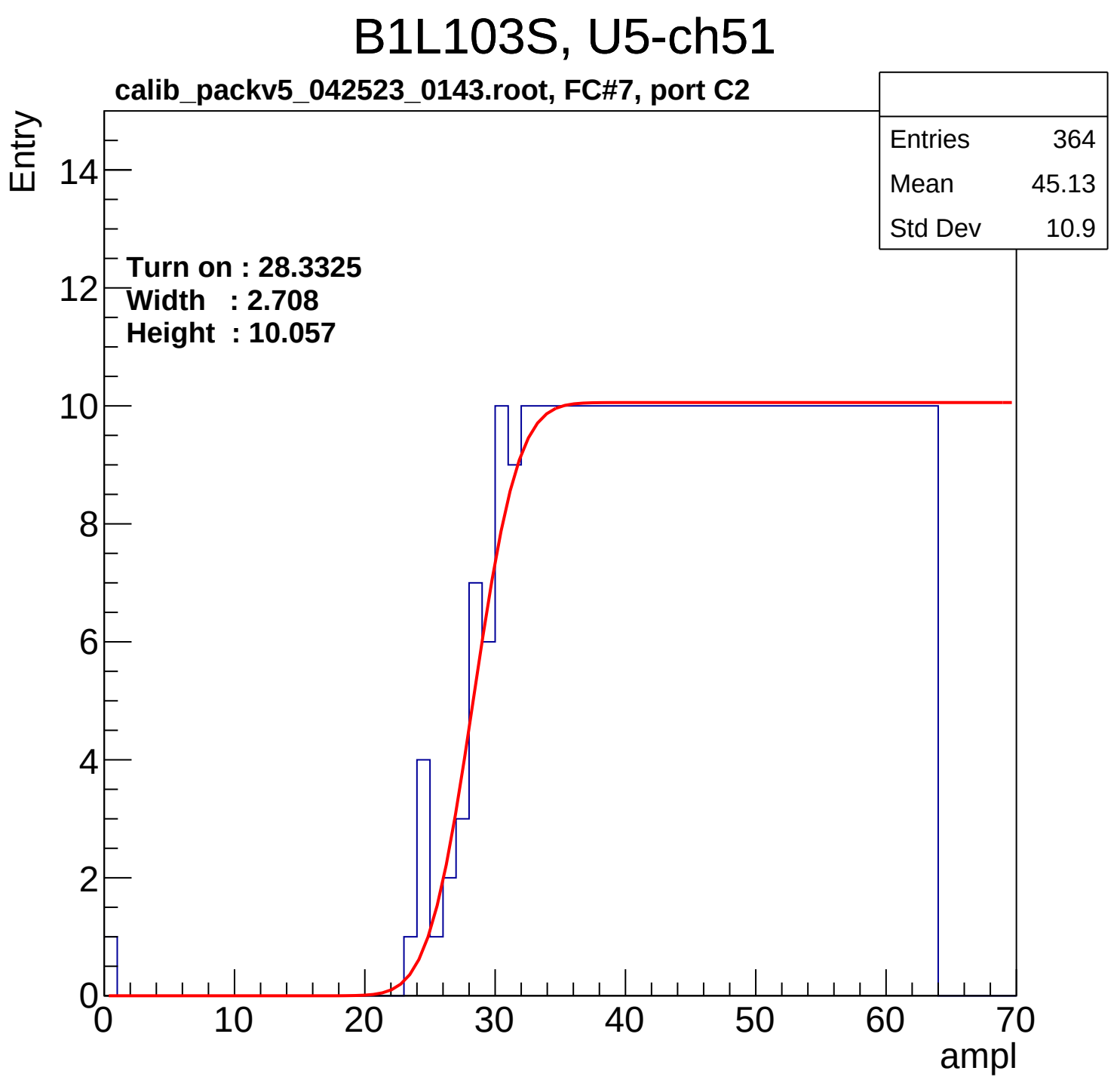

B1L103S, U5-ch46
calib_packv5_042523_0143.root, FC#7, port C2
Entries 398
Mean 43.17
Std Dev 12.49
Turn on : 25.1795
Width : 4.391
Height : 10.088
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

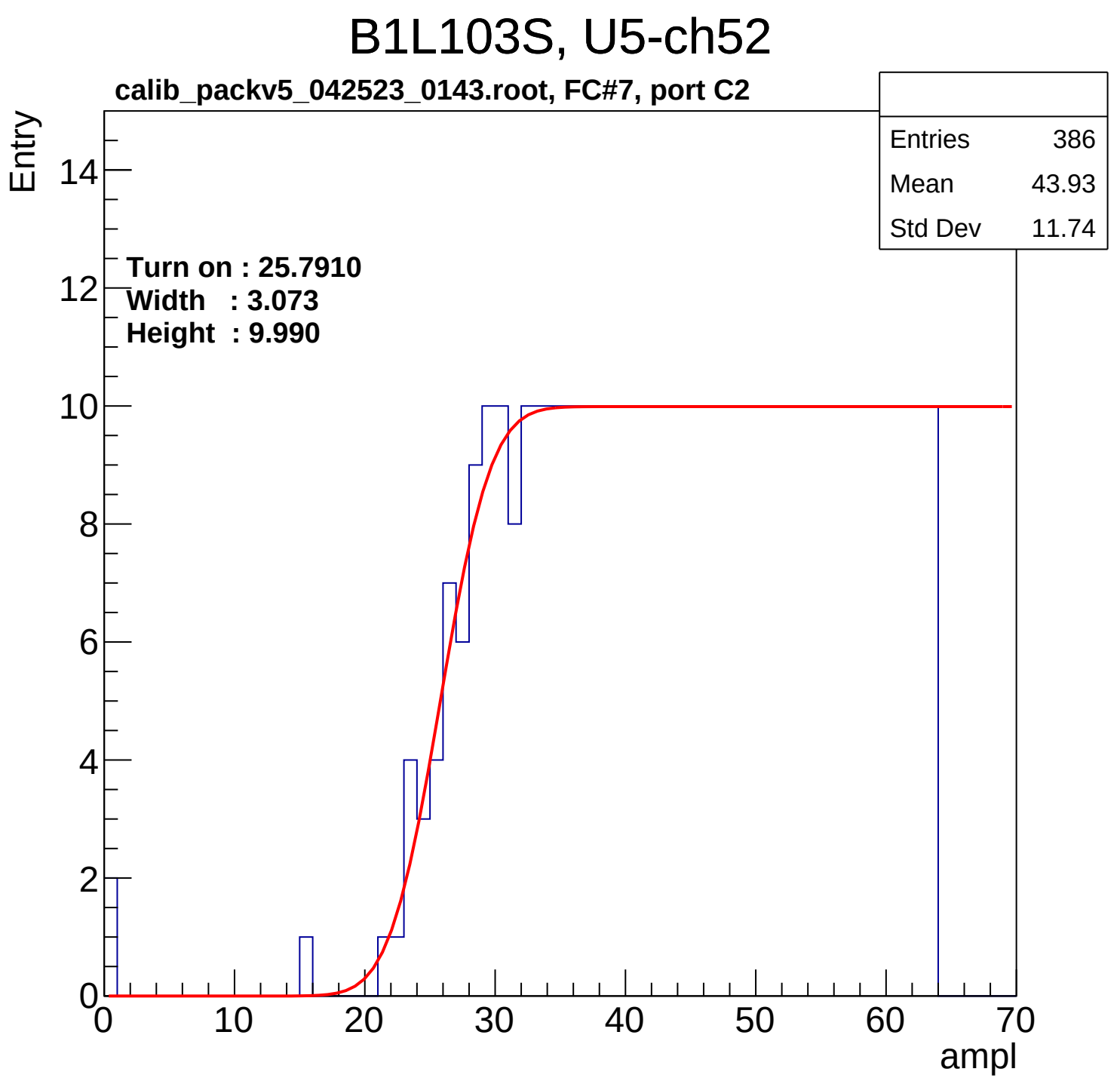

B1L103S, U5-ch47
calib_packv5_042523_0143.root, FC#7, port C2
Entries 366
Mean 44.92
Std Dev 11.21
Turn on : 27.3800
Width : 3.717
Height : 10.015
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

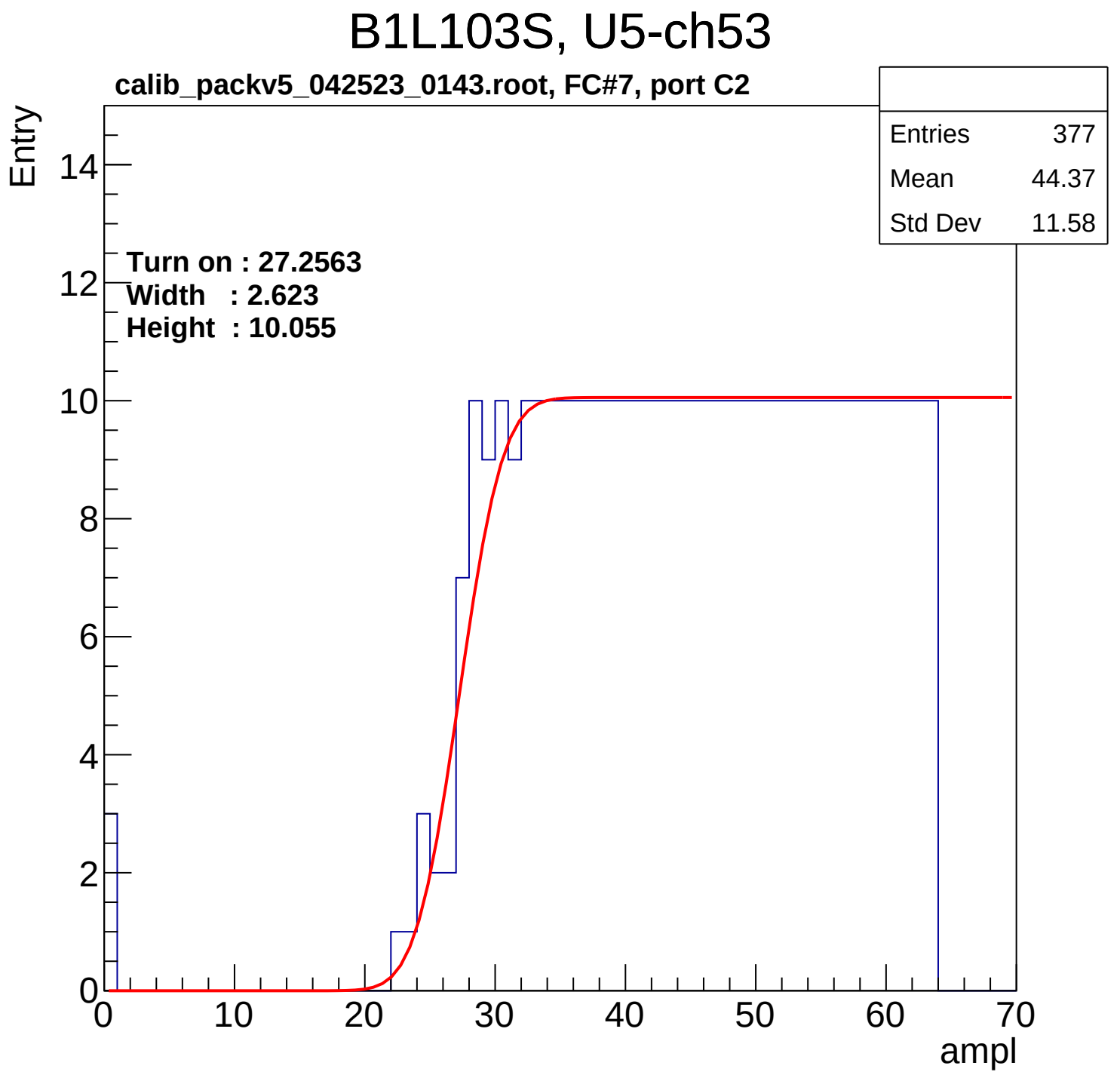

B1L103S, U5-ch48
calib_packv5_042523_0143.root, FC#7, port C2
Entries 390
Mean 43.61
Std Dev 12.17
Turn on : 25.6662
Width : 4.210
Height : 10.066
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

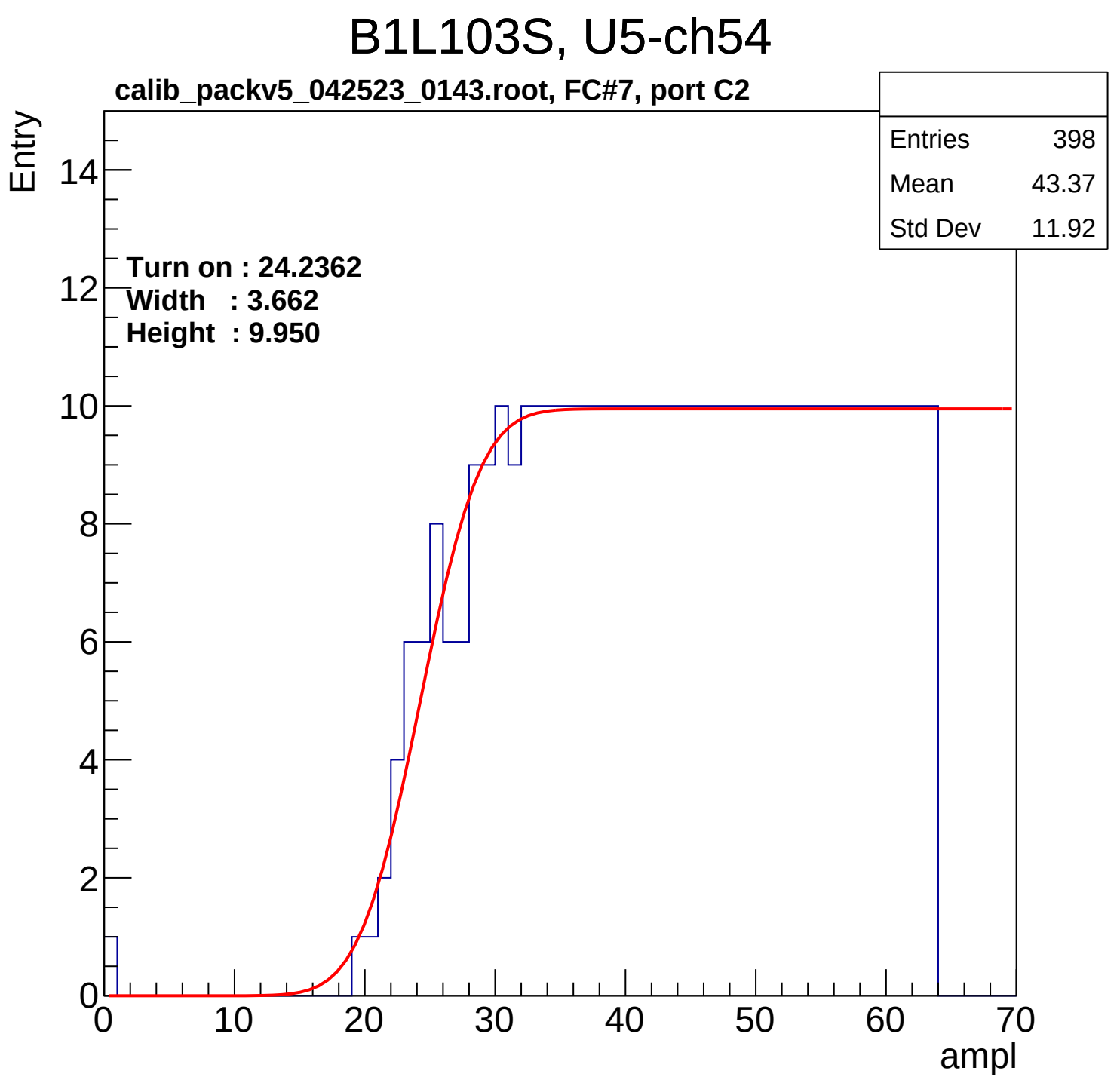

B1L103S, U5-ch49
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.19
Std Dev 11.72
Turn on : 27.1878
Width : 3.410
Height : 10.095
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

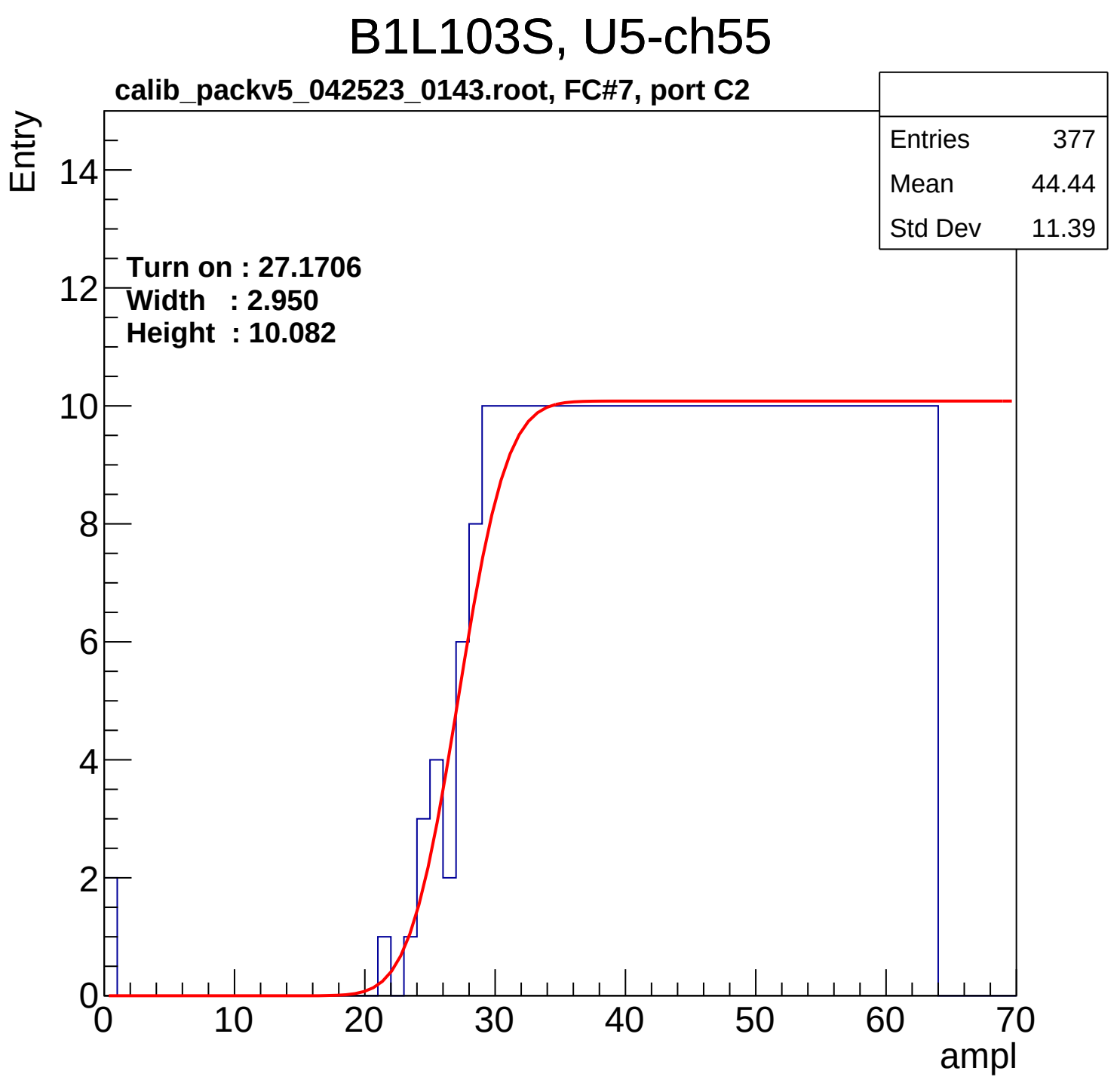

B1L103S, U5-ch50
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 44.02
Std Dev 11.94
Turn on : 26.0170
Width : 3.363
Height : 9.993
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

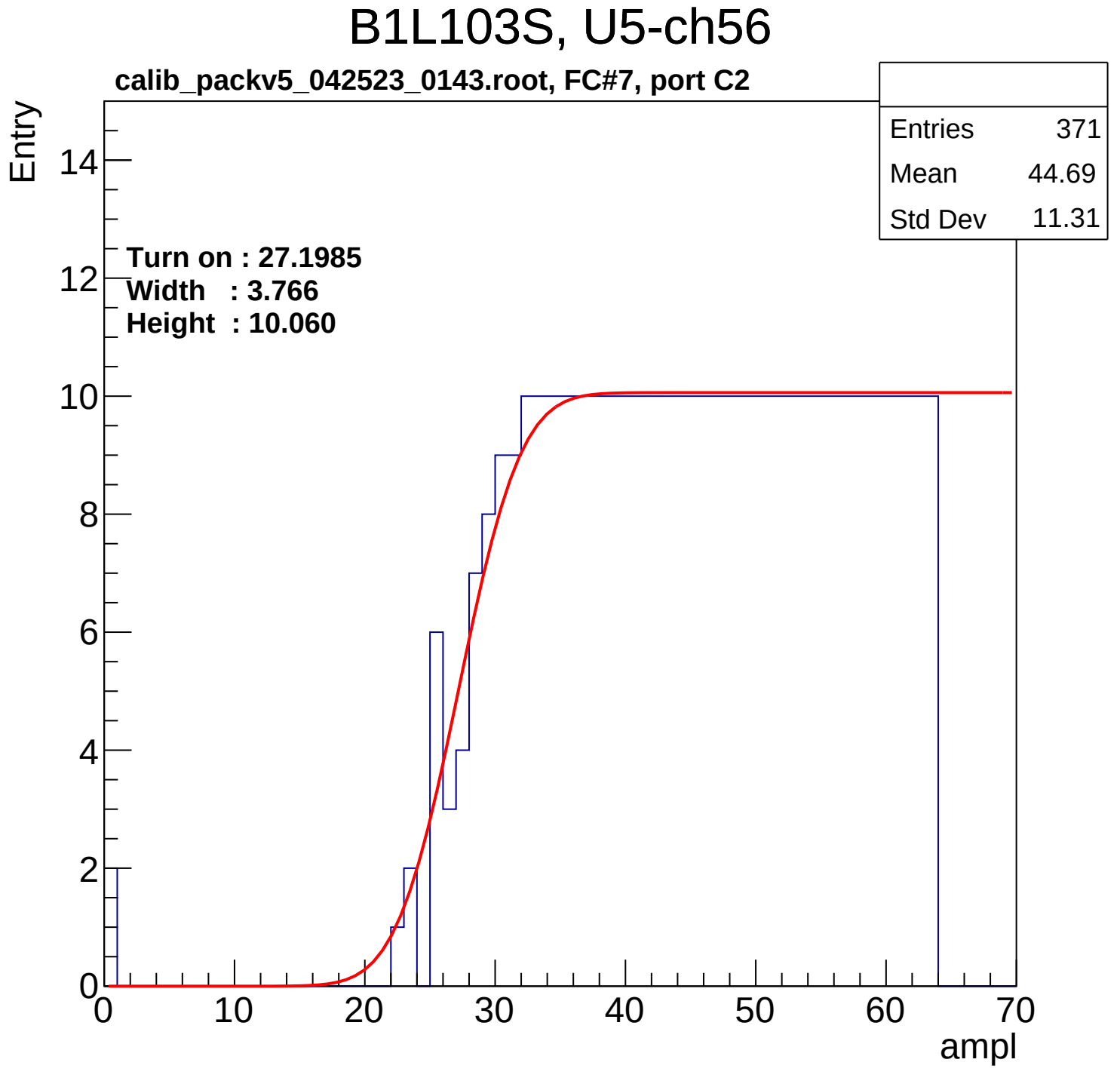

B1L103S, U5-ch51
calib_packv5_042523_0143.root, FC#7, port C2
Entries 364
Mean 45.13
Std Dev 10.9
Turn on : 28.3325
Width : 2.708
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

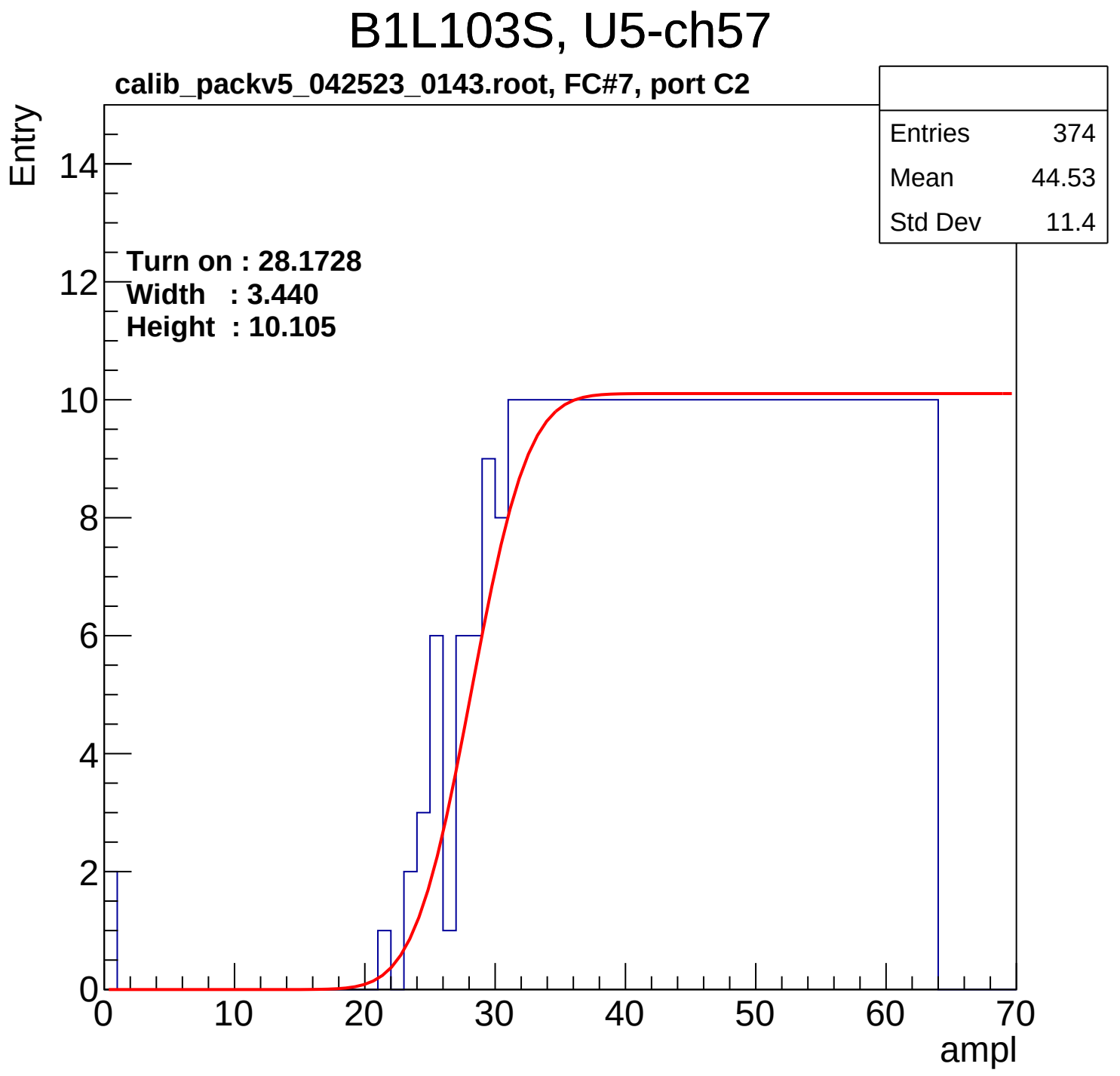

B1L103S, U5-ch52
calib_packv5_042523_0143.root, FC#7, port C2
Entries 386
Mean 43.93
Std Dev 11.74
Turn on : 25.7910
Width : 3.073
Height : 9.990
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

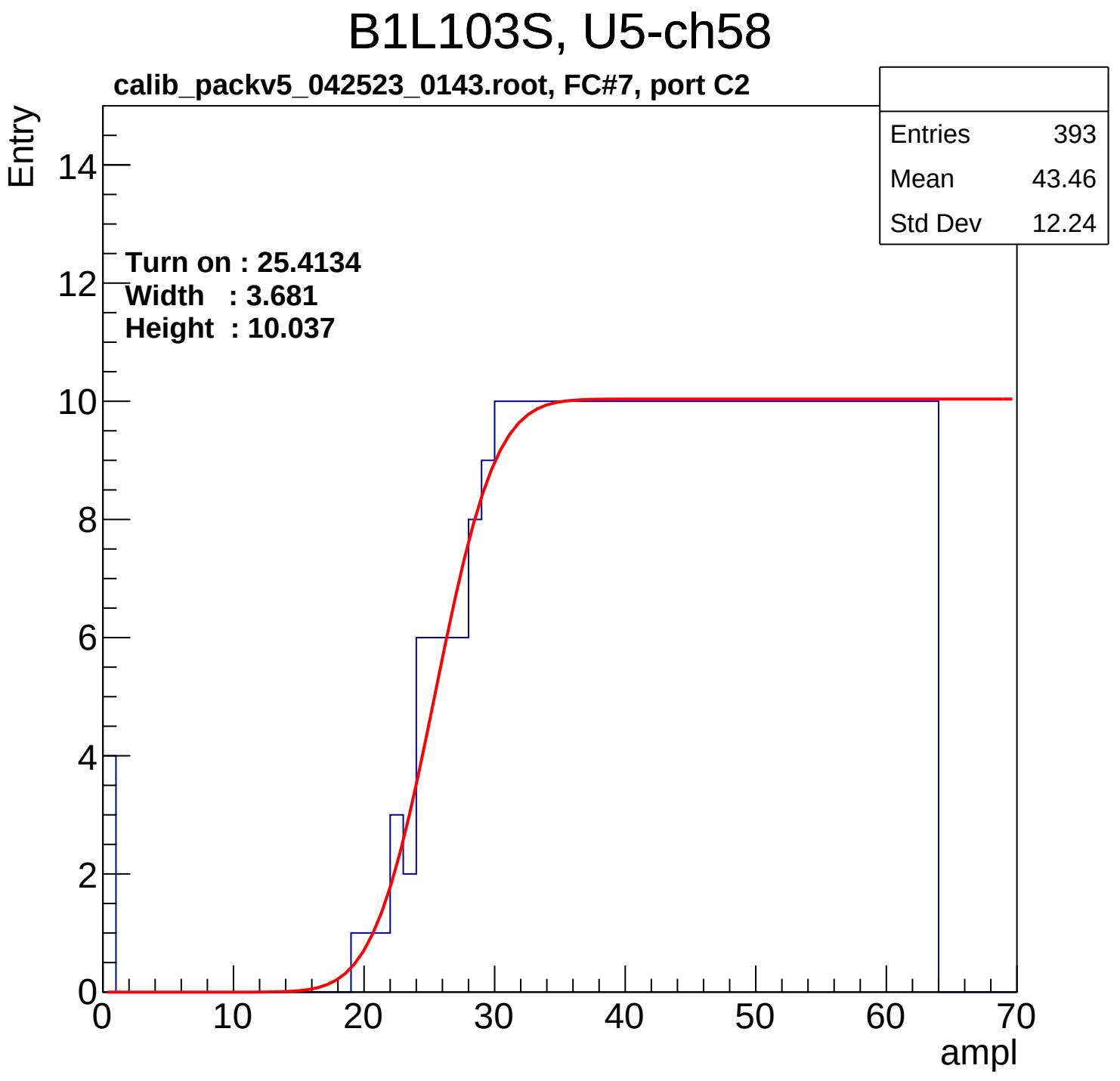

B1L103S, U5-ch53
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.37
Std Dev 11.58
Turn on : 27.2563
Width : 2.623
Height : 10.055
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

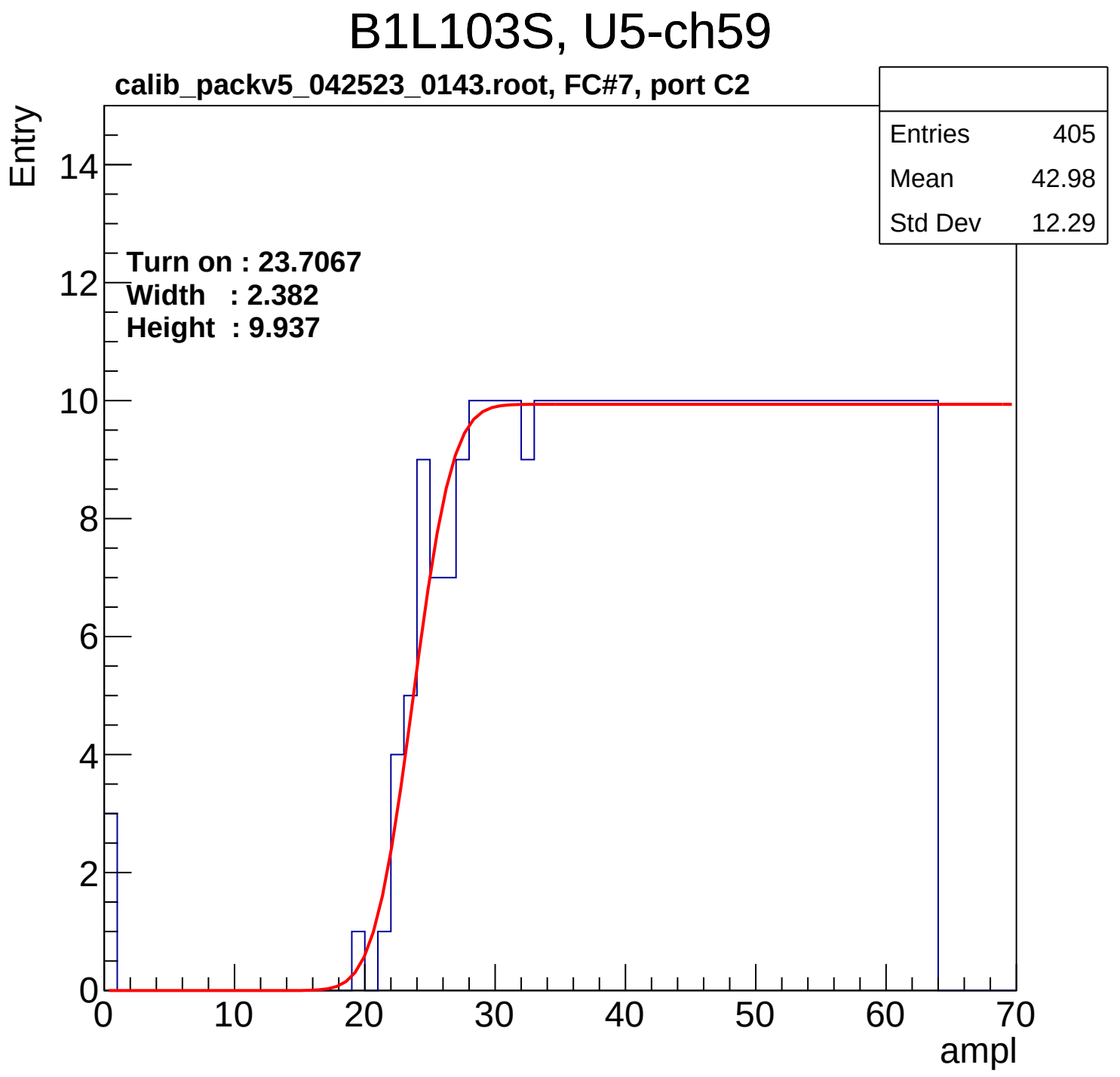

B1L103S, U5-ch54
calib_packv5_042523_0143.root, FC#7, port C2
Entries 398
Mean 43.37
Std Dev 11.92
Turn on : 24.2362
Width : 3.662
Height : 9.950
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

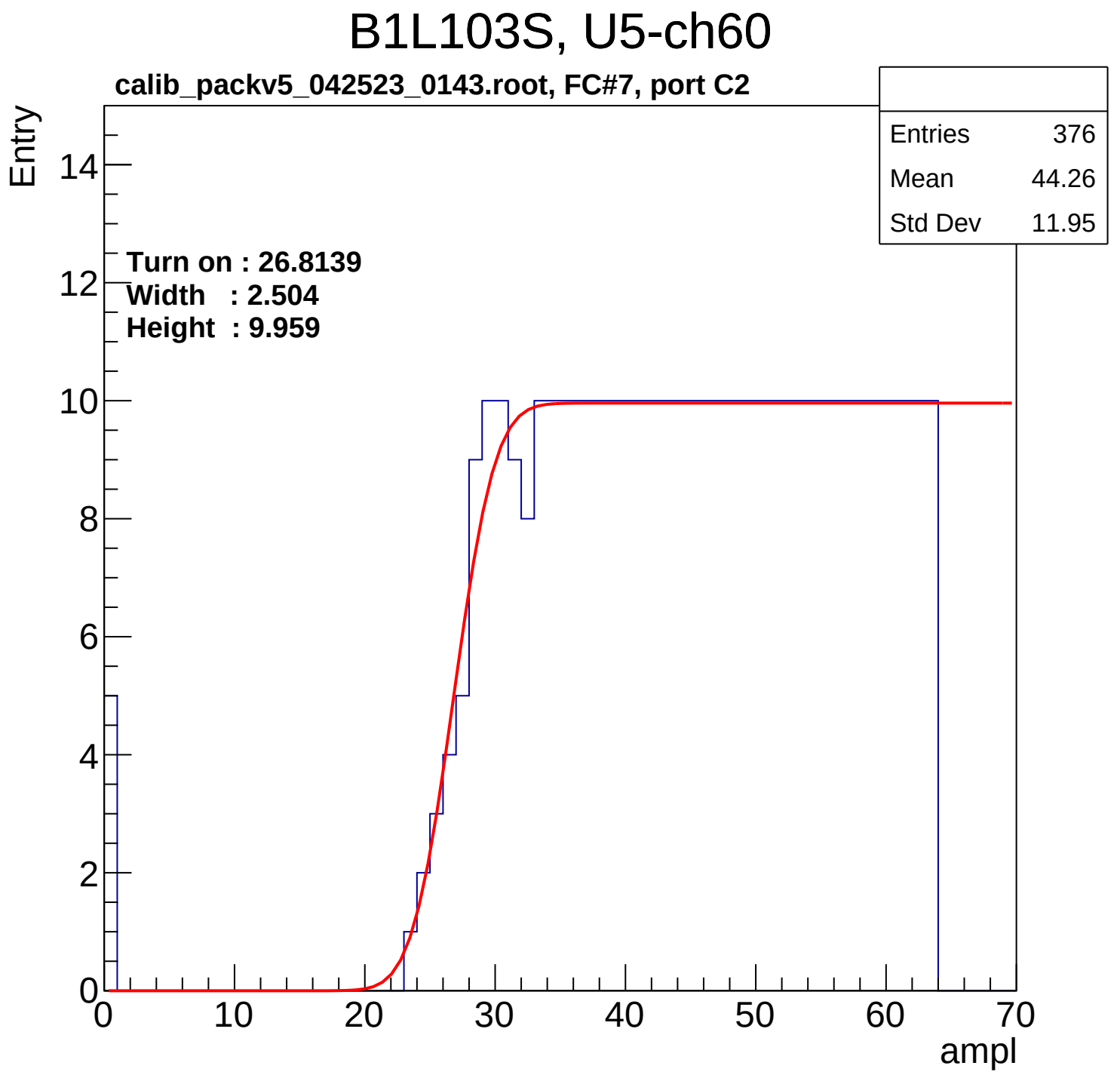

B1L103S, U5-ch55
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.44
Std Dev 11.39
Turn on : 27.1706
Width : 2.950
Height : 10.082
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

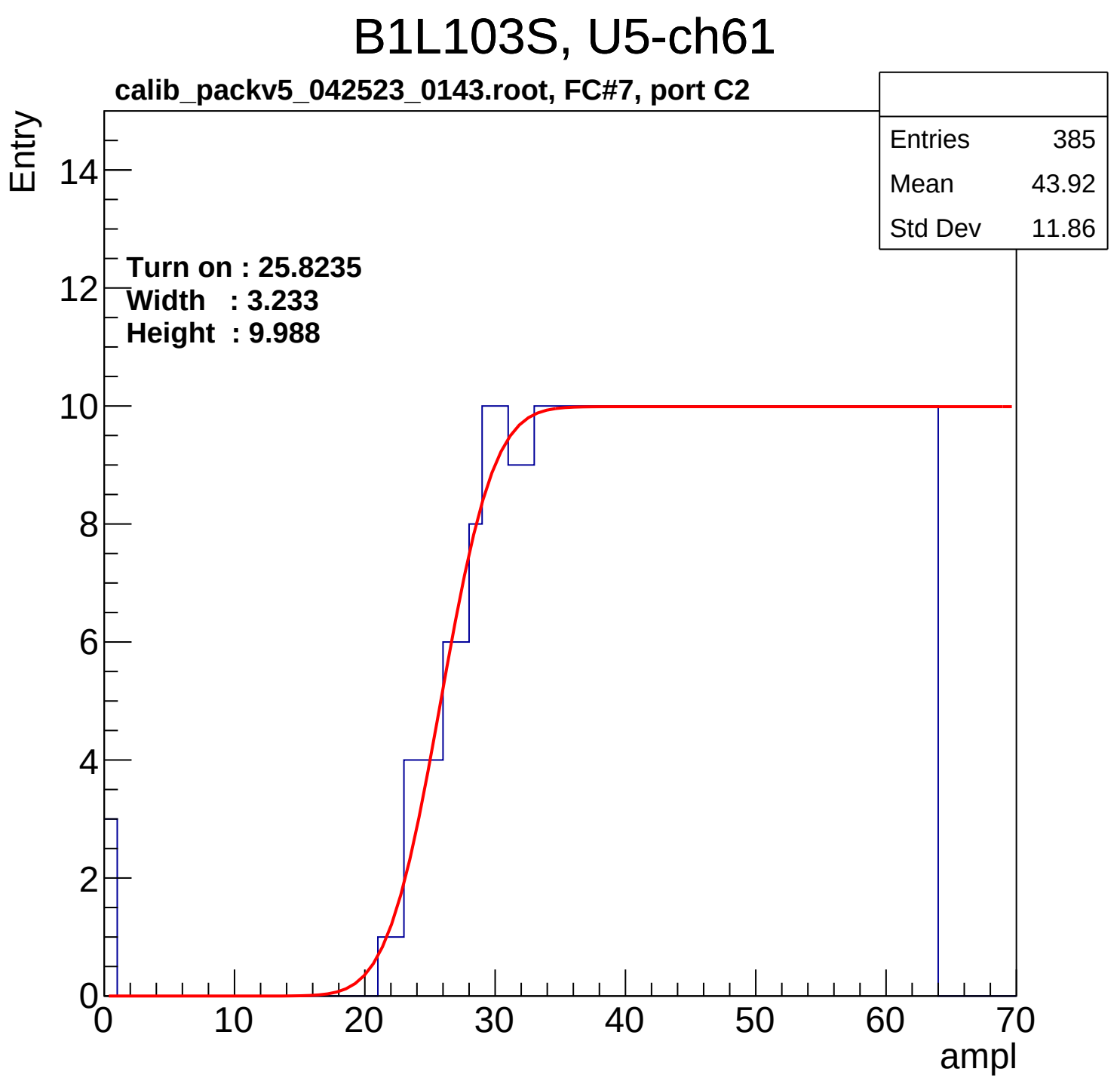

B1L103S, U5-ch56
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.69
Std Dev 11.31
Turn on : 27.1985
Width : 3.766
Height : 10.060
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

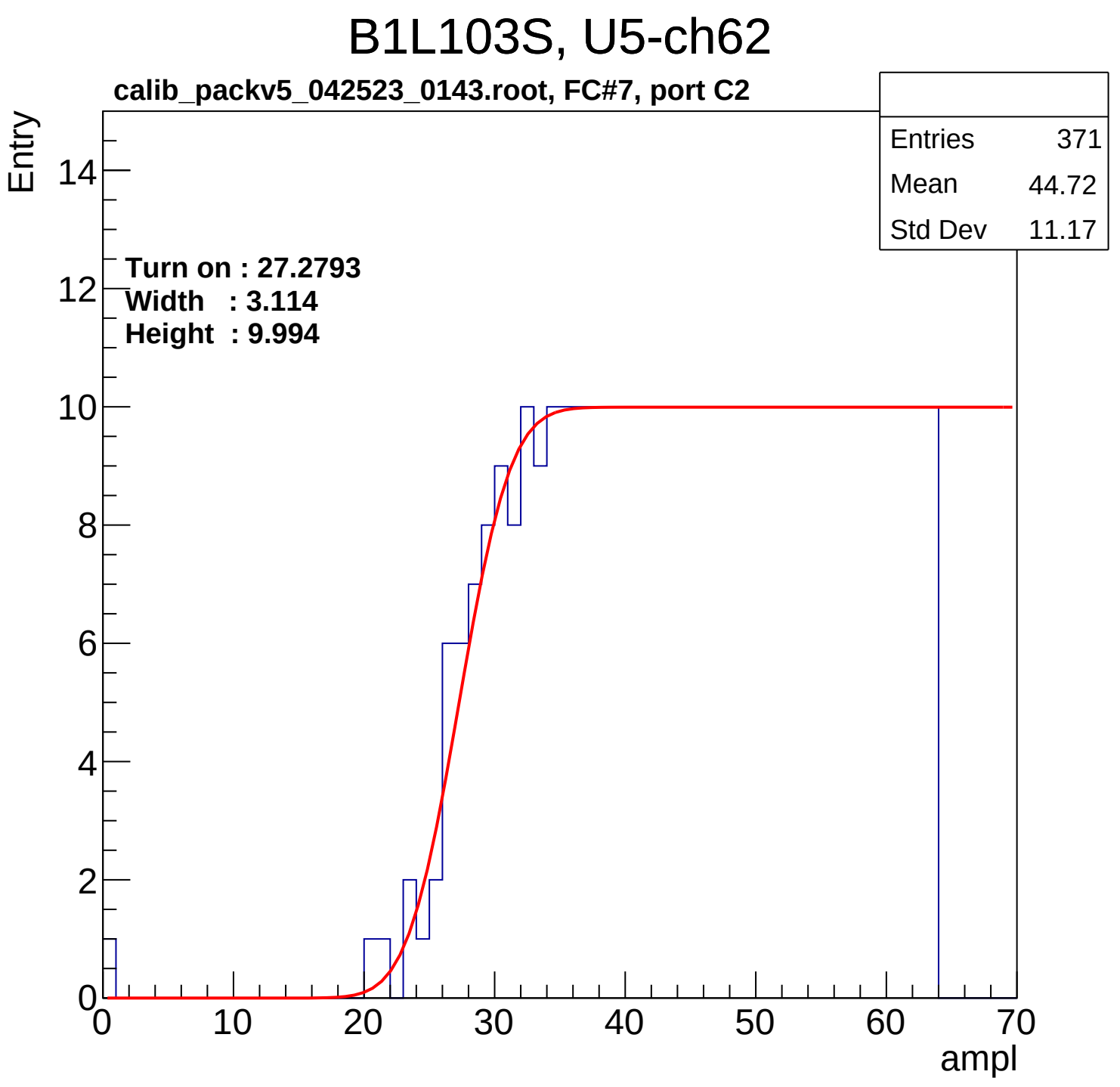

B1L103S, U5-ch57
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.53
Std Dev 11.4
Turn on : 28.1728
Width : 3.440
Height : 10.105
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

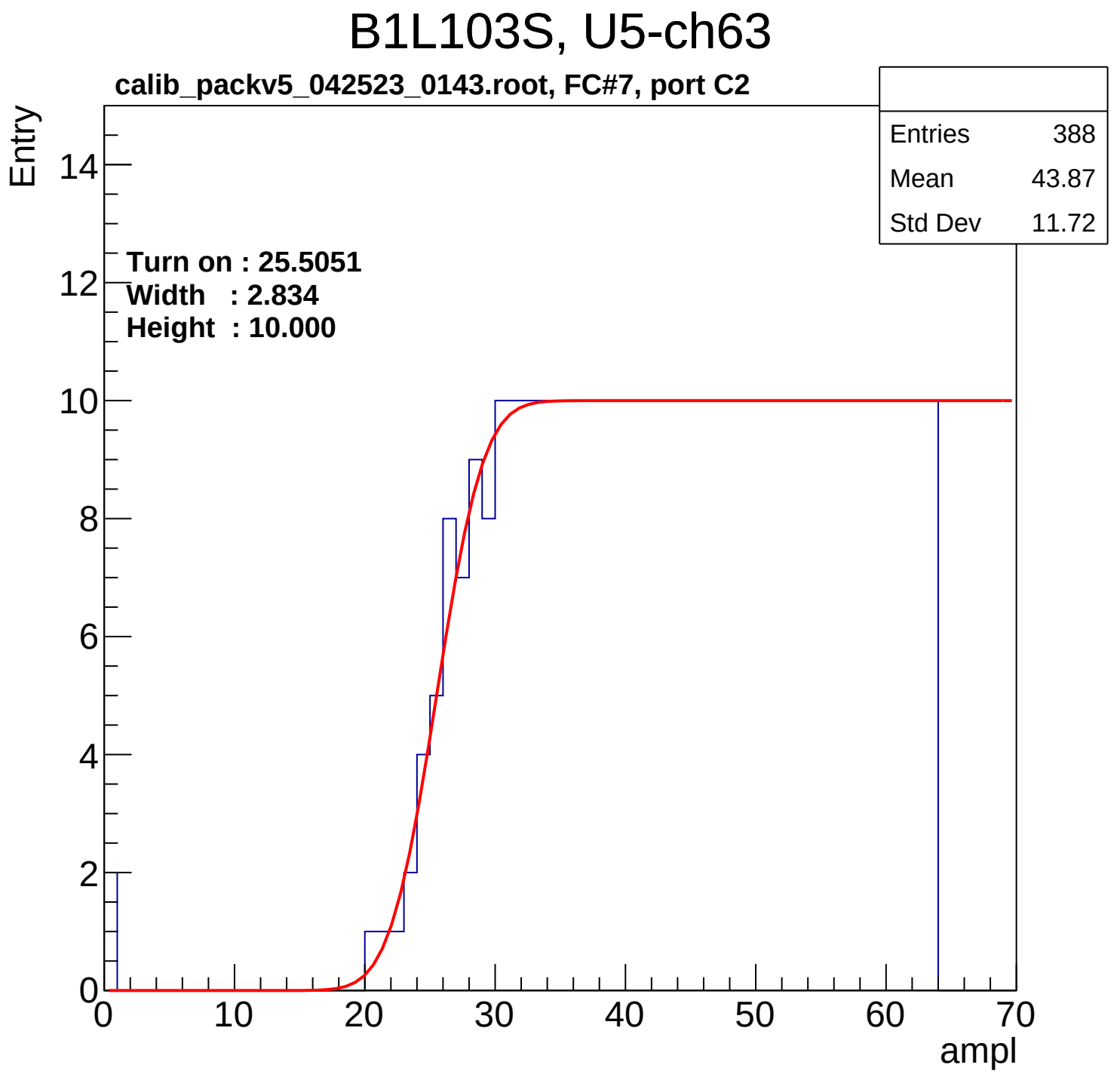

B1L103S, U5-ch58
calib_packv5_042523_0143.root, FC#7, port C2
Entries 393
Mean 43.46
Std Dev 12.24
Turn on : 25.4134
Width : 3.681
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

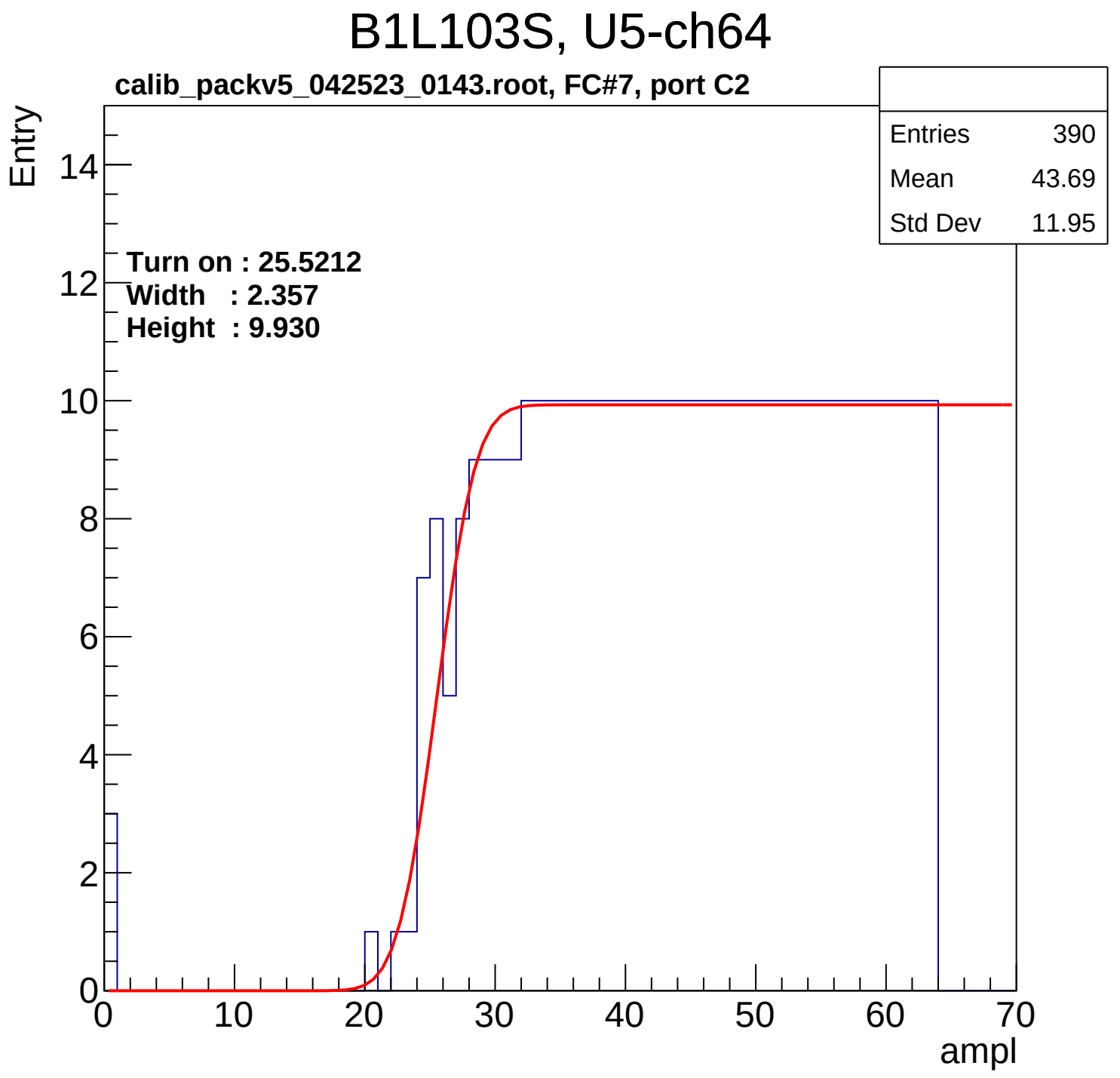

B1L103S, U5-ch59
calib_packv5_042523_0143.root, FC#7, port C2
Entries 405
Mean 42.98
Std Dev 12.29
Turn on : 23.7067
Width : 2.382
Height : 9.937
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

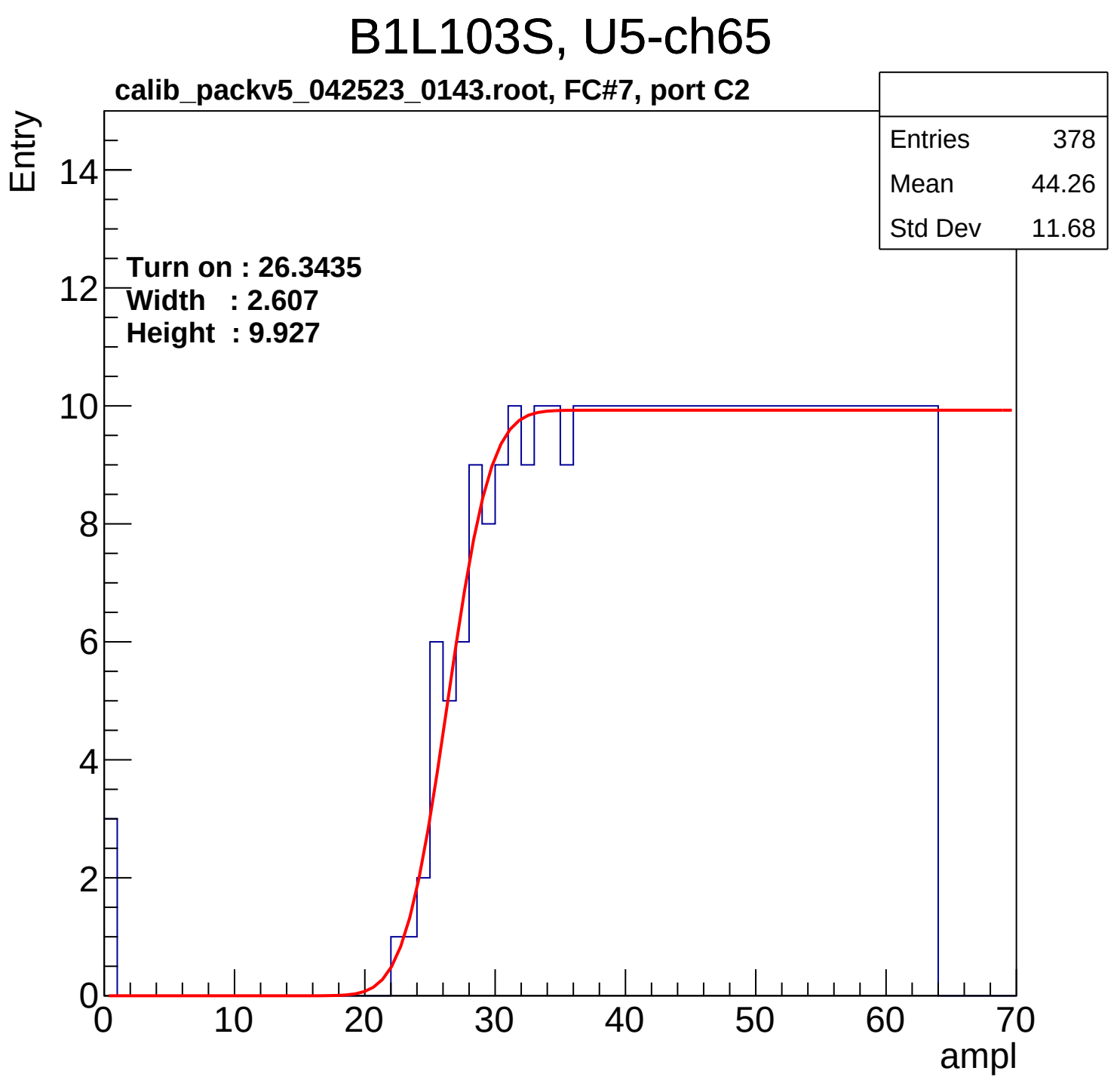

B1L103S, U5-ch60
calib_packv5_042523_0143.root, FC#7, port C2
Entries 376
Mean 44.26
Std Dev 11.95
Turn on : 26.8139
Width : 2.504
Height : 9.959
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

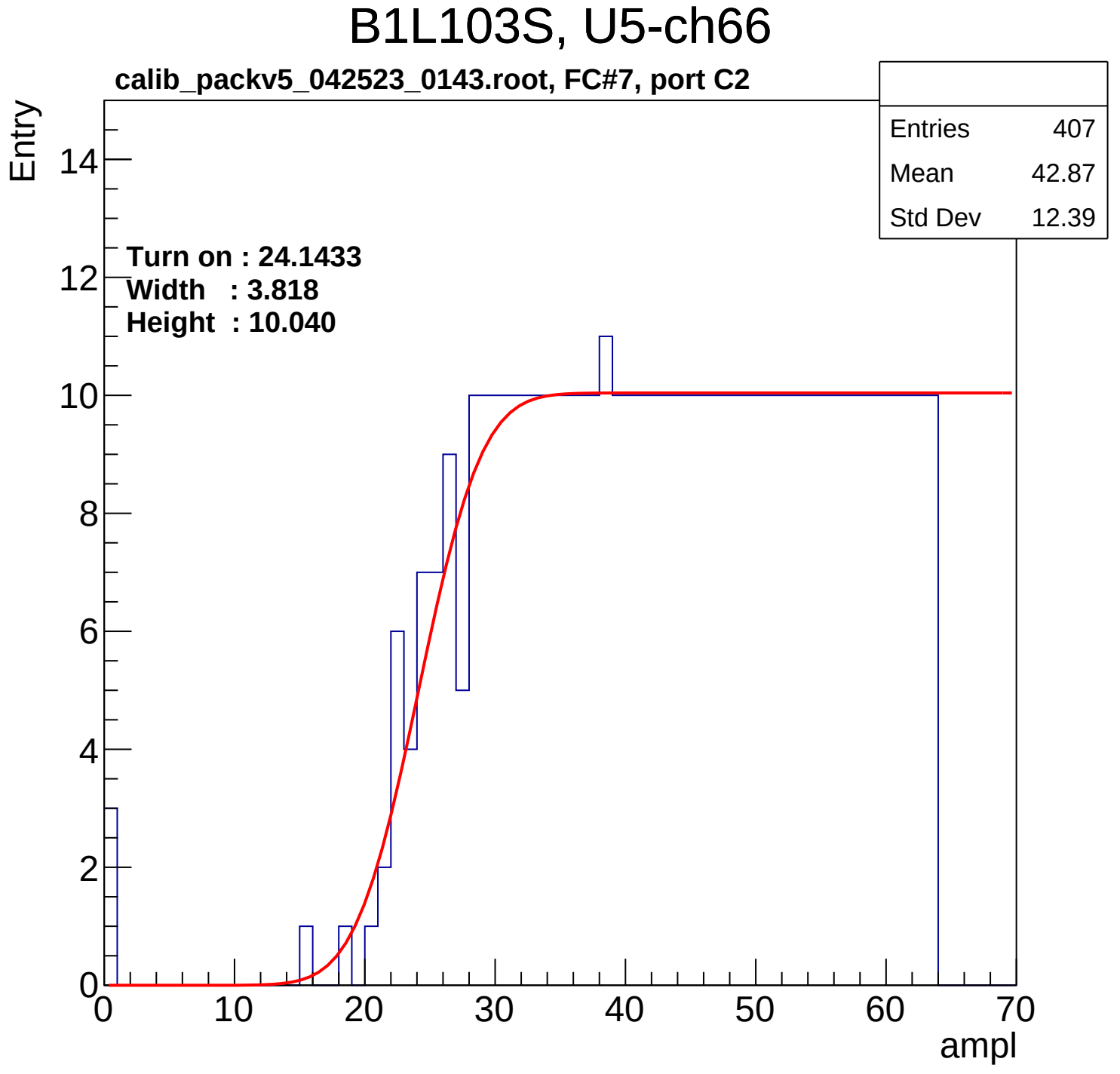

B1L103S, U5-ch61
calib_packv5_042523_0143.root, FC#7, port C2
Entries 385
Mean 43.92
Std Dev 11.86
Turn on : 25.8235
Width : 3.233
Height : 9.988
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

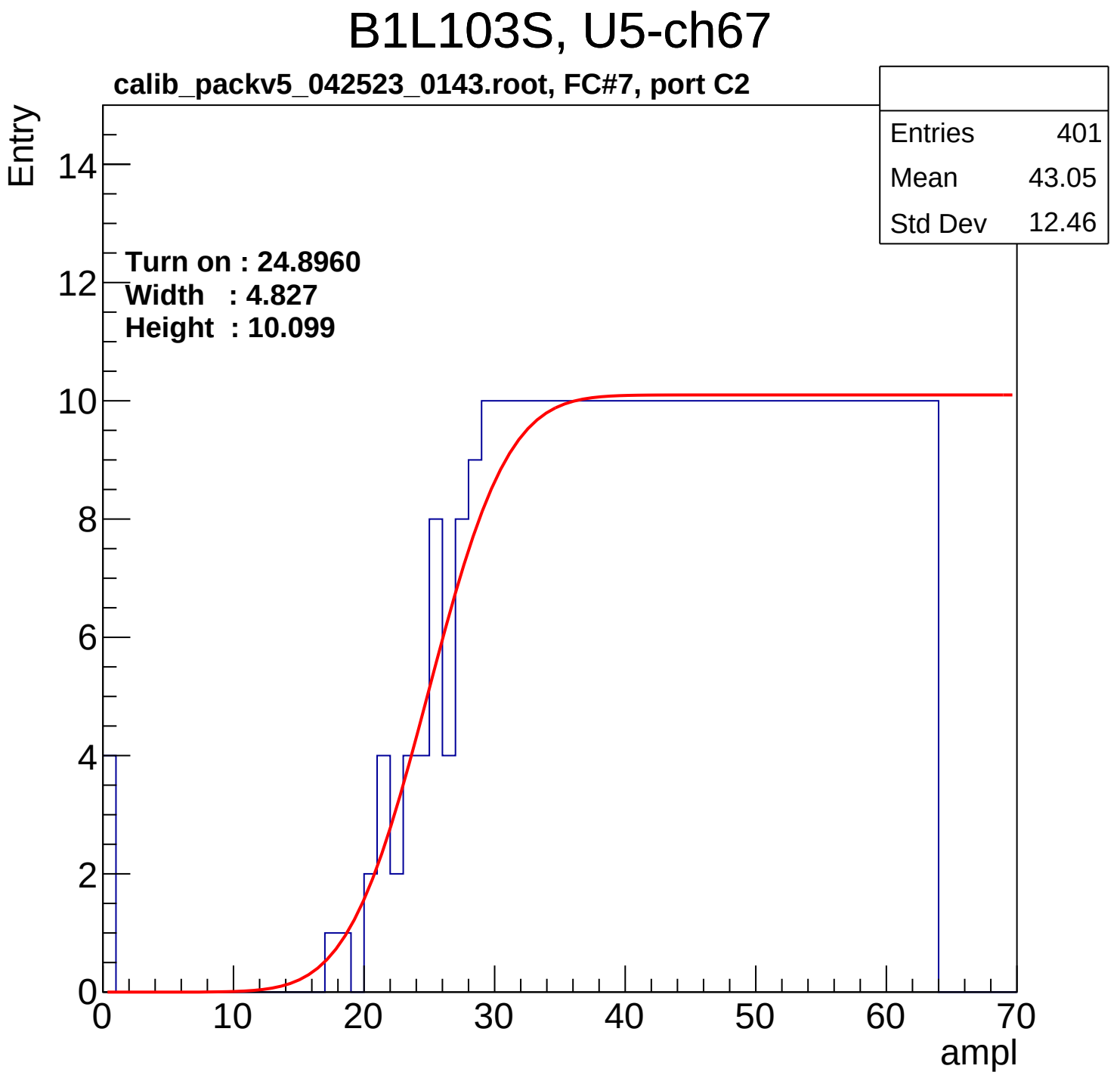

B1L103S, U5-ch62
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.72
Std Dev 11.17
Turn on : 27.2793
Width : 3.114
Height : 9.994
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

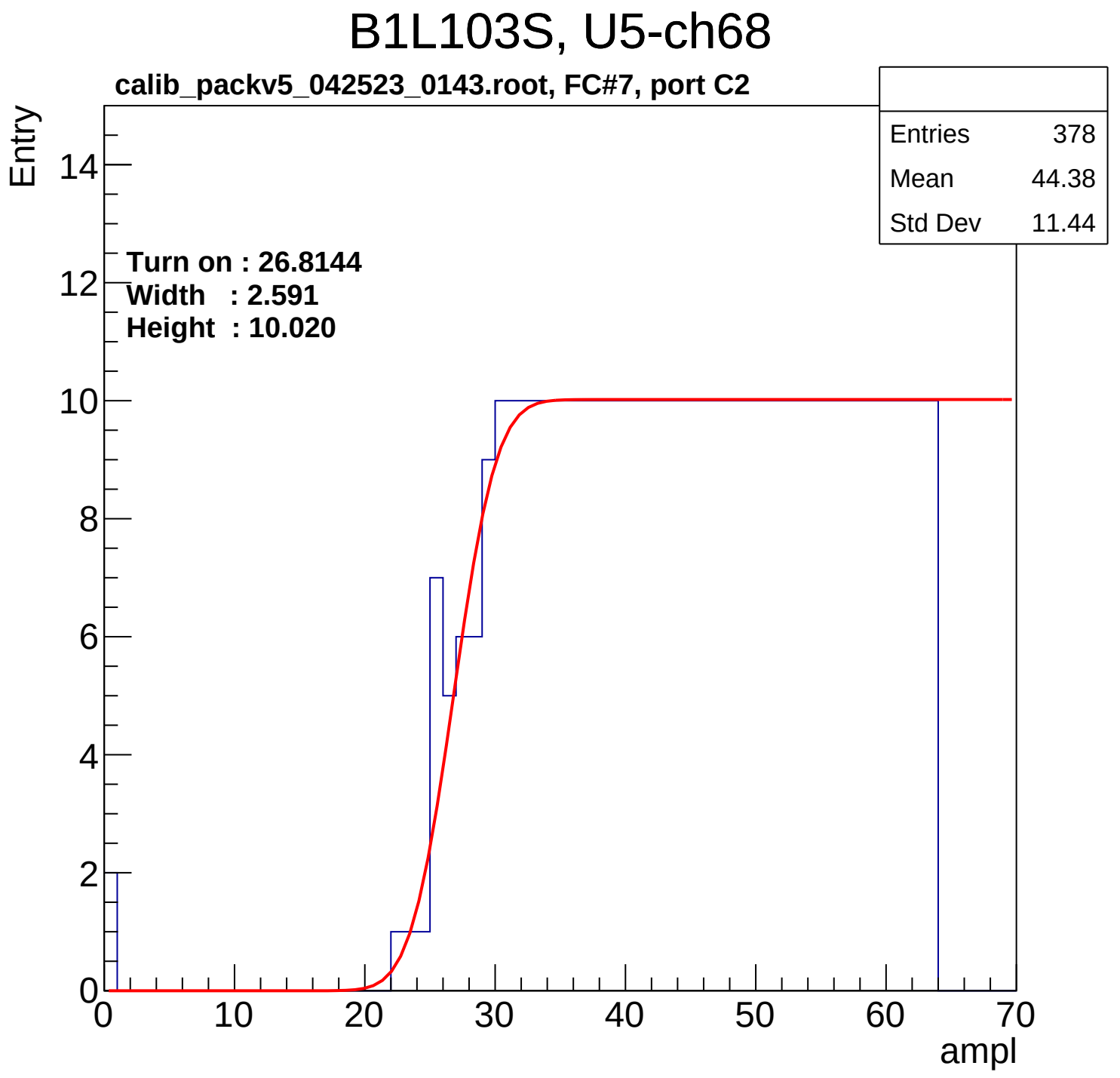

B1L103S, U5-ch63
calib_packv5_042523_0143.root, FC#7, port C2
Entries 388
Mean 43.87
Std Dev 11.72
Turn on : 25.5051
Width : 2.834
Height : 10.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

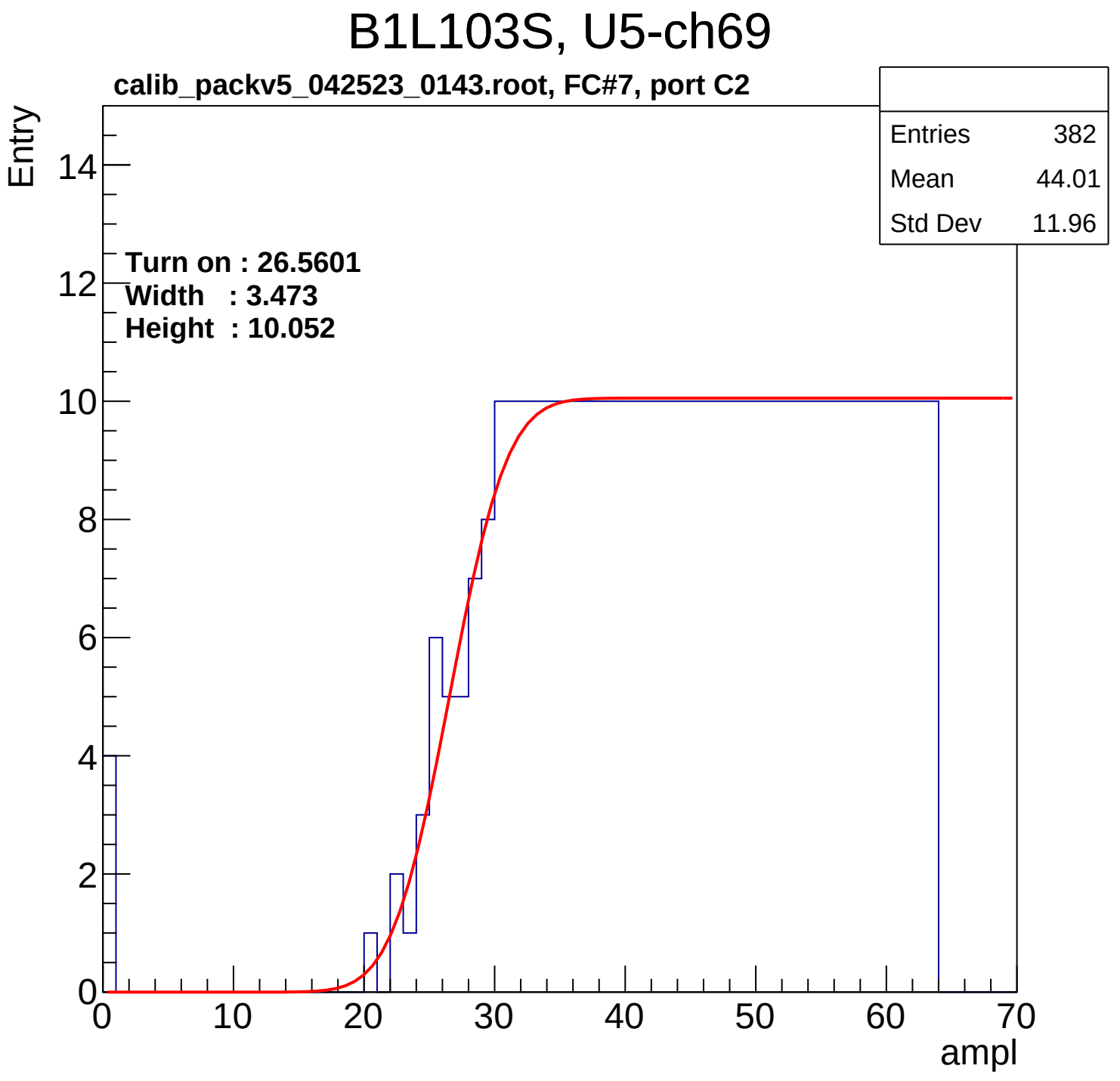

B1L103S, U5-ch64
calib_packv5_042523_0143.root, FC#7, port C2
Entries 390
Mean 43.69
Std Dev 11.95
Turn on : 25.5212
Width : 2.357
Height : 9.930
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

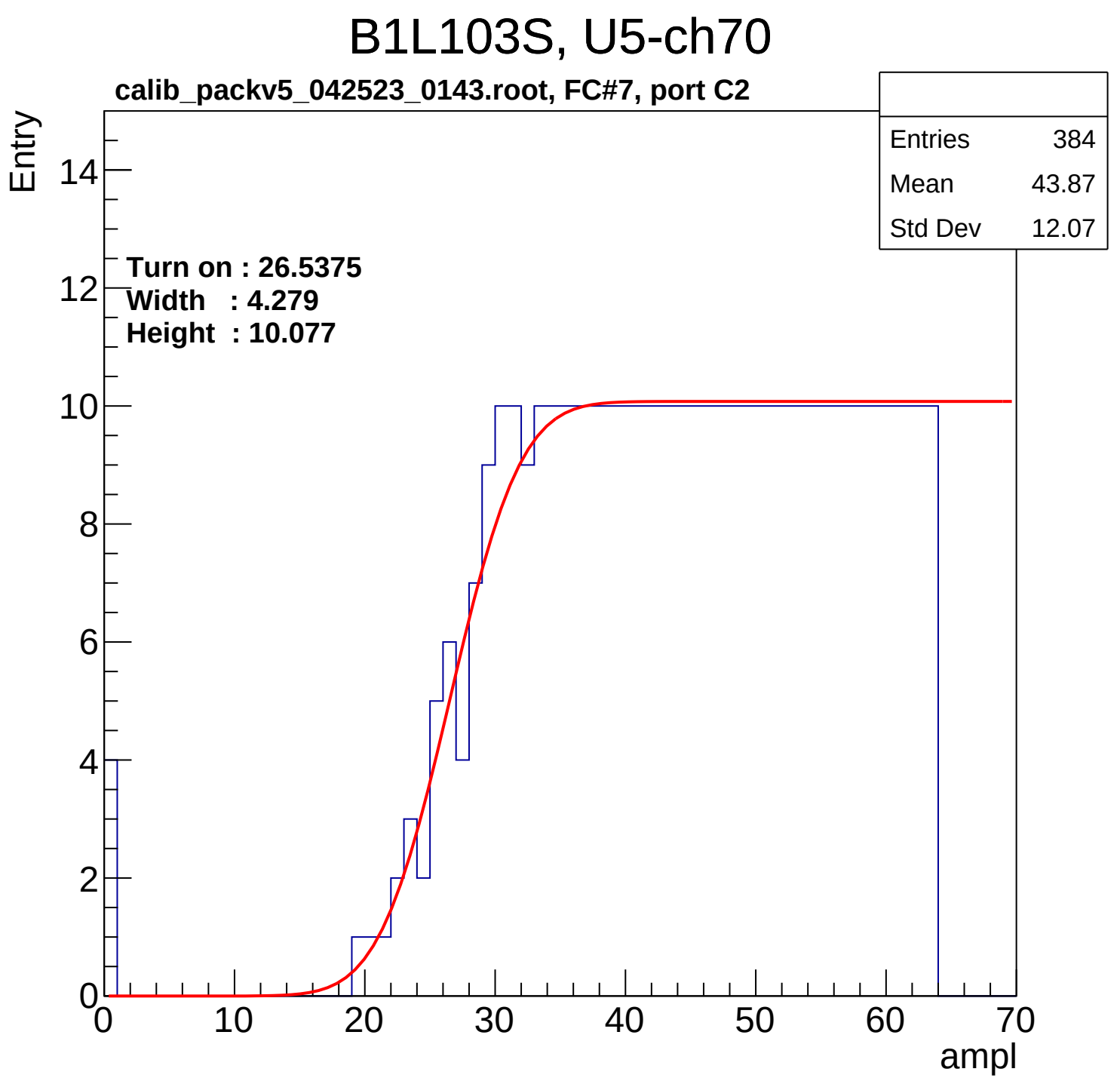

B1L103S, U5-ch65
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.26
Std Dev 11.68
Turn on : 26.3435
Width : 2.607
Height : 9.927
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

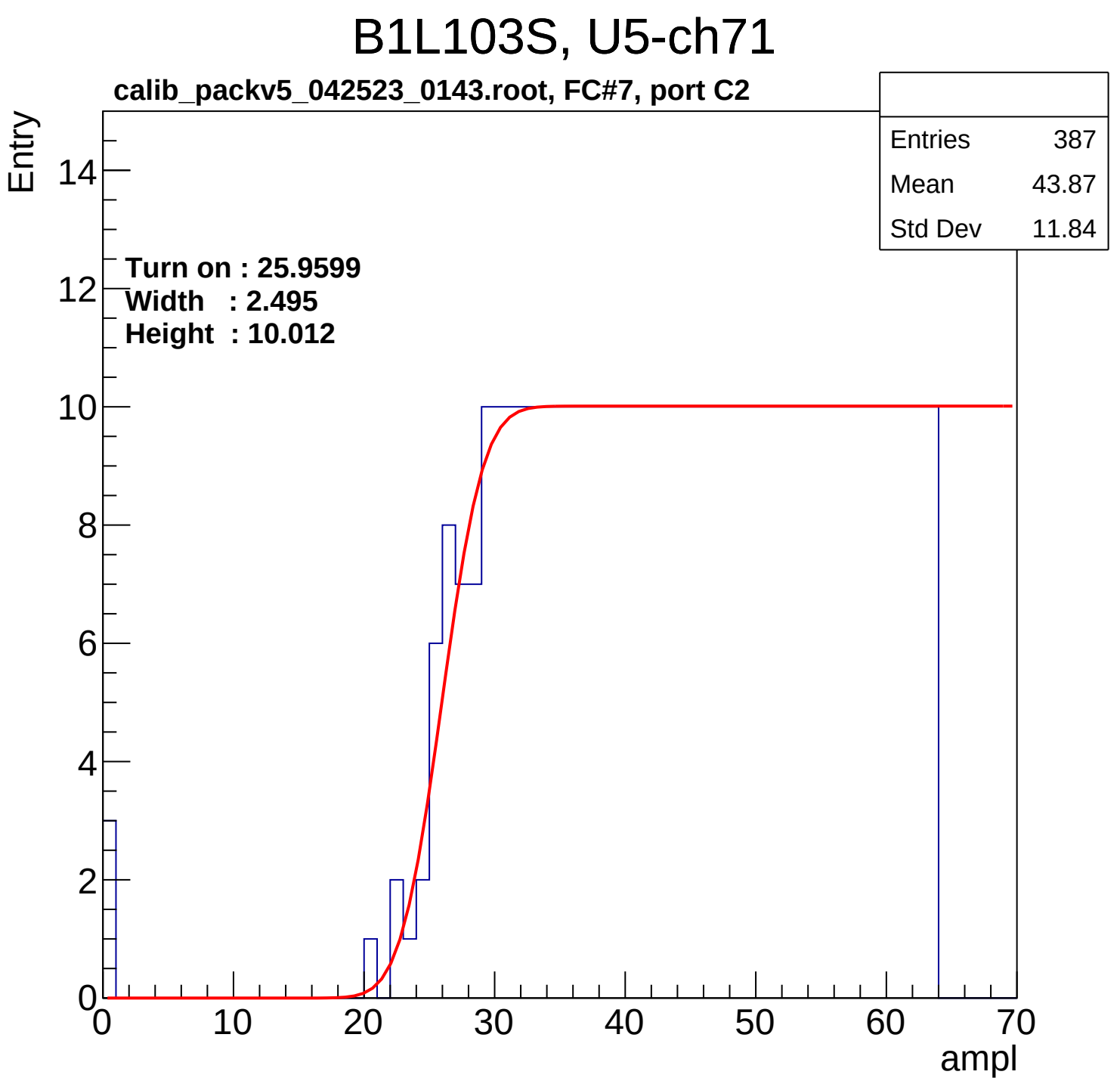

B1L103S, U5-ch66
calib_packv5_042523_0143.root, FC#7, port C2
Entries 407
Mean 42.87
Std Dev 12.39
Turn on : 24.1433
Width : 3.818
Height : 10.040
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

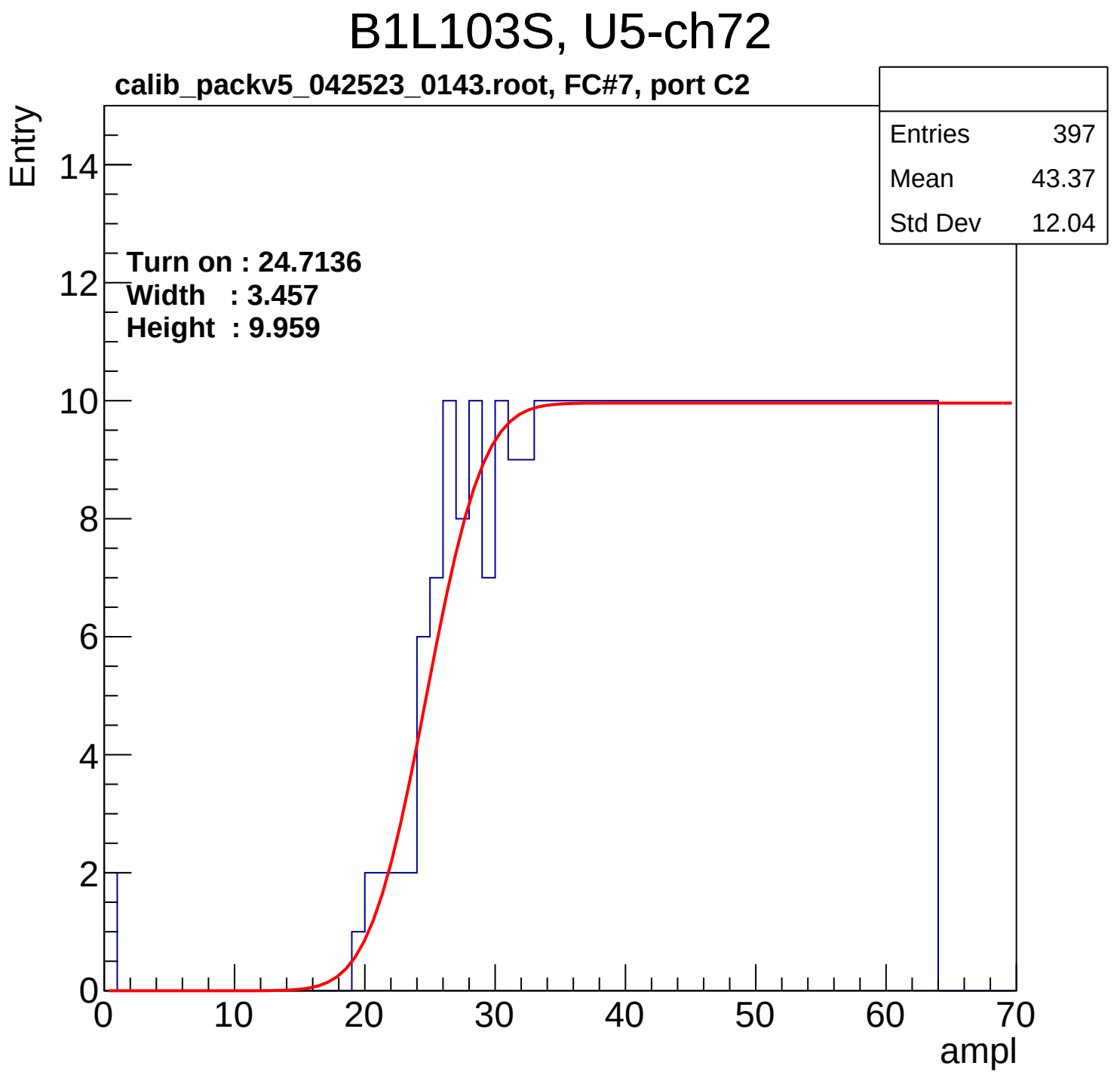

B1L103S, U5-ch67
calib_packv5_042523_0143.root, FC#7, port C2
Entries 401
Mean 43.05
Std Dev 12.46
Turn on : 24.8960
Width : 4.827
Height : 10.099
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

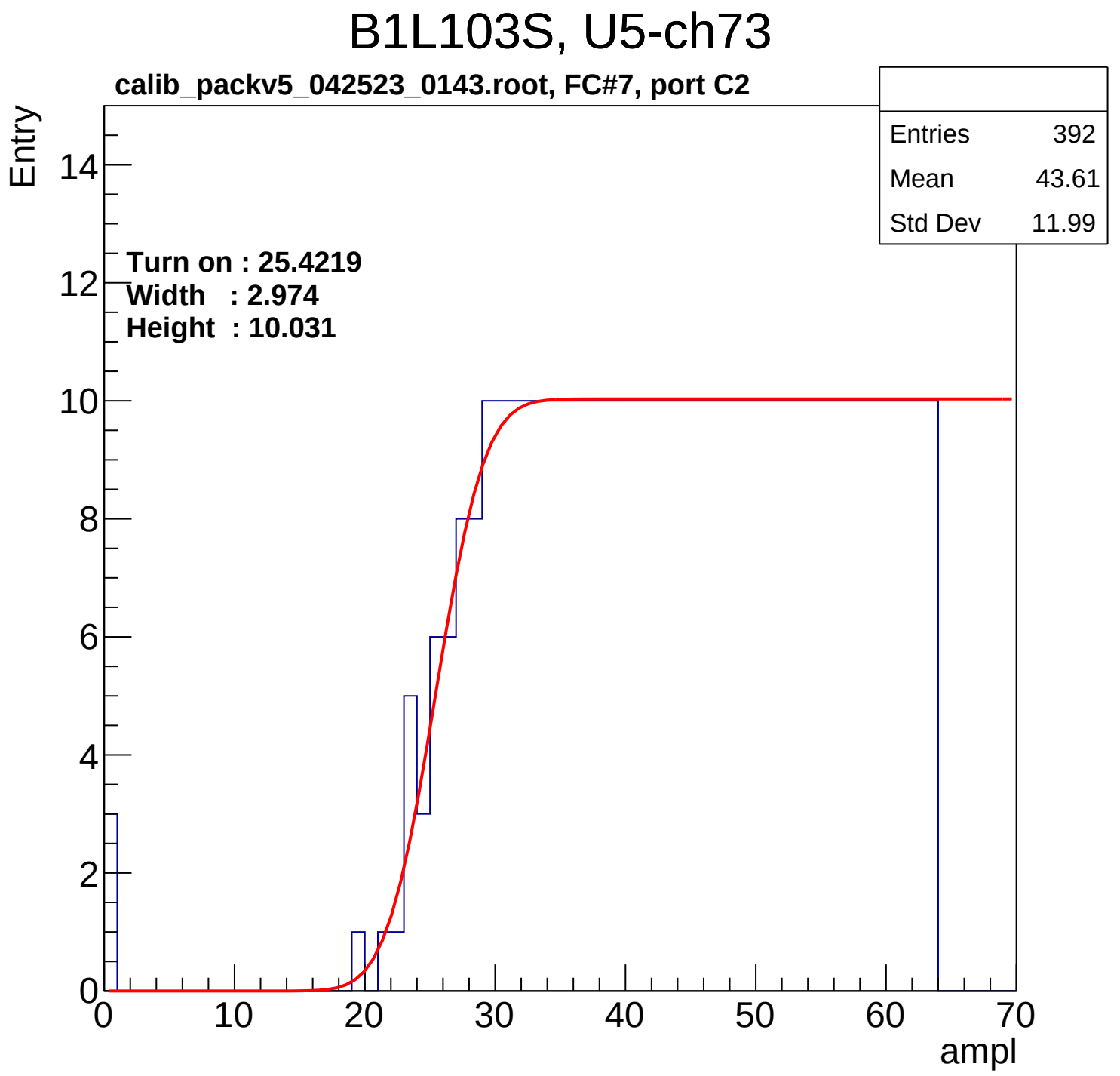

B1L103S, U5-ch68
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.38
Std Dev 11.44
Turn on : 26.8144
Width : 2.591
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

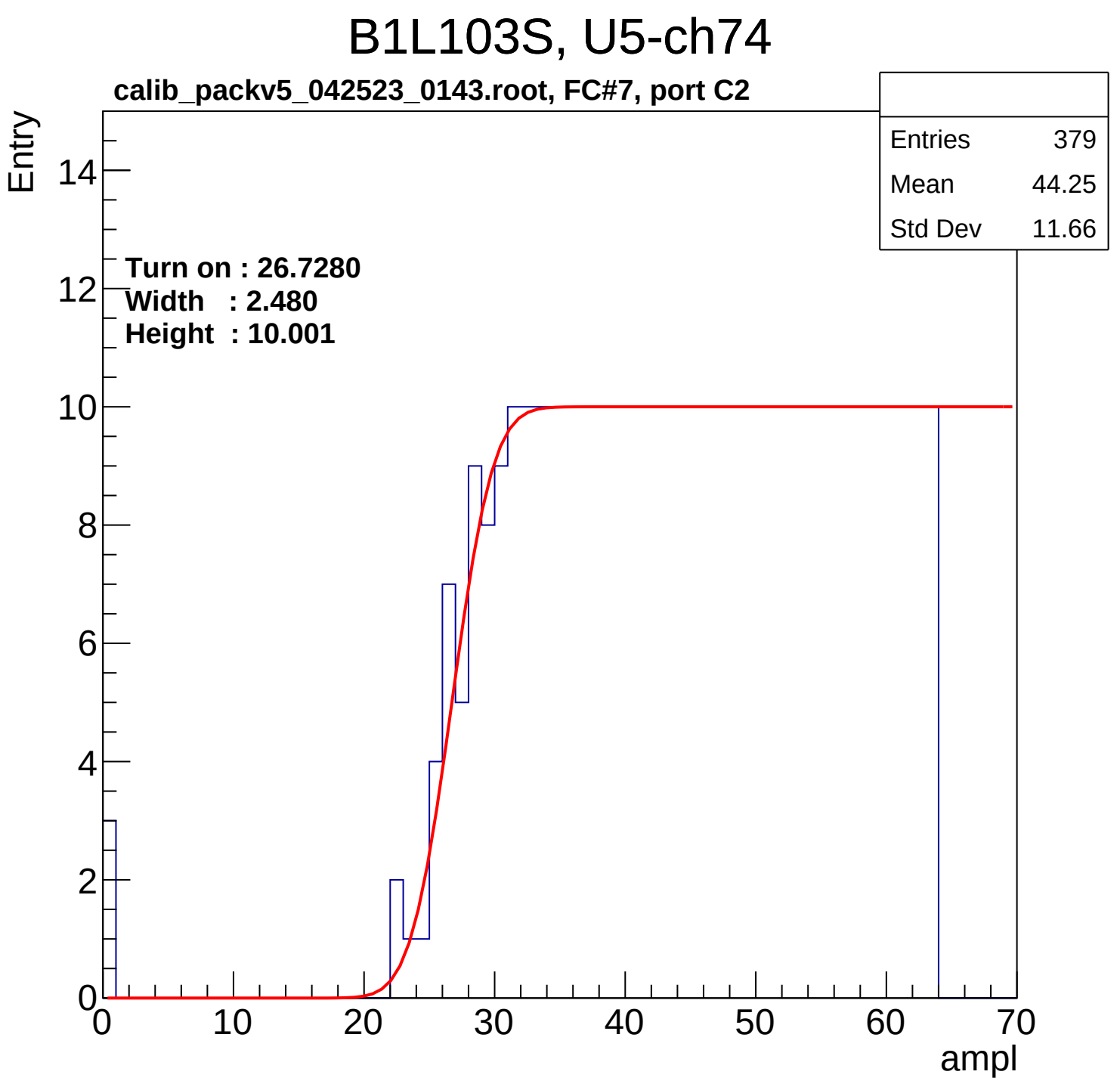

B1L103S, U5-ch69
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 44.01
Std Dev 11.96
Turn on : 26.5601
Width : 3.473
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

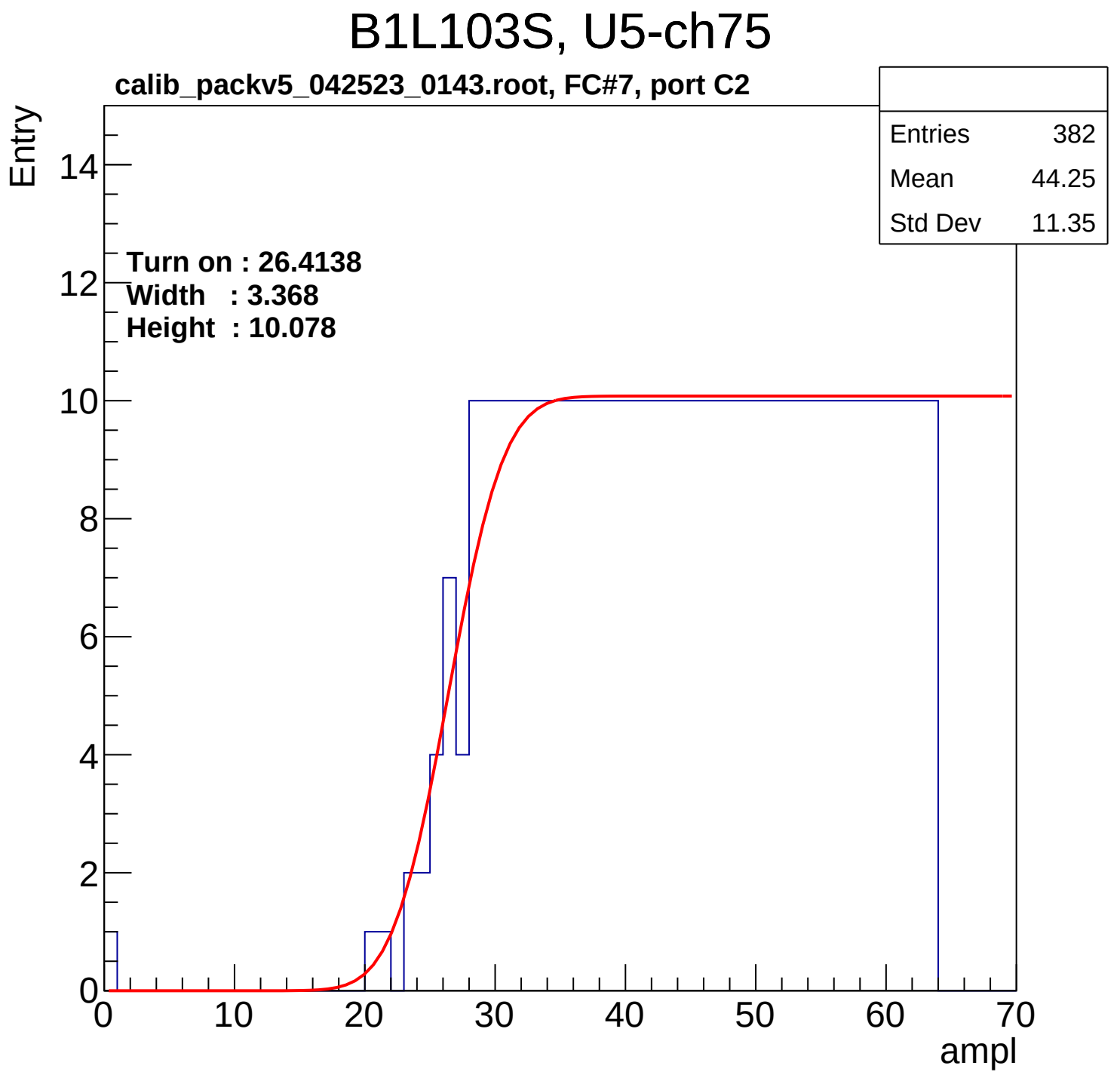

B1L103S, U5-ch70
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 43.87
Std Dev 12.07
Turn on : 26.5375
Width : 4.279
Height : 10.077
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

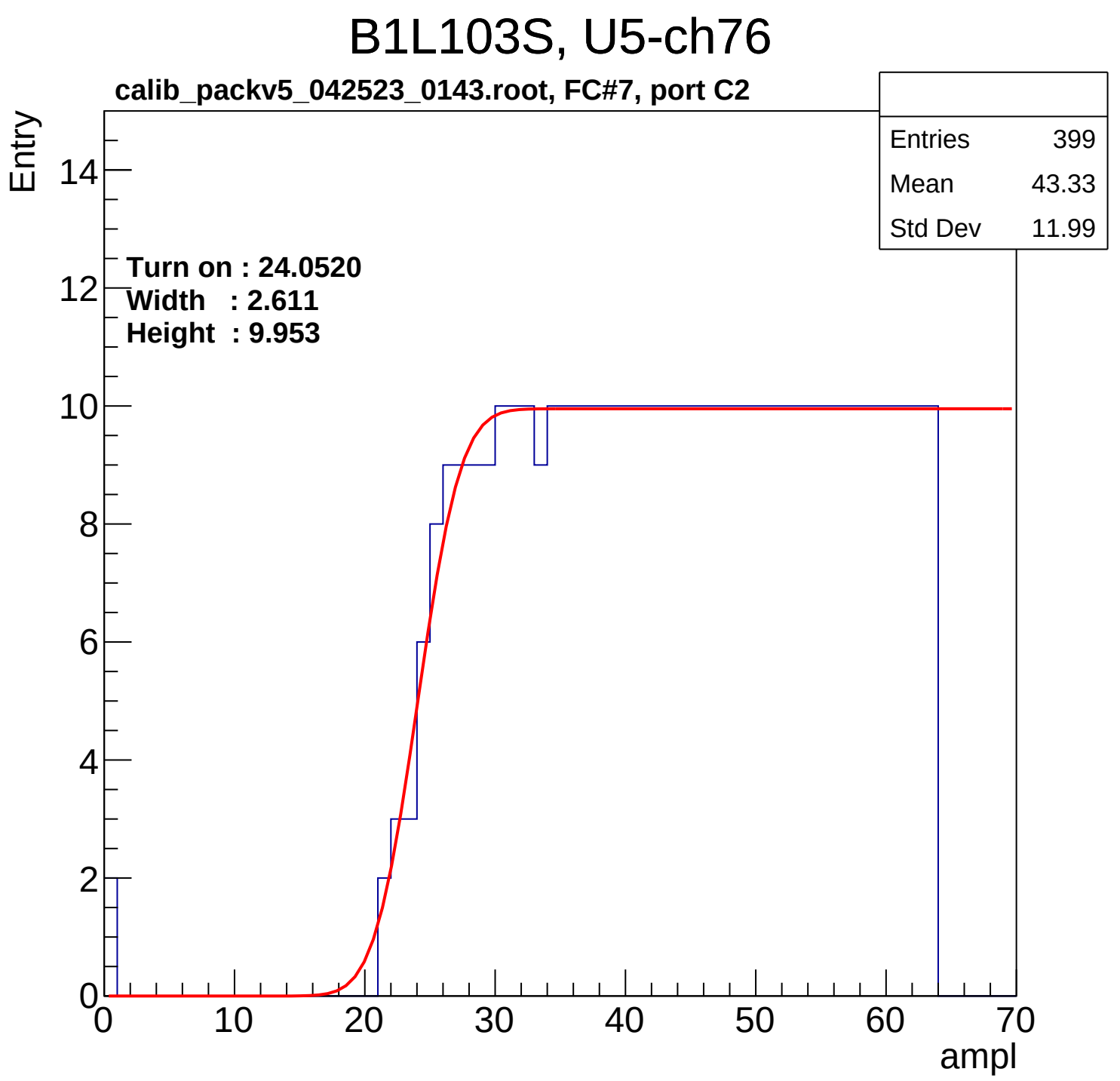

B1L103S, U5-ch71
calib_packv5_042523_0143.root, FC#7, port C2
Entries 387
Mean 43.87
Std Dev 11.84
Turn on : 25.9599
Width : 2.495
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

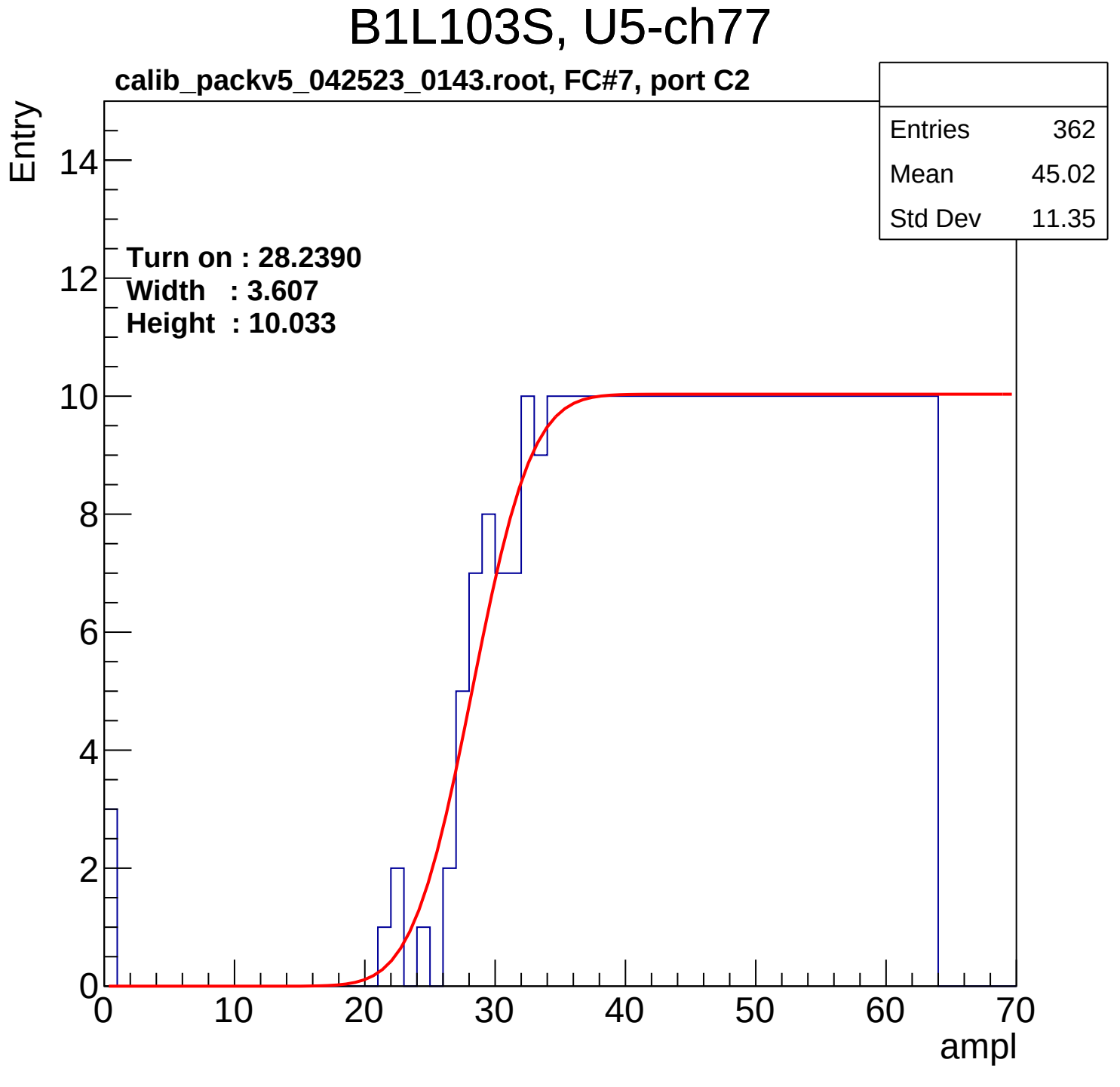

B1L103S, U5-ch72
calib_packv5_042523_0143.root, FC#7, port C2
Entries 397
Mean 43.37
Std Dev 12.04
Turn on : 24.7136
Width : 3.457
Height : 9.959
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

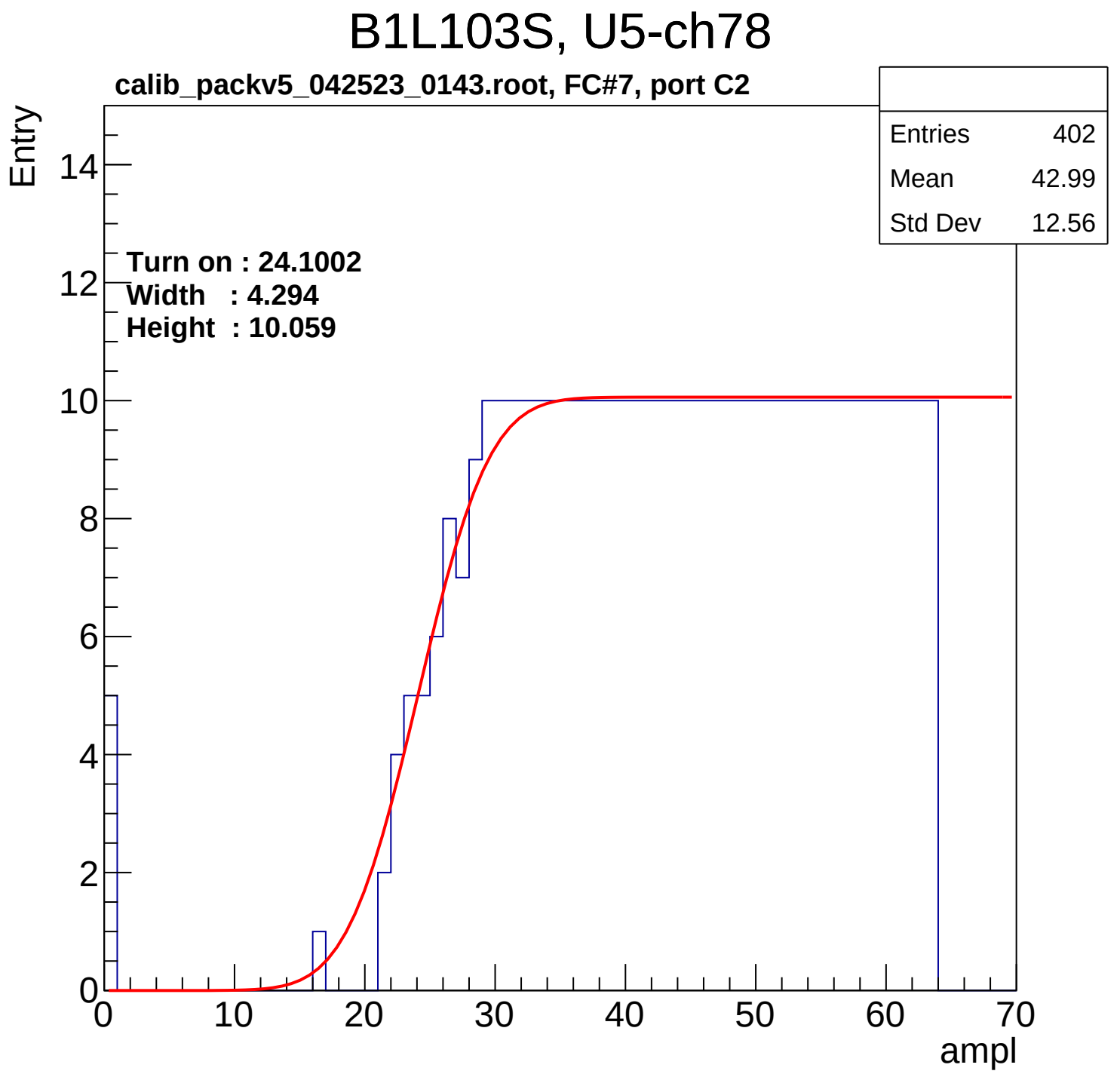

B1L103S, U5-ch73
calib_packv5_042523_0143.root, FC#7, port C2
Entries 392
Mean 43.61
Std Dev 11.99
Turn on : 25.4219
Width : 2.974
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

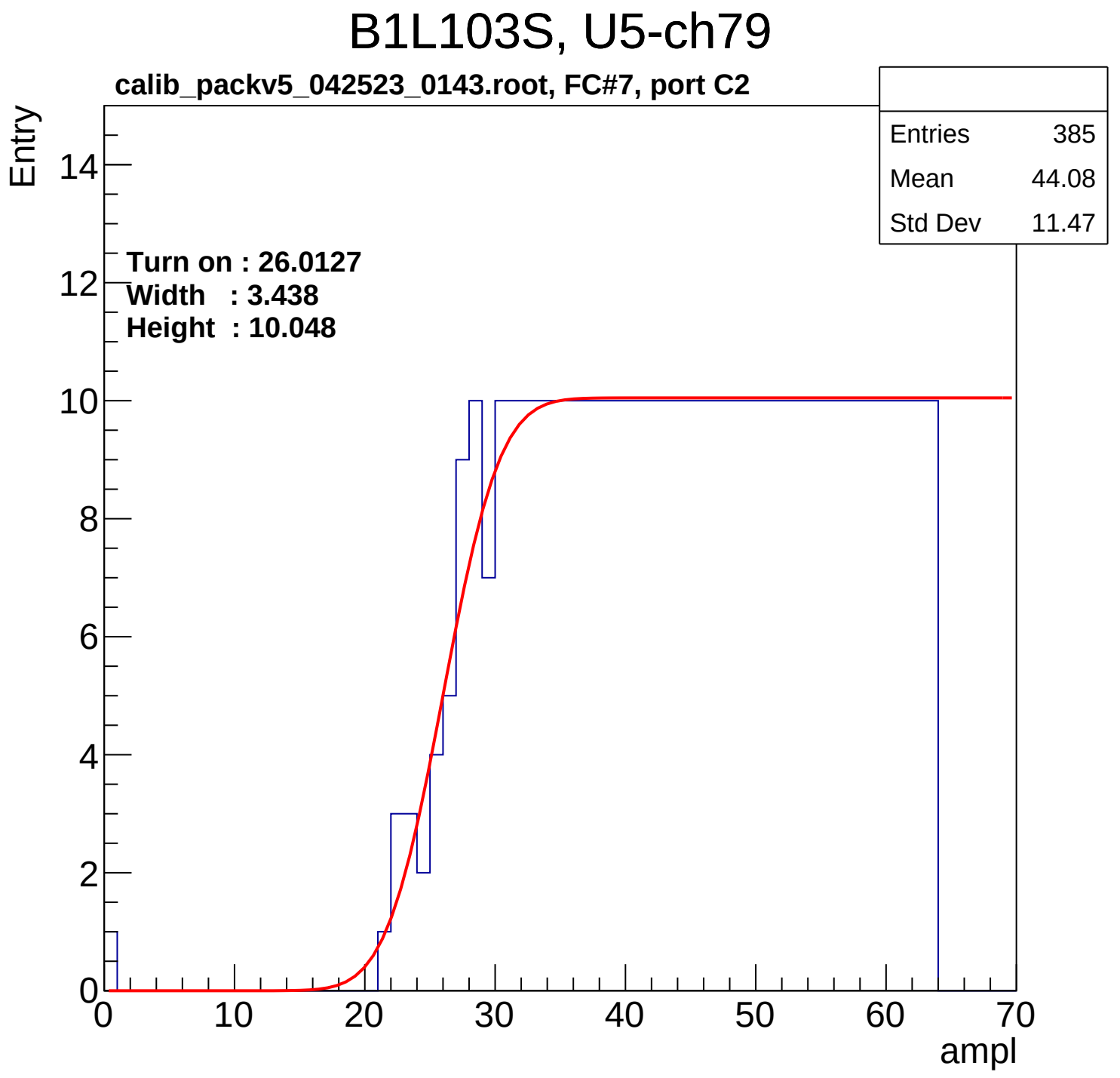

B1L103S, U5-ch74
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.25
Std Dev 11.66
Turn on : 26.7280
Width : 2.480
Height : 10.001
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

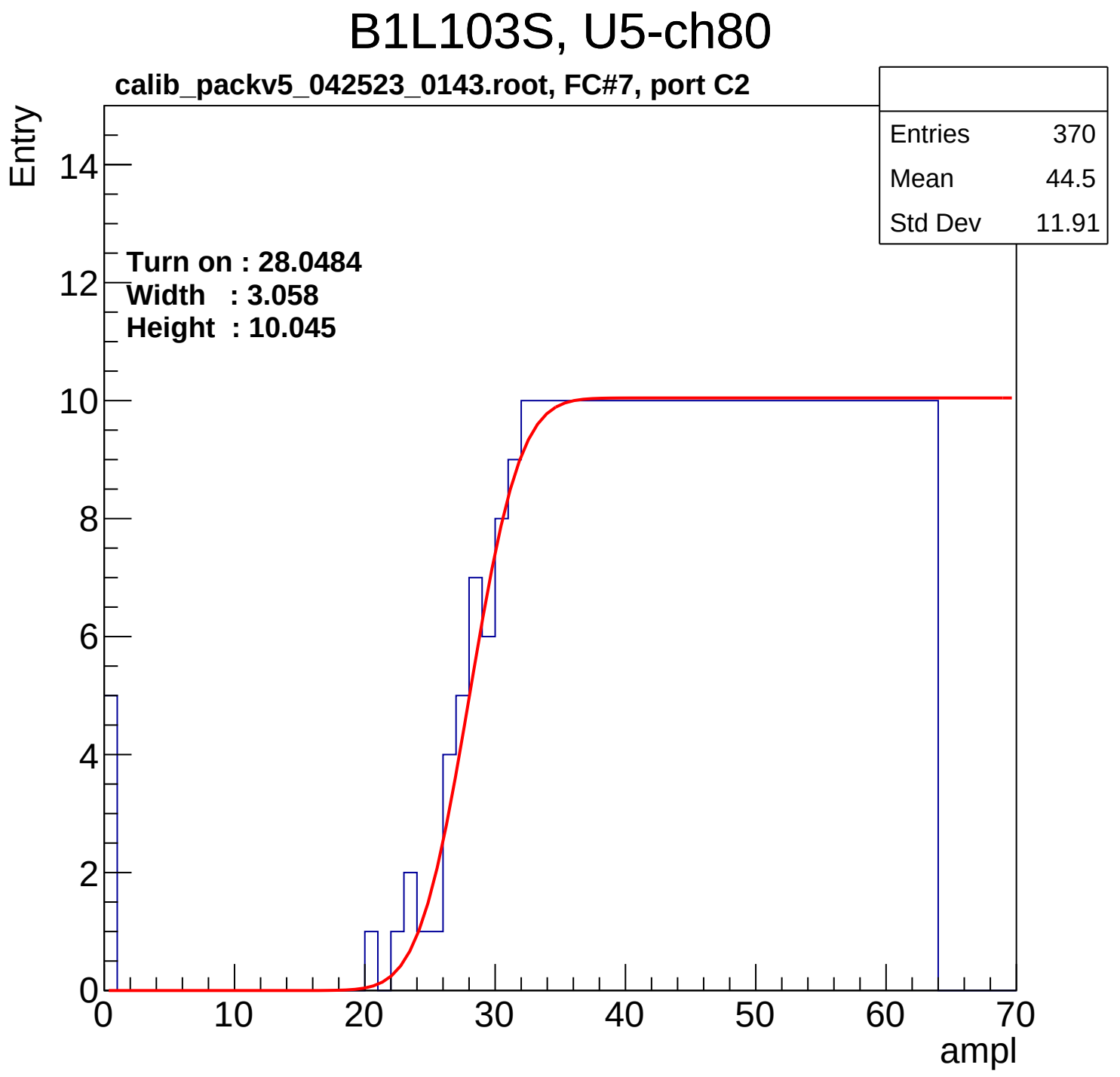

B1L103S, U5-ch75
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 44.25
Std Dev 11.35
Turn on : 26.4138
Width : 3.368
Height : 10.078
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

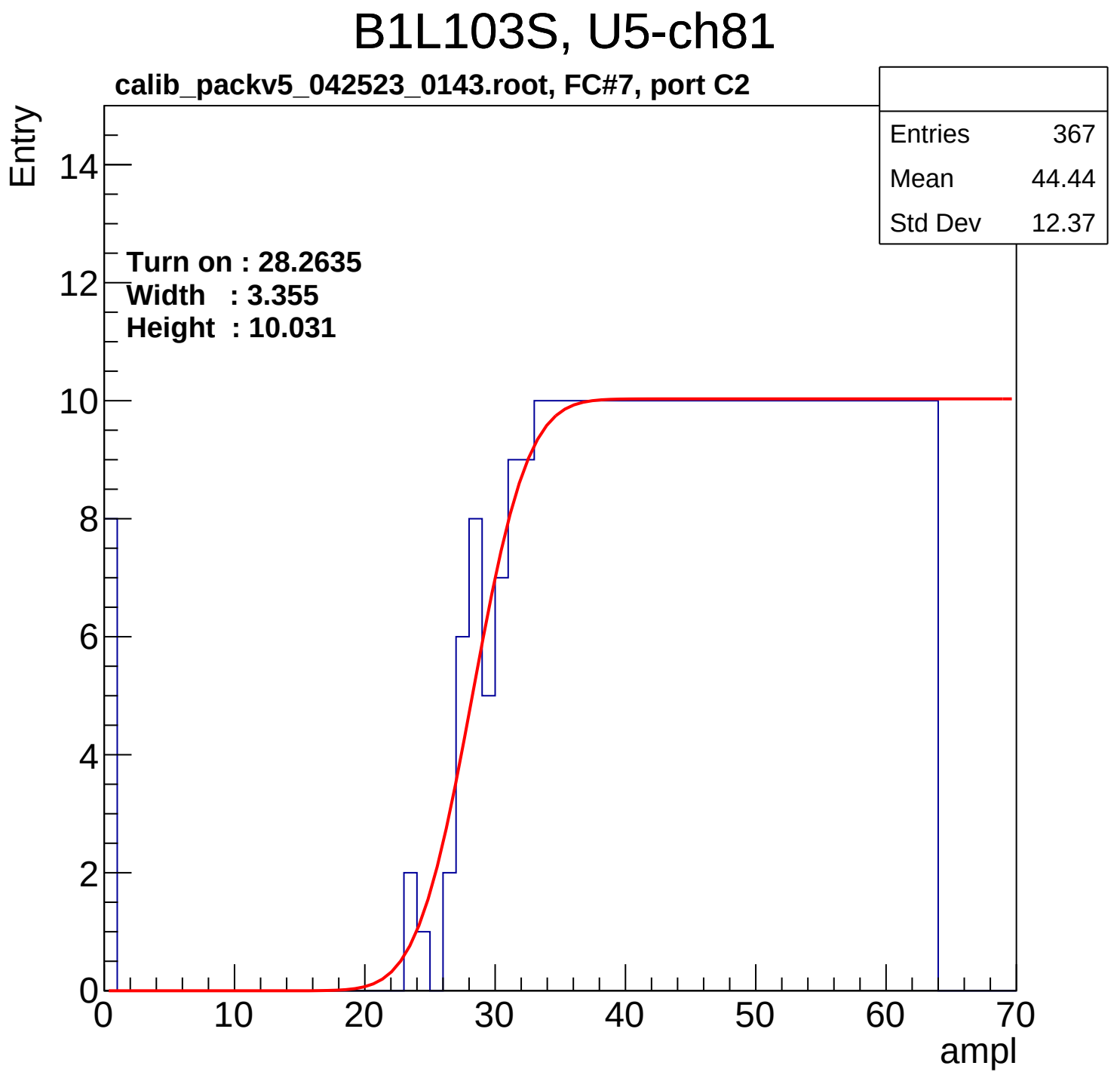

B1L103S, U5-ch76
calib_packv5_042523_0143.root, FC#7, port C2
Entries 399
Mean 43.33
Std Dev 11.99
Turn on : 24.0520
Width : 2.611
Height : 9.953
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

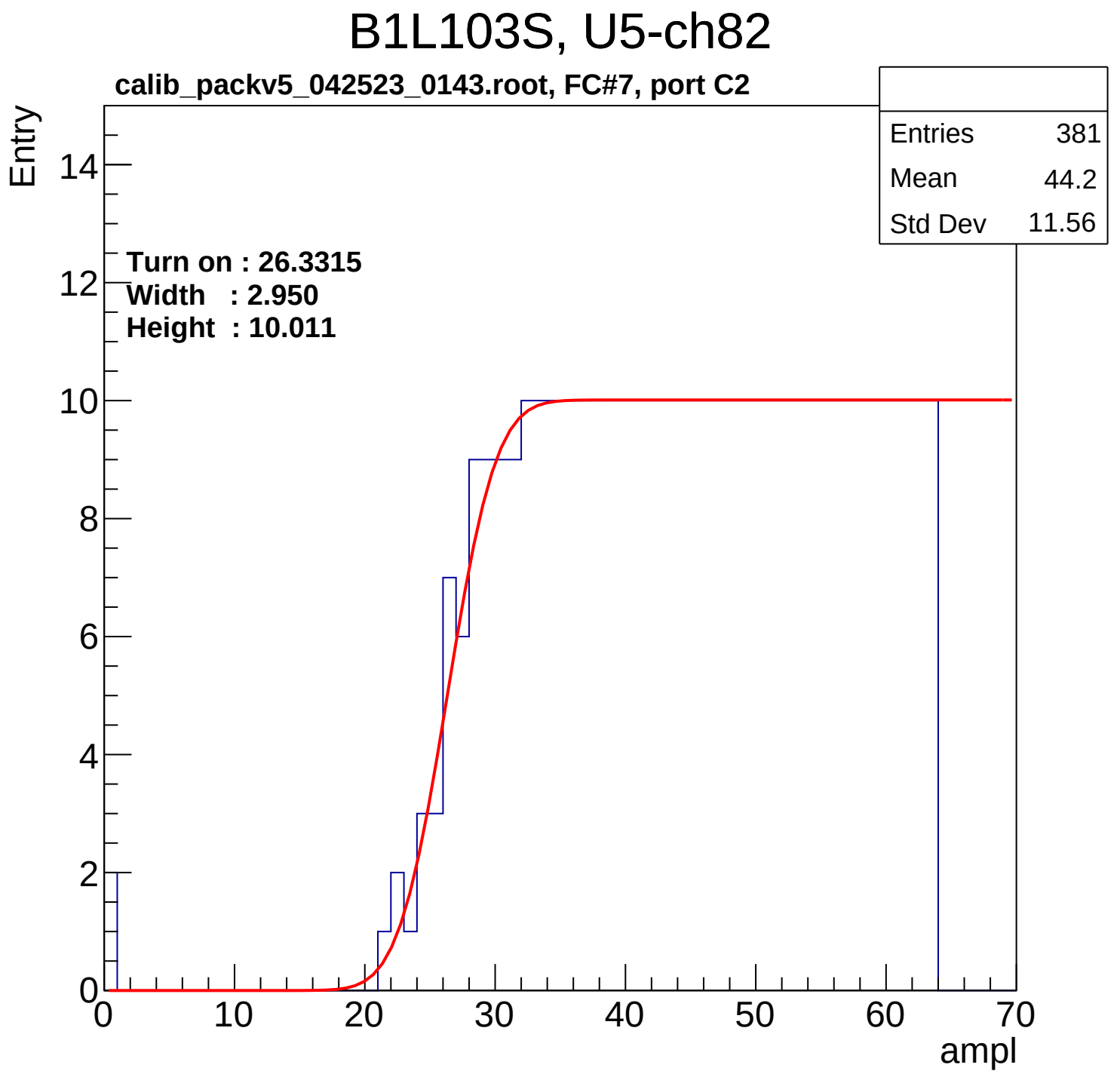

B1L103S, U5-ch77
calib_packv5_042523_0143.root, FC#7, port C2
Entries 362
Mean 45.02
Std Dev 11.35
Turn on : 28.2390
Width : 3.607
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

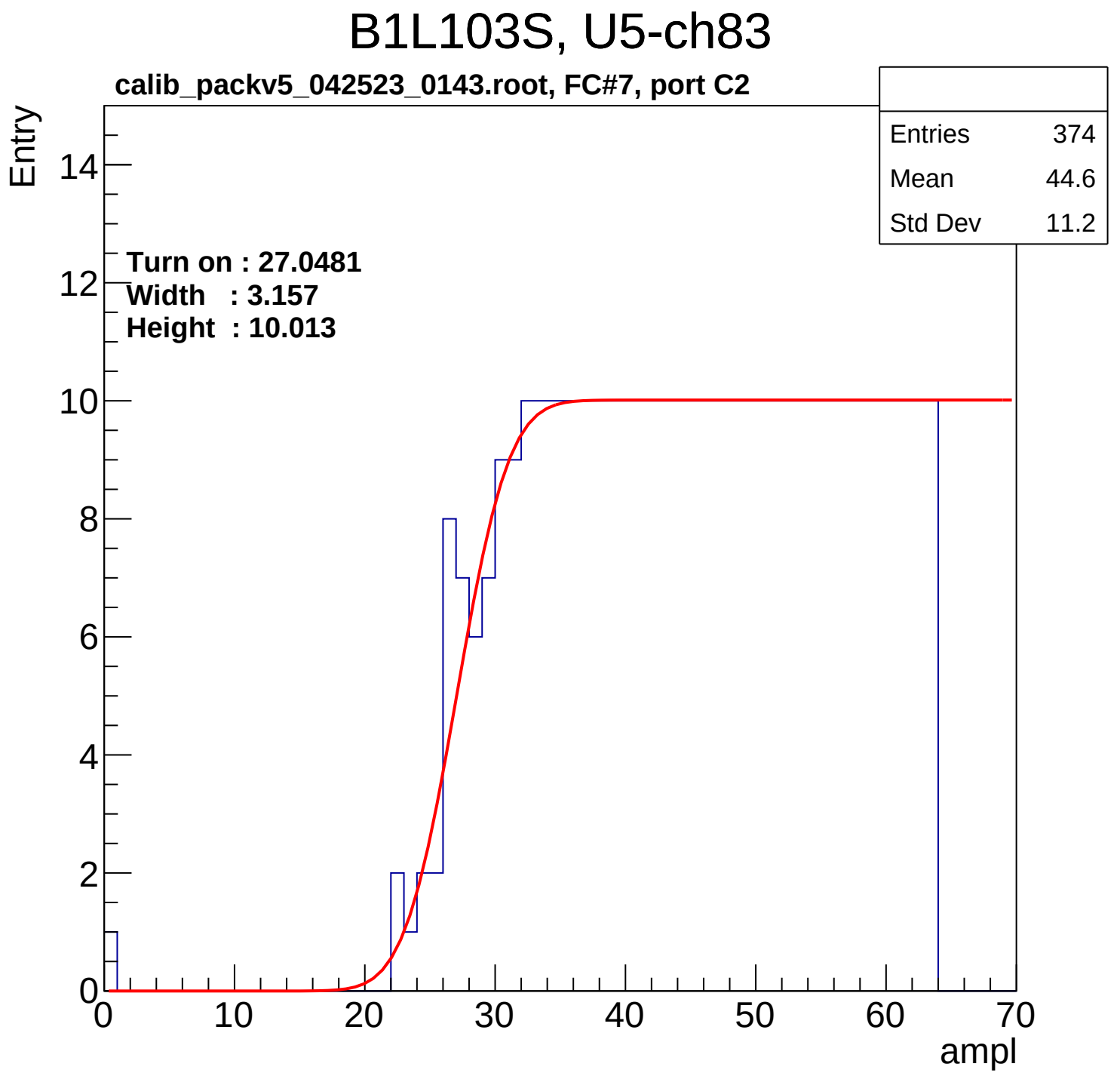

B1L103S, U5-ch78
calib_packv5_042523_0143.root, FC#7, port C2
Entries 402
Mean 42.99
Std Dev 12.56
Turn on : 24.1002
Width : 4.294
Height : 10.059
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

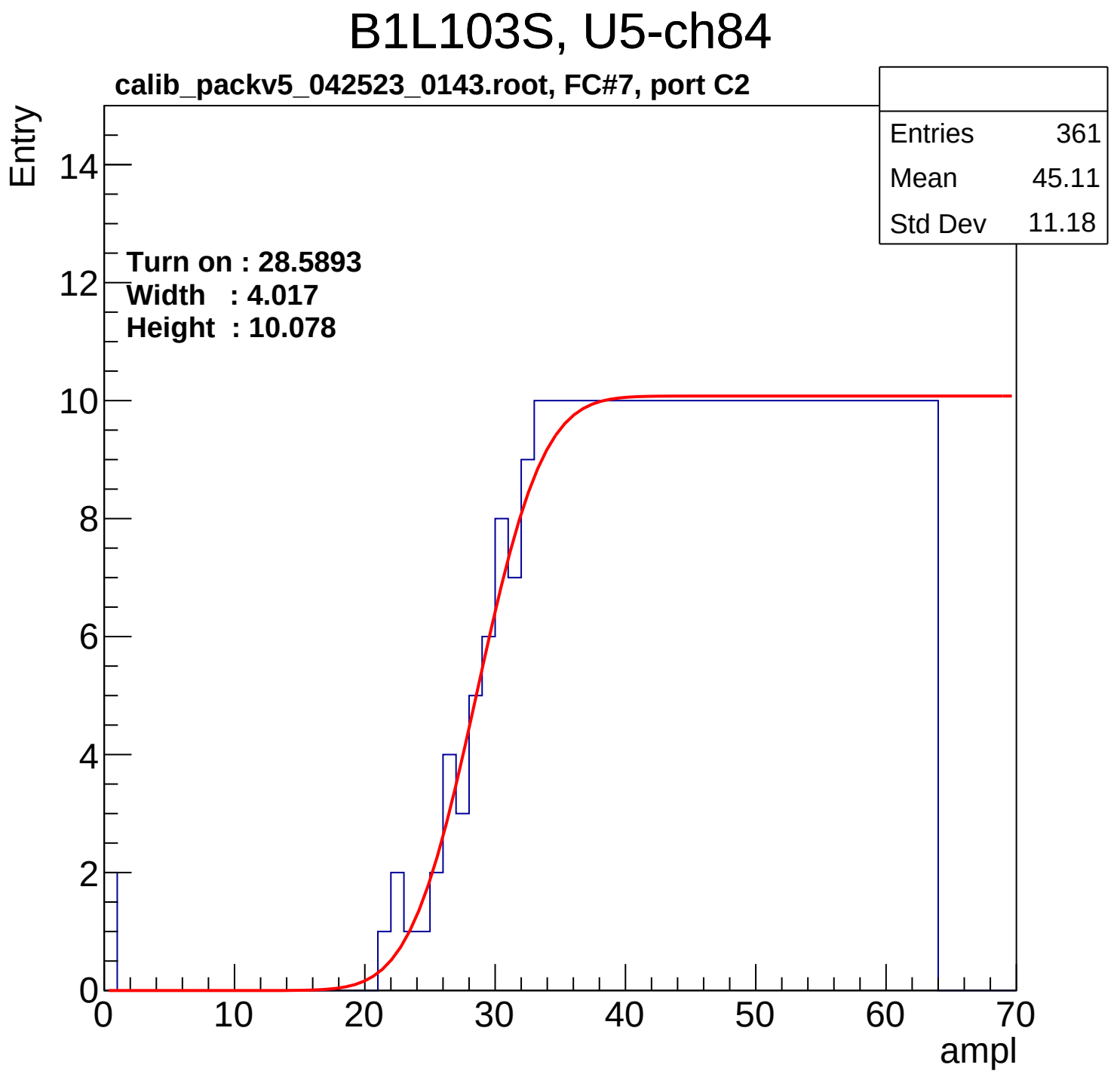

B1L103S, U5-ch79
calib_packv5_042523_0143.root, FC#7, port C2
Entries 385
Mean 44.08
Std Dev 11.47
Turn on : 26.0127
Width : 3.438
Height : 10.048
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

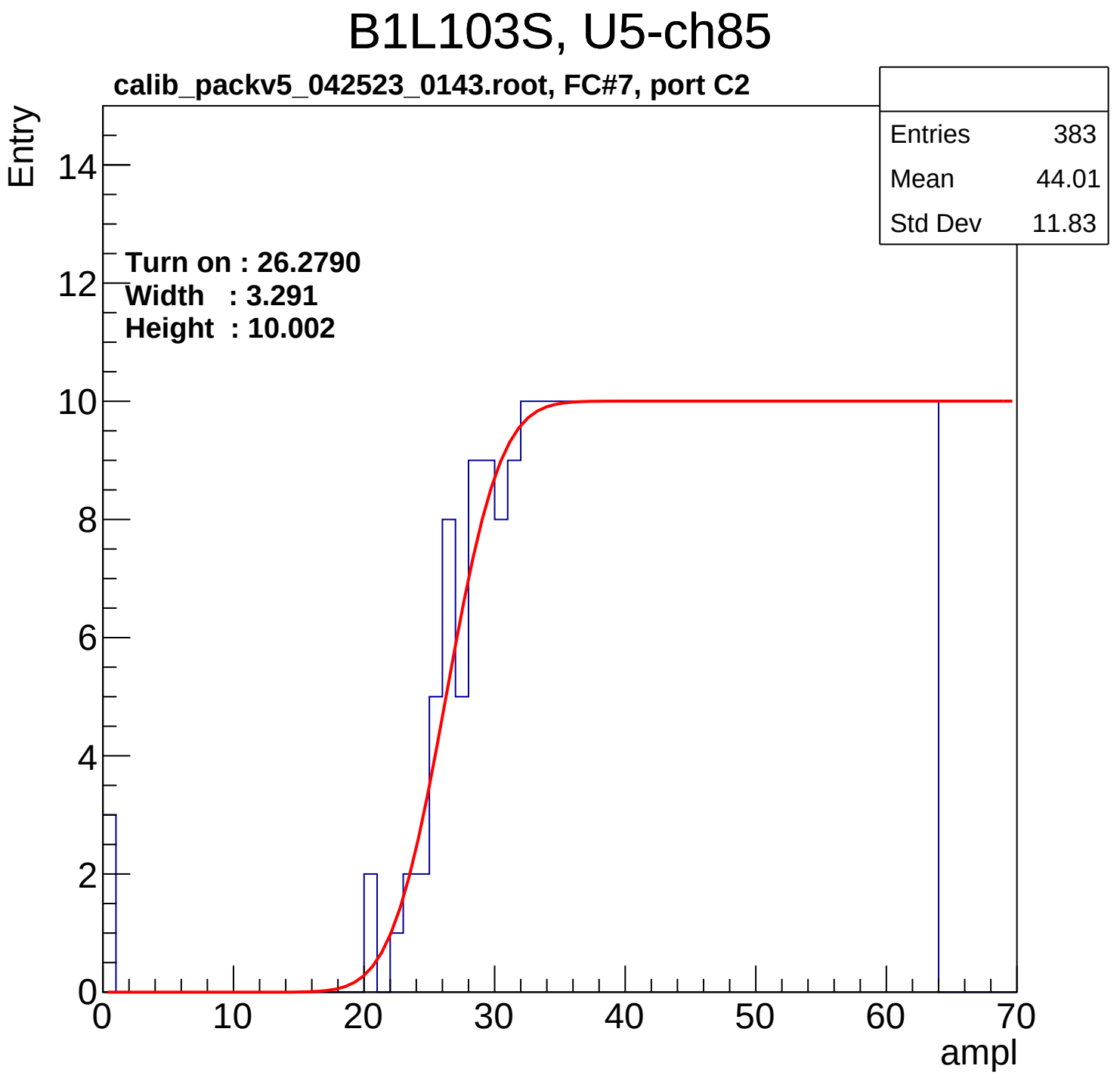

B1L103S, U5-ch80
calib_packv5_042523_0143.root, FC#7, port C2
Entries 370
Mean 44.5
Std Dev 11.91
Turn on : 28.0484
Width : 3.058
Height : 10.045
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

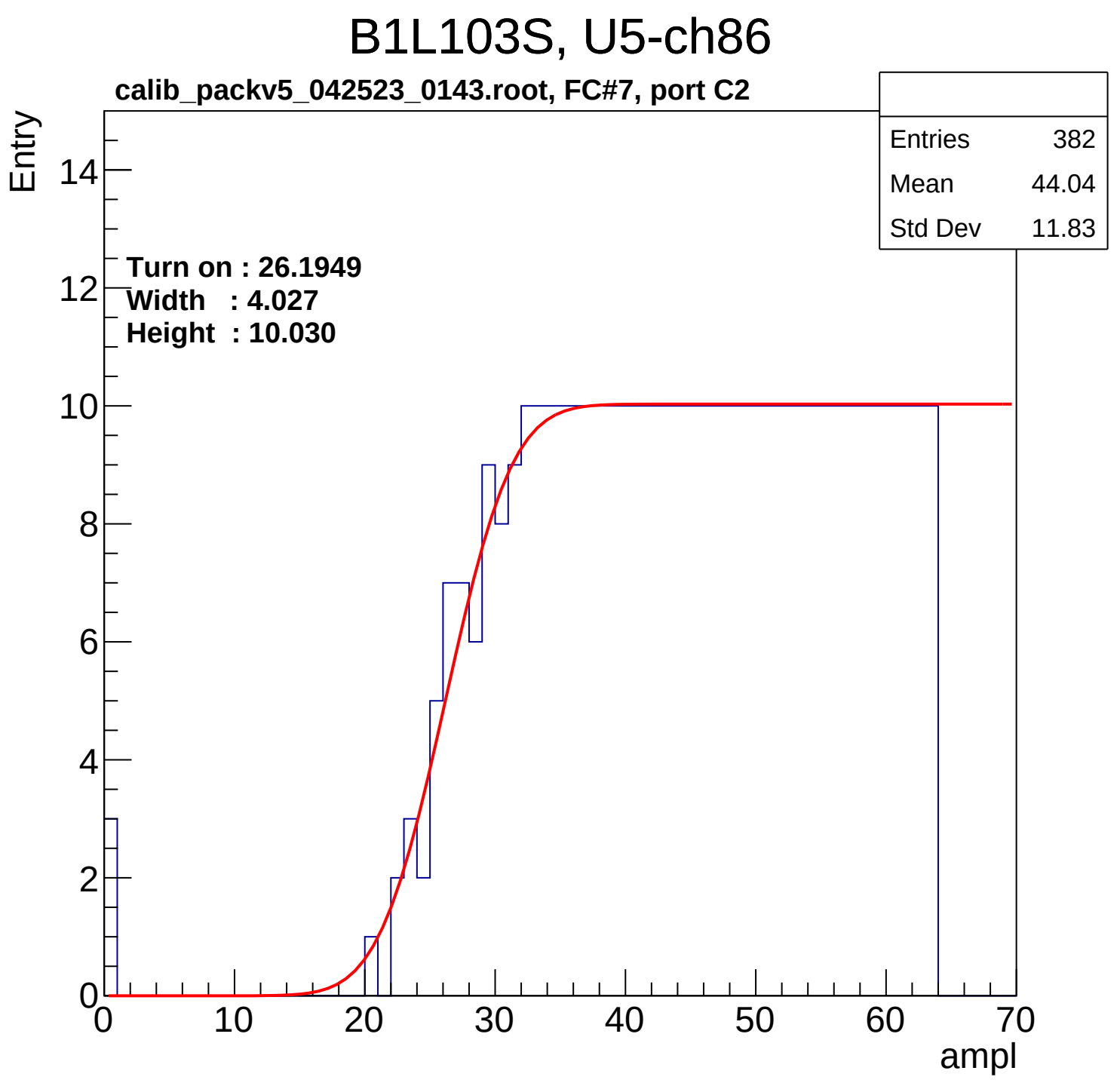

B1L103S, U5-ch81
calib_packv5_042523_0143.root, FC#7, port C2
Entries 367
Mean 44.44
Std Dev 12.37
Turn on : 28.2635
Width : 3.355
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

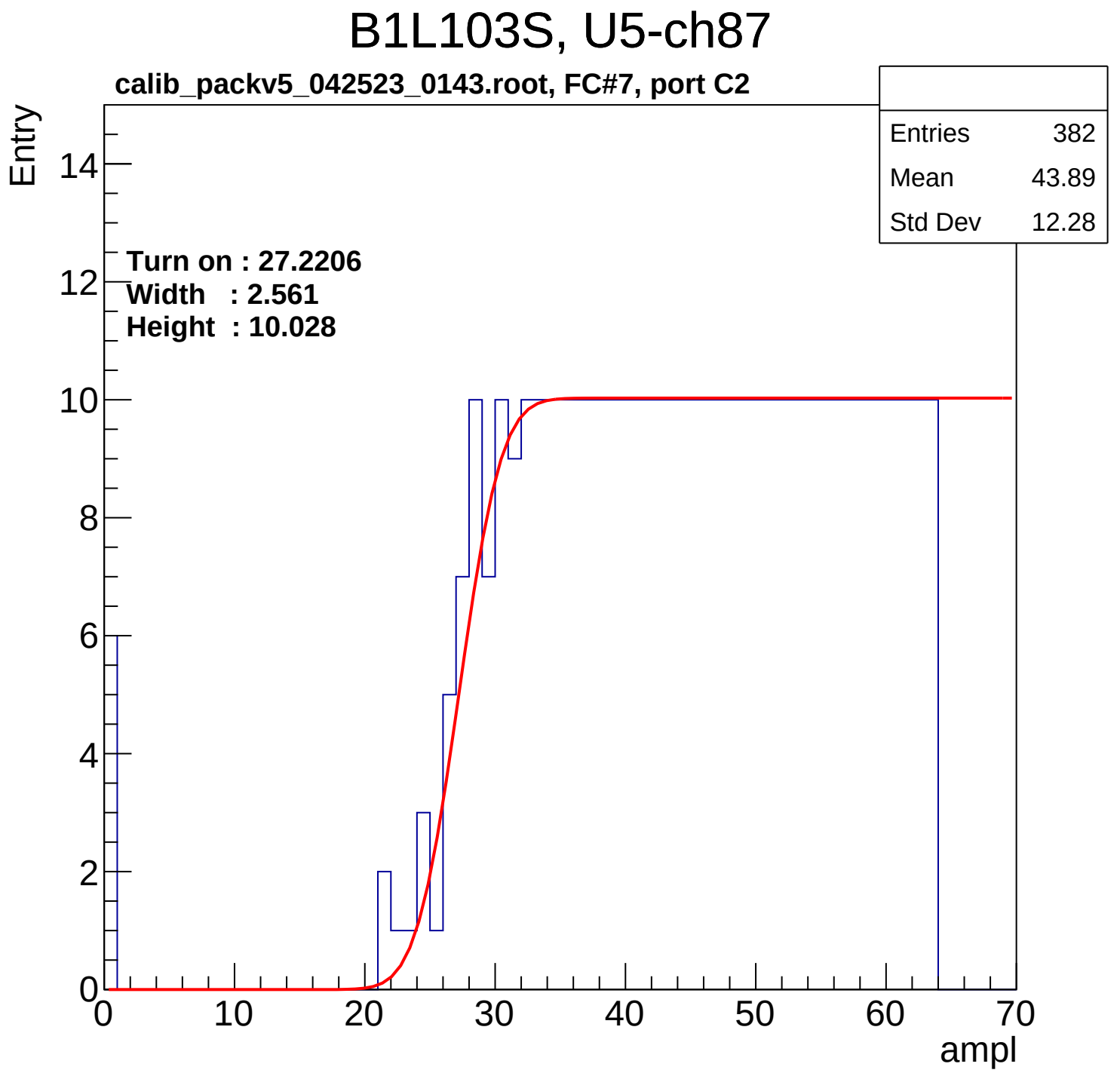

B1L103S, U5-ch82
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.2
Std Dev 11.56
Turn on : 26.3315
Width : 2.950
Height : 10.011
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

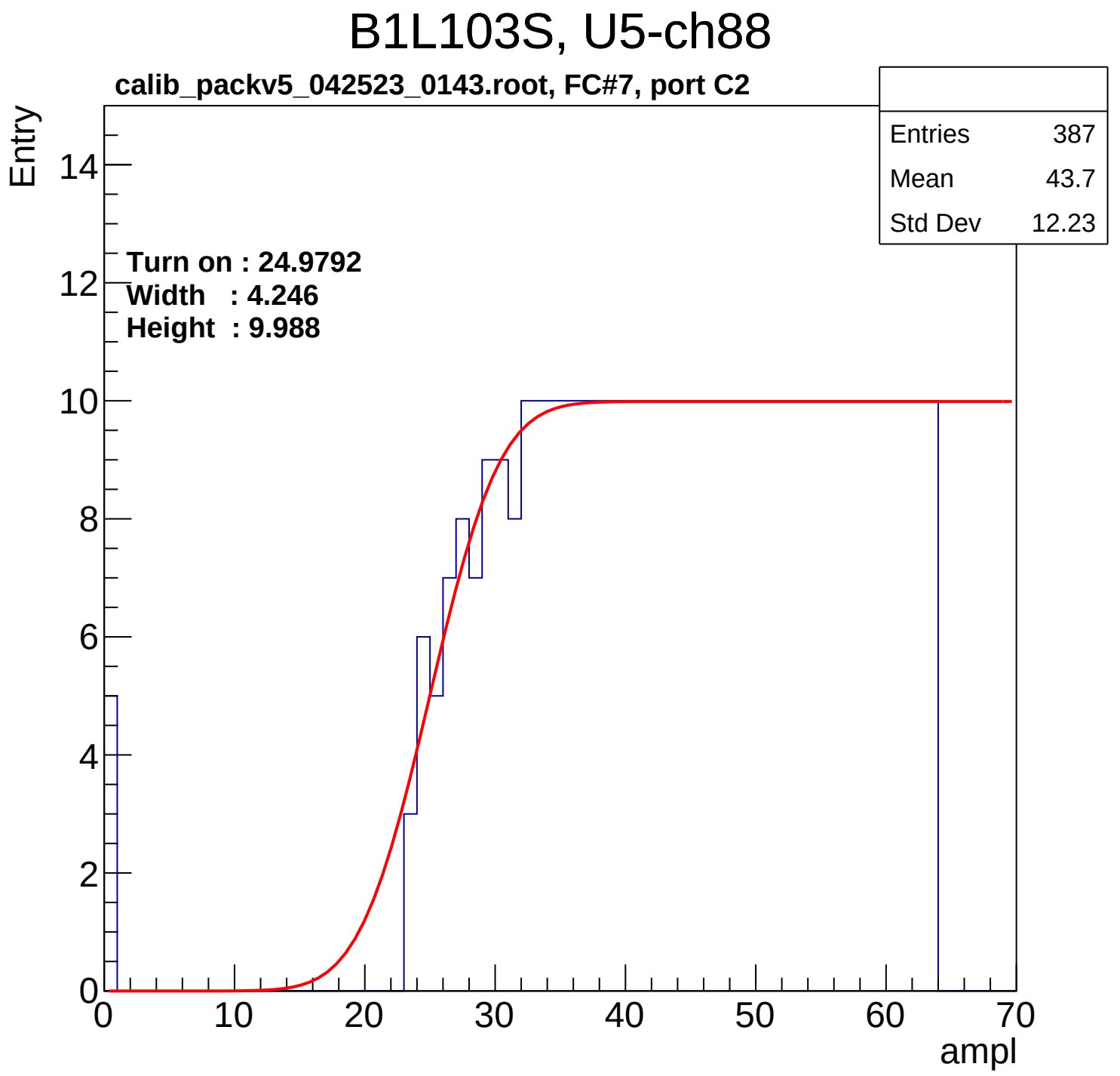

B1L103S, U5-ch83
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.6
Std Dev 11.2
Turn on : 27.0481
Width : 3.157
Height : 10.013
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

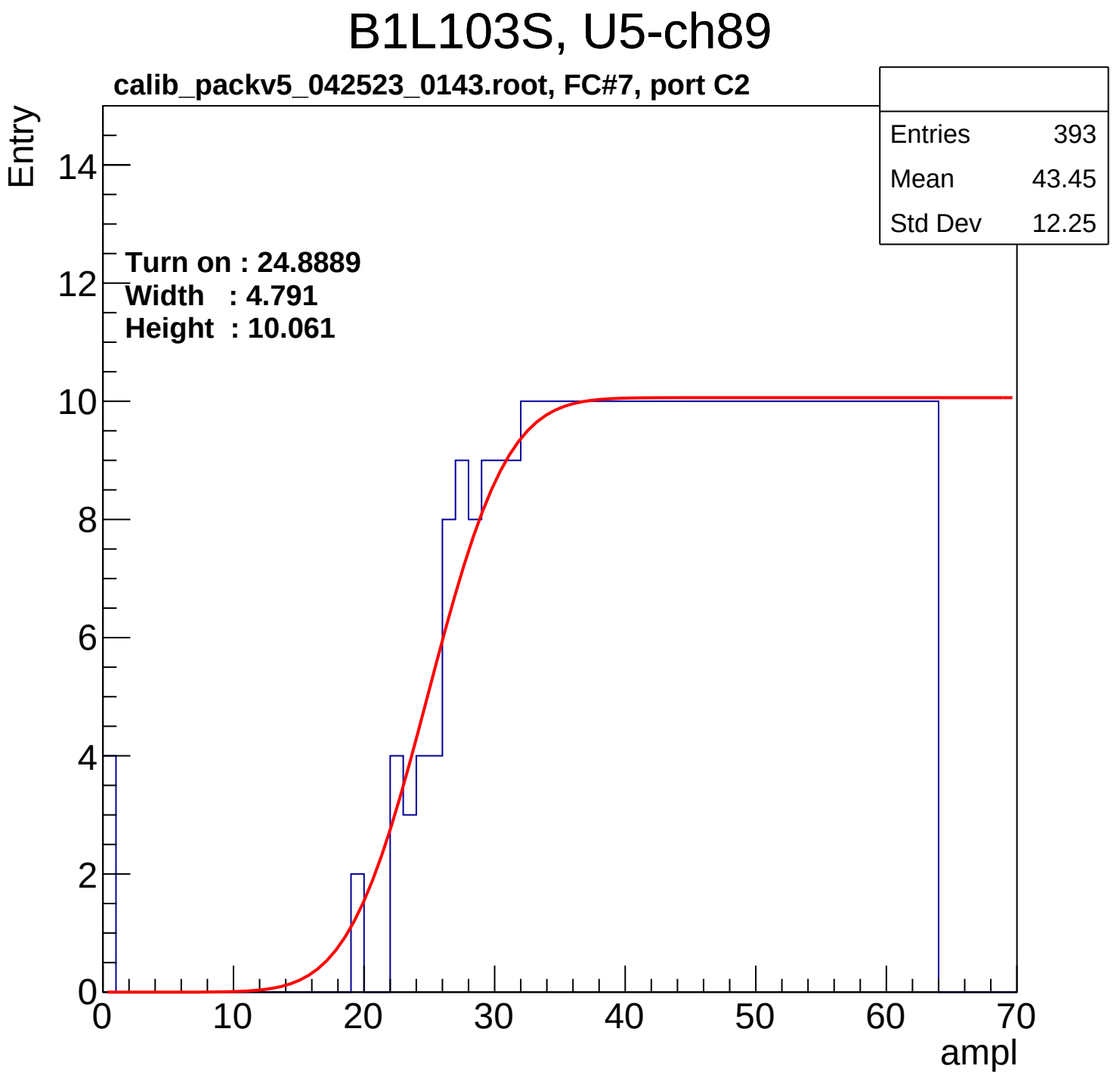

B1L103S, U5-ch84
calib_packv5_042523_0143.root, FC#7, port C2
Entries 361
Mean 45.11
Std Dev 11.18
Turn on : 28.5893
Width : 4.017
Height : 10.078
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

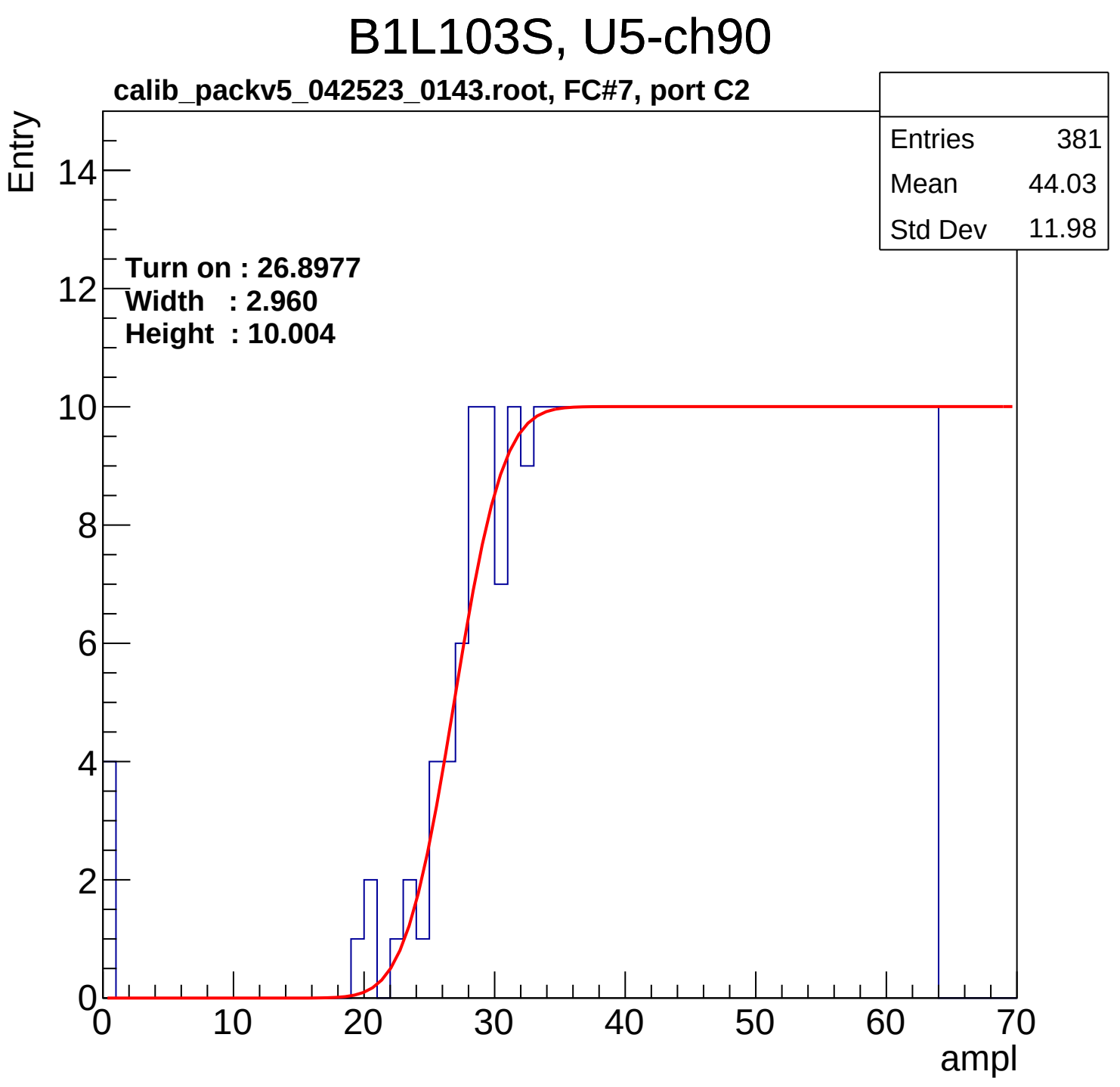

B1L103S, U5-ch85
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 44.01
Std Dev 11.83
Turn on : 26.2790
Width : 3.291
Height : 10.002
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

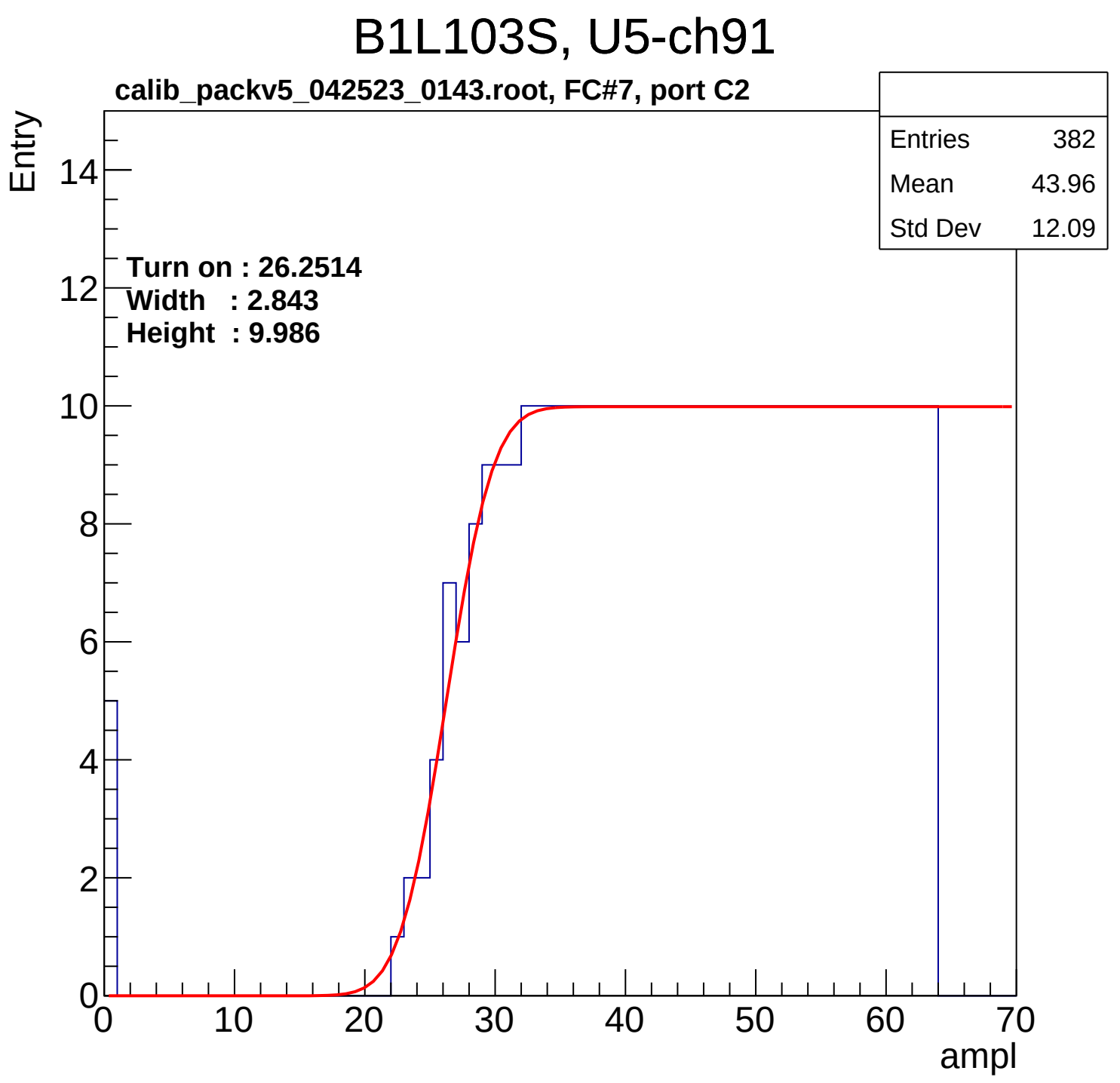

B1L103S, U5-ch86
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 44.04
Std Dev 11.83
Turn on : 26.1949
Width : 4.027
Height : 10.030
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

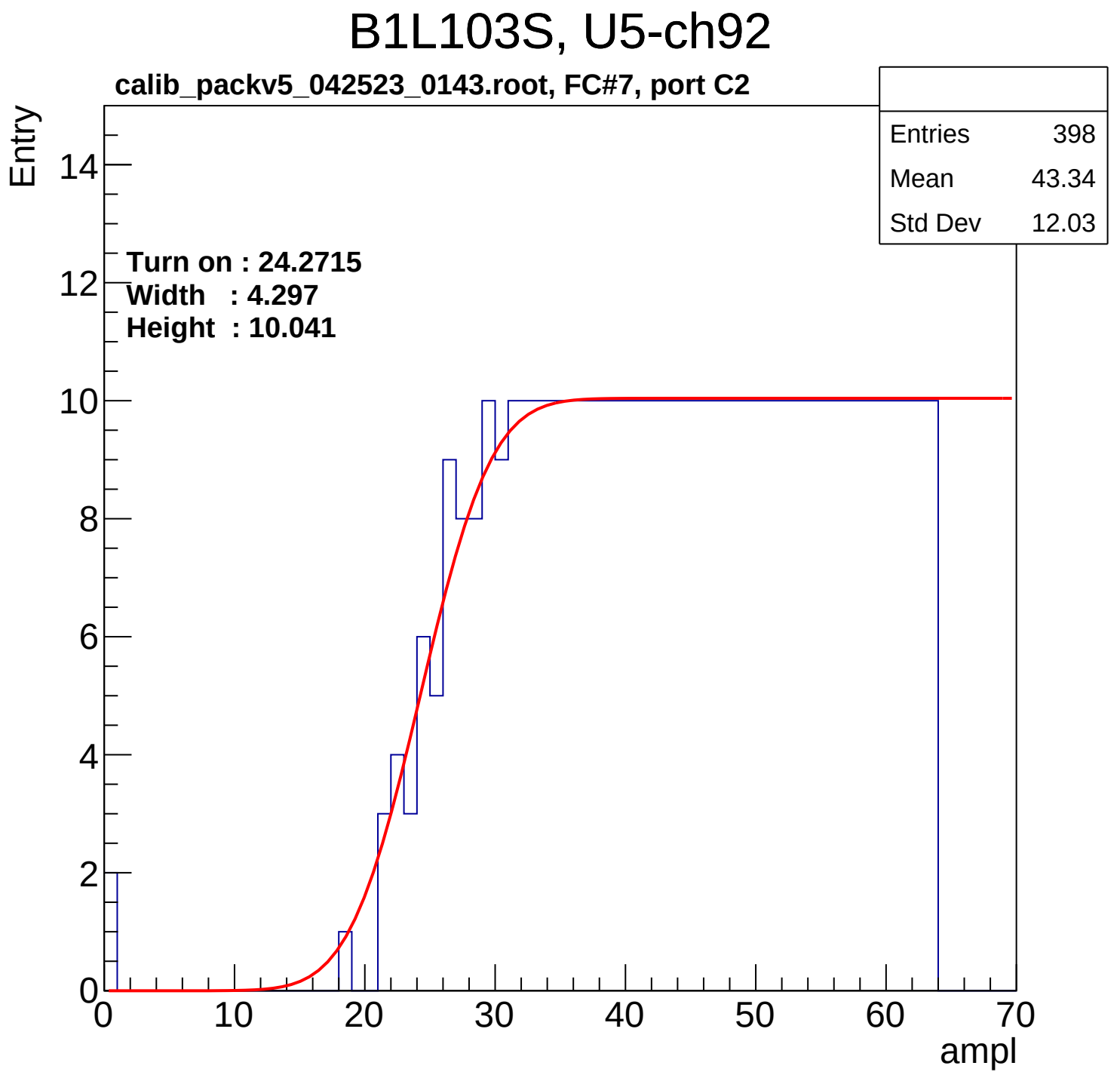

B1L103S, U5-ch87
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 43.89
Std Dev 12.28
Turn on : 27.2206
Width : 2.561
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

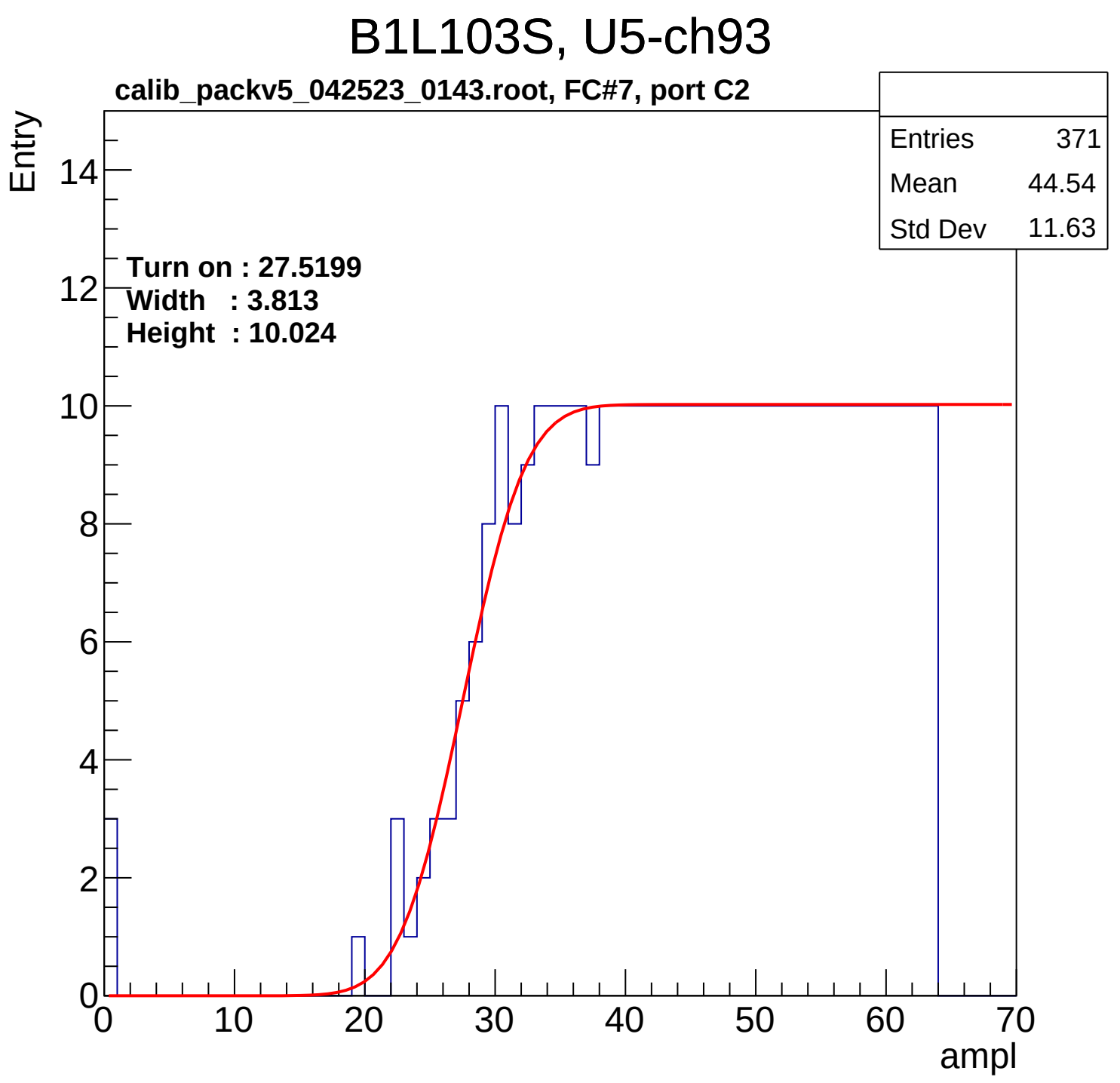

B1L103S, U5-ch88
calib_packv5_042523_0143.root, FC#7, port C2
Entries 387
Mean 43.7
Std Dev 12.23
Turn on : 24.9792
Width : 4.246
Height : 9.988
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

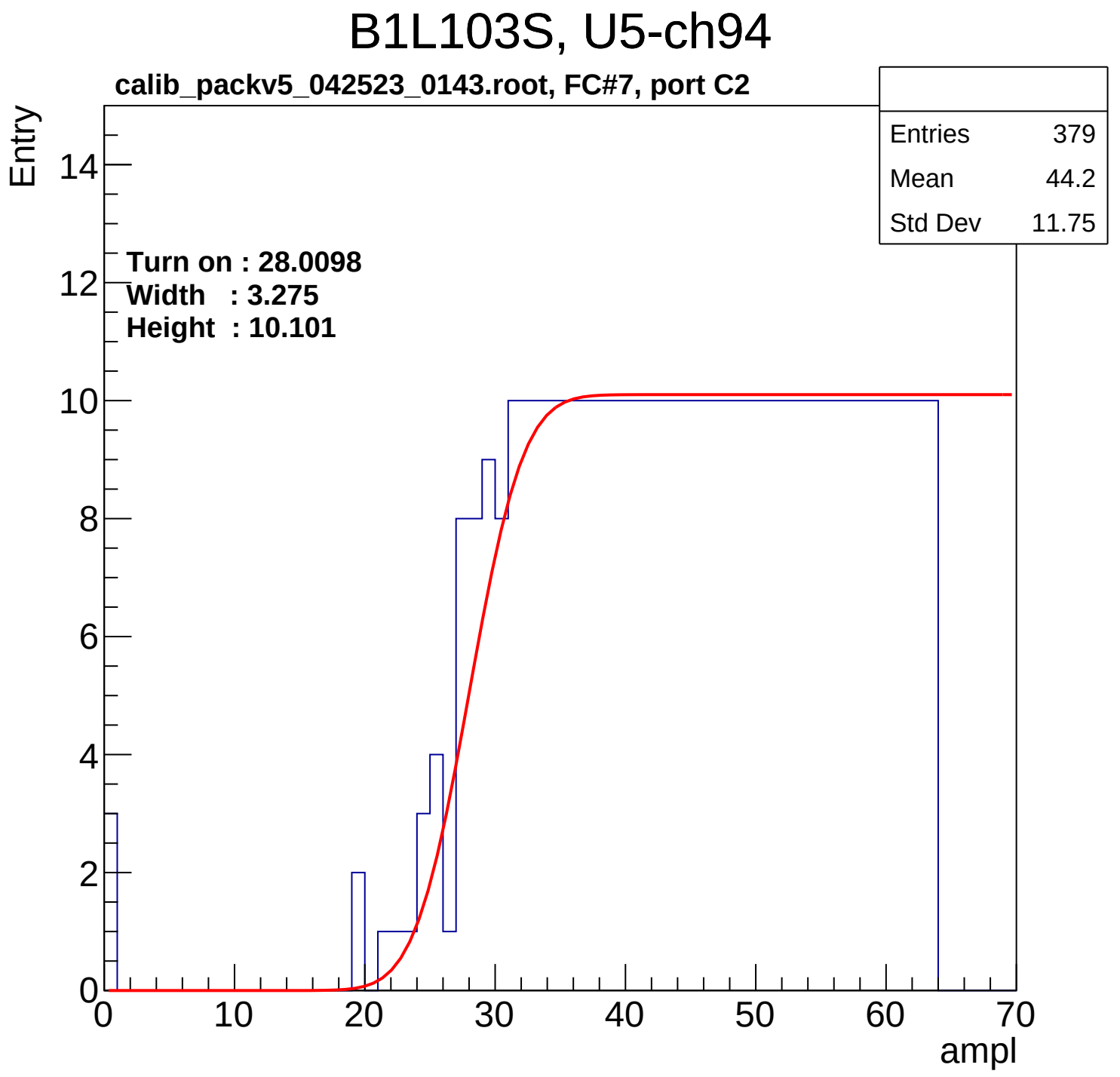

B1L103S, U5-ch89
calib_packv5_042523_0143.root, FC#7, port C2
Entries 393
Mean 43.45
Std Dev 12.25
Turn on : 24.8889
Width : 4.791
Height : 10.061
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

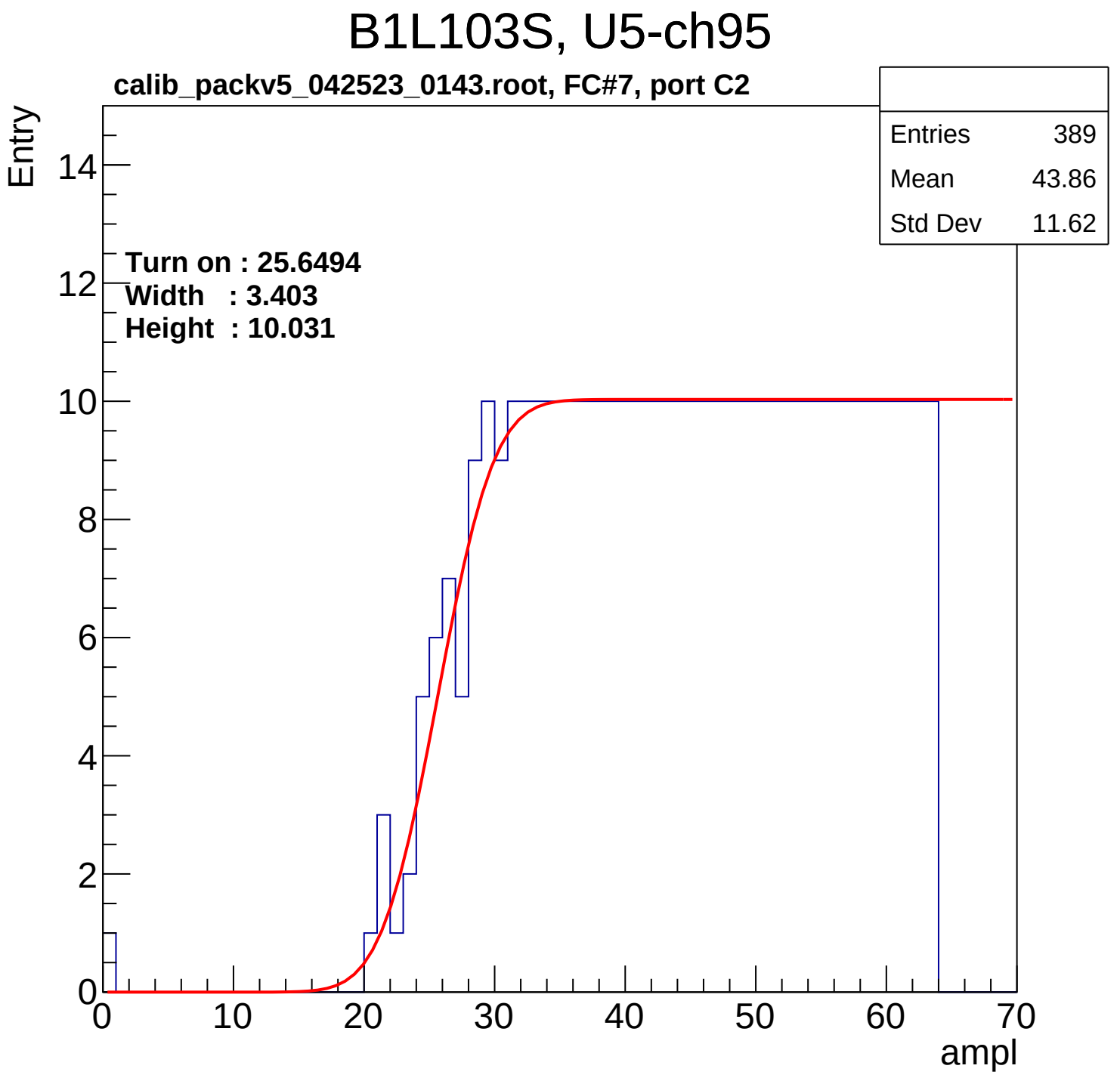

B1L103S, U5-ch90
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.03
Std Dev 11.98
Turn on : 26.8977
Width : 2.960
Height : 10.004
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

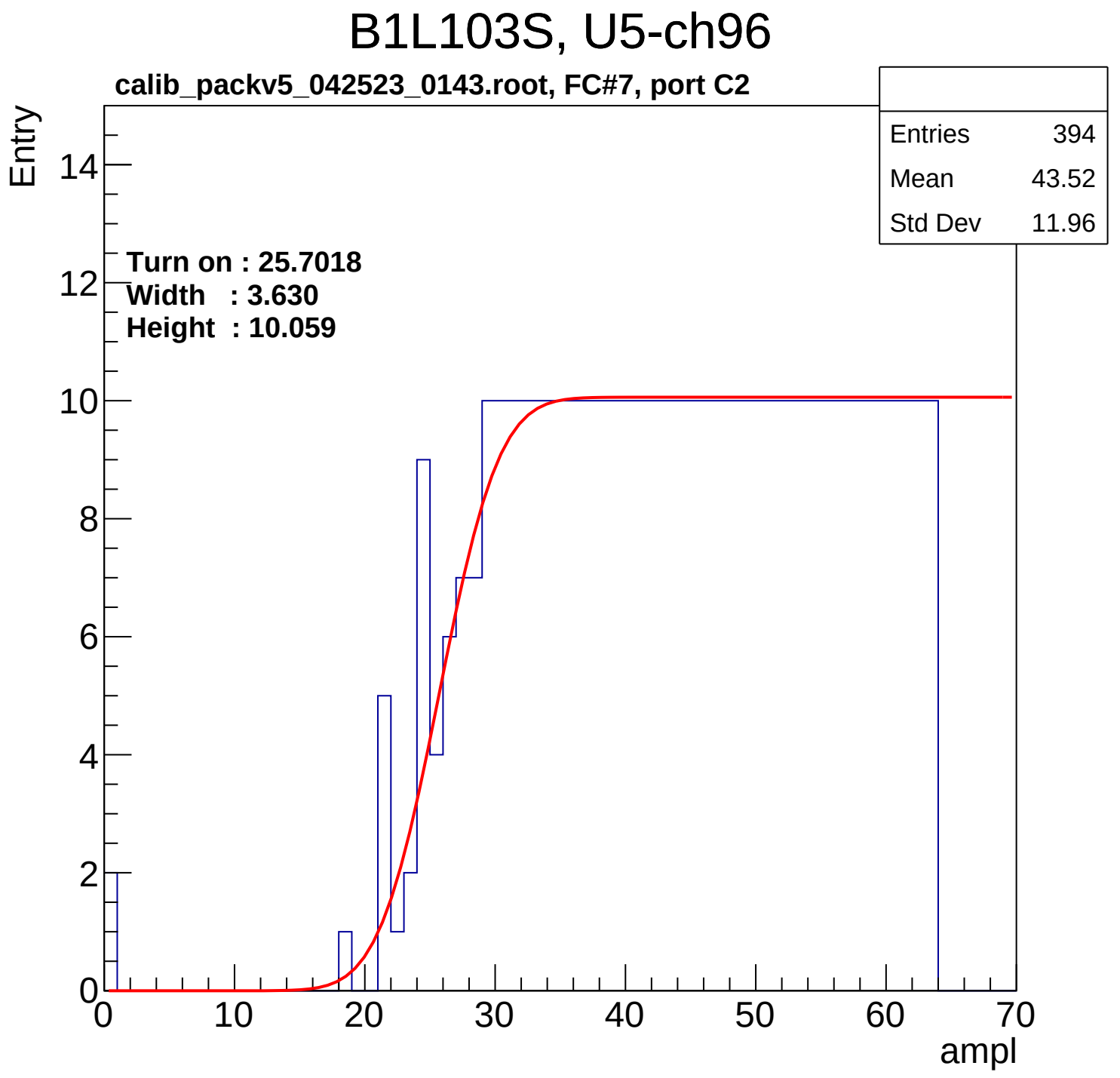

B1L103S, U5-ch91
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 43.96
Std Dev 12.09
Turn on : 26.2514
Width : 2.843
Height : 9.986
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

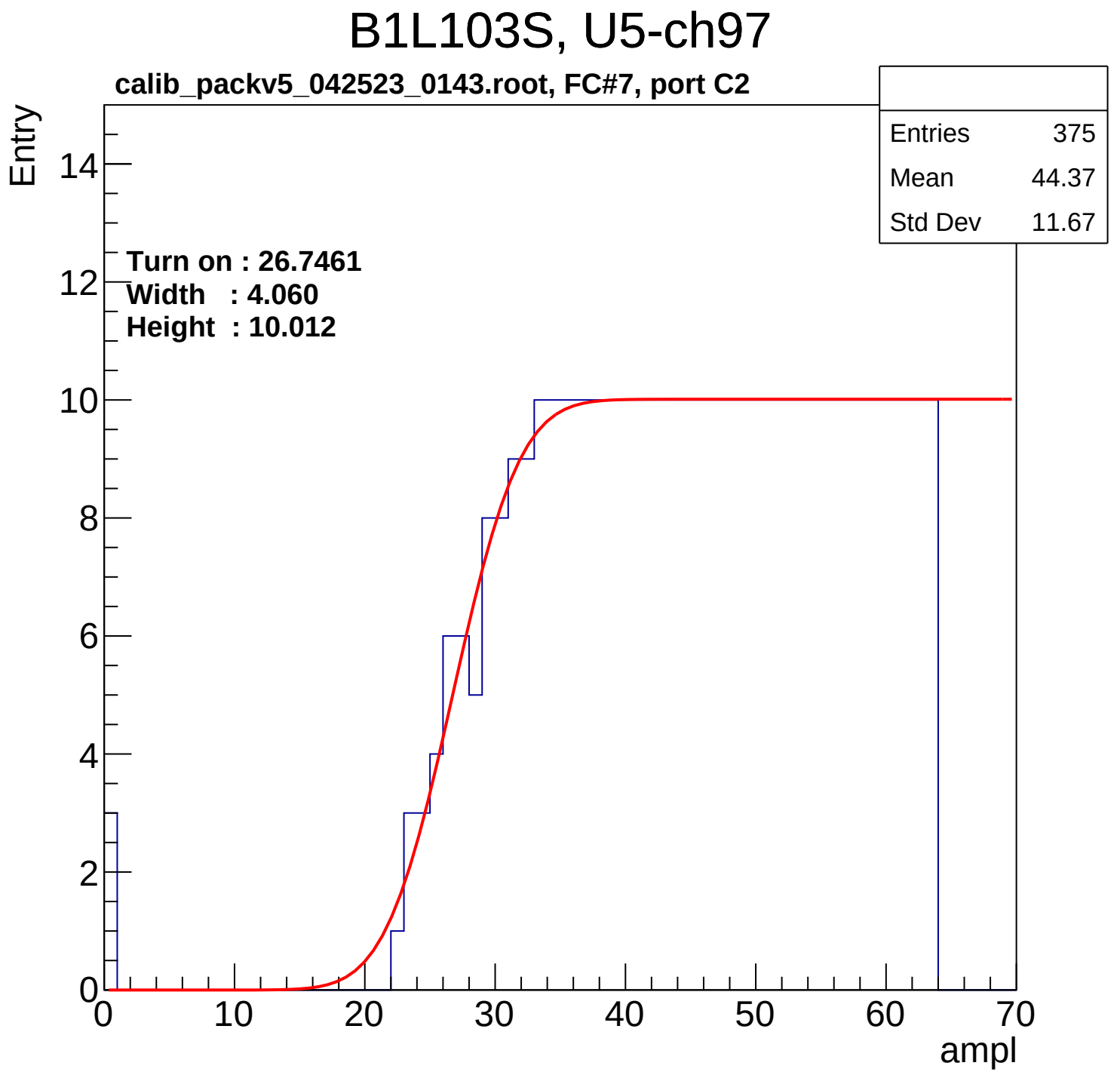

B1L103S, U5-ch92
calib_packv5_042523_0143.root, FC#7, port C2
Entries 398
Mean 43.34
Std Dev 12.03
Turn on : 24.2715
Width : 4.297
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

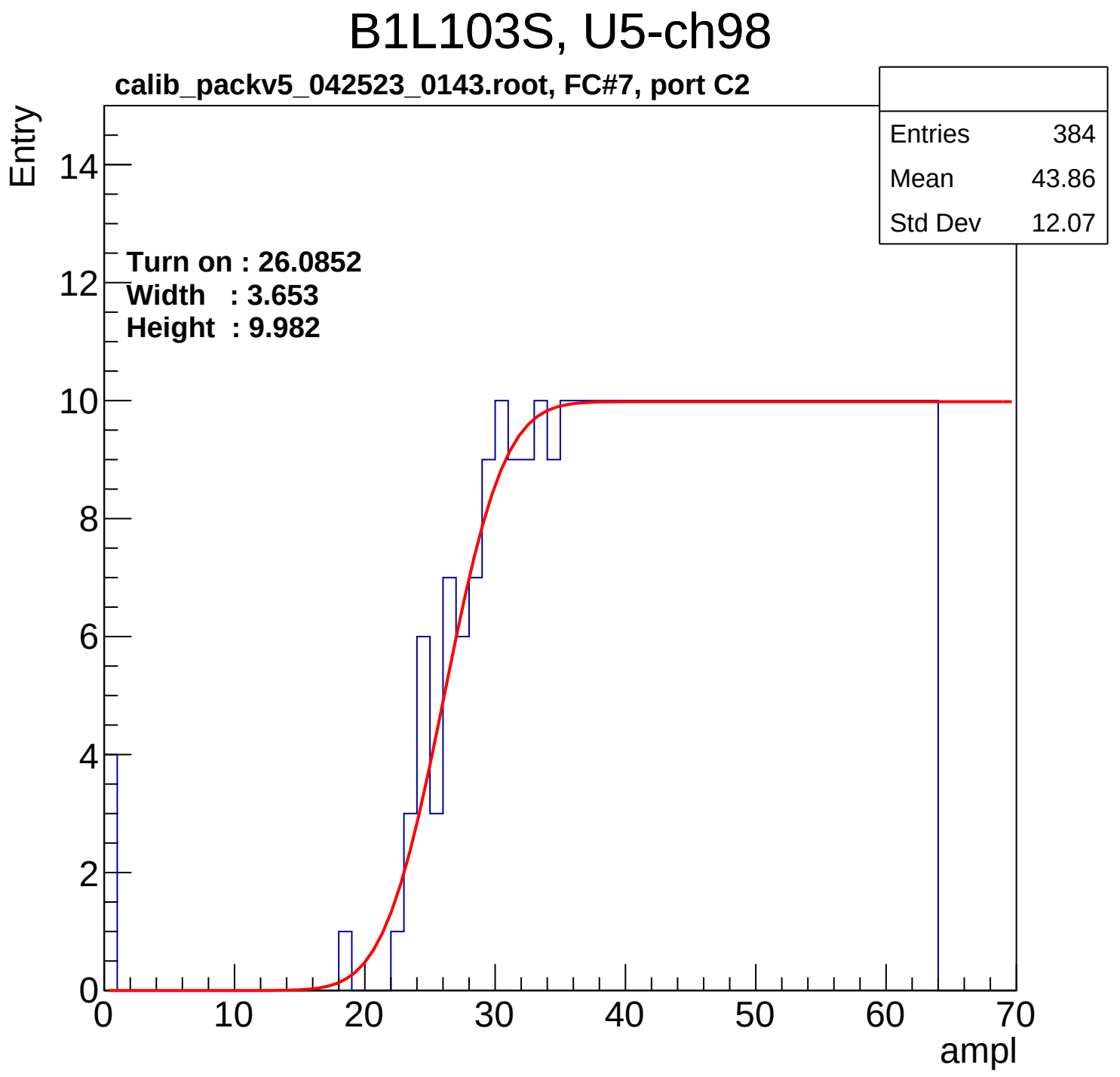

B1L103S, U5-ch93
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.54
Std Dev 11.63
Turn on : 27.5199
Width : 3.813
Height : 10.024
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

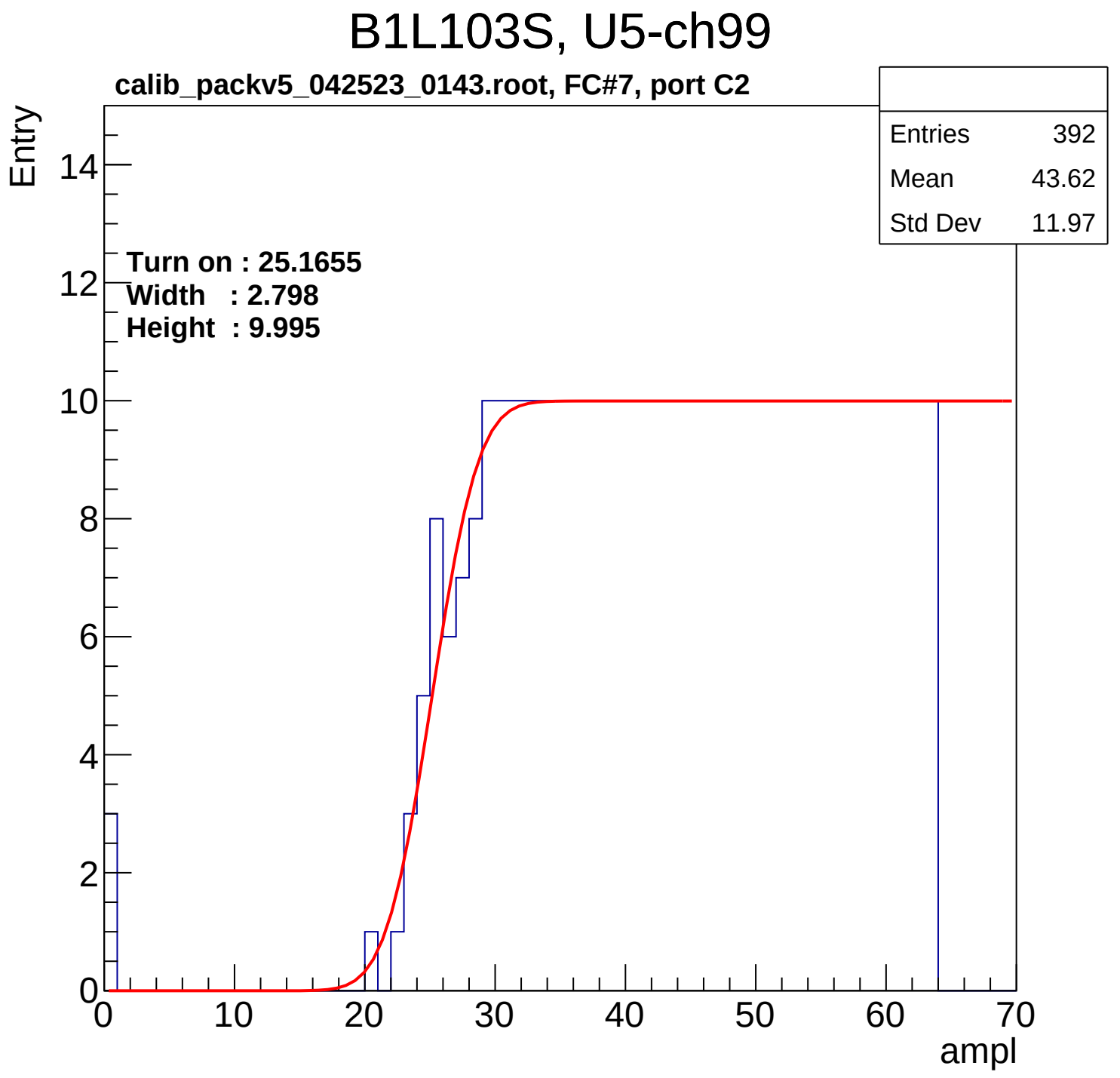

B1L103S, U5-ch94
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.2
Std Dev 11.75
Turn on : 28.0098
Width : 3.275
Height : 10.101
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

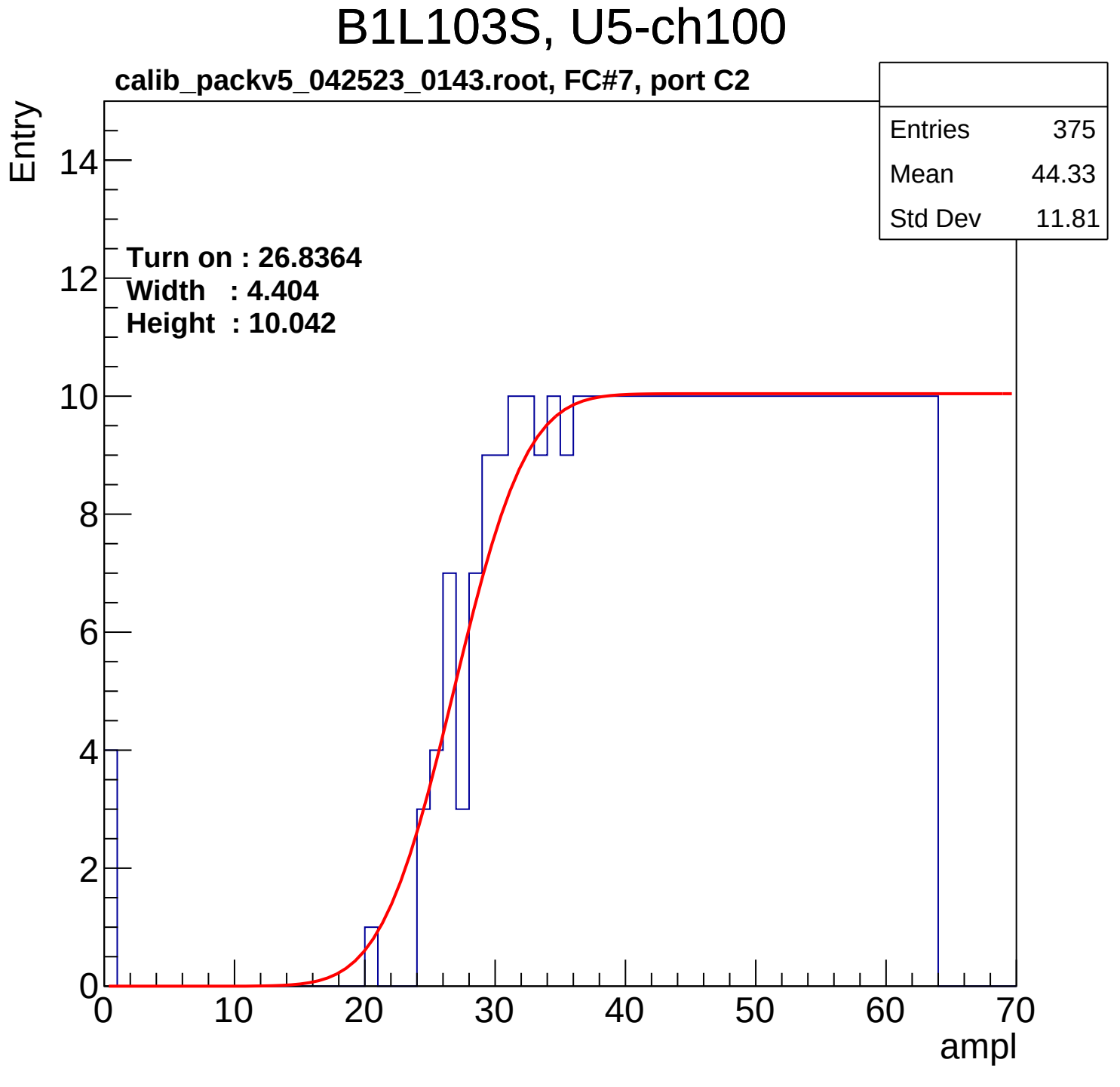

B1L103S, U5-ch95
calib_packv5_042523_0143.root, FC#7, port C2
Entries 389
Mean 43.86
Std Dev 11.62
Turn on : 25.6494
Width : 3.403
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

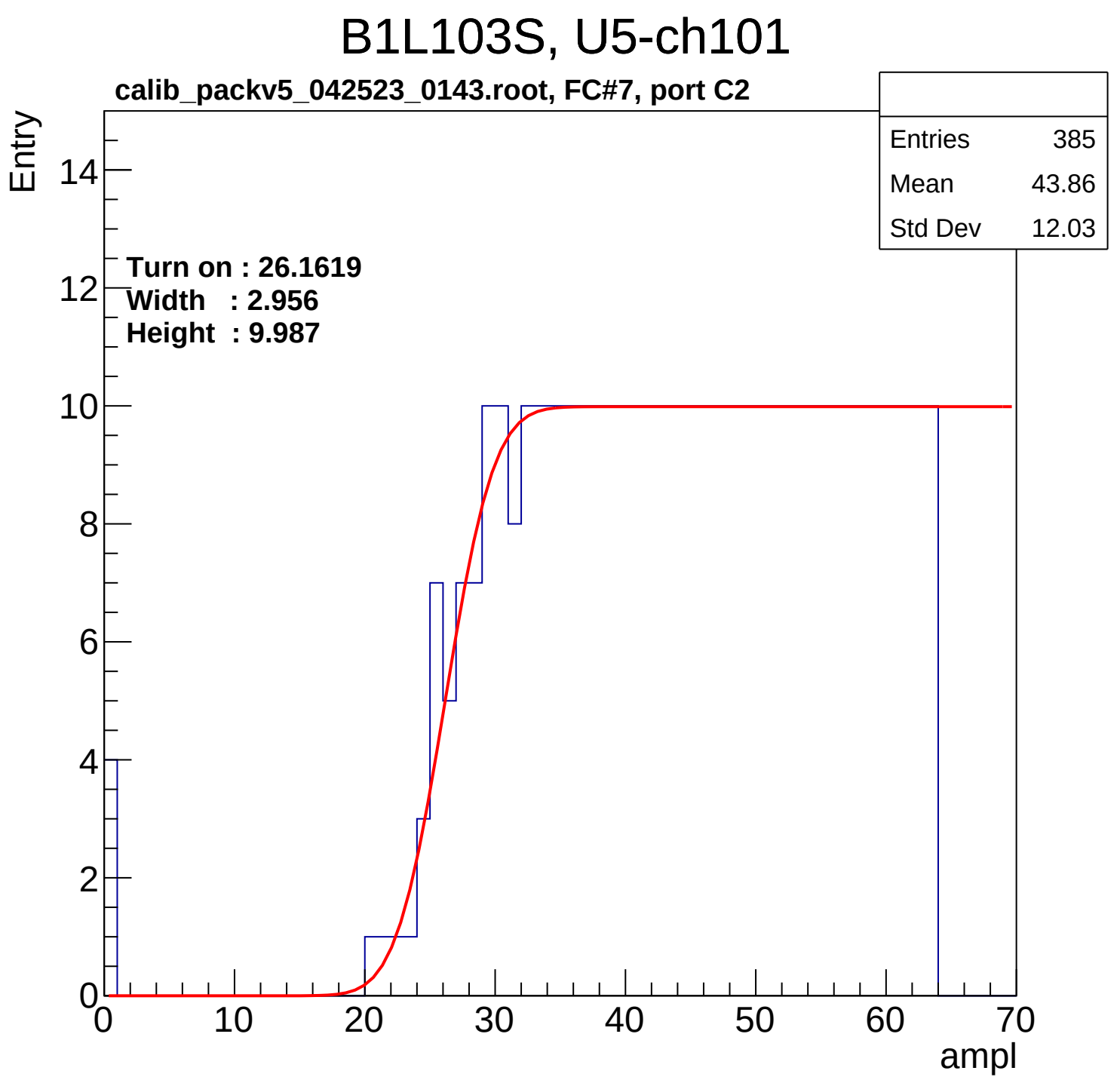

B1L103S, U5-ch96
calib_packv5_042523_0143.root, FC#7, port C2
Entries 394
Mean 43.52
Std Dev 11.96
Turn on : 25.7018
Width : 3.630
Height : 10.059
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

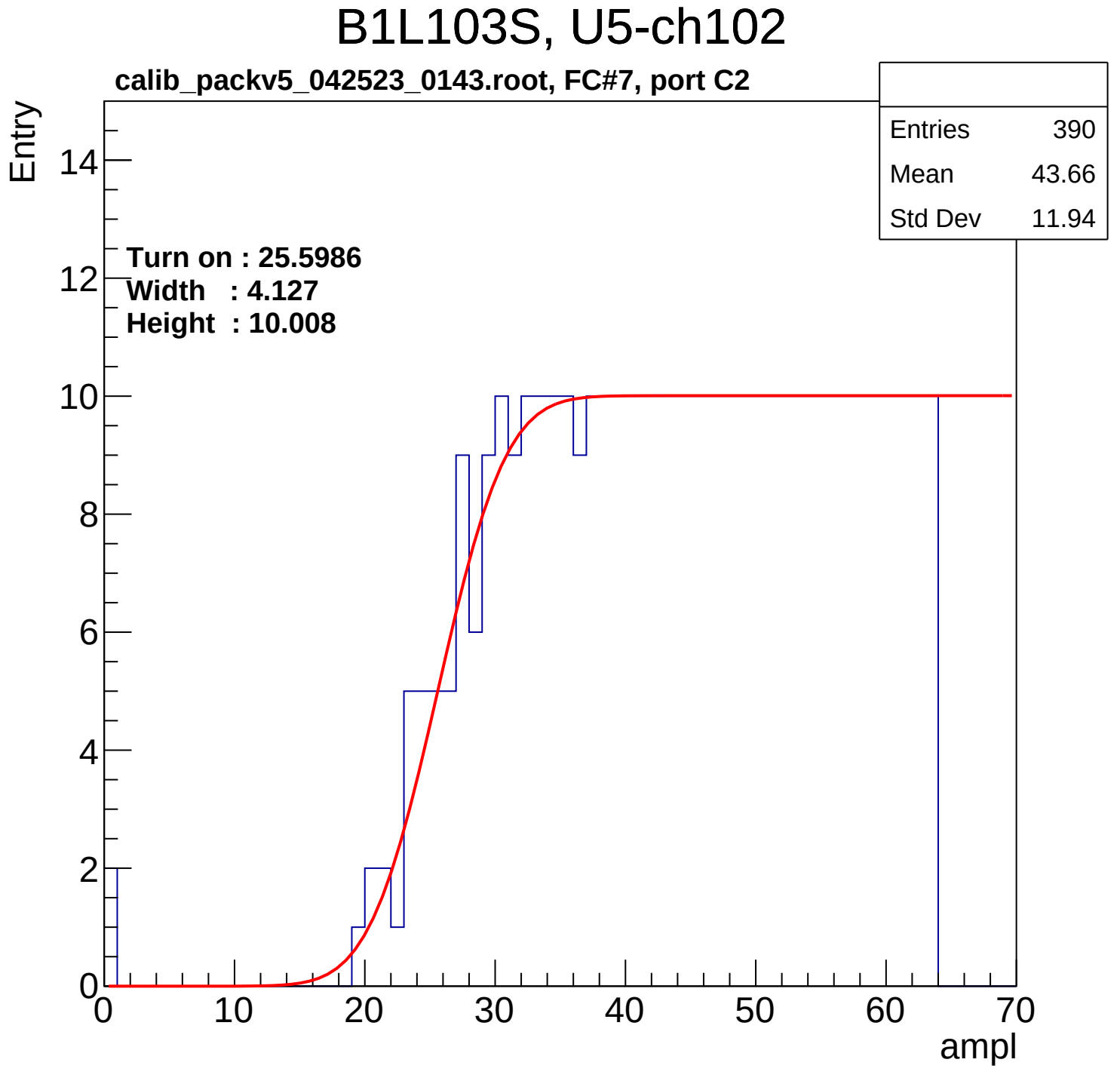

B1L103S, U5-ch97
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.37
Std Dev 11.67
Turn on : 26.7461
Width : 4.060
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

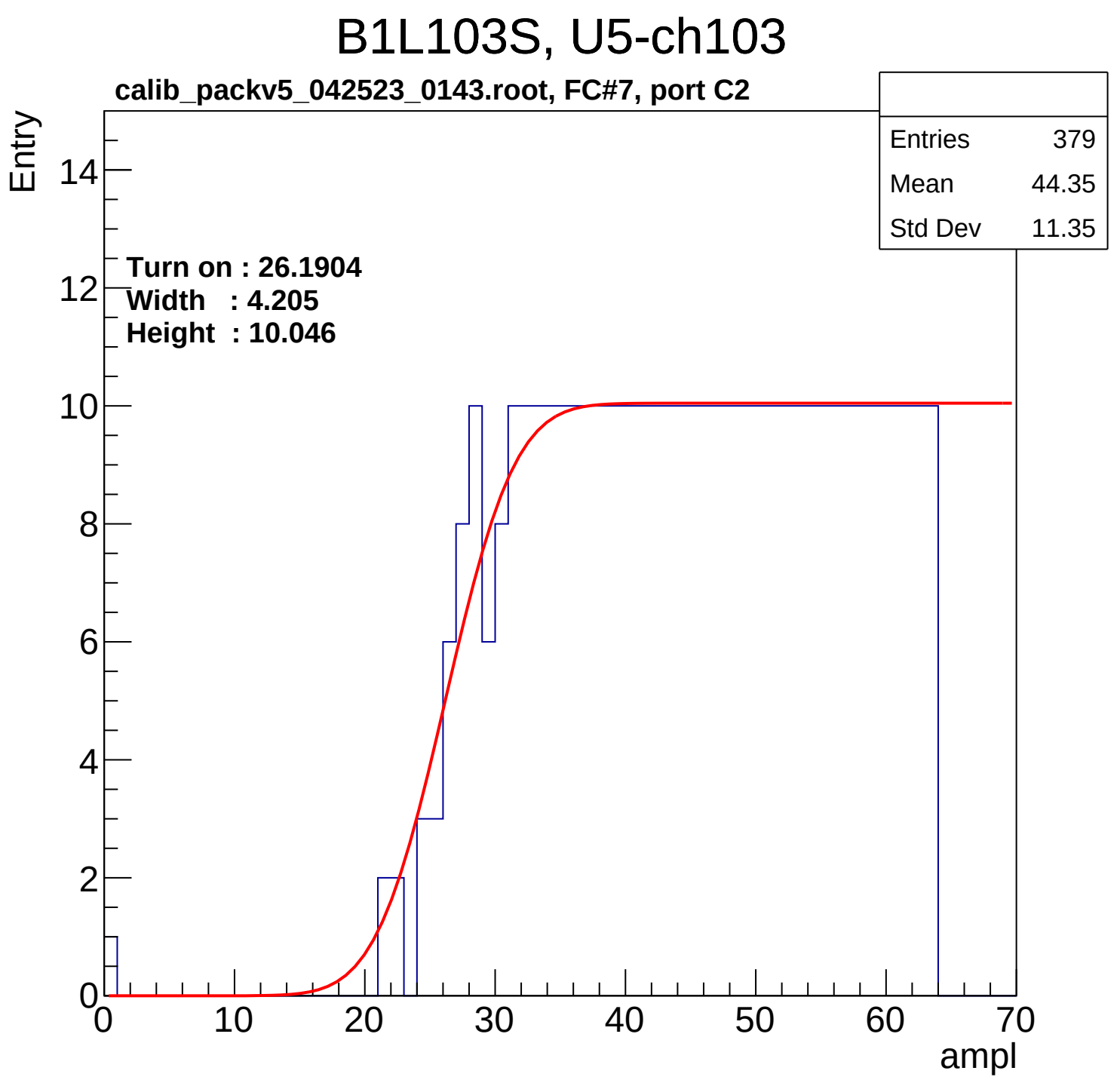

B1L103S, U5-ch98
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 43.86
Std Dev 12.07
Turn on : 26.0852
Width : 3.653
Height : 9.982
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

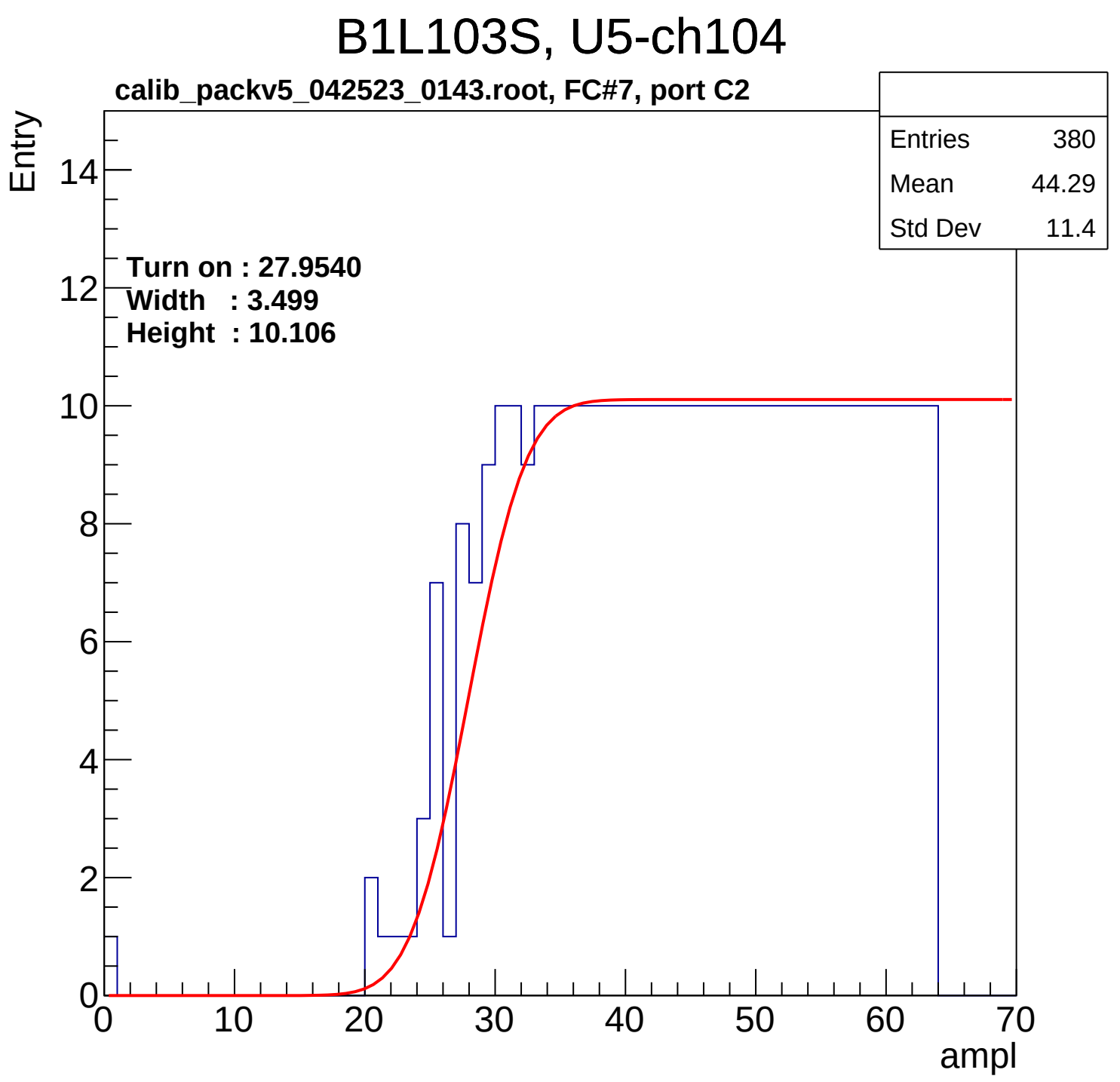

B1L103S, U5-ch99
calib_packv5_042523_0143.root, FC#7, port C2
Entries 392
Mean 43.62
Std Dev 11.97
Turn on : 25.1655
Width : 2.798
Height : 9.995
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

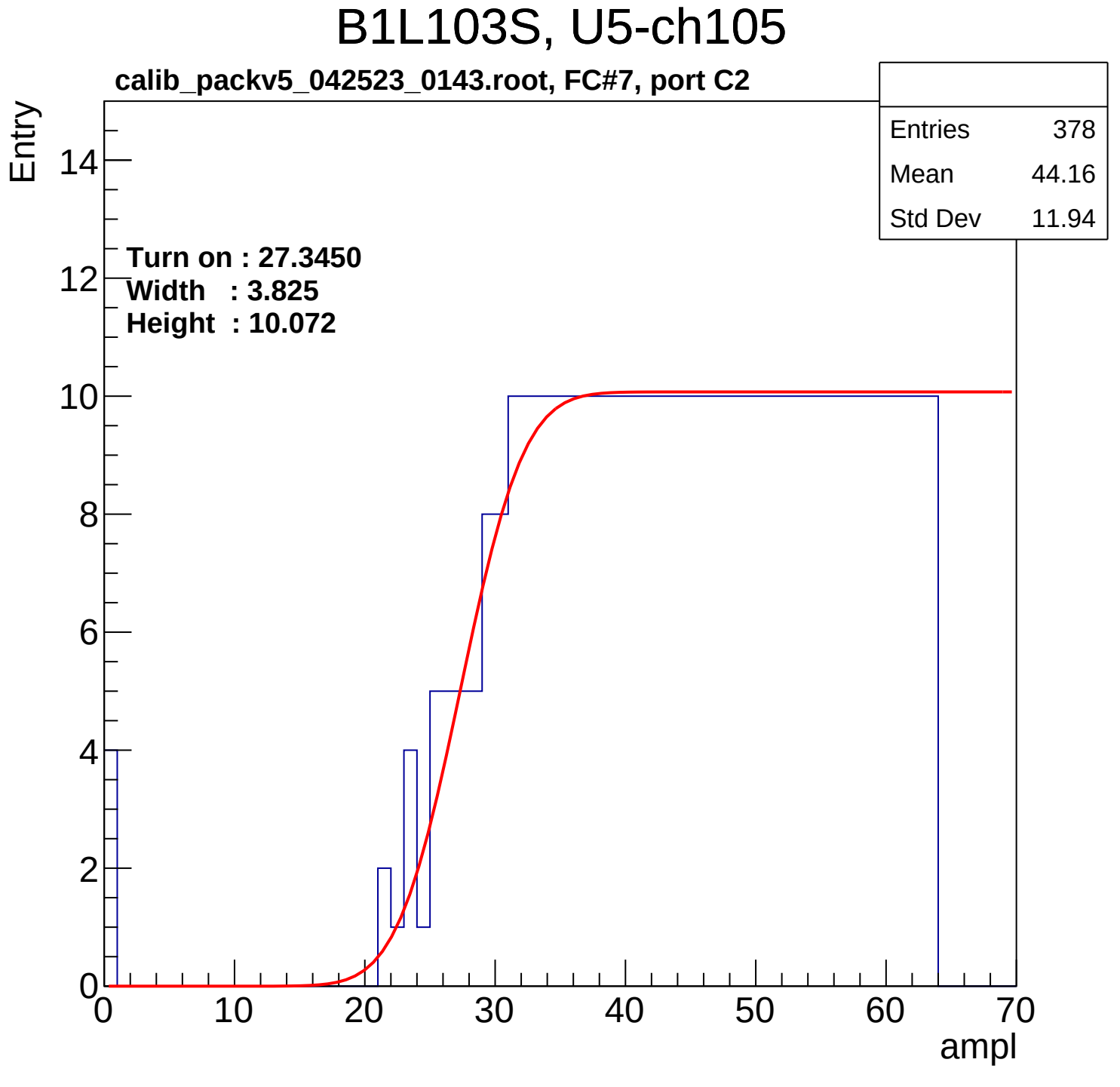

B1L103S, U5-ch100
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.33
Std Dev 11.81
Turn on : 26.8364
Width : 4.404
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

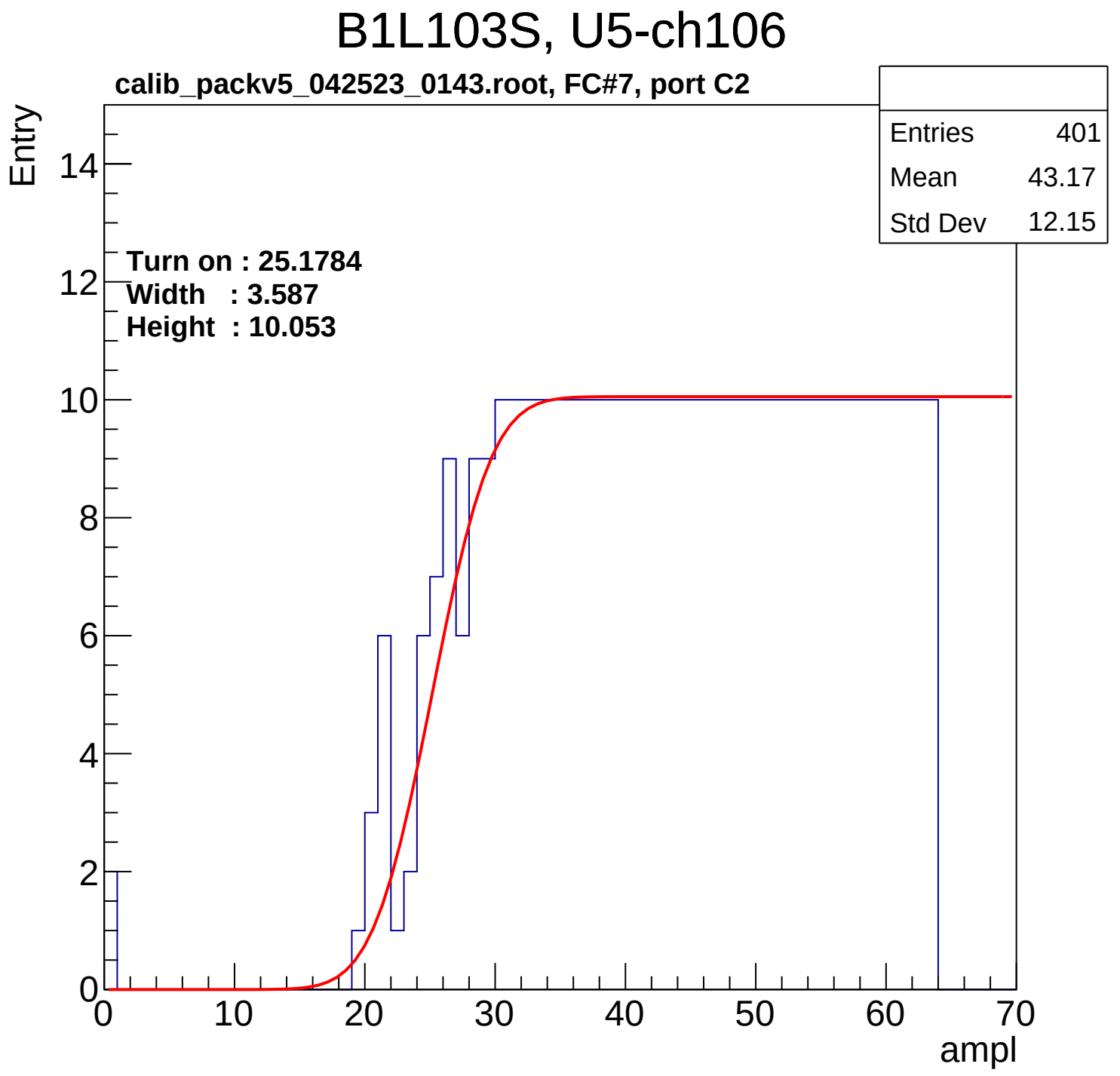

B1L103S, U5-ch101
calib_packv5_042523_0143.root, FC#7, port C2
Entries 385
Mean 43.86
Std Dev 12.03
Turn on : 26.1619
Width : 2.956
Height : 9.987
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

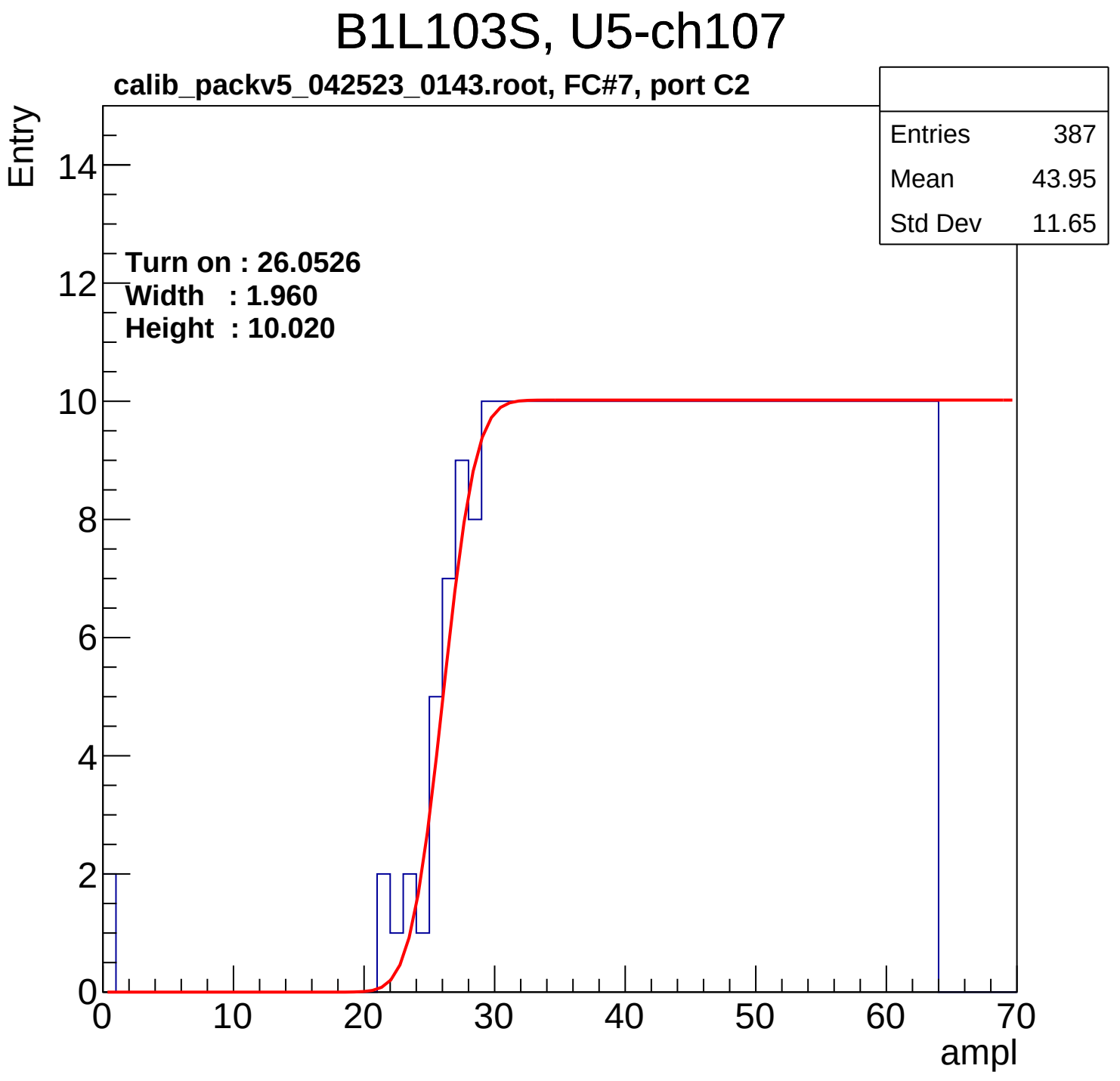

B1L103S, U5-ch102
calib_packv5_042523_0143.root, FC#7, port C2
Entries 390
Mean 43.66
Std Dev 11.94
Turn on : 25.5986
Width : 4.127
Height : 10.008
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

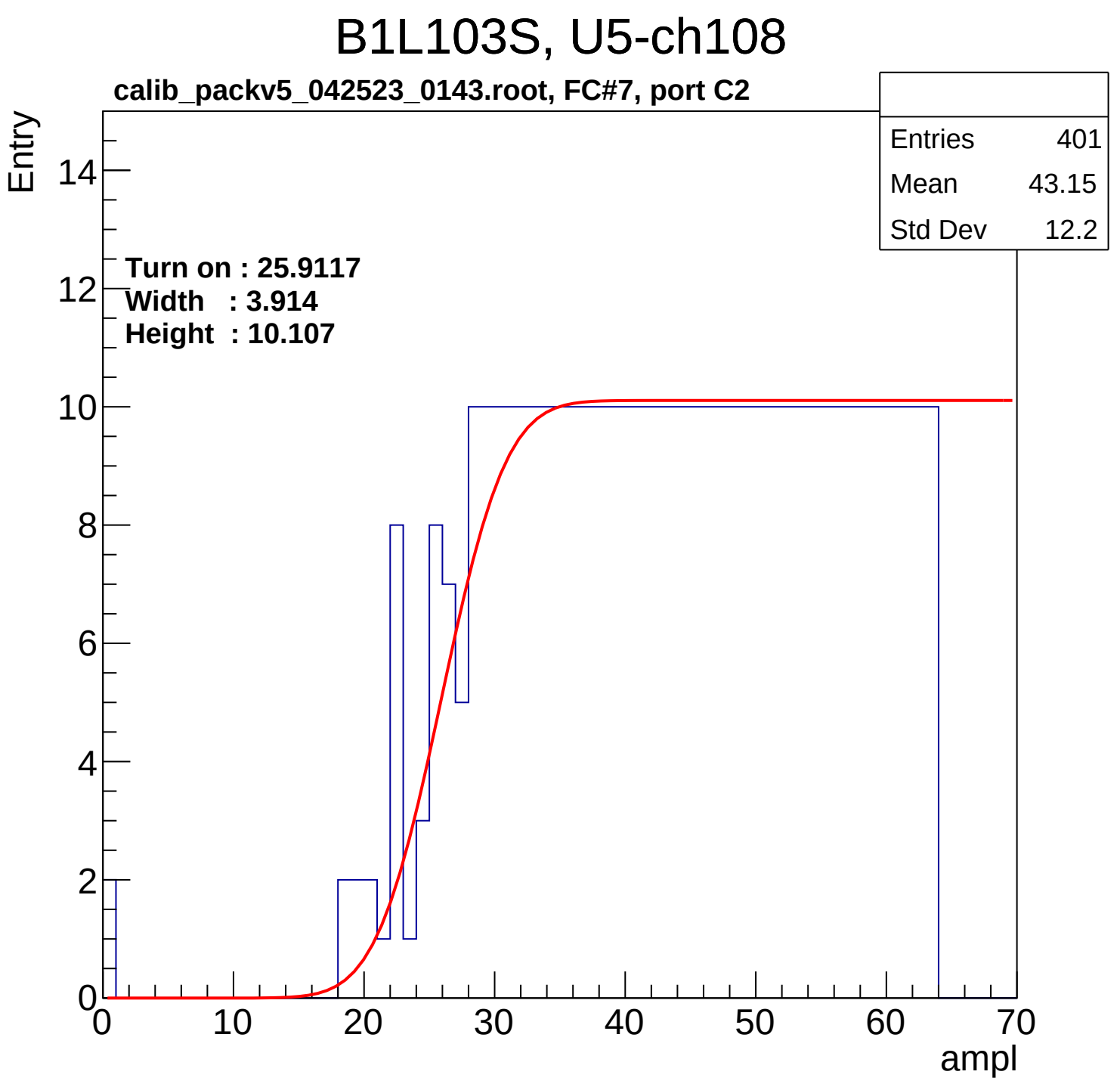

B1L103S, U5-ch103
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.35
Std Dev 11.35
Turn on : 26.1904
Width : 4.205
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

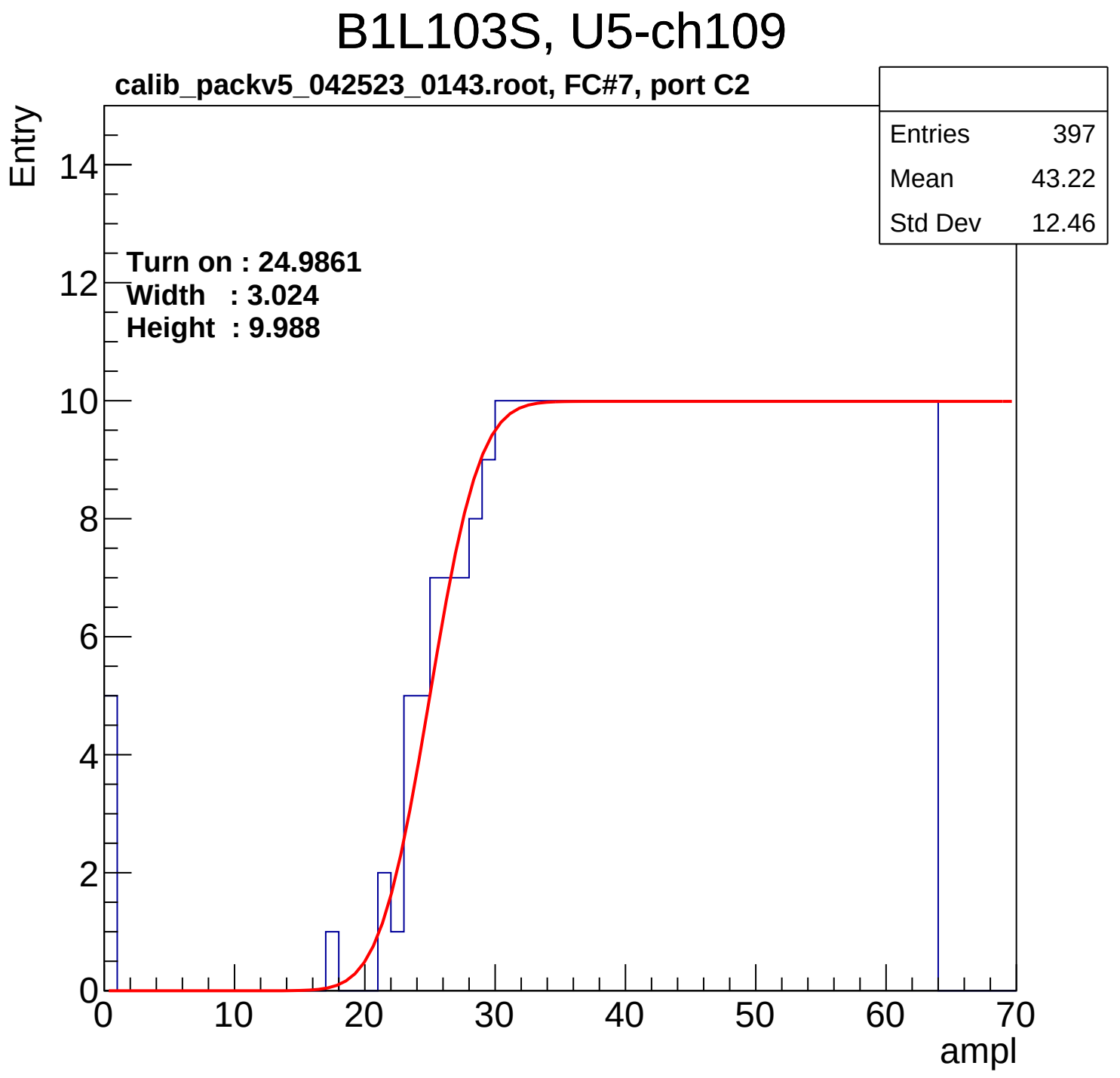

B1L103S, U5-ch104
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.29
Std Dev 11.4
Turn on : 27.9540
Width : 3.499
Height : 10.106
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

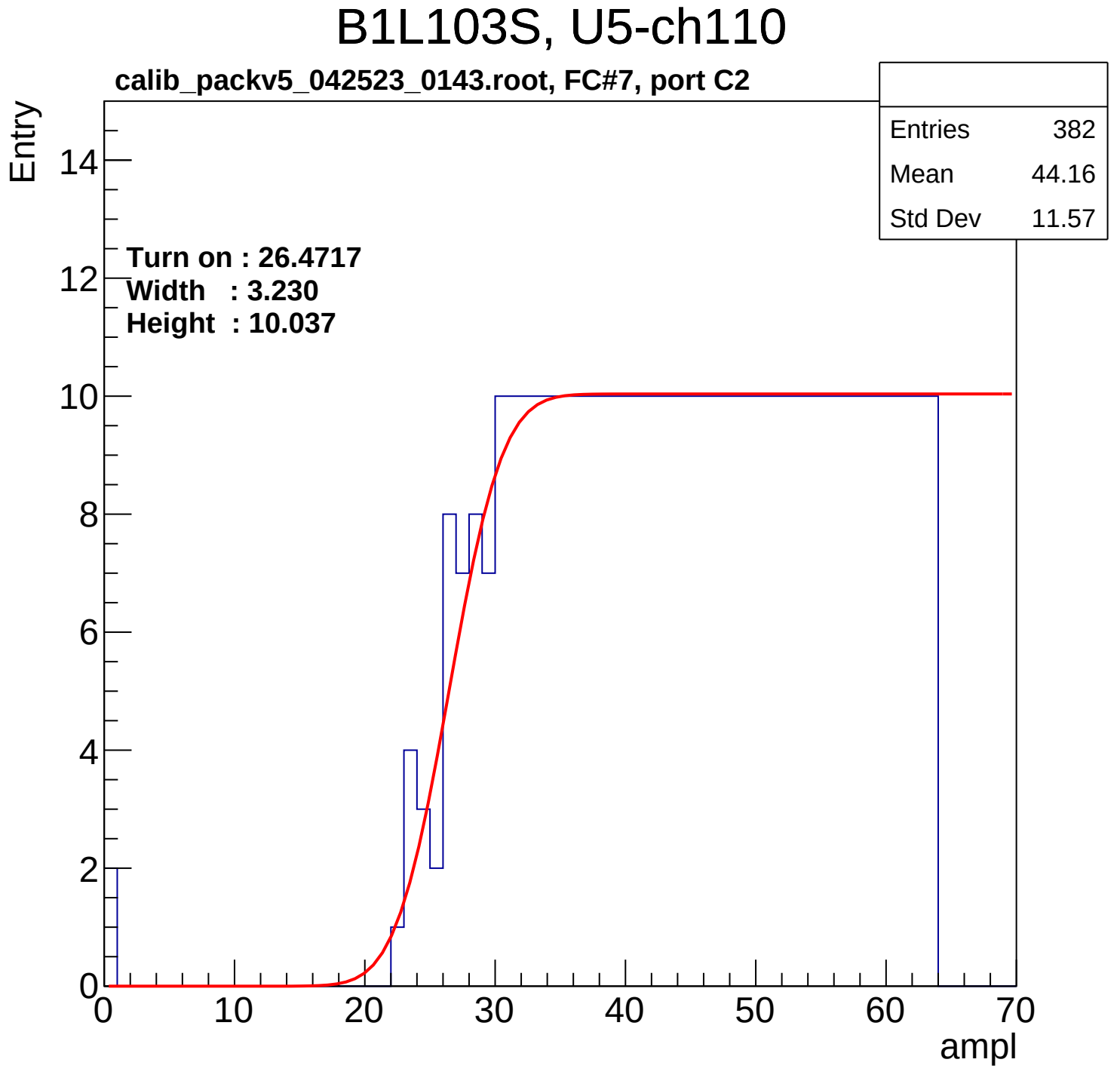

B1L103S, U5-ch105
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.16
Std Dev 11.94
Turn on : 27.3450
Width : 3.825
Height : 10.072
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

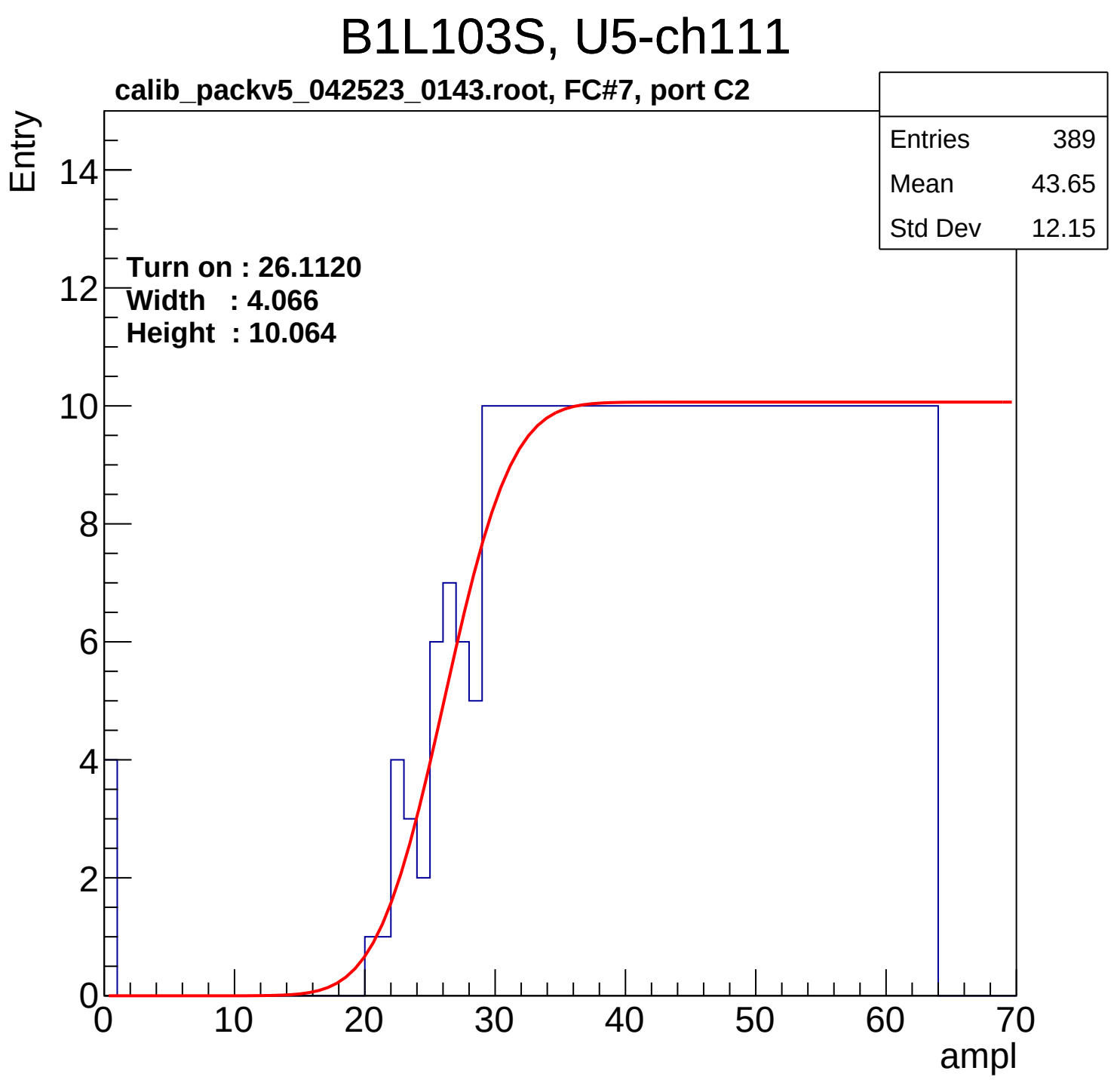

B1L103S, U5-ch106
calib_packv5_042523_0143.root, FC#7, port C2
Entries 401
Mean 43.17
Std Dev 12.15
Turn on : 25.1784
Width : 3.587
Height : 10.053
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

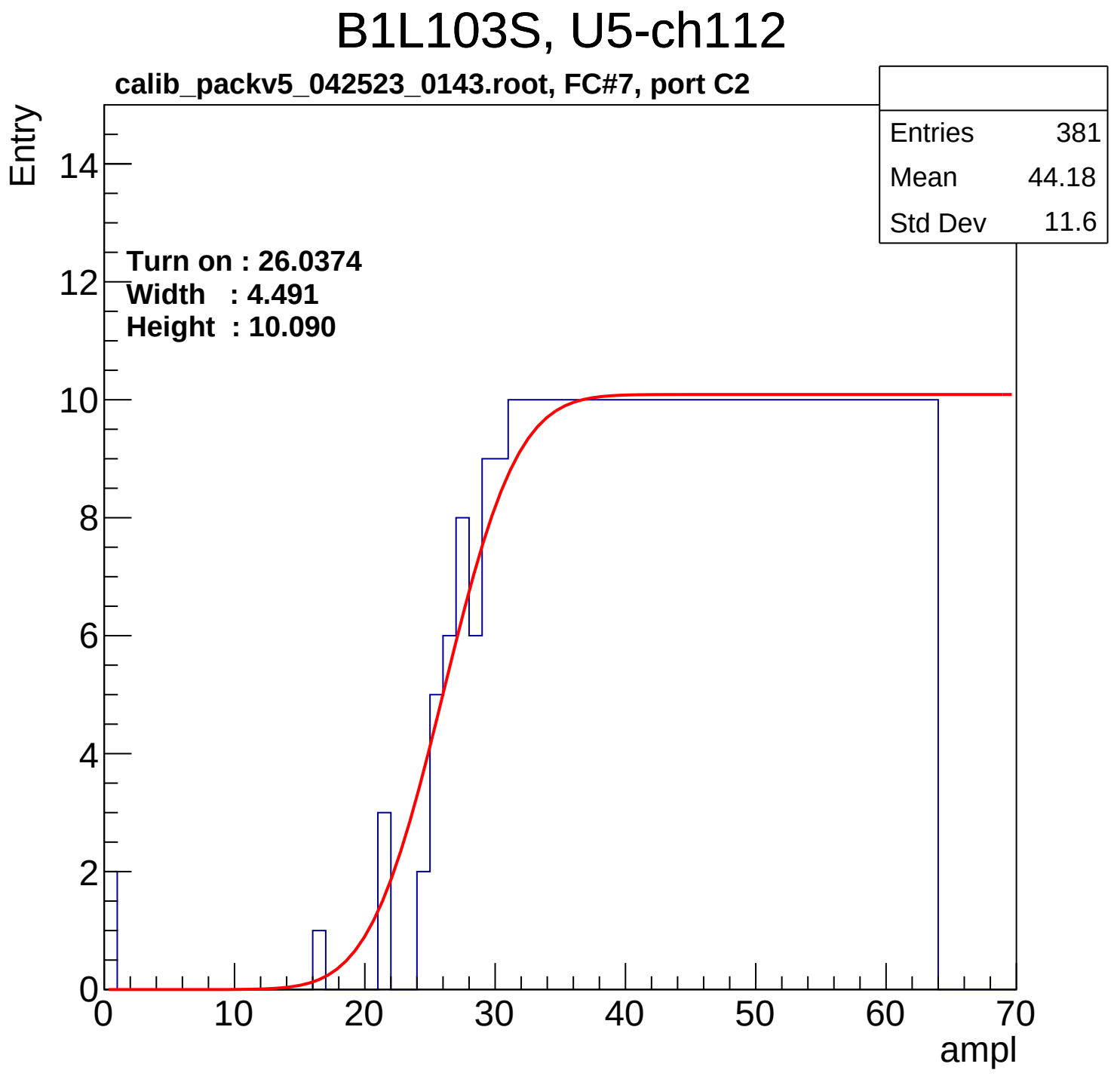

B1L103S, U5-ch107
calib_packv5_042523_0143.root, FC#7, port C2
Entries 387
Mean 43.95
Std Dev 11.65
Turn on : 26.0526
Width : 1.960
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

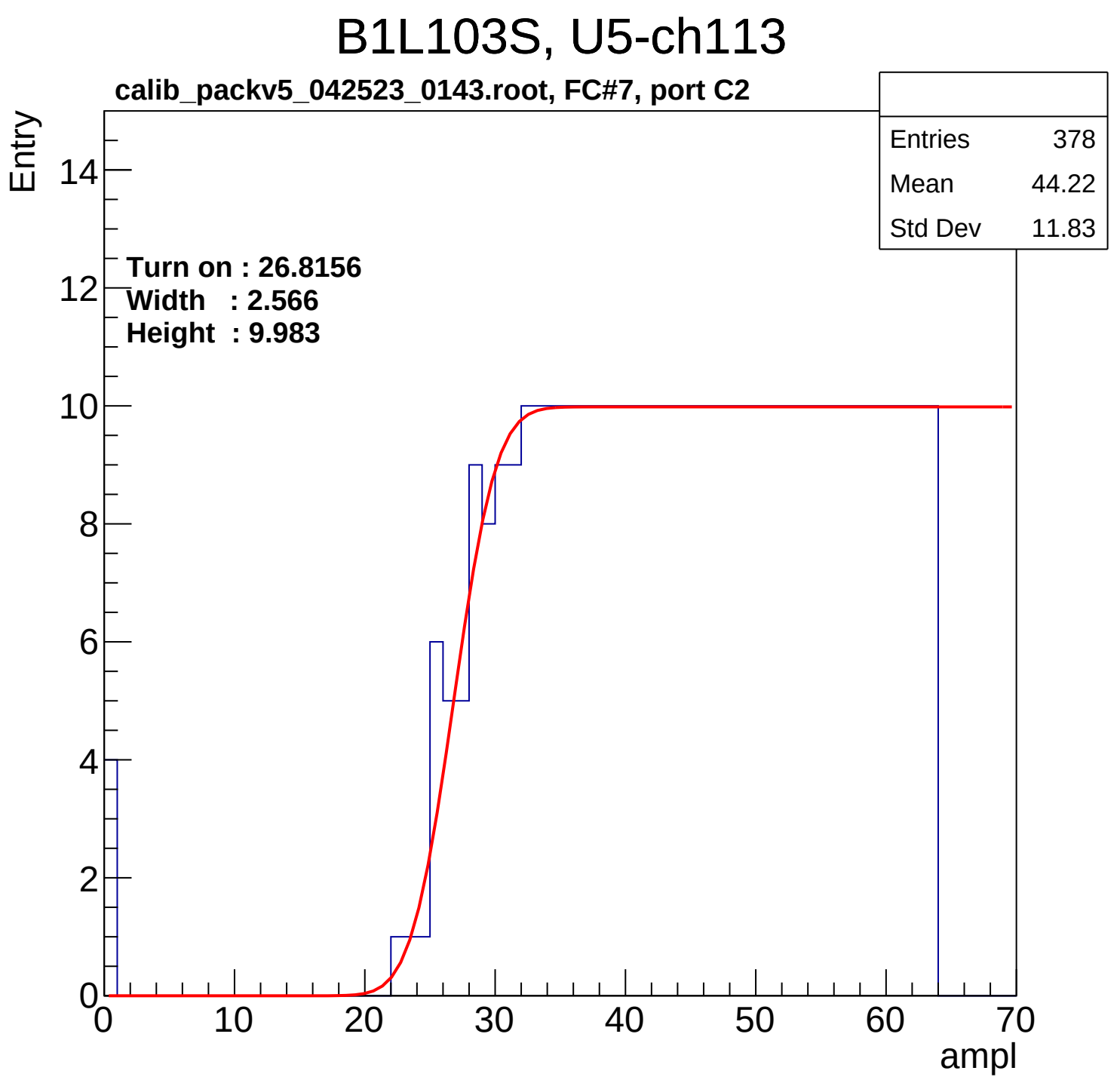

B1L103S, U5-ch108
calib_packv5_042523_0143.root, FC#7, port C2
Entries 401
Mean 43.15
Std Dev 12.2
Turn on : 25.9117
Width : 3.914
Height : 10.107
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

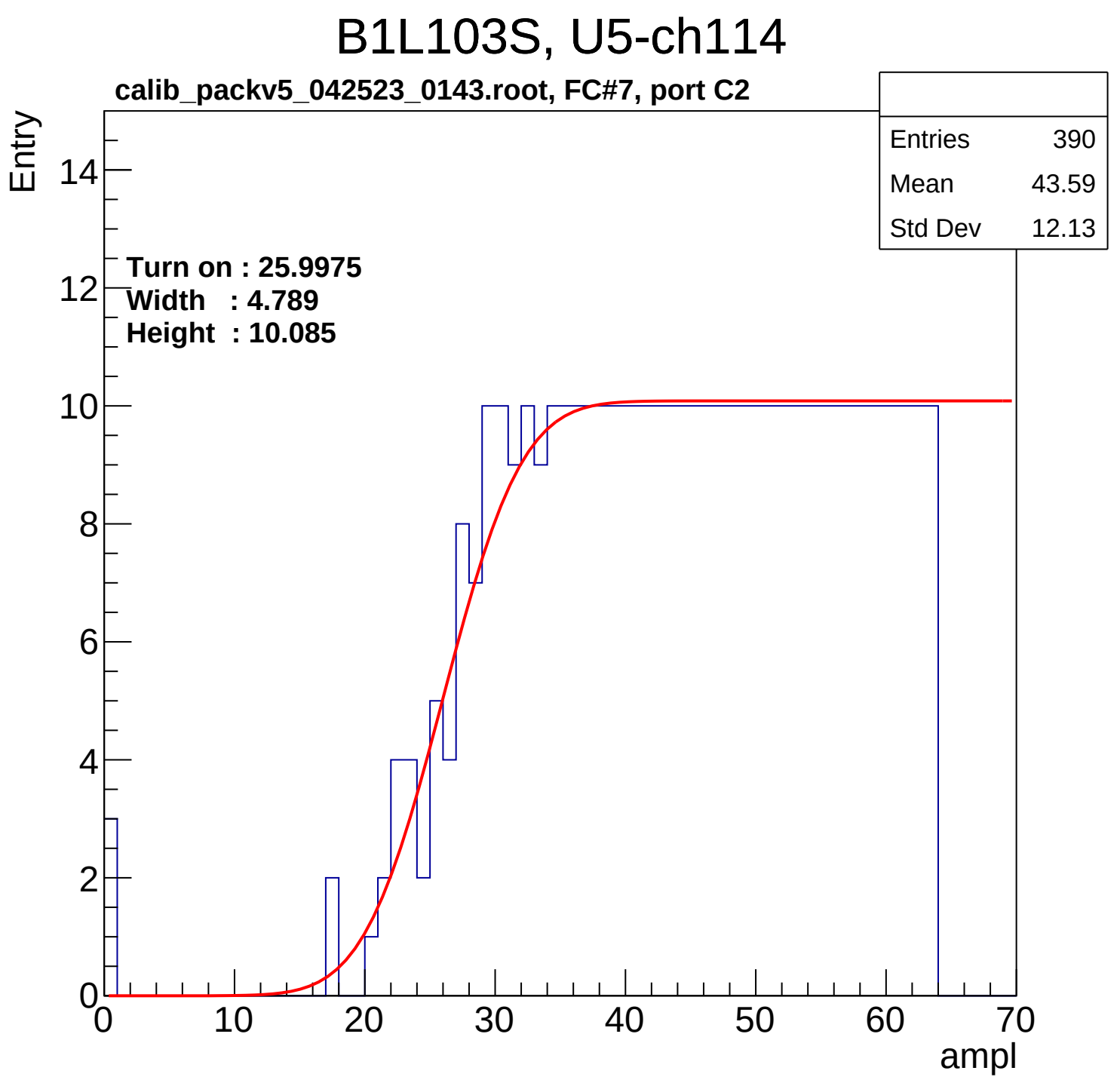

B1L103S, U5-ch109
calib_packv5_042523_0143.root, FC#7, port C2
Entries 397
Mean 43.22
Std Dev 12.46
Turn on : 24.9861
Width : 3.024
Height : 9.988
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

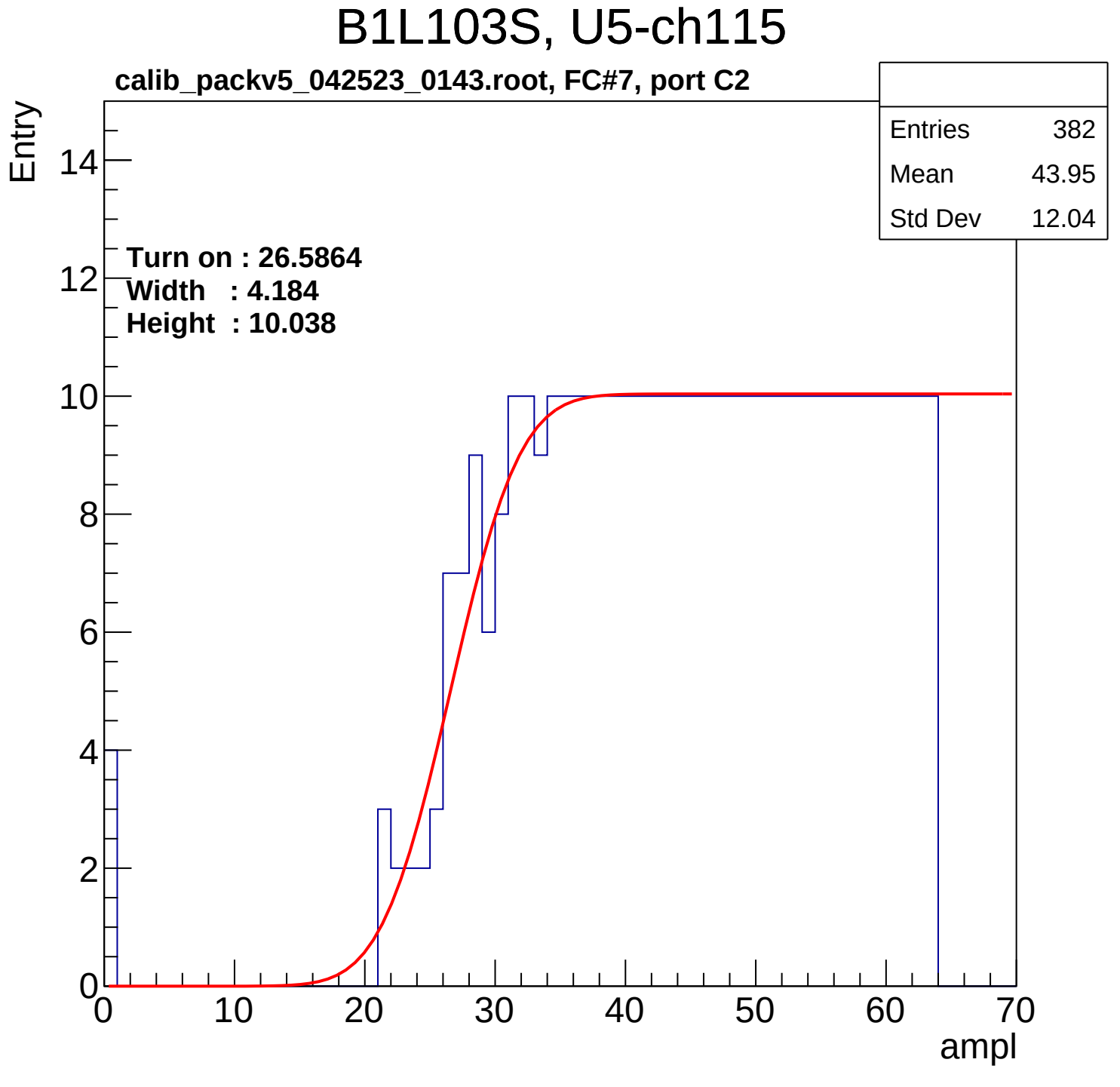

B1L103S, U5-ch110
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 44.16
Std Dev 11.57
Turn on : 26.4717
Width : 3.230
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

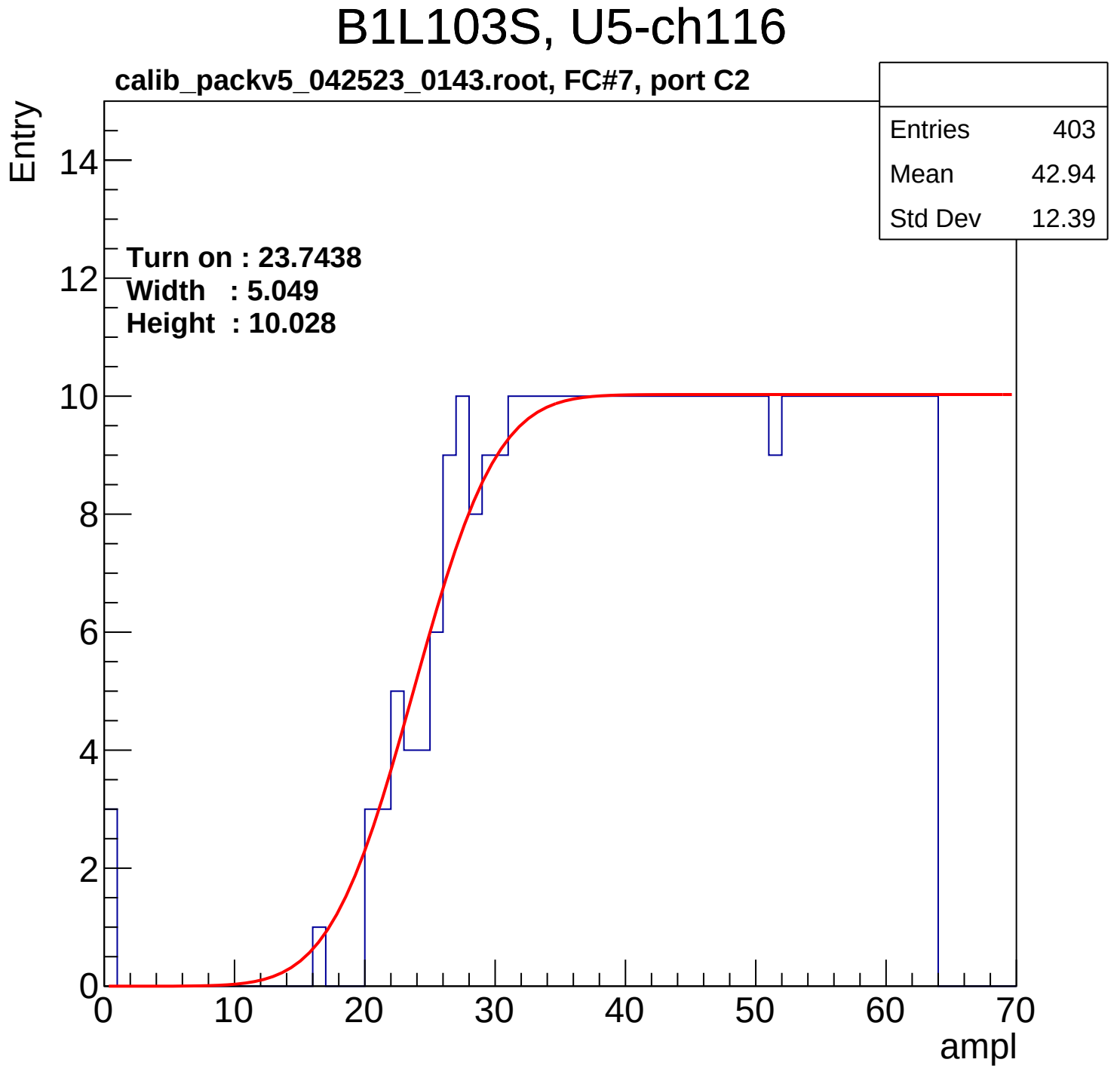

B1L103S, U5-ch111
calib_packv5_042523_0143.root, FC#7, port C2
Entries 389
Mean 43.65
Std Dev 12.15
Turn on : 26.1120
Width : 4.066
Height : 10.064
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

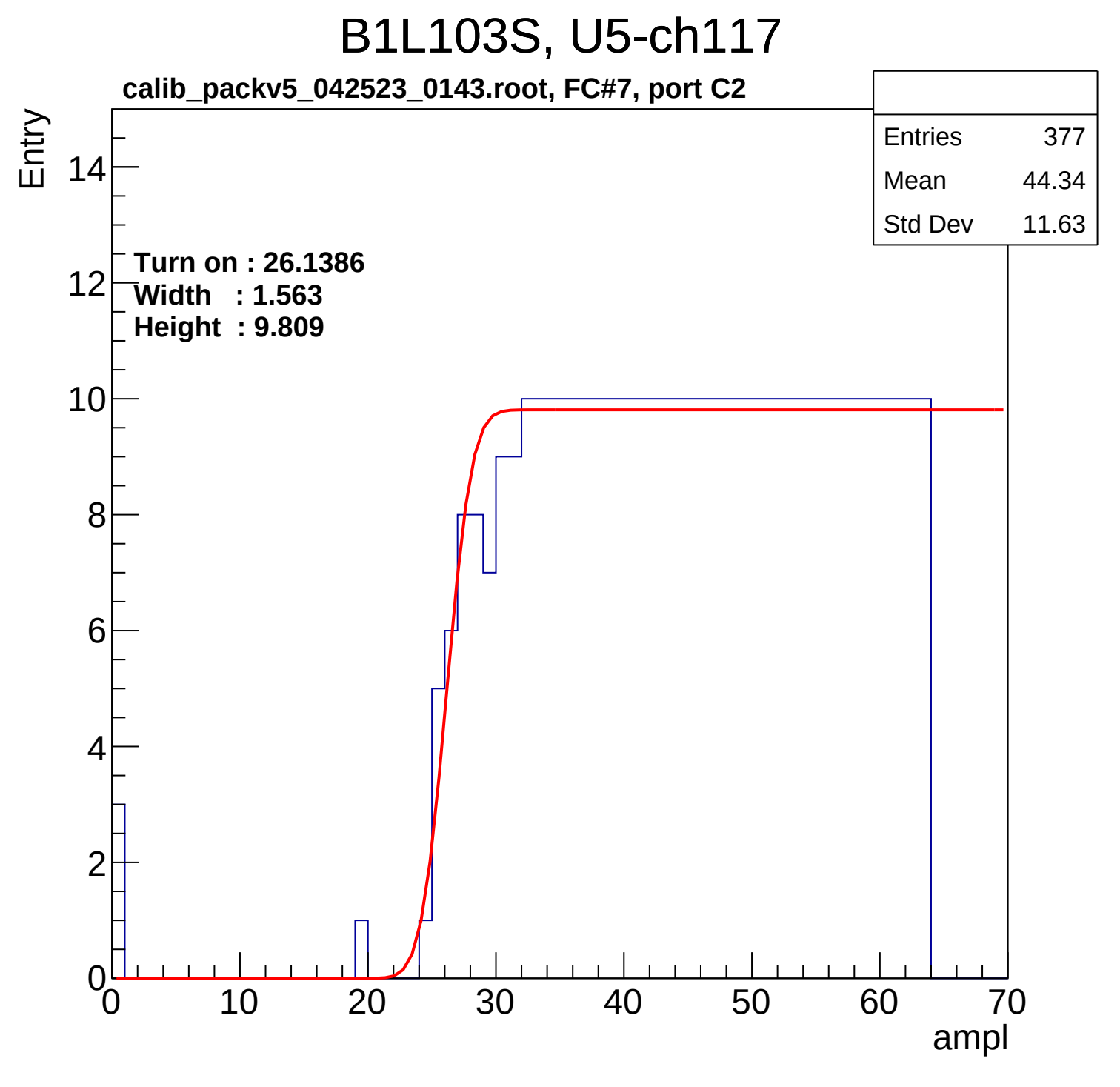

B1L103S, U5-ch112
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.18
Std Dev 11.6
Turn on : 26.0374
Width : 4.491
Height : 10.090
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

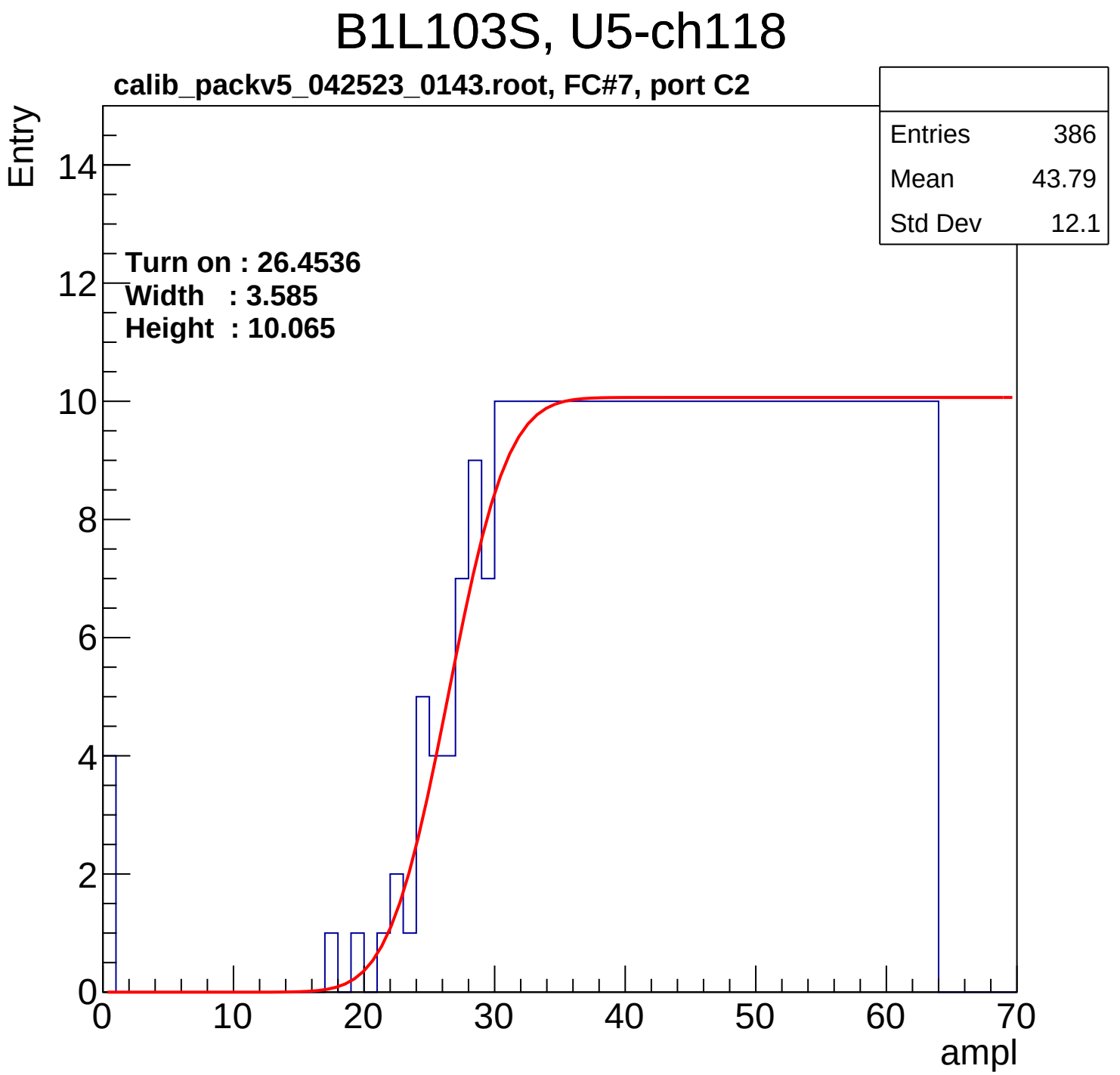

B1L103S, U5-ch113
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.22
Std Dev 11.83
Turn on : 26.8156
Width : 2.566
Height : 9.983
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

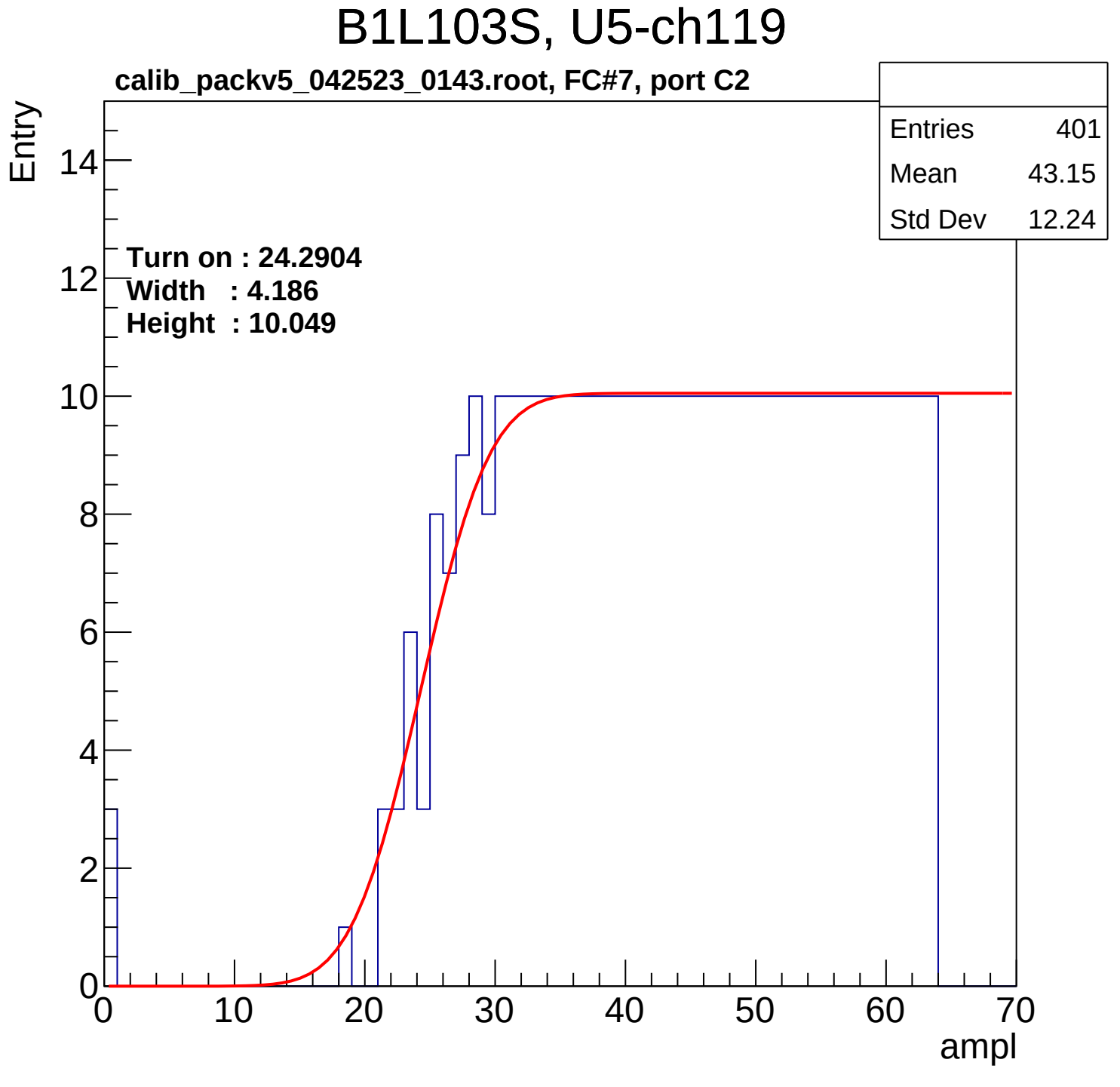

B1L103S, U5-ch114
calib_packv5_042523_0143.root, FC#7, port C2
Entries 390
Mean 43.59
Std Dev 12.13
Turn on : 25.9975
Width : 4.789
Height : 10.085
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

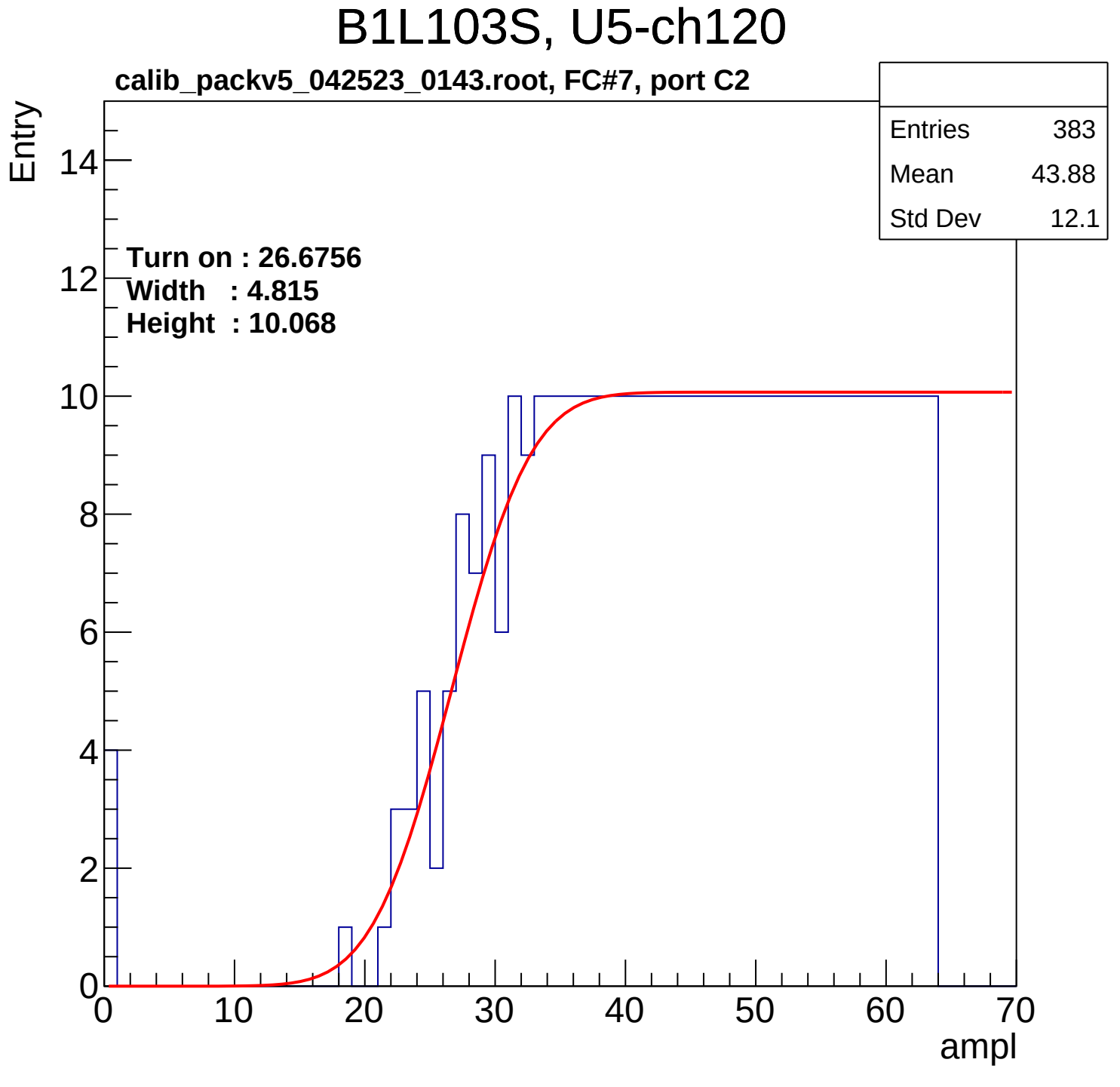

B1L103S, U5-ch115
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 43.95
Std Dev 12.04
Turn on : 26.5864
Width : 4.184
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

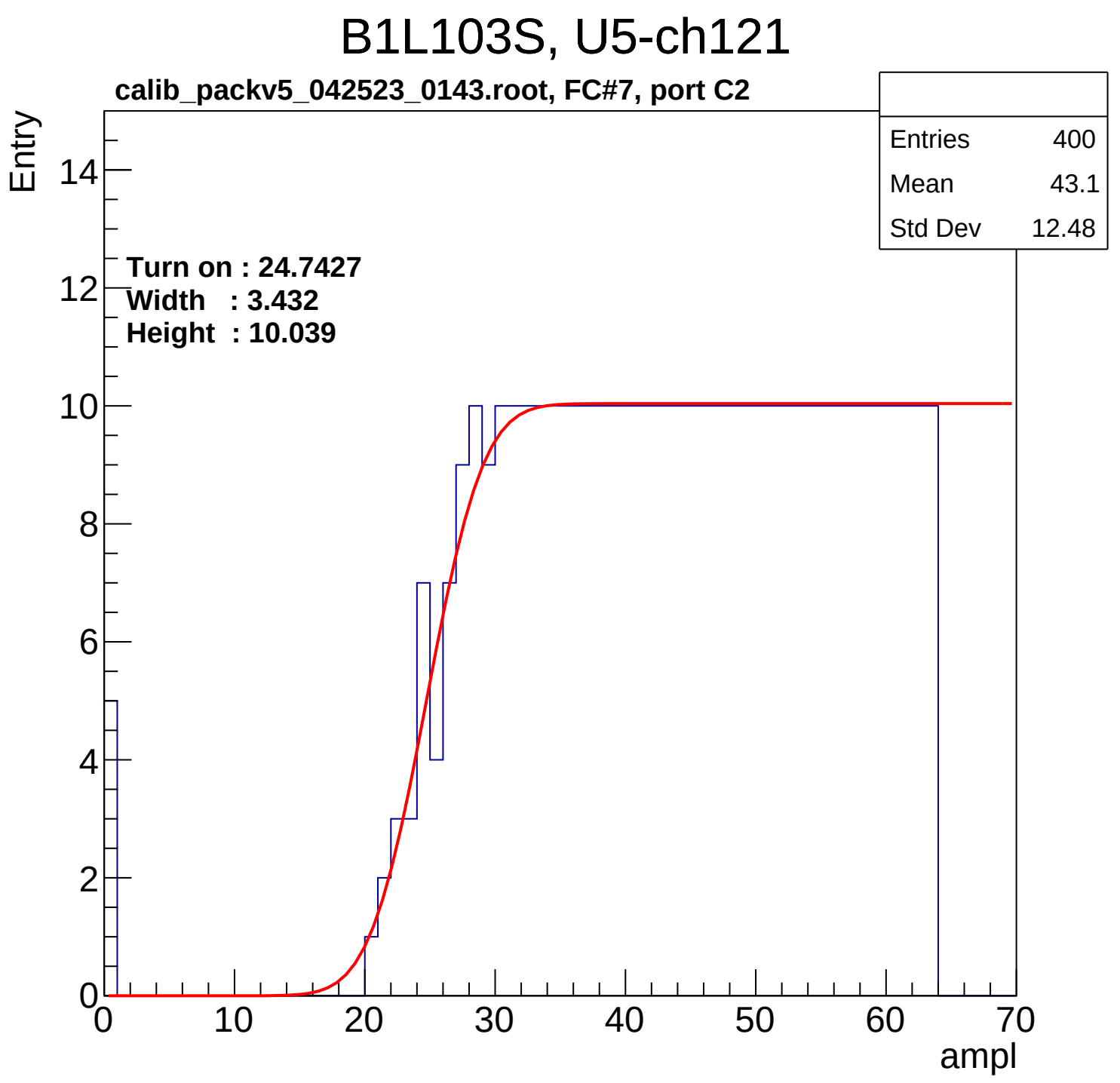

B1L103S, U5-ch116
calib_packv5_042523_0143.root, FC#7, port C2
Entries 403
Mean 42.94
Std Dev 12.39
Turn on : 23.7438
Width : 5.049
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

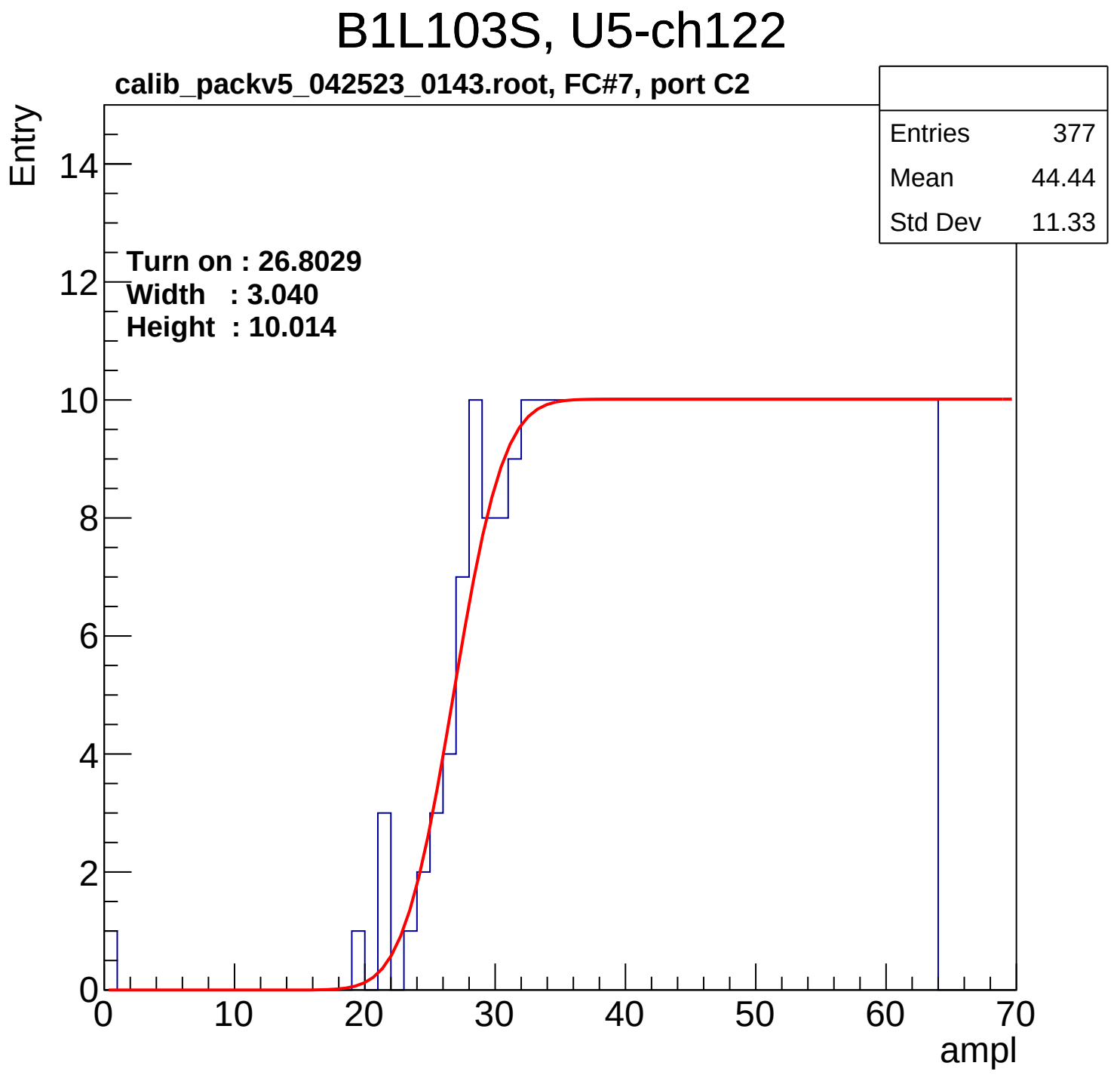

B1L103S, U5-ch117
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.34
Std Dev 11.63
Turn on : 26.1386
Width : 1.563
Height : 9.809
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

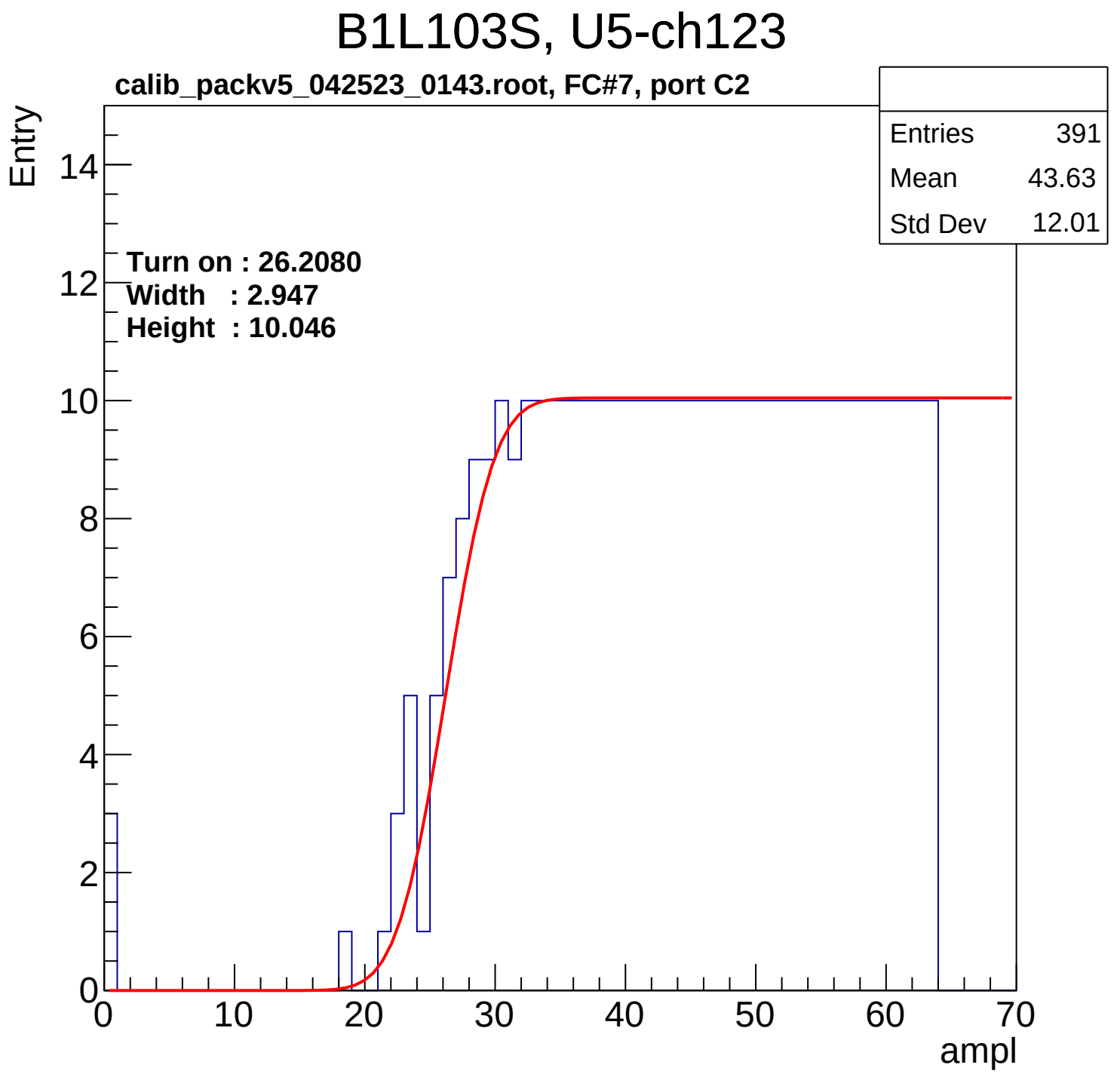

B1L103S, U5-ch118
calib_packv5_042523_0143.root, FC#7, port C2
Entries 386
Mean 43.79
Std Dev 12.1
Turn on : 26.4536
Width : 3.585
Height : 10.065
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

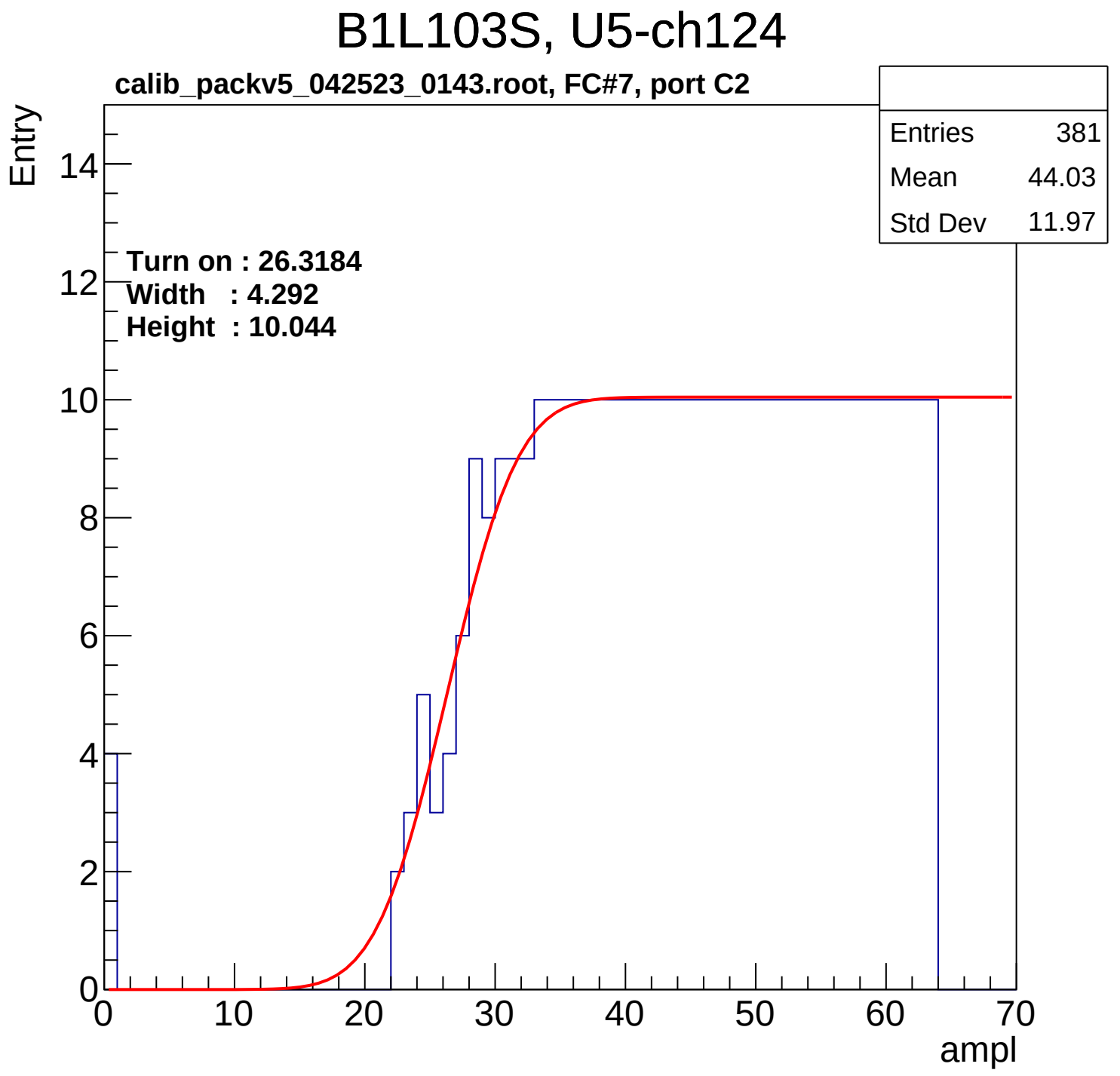

B1L103S, U5-ch119
calib_packv5_042523_0143.root, FC#7, port C2
Entries 401
Mean 43.15
Std Dev 12.24
Turn on : 24.2904
Width : 4.186
Height : 10.049
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

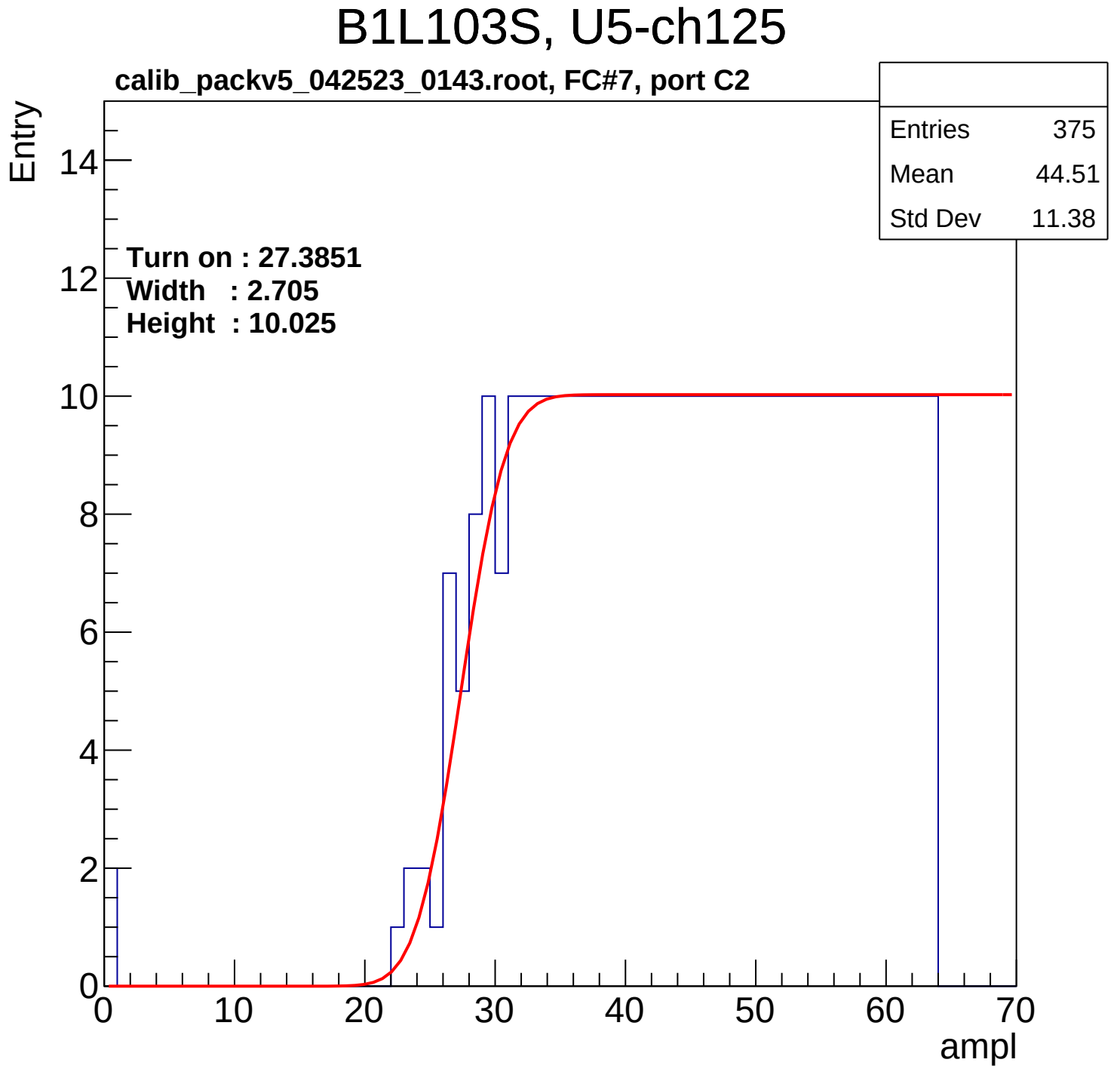

B1L103S, U5-ch120
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 43.88
Std Dev 12.1
Turn on : 26.6756
Width : 4.815
Height : 10.068
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

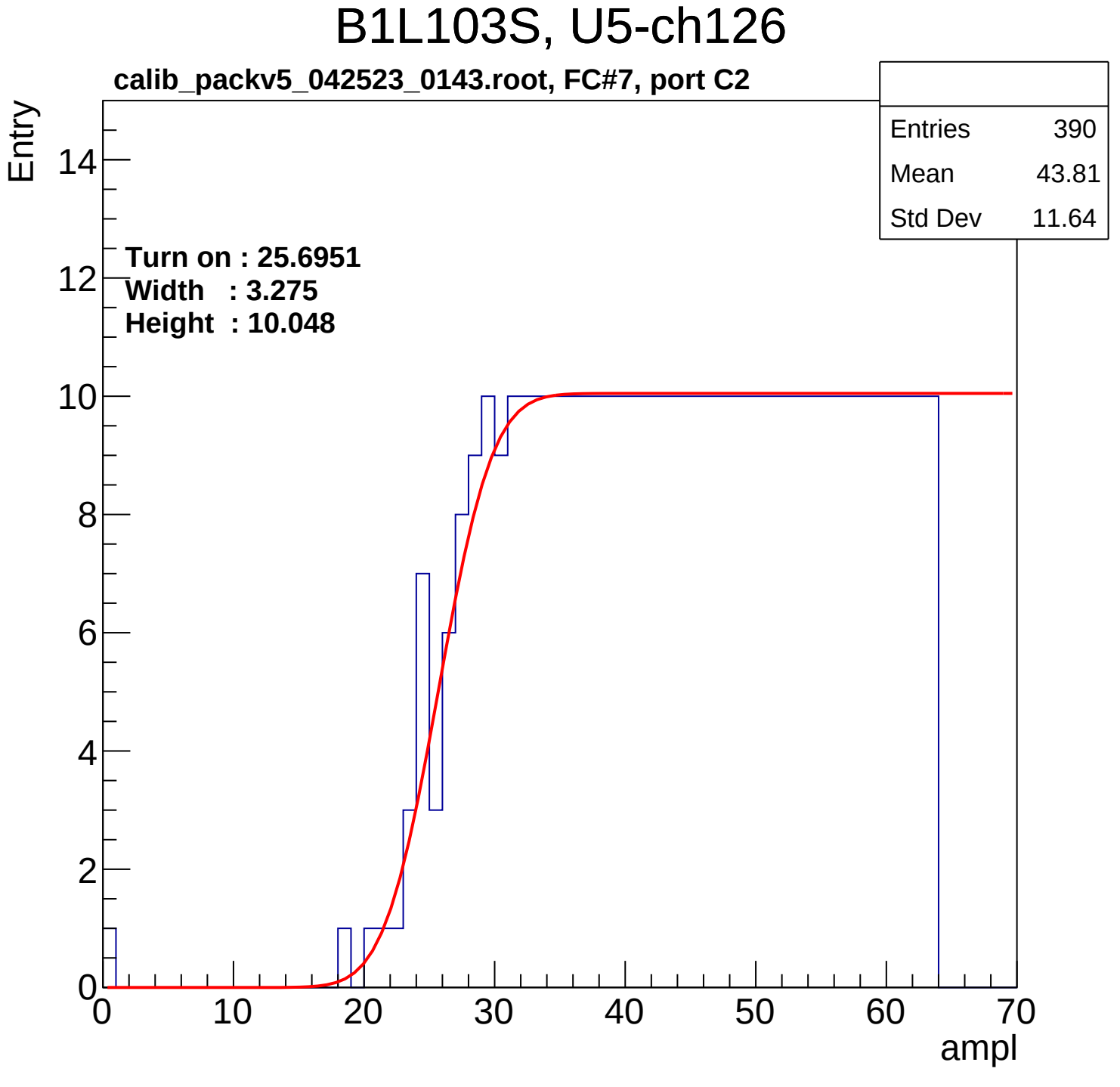

B1L103S, U5-ch121
calib_packv5_042523_0143.root, FC#7, port C2
Entries 400
Mean 43.1
Std Dev 12.48
Turn on : 24.7427
Width : 3.432
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

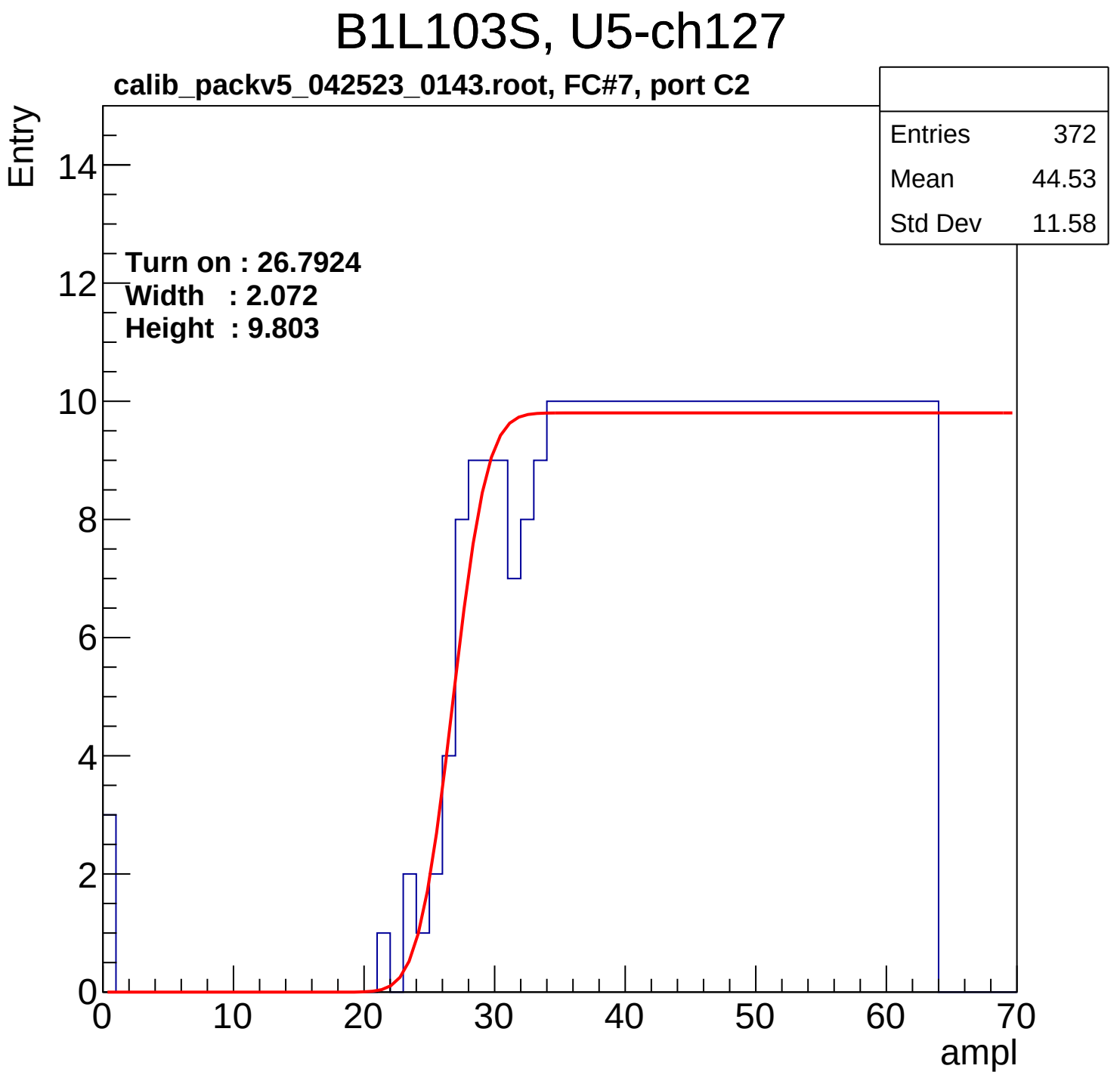

B1L103S, U5-ch122
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.44
Std Dev 11.33
Turn on : 26.8029
Width : 3.040
Height : 10.014
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

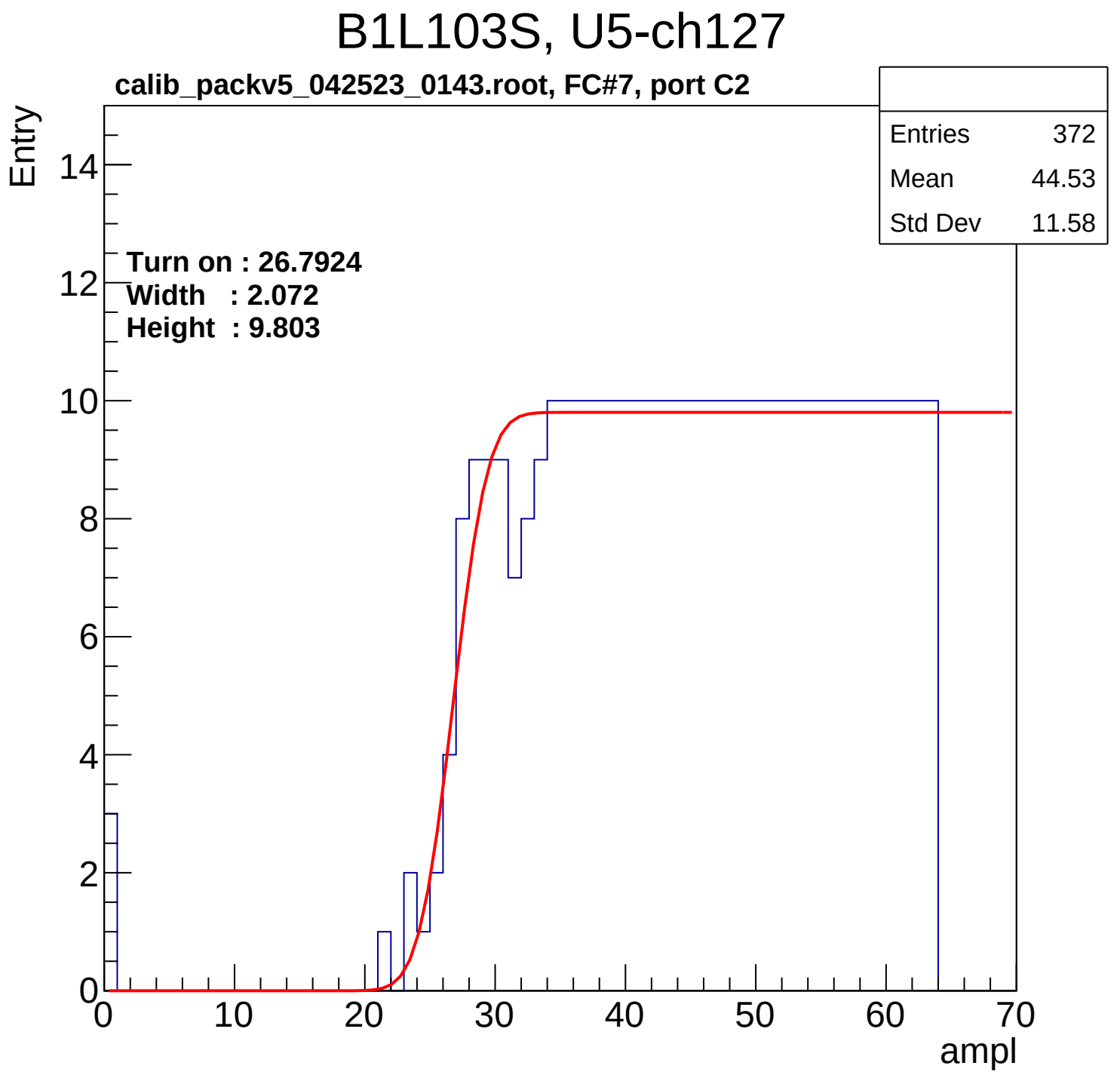

B1L103S, U5-ch123
calib_packv5_042523_0143.root, FC#7, port C2
Entries 391
Mean 43.63
Std Dev 12.01
Turn on : 26.2080
Width : 2.947
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U5-ch124
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.03
Std Dev 11.97
Turn on : 26.3184
Width : 4.292
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U5-ch125
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.51
Std Dev 11.38
Turn on : 27.3851
Width : 2.705
Height : 10.025
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U5-ch126
calib_packv5_042523_0143.root, FC#7, port C2
Entries 390
Mean 43.81
Std Dev 11.64
Turn on : 25.6951
Width : 3.275
Height : 10.048
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U5-ch127
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.53
Std Dev 11.58
Turn on : 26.7924
Width : 2.072
Height : 9.803
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U5-ch127
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.53
Std Dev 11.58
Turn on : 26.7924
Width : 2.072
Height : 9.803
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70