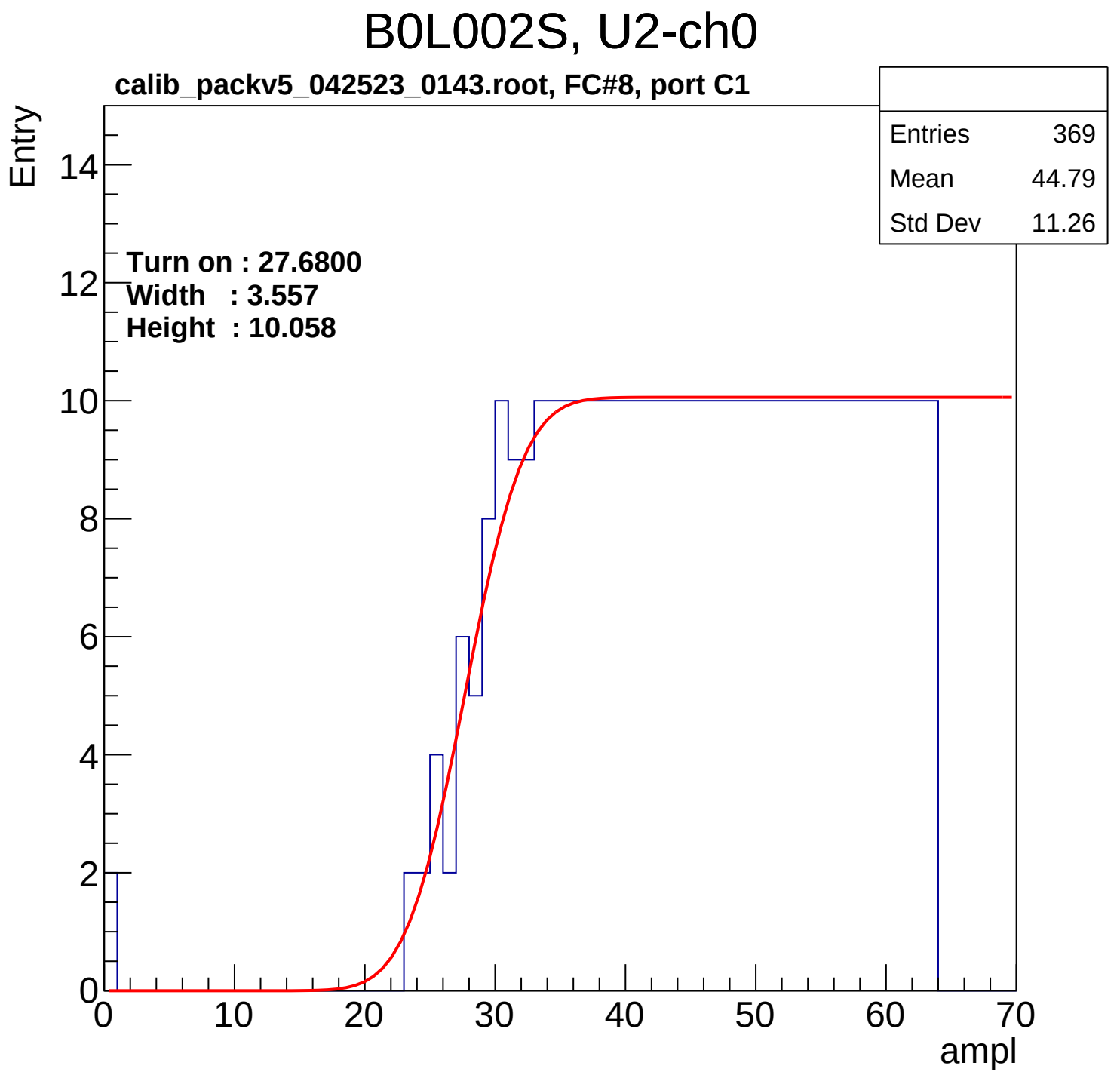
B0L002S, U2-ch0
calib_packv5_042523_0143.root, FC#8, port C1
Entries 369
Mean 44.79
Std Dev 11.26
Turn on : 27.6800
Width : 3.557
Height : 10.058
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ampl
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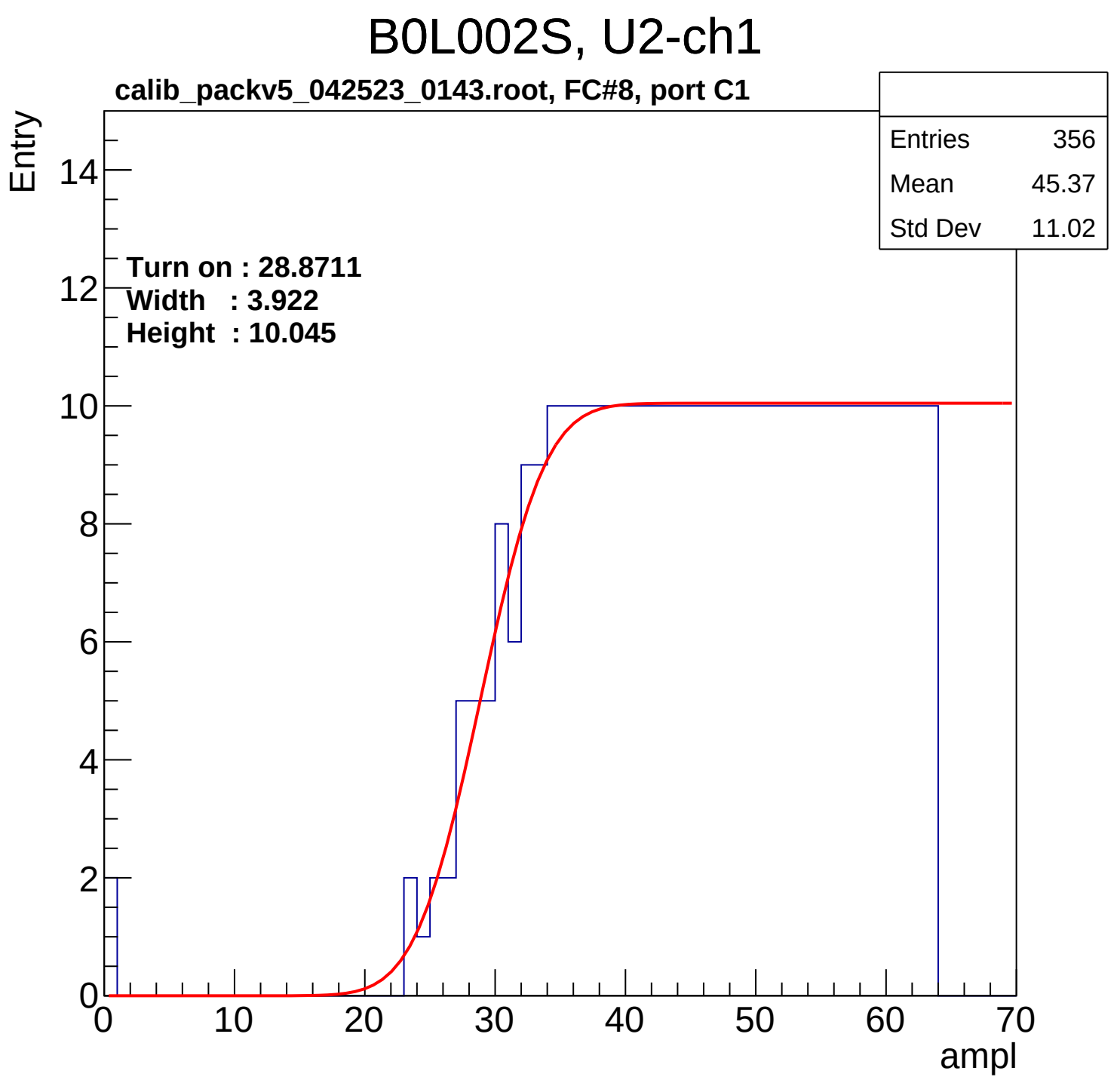
B0L002S, U2-ch1
calib_packv5_042523_0143.root, FC#8, port C1
Entries 356
Mean 45.37
Std Dev 11.02
Turn on : 28.8711
Width : 3.922
Height : 10.045
Entry
ampl
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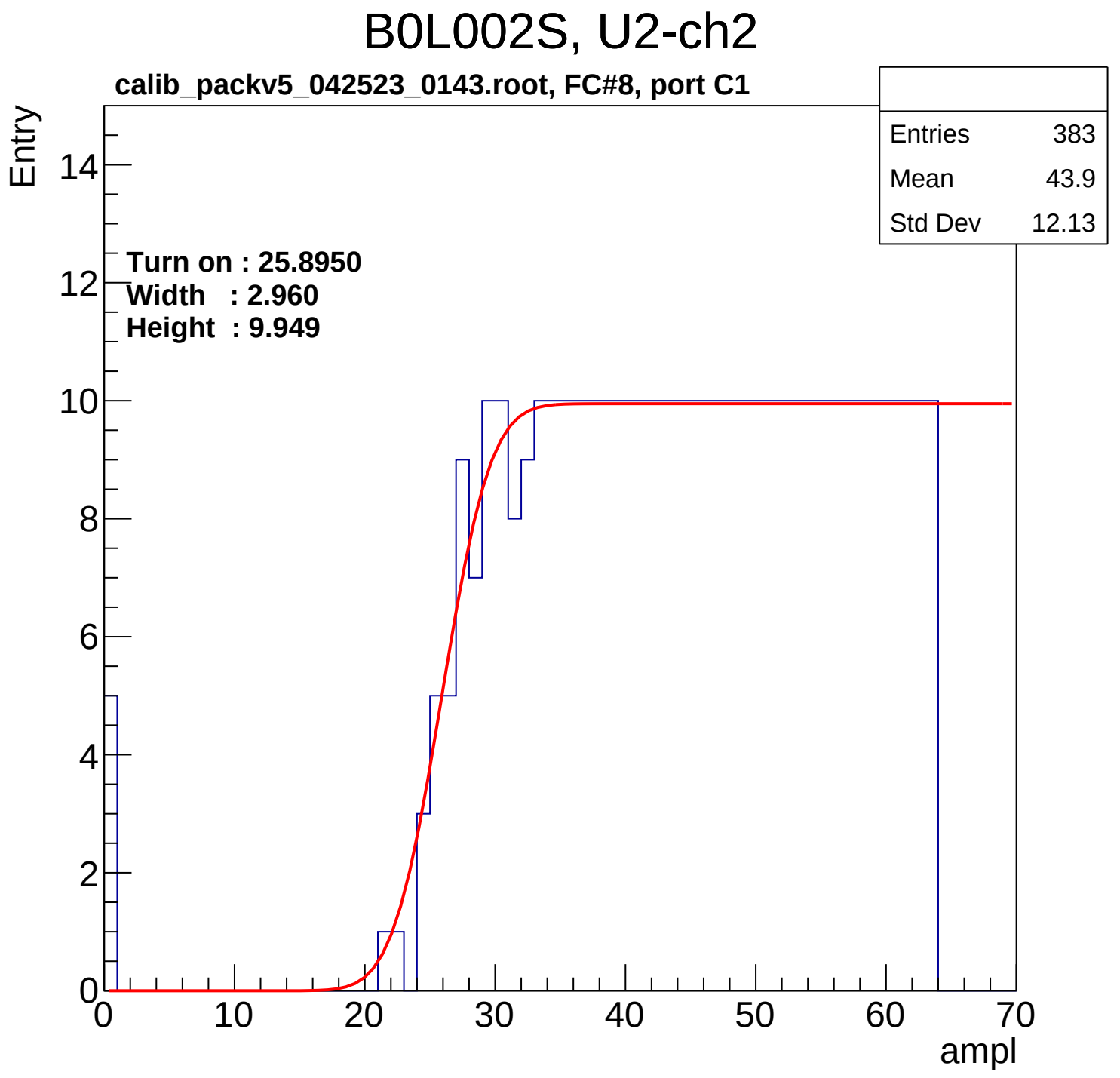
B0L002S, U2-ch2
calib_packv5_042523_0143.root, FC#8, port C1
Entries 383
Mean 43.9
Std Dev 12.13
Turn on : 25.8950
Width : 2.960
Height : 9.949
Entry
ampl
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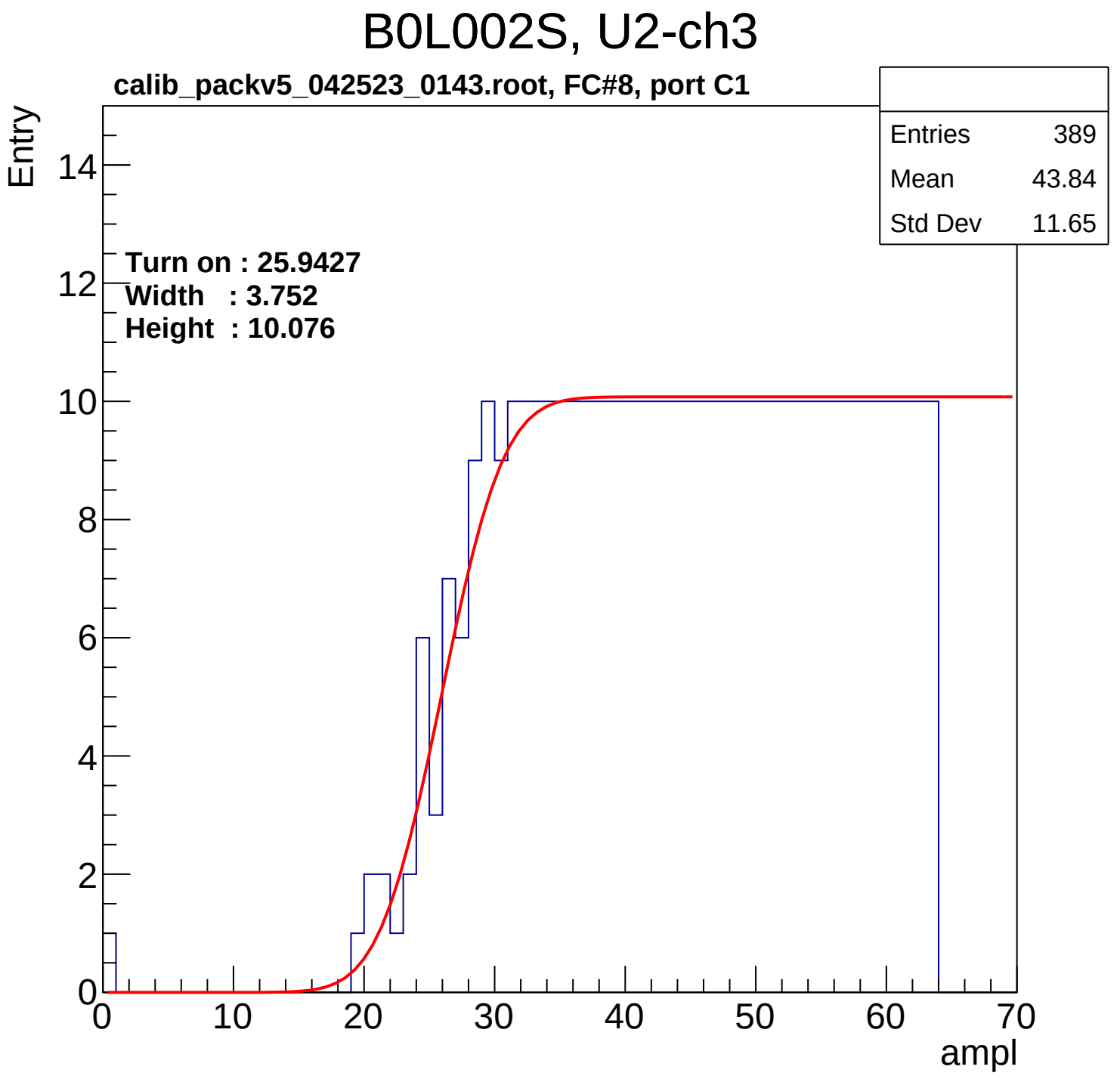
B0L002S, U2-ch3
calib_packv5_042523_0143.root, FC#8, port C1
Entries 389
Mean 43.84
Std Dev 11.65
Turn on : 25.9427
Width : 3.752
Height : 10.076
Entry
ampl
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6
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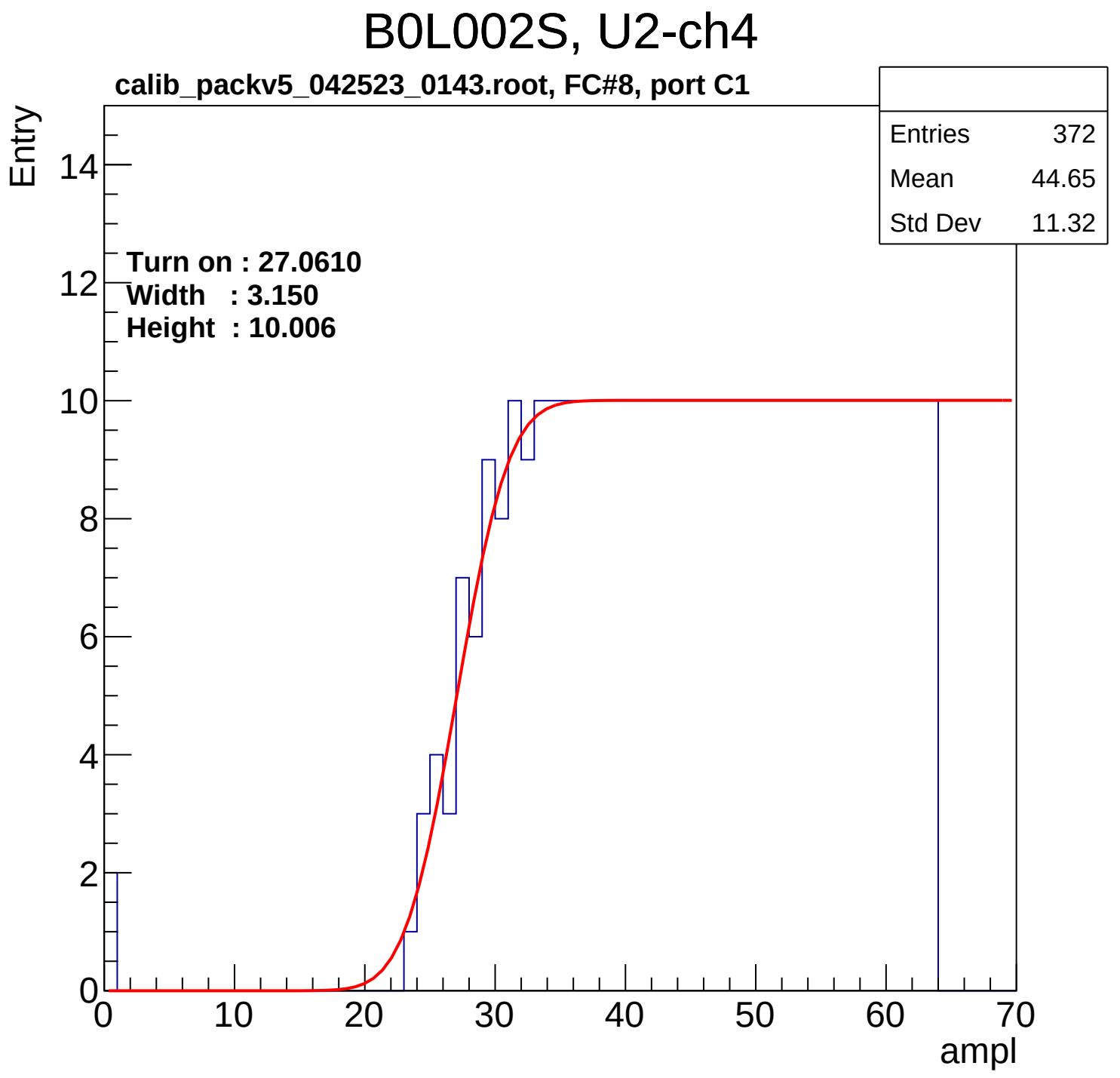
B0L002S, U2-ch4
calib_packv5_042523_0143.root, FC#8, port C1
Entries 372
Mean 44.65
Std Dev 11.32
Turn on : 27.0610
Width : 3.150
Height : 10.006
Entry
ampl
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6
8
10
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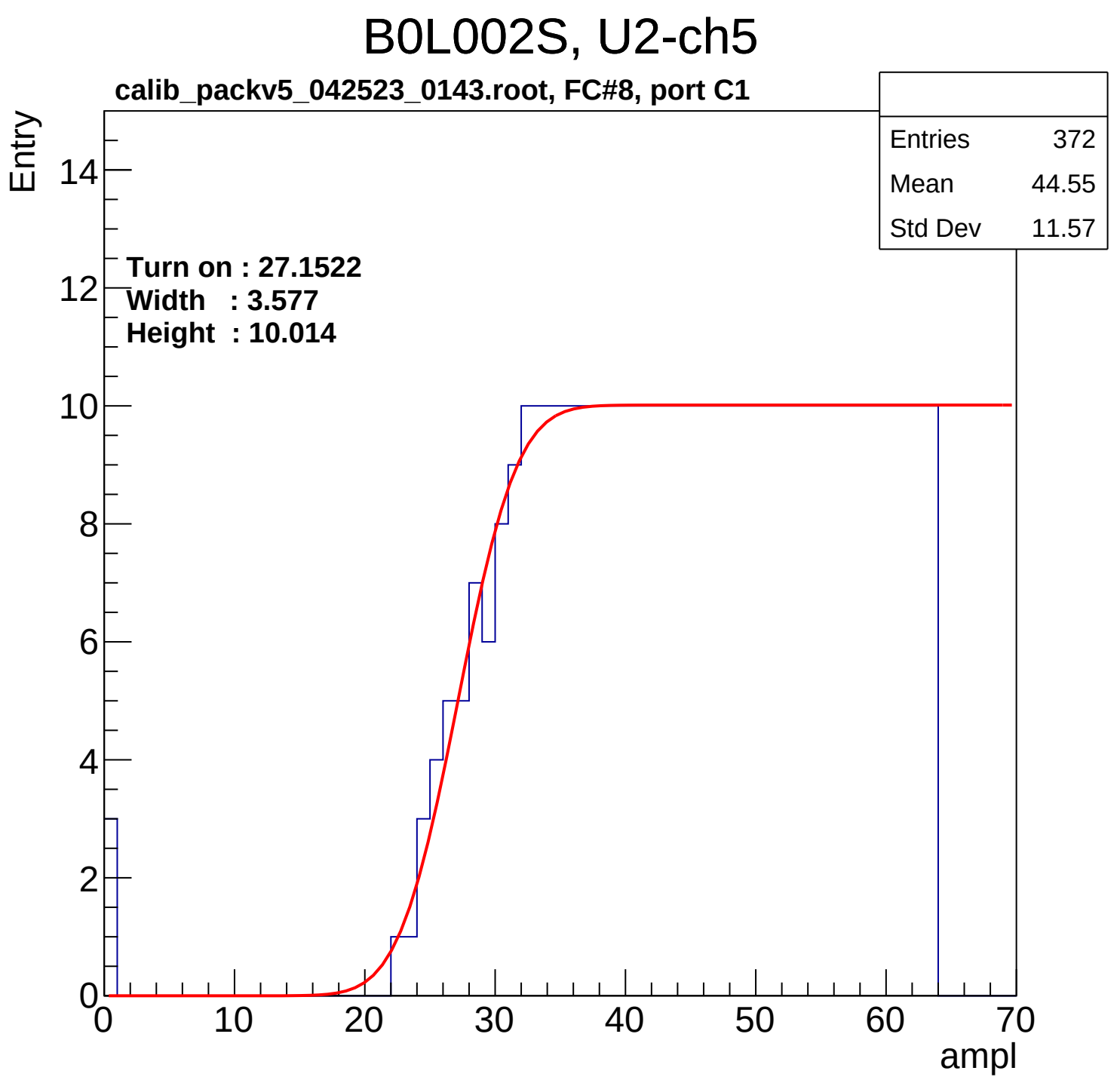
B0L002S, U2-ch5
calib_packv5_042523_0143.root, FC#8, port C1
Entries 372
Mean 44.55
Std Dev 11.57
Turn on : 27.1522
Width : 3.577
Height : 10.014
Entry
ampl
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6
8
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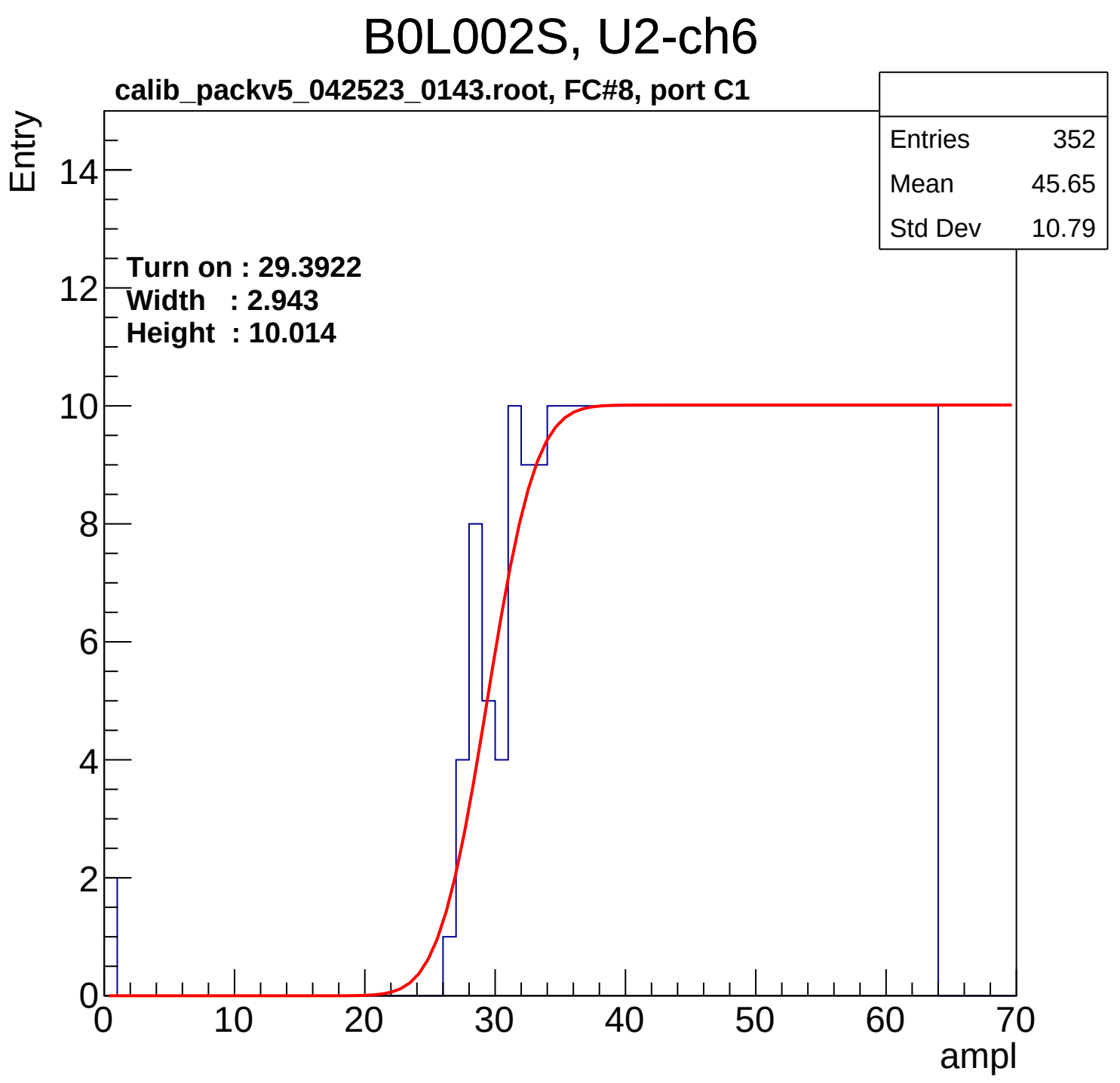
B0L002S, U2-ch6
calib_packv5_042523_0143.root, FC#8, port C1
Entries 352
Mean 45.65
Std Dev 10.79
Turn on : 29.3922
Width : 2.943
Height : 10.014
Entry
ampl
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2
4
6
8
10
12
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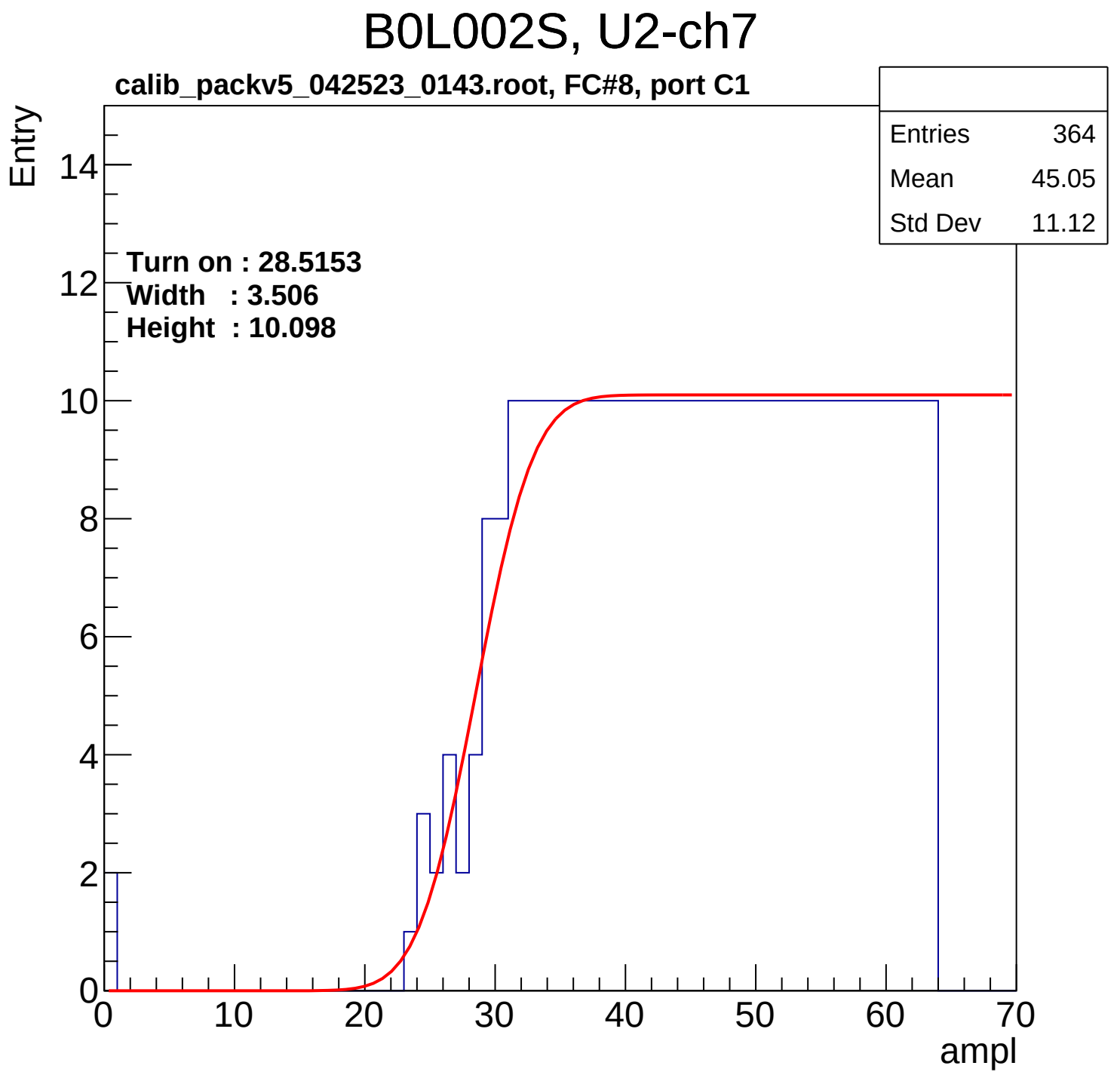
B0L002S, U2-ch7
calib_packv5_042523_0143.root, FC#8, port C1
Entries 364
Mean 45.05
Std Dev 11.12
Turn on : 28.5153
Width : 3.506
Height : 10.098
Entry
ampl
0
2
4
6
8
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12
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60
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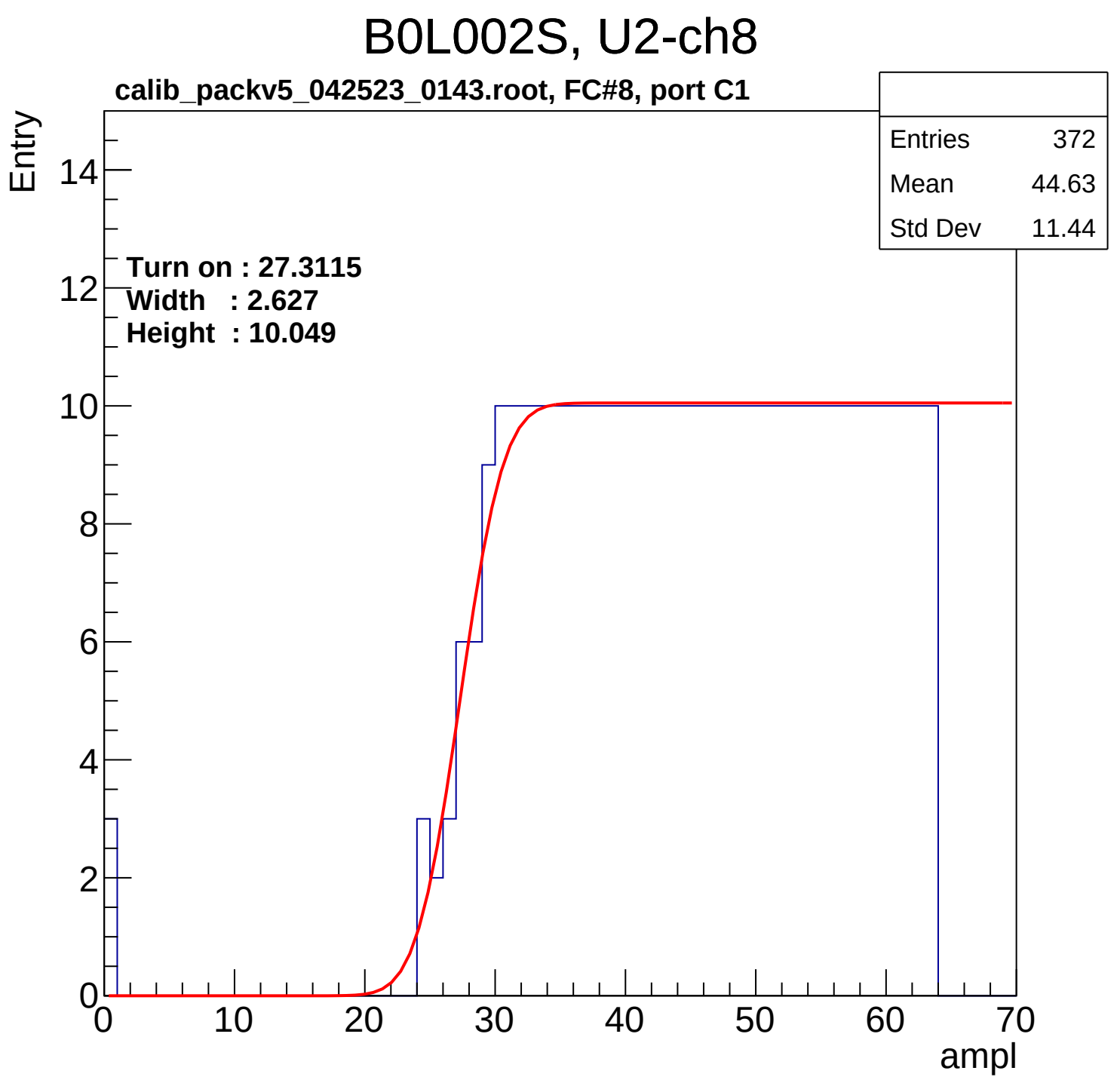
B0L002S, U2-ch8
calib_packv5_042523_0143.root, FC#8, port C1
Entries 372
Mean 44.63
Std Dev 11.44
Turn on : 27.3115
Width : 2.627
Height : 10.049
Entry
ampl
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4
6
8
10
12
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0
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60
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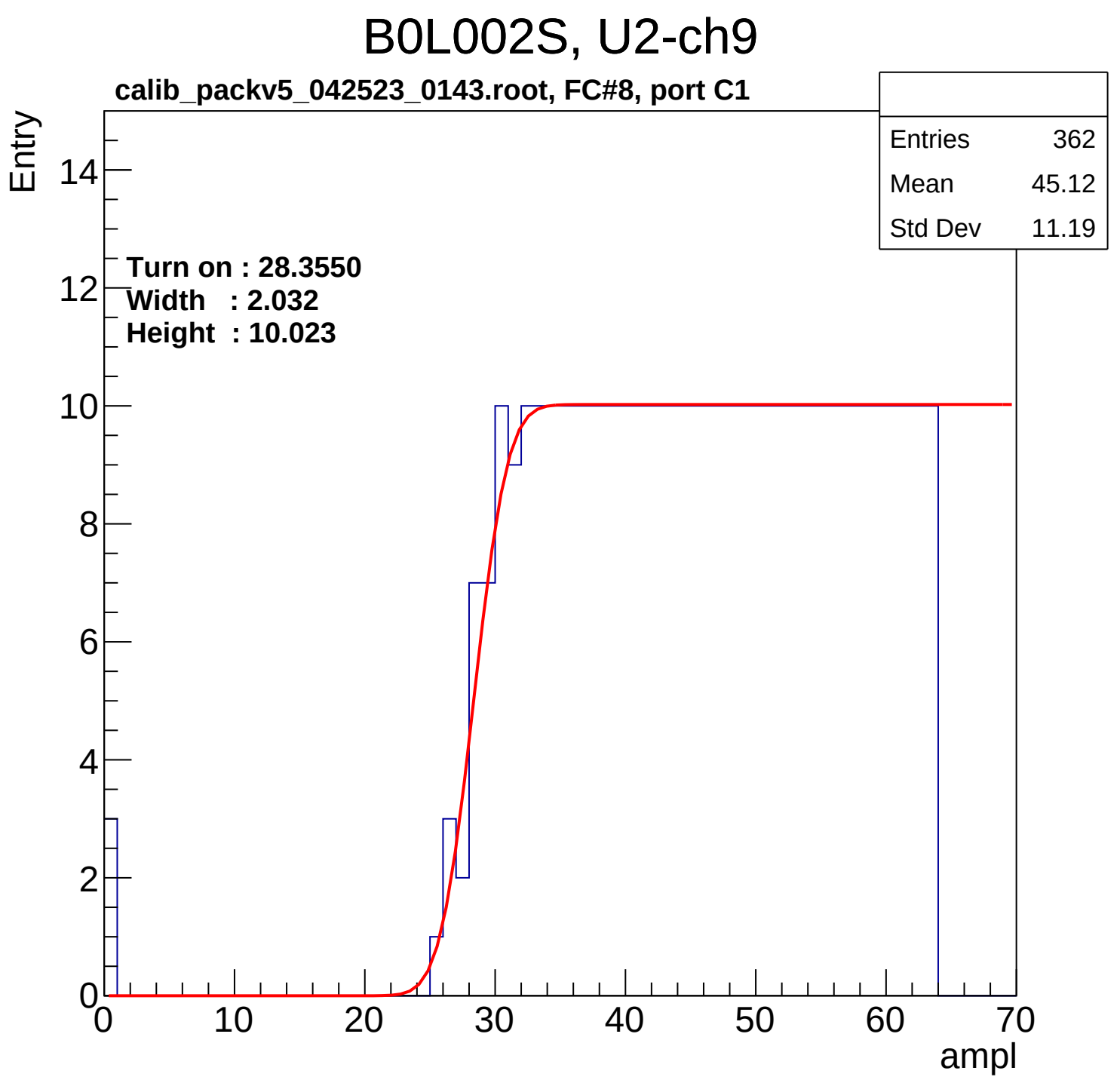
B0L002S, U2-ch9
calib_packv5_042523_0143.root, FC#8, port C1
Entries 362
Mean 45.12
Std Dev 11.19
Turn on : 28.3550
Width : 2.032
Height : 10.023
Entry
ampl
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2
4
6
8
10
12
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0
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20
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60
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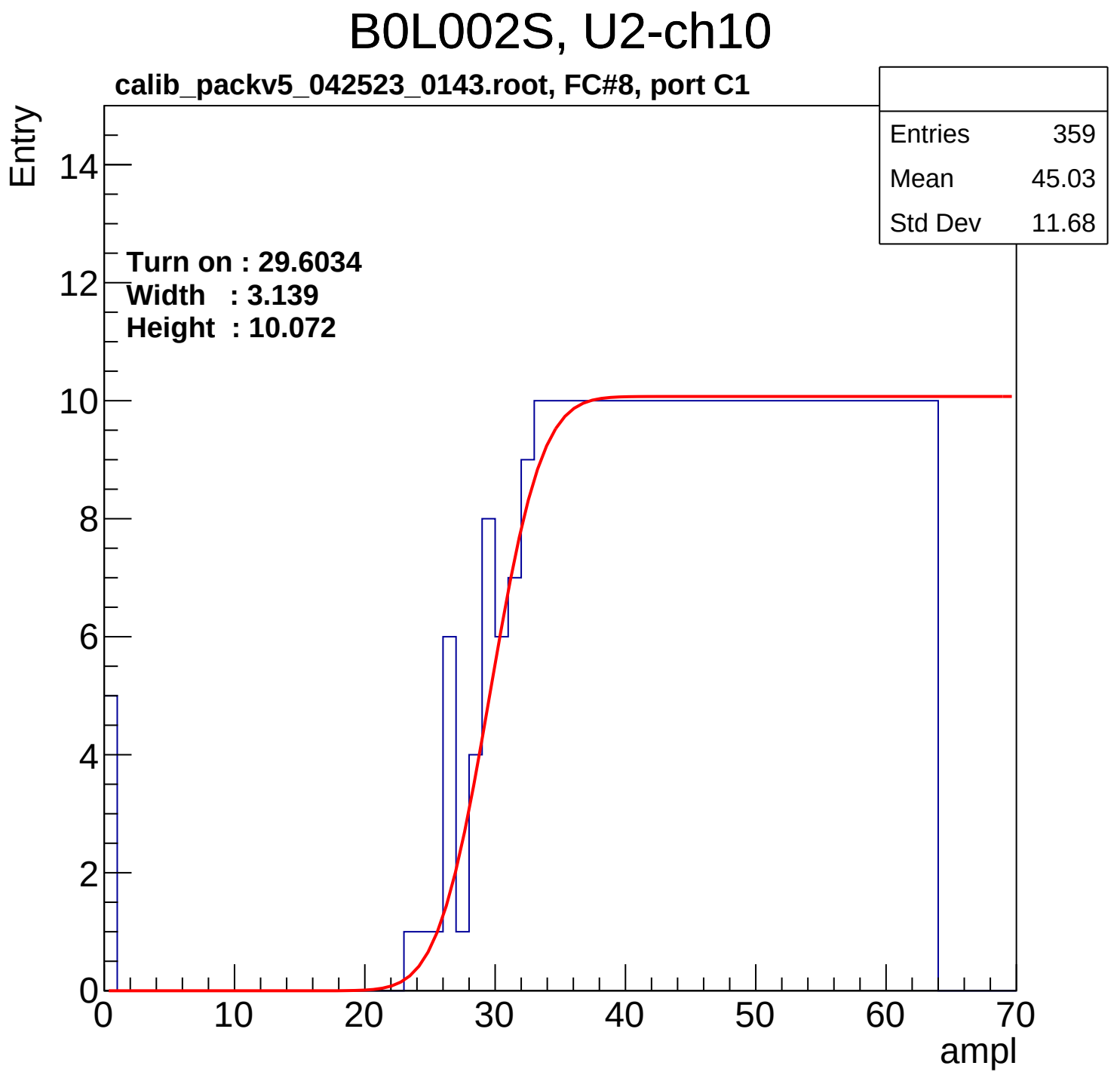
B0L002S, U2-ch10
calib_packv5_042523_0143.root, FC#8, port C1
Entries 359
Mean 45.03
Std Dev 11.68
Turn on : 29.6034
Width : 3.139
Height : 10.072
Entry
ampl
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2
4
6
8
10
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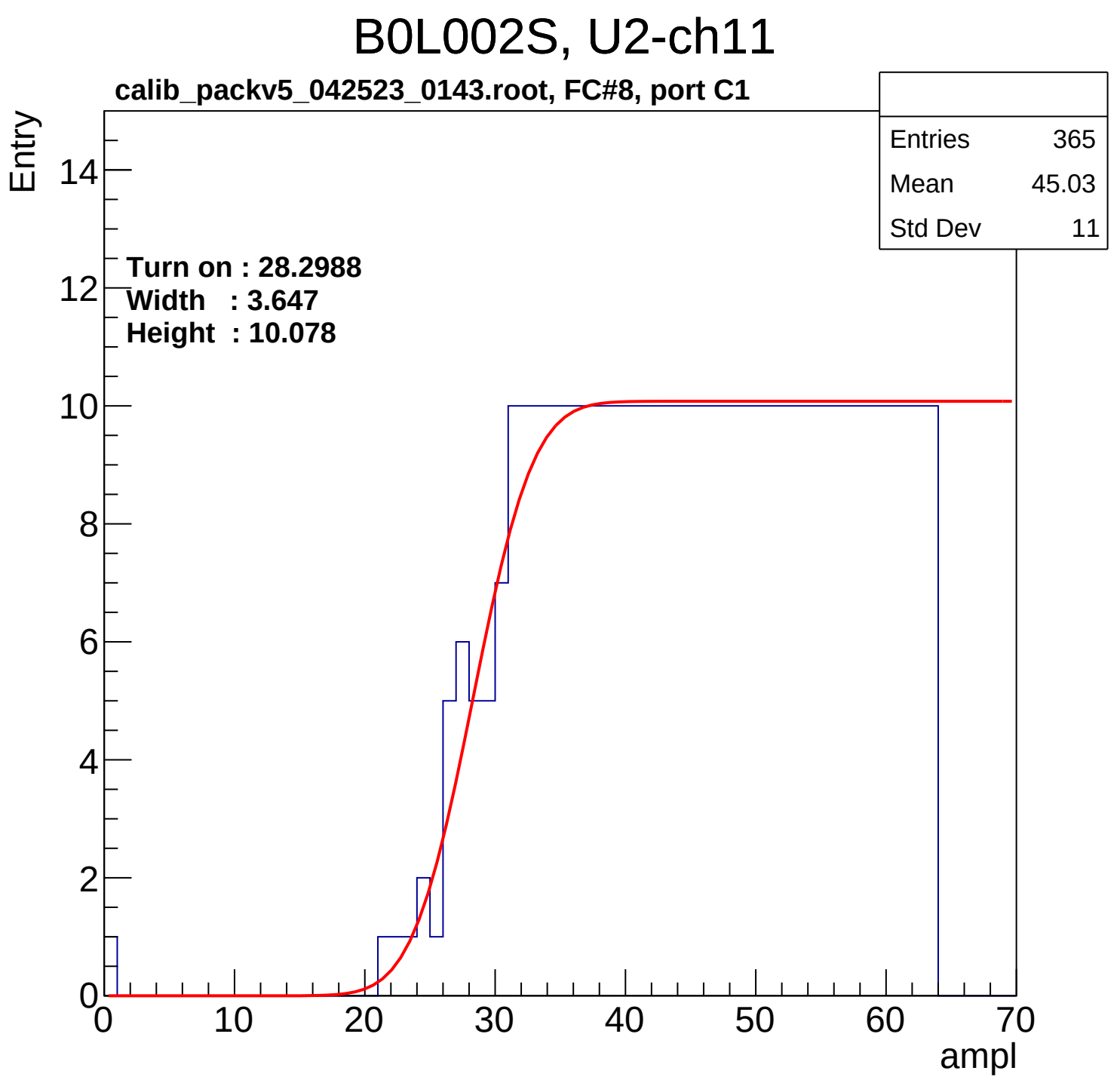
B0L002S, U2-ch11
calib_packv5_042523_0143.root, FC#8, port C1
Entries 365
Mean 45.03
Std Dev 11
Turn on : 28.2988
Width : 3.647
Height : 10.078
Entry
ampl
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6
8
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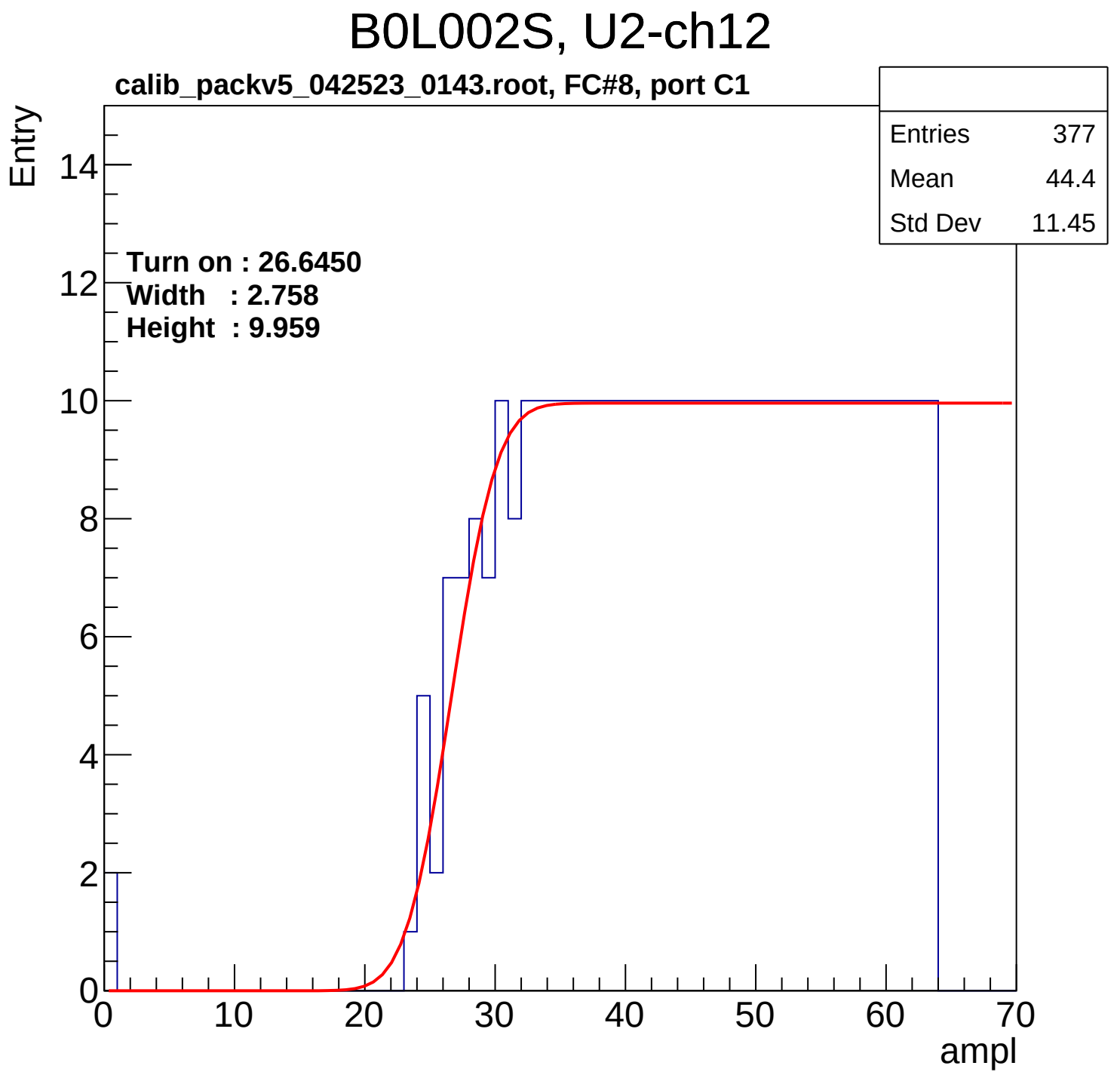
B0L002S, U2-ch12
calib_packv5_042523_0143.root, FC#8, port C1
Entries 377
Mean 44.4
Std Dev 11.45
Turn on : 26.6450
Width : 2.758
Height : 9.959
Entry
ampl
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4
6
8
10
12
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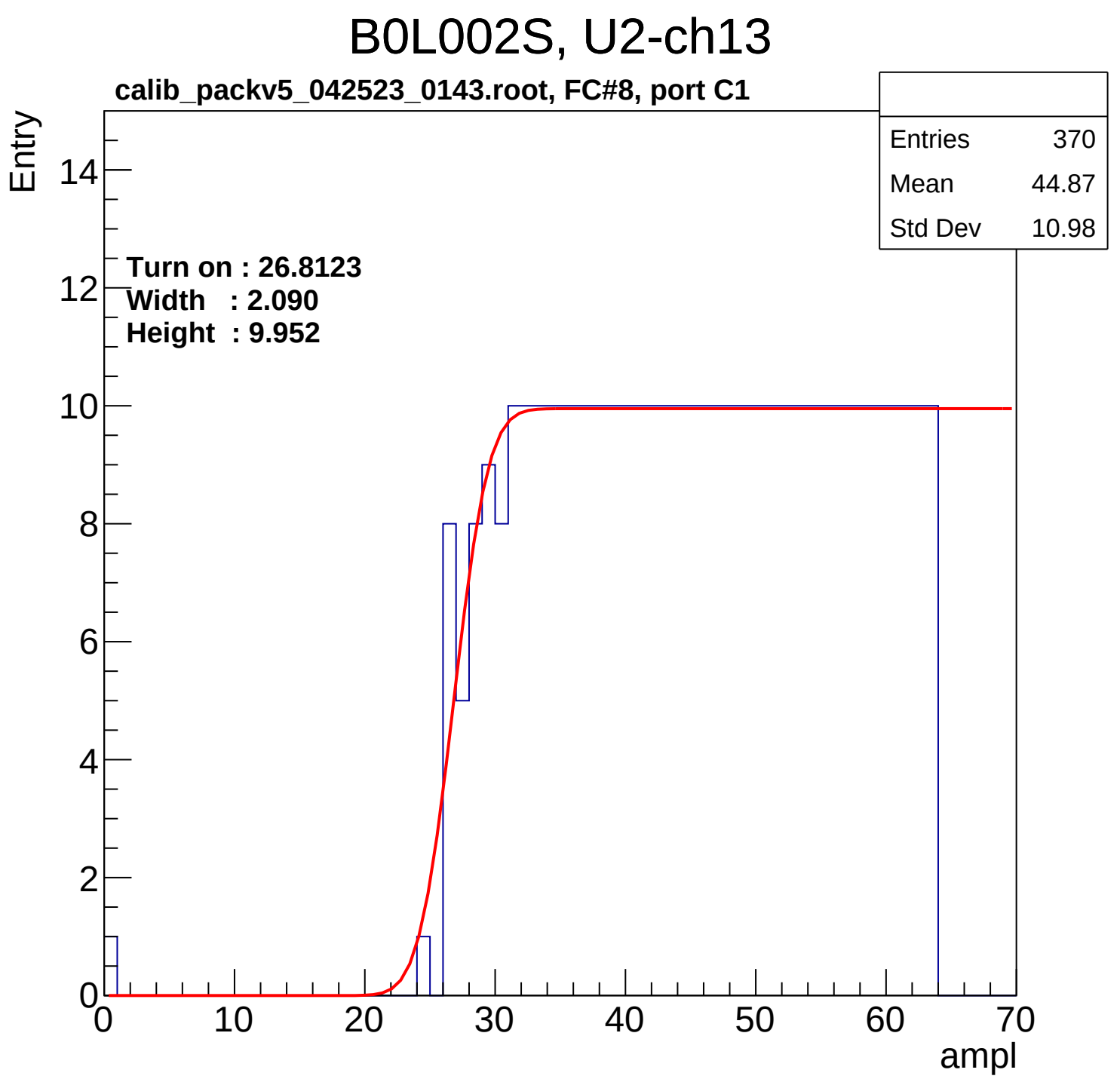
B0L002S, U2-ch13
calib_packv5_042523_0143.root, FC#8, port C1
Entries 370
Mean 44.87
Std Dev 10.98
Turn on : 26.8123
Width : 2.090
Height : 9.952
Entry
ampl
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4
6
8
10
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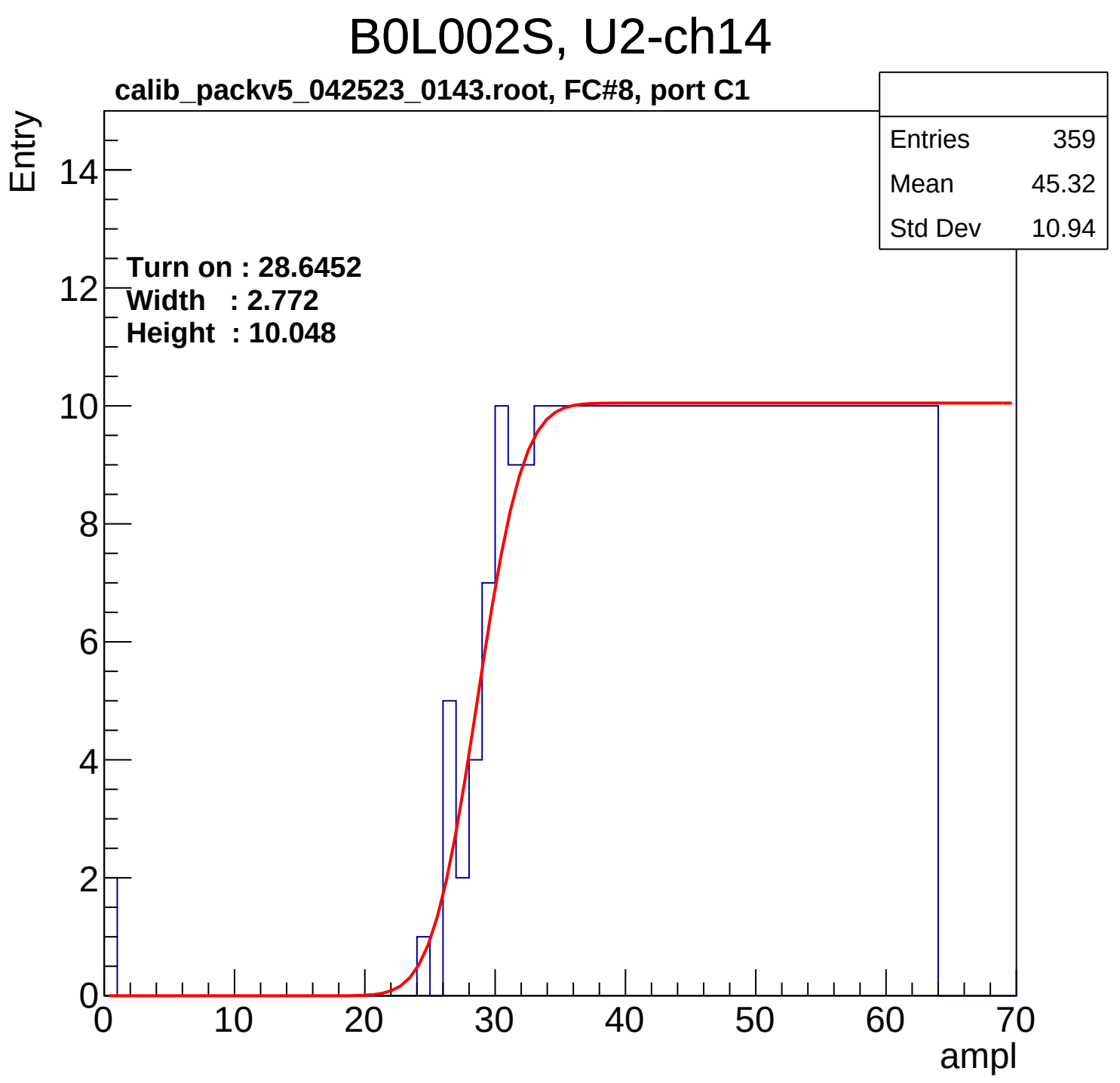
B0L002S, U2-ch14
calib_packv5_042523_0143.root, FC#8, port C1
Entries 359
Mean 45.32
Std Dev 10.94
Turn on : 28.6452
Width : 2.772
Height : 10.048
Entry
ampl
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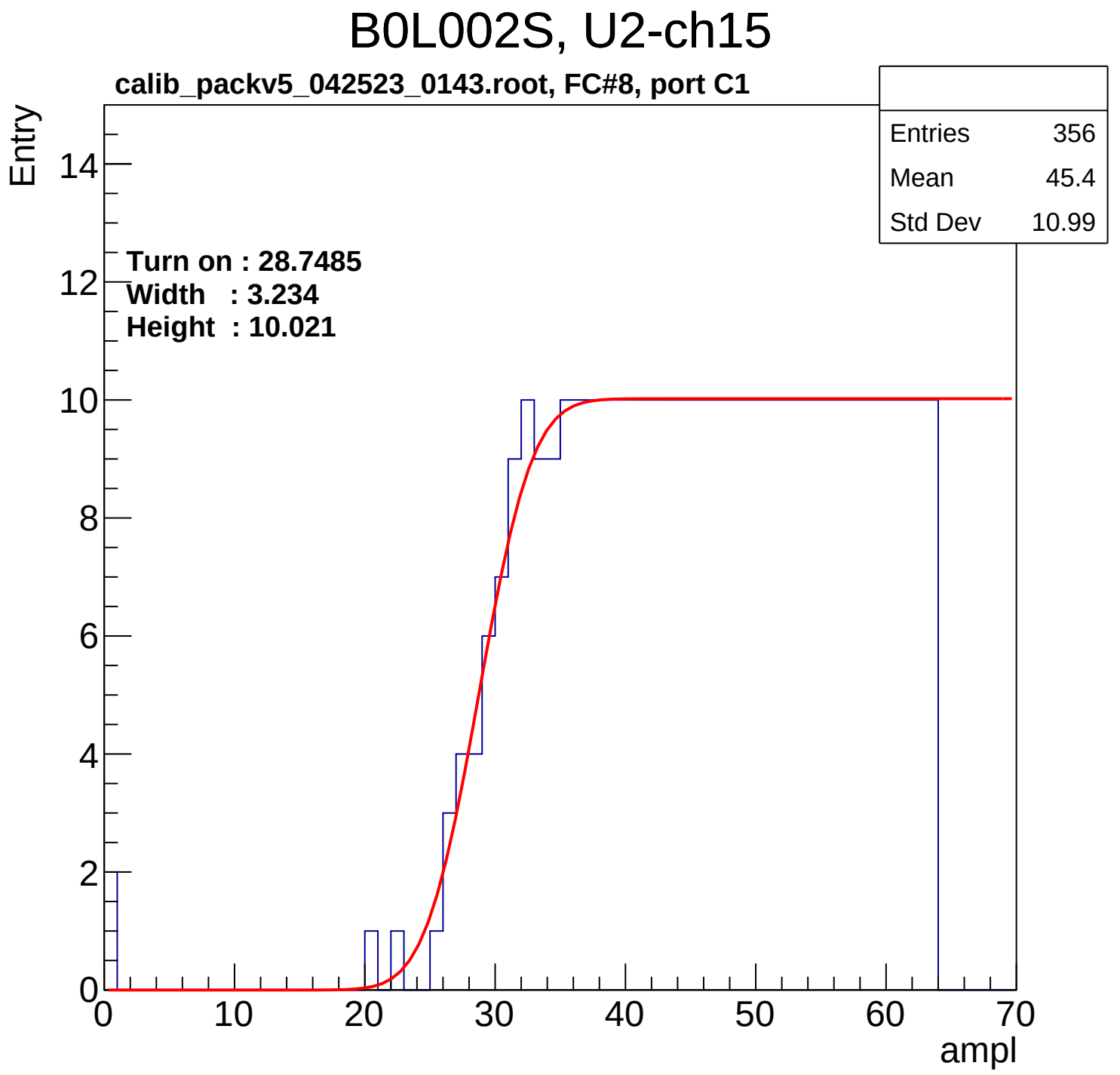
B0L002S, U2-ch15
calib_packv5_042523_0143.root, FC#8, port C1
Entries 356
Mean 45.4
Std Dev 10.99
Turn on : 28.7485
Width : 3.234
Height : 10.021
Entry
ampl
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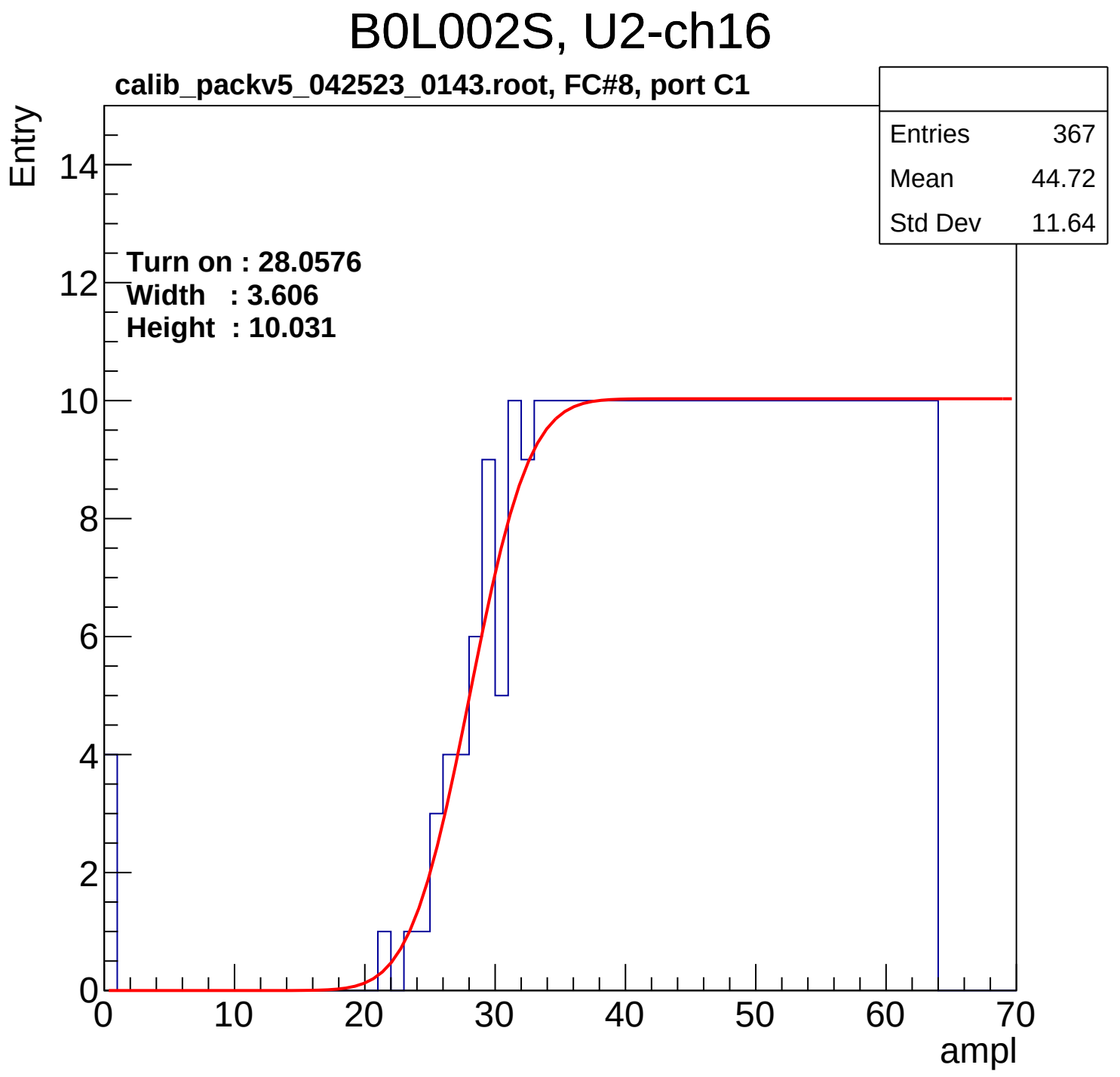
B0L002S, U2-ch16
calib_packv5_042523_0143.root, FC#8, port C1
Entries 367
Mean 44.72
Std Dev 11.64
Turn on : 28.0576
Width : 3.606
Height : 10.031
Entry
ampl
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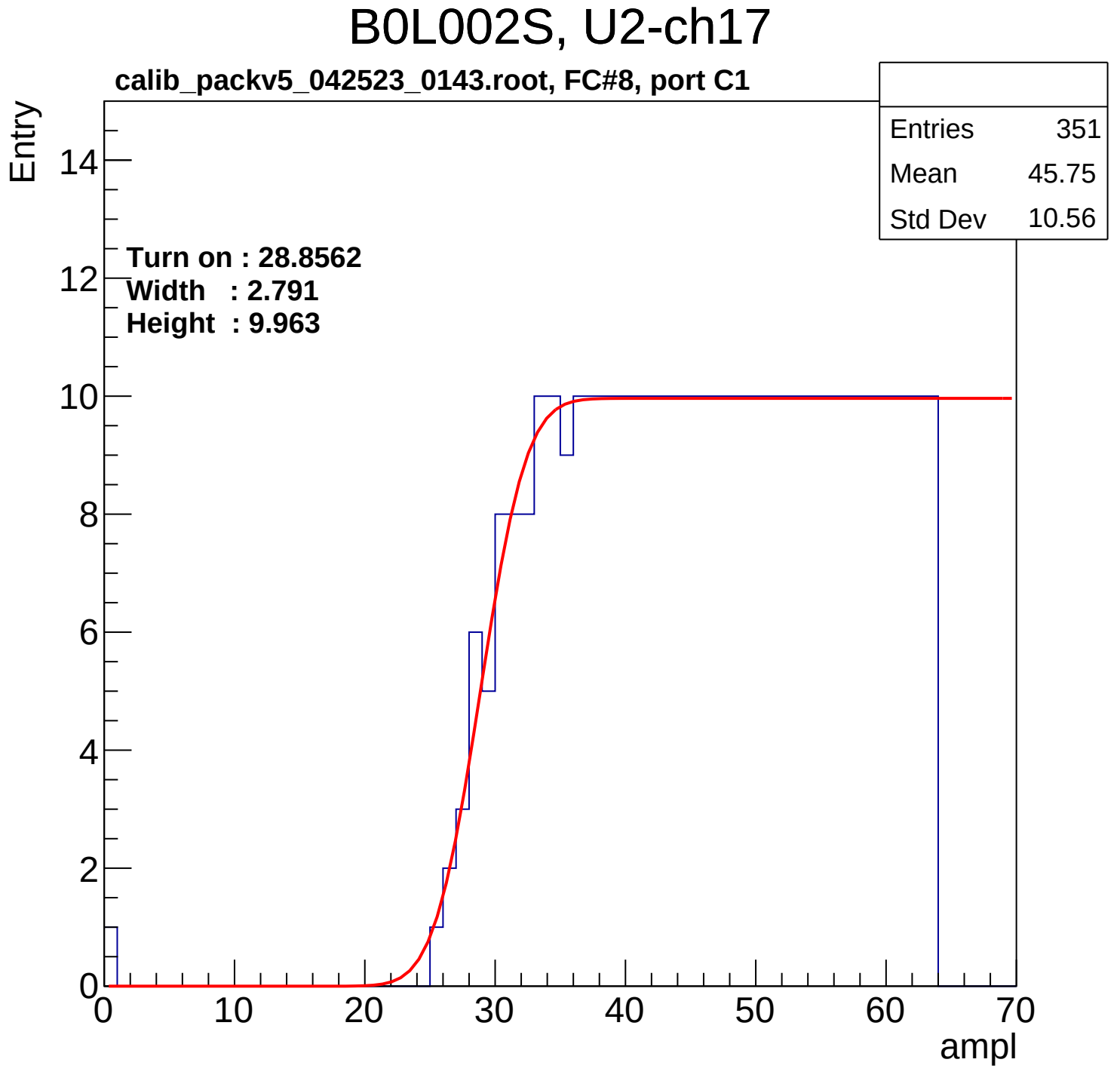
B0L002S, U2-ch17
calib_packv5_042523_0143.root, FC#8, port C1
Entries 351
Mean 45.75
Std Dev 10.56
Turn on : 28.8562
Width : 2.791
Height : 9.963
Entry
ampl
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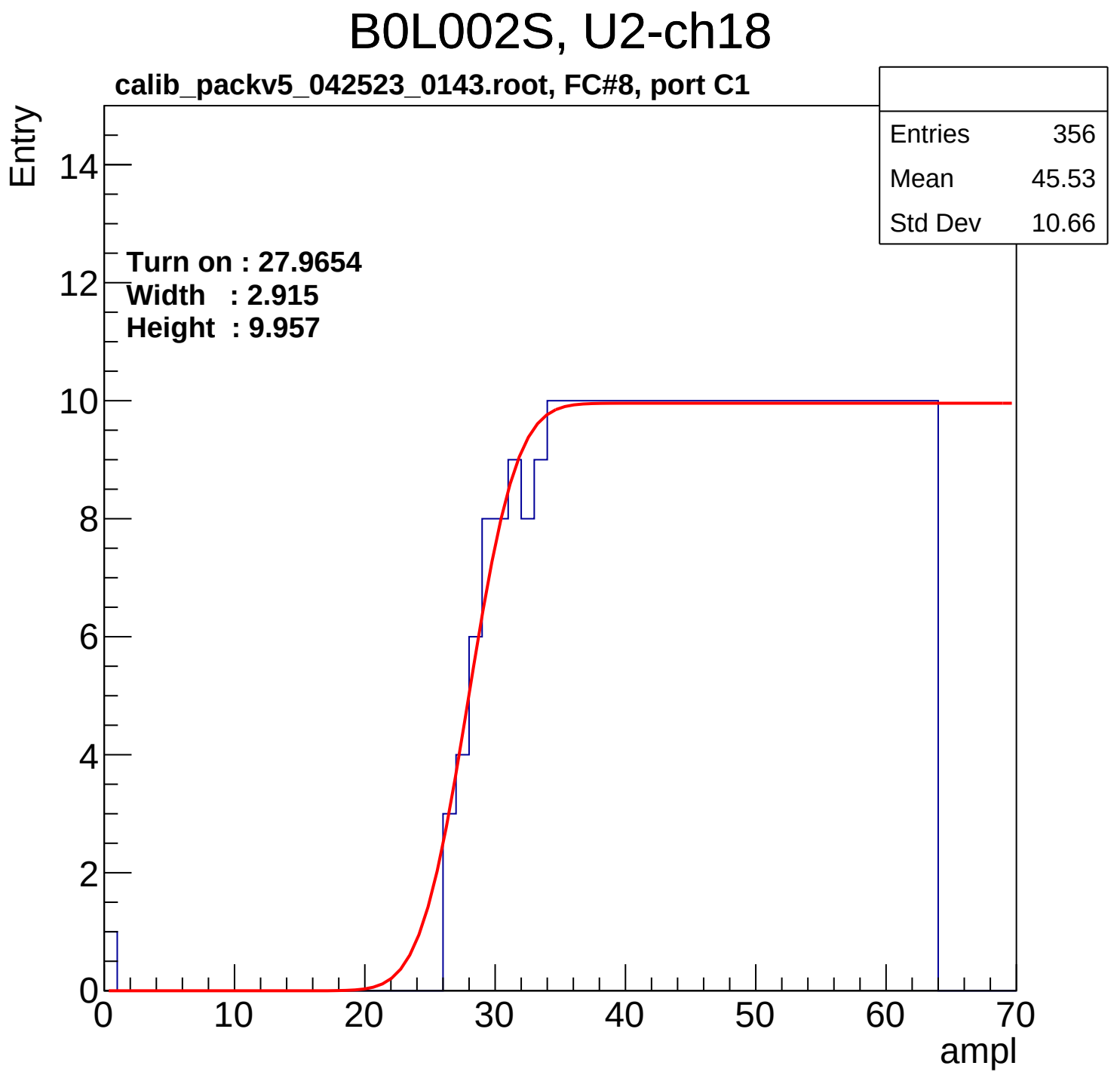
B0L002S, U2-ch18
calib_packv5_042523_0143.root, FC#8, port C1
Entries 356
Mean 45.53
Std Dev 10.66
Turn on : 27.9654
Width : 2.915
Height : 9.957
Entry
ampl
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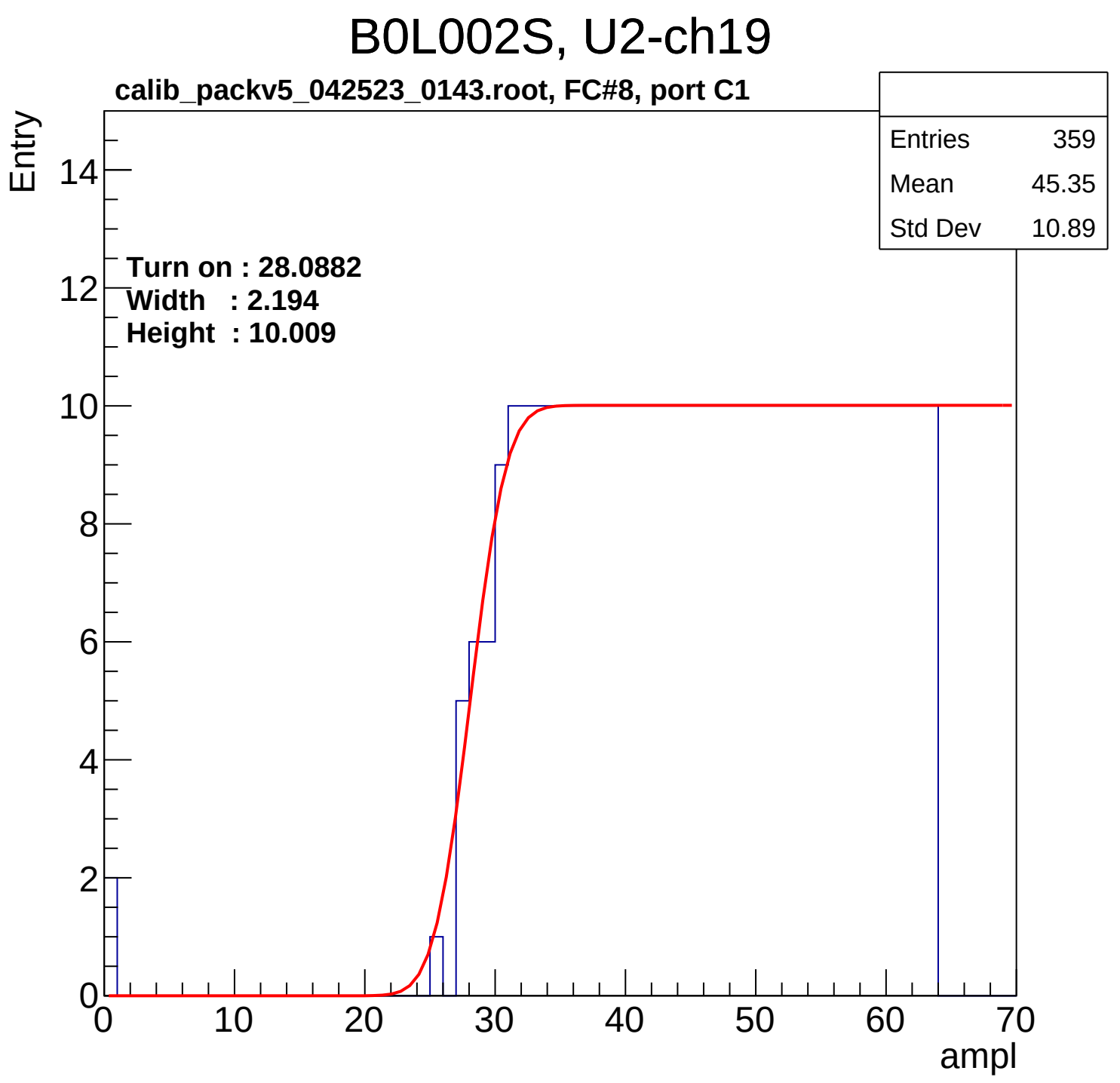
B0L002S, U2-ch19
calib_packv5_042523_0143.root, FC#8, port C1
Entries 359
Mean 45.35
Std Dev 10.89
Turn on : 28.0882
Width : 2.194
Height : 10.009
Entry
ampl
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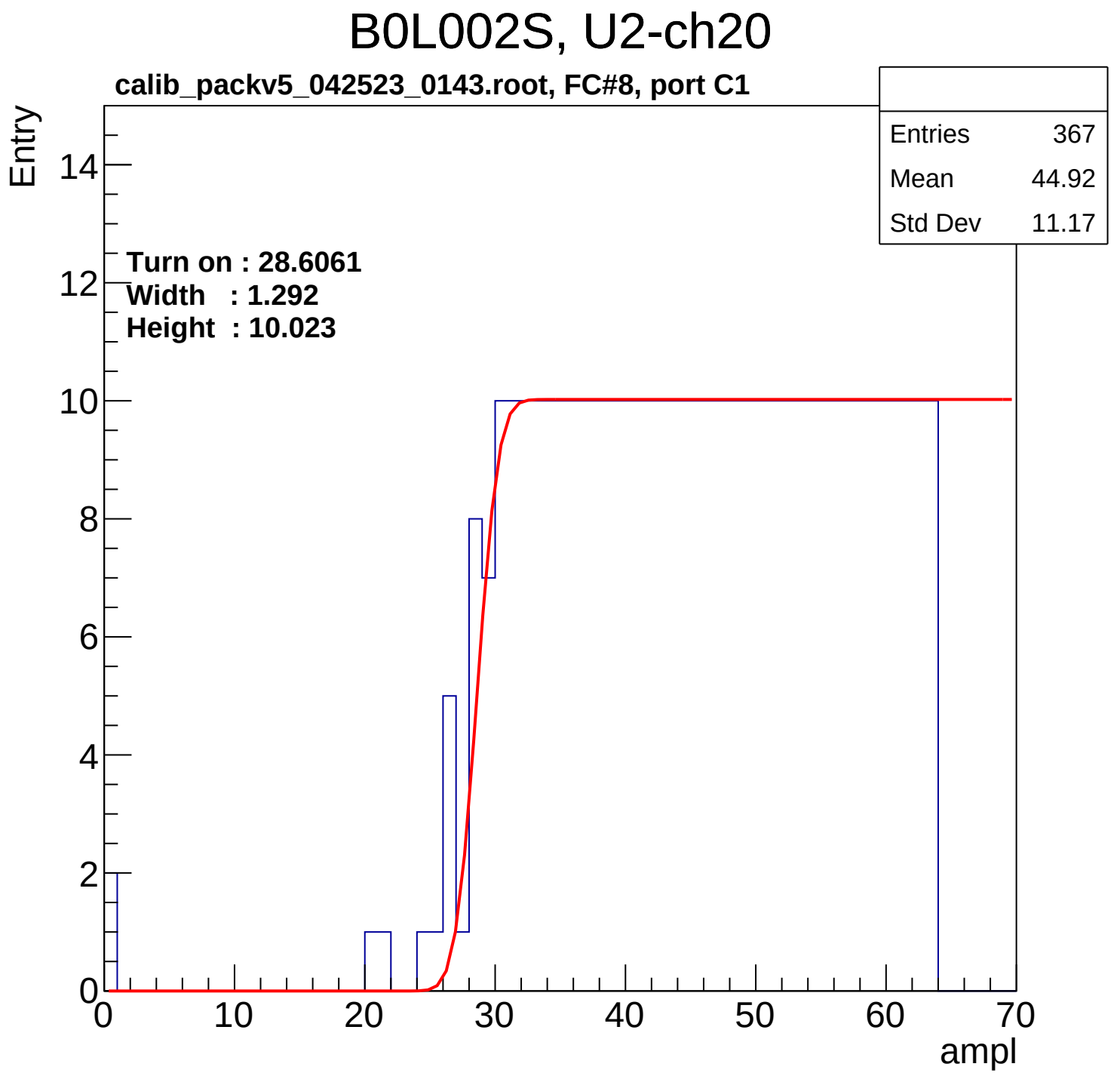
B0L002S, U2-ch20
calib_packv5_042523_0143.root, FC#8, port C1
Entries 367
Mean 44.92
Std Dev 11.17
Turn on : 28.6061
Width : 1.292
Height : 10.023
Entry
ampl
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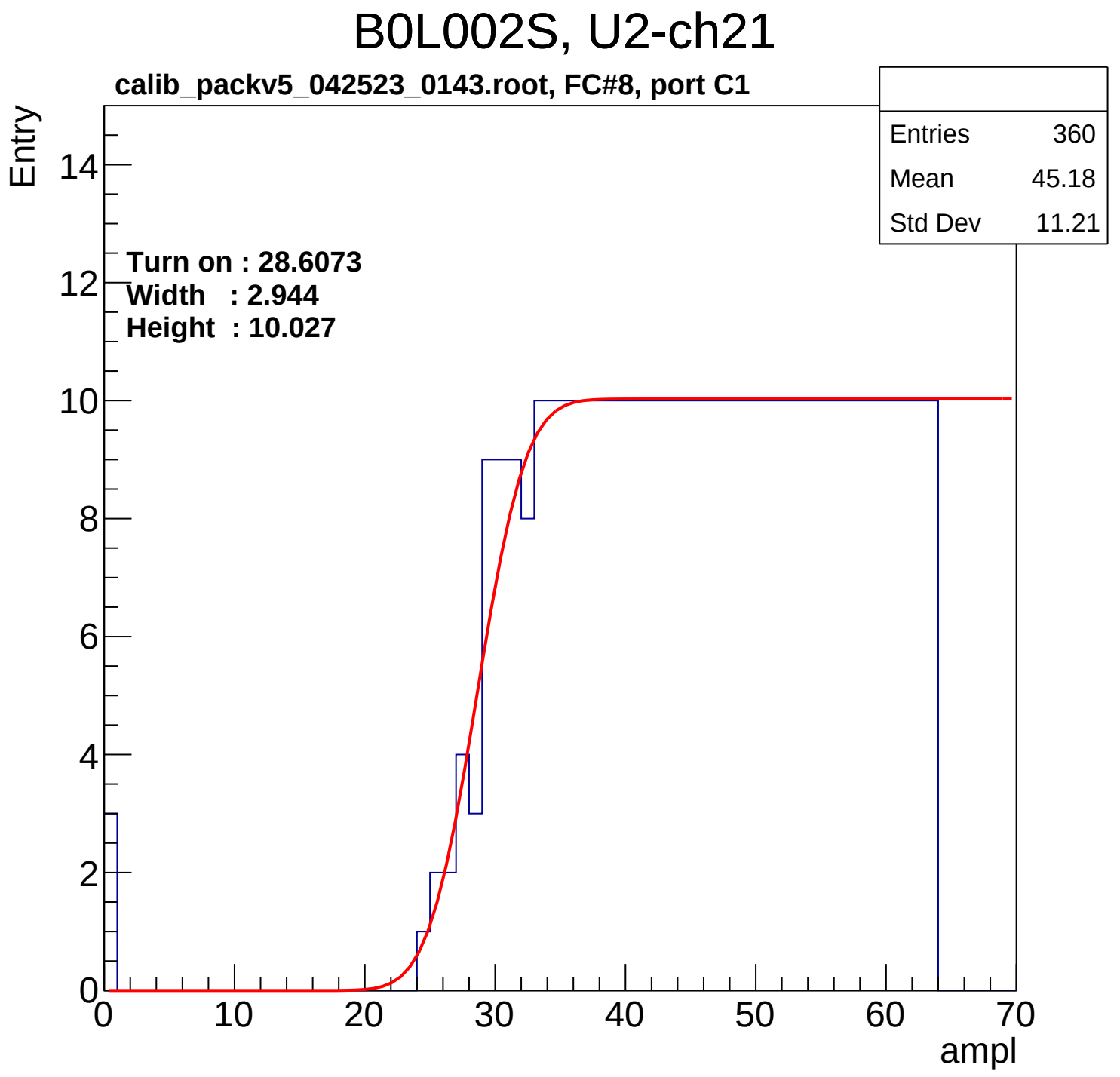
B0L002S, U2-ch21
calib_packv5_042523_0143.root, FC#8, port C1
Entries 360
Mean 45.18
Std Dev 11.21
Turn on : 28.6073
Width : 2.944
Height : 10.027
Entry
ampl
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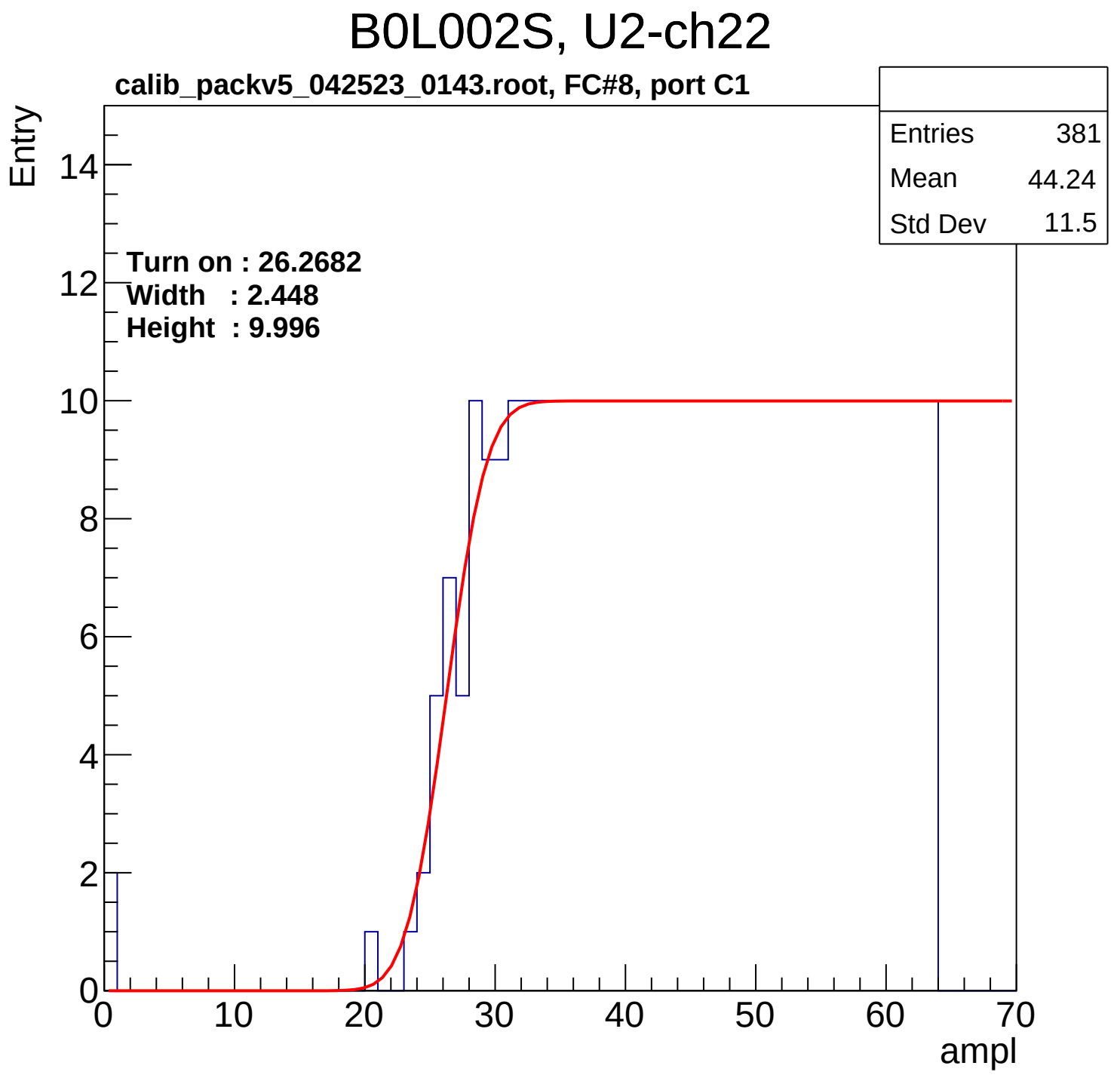
B0L002S, U2-ch22
calib_packv5_042523_0143.root, FC#8, port C1
Entries 381
Mean 44.24
Std Dev 11.5
Turn on : 26.2682
Width : 2.448
Height : 9.996
Entry
ampl
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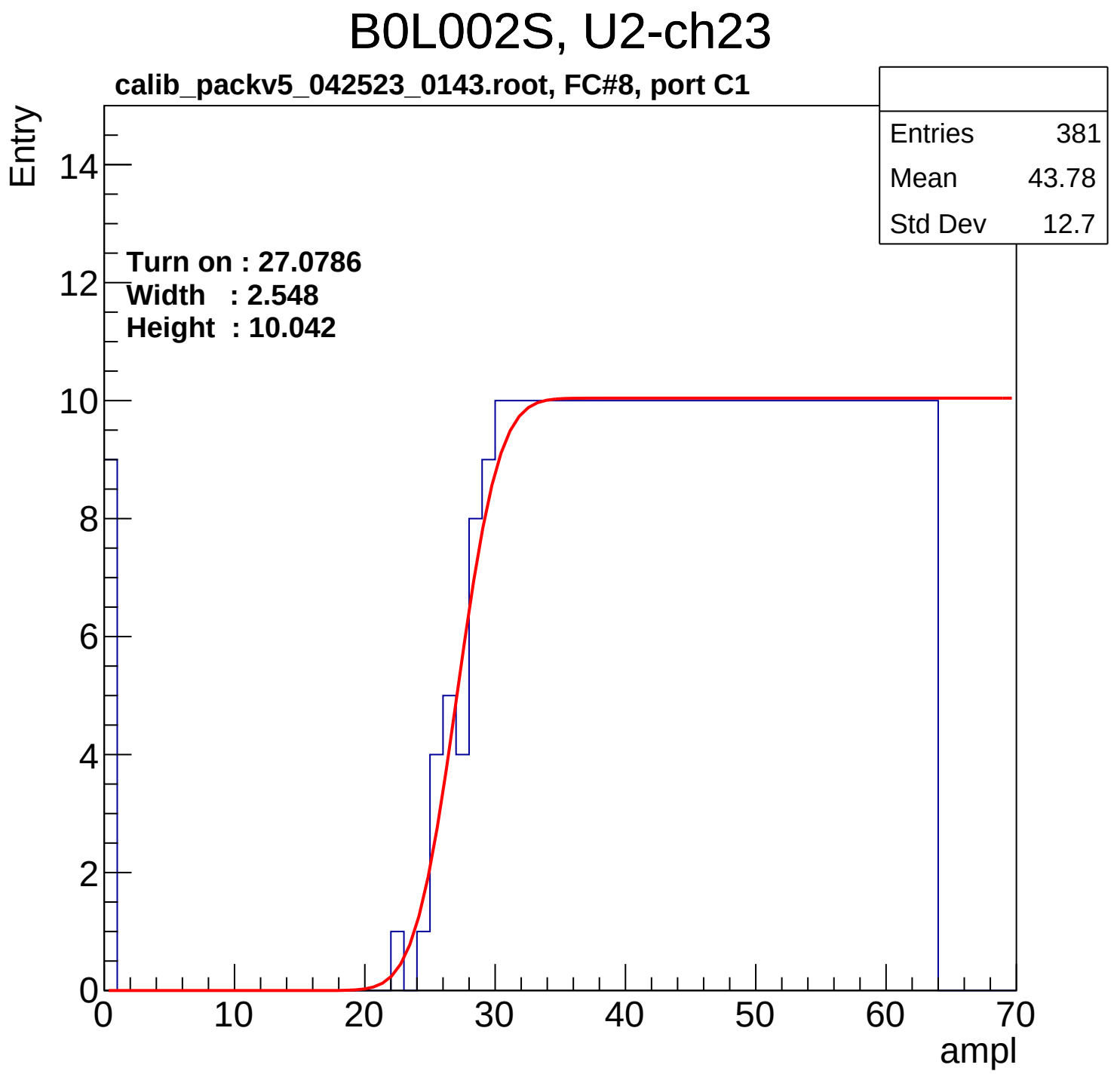
B0L002S, U2-ch23
calib_packv5_042523_0143.root, FC#8, port C1
Entries 381
Mean 43.78
Std Dev 12.7
Turn on : 27.0786
Width : 2.548
Height : 10.042
Entry
ampl
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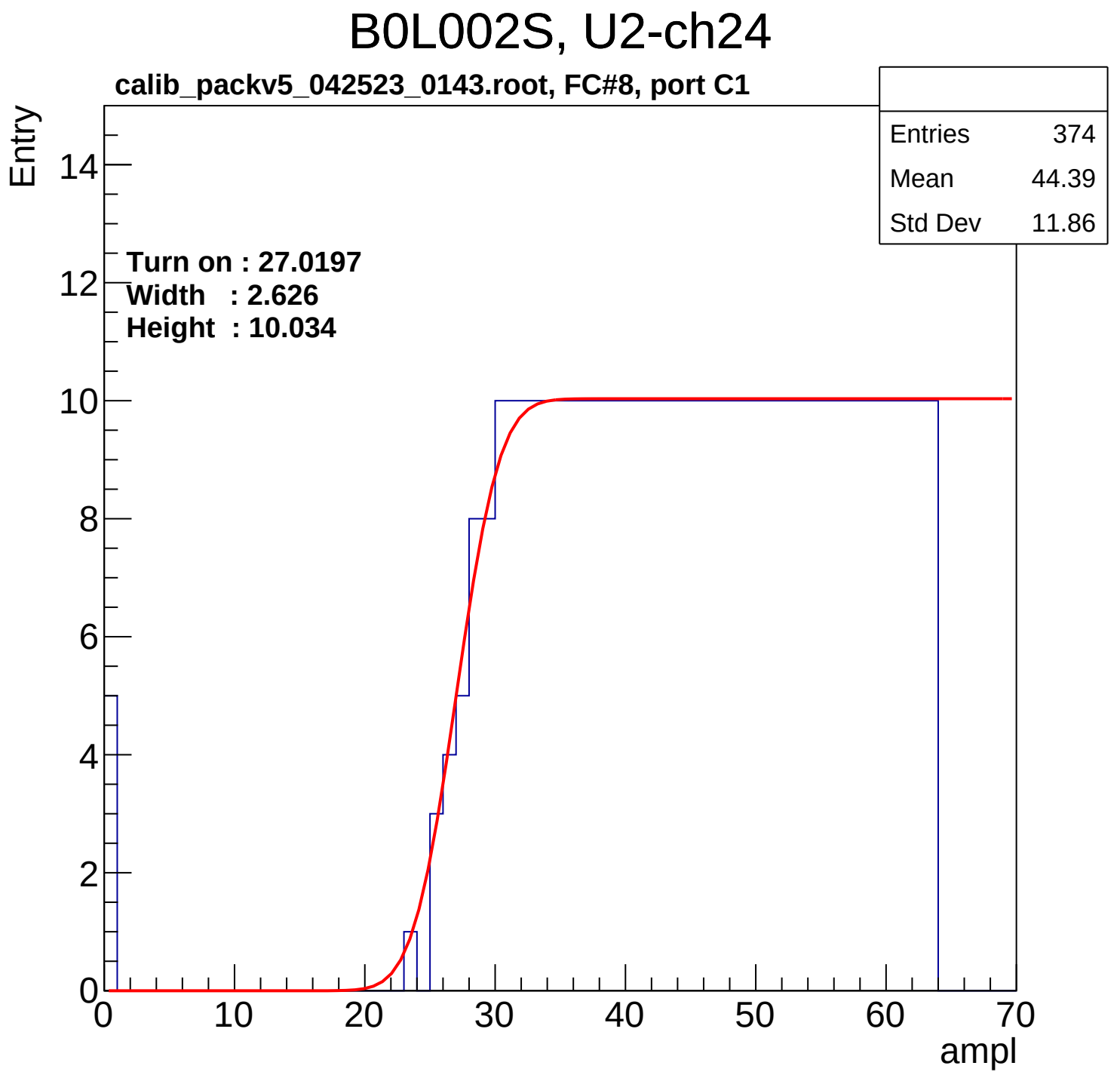
B0L002S, U2-ch24
calib_packv5_042523_0143.root, FC#8, port C1
Entries 374
Mean 44.39
Std Dev 11.86
Turn on : 27.0197
Width : 2.626
Height : 10.034
Entry
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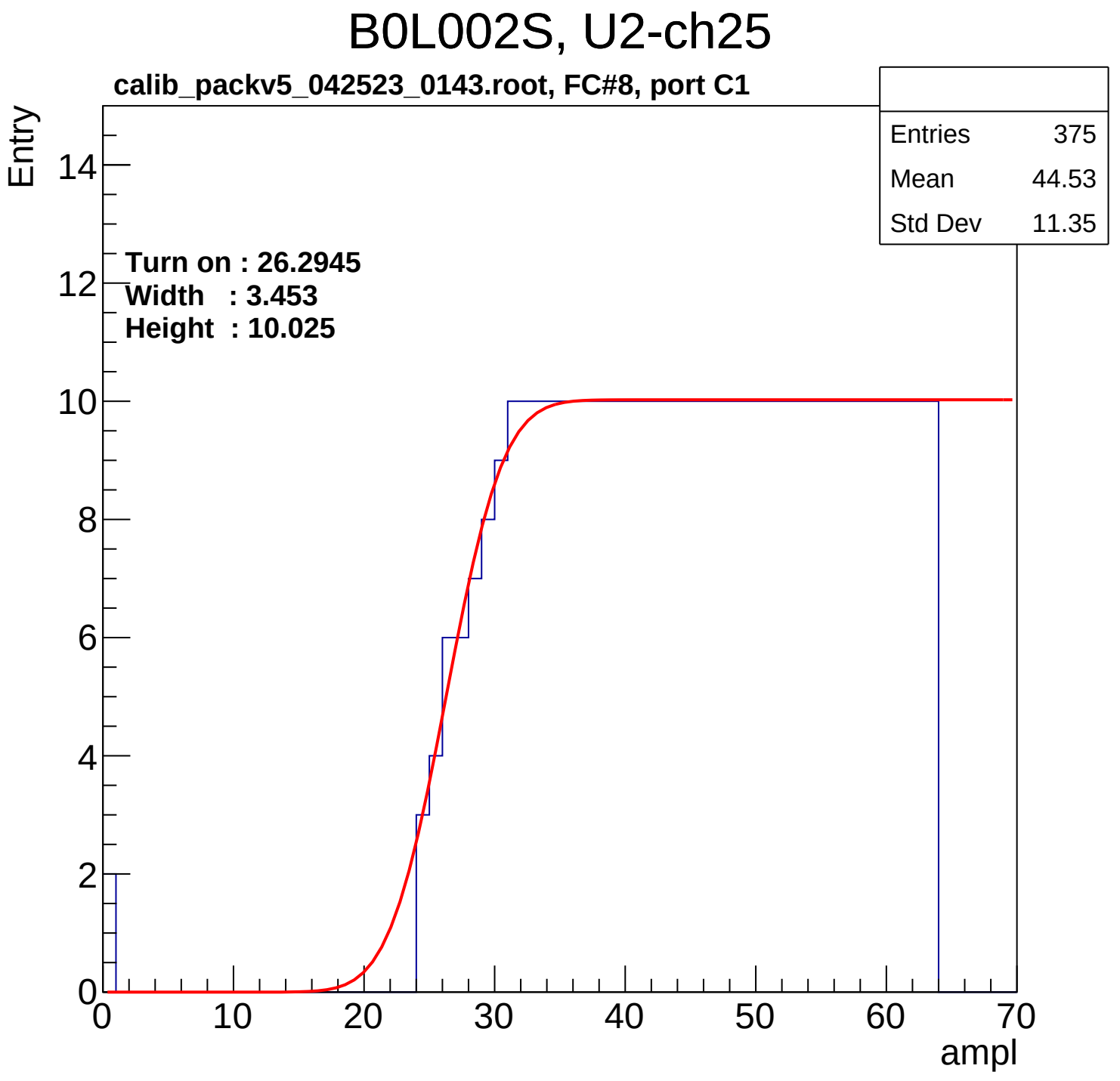
B0L002S, U2-ch25
calib_packv5_042523_0143.root, FC#8, port C1
Entries 375
Mean 44.53
Std Dev 11.35
Turn on : 26.2945
Width : 3.453
Height : 10.025
Entry
ampl
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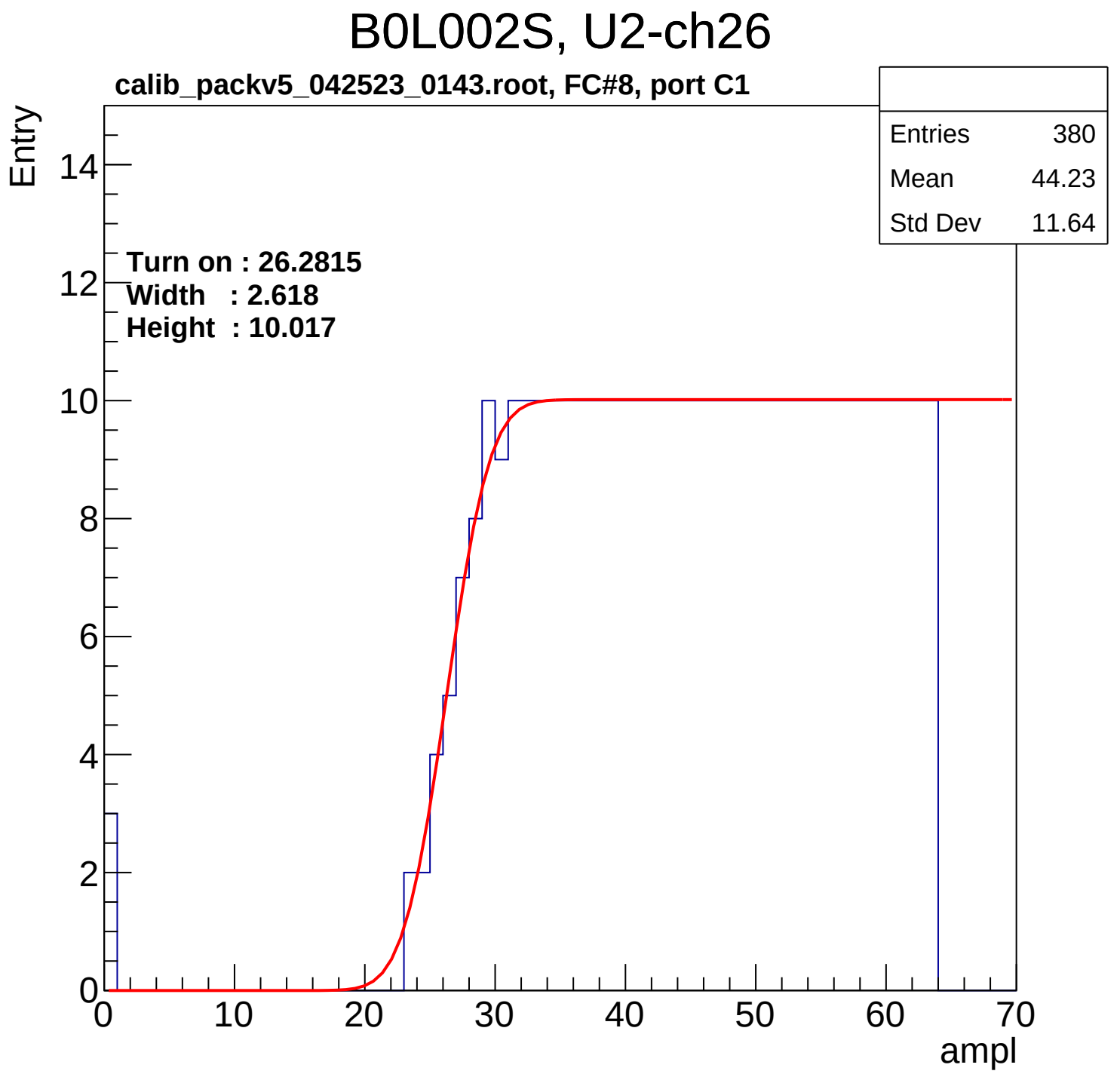
B0L002S, U2-ch26
calib_packv5_042523_0143.root, FC#8, port C1
Entries 380
Mean 44.23
Std Dev 11.64
Turn on : 26.2815
Width : 2.618
Height : 10.017
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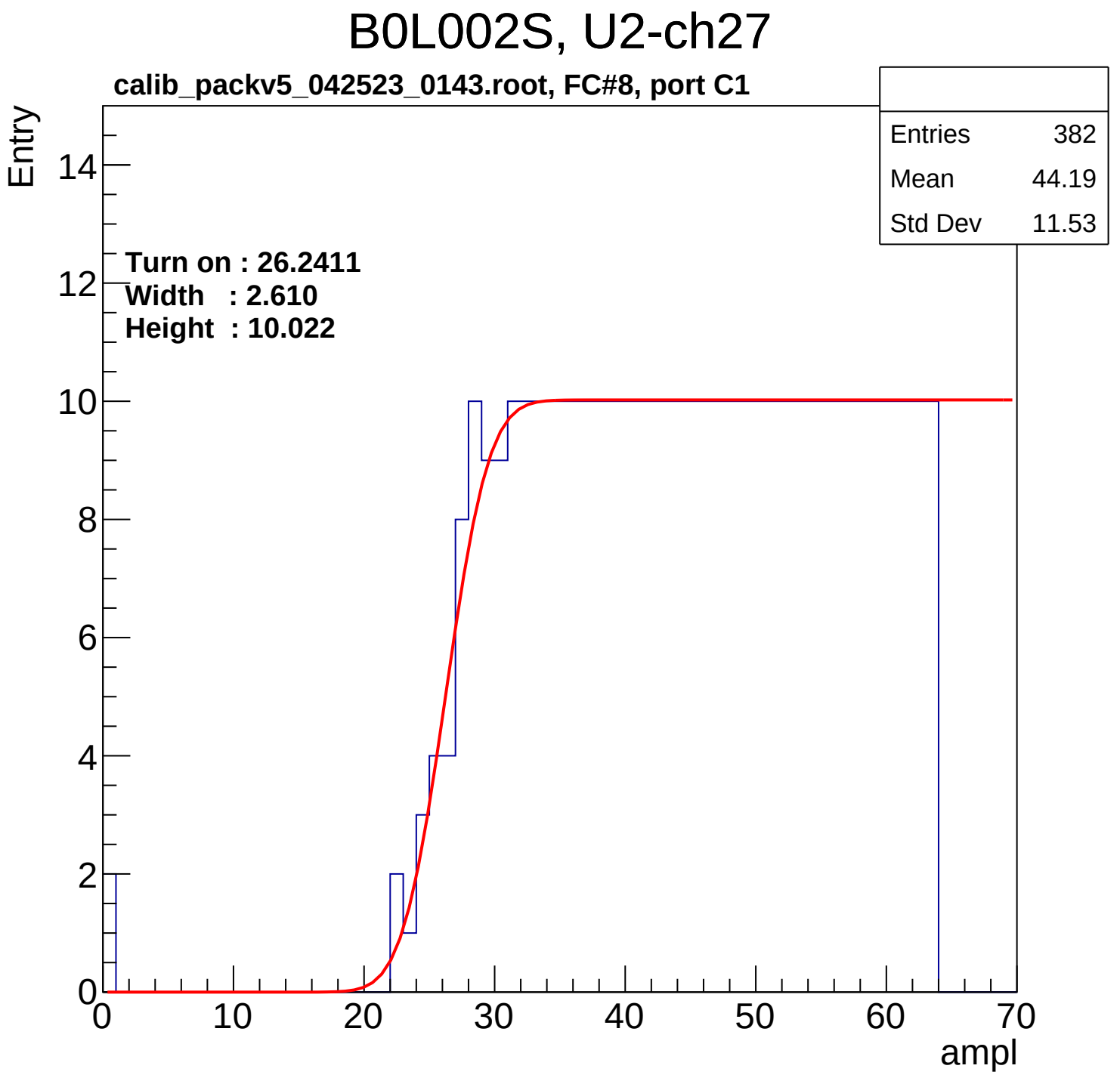
B0L002S, U2-ch27
calib_packv5_042523_0143.root, FC#8, port C1
Entries 382
Mean 44.19
Std Dev 11.53
Turn on : 26.2411
Width : 2.610
Height : 10.022
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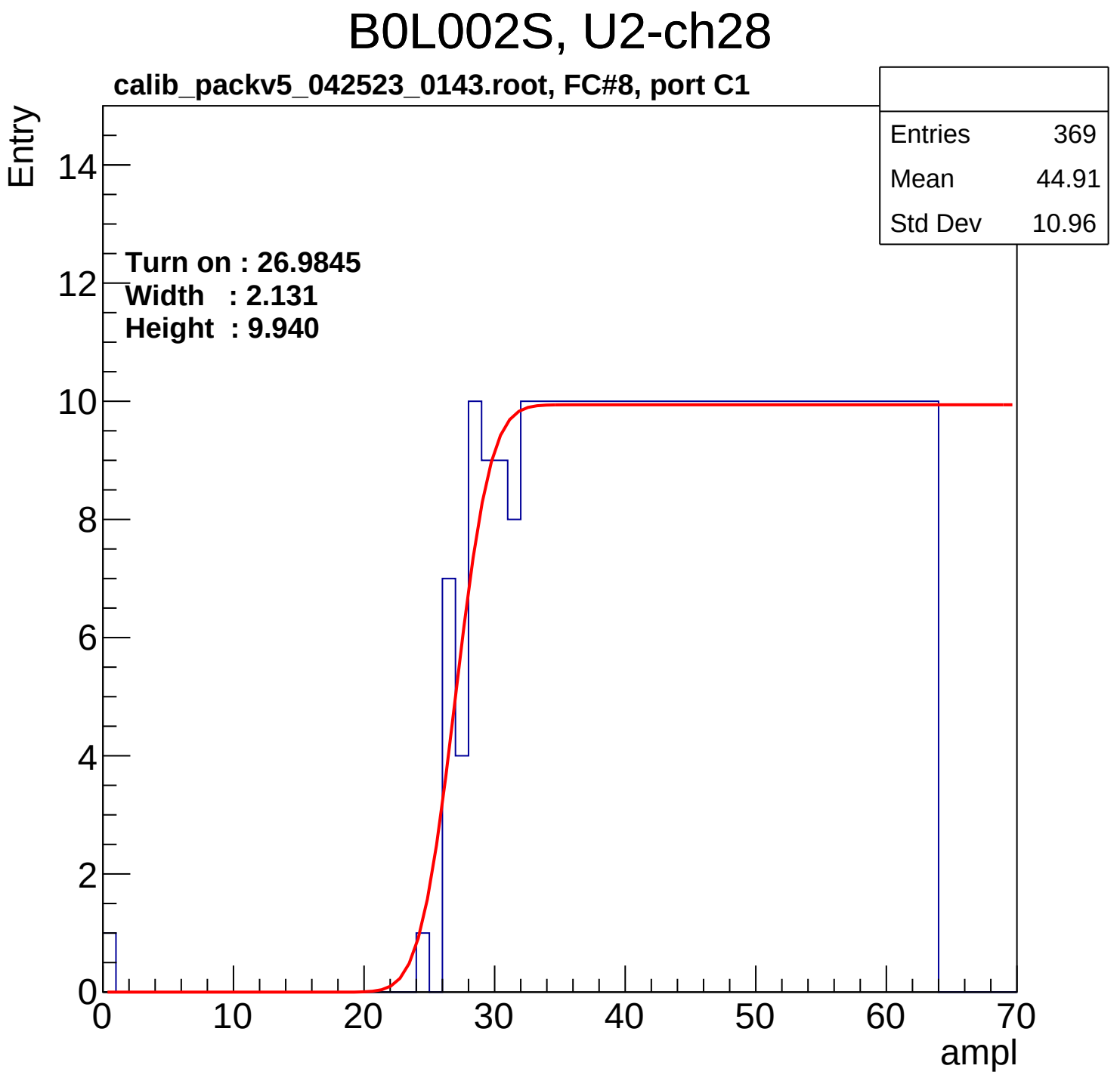
B0L002S, U2-ch28
calib_packv5_042523_0143.root, FC#8, port C1
Entries 369
Mean 44.91
Std Dev 10.96
Turn on : 26.9845
Width : 2.131
Height : 9.940
Entry
ampl
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4
6
8
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12
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20
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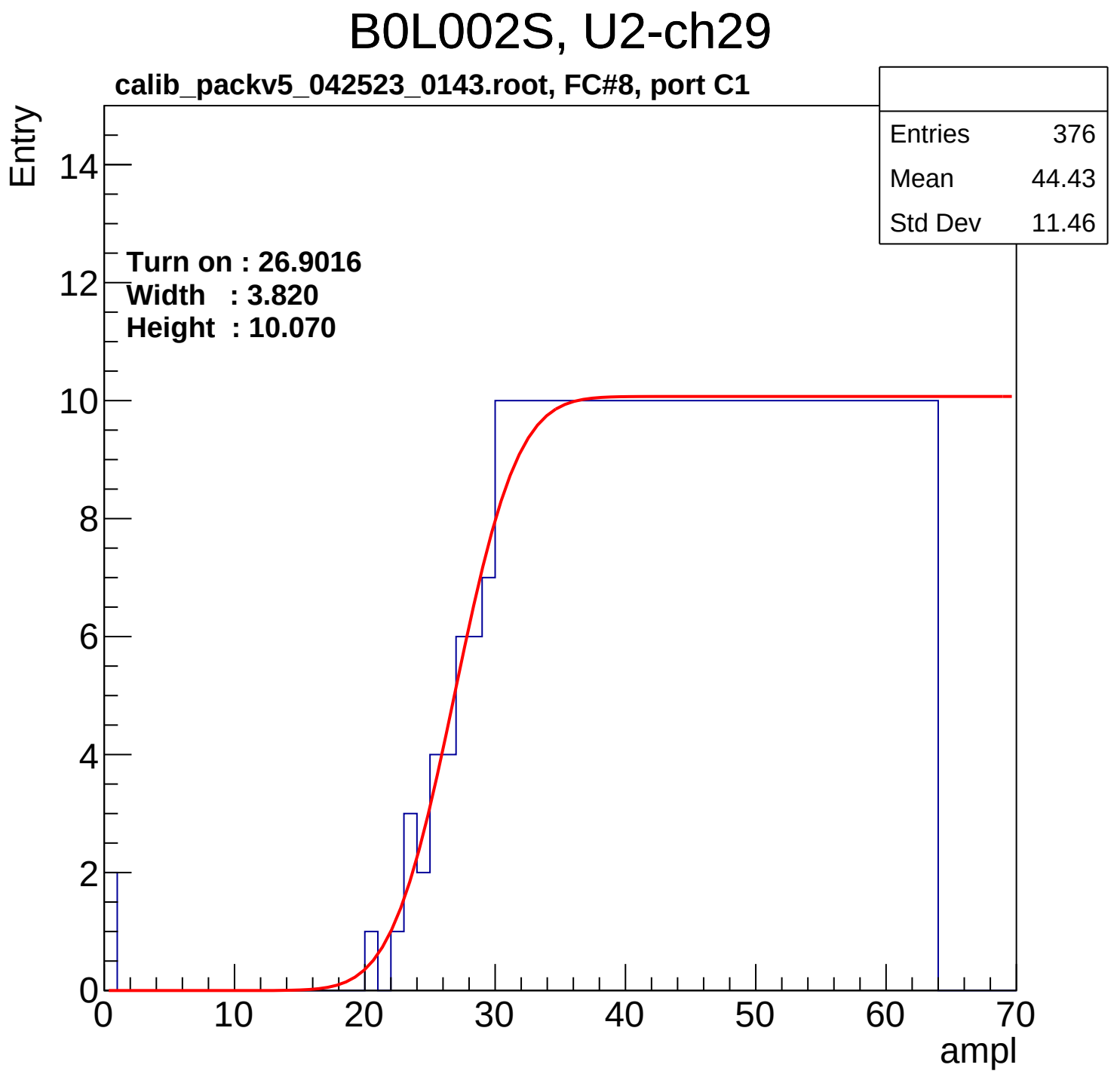
B0L002S, U2-ch29
calib_packv5_042523_0143.root, FC#8, port C1
Entries 376
Mean 44.43
Std Dev 11.46
Turn on : 26.9016
Width : 3.820
Height : 10.070
Entry
ampl
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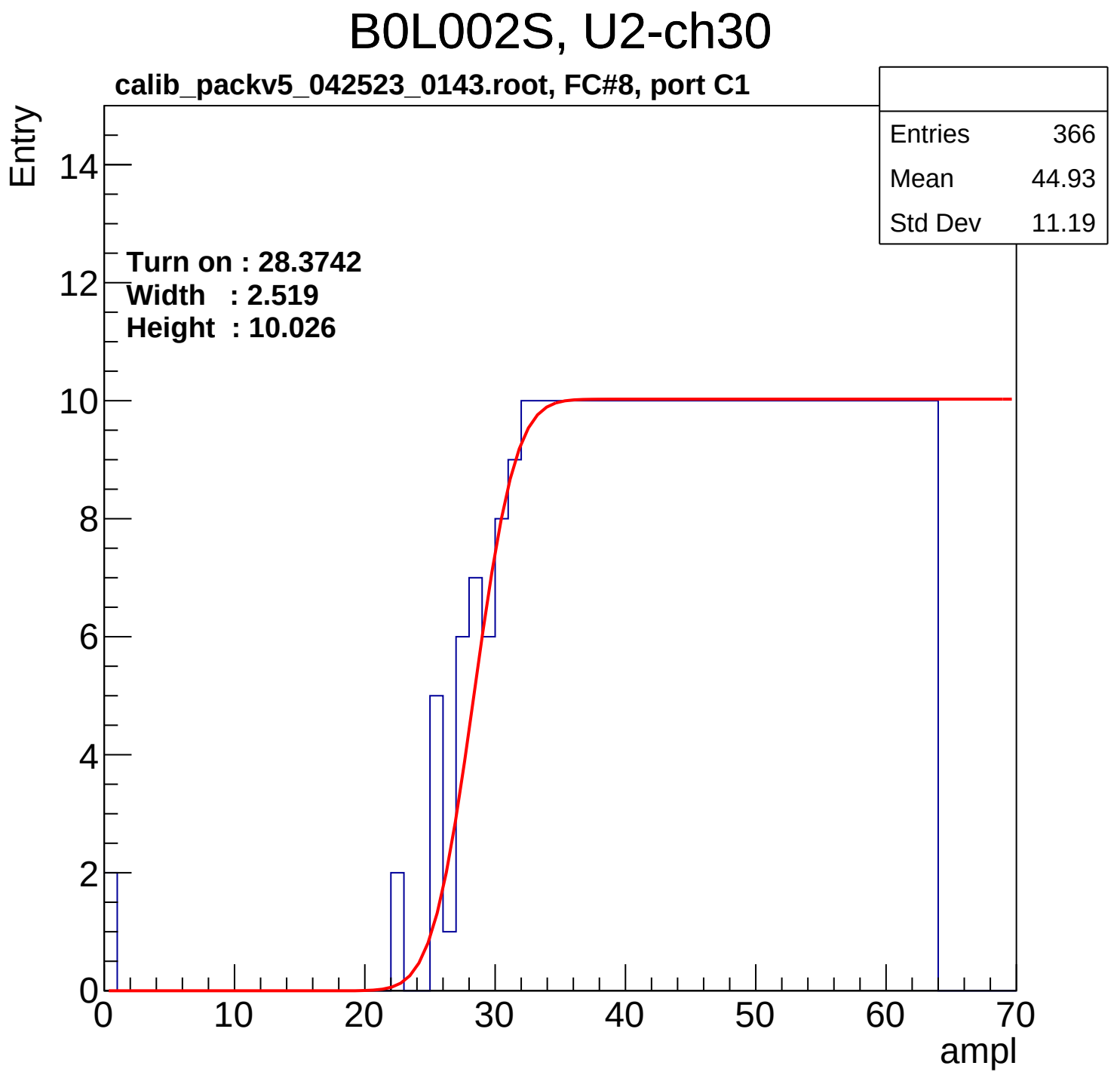
B0L002S, U2-ch30
calib_packv5_042523_0143.root, FC#8, port C1
Entries 366
Mean 44.93
Std Dev 11.19
Turn on : 28.3742
Width : 2.519
Height : 10.026
Entry
ampl
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2
4
6
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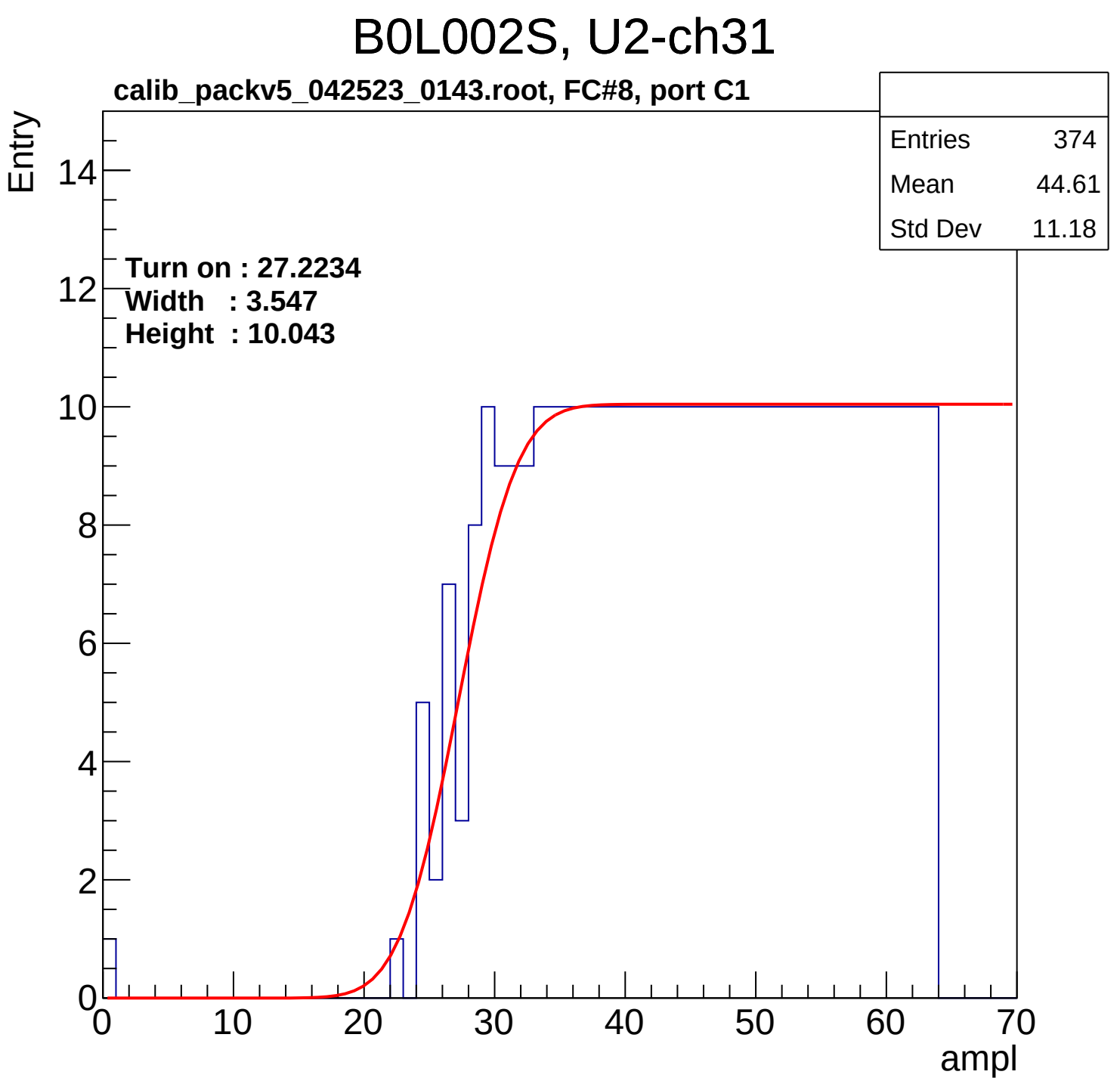
B0L002S, U2-ch31
calib_packv5_042523_0143.root, FC#8, port C1
Entries 374
Mean 44.61
Std Dev 11.18
Turn on : 27.2234
Width : 3.547
Height : 10.043
Entry
ampl
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2
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6
8
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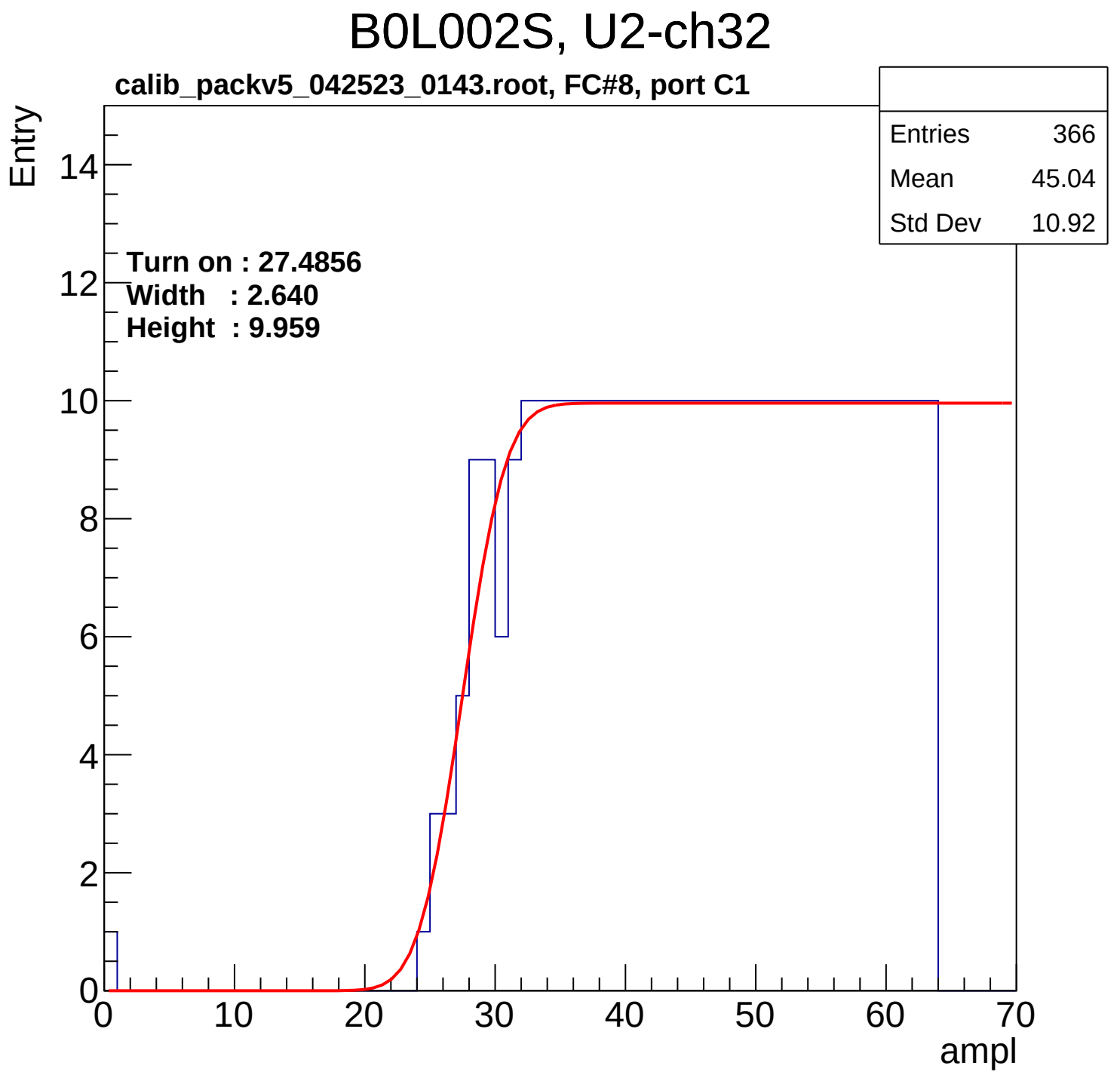
B0L002S, U2-ch32
calib_packv5_042523_0143.root, FC#8, port C1
Entries 366
Mean 45.04
Std Dev 10.92
Turn on : 27.4856
Width : 2.640
Height : 9.959
Entry
ampl
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4
6
8
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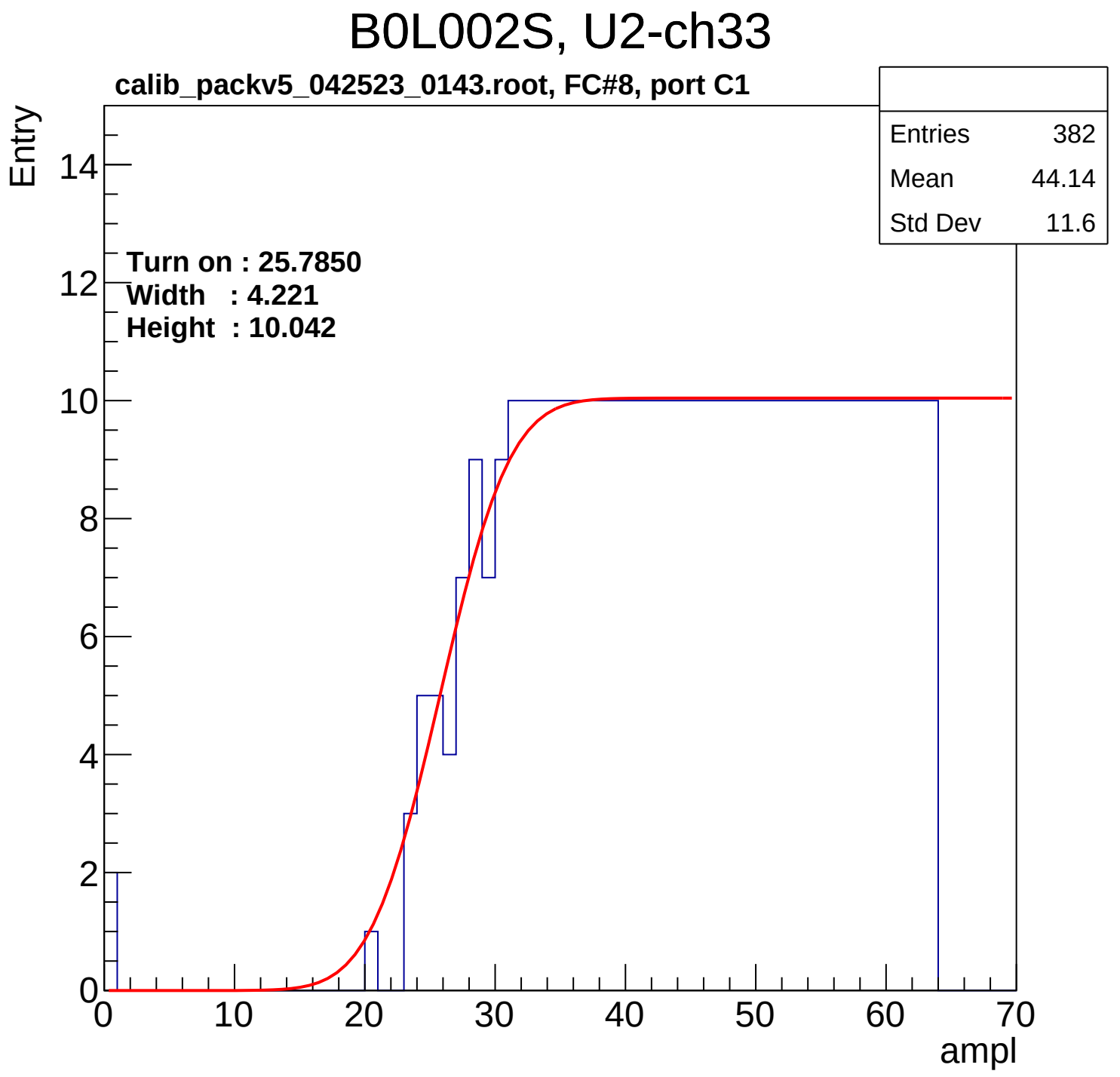
B0L002S, U2-ch33
calib_packv5_042523_0143.root, FC#8, port C1
Entries 382
Mean 44.14
Std Dev 11.6
Turn on : 25.7850
Width : 4.221
Height : 10.042
Entry
ampl
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2
4
6
8
10
12
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0
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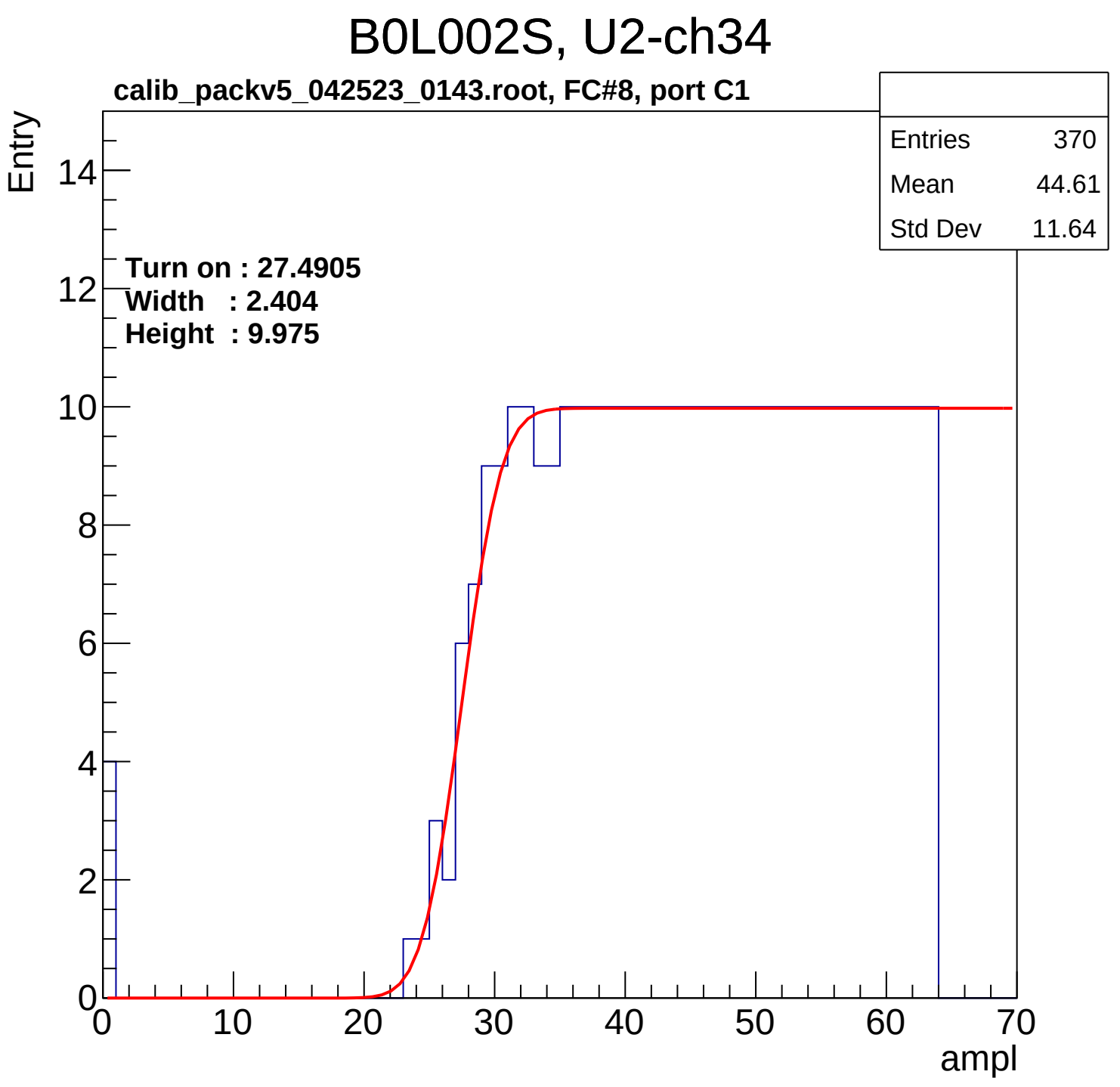
B0L002S, U2-ch34
calib_packv5_042523_0143.root, FC#8, port C1
Entries 370
Mean 44.61
Std Dev 11.64
Turn on : 27.4905
Width : 2.404
Height : 9.975
Entry
ampl
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2
4
6
8
10
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0
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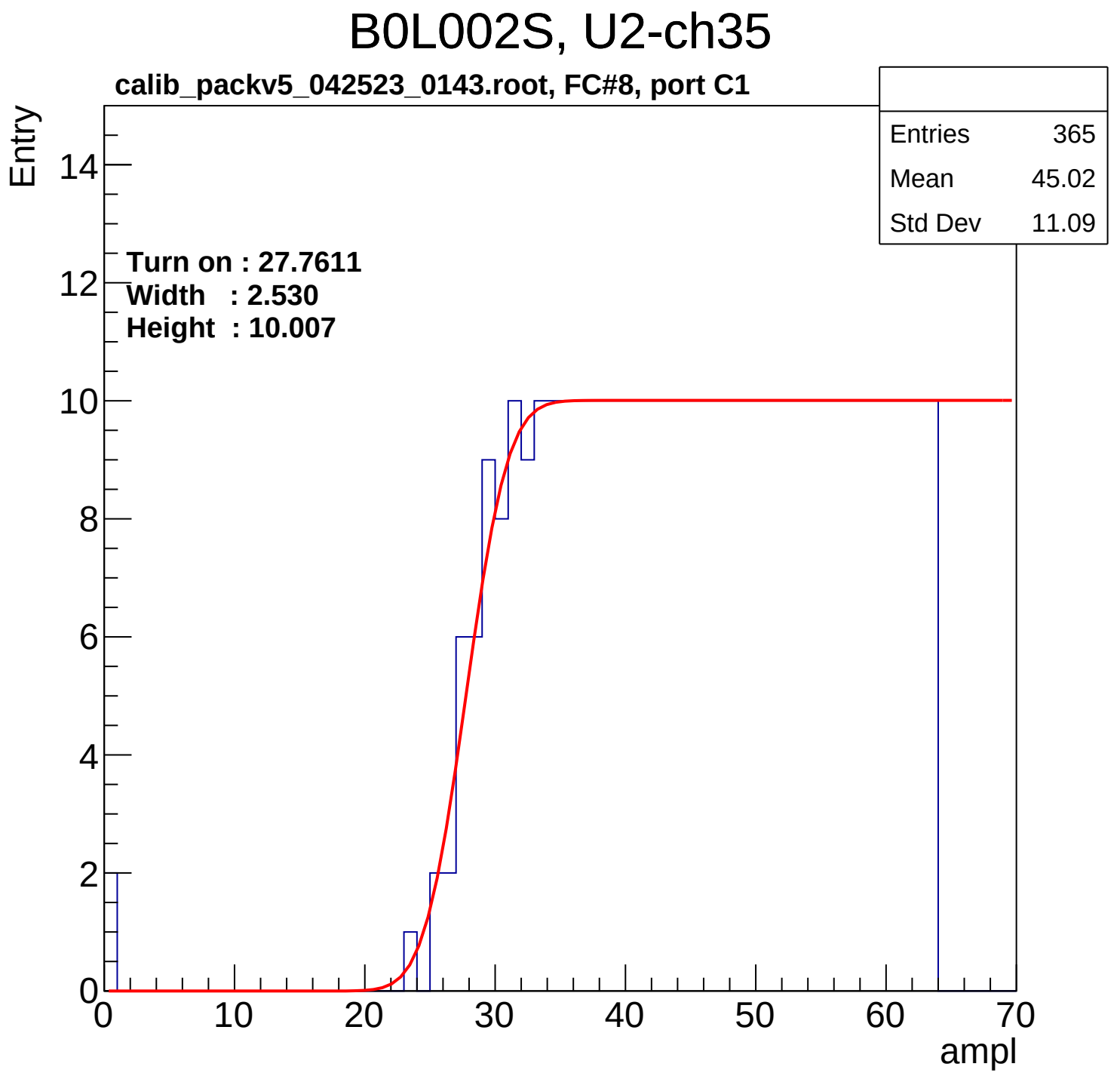
B0L002S, U2-ch35
calib_packv5_042523_0143.root, FC#8, port C1
Entries 365
Mean 45.02
Std Dev 11.09
Turn on : 27.7611
Width : 2.530
Height : 10.007
Entry
ampl
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4
6
8
10
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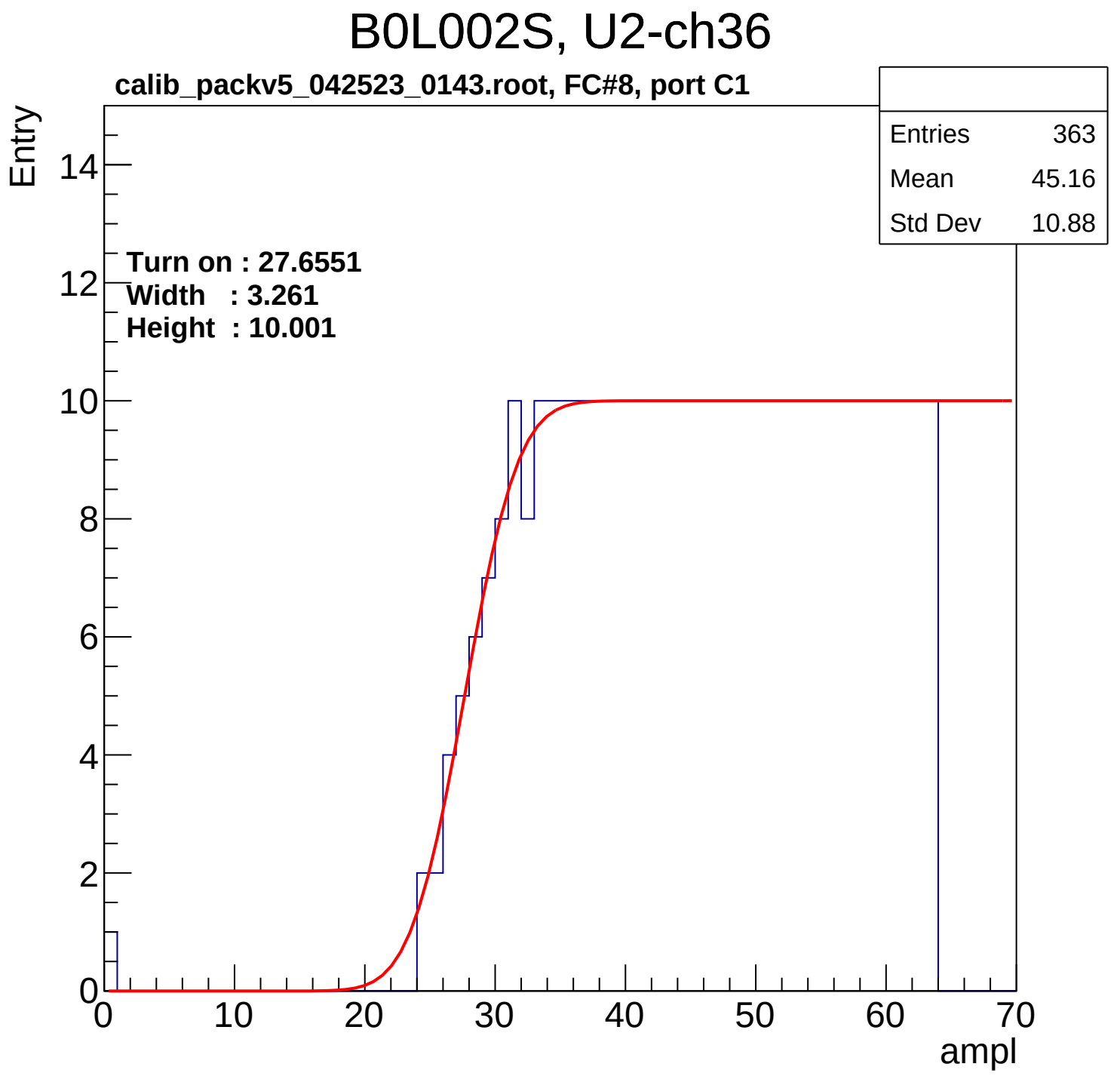
B0L002S, U2-ch36
calib_packv5_042523_0143.root, FC#8, port C1
Entries 363
Mean 45.16
Std Dev 10.88
Turn on : 27.6551
Width : 3.261
Height : 10.001
Entry
ampl
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2
4
6
8
10
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0
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40
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60
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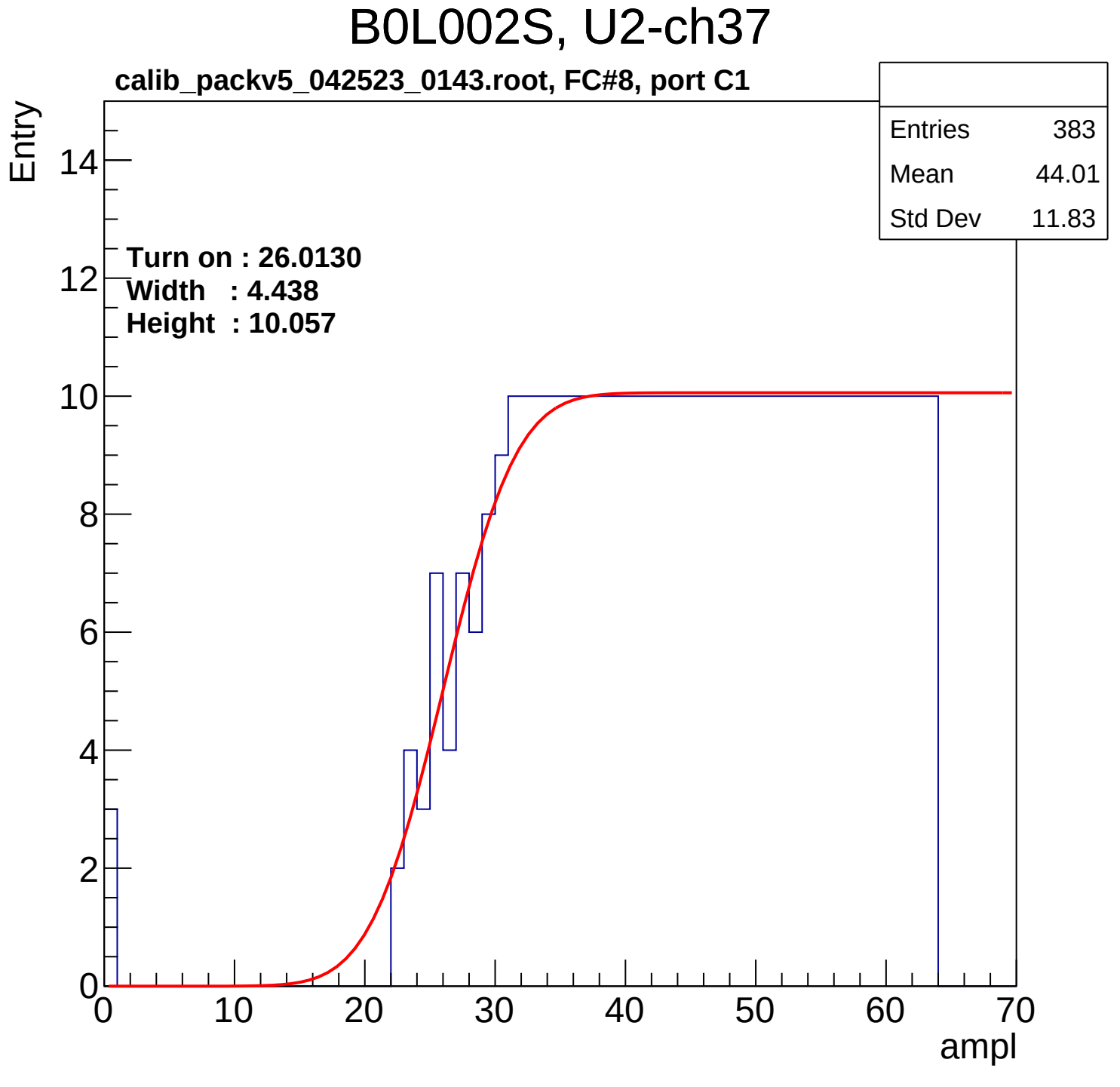
B0L002S, U2-ch37
calib_packv5_042523_0143.root, FC#8, port C1
Entries 383
Mean 44.01
Std Dev 11.83
Turn on : 26.0130
Width : 4.438
Height : 10.057
Entry
ampl
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4
6
8
10
12
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0
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60
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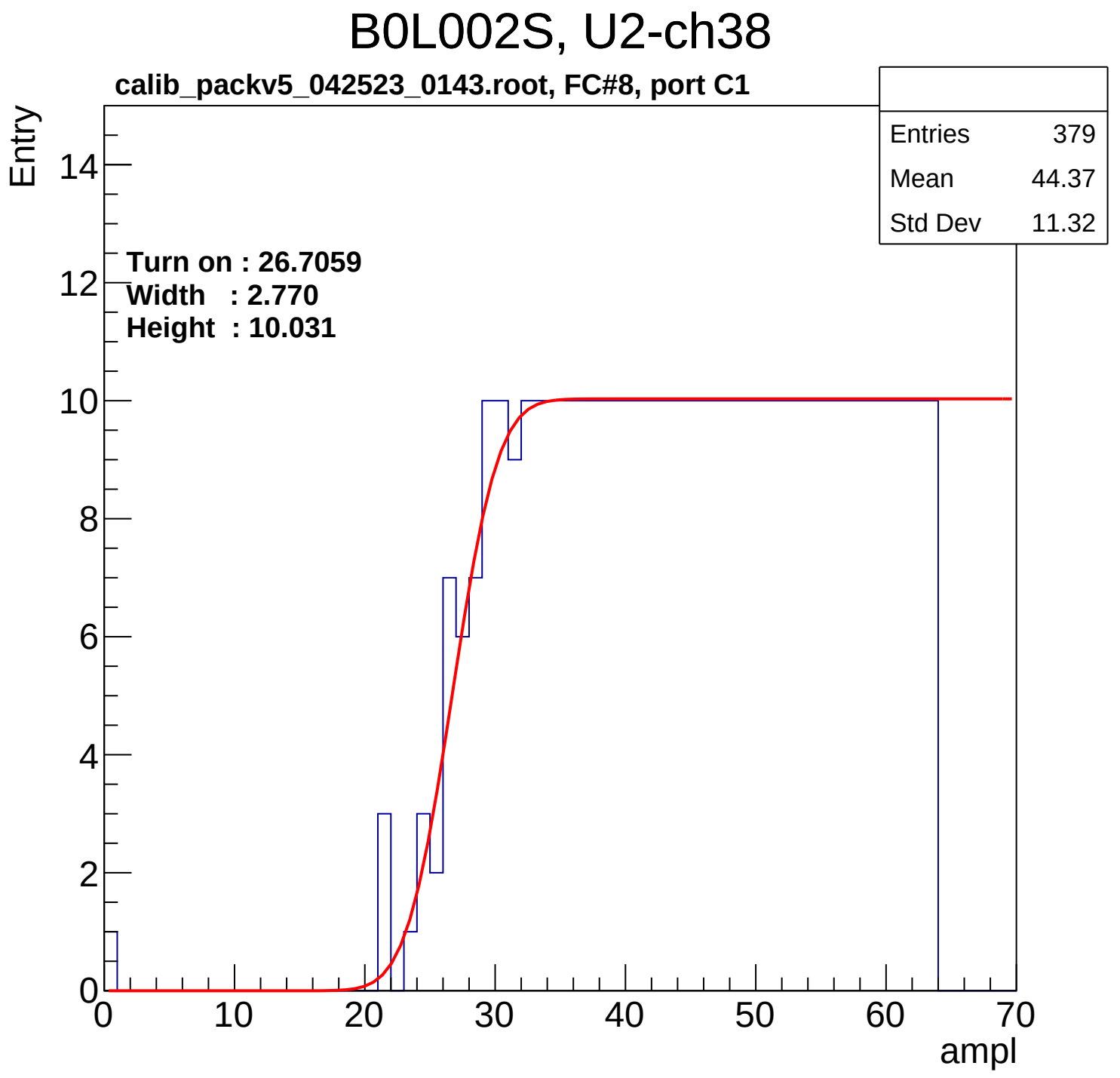
B0L002S, U2-ch38
calib_packv5_042523_0143.root, FC#8, port C1
Entries 379
Mean 44.37
Std Dev 11.32
Turn on : 26.7059
Width : 2.770
Height : 10.031
Entry
ampl
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2
4
6
8
10
12
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0
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20
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40
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60
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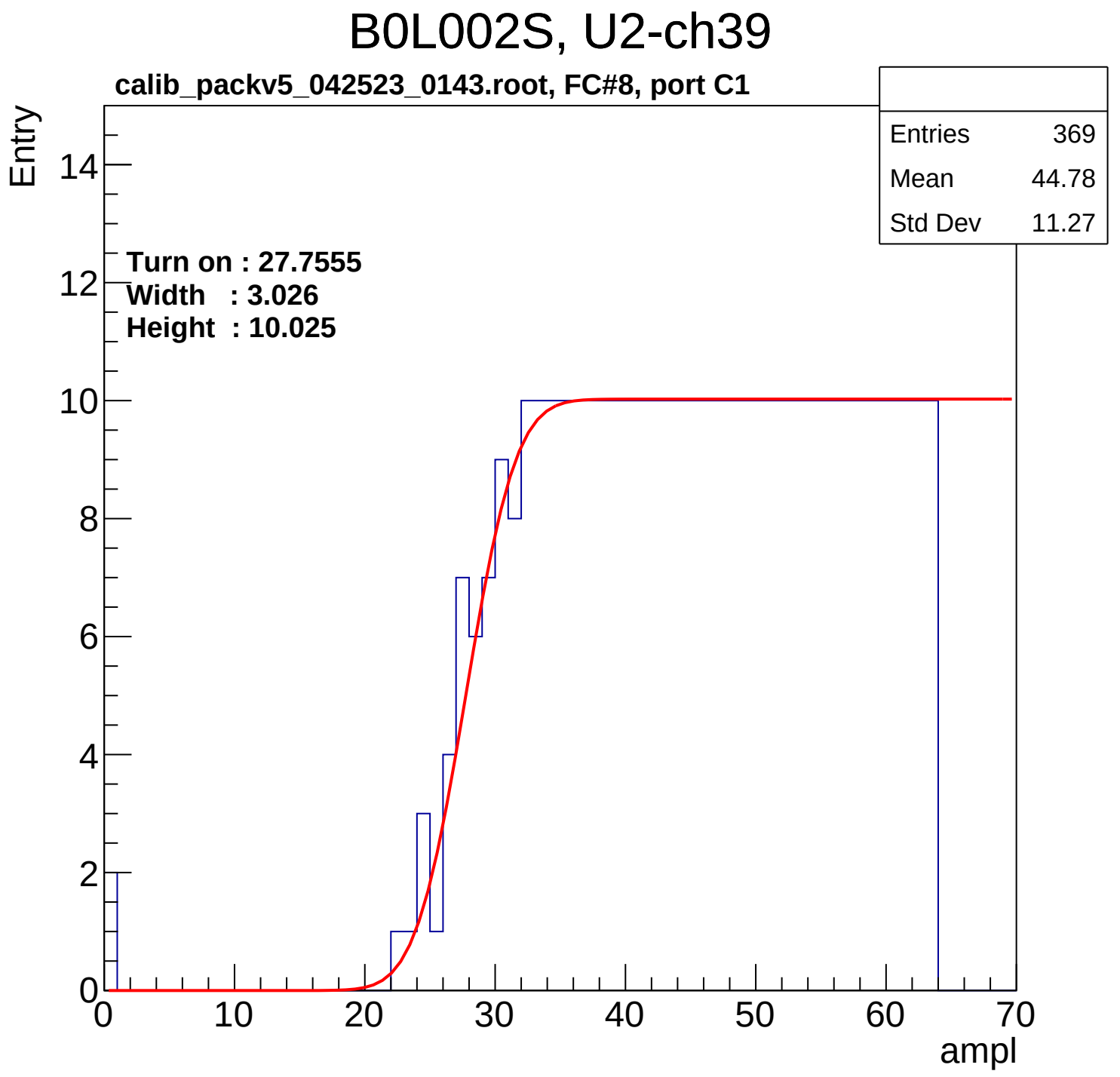
B0L002S, U2-ch39
calib_packv5_042523_0143.root, FC#8, port C1
Entries 369
Mean 44.78
Std Dev 11.27
Turn on : 27.7555
Width : 3.026
Height : 10.025
Entry
ampl
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6
8
10
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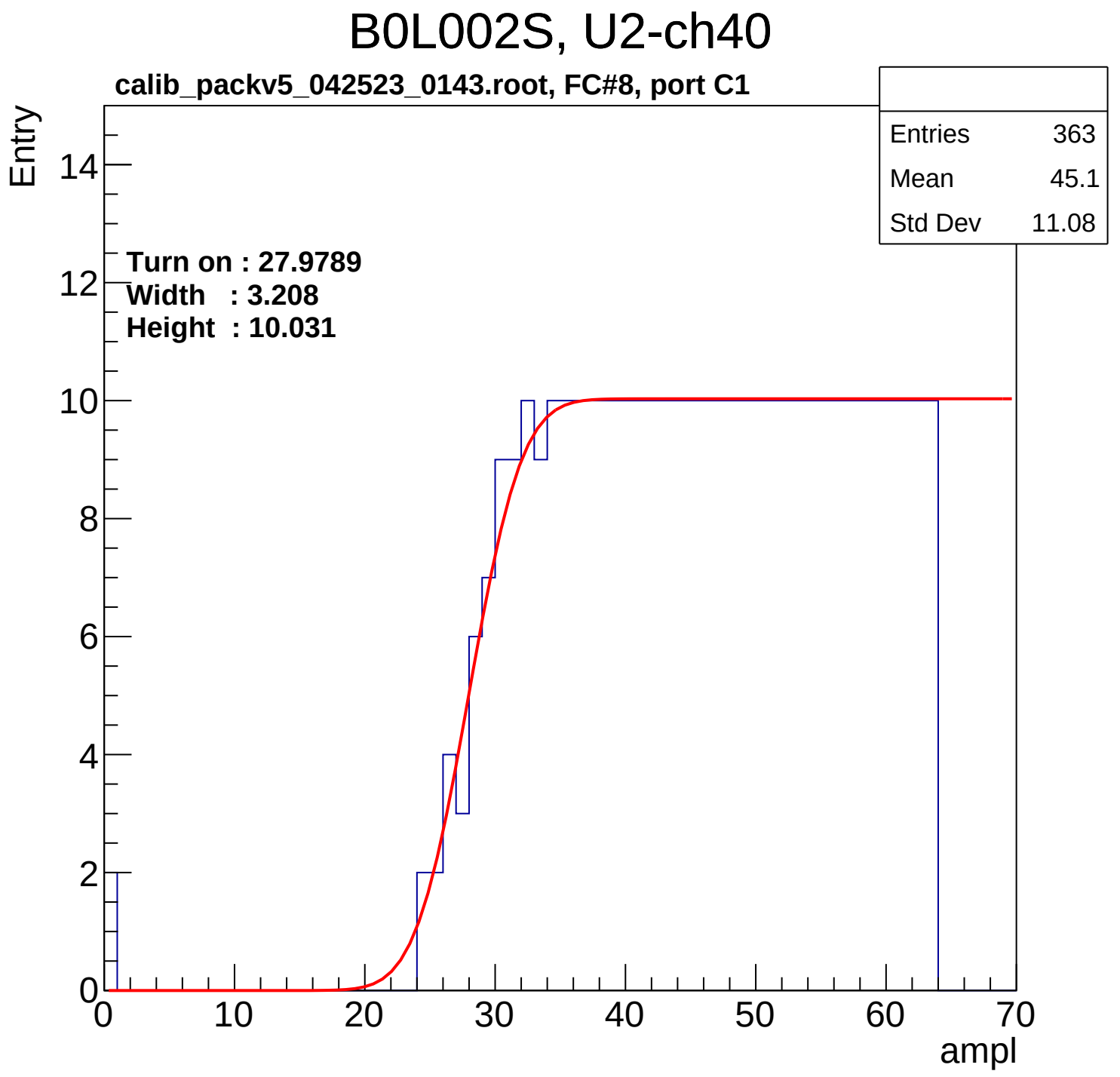
B0L002S, U2-ch40
calib_packv5_042523_0143.root, FC#8, port C1
Entries 363
Mean 45.1
Std Dev 11.08
Turn on : 27.9789
Width : 3.208
Height : 10.031
Entry
ampl
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6
8
10
12
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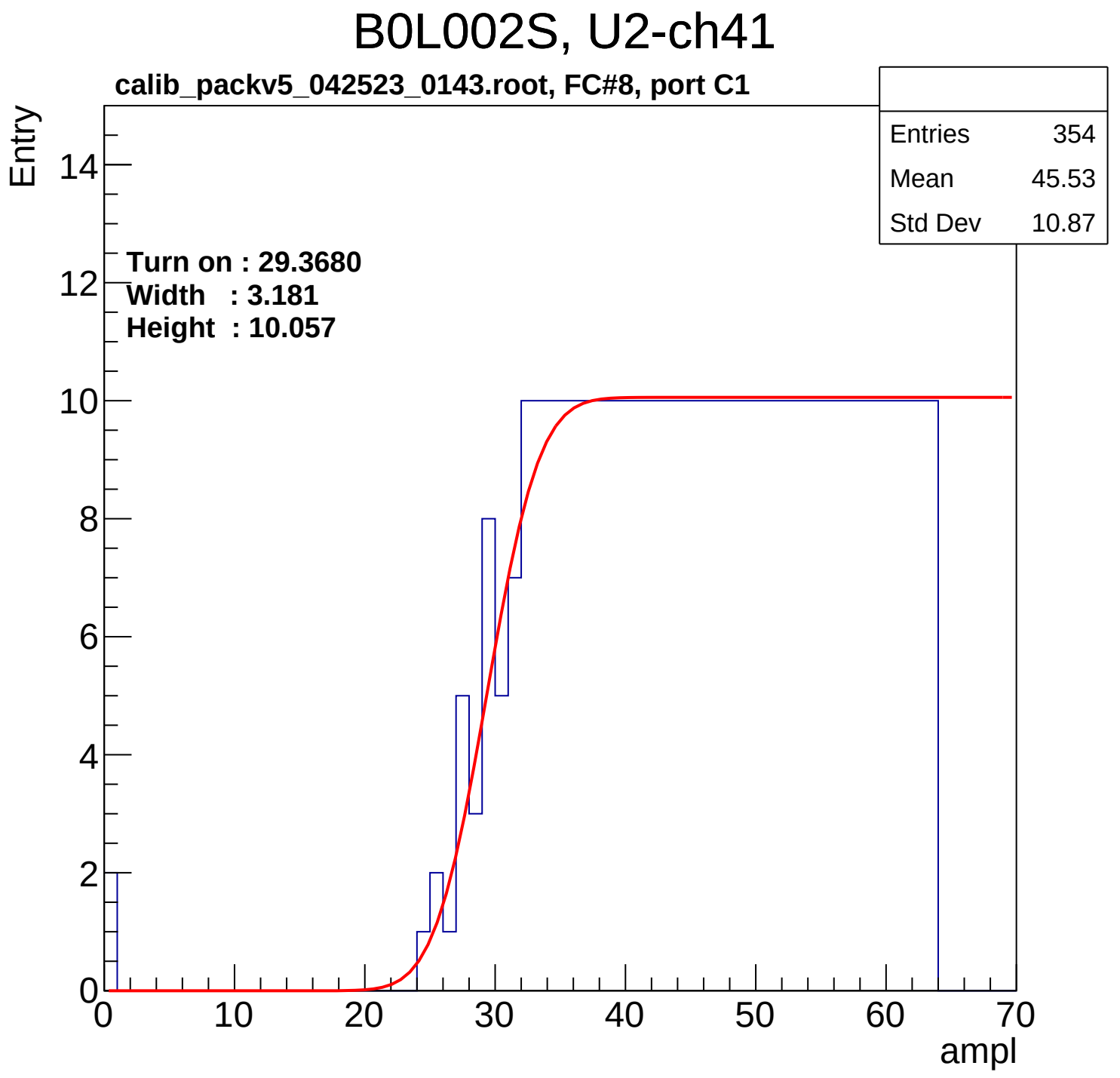
B0L002S, U2-ch41
calib_packv5_042523_0143.root, FC#8, port C1
Entries 354
Mean 45.53
Std Dev 10.87
Turn on : 29.3680
Width : 3.181
Height : 10.057
Entry
ampl
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6
8
10
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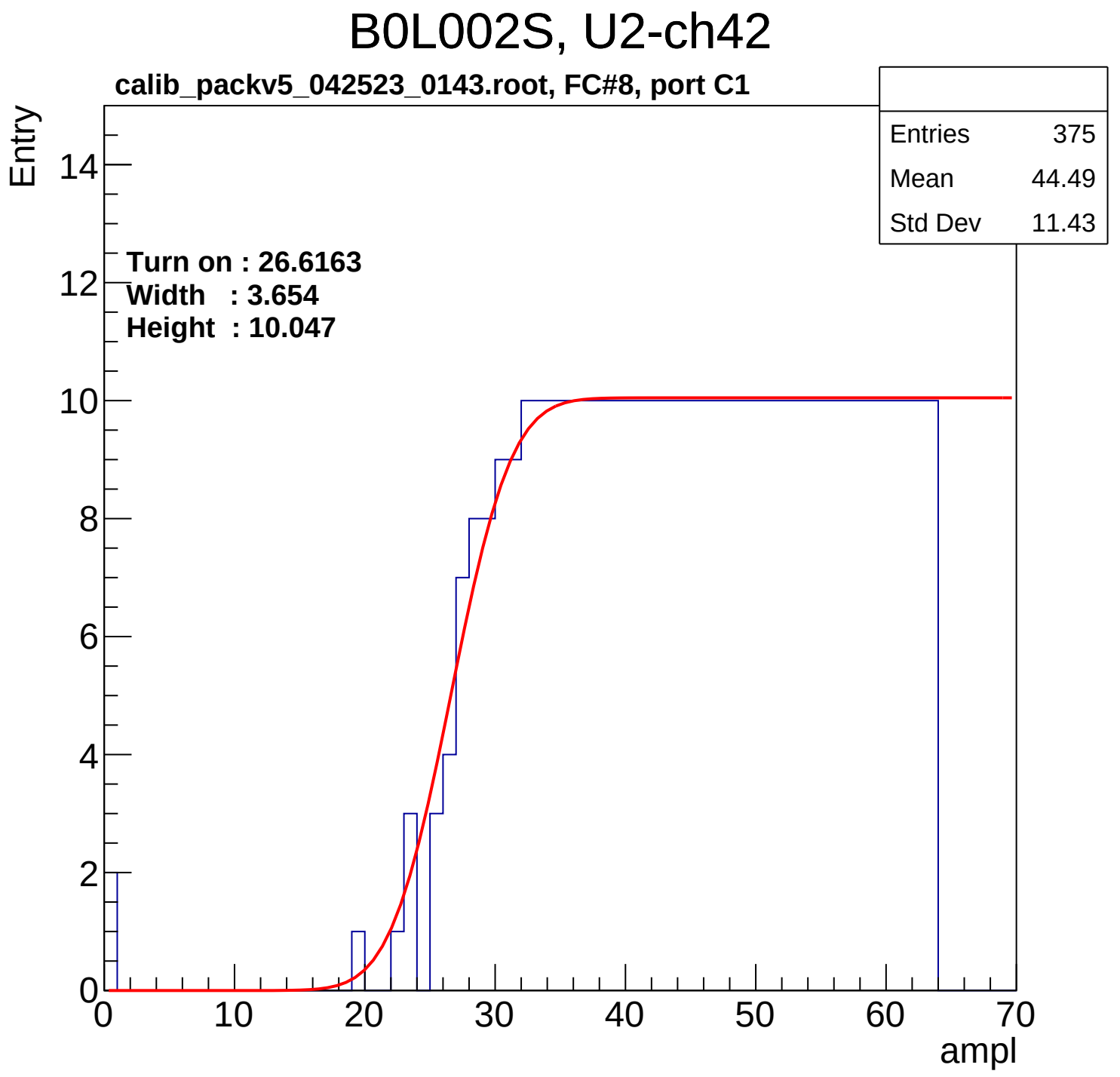
B0L002S, U2-ch42
calib_packv5_042523_0143.root, FC#8, port C1
Entries 375
Mean 44.49
Std Dev 11.43
Turn on : 26.6163
Width : 3.654
Height : 10.047
Entry
ampl
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6
8
10
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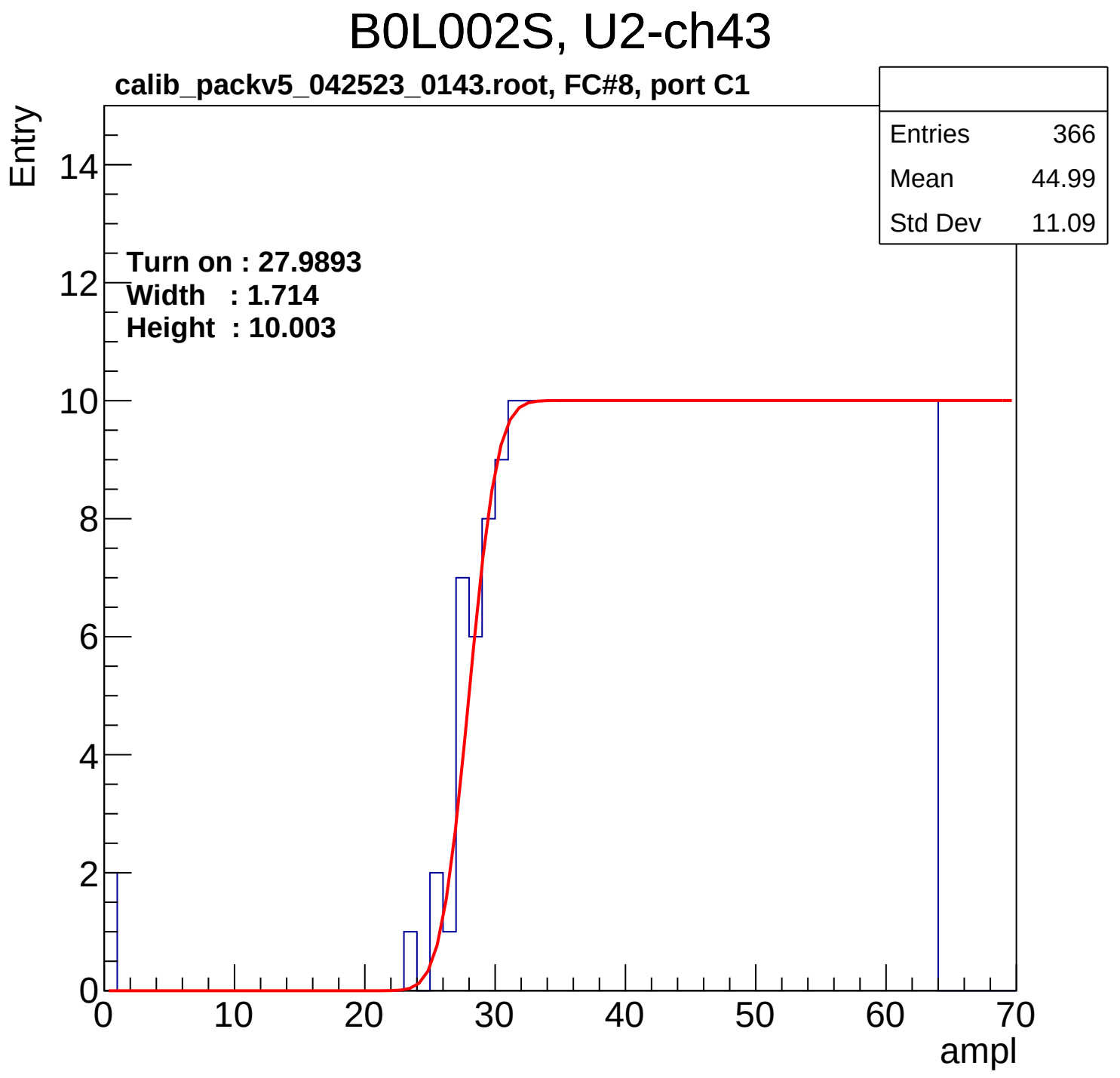
B0L002S, U2-ch43
calib_packv5_042523_0143.root, FC#8, port C1
Entries 366
Mean 44.99
Std Dev 11.09
Turn on : 27.9893
Width : 1.714
Height : 10.003
Entry
ampl
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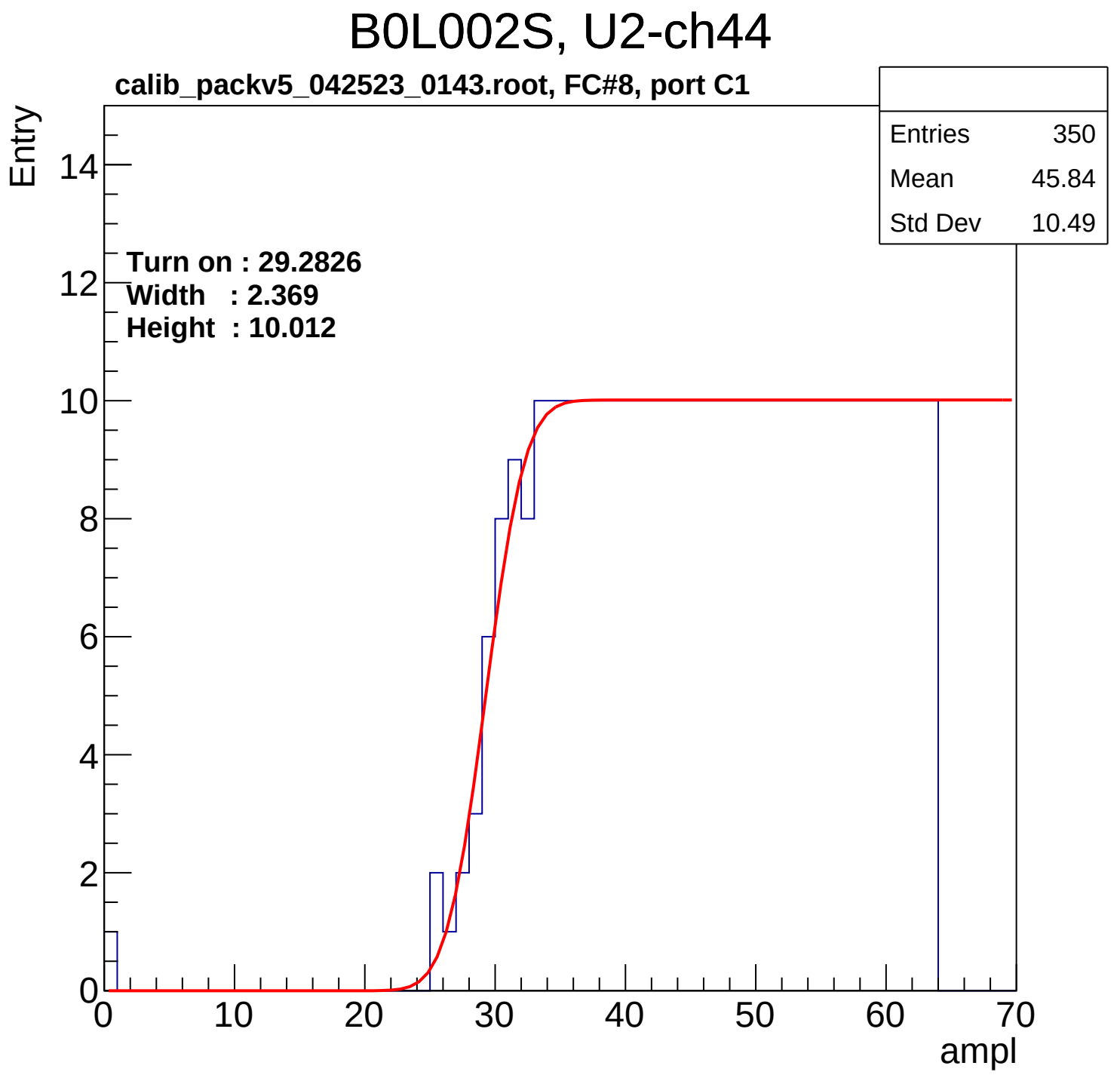
B0L002S, U2-ch44
calib_packv5_042523_0143.root, FC#8, port C1
Entries 350
Mean 45.84
Std Dev 10.49
Turn on : 29.2826
Width : 2.369
Height : 10.012
Entry
ampl
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8
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12
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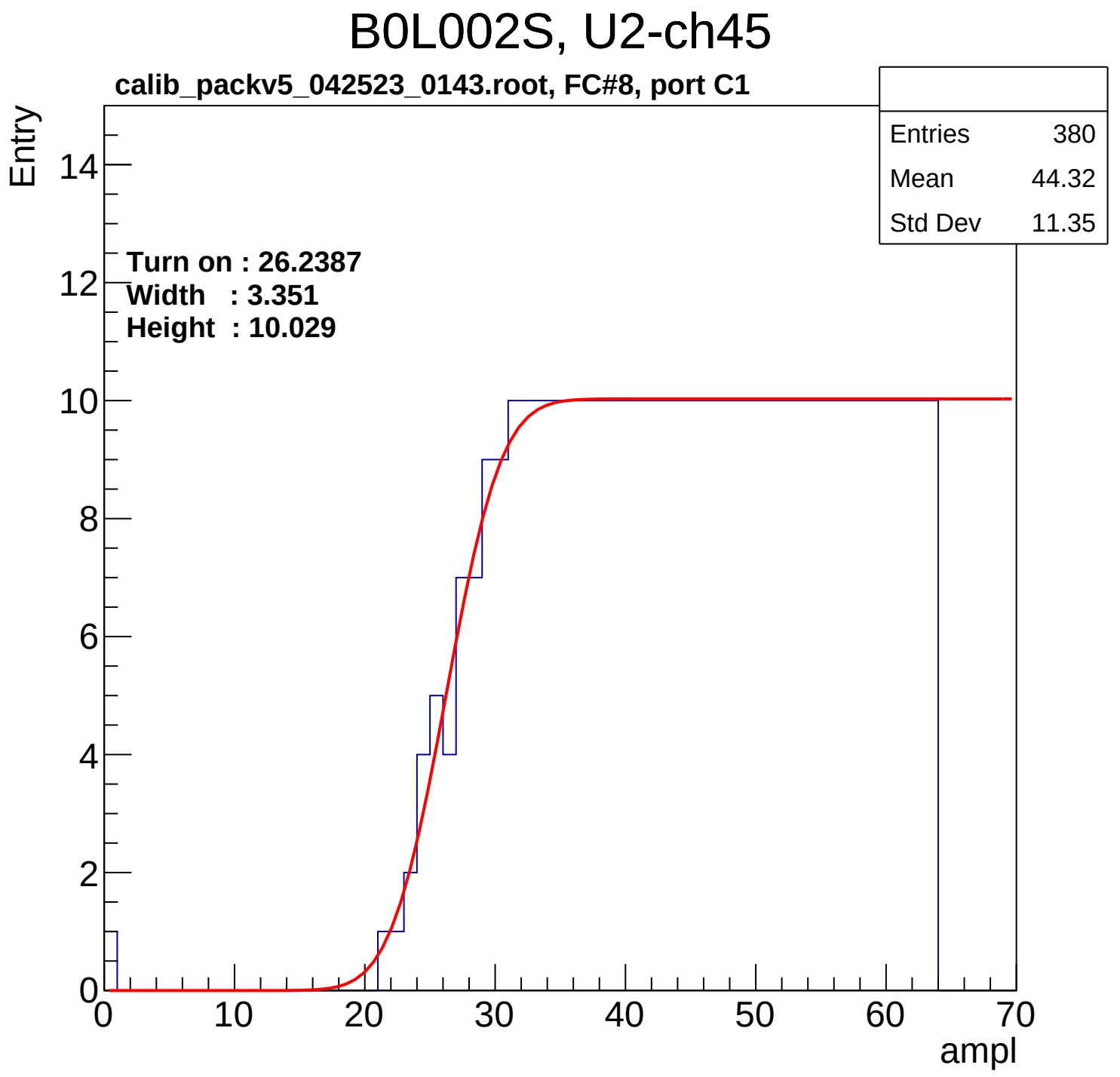
B0L002S, U2-ch45
calib_packv5_042523_0143.root, FC#8, port C1
Entries 380
Mean 44.32
Std Dev 11.35
Turn on : 26.2387
Width : 3.351
Height : 10.029
Entry
ampl
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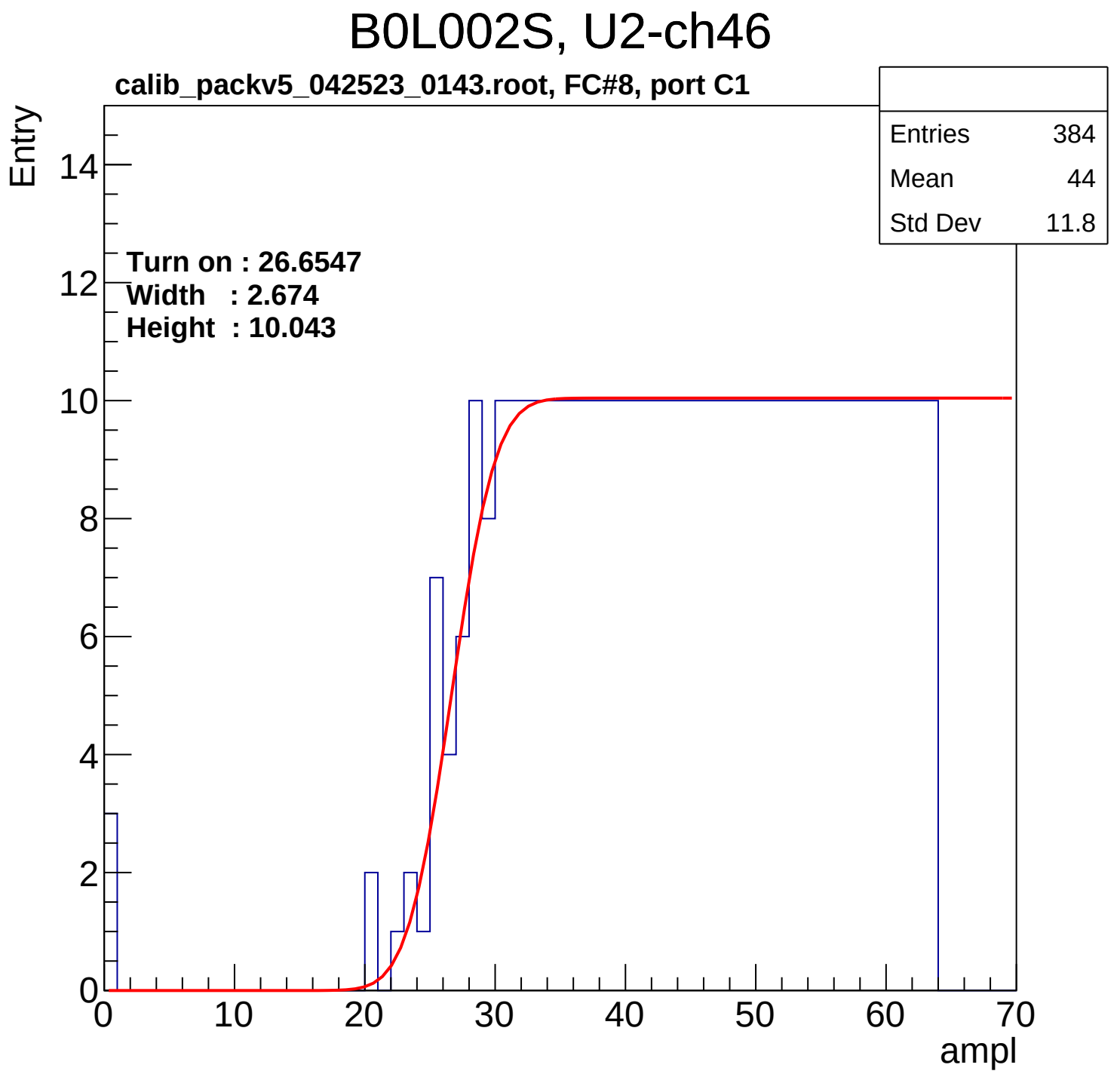
B0L002S, U2-ch46
calib_packv5_042523_0143.root, FC#8, port C1
Entries 384
Mean 44
Std Dev 11.8
Turn on : 26.6547
Width : 2.674
Height : 10.043
Entry
ampl
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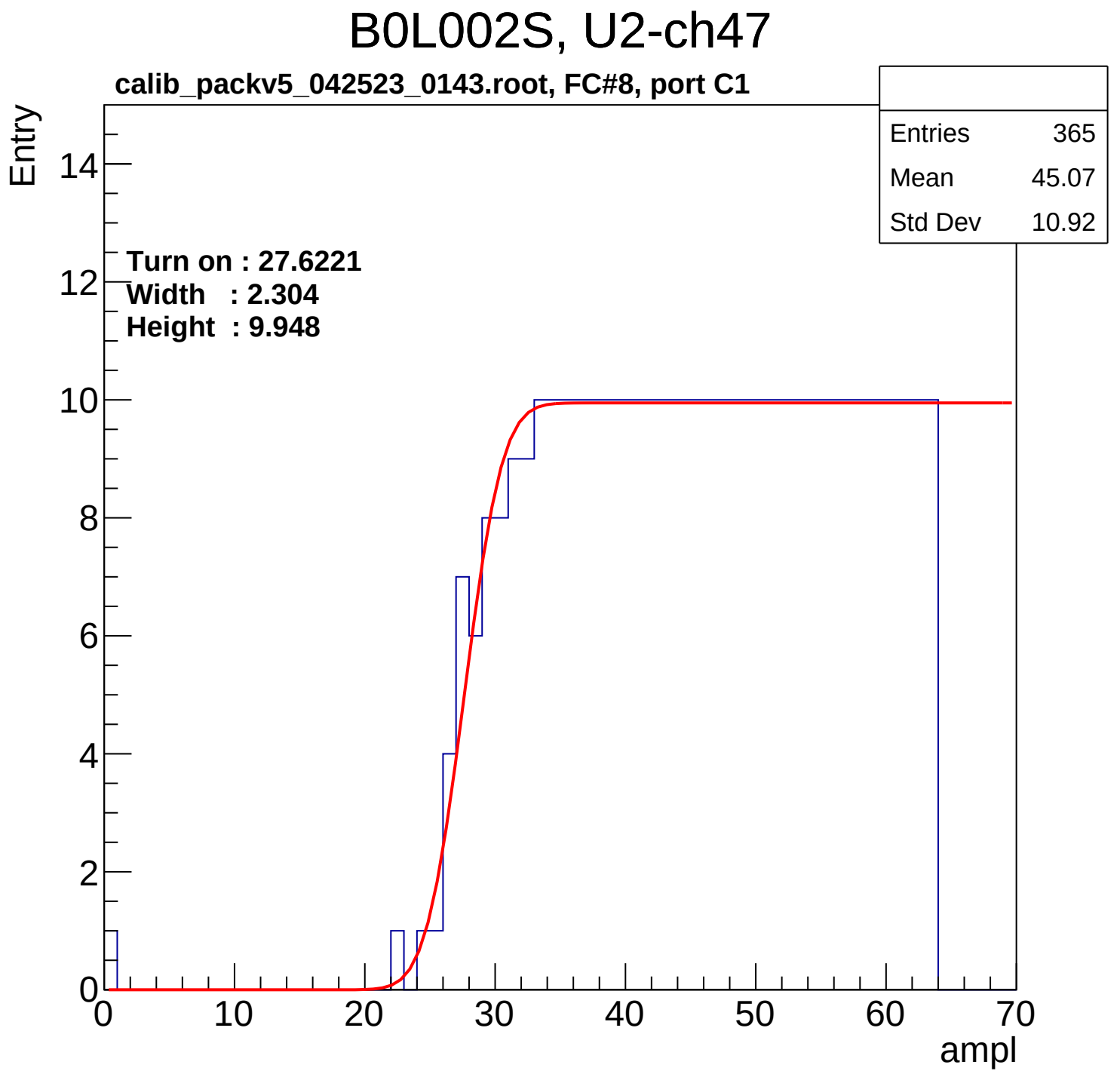
B0L002S, U2-ch47
calib_packv5_042523_0143.root, FC#8, port C1
Entries 365
Mean 45.07
Std Dev 10.92
Turn on : 27.6221
Width : 2.304
Height : 9.948
Entry
ampl
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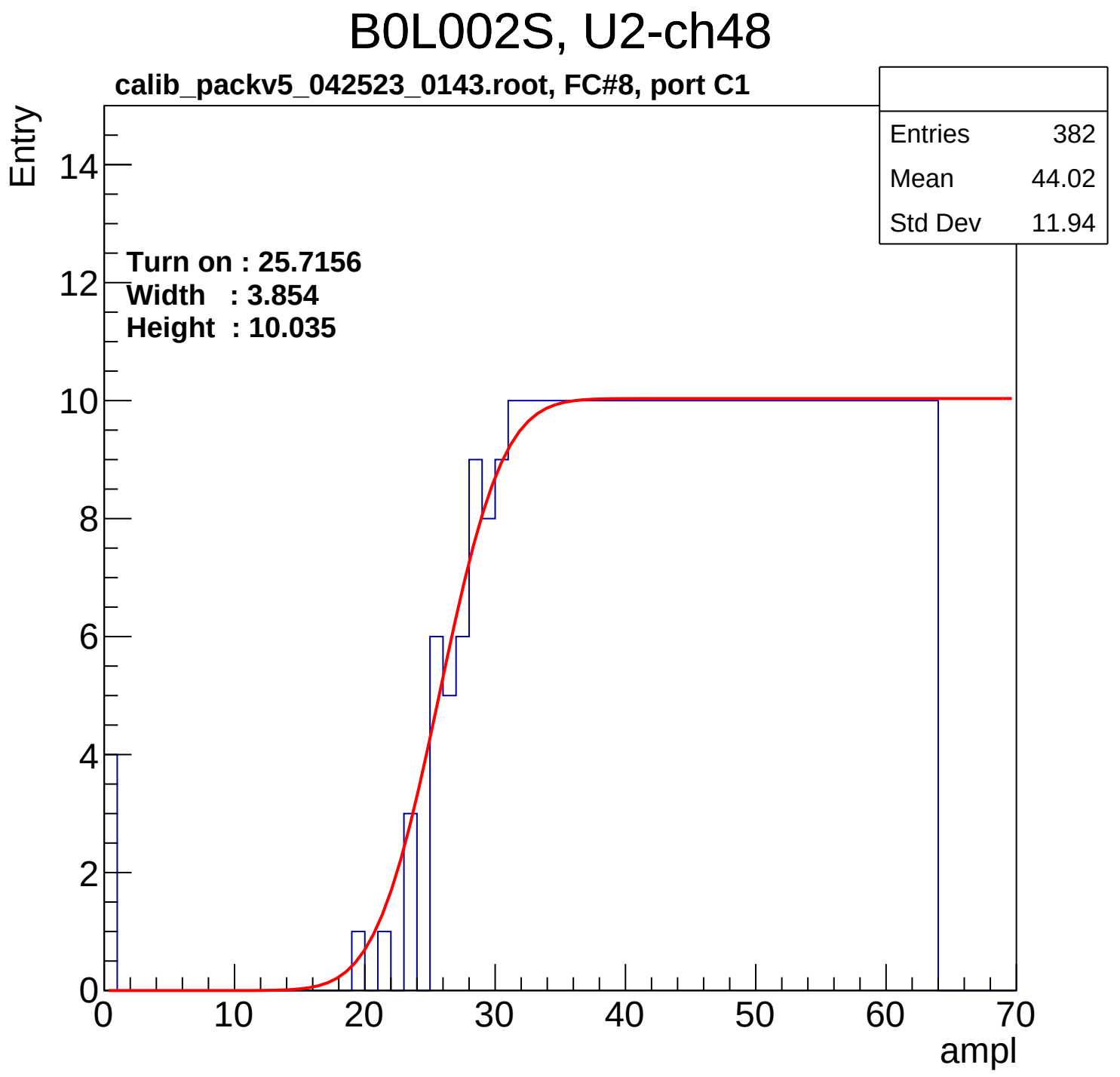
B0L002S, U2-ch48
calib_packv5_042523_0143.root, FC#8, port C1
Entries 382
Mean 44.02
Std Dev 11.94
Turn on : 25.7156
Width : 3.854
Height : 10.035
Entry
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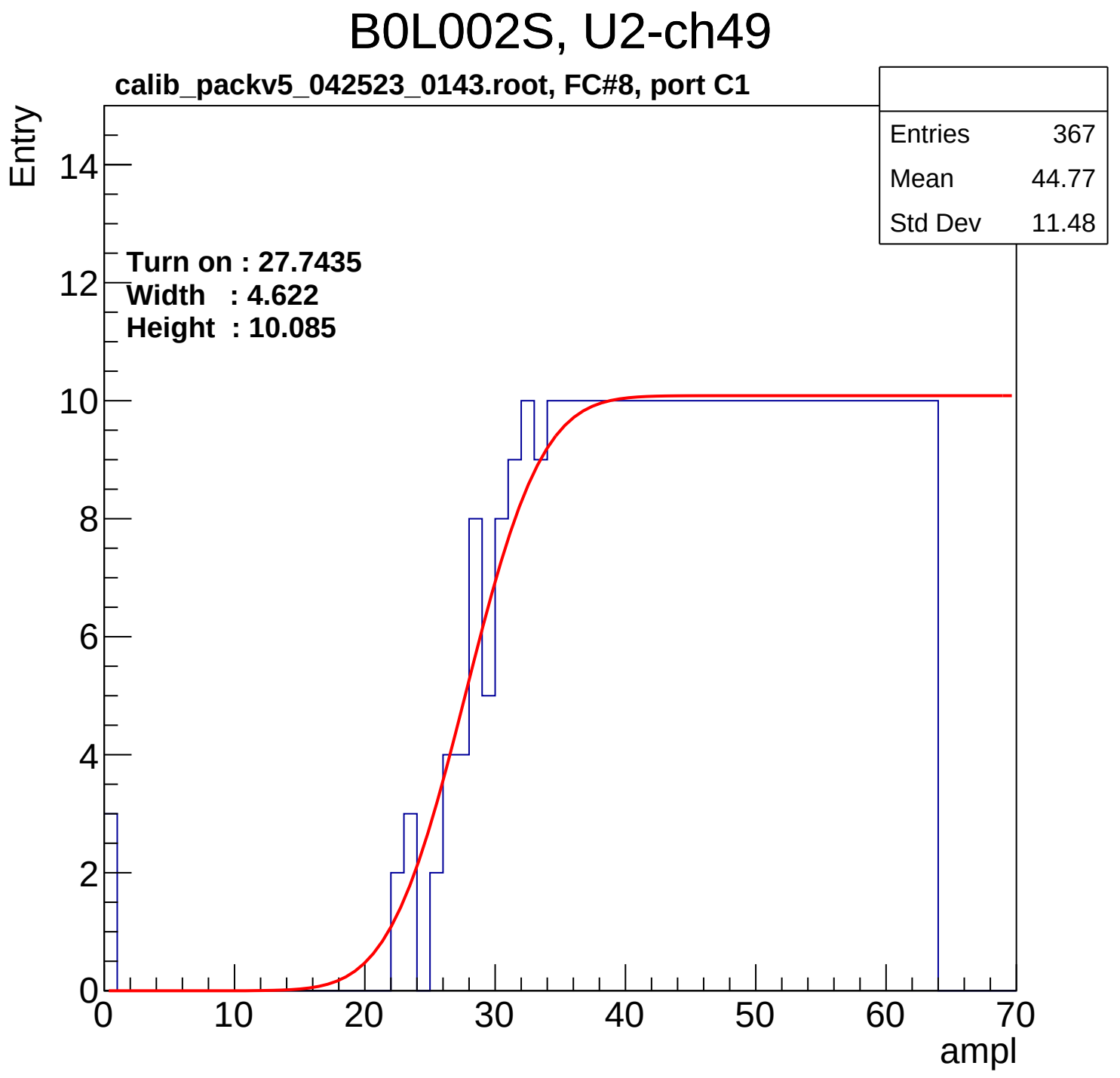
B0L002S, U2-ch49
calib_packv5_042523_0143.root, FC#8, port C1
Entries 367
Mean 44.77
Std Dev 11.48
Turn on : 27.7435
Width : 4.622
Height : 10.085
Entry
ampl
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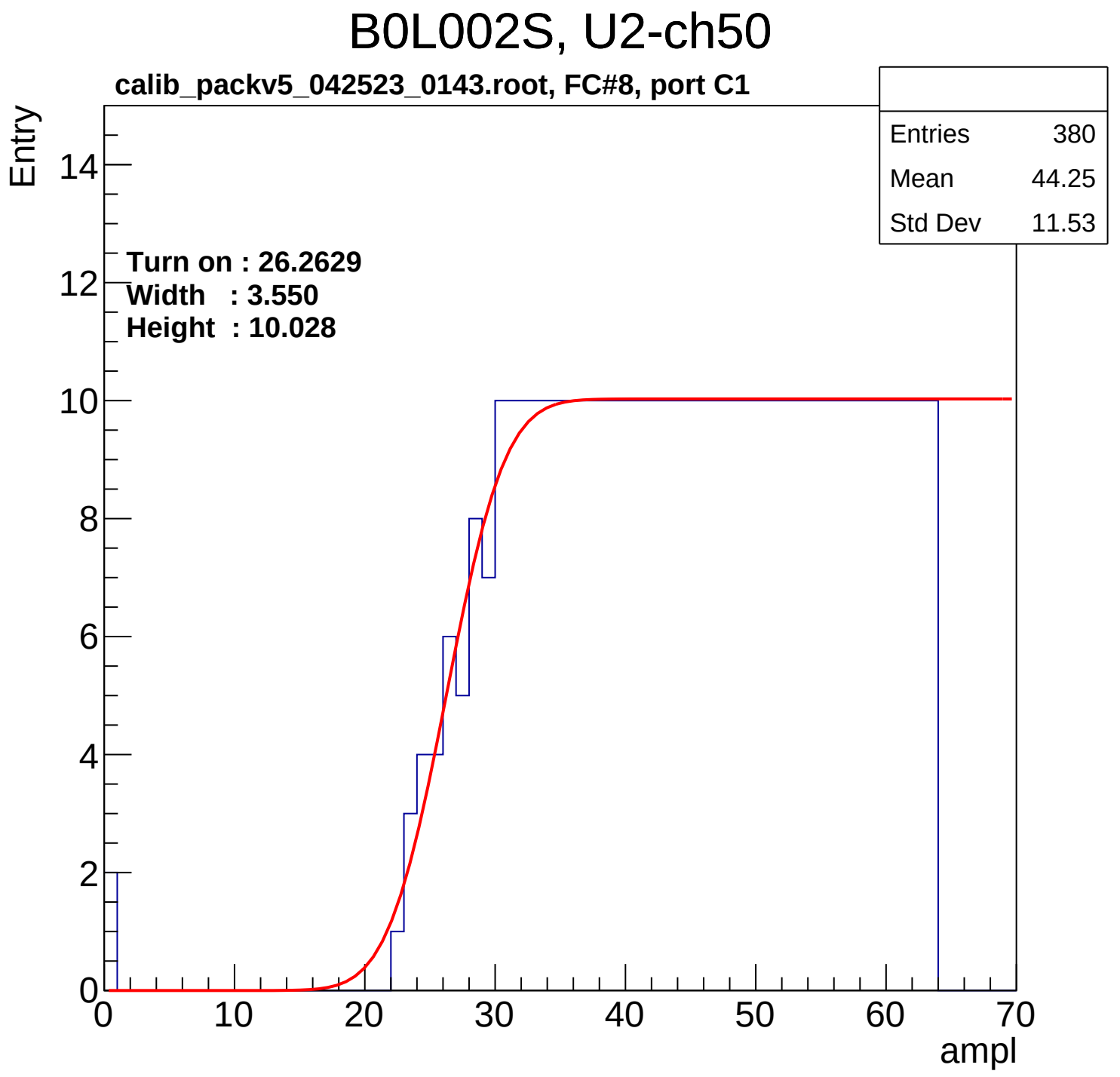
B0L002S, U2-ch50
calib_packv5_042523_0143.root, FC#8, port C1
Entries 380
Mean 44.25
Std Dev 11.53
Turn on : 26.2629
Width : 3.550
Height : 10.028
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ampl
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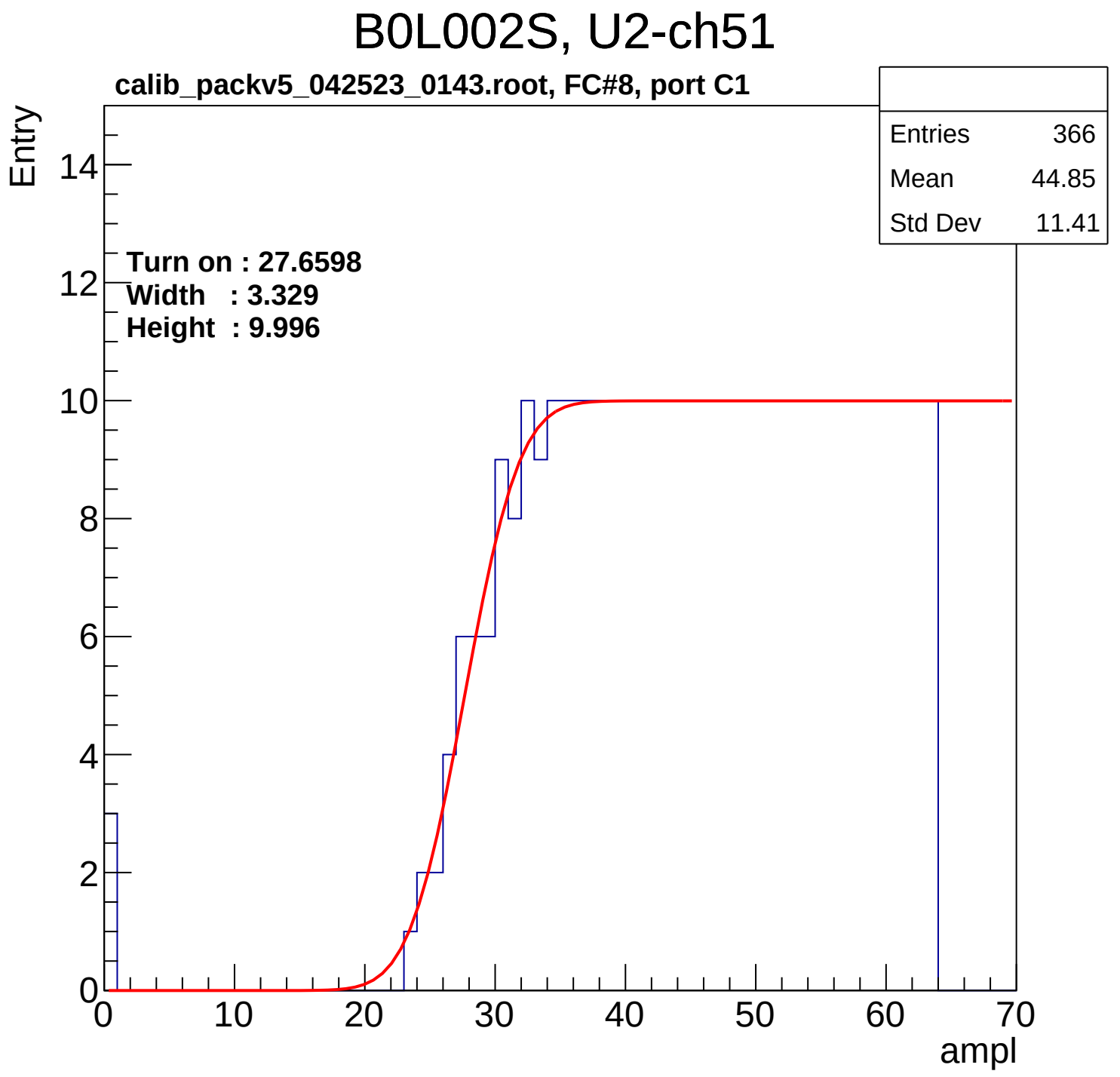
B0L002S, U2-ch51
calib_packv5_042523_0143.root, FC#8, port C1
Entries 366
Mean 44.85
Std Dev 11.41
Turn on : 27.6598
Width : 3.329
Height : 9.996
Entry
ampl
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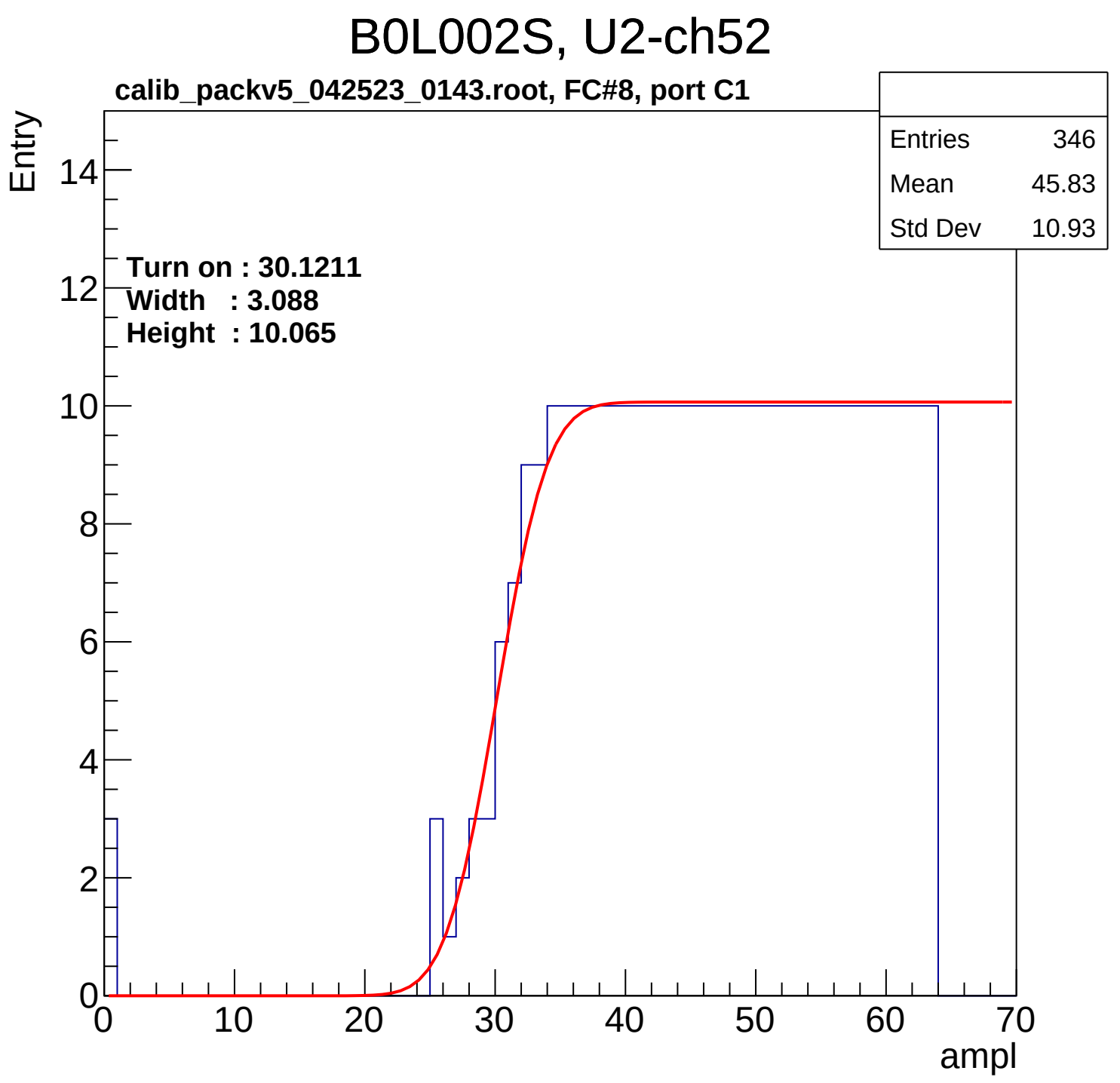
B0L002S, U2-ch52
calib_packv5_042523_0143.root, FC#8, port C1
Entries 346
Mean 45.83
Std Dev 10.93
Turn on : 30.1211
Width : 3.088
Height : 10.065
Entry
ampl
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8
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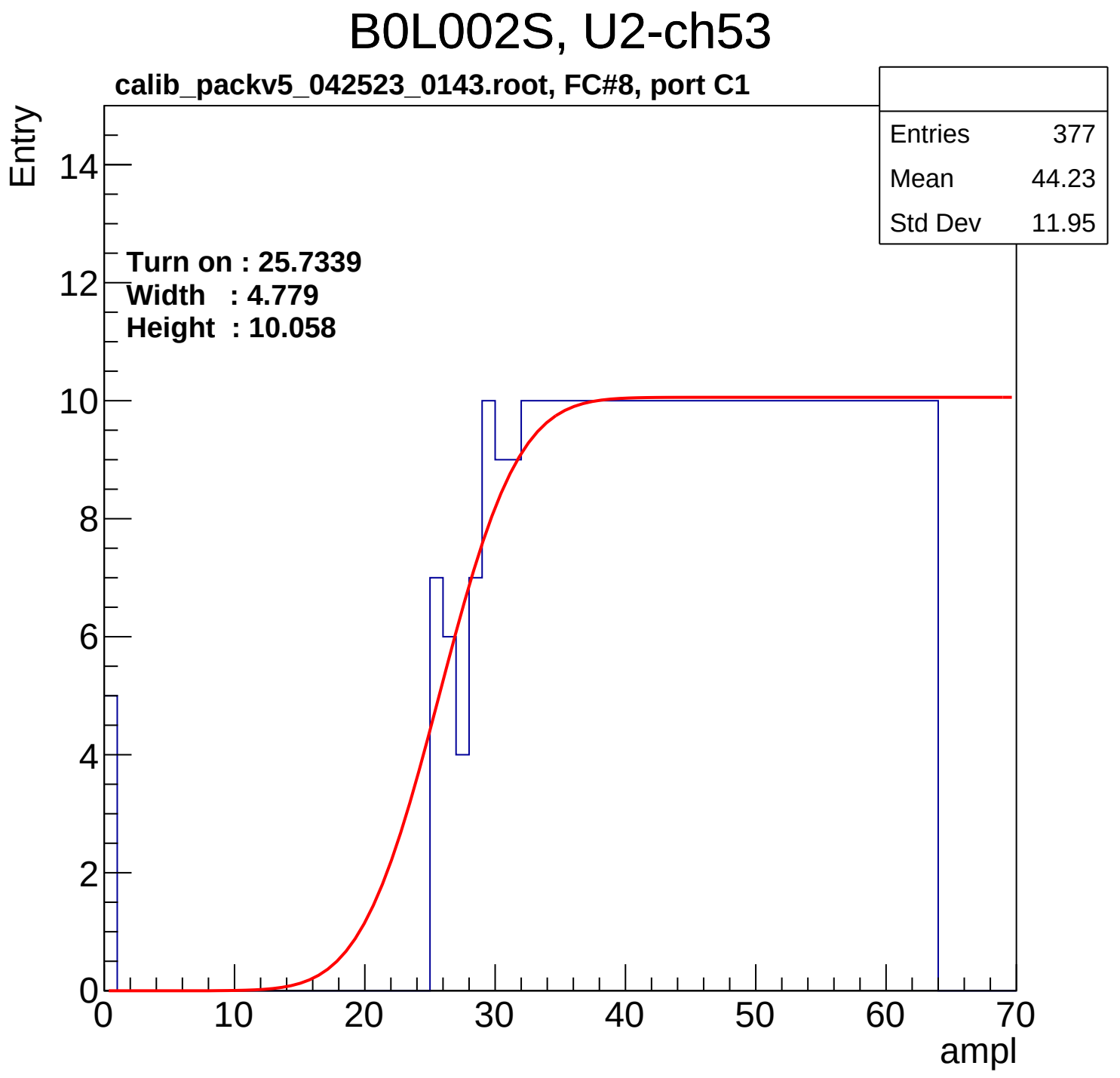
B0L002S, U2-ch53
calib_packv5_042523_0143.root, FC#8, port C1
Entries 377
Mean 44.23
Std Dev 11.95
Turn on : 25.7339
Width : 4.779
Height : 10.058
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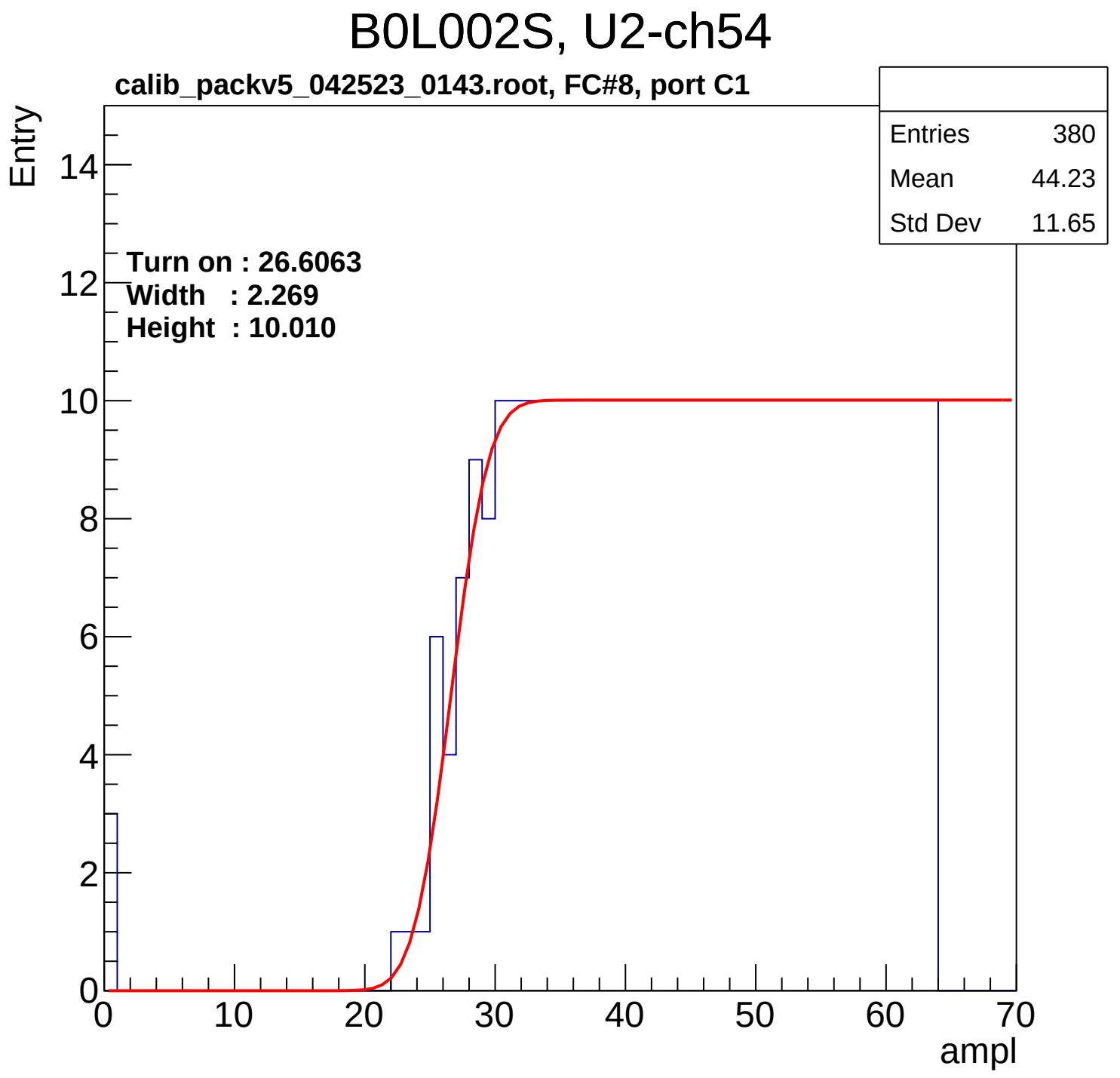
B0L002S, U2-ch54
calib_packv5_042523_0143.root, FC#8, port C1
Entries 380
Mean 44.23
Std Dev 11.65
Turn on : 26.6063
Width : 2.269
Height : 10.010
Entry
ampl
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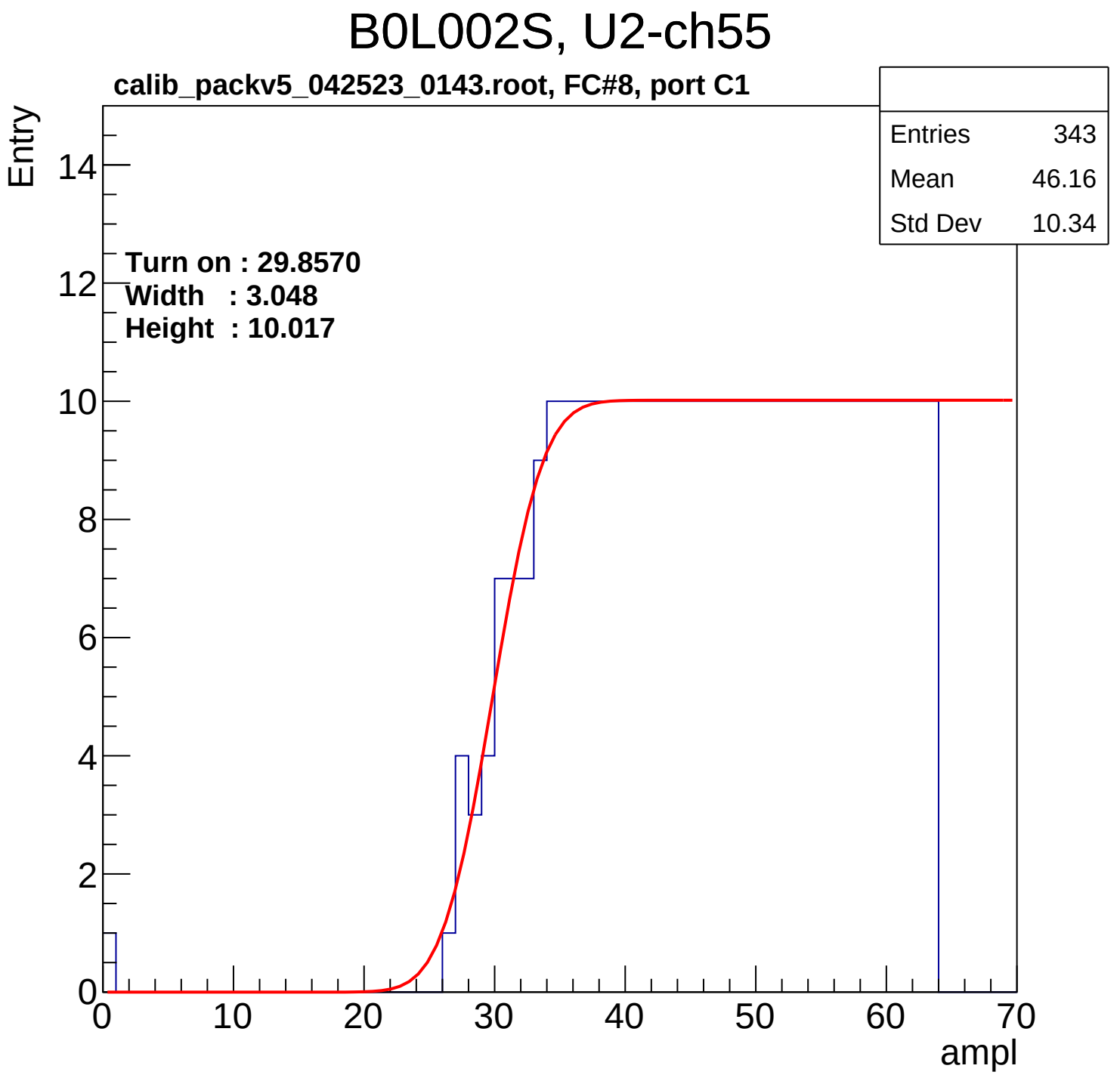
B0L002S, U2-ch55
calib_packv5_042523_0143.root, FC#8, port C1
Entries 343
Mean 46.16
Std Dev 10.34
Turn on : 29.8570
Width : 3.048
Height : 10.017
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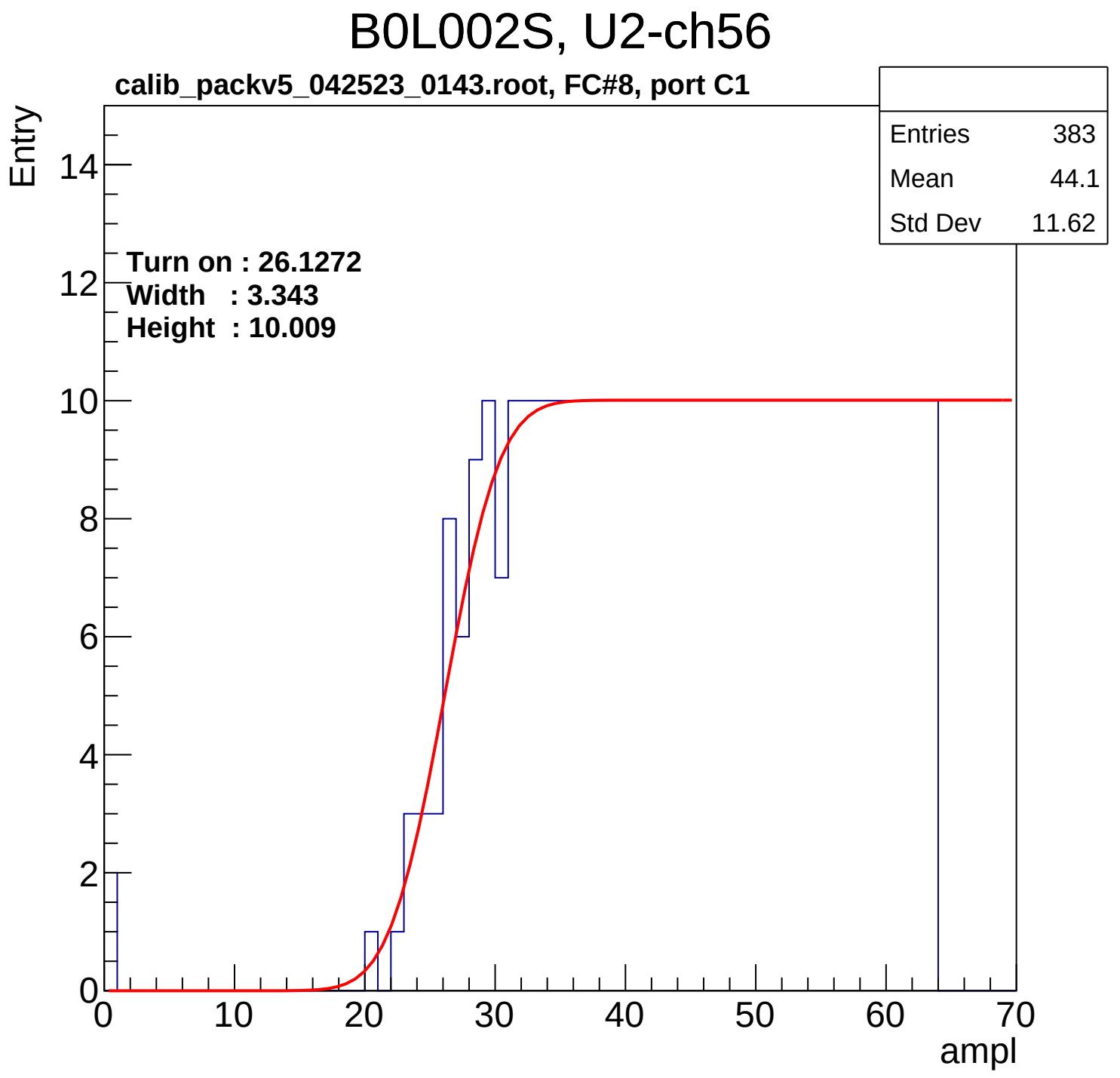
B0L002S, U2-ch56
calib_packv5_042523_0143.root, FC#8, port C1
Entries 383
Mean 44.1
Std Dev 11.62
Turn on : 26.1272
Width : 3.343
Height : 10.009
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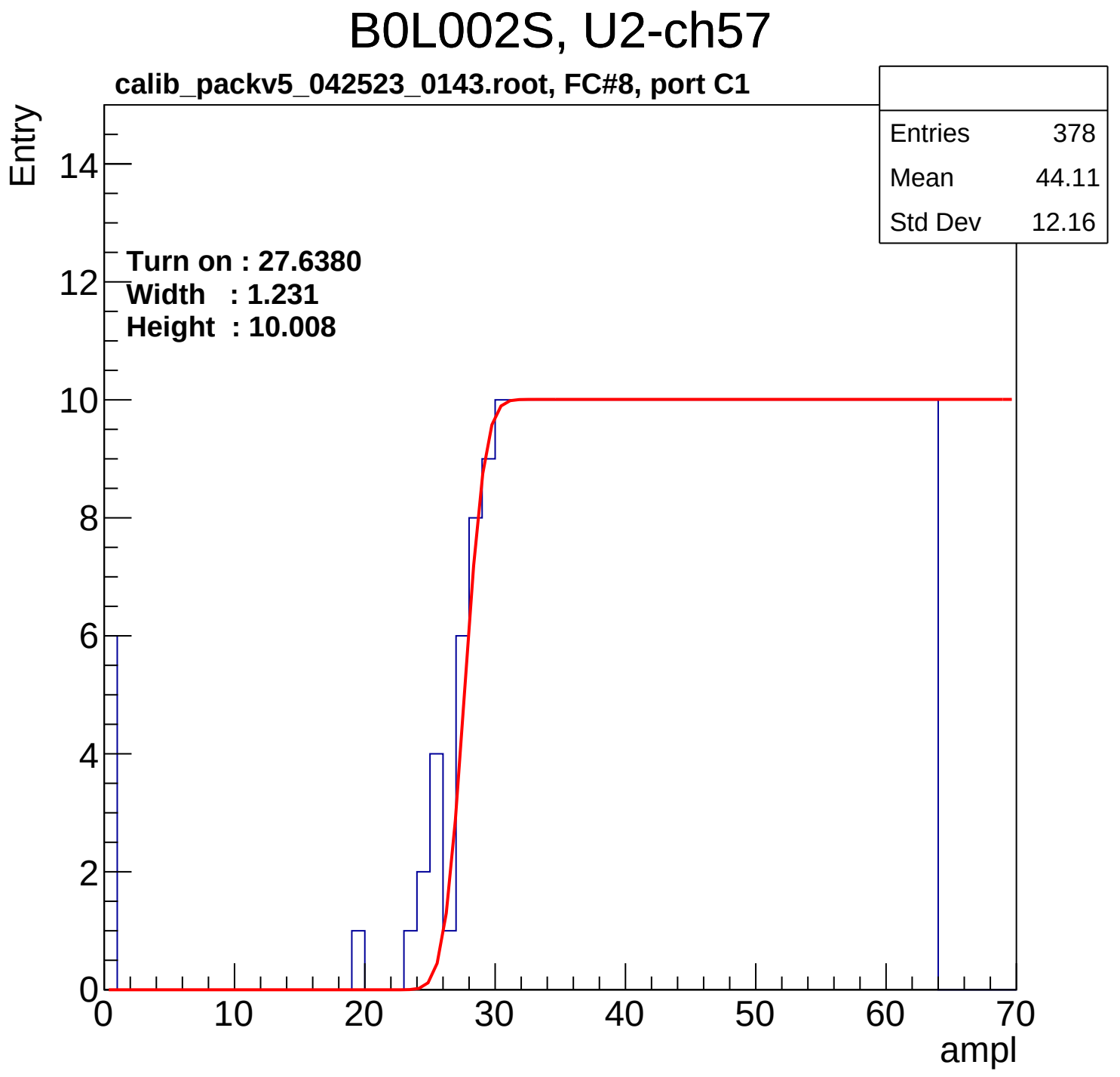
B0L002S, U2-ch57
calib_packv5_042523_0143.root, FC#8, port C1
Entries 378
Mean 44.11
Std Dev 12.16
Turn on : 27.6380
Width : 1.231
Height : 10.008
Entry
ampl
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4
6
8
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20
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40
50
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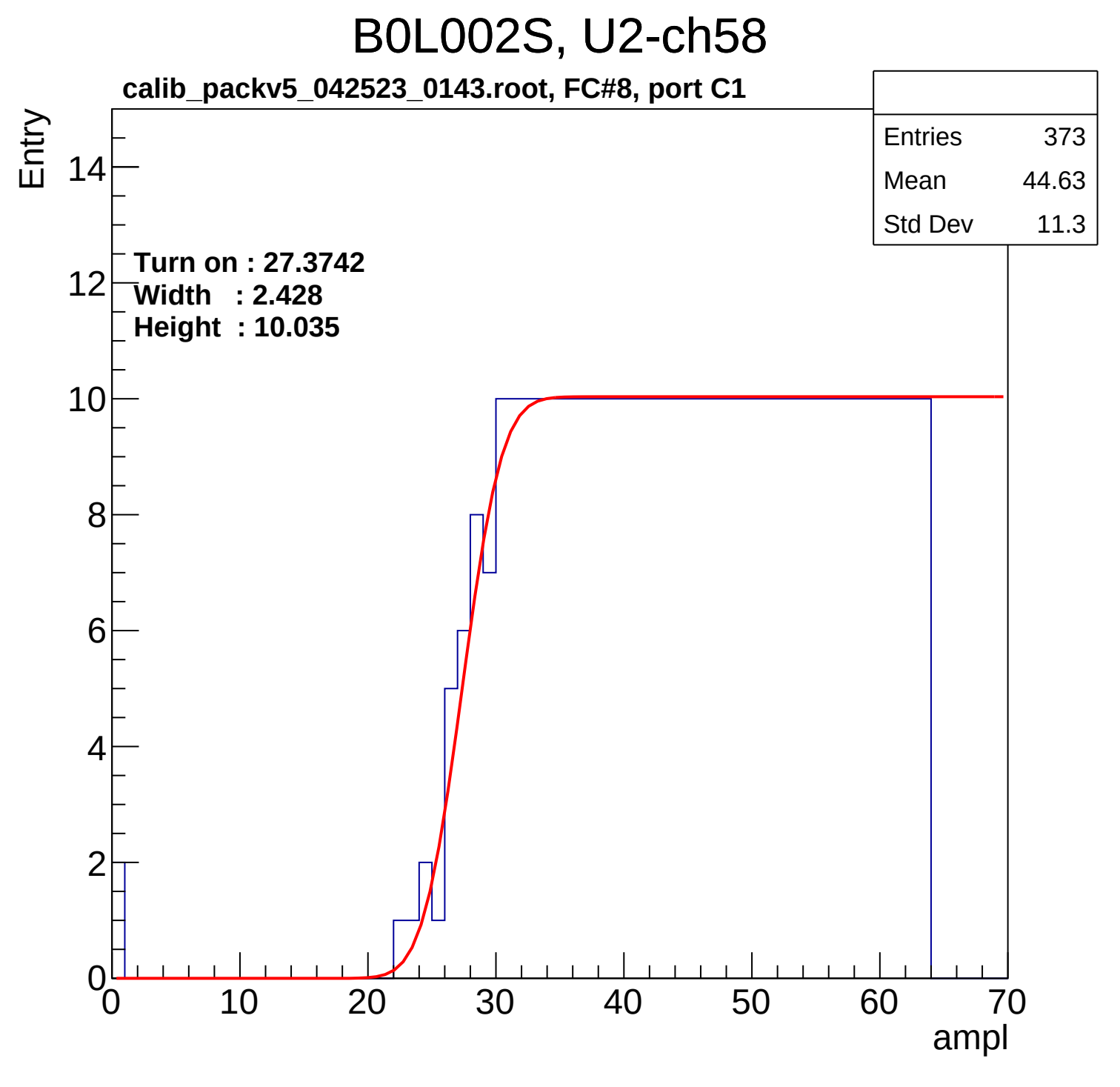
B0L002S, U2-ch58
calib_packv5_042523_0143.root, FC#8, port C1
Entries 373
Mean 44.63
Std Dev 11.3
Turn on : 27.3742
Width : 2.428
Height : 10.035
Entry
ampl
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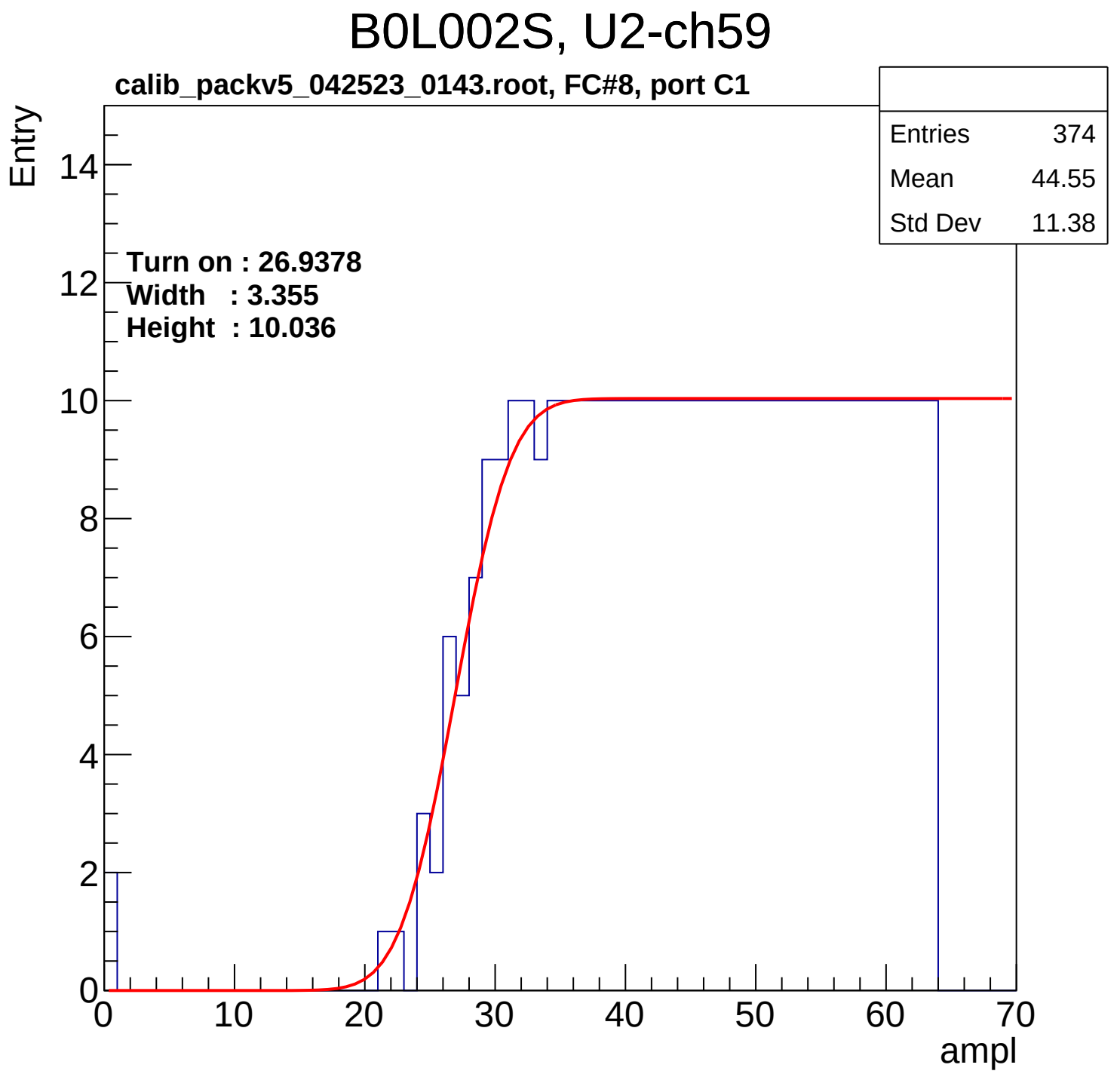
B0L002S, U2-ch59
calib_packv5_042523_0143.root, FC#8, port C1
Entries 374
Mean 44.55
Std Dev 11.38
Turn on : 26.9378
Width : 3.355
Height : 10.036
Entry
ampl
0
2
4
6
8
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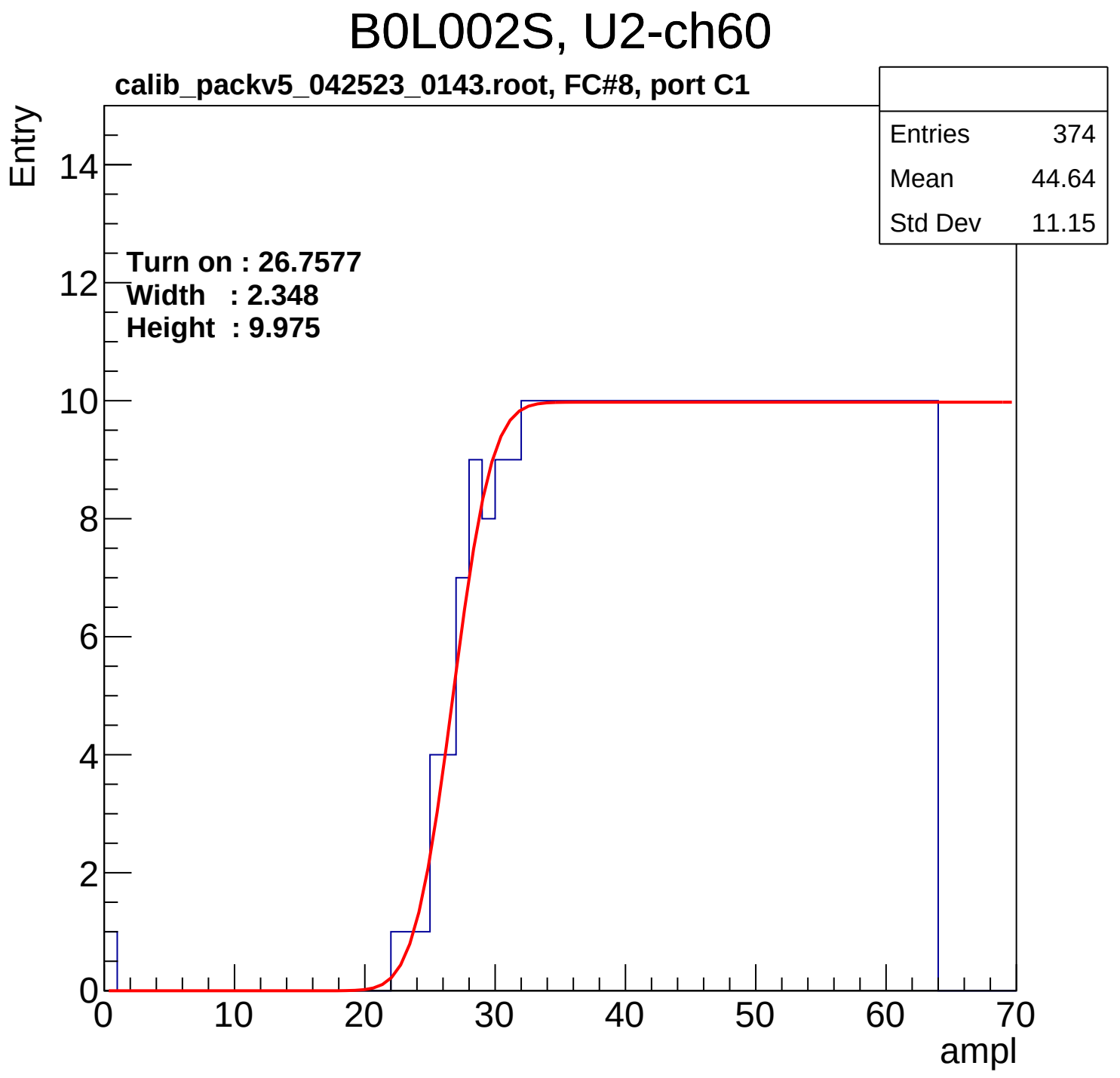
B0L002S, U2-ch60
calib_packv5_042523_0143.root, FC#8, port C1
Entries 374
Mean 44.64
Std Dev 11.15
Turn on : 26.7577
Width : 2.348
Height : 9.975
Entry
ampl
0
2
4
6
8
10
12
14
0
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40
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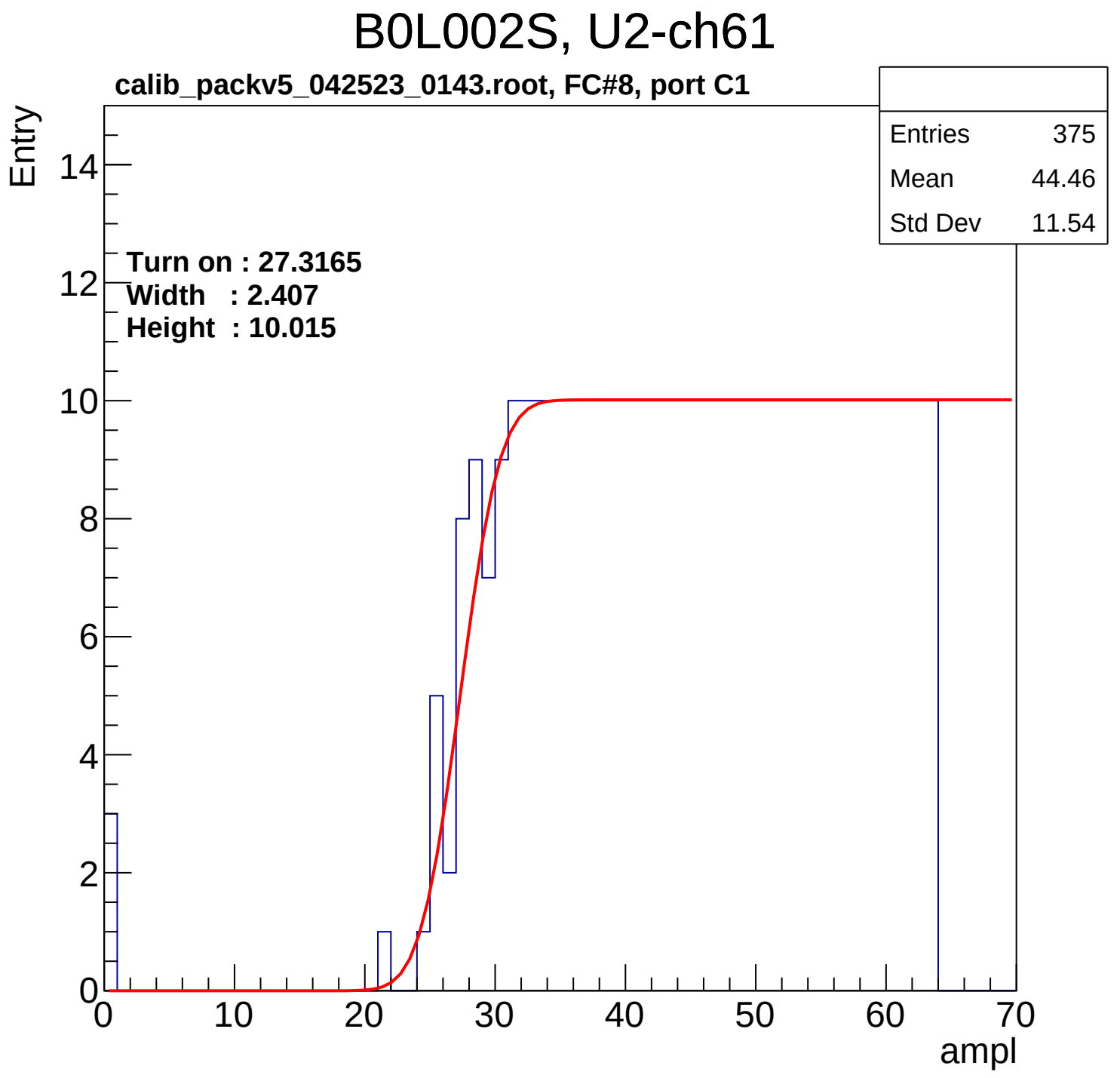
B0L002S, U2-ch61
calib_packv5_042523_0143.root, FC#8, port C1
Entries 375
Mean 44.46
Std Dev 11.54
Turn on : 27.3165
Width : 2.407
Height : 10.015
Entry
ampl
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2
4
6
8
10
12
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0
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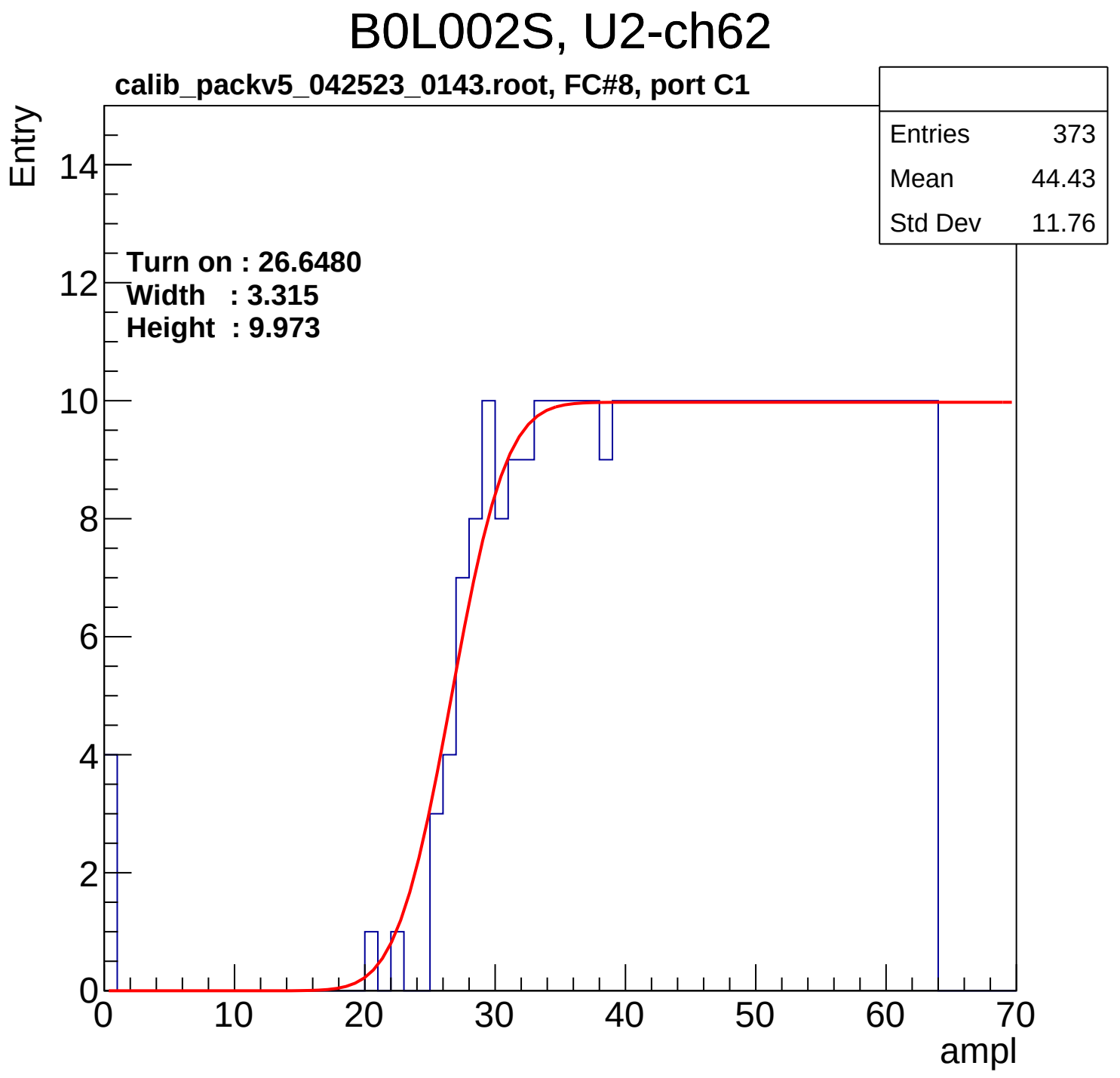
B0L002S, U2-ch62
calib_packv5_042523_0143.root, FC#8, port C1
Entries 373
Mean 44.43
Std Dev 11.76
Turn on : 26.6480
Width : 3.315
Height : 9.973
Entry
ampl
0
2
4
6
8
10
12
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0
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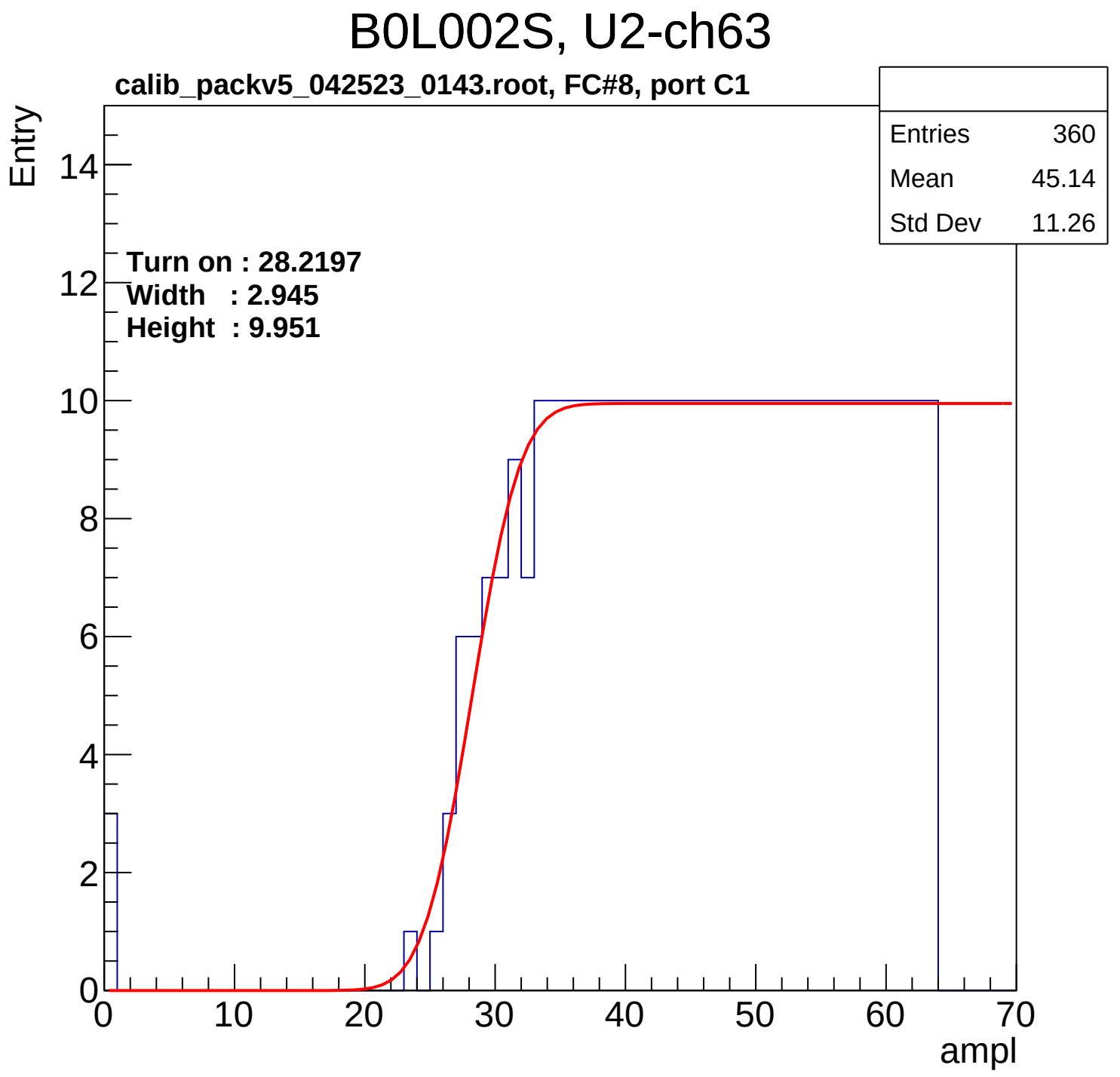
B0L002S, U2-ch63
calib_packv5_042523_0143.root, FC#8, port C1
Entries 360
Mean 45.14
Std Dev 11.26
Turn on : 28.2197
Width : 2.945
Height : 9.951
Entry
ampl
0
2
4
6
8
10
12
14
0
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40
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60
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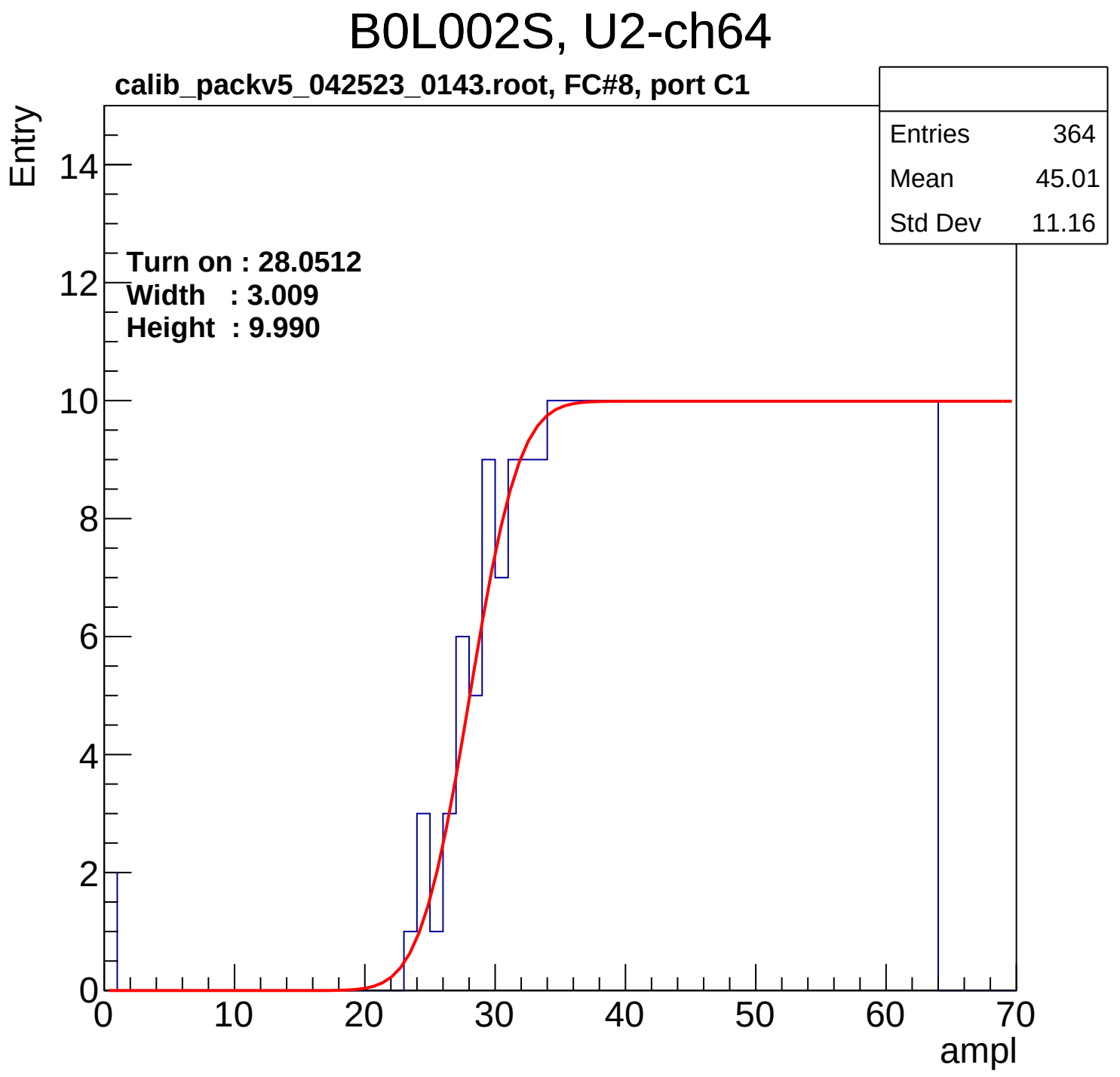
B0L002S, U2-ch64
calib_packv5_042523_0143.root, FC#8, port C1
Entries 364
Mean 45.01
Std Dev 11.16
Turn on : 28.0512
Width : 3.009
Height : 9.990
Entry
ampl
0
2
4
6
8
10
12
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0
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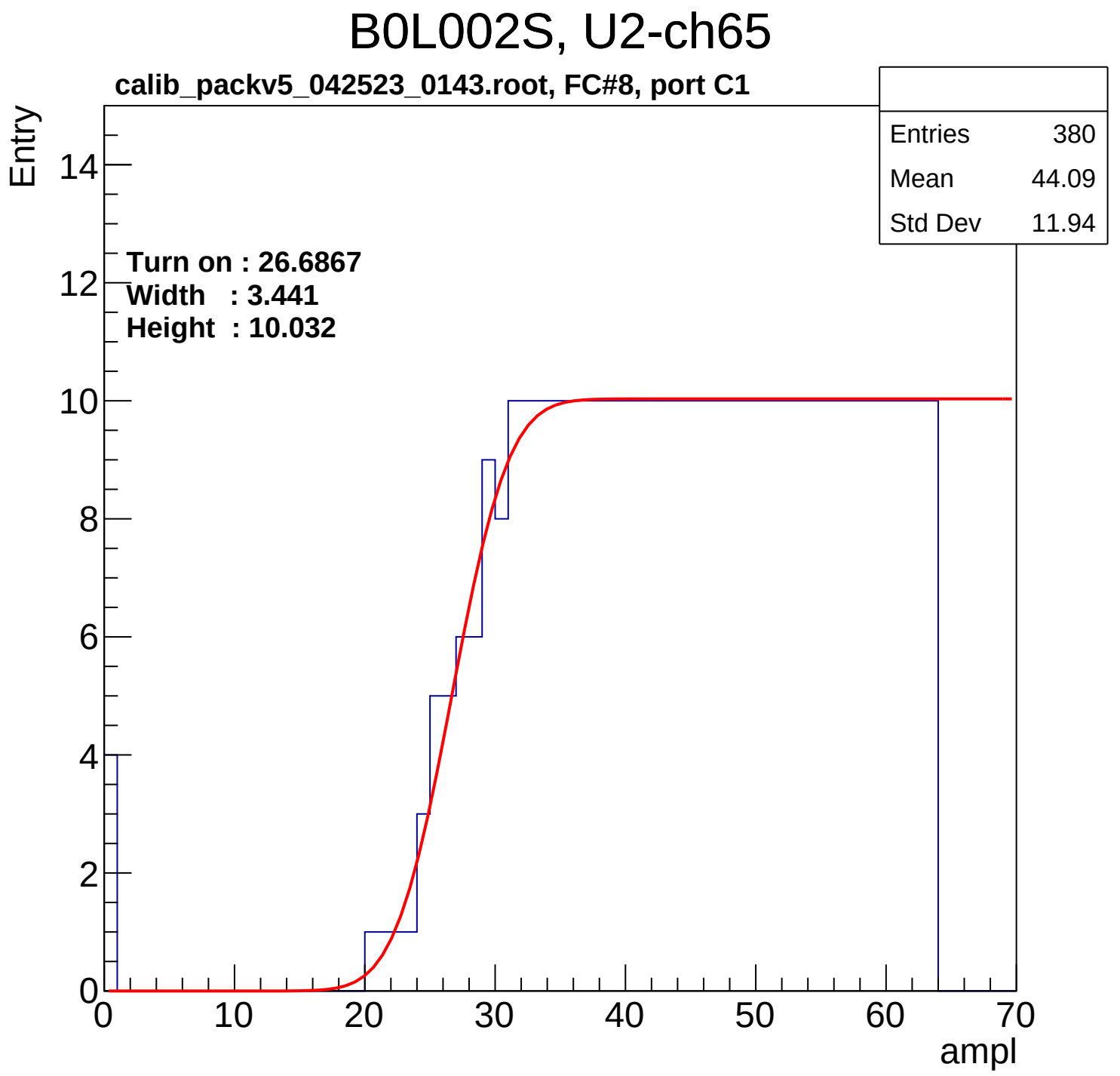
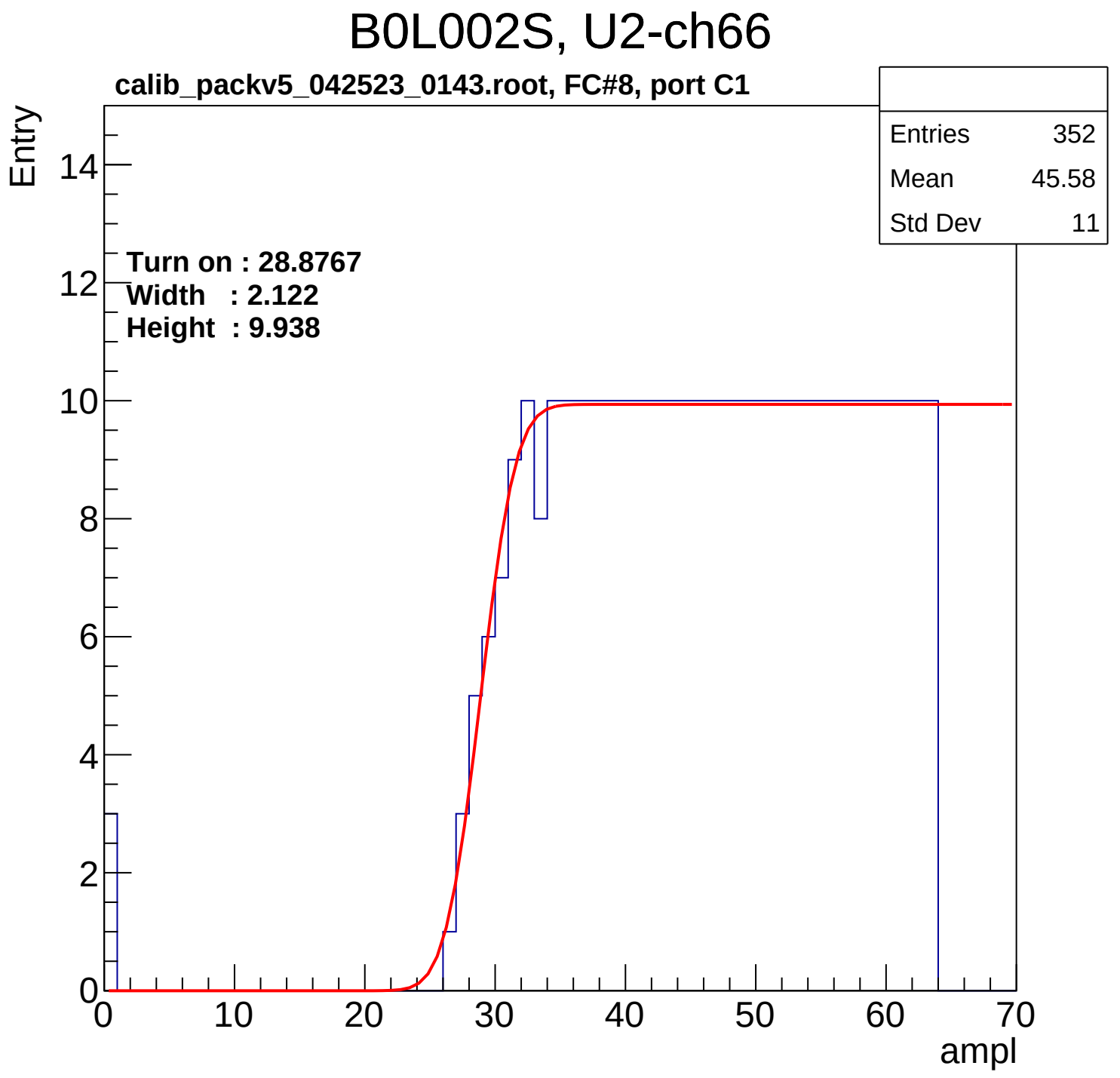

B0L002S, U2-ch65
calib_packv5_042523_0143.root, FC#8, port C1
Entries 380
Mean 44.09
Std Dev 11.94
Turn on : 26.6867
Width : 3.441
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L002S, U2-ch66
calib_packv5_042523_0143.root, FC#8, port C1
Entries 352
Mean 45.58
Std Dev 11
Turn on : 28.8767
Width : 2.122
Height : 9.938
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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60
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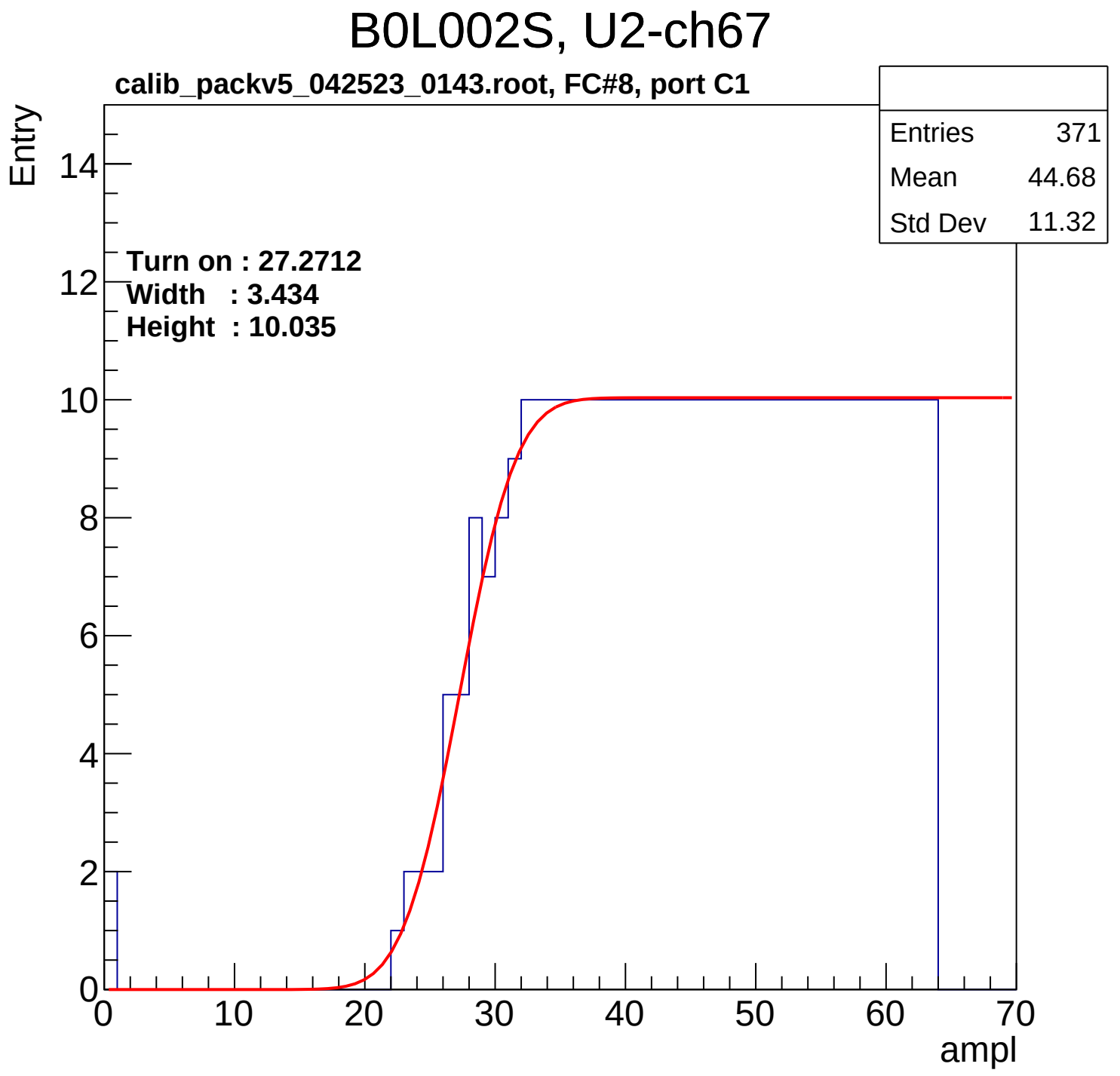
B0L002S, U2-ch67
calib_packv5_042523_0143.root, FC#8, port C1
Entries 371
Mean 44.68
Std Dev 11.32
Turn on : 27.2712
Width : 3.434
Height : 10.035
Entry
ampl
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2
4
6
8
10
12
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0
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60
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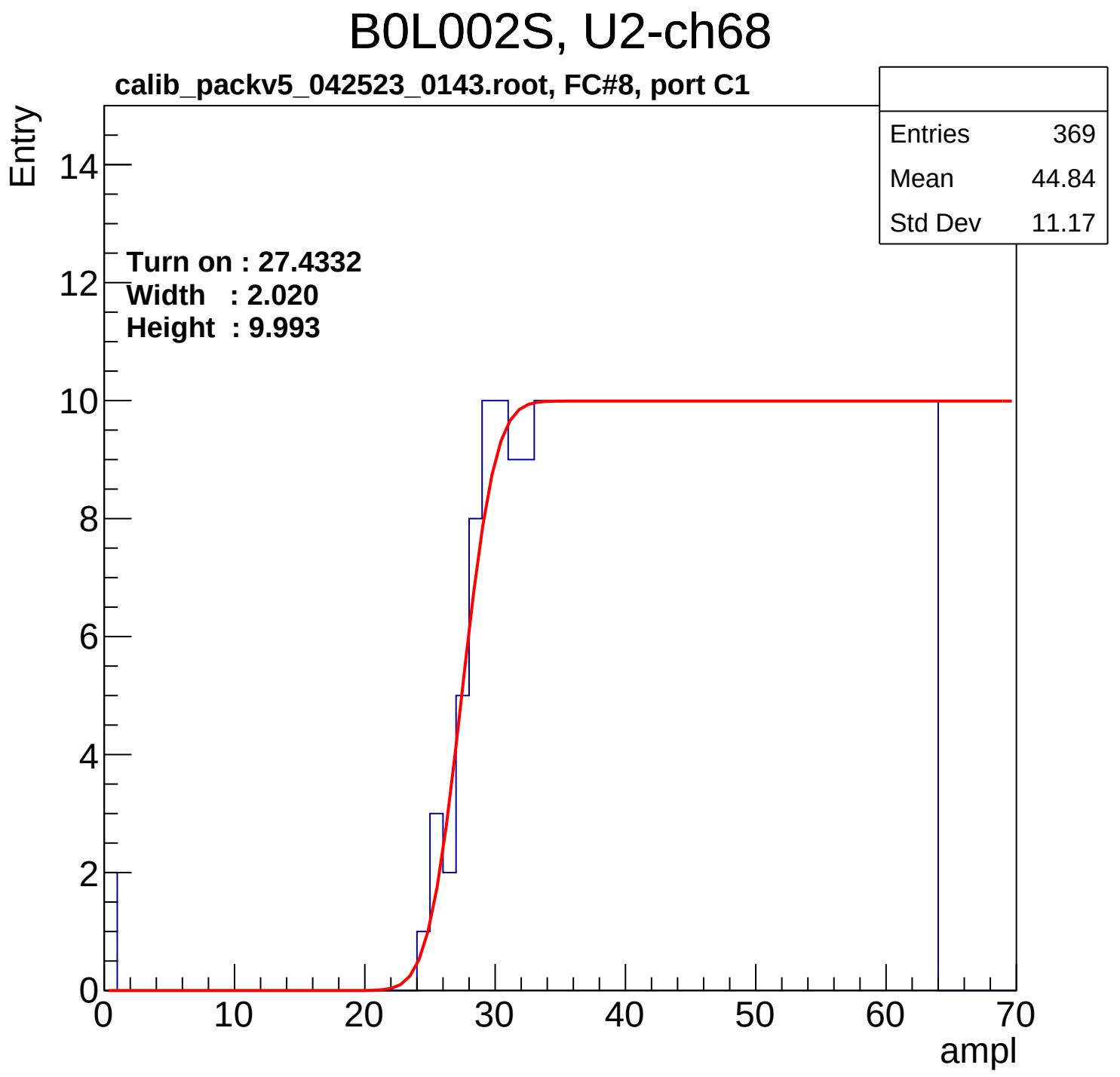
B0L002S, U2-ch68
calib_packv5_042523_0143.root, FC#8, port C1
Entries 369
Mean 44.84
Std Dev 11.17
Turn on : 27.4332
Width : 2.020
Height : 9.993
Entry
ampl
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4
6
8
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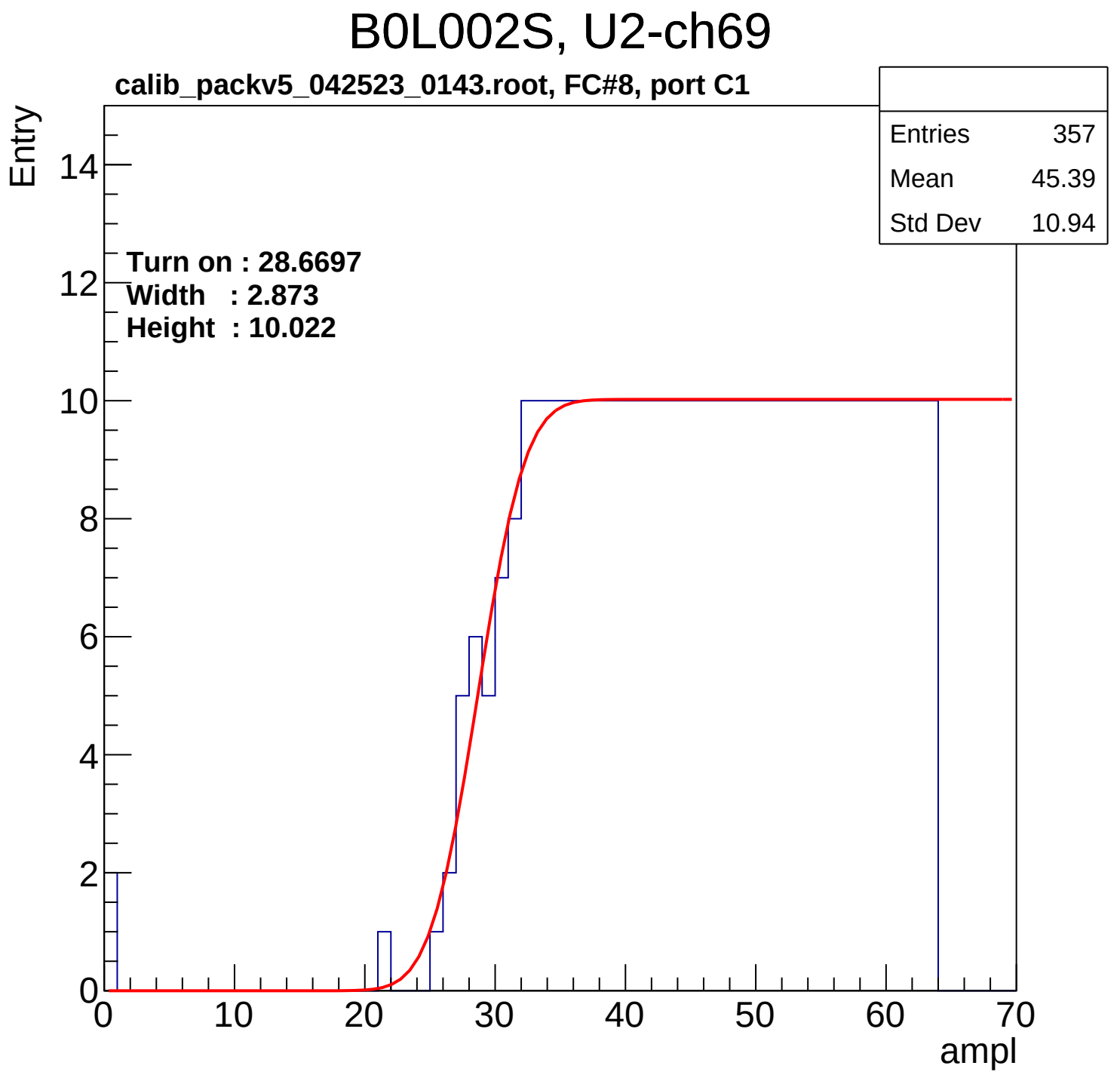
B0L002S, U2-ch69
calib_packv5_042523_0143.root, FC#8, port C1
Entries 357
Mean 45.39
Std Dev 10.94
Turn on : 28.6697
Width : 2.873
Height : 10.022
Entry
ampl
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2
4
6
8
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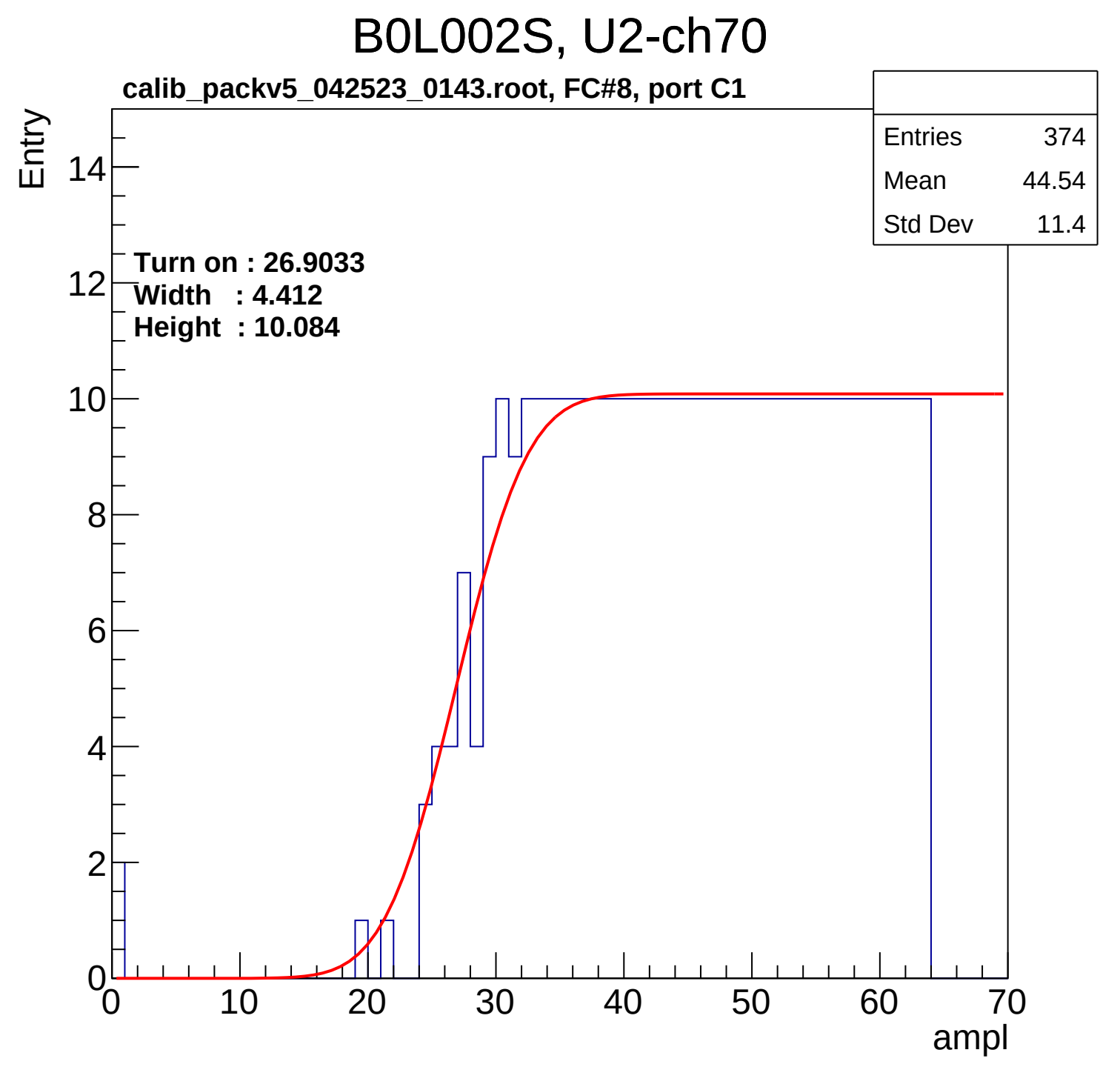
B0L002S, U2-ch70
calib_packv5_042523_0143.root, FC#8, port C1
Entries 374
Mean 44.54
Std Dev 11.4
Turn on : 26.9033
Width : 4.412
Height : 10.084
Entry
ampl
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4
6
8
10
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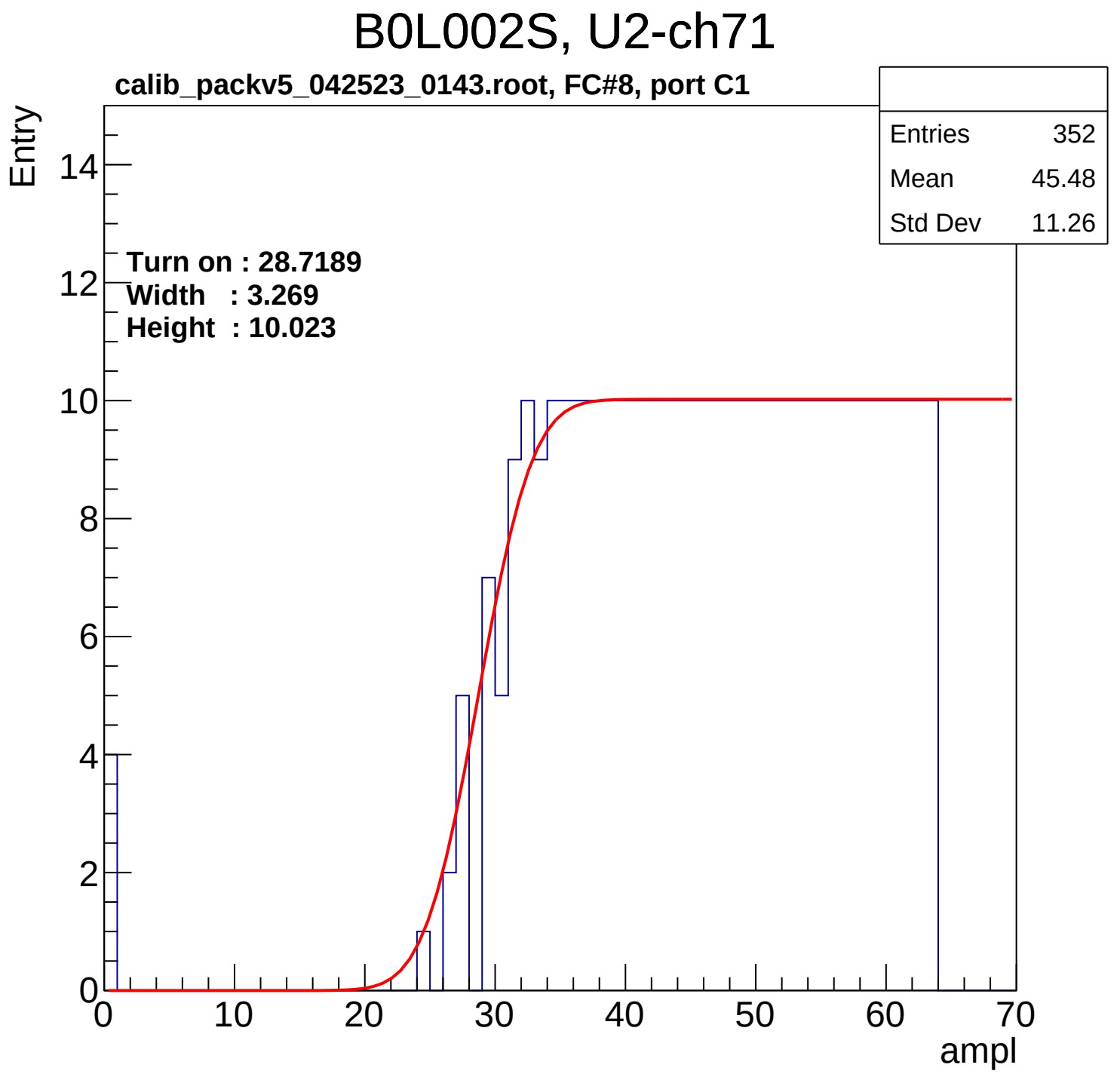
B0L002S, U2-ch71
calib_packv5_042523_0143.root, FC#8, port C1
Entries 352
Mean 45.48
Std Dev 11.26
Turn on : 28.7189
Width : 3.269
Height : 10.023
Entry
ampl
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6
8
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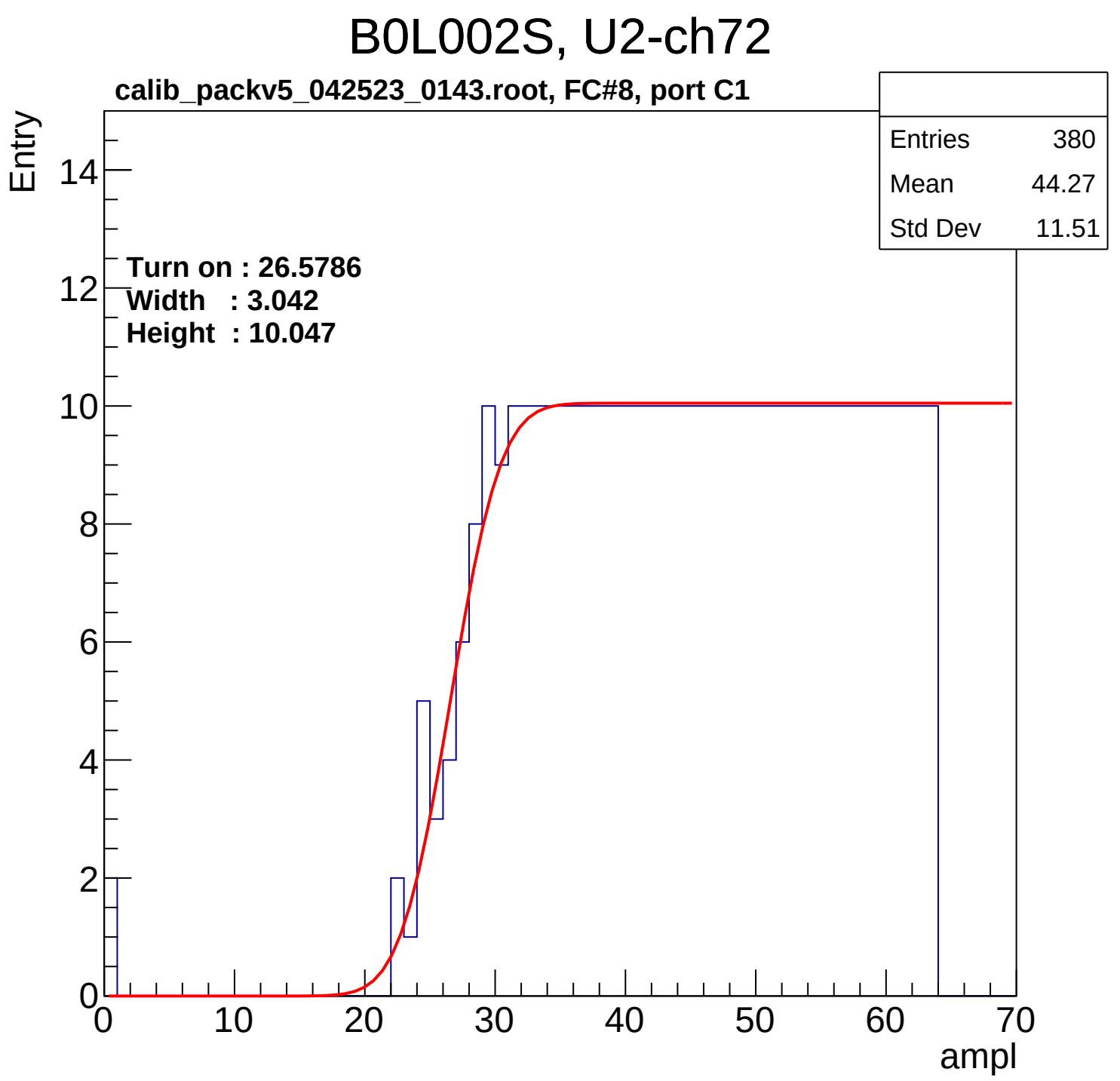
B0L002S, U2-ch72
calib_packv5_042523_0143.root, FC#8, port C1
Entries 380
Mean 44.27
Std Dev 11.51
Turn on : 26.5786
Width : 3.042
Height : 10.047
Entry
ampl
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6
8
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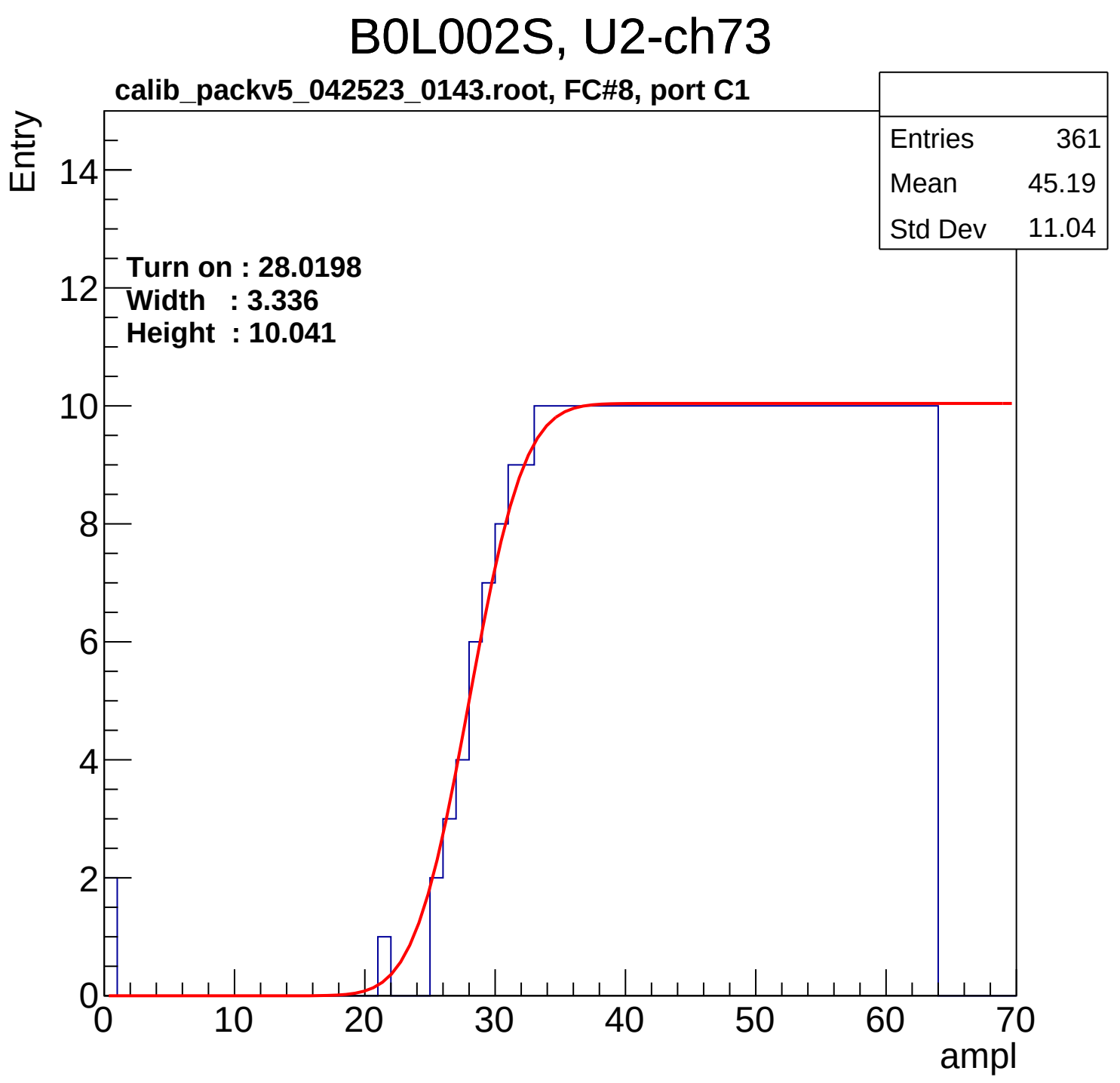
B0L002S, U2-ch73
calib_packv5_042523_0143.root, FC#8, port C1
Entries 361
Mean 45.19
Std Dev 11.04
Turn on : 28.0198
Width : 3.336
Height : 10.041
Entry
ampl
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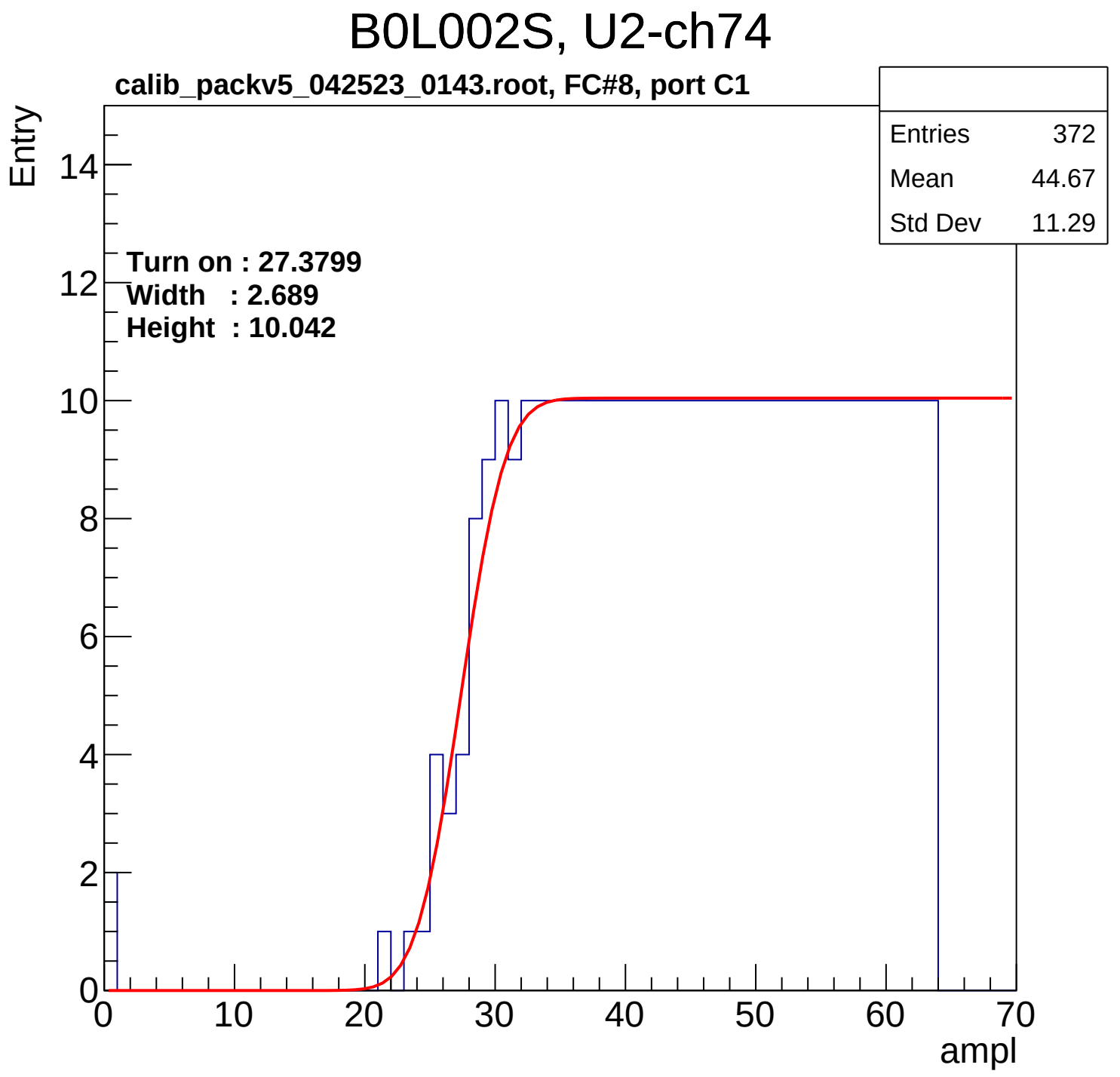
B0L002S, U2-ch74
calib_packv5_042523_0143.root, FC#8, port C1
Entries 372
Mean 44.67
Std Dev 11.29
Turn on : 27.3799
Width : 2.689
Height : 10.042
Entry
ampl
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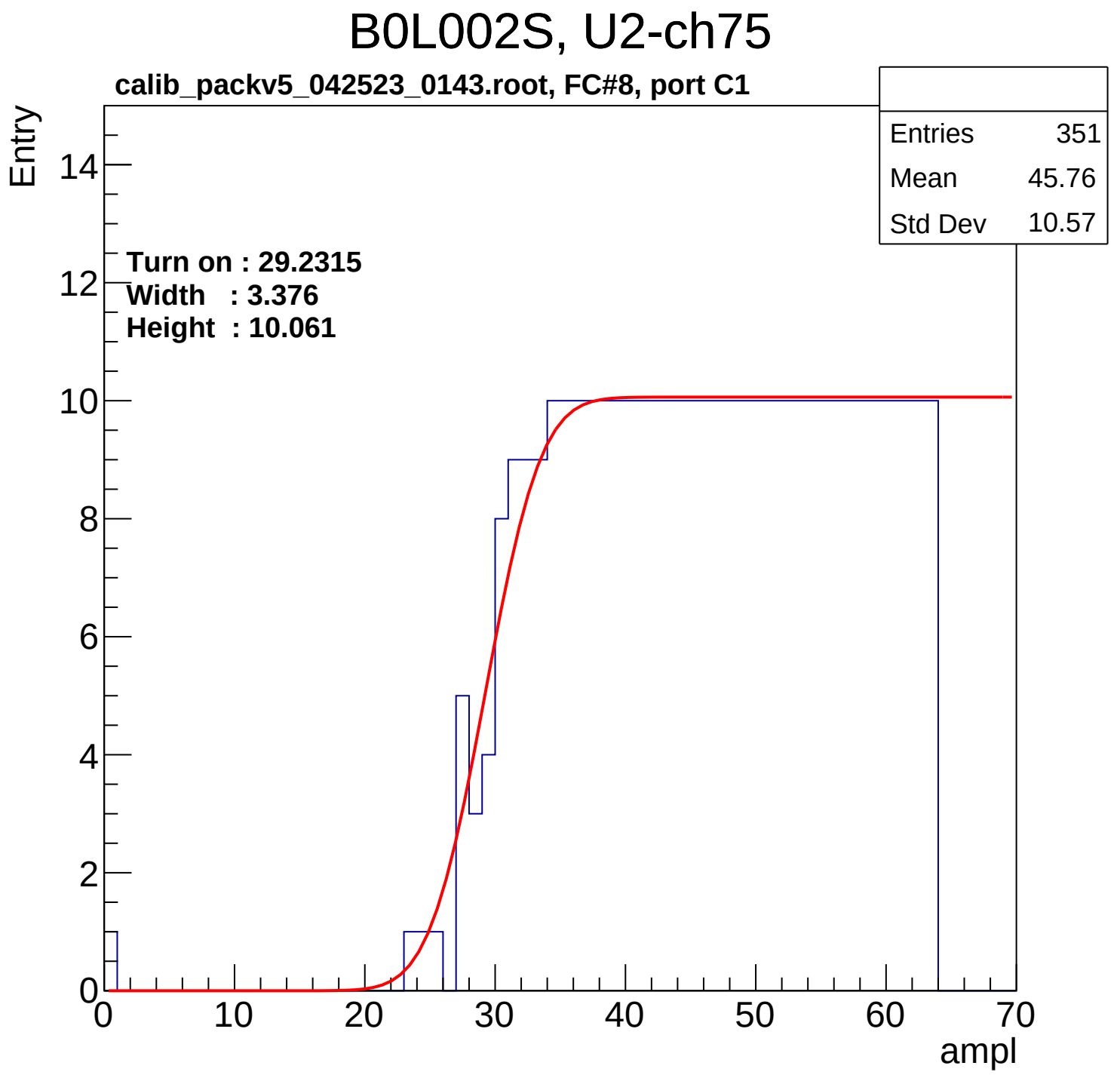
B0L002S, U2-ch75
calib_packv5_042523_0143.root, FC#8, port C1
Entries 351
Mean 45.76
Std Dev 10.57
Turn on : 29.2315
Width : 3.376
Height : 10.061
Entry
ampl
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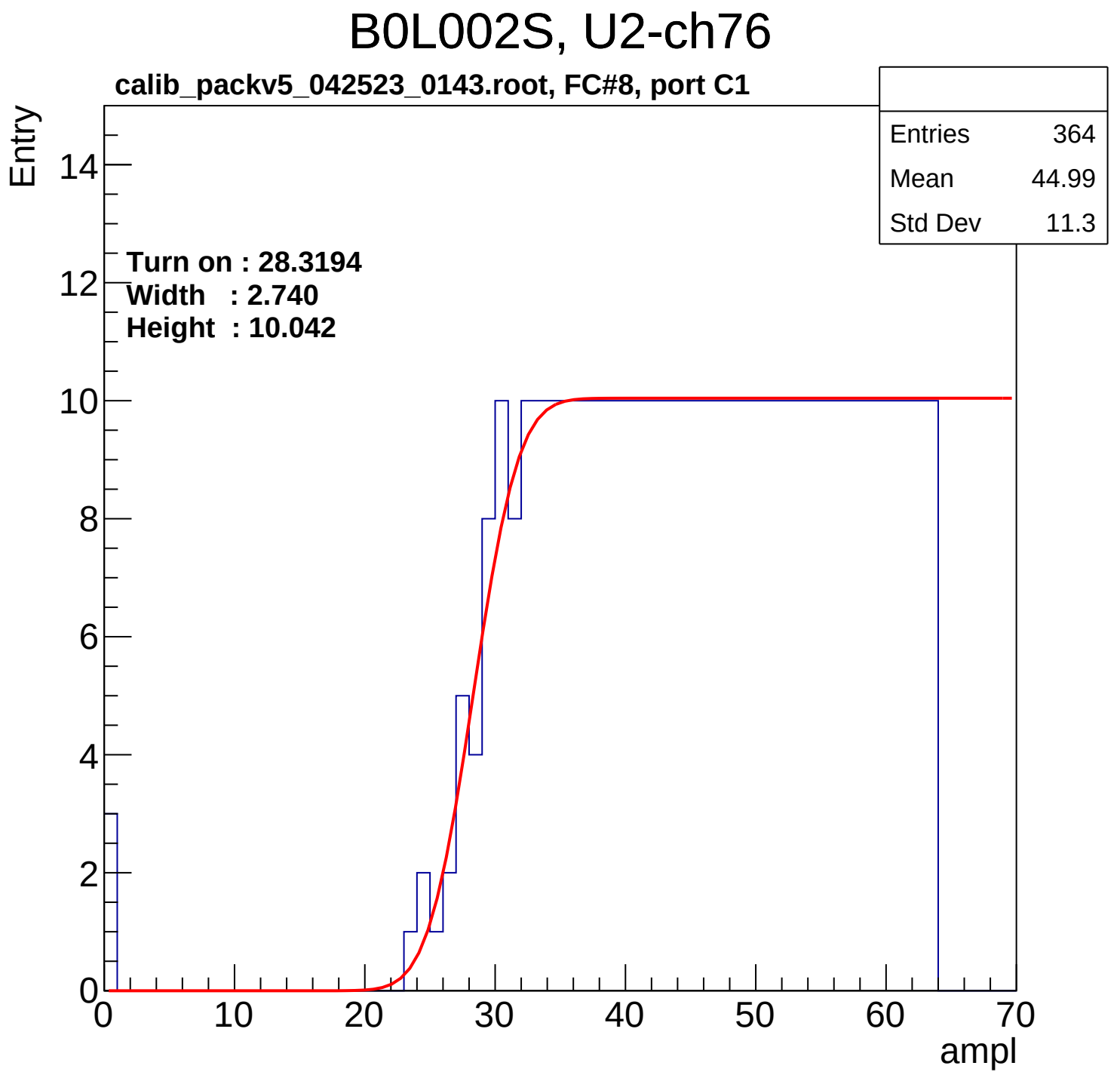
B0L002S, U2-ch76
calib_packv5_042523_0143.root, FC#8, port C1
Entries 364
Mean 44.99
Std Dev 11.3
Turn on : 28.3194
Width : 2.740
Height : 10.042
Entry
ampl
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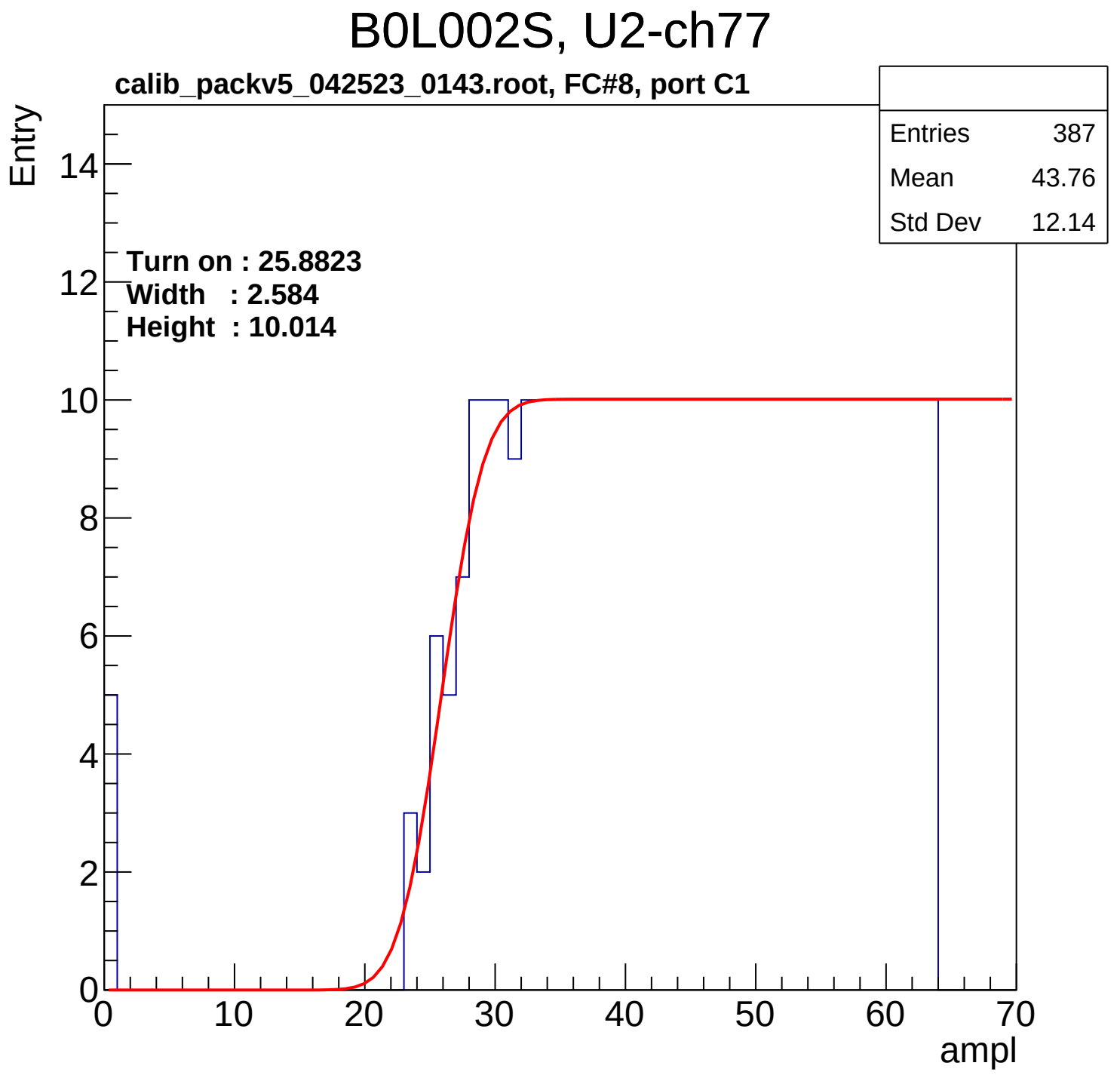
B0L002S, U2-ch77
calib_packv5_042523_0143.root, FC#8, port C1
Entries 387
Mean 43.76
Std Dev 12.14
Turn on : 25.8823
Width : 2.584
Height : 10.014
Entry
ampl
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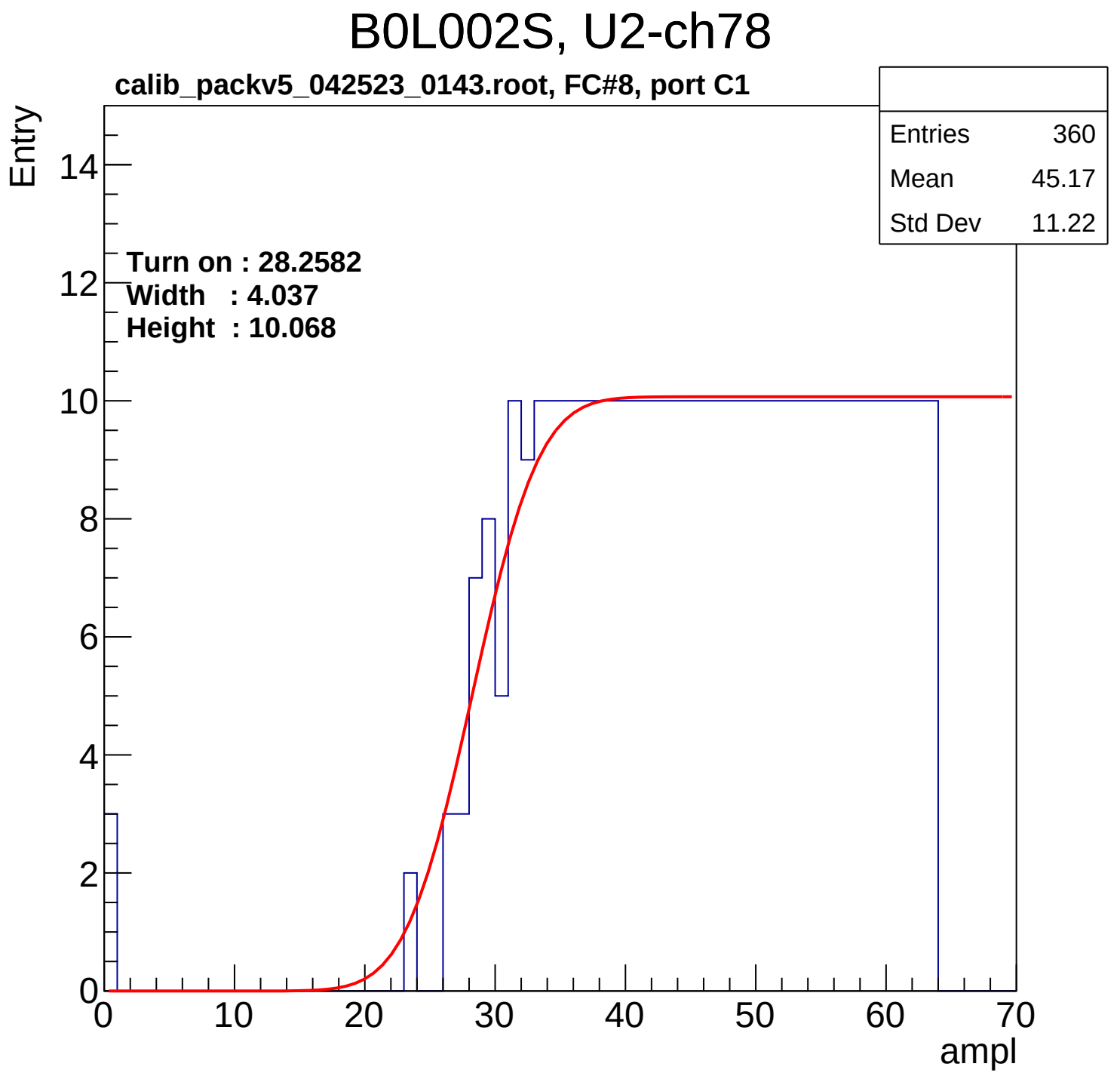
B0L002S, U2-ch78
calib_packv5_042523_0143.root, FC#8, port C1
Entries 360
Mean 45.17
Std Dev 11.22
Turn on : 28.2582
Width : 4.037
Height : 10.068
Entry
ampl
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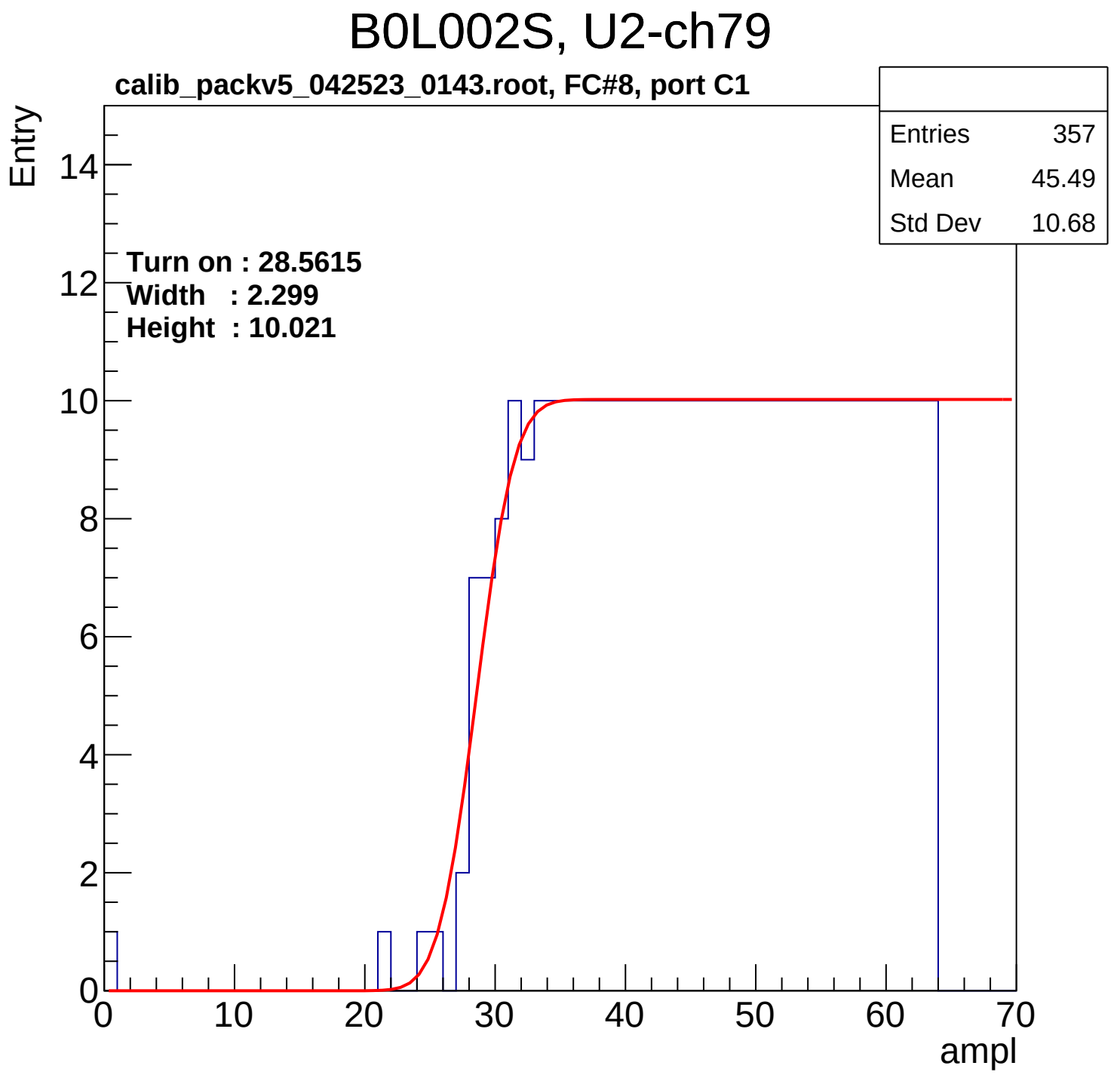
B0L002S, U2-ch79
calib_packv5_042523_0143.root, FC#8, port C1
Entries 357
Mean 45.49
Std Dev 10.68
Turn on : 28.5615
Width : 2.299
Height : 10.021
Entry
ampl
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8
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0
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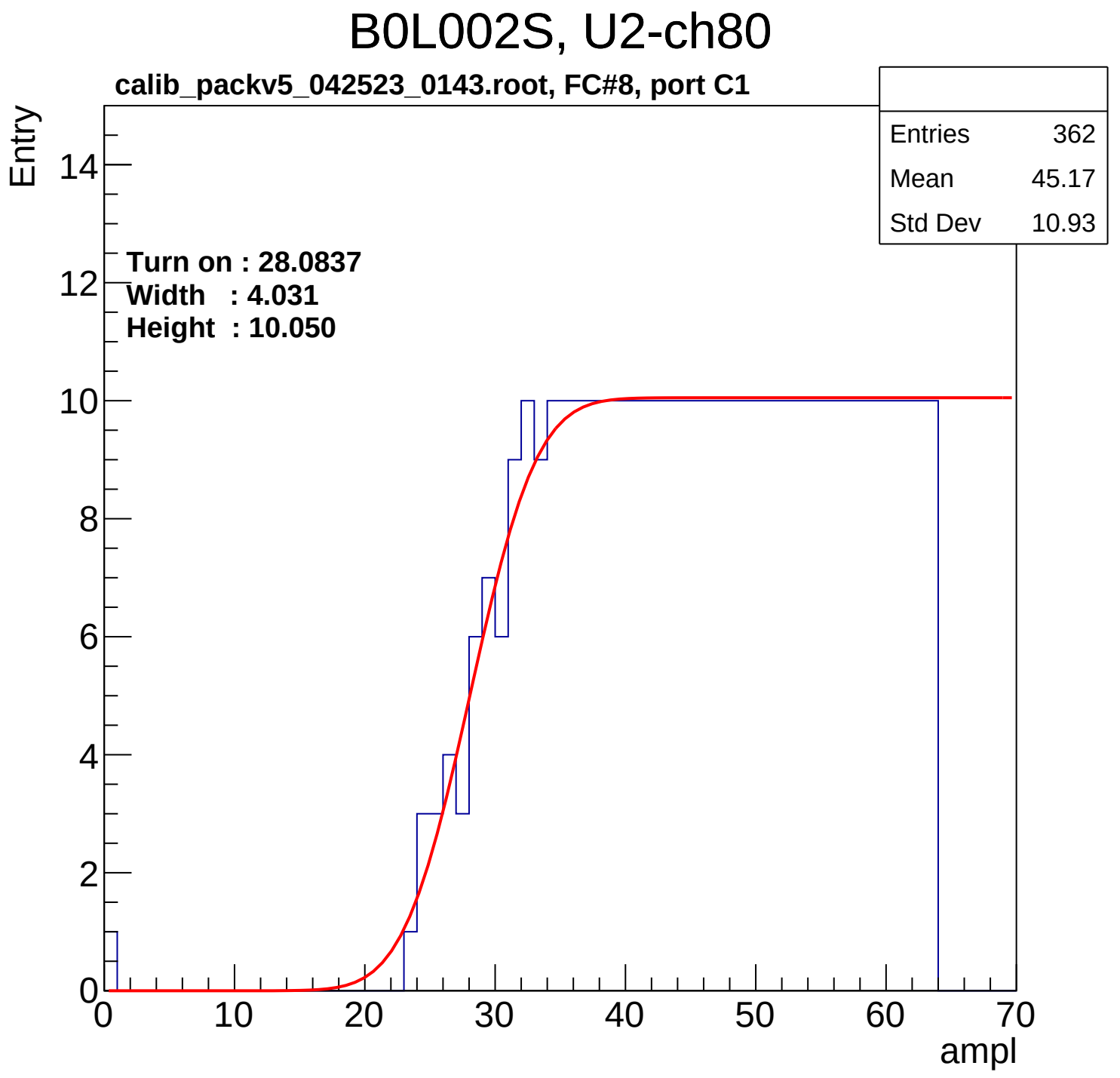
B0L002S, U2-ch80
calib_packv5_042523_0143.root, FC#8, port C1
Entries 362
Mean 45.17
Std Dev 10.93
Turn on : 28.0837
Width : 4.031
Height : 10.050
Entry
ampl
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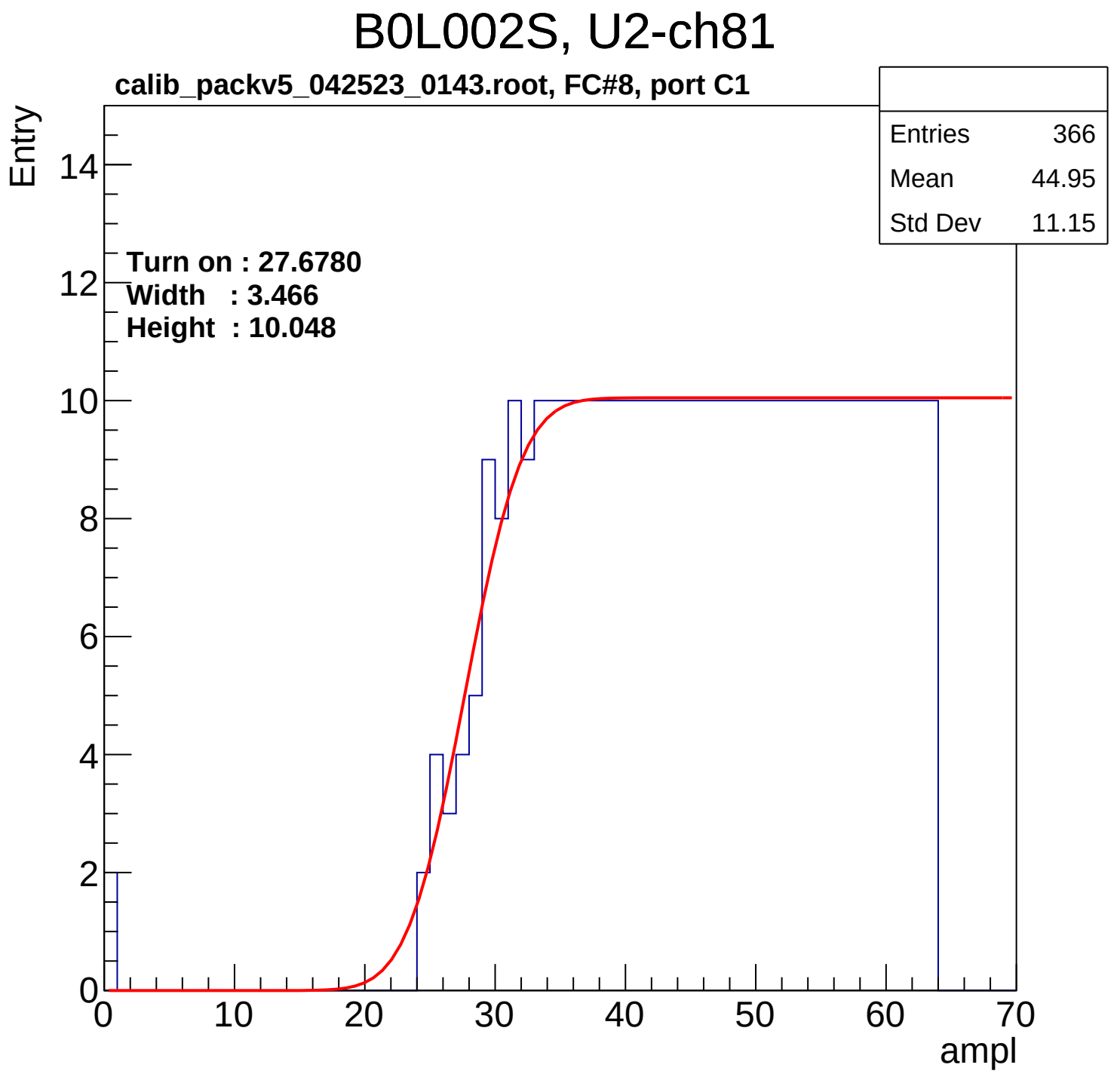
B0L002S, U2-ch81
calib_packv5_042523_0143.root, FC#8, port C1
Entries 366
Mean 44.95
Std Dev 11.15
Turn on : 27.6780
Width : 3.466
Height : 10.048
Entry
ampl
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4
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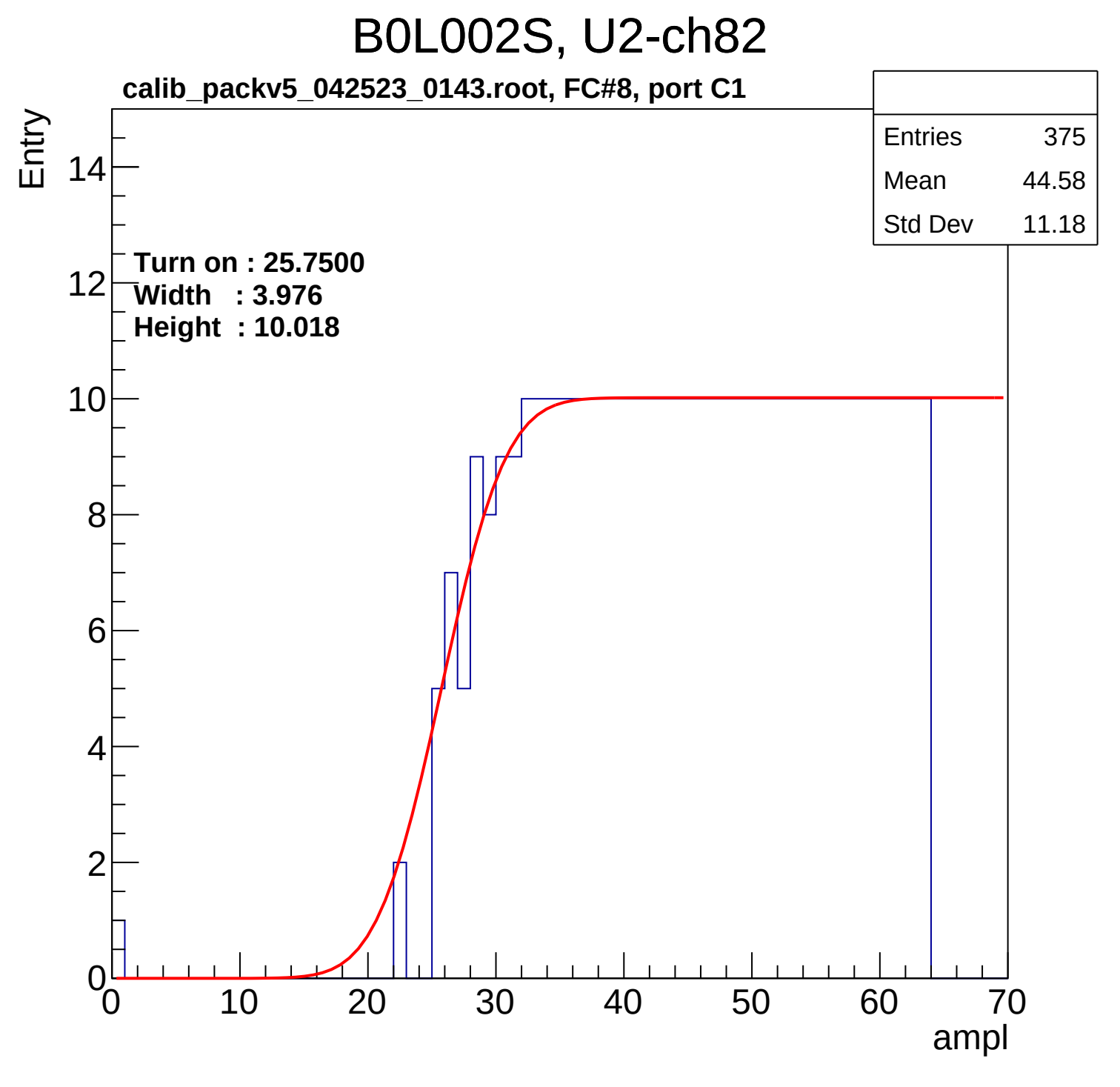
B0L002S, U2-ch82
calib_packv5_042523_0143.root, FC#8, port C1
Entries 375
Mean 44.58
Std Dev 11.18
Turn on : 25.7500
Width : 3.976
Height : 10.018
Entry
ampl
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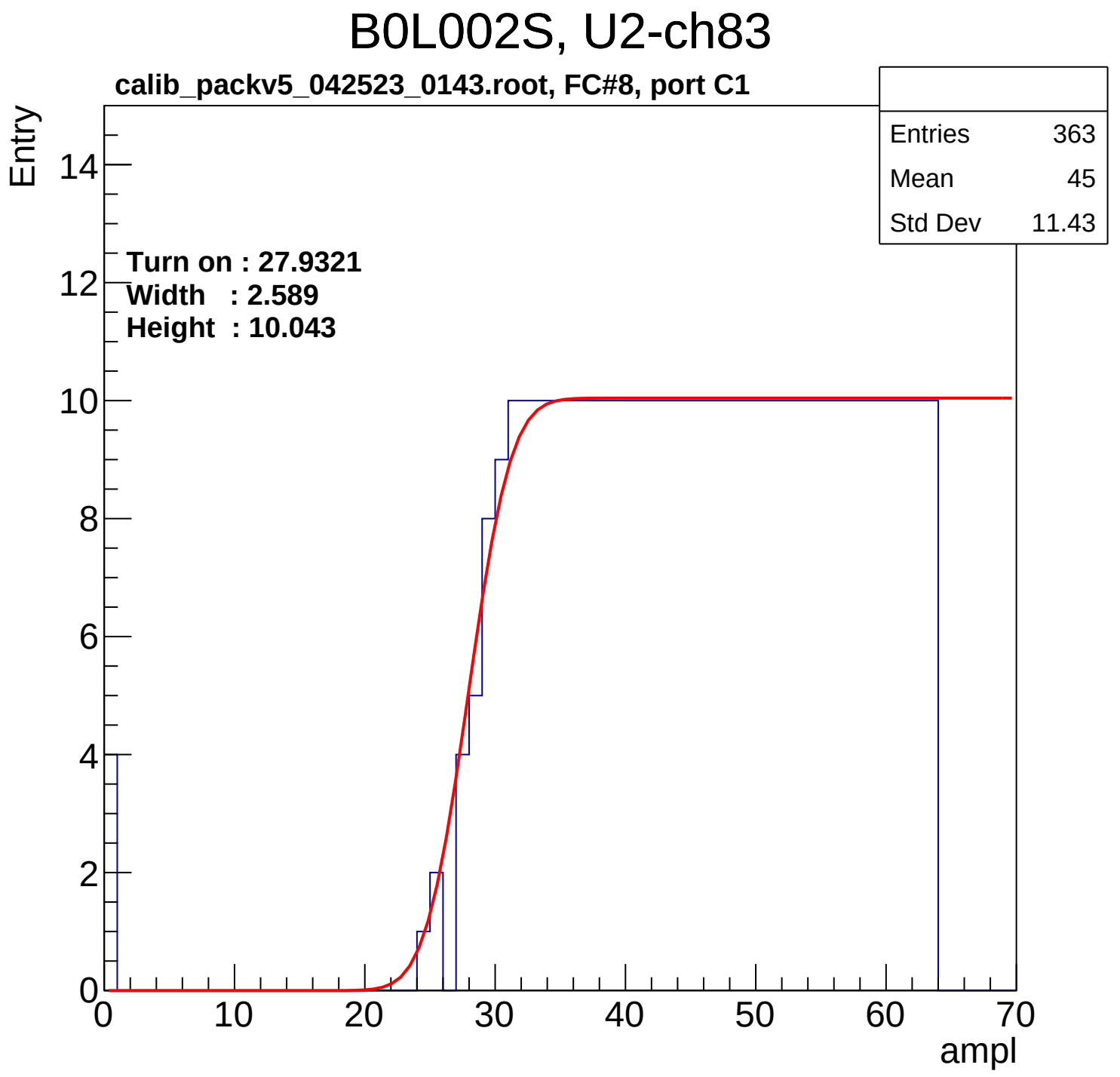
B0L002S, U2-ch83
calib_packv5_042523_0143.root, FC#8, port C1
Entries 363
Mean 45
Std Dev 11.43
Turn on : 27.9321
Width : 2.589
Height : 10.043
Entry
ampl
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6
8
10
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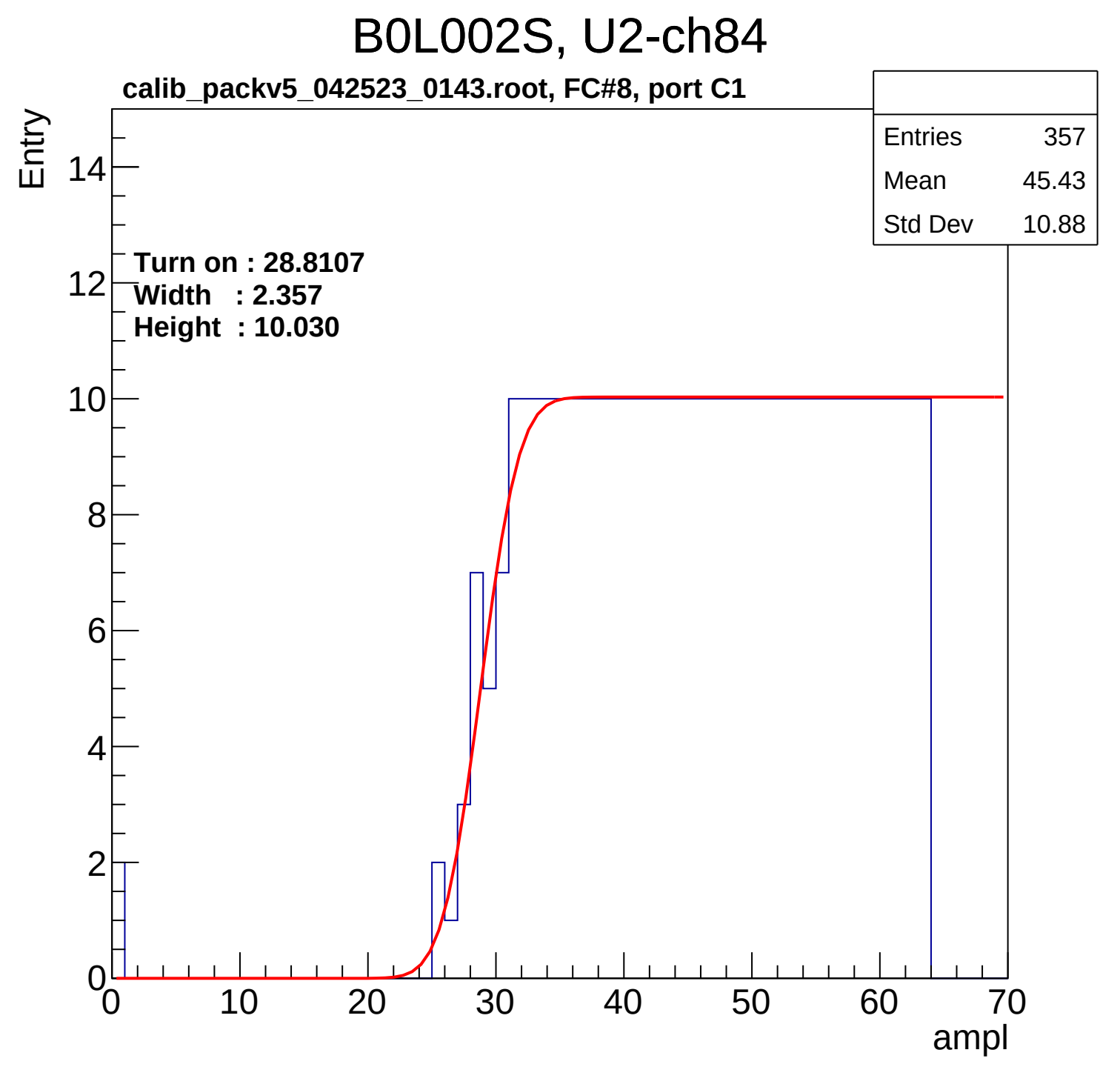
B0L002S, U2-ch84
calib_packv5_042523_0143.root, FC#8, port C1
Entries 357
Mean 45.43
Std Dev 10.88
Turn on : 28.8107
Width : 2.357
Height : 10.030
Entry
ampl
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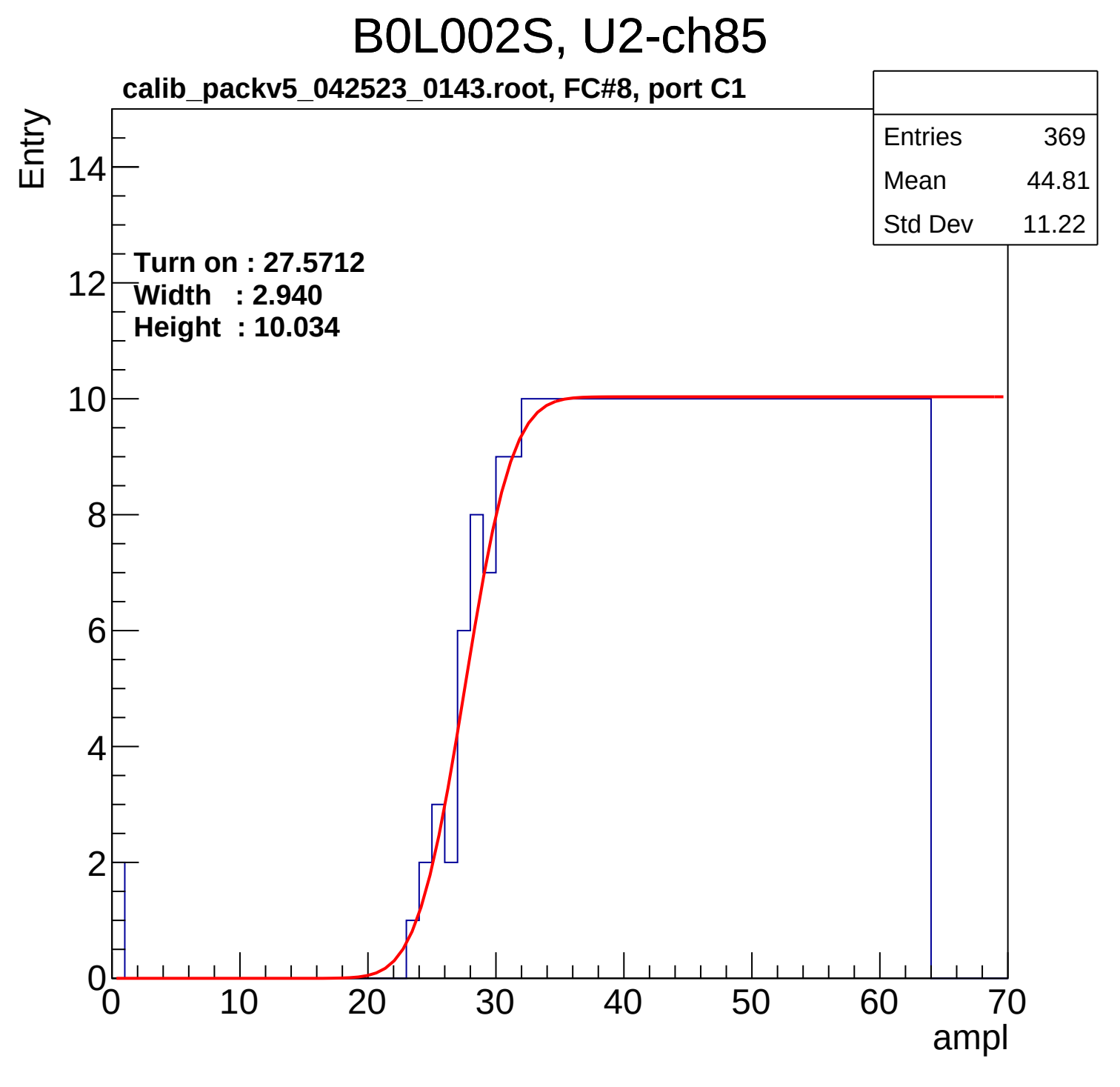
B0L002S, U2-ch85
calib_packv5_042523_0143.root, FC#8, port C1
Entries 369
Mean 44.81
Std Dev 11.22
Turn on : 27.5712
Width : 2.940
Height : 10.034
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ampl
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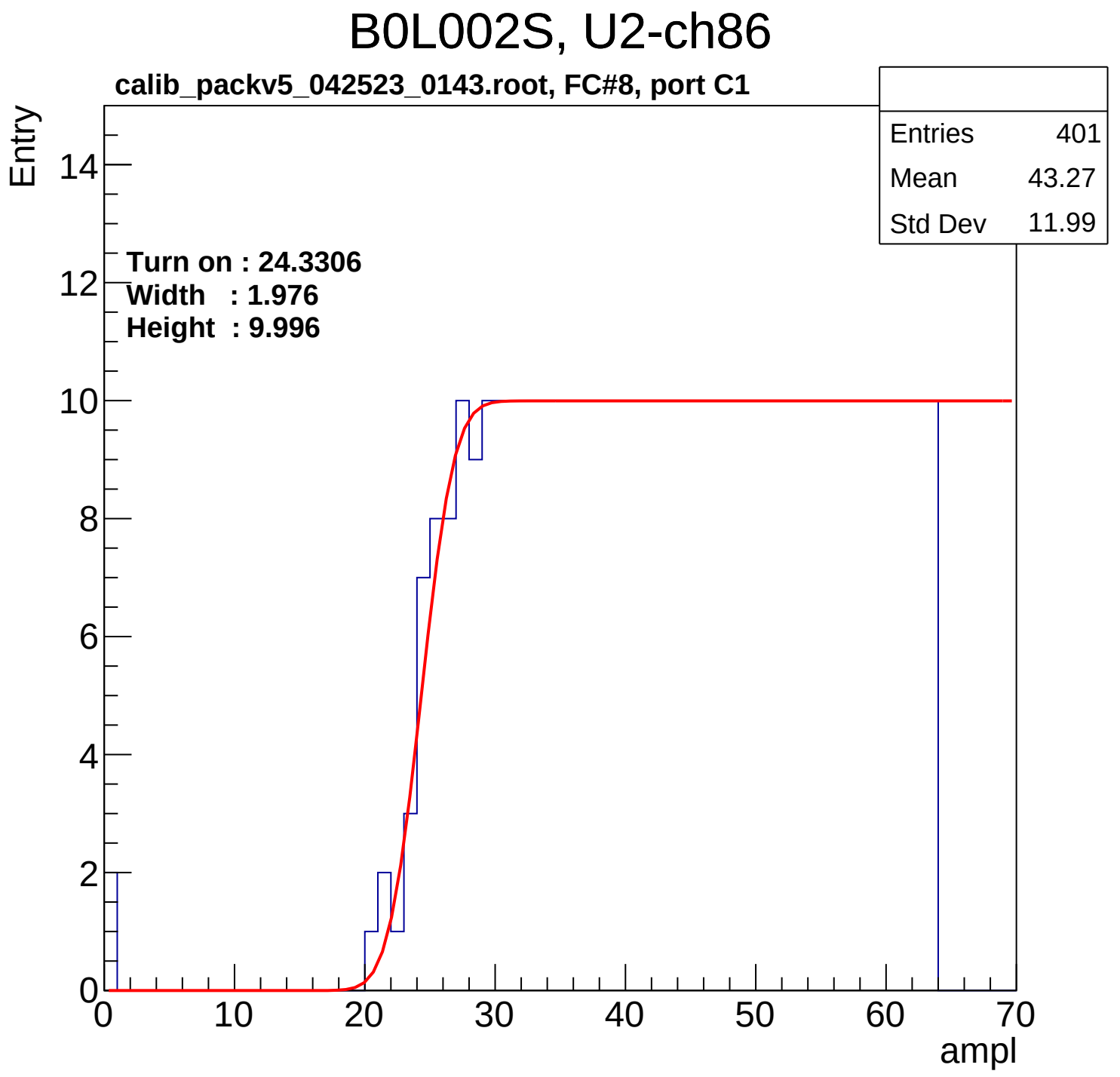
B0L002S, U2-ch86
calib_packv5_042523_0143.root, FC#8, port C1
Entries 401
Mean 43.27
Std Dev 11.99
Turn on : 24.3306
Width : 1.976
Height : 9.996
Entry
ampl
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2
4
6
8
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12
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10
20
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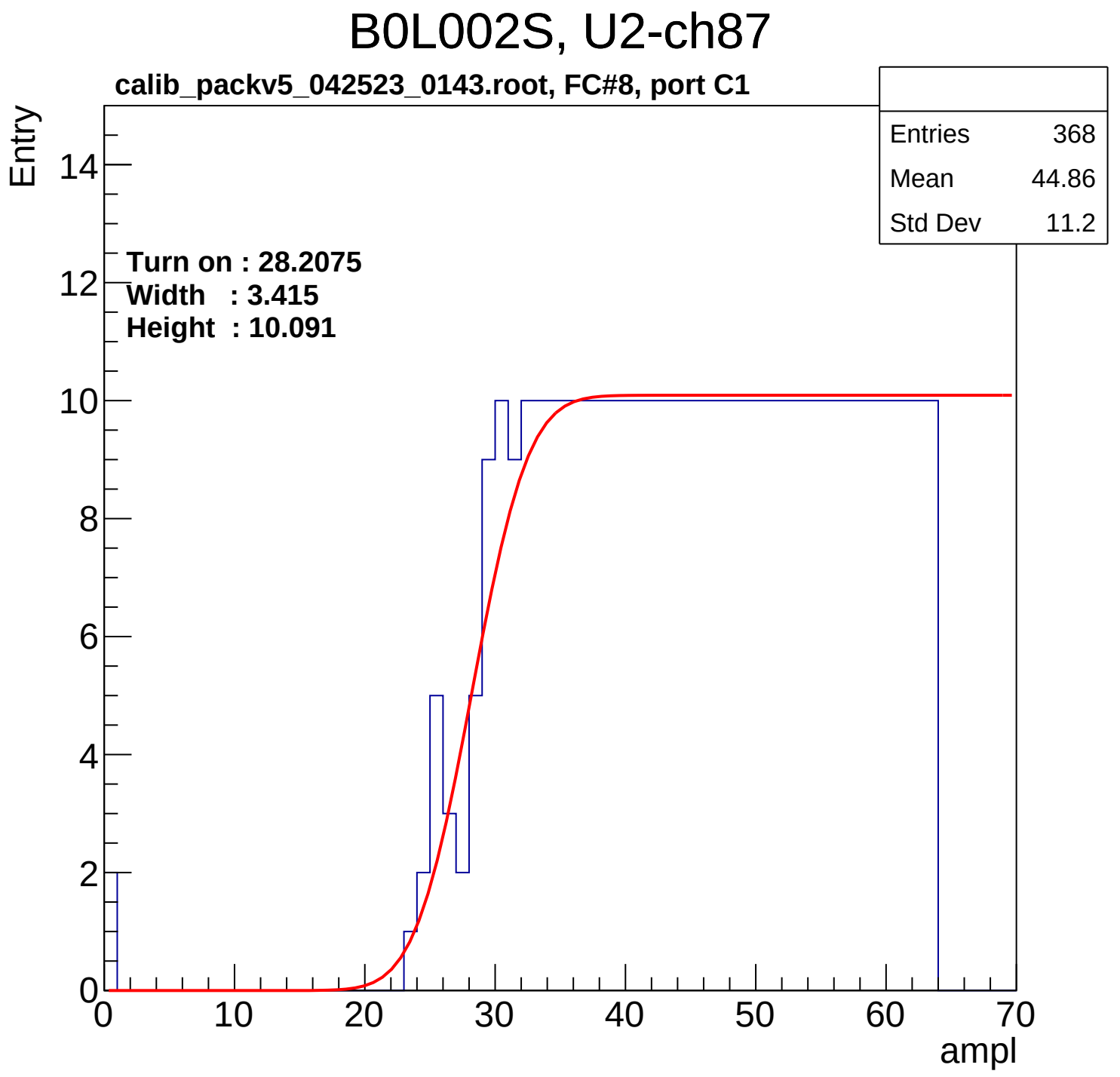
B0L002S, U2-ch87
calib_packv5_042523_0143.root, FC#8, port C1
Entries 368
Mean 44.86
Std Dev 11.2
Turn on : 28.2075
Width : 3.415
Height : 10.091
Entry
ampl
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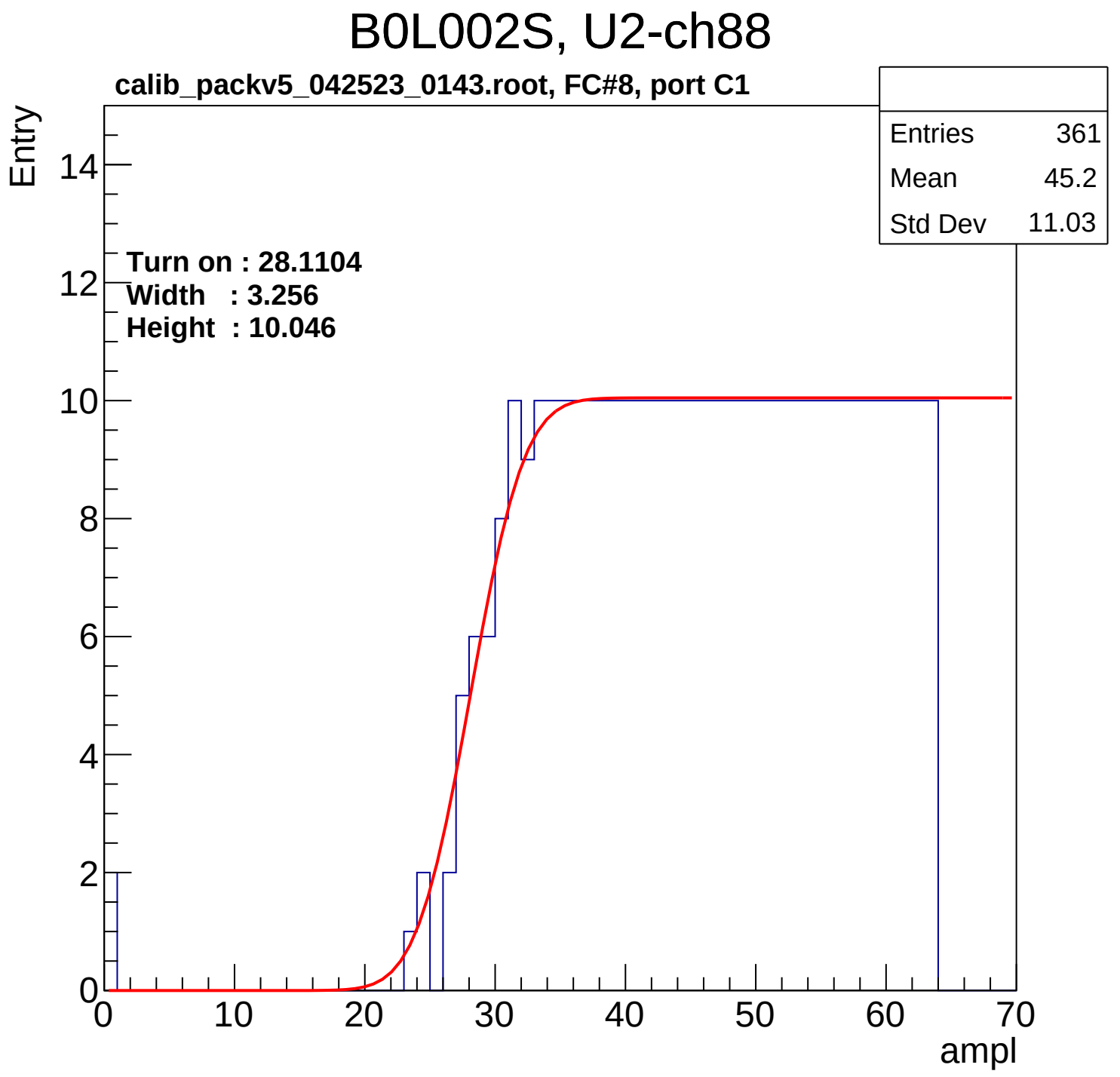
B0L002S, U2-ch88
calib_packv5_042523_0143.root, FC#8, port C1
Entries 361
Mean 45.2
Std Dev 11.03
Turn on : 28.1104
Width : 3.256
Height : 10.046
Entry
ampl
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4
6
8
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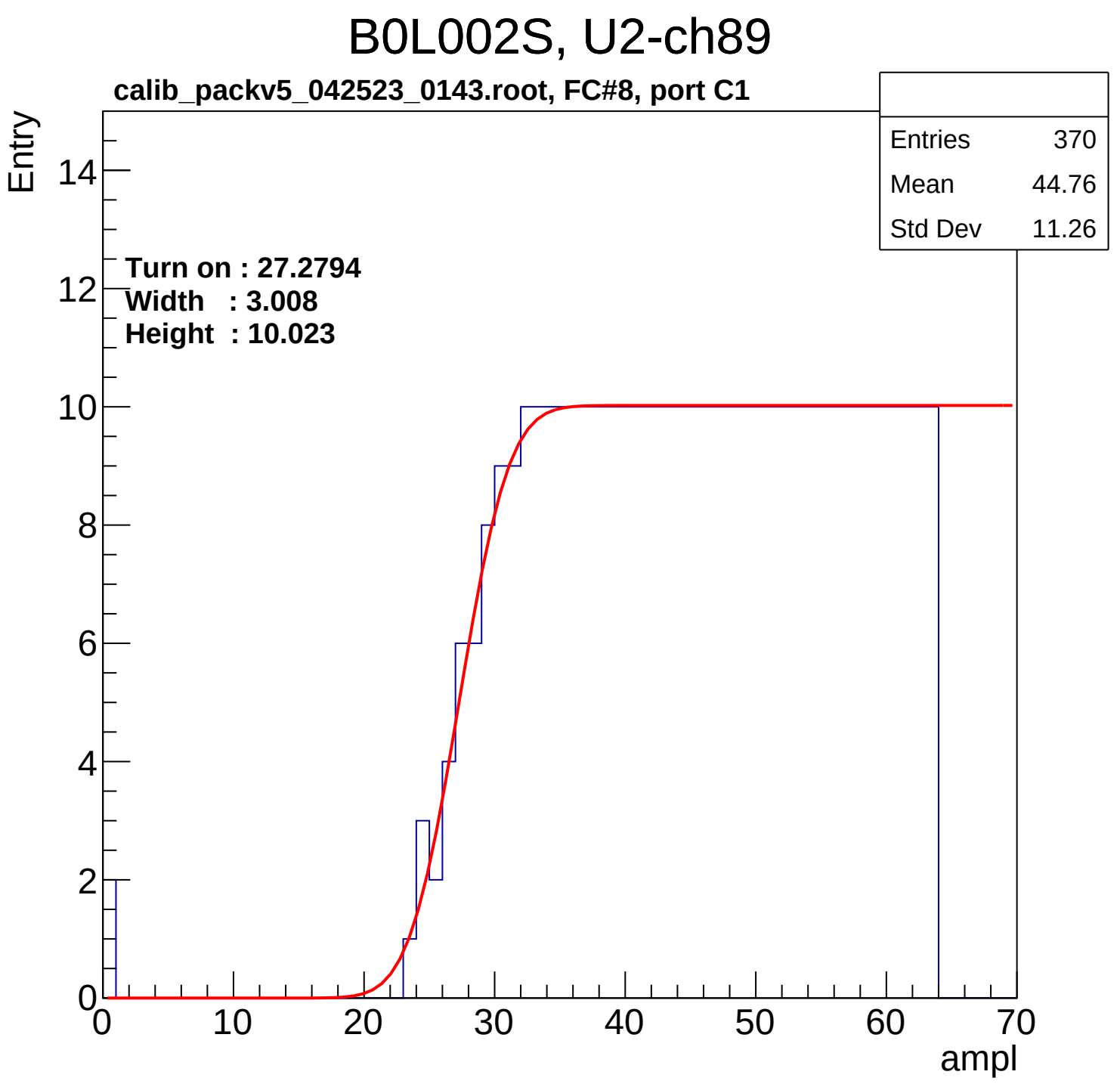
B0L002S, U2-ch89
calib_packv5_042523_0143.root, FC#8, port C1
Entries 370
Mean 44.76
Std Dev 11.26
Turn on : 27.2794
Width : 3.008
Height : 10.023
Entry
ampl
0
2
4
6
8
10
12
14
0
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40
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60
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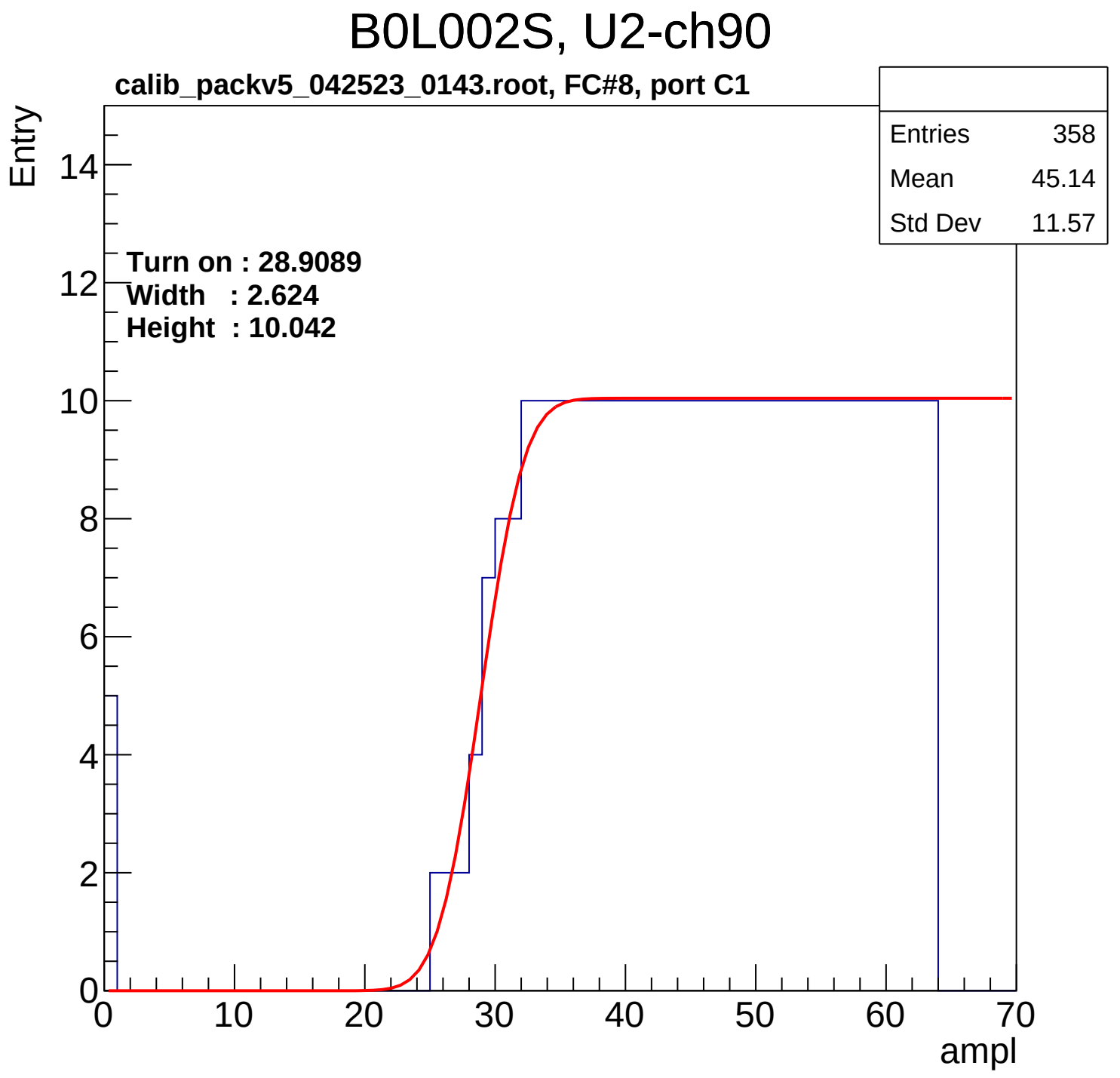
B0L002S, U2-ch90
calib_packv5_042523_0143.root, FC#8, port C1
Entries 358
Mean 45.14
Std Dev 11.57
Turn on : 28.9089
Width : 2.624
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
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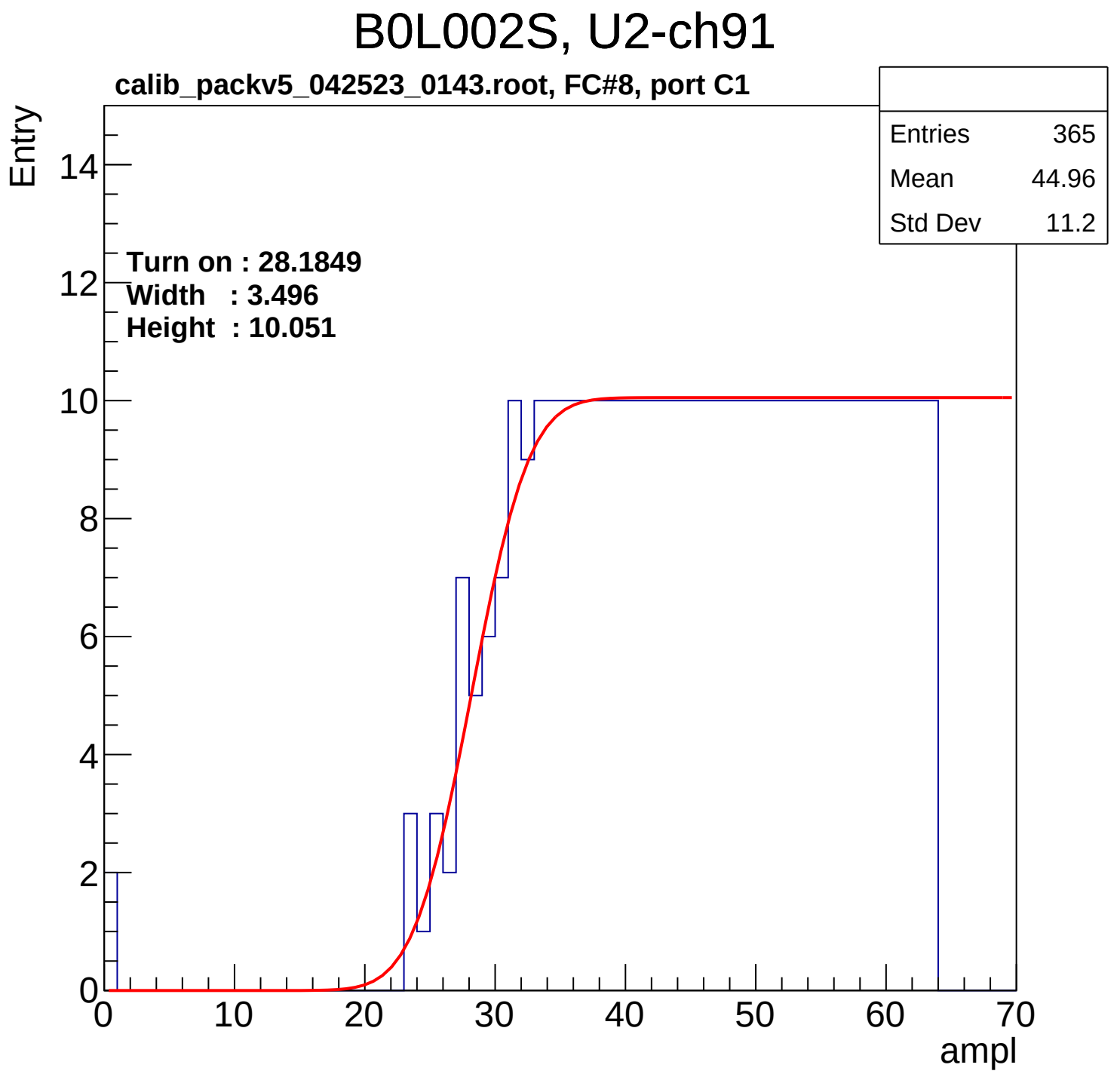
B0L002S, U2-ch91
calib_packv5_042523_0143.root, FC#8, port C1
Entries 365
Mean 44.96
Std Dev 11.2
Turn on : 28.1849
Width : 3.496
Height : 10.051
Entry
ampl
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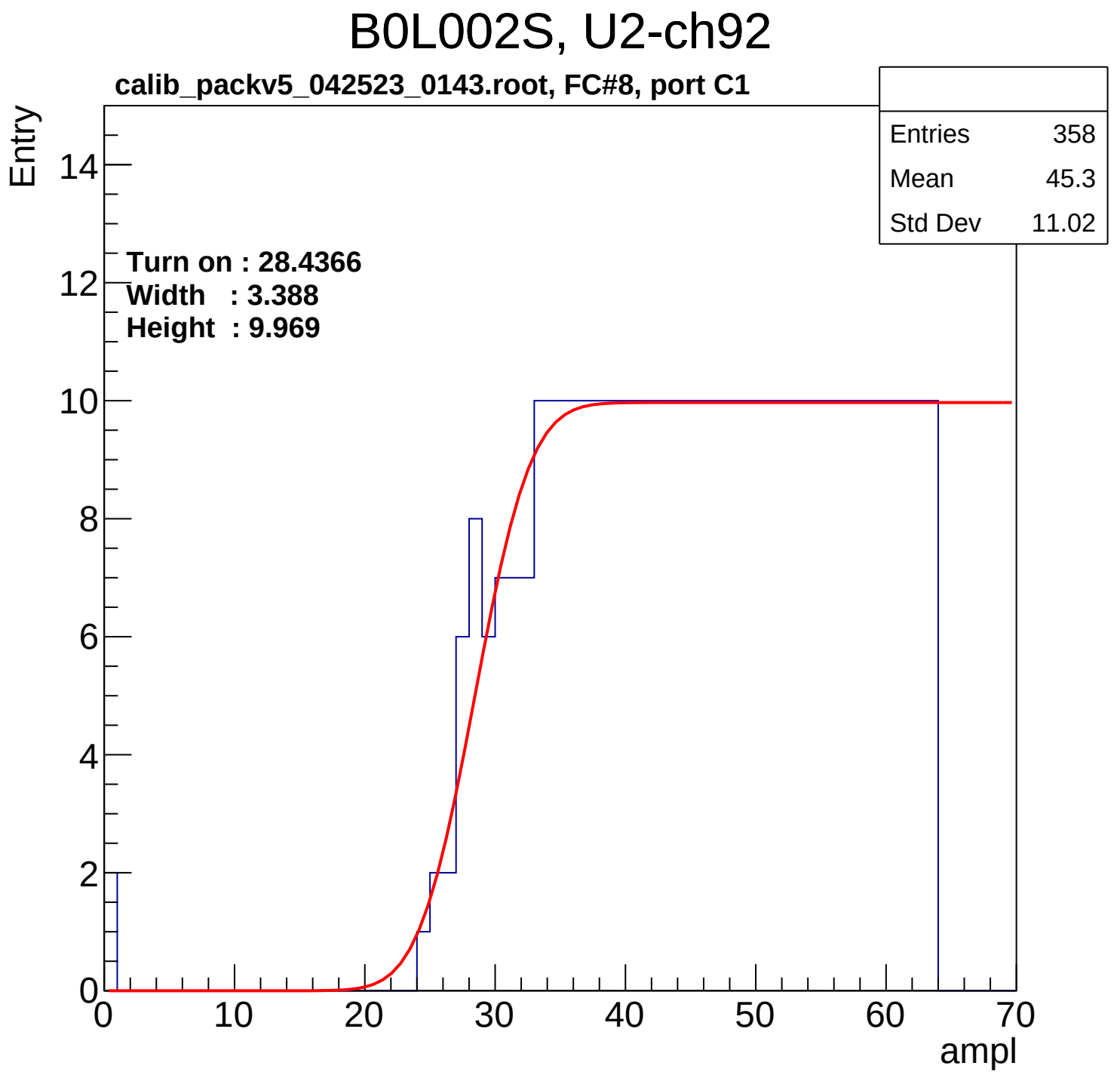
B0L002S, U2-ch92
calib_packv5_042523_0143.root, FC#8, port C1
Entries 358
Mean 45.3
Std Dev 11.02
Turn on : 28.4366
Width : 3.388
Height : 9.969
Entry
ampl
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2
4
6
8
10
12
14
0
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60
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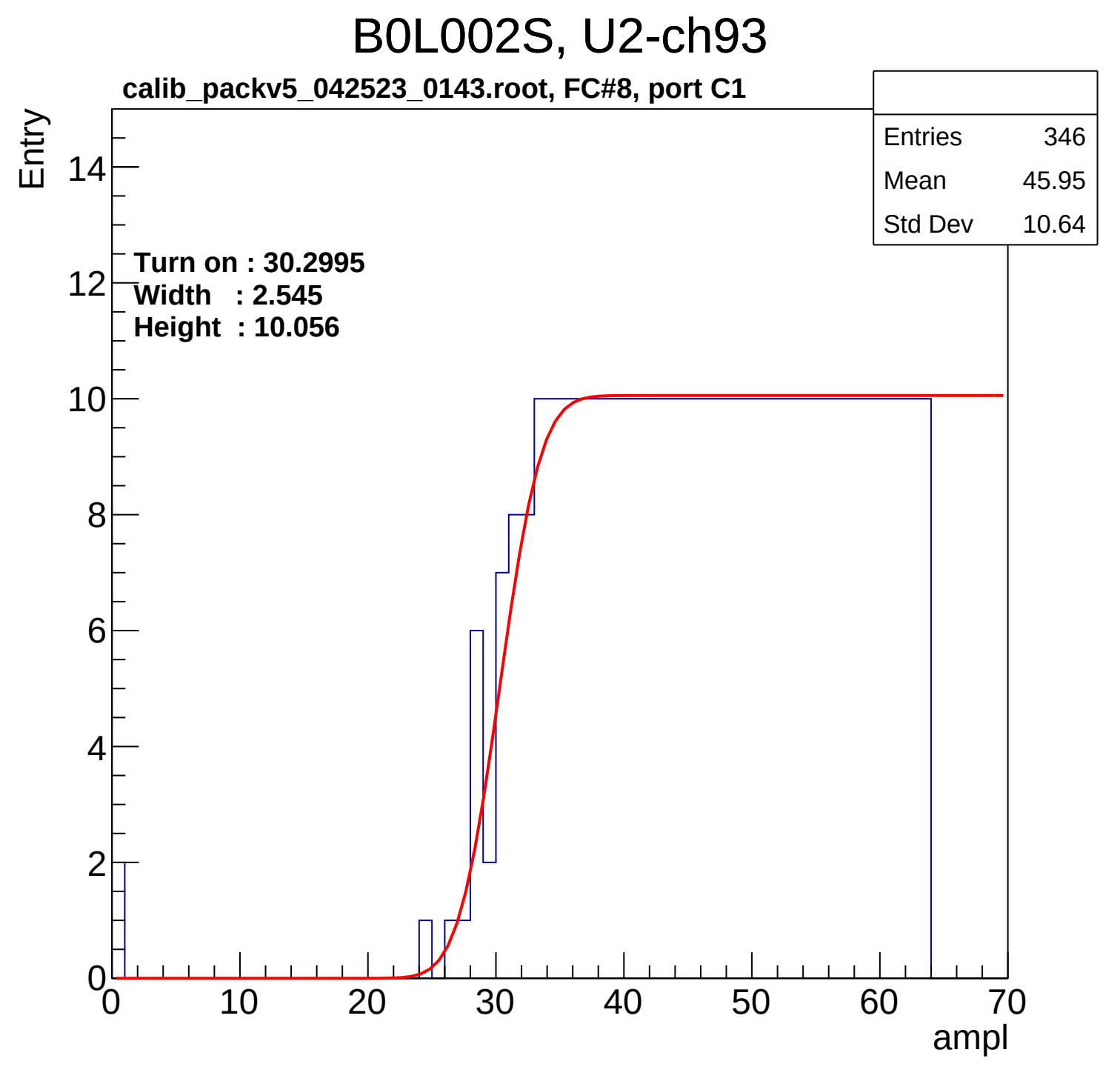
B0L002S, U2-ch93
calib_packv5_042523_0143.root, FC#8, port C1
Entries 346
Mean 45.95
Std Dev 10.64
Turn on : 30.2995
Width : 2.545
Height : 10.056
Entry
ampl
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2
4
6
8
10
12
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0
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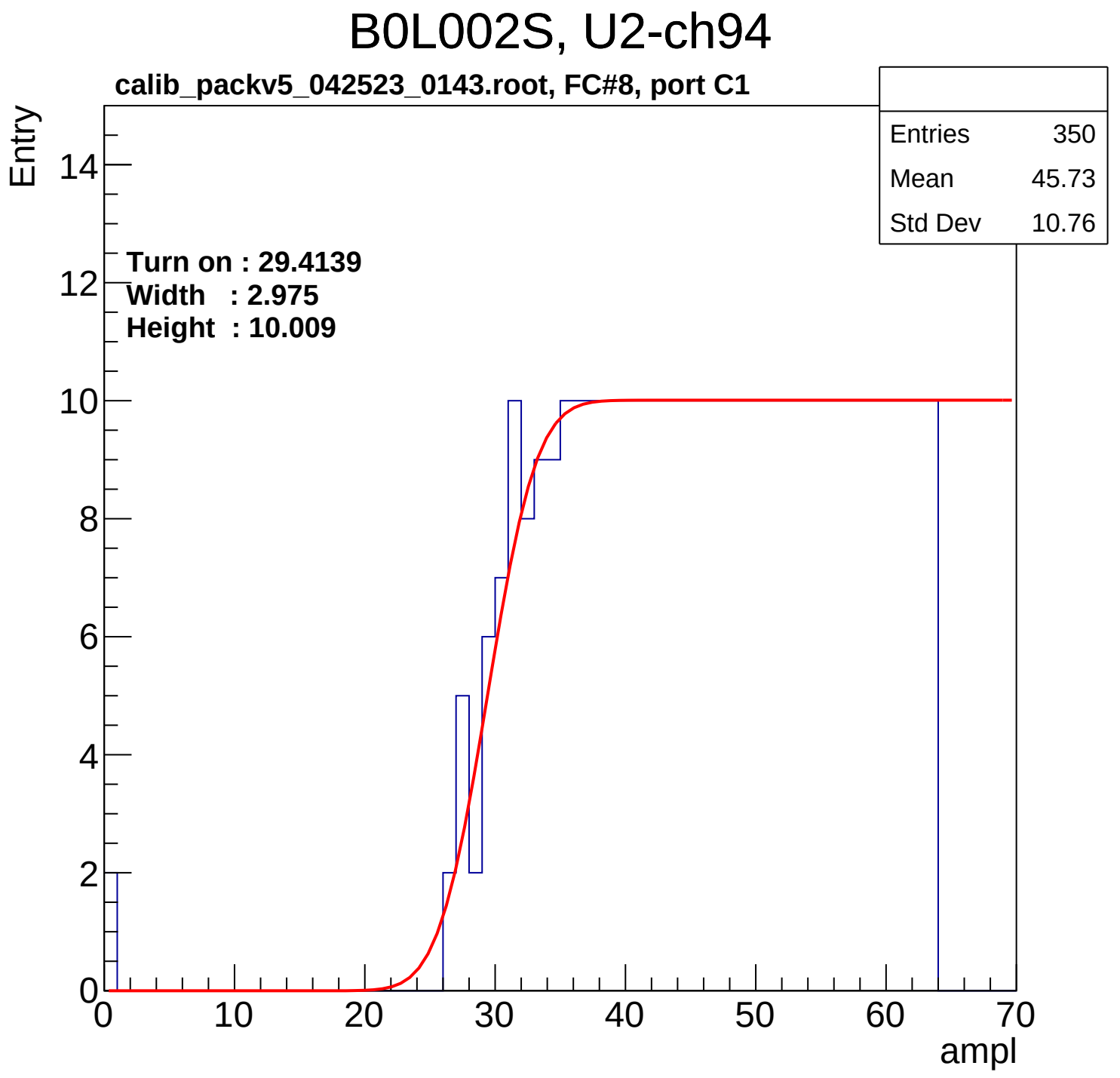
B0L002S, U2-ch94
calib_packv5_042523_0143.root, FC#8, port C1
Entries 350
Mean 45.73
Std Dev 10.76
Turn on : 29.4139
Width : 2.975
Height : 10.009
Entry
ampl
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2
4
6
8
10
12
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0
10
20
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40
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60
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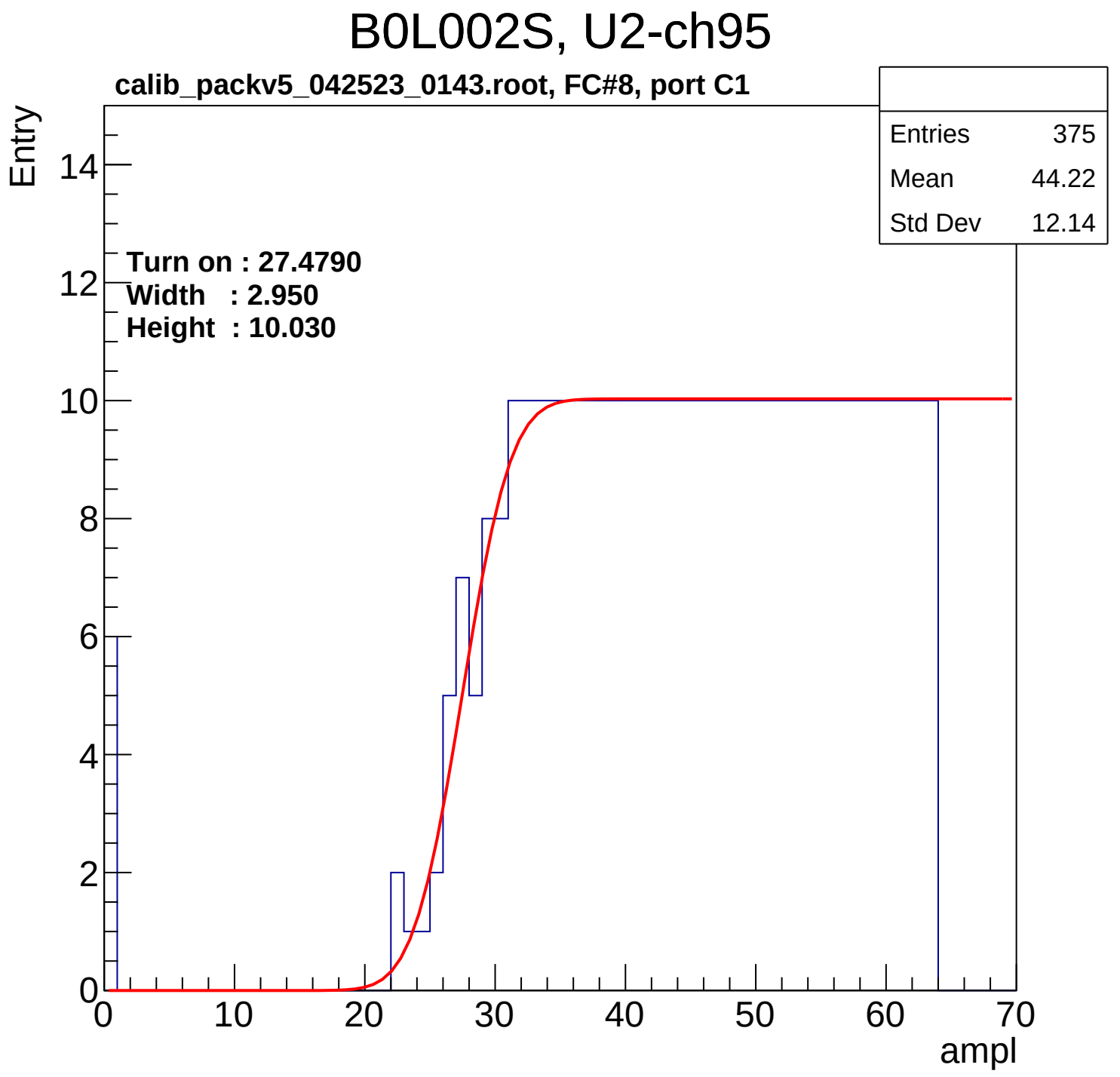
B0L002S, U2-ch95
calib_packv5_042523_0143.root, FC#8, port C1
Entries 375
Mean 44.22
Std Dev 12.14
Turn on : 27.4790
Width : 2.950
Height : 10.030
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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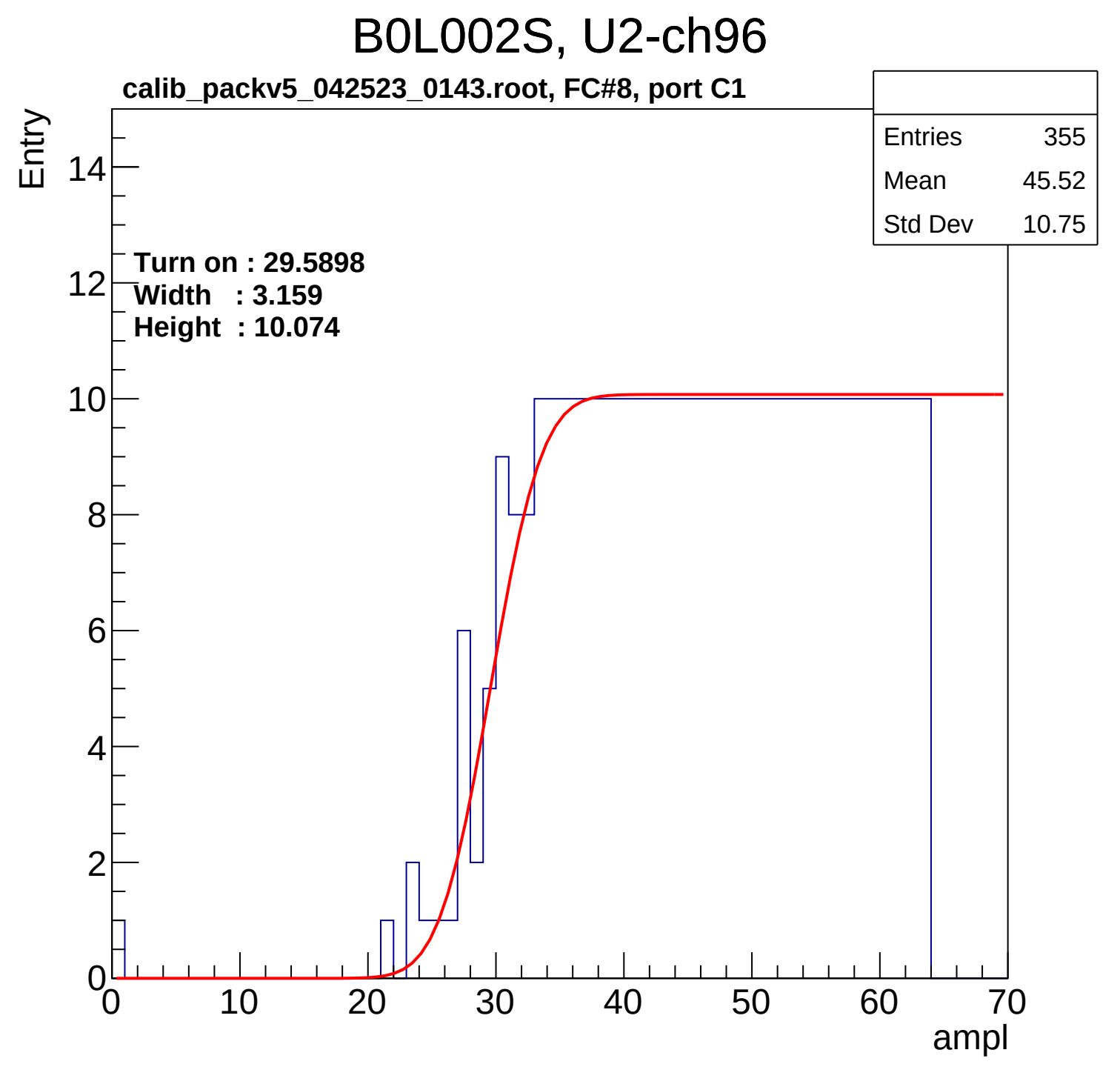
B0L002S, U2-ch96
calib_packv5_042523_0143.root, FC#8, port C1
Entries 355
Mean 45.52
Std Dev 10.75
Turn on : 29.5898
Width : 3.159
Height : 10.074
Entry
ampl
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2
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6
8
10
12
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0
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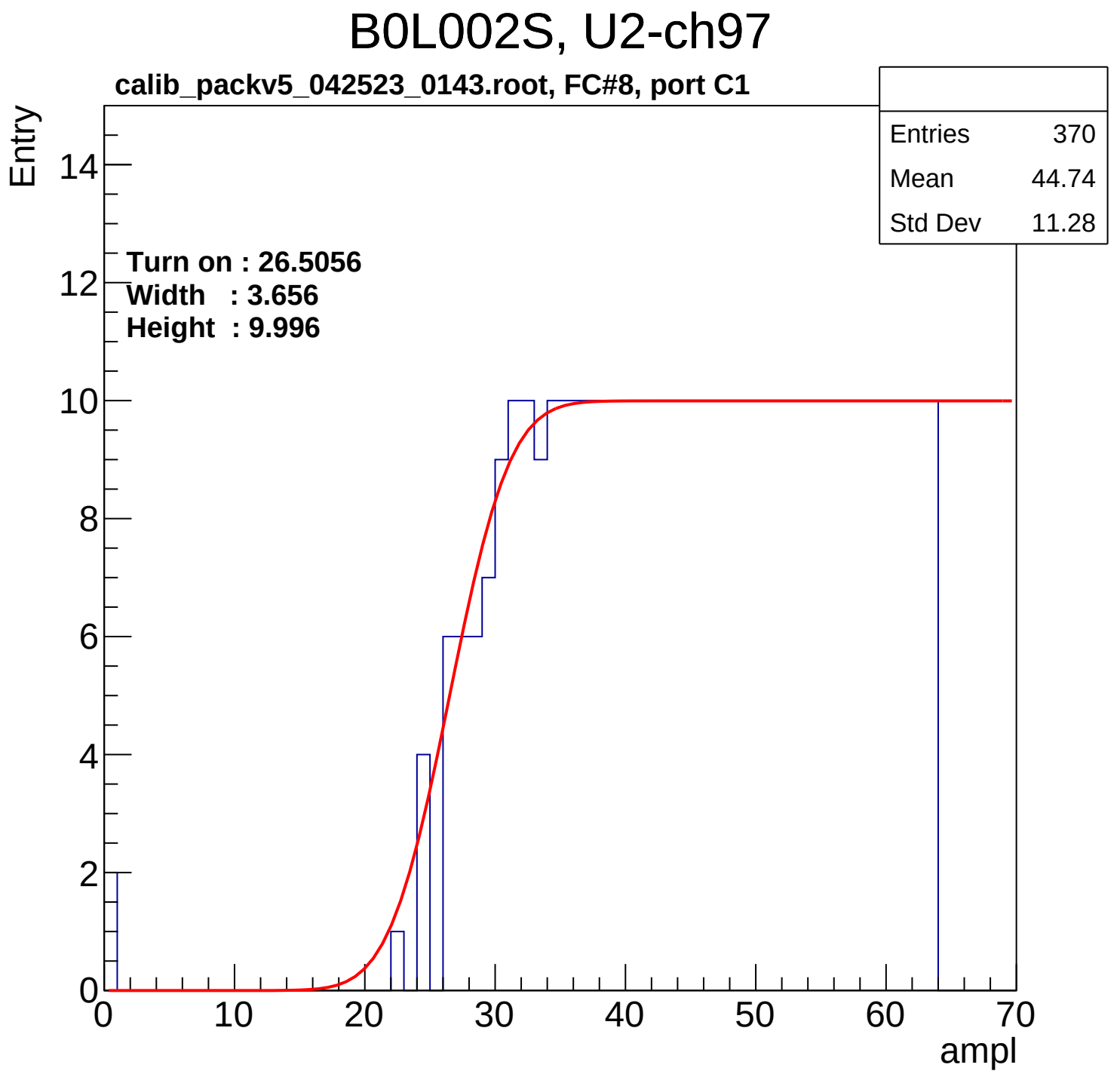
B0L002S, U2-ch97
calib_packv5_042523_0143.root, FC#8, port C1
Entries 370
Mean 44.74
Std Dev 11.28
Turn on : 26.5056
Width : 3.656
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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60
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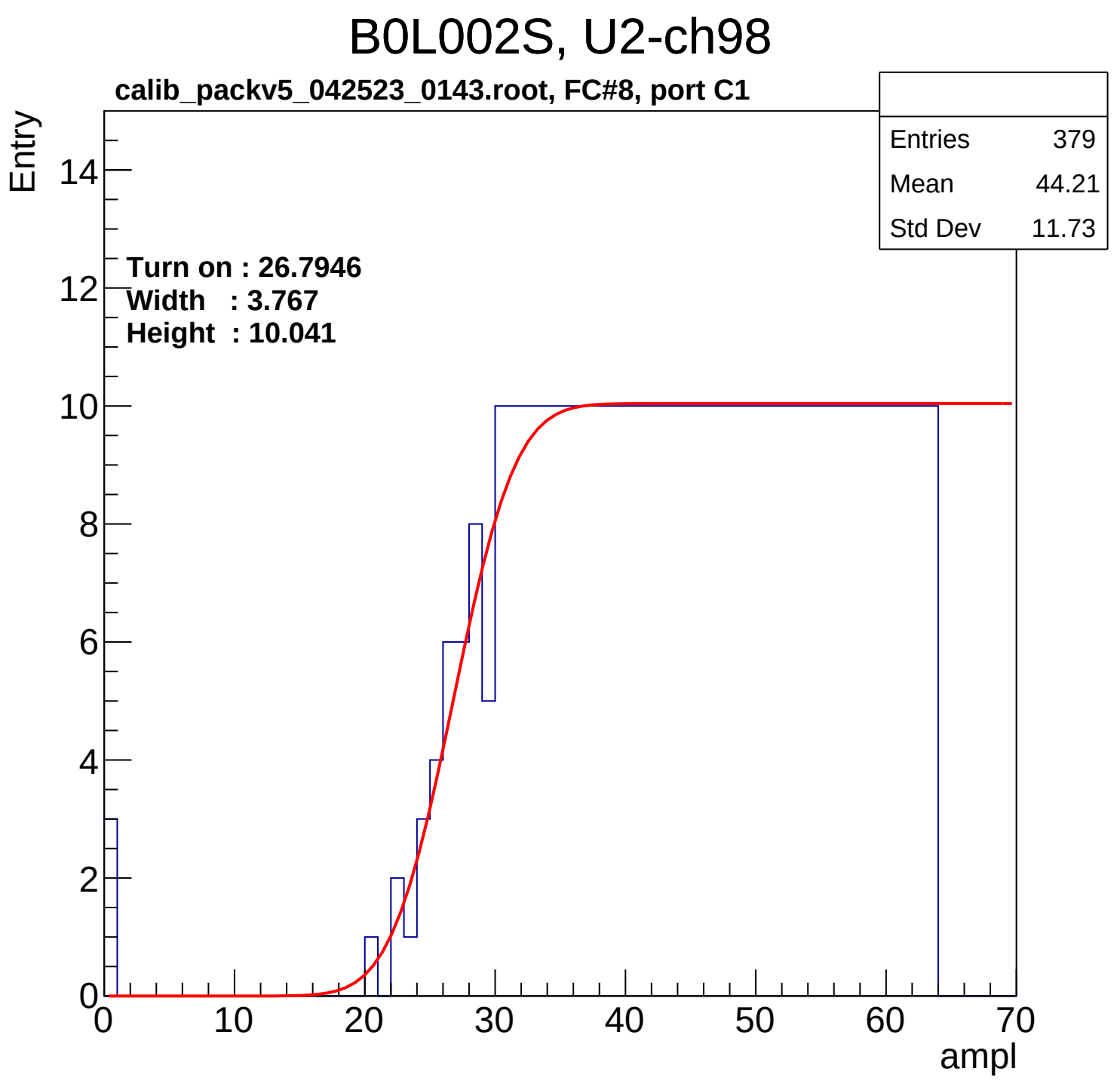
B0L002S, U2-ch98
calib_packv5_042523_0143.root, FC#8, port C1
Entries 379
Mean 44.21
Std Dev 11.73
Turn on : 26.7946
Width : 3.767
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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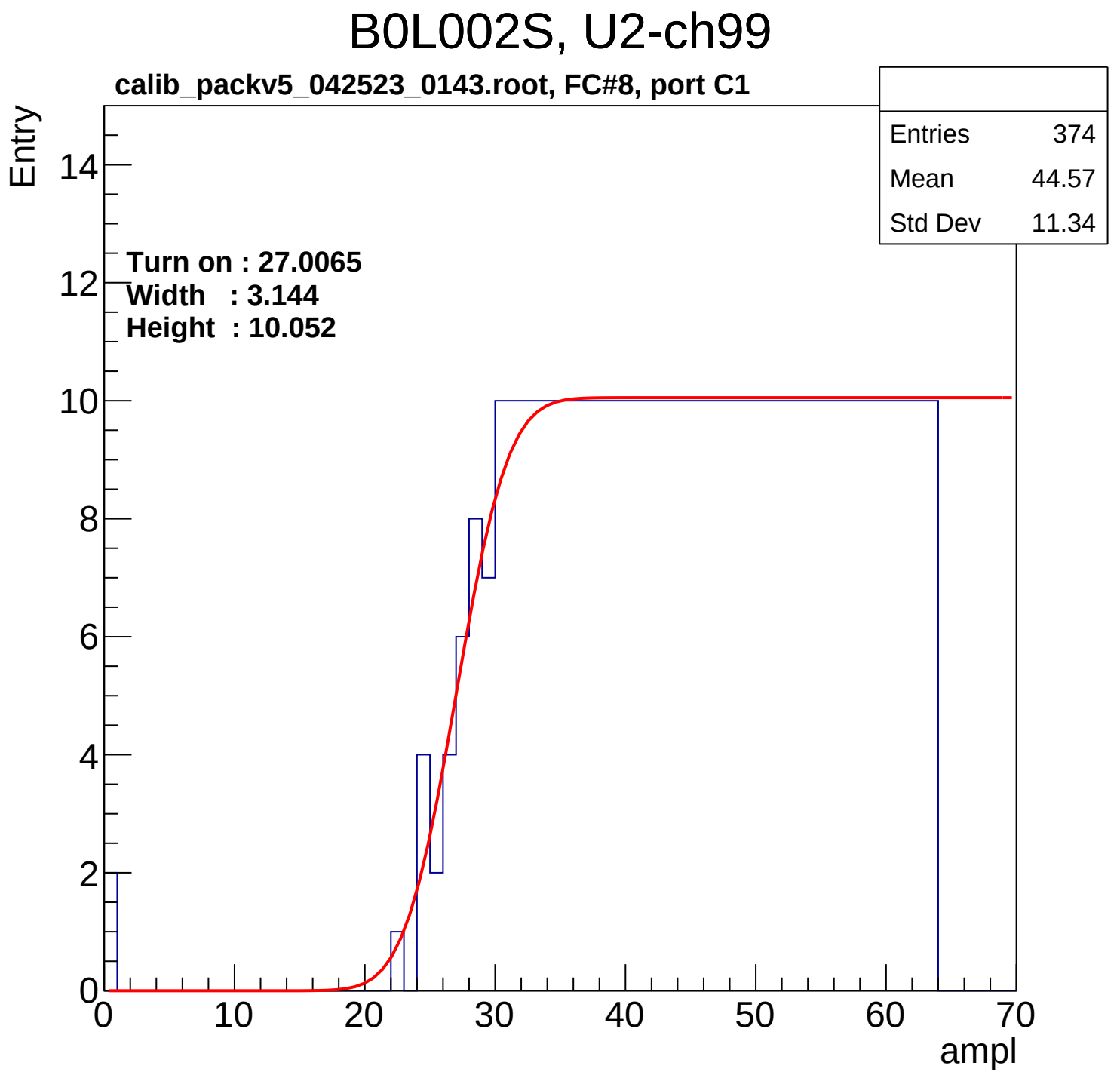
B0L002S, U2-ch99
calib_packv5_042523_0143.root, FC#8, port C1
Entries 374
Mean 44.57
Std Dev 11.34
Turn on : 27.0065
Width : 3.144
Height : 10.052
Entry
ampl
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6
8
10
12
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0
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20
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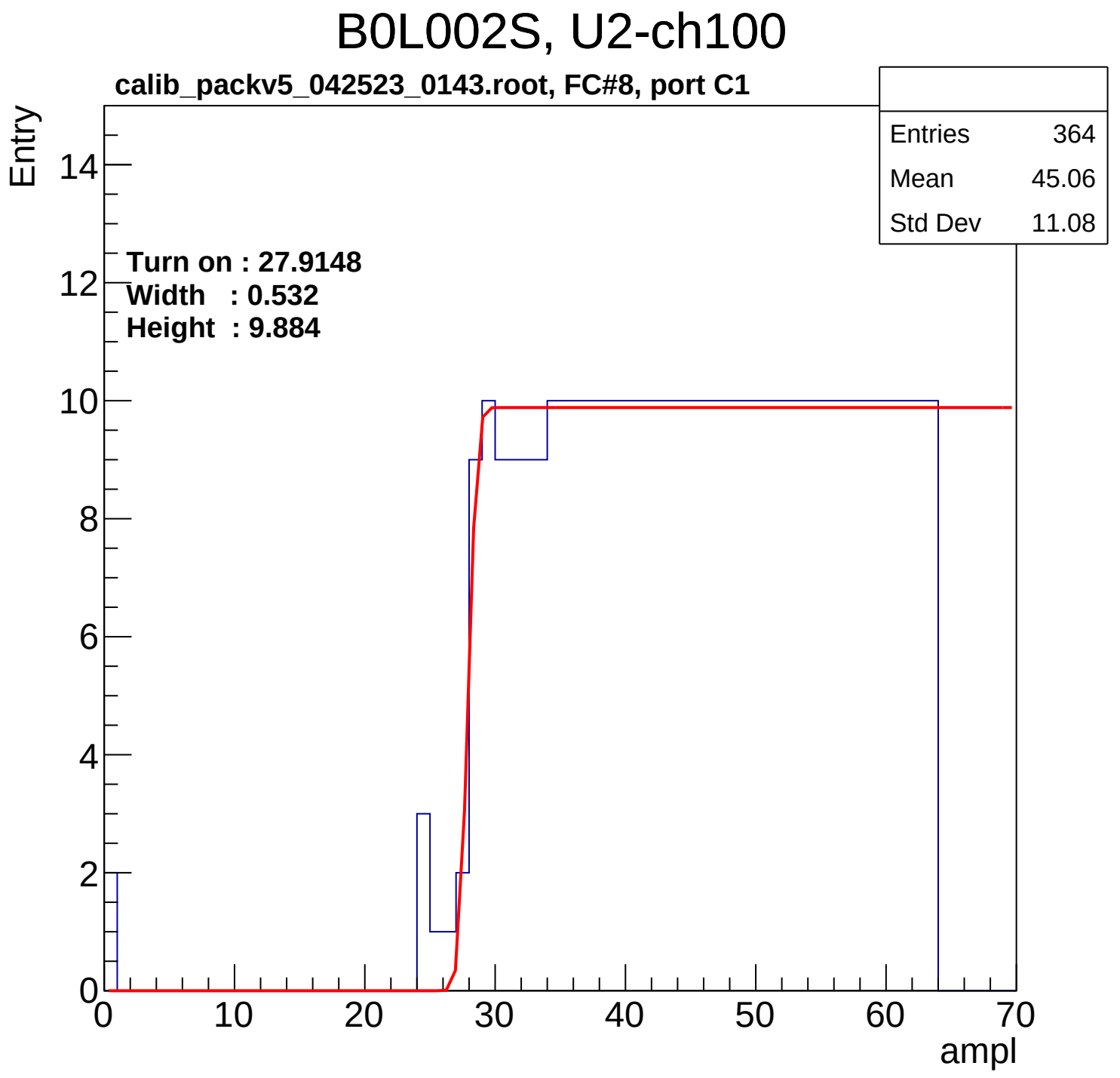
B0L002S, U2-ch100
calib_packv5_042523_0143.root, FC#8, port C1
Entries 364
Mean 45.06
Std Dev 11.08
Turn on : 27.9148
Width : 0.532
Height : 9.884
Entry
ampl
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4
6
8
10
12
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0
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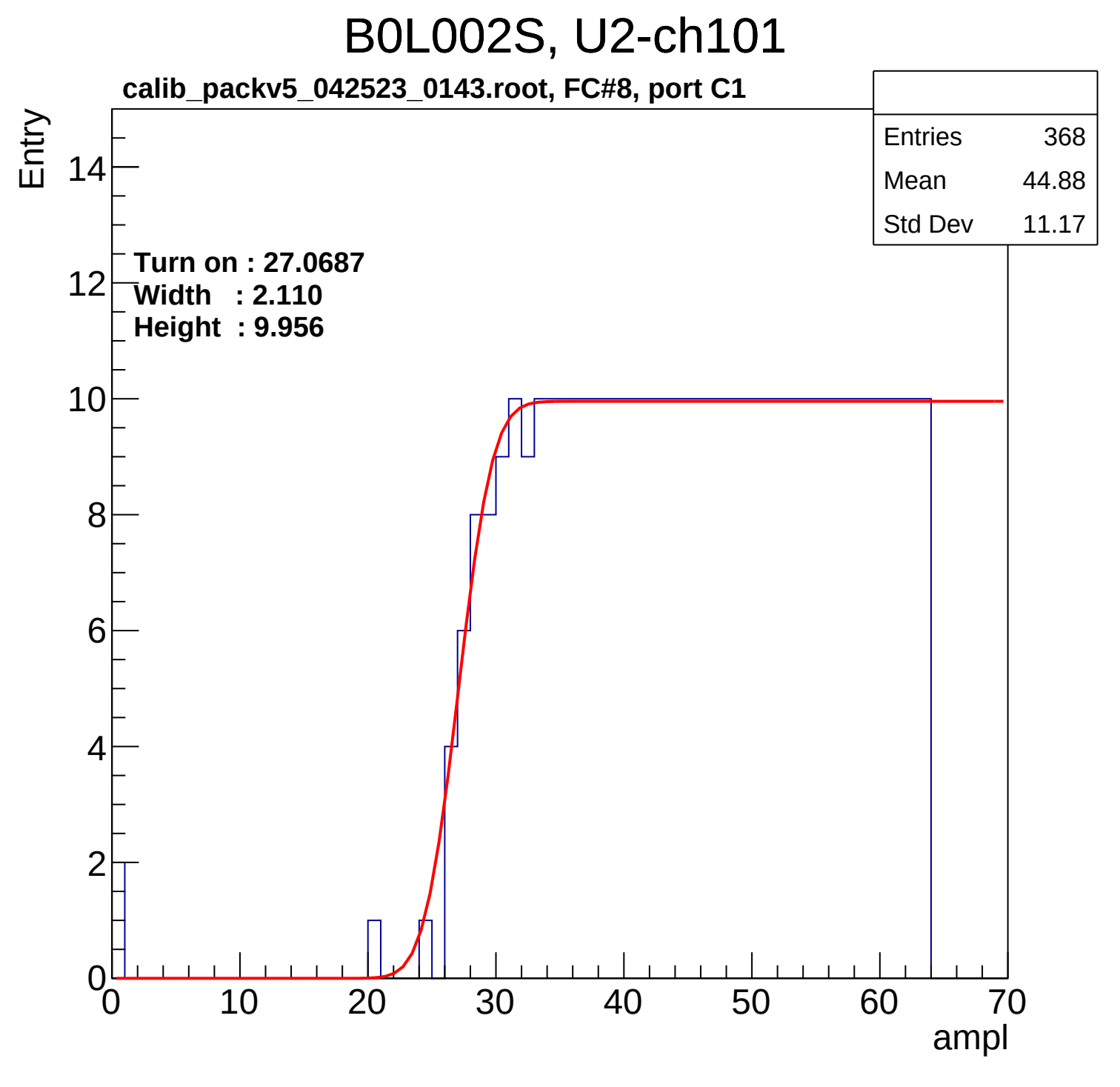
B0L002S, U2-ch101
calib_packv5_042523_0143.root, FC#8, port C1
Entries 368
Mean 44.88
Std Dev 11.17
Turn on : 27.0687
Width : 2.110
Height : 9.956
Entry
ampl
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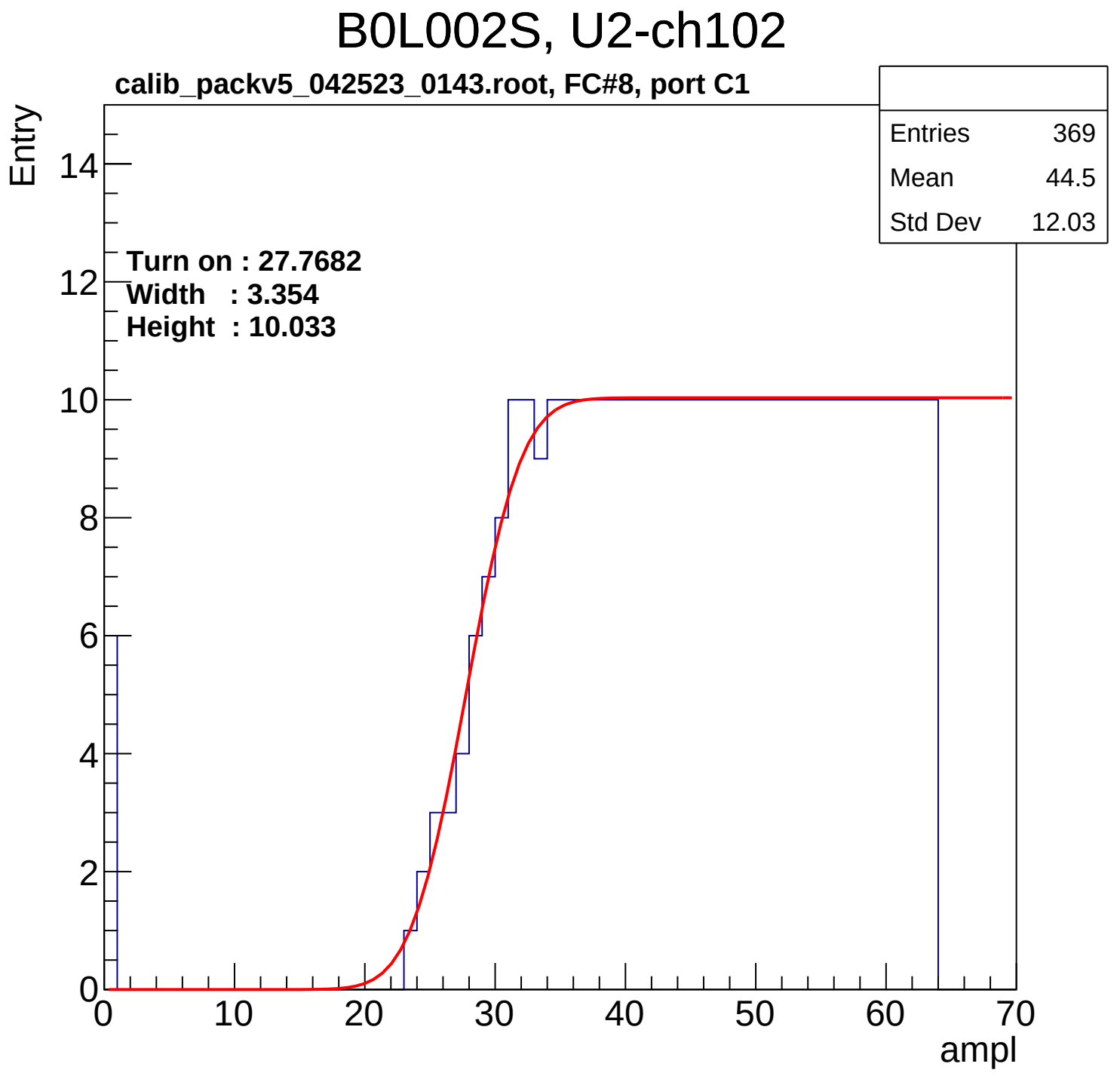
B0L002S, U2-ch102
calib_packv5_042523_0143.root, FC#8, port C1
Entries 369
Mean 44.5
Std Dev 12.03
Turn on : 27.7682
Width : 3.354
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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60
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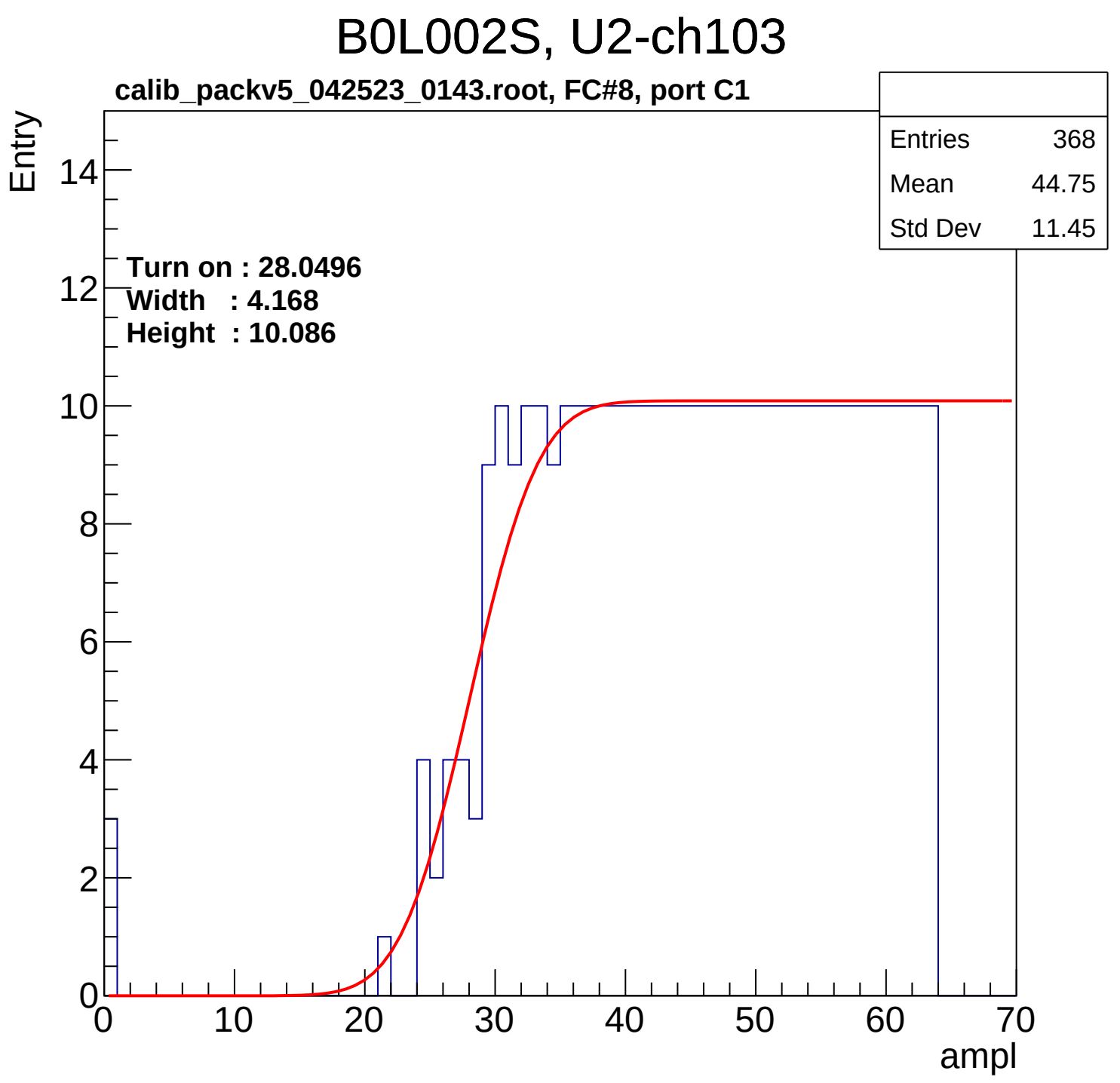
B0L002S, U2-ch103
calib_packv5_042523_0143.root, FC#8, port C1
Entries 368
Mean 44.75
Std Dev 11.45
Turn on : 28.0496
Width : 4.168
Height : 10.086
Entry
ampl
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4
6
8
10
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0
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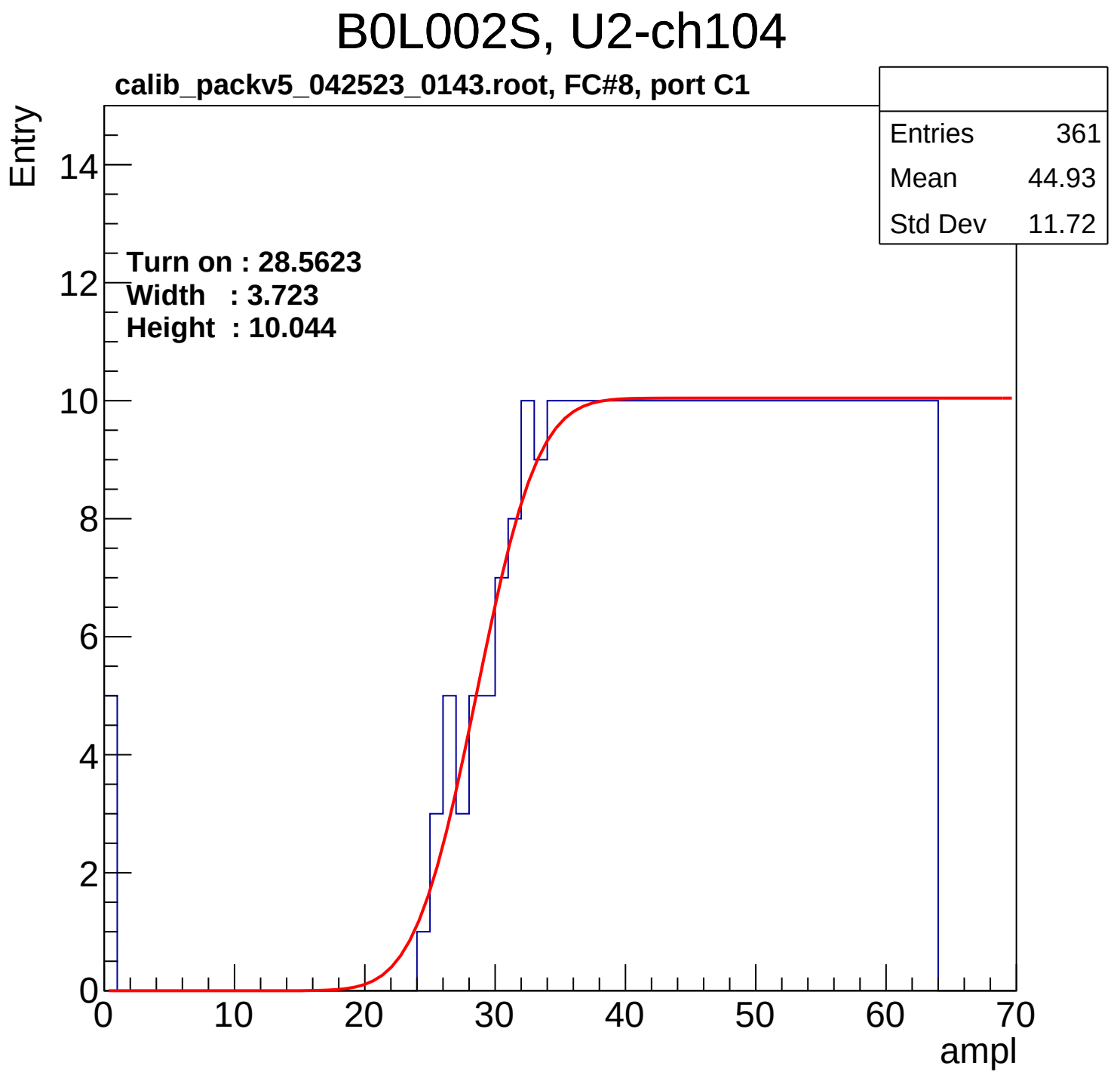
B0L002S, U2-ch104
calib_packv5_042523_0143.root, FC#8, port C1
Entries 361
Mean 44.93
Std Dev 11.72
Turn on : 28.5623
Width : 3.723
Height : 10.044
Entry
ampl
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6
8
10
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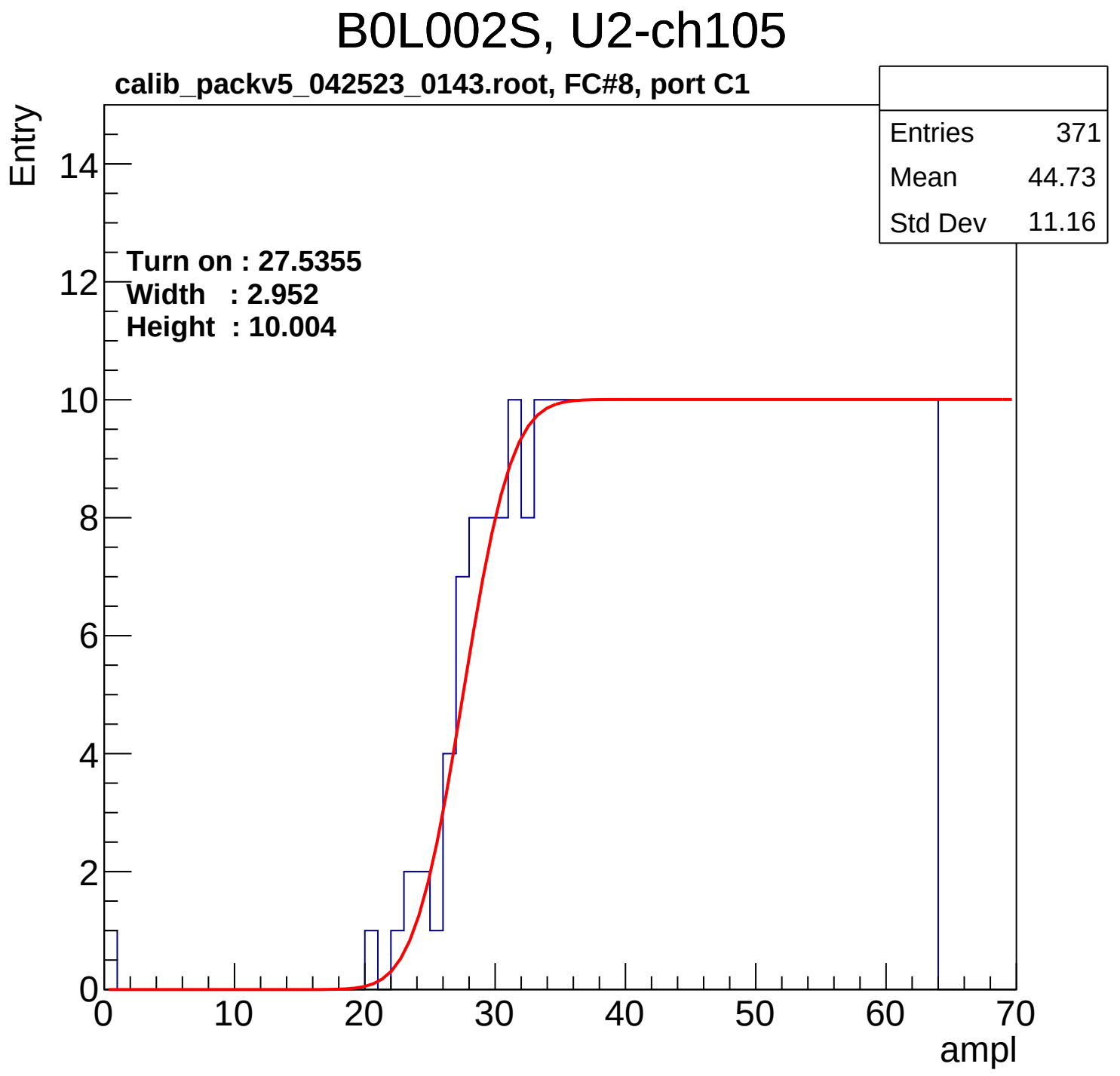
B0L002S, U2-ch105
calib_packv5_042523_0143.root, FC#8, port C1
Entries 371
Mean 44.73
Std Dev 11.16
Turn on : 27.5355
Width : 2.952
Height : 10.004
Entry
ampl
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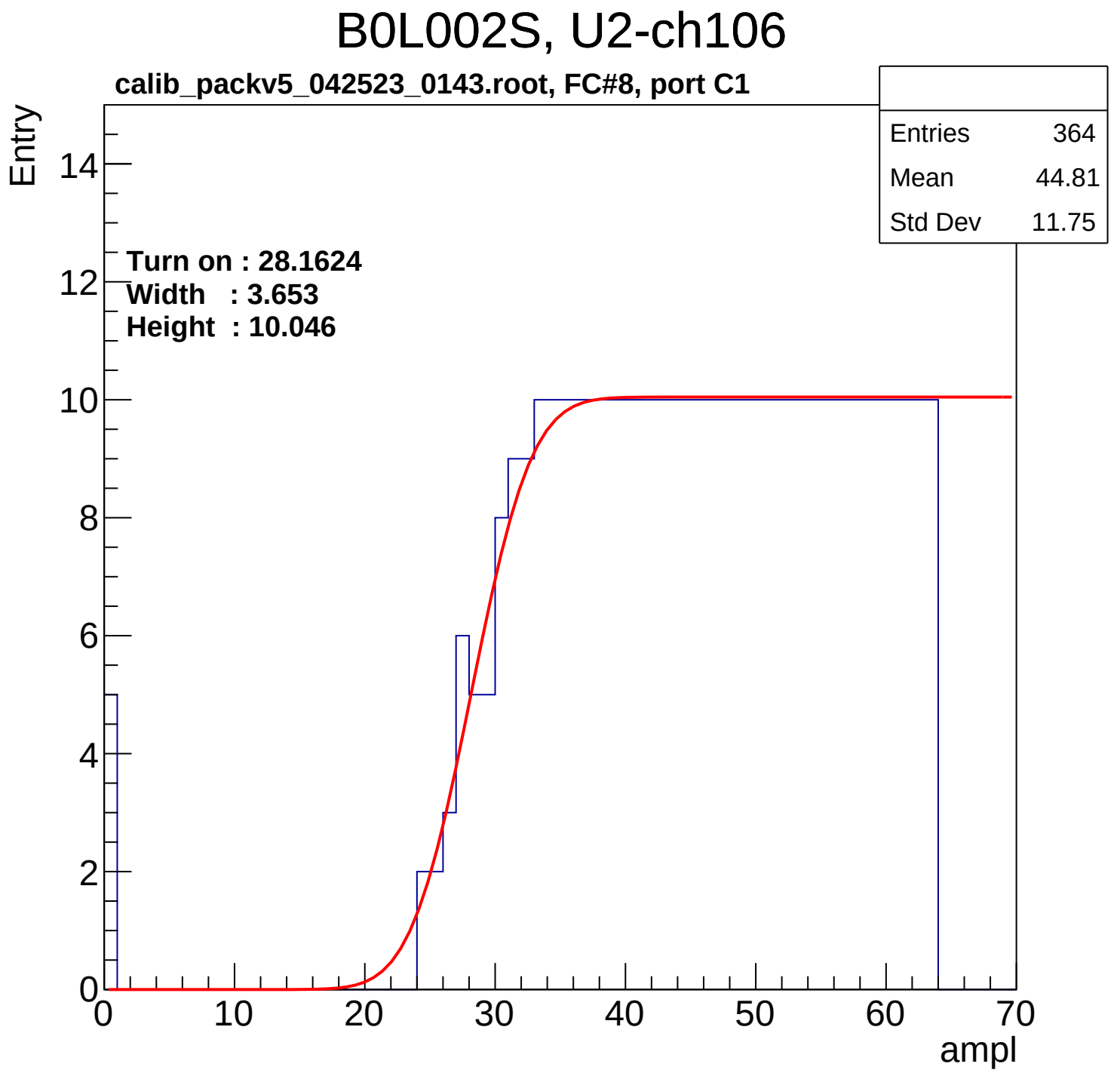
B0L002S, U2-ch106
calib_packv5_042523_0143.root, FC#8, port C1
Entries 364
Mean 44.81
Std Dev 11.75
Turn on : 28.1624
Width : 3.653
Height : 10.046
Entry
ampl
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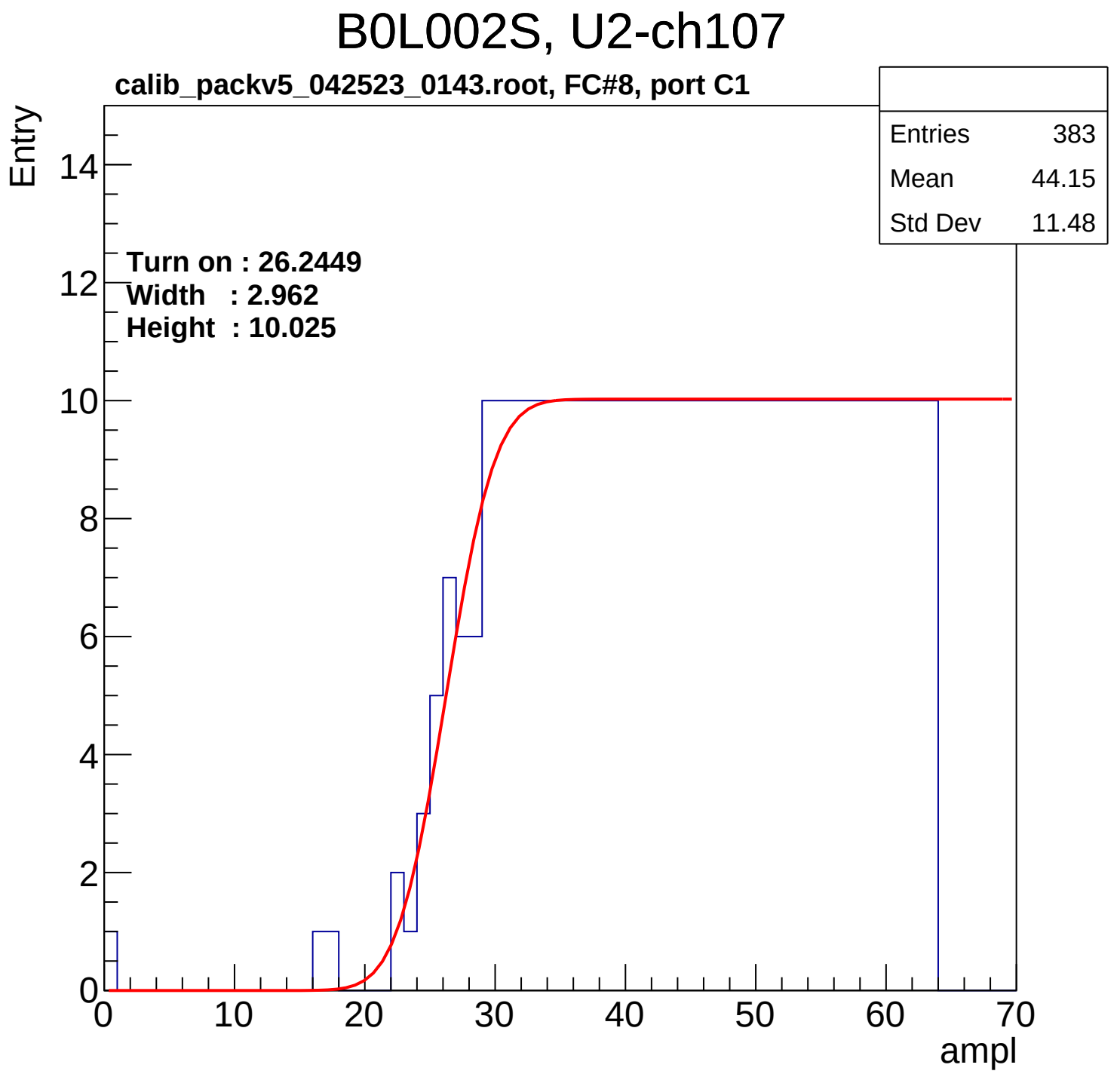
B0L002S, U2-ch107
calib_packv5_042523_0143.root, FC#8, port C1
Entries 383
Mean 44.15
Std Dev 11.48
Turn on : 26.2449
Width : 2.962
Height : 10.025
Entry
ampl
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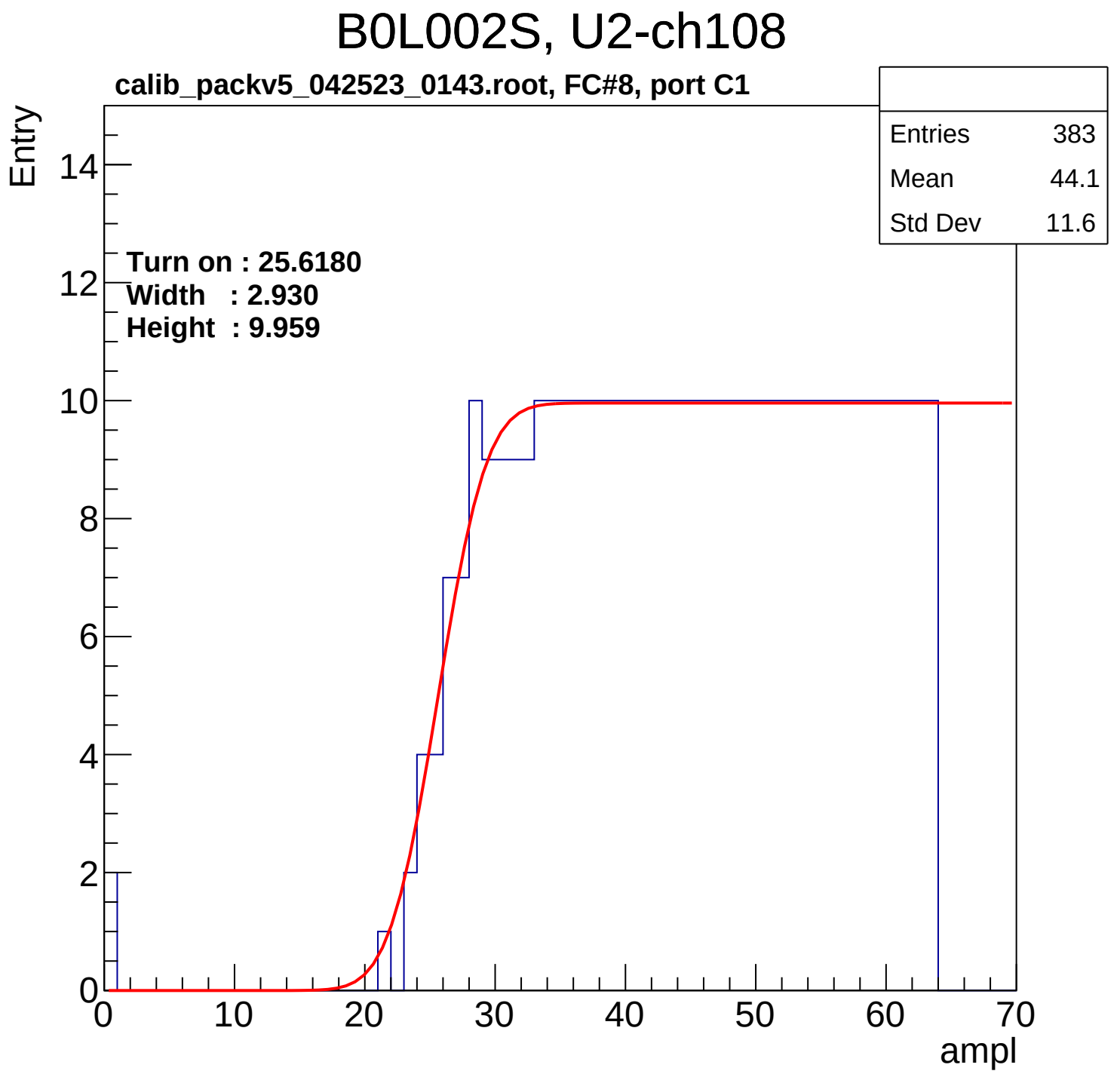
B0L002S, U2-ch108
calib_packv5_042523_0143.root, FC#8, port C1
Entries 383
Mean 44.1
Std Dev 11.6
Turn on : 25.6180
Width : 2.930
Height : 9.959
Entry
ampl
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2
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8
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0
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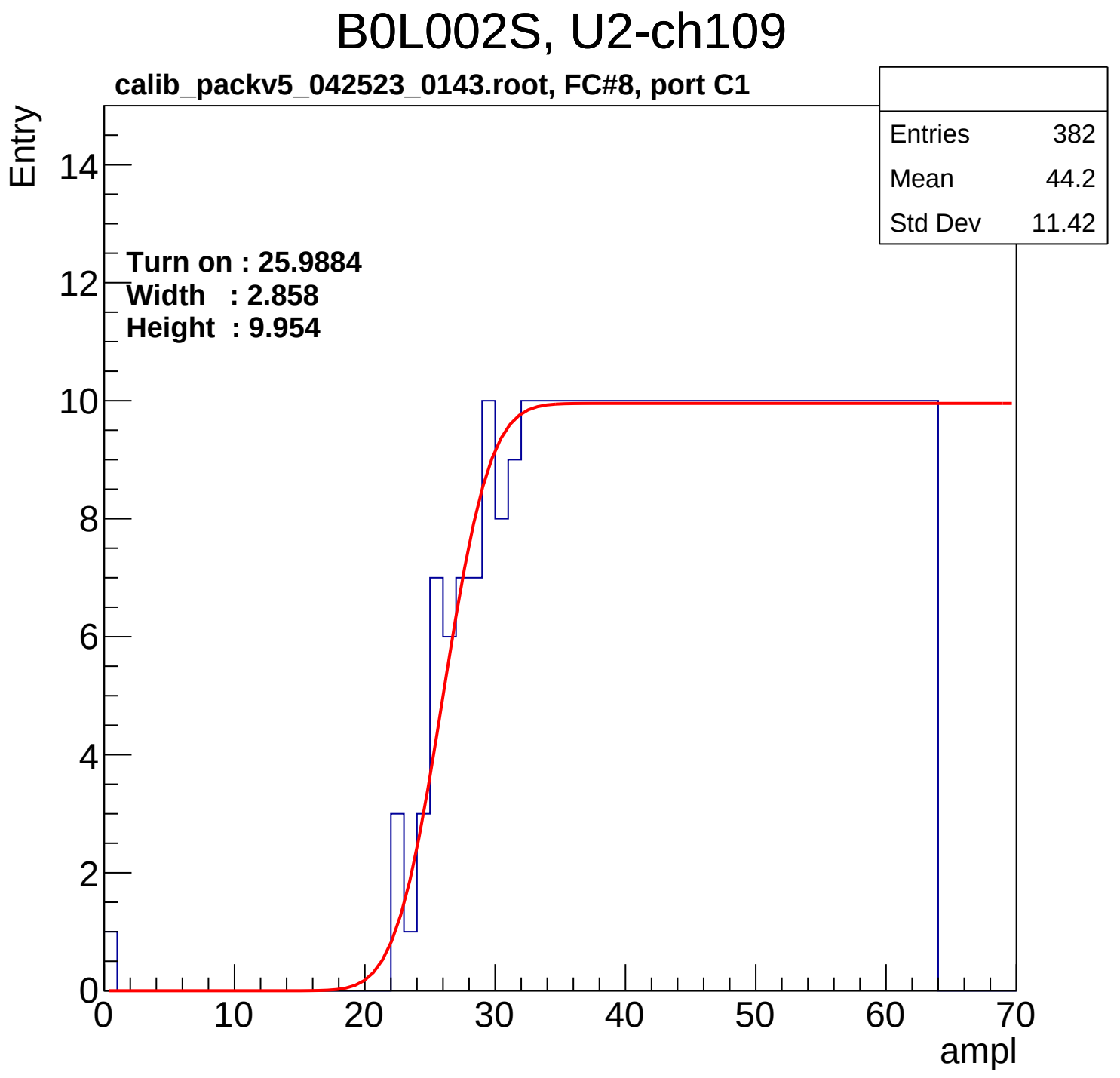
B0L002S, U2-ch109
calib_packv5_042523_0143.root, FC#8, port C1
Entries 382
Mean 44.2
Std Dev 11.42
Turn on : 25.9884
Width : 2.858
Height : 9.954
Entry
ampl
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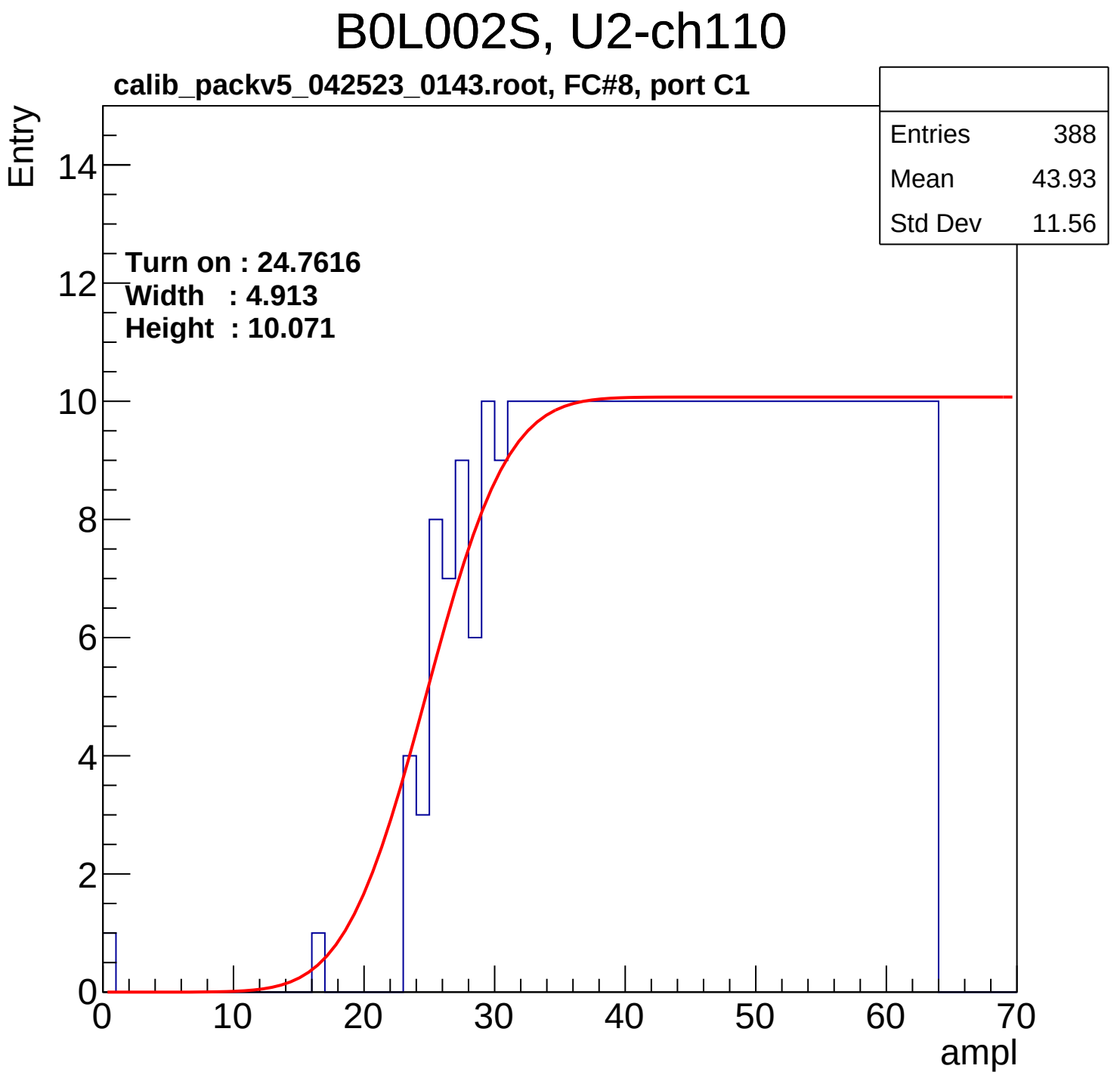
B0L002S, U2-ch110
calib_packv5_042523_0143.root, FC#8, port C1
Entries 388
Mean 43.93
Std Dev 11.56
Turn on : 24.7616
Width : 4.913
Height : 10.071
Entry
ampl
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2
4
6
8
10
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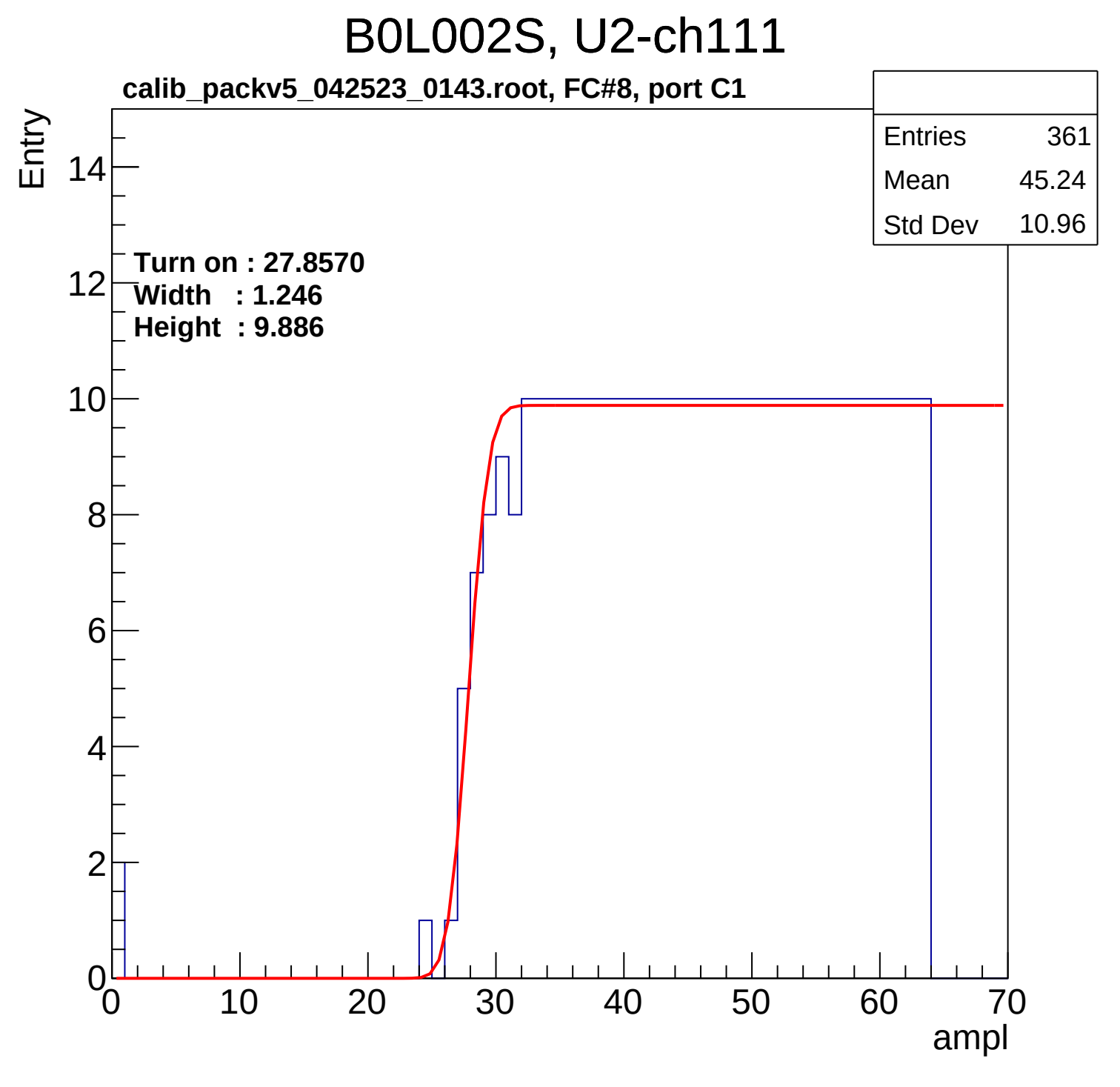
B0L002S, U2-ch111
calib_packv5_042523_0143.root, FC#8, port C1
Entries 361
Mean 45.24
Std Dev 10.96
Turn on : 27.8570
Width : 1.246
Height : 9.886
Entry
ampl
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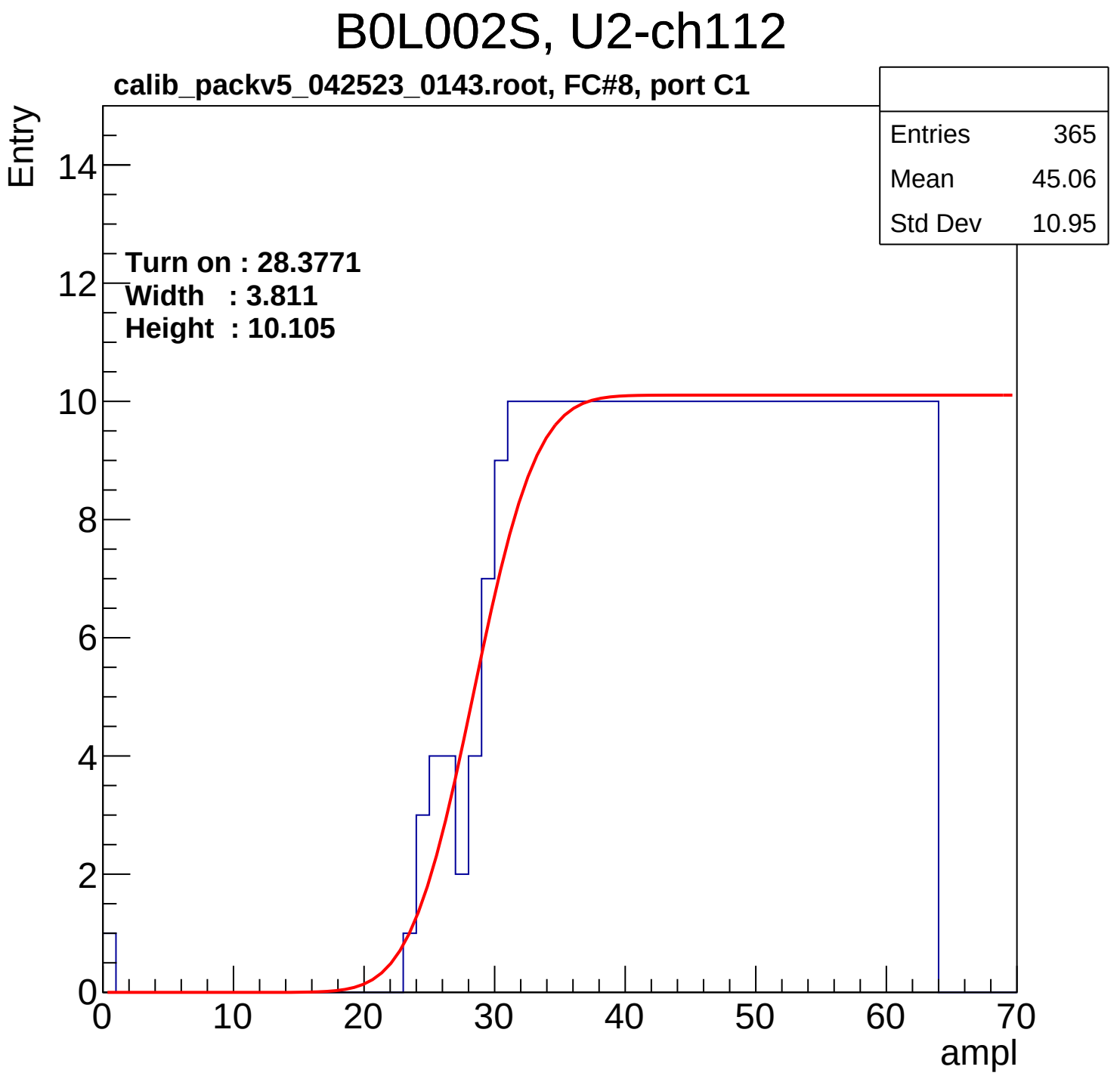
B0L002S, U2-ch112
calib_packv5_042523_0143.root, FC#8, port C1
Entries 365
Mean 45.06
Std Dev 10.95
Turn on : 28.3771
Width : 3.811
Height : 10.105
Entry
ampl
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6
8
10
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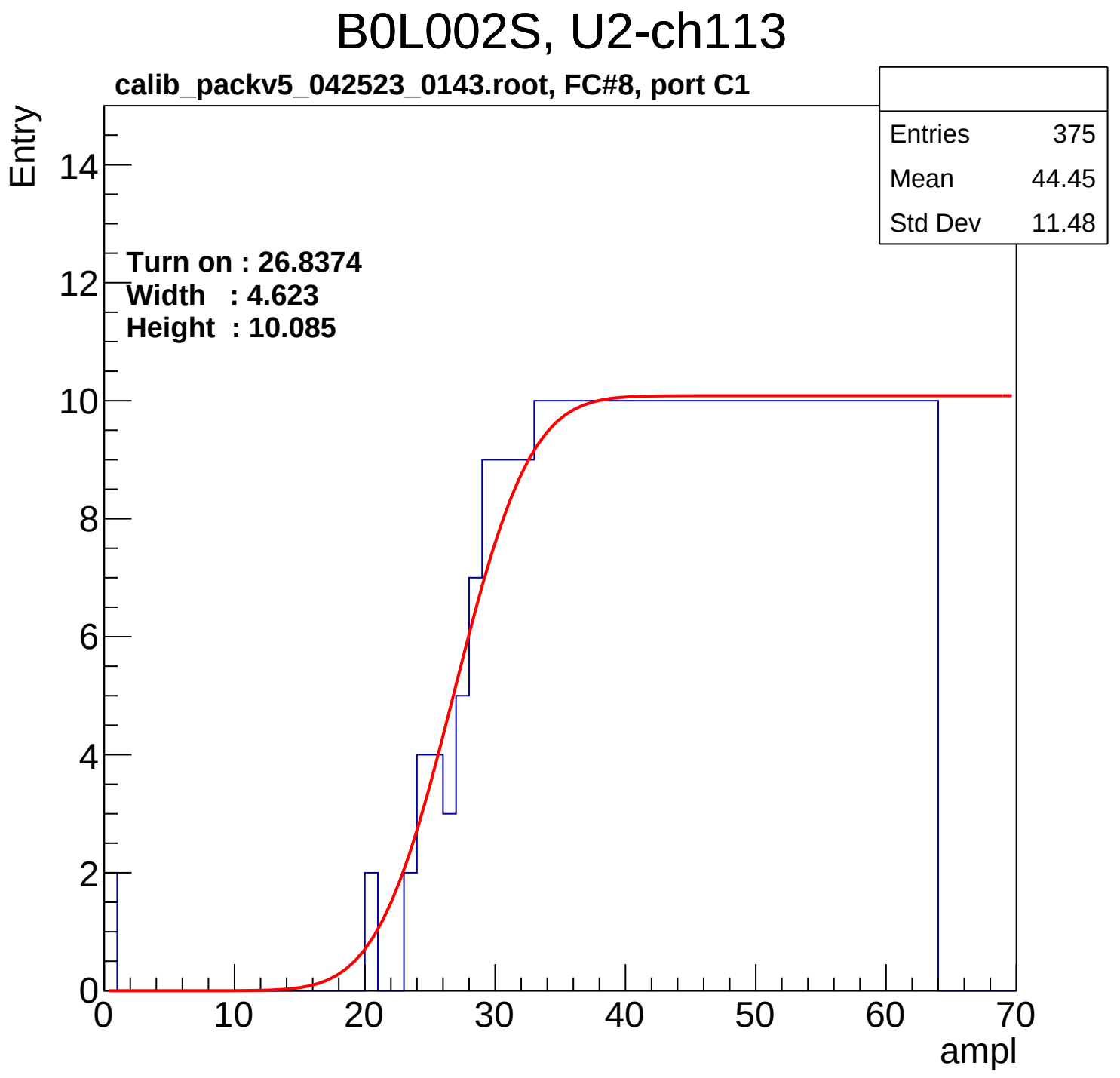
B0L002S, U2-ch113
calib_packv5_042523_0143.root, FC#8, port C1
Entries 375
Mean 44.45
Std Dev 11.48
Turn on : 26.8374
Width : 4.623
Height : 10.085
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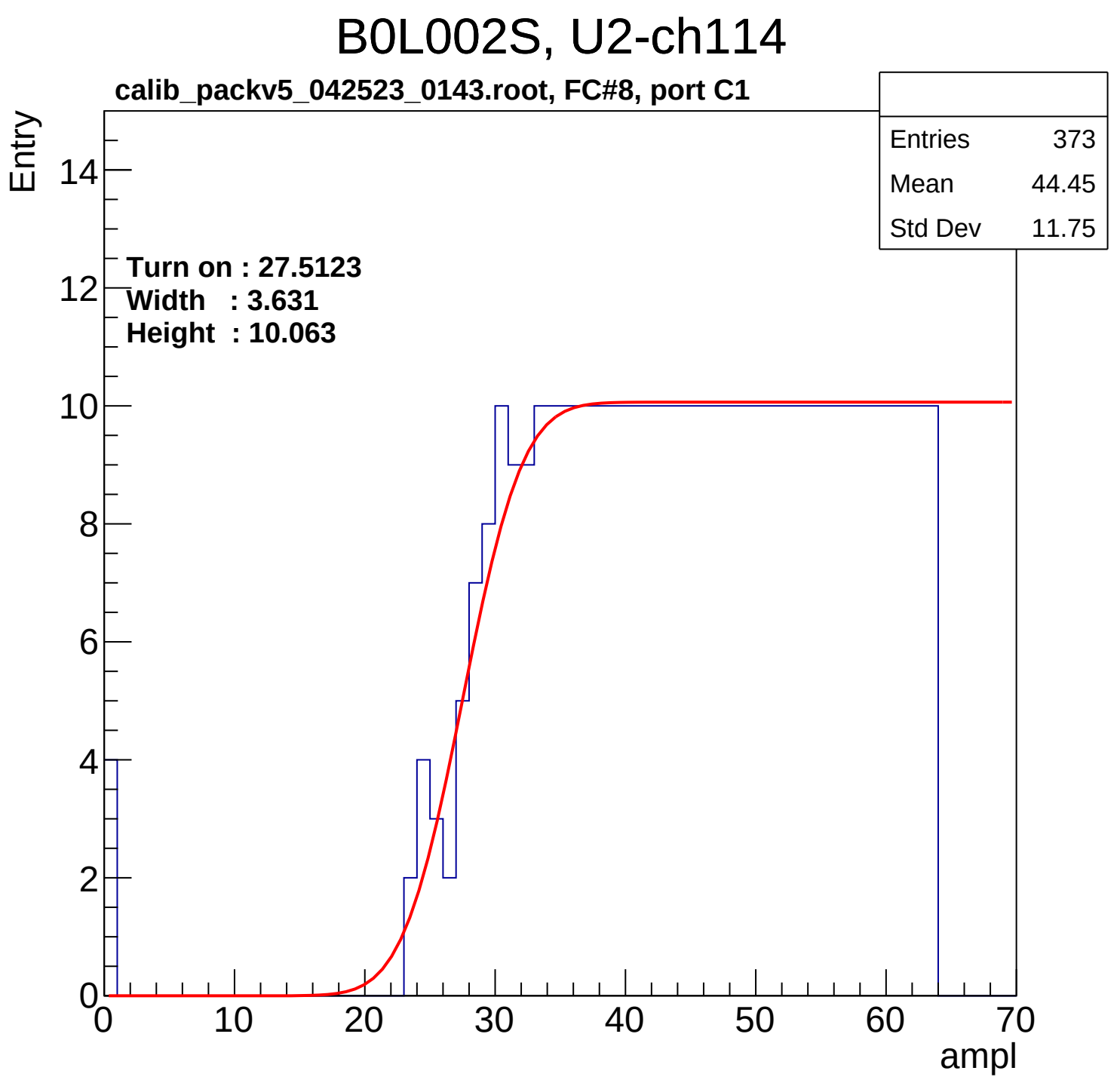
B0L002S, U2-ch114
calib_packv5_042523_0143.root, FC#8, port C1
Entries 373
Mean 44.45
Std Dev 11.75
Turn on : 27.5123
Width : 3.631
Height : 10.063
Entry
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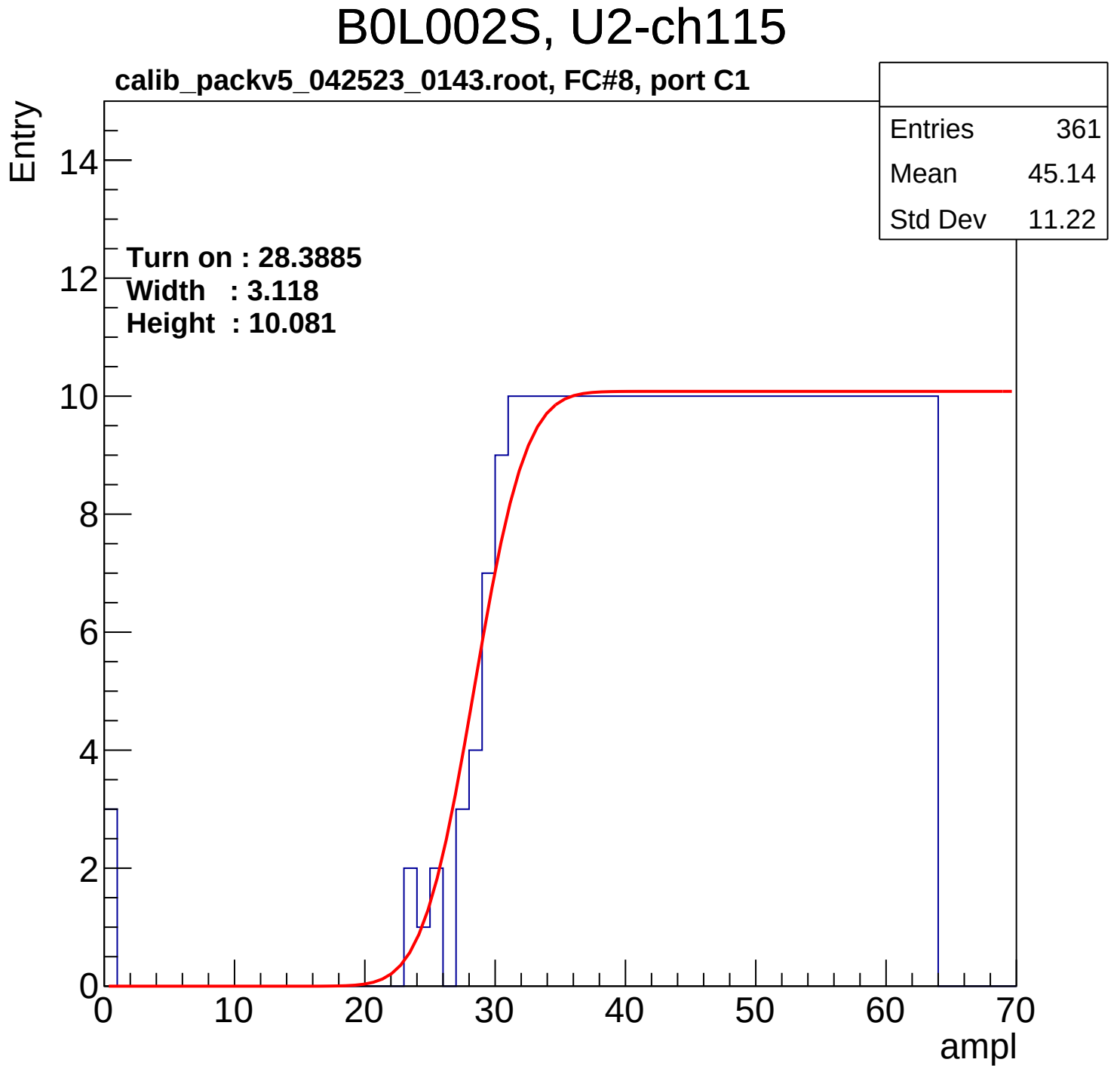
B0L002S, U2-ch115
calib_packv5_042523_0143.root, FC#8, port C1
Entries 361
Mean 45.14
Std Dev 11.22
Turn on : 28.3885
Width : 3.118
Height : 10.081
Entry
ampl
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4
6
8
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12
14
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10
20
30
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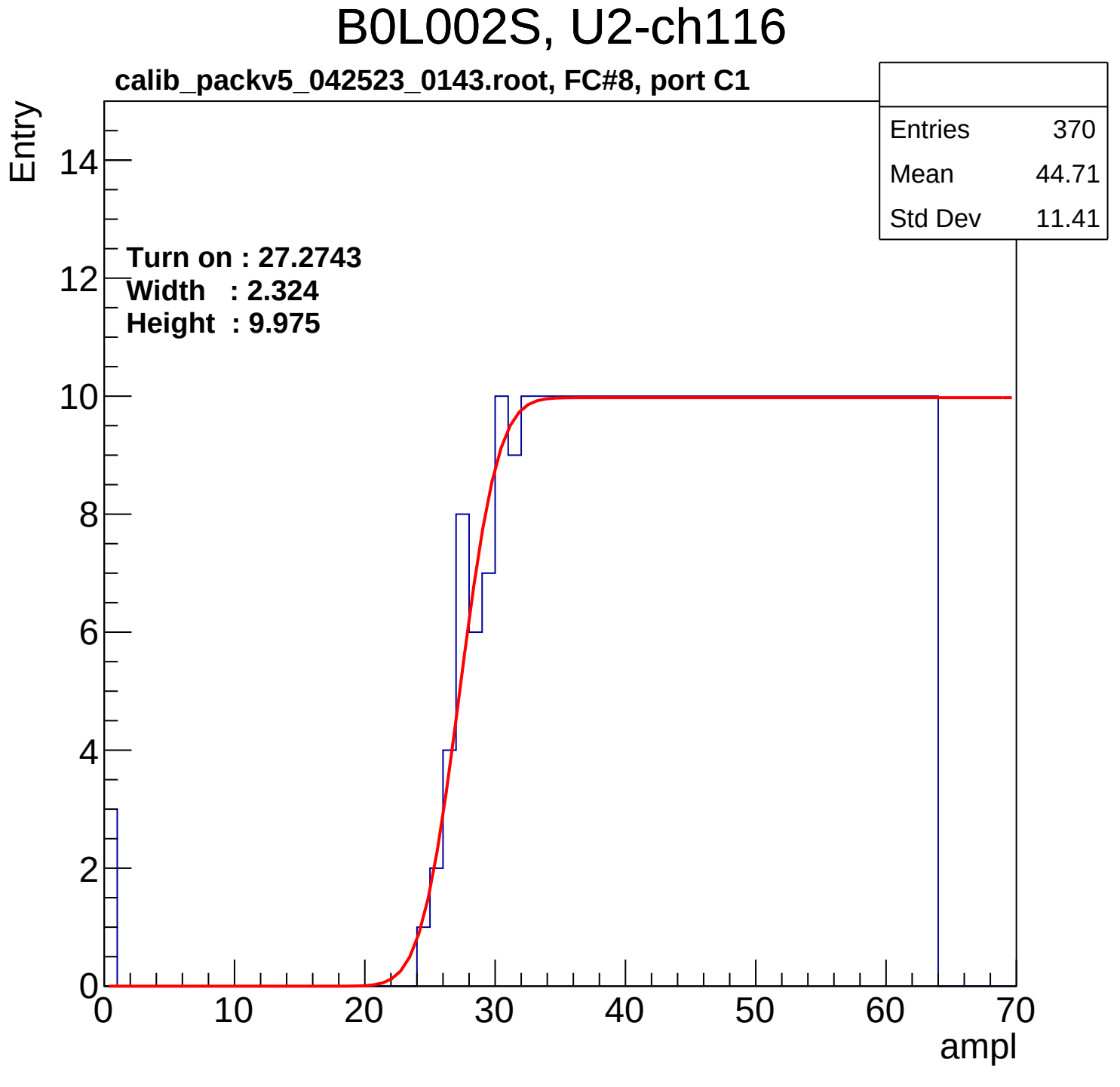
60
70


B0L002S, U2-ch116
calib_packv5_042523_0143.root, FC#8, port C1
Entries 370
Mean 44.71
Std Dev 11.41
Turn on : 27.2743
Width : 2.324
Height : 9.975
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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60
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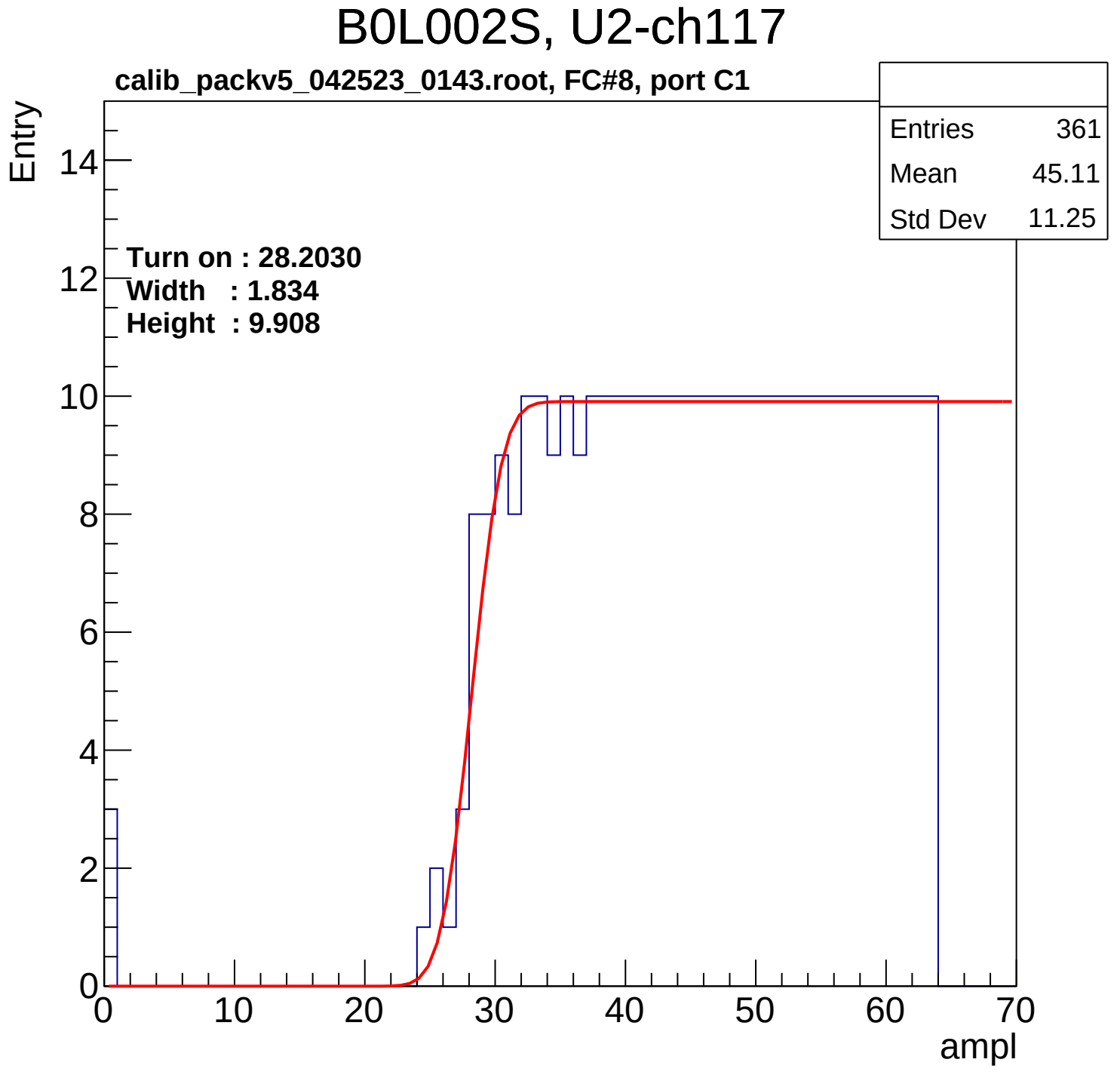
B0L002S, U2-ch117
calib_packv5_042523_0143.root, FC#8, port C1
Entries 361
Mean 45.11
Std Dev 11.25
Turn on : 28.2030
Width : 1.834
Height : 9.908
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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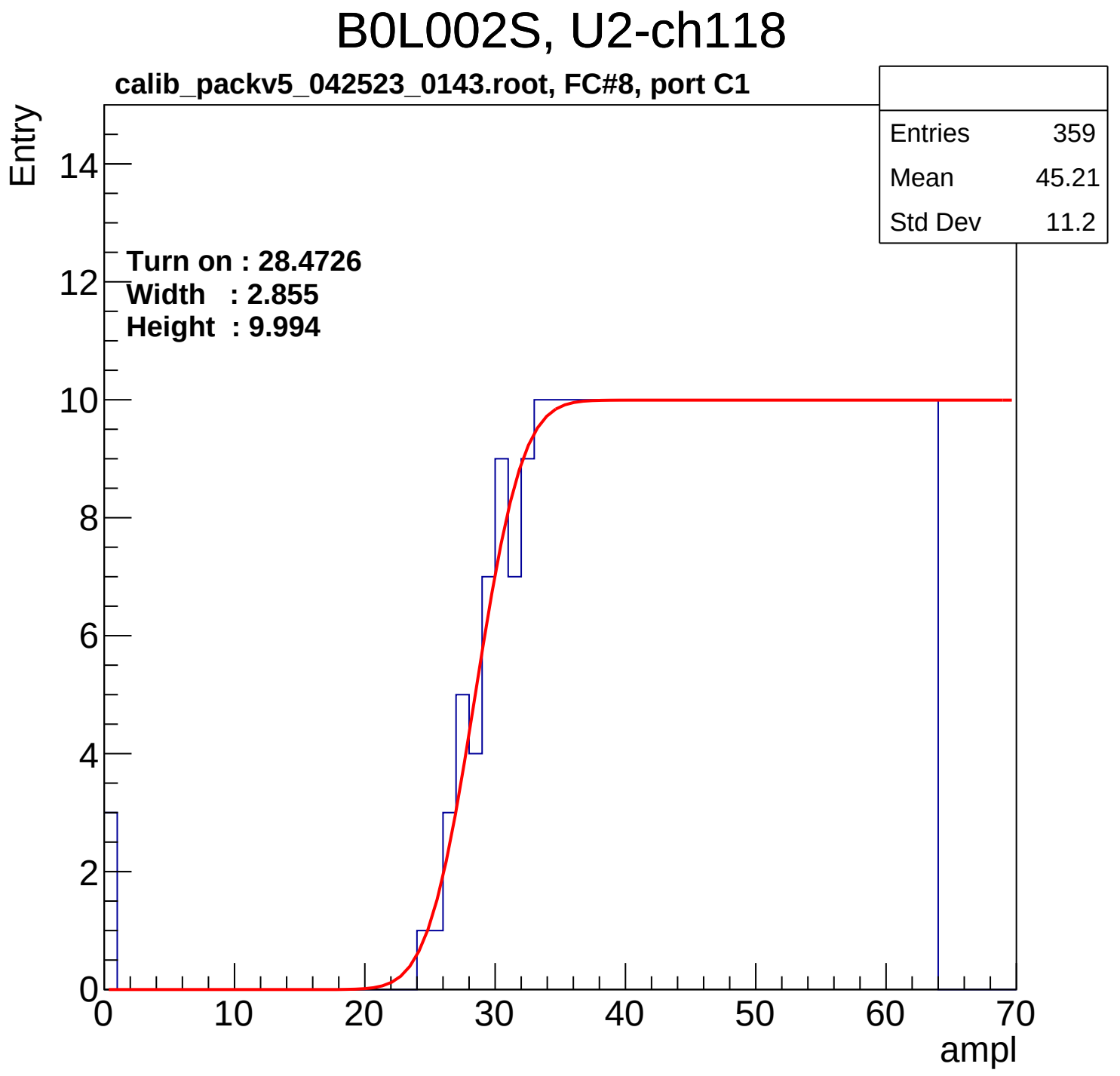
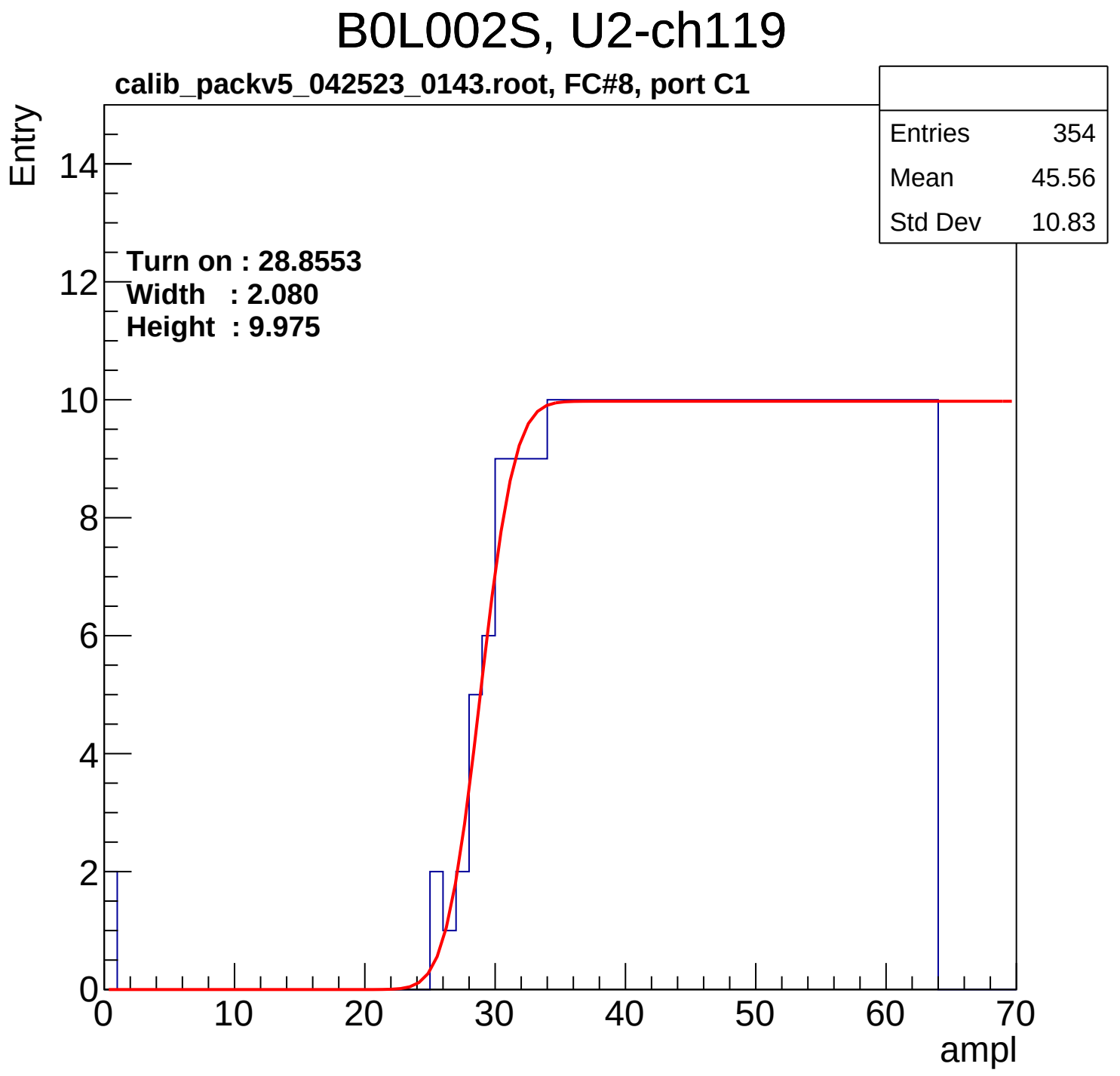
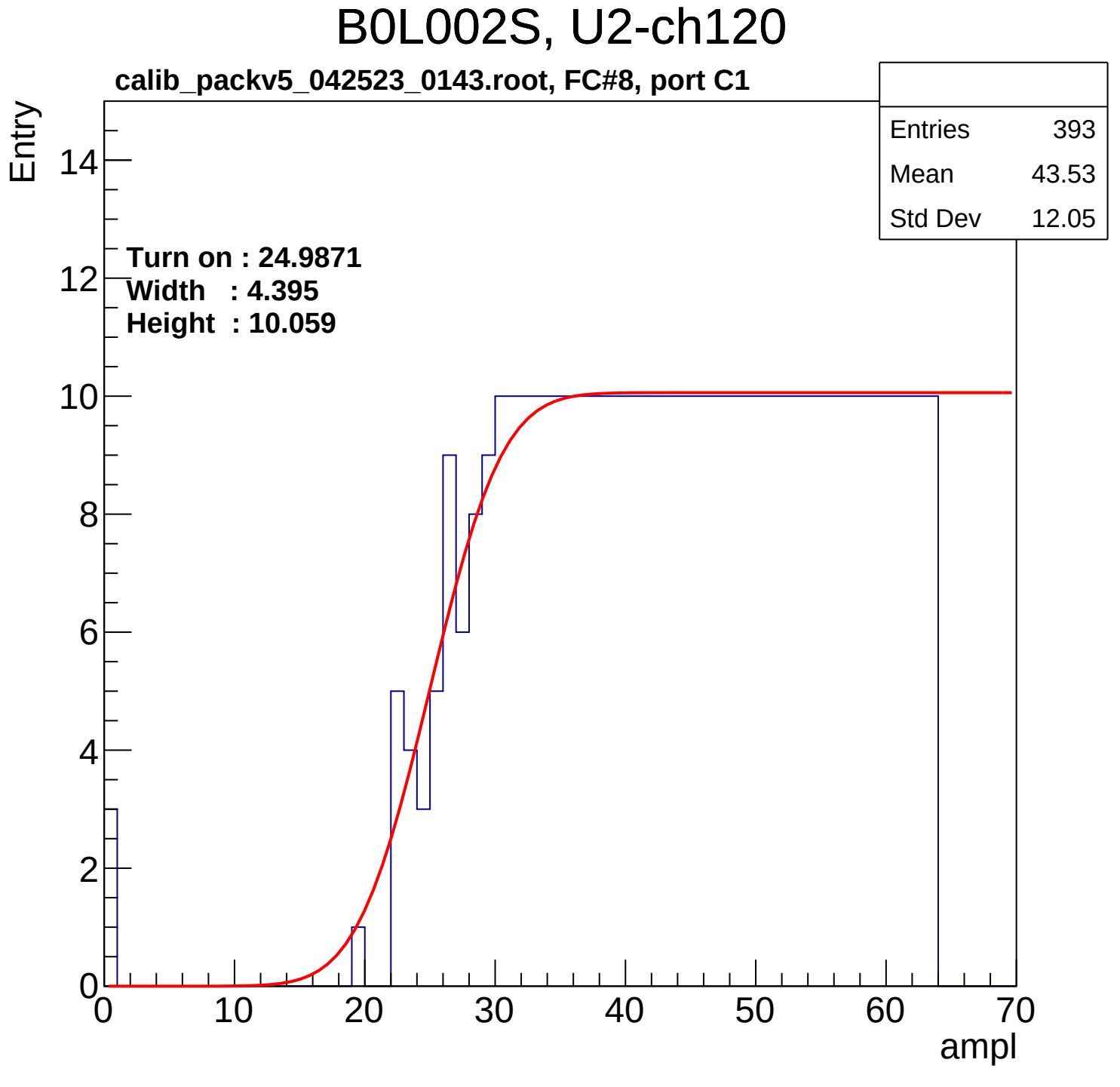
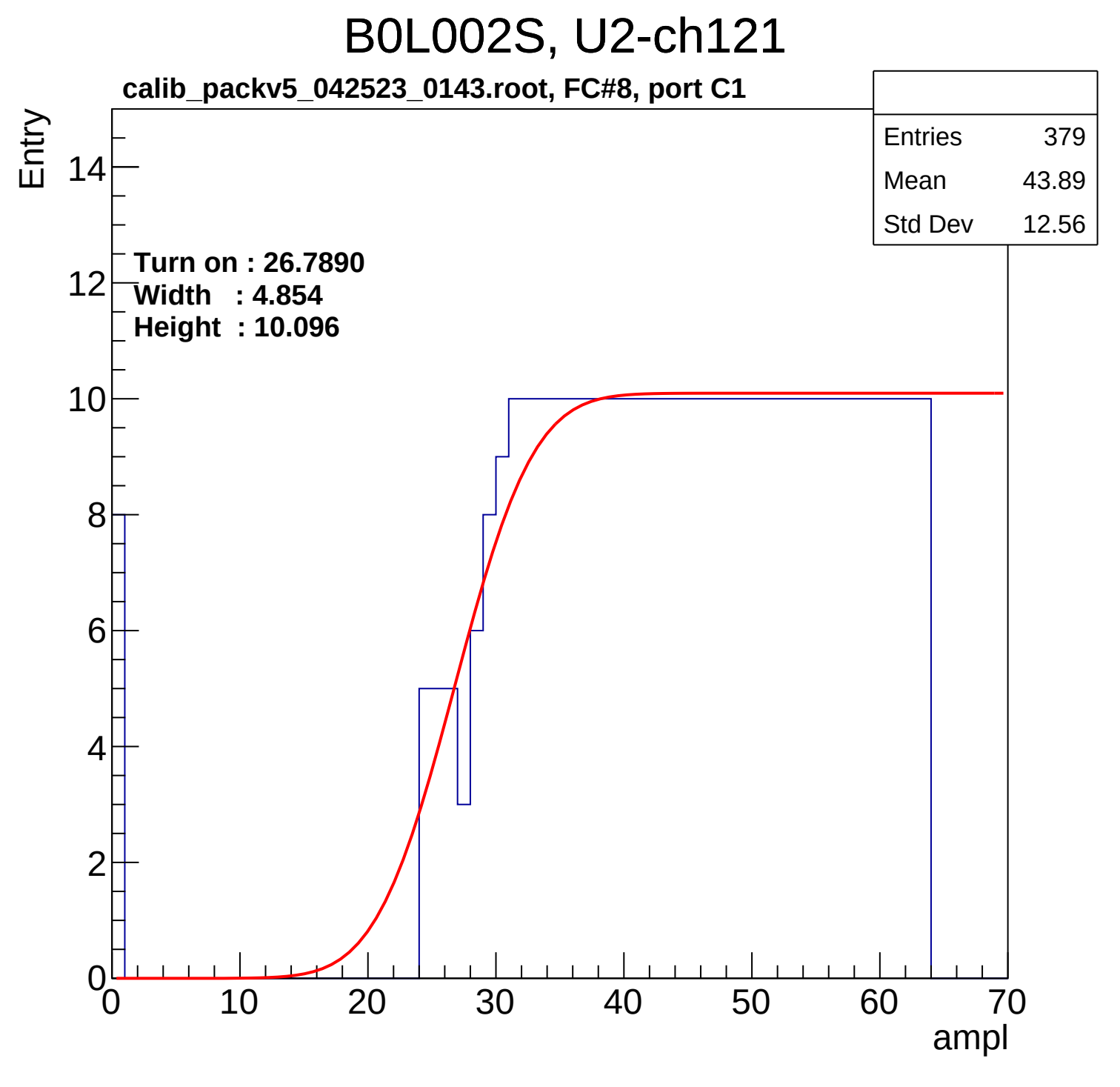
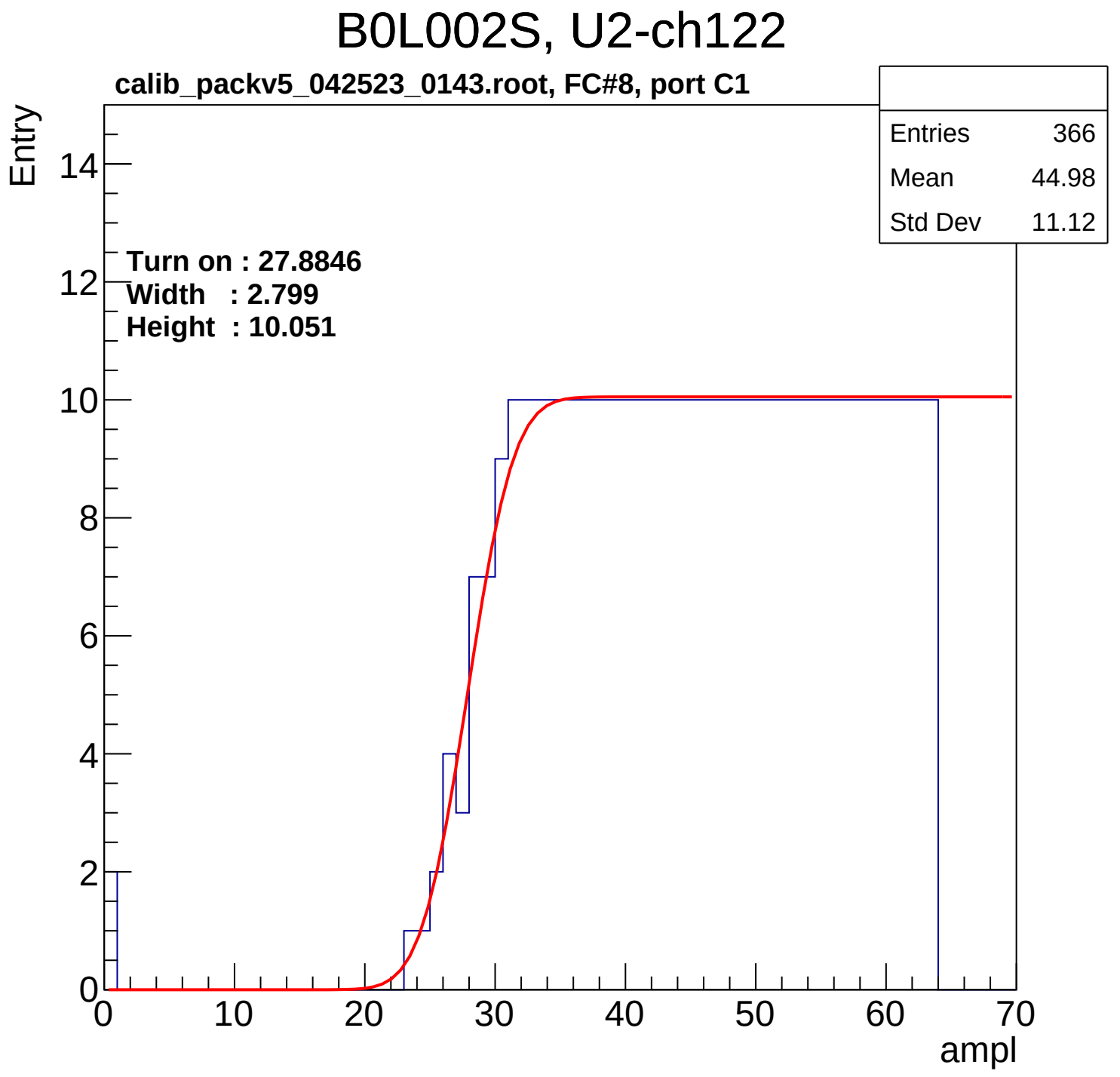
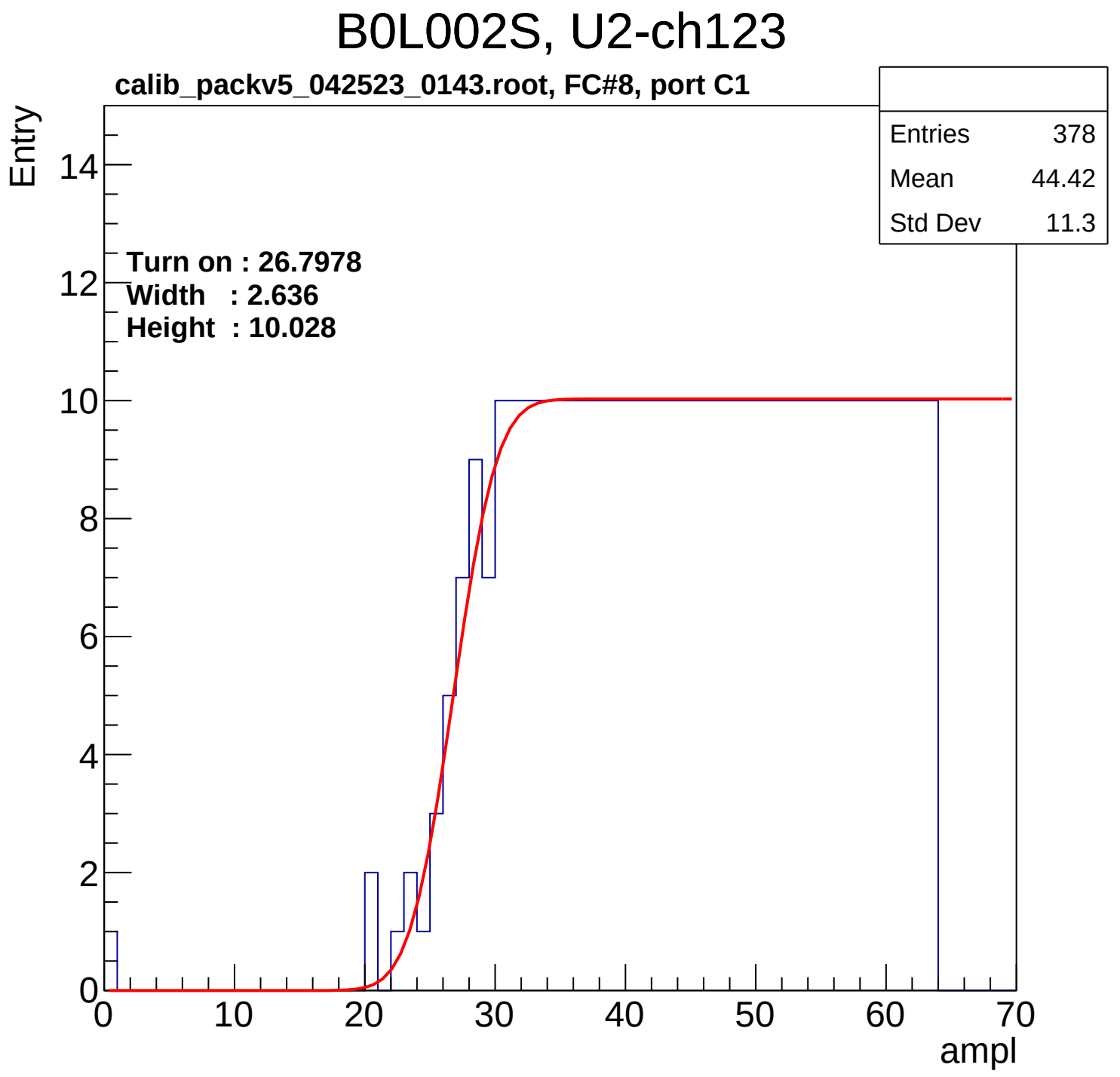

B0L002S, U2-ch118
calib_packv5_042523_0143.root, FC#8, port C1
Entries 359
Mean 45.21
Std Dev 11.2
Turn on : 28.4726
Width : 2.855
Height : 9.994
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

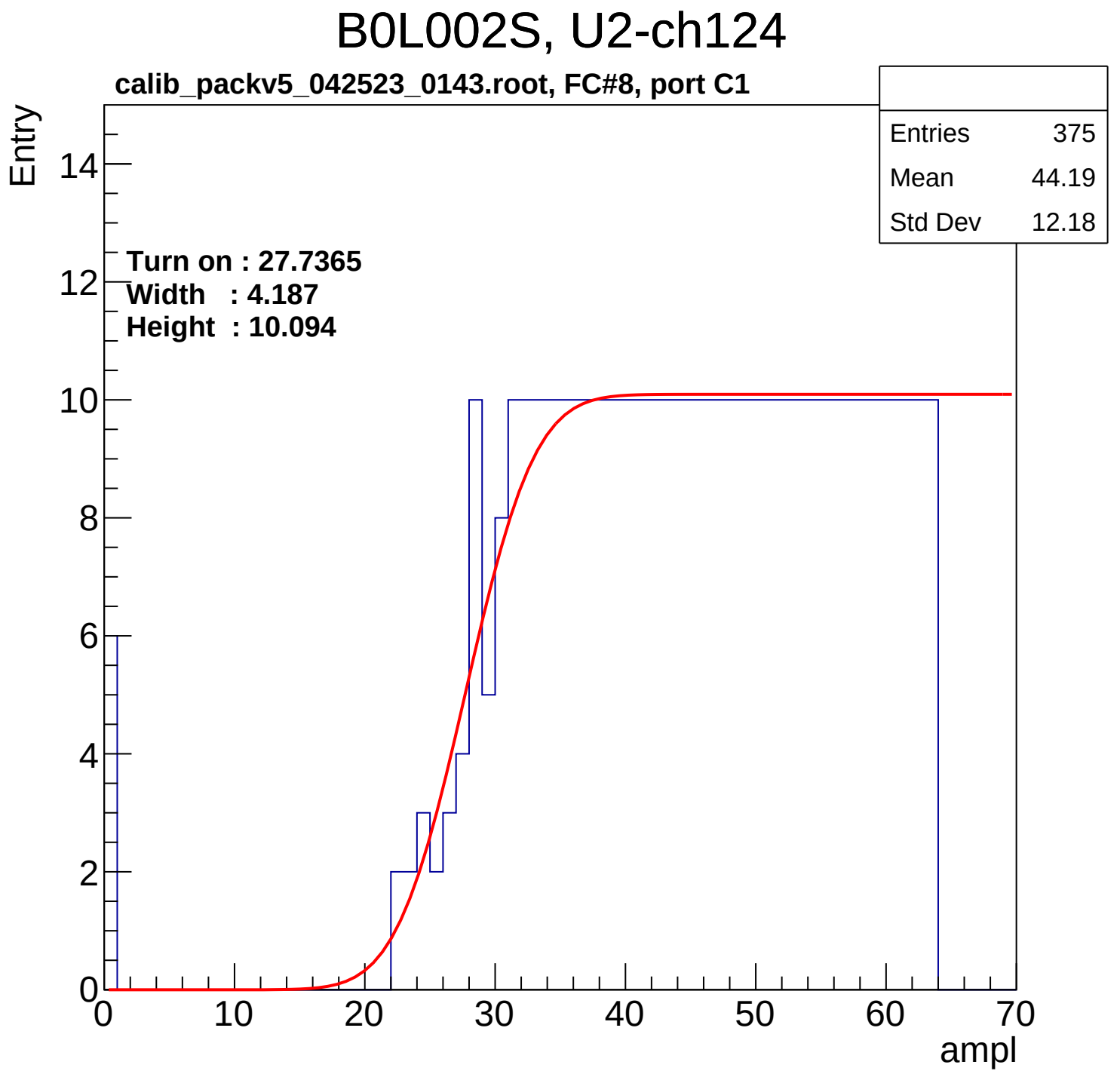

B0L002S, U2-ch119
calib_packv5_042523_0143.root, FC#8, port C1
Entries 354
Mean 45.56
Std Dev 10.83
Turn on : 28.8553
Width : 2.080
Height : 9.975
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

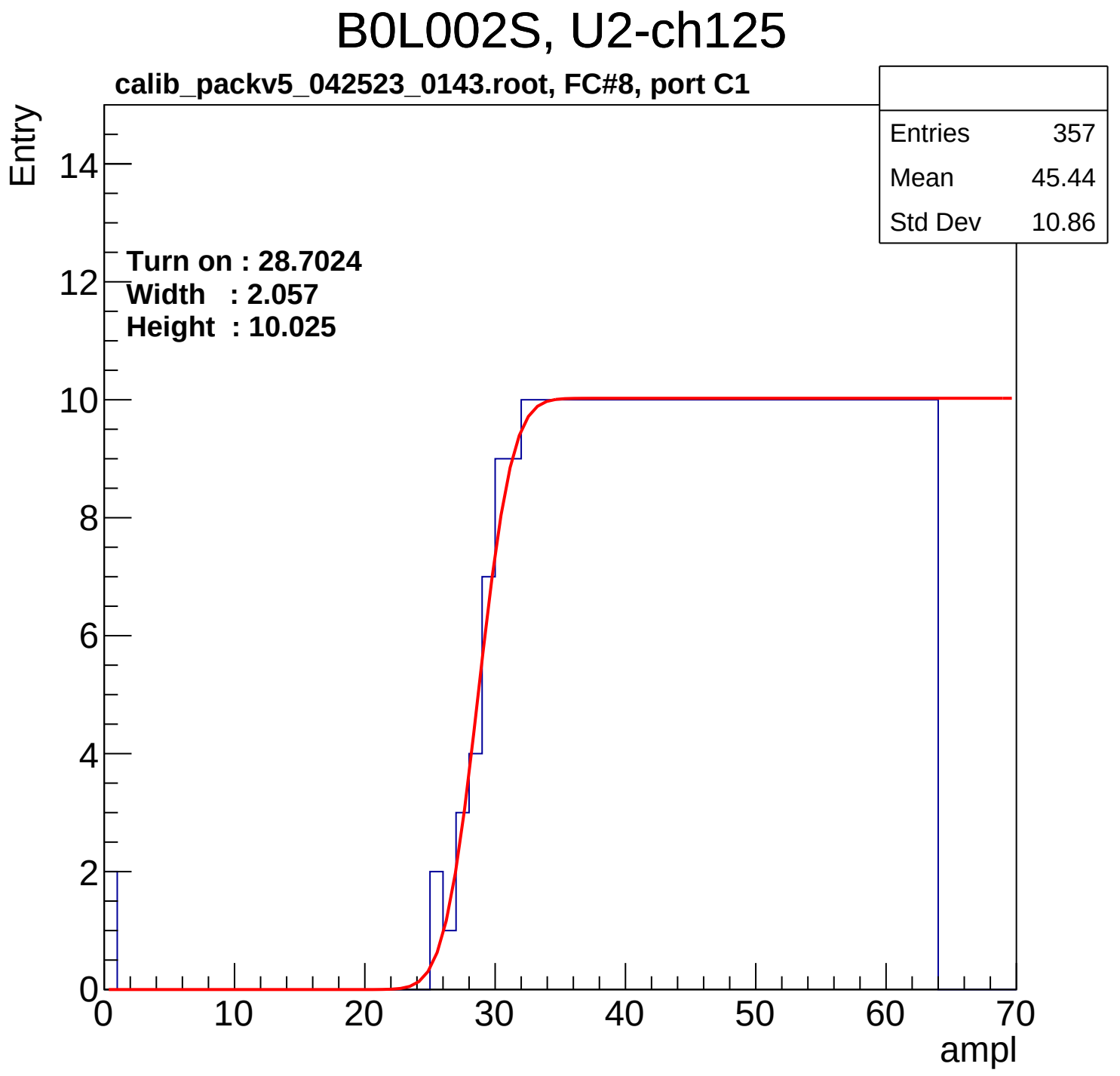

B0L002S, U2-ch120
calib_packv5_042523_0143.root, FC#8, port C1
Entries 393
Mean 43.53
Std Dev 12.05
Turn on : 24.9871
Width : 4.395
Height : 10.059
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

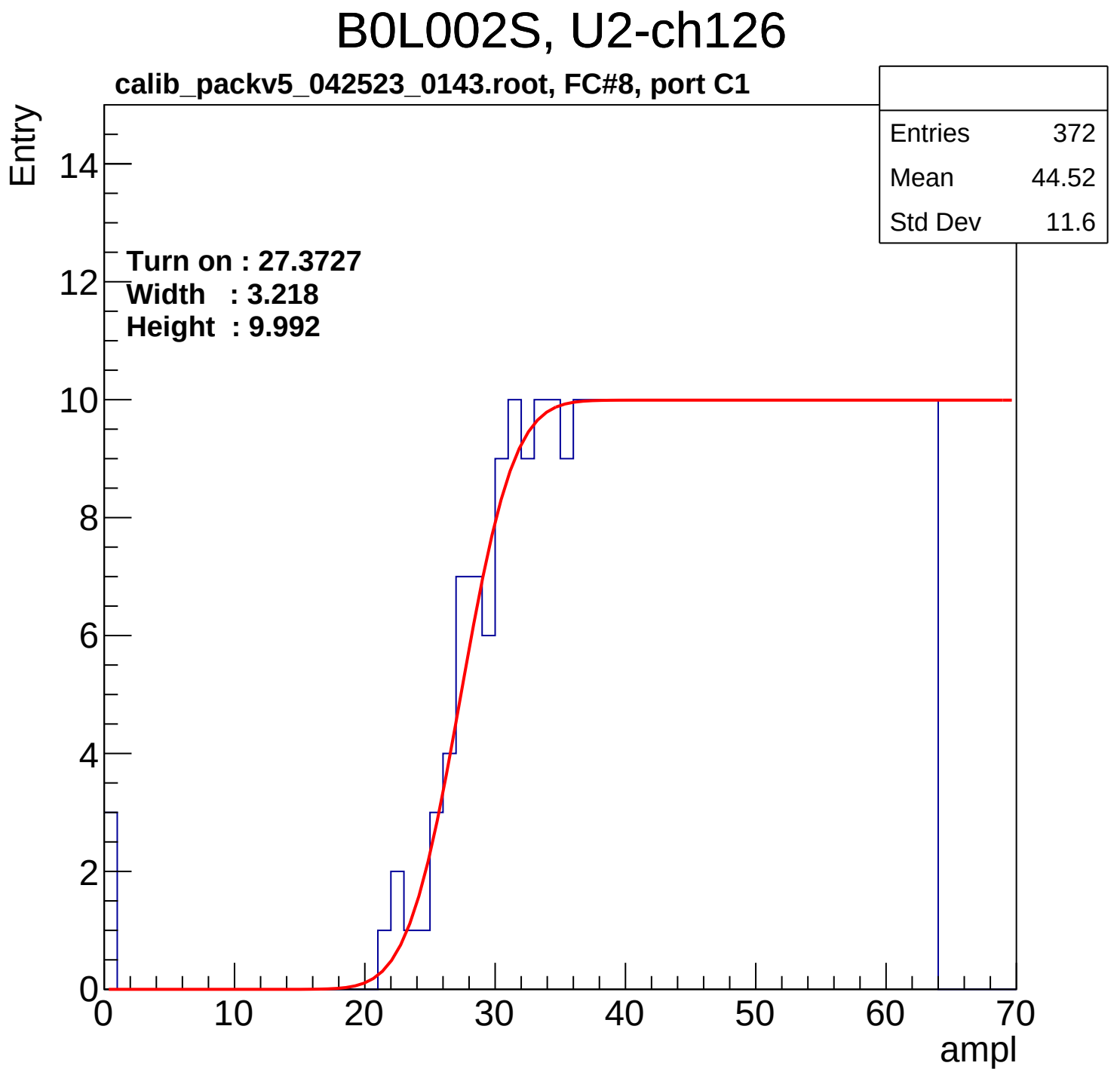

B0L002S, U2-ch121
calib_packv5_042523_0143.root, FC#8, port C1
Entries 379
Mean 43.89
Std Dev 12.56
Turn on : 26.7890
Width : 4.854
Height : 10.096
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

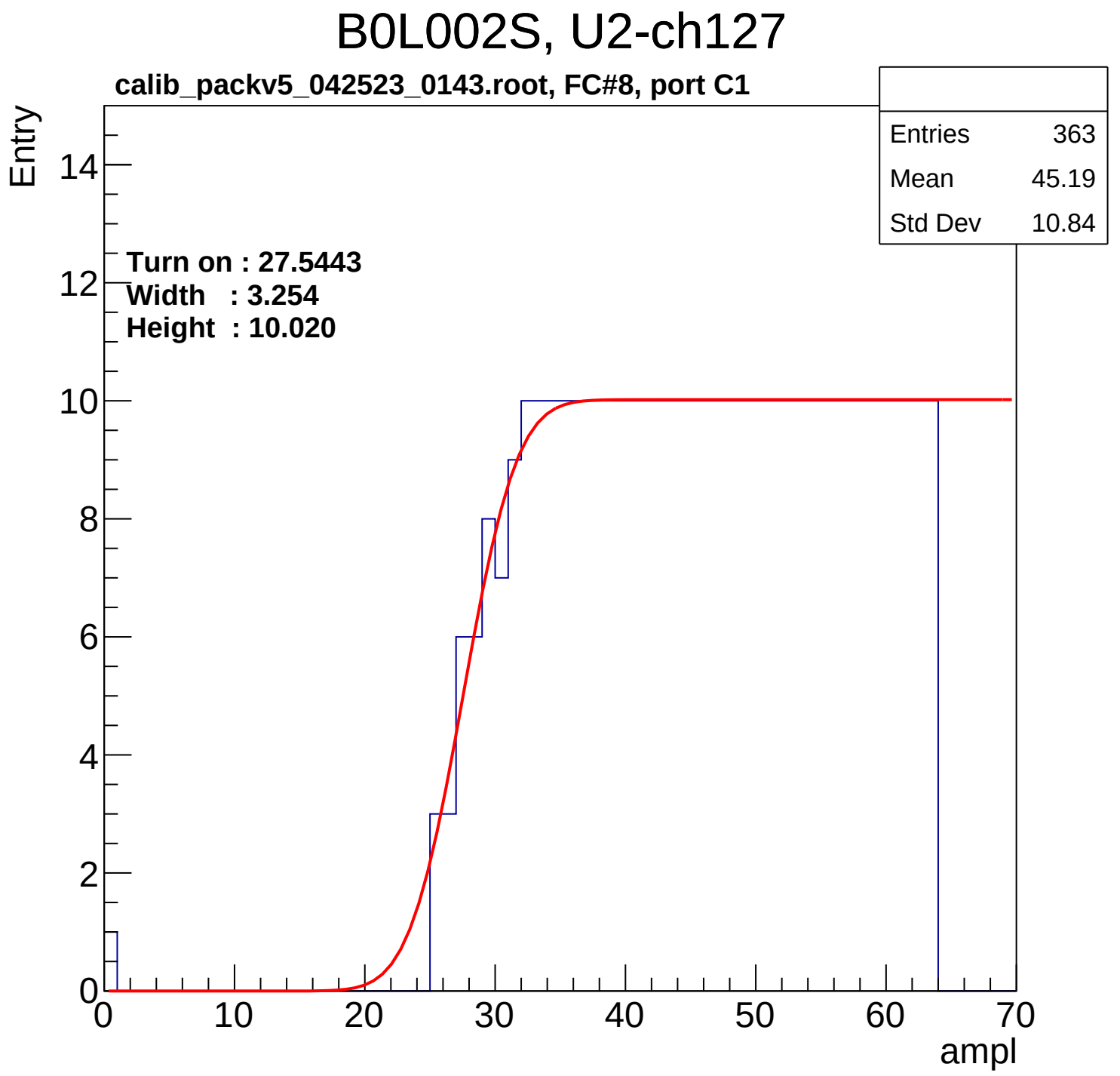

B0L002S, U2-ch122
calib_packv5_042523_0143.root, FC#8, port C1
Entries 366
Mean 44.98
Std Dev 11.12
Turn on : 27.8846
Width : 2.799
Height : 10.051
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

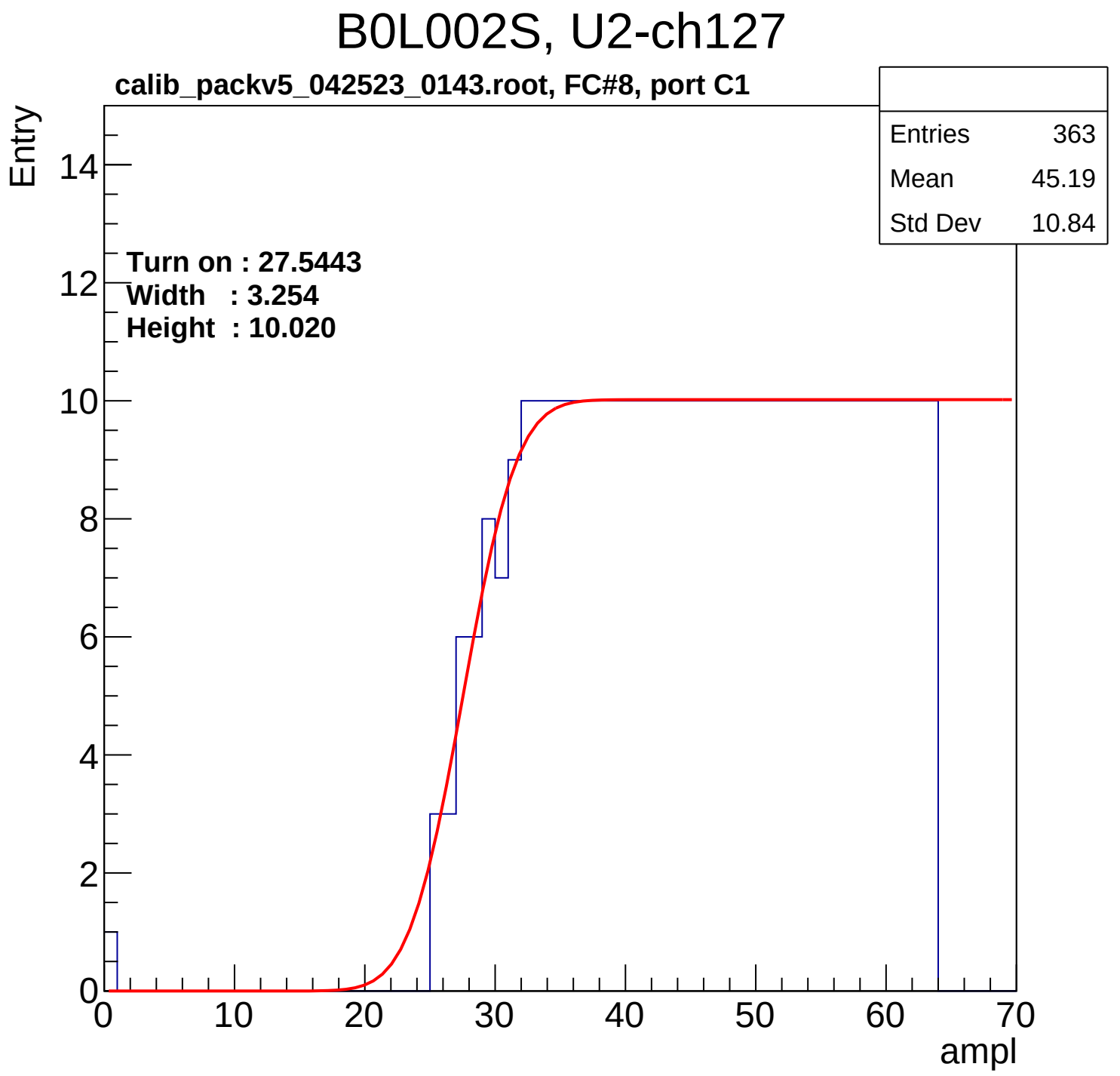

B0L002S, U2-ch123
calib_packv5_042523_0143.root, FC#8, port C1
Entries 378
Mean 44.42
Std Dev 11.3
Turn on : 26.7978
Width : 2.636
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L002S, U2-ch124
calib_packv5_042523_0143.root, FC#8, port C1
Entries 375
Mean 44.19
Std Dev 12.18
Turn on : 27.7365
Width : 4.187
Height : 10.094
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L002S, U2-ch125
calib_packv5_042523_0143.root, FC#8, port C1
Entries 357
Mean 45.44
Std Dev 10.86
Turn on : 28.7024
Width : 2.057
Height : 10.025
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L002S, U2-ch126
calib_packv5_042523_0143.root, FC#8, port C1
Entries 372
Mean 44.52
Std Dev 11.6
Turn on : 27.3727
Width : 3.218
Height : 9.992
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L002S, U2-ch127
calib_packv5_042523_0143.root, FC#8, port C1
Entries 363
Mean 45.19
Std Dev 10.84
Turn on : 27.5443
Width : 3.254
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L002S, U2-ch127
calib_packv5_042523_0143.root, FC#8, port C1
Entries 363
Mean 45.19
Std Dev 10.84
Turn on : 27.5443
Width : 3.254
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70