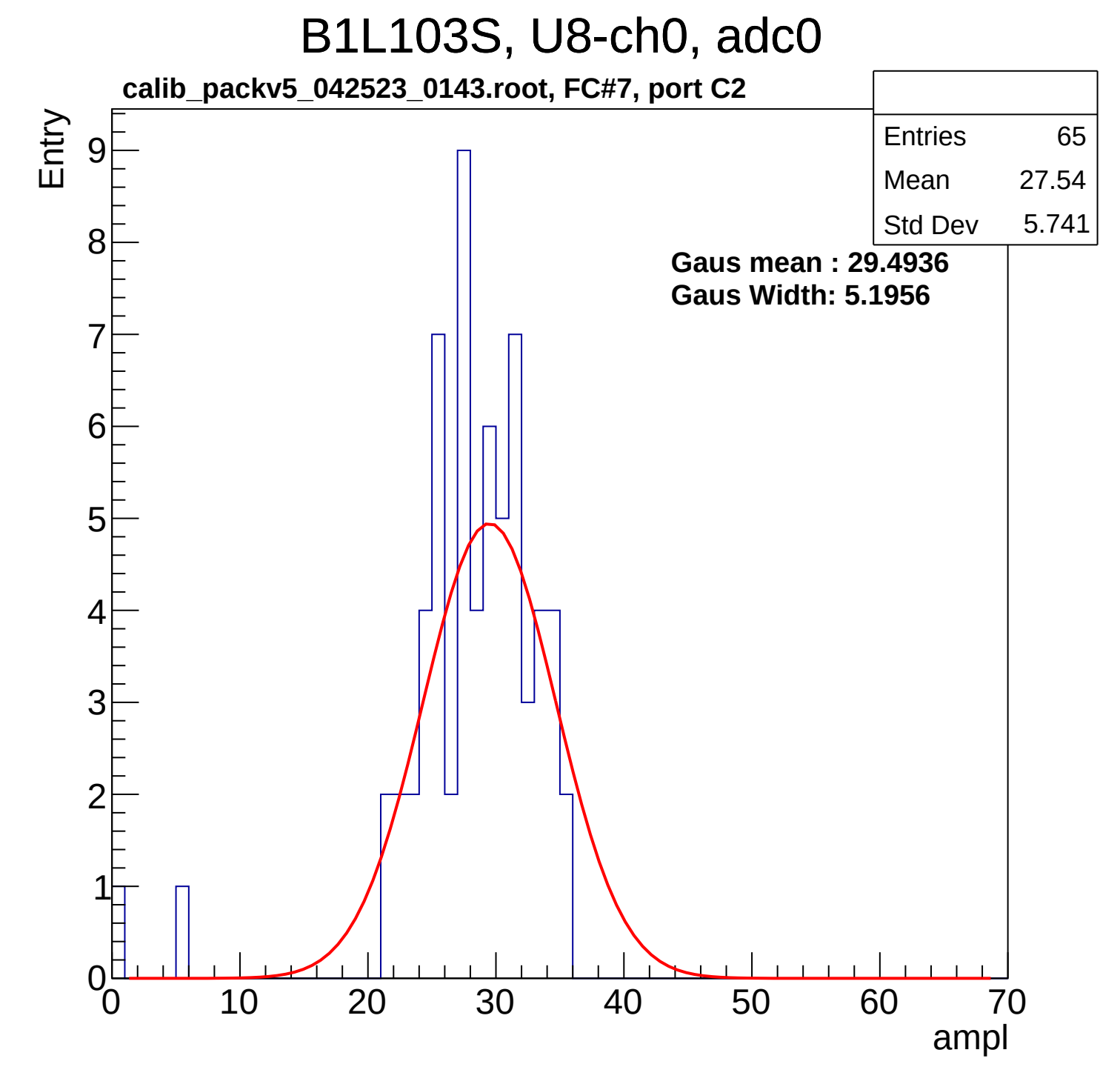
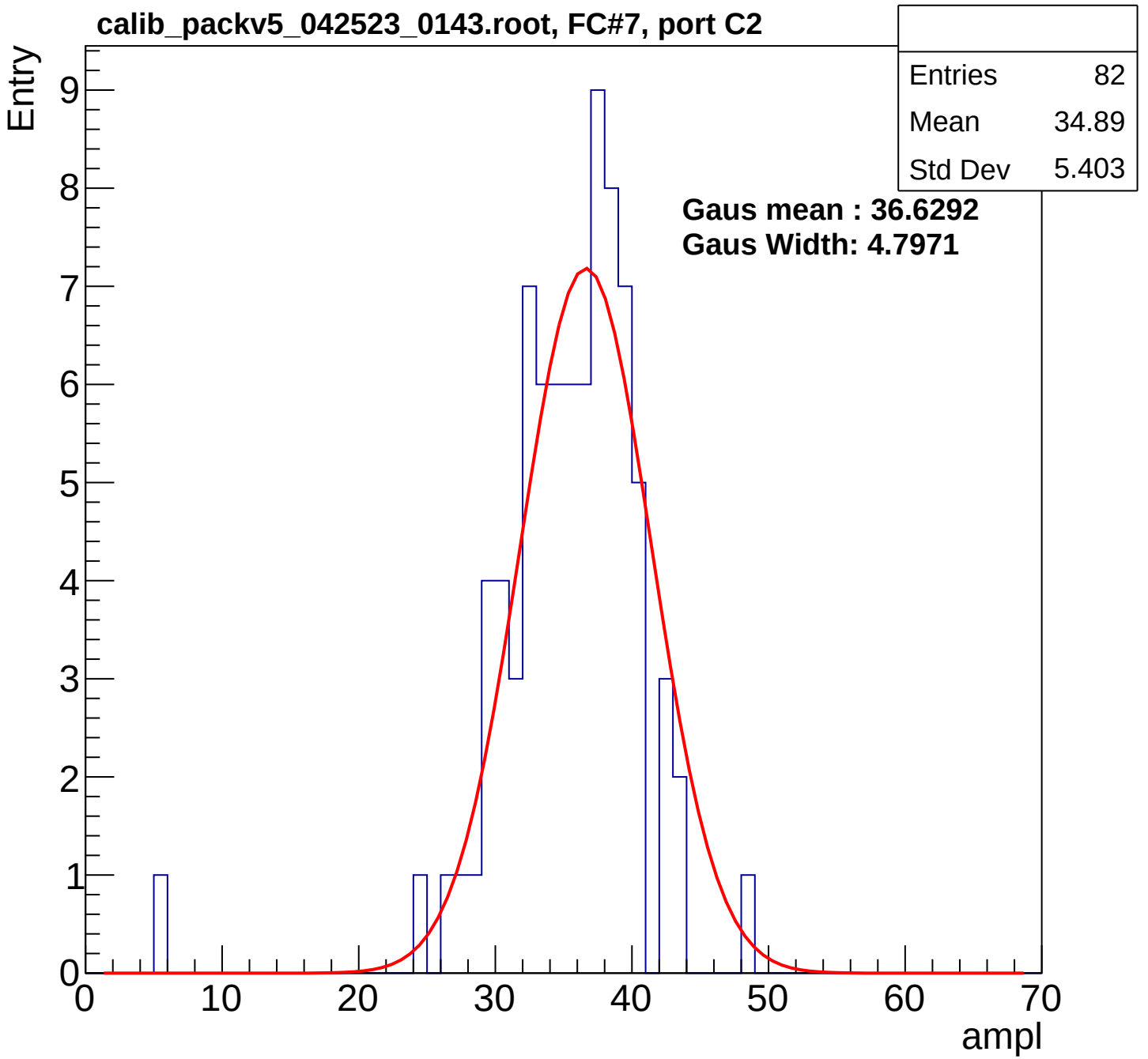
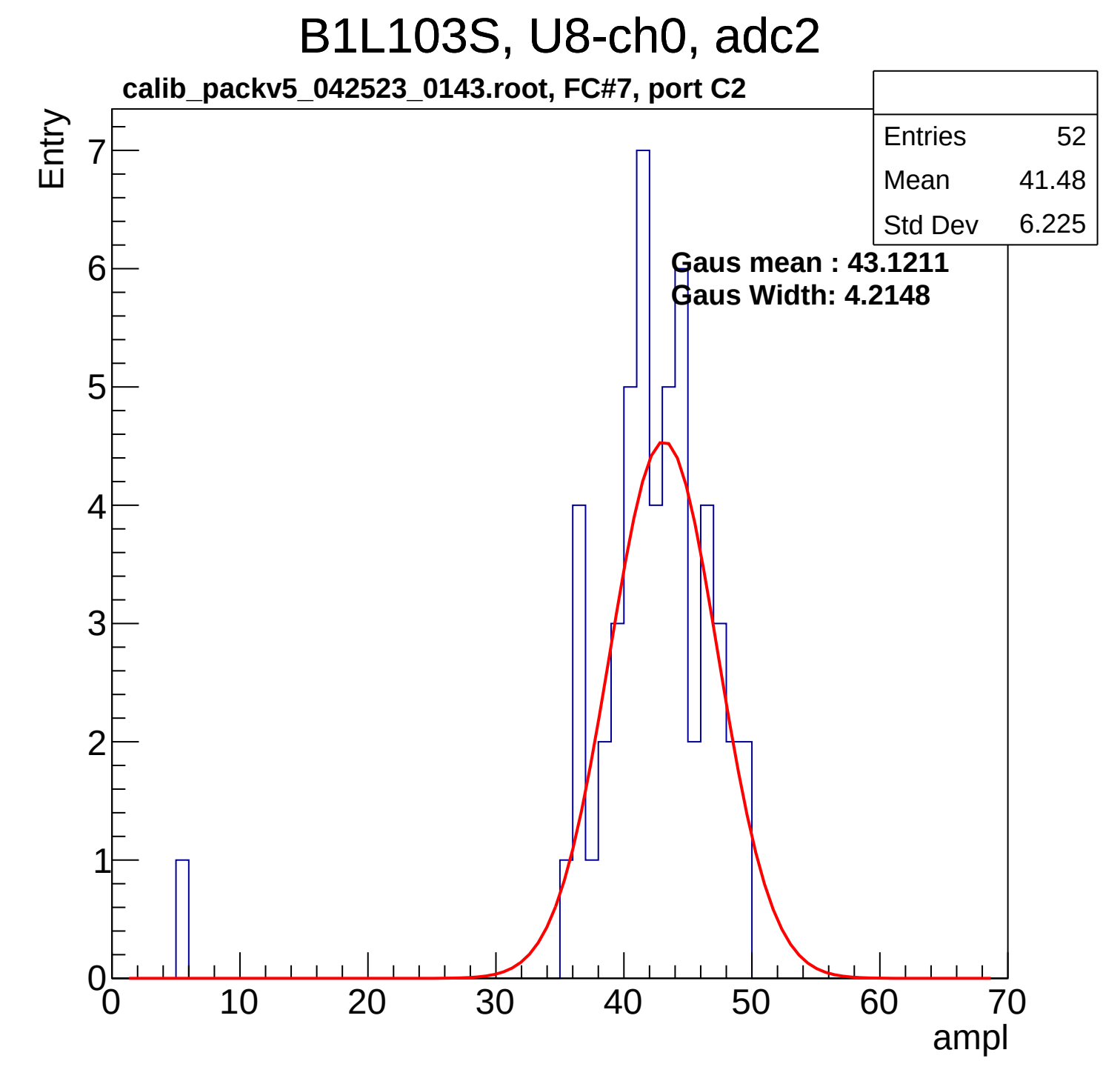
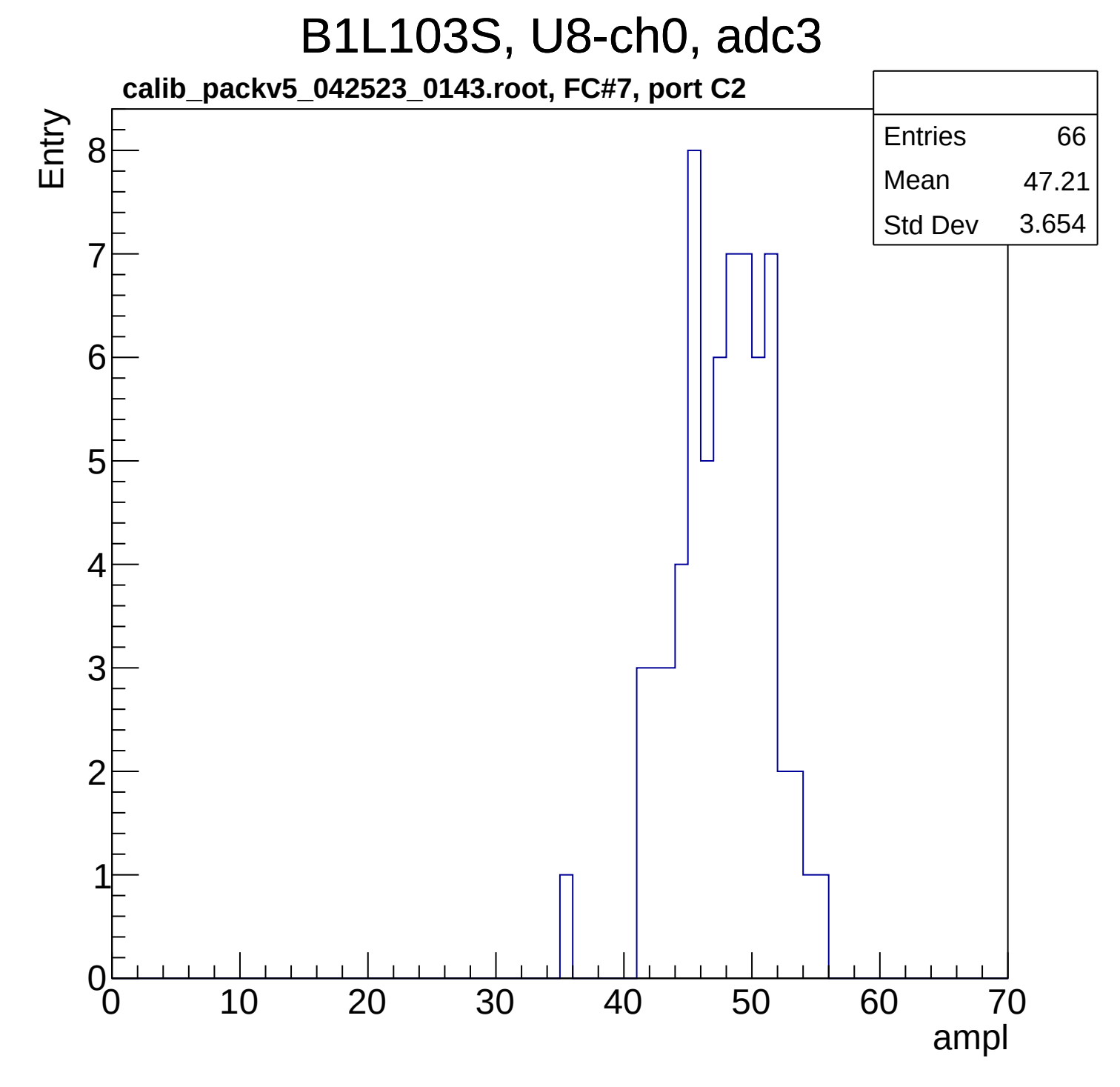
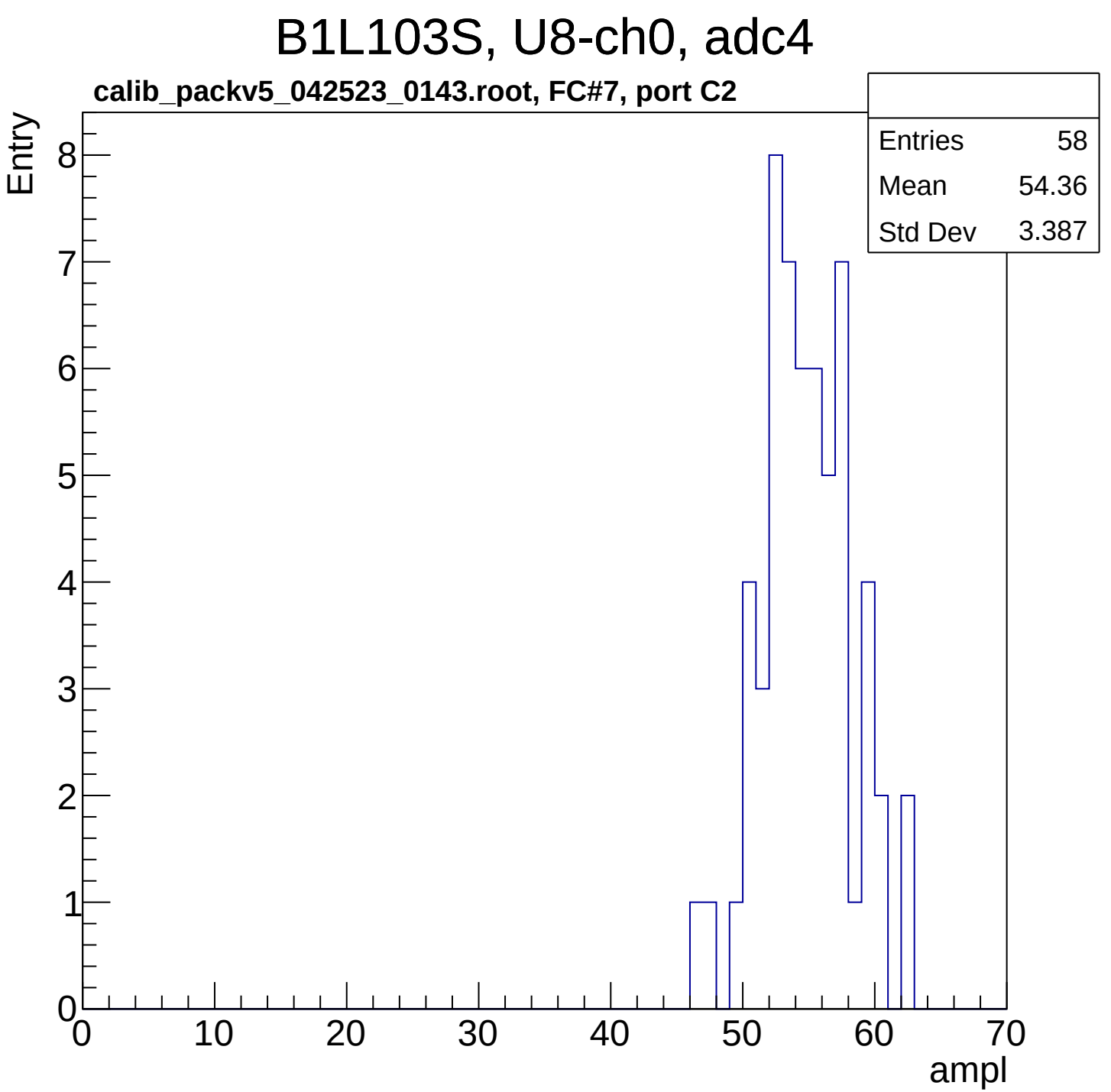
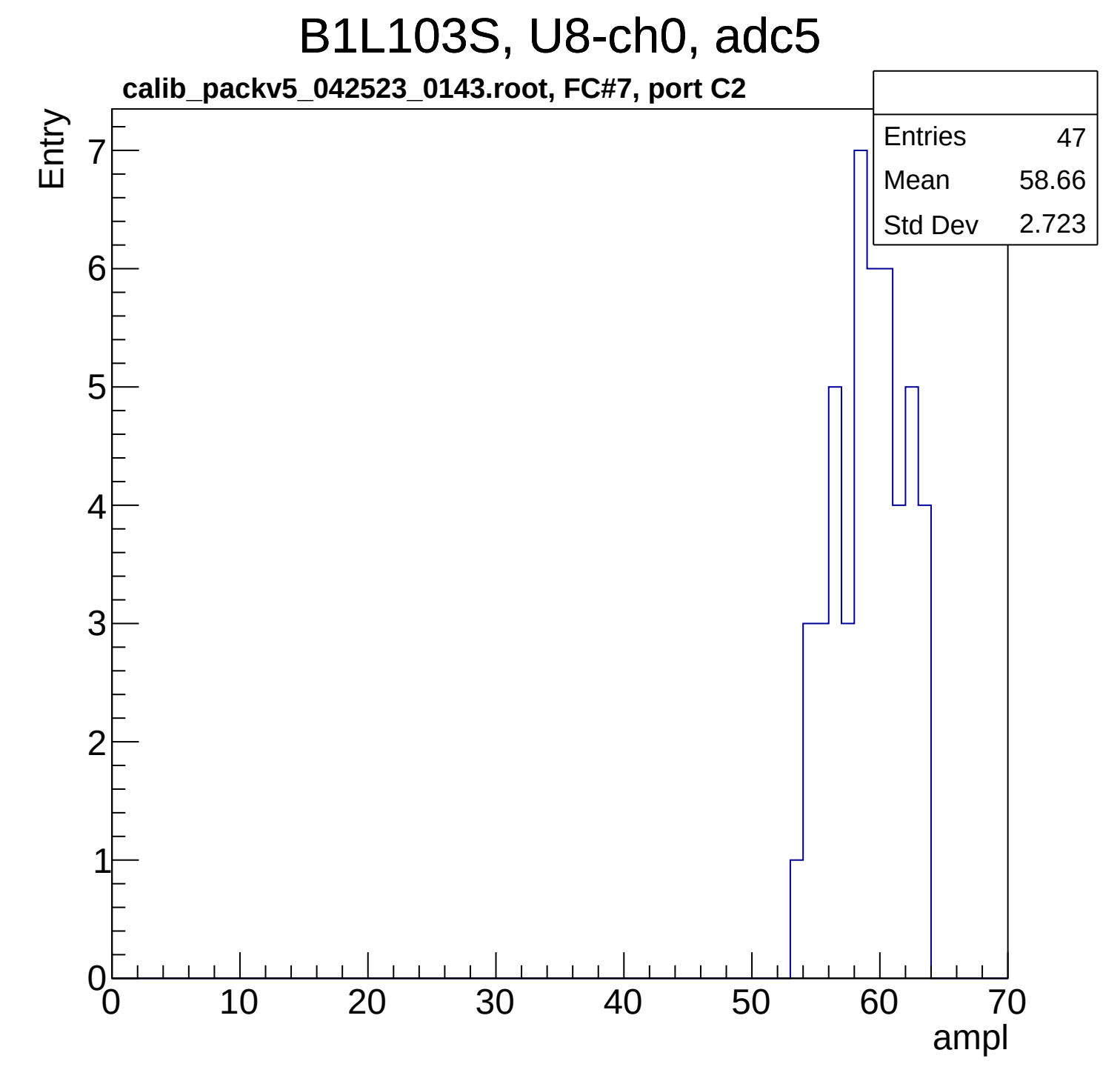

B1L103S, U8-ch0, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 27.54
Std Dev 5.741
Gaus mean : 29.4936
Gaus Width: 5.1956
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

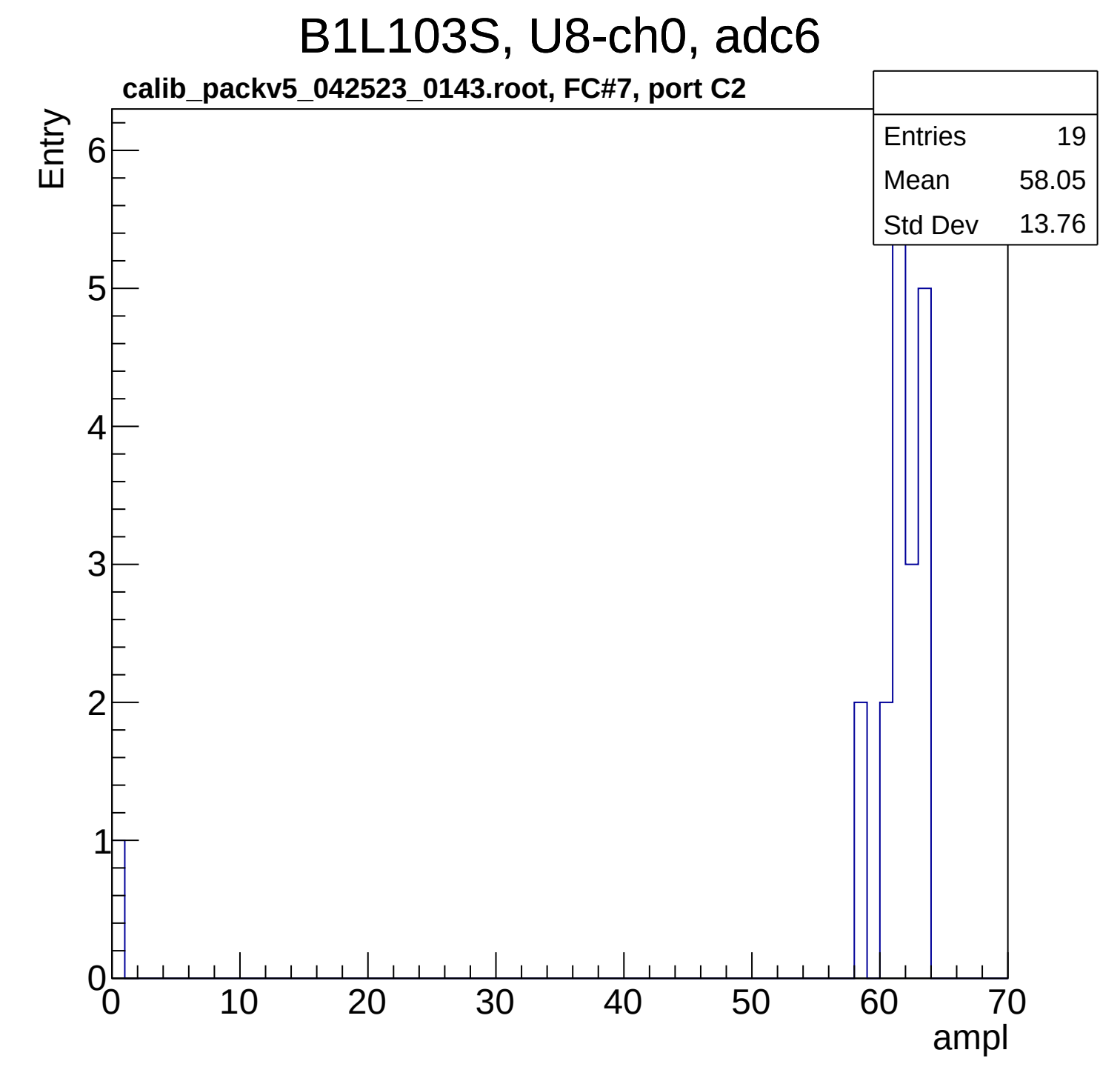

B1L103S, U8-ch0, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 82
Mean 34.89
Std Dev 5.403
Gaus mean : 36.6292
Gaus Width: 4.7971
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

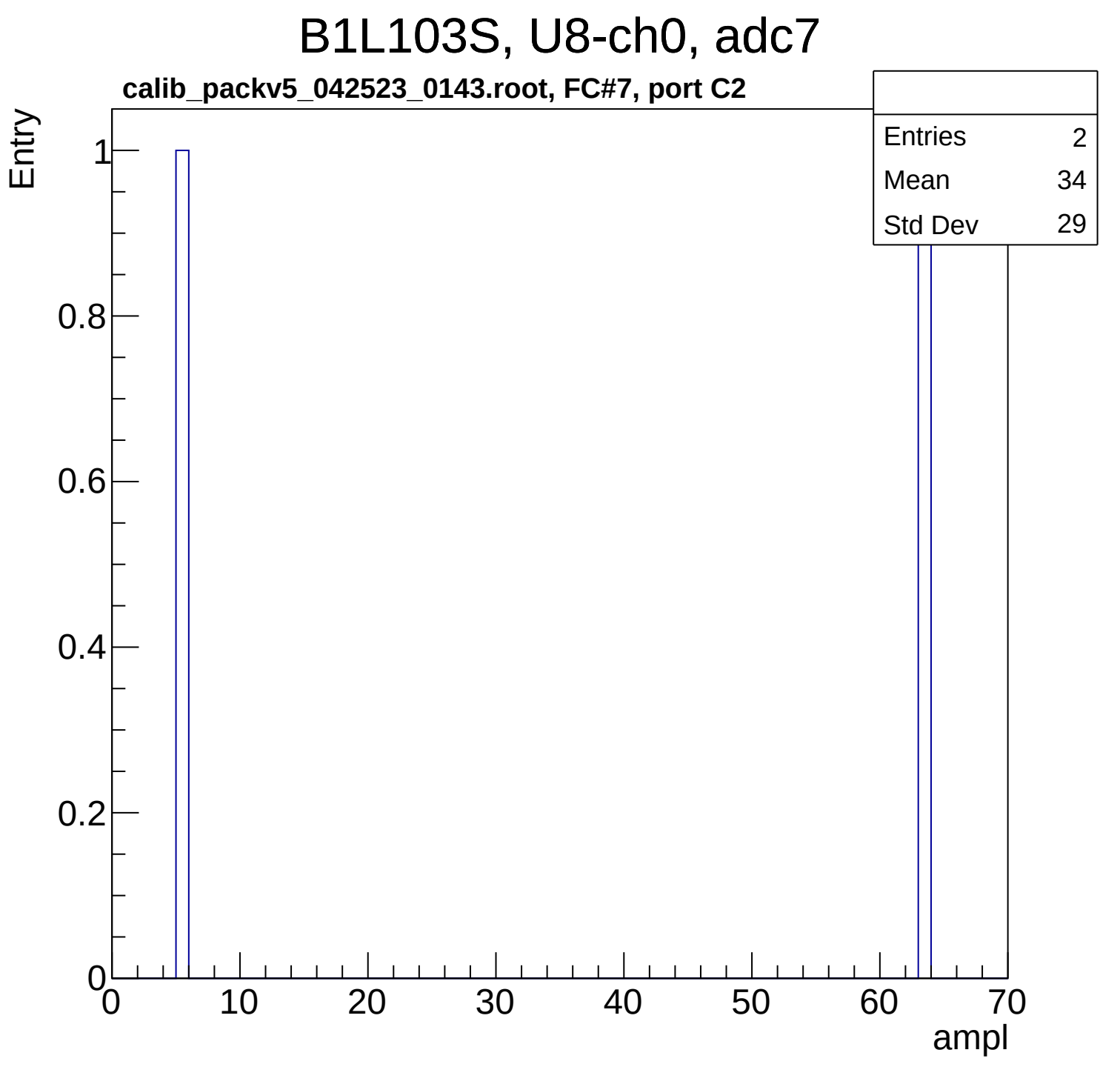

B1L103S, U8-ch0, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 41.48
Std Dev 6.225
Gaus mean : 43.1211
Gaus Width: 4.2148
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

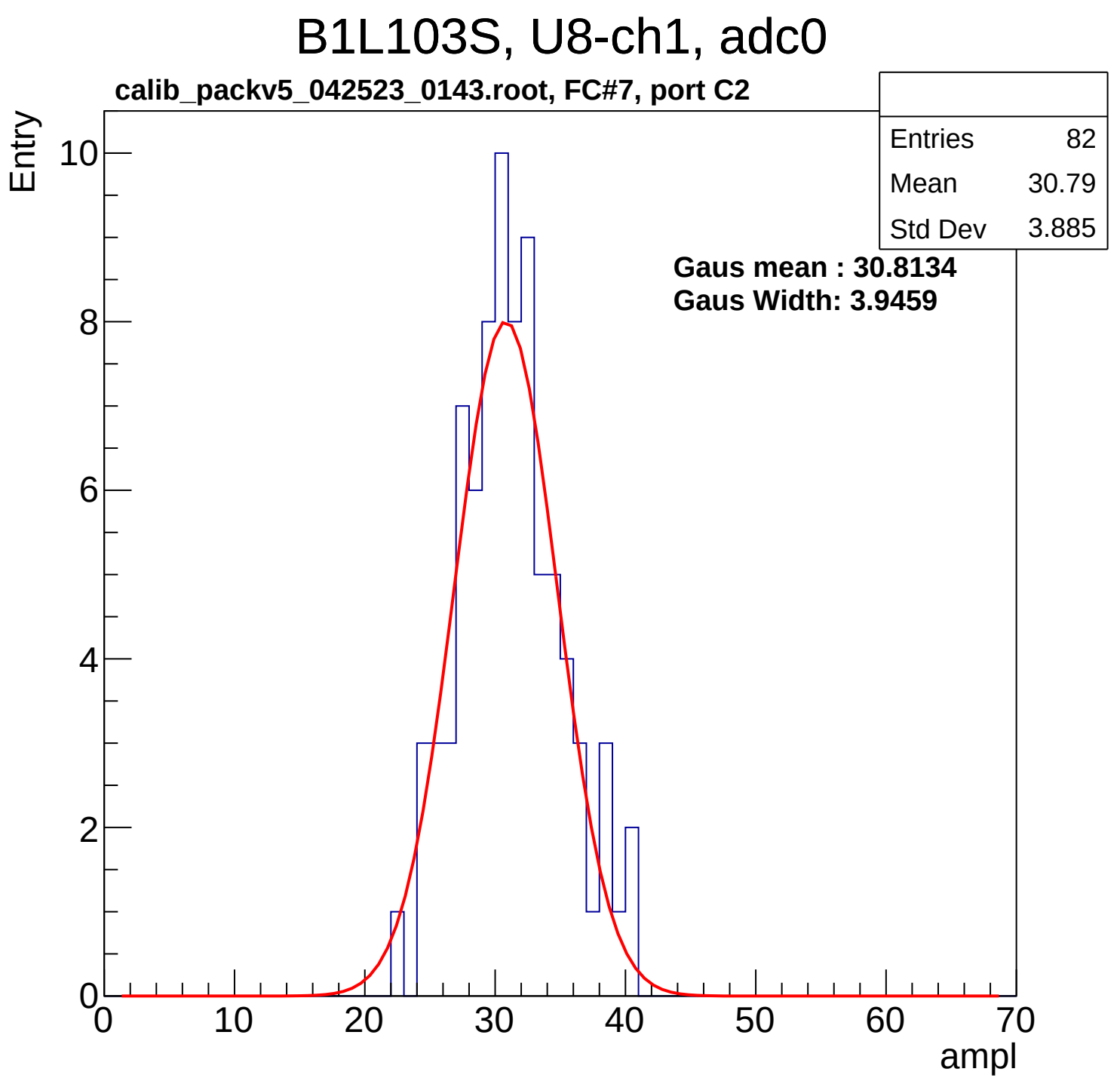

B1L103S, U8-ch0, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 47.21
Std Dev 3.654
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

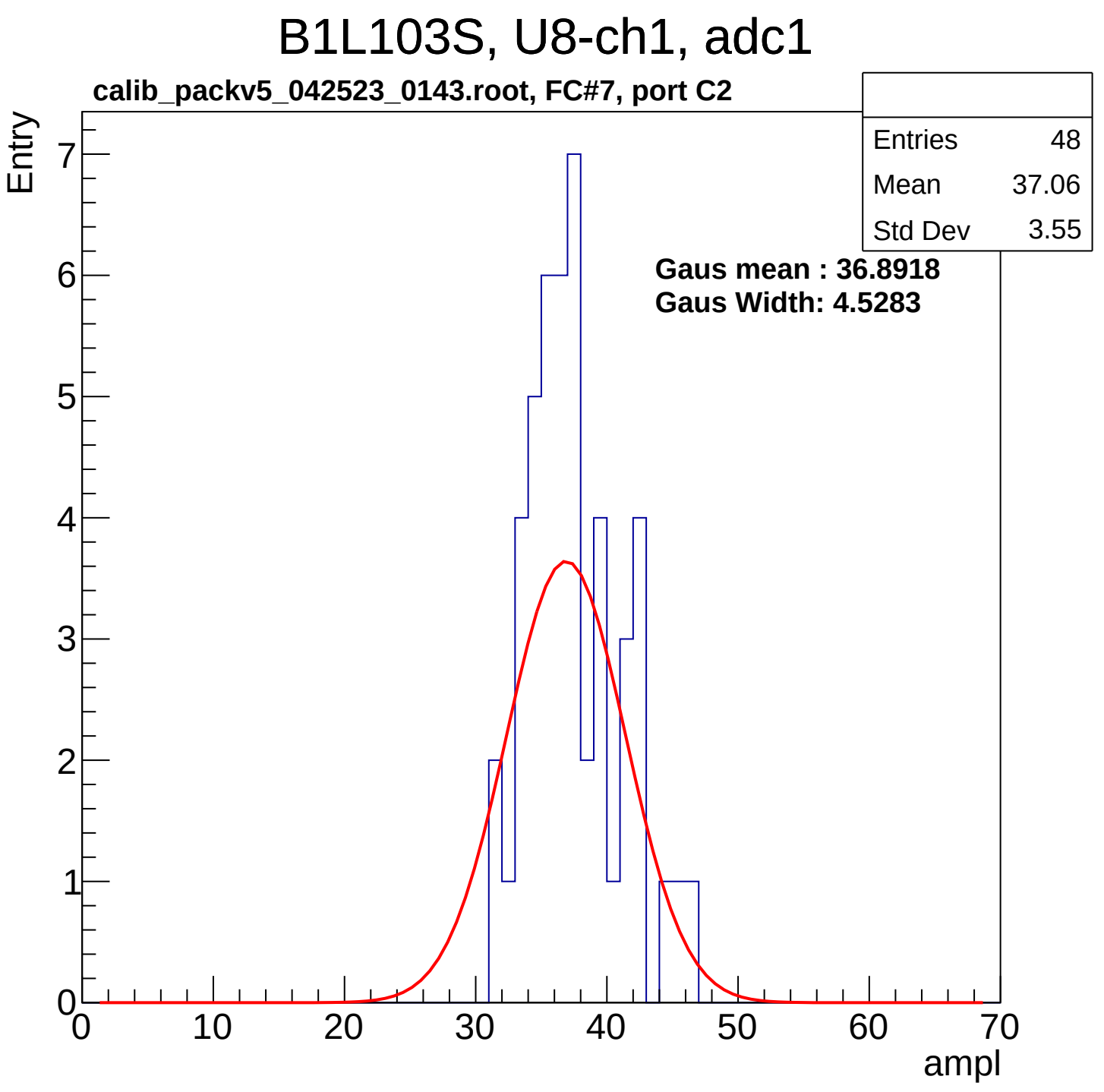

B1L103S, U8-ch0, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 54.36
Std Dev 3.387
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

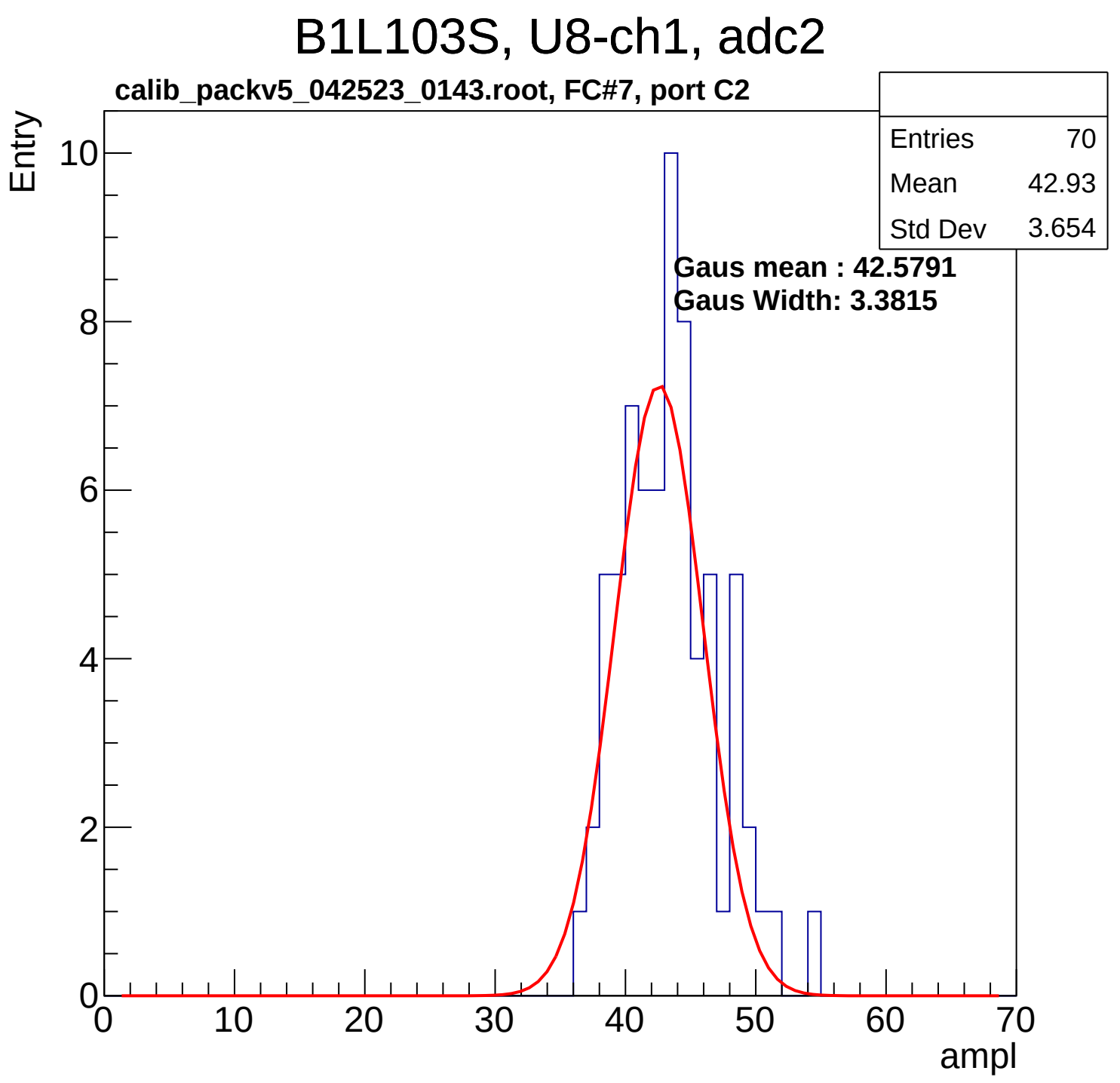

B1L103S, U8-ch0, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 58.66
Std Dev 2.723
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

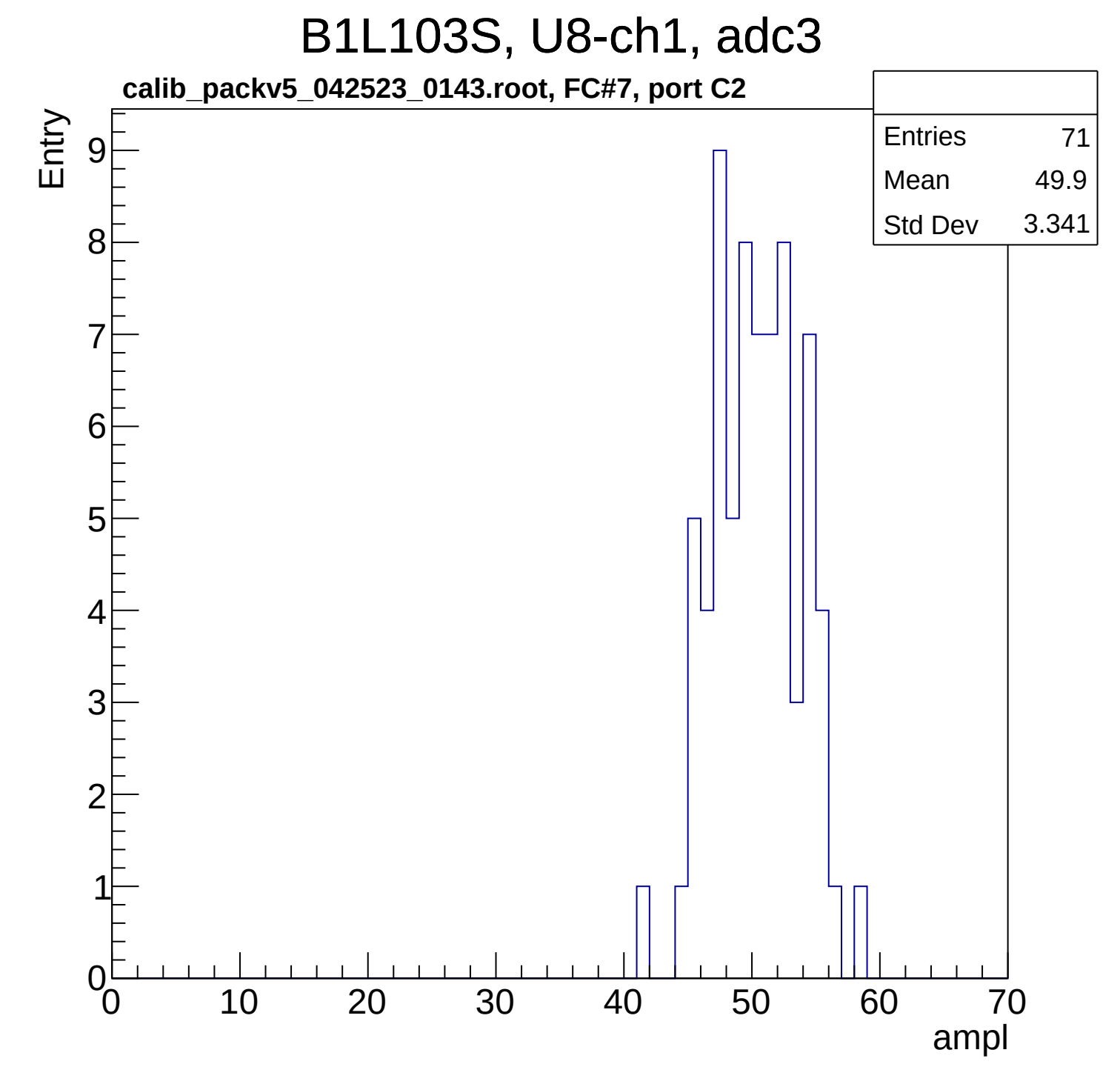

B1L103S, U8-ch0, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 19
Mean 58.05
Std Dev 13.76
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

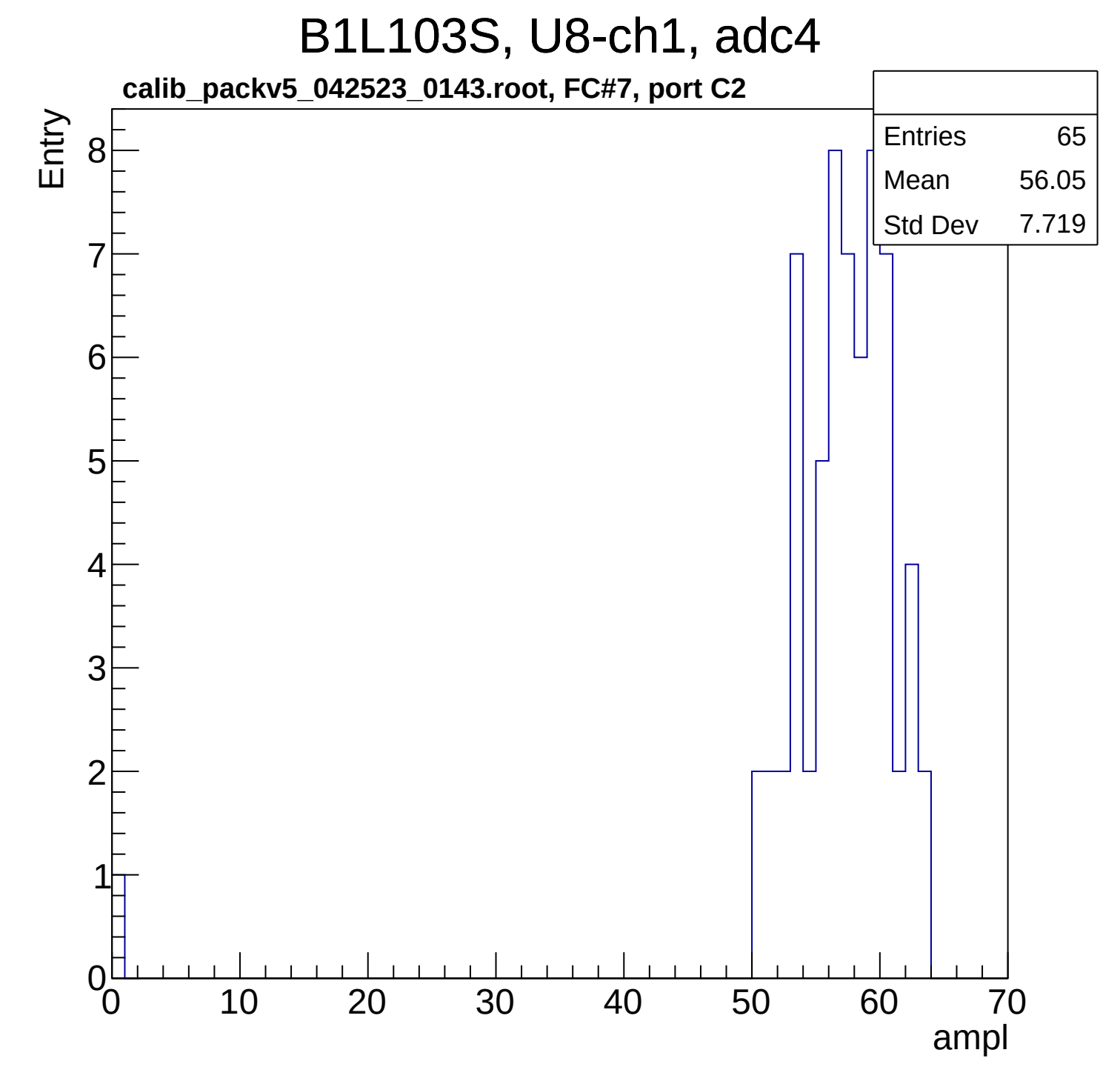

B1L103S, U8-ch0, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 34
Std Dev 29
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

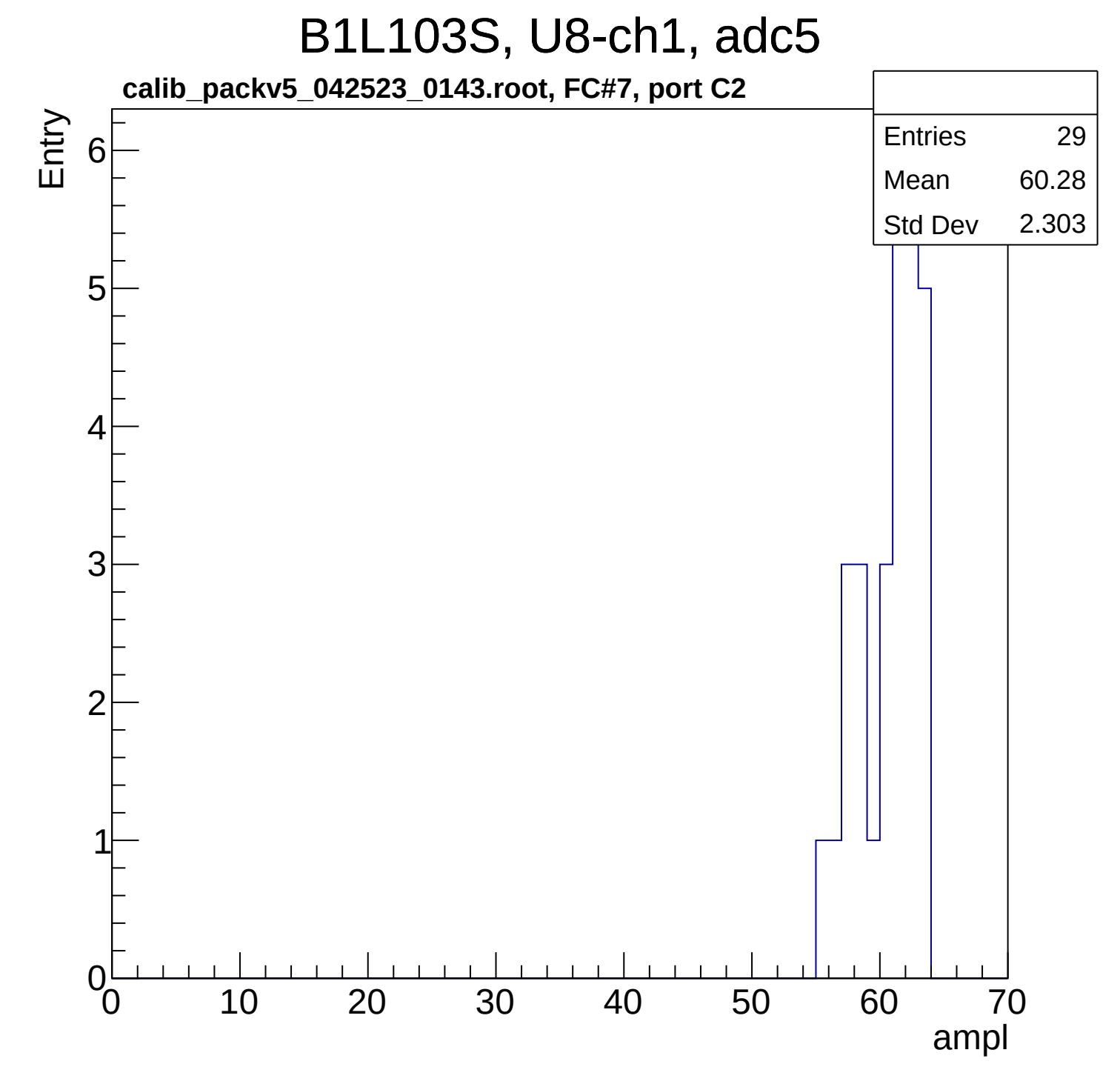

B1L103S, U8-ch1, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 82
Mean 30.79
Std Dev 3.885
Gaus mean : 30.8134
Gaus Width: 3.9459
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

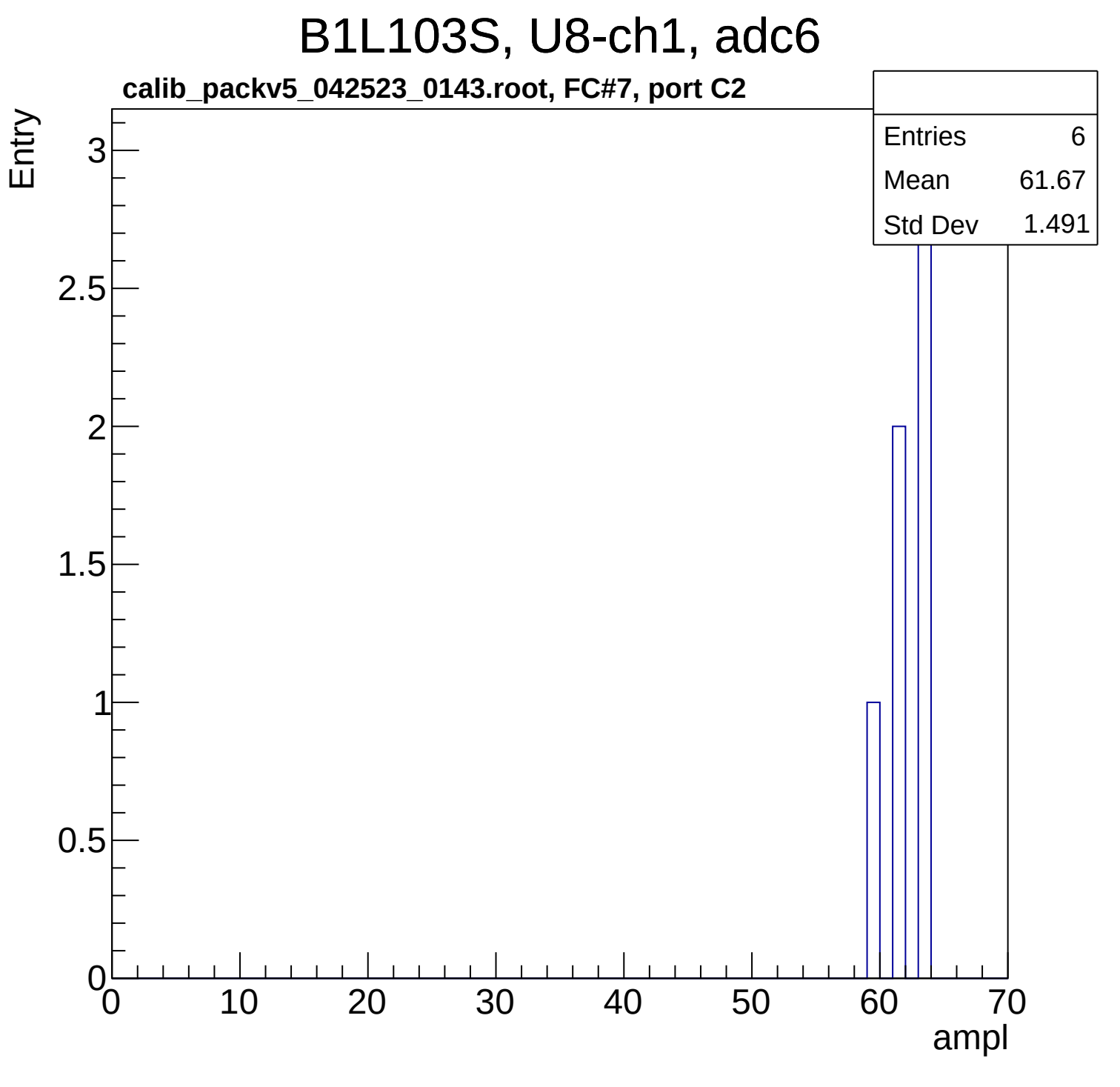

B1L103S, U8-ch1, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 37.06
Std Dev 3.55
Gaus mean : 36.8918
Gaus Width: 4.5283
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

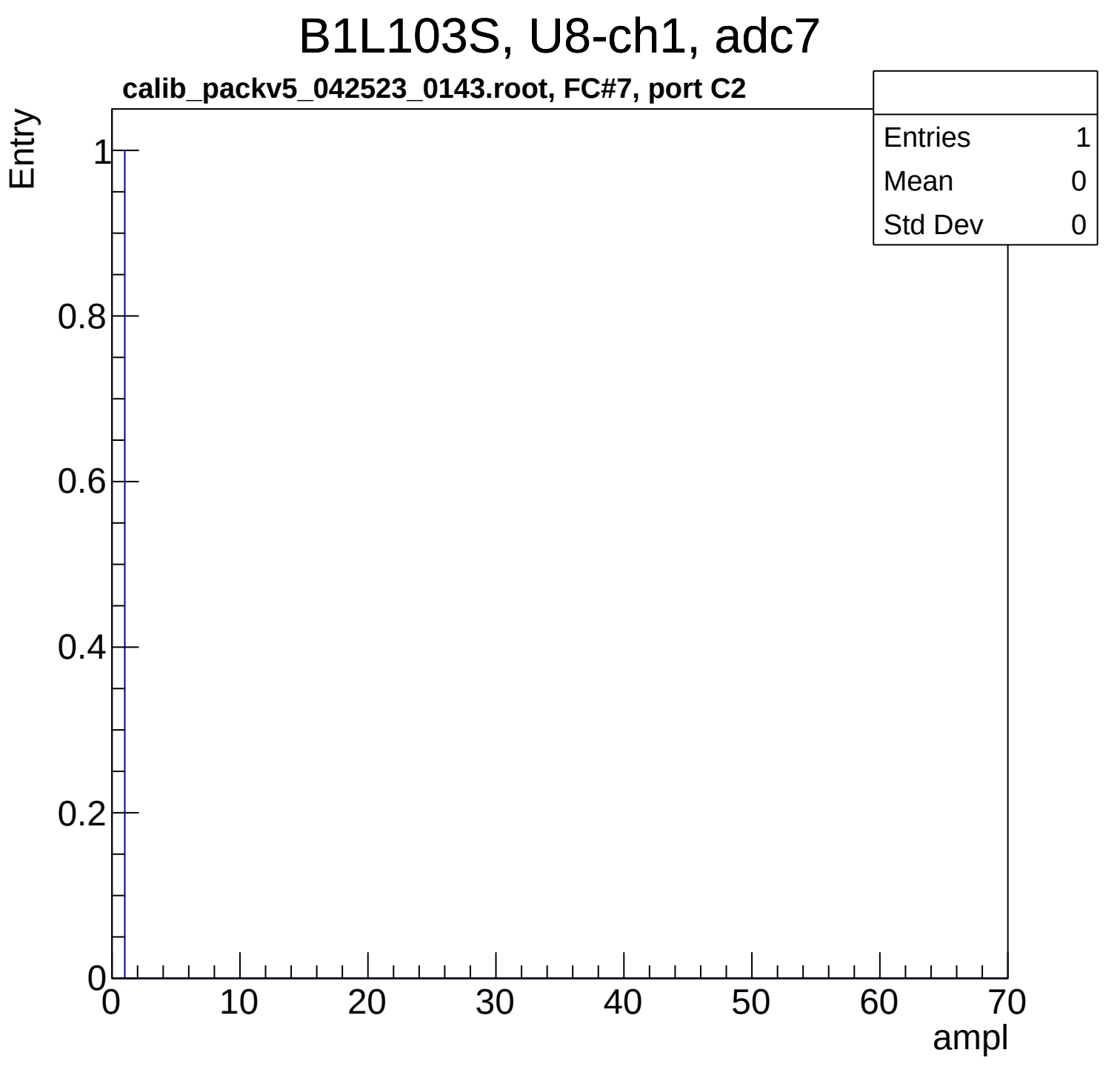

B1L103S, U8-ch1, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 42.93
Std Dev 3.654
Gaus mean : 42.5791
Gaus Width: 3.3815
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

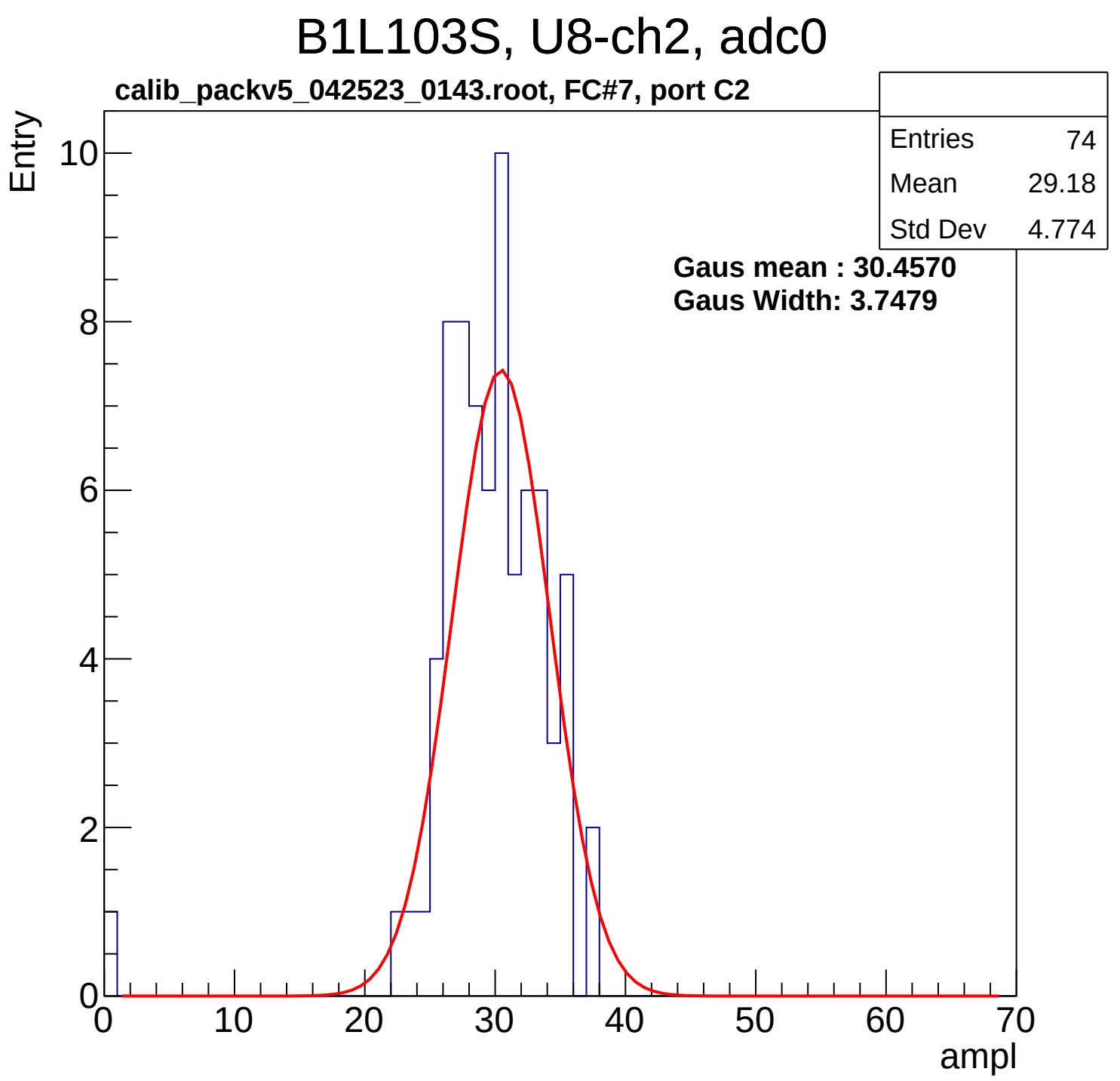

B1L103S, U8-ch1, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 49.9
Std Dev 3.341
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

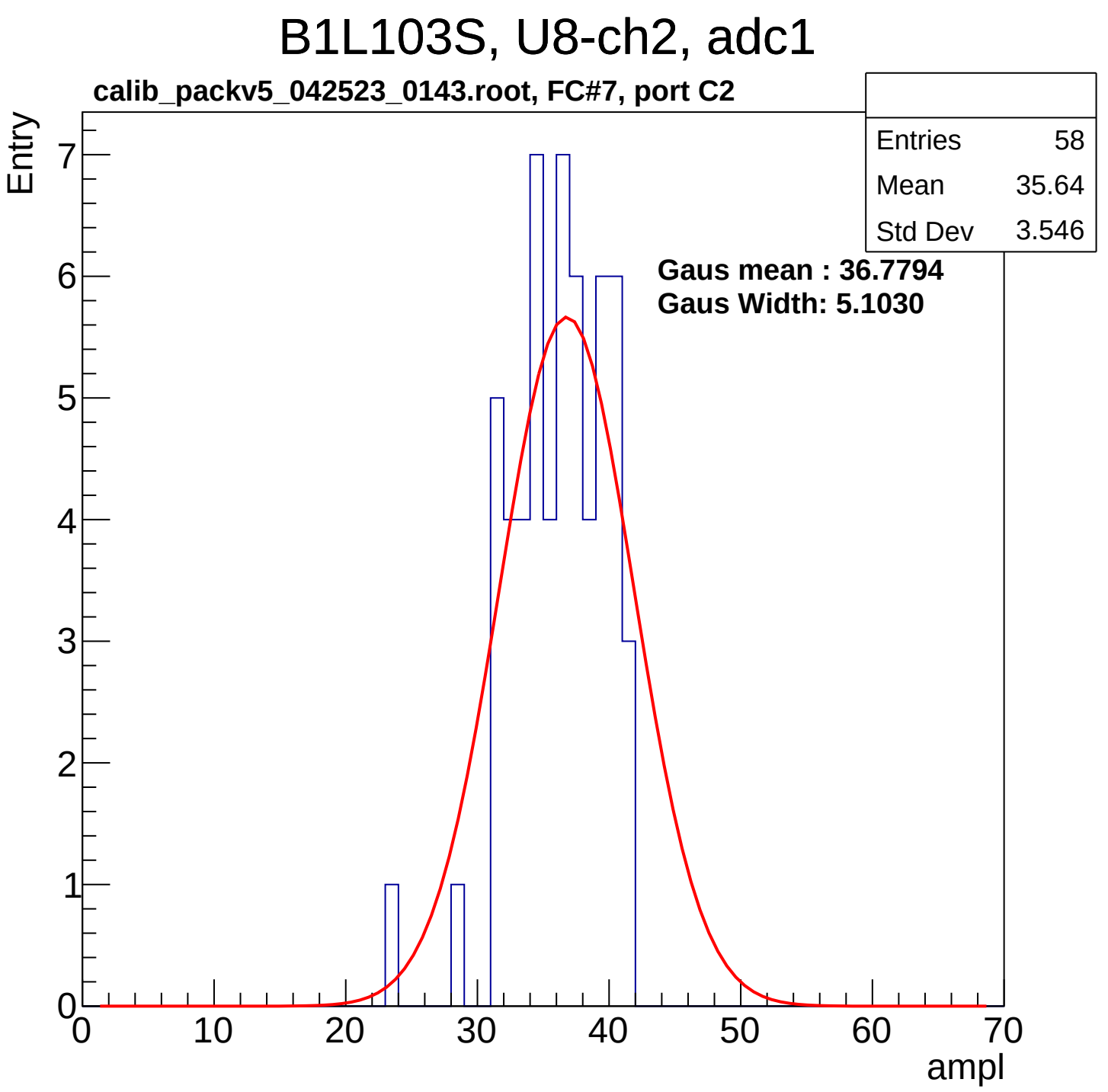

B1L103S, U8-ch1, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 56.05
Std Dev 7.719
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

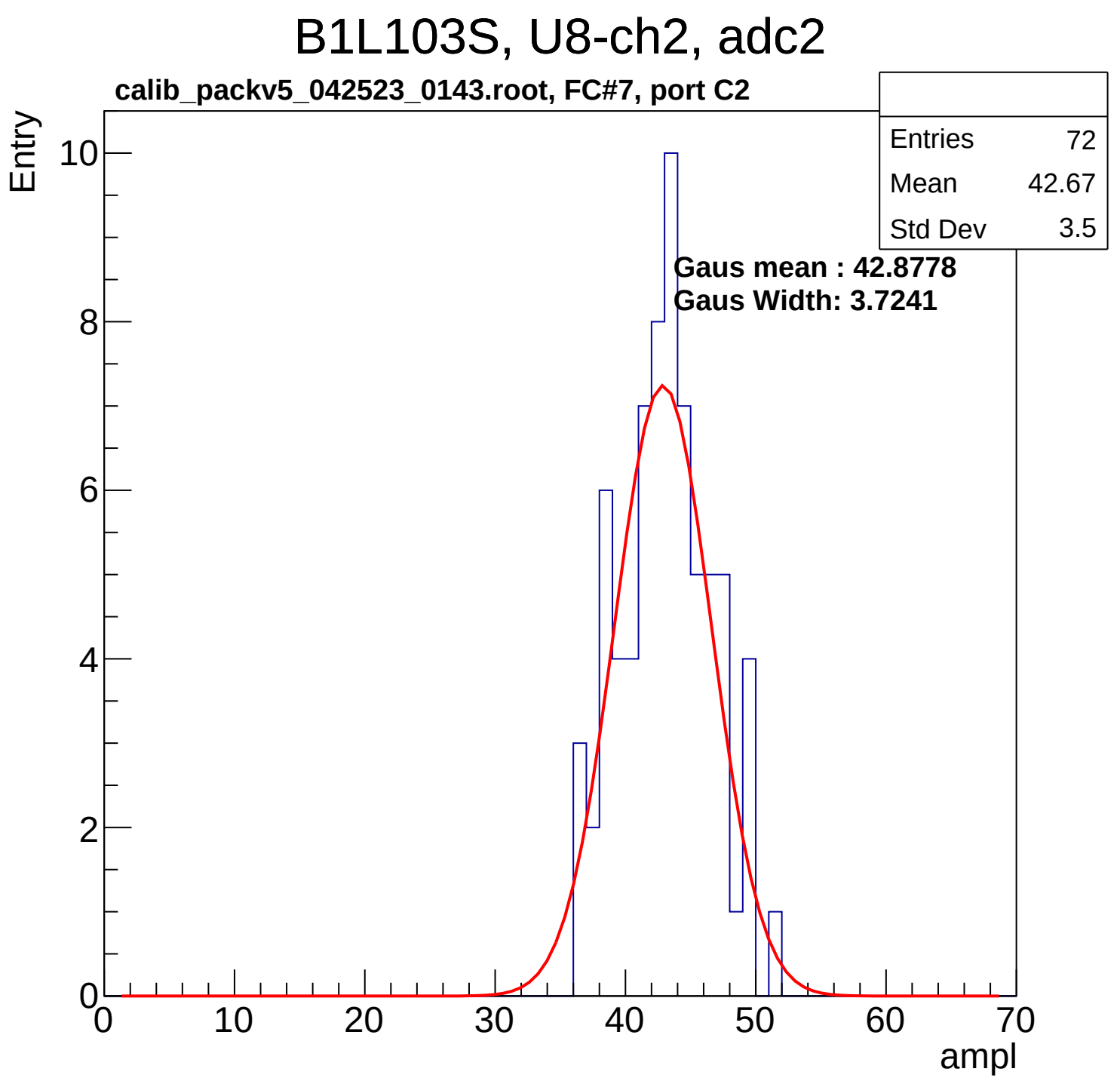

B1L103S, U8-ch1, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 29
Mean 60.28
Std Dev 2.303
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

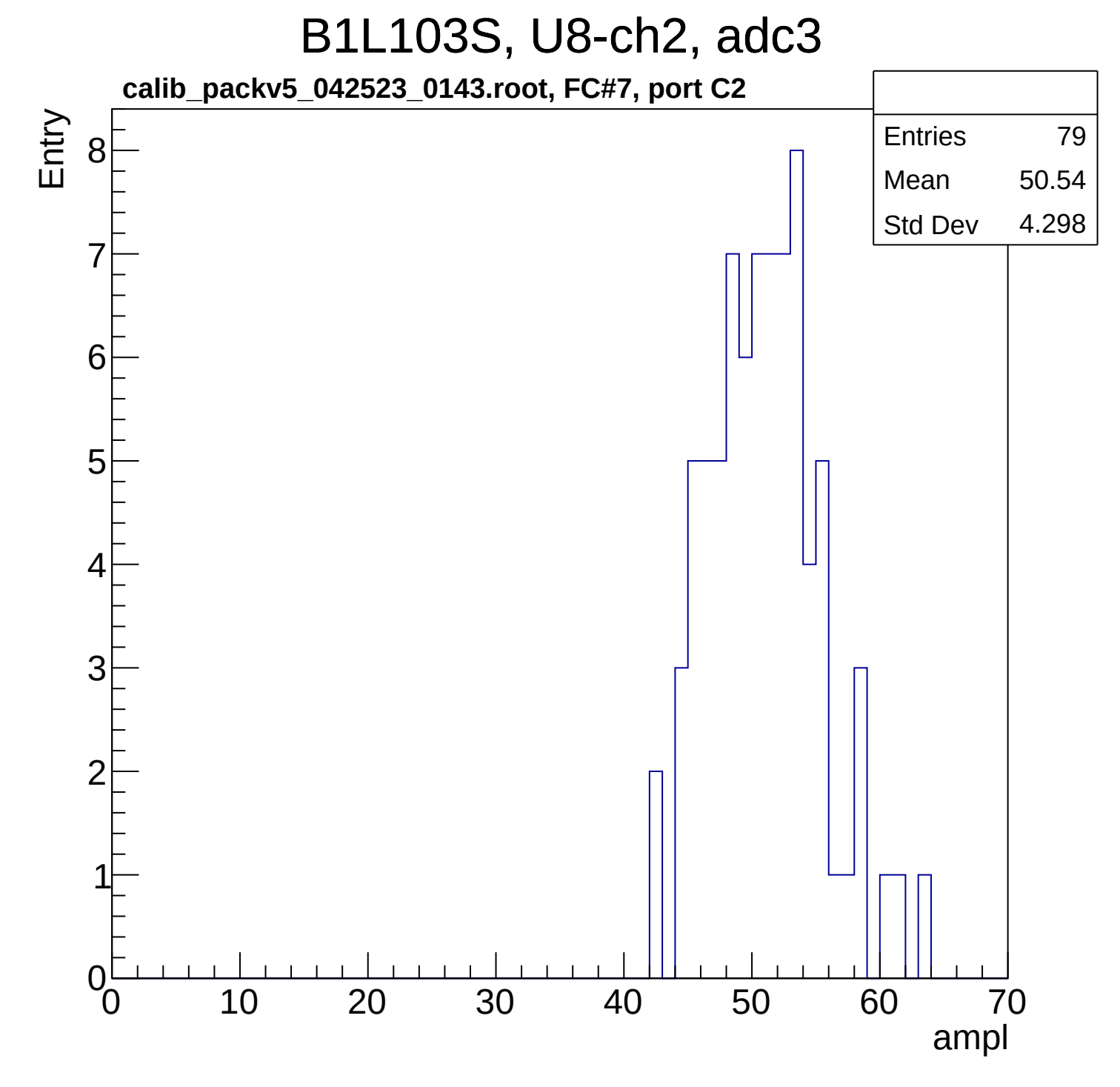

B1L103S, U8-ch1, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 61.67
Std Dev 1.491
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

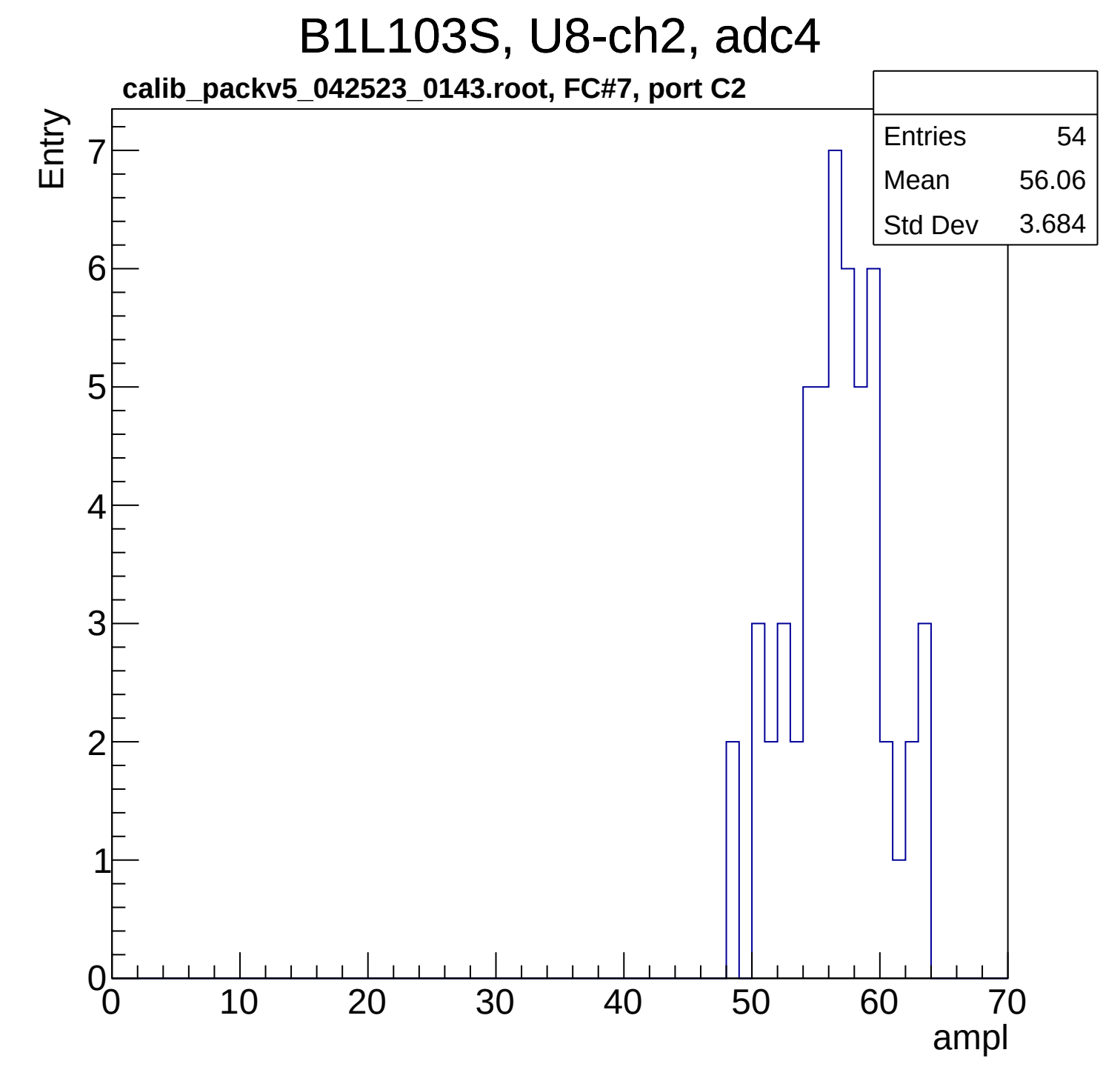

B1L103S, U8-ch1, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

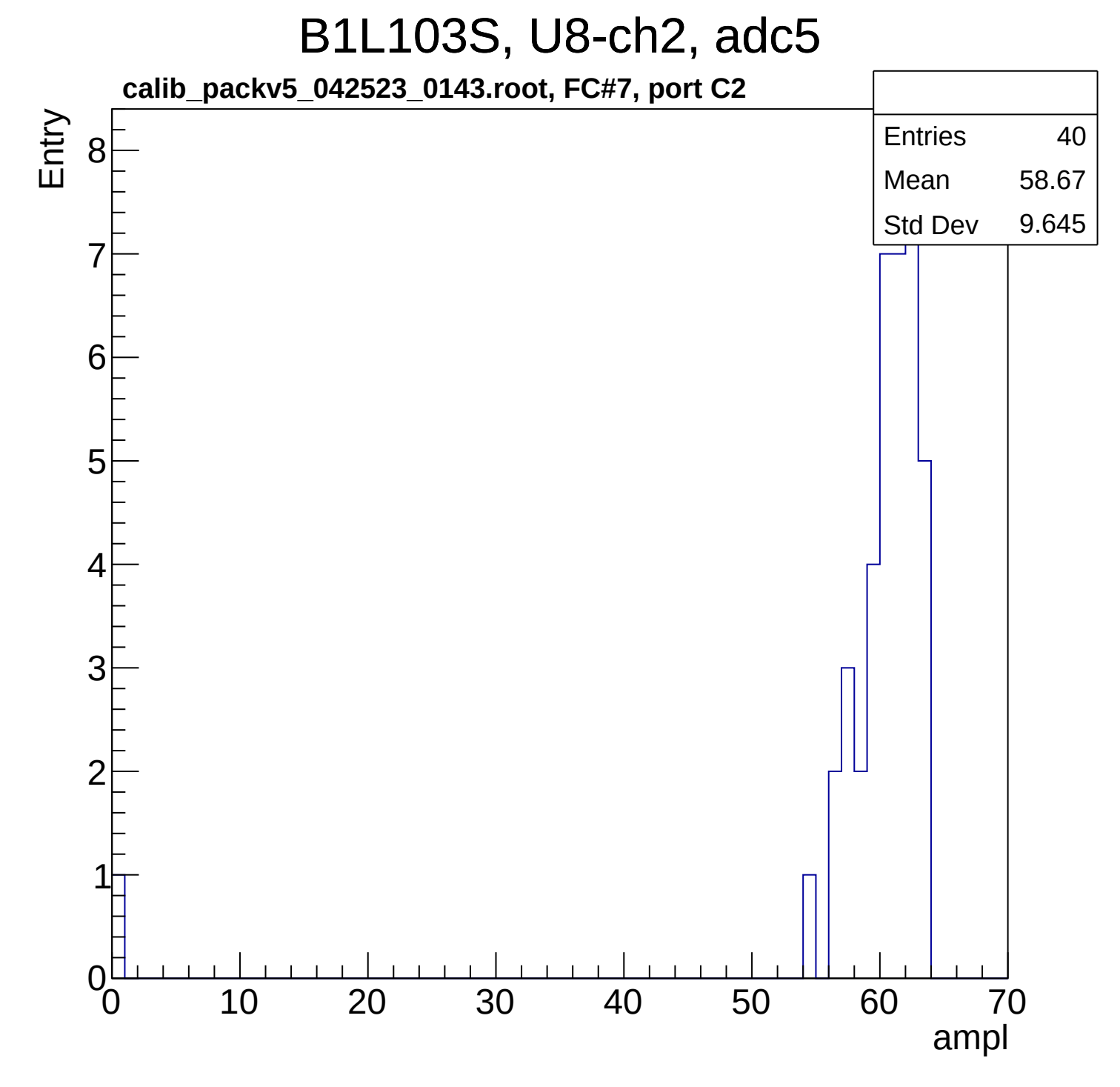

B1L103S, U8-ch2, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 29.18
Std Dev 4.774
Gaus mean : 30.4570
Gaus Width: 3.7479
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

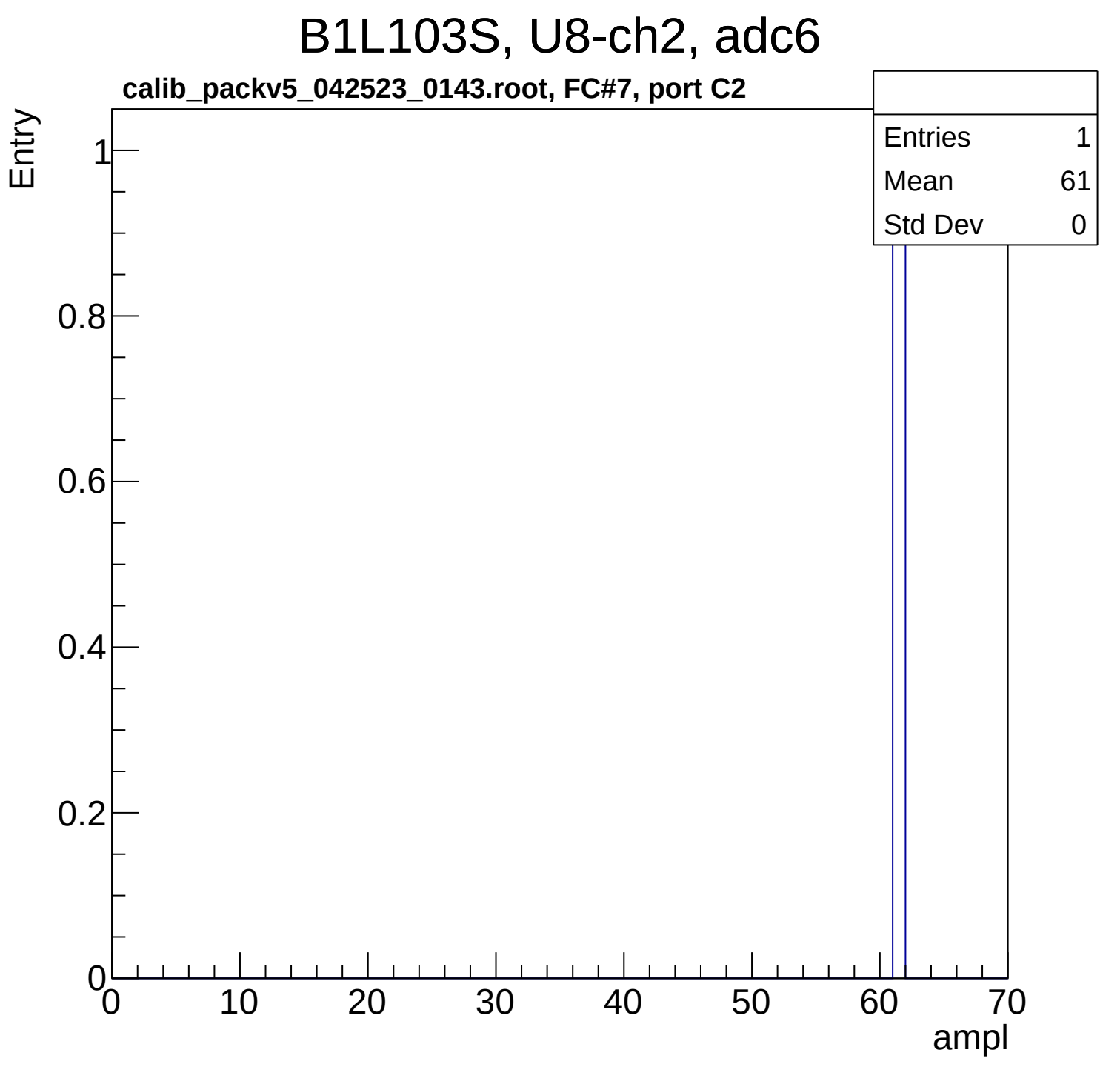

B1L103S, U8-ch2, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 35.64
Std Dev 3.546
Gaus mean : 36.7794
Gaus Width: 5.1030
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

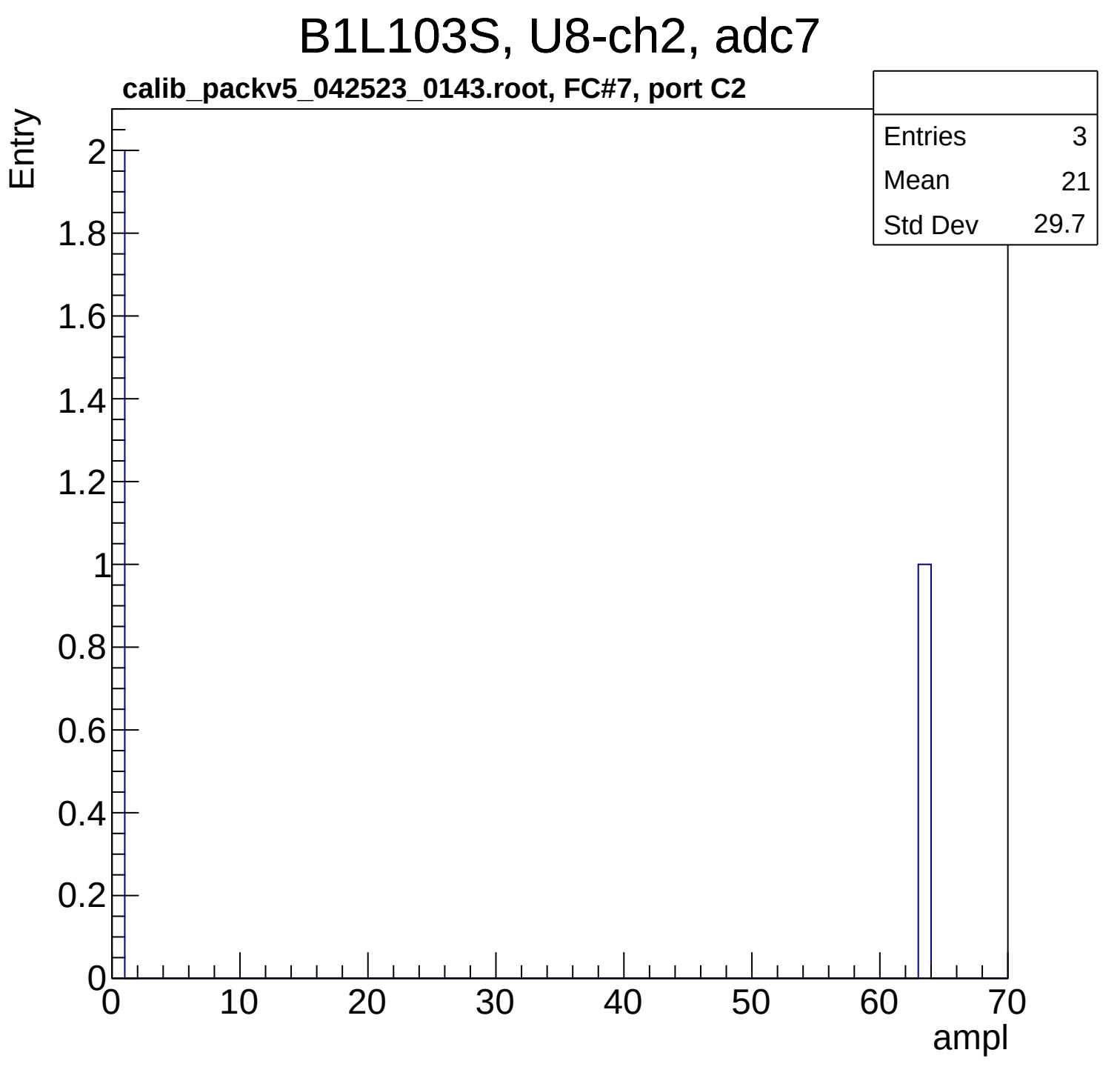

B1L103S, U8-ch2, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 42.67
Std Dev 3.5
Gaus mean : 42.8778
Gaus Width: 3.7241
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

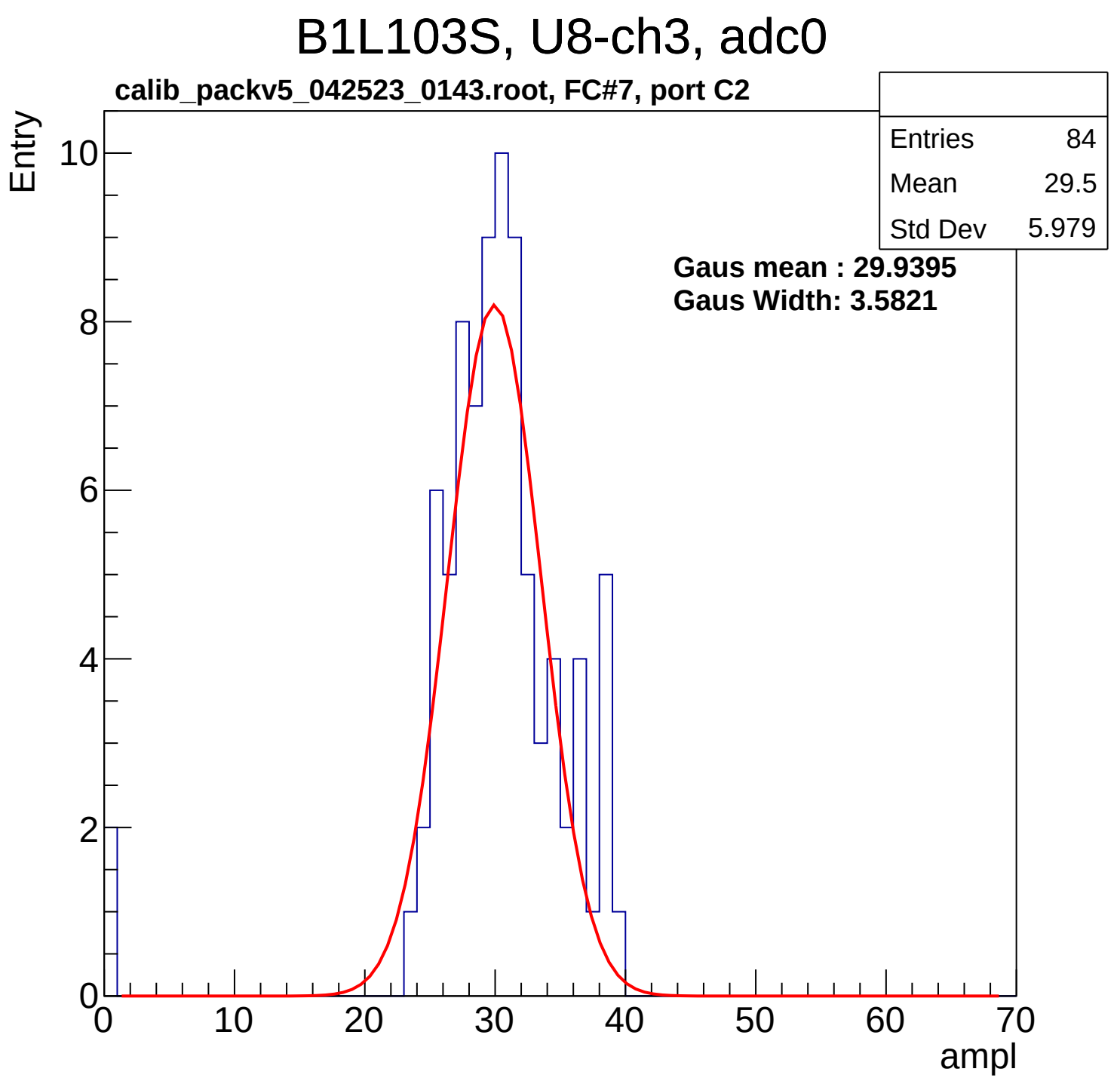

B1L103S, U8-ch2, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 79
Mean 50.54
Std Dev 4.298
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

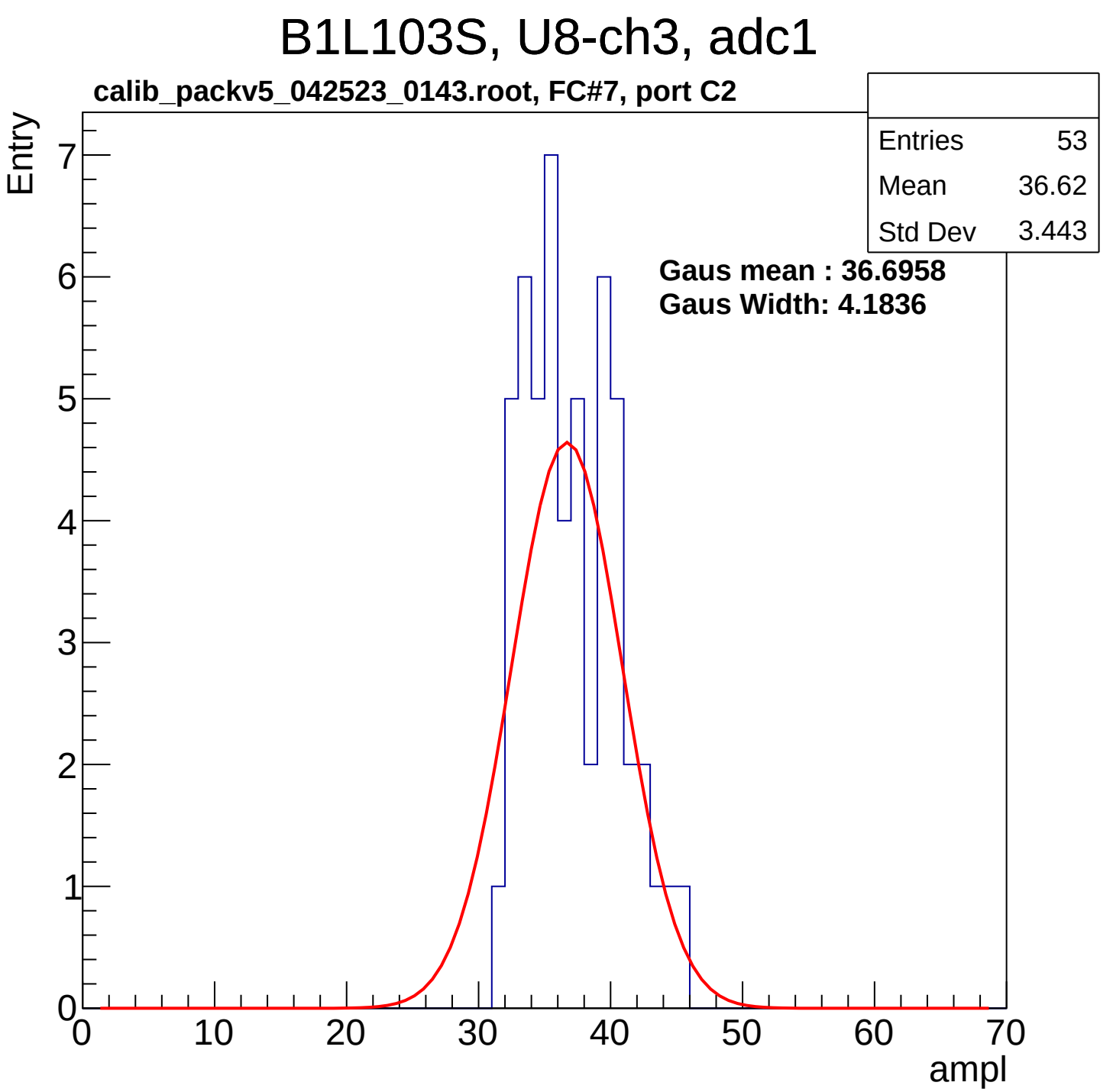

B1L103S, U8-ch2, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 56.06
Std Dev 3.684
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

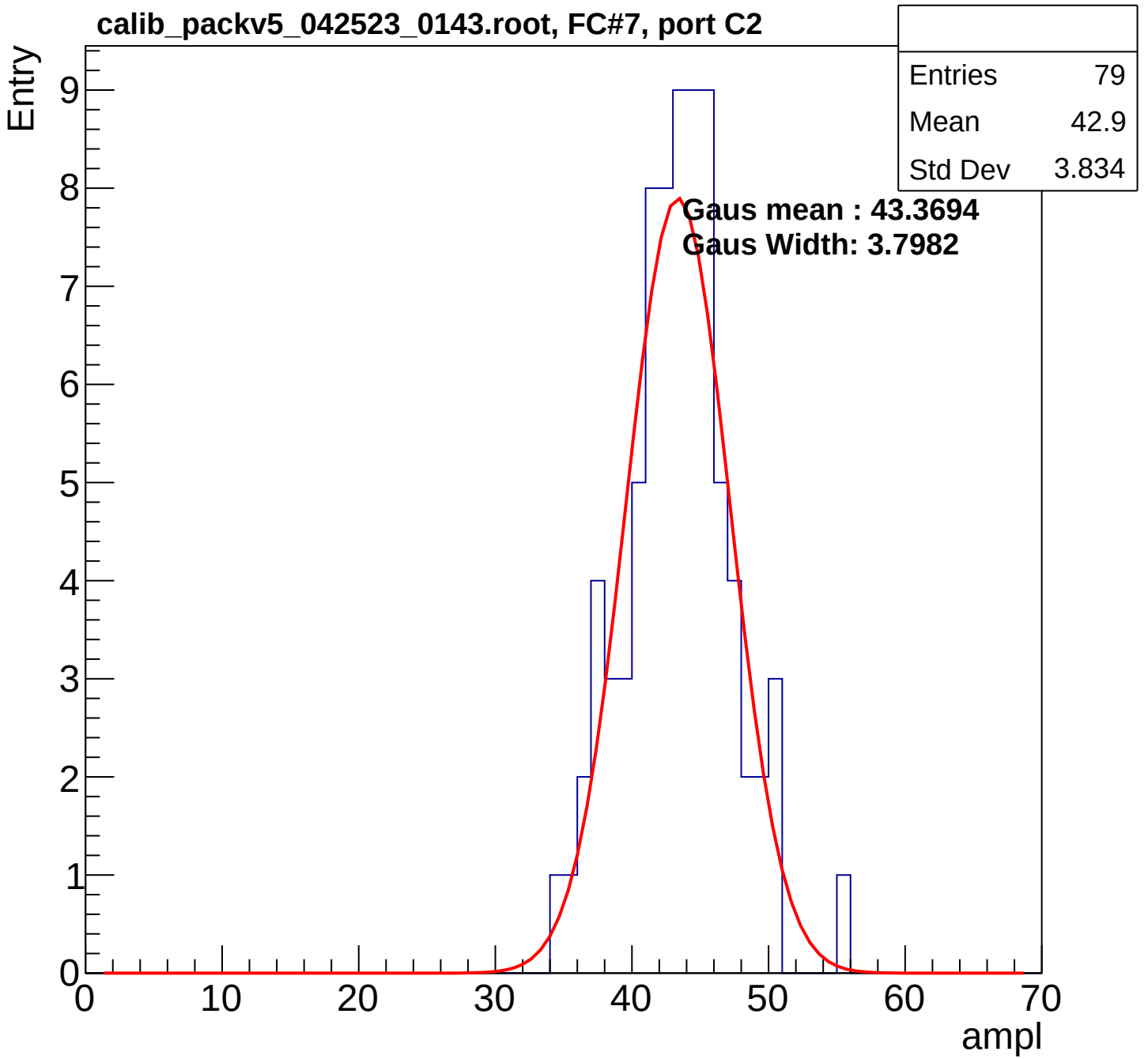

B1L103S, U8-ch2, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 40
Mean 58.67
Std Dev 9.645
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

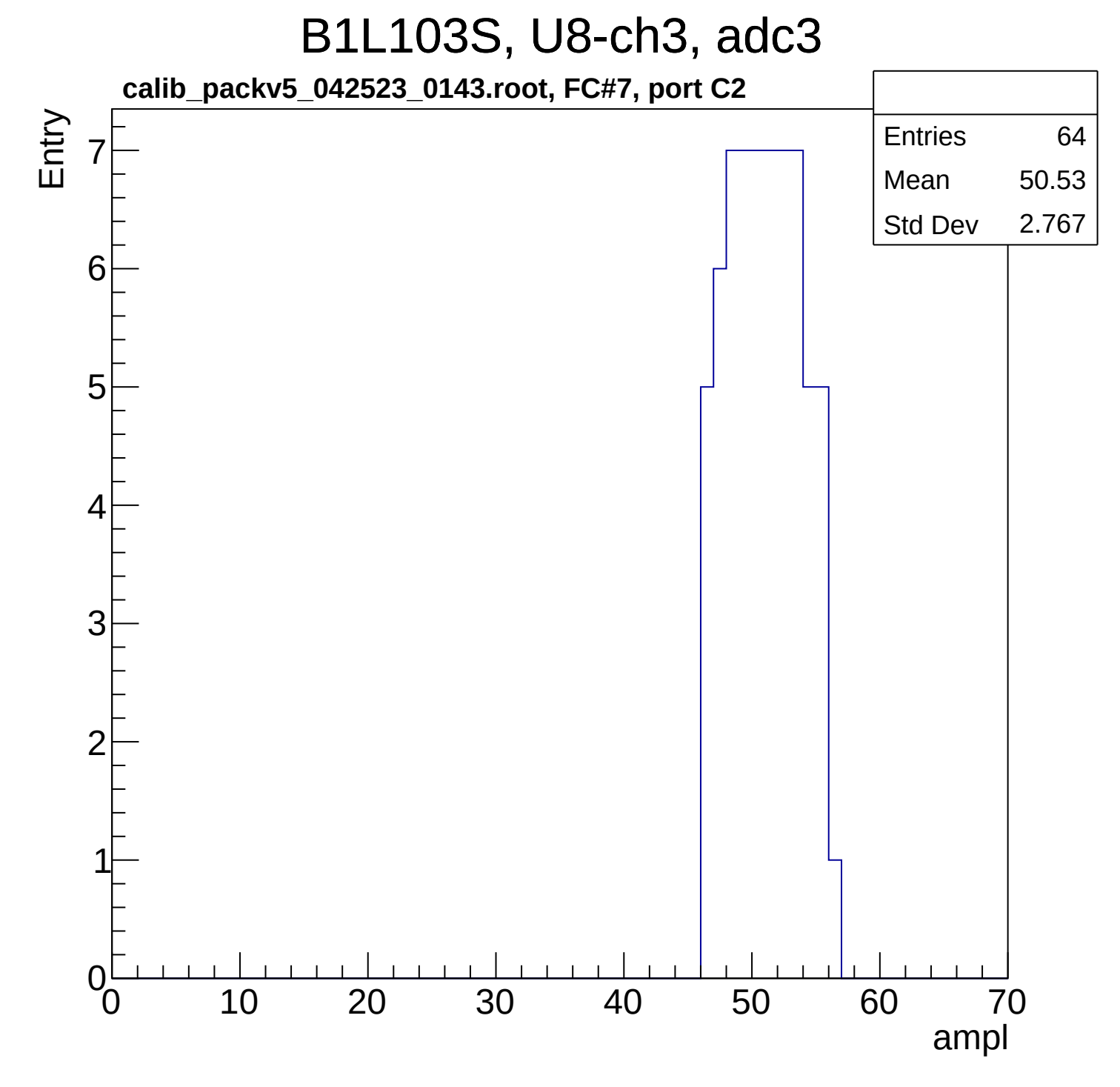

B1L103S, U8-ch2, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 61
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

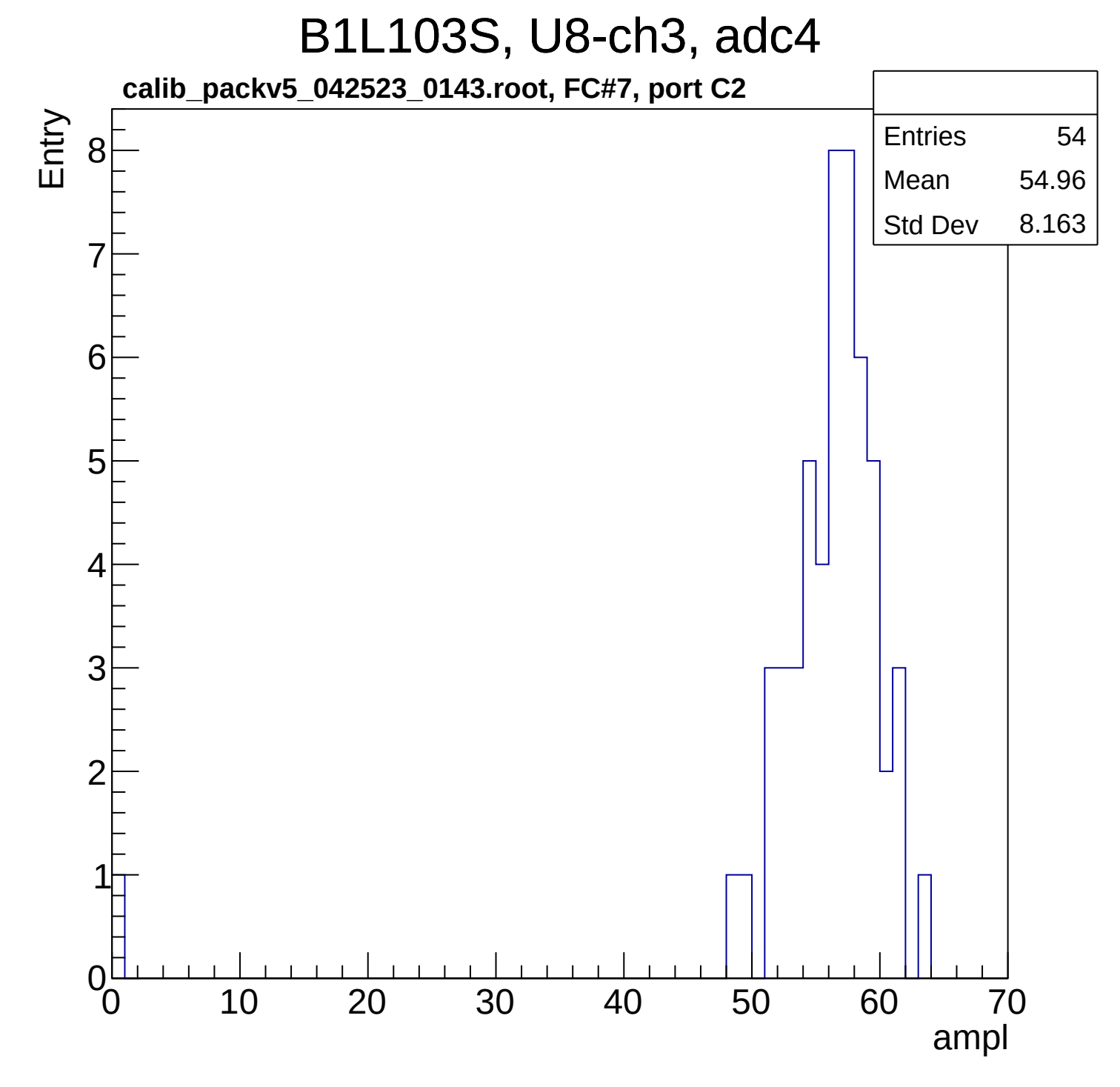

B1L103S, U8-ch2, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 21
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

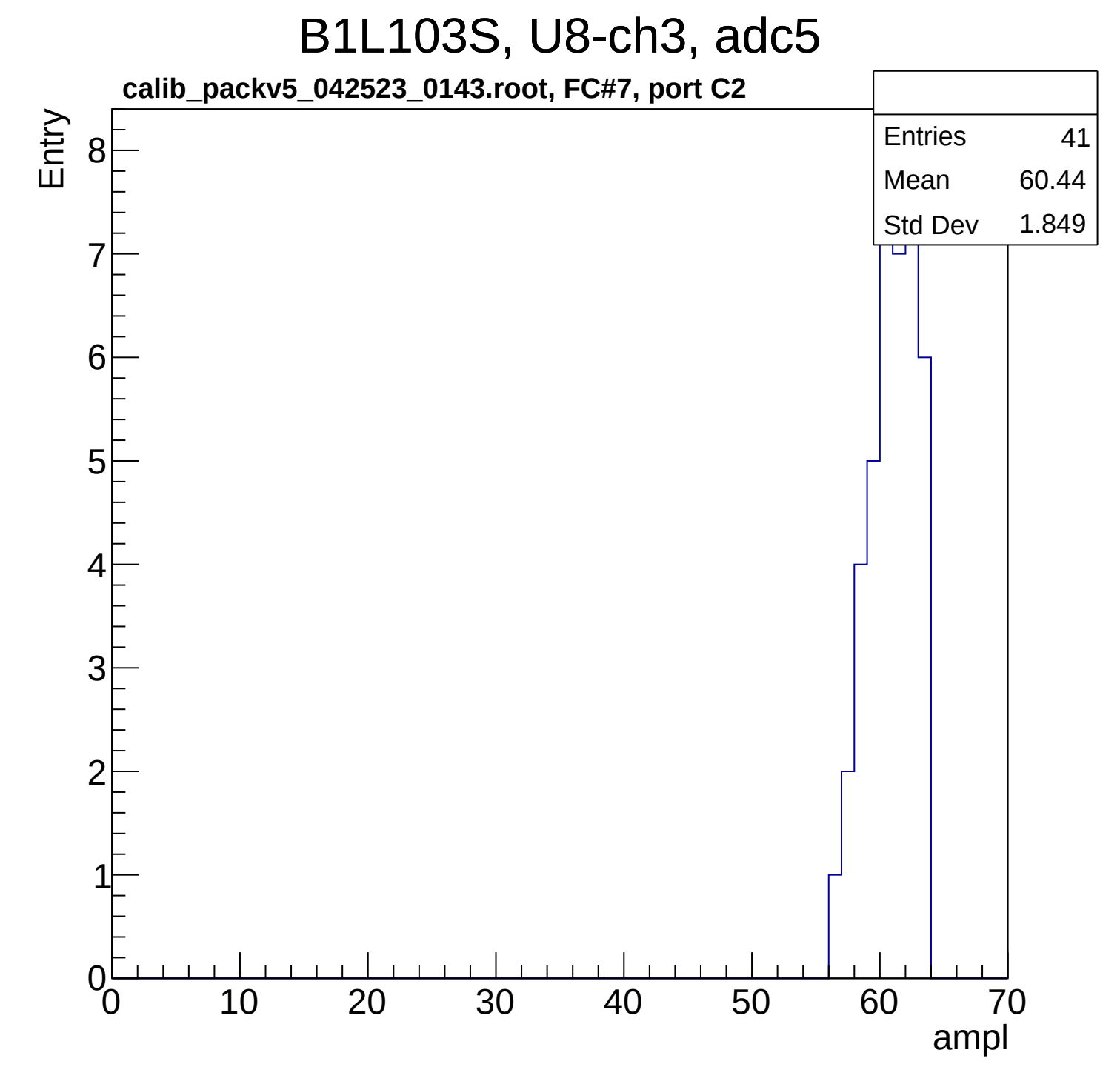

B1L103S, U8-ch3, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 84
Mean 29.5
Std Dev 5.979
Gaus mean : 29.9395
Gaus Width: 3.5821
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

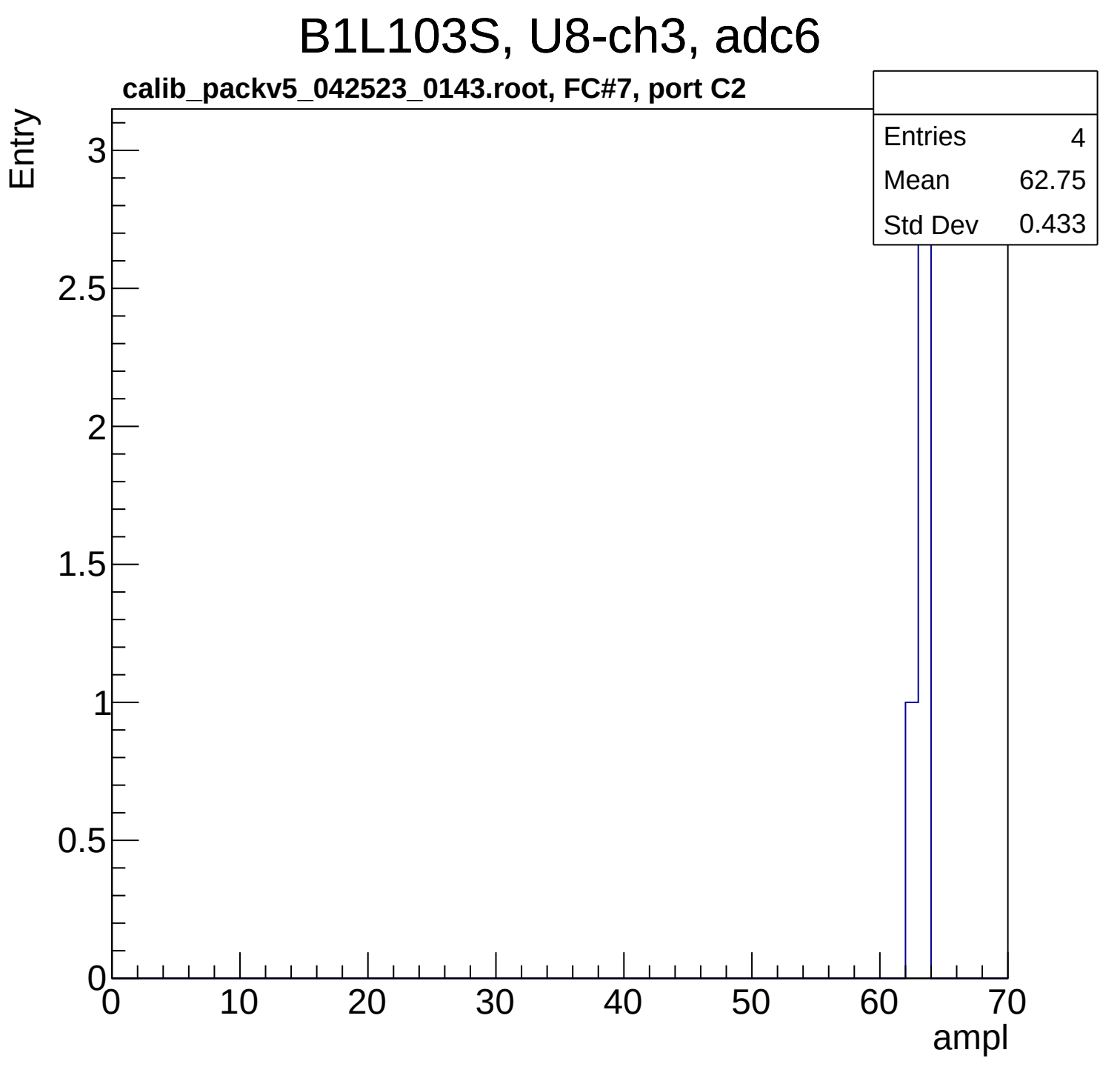

B1L103S, U8-ch3, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 36.62
Std Dev 3.443
Gaus mean : 36.6958
Gaus Width: 4.1836
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

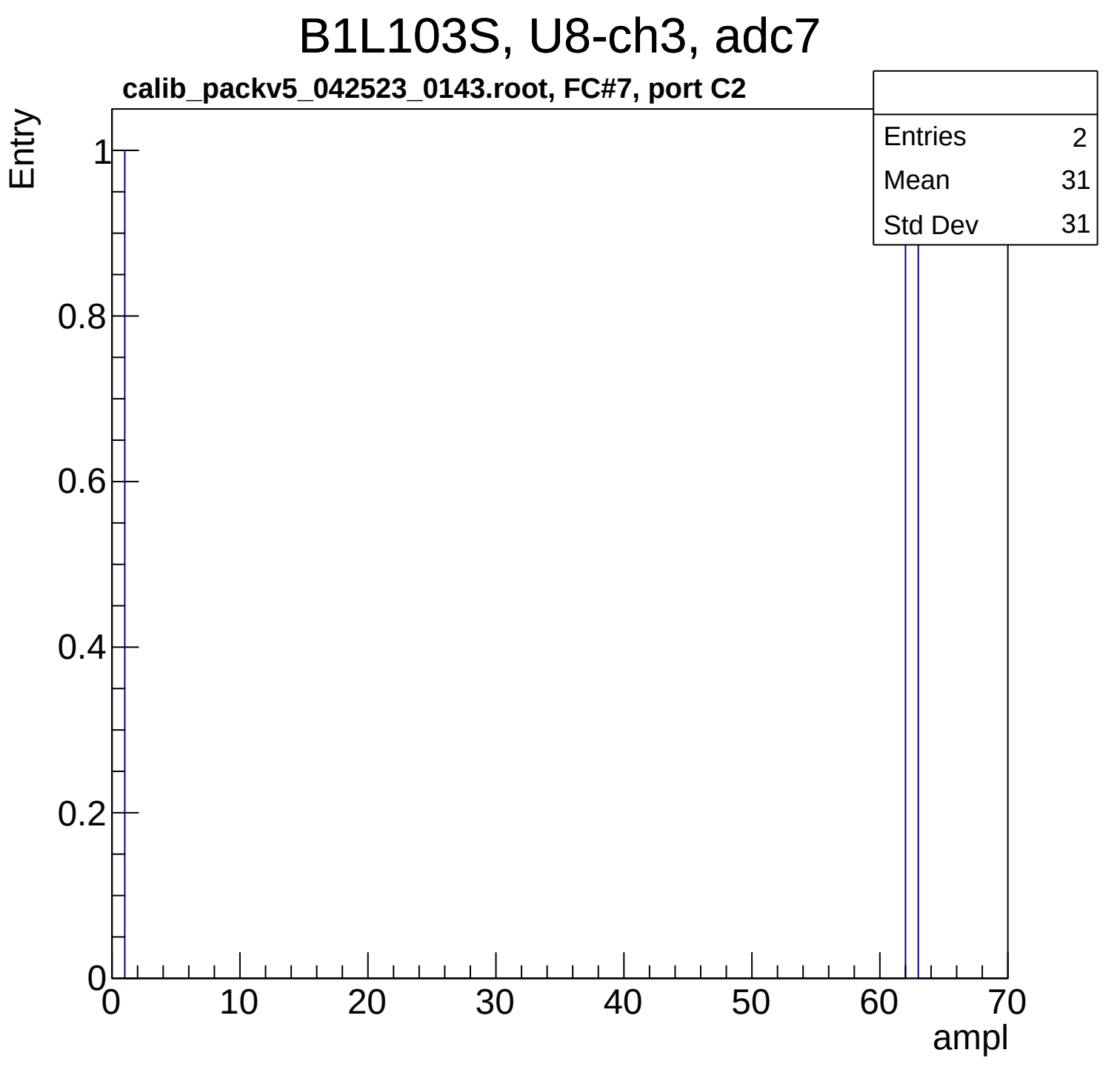

B1L103S, U8-ch3, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 79
Mean 42.9
Std Dev 3.834
Gaus mean : 43.3694
Gaus Width: 3.7982
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

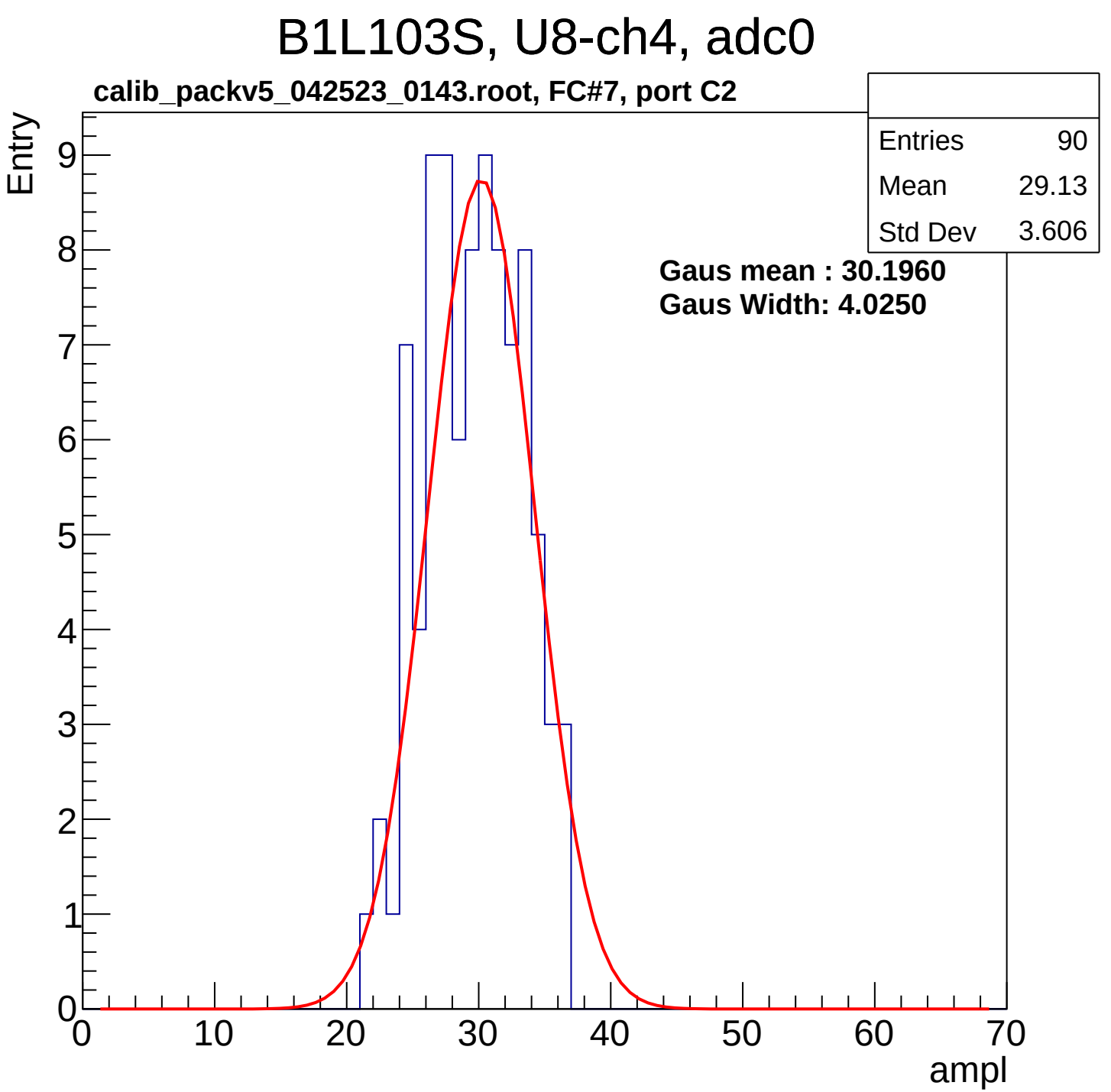

B1L103S, U8-ch3, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 50.53
Std Dev 2.767
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

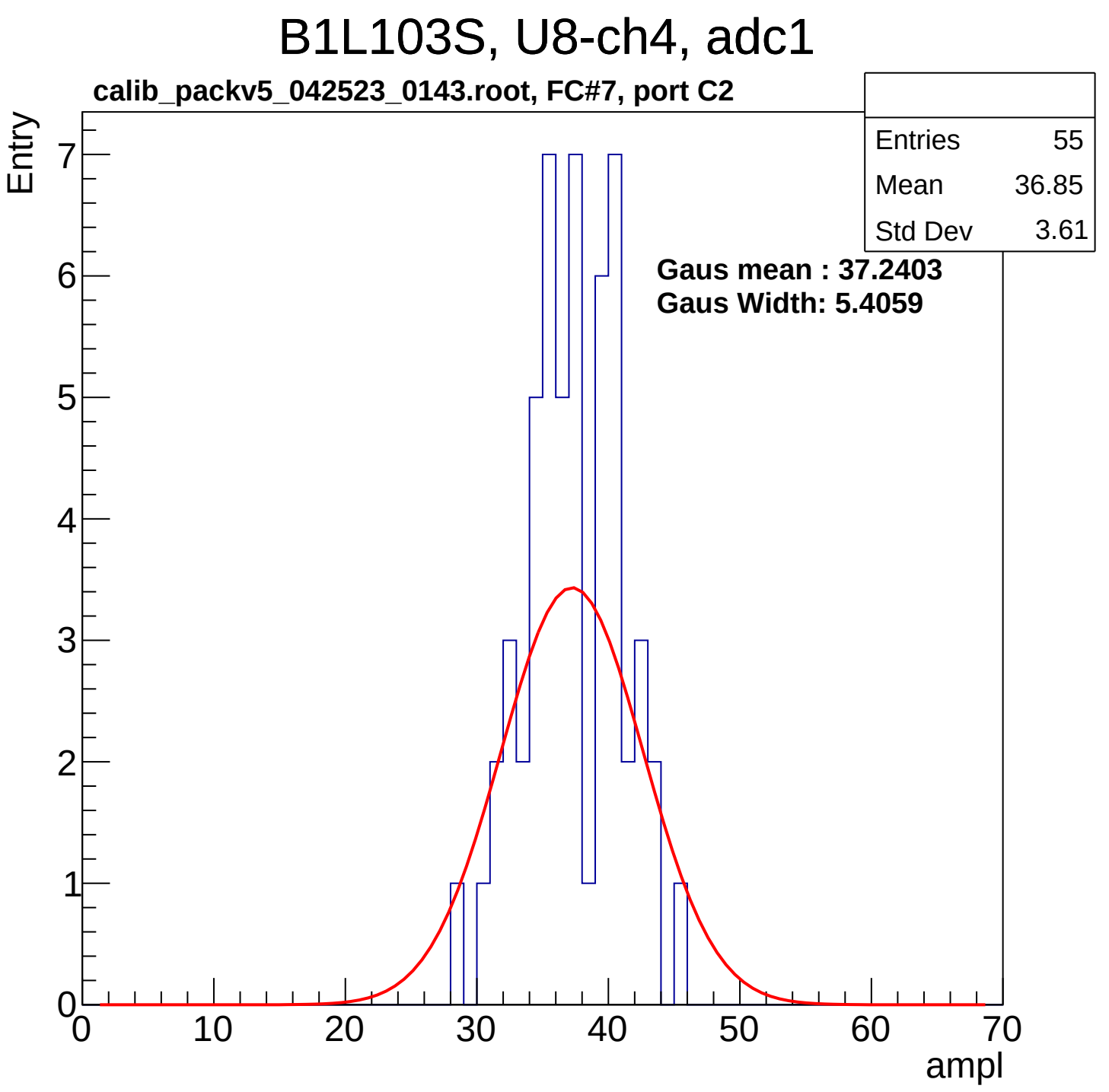

B1L103S, U8-ch3, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 54.96
Std Dev 8.163
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

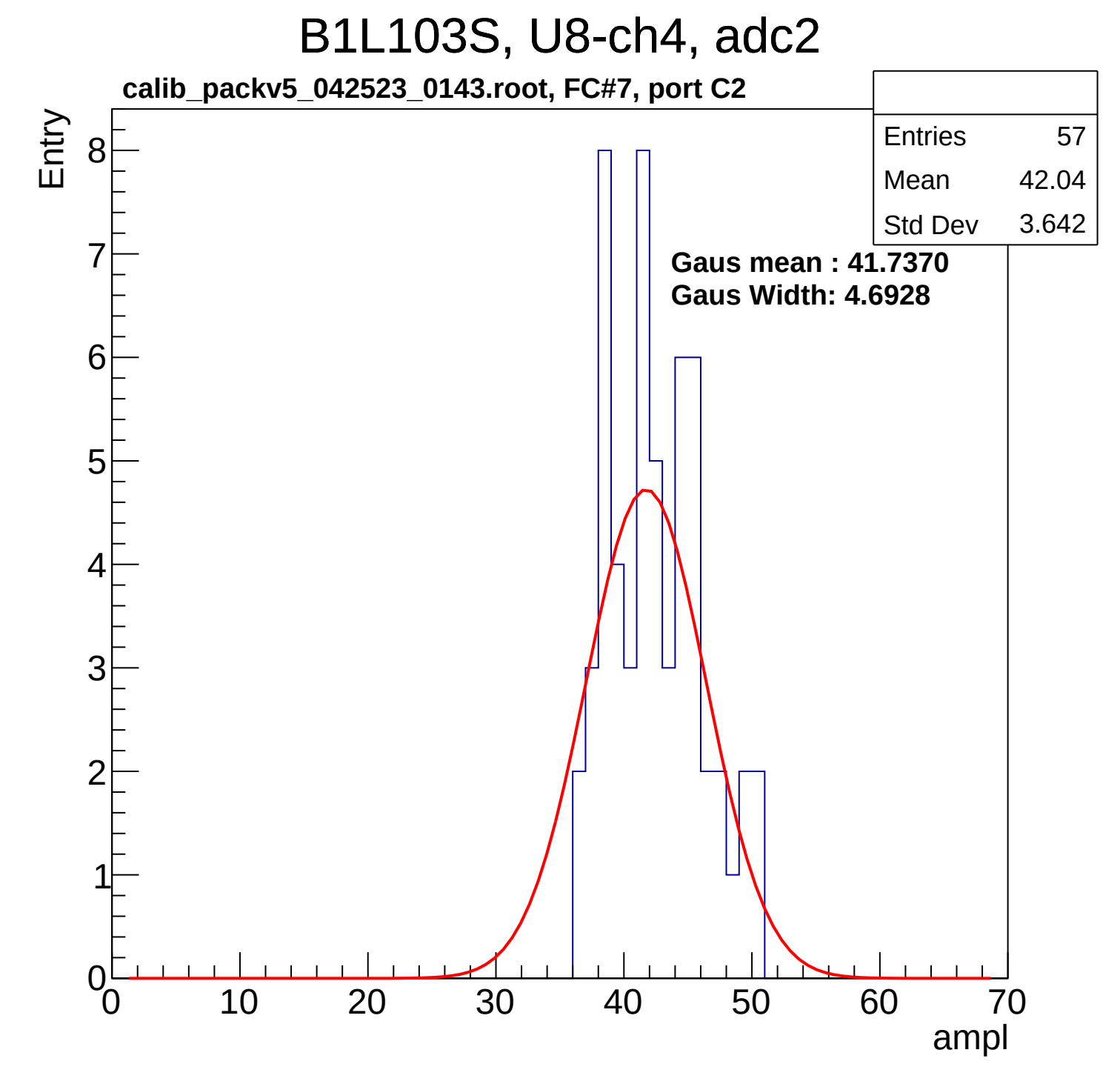

B1L103S, U8-ch3, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 41
Mean 60.44
Std Dev 1.849
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

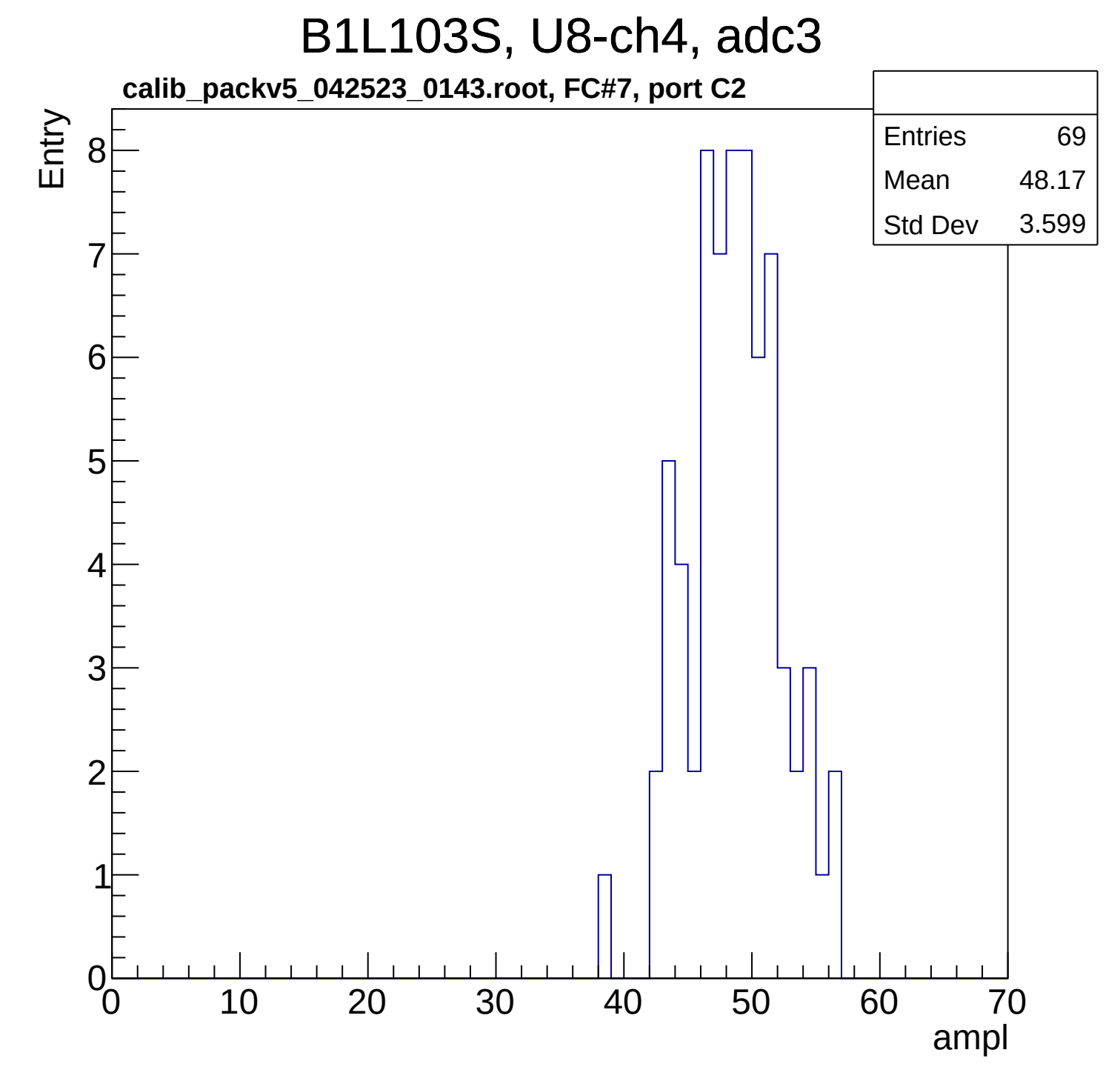

B1L103S, U8-ch3, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 62.75
Std Dev 0.433
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

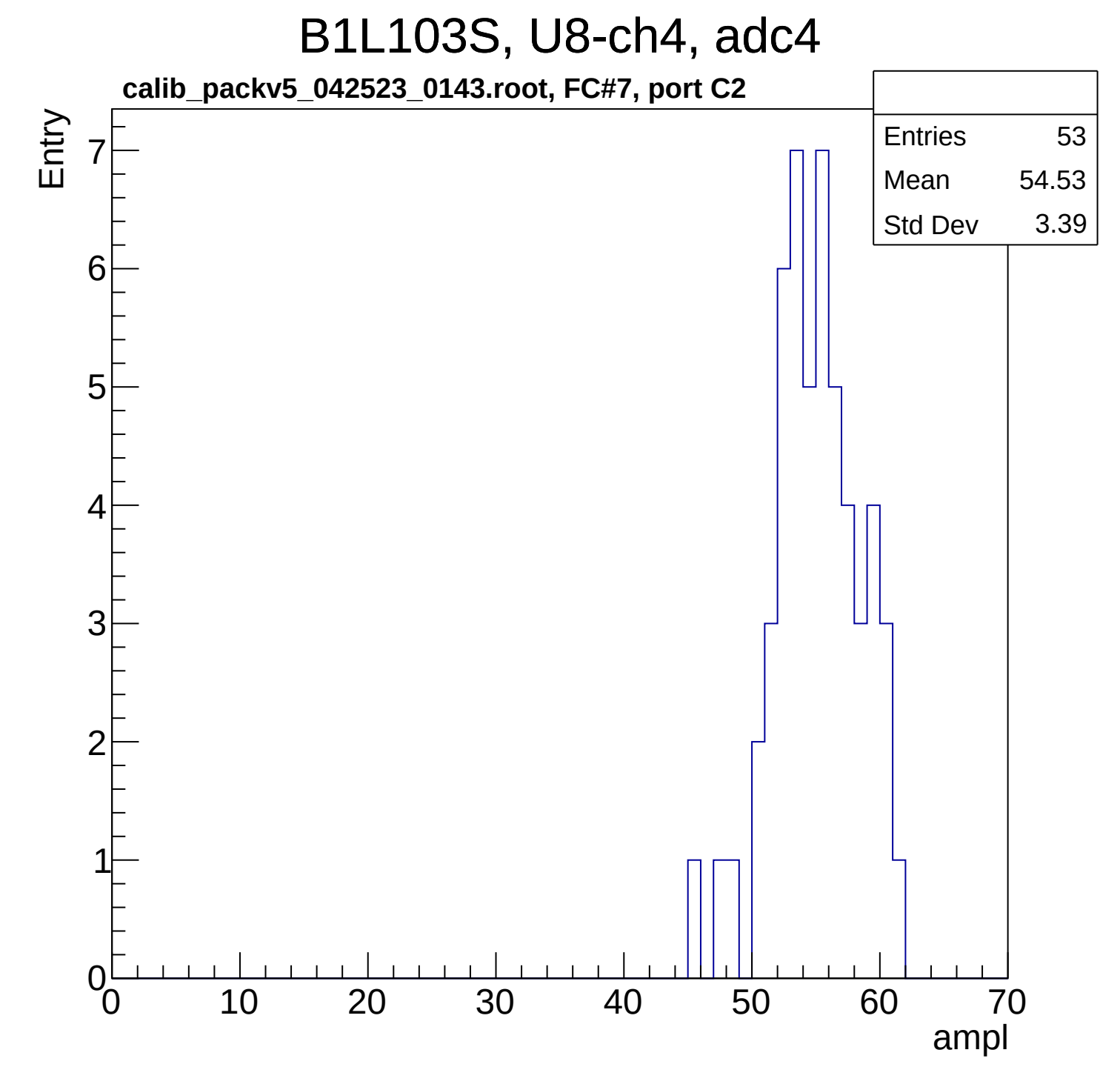

B1L103S, U8-ch3, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 31
Std Dev 31
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

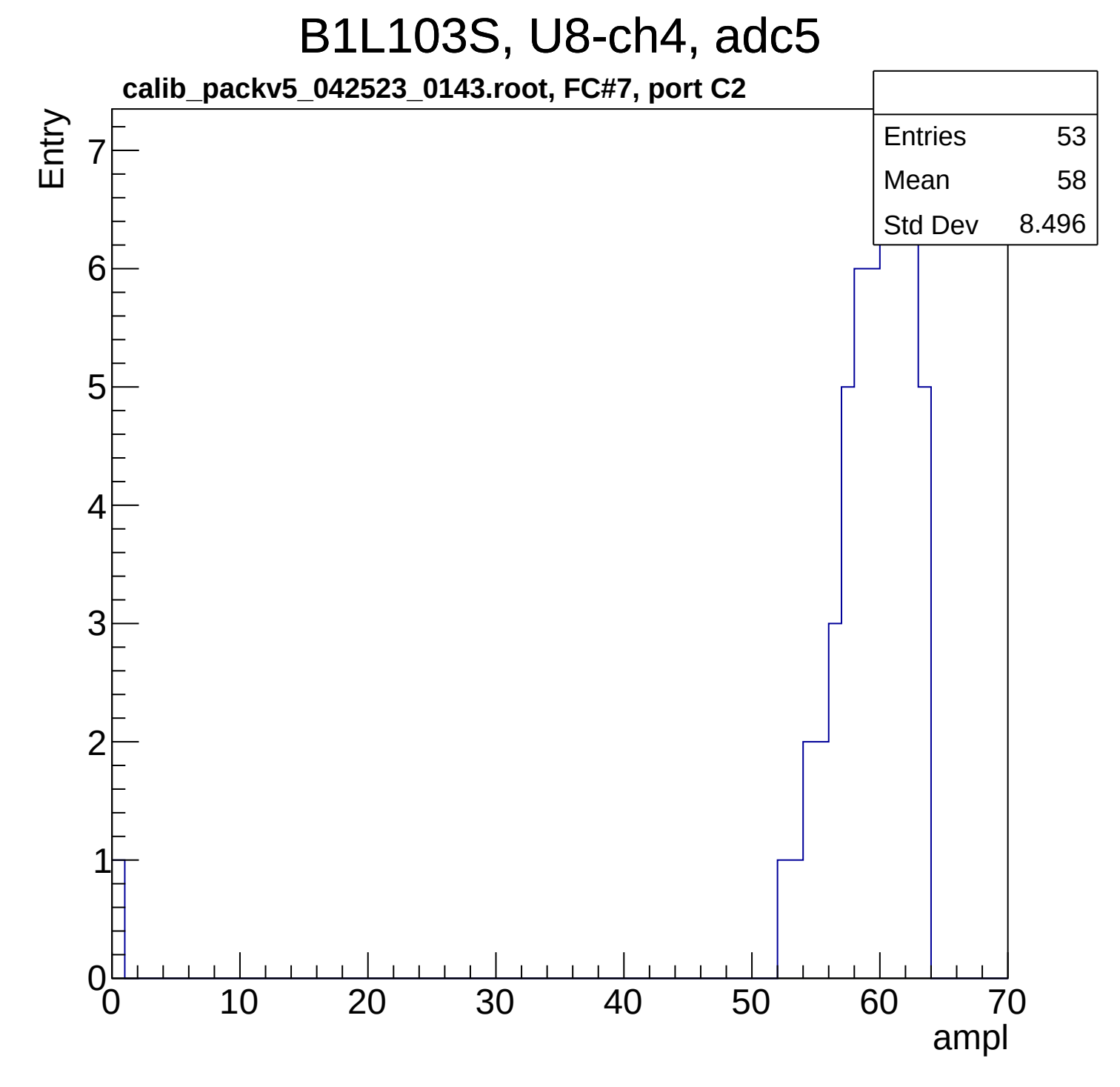

B1L103S, U8-ch4, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 90
Mean 29.13
Std Dev 3.606
Gaus mean : 30.1960
Gaus Width: 4.0250
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

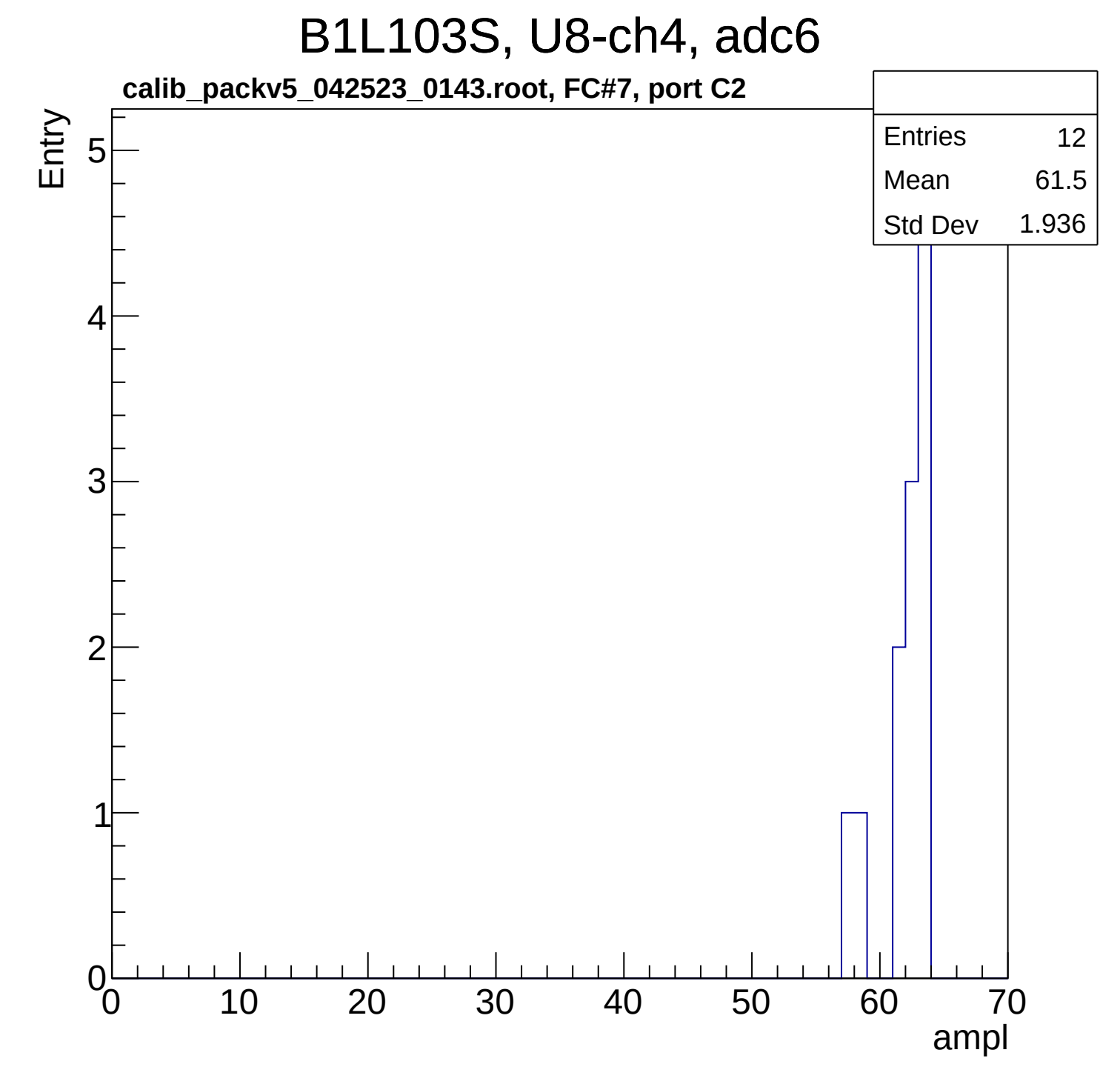

B1L103S, U8-ch4, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 36.85
Std Dev 3.61
Gaus mean : 37.2403
Gaus Width: 5.4059
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

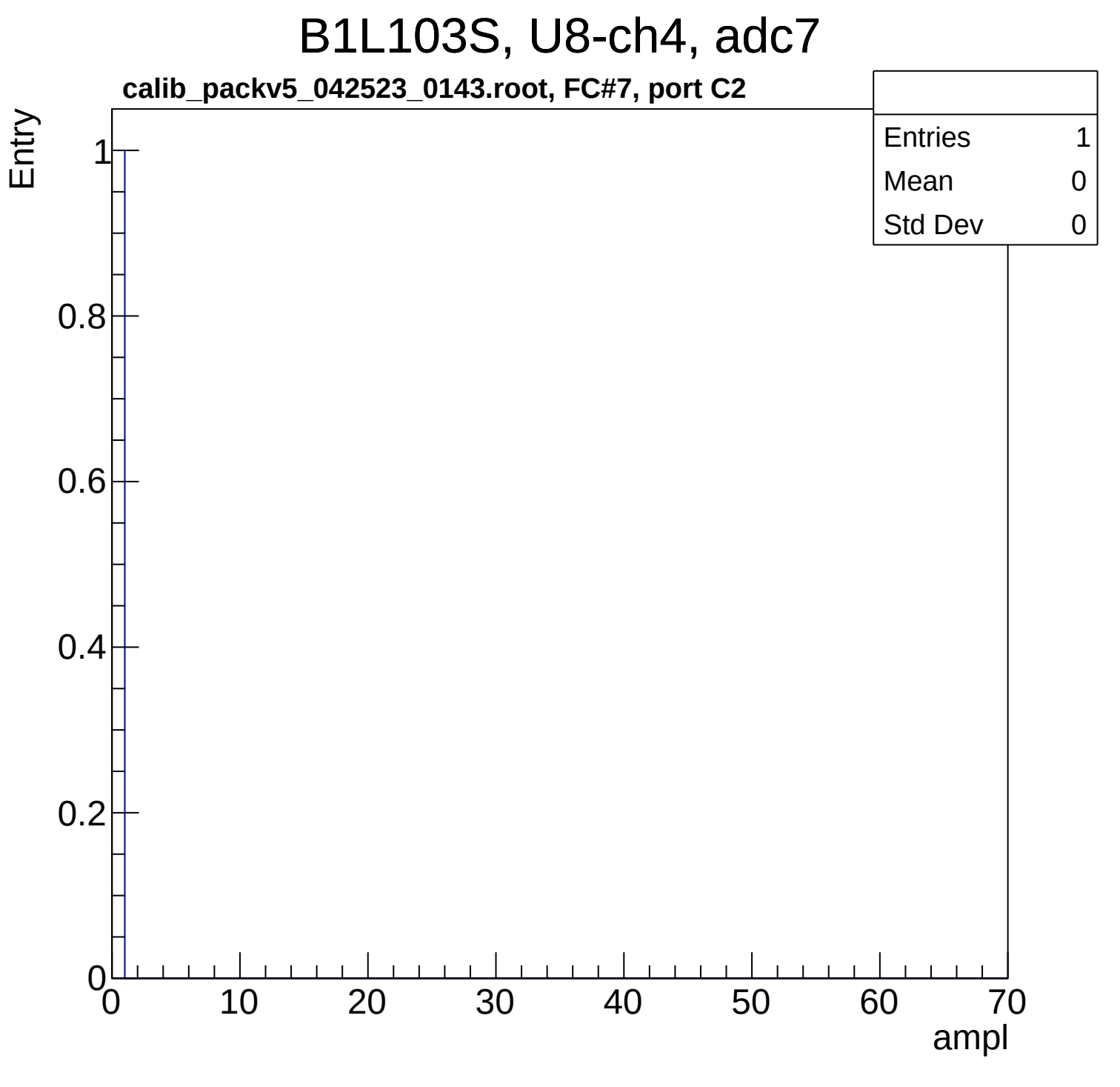

B1L103S, U8-ch4, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 42.04
Std Dev 3.642
Gaus mean : 41.7370
Gaus Width: 4.6928
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

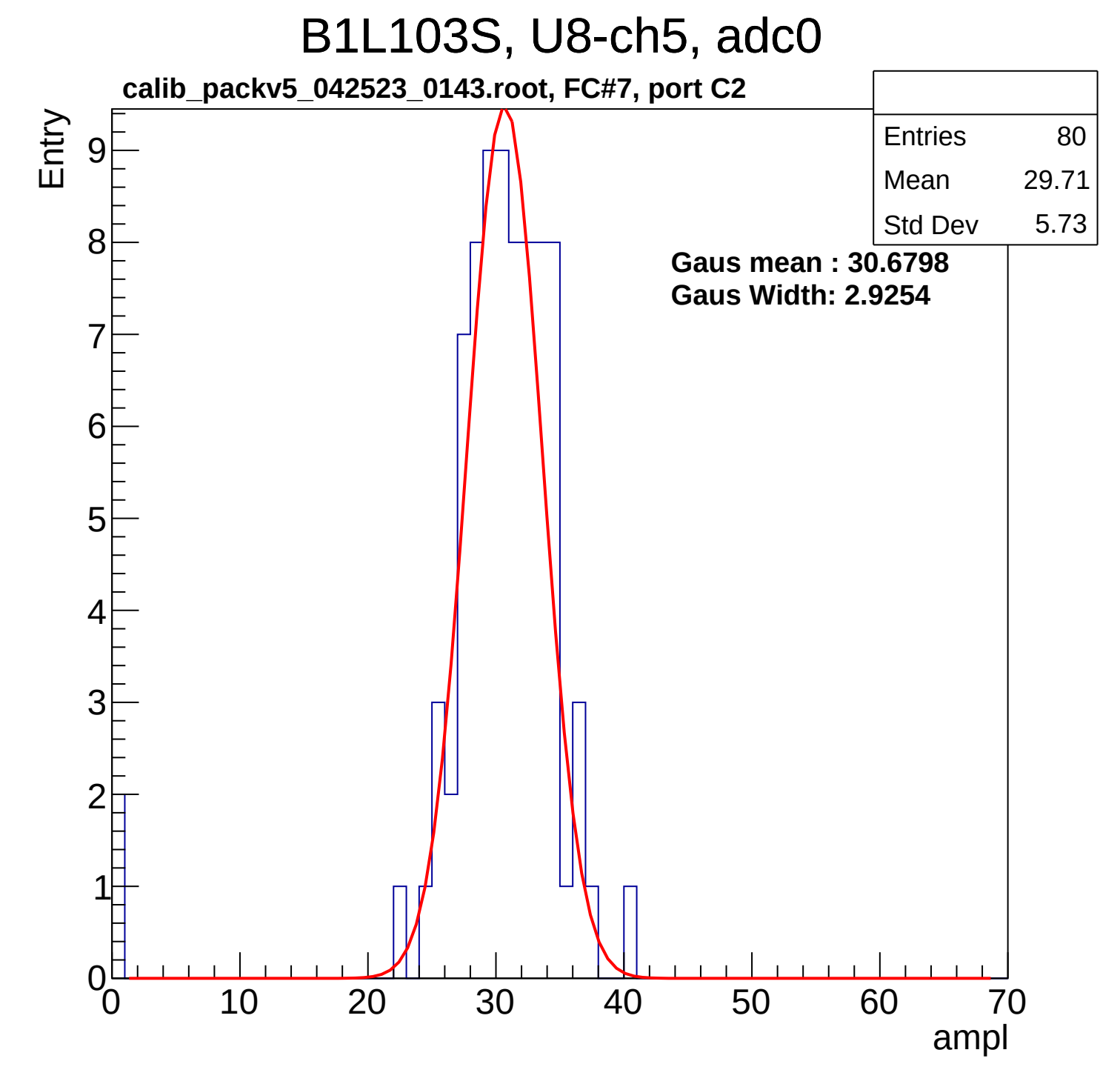

B1L103S, U8-ch4, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 48.17
Std Dev 3.599
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

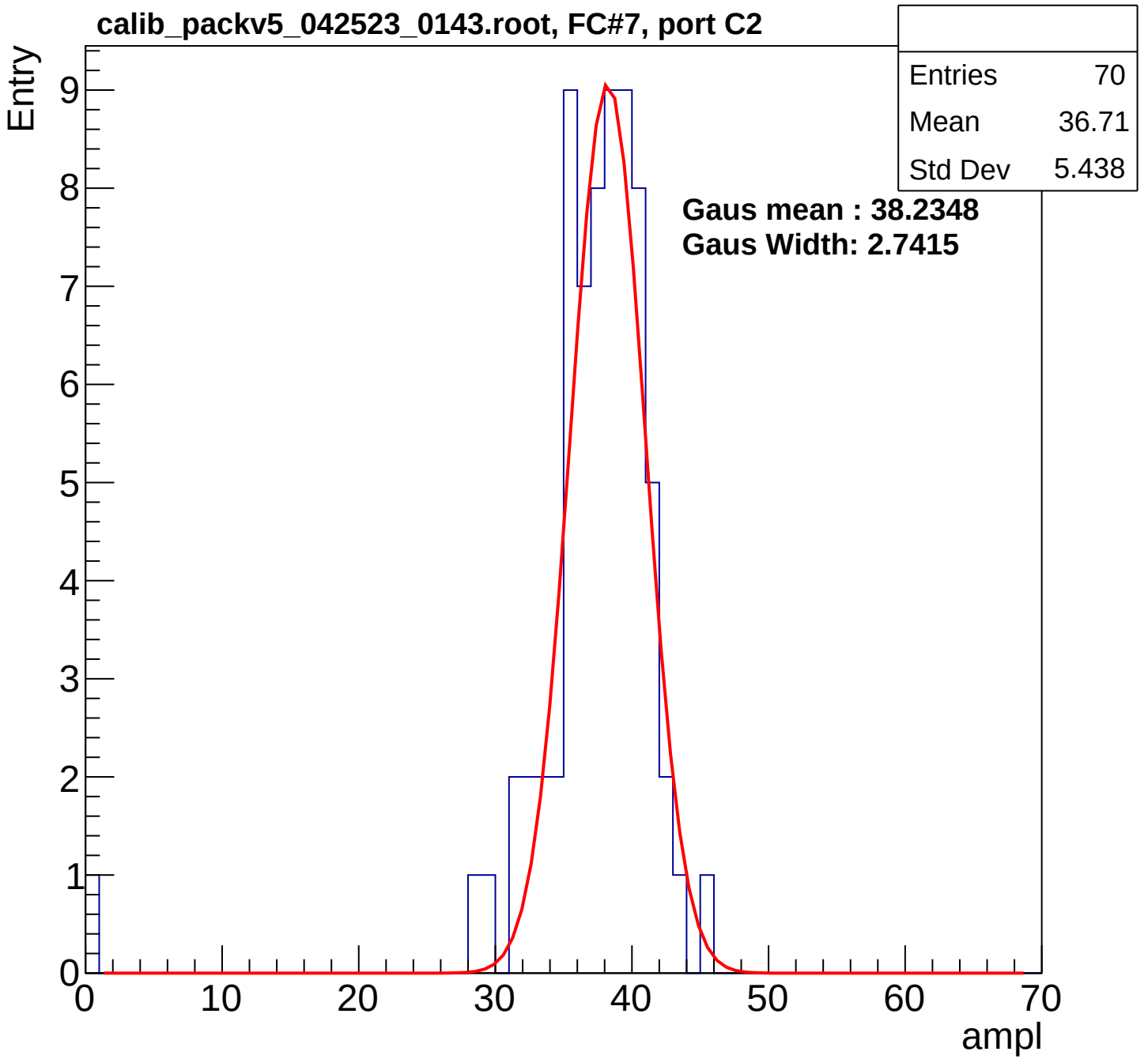

B1L103S, U8-ch4, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 54.53
Std Dev 3.39
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

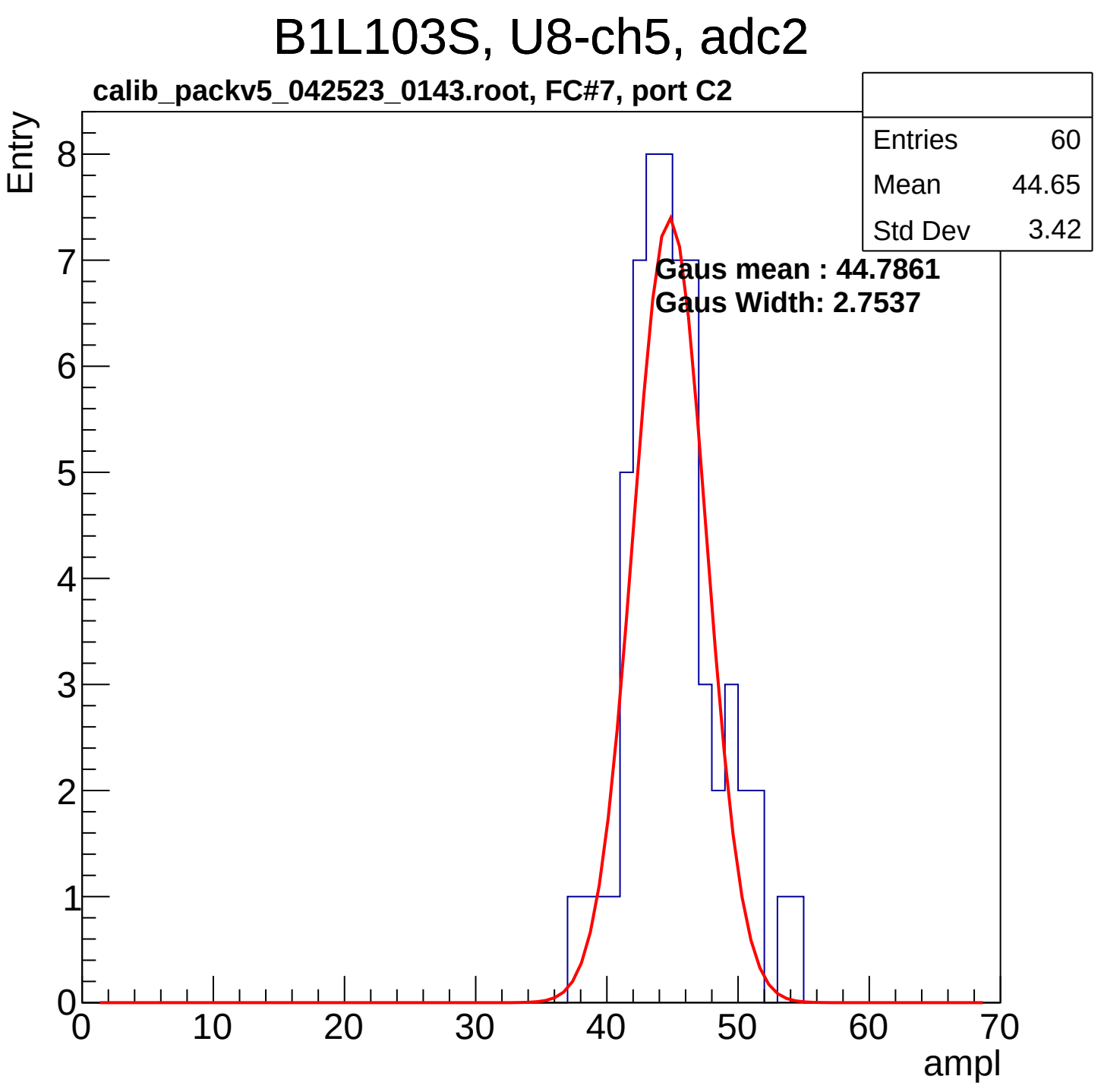

B1L103S, U8-ch4, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 58
Std Dev 8.496
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

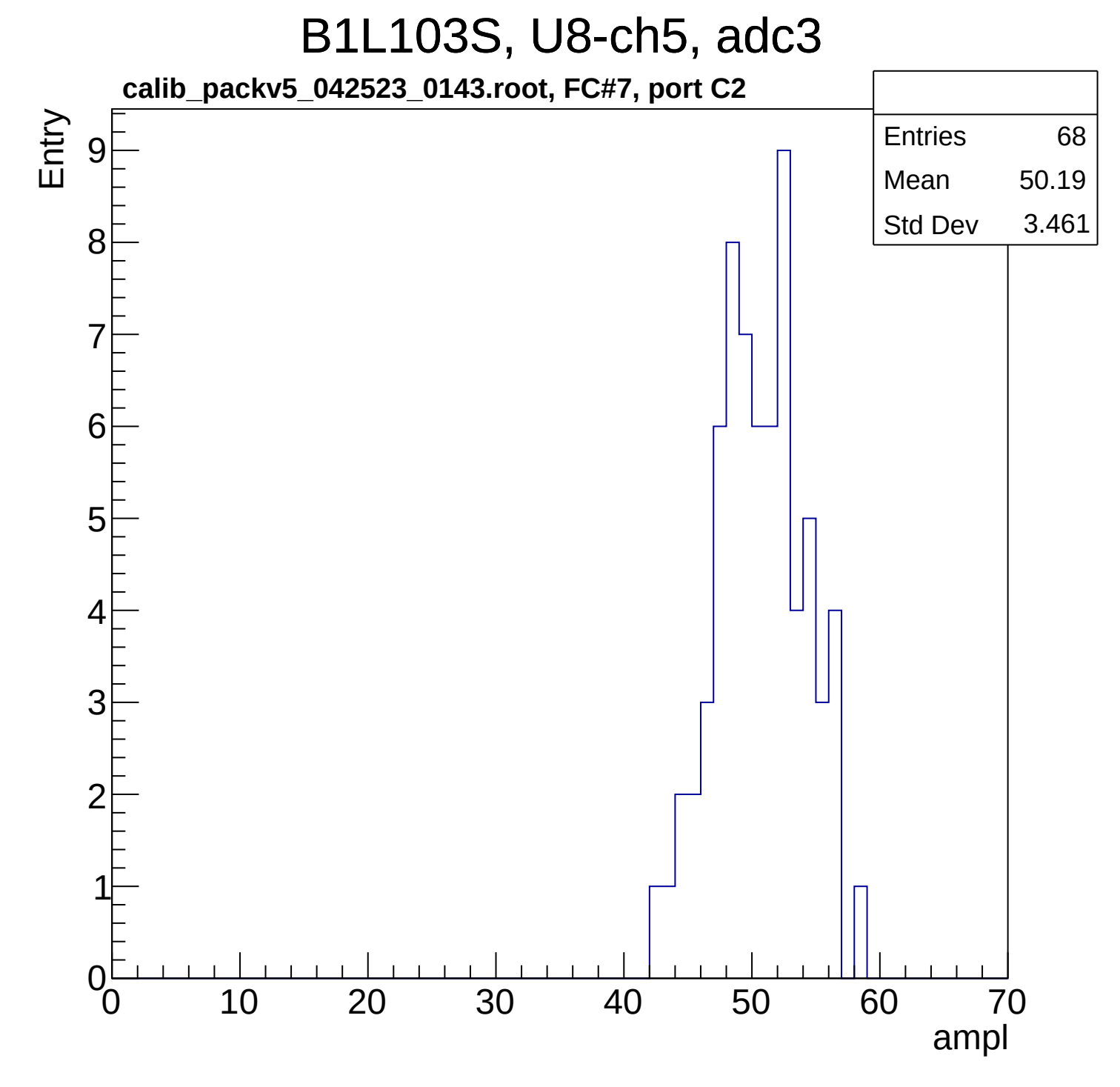

B1L103S, U8-ch4, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 12
Mean 61.5
Std Dev 1.936
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

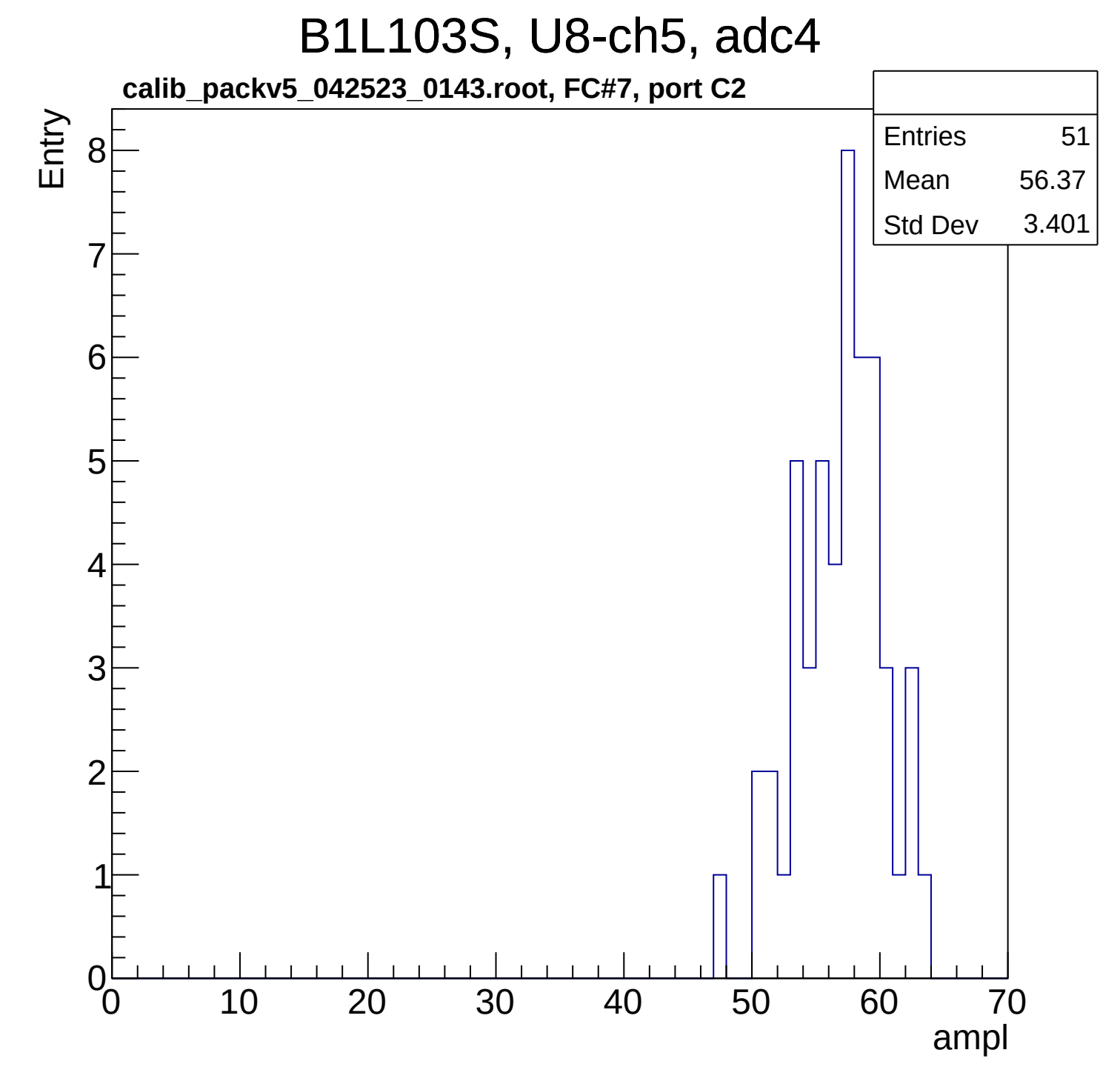

B1L103S, U8-ch4, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

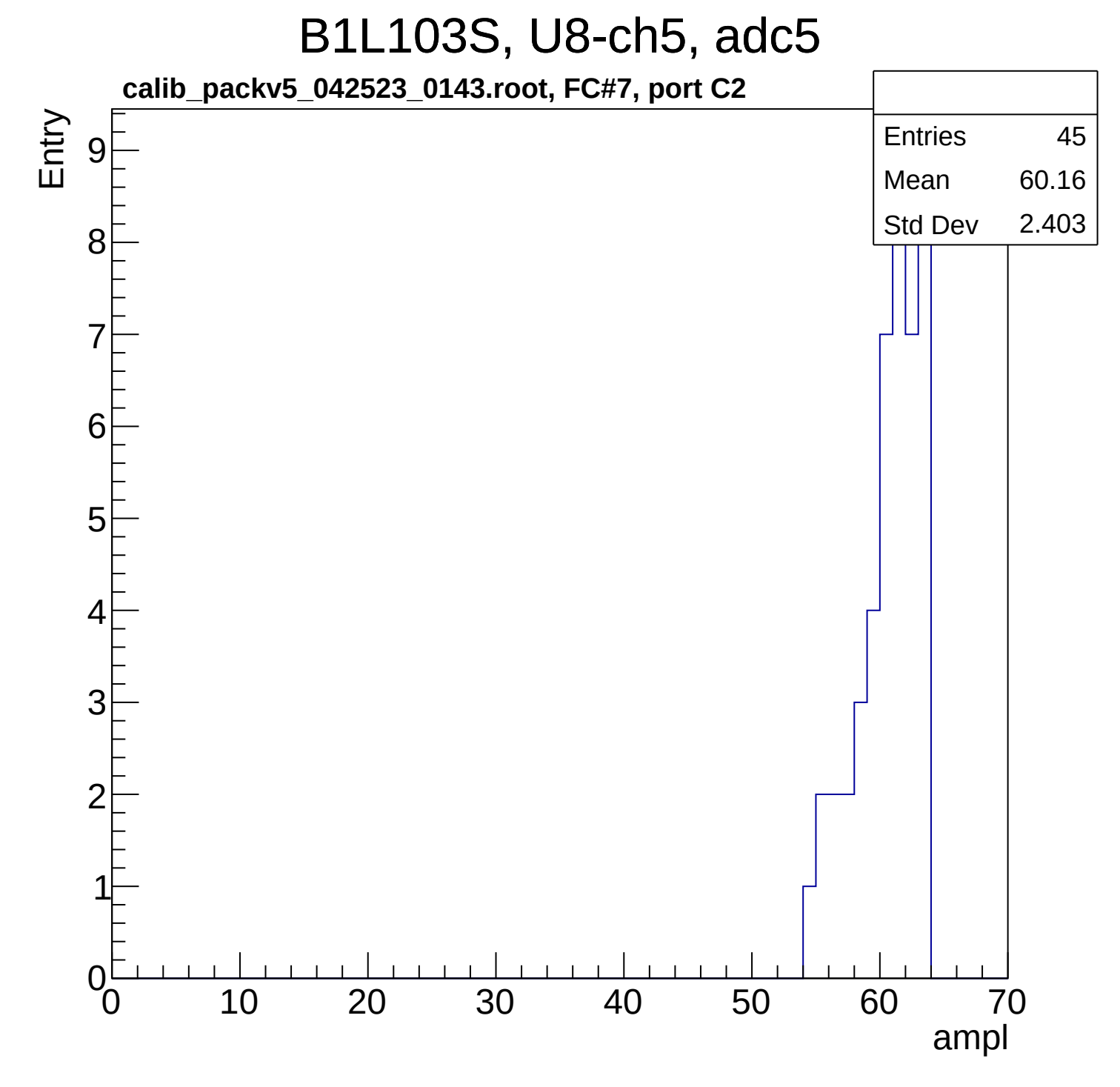

B1L103S, U8-ch5, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 80
Mean 29.71
Std Dev 5.73
Gaus mean : 30.6798
Gaus Width: 2.9254
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

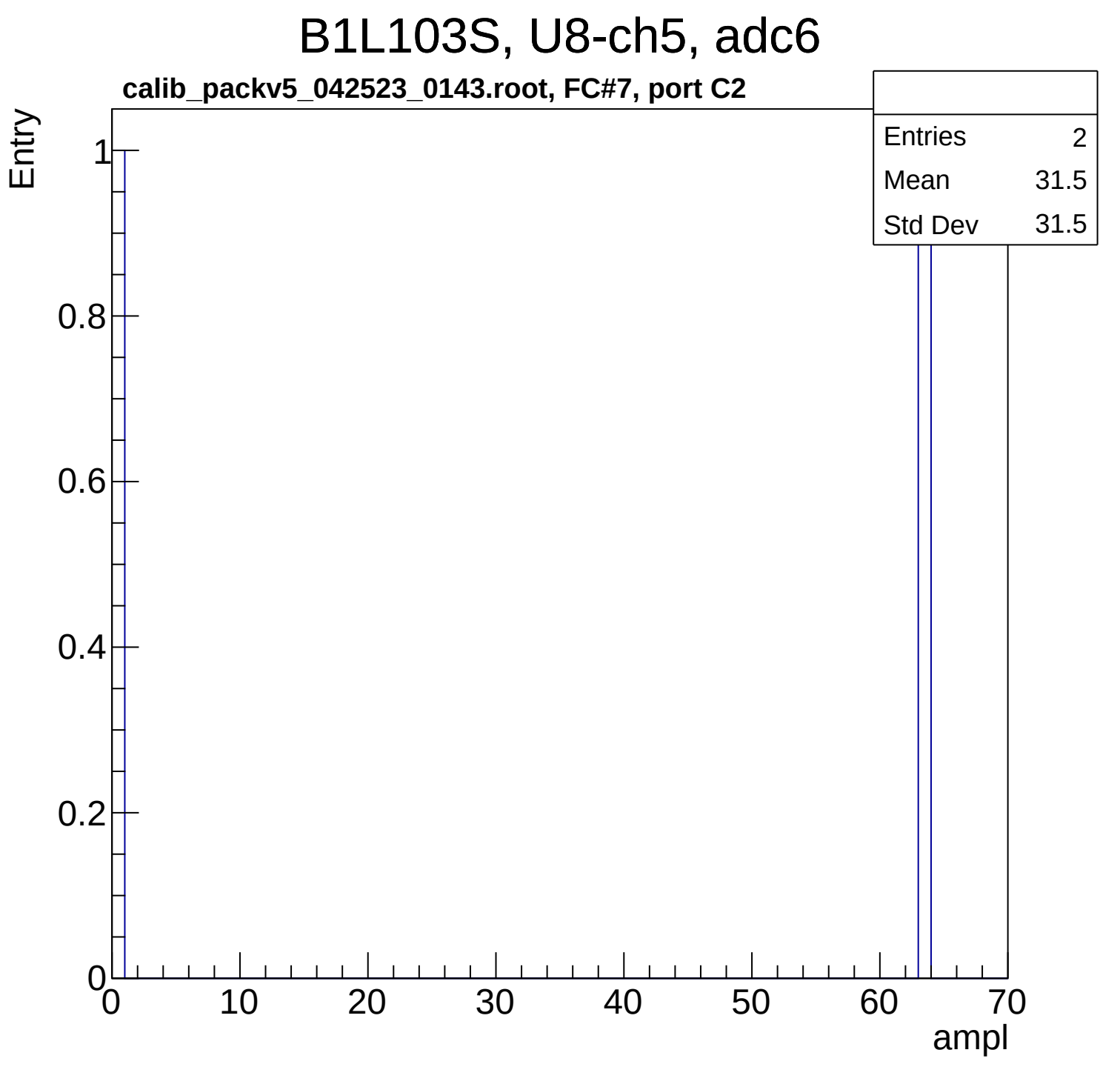

B1L103S, U8-ch5, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 36.71
Std Dev 5.438
Gaus mean : 38.2348
Gaus Width: 2.7415
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

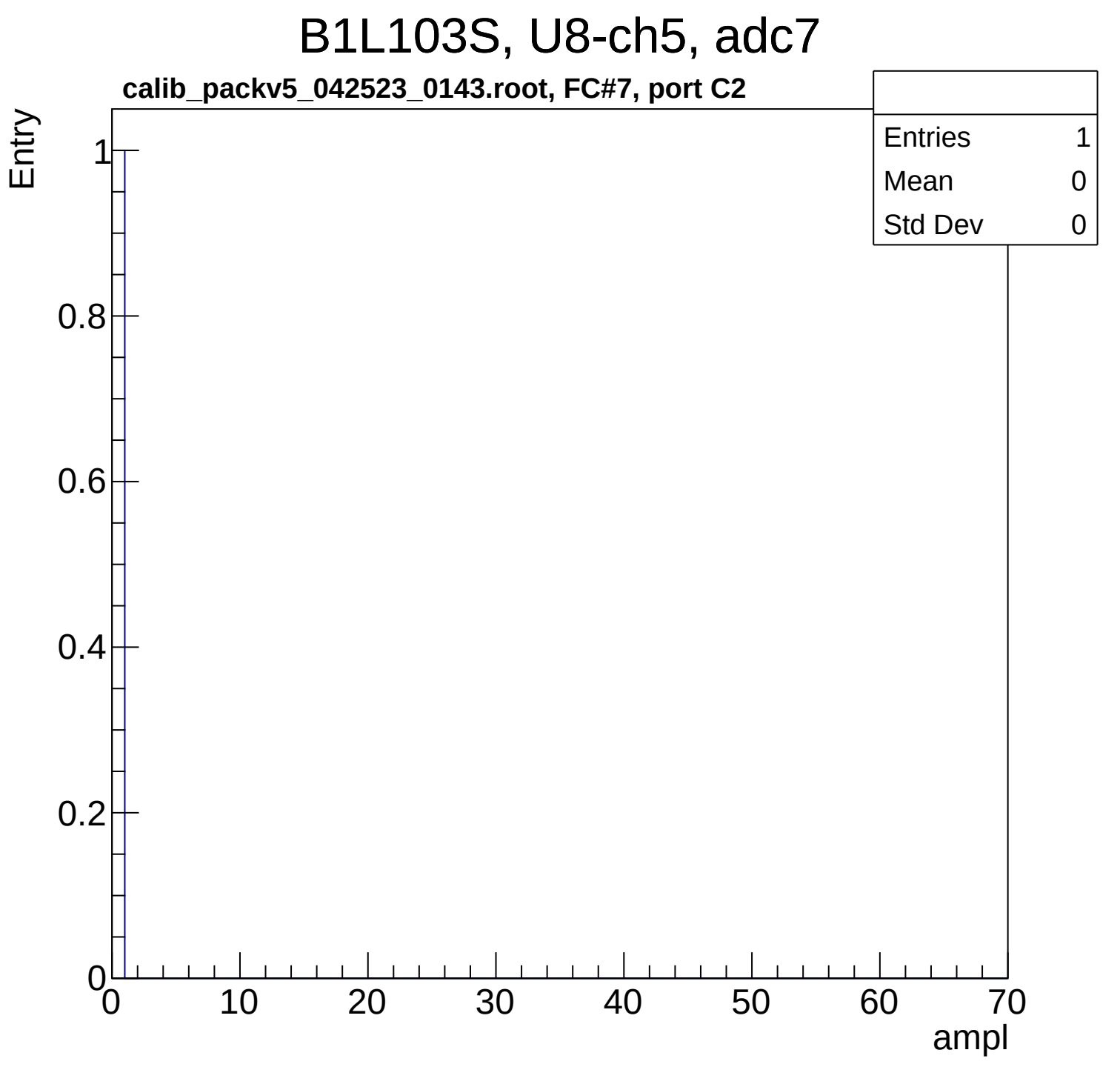

B1L103S, U8-ch5, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 44.65
Std Dev 3.42
Gaus mean : 44.7861
Gaus Width: 2.7537
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

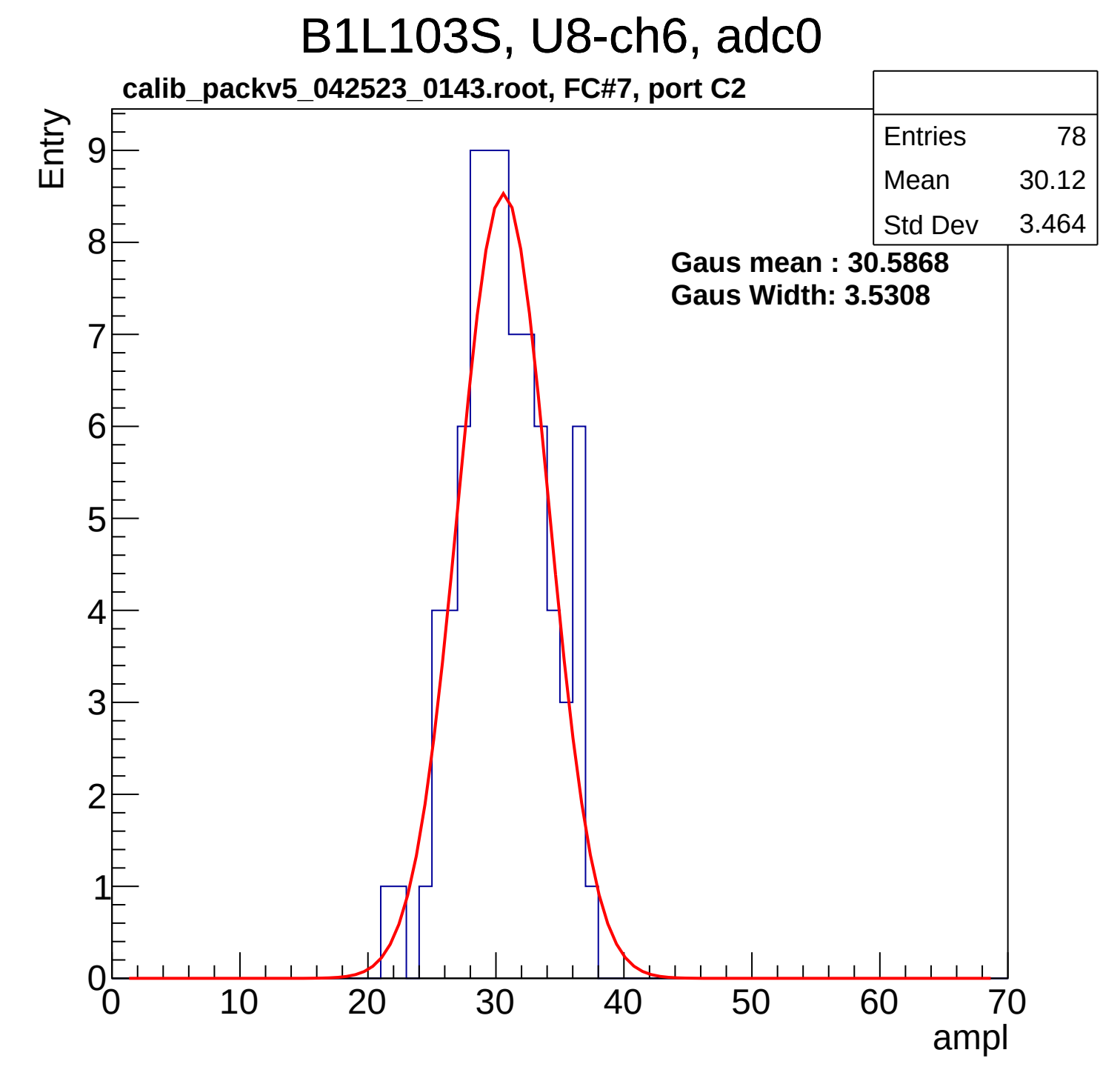

B1L103S, U8-ch5, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 50.19
Std Dev 3.461
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

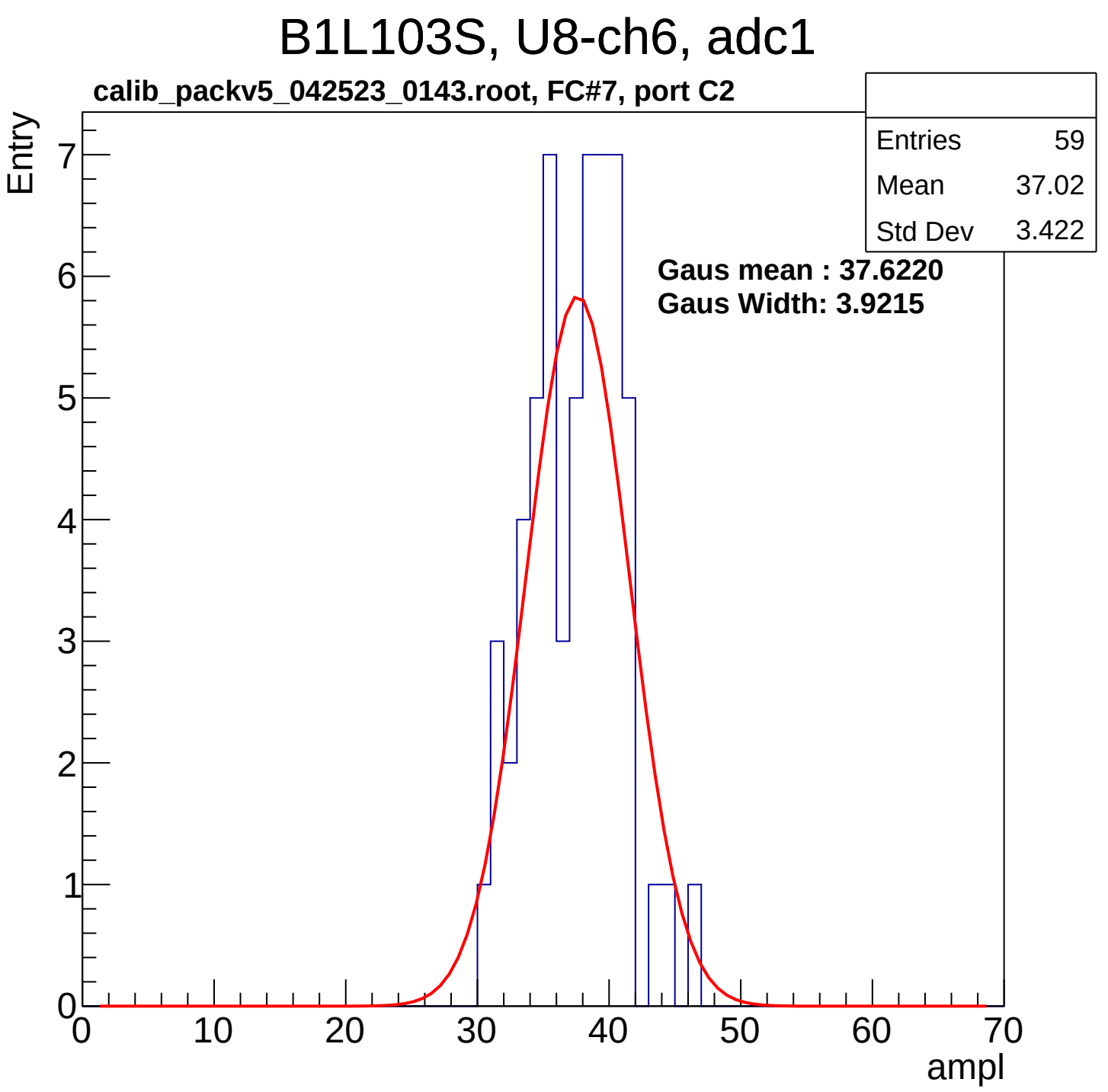

B1L103S, U8-ch5, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 56.37
Std Dev 3.401
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

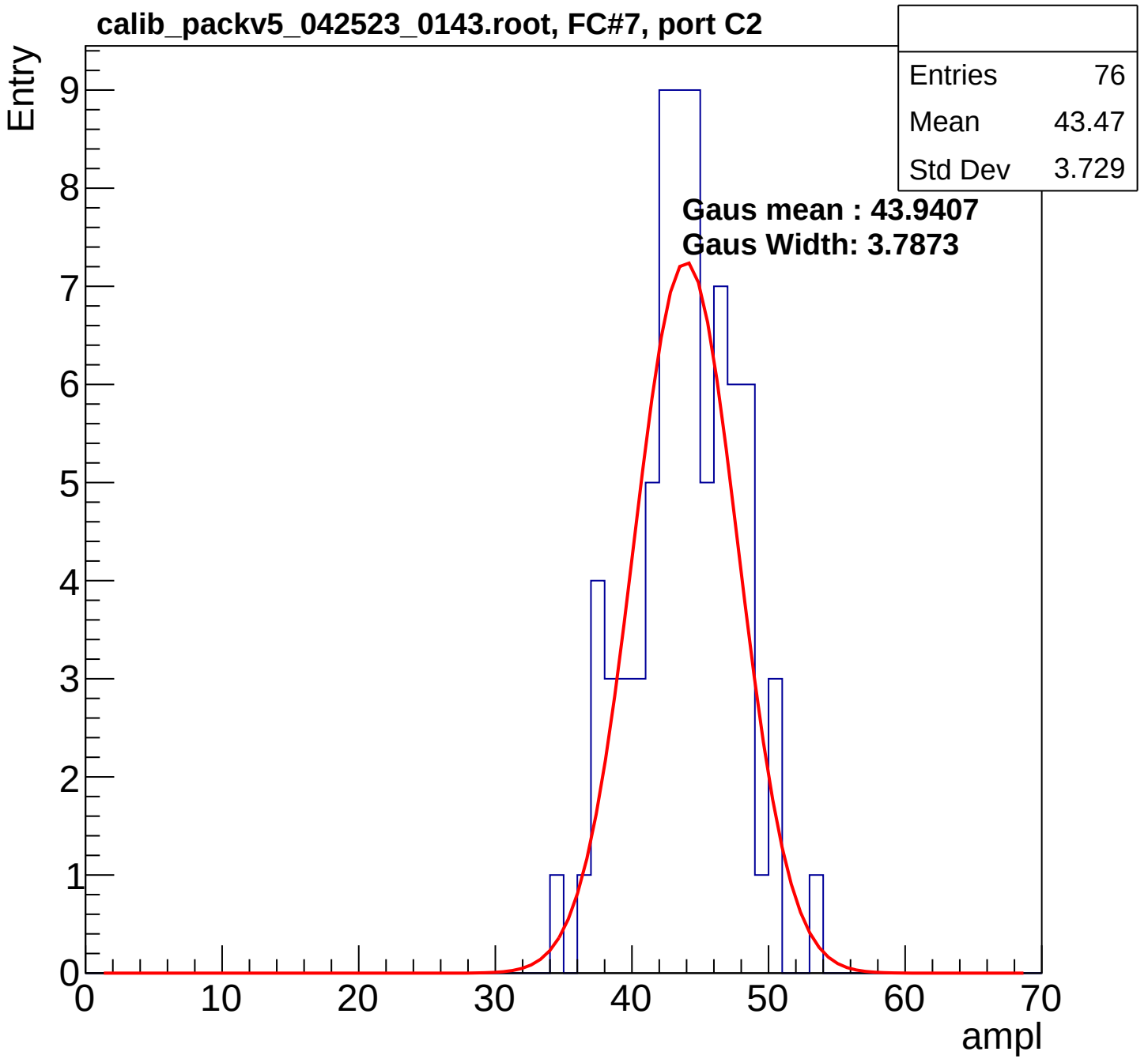

B1L103S, U8-ch5, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 45
Mean 60.16
Std Dev 2.403
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

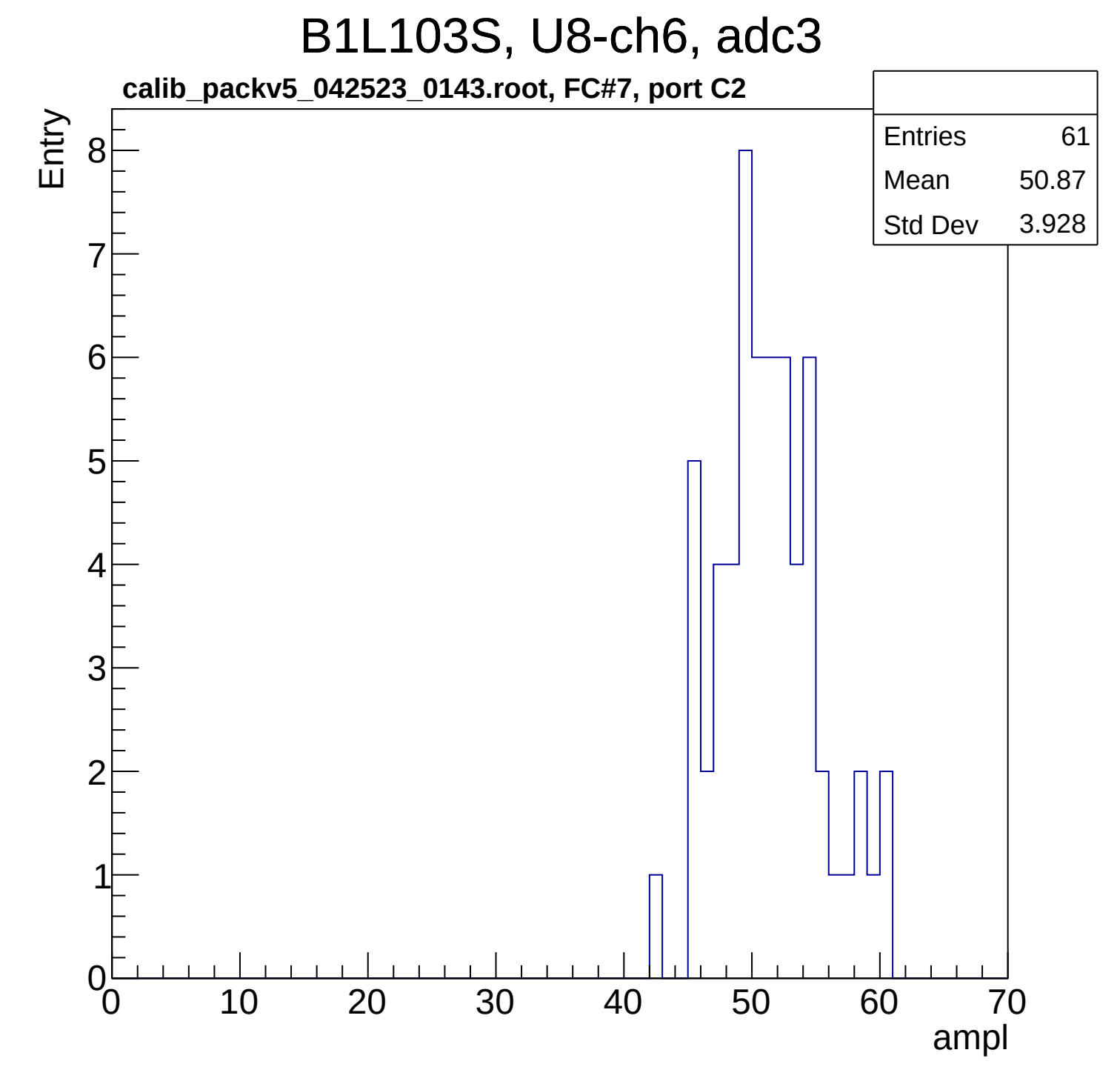

B1L103S, U8-ch5, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

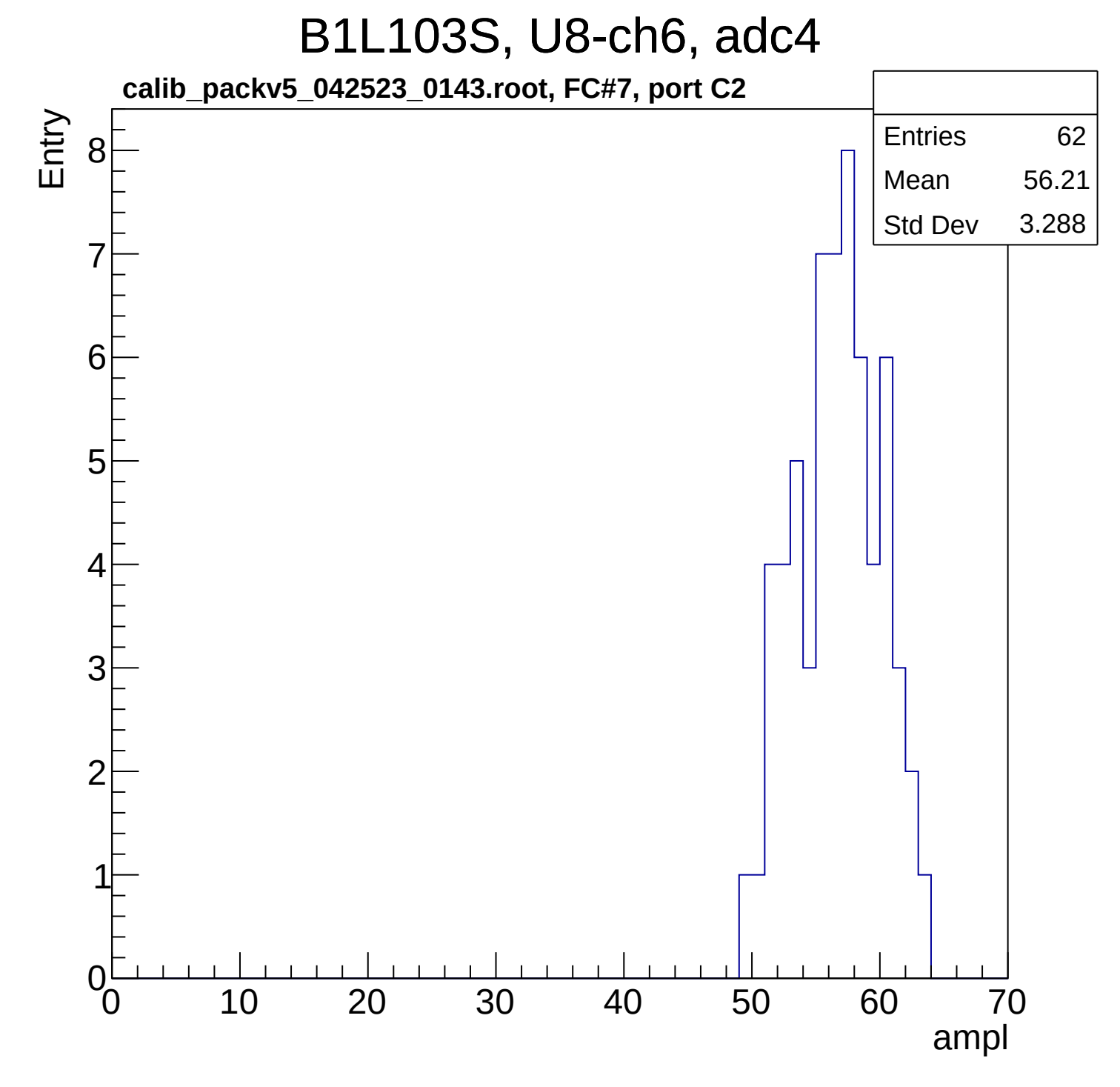

B1L103S, U8-ch5, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

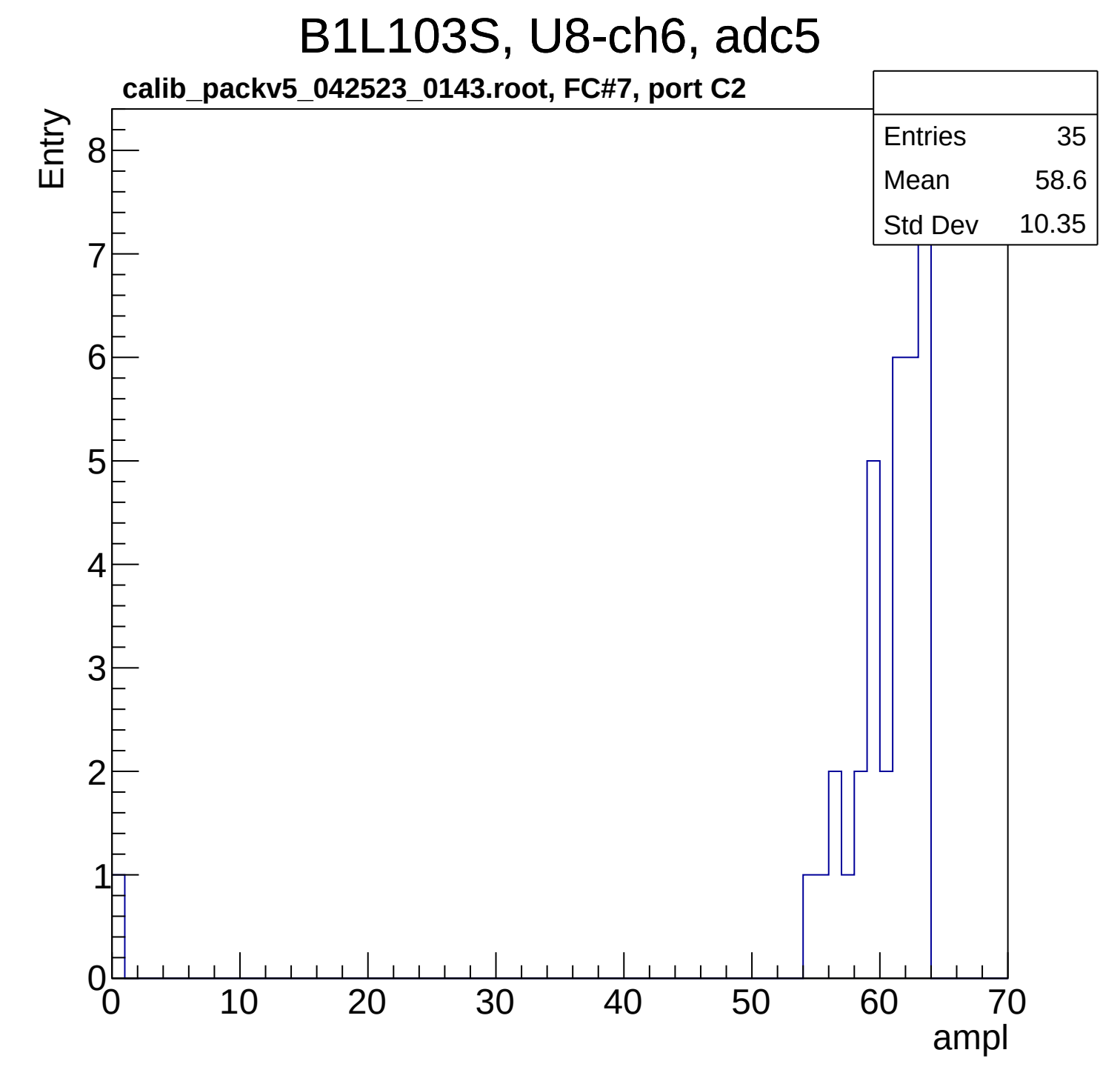

B1L103S, U8-ch6, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 30.12
Std Dev 3.464
Gaus mean : 30.5868
Gaus Width: 3.5308
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

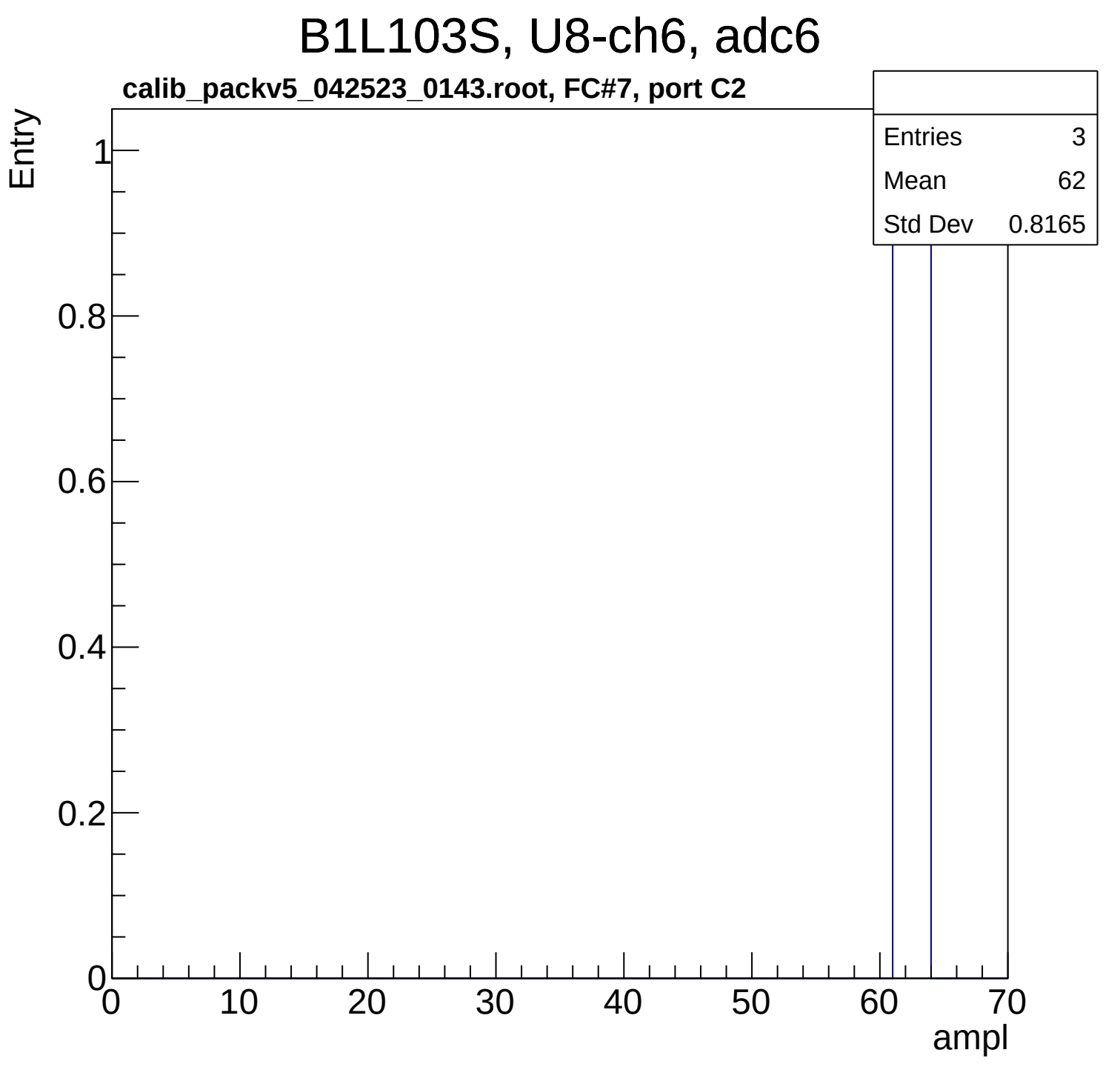

B1L103S, U8-ch6, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 37.02
Std Dev 3.422
Gaus mean : 37.6220
Gaus Width: 3.9215
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

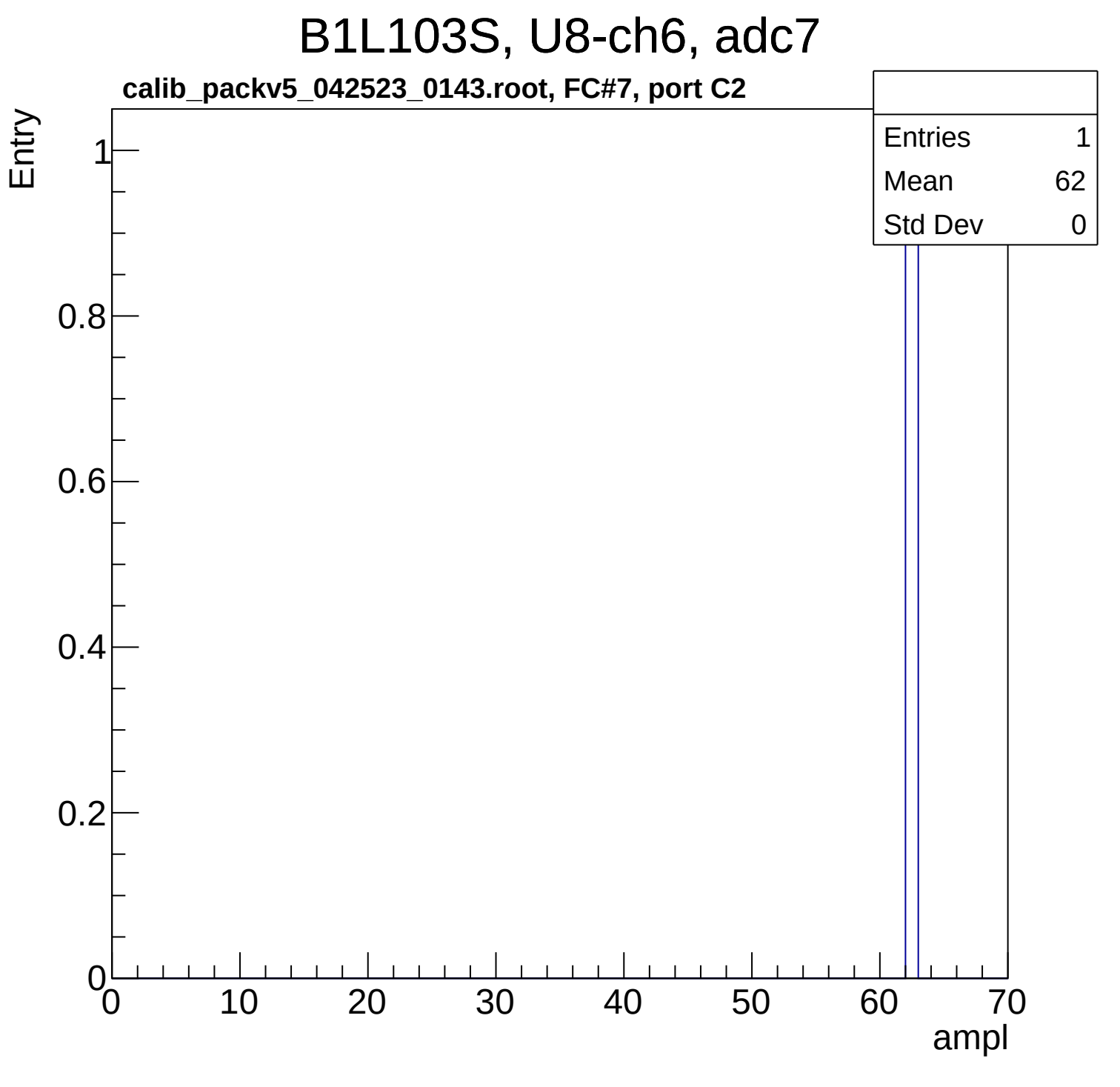

B1L103S, U8-ch6, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 76
Mean 43.47
Std Dev 3.729
Gaus mean : 43.9407
Gaus Width: 3.7873
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

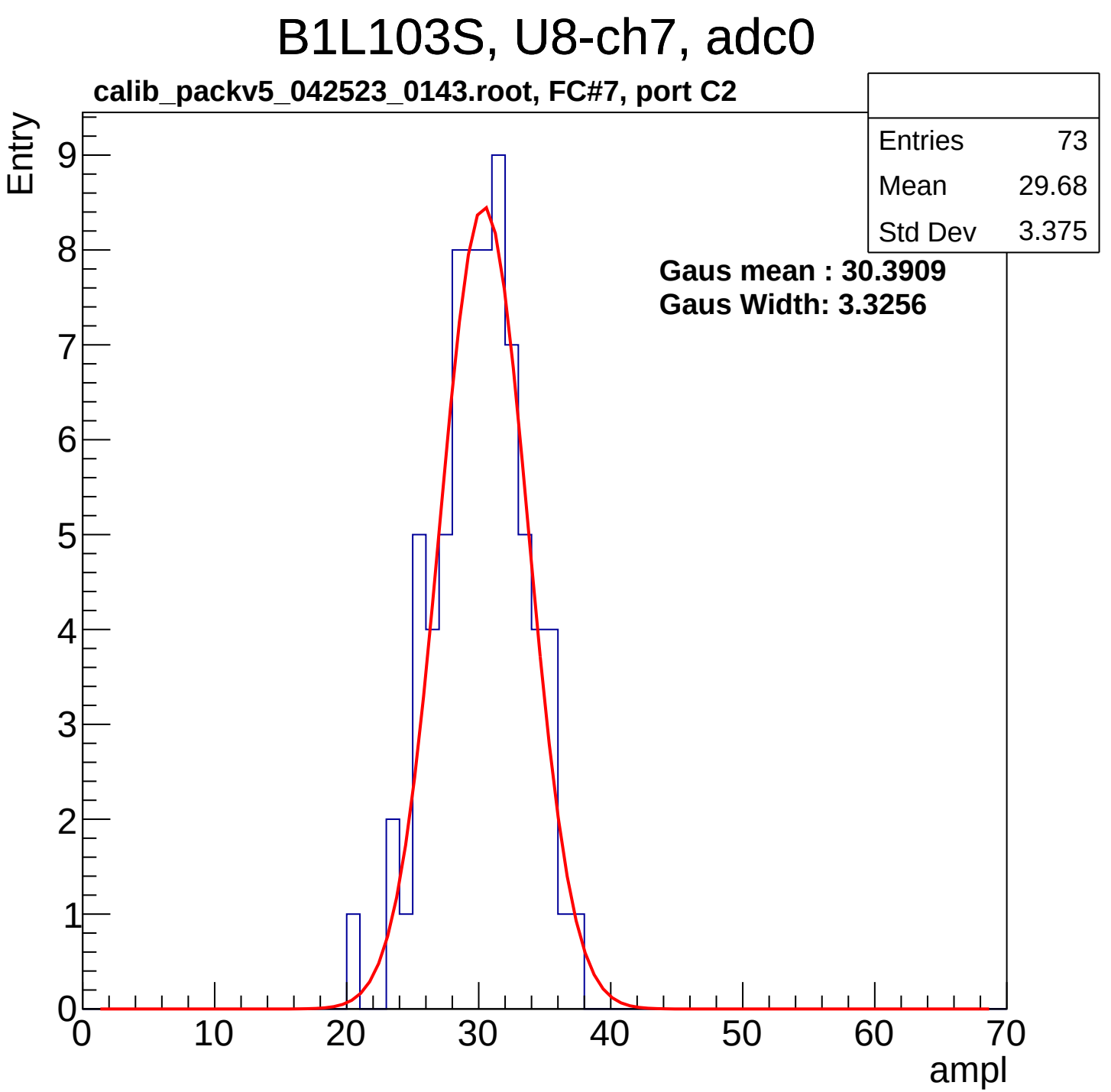

B1L103S, U8-ch6, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 50.87
Std Dev 3.928
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

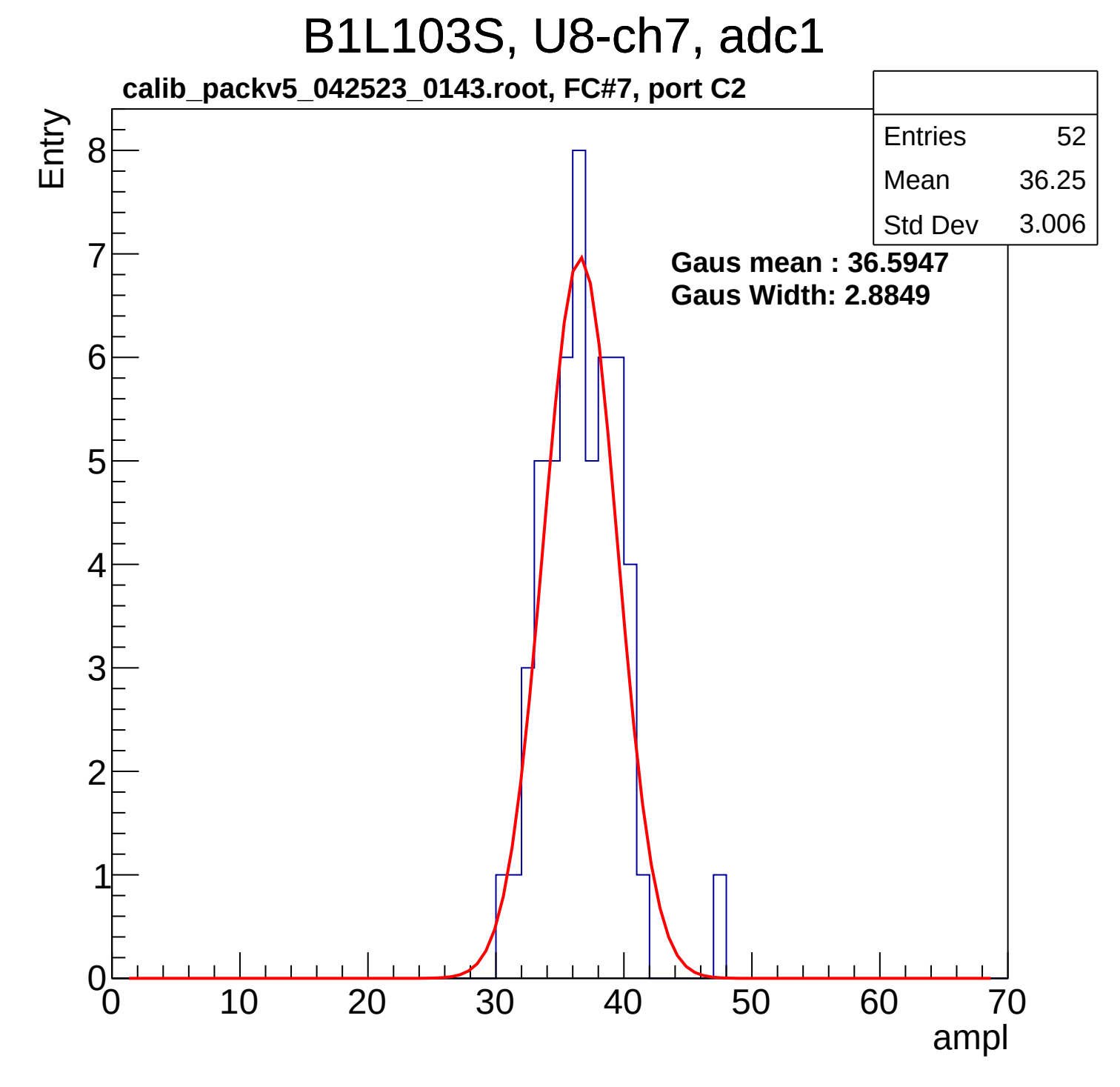

B1L103S, U8-ch6, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 56.21
Std Dev 3.288
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

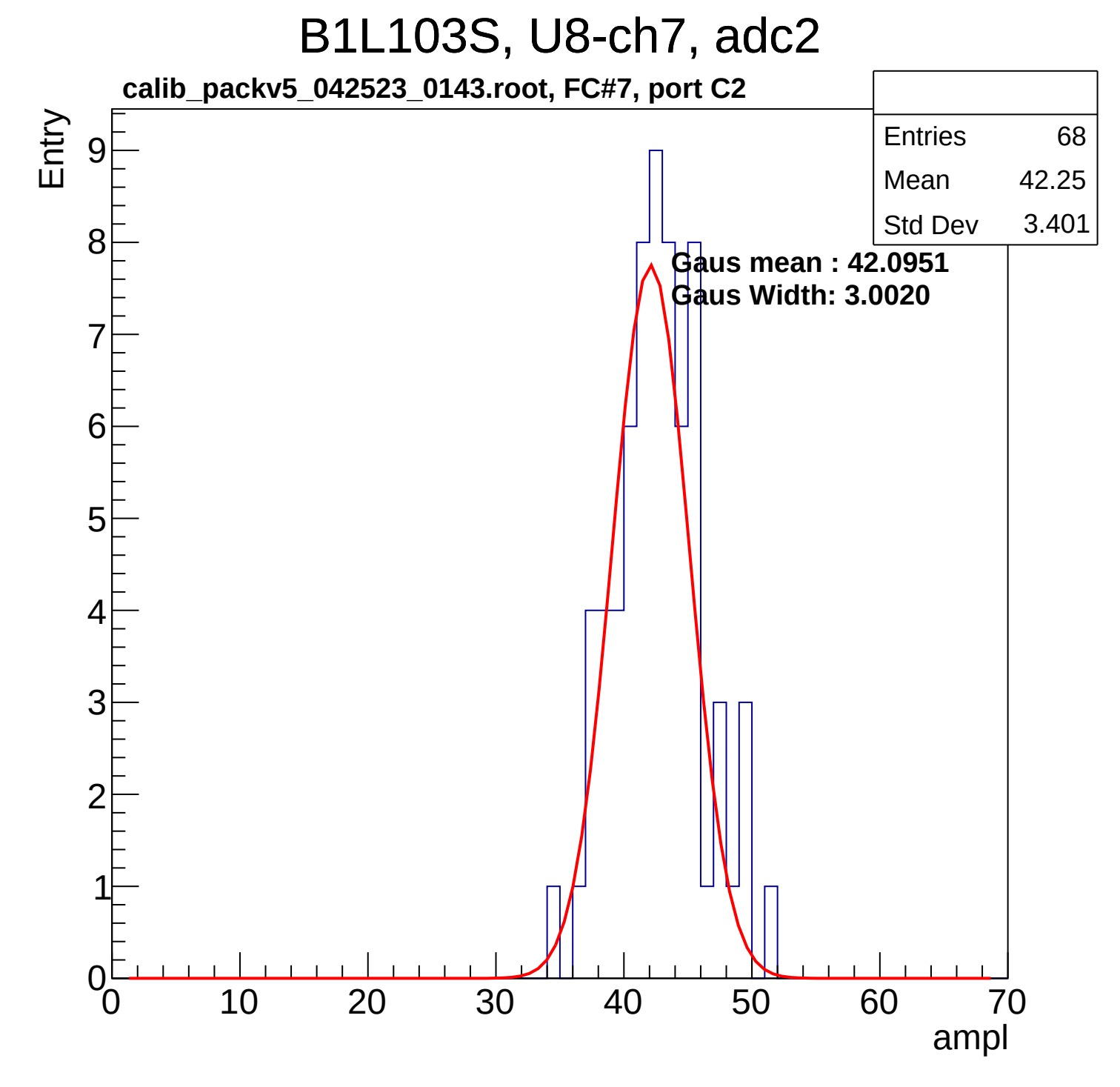

B1L103S, U8-ch6, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 35
Mean 58.6
Std Dev 10.35
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

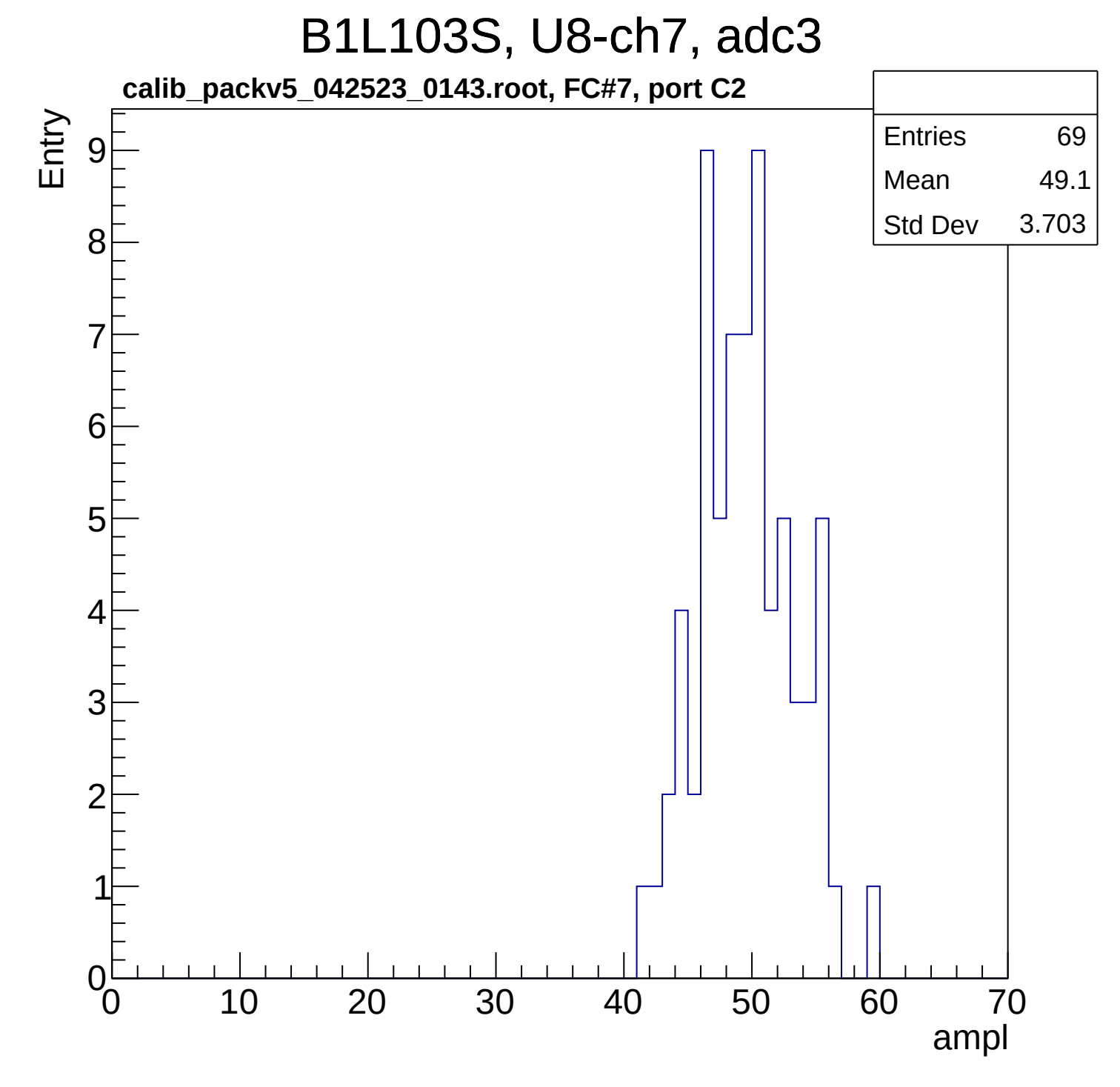

B1L103S, U8-ch6, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 62
Std Dev 0.8165
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

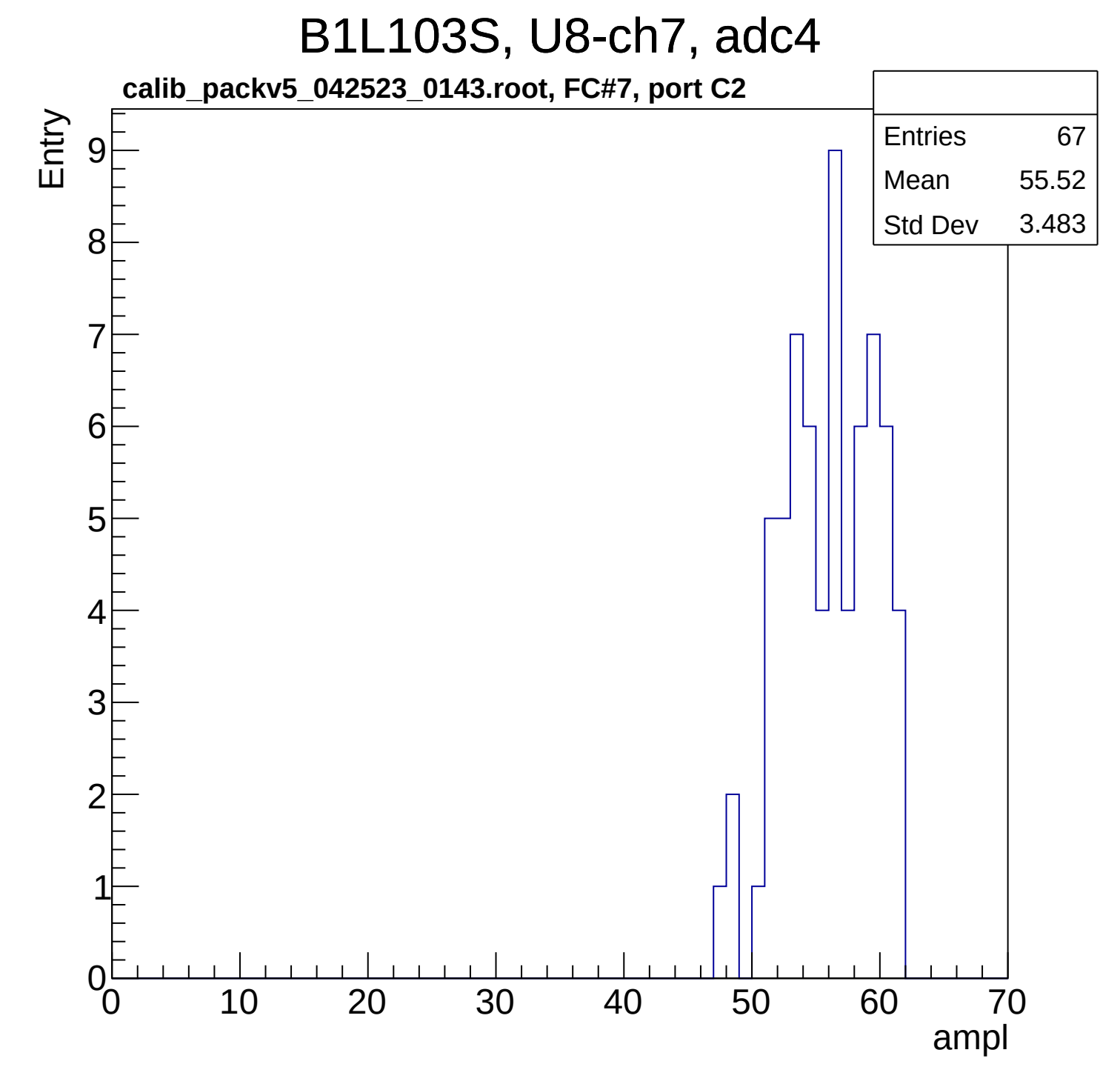

B1L103S, U8-ch6, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

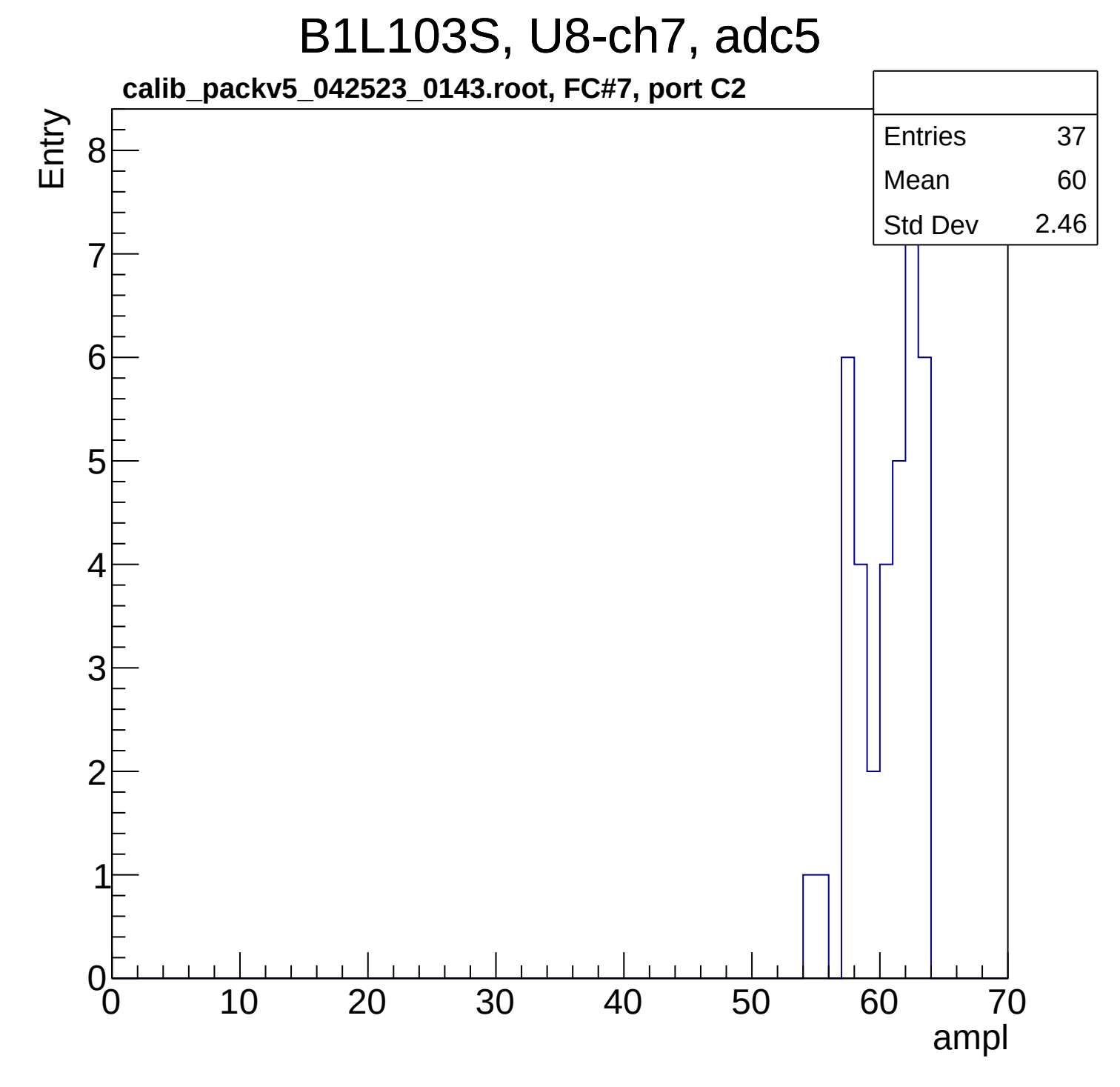

B1L103S, U8-ch7, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 29.68
Std Dev 3.375
Gaus mean : 30.3909
Gaus Width: 3.3256
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

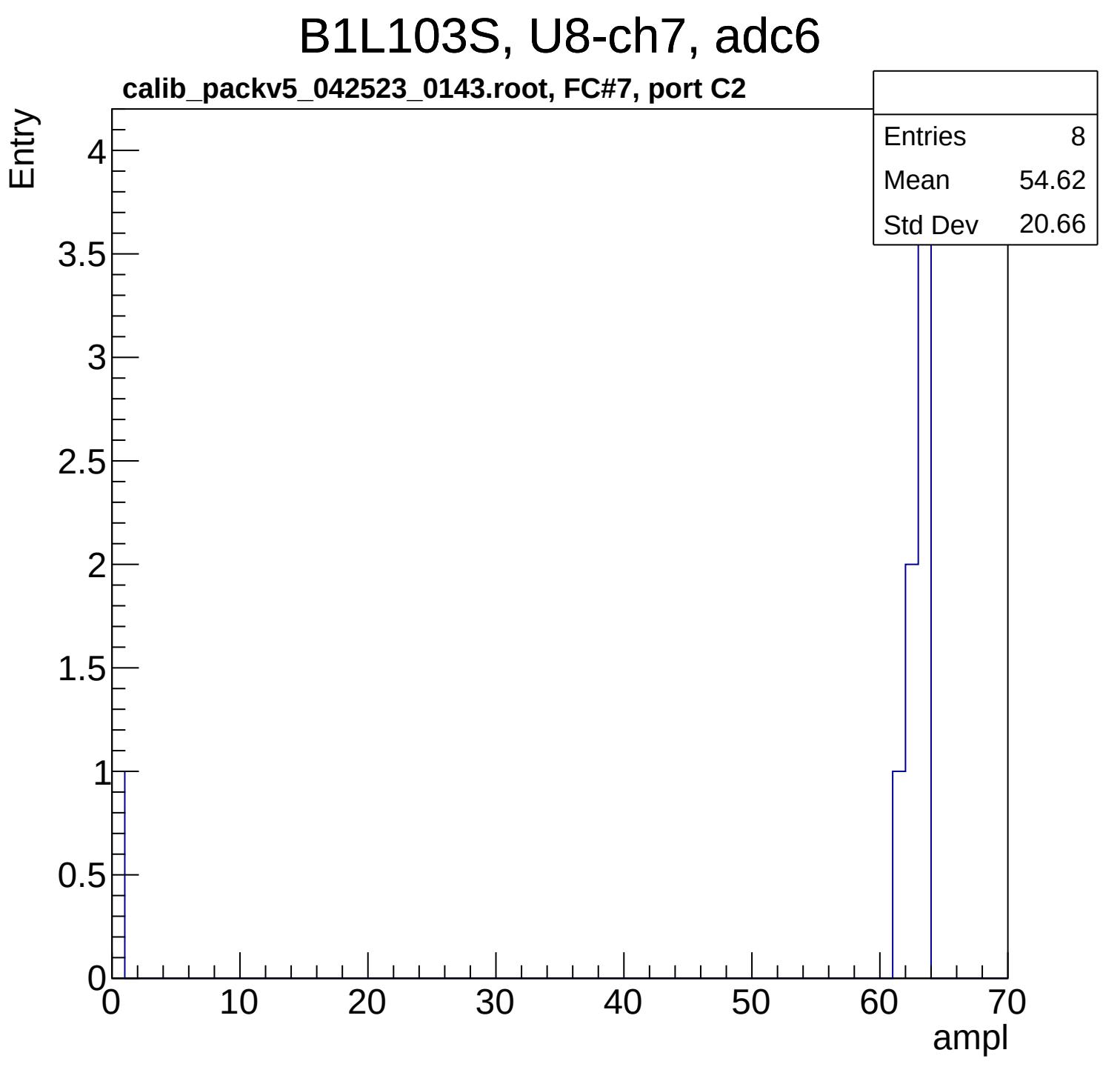

B1L103S, U8-ch7, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 36.25
Std Dev 3.006
Gaus mean : 36.5947
Gaus Width: 2.8849
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

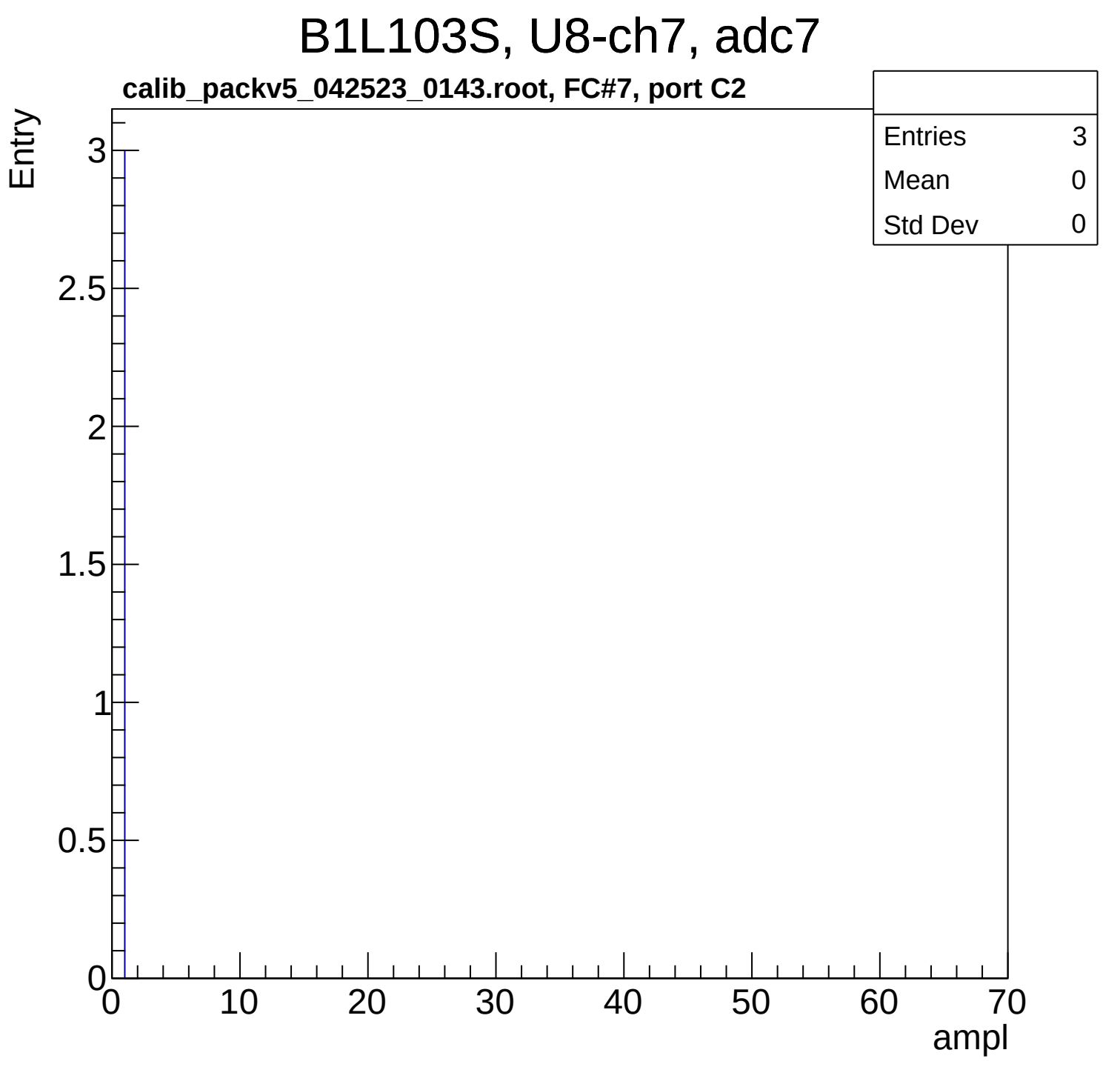

B1L103S, U8-ch7, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 42.25
Std Dev 3.401
Gaus mean : 42.0951
Gaus Width: 3.0020
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

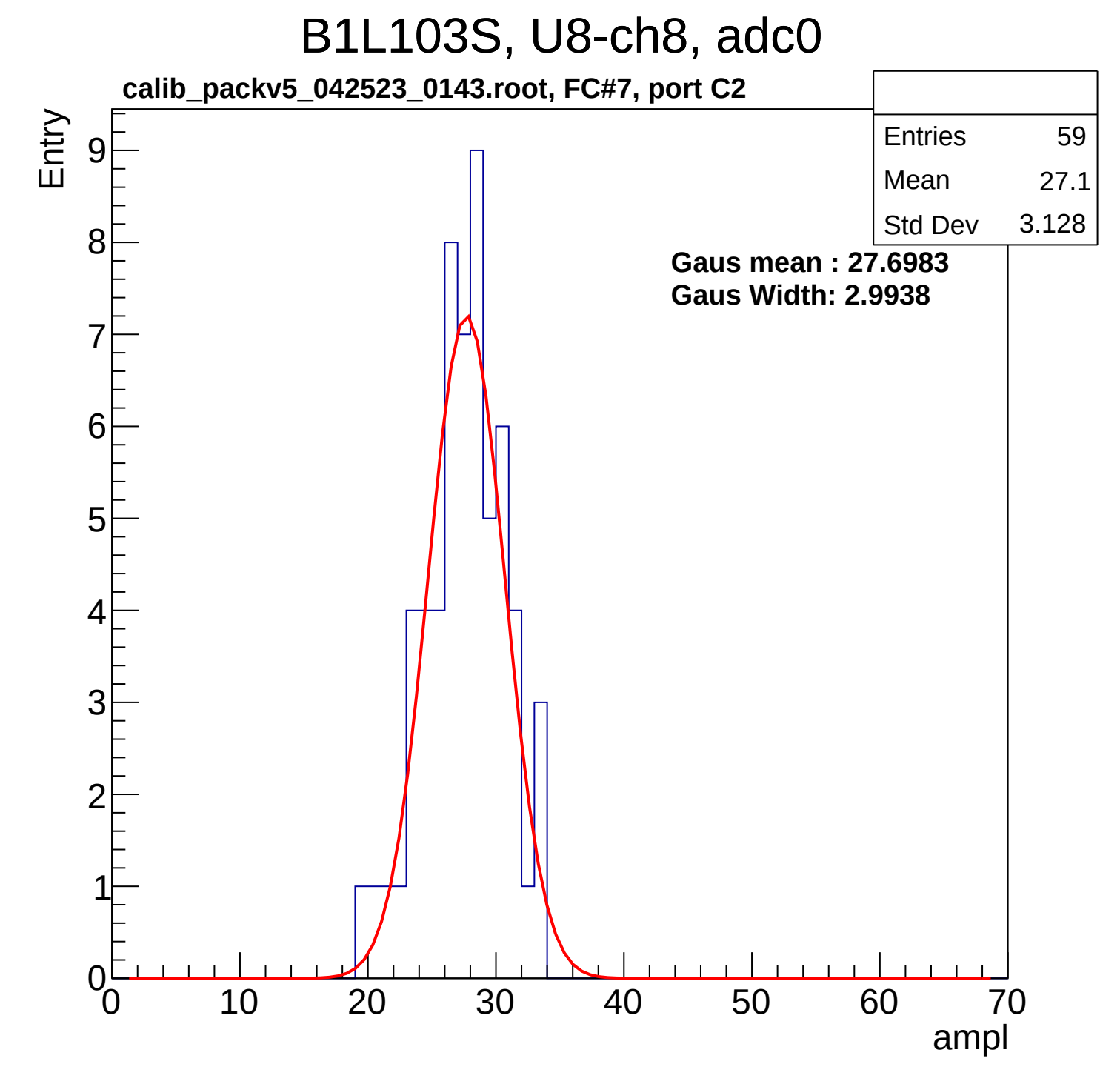

B1L103S, U8-ch7, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 49.1
Std Dev 3.703
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

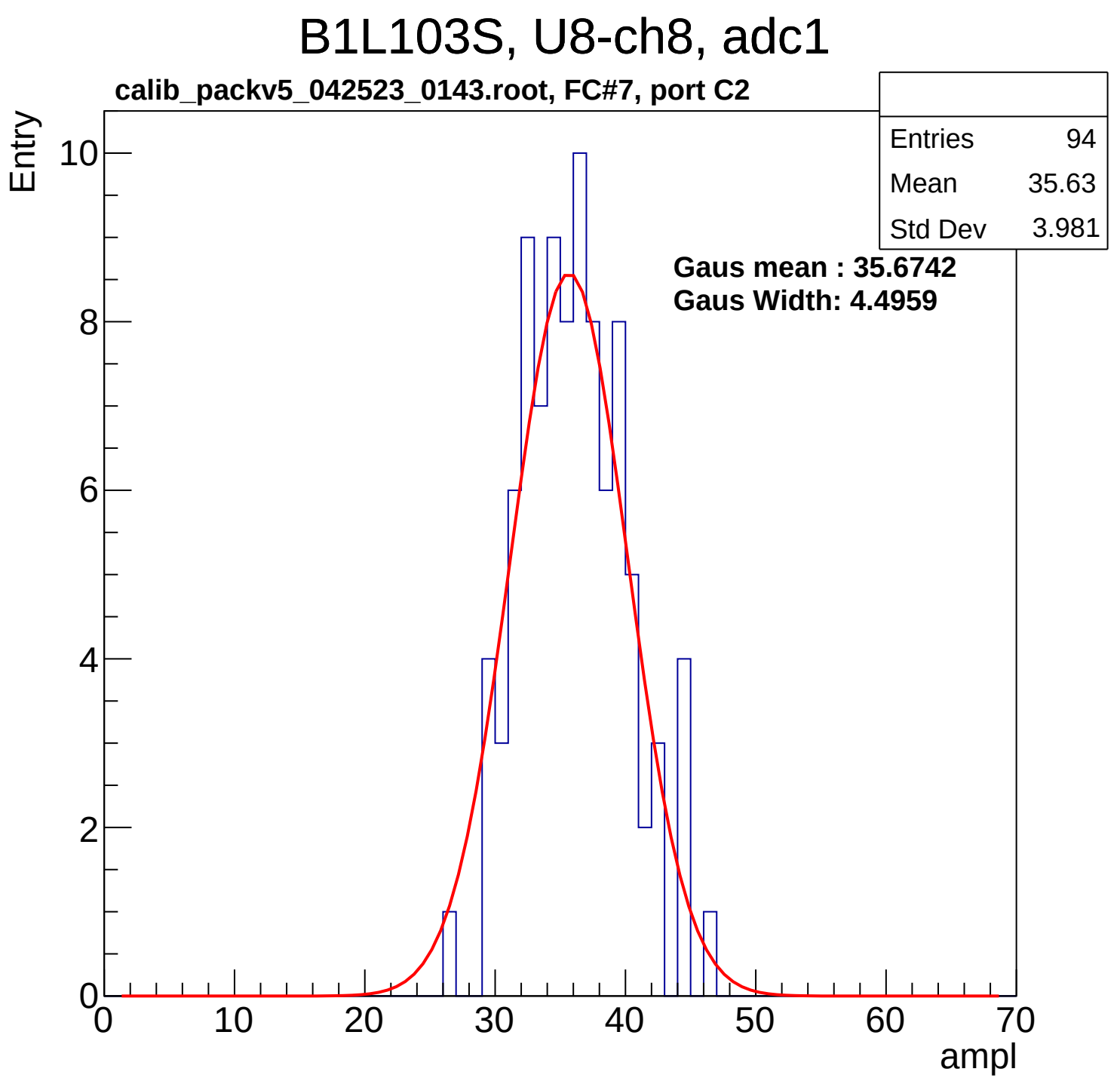

B1L103S, U8-ch7, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 55.52
Std Dev 3.483
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

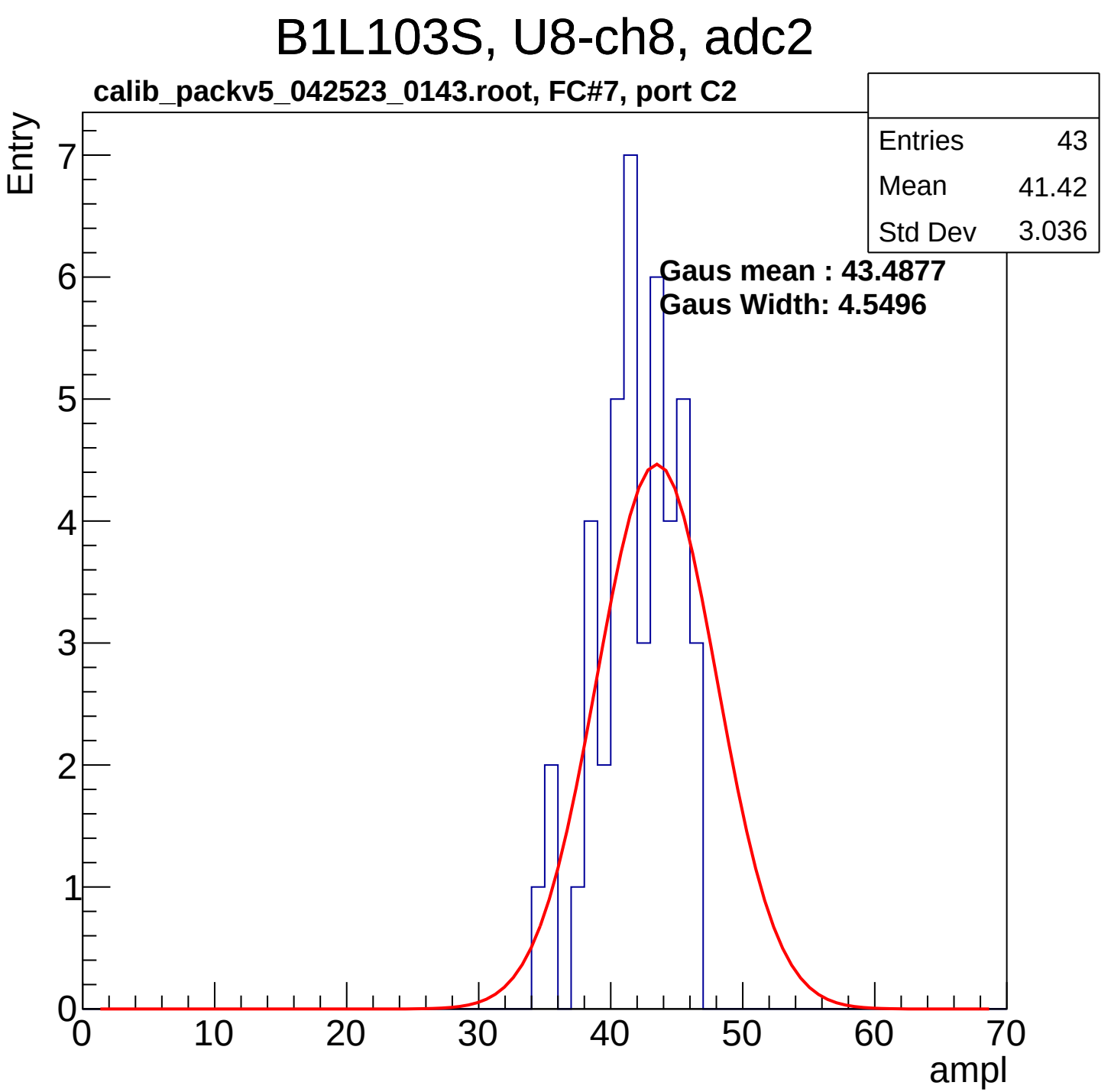

B1L103S, U8-ch7, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 37
Mean 60
Std Dev 2.46
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

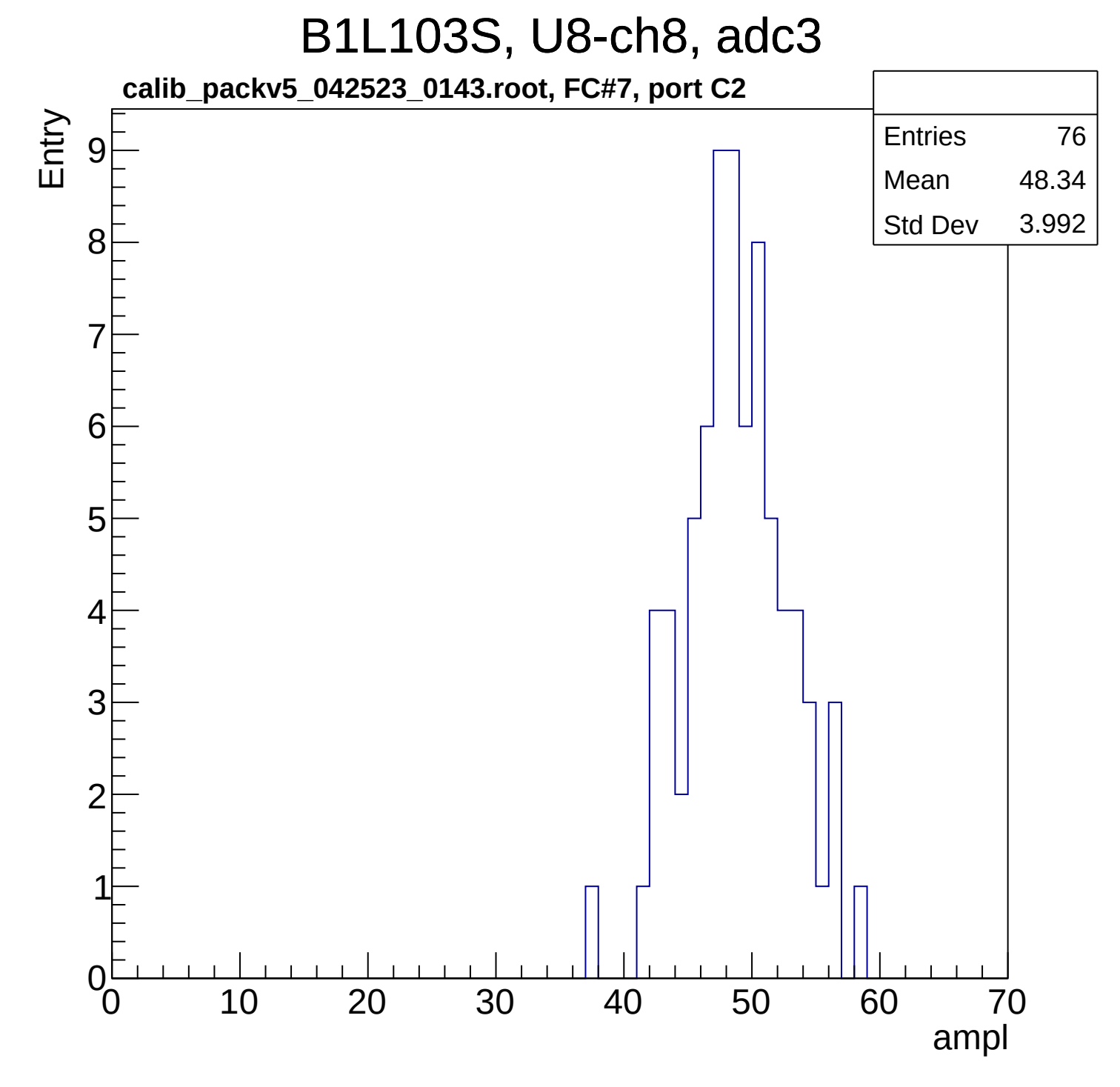

B1L103S, U8-ch7, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 8
Mean 54.62
Std Dev 20.66
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

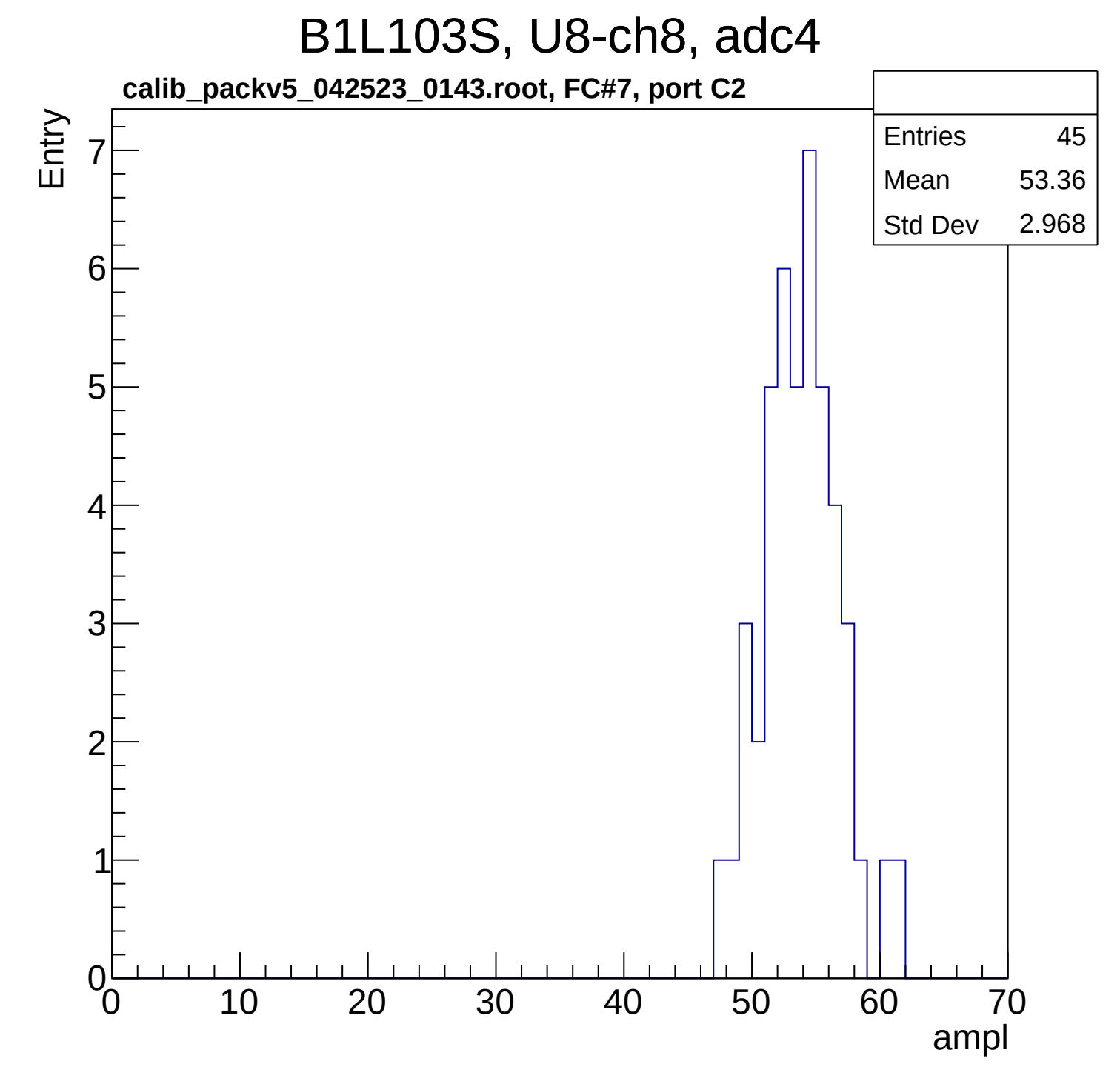

B1L103S, U8-ch7, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 0
Std Dev 0
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl

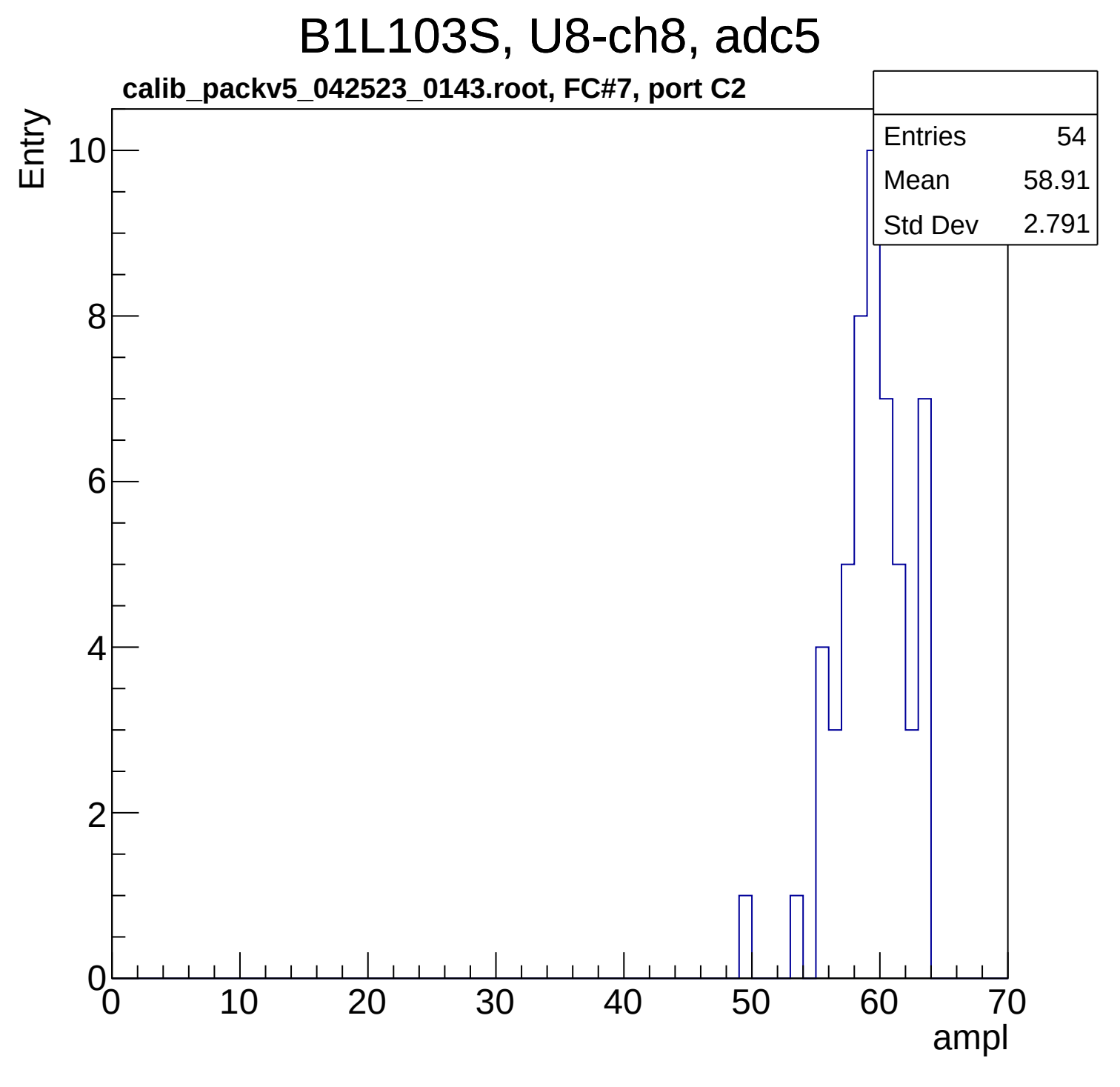

B1L103S, U8-ch8, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 27.1
Std Dev 3.128
Gaus mean : 27.6983
Gaus Width: 2.9938
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

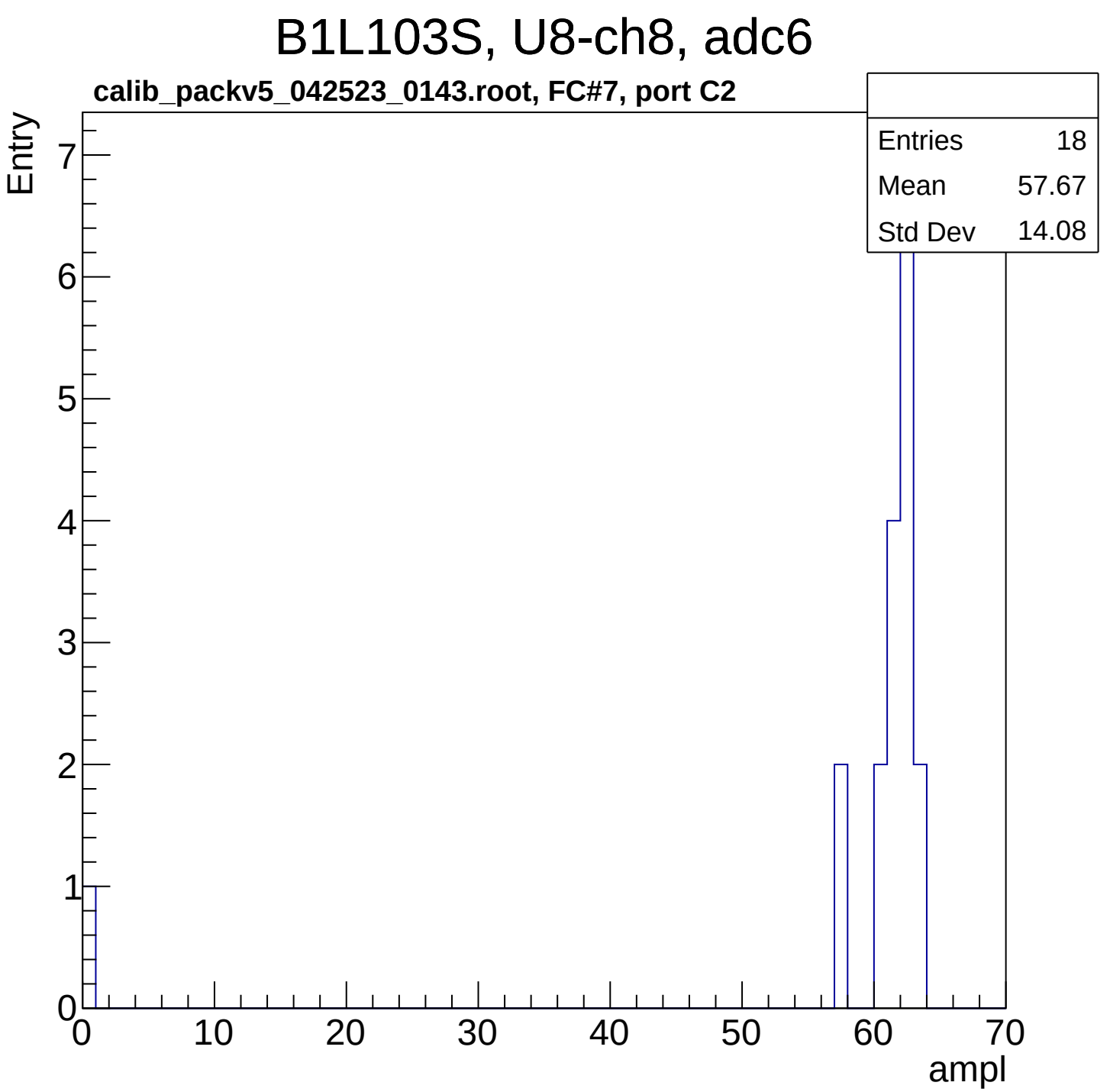

B1L103S, U8-ch8, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 94
Mean 35.63
Std Dev 3.981
Gaus mean : 35.6742
Gaus Width: 4.4959
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

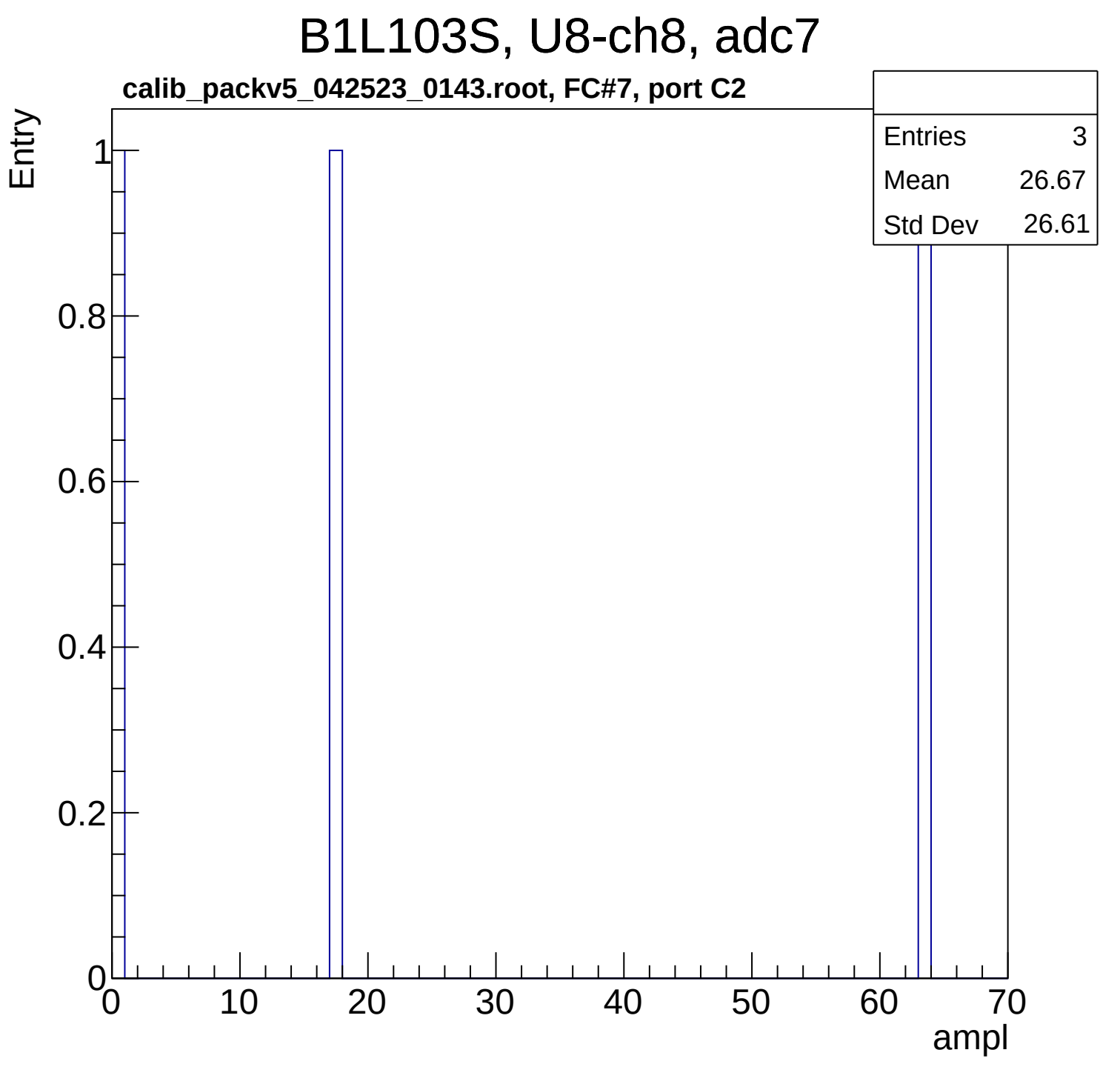

B1L103S, U8-ch8, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 43
Mean 41.42
Std Dev 3.036
Gaus mean : 43.4877
Gaus Width: 4.5496
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

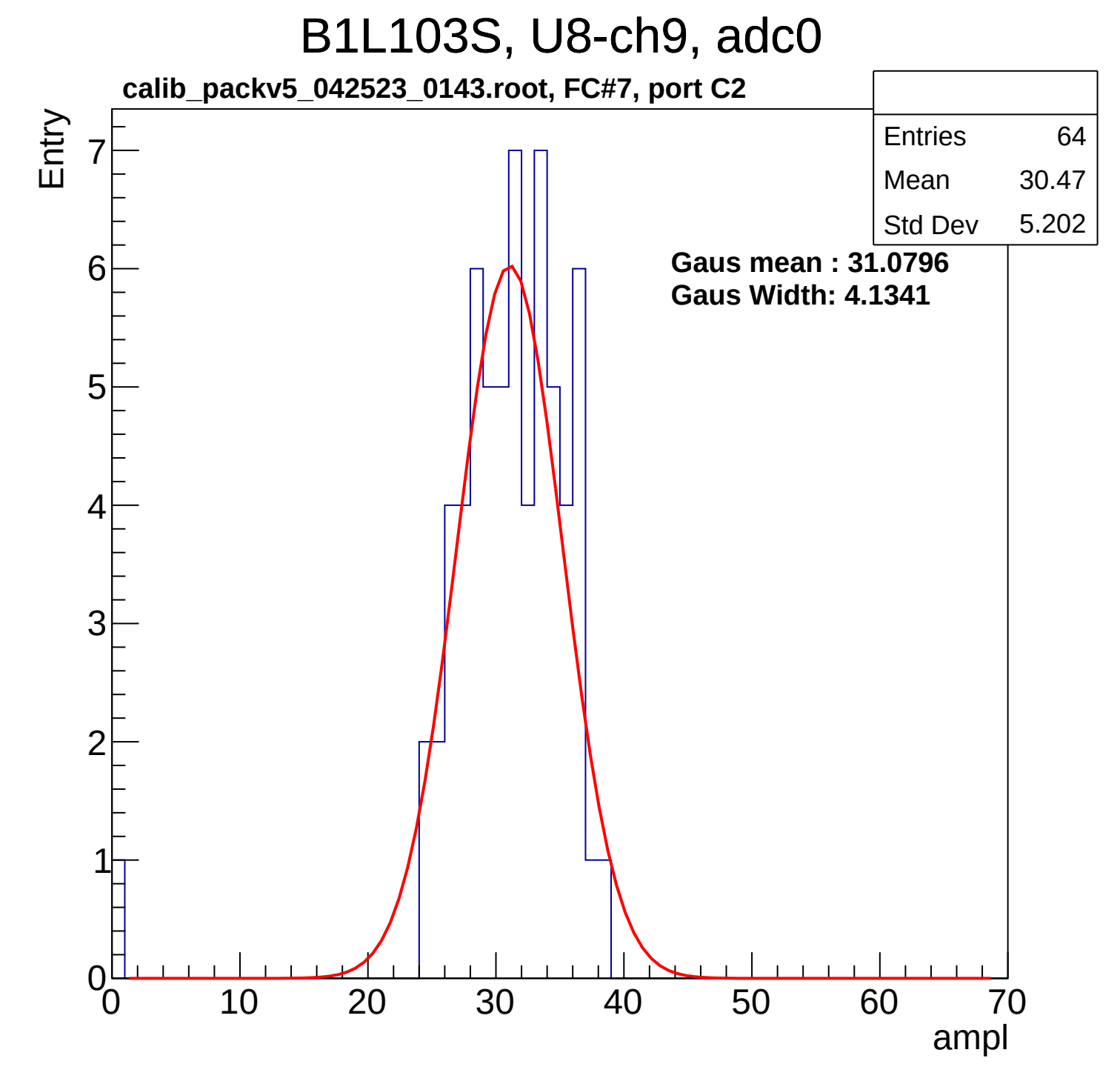

B1L103S, U8-ch8, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 76
Mean 48.34
Std Dev 3.992
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

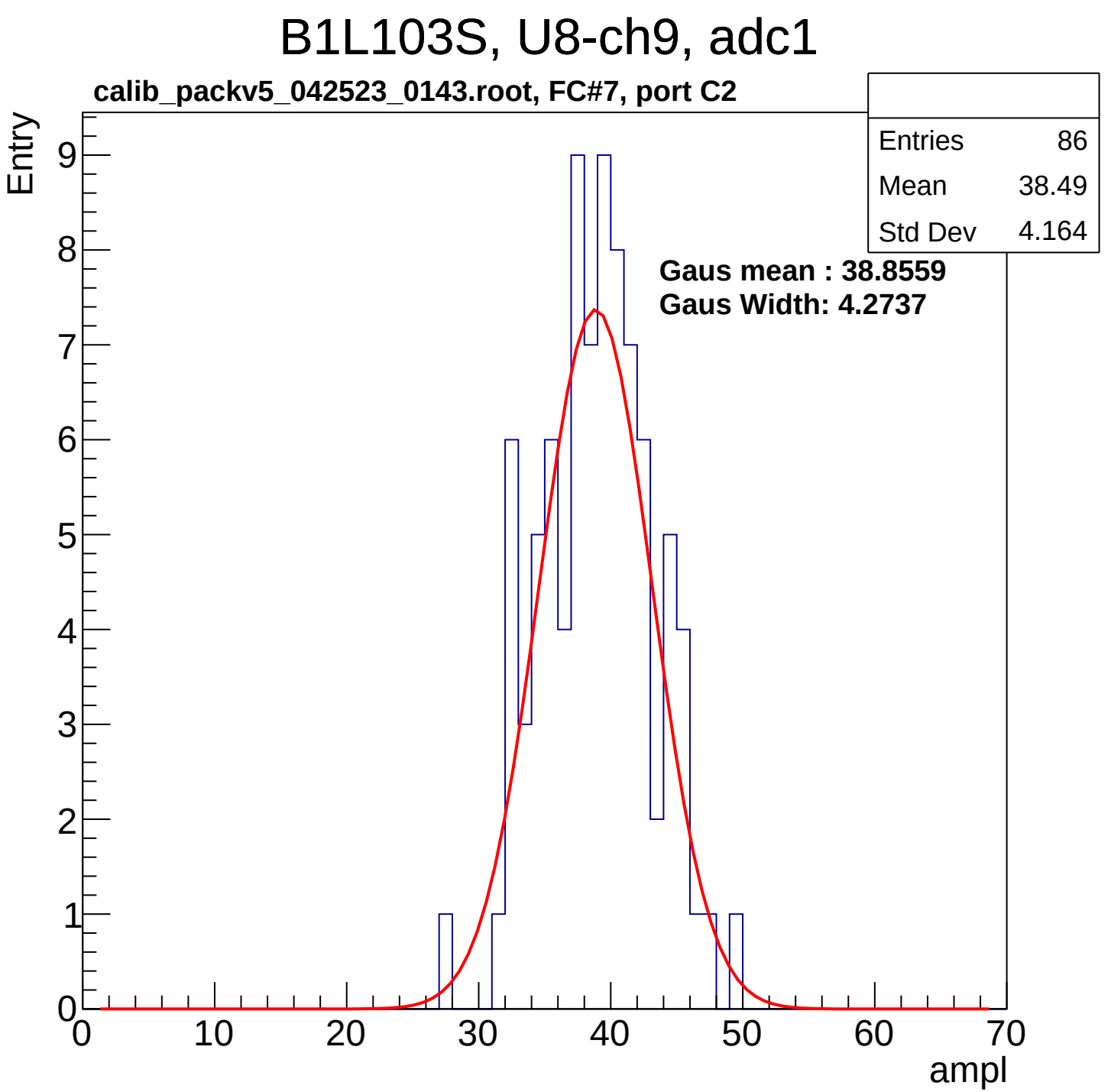

B1L103S, U8-ch8, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 45
Mean 53.36
Std Dev 2.968
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

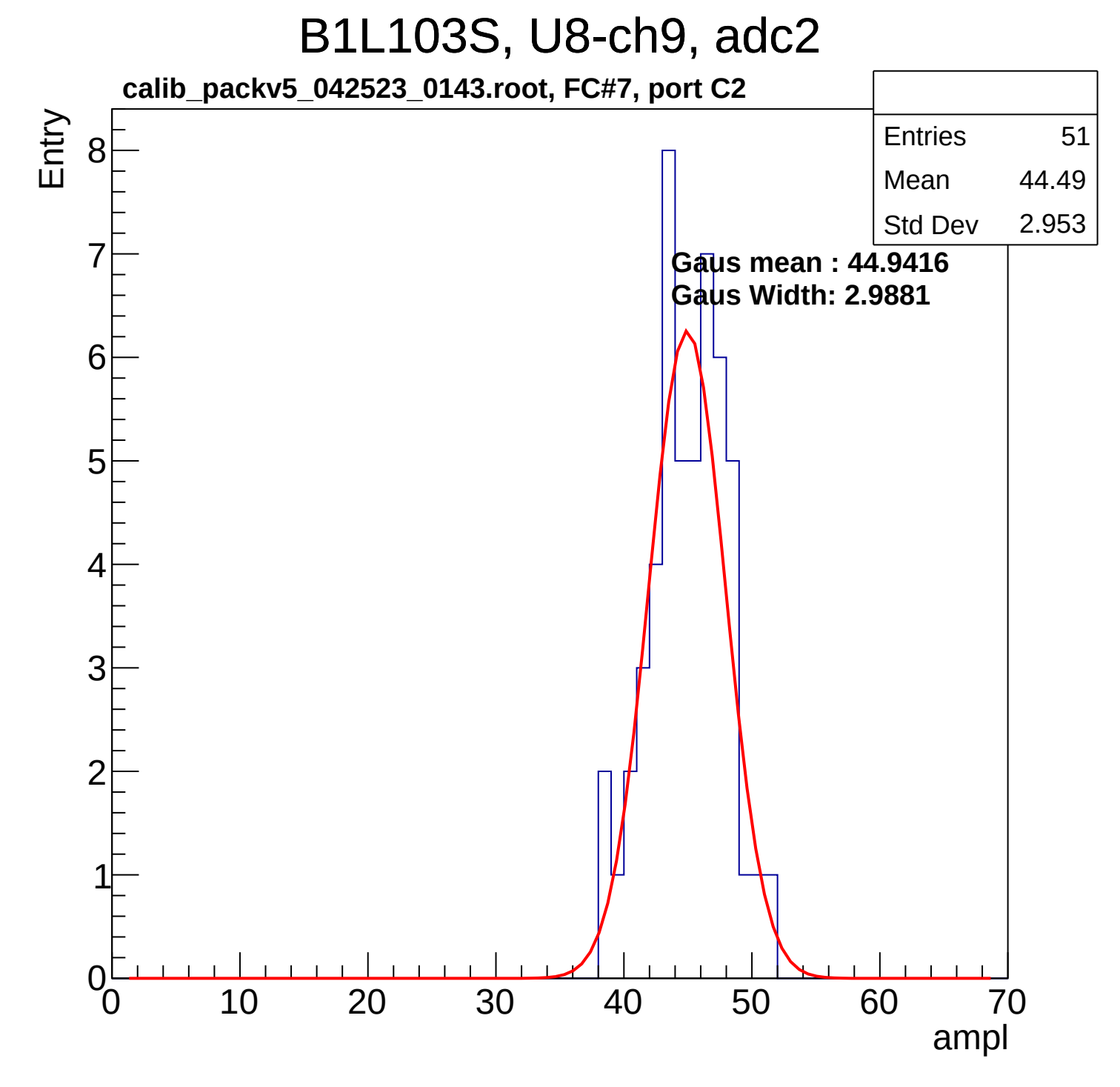

B1L103S, U8-ch8, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 58.91
Std Dev 2.791
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

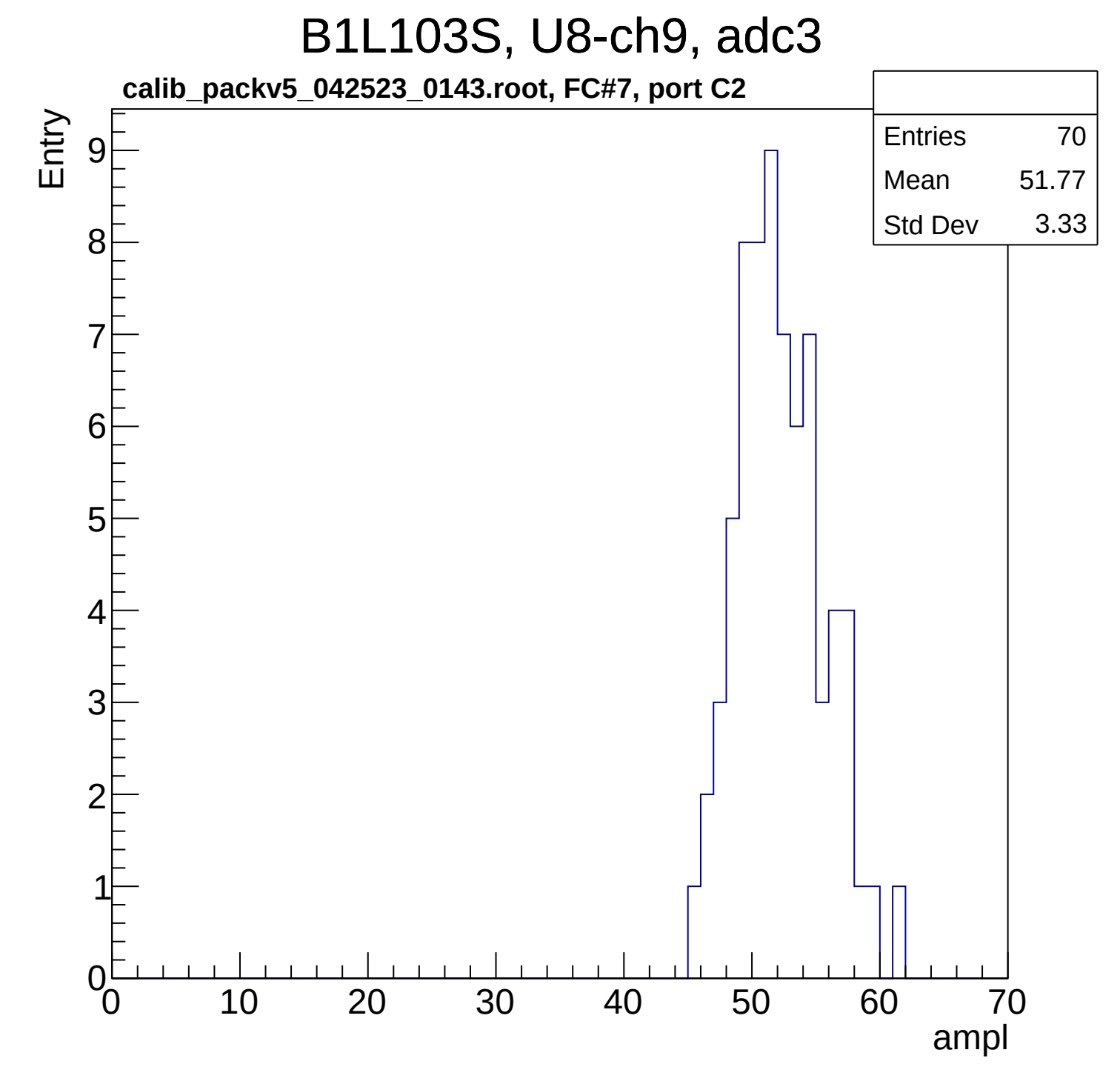

B1L103S, U8-ch8, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 18
Mean 57.67
Std Dev 14.08
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

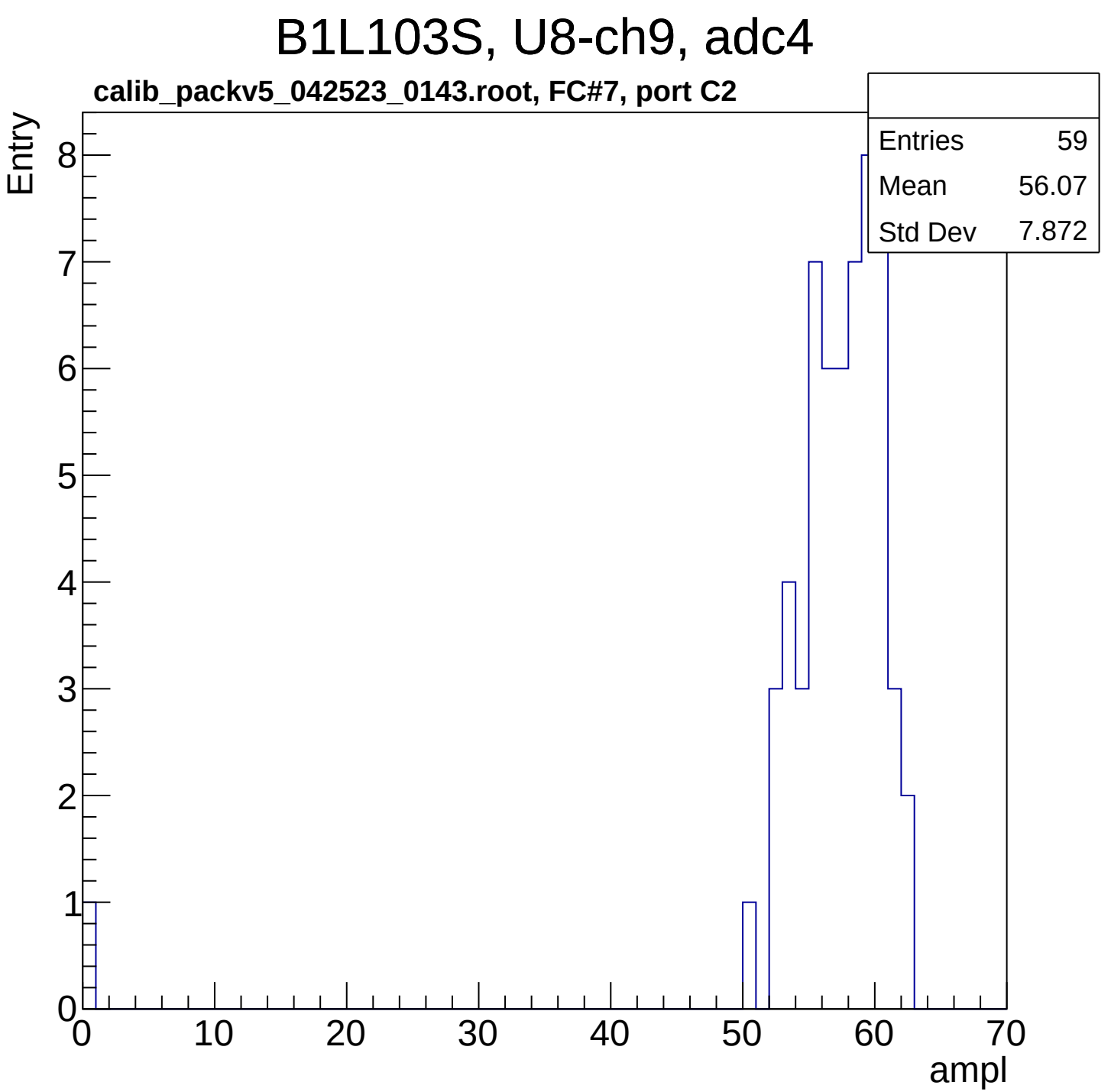

B1L103S, U8-ch8, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 26.67
Std Dev 26.61
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

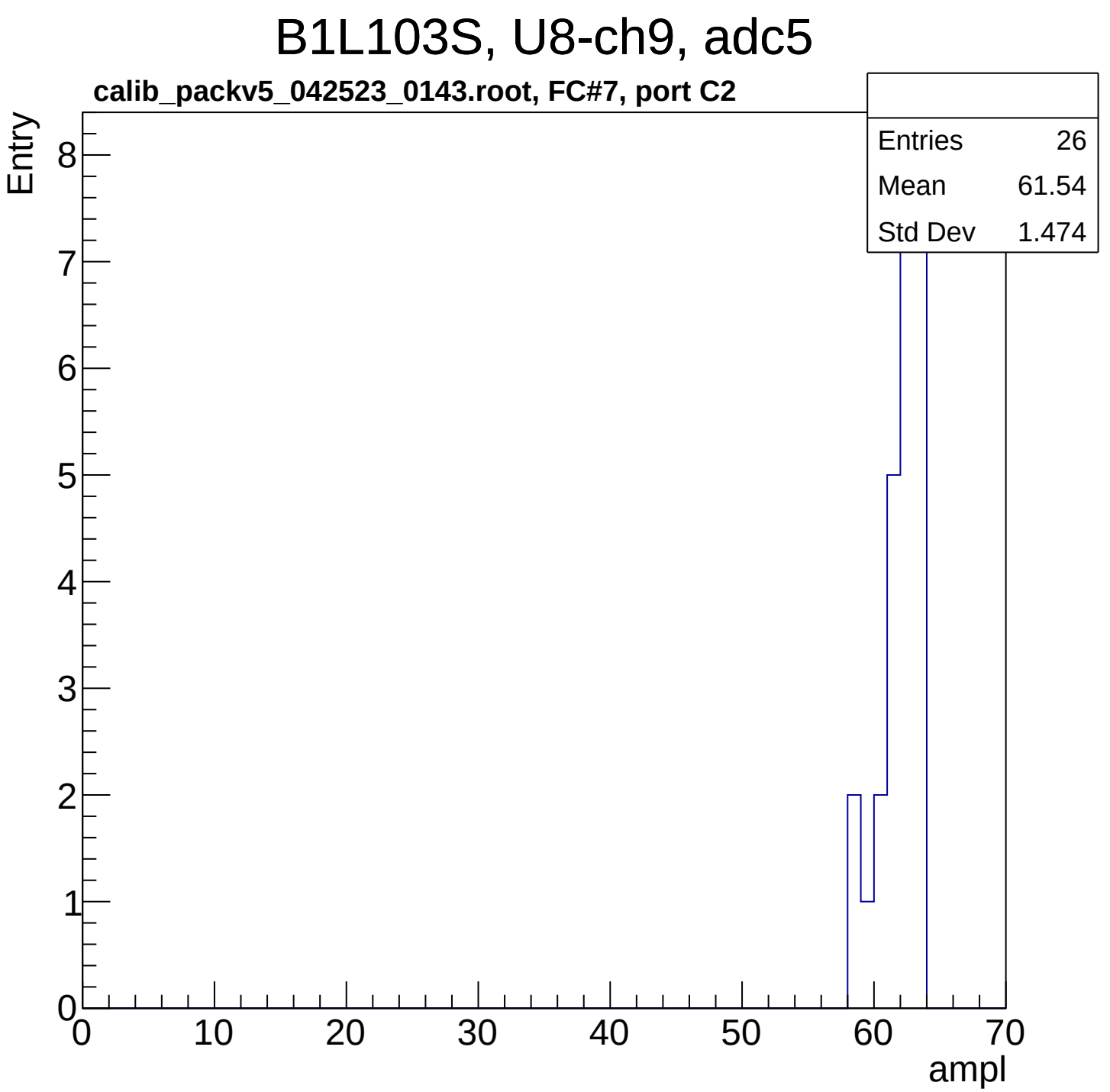

B1L103S, U8-ch9, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 30.47
Std Dev 5.202
Gaus mean : 31.0796
Gaus Width: 4.1341
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

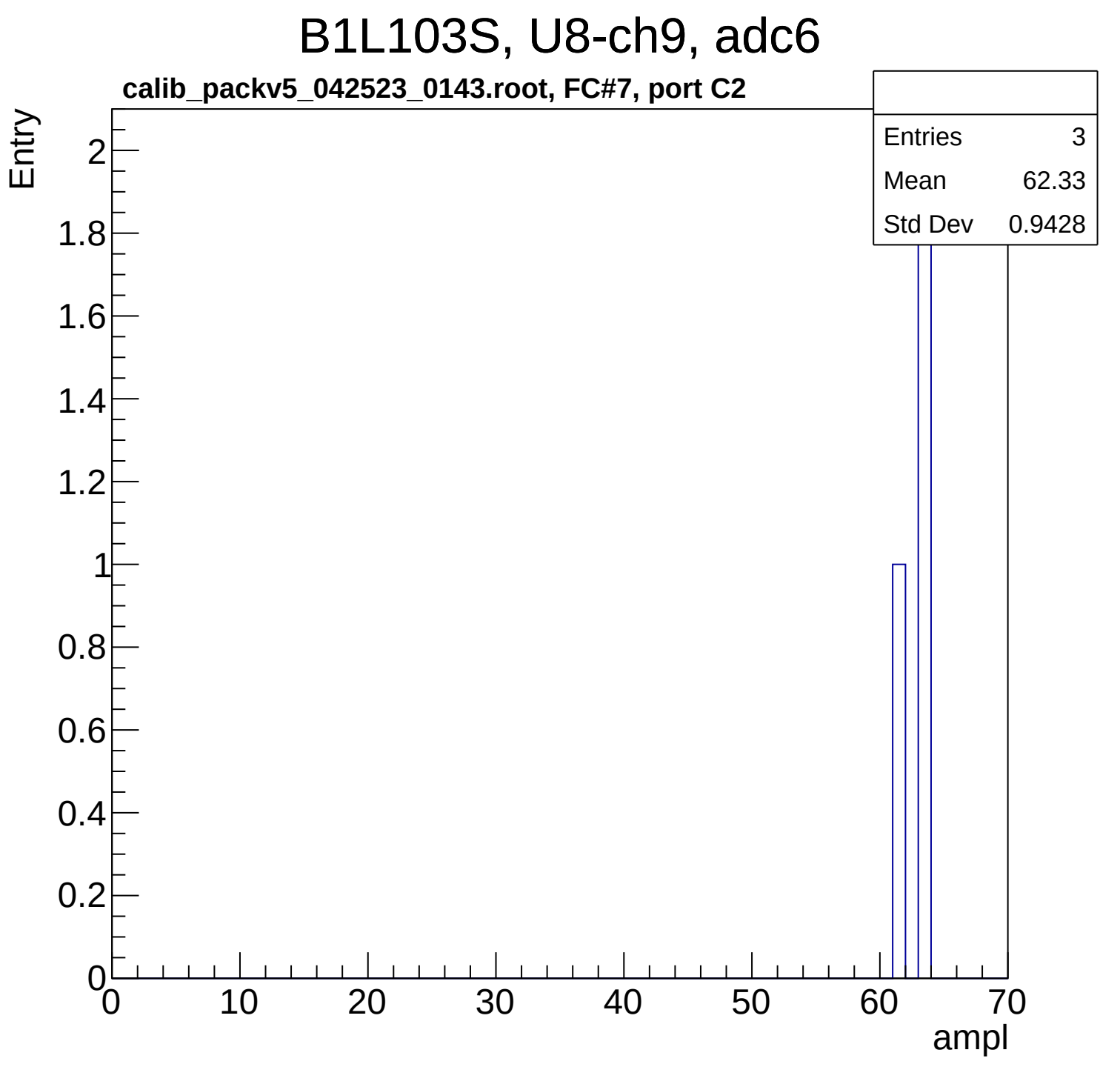

B1L103S, U8-ch9, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 86
Mean 38.49
Std Dev 4.164
Gaus mean : 38.8559
Gaus Width: 4.2737
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

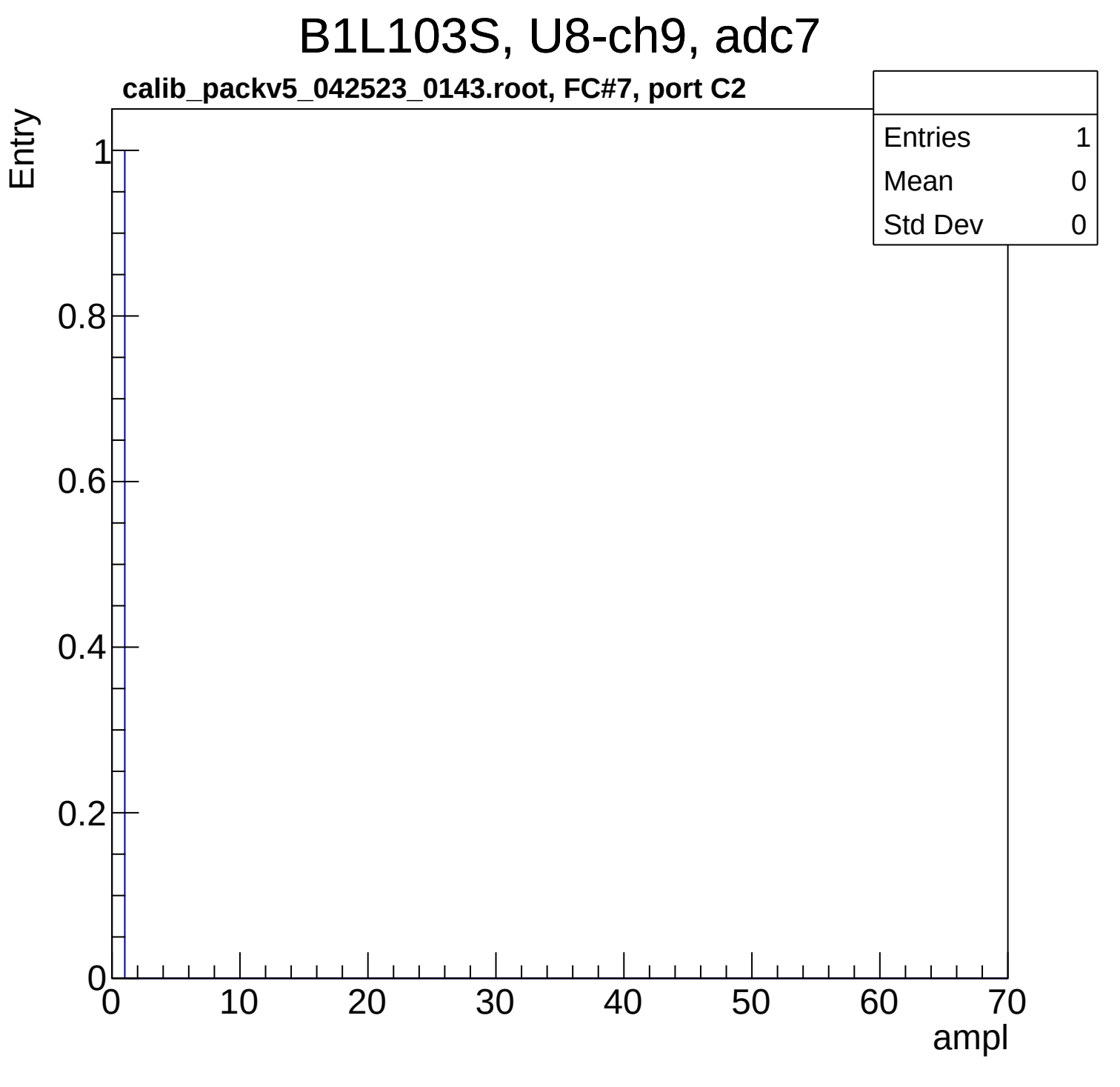

B1L103S, U8-ch9, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 44.49
Std Dev 2.953
Gaus mean : 44.9416
Gaus Width: 2.9881
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

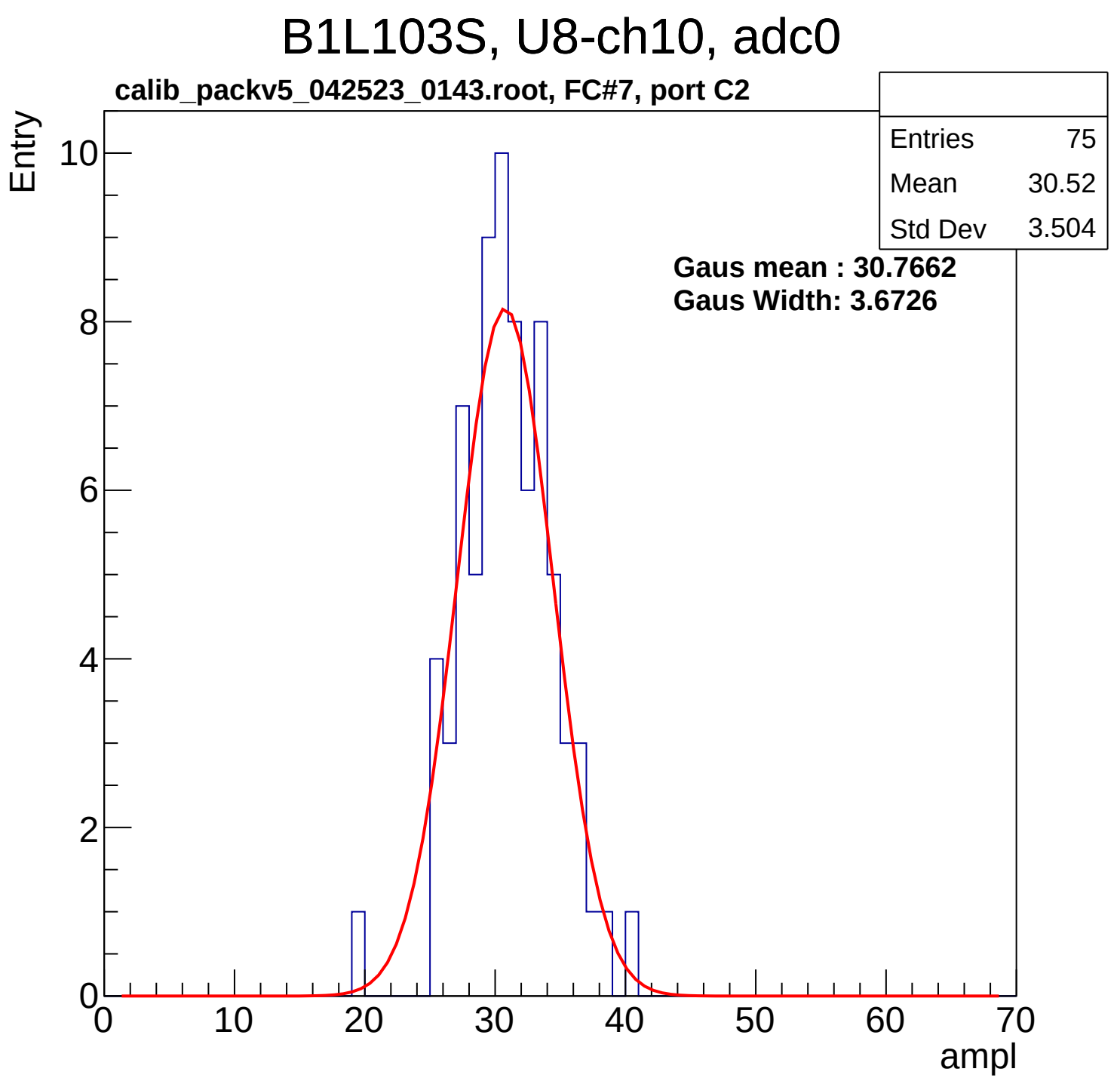

B1L103S, U8-ch9, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 51.77
Std Dev 3.33
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

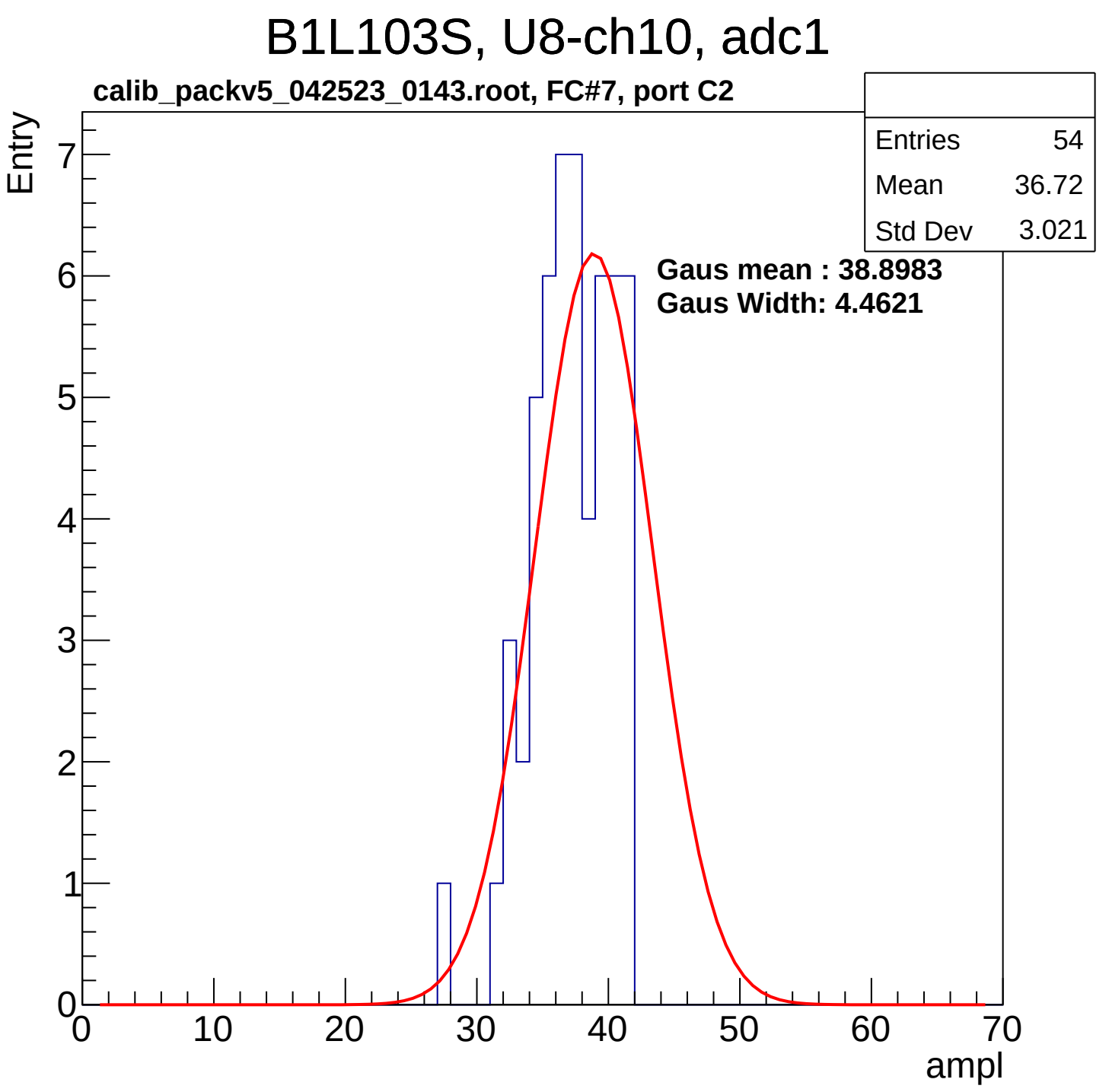

B1L103S, U8-ch9, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 56.07
Std Dev 7.872
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

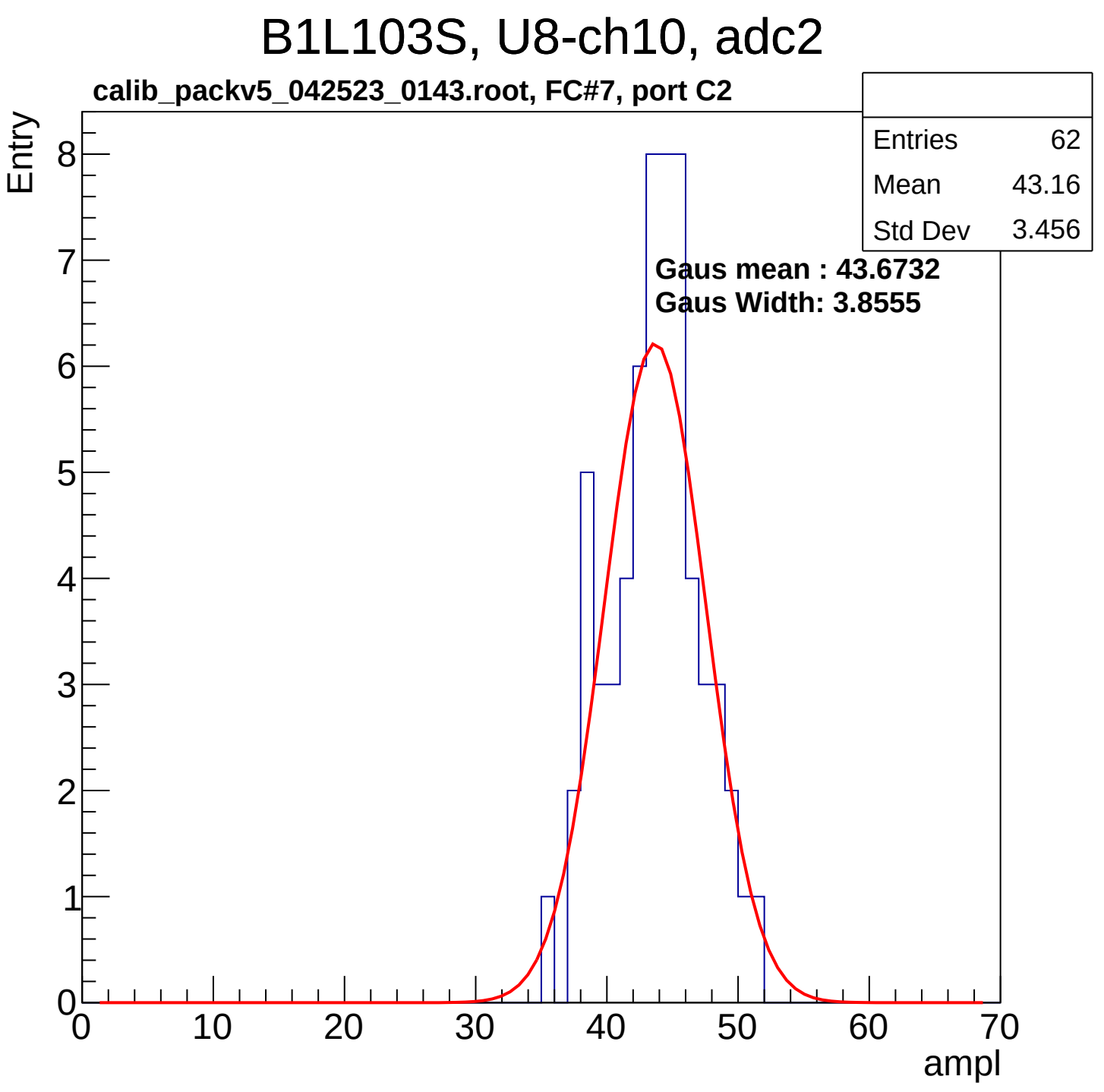

B1L103S, U8-ch9, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 26
Mean 61.54
Std Dev 1.474
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

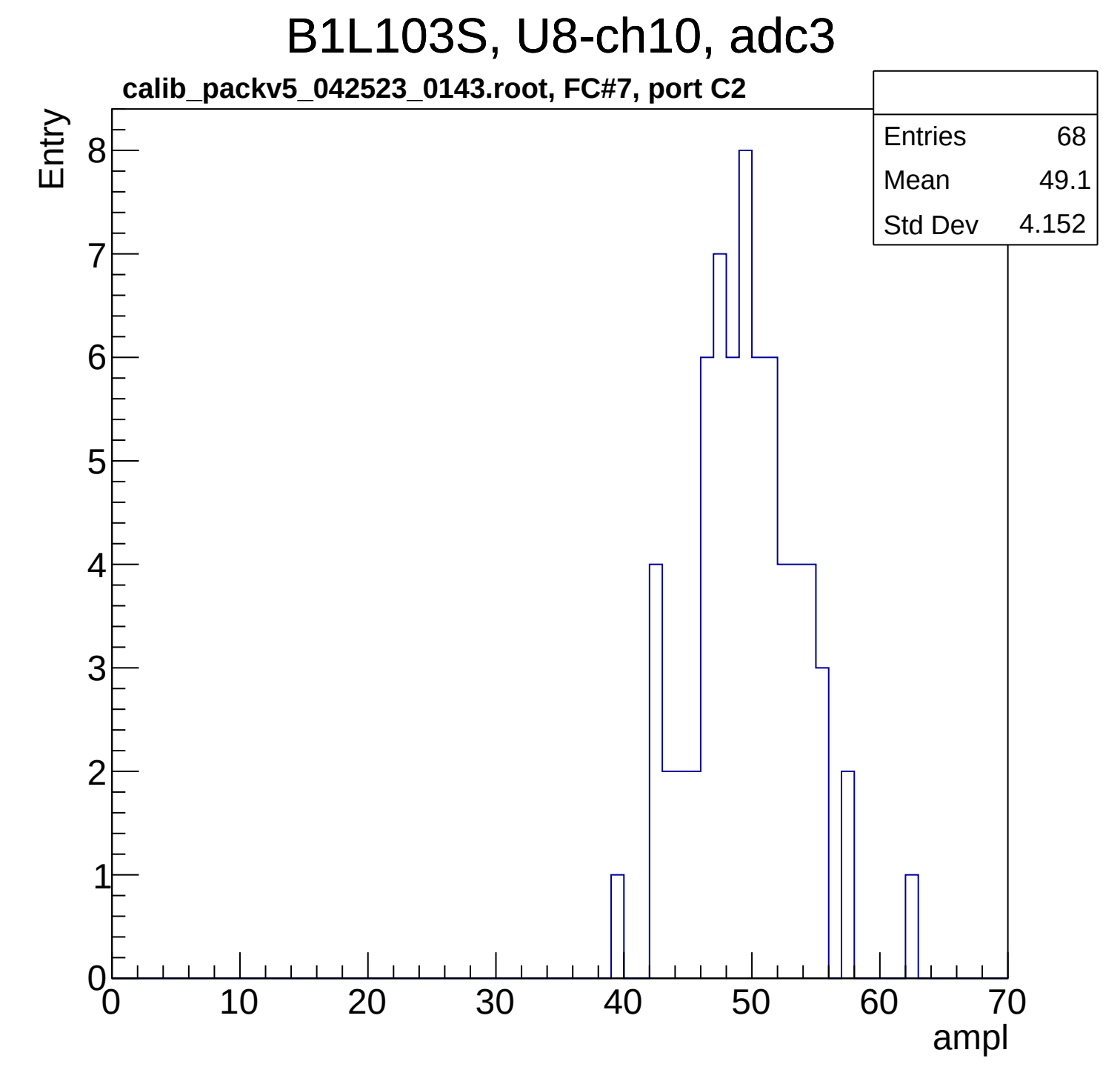

B1L103S, U8-ch9, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 62.33
Std Dev 0.9428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

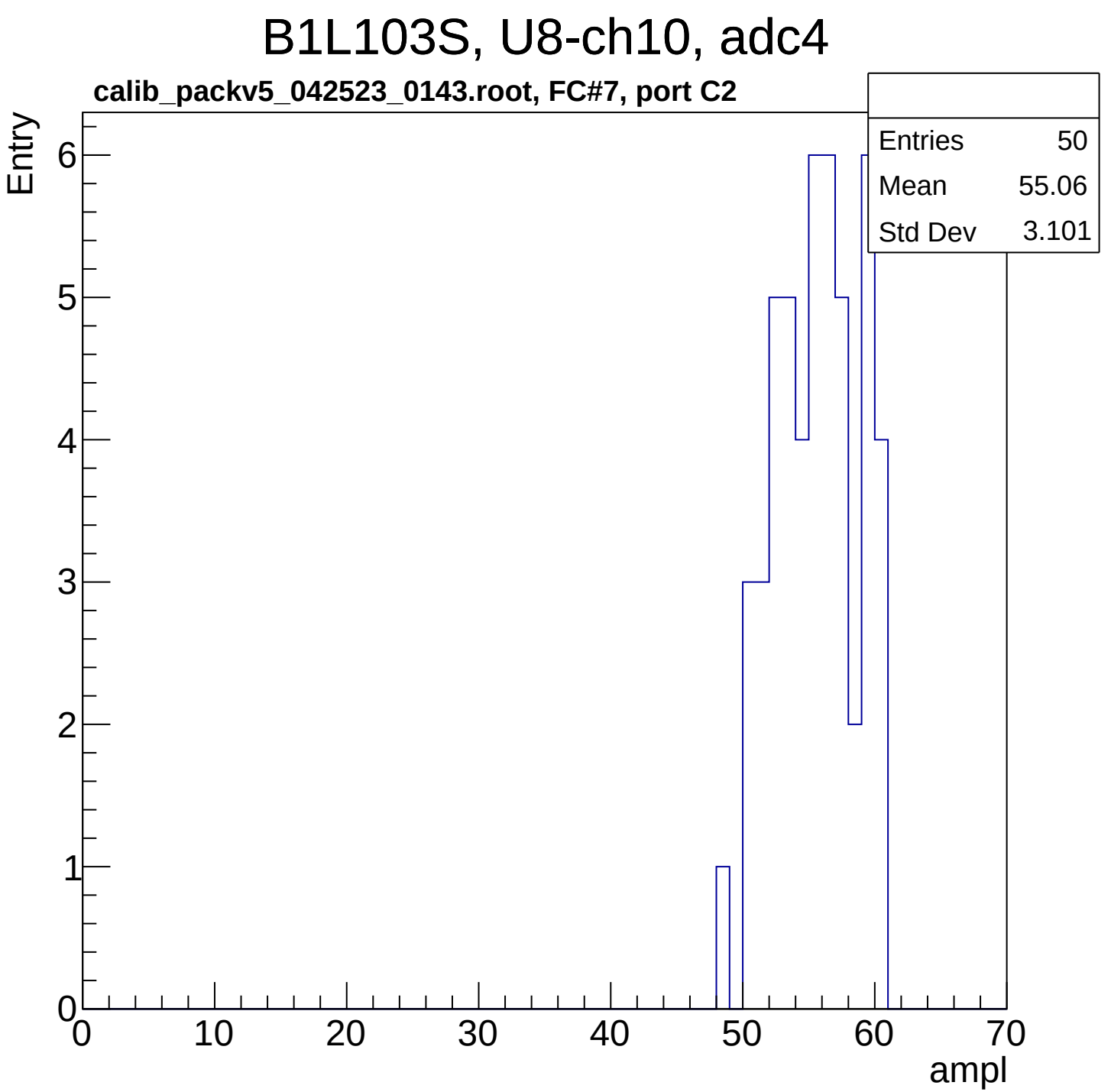

B1L103S, U8-ch9, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

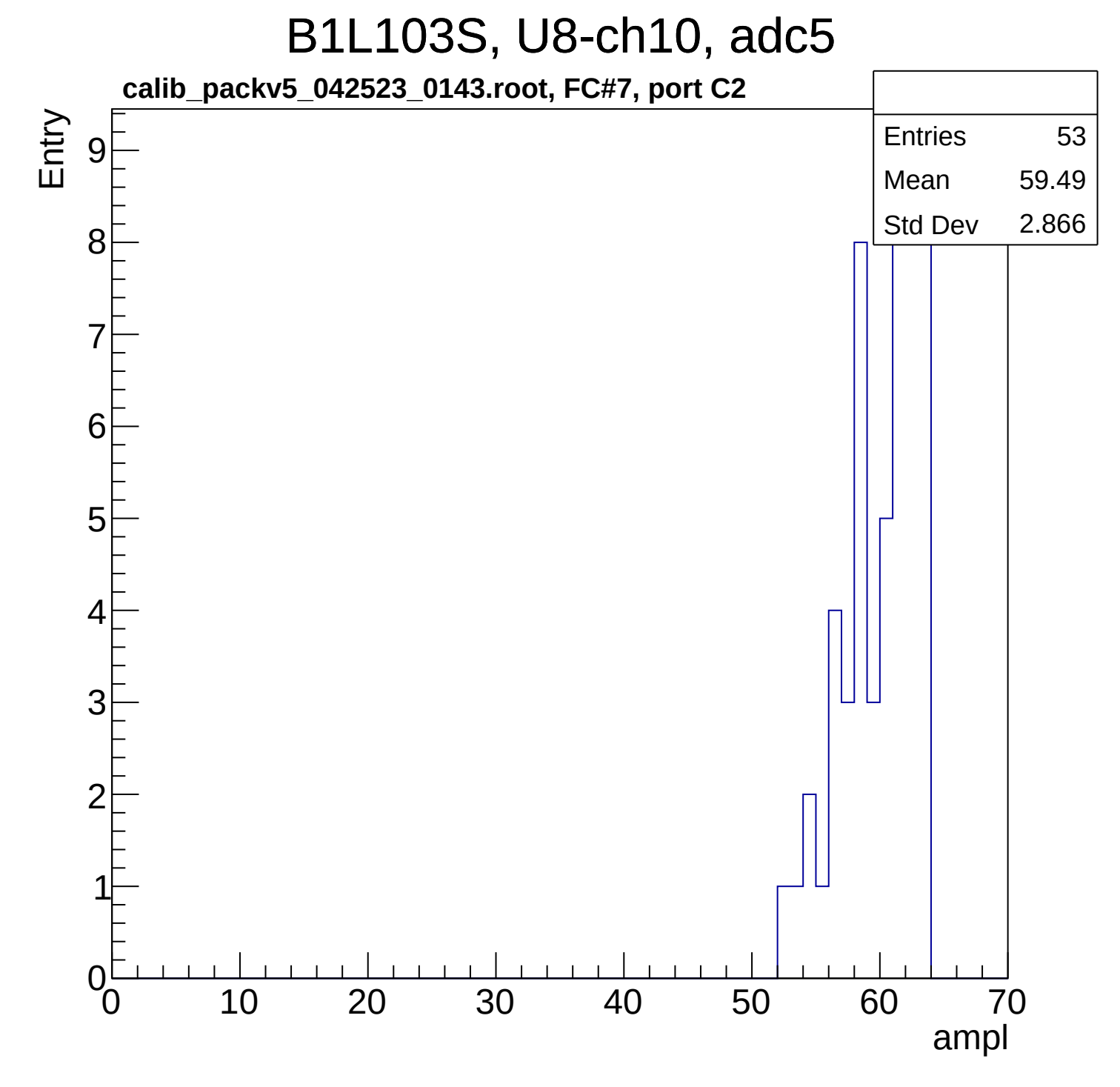

B1L103S, U8-ch10, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 30.52
Std Dev 3.504
Gaus mean : 30.7662
Gaus Width: 3.6726
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

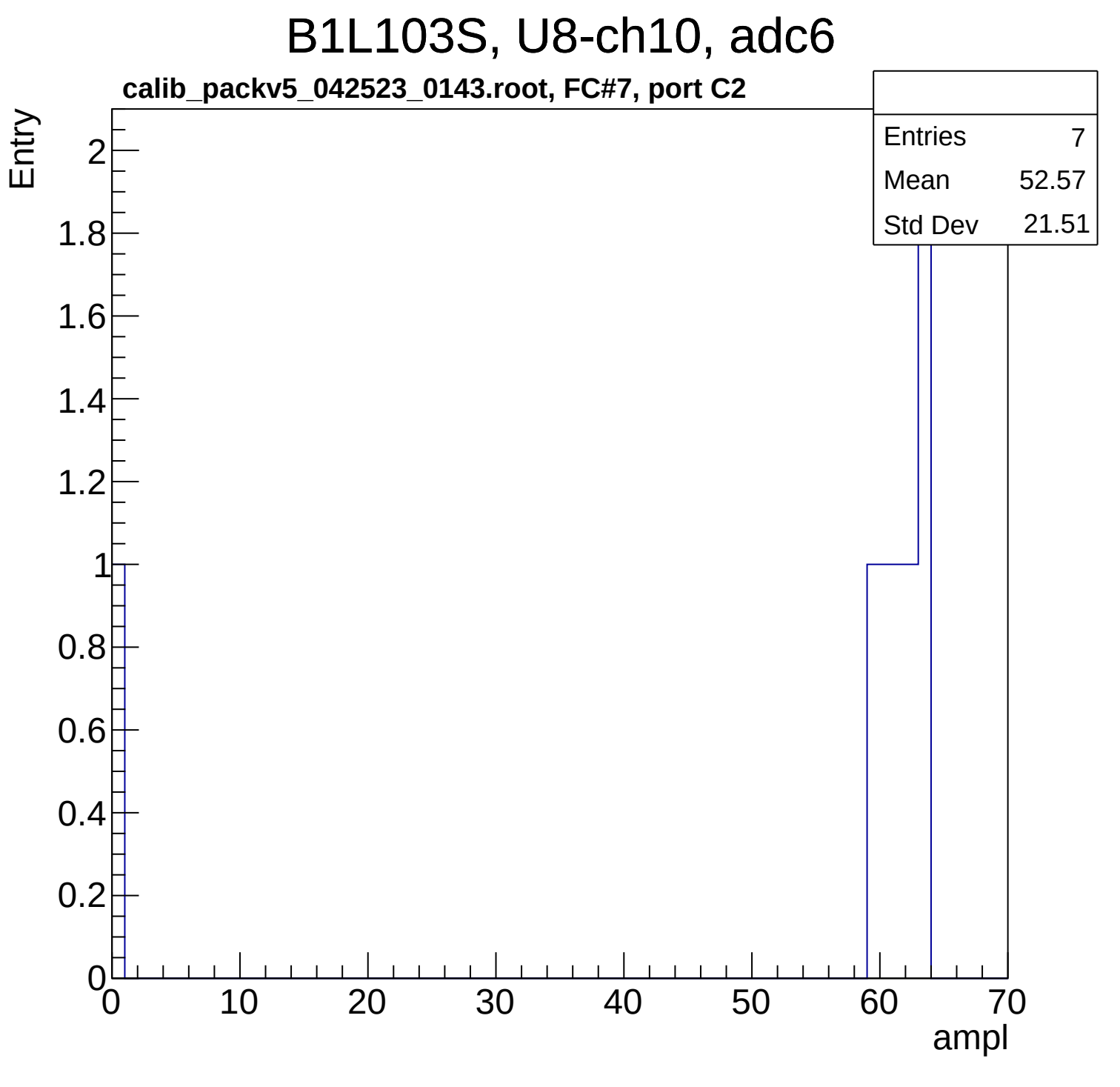

B1L103S, U8-ch10, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 36.72
Std Dev 3.021
Gaus mean : 38.8983
Gaus Width: 4.4621
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

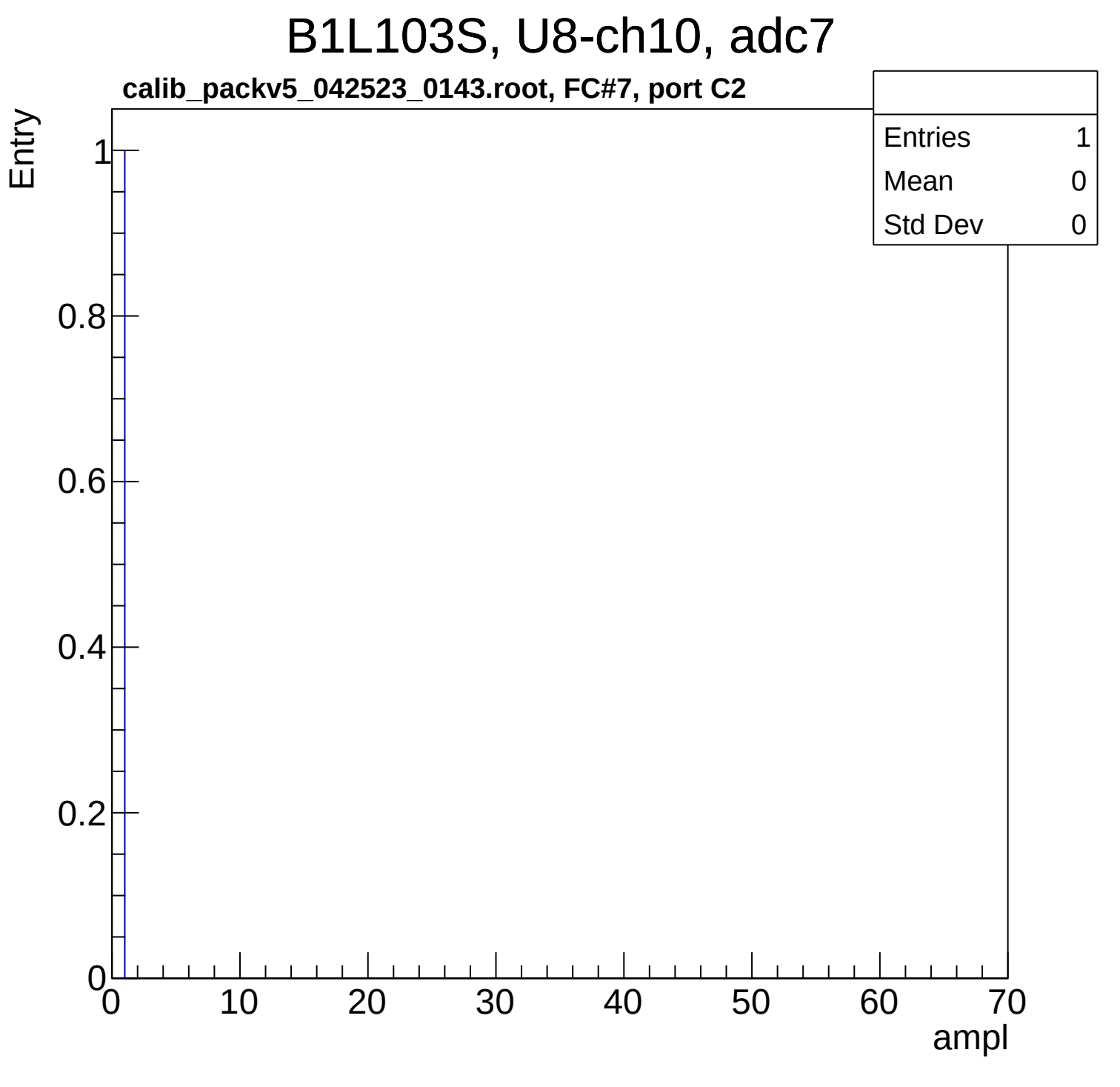

B1L103S, U8-ch10, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 43.16
Std Dev 3.456
Gaus mean : 43.6732
Gaus Width: 3.8555
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

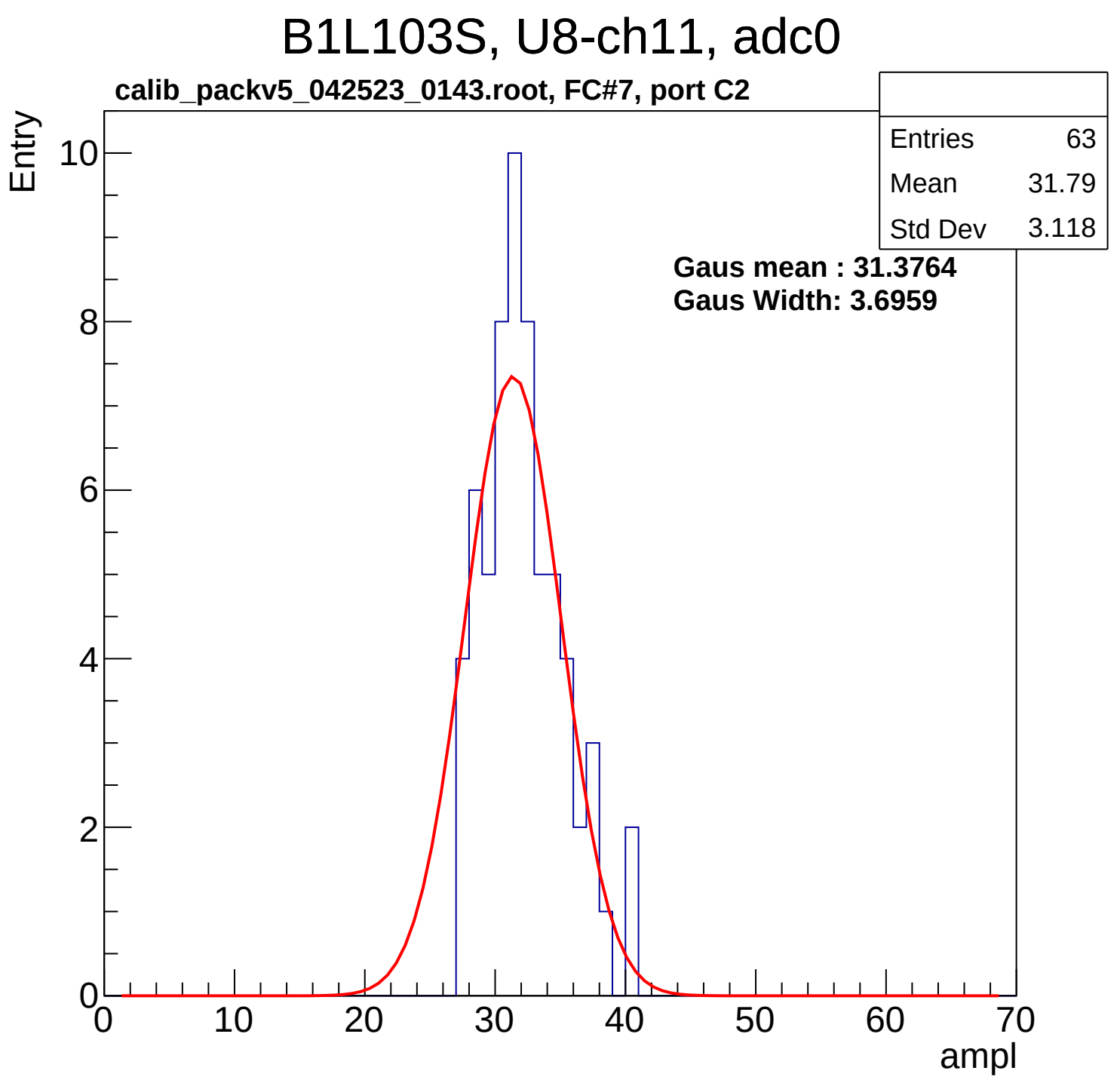

B1L103S, U8-ch10, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 49.1
Std Dev 4.152
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

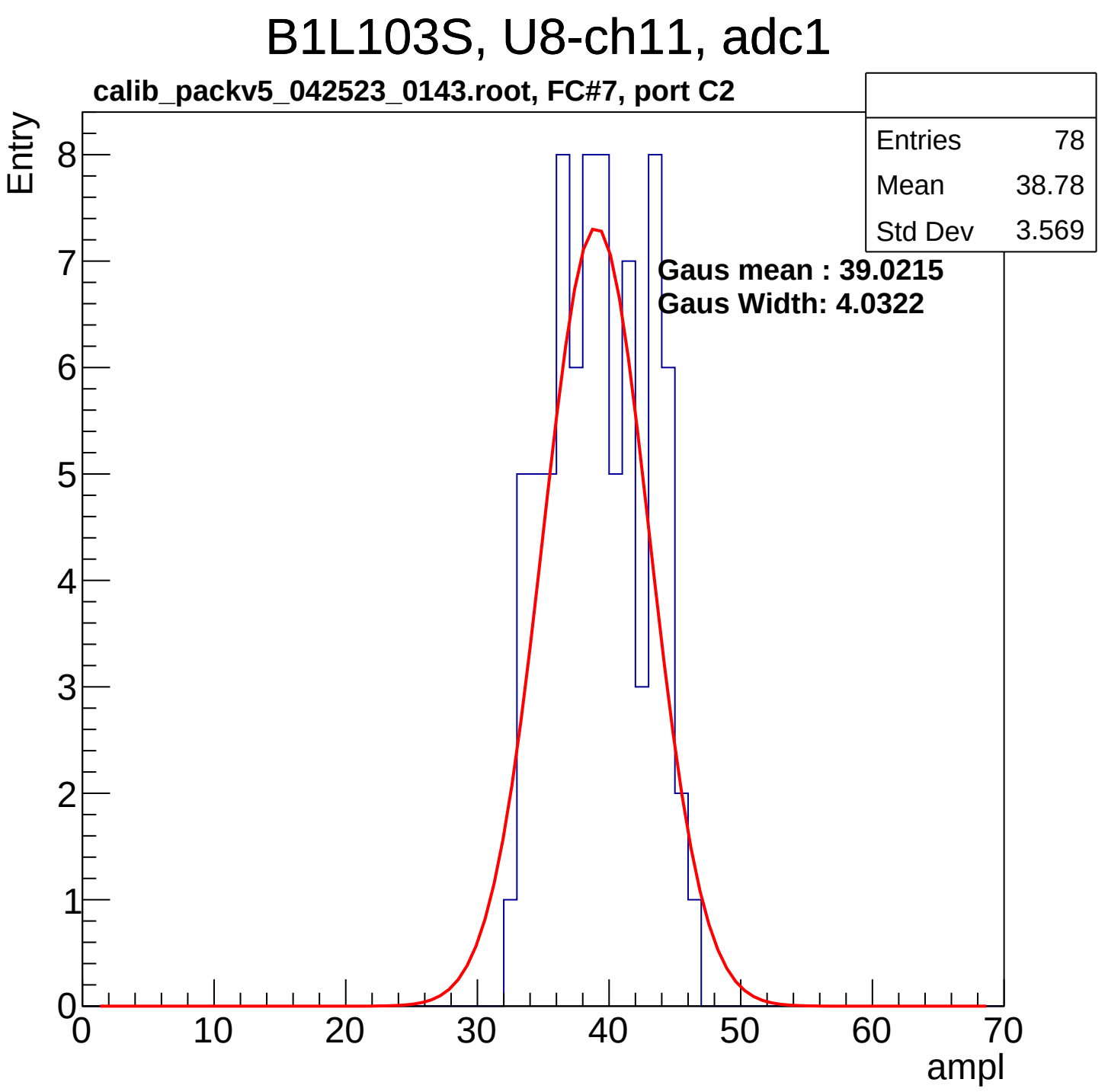

B1L103S, U8-ch10, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 55.06
Std Dev 3.101
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

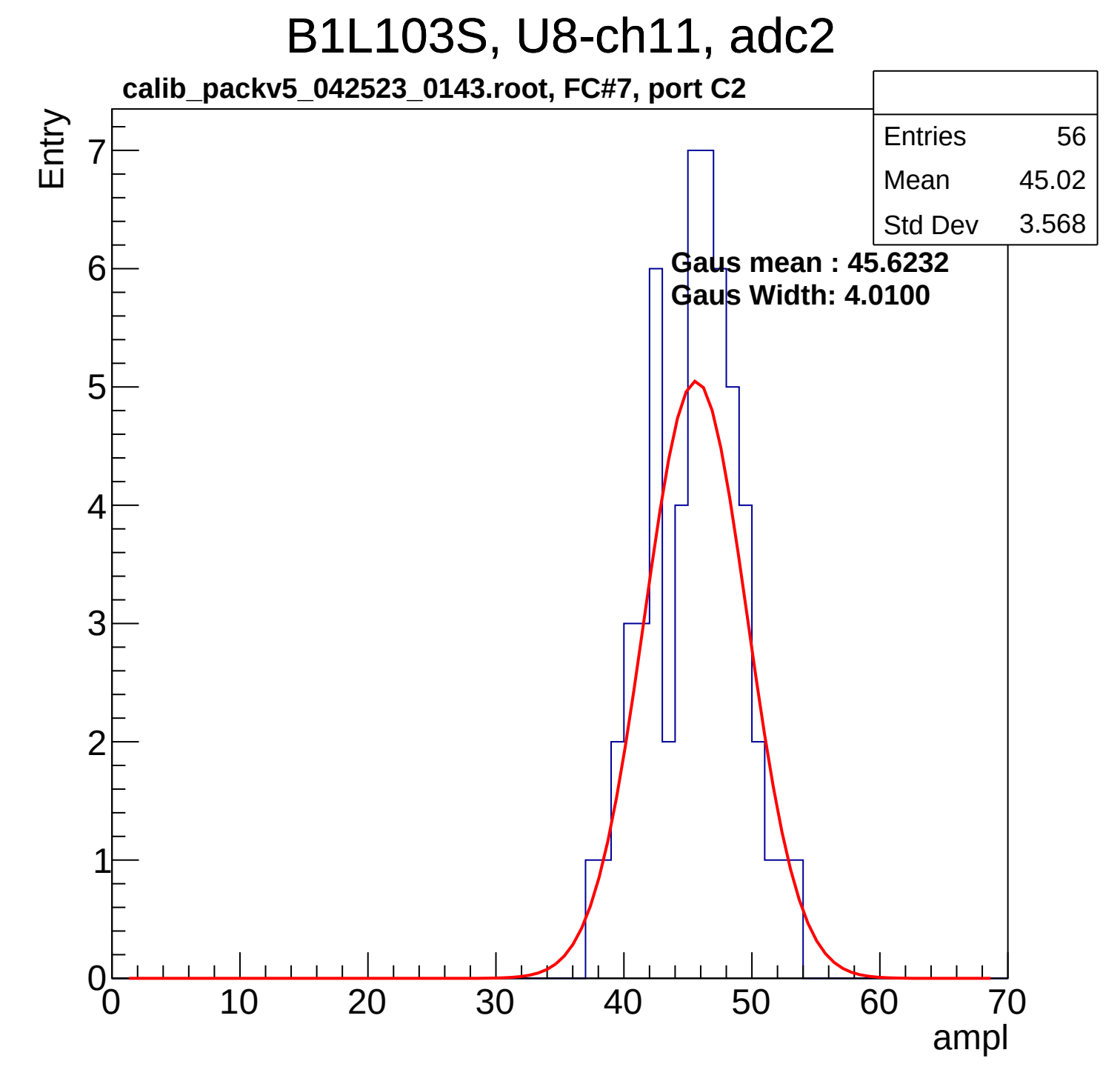

B1L103S, U8-ch10, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 59.49
Std Dev 2.866
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

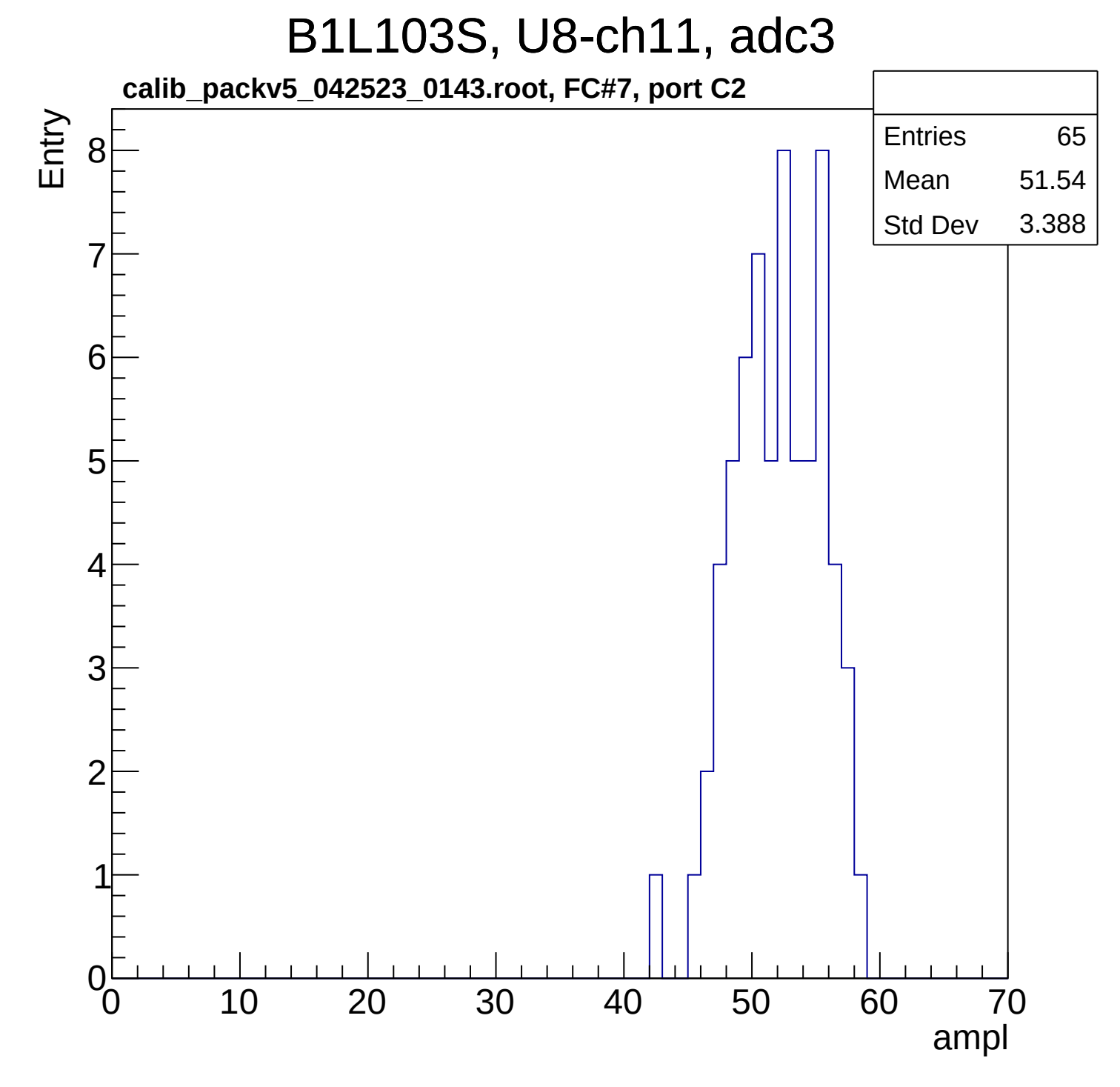

B1L103S, U8-ch10, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 7
Mean 52.57
Std Dev 21.51
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

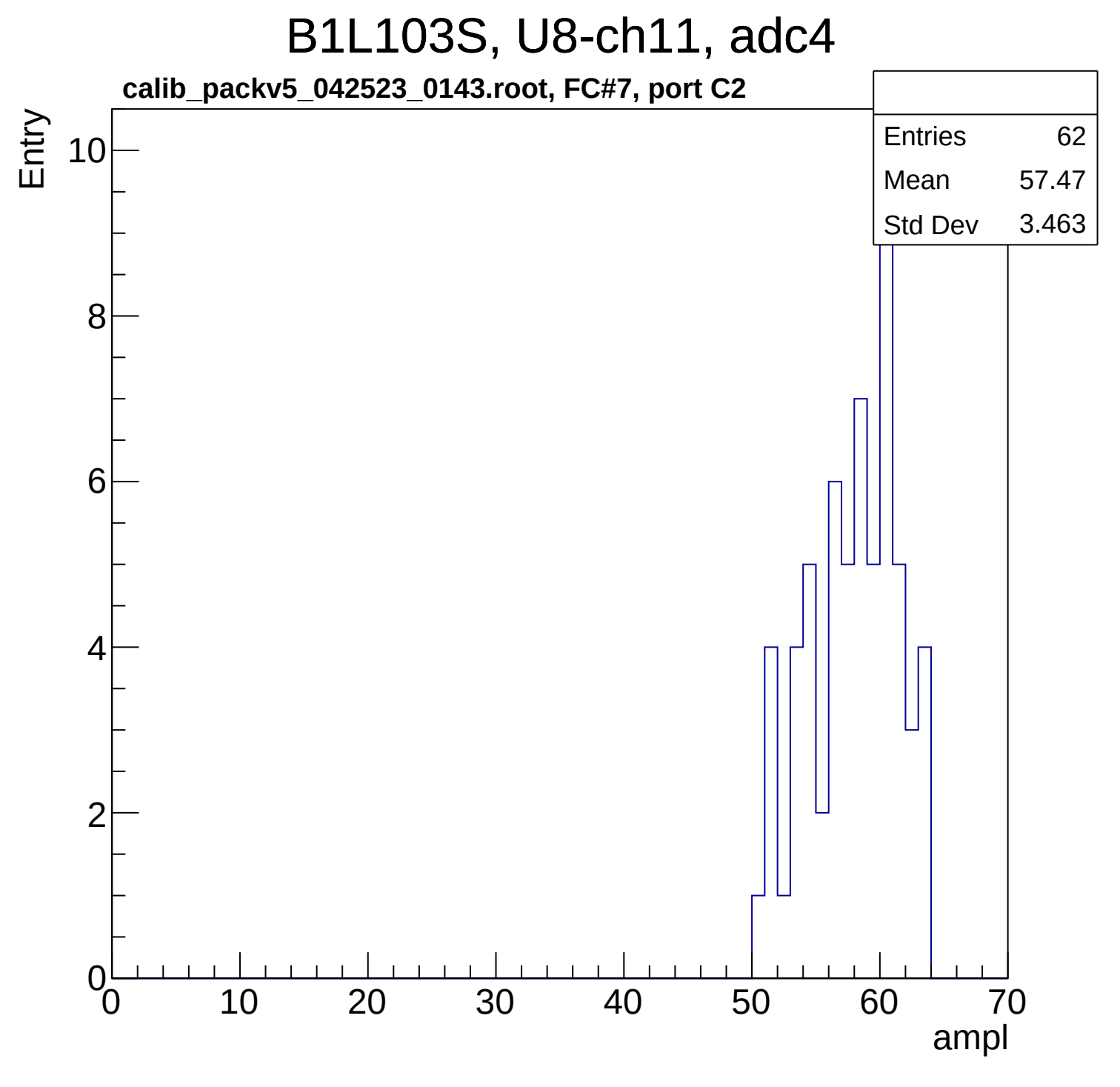

B1L103S, U8-ch10, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

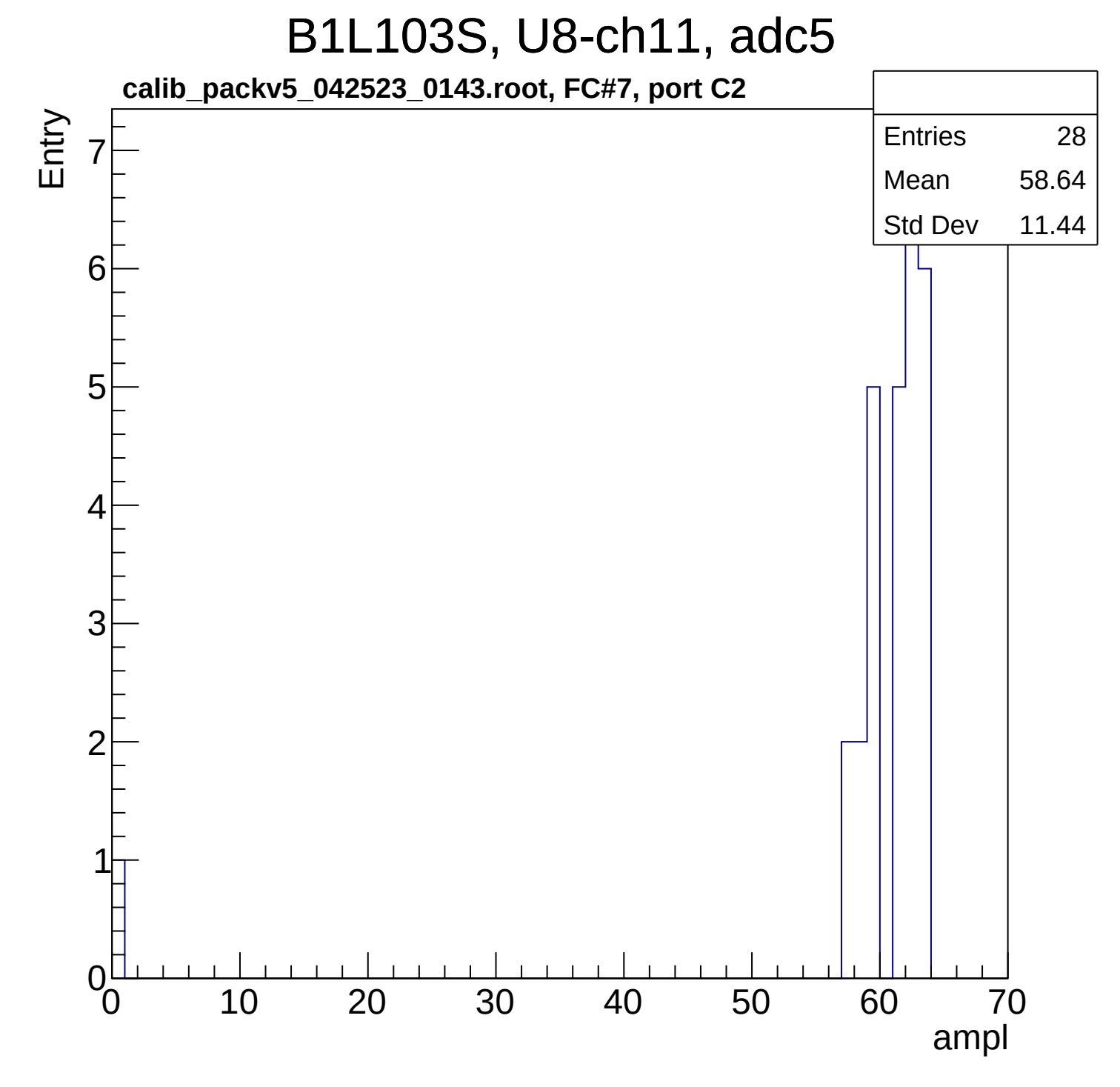

B1L103S, U8-ch11, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 31.79
Std Dev 3.118
Gaus mean : 31.3764
Gaus Width: 3.6959
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

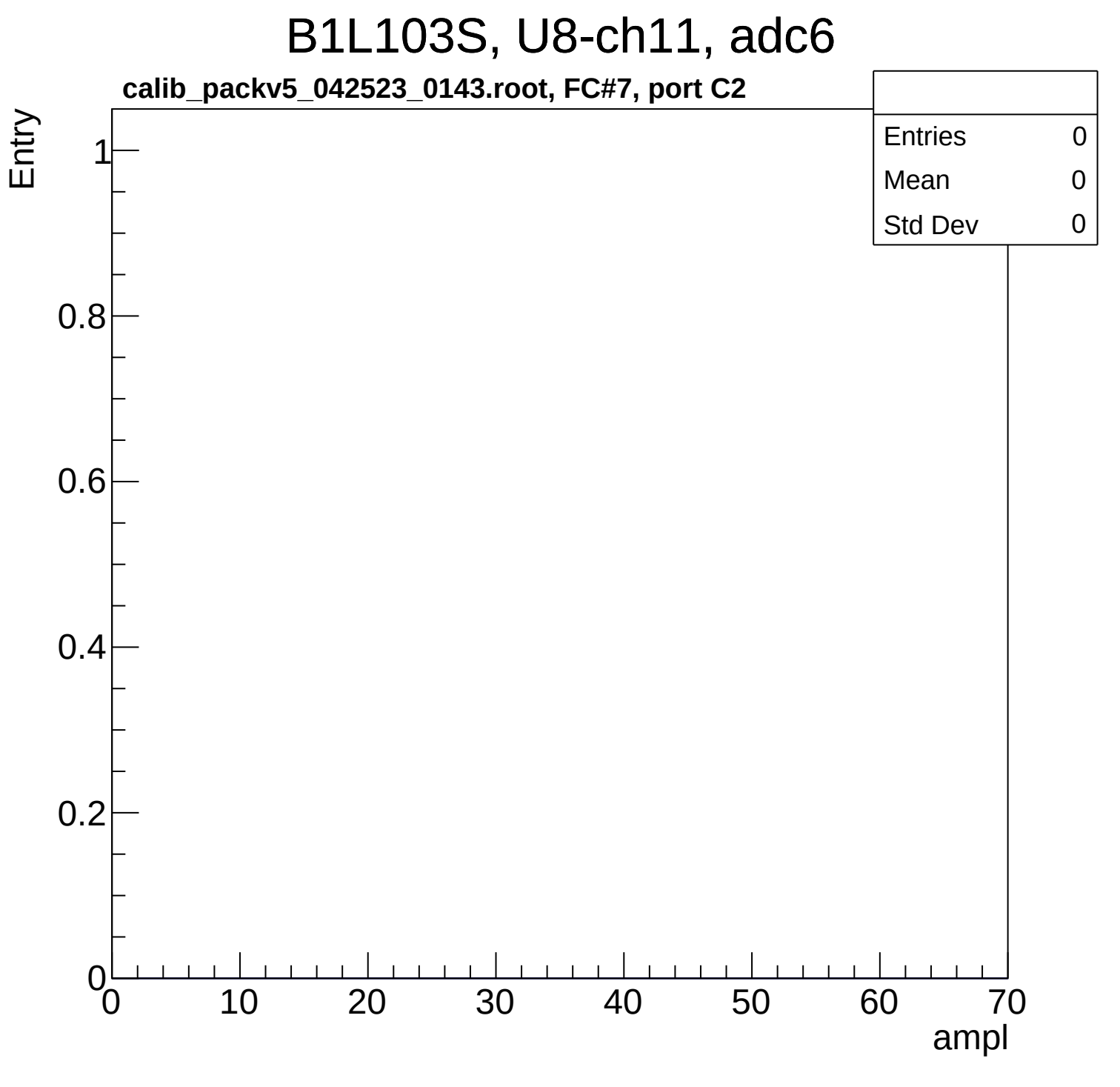

B1L103S, U8-ch11, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 38.78
Std Dev 3.569
Gaus mean : 39.0215
Gaus Width: 4.0322
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

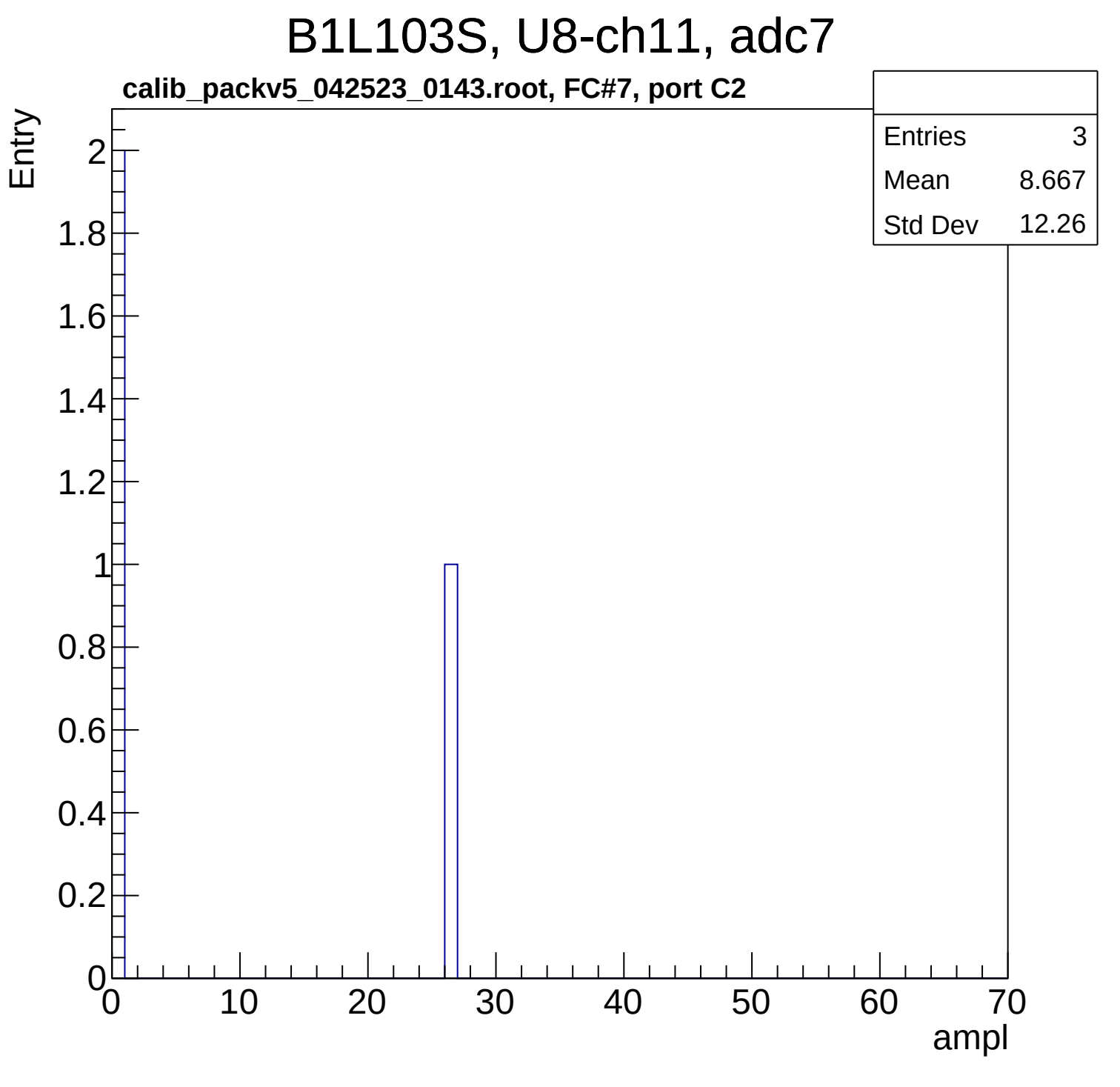

B1L103S, U8-ch11, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 45.02
Std Dev 3.568
Gaus mean : 45.6232
Gaus Width: 4.0100
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

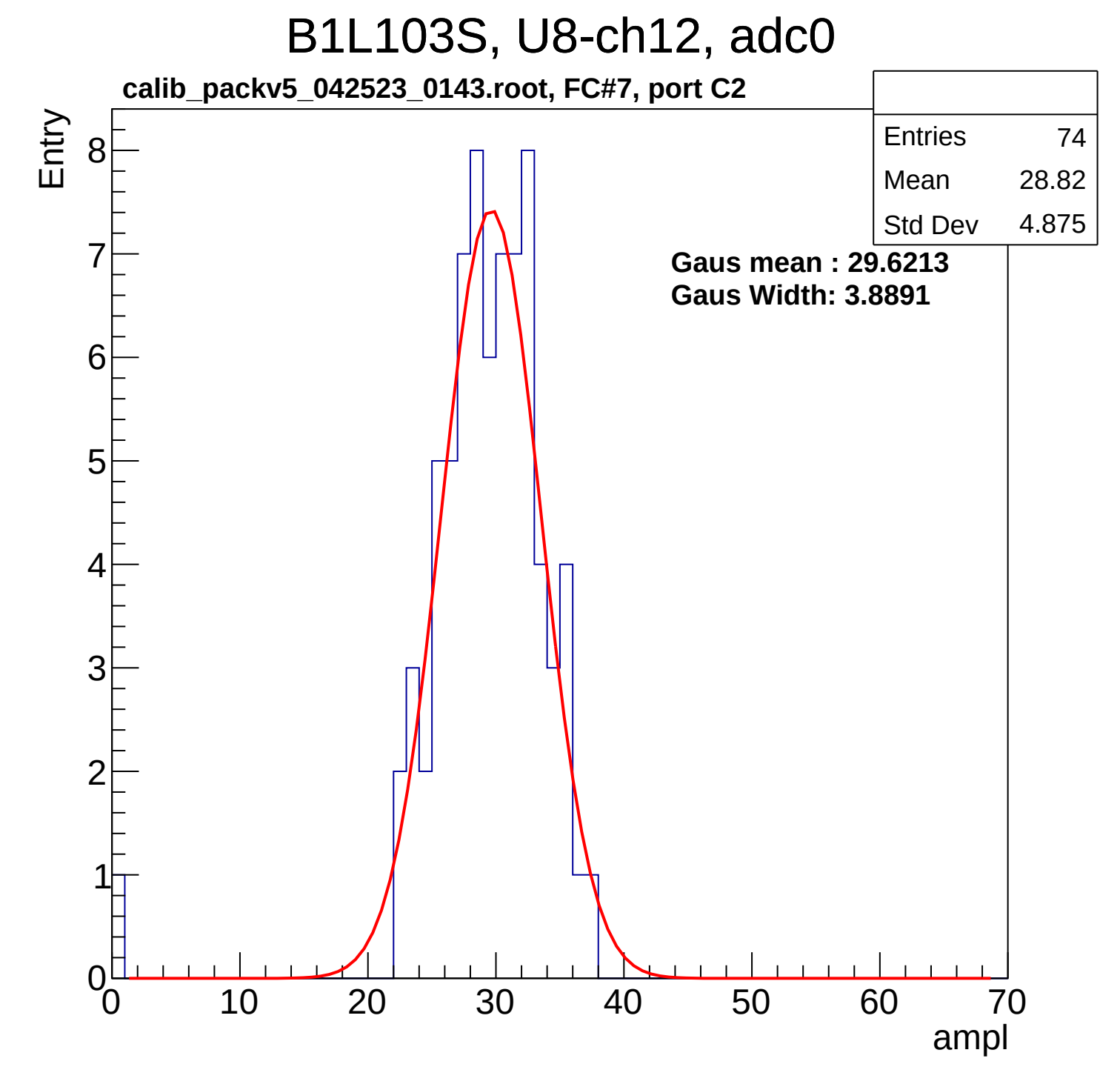

B1L103S, U8-ch11, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 51.54
Std Dev 3.388
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

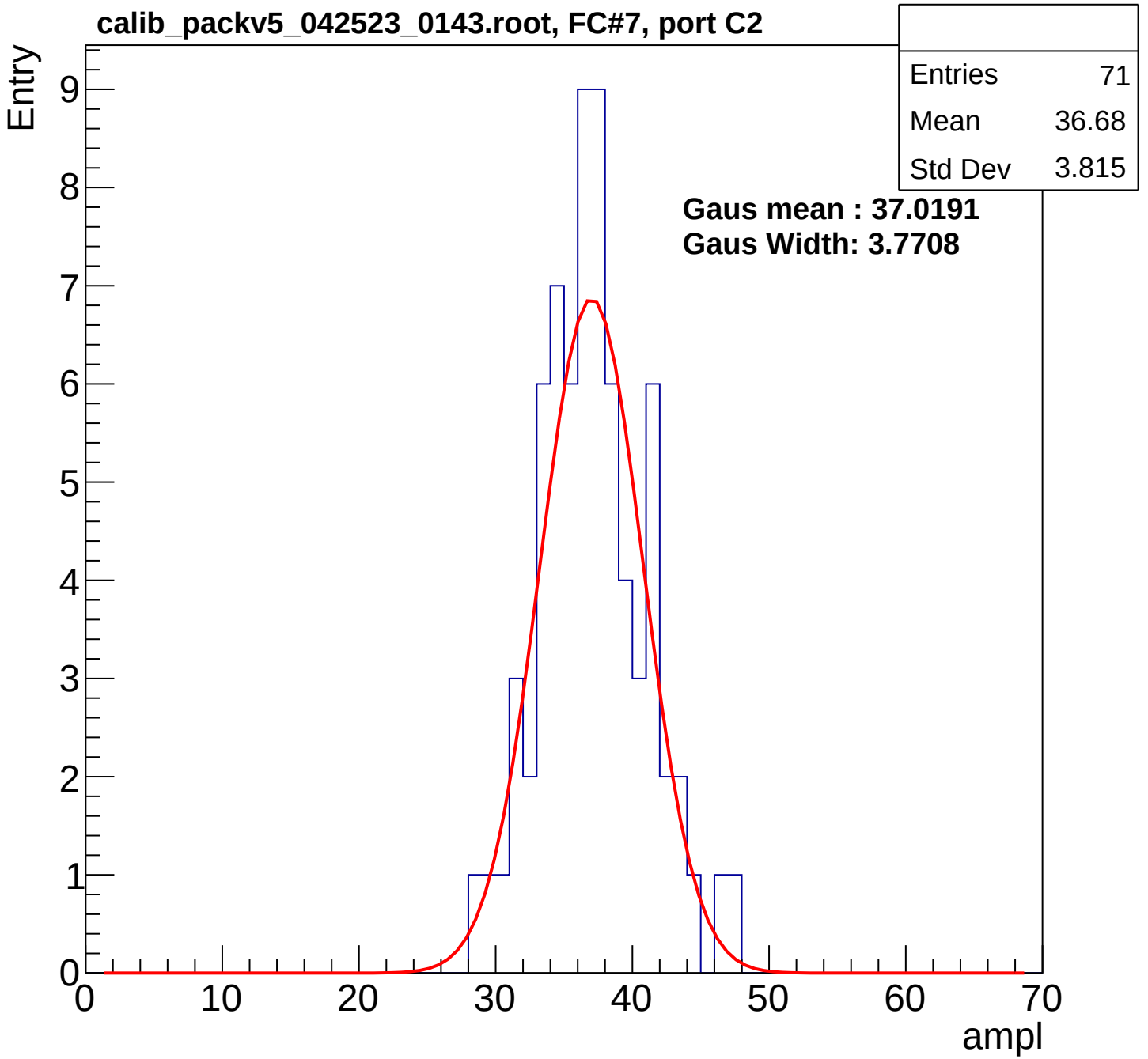

B1L103S, U8-ch11, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 57.47
Std Dev 3.463
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

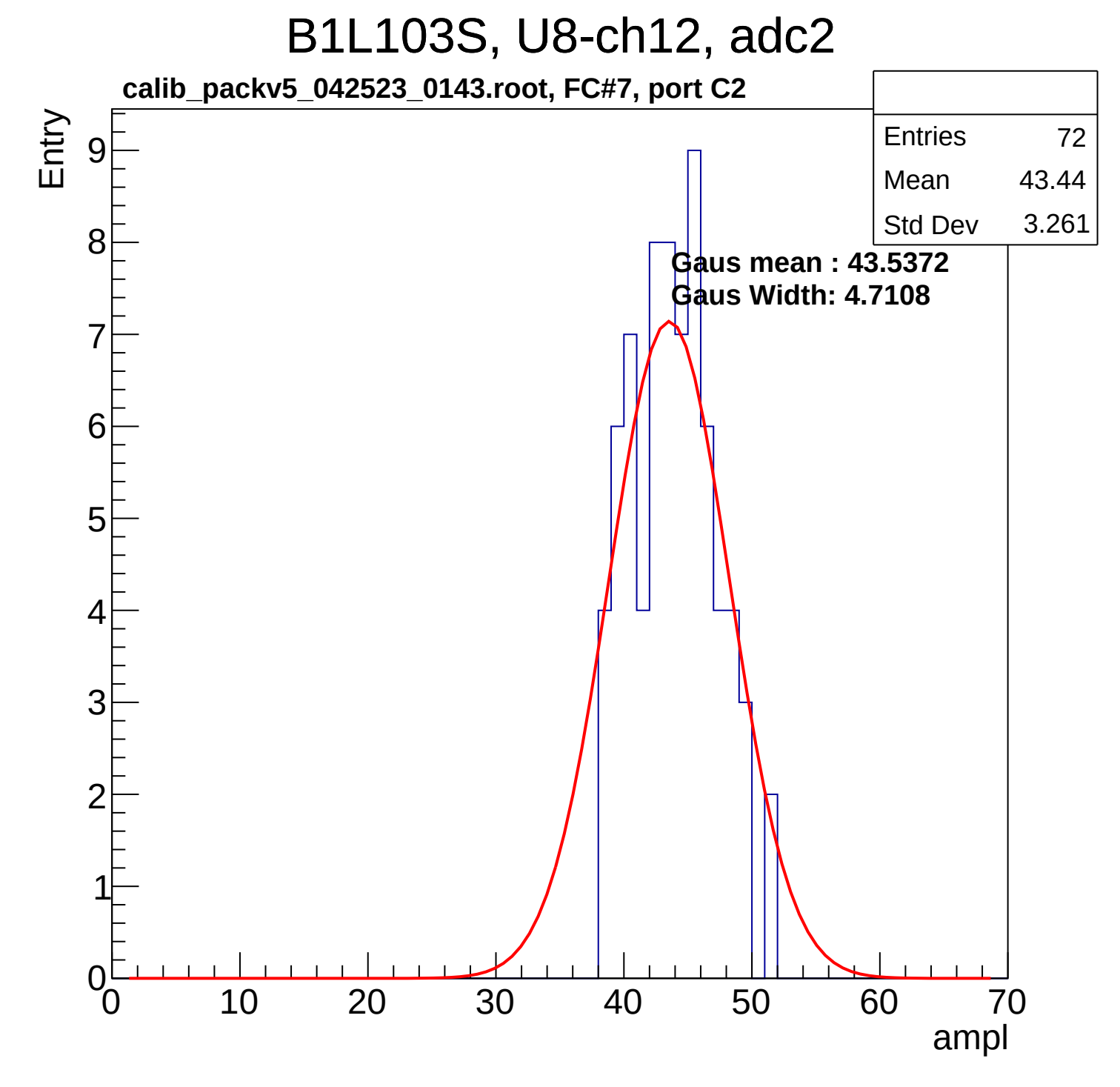

B1L103S, U8-ch11, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 28
Mean 58.64
Std Dev 11.44
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

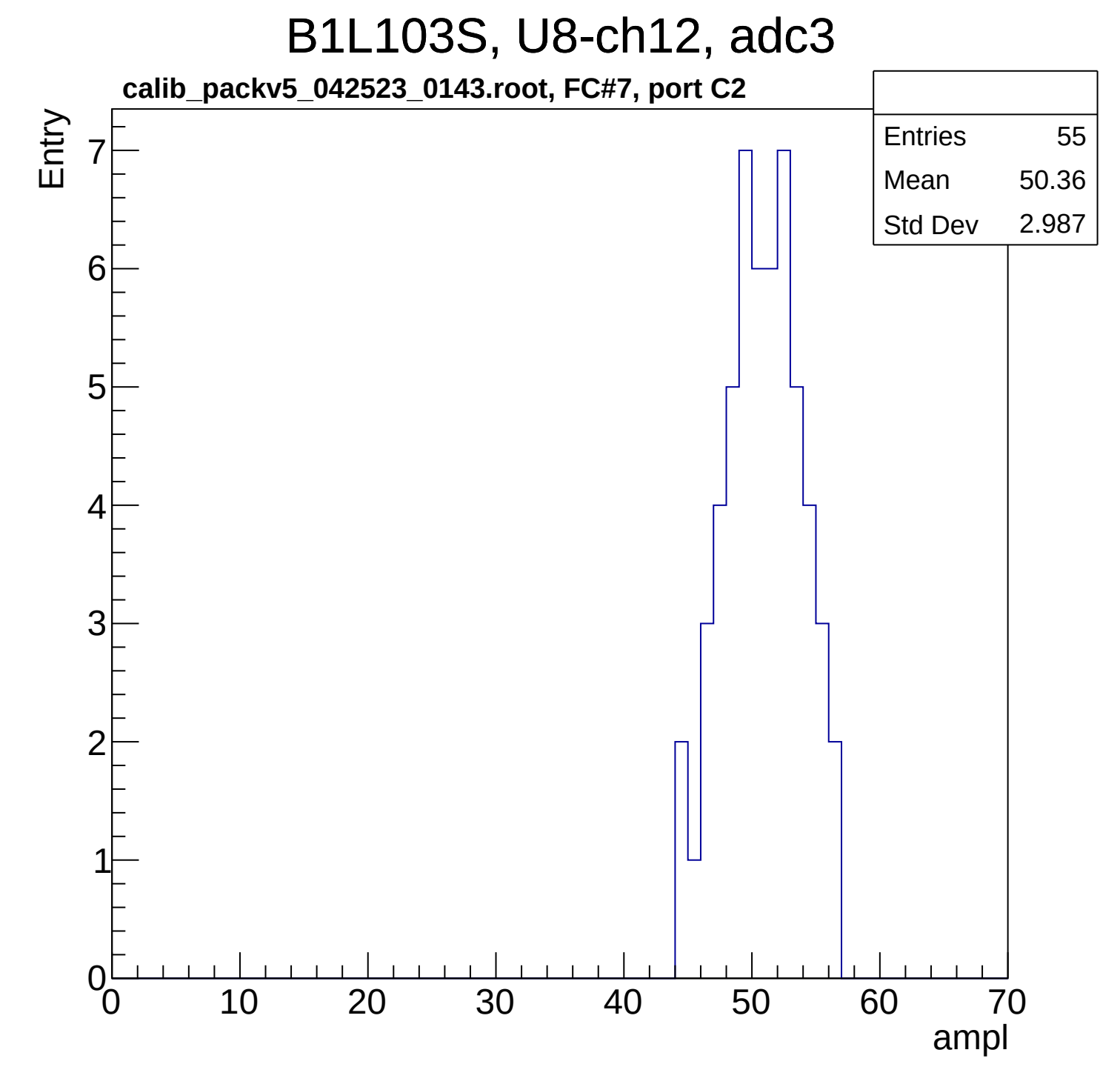

B1L103S, U8-ch11, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

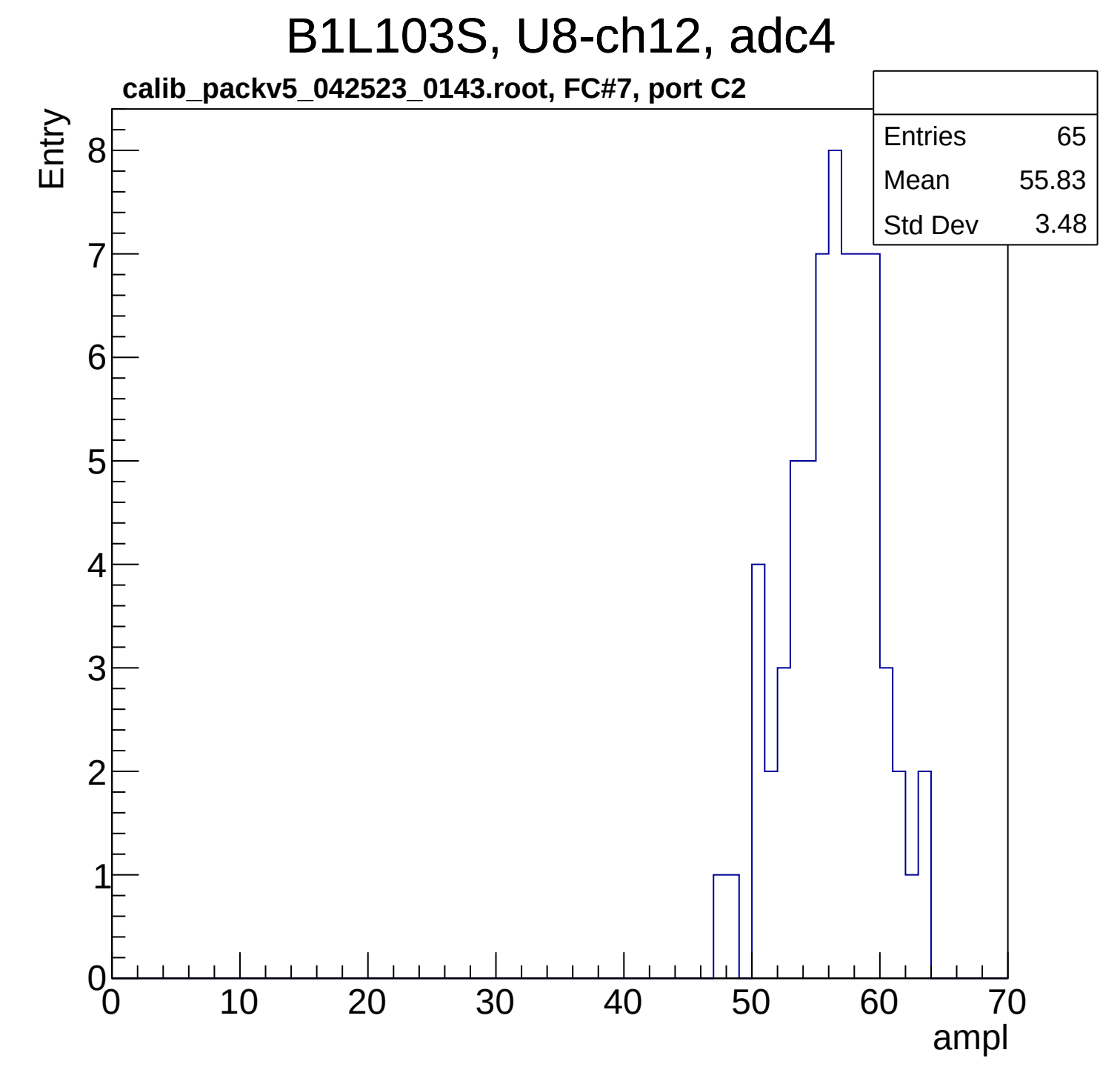

B1L103S, U8-ch11, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 8.667
Std Dev 12.26
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

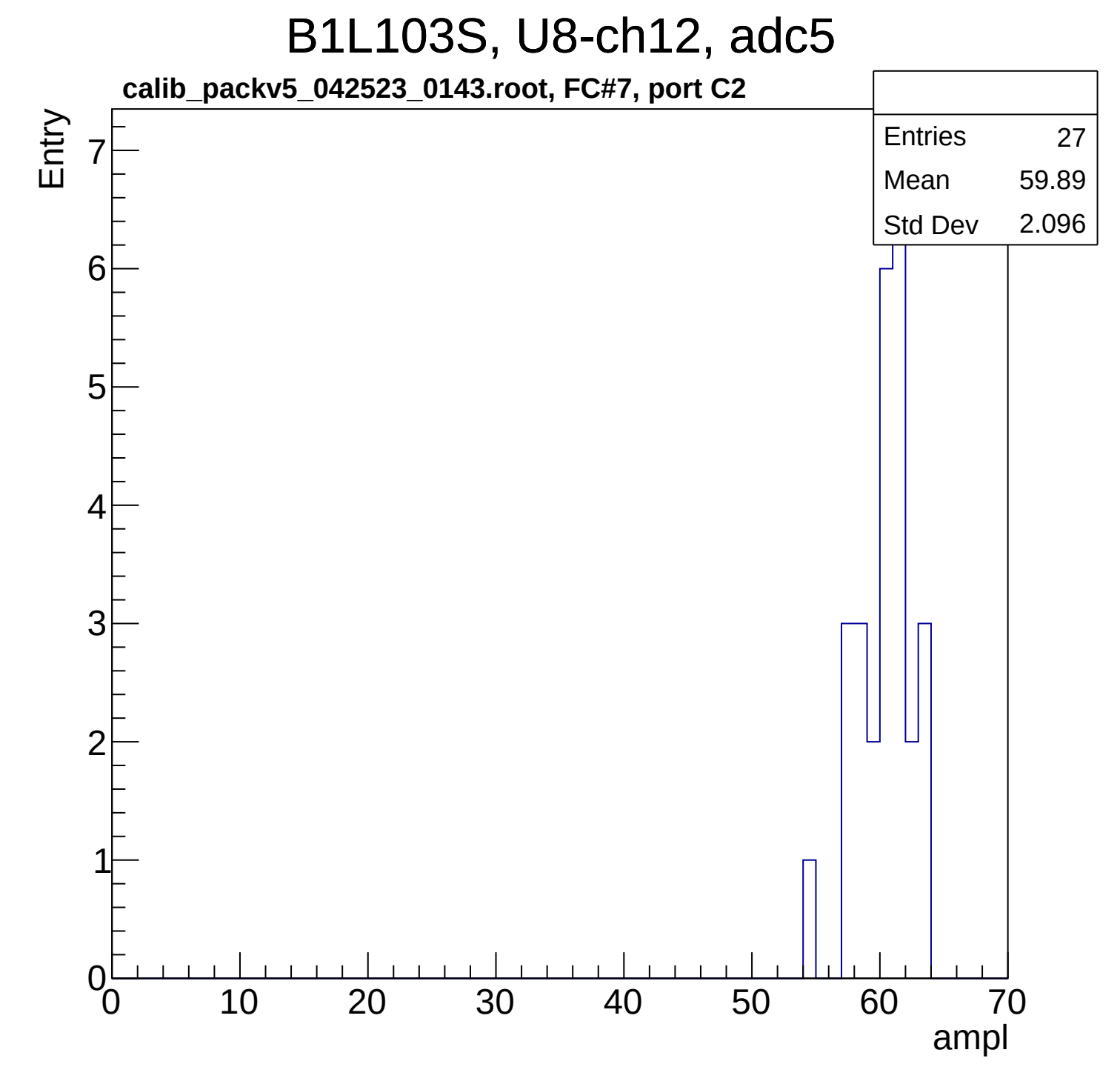

B1L103S, U8-ch12, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 28.82
Std Dev 4.875
Gaus mean : 29.6213
Gaus Width: 3.8891
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

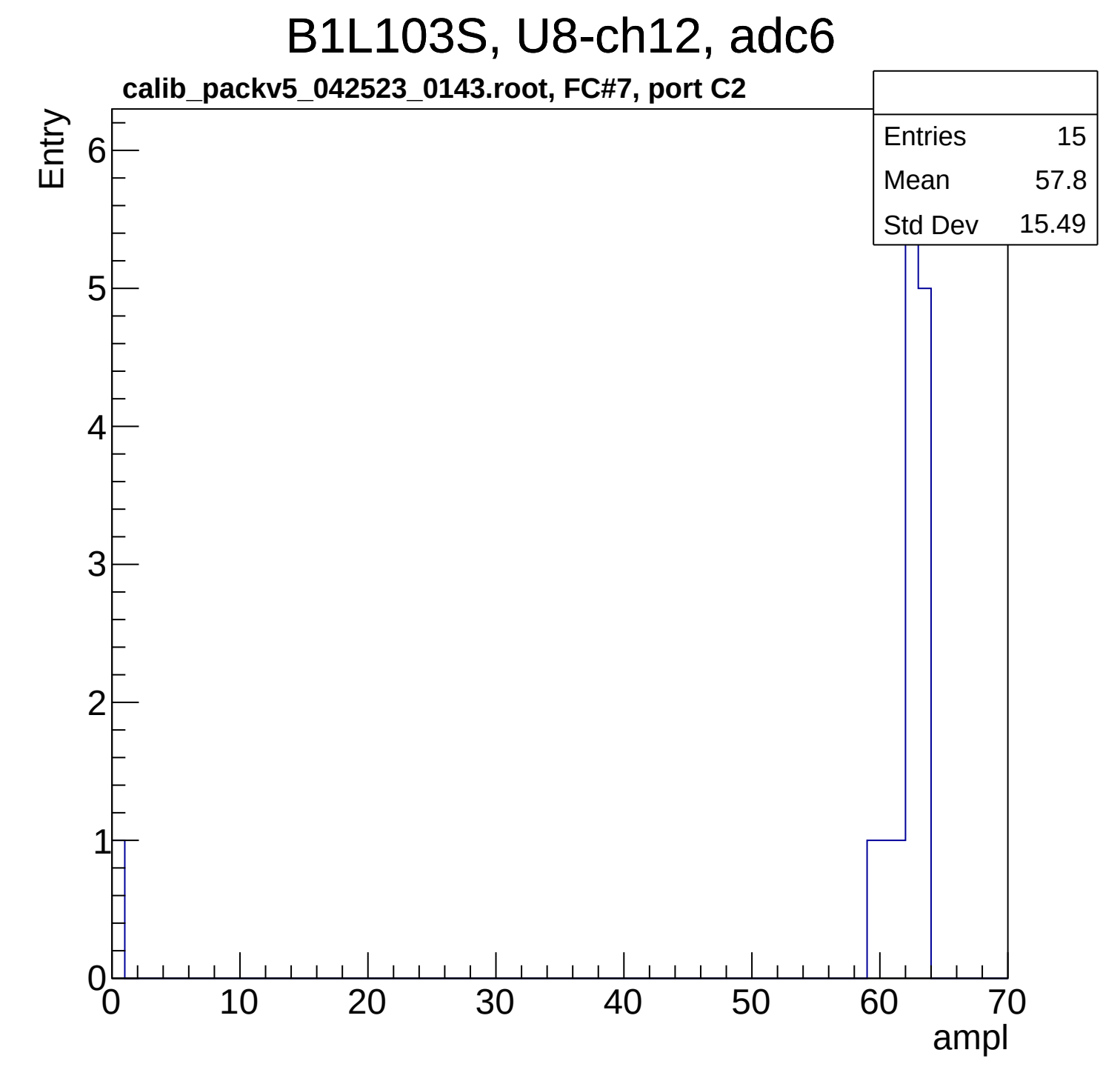

B1L103S, U8-ch12, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 36.68
Std Dev 3.815
Gaus mean : 37.0191
Gaus Width: 3.7708
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

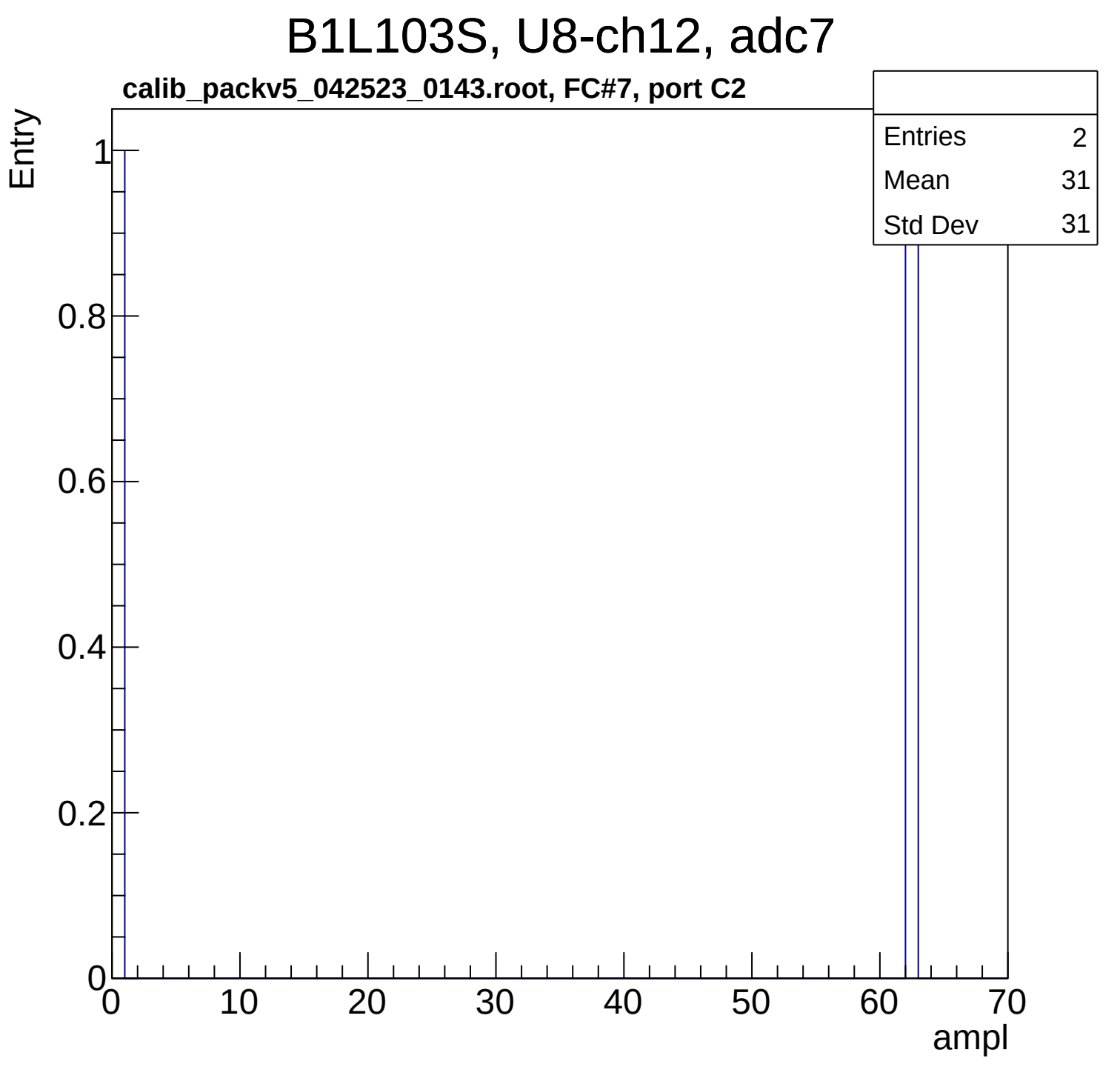

B1L103S, U8-ch12, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 43.44
Std Dev 3.261
Gaus mean : 43.5372
Gaus Width: 4.7108
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

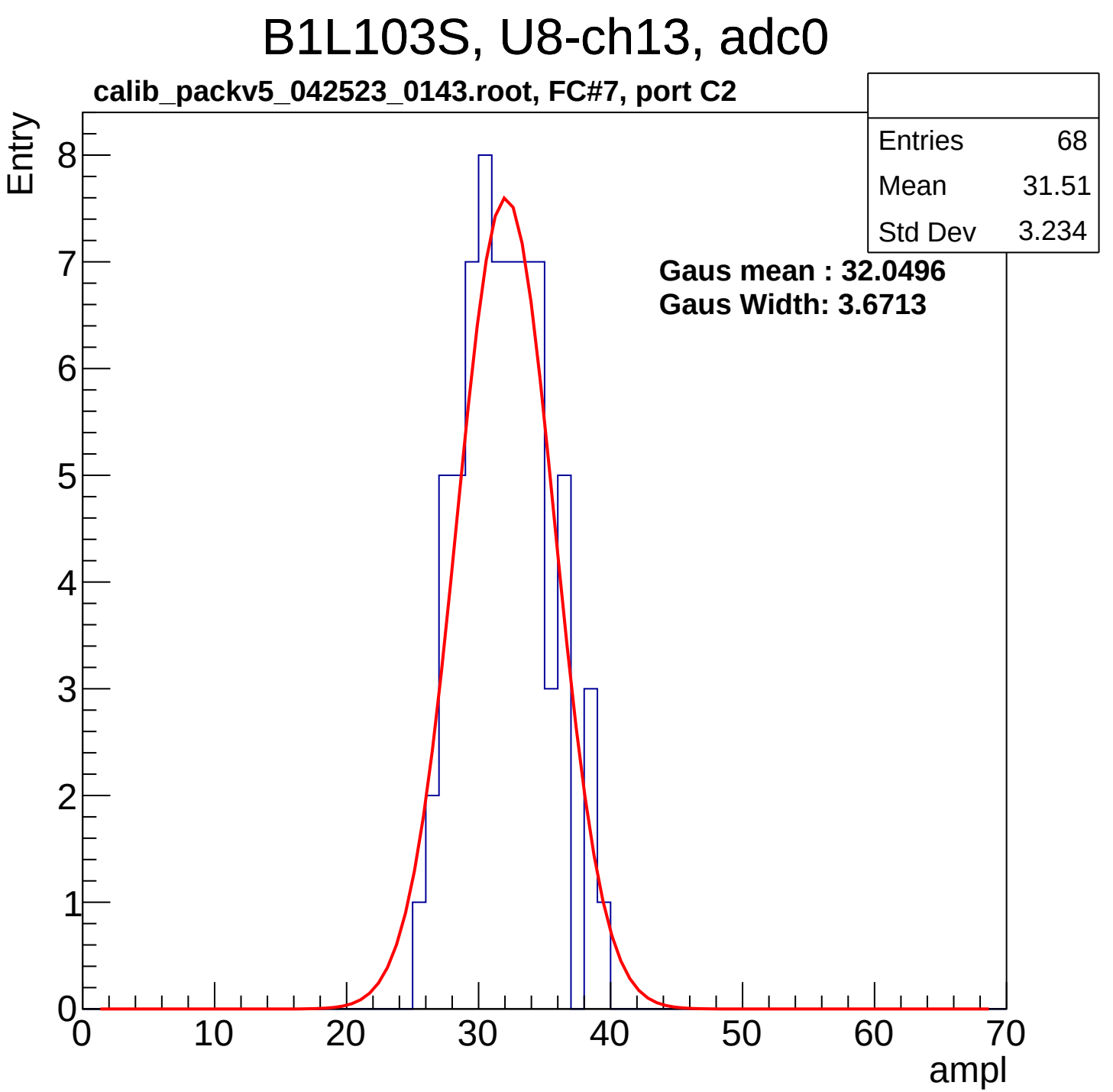

B1L103S, U8-ch12, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 50.36
Std Dev 2.987
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

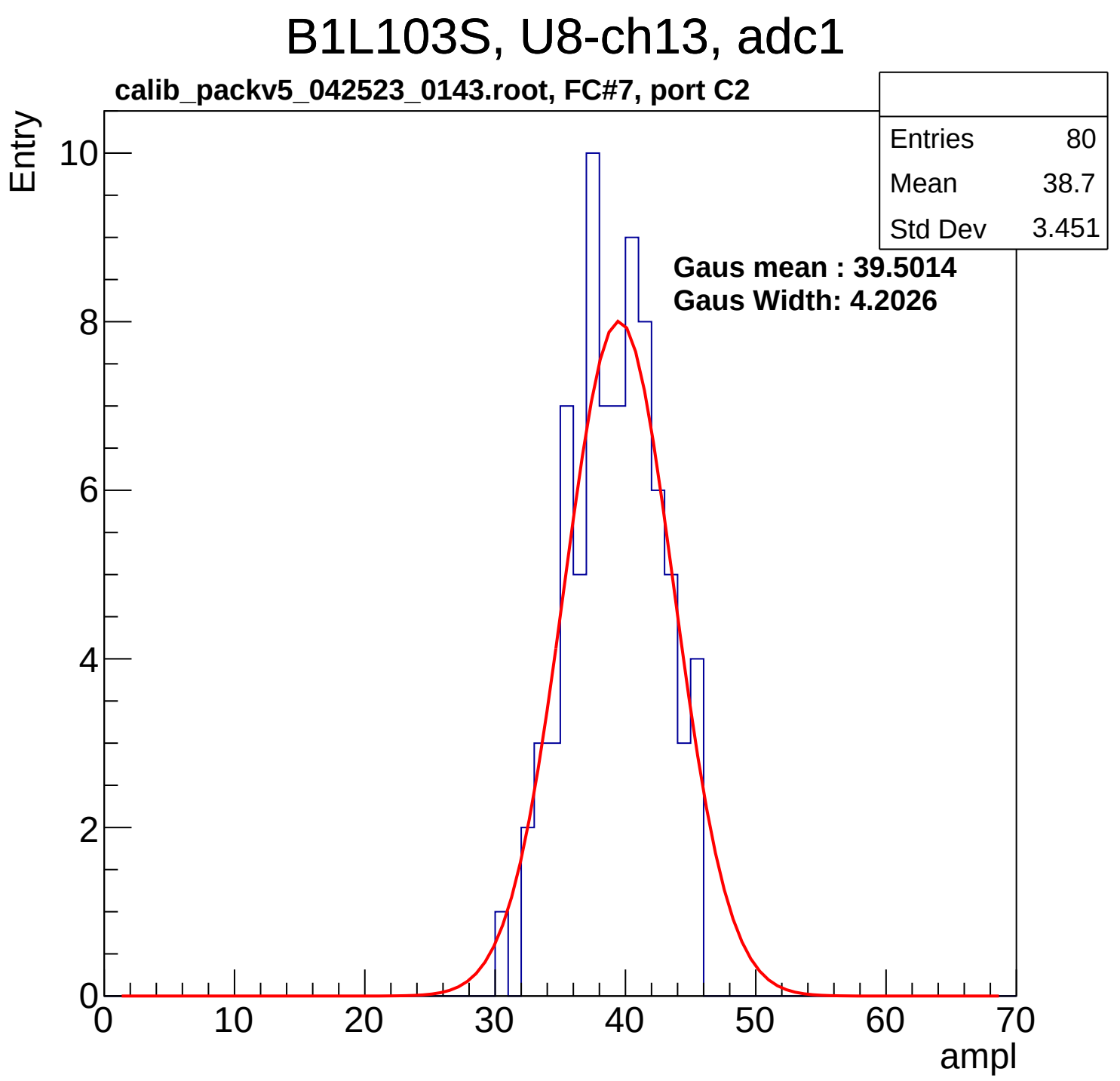

B1L103S, U8-ch12, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 55.83
Std Dev 3.48
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

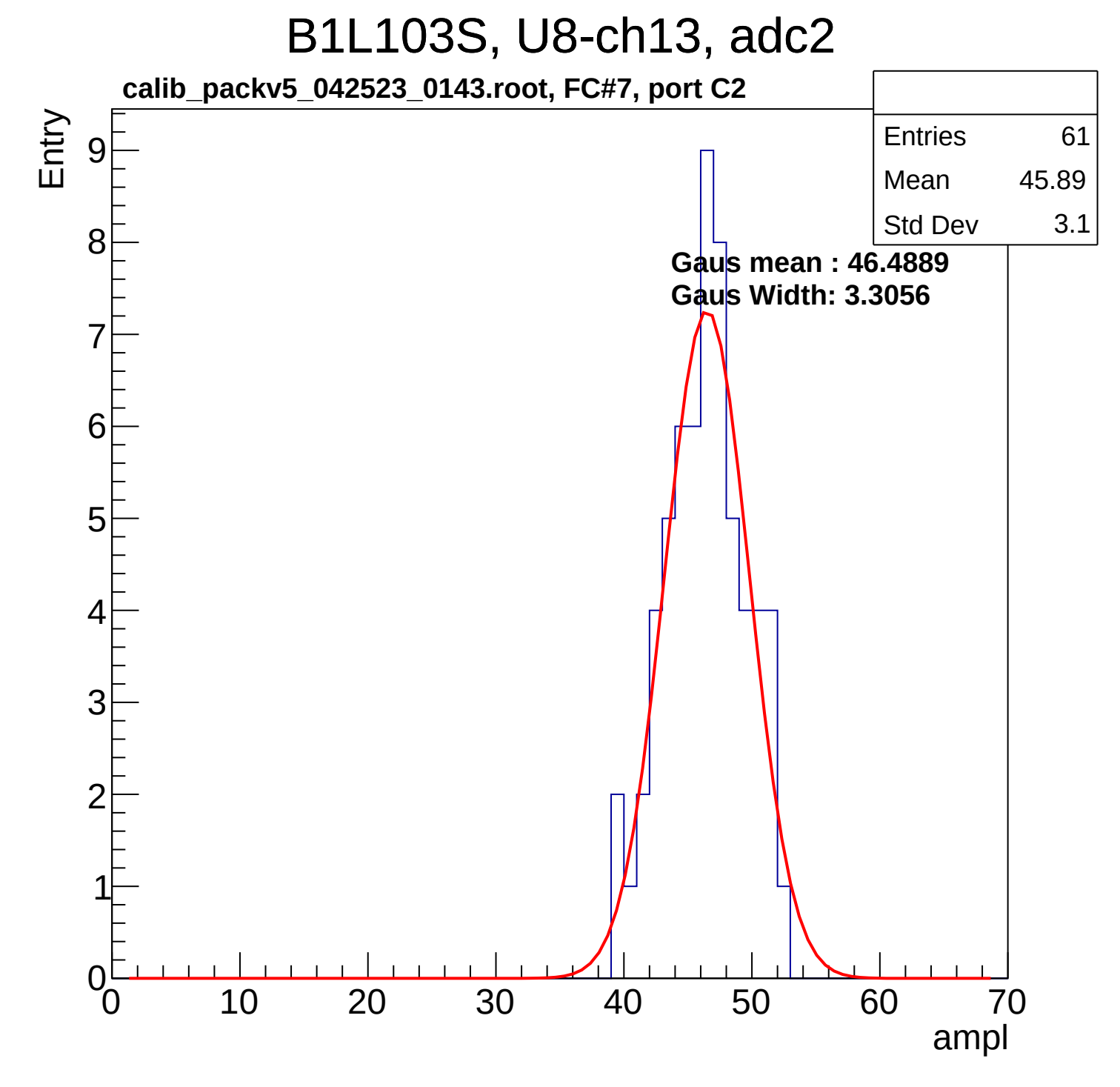

B1L103S, U8-ch12, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 27
Mean 59.89
Std Dev 2.096
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

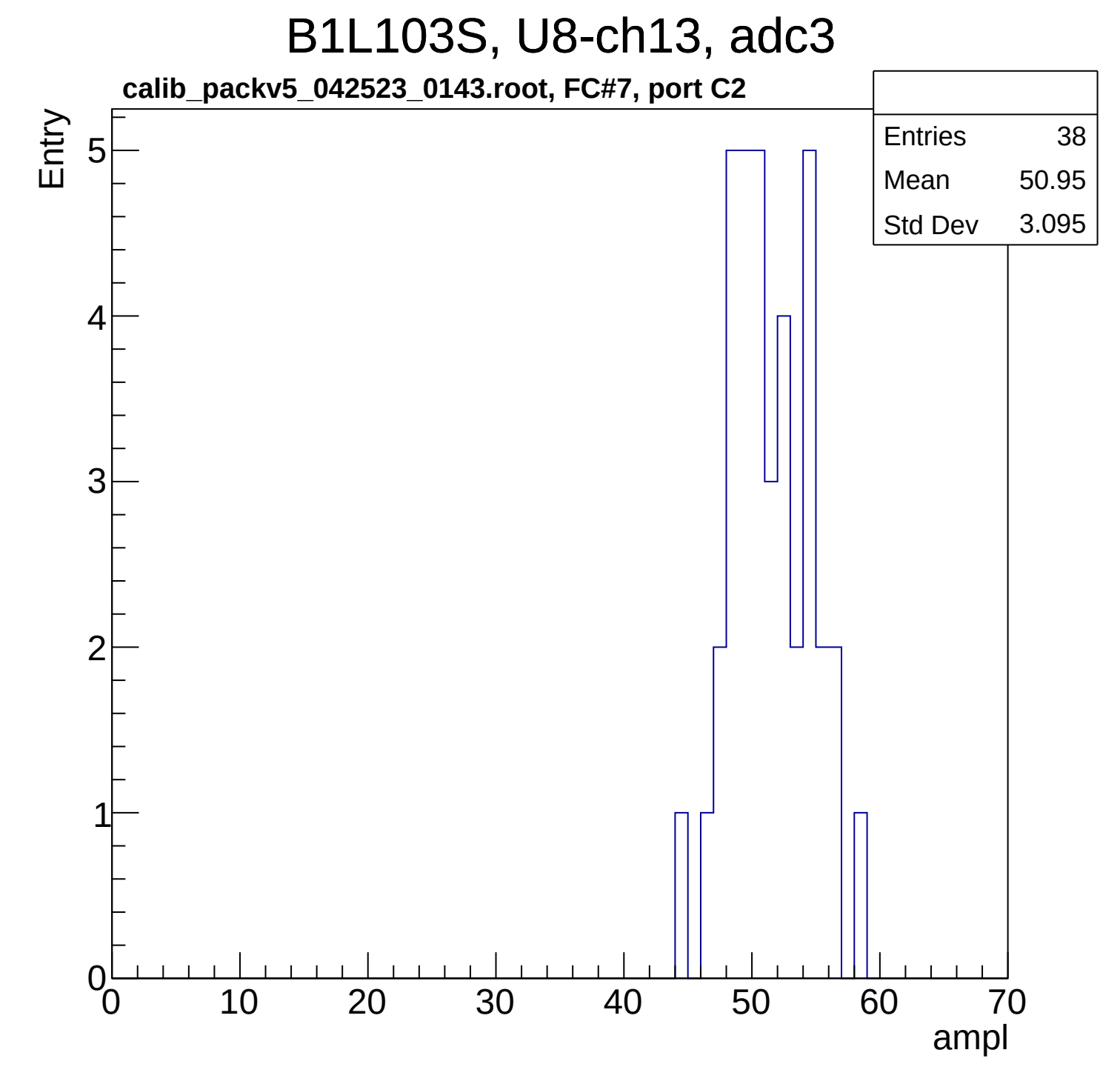

B1L103S, U8-ch12, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 15
Mean 57.8
Std Dev 15.49
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

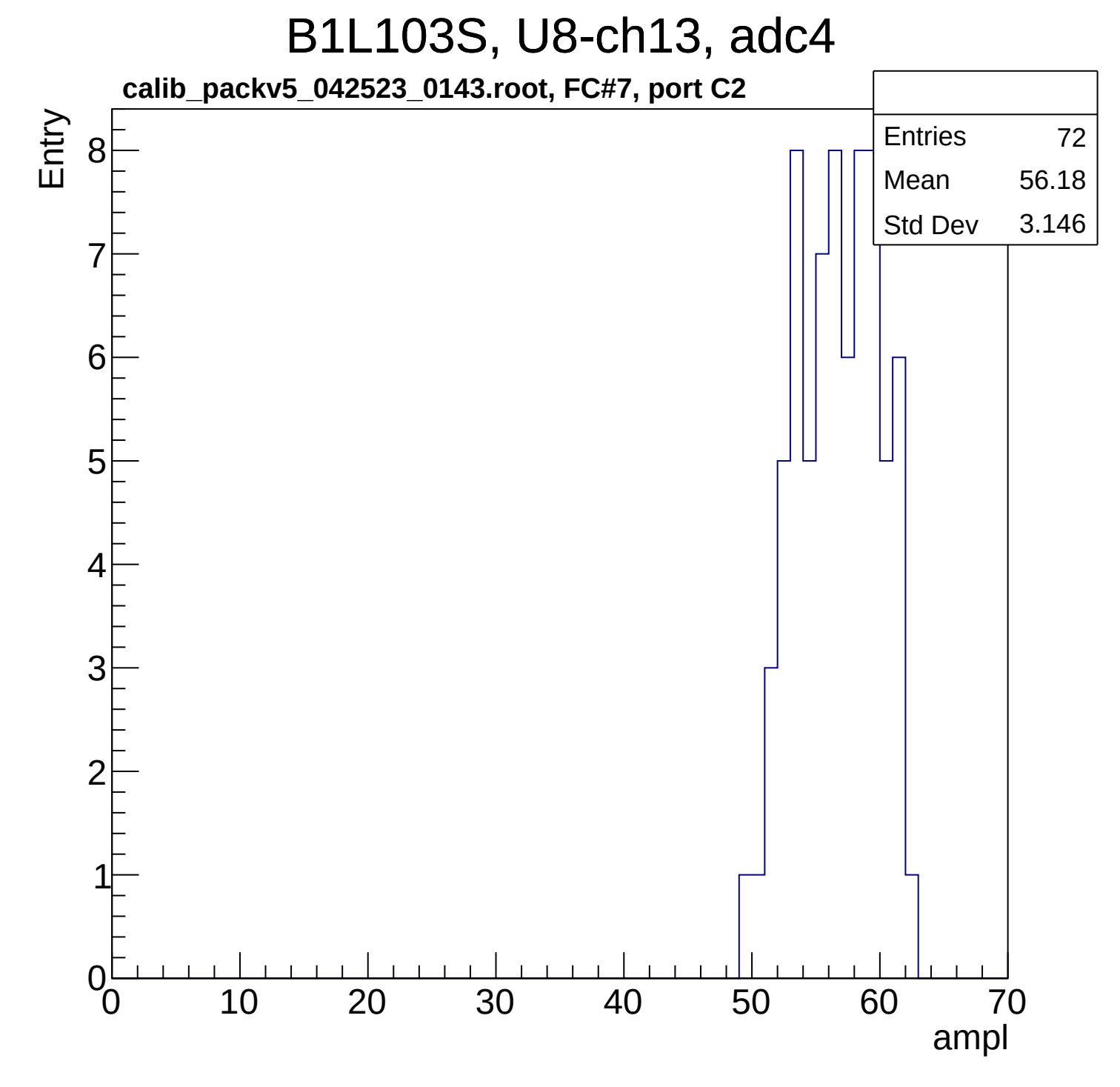

B1L103S, U8-ch12, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 31
Std Dev 31
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

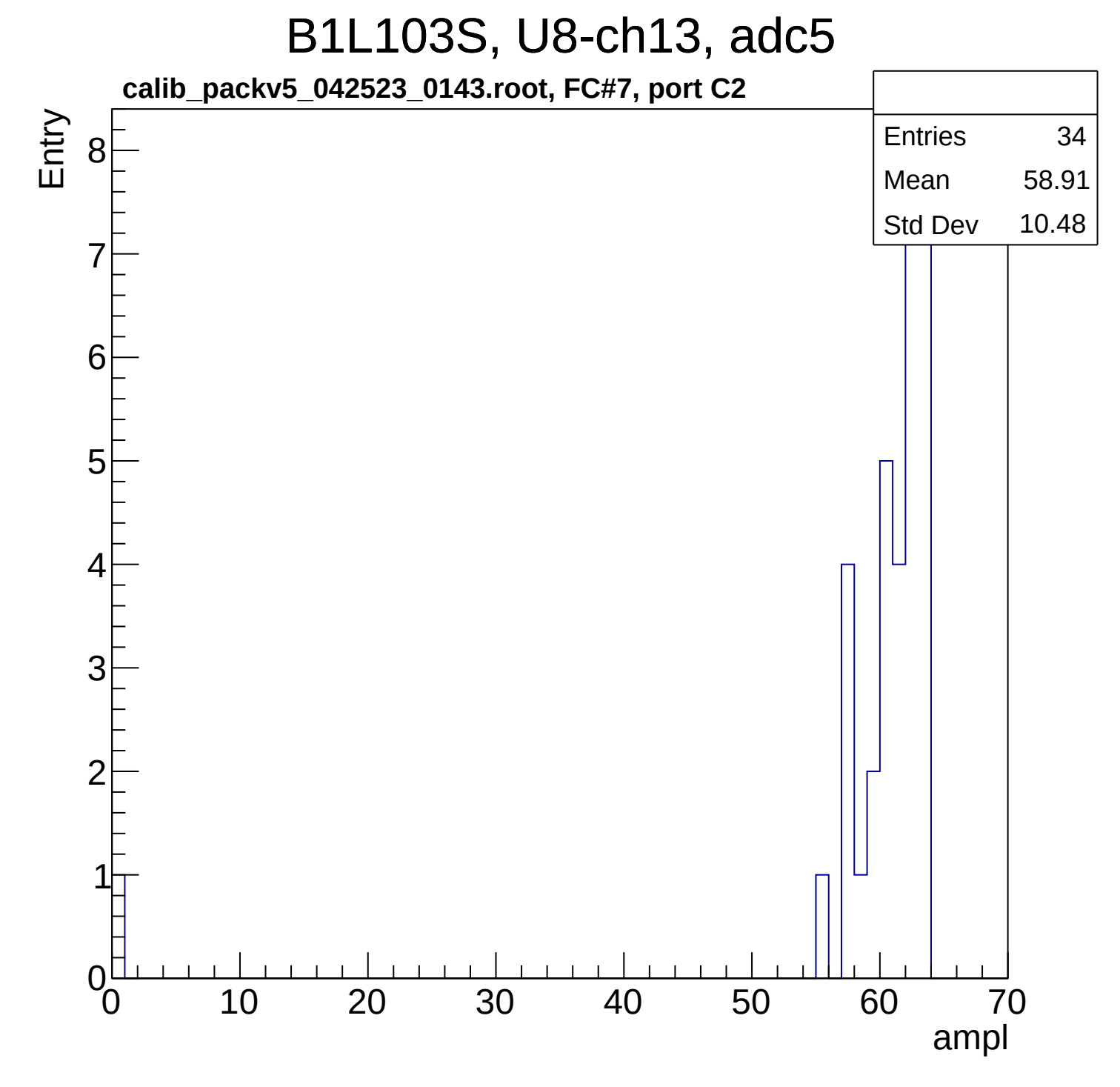

B1L103S, U8-ch13, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 31.51
Std Dev 3.234
Gaus mean : 32.0496
Gaus Width: 3.6713
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

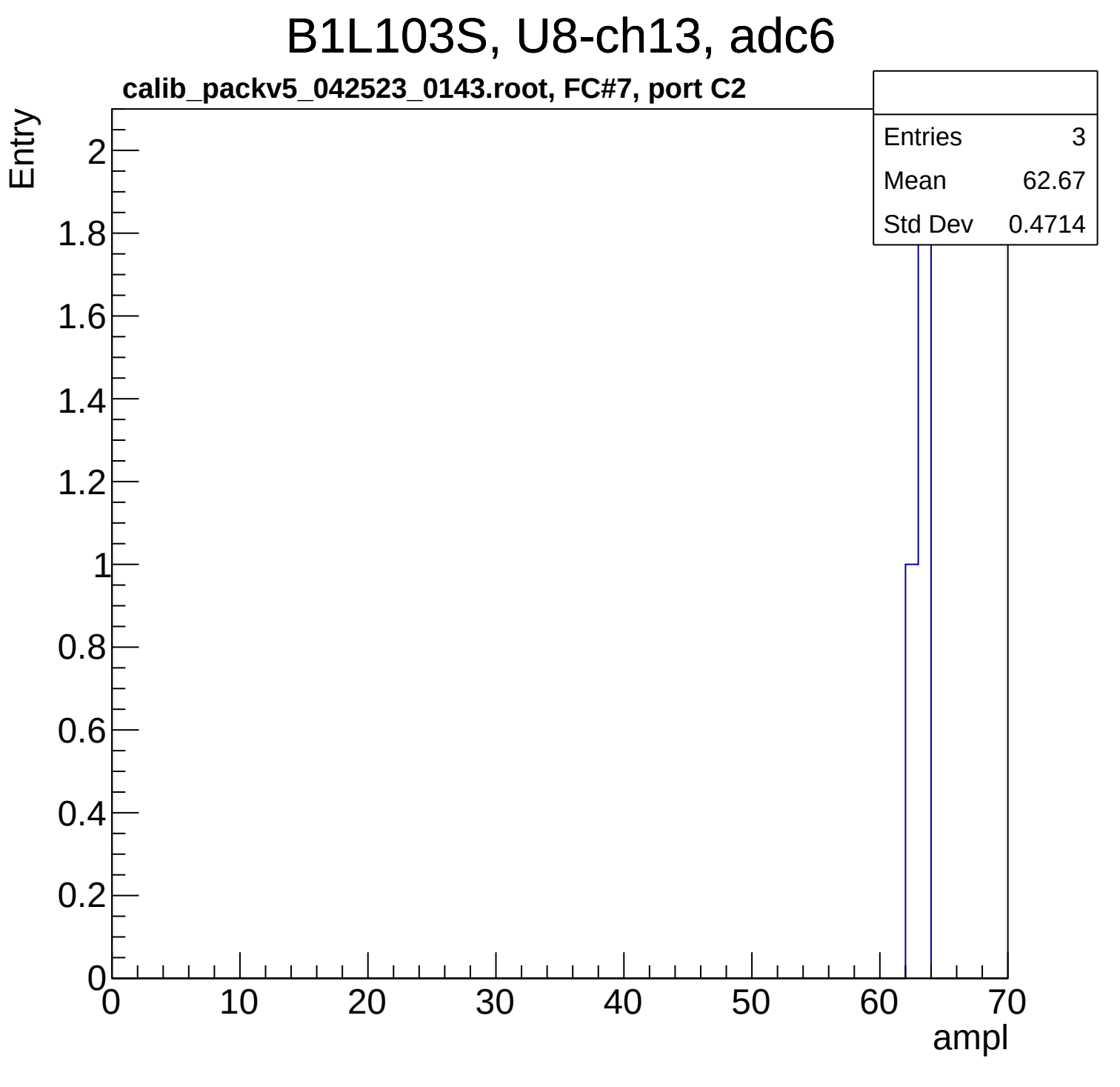

B1L103S, U8-ch13, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 80
Mean 38.7
Std Dev 3.451
Gaus mean : 39.5014
Gaus Width: 4.2026
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

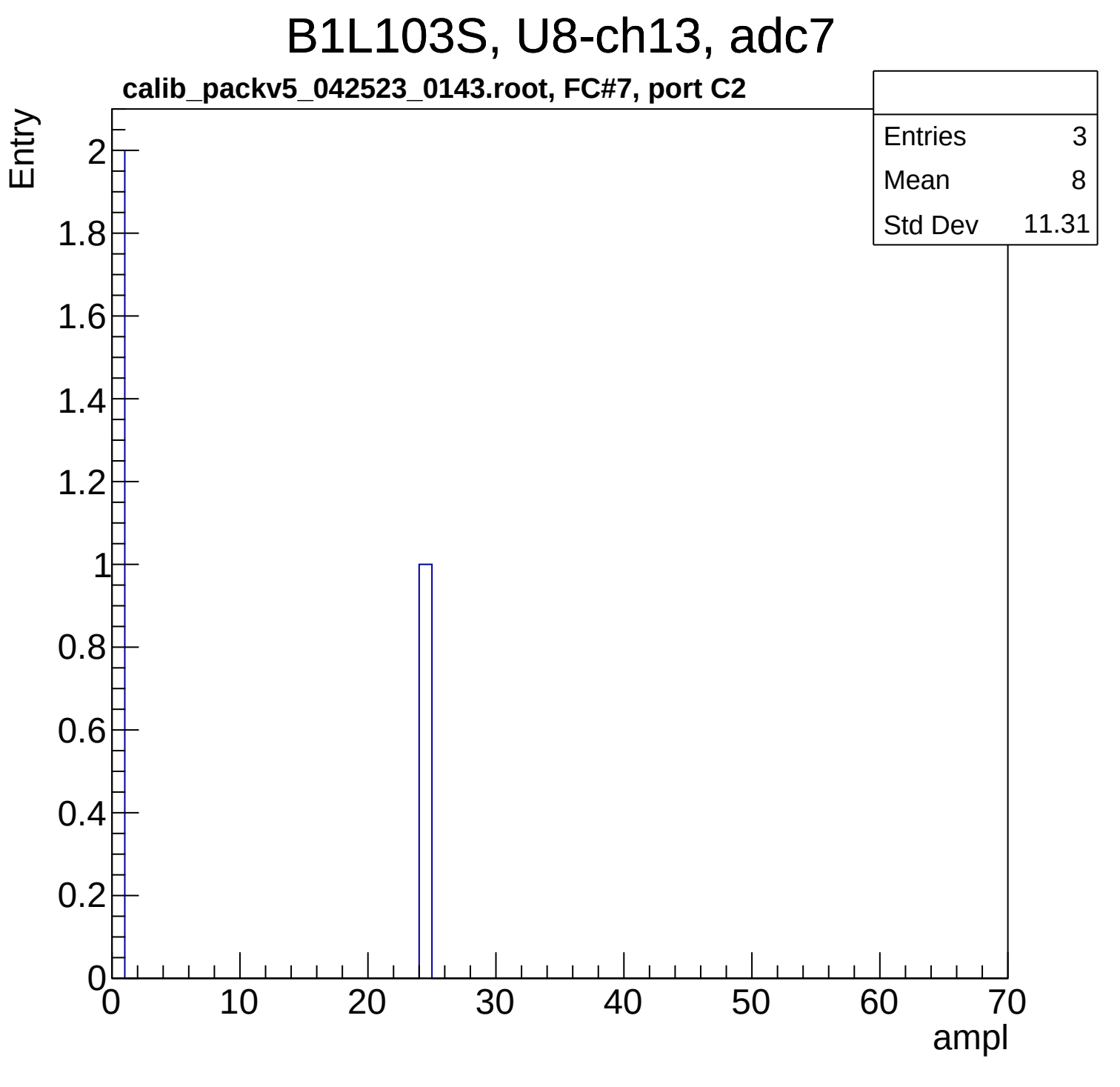

B1L103S, U8-ch13, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 45.89
Std Dev 3.1
Gaus mean : 46.4889
Gaus Width: 3.3056
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

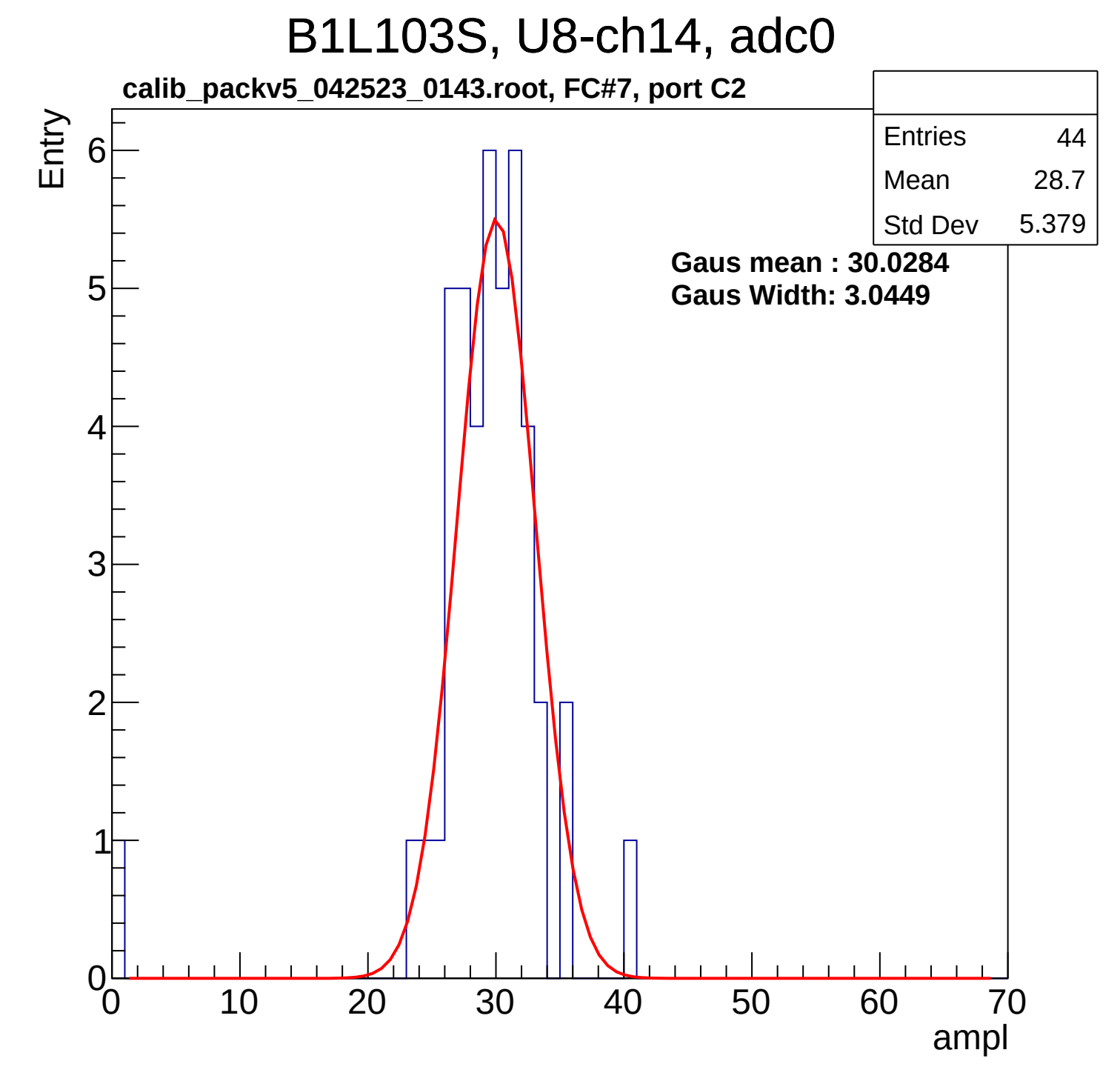

B1L103S, U8-ch13, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 38
Mean 50.95
Std Dev 3.095
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

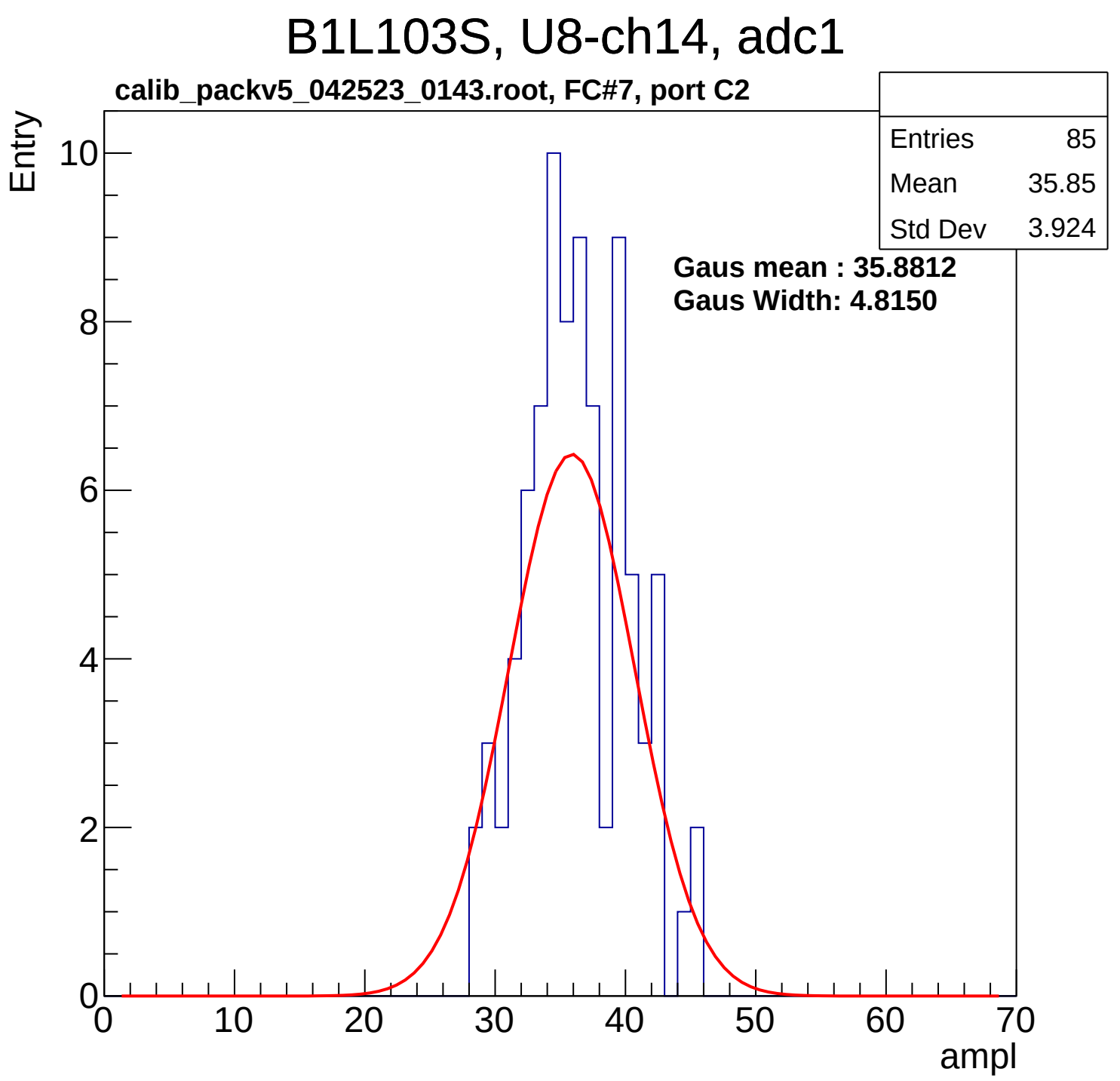

B1L103S, U8-ch13, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 56.18
Std Dev 3.146
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

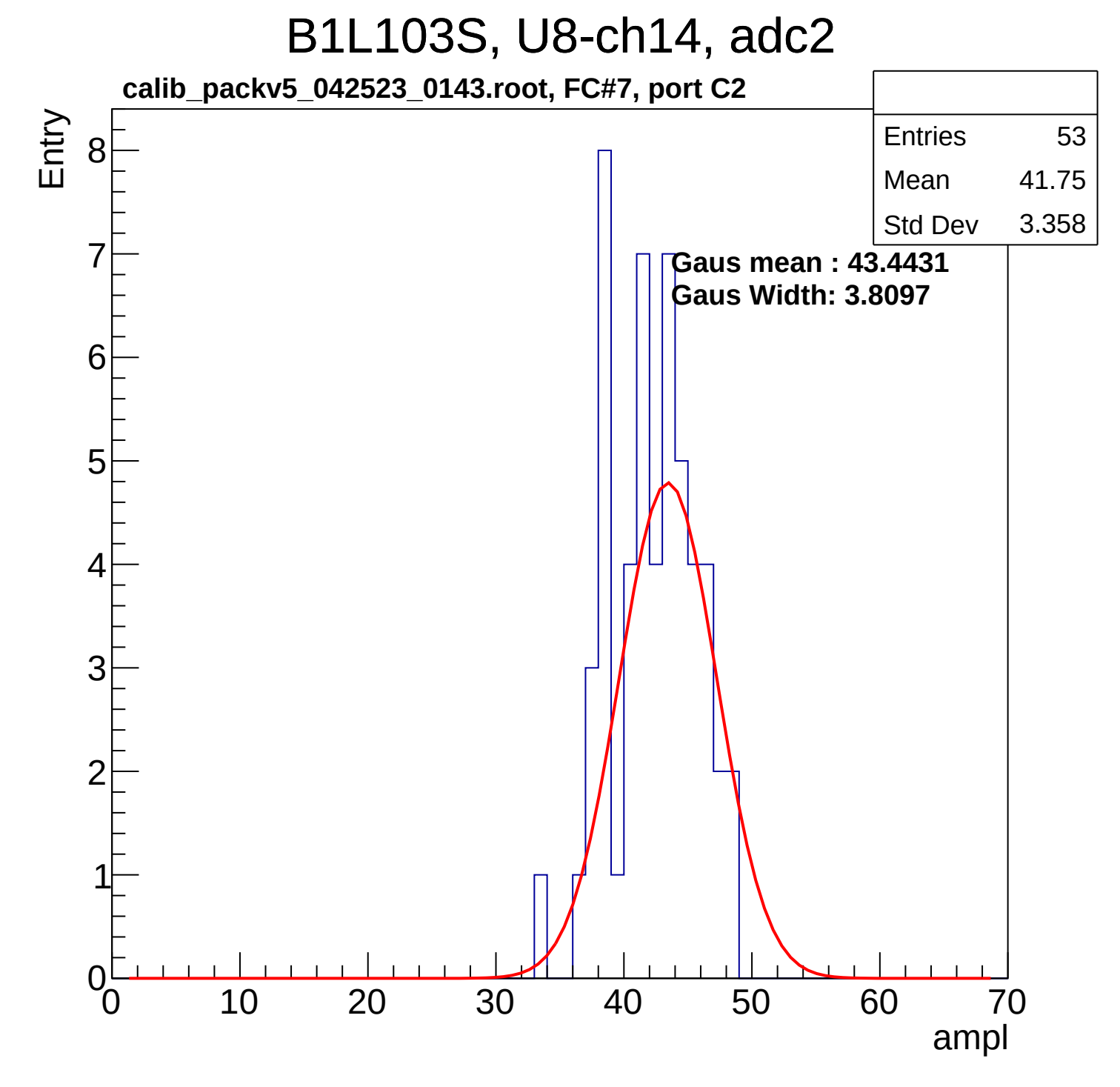

B1L103S, U8-ch13, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 34
Mean 58.91
Std Dev 10.48
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

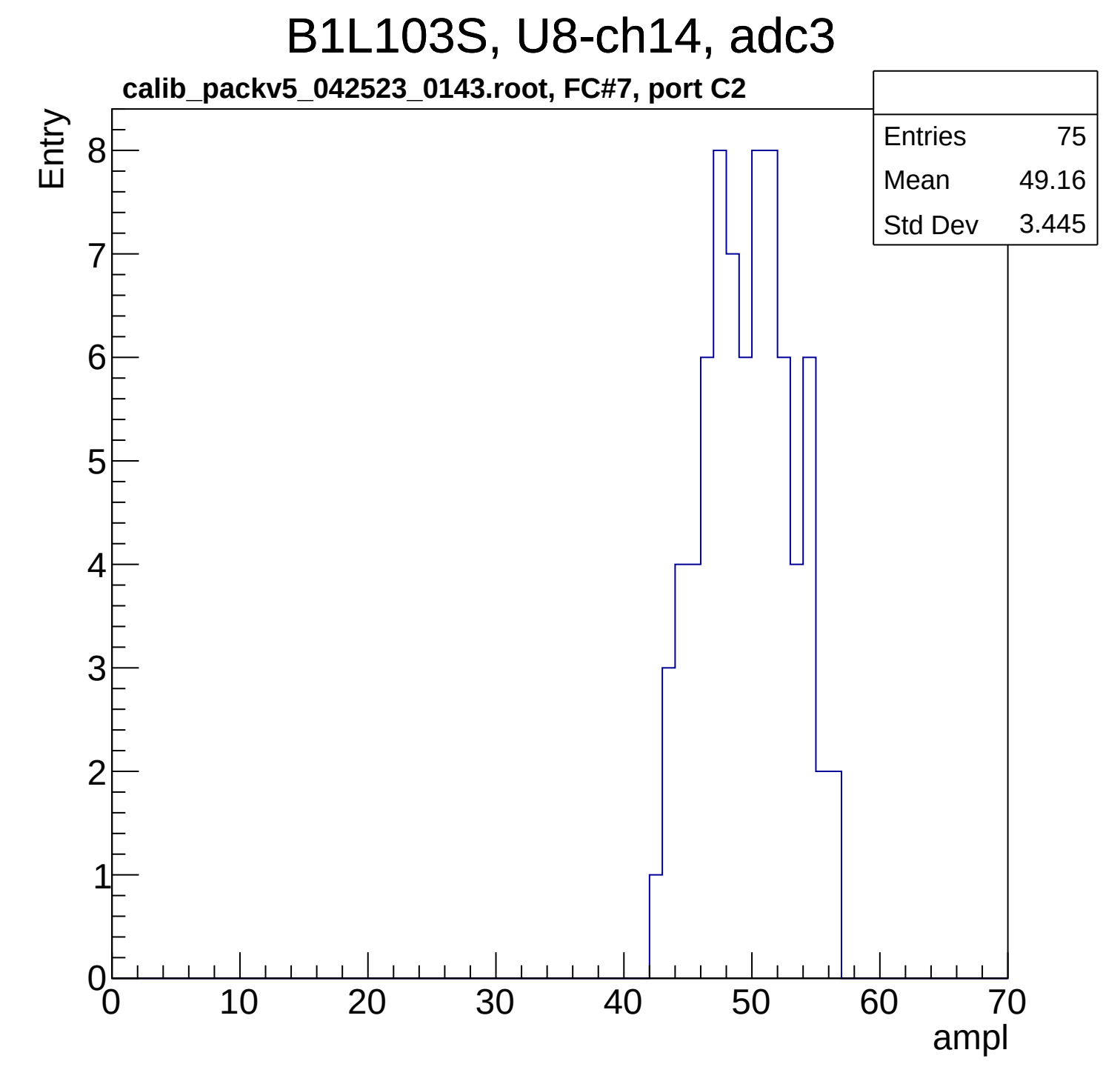

B1L103S, U8-ch13, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

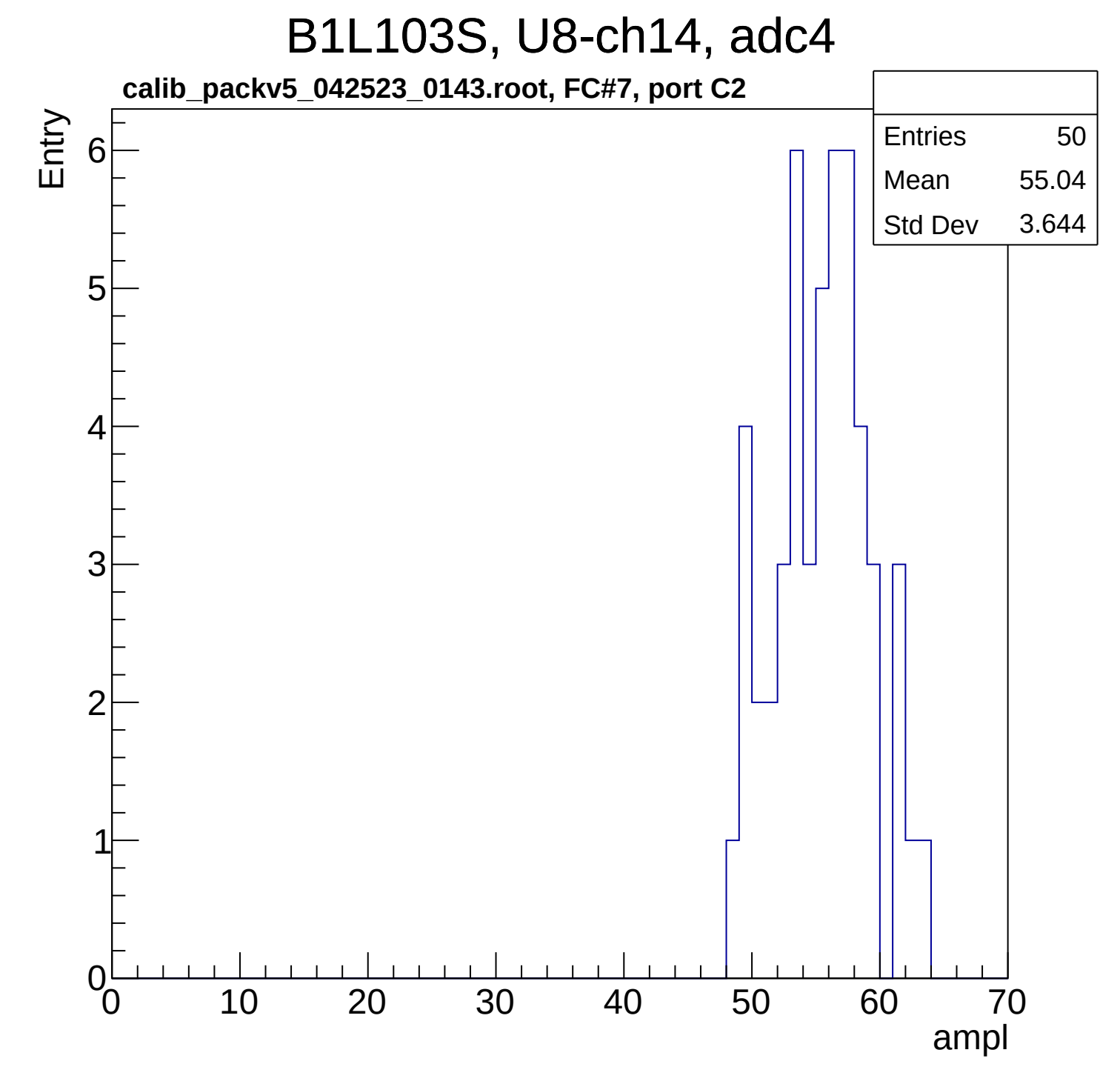

B1L103S, U8-ch13, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 8
Std Dev 11.31
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

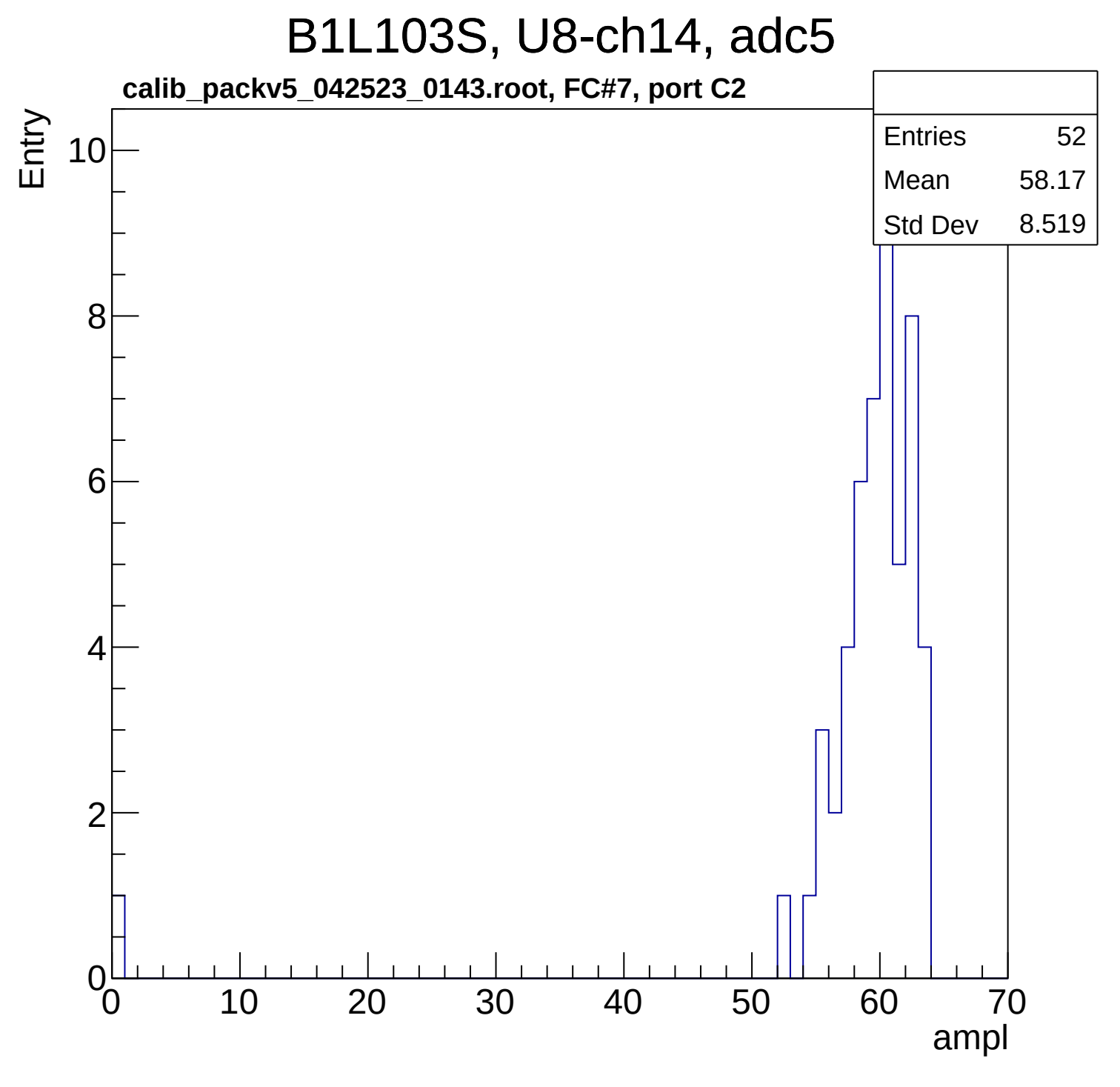

B1L103S, U8-ch14, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 44
Mean 28.7
Std Dev 5.379
Gaus mean : 30.0284
Gaus Width: 3.0449
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

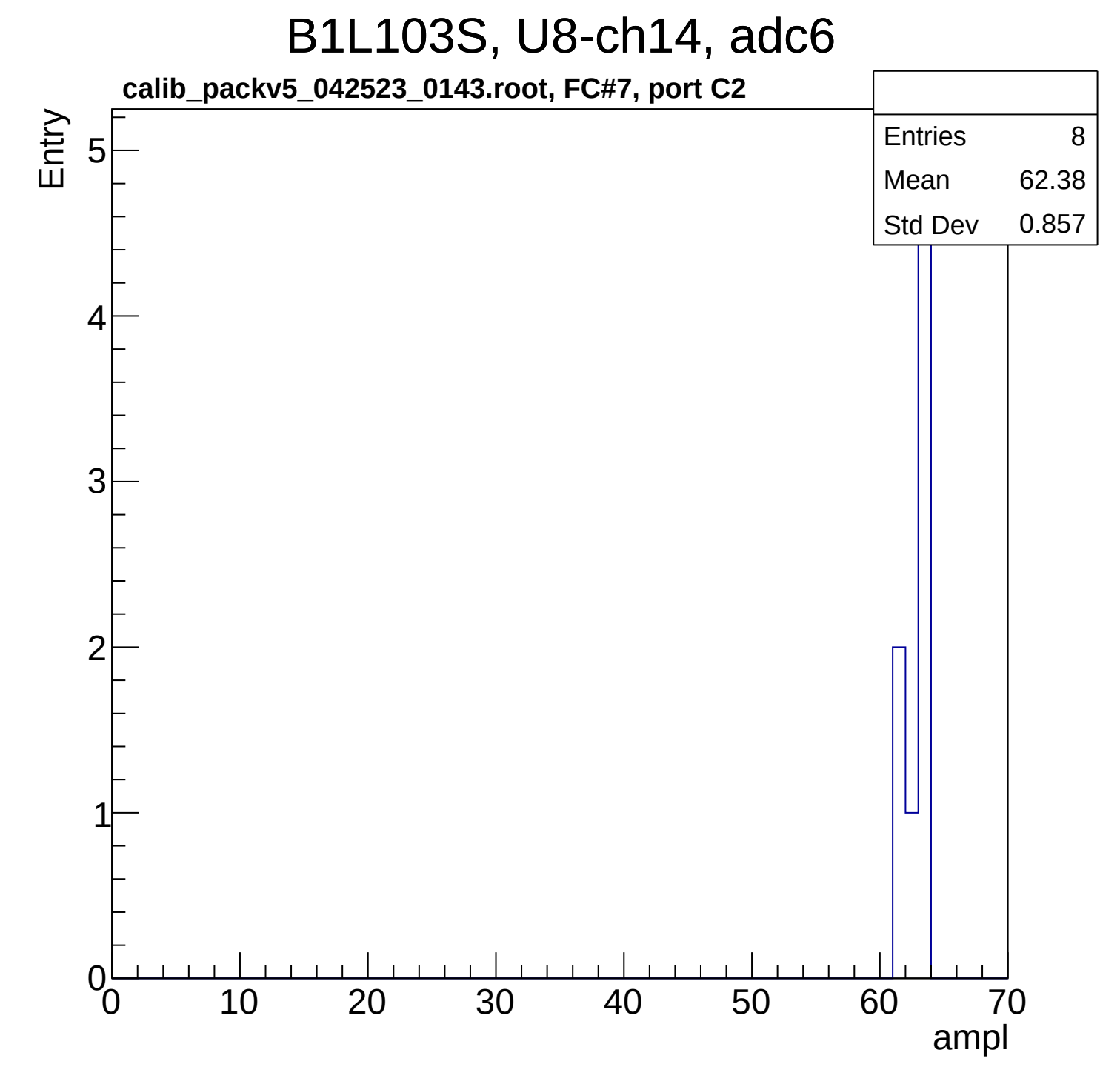

B1L103S, U8-ch14, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 85
Mean 35.85
Std Dev 3.924
Gaus mean : 35.8812
Gaus Width: 4.8150
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

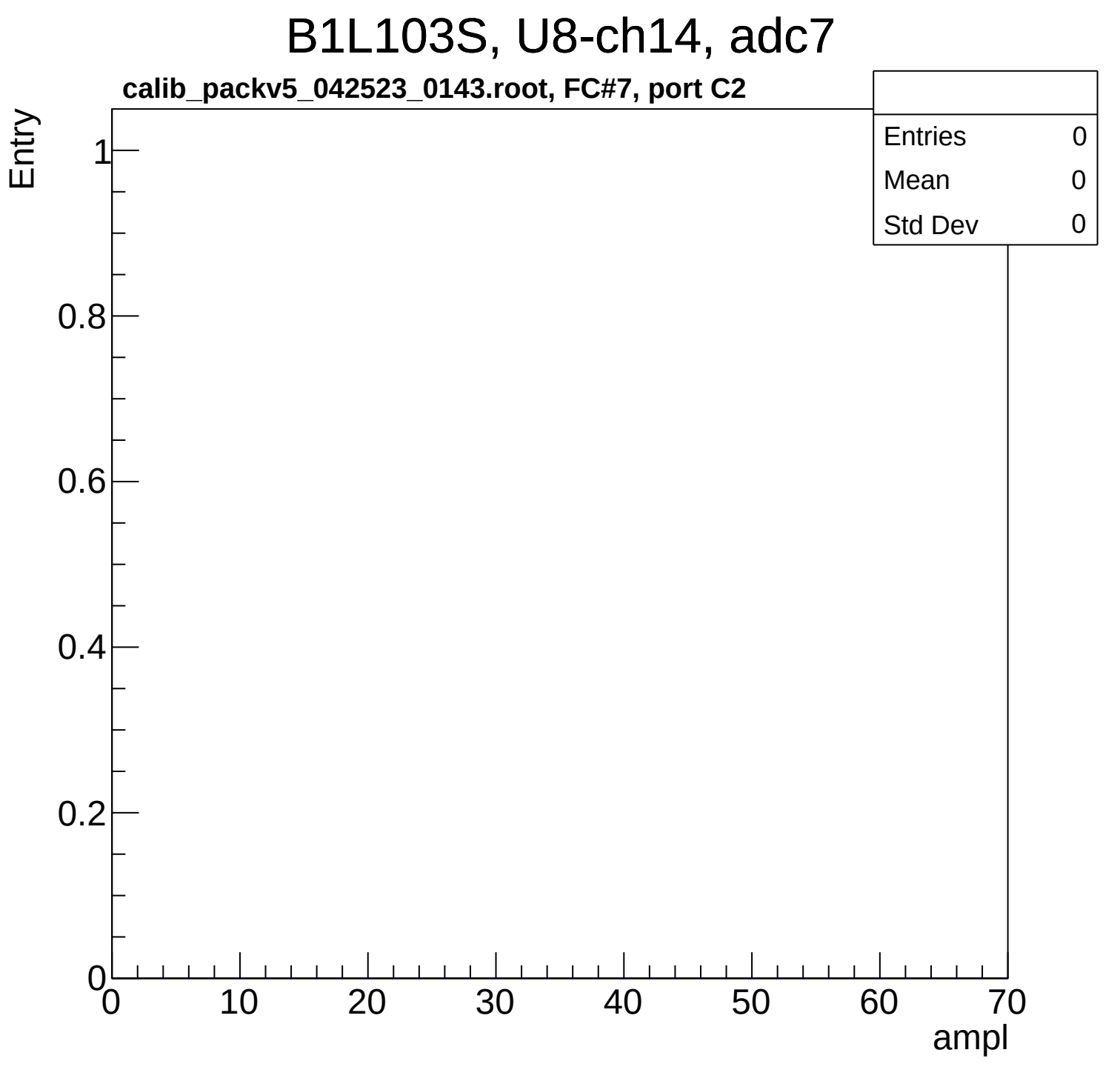

B1L103S, U8-ch14, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 41.75
Std Dev 3.358
Gaus mean : 43.4431
Gaus Width: 3.8097
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

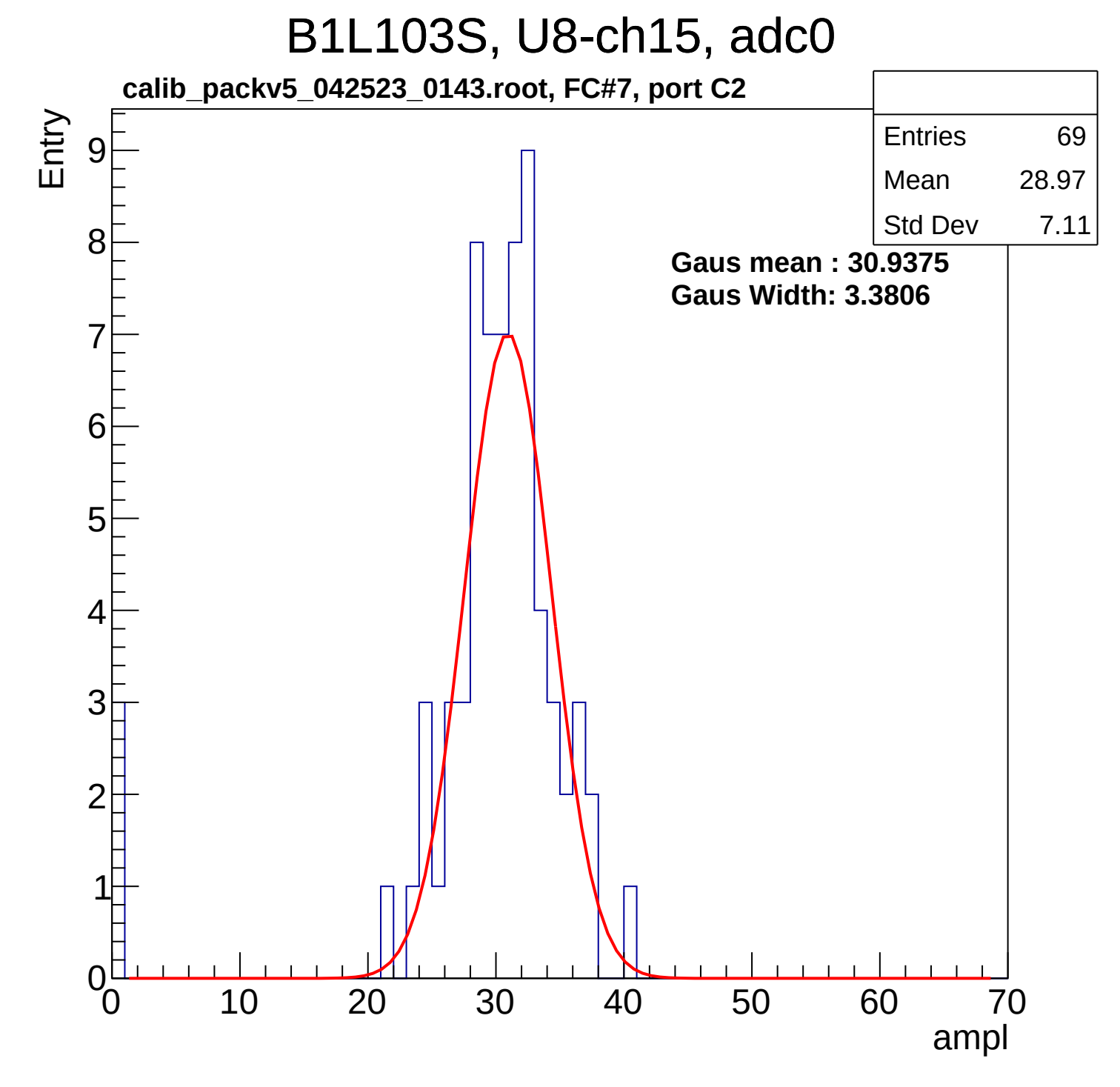

B1L103S, U8-ch14, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 49.16
Std Dev 3.445
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

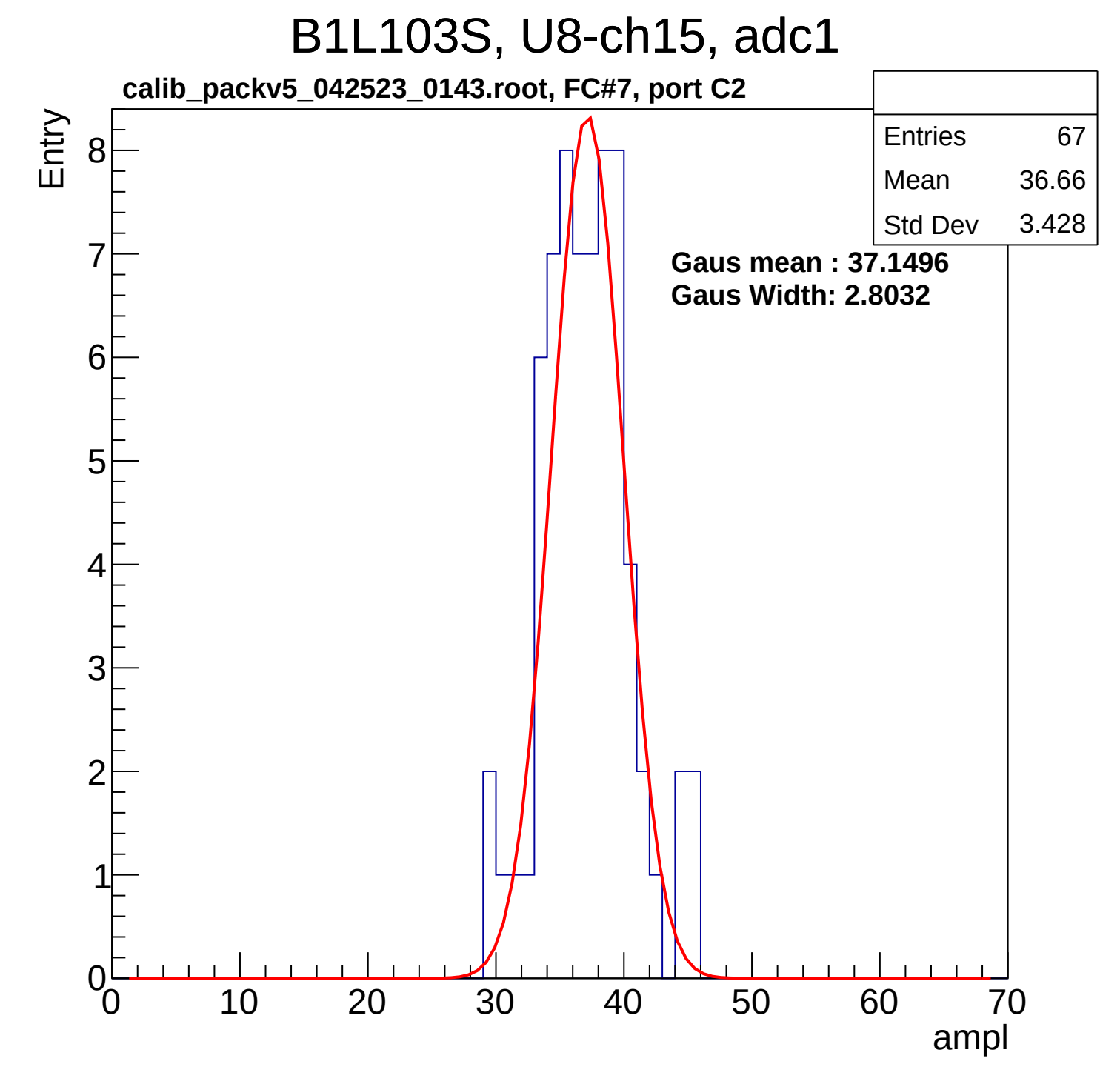

B1L103S, U8-ch14, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 55.04
Std Dev 3.644
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

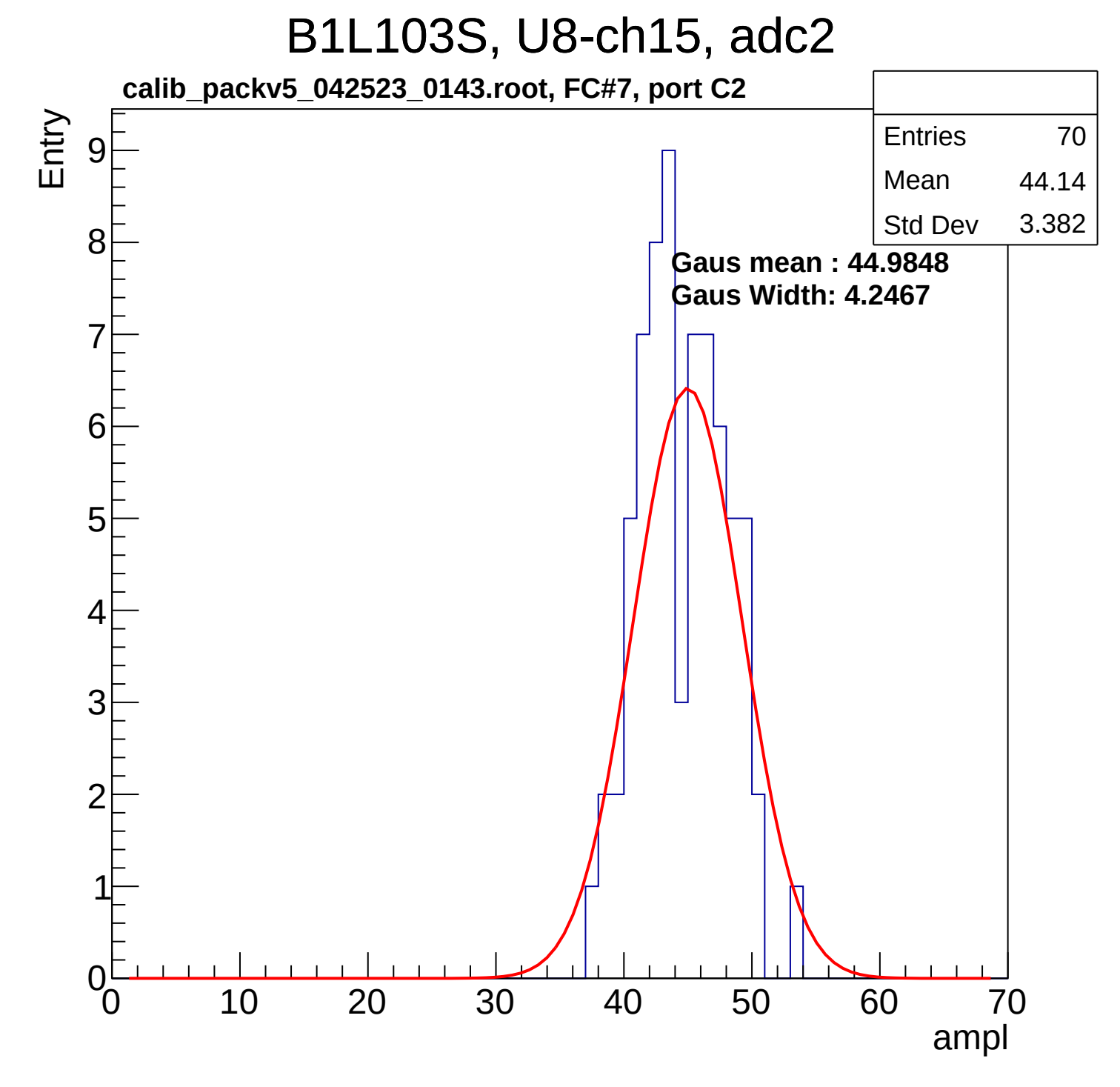

B1L103S, U8-ch14, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 58.17
Std Dev 8.519
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

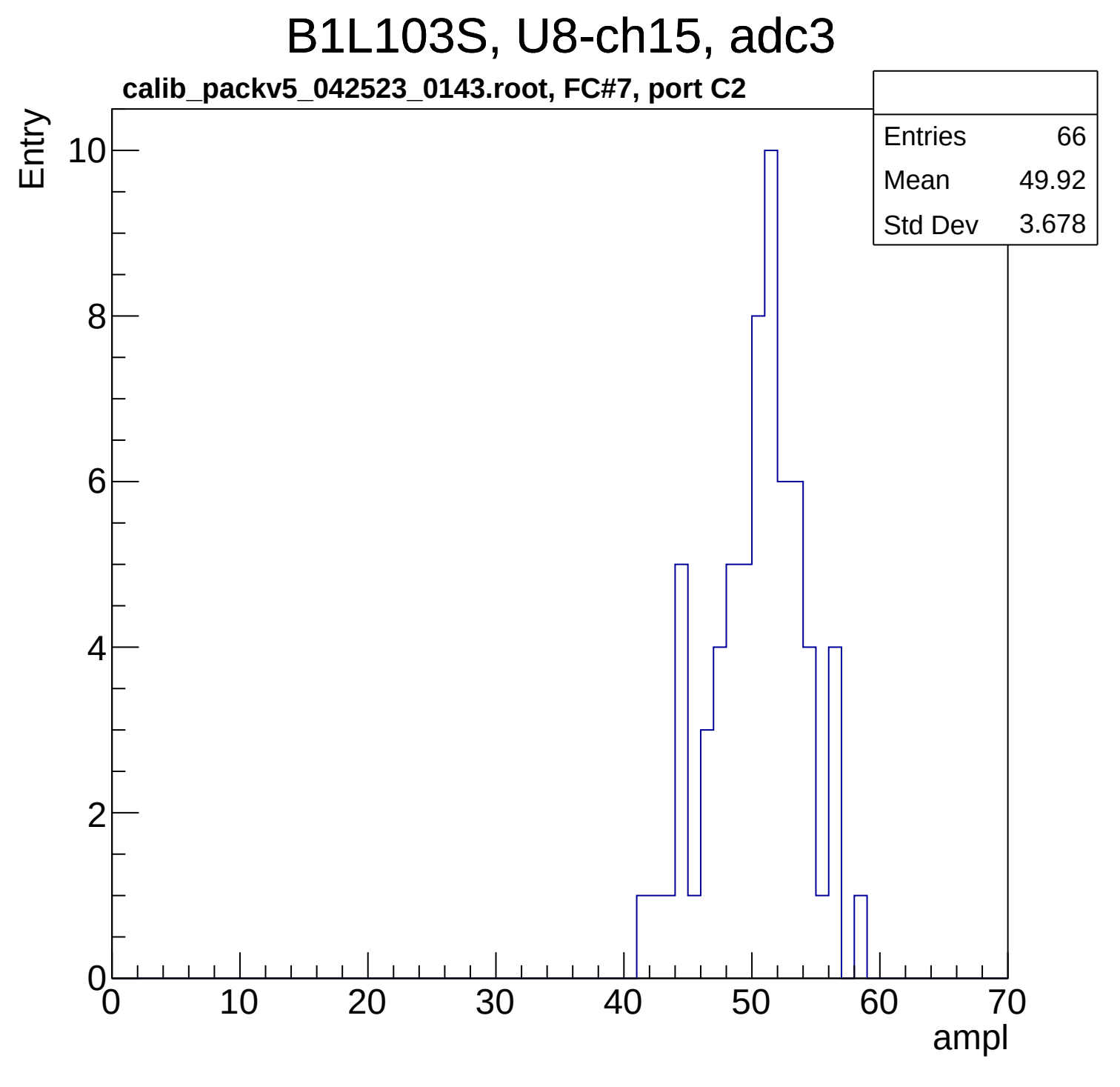

B1L103S, U8-ch14, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 8
Mean 62.38
Std Dev 0.857
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

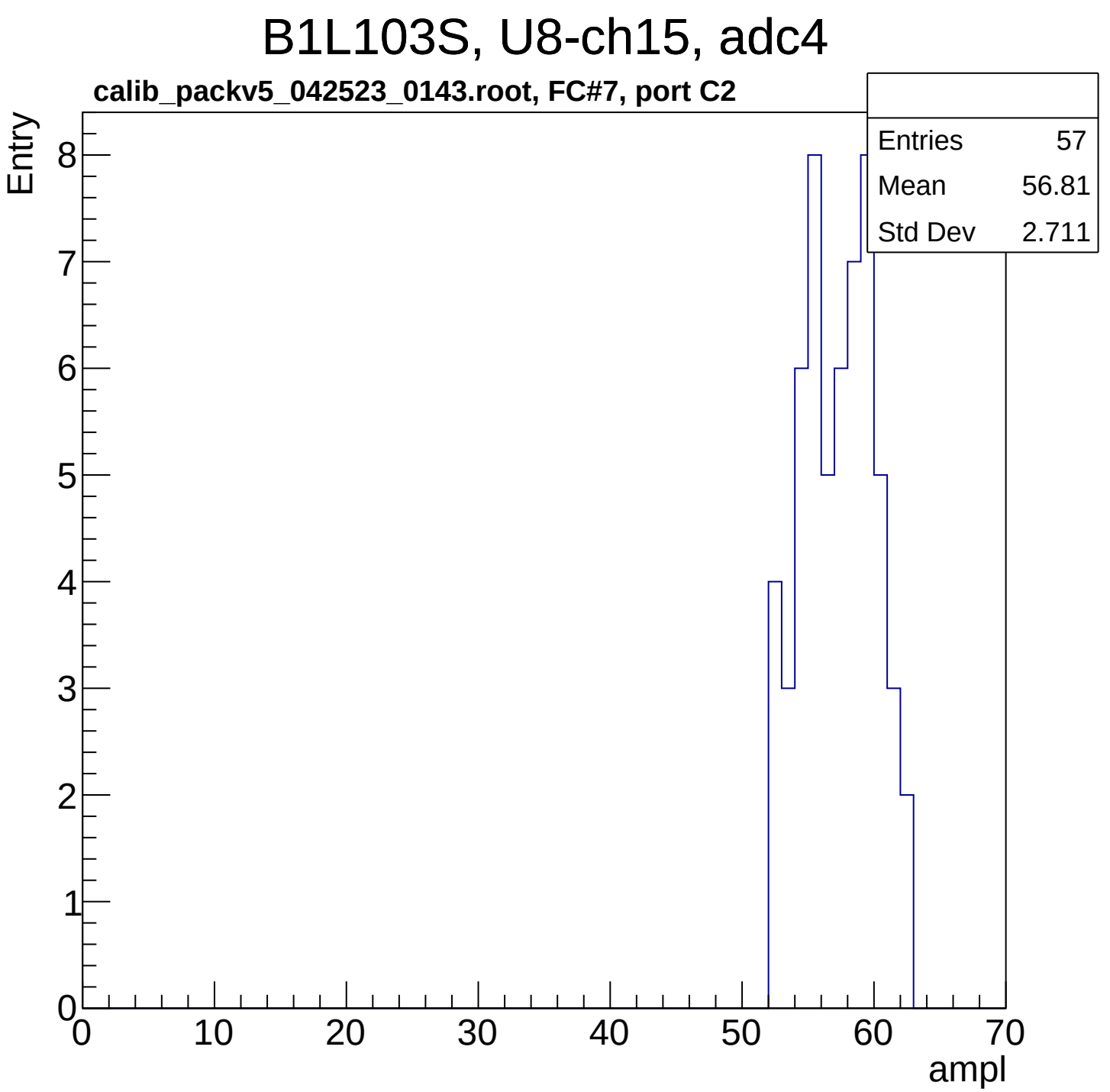

B1L103S, U8-ch14, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

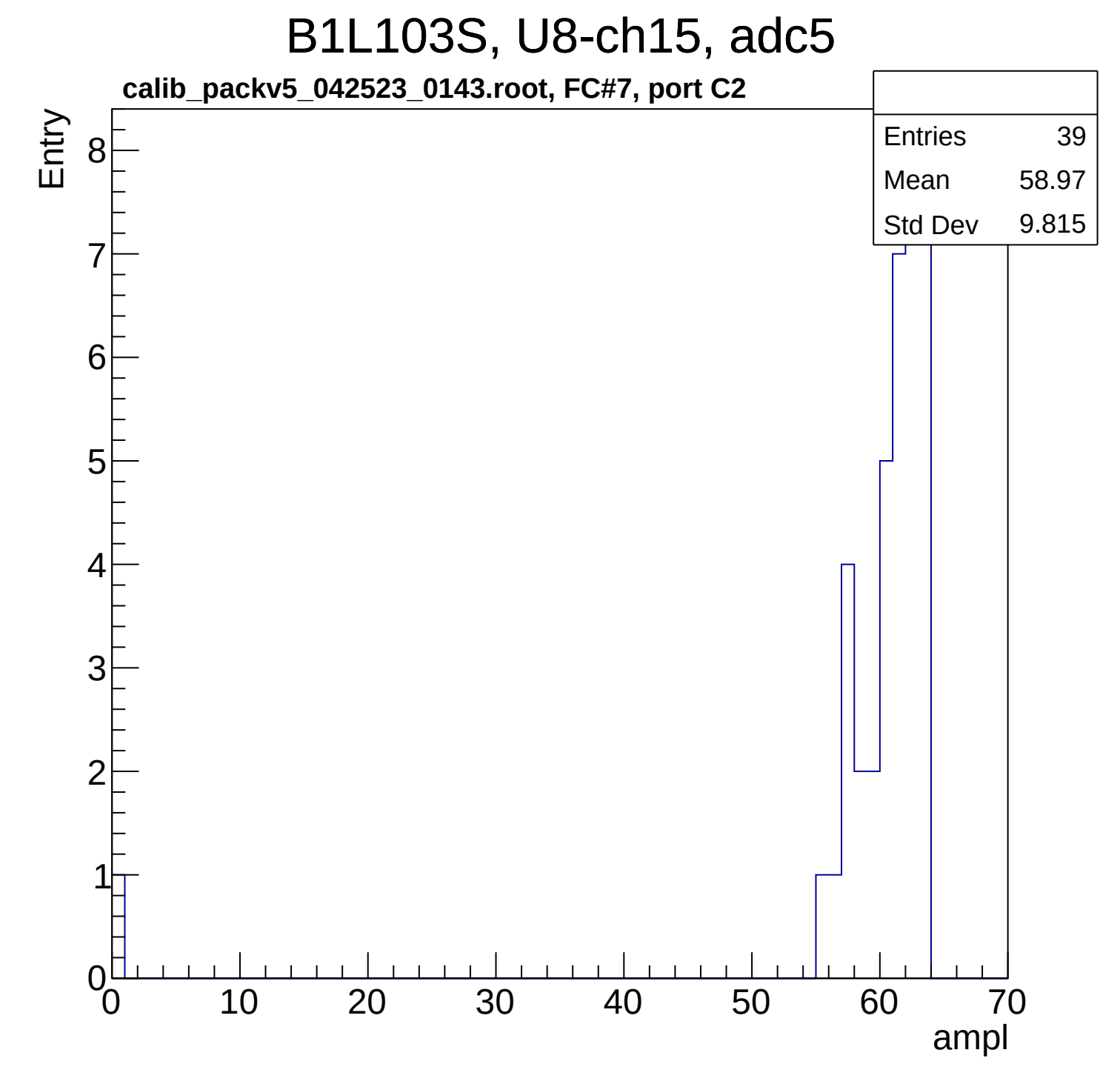

B1L103S, U8-ch15, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 28.97
Std Dev 7.11
Gaus mean : 30.9375
Gaus Width: 3.3806
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

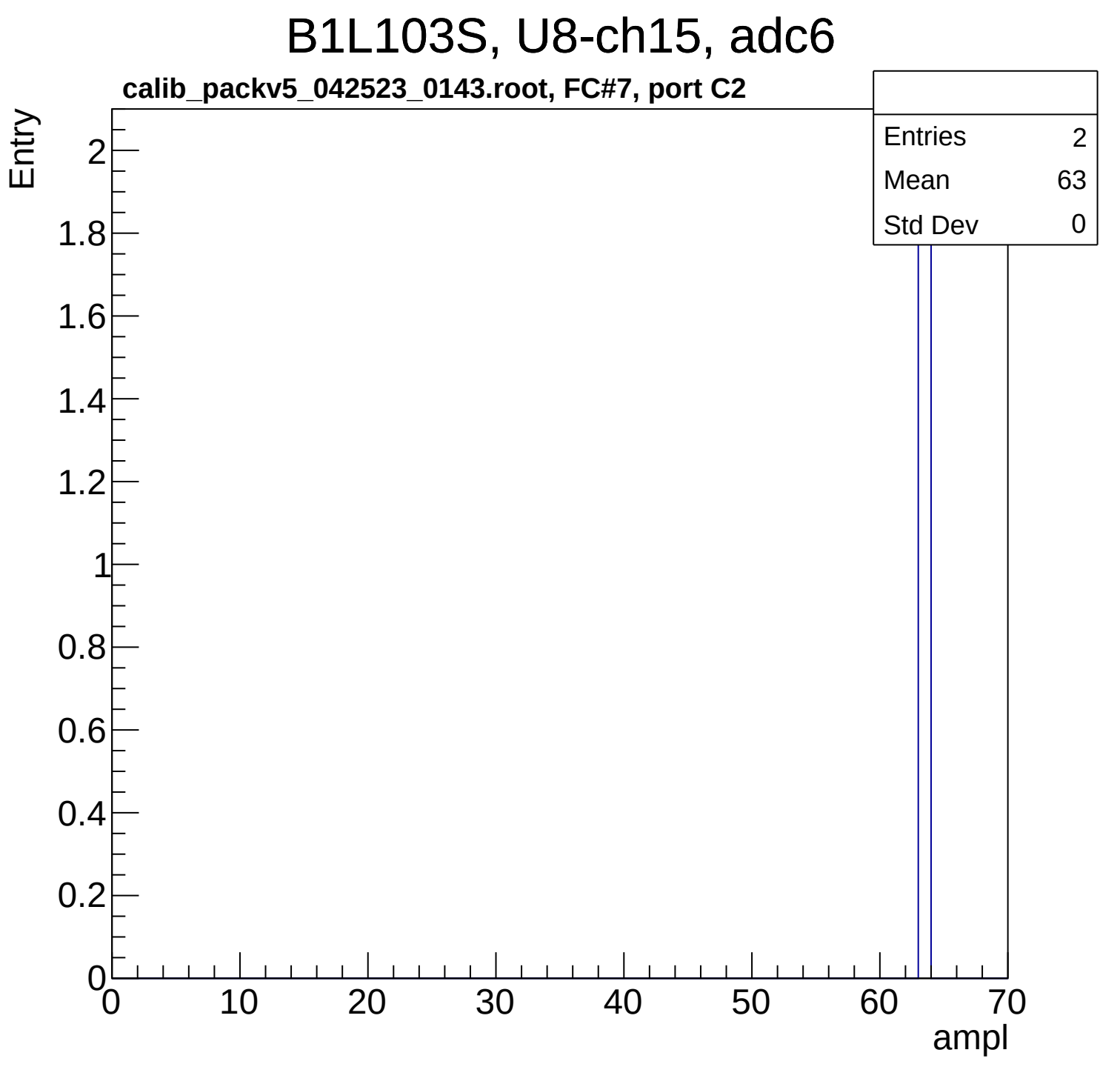

B1L103S, U8-ch15, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 36.66
Std Dev 3.428
Gaus mean : 37.1496
Gaus Width: 2.8032
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

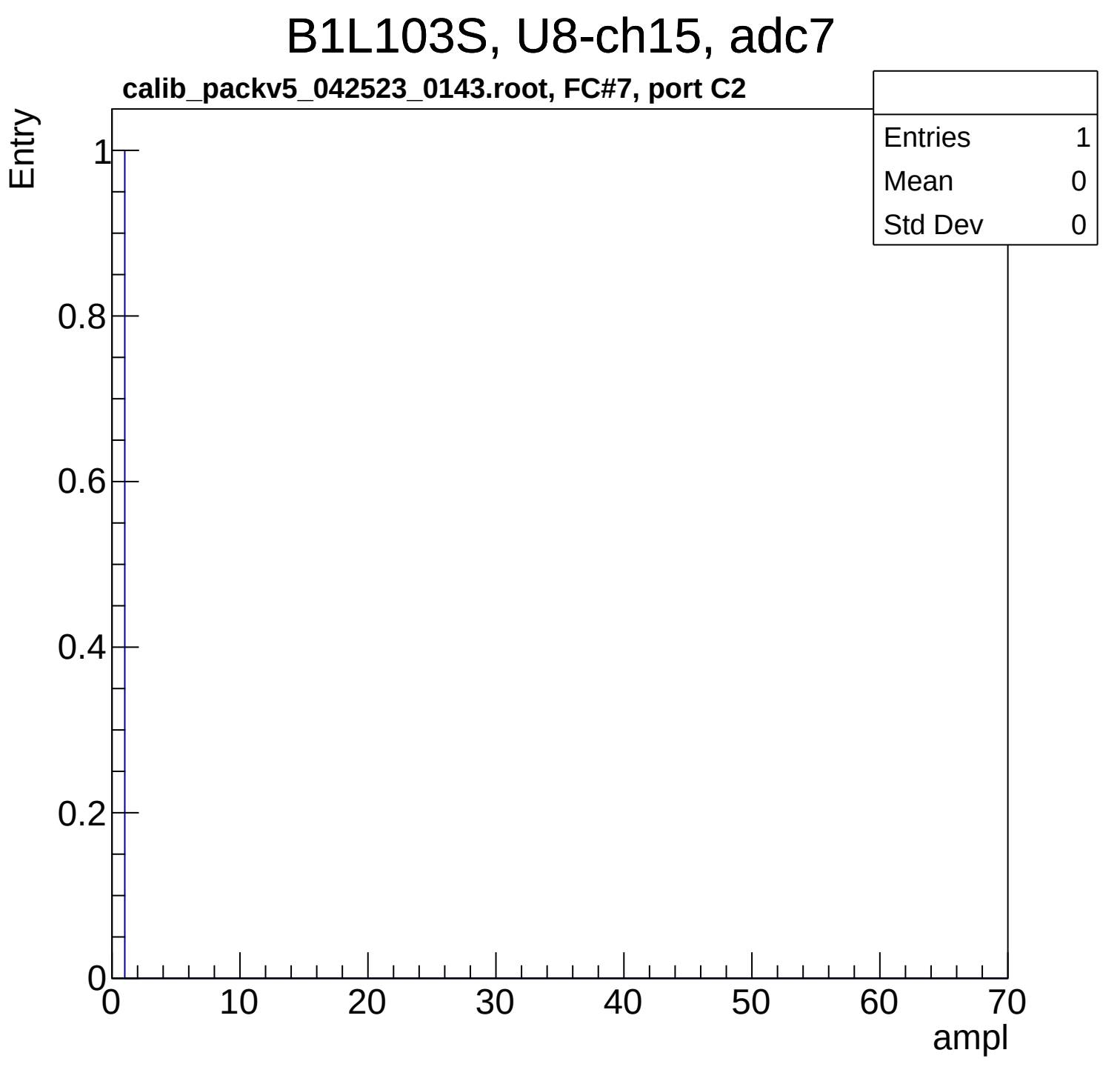

B1L103S, U8-ch15, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 44.14
Std Dev 3.382
Gaus mean : 44.9848
Gaus Width: 4.2467
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

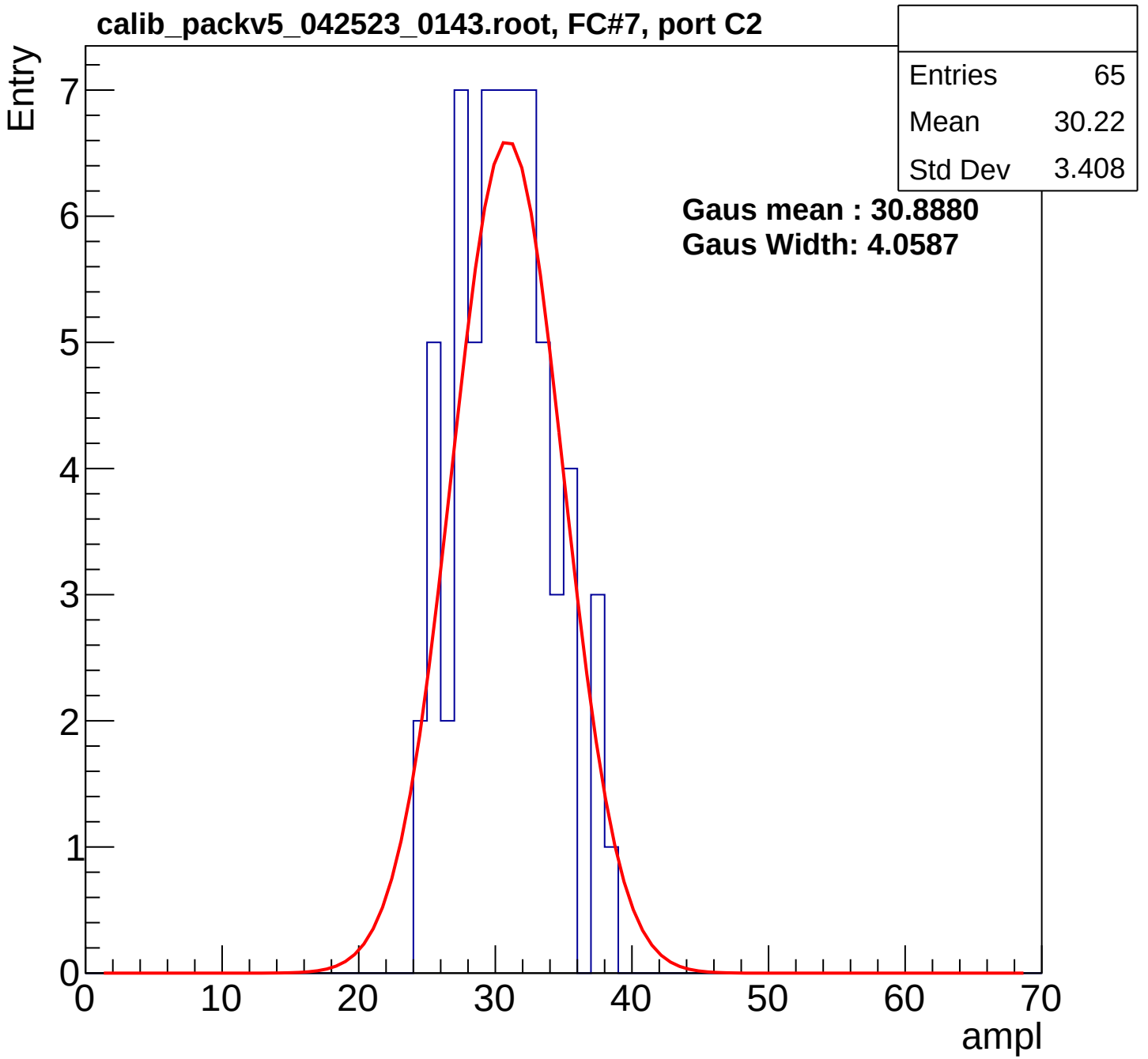

B1L103S, U8-ch15, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 49.92
Std Dev 3.678
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

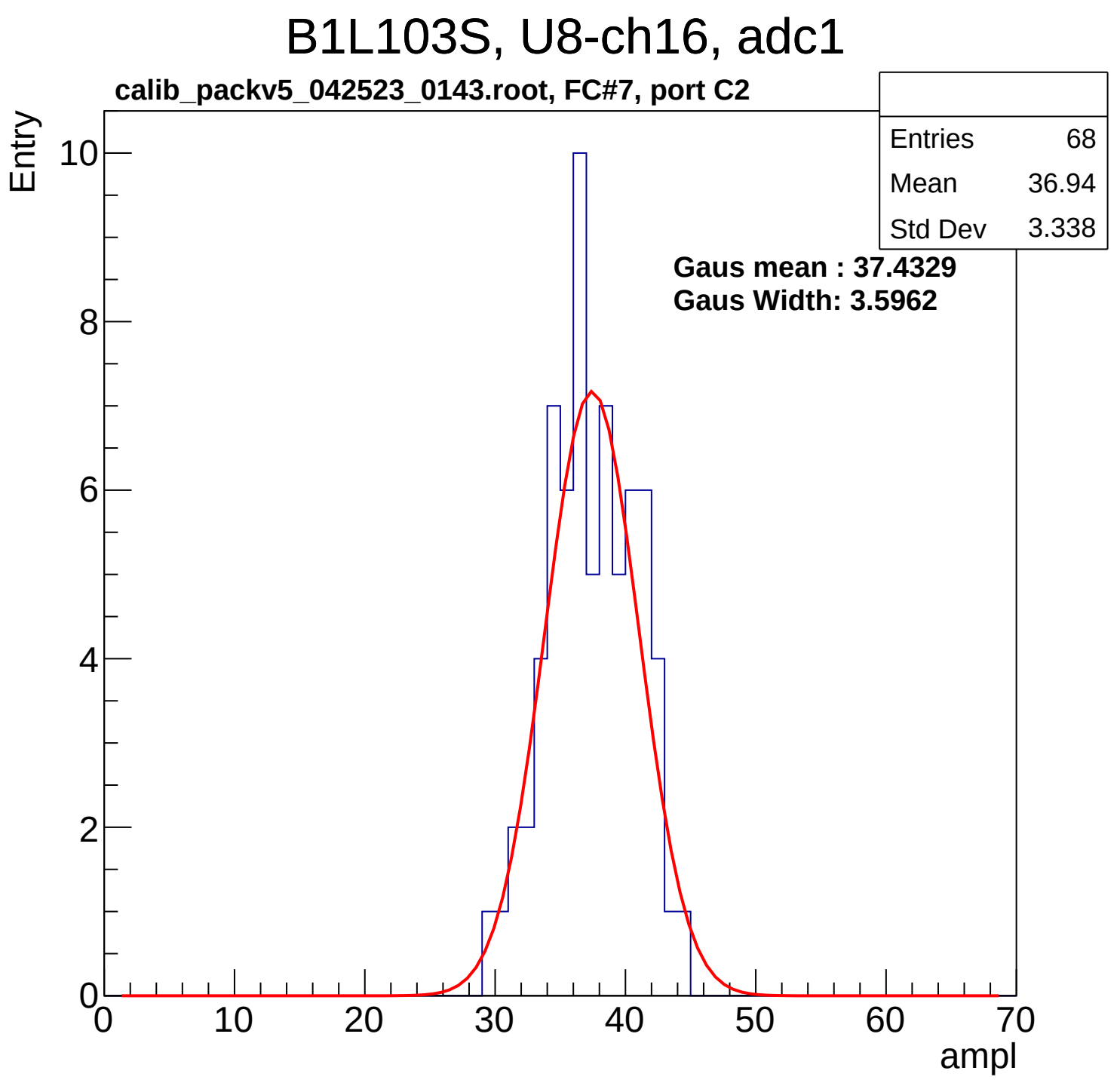

B1L103S, U8-ch15, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 56.81
Std Dev 2.711
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

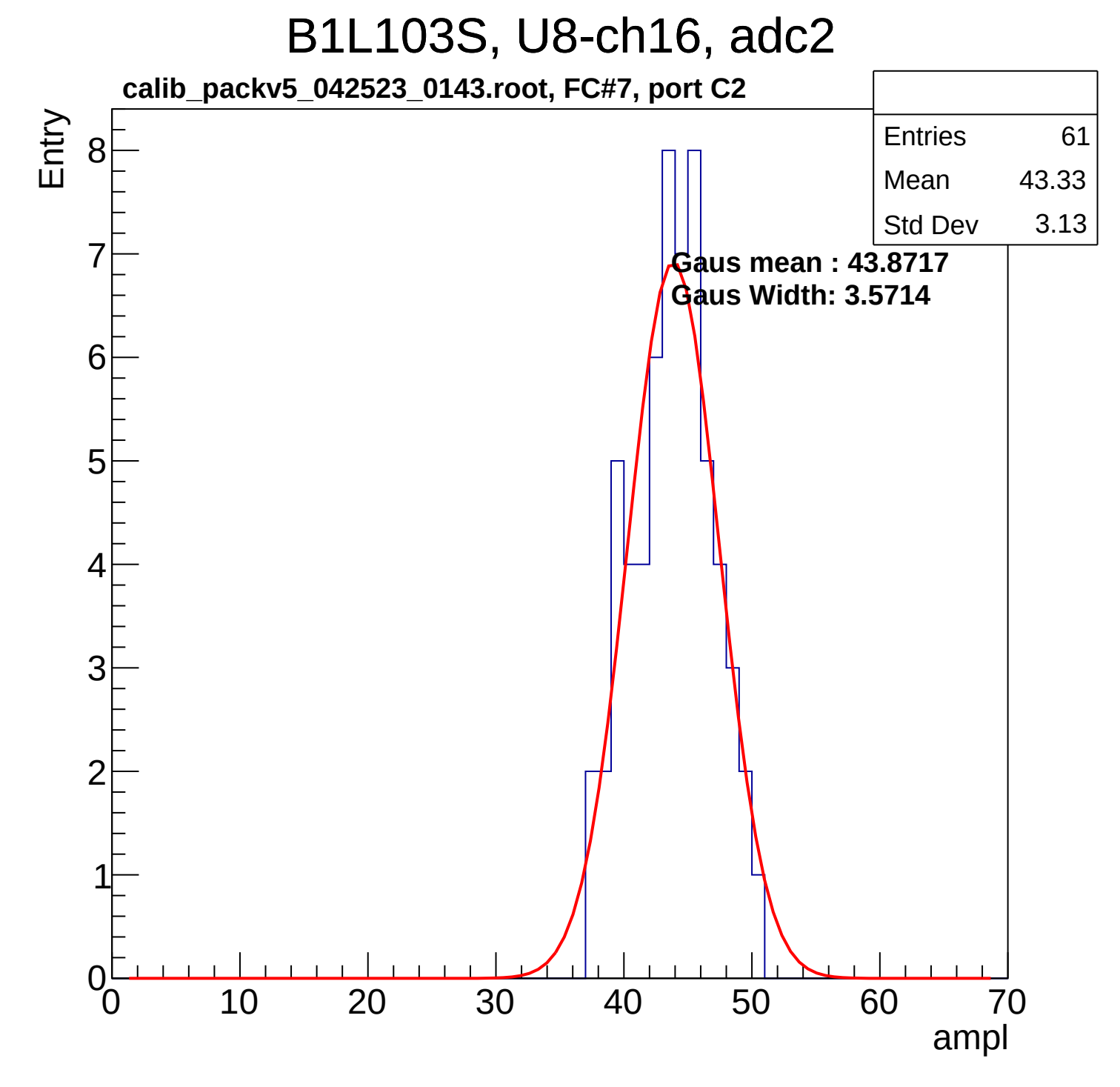

B1L103S, U8-ch15, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 39
Mean 58.97
Std Dev 9.815
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

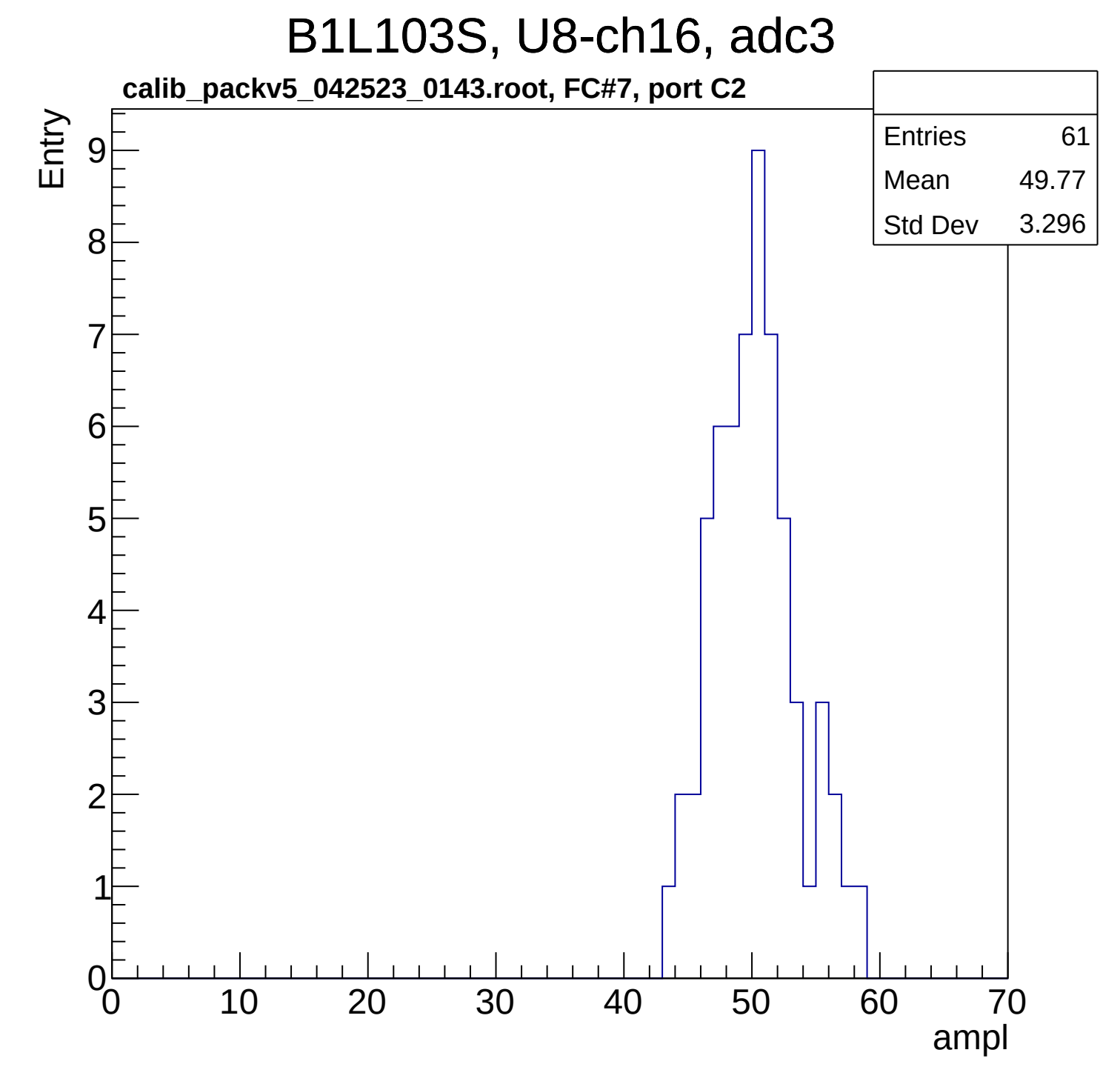

B1L103S, U8-ch15, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

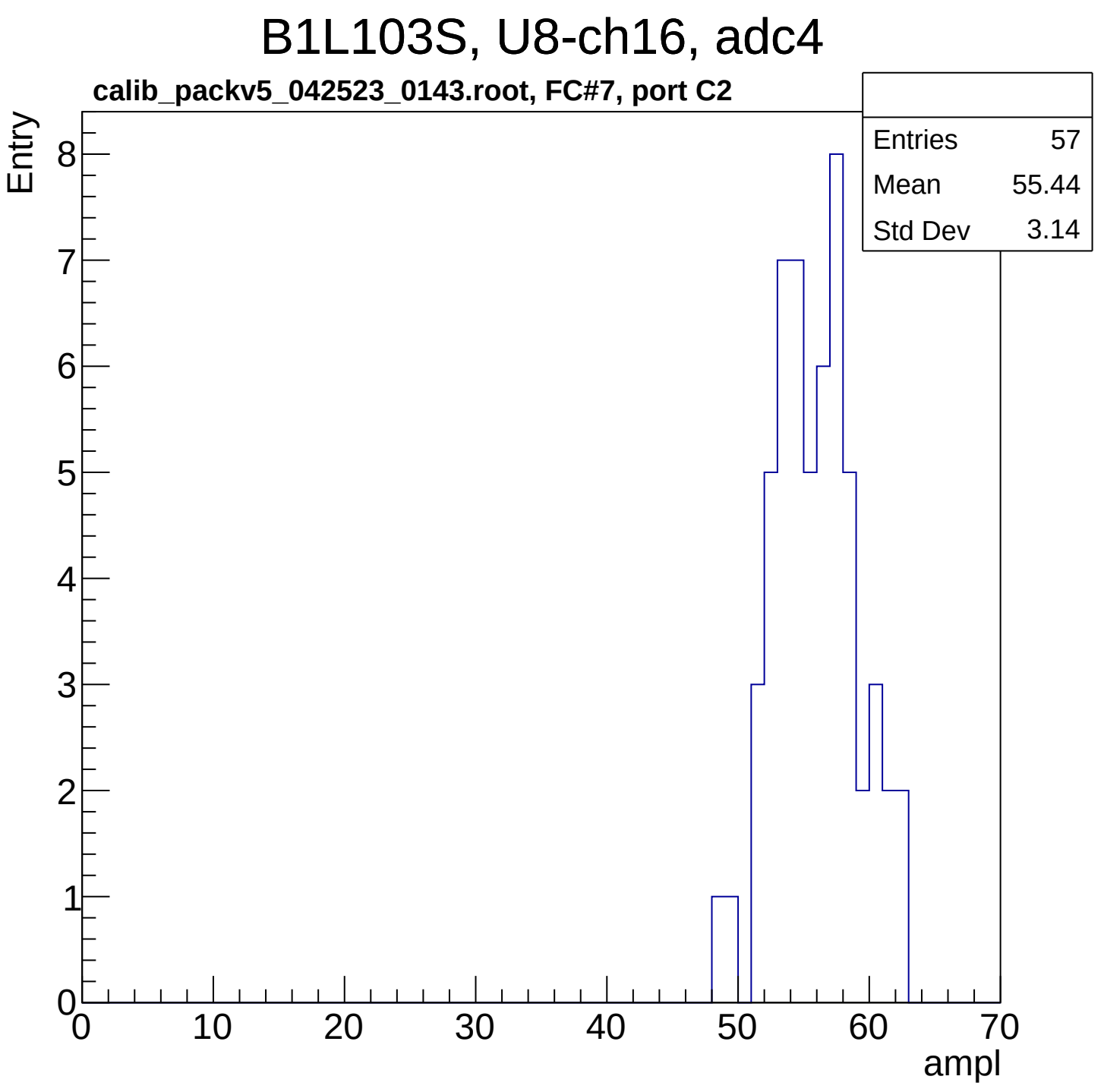

B1L103S, U8-ch15, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

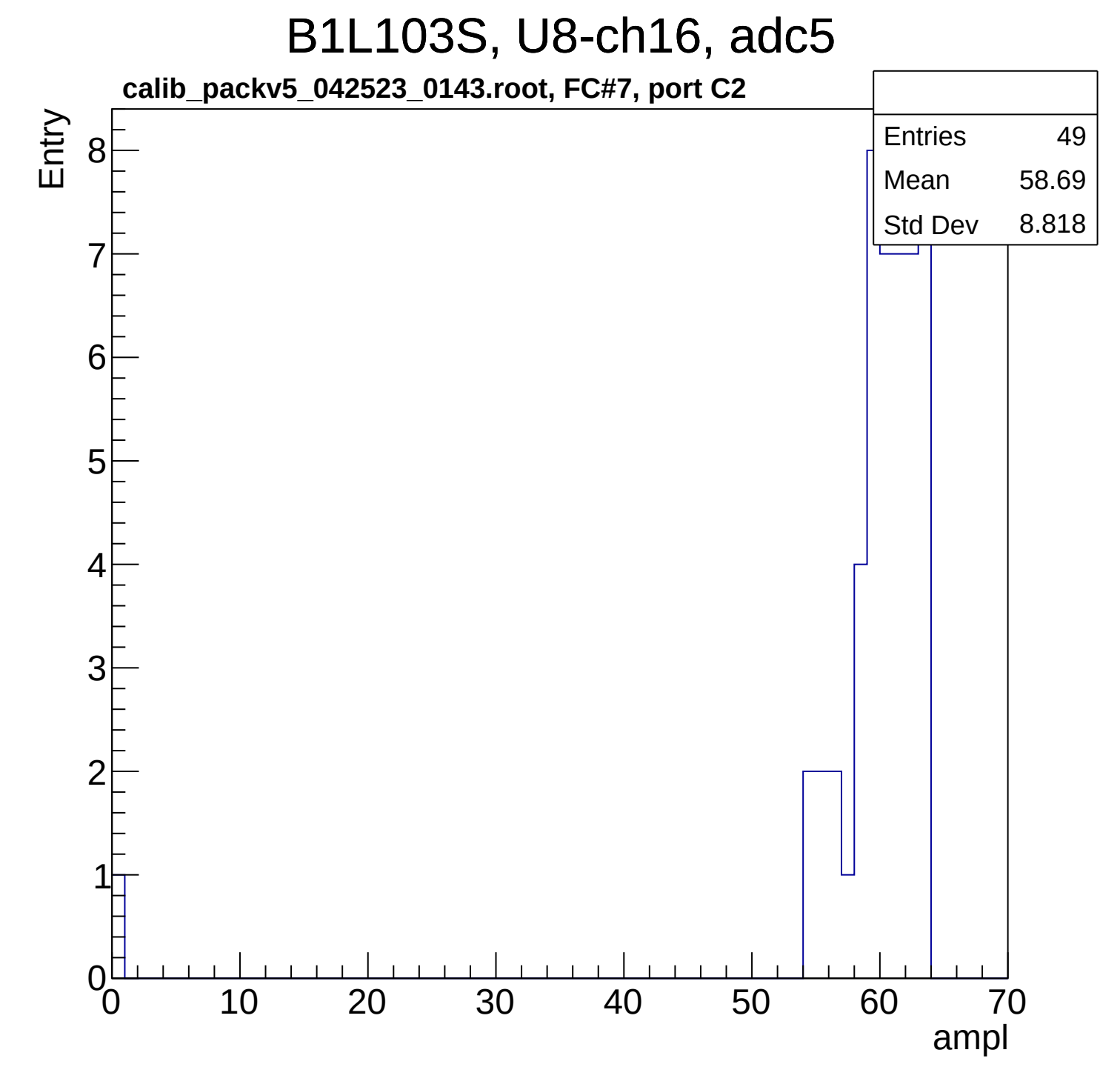

B1L103S, U8-ch16, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 30.22
Std Dev 3.408
Gaus mean : 30.8880
Gaus Width: 4.0587
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

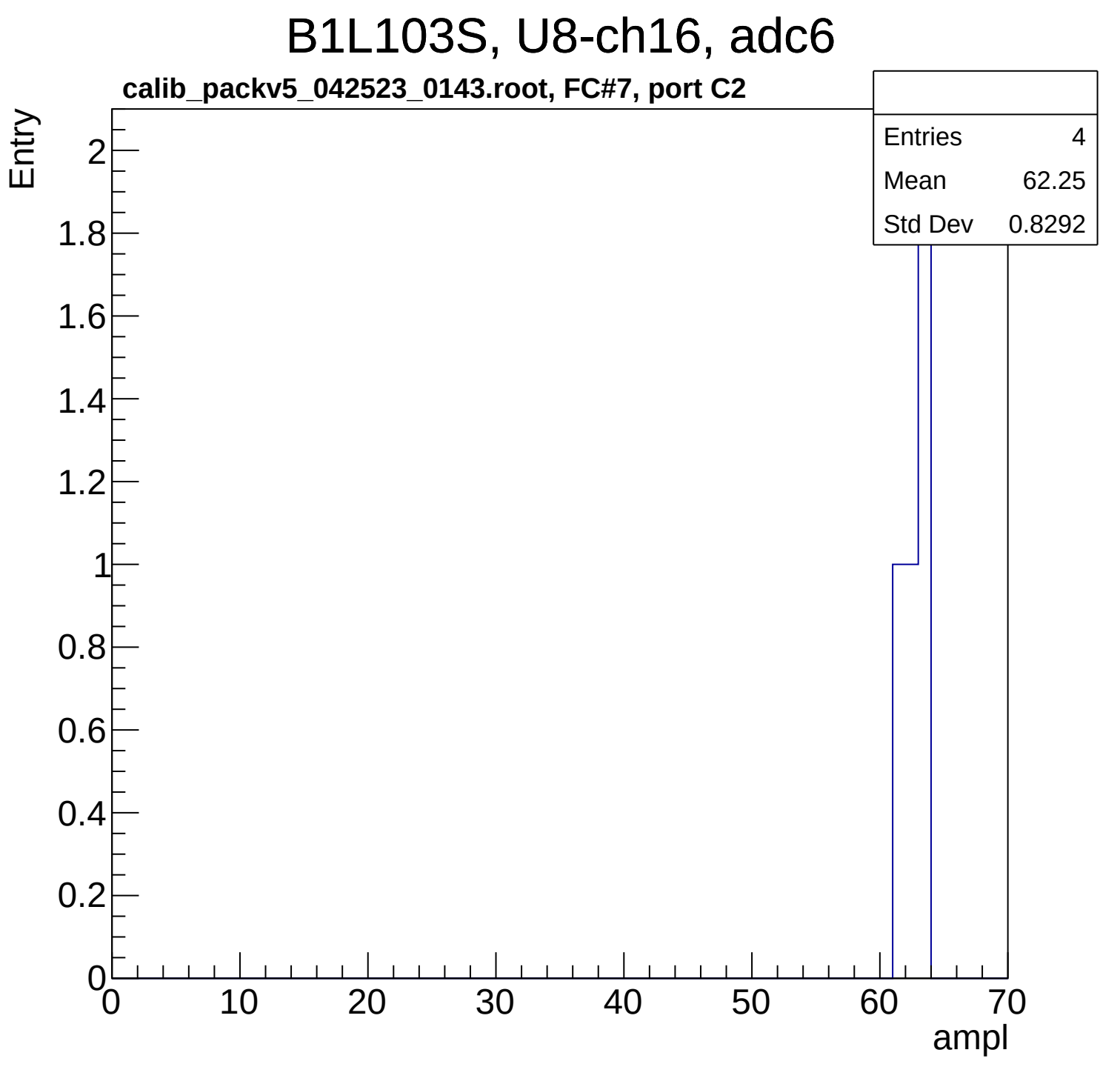

B1L103S, U8-ch16, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 36.94
Std Dev 3.338
Gaus mean : 37.4329
Gaus Width: 3.5962
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

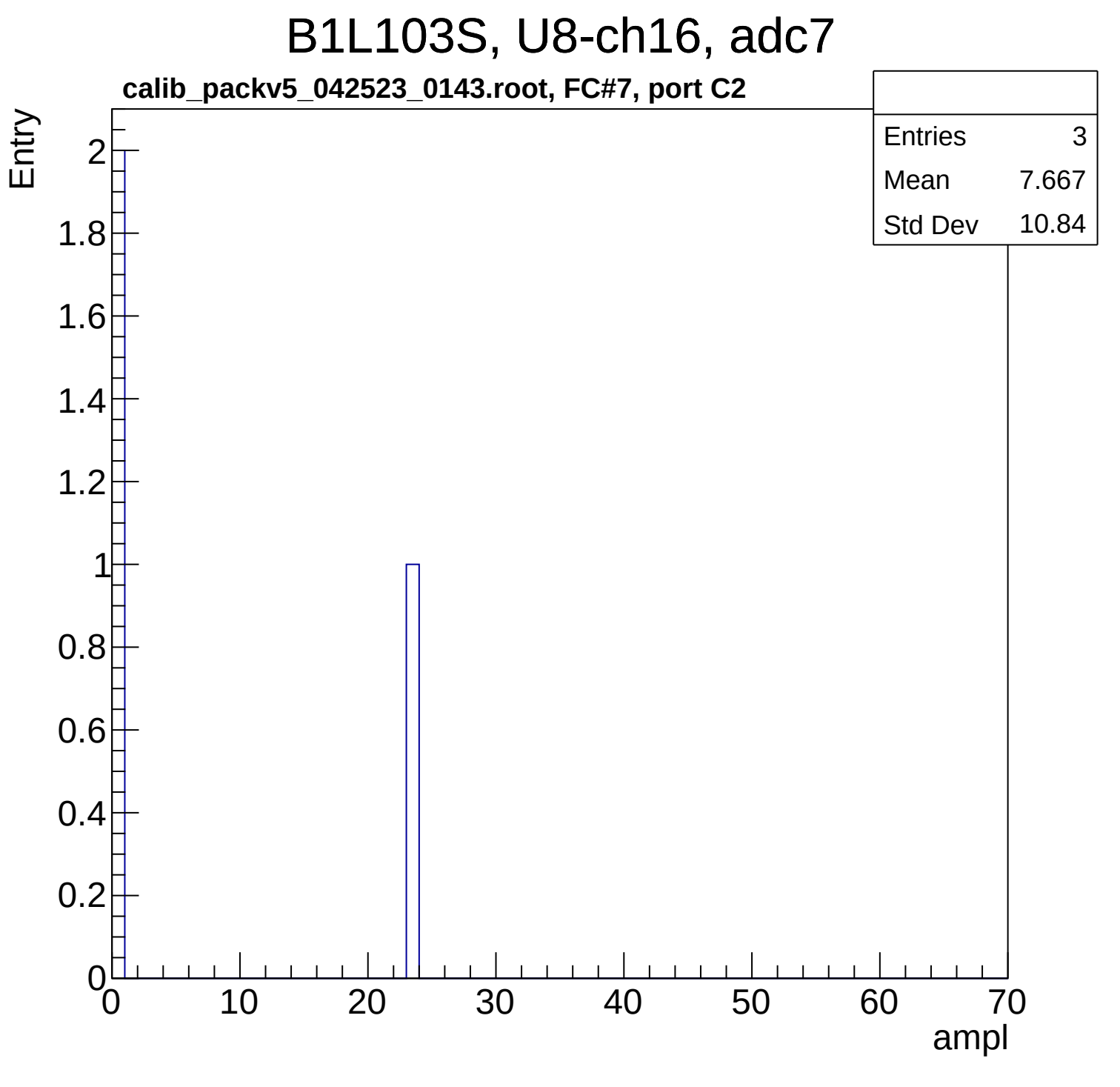

B1L103S, U8-ch16, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 43.33
Std Dev 3.13
Gaus mean : 43.8717
Gaus Width: 3.5714
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

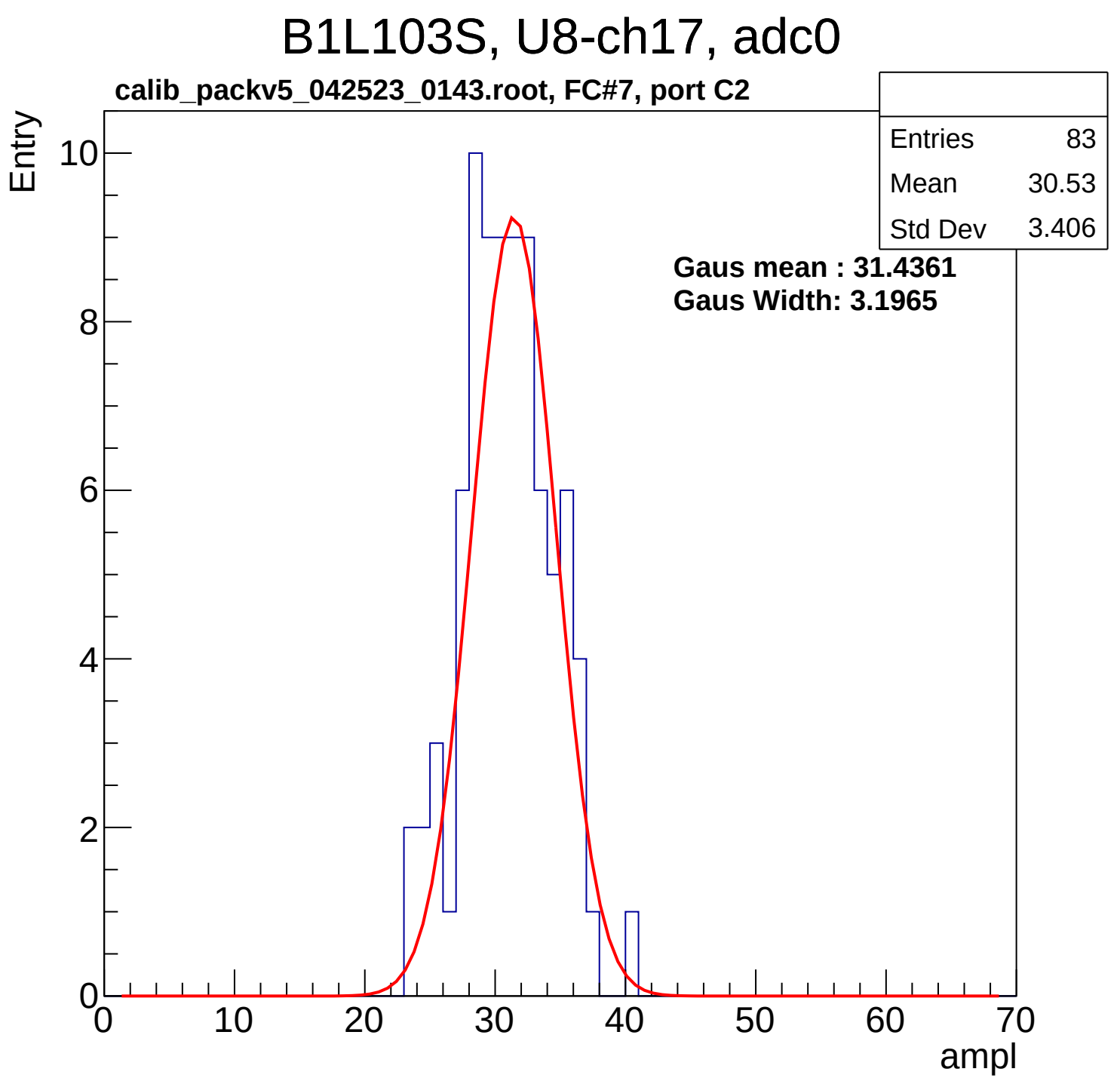

B1L103S, U8-ch16, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 49.77
Std Dev 3.296
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

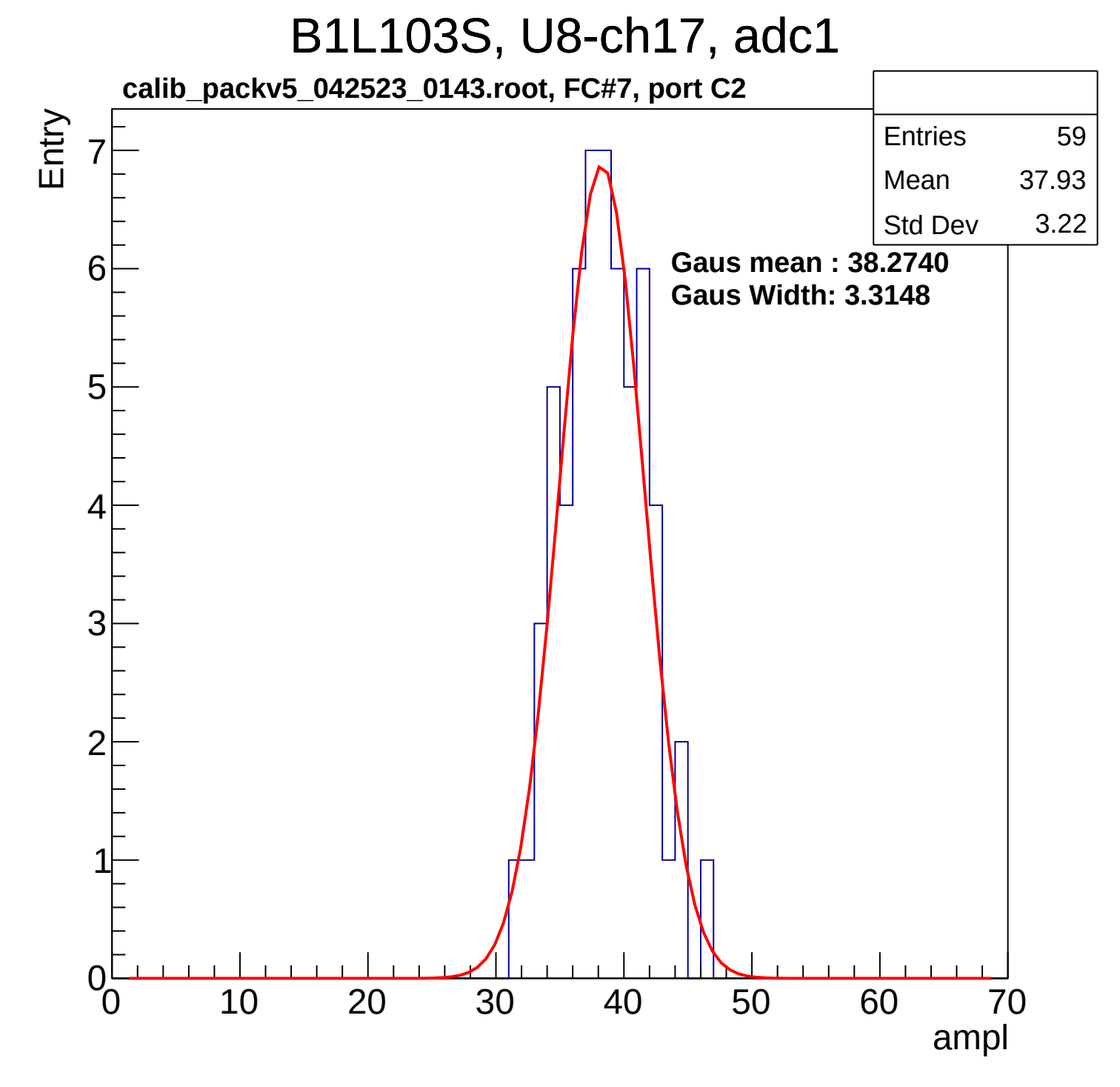

B1L103S, U8-ch16, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 55.44
Std Dev 3.14
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

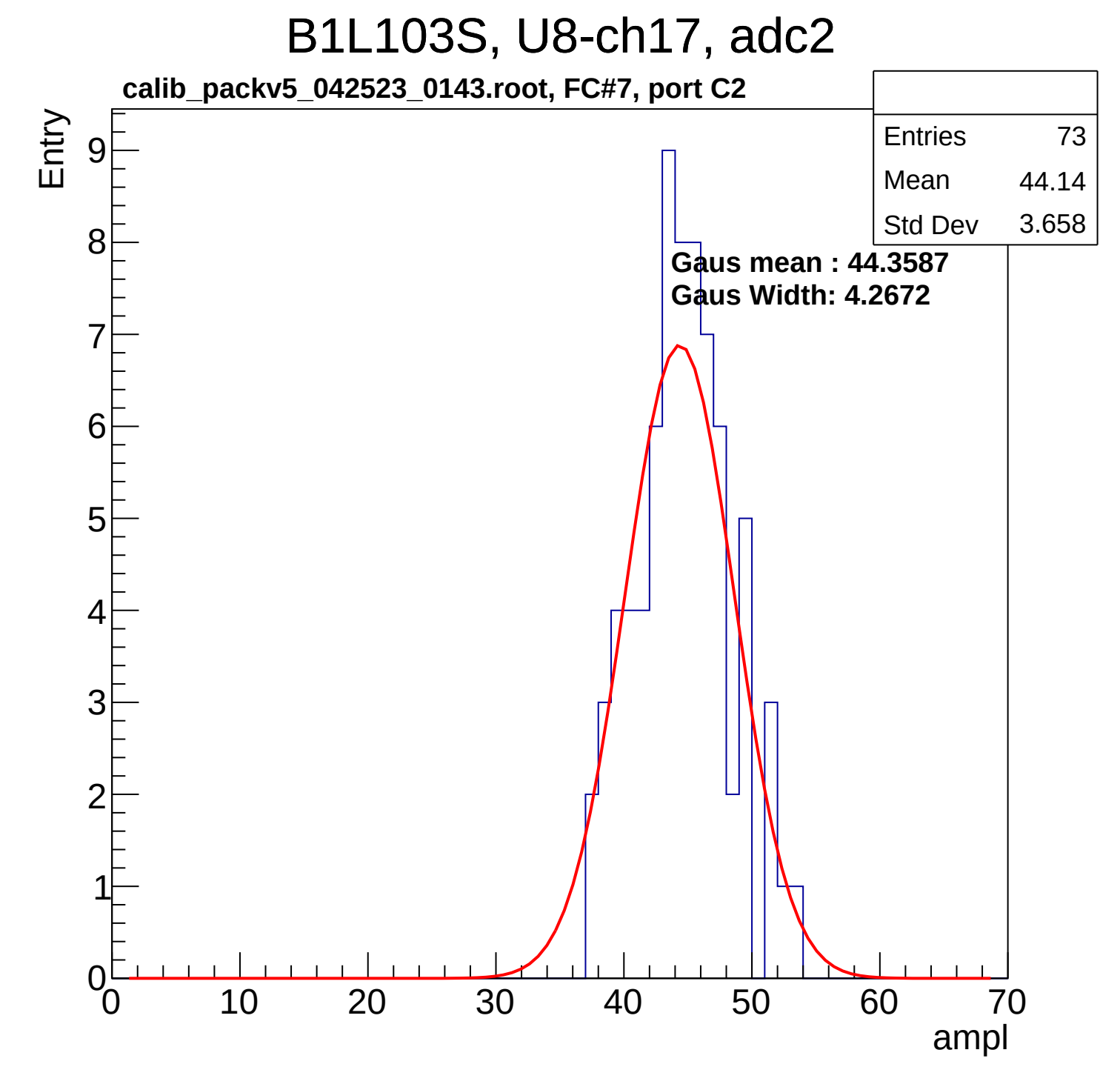

B1L103S, U8-ch16, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 58.69
Std Dev 8.818
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

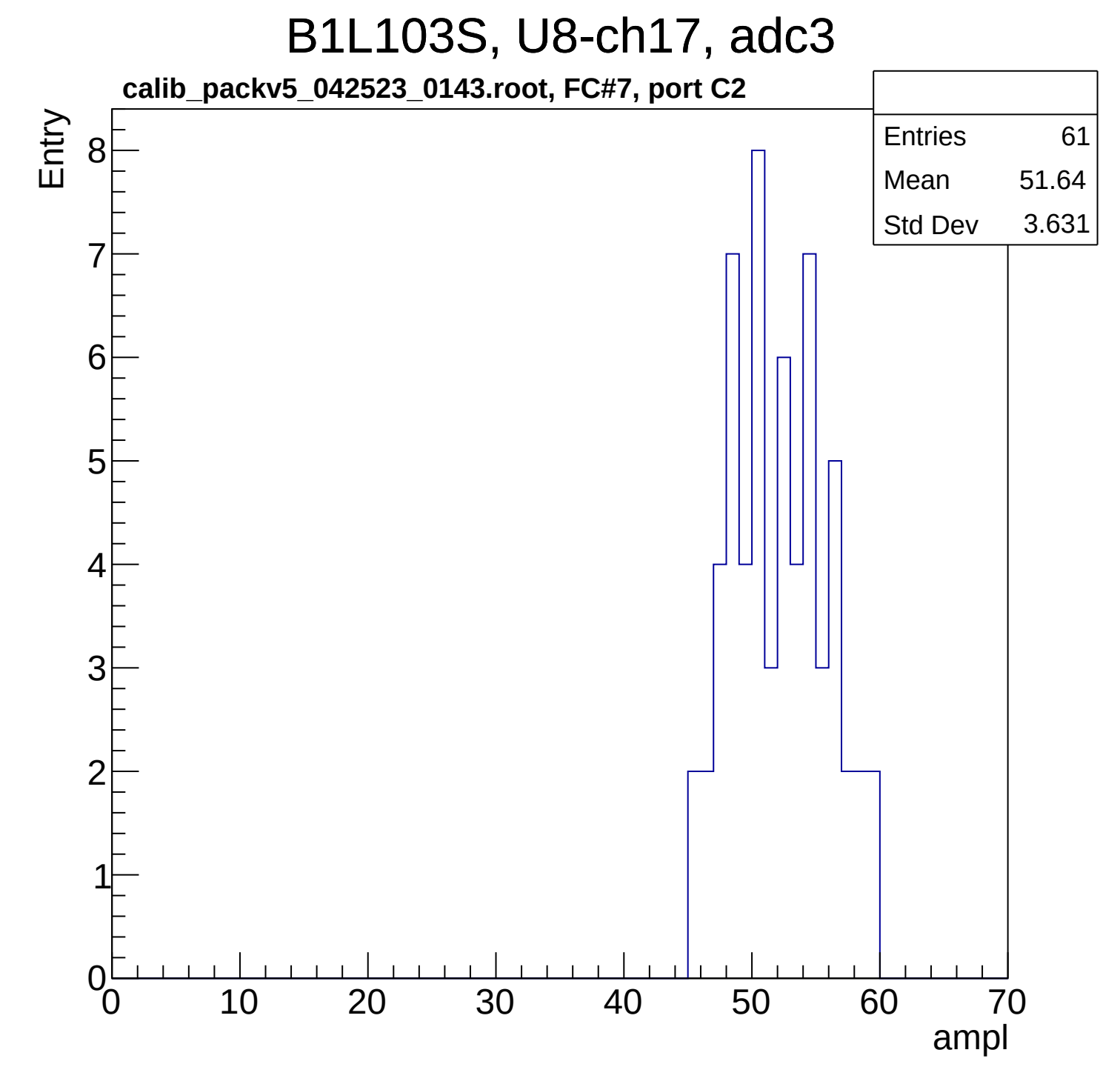

B1L103S, U8-ch16, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

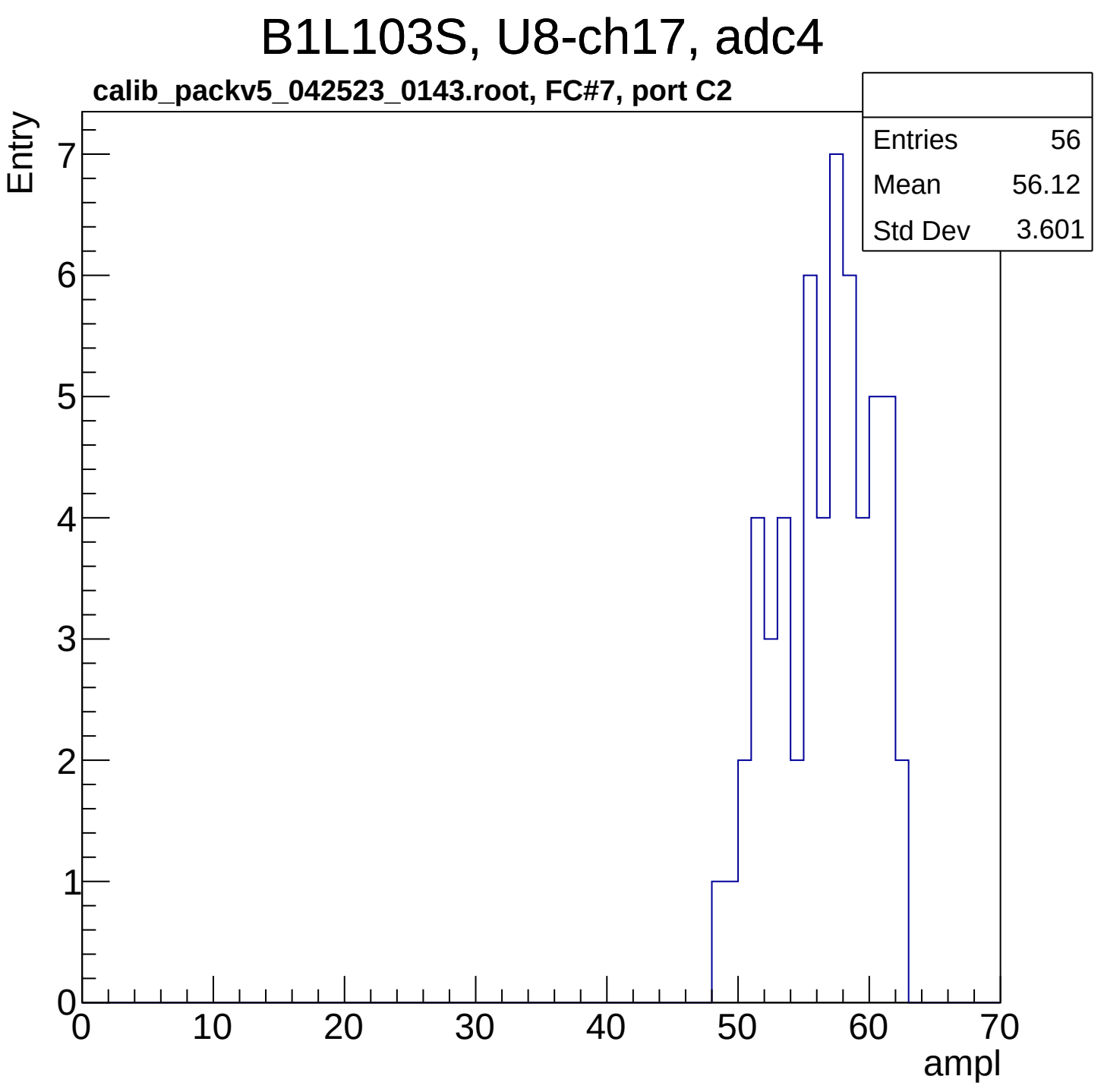

B1L103S, U8-ch16, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 7.667
Std Dev 10.84
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

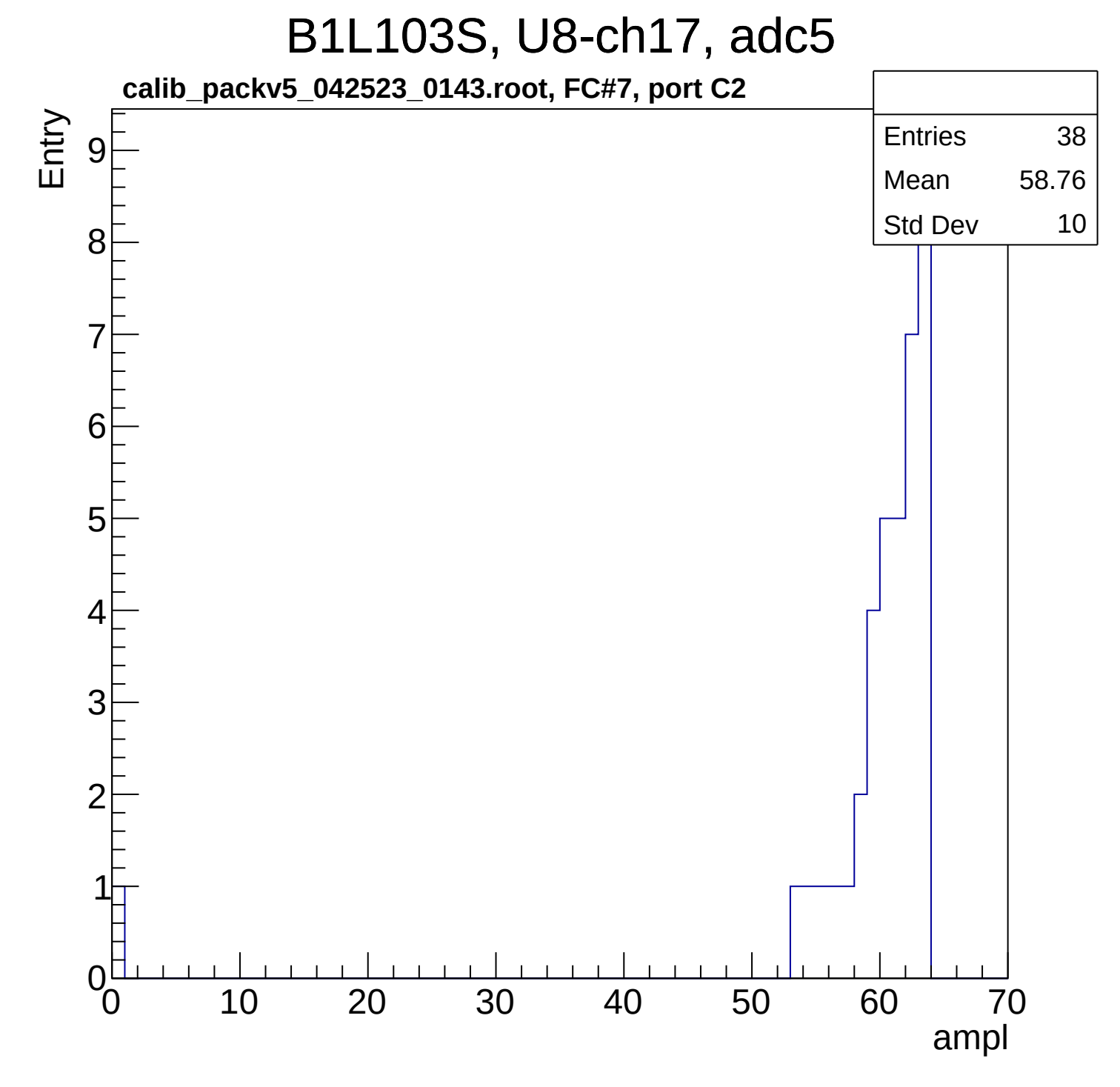

B1L103S, U8-ch17, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 83
Mean 30.53
Std Dev 3.406
Gaus mean : 31.4361
Gaus Width: 3.1965
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

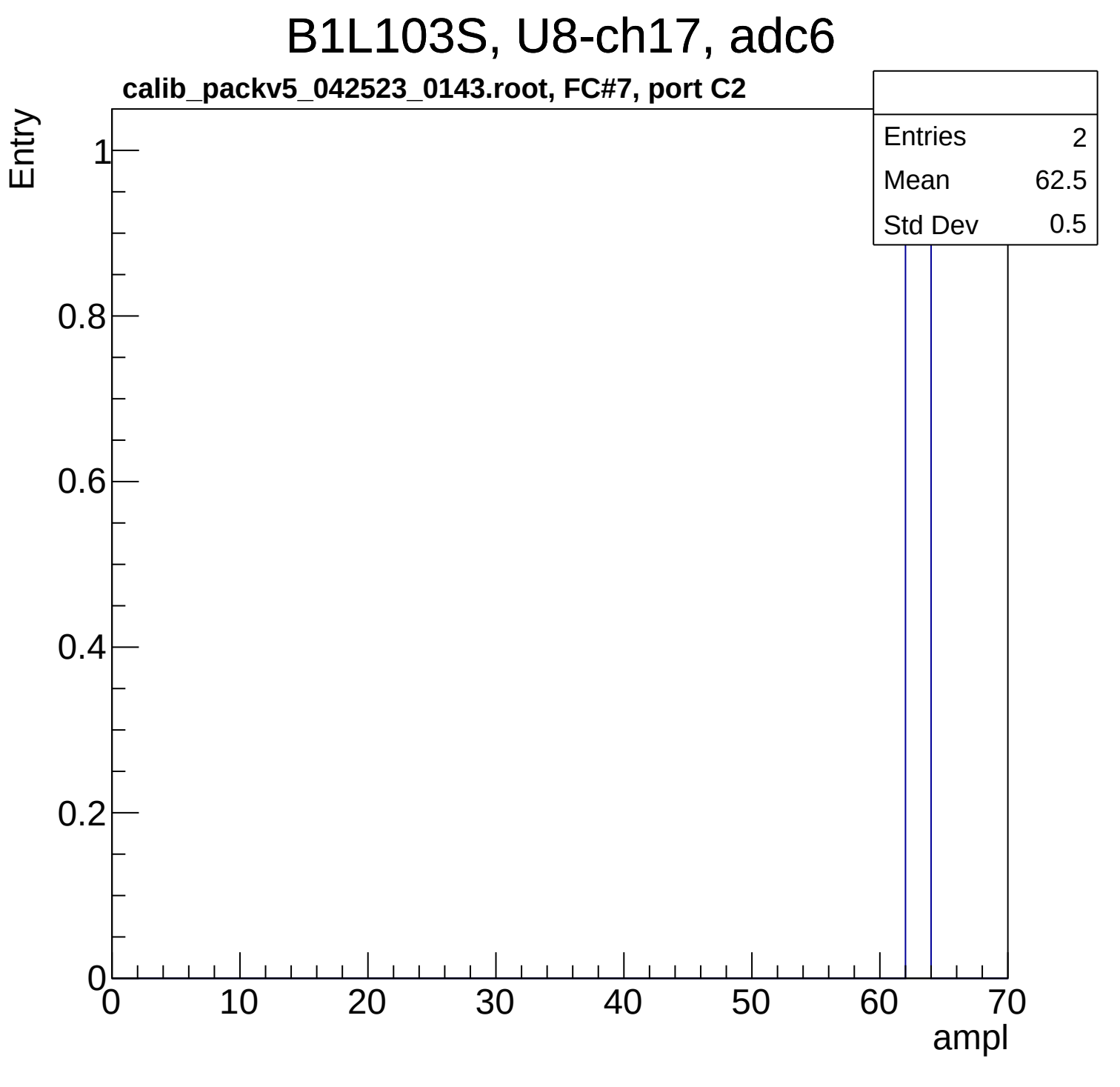

B1L103S, U8-ch17, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 37.93
Std Dev 3.22
Gaus mean : 38.2740
Gaus Width: 3.3148
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

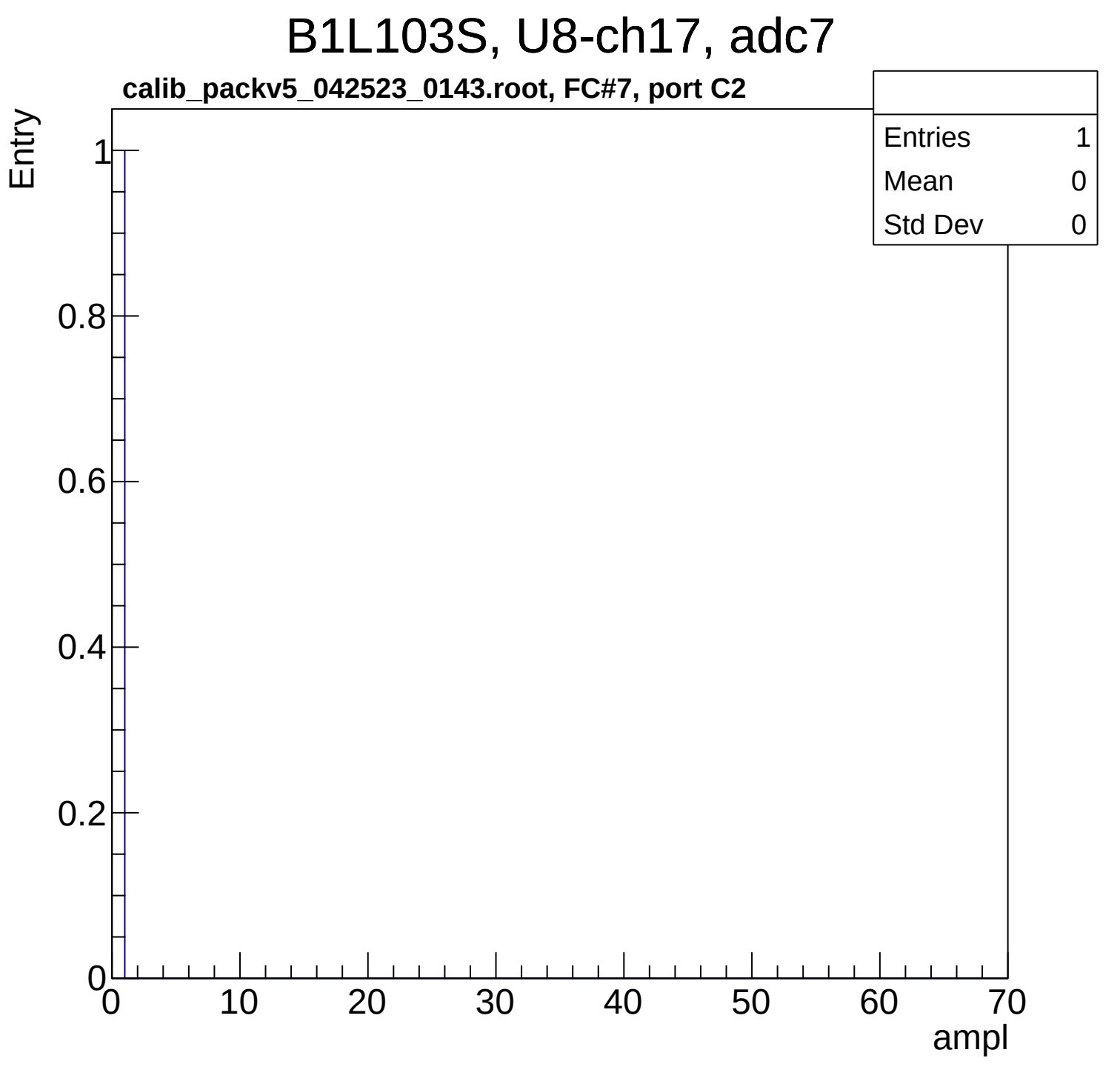

B1L103S, U8-ch17, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 44.14
Std Dev 3.658
Gaus mean : 44.3587
Gaus Width: 4.2672
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

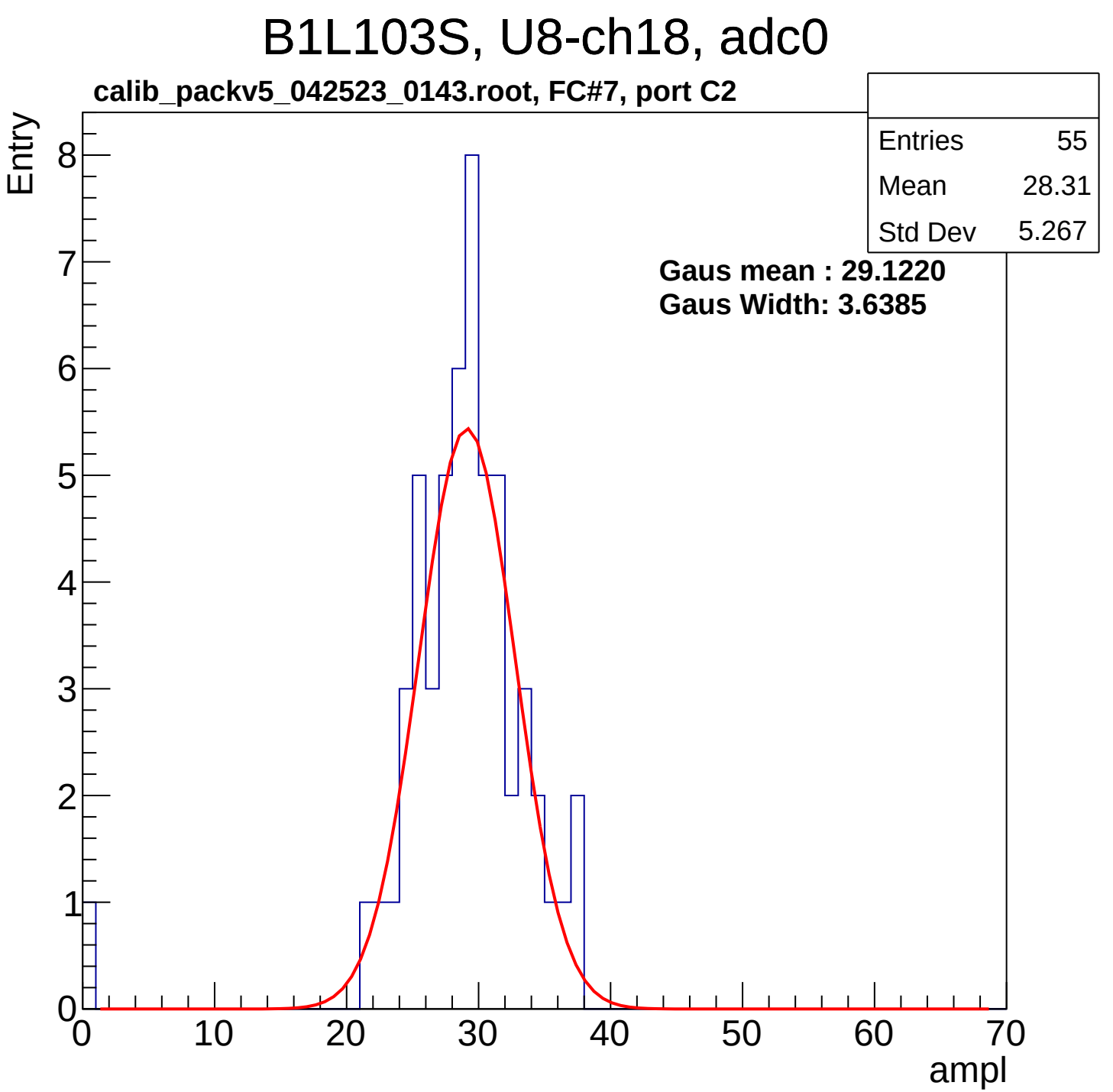

B1L103S, U8-ch17, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 51.64
Std Dev 3.631
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

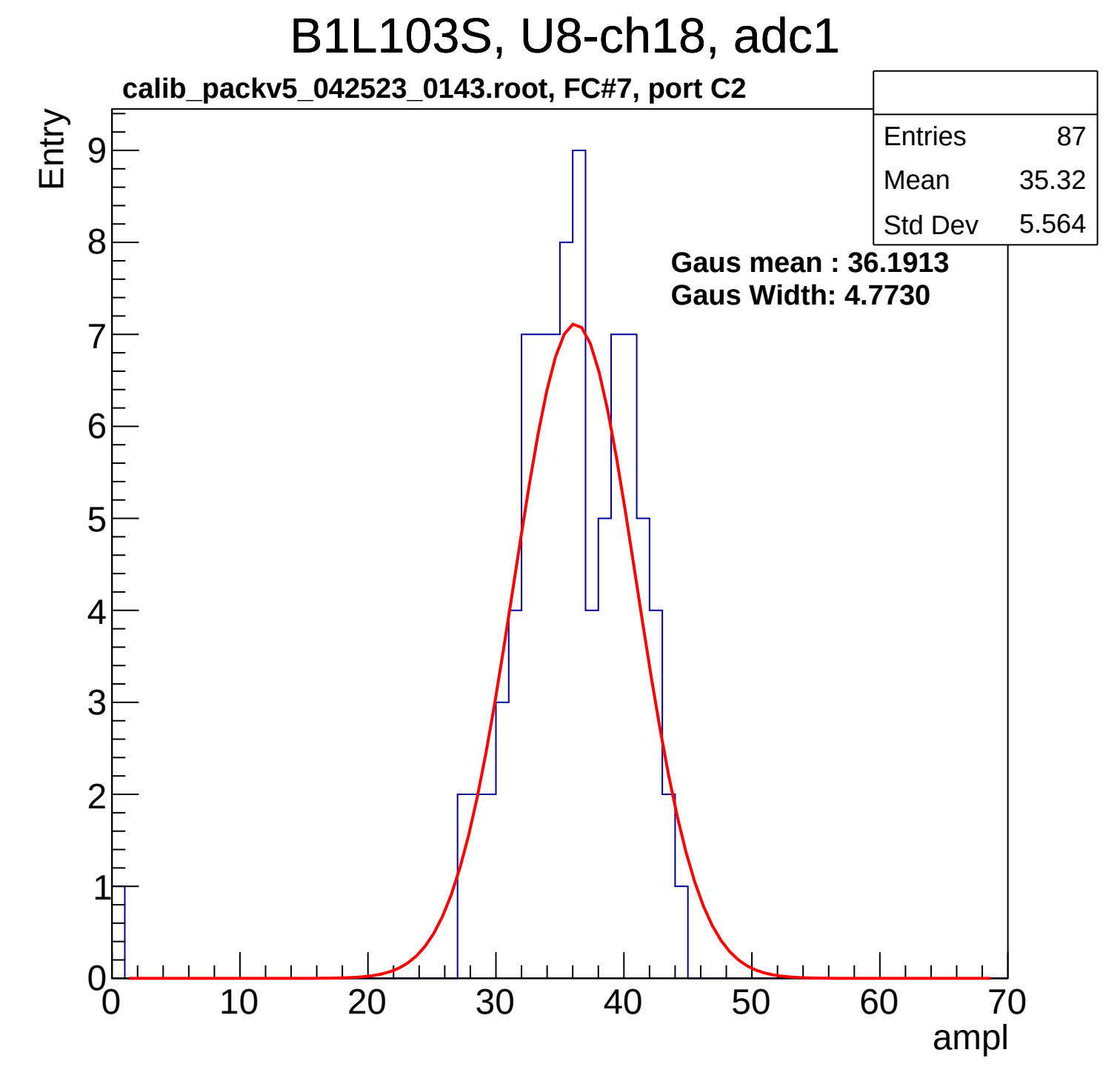

B1L103S, U8-ch17, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 56.12
Std Dev 3.601
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

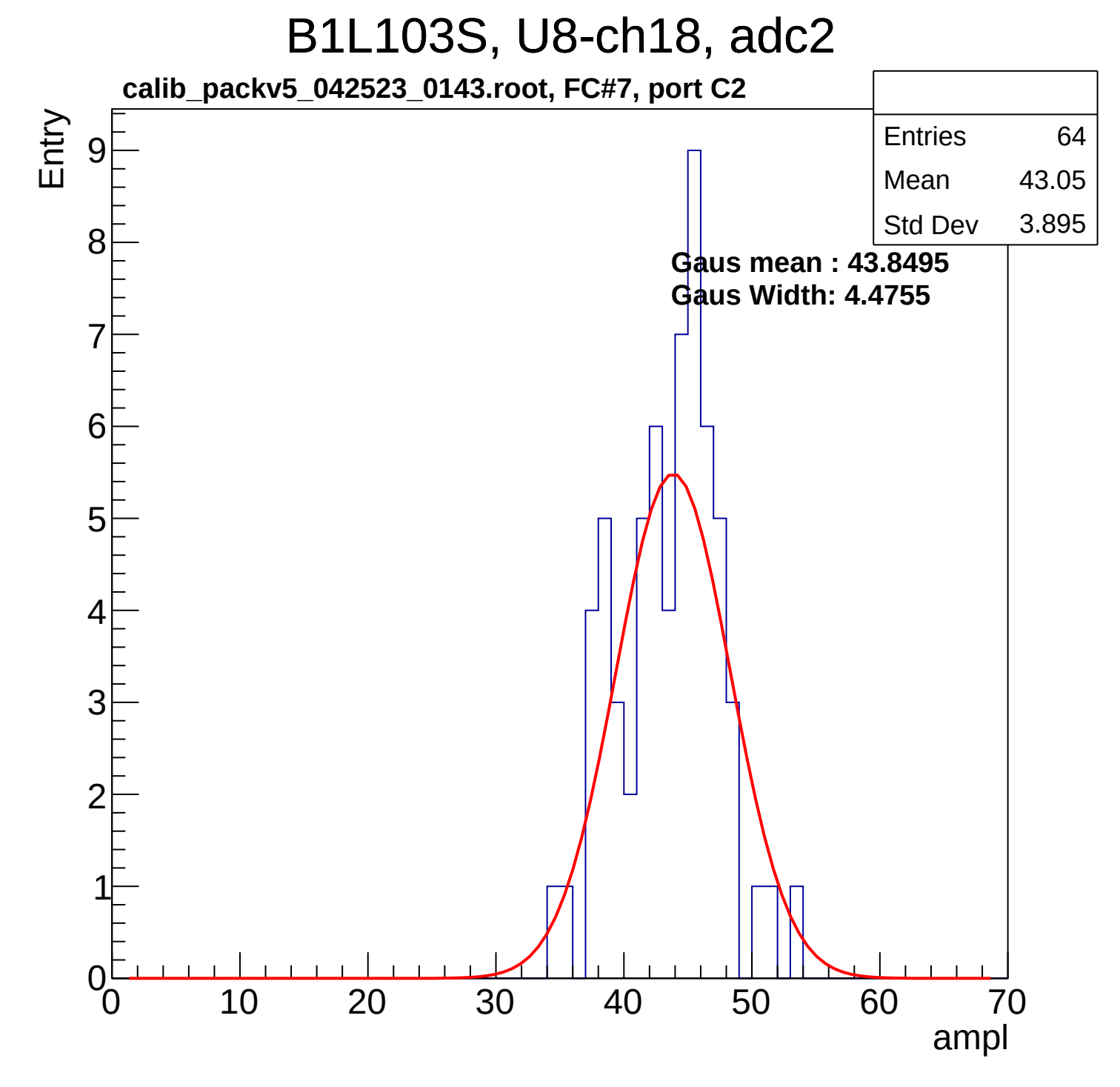

B1L103S, U8-ch17, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 38
Mean 58.76
Std Dev 10
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

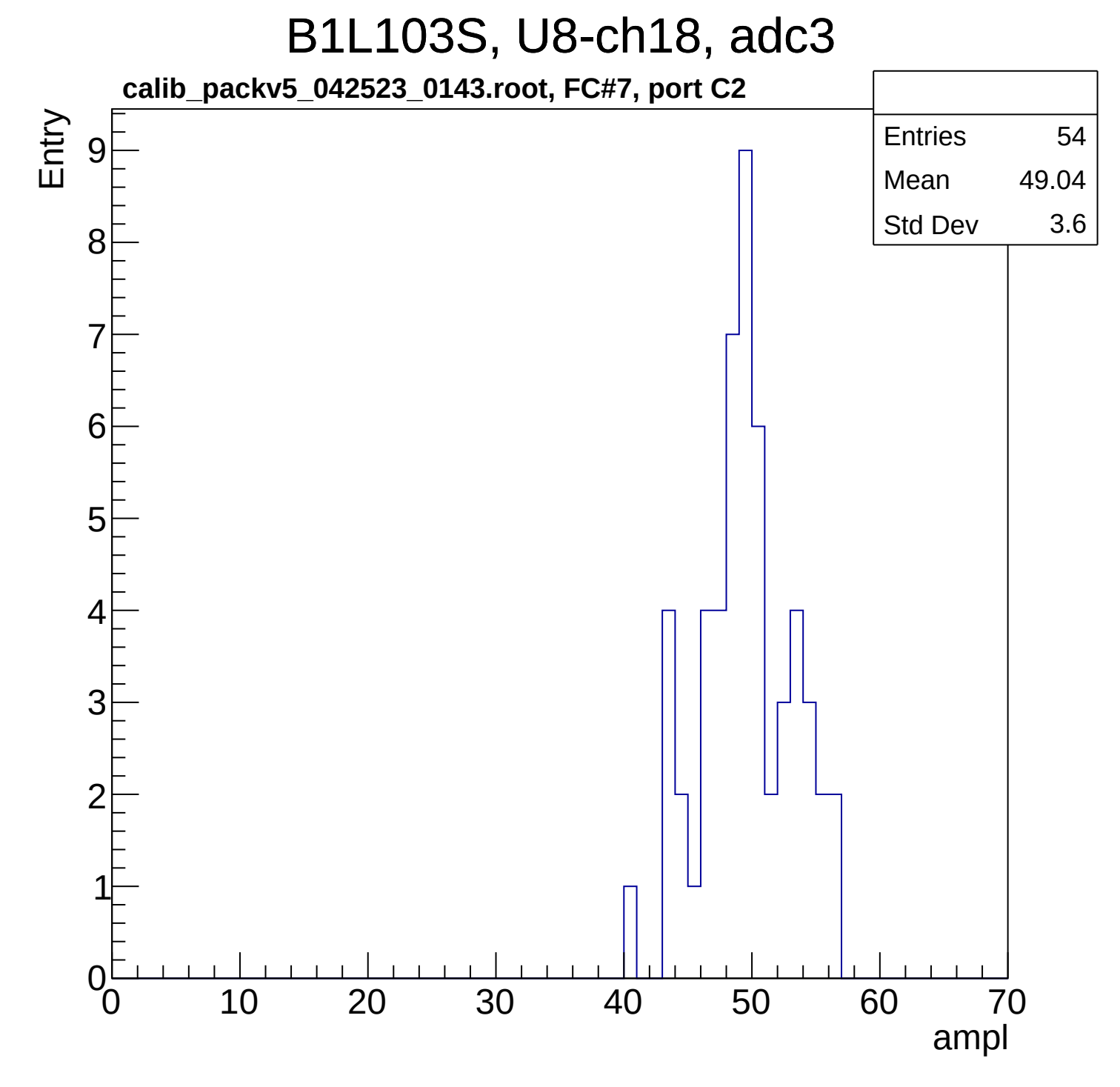

B1L103S, U8-ch17, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

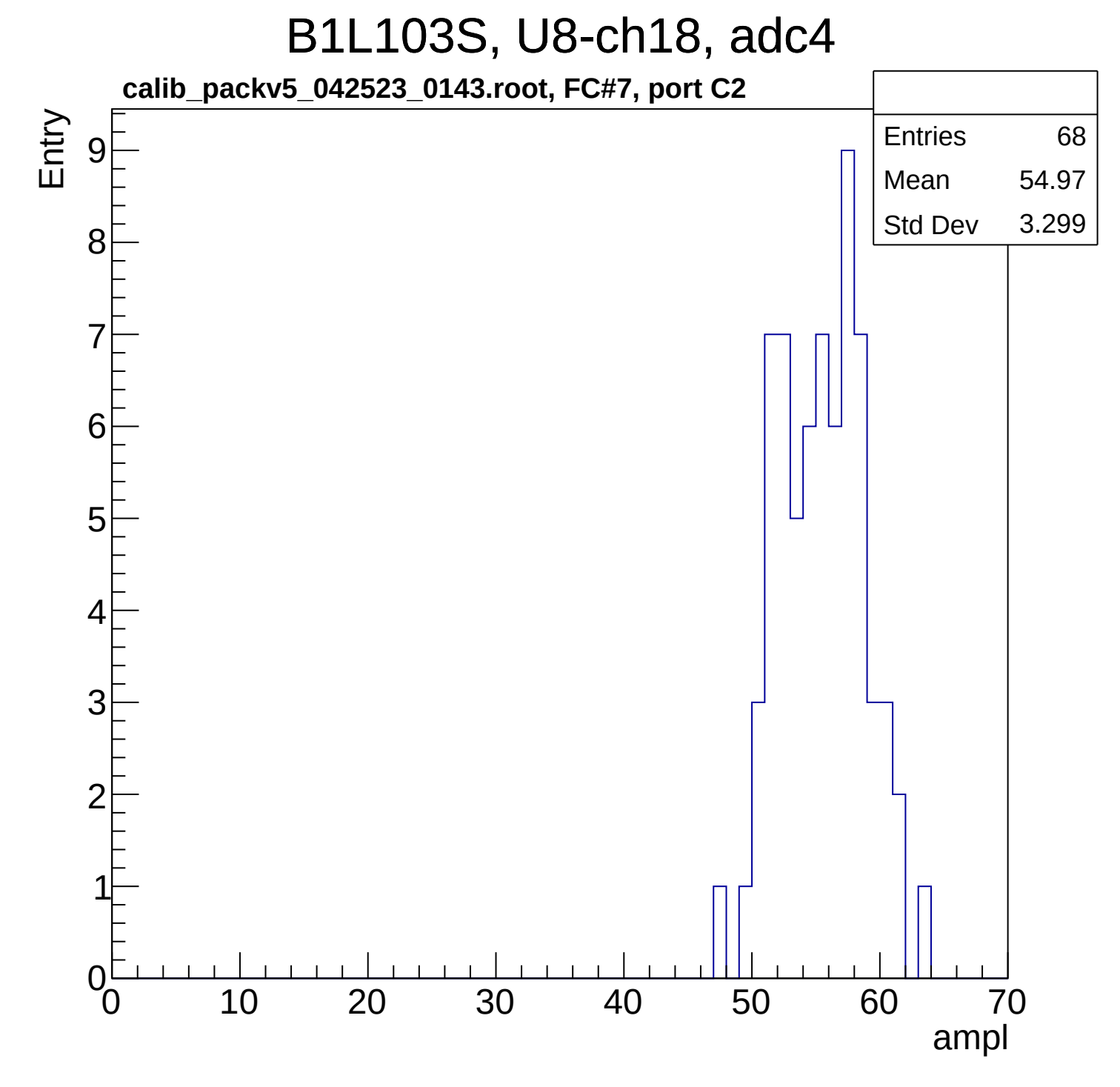

B1L103S, U8-ch17, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

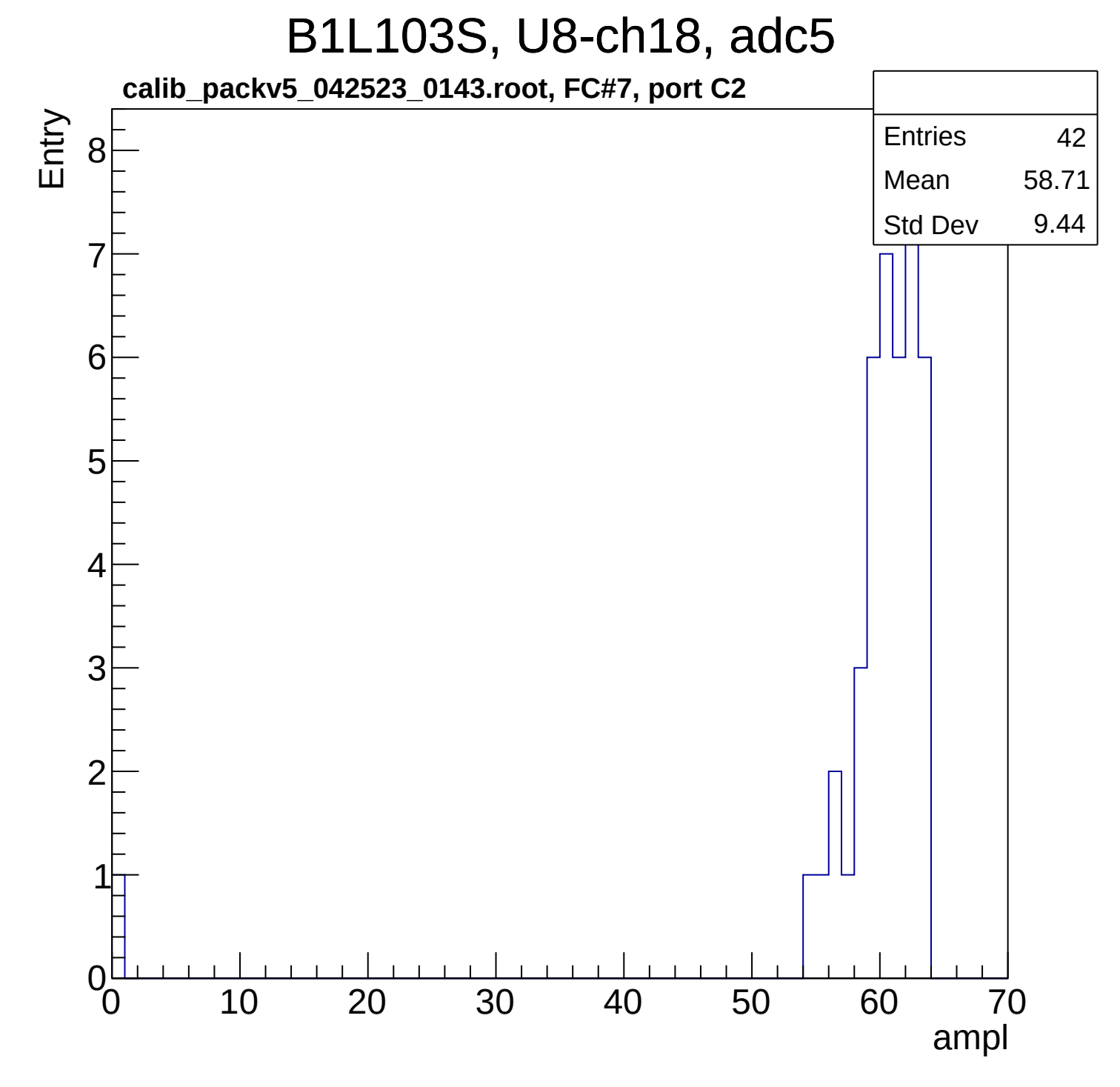

B1L103S, U8-ch18, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 28.31
Std Dev 5.267
Gaus mean : 29.1220
Gaus Width: 3.6385
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

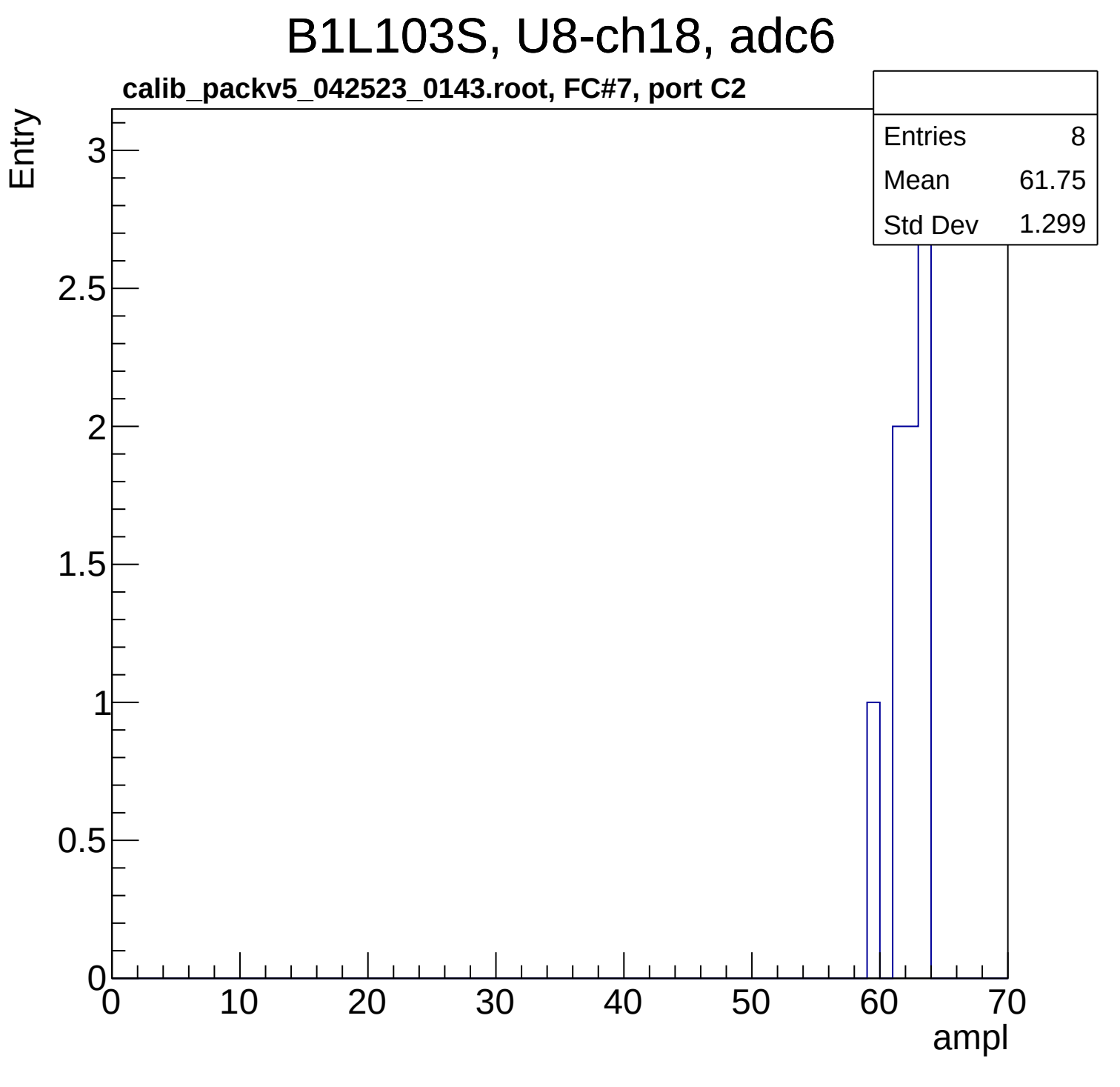

B1L103S, U8-ch18, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 87
Mean 35.32
Std Dev 5.564
Gaus mean : 36.1913
Gaus Width: 4.7730
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

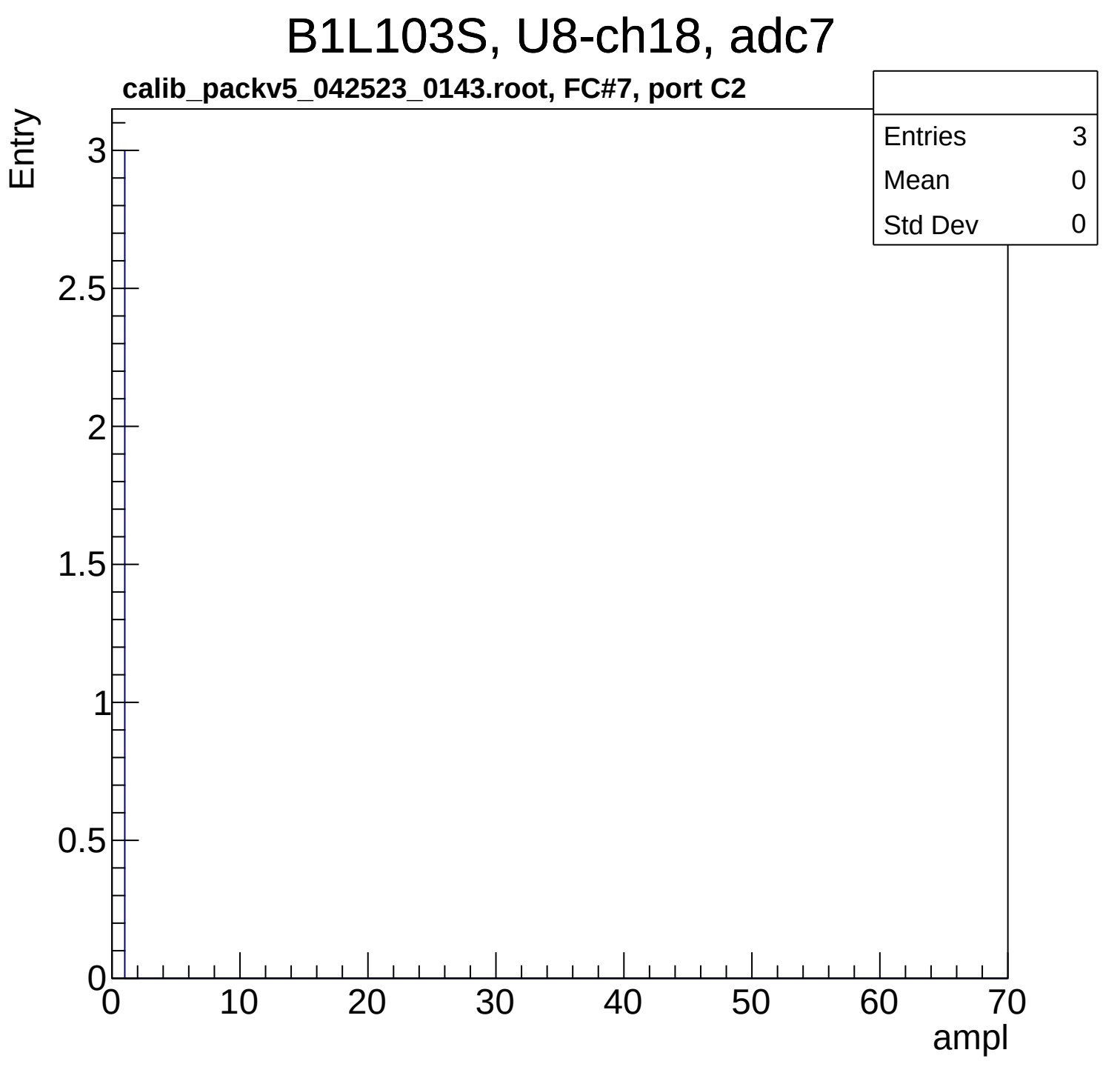

B1L103S, U8-ch18, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 43.05
Std Dev 3.895
Gaus mean : 43.8495
Gaus Width: 4.4755
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

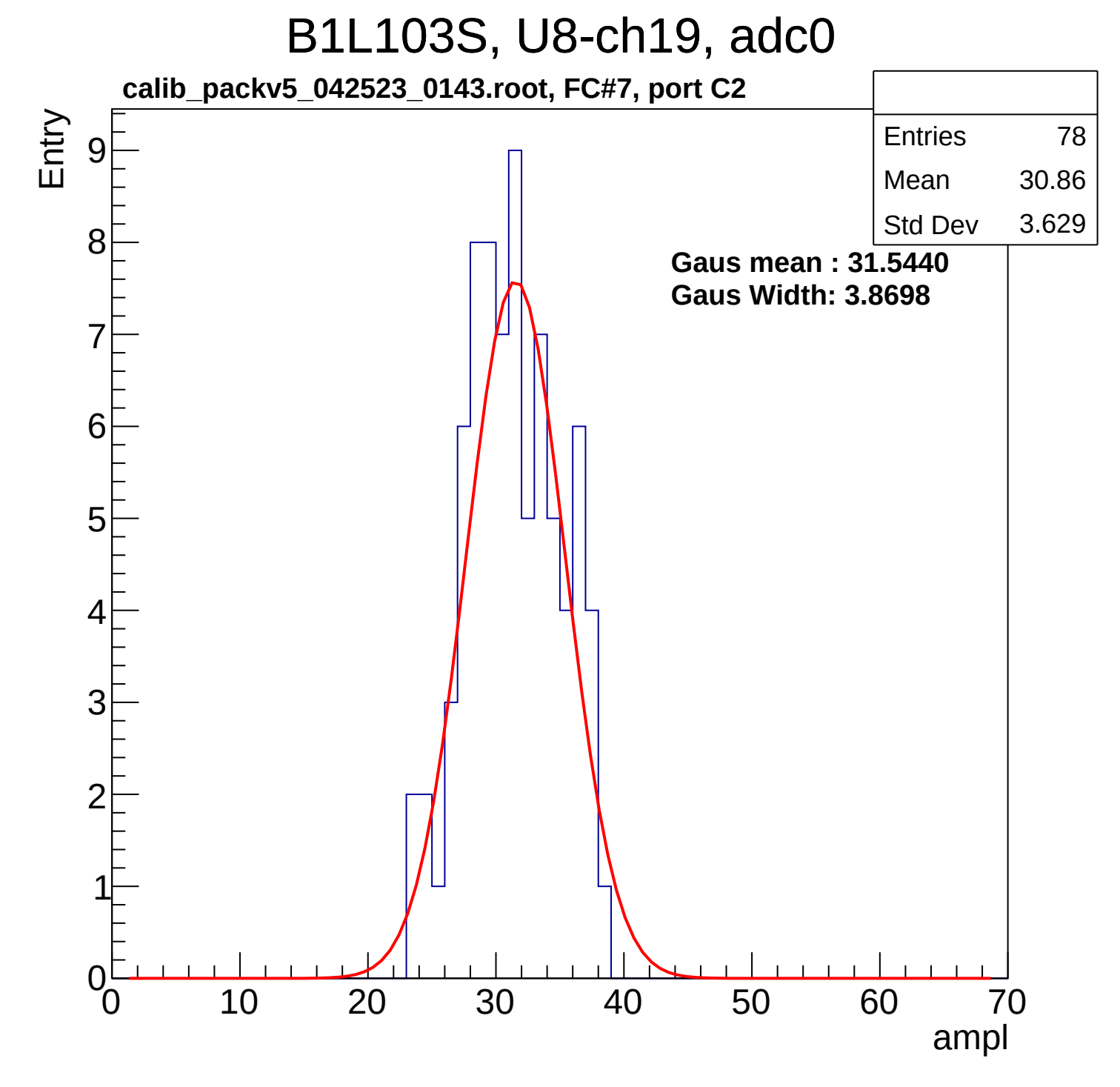

B1L103S, U8-ch18, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 49.04
Std Dev 3.6
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

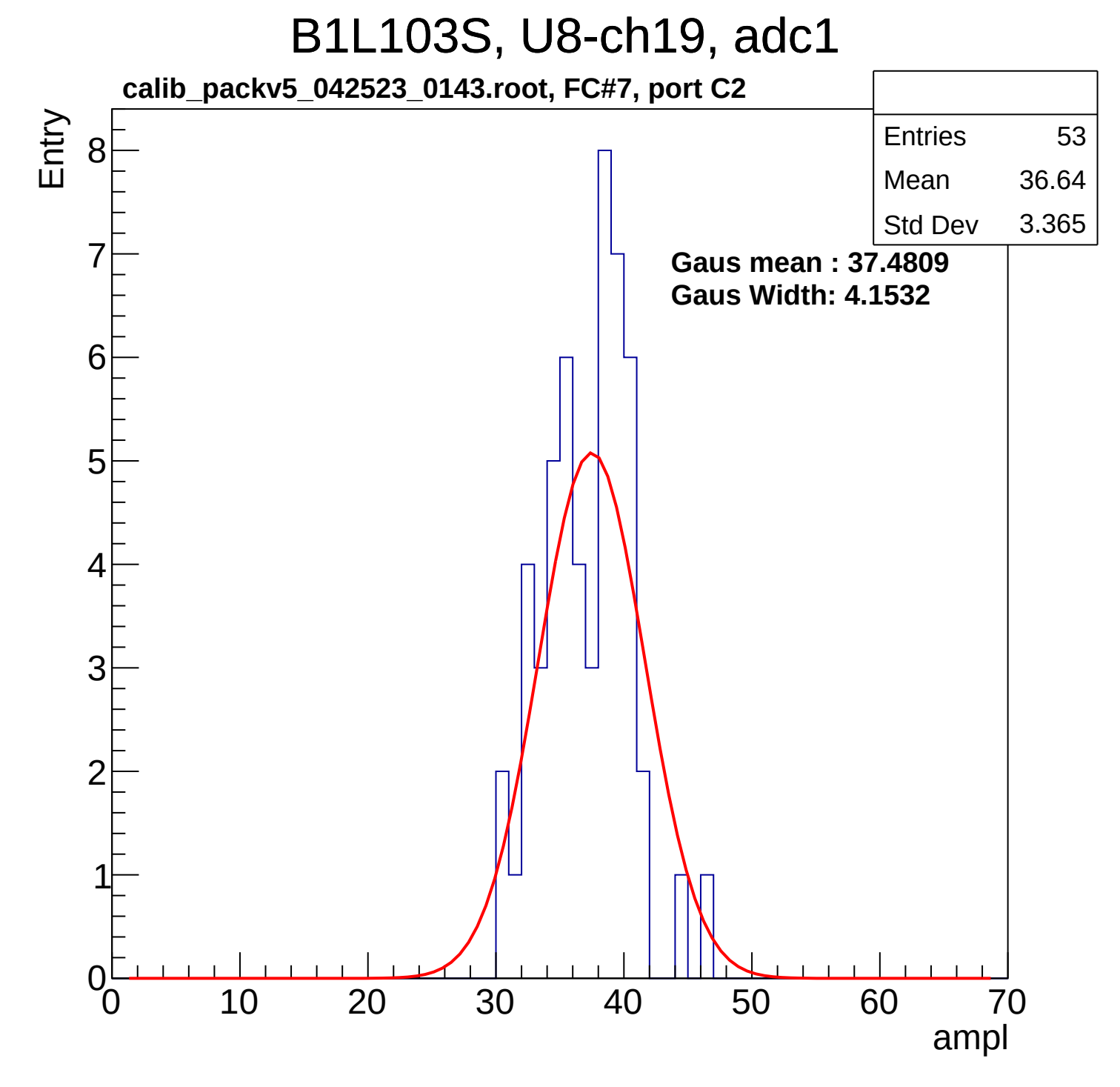

B1L103S, U8-ch18, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 54.97
Std Dev 3.299
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

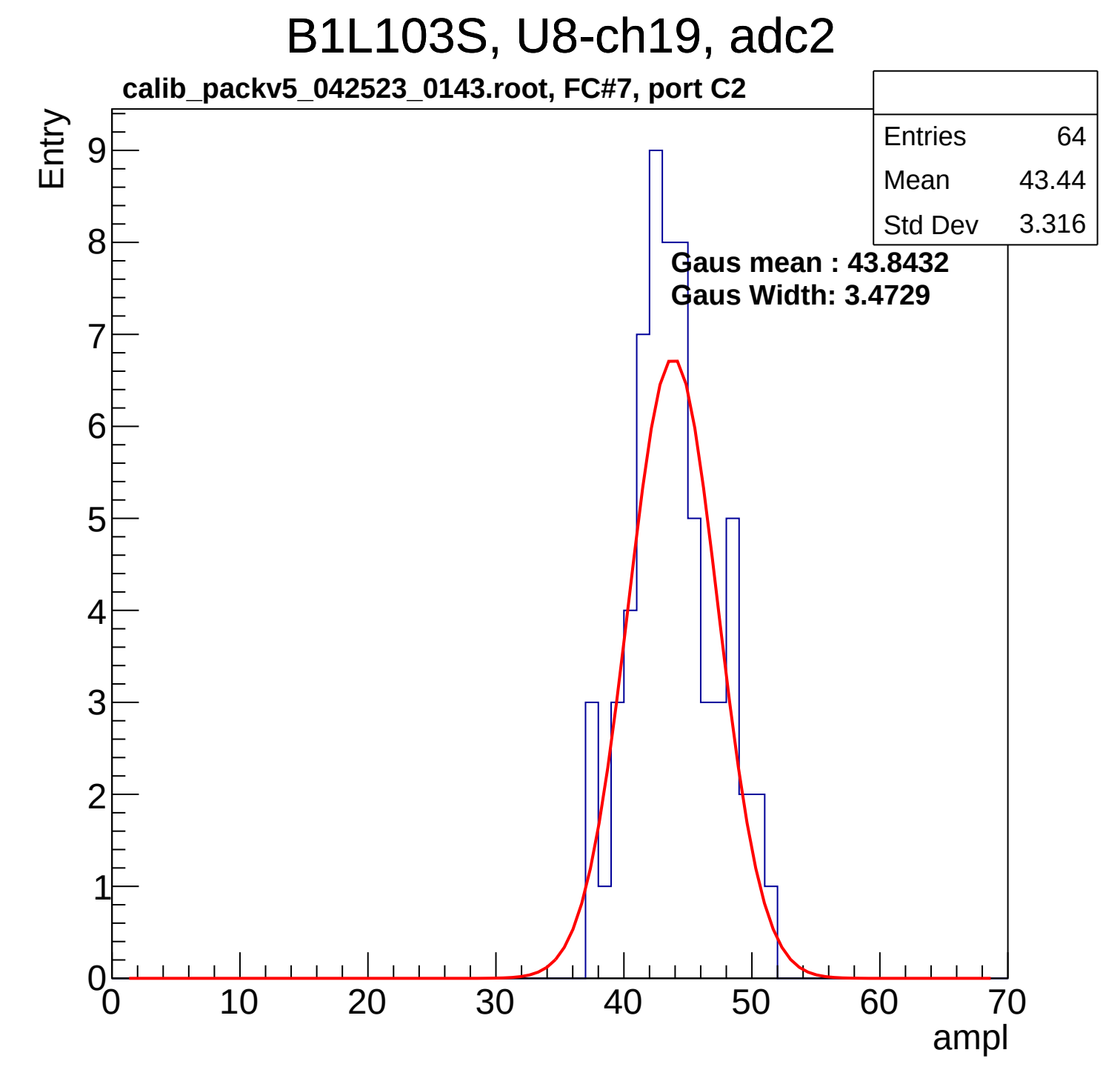

B1L103S, U8-ch18, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 42
Mean 58.71
Std Dev 9.44
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

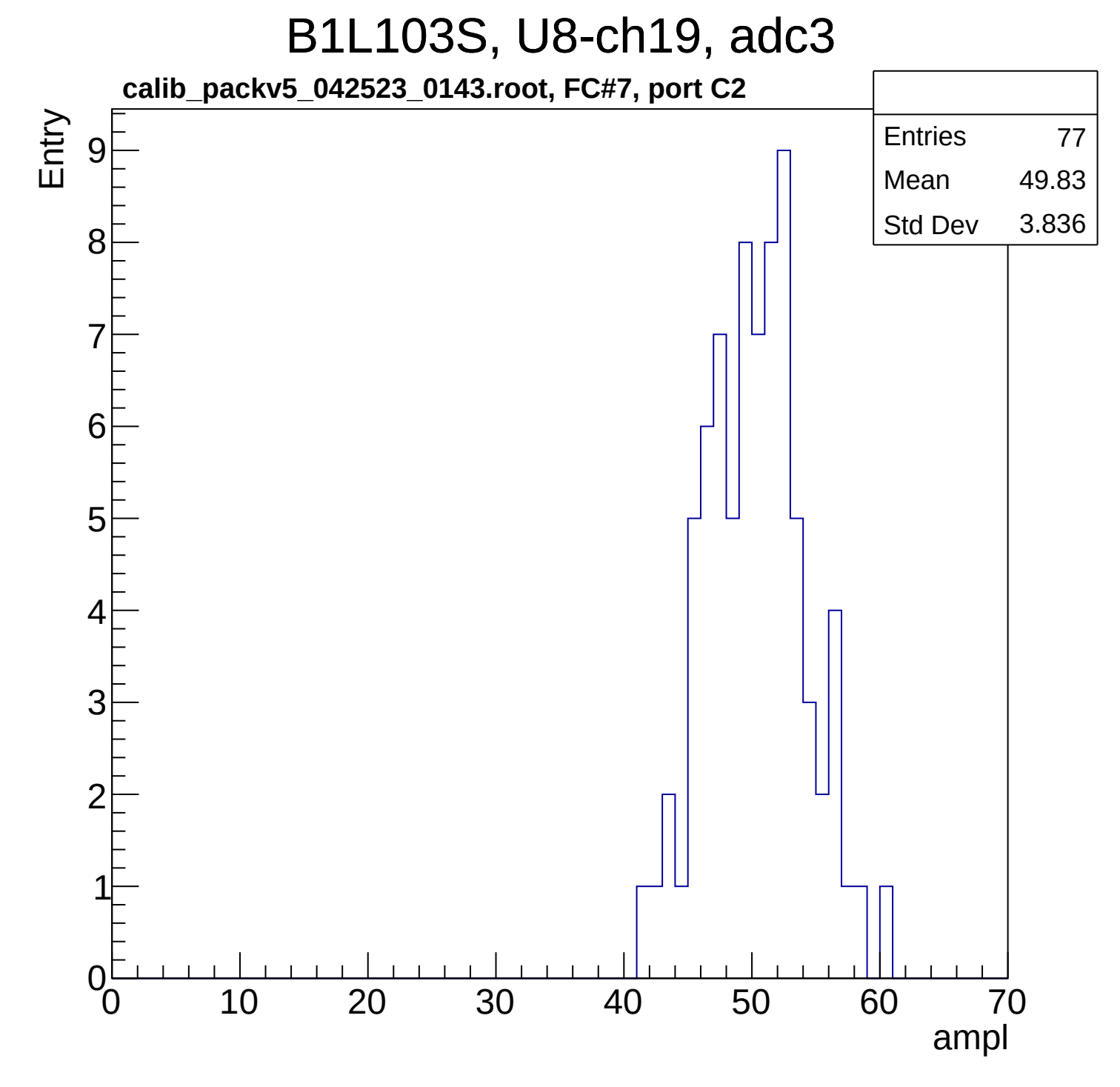

B1L103S, U8-ch18, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 8
Mean 61.75
Std Dev 1.299
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

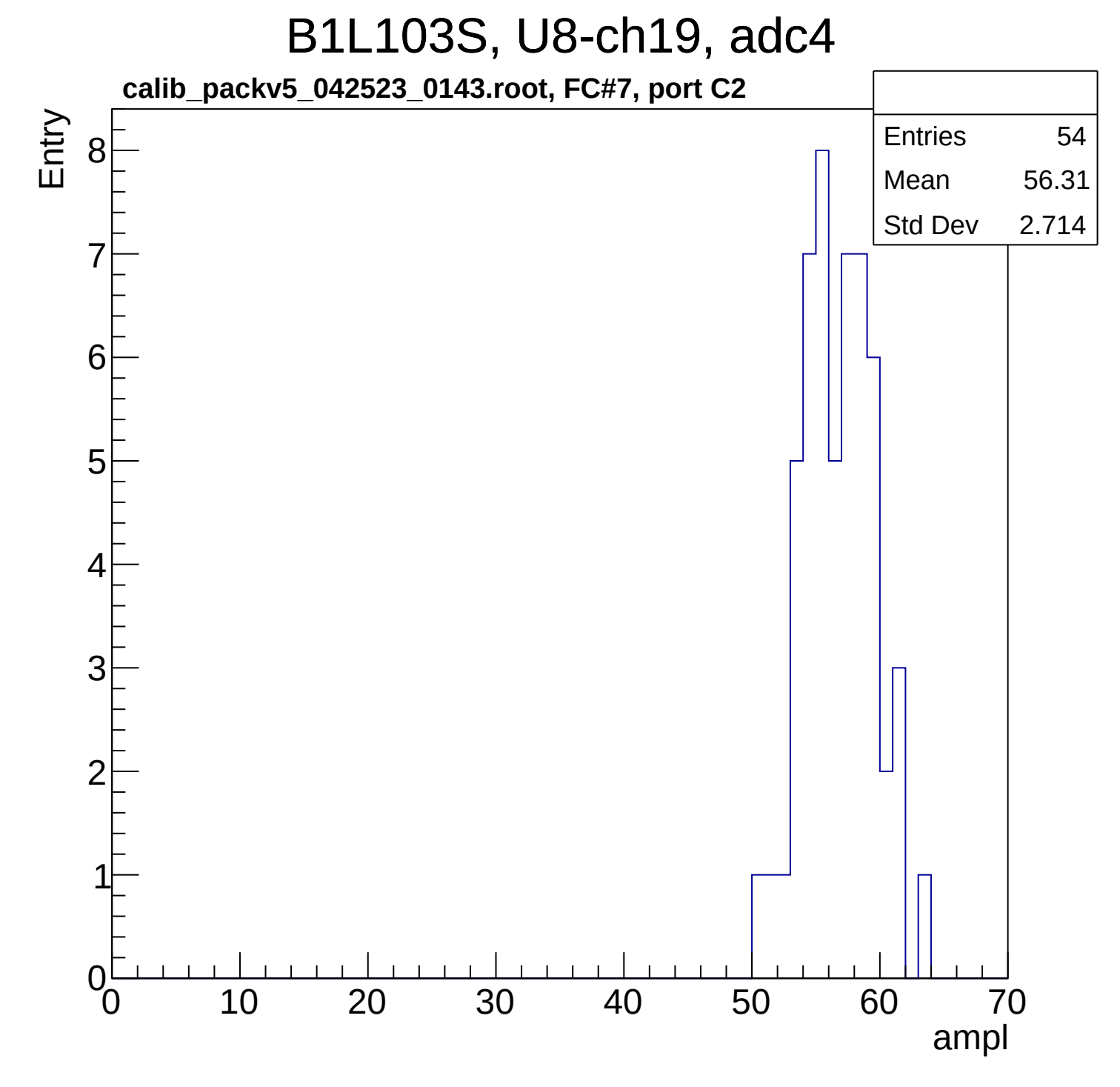

B1L103S, U8-ch18, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 0
Std Dev 0
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl

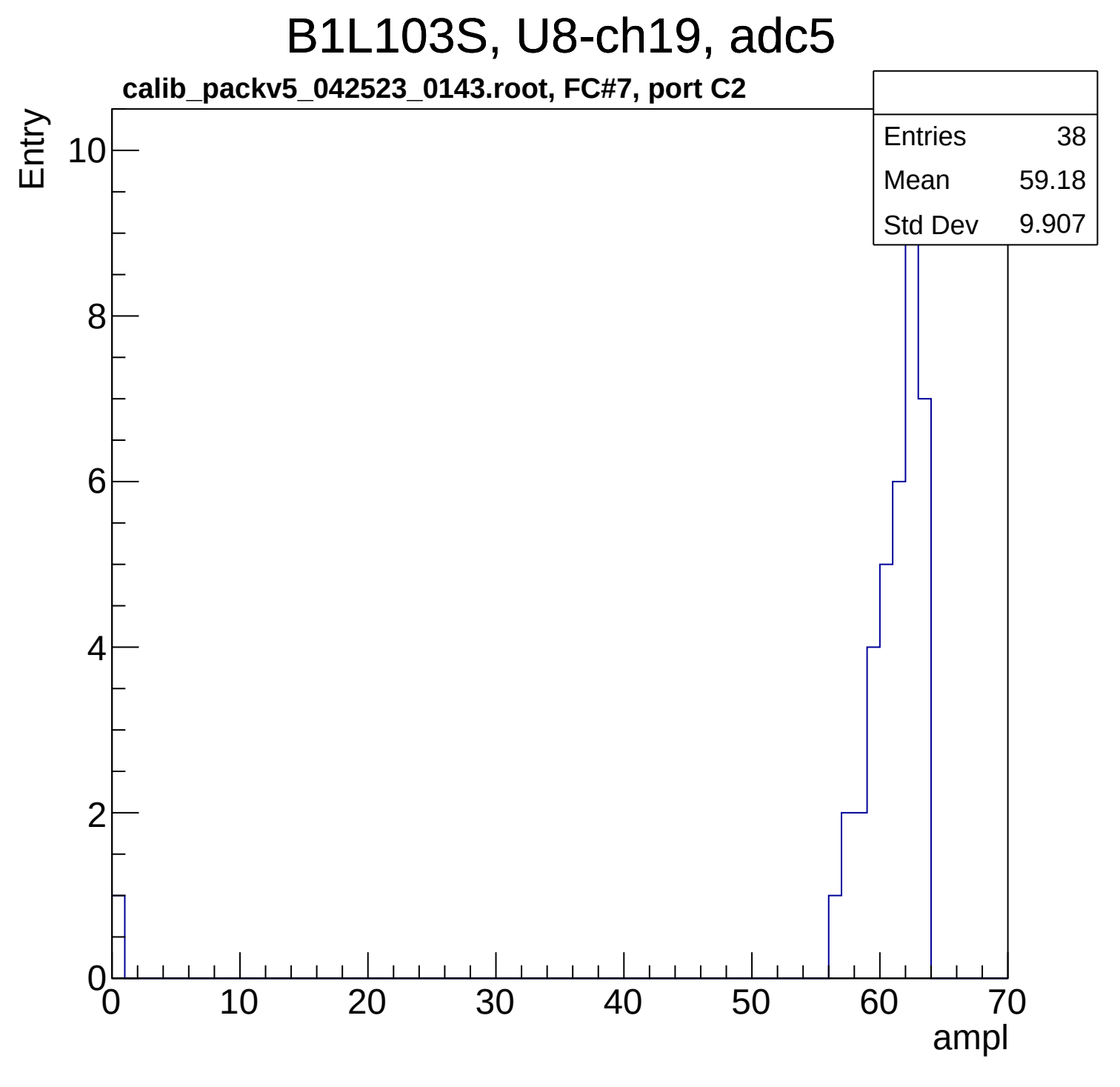

B1L103S, U8-ch19, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 30.86
Std Dev 3.629
Gaus mean : 31.5440
Gaus Width: 3.8698
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

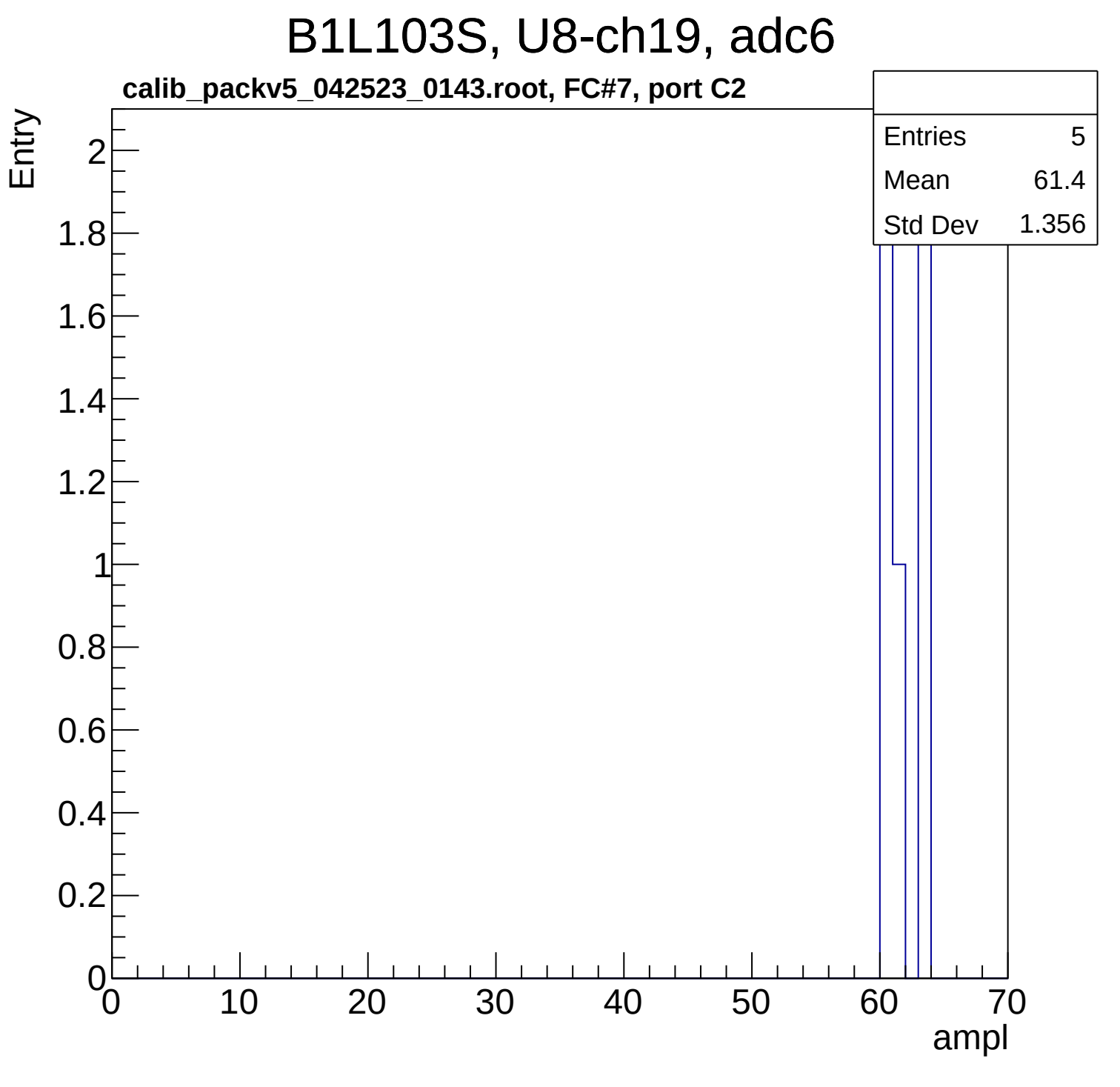

B1L103S, U8-ch19, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 36.64
Std Dev 3.365
Gaus mean : 37.4809
Gaus Width: 4.1532
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

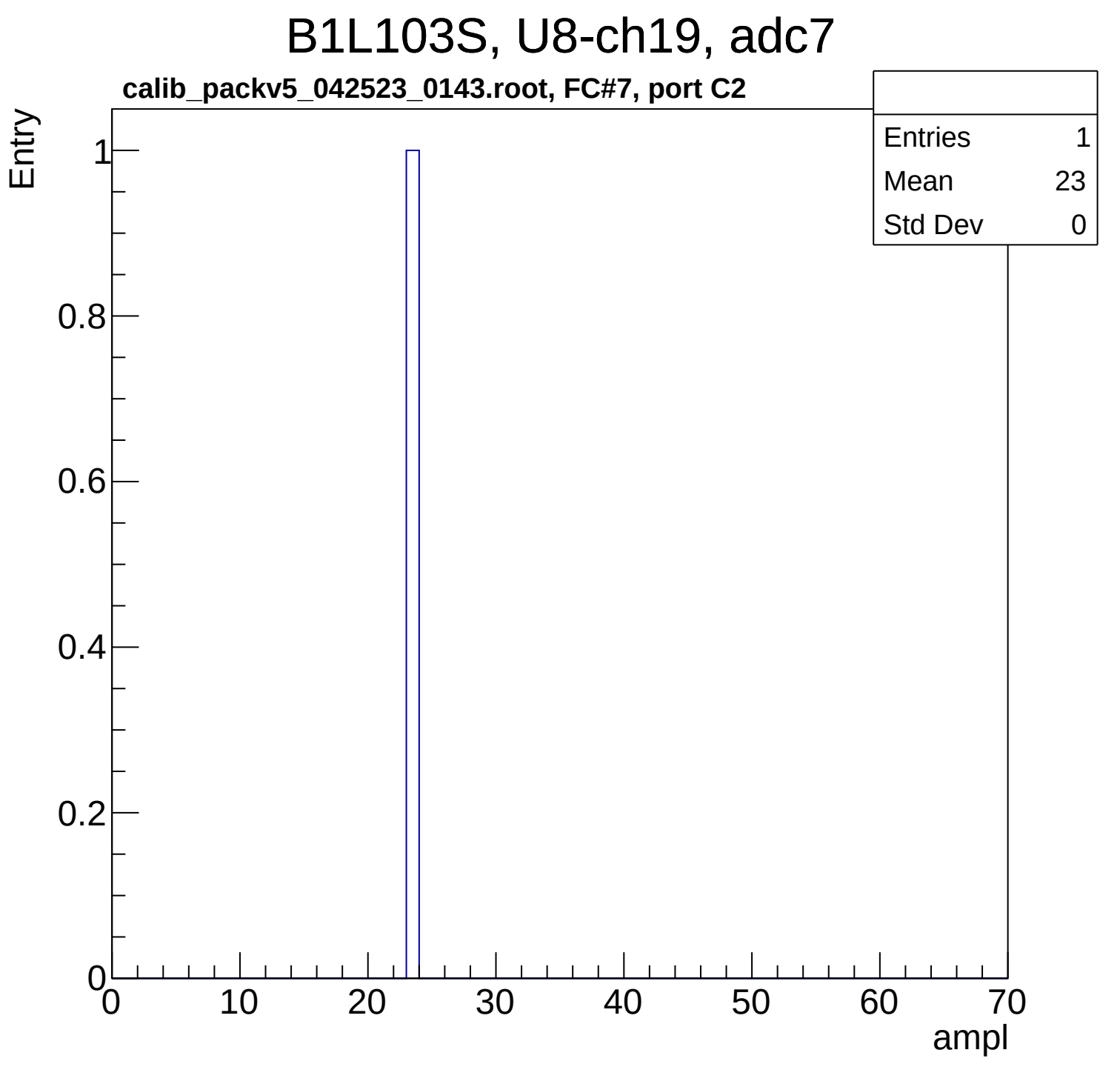

B1L103S, U8-ch19, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 43.44
Std Dev 3.316
Gaus mean : 43.8432
Gaus Width: 3.4729
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

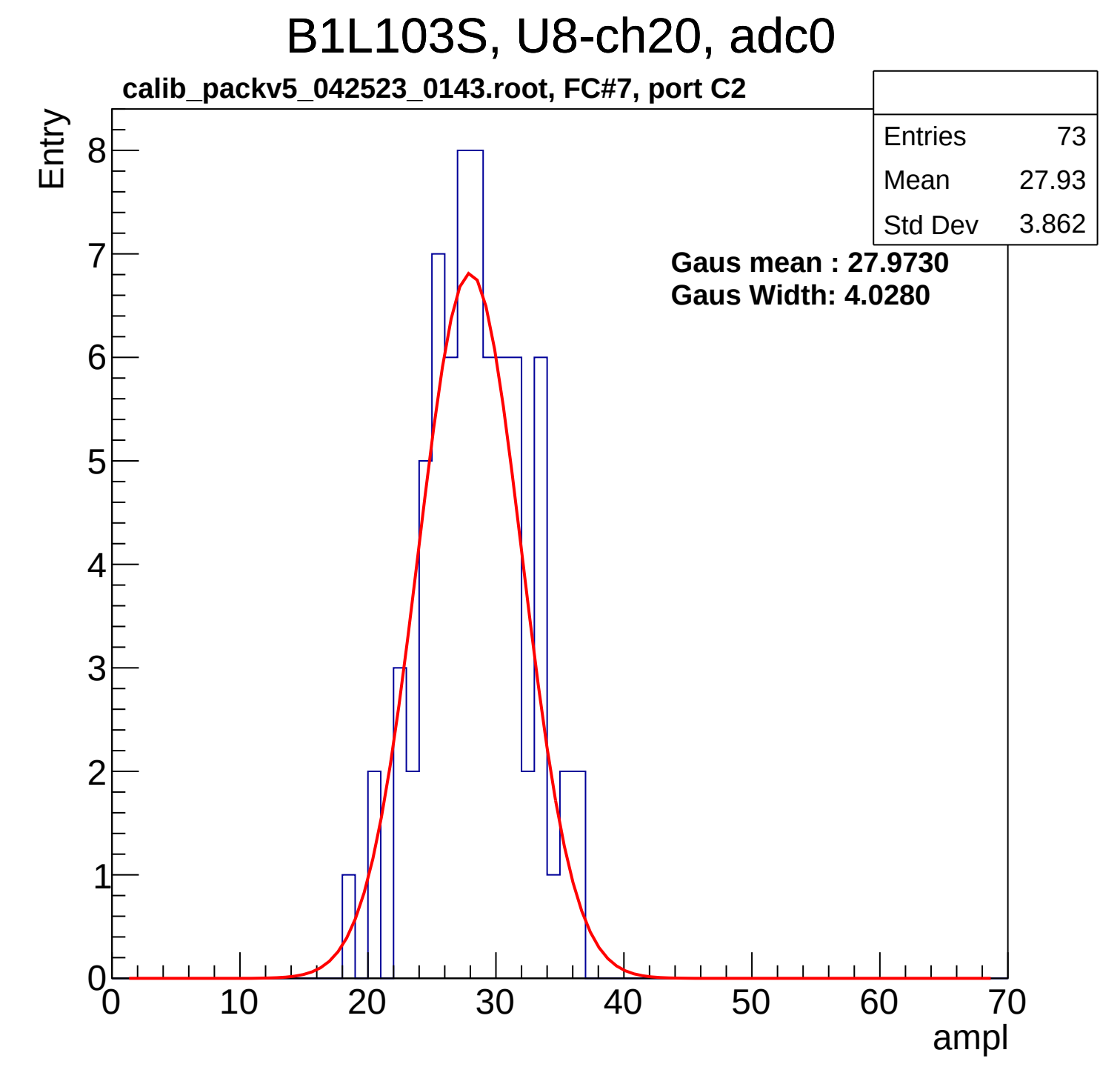

B1L103S, U8-ch19, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 49.83
Std Dev 3.836
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

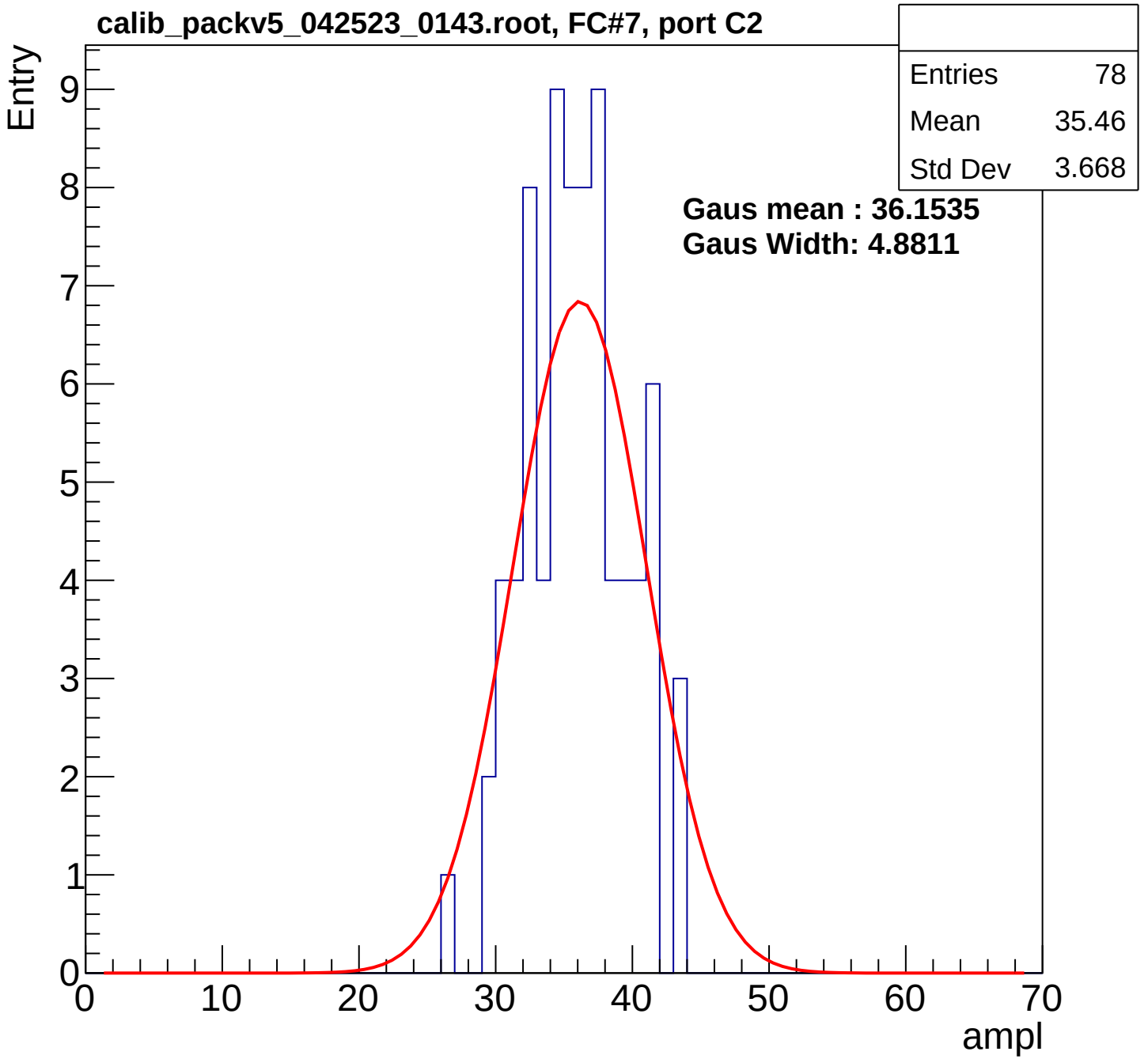

B1L103S, U8-ch19, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 56.31
Std Dev 2.714
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

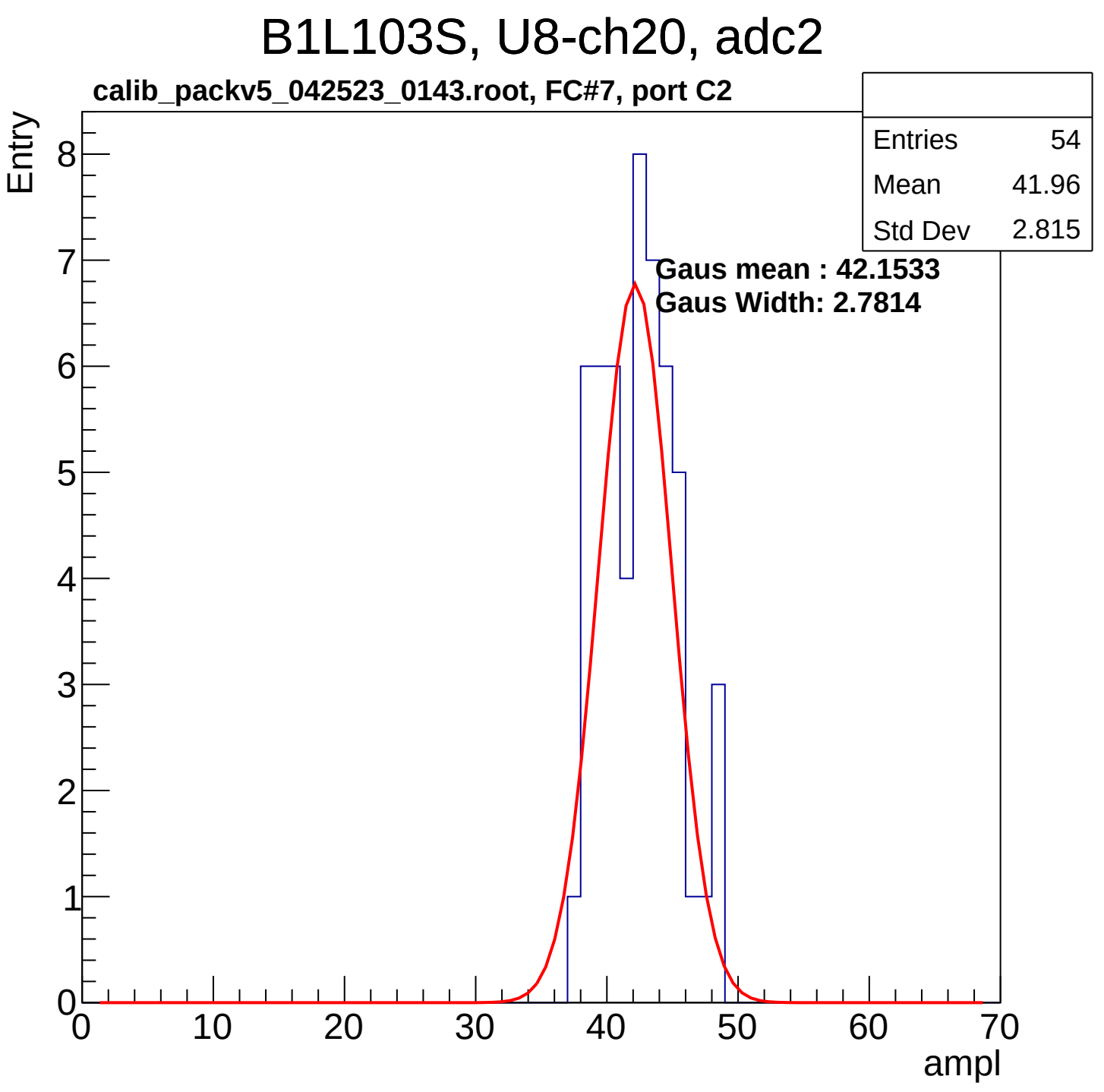

B1L103S, U8-ch19, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 38
Mean 59.18
Std Dev 9.907
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

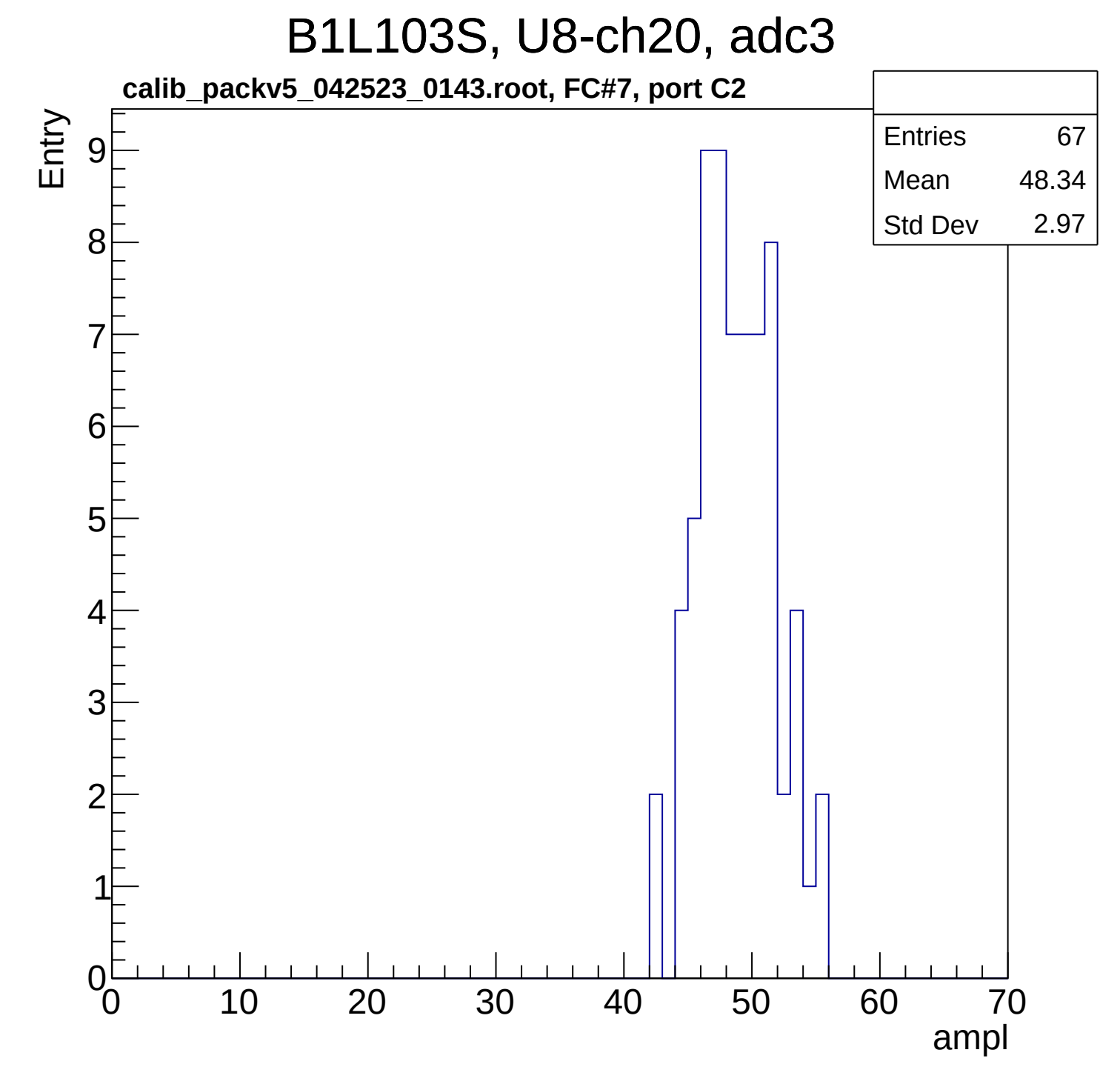

B1L103S, U8-ch19, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 61.4
Std Dev 1.356
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

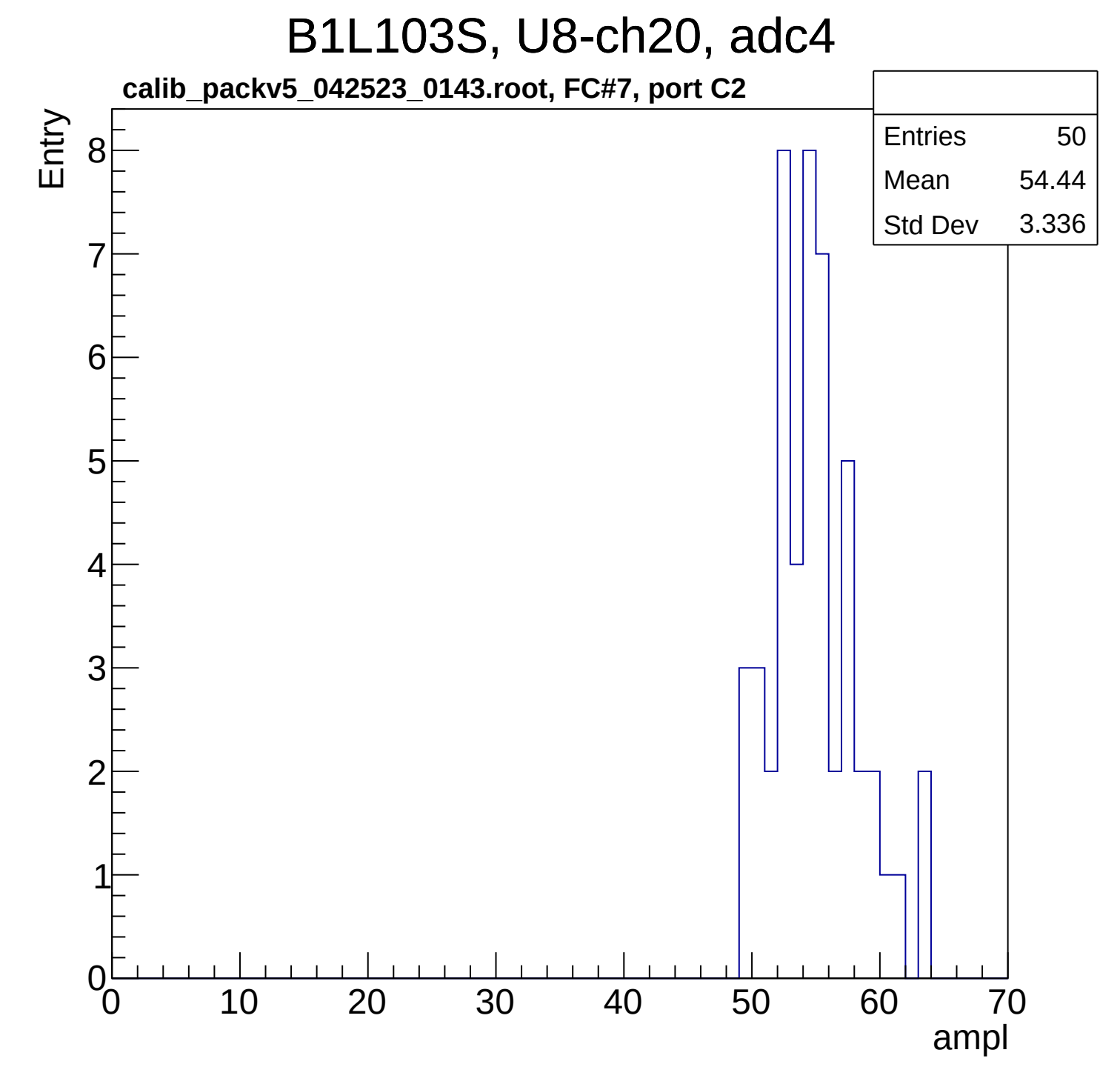

B1L103S, U8-ch19, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 23
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

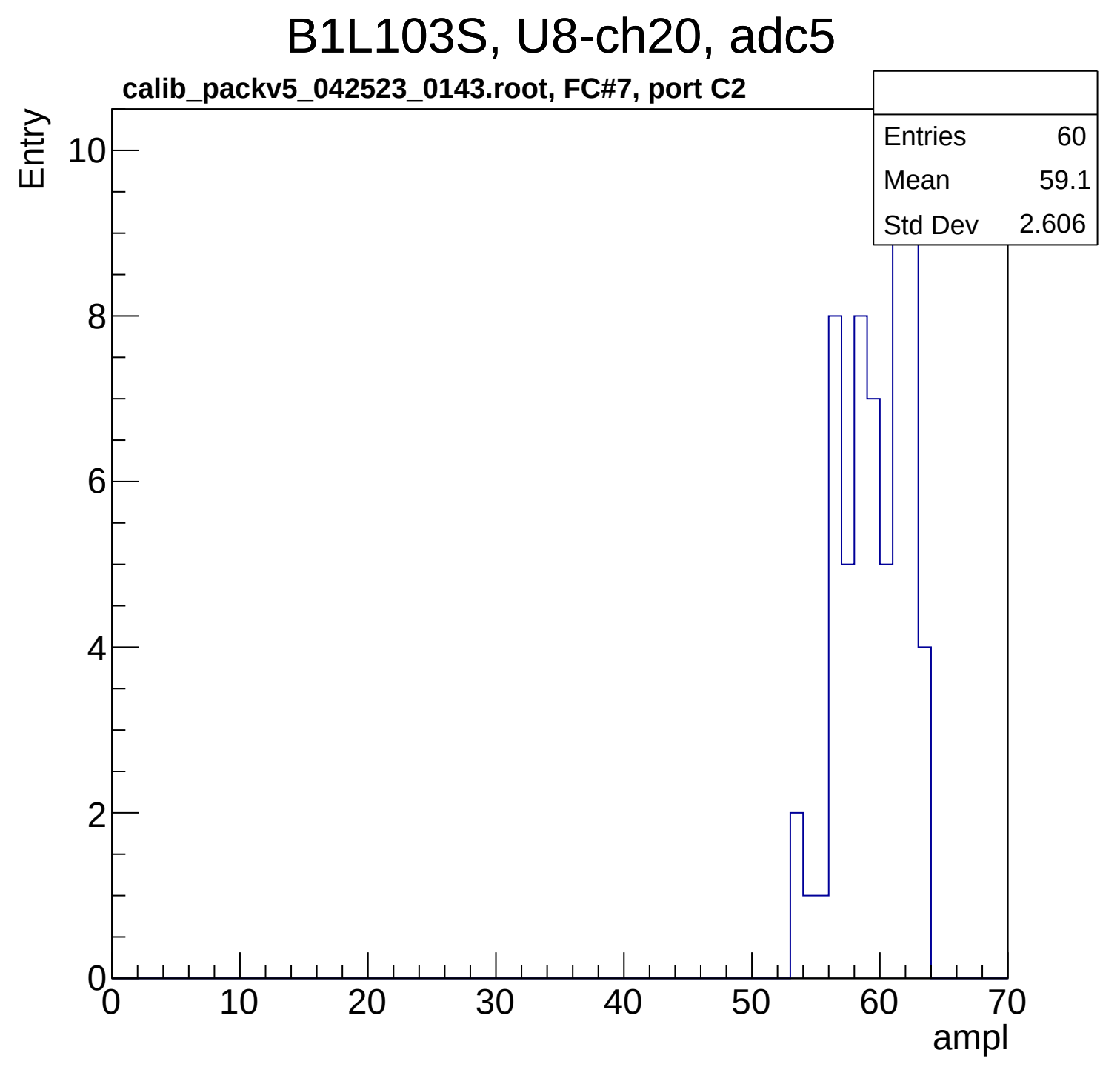

B1L103S, U8-ch20, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 27.93
Std Dev 3.862
Gaus mean : 27.9730
Gaus Width: 4.0280
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

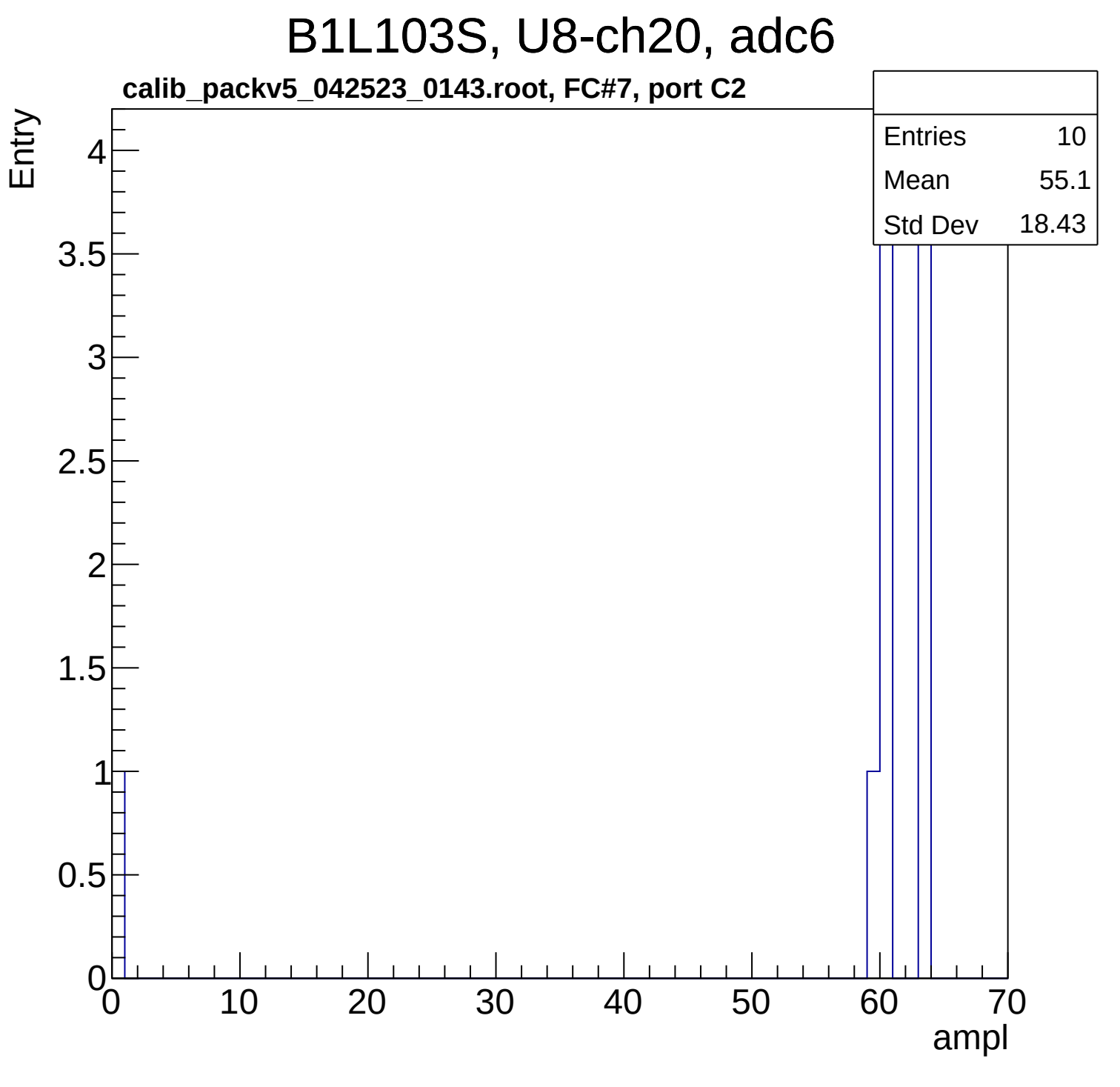

B1L103S, U8-ch20, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 35.46
Std Dev 3.668
Gaus mean : 36.1535
Gaus Width: 4.8811
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

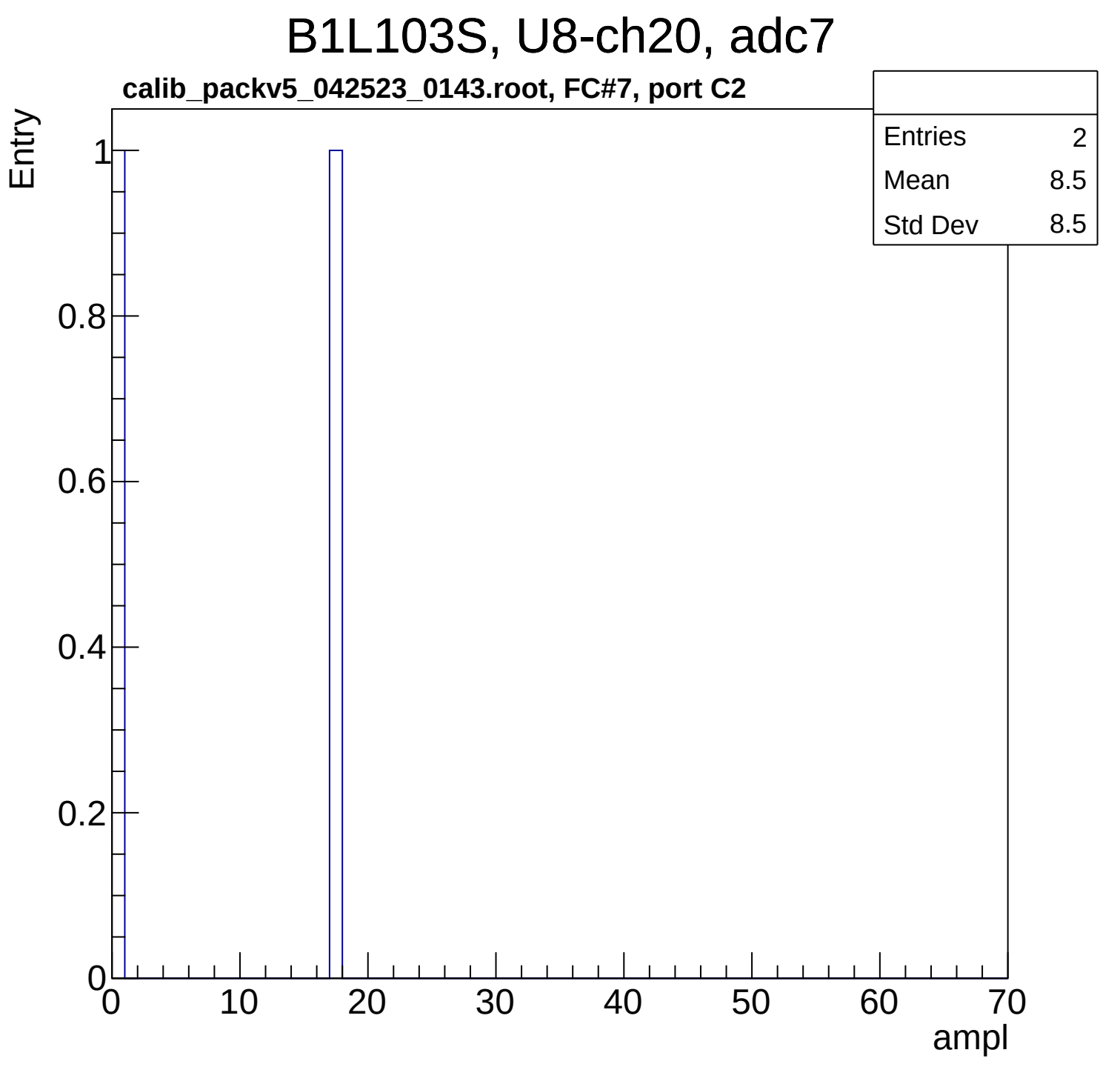

B1L103S, U8-ch20, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 41.96
Std Dev 2.815
Gaus mean : 42.1533
Gaus Width: 2.7814
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

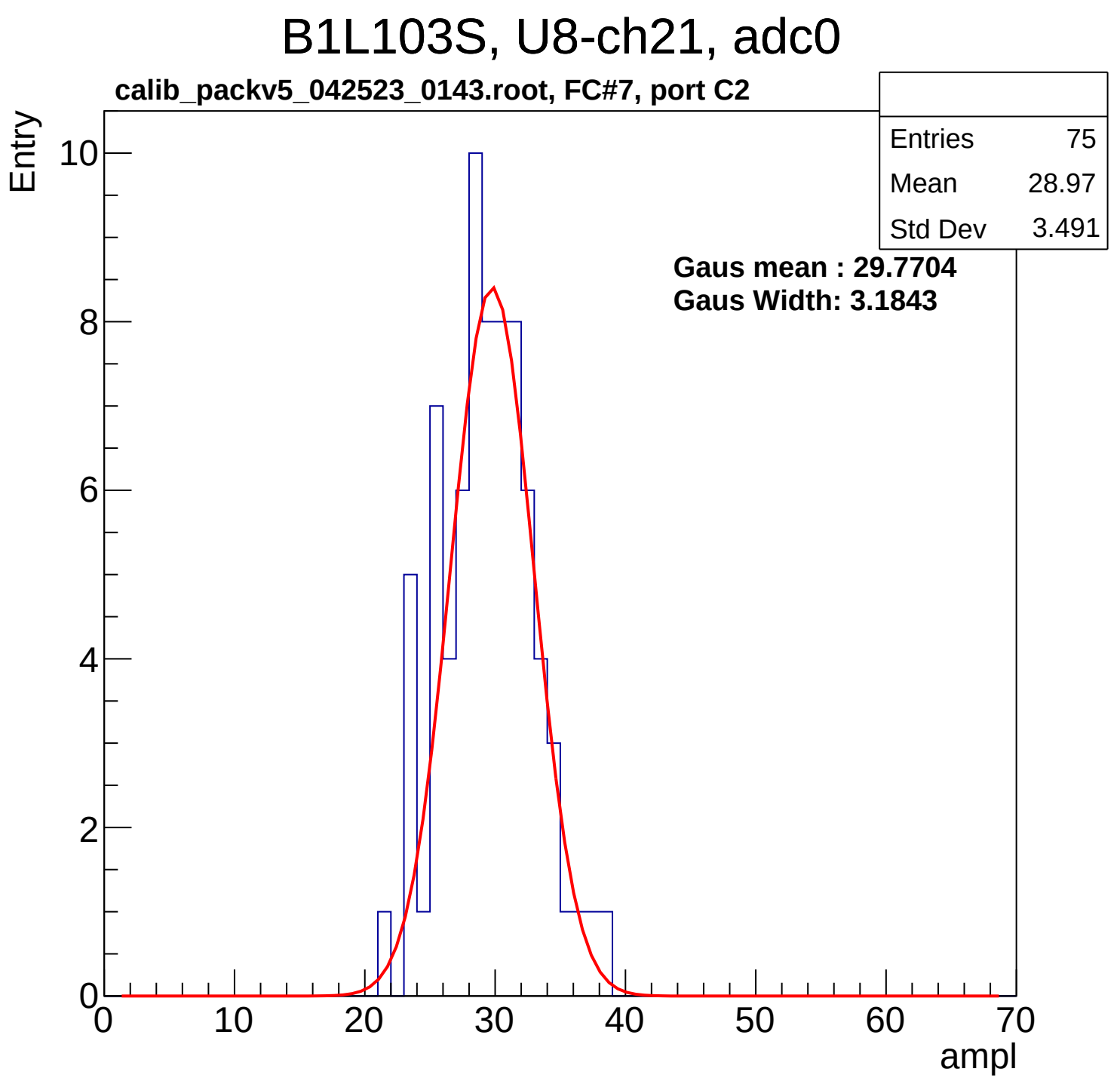

B1L103S, U8-ch20, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 48.34
Std Dev 2.97
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

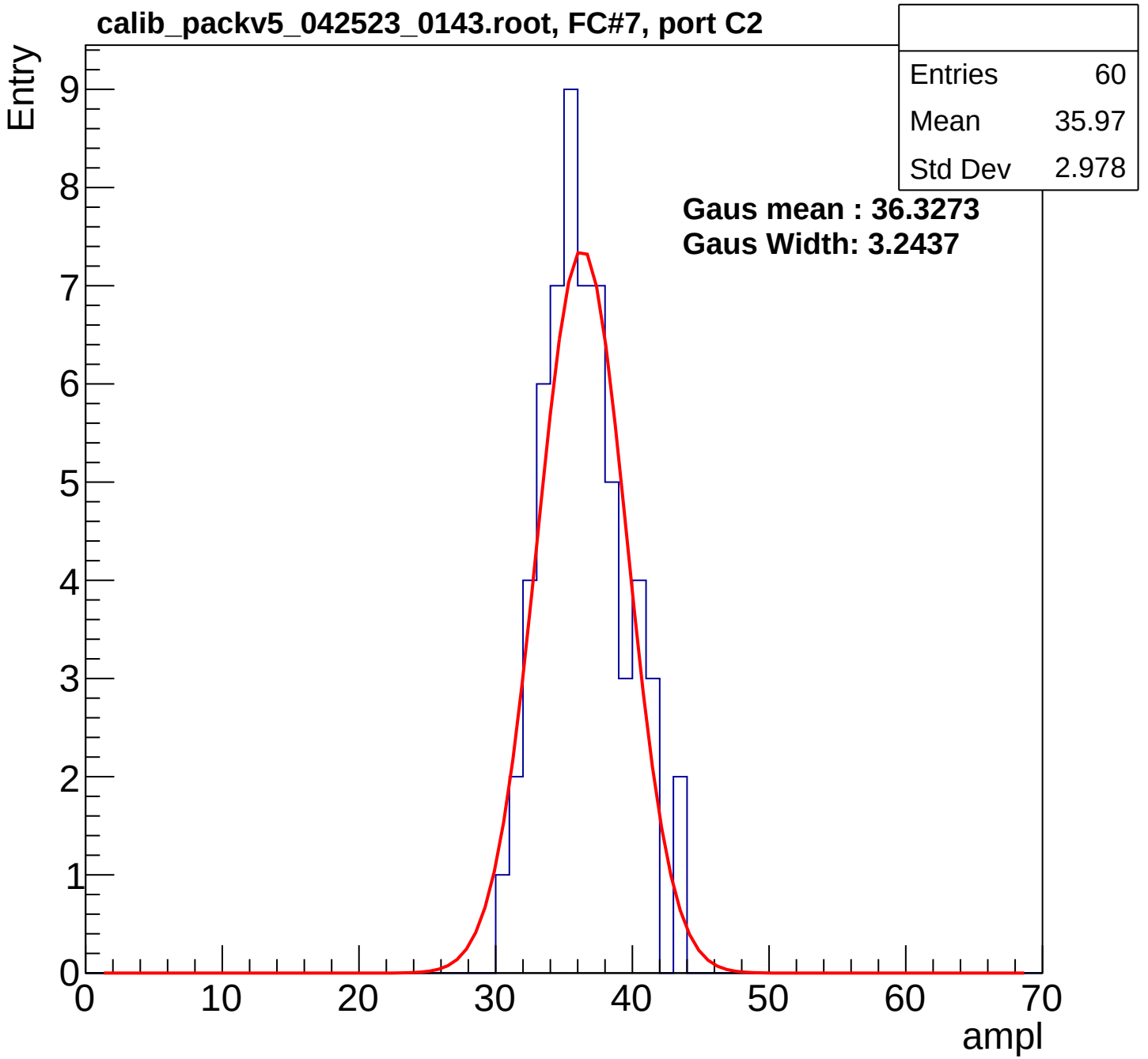

B1L103S, U8-ch20, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 54.44
Std Dev 3.336
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

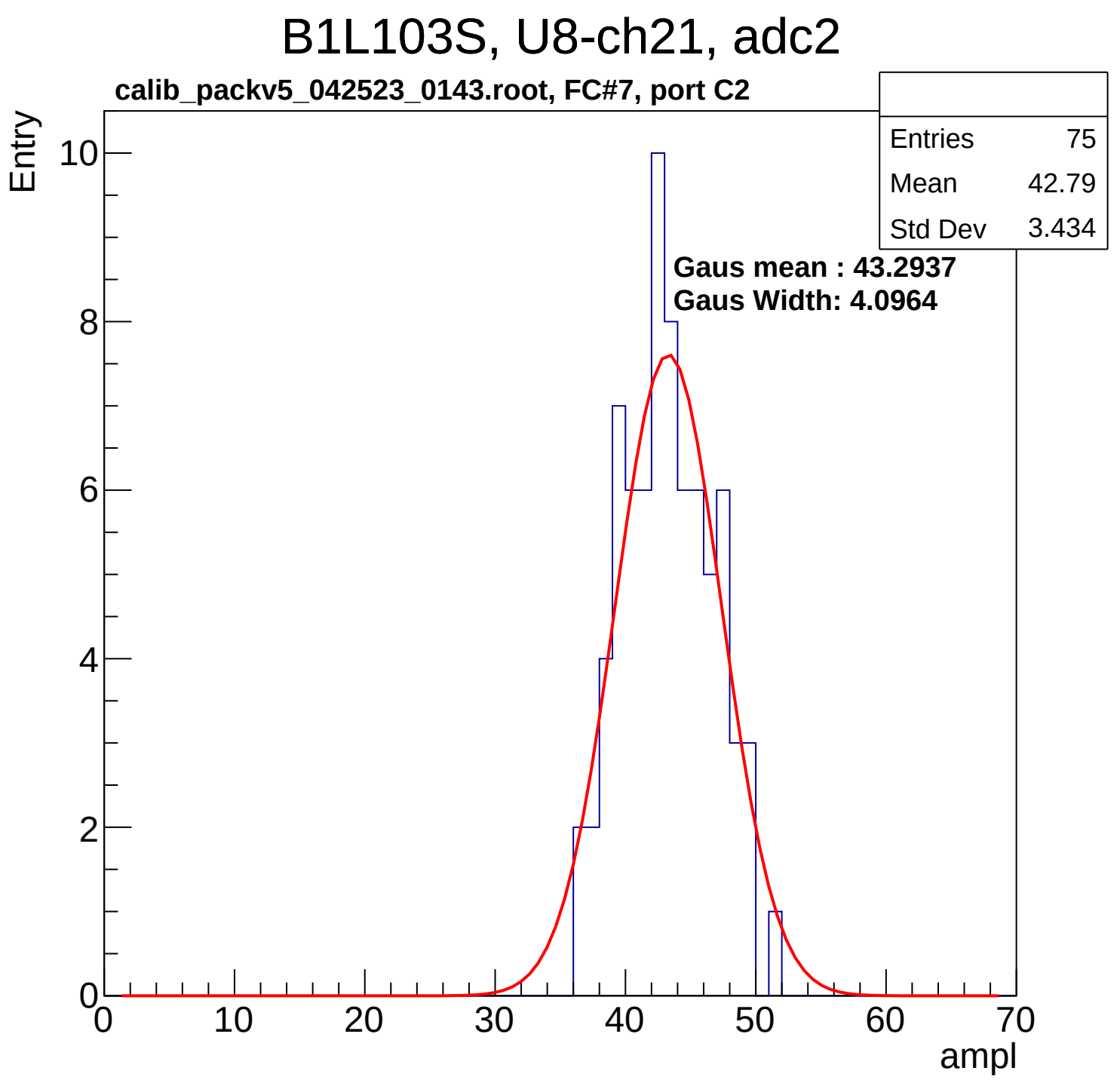

B1L103S, U8-ch20, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 59.1
Std Dev 2.606
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

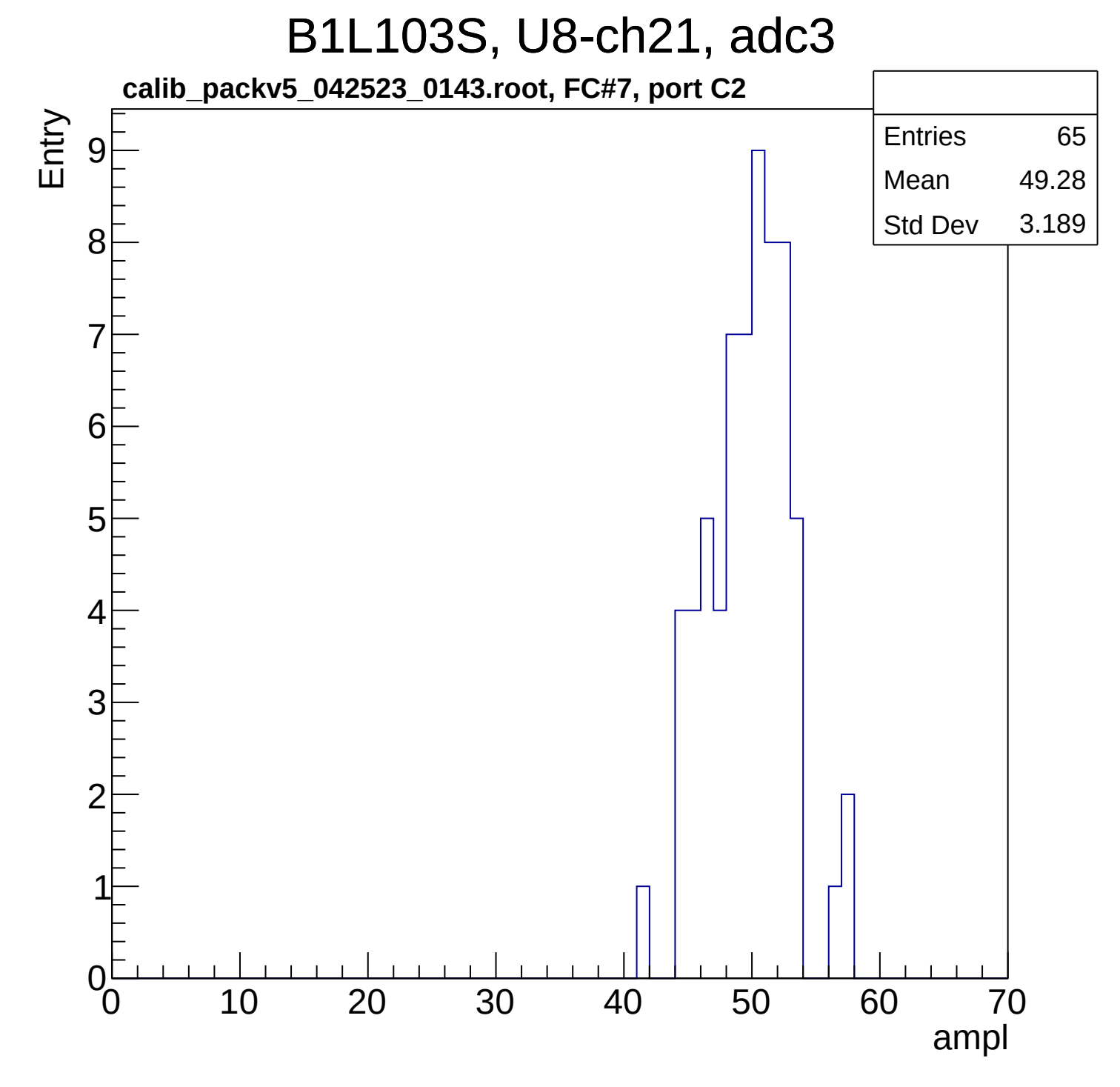

B1L103S, U8-ch20, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 10
Mean 55.1
Std Dev 18.43
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

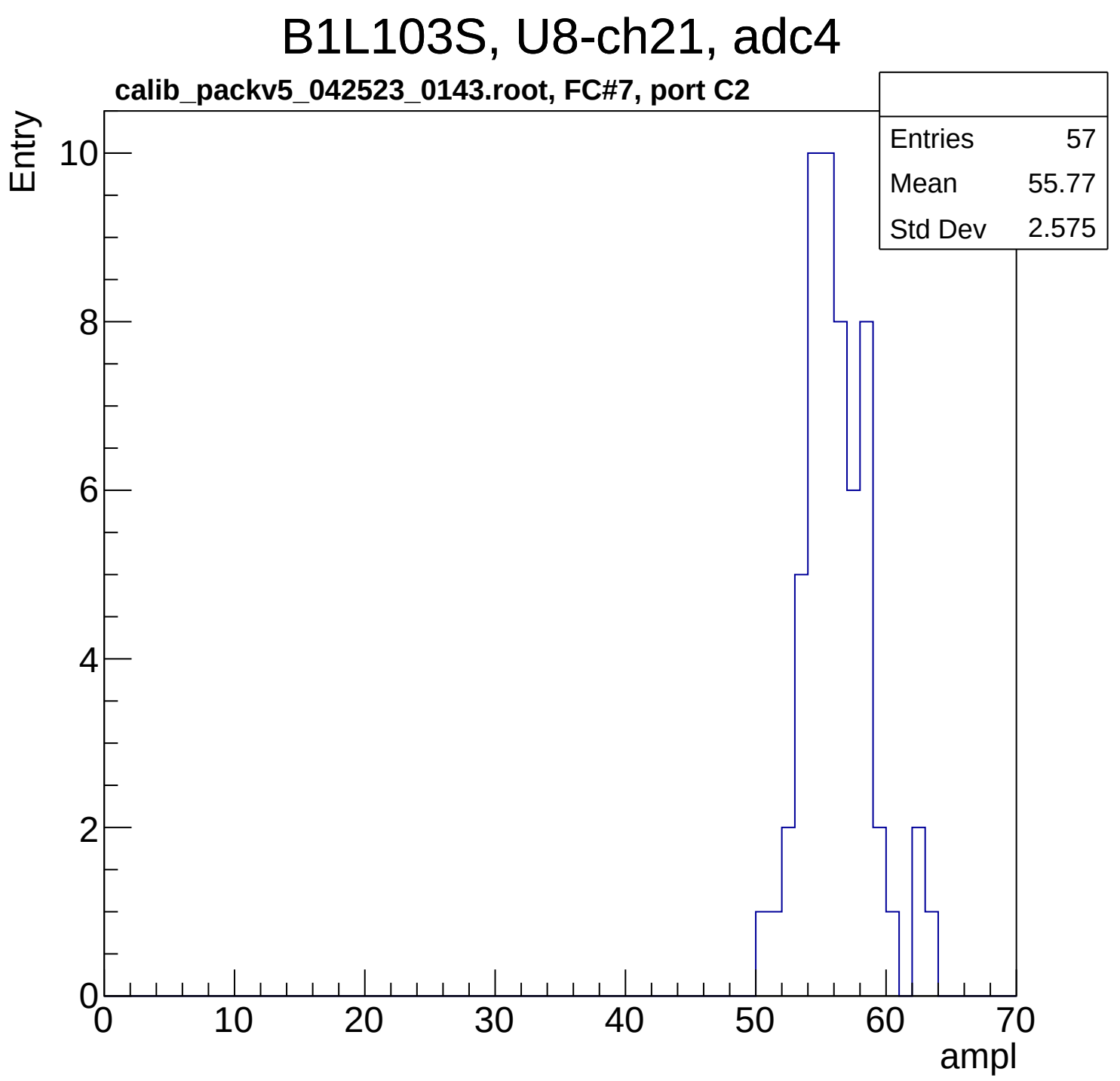

B1L103S, U8-ch20, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 8.5
Std Dev 8.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

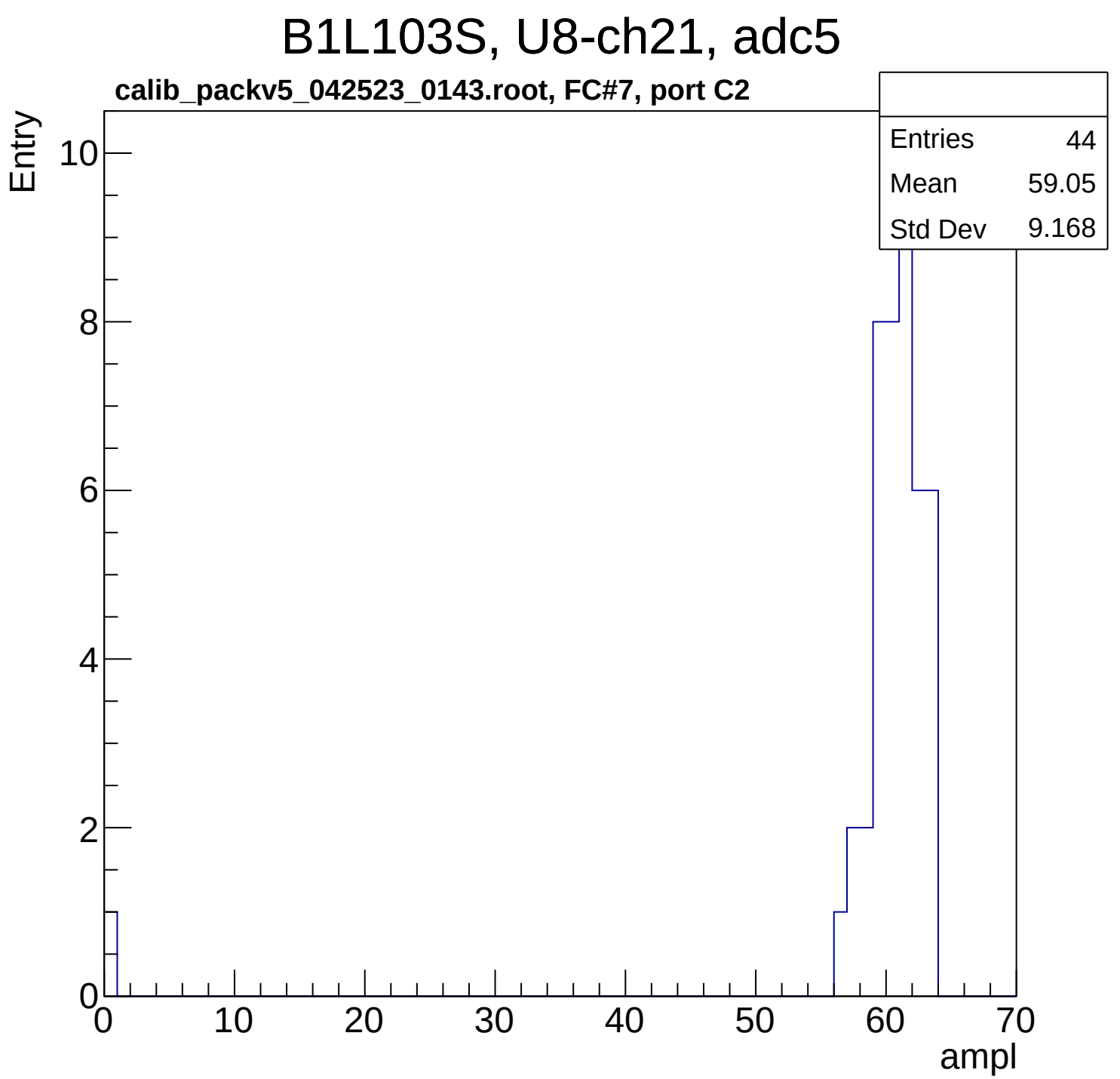

B1L103S, U8-ch21, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 28.97
Std Dev 3.491
Gaus mean : 29.7704
Gaus Width: 3.1843
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

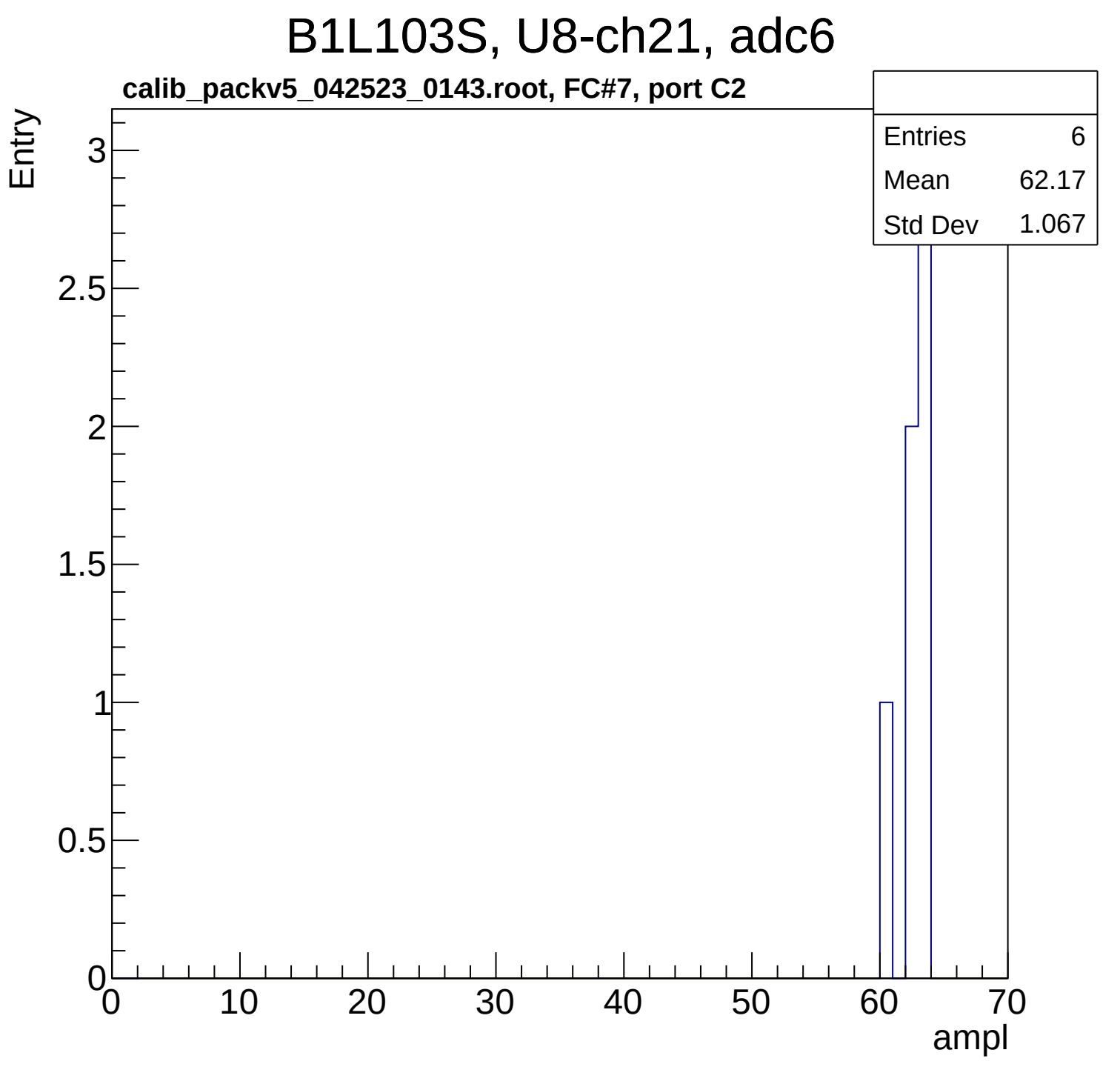

B1L103S, U8-ch21, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 35.97
Std Dev 2.978
Gaus mean : 36.3273
Gaus Width: 3.2437
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

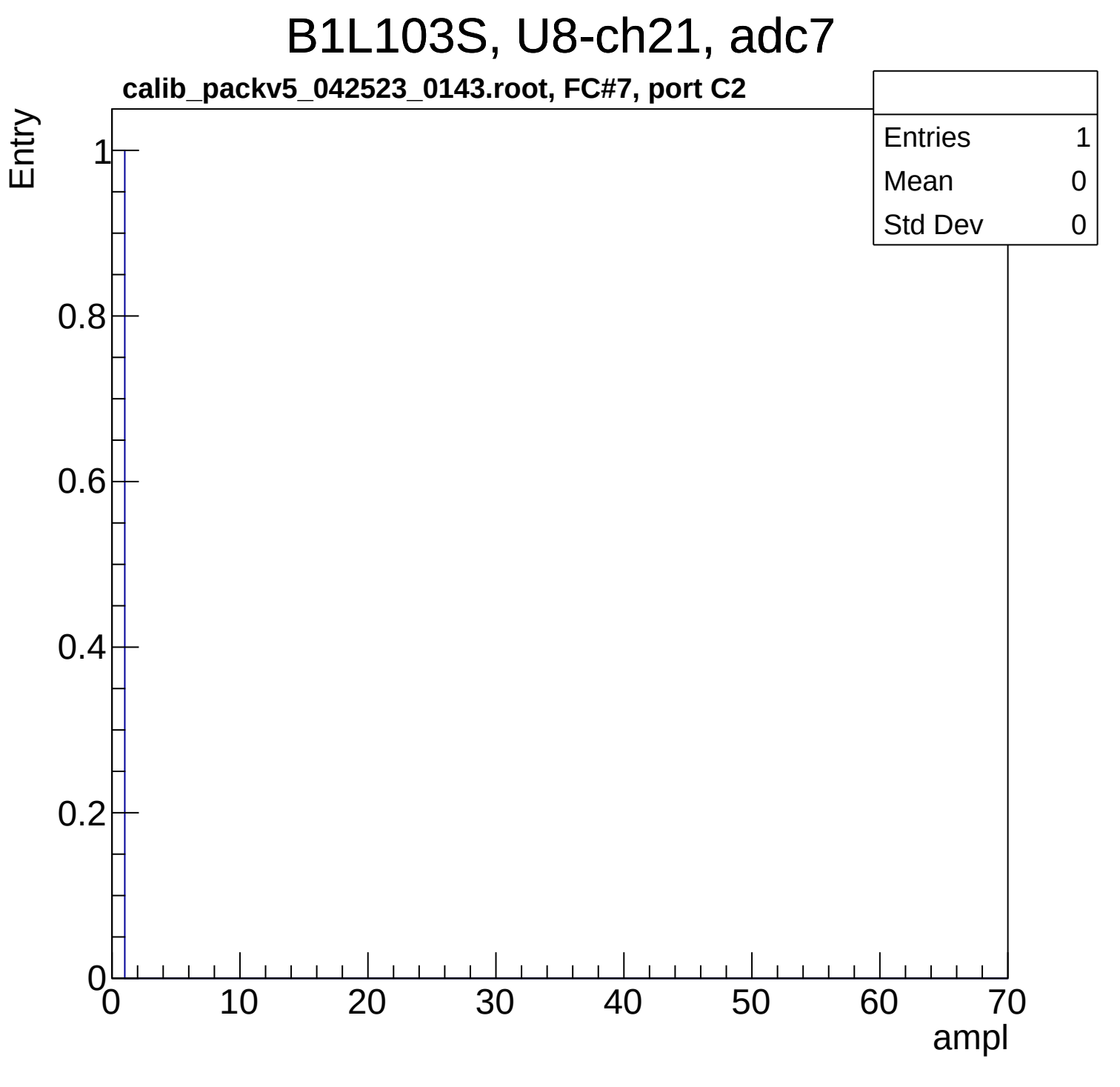

B1L103S, U8-ch21, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 42.79
Std Dev 3.434
Gaus mean : 43.2937
Gaus Width: 4.0964
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

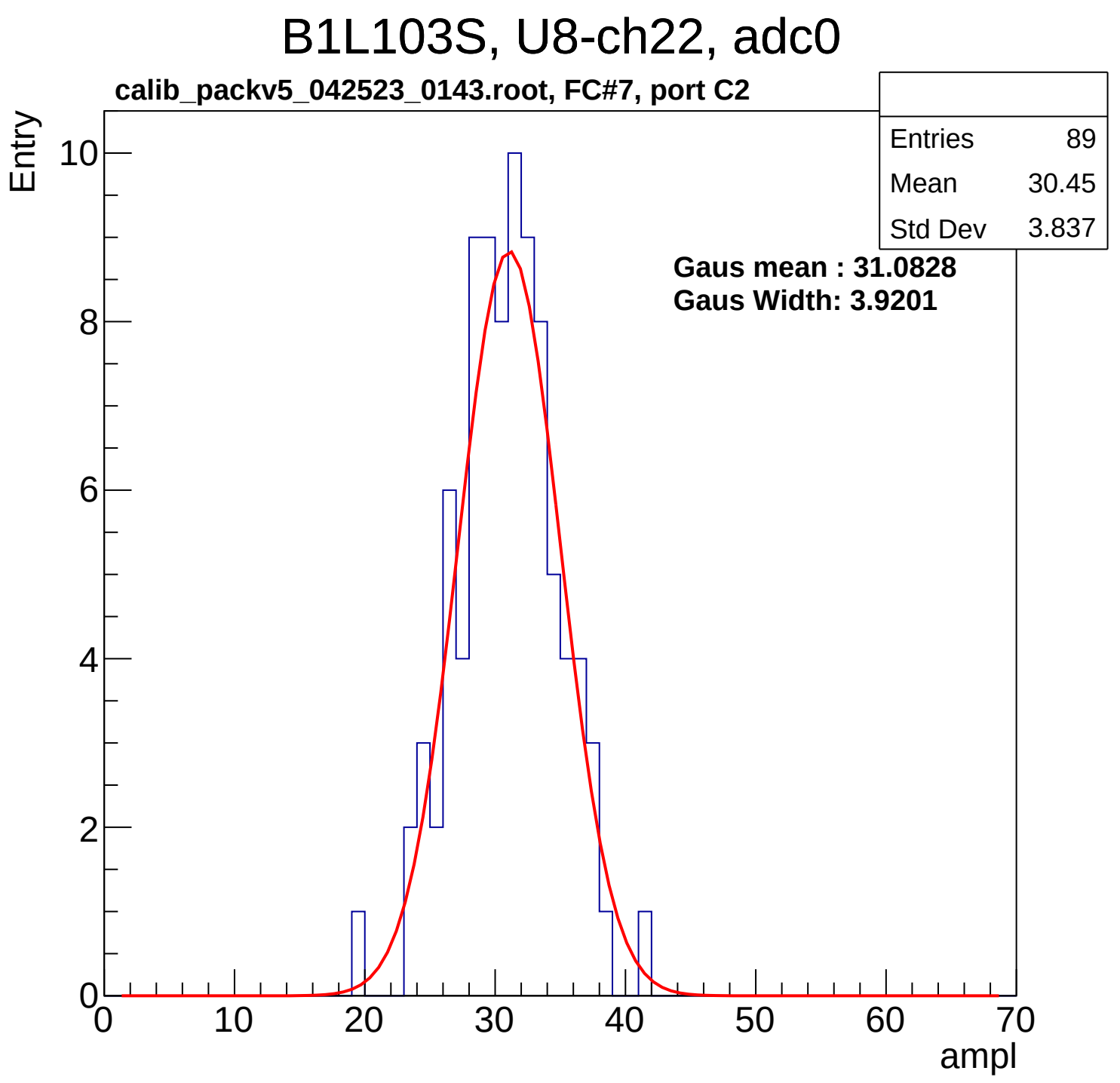

B1L103S, U8-ch21, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 49.28
Std Dev 3.189
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

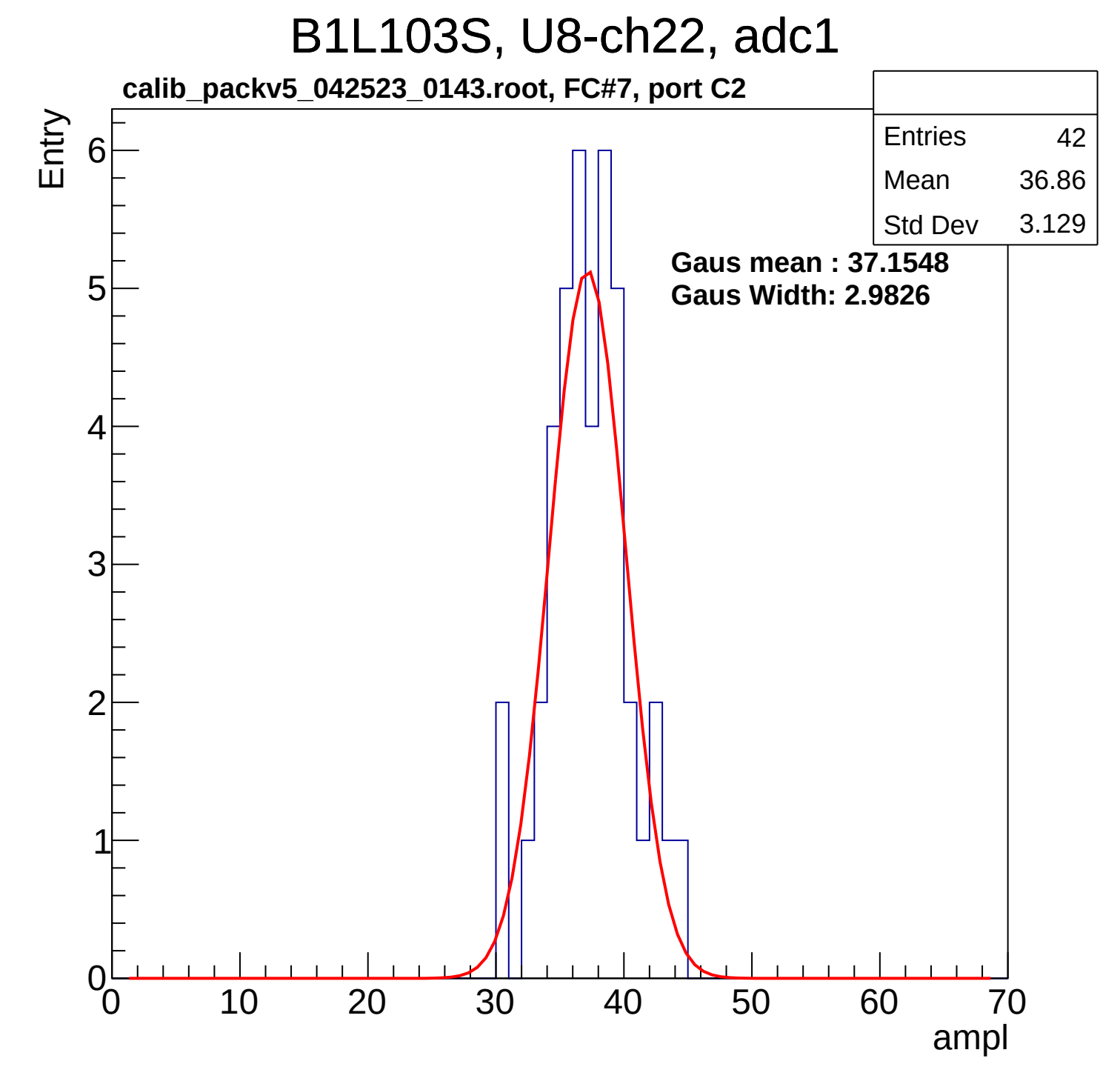

B1L103S, U8-ch21, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 55.77
Std Dev 2.575
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

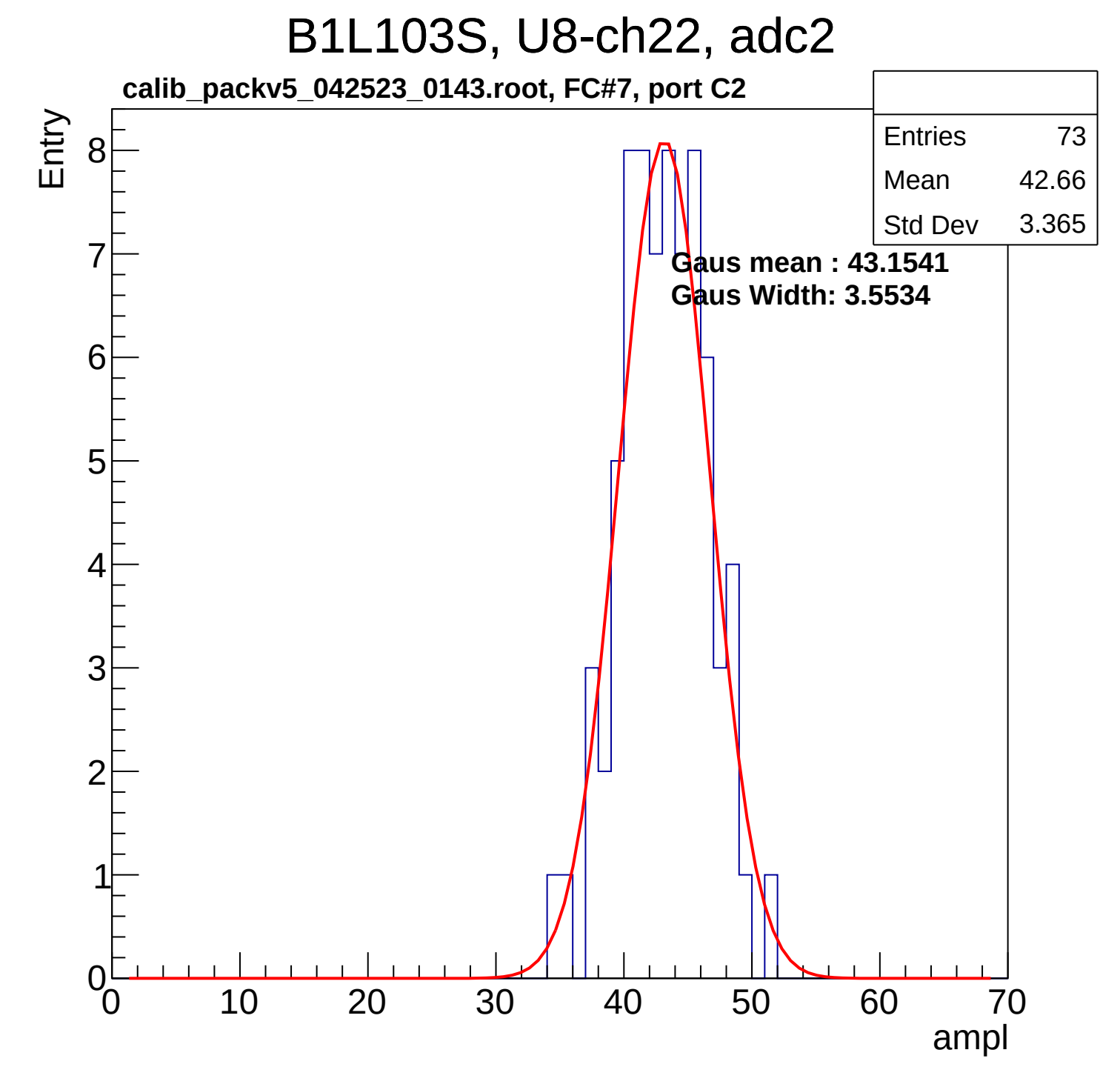

B1L103S, U8-ch21, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 44
Mean 59.05
Std Dev 9.168
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

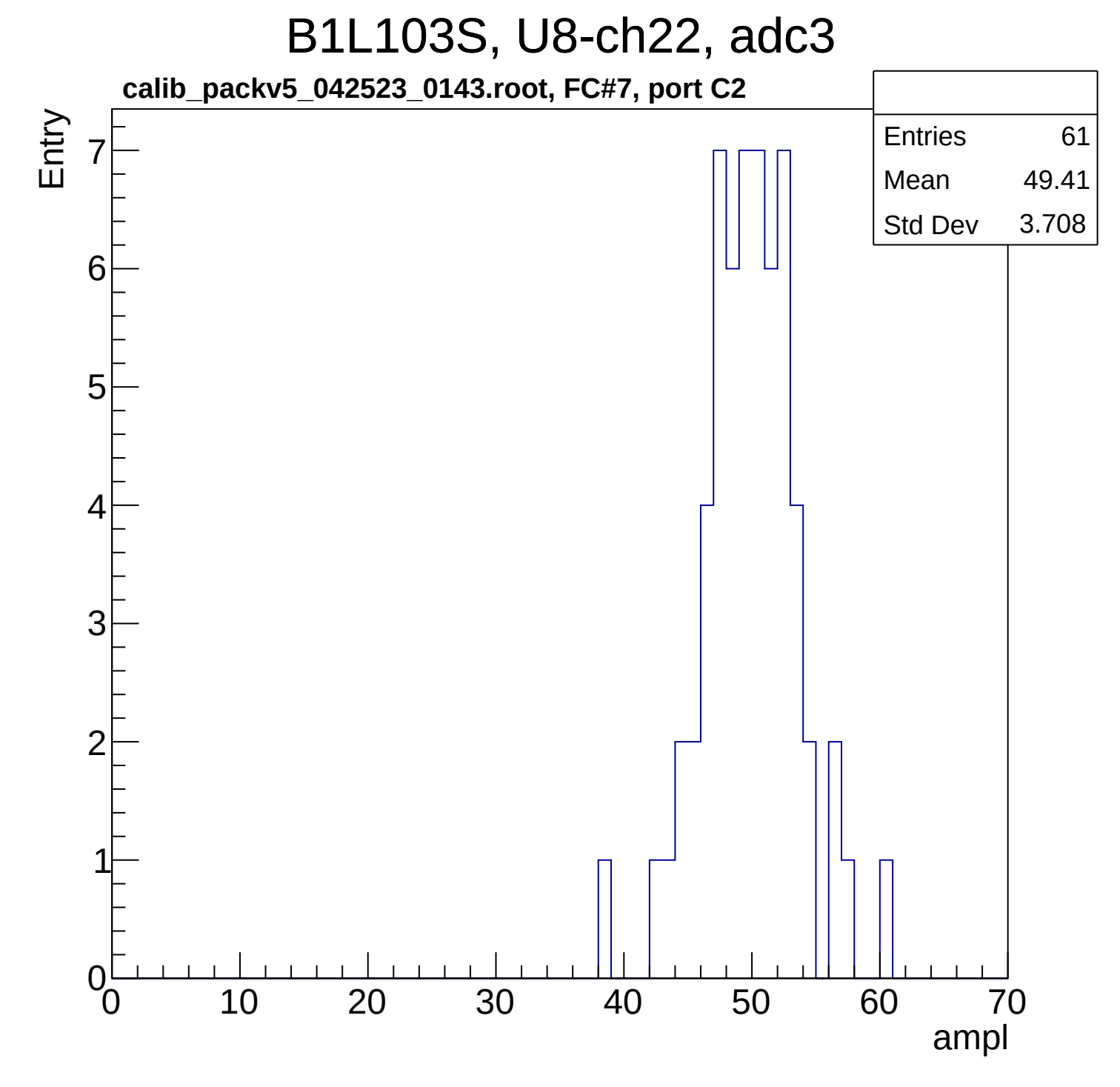

B1L103S, U8-ch21, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 62.17
Std Dev 1.067
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

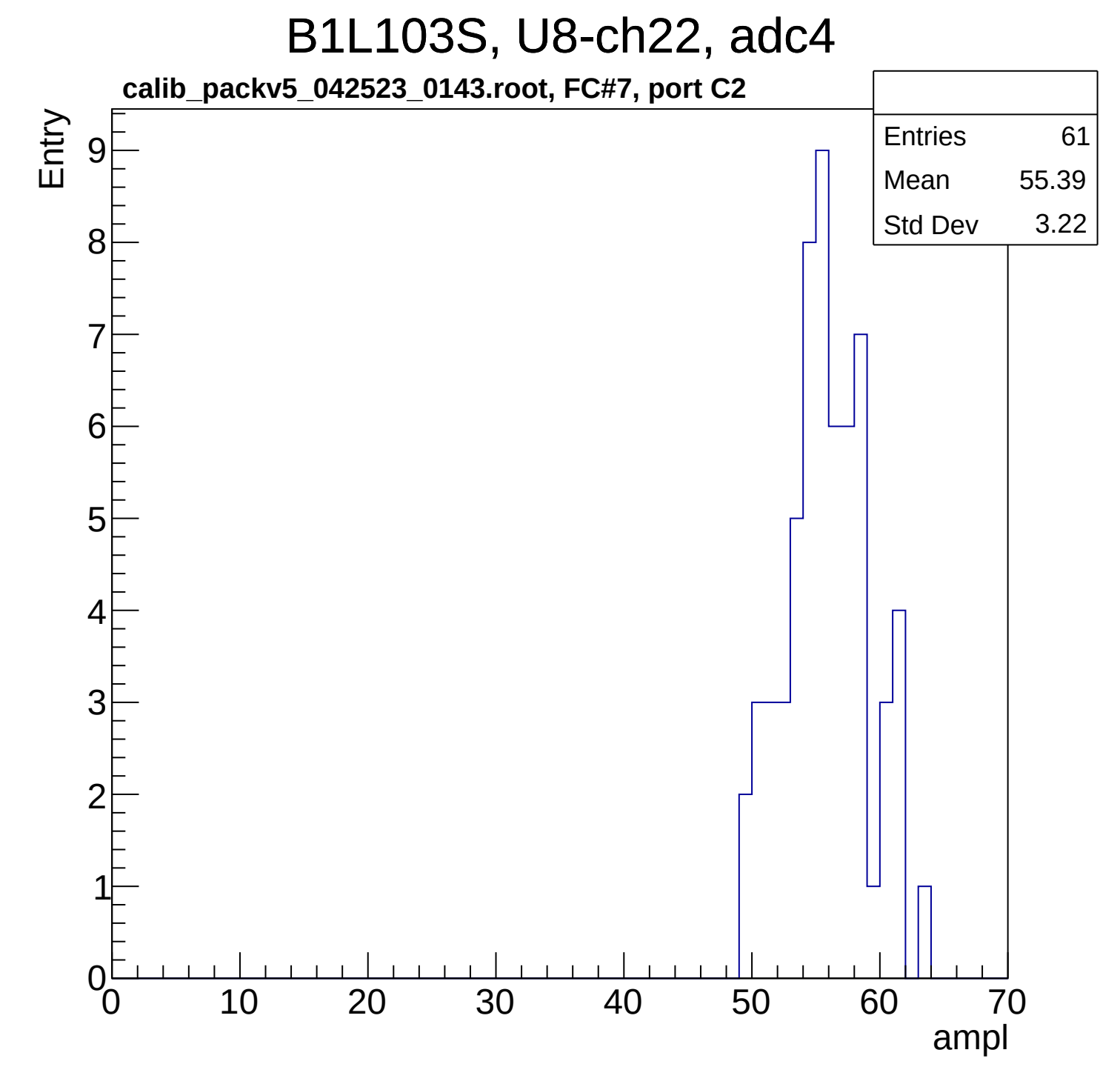

B1L103S, U8-ch21, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

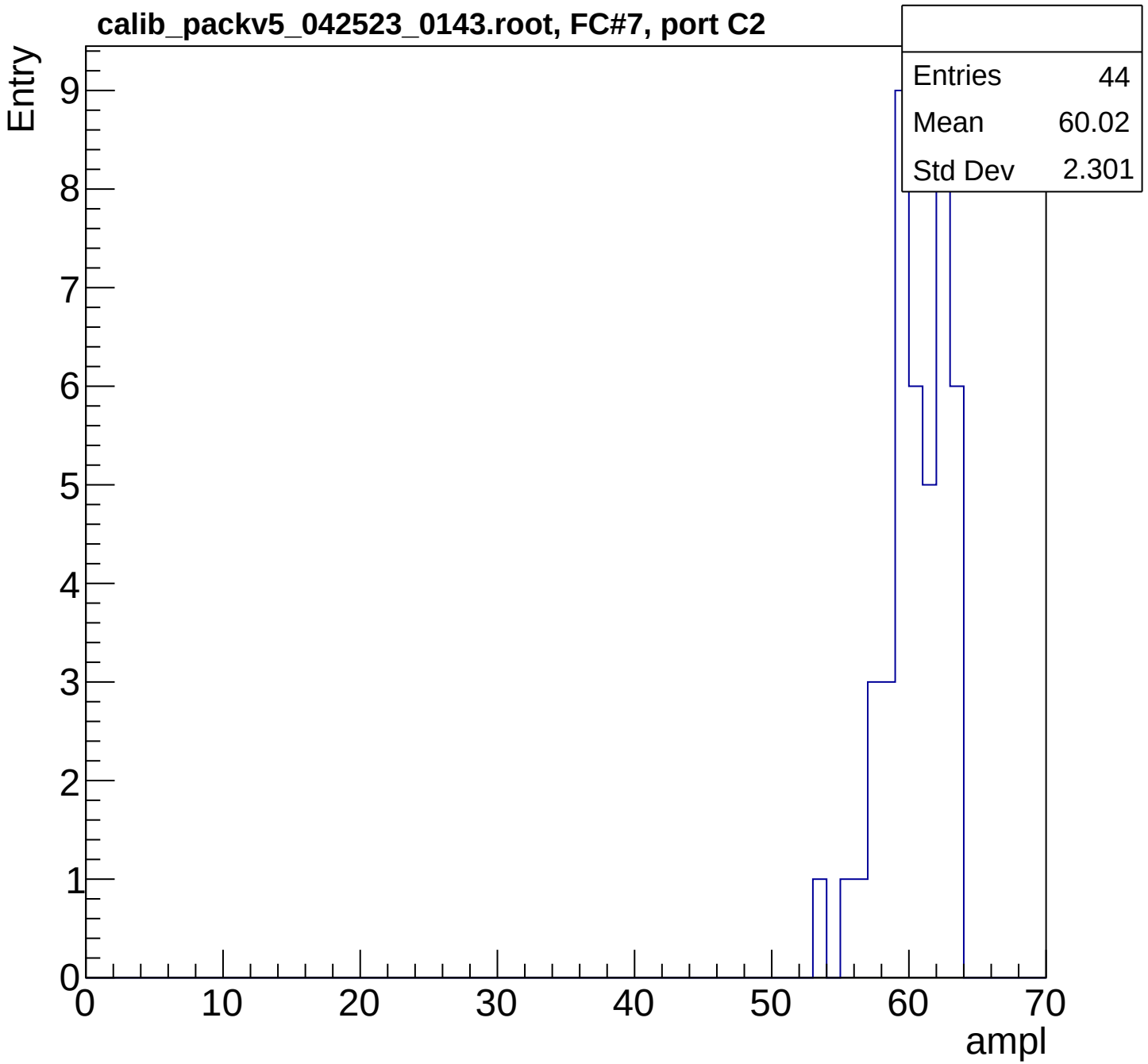

B1L103S, U8-ch22, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 89
Mean 30.45
Std Dev 3.837
Gaus mean : 31.0828
Gaus Width: 3.9201
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

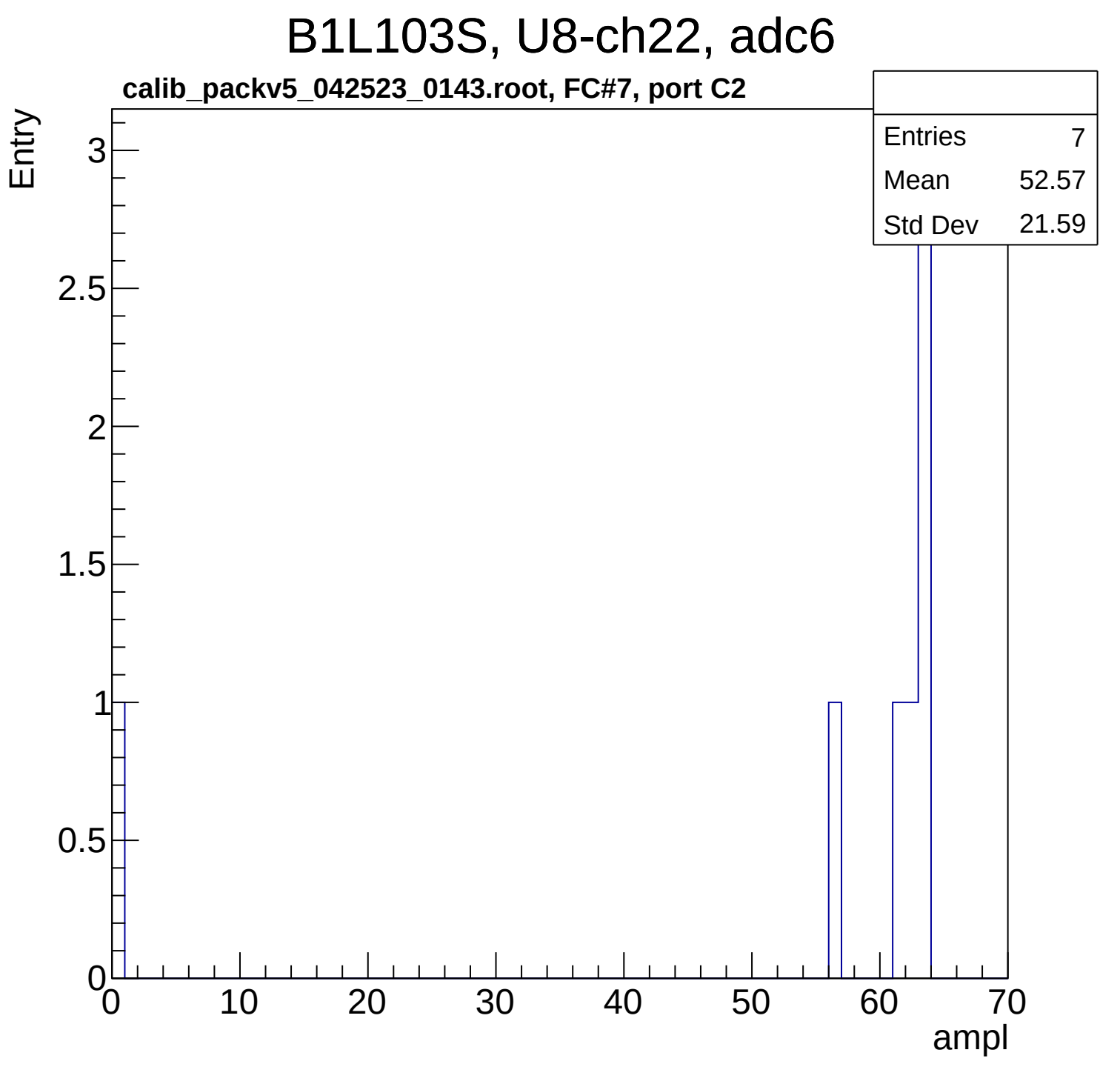

B1L103S, U8-ch22, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 42
Mean 36.86
Std Dev 3.129
Gaus mean : 37.1548
Gaus Width: 2.9826
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

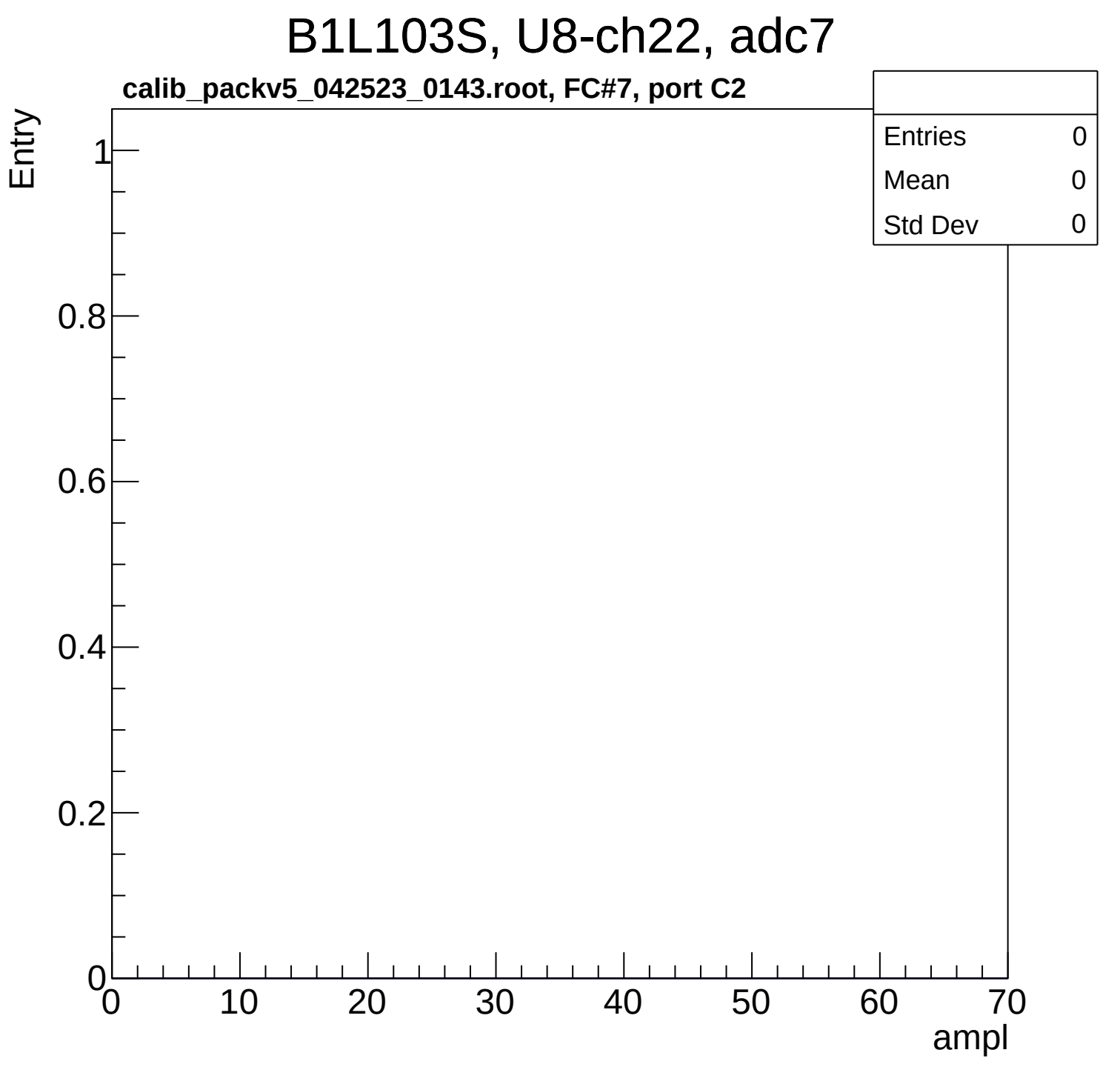

B1L103S, U8-ch22, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 42.66
Std Dev 3.365
Gaus mean : 43.1541
Gaus Width: 3.5534
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

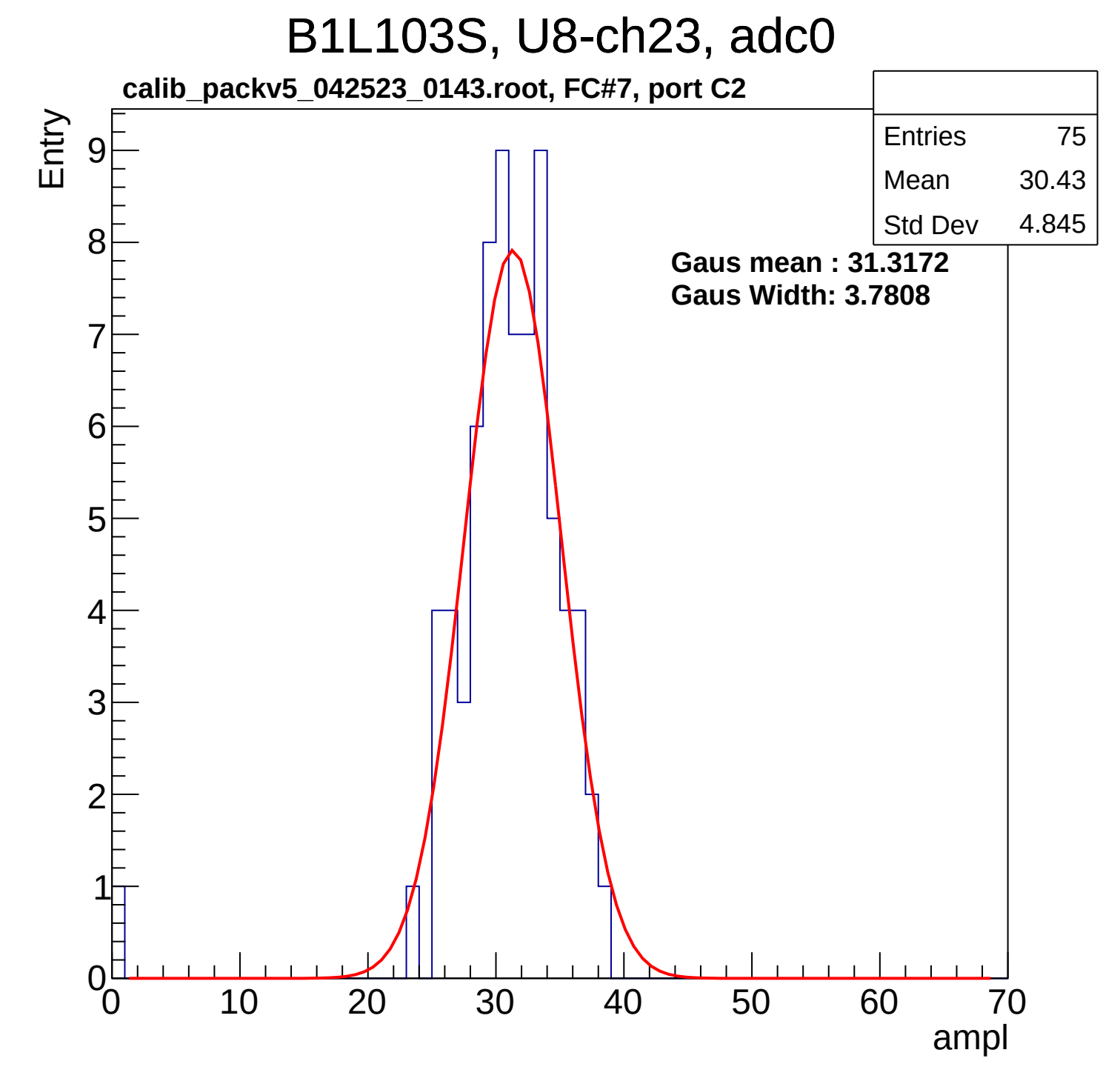

B1L103S, U8-ch22, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 49.41
Std Dev 3.708
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

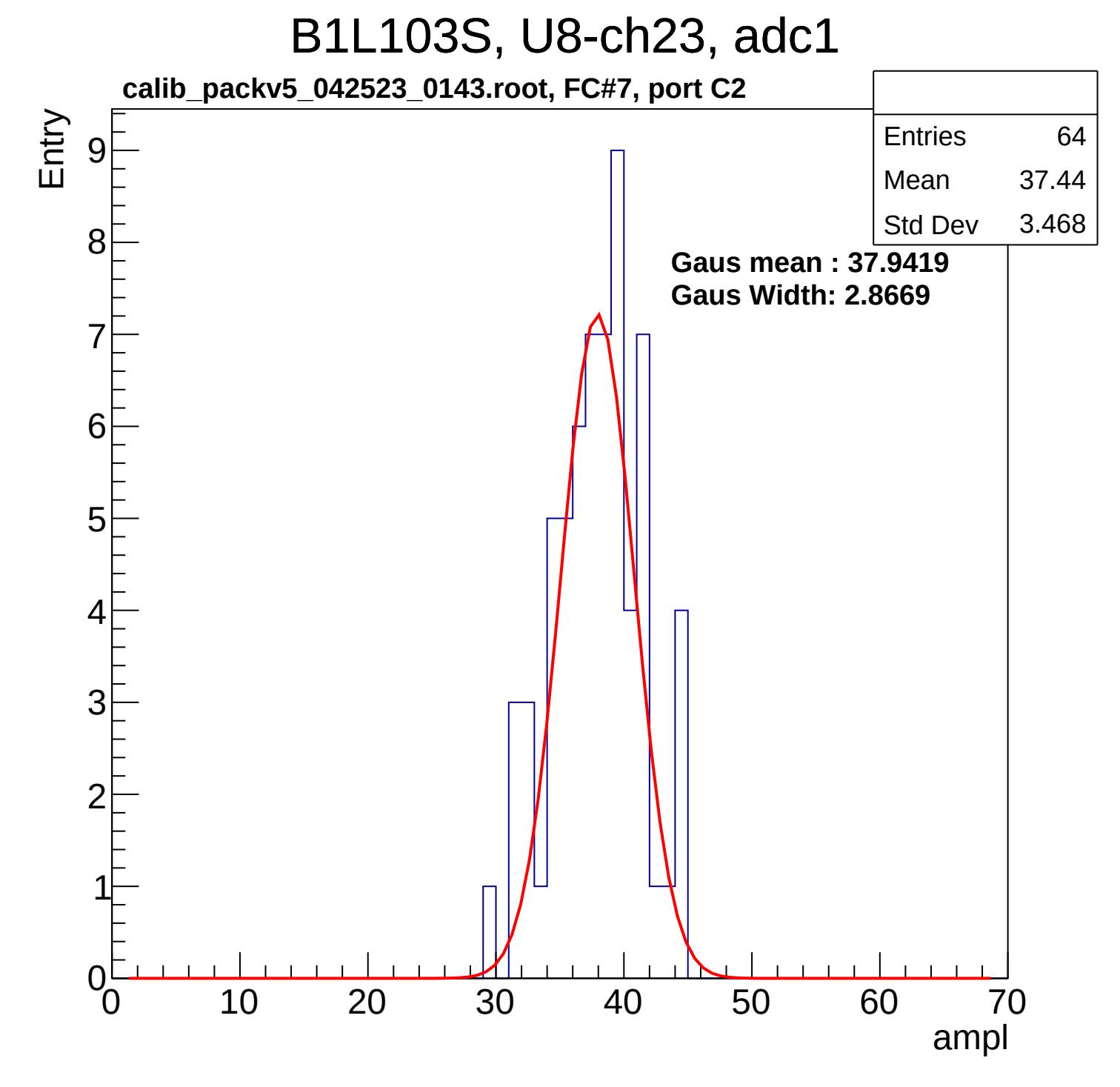

B1L103S, U8-ch22, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 55.39
Std Dev 3.22
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

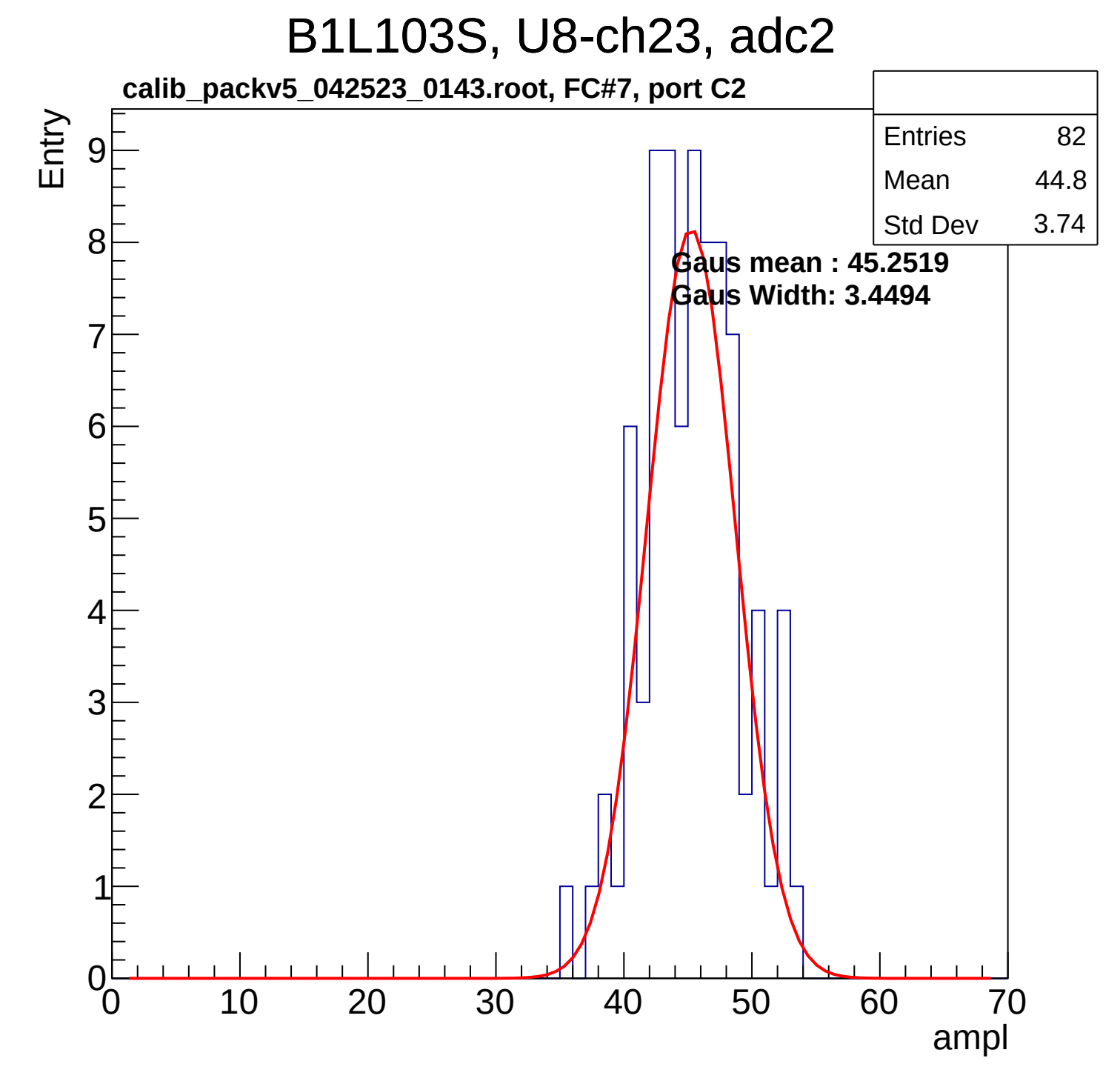

B1L103S, U8-ch22, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 44
Mean 60.02
Std Dev 2.301
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

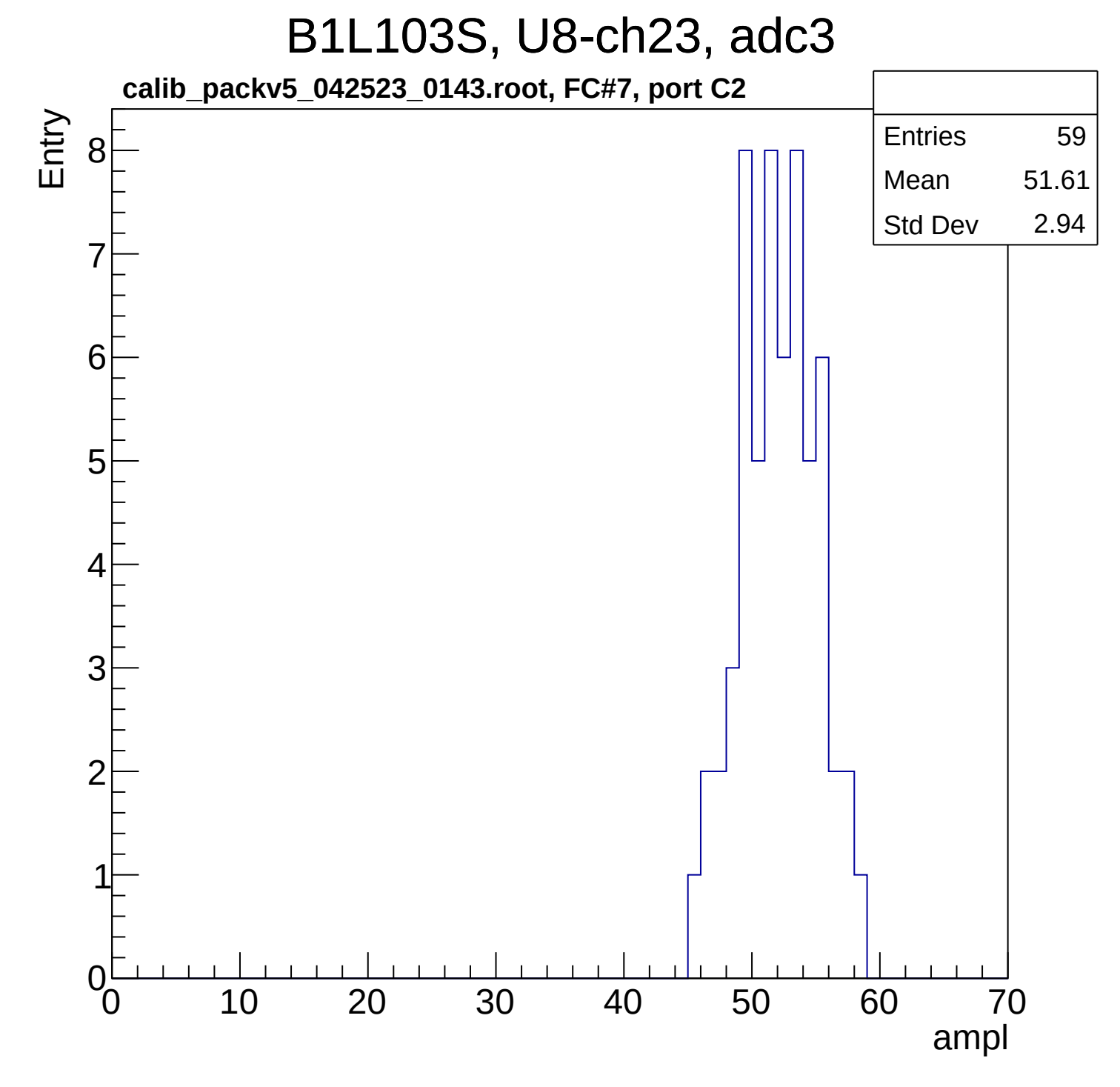

B1L103S, U8-ch22, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 7
Mean 52.57
Std Dev 21.59
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

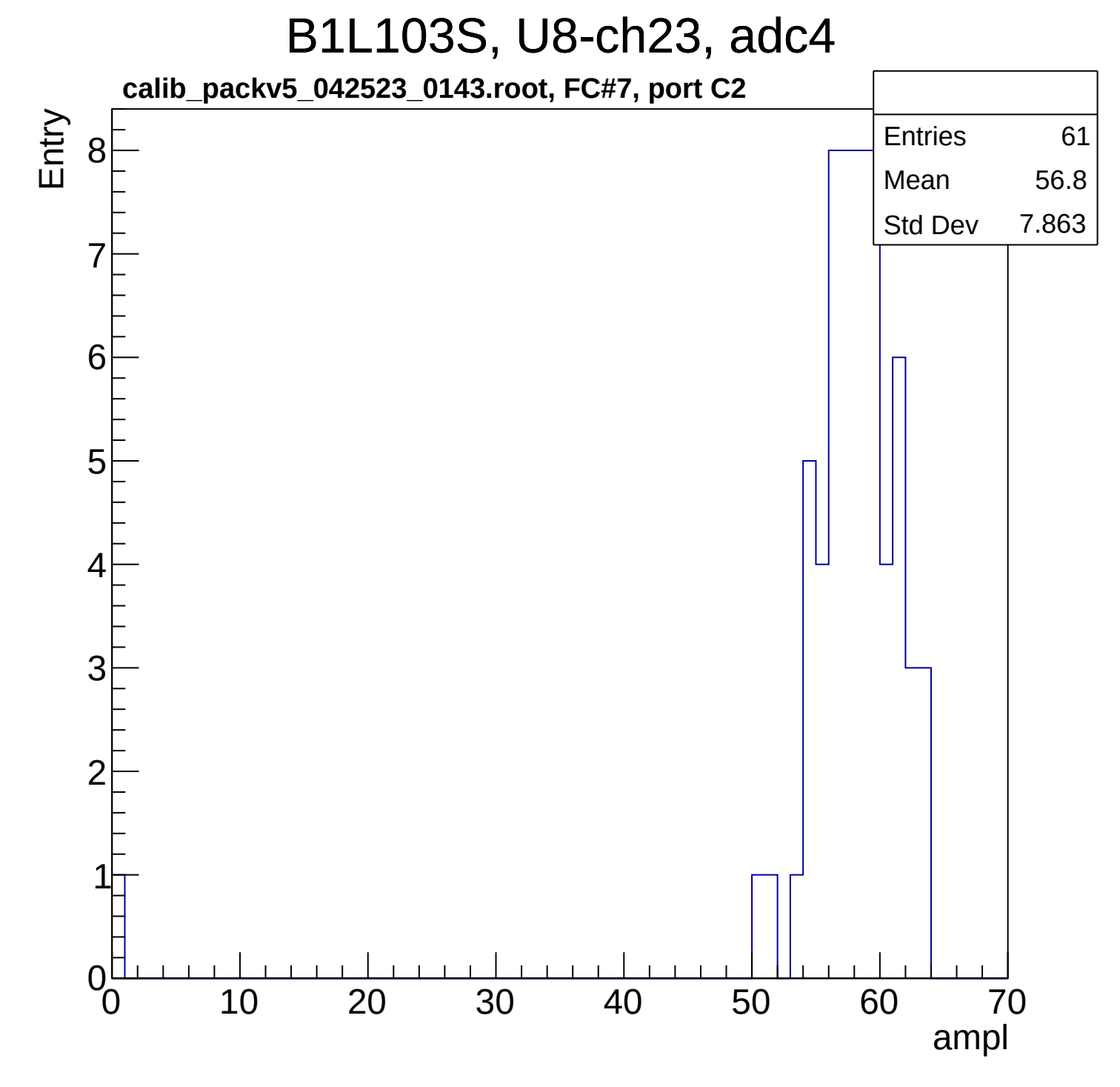

B1L103S, U8-ch22, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

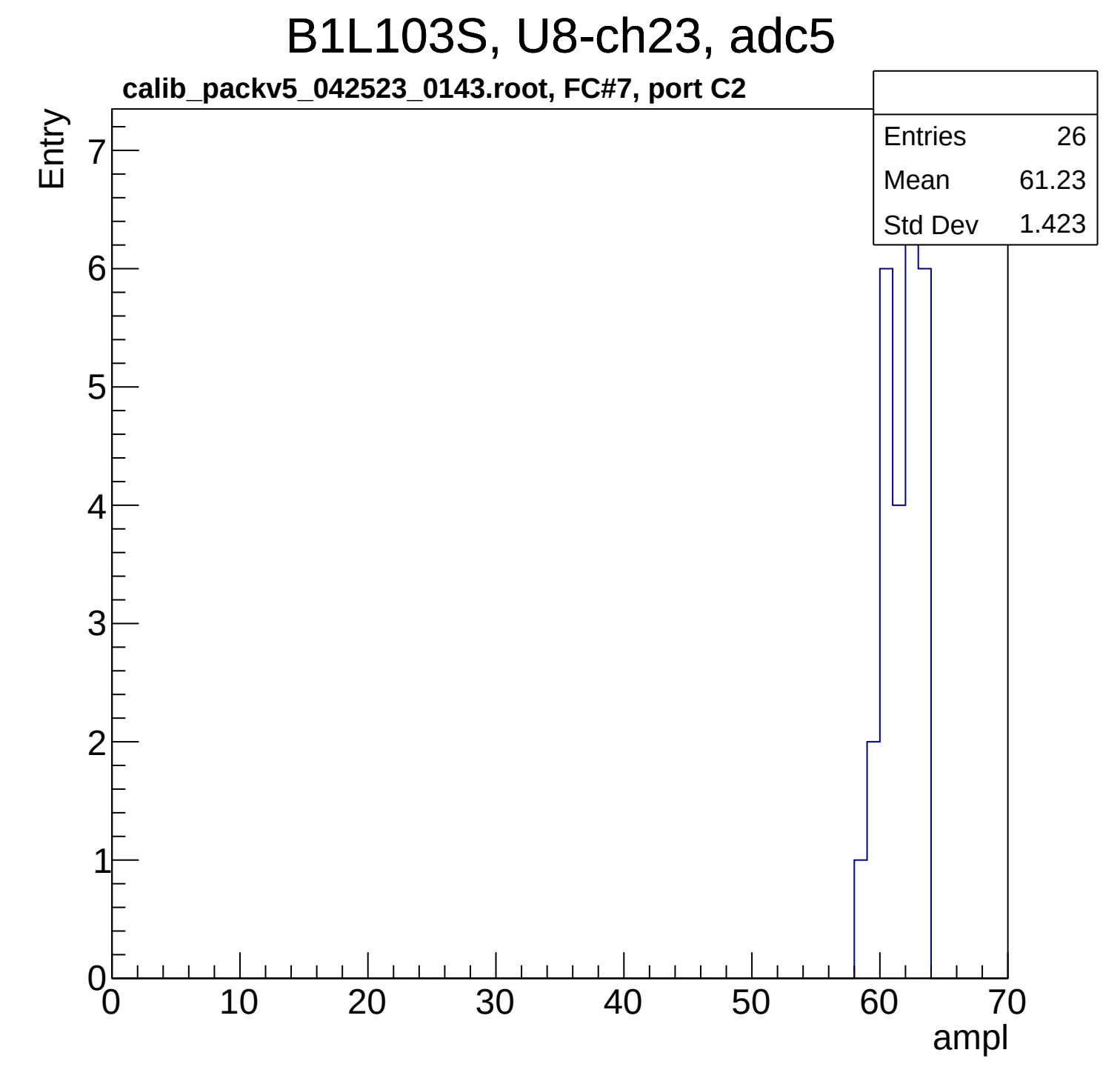

B1L103S, U8-ch23, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 30.43
Std Dev 4.845
Gaus mean : 31.3172
Gaus Width: 3.7808
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

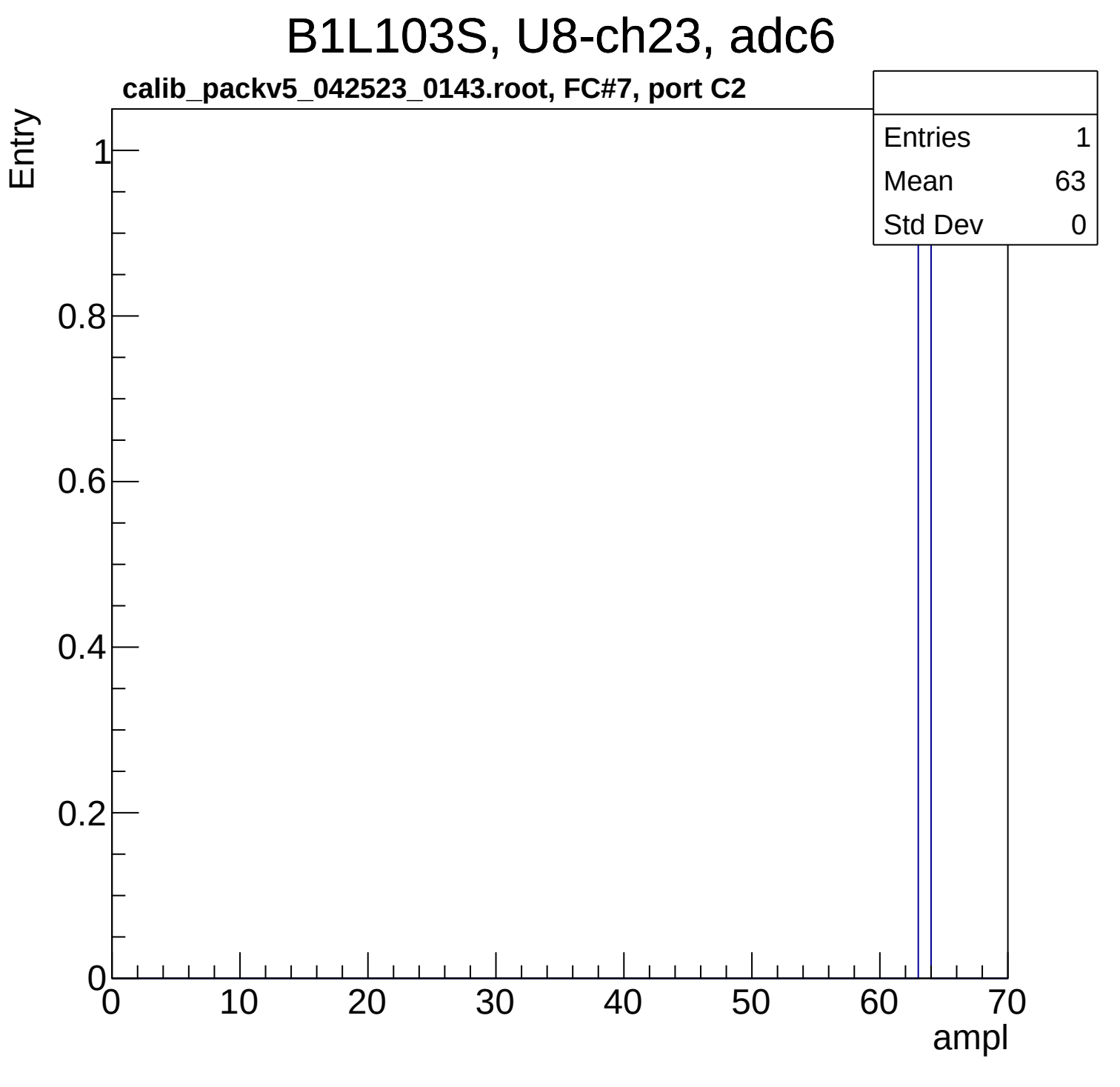

B1L103S, U8-ch23, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 37.44
Std Dev 3.468
Gaus mean : 37.9419
Gaus Width: 2.8669
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

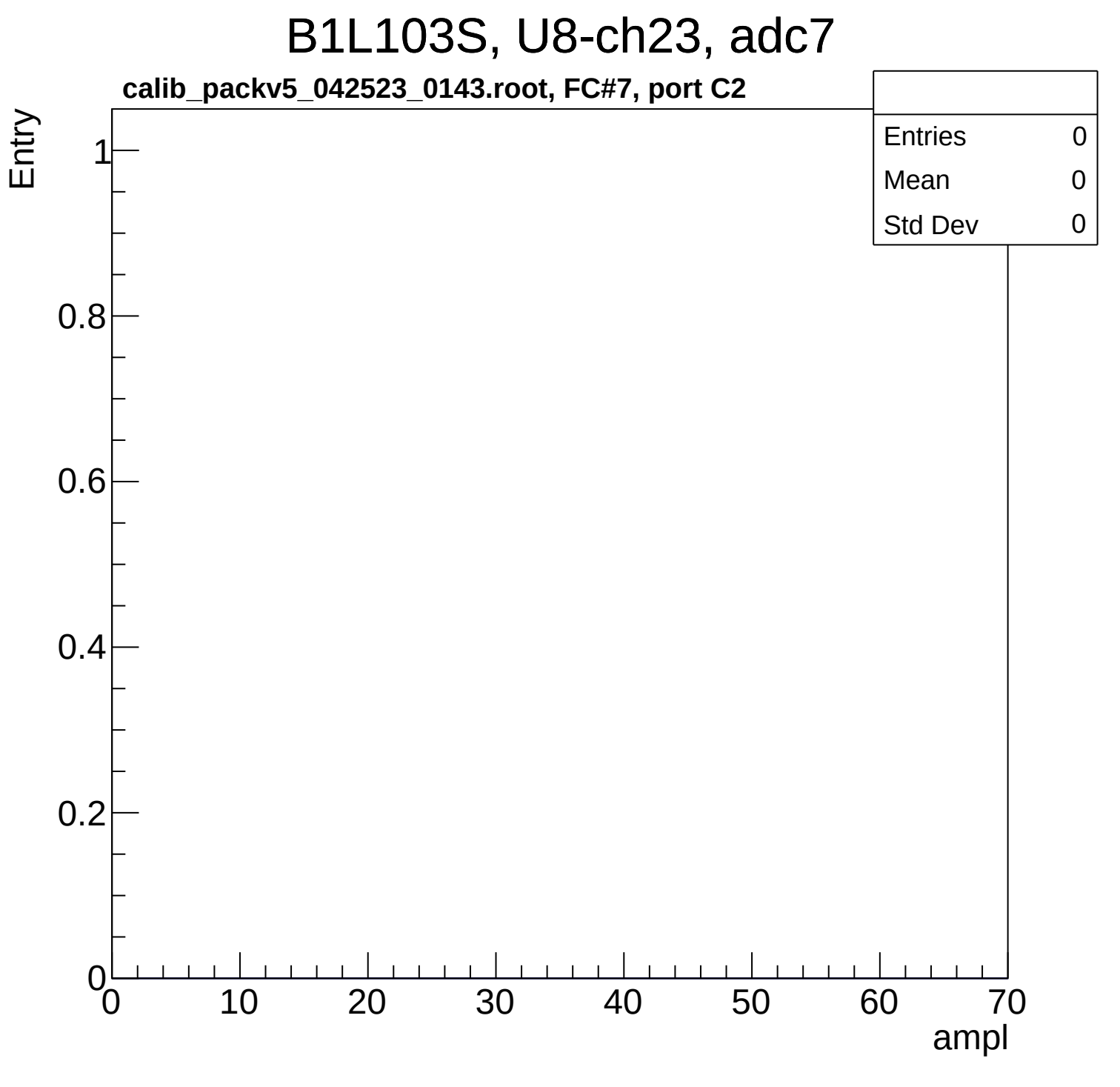

B1L103S, U8-ch23, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 82
Mean 44.8
Std Dev 3.74
Gaus mean : 45.2519
Gaus Width: 3.4494
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

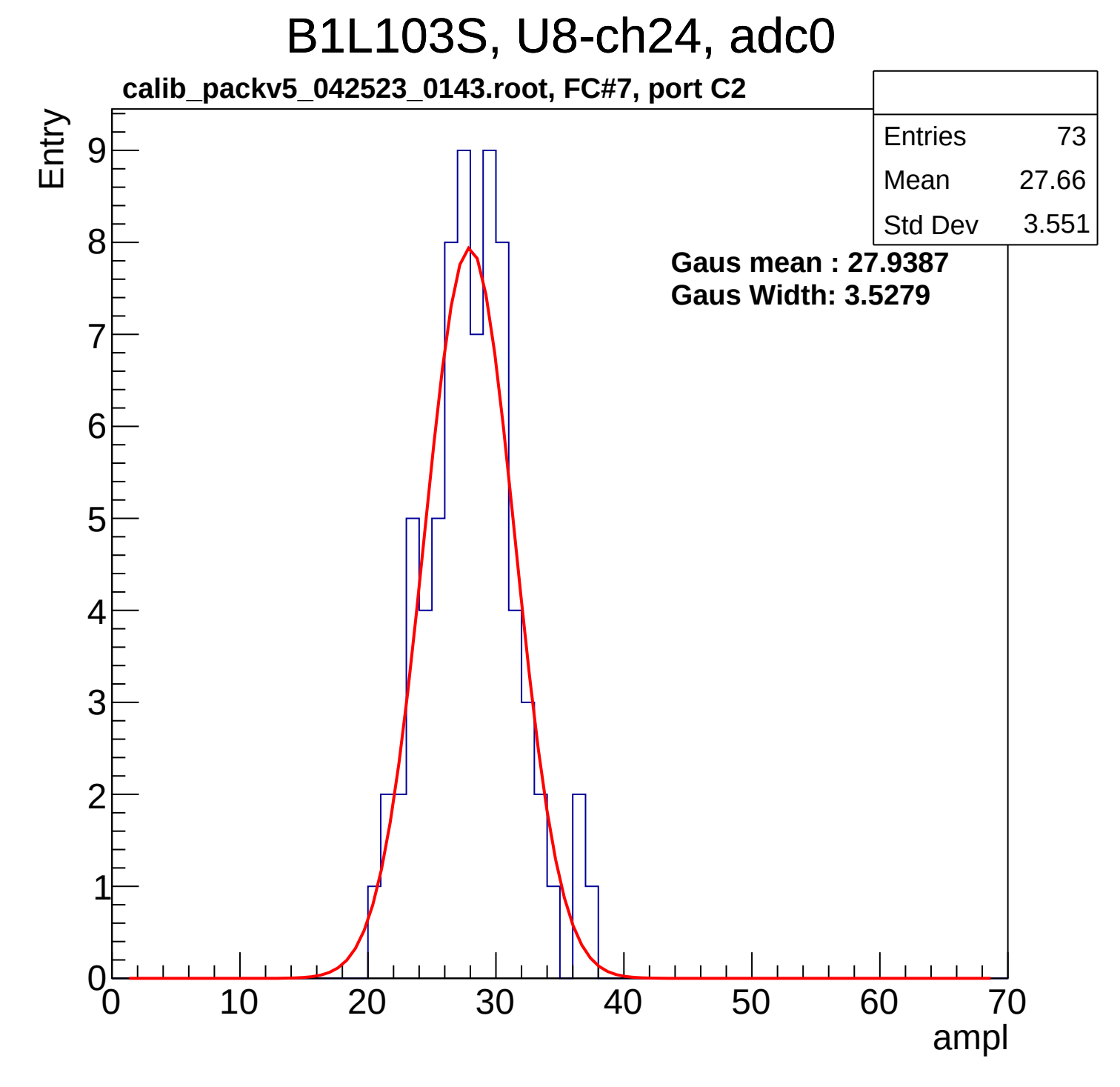

B1L103S, U8-ch23, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 51.61
Std Dev 2.94
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

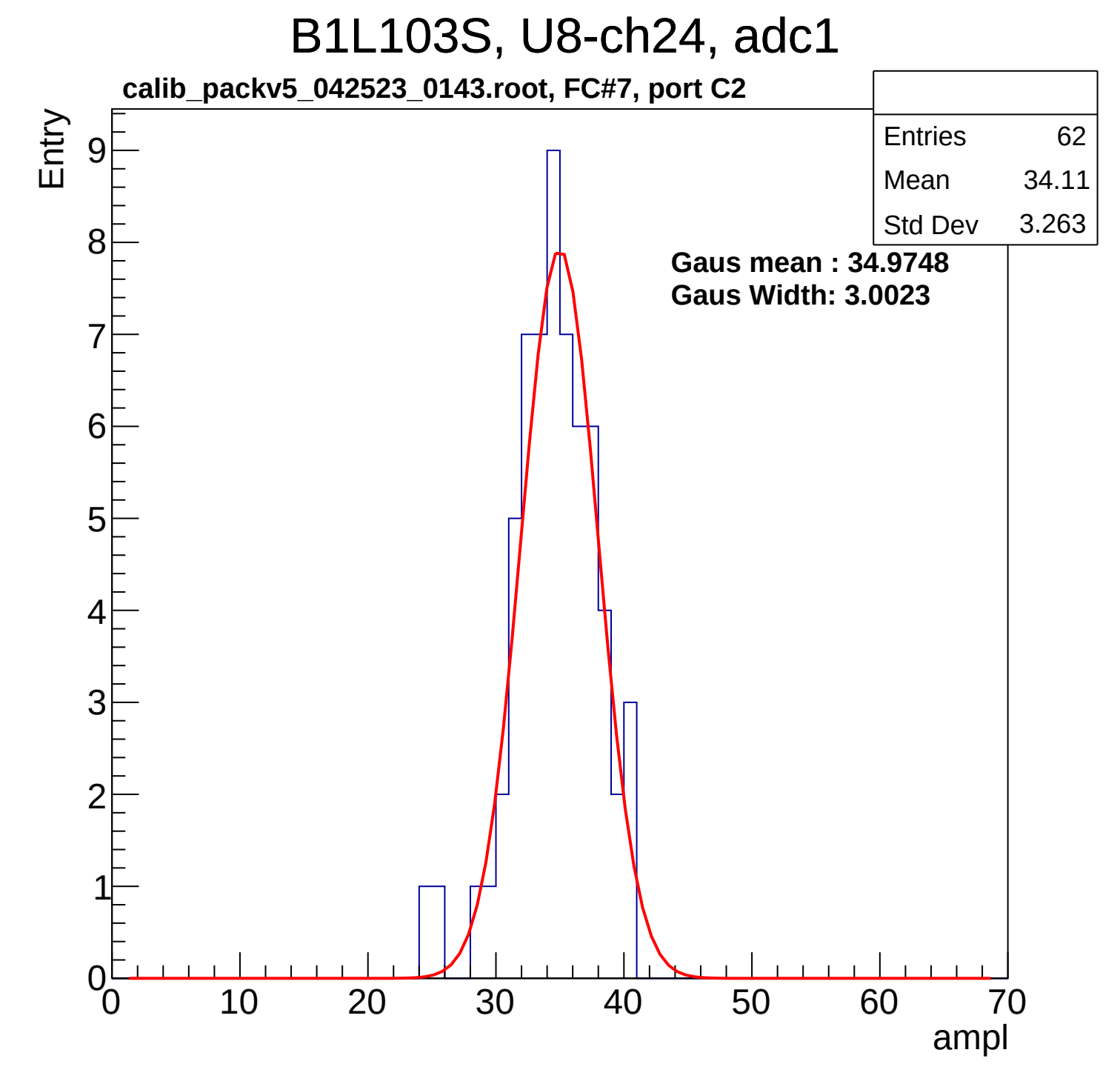

B1L103S, U8-ch23, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 56.8
Std Dev 7.863
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

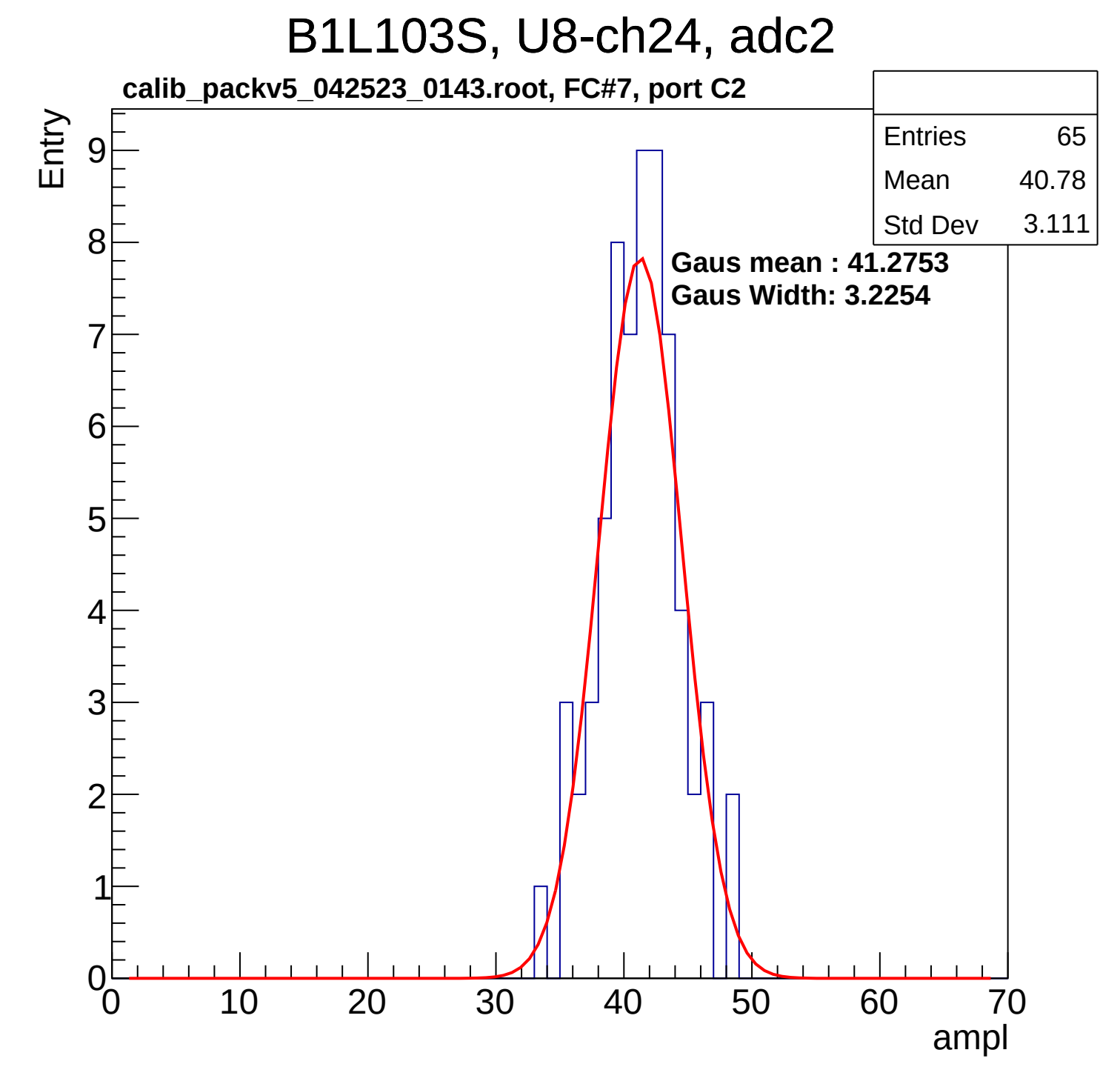

B1L103S, U8-ch23, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 26
Mean 61.23
Std Dev 1.423
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

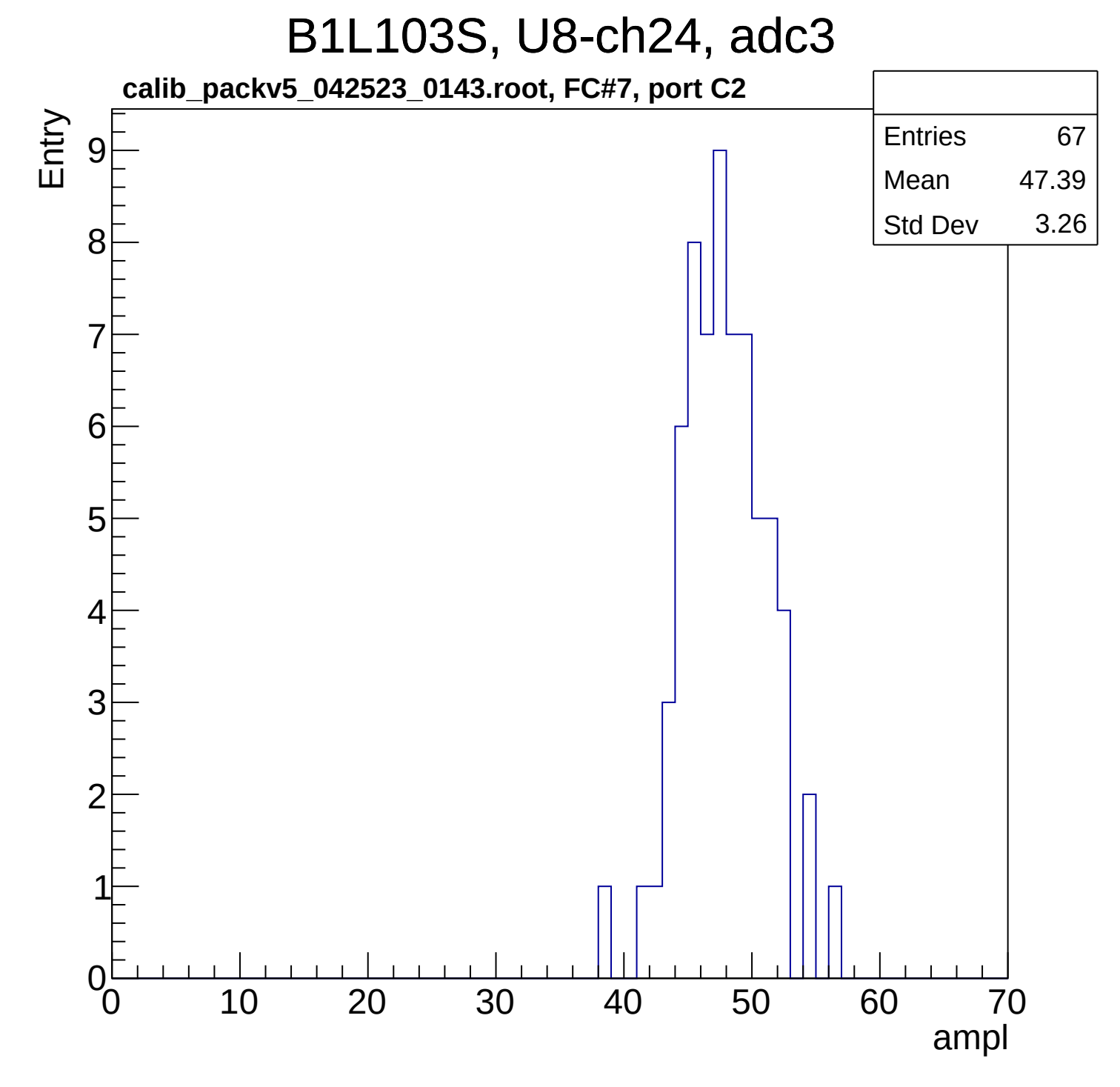

B1L103S, U8-ch23, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

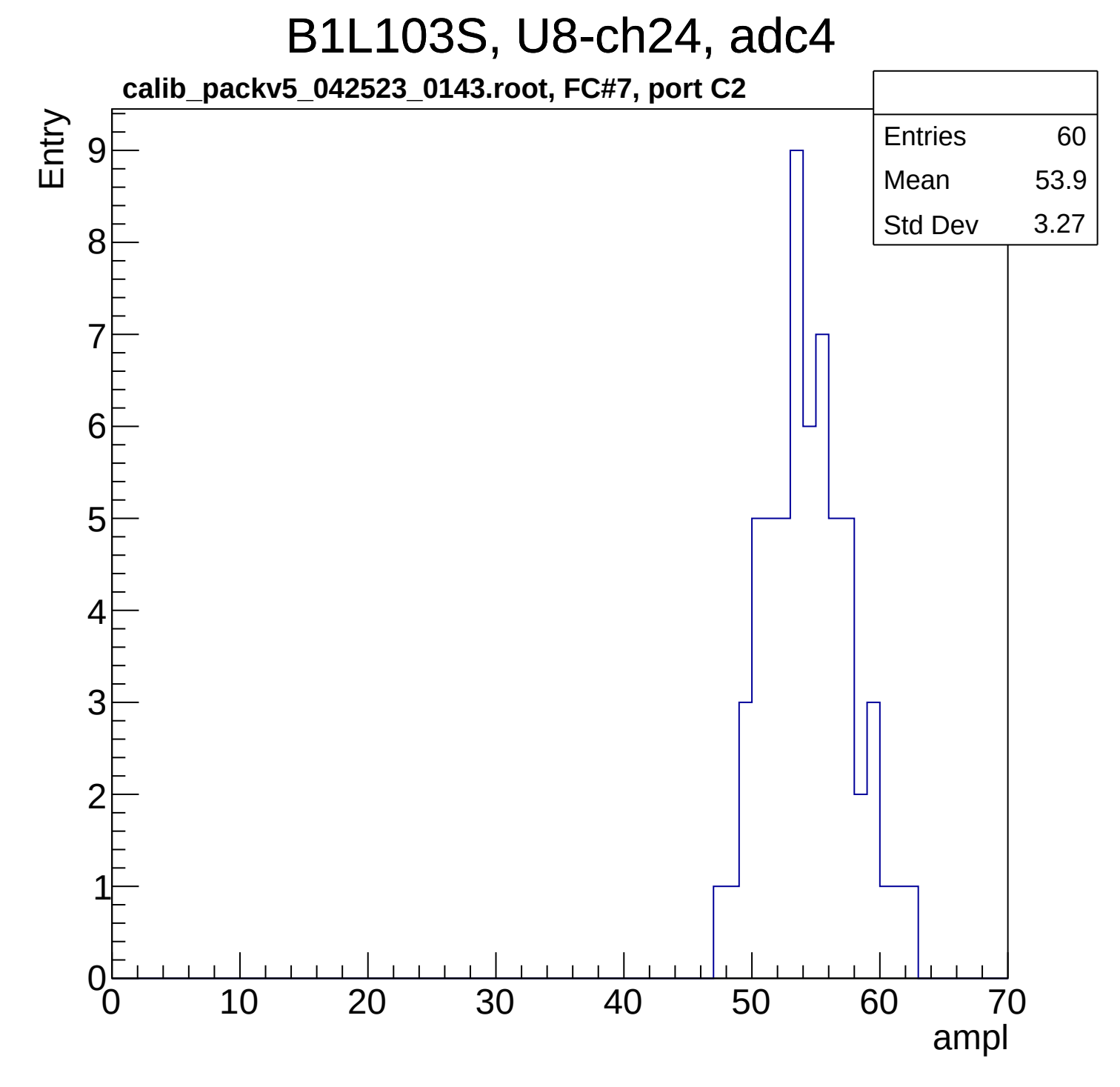

B1L103S, U8-ch23, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

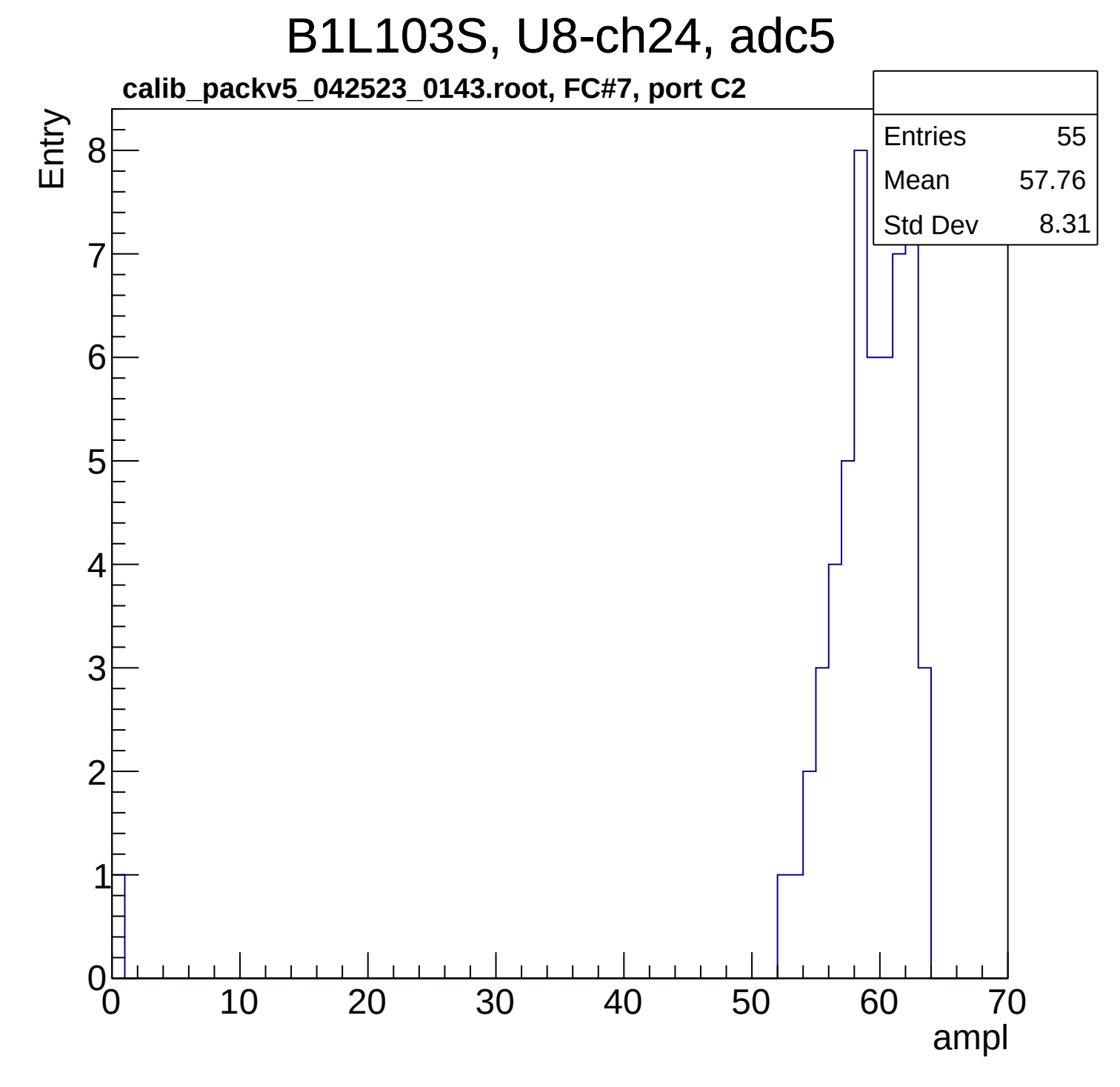

B1L103S, U8-ch24, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 27.66
Std Dev 3.551
Gaus mean : 27.9387
Gaus Width: 3.5279
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

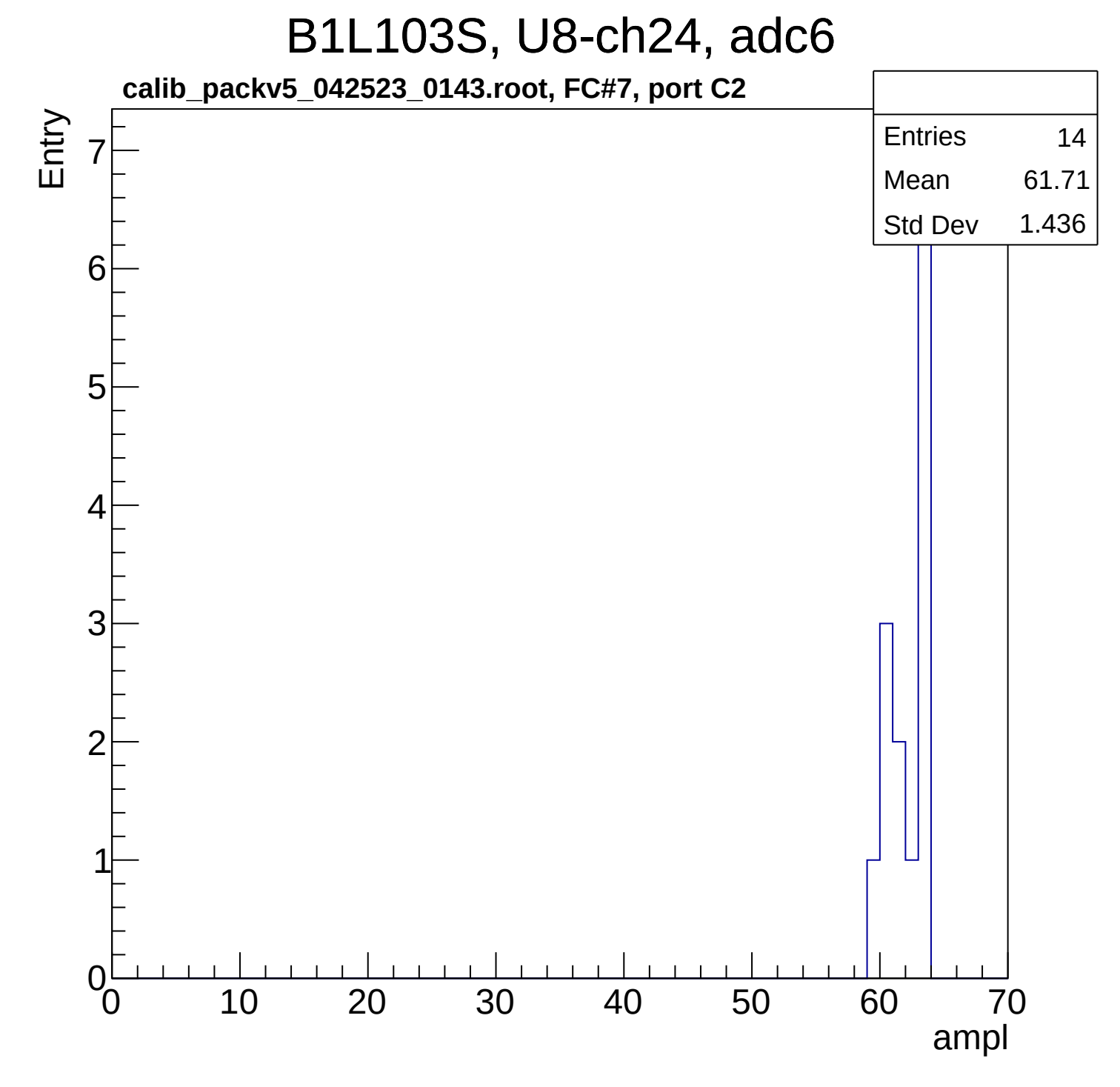

B1L103S, U8-ch24, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 34.11
Std Dev 3.263
Gaus mean : 34.9748
Gaus Width: 3.0023
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

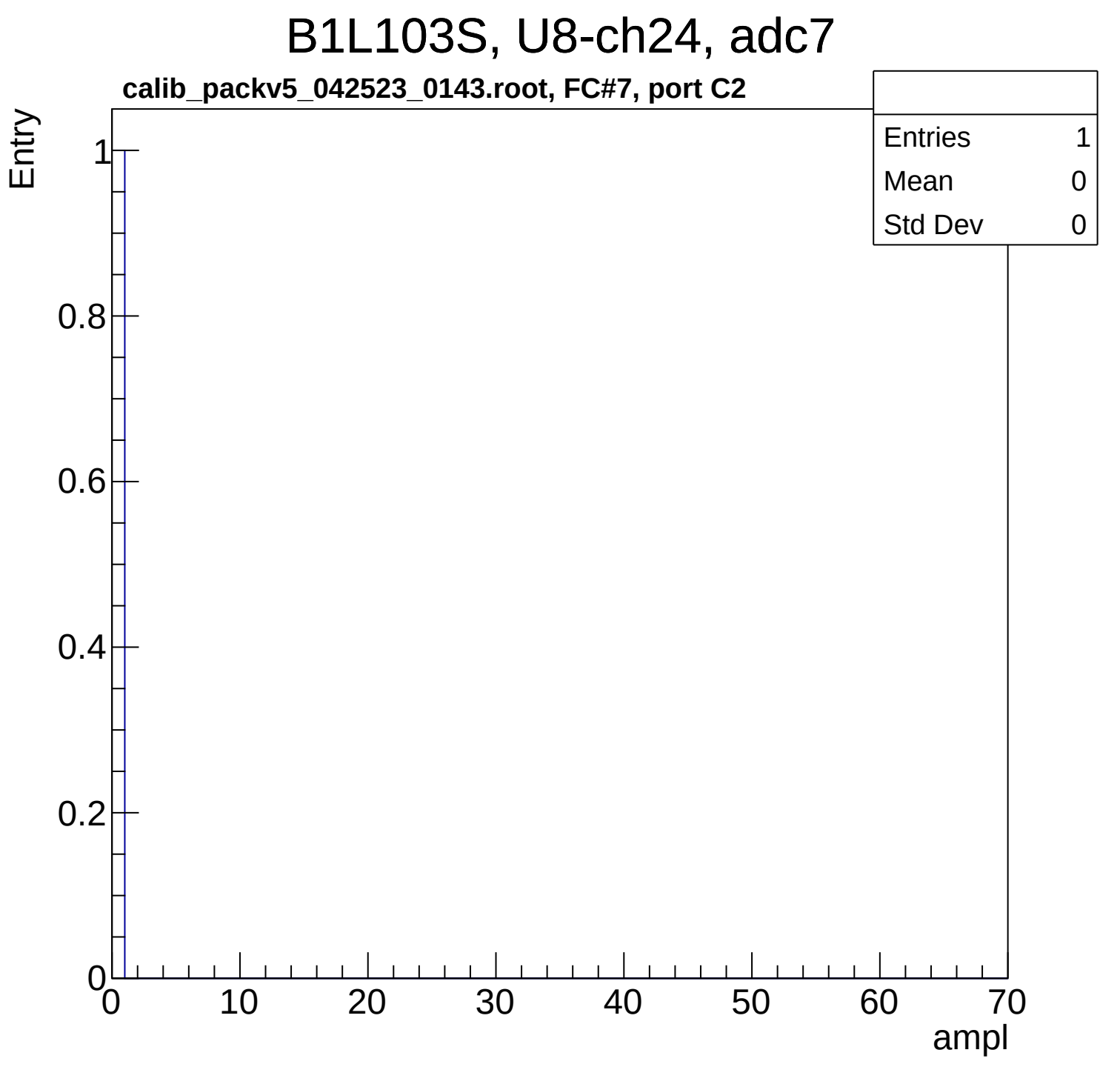

B1L103S, U8-ch24, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 40.78
Std Dev 3.111
Gaus mean : 41.2753
Gaus Width: 3.2254
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

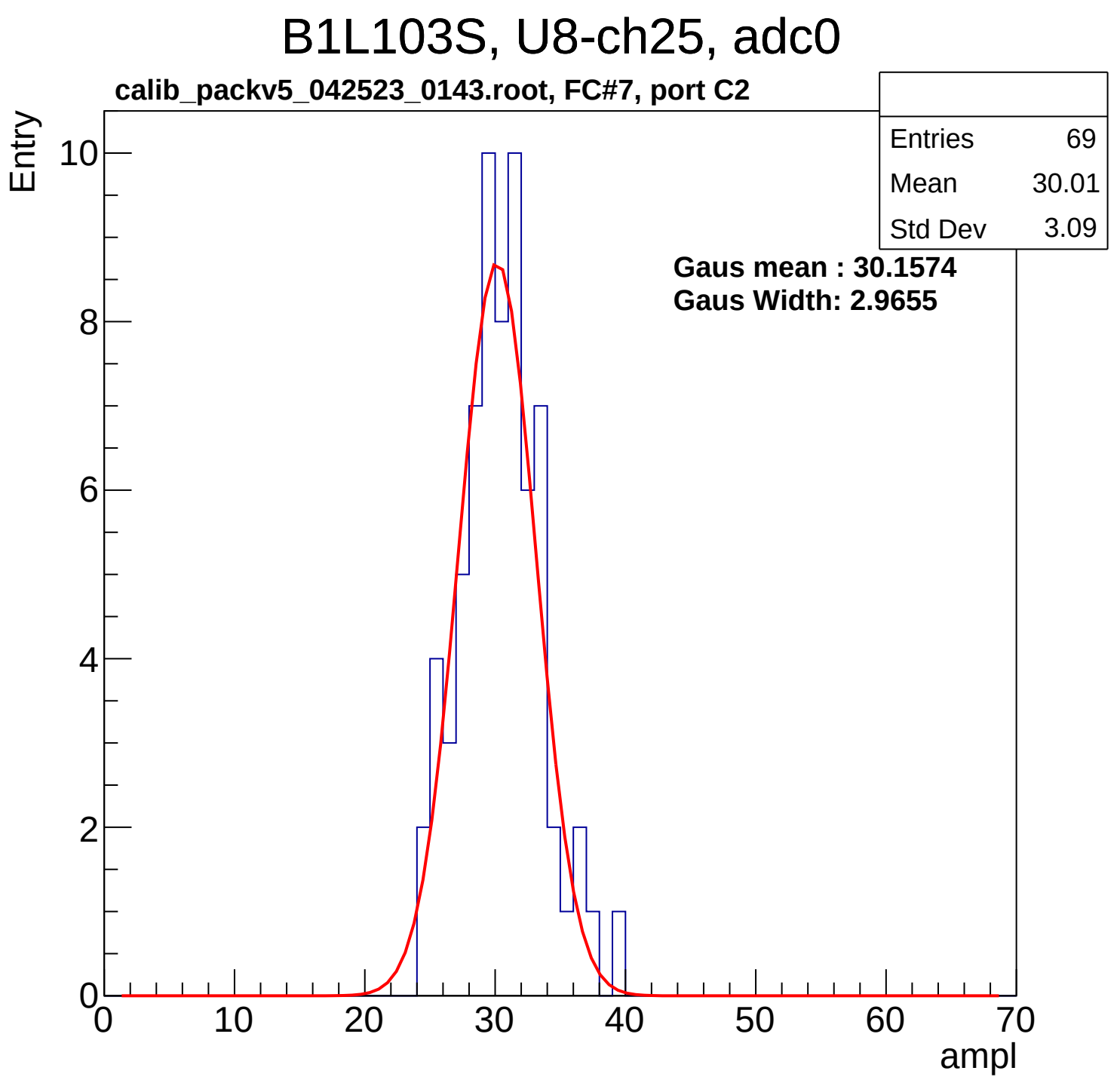

B1L103S, U8-ch24, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 47.39
Std Dev 3.26
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

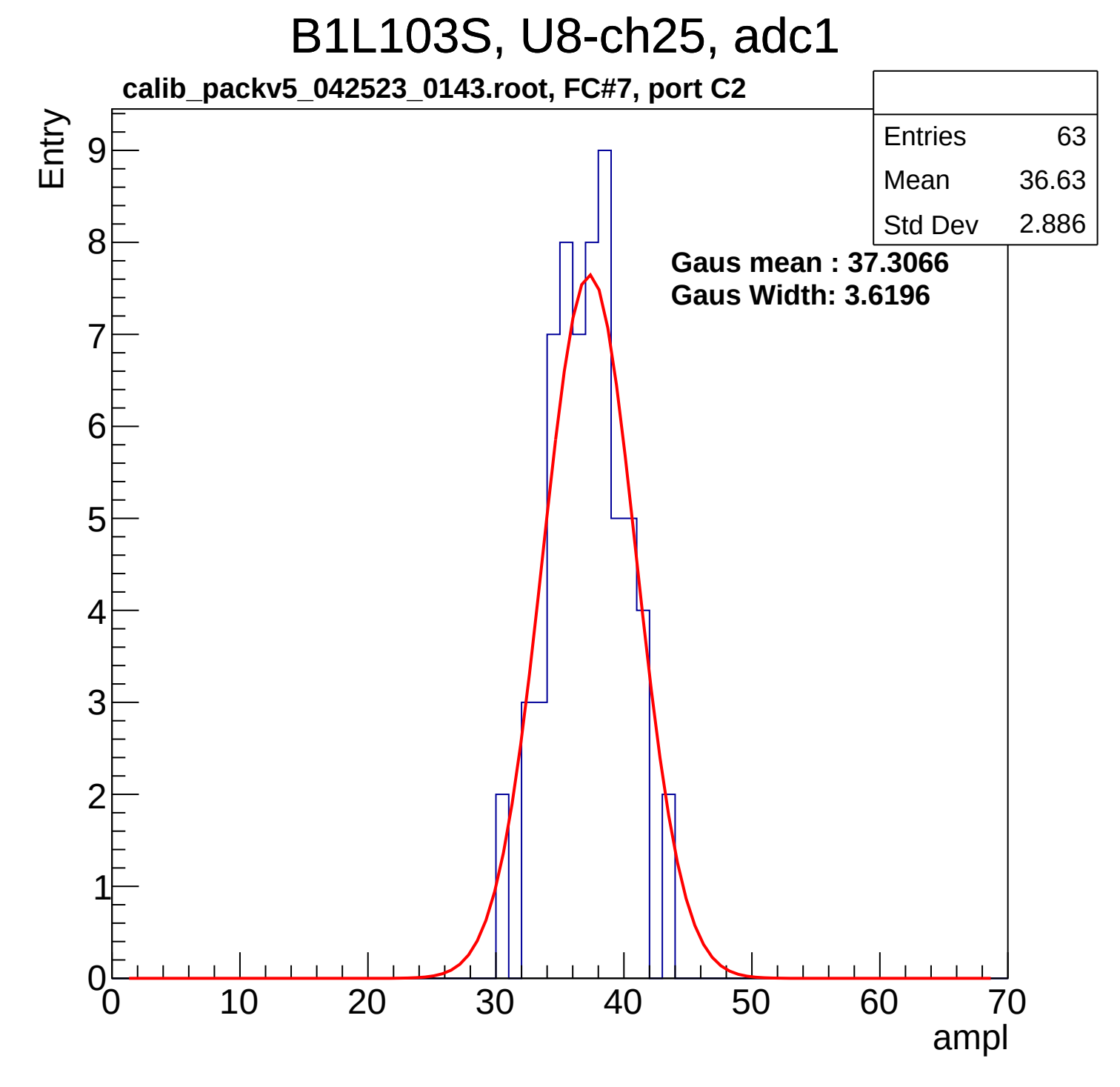

B1L103S, U8-ch24, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 53.9
Std Dev 3.27
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

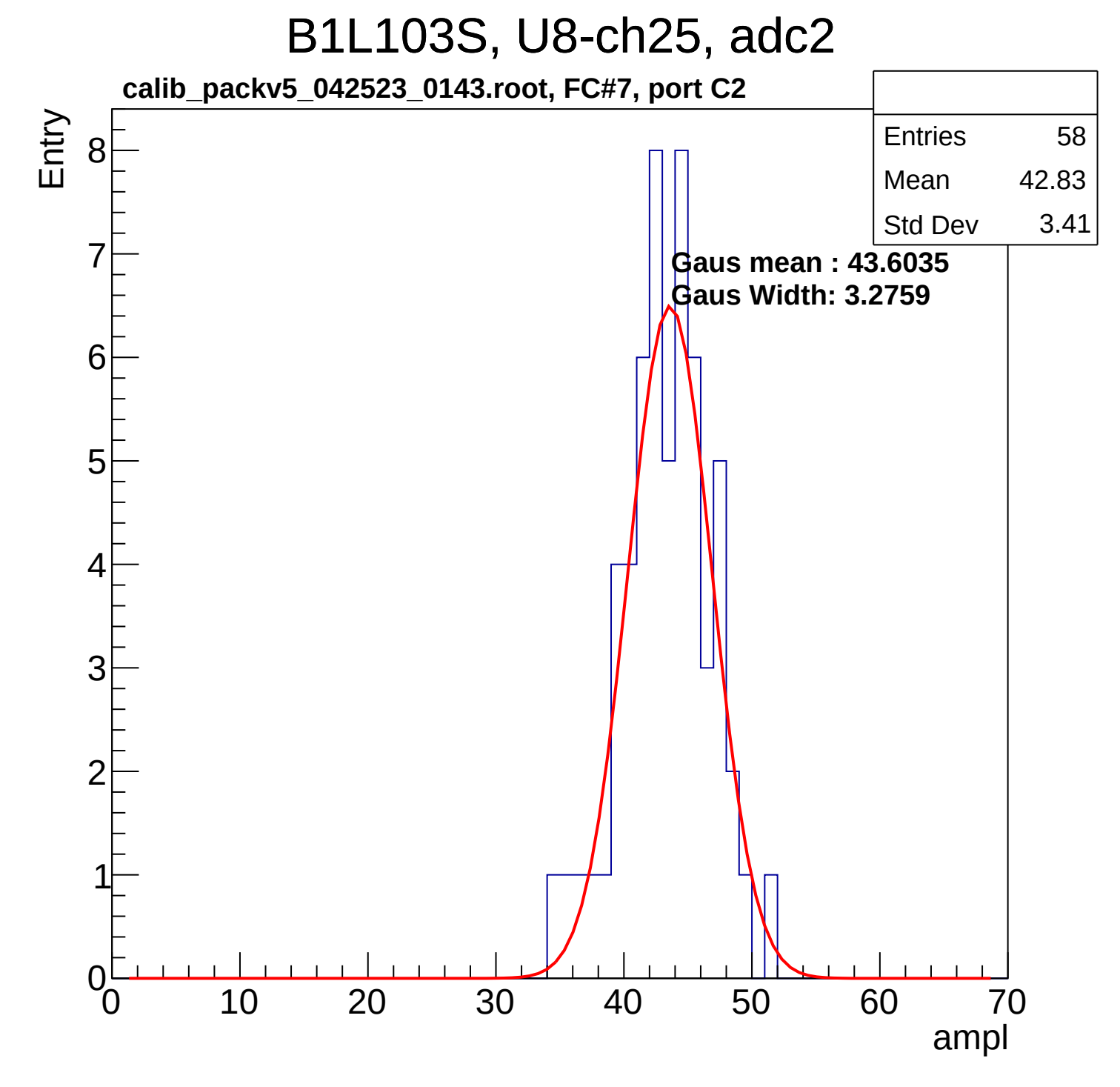

B1L103S, U8-ch24, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 57.76
Std Dev 8.31
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

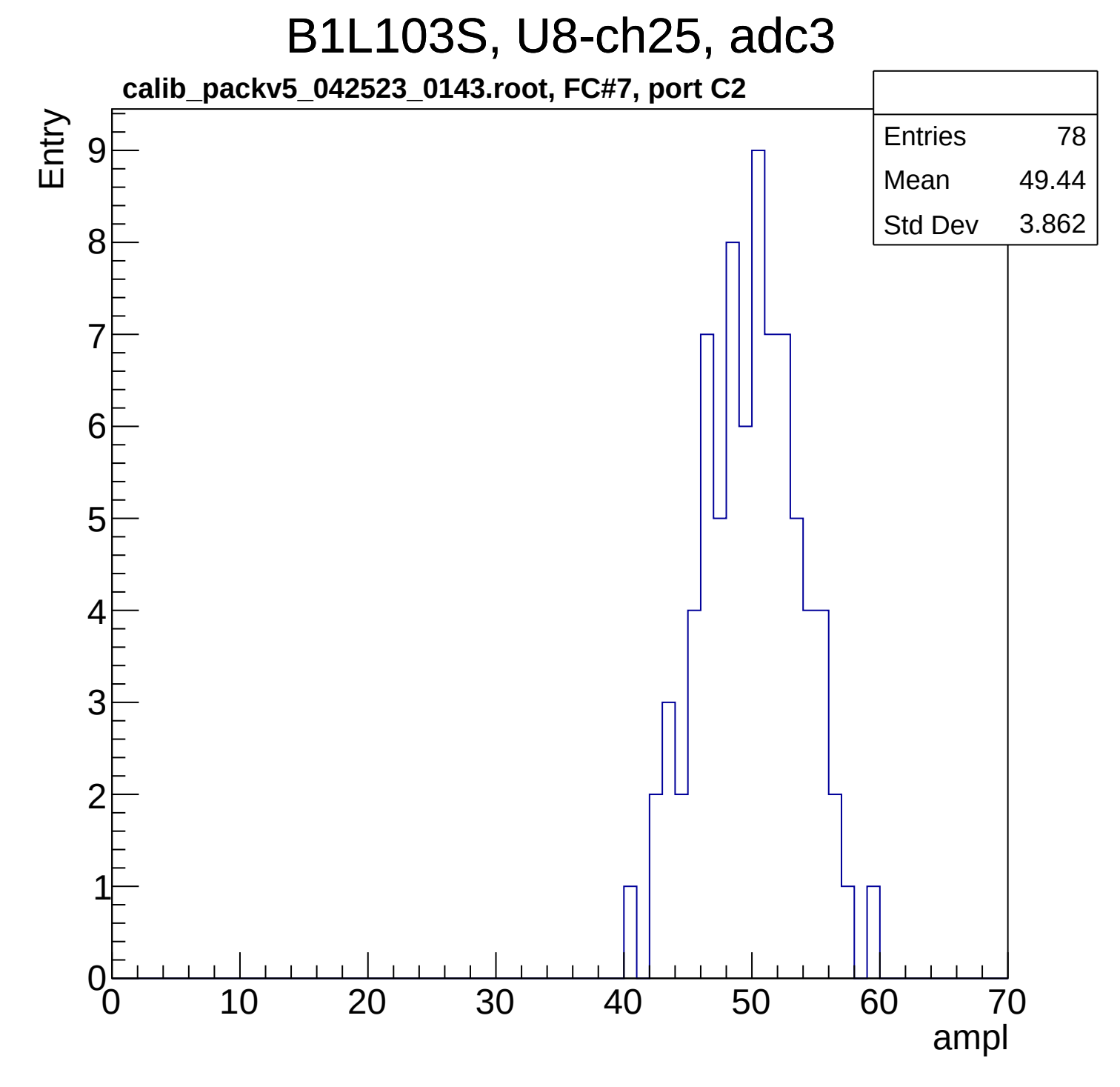

B1L103S, U8-ch24, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 14
Mean 61.71
Std Dev 1.436
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

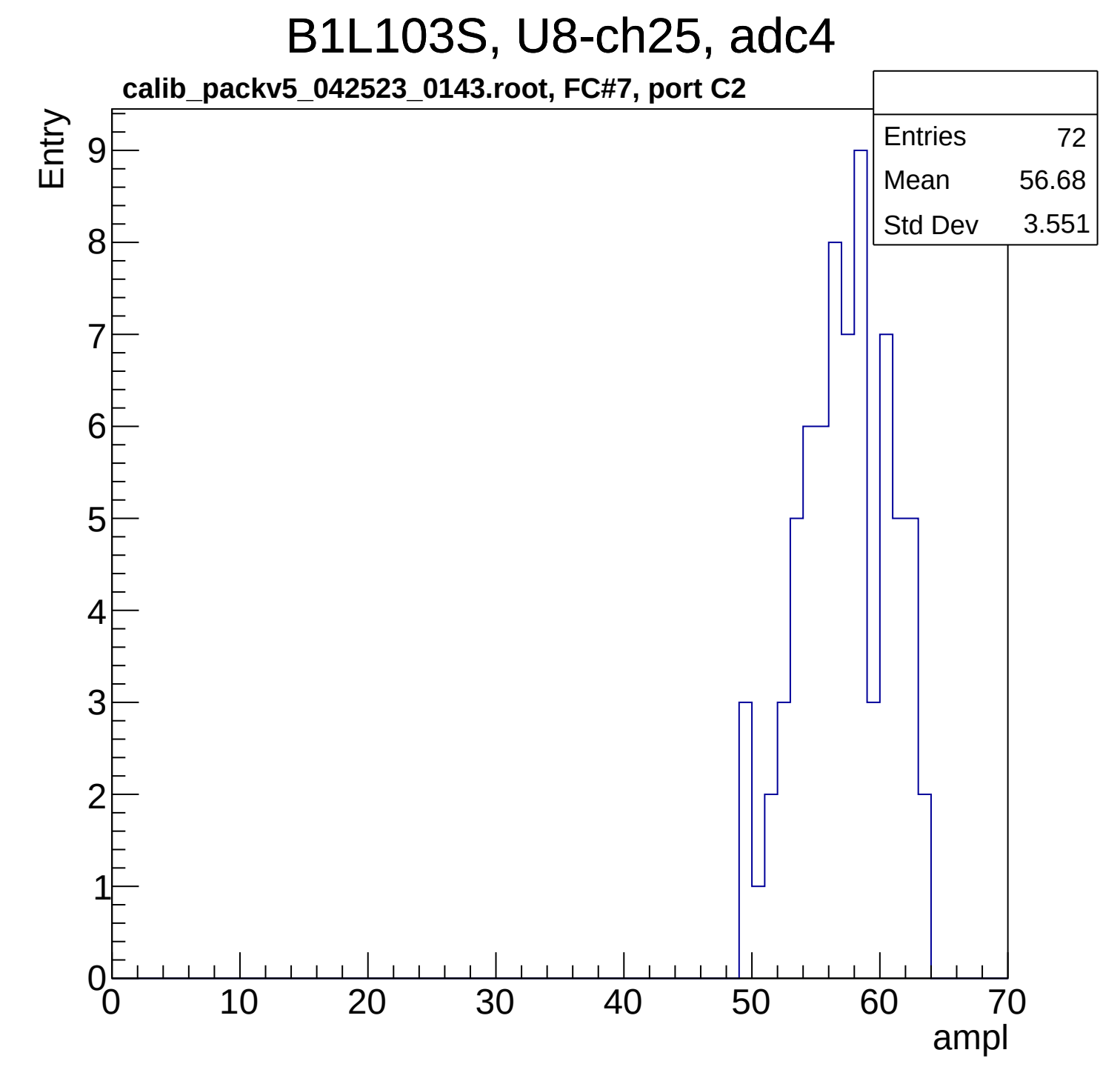

B1L103S, U8-ch24, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

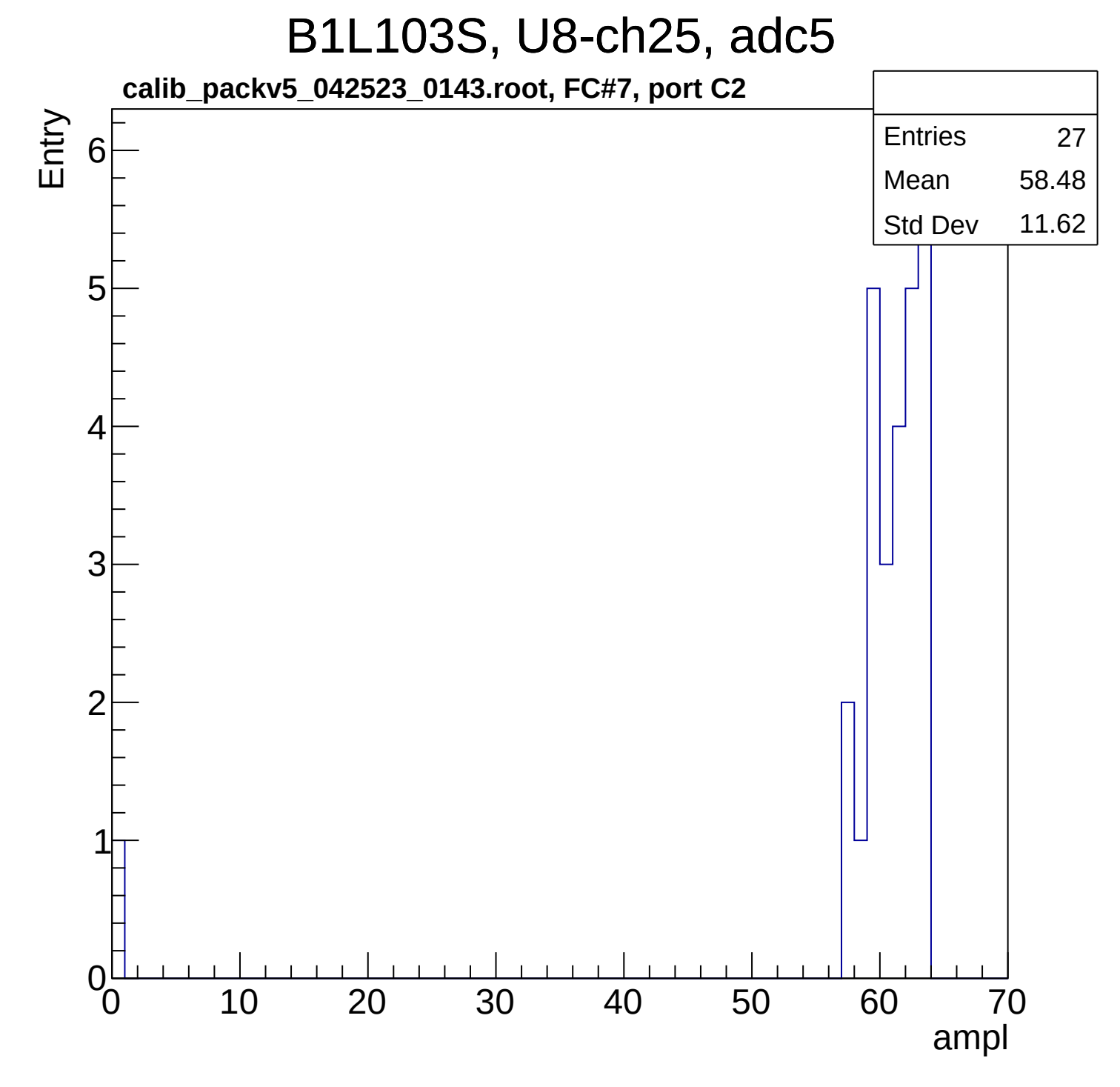

B1L103S, U8-ch25, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 30.01
Std Dev 3.09
Gaus mean : 30.1574
Gaus Width: 2.9655
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

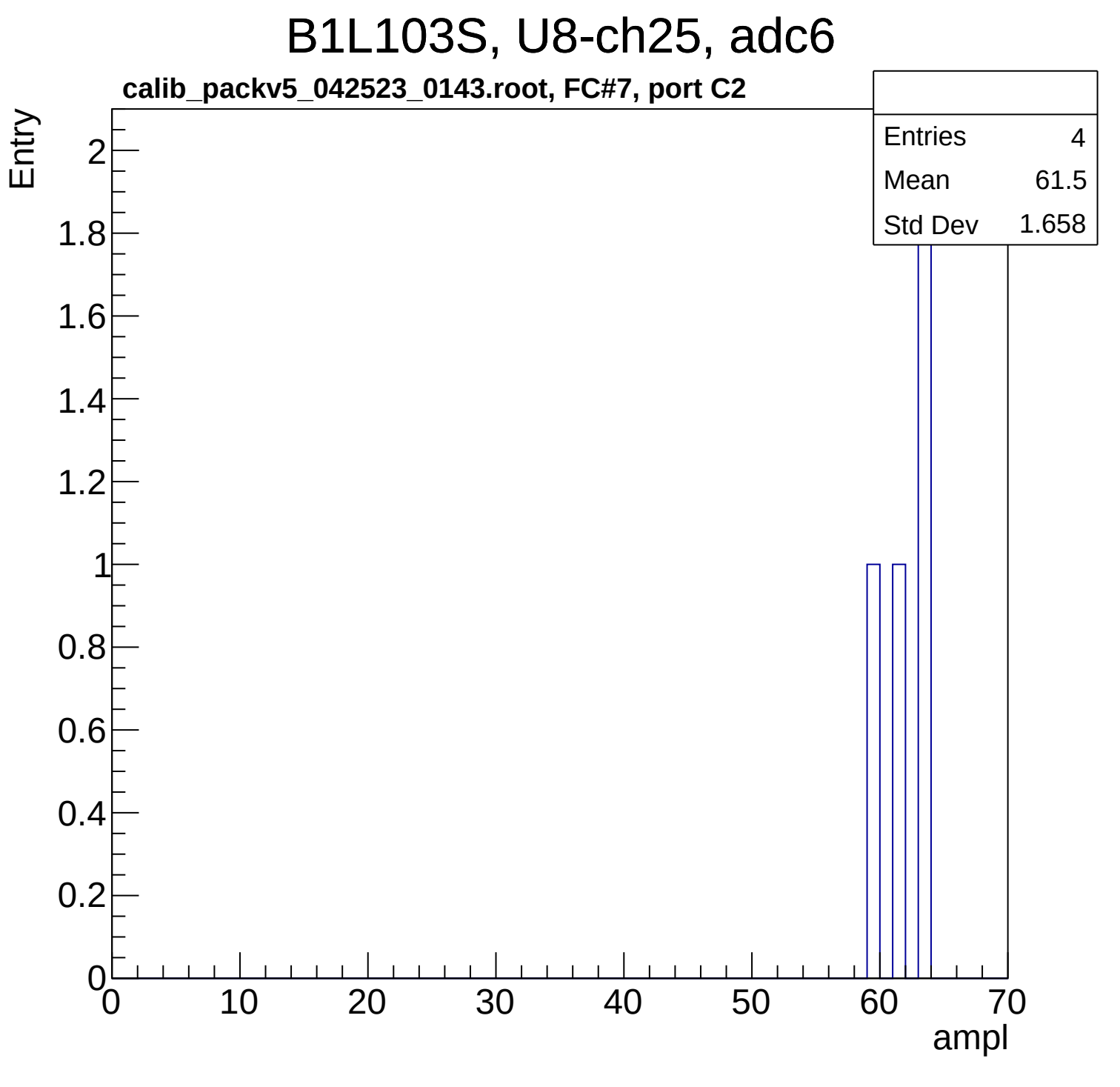

B1L103S, U8-ch25, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 36.63
Std Dev 2.886
Gaus mean : 37.3066
Gaus Width: 3.6196
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

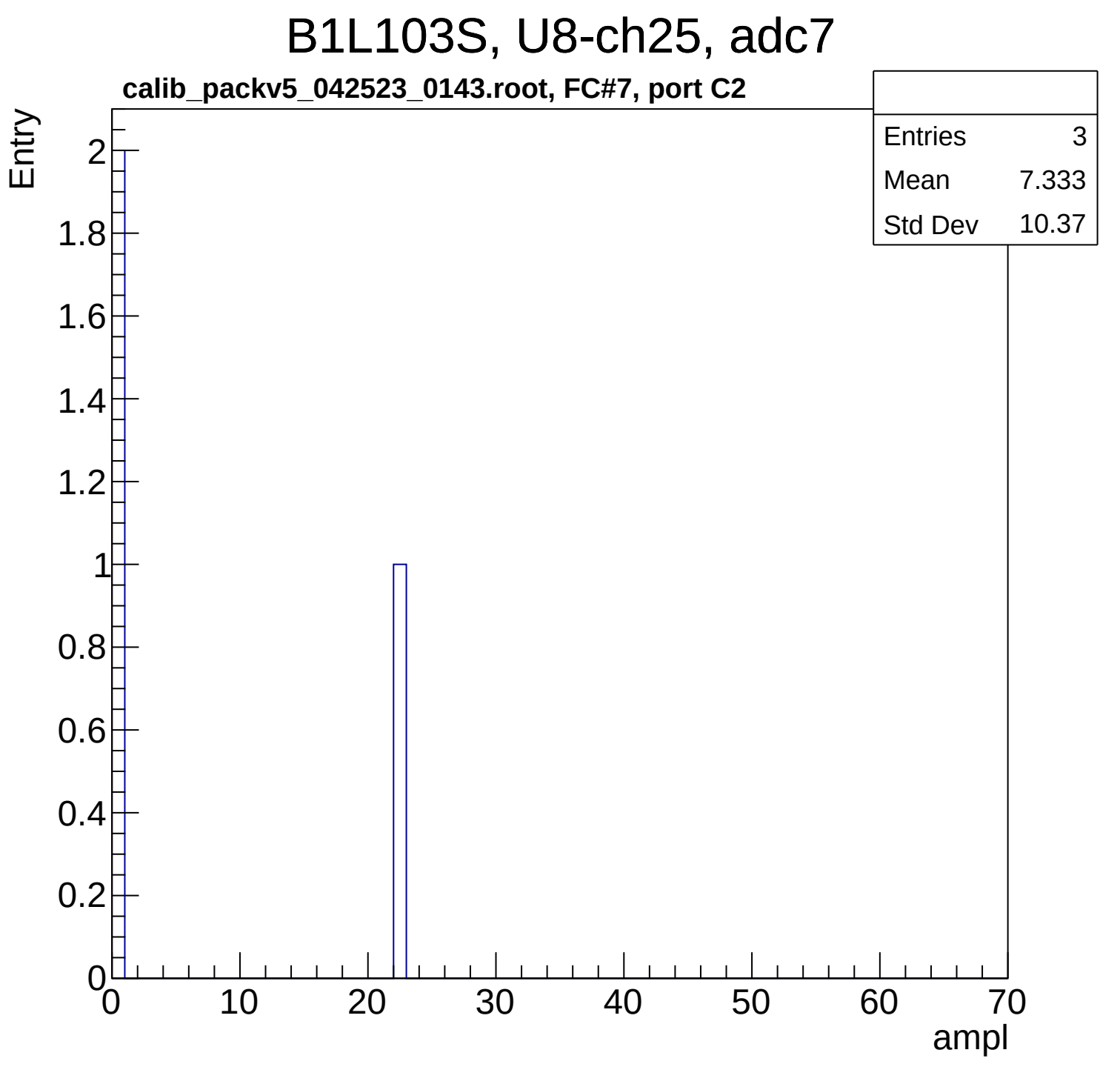

B1L103S, U8-ch25, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 42.83
Std Dev 3.41
Gaus mean : 43.6035
Gaus Width: 3.2759
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

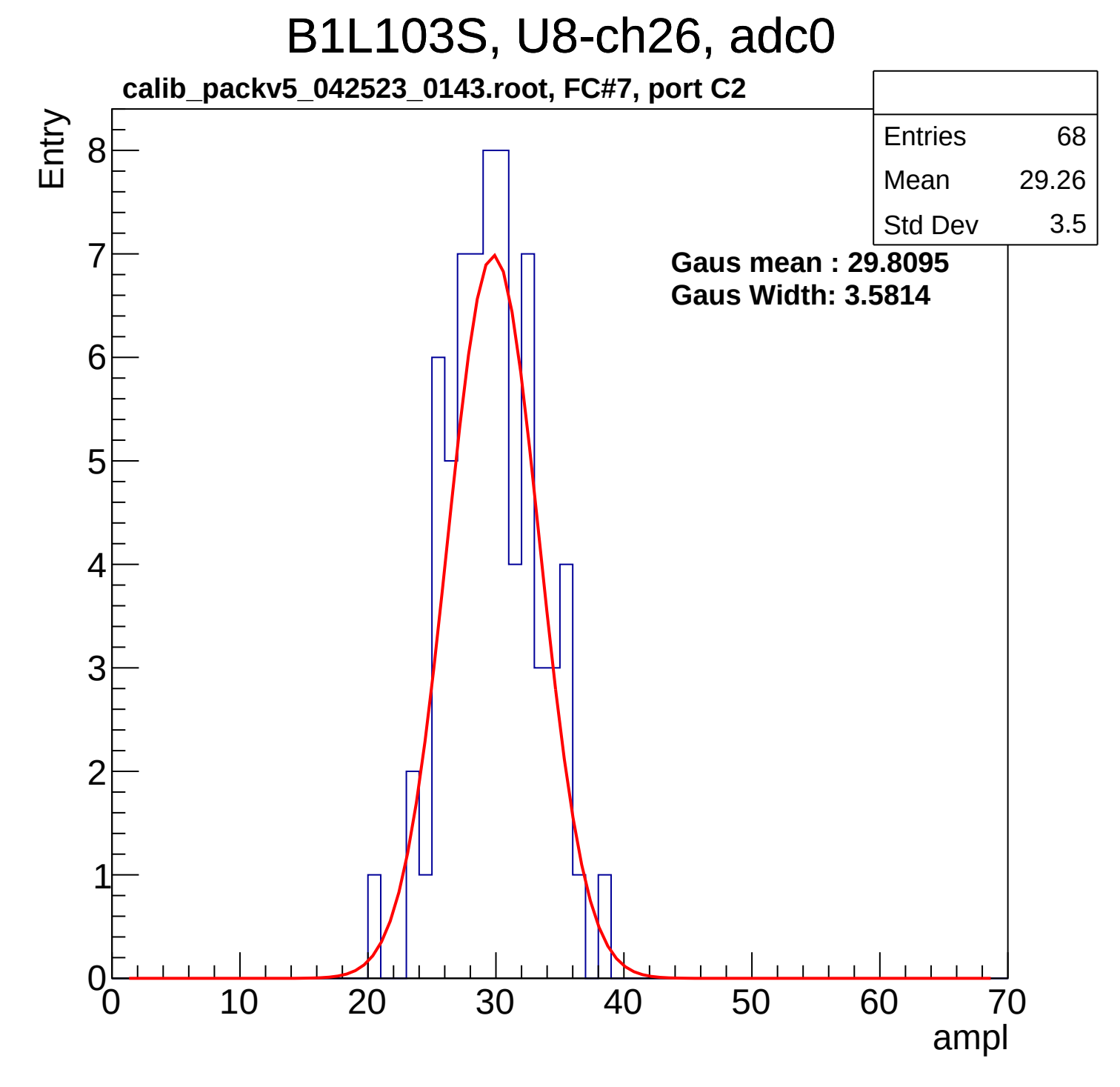

B1L103S, U8-ch25, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 49.44
Std Dev 3.862
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

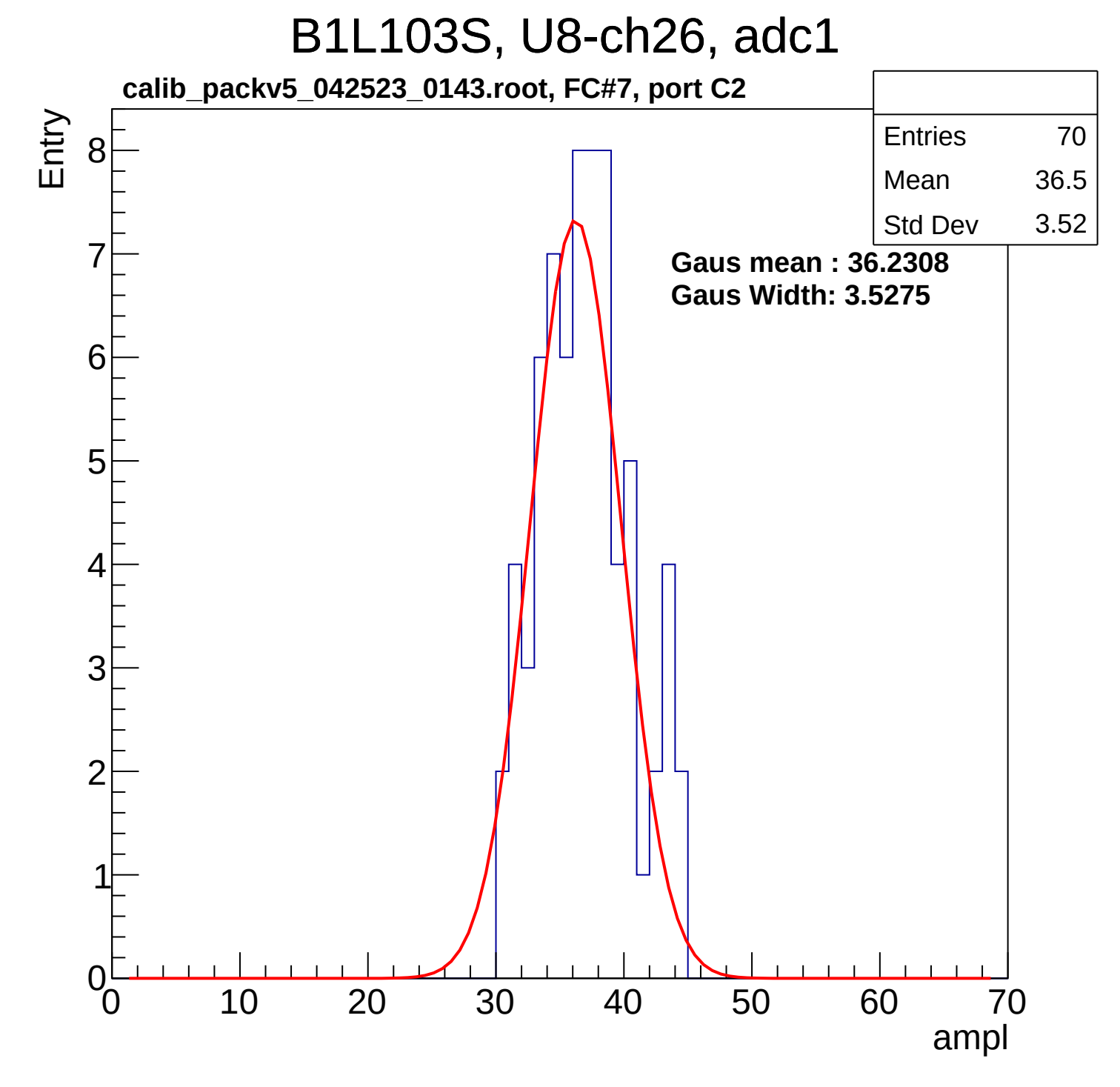

B1L103S, U8-ch25, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 56.68
Std Dev 3.551
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

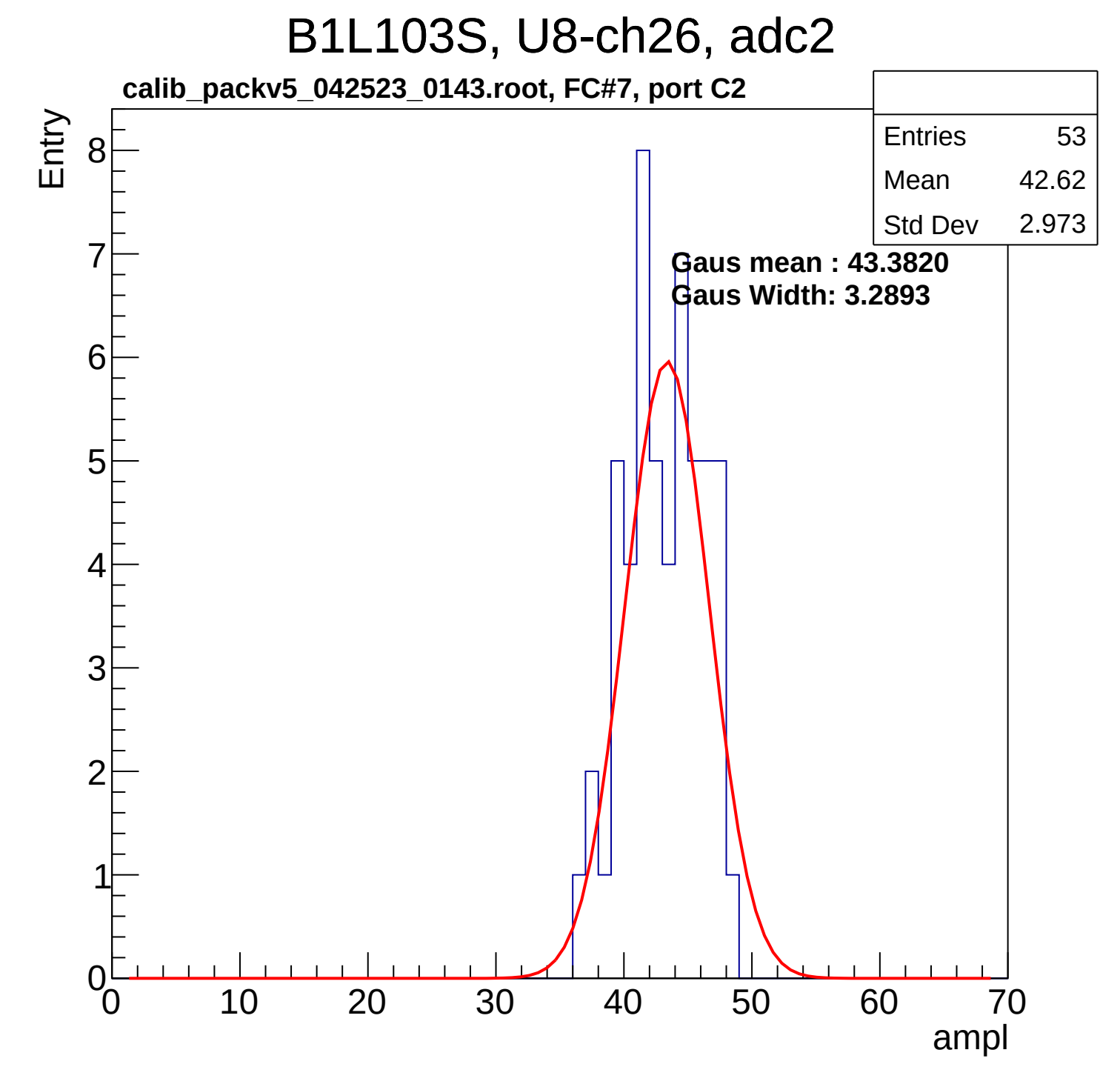

B1L103S, U8-ch25, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 27
Mean 58.48
Std Dev 11.62
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

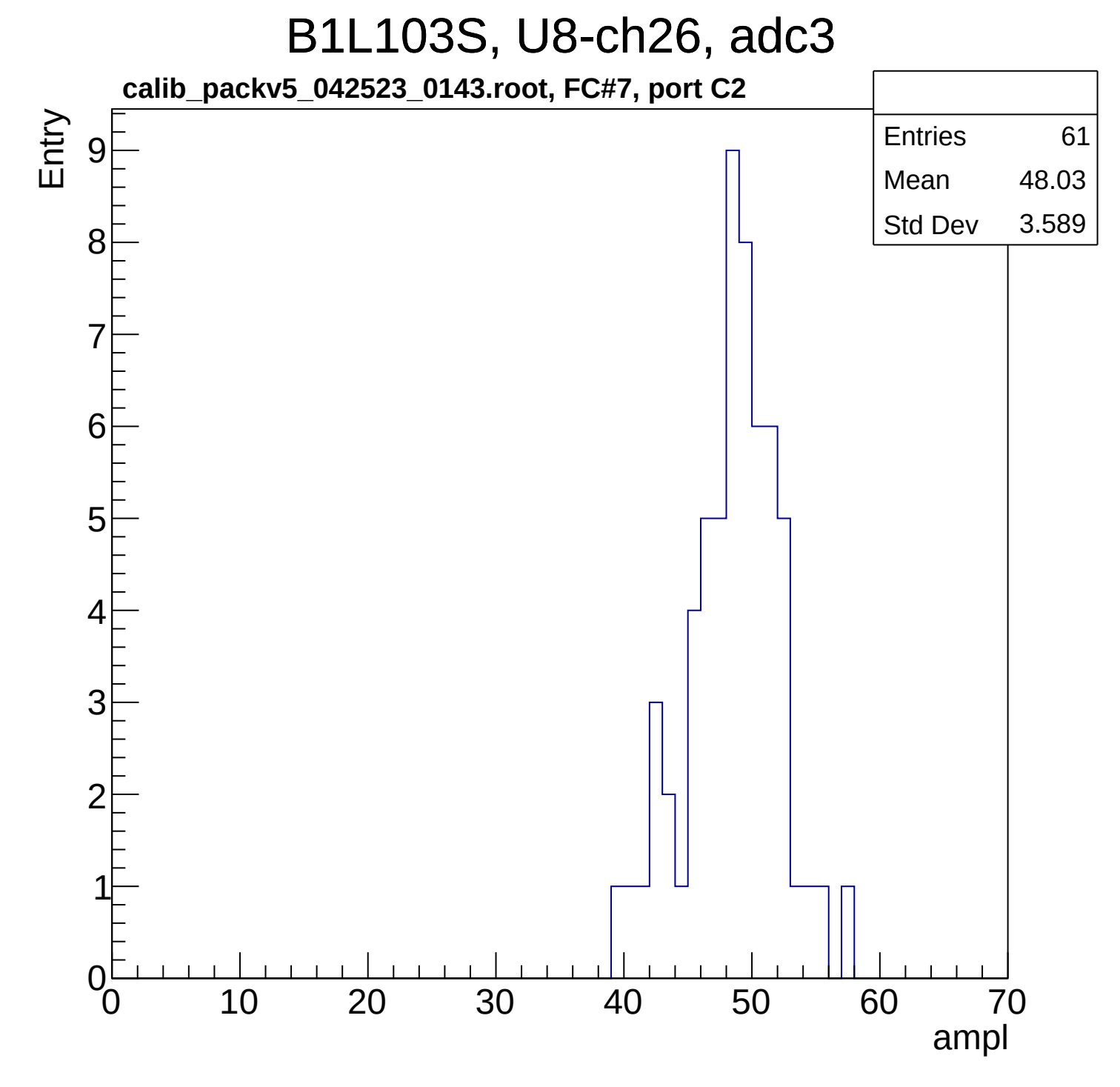

B1L103S, U8-ch25, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 61.5
Std Dev 1.658
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

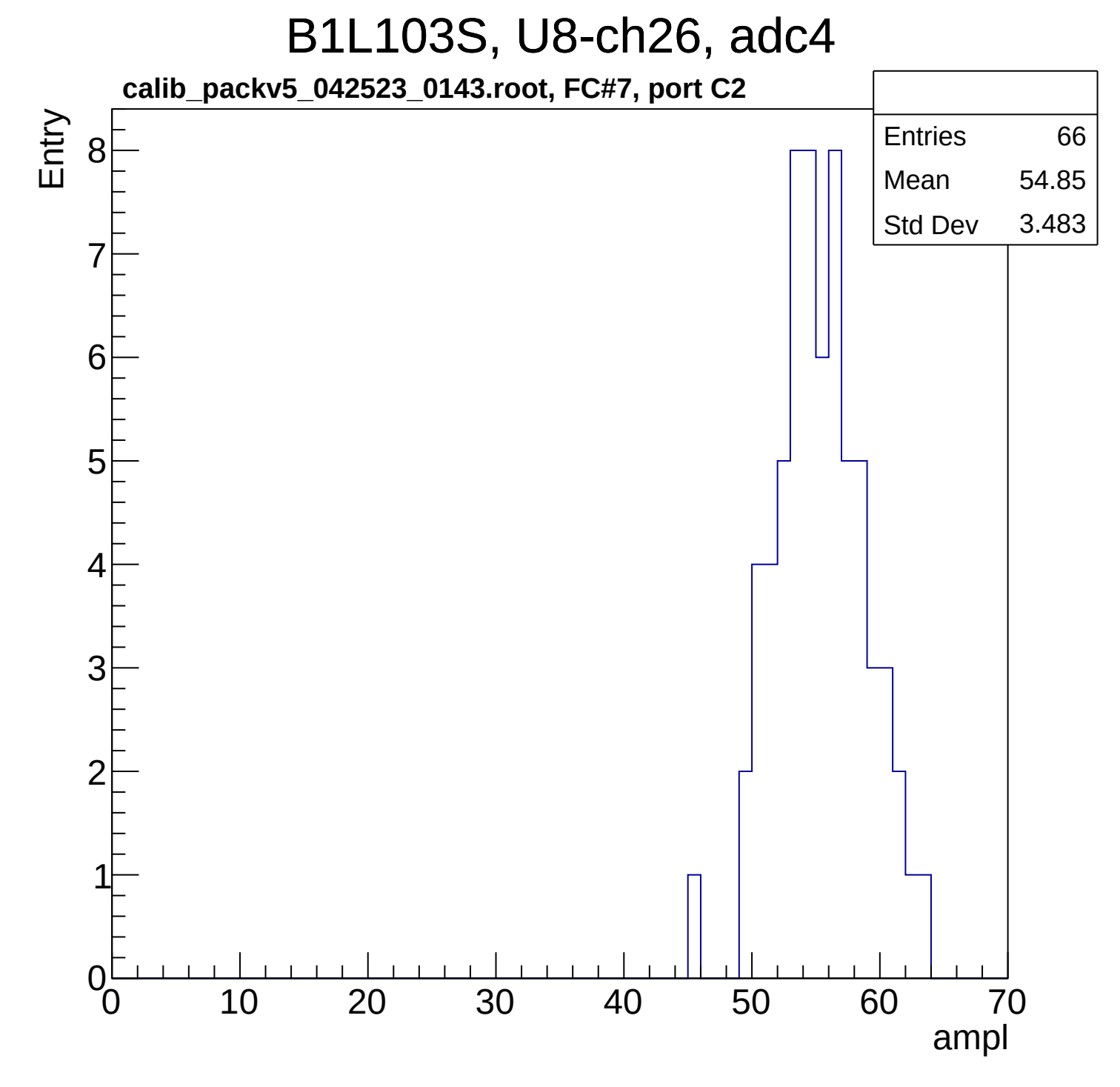

B1L103S, U8-ch25, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 7.333
Std Dev 10.37
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

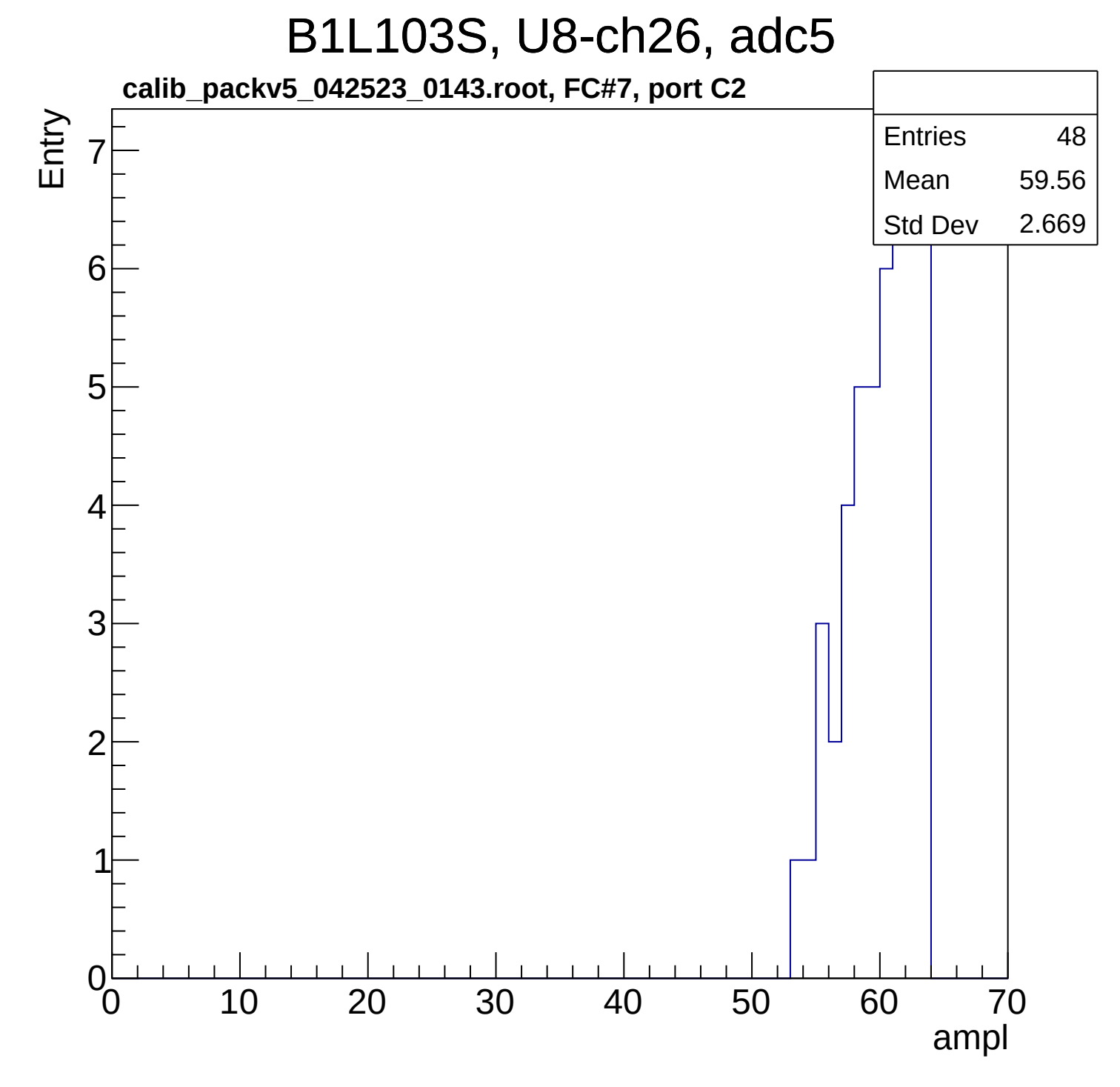

B1L103S, U8-ch26, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 29.26
Std Dev 3.5
Gaus mean : 29.8095
Gaus Width: 3.5814
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

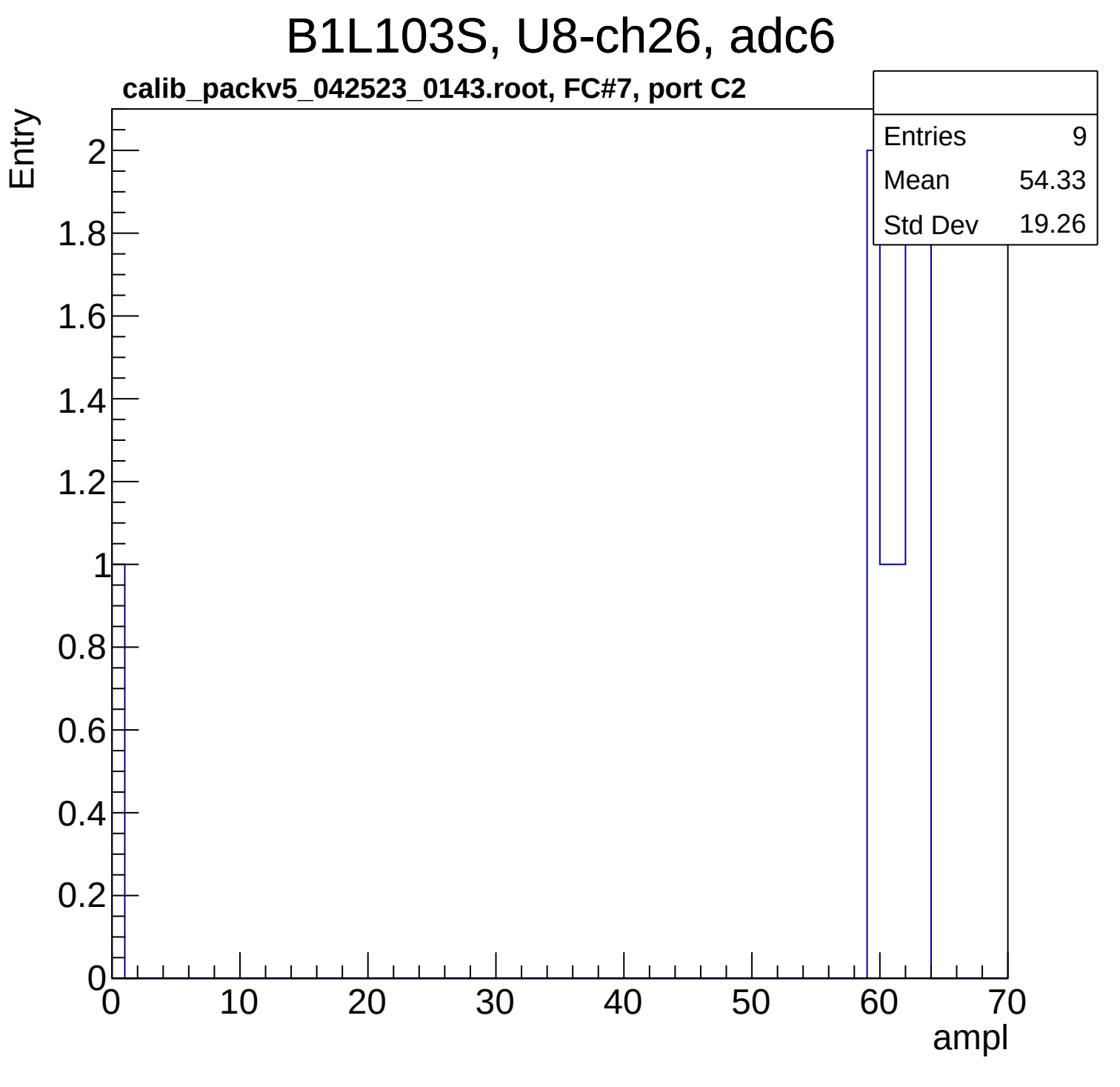

B1L103S, U8-ch26, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 36.5
Std Dev 3.52
Gaus mean : 36.2308
Gaus Width: 3.5275
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

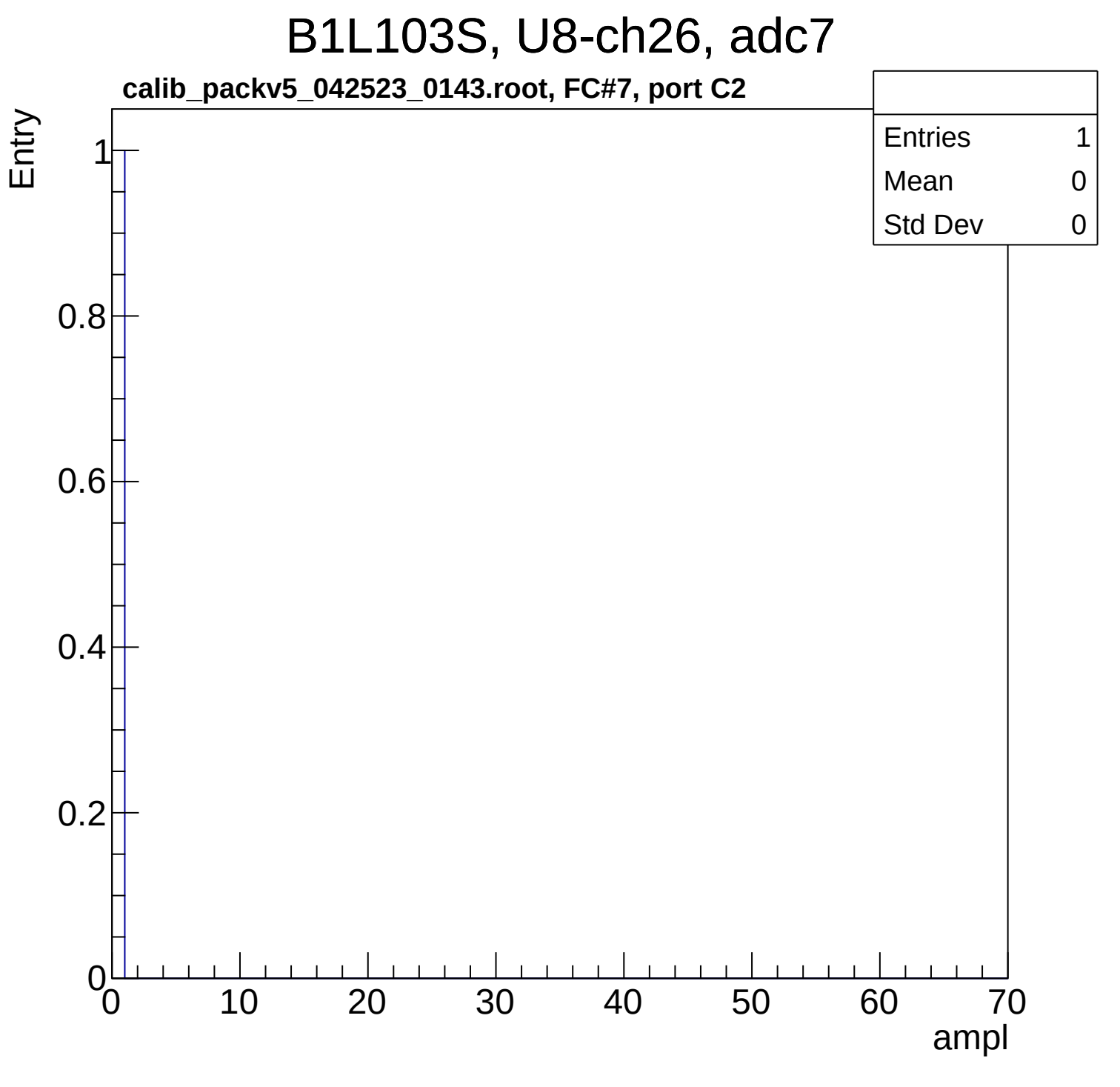

B1L103S, U8-ch26, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 42.62
Std Dev 2.973
Gaus mean : 43.3820
Gaus Width: 3.2893
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

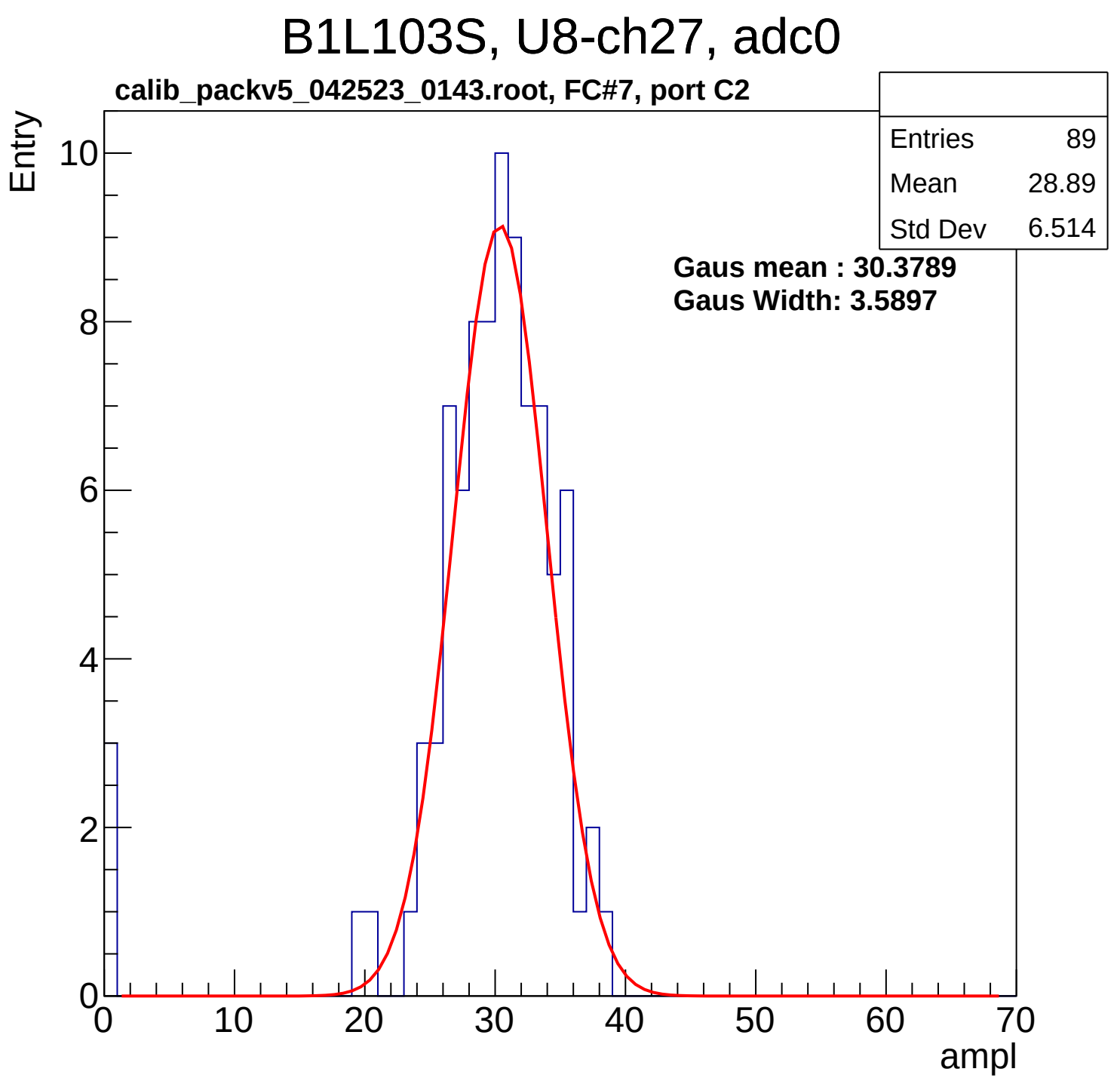

B1L103S, U8-ch26, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 48.03
Std Dev 3.589
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

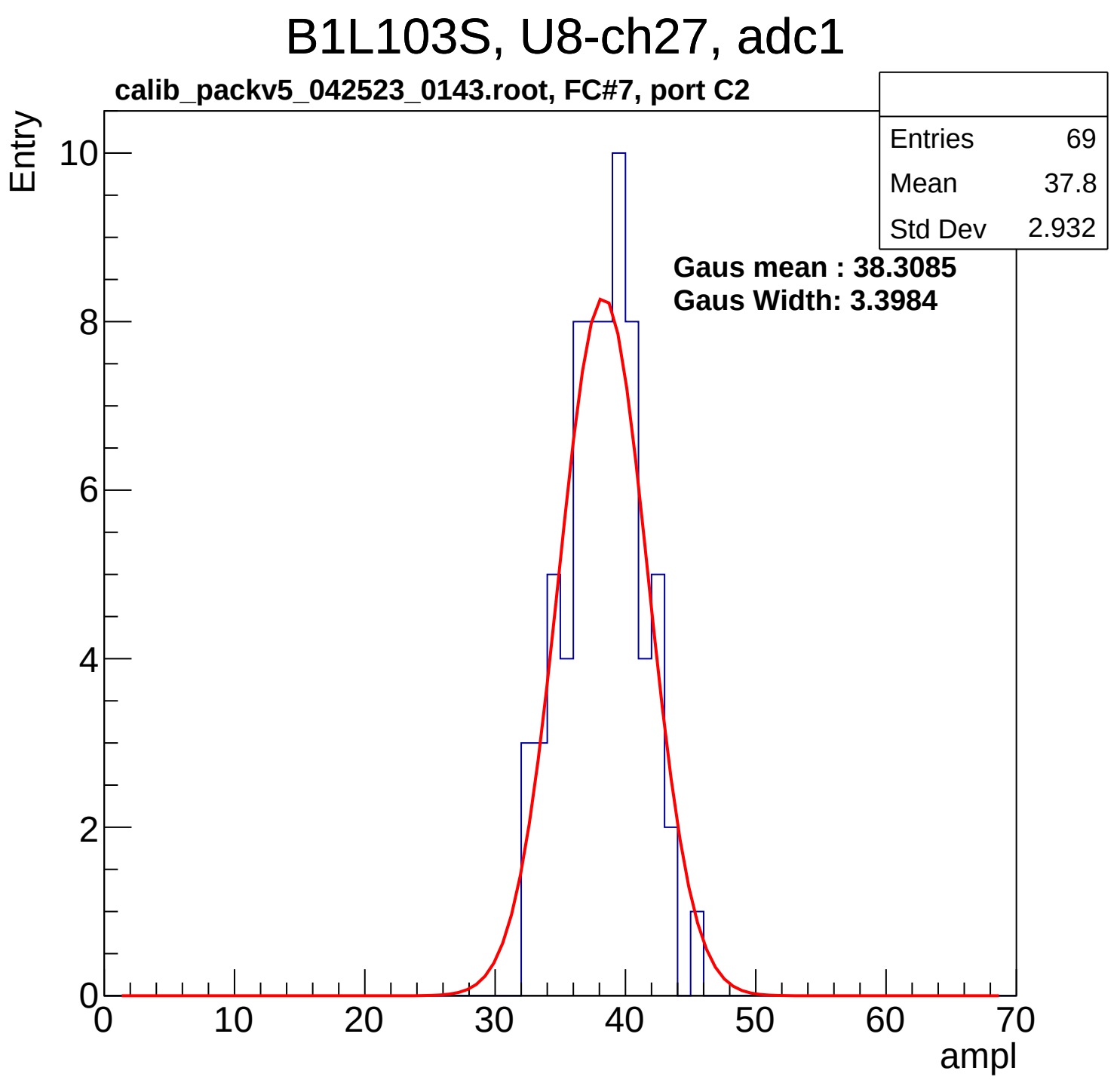

B1L103S, U8-ch26, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 54.85
Std Dev 3.483
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

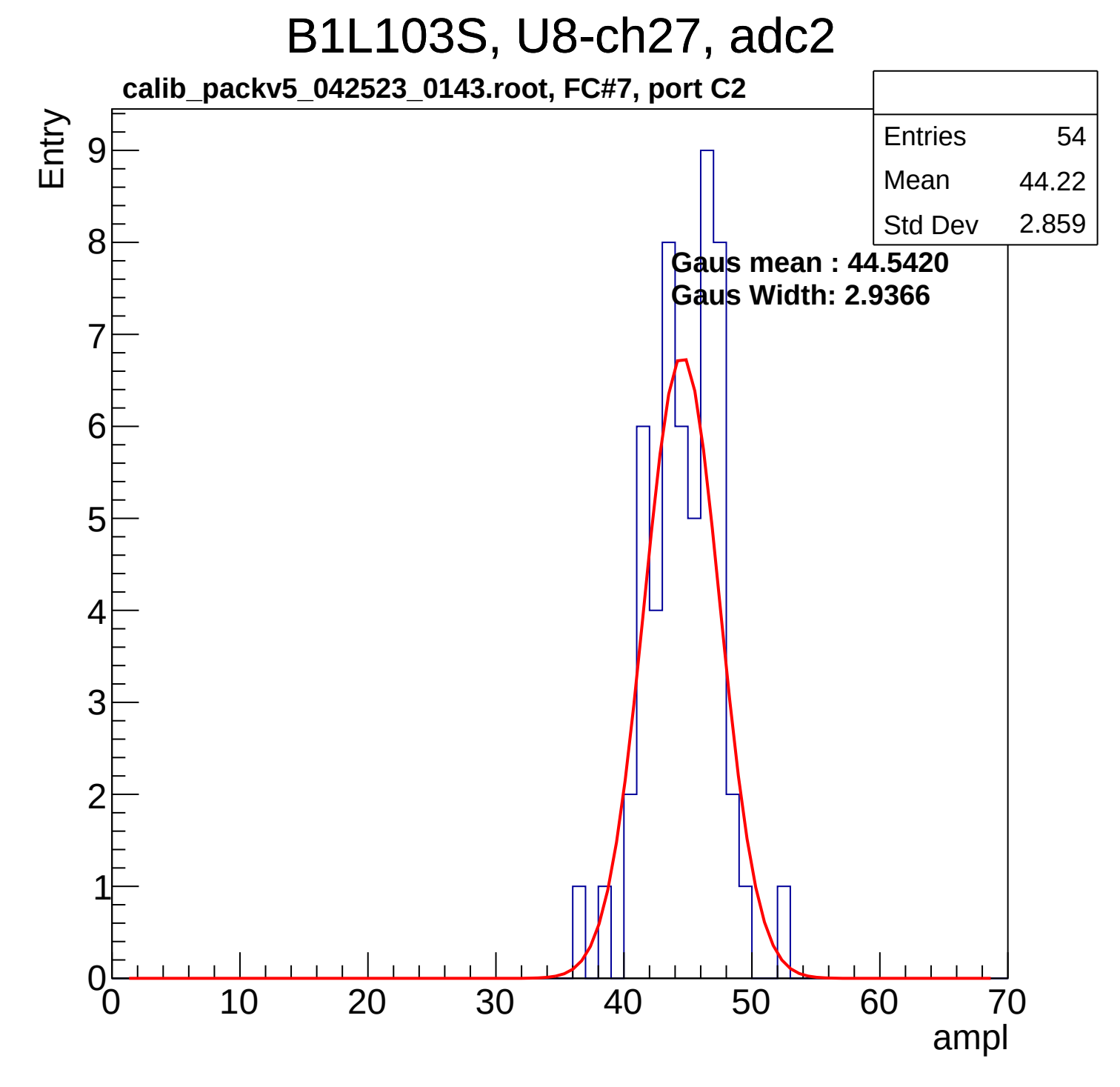

B1L103S, U8-ch26, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 59.56
Std Dev 2.669
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

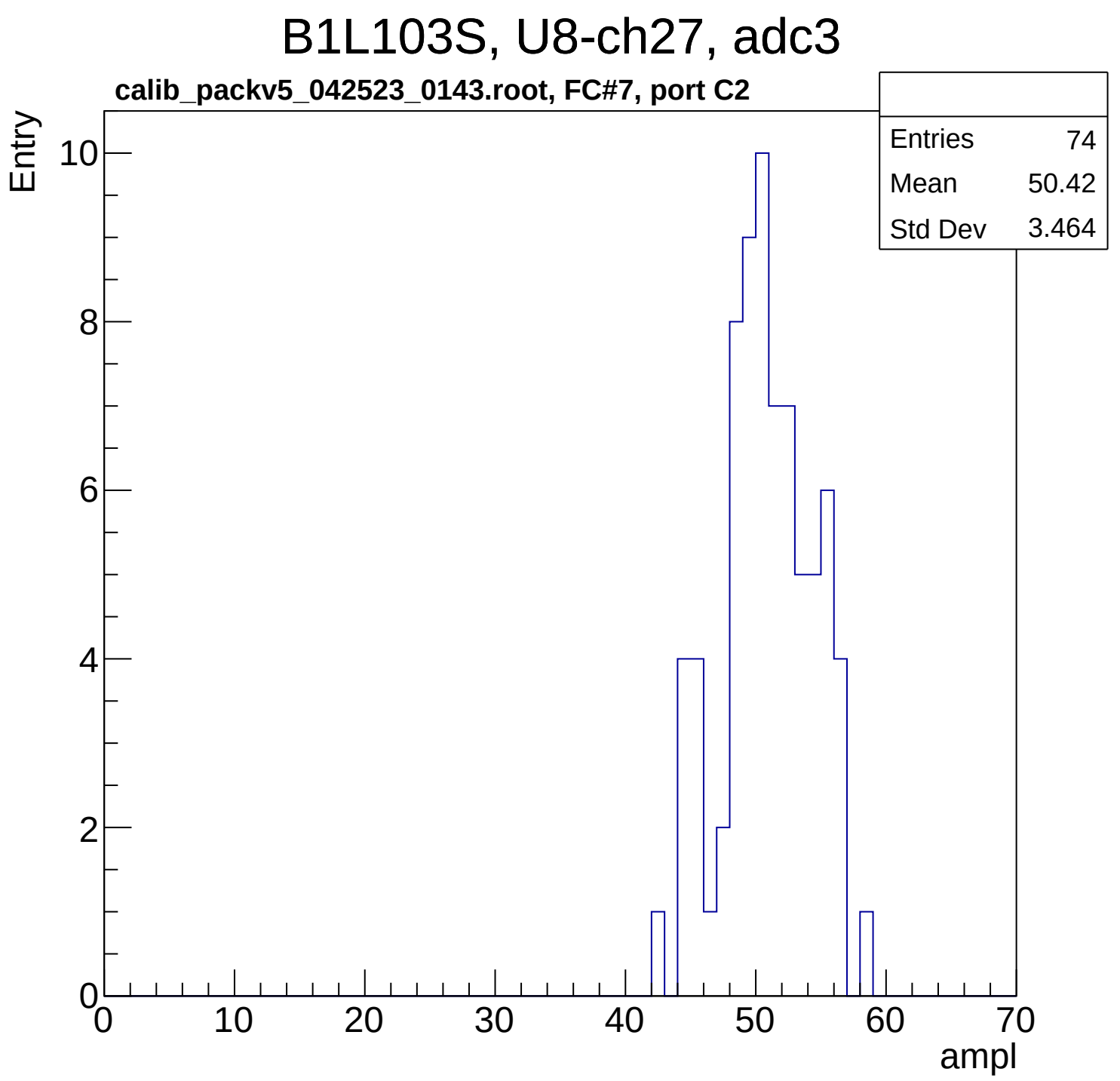

B1L103S, U8-ch26, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 9
Mean 54.33
Std Dev 19.26
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

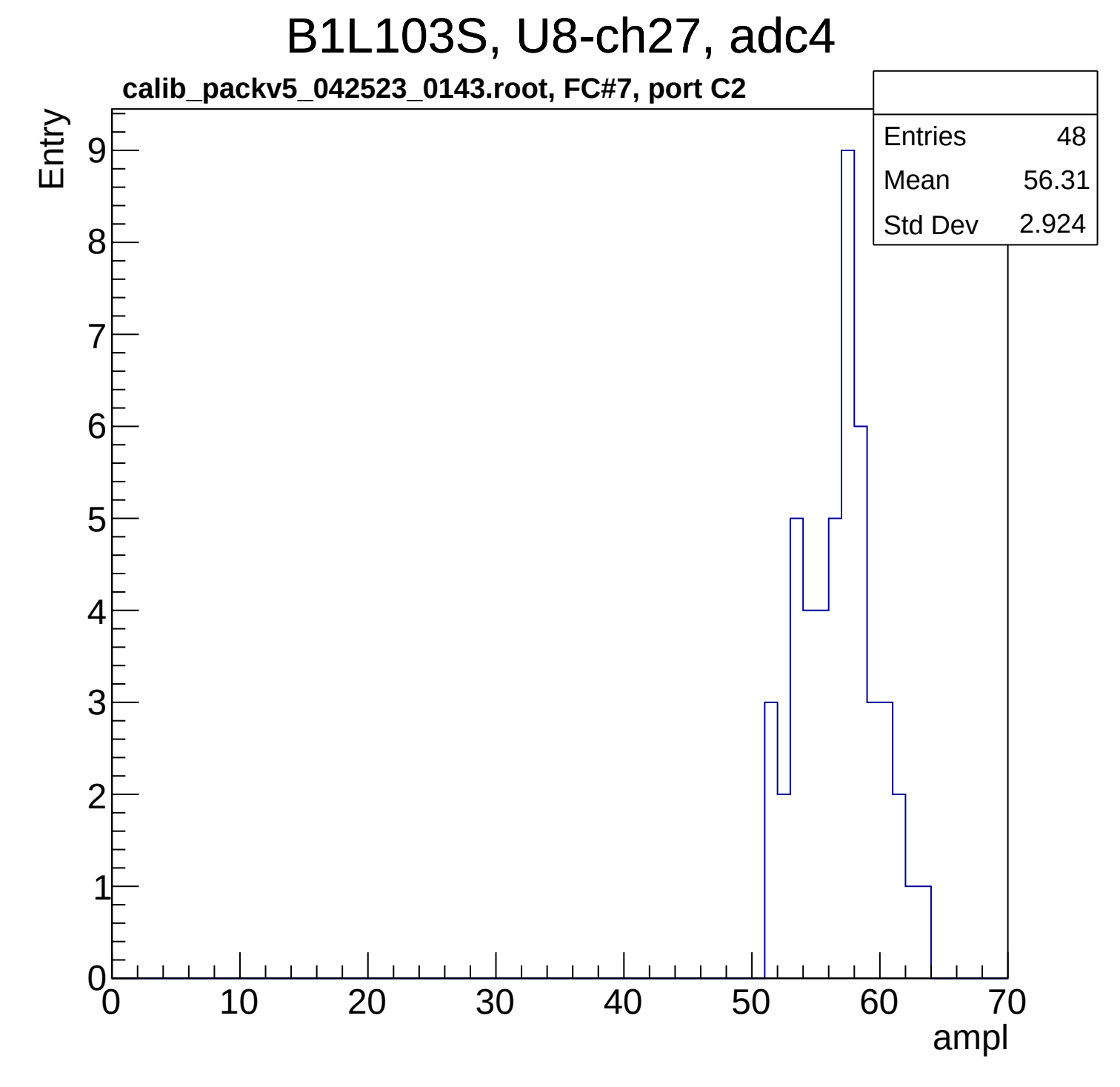

B1L103S, U8-ch26, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

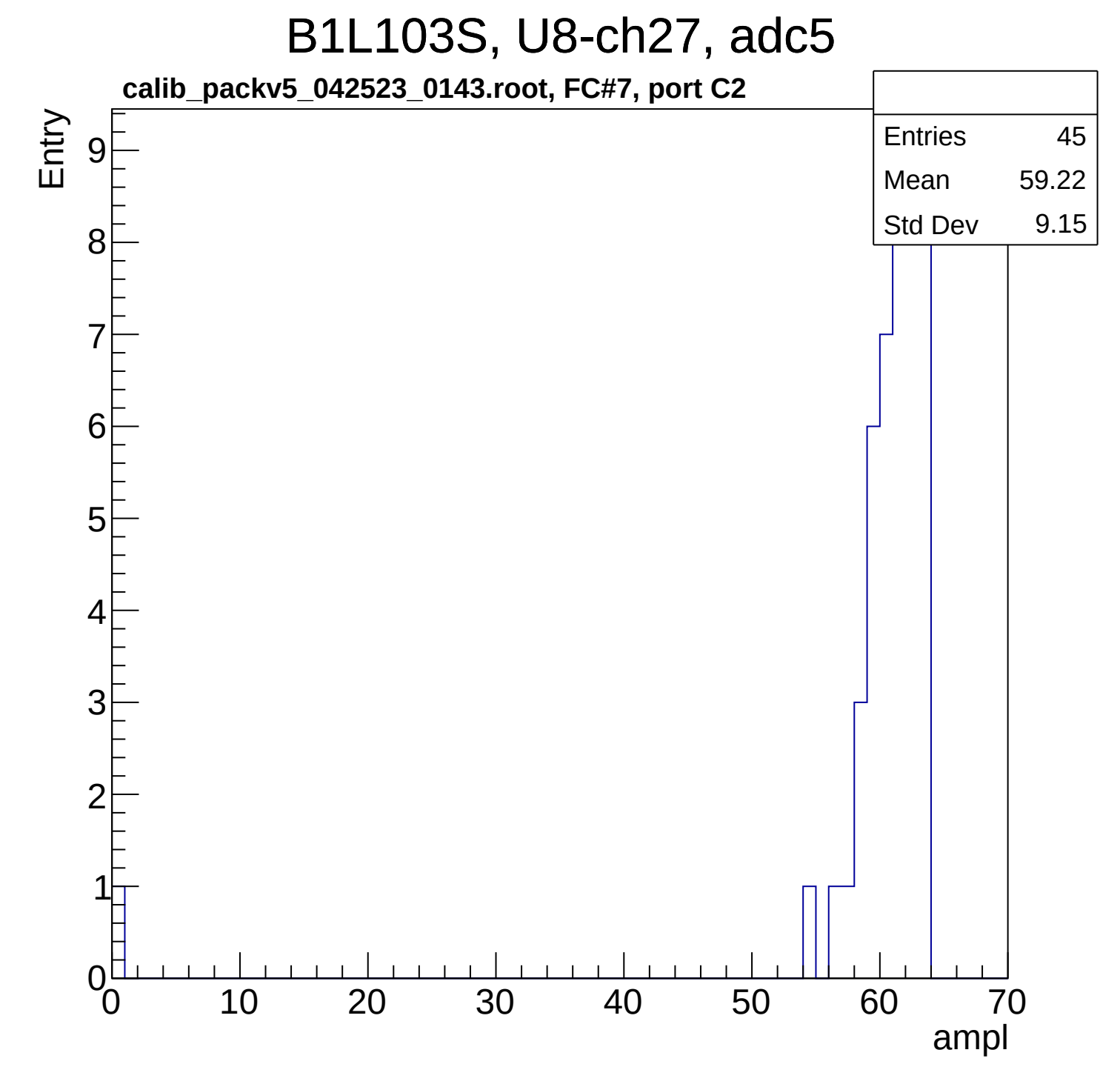

B1L103S, U8-ch27, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 89
Mean 28.89
Std Dev 6.514
Gaus mean : 30.3789
Gaus Width: 3.5897
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

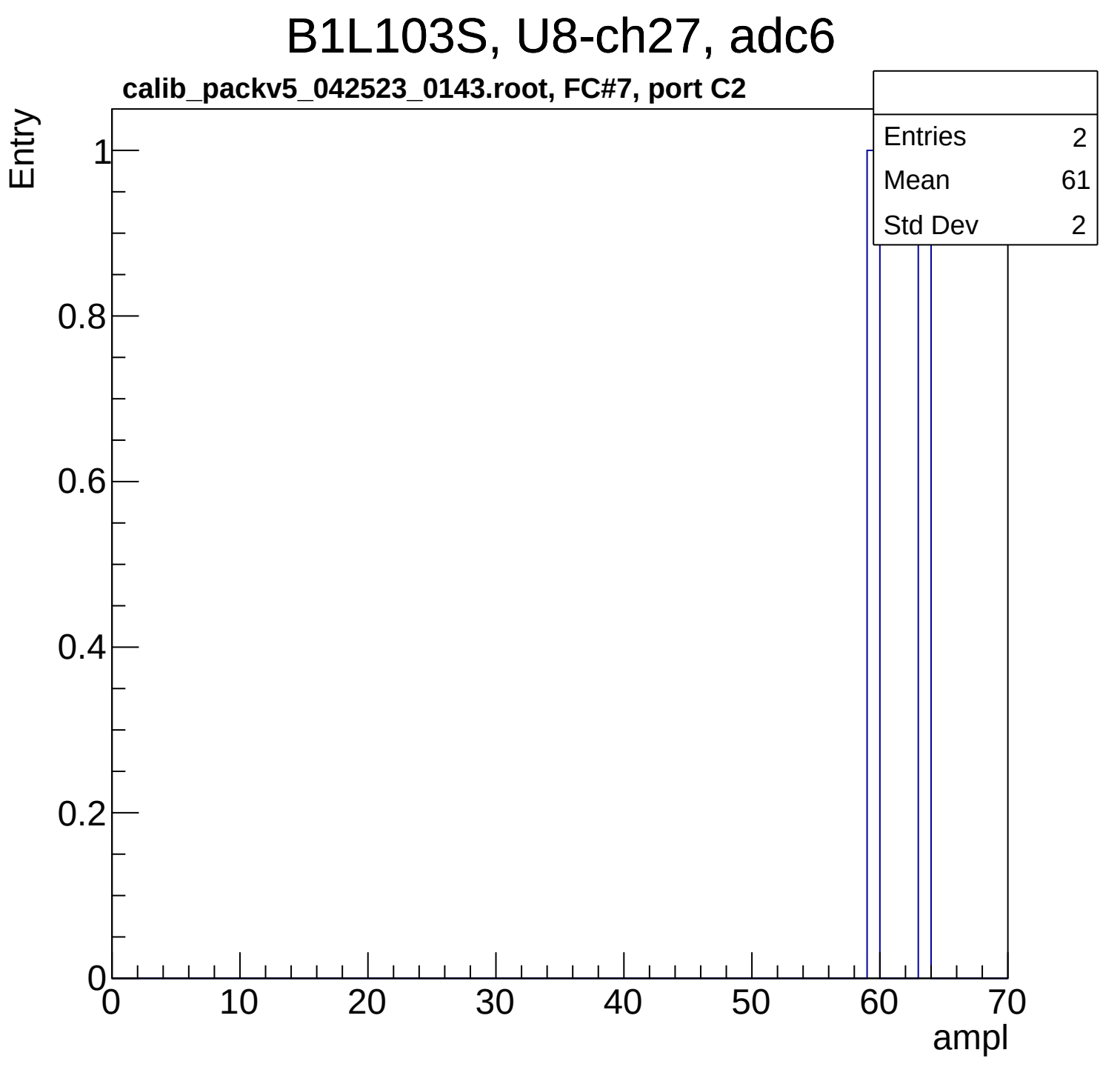

B1L103S, U8-ch27, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 37.8
Std Dev 2.932
Gaus mean : 38.3085
Gaus Width: 3.3984
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

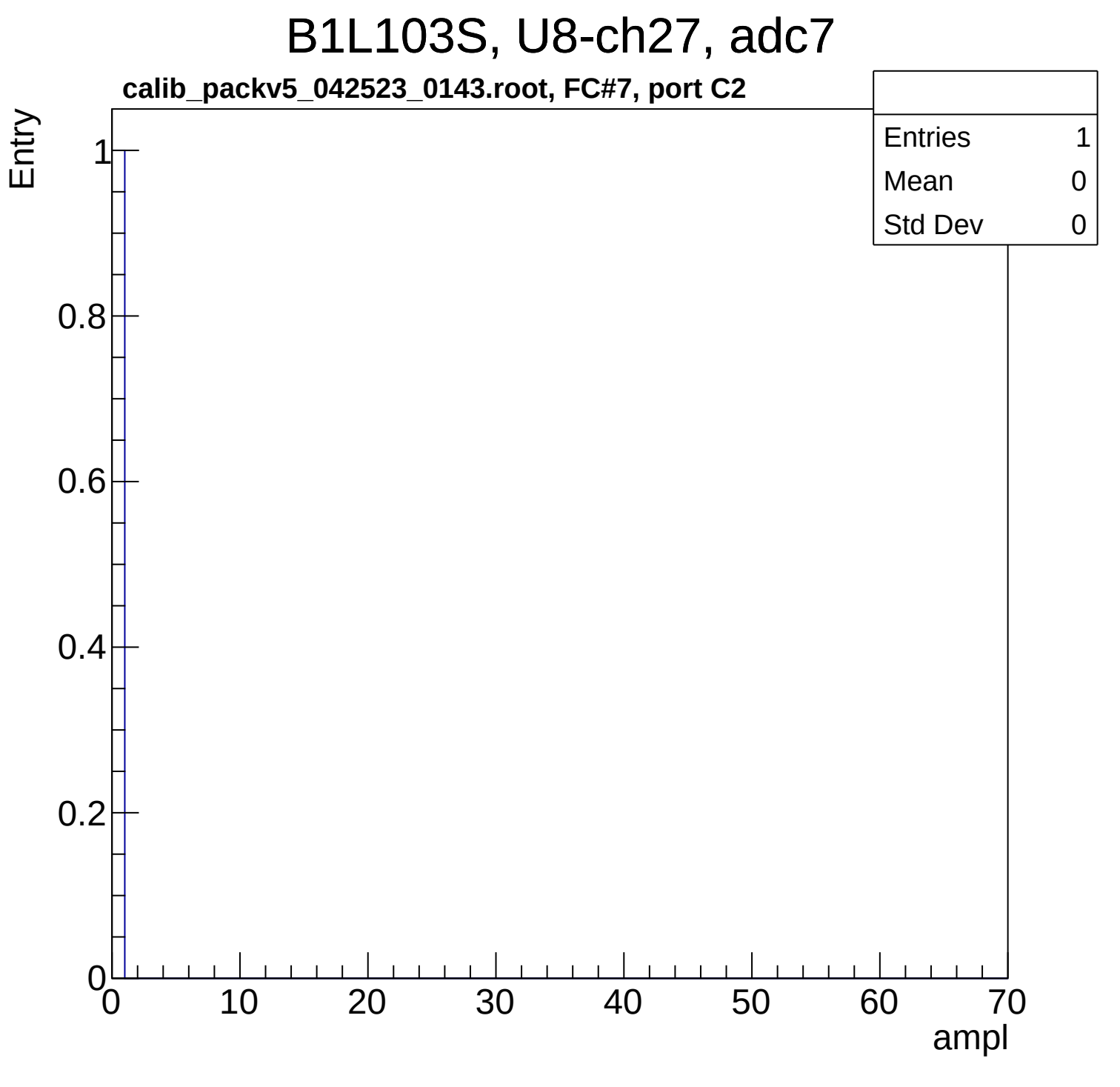

B1L103S, U8-ch27, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 44.22
Std Dev 2.859
Gaus mean : 44.5420
Gaus Width: 2.9366
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

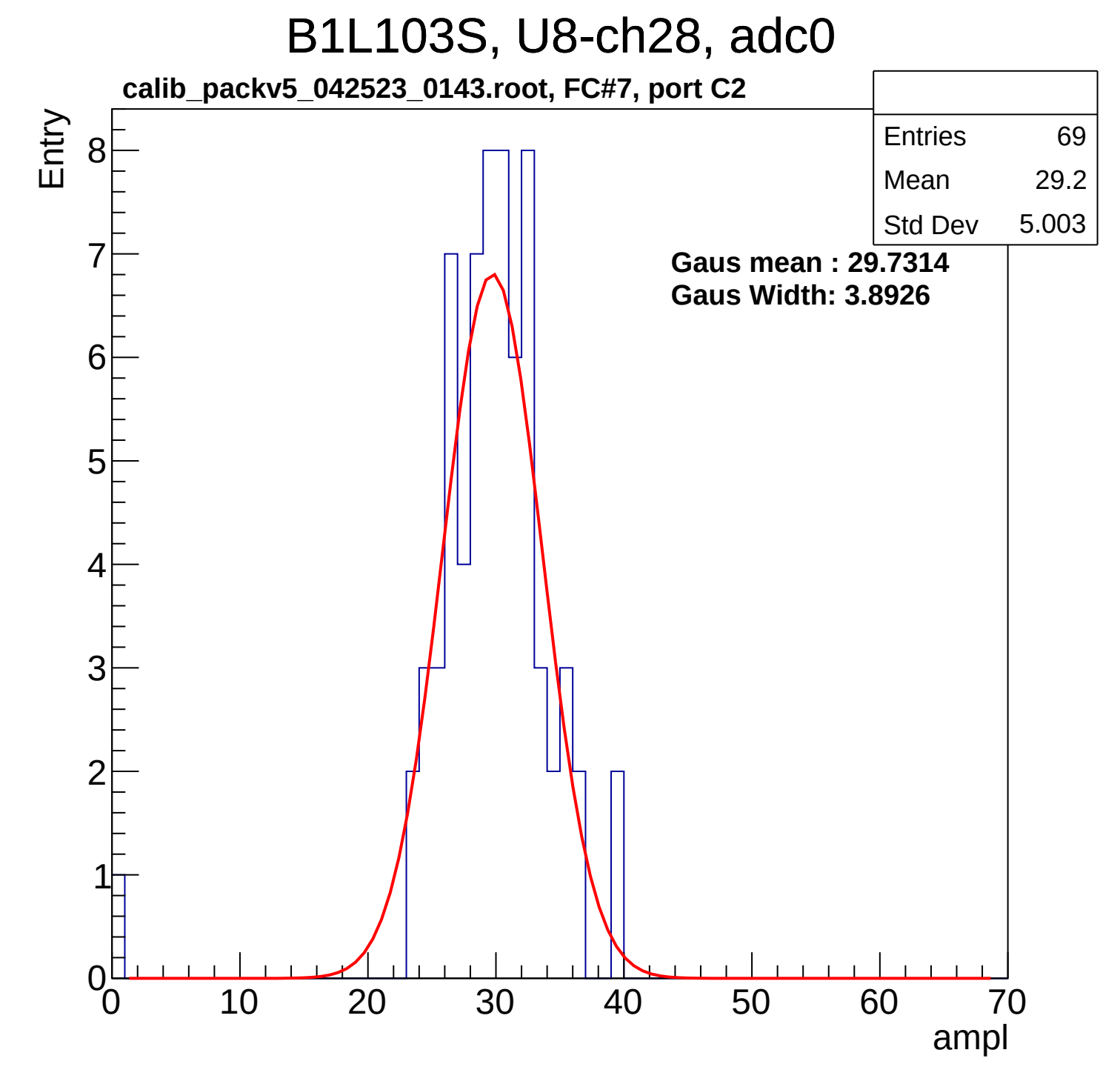

B1L103S, U8-ch27, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 50.42
Std Dev 3.464
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

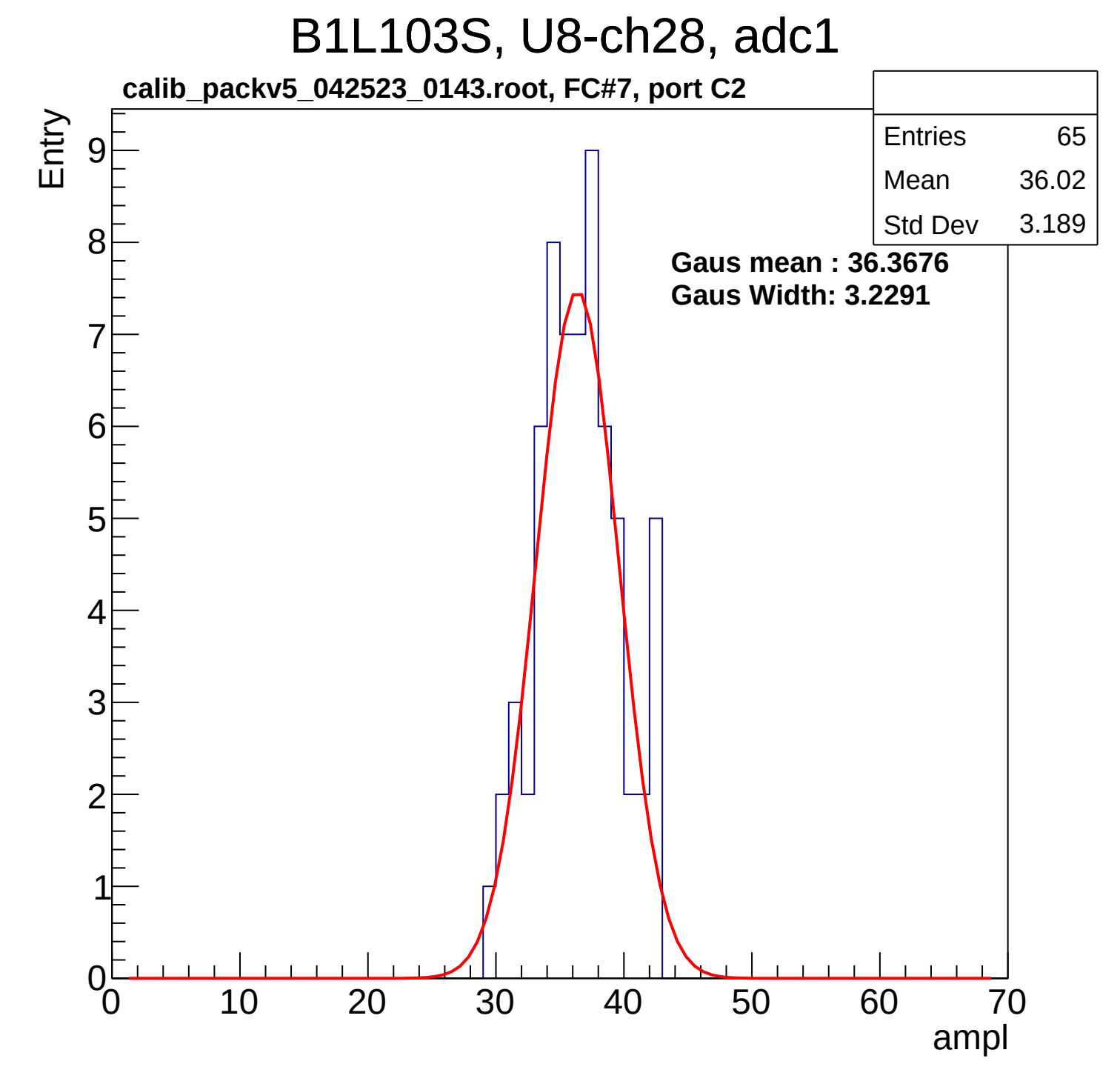

B1L103S, U8-ch27, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 56.31
Std Dev 2.924
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

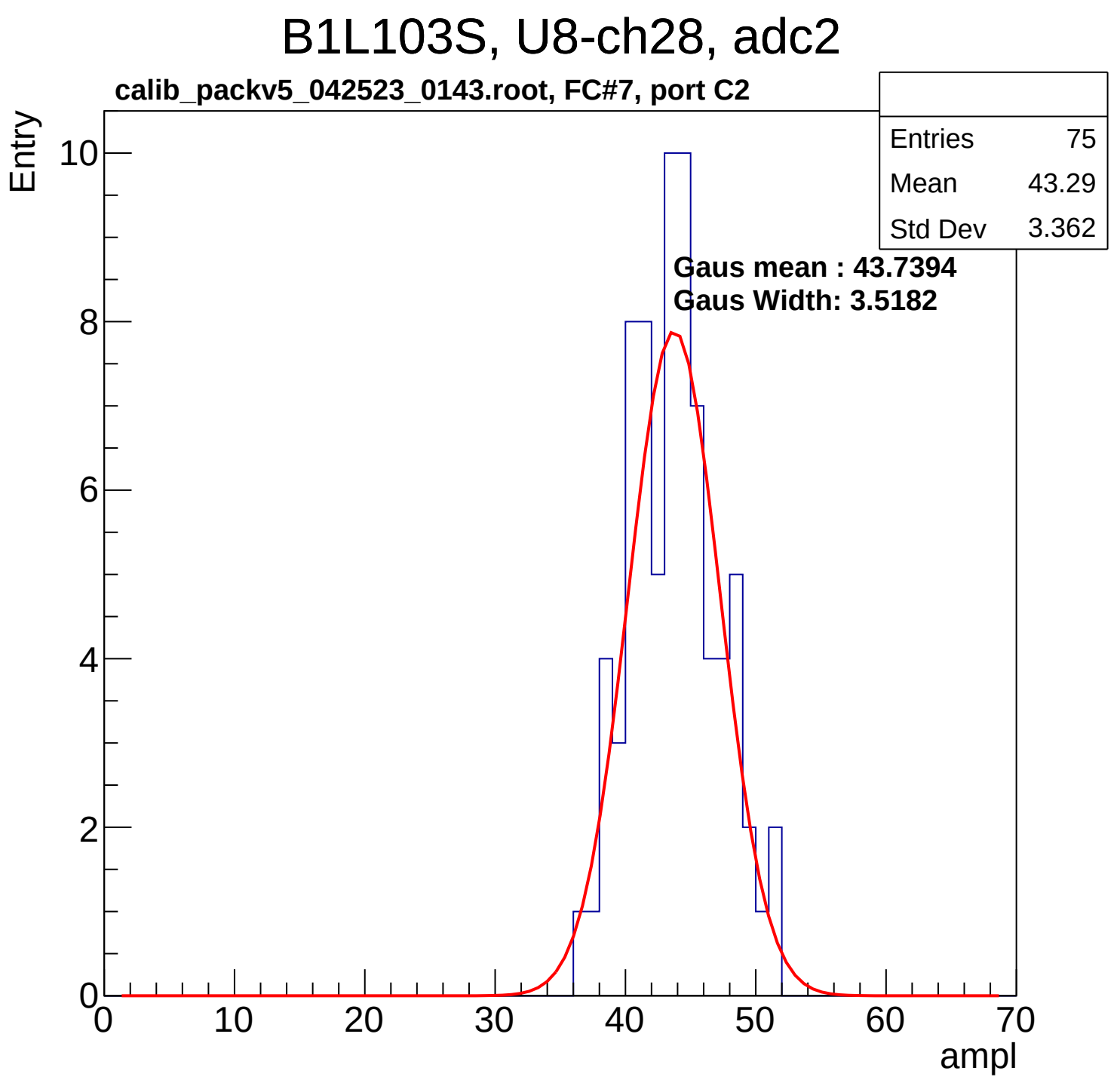

B1L103S, U8-ch27, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 45
Mean 59.22
Std Dev 9.15
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

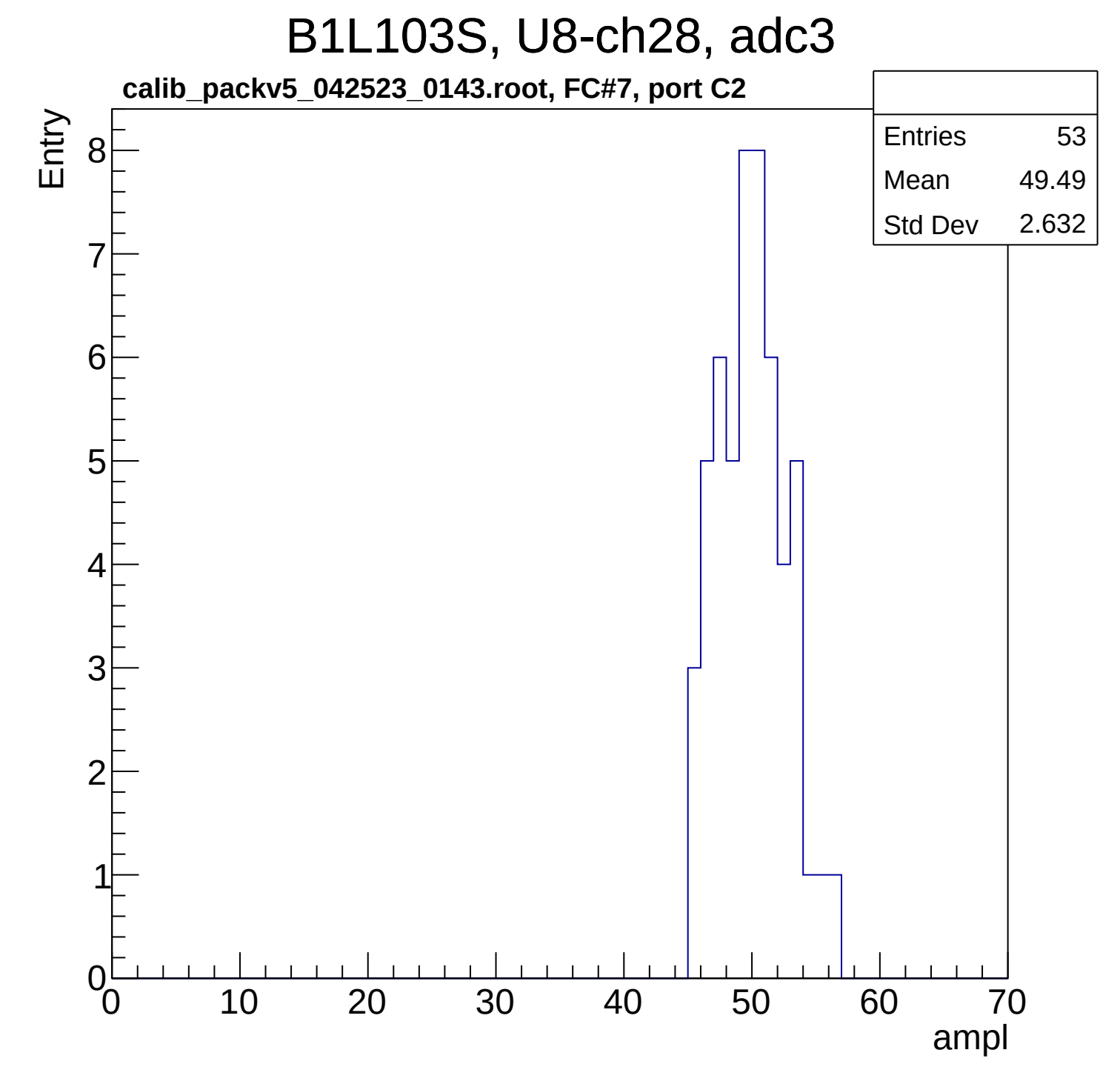

B1L103S, U8-ch27, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 61
Std Dev 2
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

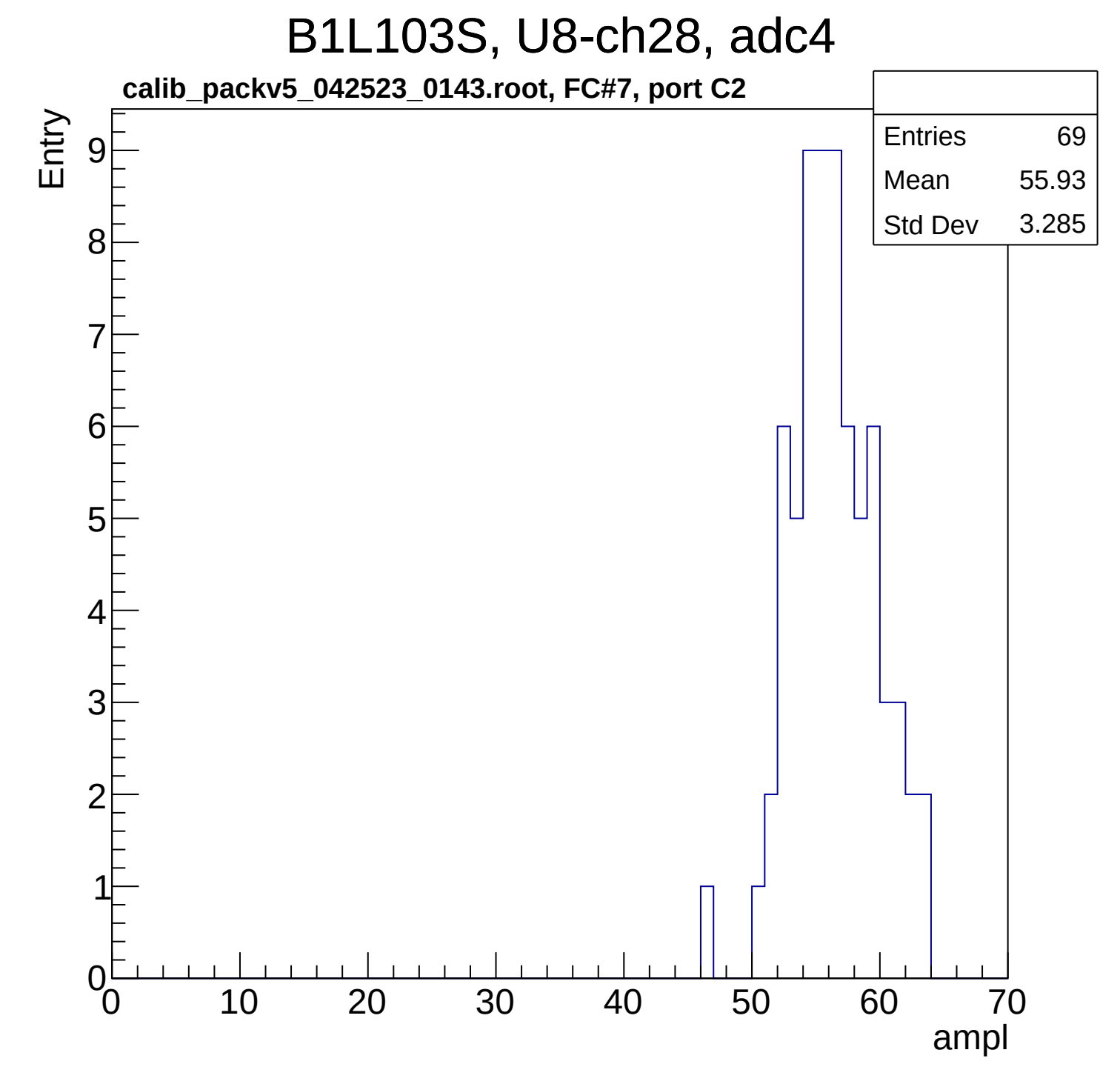

B1L103S, U8-ch27, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

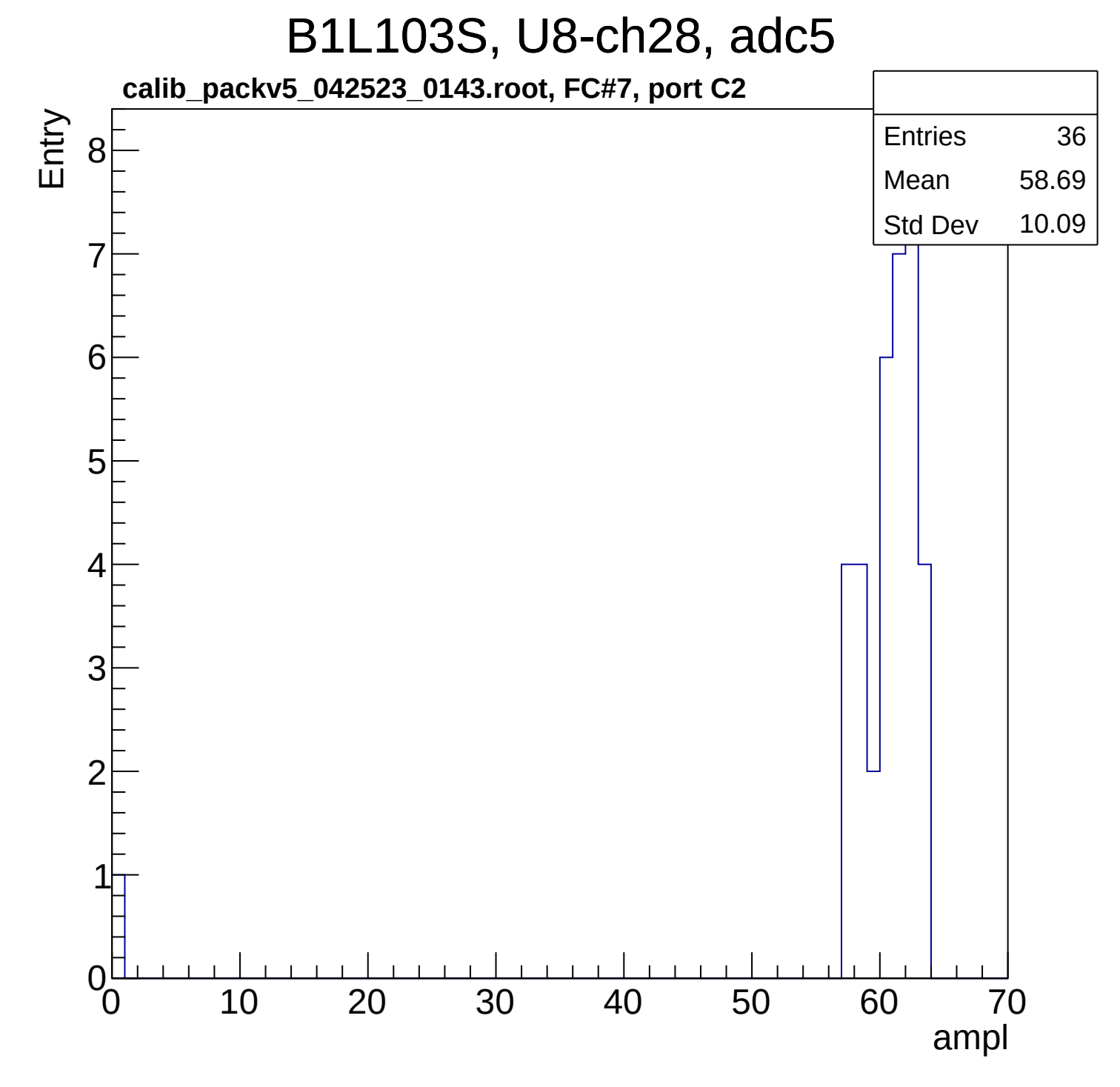

B1L103S, U8-ch28, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 29.2
Std Dev 5.003
Gaus mean : 29.7314
Gaus Width: 3.8926
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

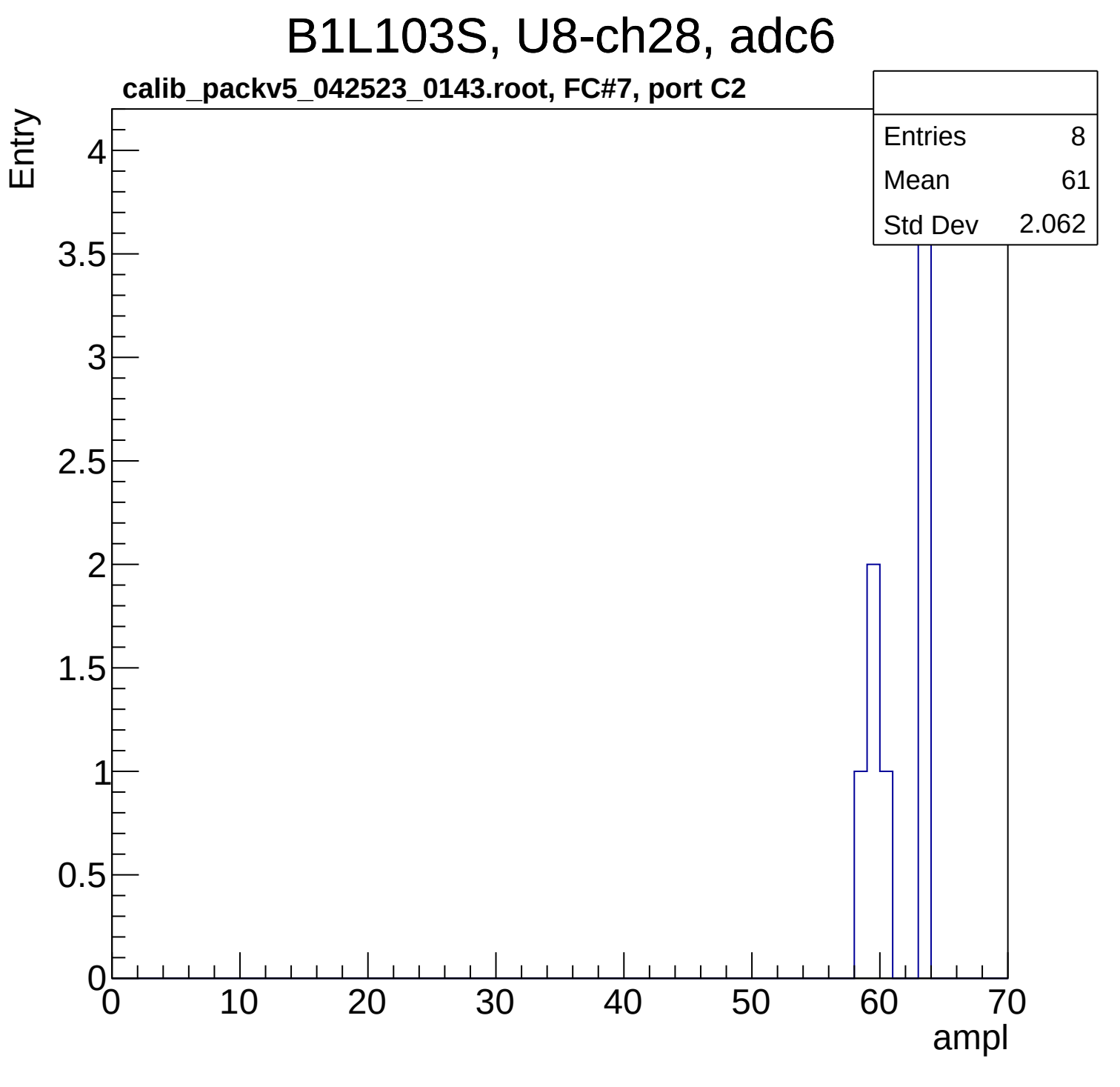

B1L103S, U8-ch28, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 36.02
Std Dev 3.189
Gaus mean : 36.3676
Gaus Width: 3.2291
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

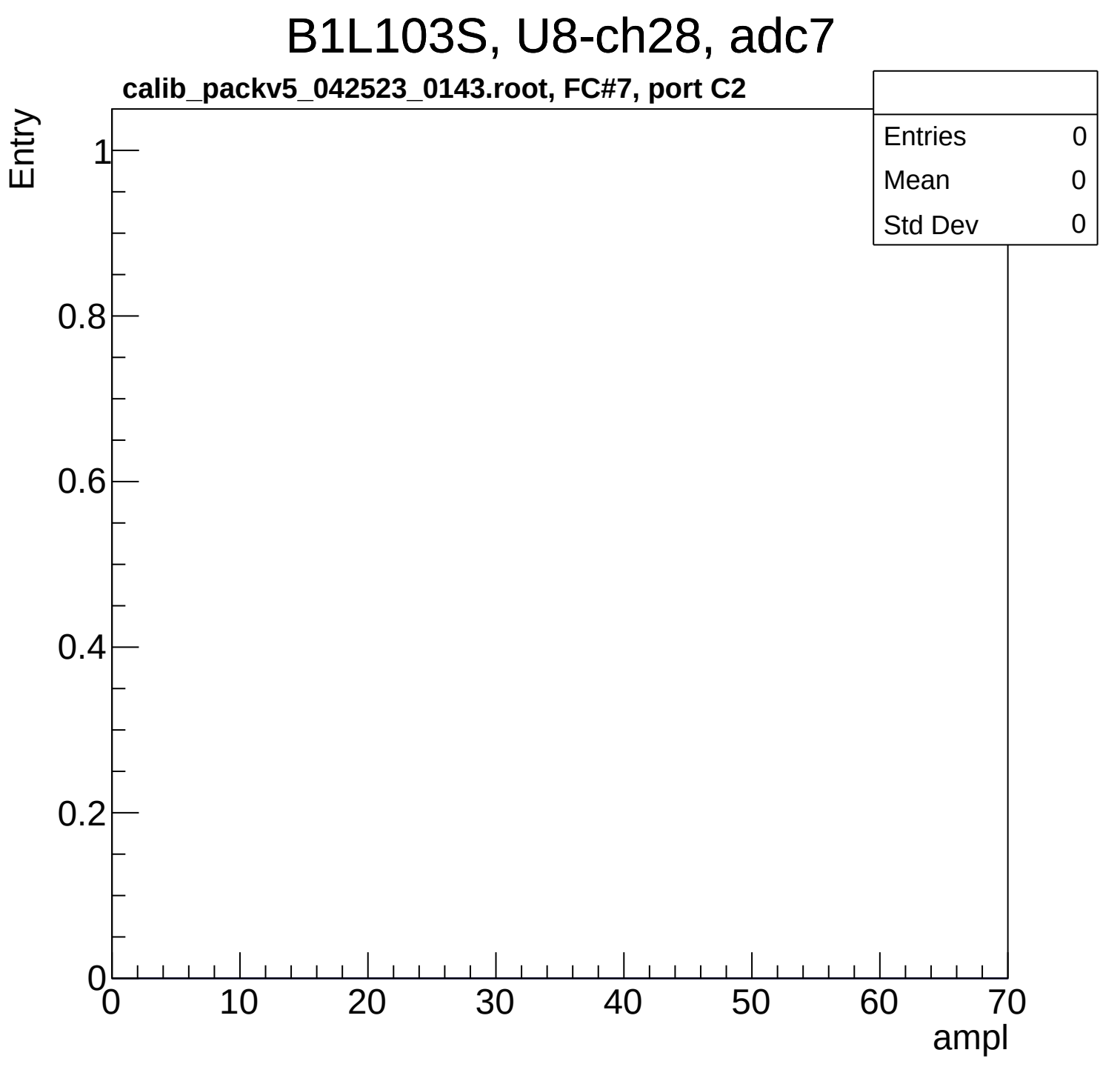

B1L103S, U8-ch28, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 43.29
Std Dev 3.362
Gaus mean : 43.7394
Gaus Width: 3.5182
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

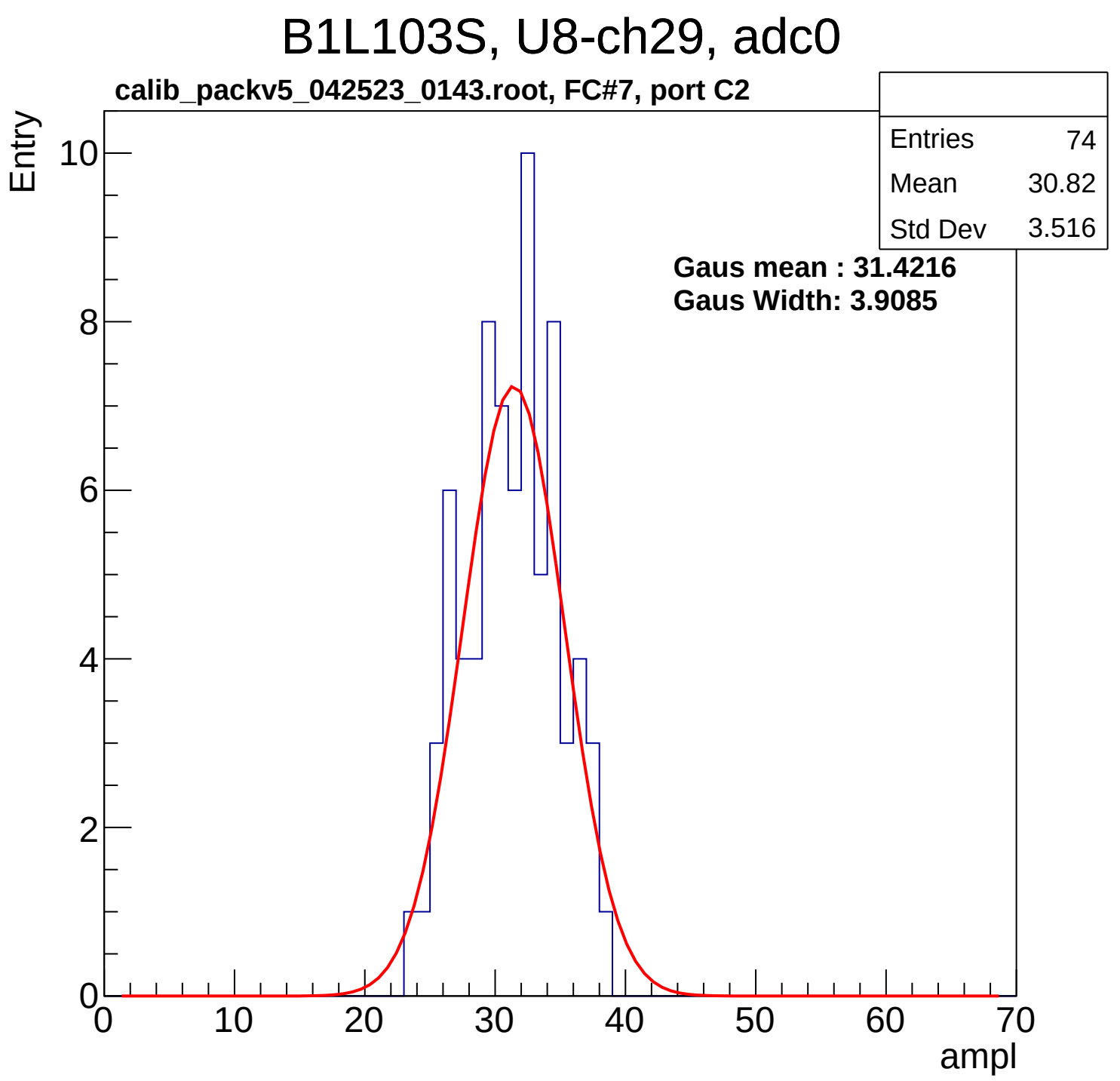

B1L103S, U8-ch28, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 49.49
Std Dev 2.632
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

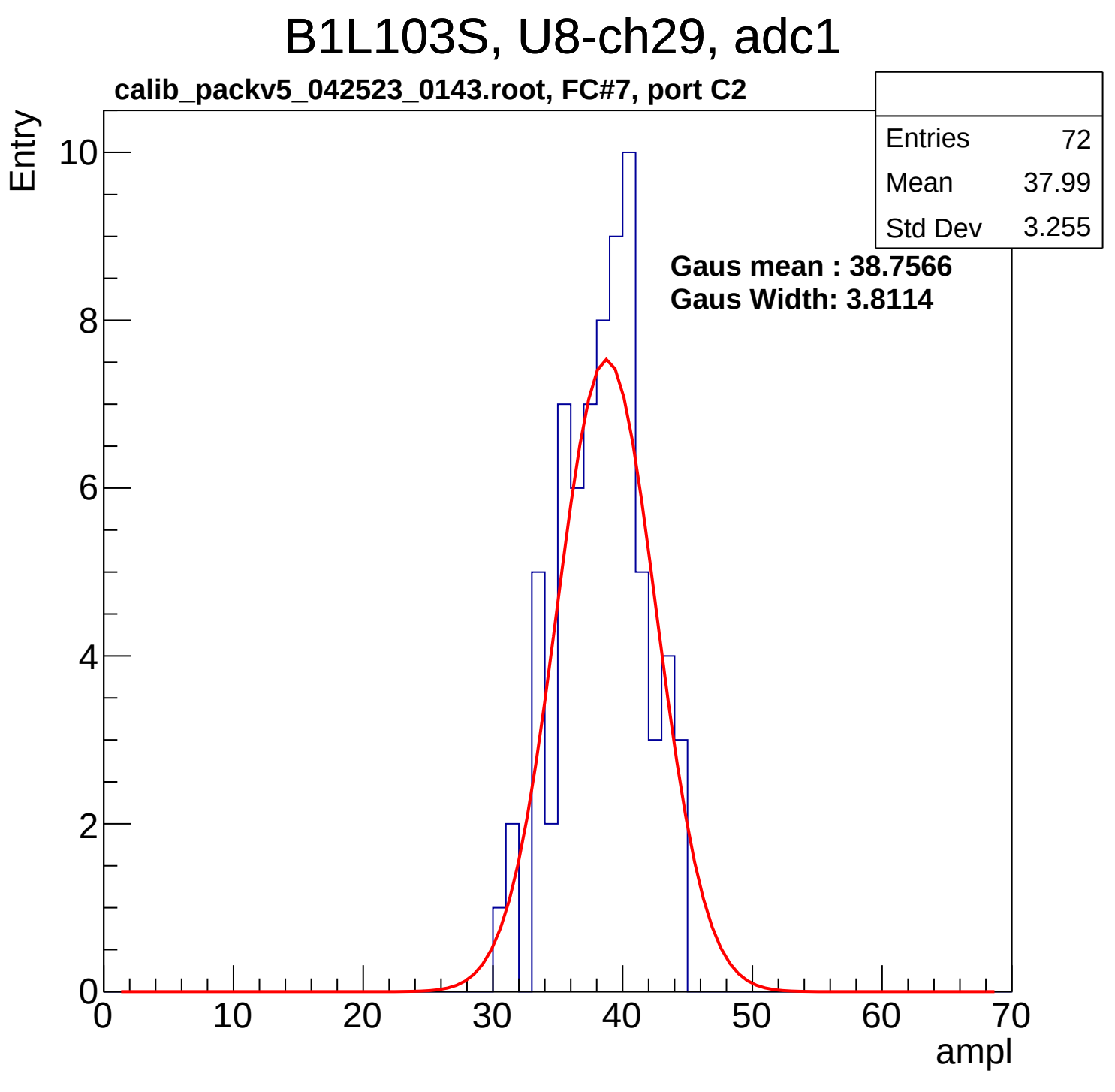

B1L103S, U8-ch28, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 55.93
Std Dev 3.285
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

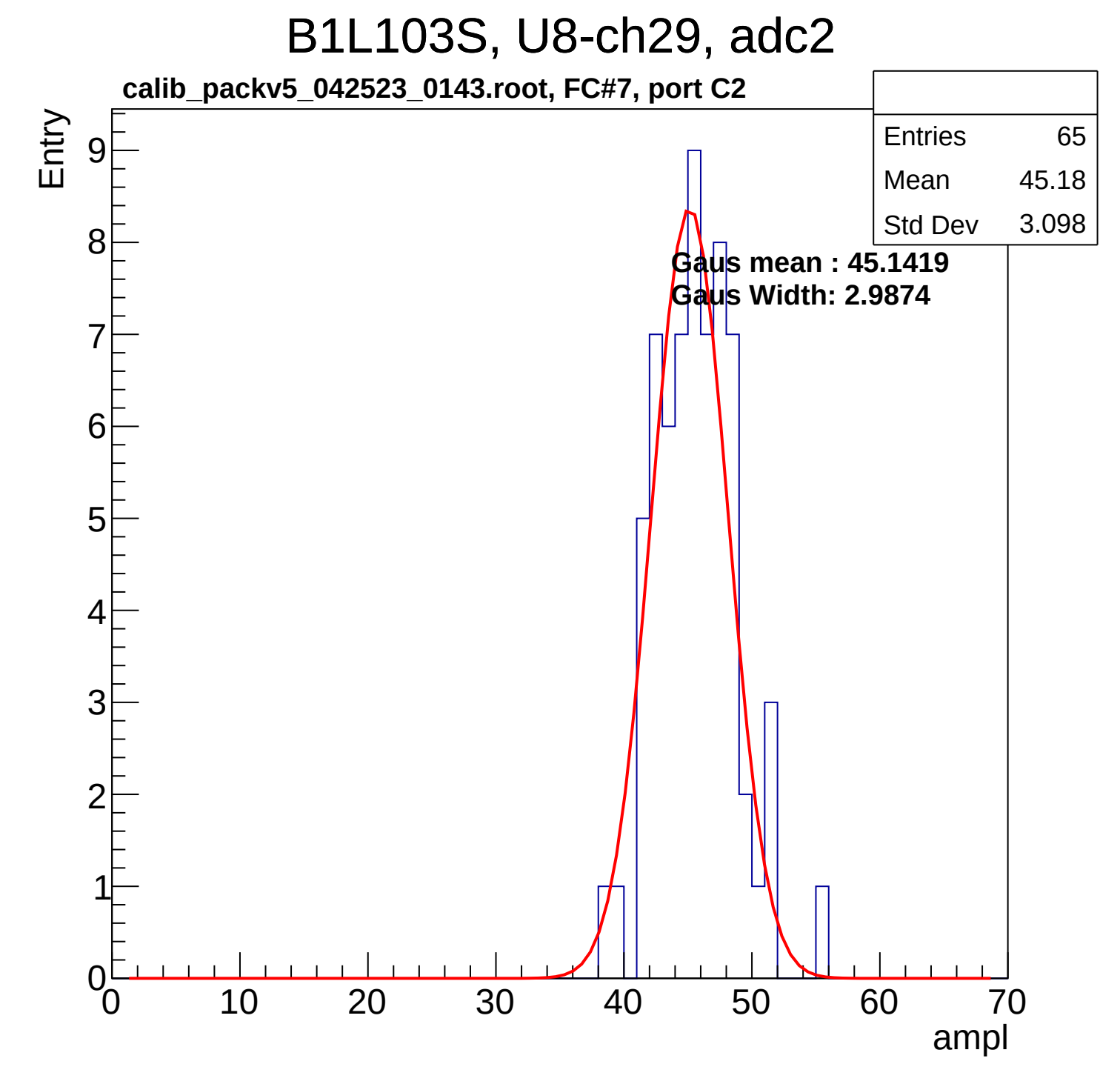

B1L103S, U8-ch28, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 36
Mean 58.69
Std Dev 10.09
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

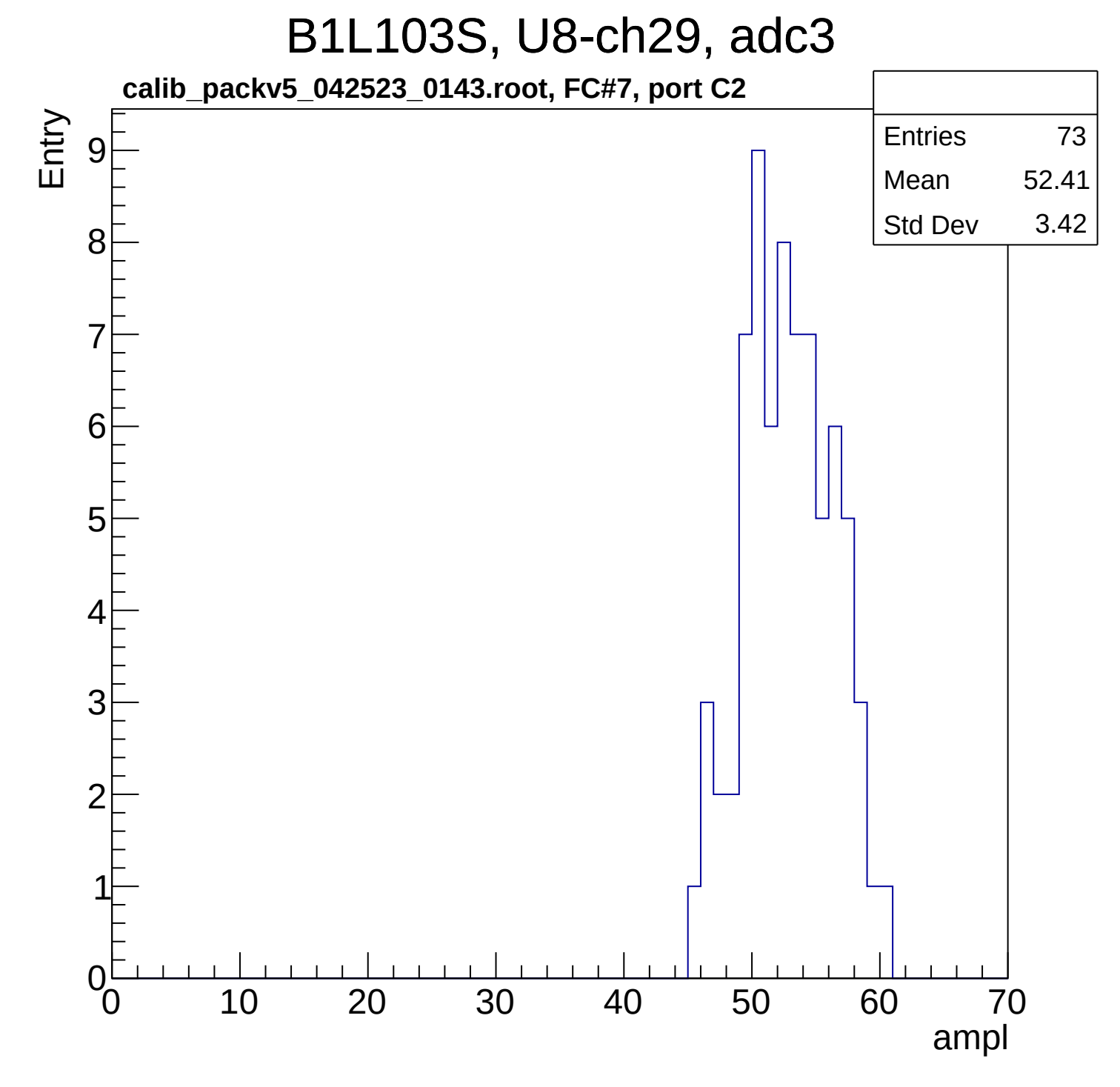

B1L103S, U8-ch28, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 8
Mean 61
Std Dev 2.062
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

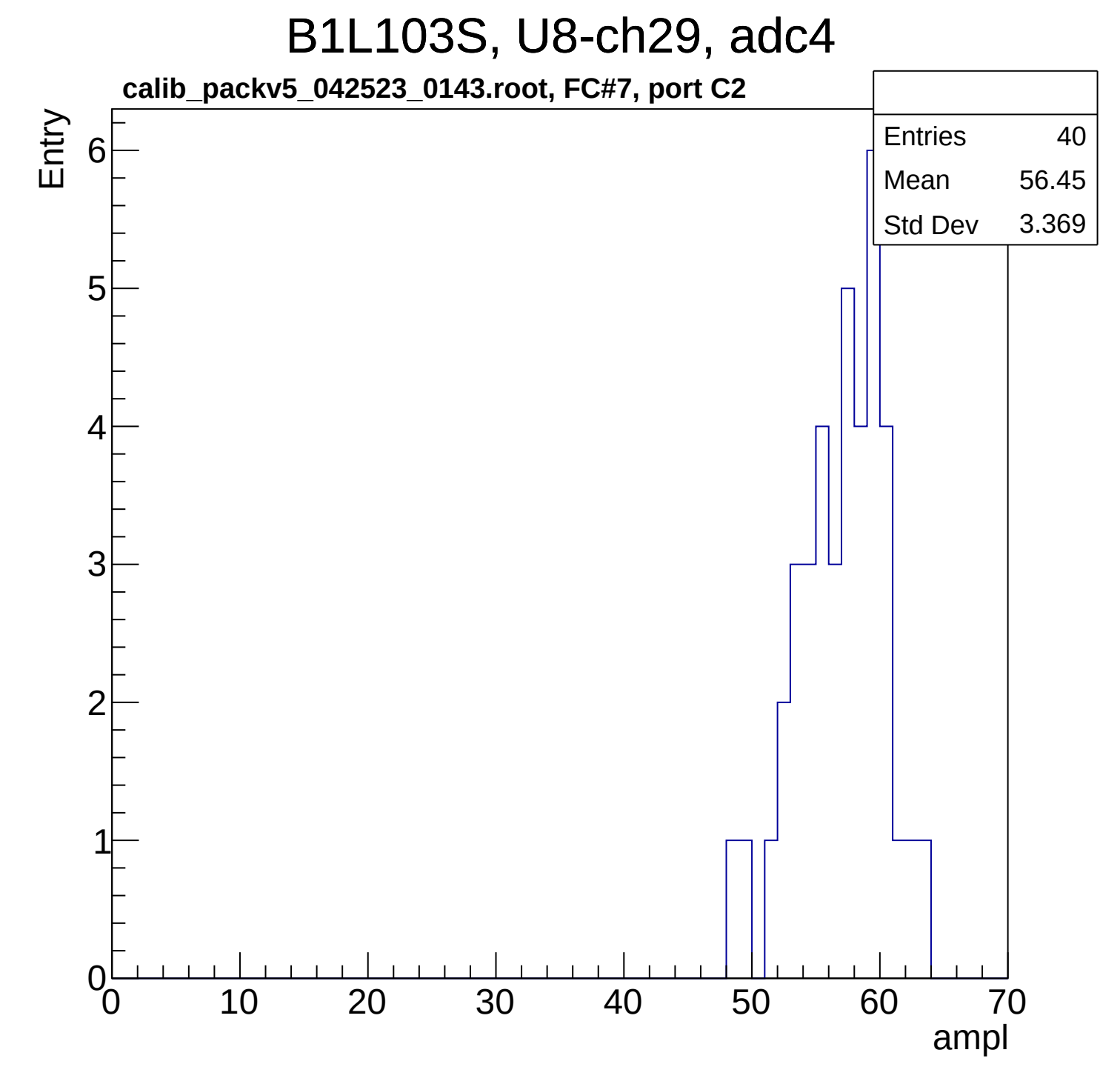

B1L103S, U8-ch28, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

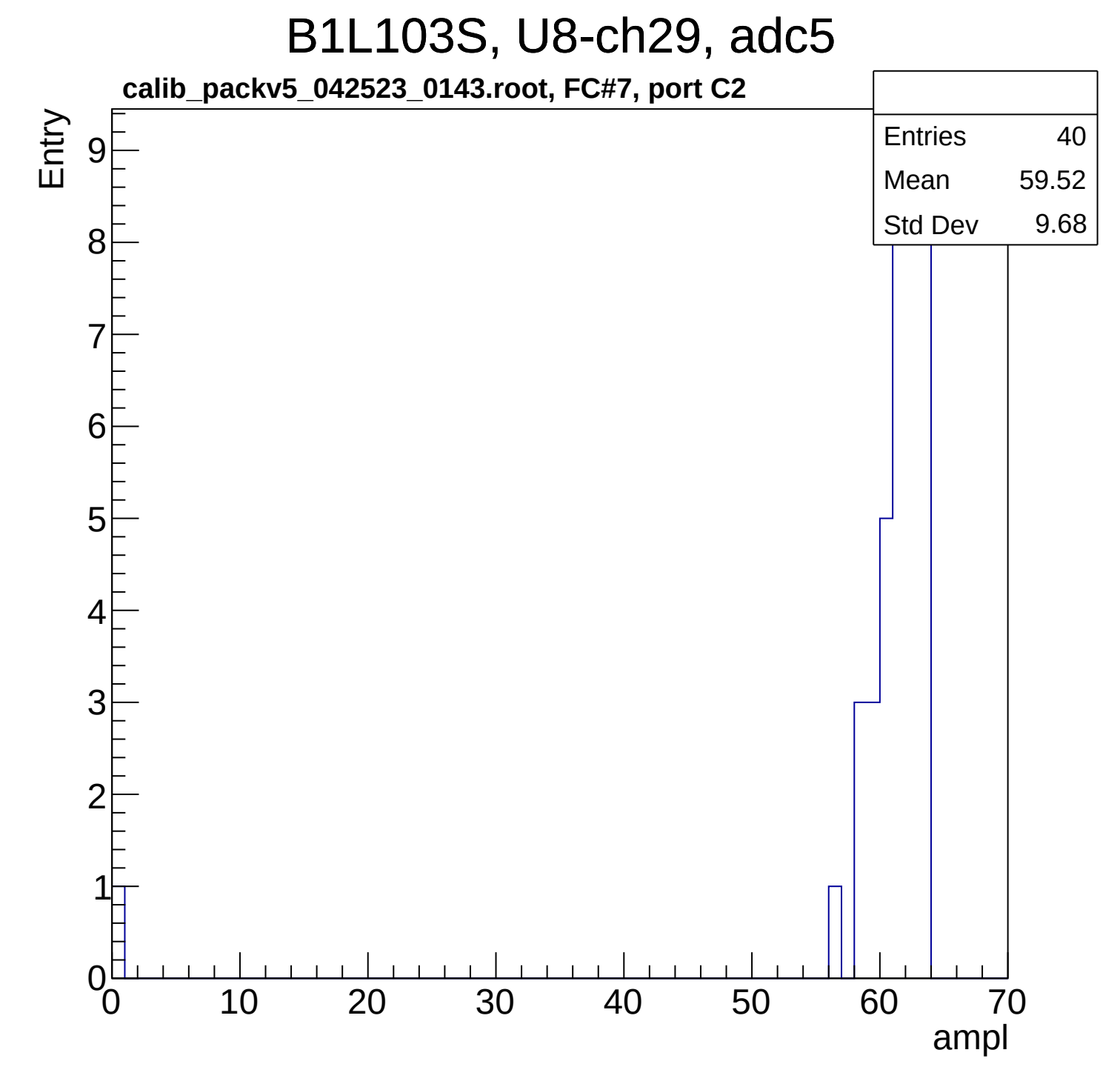

B1L103S, U8-ch29, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 30.82
Std Dev 3.516
Gaus mean : 31.4216
Gaus Width: 3.9085
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

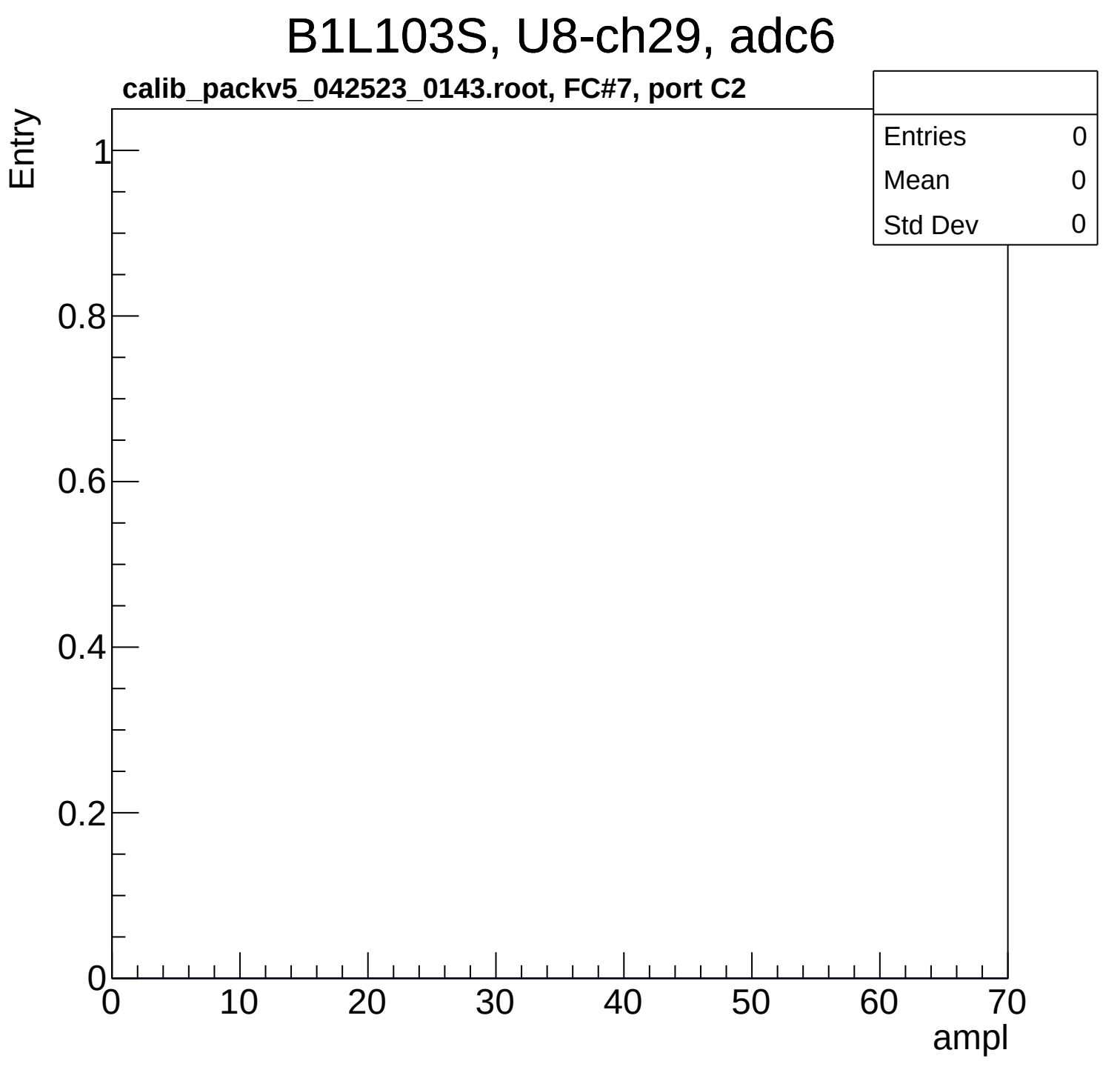

B1L103S, U8-ch29, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 37.99
Std Dev 3.255
Gaus mean : 38.7566
Gaus Width: 3.8114
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

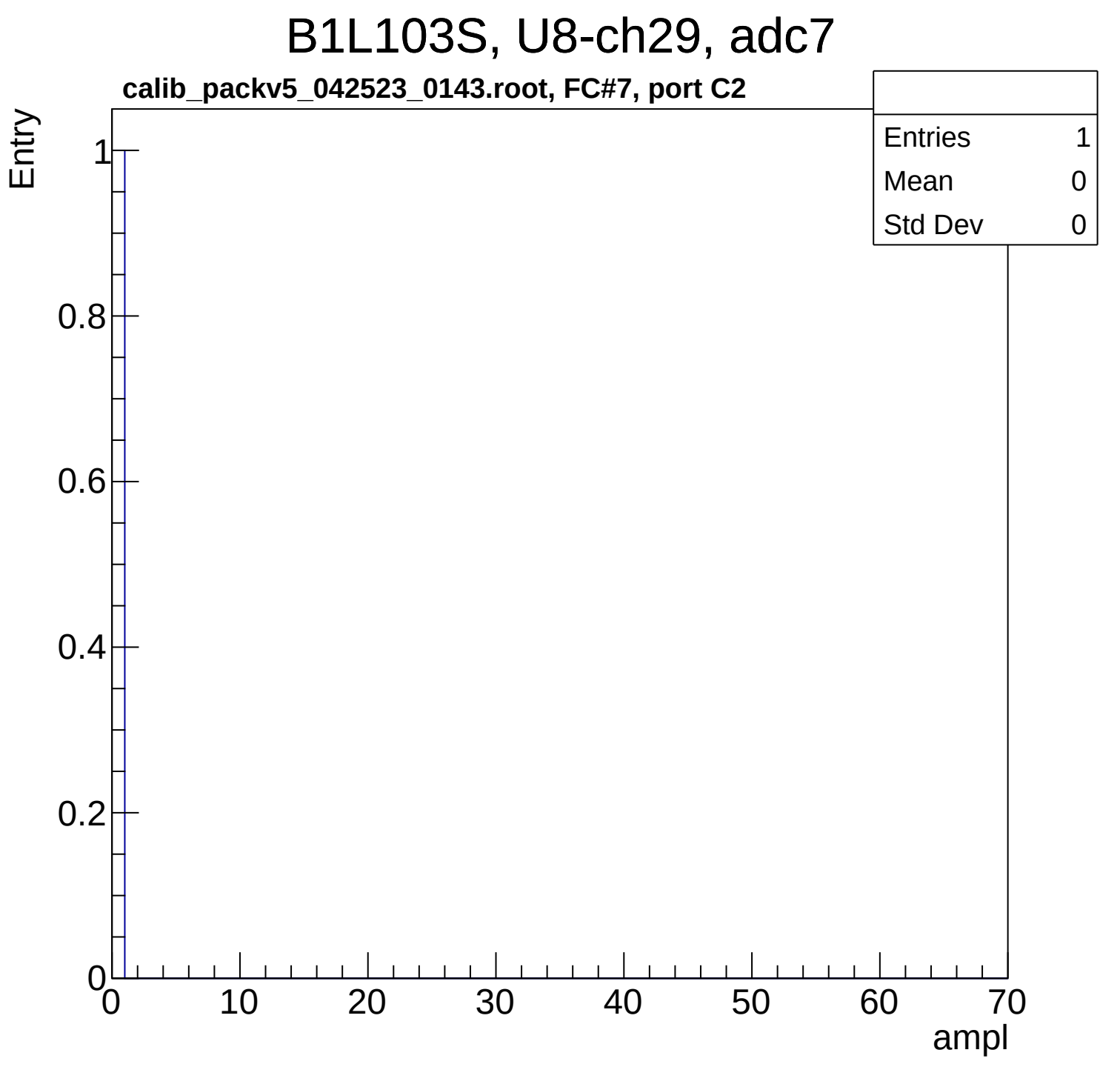

B1L103S, U8-ch29, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 45.18
Std Dev 3.098
Gaus mean : 45.1419
Gaus Width: 2.9874
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

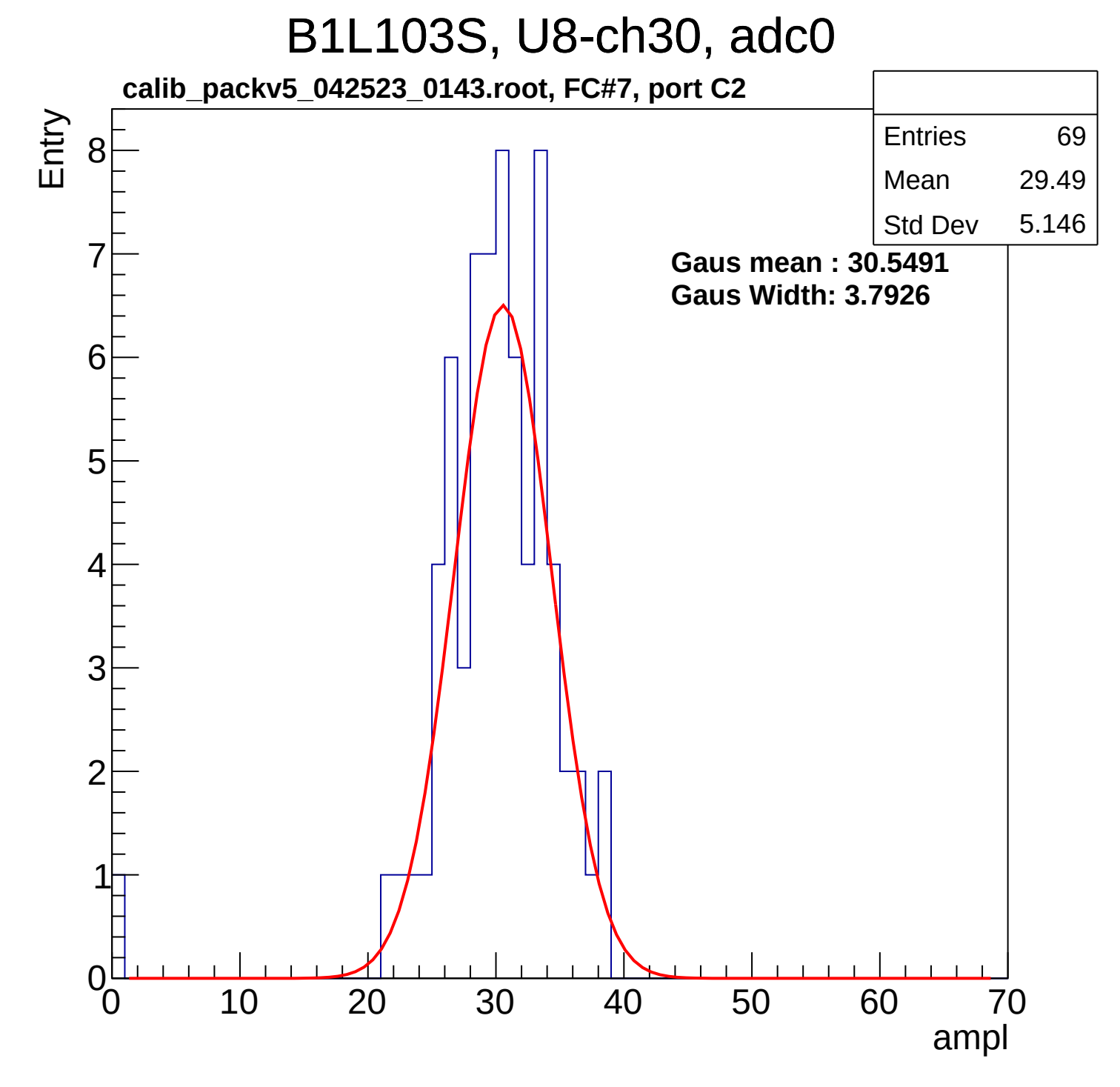

B1L103S, U8-ch29, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 52.41
Std Dev 3.42
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

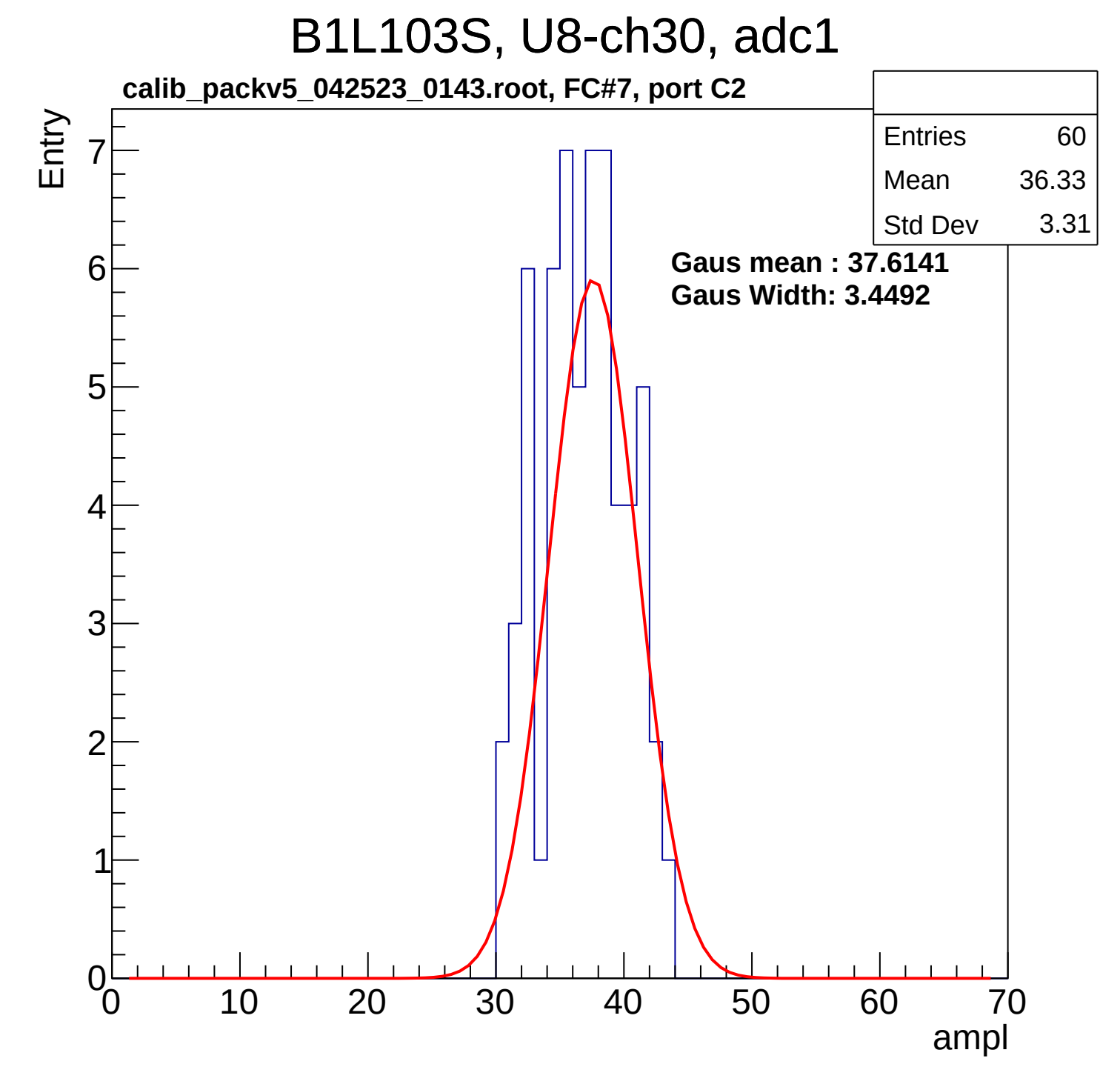

B1L103S, U8-ch29, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 40
Mean 56.45
Std Dev 3.369
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

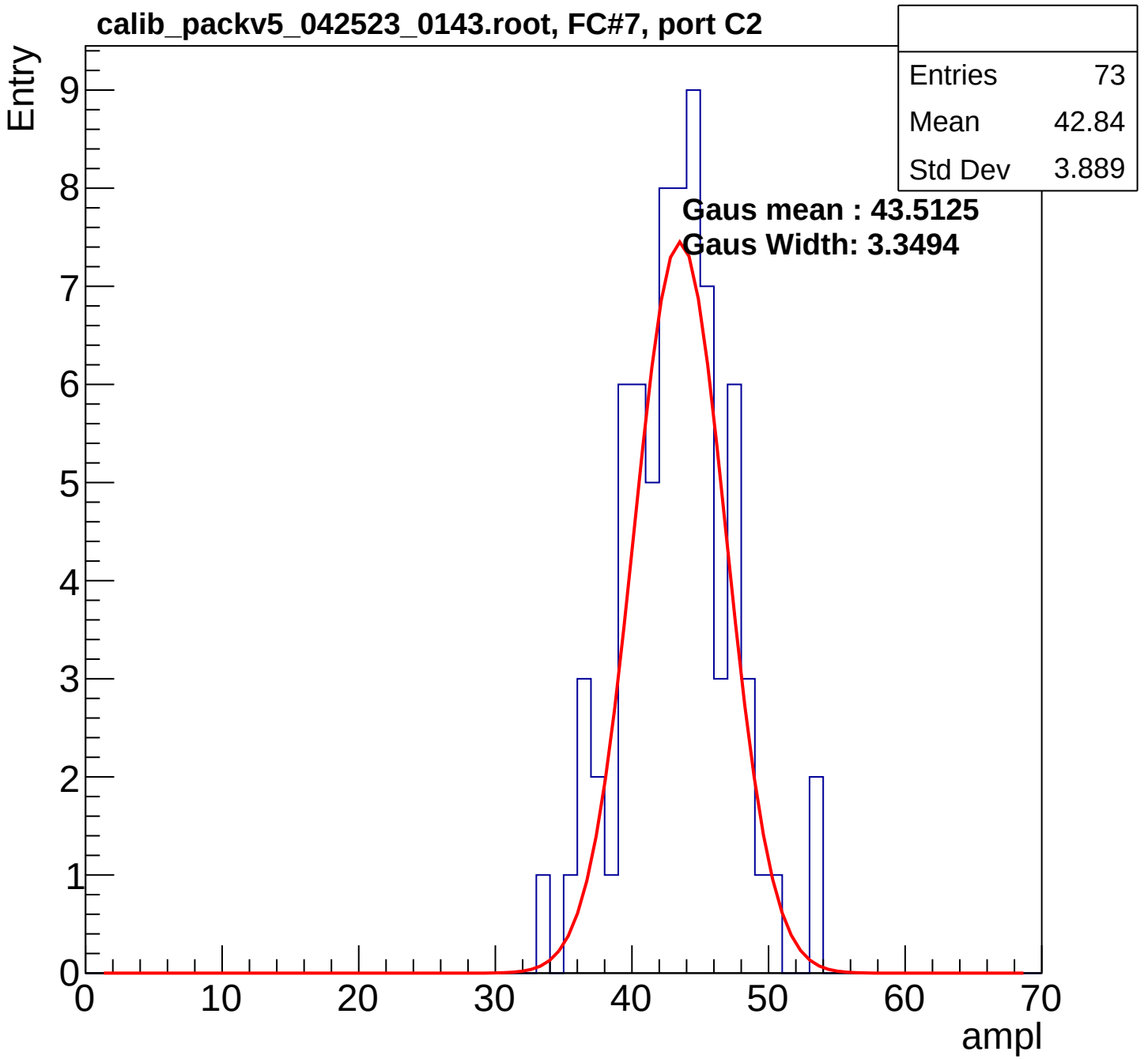

B1L103S, U8-ch29, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 40
Mean 59.52
Std Dev 9.68
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

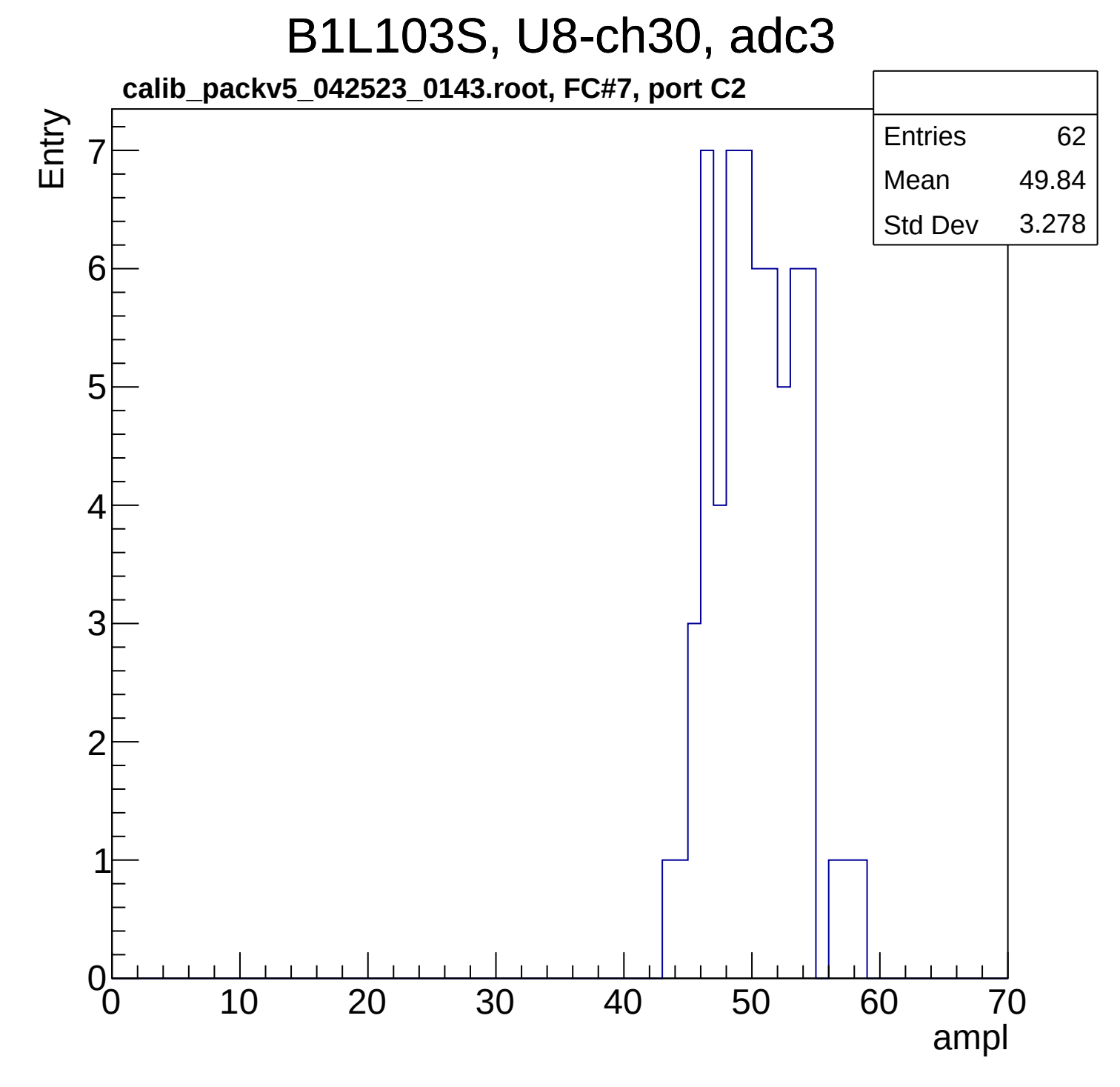

B1L103S, U8-ch29, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

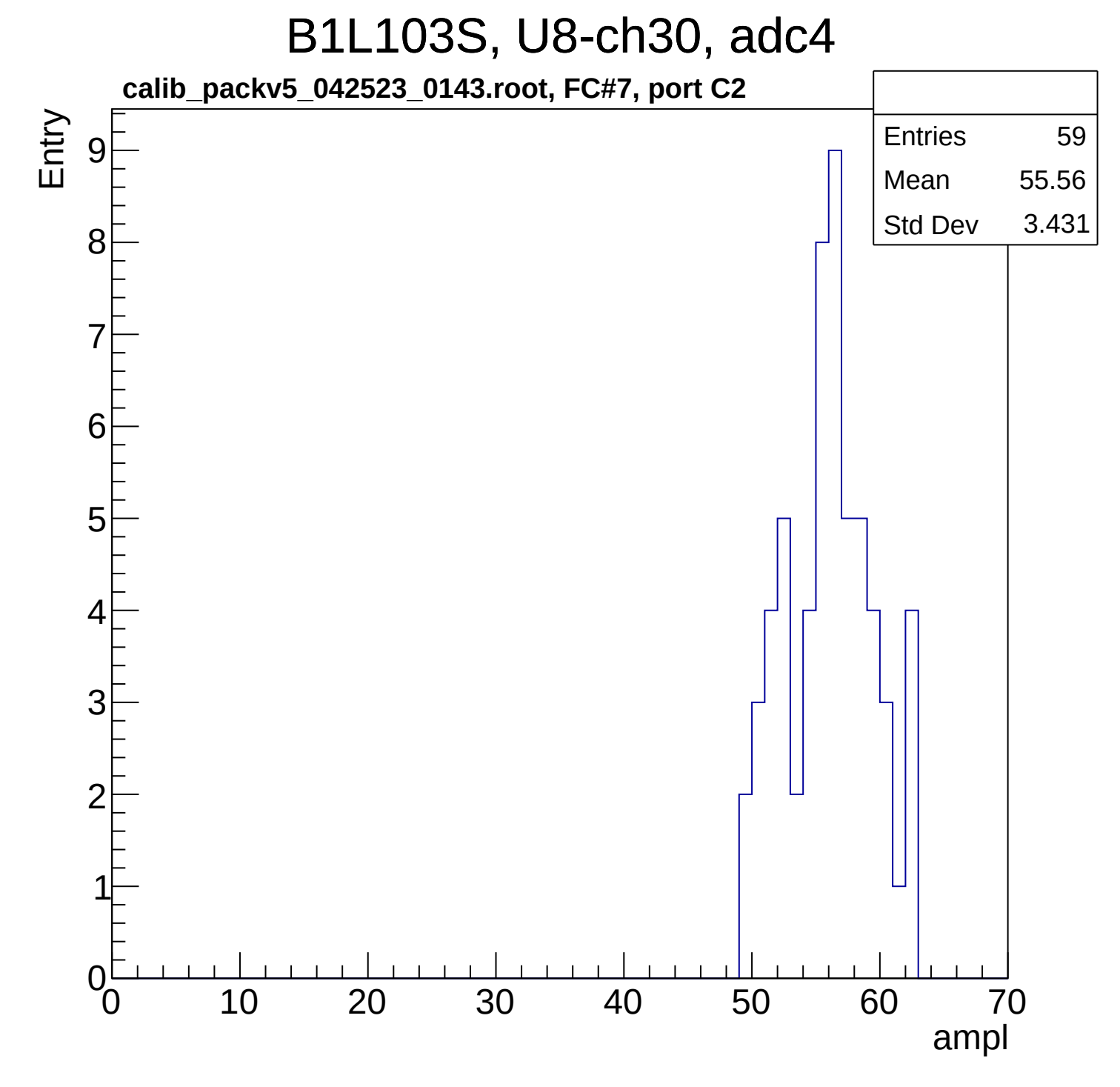

B1L103S, U8-ch29, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

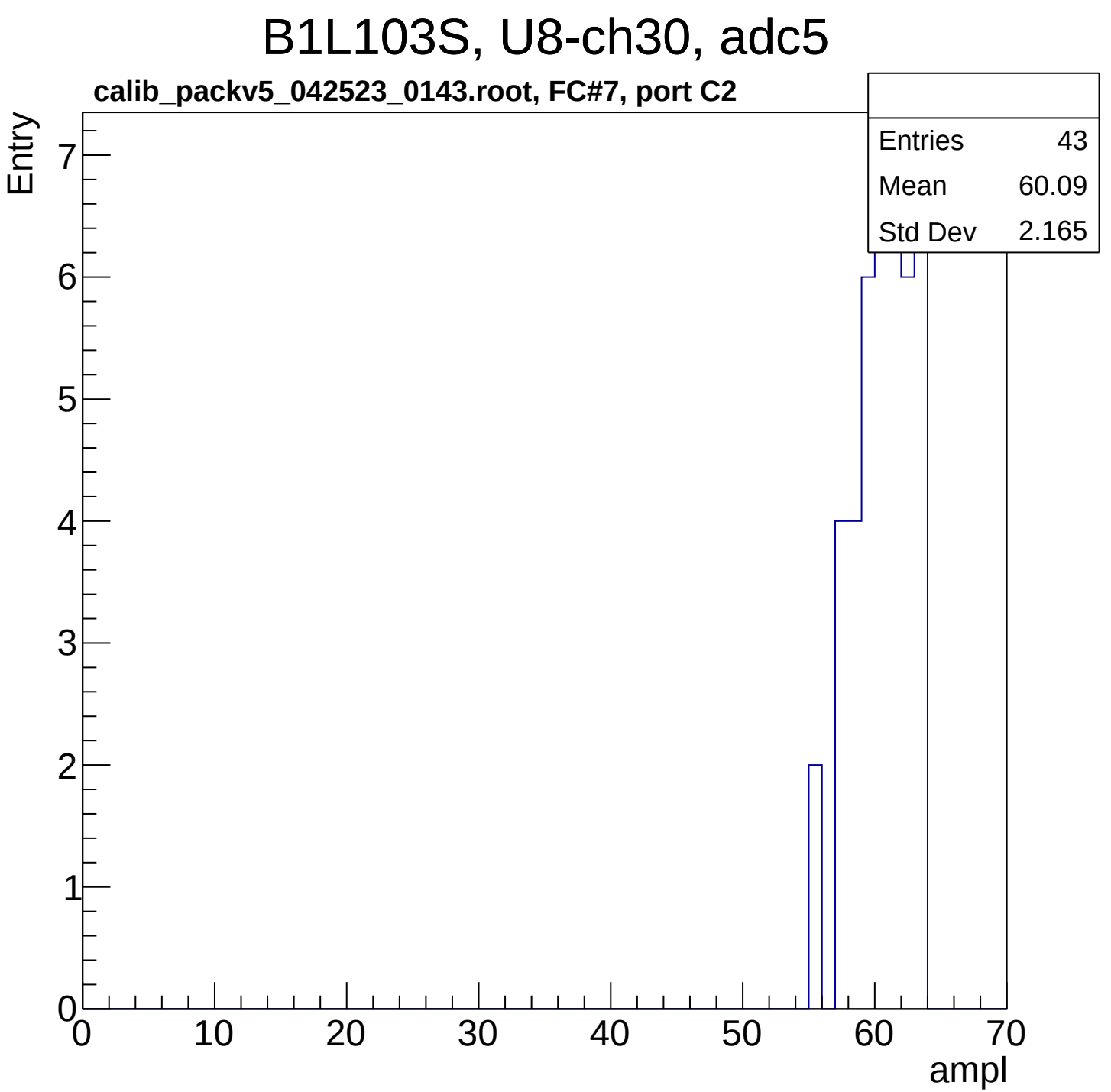

B1L103S, U8-ch30, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 29.49
Std Dev 5.146
Gaus mean : 30.5491
Gaus Width: 3.7926
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

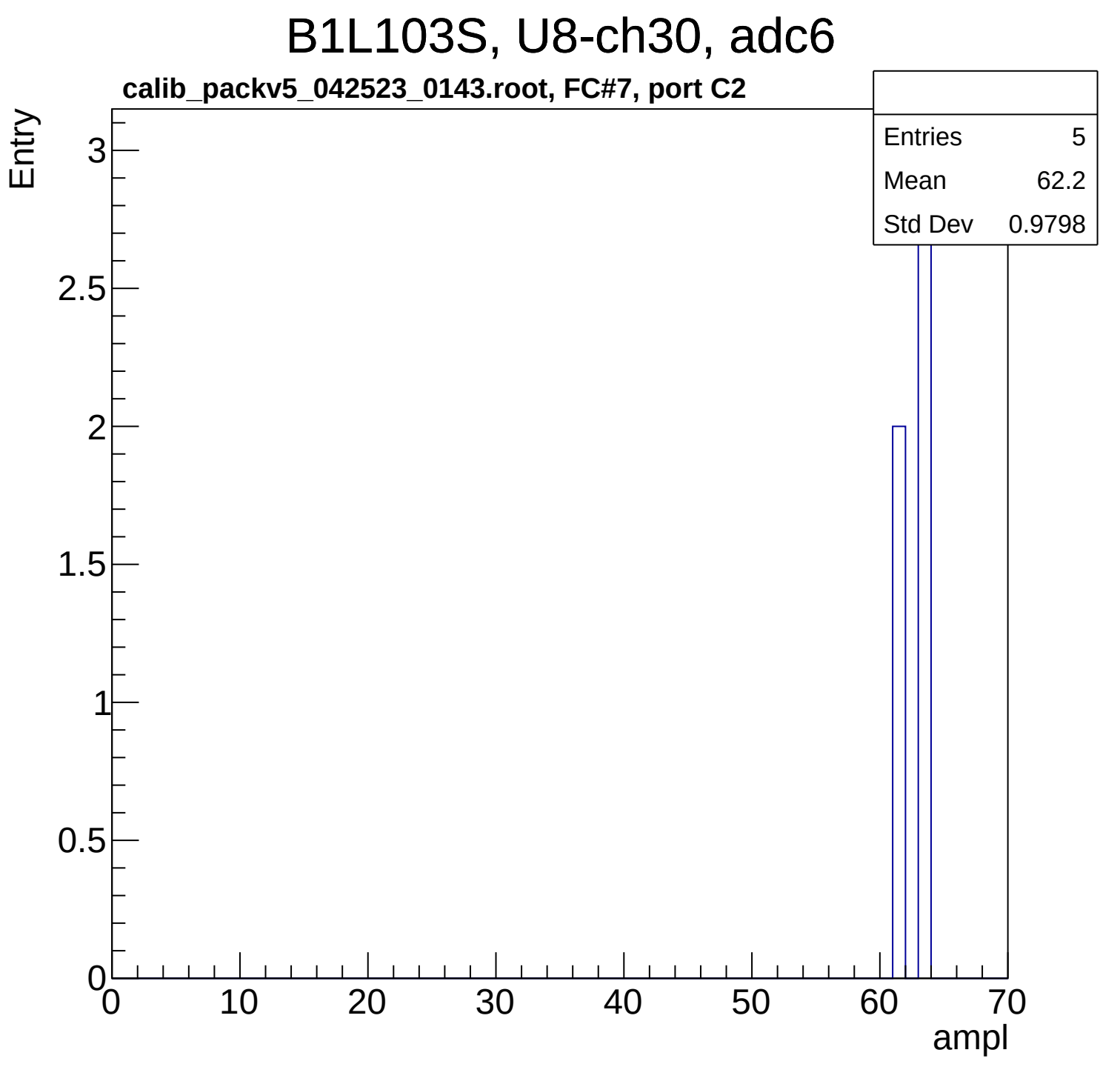

B1L103S, U8-ch30, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 36.33
Std Dev 3.31
Gaus mean : 37.6141
Gaus Width: 3.4492
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

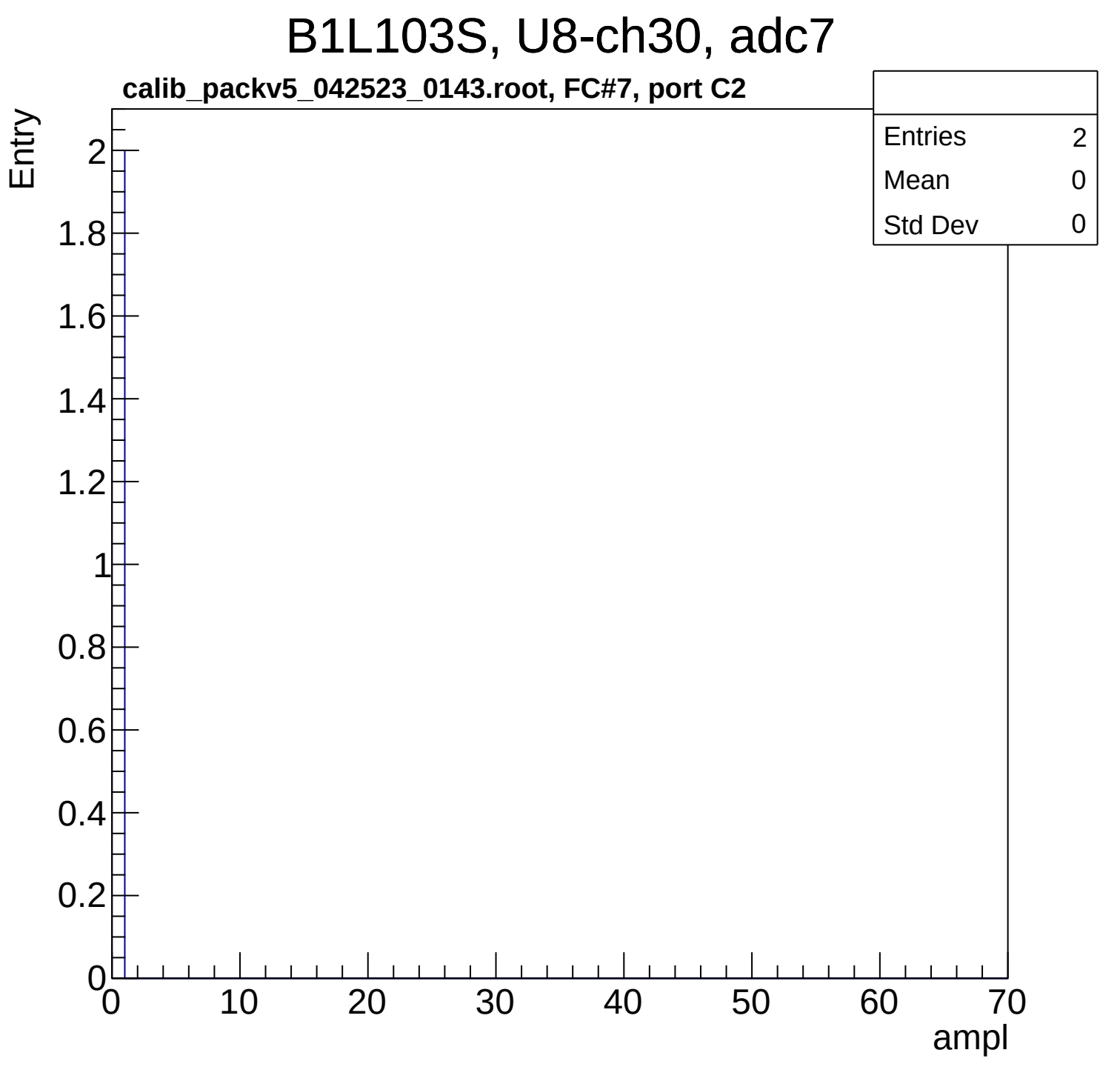

B1L103S, U8-ch30, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 42.84
Std Dev 3.889
Gaus mean : 43.5125
Gaus Width: 3.3494
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

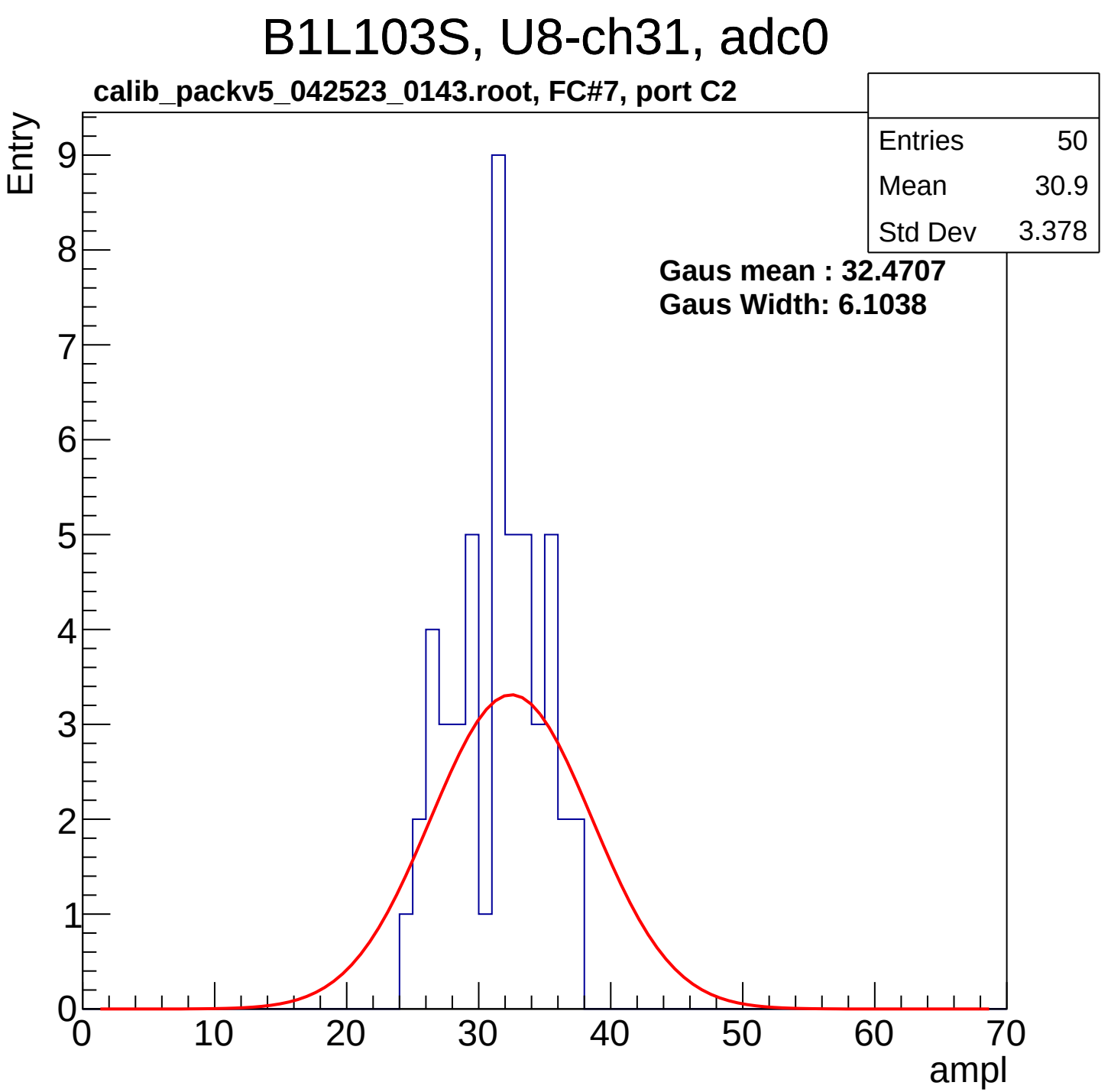

B1L103S, U8-ch30, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 49.84
Std Dev 3.278
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

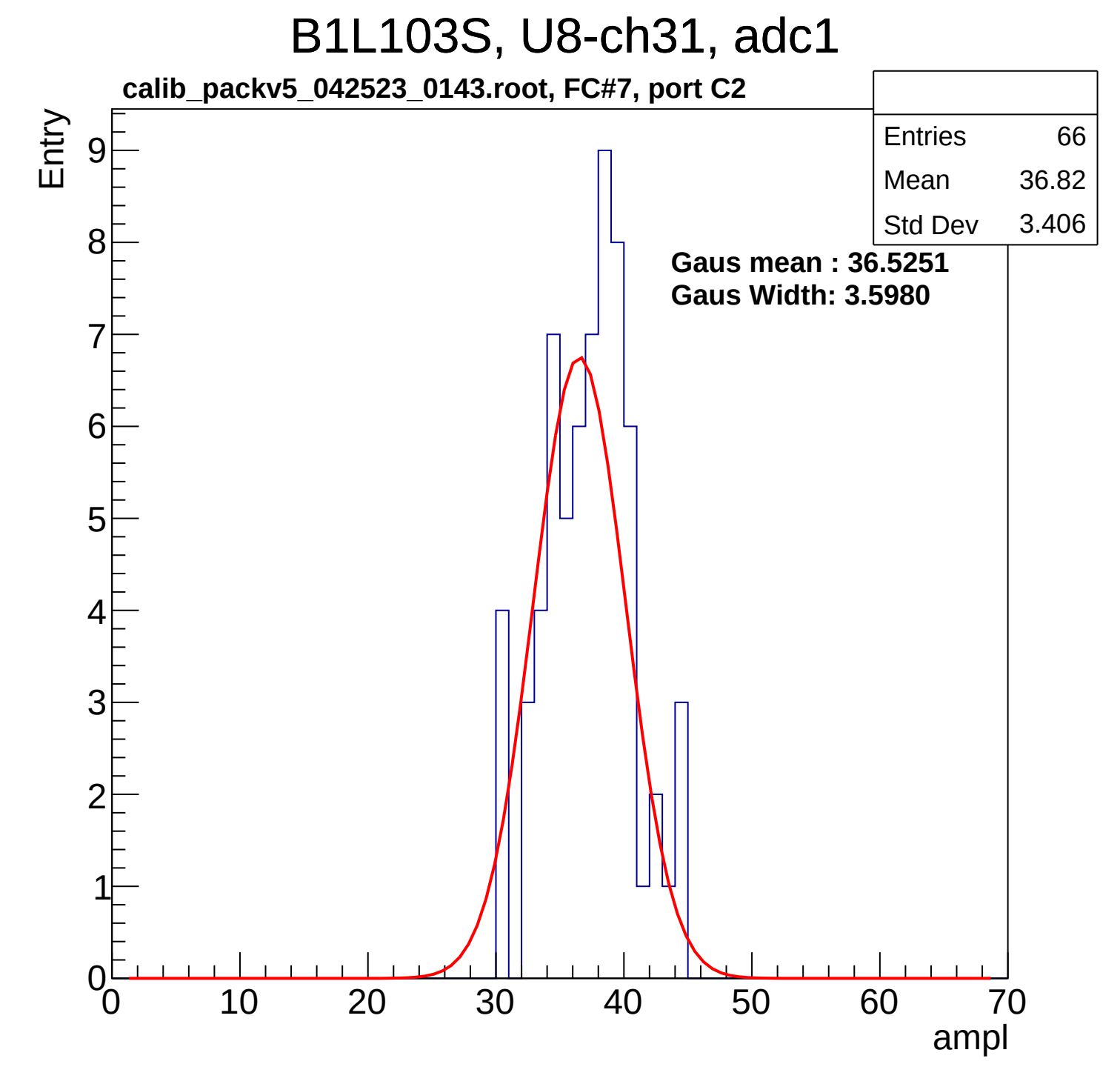

B1L103S, U8-ch30, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 55.56
Std Dev 3.431
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

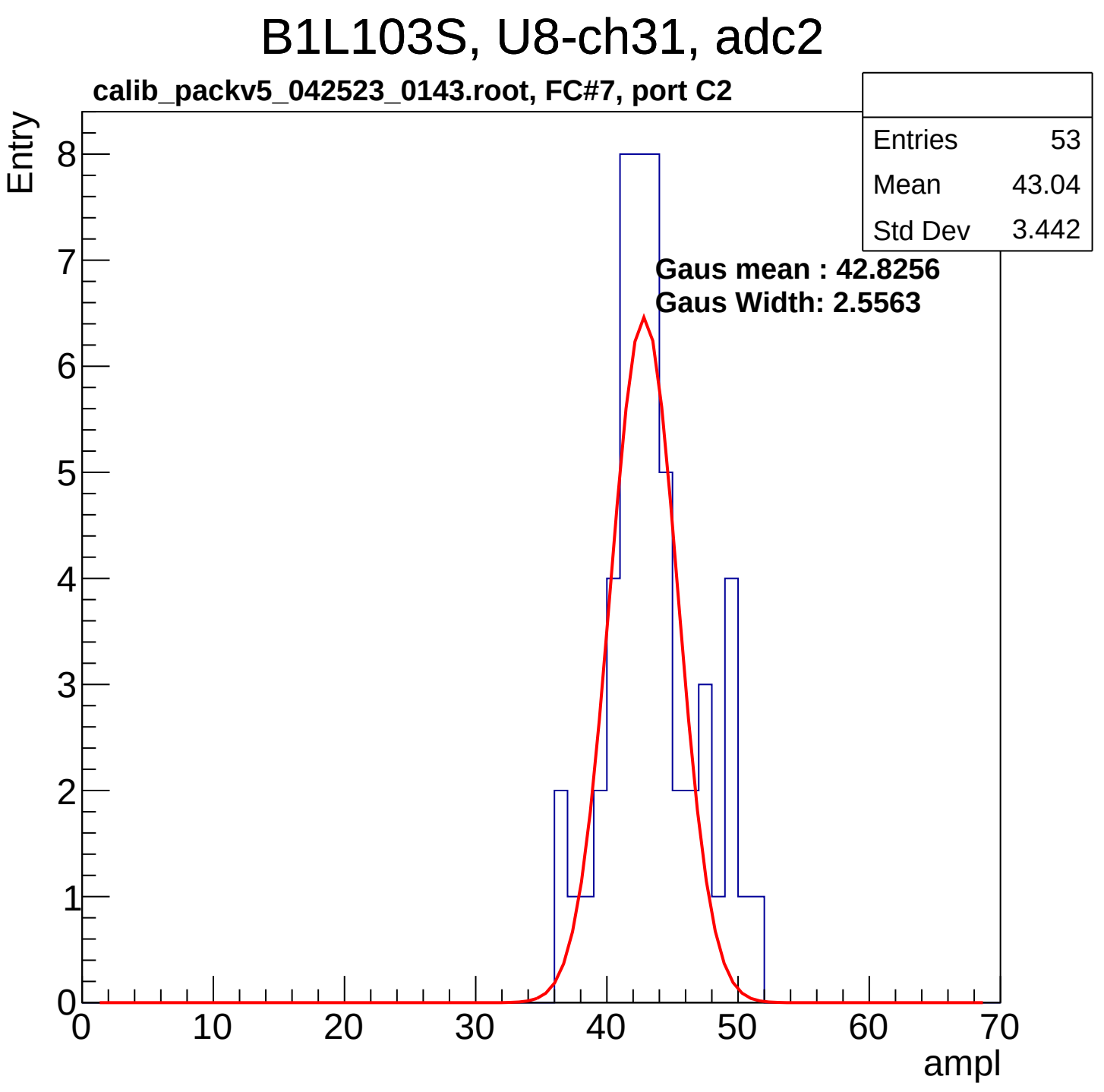

B1L103S, U8-ch30, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 43
Mean 60.09
Std Dev 2.165
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

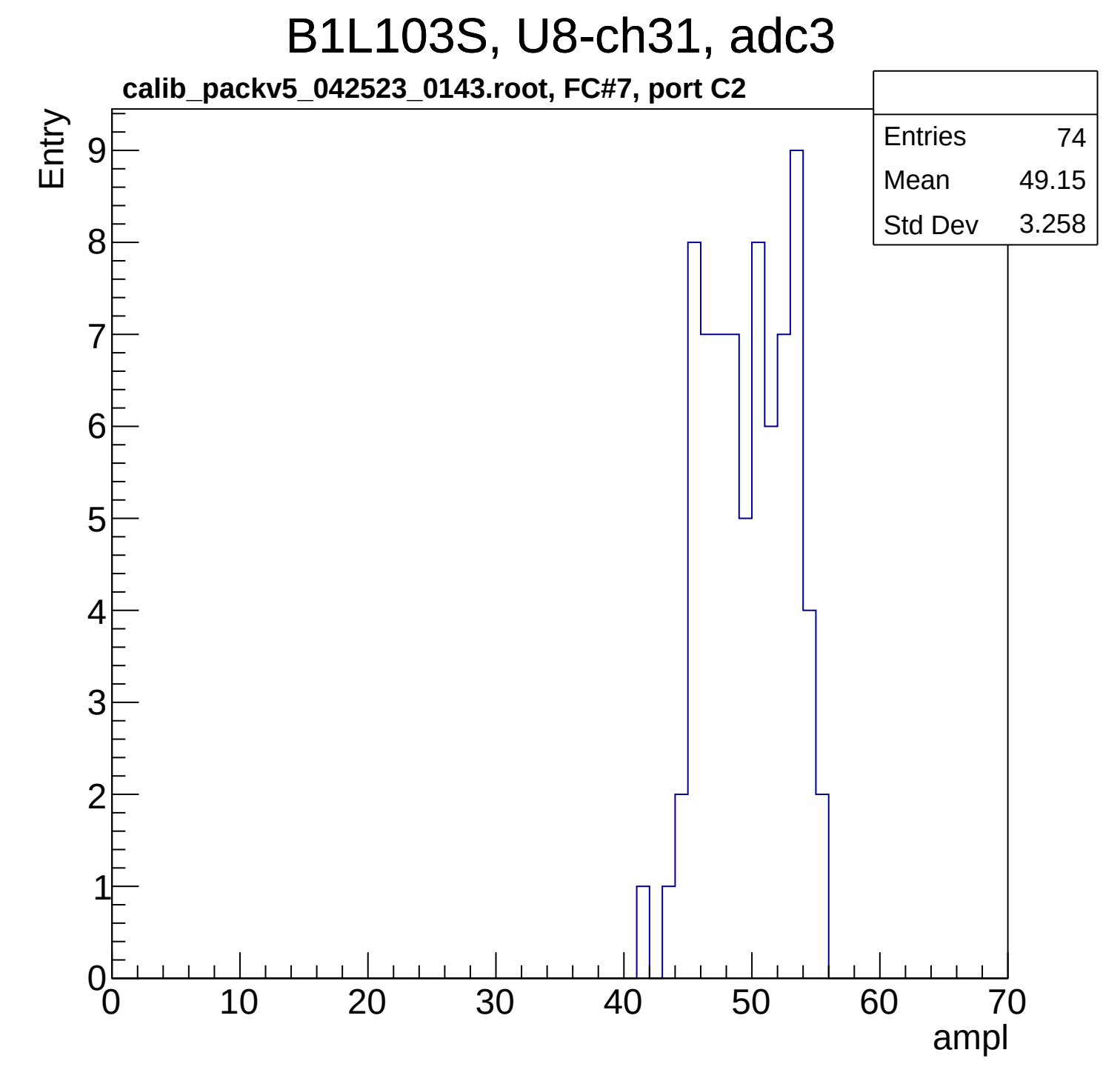

B1L103S, U8-ch30, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 62.2
Std Dev 0.9798
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

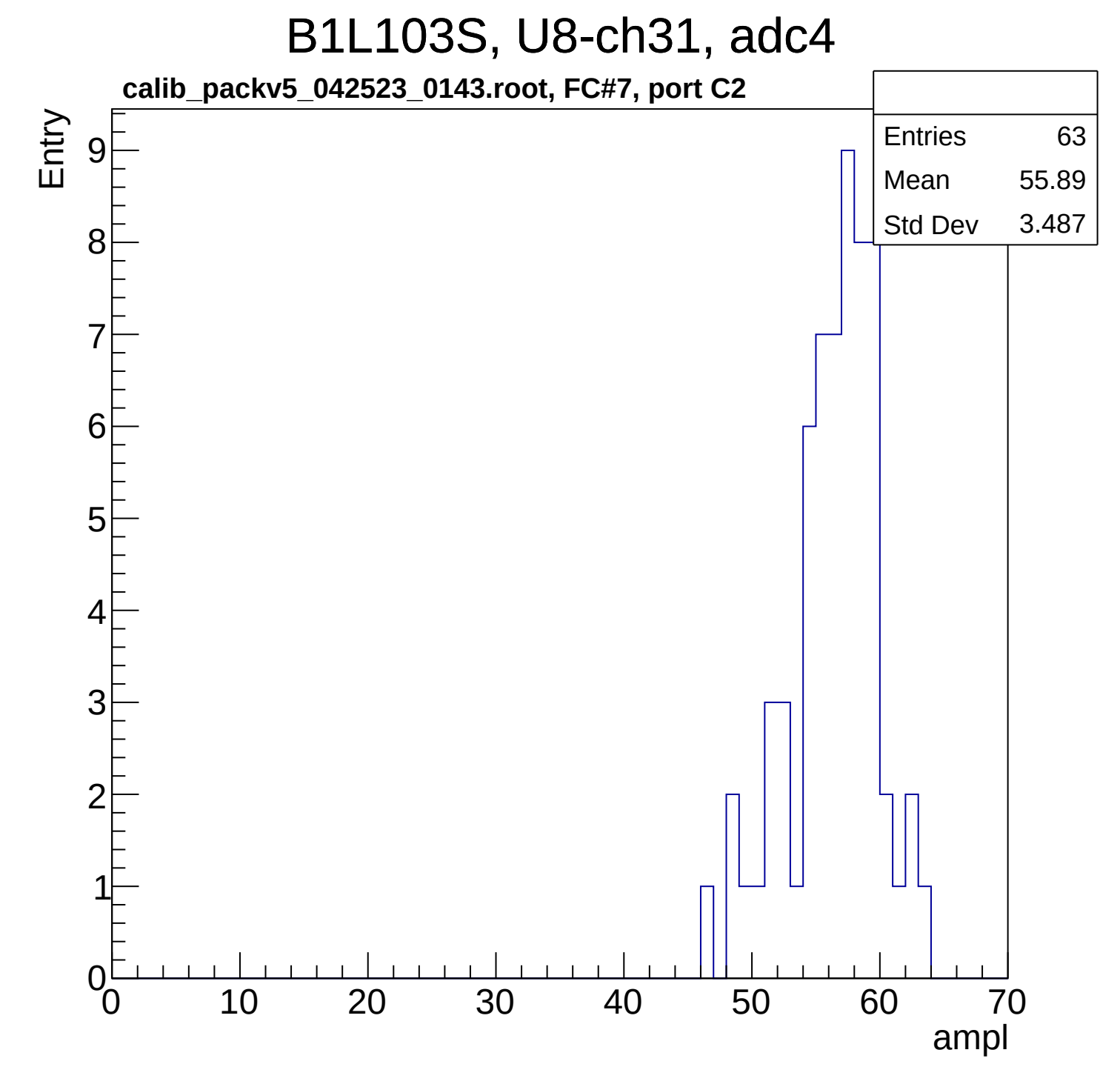

B1L103S, U8-ch30, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

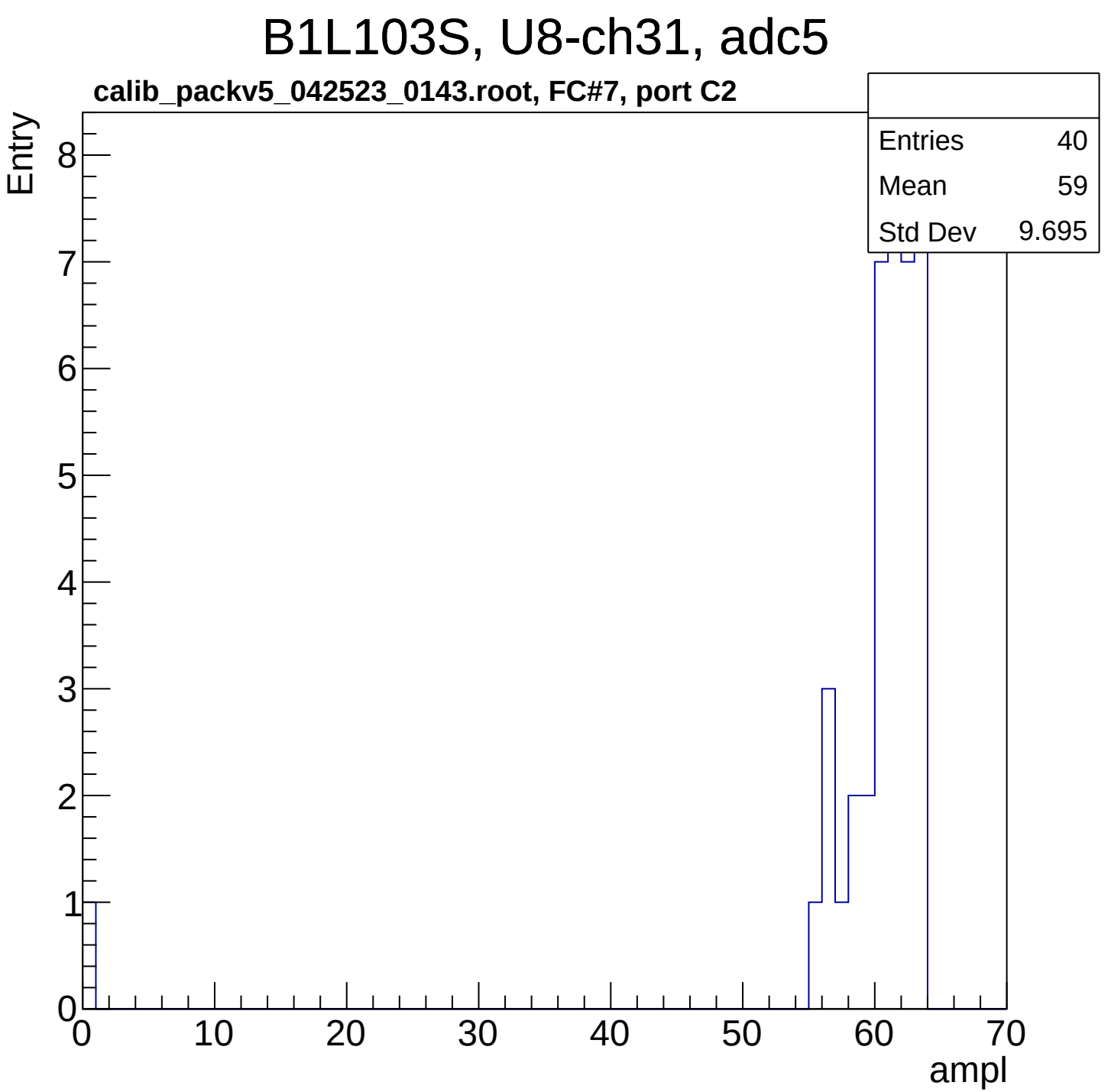

B1L103S, U8-ch31, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 30.9
Std Dev 3.378
Gaus mean : 32.4707
Gaus Width: 6.1038
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

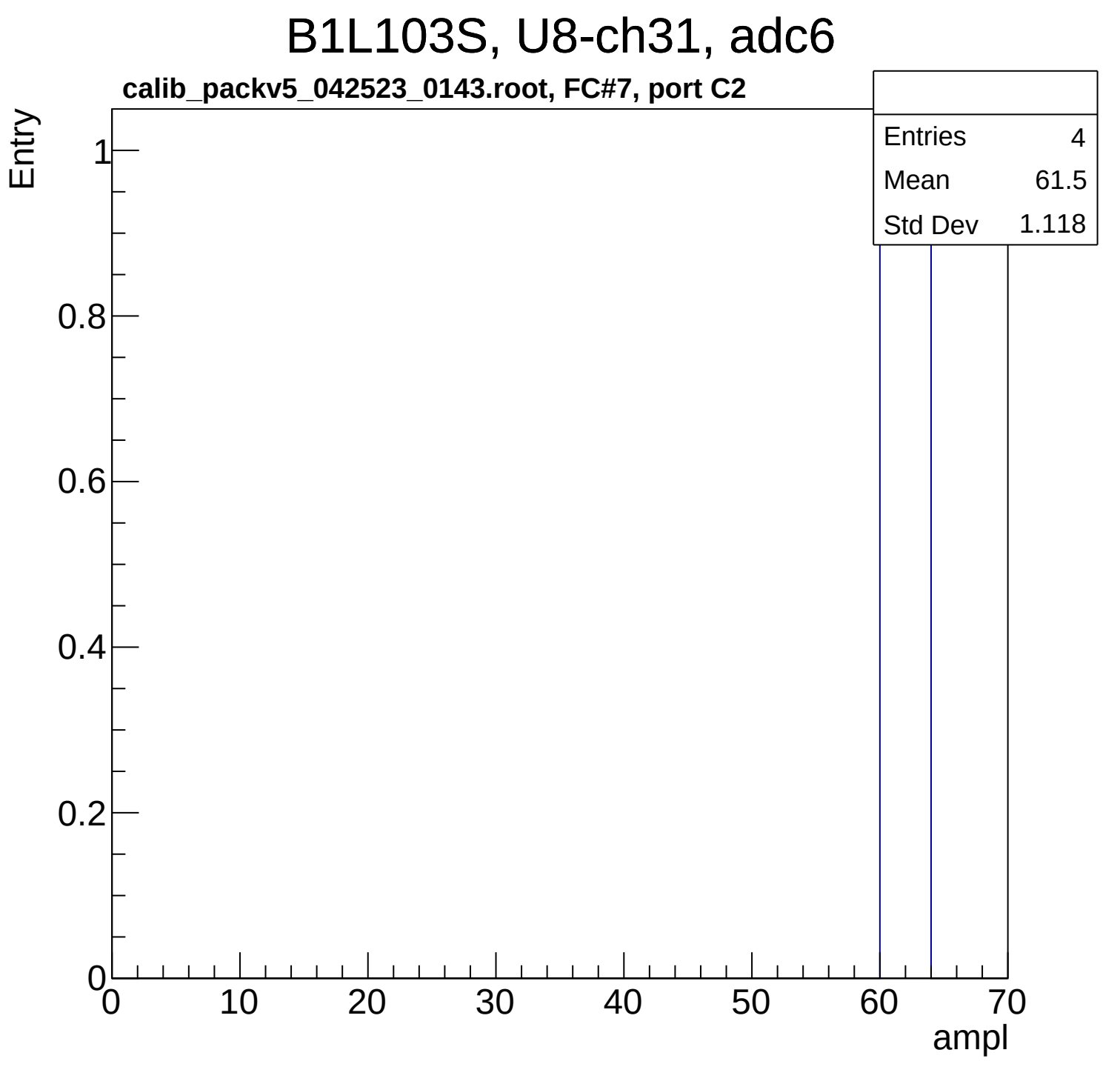

B1L103S, U8-ch31, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 36.82
Std Dev 3.406
Gaus mean : 36.5251
Gaus Width: 3.5980
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

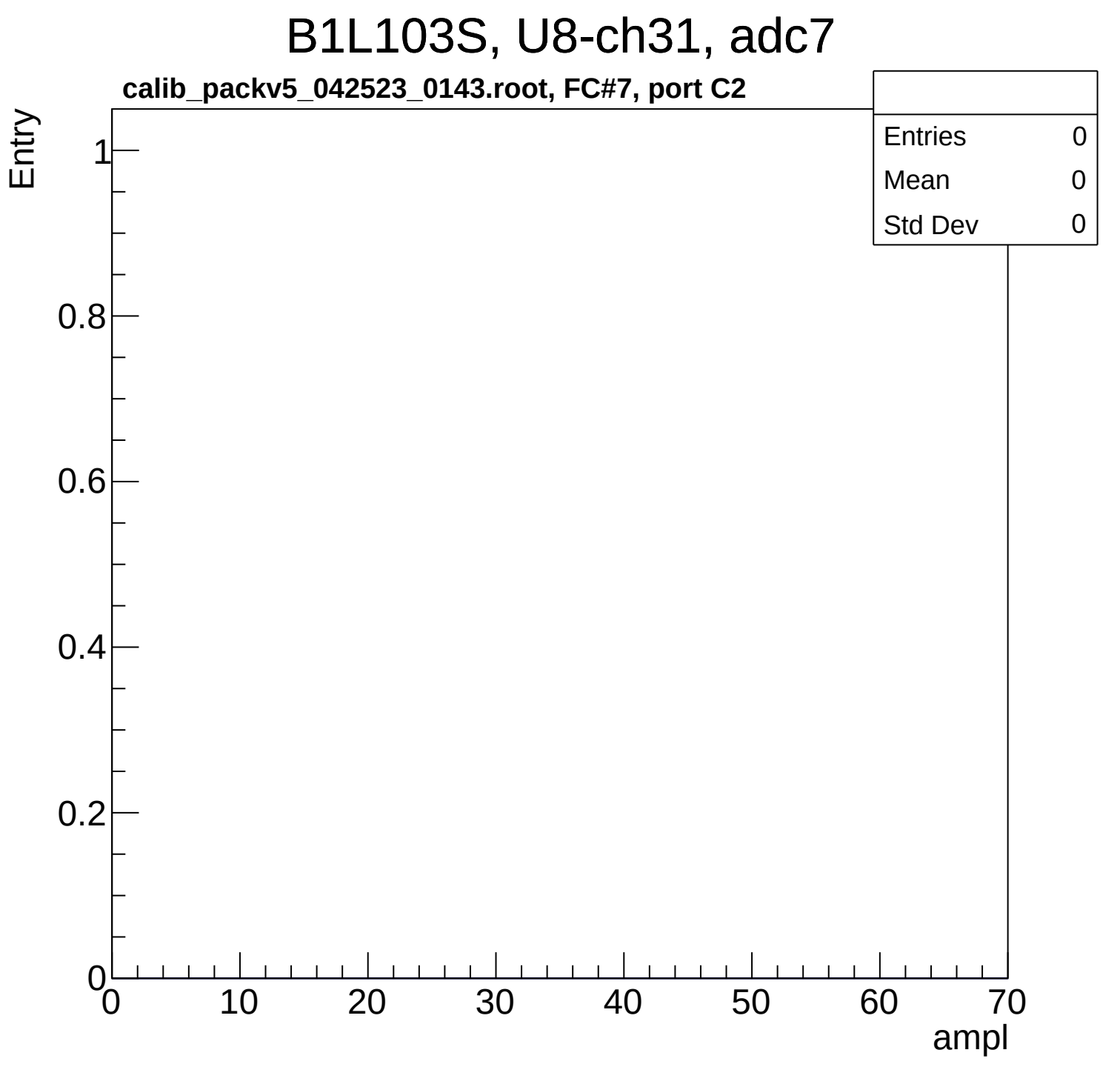

B1L103S, U8-ch31, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 43.04
Std Dev 3.442
Gaus mean : 42.8256
Gaus Width: 2.5563
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

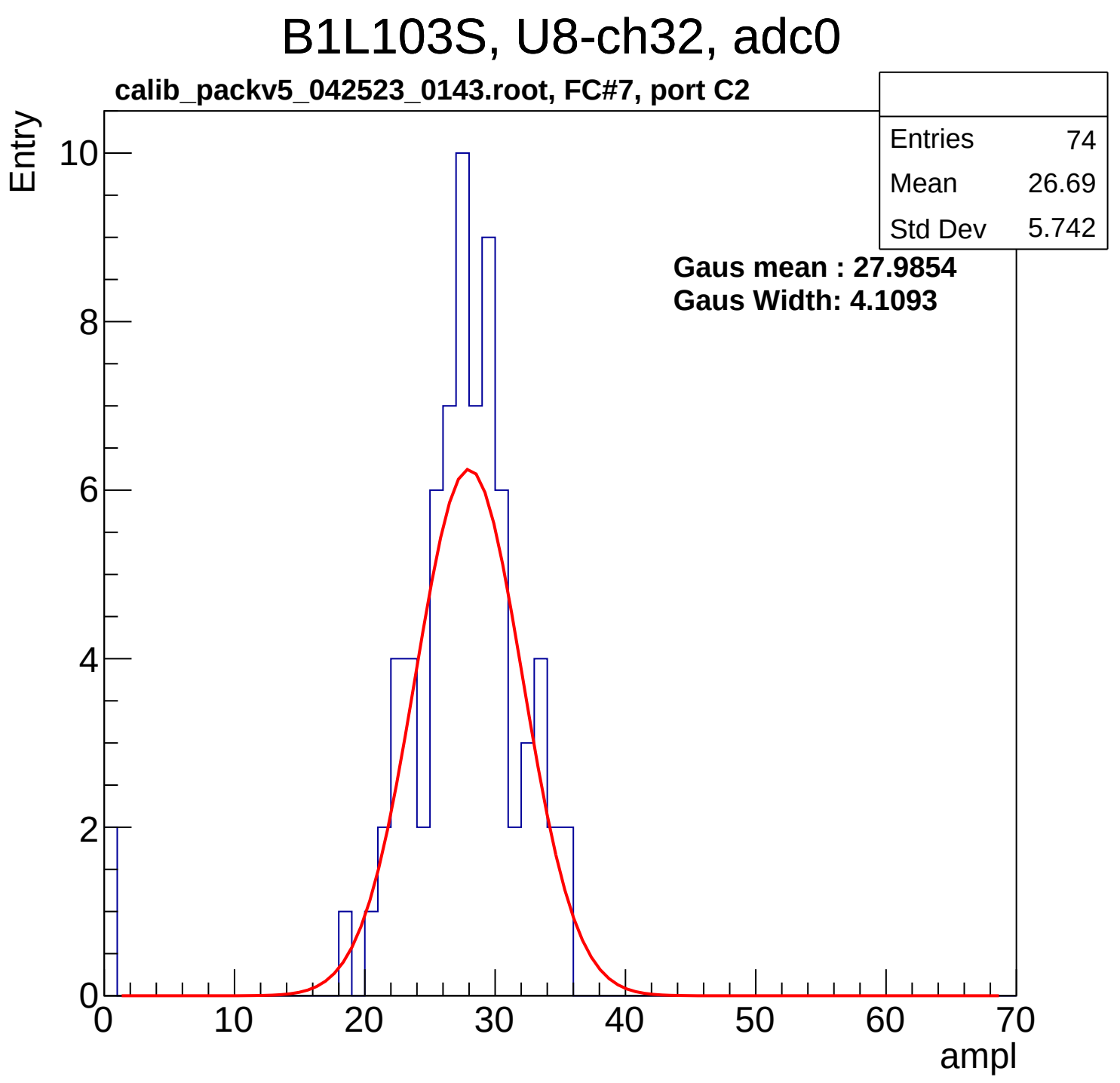

B1L103S, U8-ch31, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 49.15
Std Dev 3.258
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

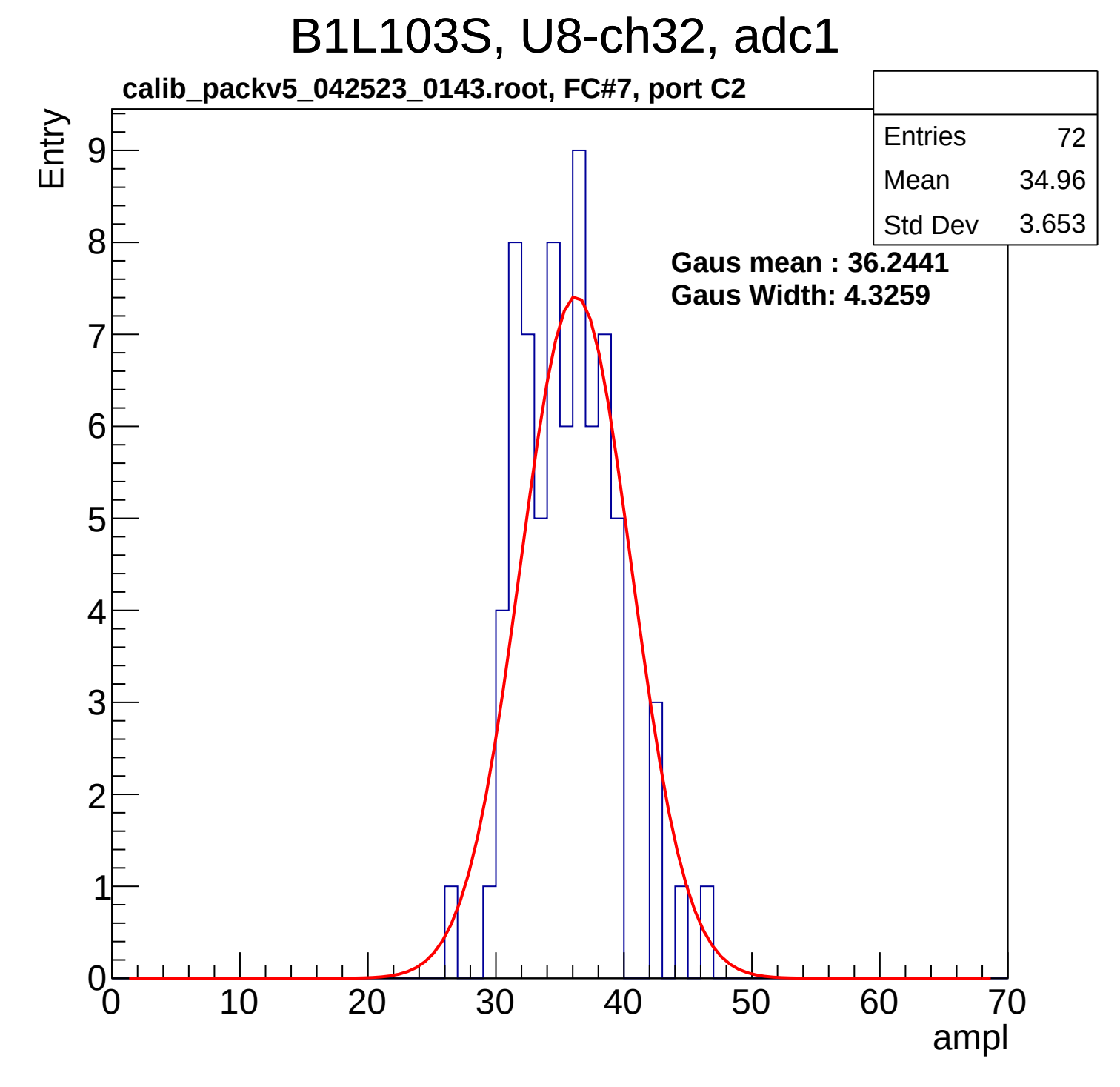

B1L103S, U8-ch31, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 55.89
Std Dev 3.487
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

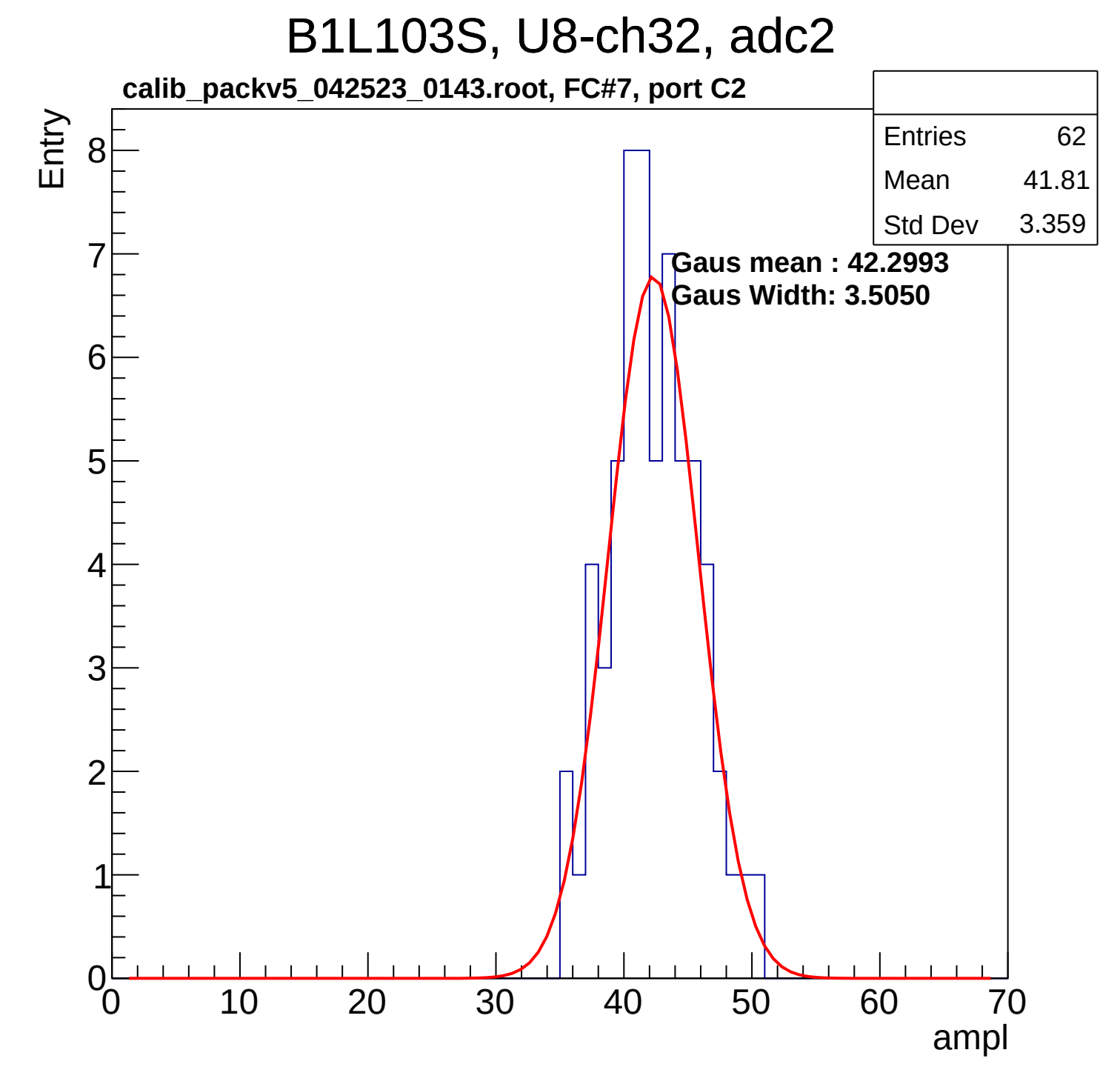

B1L103S, U8-ch31, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 40
Mean 59
Std Dev 9.695
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

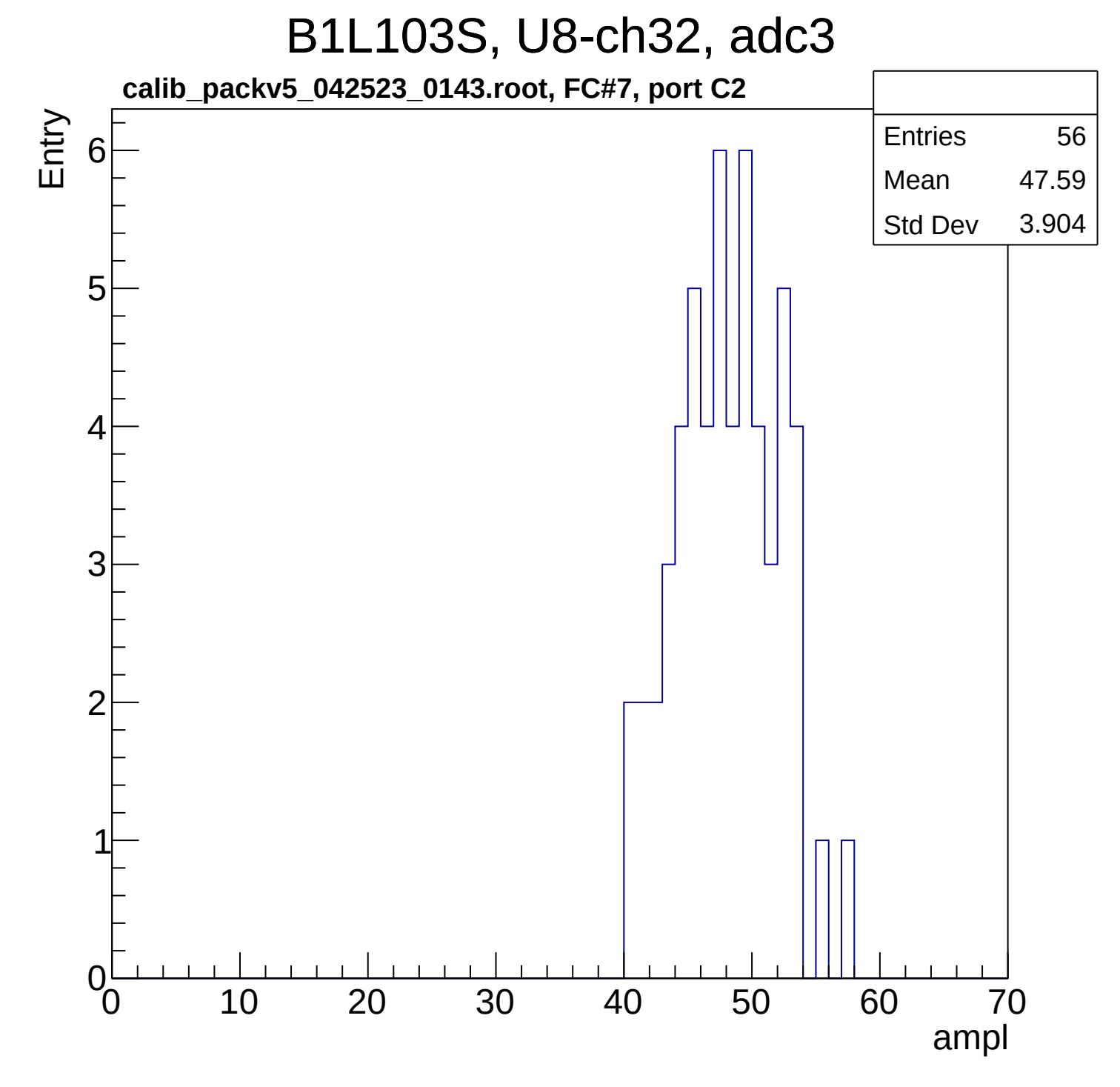

B1L103S, U8-ch31, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 61.5
Std Dev 1.118
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

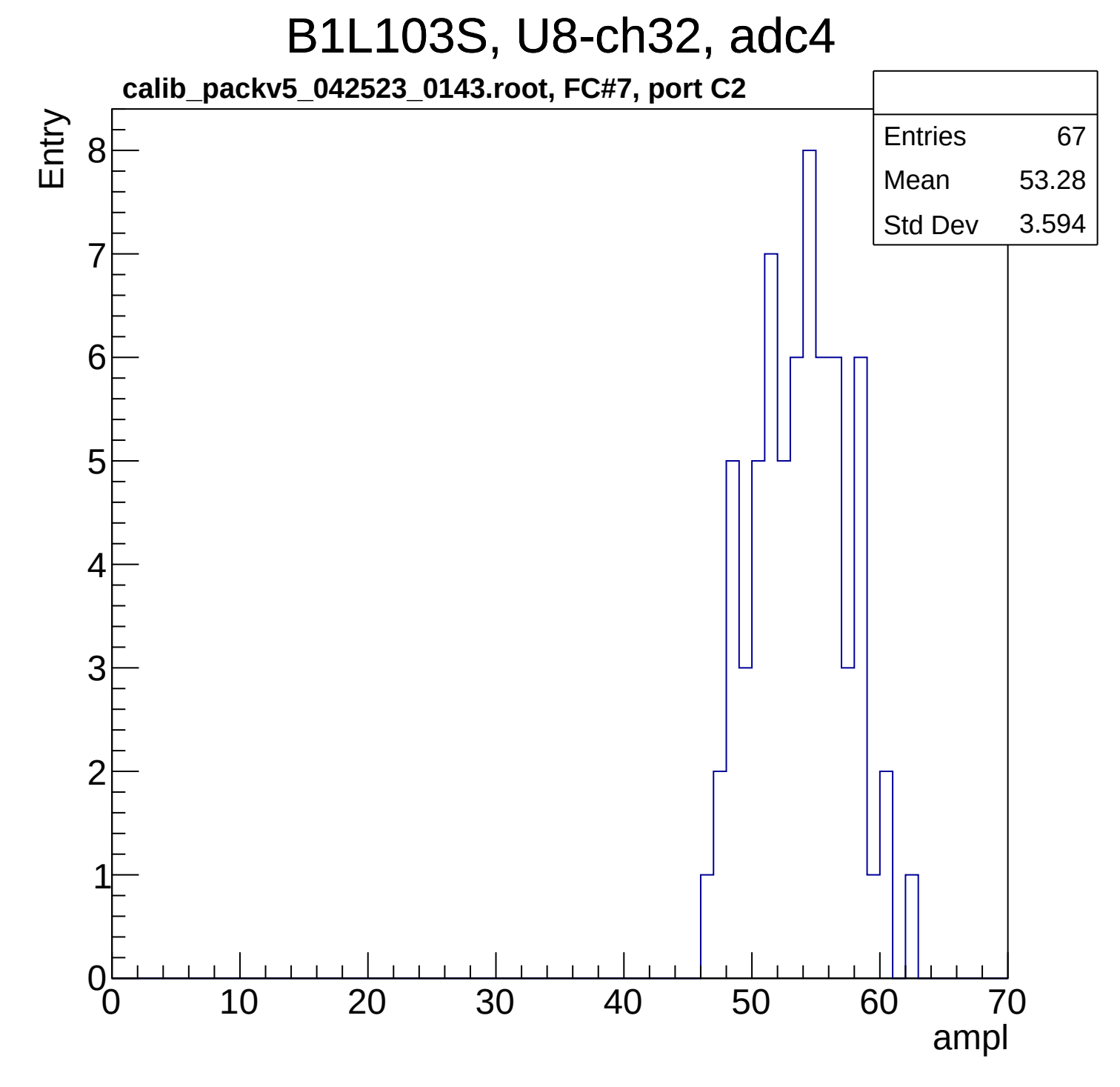

B1L103S, U8-ch31, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

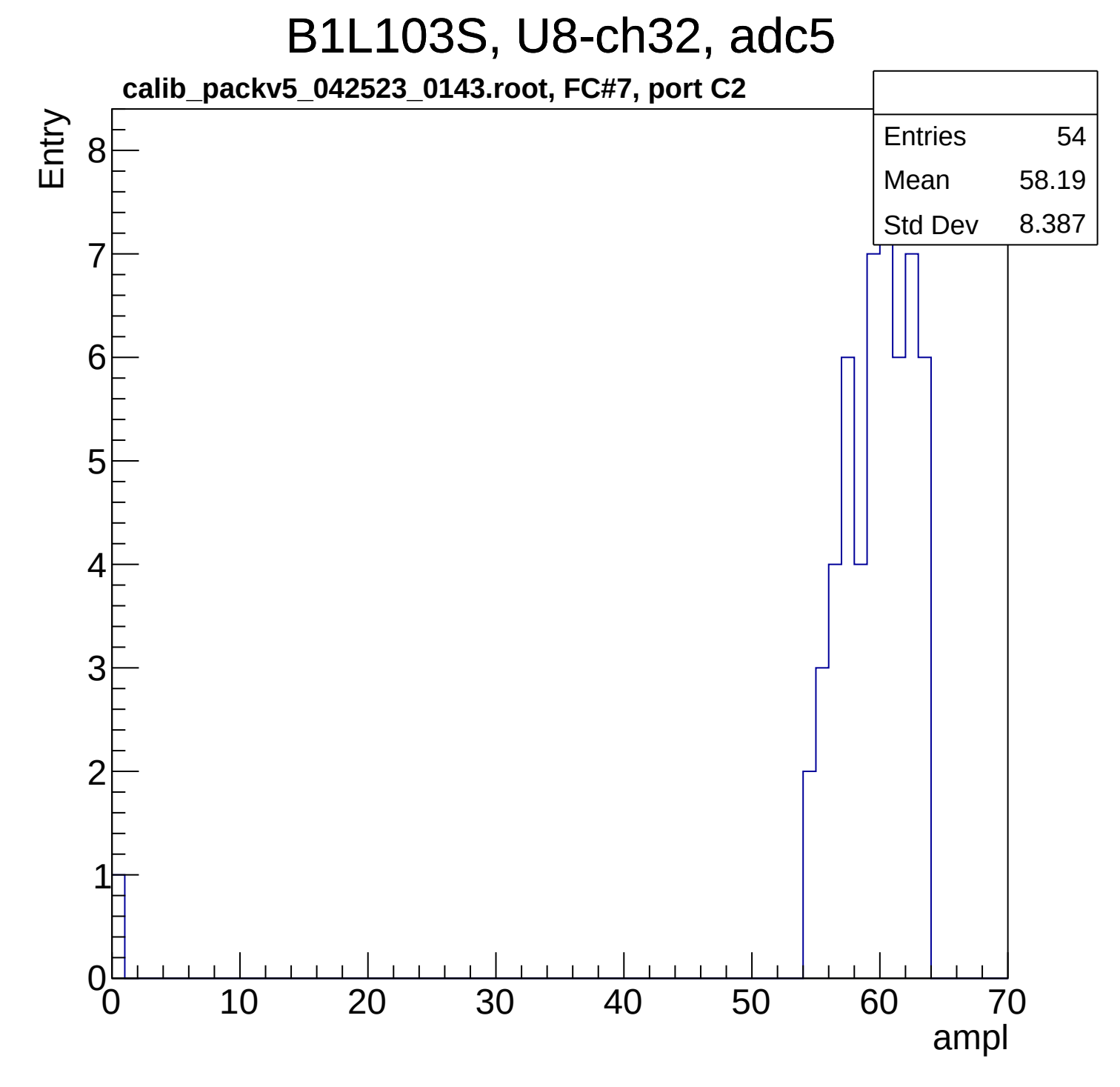

B1L103S, U8-ch32, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 26.69
Std Dev 5.742
Gaus mean : 27.9854
Gaus Width: 4.1093
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

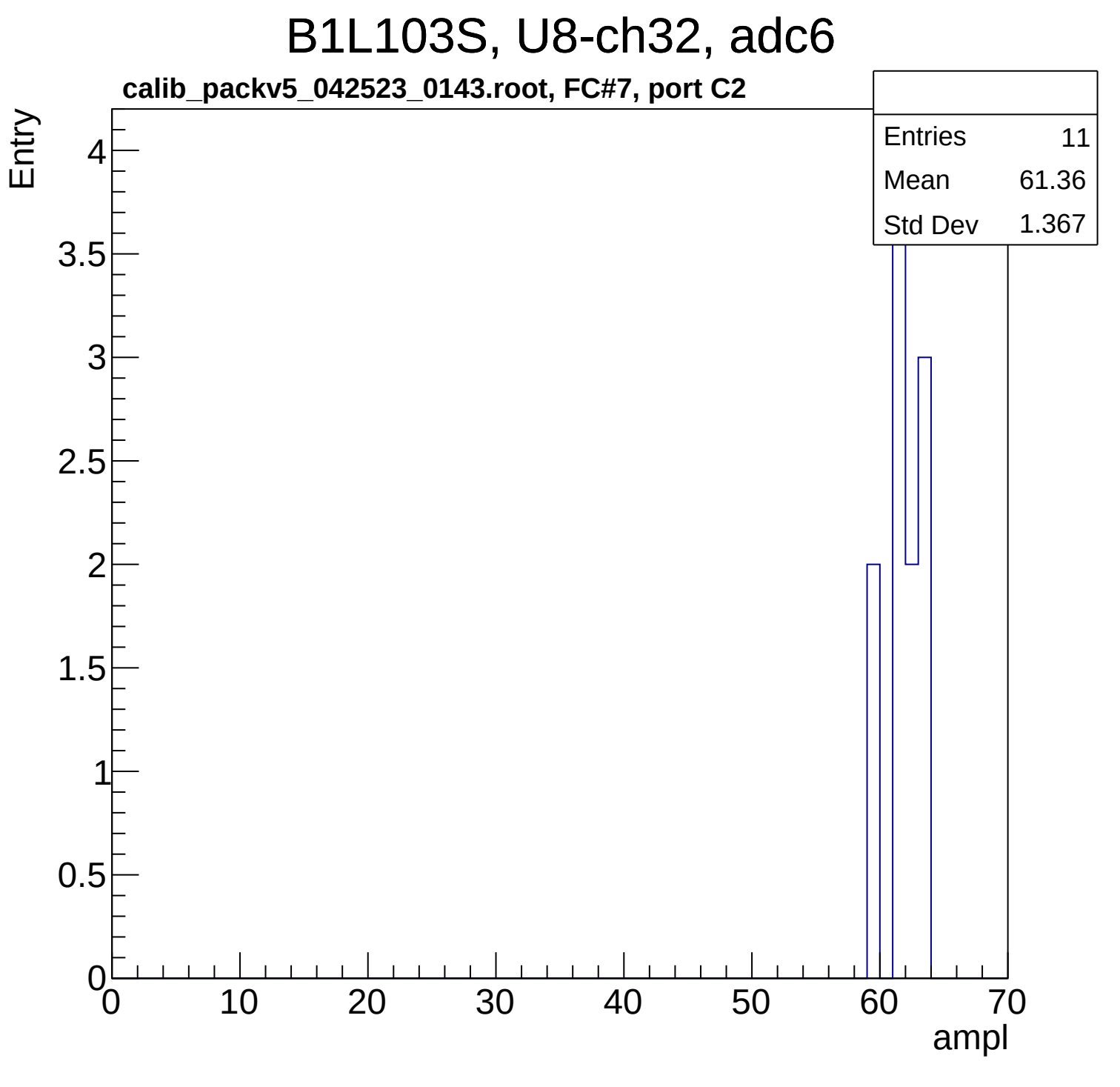

B1L103S, U8-ch32, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 34.96
Std Dev 3.653
Gaus mean : 36.2441
Gaus Width: 4.3259
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

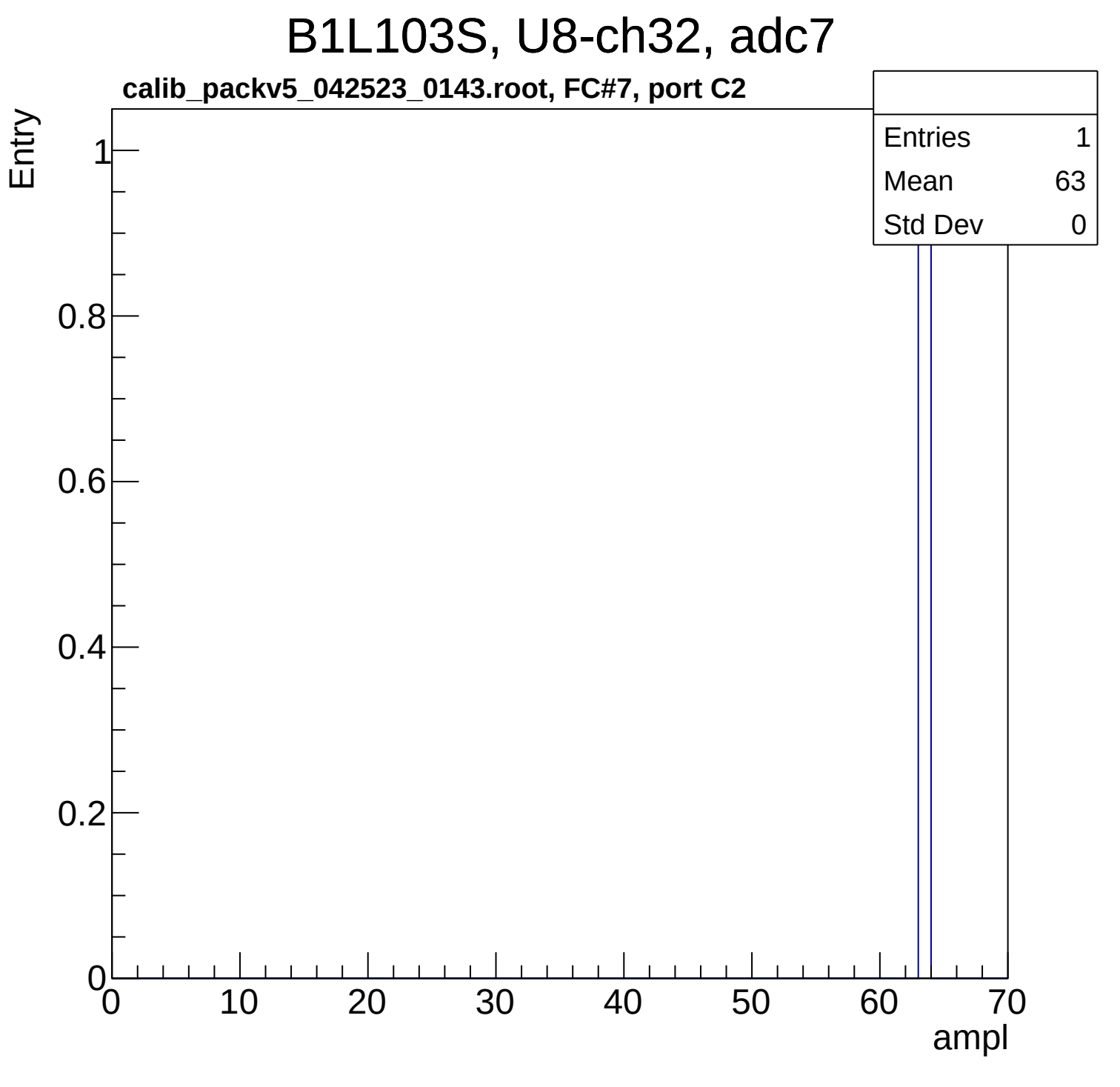

B1L103S, U8-ch32, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 41.81
Std Dev 3.359
Gaus mean : 42.2993
Gaus Width: 3.5050
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

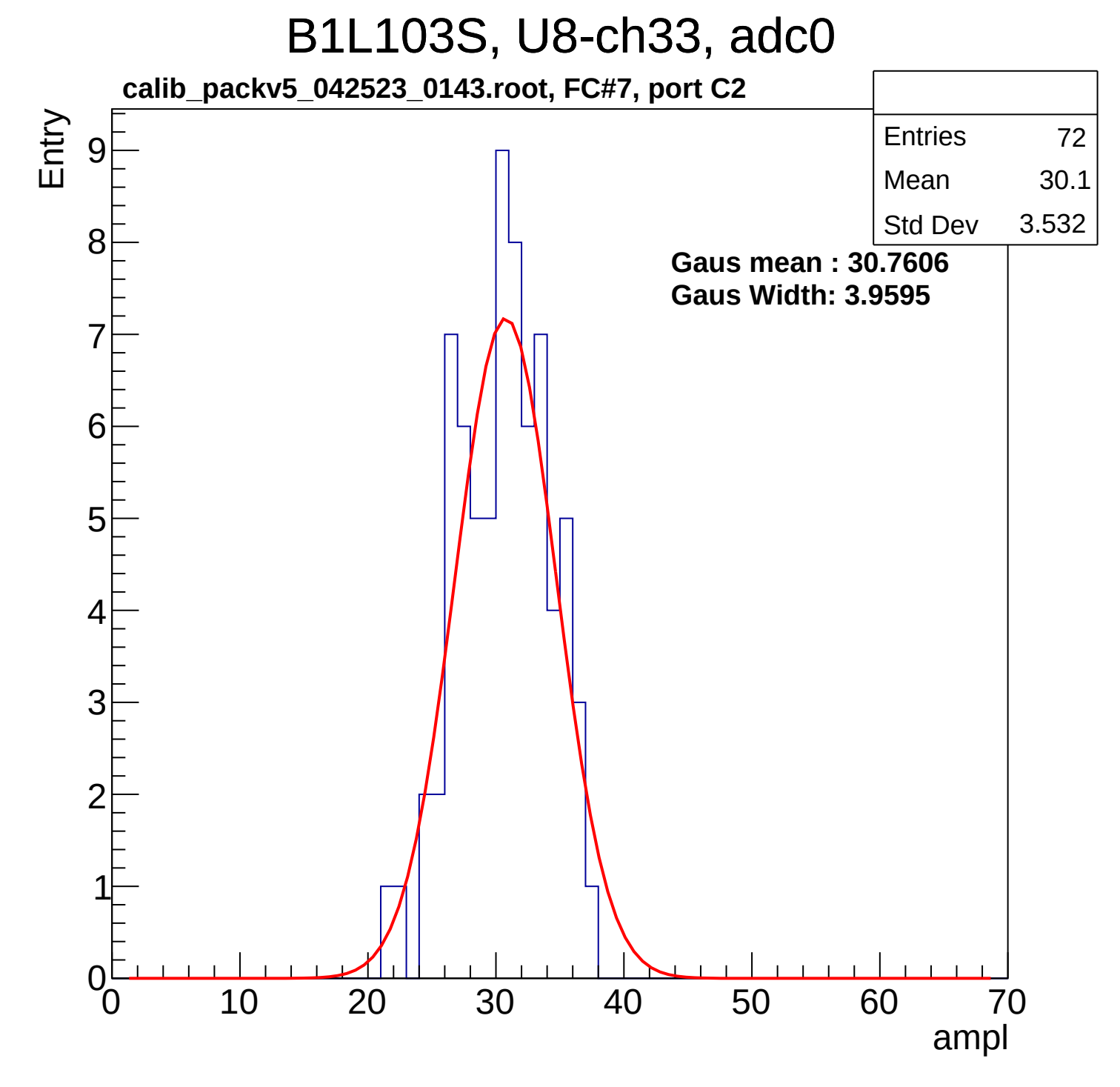

B1L103S, U8-ch32, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 47.59
Std Dev 3.904
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

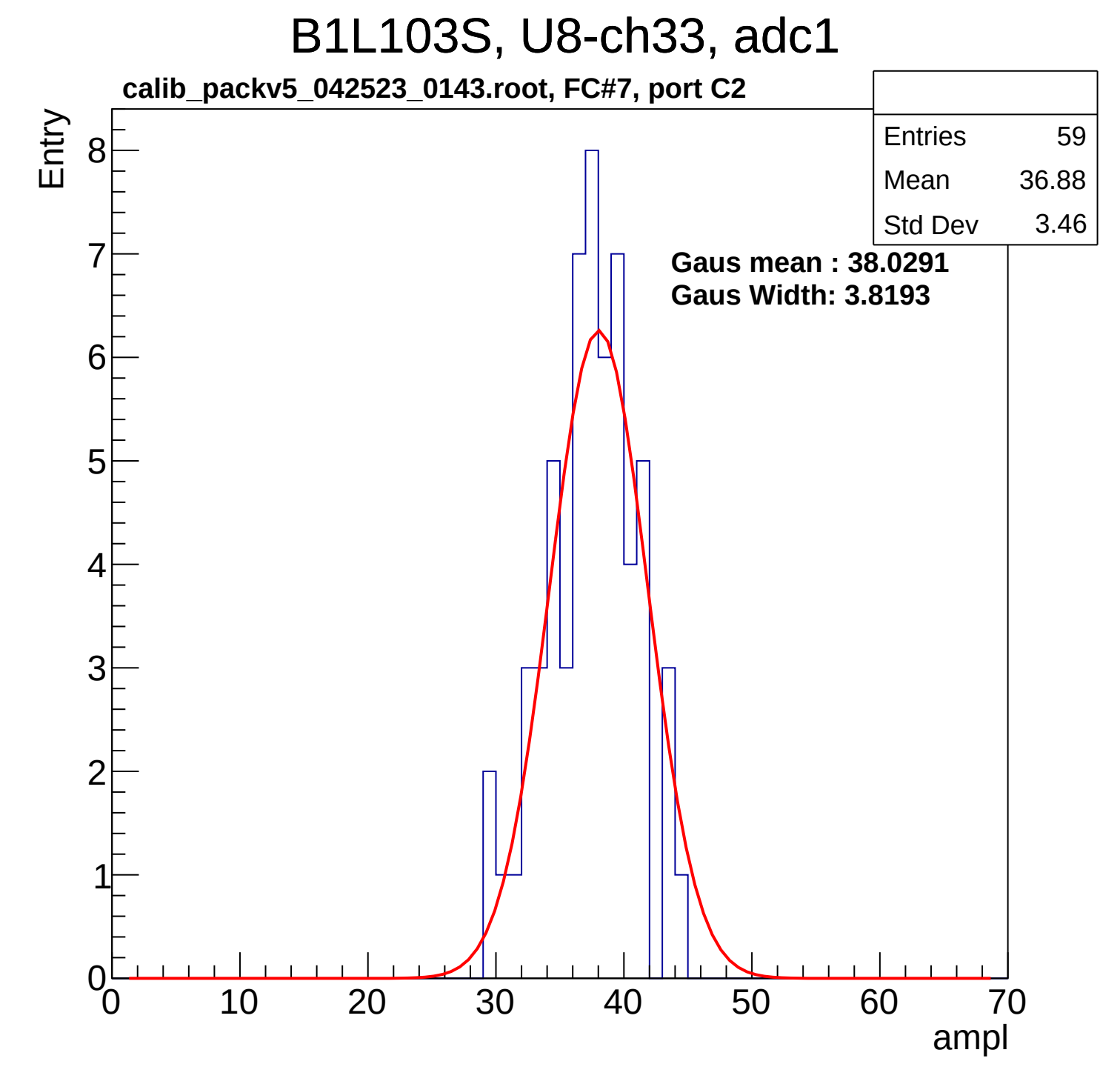

B1L103S, U8-ch32, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 53.28
Std Dev 3.594
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

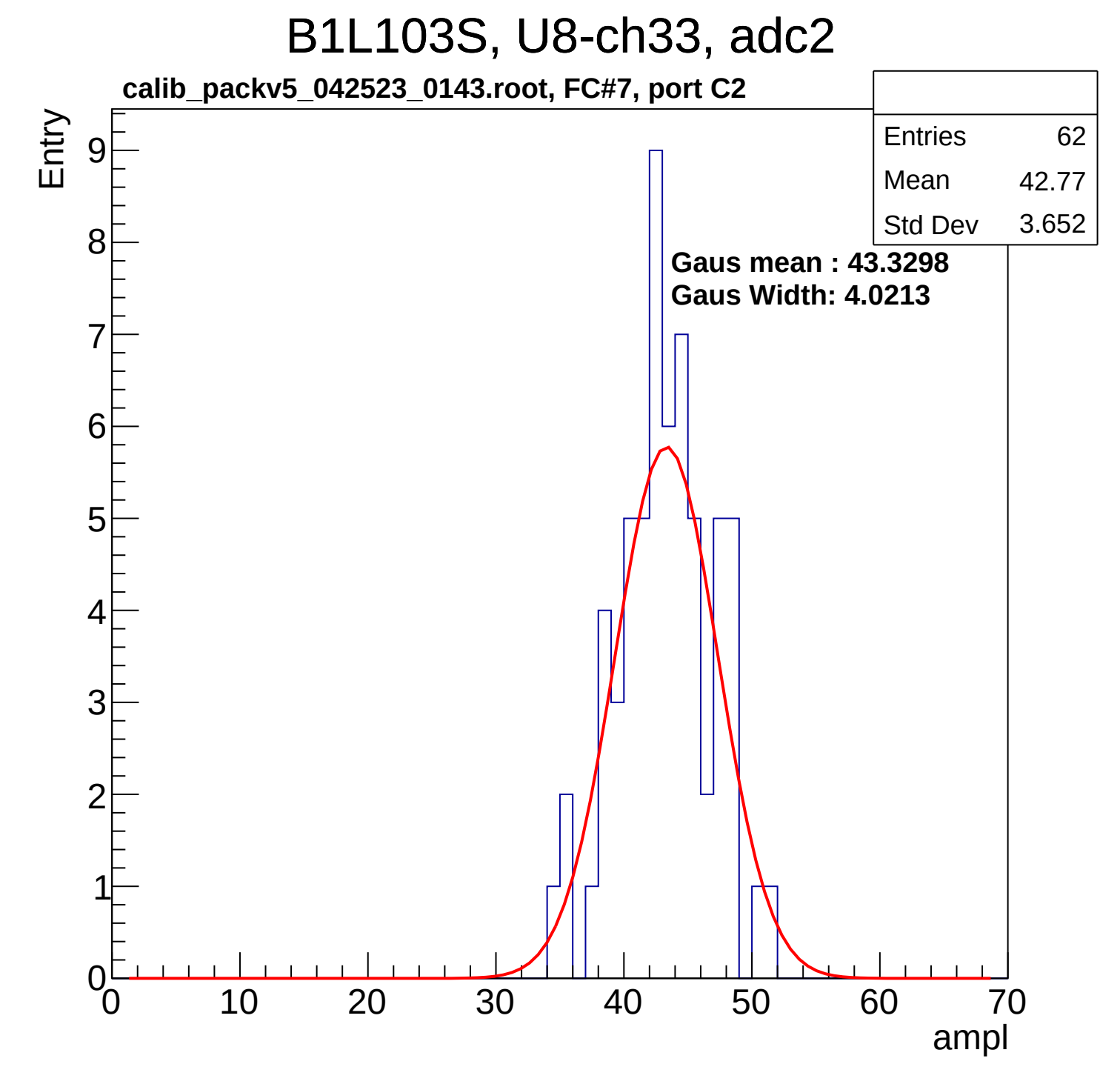

B1L103S, U8-ch32, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 58.19
Std Dev 8.387
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

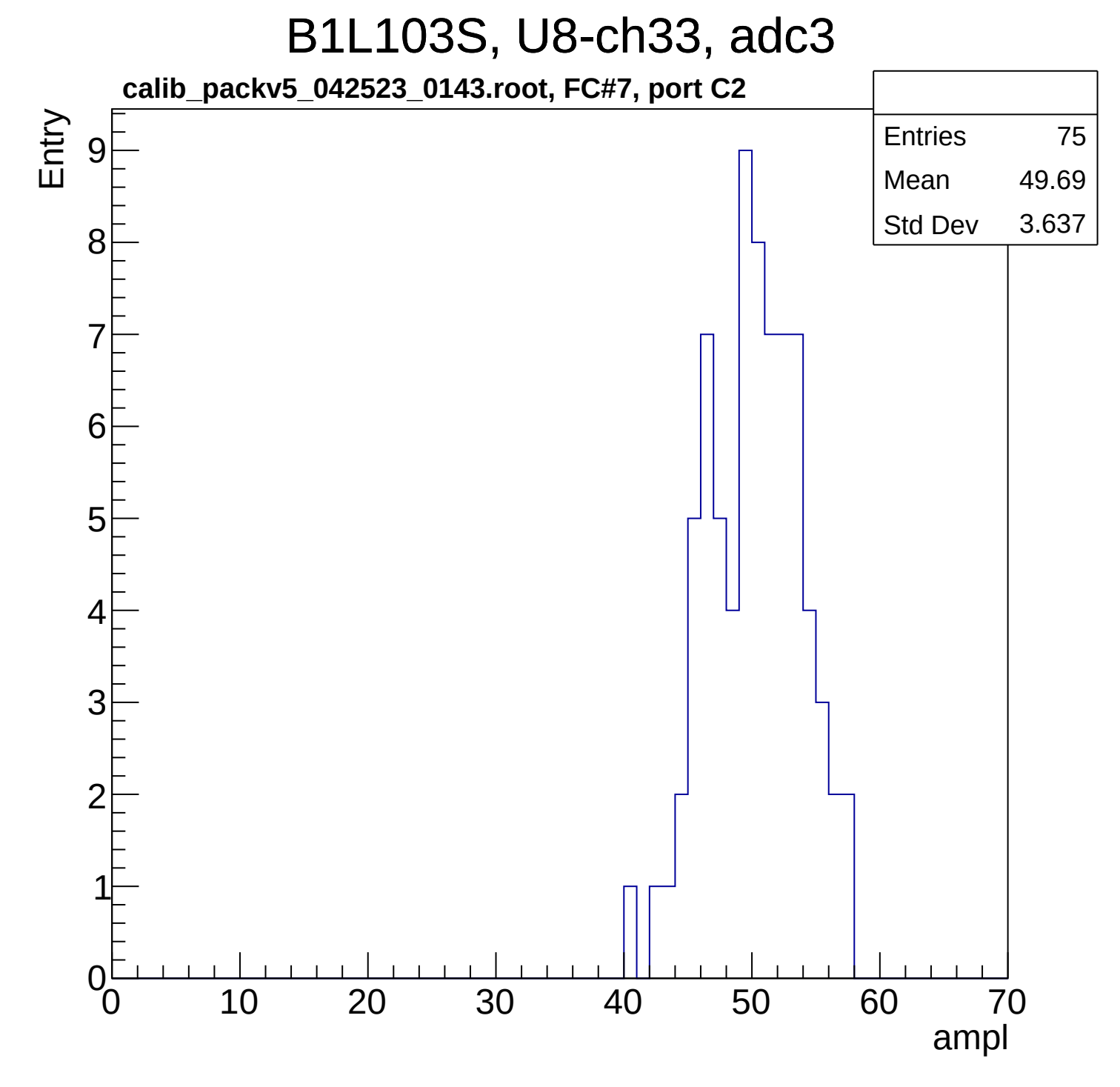

B1L103S, U8-ch32, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 11
Mean 61.36
Std Dev 1.367
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

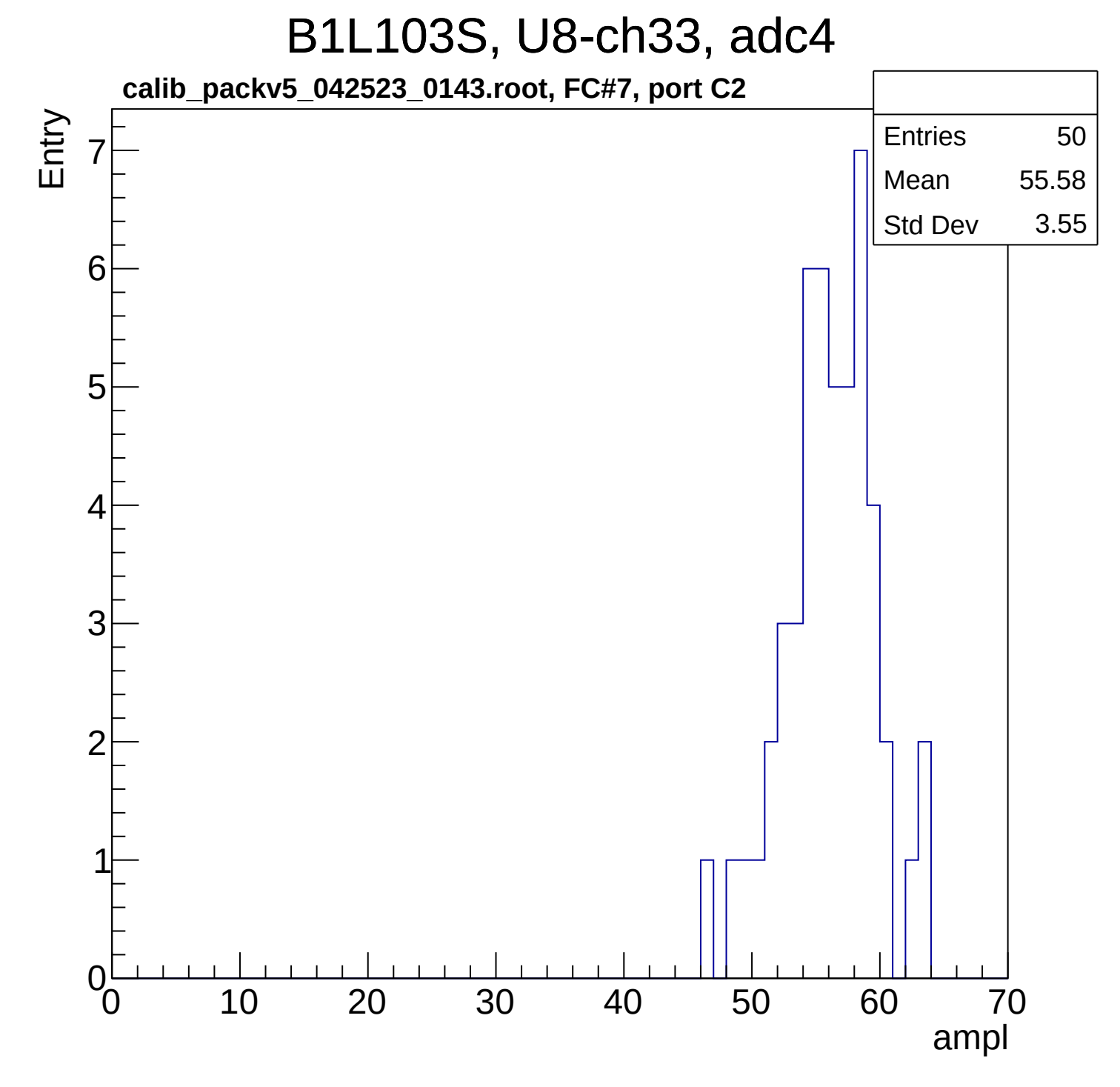

B1L103S, U8-ch32, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

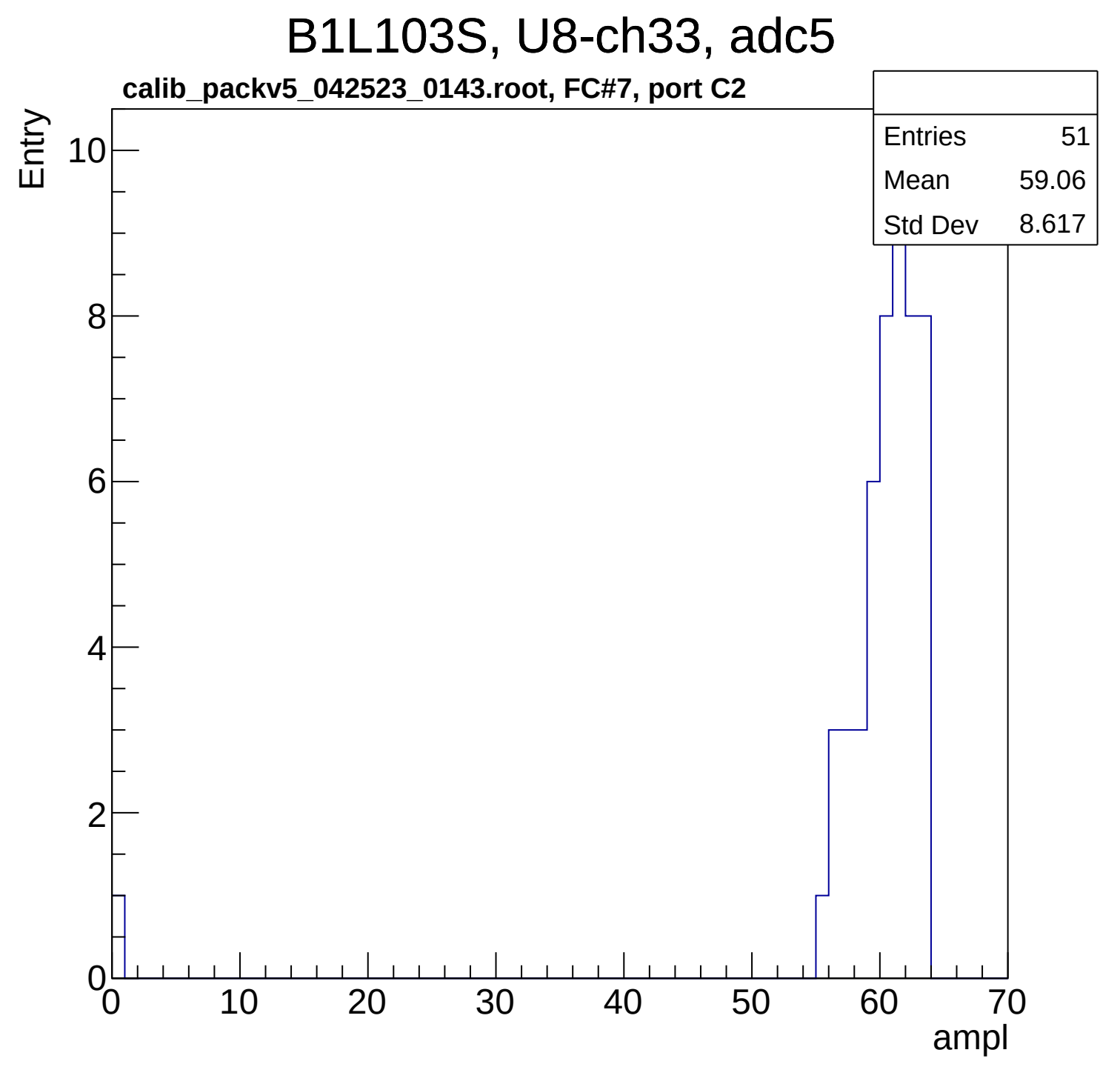

B1L103S, U8-ch33, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 30.1
Std Dev 3.532
Gaus mean : 30.7606
Gaus Width: 3.9595
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

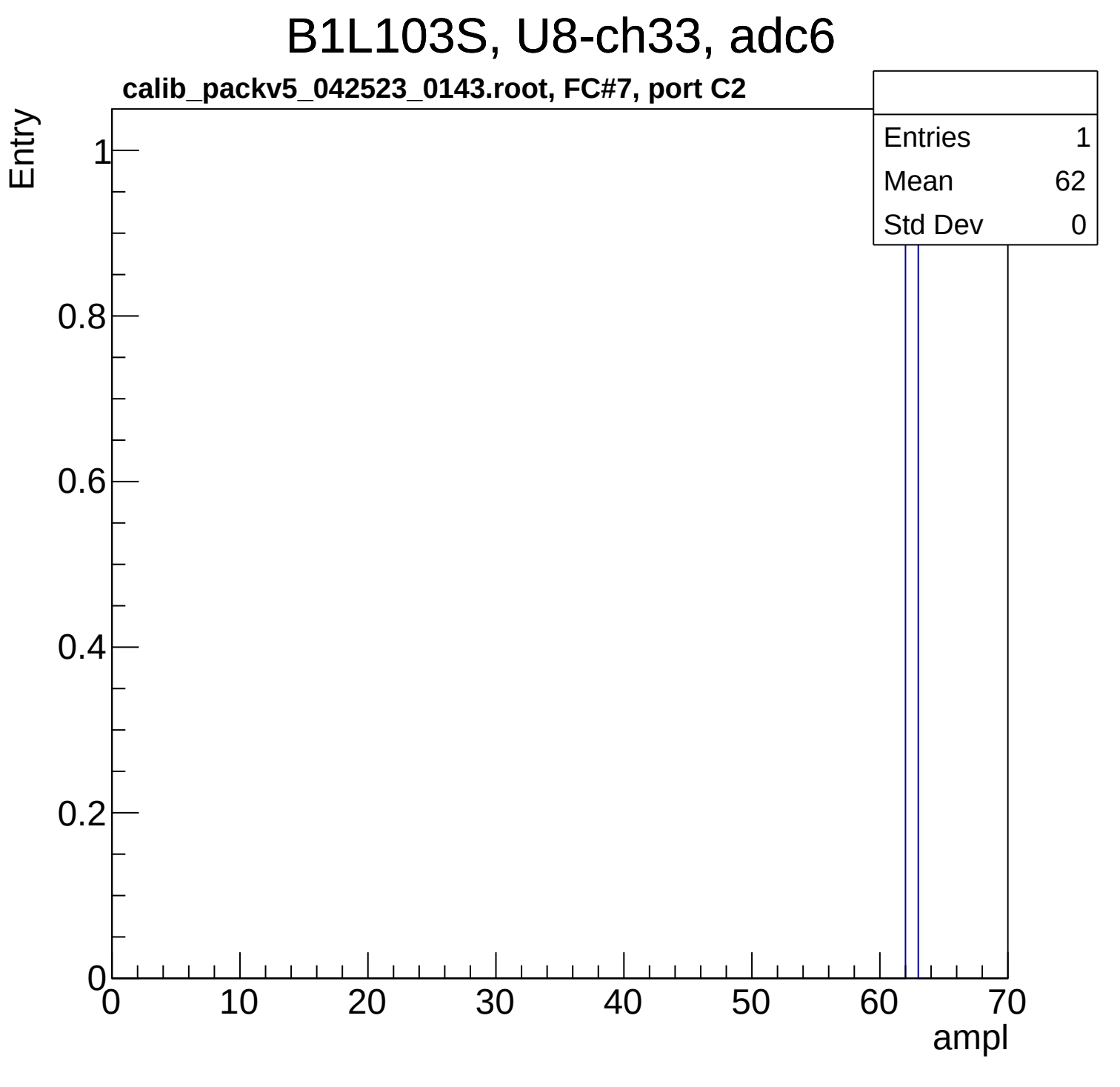

B1L103S, U8-ch33, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 36.88
Std Dev 3.46
Gaus mean : 38.0291
Gaus Width: 3.8193
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

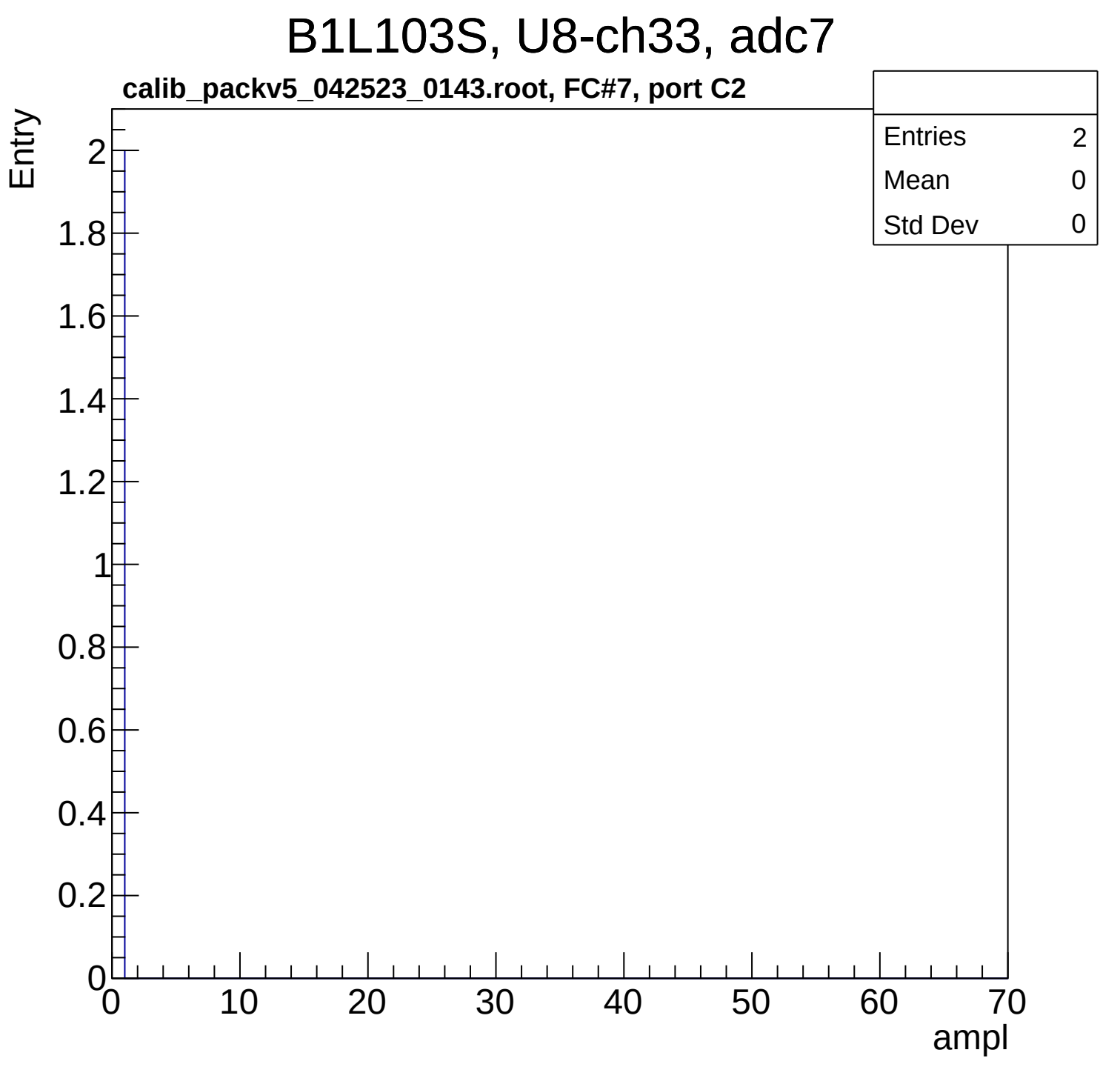

B1L103S, U8-ch33, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 42.77
Std Dev 3.652
Gaus mean : 43.3298
Gaus Width: 4.0213
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

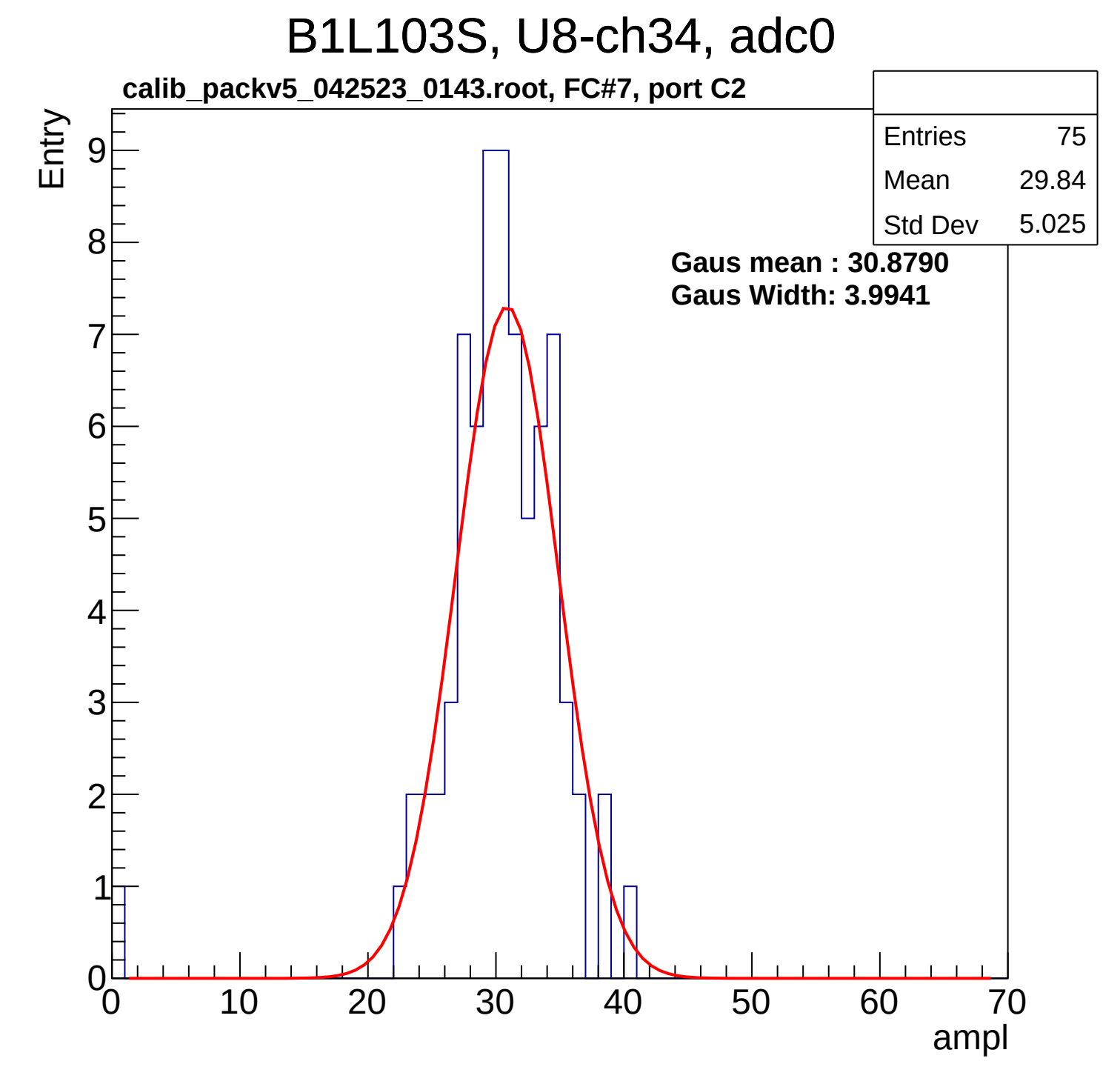

B1L103S, U8-ch33, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 49.69
Std Dev 3.637
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

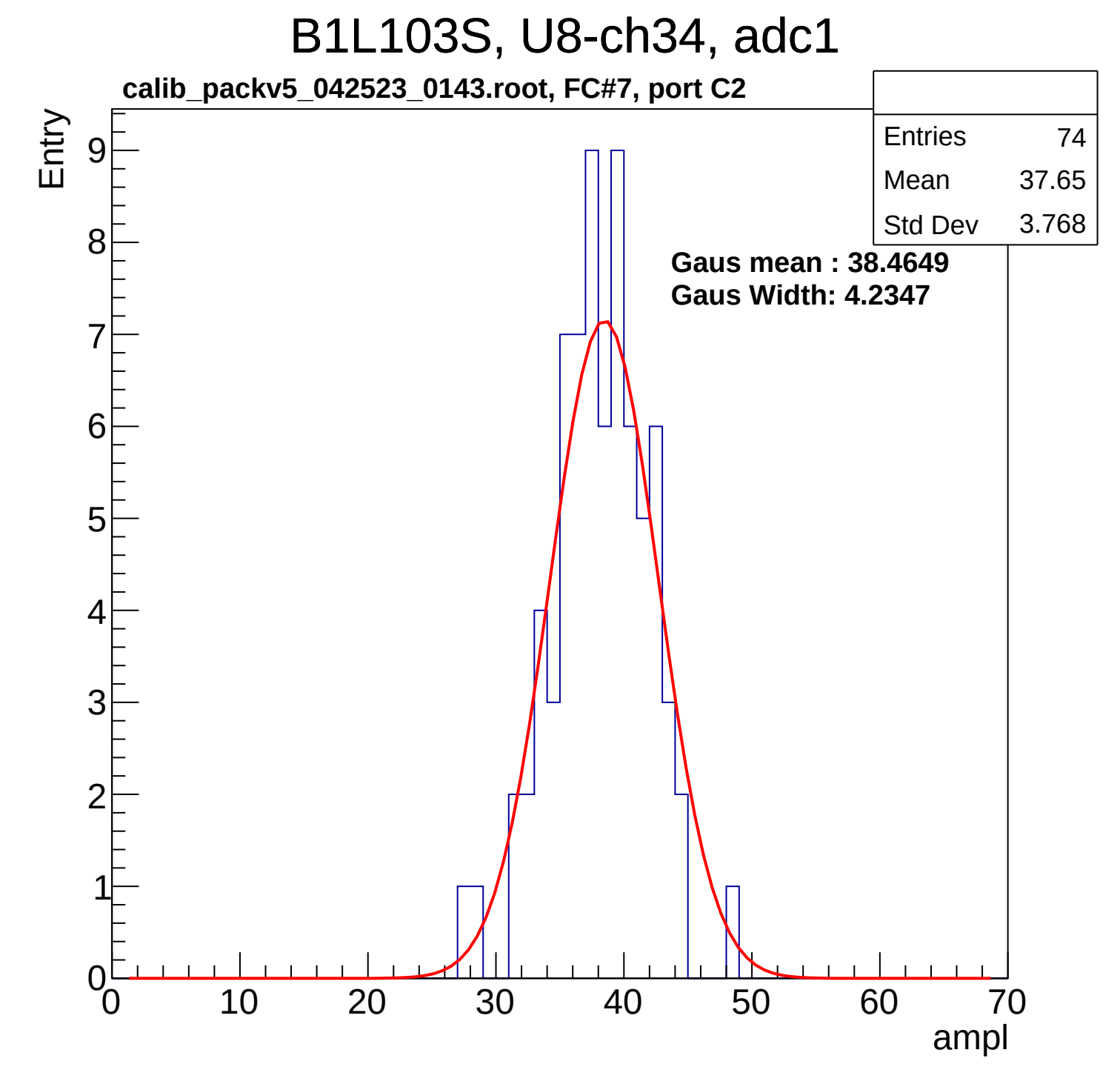

B1L103S, U8-ch33, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 55.58
Std Dev 3.55
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

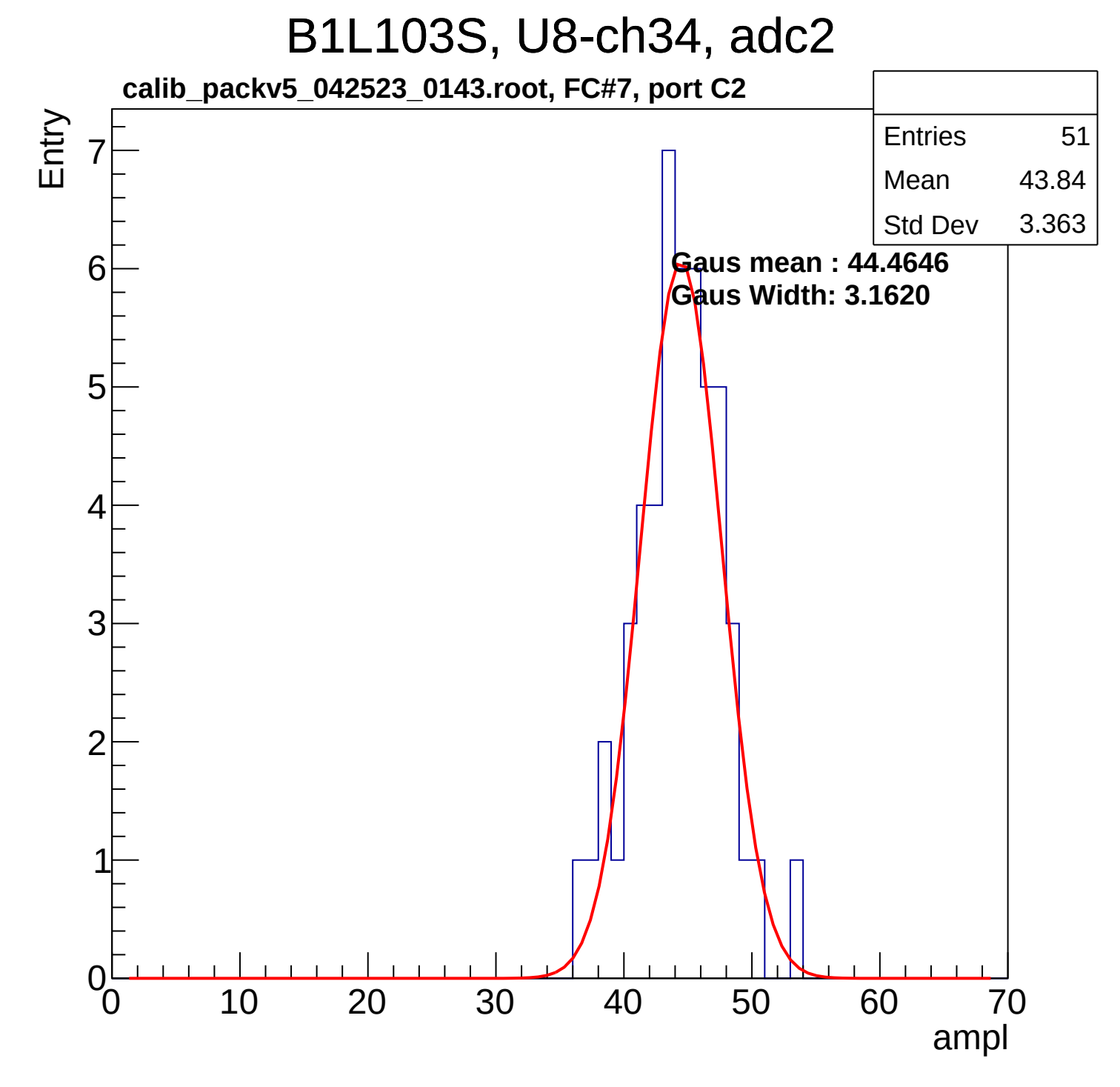

B1L103S, U8-ch33, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 59.06
Std Dev 8.617
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

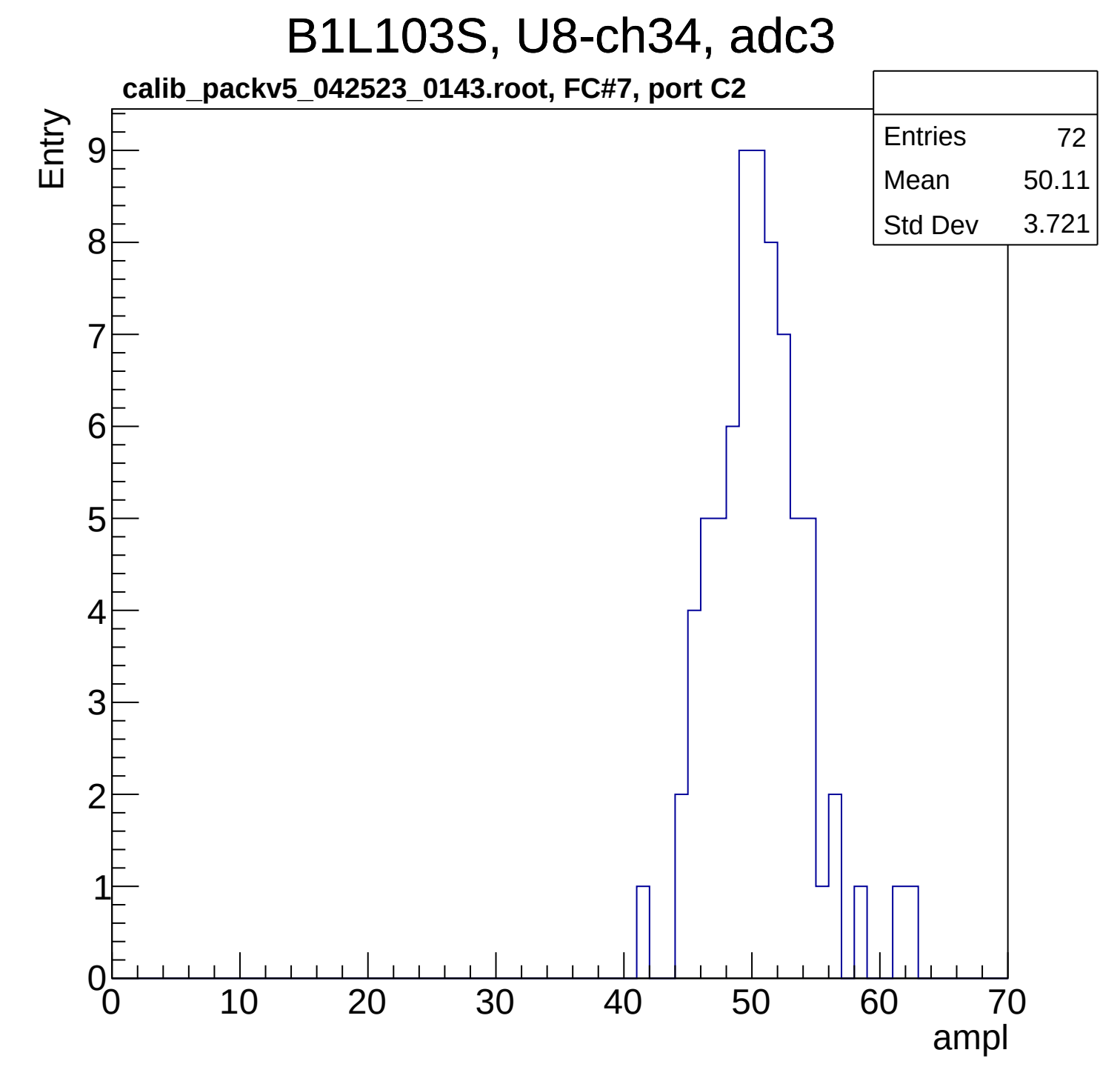

B1L103S, U8-ch33, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

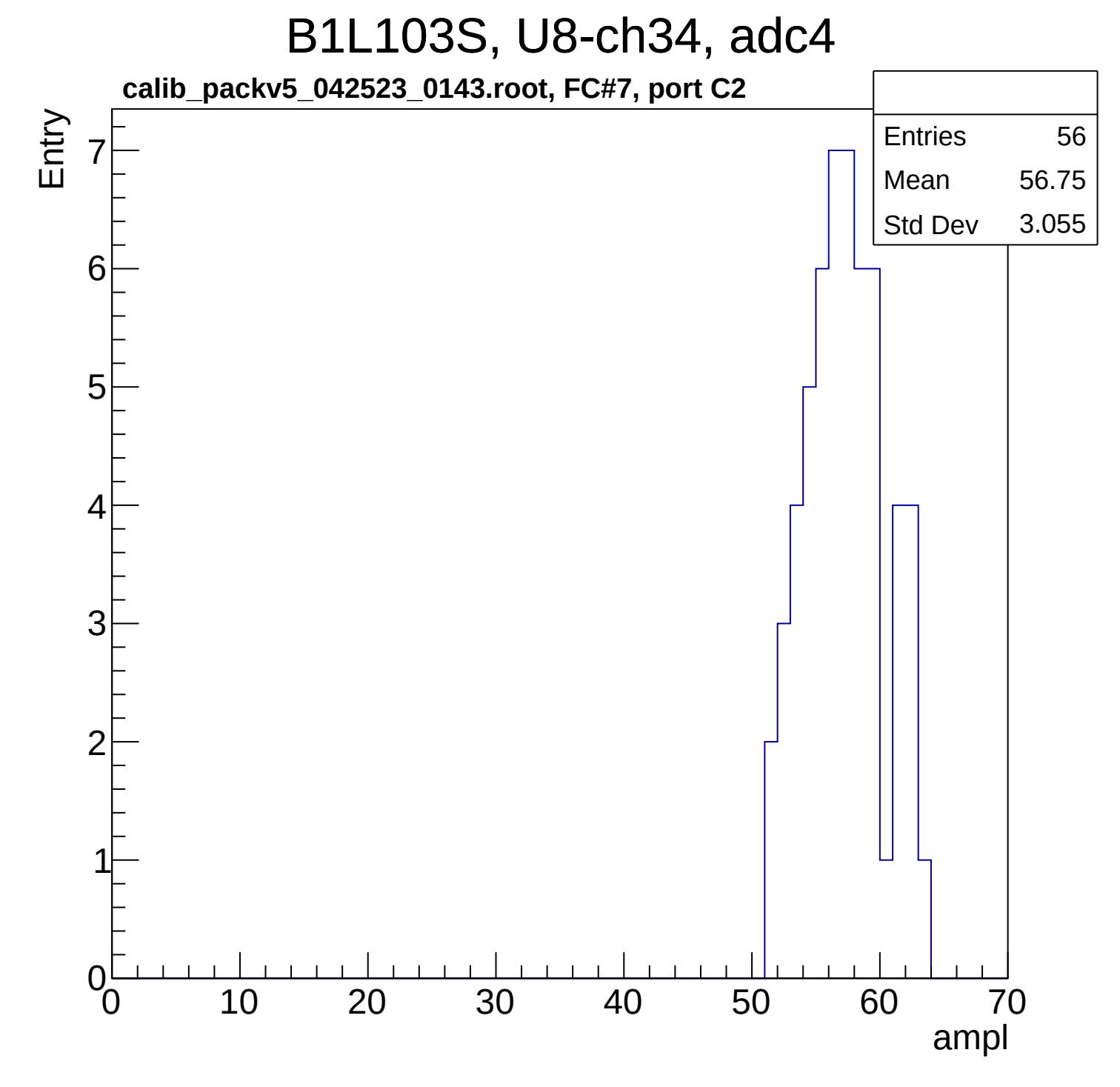

B1L103S, U8-ch33, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

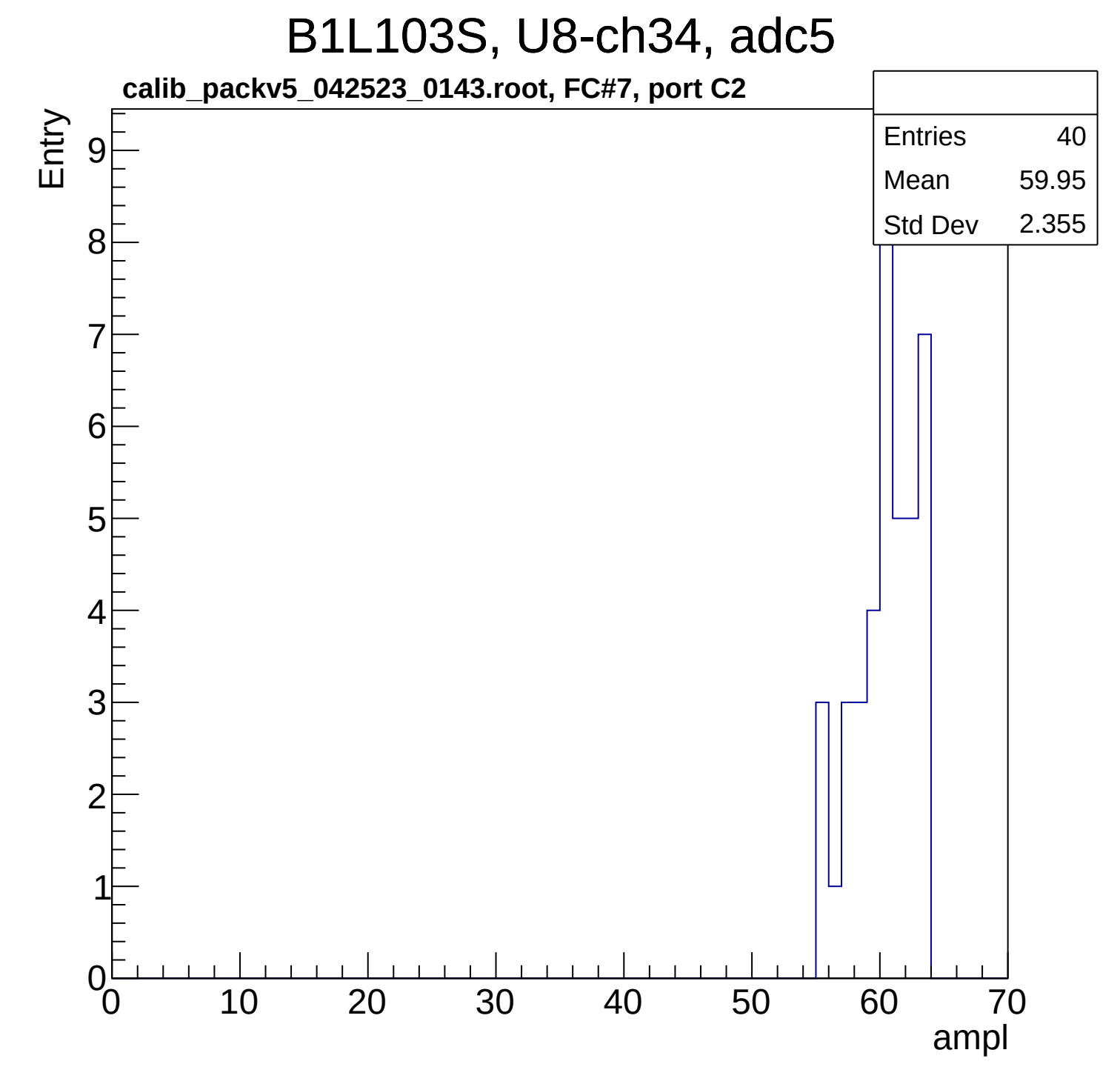

B1L103S, U8-ch34, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 29.84
Std Dev 5.025
Gaus mean : 30.8790
Gaus Width: 3.9941
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

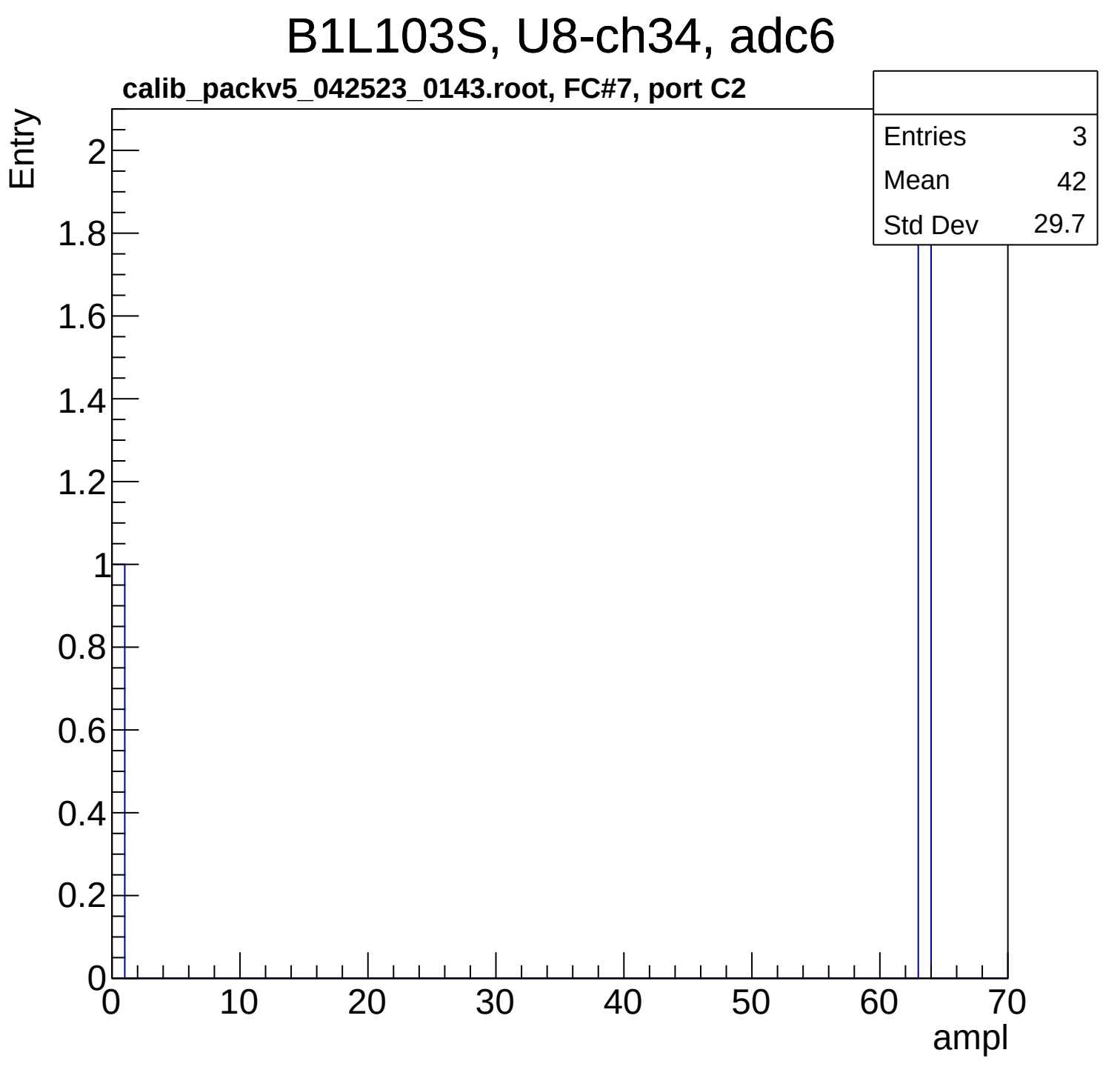

B1L103S, U8-ch34, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 37.65
Std Dev 3.768
Gaus mean : 38.4649
Gaus Width: 4.2347
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

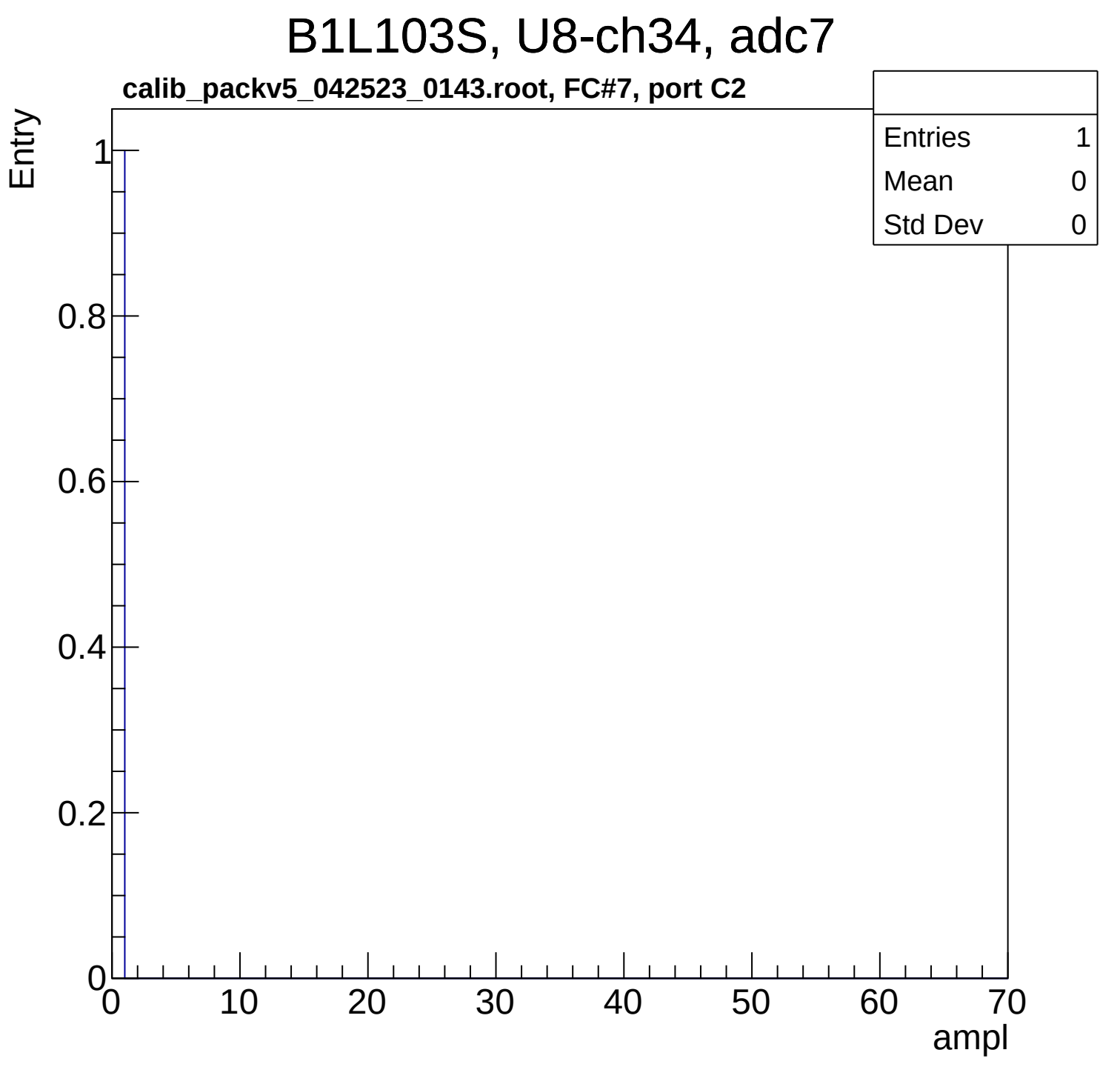

B1L103S, U8-ch34, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 43.84
Std Dev 3.363
Gaus mean : 44.4646
Gaus Width: 3.1620
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

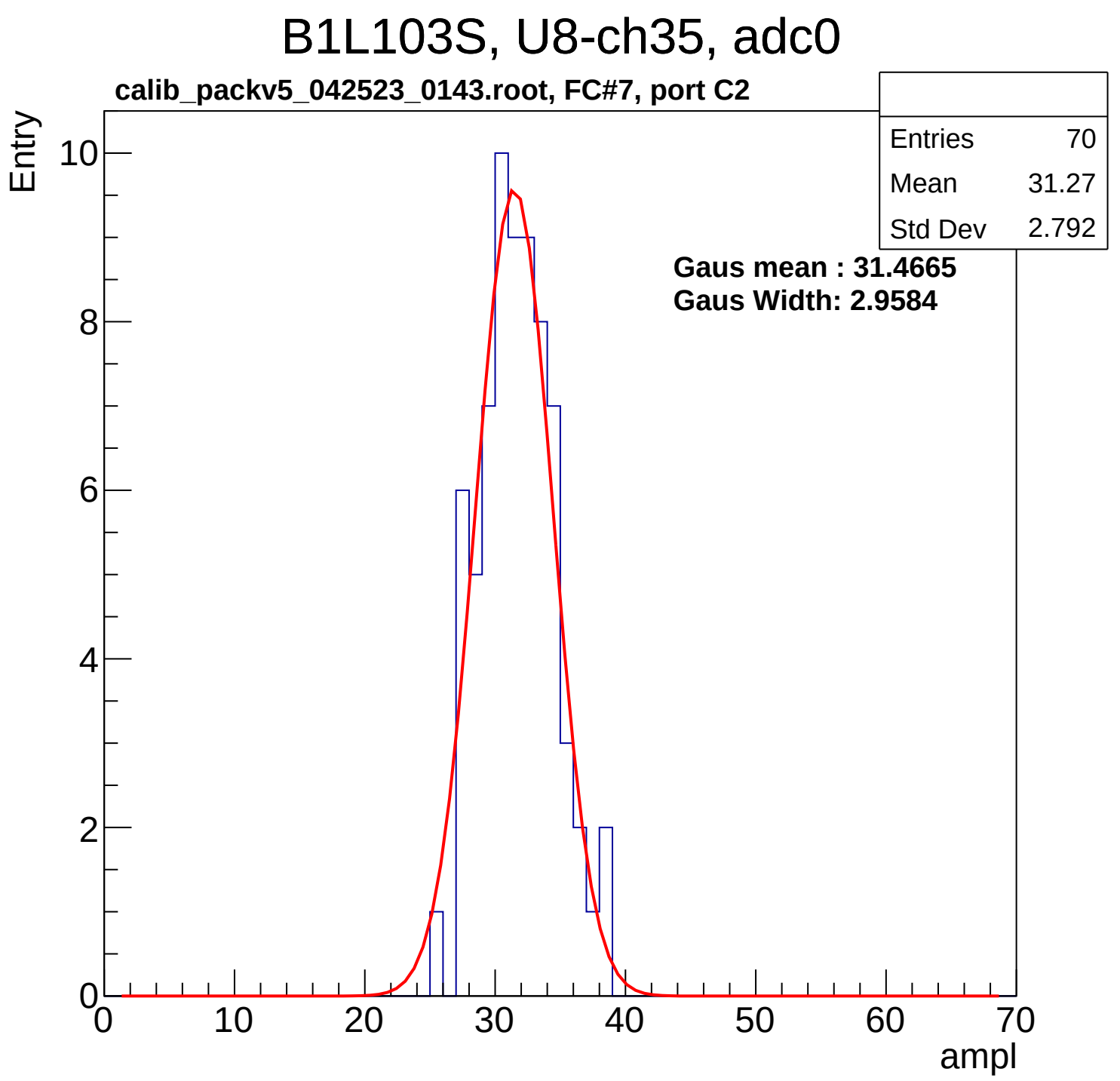

B1L103S, U8-ch34, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 50.11
Std Dev 3.721
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

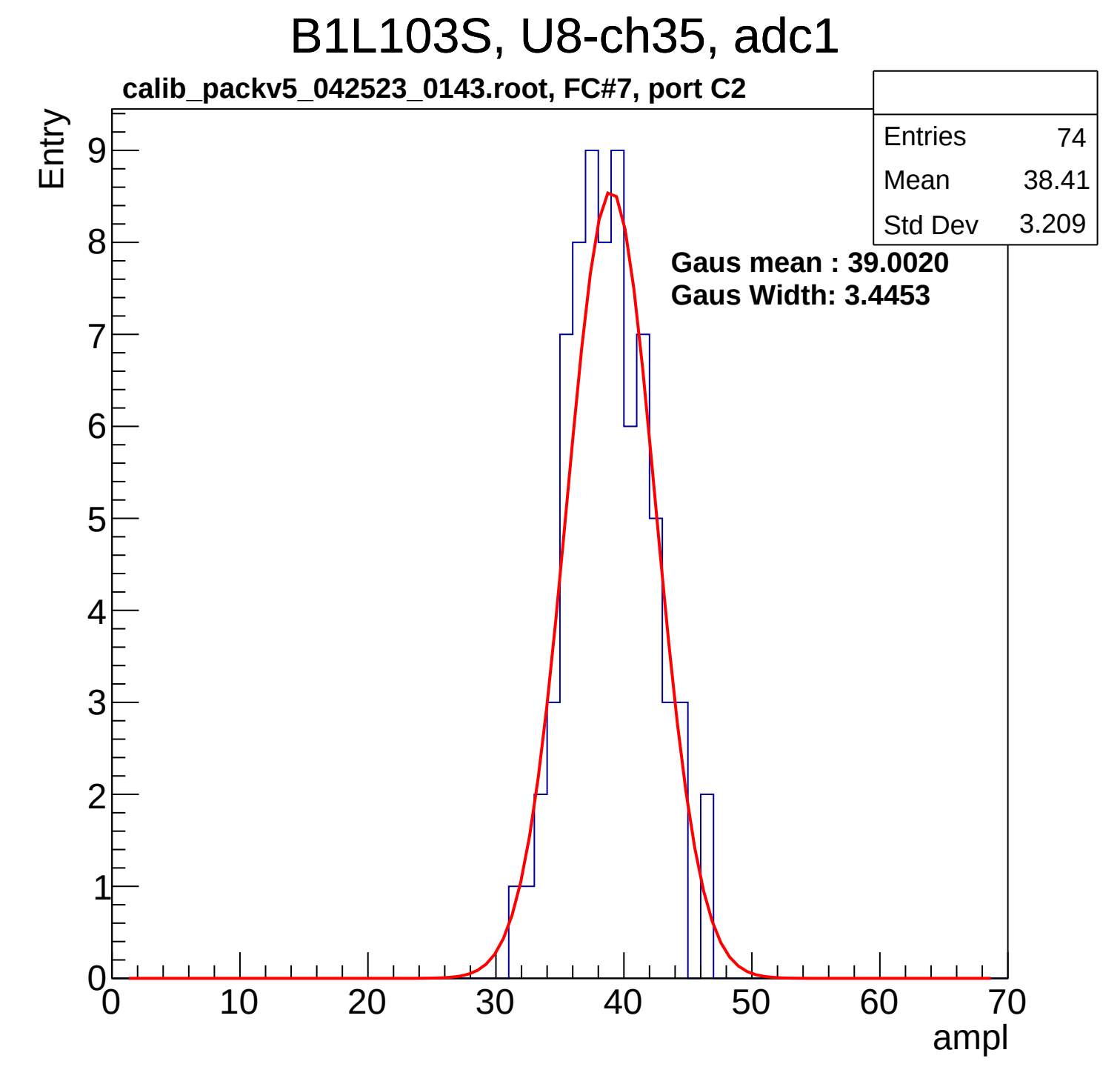

B1L103S, U8-ch34, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 56.75
Std Dev 3.055
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

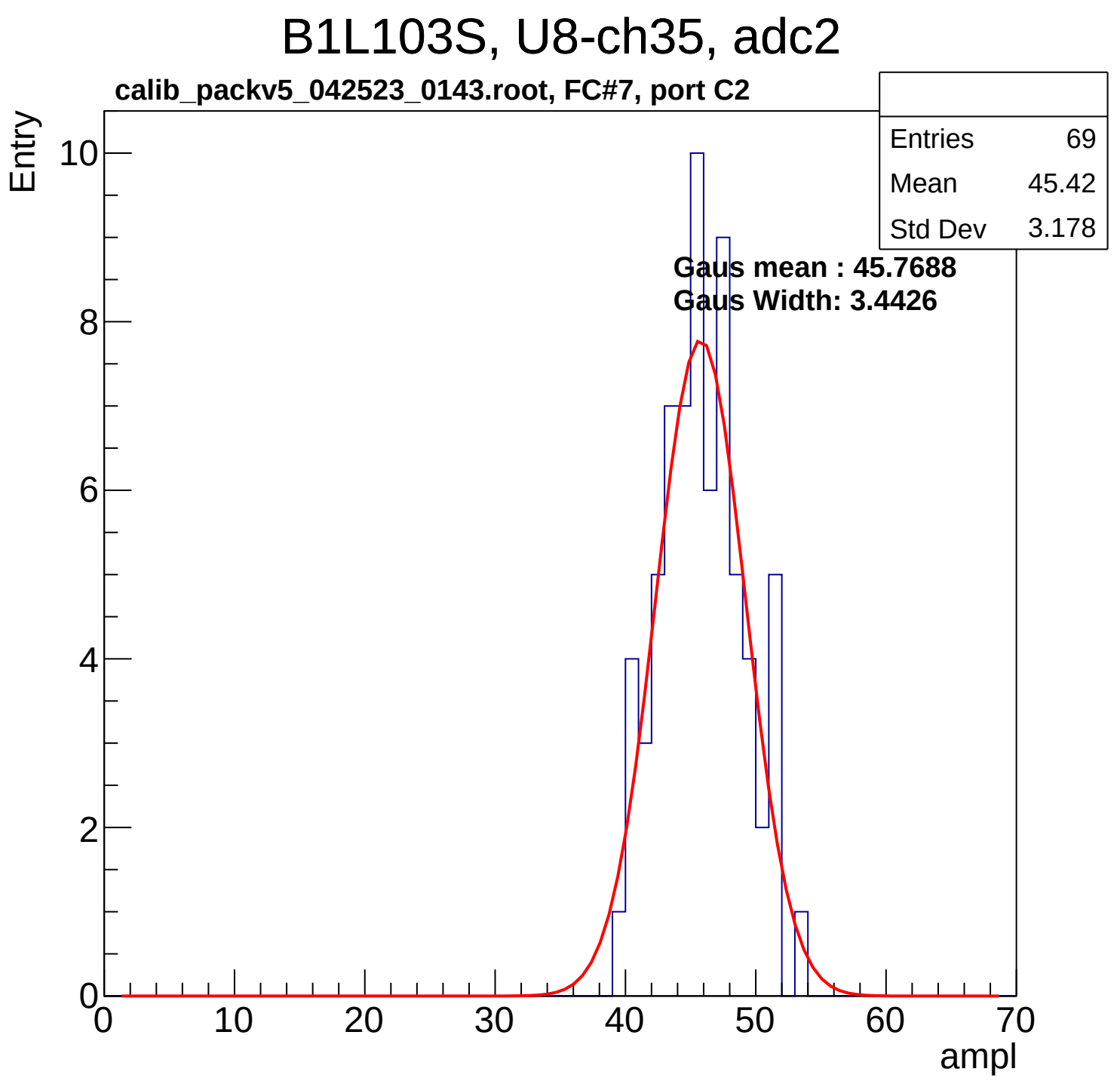

B1L103S, U8-ch34, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 40
Mean 59.95
Std Dev 2.355
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

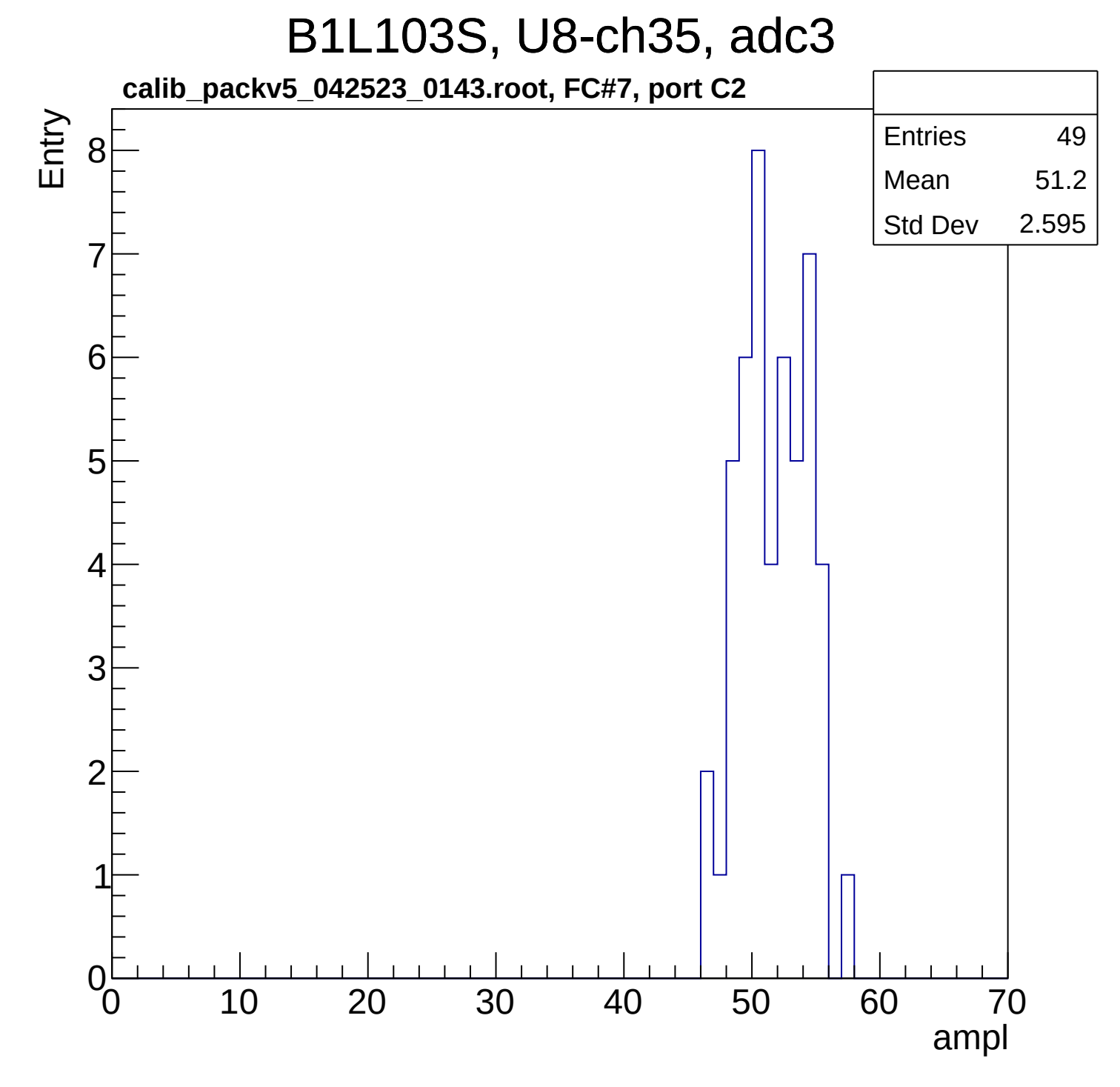

B1L103S, U8-ch34, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 42
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

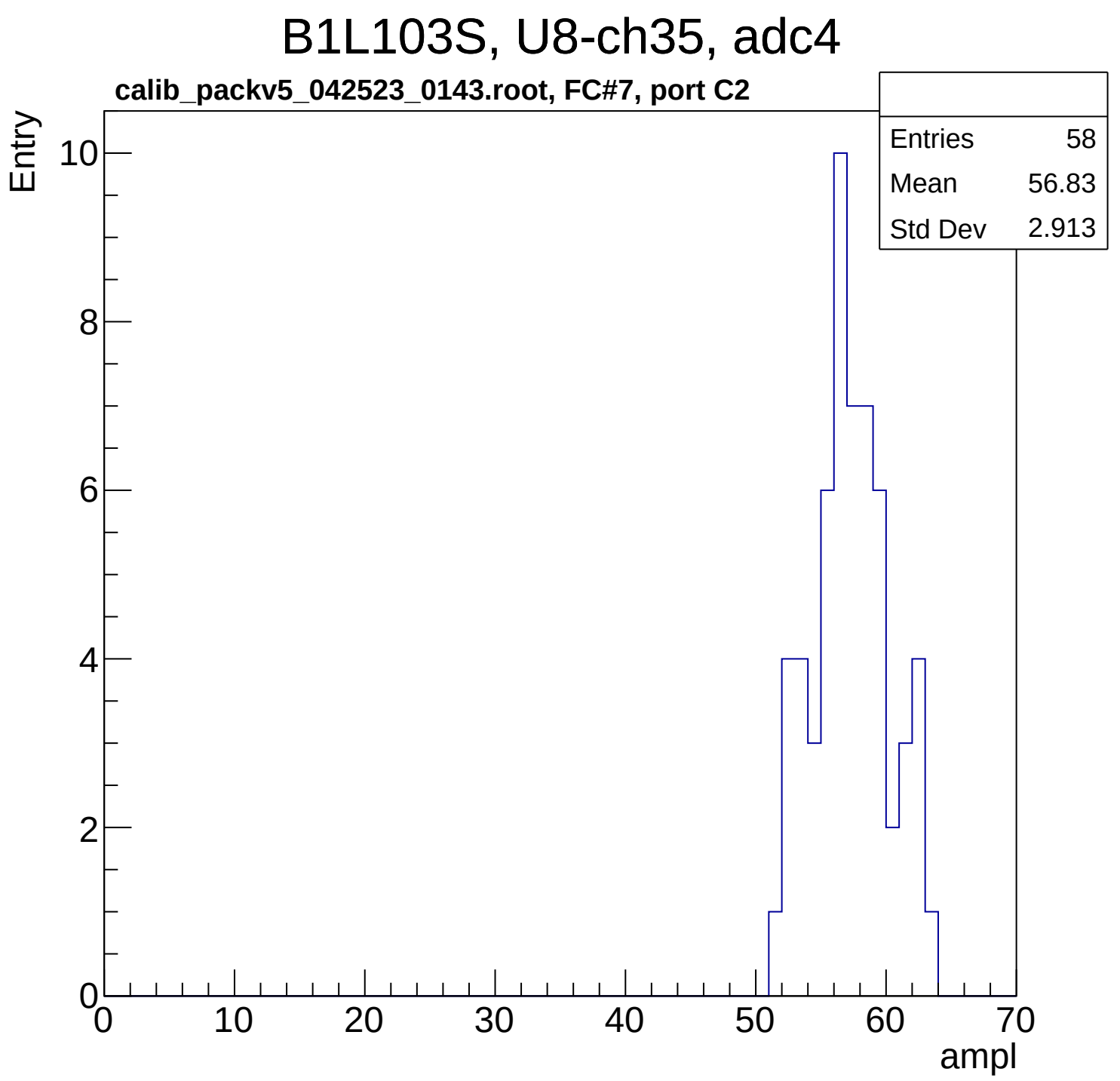

B1L103S, U8-ch34, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

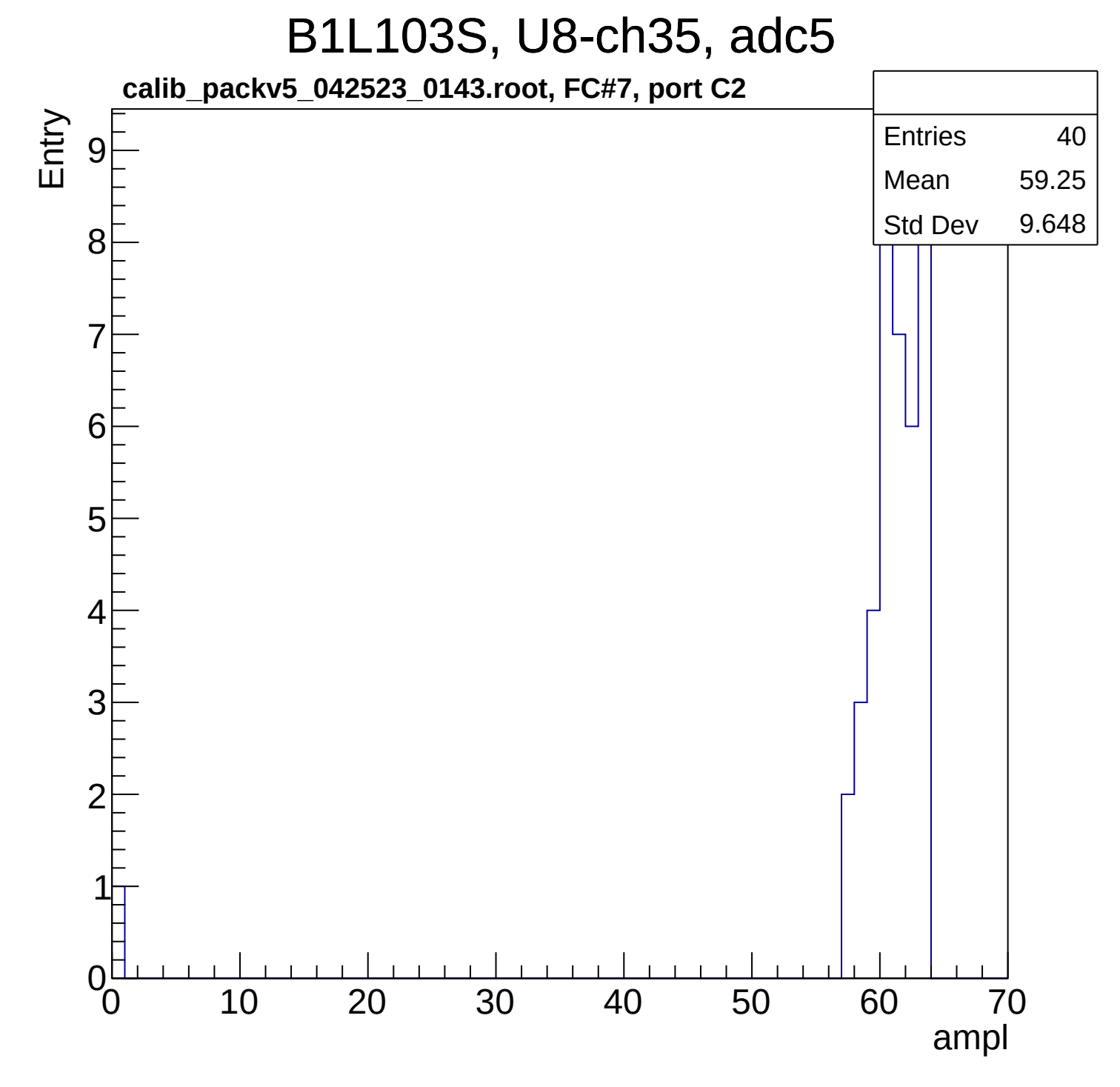

B1L103S, U8-ch35, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 31.27
Std Dev 2.792
Gaus mean : 31.4665
Gaus Width: 2.9584
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

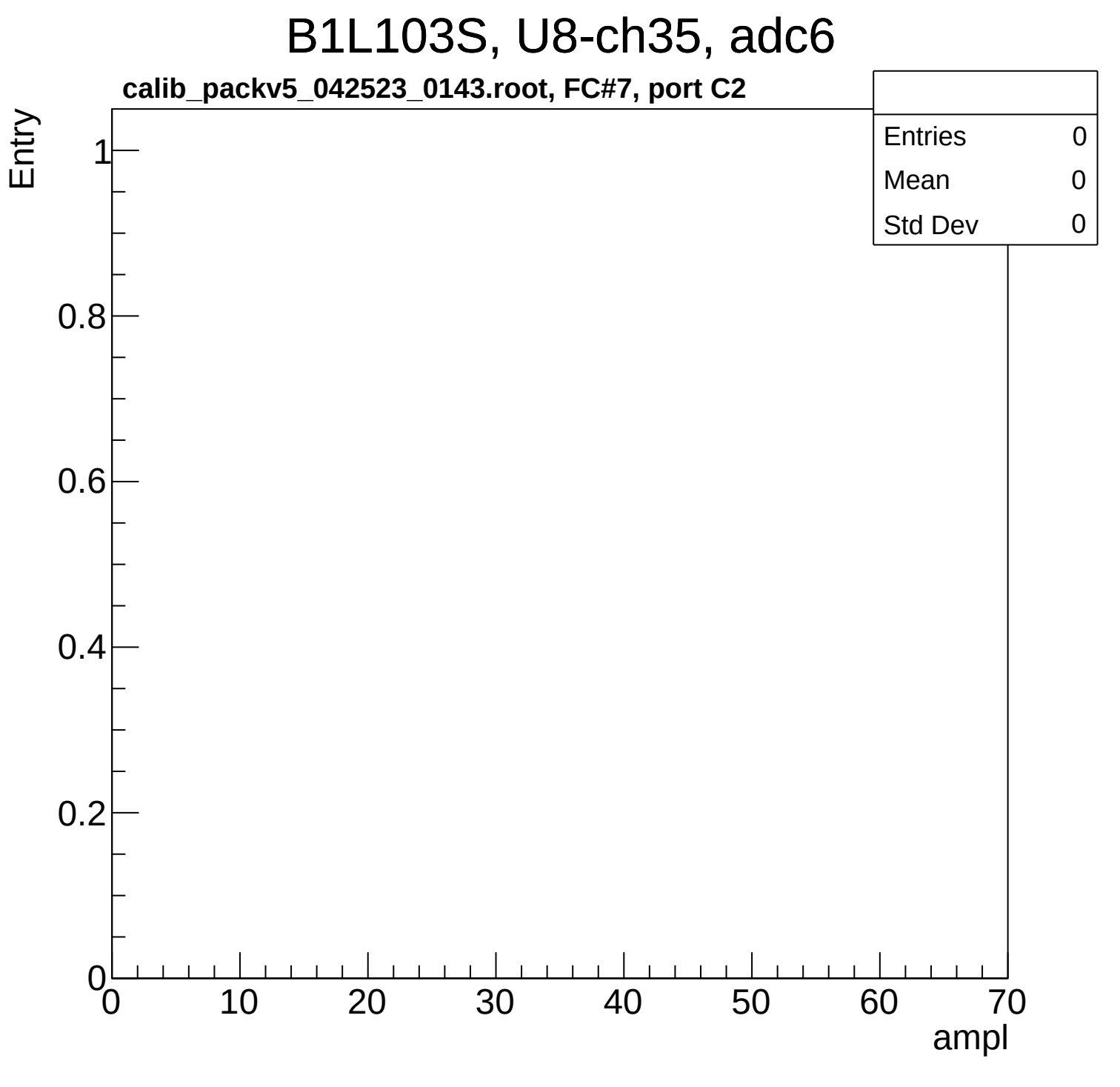

B1L103S, U8-ch35, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 38.41
Std Dev 3.209
Gaus mean : 39.0020
Gaus Width: 3.4453
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

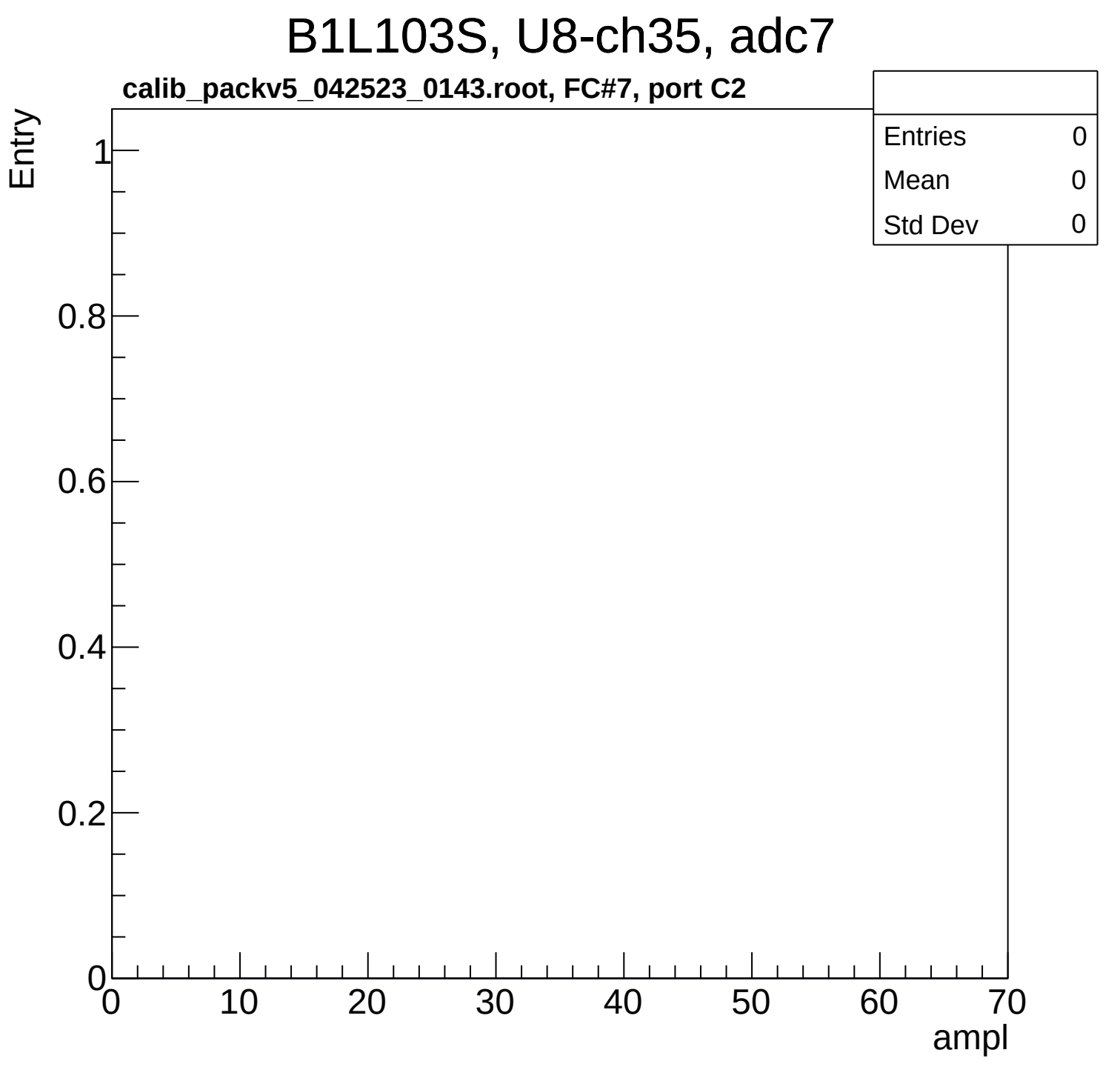

B1L103S, U8-ch35, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 45.42
Std Dev 3.178
Gaus mean : 45.7688
Gaus Width: 3.4426
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

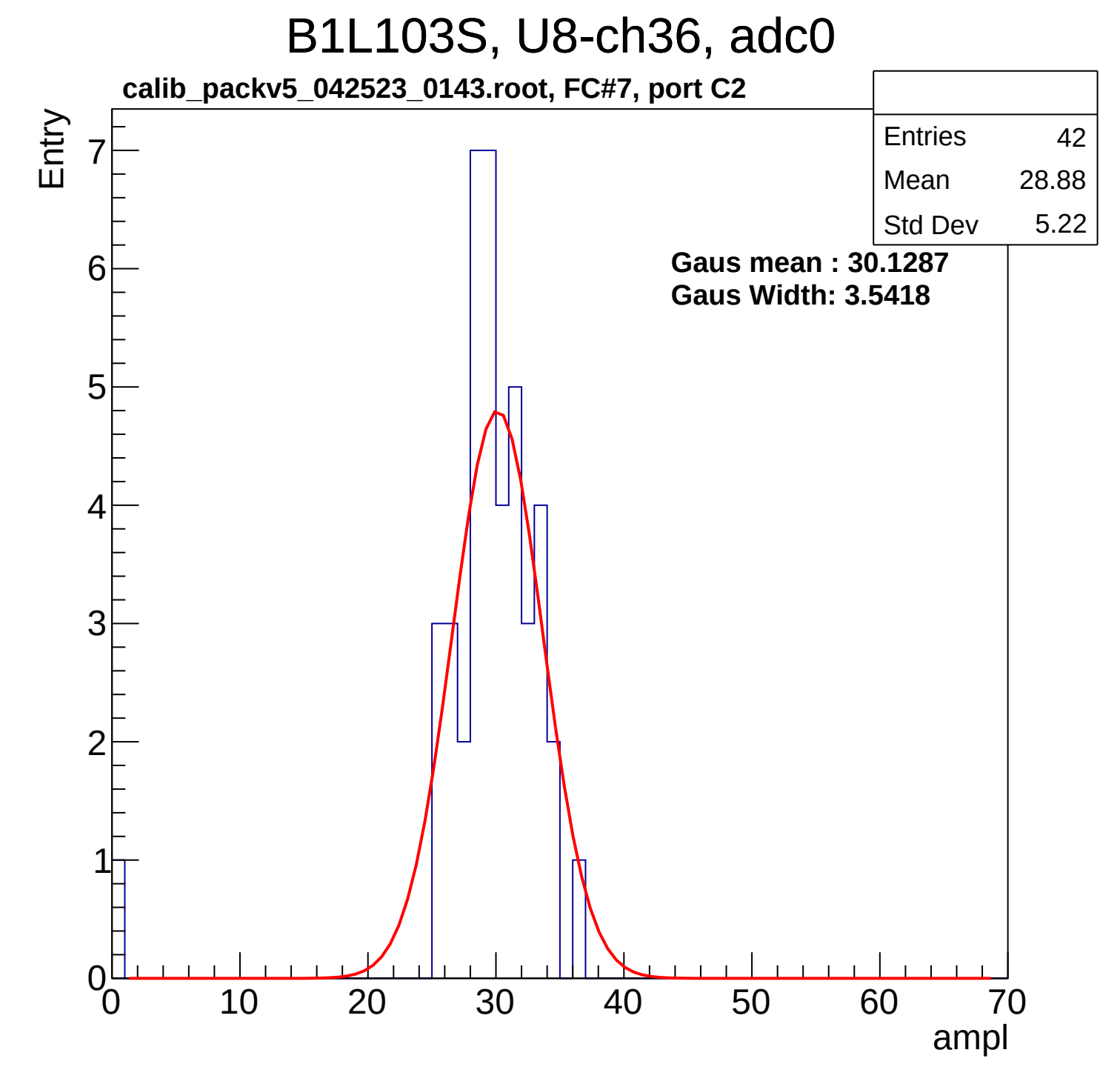

B1L103S, U8-ch35, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 51.2
Std Dev 2.595
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

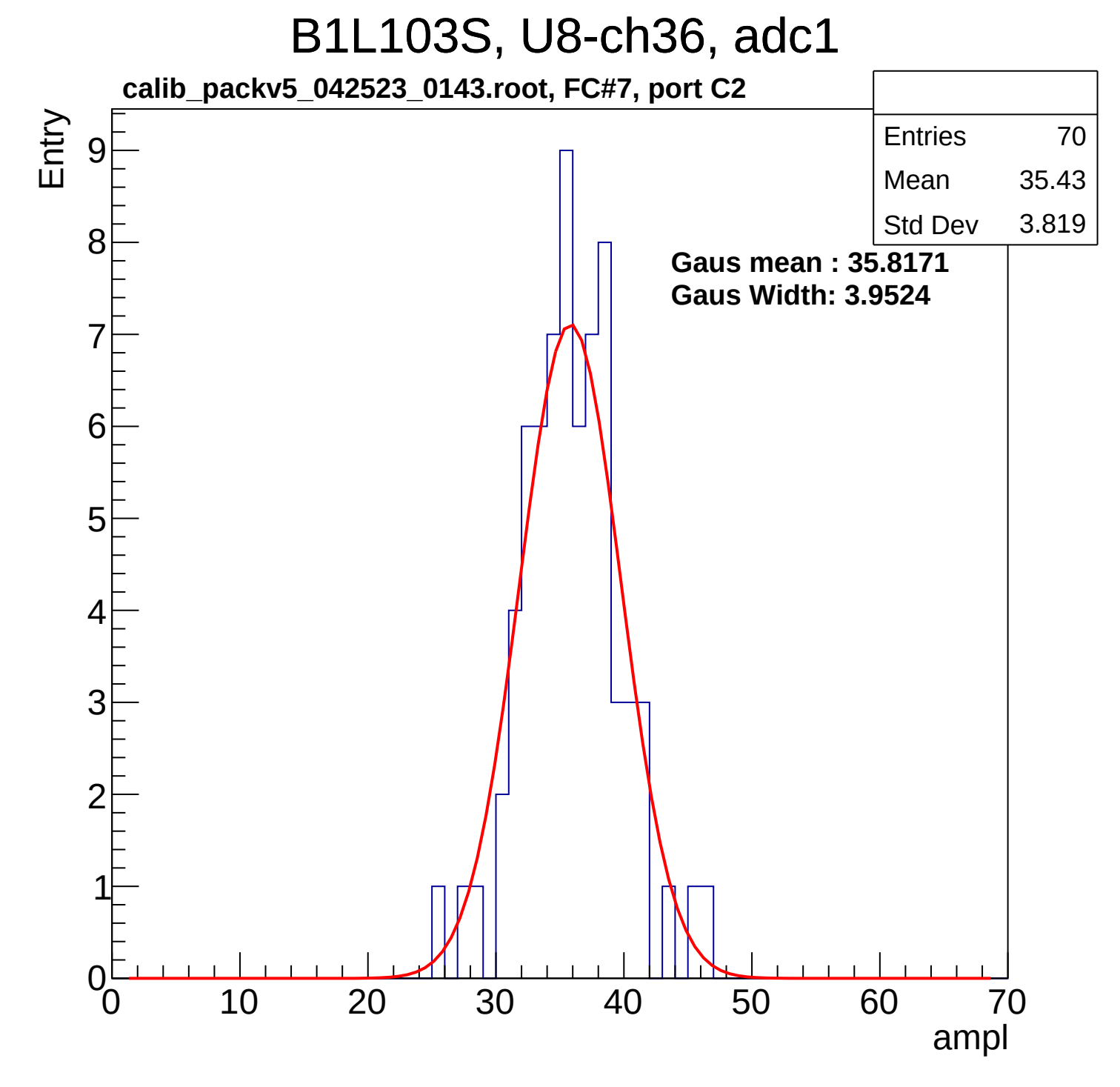

B1L103S, U8-ch35, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 56.83
Std Dev 2.913
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

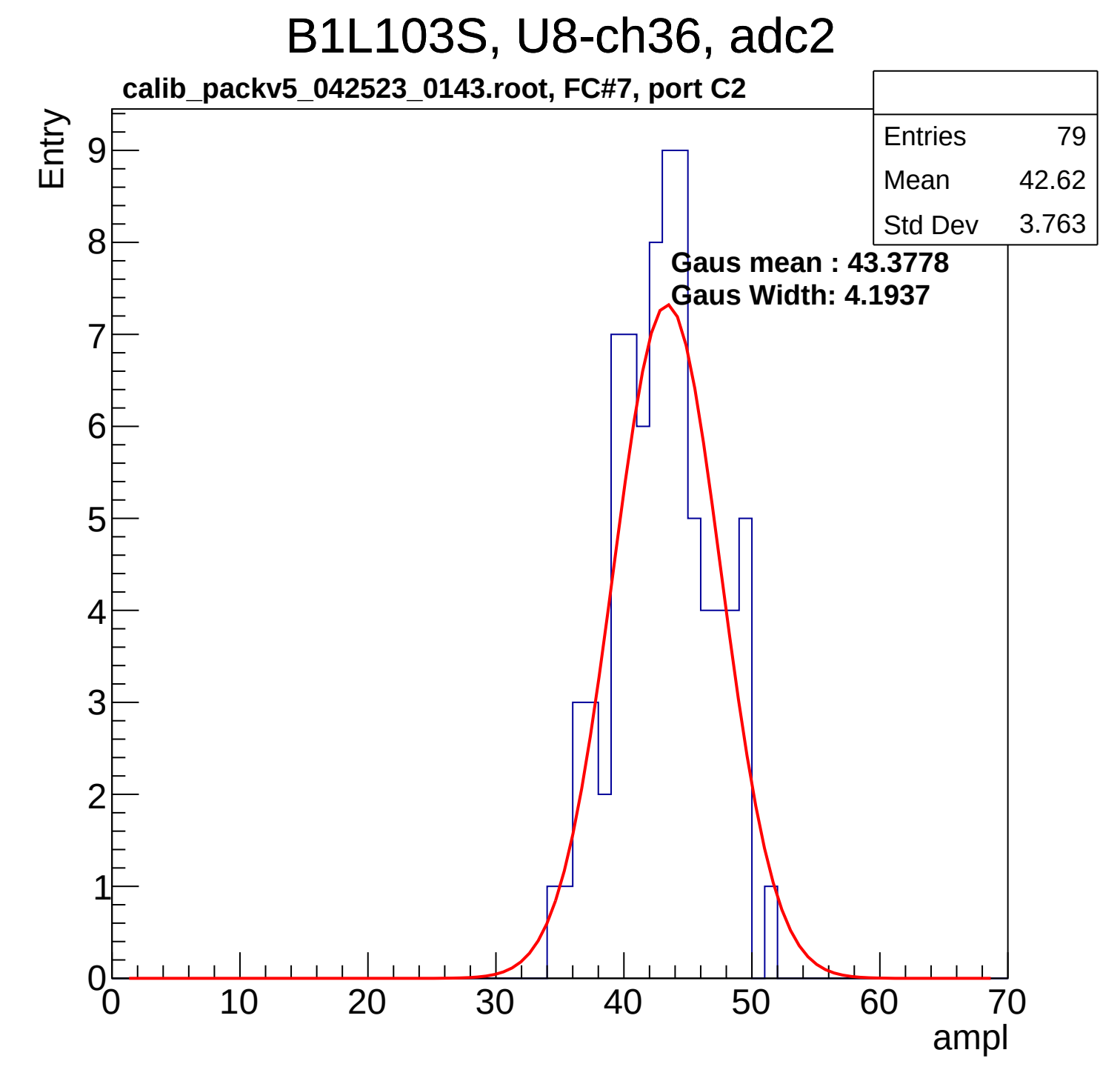

B1L103S, U8-ch35, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 40
Mean 59.25
Std Dev 9.648
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

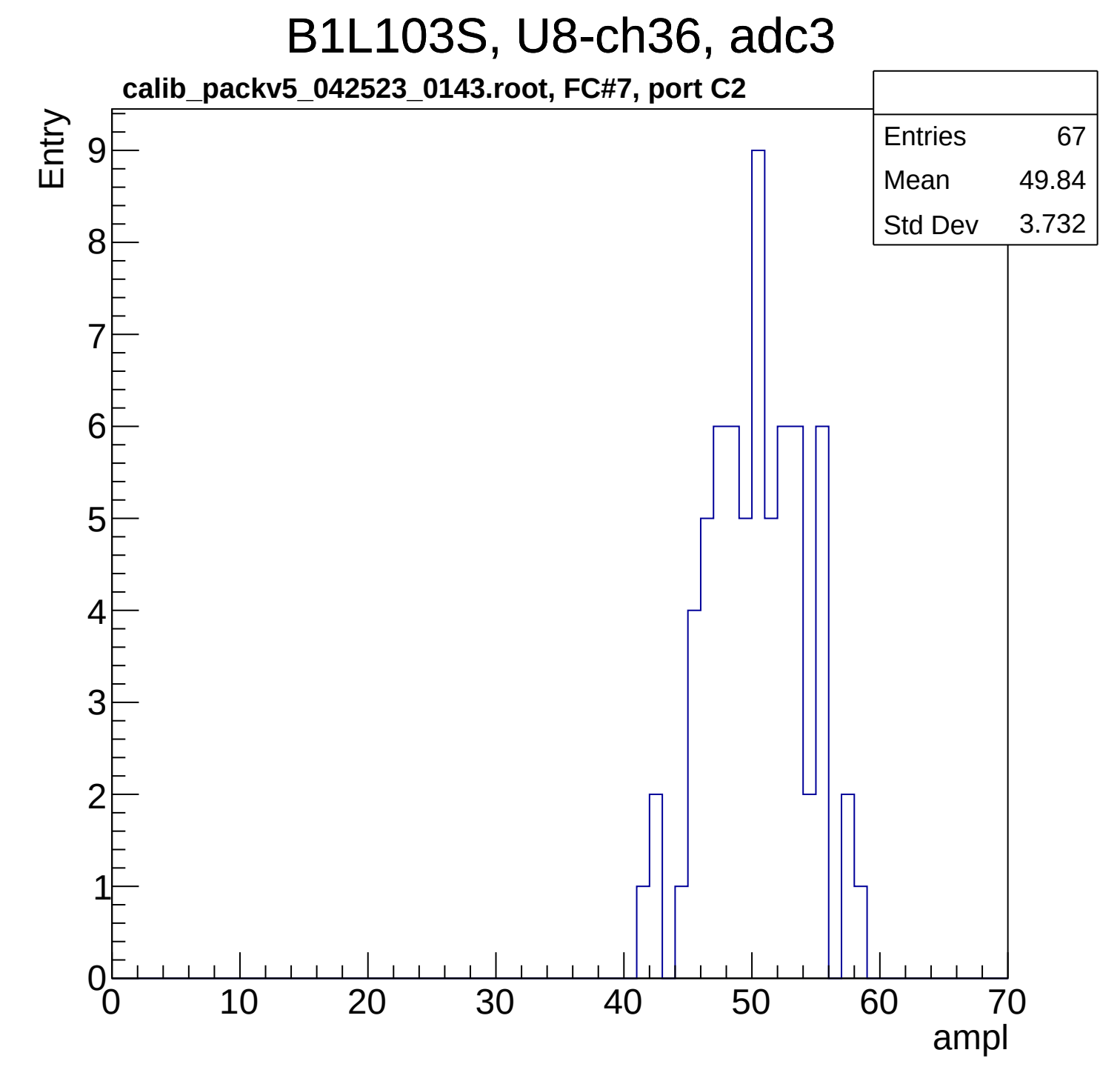

B1L103S, U8-ch35, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

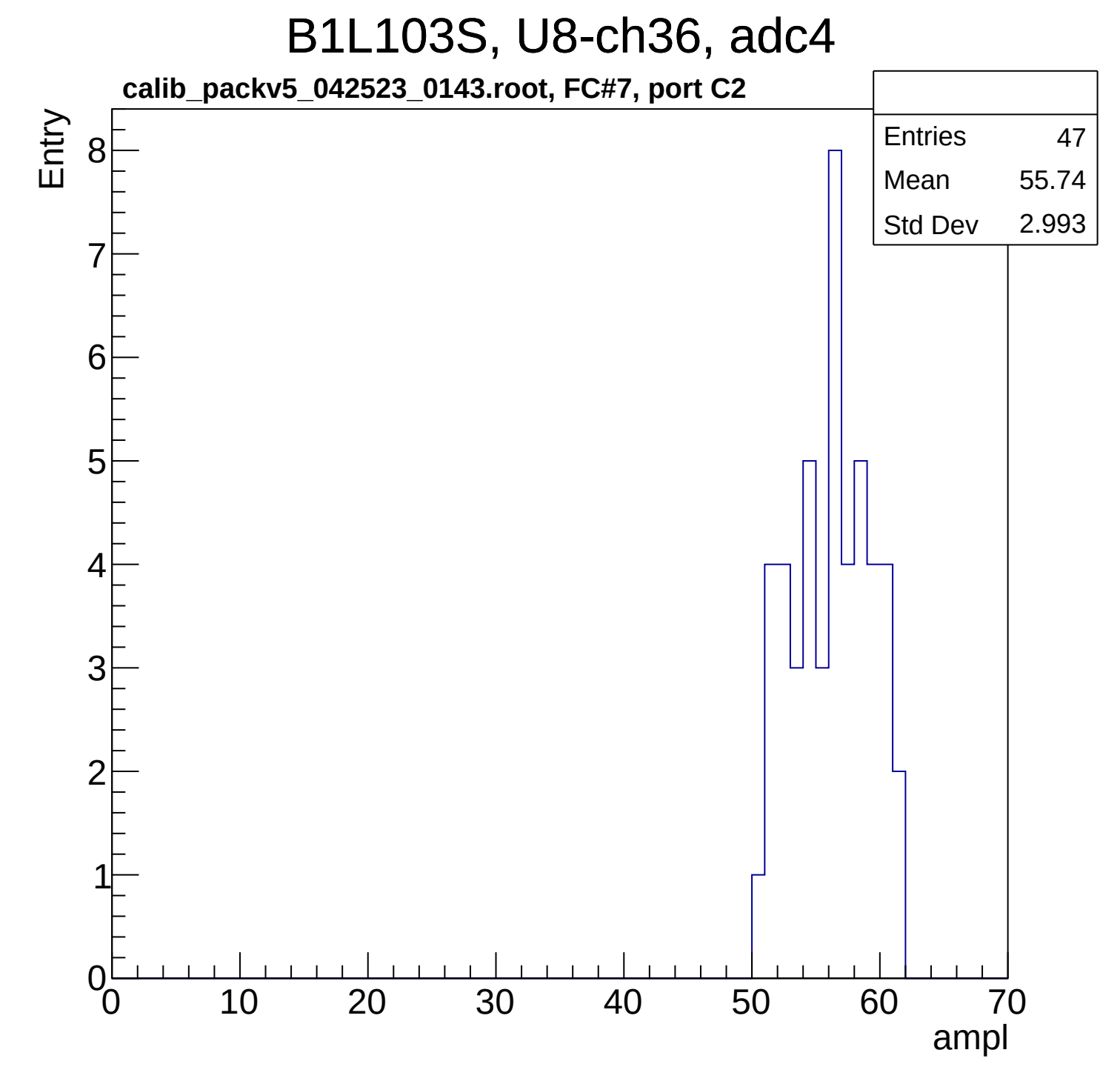

B1L103S, U8-ch35, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

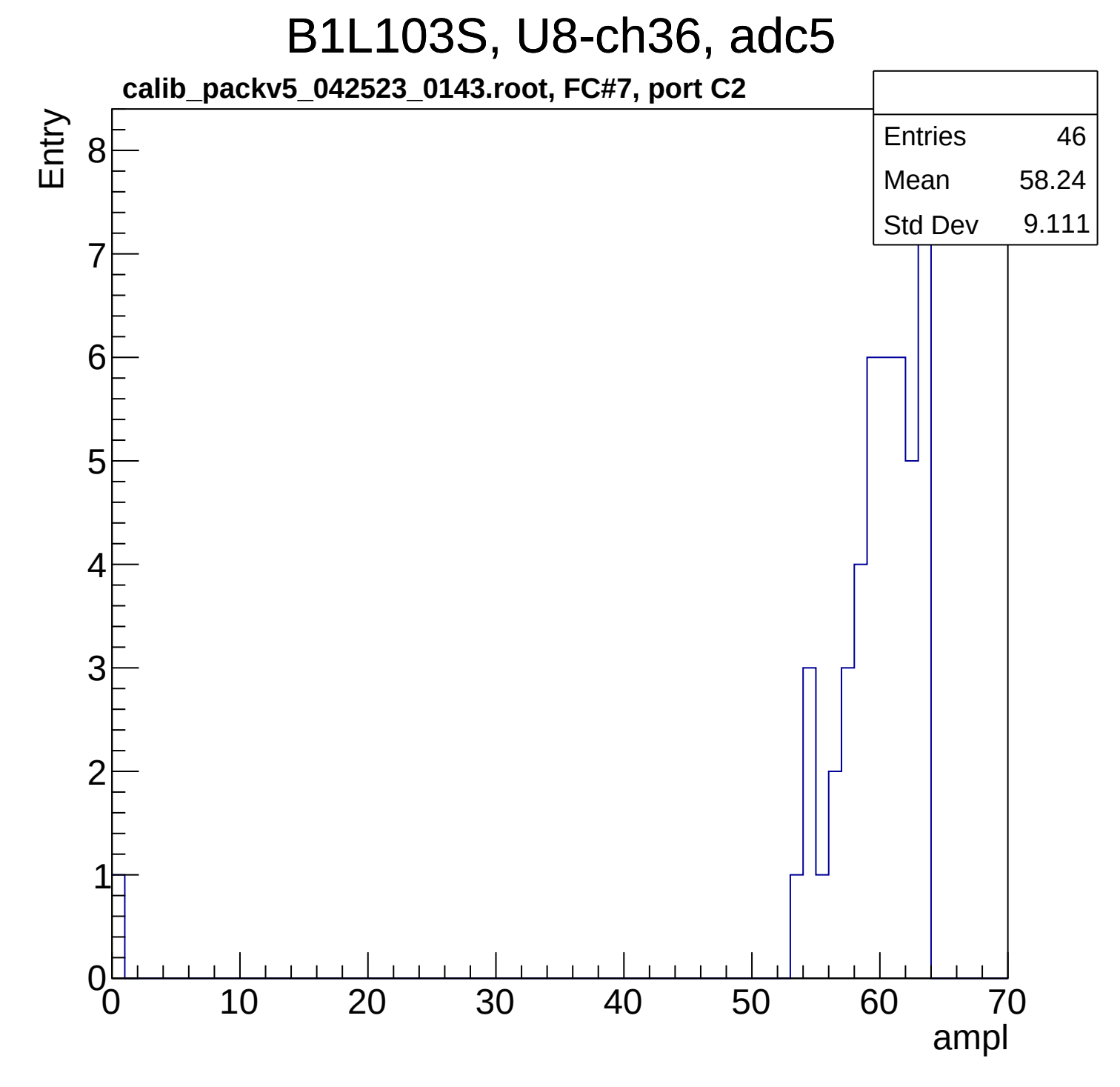

B1L103S, U8-ch36, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 42
Mean 28.88
Std Dev 5.22
Gaus mean : 30.1287
Gaus Width: 3.5418
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

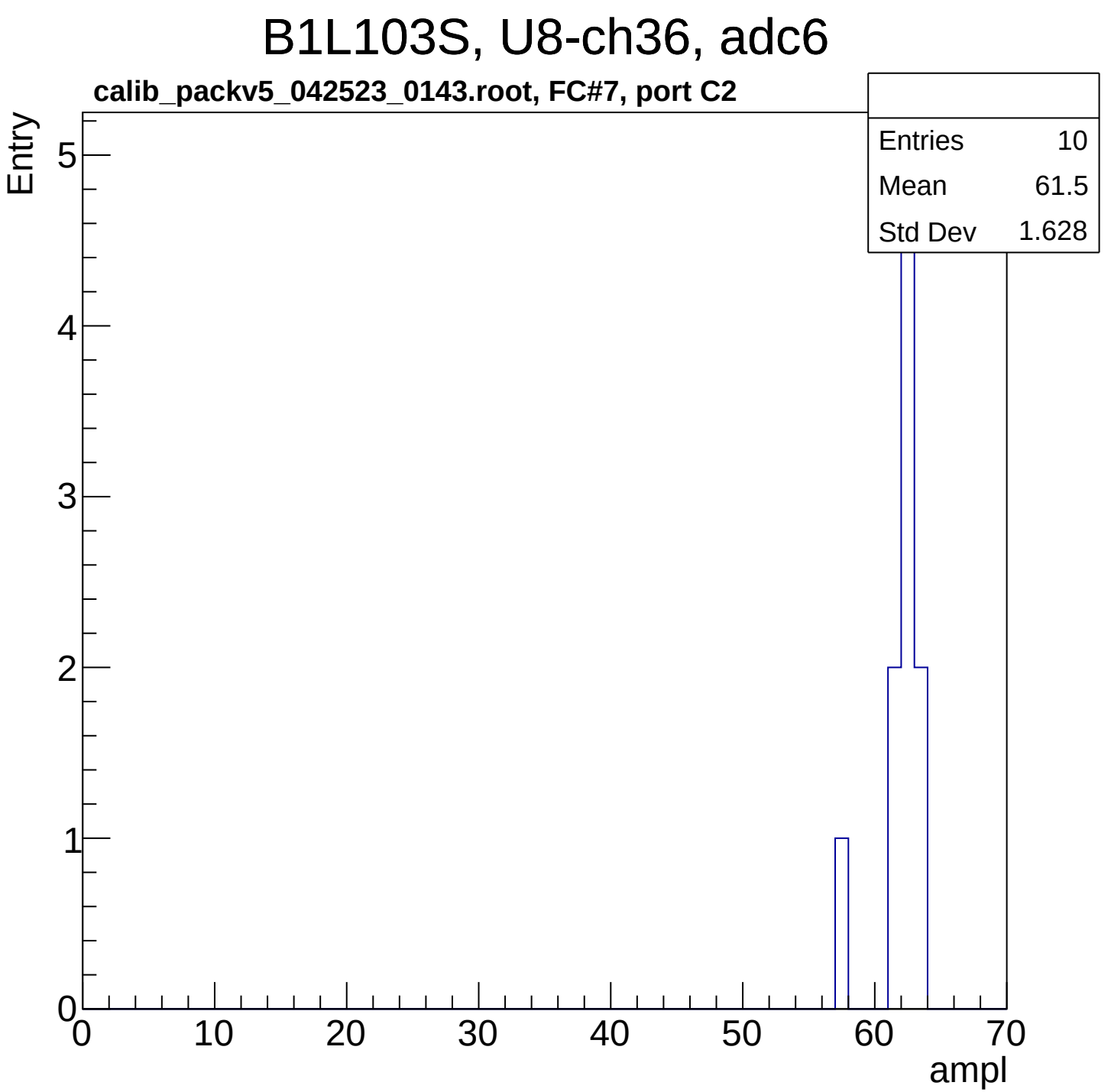

B1L103S, U8-ch36, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 35.43
Std Dev 3.819
Gaus mean : 35.8171
Gaus Width: 3.9524
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

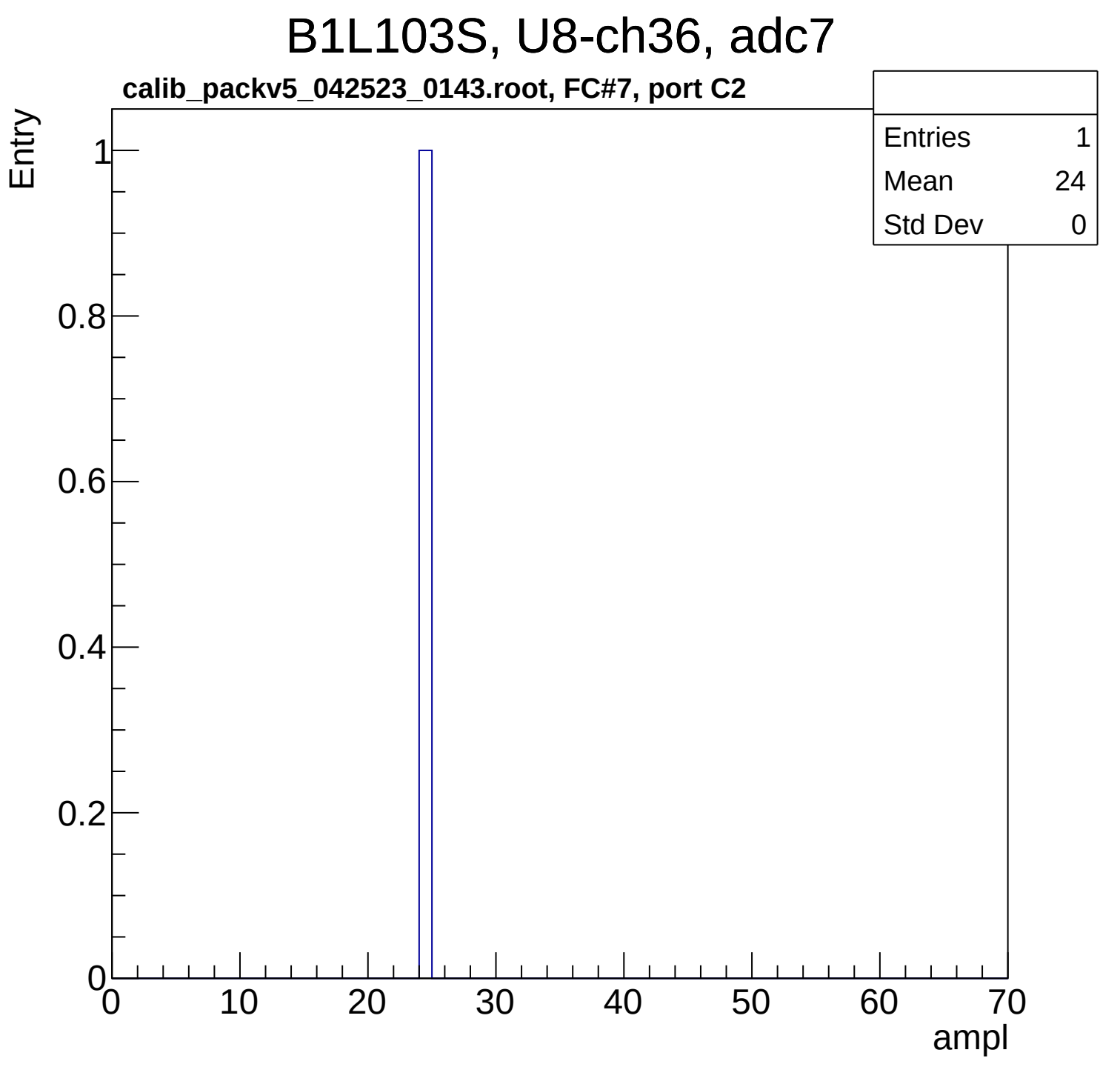

B1L103S, U8-ch36, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 79
Mean 42.62
Std Dev 3.763
Gaus mean : 43.3778
Gaus Width: 4.1937
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

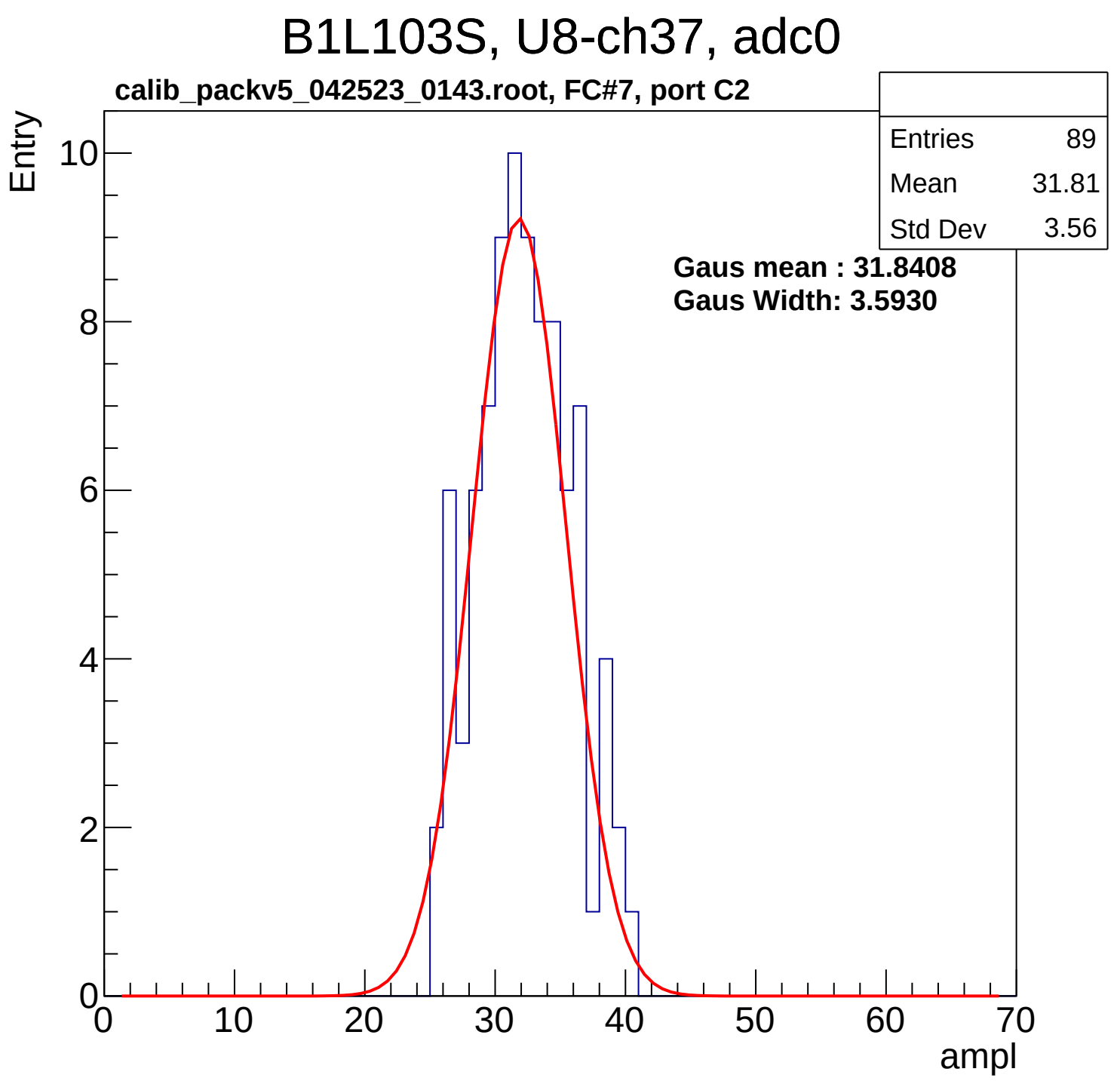

B1L103S, U8-ch36, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 49.84
Std Dev 3.732
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

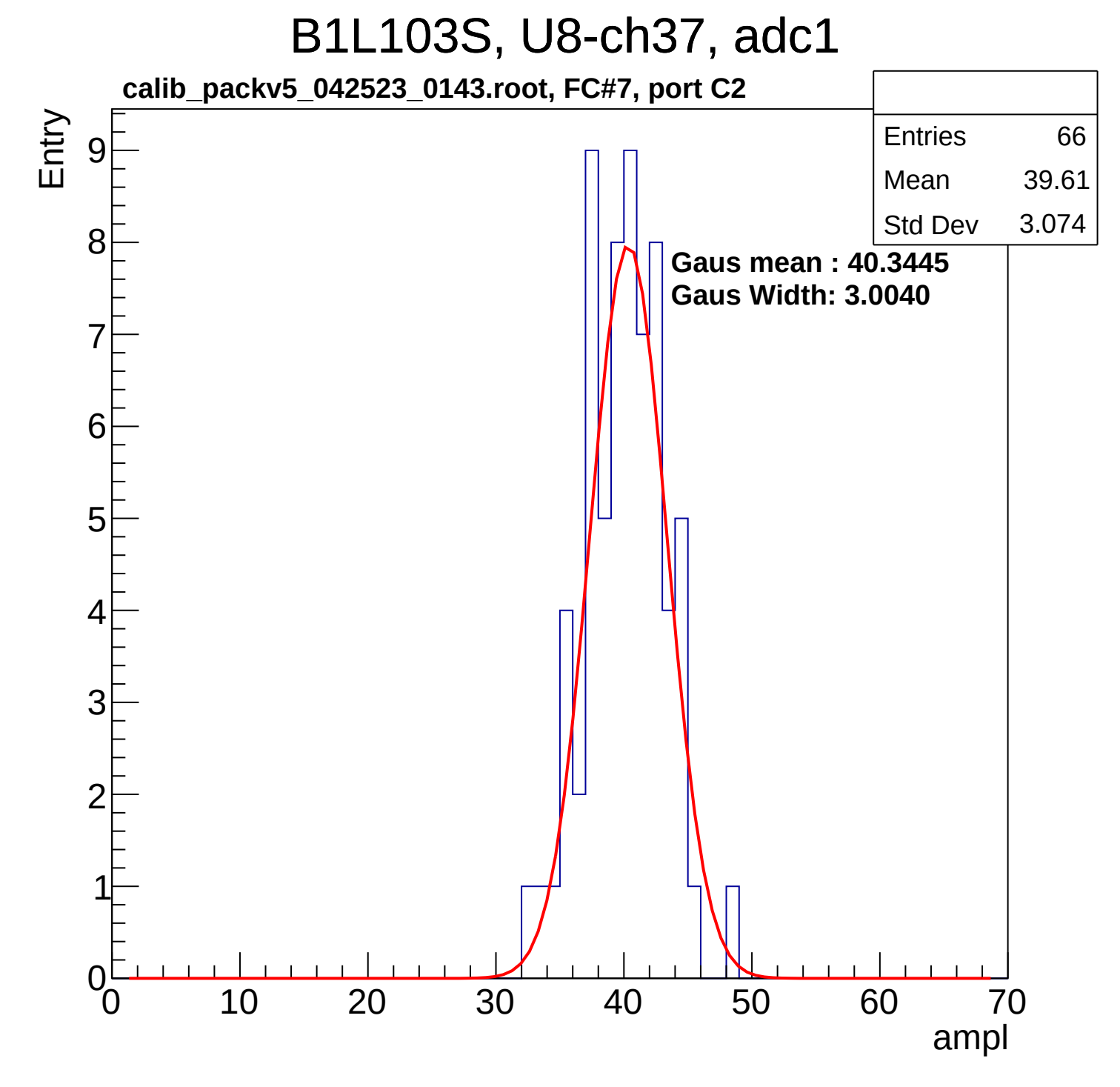

B1L103S, U8-ch36, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 55.74
Std Dev 2.993
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

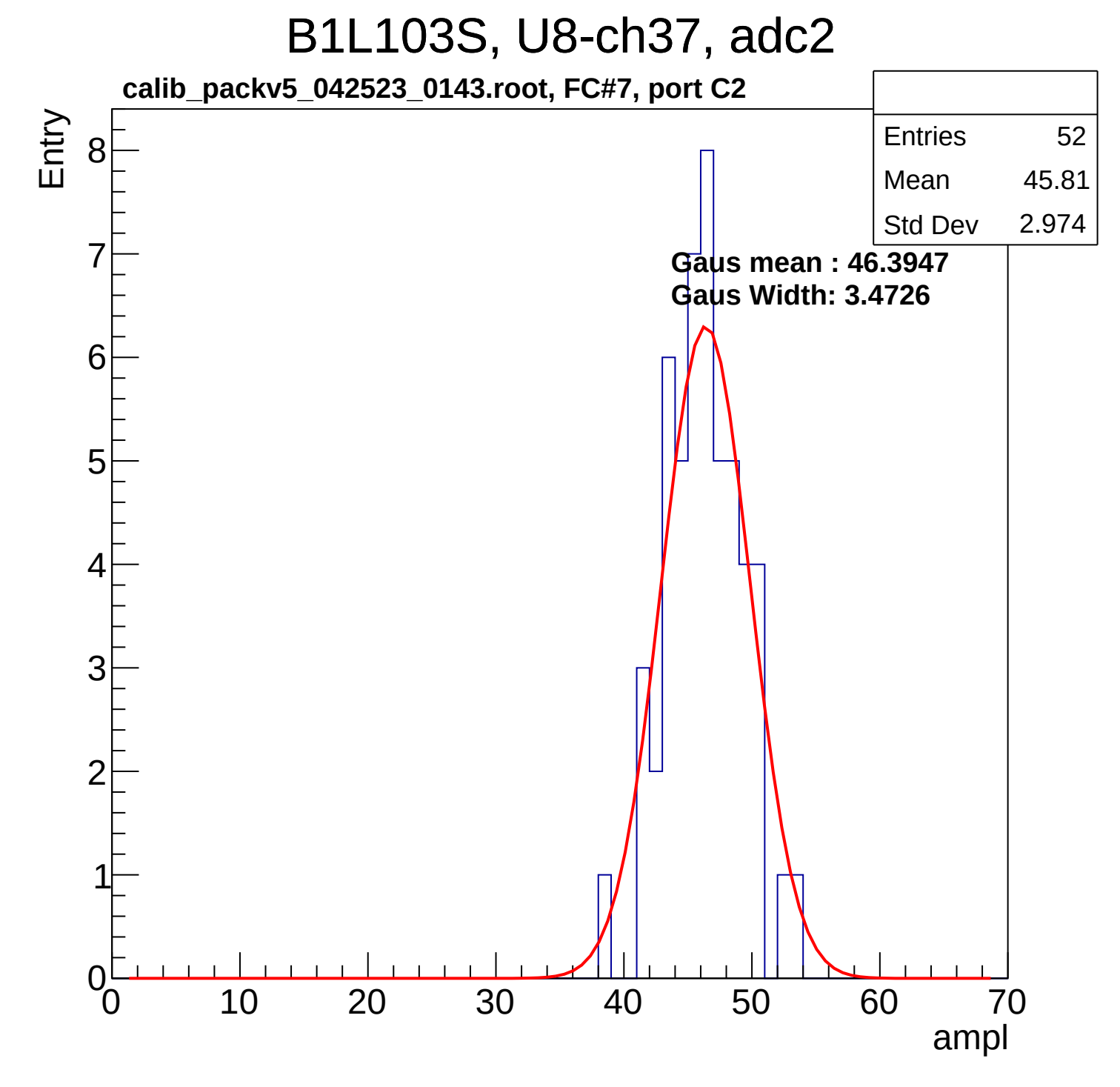

B1L103S, U8-ch36, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 46
Mean 58.24
Std Dev 9.111
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

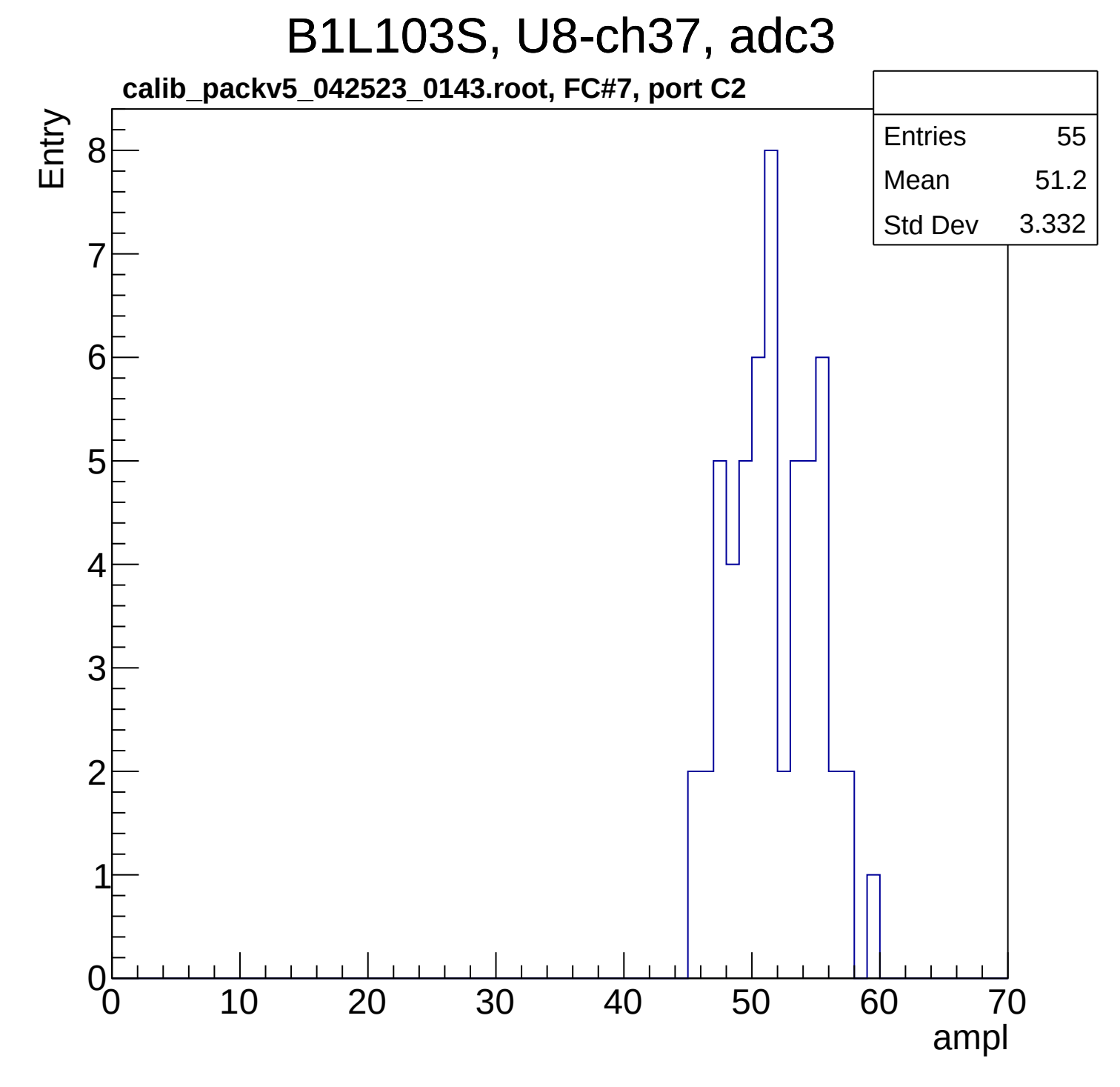

B1L103S, U8-ch36, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 10
Mean 61.5
Std Dev 1.628
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

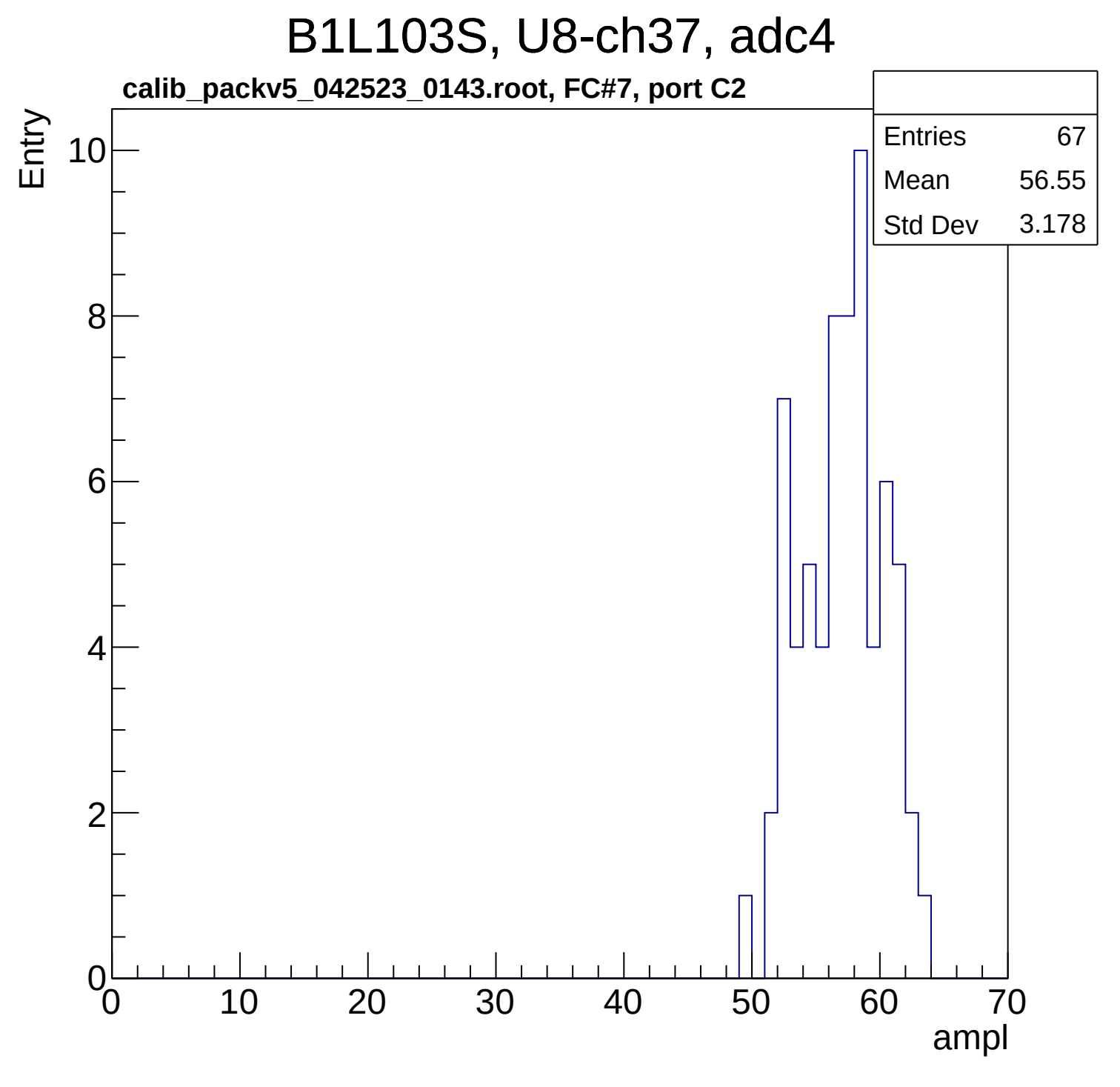

B1L103S, U8-ch36, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 24
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

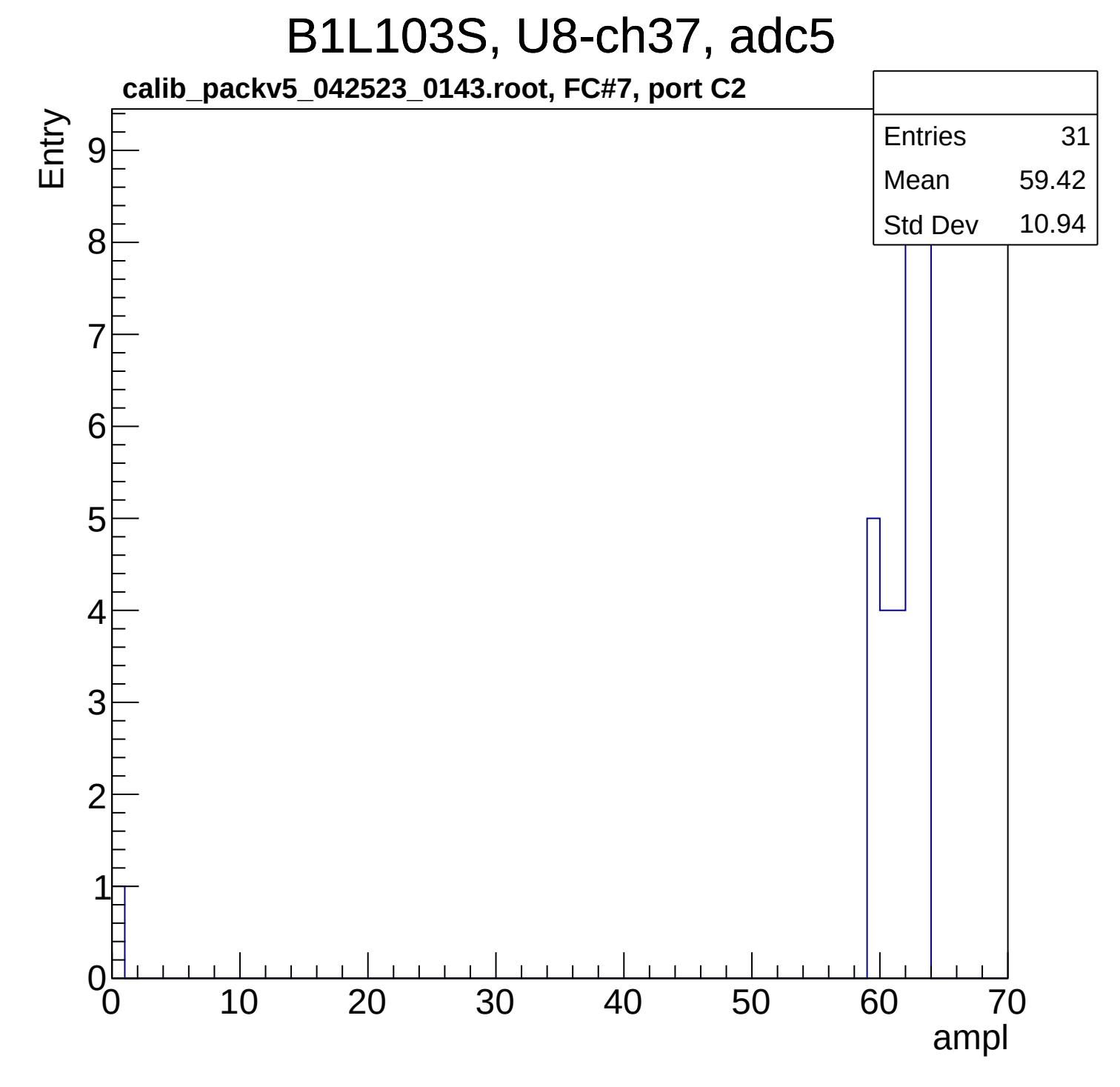

B1L103S, U8-ch37, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 89
Mean 31.81
Std Dev 3.56
Gaus mean : 31.8408
Gaus Width: 3.5930
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

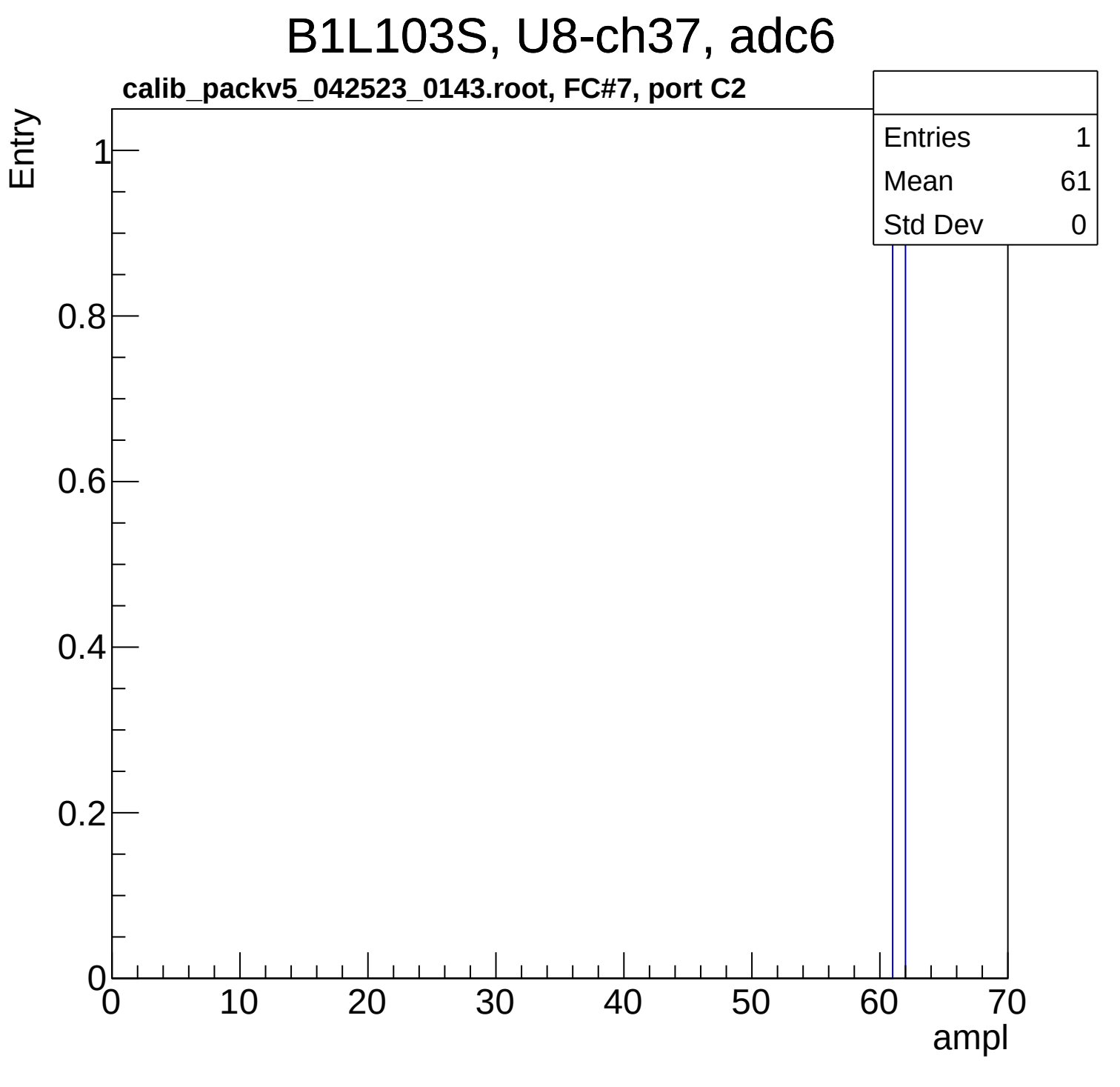

B1L103S, U8-ch37, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 39.61
Std Dev 3.074
Gaus mean : 40.3445
Gaus Width: 3.0040
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

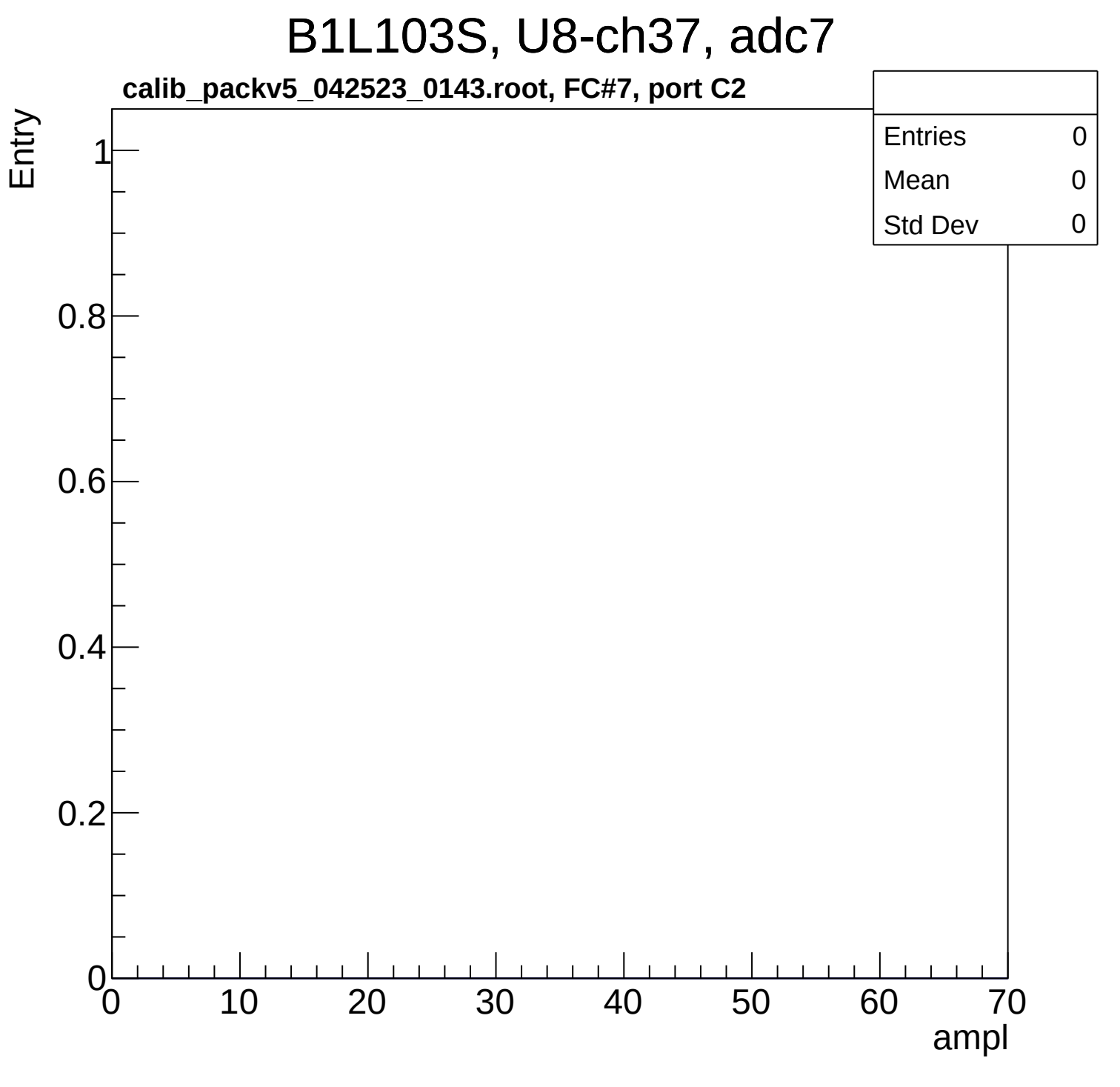

B1L103S, U8-ch37, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 45.81
Std Dev 2.974
Gaus mean : 46.3947
Gaus Width: 3.4726
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

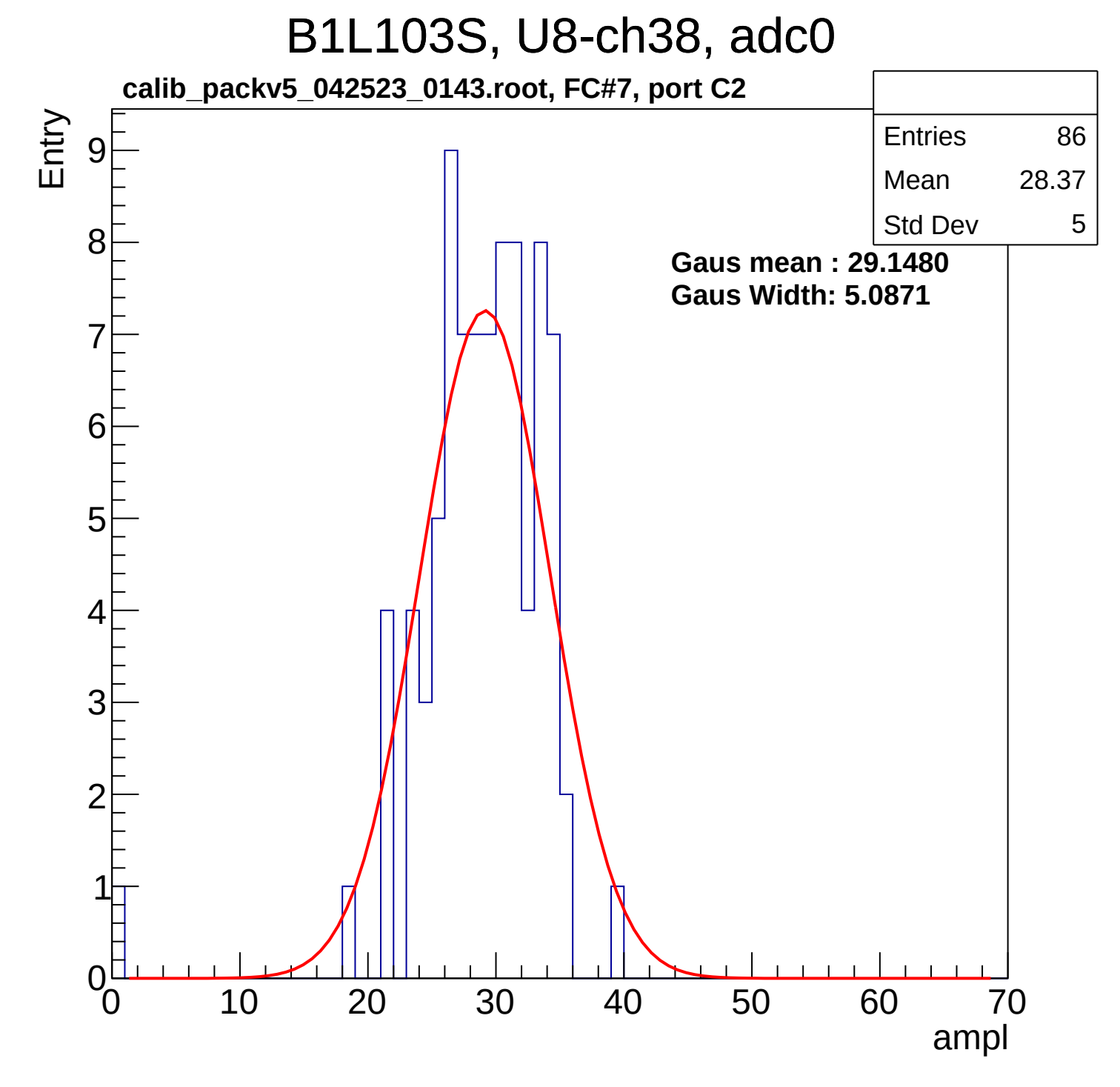

B1L103S, U8-ch37, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 51.2
Std Dev 3.332
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

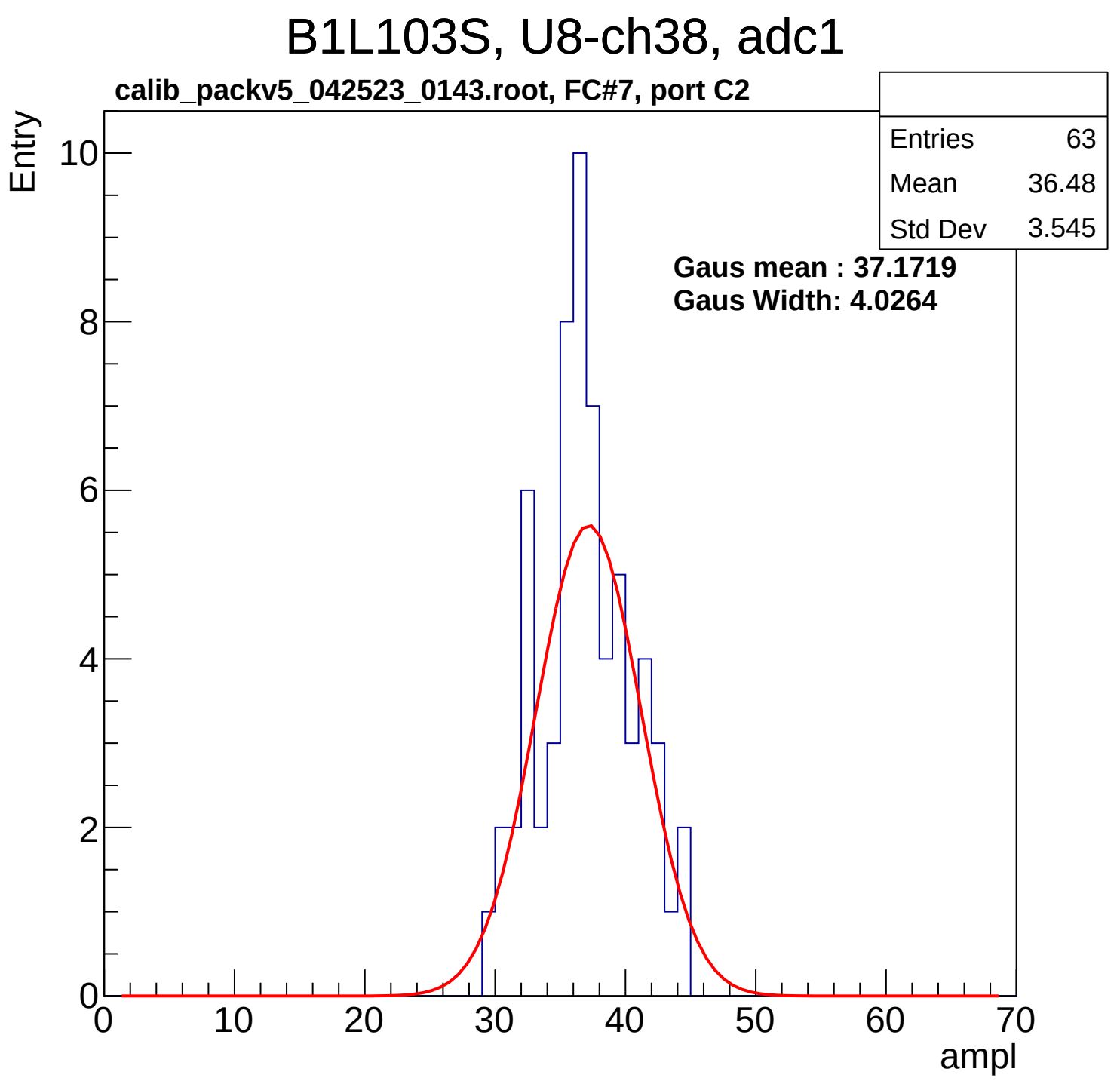

B1L103S, U8-ch37, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 56.55
Std Dev 3.178
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

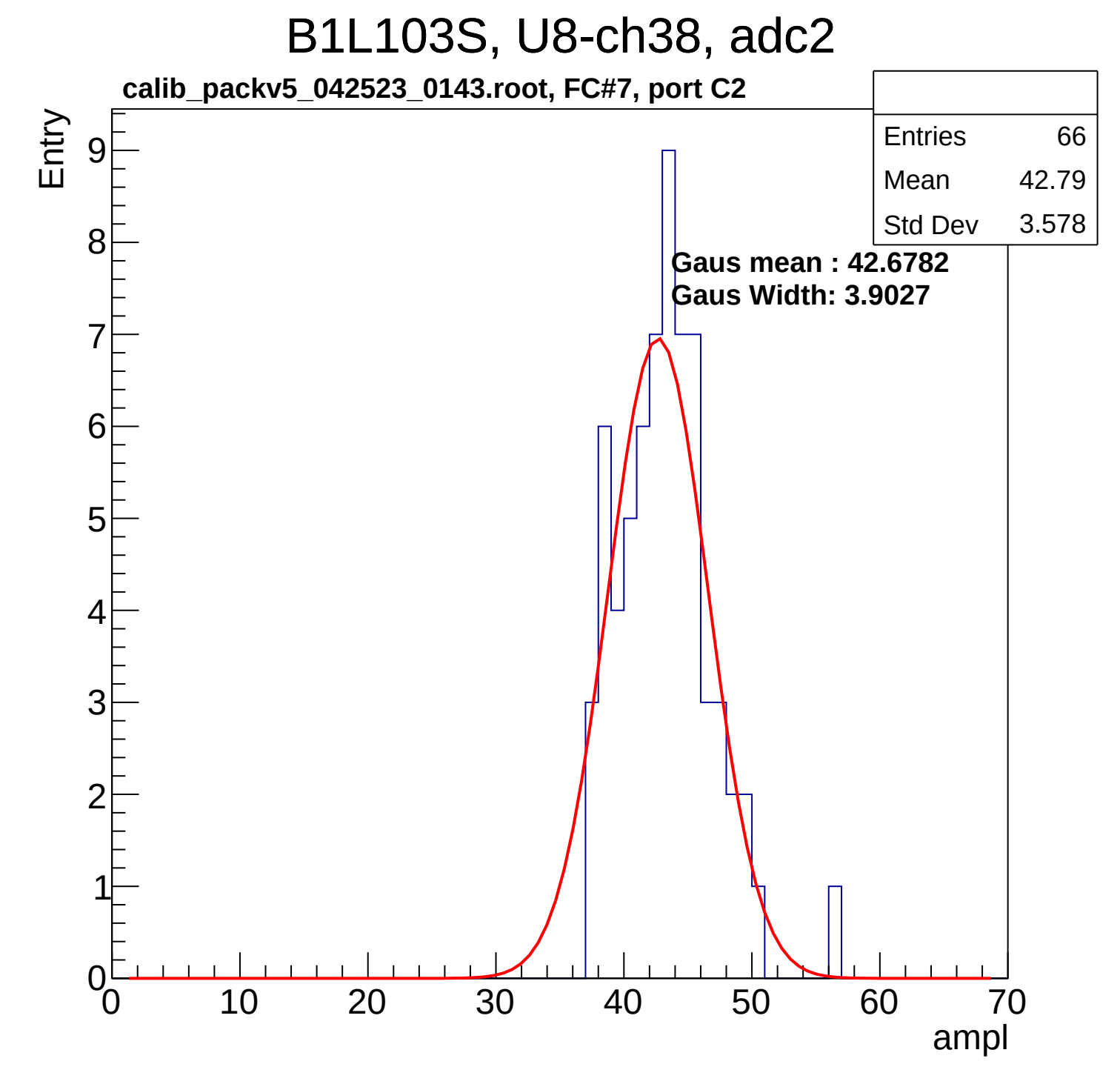

B1L103S, U8-ch37, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 31
Mean 59.42
Std Dev 10.94
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

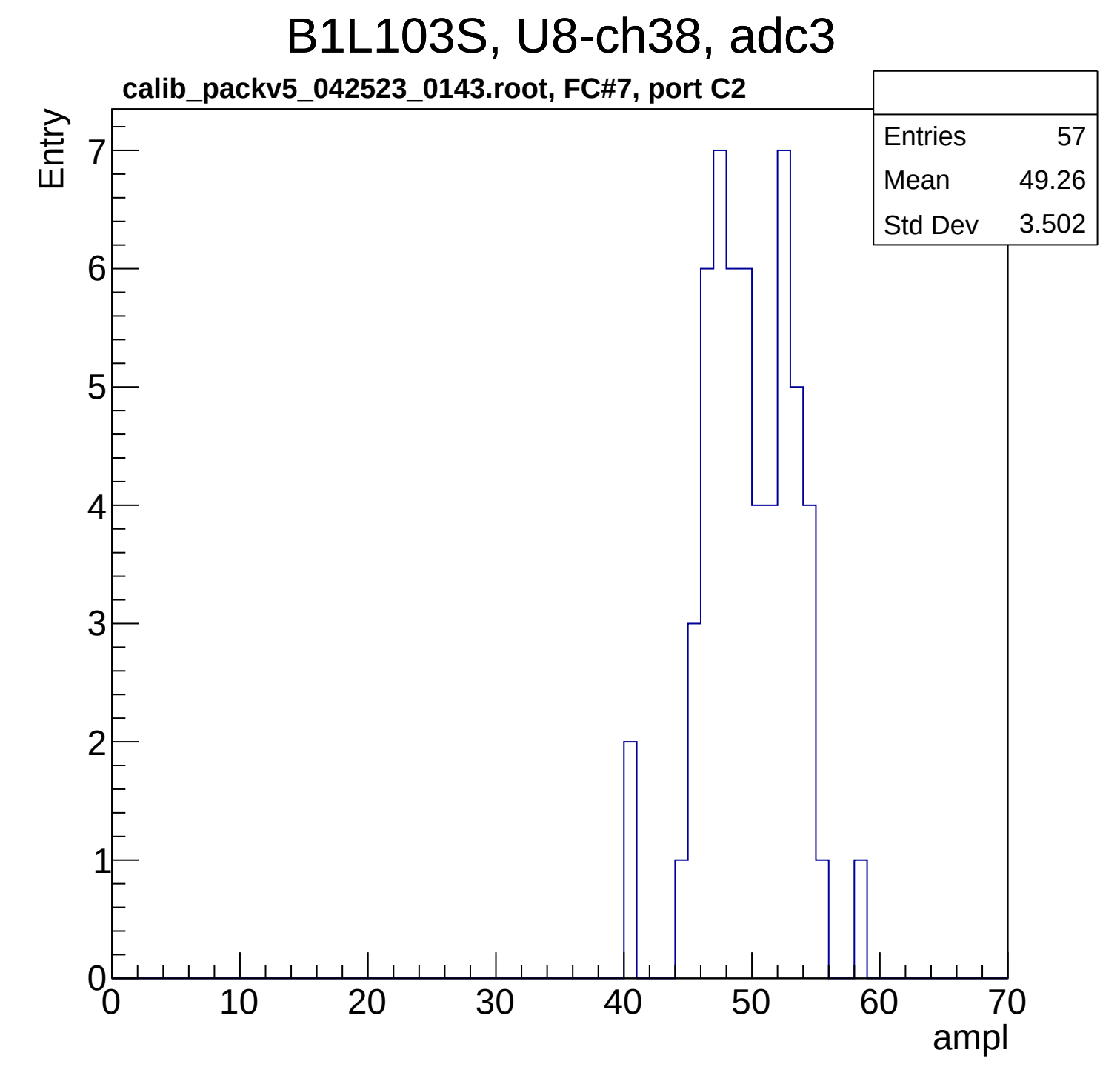

B1L103S, U8-ch37, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 61
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

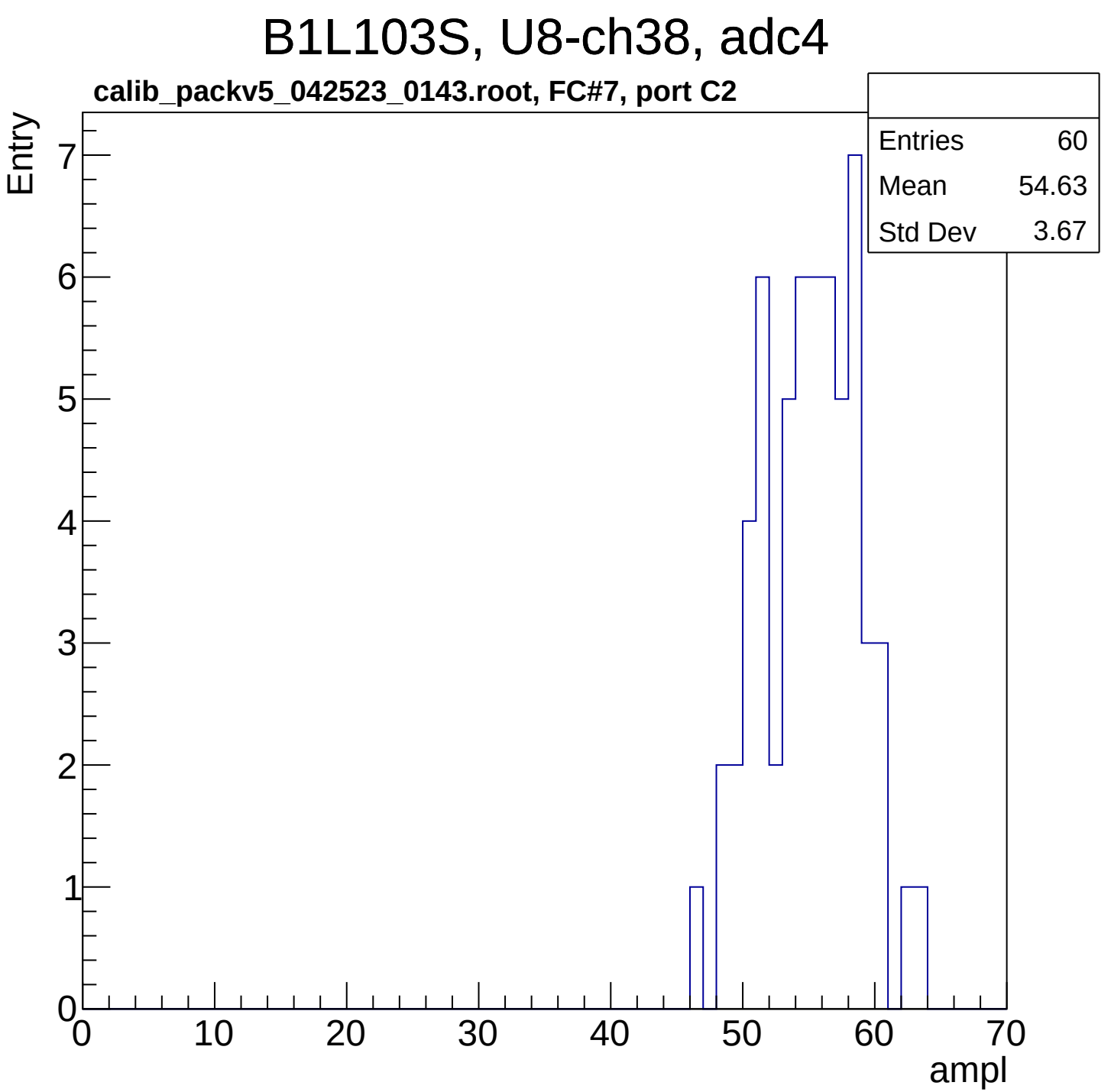

B1L103S, U8-ch37, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

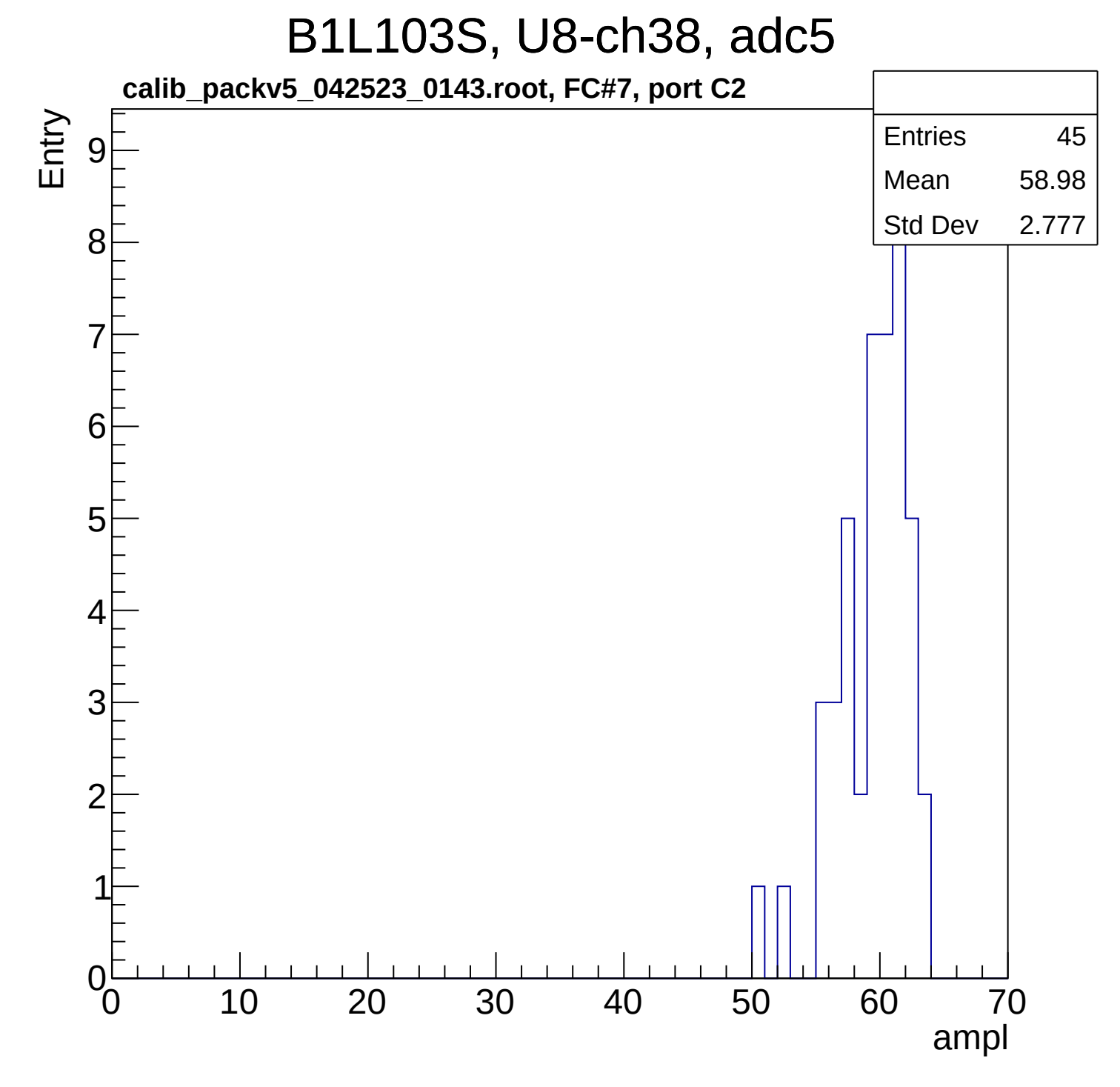

B1L103S, U8-ch38, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 86
Mean 28.37
Std Dev 5
Gaus mean : 29.1480
Gaus Width: 5.0871
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

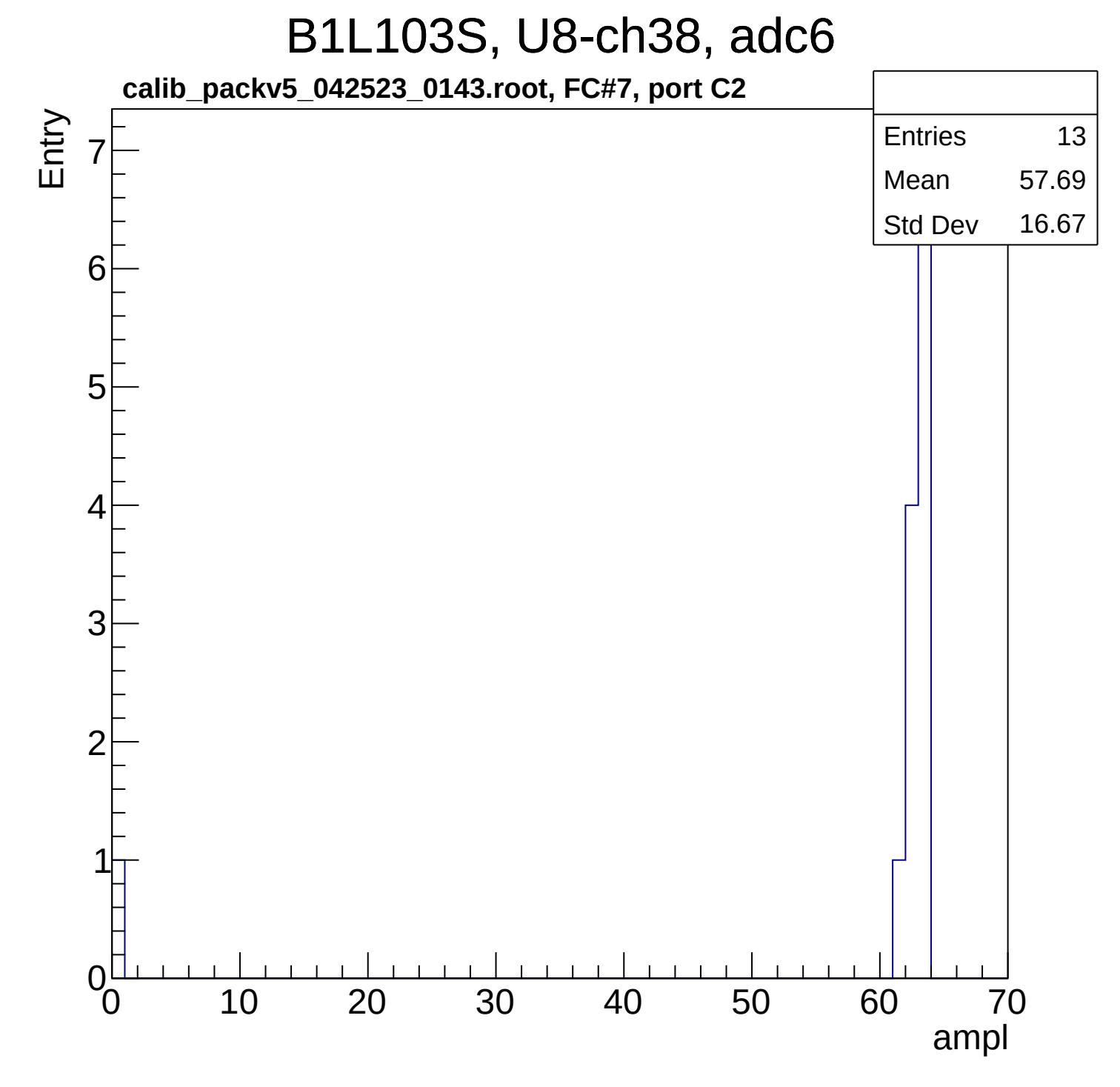

B1L103S, U8-ch38, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 36.48
Std Dev 3.545
Gaus mean : 37.1719
Gaus Width: 4.0264
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

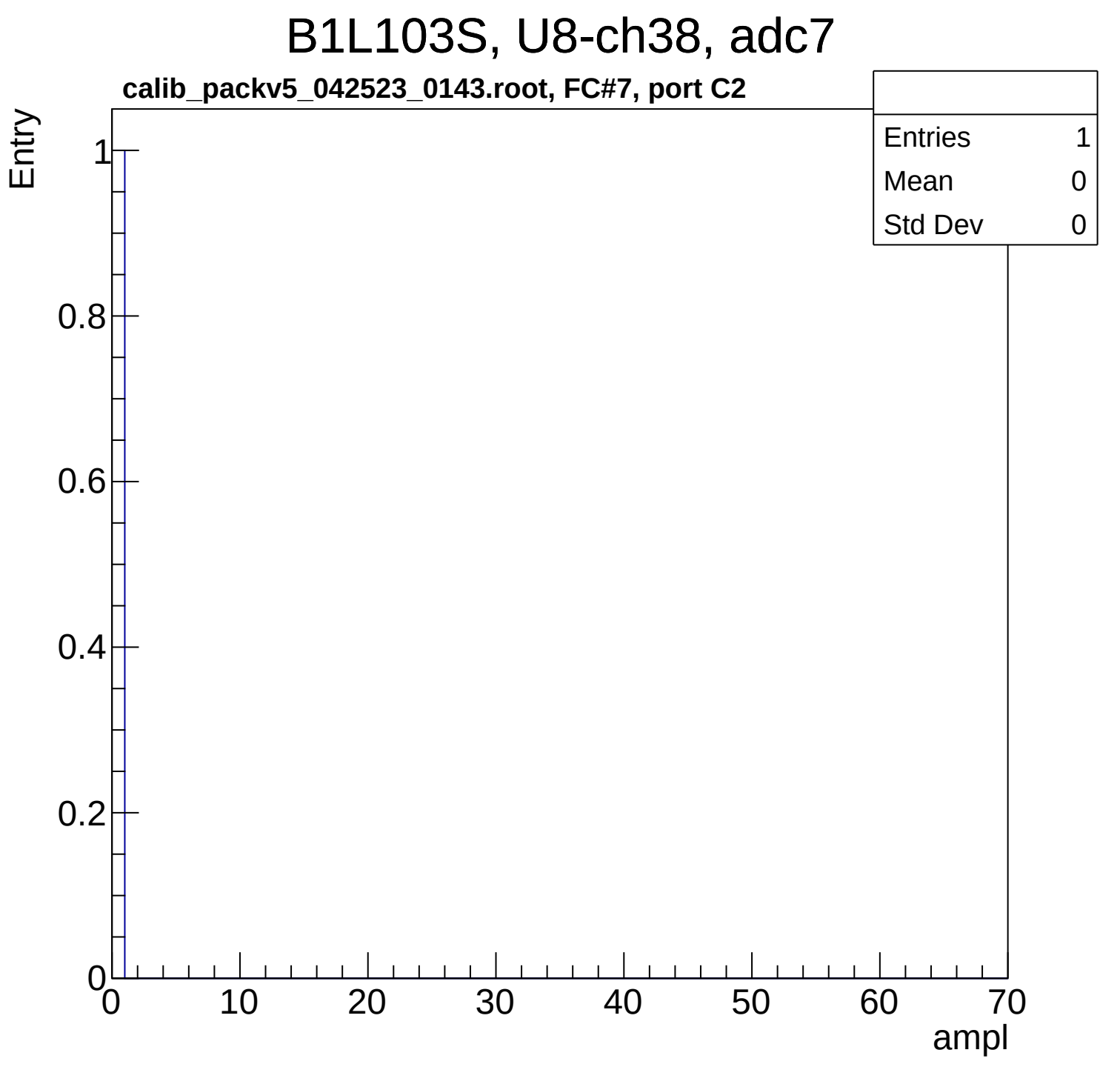

B1L103S, U8-ch38, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 42.79
Std Dev 3.578
Gaus mean : 42.6782
Gaus Width: 3.9027
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

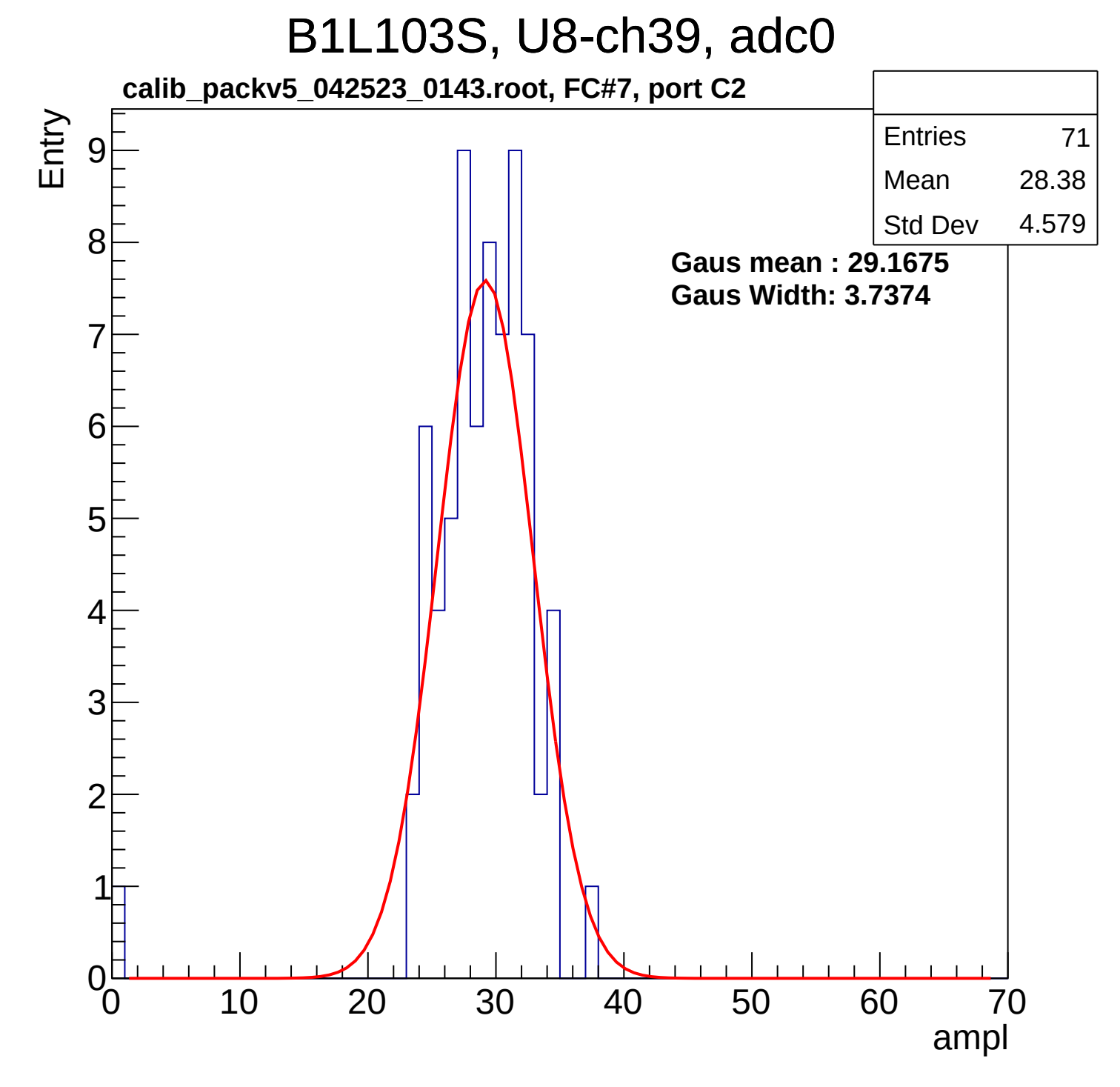

B1L103S, U8-ch38, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 49.26
Std Dev 3.502
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

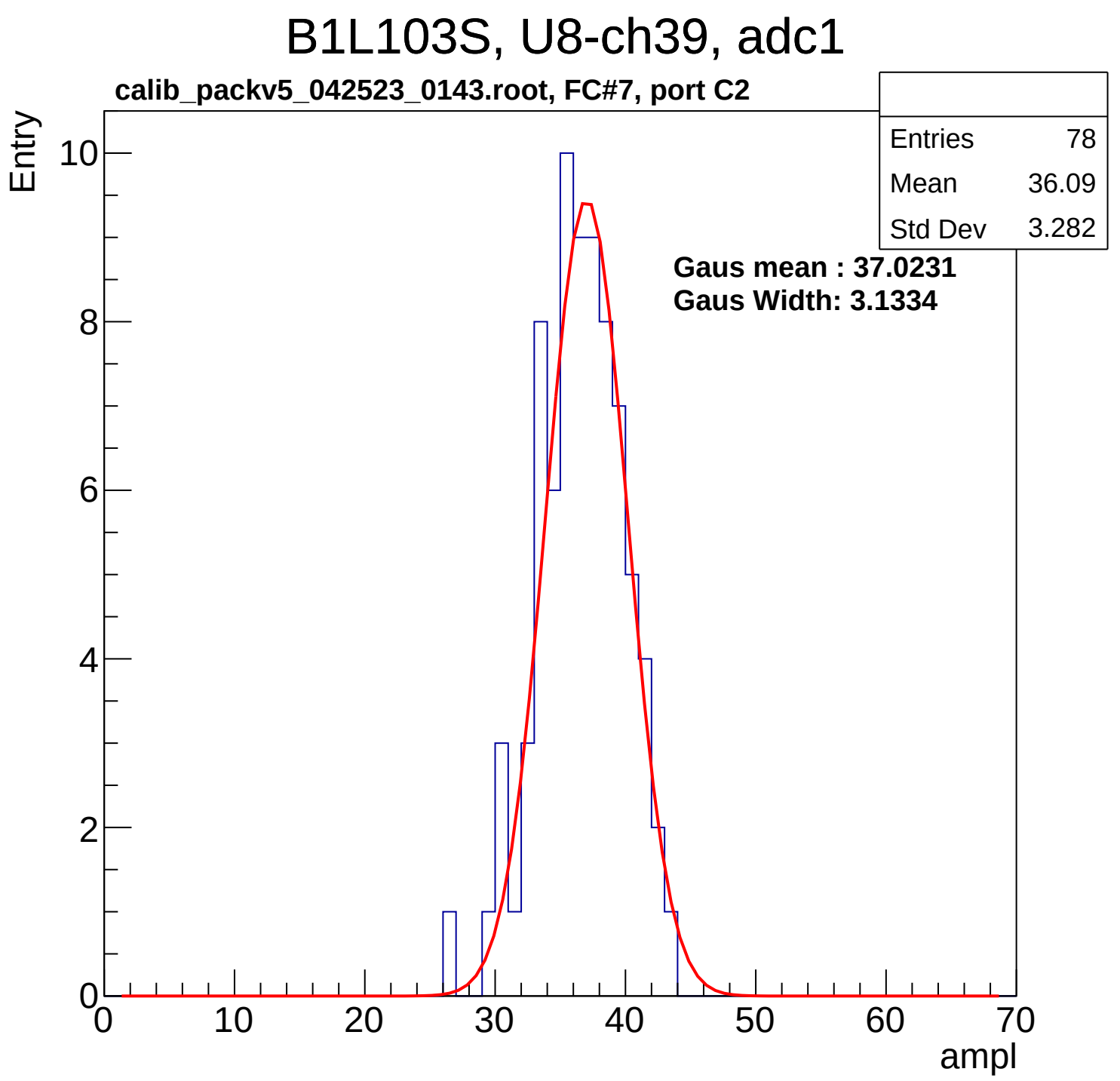

B1L103S, U8-ch38, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 54.63
Std Dev 3.67
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

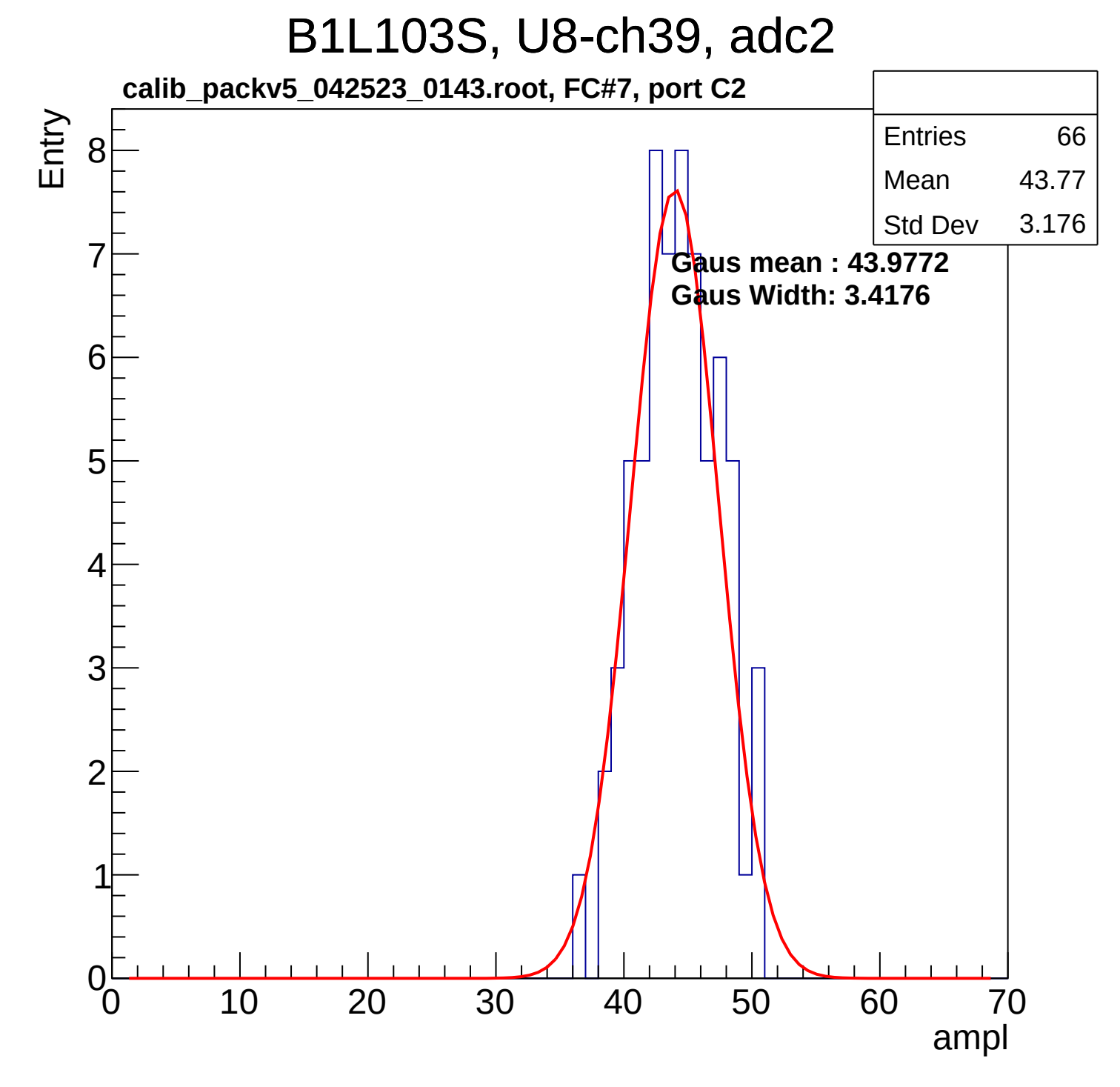

B1L103S, U8-ch38, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 45
Mean 58.98
Std Dev 2.777
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

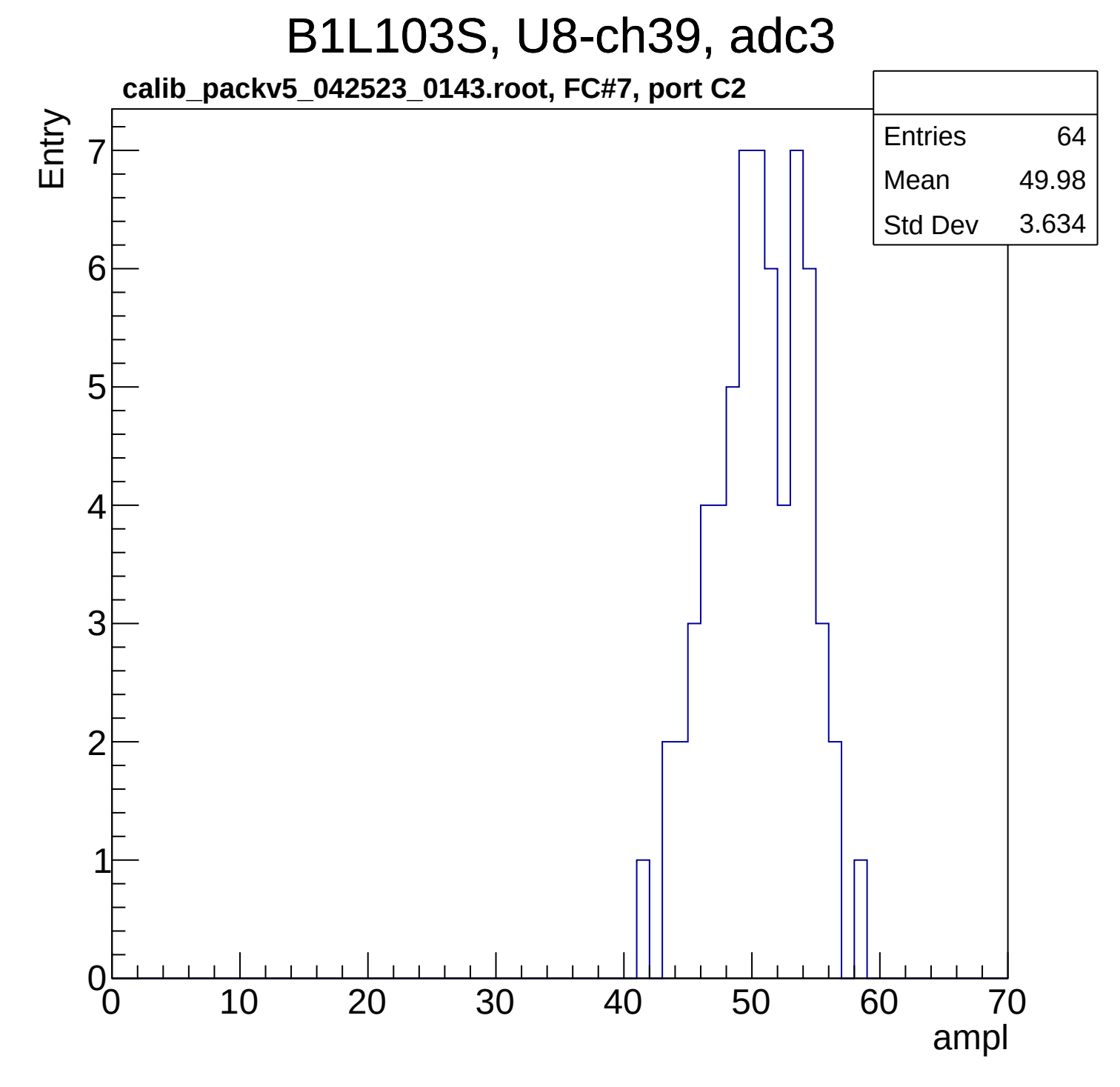

B1L103S, U8-ch38, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 13
Mean 57.69
Std Dev 16.67
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

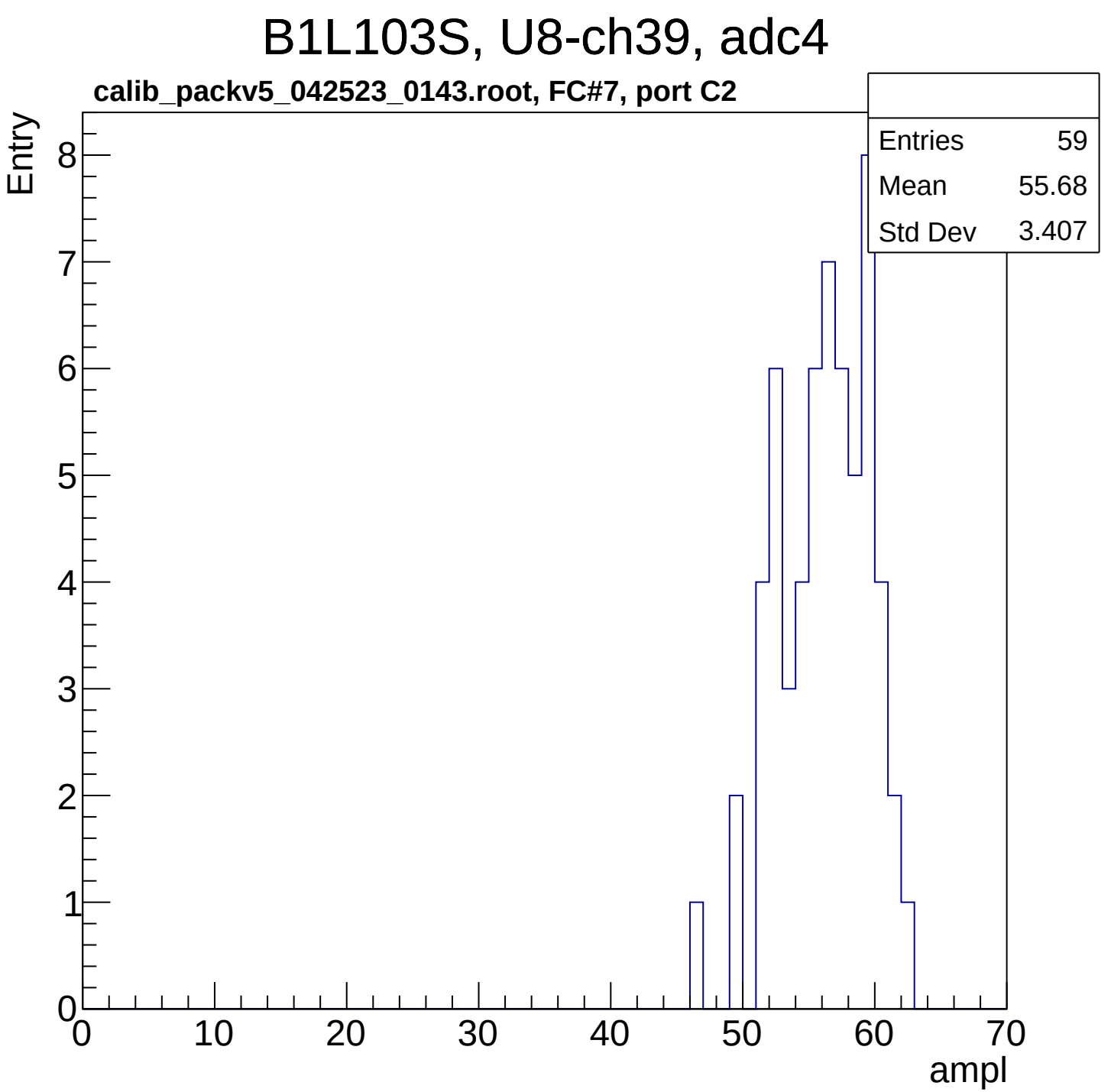

B1L103S, U8-ch38, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

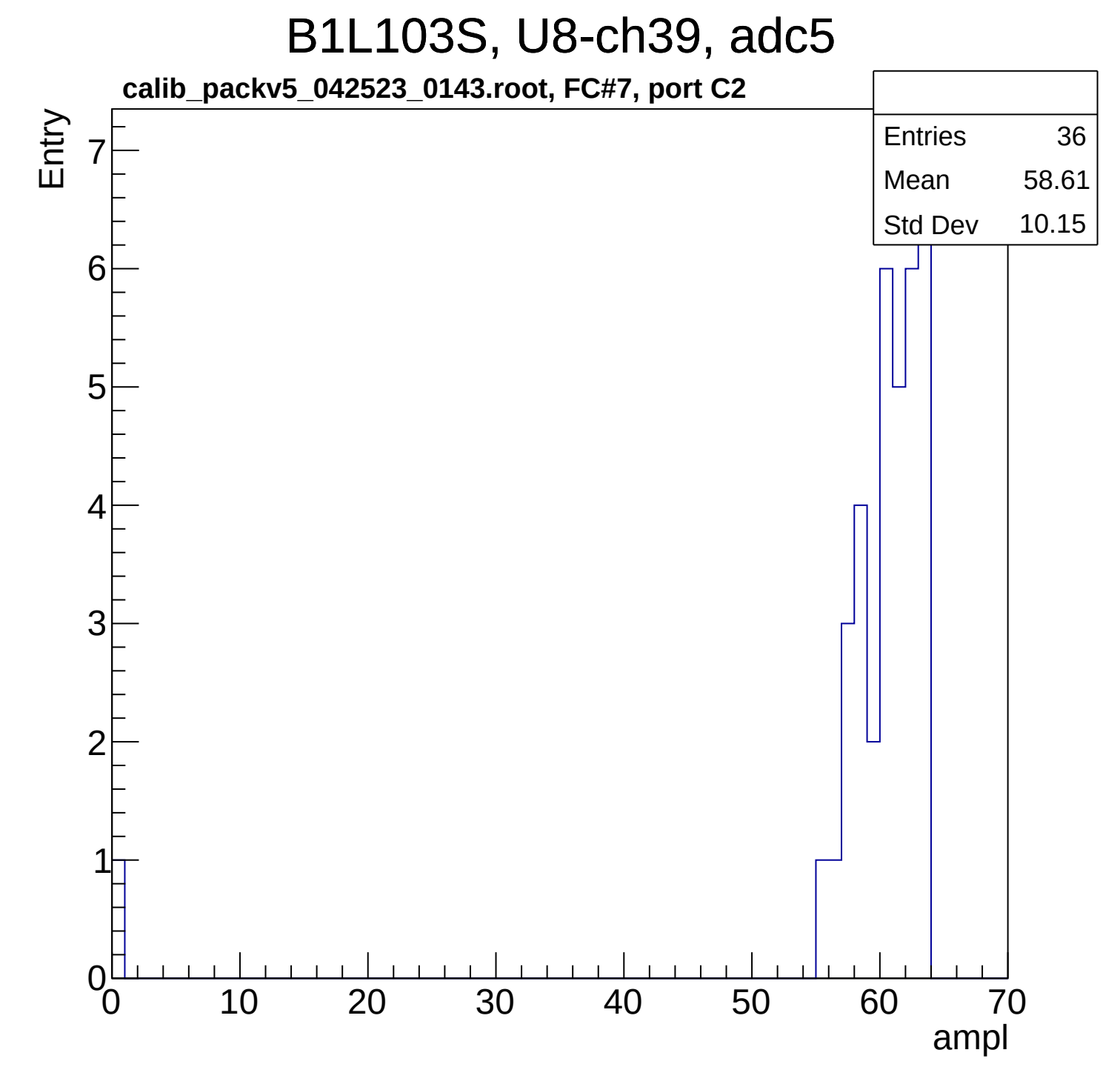

B1L103S, U8-ch39, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 28.38
Std Dev 4.579
Gaus mean : 29.1675
Gaus Width: 3.7374
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

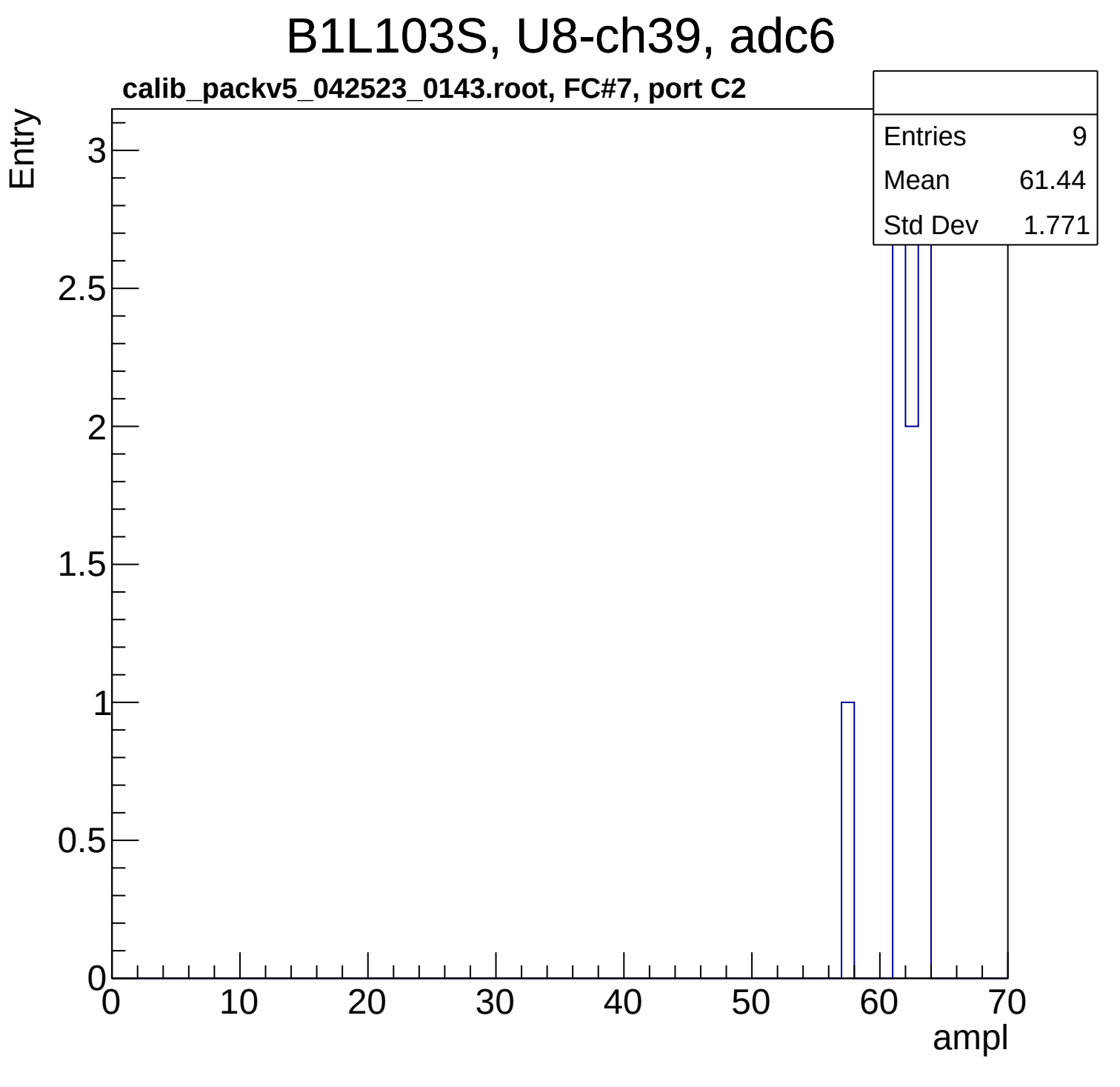

B1L103S, U8-ch39, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 36.09
Std Dev 3.282
Gaus mean : 37.0231
Gaus Width: 3.1334
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

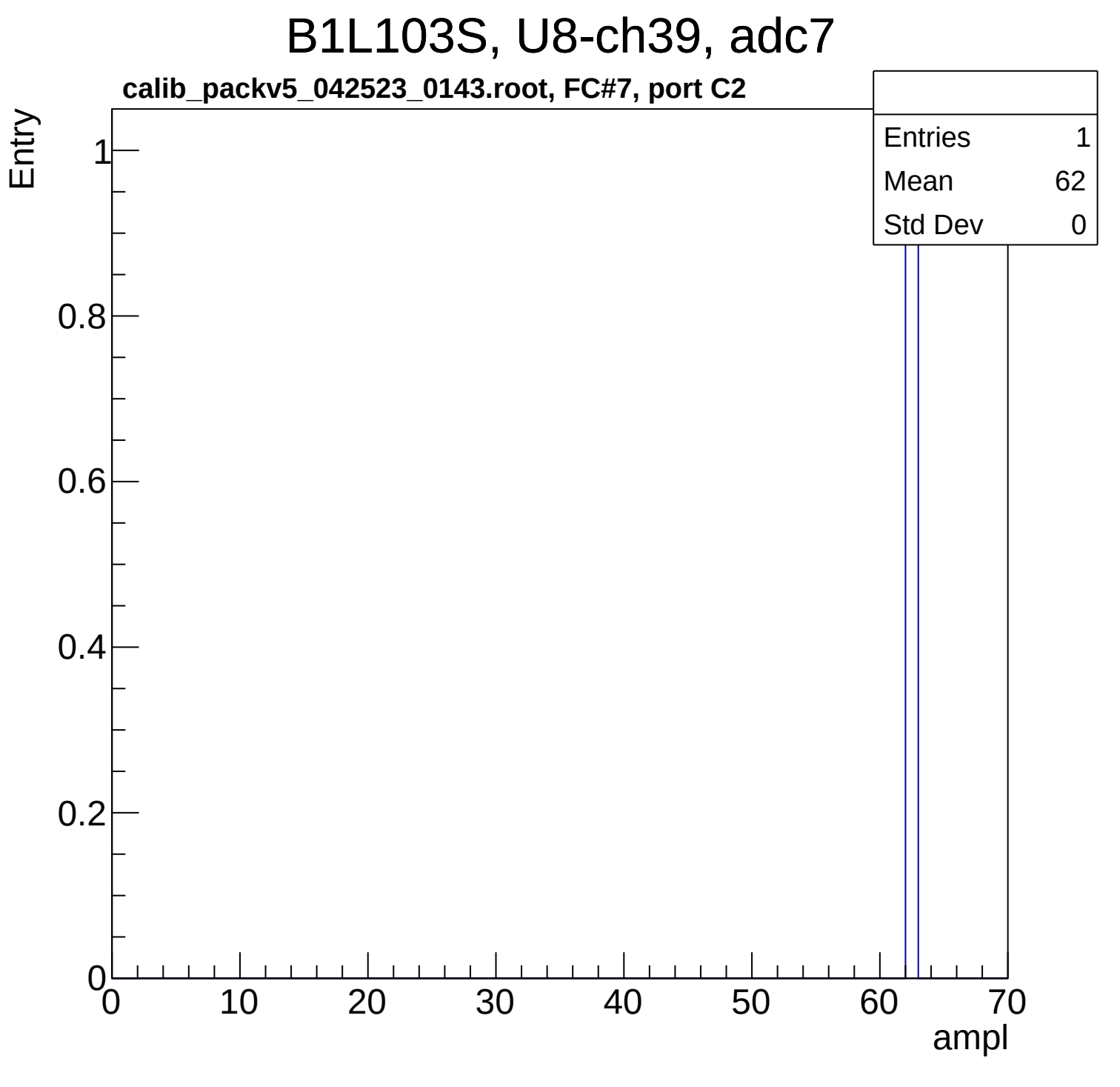

B1L103S, U8-ch39, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 43.77
Std Dev 3.176
Gaus mean : 43.9772
Gaus Width: 3.4176
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

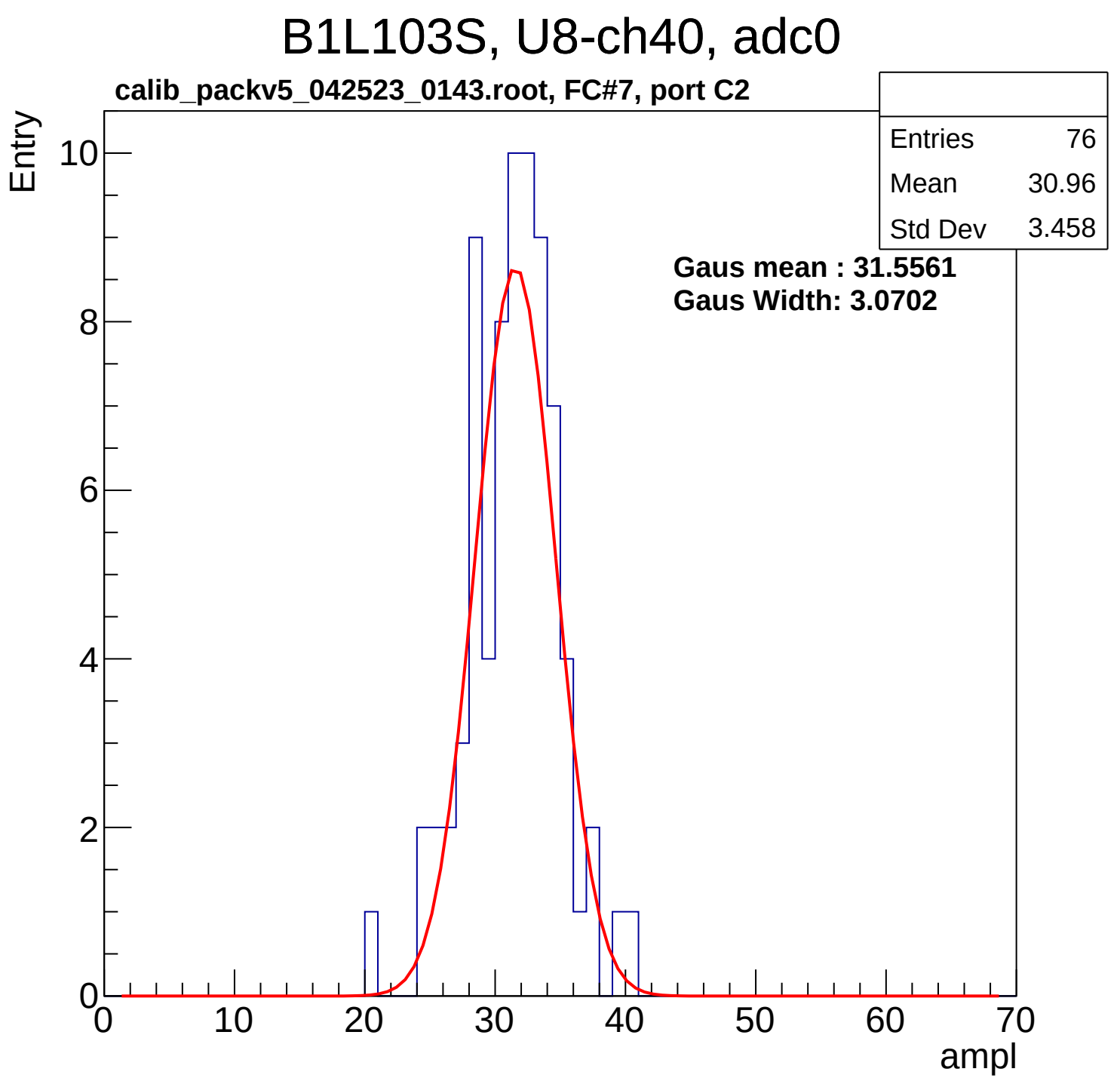

B1L103S, U8-ch39, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 49.98
Std Dev 3.634
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

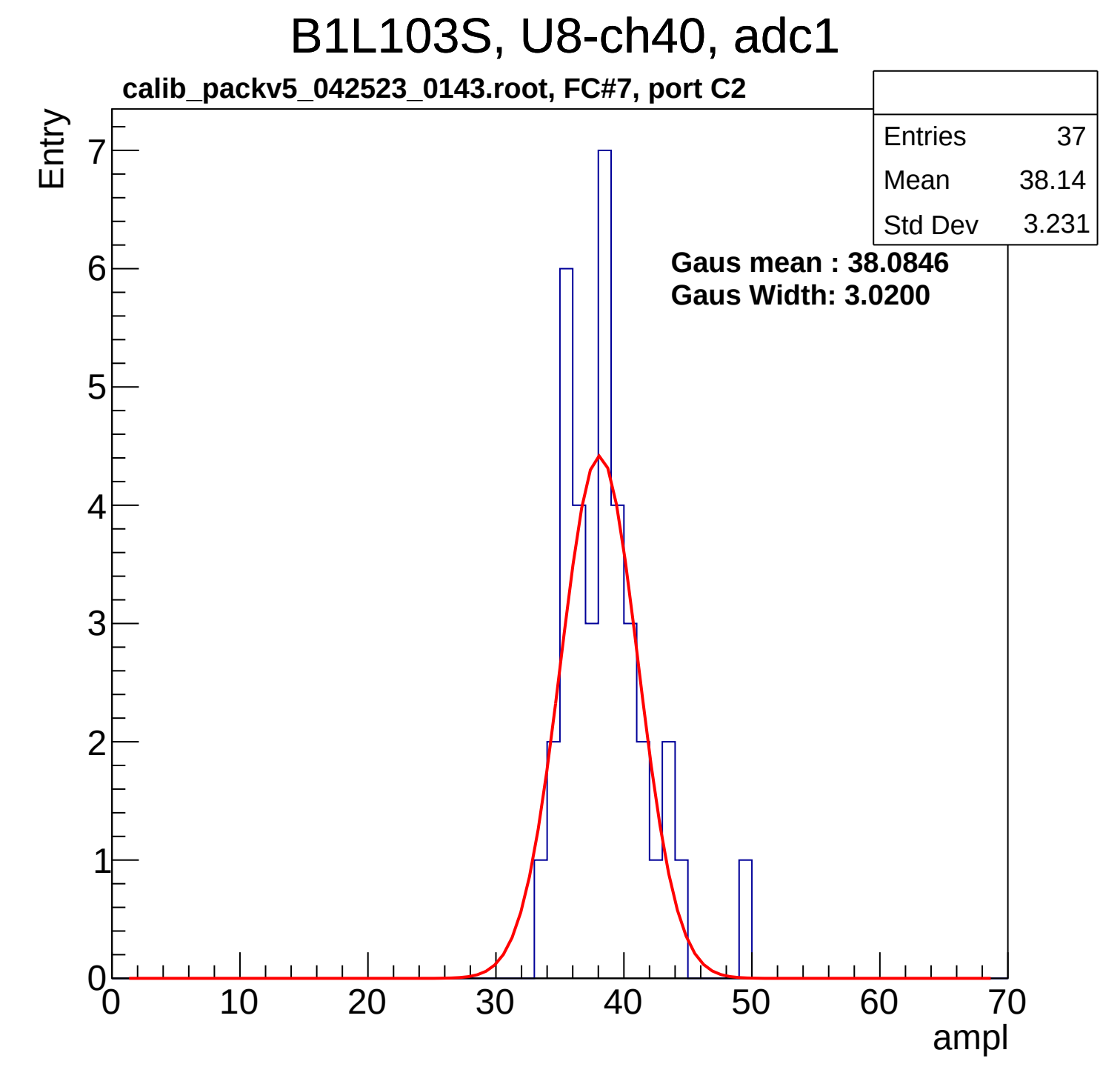

B1L103S, U8-ch39, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 55.68
Std Dev 3.407
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

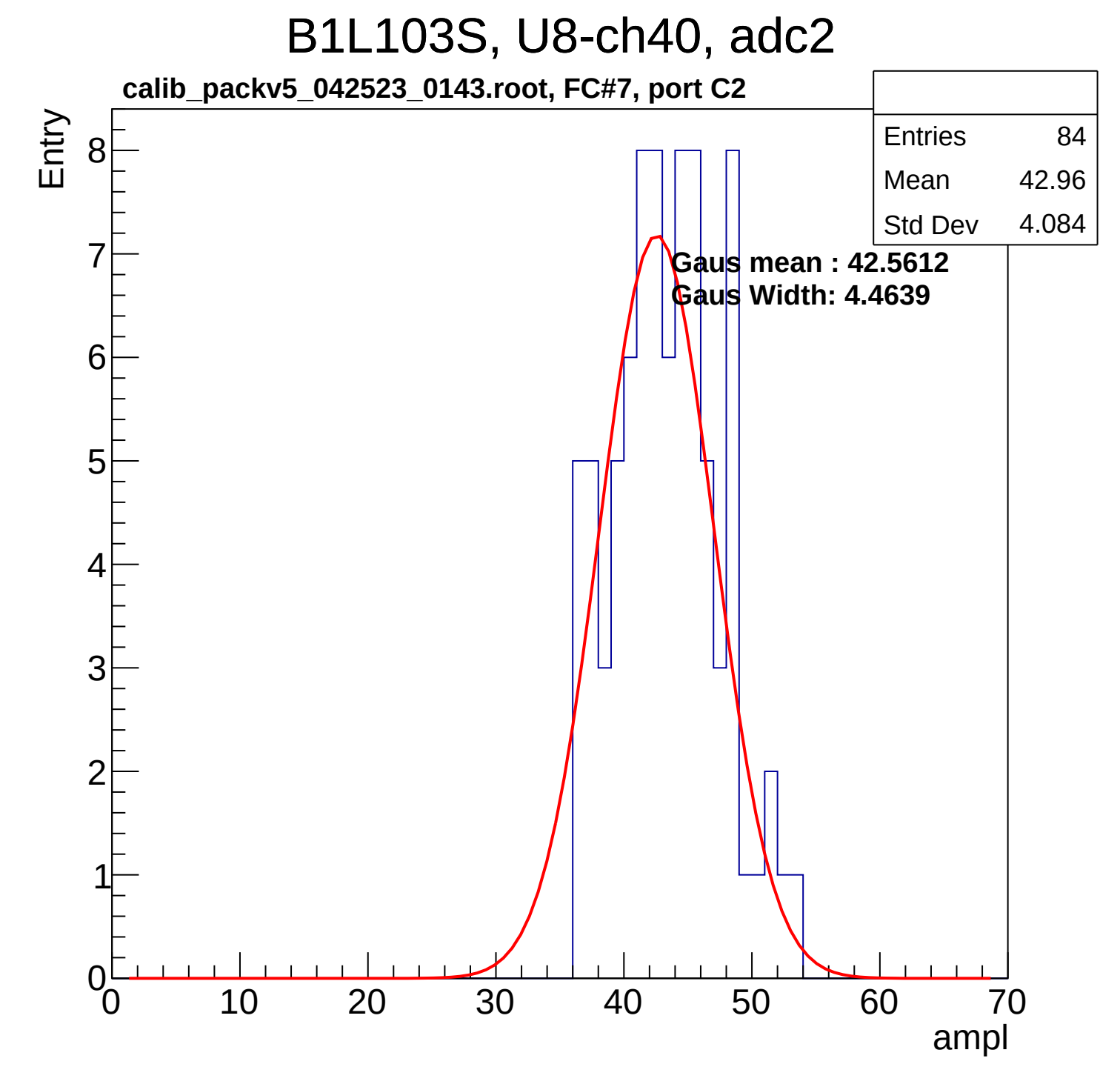

B1L103S, U8-ch39, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 36
Mean 58.61
Std Dev 10.15
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

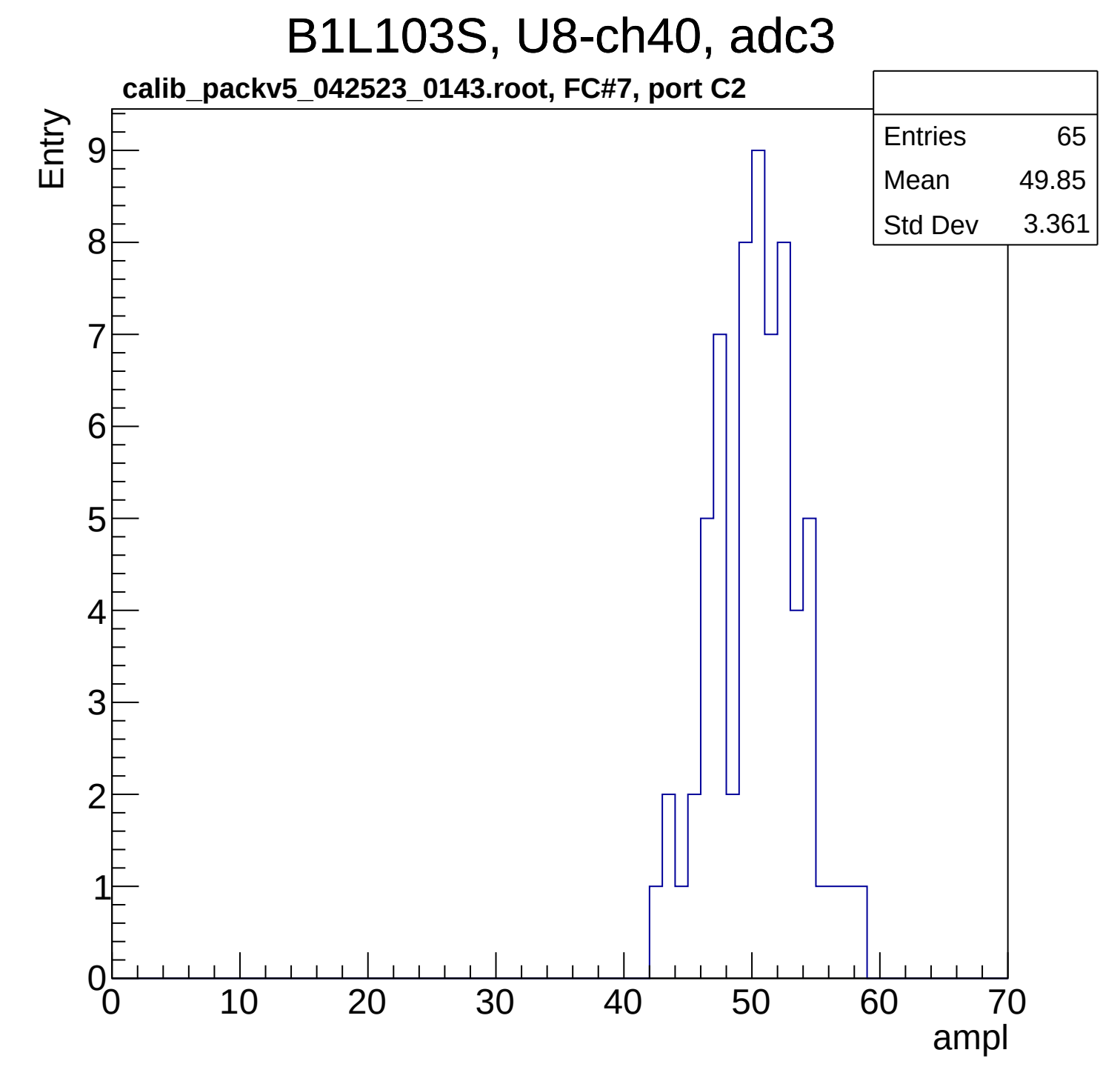

B1L103S, U8-ch39, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 9
Mean 61.44
Std Dev 1.771
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

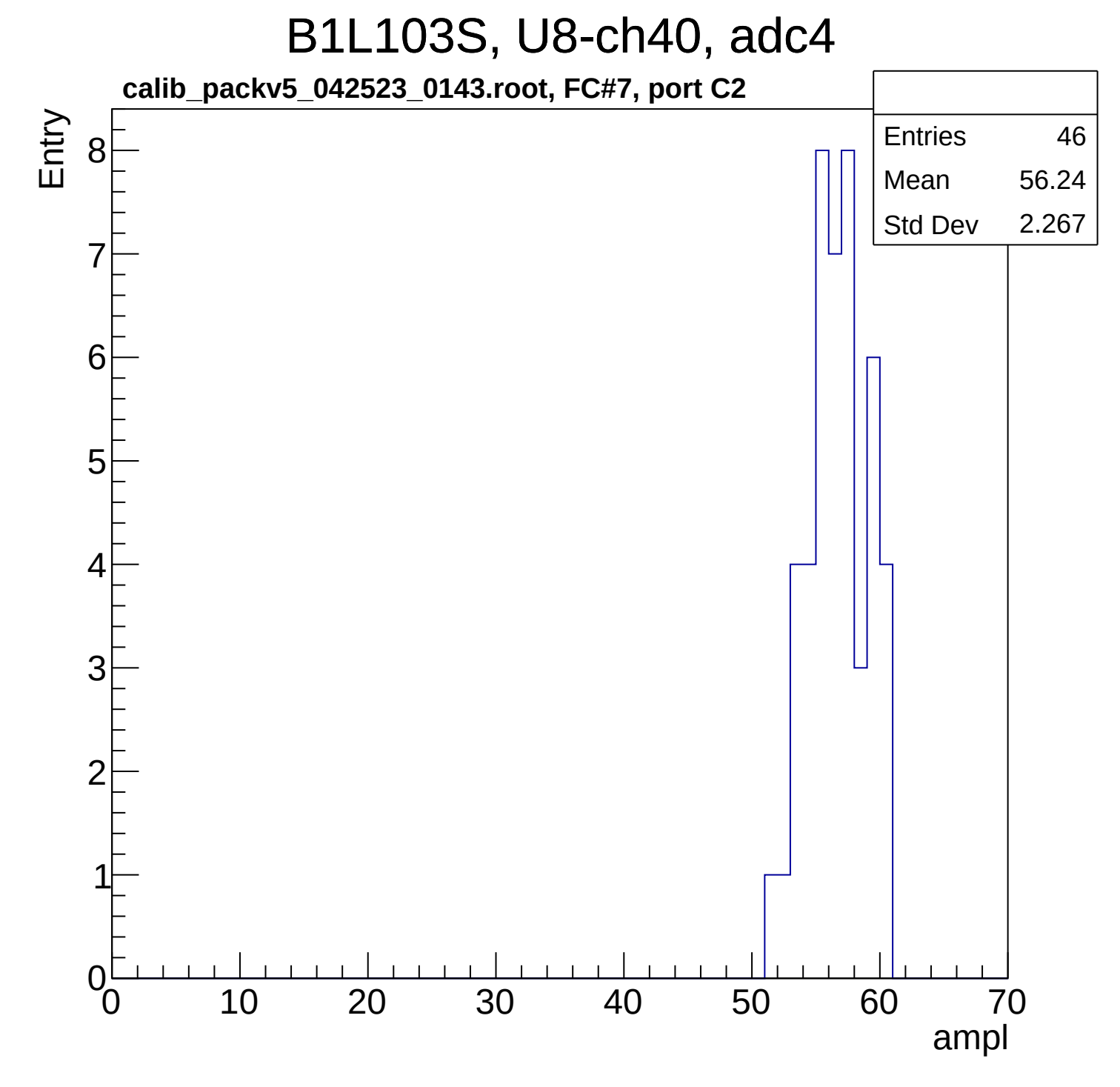

B1L103S, U8-ch39, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

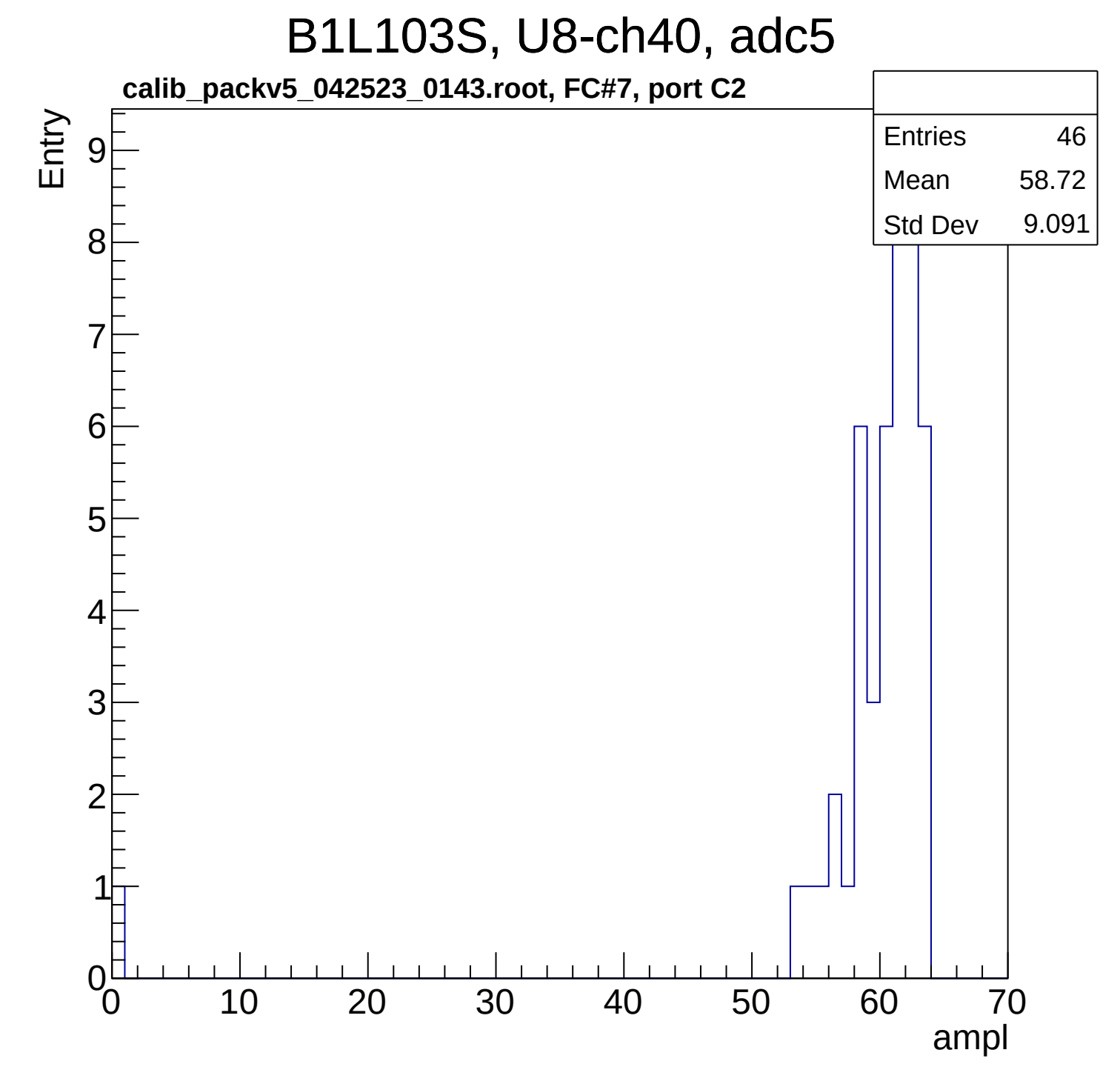

B1L103S, U8-ch40, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 76
Mean 30.96
Std Dev 3.458
Gaus mean : 31.5561
Gaus Width: 3.0702
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

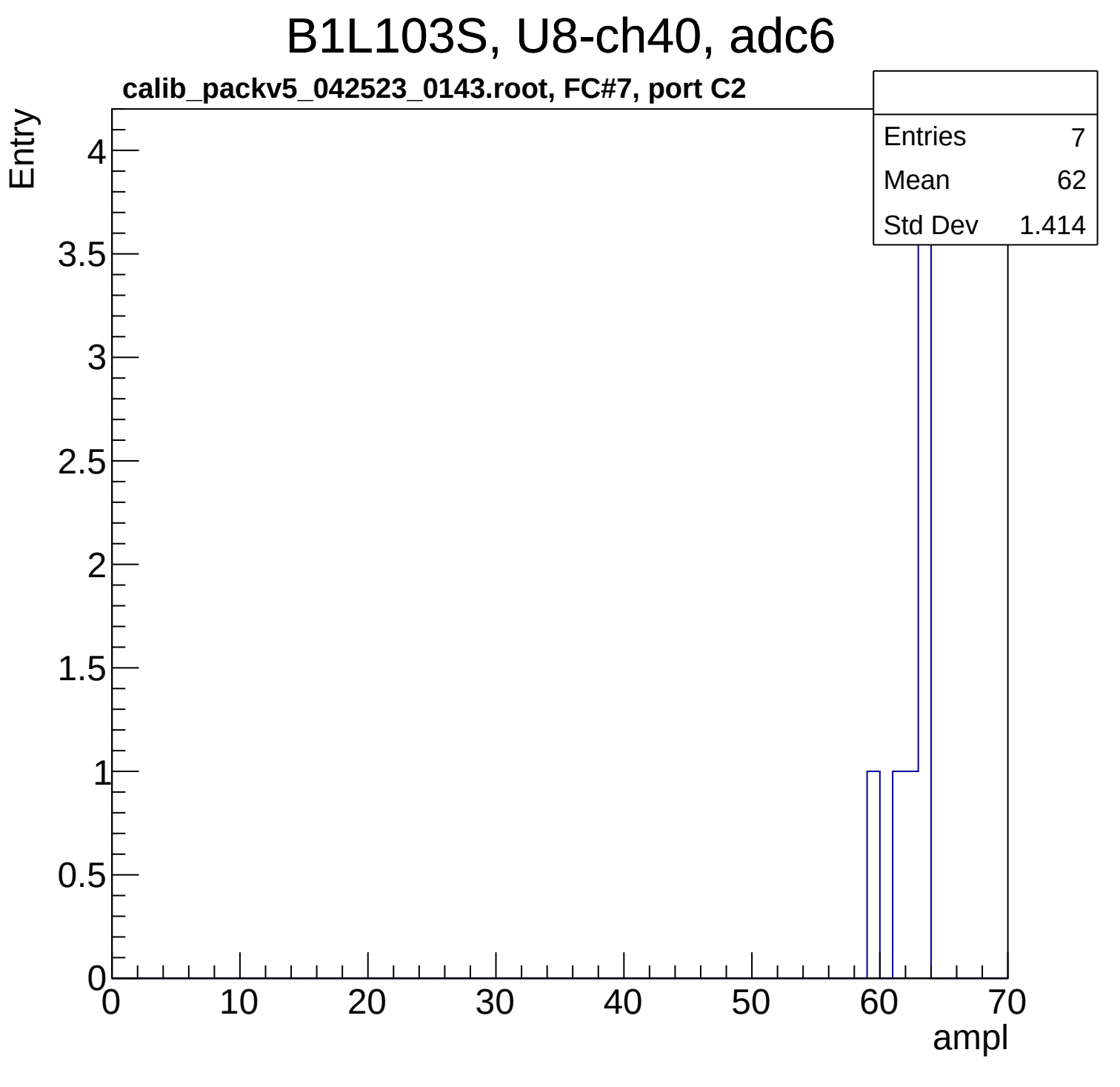

B1L103S, U8-ch40, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 37
Mean 38.14
Std Dev 3.231
Gaus mean : 38.0846
Gaus Width: 3.0200
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

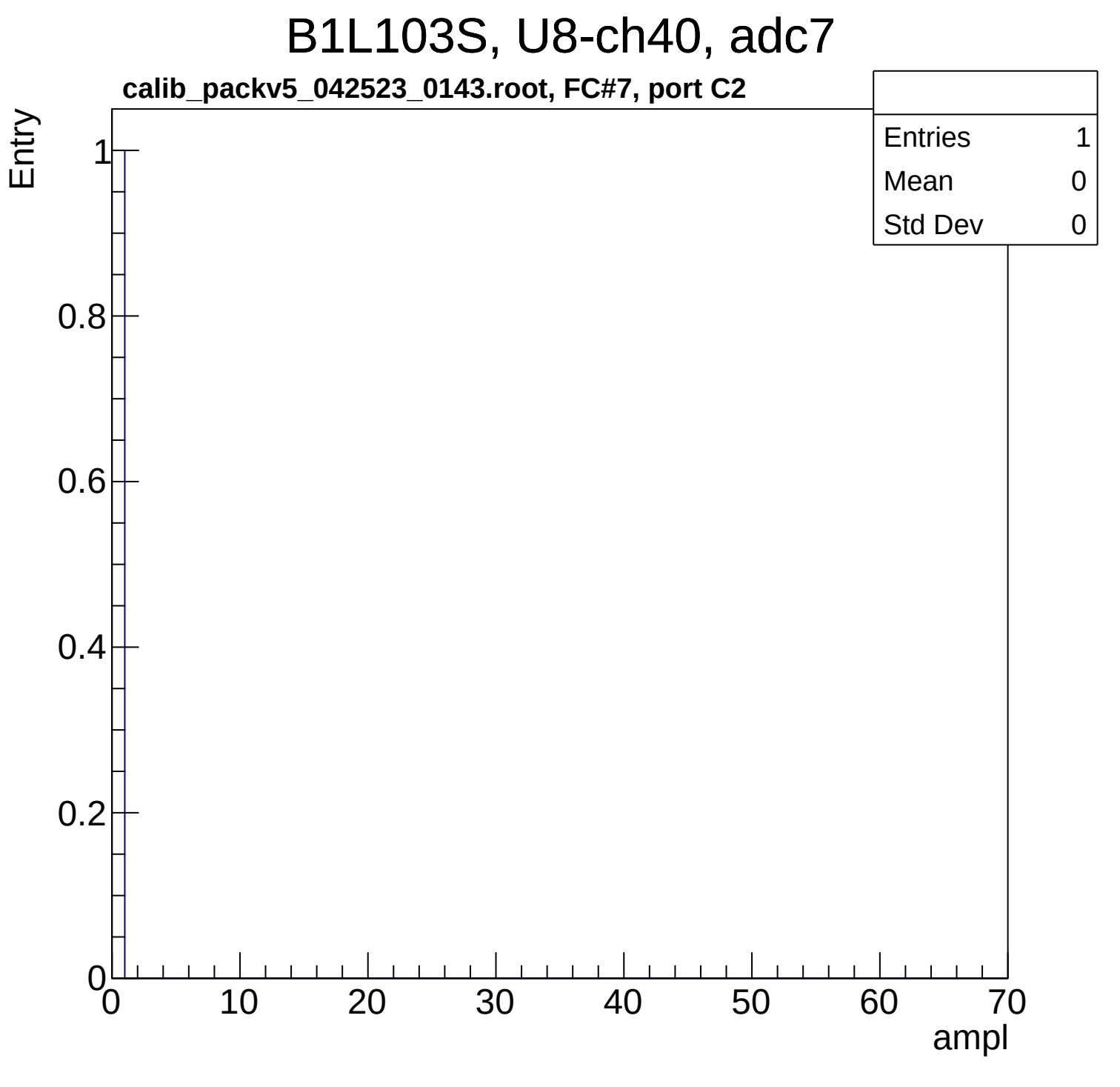

B1L103S, U8-ch40, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 84
Mean 42.96
Std Dev 4.084
Gaus mean : 42.5612
Gaus Width: 4.4639
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

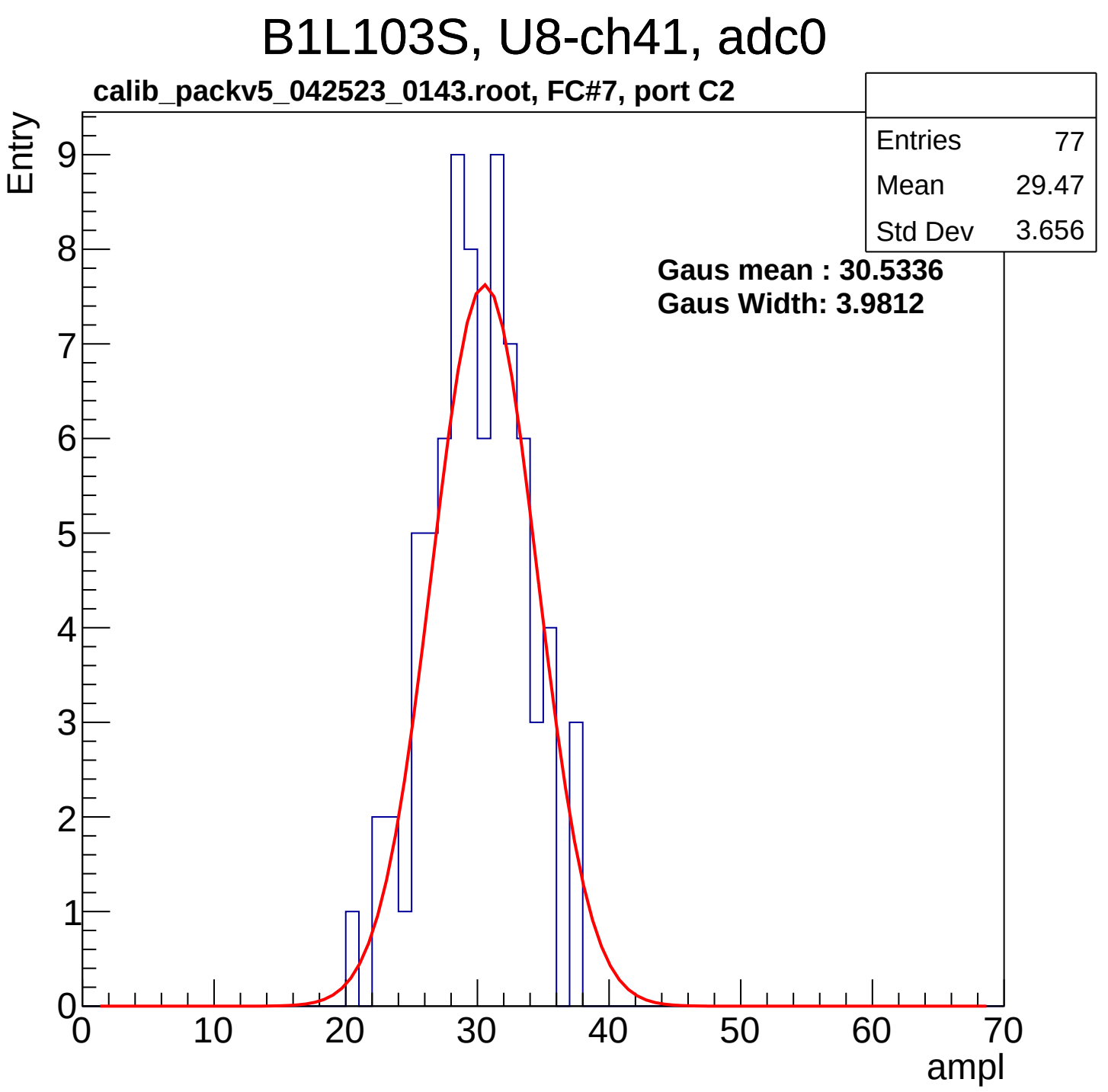

B1L103S, U8-ch40, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 49.85
Std Dev 3.361
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

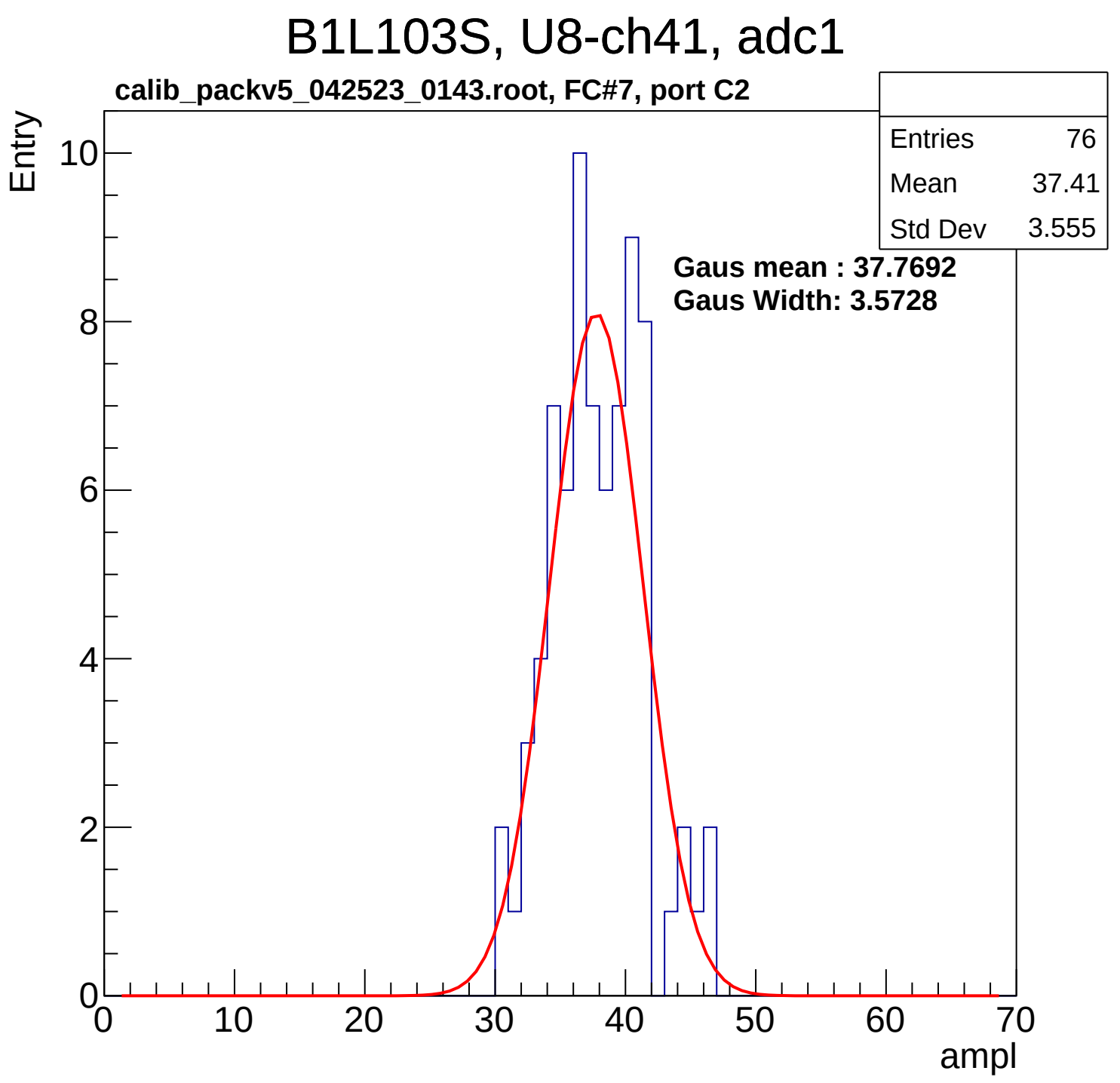

B1L103S, U8-ch40, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 46
Mean 56.24
Std Dev 2.267
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

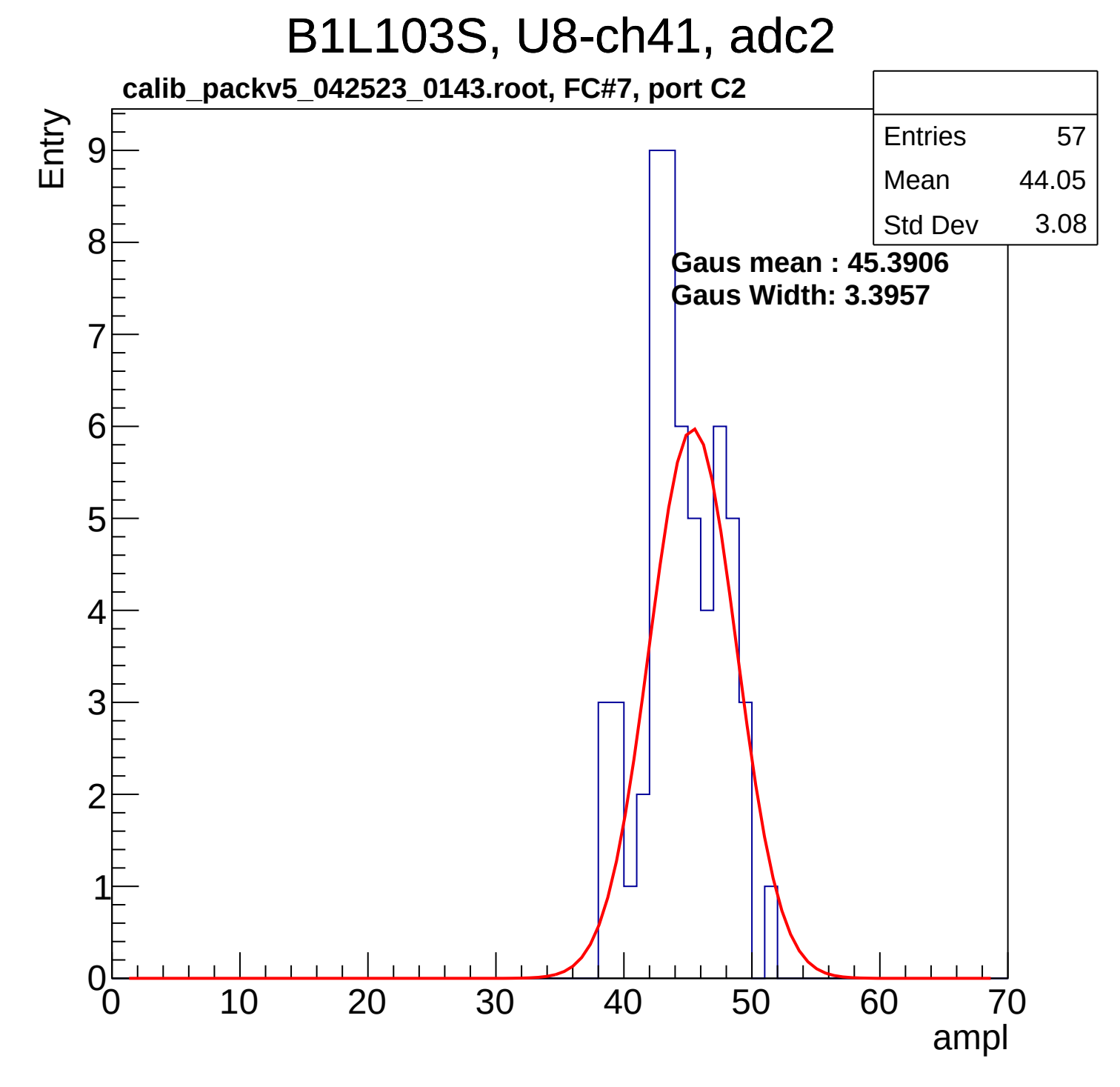

B1L103S, U8-ch40, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 46
Mean 58.72
Std Dev 9.091
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

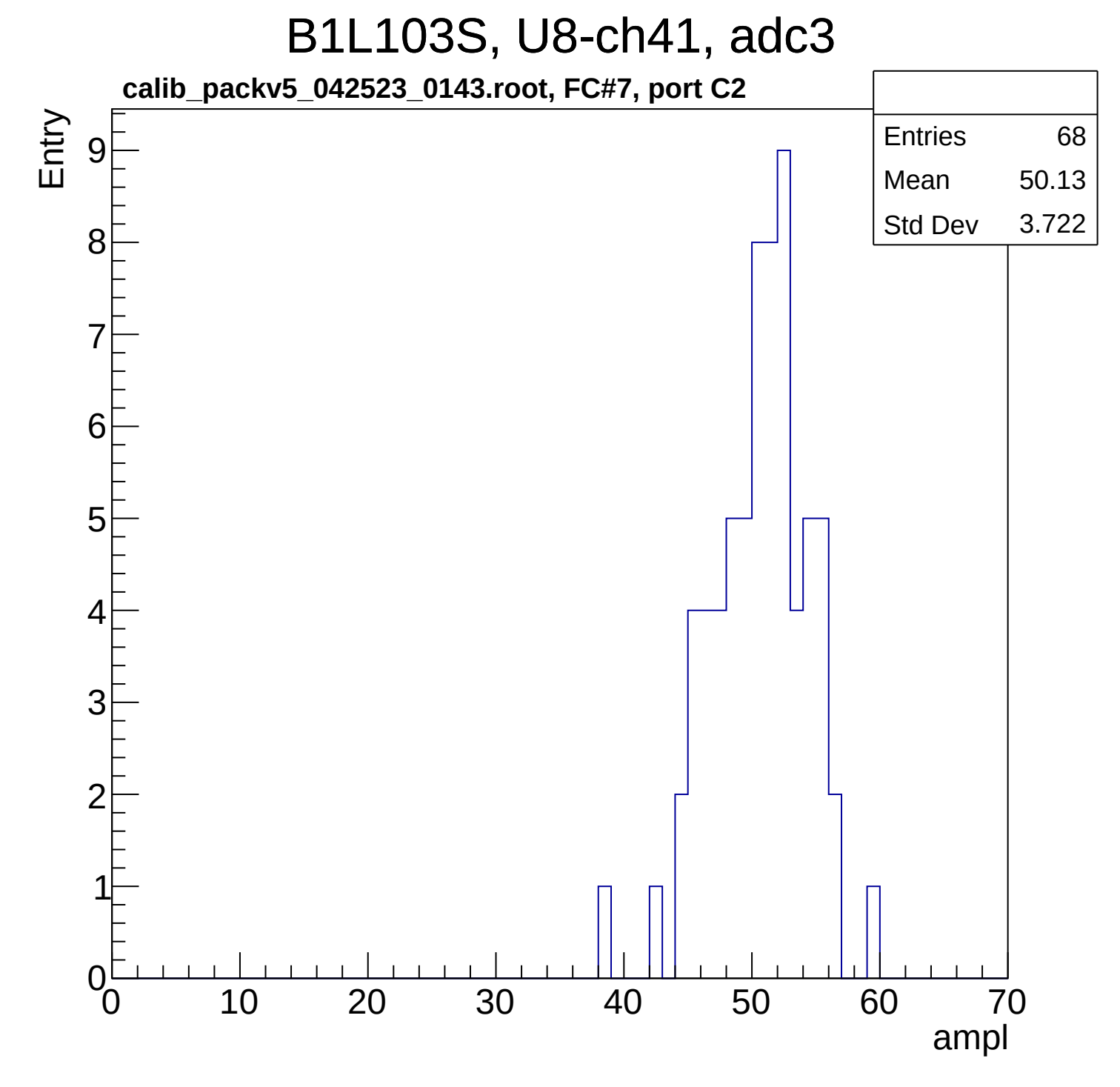

B1L103S, U8-ch40, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 7
Mean 62
Std Dev 1.414
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

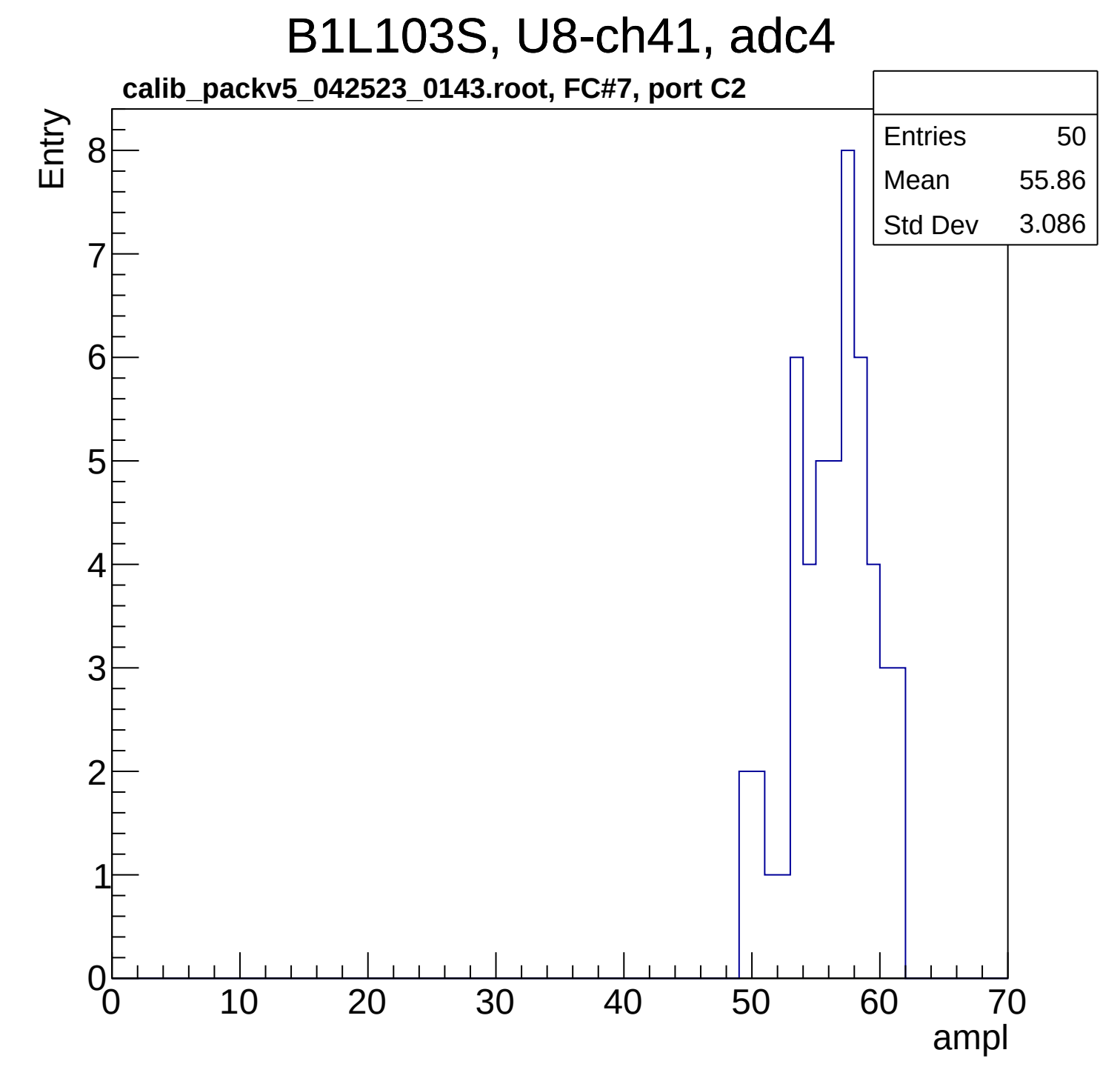

B1L103S, U8-ch40, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

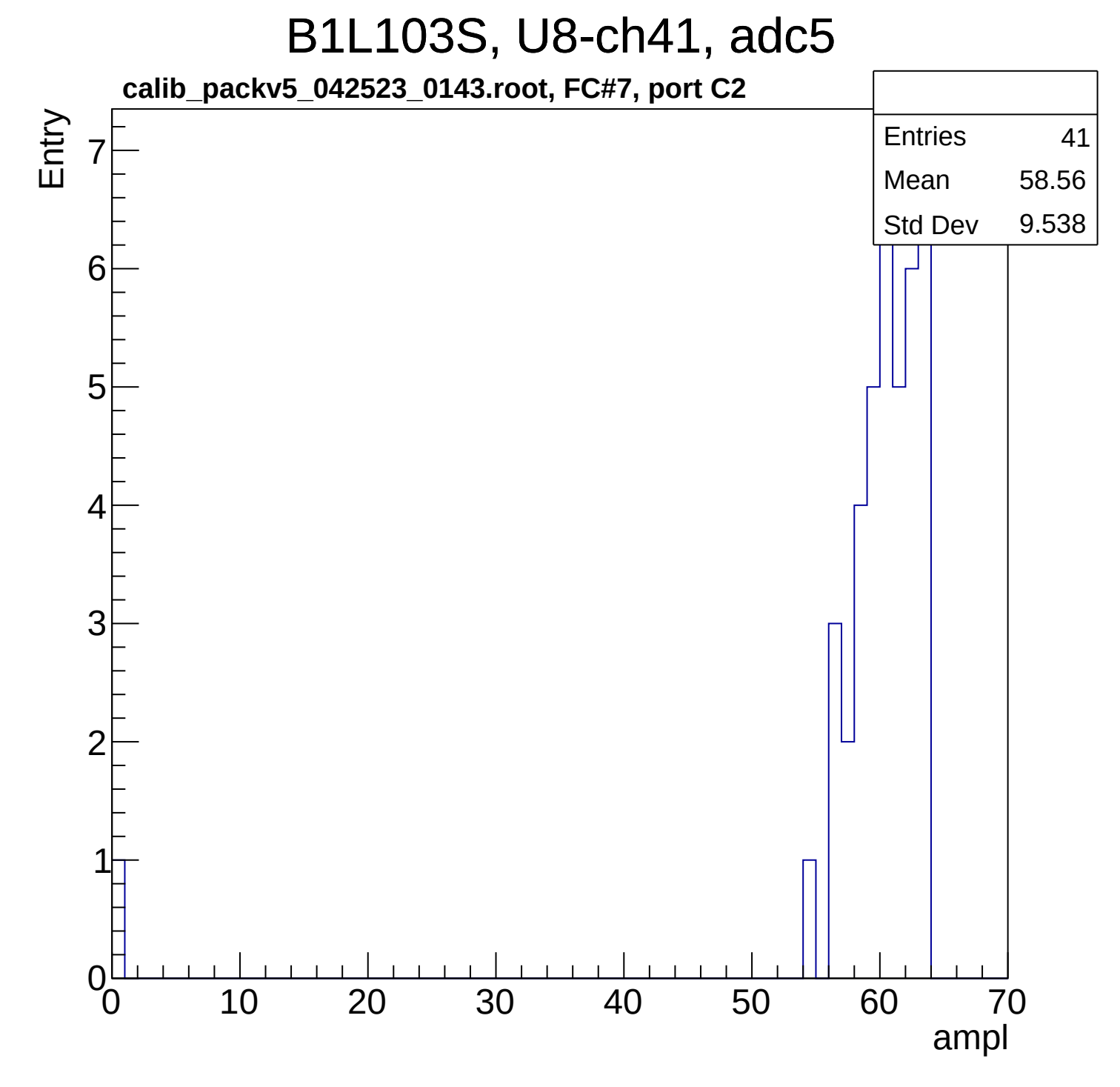

B1L103S, U8-ch41, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 29.47
Std Dev 3.656
Gaus mean : 30.5336
Gaus Width: 3.9812
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

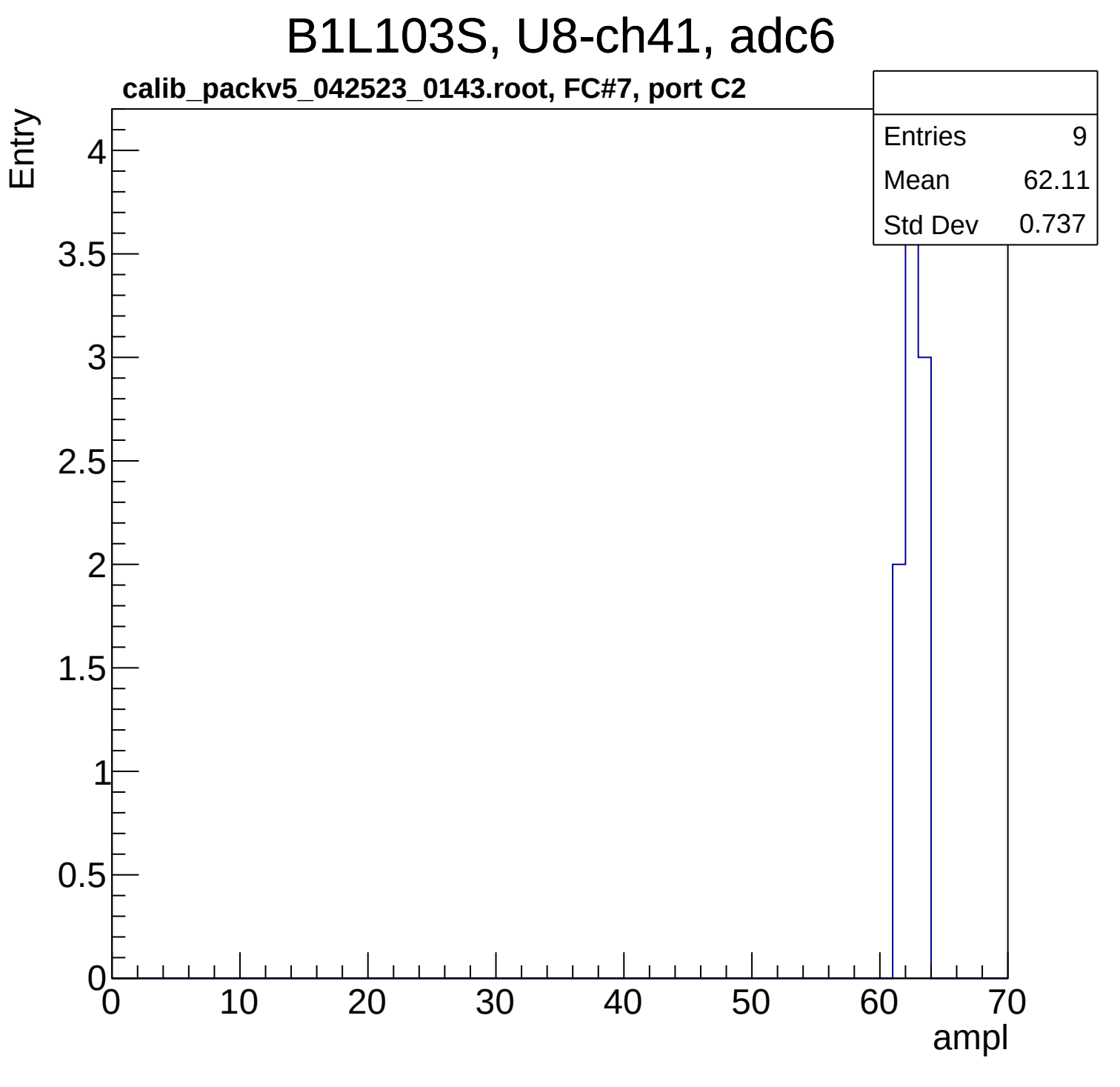

B1L103S, U8-ch41, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 76
Mean 37.41
Std Dev 3.555
Gaus mean : 37.7692
Gaus Width: 3.5728
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

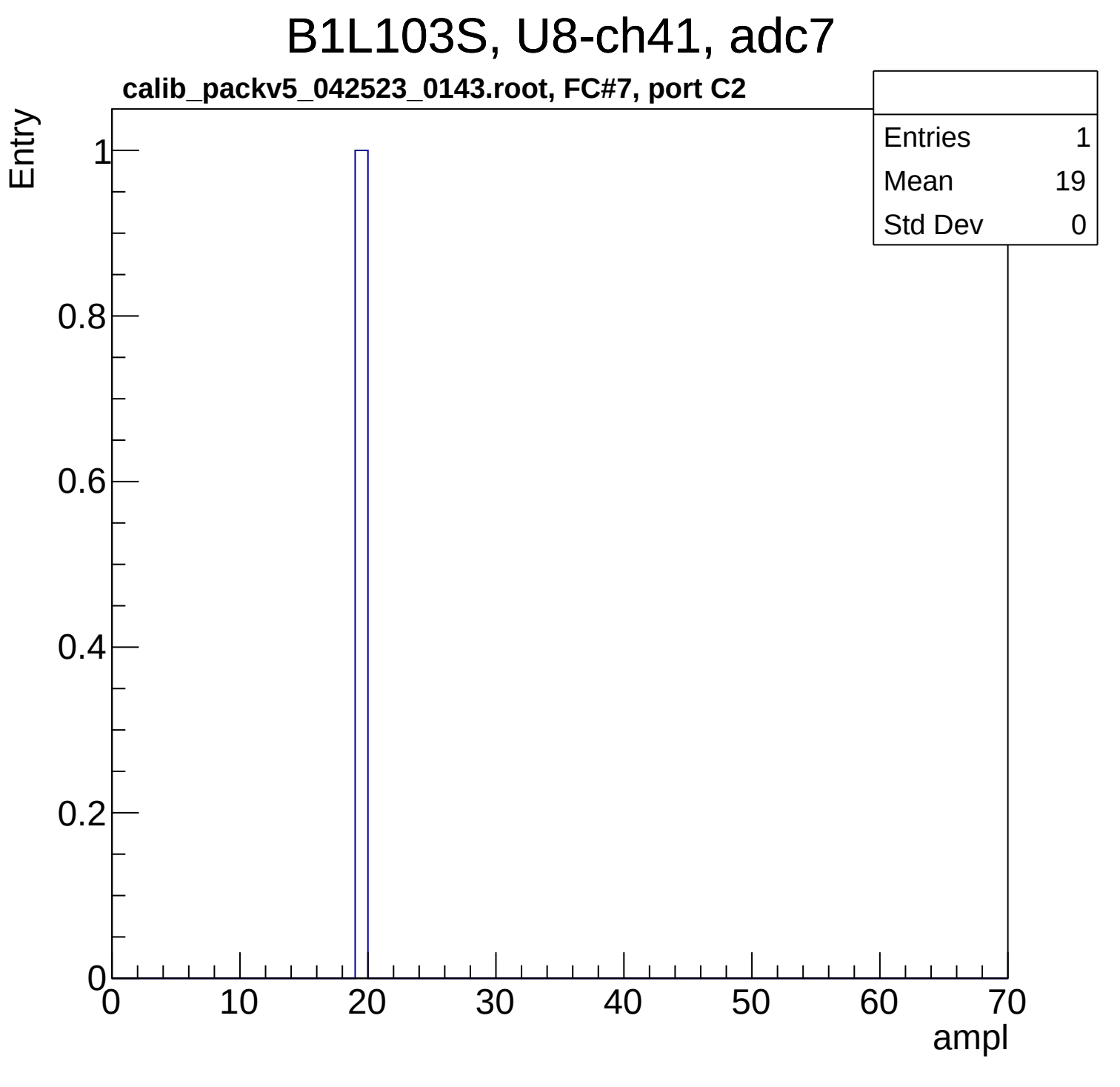

B1L103S, U8-ch41, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 44.05
Std Dev 3.08
Gaus mean : 45.3906
Gaus Width: 3.3957
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

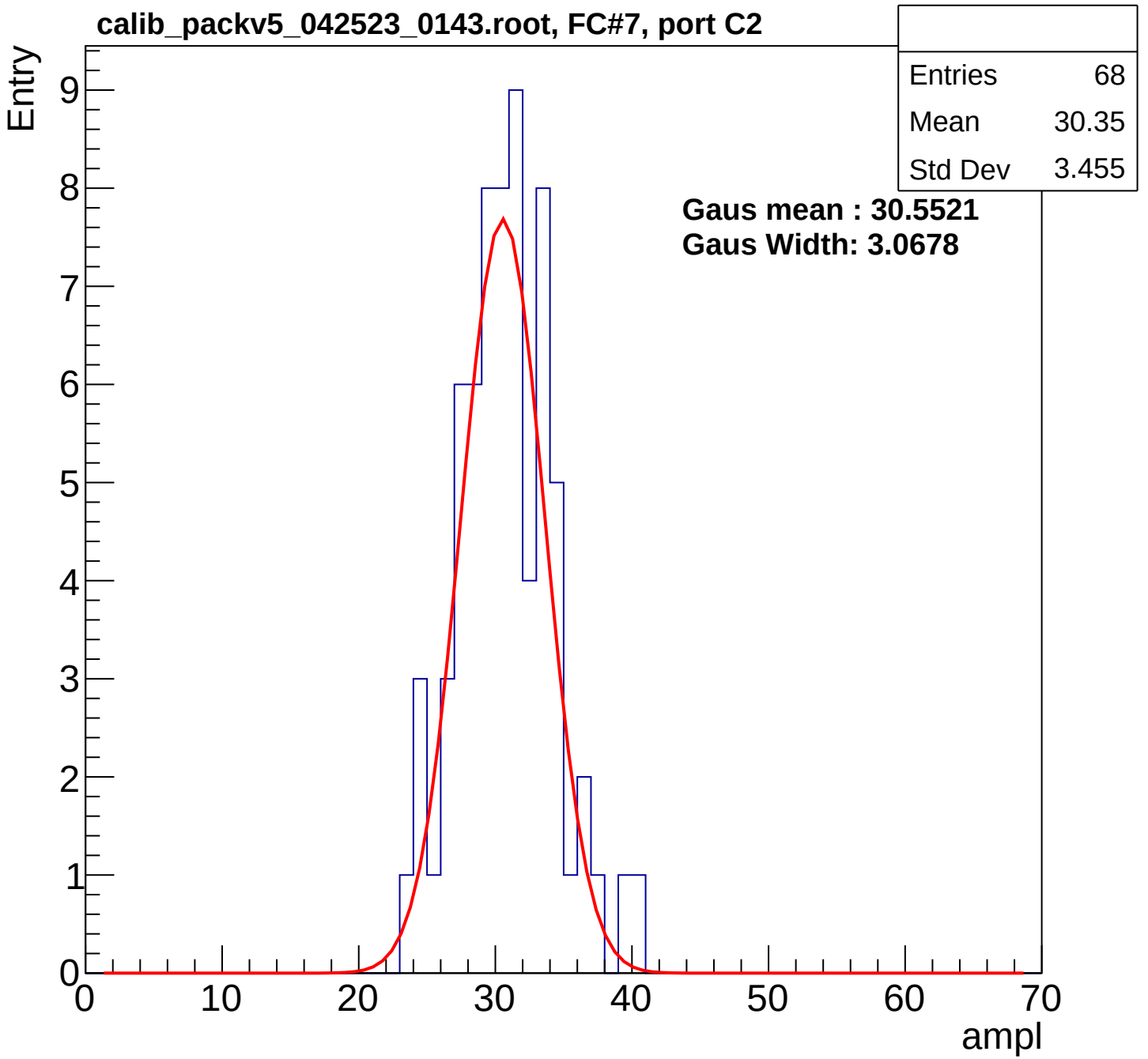

B1L103S, U8-ch41, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 50.13
Std Dev 3.722
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

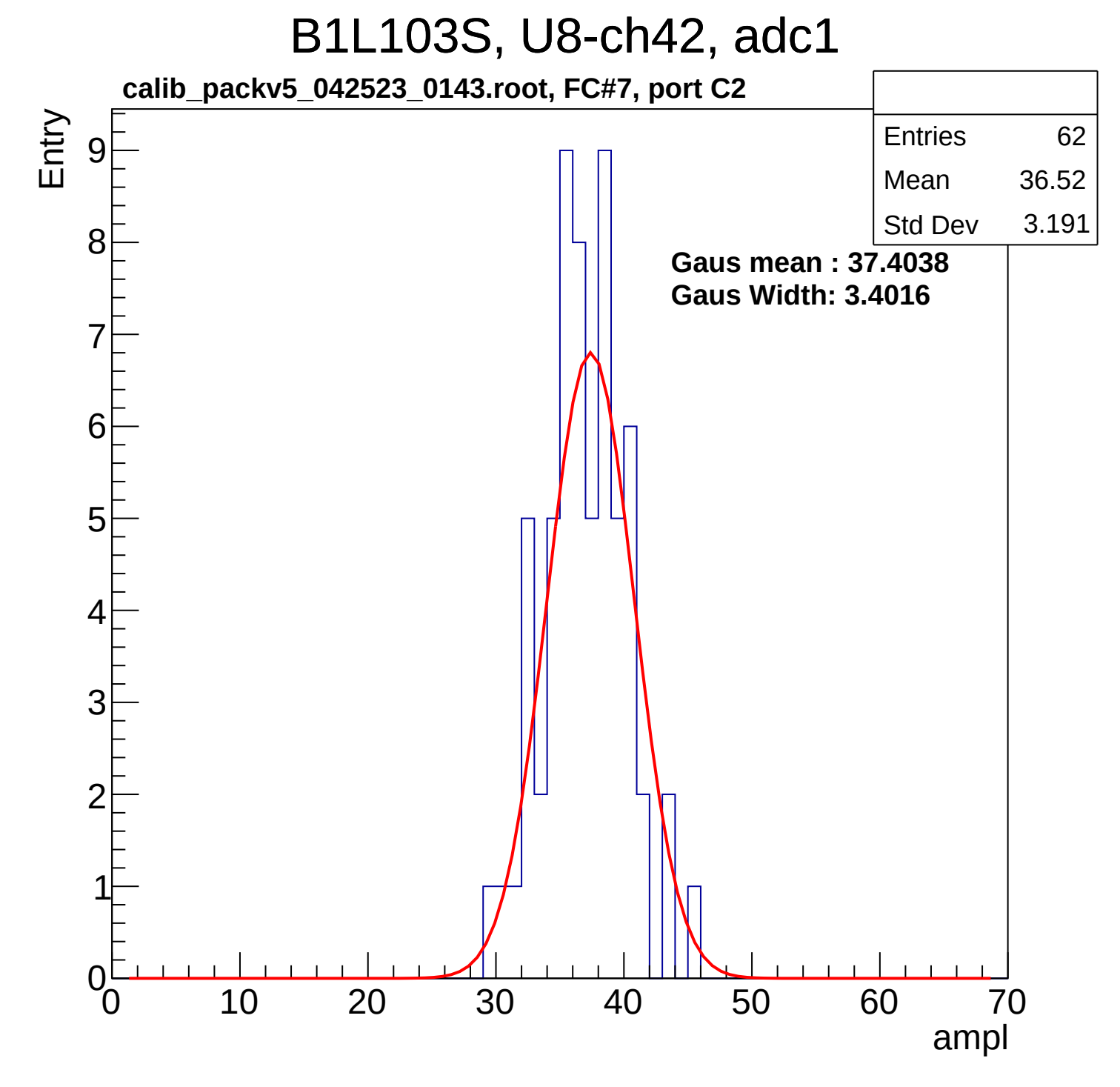

B1L103S, U8-ch41, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 55.86
Std Dev 3.086
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

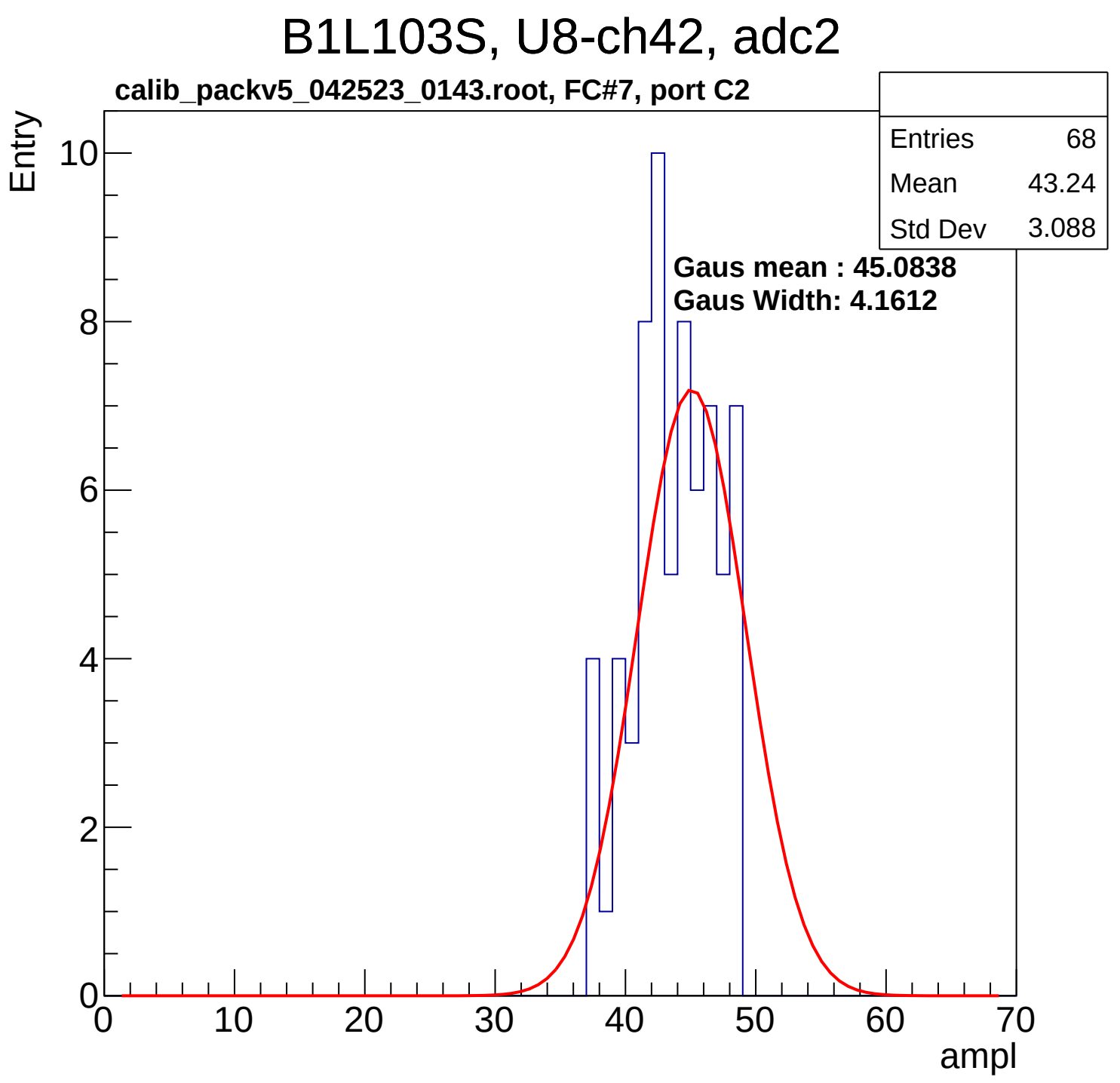

B1L103S, U8-ch41, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 41
Mean 58.56
Std Dev 9.538
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

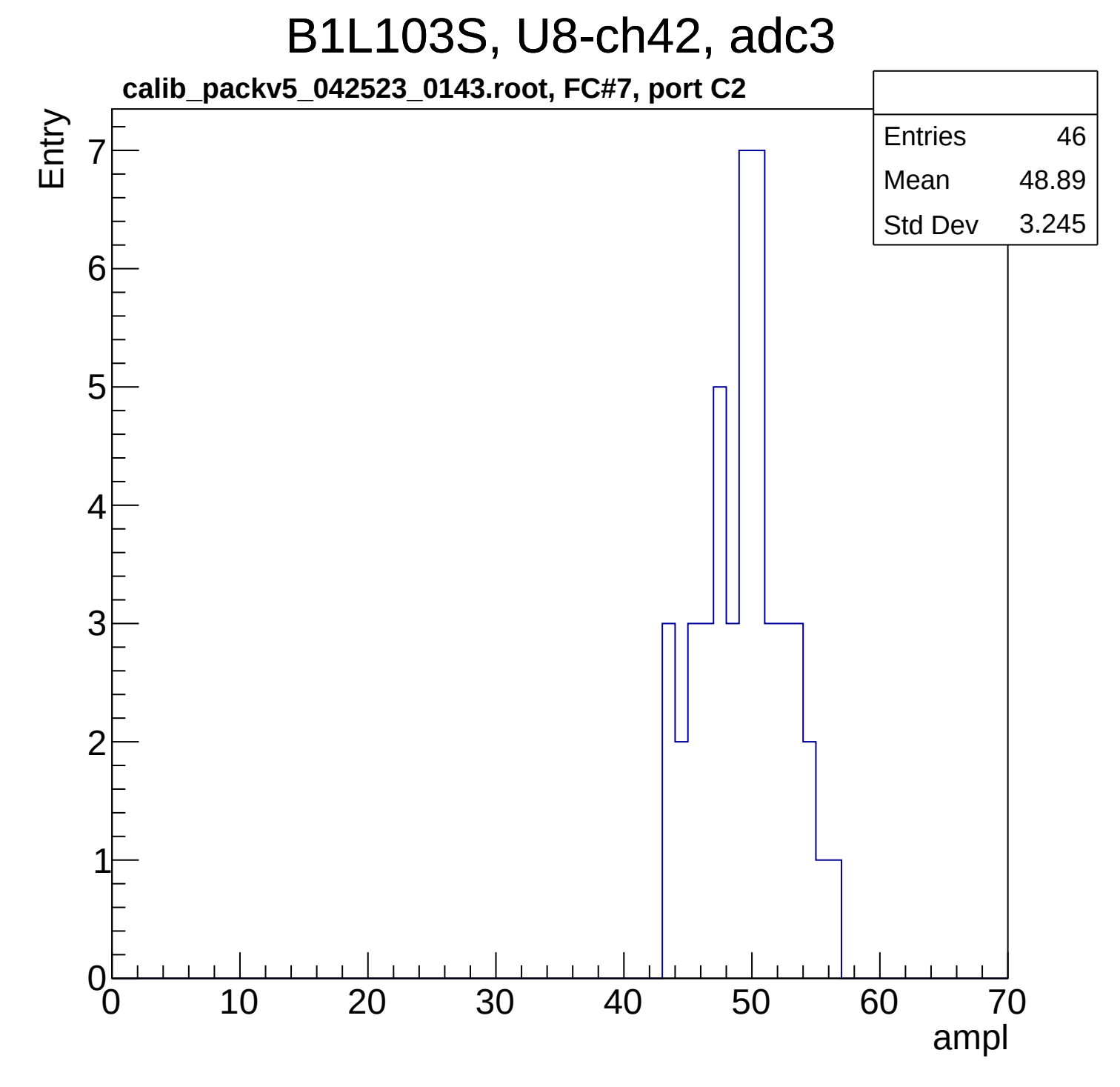

B1L103S, U8-ch41, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 9
Mean 62.11
Std Dev 0.737
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

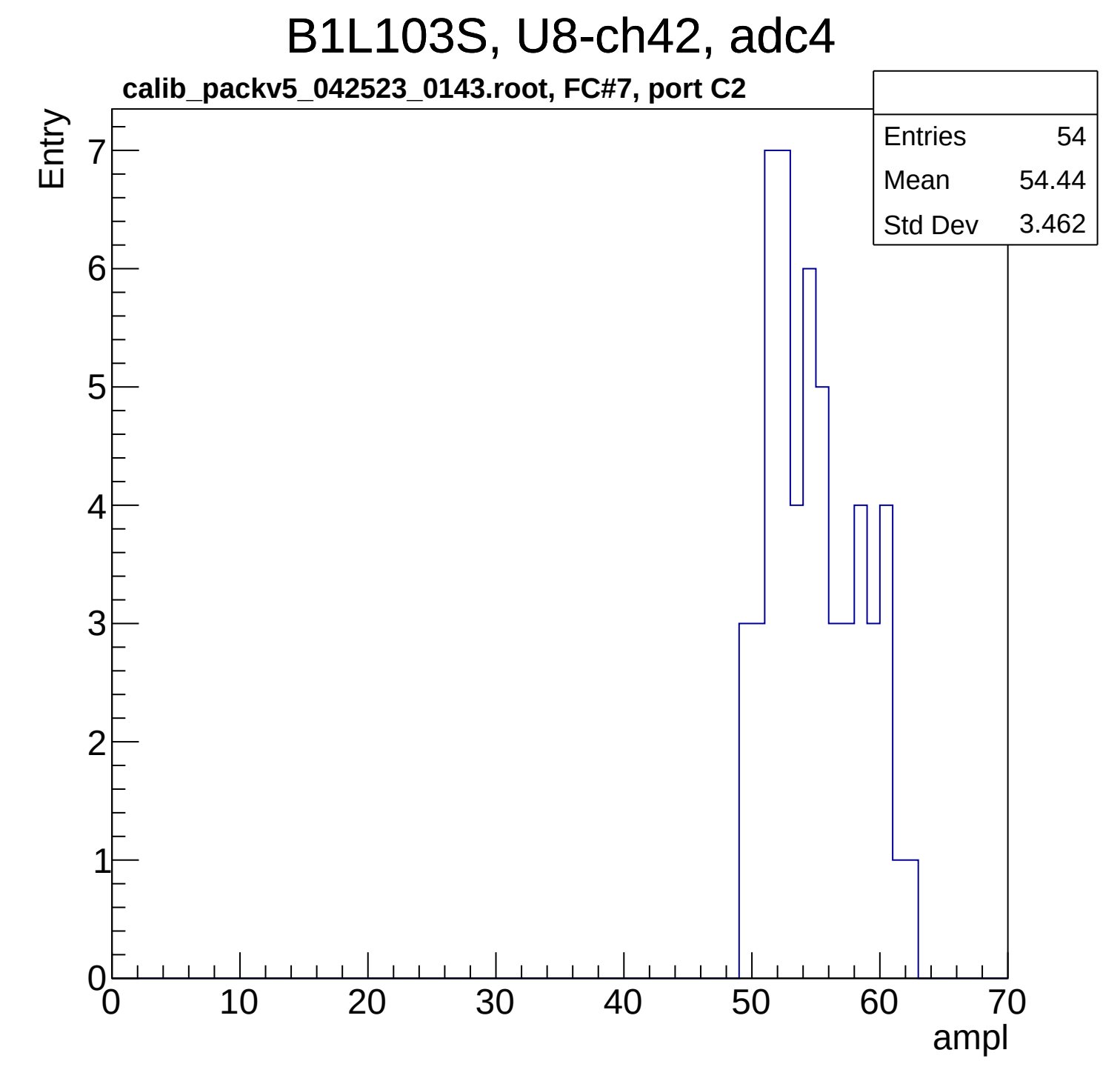

B1L103S, U8-ch41, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 19
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

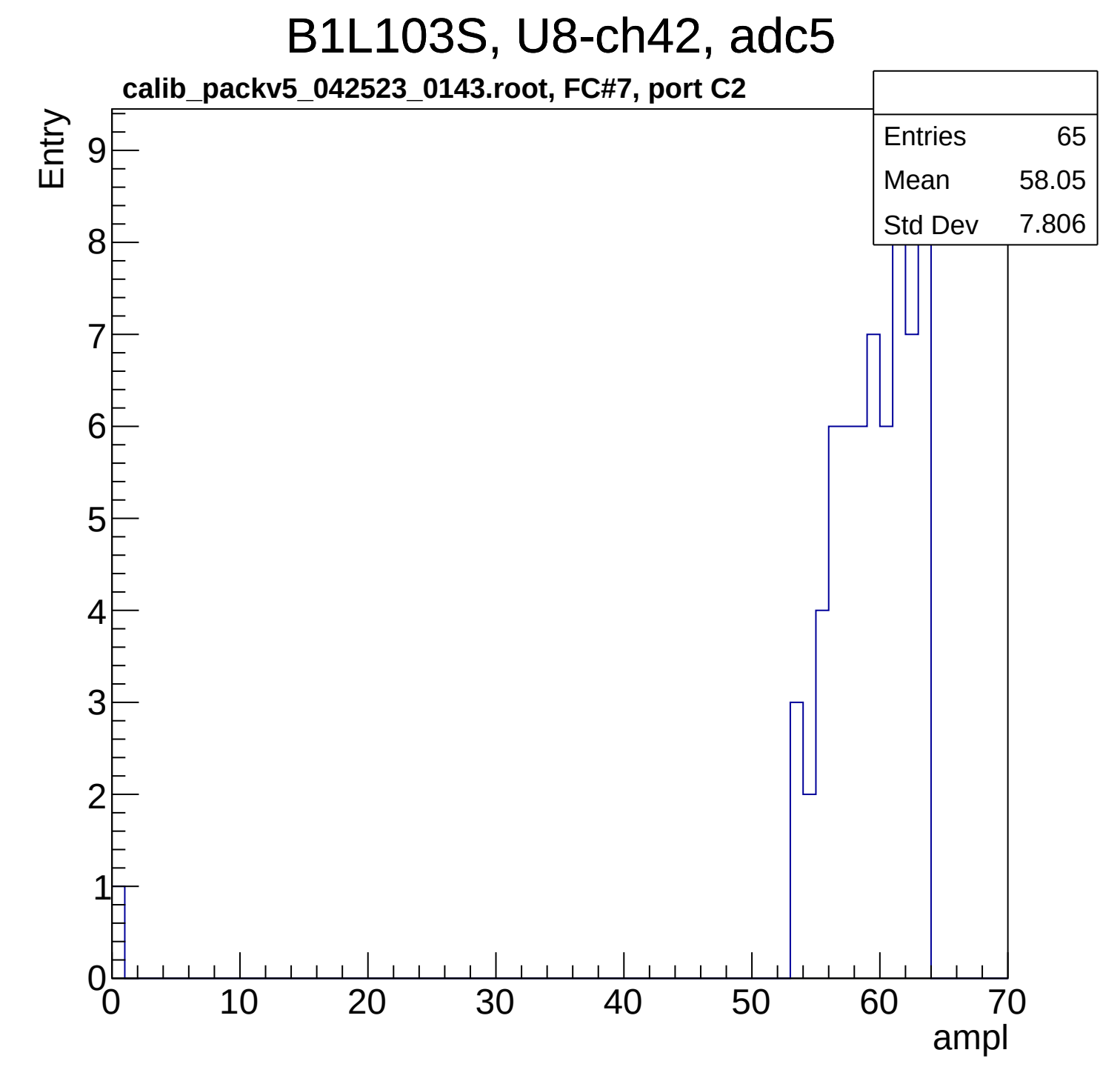

B1L103S, U8-ch42, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 30.35
Std Dev 3.455
Gaus mean : 30.5521
Gaus Width: 3.0678
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

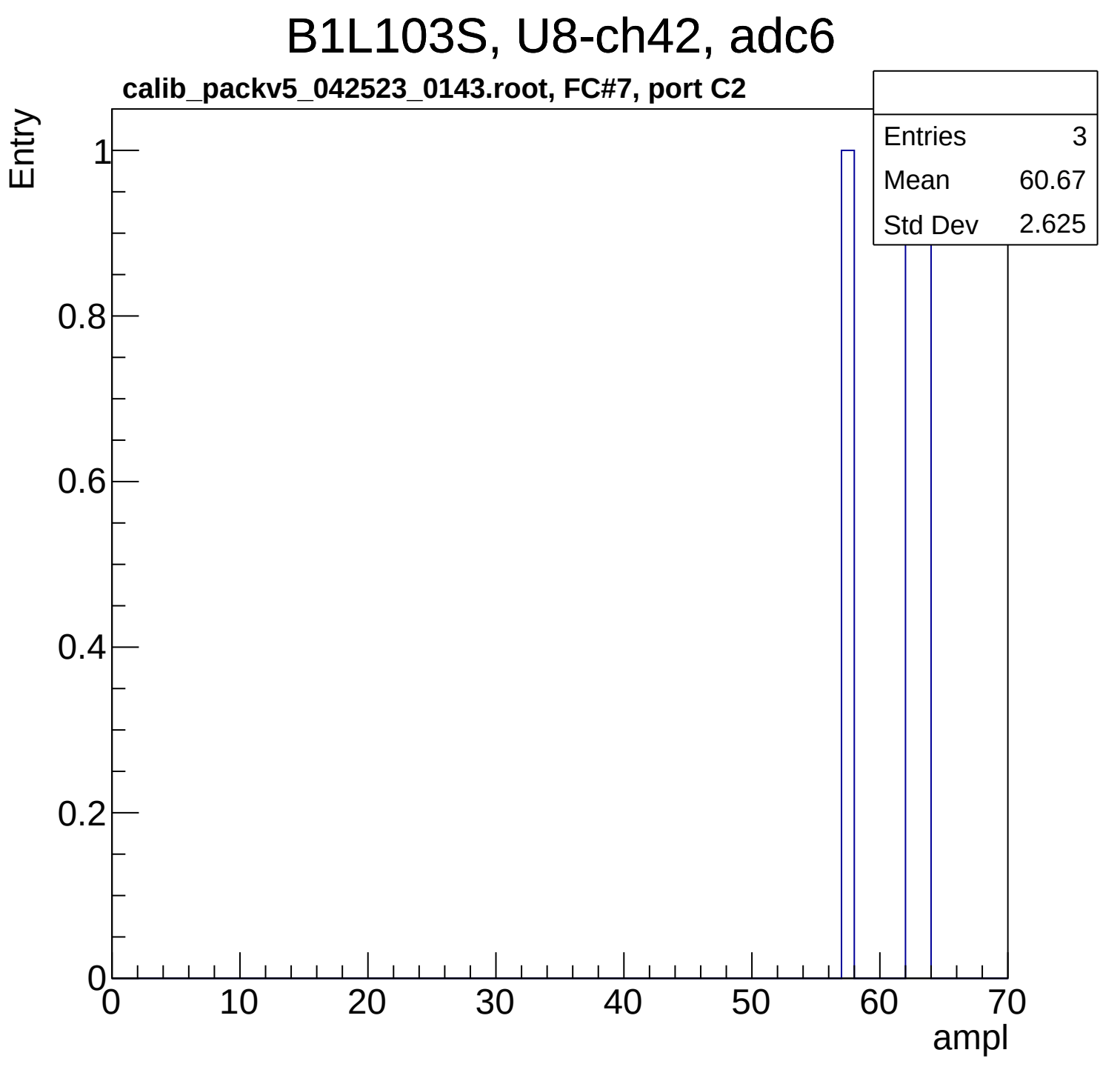

B1L103S, U8-ch42, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 36.52
Std Dev 3.191
Gaus mean : 37.4038
Gaus Width: 3.4016
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

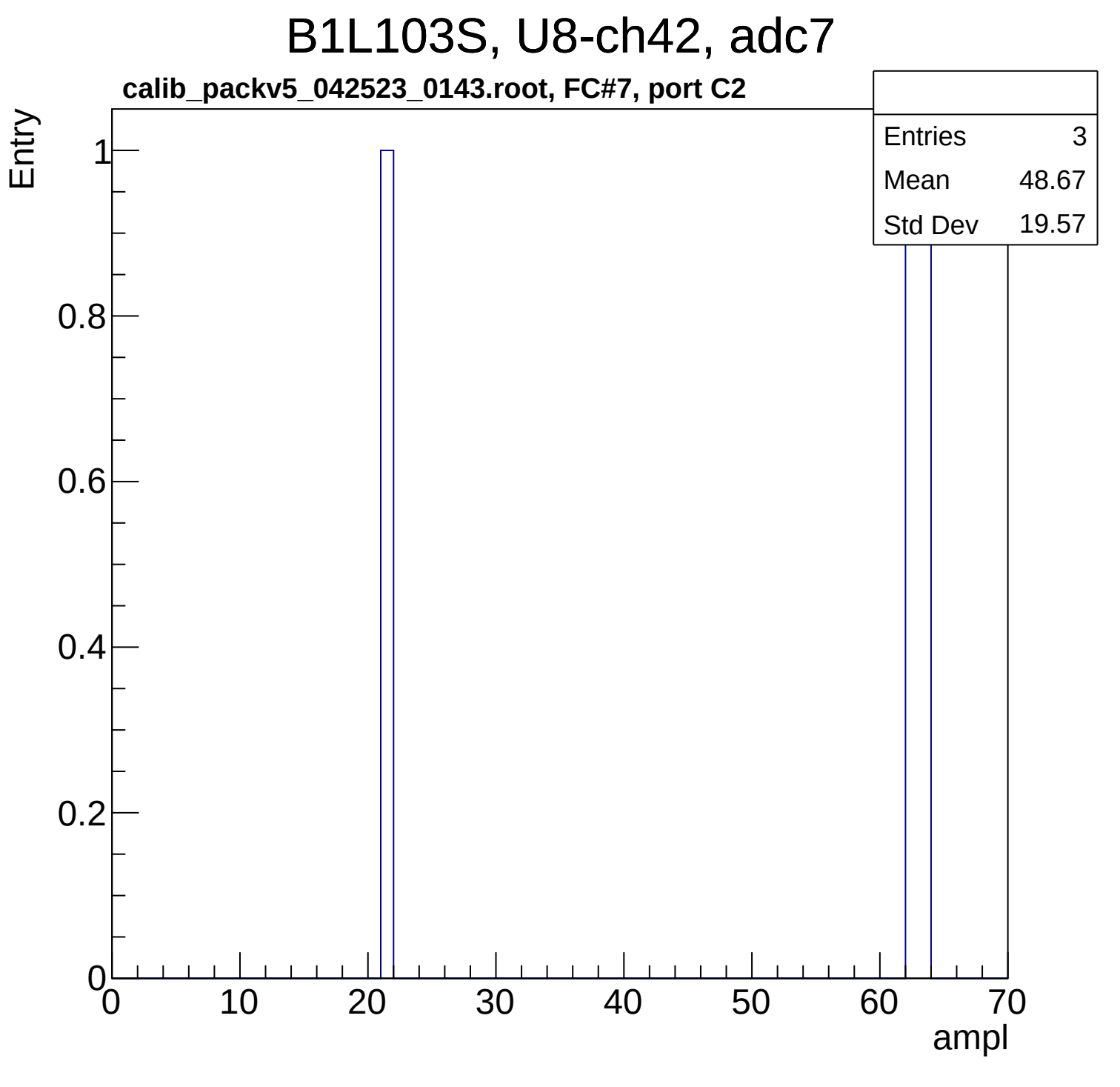

B1L103S, U8-ch42, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 43.24
Std Dev 3.088
Gaus mean : 45.0838
Gaus Width: 4.1612
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

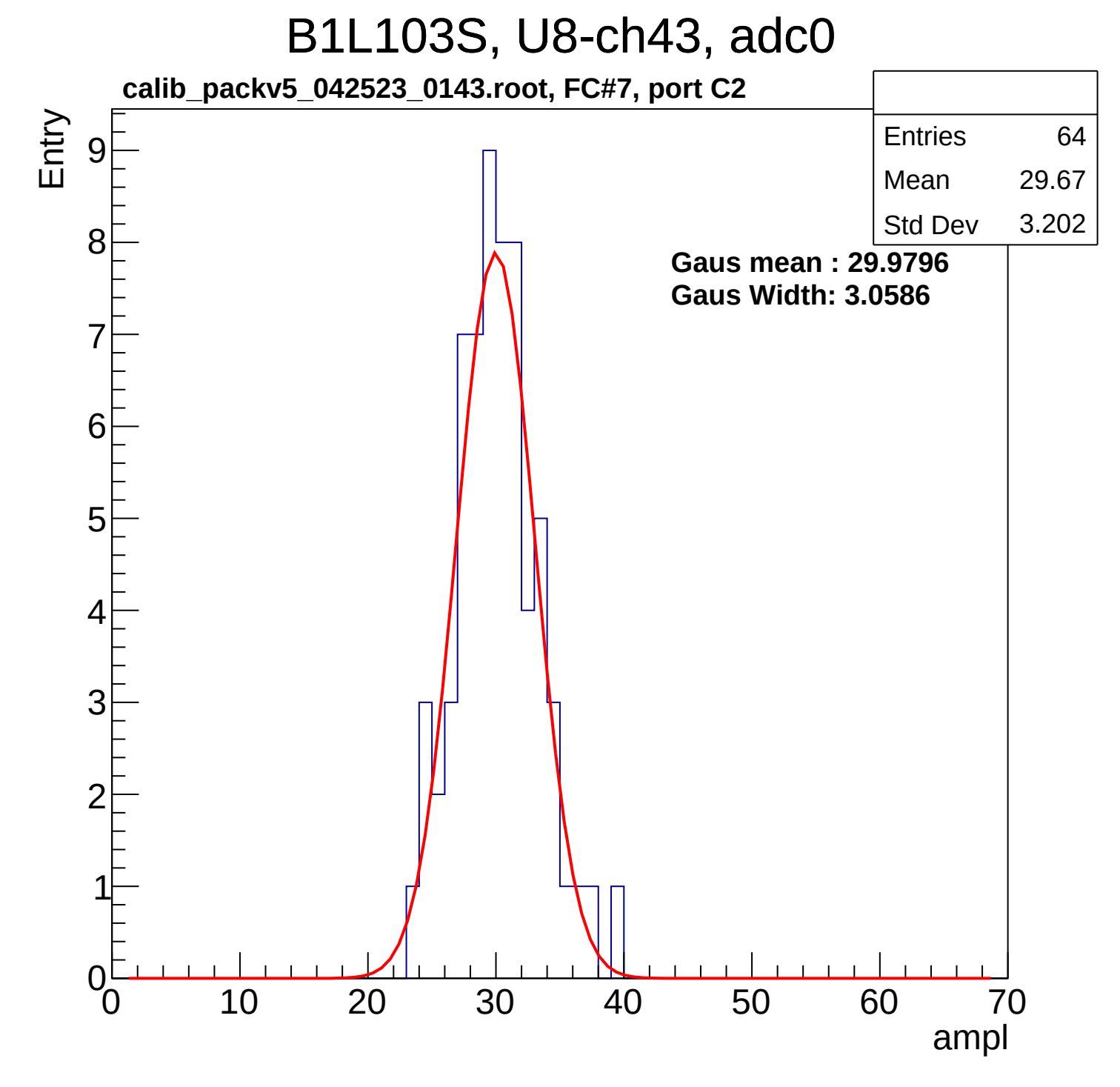

B1L103S, U8-ch42, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 46
Mean 48.89
Std Dev 3.245
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

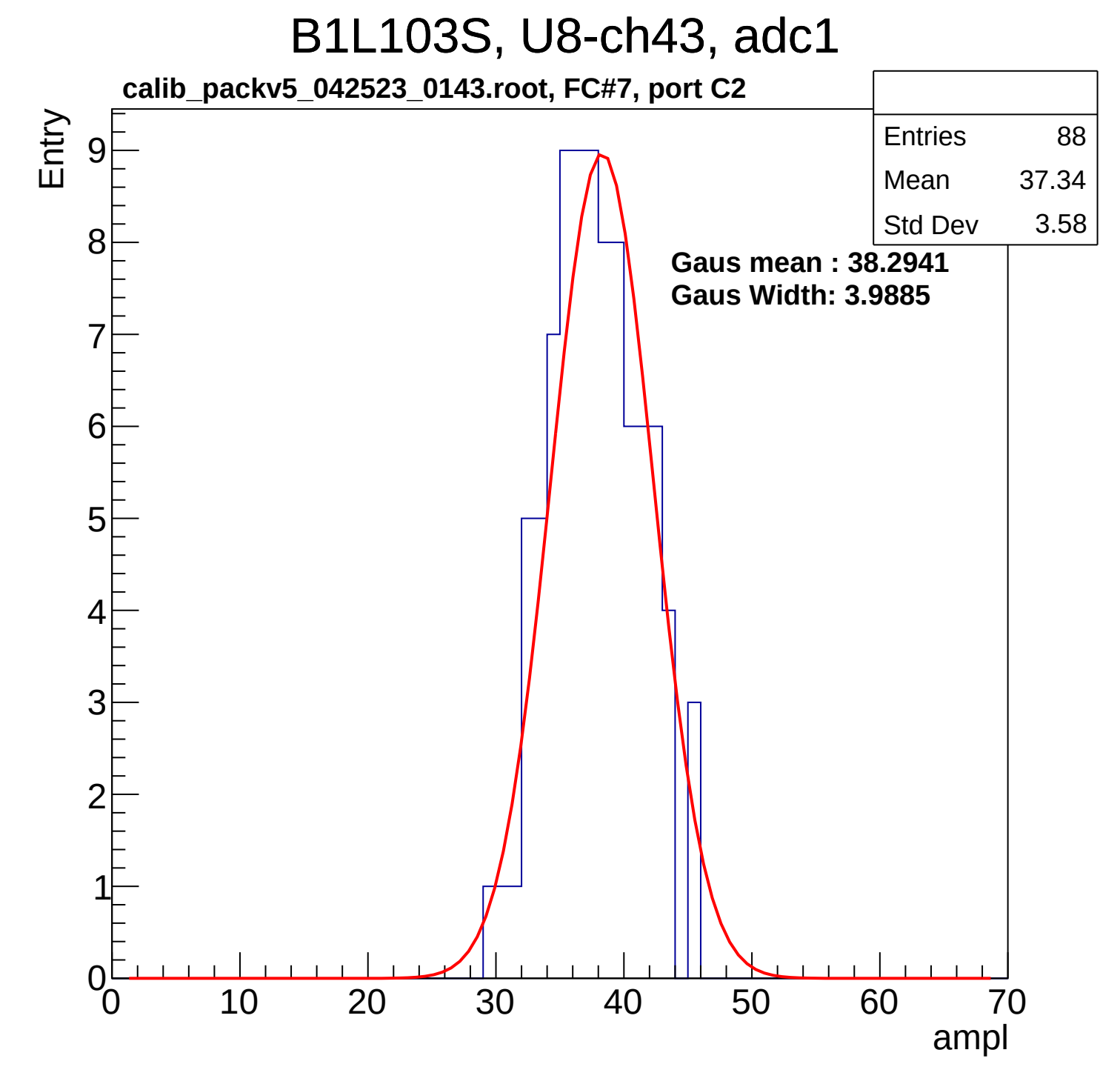

B1L103S, U8-ch42, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 54.44
Std Dev 3.462
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

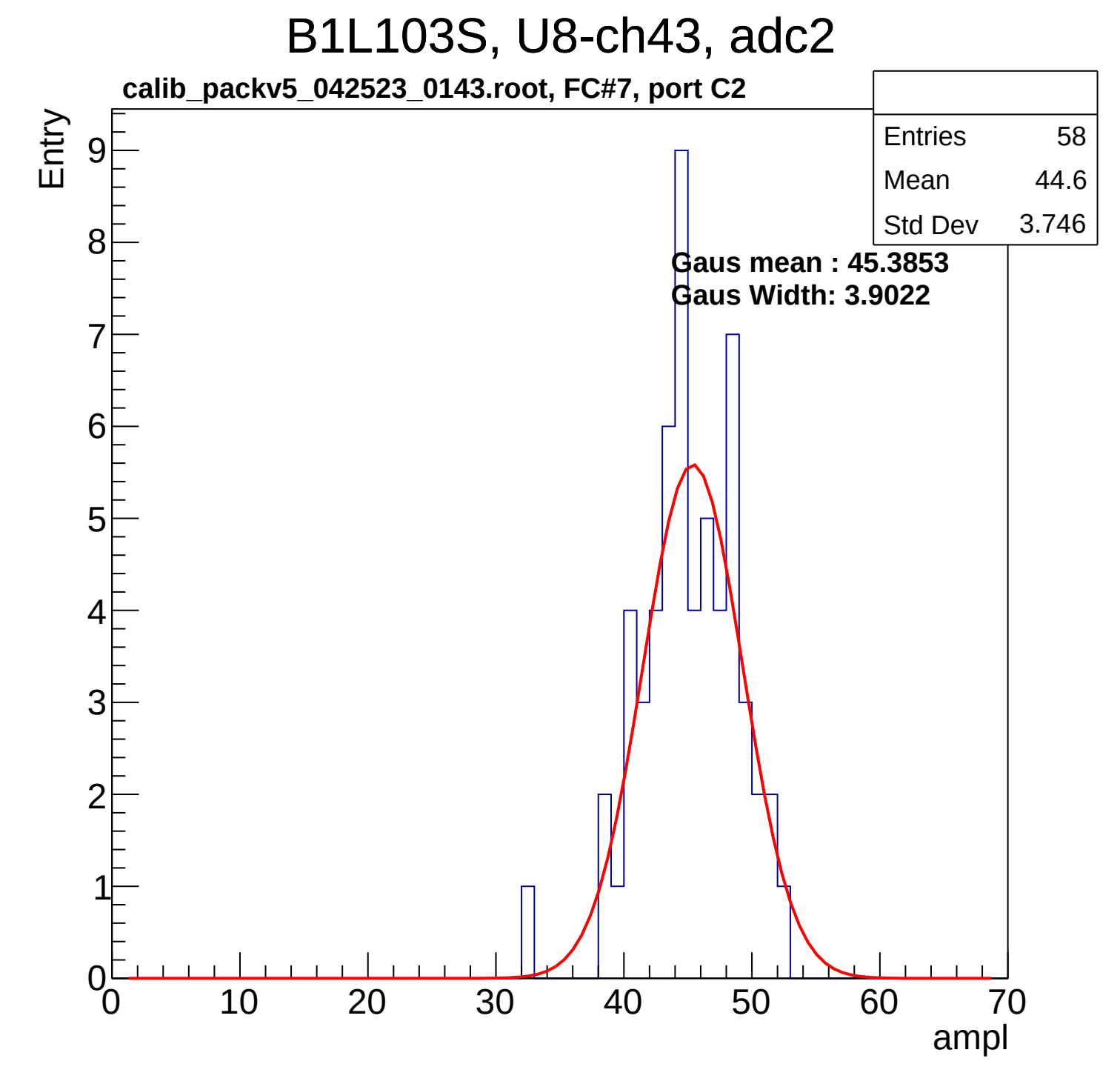

B1L103S, U8-ch42, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 58.05
Std Dev 7.806
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

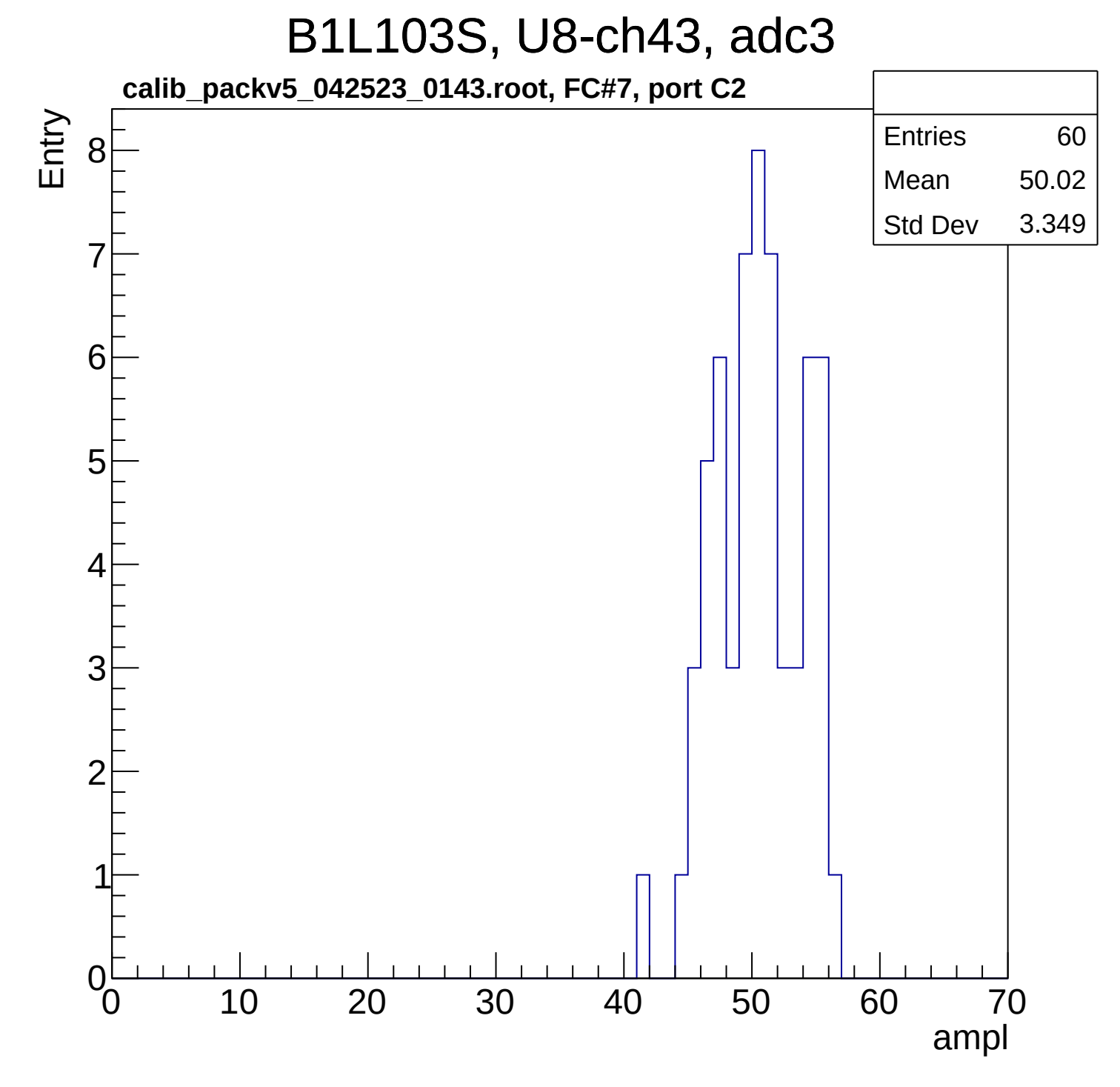

B1L103S, U8-ch42, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 60.67
Std Dev 2.625
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

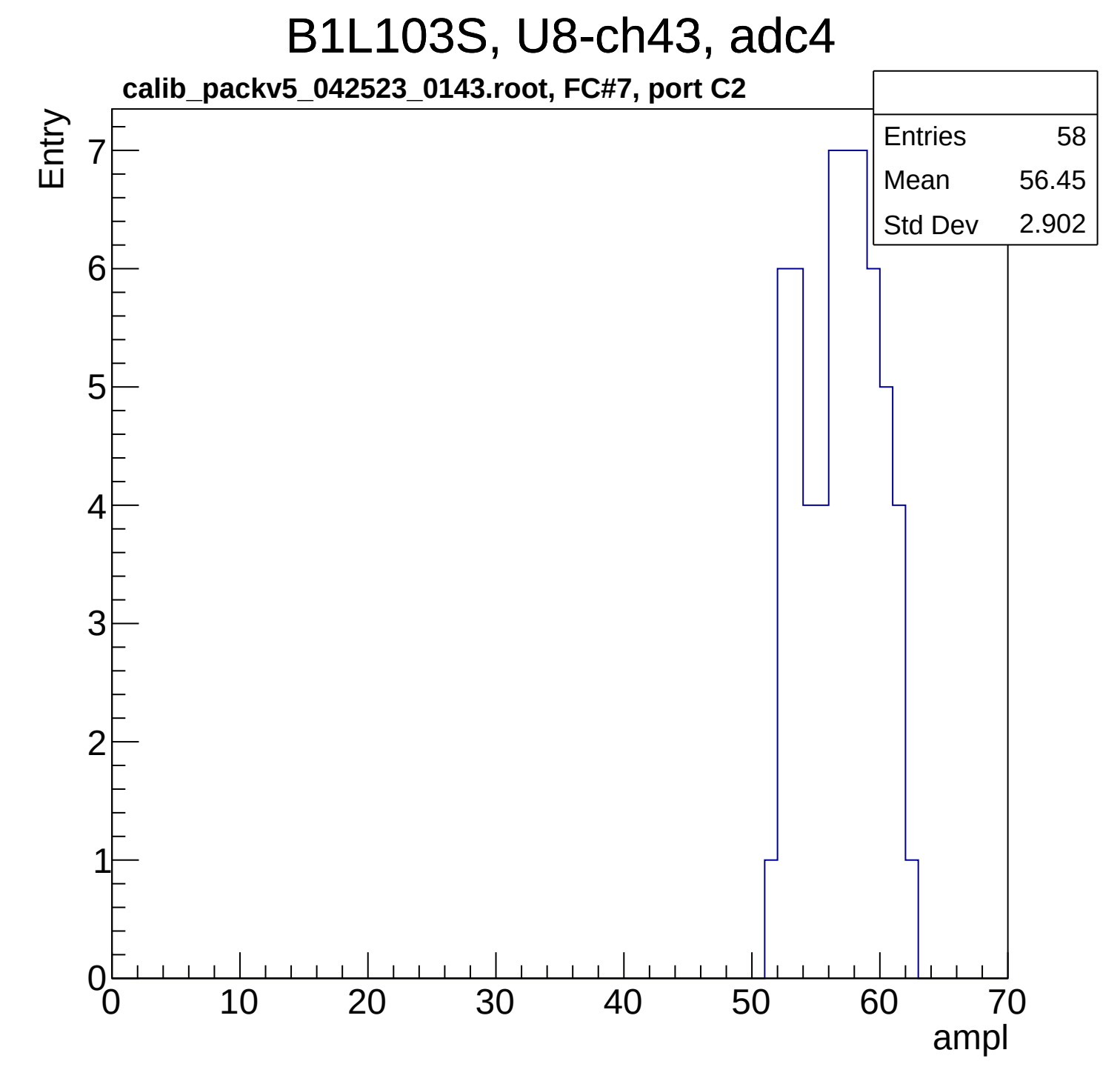

B1L103S, U8-ch42, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 48.67
Std Dev 19.57
Entry
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70
ampl

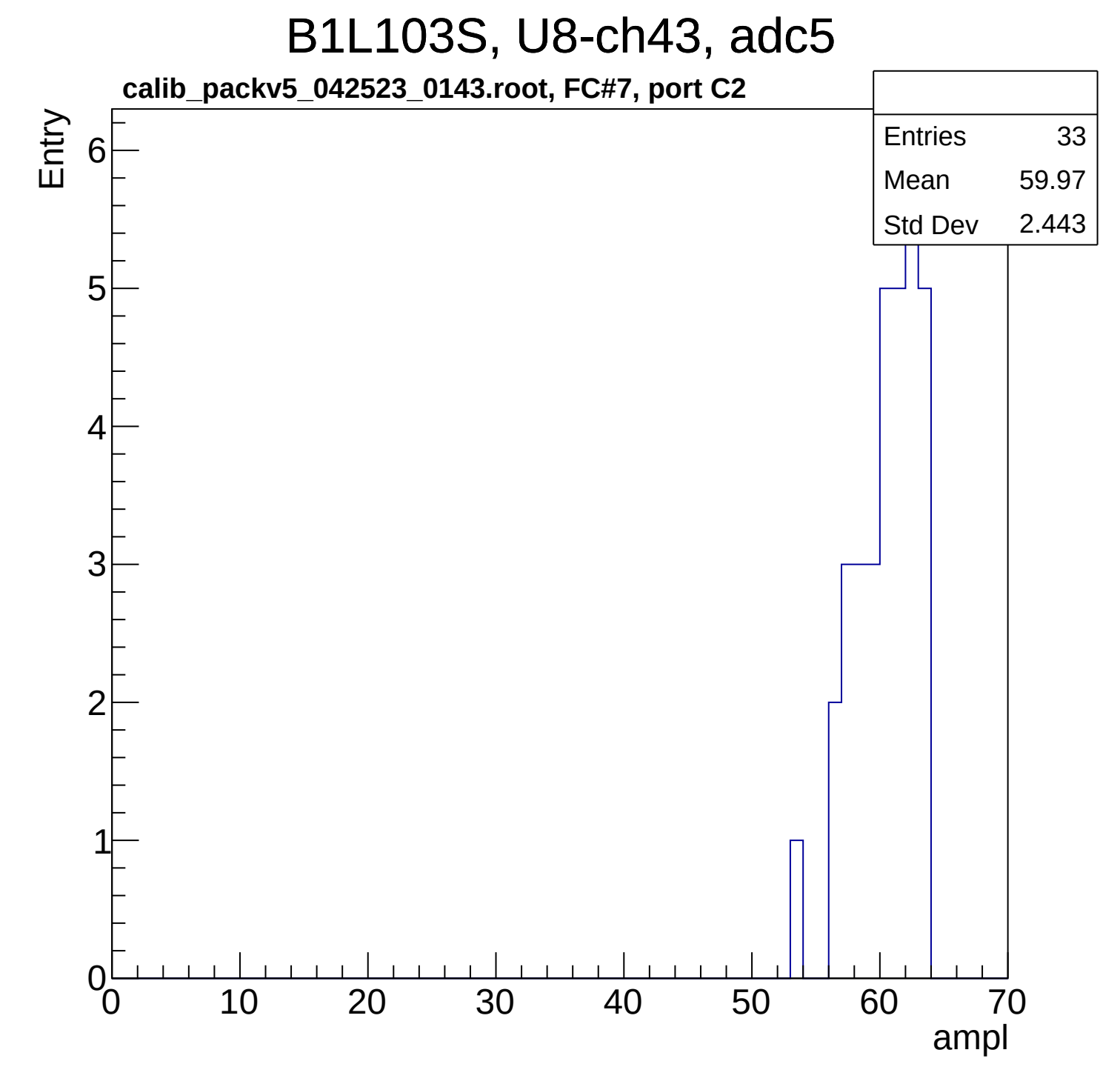

B1L103S, U8-ch43, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 29.67
Std Dev 3.202
Gaus mean : 29.9796
Gaus Width: 3.0586
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

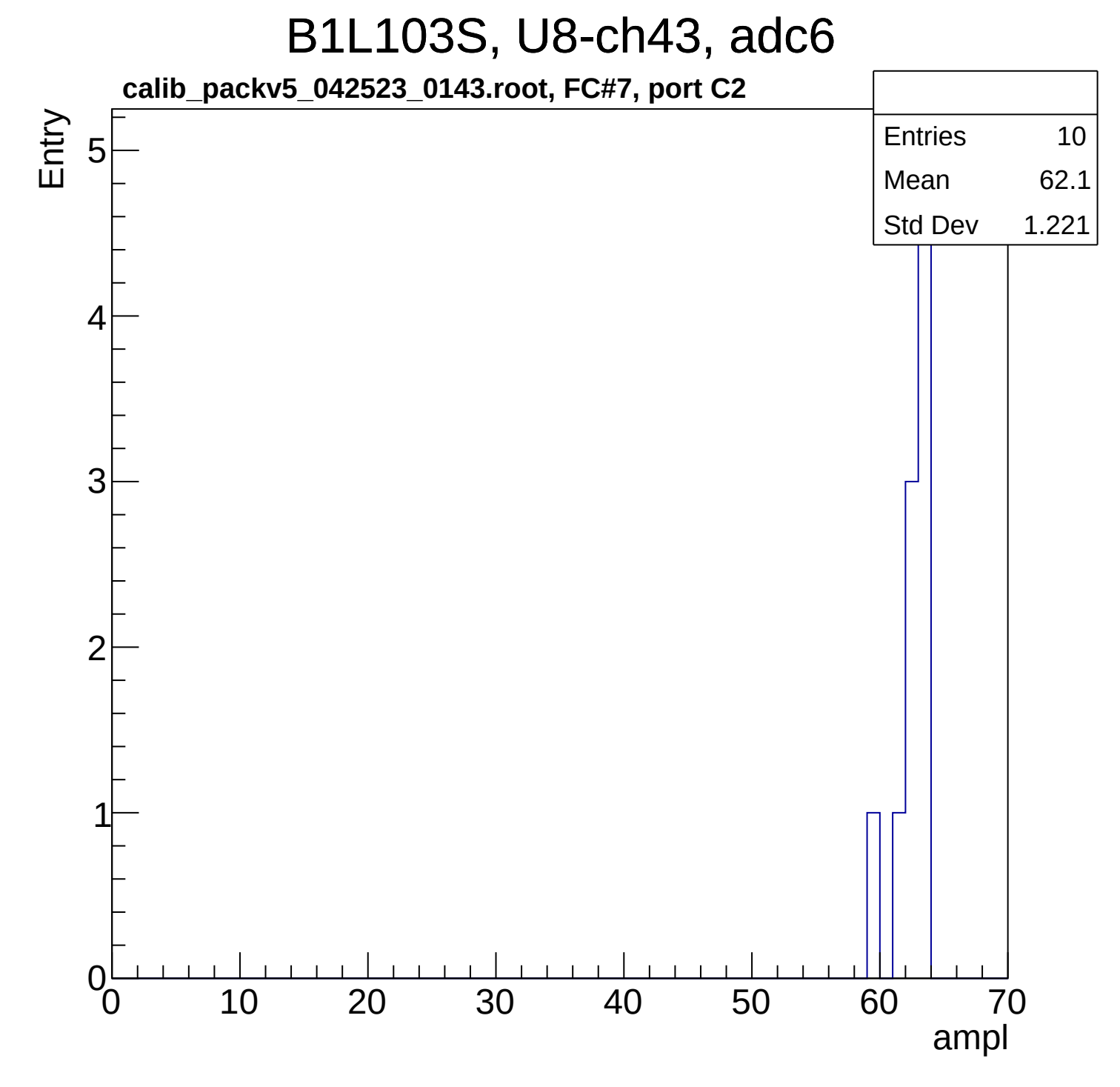

B1L103S, U8-ch43, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 88
Mean 37.34
Std Dev 3.58
Gaus mean : 38.2941
Gaus Width: 3.9885
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

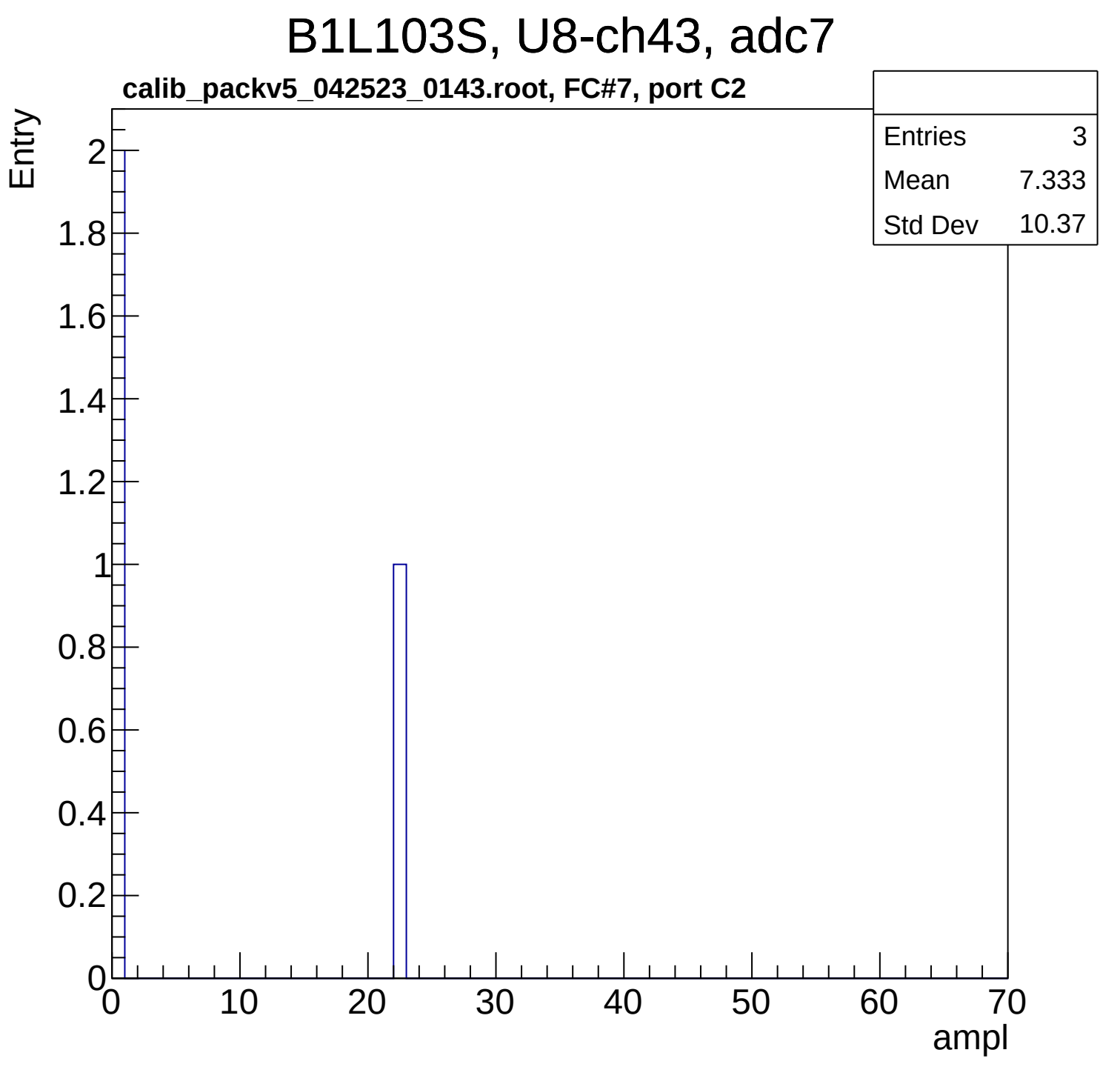

B1L103S, U8-ch43, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 44.6
Std Dev 3.746
Gaus mean : 45.3853
Gaus Width: 3.9022
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

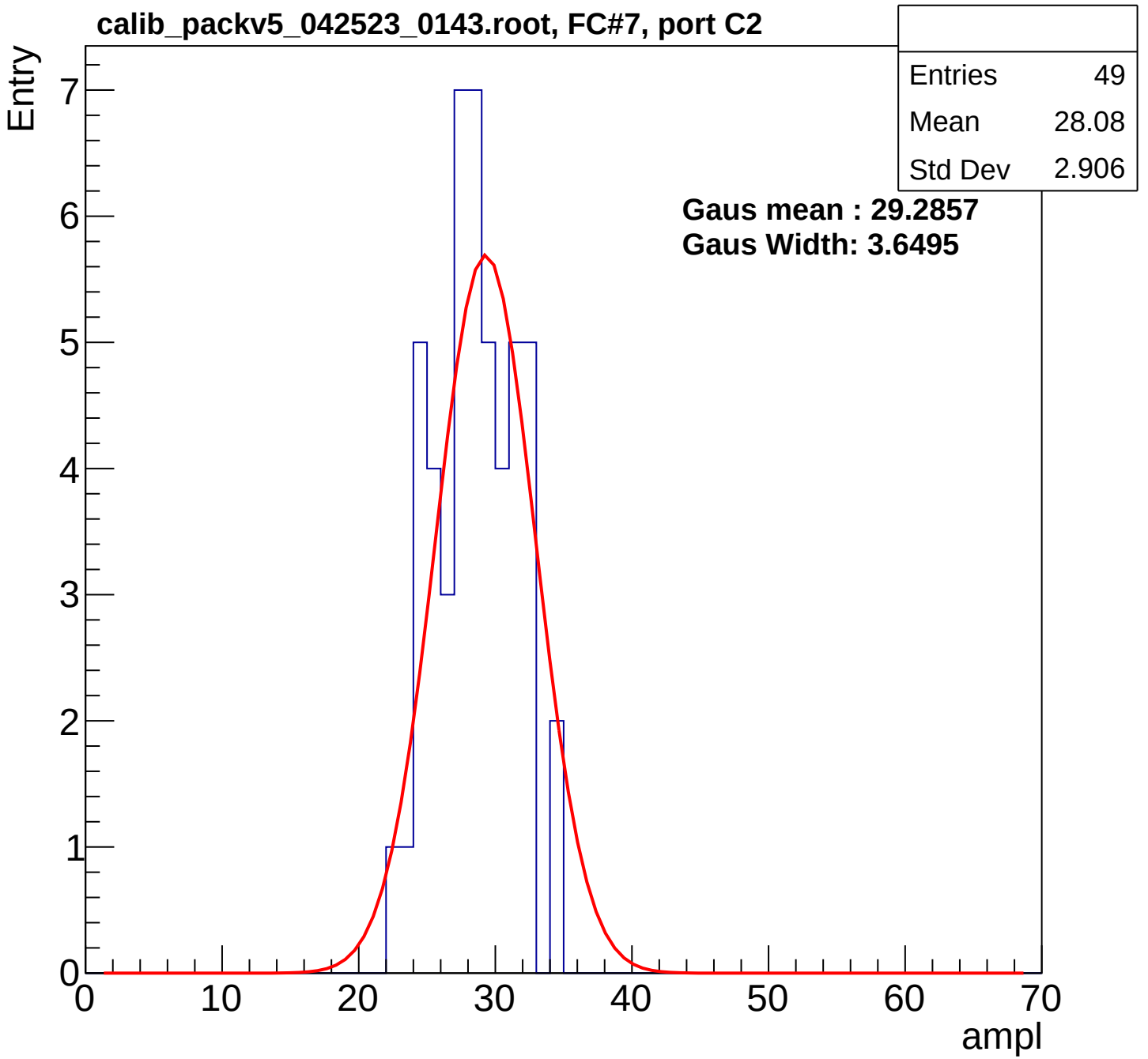

B1L103S, U8-ch43, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 50.02
Std Dev 3.349
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

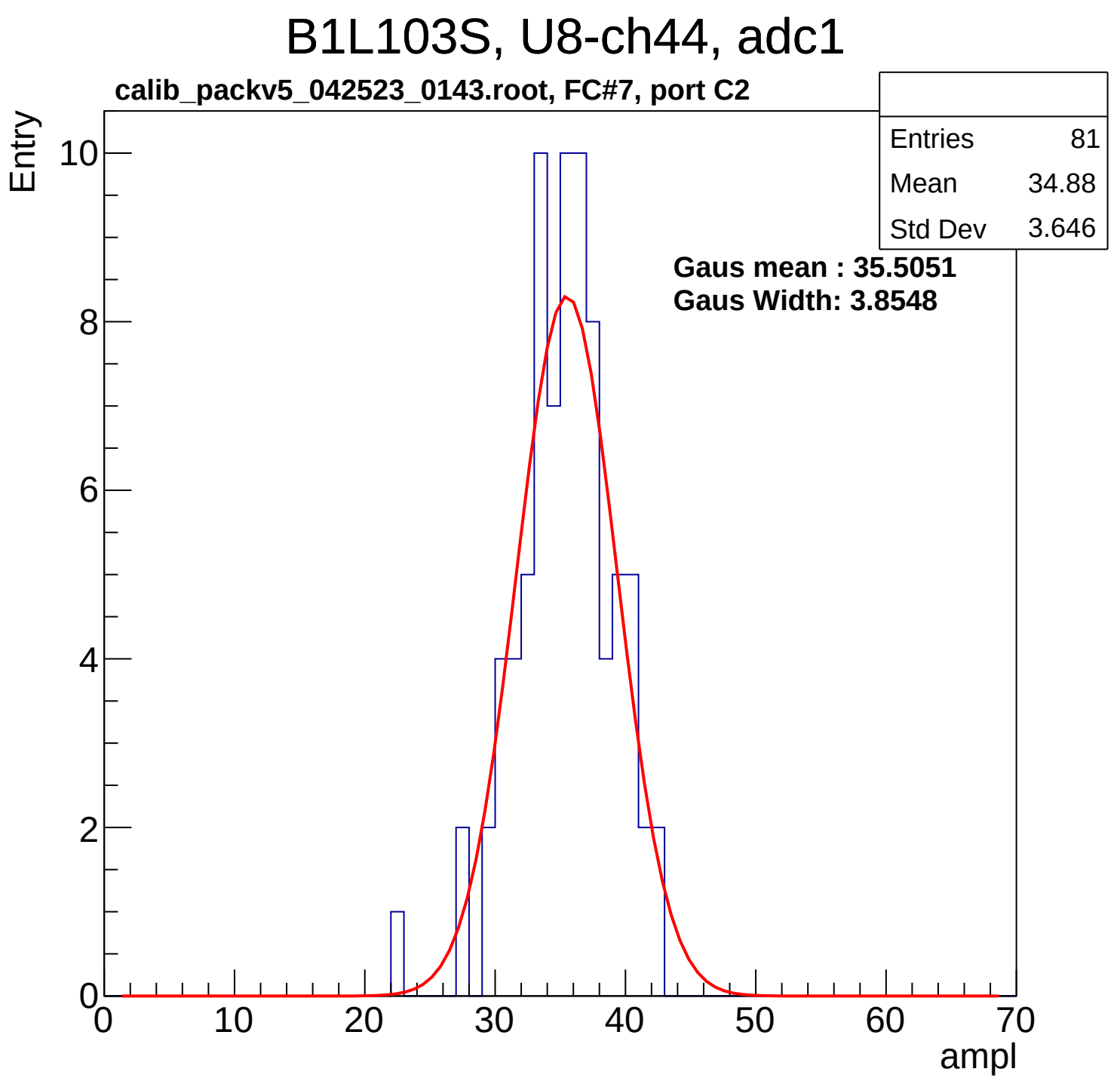

B1L103S, U8-ch43, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 56.45
Std Dev 2.902
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

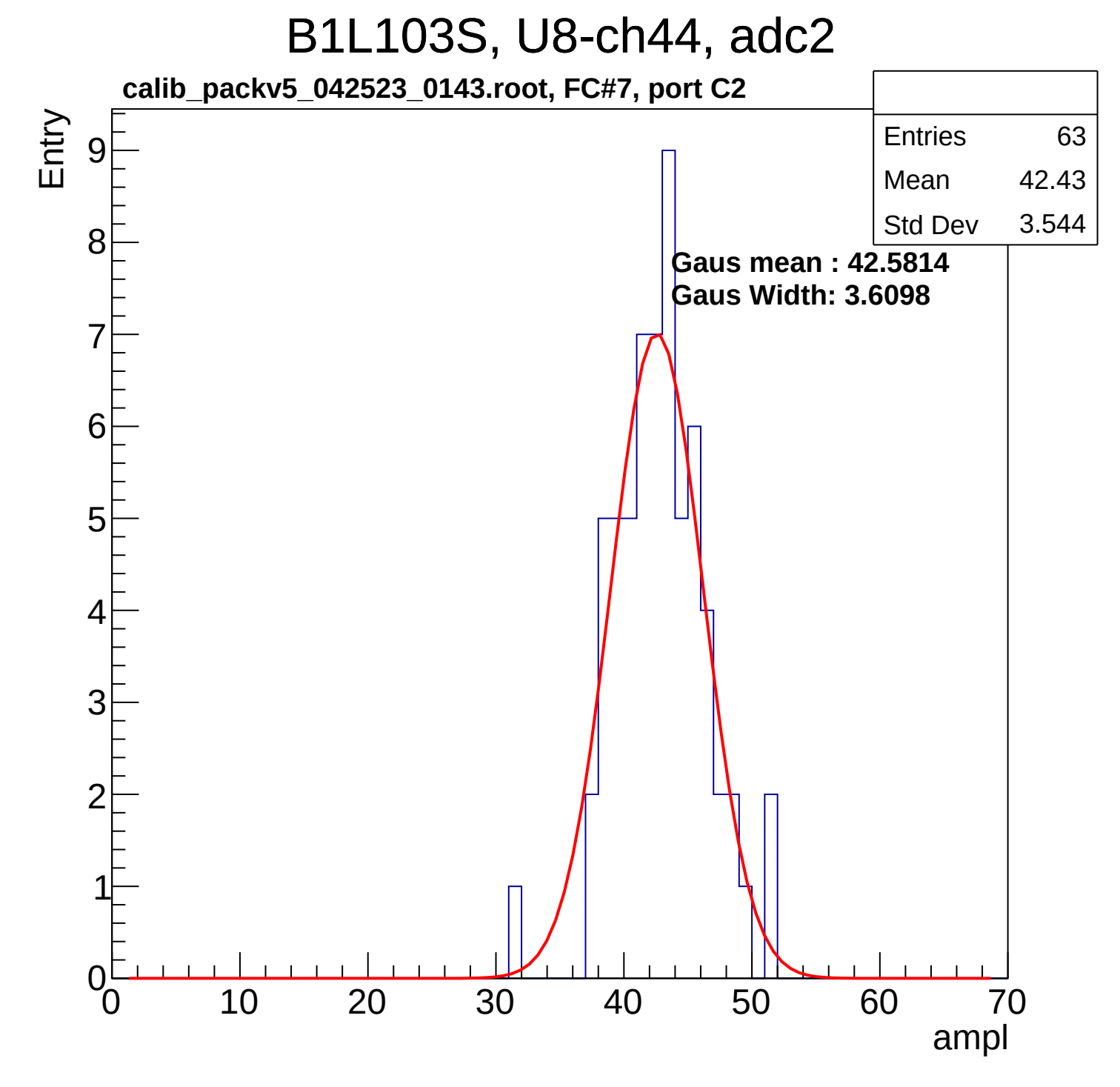

B1L103S, U8-ch43, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 33
Mean 59.97
Std Dev 2.443
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

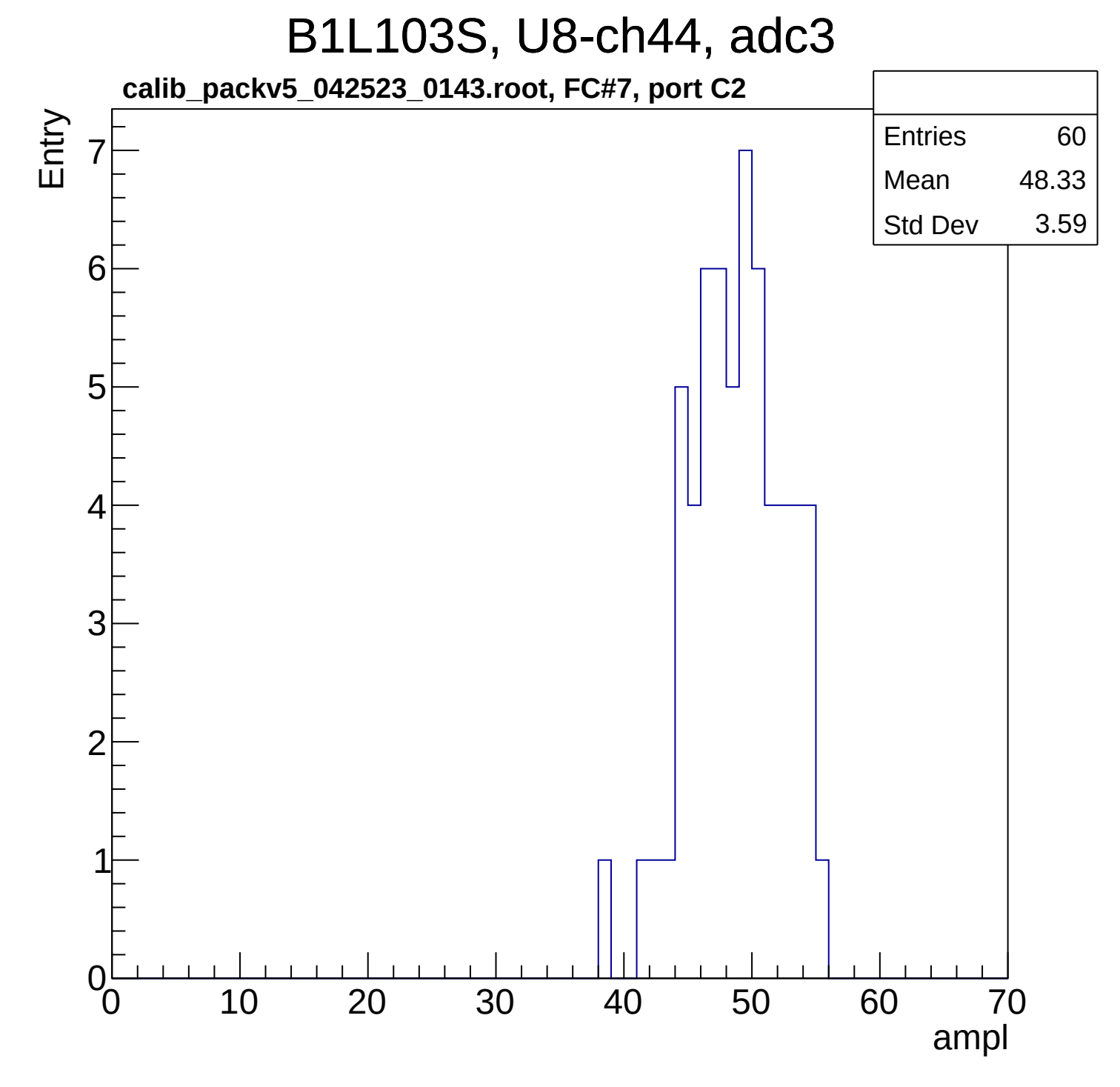

B1L103S, U8-ch43, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 10
Mean 62.1
Std Dev 1.221
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

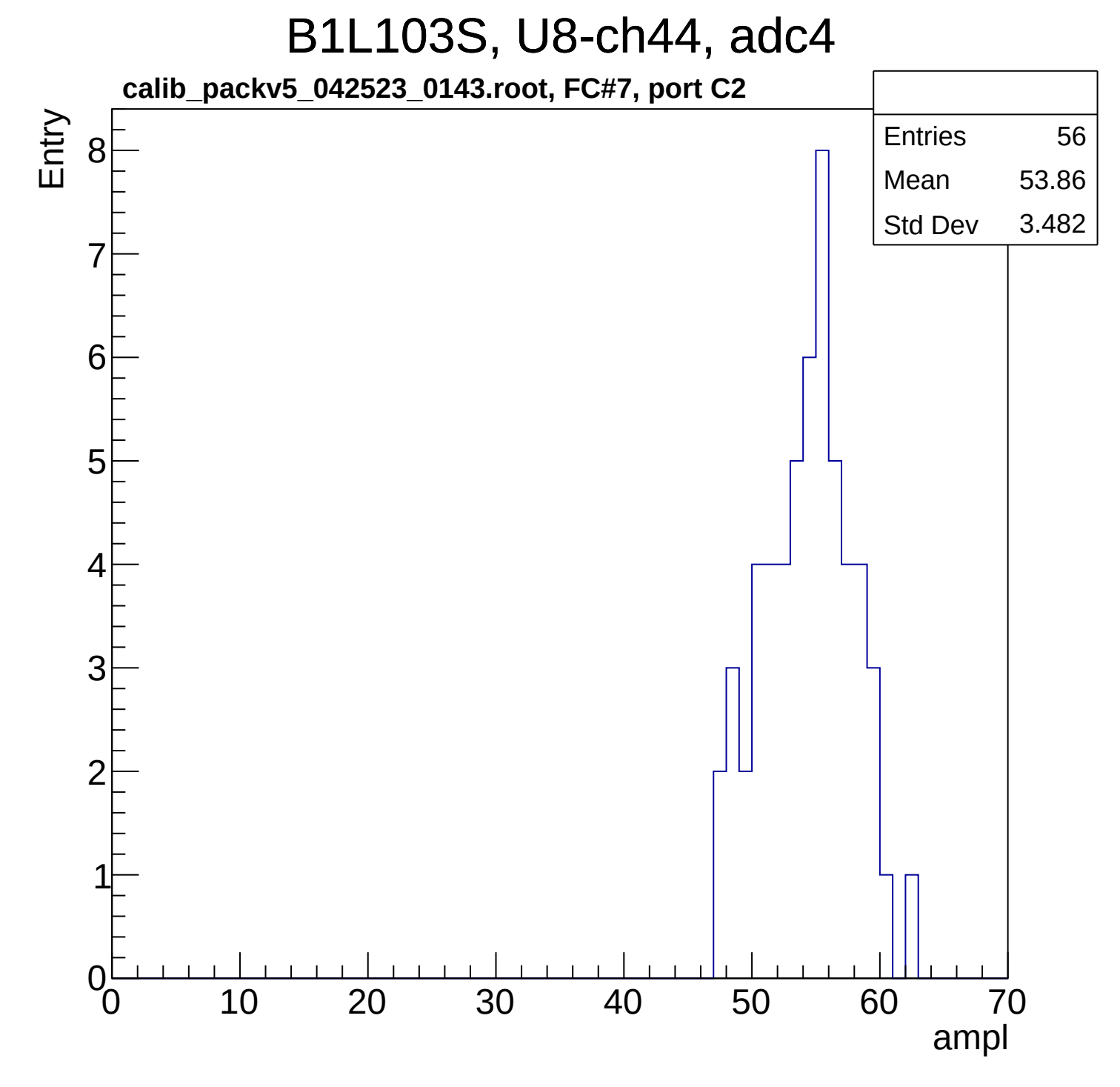

B1L103S, U8-ch43, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 7.333
Std Dev 10.37
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

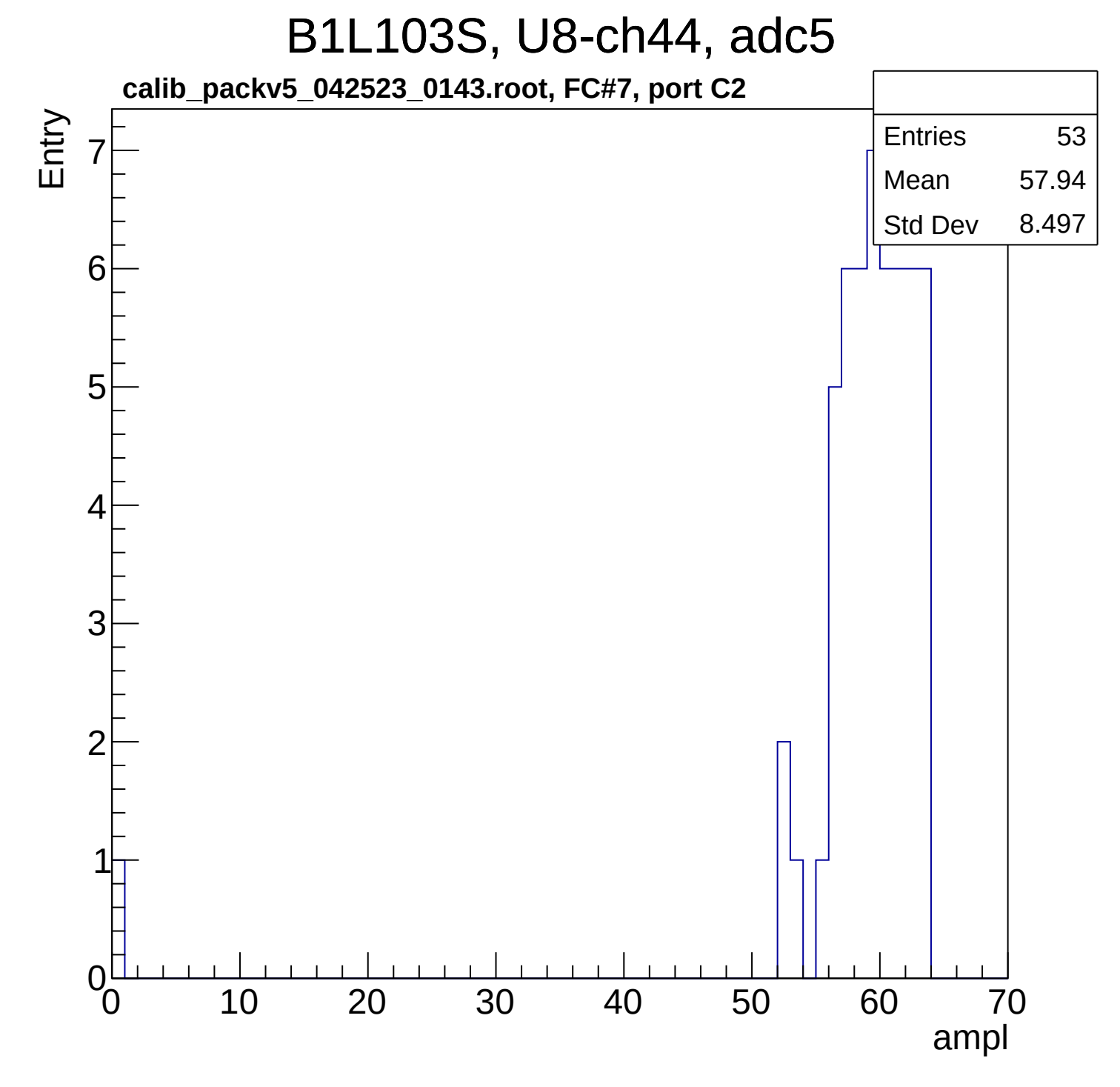

B1L103S, U8-ch44, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 28.08
Std Dev 2.906
Gaus mean : 29.2857
Gaus Width: 3.6495
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

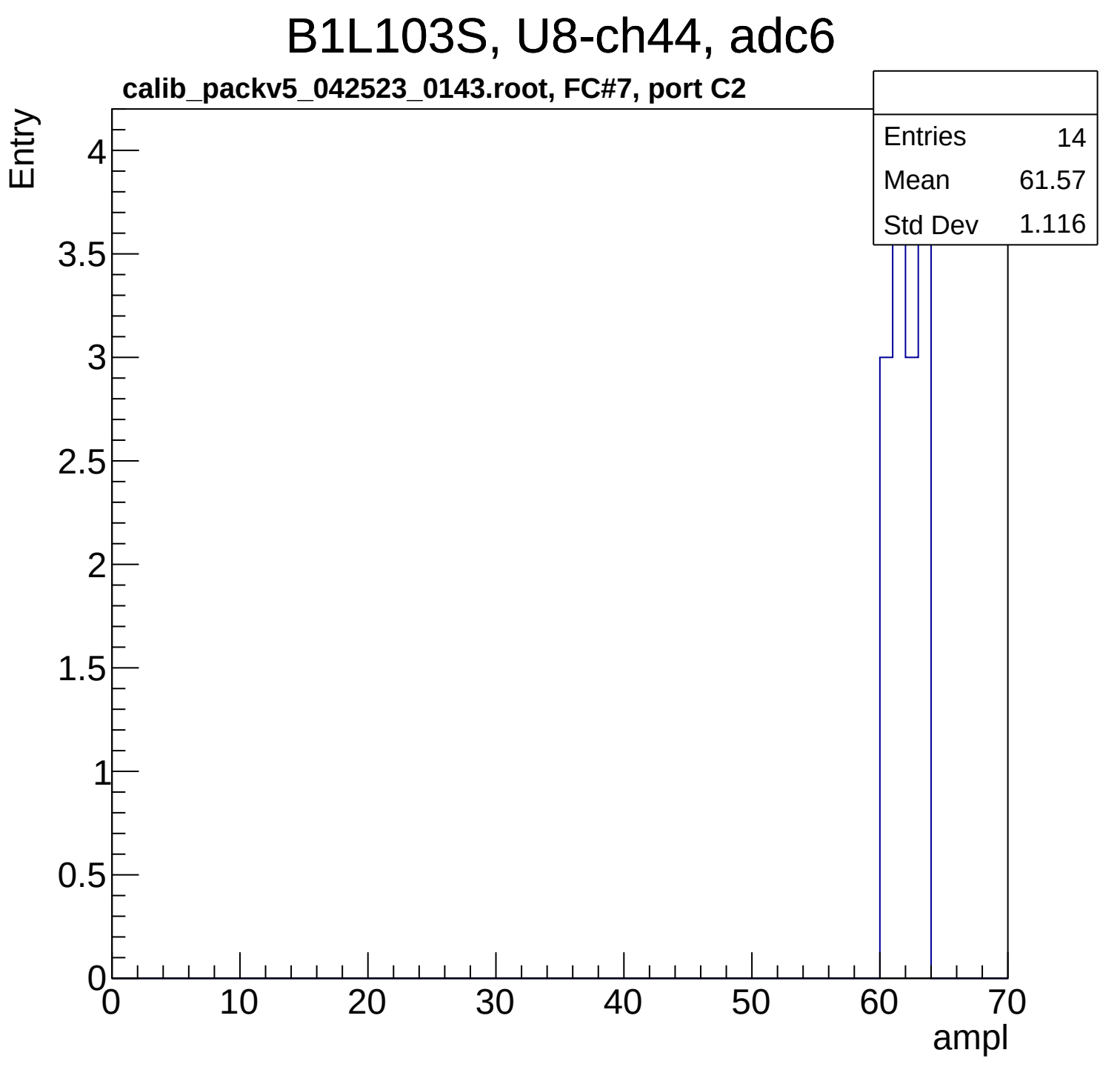

B1L103S, U8-ch44, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 81
Mean 34.88
Std Dev 3.646
Gaus mean : 35.5051
Gaus Width: 3.8548
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

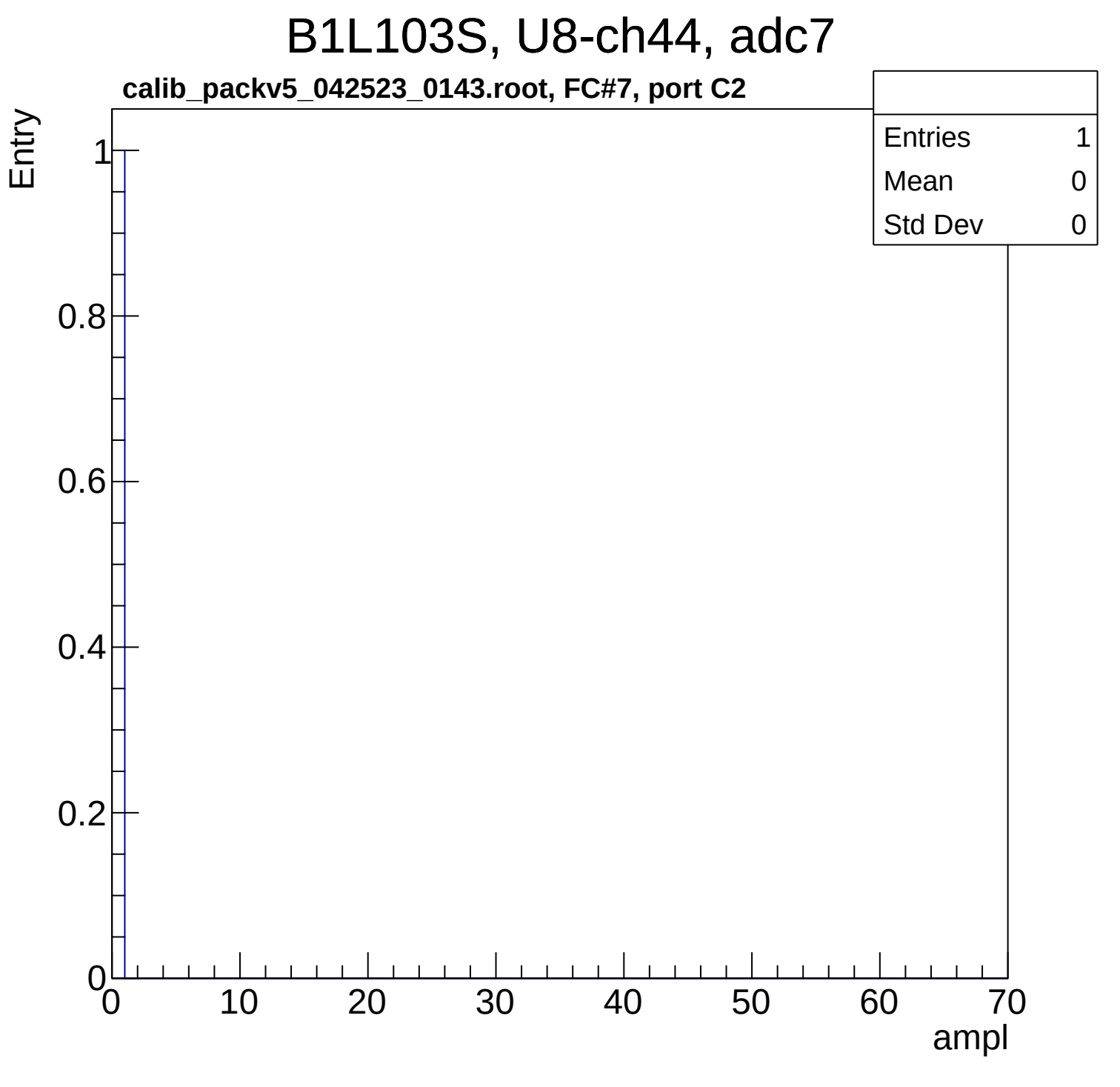

B1L103S, U8-ch44, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 42.43
Std Dev 3.544
Gaus mean : 42.5814
Gaus Width: 3.6098
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

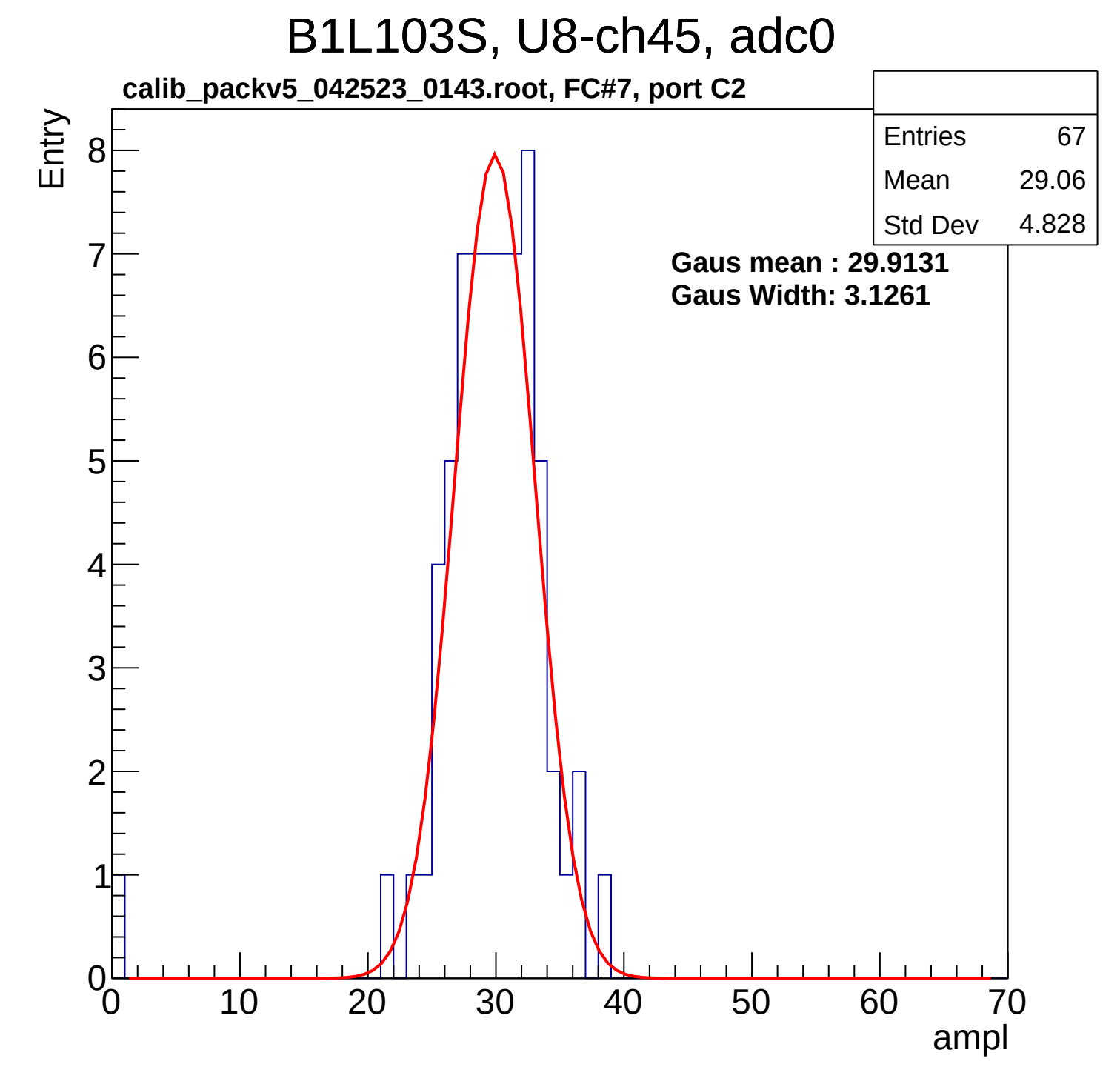

B1L103S, U8-ch44, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 48.33
Std Dev 3.59
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

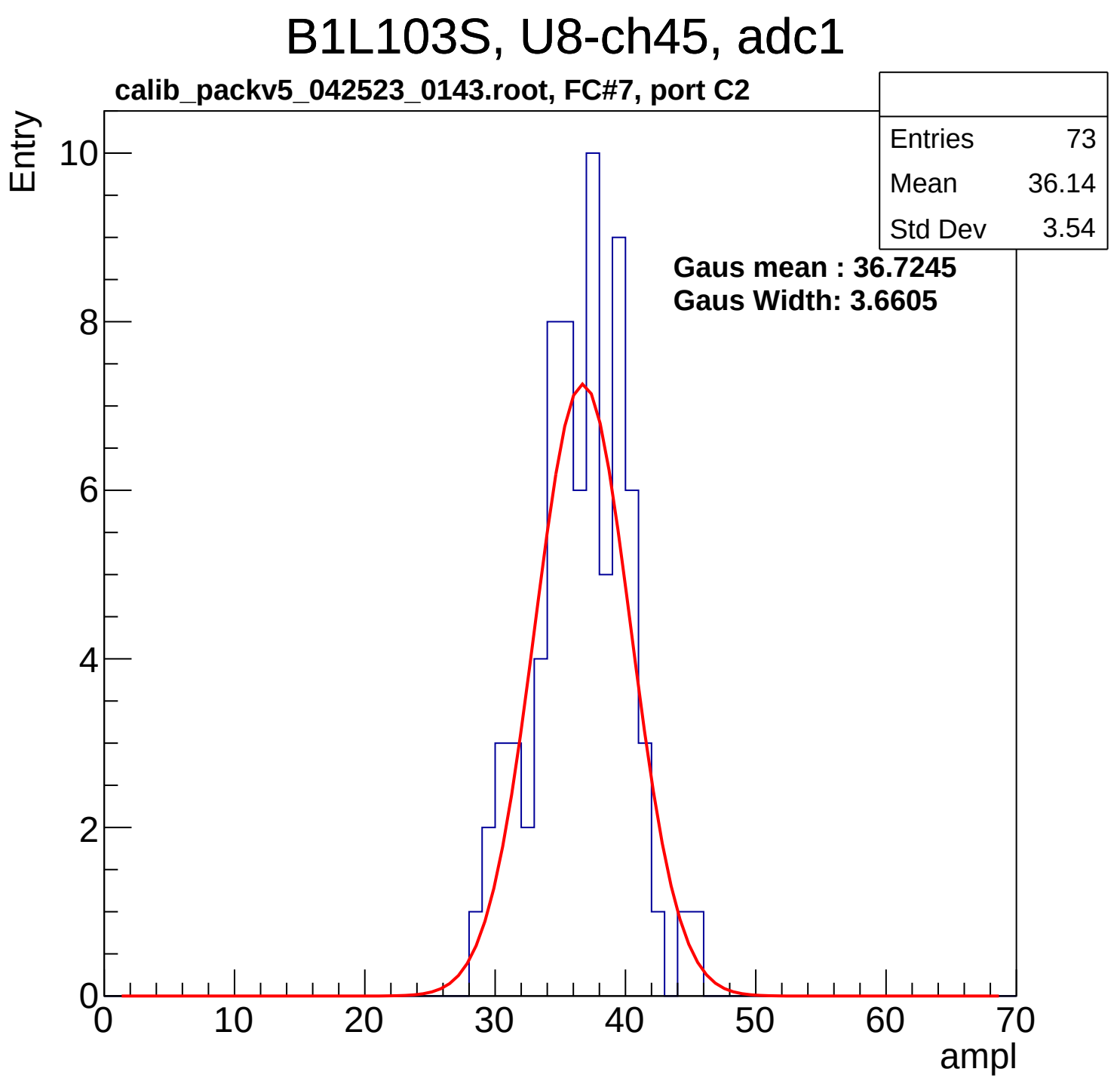

B1L103S, U8-ch44, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 53.86
Std Dev 3.482
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

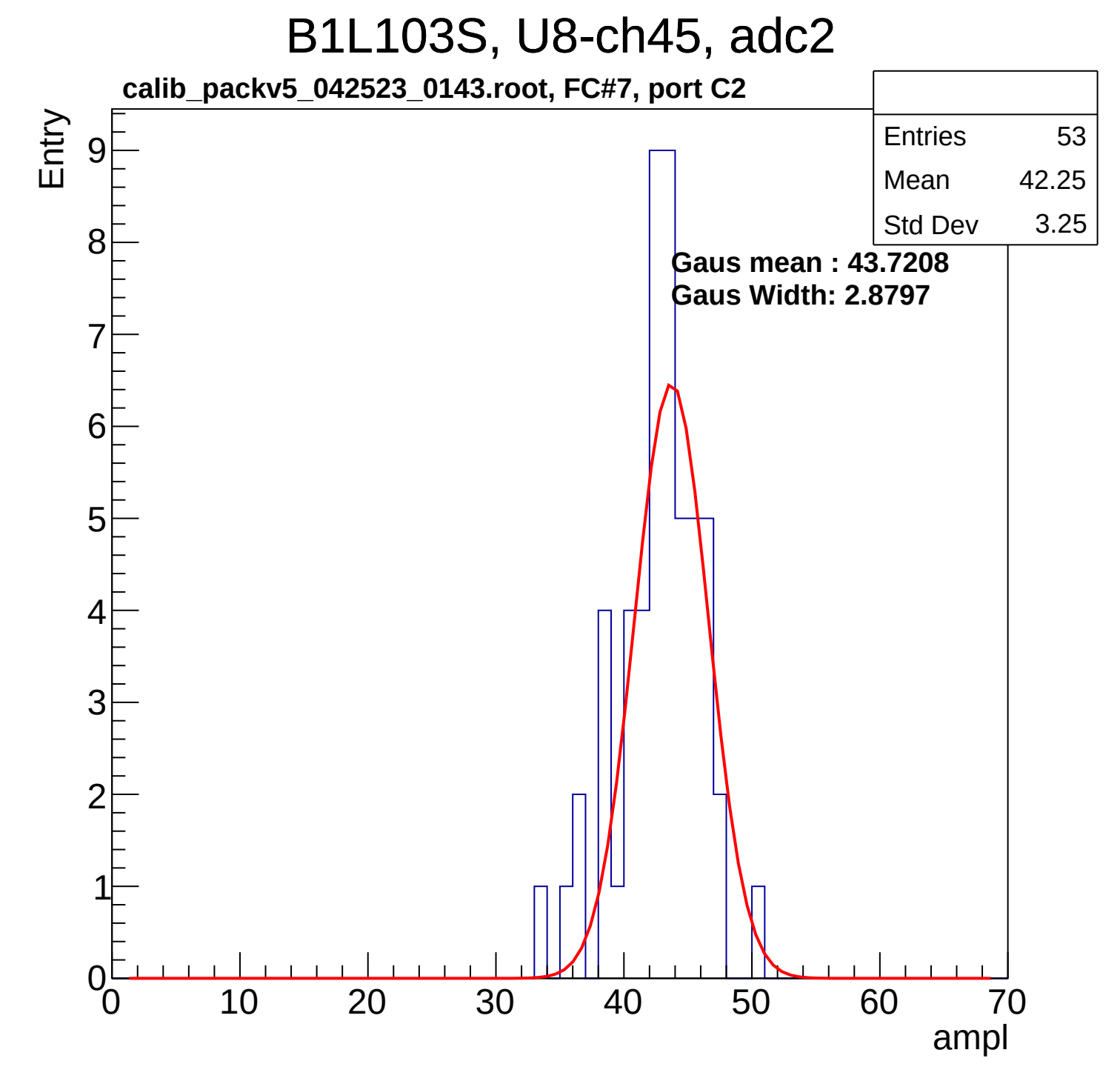

B1L103S, U8-ch44, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 57.94
Std Dev 8.497
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

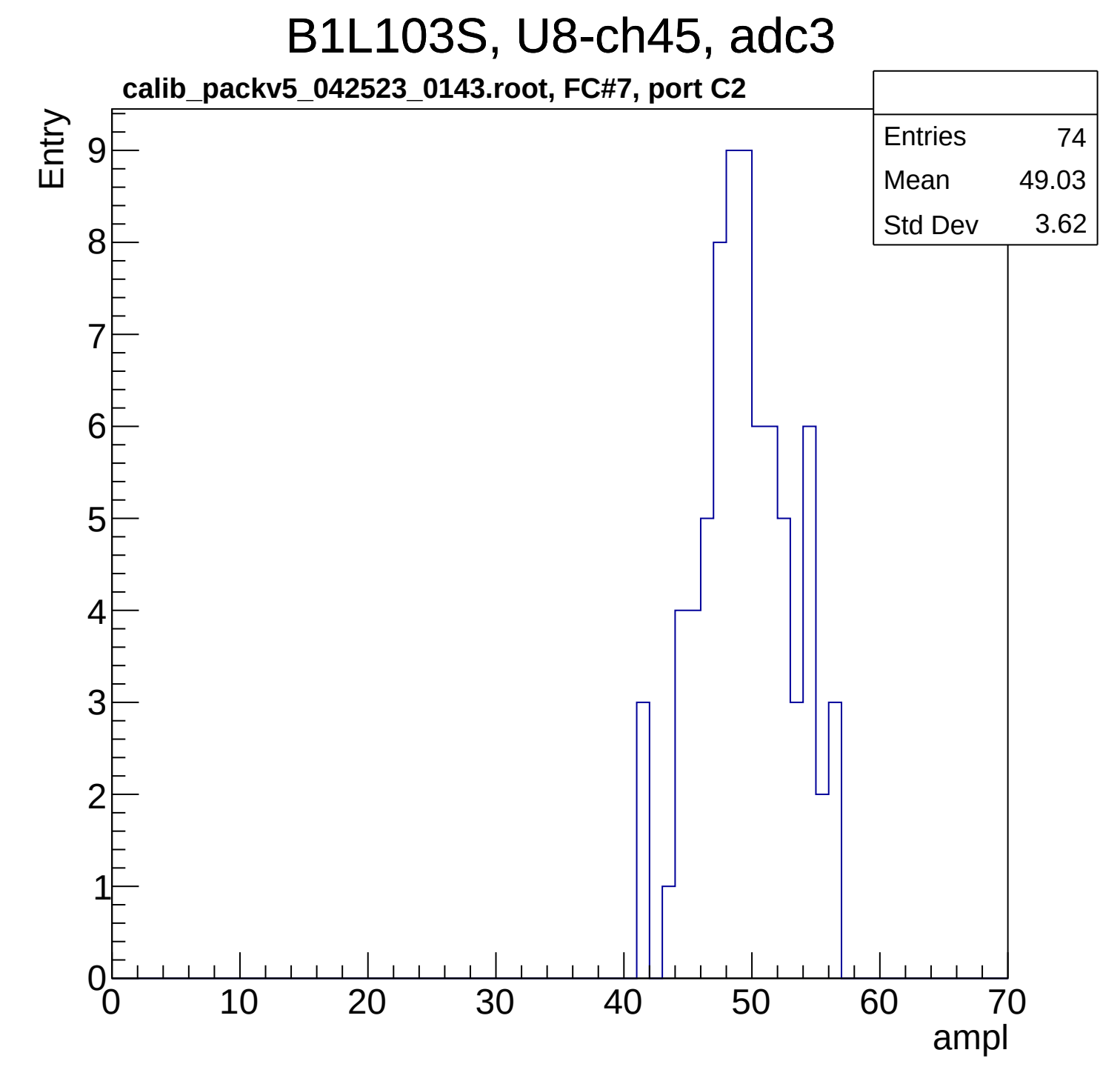

B1L103S, U8-ch44, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 14
Mean 61.57
Std Dev 1.116
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

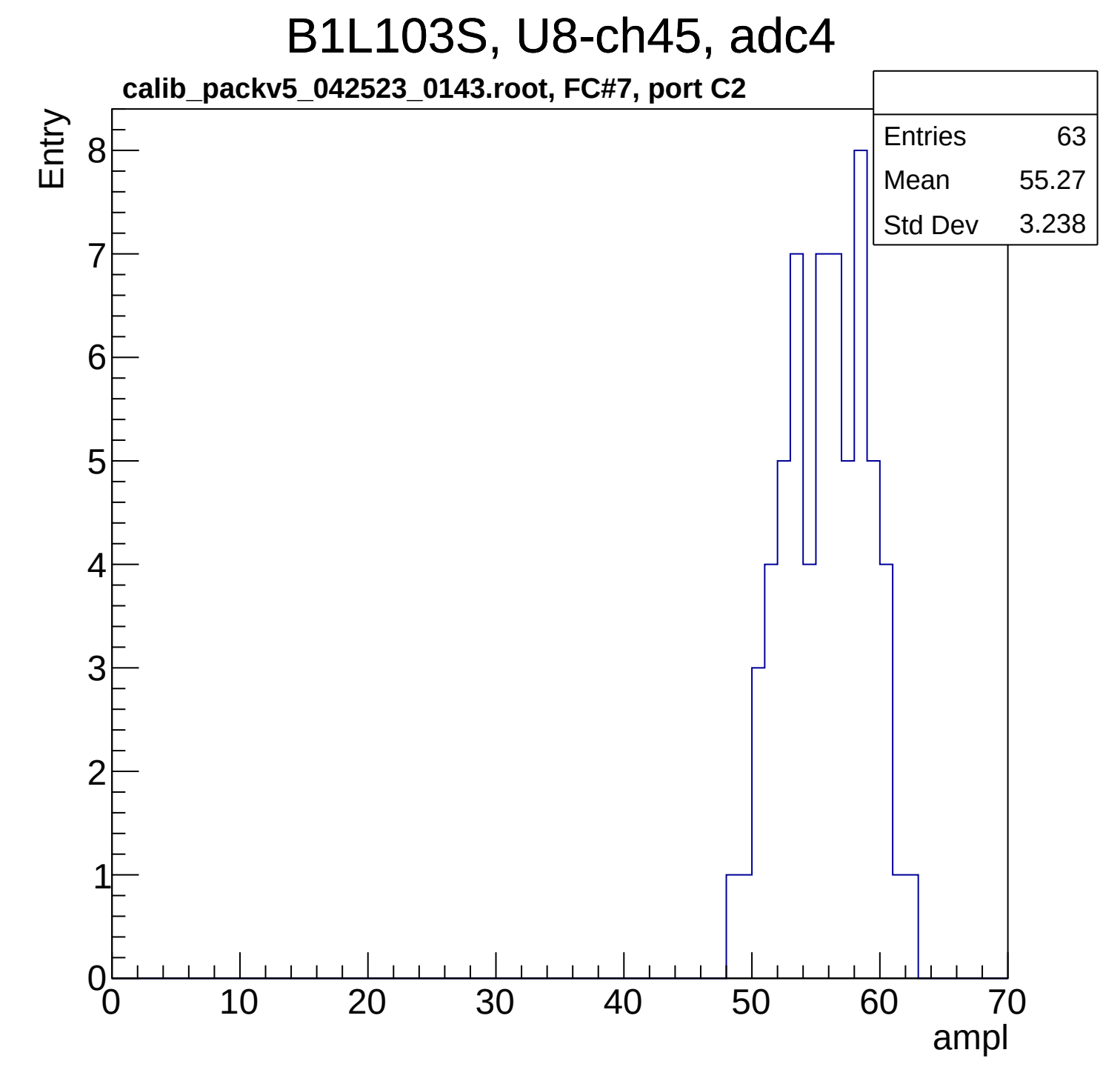

B1L103S, U8-ch44, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

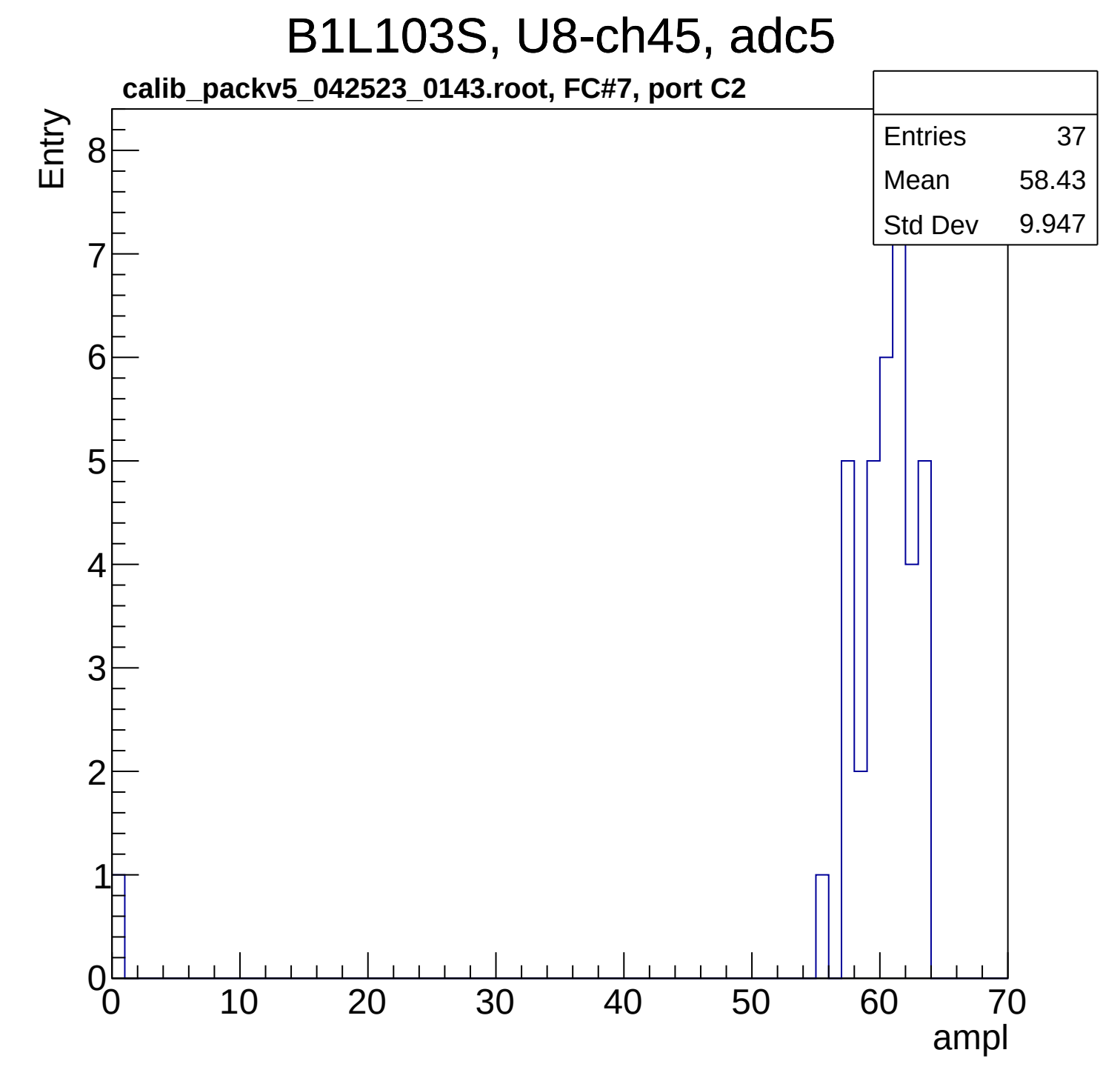

B1L103S, U8-ch45, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 29.06
Std Dev 4.828
Gaus mean : 29.9131
Gaus Width: 3.1261
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

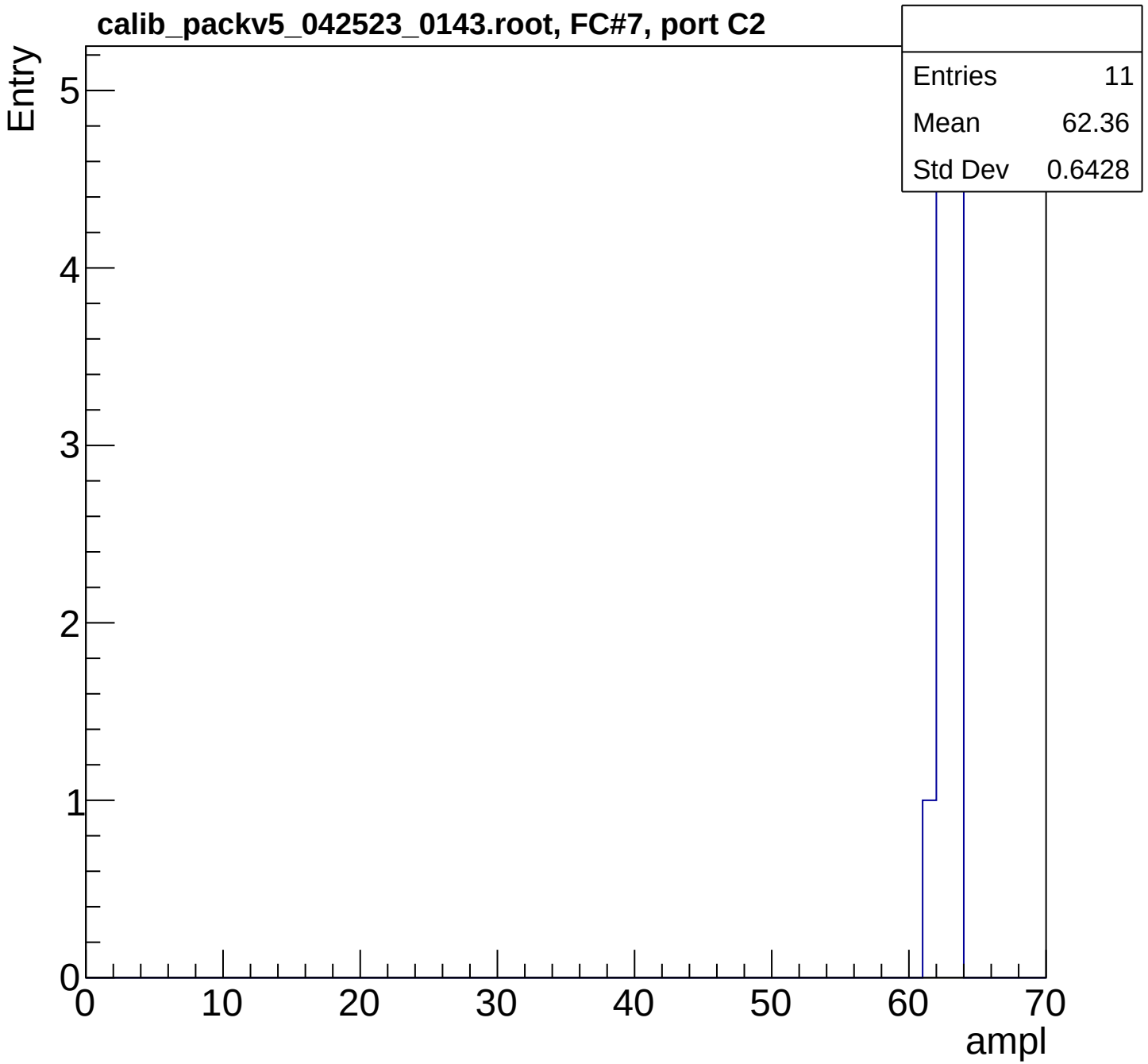

B1L103S, U8-ch45, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 36.14
Std Dev 3.54
Gaus mean : 36.7245
Gaus Width: 3.6605
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

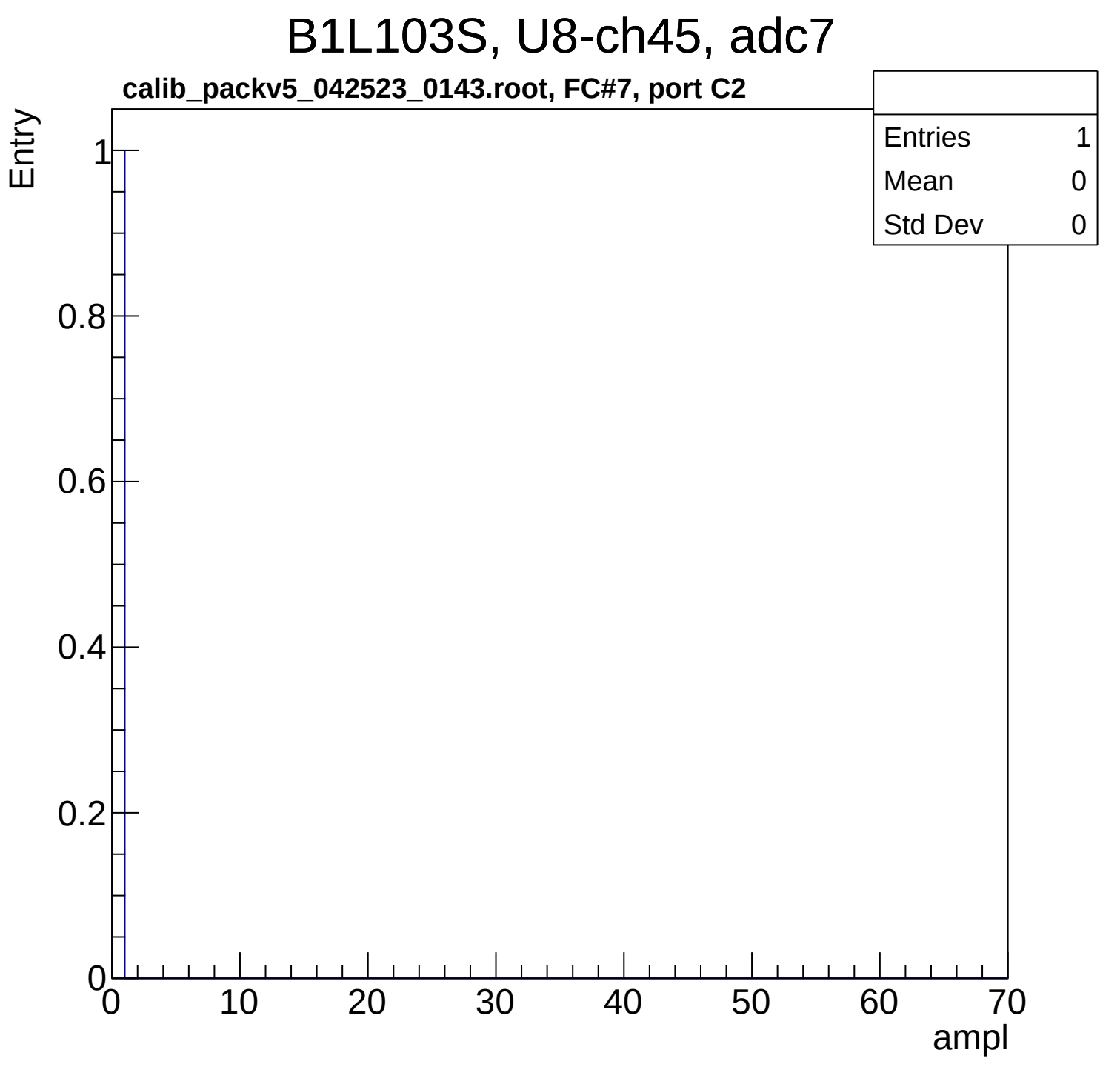

B1L103S, U8-ch45, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 42.25
Std Dev 3.25
Gaus mean : 43.7208
Gaus Width: 2.8797
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

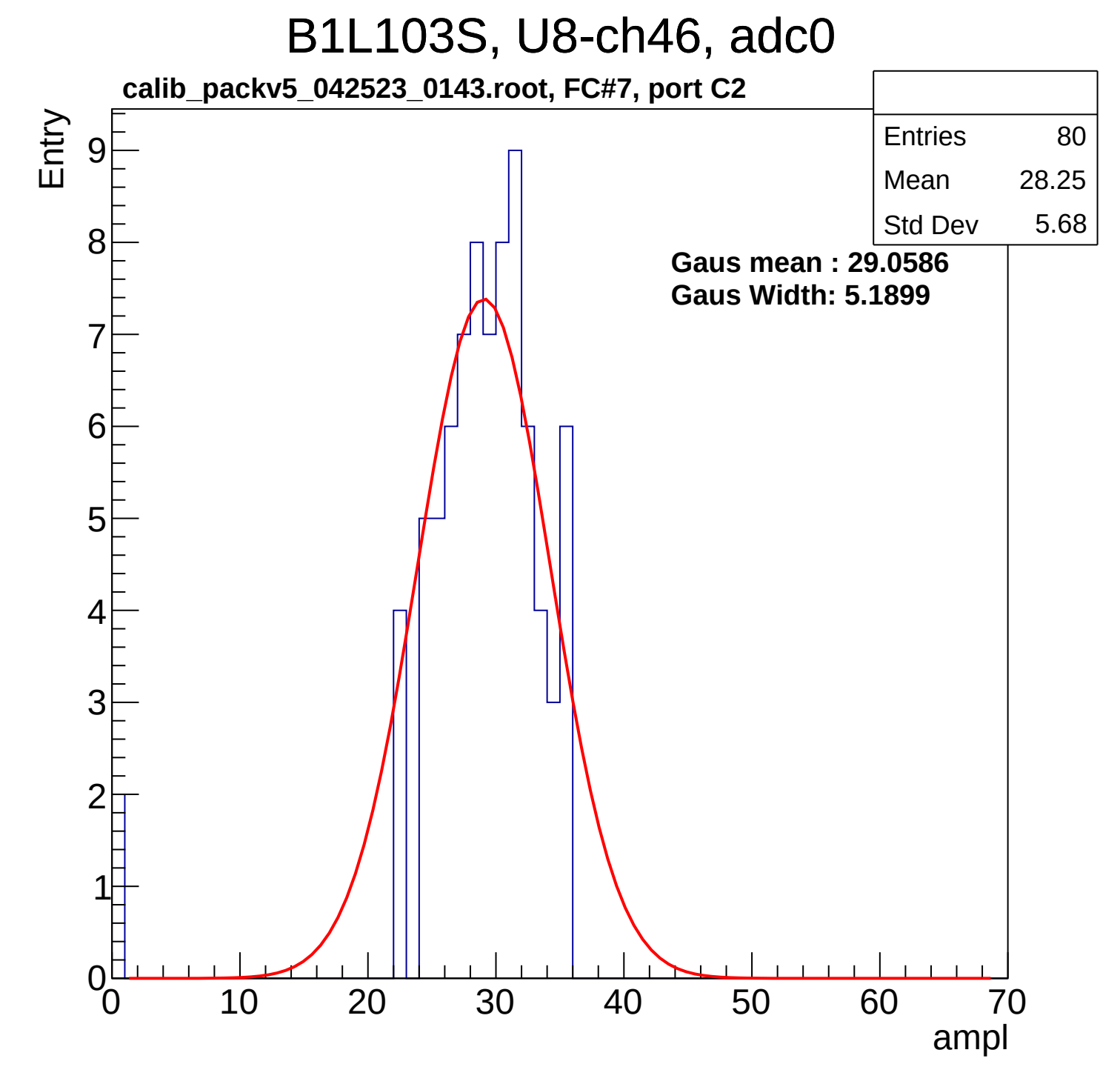

B1L103S, U8-ch45, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 49.03
Std Dev 3.62
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

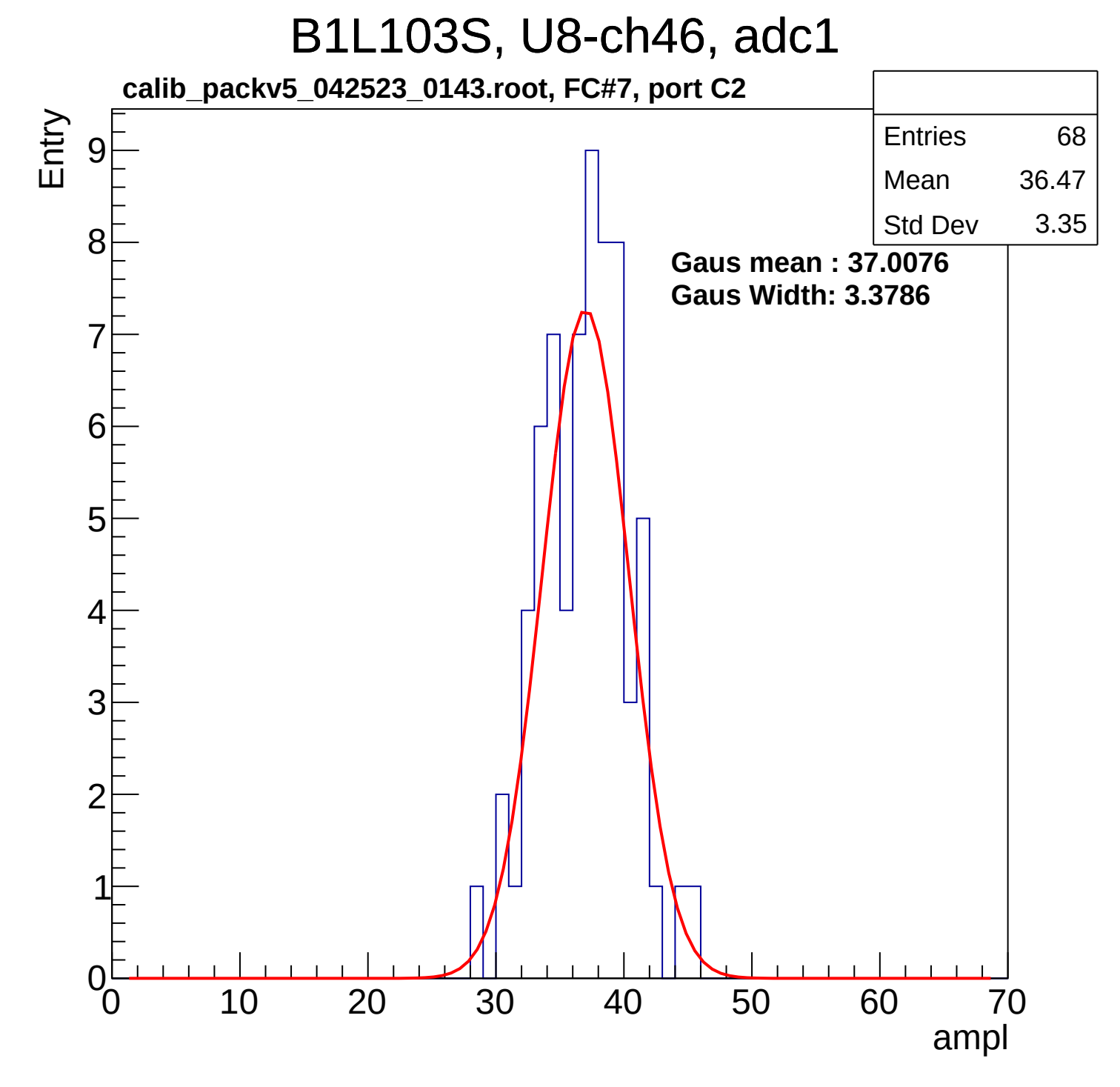

B1L103S, U8-ch45, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 55.27
Std Dev 3.238
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

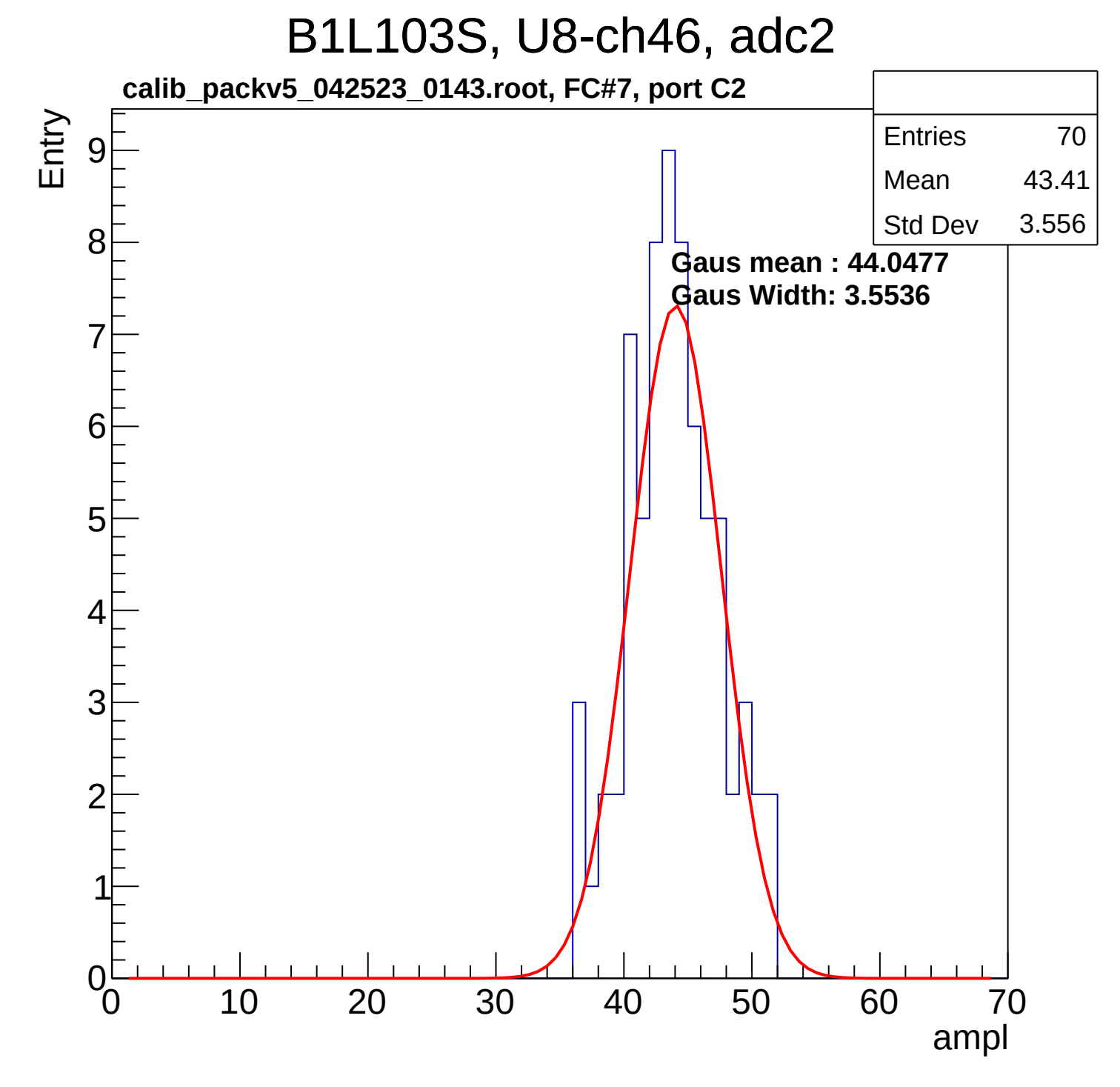

B1L103S, U8-ch45, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 37
Mean 58.43
Std Dev 9.947
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

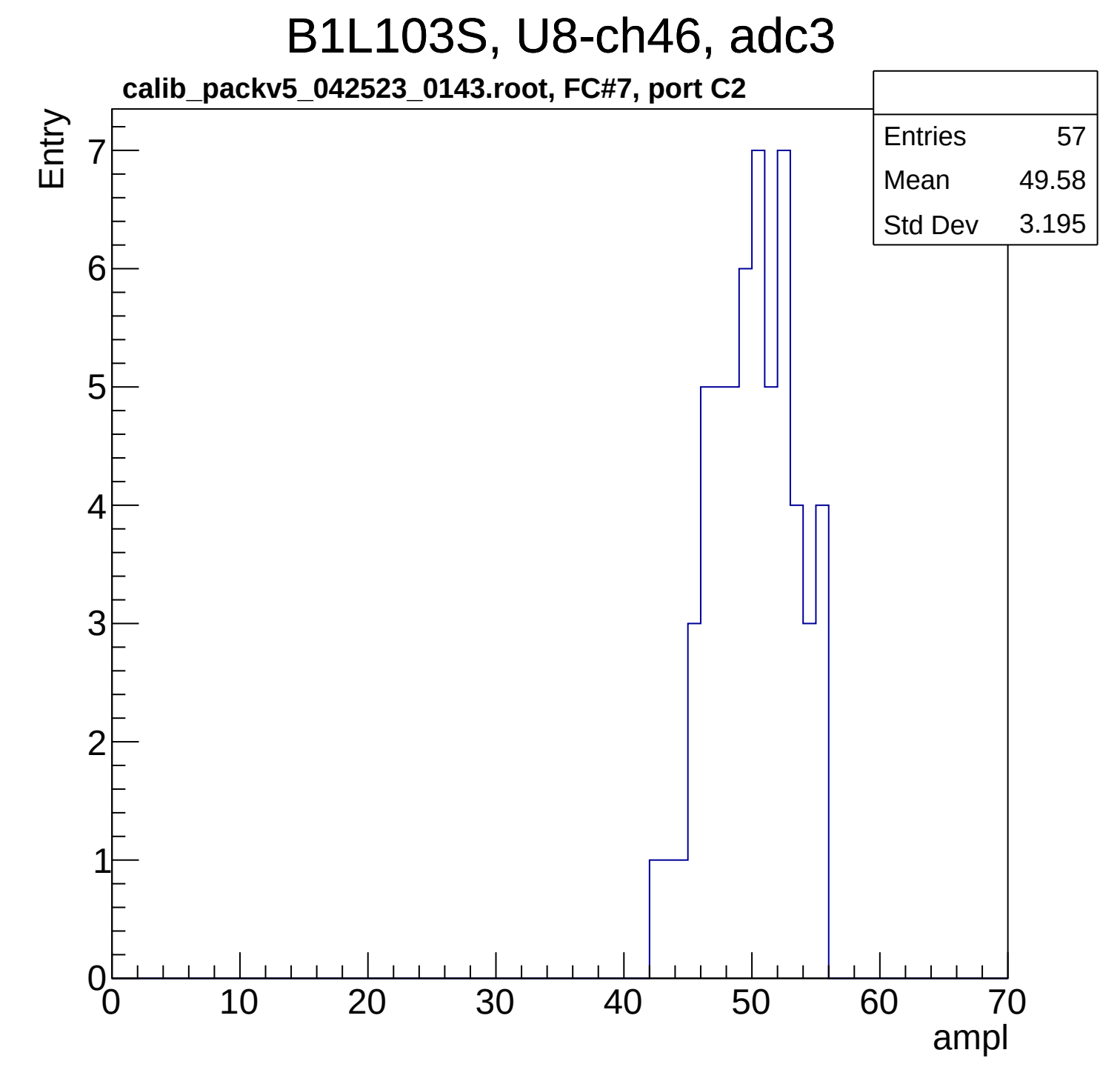

B1L103S, U8-ch45, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 11
Mean 62.36
Std Dev 0.6428
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

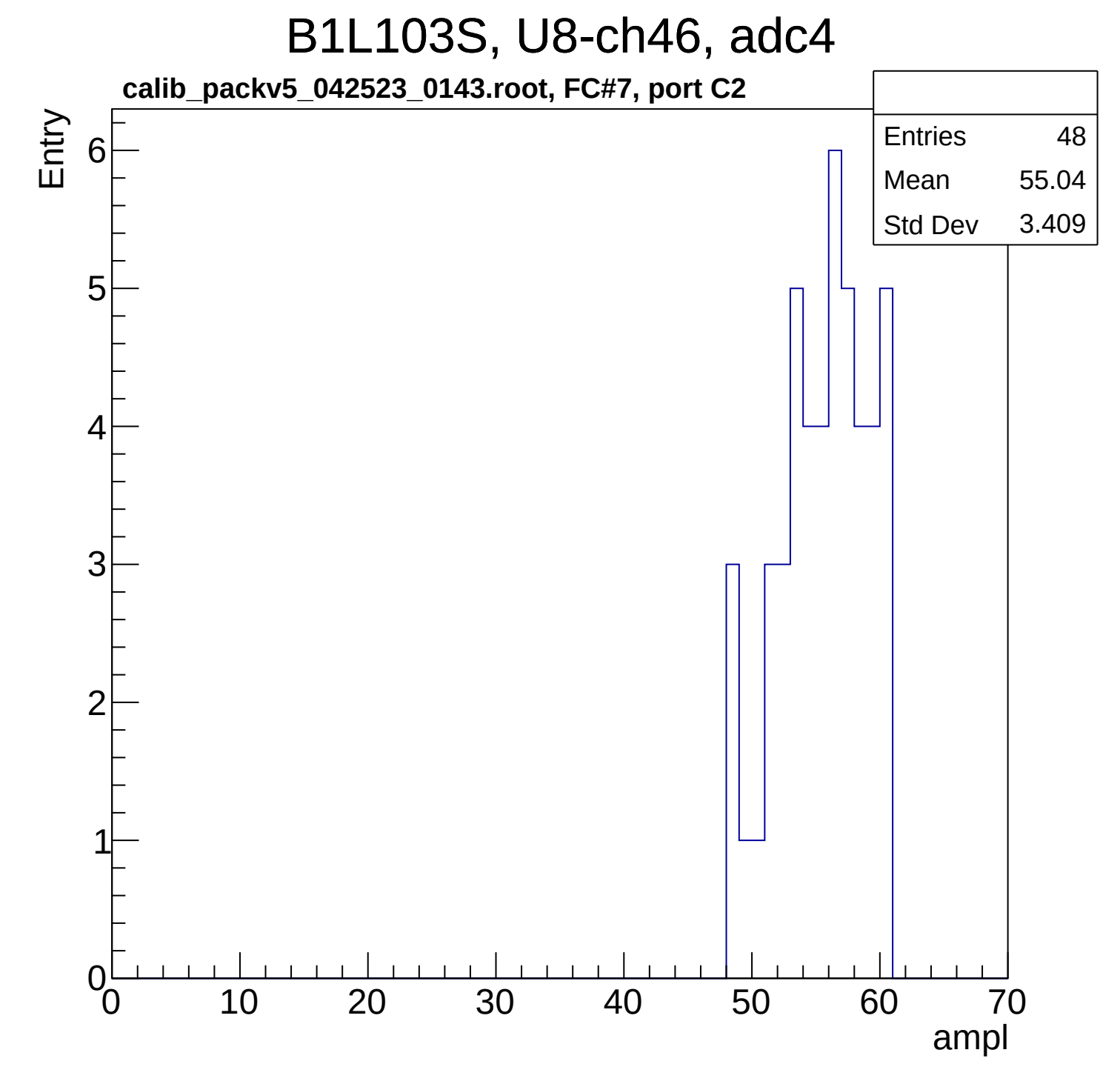

B1L103S, U8-ch45, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

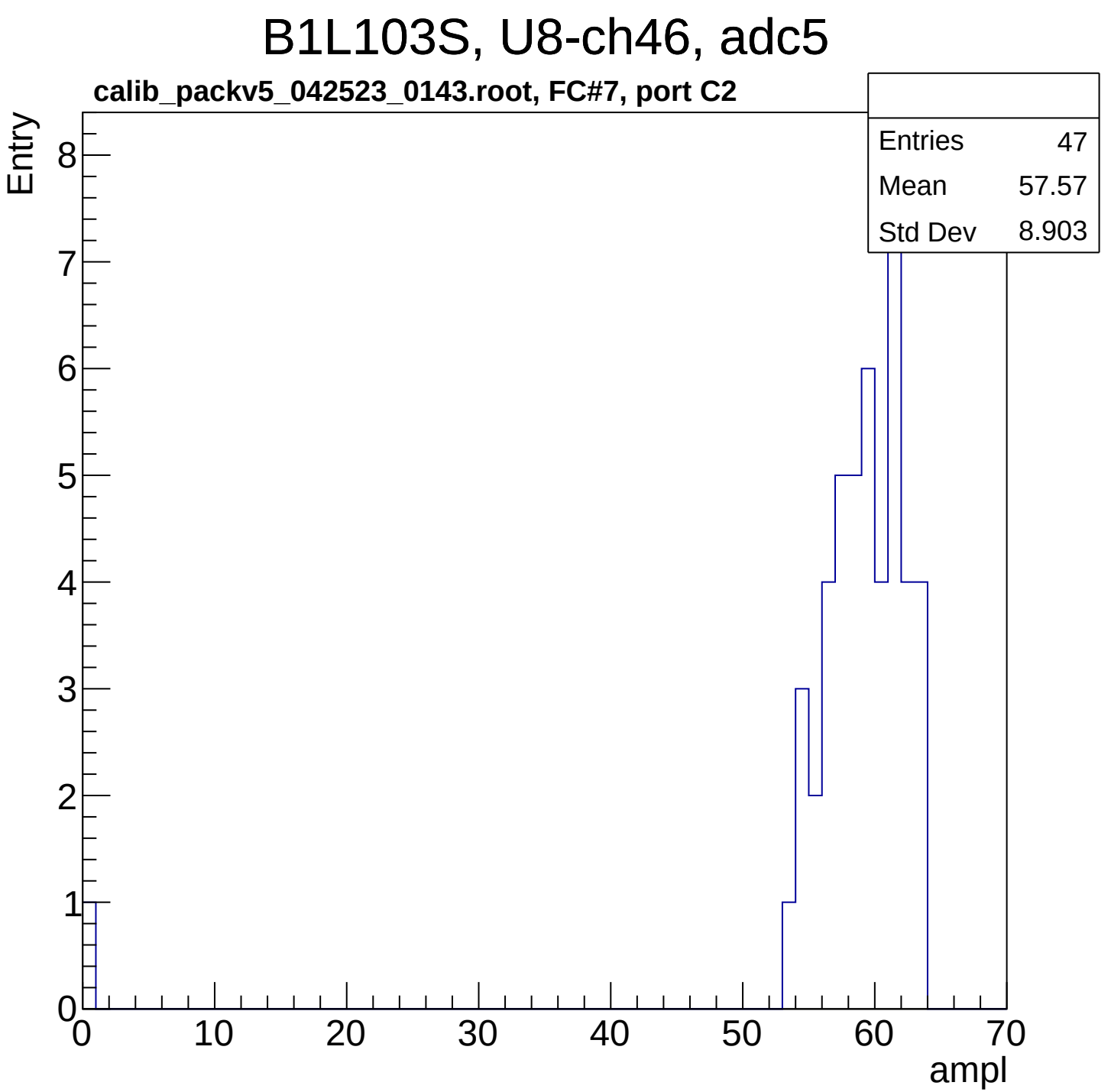

B1L103S, U8-ch46, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 80
Mean 28.25
Std Dev 5.68
Gaus mean : 29.0586
Gaus Width: 5.1899
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

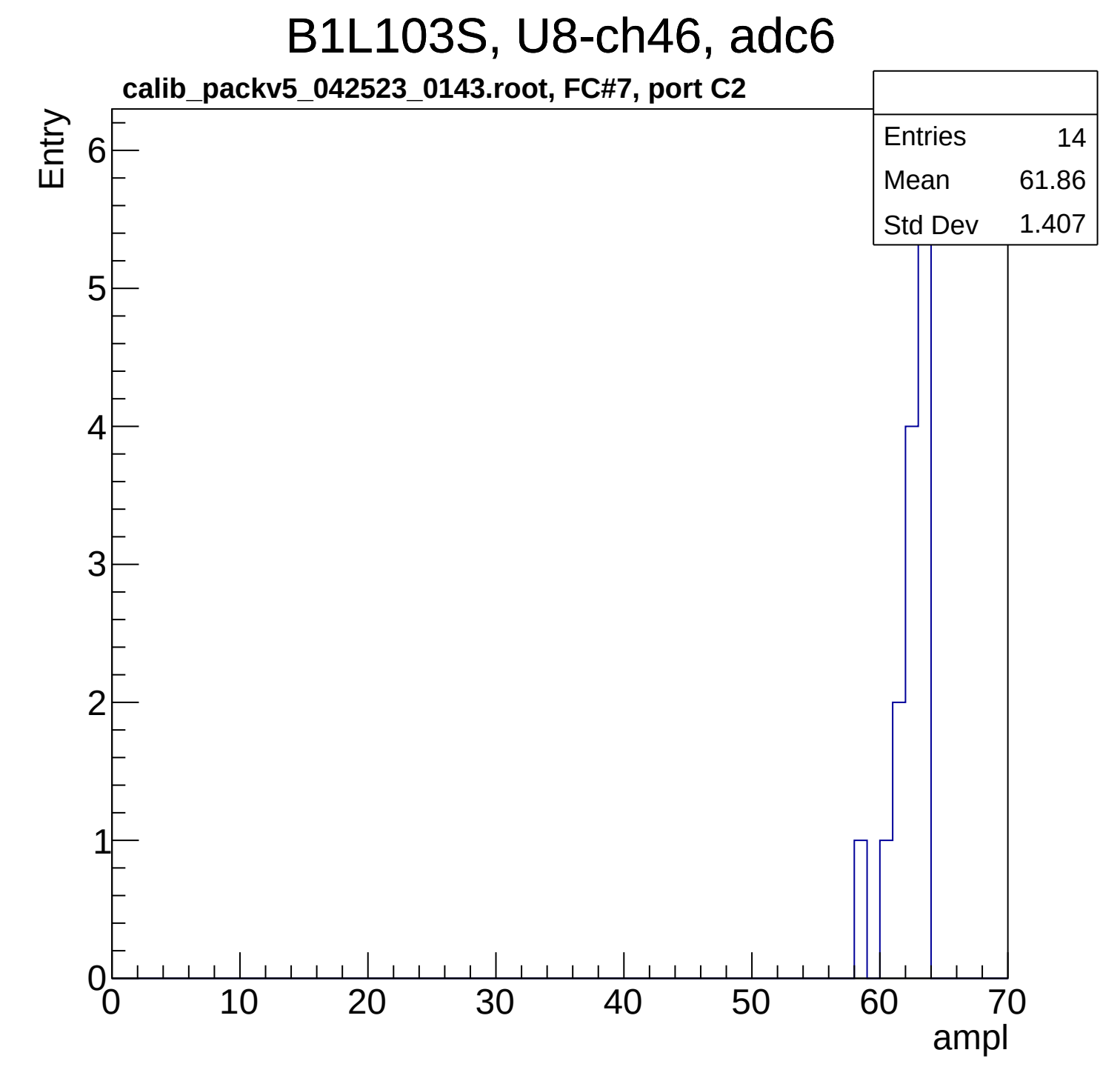

B1L103S, U8-ch46, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 36.47
Std Dev 3.35
Gaus mean : 37.0076
Gaus Width: 3.3786
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

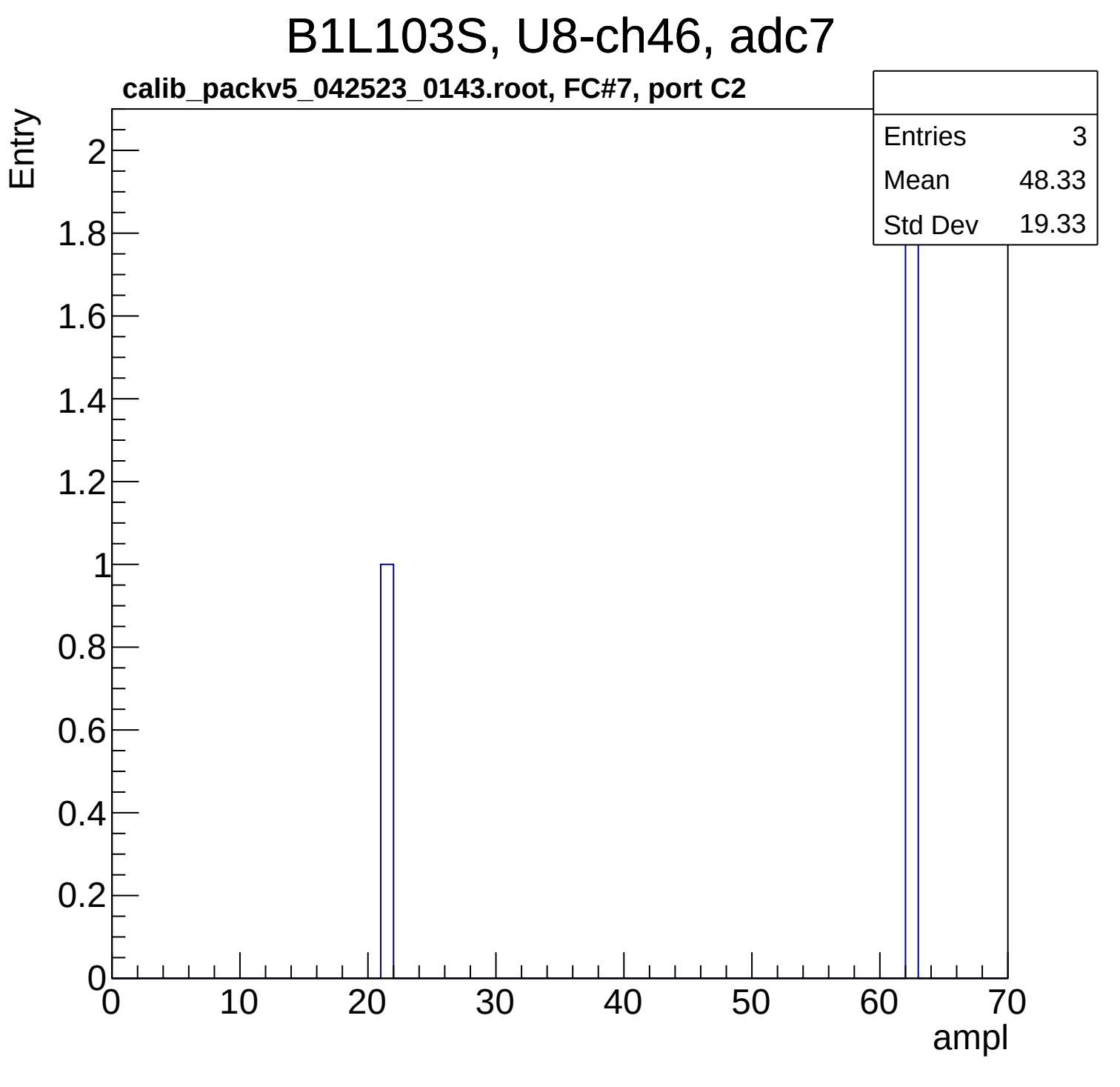

B1L103S, U8-ch46, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 43.41
Std Dev 3.556
Gaus mean : 44.0477
Gaus Width: 3.5536
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

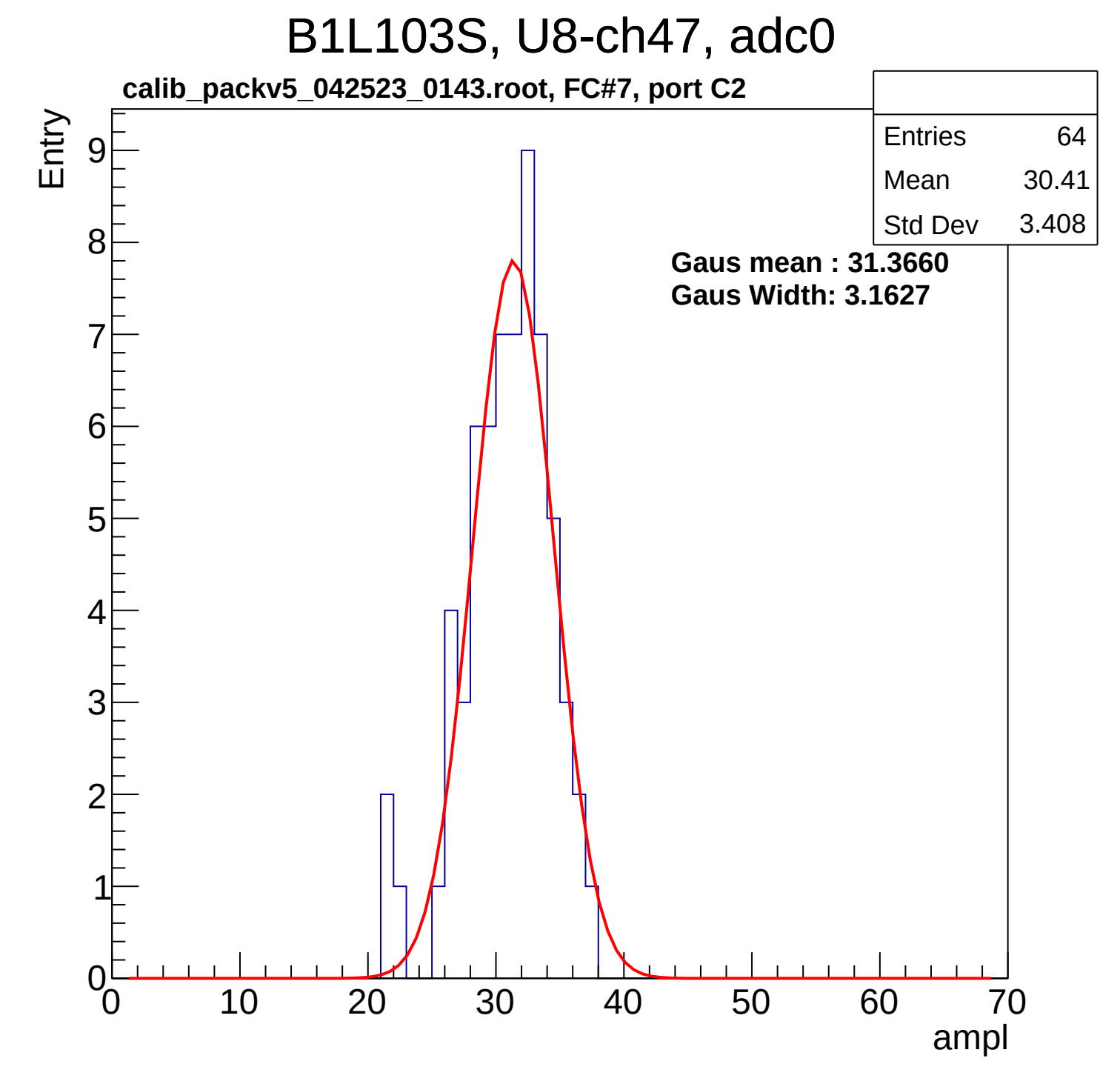

B1L103S, U8-ch46, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 49.58
Std Dev 3.195
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

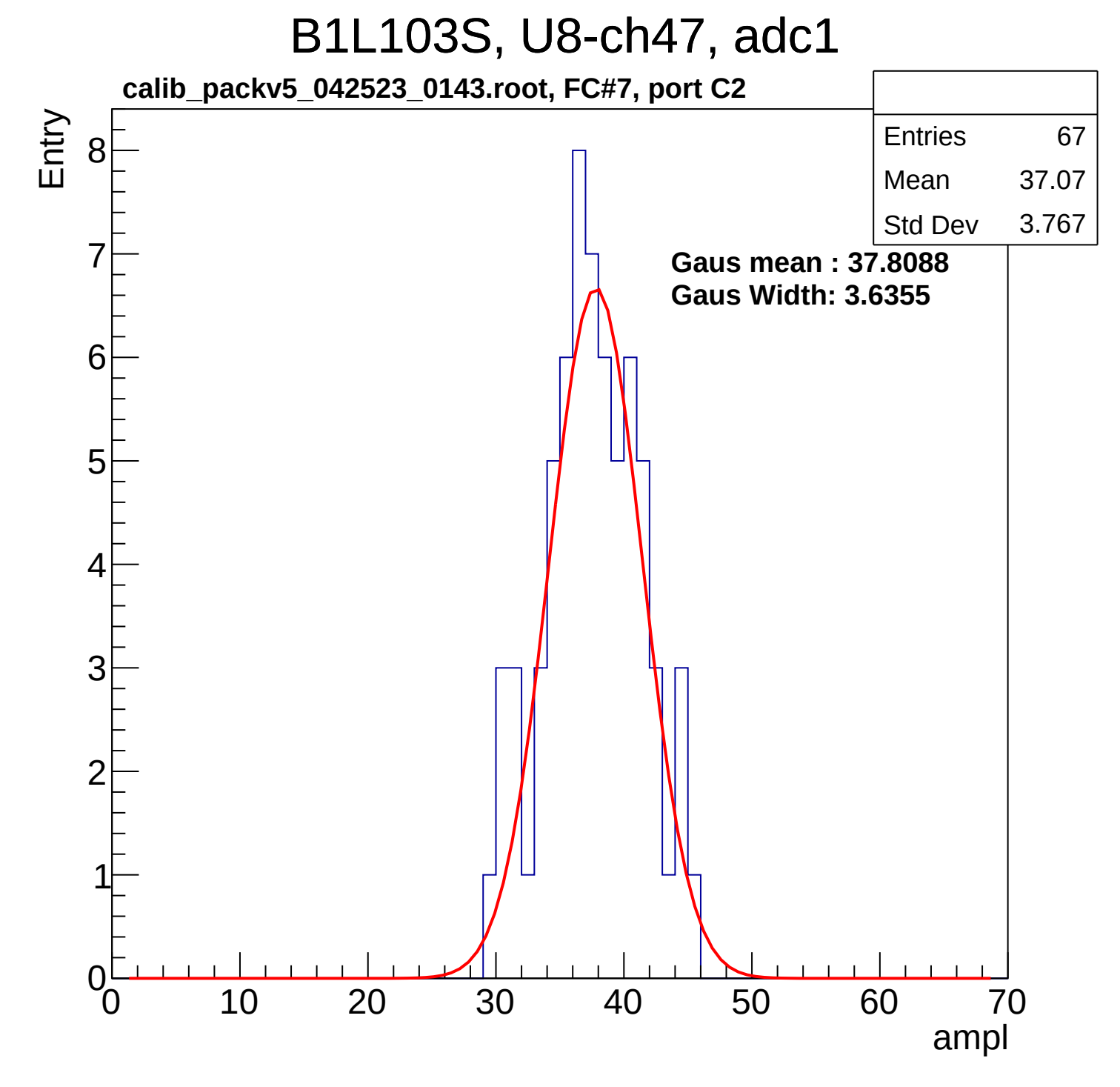

B1L103S, U8-ch46, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 55.04
Std Dev 3.409
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

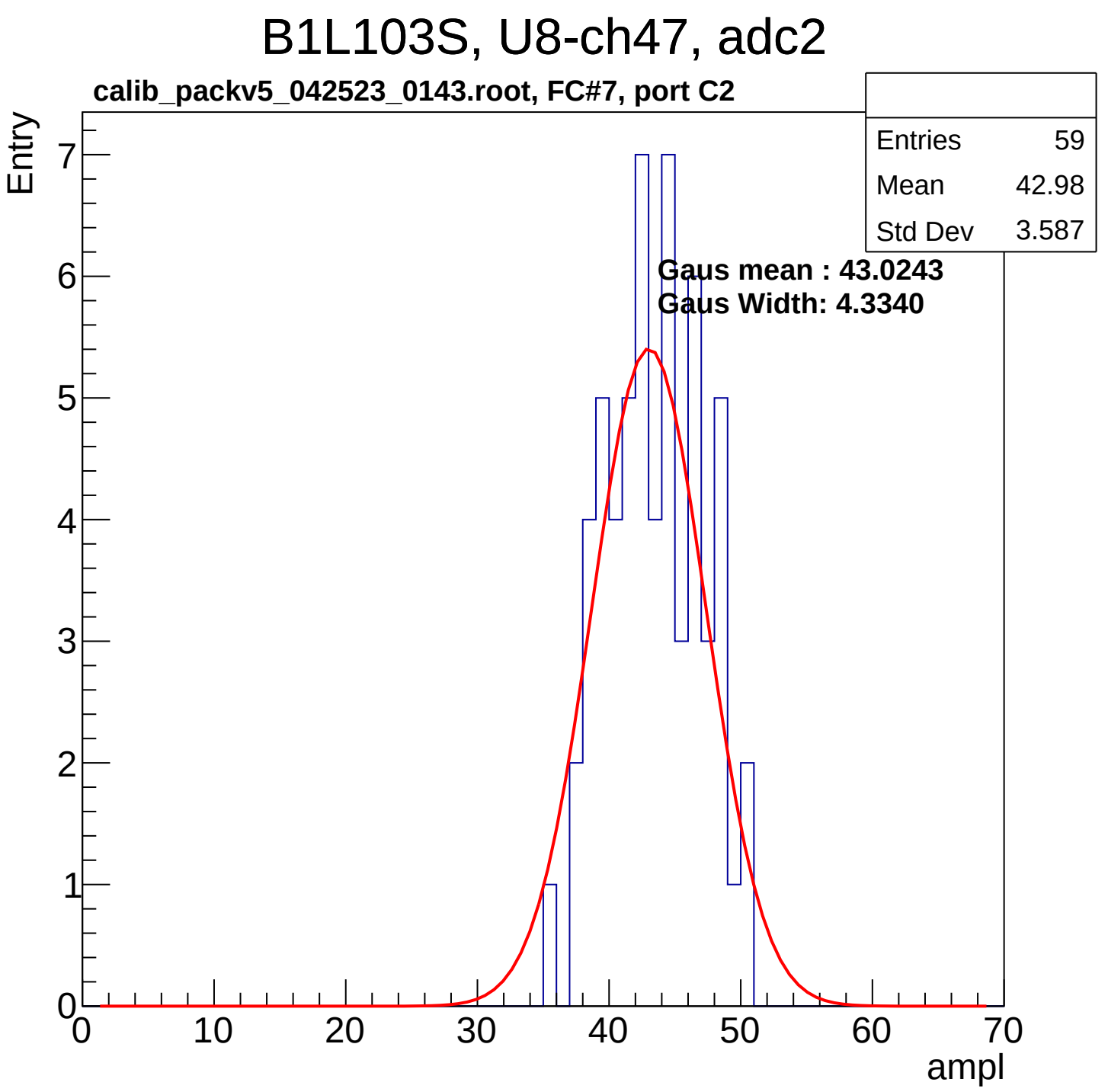

B1L103S, U8-ch46, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 57.57
Std Dev 8.903
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

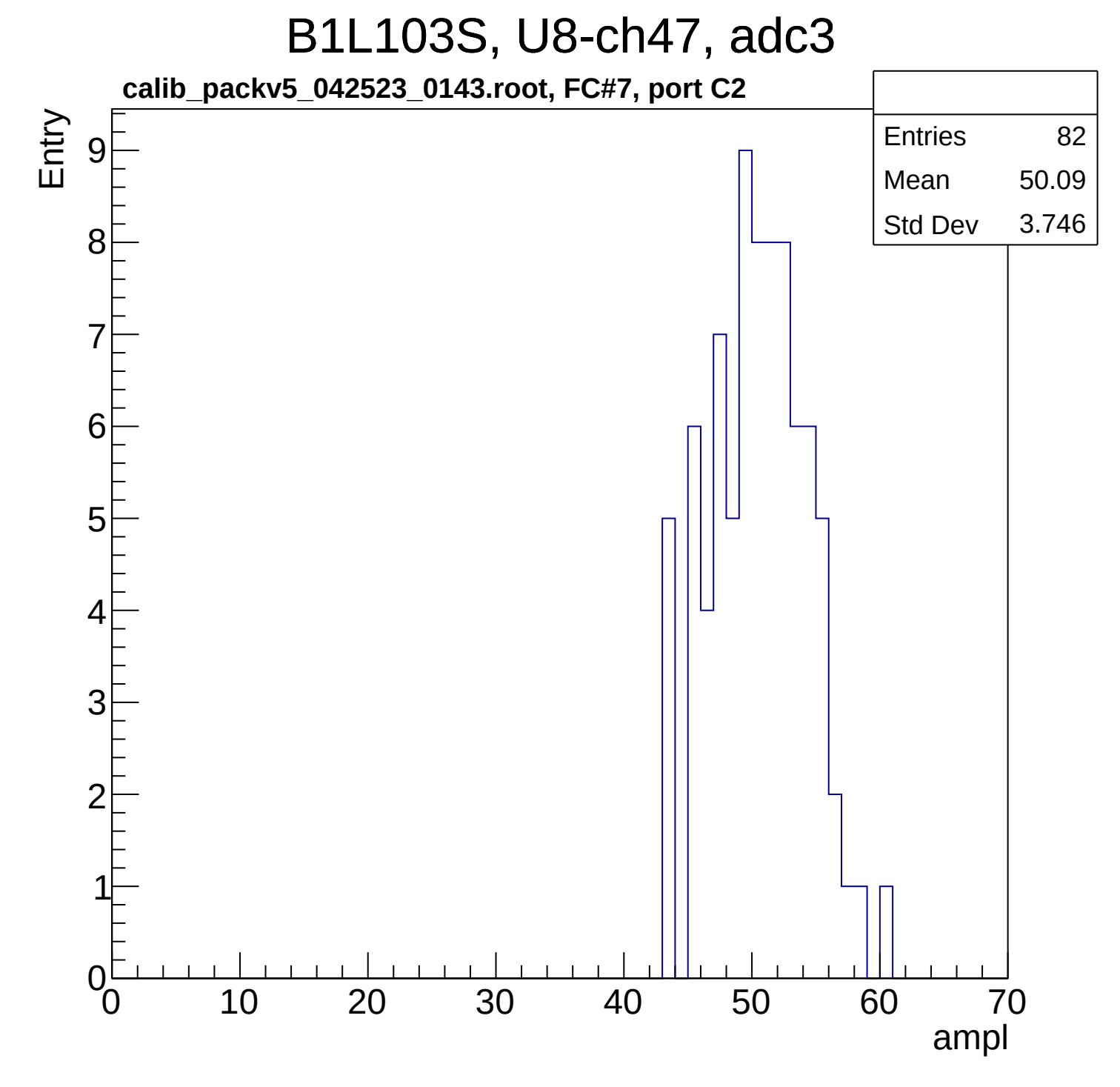

B1L103S, U8-ch46, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 14
Mean 61.86
Std Dev 1.407
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

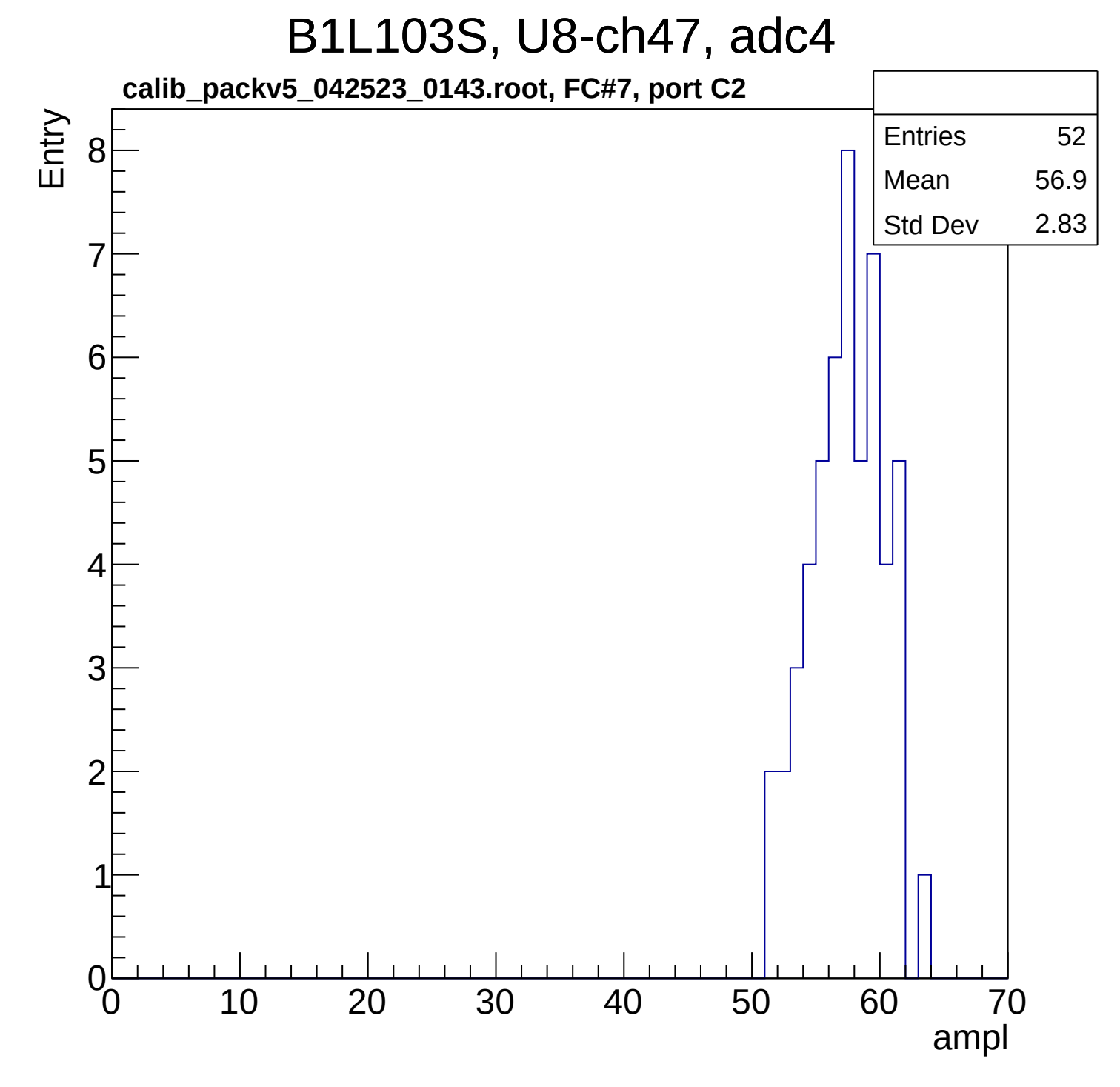

B1L103S, U8-ch46, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 48.33
Std Dev 19.33
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

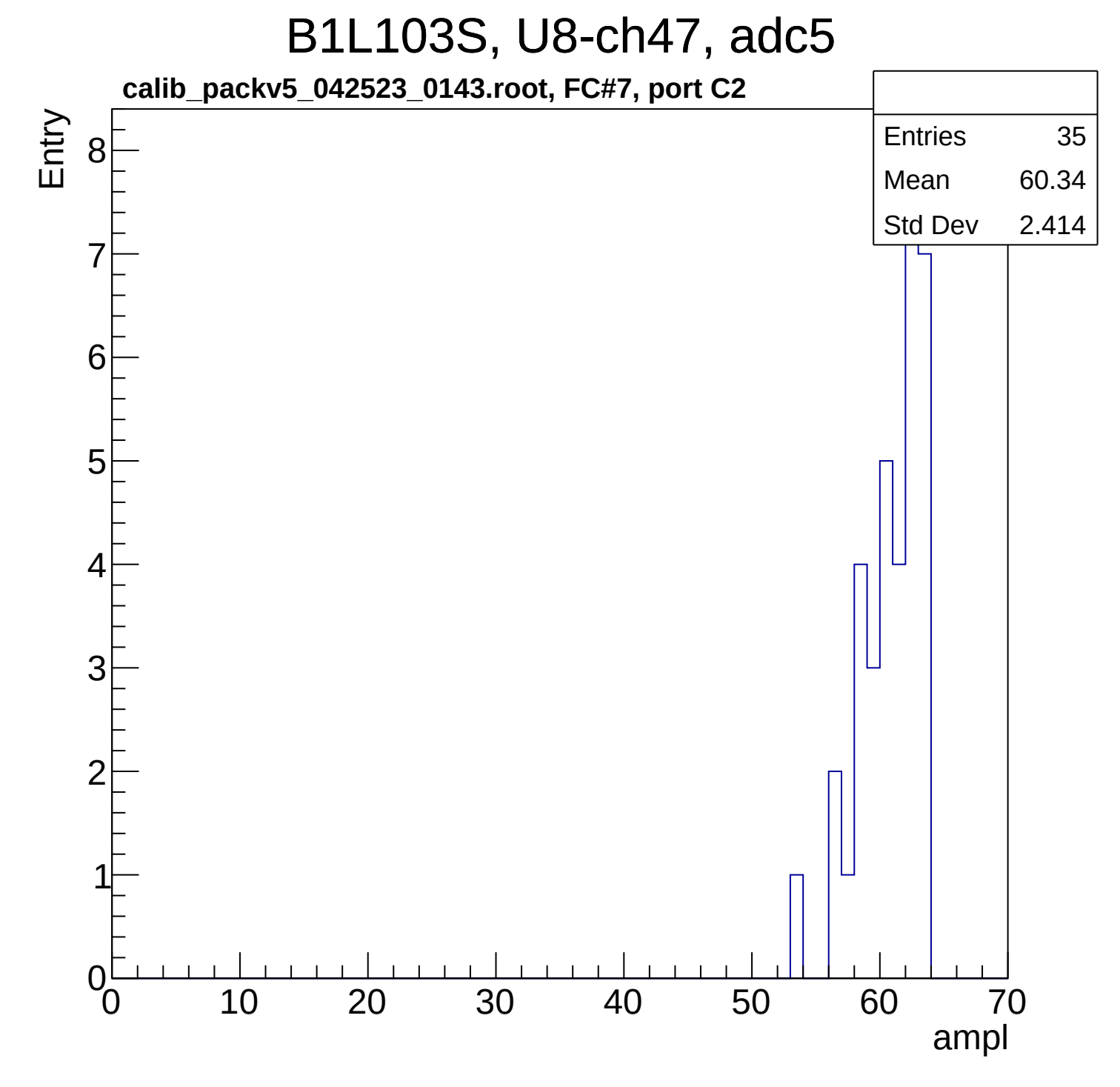

B1L103S, U8-ch47, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 30.41
Std Dev 3.408
Gaus mean : 31.3660
Gaus Width: 3.1627
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

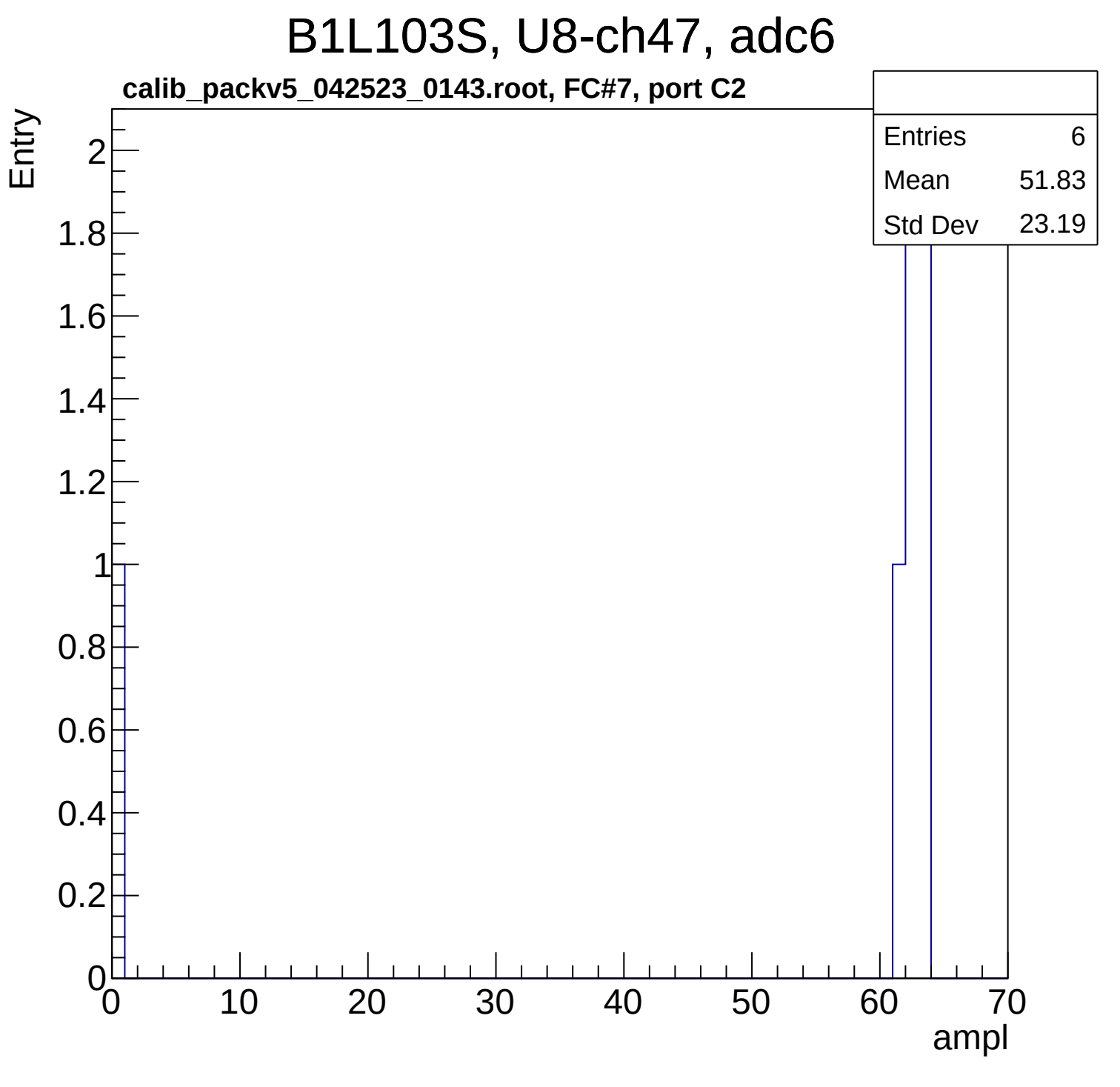

B1L103S, U8-ch47, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 37.07
Std Dev 3.767
Gaus mean : 37.8088
Gaus Width: 3.6355
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

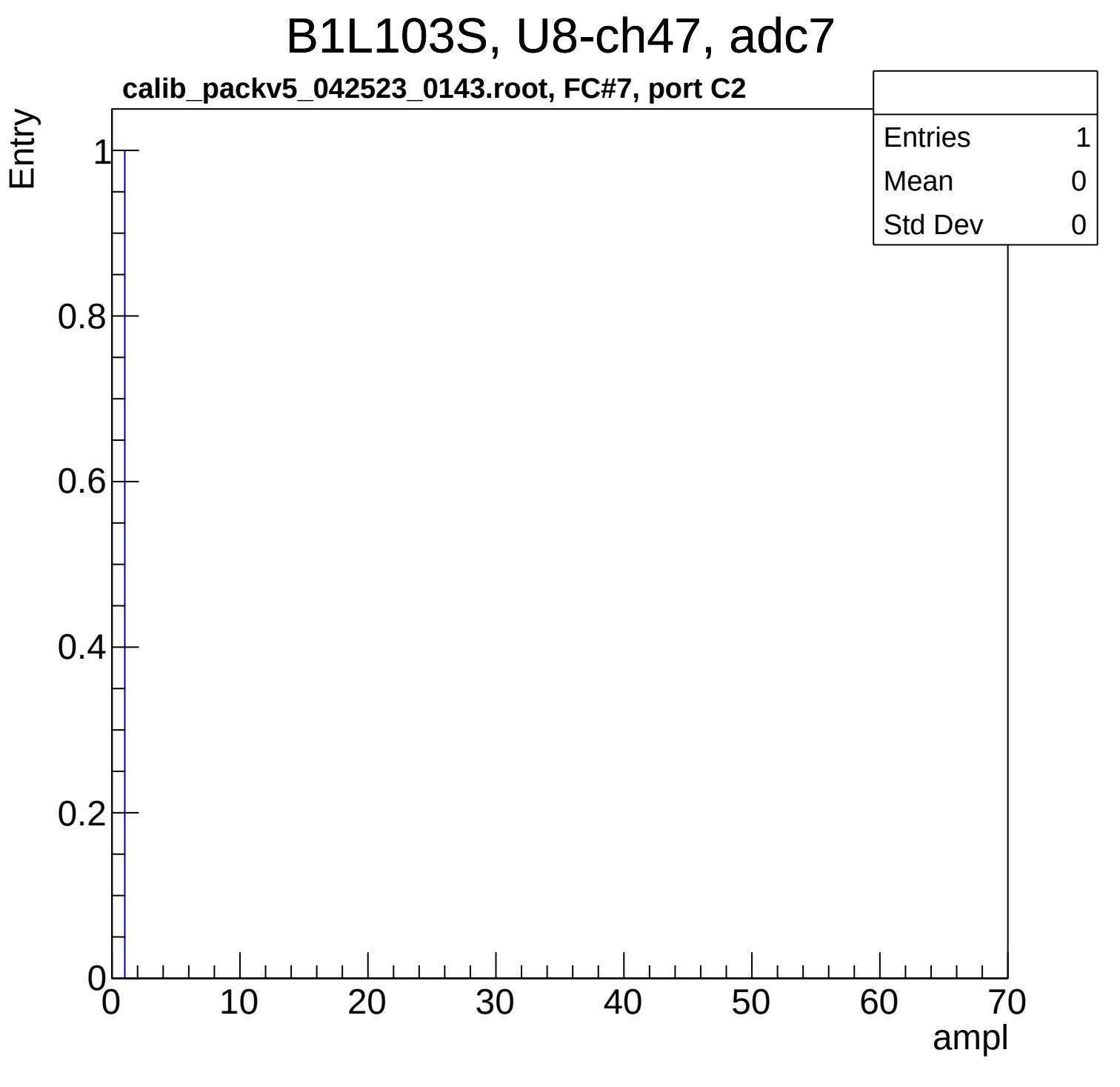

B1L103S, U8-ch47, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 42.98
Std Dev 3.587
Gaus mean : 43.0243
Gaus Width: 4.3340
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

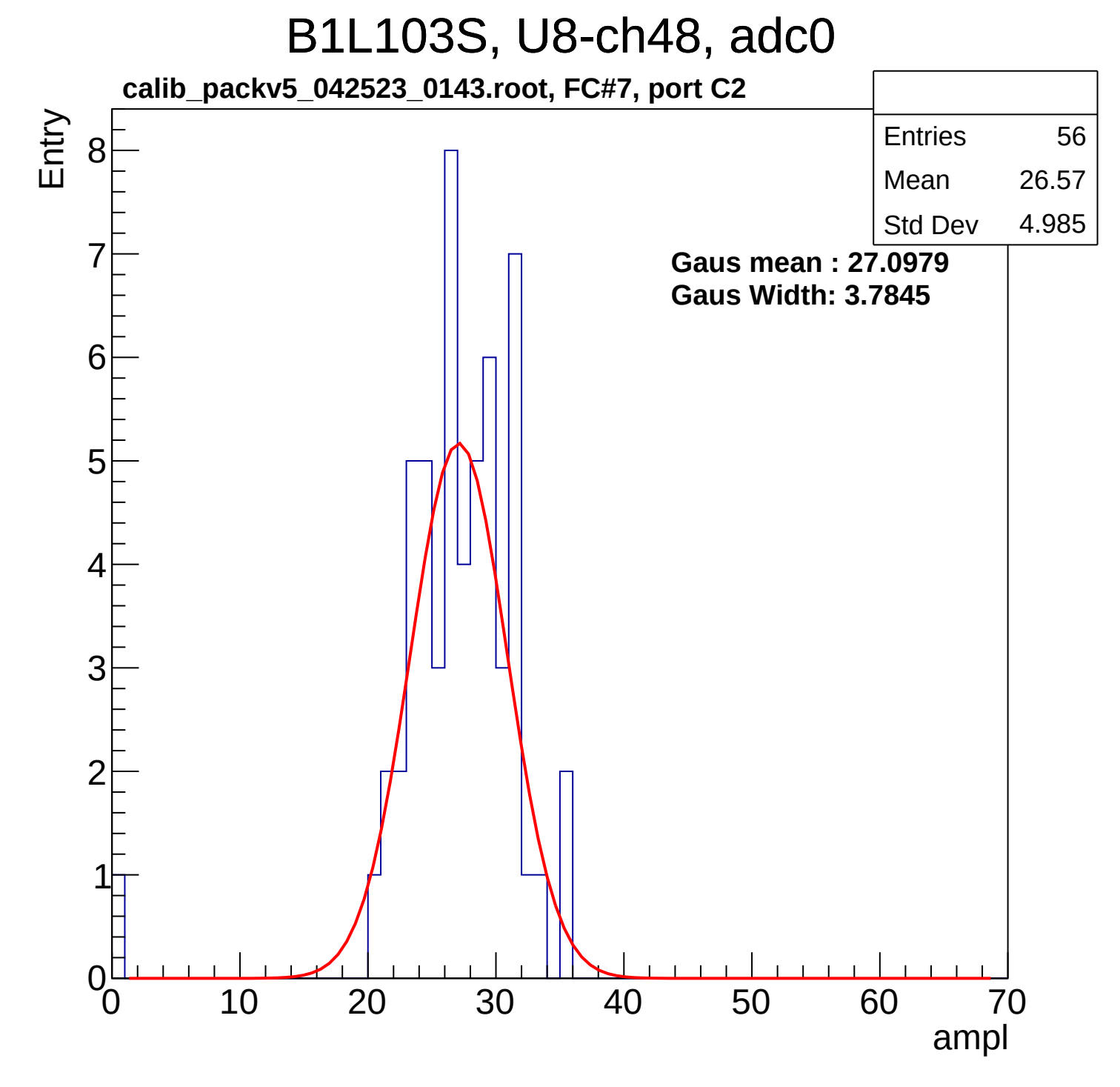

B1L103S, U8-ch47, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 82
Mean 50.09
Std Dev 3.746
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

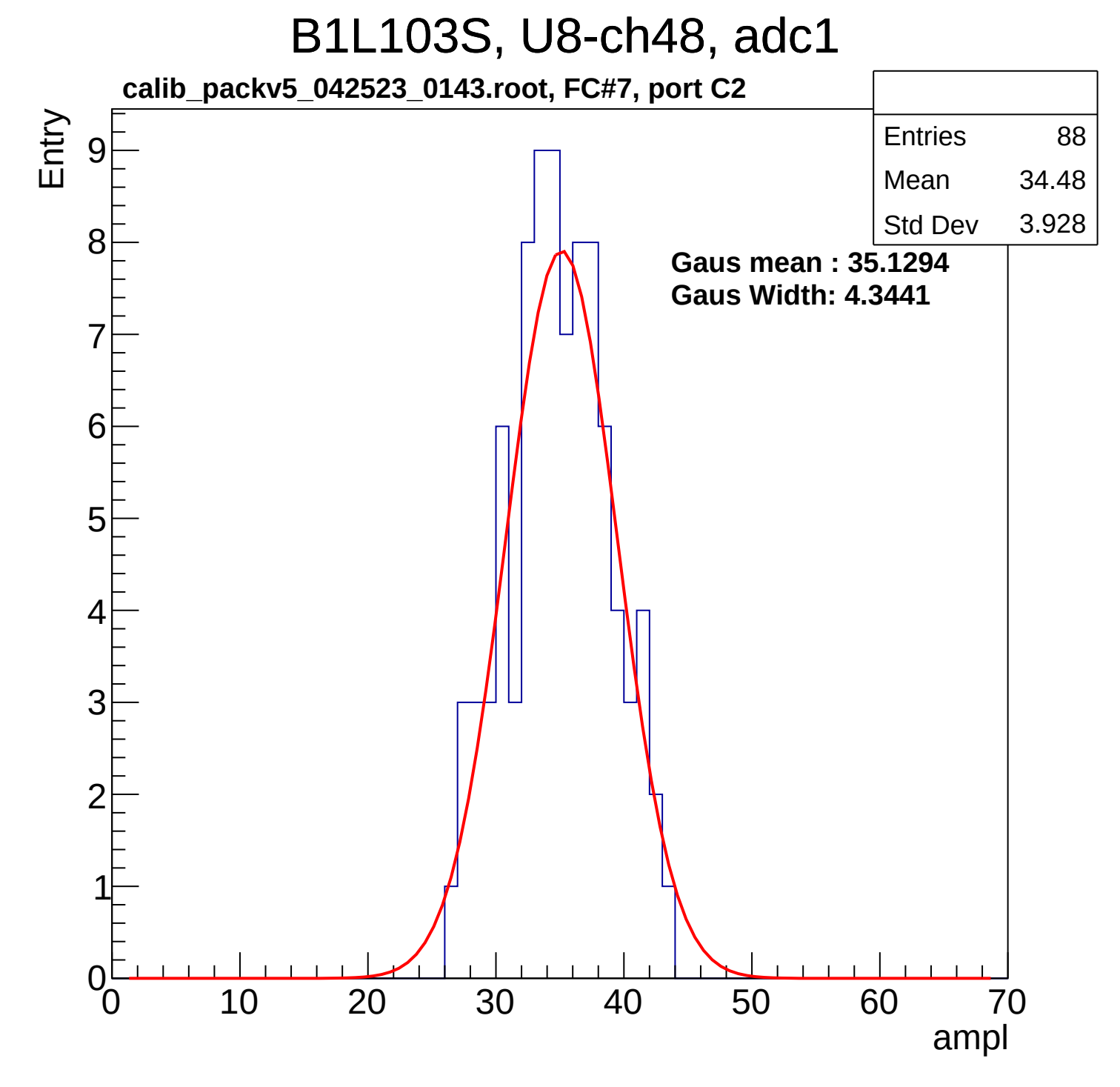

B1L103S, U8-ch47, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 56.9
Std Dev 2.83
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

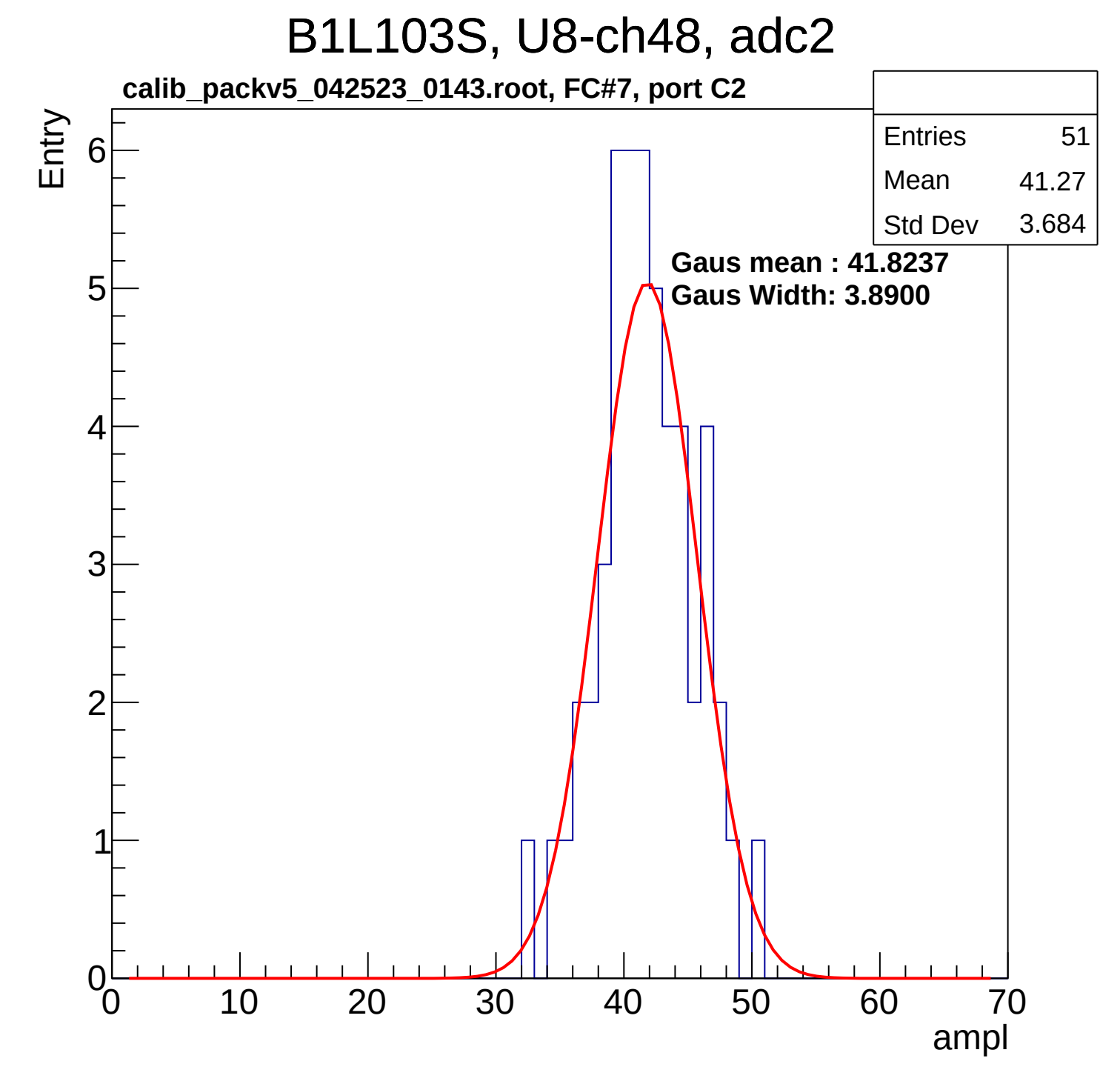

B1L103S, U8-ch47, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 35
Mean 60.34
Std Dev 2.414
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

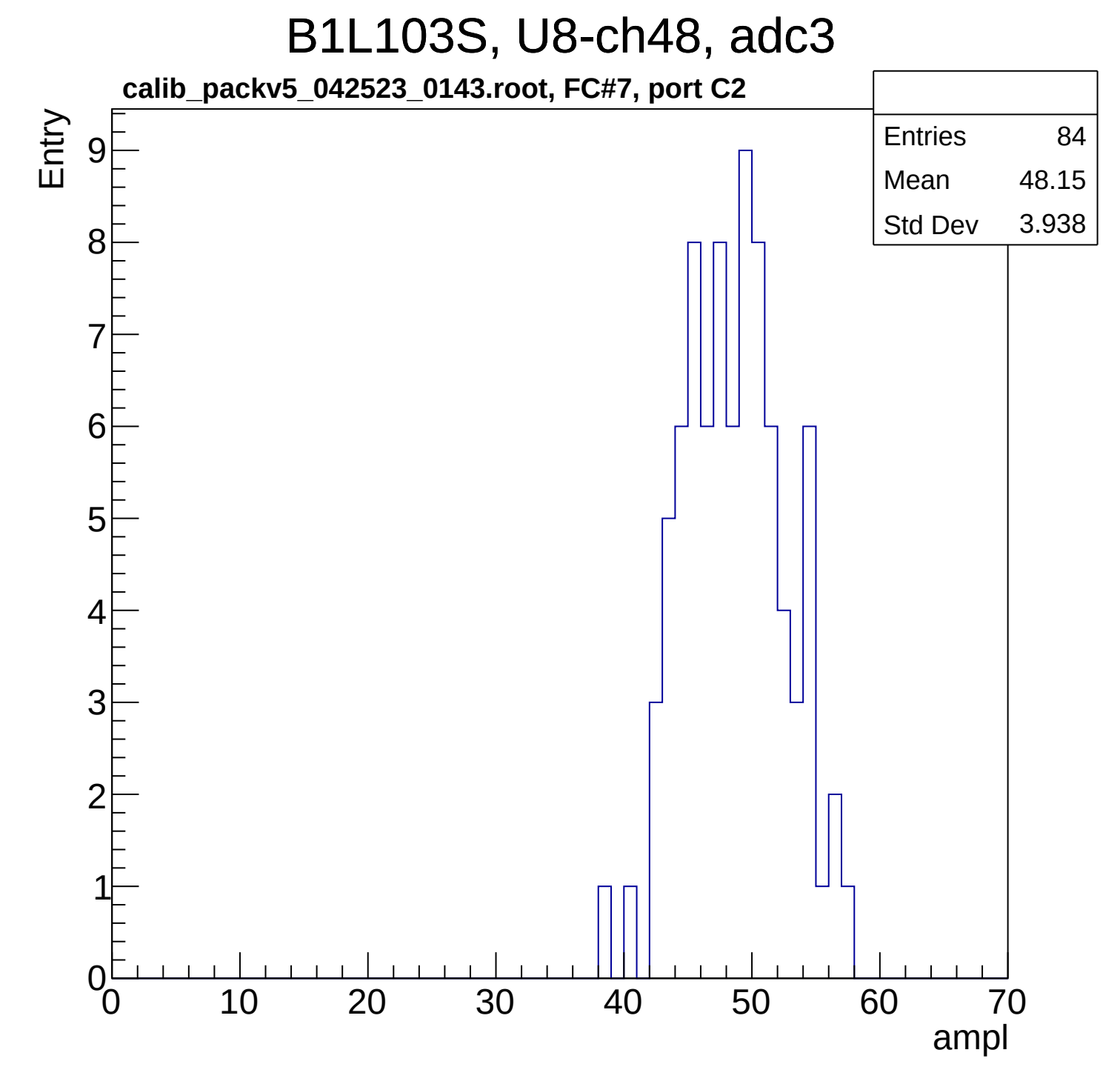

B1L103S, U8-ch47, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 51.83
Std Dev 23.19
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

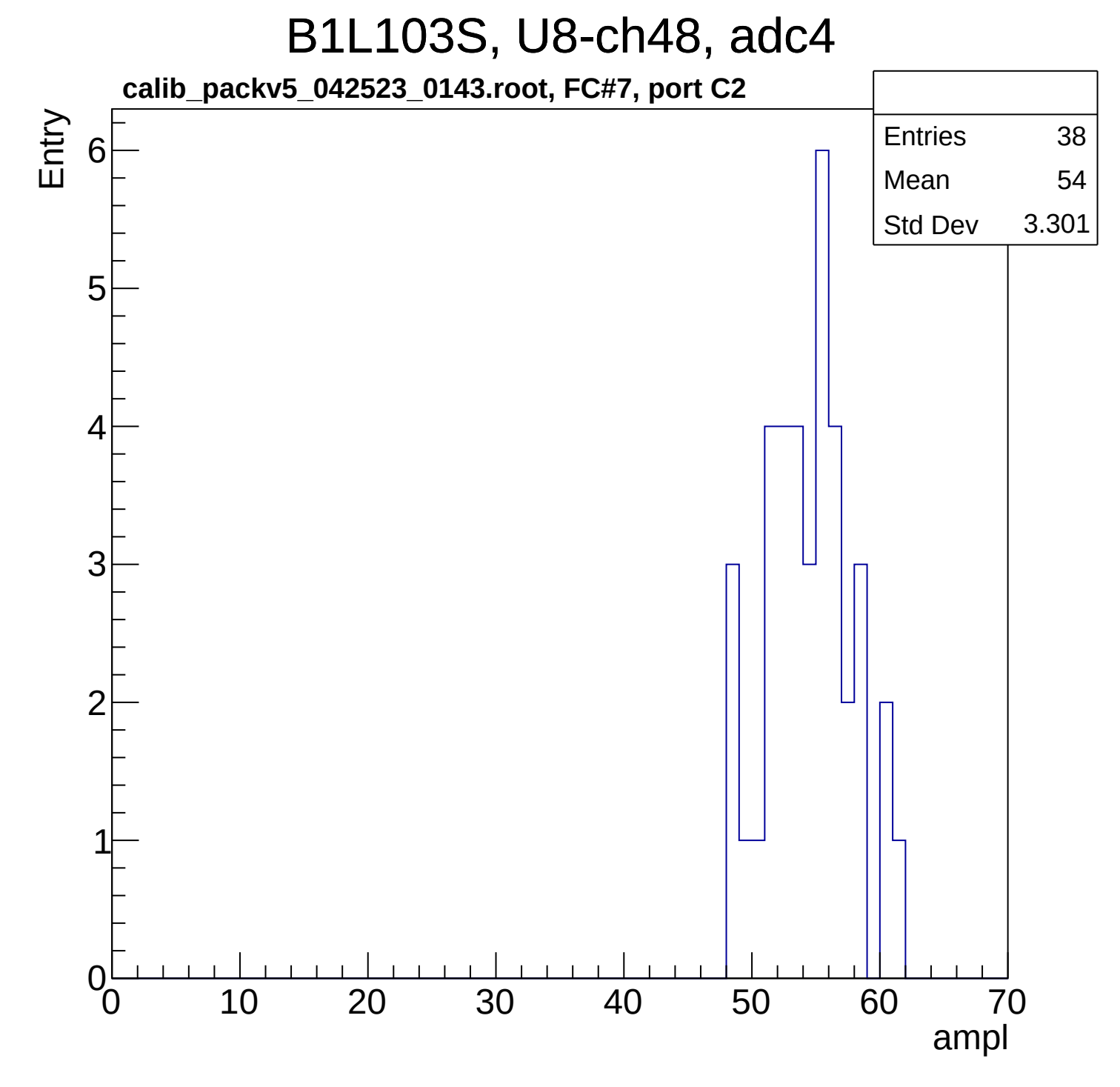

B1L103S, U8-ch47, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

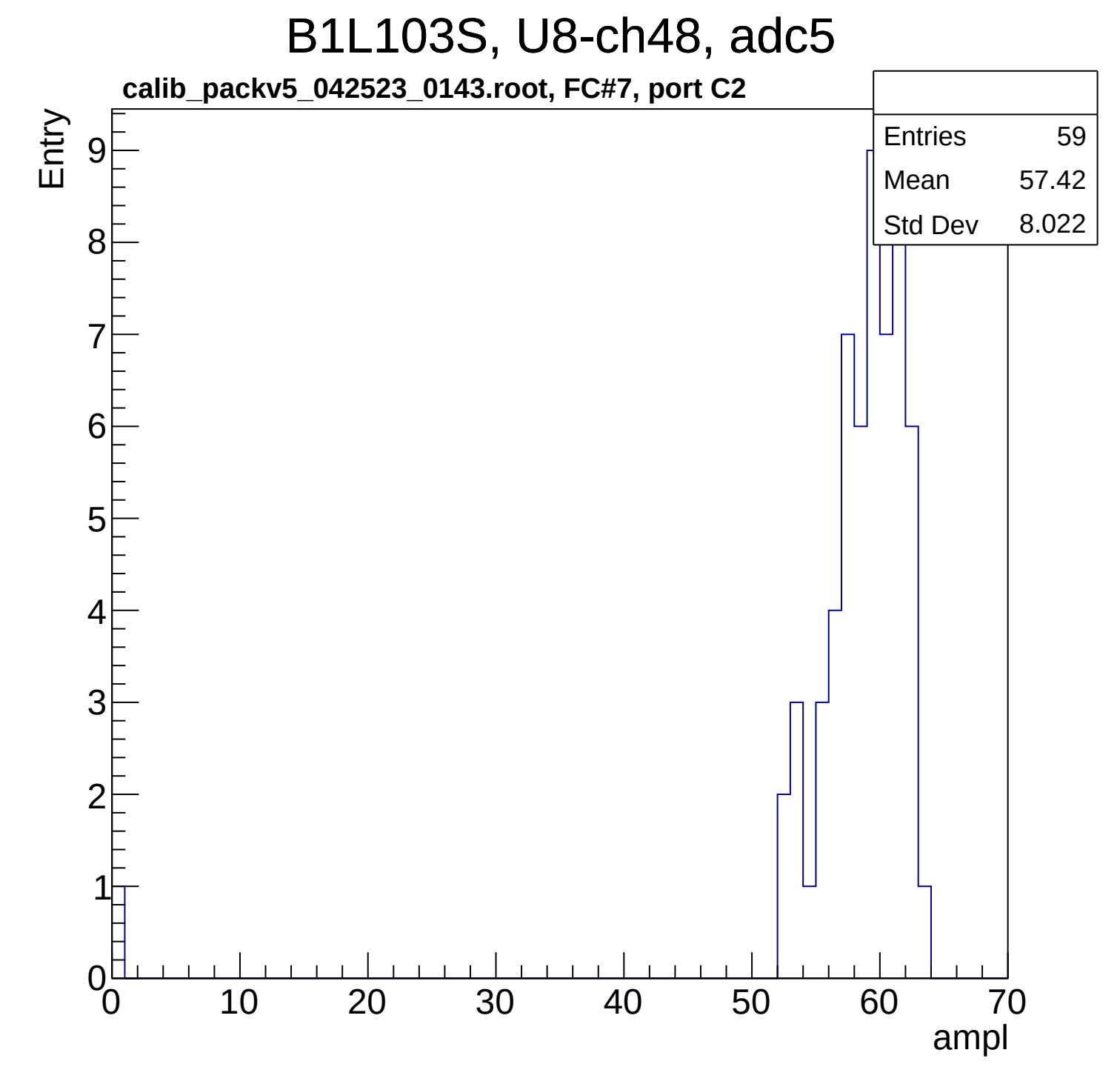

B1L103S, U8-ch48, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 26.57
Std Dev 4.985
Gaus mean : 27.0979
Gaus Width: 3.7845
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

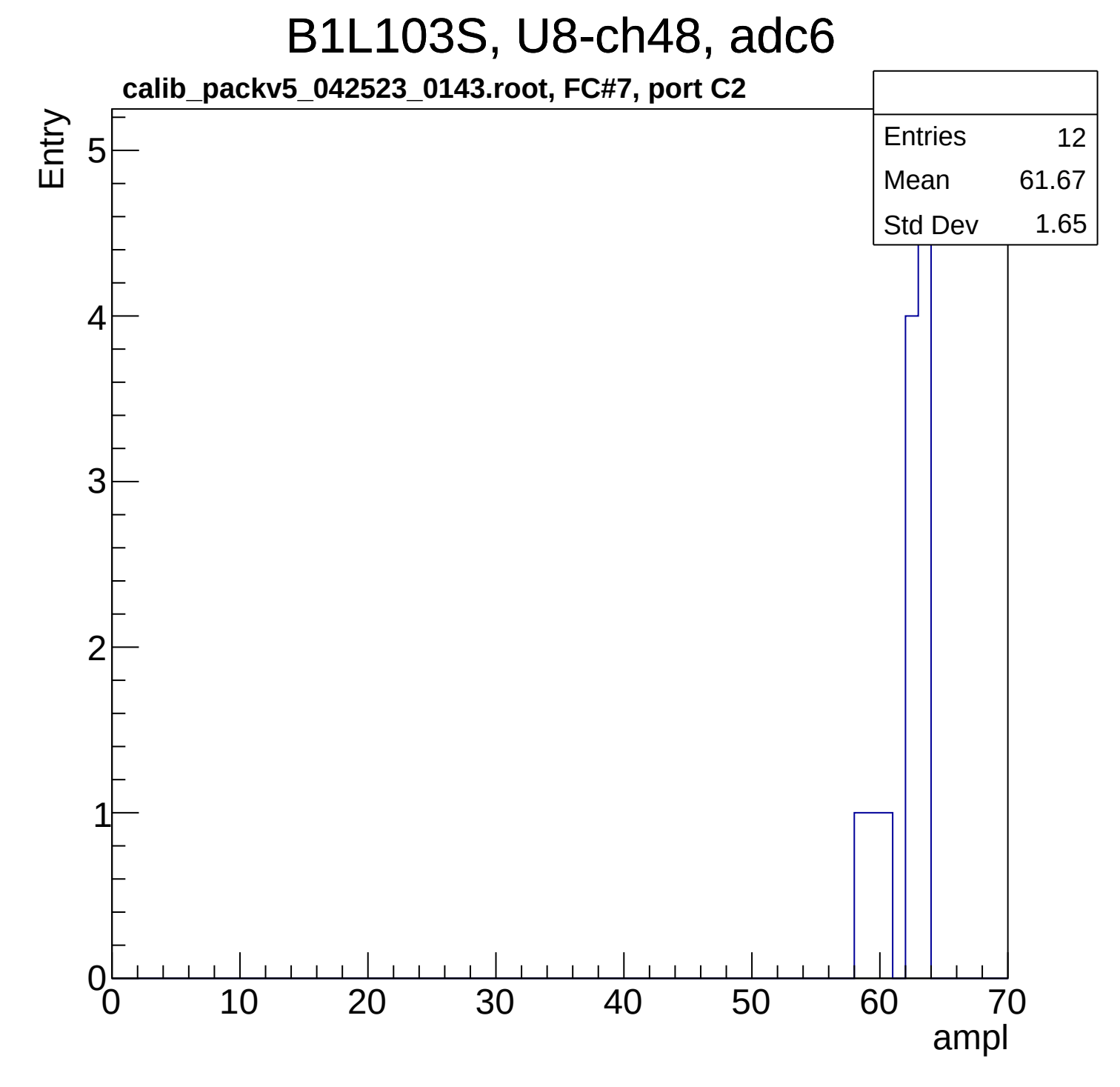

B1L103S, U8-ch48, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 88
Mean 34.48
Std Dev 3.928
Gaus mean : 35.1294
Gaus Width: 4.3441
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

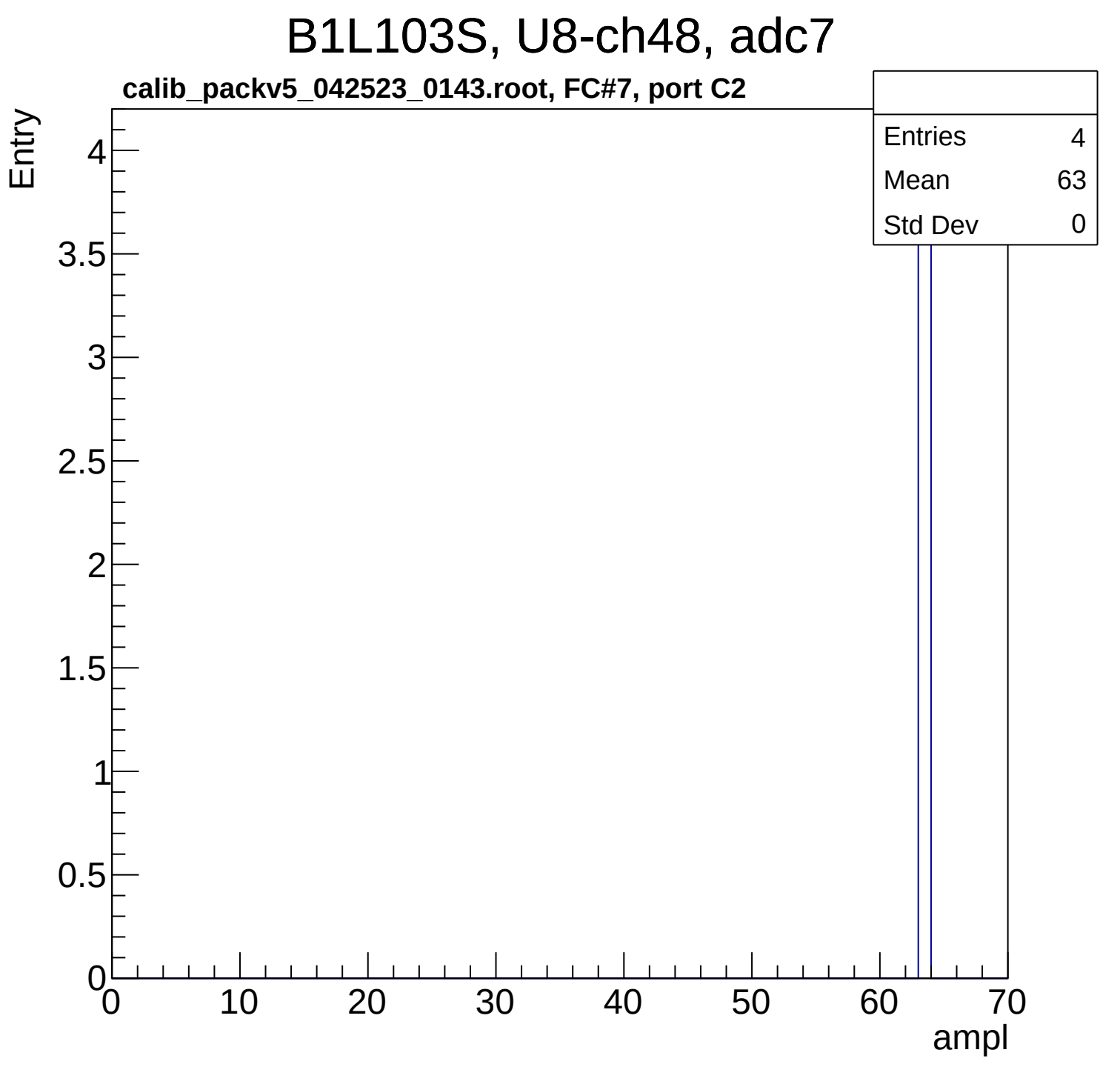

B1L103S, U8-ch48, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 41.27
Std Dev 3.684
Gaus mean : 41.8237
Gaus Width: 3.8900
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

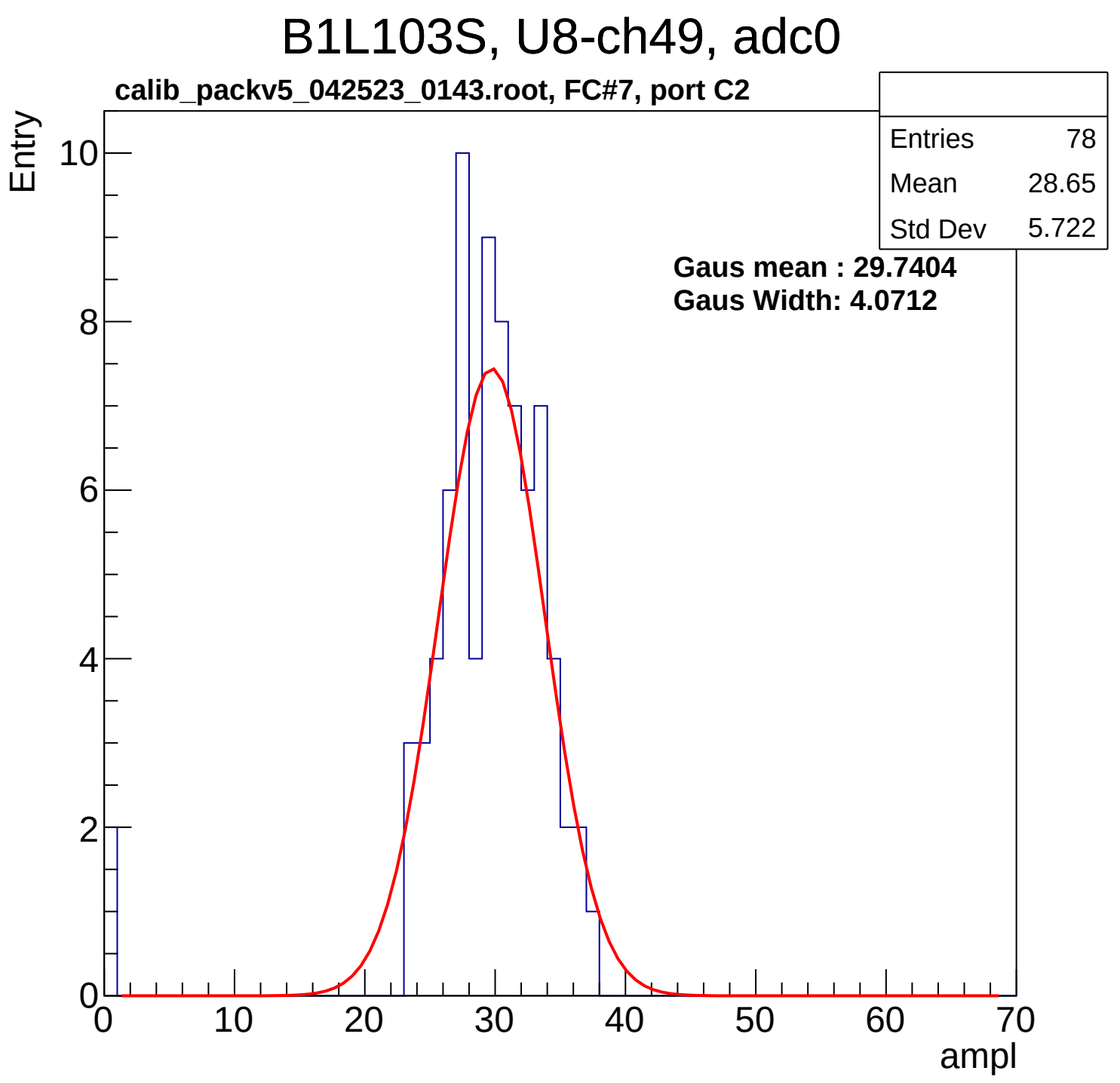

B1L103S, U8-ch48, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 84
Mean 48.15
Std Dev 3.938
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

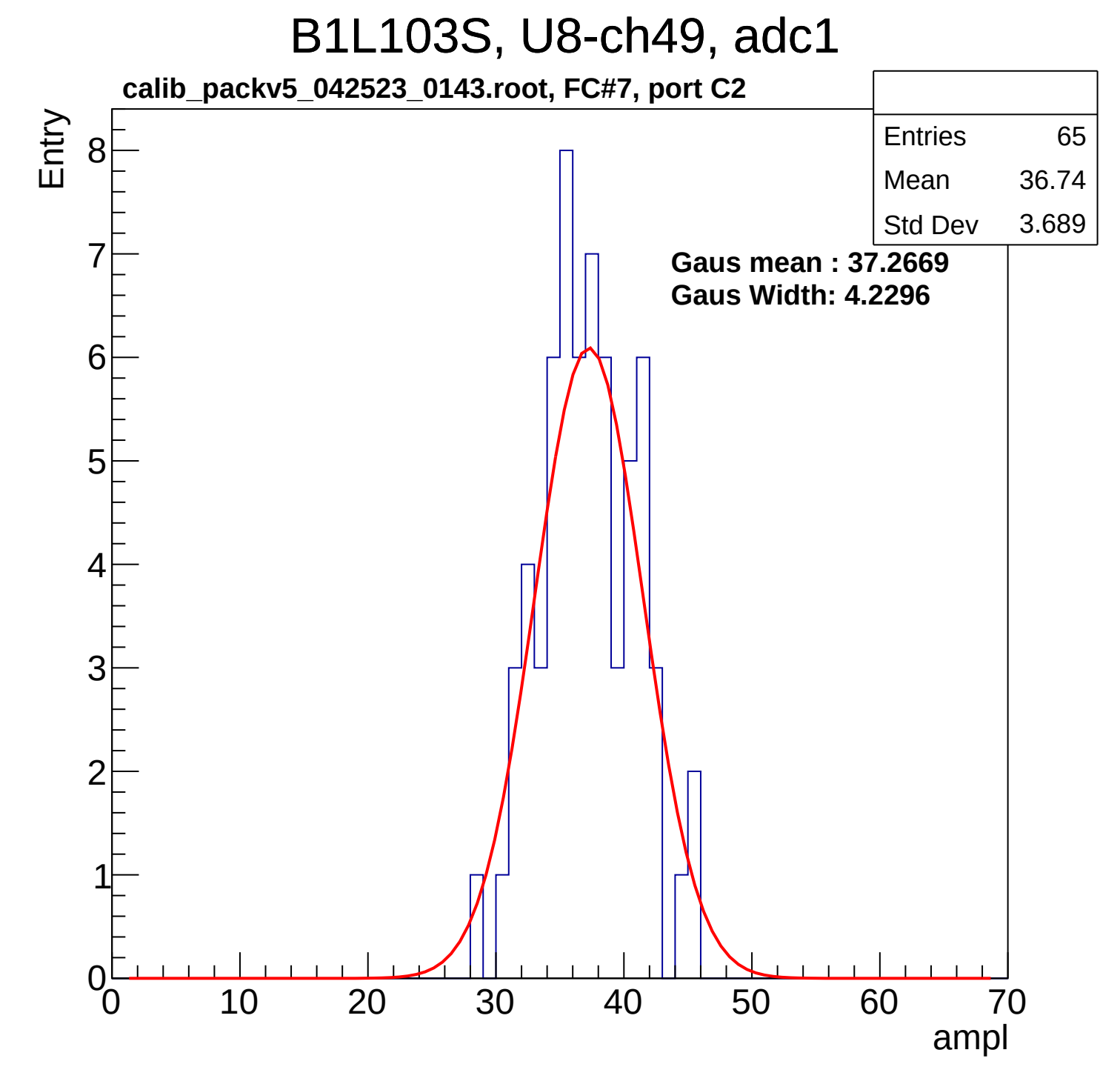

B1L103S, U8-ch48, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 38
Mean 54
Std Dev 3.301
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

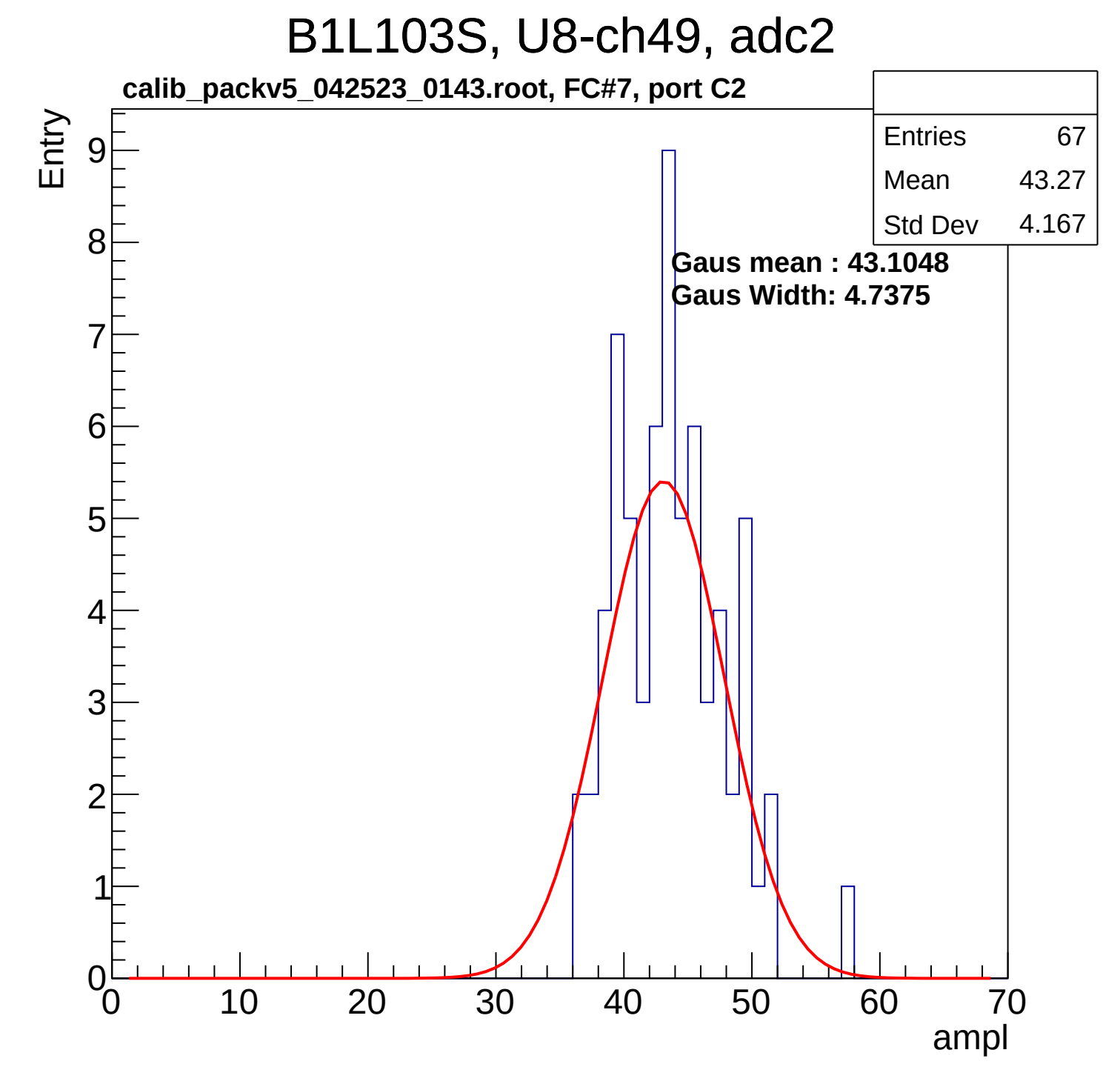

B1L103S, U8-ch48, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 57.42
Std Dev 8.022
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

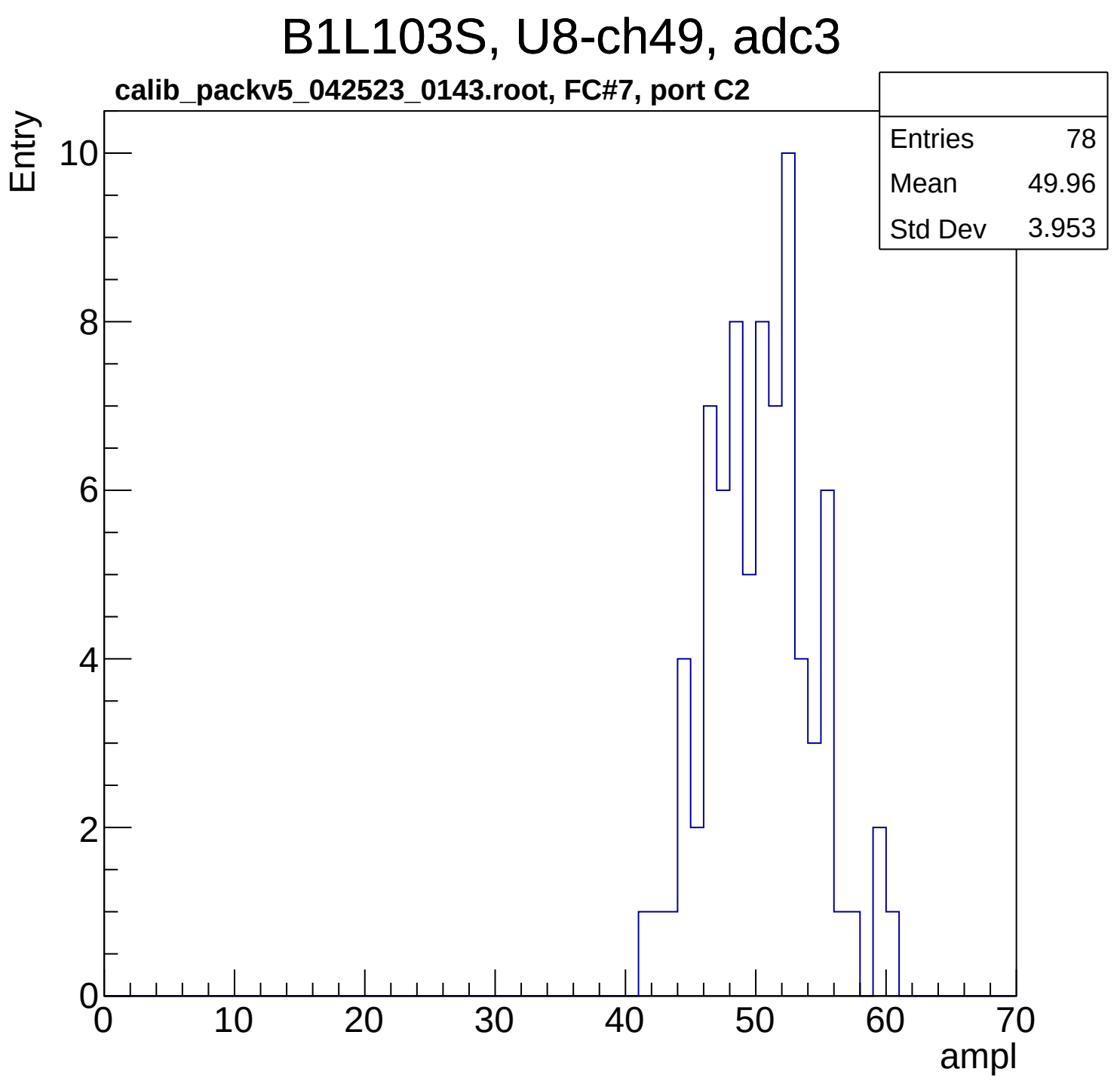

B1L103S, U8-ch48, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 12
Mean 61.67
Std Dev 1.65
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

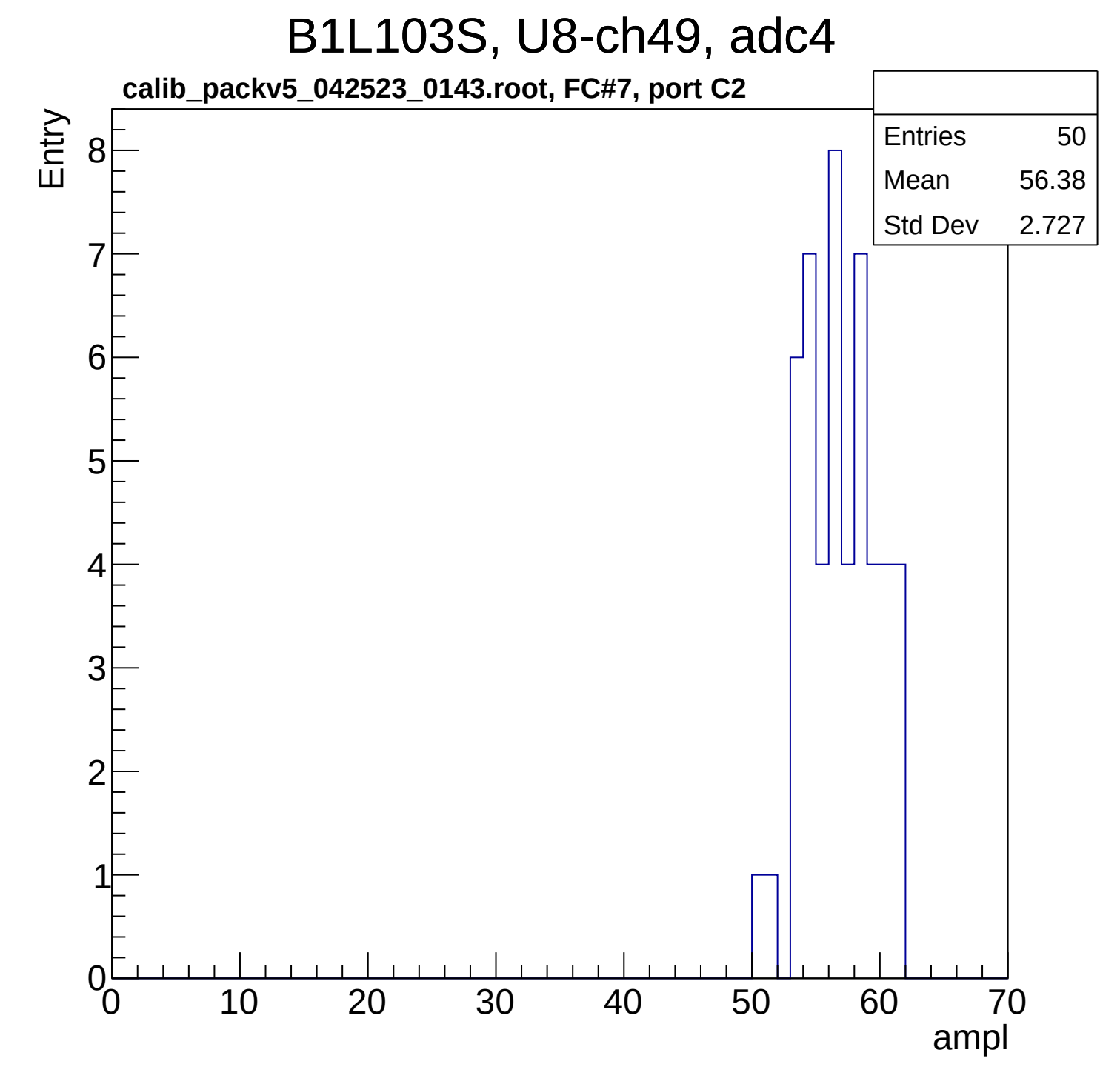

B1L103S, U8-ch48, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 63
Std Dev 0
Entry
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70
ampl

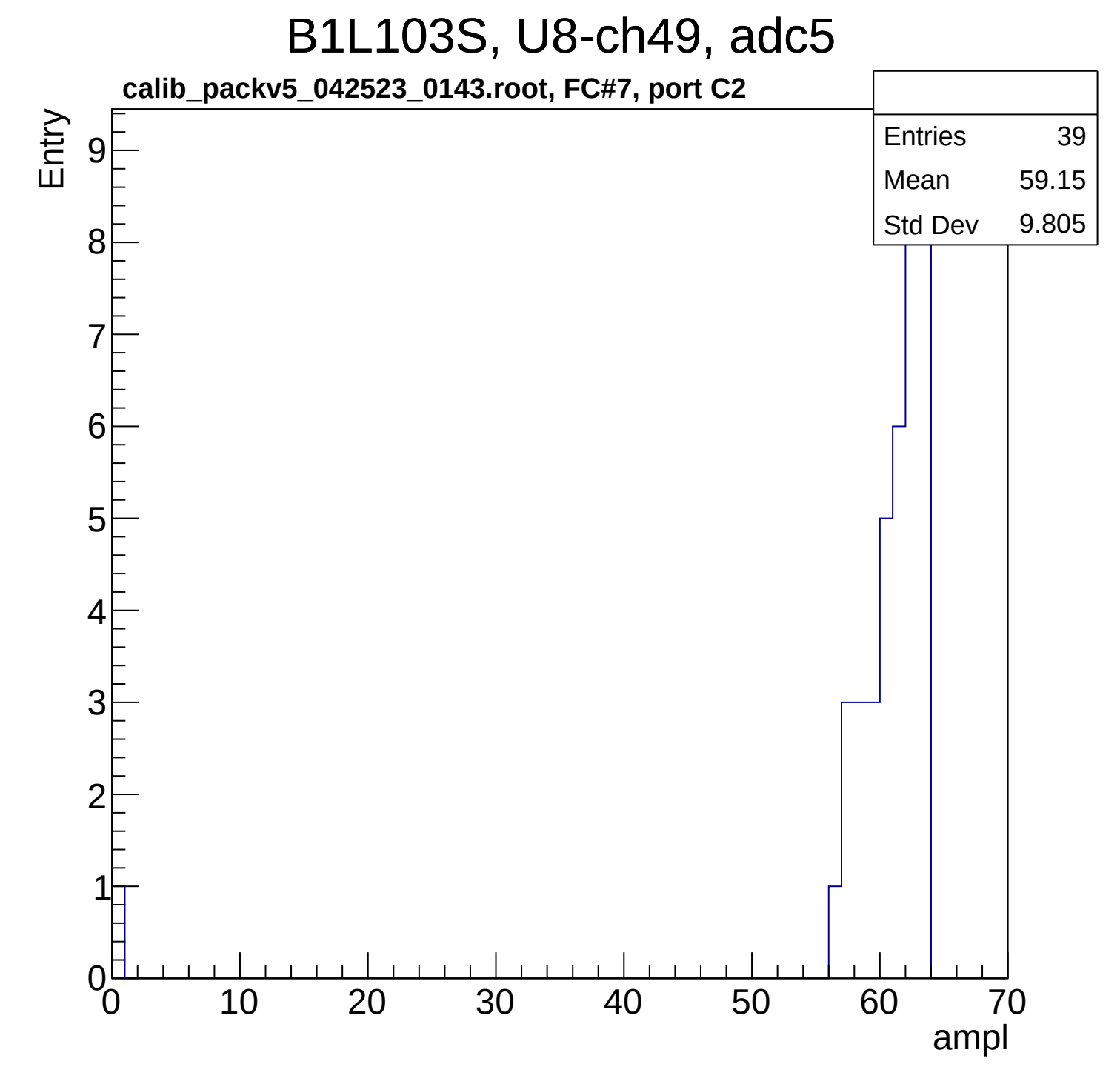

B1L103S, U8-ch49, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 28.65
Std Dev 5.722
Gaus mean : 29.7404
Gaus Width: 4.0712
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

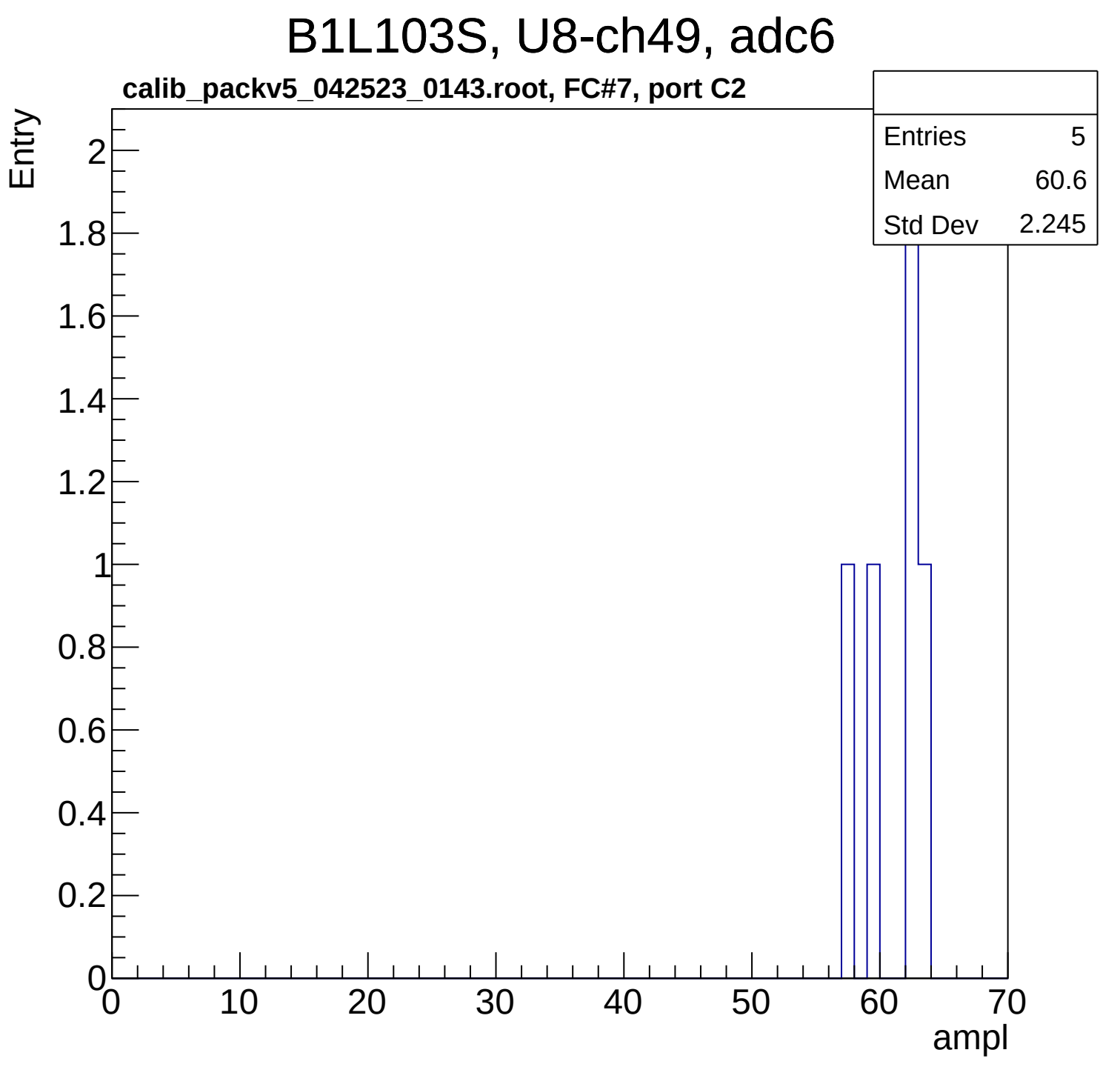

B1L103S, U8-ch49, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 36.74
Std Dev 3.689
Gaus mean : 37.2669
Gaus Width: 4.2296
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

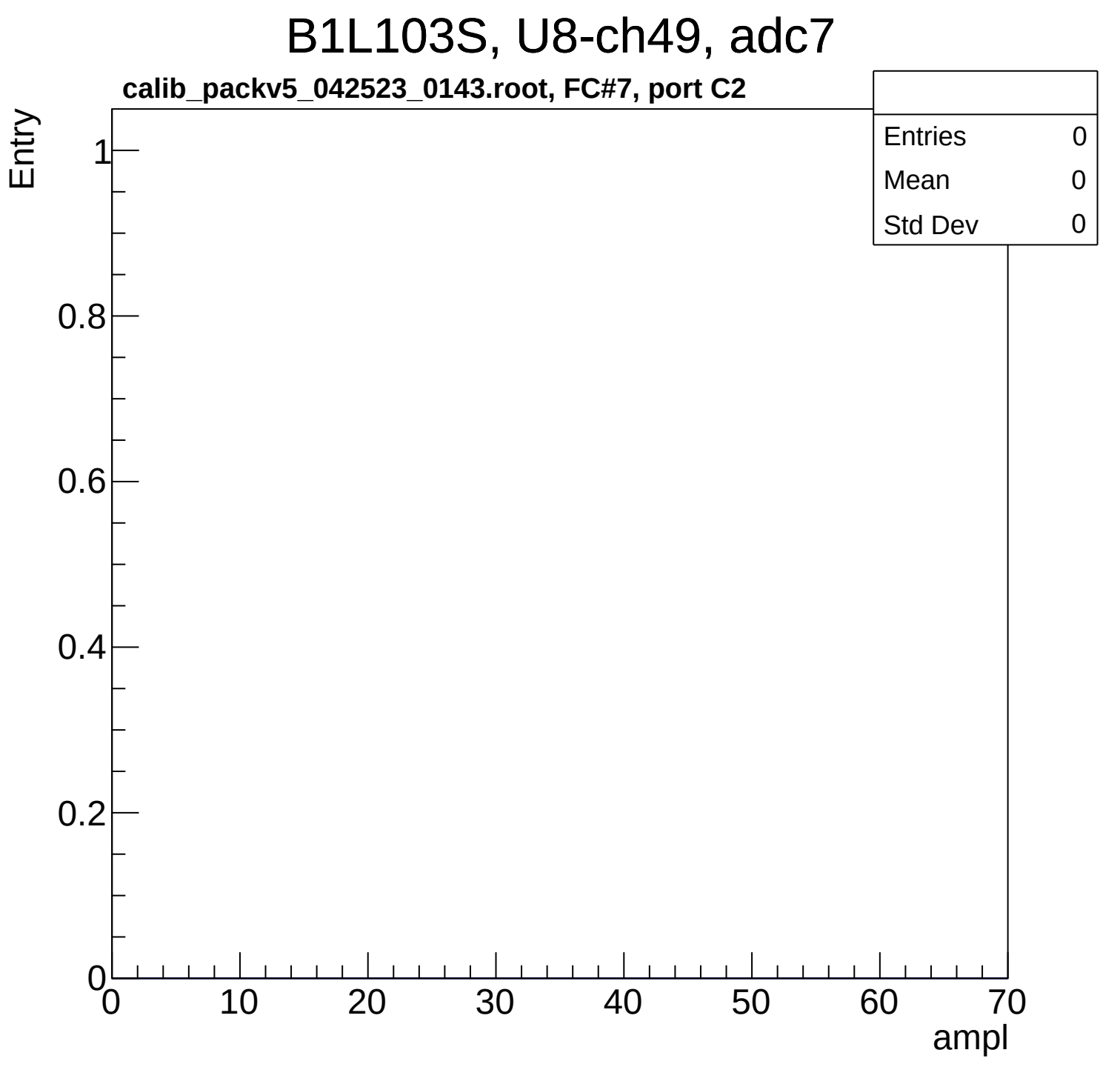

B1L103S, U8-ch49, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 43.27
Std Dev 4.167
Gaus mean : 43.1048
Gaus Width: 4.7375
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

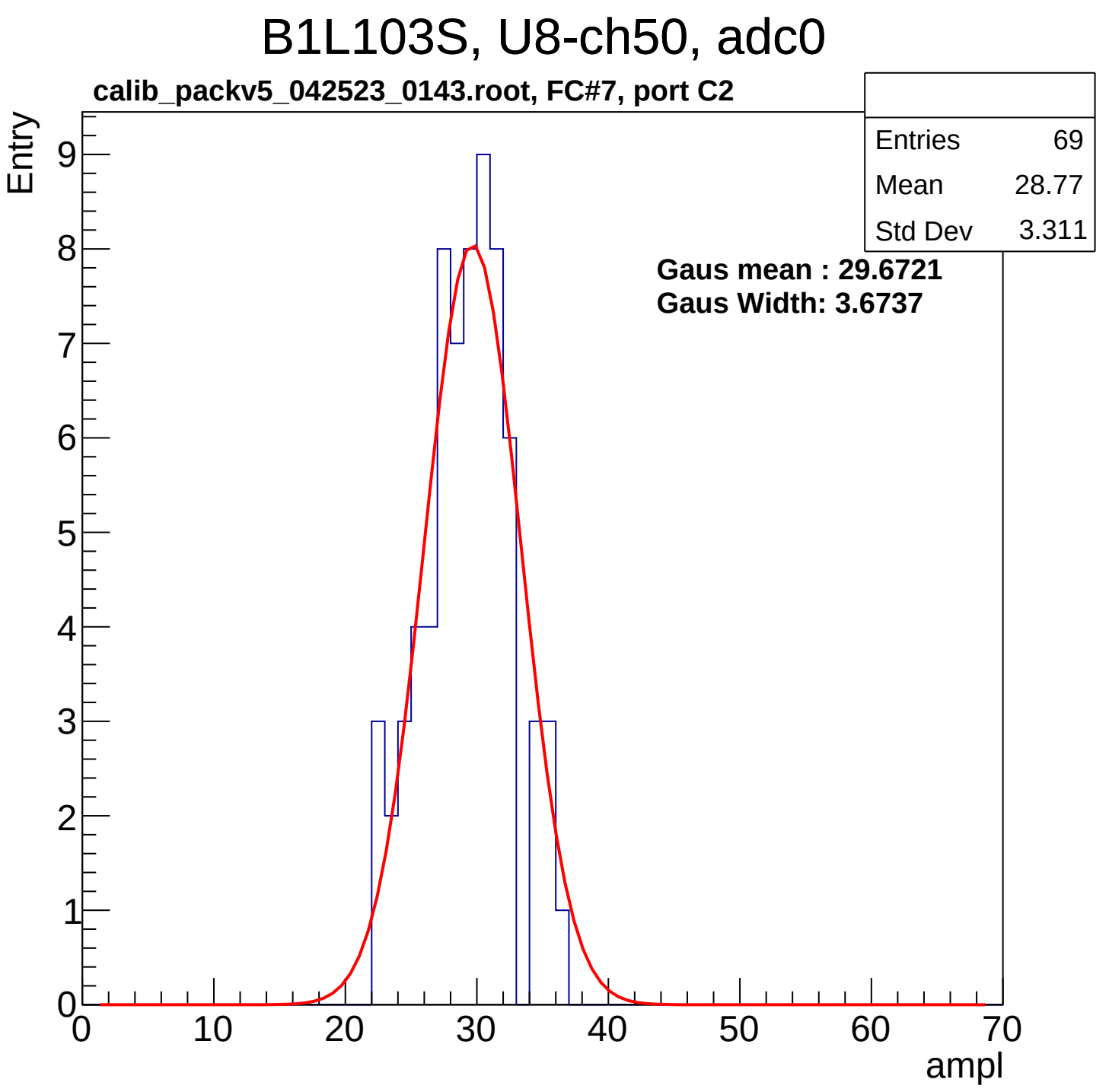

B1L103S, U8-ch49, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 49.96
Std Dev 3.953
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

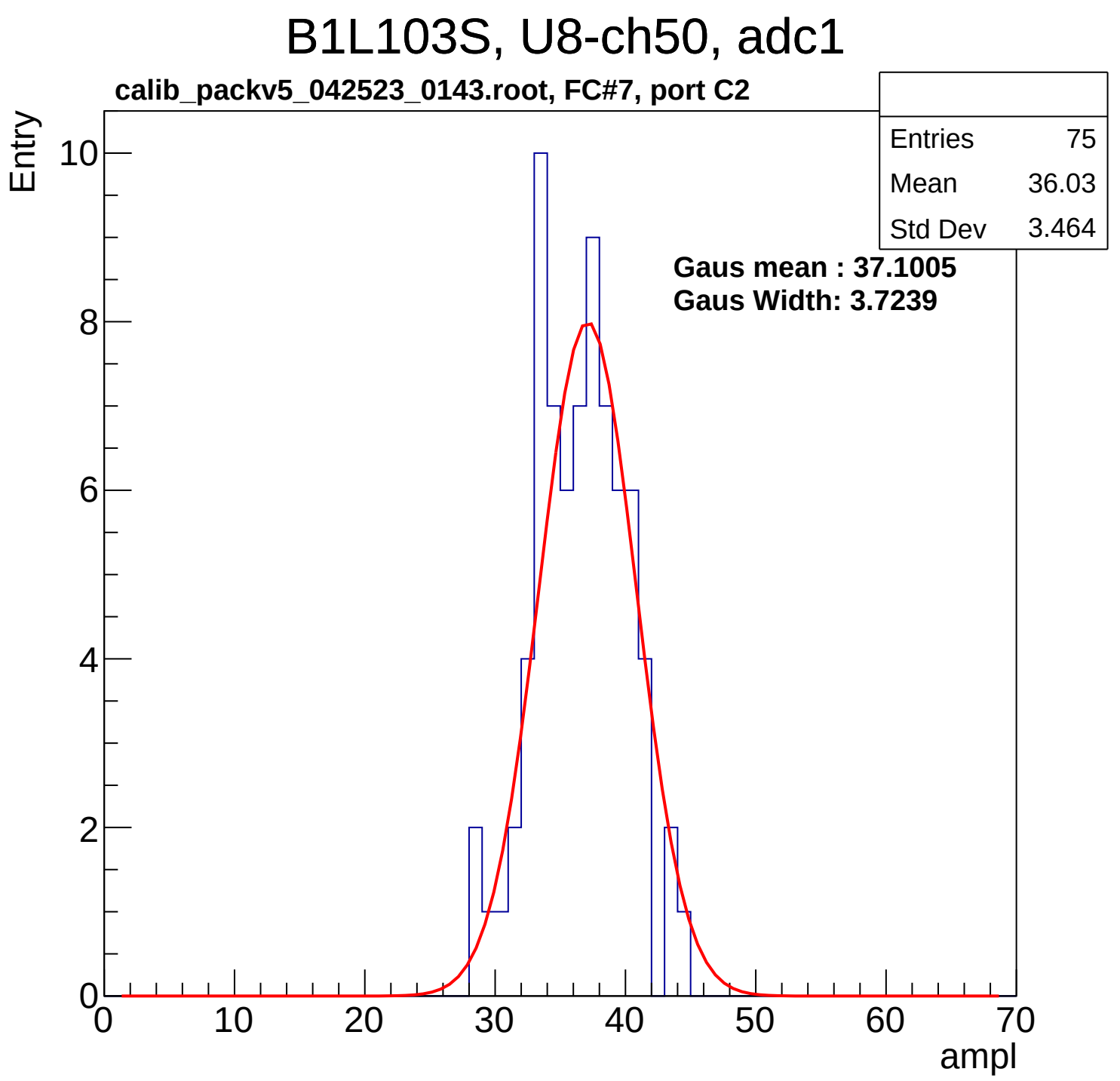

B1L103S, U8-ch49, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 56.38
Std Dev 2.727
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

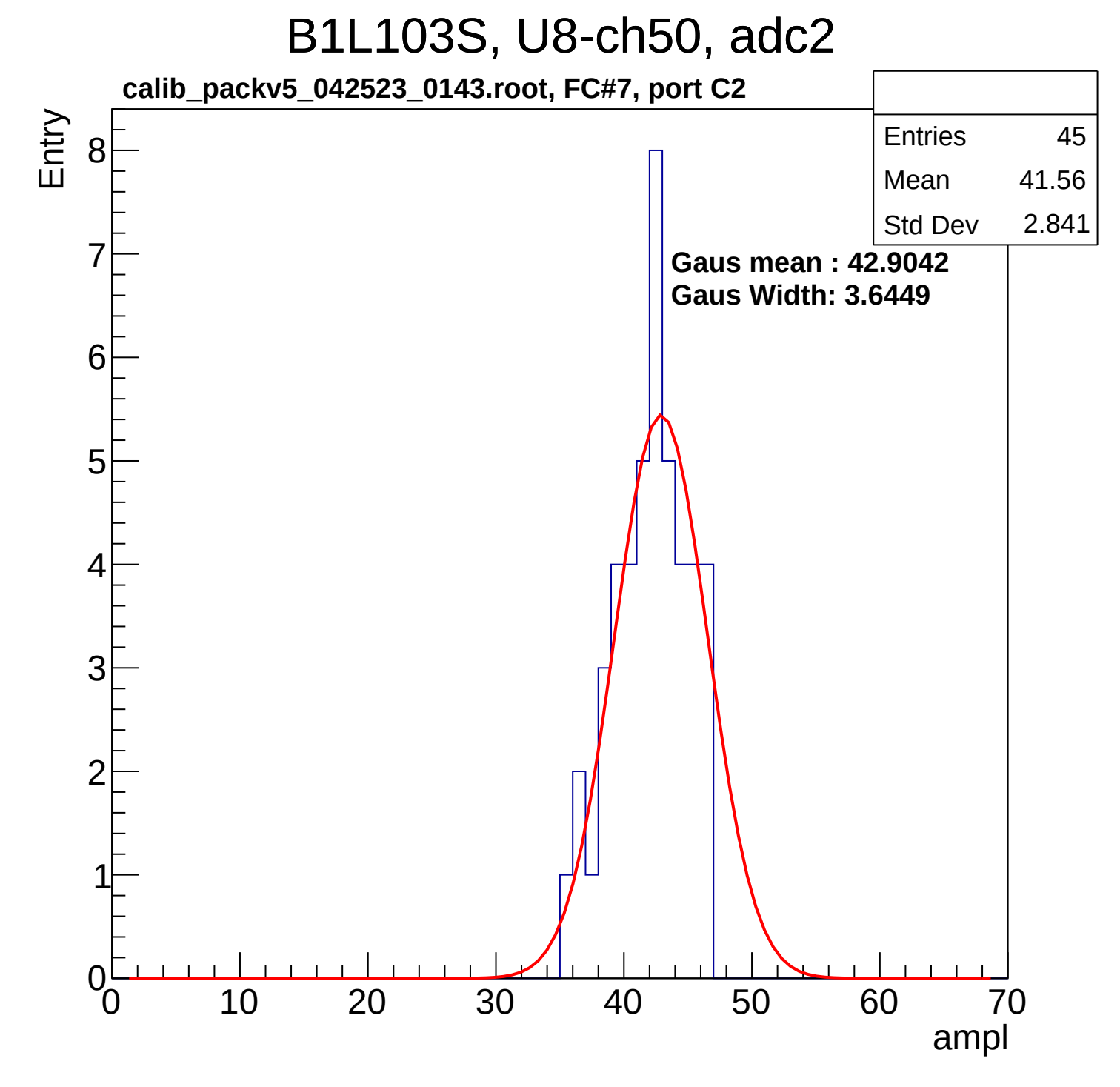

B1L103S, U8-ch49, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 39
Mean 59.15
Std Dev 9.805
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

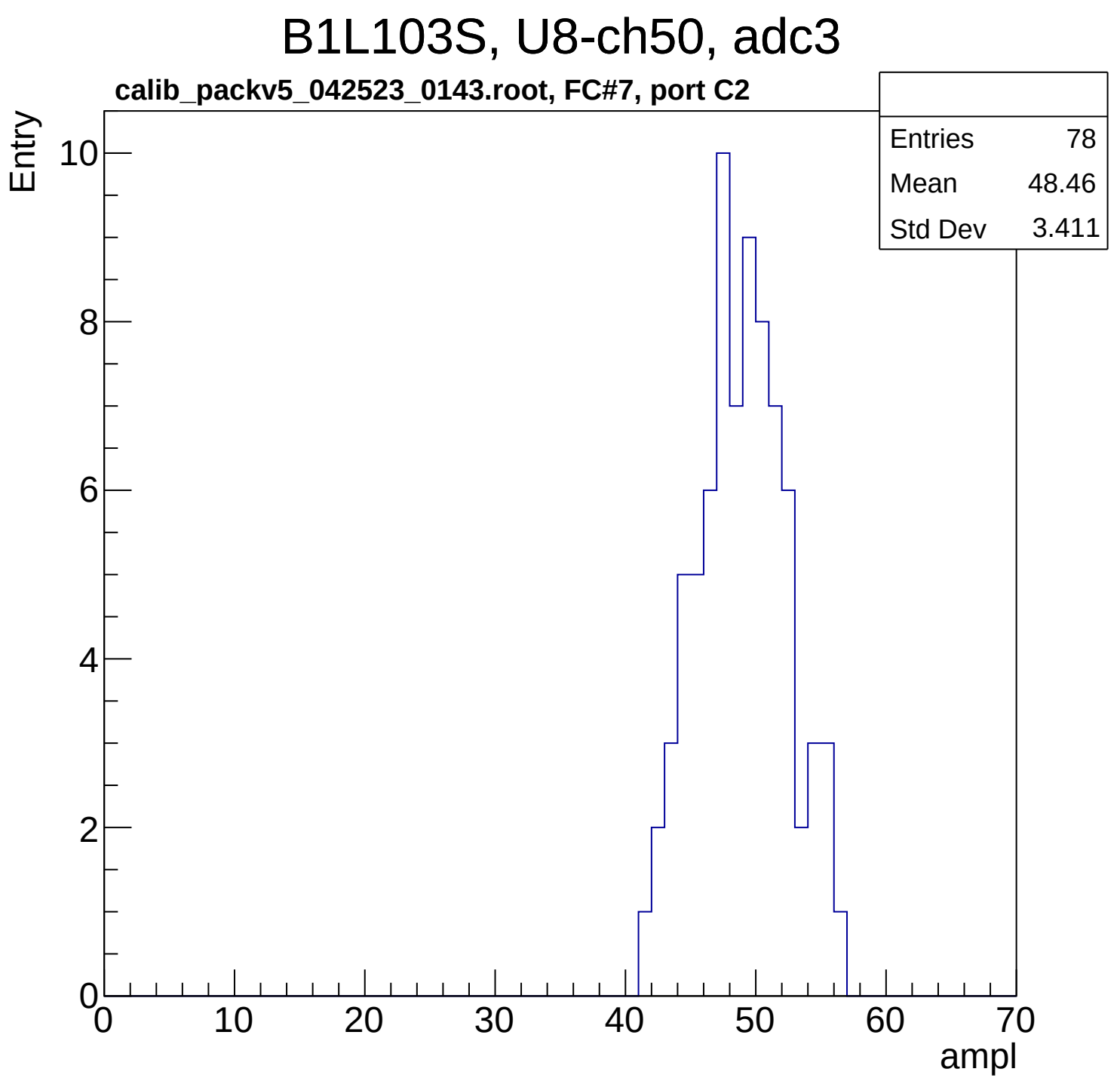

B1L103S, U8-ch49, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 60.6
Std Dev 2.245
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

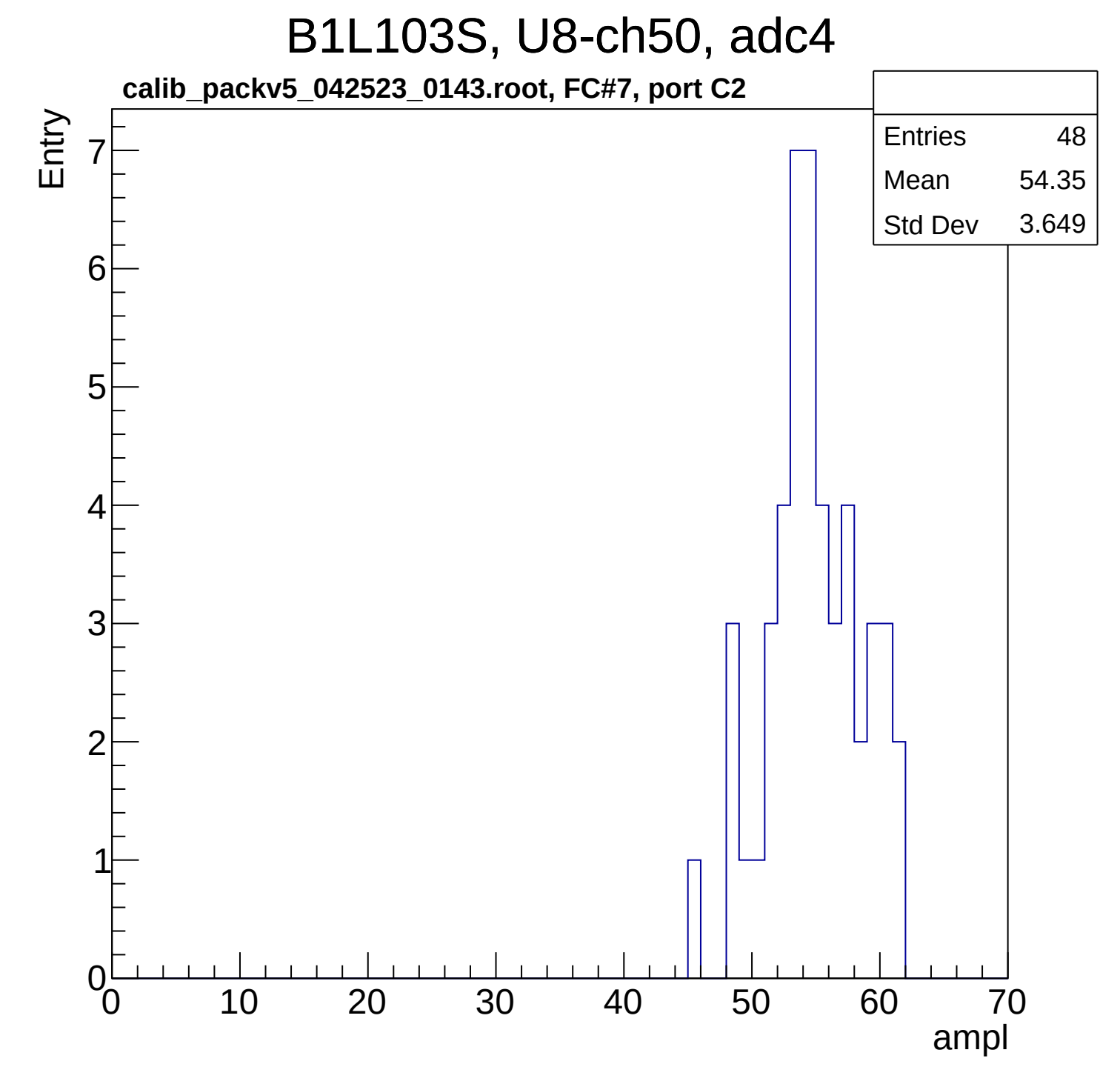

B1L103S, U8-ch49, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

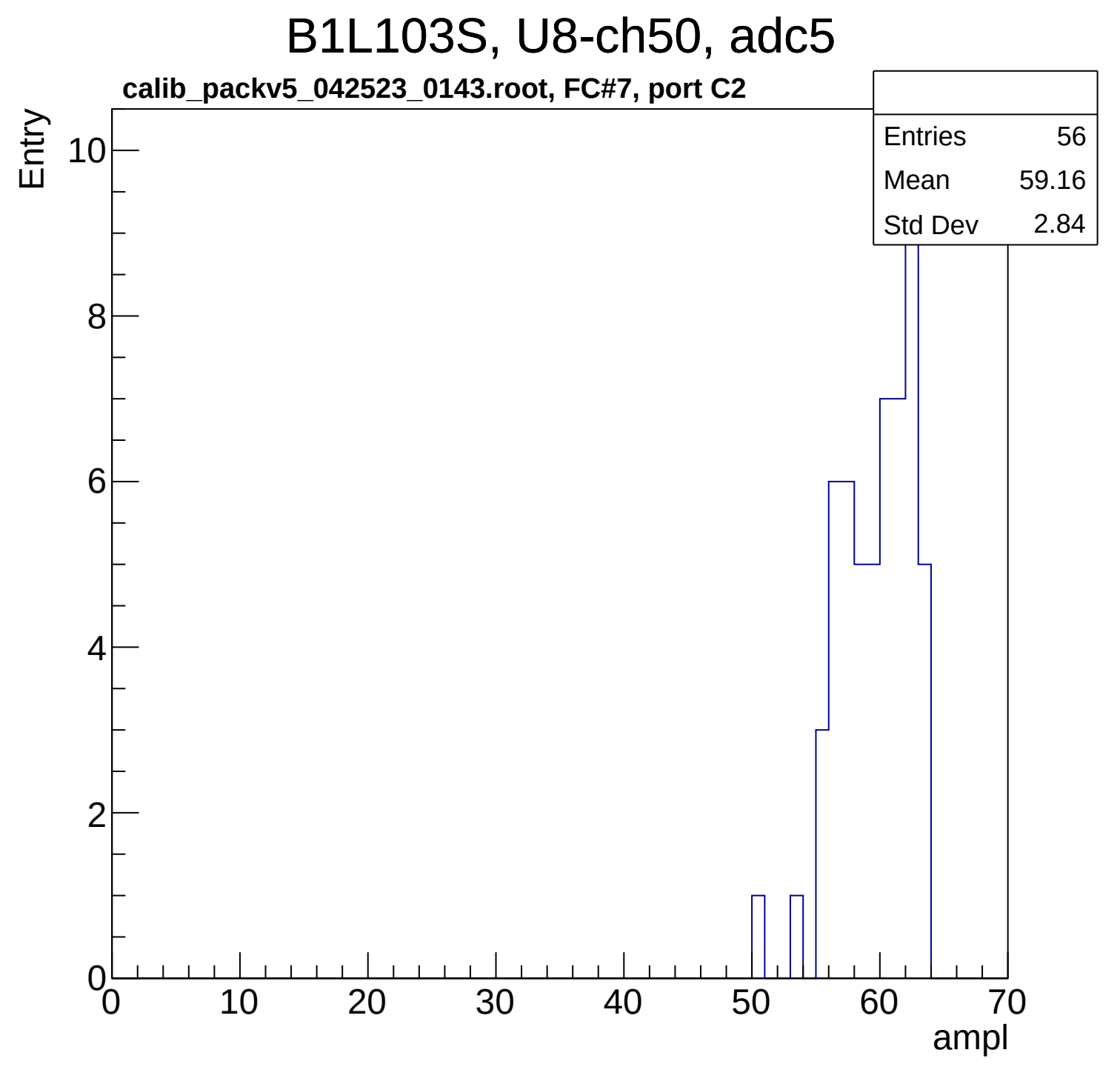

B1L103S, U8-ch50, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 28.77
Std Dev 3.311
Gaus mean : 29.6721
Gaus Width: 3.6737
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

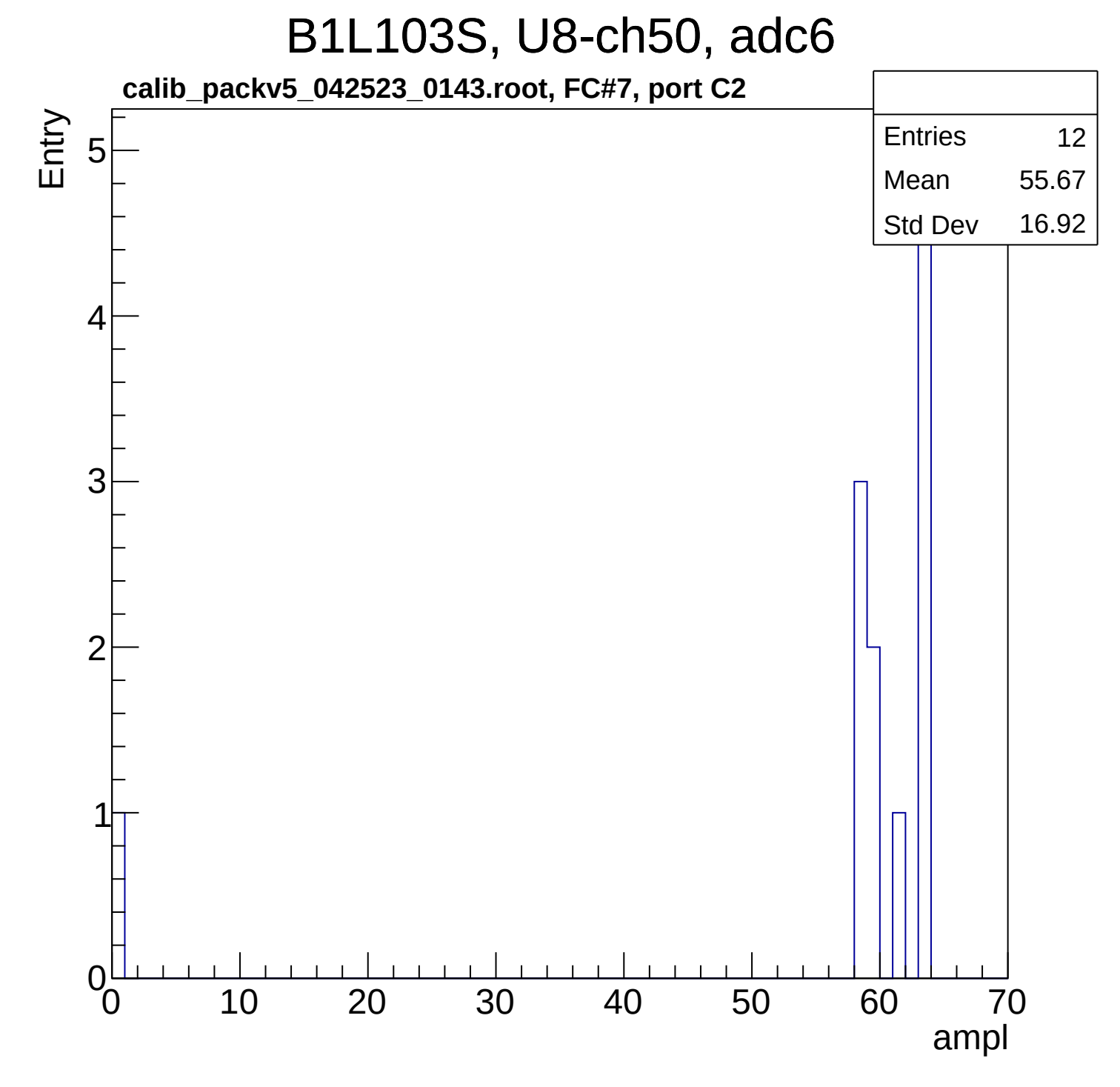

B1L103S, U8-ch50, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 36.03
Std Dev 3.464
Gaus mean : 37.1005
Gaus Width: 3.7239
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

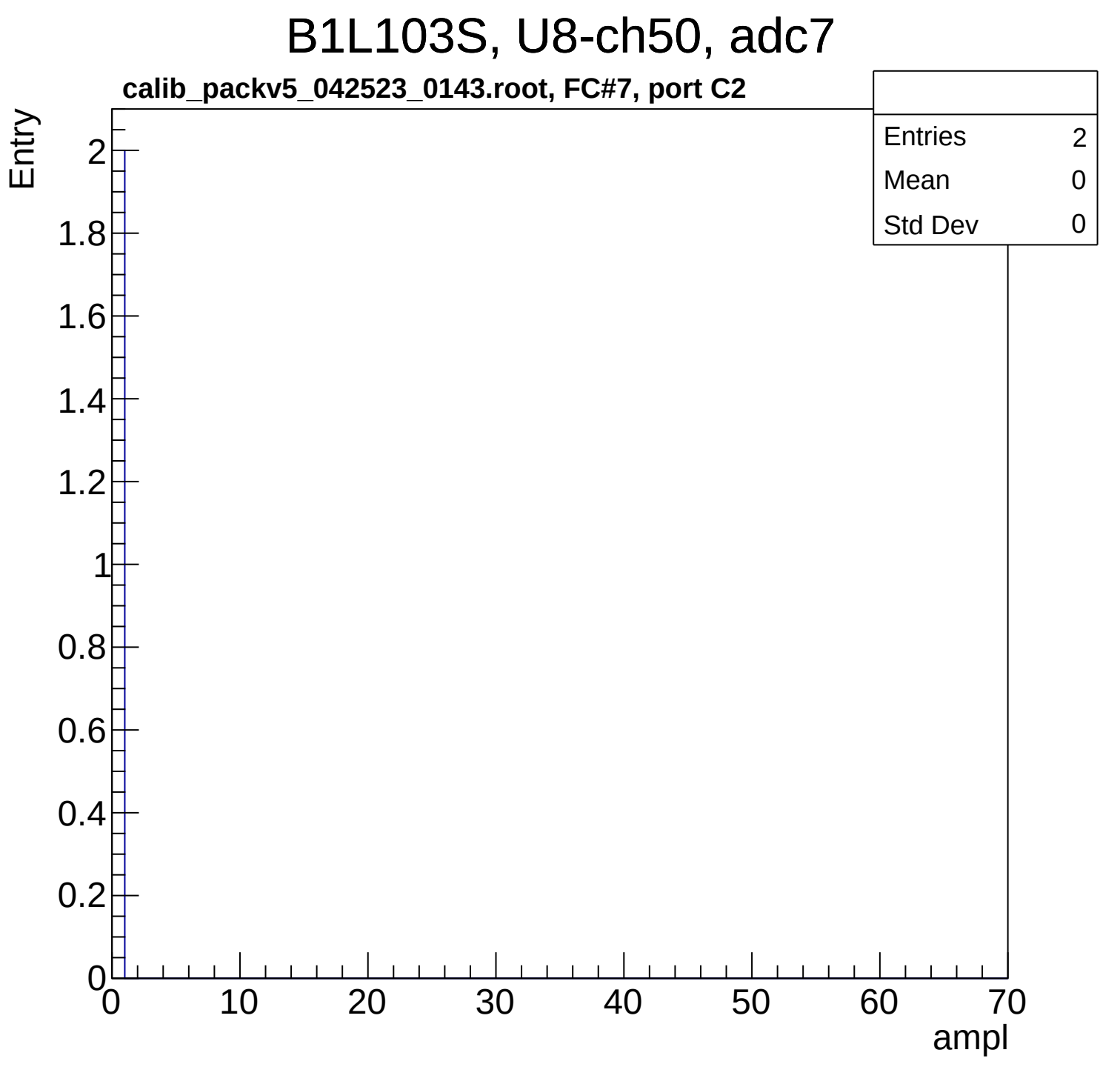

B1L103S, U8-ch50, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 45
Mean 41.56
Std Dev 2.841
Gaus mean : 42.9042
Gaus Width: 3.6449
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

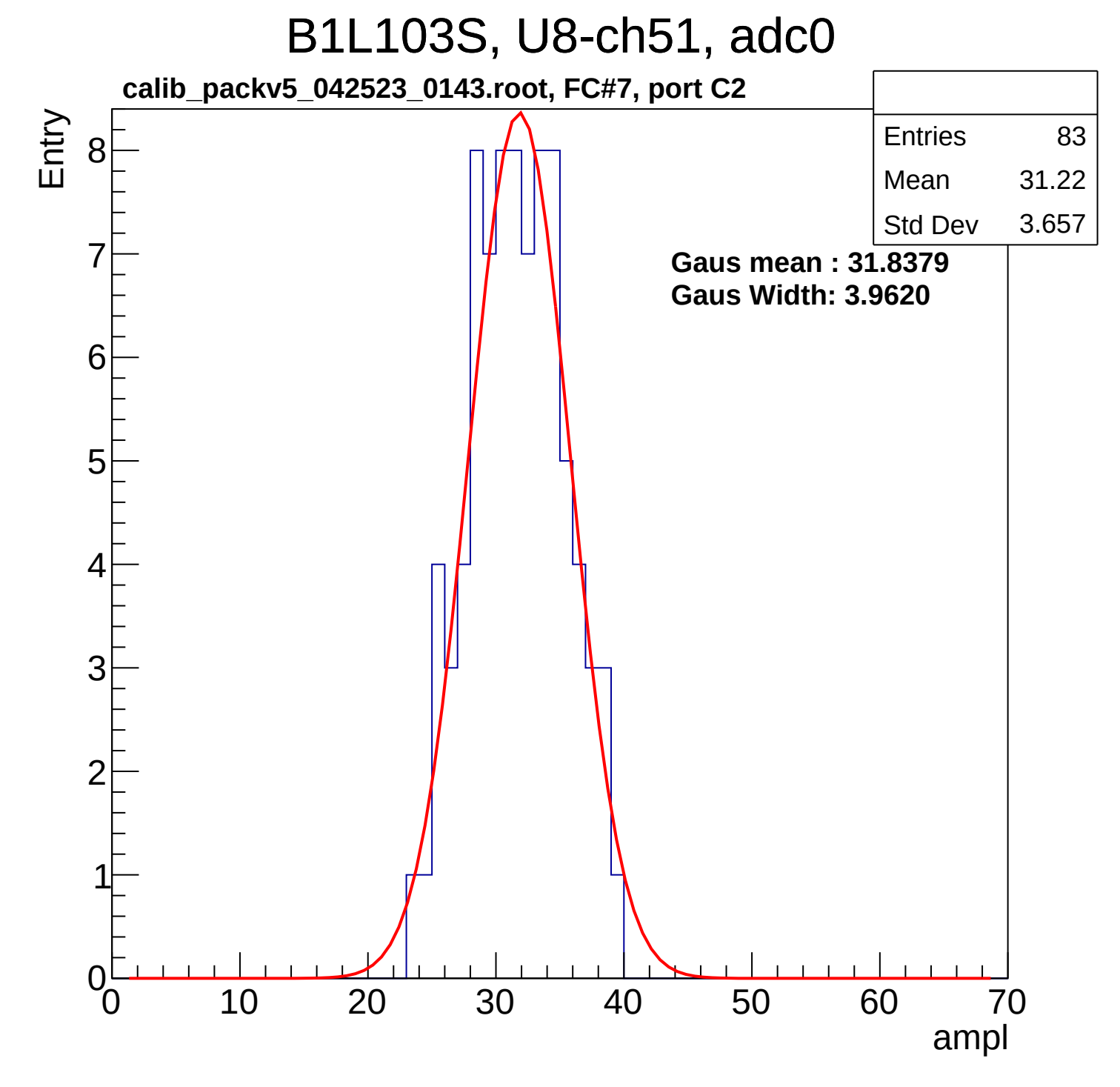

B1L103S, U8-ch50, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 48.46
Std Dev 3.411
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

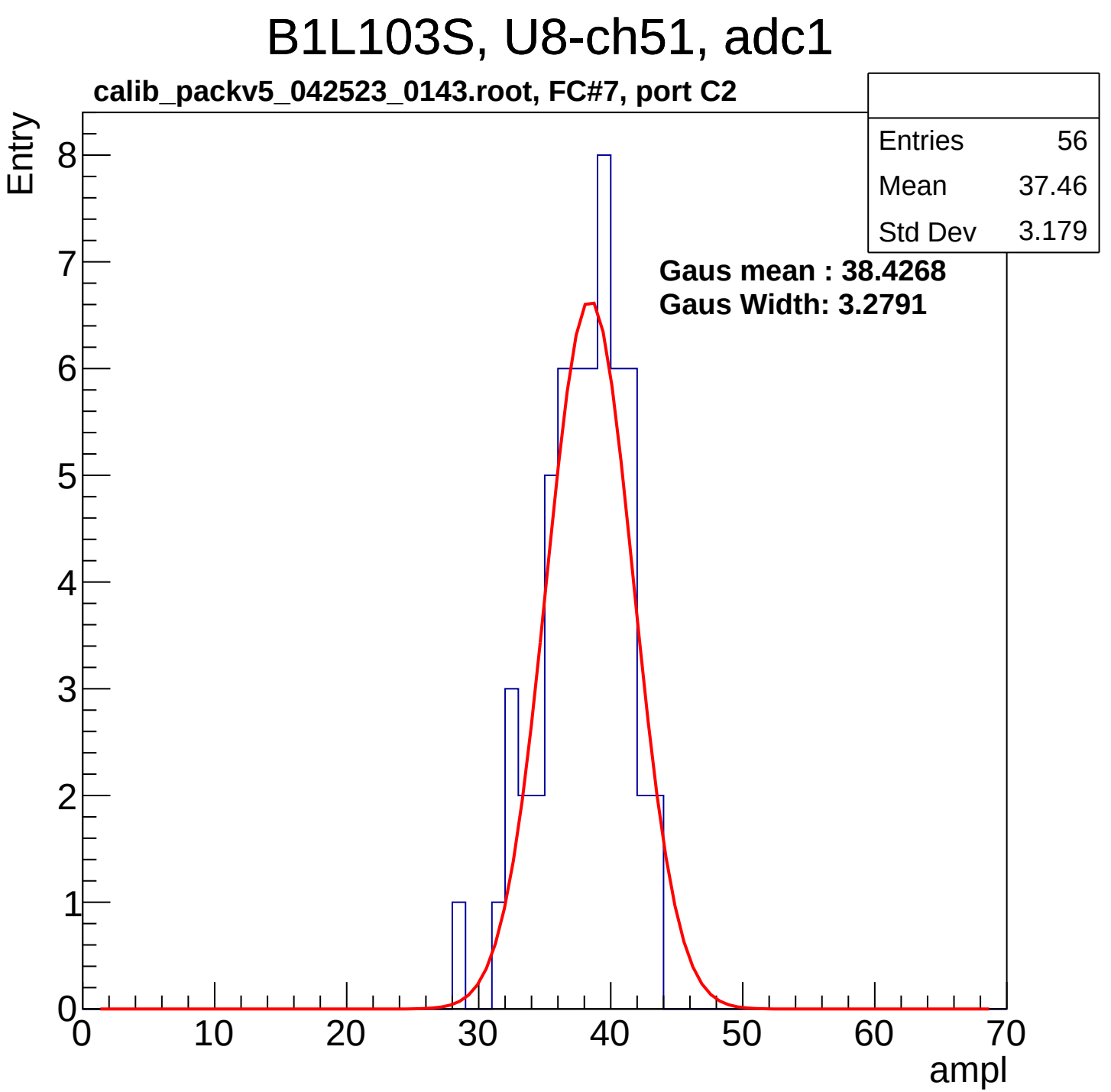

B1L103S, U8-ch50, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 54.35
Std Dev 3.649
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

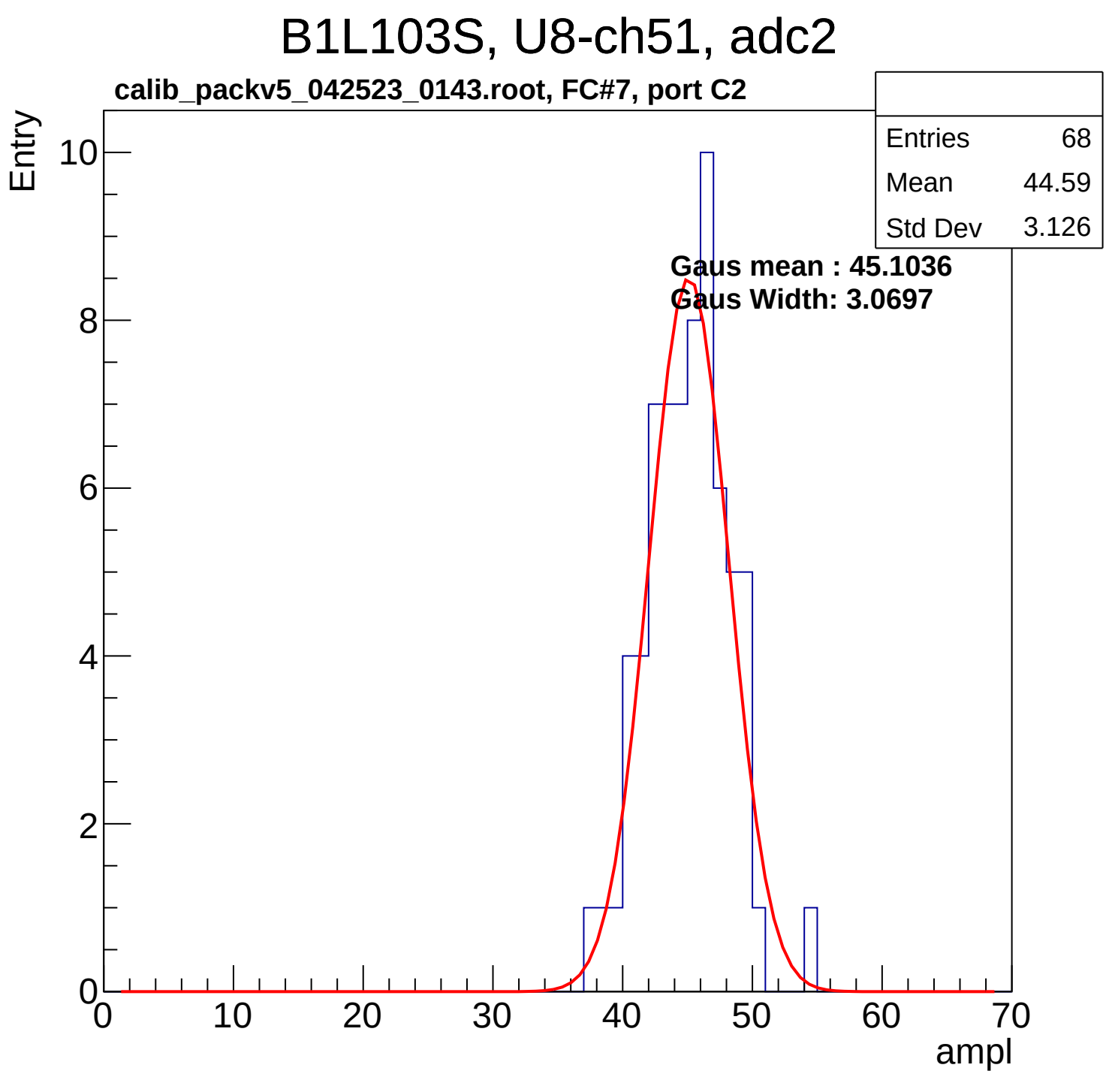

B1L103S, U8-ch50, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 59.16
Std Dev 2.84
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

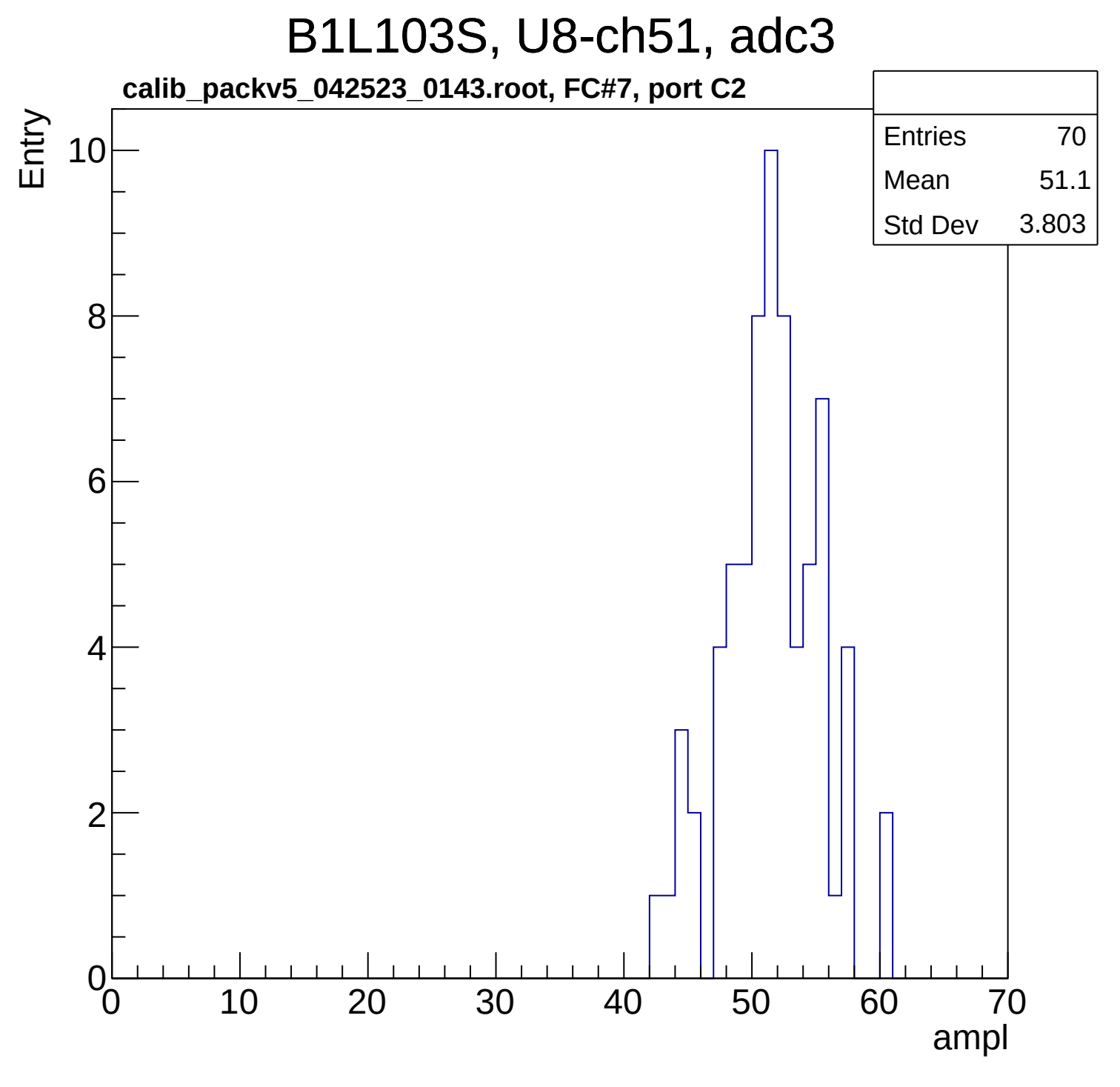

B1L103S, U8-ch50, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 12
Mean 55.67
Std Dev 16.92
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

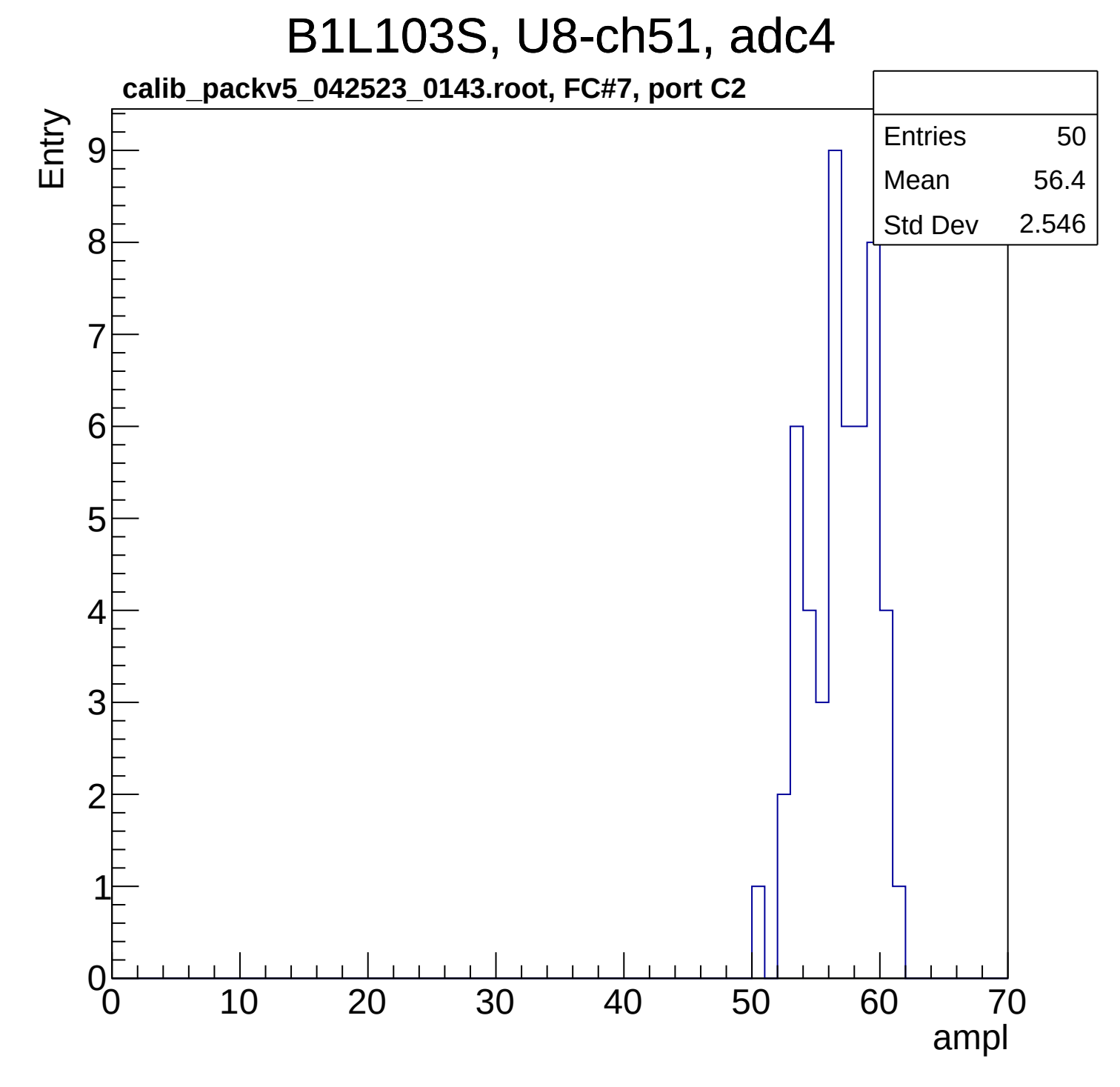

B1L103S, U8-ch50, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

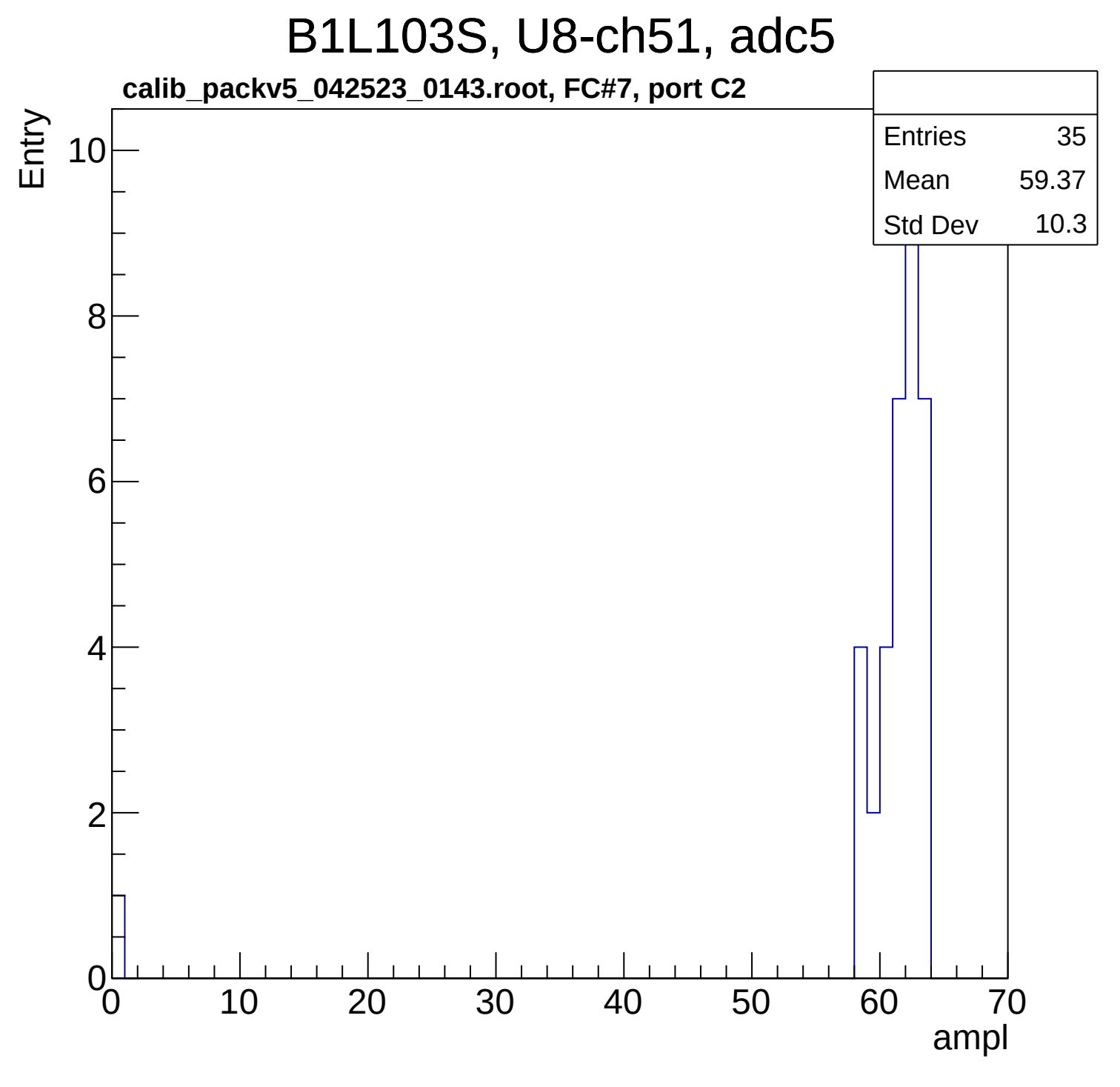

B1L103S, U8-ch51, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 83
Mean 31.22
Std Dev 3.657
Gaus mean : 31.8379
Gaus Width: 3.9620
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

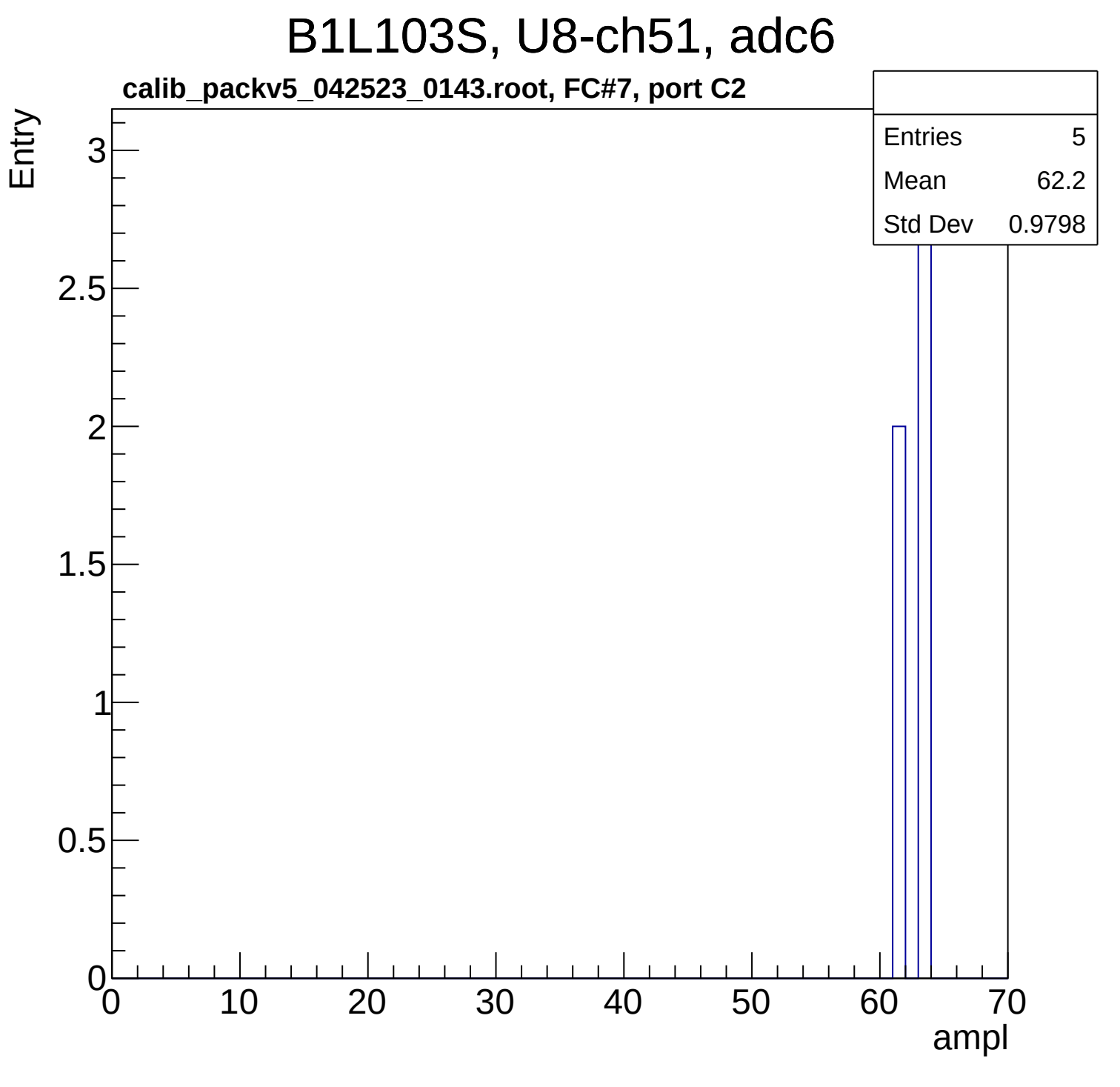

B1L103S, U8-ch51, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 37.46
Std Dev 3.179
Gaus mean : 38.4268
Gaus Width: 3.2791
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

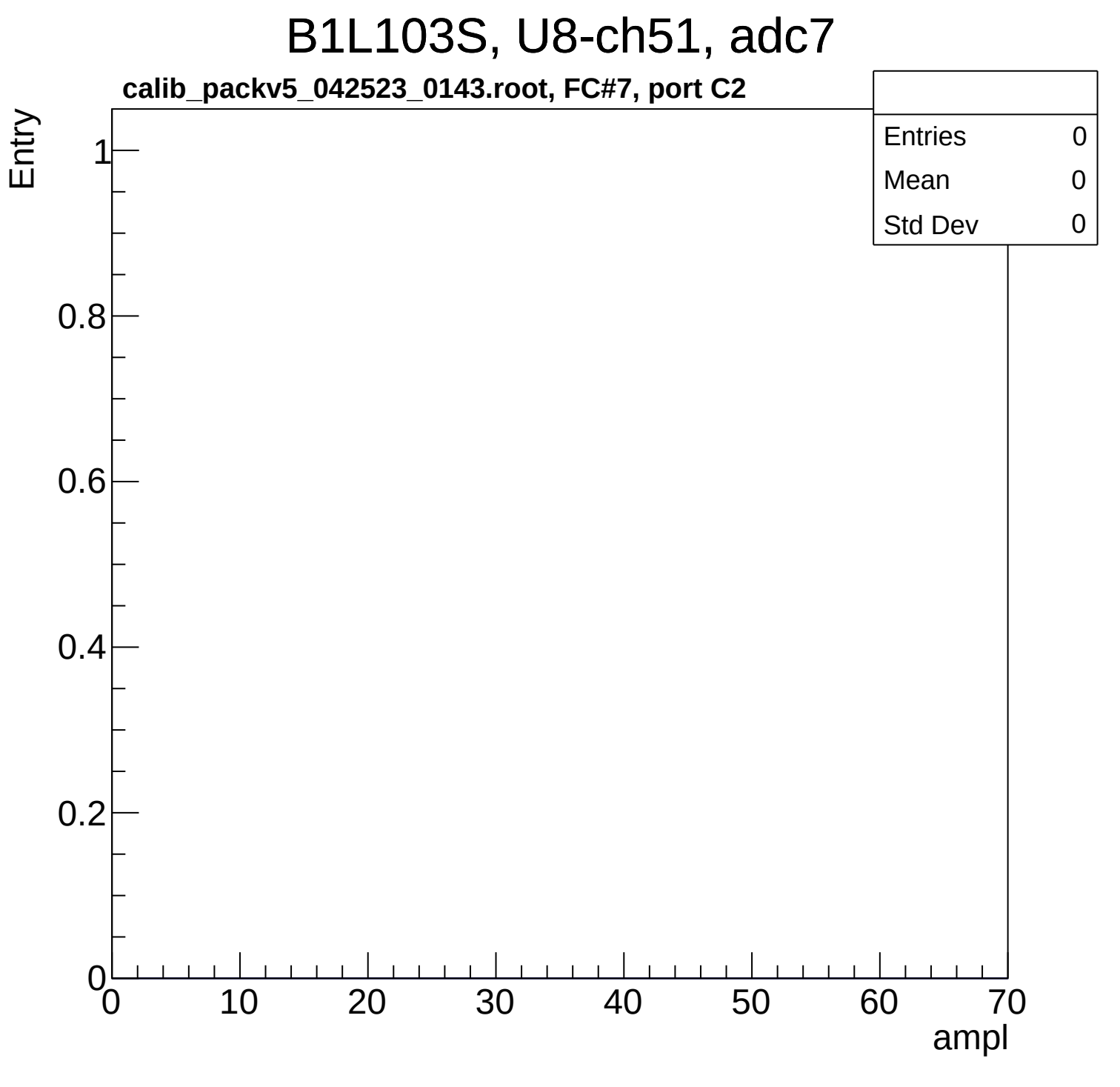

B1L103S, U8-ch51, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 44.59
Std Dev 3.126
Gaus mean : 45.1036
Gaus Width: 3.0697
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

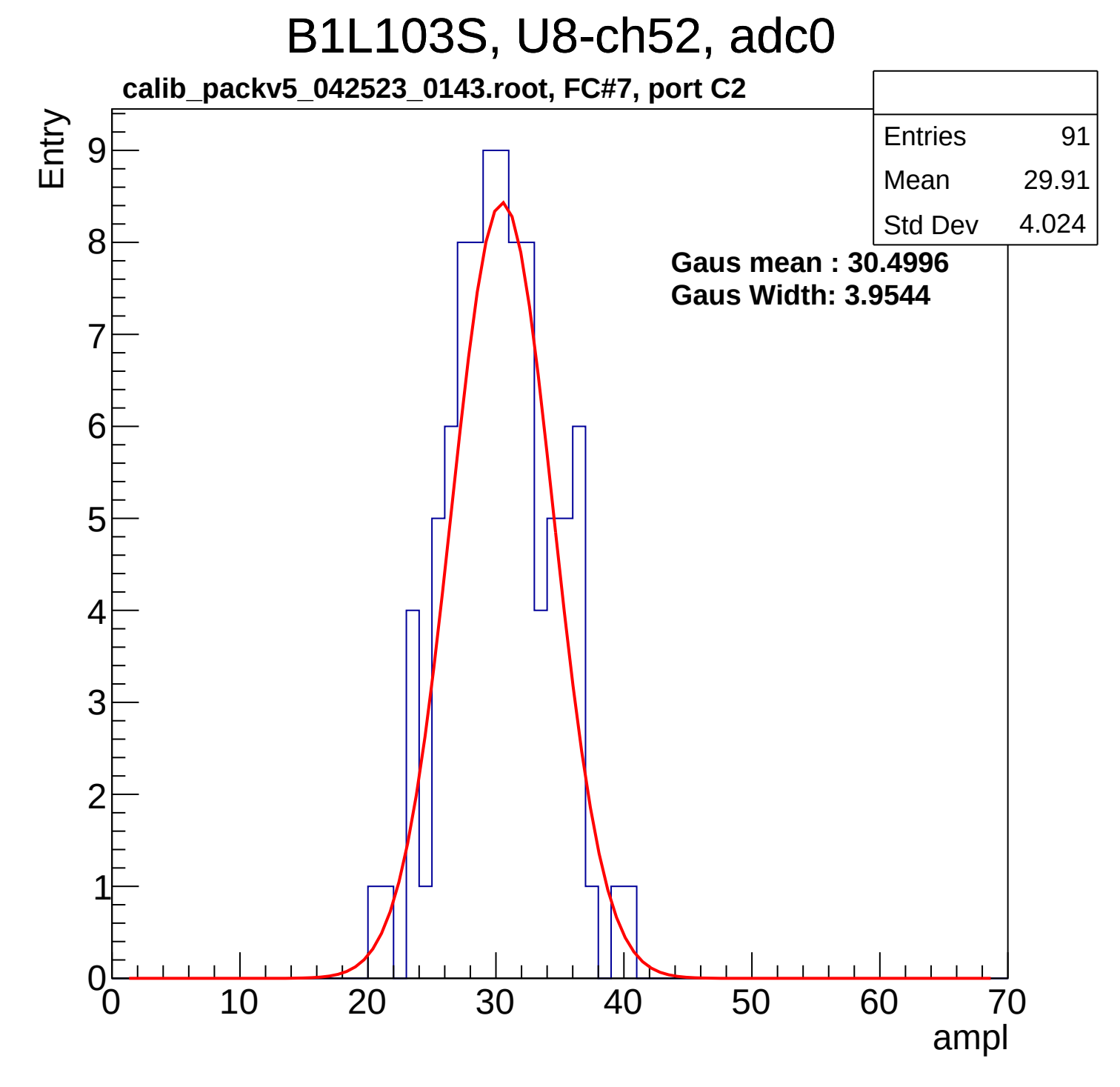

B1L103S, U8-ch51, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 51.1
Std Dev 3.803
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

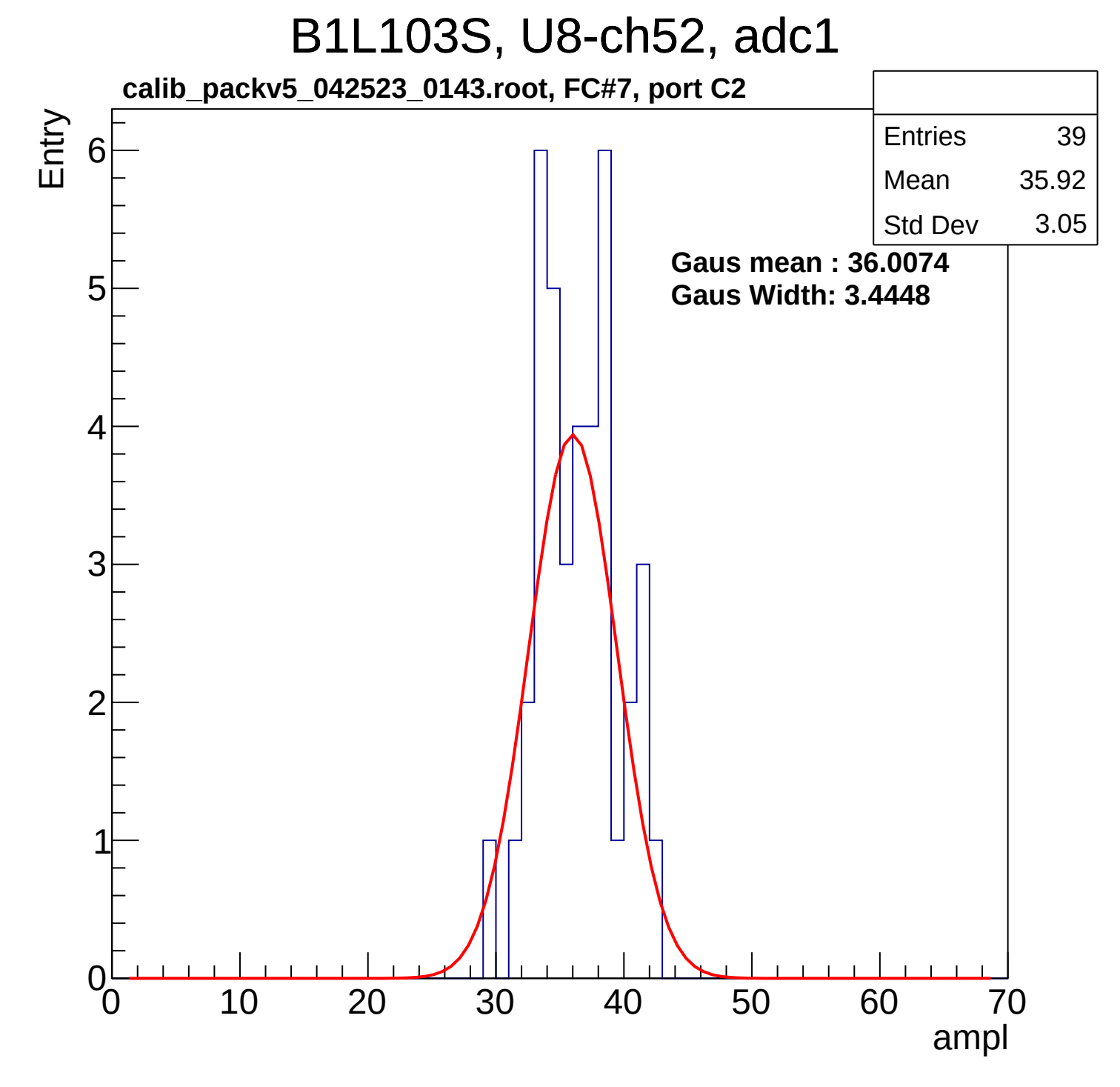

B1L103S, U8-ch51, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 56.4
Std Dev 2.546
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

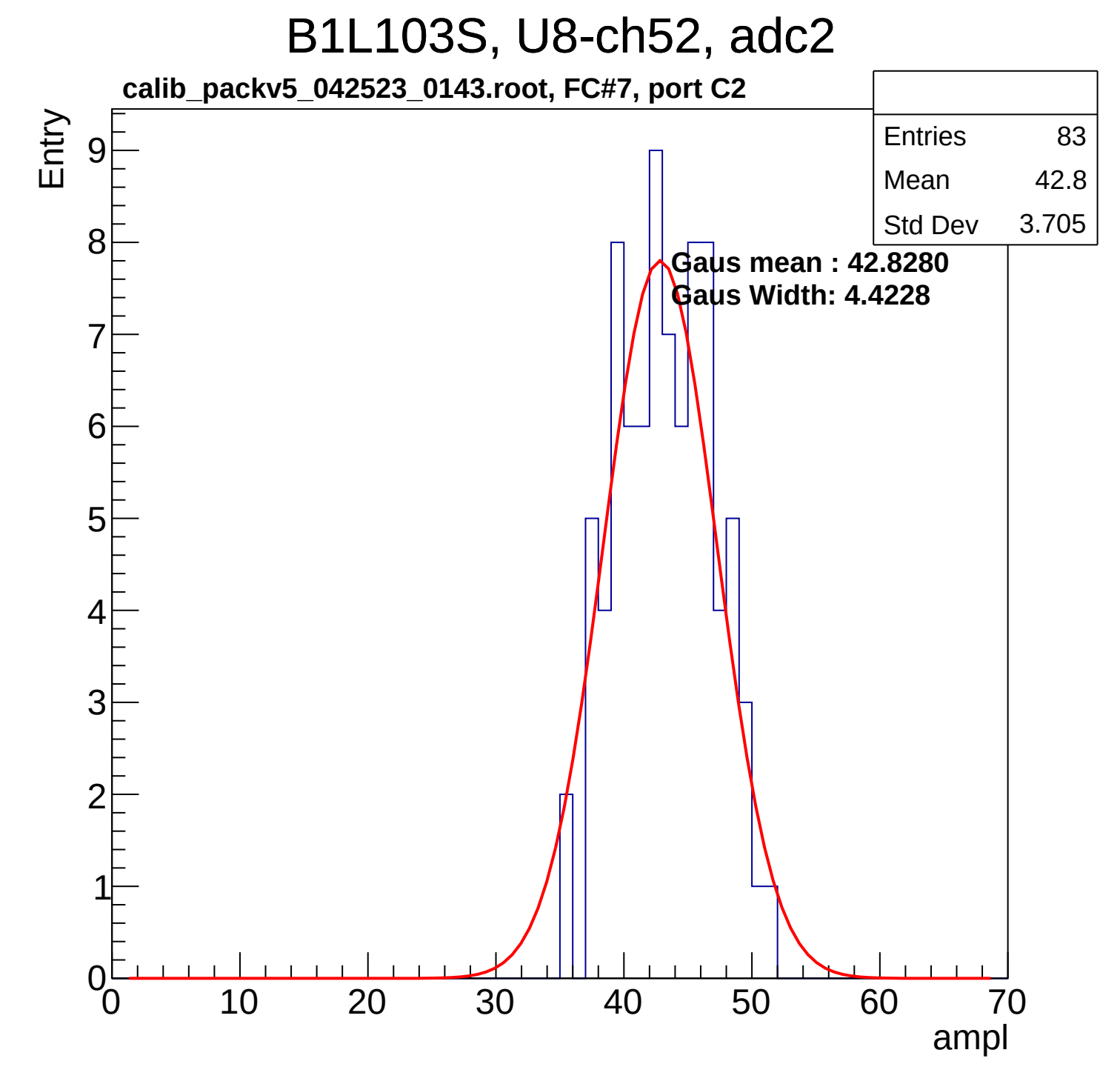

B1L103S, U8-ch51, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 35
Mean 59.37
Std Dev 10.3
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

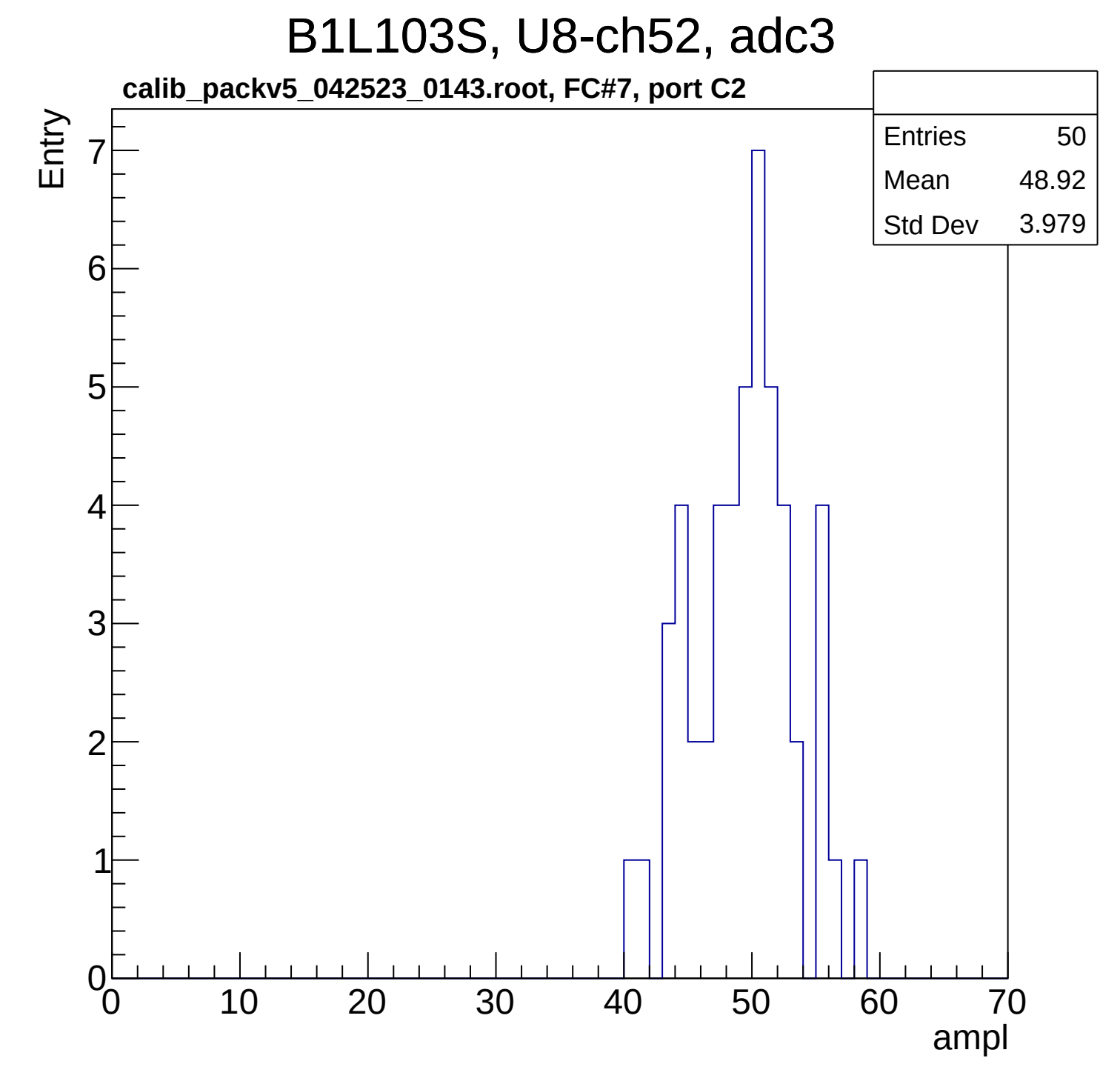

B1L103S, U8-ch51, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 62.2
Std Dev 0.9798
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

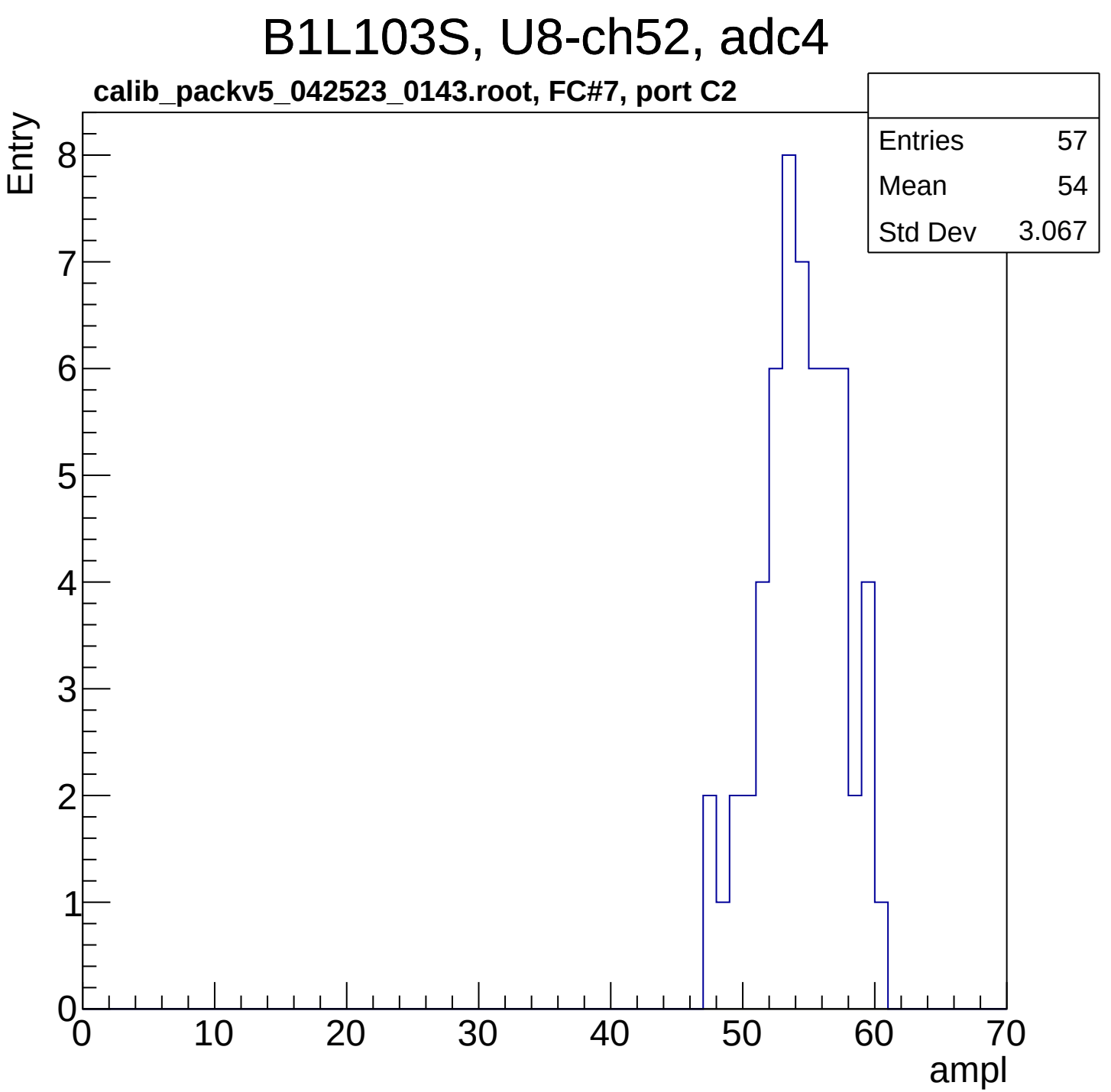

B1L103S, U8-ch51, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

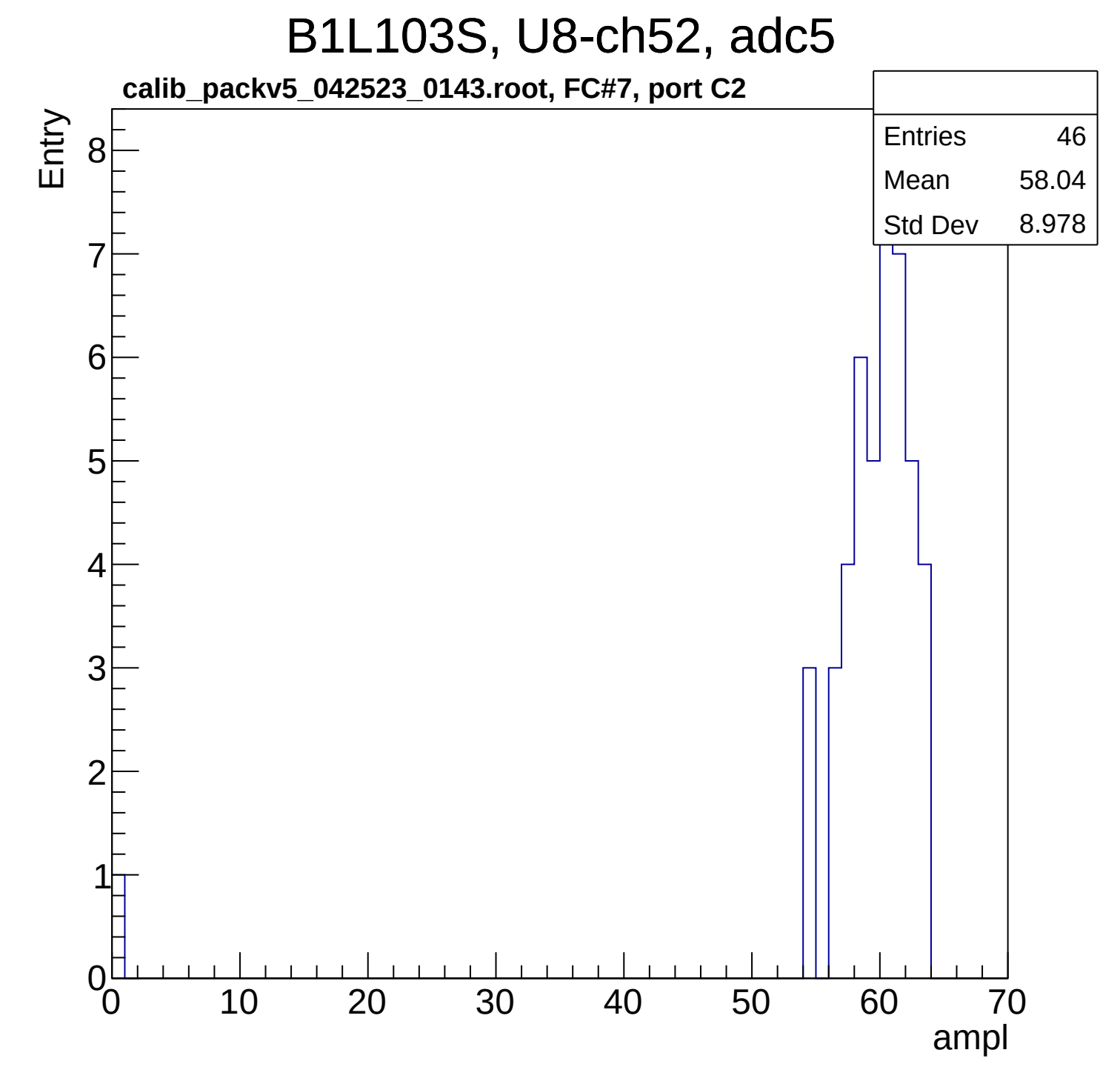

B1L103S, U8-ch52, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 91
Mean 29.91
Std Dev 4.024
Gaus mean : 30.4996
Gaus Width: 3.9544
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

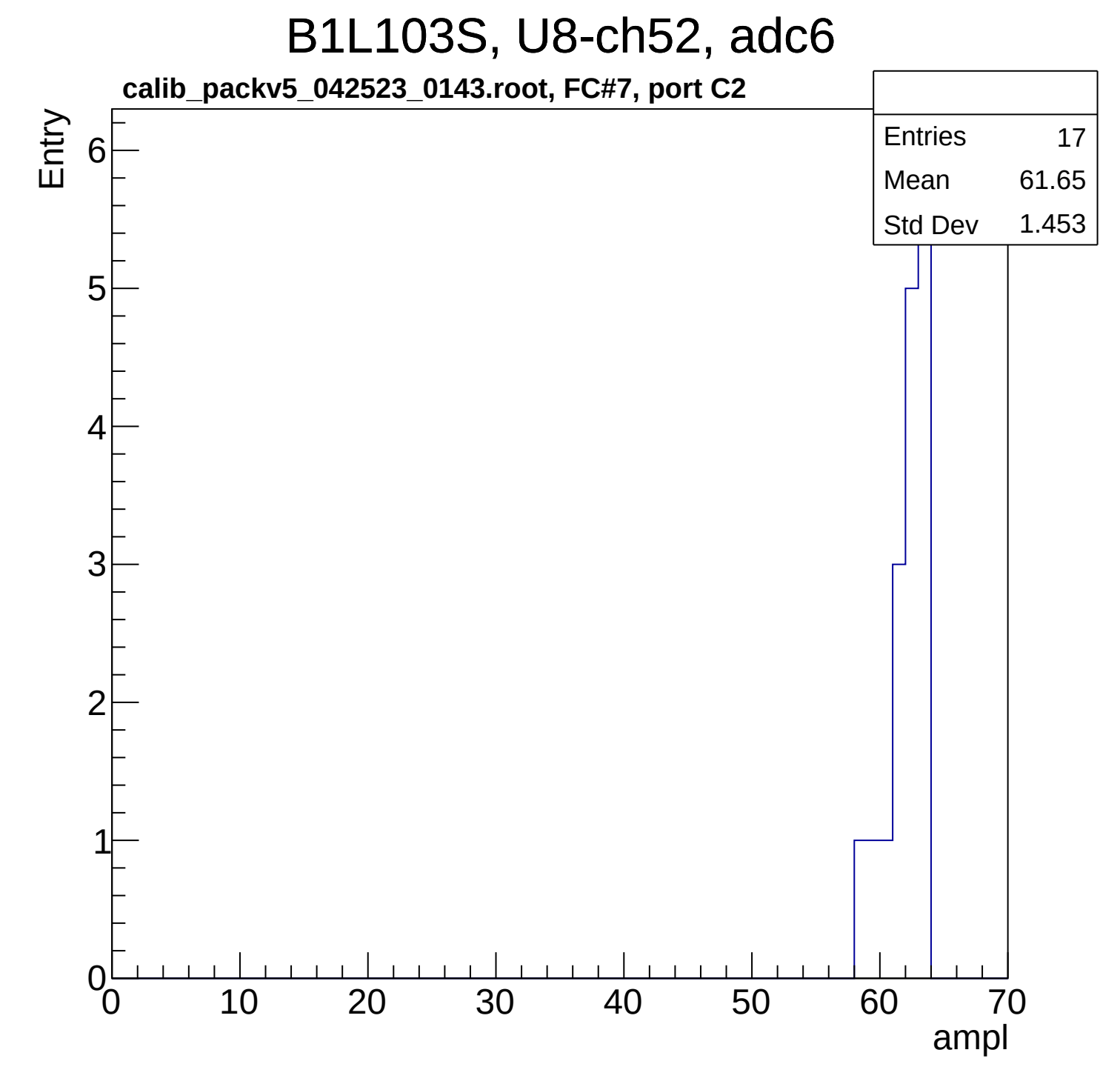

B1L103S, U8-ch52, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 39
Mean 35.92
Std Dev 3.05
Gaus mean : 36.0074
Gaus Width: 3.4448
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

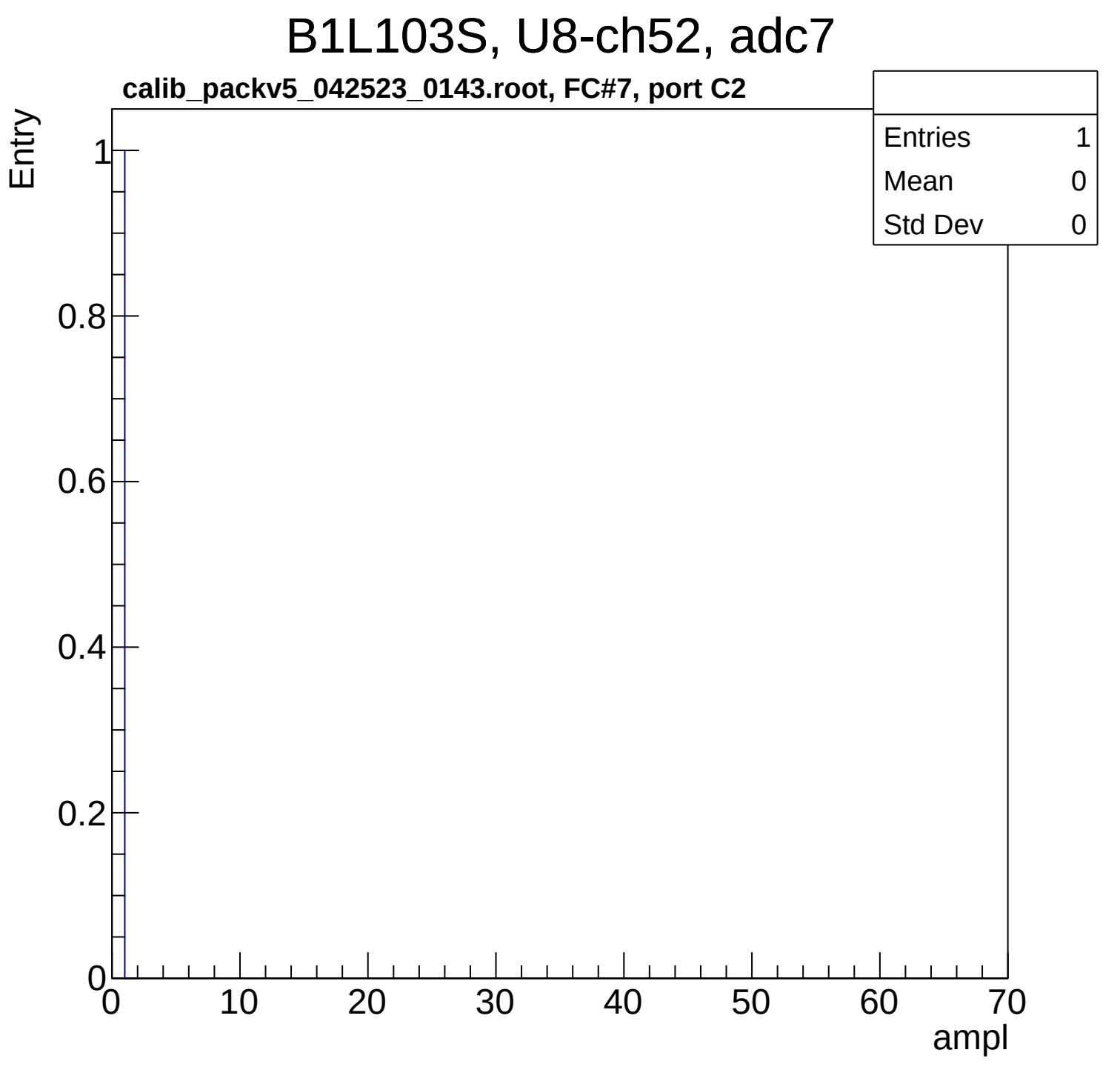

B1L103S, U8-ch52, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 83
Mean 42.8
Std Dev 3.705
Gaus mean : 42.8280
Gaus Width: 4.4228
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

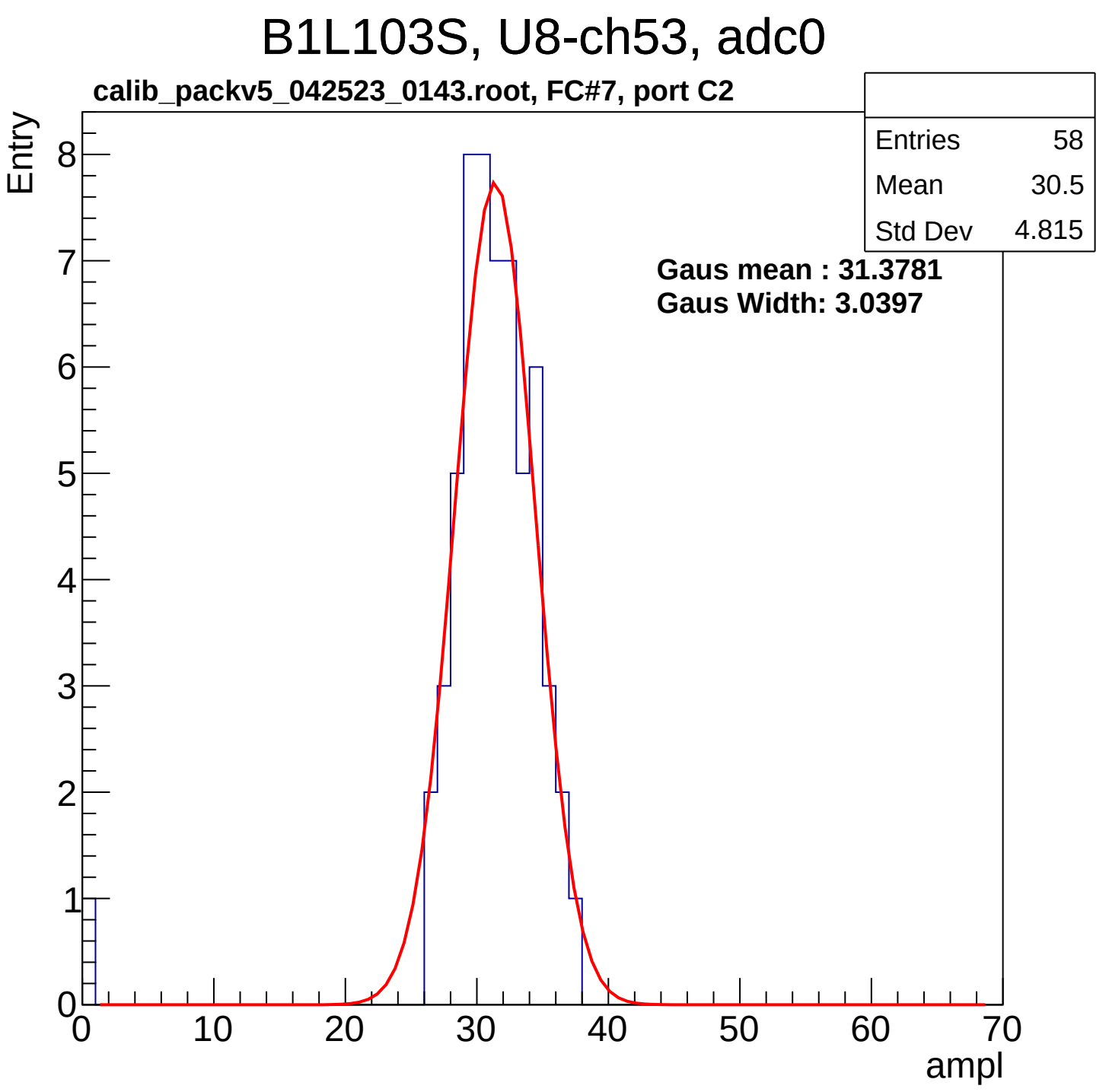

B1L103S, U8-ch52, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 48.92
Std Dev 3.979
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

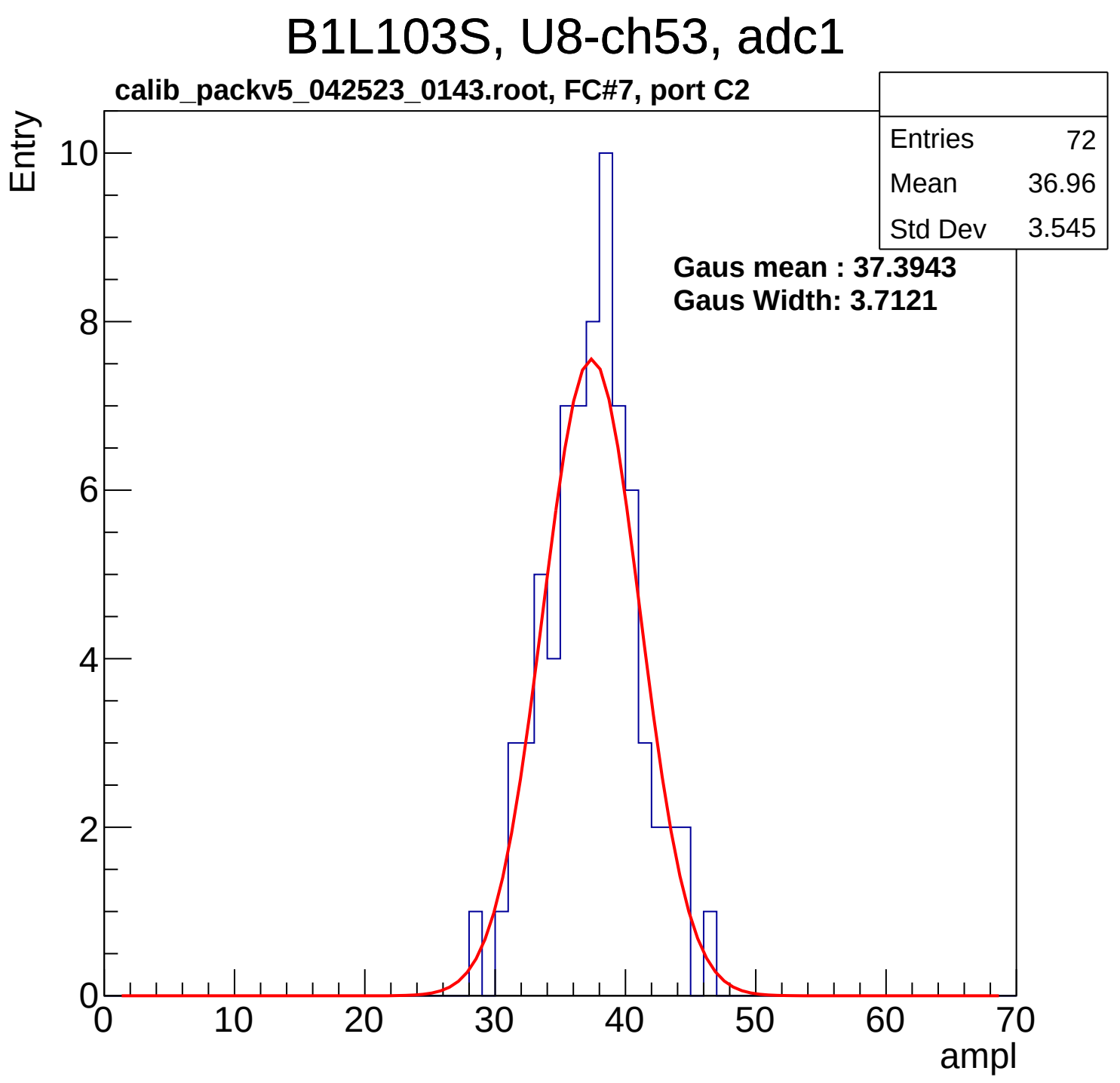

B1L103S, U8-ch52, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 54
Std Dev 3.067
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

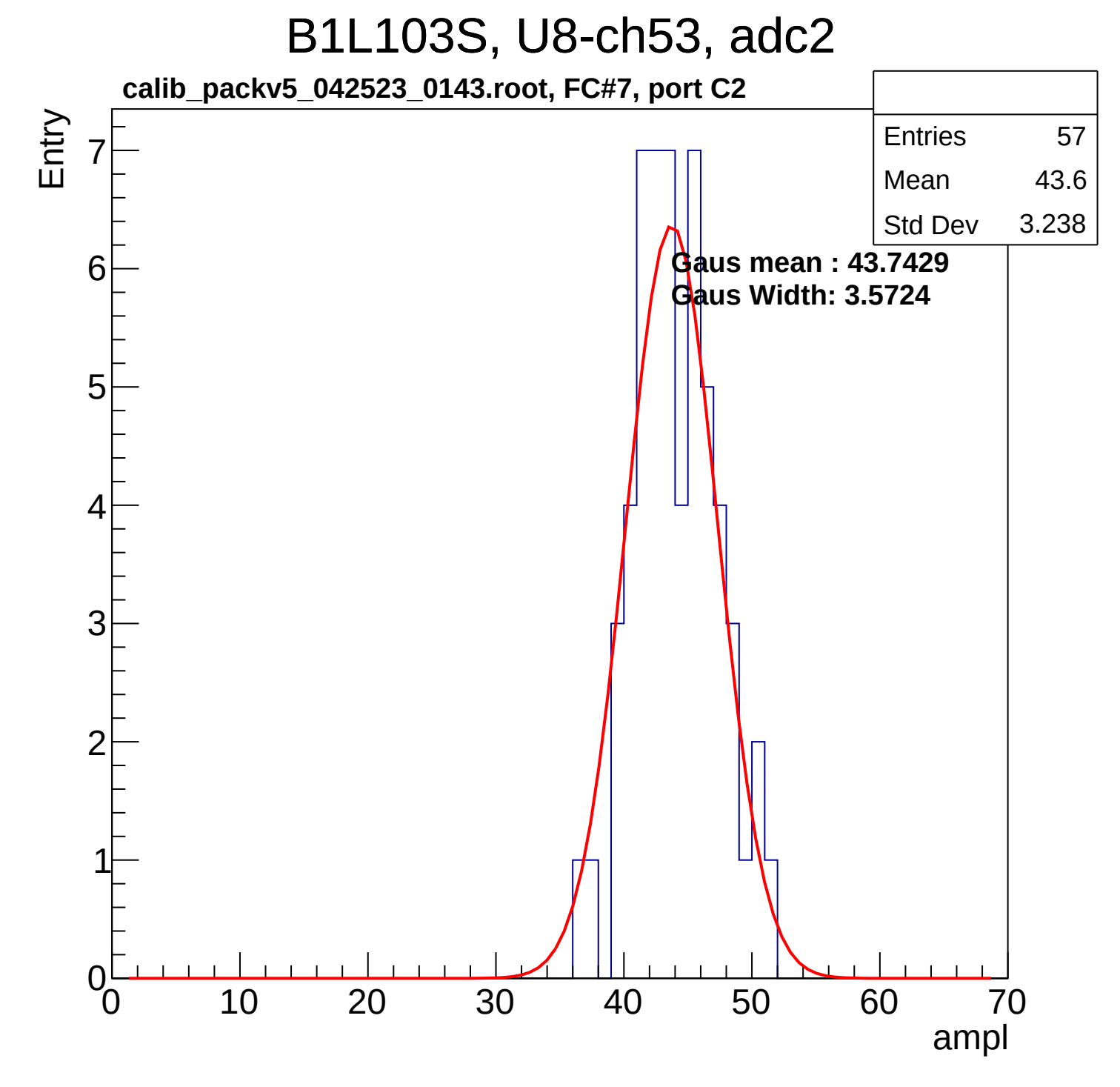

B1L103S, U8-ch52, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 46
Mean 58.04
Std Dev 8.978
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

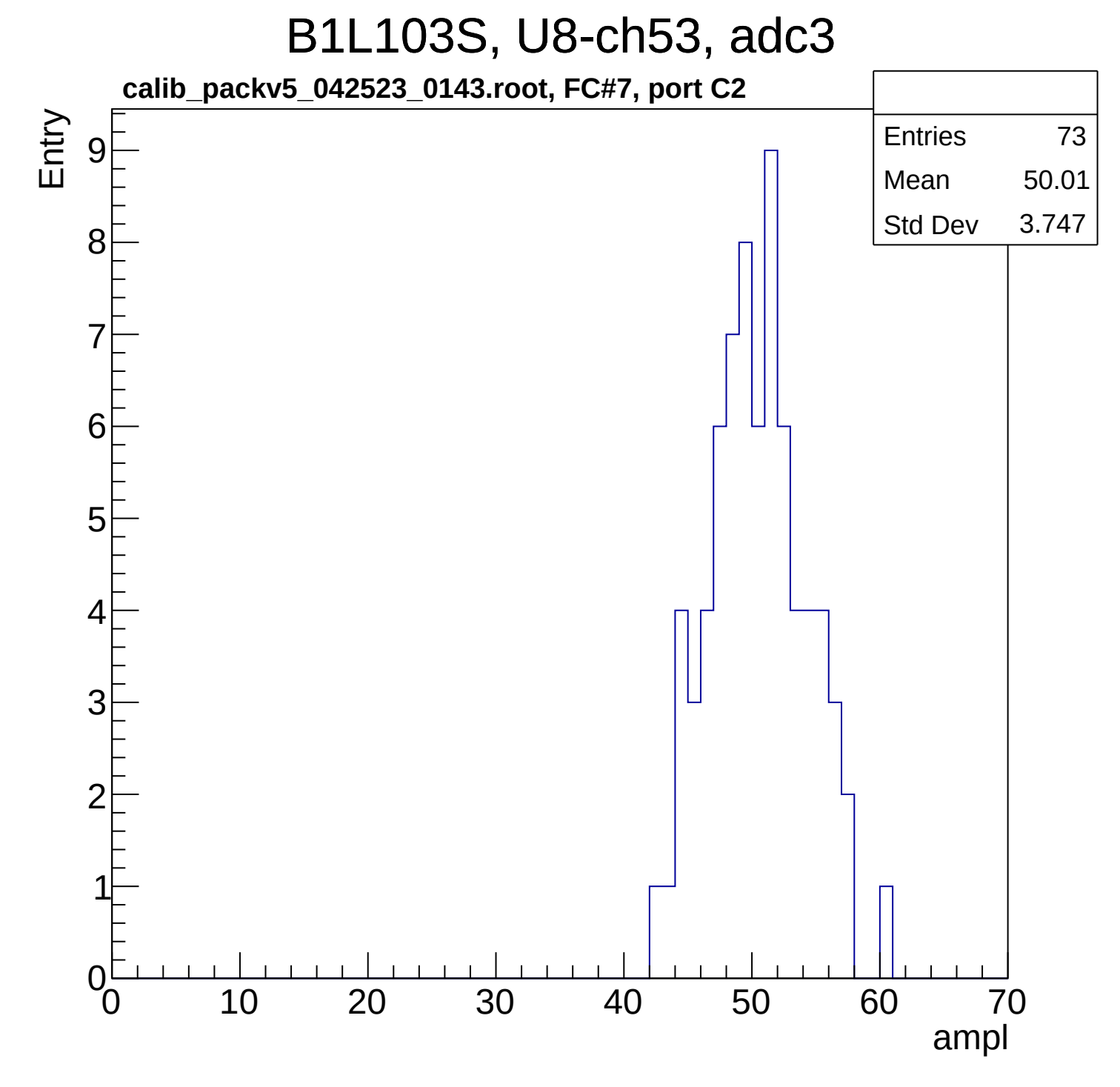

B1L103S, U8-ch52, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 17
Mean 61.65
Std Dev 1.453
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

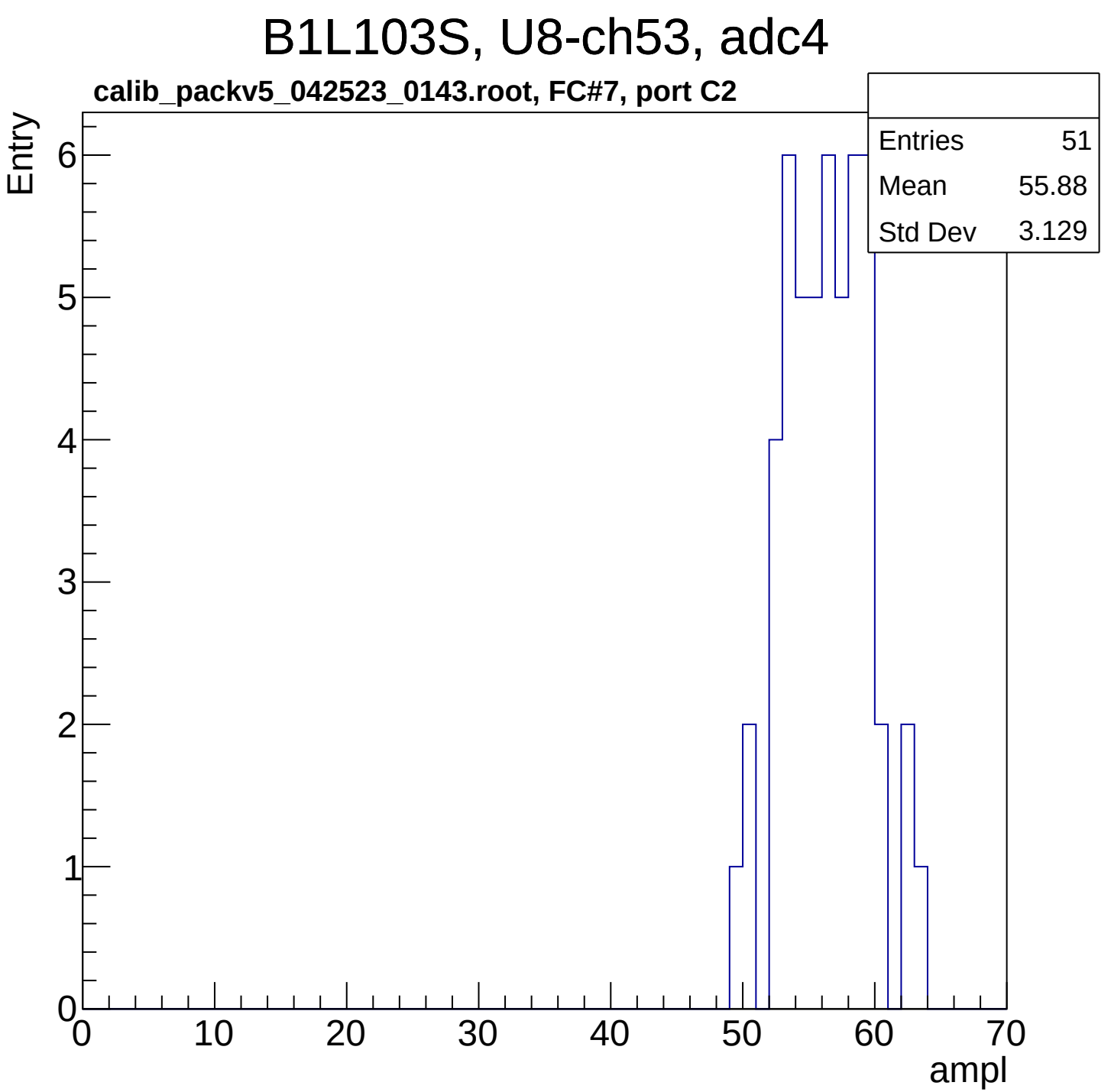

B1L103S, U8-ch52, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

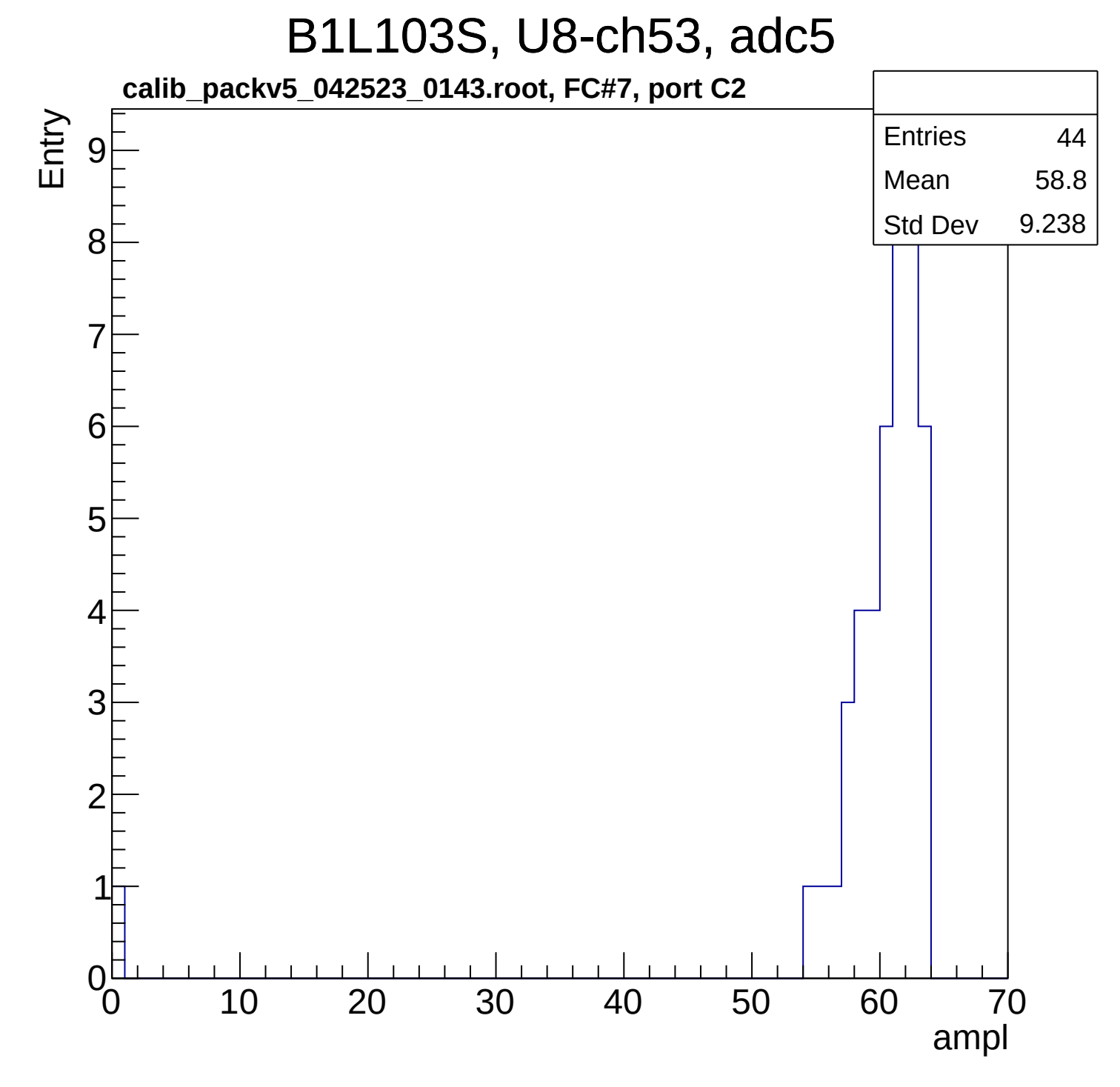

B1L103S, U8-ch53, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 30.5
Std Dev 4.815
Gaus mean : 31.3781
Gaus Width: 3.0397
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

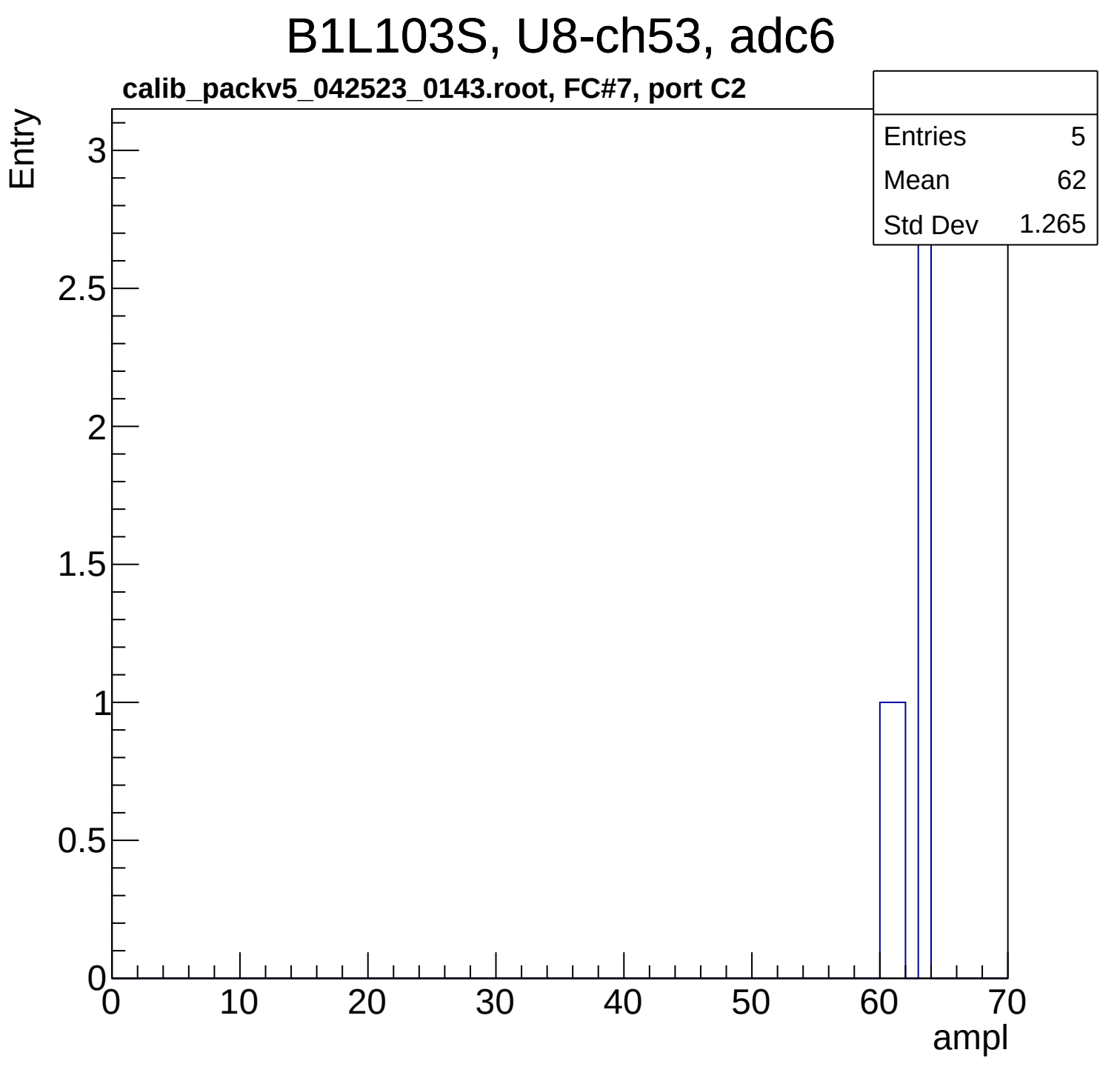

B1L103S, U8-ch53, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 36.96
Std Dev 3.545
Gaus mean : 37.3943
Gaus Width: 3.7121
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

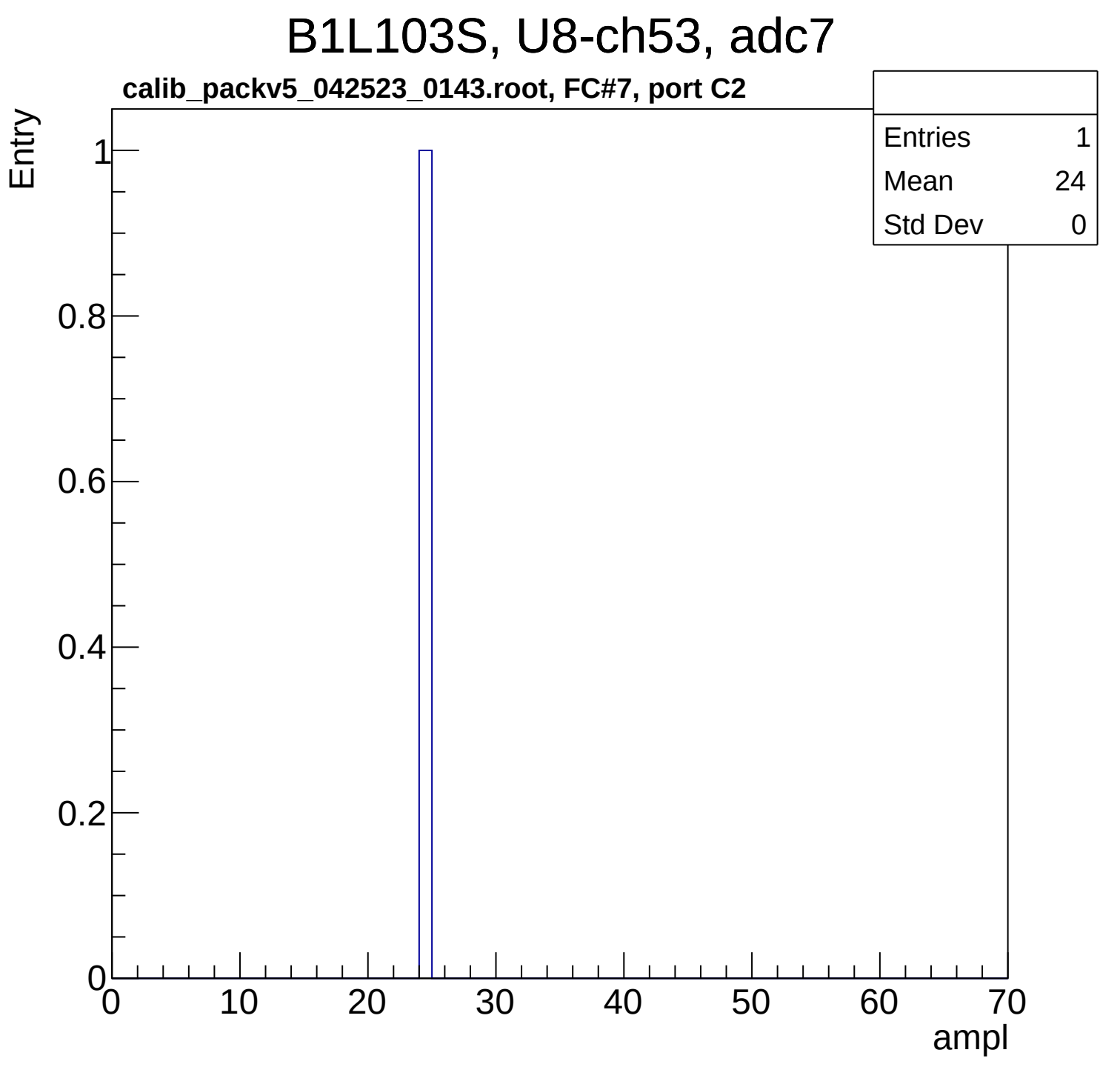

B1L103S, U8-ch53, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 43.6
Std Dev 3.238
Gaus mean : 43.7429
Gaus Width: 3.5724
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

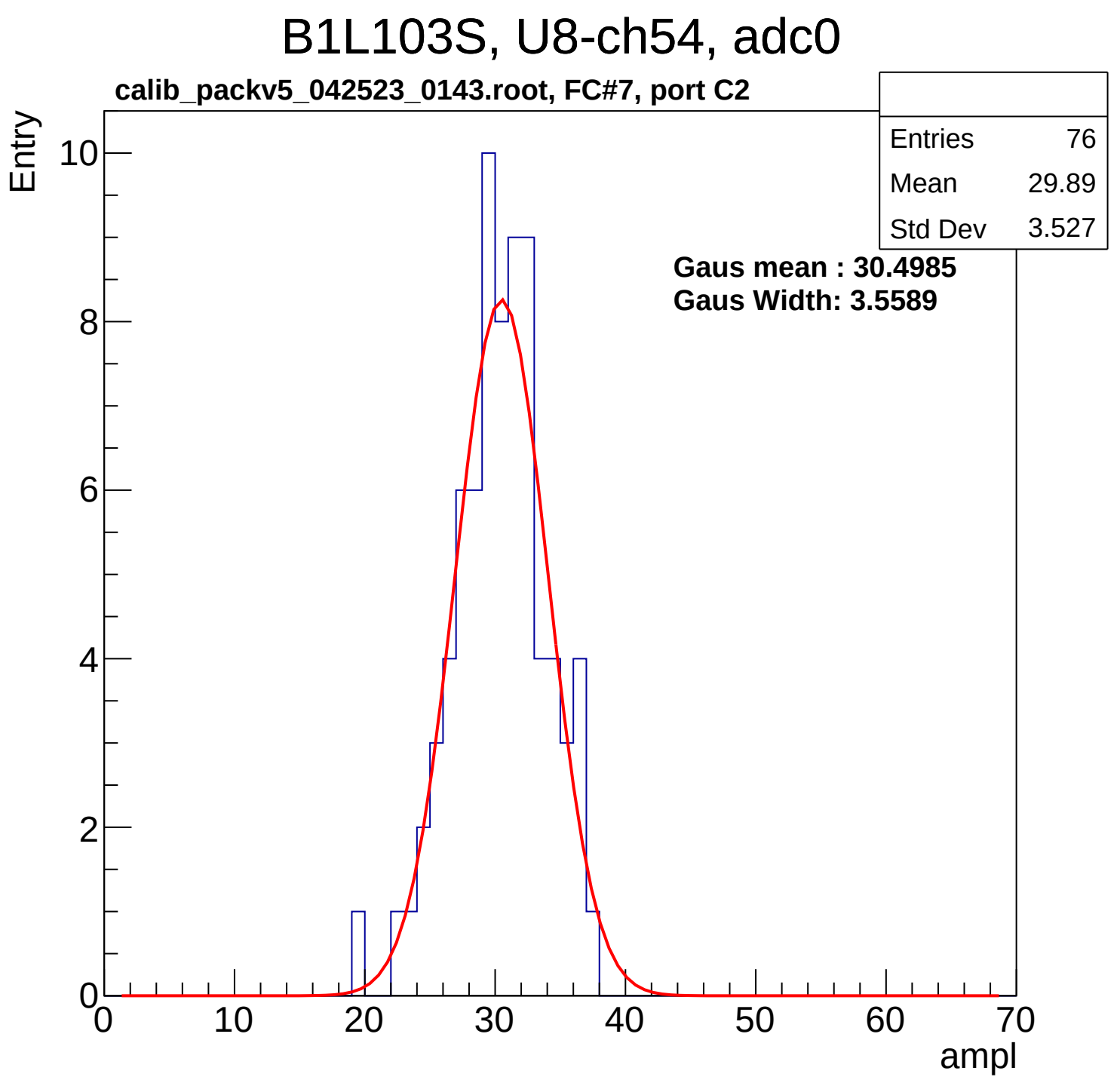

B1L103S, U8-ch53, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 50.01
Std Dev 3.747
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

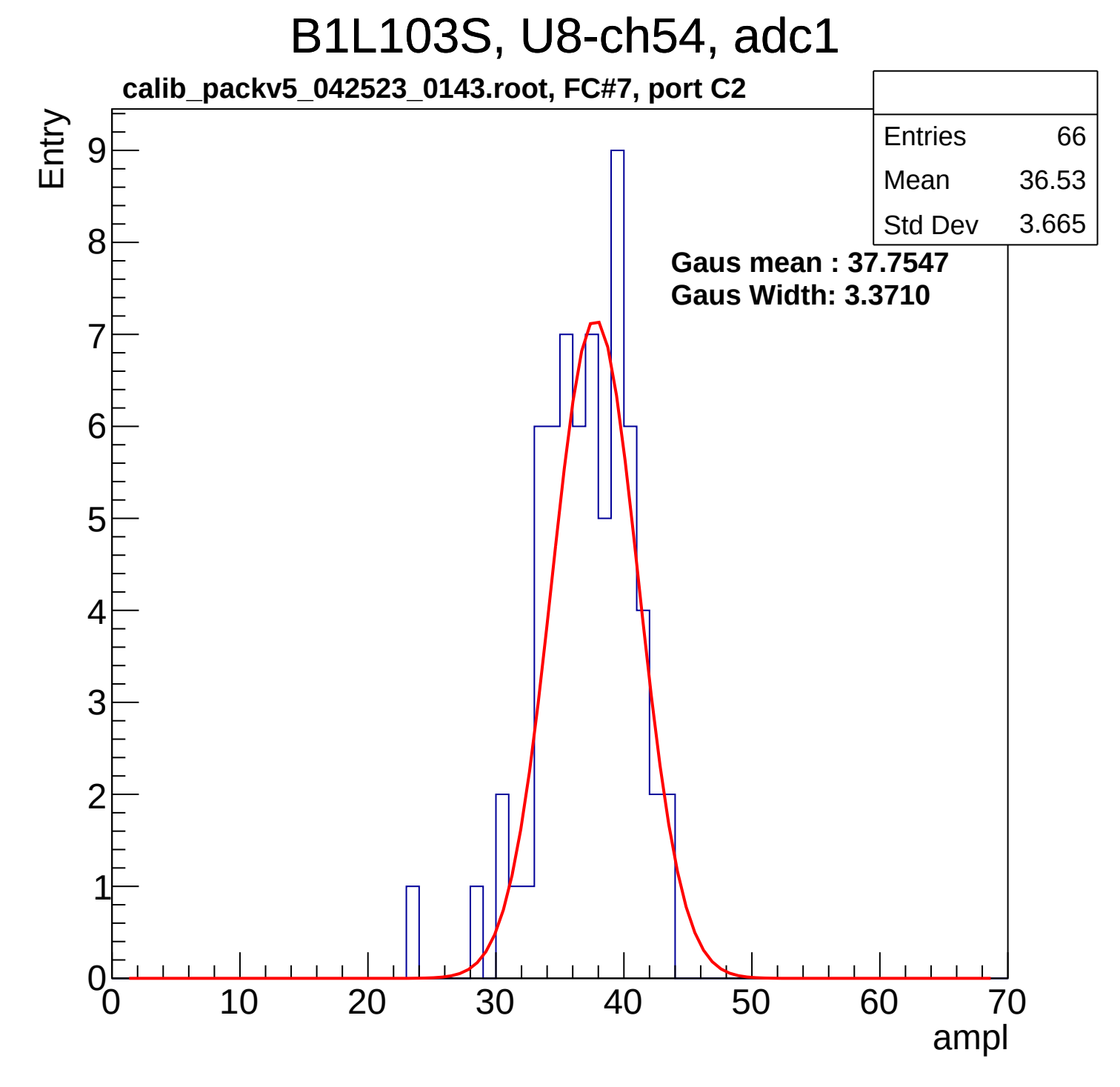

B1L103S, U8-ch53, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 55.88
Std Dev 3.129
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

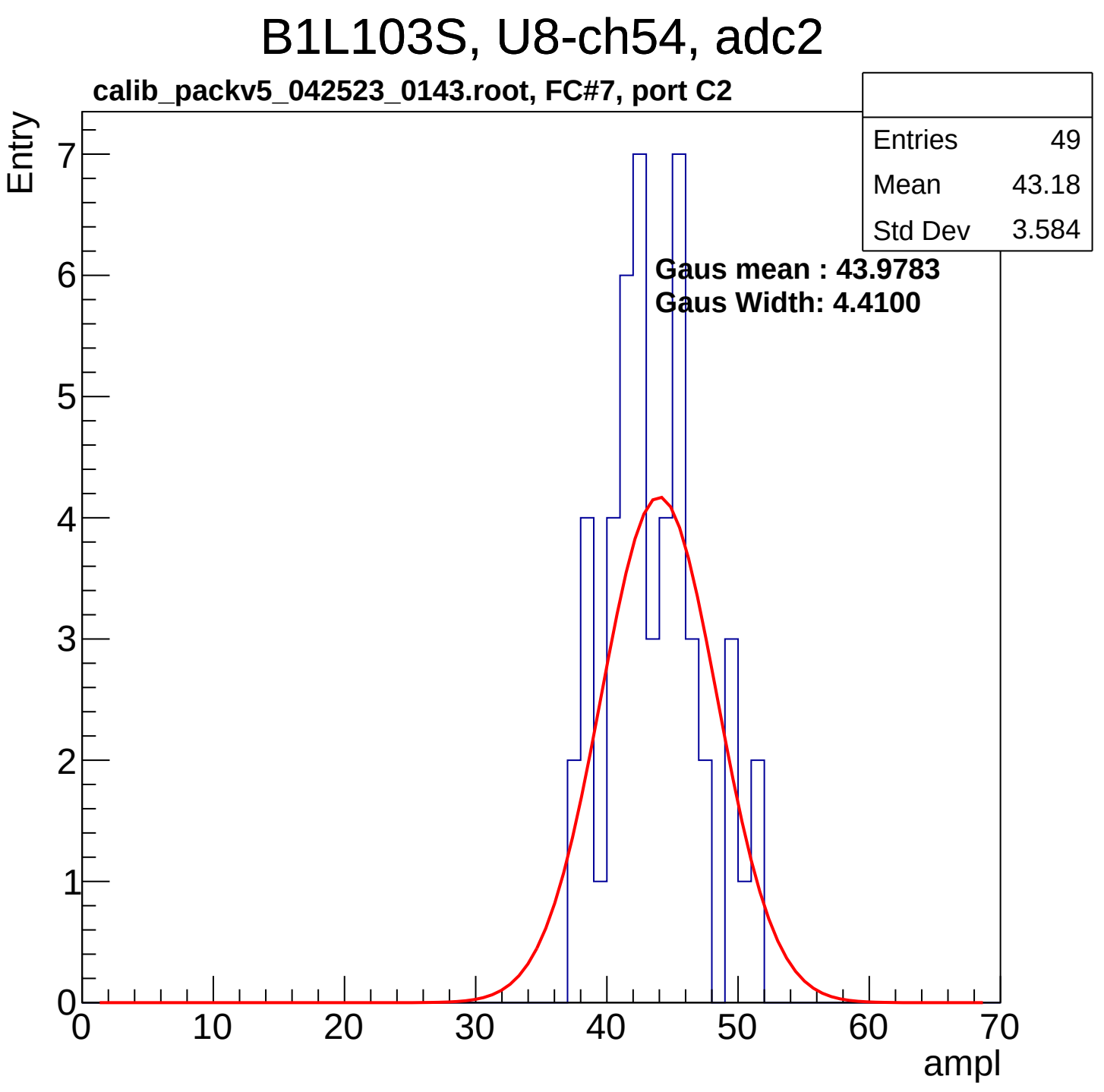

B1L103S, U8-ch53, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 44
Mean 58.8
Std Dev 9.238
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

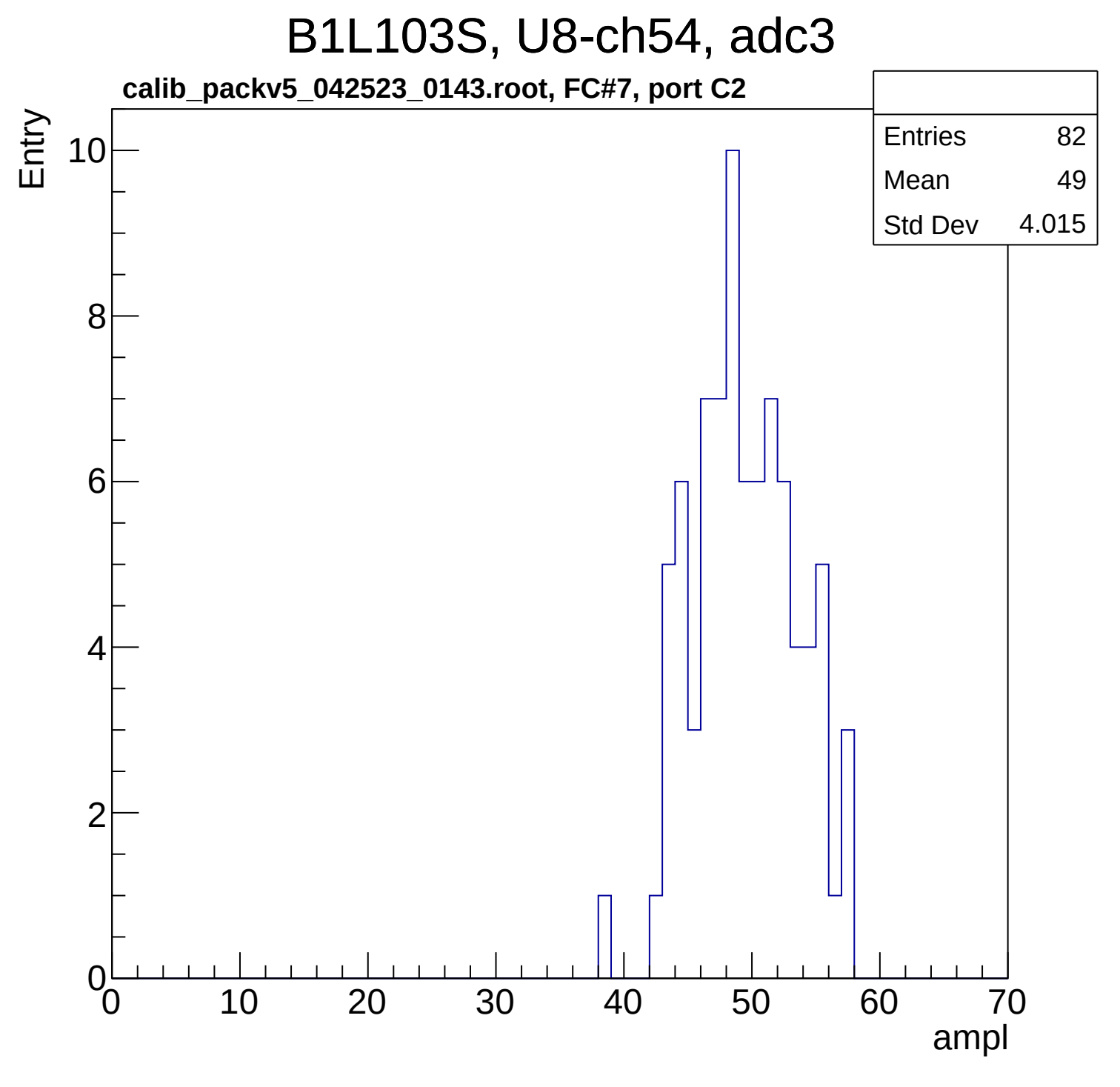

B1L103S, U8-ch53, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 62
Std Dev 1.265
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

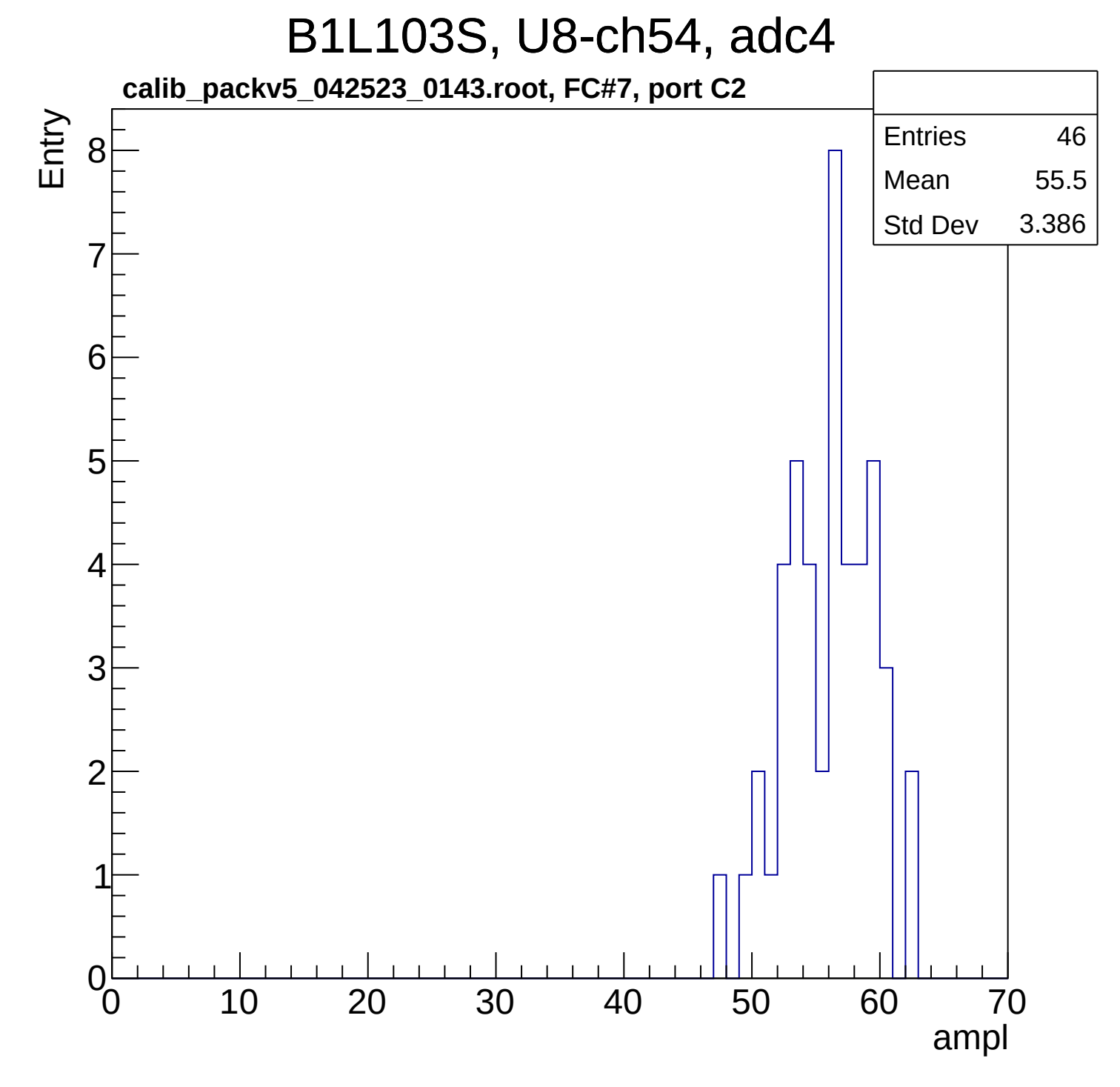

B1L103S, U8-ch53, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 24
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

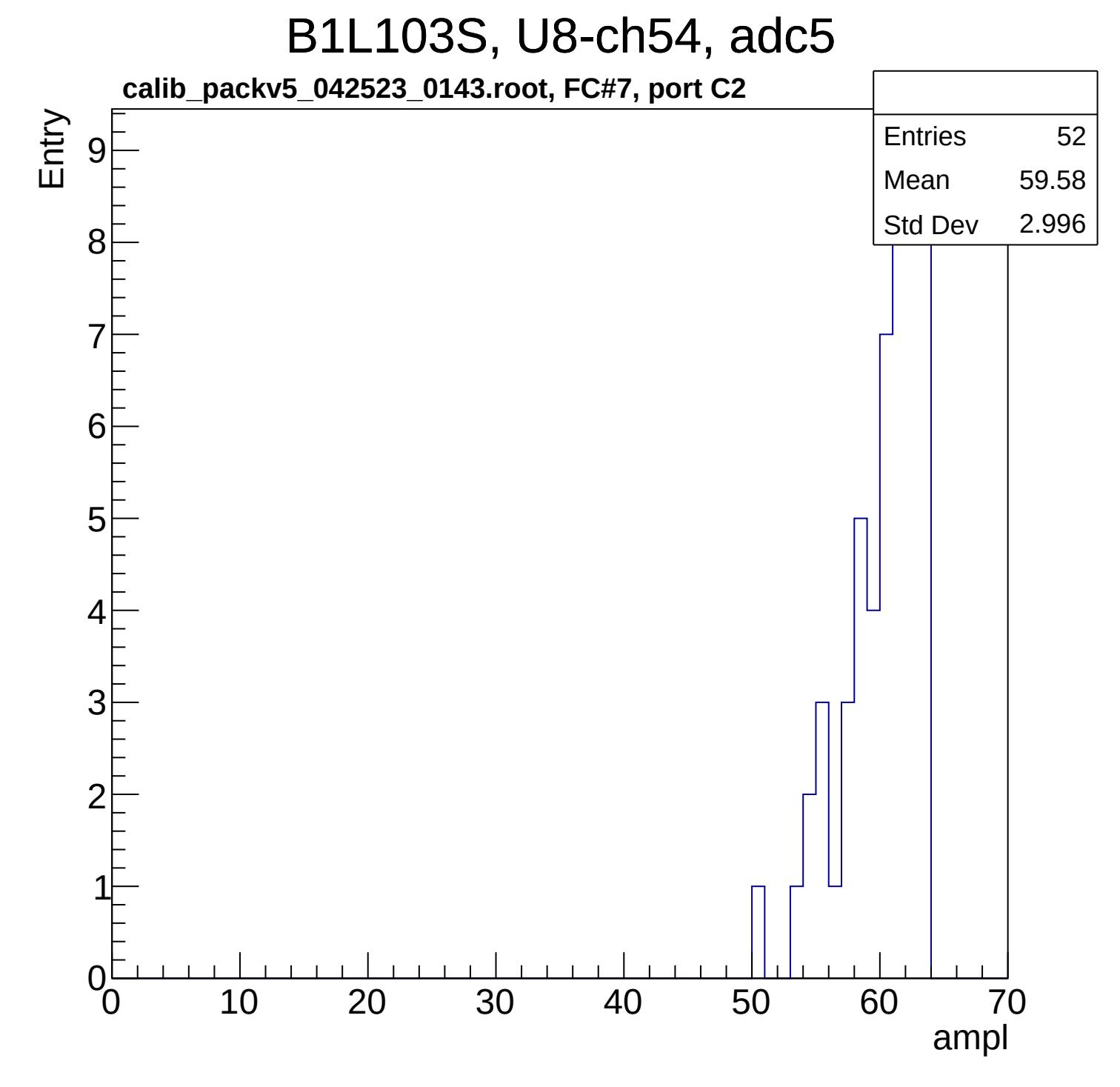

B1L103S, U8-ch54, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 76
Mean 29.89
Std Dev 3.527
Gaus mean : 30.4985
Gaus Width: 3.5589
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

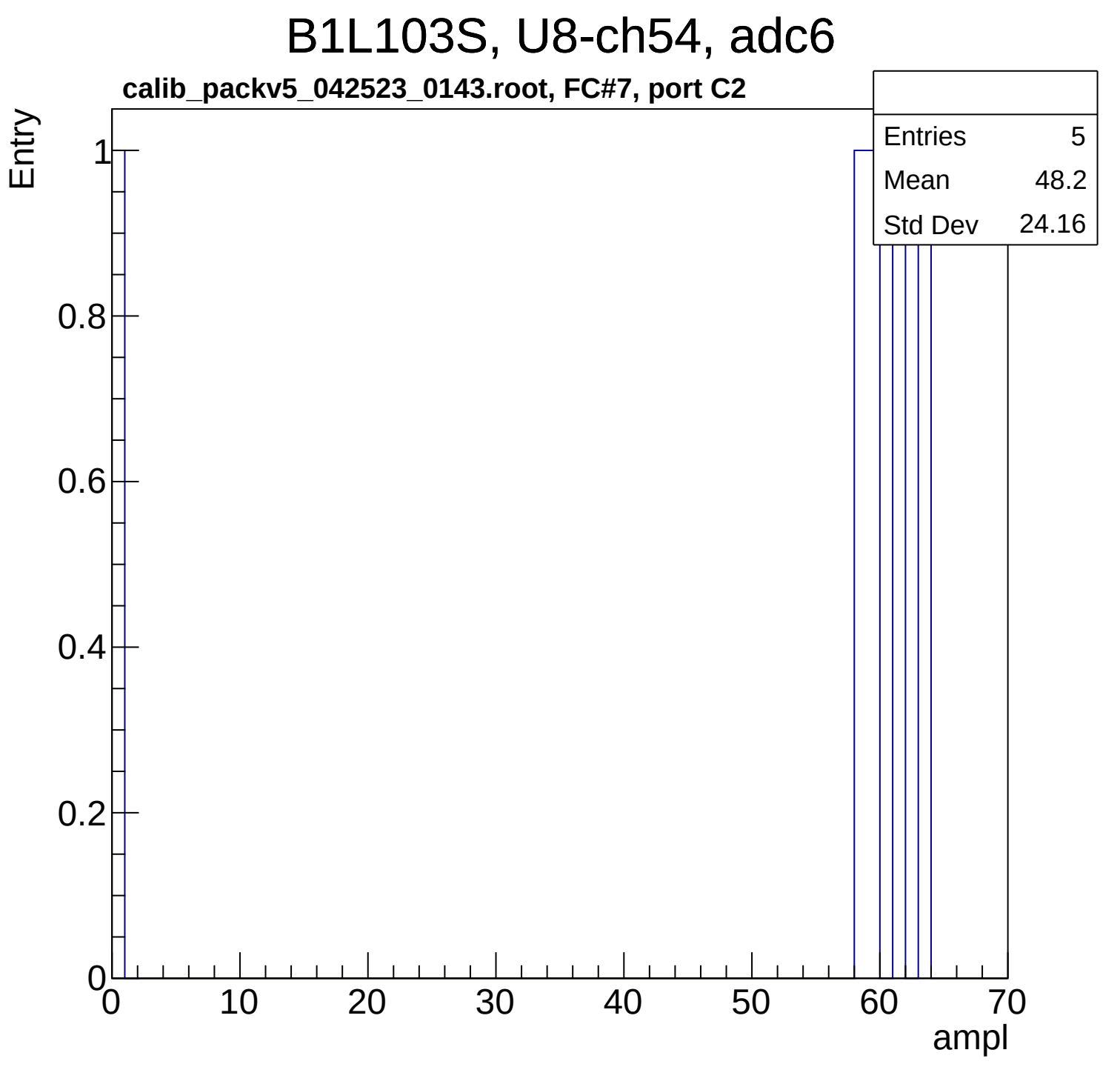

B1L103S, U8-ch54, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 36.53
Std Dev 3.665
Gaus mean : 37.7547
Gaus Width: 3.3710
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

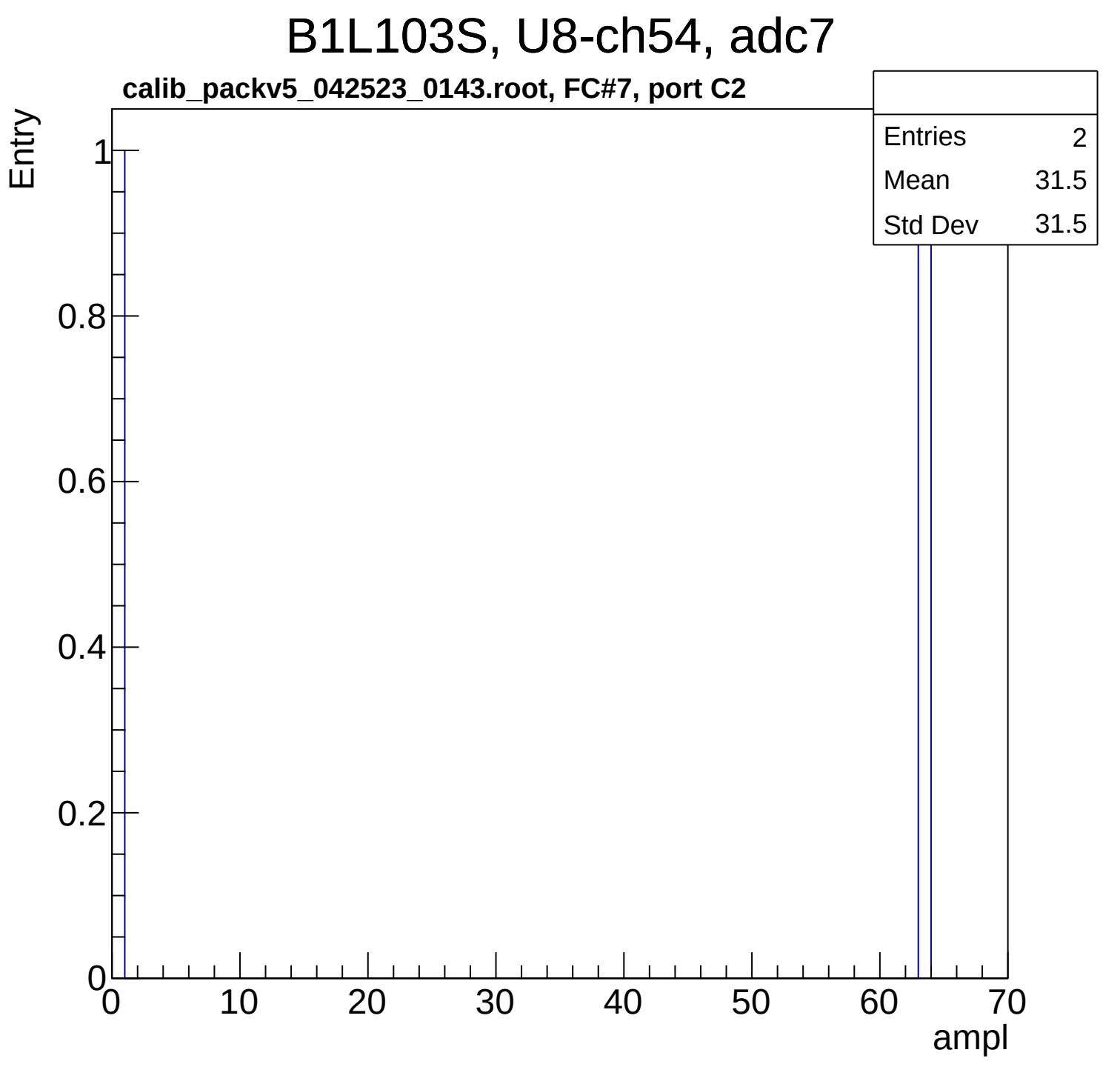

B1L103S, U8-ch54, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 43.18
Std Dev 3.584
Gaus mean : 43.9783
Gaus Width: 4.4100
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

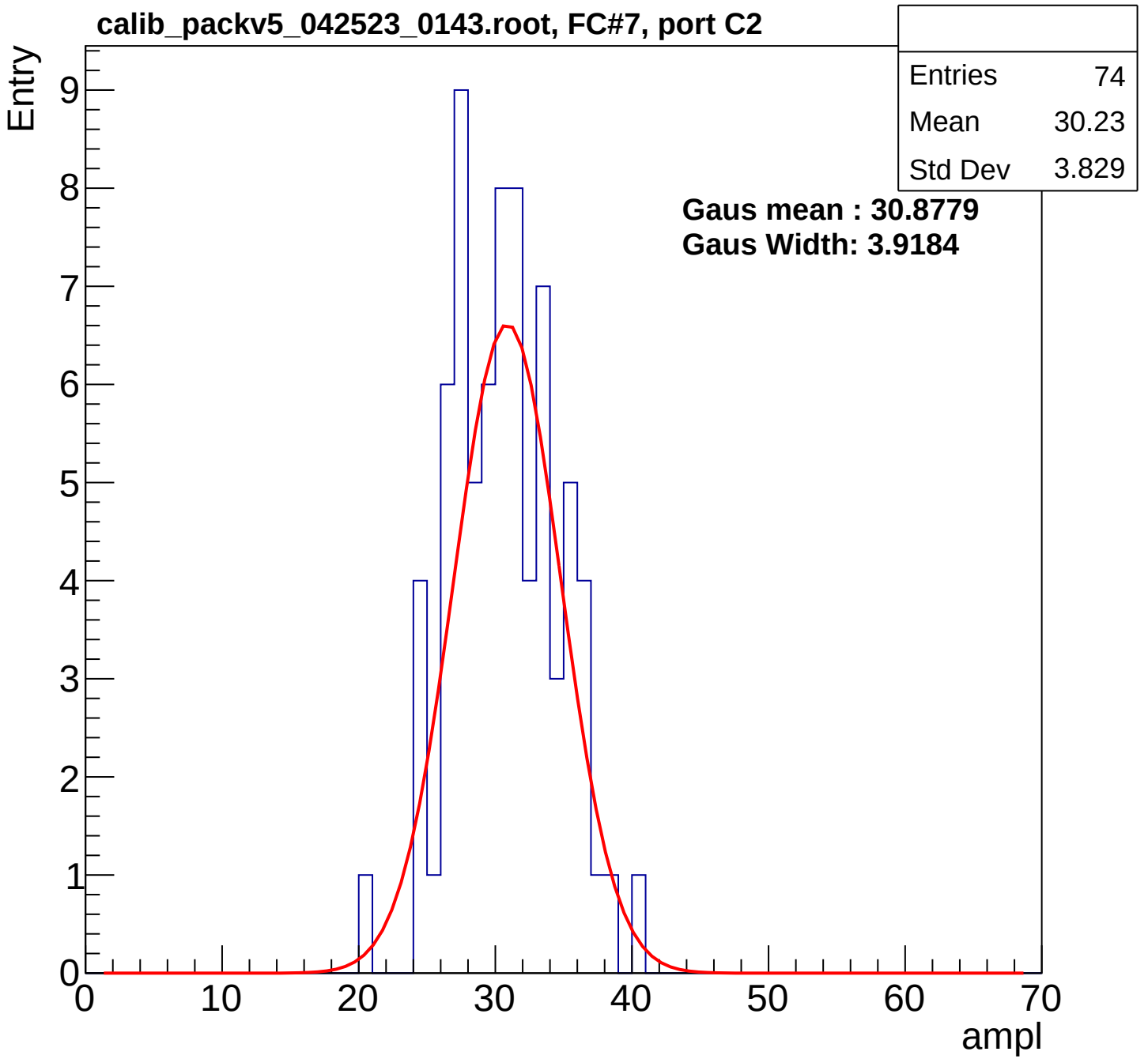

B1L103S, U8-ch54, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 82
Mean 49
Std Dev 4.015
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

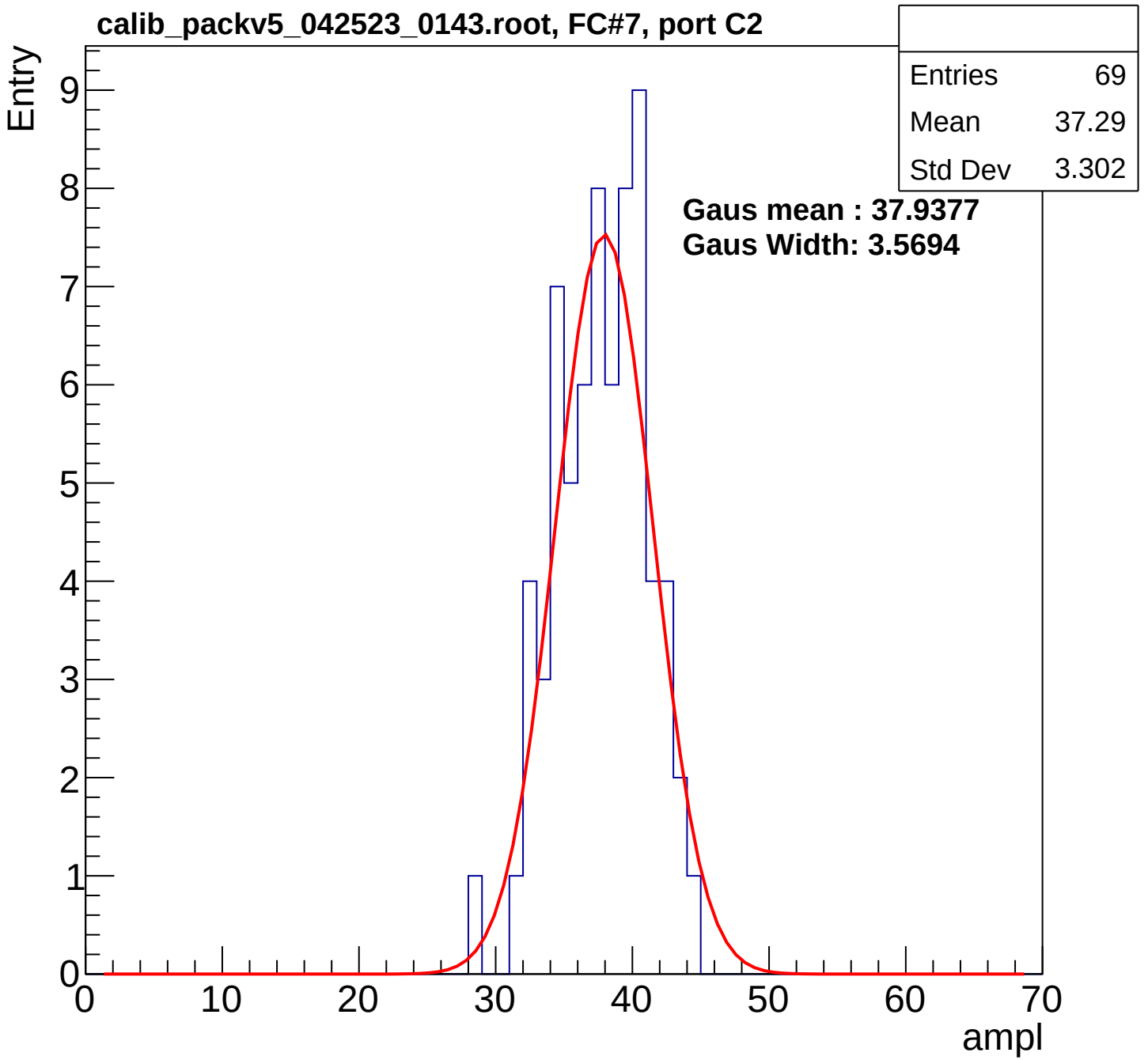

B1L103S, U8-ch54, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 46
Mean 55.5
Std Dev 3.386
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

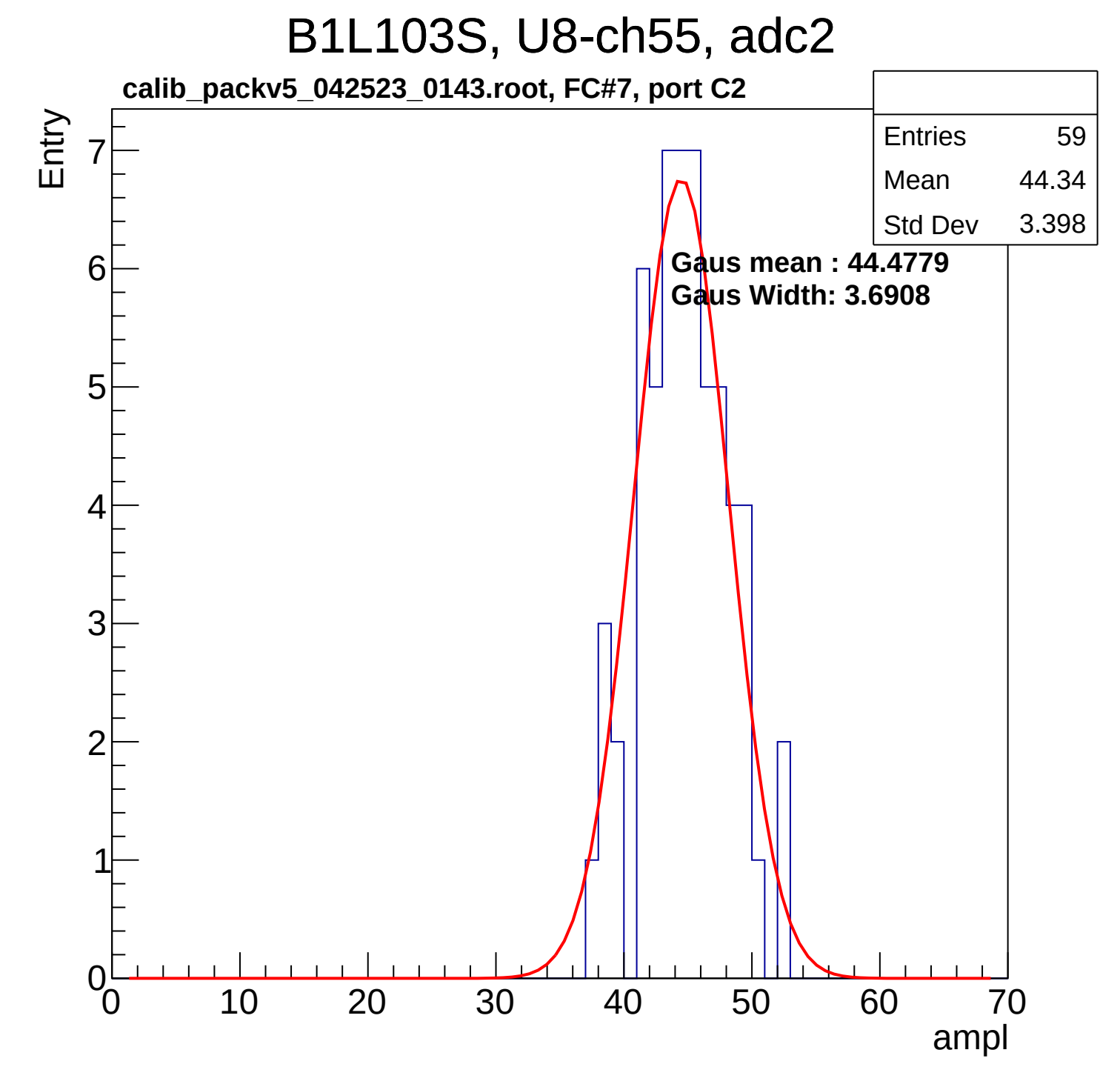

B1L103S, U8-ch54, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 59.58
Std Dev 2.996
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

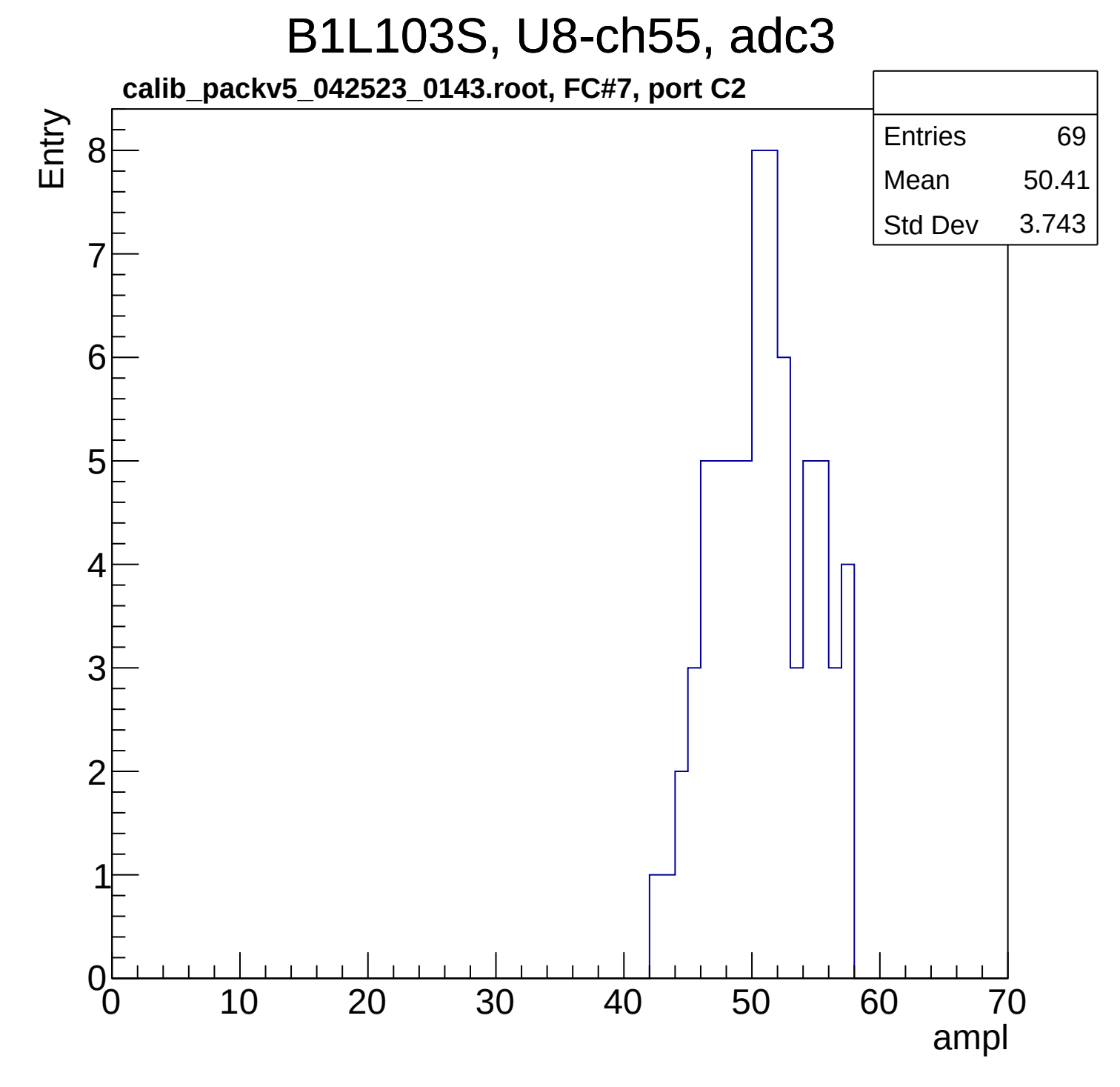

B1L103S, U8-ch54, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 48.2
Std Dev 24.16
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

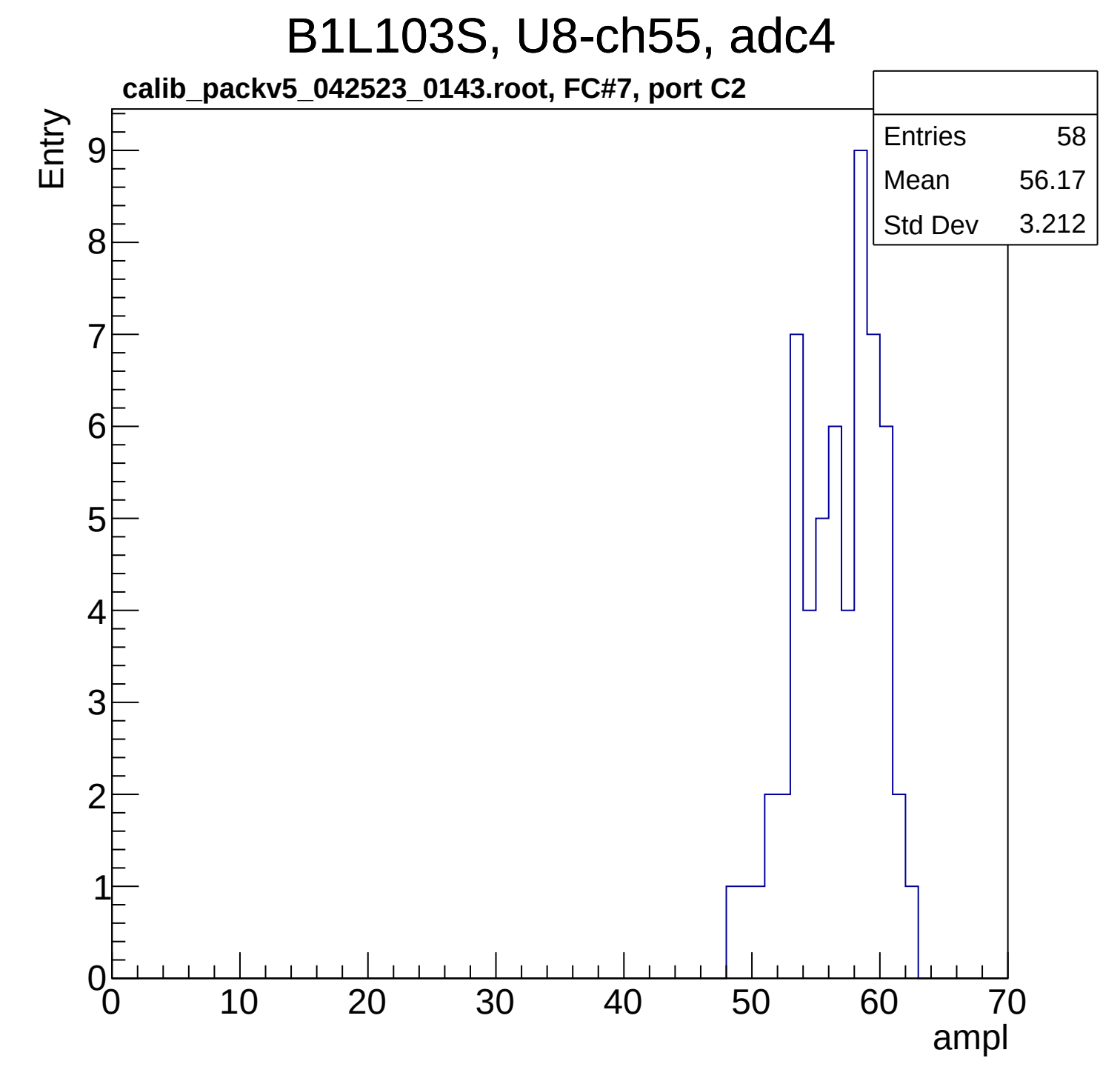

B1L103S, U8-ch54, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

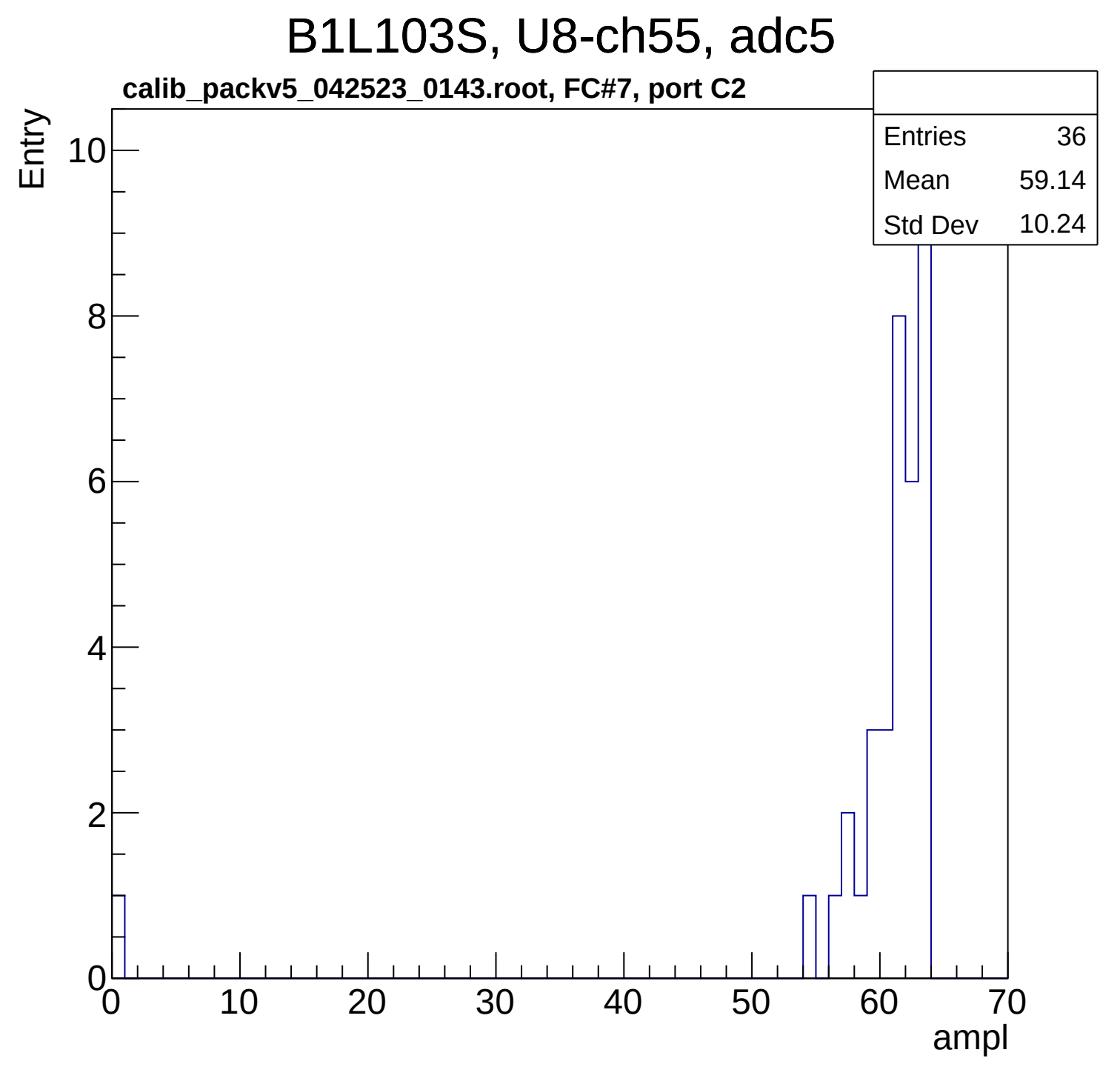

B1L103S, U8-ch55, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 30.23
Std Dev 3.829
Gaus mean : 30.8779
Gaus Width: 3.9184
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

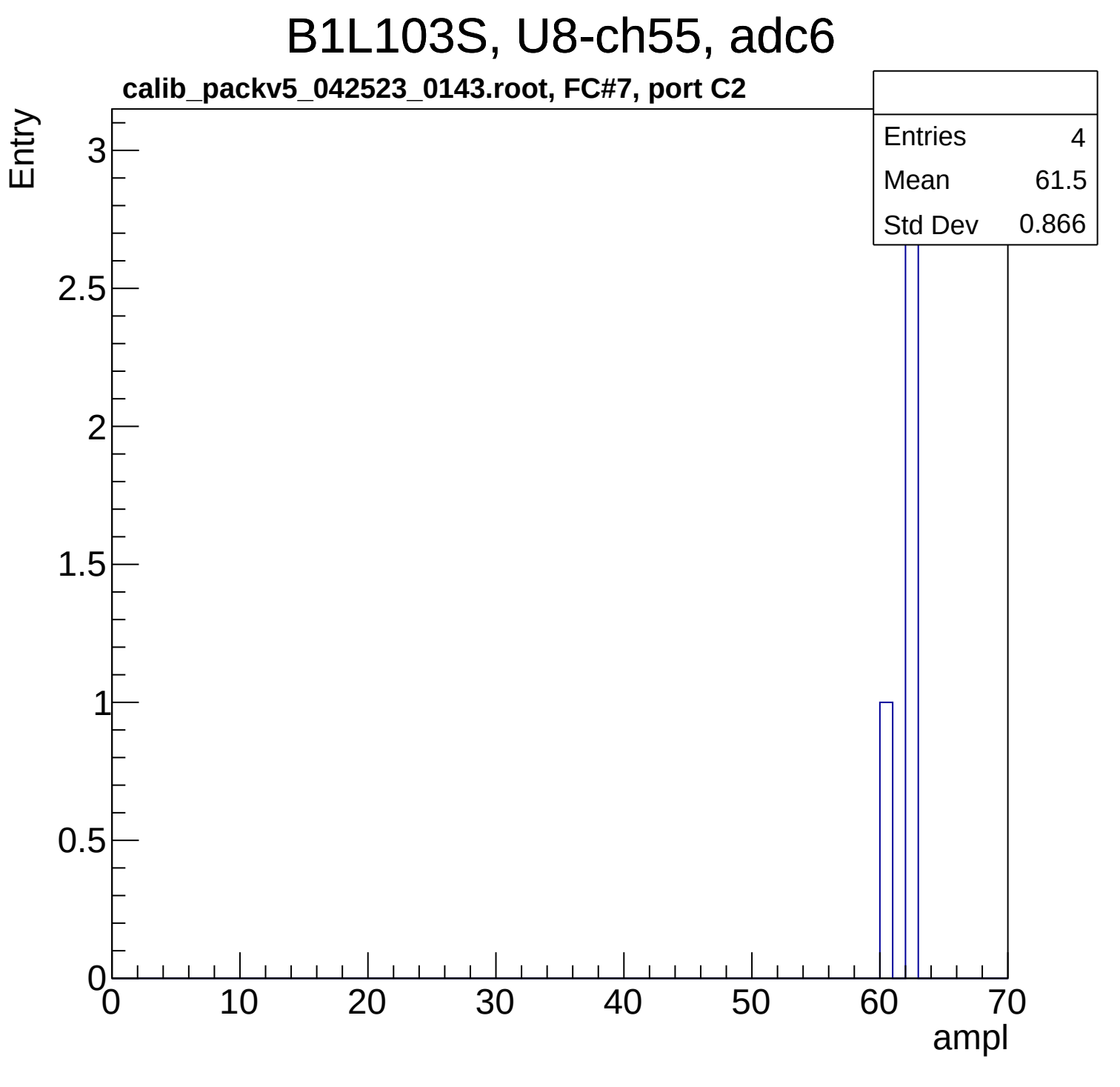

B1L103S, U8-ch55, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 37.29
Std Dev 3.302
Gaus mean : 37.9377
Gaus Width: 3.5694
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

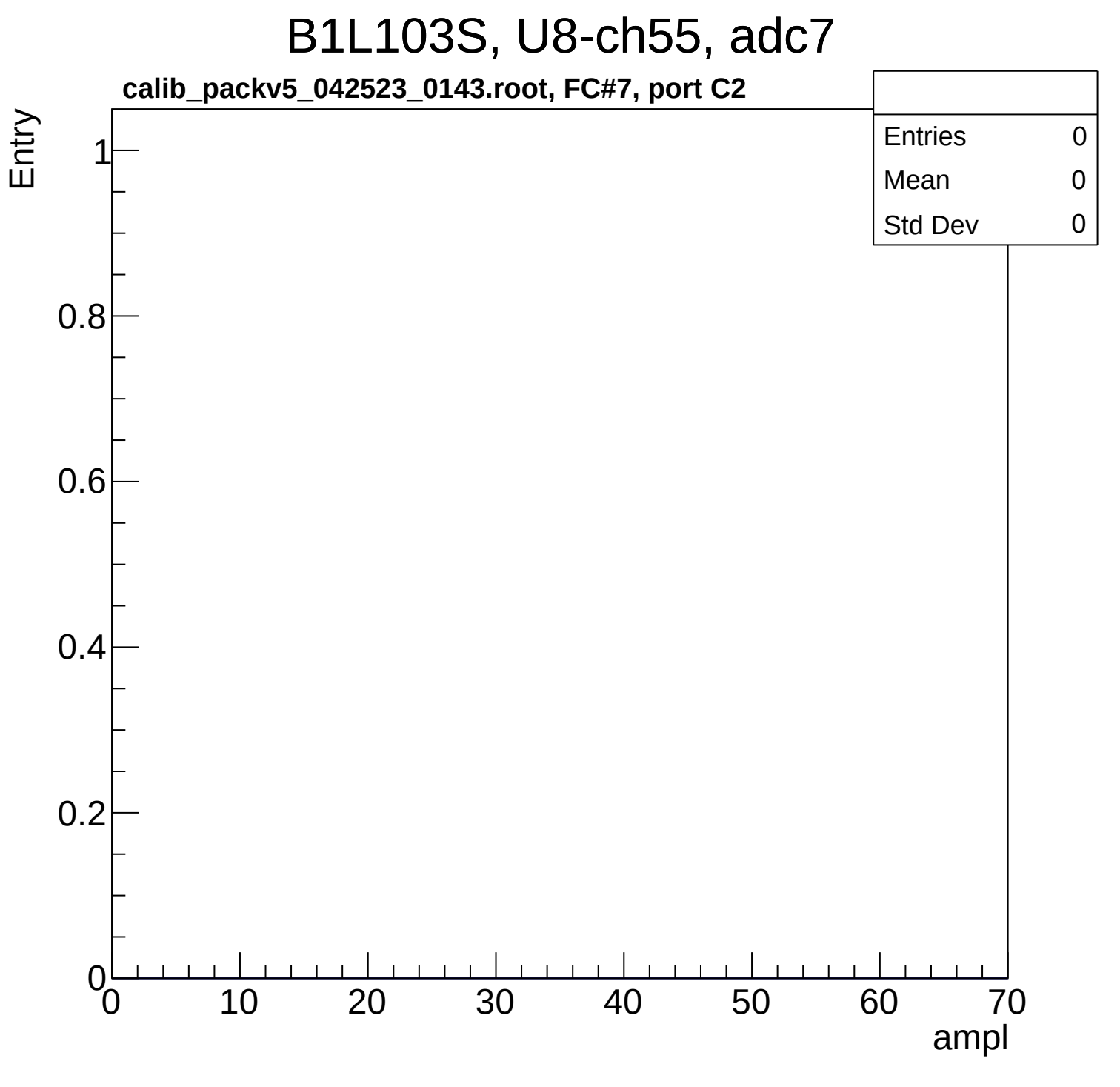

B1L103S, U8-ch55, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 44.34
Std Dev 3.398
Gaus mean : 44.4779
Gaus Width: 3.6908
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

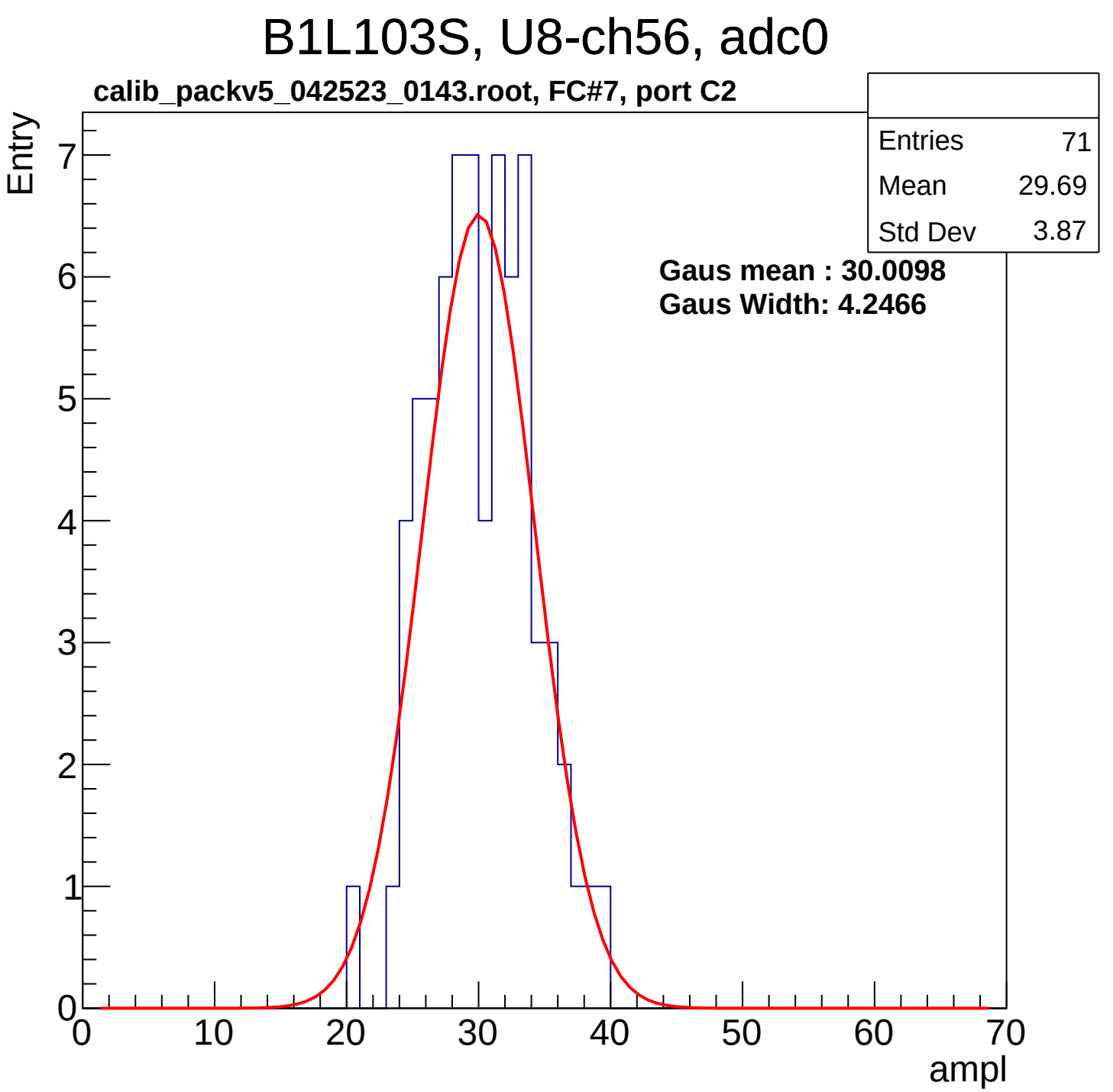

B1L103S, U8-ch55, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 50.41
Std Dev 3.743
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

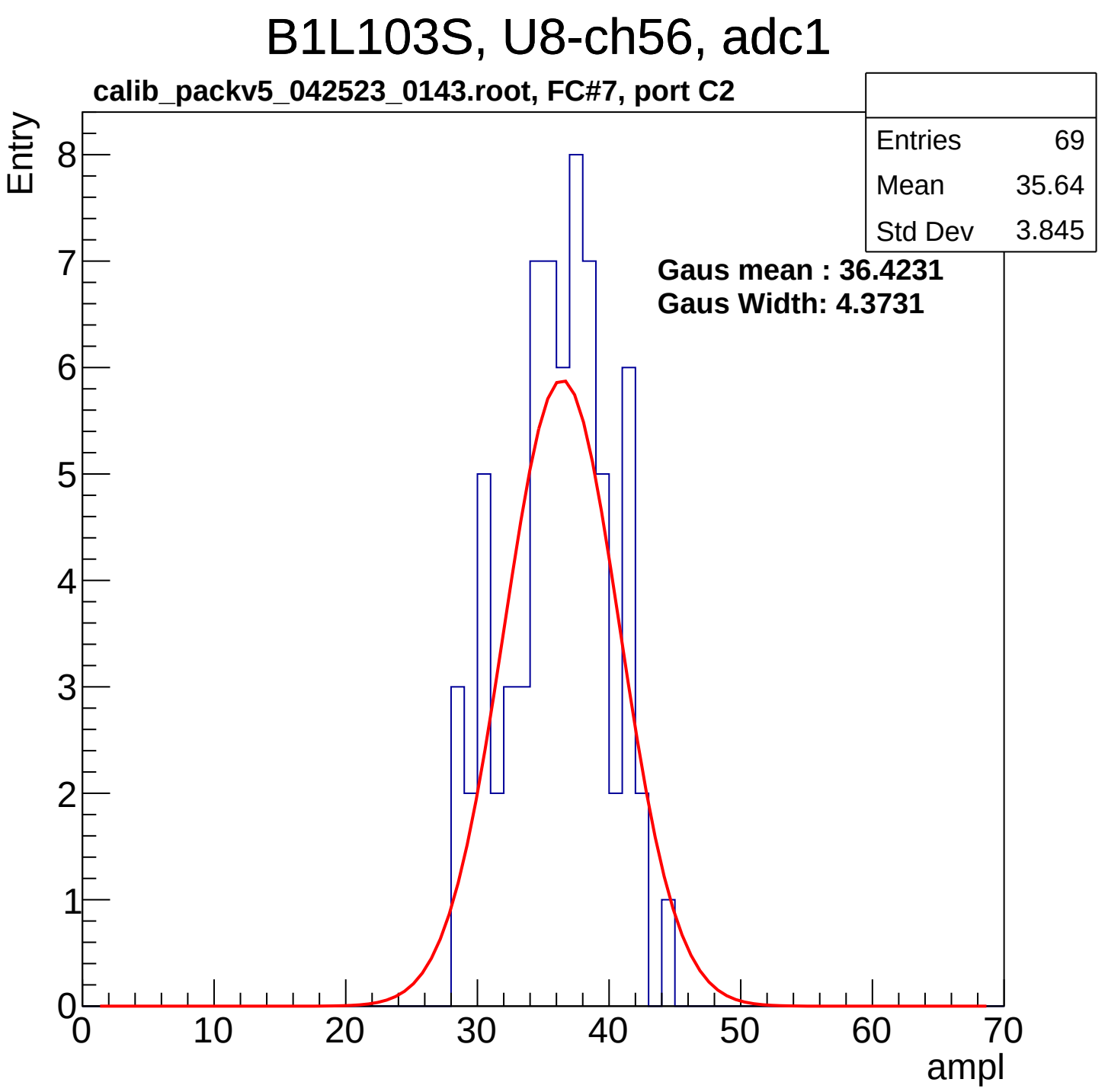

B1L103S, U8-ch55, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 56.17
Std Dev 3.212
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

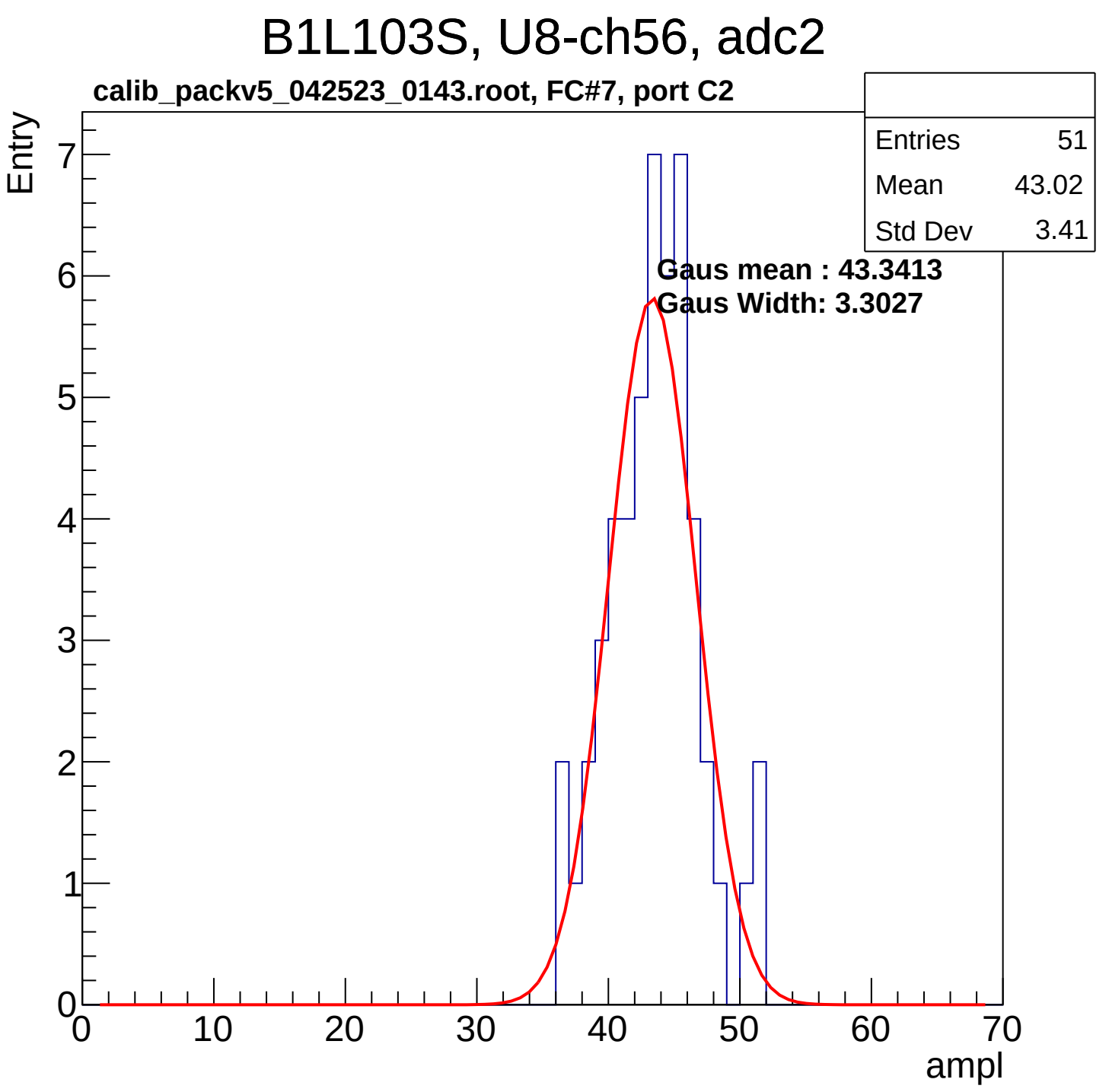

B1L103S, U8-ch55, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 36
Mean 59.14
Std Dev 10.24
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

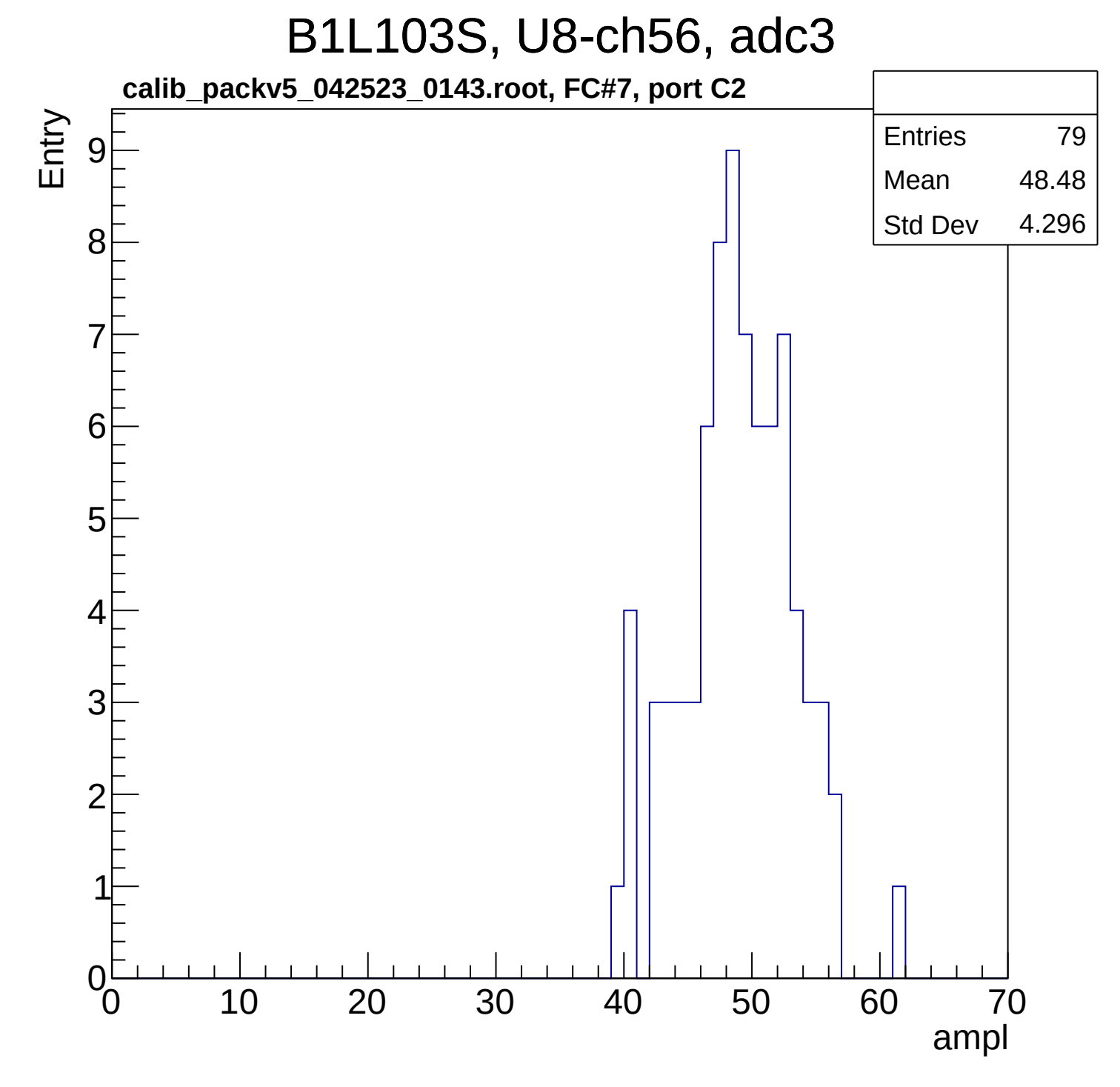

B1L103S, U8-ch55, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 61.5
Std Dev 0.866
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

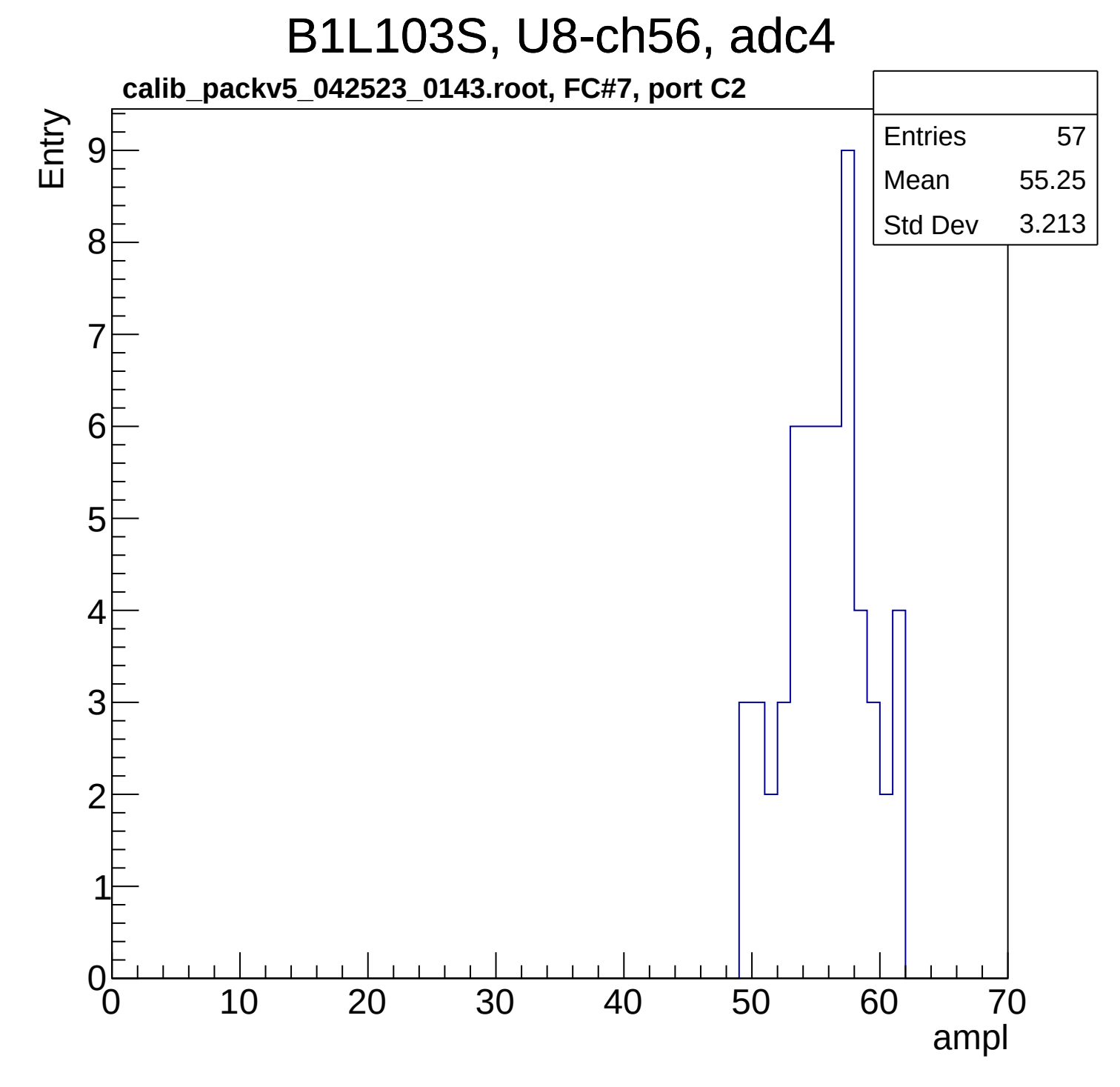

B1L103S, U8-ch55, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

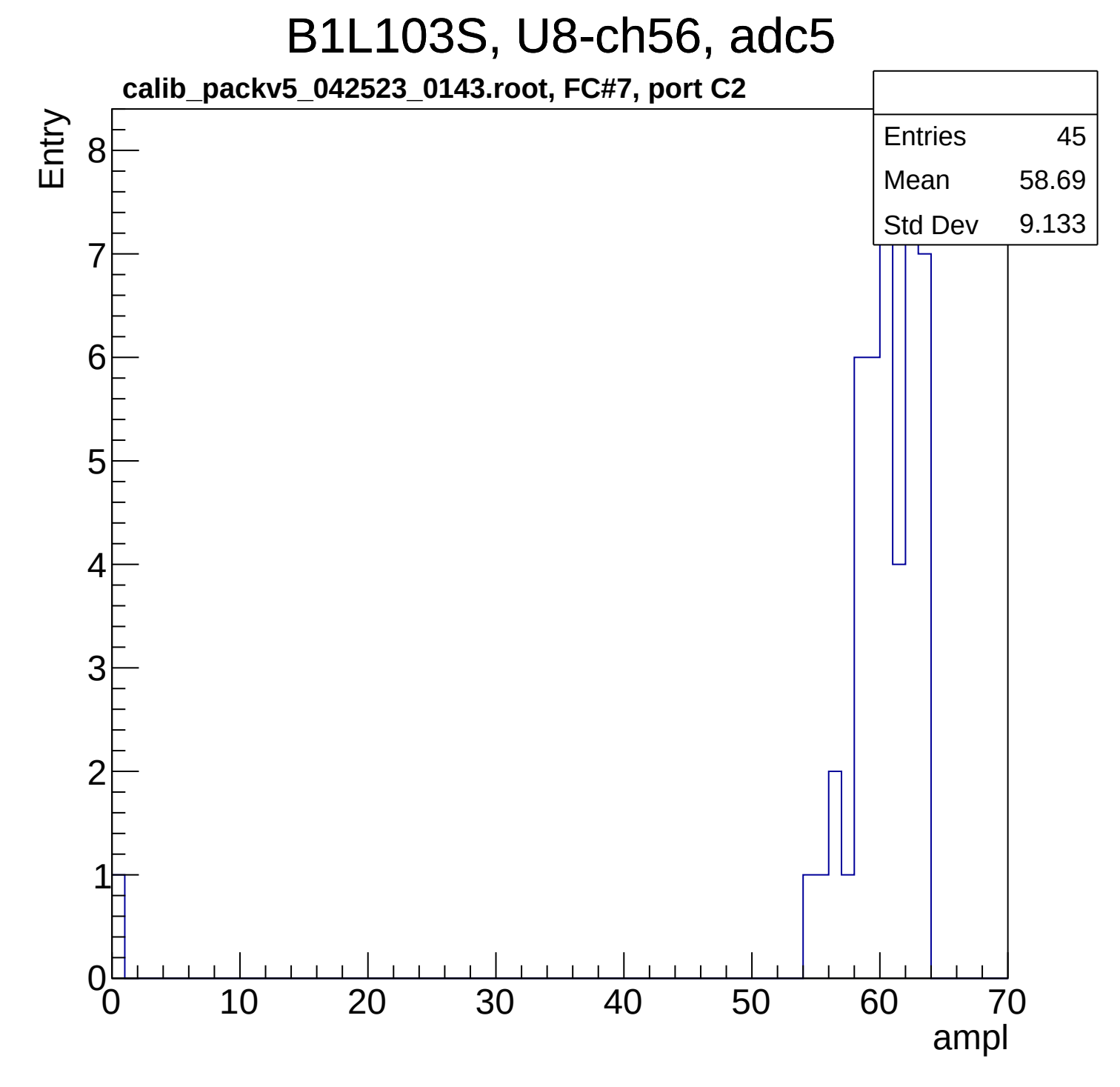

B1L103S, U8-ch56, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 29.69
Std Dev 3.87
Gaus mean : 30.0098
Gaus Width: 4.2466
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

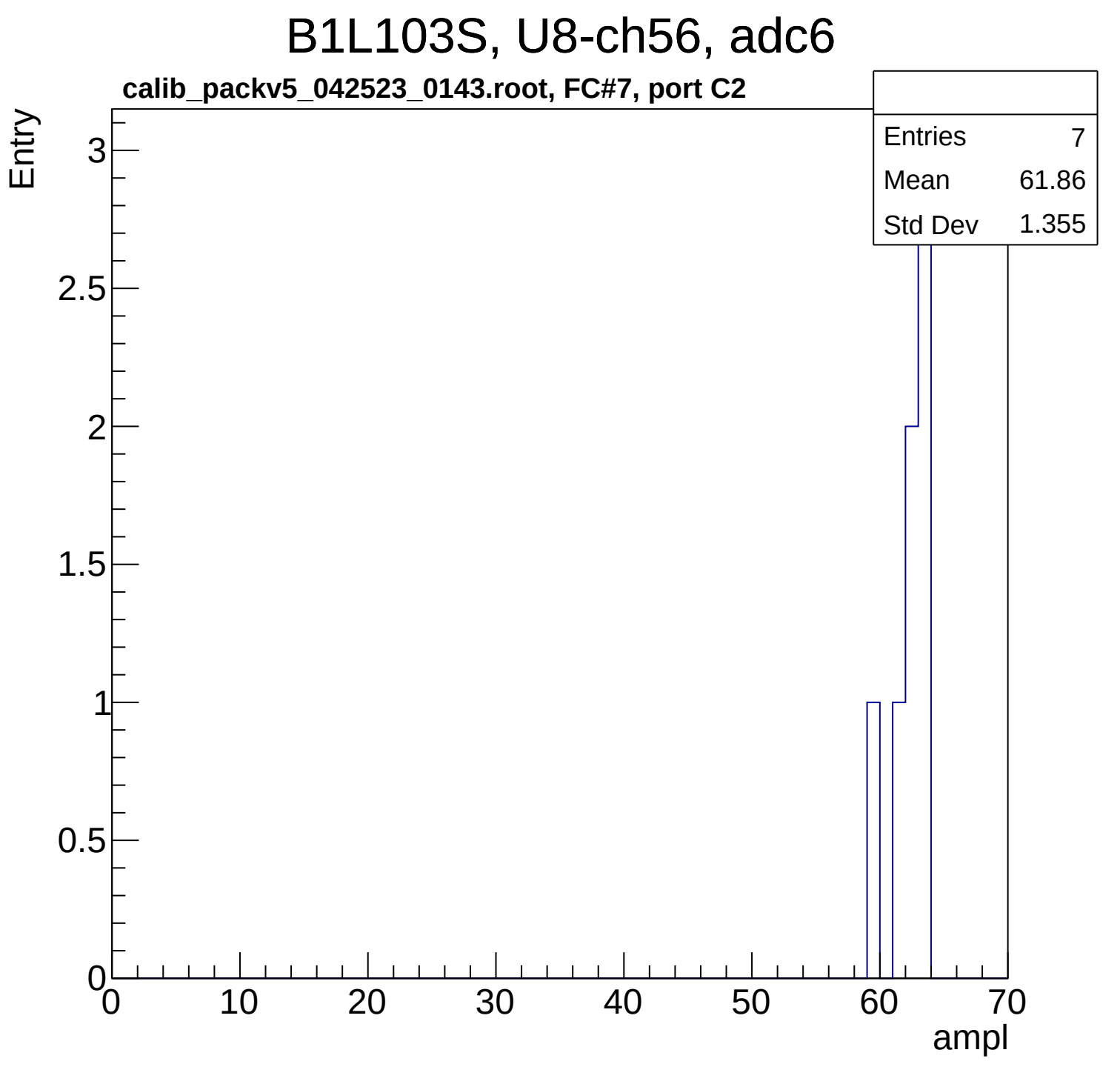

B1L103S, U8-ch56, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 35.64
Std Dev 3.845
Gaus mean : 36.4231
Gaus Width: 4.3731
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

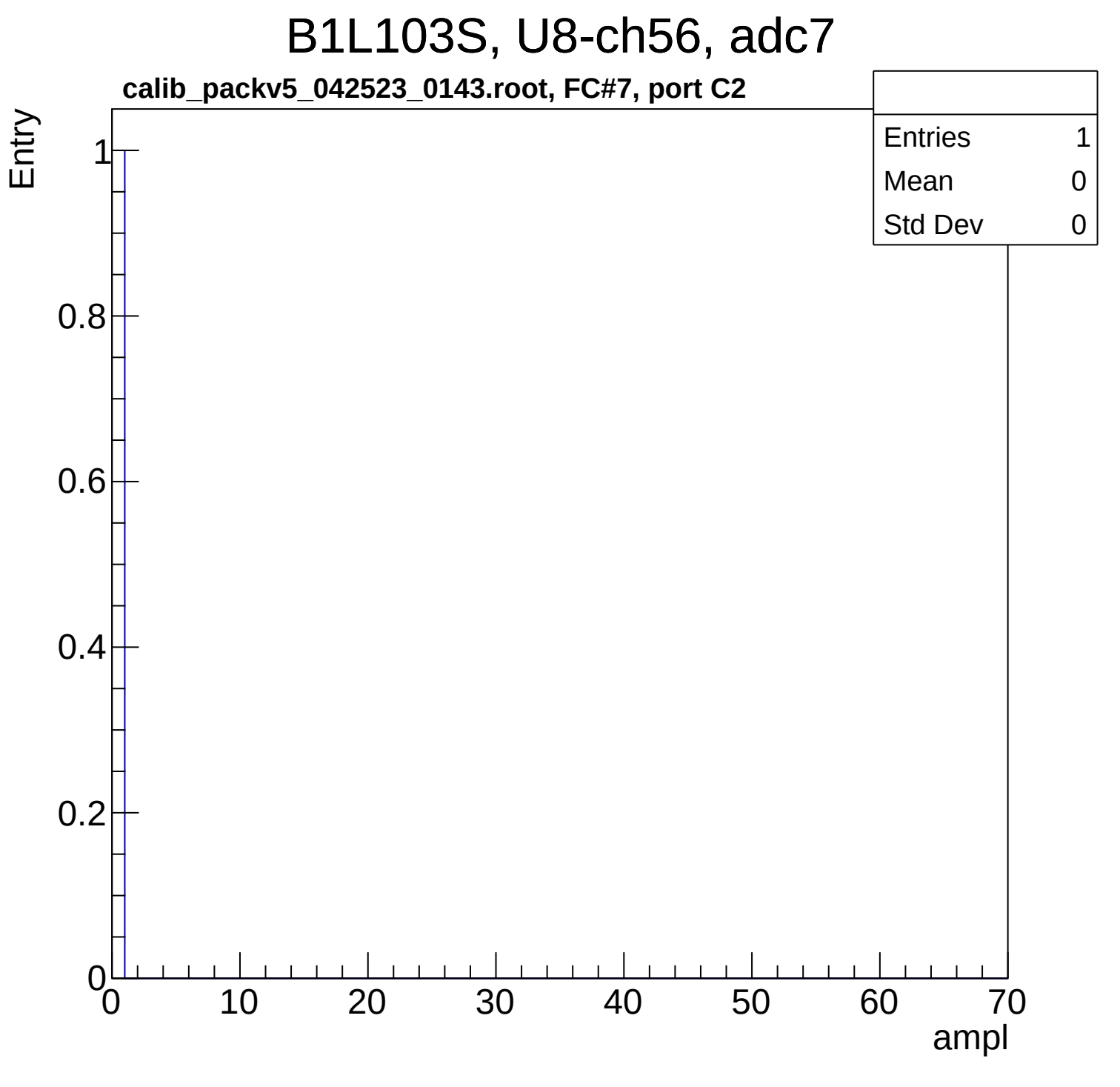

B1L103S, U8-ch56, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 43.02
Std Dev 3.41
Gaus mean : 43.3413
Gaus Width: 3.3027
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

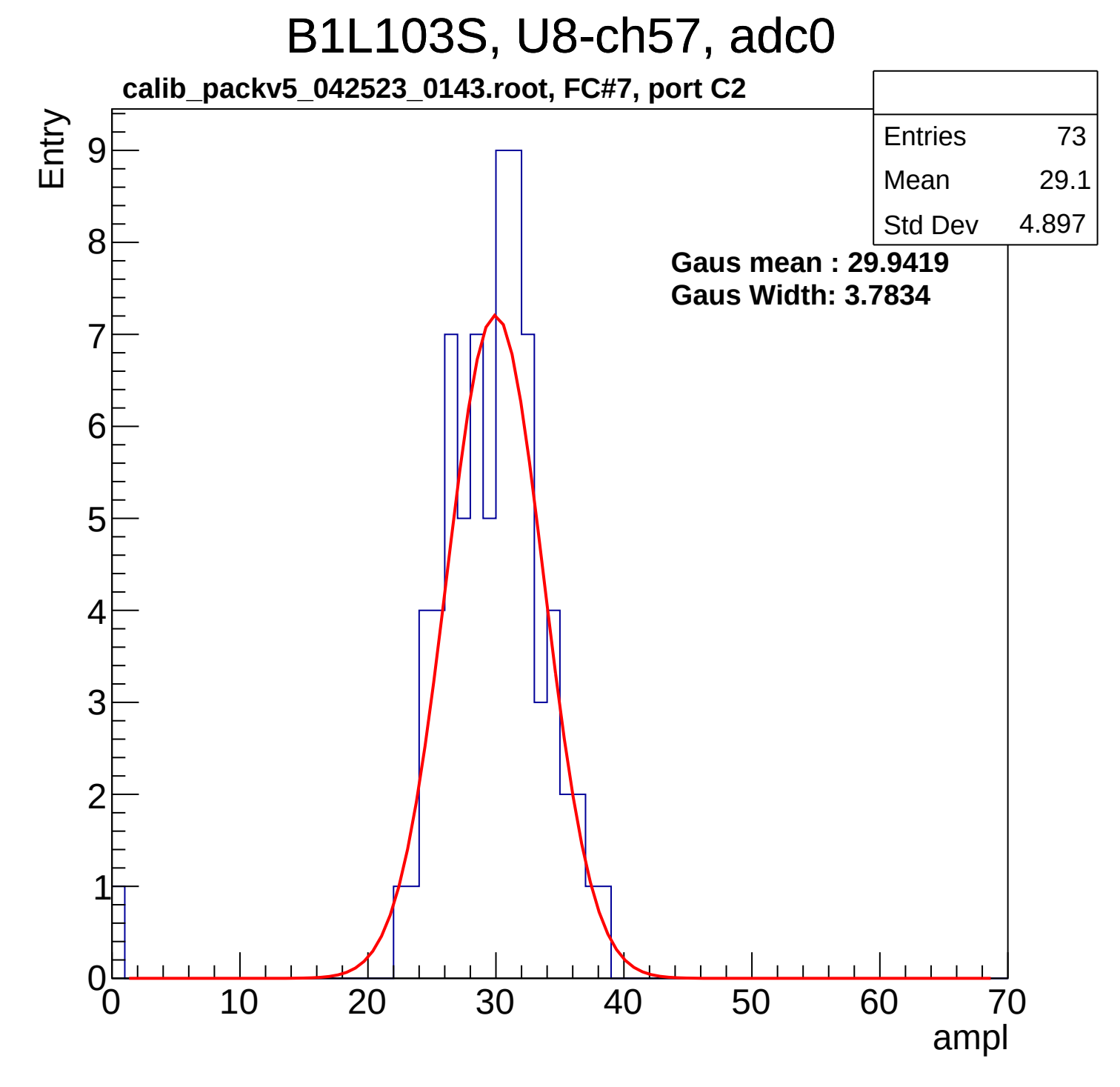

B1L103S, U8-ch56, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 79
Mean 48.48
Std Dev 4.296
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

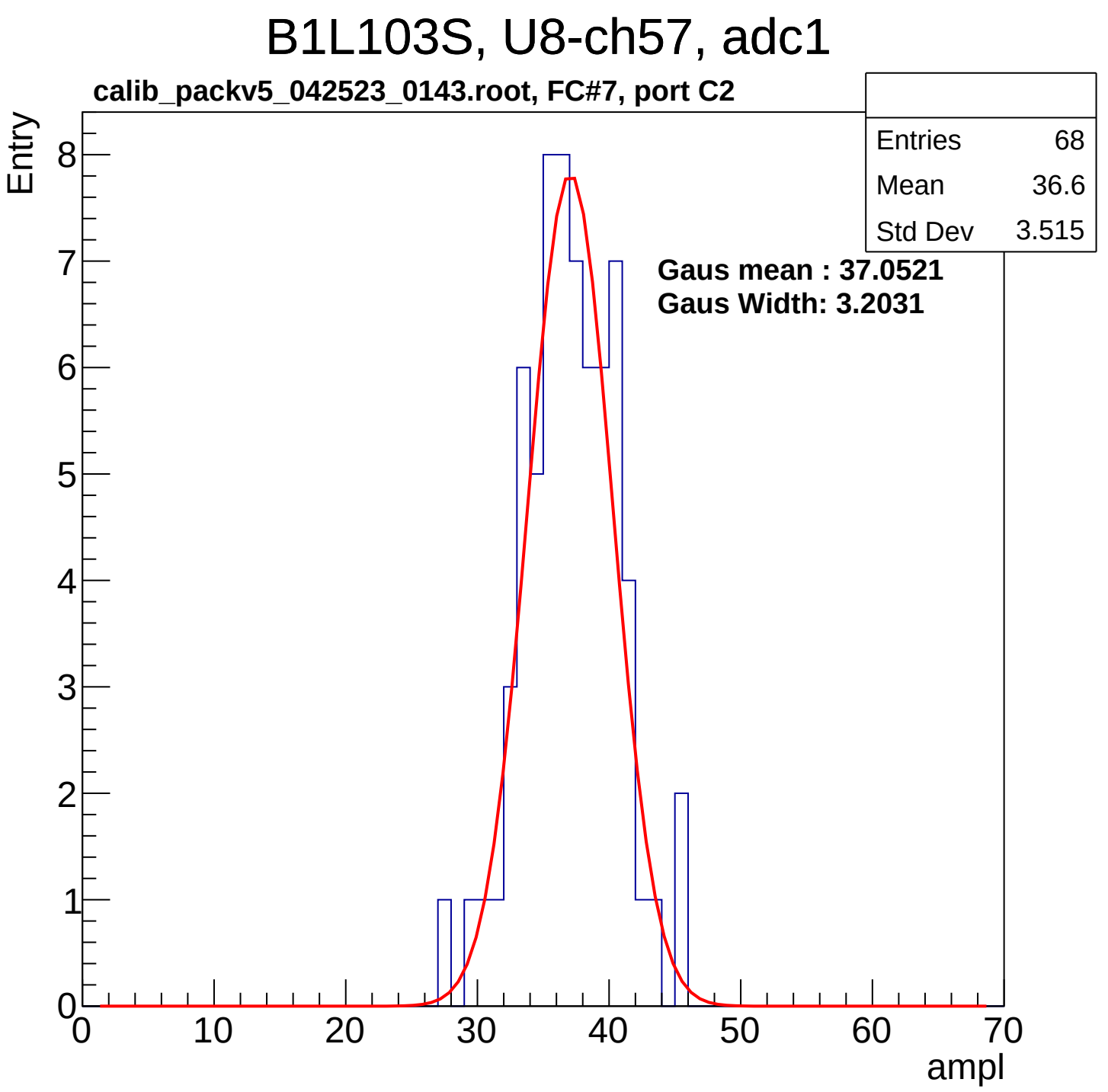

B1L103S, U8-ch56, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 55.25
Std Dev 3.213
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

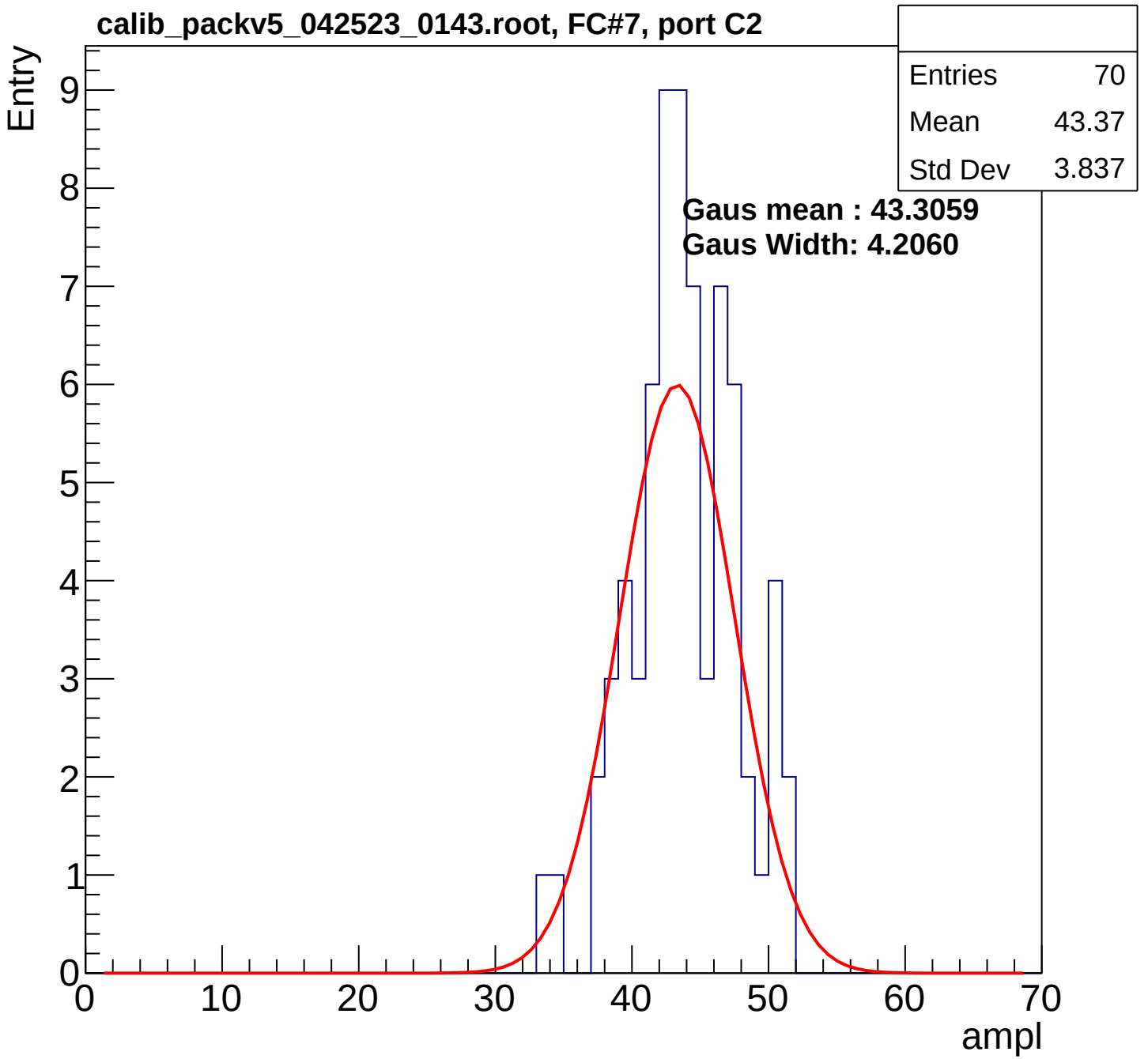

B1L103S, U8-ch56, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 45
Mean 58.69
Std Dev 9.133
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

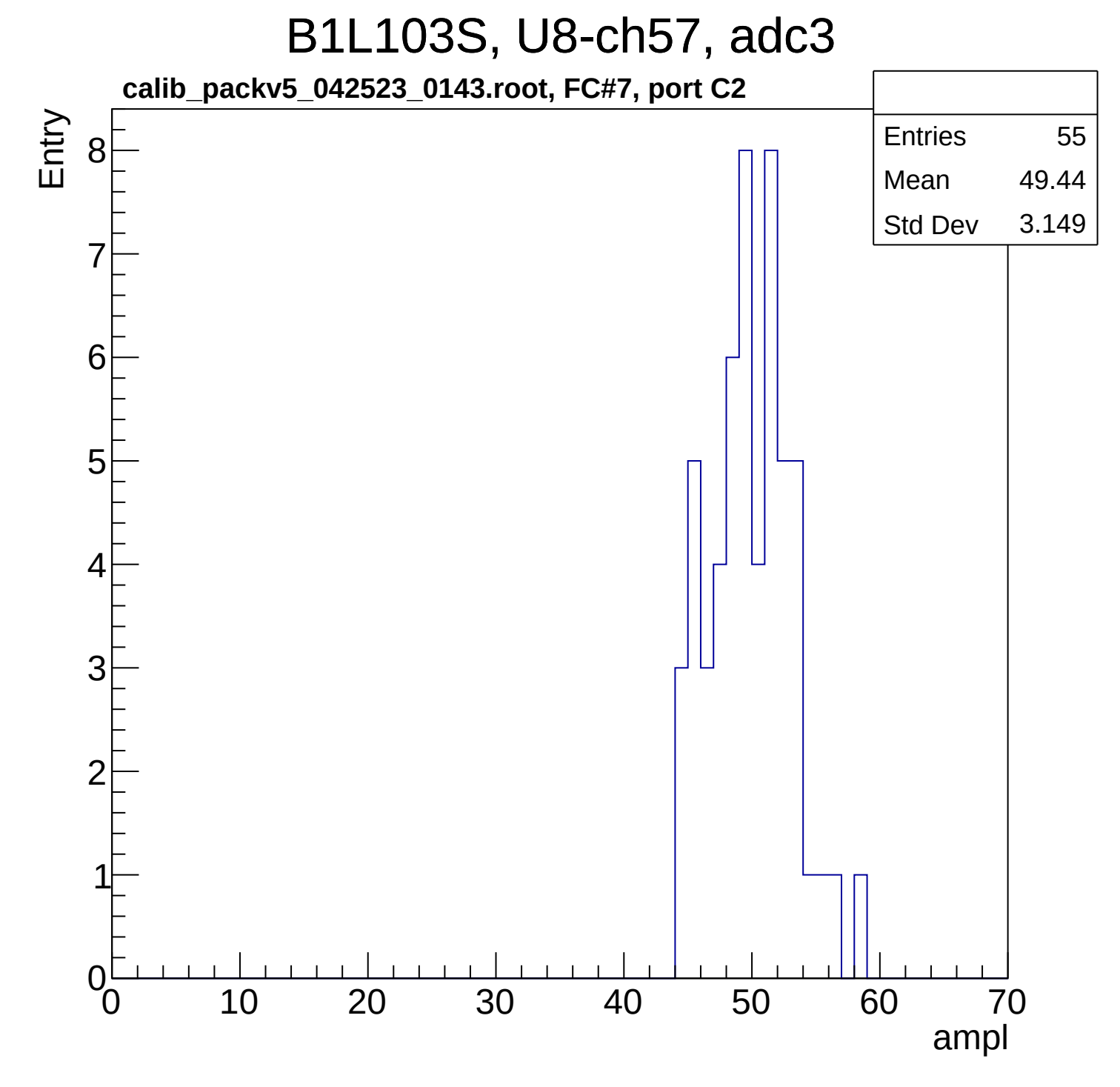

B1L103S, U8-ch56, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 7
Mean 61.86
Std Dev 1.355
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

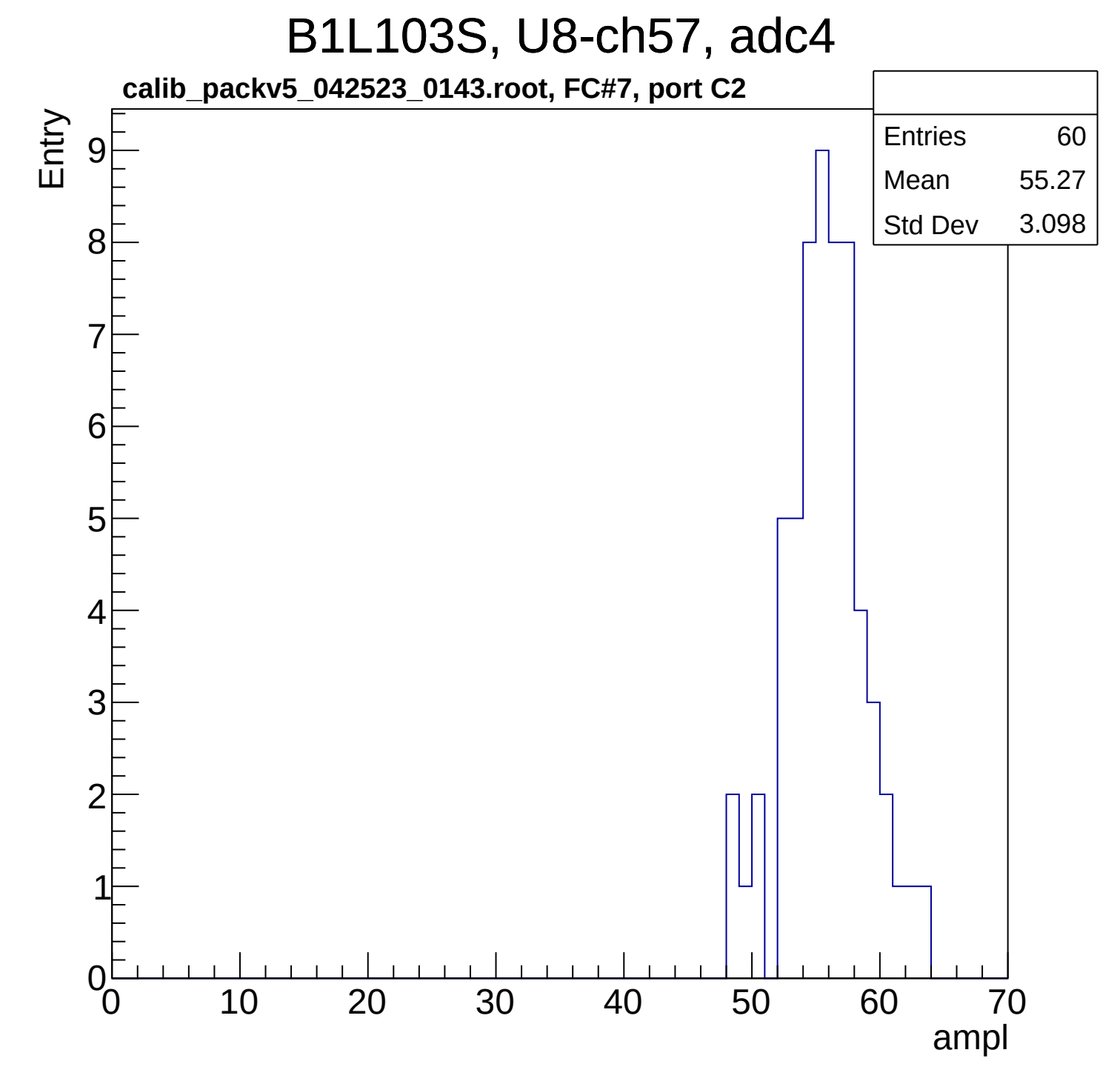

B1L103S, U8-ch56, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

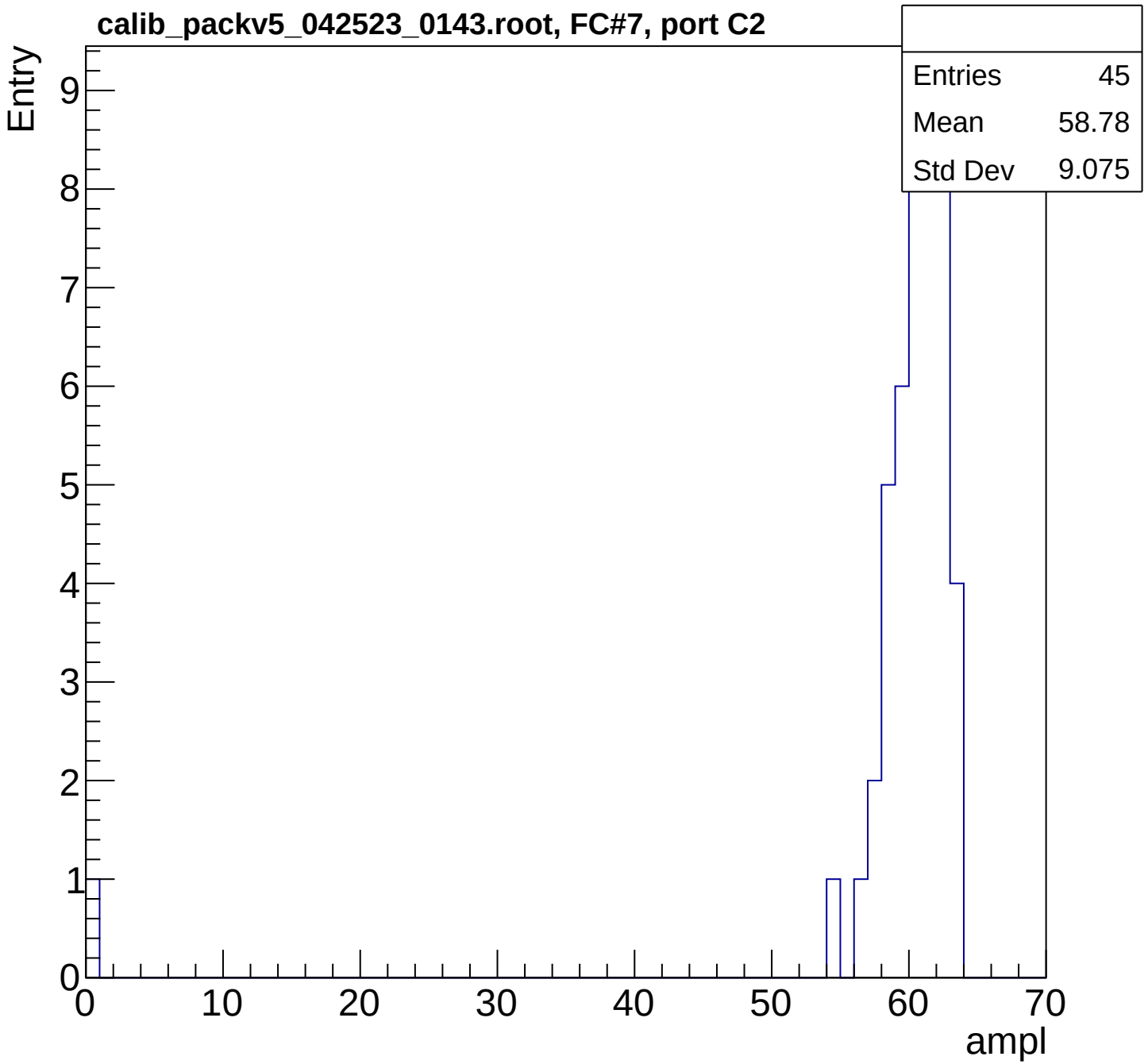

B1L103S, U8-ch57, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 29.1
Std Dev 4.897
Gaus mean : 29.9419
Gaus Width: 3.7834
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

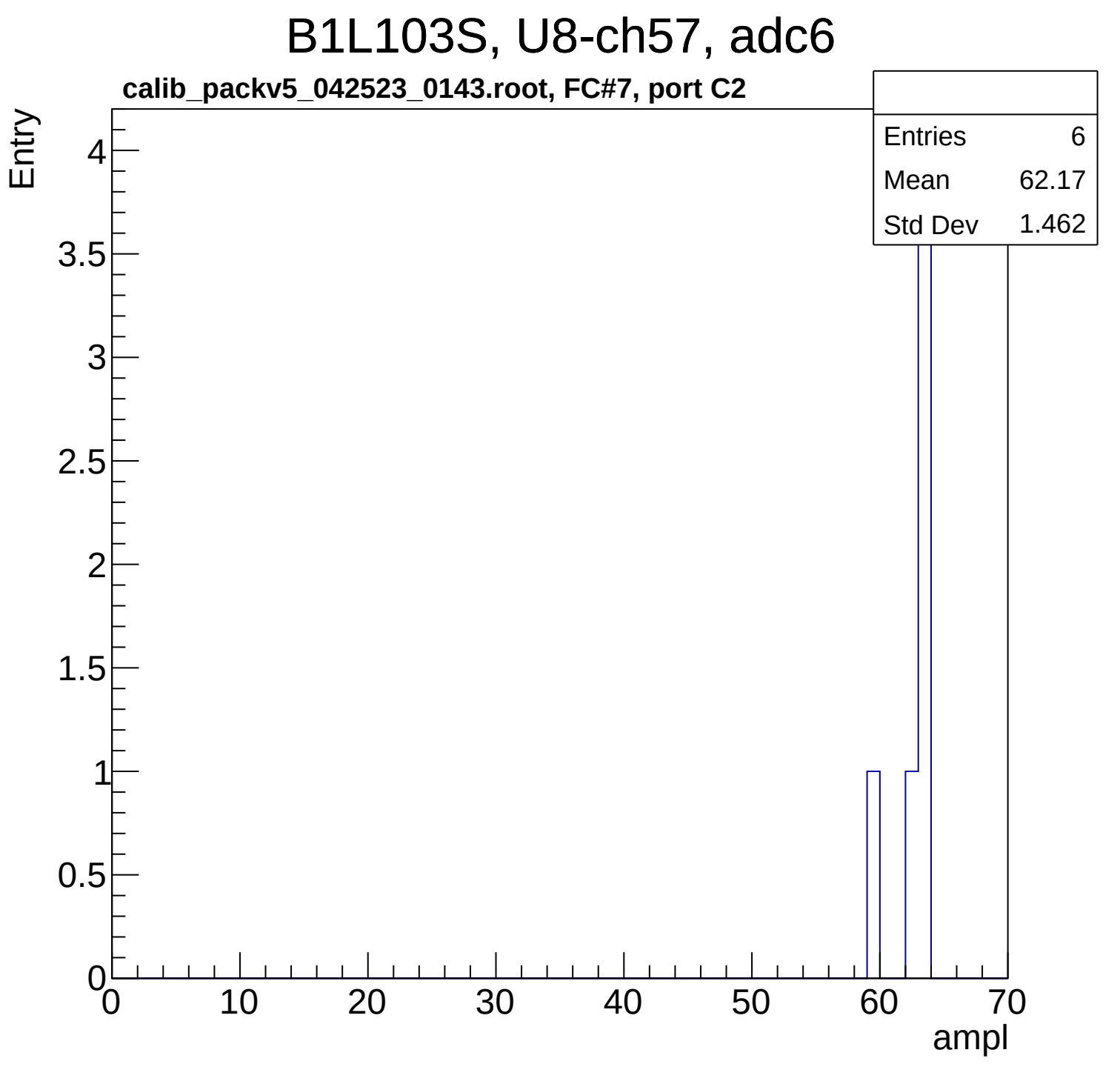

B1L103S, U8-ch57, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 36.6
Std Dev 3.515
Gaus mean : 37.0521
Gaus Width: 3.2031
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

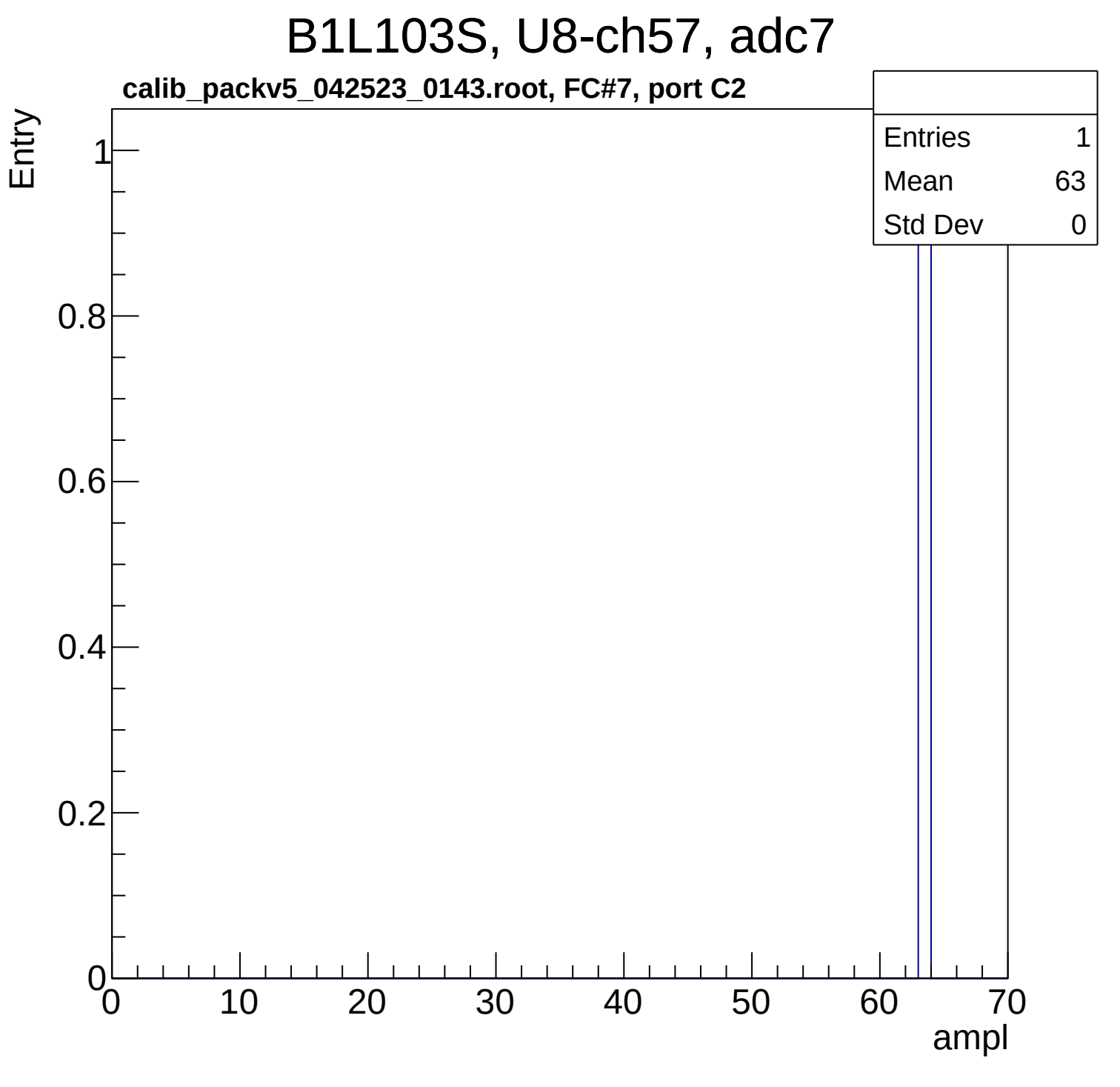

B1L103S, U8-ch57, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 43.37
Std Dev 3.837
Gaus mean : 43.3059
Gaus Width: 4.2060
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

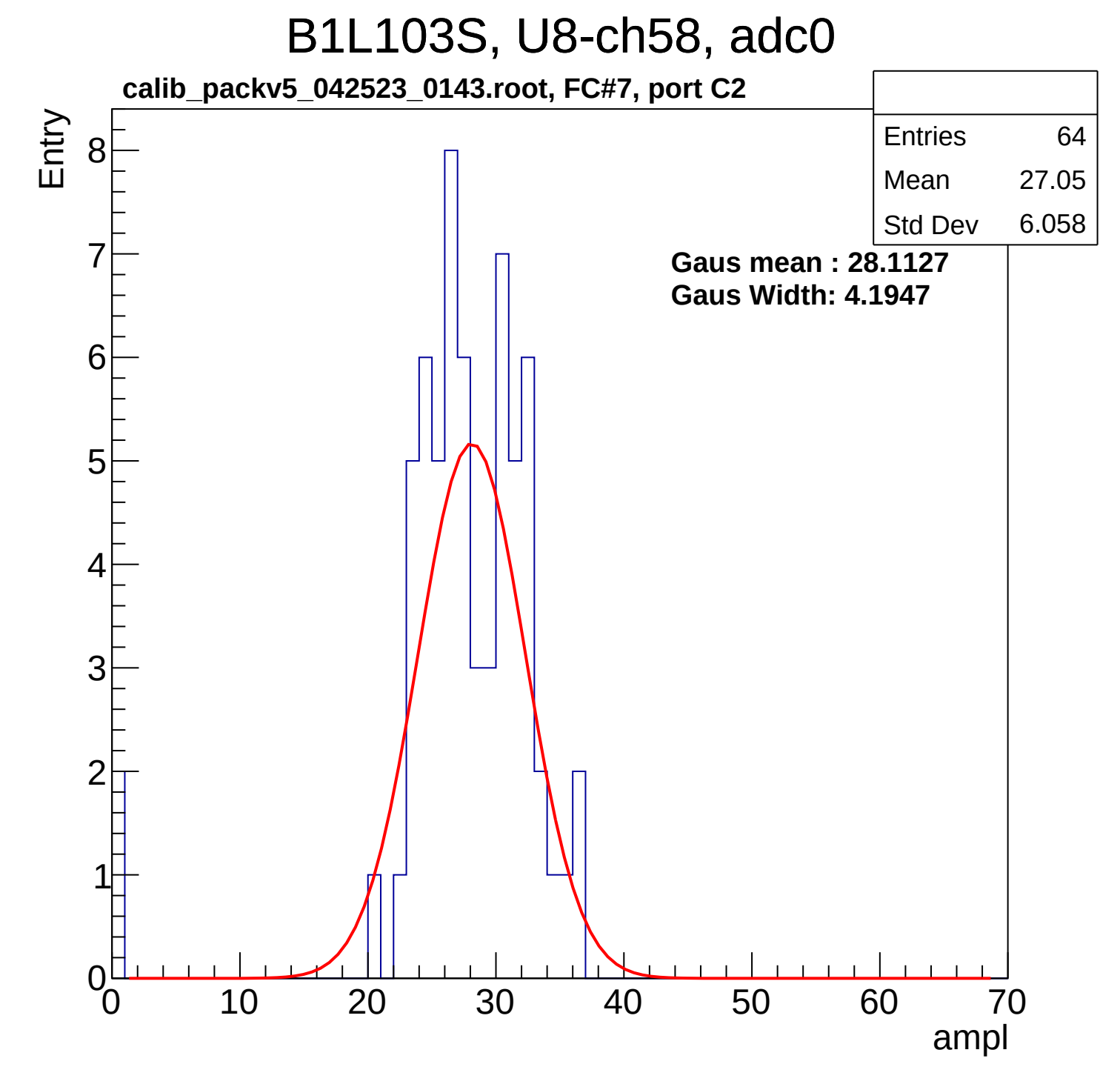

B1L103S, U8-ch57, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 49.44
Std Dev 3.149
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

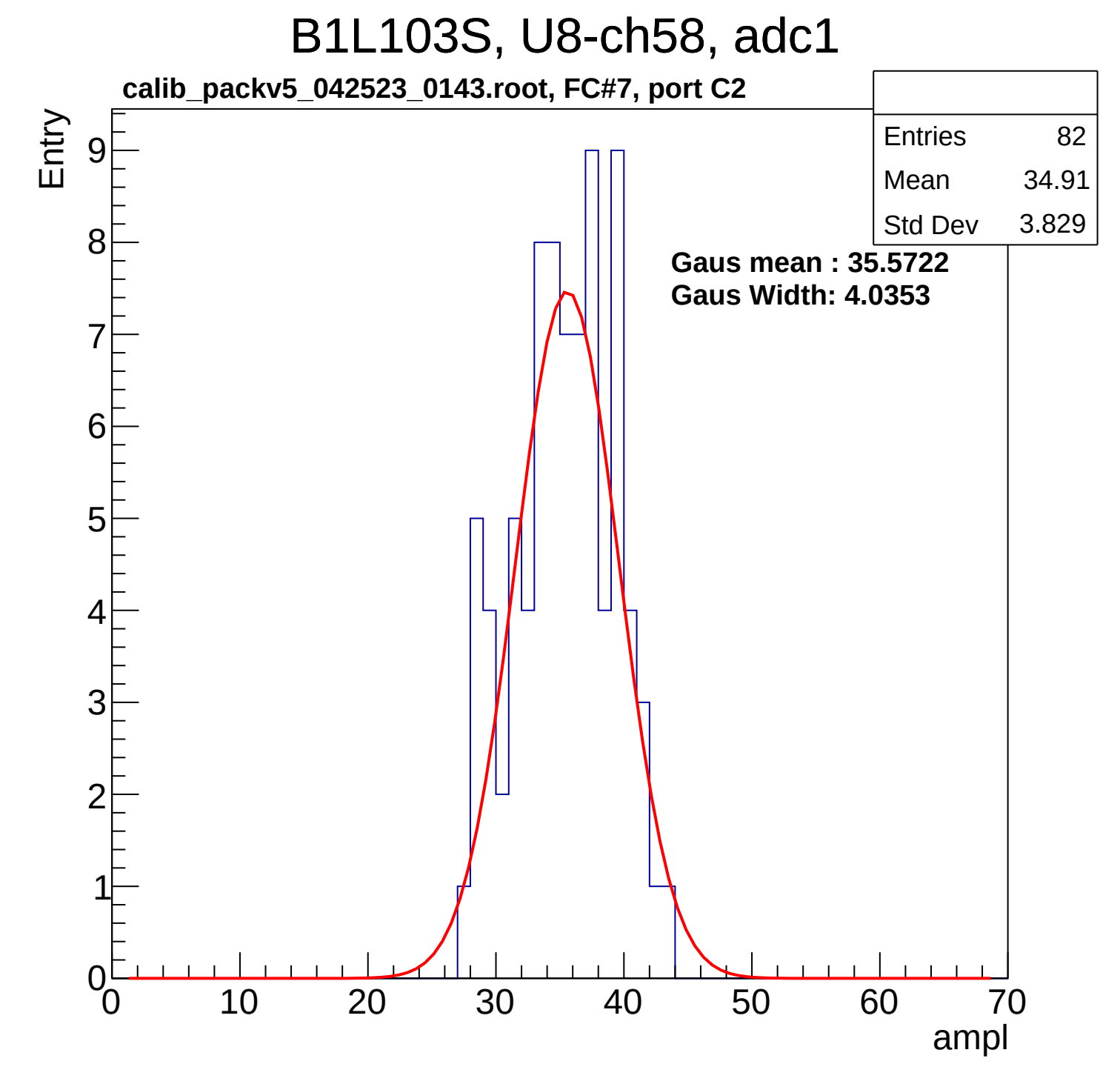

B1L103S, U8-ch57, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 55.27
Std Dev 3.098
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

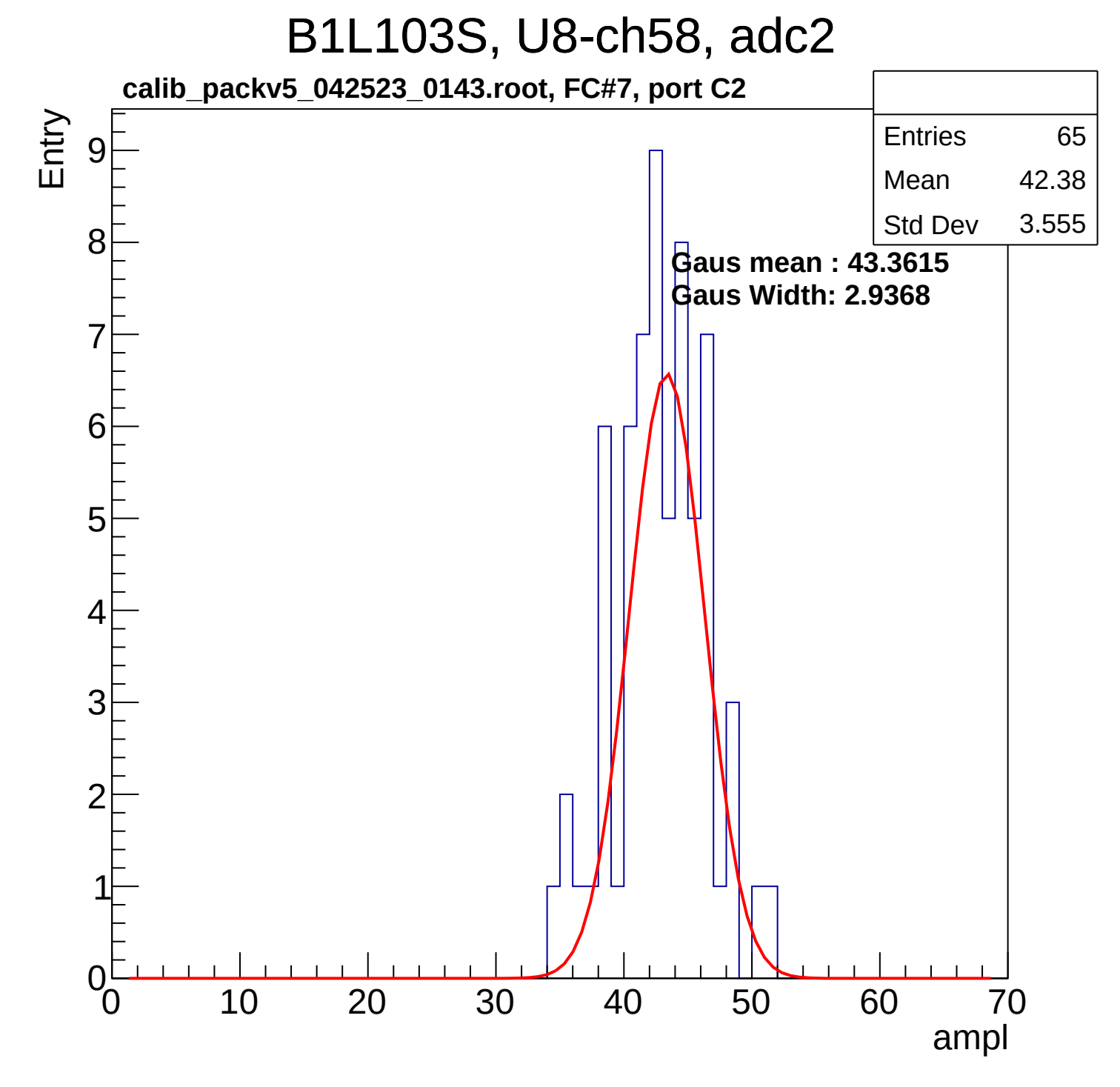

B1L103S, U8-ch57, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 45
Mean 58.78
Std Dev 9.075
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

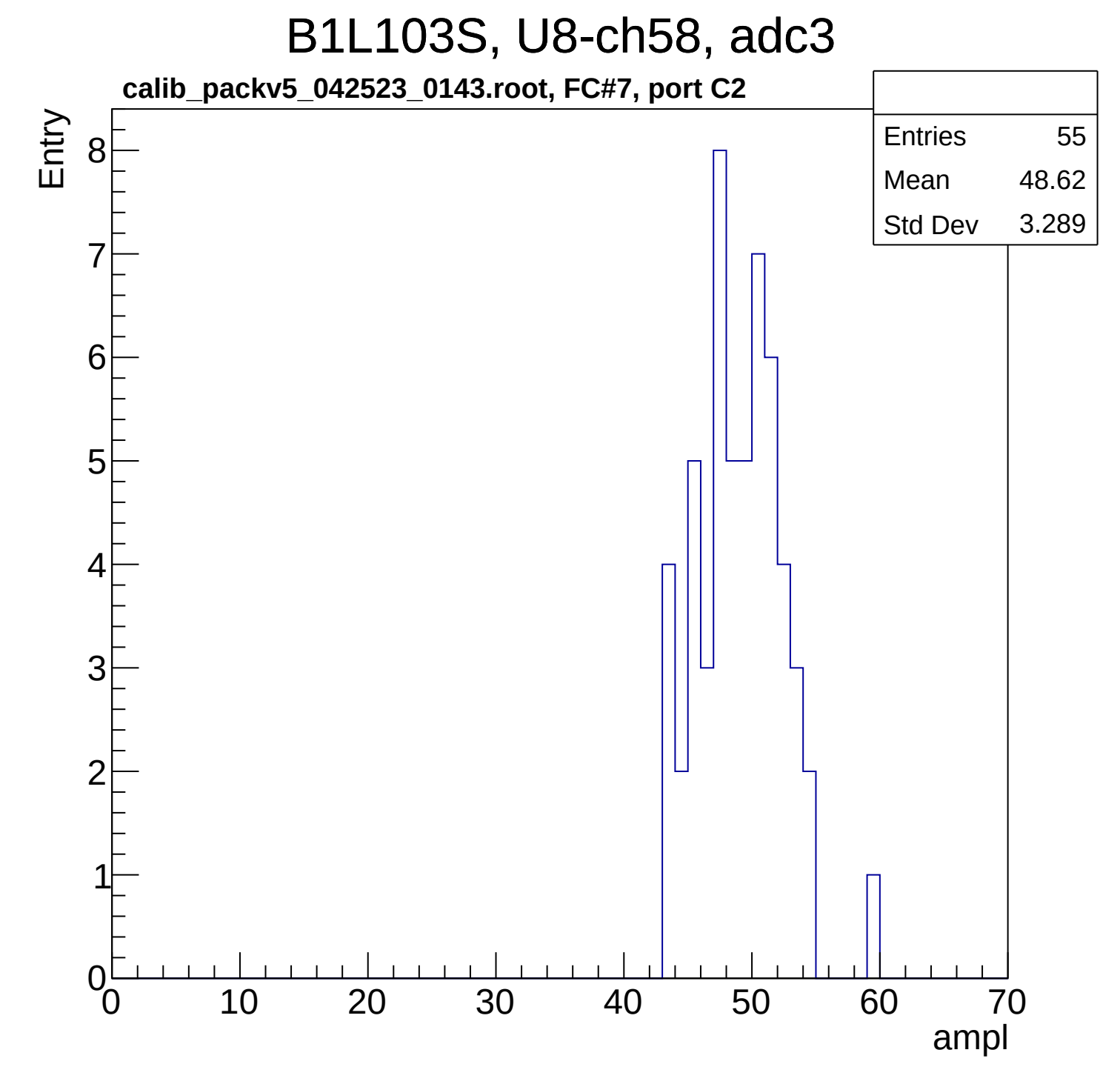

B1L103S, U8-ch57, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 62.17
Std Dev 1.462
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

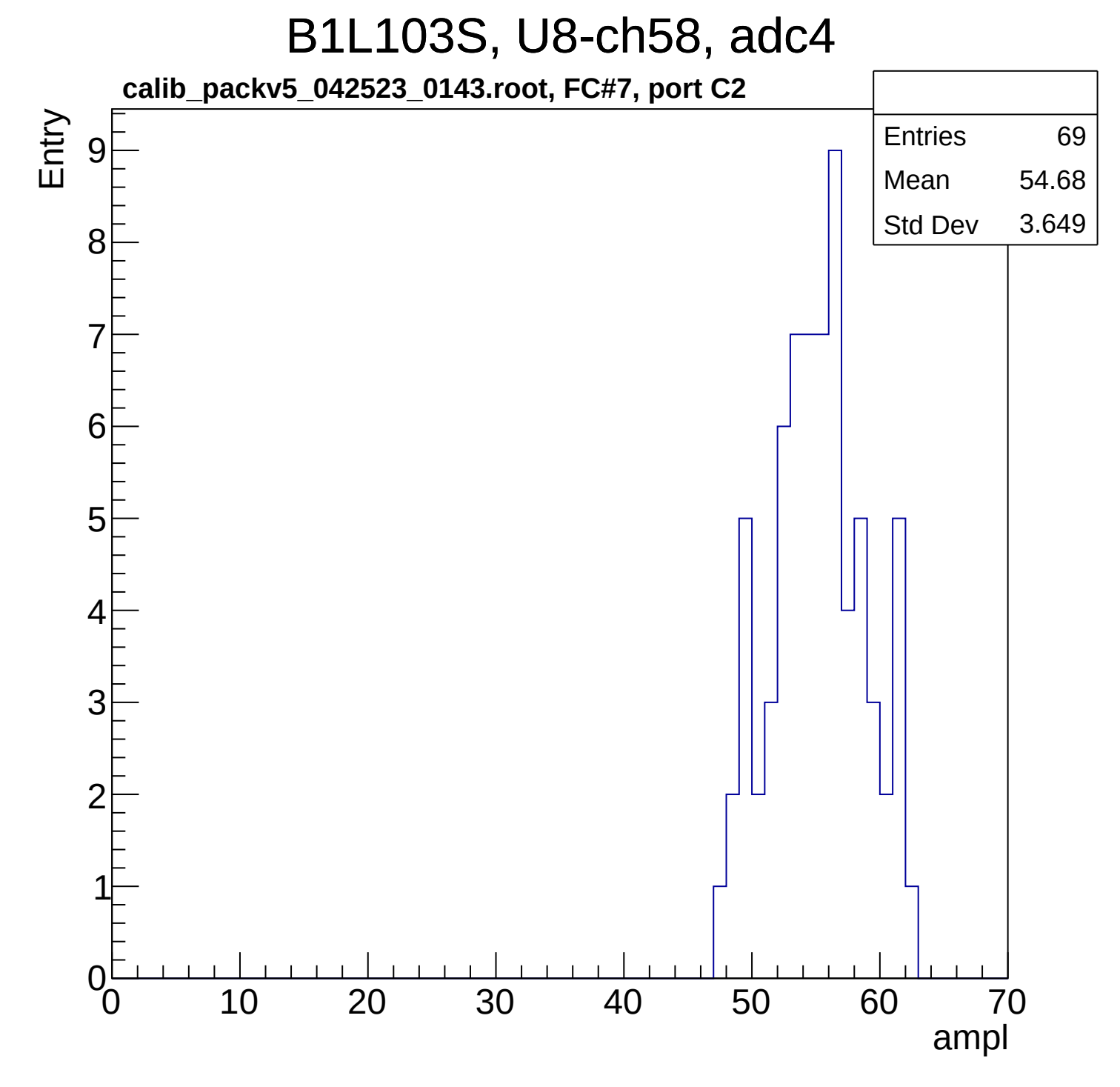

B1L103S, U8-ch57, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

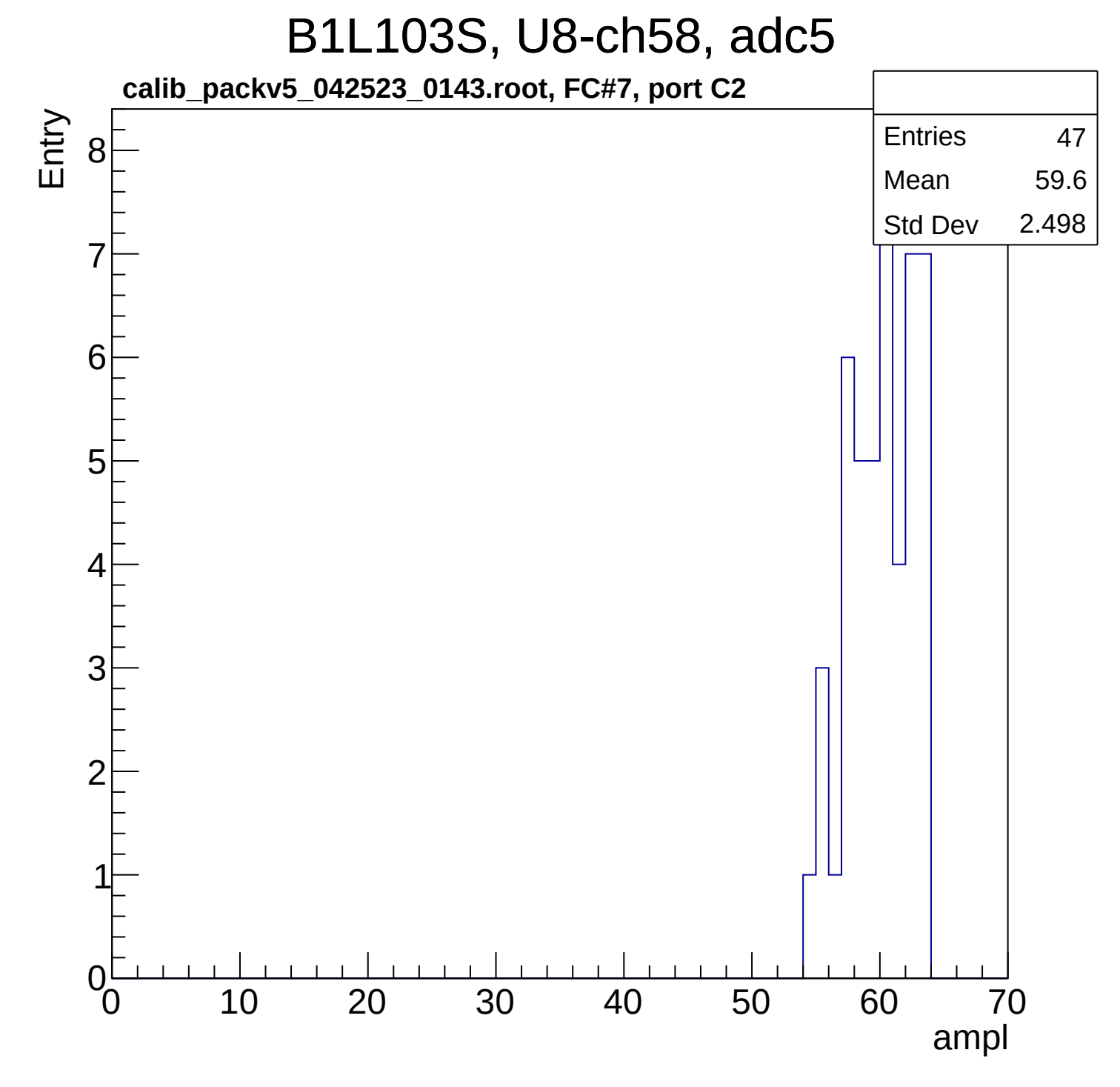

B1L103S, U8-ch58, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 27.05
Std Dev 6.058
Gaus mean : 28.1127
Gaus Width: 4.1947
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

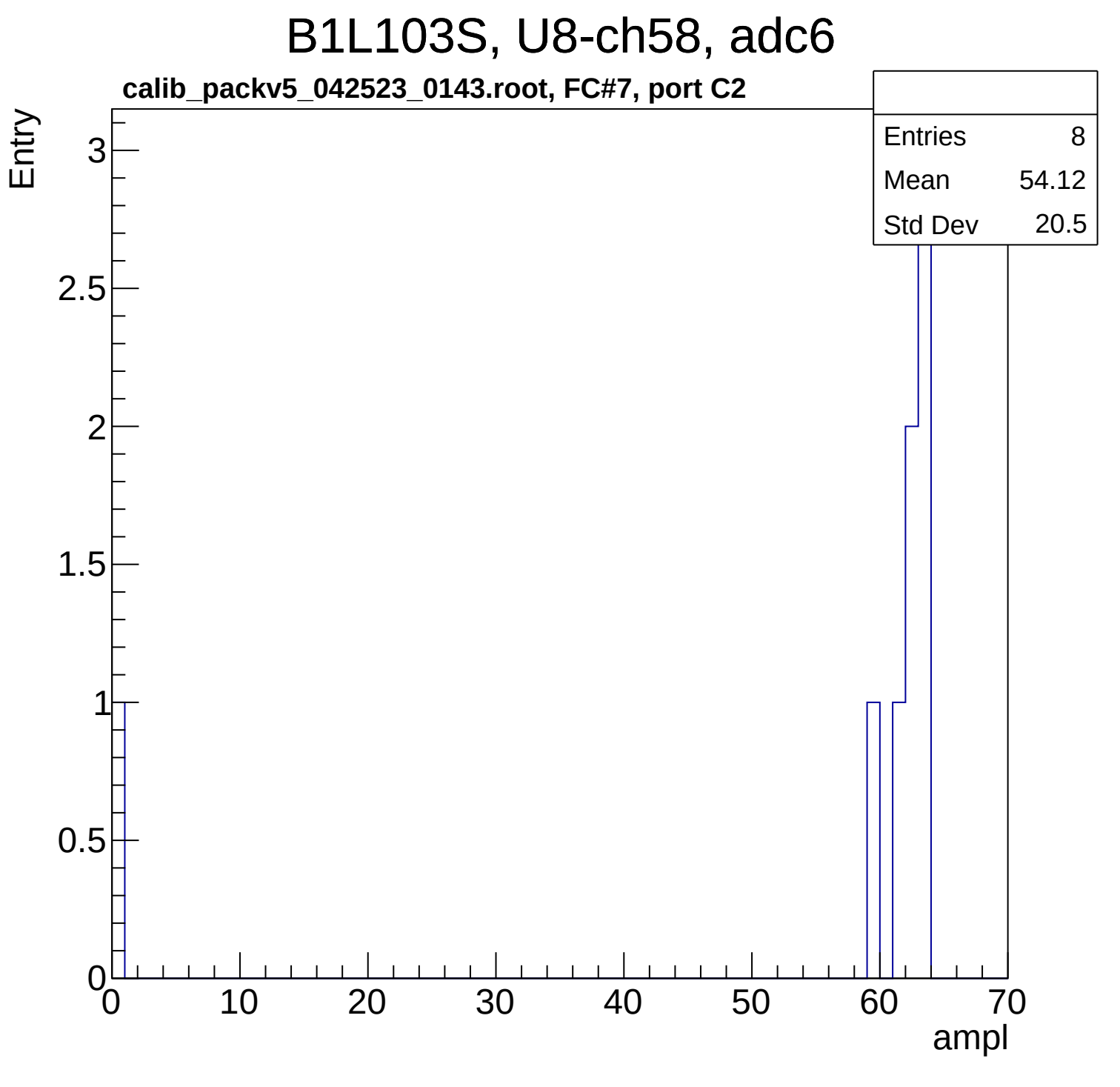

B1L103S, U8-ch58, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 82
Mean 34.91
Std Dev 3.829
Gaus mean : 35.5722
Gaus Width: 4.0353
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

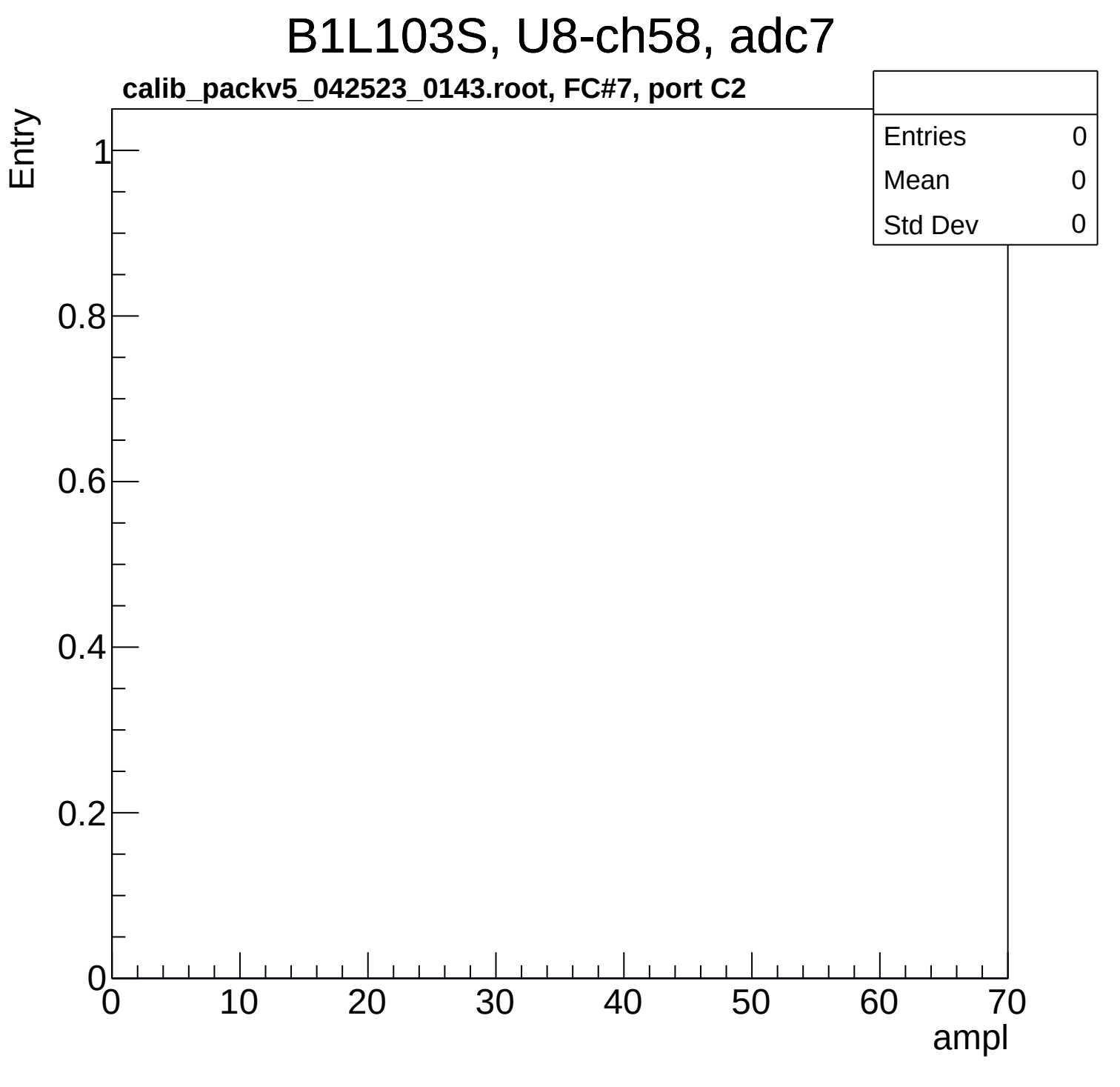

B1L103S, U8-ch58, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 42.38
Std Dev 3.555
Gaus mean : 43.3615
Gaus Width: 2.9368
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

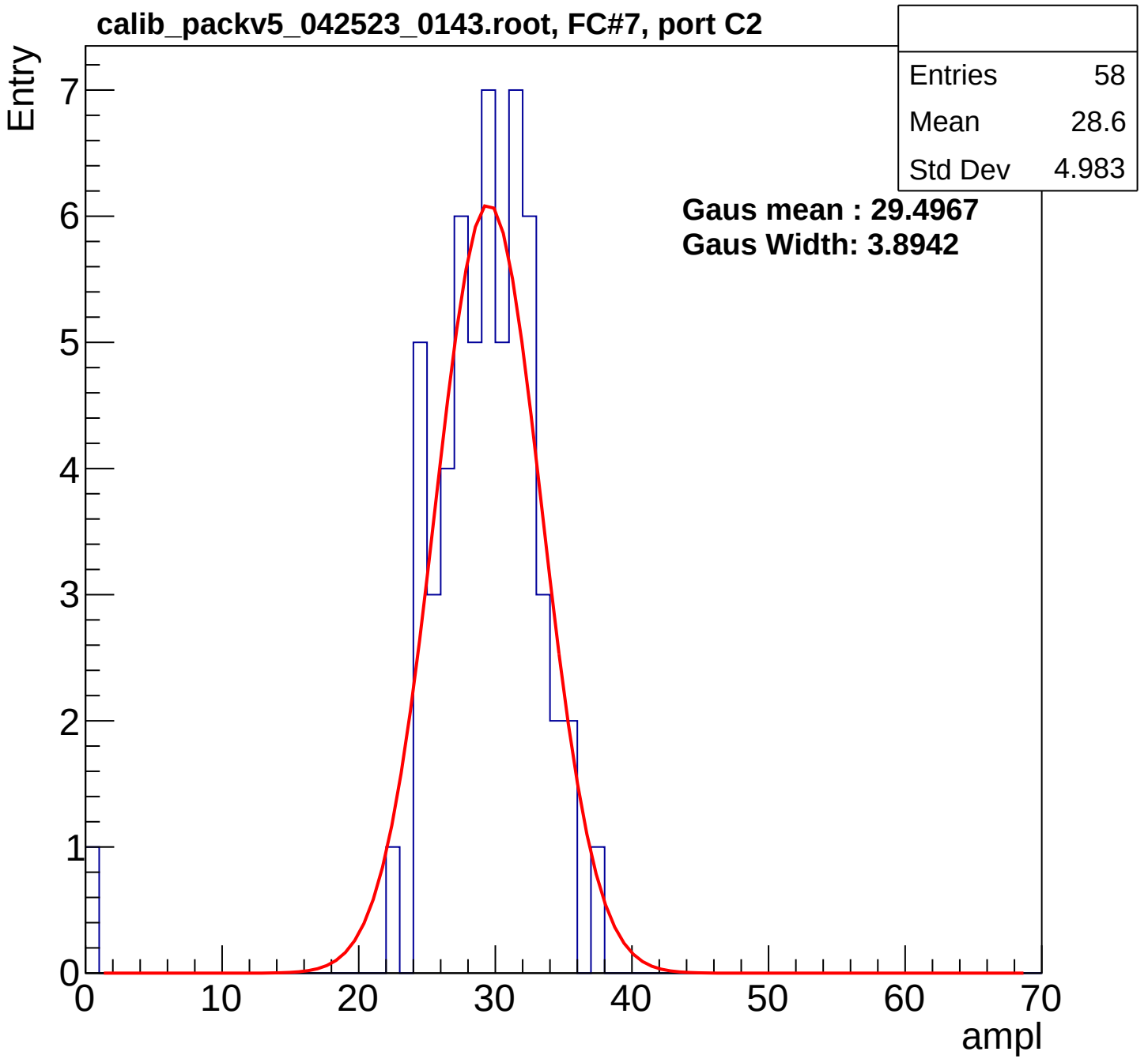

B1L103S, U8-ch58, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 48.62
Std Dev 3.289
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

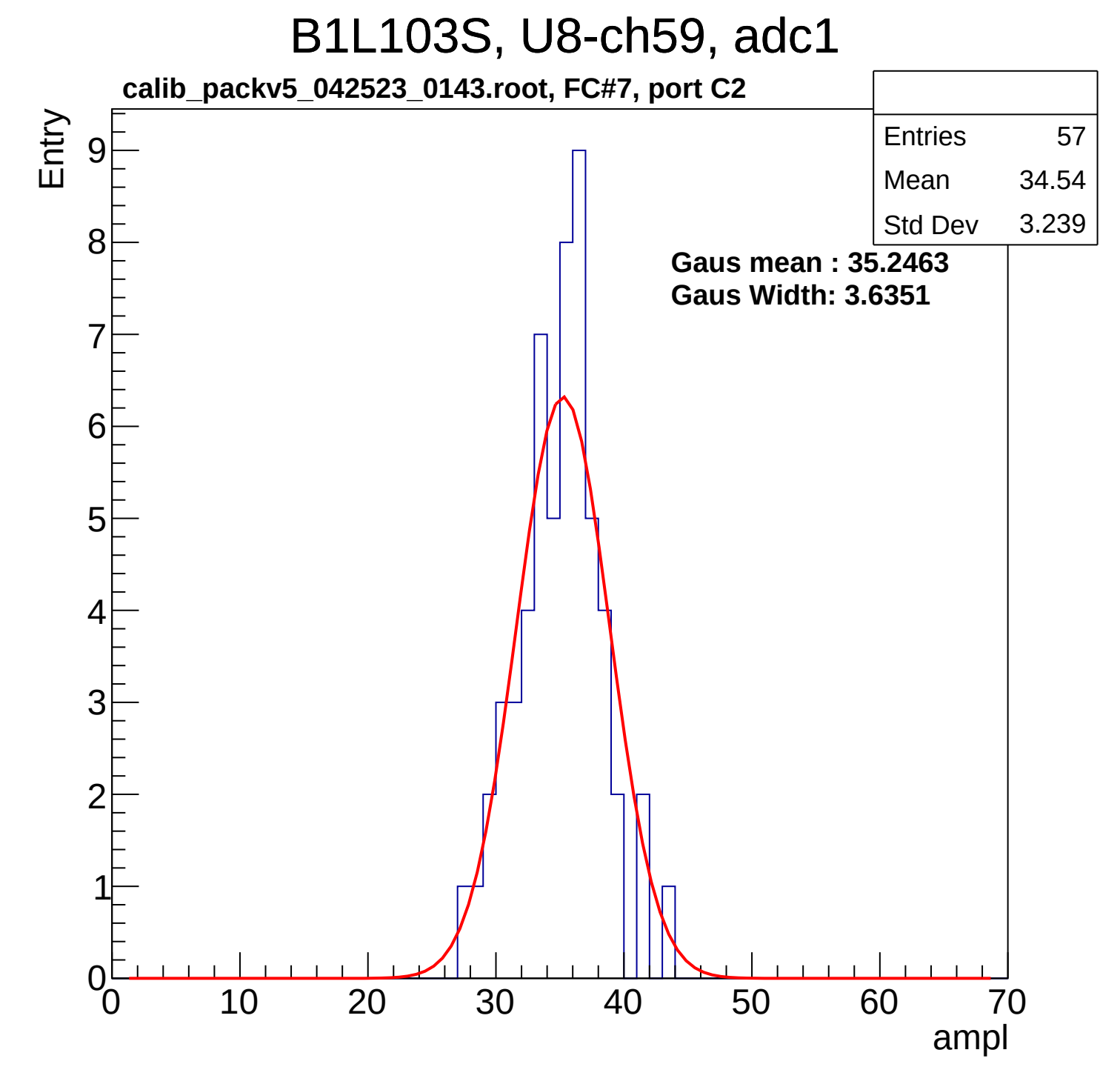

B1L103S, U8-ch58, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 54.68
Std Dev 3.649
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

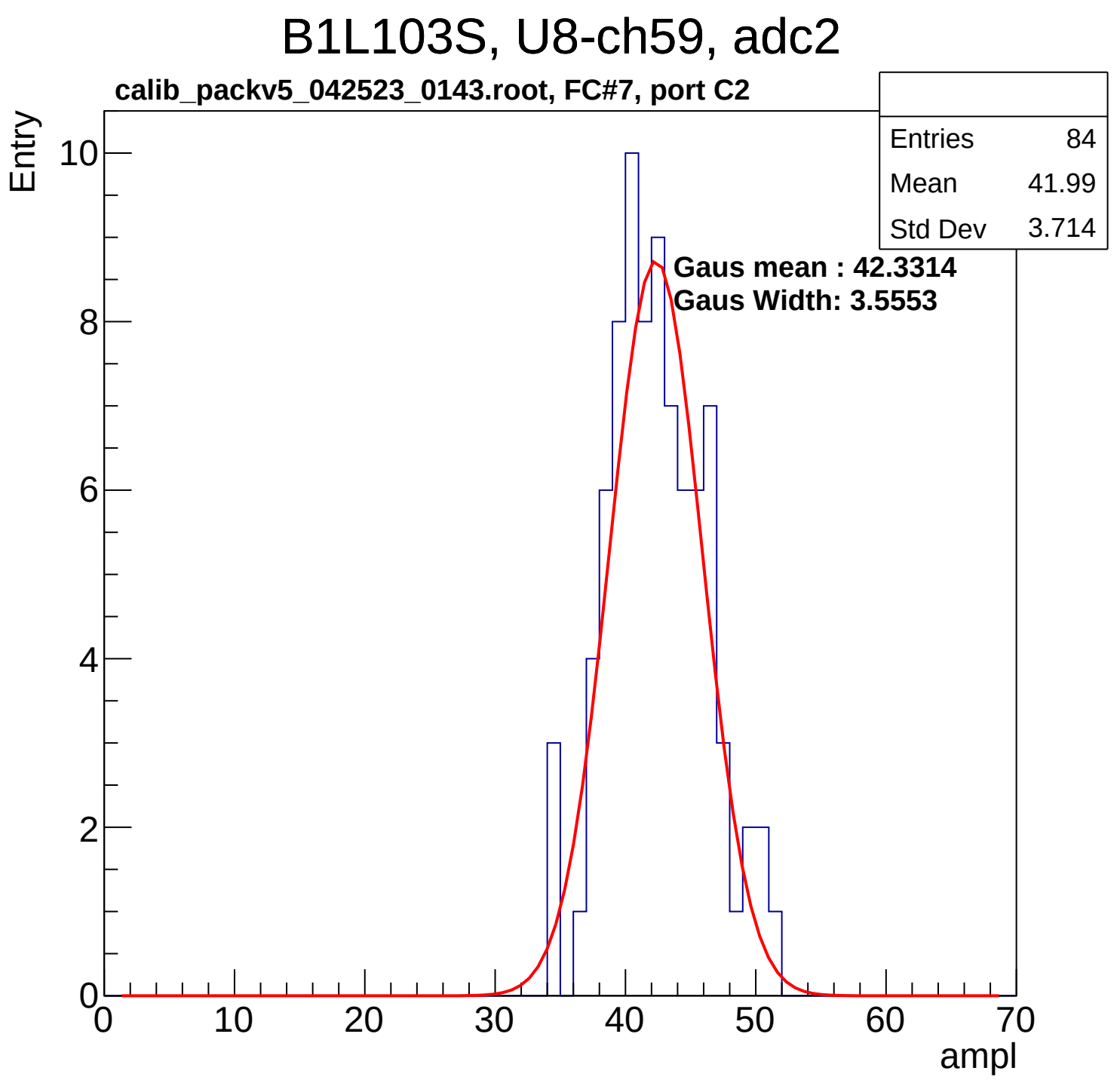

B1L103S, U8-ch58, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 59.6
Std Dev 2.498
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

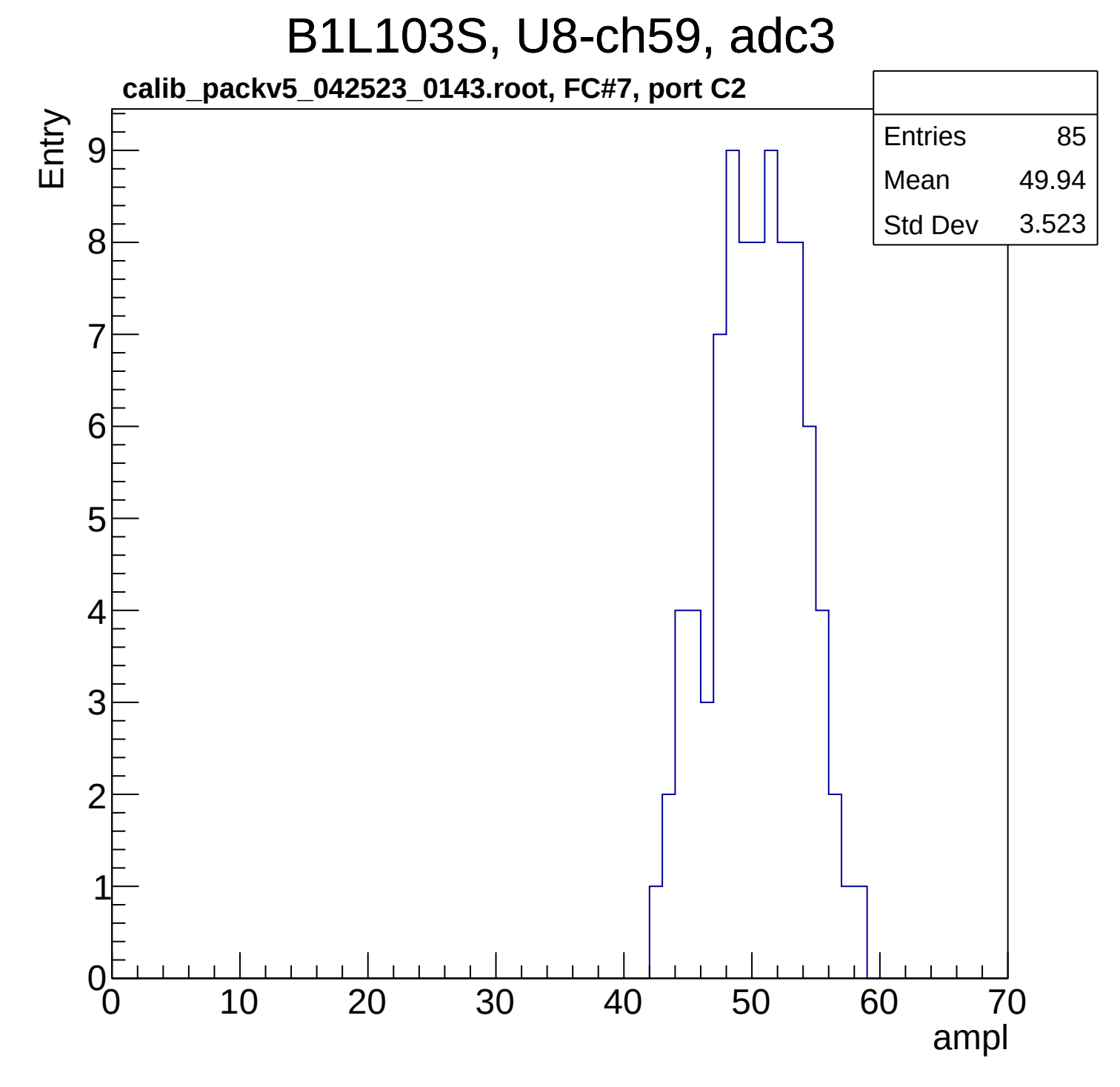

B1L103S, U8-ch58, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 8
Mean 54.12
Std Dev 20.5
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl

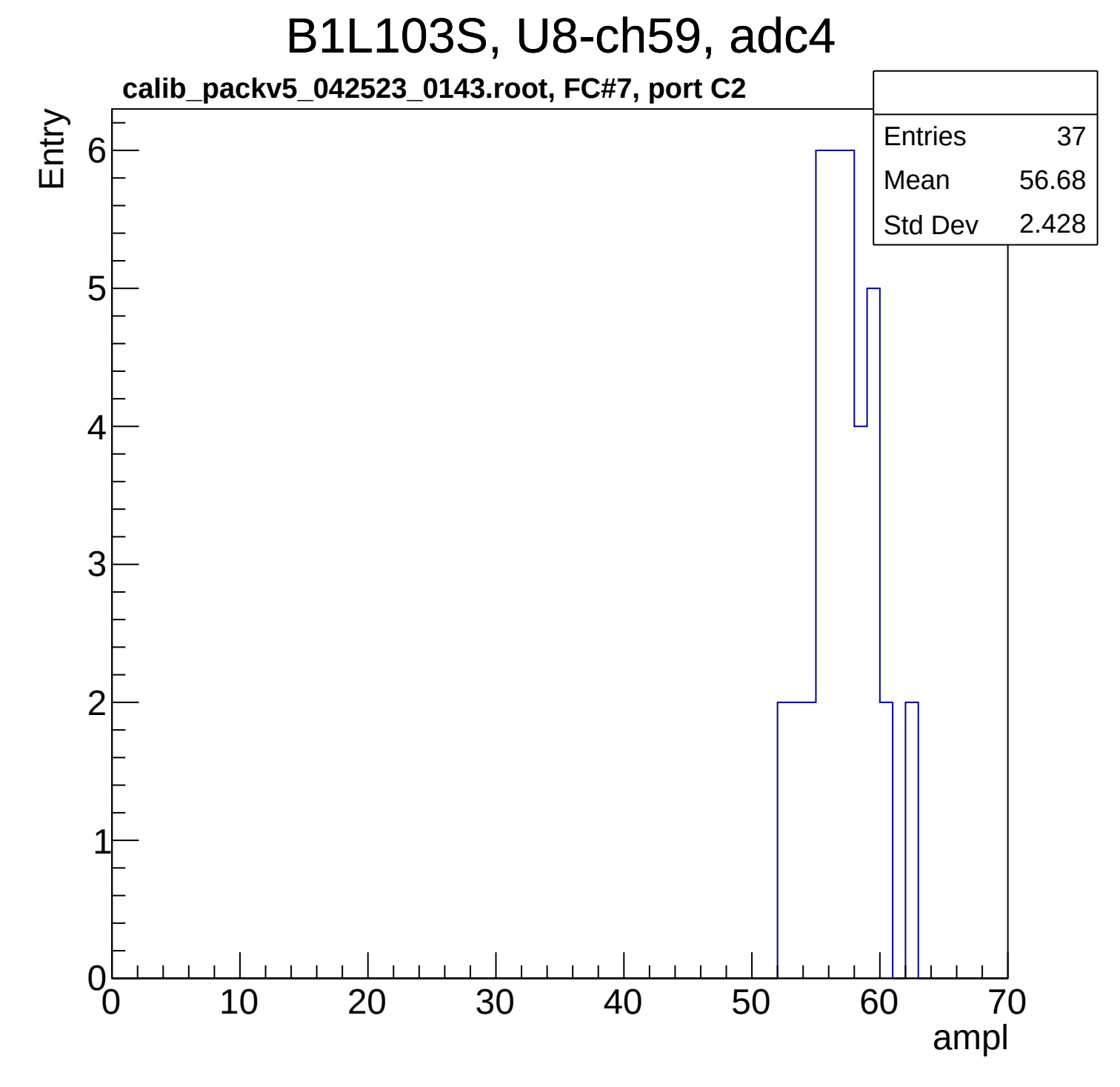

B1L103S, U8-ch58, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

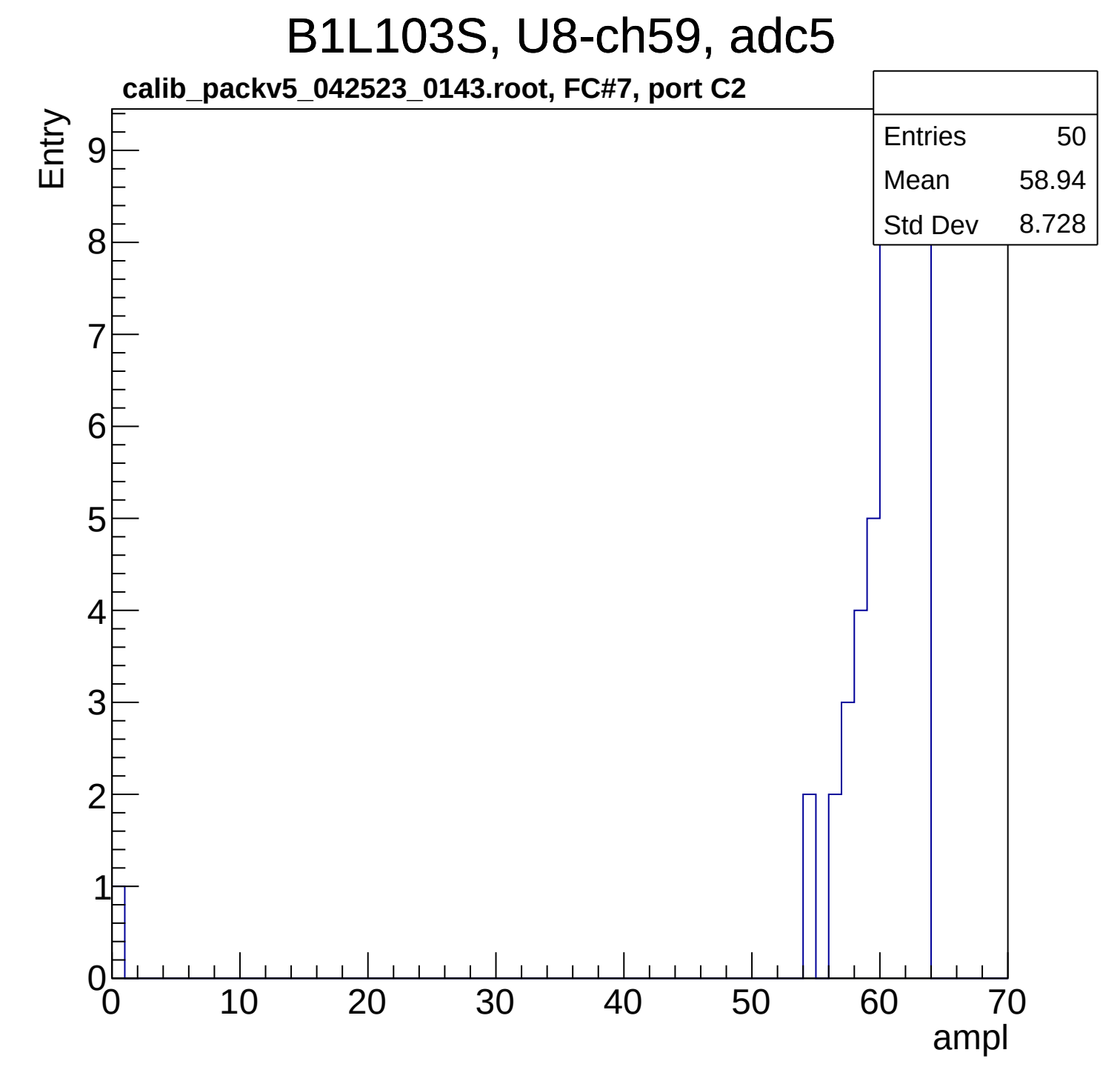

B1L103S, U8-ch59, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 28.6
Std Dev 4.983
Gaus mean : 29.4967
Gaus Width: 3.8942
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

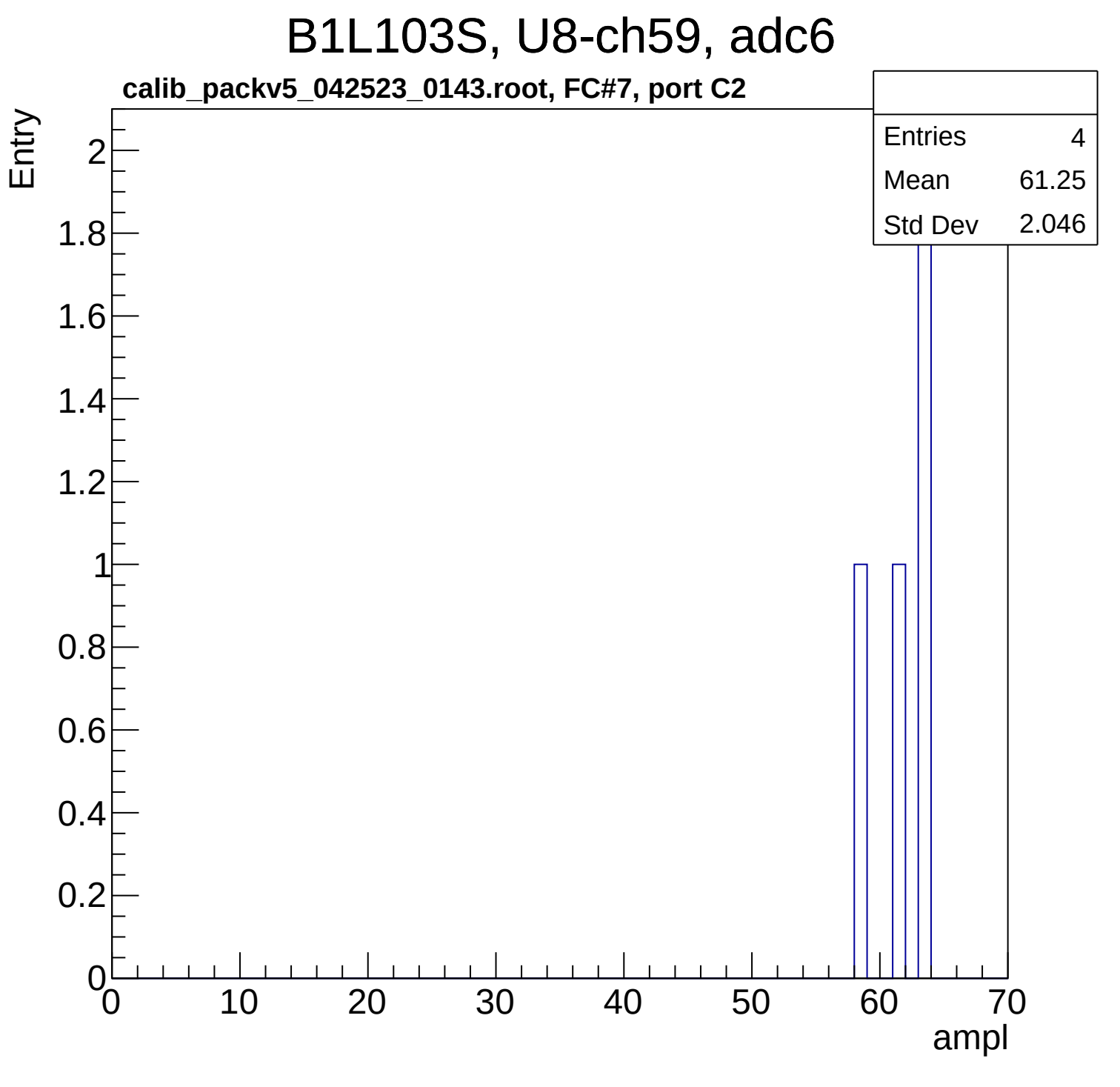

B1L103S, U8-ch59, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 34.54
Std Dev 3.239
Gaus mean : 35.2463
Gaus Width: 3.6351
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

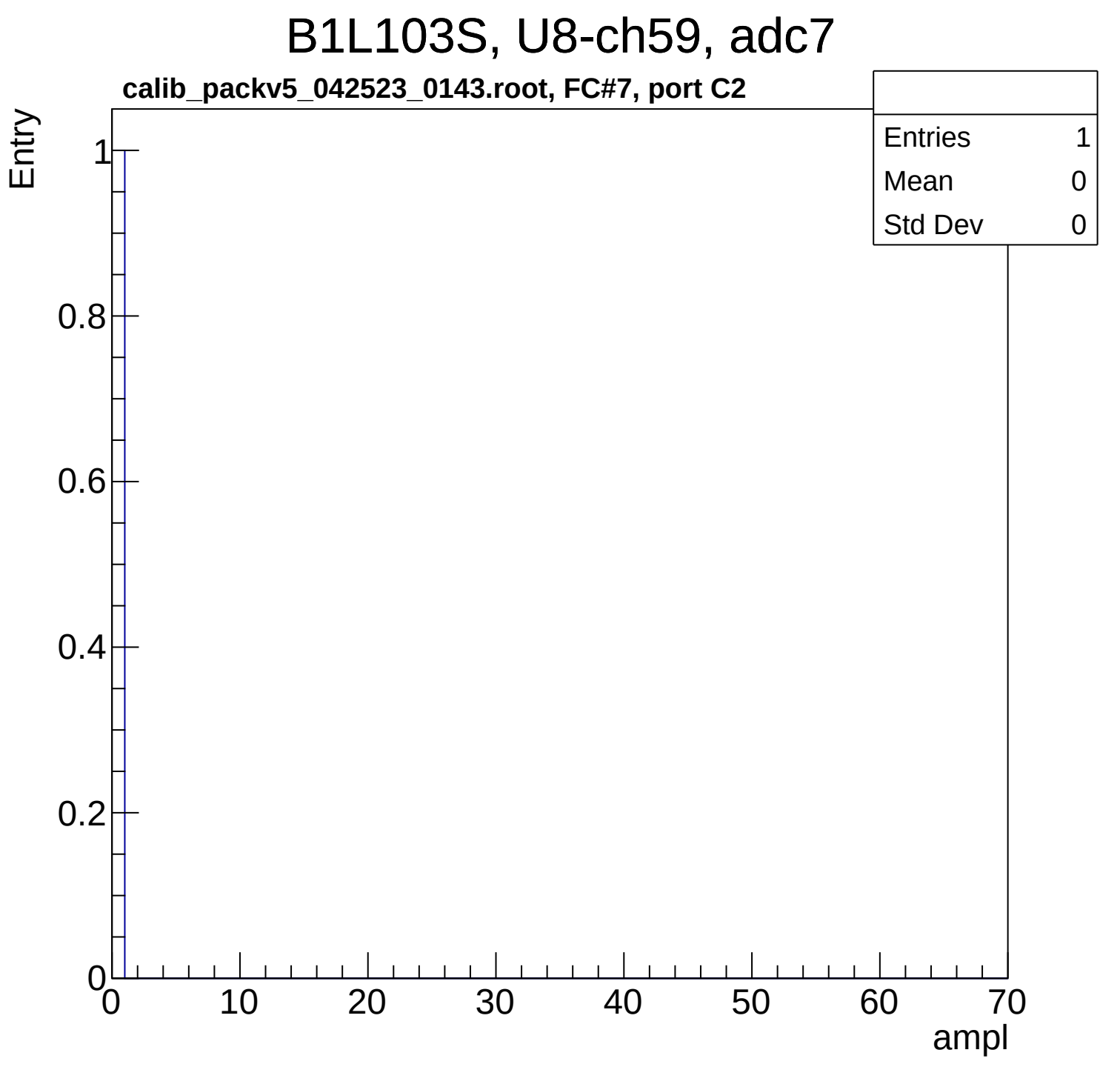

B1L103S, U8-ch59, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 84
Mean 41.99
Std Dev 3.714
Gaus mean : 42.3314
Gaus Width: 3.5553
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

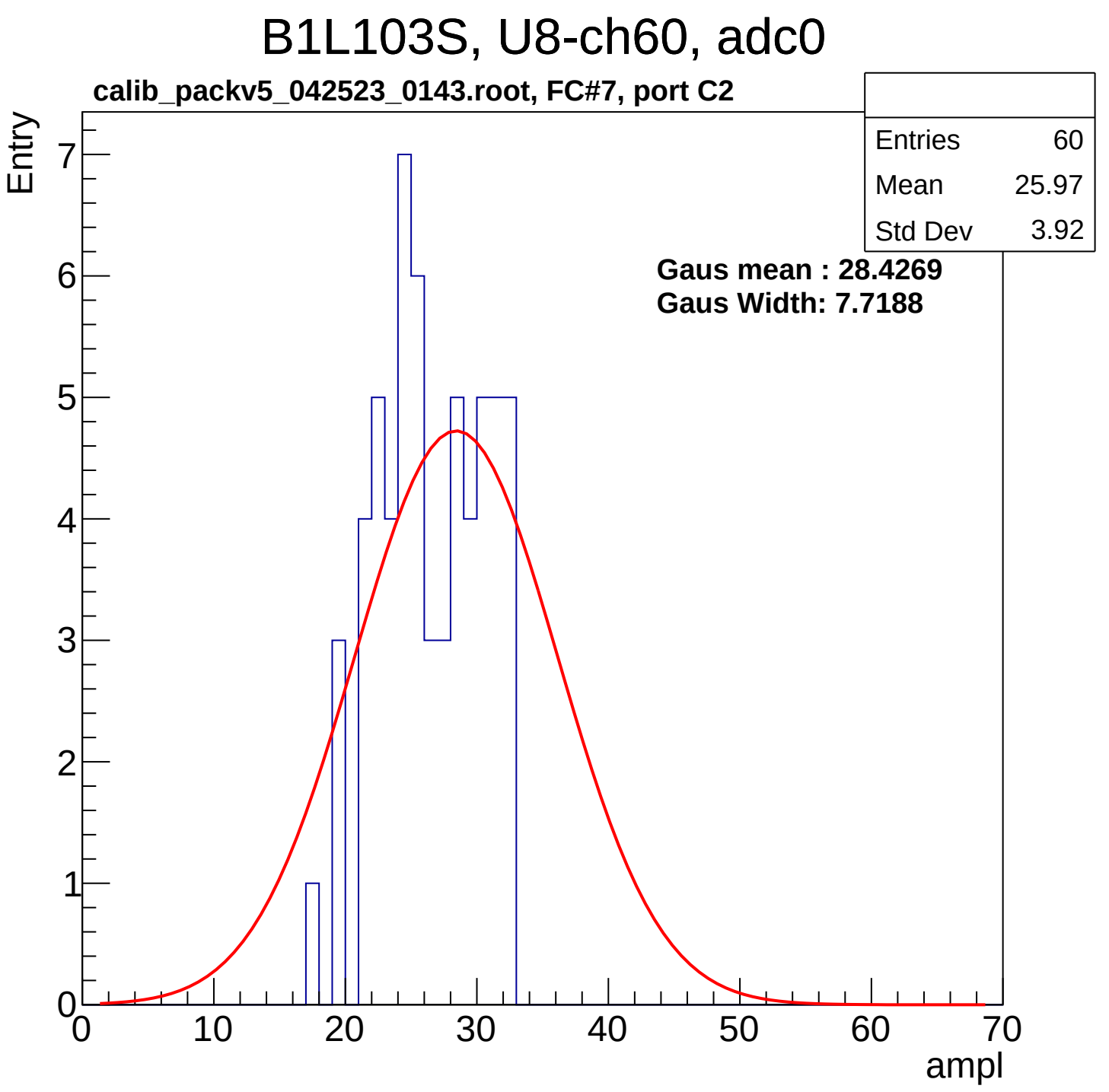

B1L103S, U8-ch59, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 85
Mean 49.94
Std Dev 3.523
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

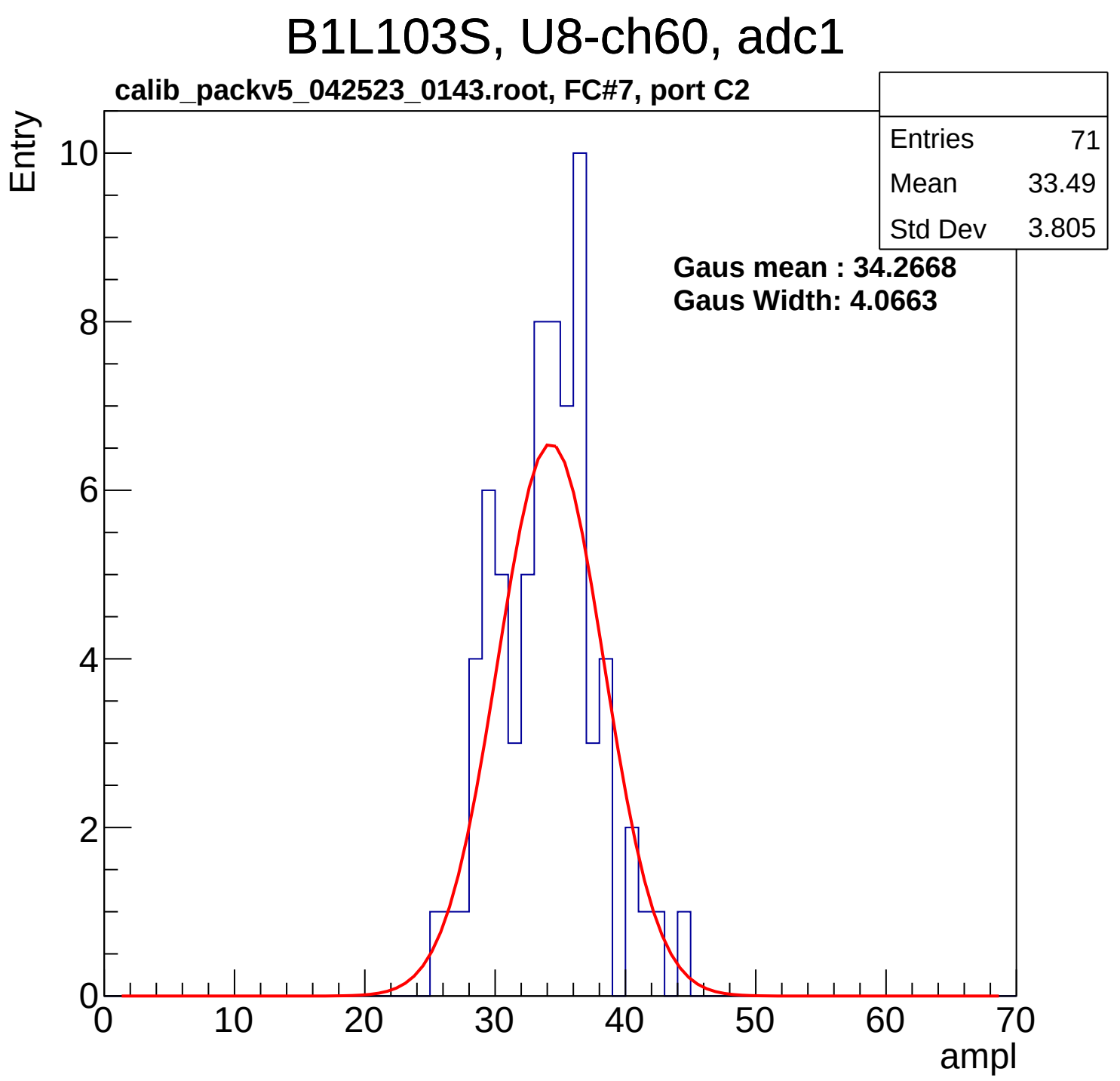

B1L103S, U8-ch59, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 37
Mean 56.68
Std Dev 2.428
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

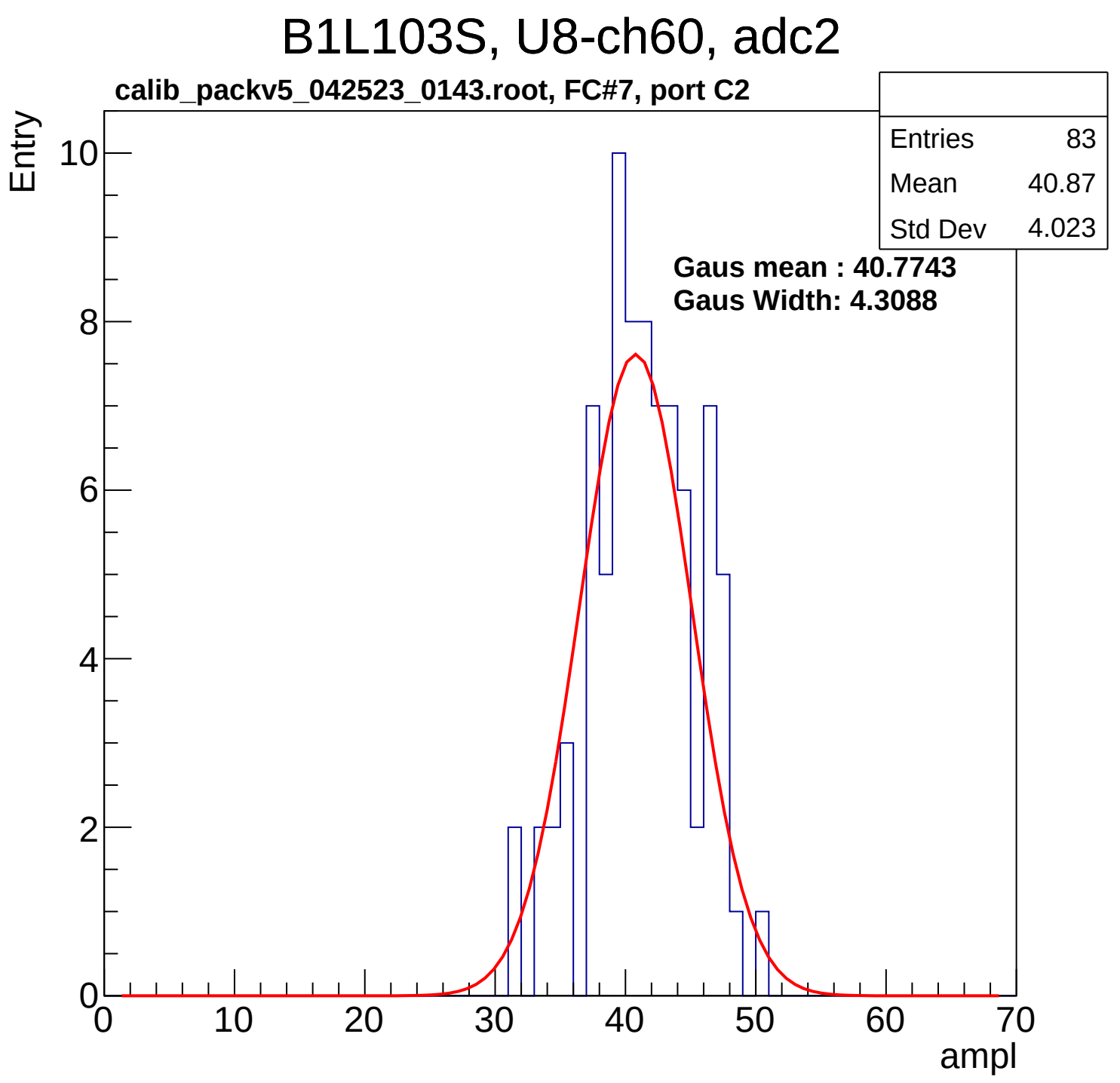

B1L103S, U8-ch59, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 58.94
Std Dev 8.728
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

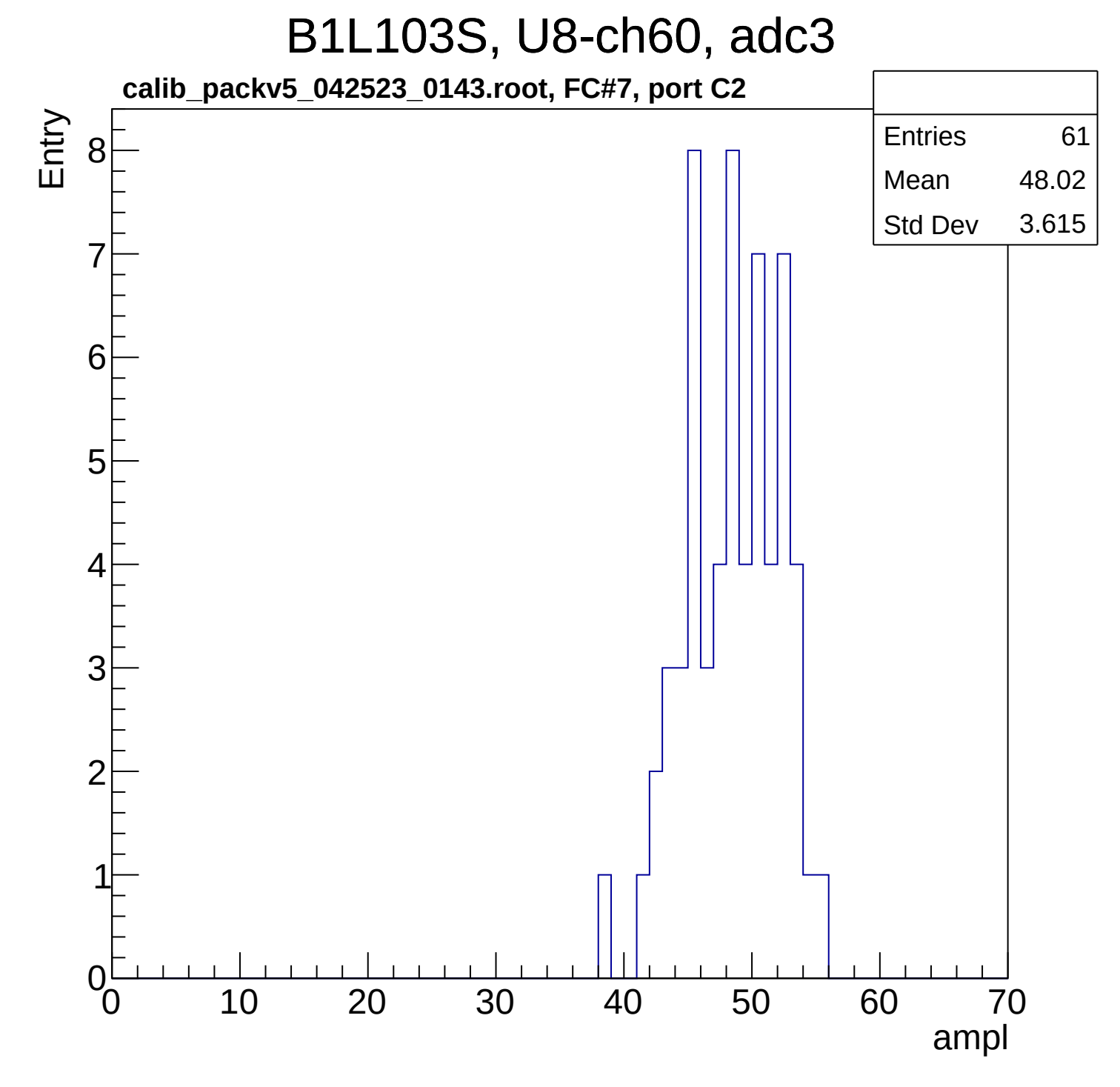

B1L103S, U8-ch59, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 61.25
Std Dev 2.046
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

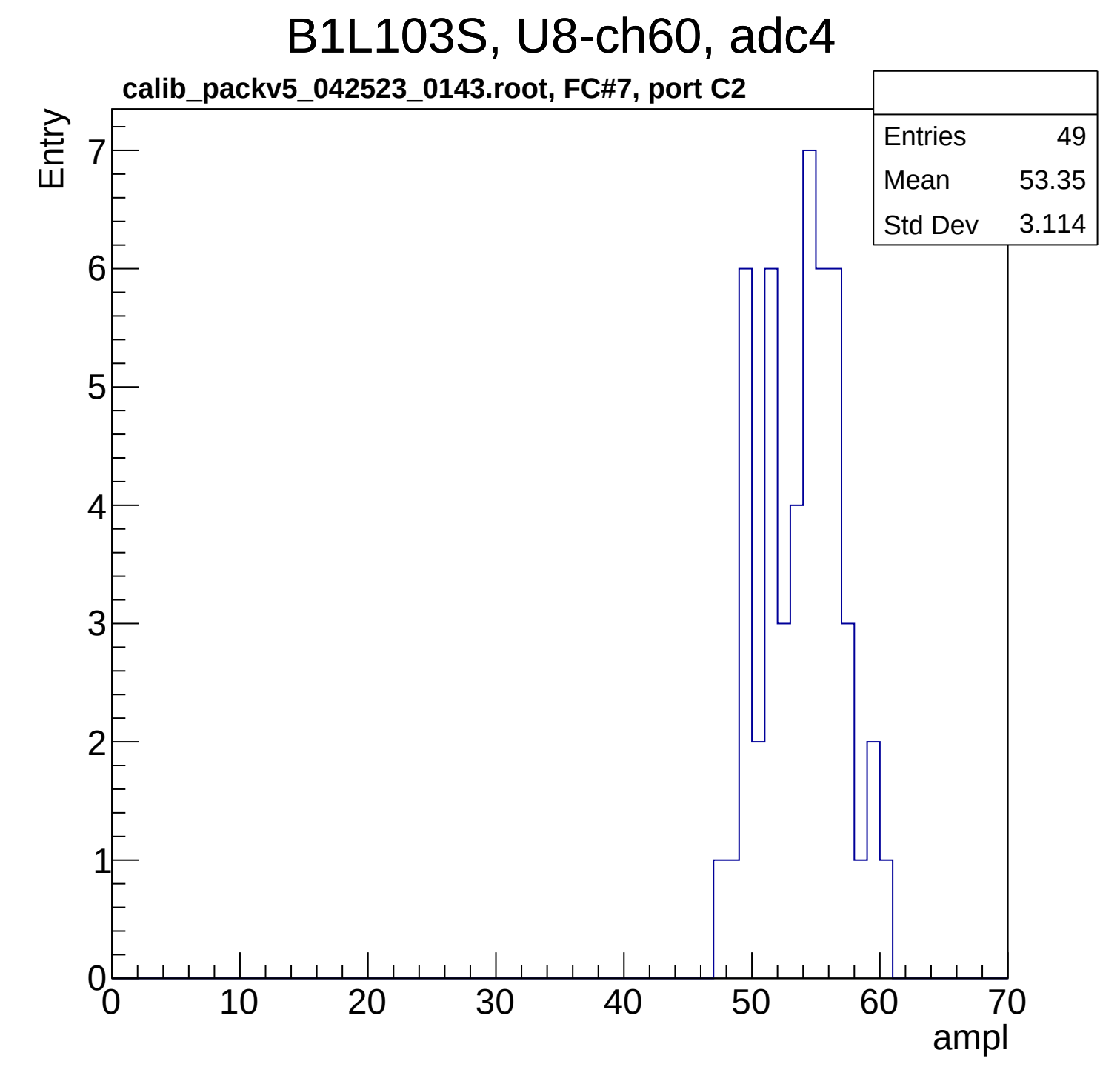

B1L103S, U8-ch59, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

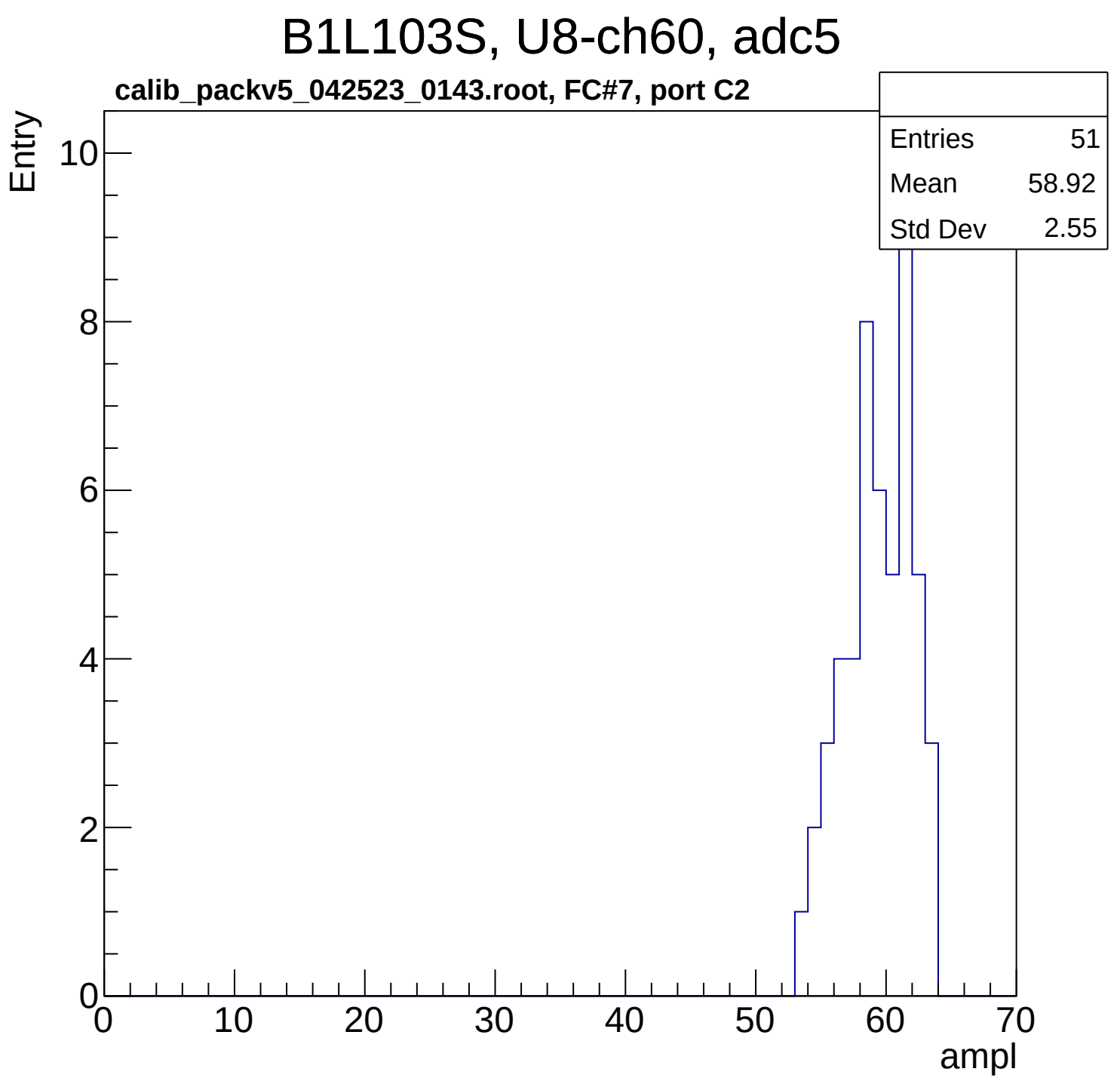

B1L103S, U8-ch60, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 25.97
Std Dev 3.92
Gaus mean : 28.4269
Gaus Width: 7.7188
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

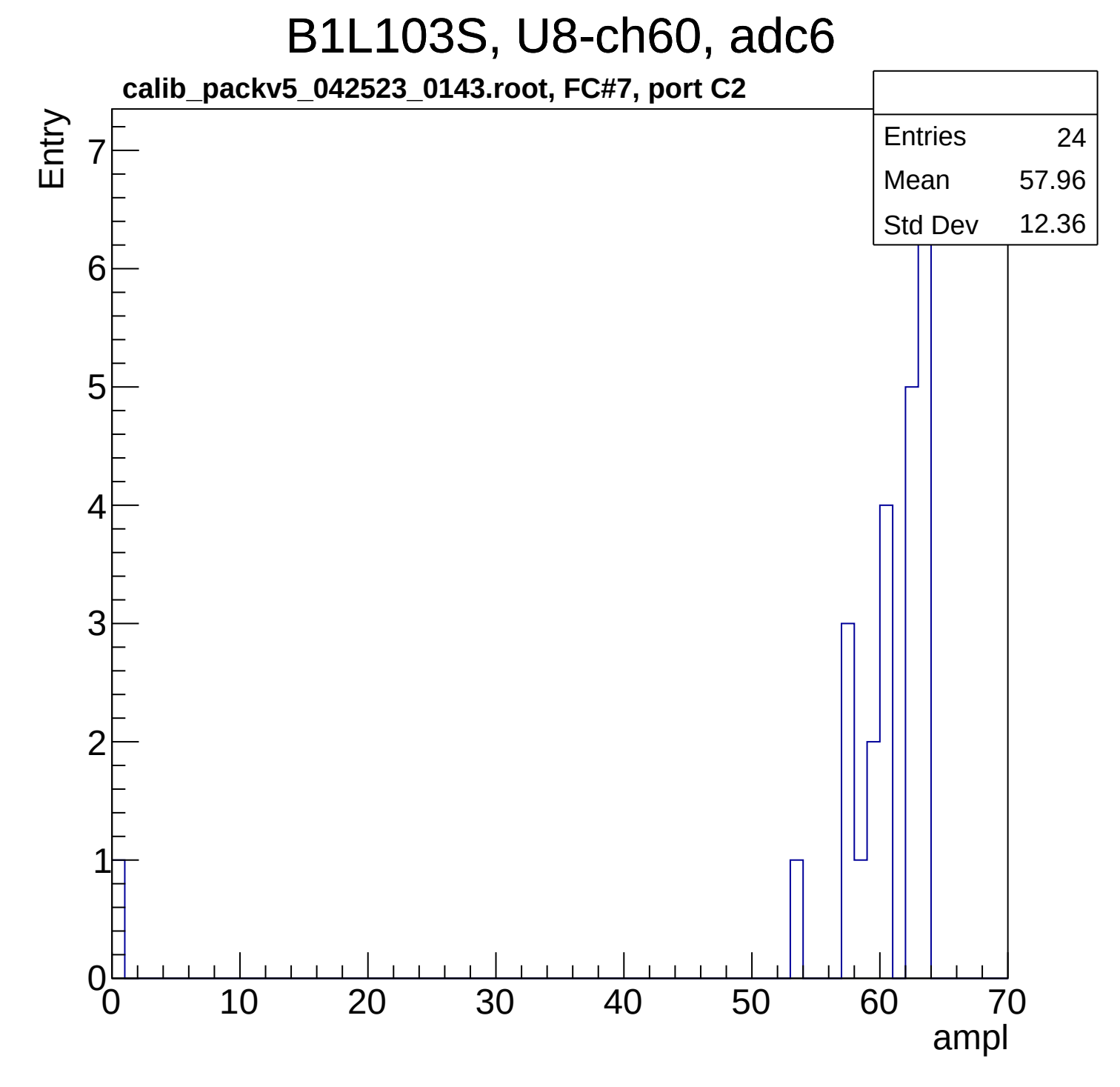

B1L103S, U8-ch60, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 33.49
Std Dev 3.805
Gaus mean : 34.2668
Gaus Width: 4.0663
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

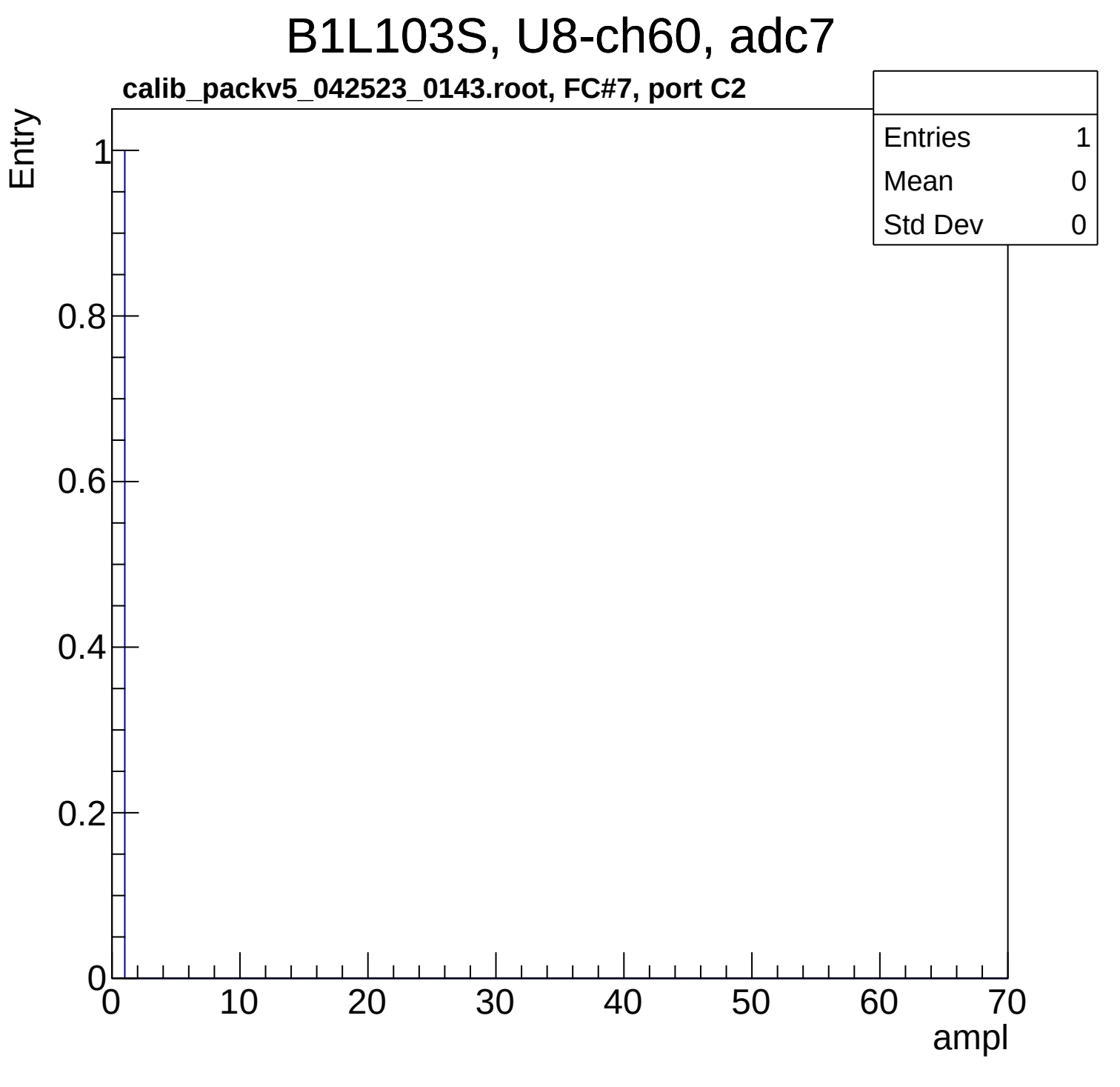

B1L103S, U8-ch60, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 83
Mean 40.87
Std Dev 4.023
Gaus mean : 40.7743
Gaus Width: 4.3088
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

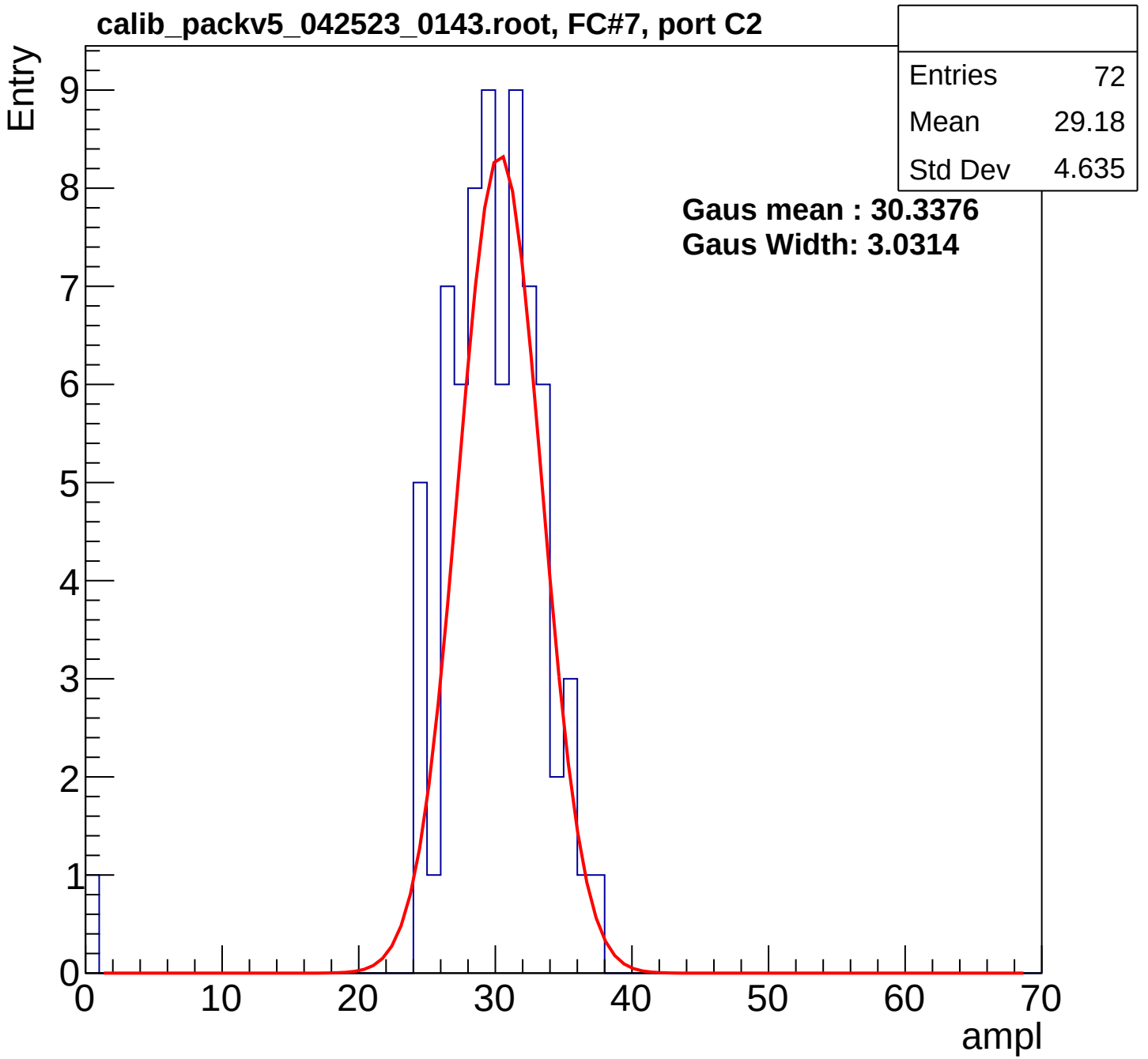

B1L103S, U8-ch60, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 48.02
Std Dev 3.615
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

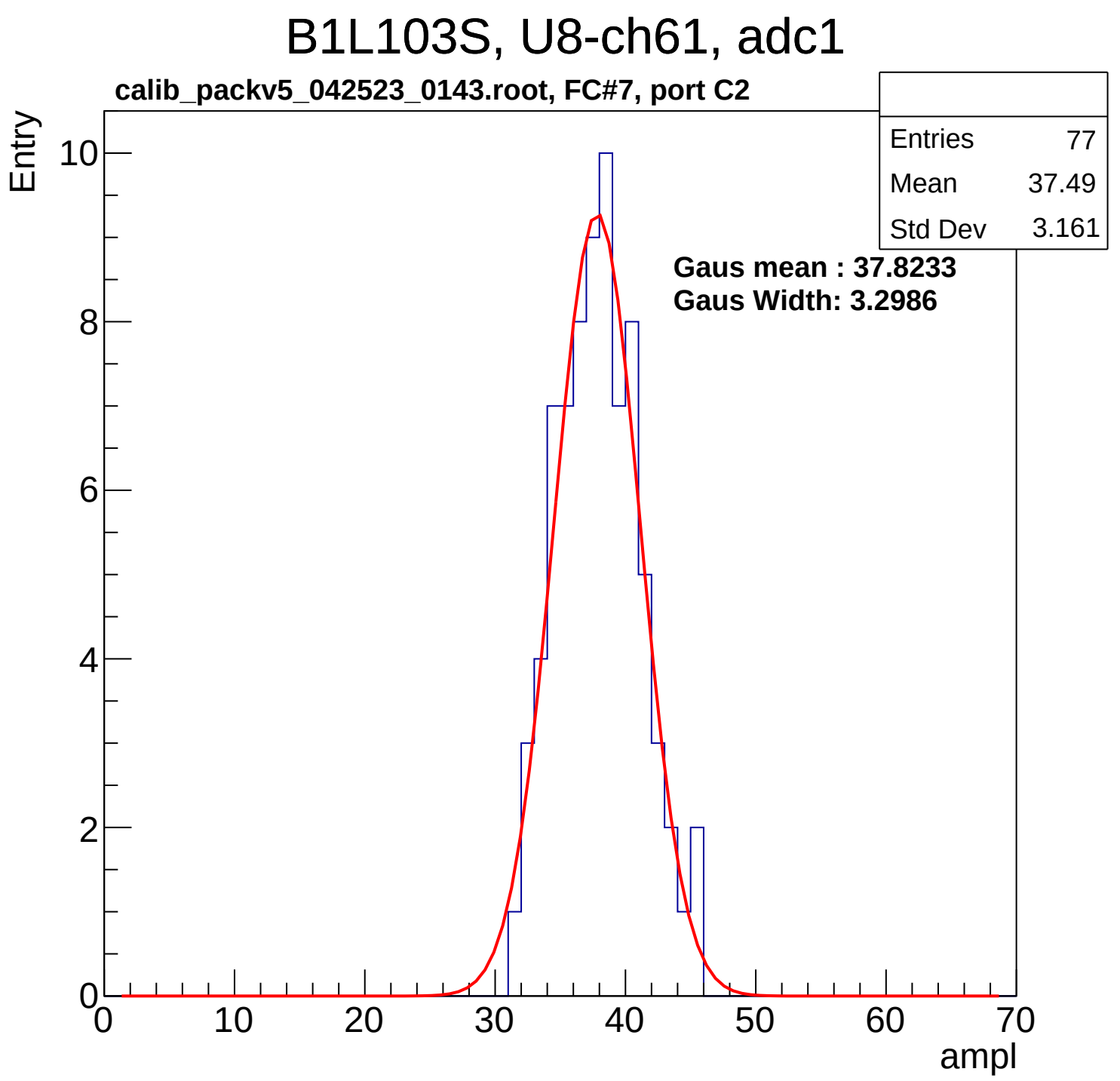

B1L103S, U8-ch60, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 53.35
Std Dev 3.114
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

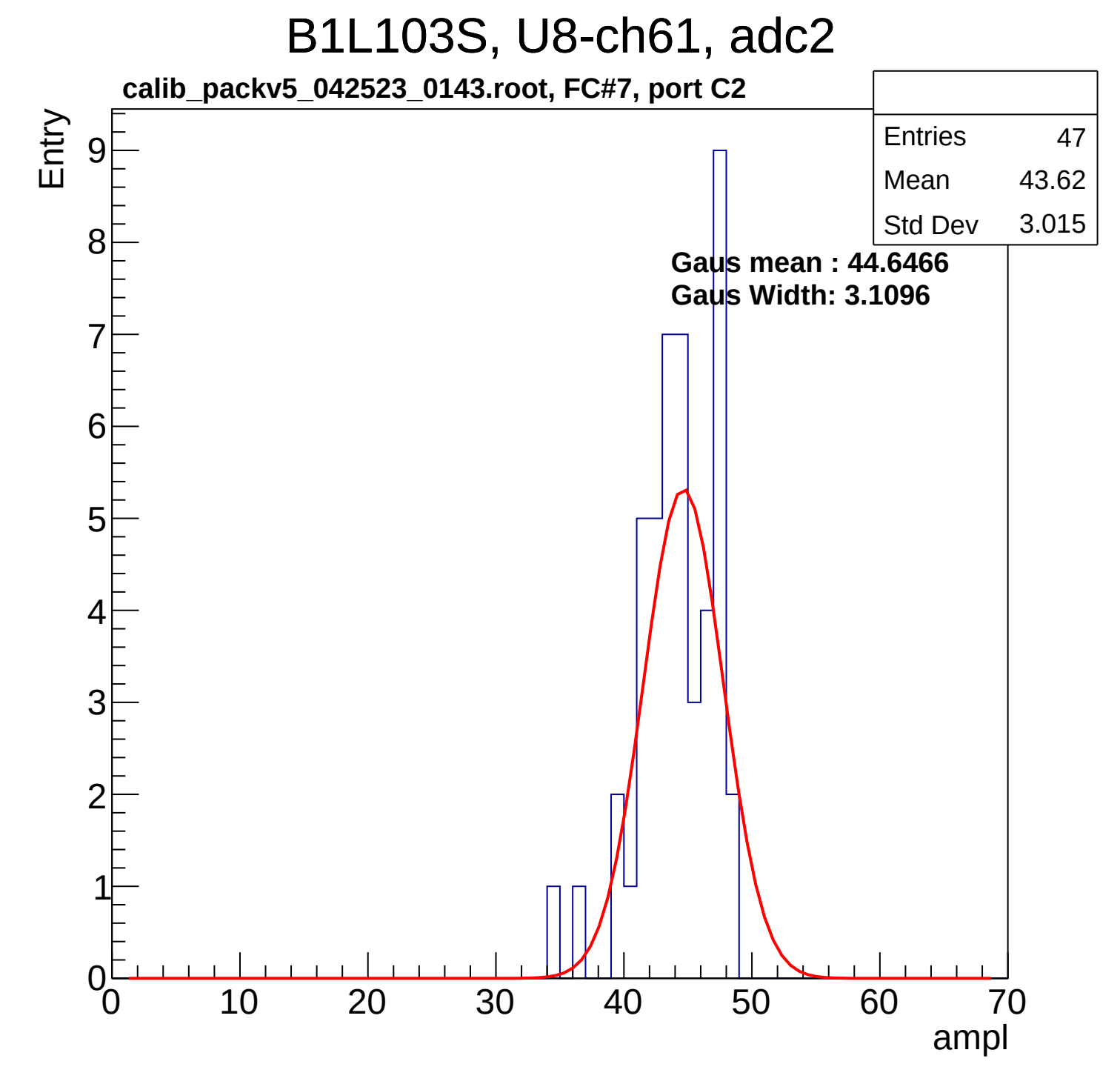

B1L103S, U8-ch60, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 58.92
Std Dev 2.55
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

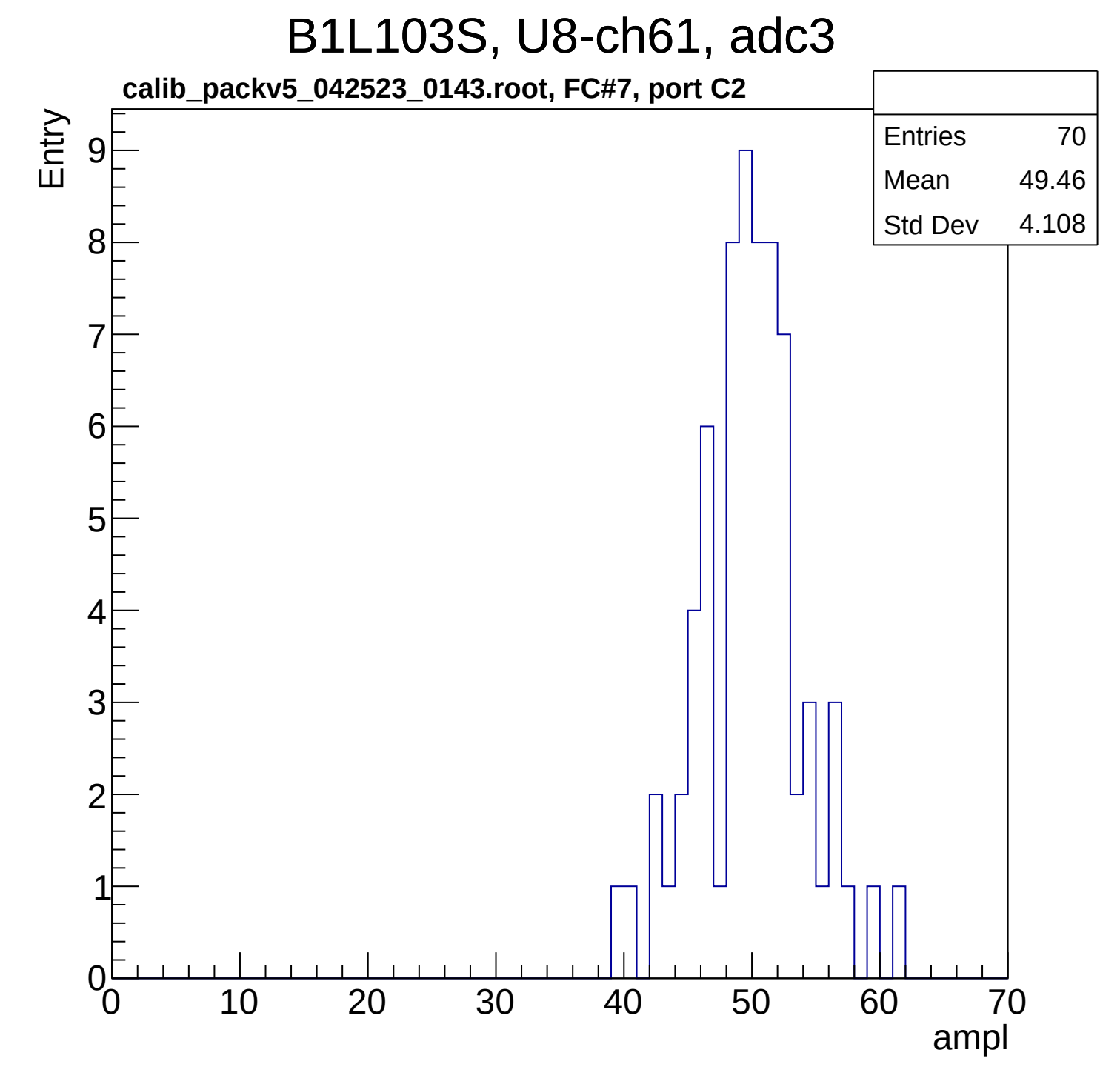

B1L103S, U8-ch60, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 24
Mean 57.96
Std Dev 12.36
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

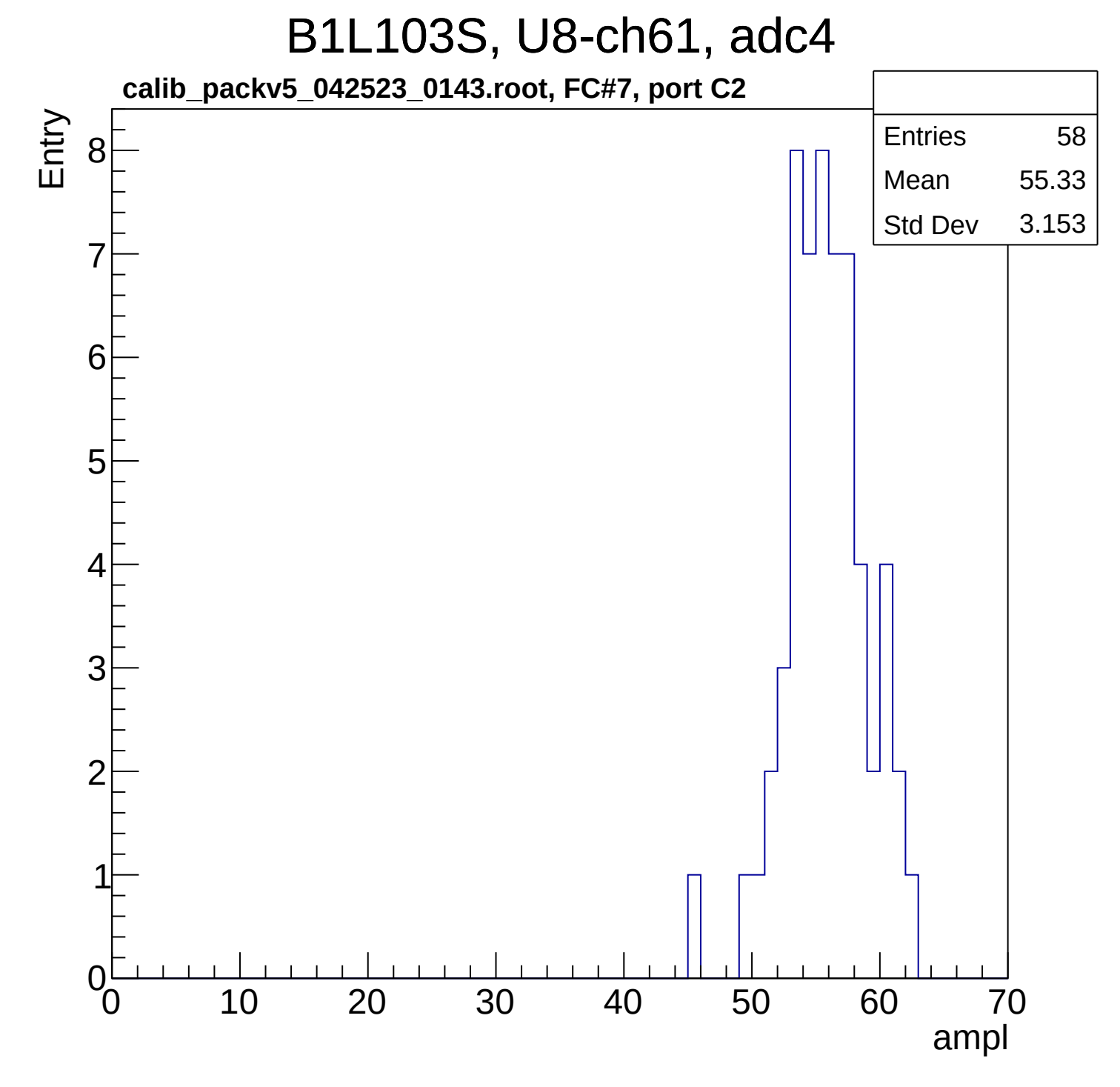

B1L103S, U8-ch60, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

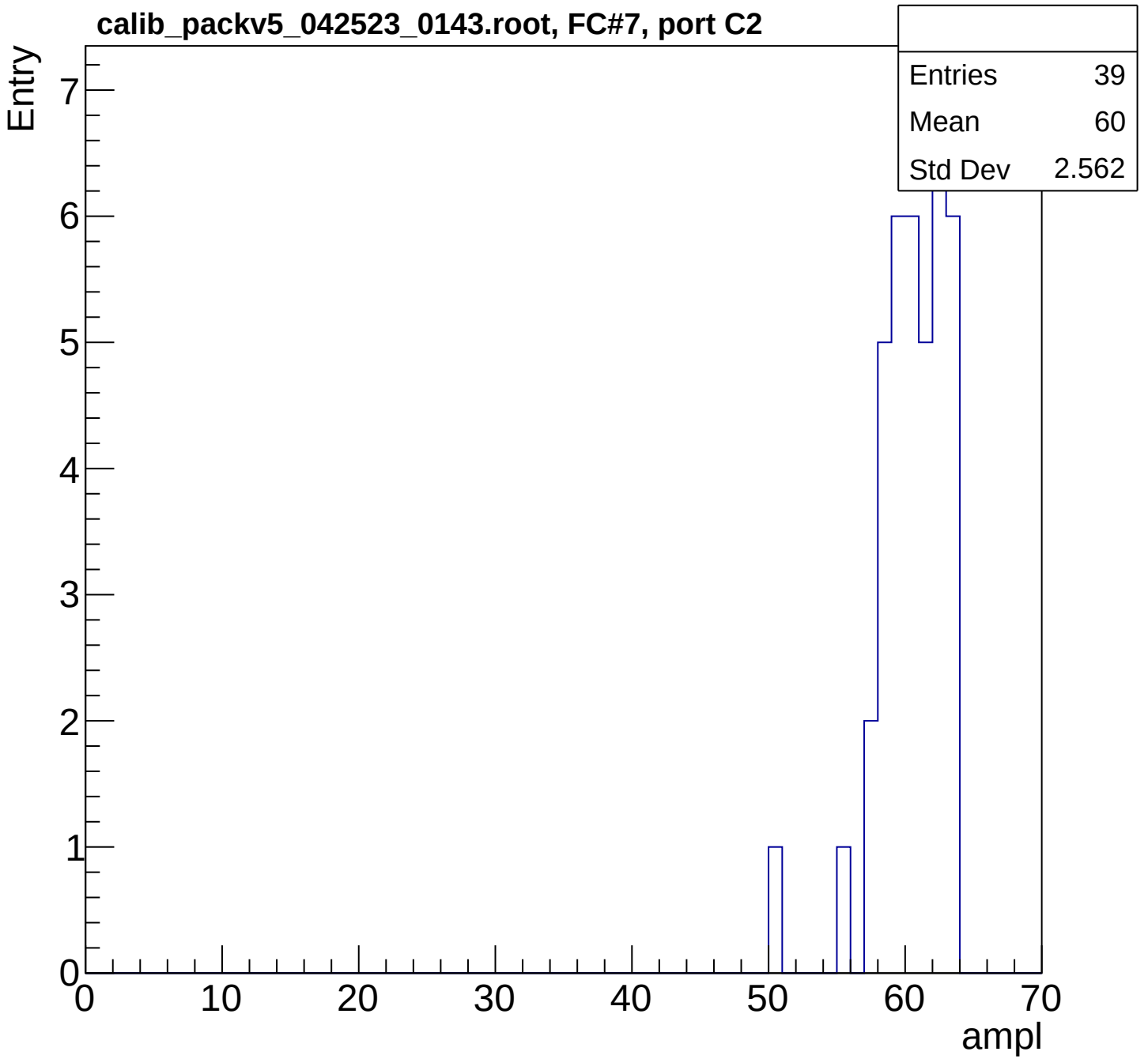

B1L103S, U8-ch61, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 29.18
Std Dev 4.635
Gaus mean : 30.3376
Gaus Width: 3.0314
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

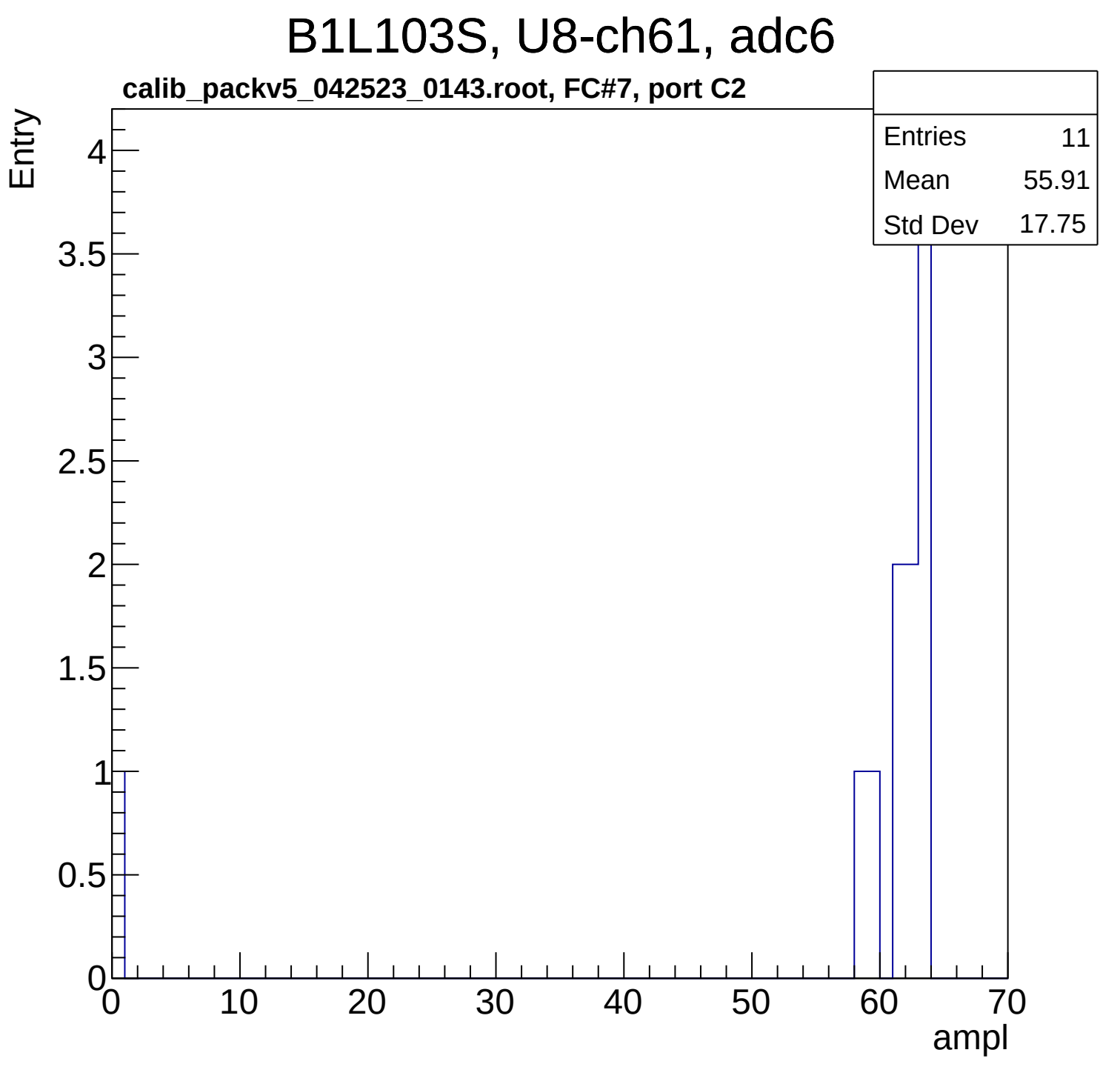

B1L103S, U8-ch61, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 37.49
Std Dev 3.161
Gaus mean : 37.8233
Gaus Width: 3.2986
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

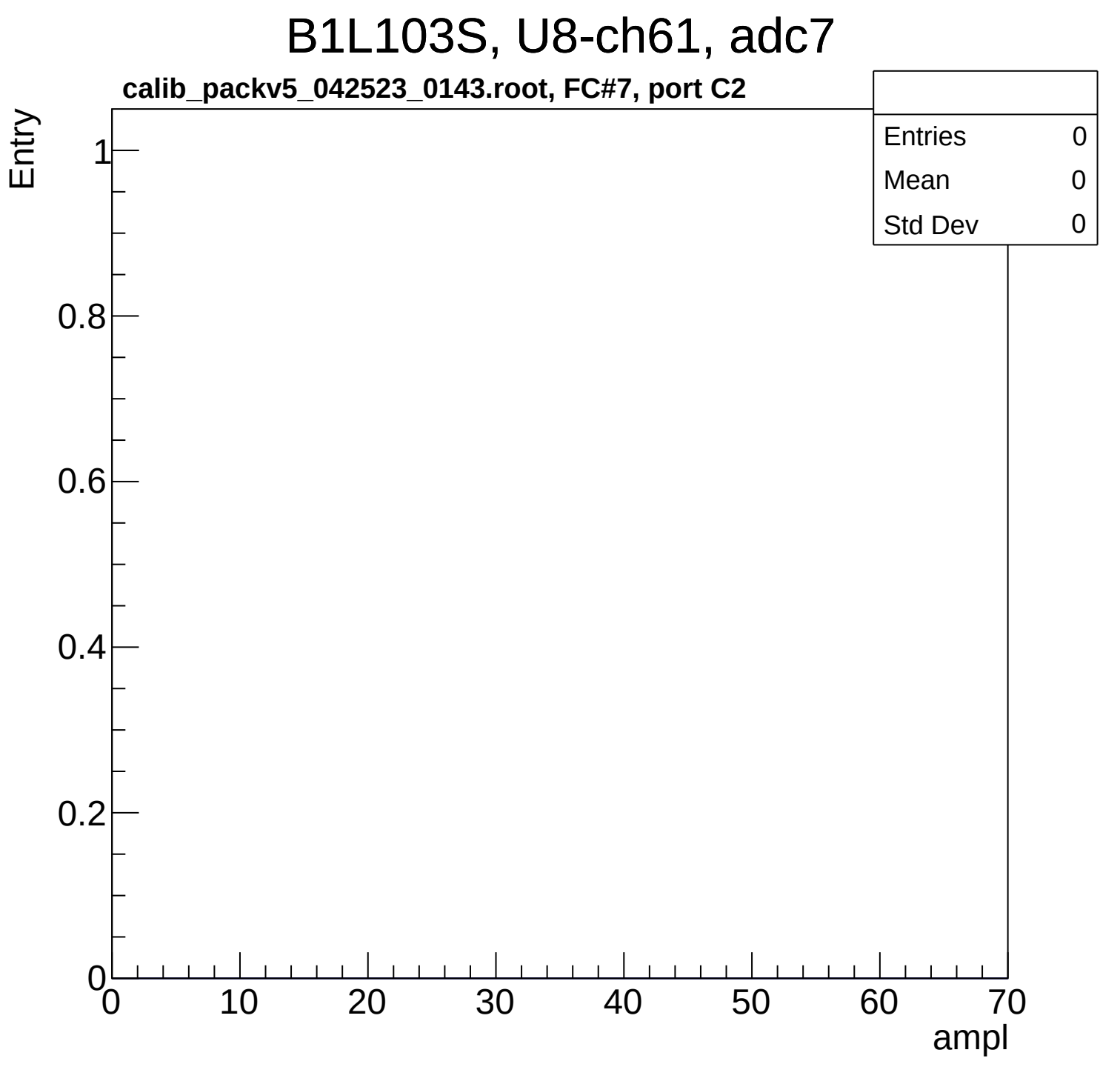

B1L103S, U8-ch61, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 43.62
Std Dev 3.015
Gaus mean : 44.6466
Gaus Width: 3.1096
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

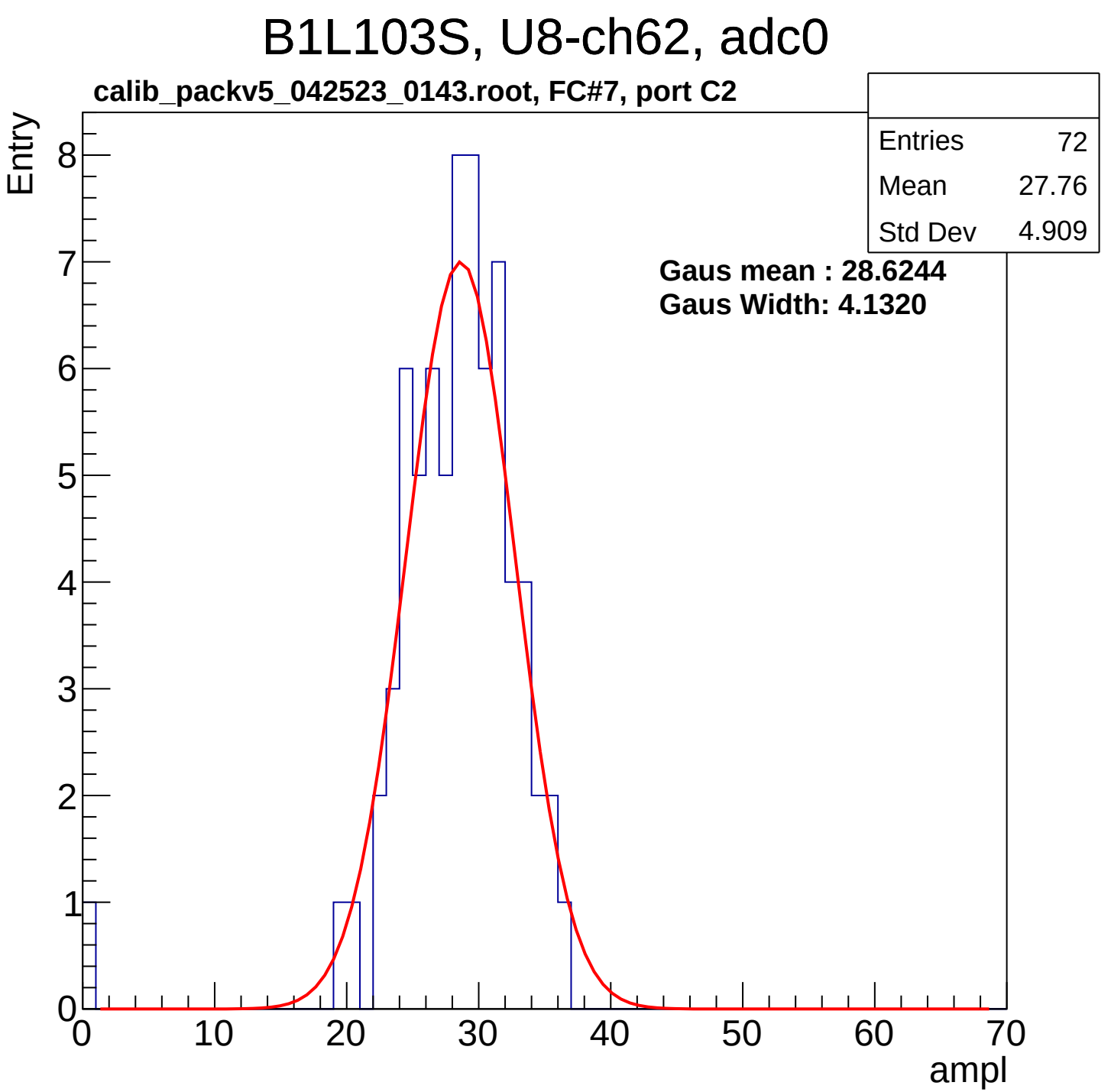

B1L103S, U8-ch61, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 49.46
Std Dev 4.108
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

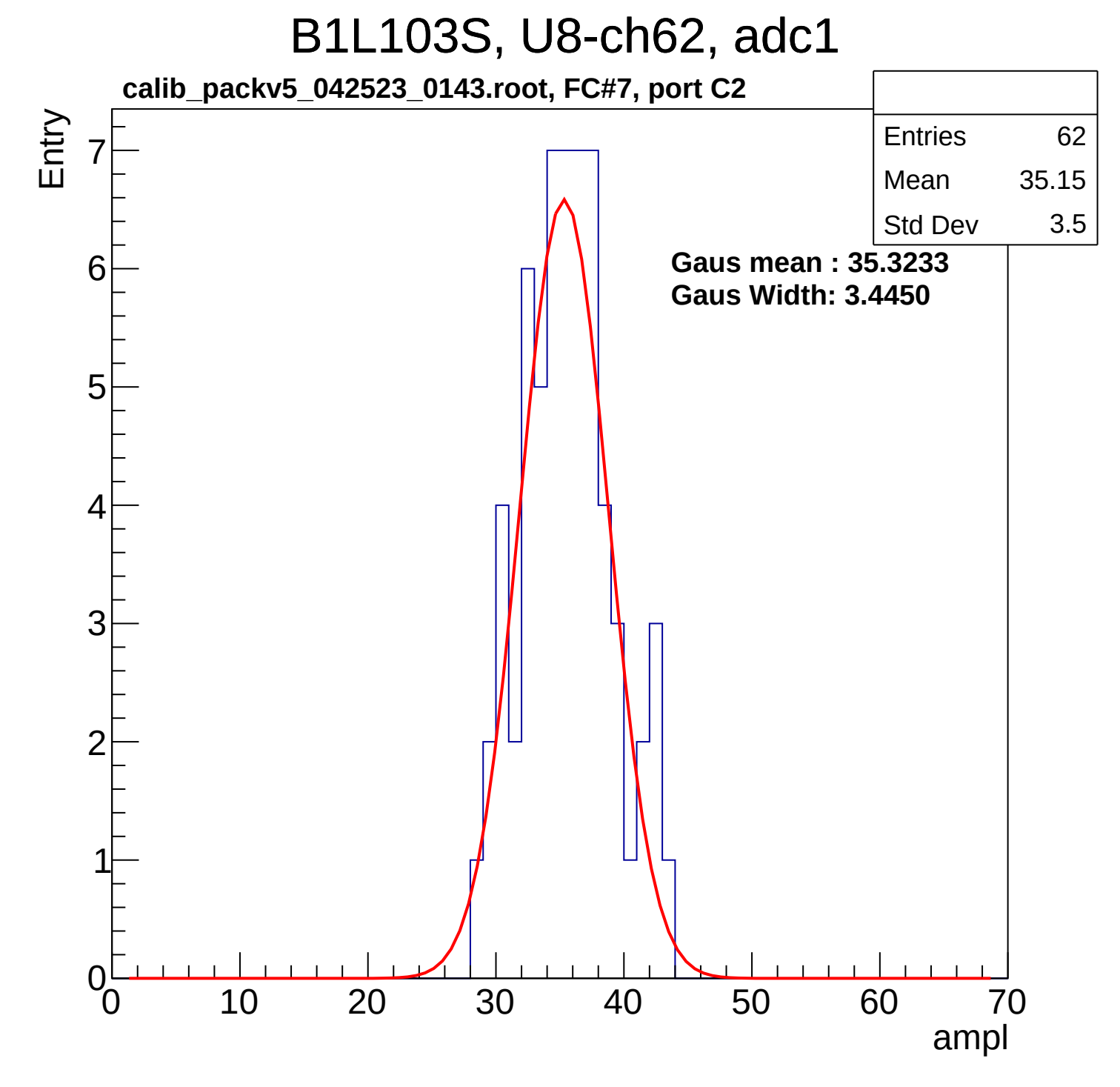

B1L103S, U8-ch61, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 55.33
Std Dev 3.153
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

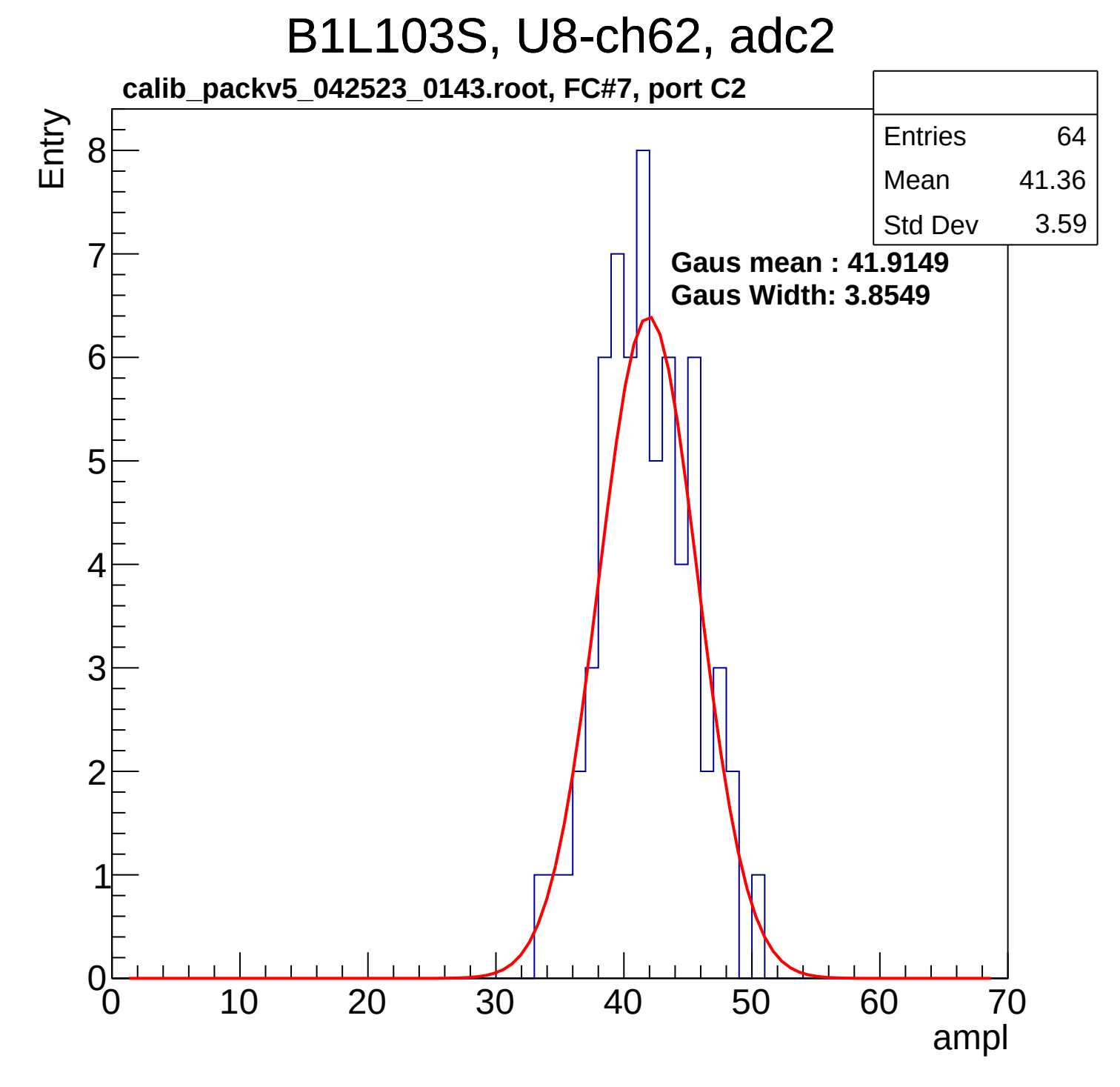

B1L103S, U8-ch61, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 39
Mean 60
Std Dev 2.562
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

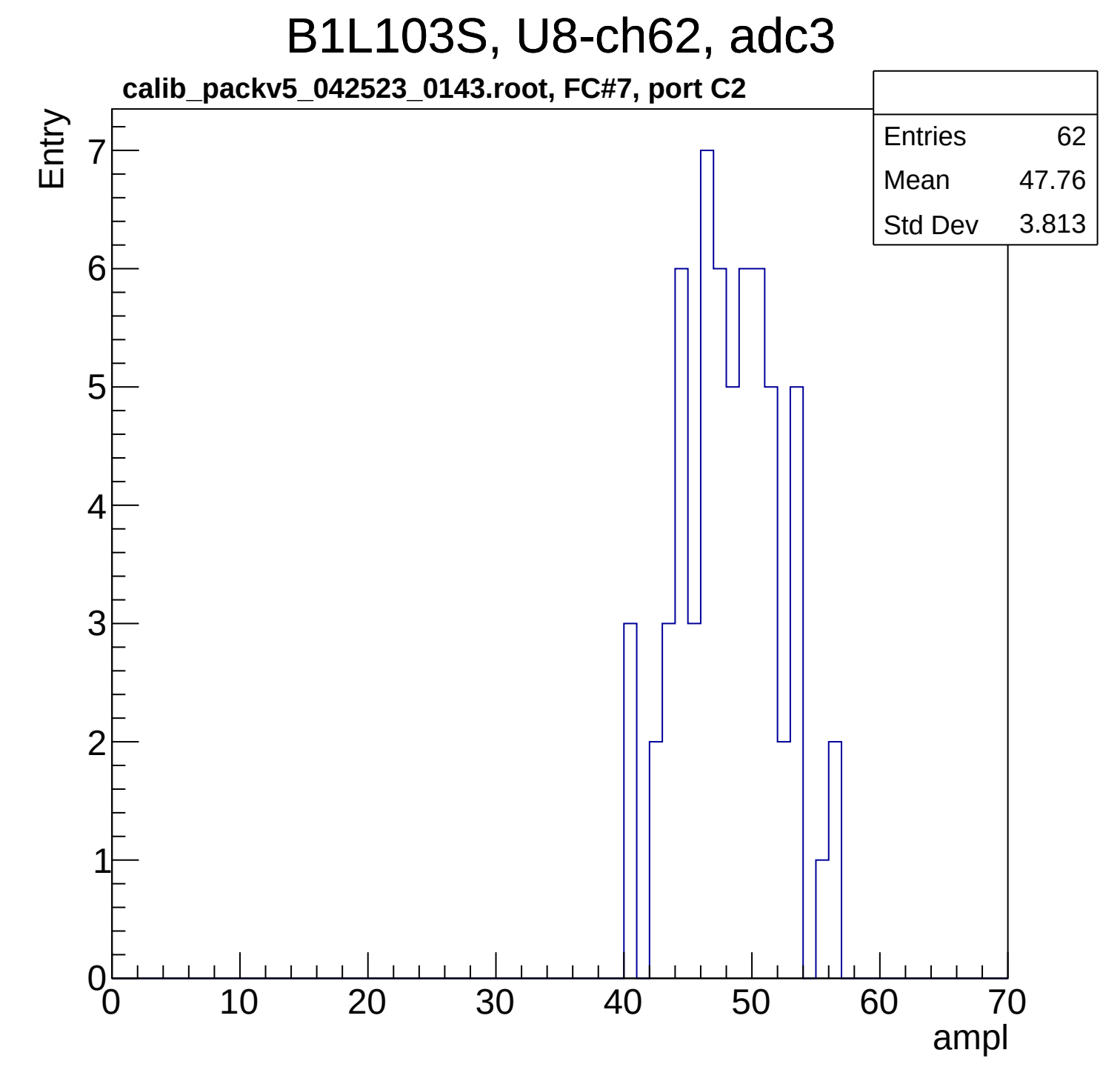

B1L103S, U8-ch61, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 11
Mean 55.91
Std Dev 17.75
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

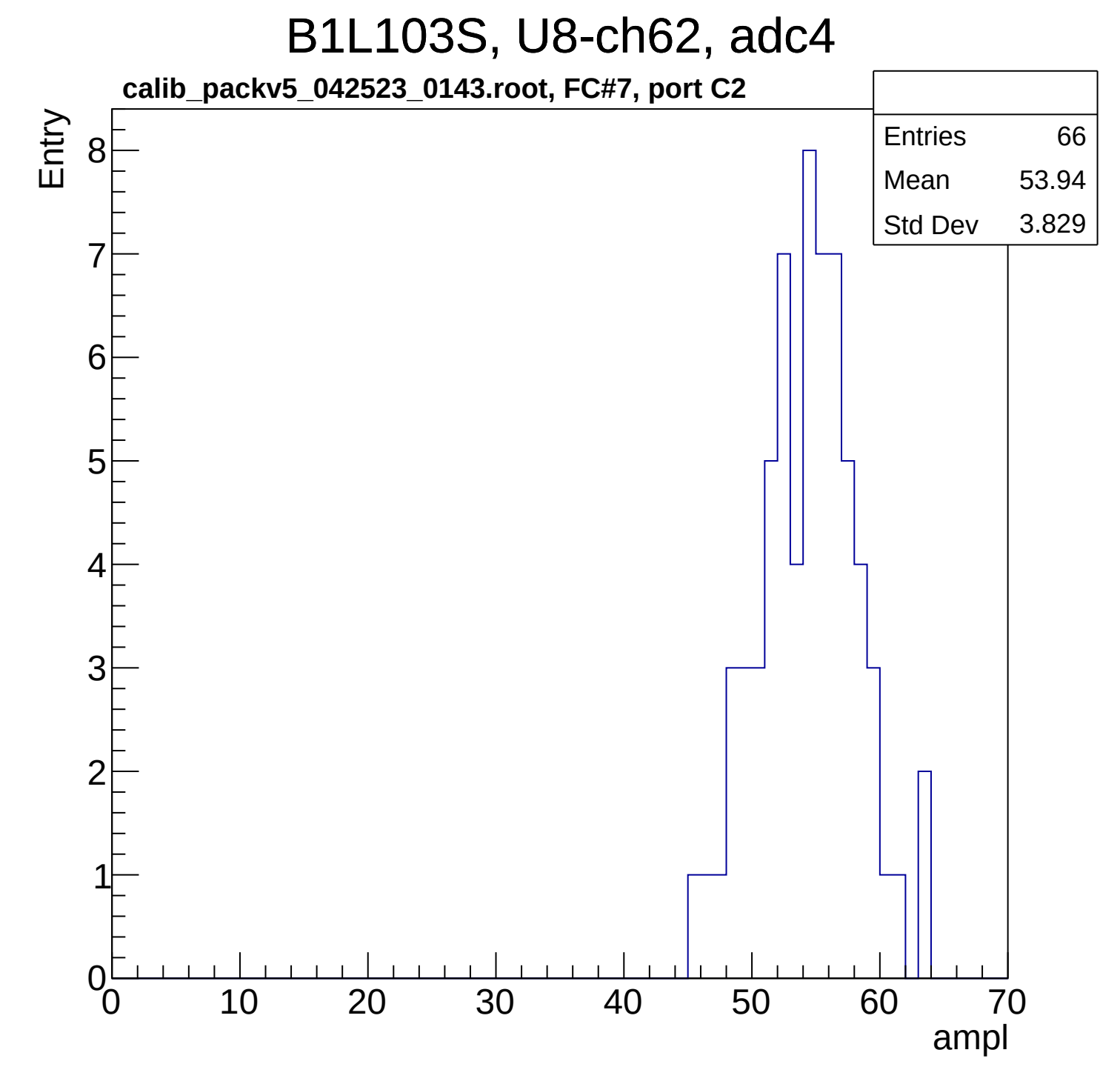

B1L103S, U8-ch61, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

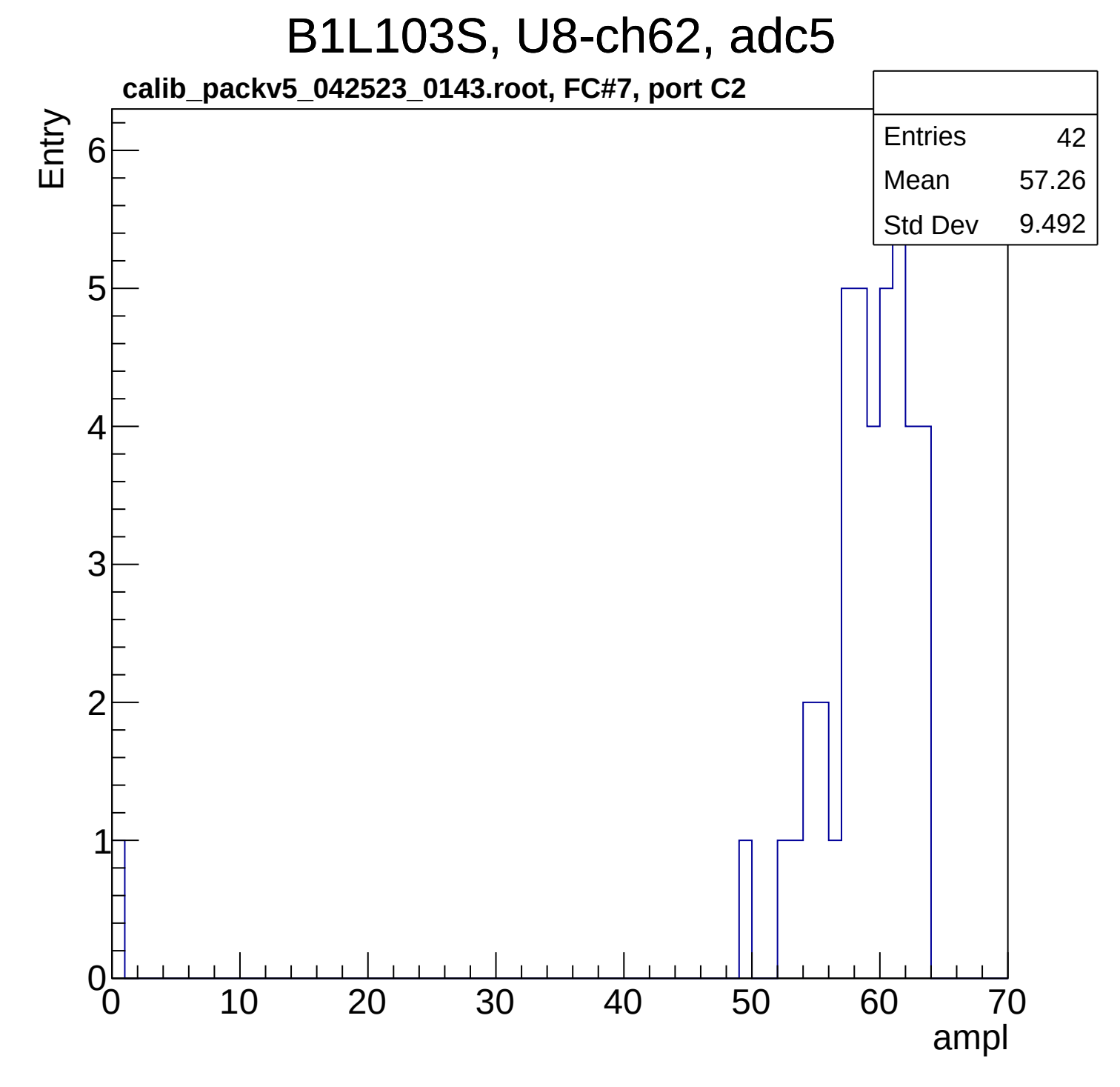

B1L103S, U8-ch62, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 27.76
Std Dev 4.909
Gaus mean : 28.6244
Gaus Width: 4.1320
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

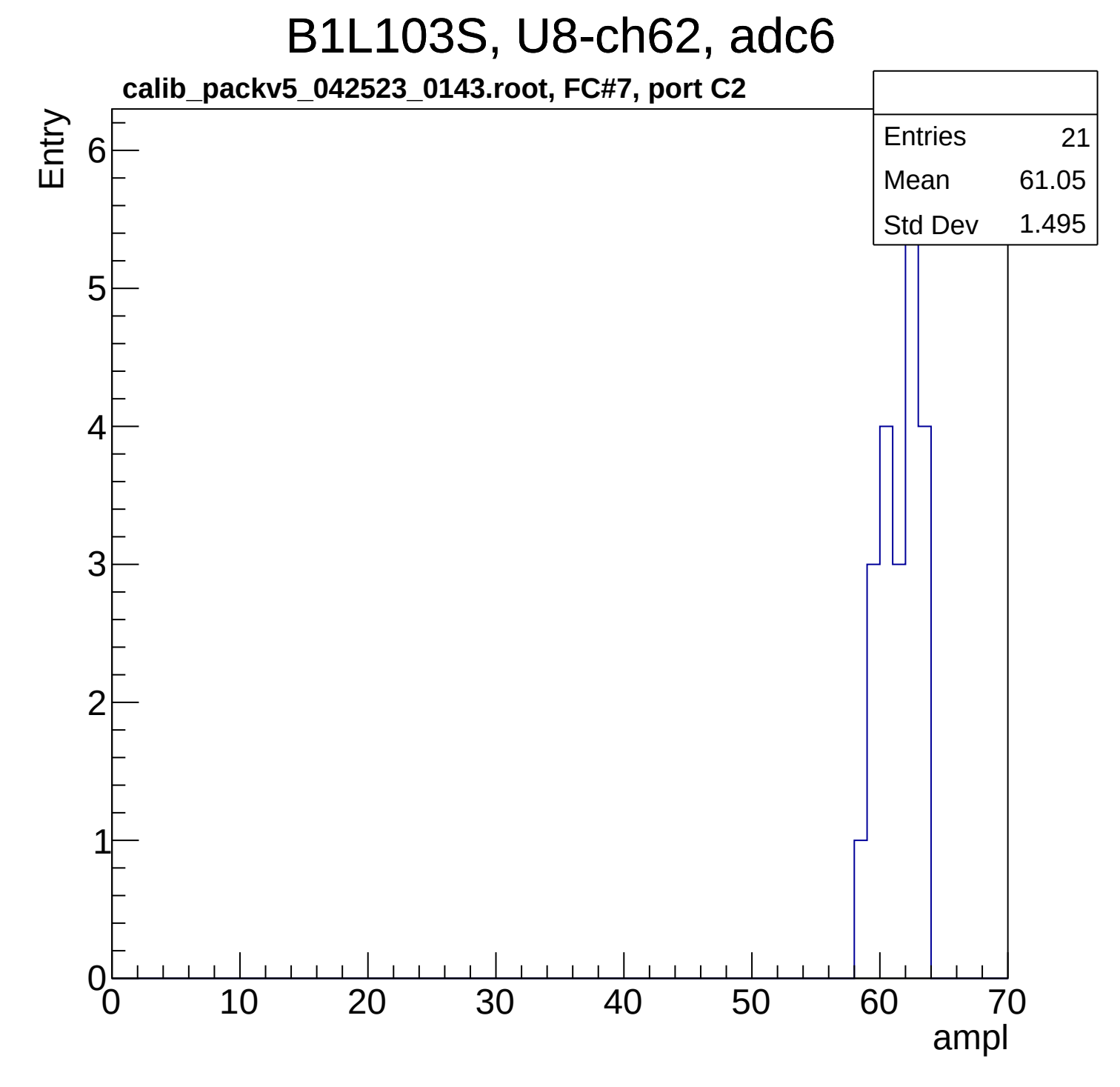

B1L103S, U8-ch62, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 35.15
Std Dev 3.5
Gaus mean : 35.3233
Gaus Width: 3.4450
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

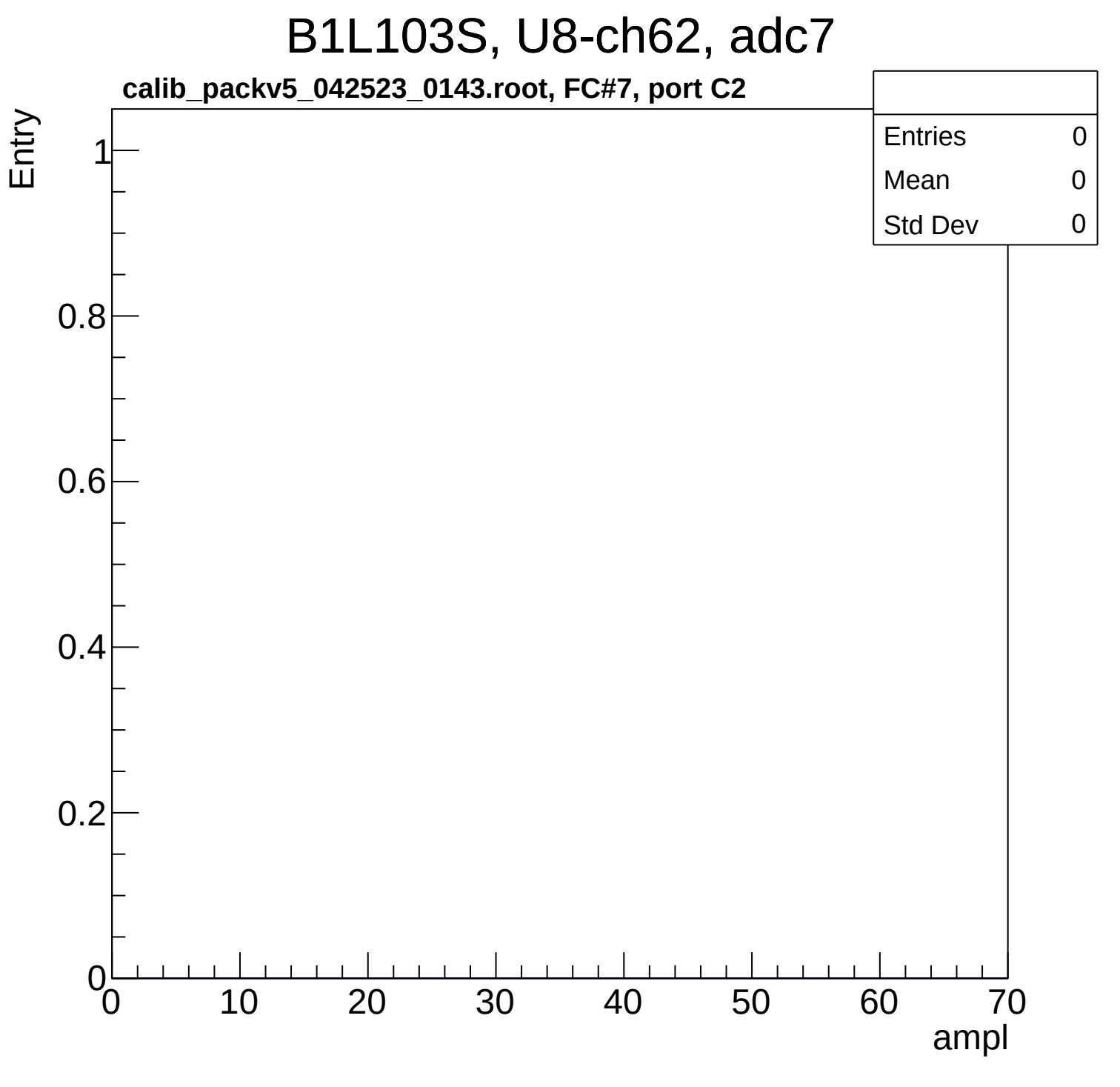

B1L103S, U8-ch62, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 41.36
Std Dev 3.59
Gaus mean : 41.9149
Gaus Width: 3.8549
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

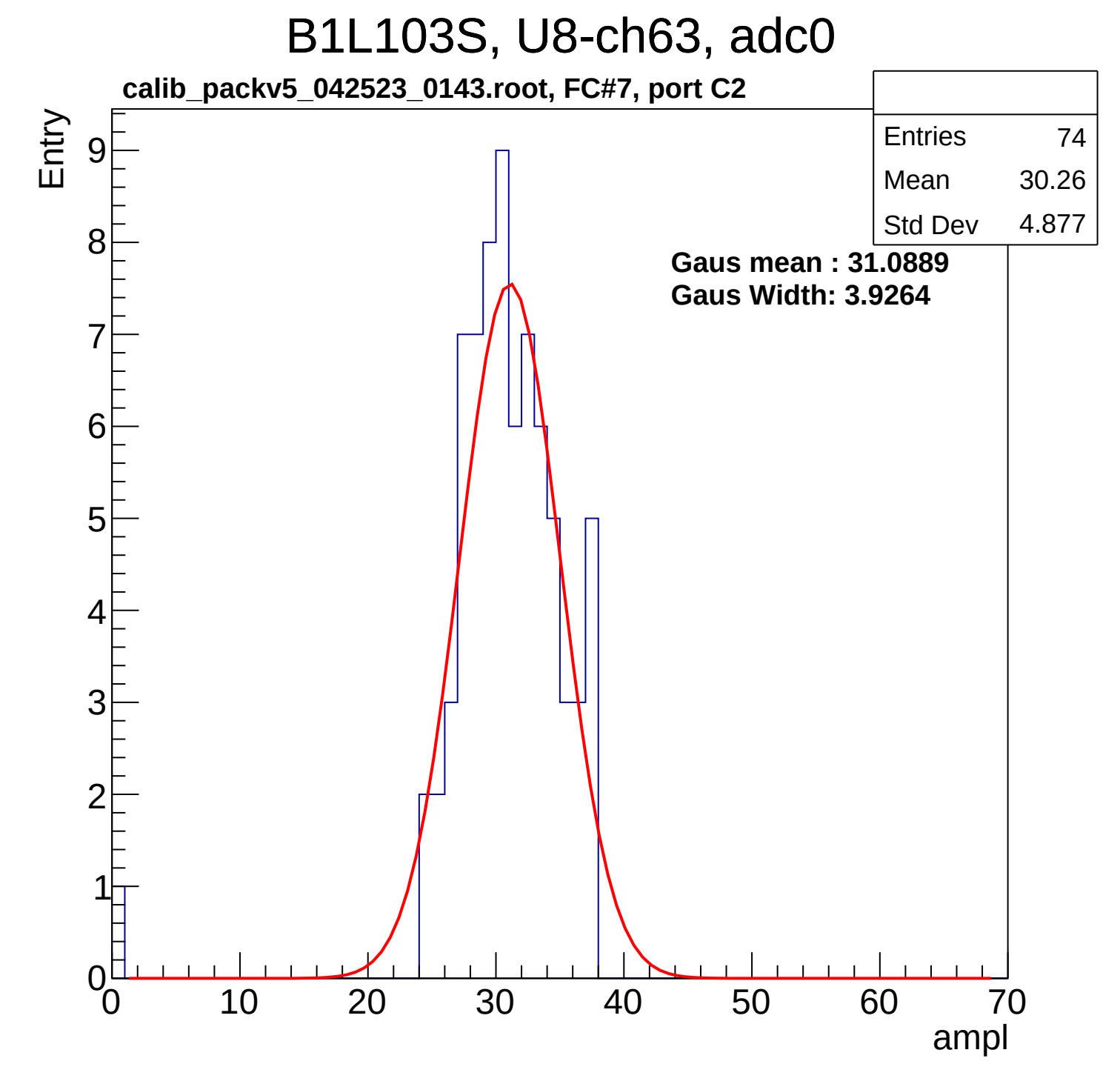

B1L103S, U8-ch62, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 47.76
Std Dev 3.813
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

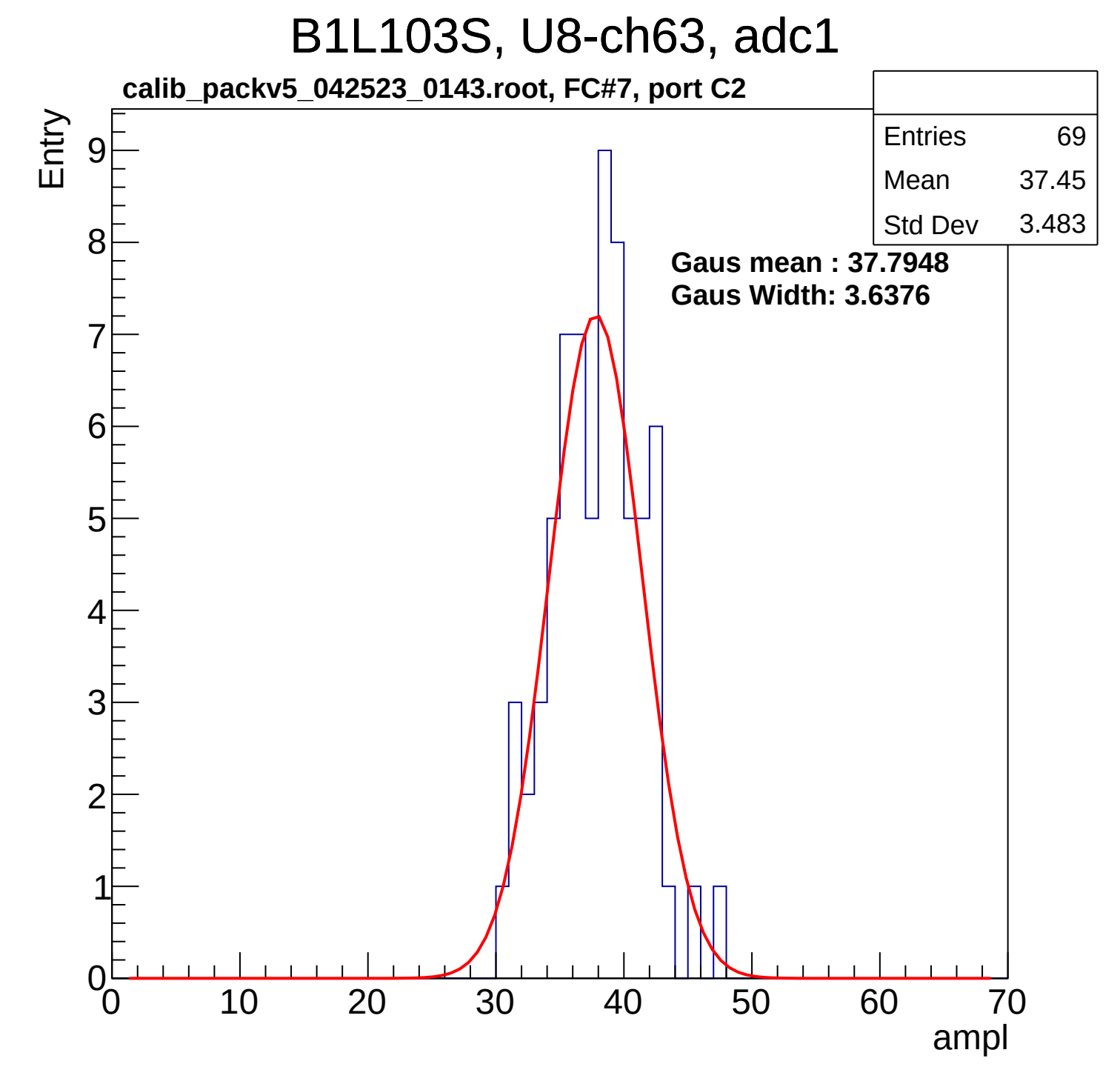

B1L103S, U8-ch62, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 53.94
Std Dev 3.829
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

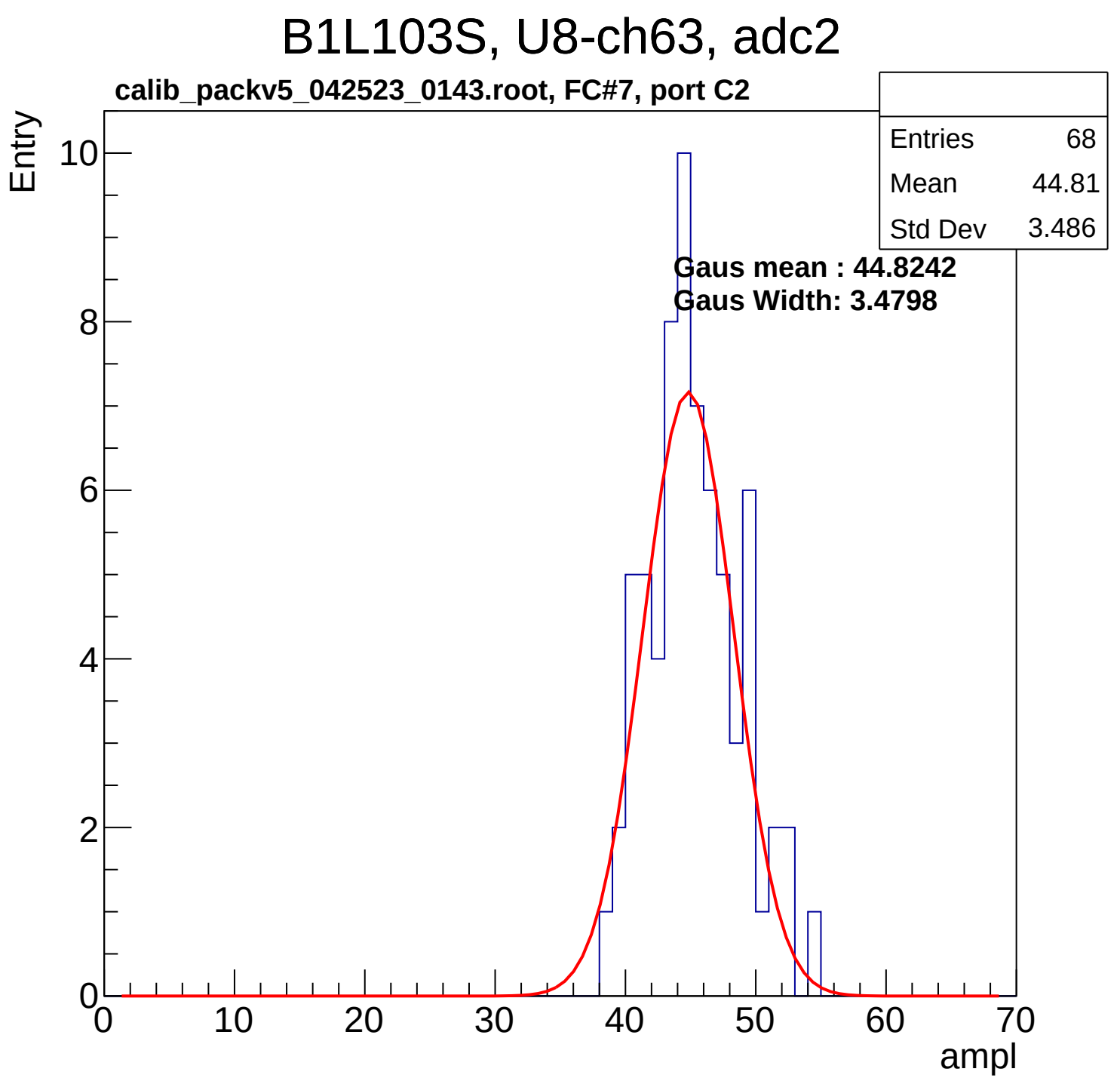

B1L103S, U8-ch62, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 42
Mean 57.26
Std Dev 9.492
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

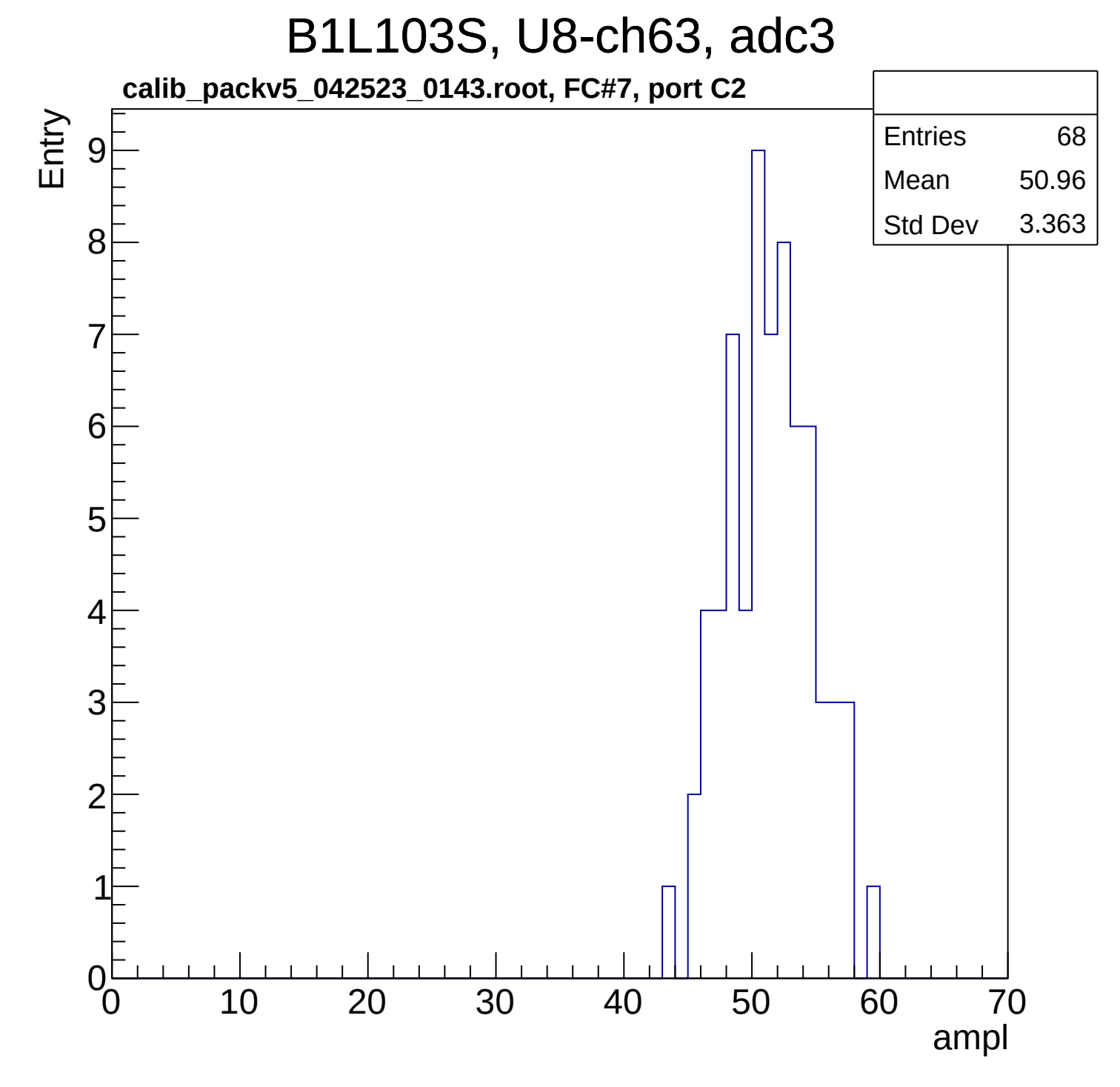

B1L103S, U8-ch62, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 21
Mean 61.05
Std Dev 1.495
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

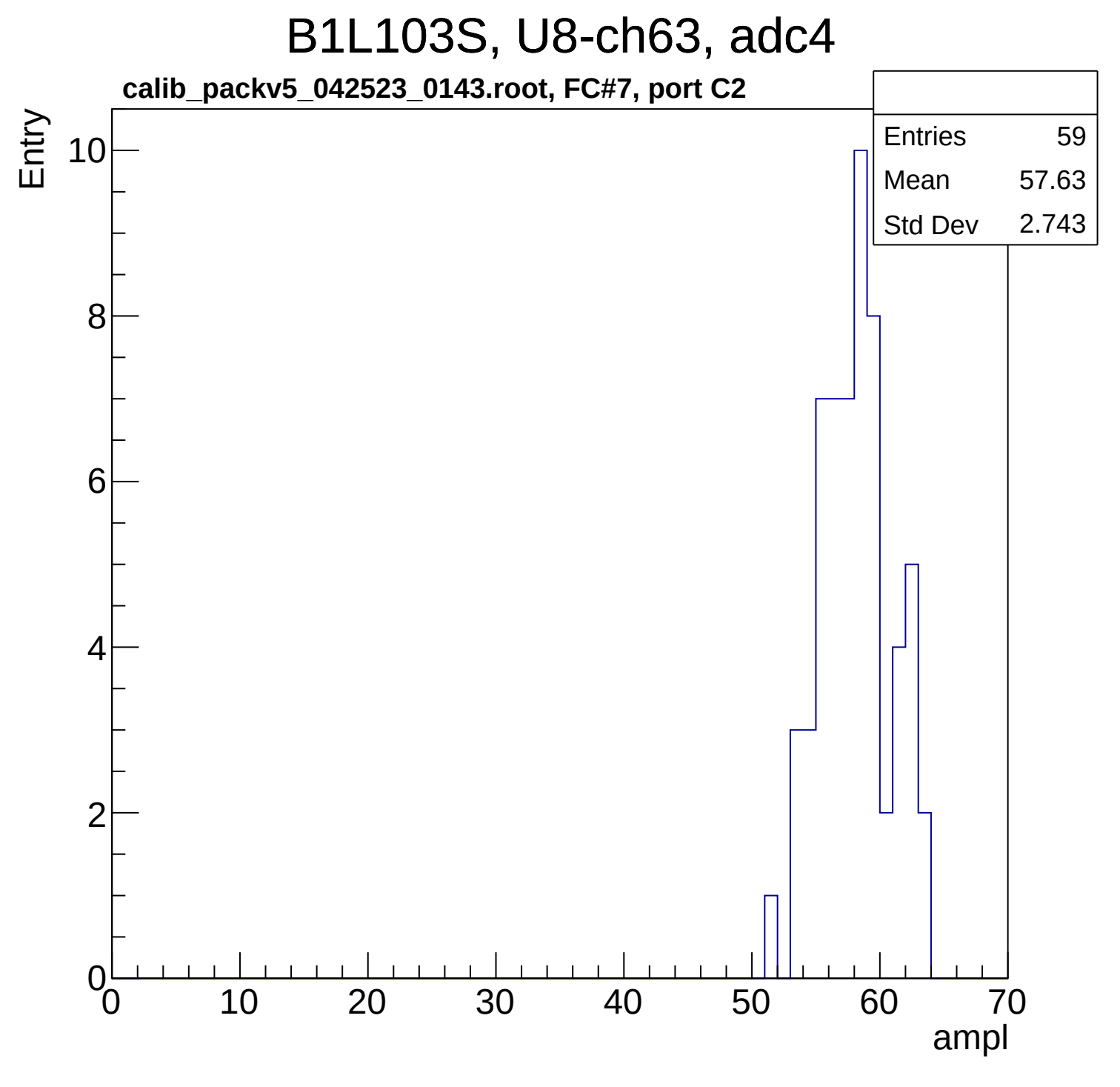

B1L103S, U8-ch62, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

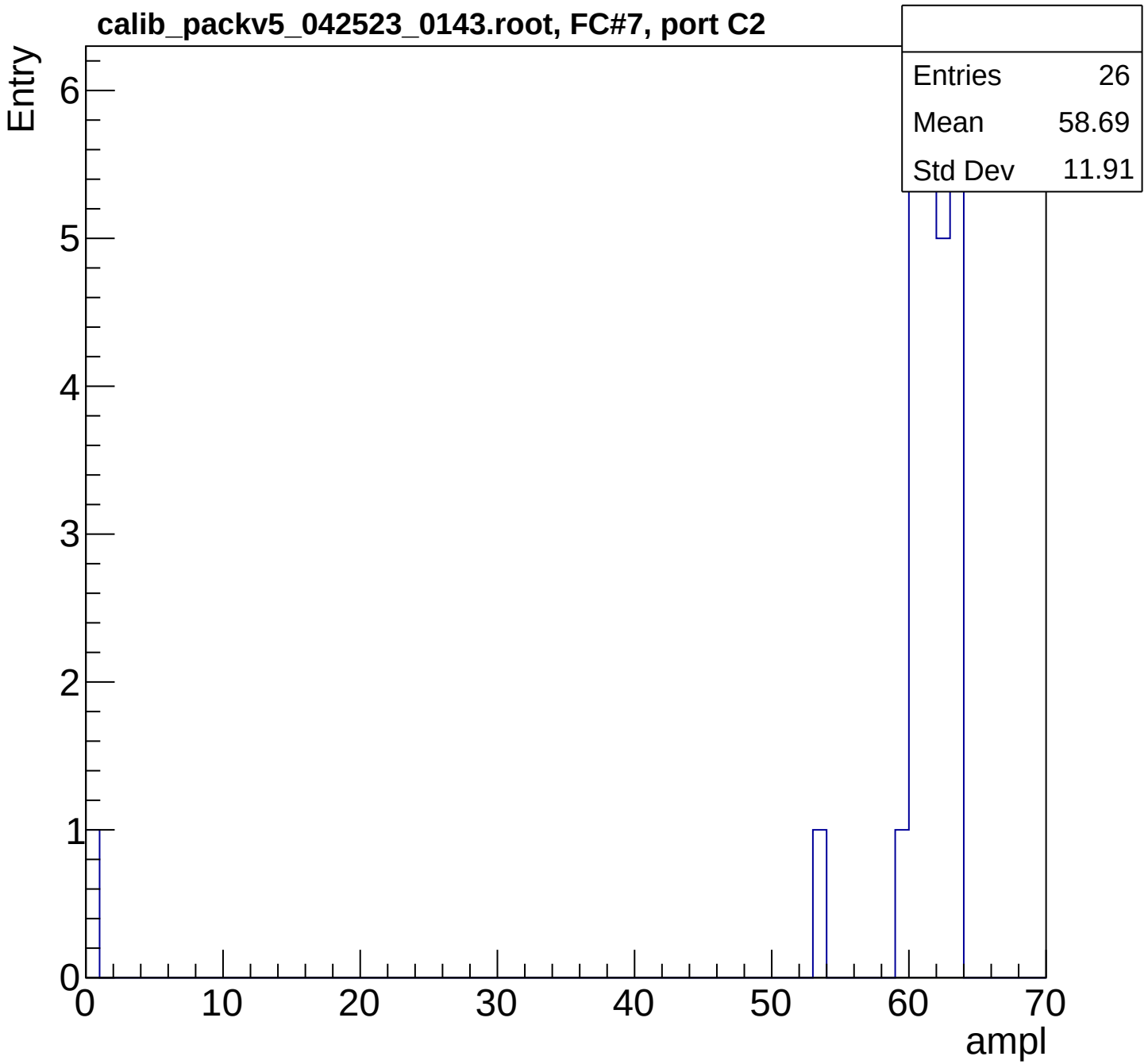

B1L103S, U8-ch63, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 30.26
Std Dev 4.877
Gaus mean : 31.0889
Gaus Width: 3.9264
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

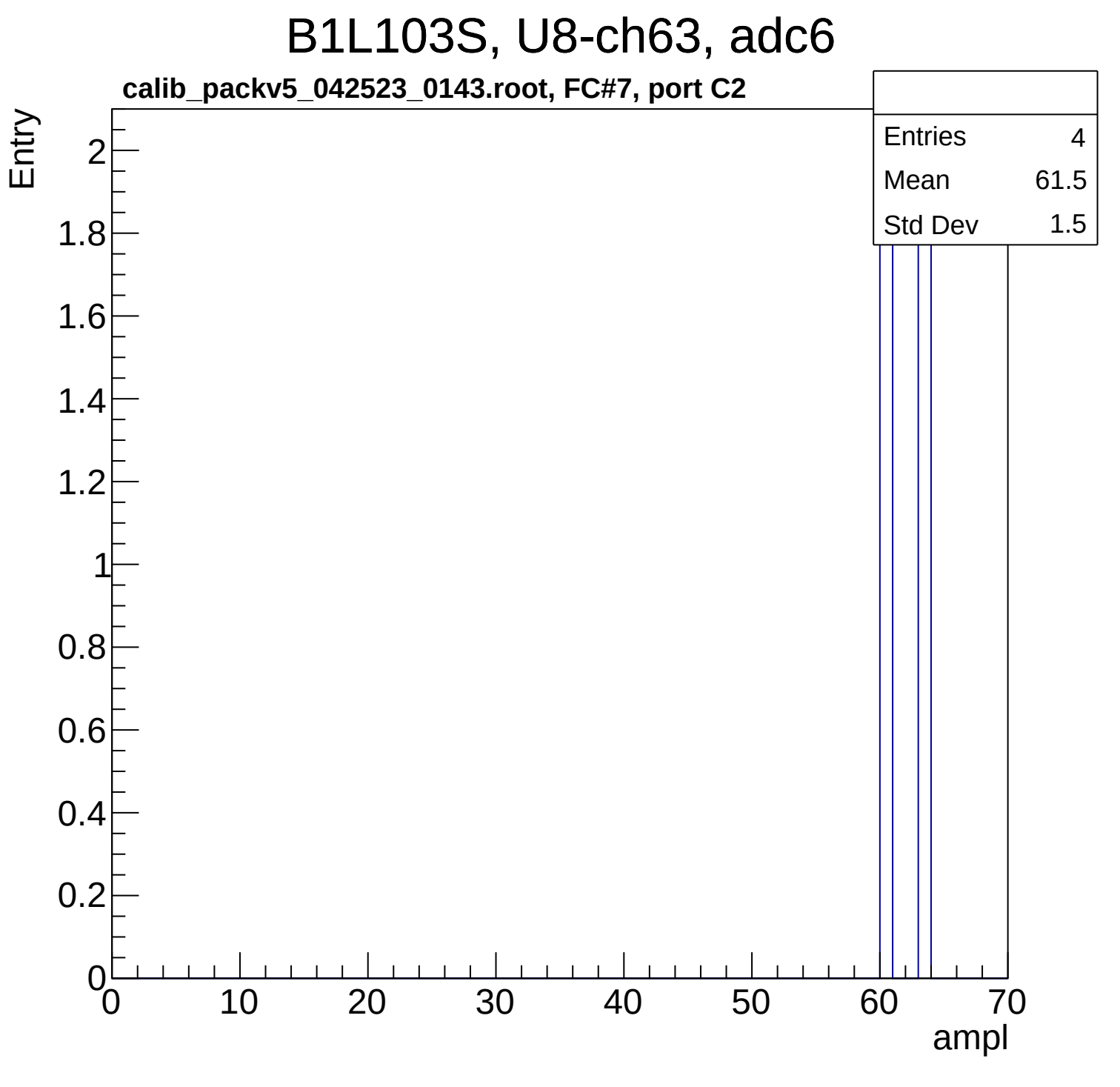

B1L103S, U8-ch63, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 37.45
Std Dev 3.483
Gaus mean : 37.7948
Gaus Width: 3.6376
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

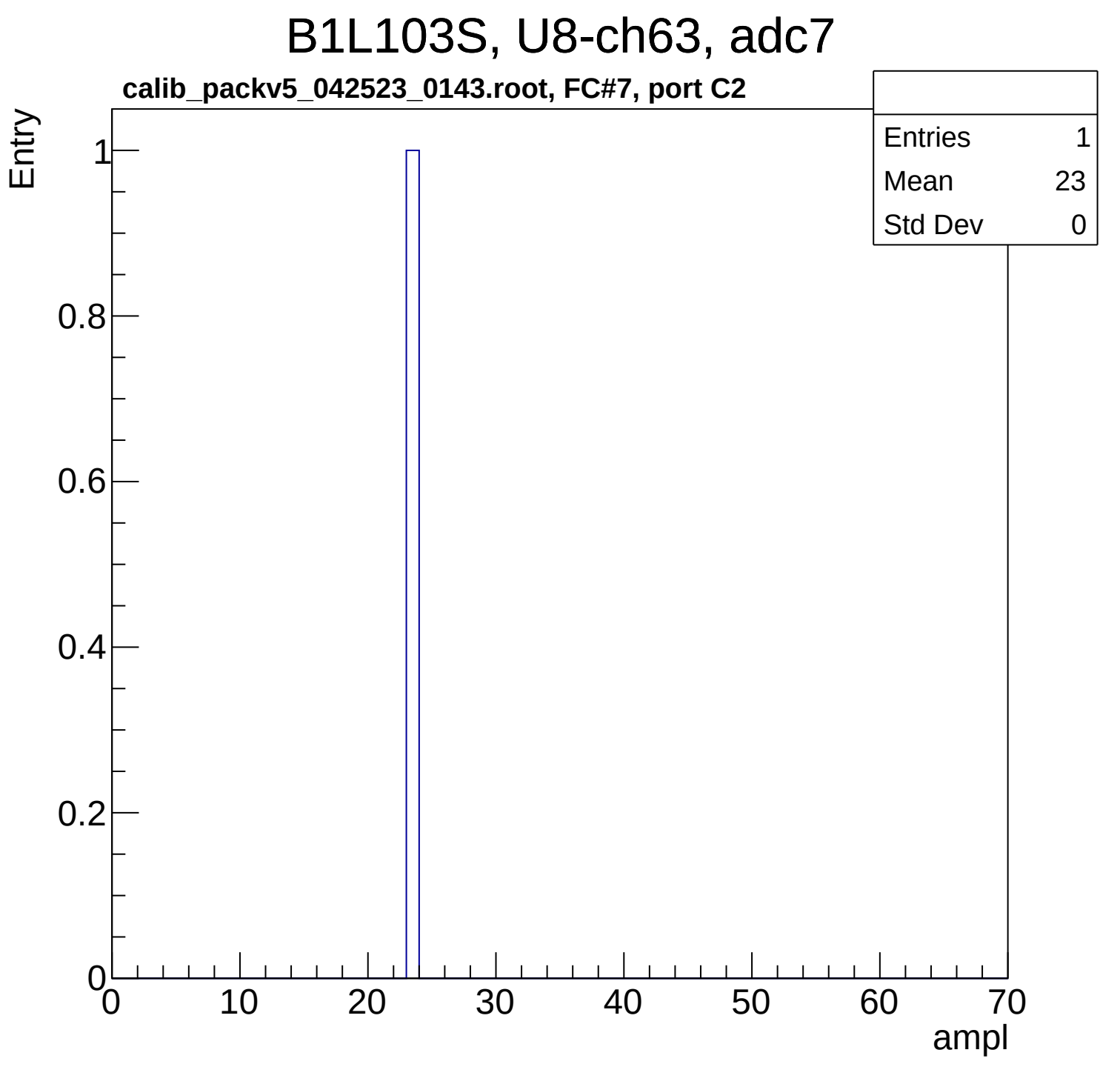

B1L103S, U8-ch63, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 44.81
Std Dev 3.486
Gaus mean : 44.8242
Gaus Width: 3.4798
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

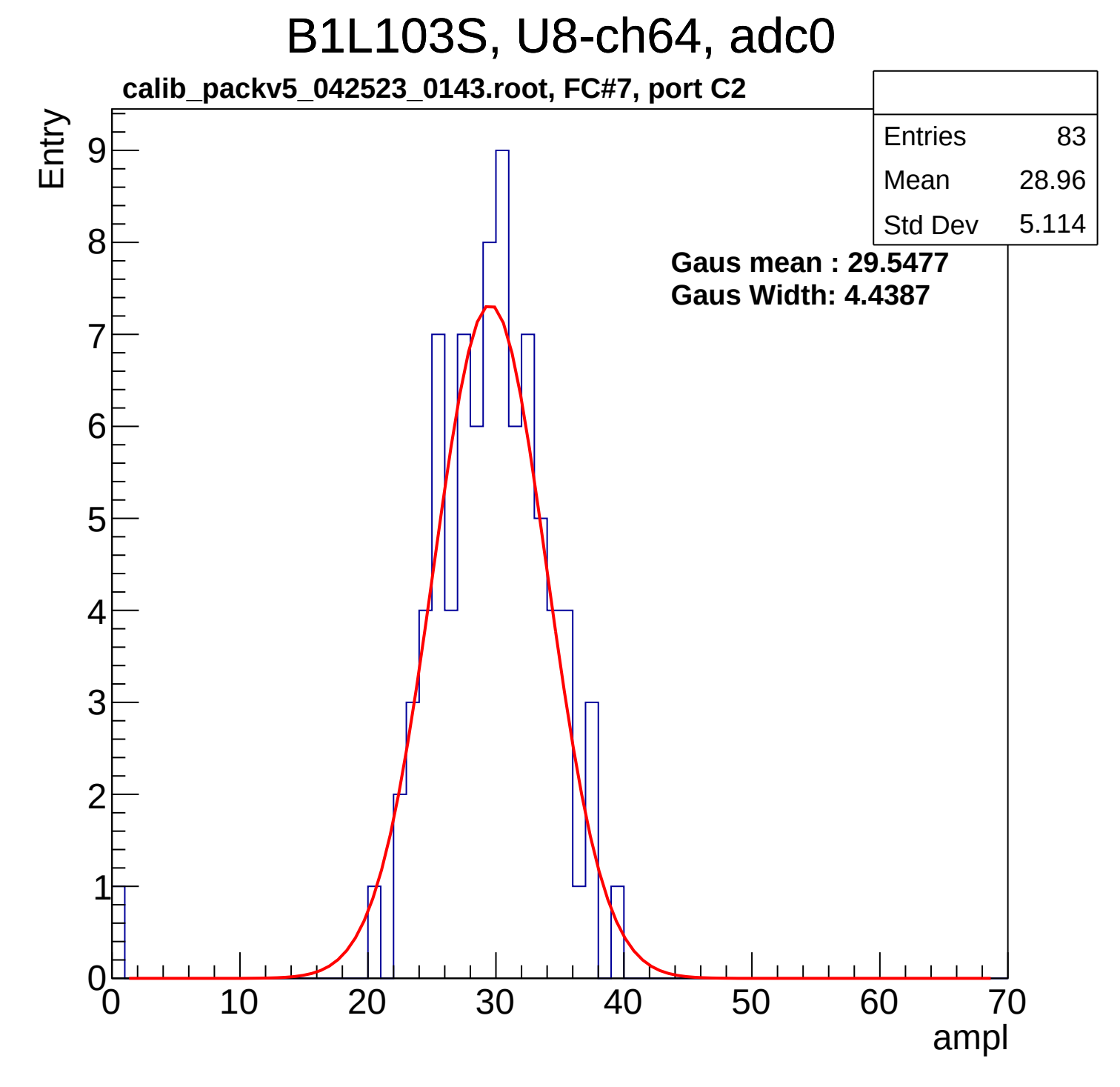

B1L103S, U8-ch63, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 50.96
Std Dev 3.363
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

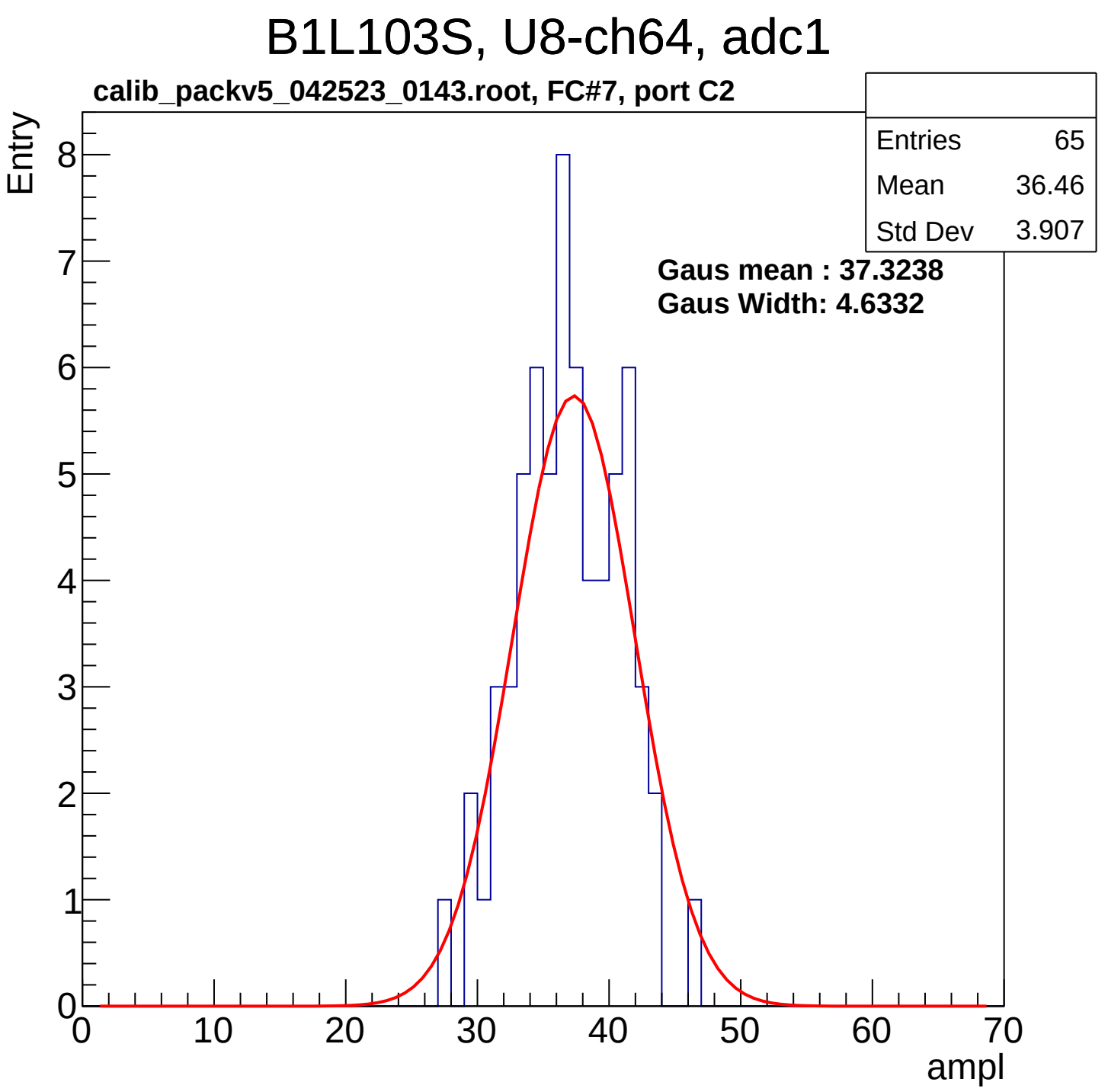

B1L103S, U8-ch63, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 57.63
Std Dev 2.743
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

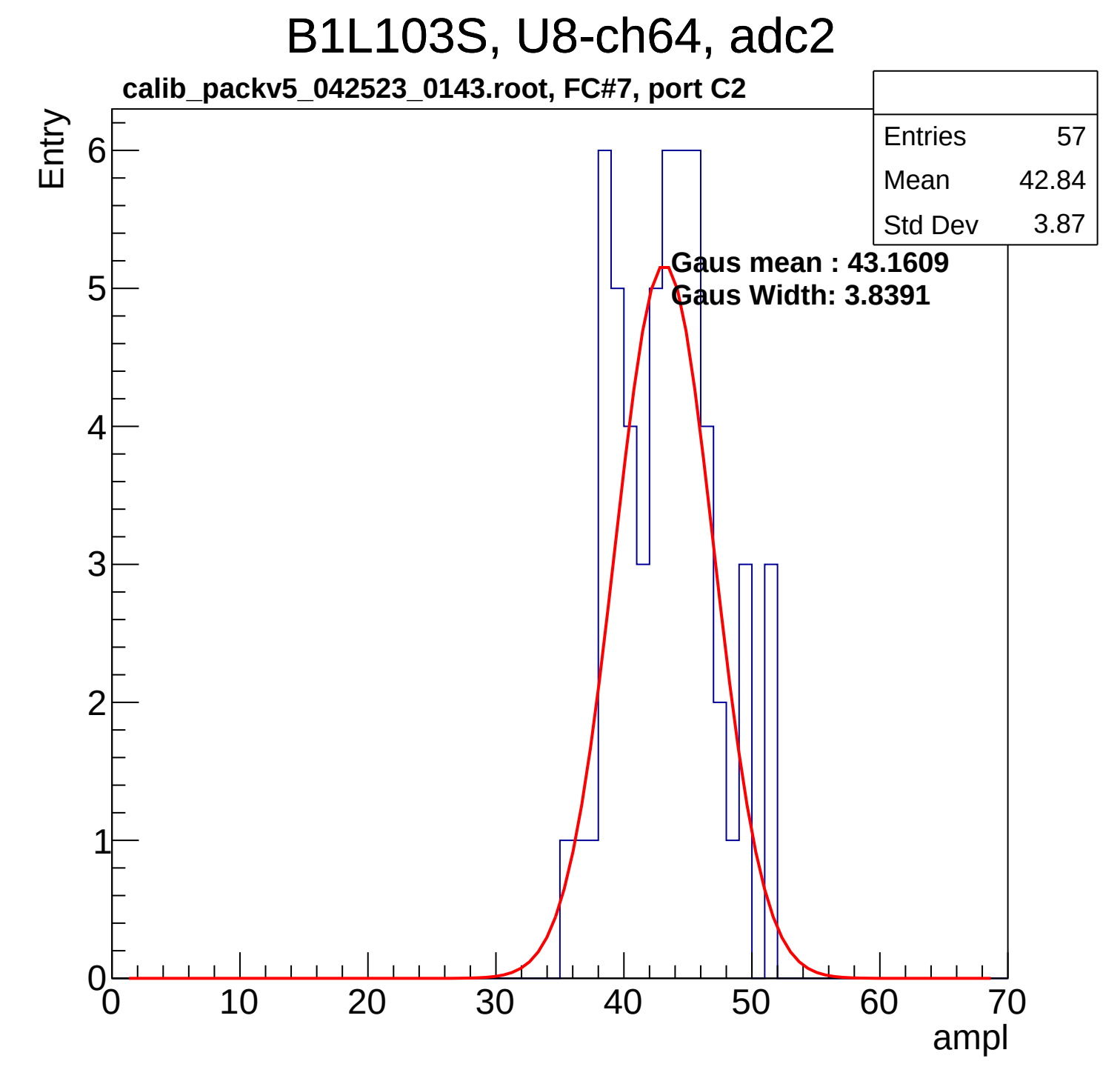

B1L103S, U8-ch63, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 26
Mean 58.69
Std Dev 11.91
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

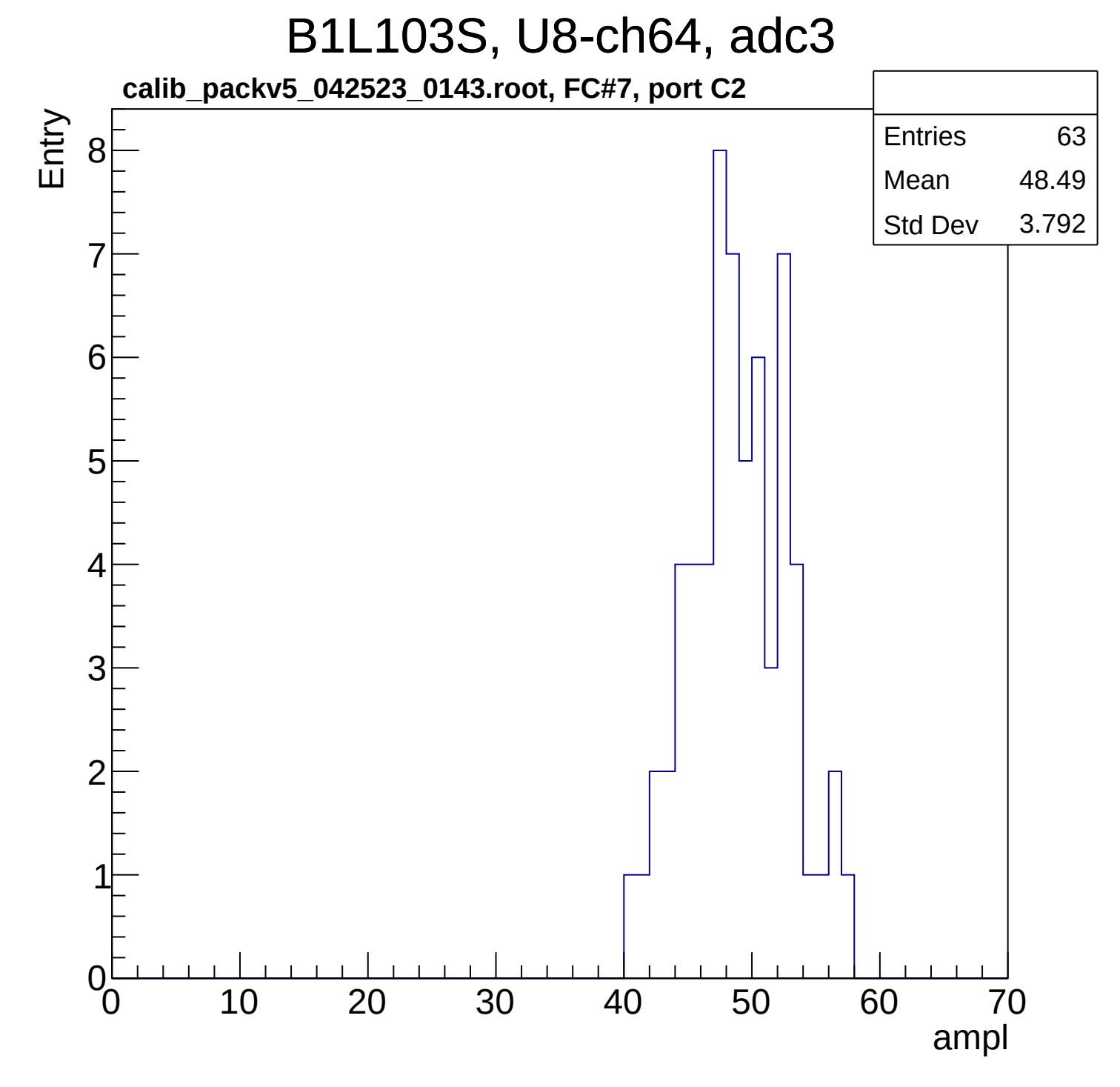

B1L103S, U8-ch63, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 61.5
Std Dev 1.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

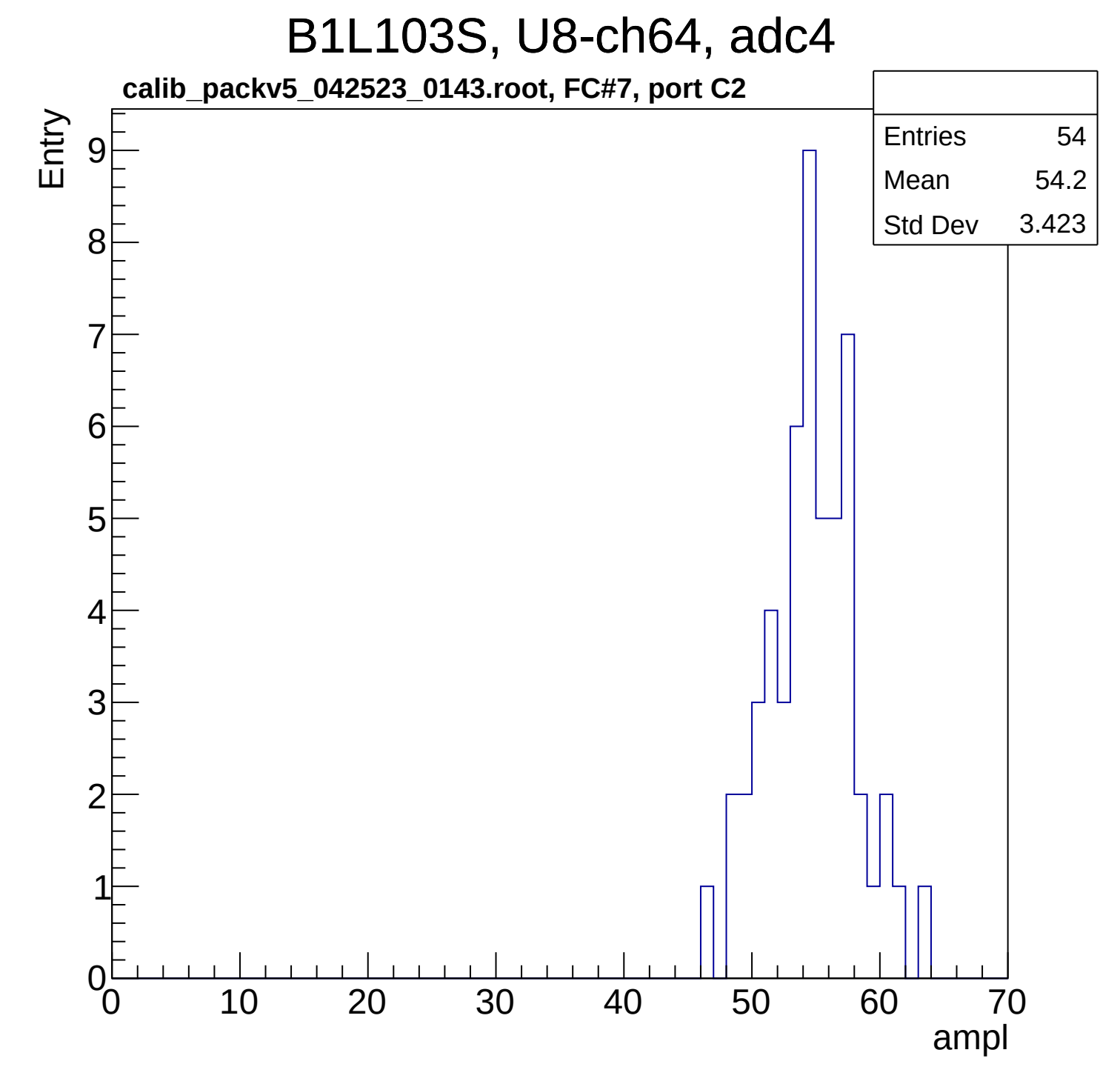

B1L103S, U8-ch63, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 23
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

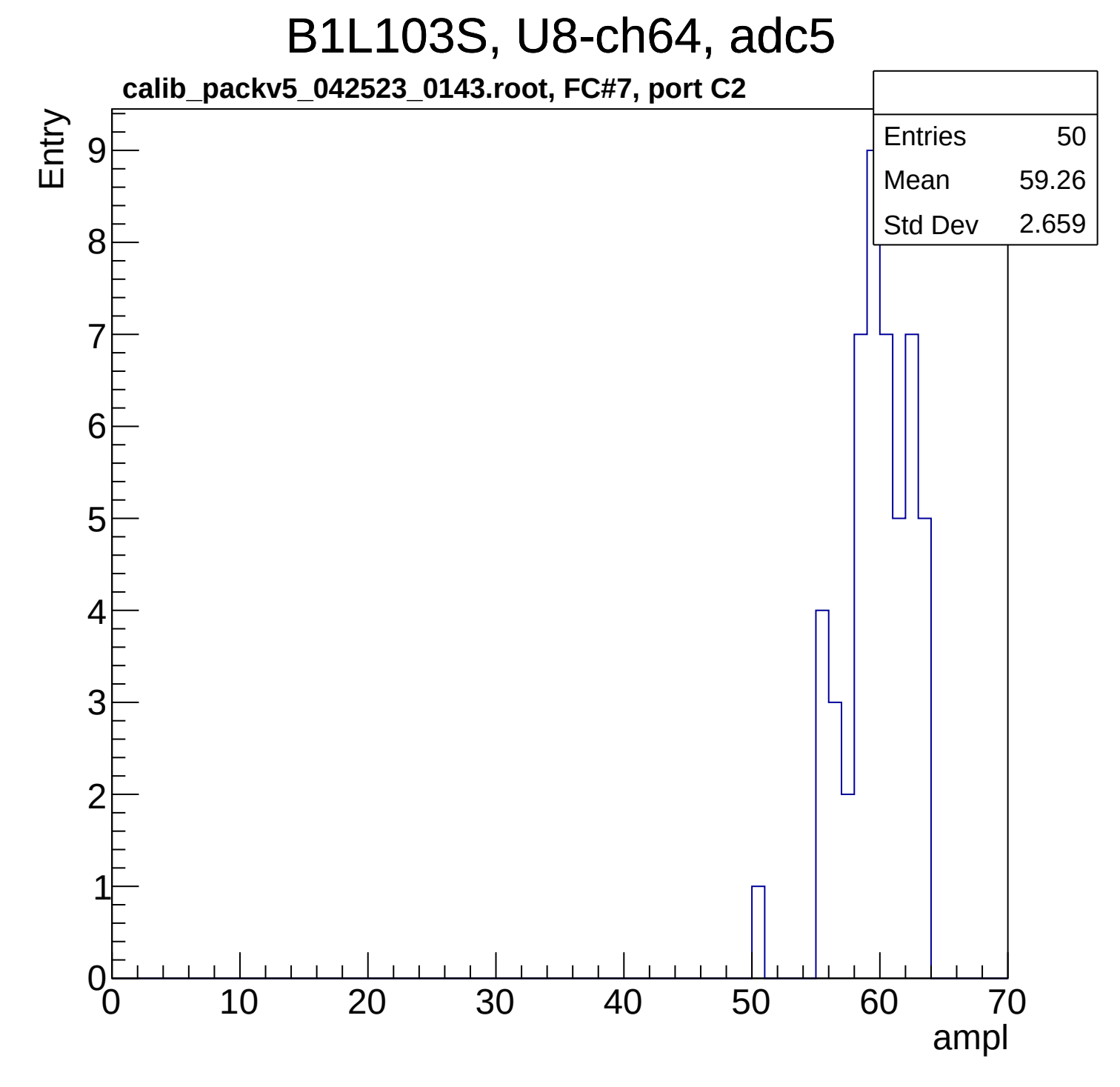

B1L103S, U8-ch64, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 83
Mean 28.96
Std Dev 5.114
Gaus mean : 29.5477
Gaus Width: 4.4387
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

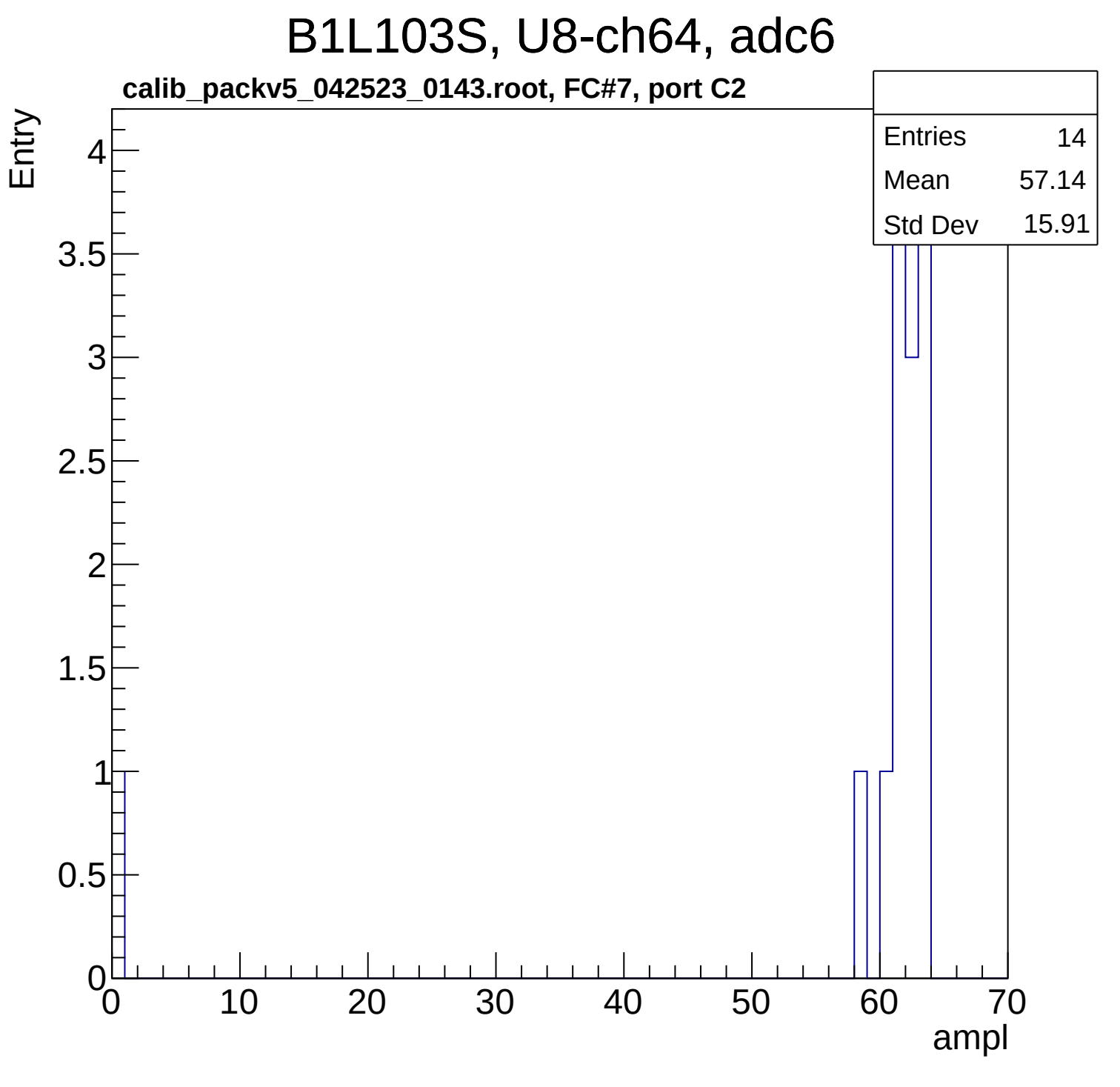

B1L103S, U8-ch64, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 36.46
Std Dev 3.907
Gaus mean : 37.3238
Gaus Width: 4.6332
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

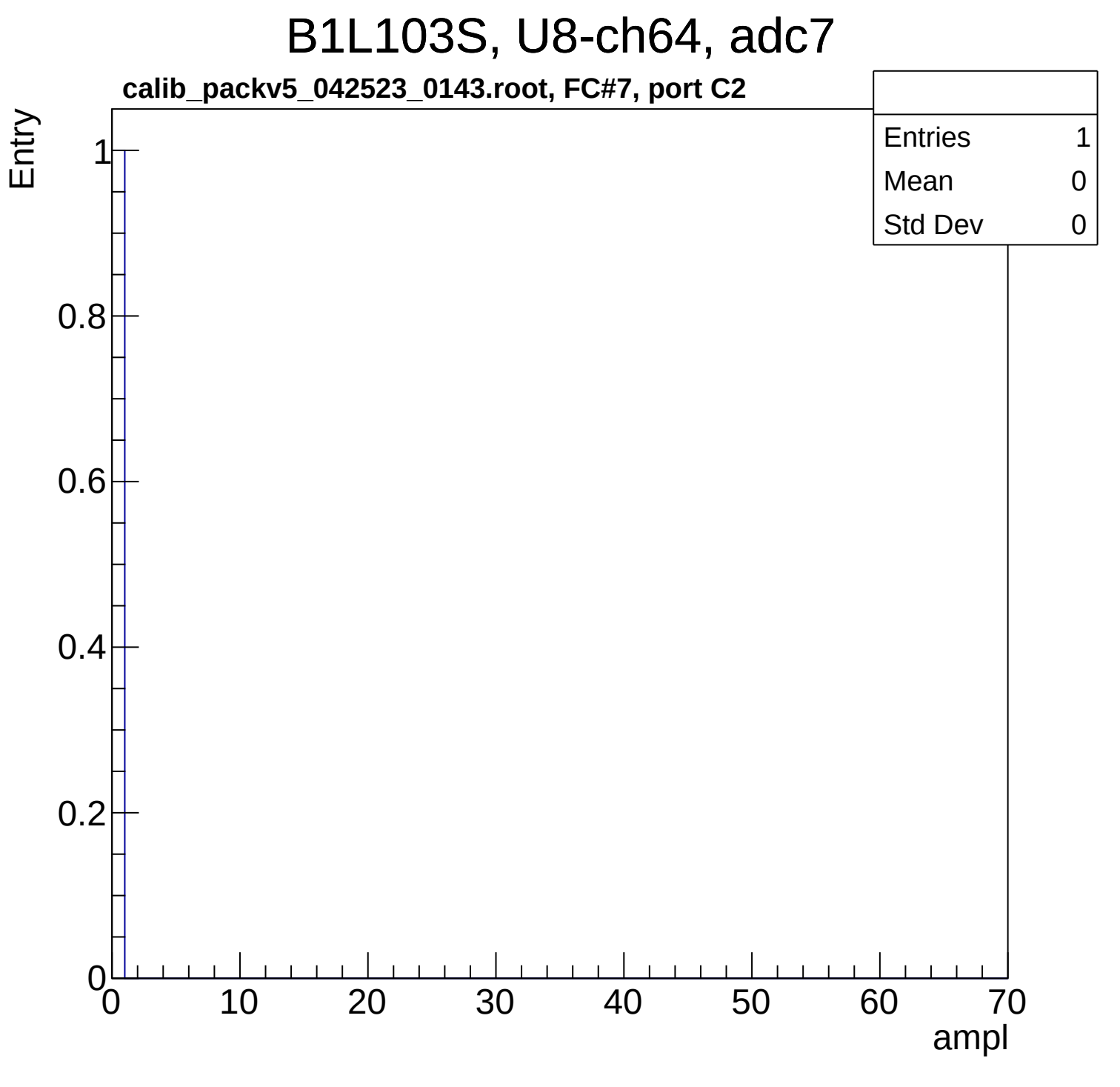

B1L103S, U8-ch64, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 42.84
Std Dev 3.87
Gaus mean : 43.1609
Gaus Width: 3.8391
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

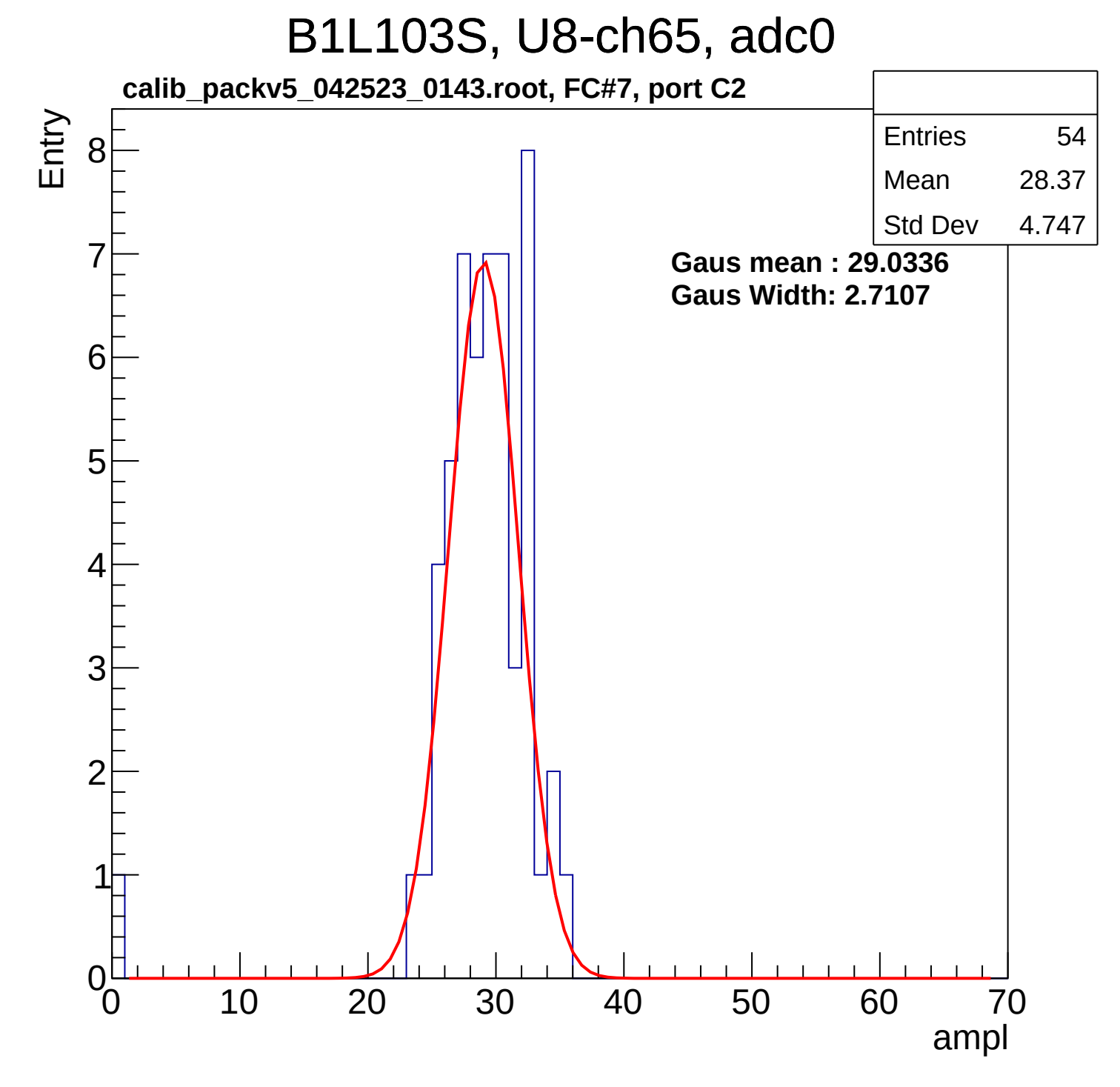

B1L103S, U8-ch64, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 48.49
Std Dev 3.792
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

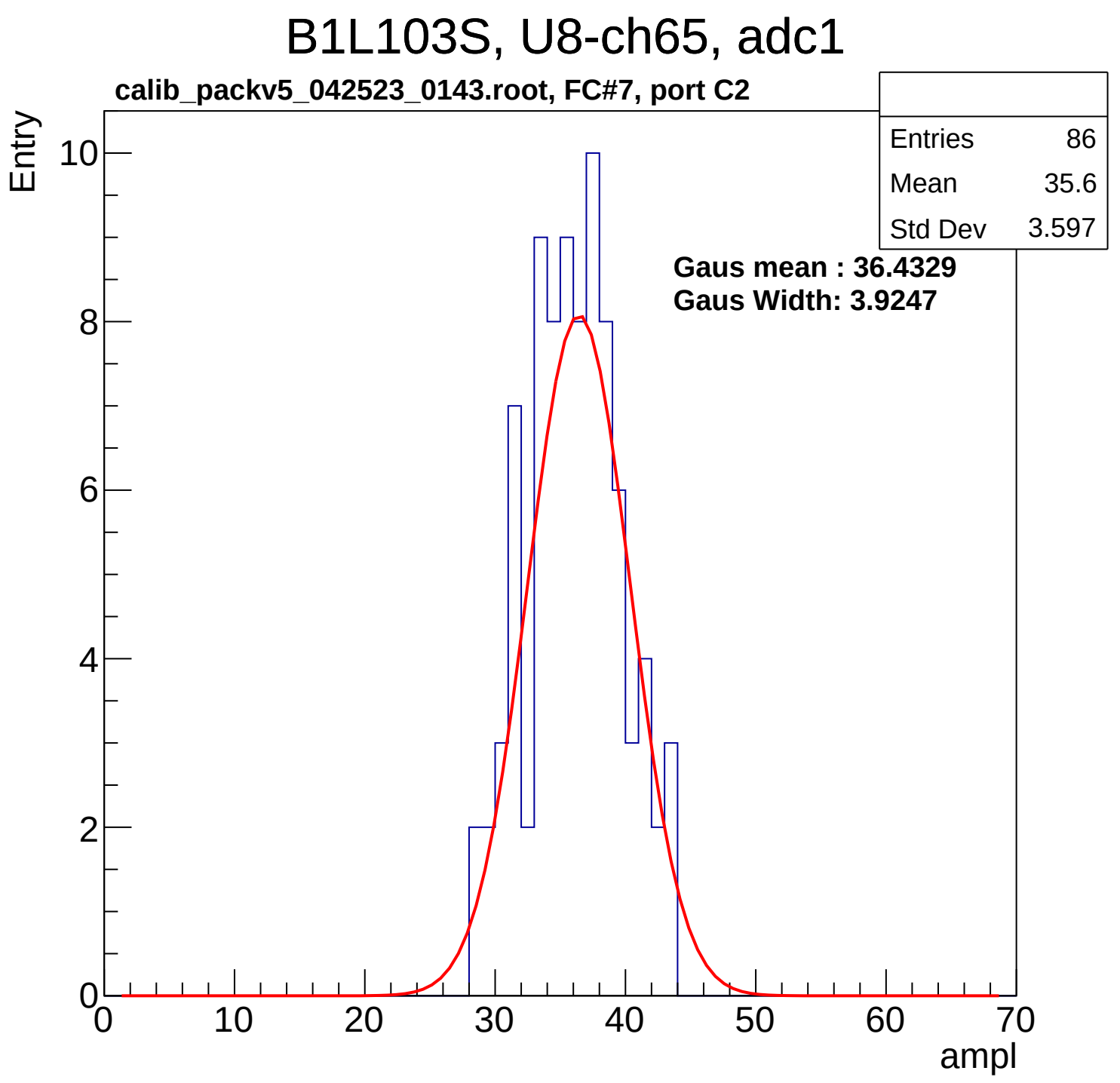

B1L103S, U8-ch64, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 54.2
Std Dev 3.423
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

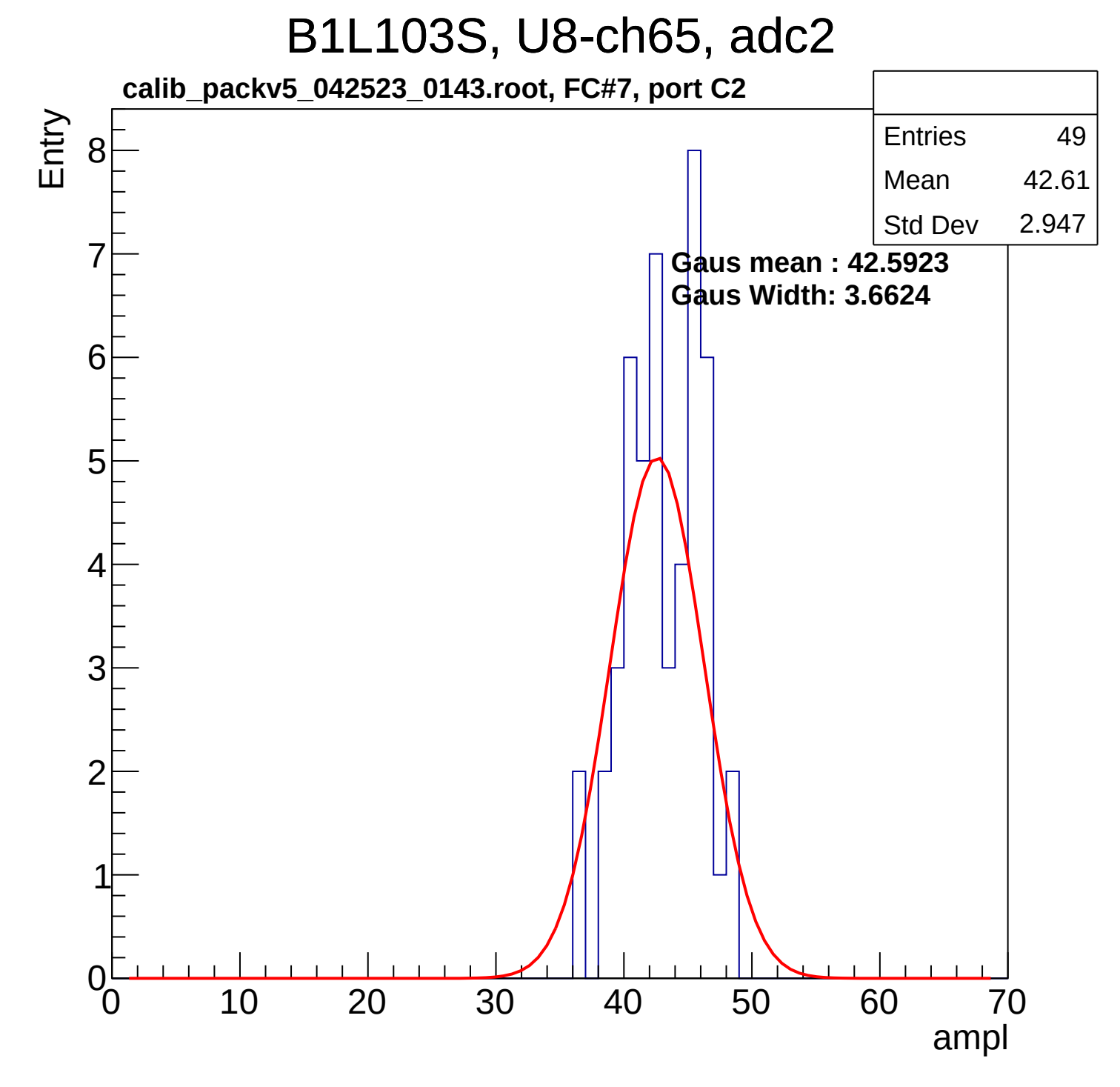

B1L103S, U8-ch64, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 59.26
Std Dev 2.659
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

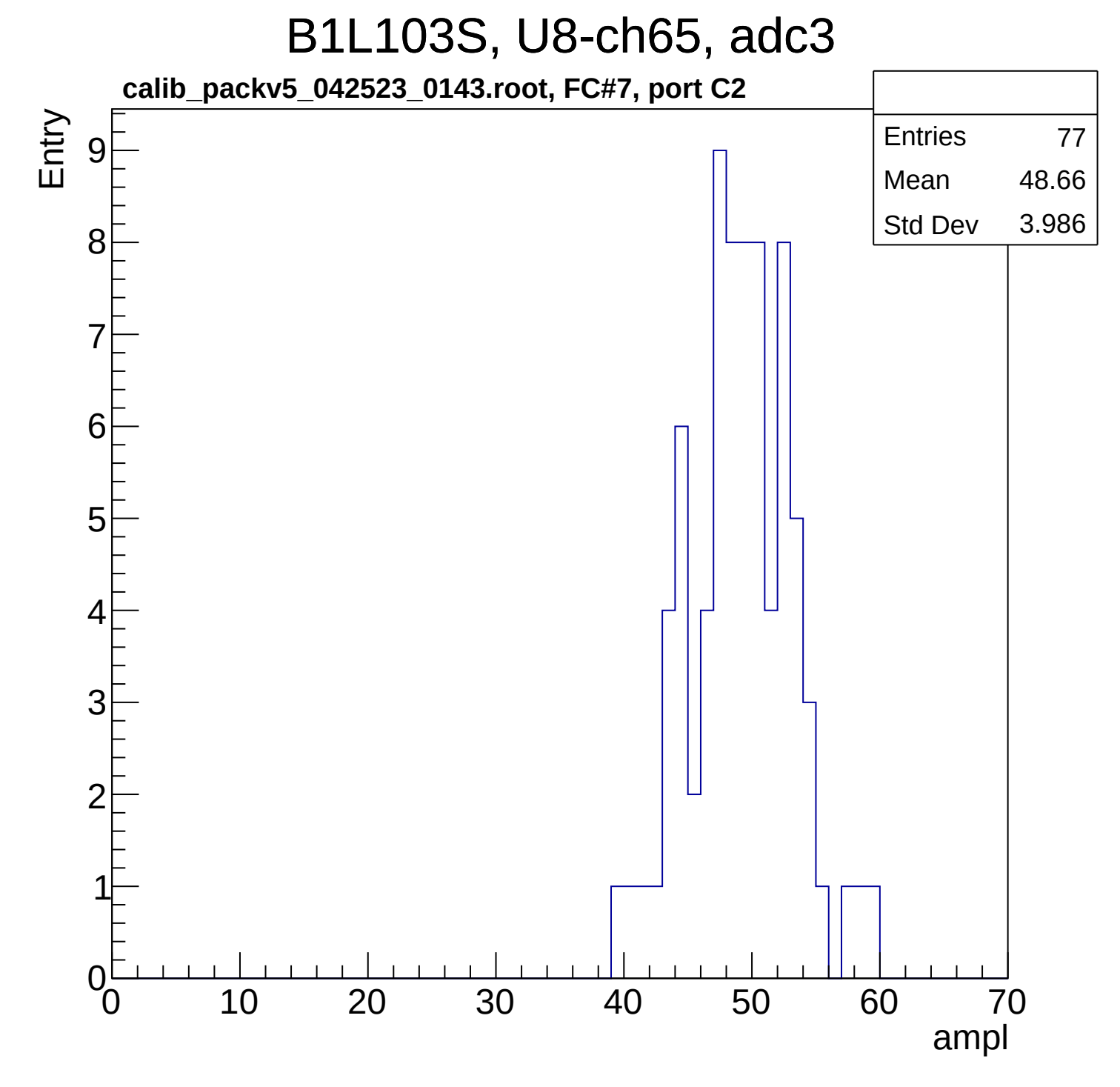

B1L103S, U8-ch64, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 14
Mean 57.14
Std Dev 15.91
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

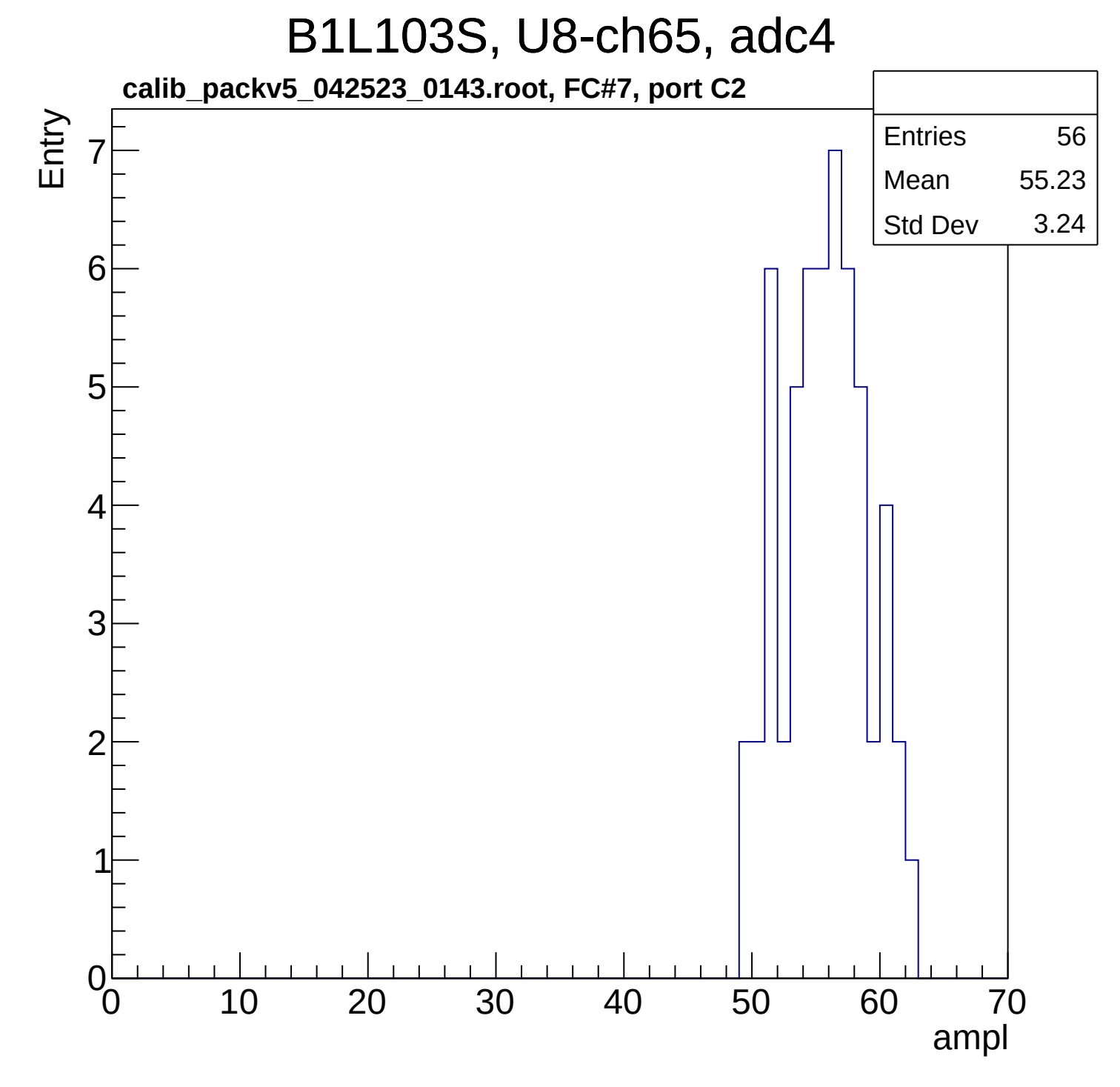

B1L103S, U8-ch64, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

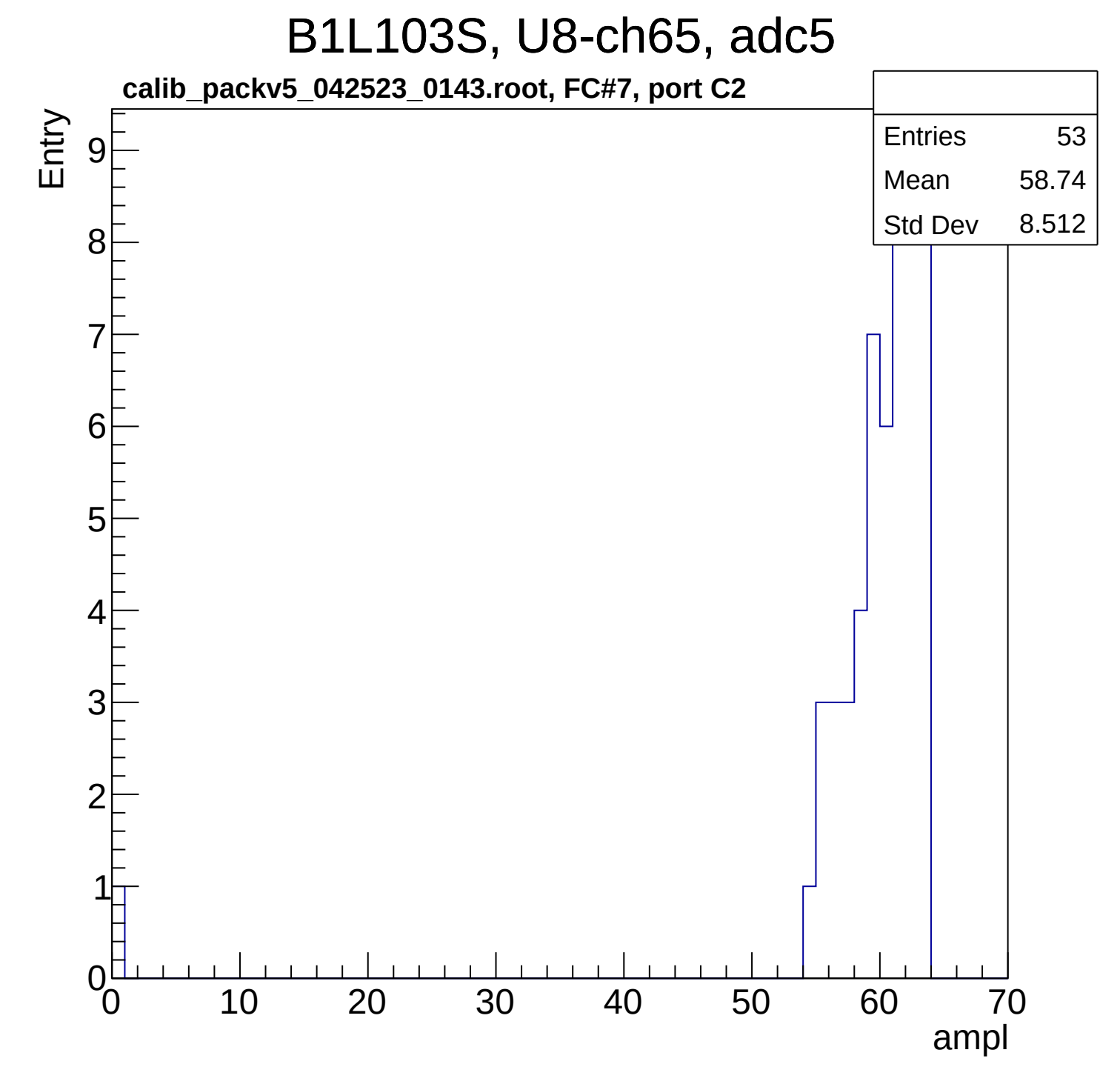

B1L103S, U8-ch65, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 28.37
Std Dev 4.747
Gaus mean : 29.0336
Gaus Width: 2.7107
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

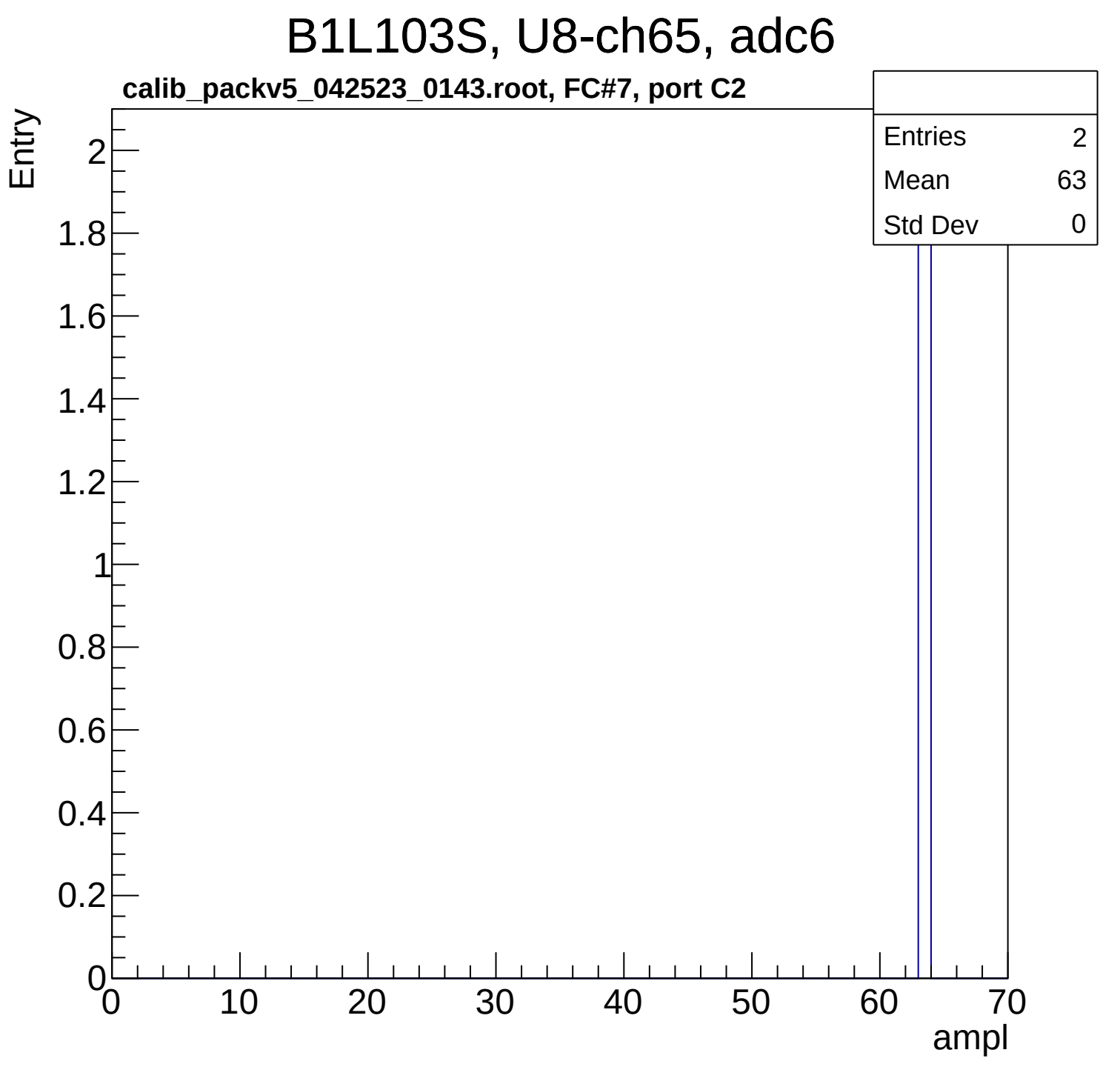

B1L103S, U8-ch65, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 86
Mean 35.6
Std Dev 3.597
Gaus mean : 36.4329
Gaus Width: 3.9247
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

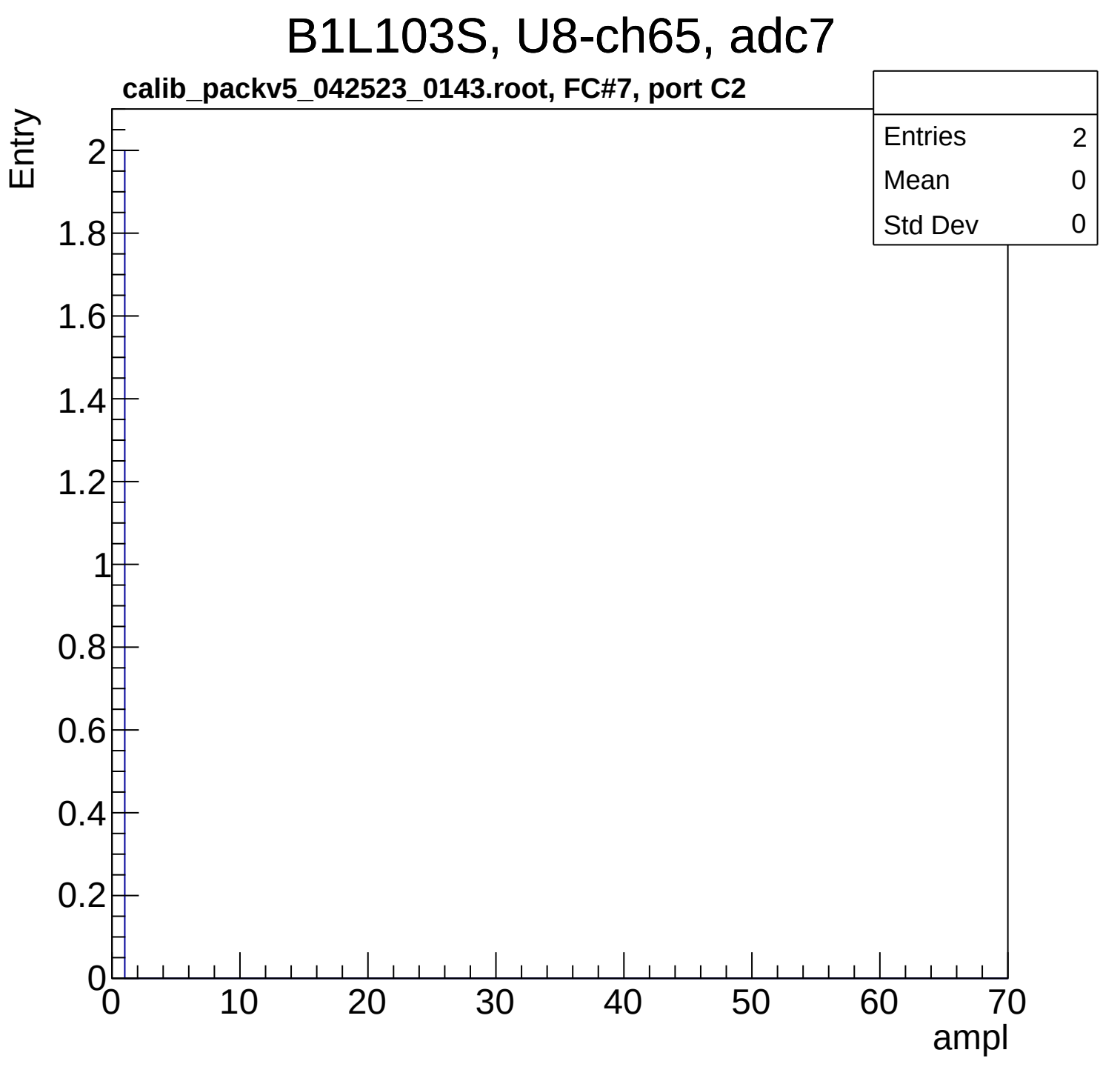

B1L103S, U8-ch65, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 42.61
Std Dev 2.947
Gaus mean : 42.5923
Gaus Width: 3.6624
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

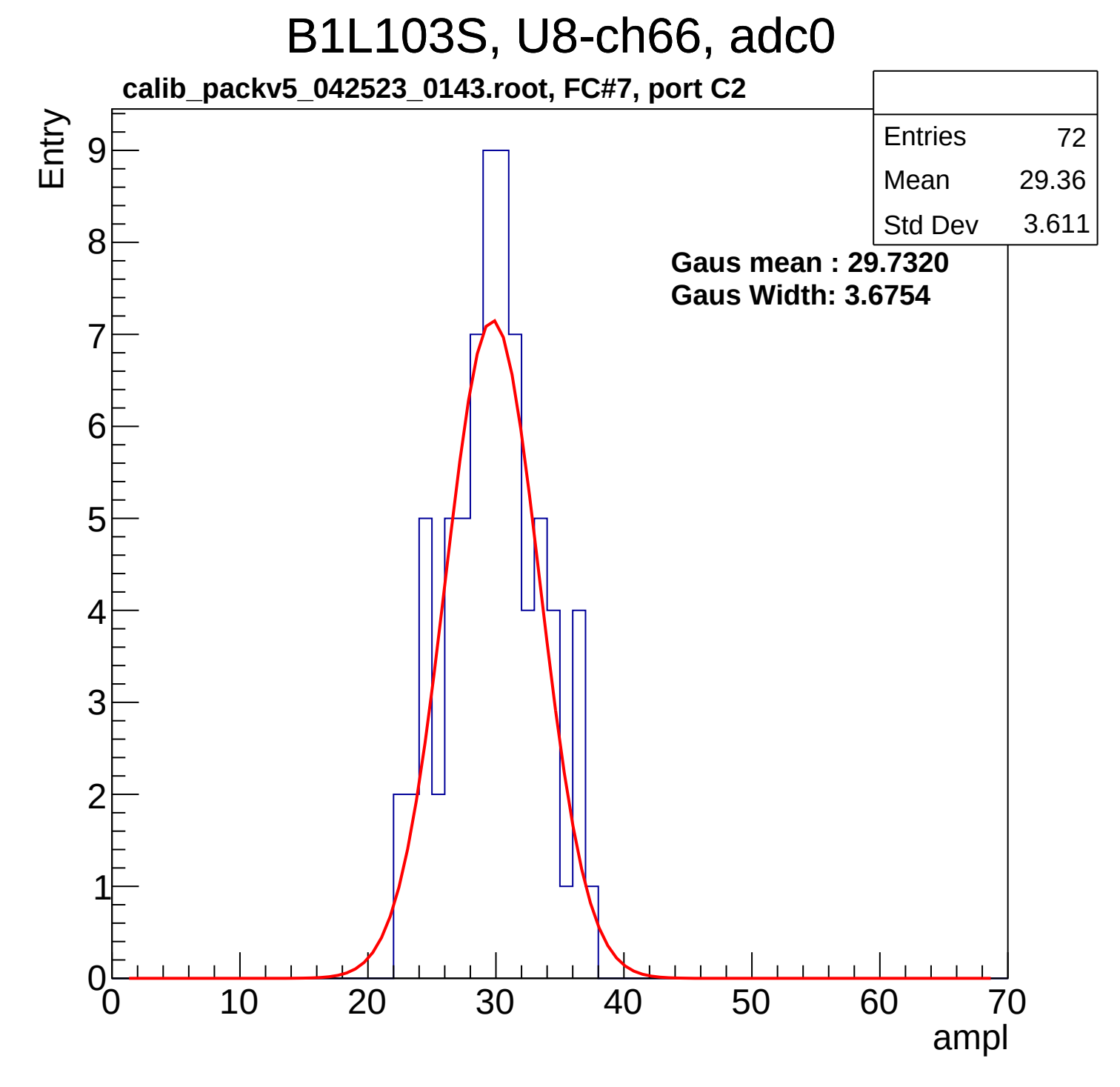

B1L103S, U8-ch65, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 48.66
Std Dev 3.986
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

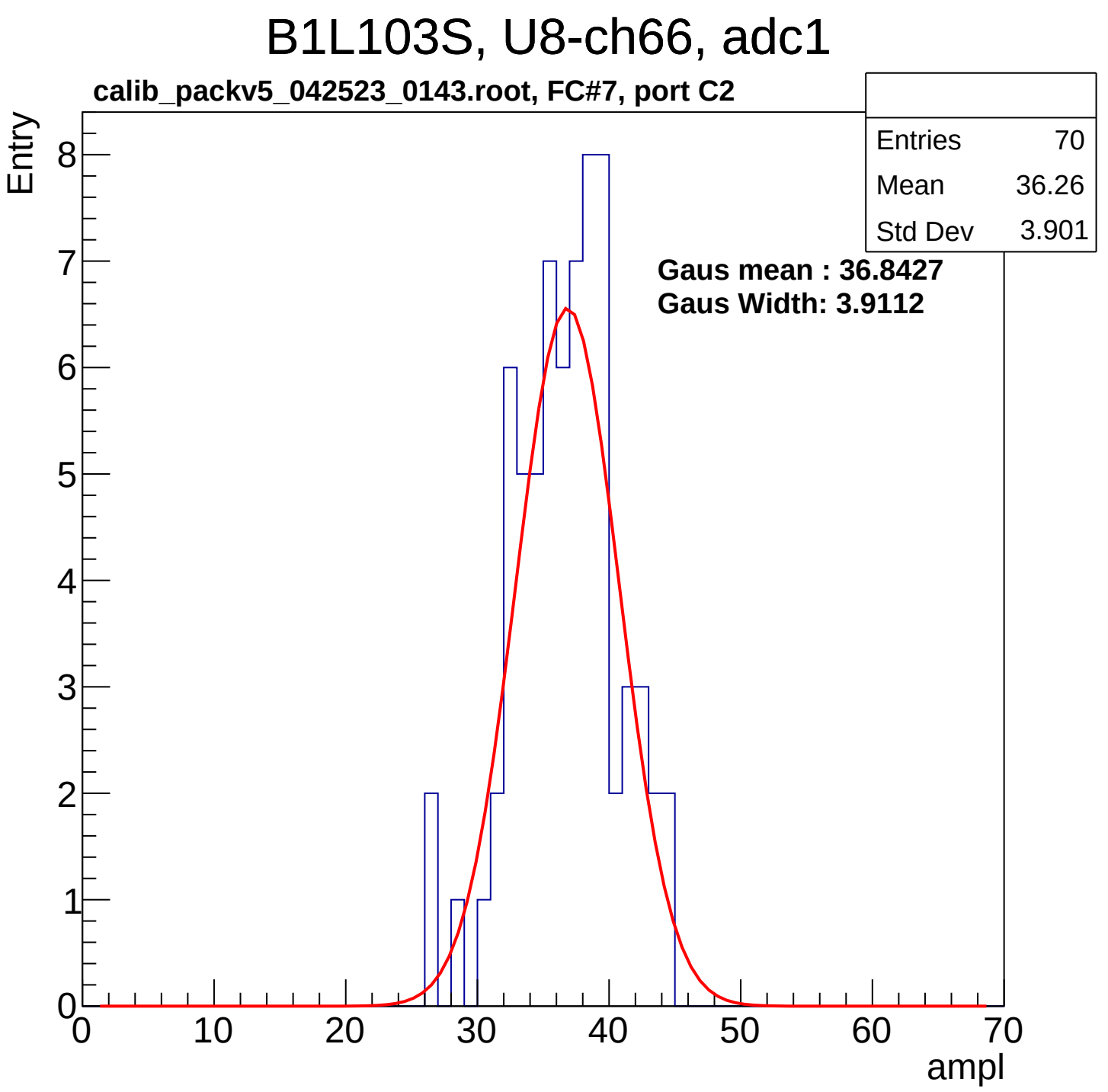

B1L103S, U8-ch65, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 55.23
Std Dev 3.24
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

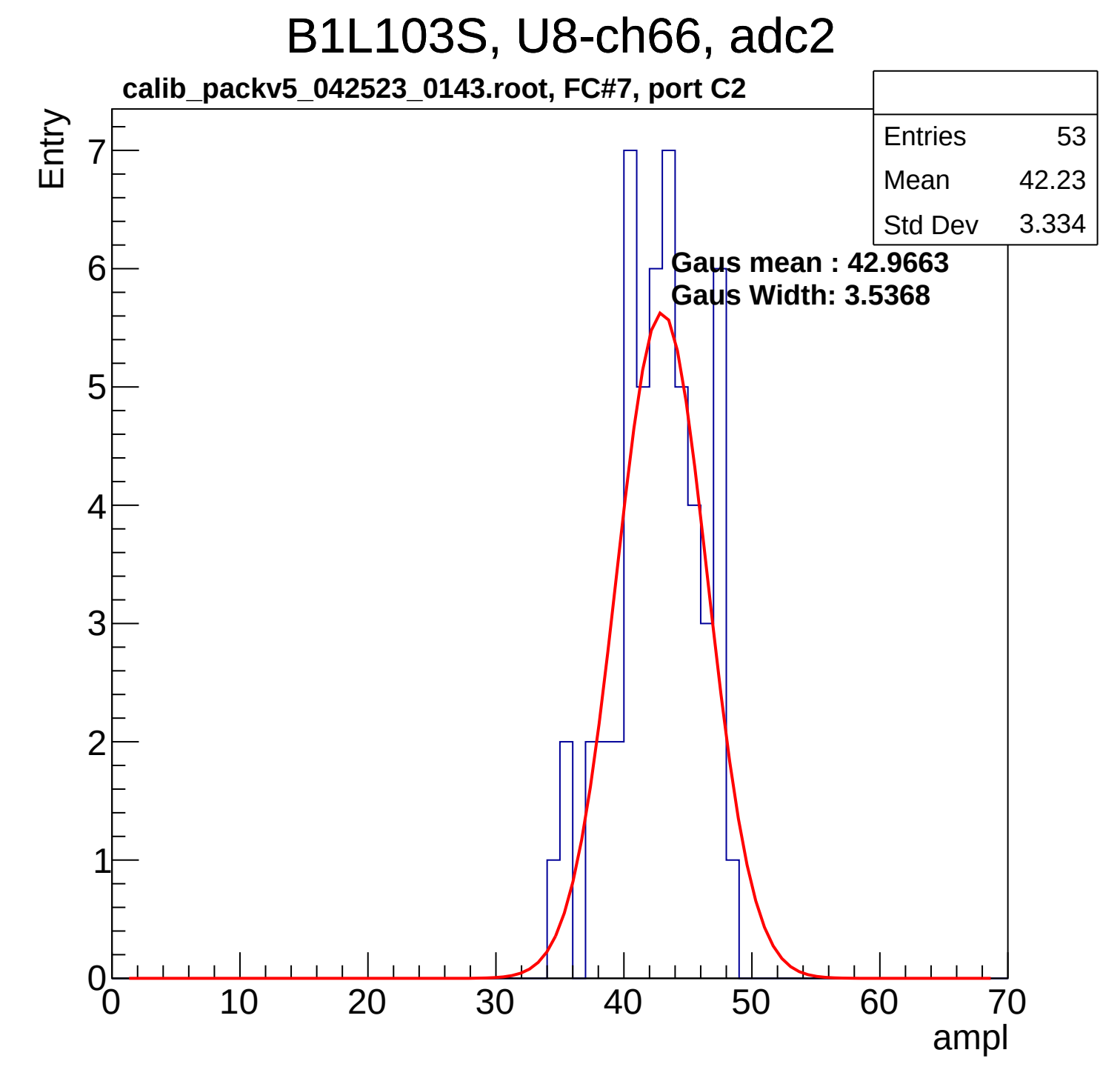

B1L103S, U8-ch65, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 58.74
Std Dev 8.512
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

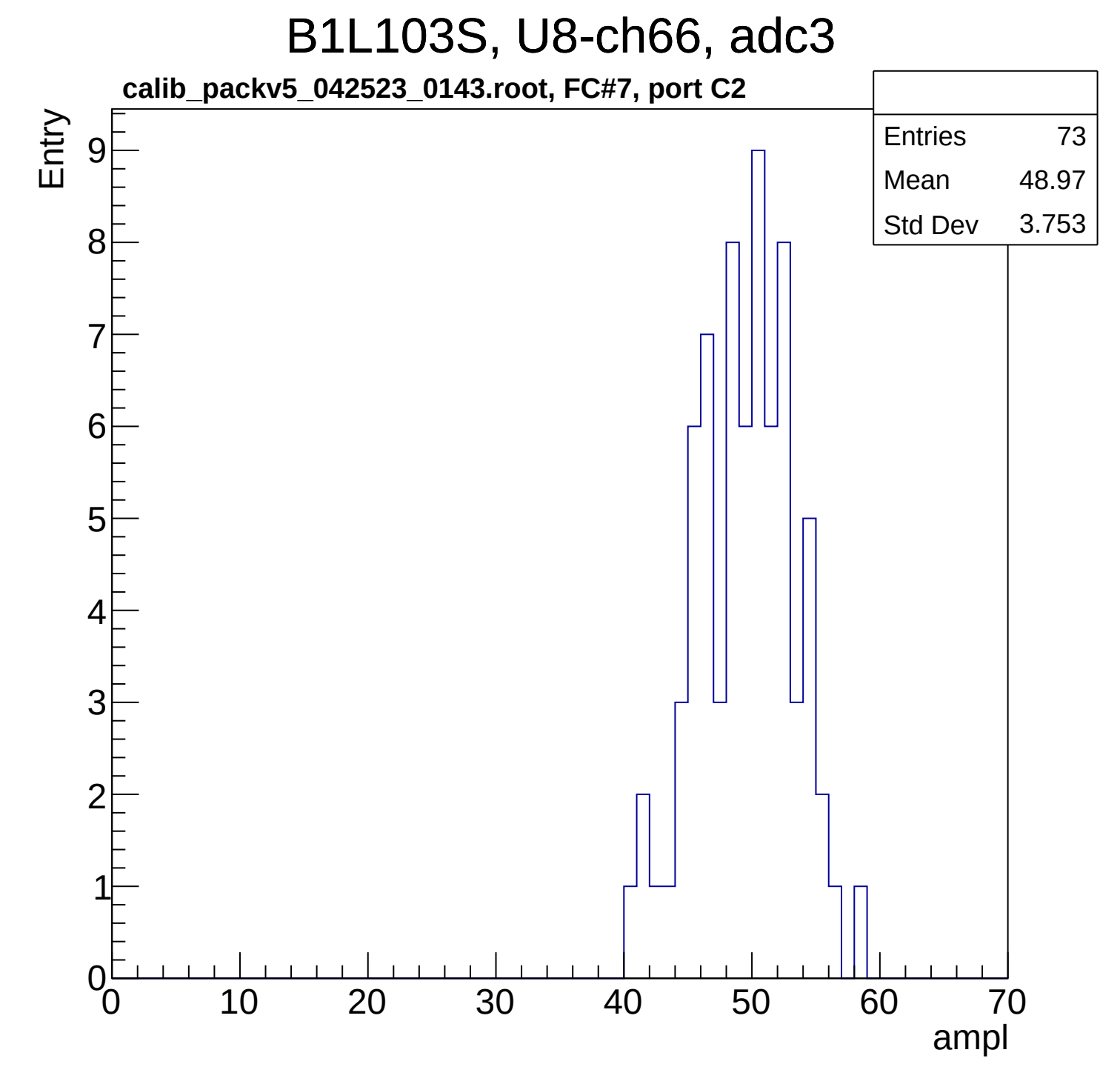

B1L103S, U8-ch65, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

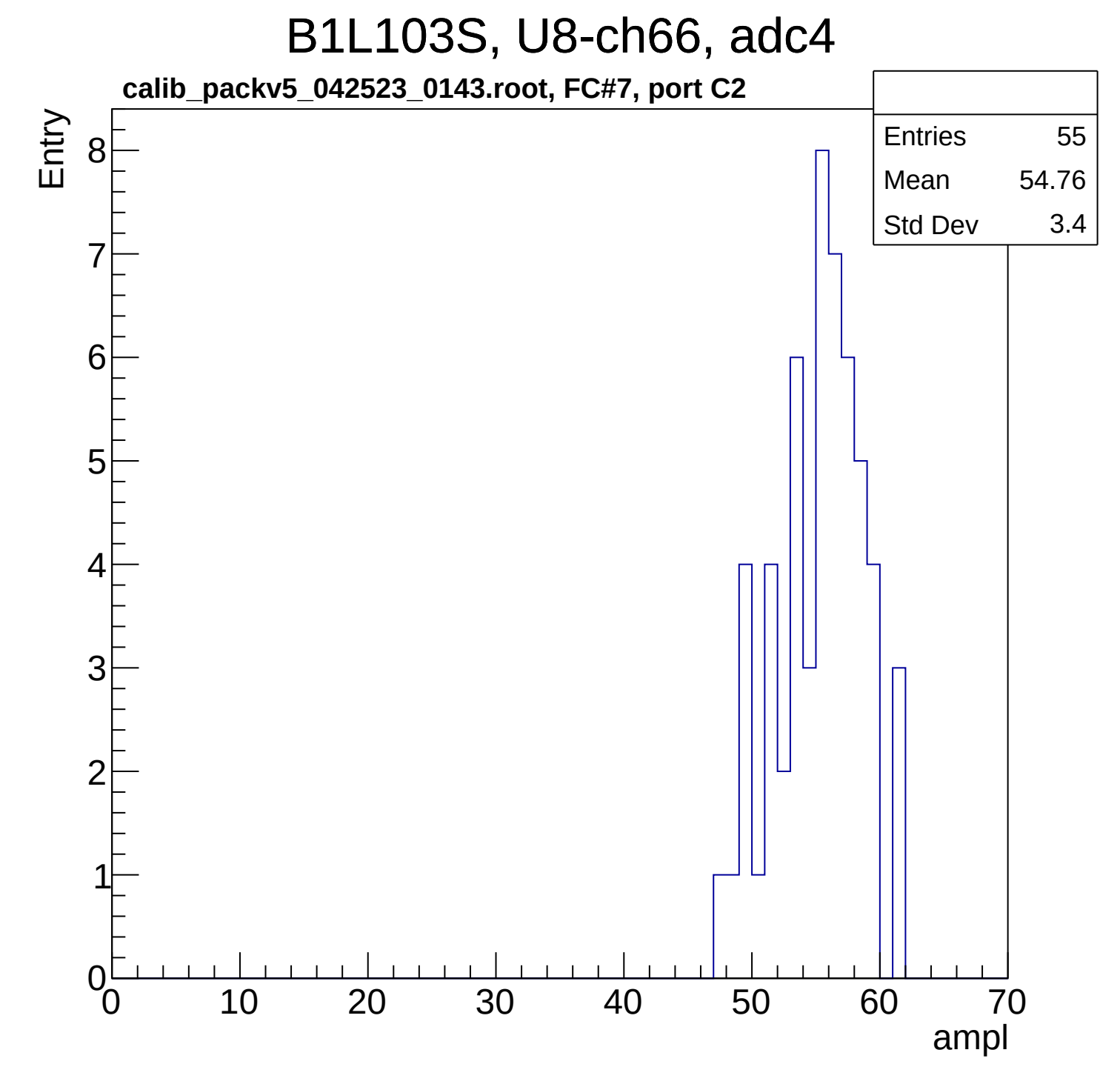

B1L103S, U8-ch65, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

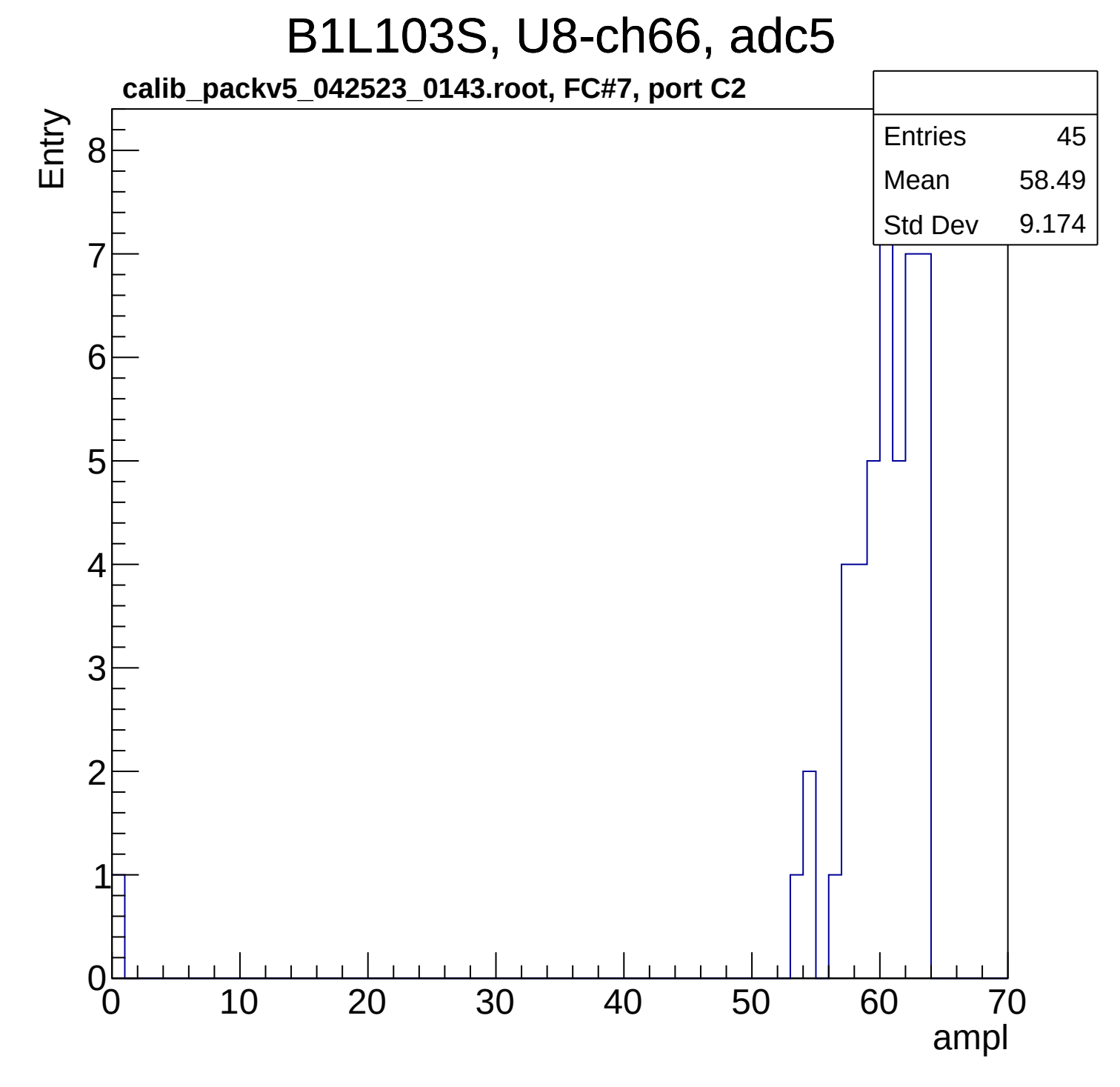

B1L103S, U8-ch66, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 29.36
Std Dev 3.611
Gaus mean : 29.7320
Gaus Width: 3.6754
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

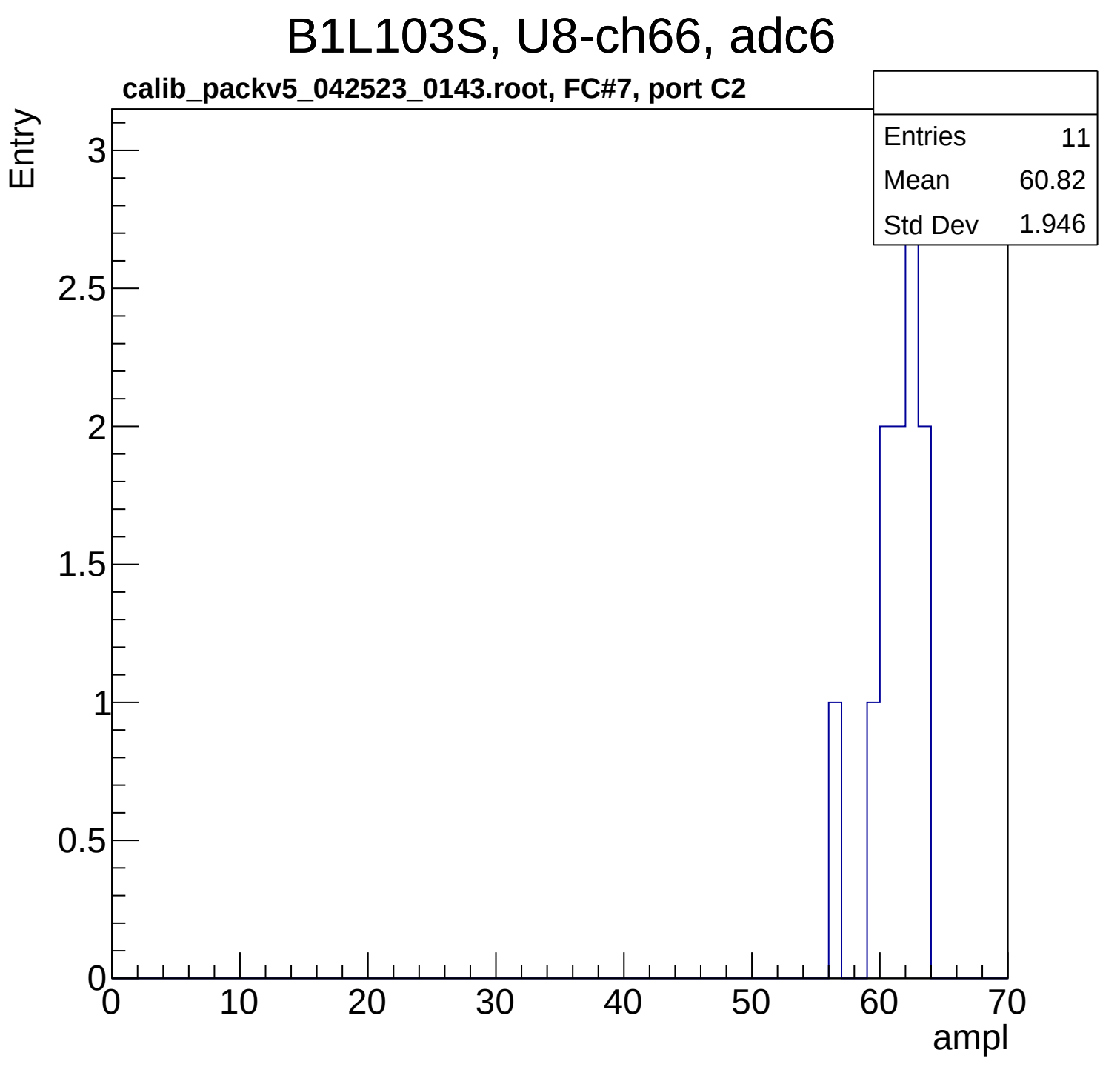

B1L103S, U8-ch66, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 36.26
Std Dev 3.901
Gaus mean : 36.8427
Gaus Width: 3.9112
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

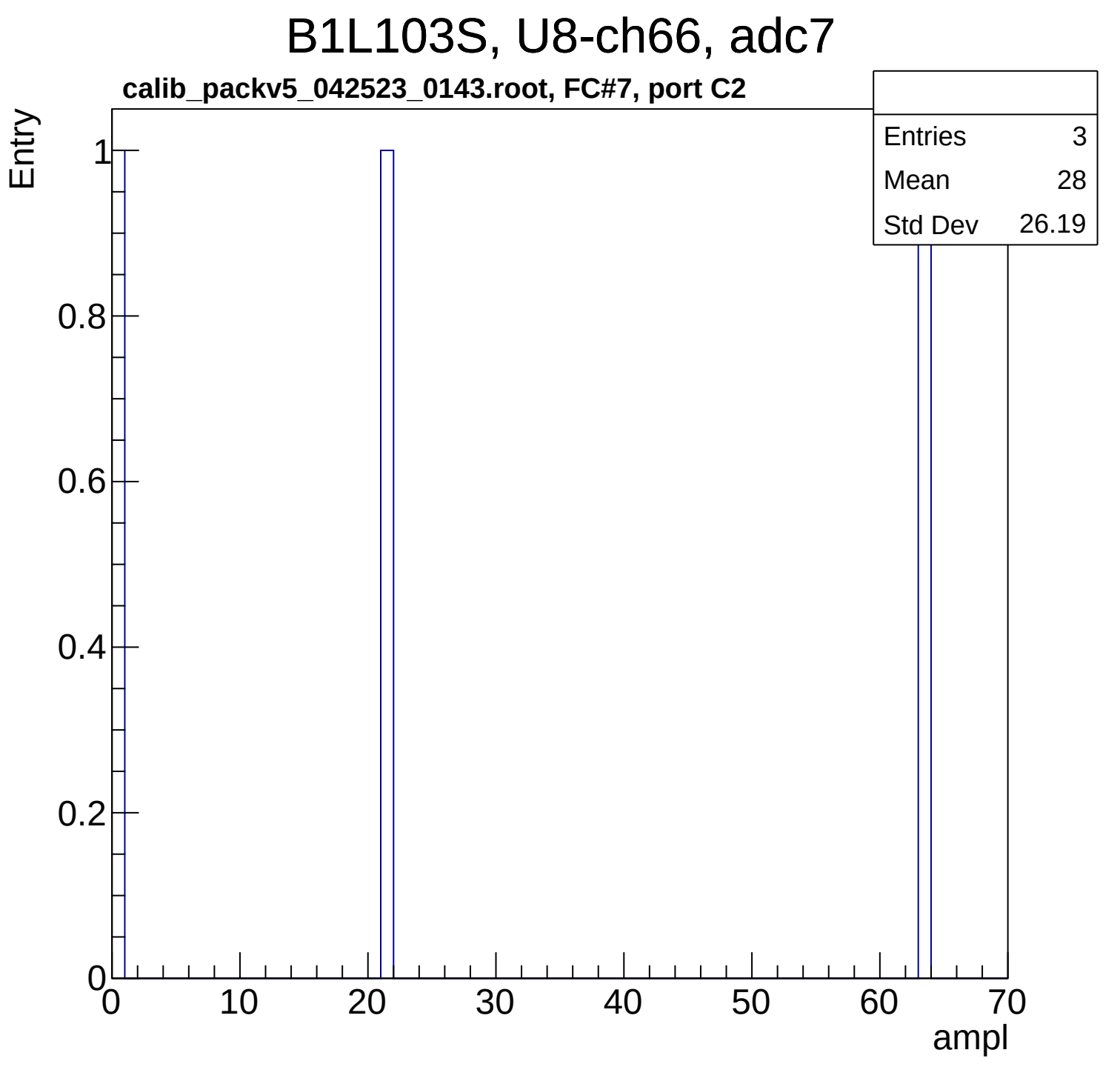

B1L103S, U8-ch66, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 42.23
Std Dev 3.334
Gaus mean : 42.9663
Gaus Width: 3.5368
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

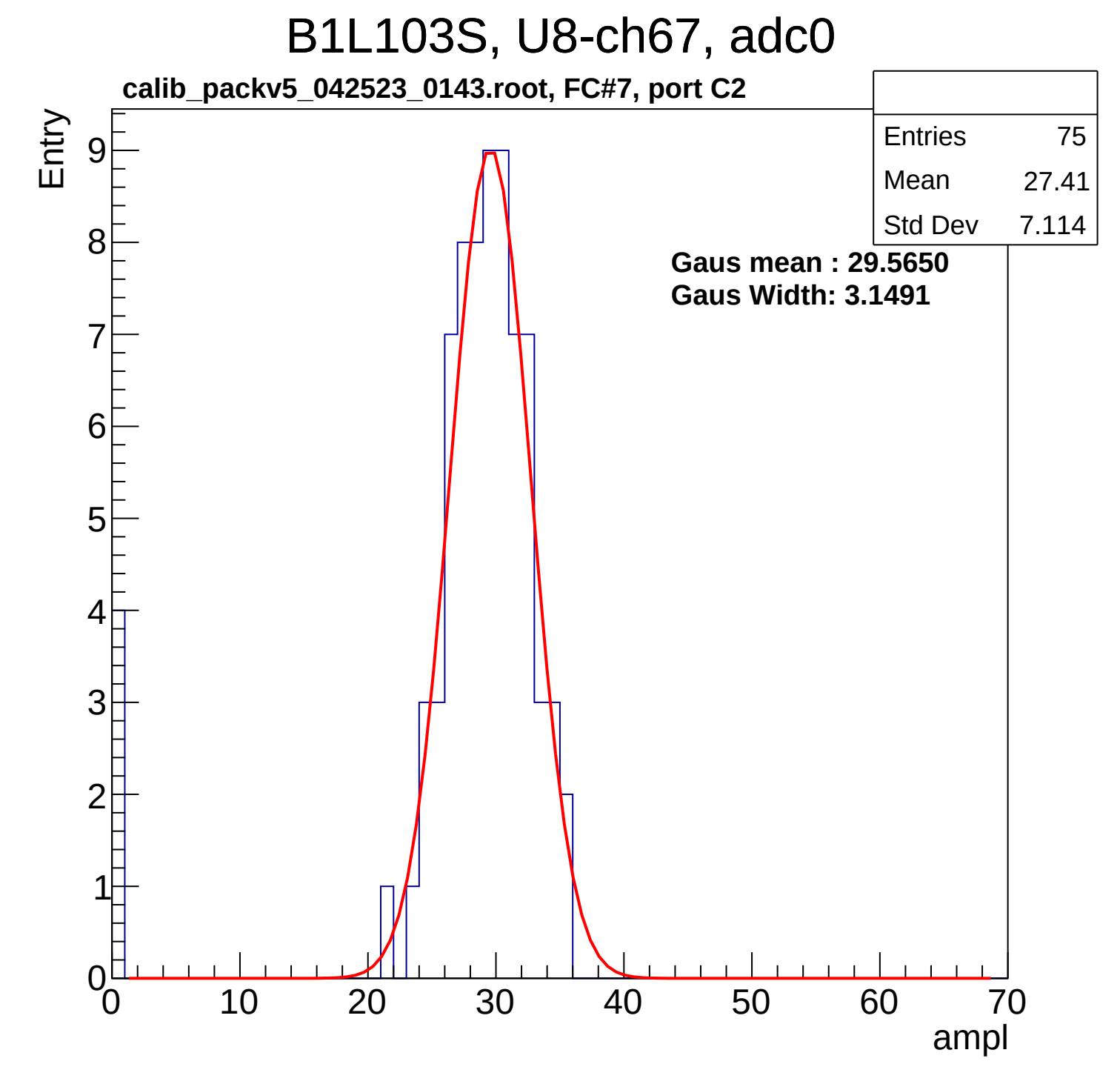

B1L103S, U8-ch66, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 48.97
Std Dev 3.753
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

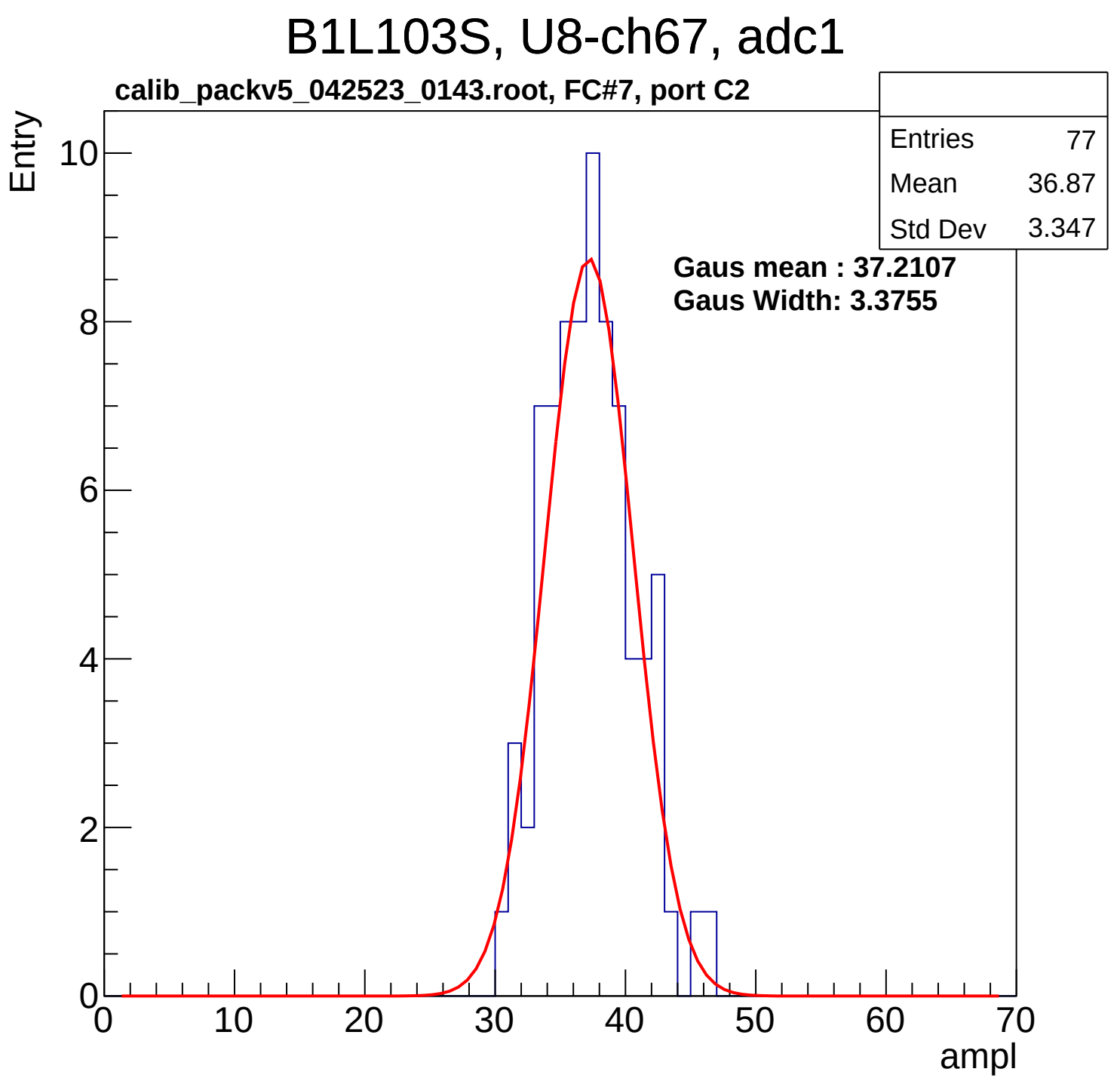

B1L103S, U8-ch66, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 54.76
Std Dev 3.4
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

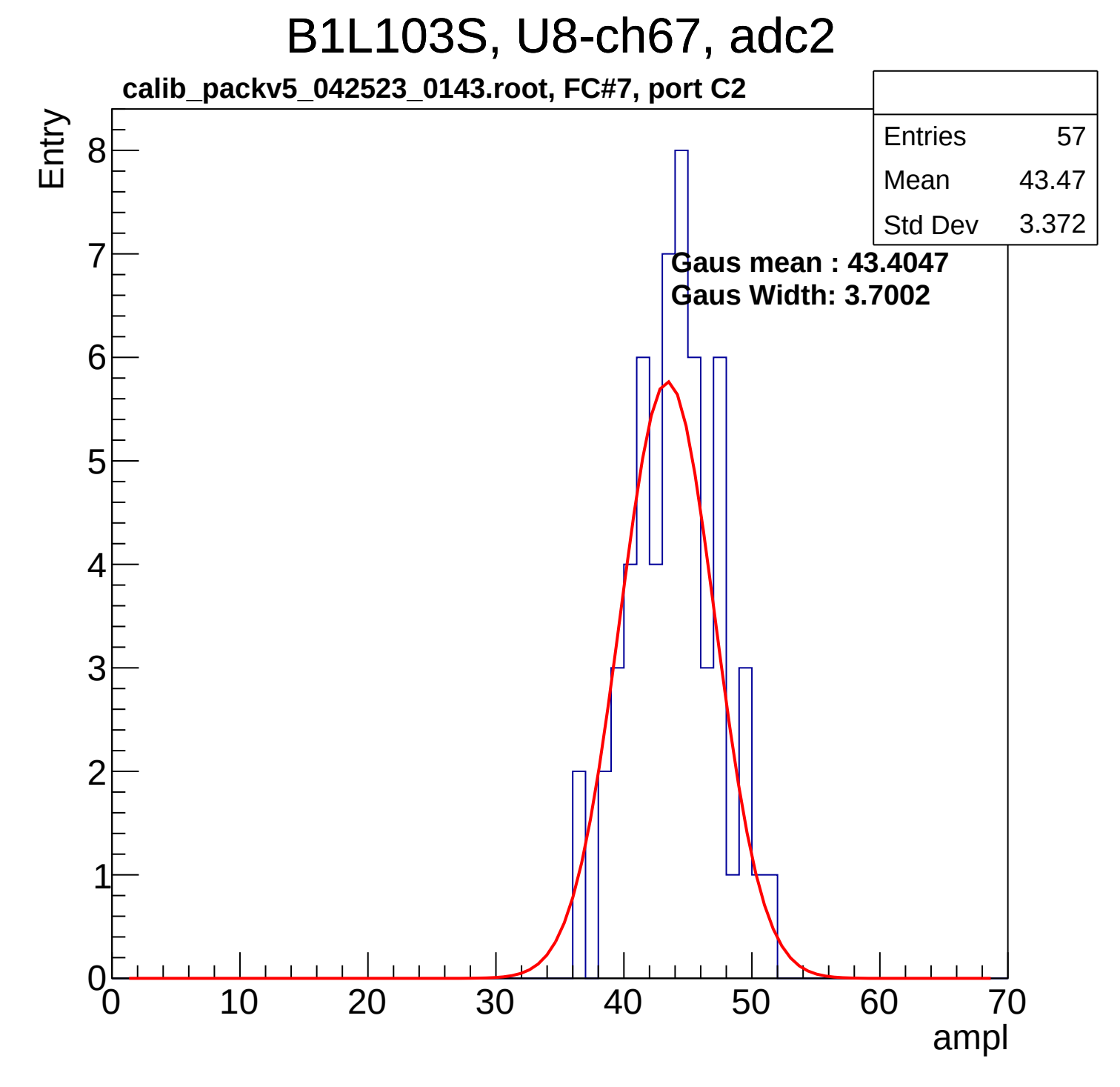

B1L103S, U8-ch66, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 45
Mean 58.49
Std Dev 9.174
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

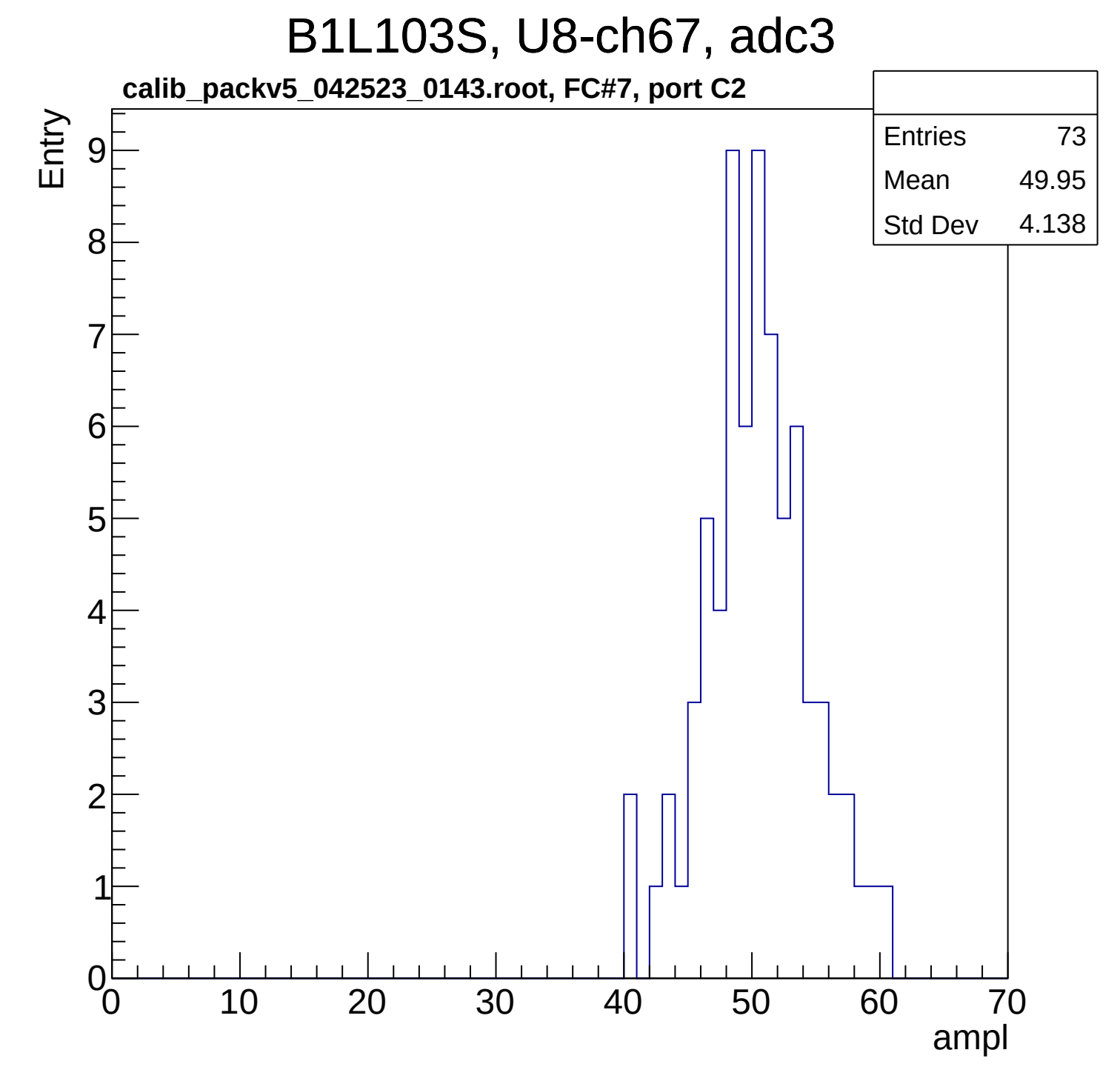

B1L103S, U8-ch66, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 11
Mean 60.82
Std Dev 1.946
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

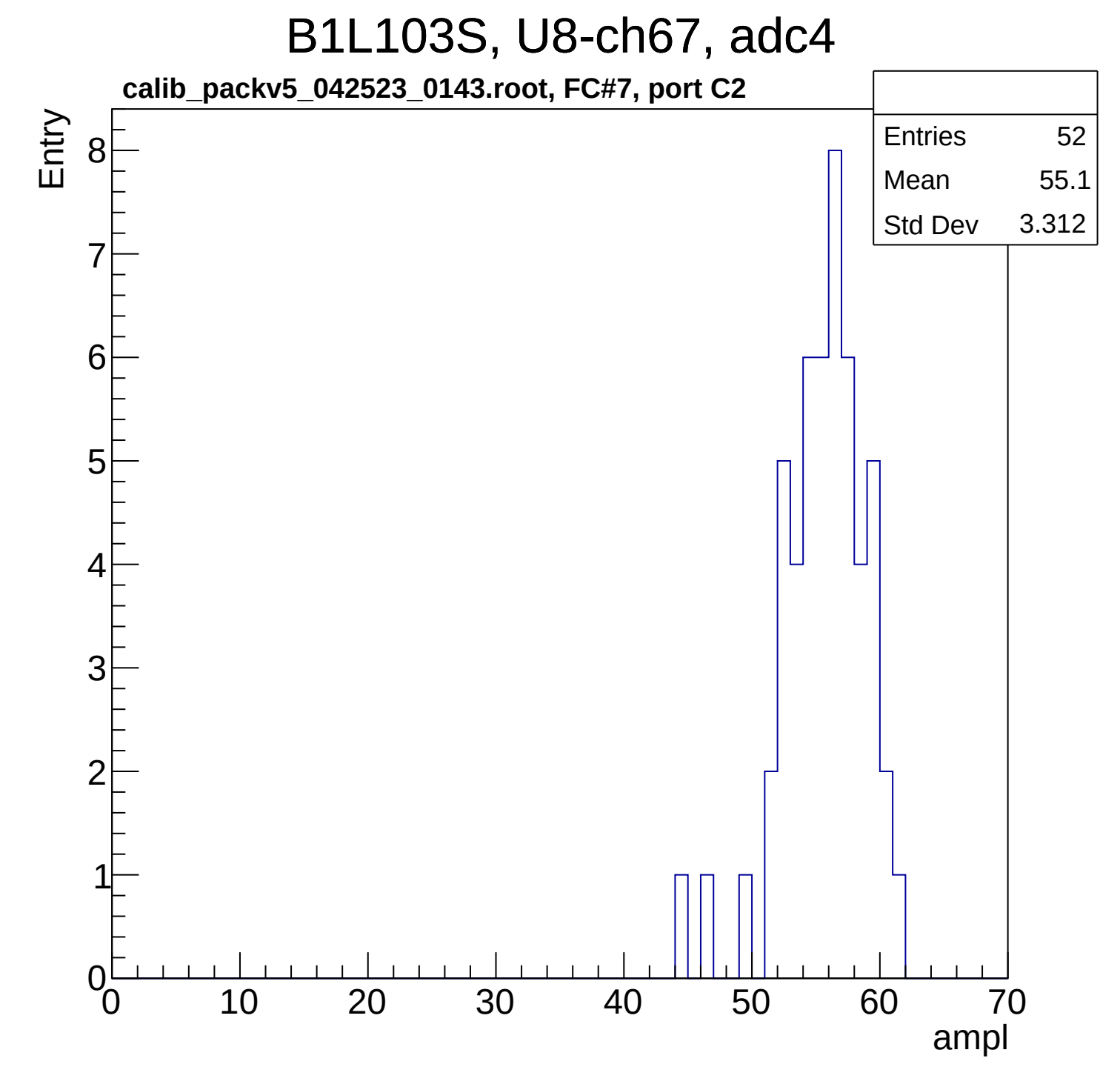

B1L103S, U8-ch66, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 28
Std Dev 26.19
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

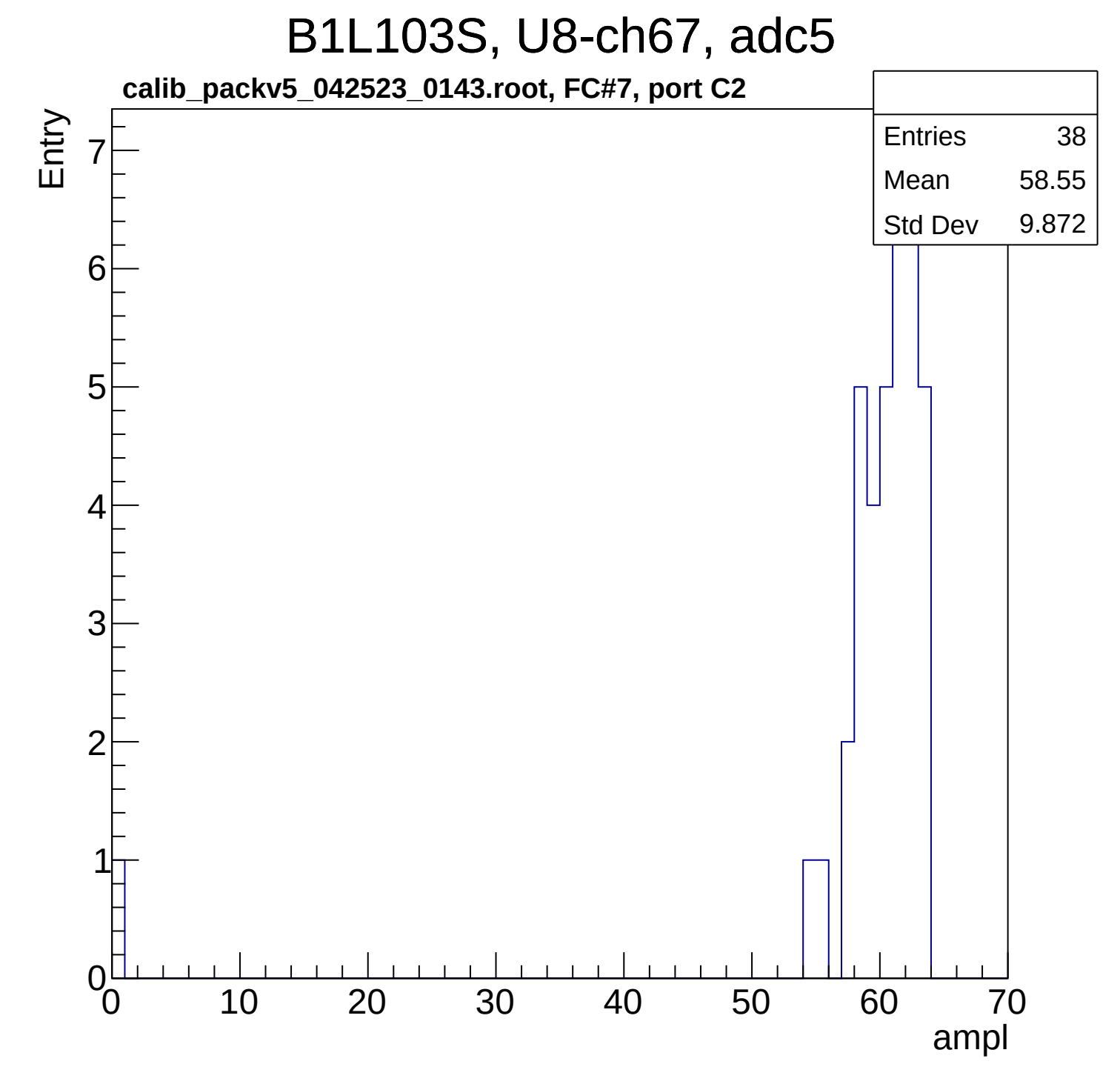

B1L103S, U8-ch67, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 27.41
Std Dev 7.114
Gaus mean : 29.5650
Gaus Width: 3.1491
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

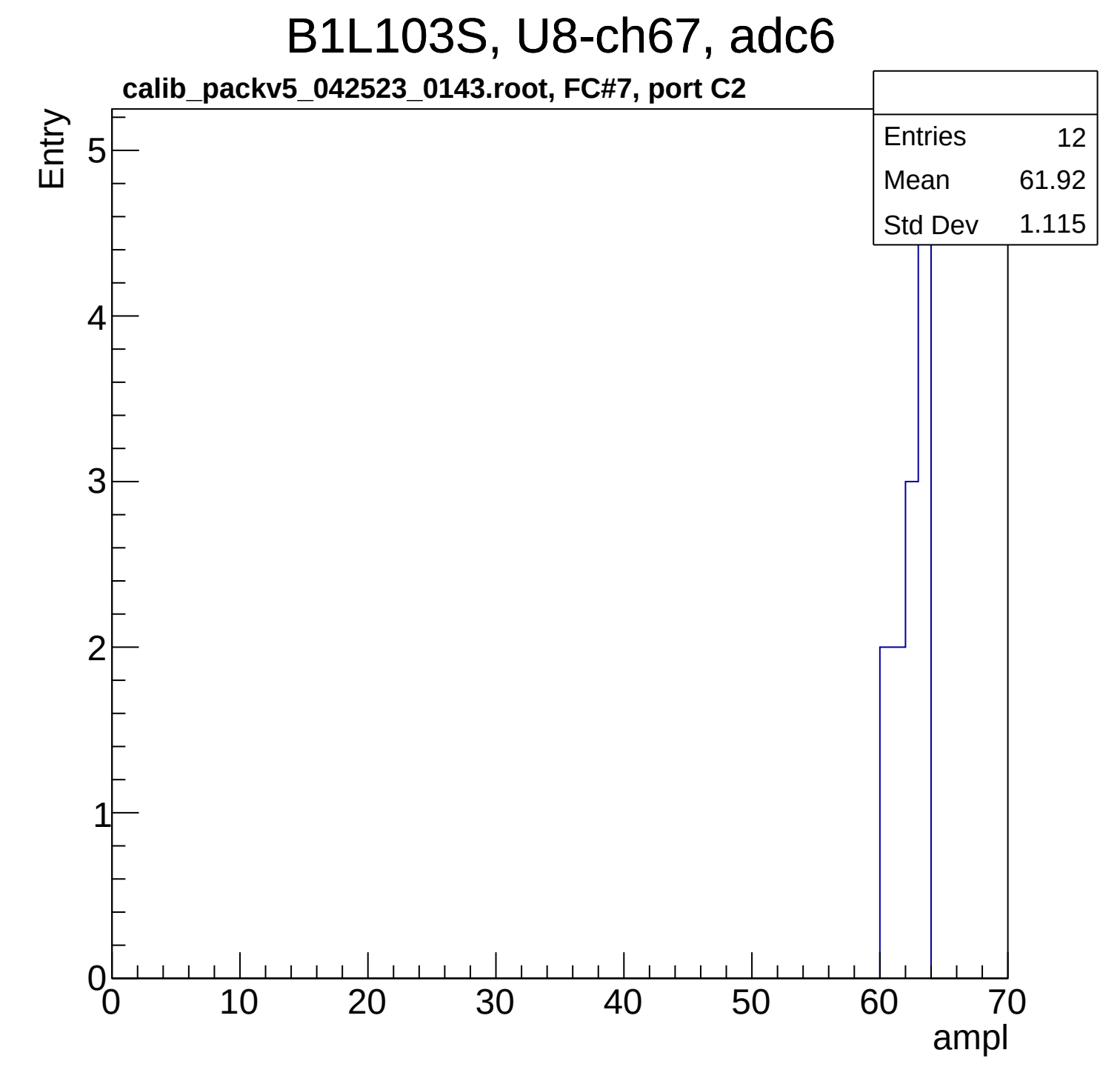

B1L103S, U8-ch67, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 36.87
Std Dev 3.347
Gaus mean : 37.2107
Gaus Width: 3.3755
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

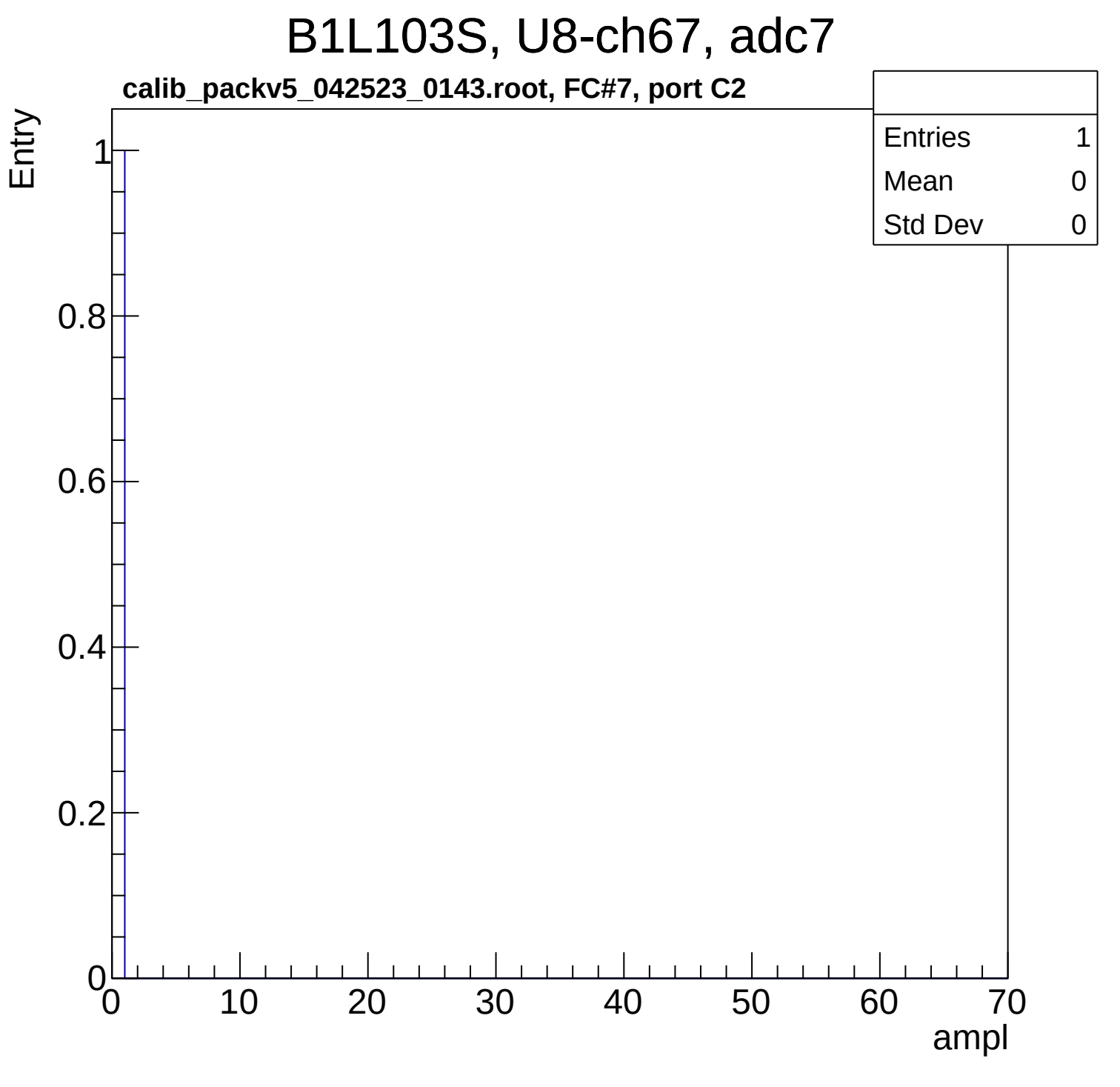

B1L103S, U8-ch67, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 43.47
Std Dev 3.372
Gaus mean : 43.4047
Gaus Width: 3.7002
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

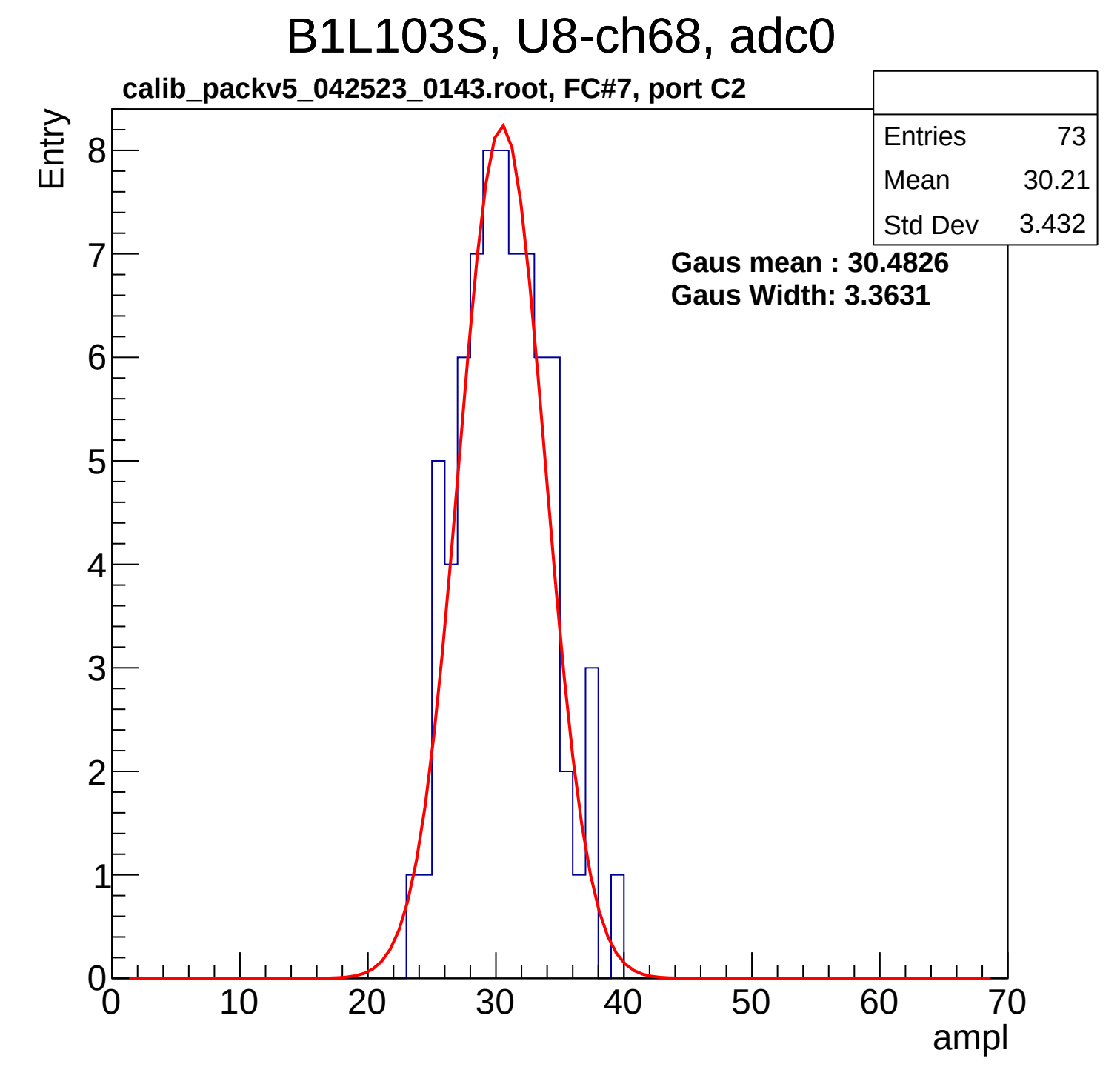

B1L103S, U8-ch67, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 49.95
Std Dev 4.138
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

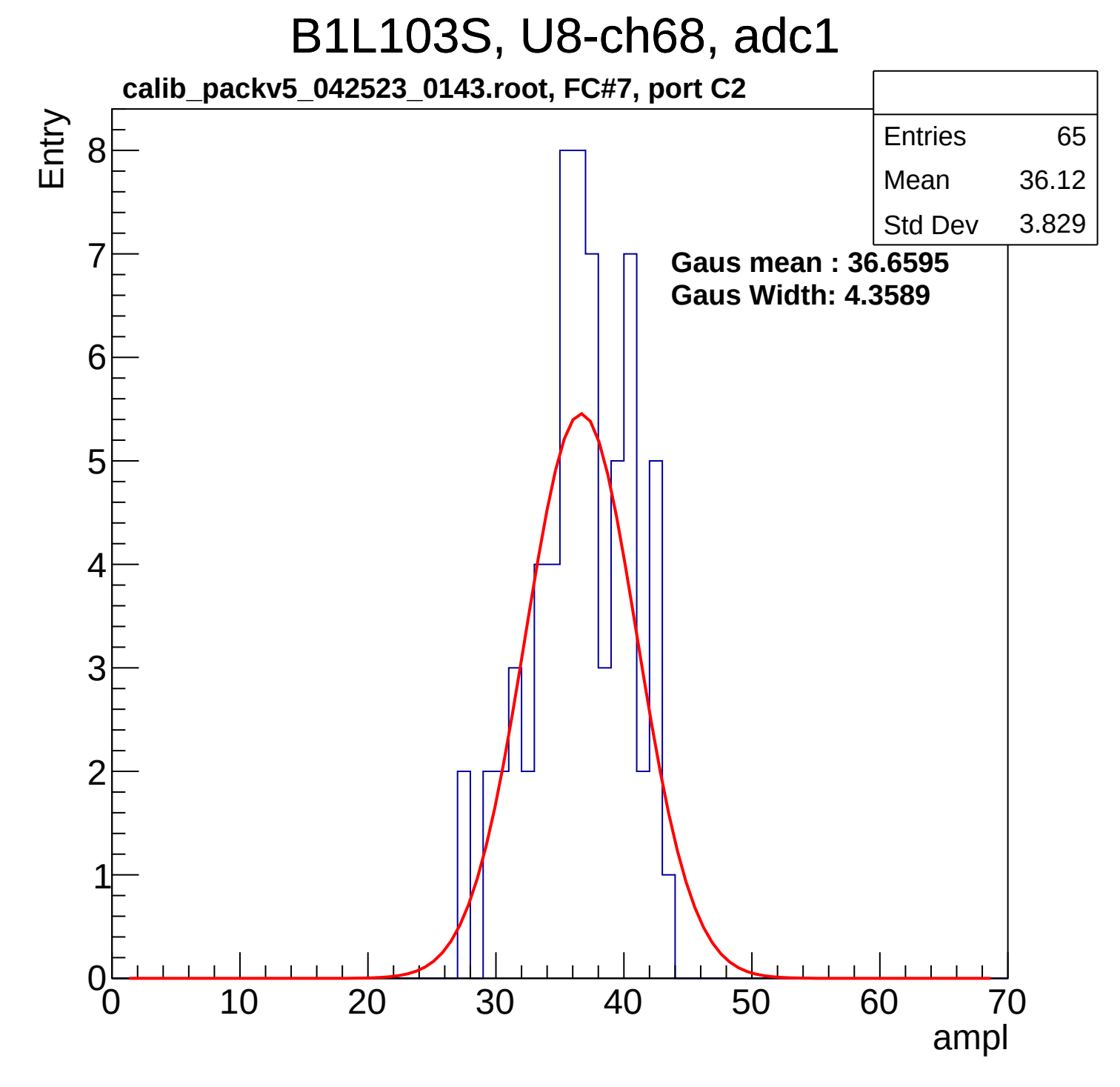

B1L103S, U8-ch67, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 55.1
Std Dev 3.312
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

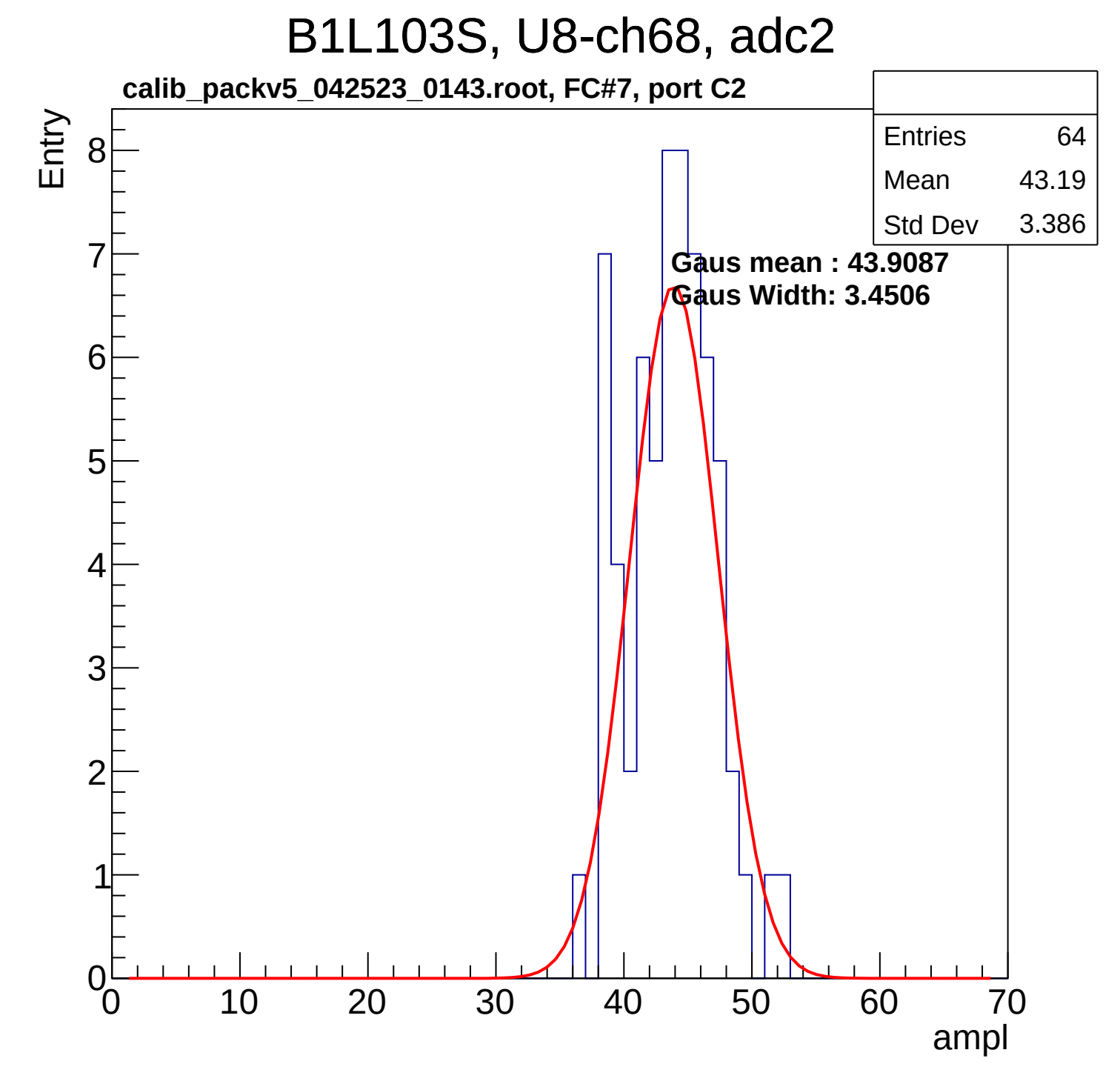

B1L103S, U8-ch67, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 38
Mean 58.55
Std Dev 9.872
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

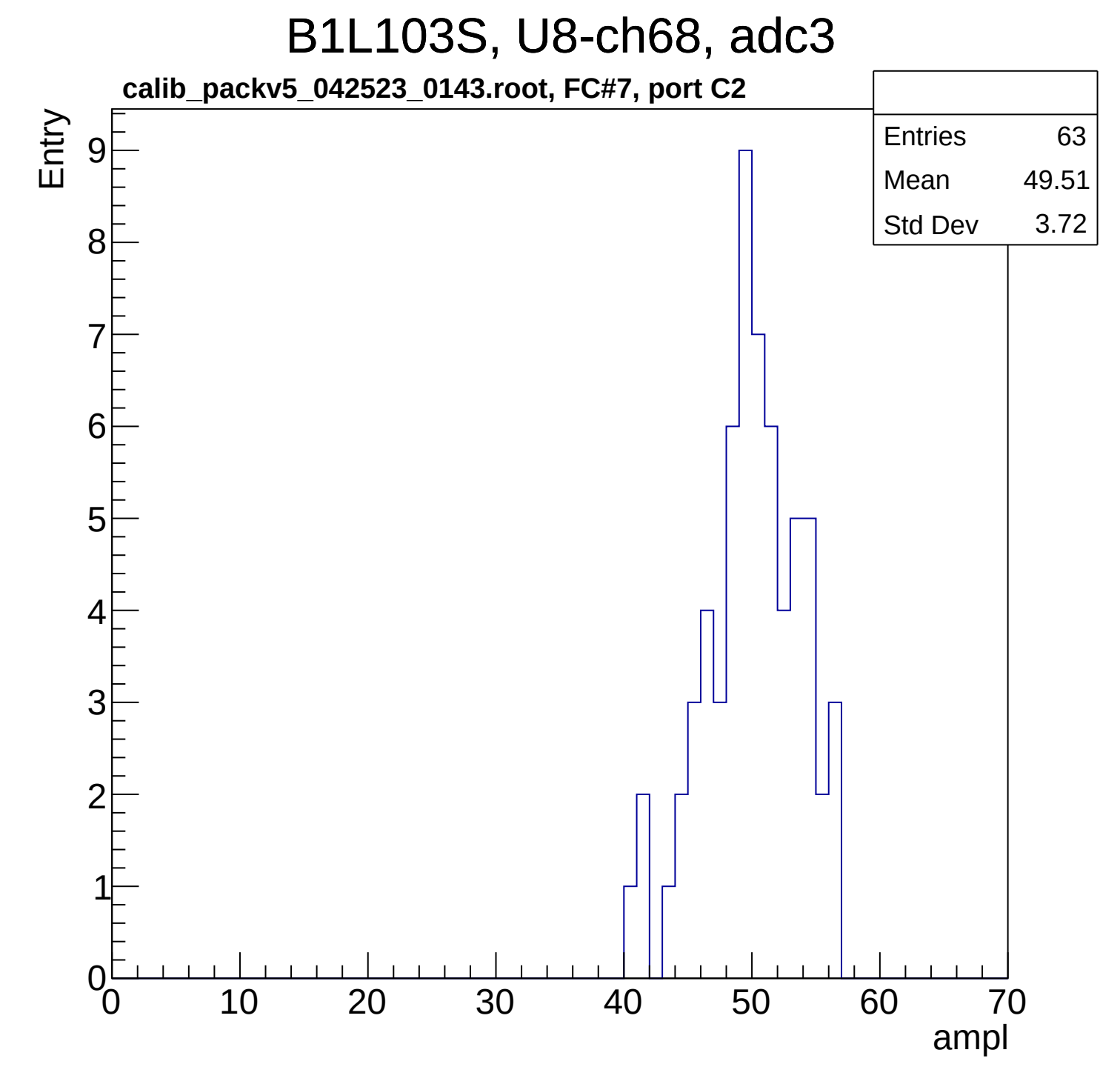

B1L103S, U8-ch67, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 12
Mean 61.92
Std Dev 1.115
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

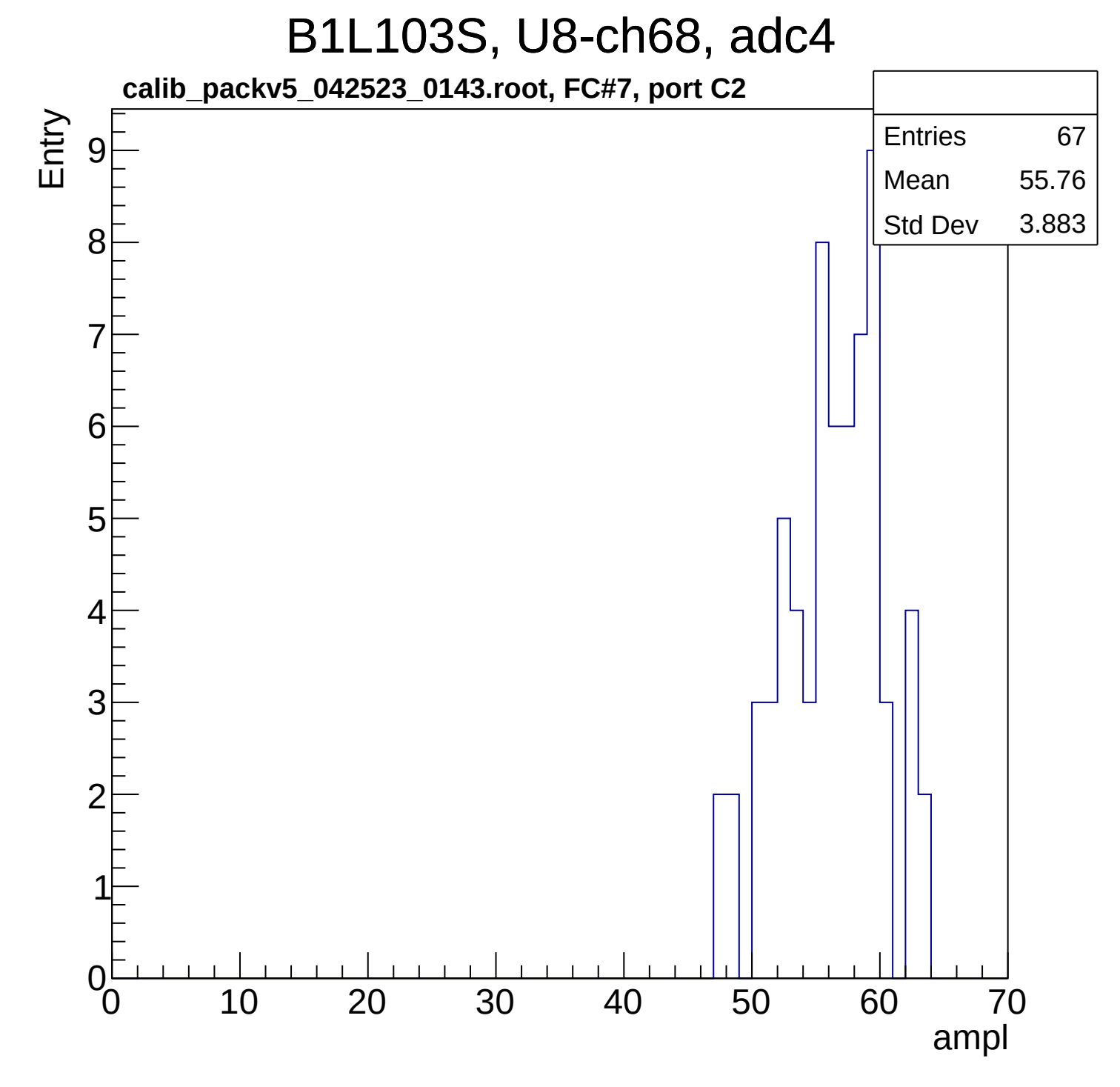

B1L103S, U8-ch67, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

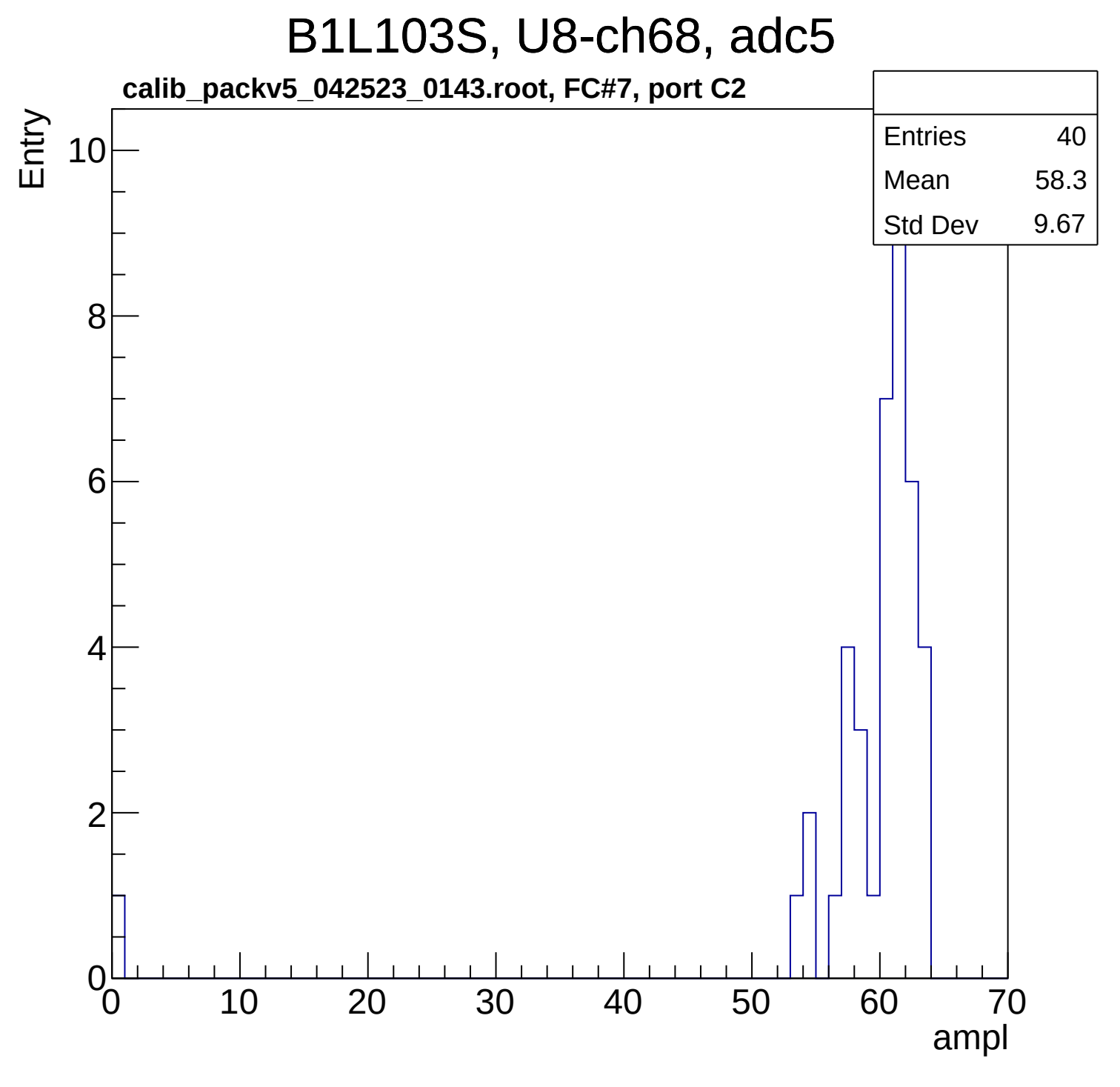

B1L103S, U8-ch68, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 30.21
Std Dev 3.432
Gaus mean : 30.4826
Gaus Width: 3.3631
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

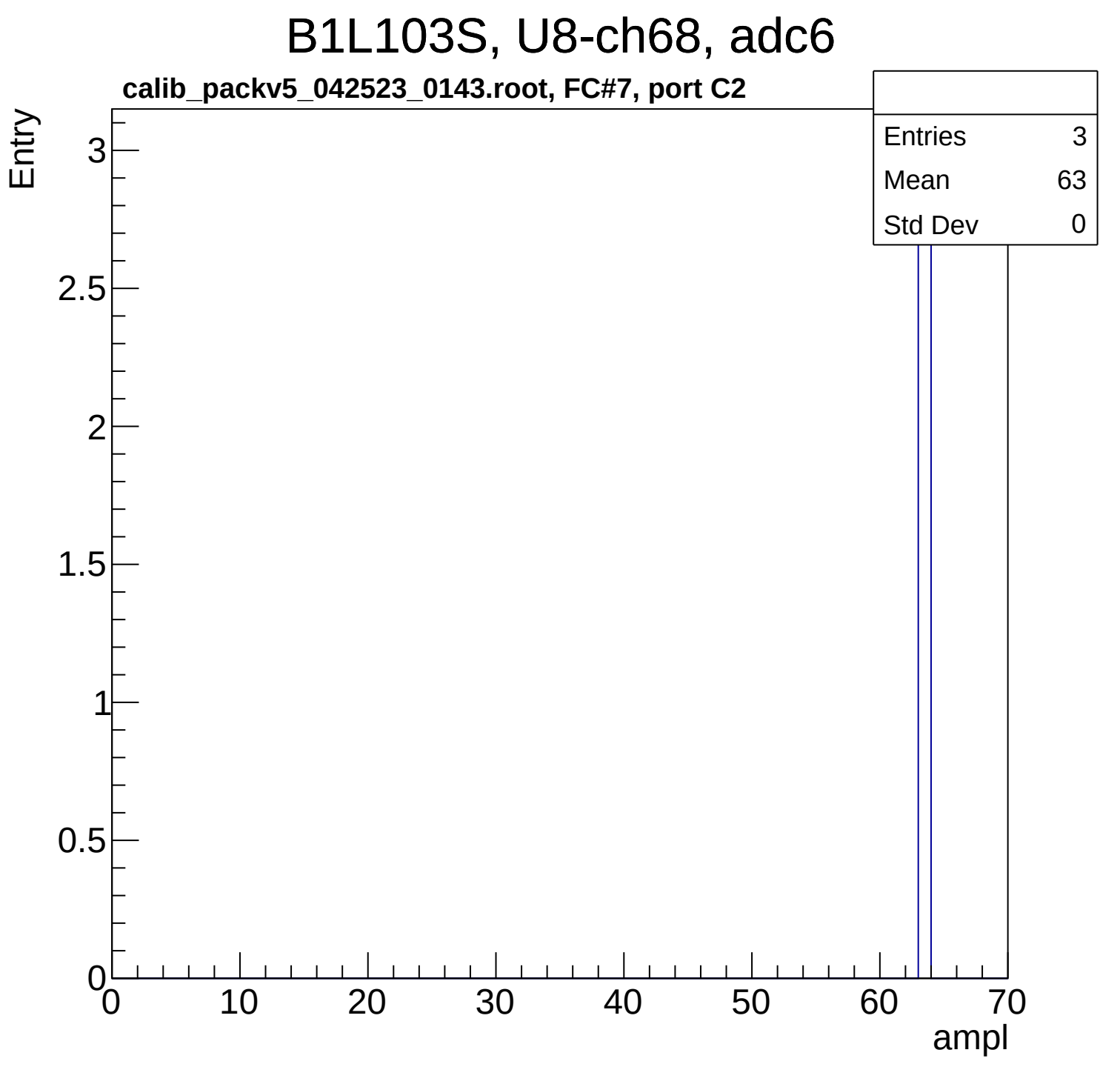

B1L103S, U8-ch68, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 36.12
Std Dev 3.829
Gaus mean : 36.6595
Gaus Width: 4.3589
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

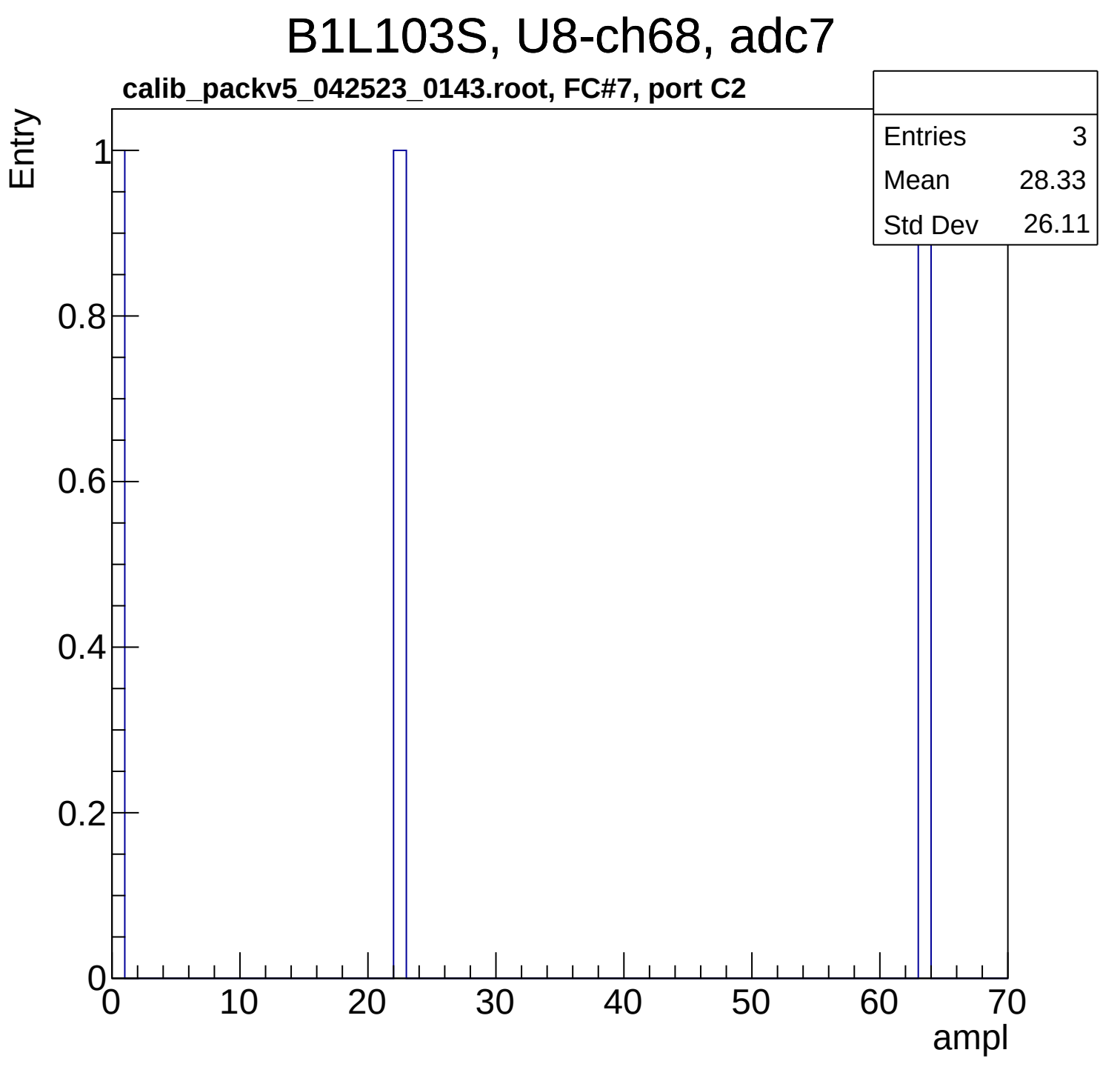

B1L103S, U8-ch68, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 43.19
Std Dev 3.386
Gaus mean : 43.9087
Gaus Width: 3.4506
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

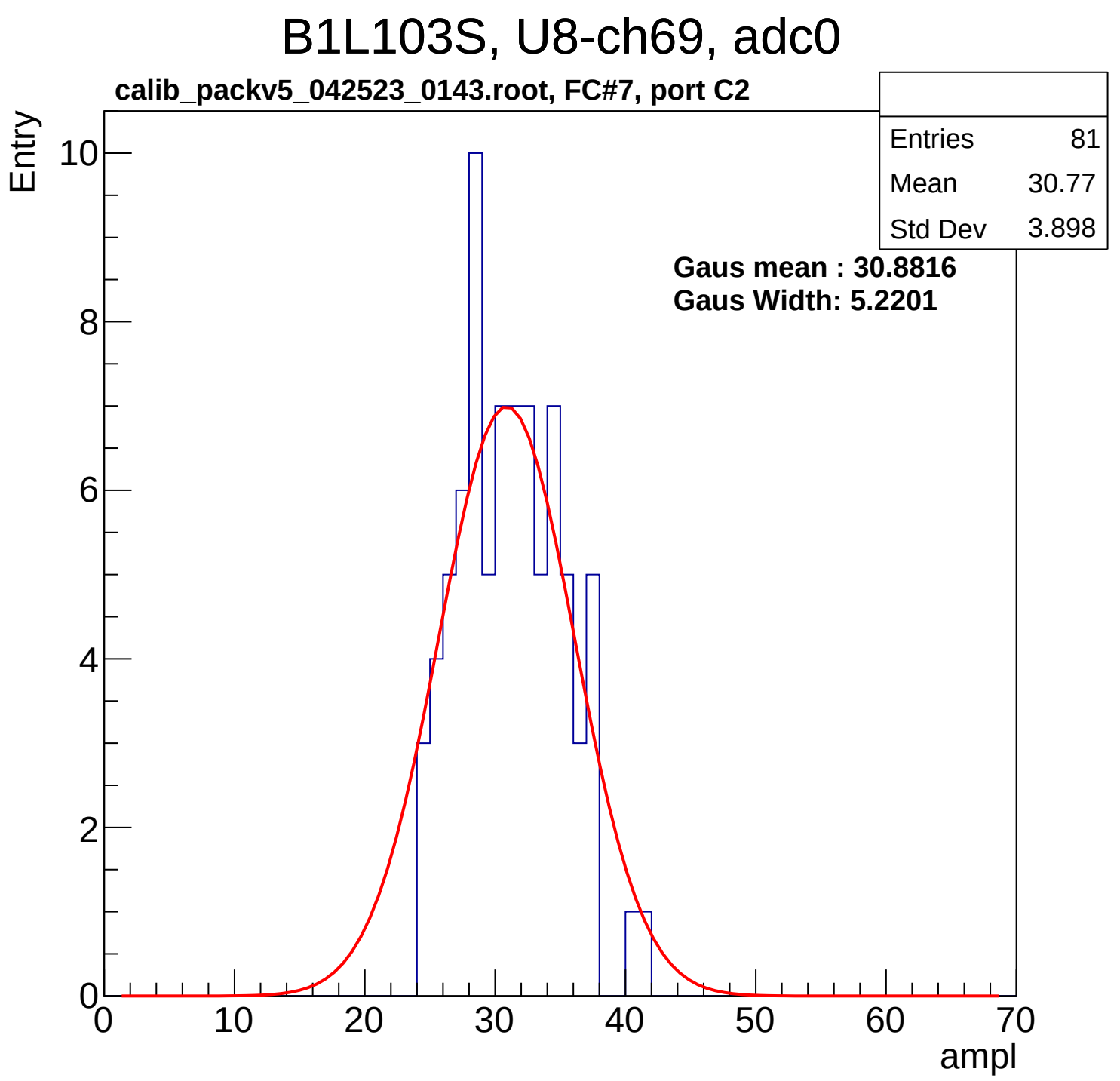

B1L103S, U8-ch68, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 49.51
Std Dev 3.72
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

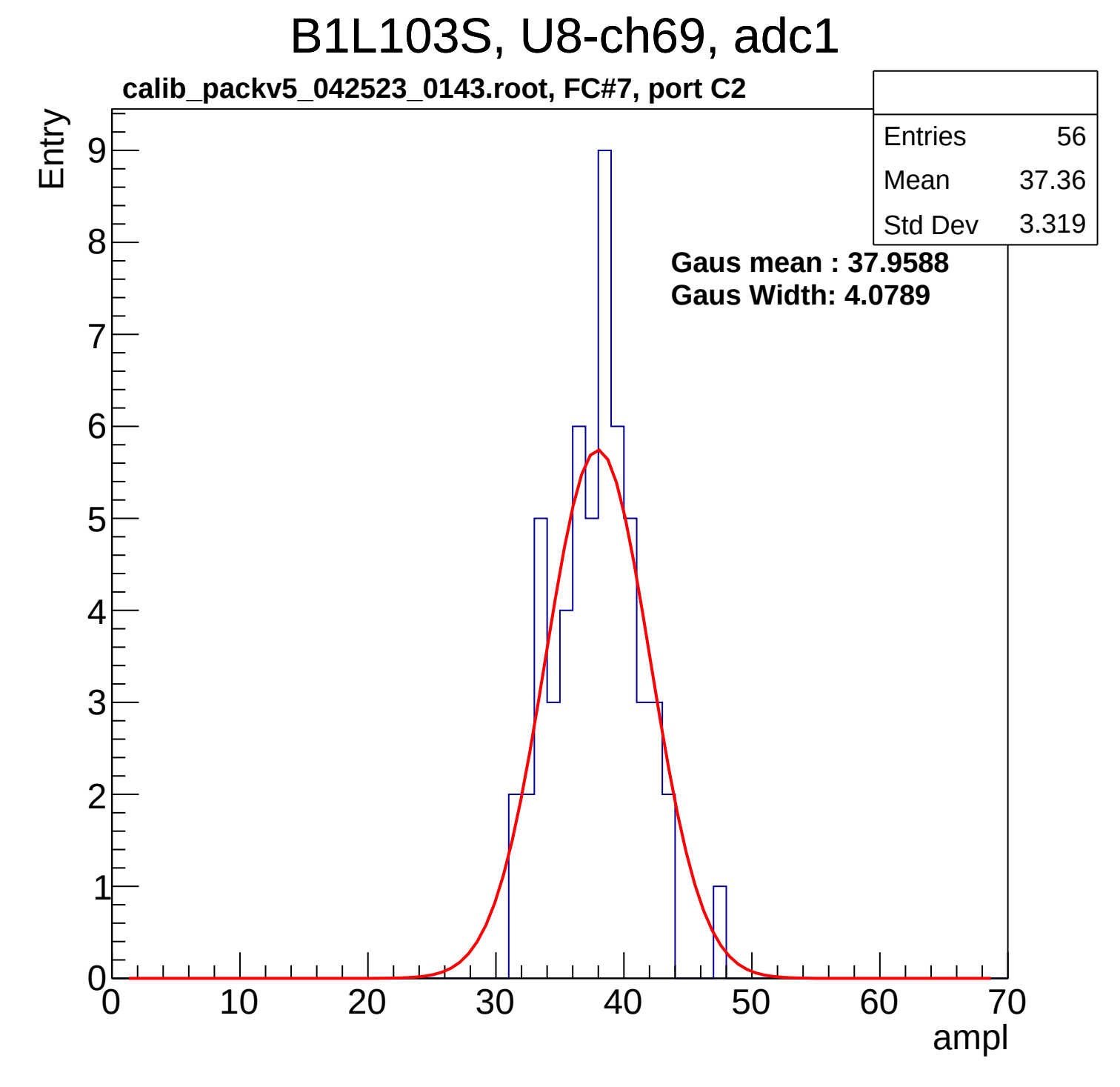

B1L103S, U8-ch68, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 55.76
Std Dev 3.883
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

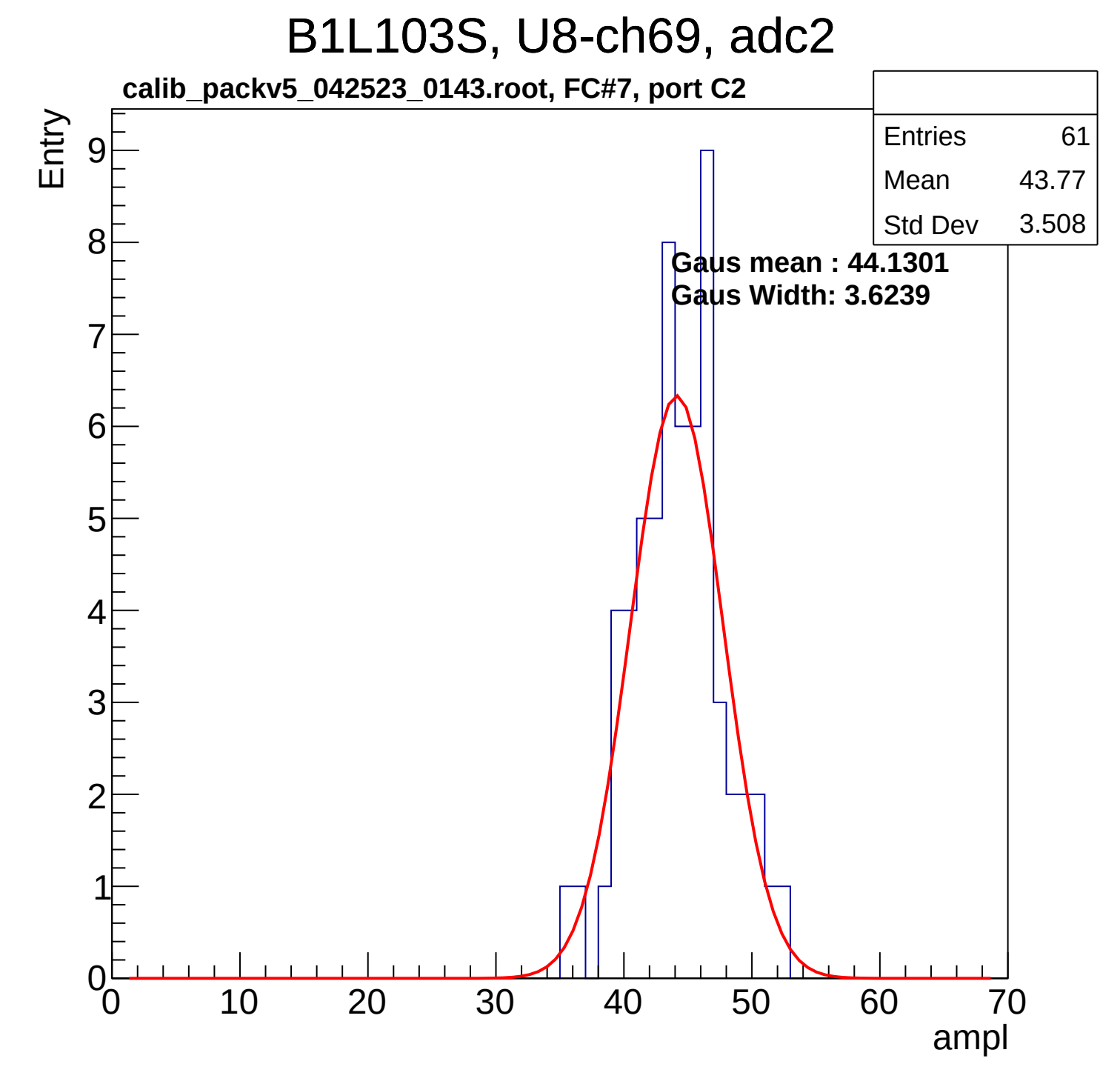

B1L103S, U8-ch68, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 40
Mean 58.3
Std Dev 9.67
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

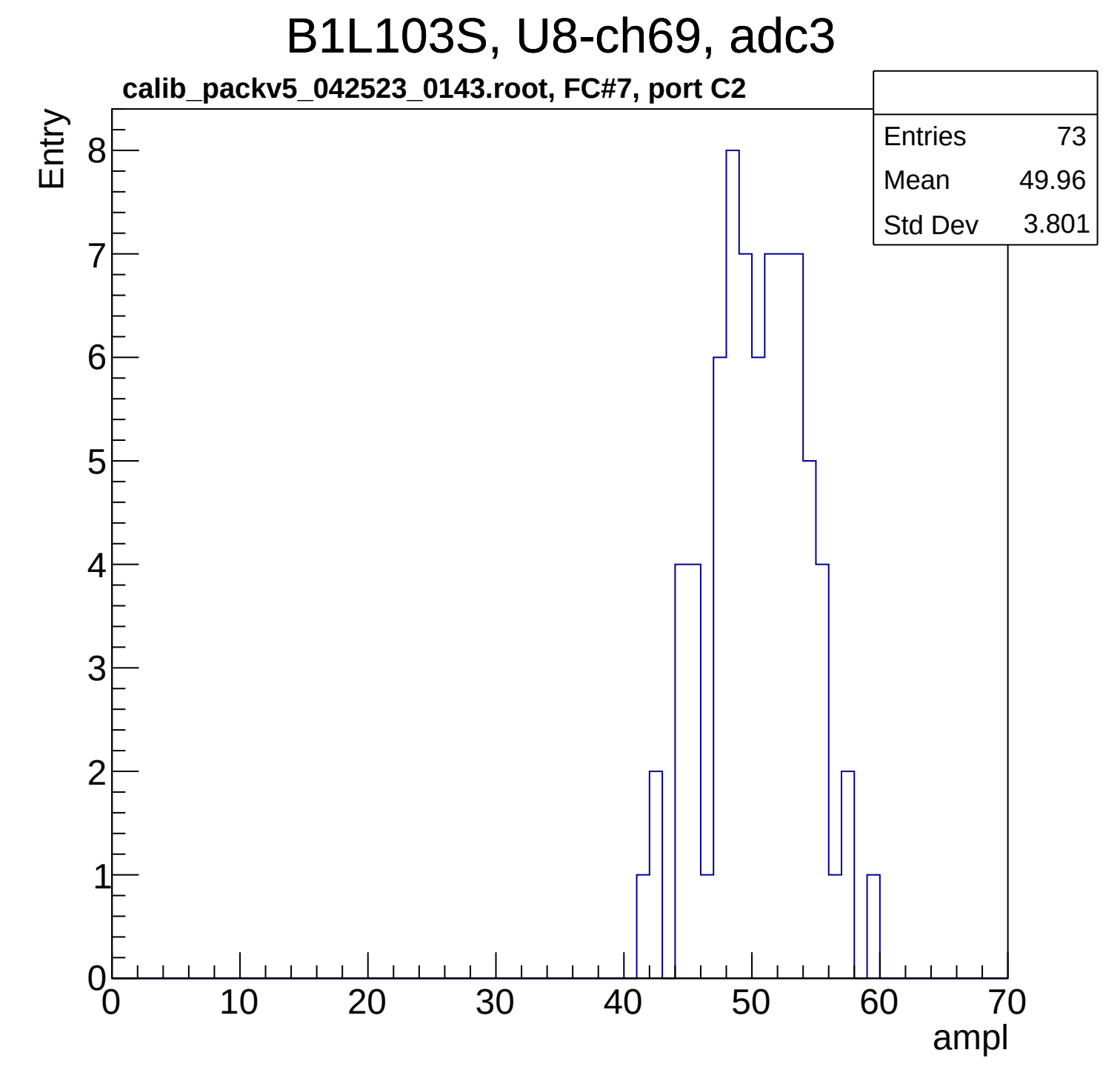

B1L103S, U8-ch68, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 63
Std Dev 0
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

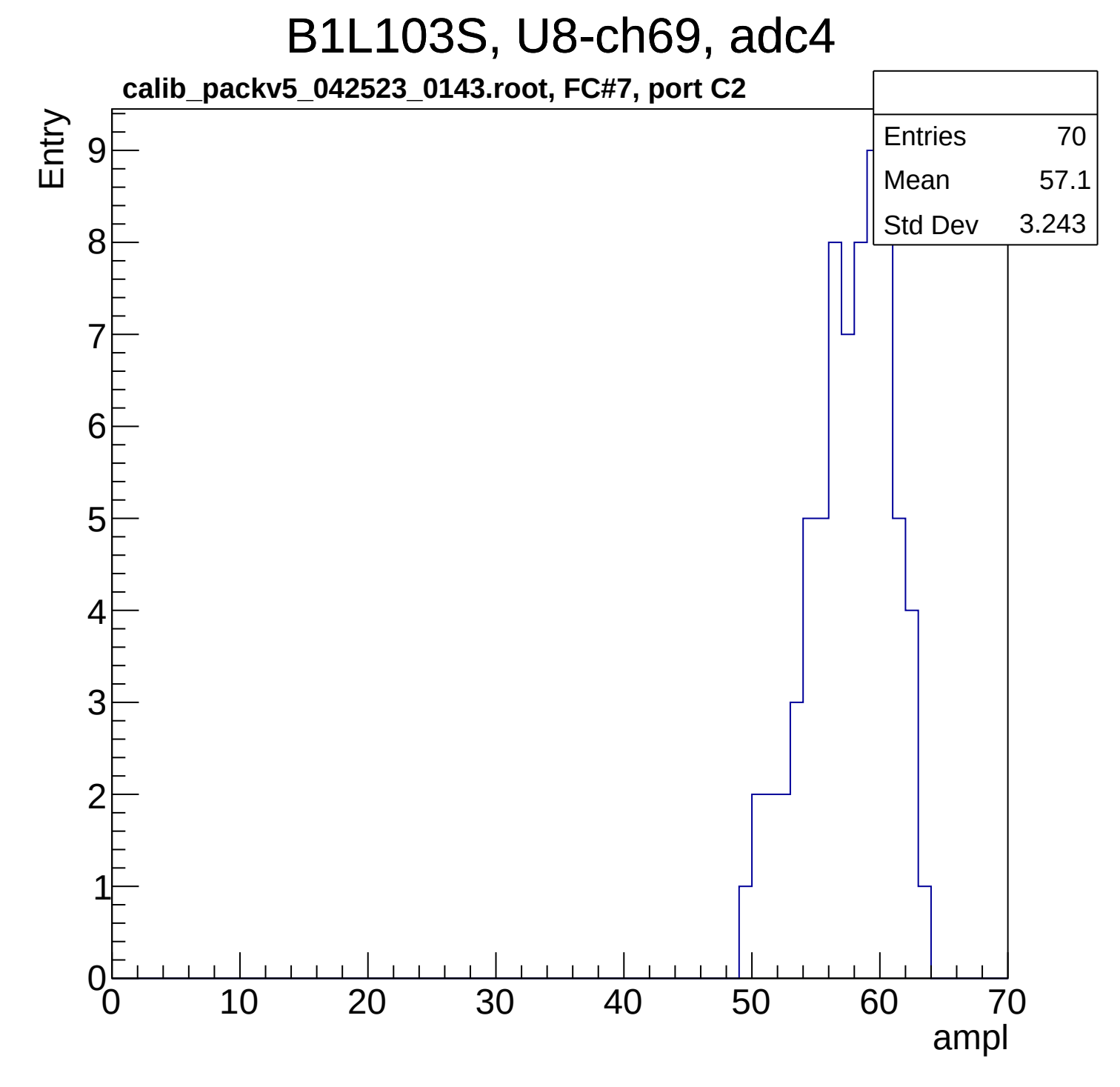

B1L103S, U8-ch68, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 28.33
Std Dev 26.11
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

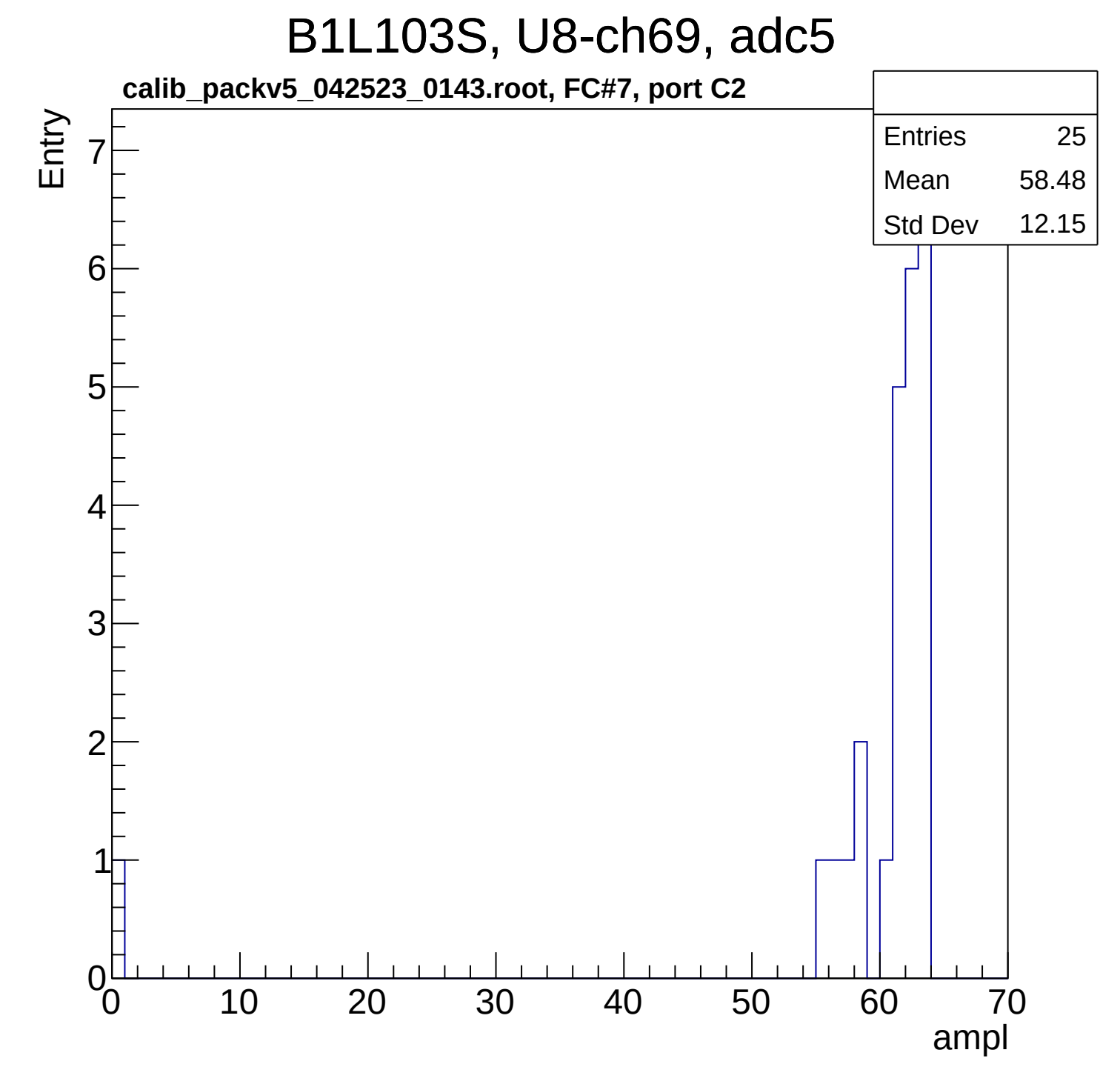

B1L103S, U8-ch69, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 81
Mean 30.77
Std Dev 3.898
Gaus mean : 30.8816
Gaus Width: 5.2201
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

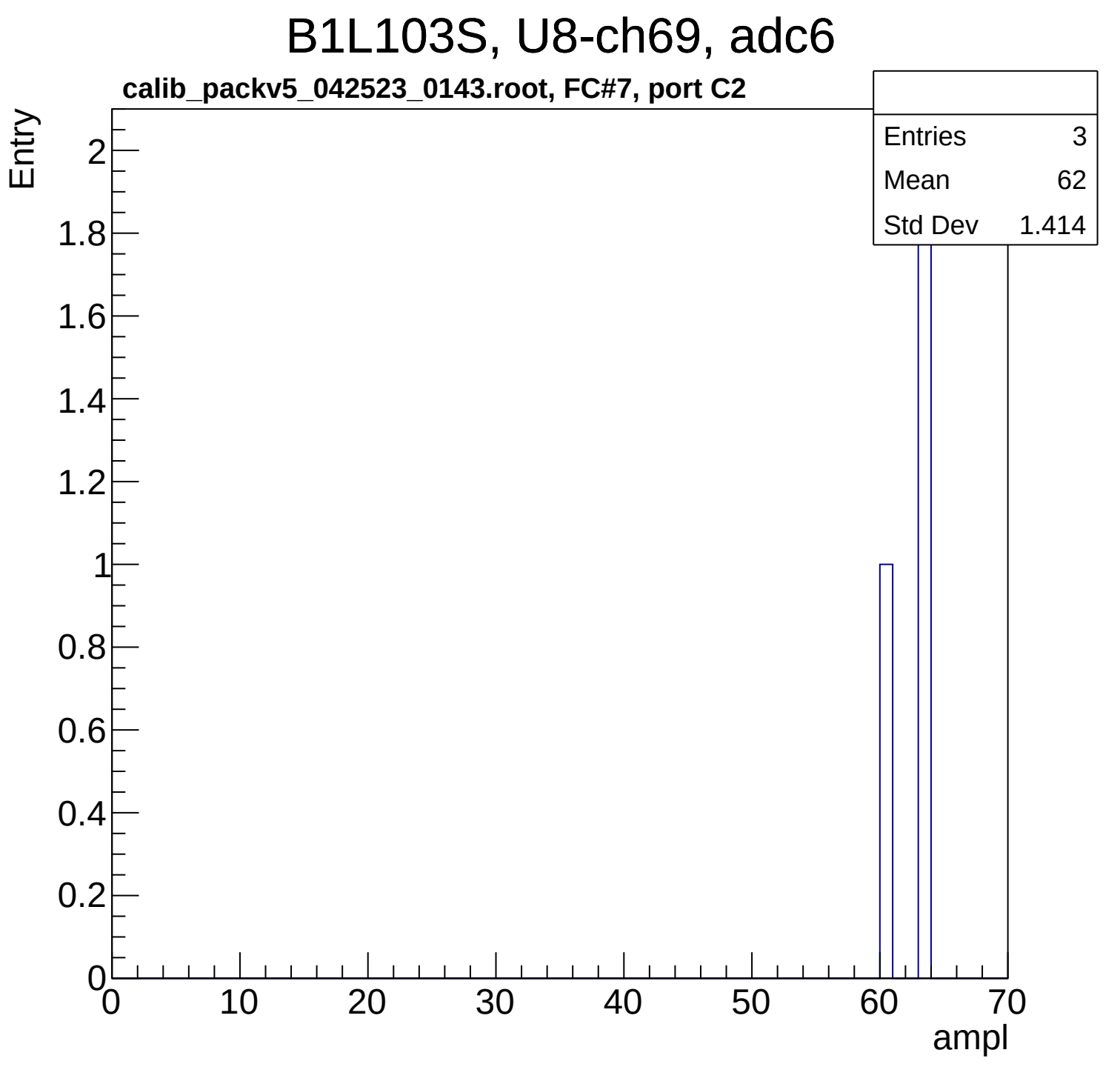

B1L103S, U8-ch69, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 37.36
Std Dev 3.319
Gaus mean : 37.9588
Gaus Width: 4.0789
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

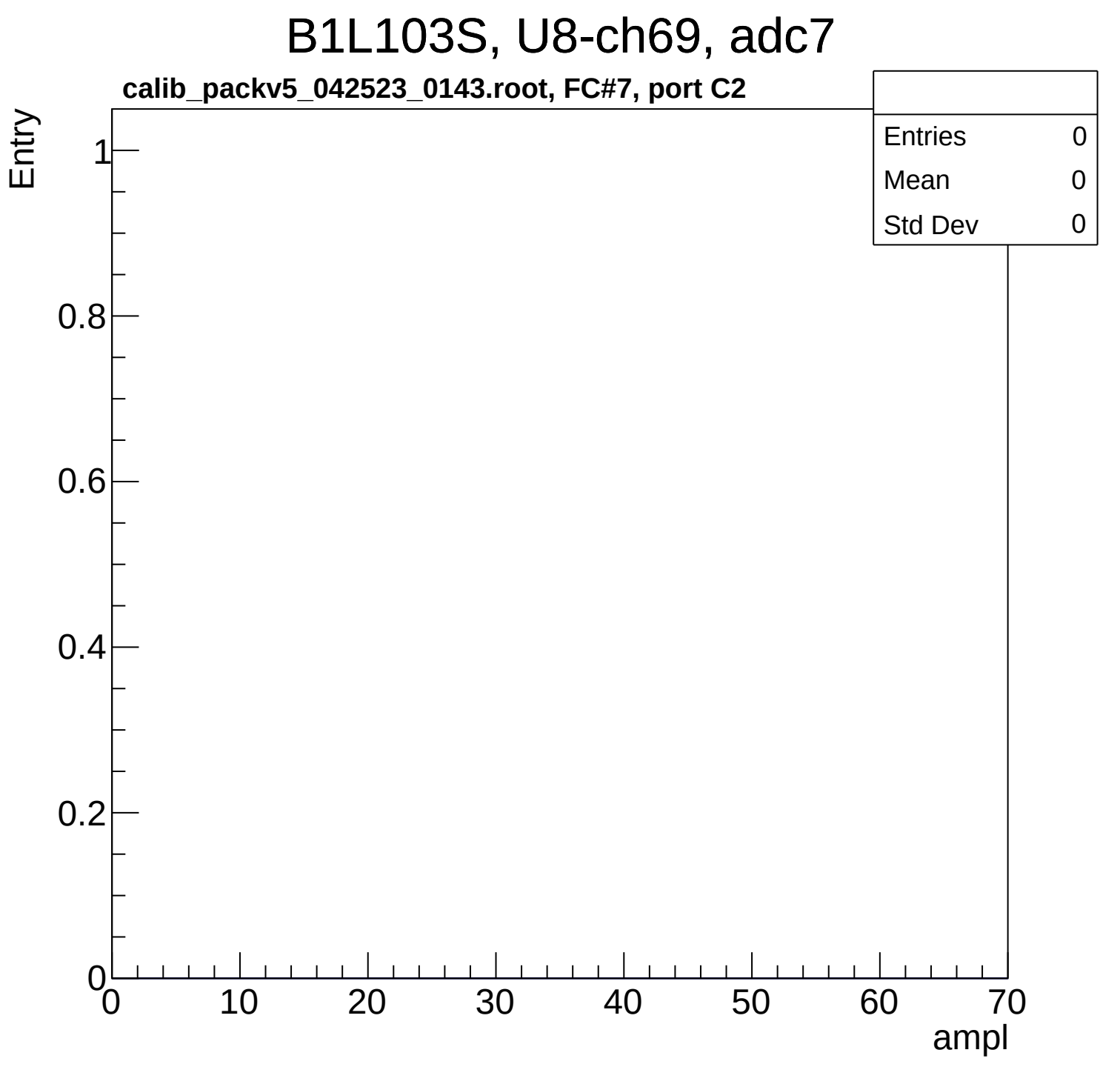

B1L103S, U8-ch69, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 43.77
Std Dev 3.508
Gaus mean : 44.1301
Gaus Width: 3.6239
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

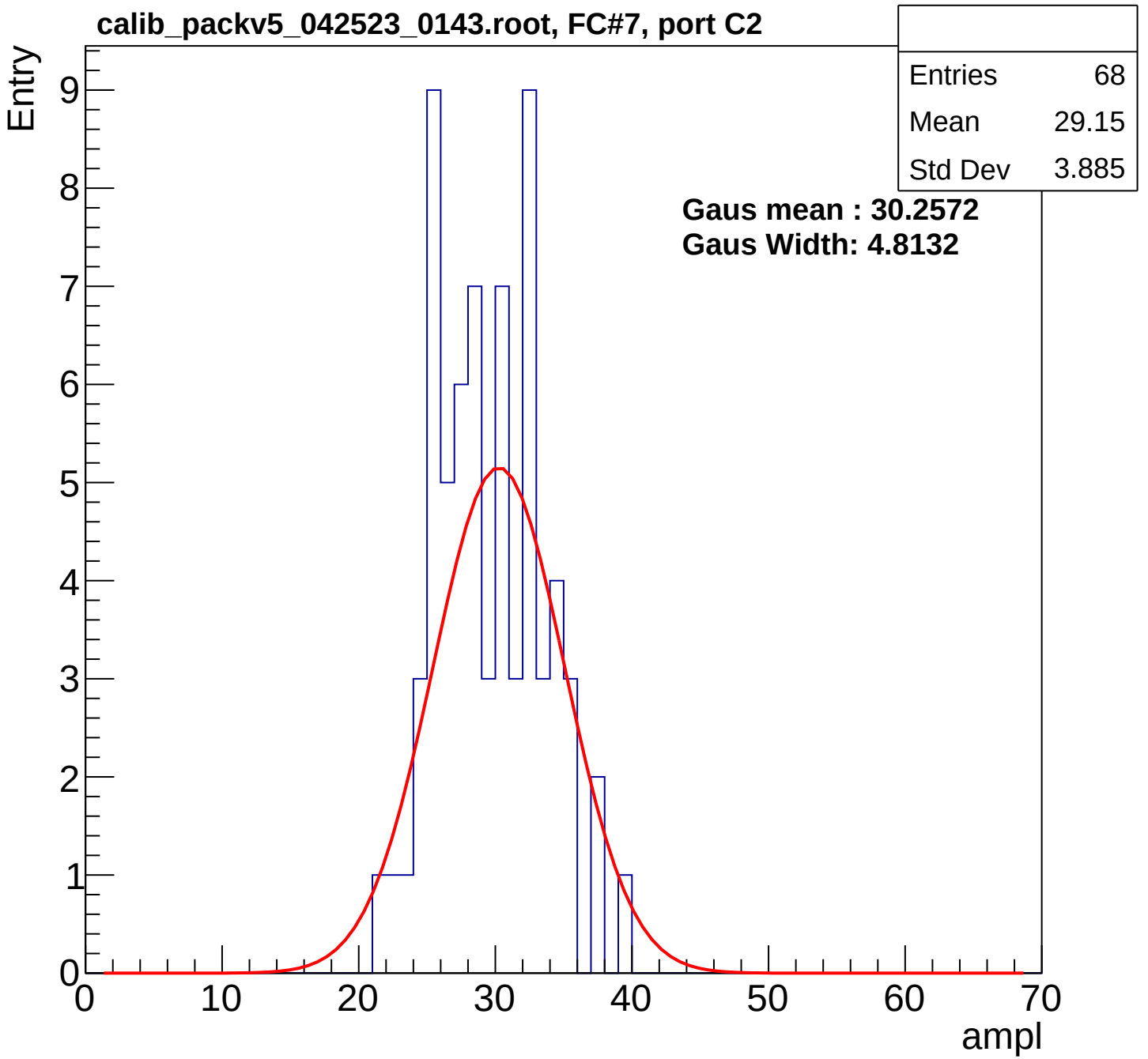

B1L103S, U8-ch69, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 49.96
Std Dev 3.801
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

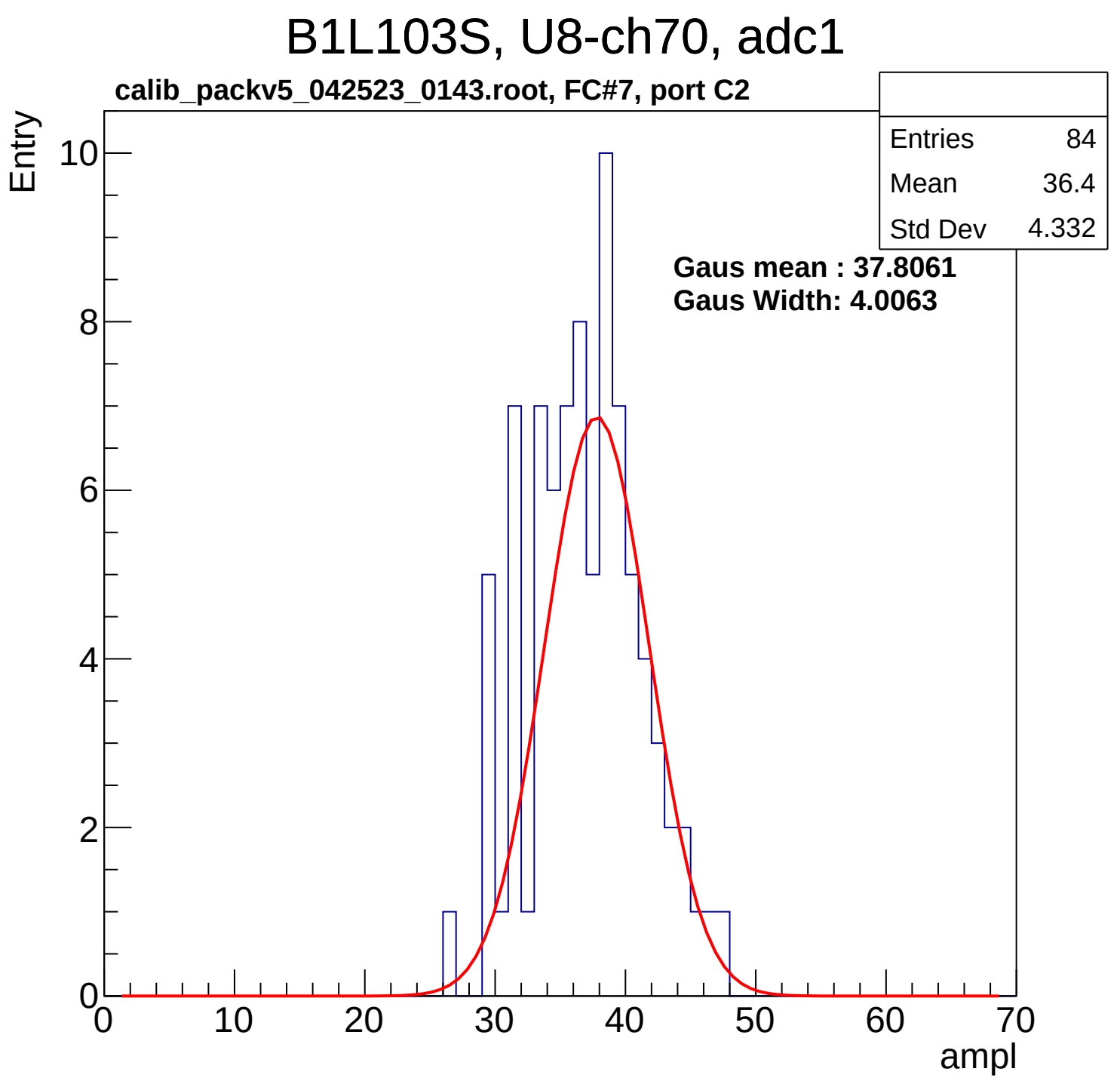

B1L103S, U8-ch69, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 57.1
Std Dev 3.243
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

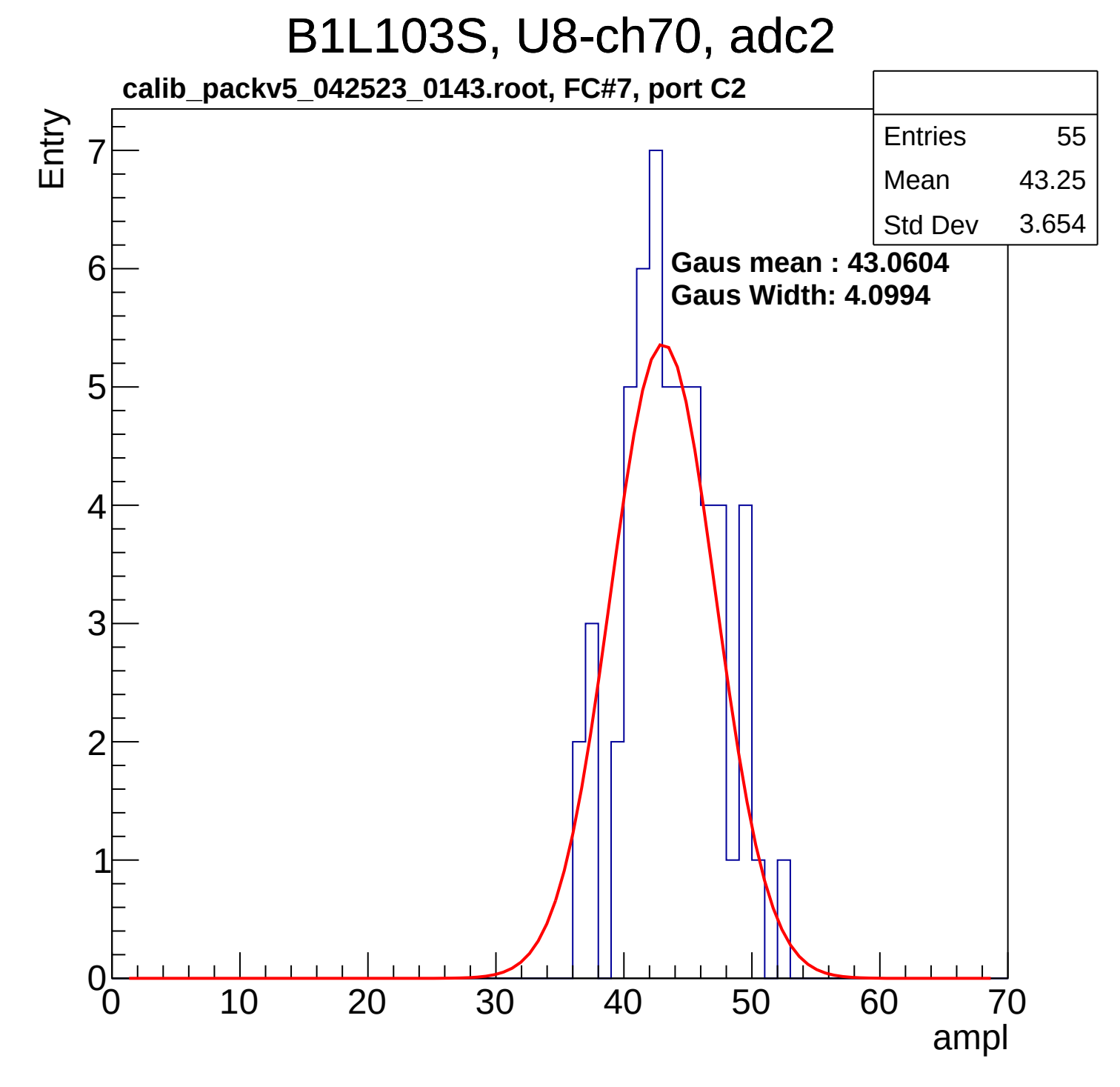

B1L103S, U8-ch69, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 25
Mean 58.48
Std Dev 12.15
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

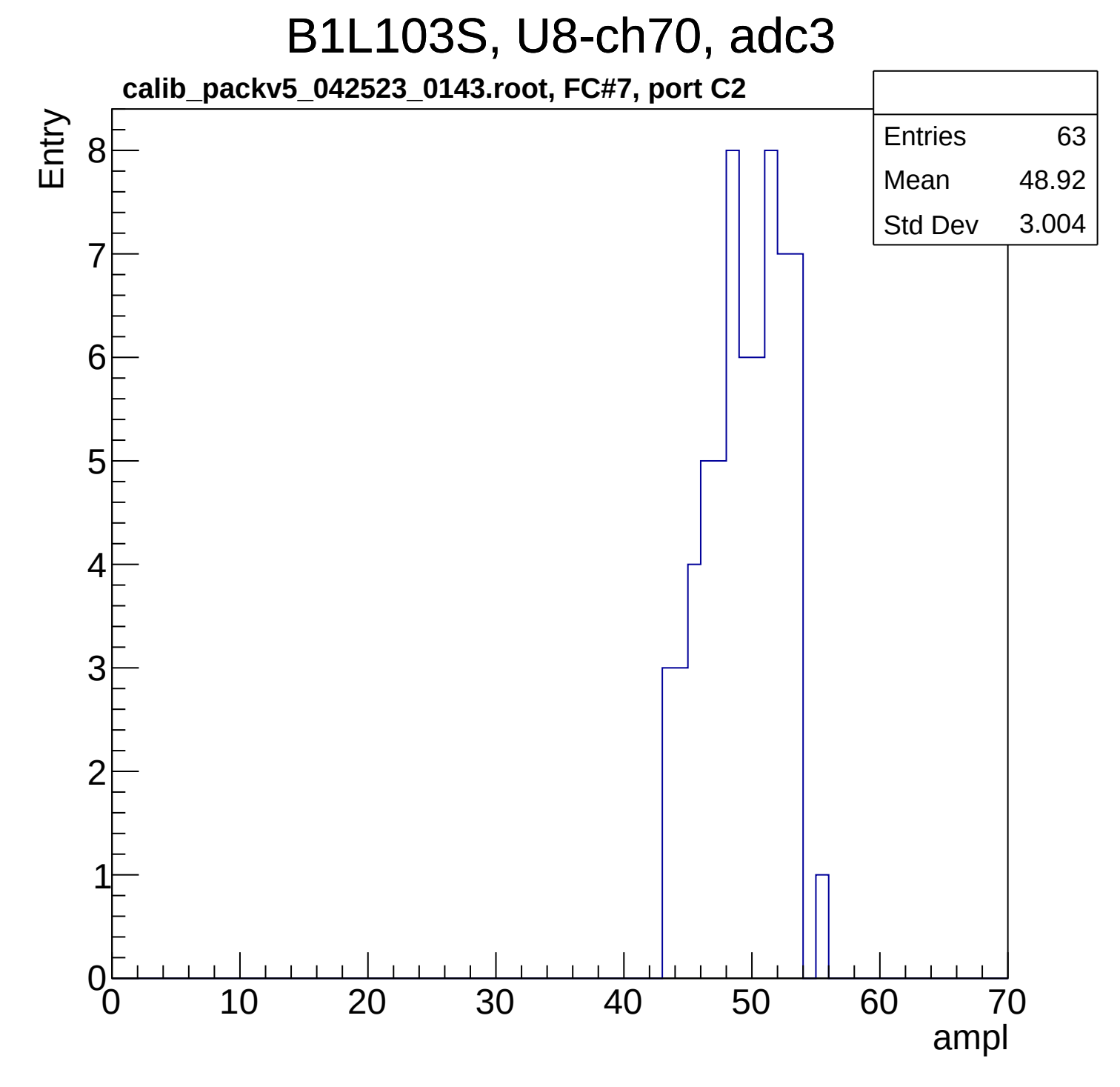

B1L103S, U8-ch69, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 62
Std Dev 1.414
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

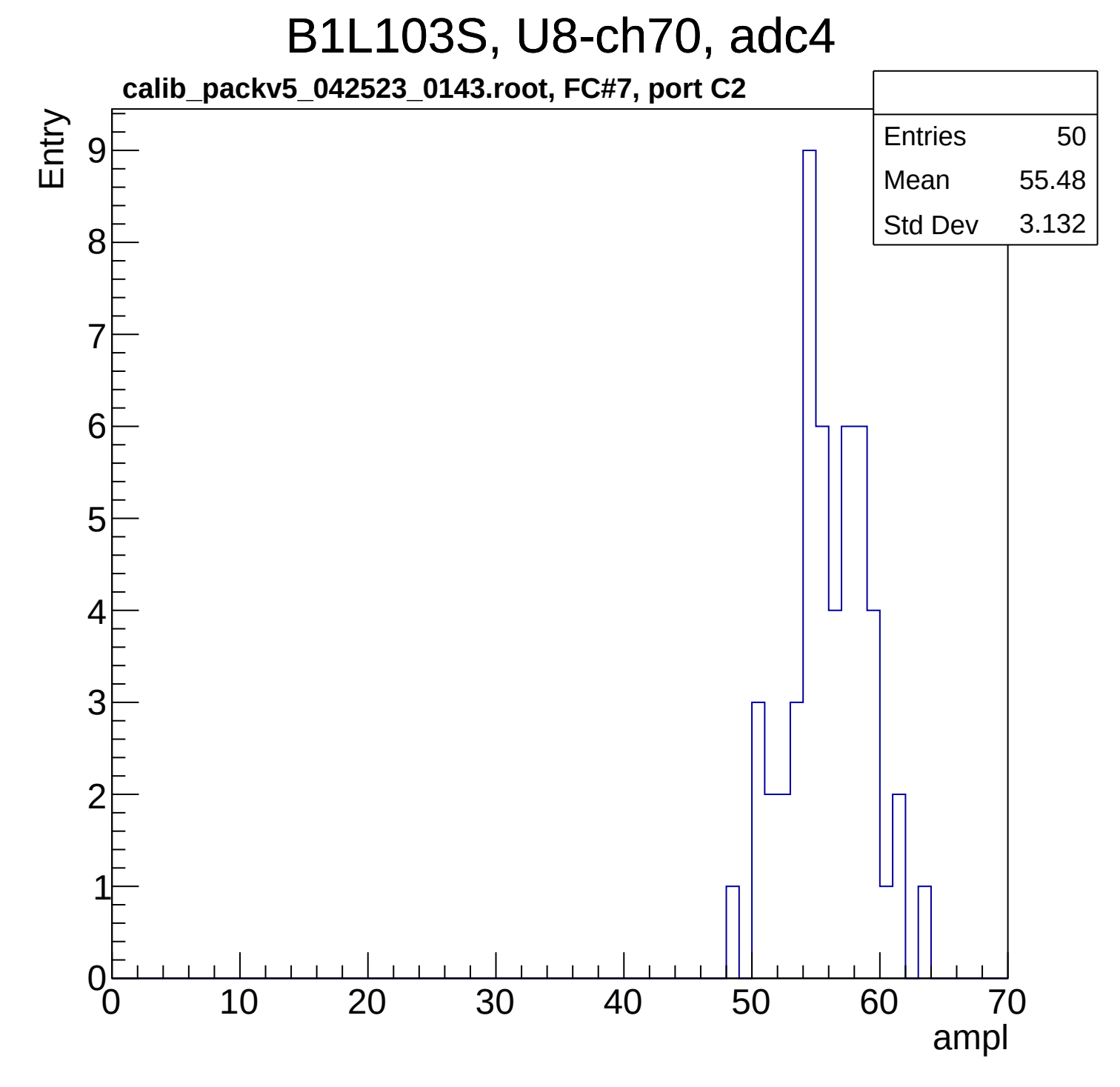

B1L103S, U8-ch69, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

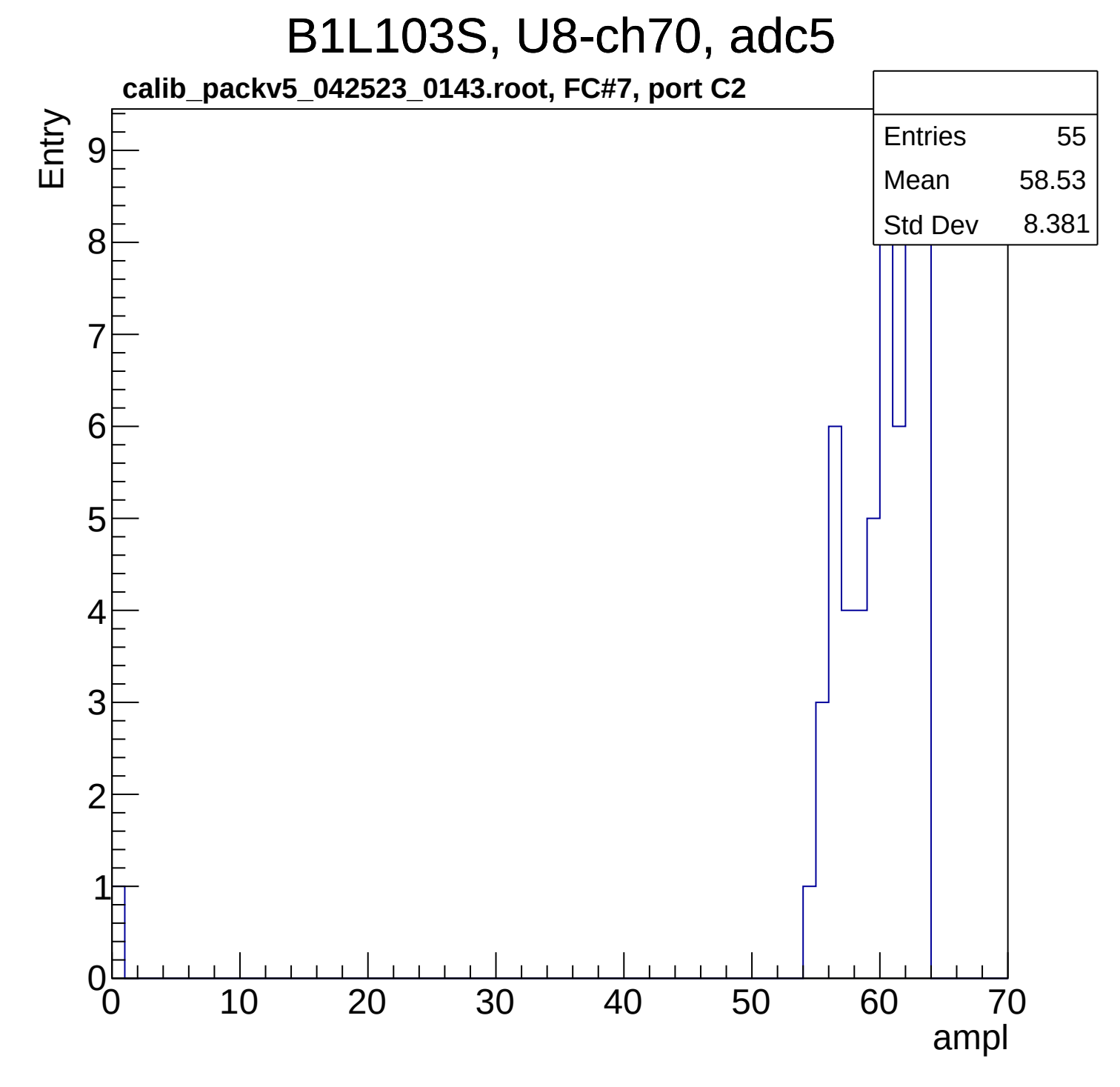

B1L103S, U8-ch70, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 29.15
Std Dev 3.885
Gaus mean : 30.2572
Gaus Width: 4.8132
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

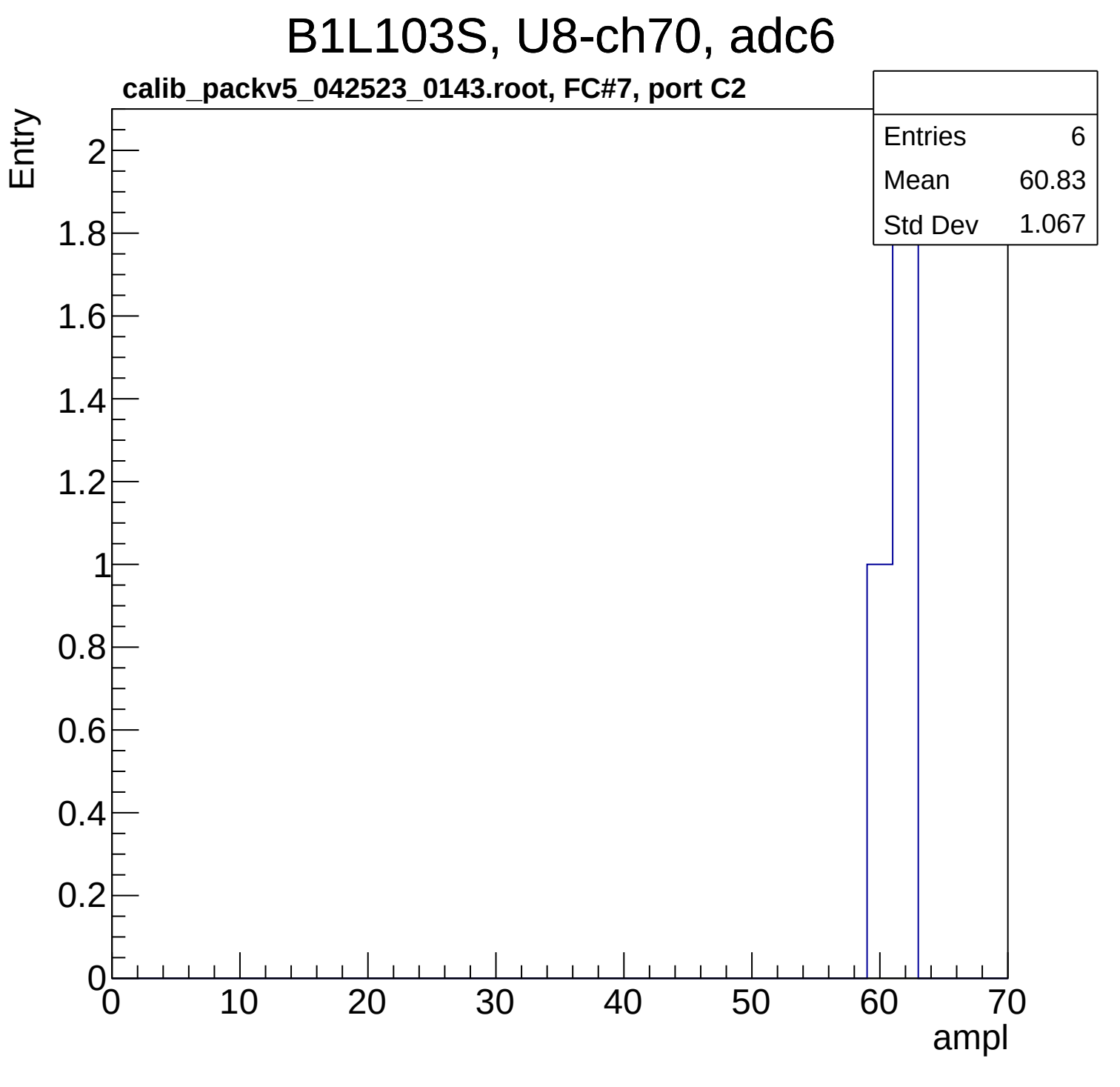

B1L103S, U8-ch70, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 84
Mean 36.4
Std Dev 4.332
Gaus mean : 37.8061
Gaus Width: 4.0063
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

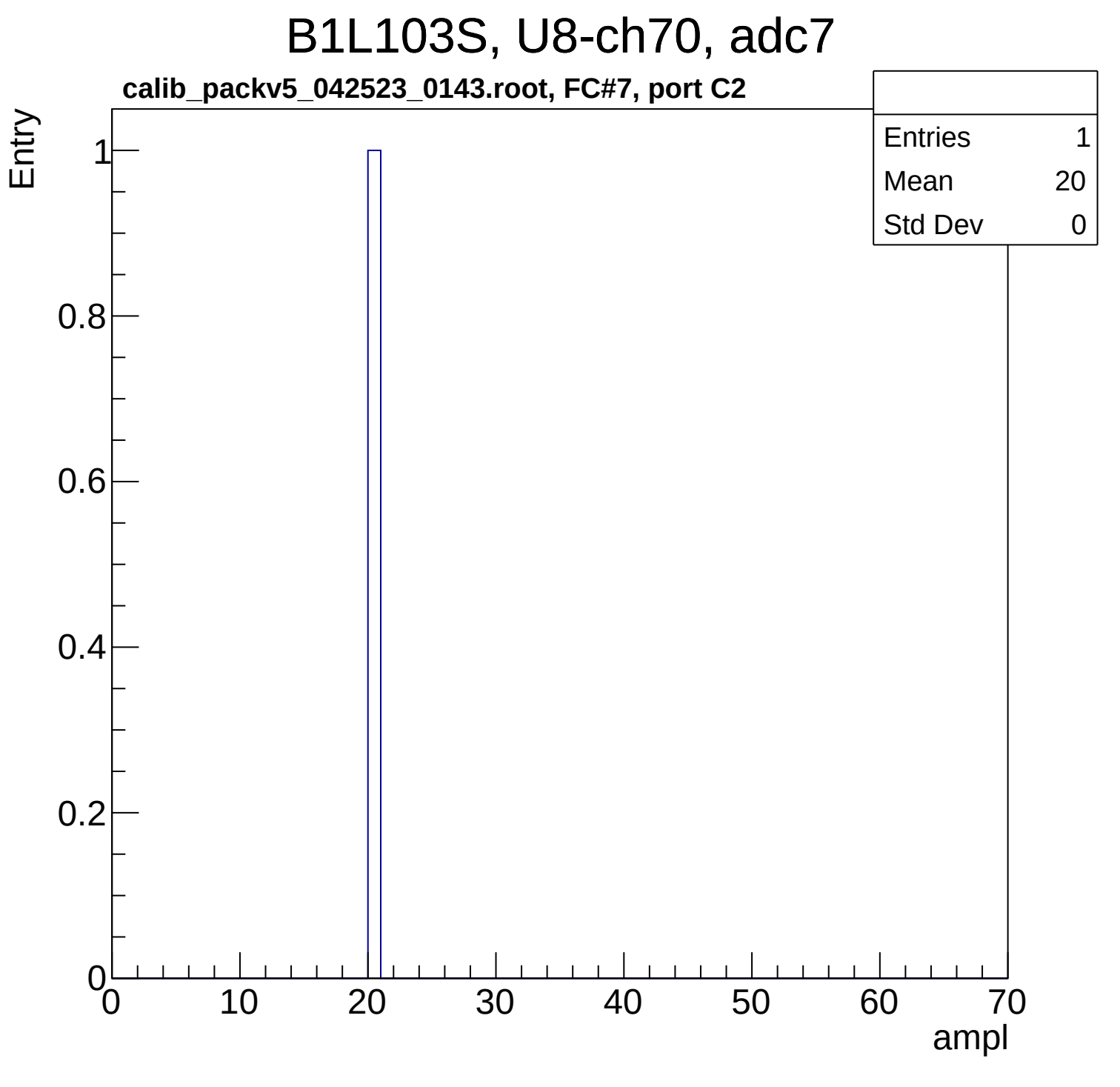

B1L103S, U8-ch70, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 43.25
Std Dev 3.654
Gaus mean : 43.0604
Gaus Width: 4.0994
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

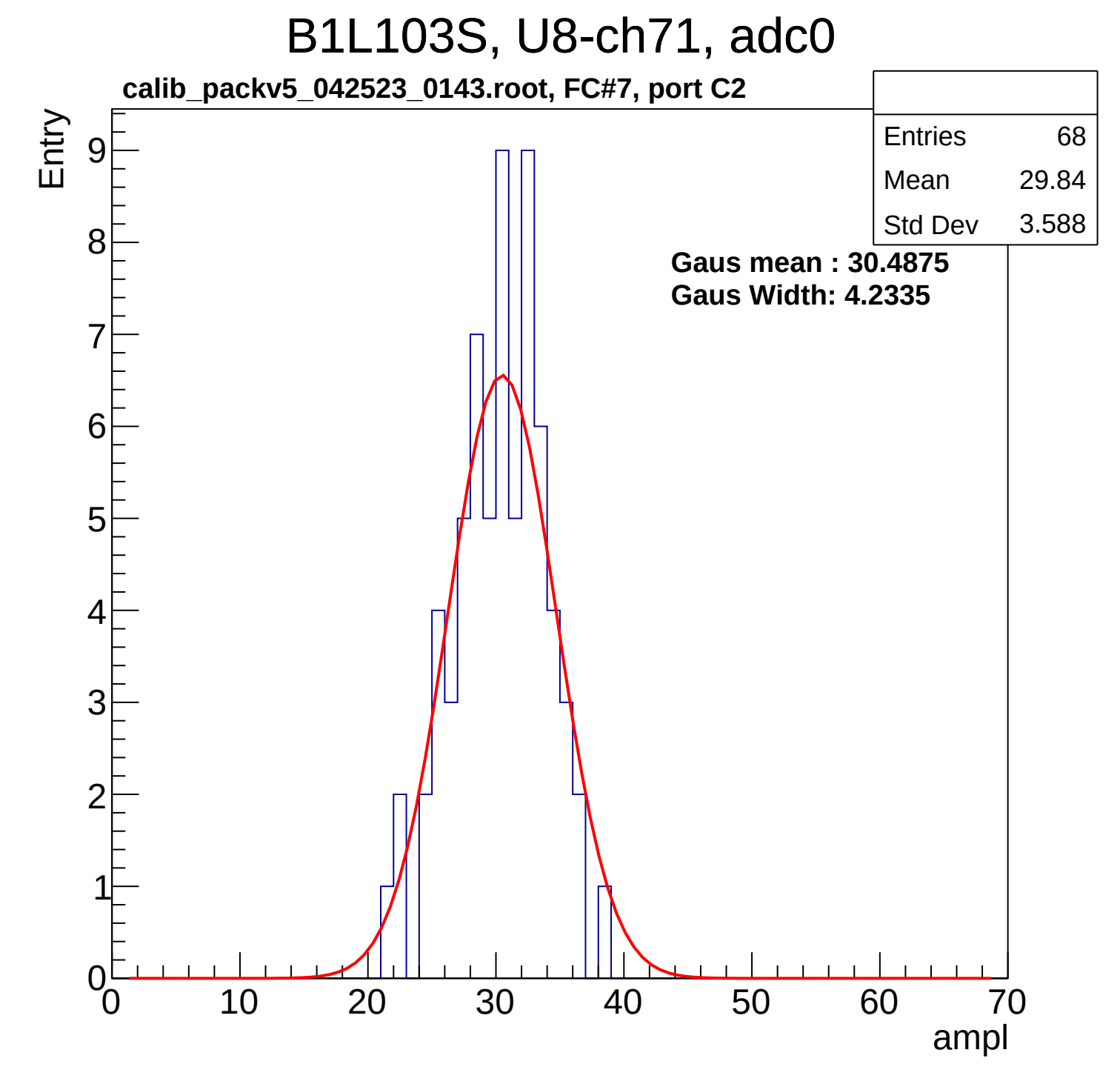

B1L103S, U8-ch70, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 48.92
Std Dev 3.004
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

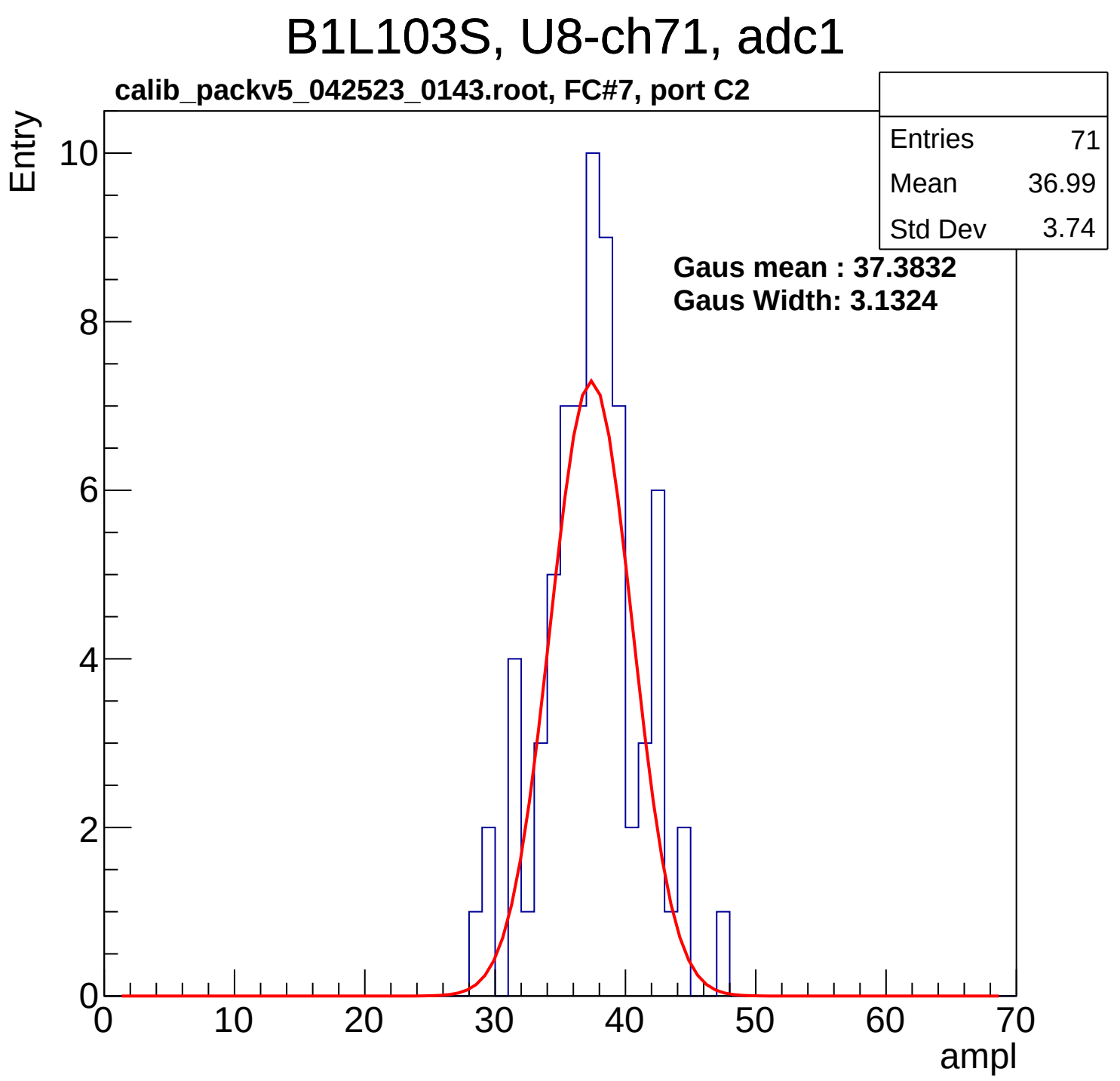

B1L103S, U8-ch70, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 55.48
Std Dev 3.132
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

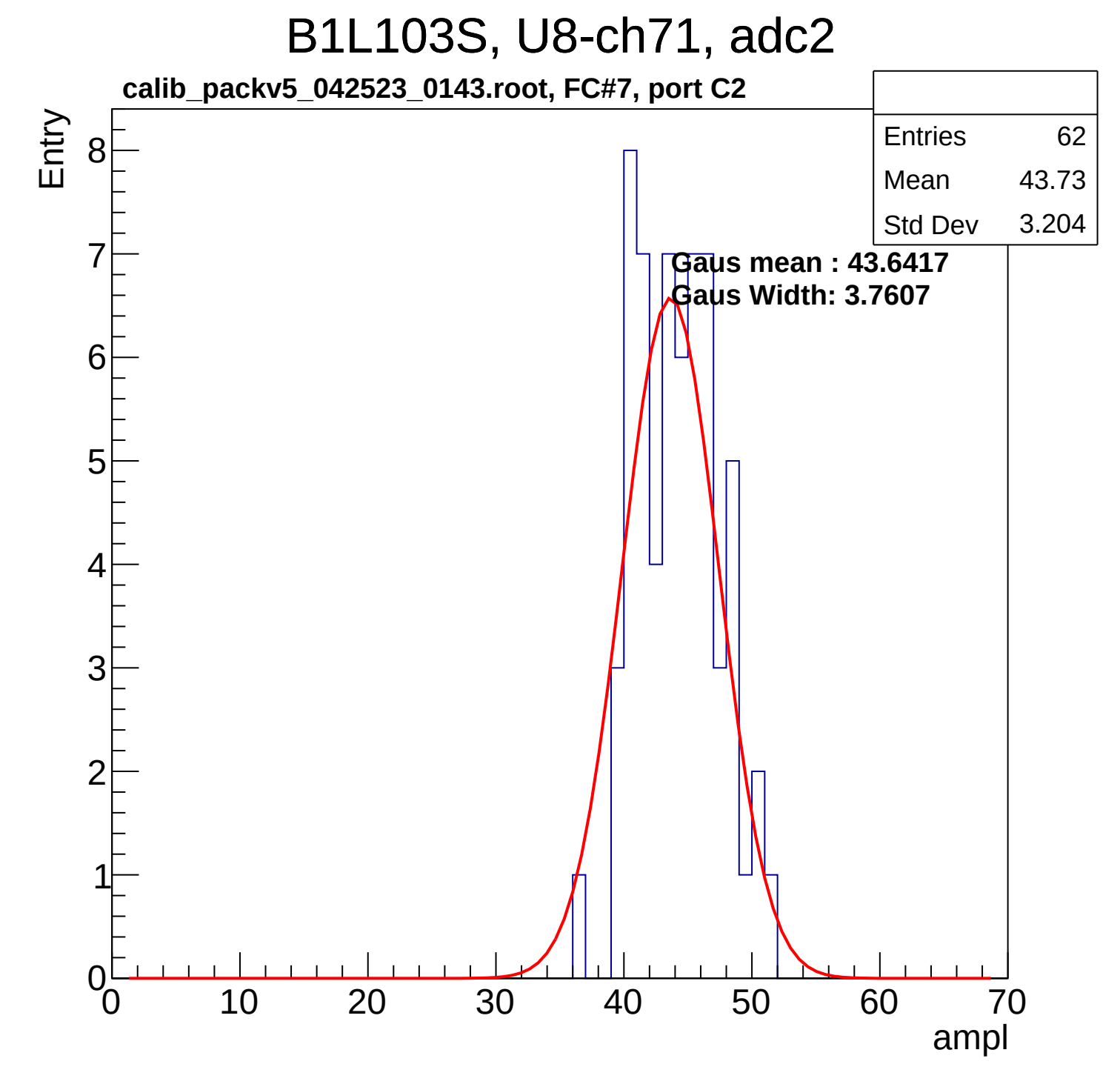

B1L103S, U8-ch70, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 58.53
Std Dev 8.381
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

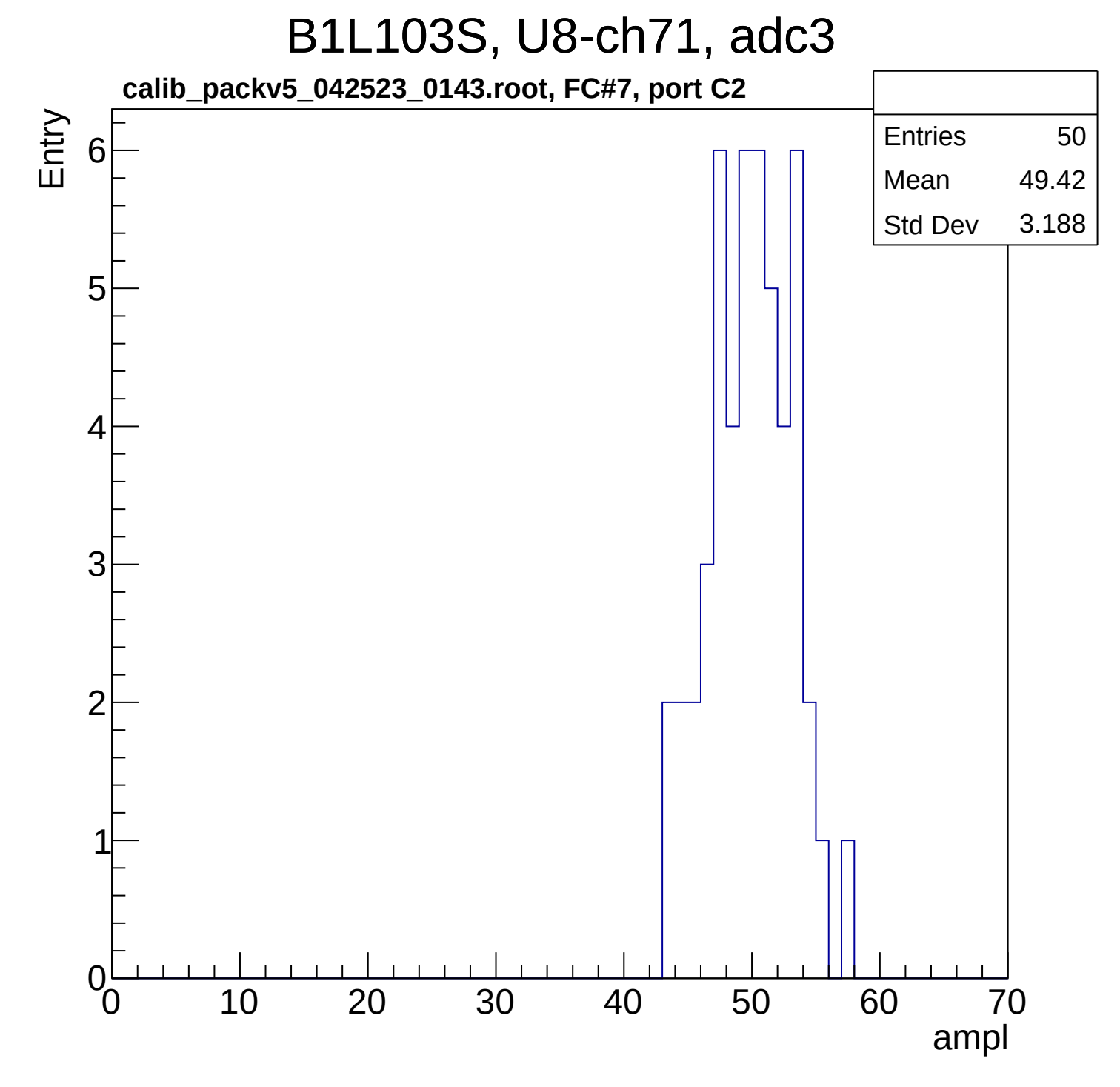

B1L103S, U8-ch70, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 60.83
Std Dev 1.067
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

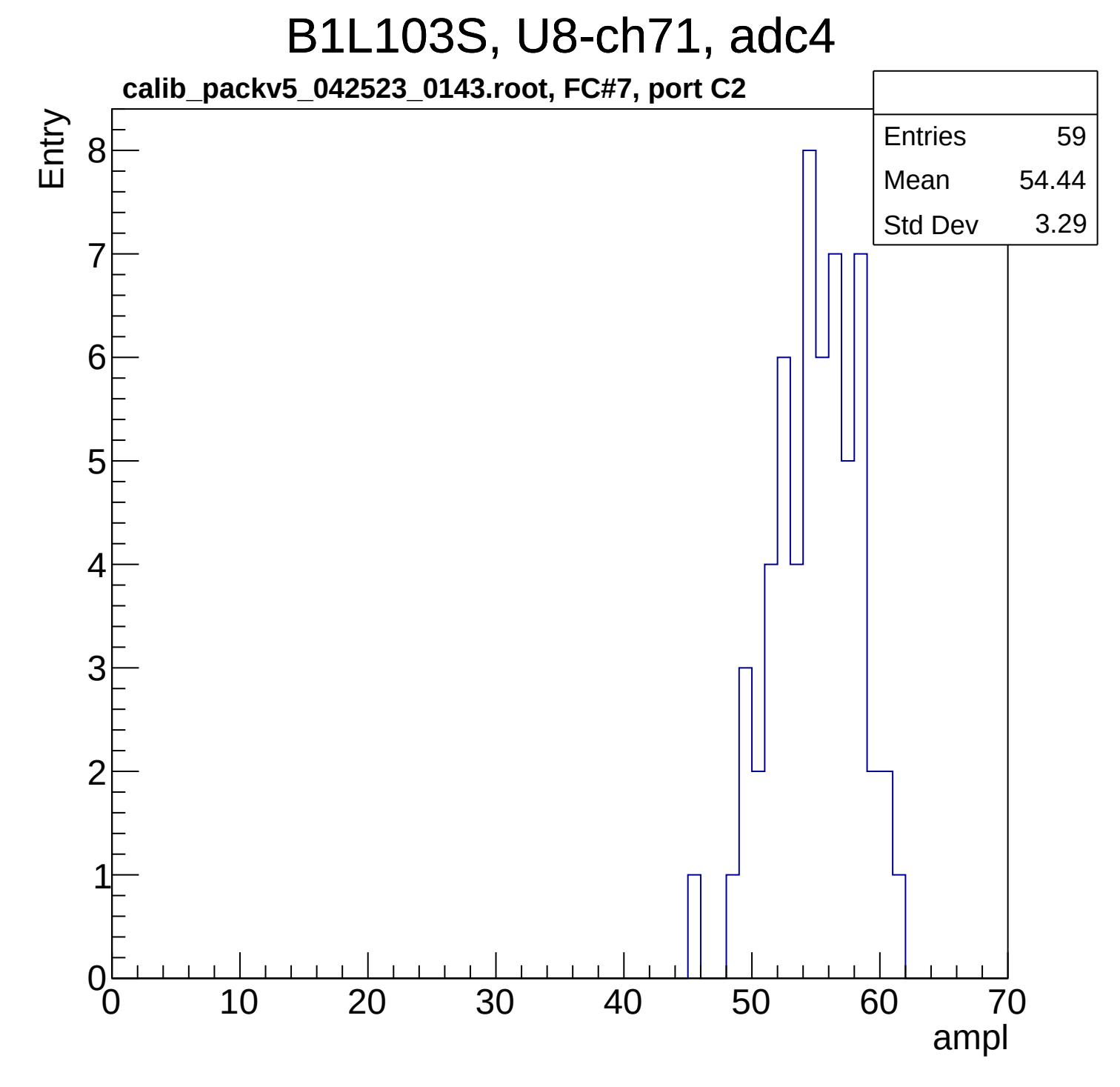

B1L103S, U8-ch70, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 20
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

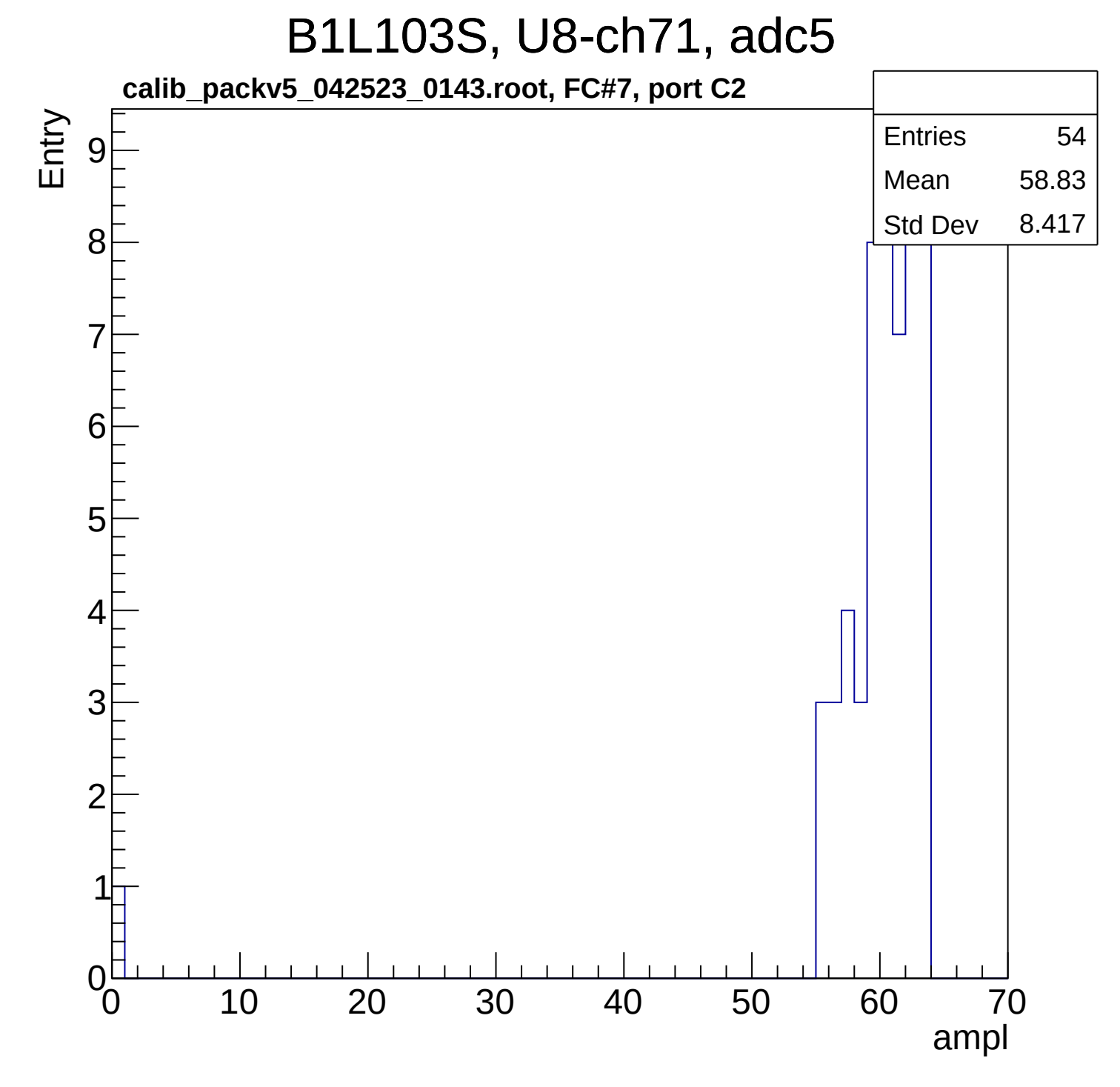

B1L103S, U8-ch71, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 29.84
Std Dev 3.588
Gaus mean : 30.4875
Gaus Width: 4.2335
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

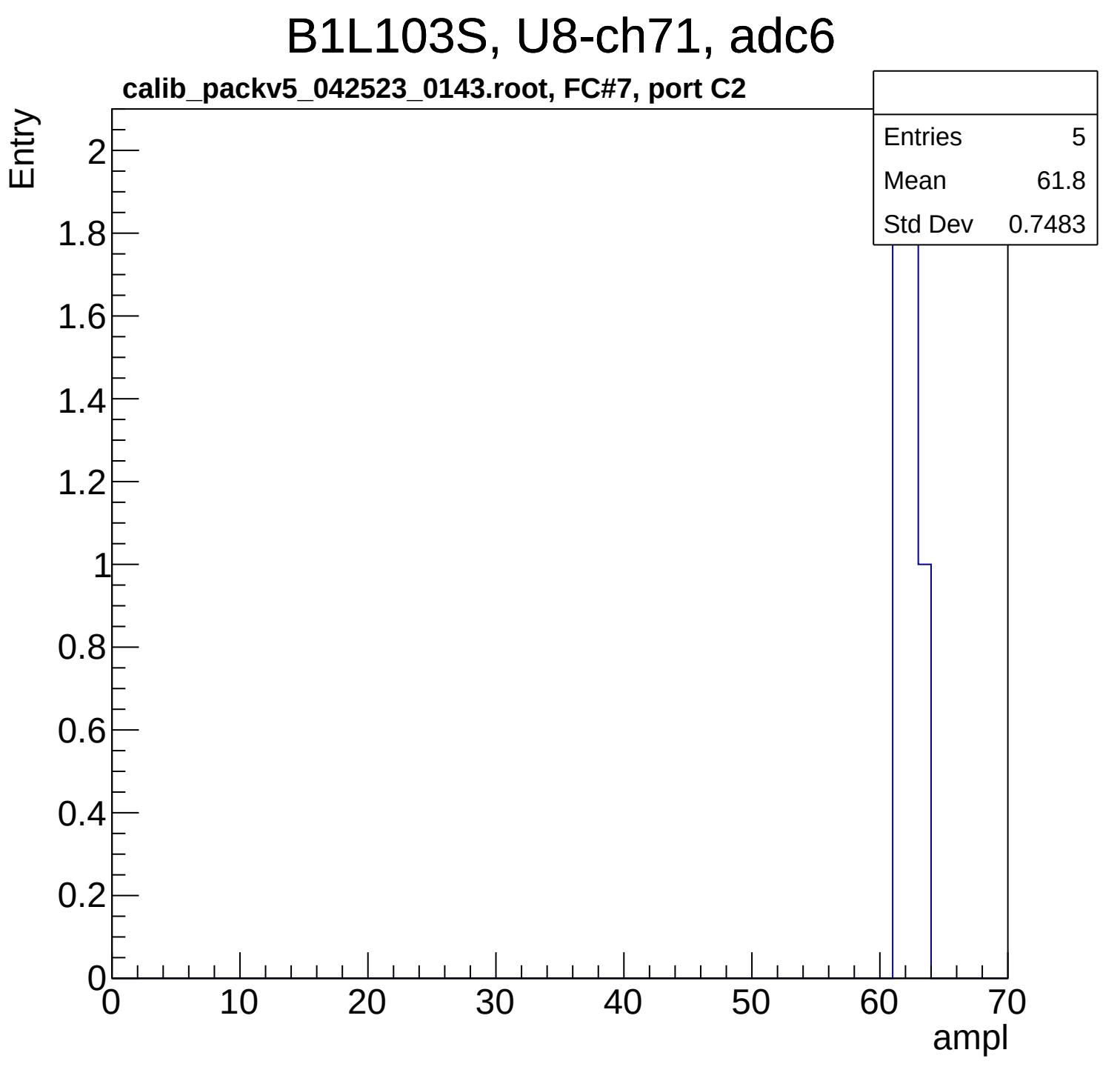

B1L103S, U8-ch71, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 36.99
Std Dev 3.74
Gaus mean : 37.3832
Gaus Width: 3.1324
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

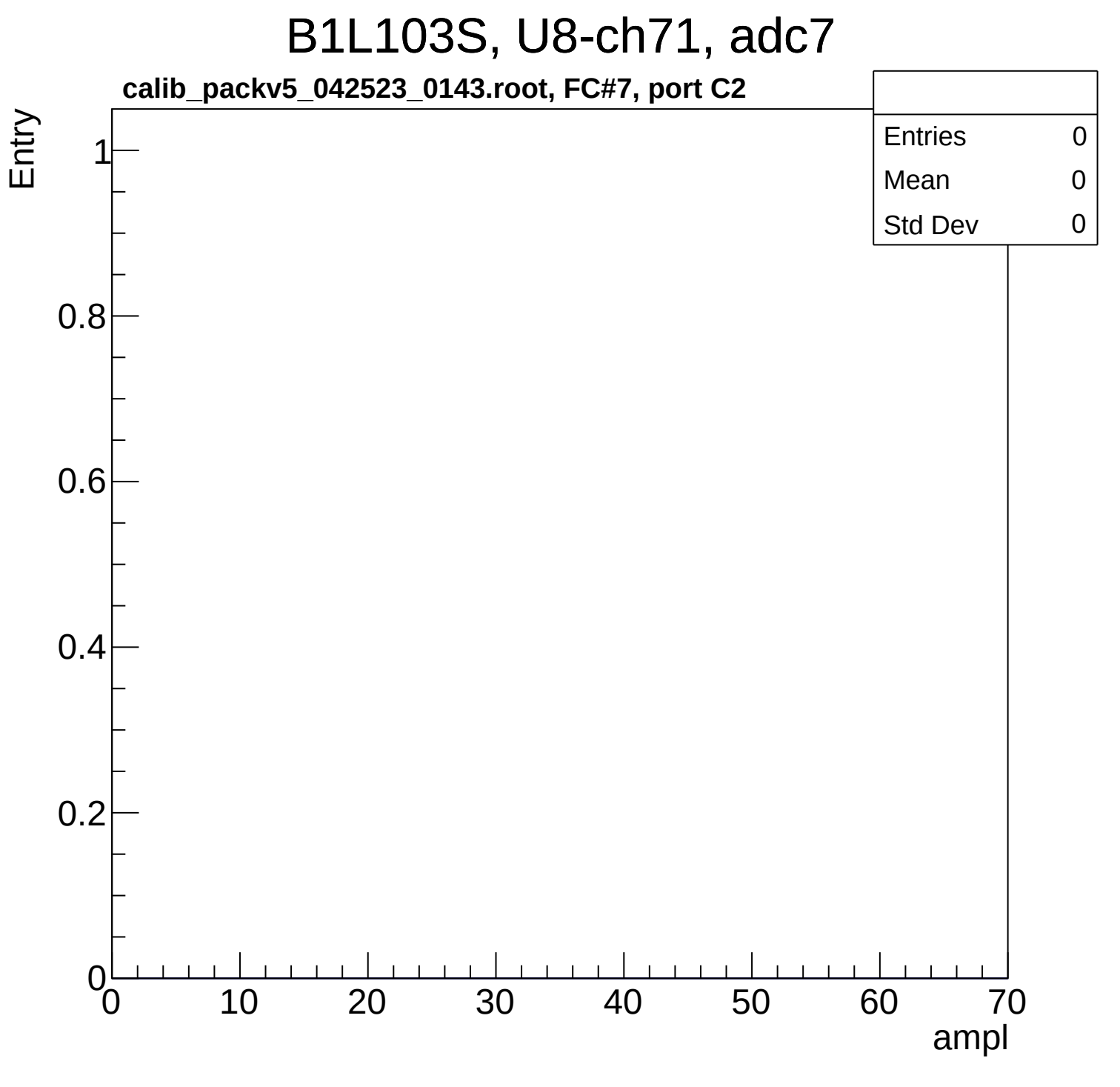

B1L103S, U8-ch71, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 43.73
Std Dev 3.204
Gaus mean : 43.6417
Gaus Width: 3.7607
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

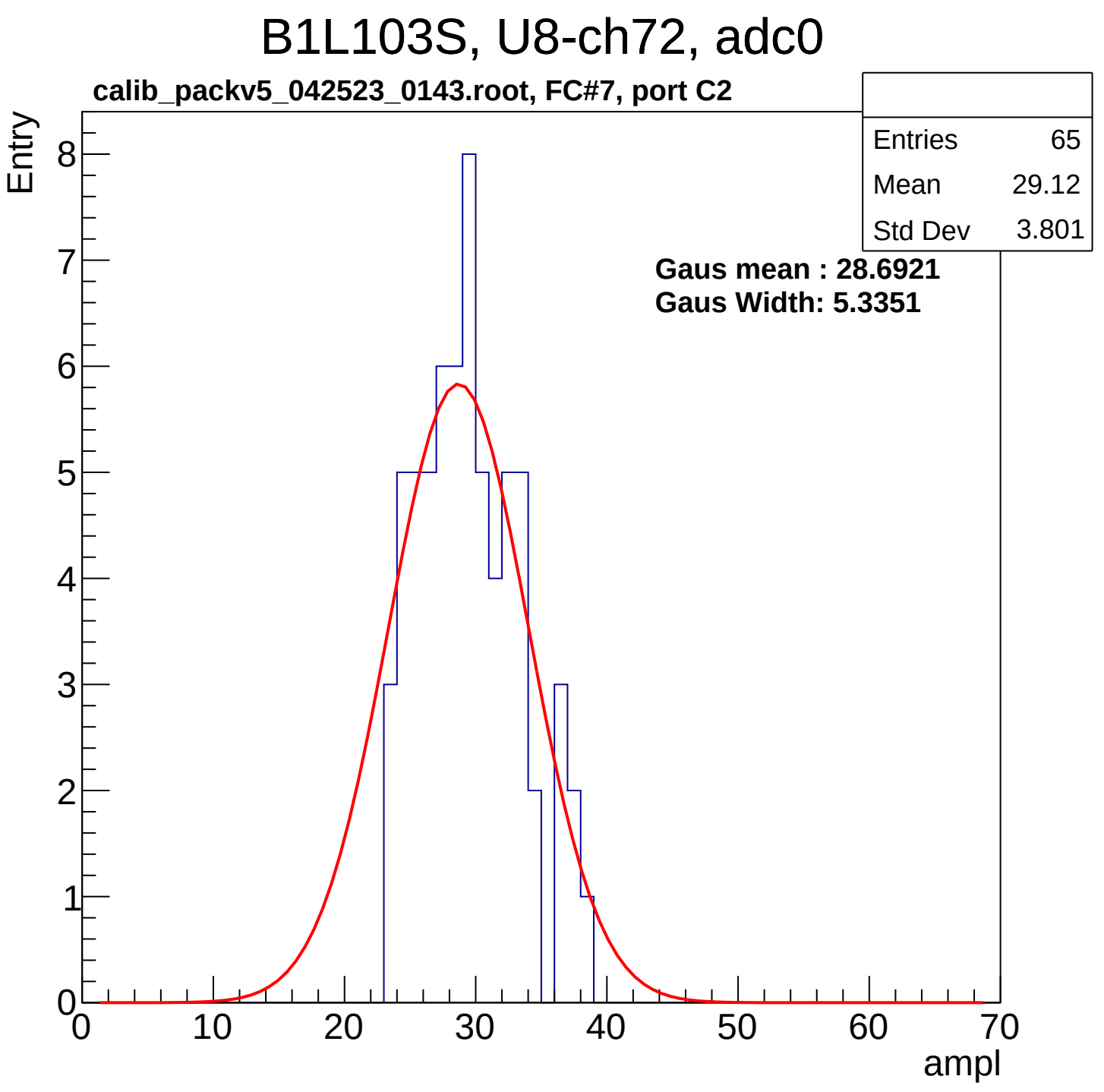

B1L103S, U8-ch71, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 49.42
Std Dev 3.188
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

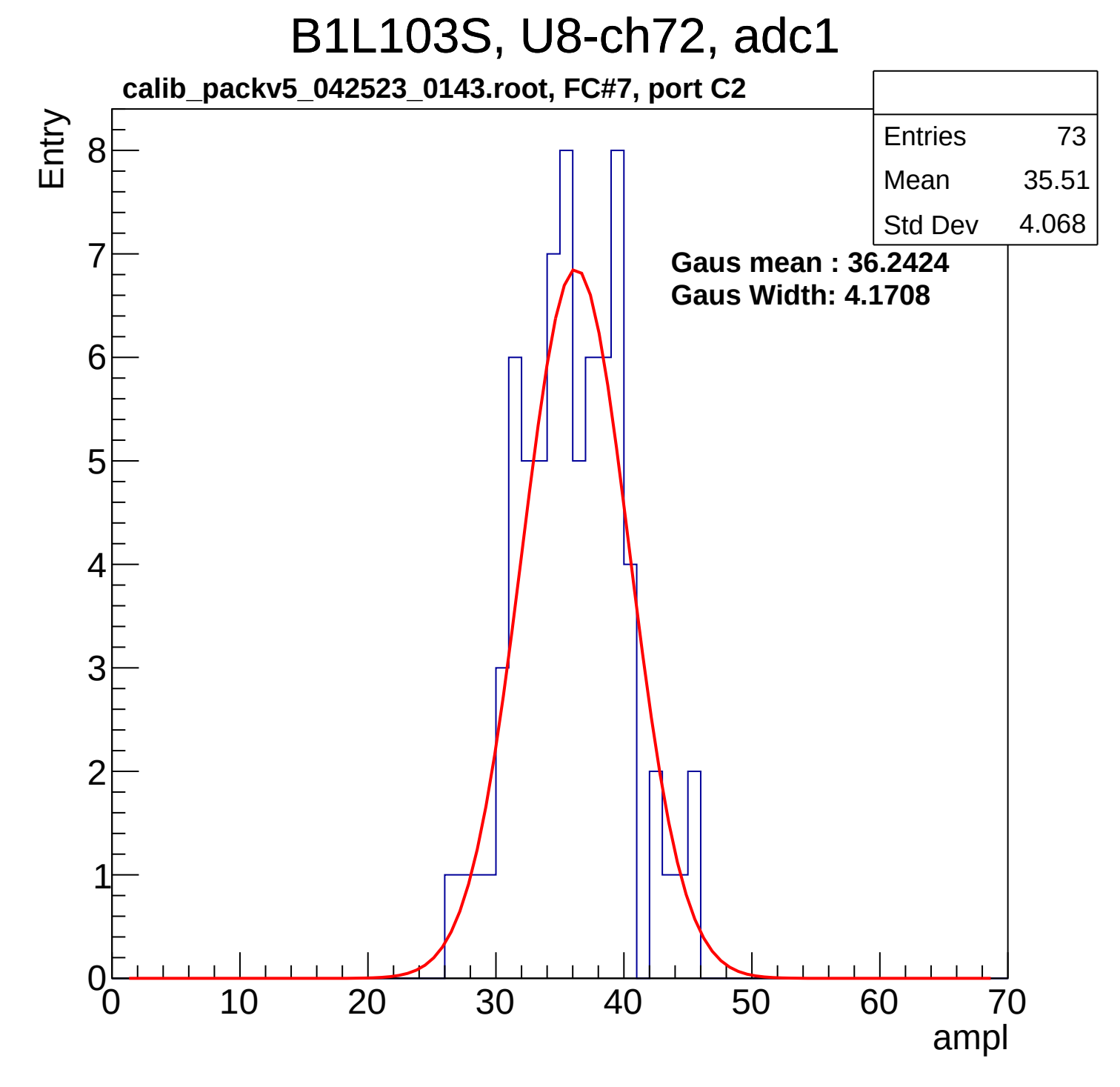

B1L103S, U8-ch71, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 54.44
Std Dev 3.29
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

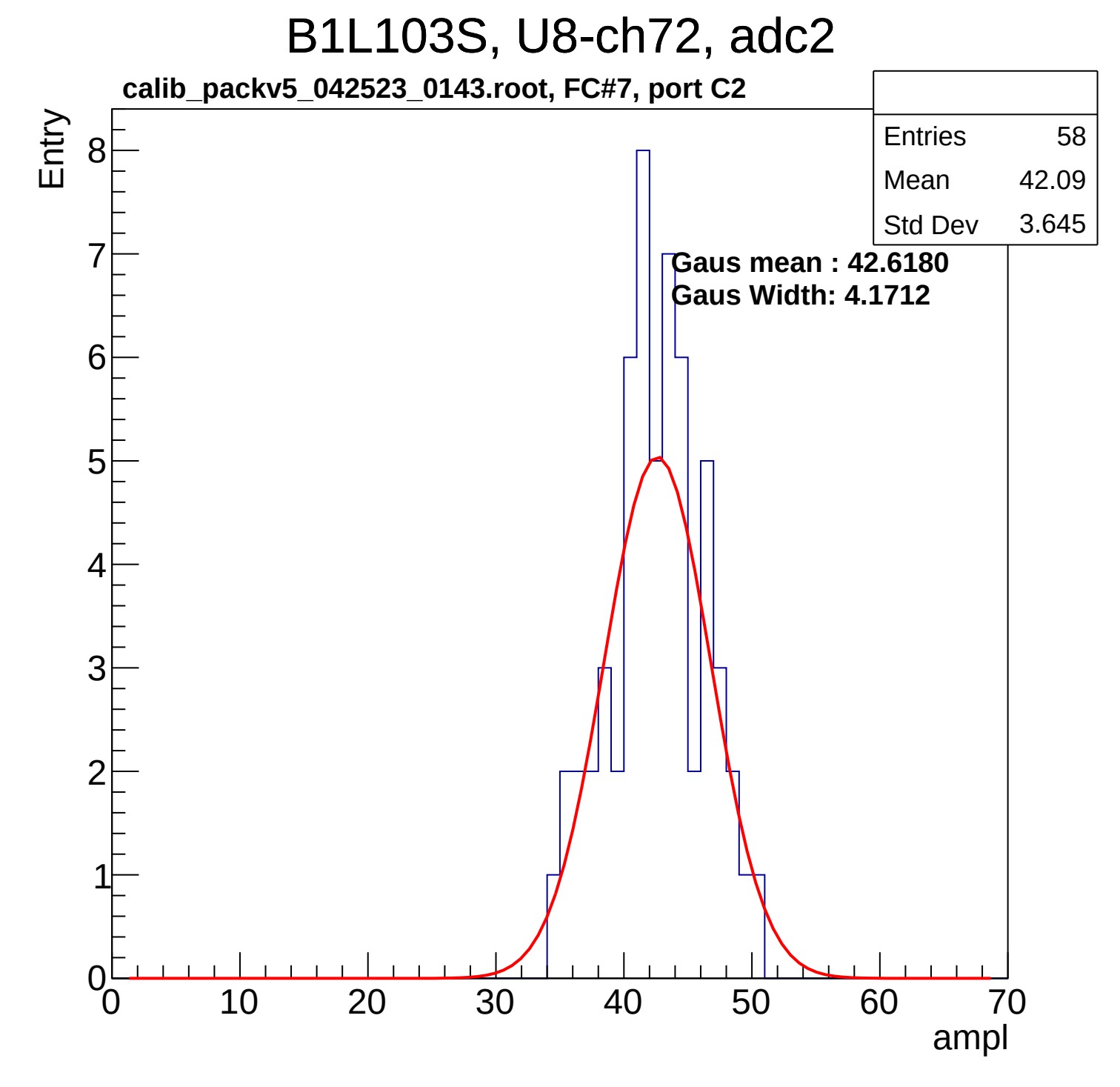

B1L103S, U8-ch71, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 58.83
Std Dev 8.417
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

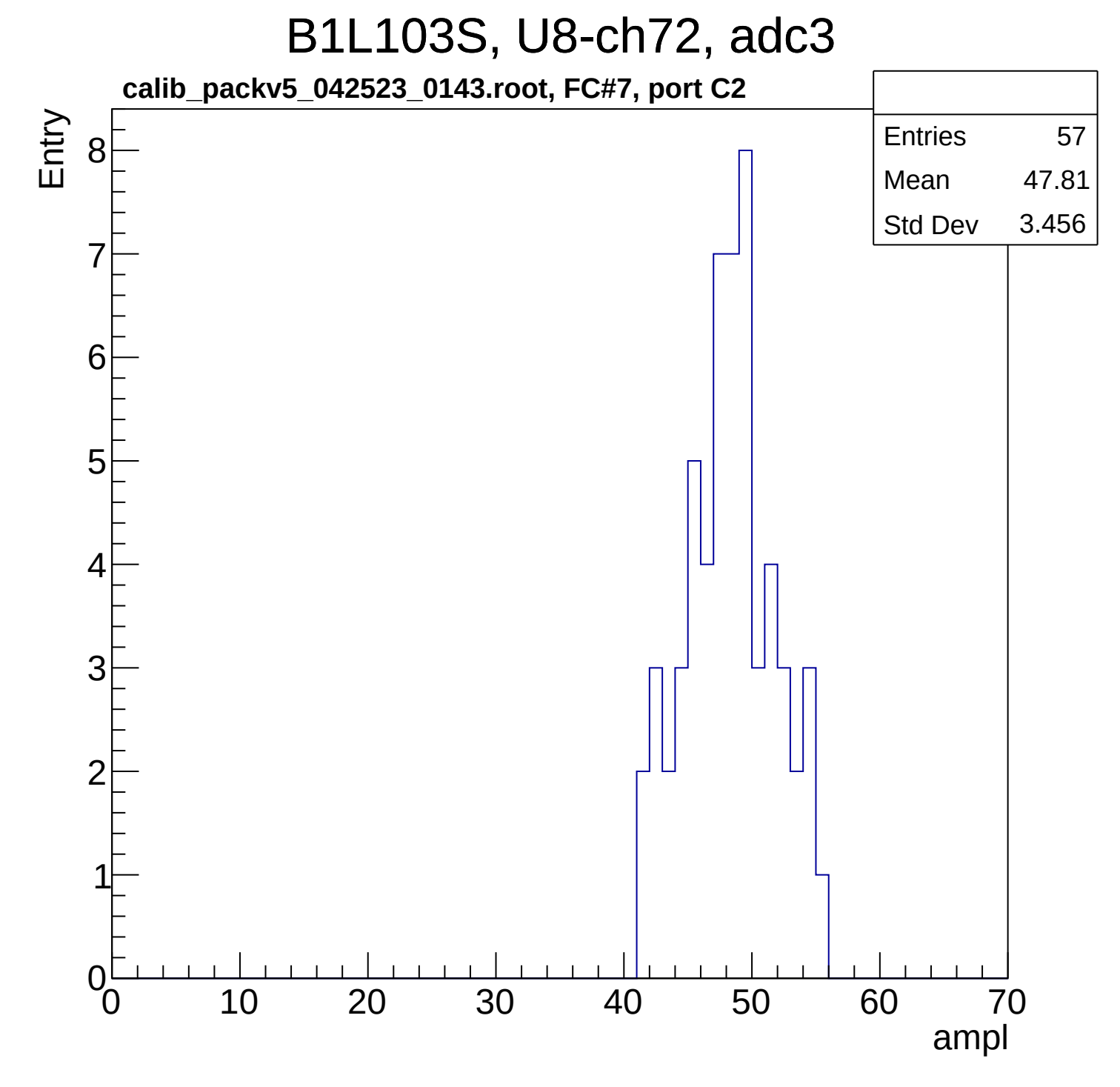

B1L103S, U8-ch71, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 61.8
Std Dev 0.7483
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

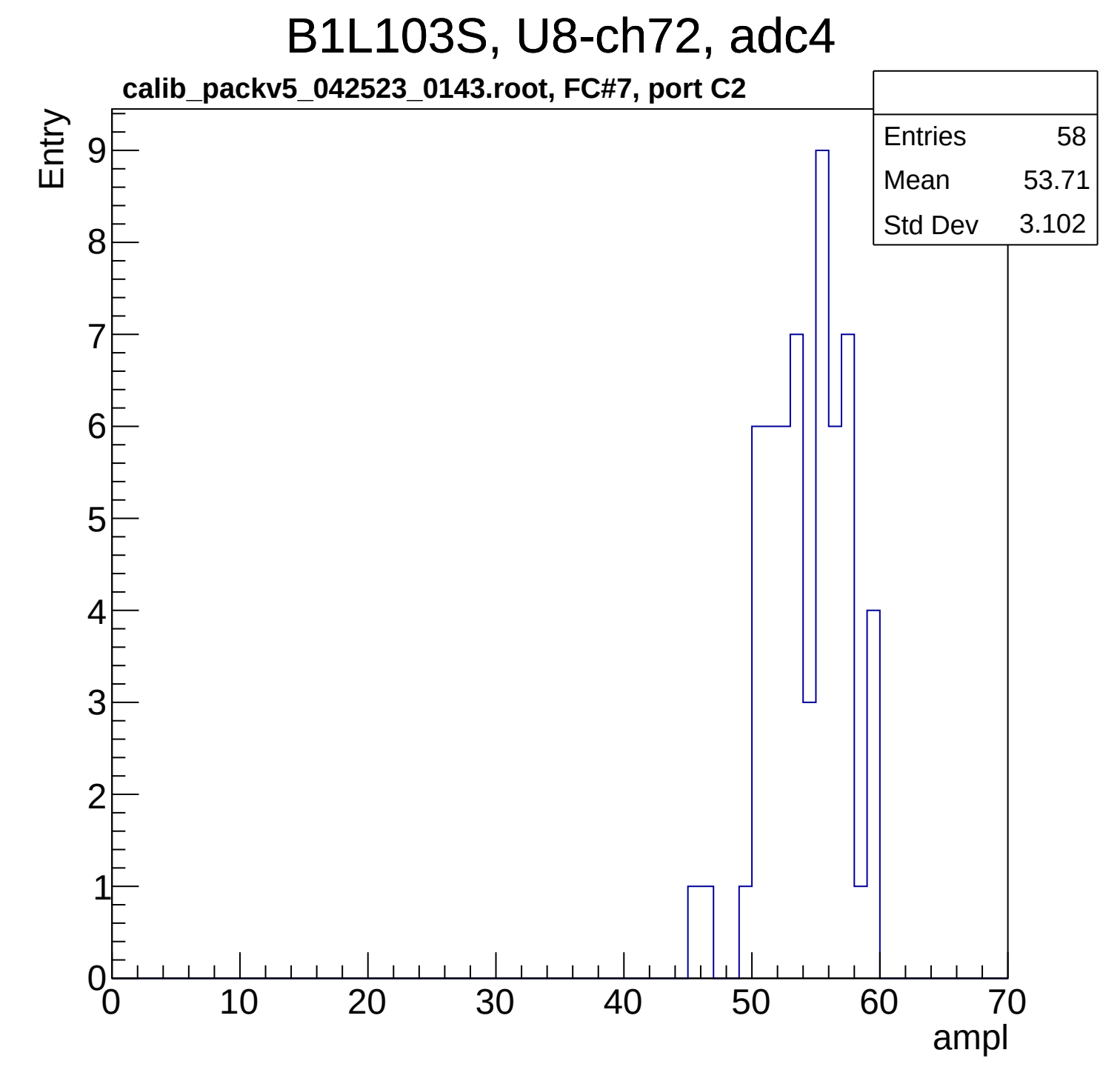

B1L103S, U8-ch71, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

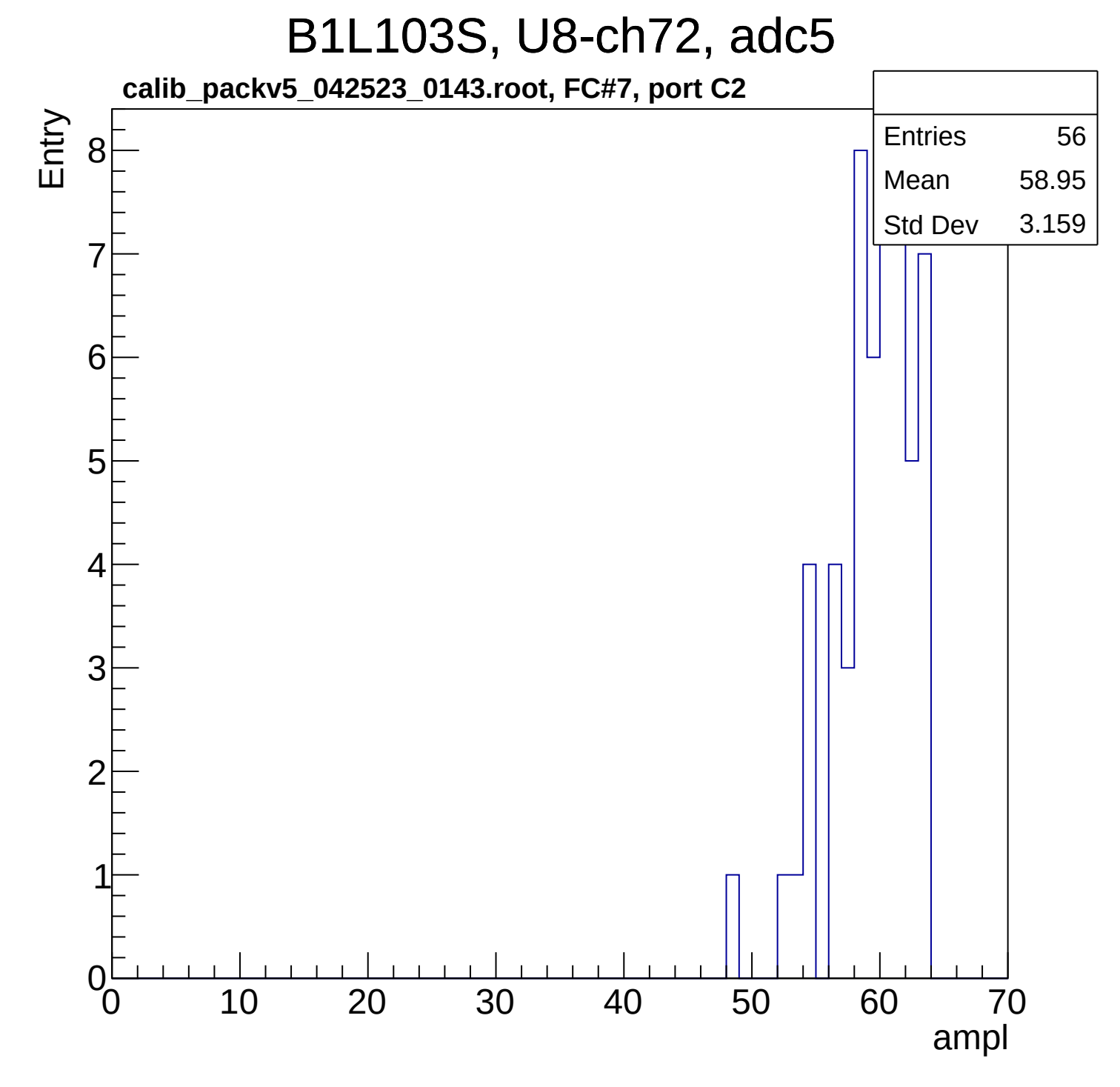

B1L103S, U8-ch72, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 29.12
Std Dev 3.801
Gaus mean : 28.6921
Gaus Width: 5.3351
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

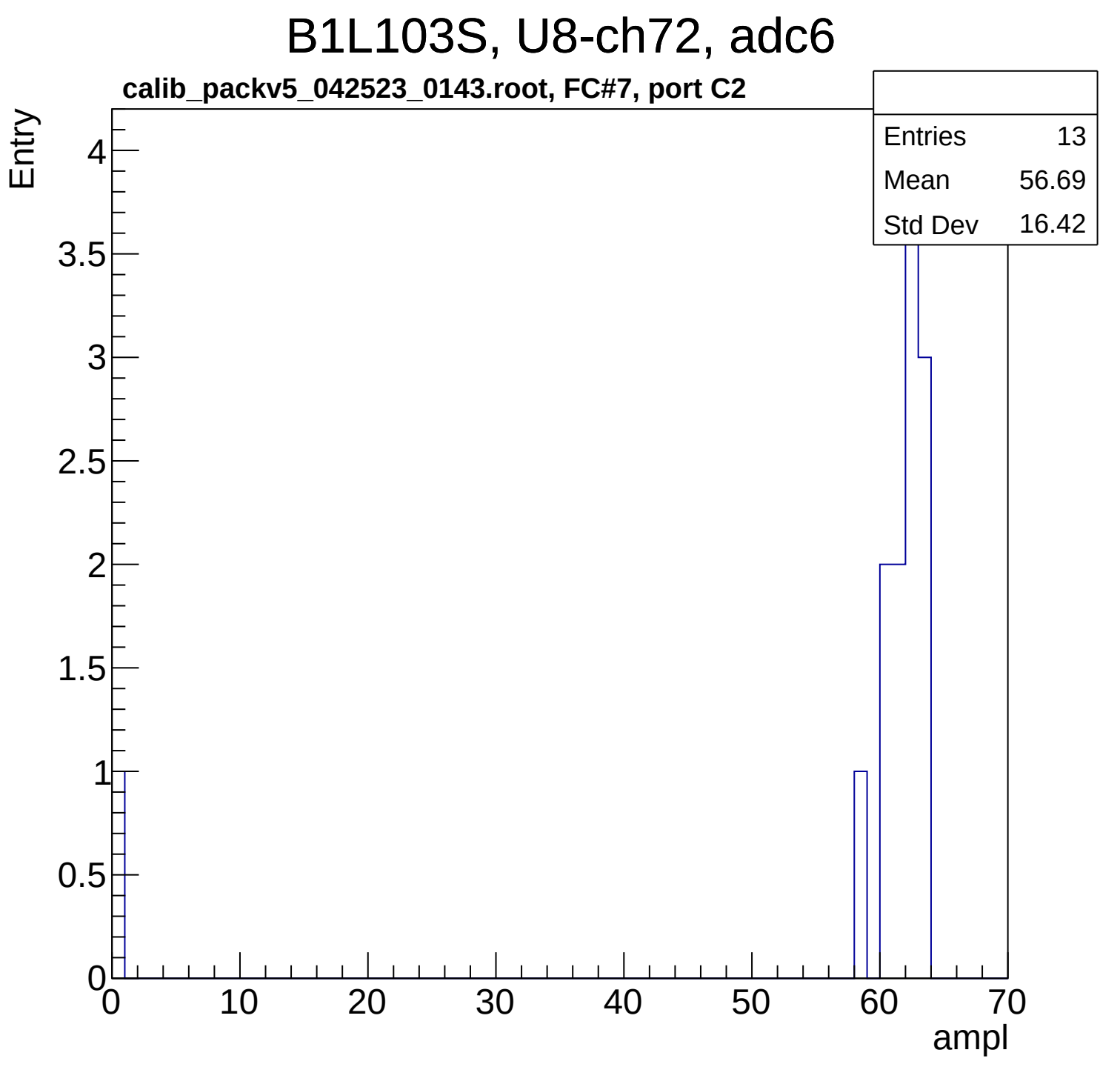

B1L103S, U8-ch72, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 35.51
Std Dev 4.068
Gaus mean : 36.2424
Gaus Width: 4.1708
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

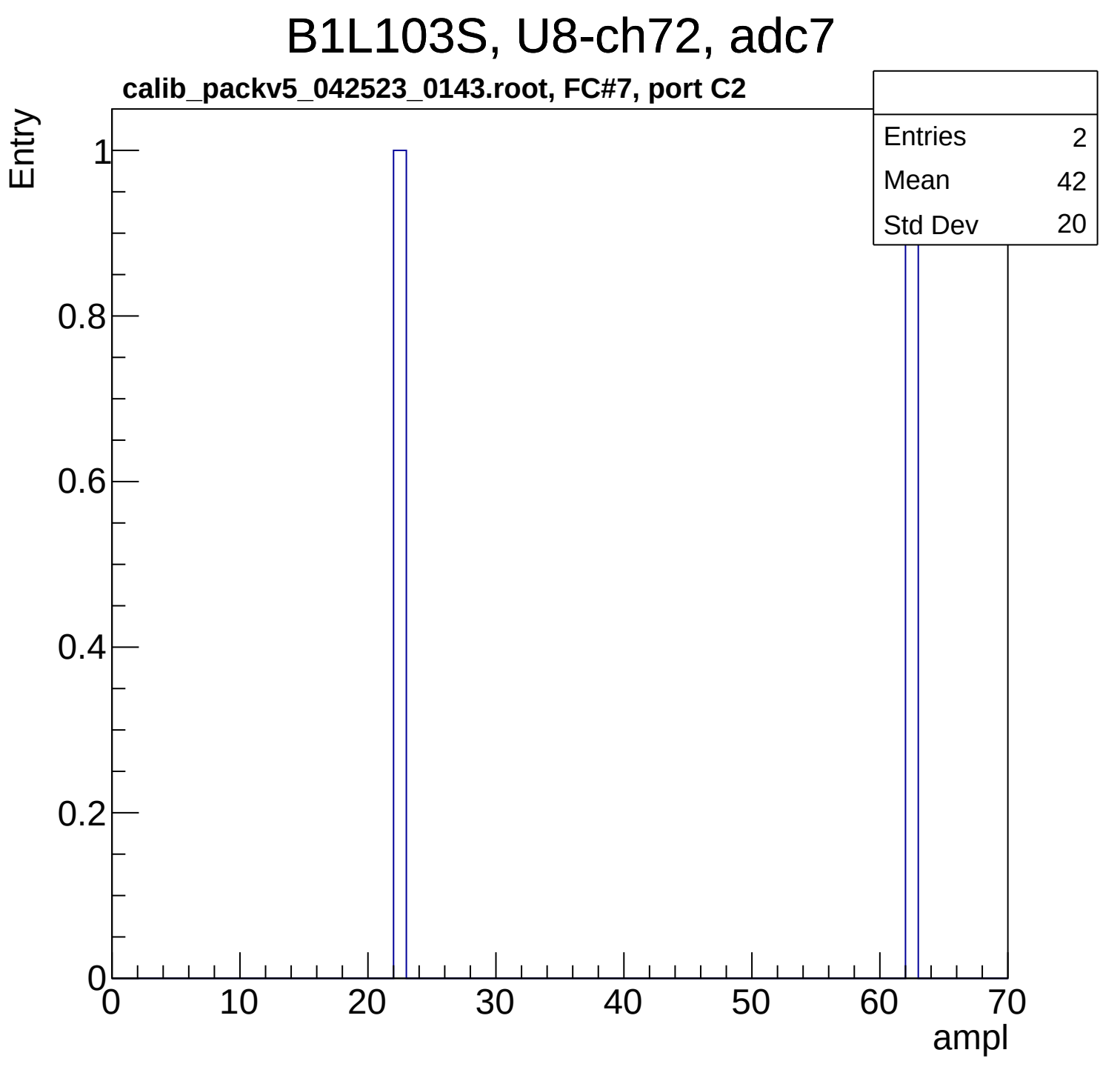

B1L103S, U8-ch72, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 42.09
Std Dev 3.645
Gaus mean : 42.6180
Gaus Width: 4.1712
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

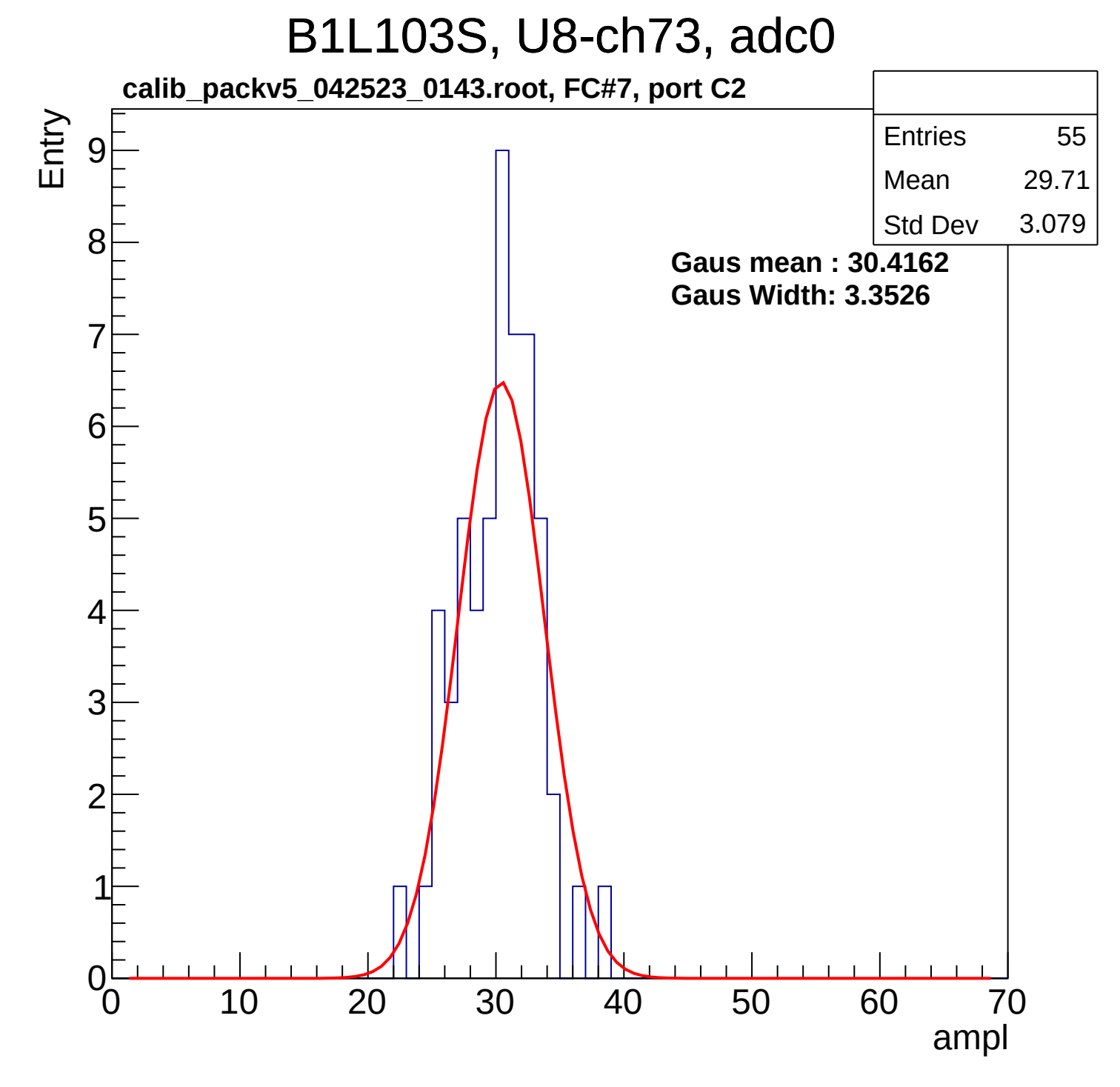

B1L103S, U8-ch72, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 47.81
Std Dev 3.456
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

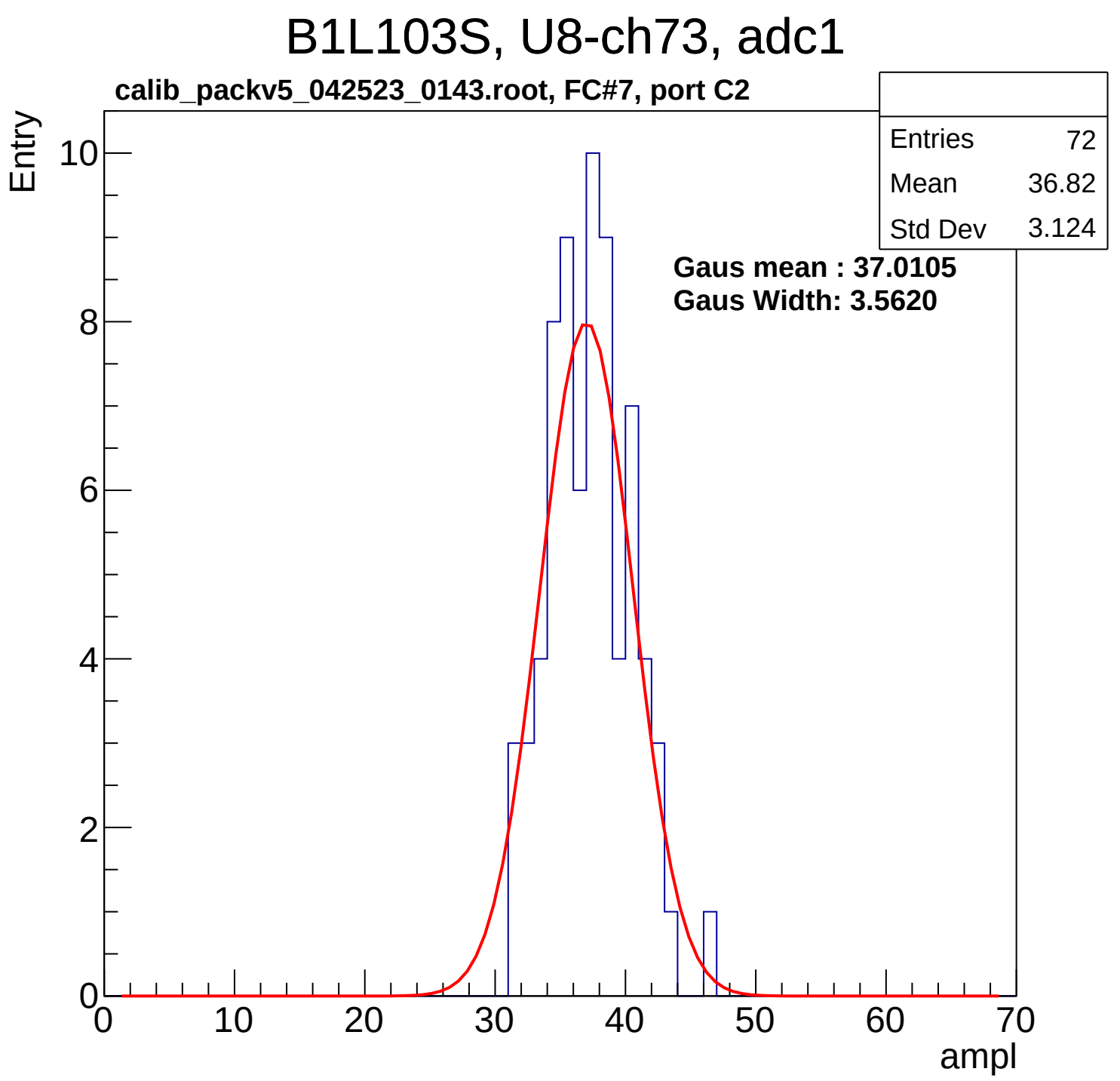

B1L103S, U8-ch72, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 53.71
Std Dev 3.102
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

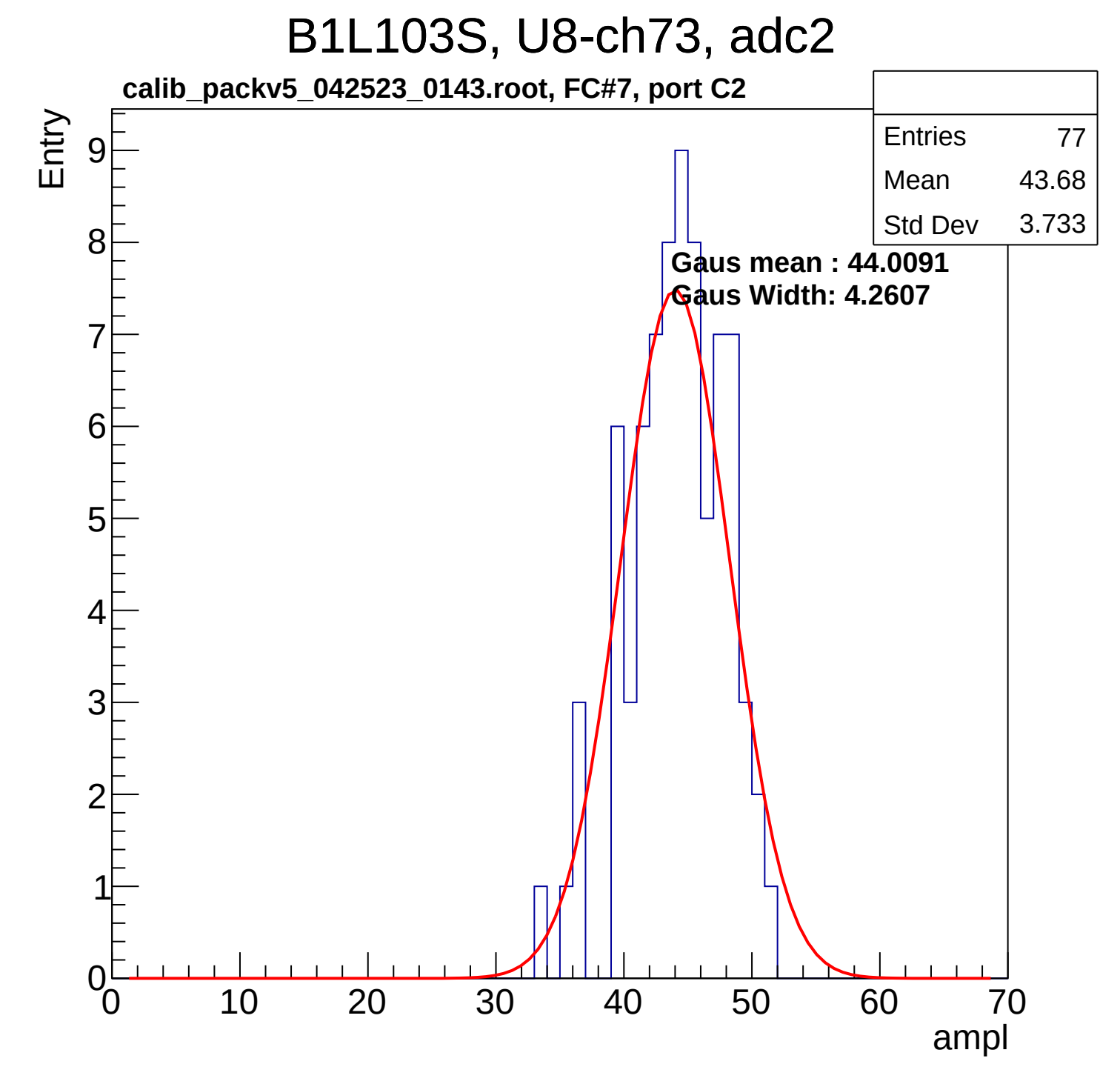

B1L103S, U8-ch72, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 58.95
Std Dev 3.159
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

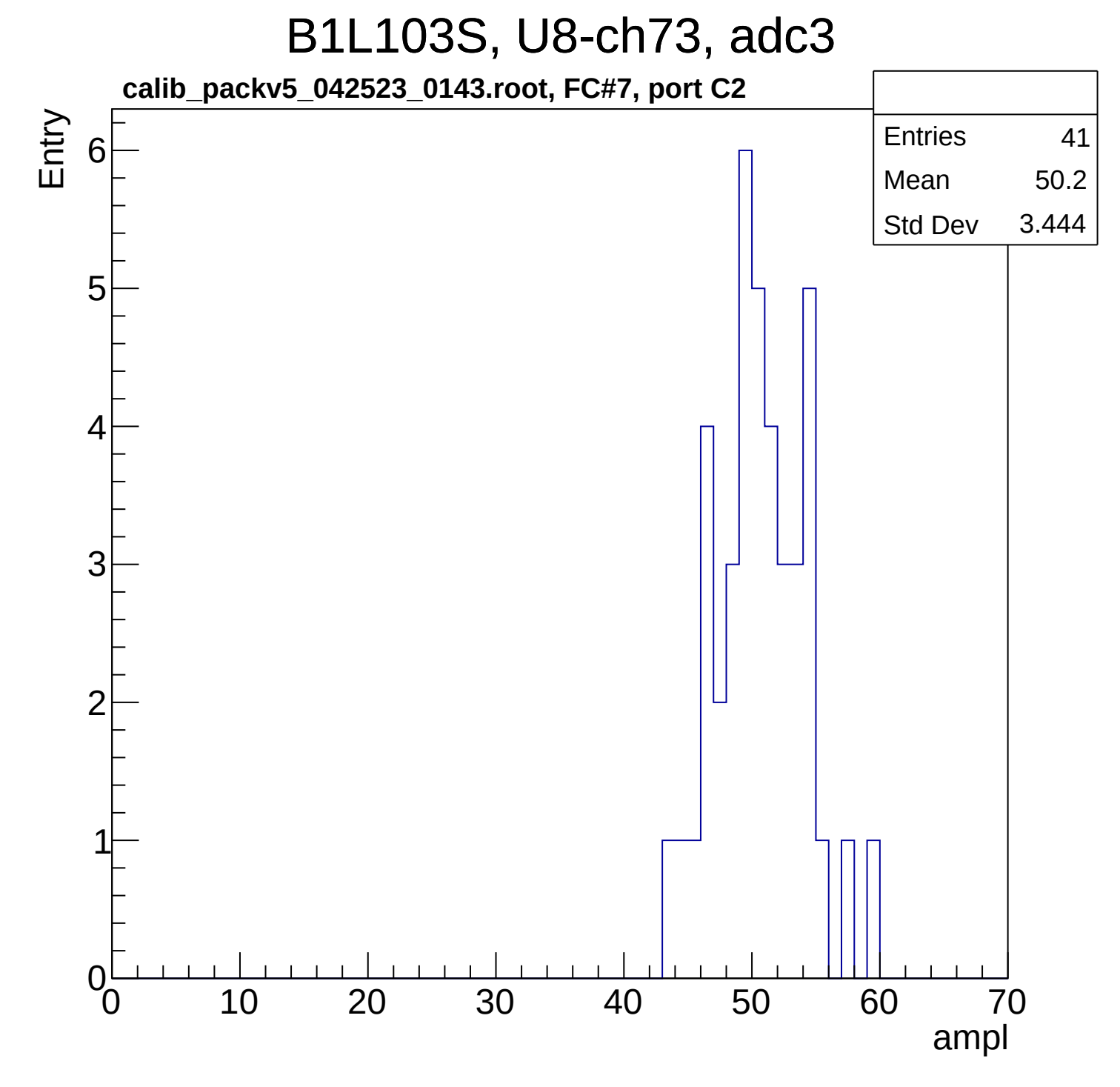

B1L103S, U8-ch72, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 13
Mean 56.69
Std Dev 16.42
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

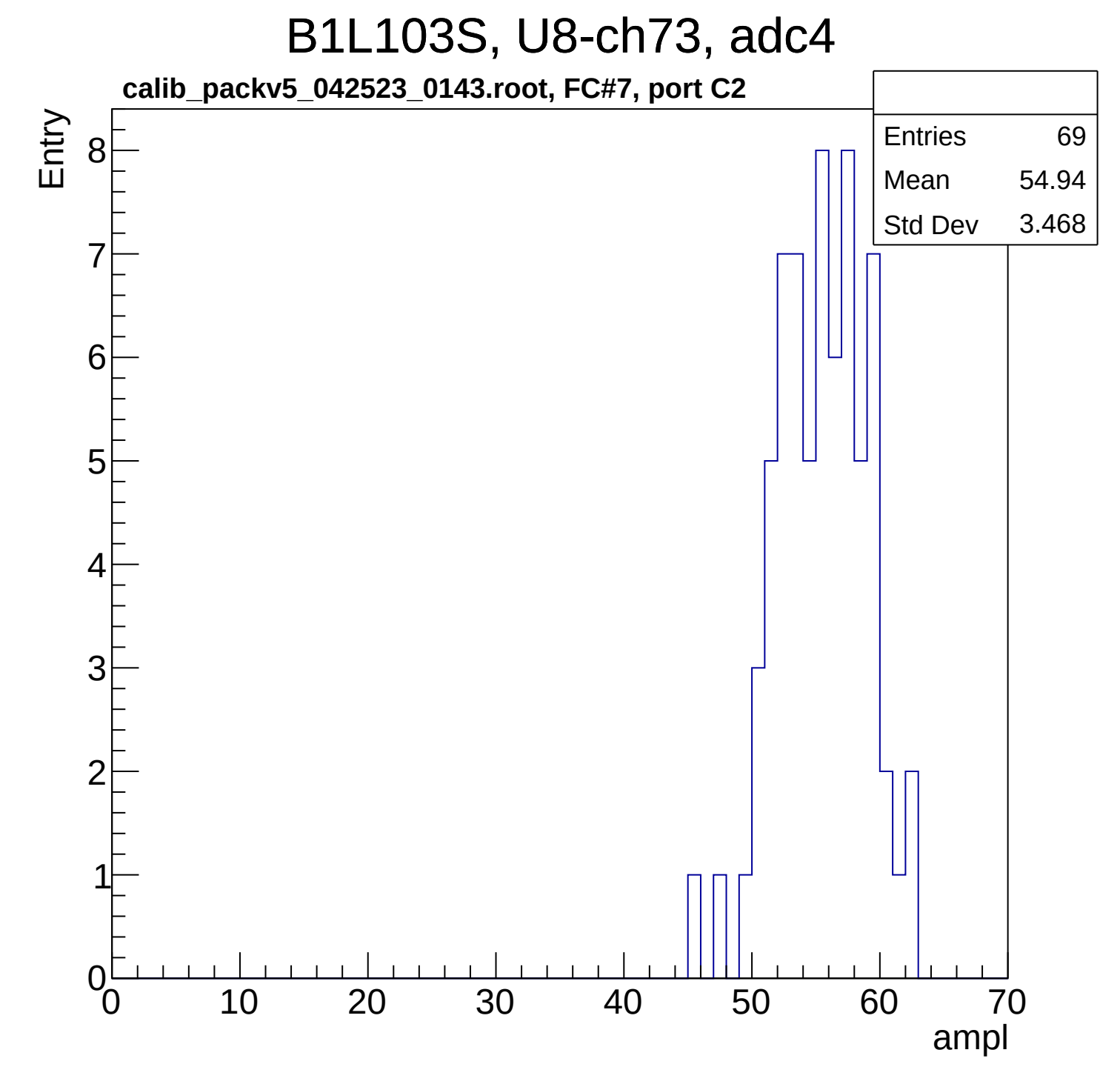

B1L103S, U8-ch72, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 42
Std Dev 20
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

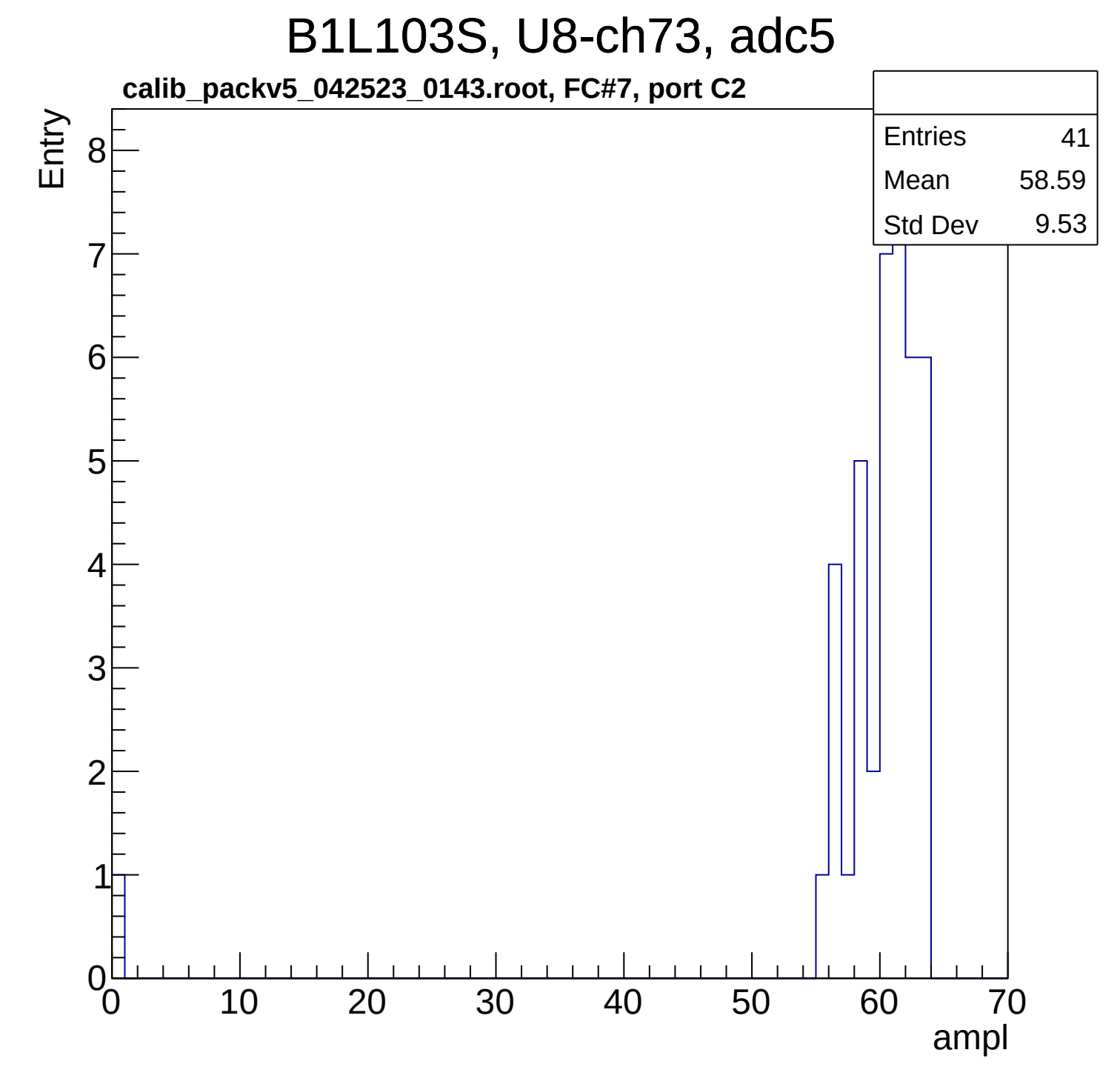

B1L103S, U8-ch73, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 29.71
Std Dev 3.079
Gaus mean : 30.4162
Gaus Width: 3.3526
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

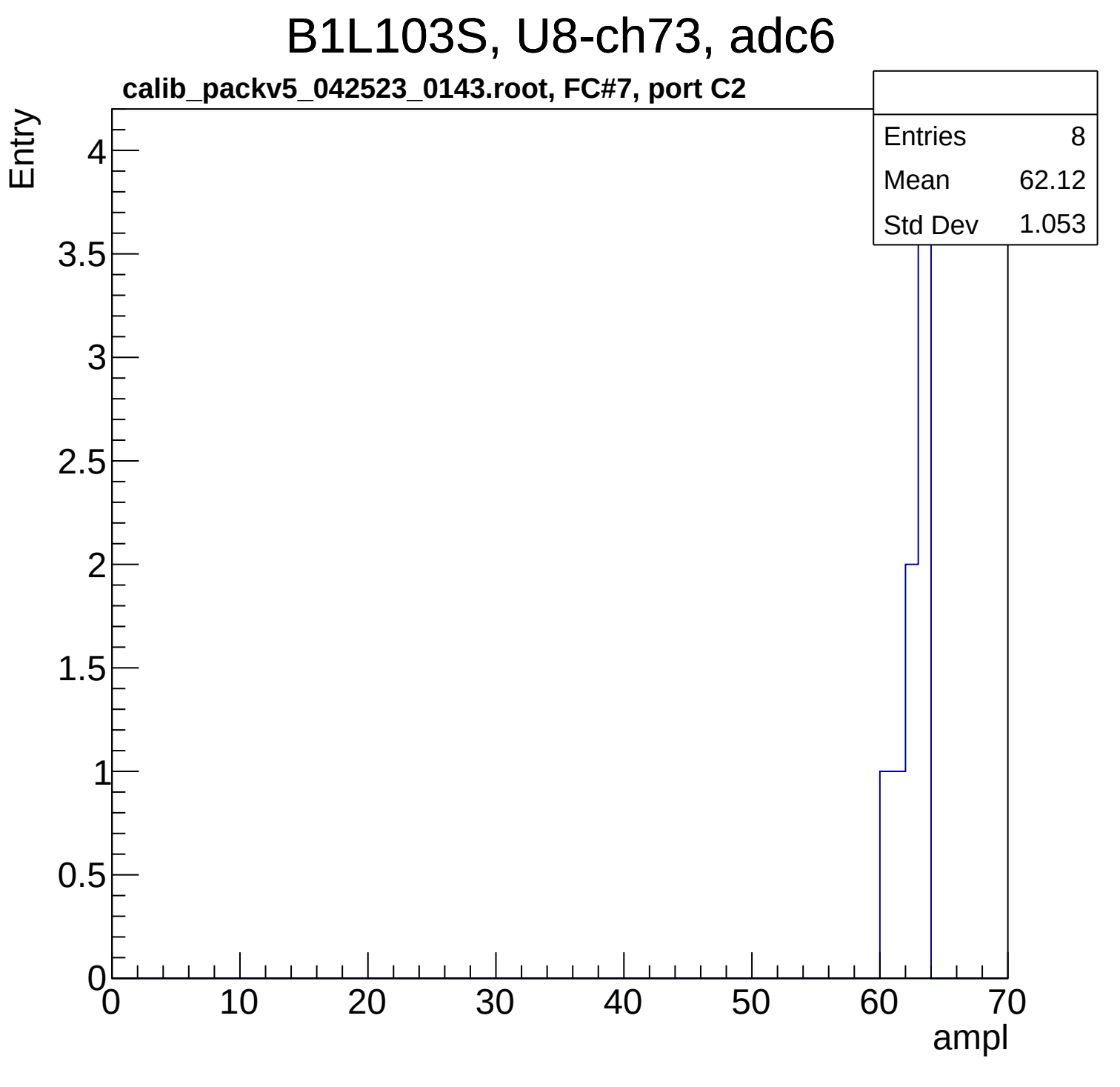

B1L103S, U8-ch73, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 36.82
Std Dev 3.124
Gaus mean : 37.0105
Gaus Width: 3.5620
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

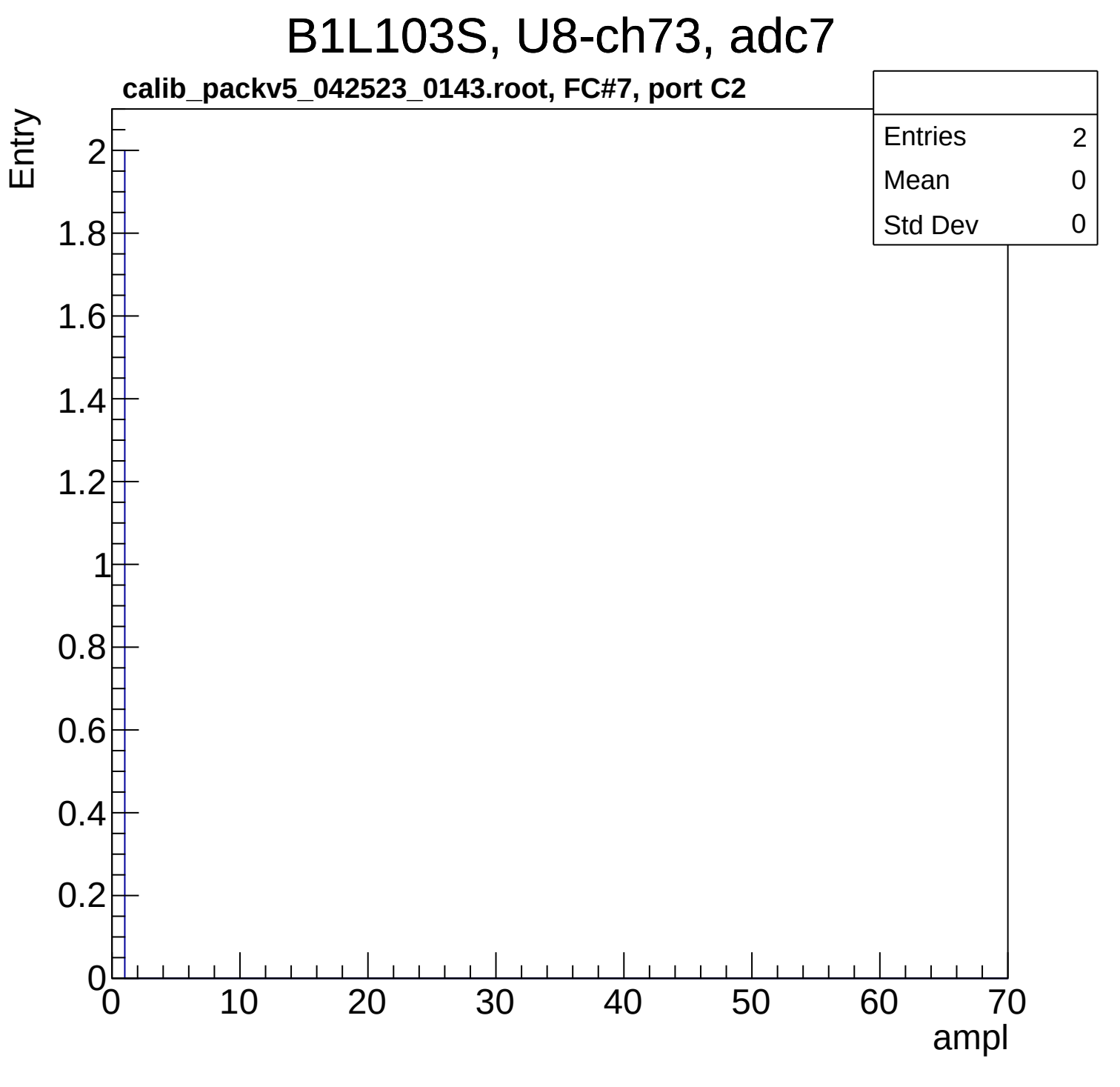

B1L103S, U8-ch73, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 43.68
Std Dev 3.733
Gaus mean : 44.0091
Gaus Width: 4.2607
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

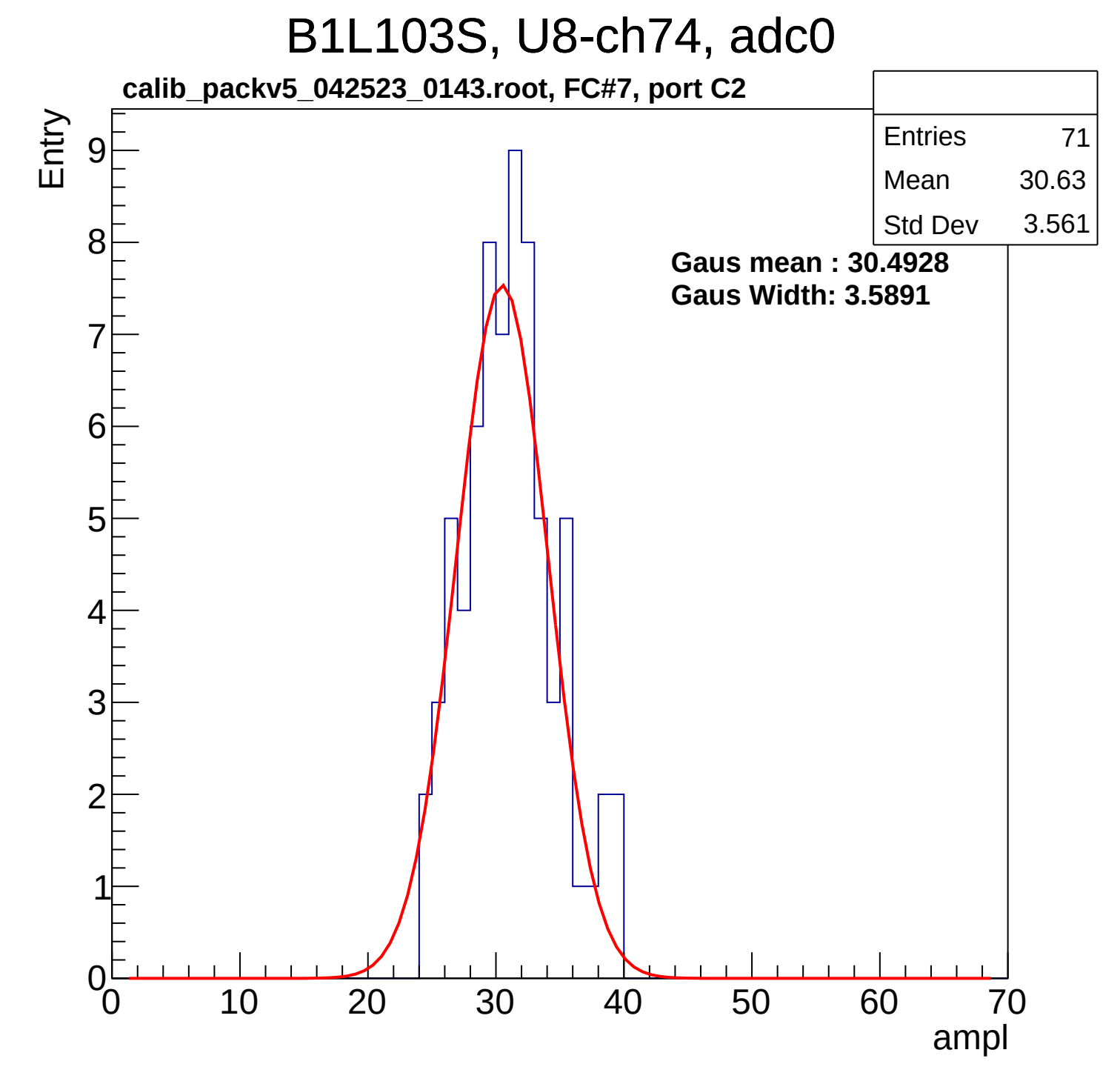

B1L103S, U8-ch73, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 41
Mean 50.2
Std Dev 3.444
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

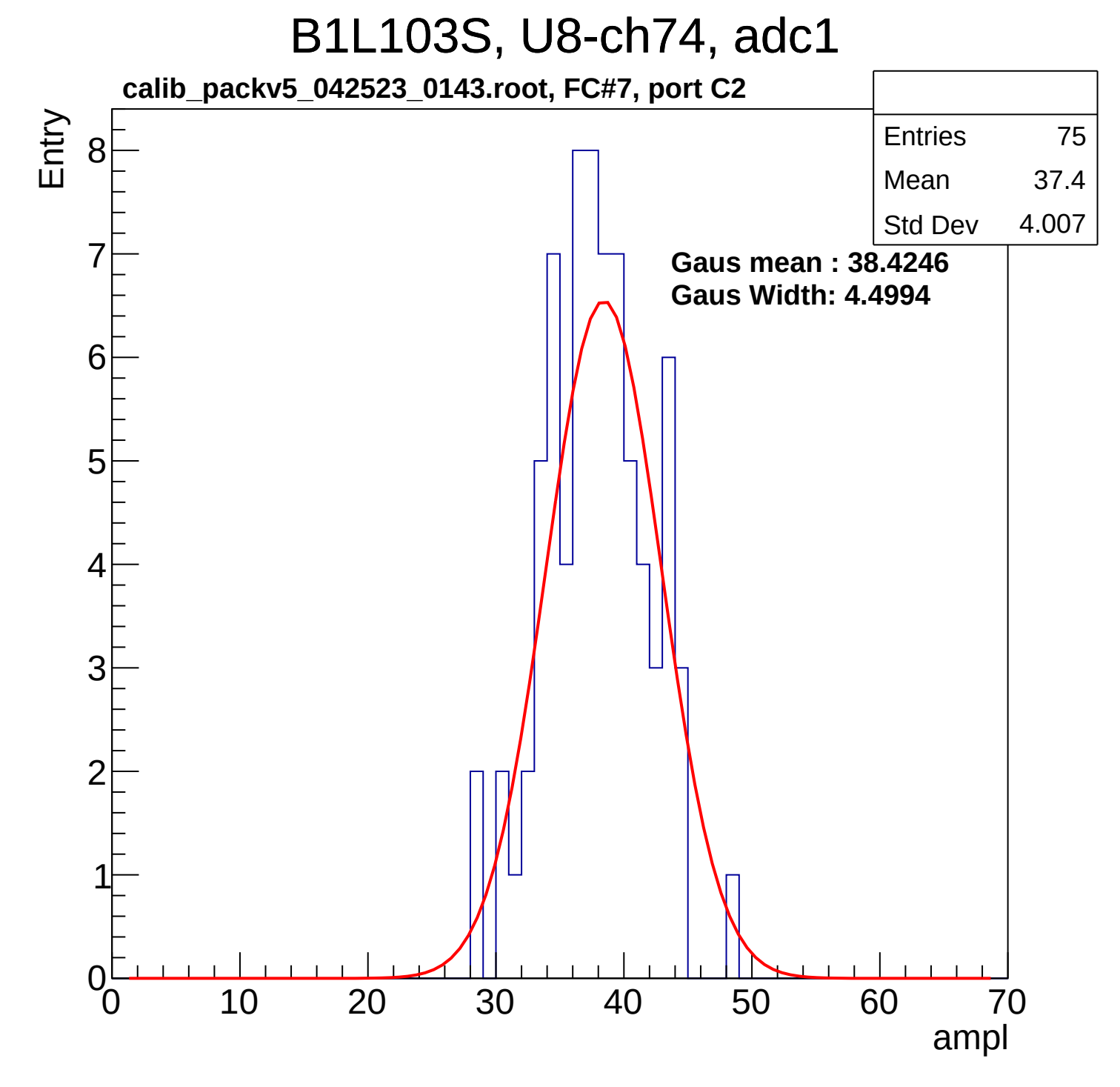

B1L103S, U8-ch73, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 54.94
Std Dev 3.468
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

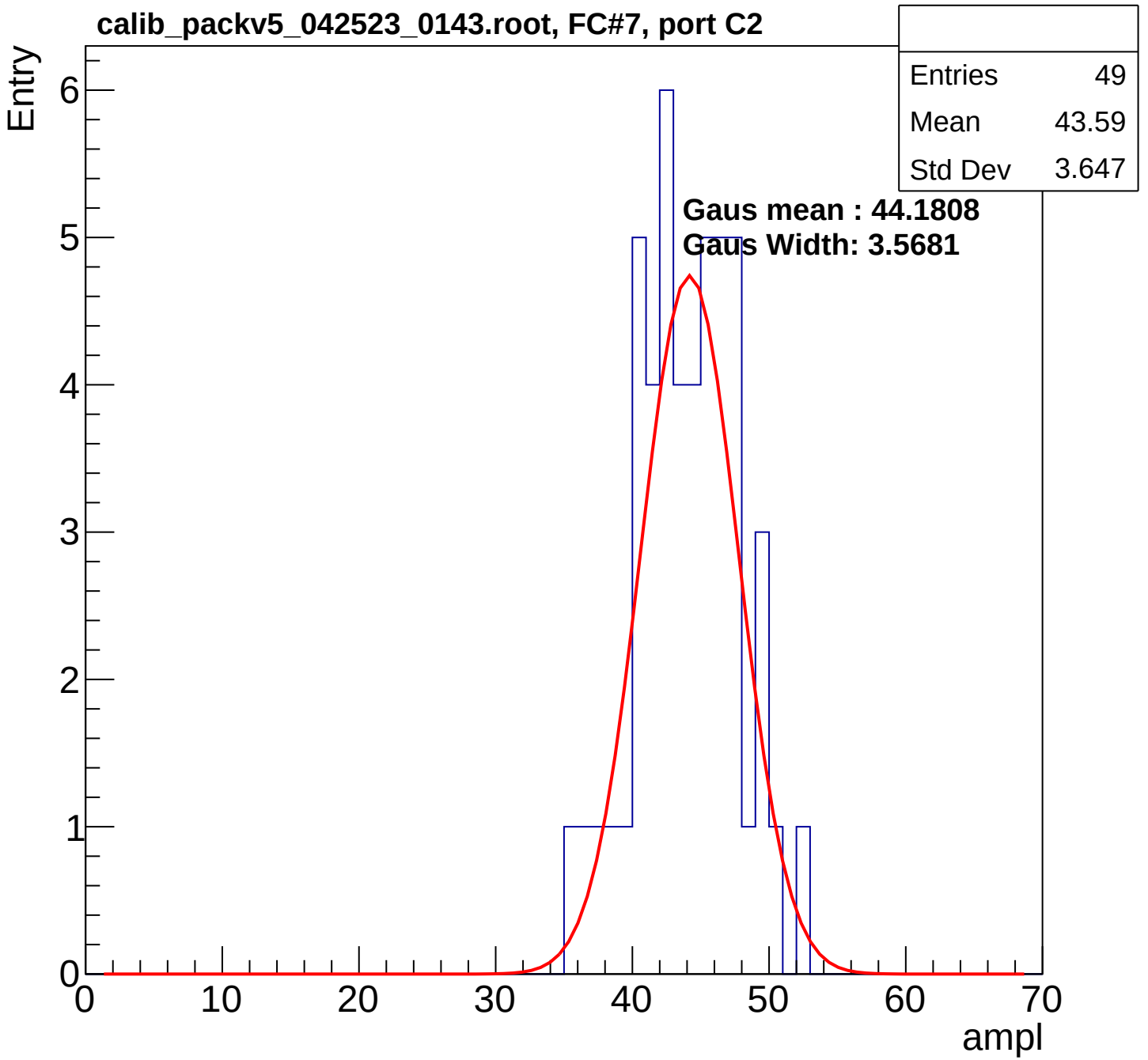

B1L103S, U8-ch73, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 41
Mean 58.59
Std Dev 9.53
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

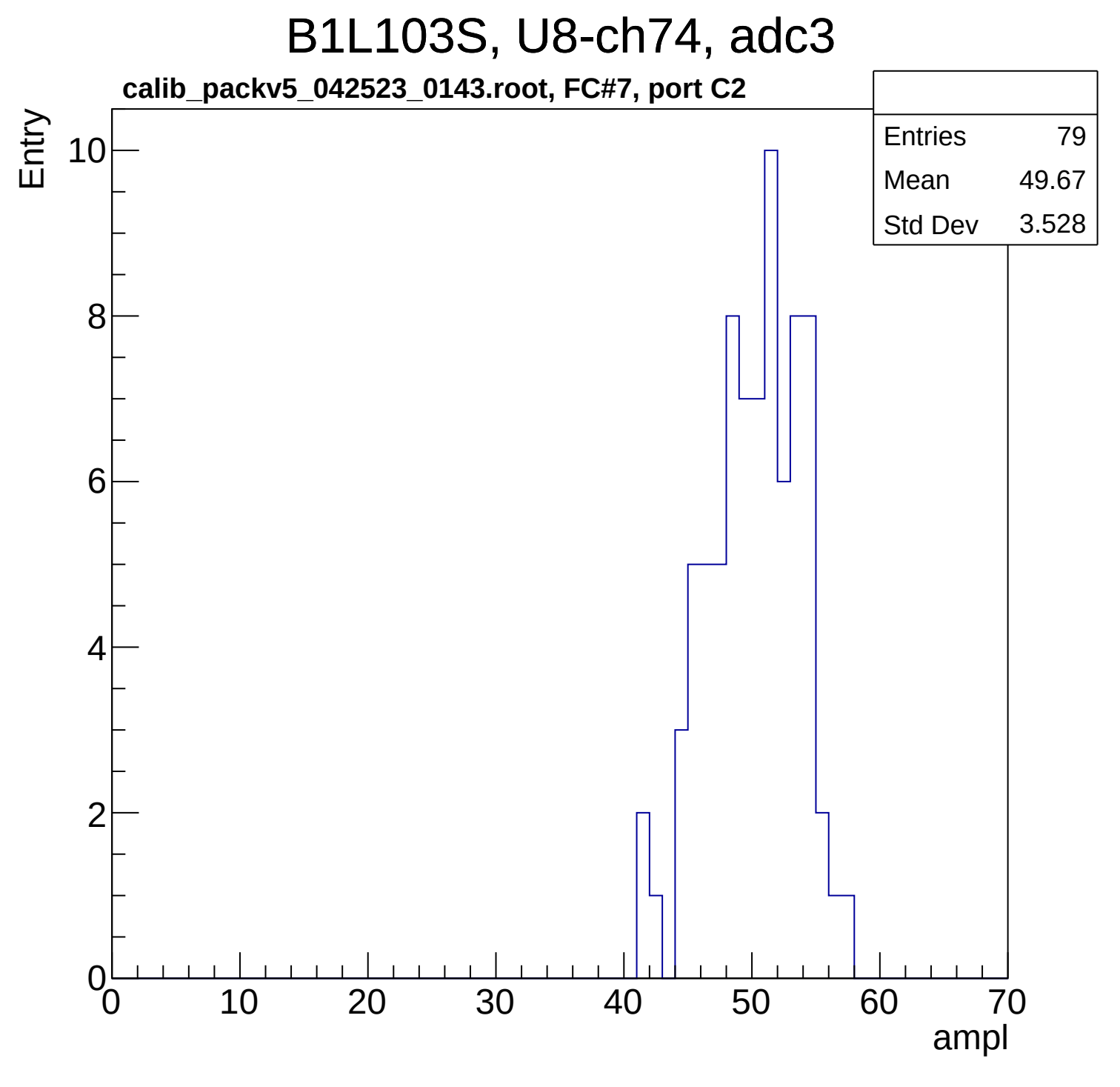

B1L103S, U8-ch73, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 8
Mean 62.12
Std Dev 1.053
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

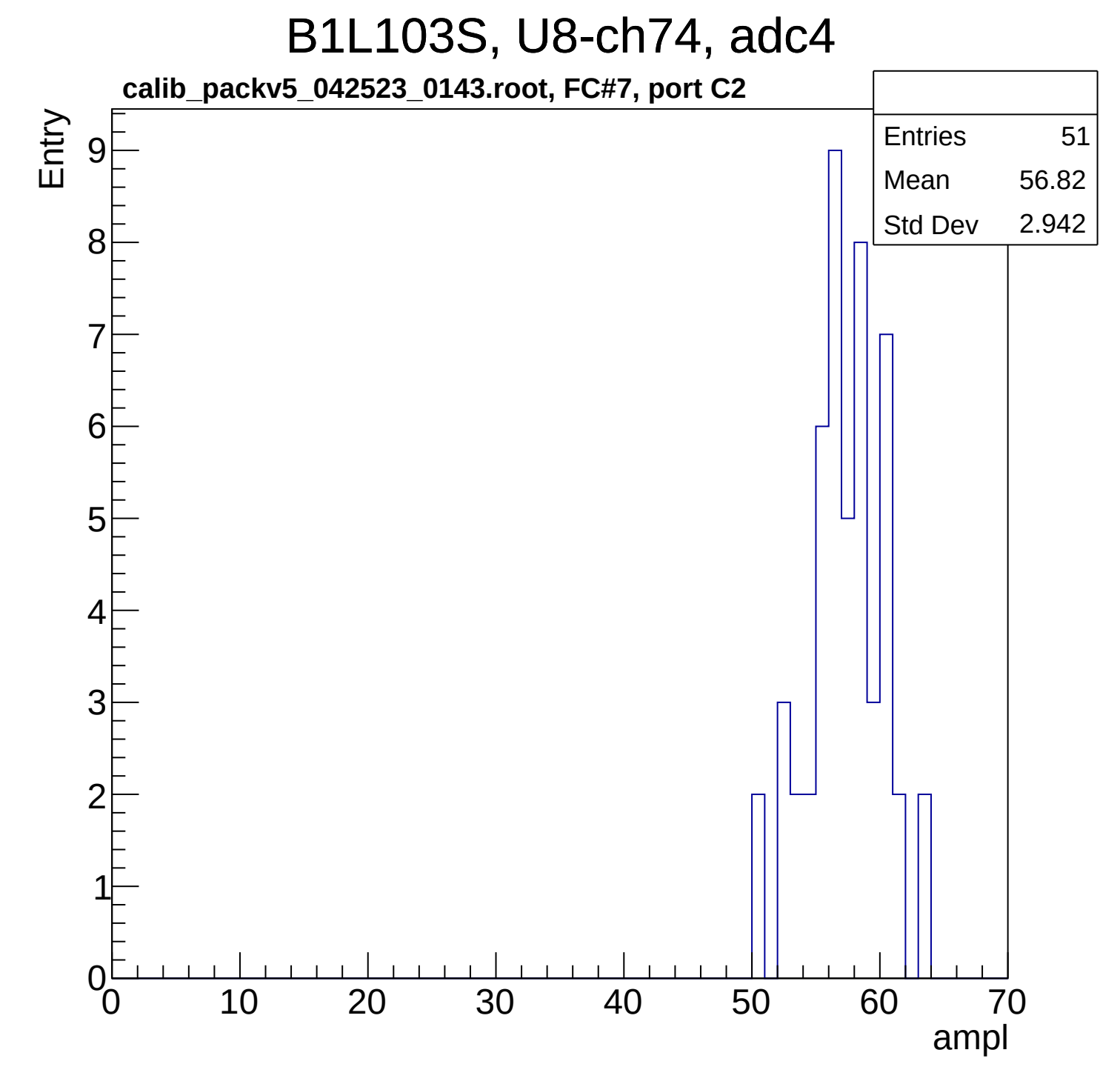

B1L103S, U8-ch73, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

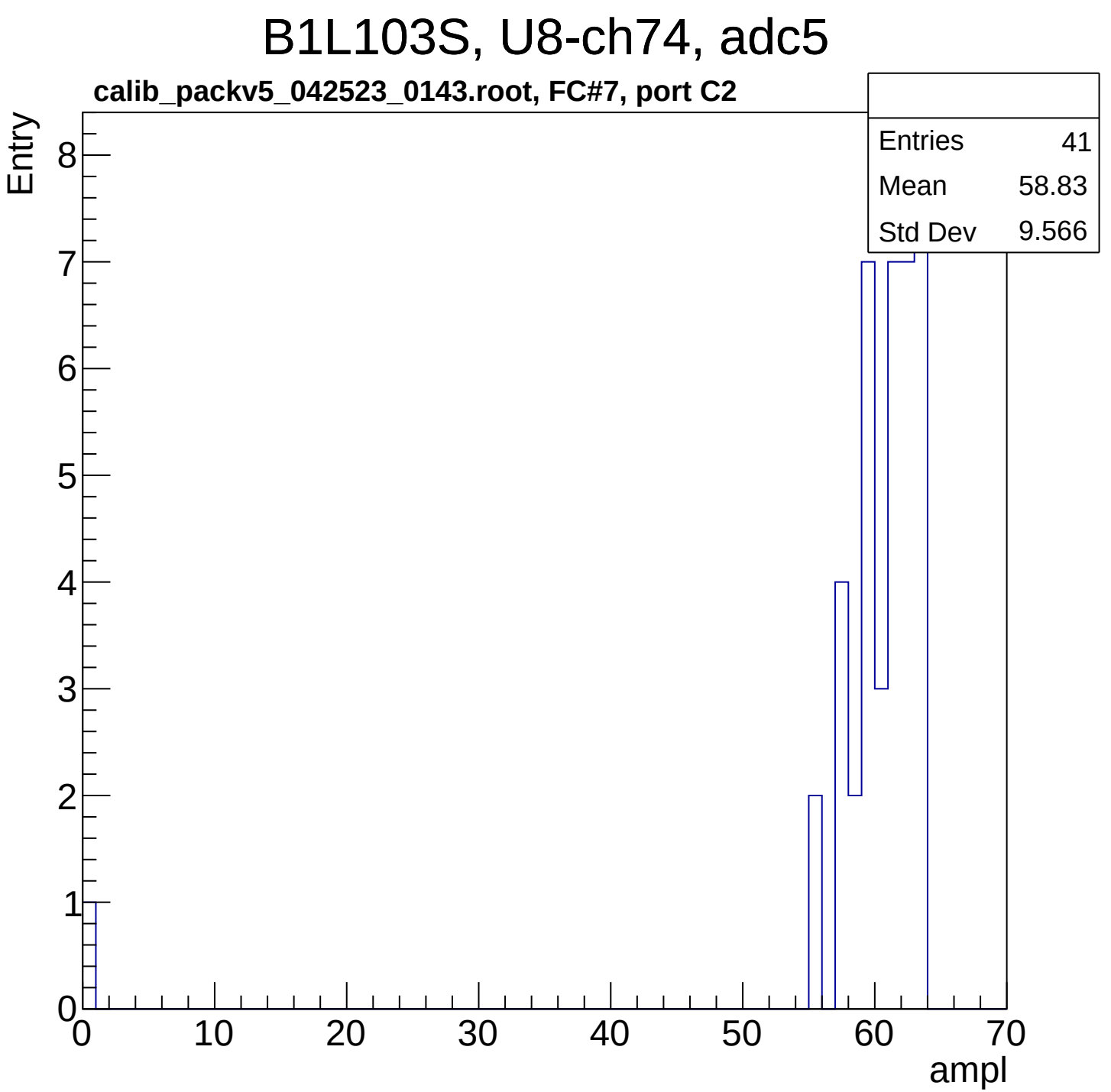

B1L103S, U8-ch74, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 30.63
Std Dev 3.561
Gaus mean : 30.4928
Gaus Width: 3.5891
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

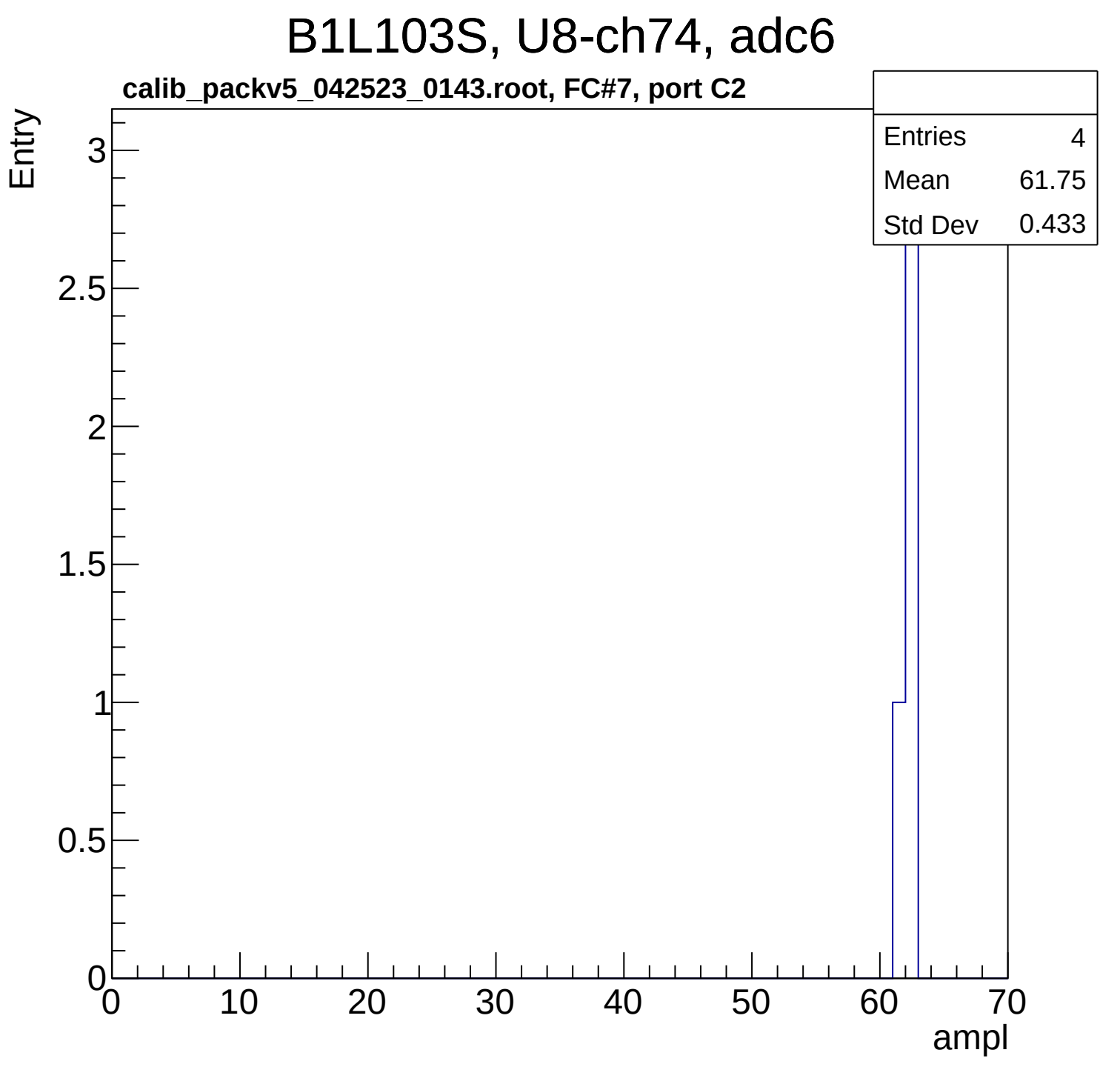

B1L103S, U8-ch74, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 37.4
Std Dev 4.007
Gaus mean : 38.4246
Gaus Width: 4.4994
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

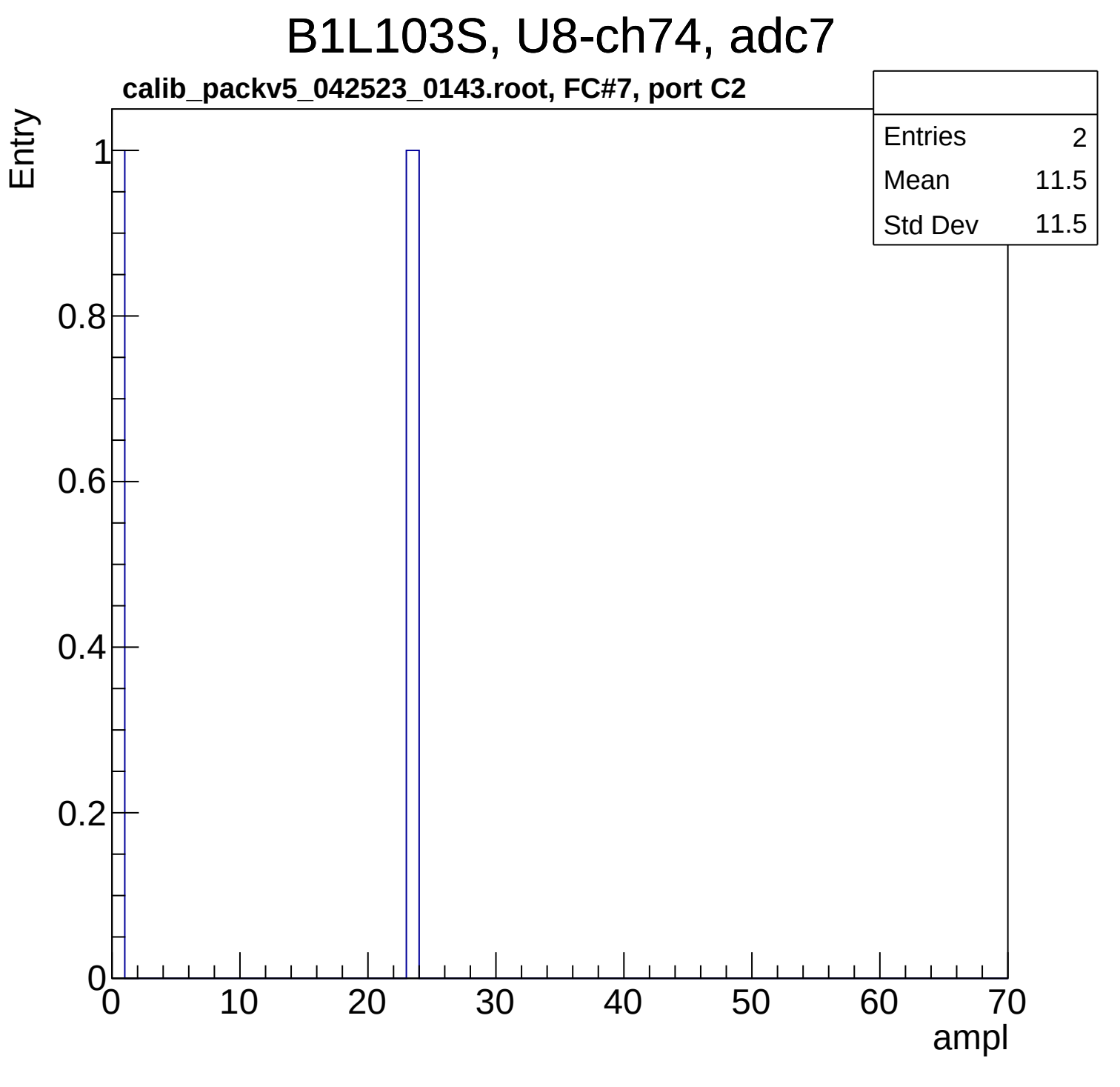

B1L103S, U8-ch74, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 43.59
Std Dev 3.647
Gaus mean : 44.1808
Gaus Width: 3.5681
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

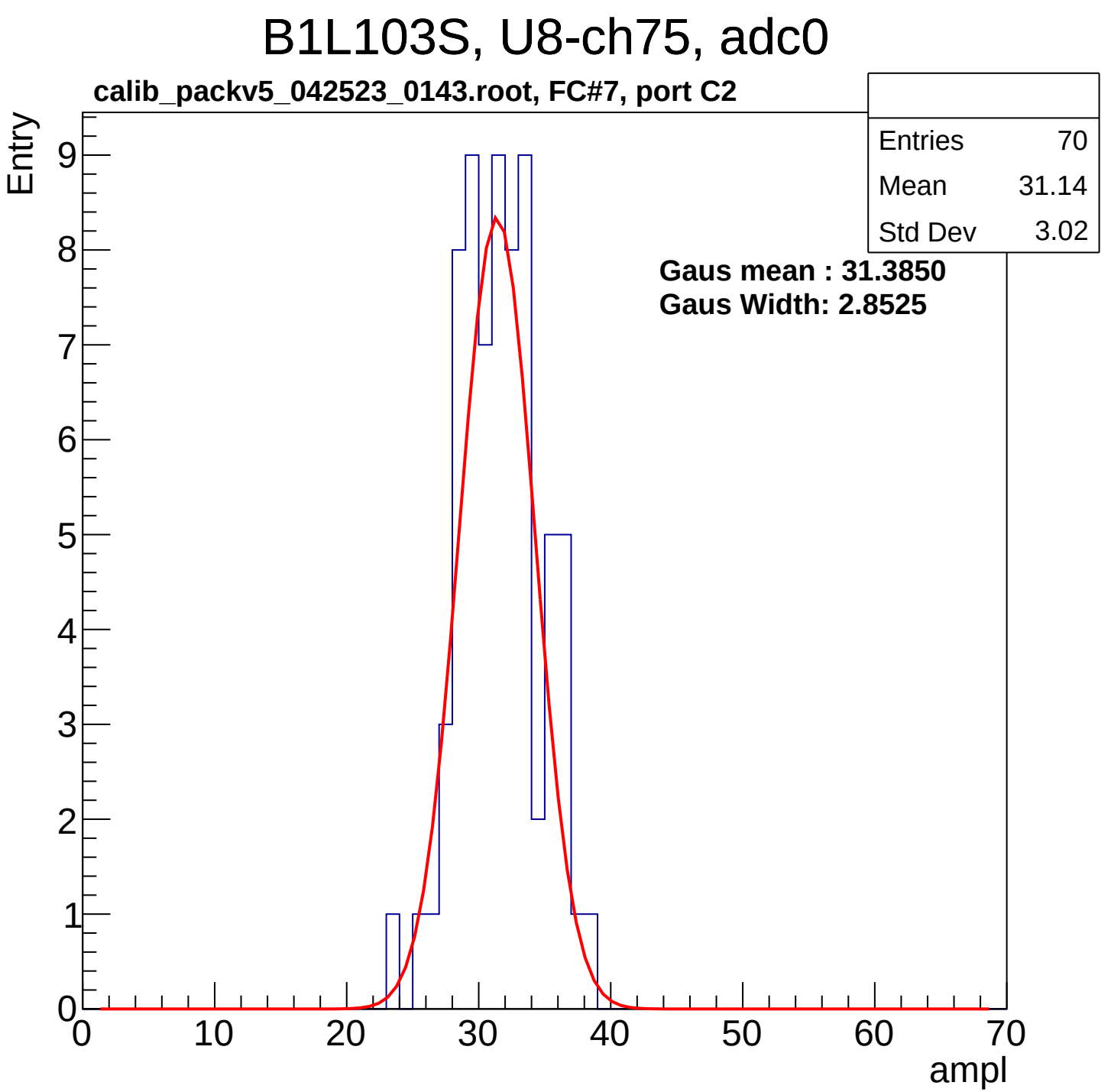

B1L103S, U8-ch74, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 79
Mean 49.67
Std Dev 3.528
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

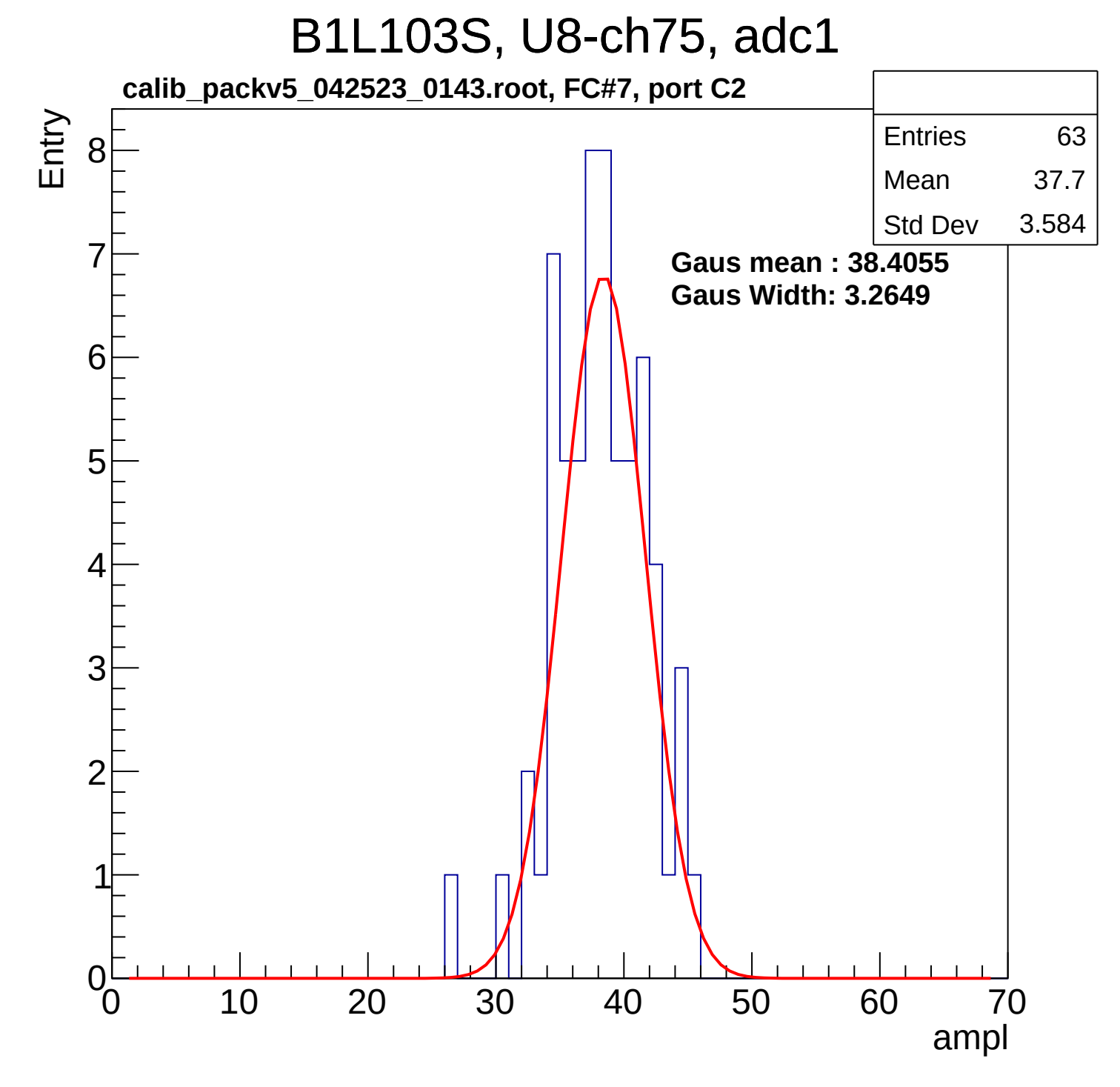

B1L103S, U8-ch74, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 56.82
Std Dev 2.942
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

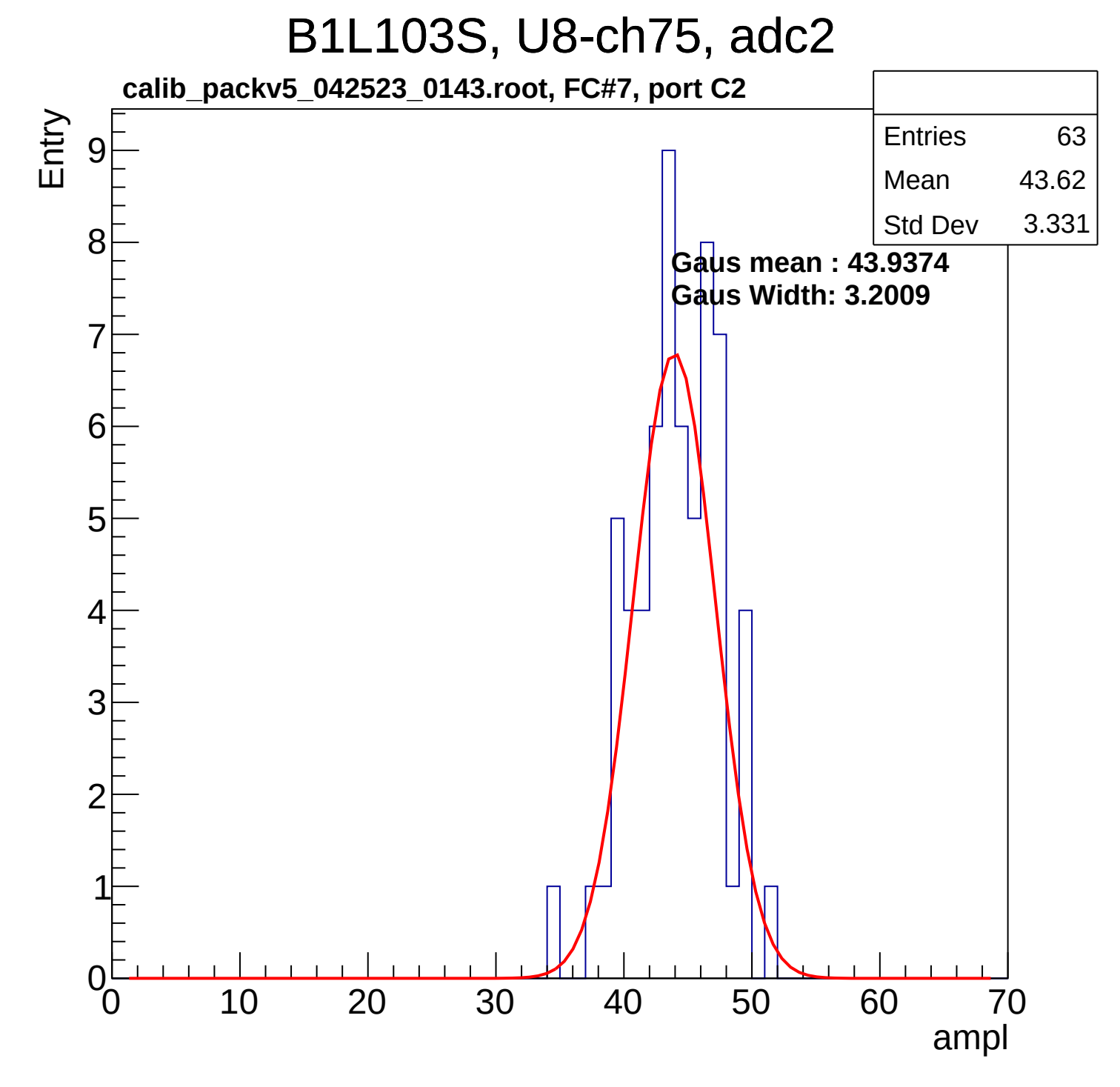

B1L103S, U8-ch74, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 41
Mean 58.83
Std Dev 9.566
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

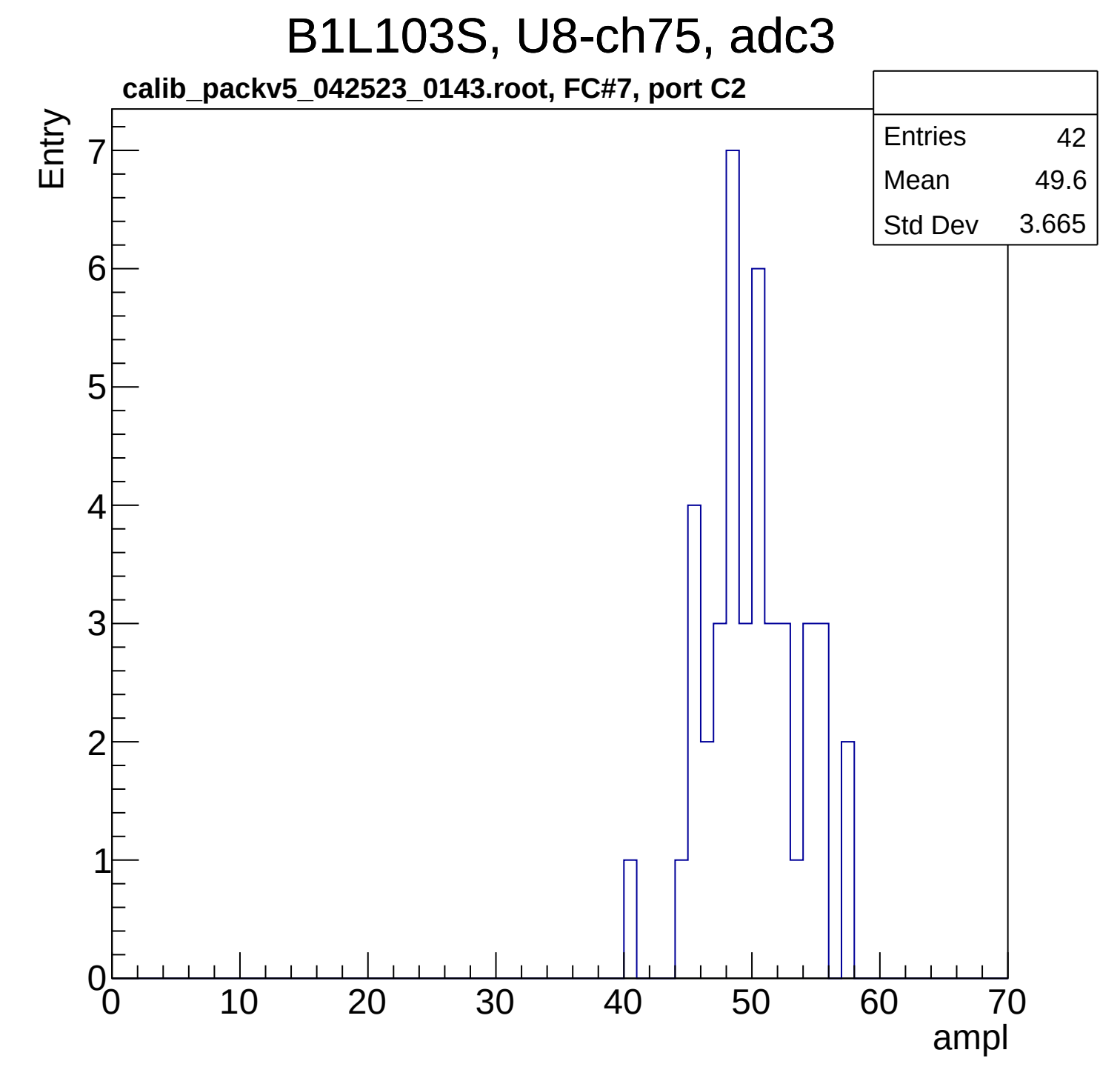

B1L103S, U8-ch74, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 61.75
Std Dev 0.433
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

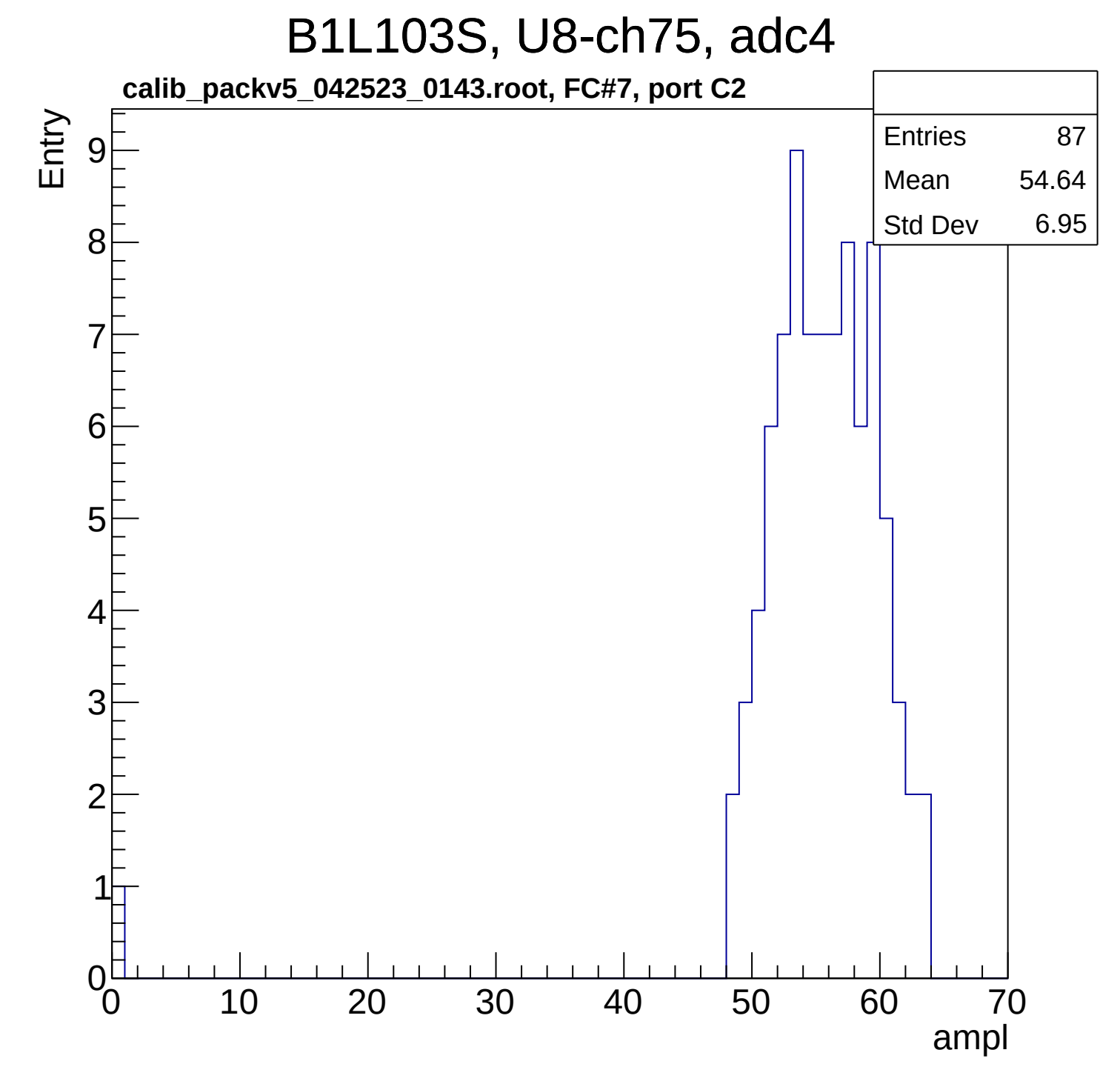

B1L103S, U8-ch74, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 11.5
Std Dev 11.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

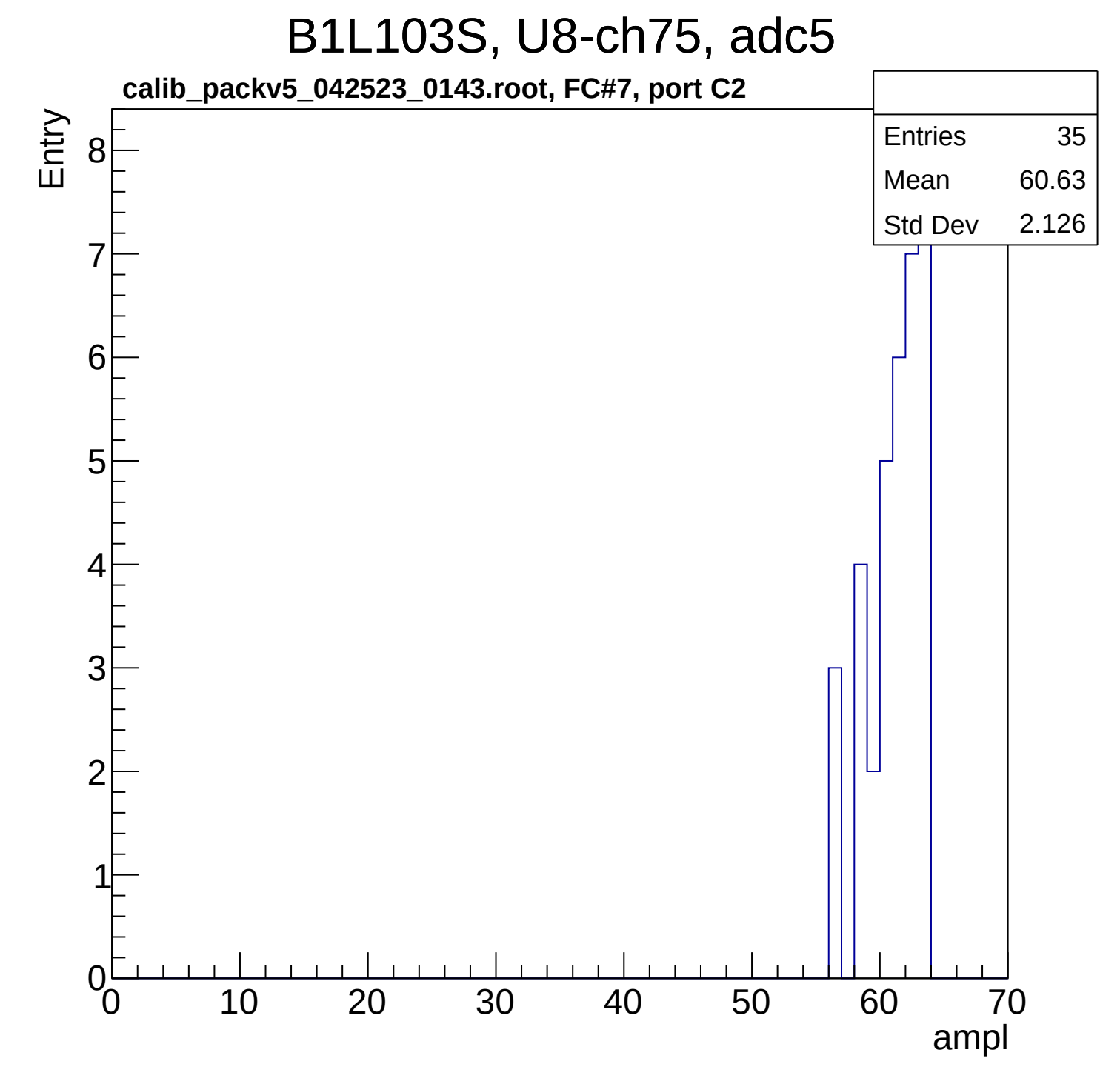

B1L103S, U8-ch75, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 31.14
Std Dev 3.02
Gaus mean : 31.3850
Gaus Width: 2.8525
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

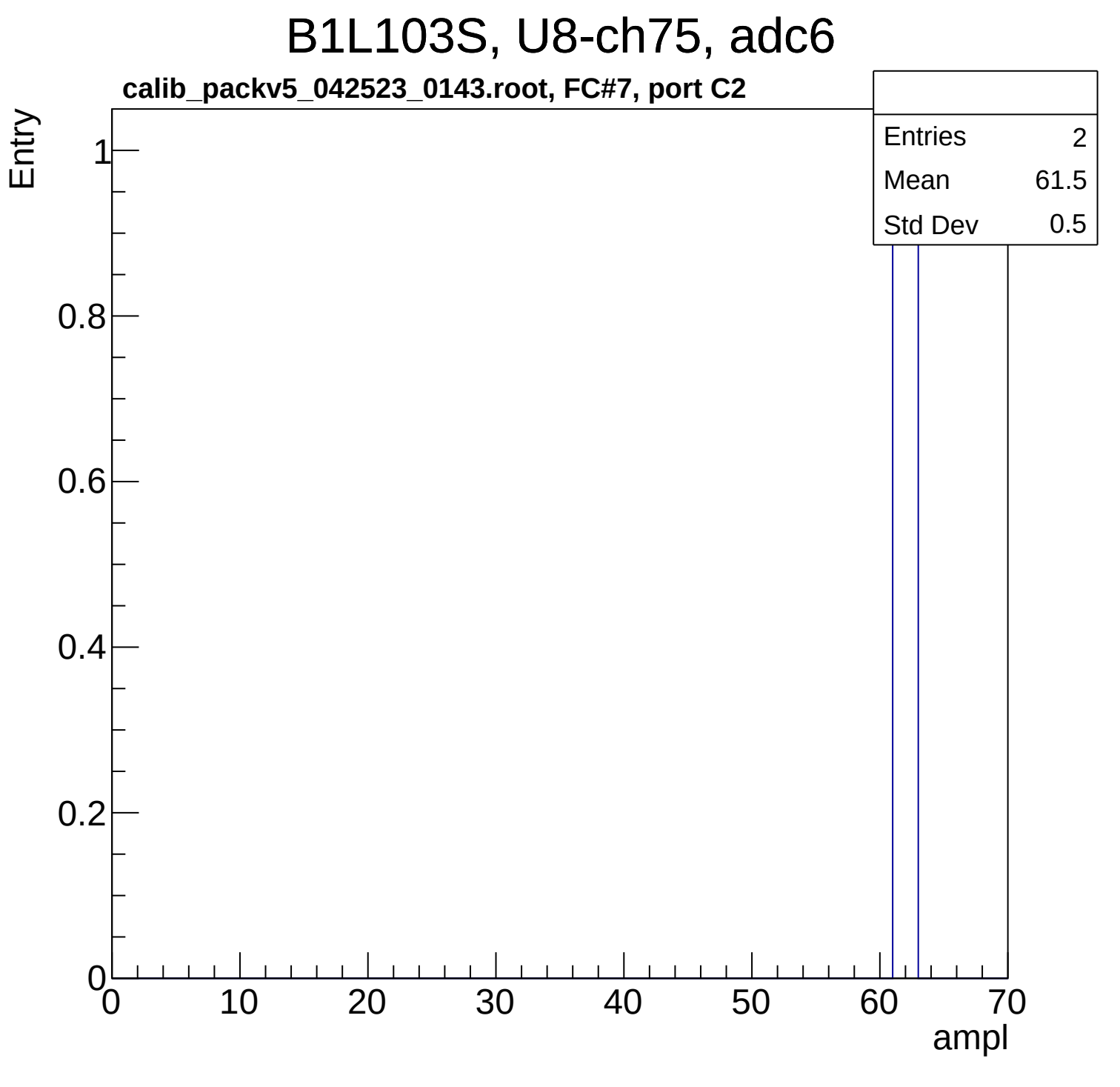

B1L103S, U8-ch75, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 37.7
Std Dev 3.584
Gaus mean : 38.4055
Gaus Width: 3.2649
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

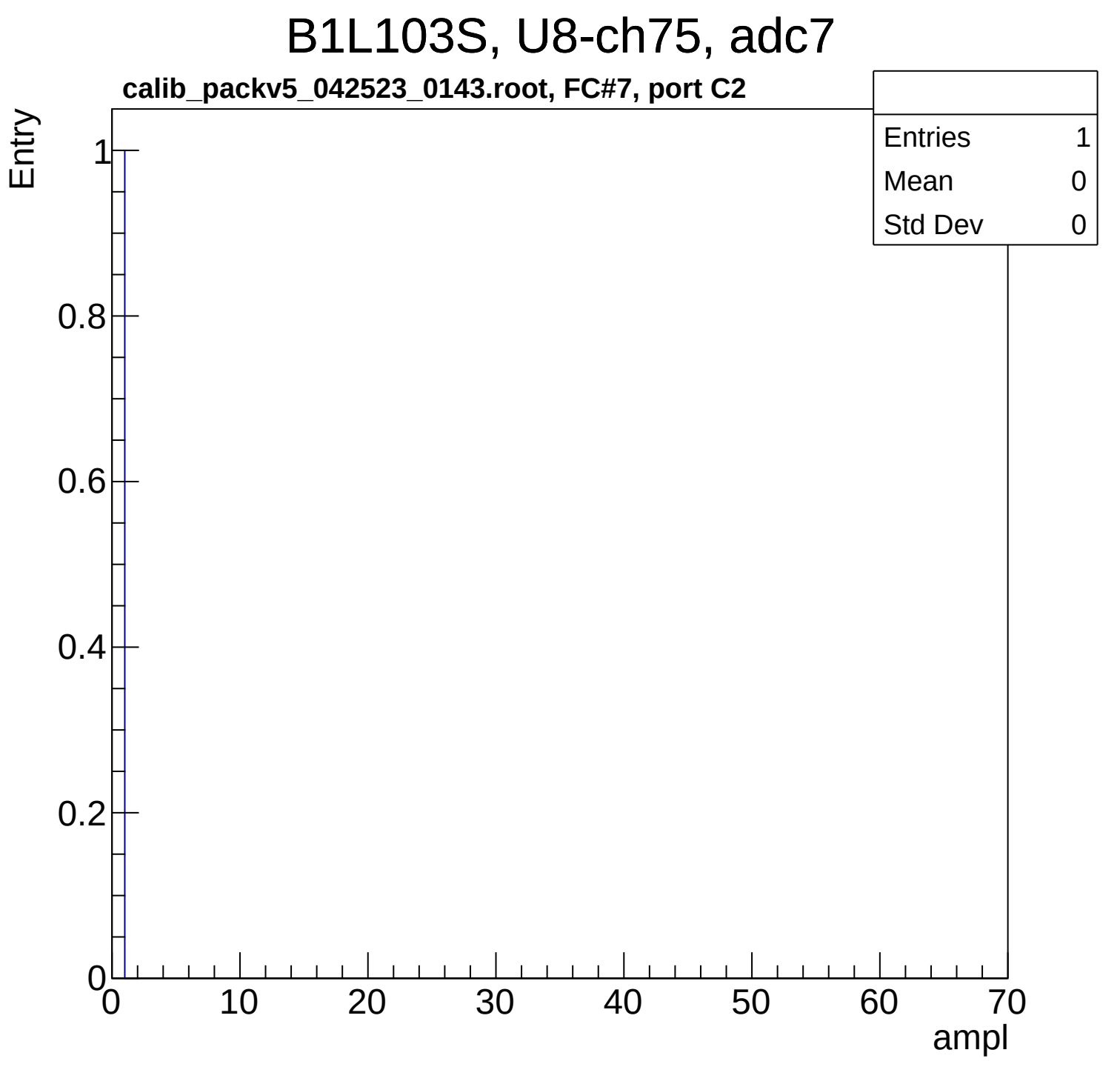

B1L103S, U8-ch75, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 43.62
Std Dev 3.331
Gaus mean : 43.9374
Gaus Width: 3.2009
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

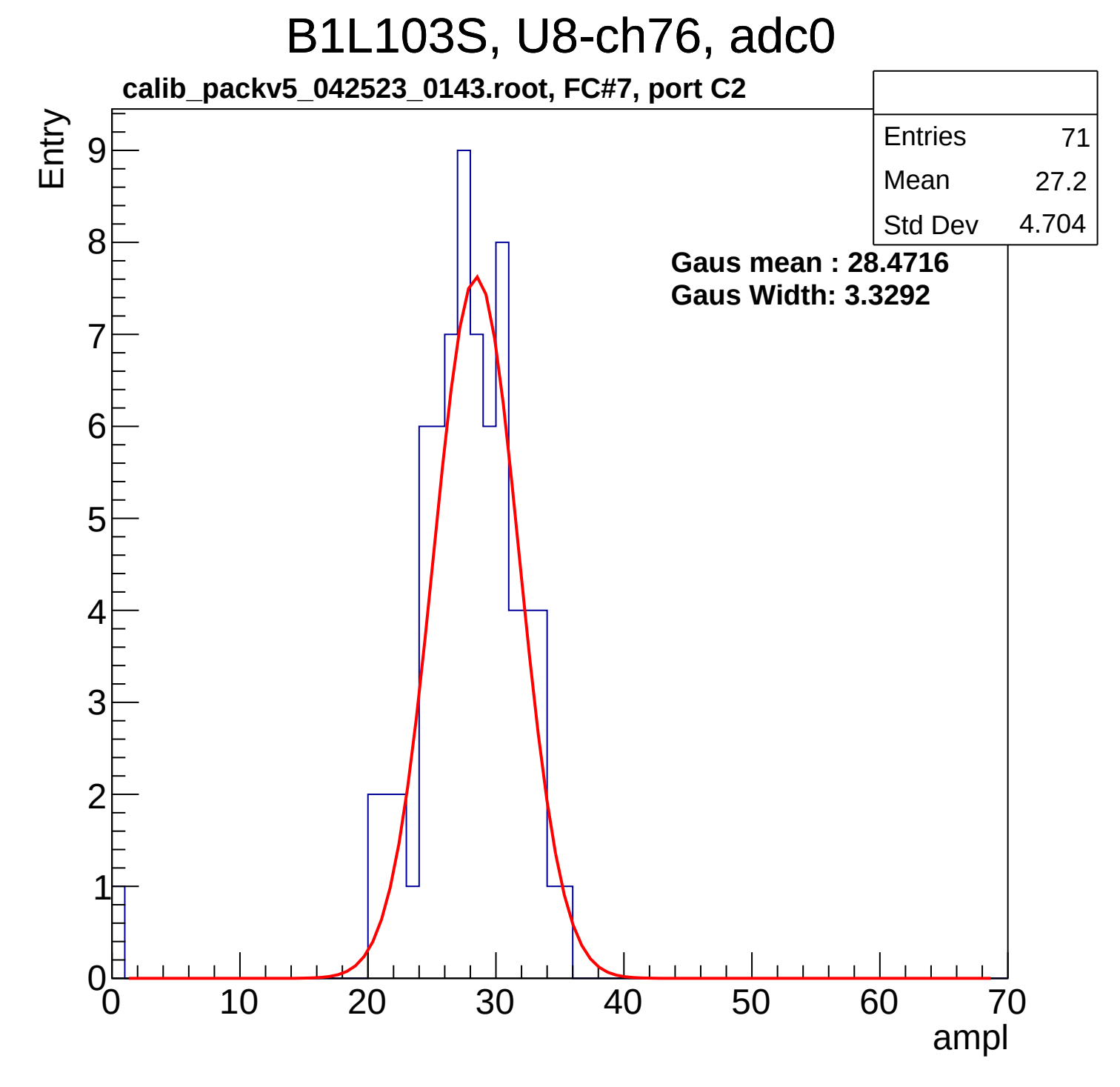

B1L103S, U8-ch75, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 42
Mean 49.6
Std Dev 3.665
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

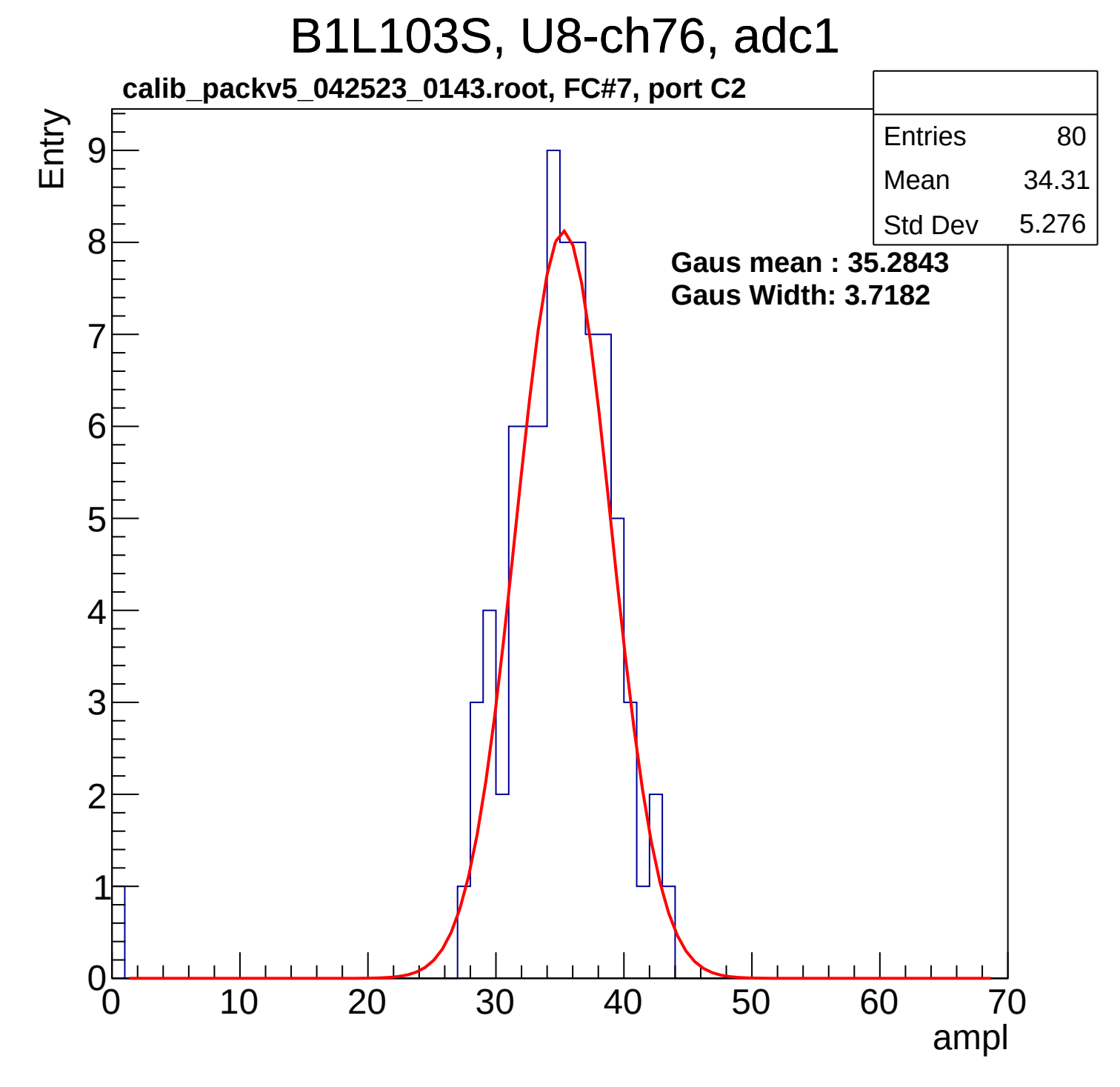

B1L103S, U8-ch75, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 87
Mean 54.64
Std Dev 6.95
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

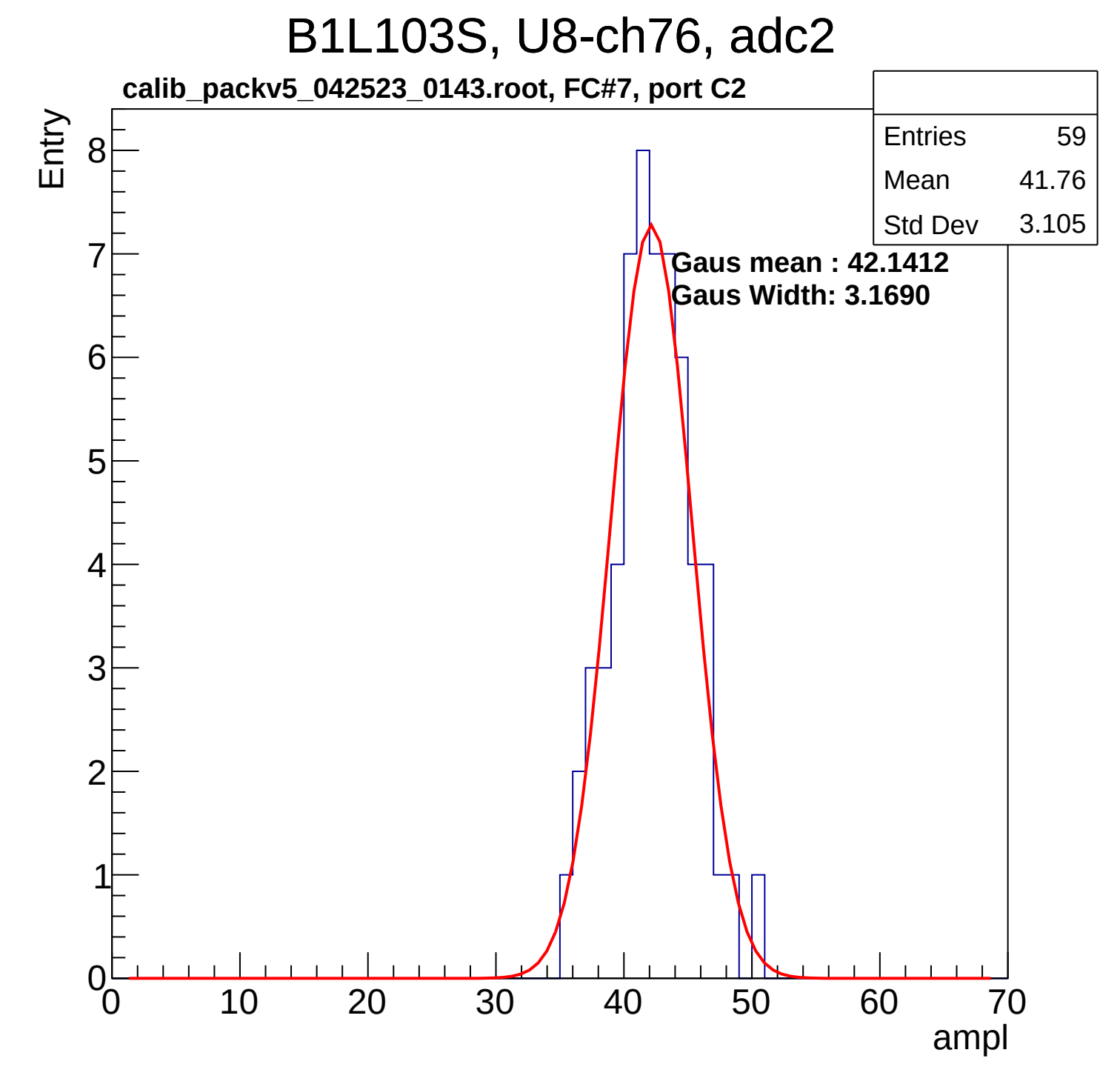

B1L103S, U8-ch75, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 35
Mean 60.63
Std Dev 2.126
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

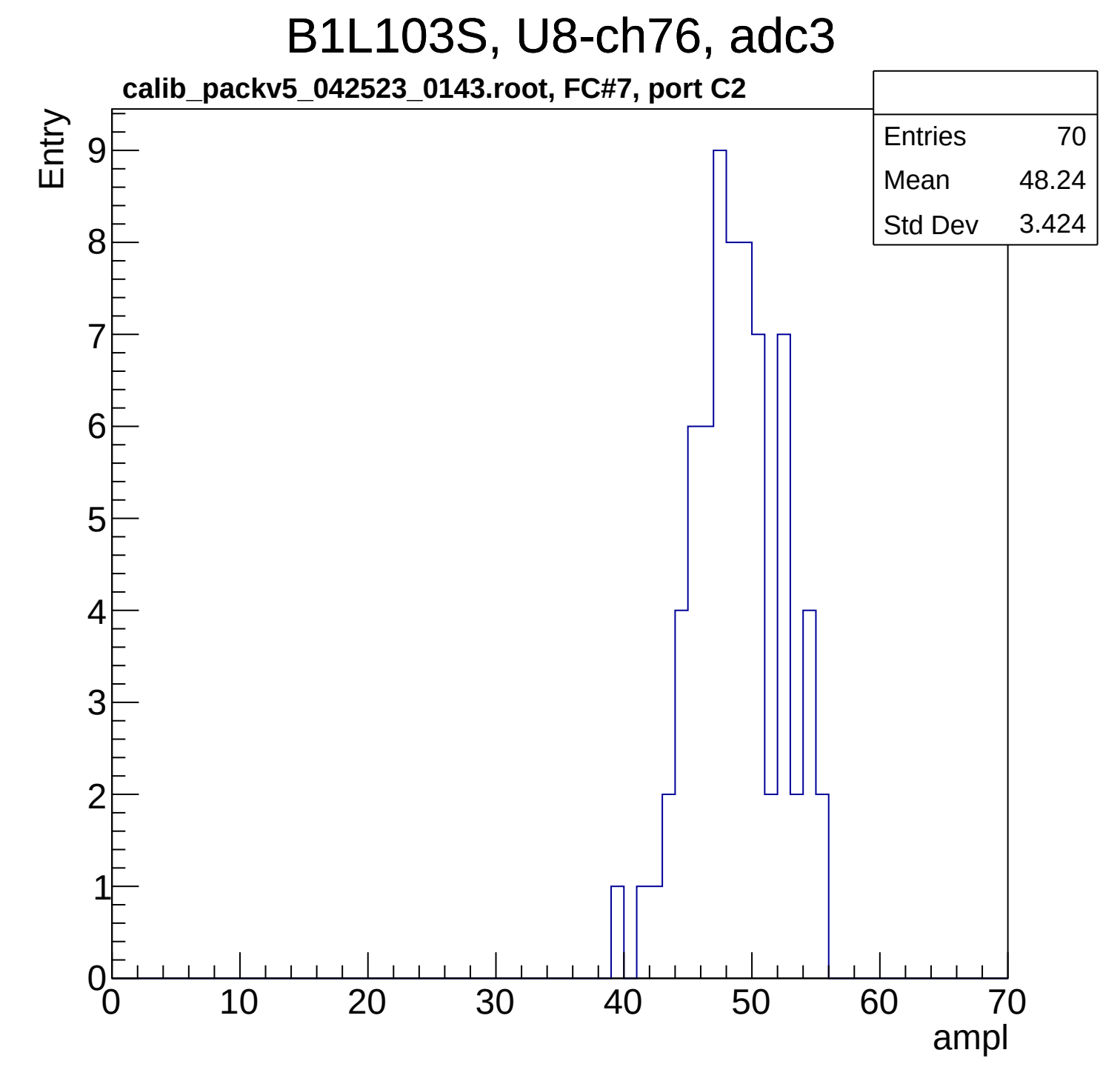

B1L103S, U8-ch75, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 61.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

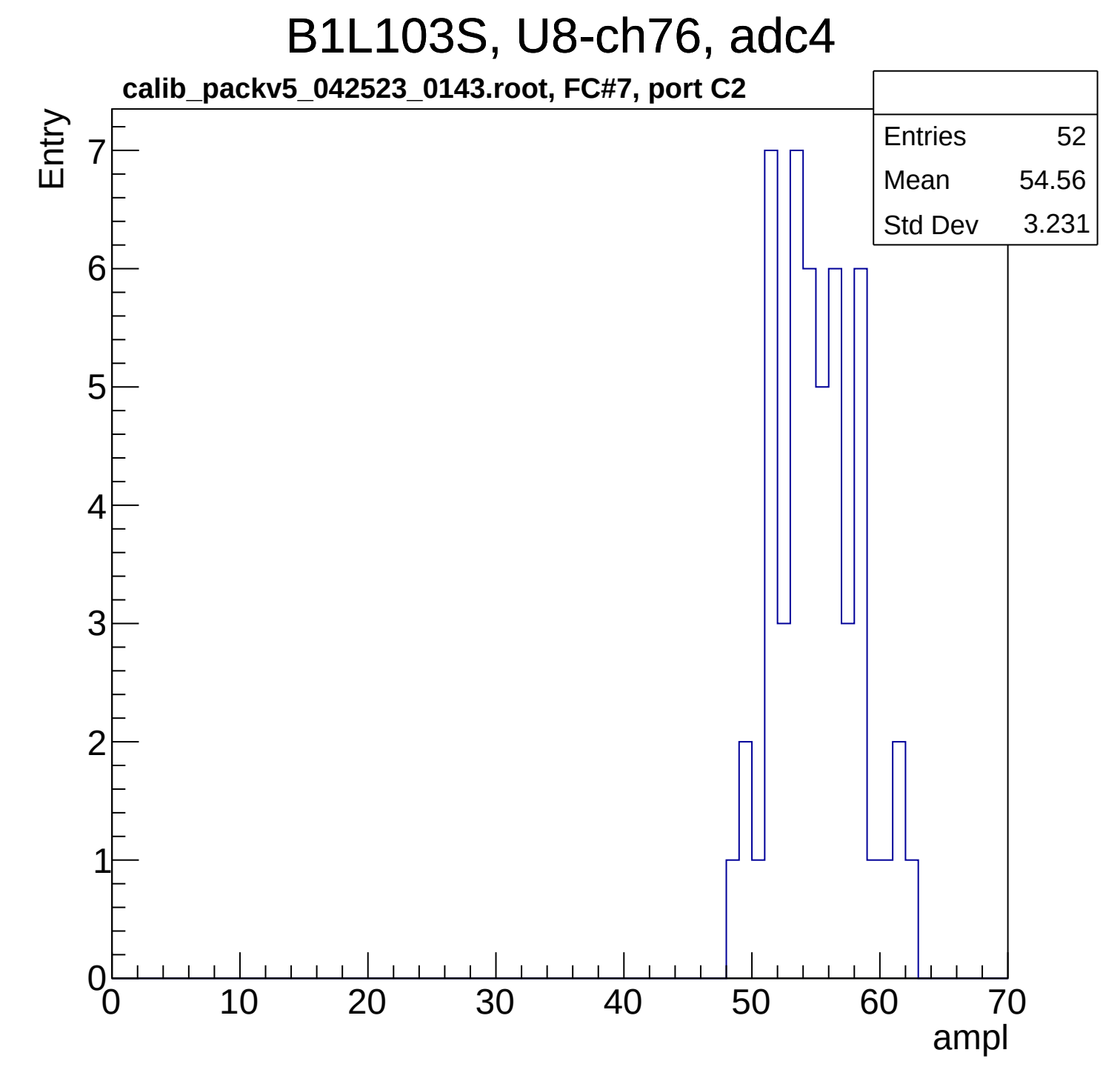

B1L103S, U8-ch75, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

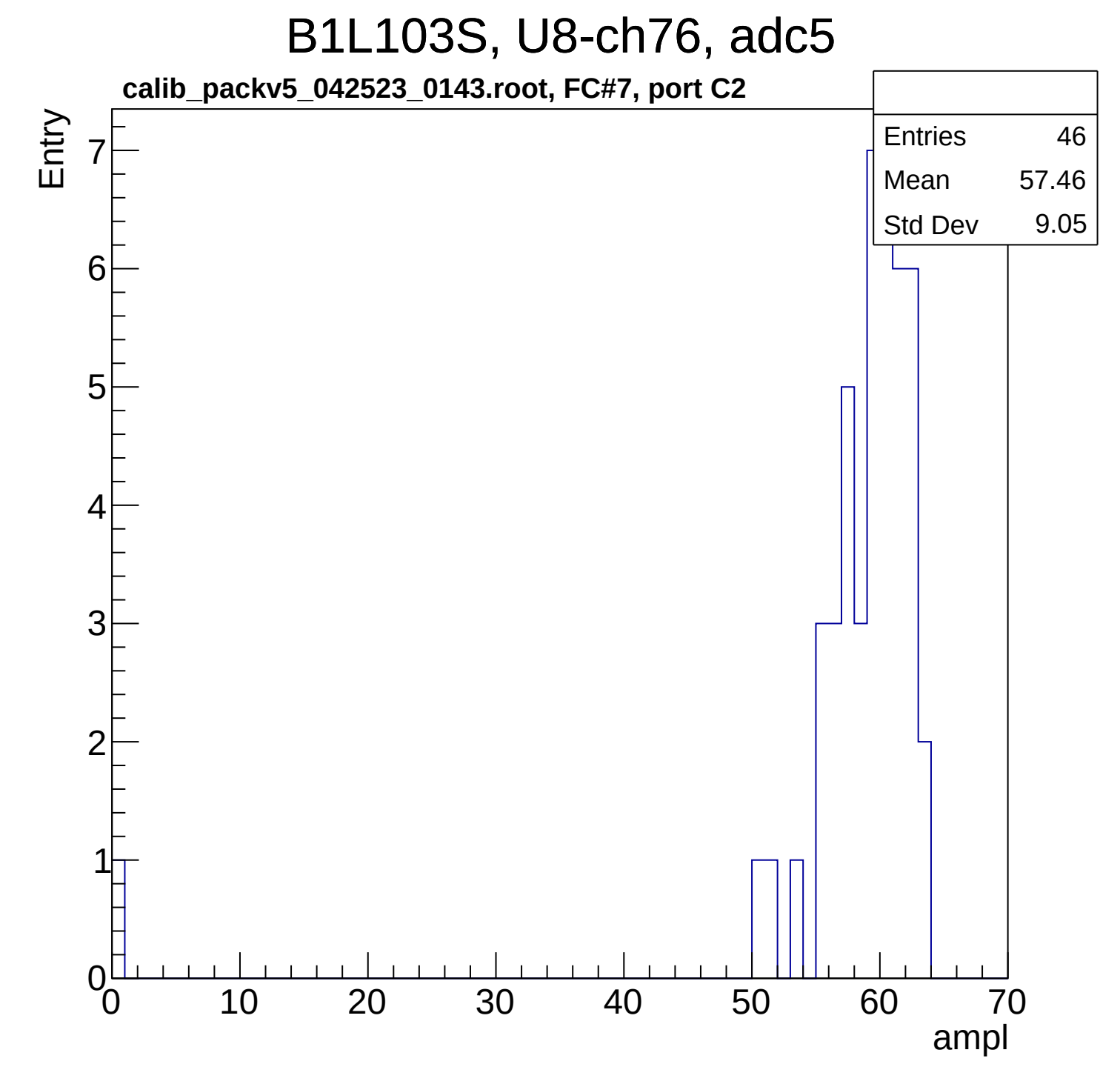

B1L103S, U8-ch76, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 27.2
Std Dev 4.704
Gaus mean : 28.4716
Gaus Width: 3.3292
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

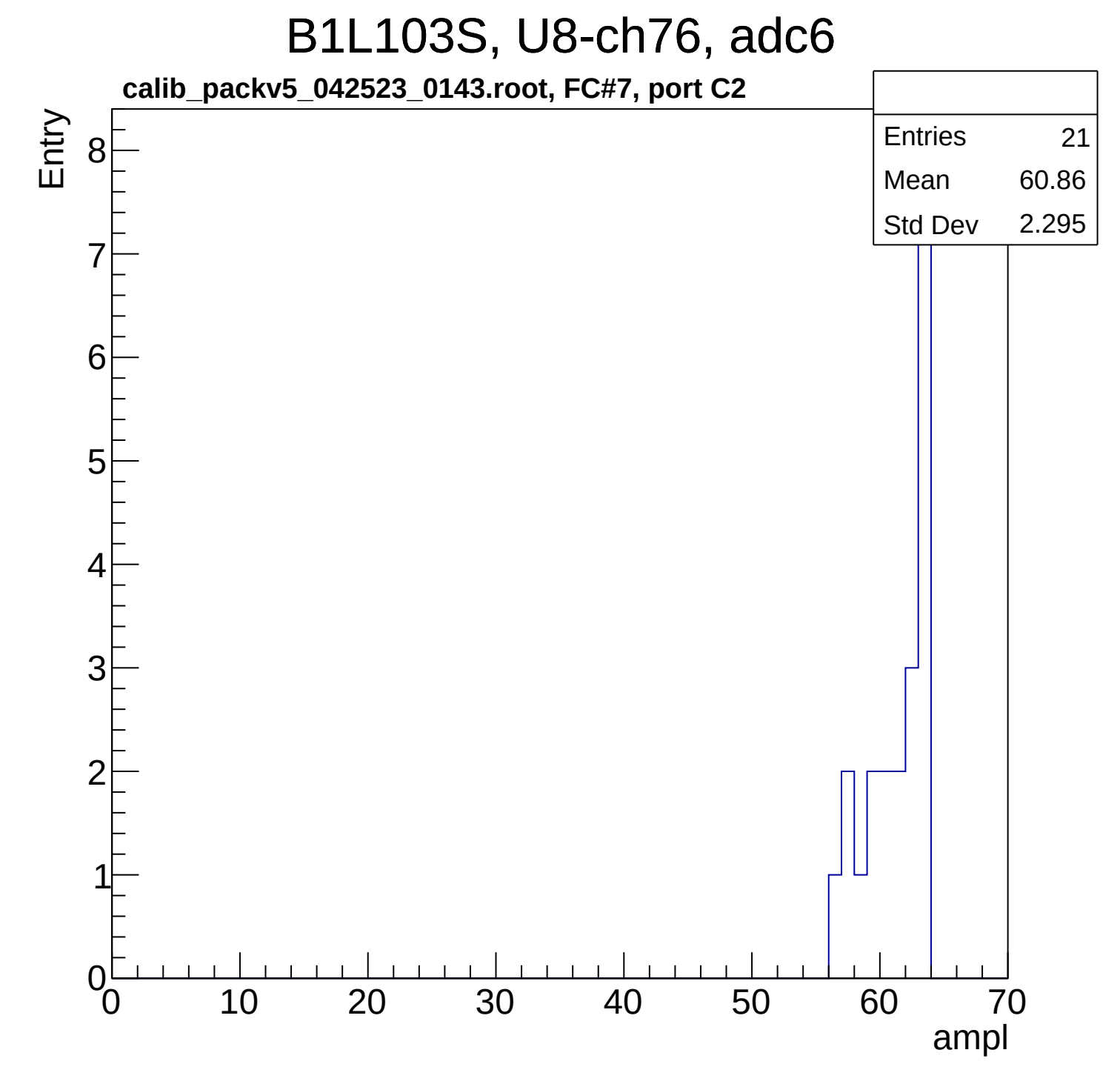

B1L103S, U8-ch76, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 80
Mean 34.31
Std Dev 5.276
Gaus mean : 35.2843
Gaus Width: 3.7182
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

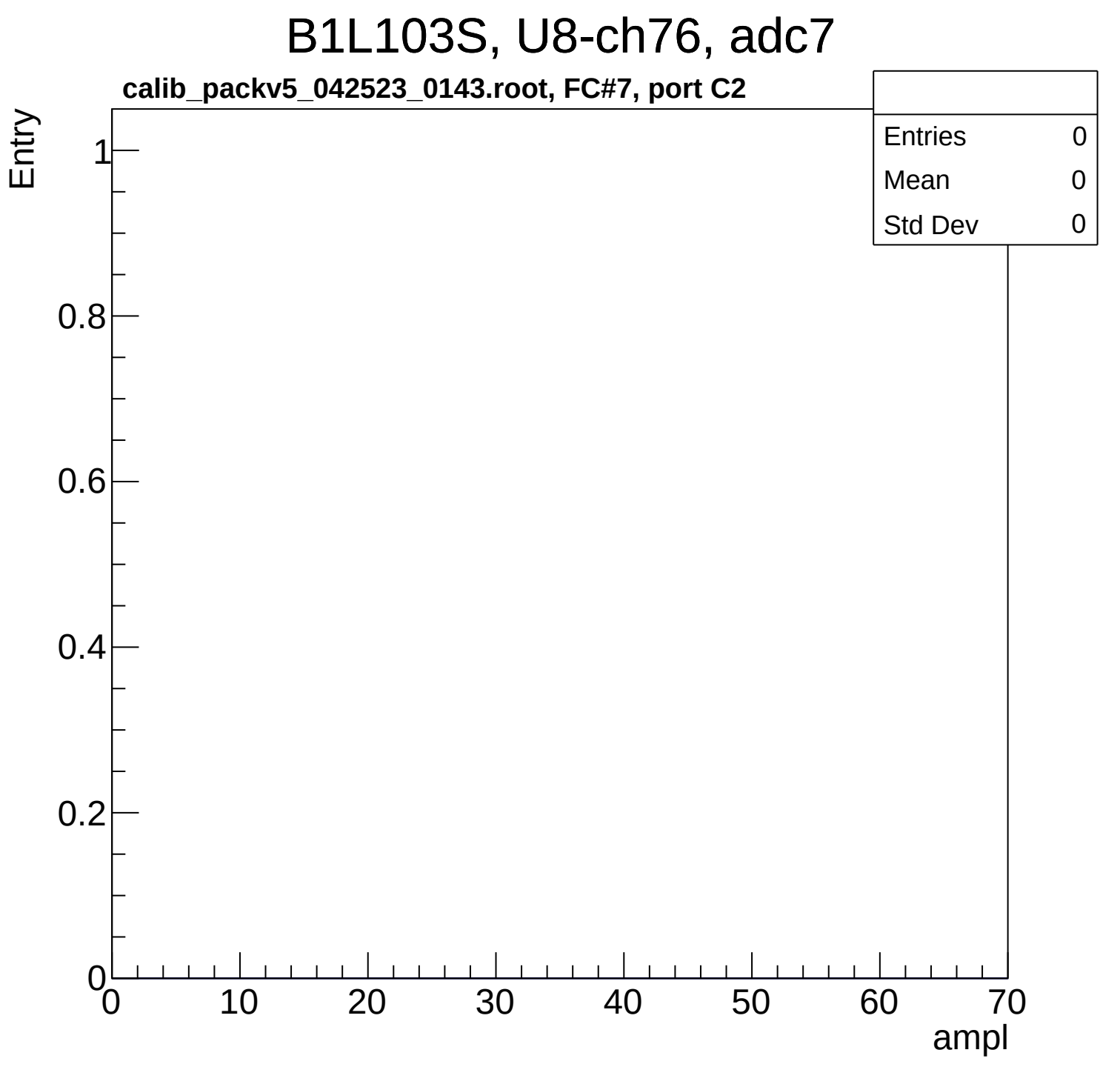

B1L103S, U8-ch76, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 41.76
Std Dev 3.105
Gaus mean : 42.1412
Gaus Width: 3.1690
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

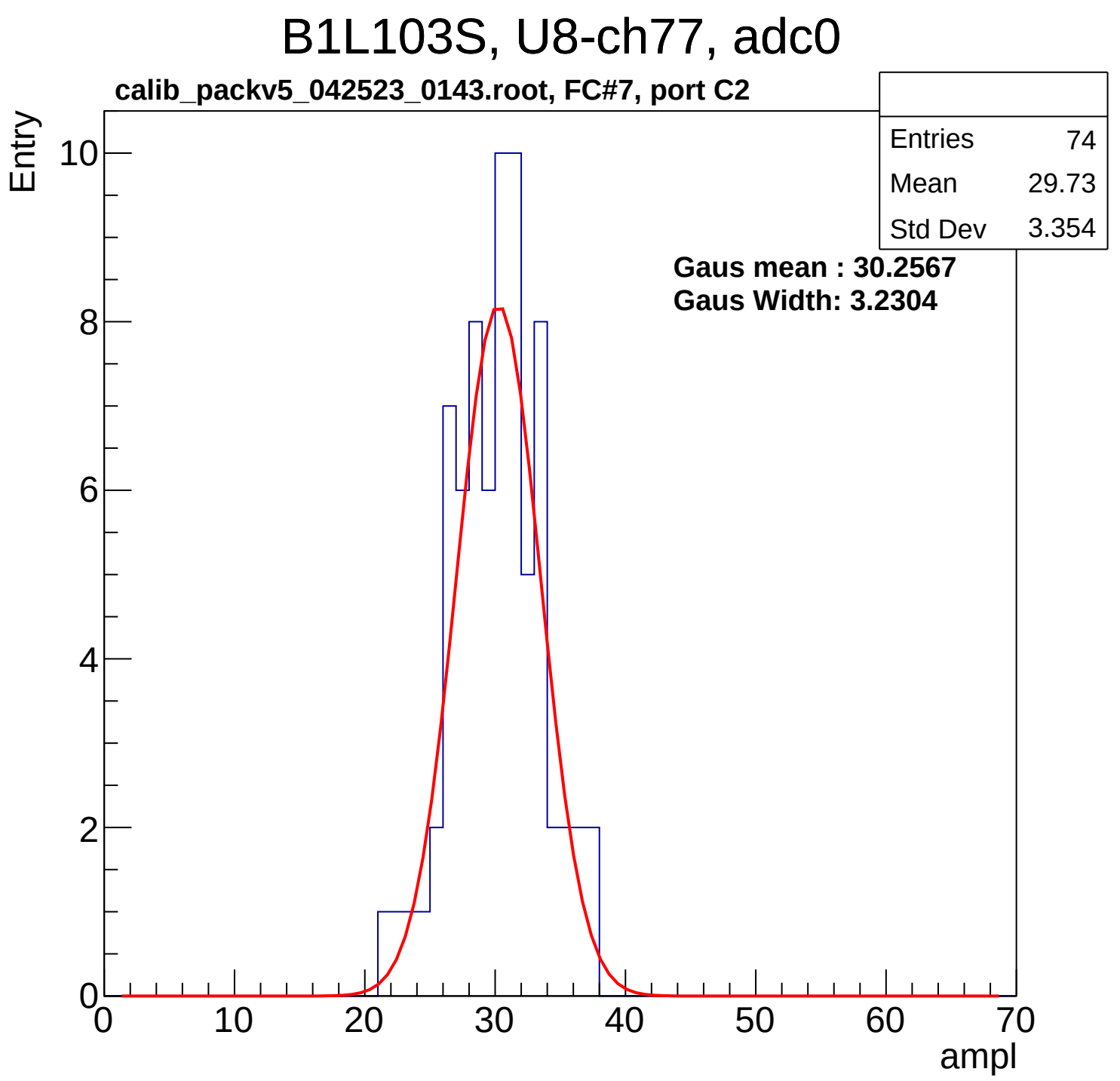

B1L103S, U8-ch76, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 48.24
Std Dev 3.424
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

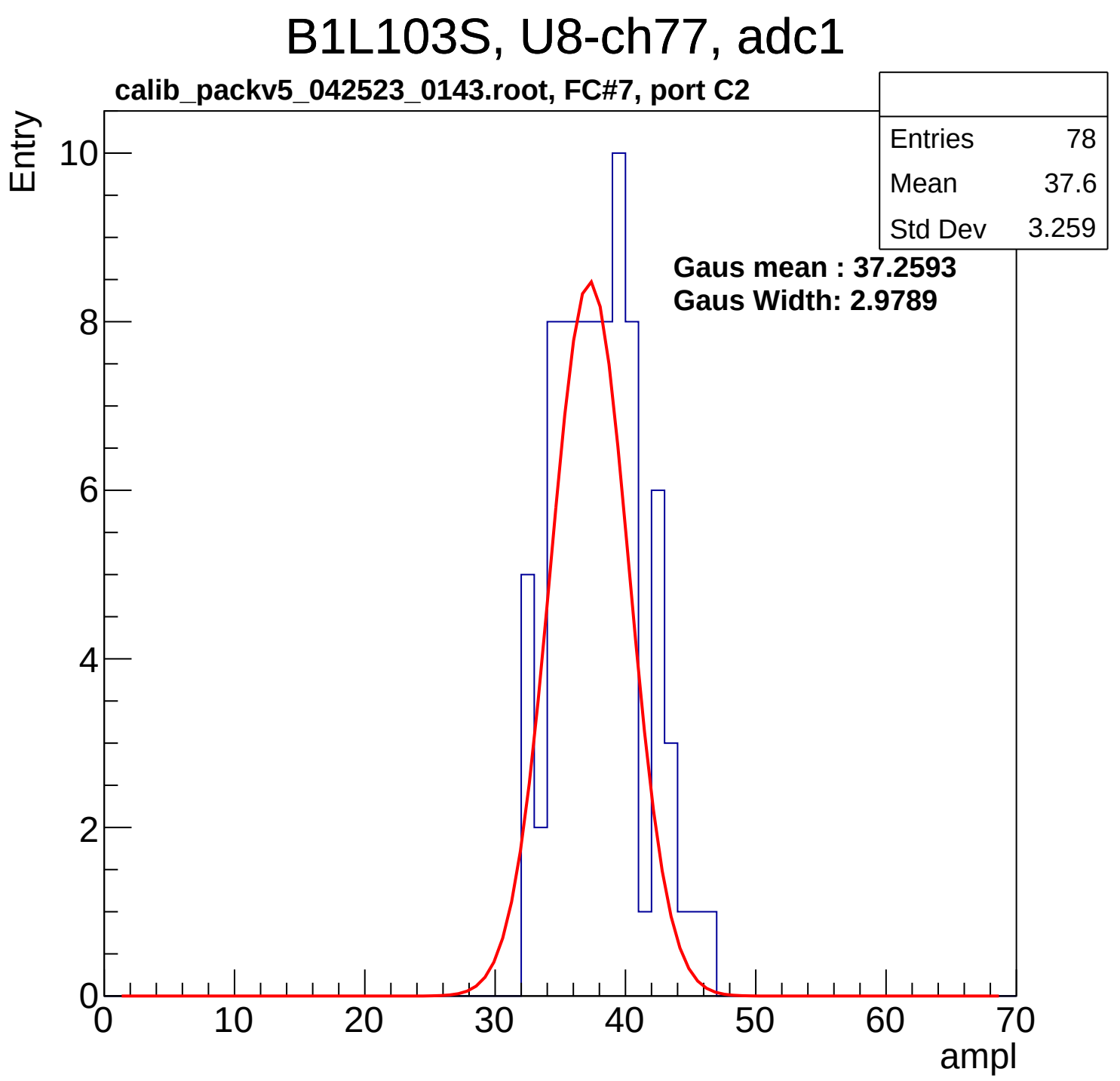

B1L103S, U8-ch76, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 54.56
Std Dev 3.231
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

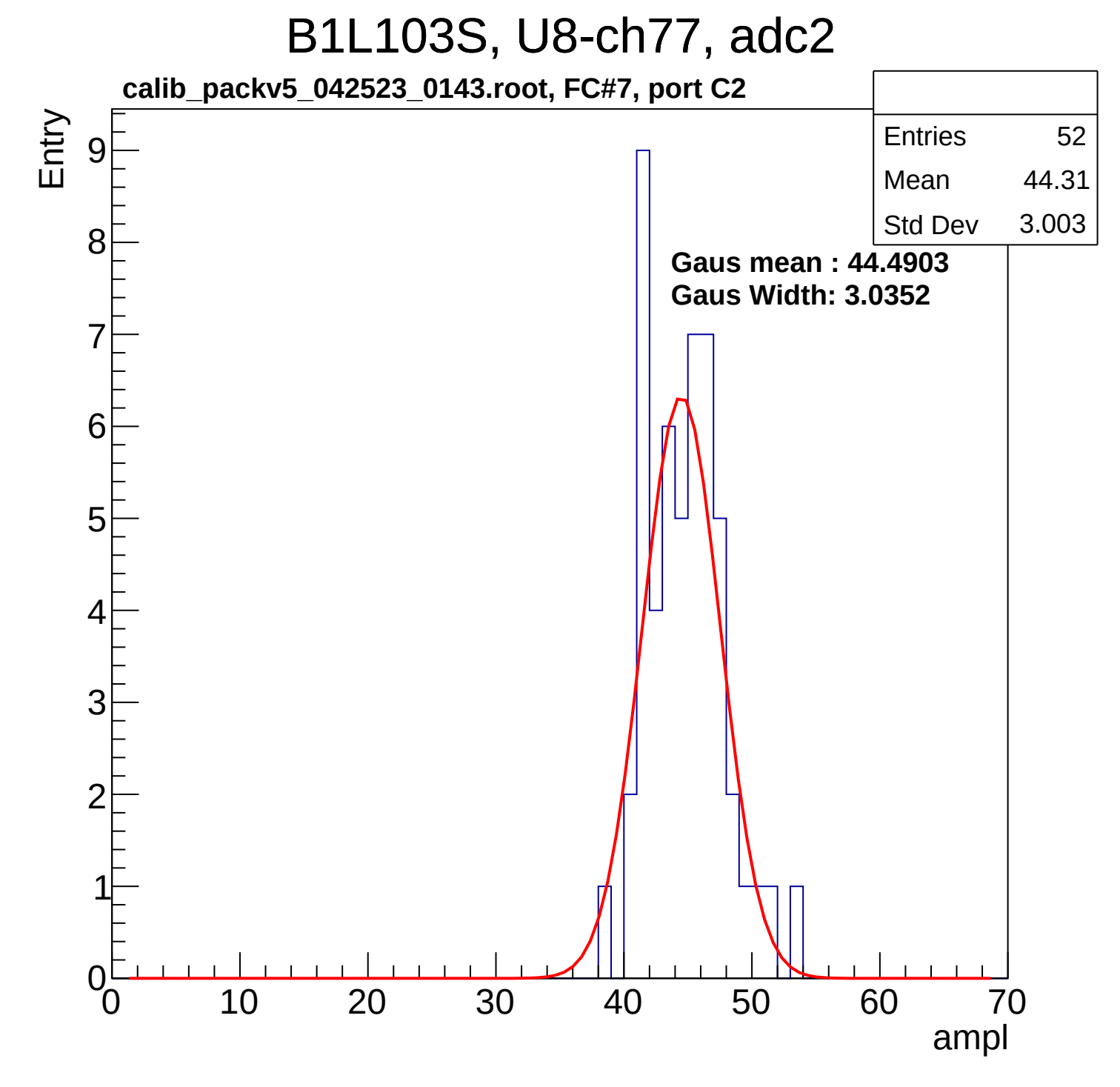

B1L103S, U8-ch76, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 46
Mean 57.46
Std Dev 9.05
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

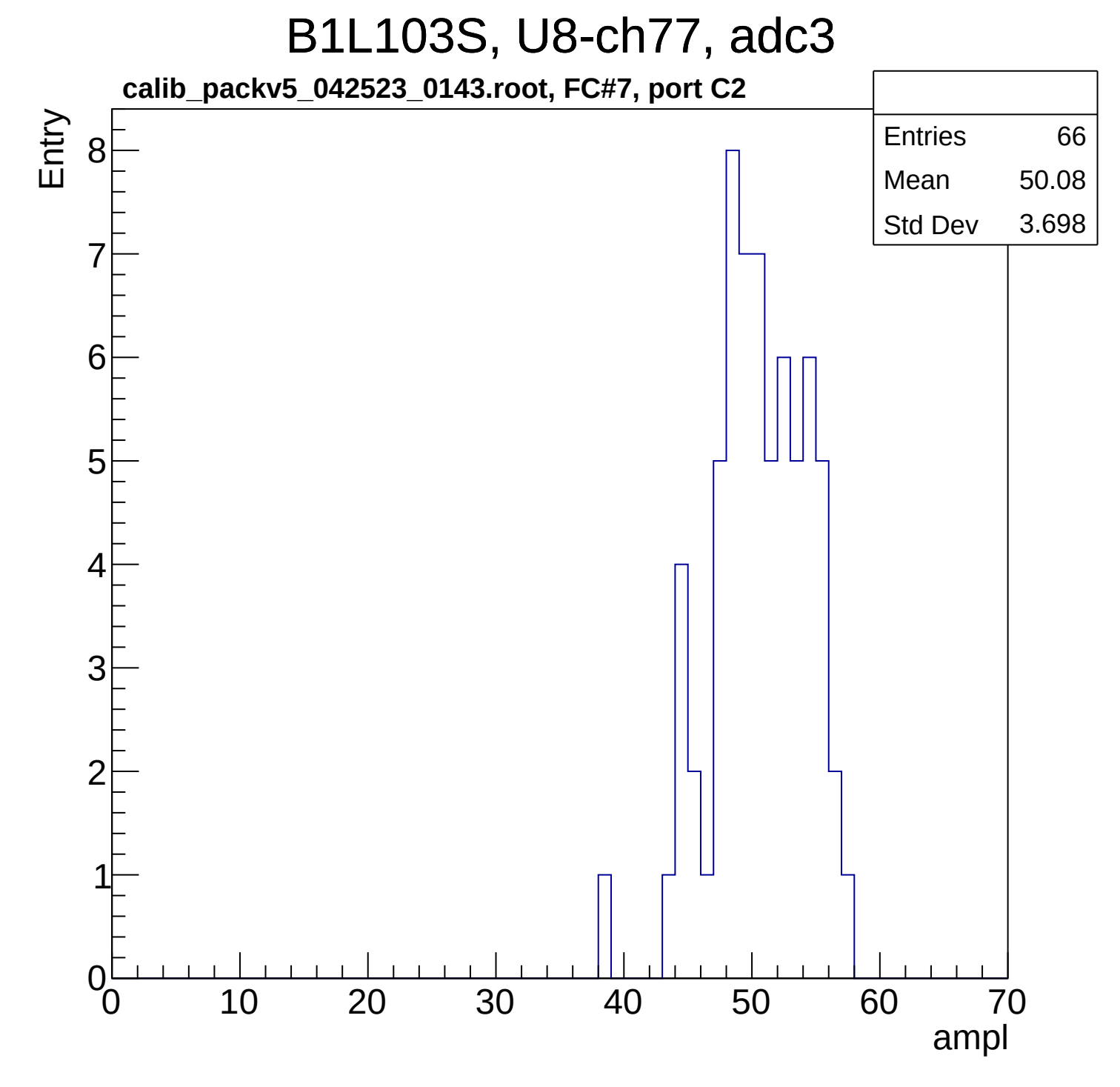

B1L103S, U8-ch76, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 21
Mean 60.86
Std Dev 2.295
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

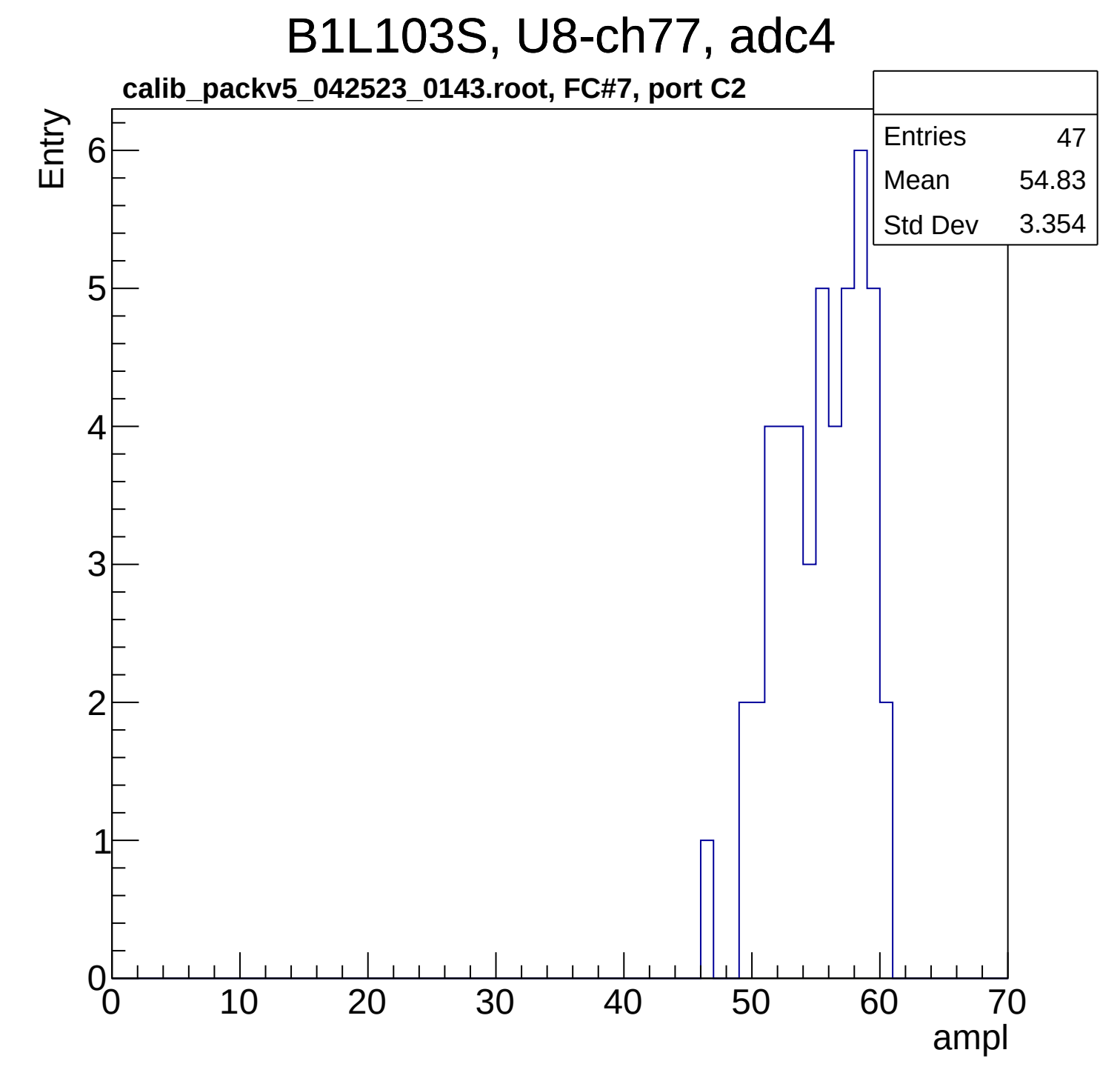

B1L103S, U8-ch76, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

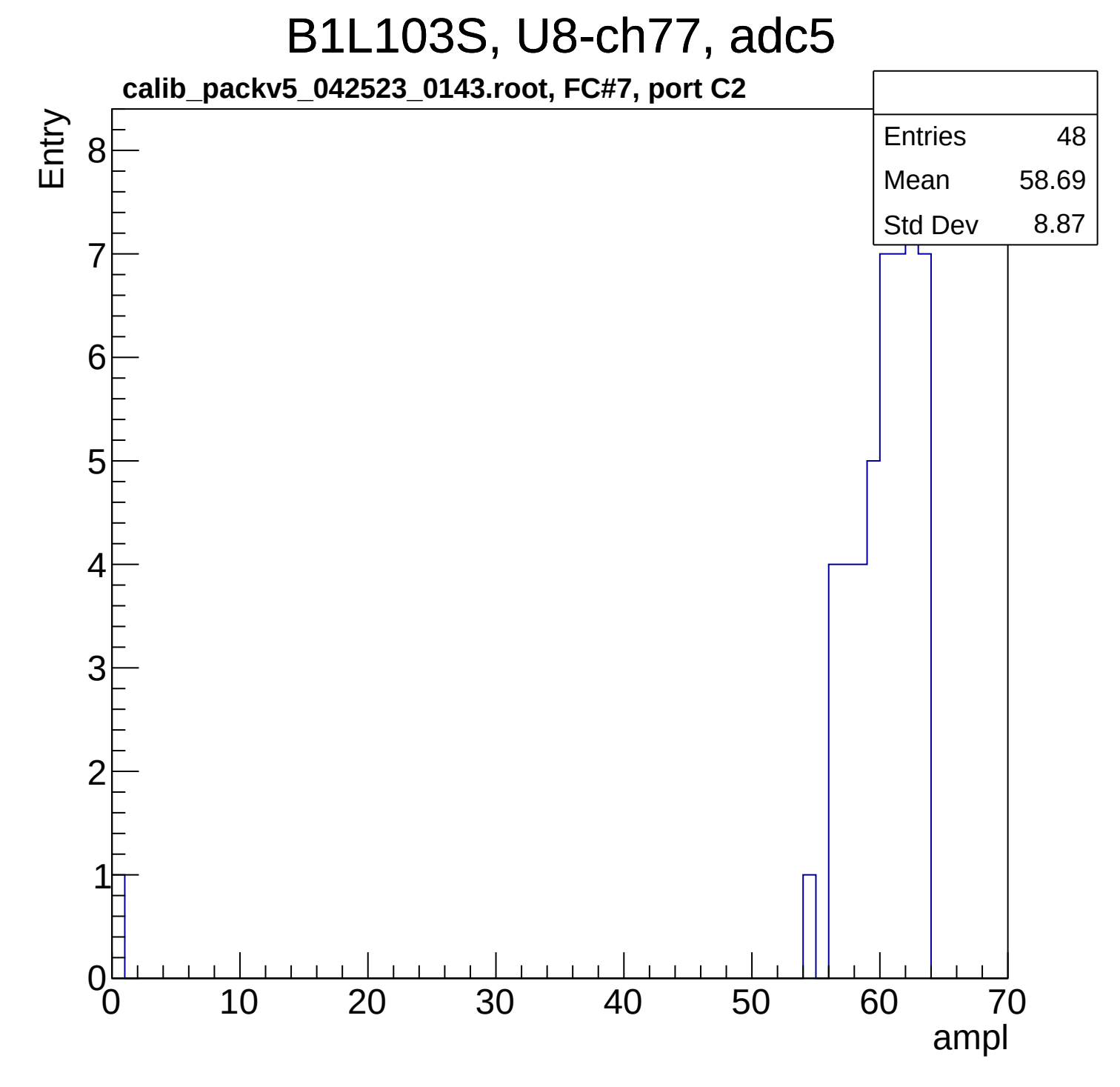

B1L103S, U8-ch77, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 29.73
Std Dev 3.354
Gaus mean : 30.2567
Gaus Width: 3.2304
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

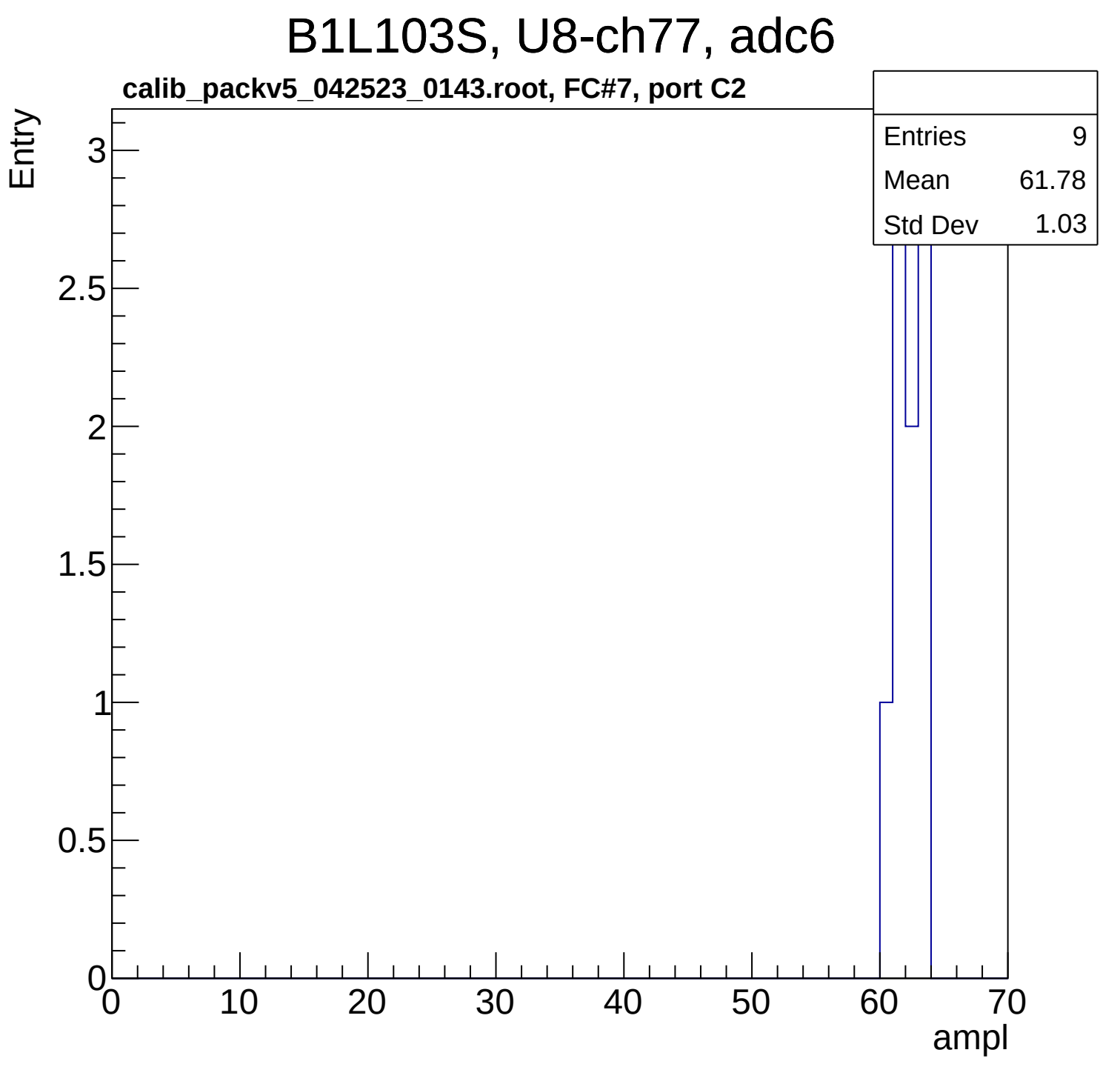

B1L103S, U8-ch77, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 78
Mean 37.6
Std Dev 3.259
Gaus mean : 37.2593
Gaus Width: 2.9789
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

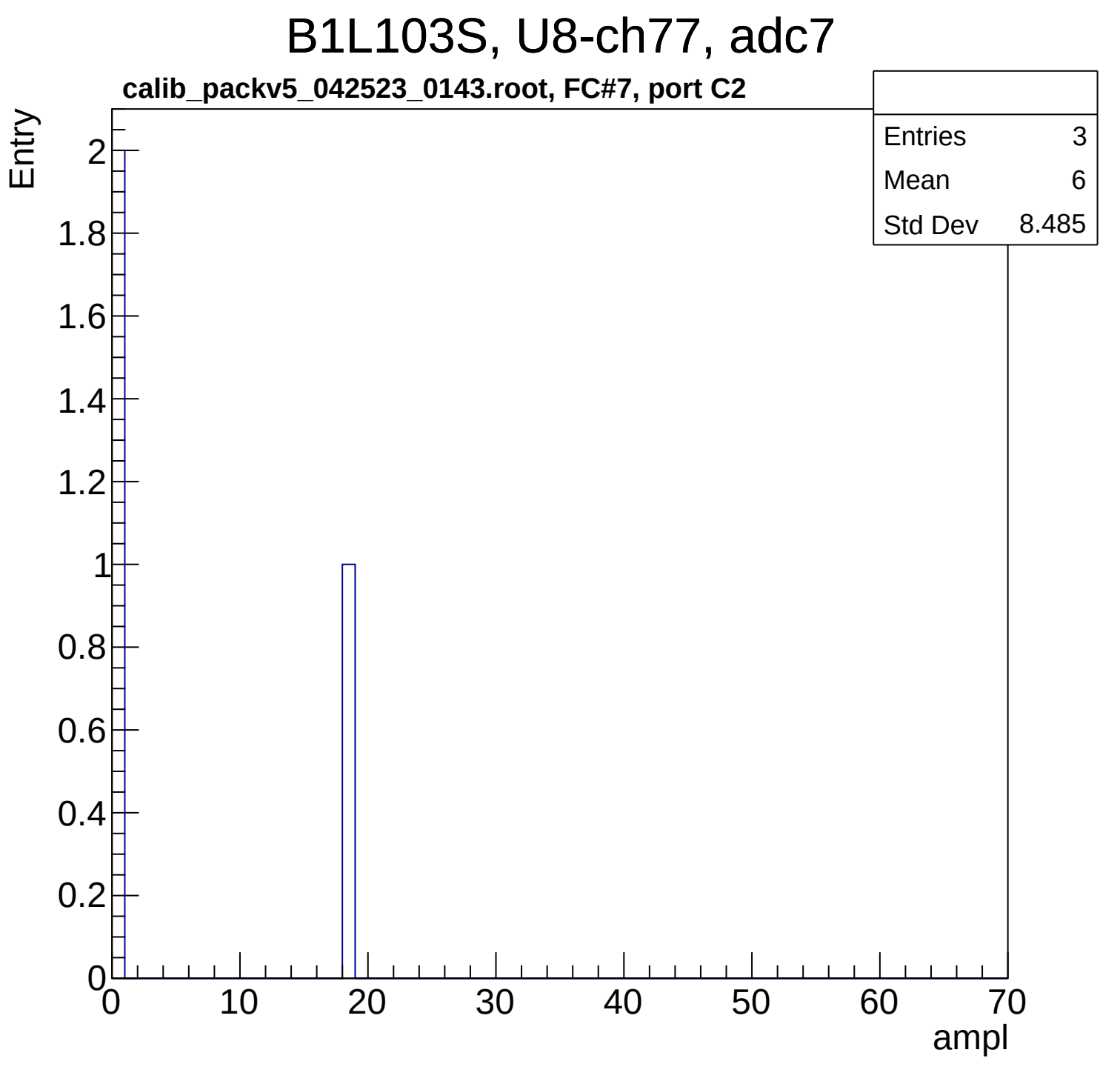

B1L103S, U8-ch77, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 44.31
Std Dev 3.003
Gaus mean : 44.4903
Gaus Width: 3.0352
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

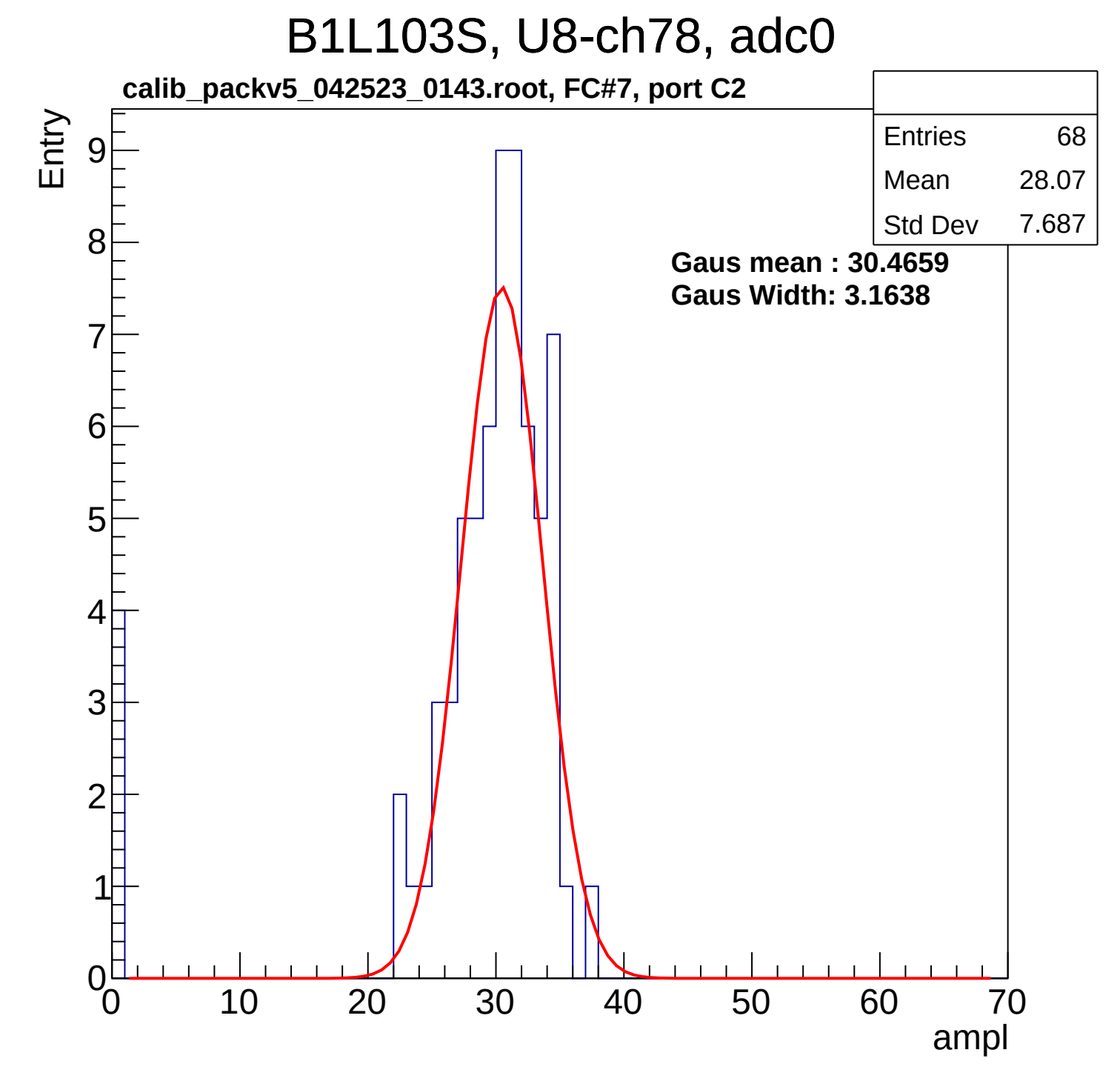

B1L103S, U8-ch77, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 50.08
Std Dev 3.698
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

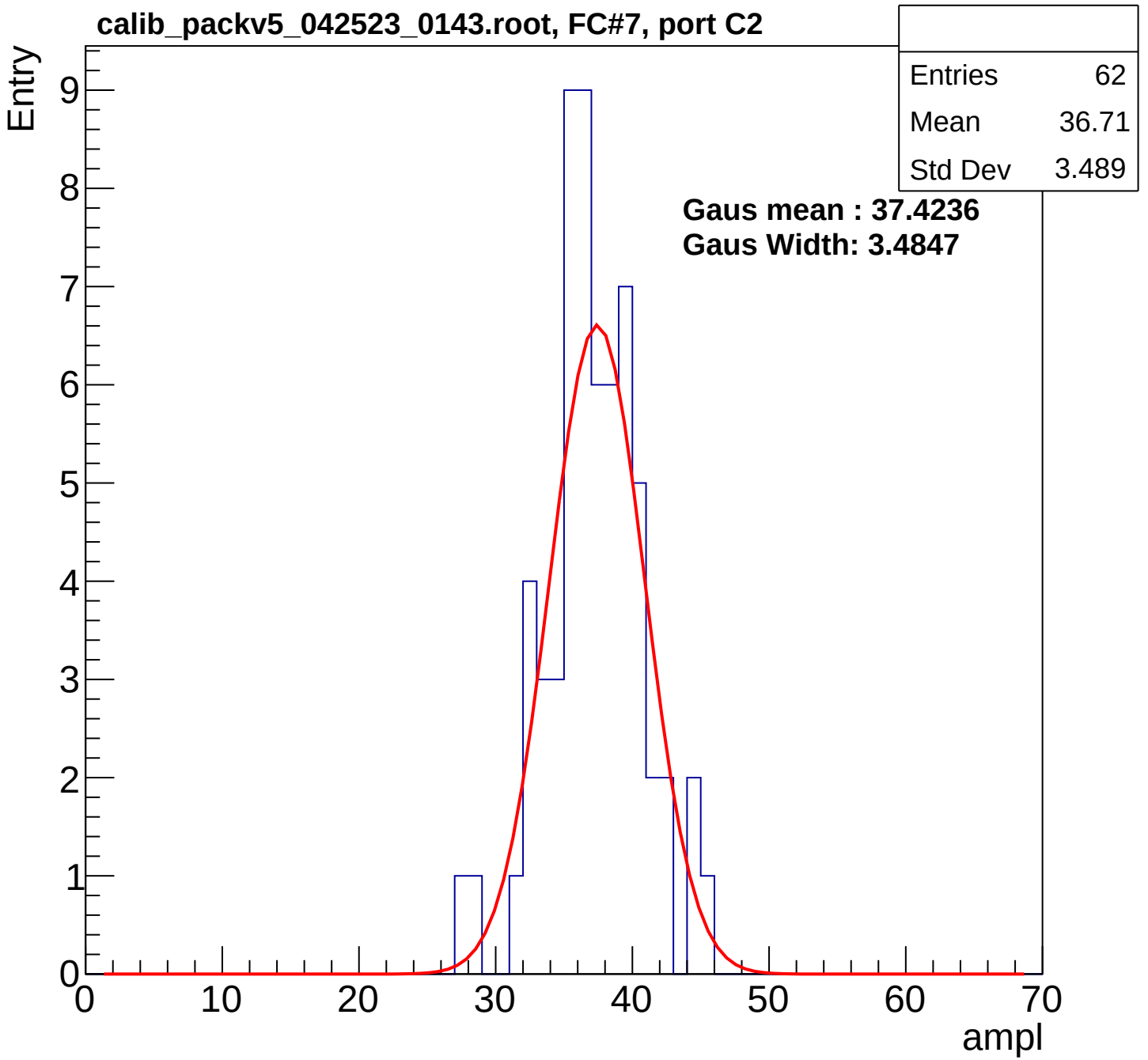

B1L103S, U8-ch77, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 54.83
Std Dev 3.354
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

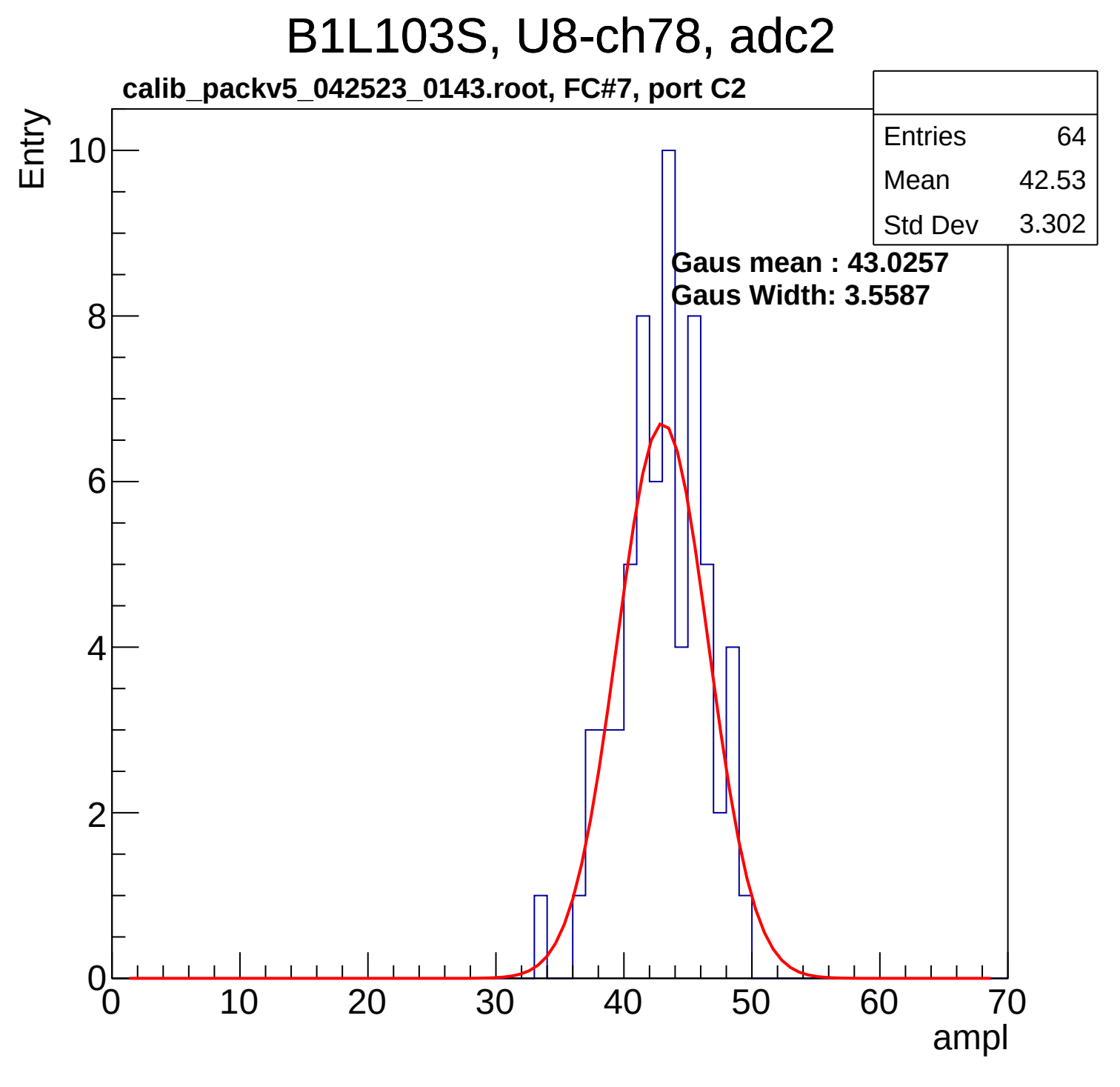

B1L103S, U8-ch77, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 58.69
Std Dev 8.87
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

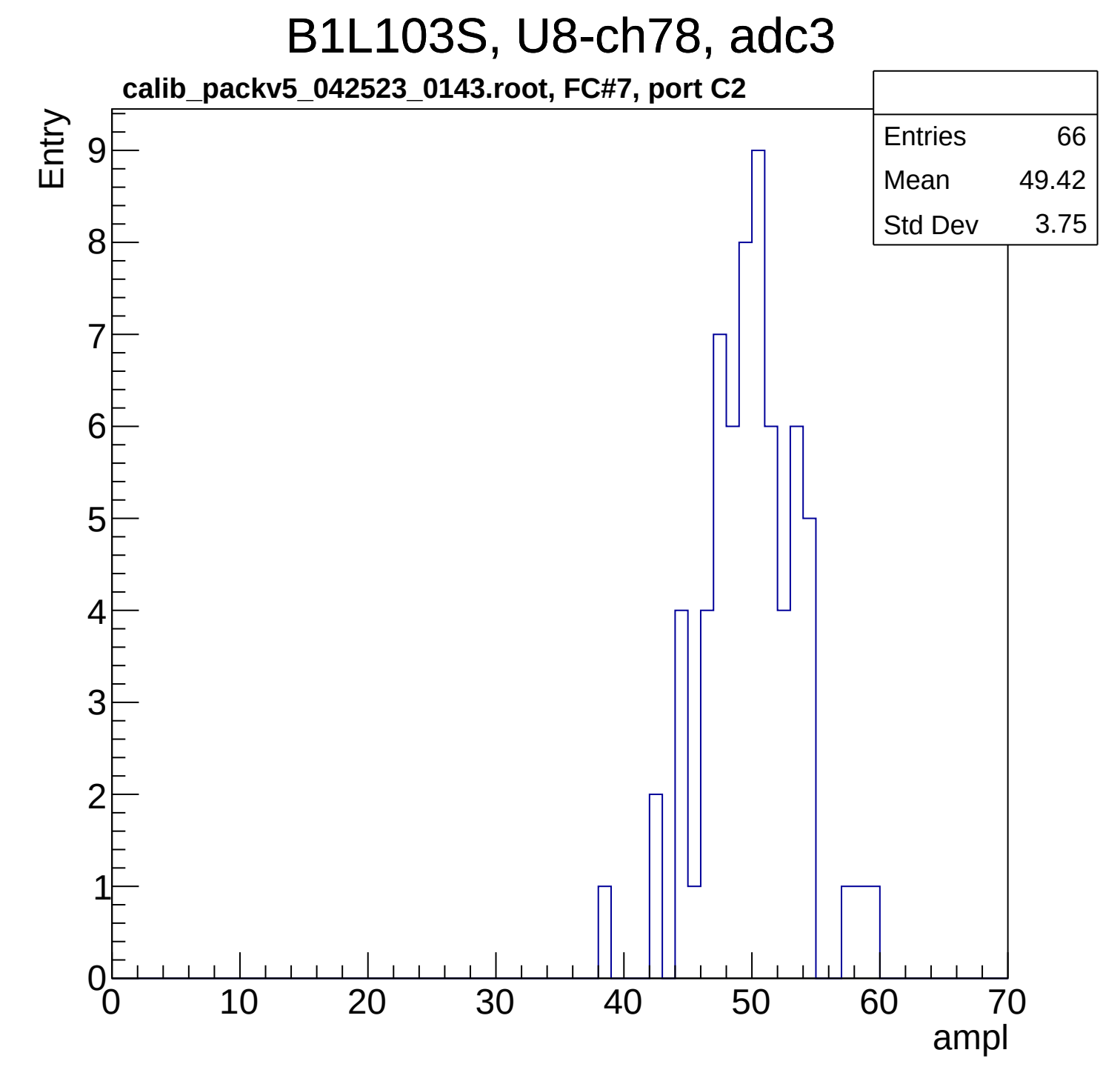

B1L103S, U8-ch77, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 9
Mean 61.78
Std Dev 1.03
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

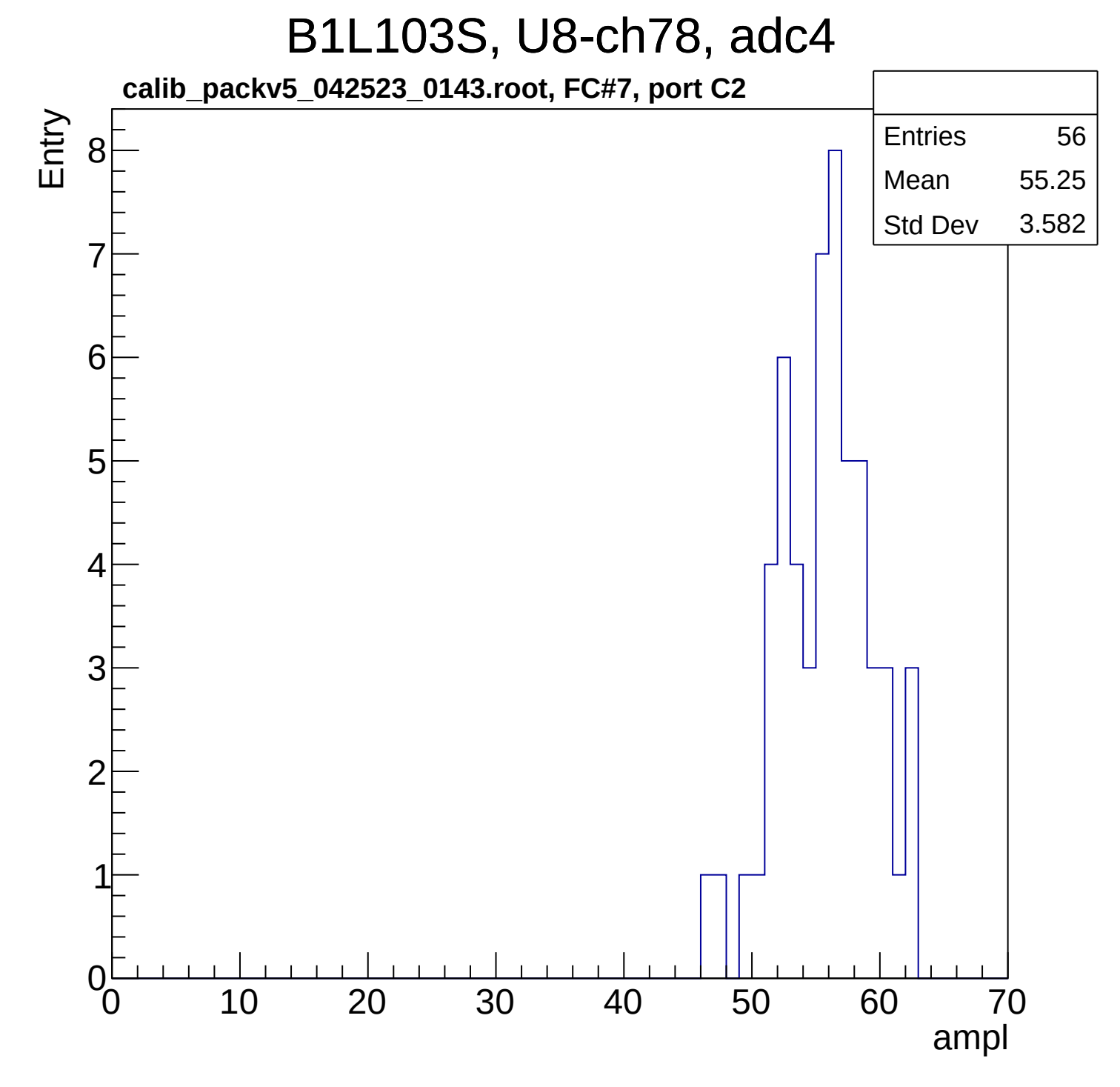

B1L103S, U8-ch77, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 6
Std Dev 8.485
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

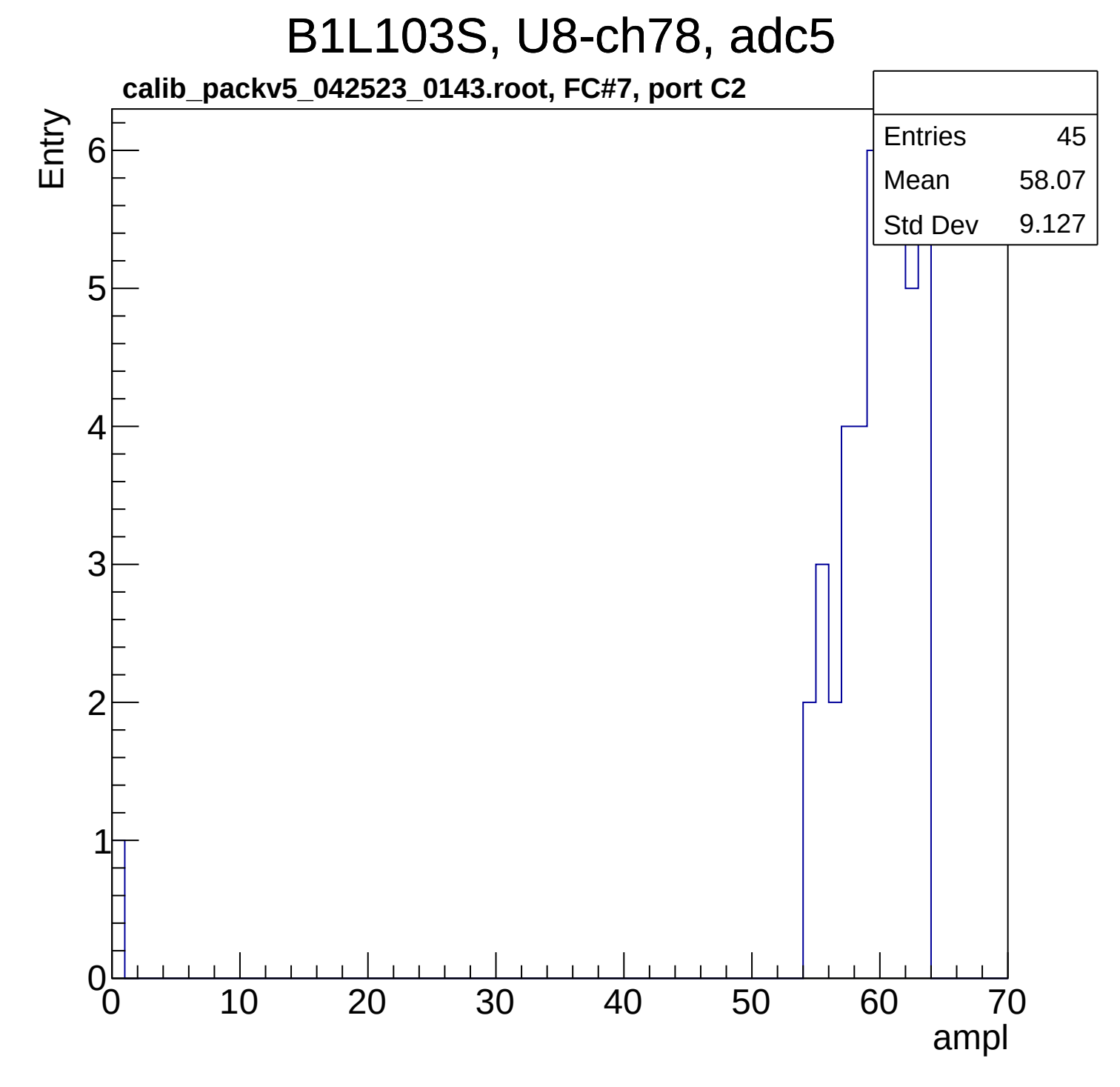

B1L103S, U8-ch78, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 28.07
Std Dev 7.687
Gaus mean : 30.4659
Gaus Width: 3.1638
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

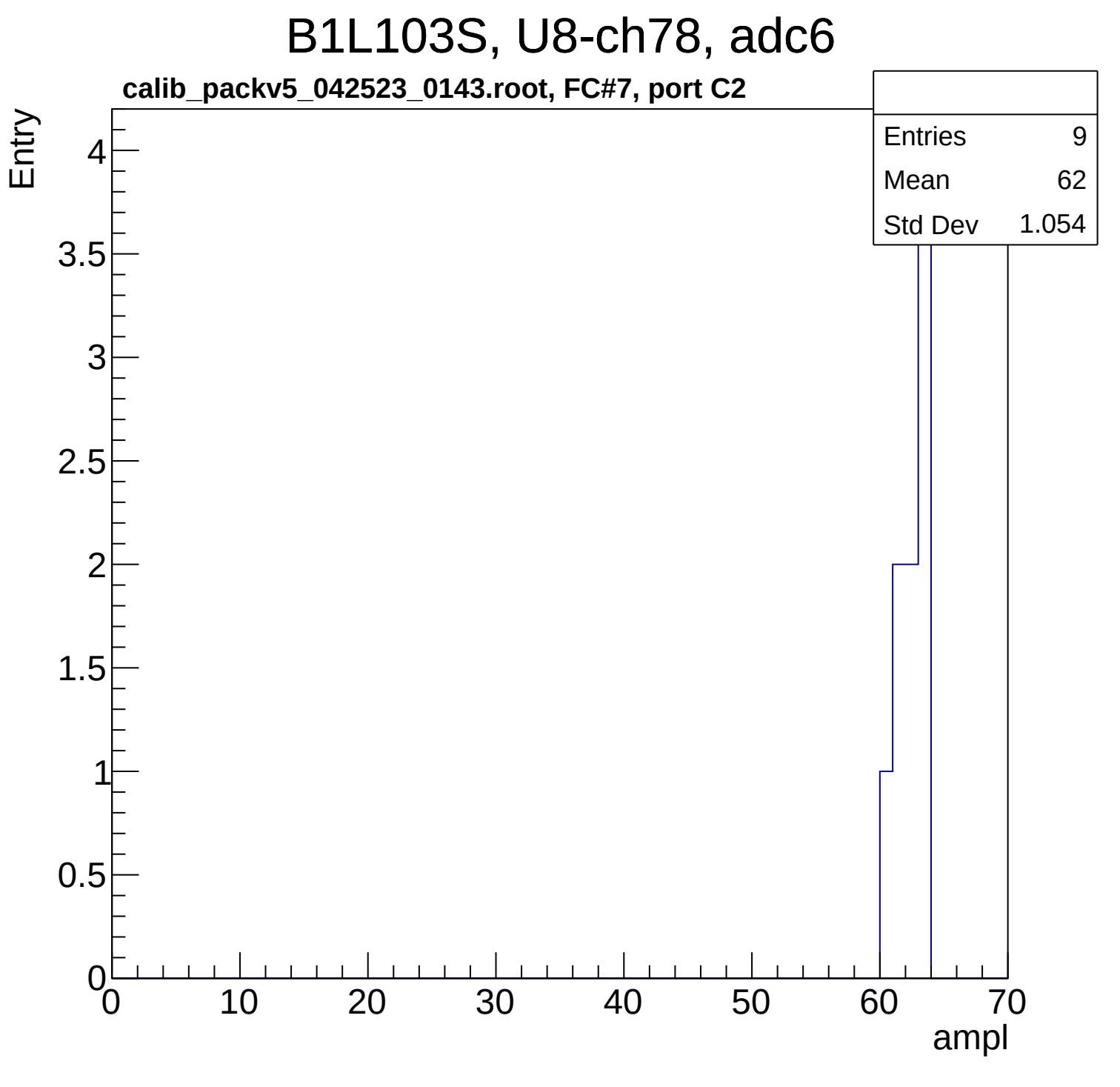

B1L103S, U8-ch78, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 36.71
Std Dev 3.489
Gaus mean : 37.4236
Gaus Width: 3.4847
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

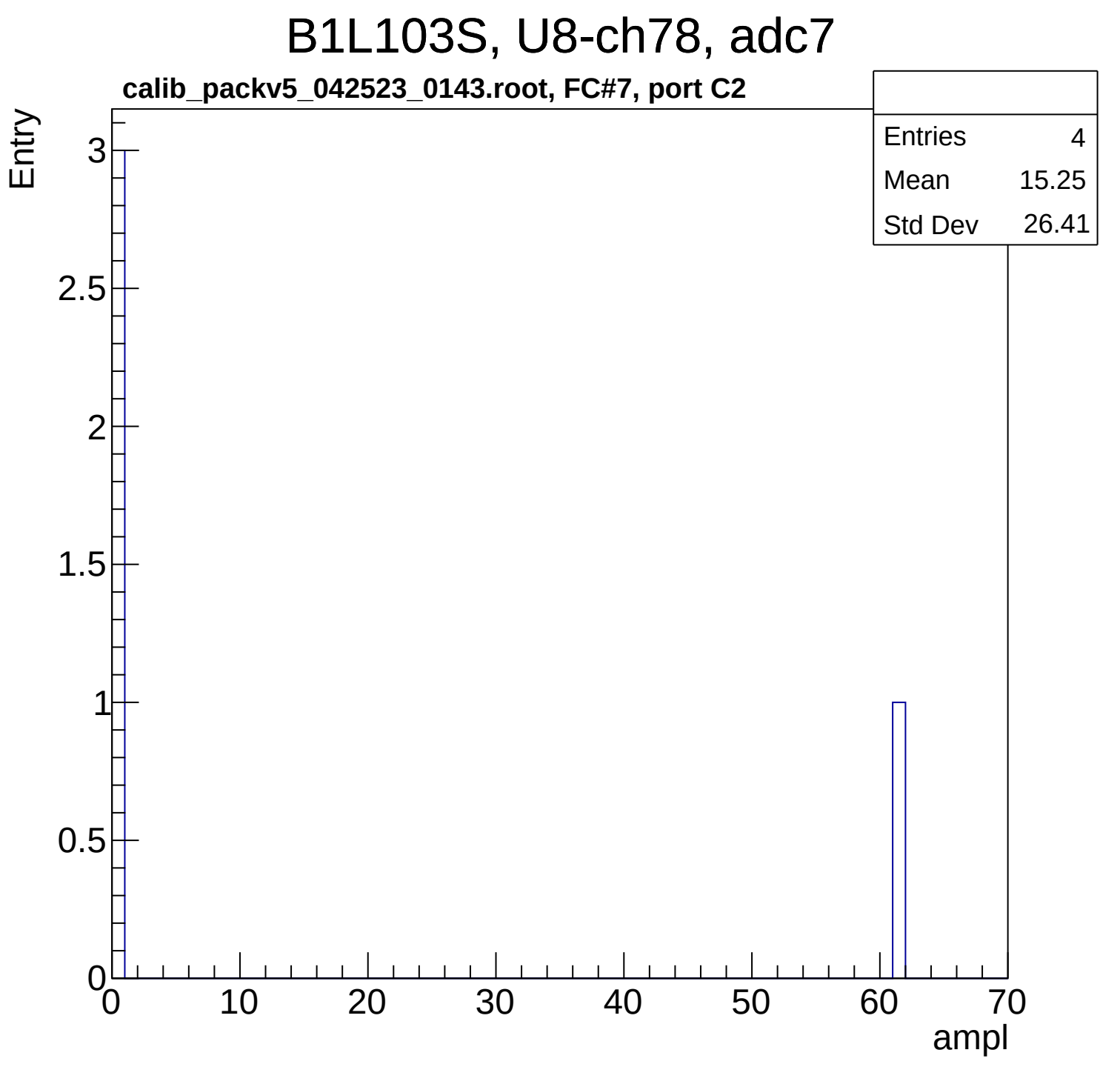

B1L103S, U8-ch78, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 42.53
Std Dev 3.302
Gaus mean : 43.0257
Gaus Width: 3.5587
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

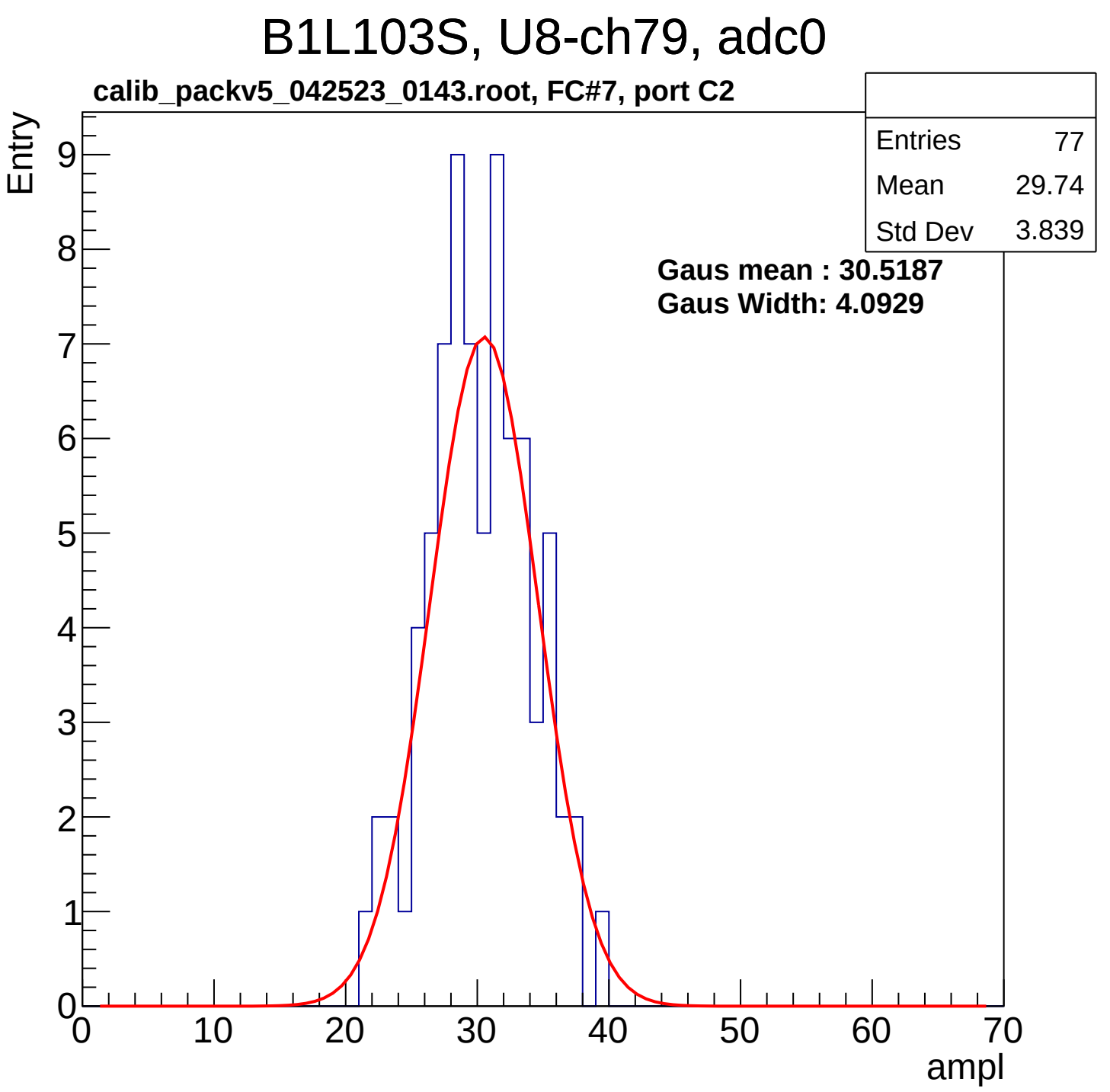

B1L103S, U8-ch78, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 49.42
Std Dev 3.75
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

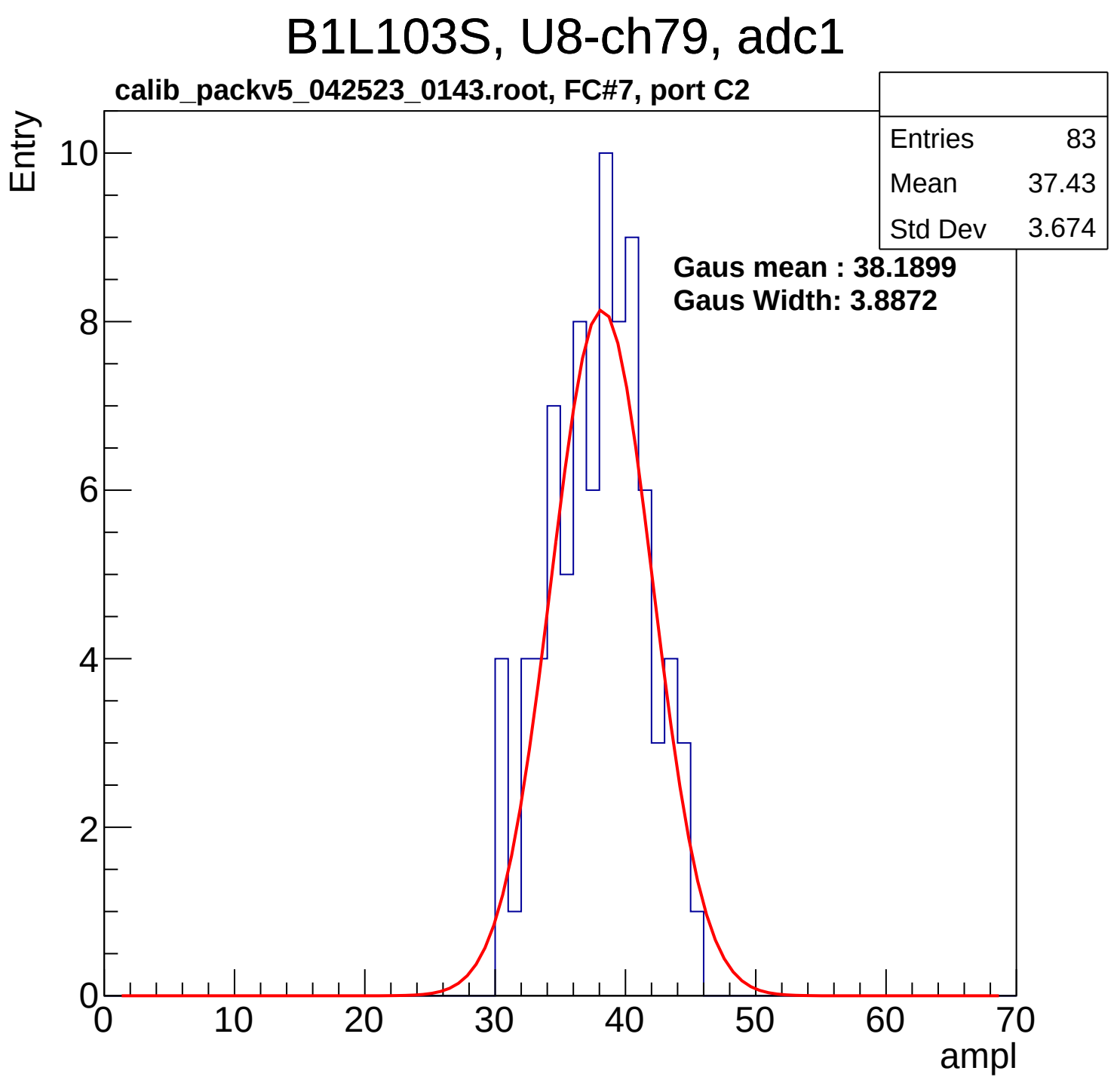

B1L103S, U8-ch78, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 55.25
Std Dev 3.582
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

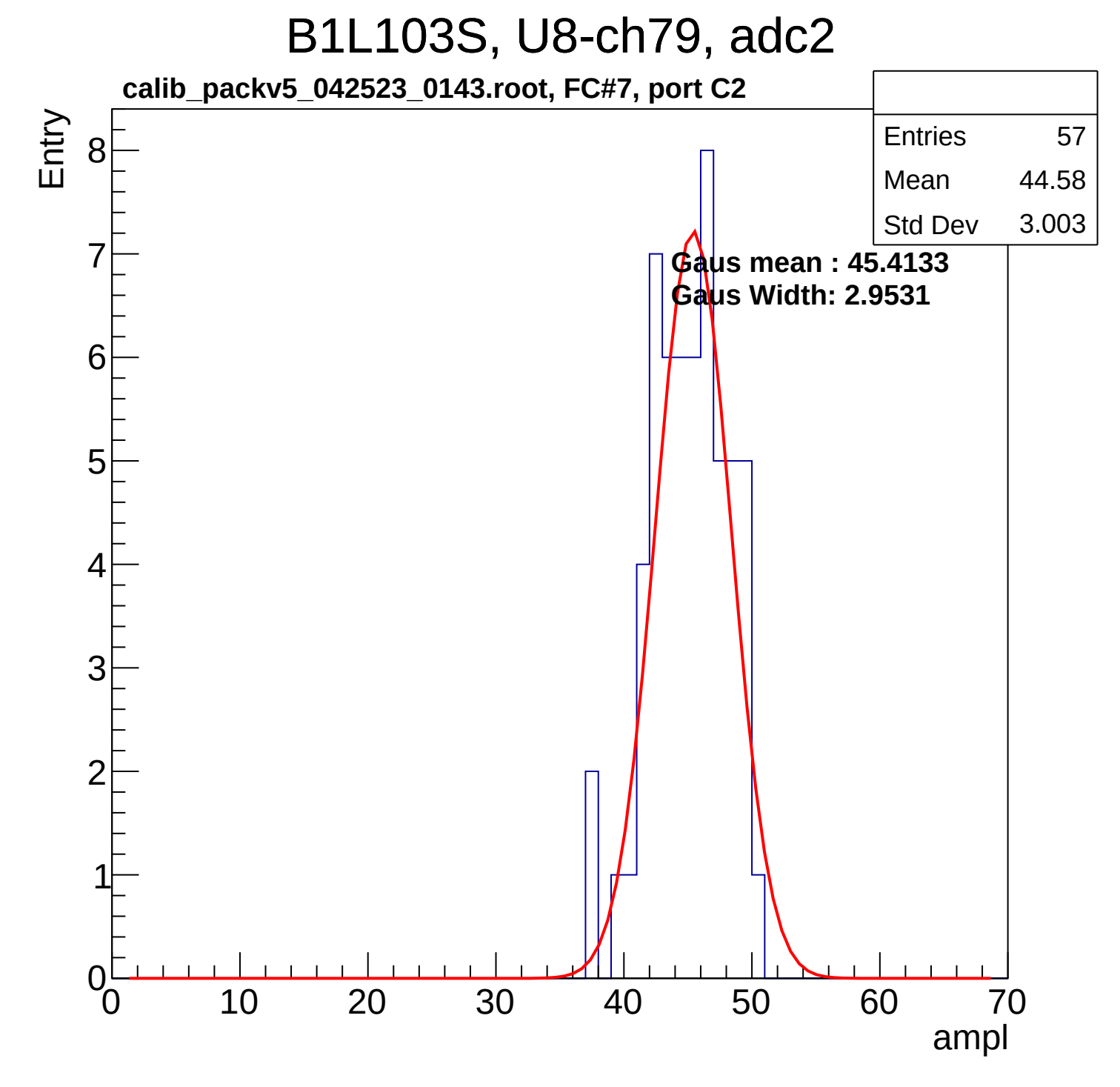

B1L103S, U8-ch78, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 45
Mean 58.07
Std Dev 9.127
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

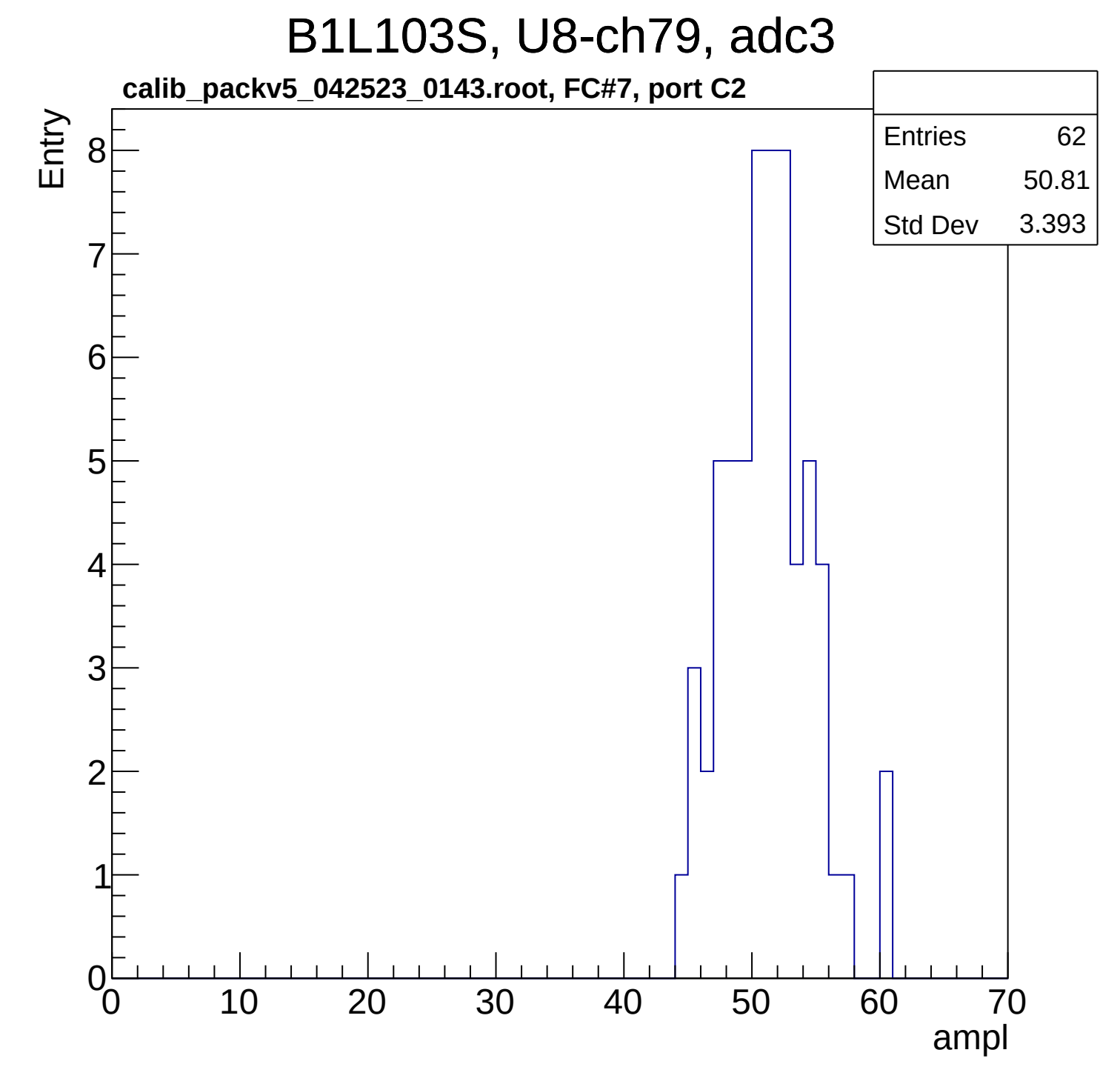

B1L103S, U8-ch78, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 9
Mean 62
Std Dev 1.054
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

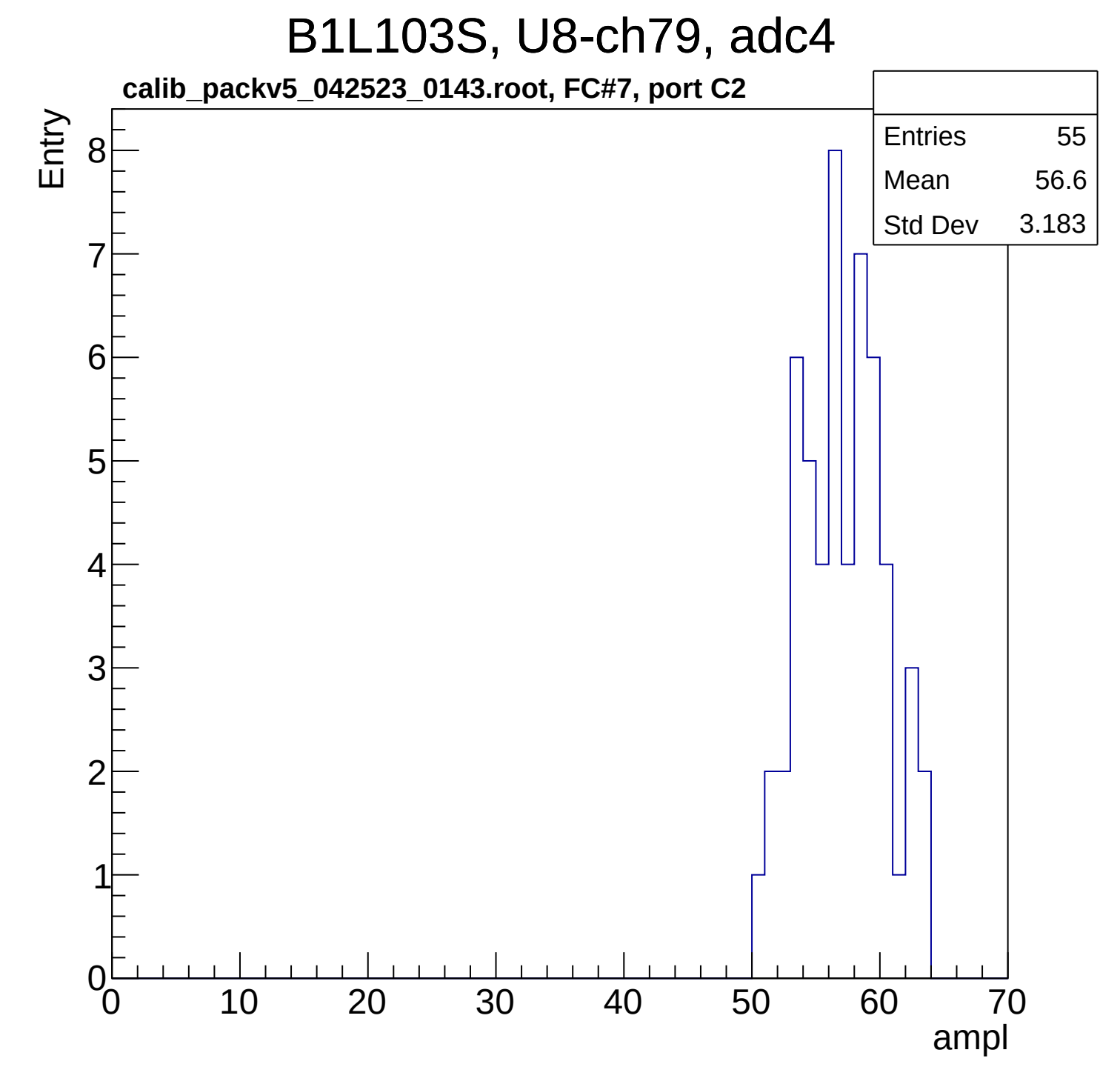

B1L103S, U8-ch78, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 15.25
Std Dev 26.41
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

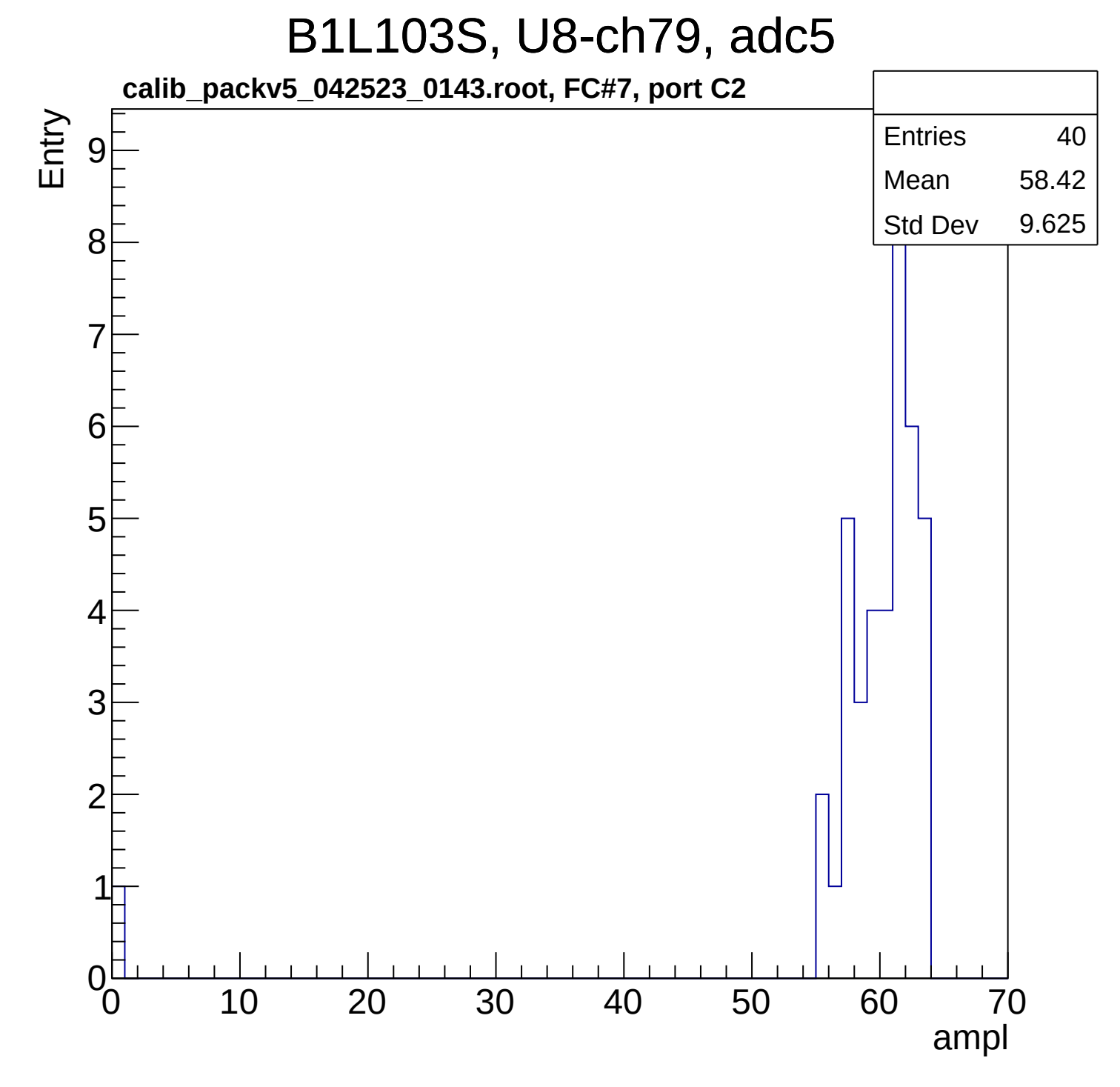

B1L103S, U8-ch79, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 29.74
Std Dev 3.839
Gaus mean : 30.5187
Gaus Width: 4.0929
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

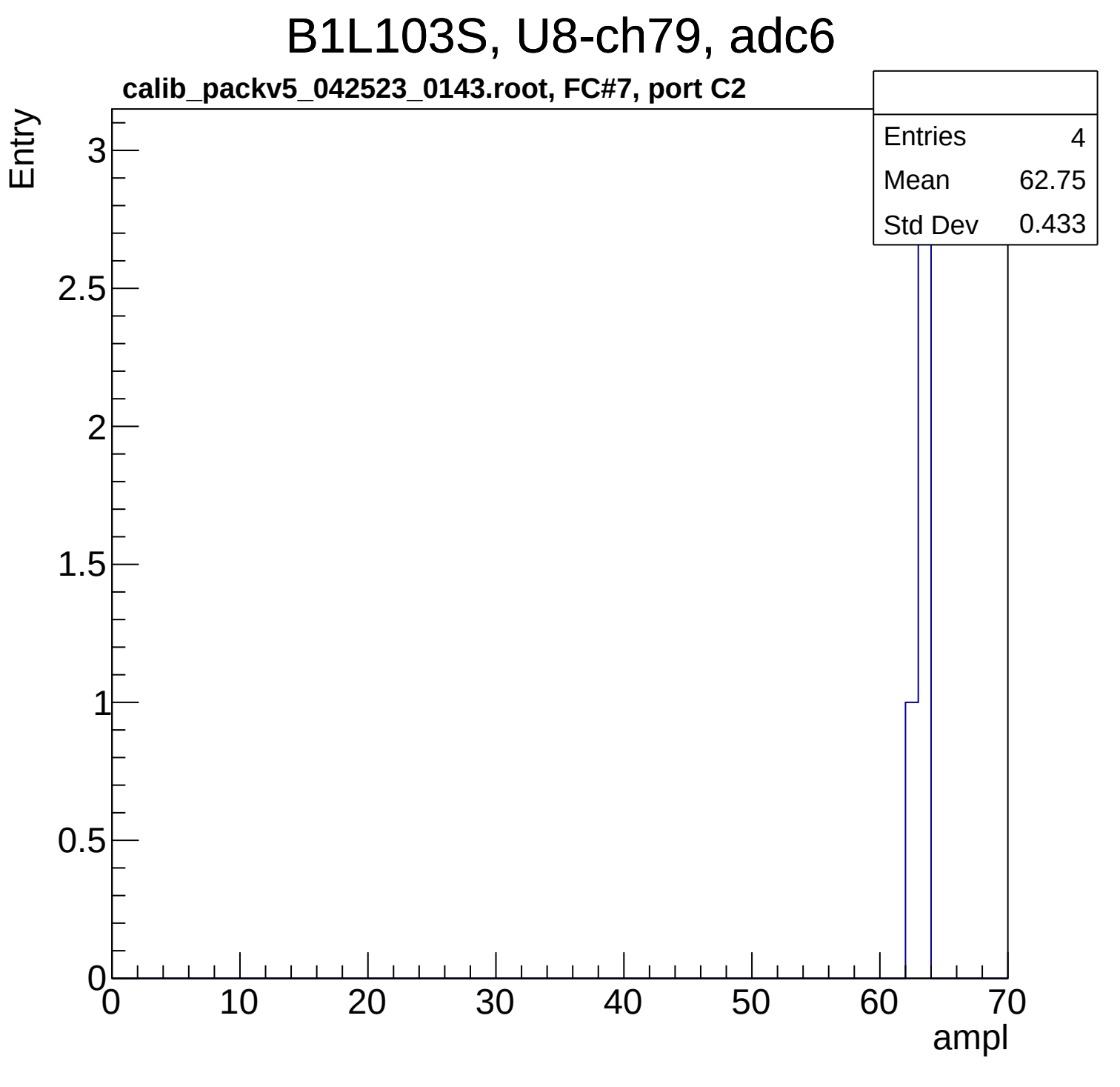

B1L103S, U8-ch79, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 83
Mean 37.43
Std Dev 3.674
Gaus mean : 38.1899
Gaus Width: 3.8872
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

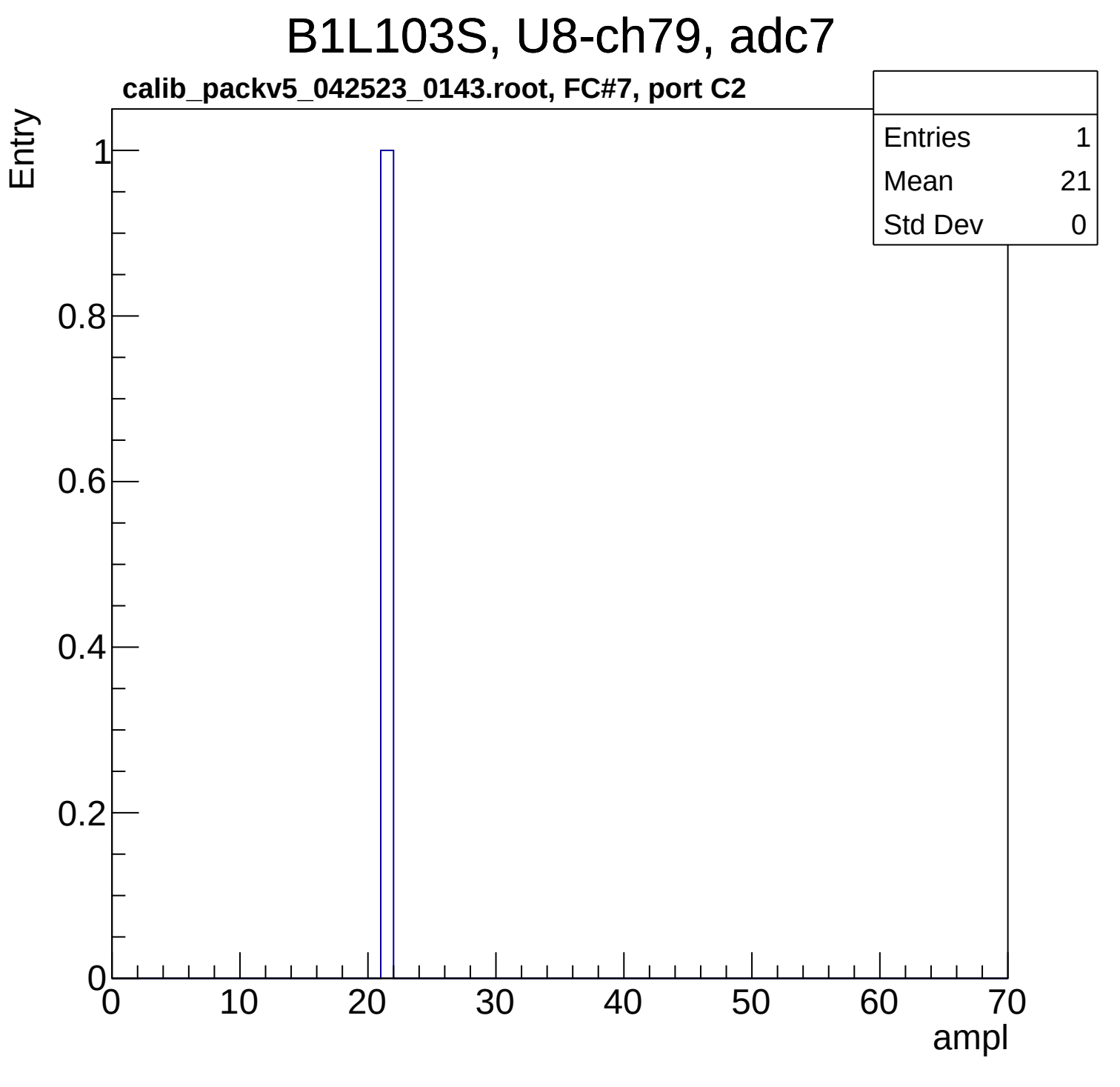

B1L103S, U8-ch79, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 44.58
Std Dev 3.003
Gaus mean : 45.4133
Gaus Width: 2.9531
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

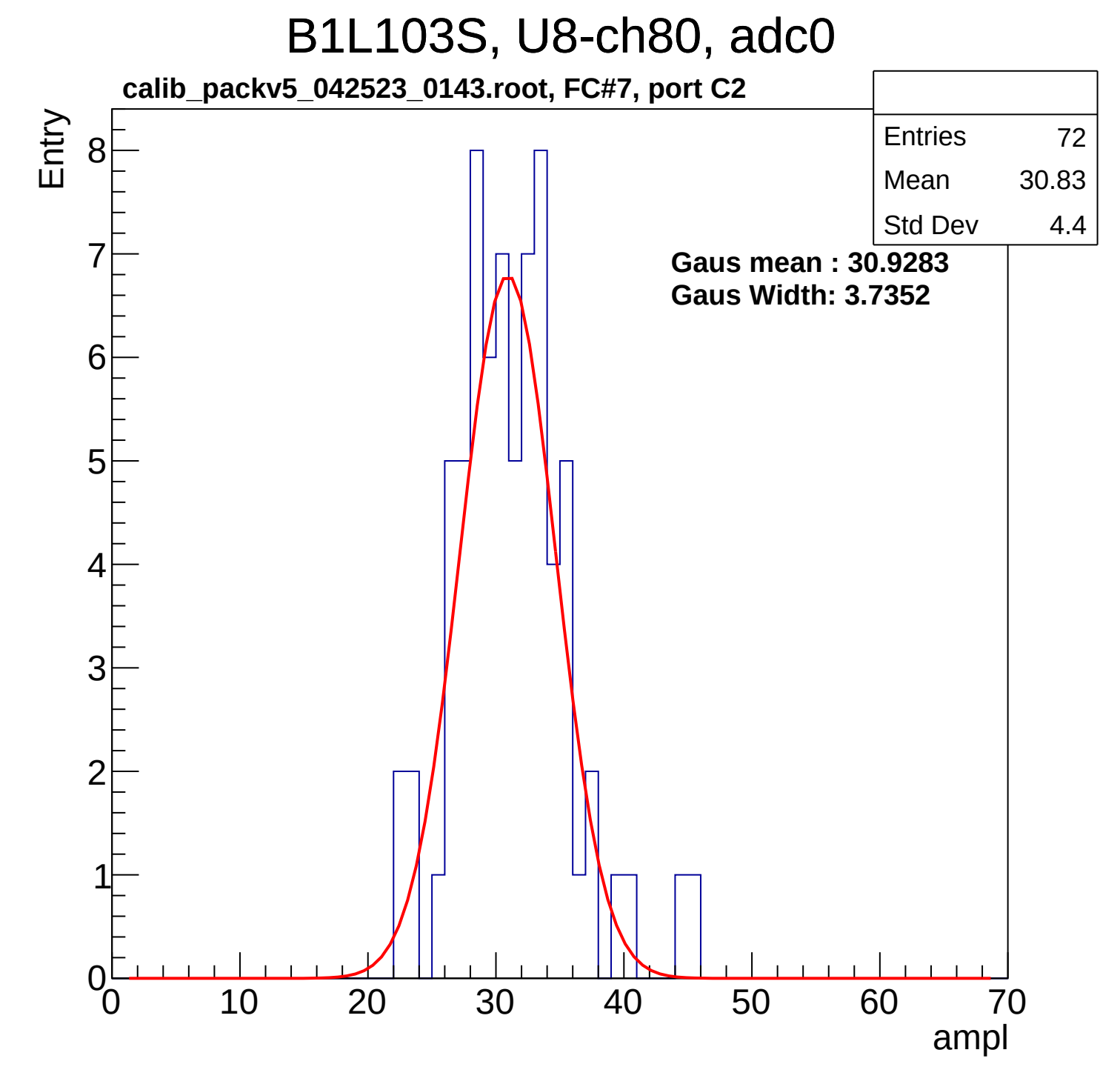

B1L103S, U8-ch79, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 50.81
Std Dev 3.393
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

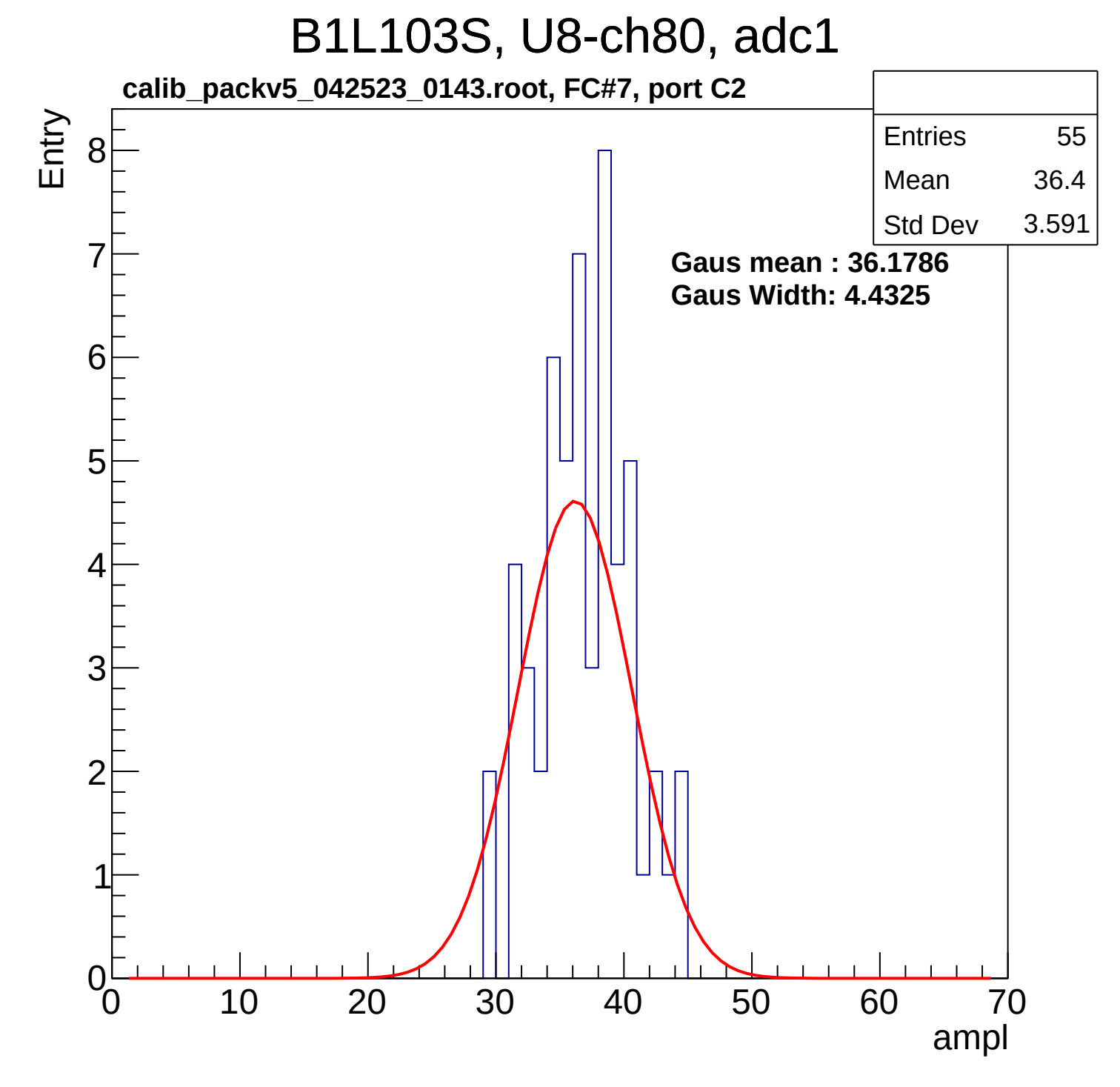

B1L103S, U8-ch79, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 56.6
Std Dev 3.183
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

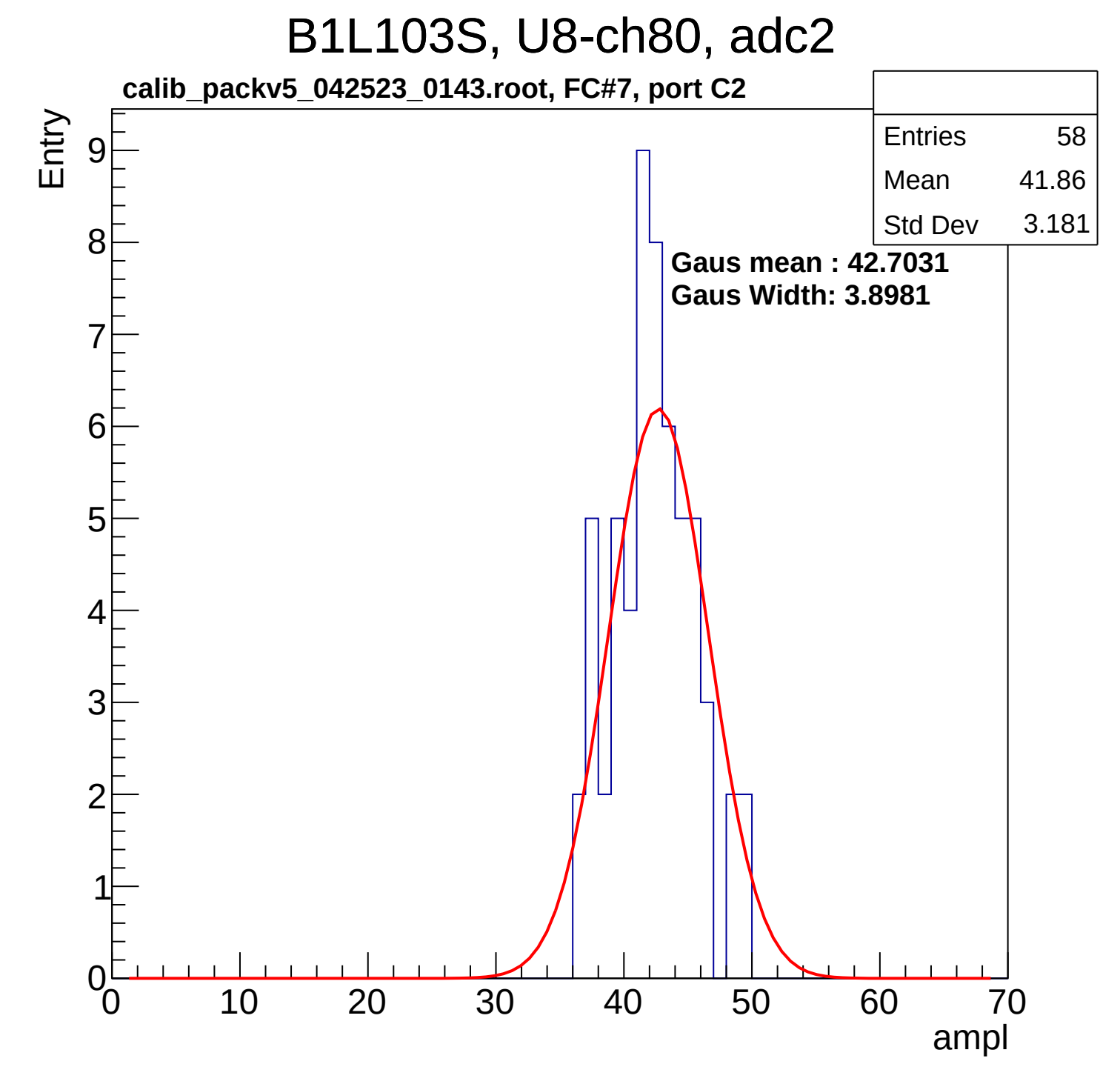

B1L103S, U8-ch79, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 40
Mean 58.42
Std Dev 9.625
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

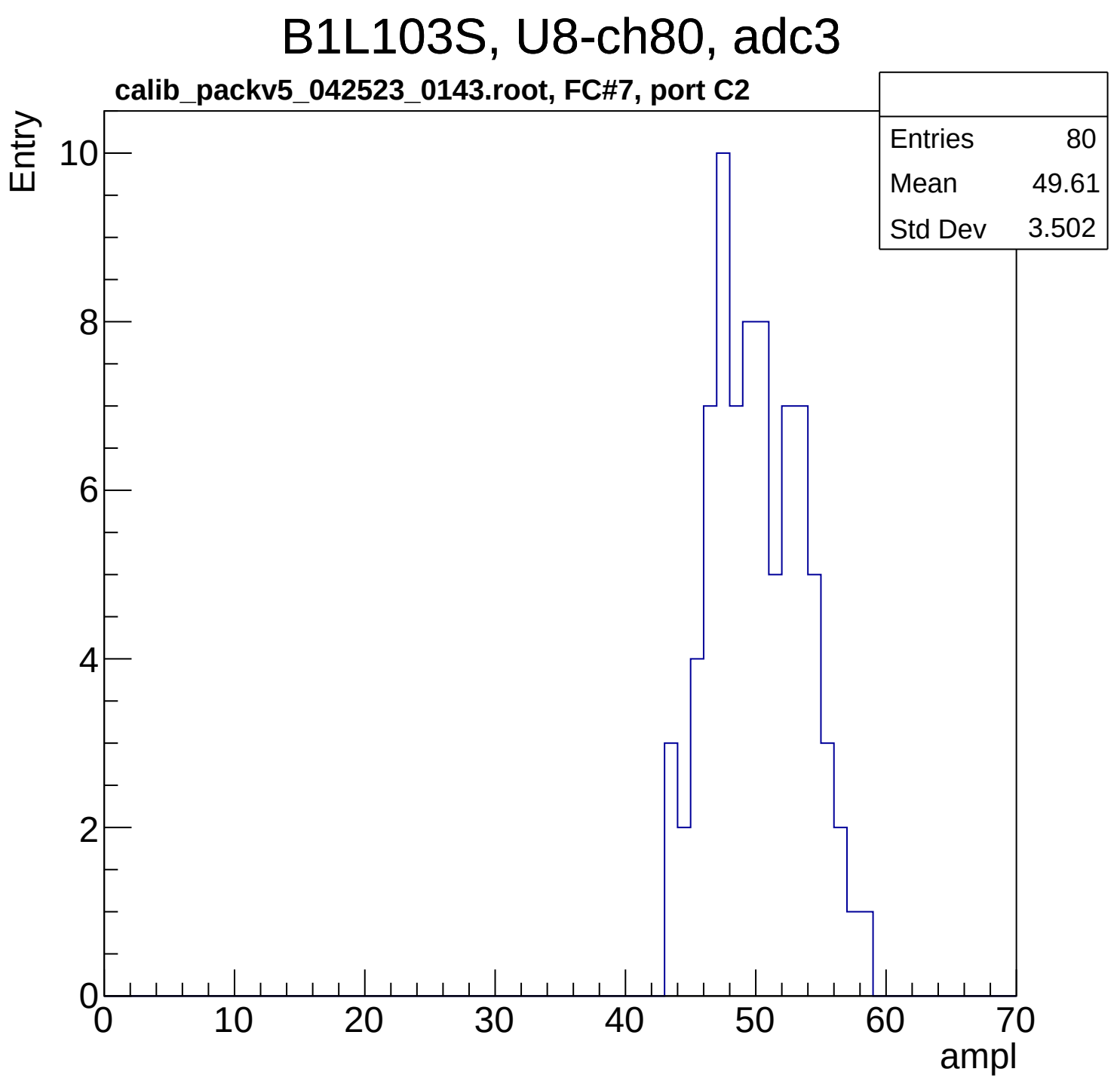

B1L103S, U8-ch79, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 62.75
Std Dev 0.433
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

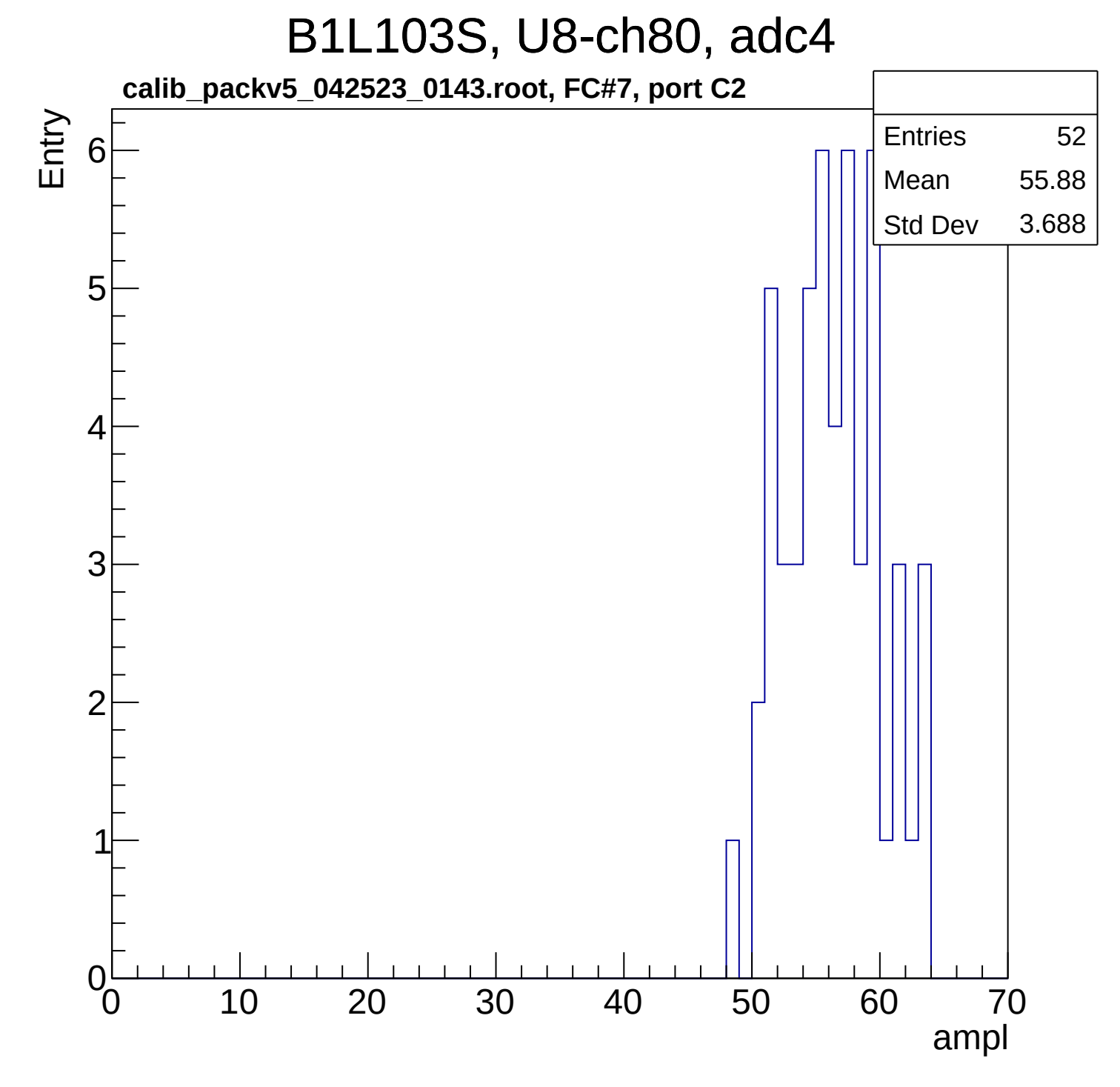

B1L103S, U8-ch79, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 21
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

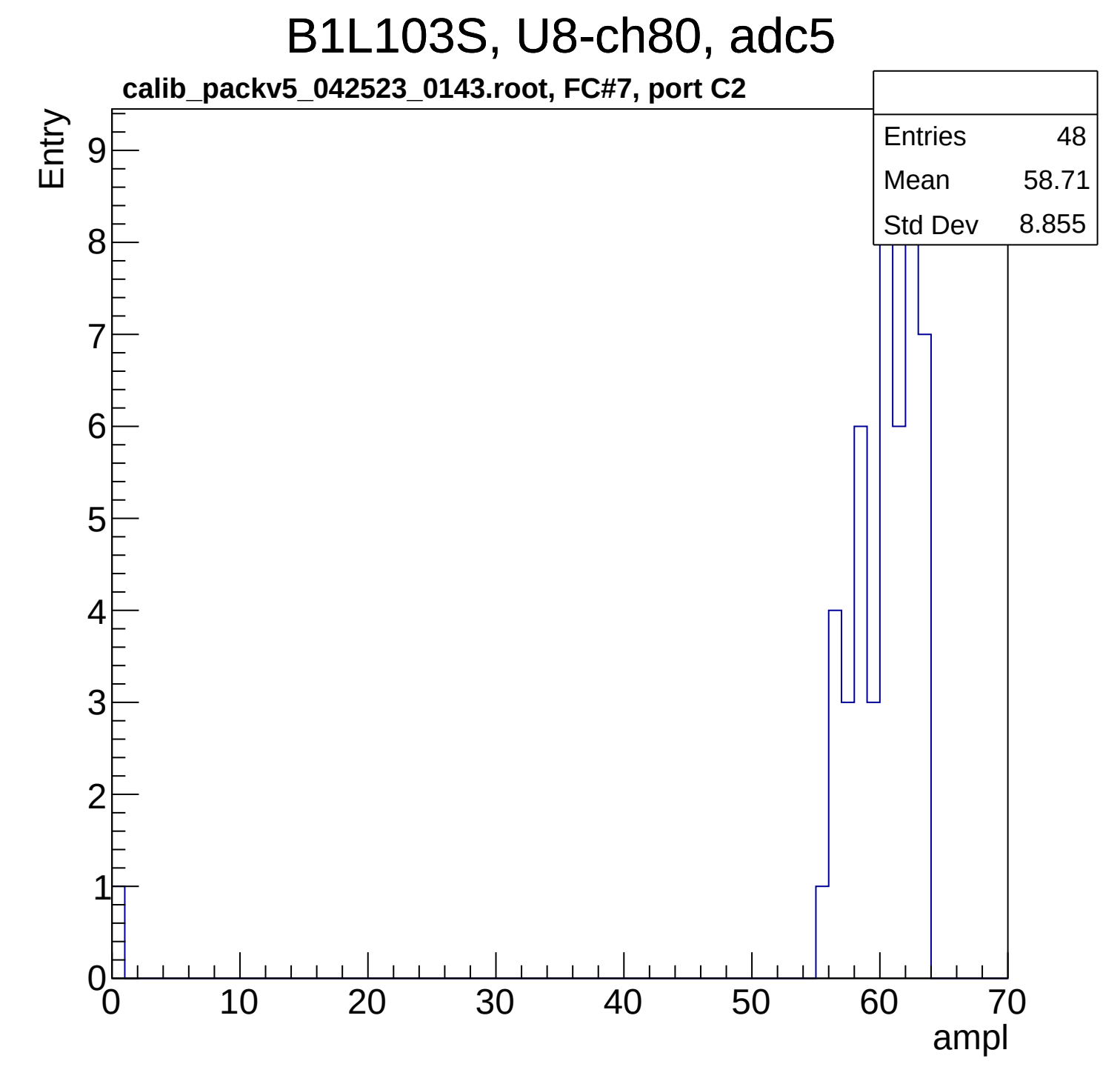

B1L103S, U8-ch80, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 30.83
Std Dev 4.4
Gaus mean : 30.9283
Gaus Width: 3.7352
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

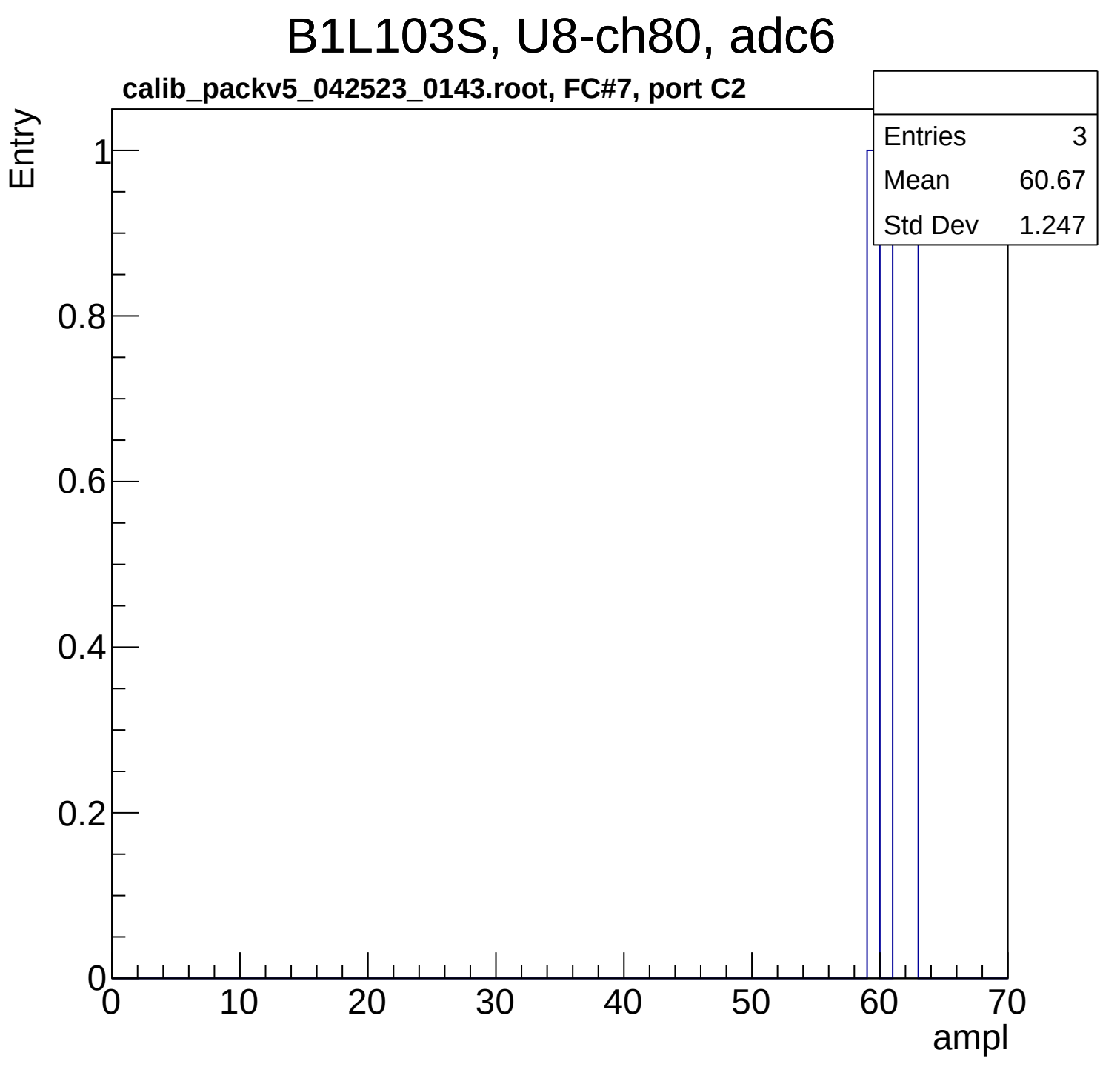

B1L103S, U8-ch80, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 36.4
Std Dev 3.591
Gaus mean : 36.1786
Gaus Width: 4.4325
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

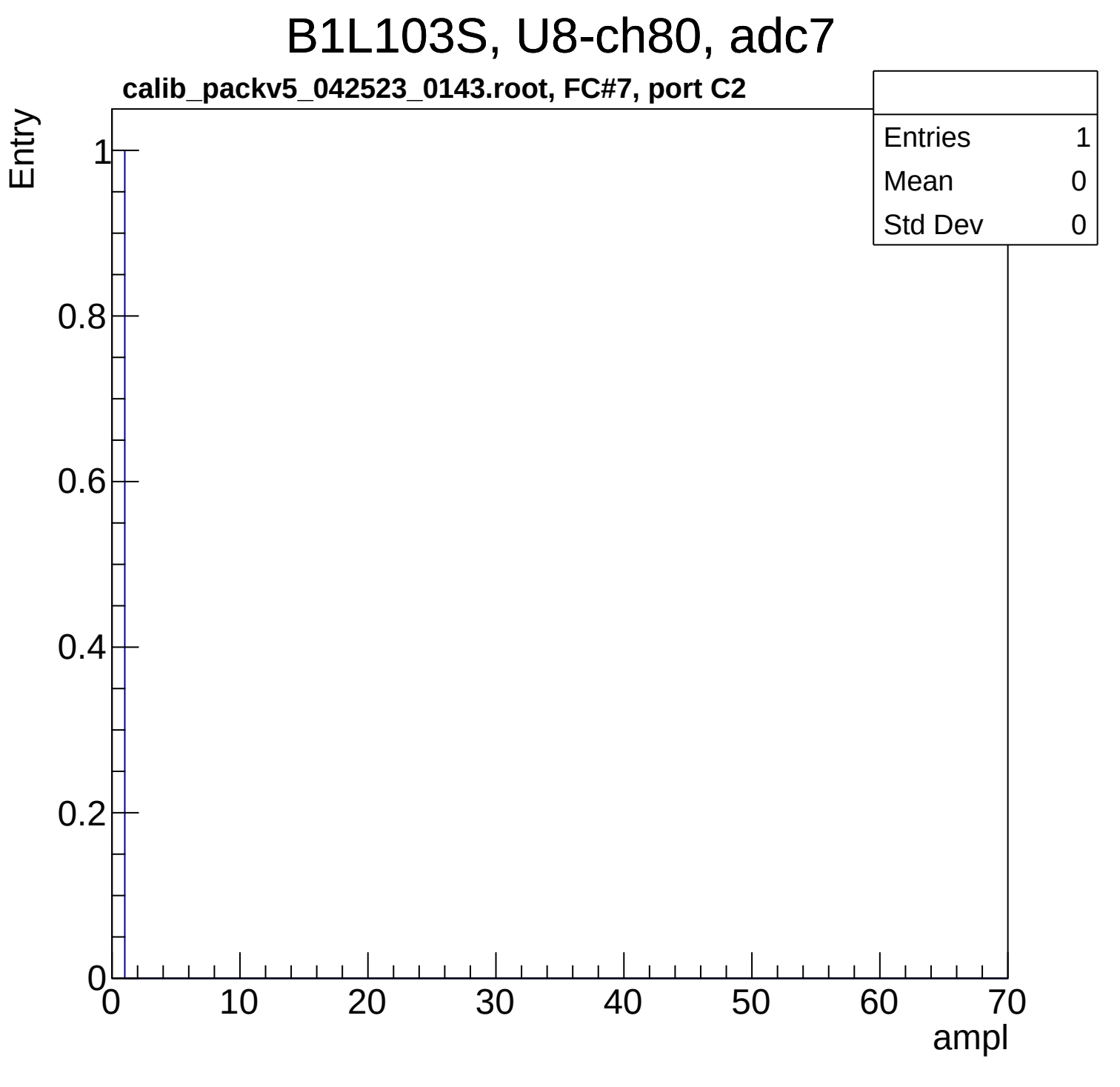

B1L103S, U8-ch80, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 41.86
Std Dev 3.181
Gaus mean : 42.7031
Gaus Width: 3.8981
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

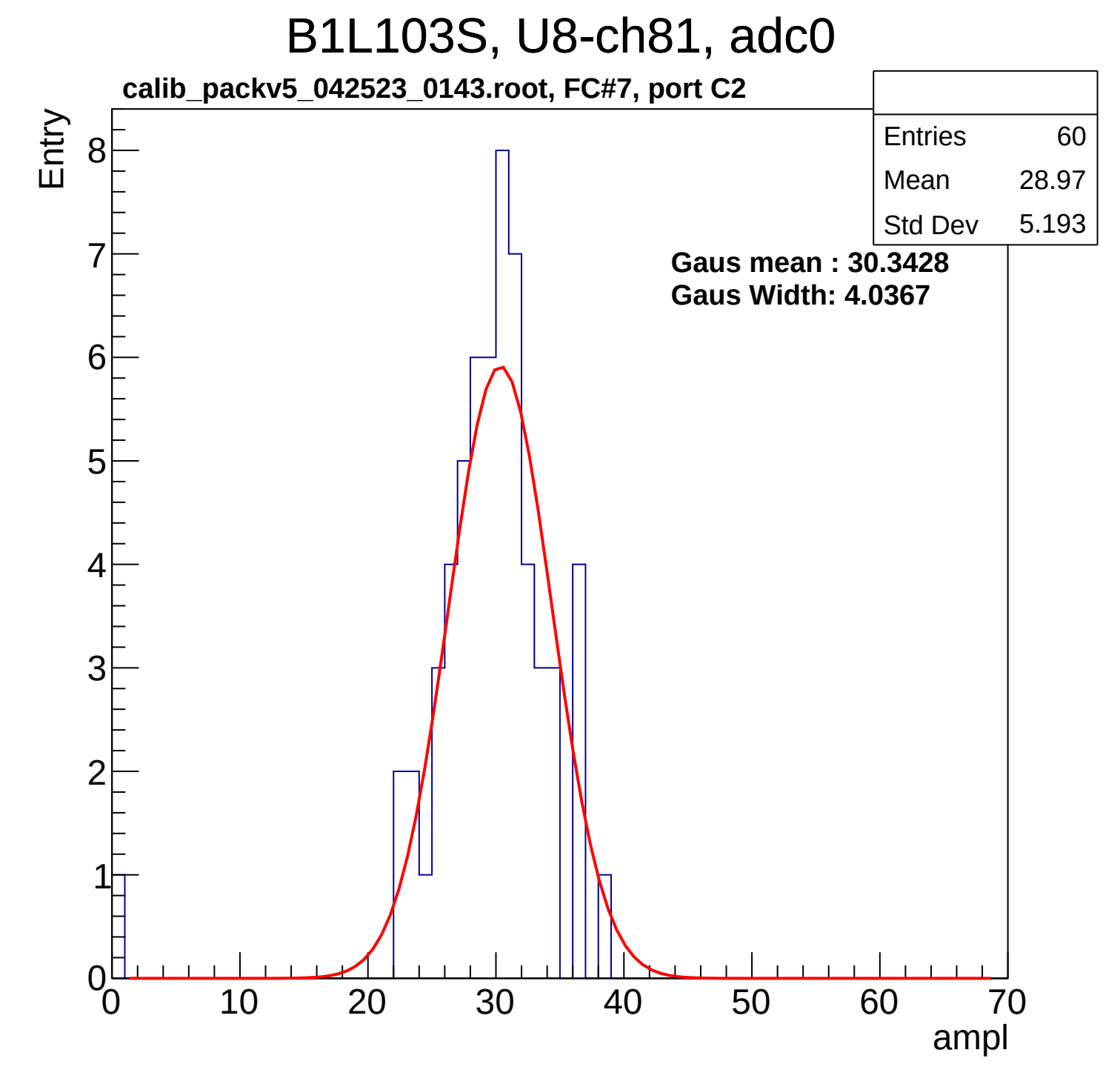

B1L103S, U8-ch80, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 80
Mean 49.61
Std Dev 3.502
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

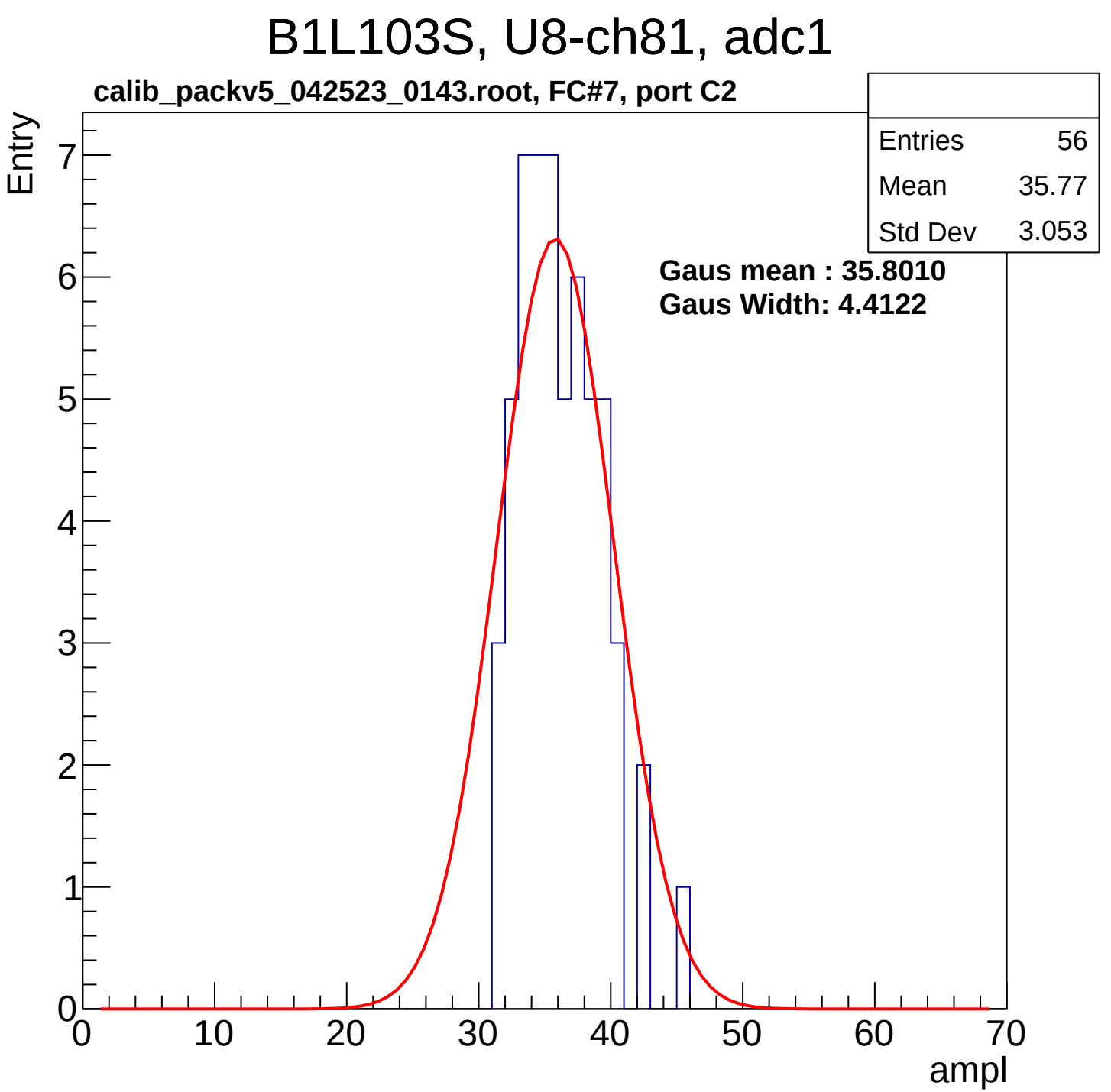

B1L103S, U8-ch80, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 55.88
Std Dev 3.688
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

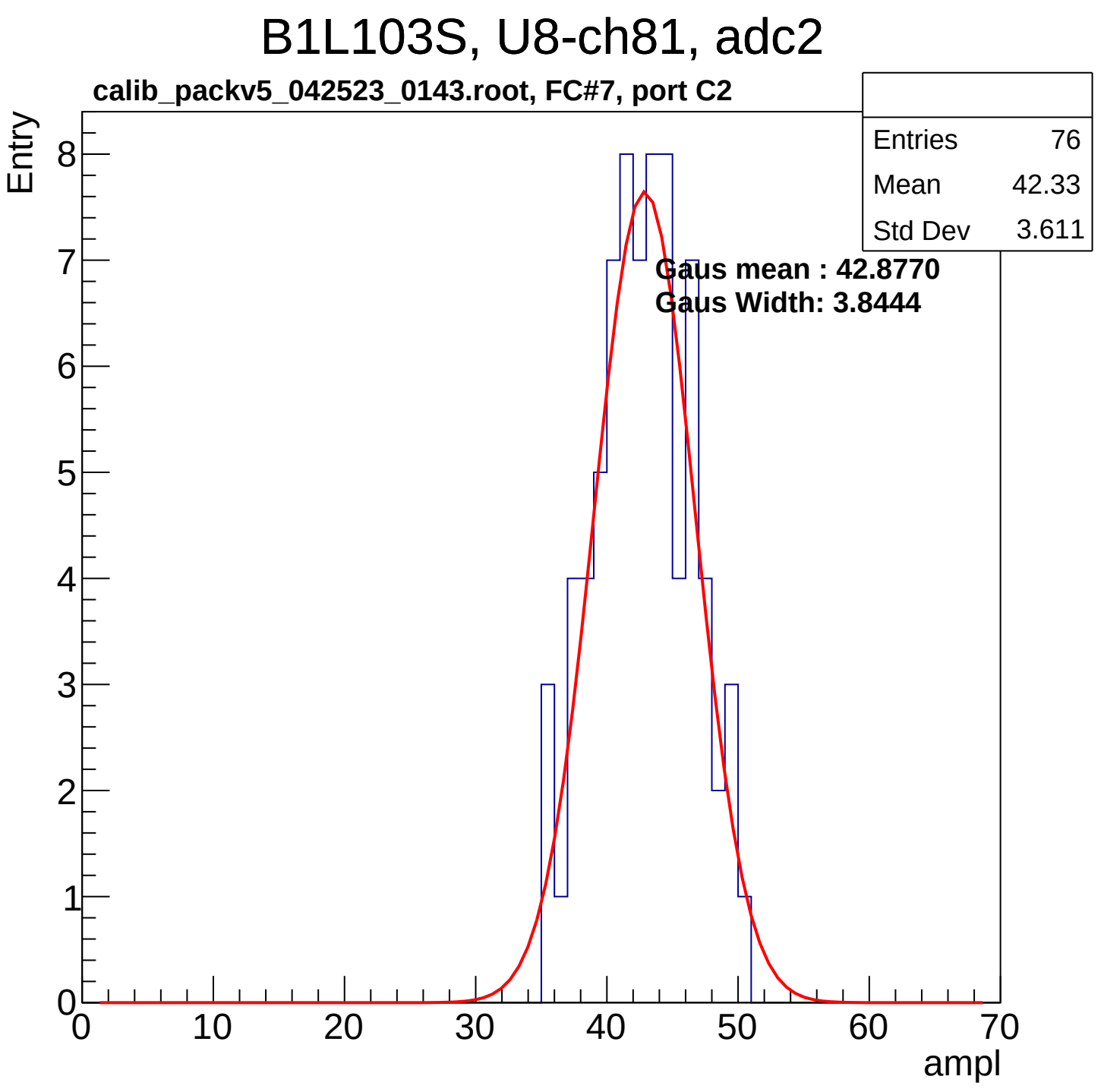

B1L103S, U8-ch80, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 58.71
Std Dev 8.855
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

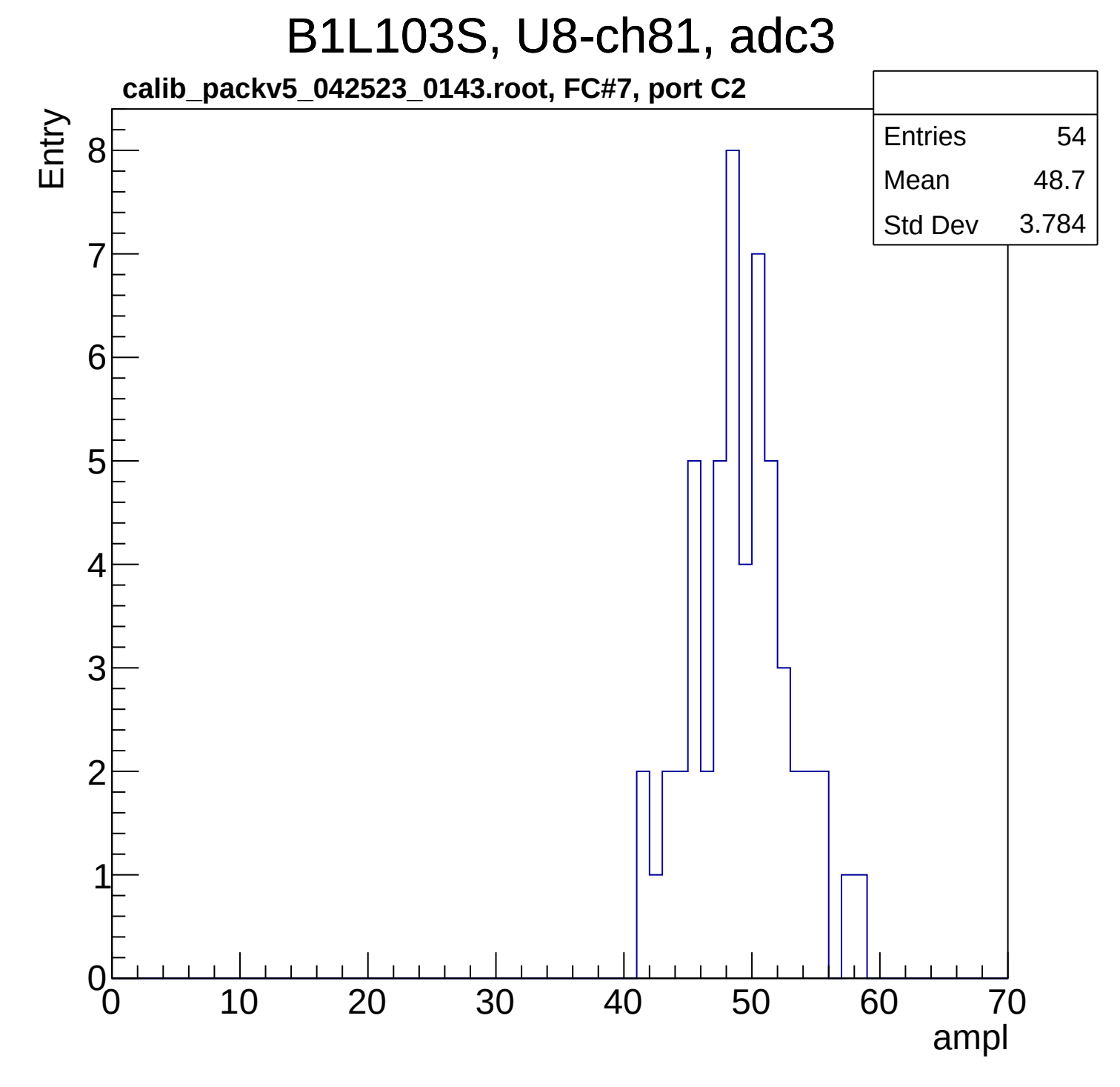

B1L103S, U8-ch80, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 60.67
Std Dev 1.247
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

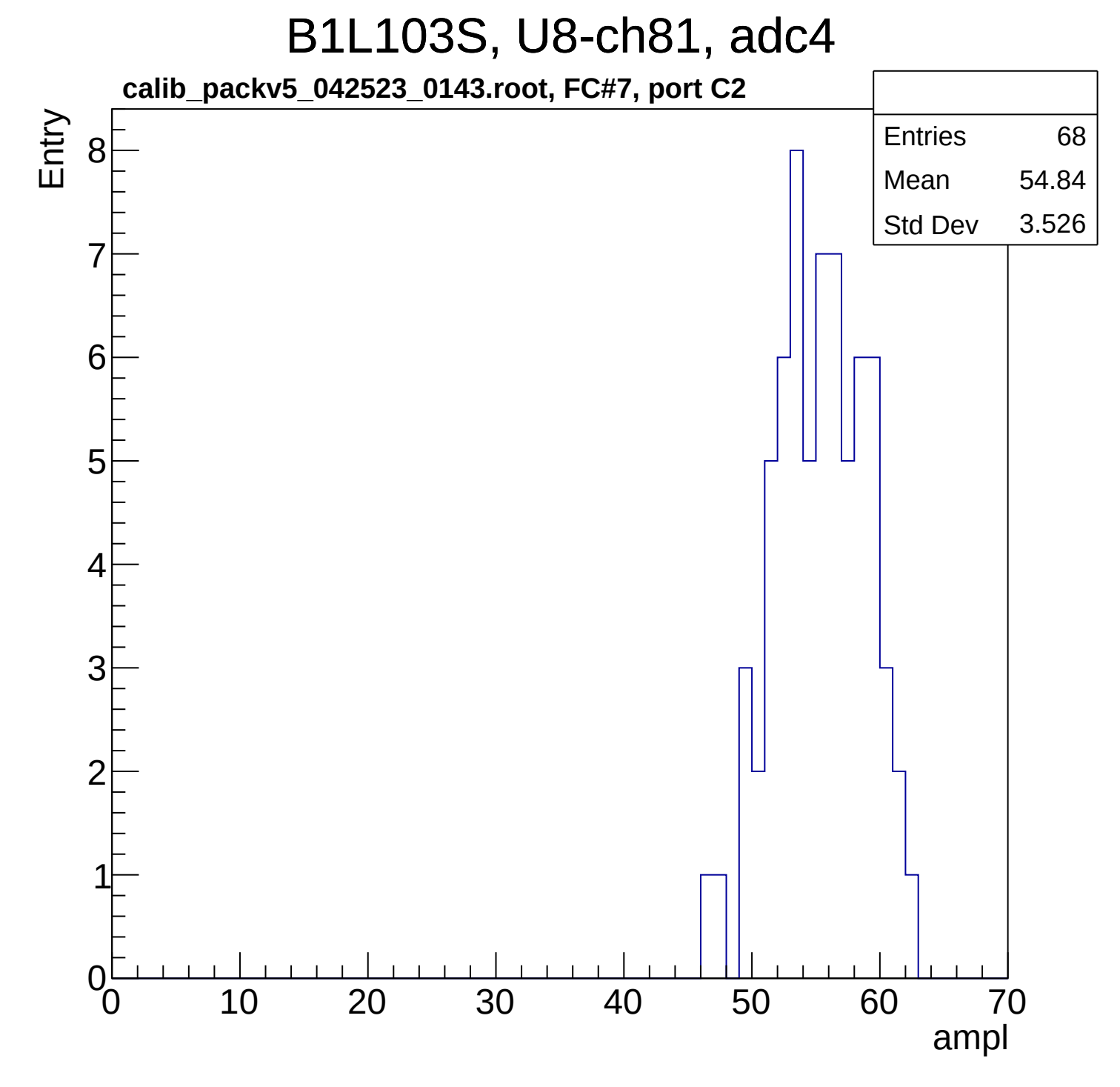

B1L103S, U8-ch80, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

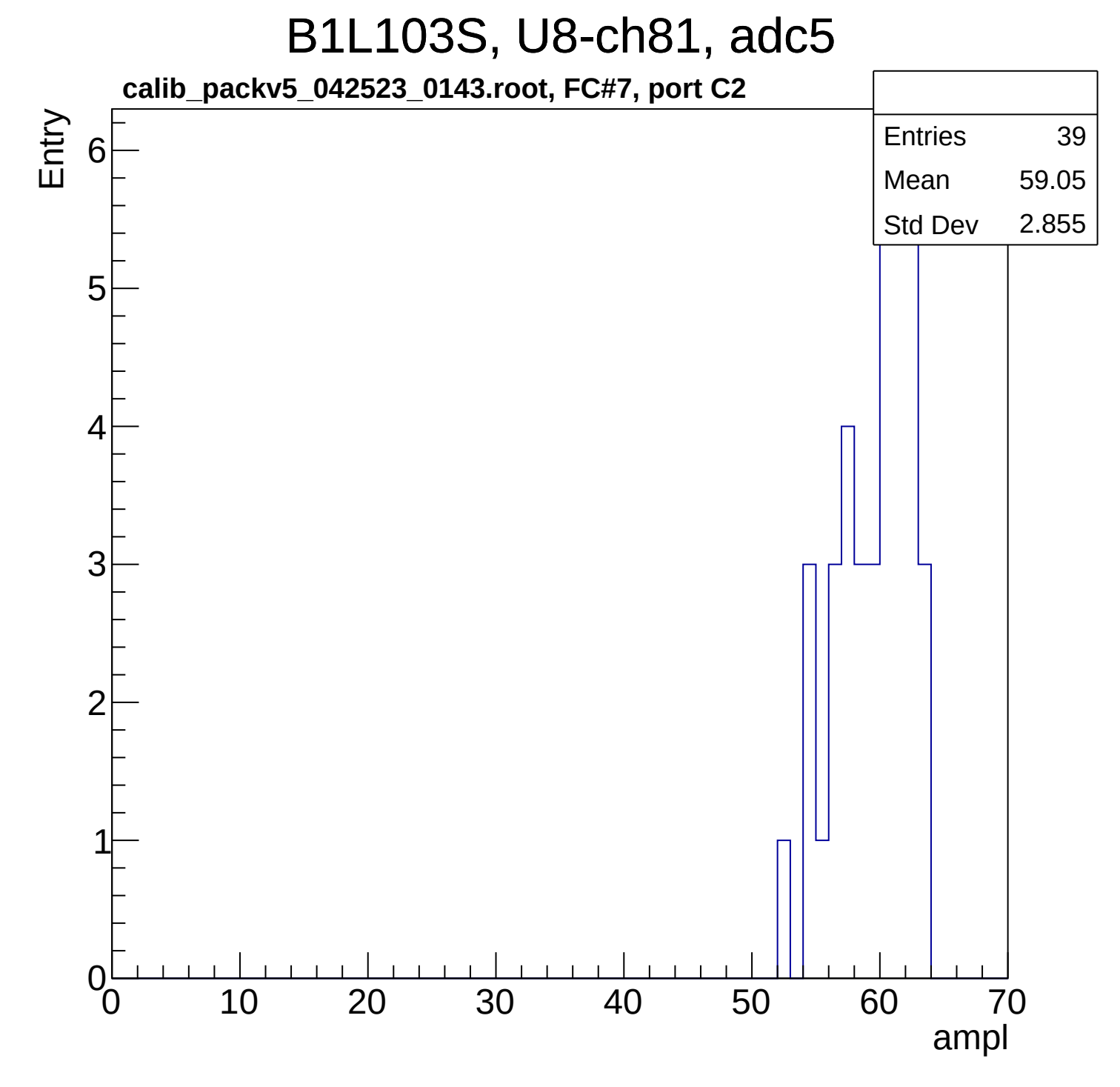

B1L103S, U8-ch81, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 28.97
Std Dev 5.193
Gaus mean : 30.3428
Gaus Width: 4.0367
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

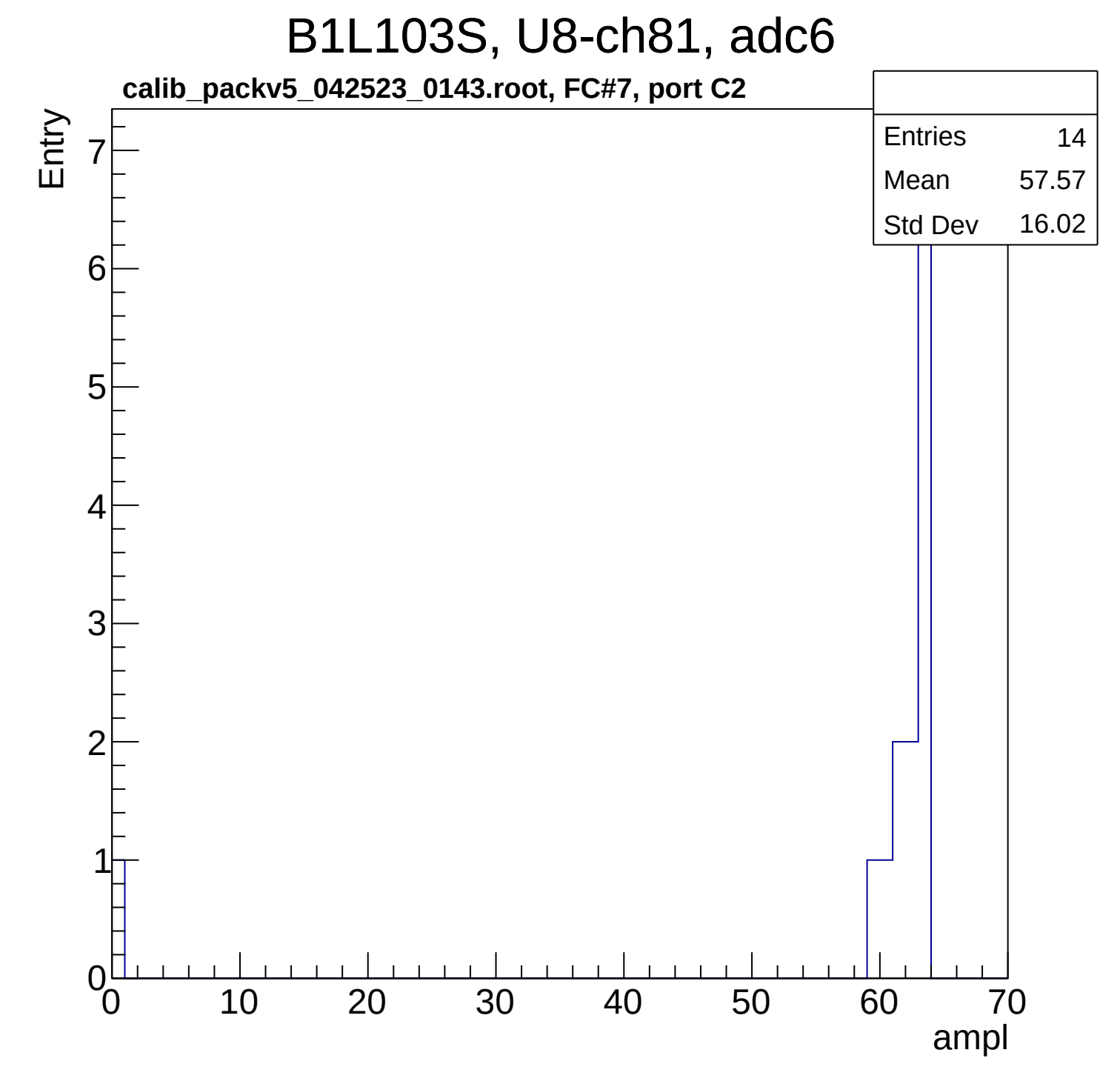

B1L103S, U8-ch81, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 35.77
Std Dev 3.053
Gaus mean : 35.8010
Gaus Width: 4.4122
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

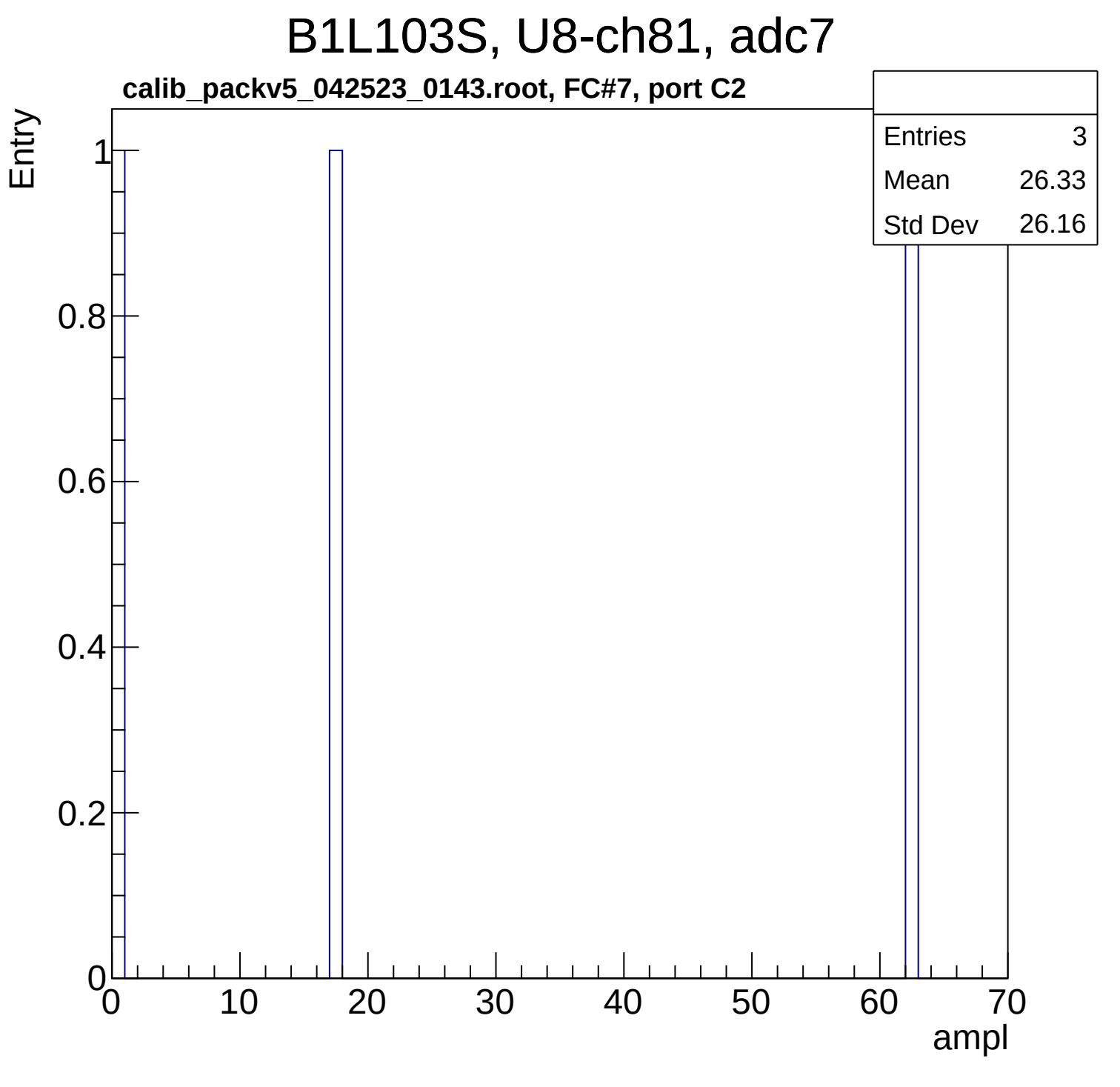

B1L103S, U8-ch81, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 76
Mean 42.33
Std Dev 3.611
Gaus mean : 42.8770
Gaus Width: 3.8444
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

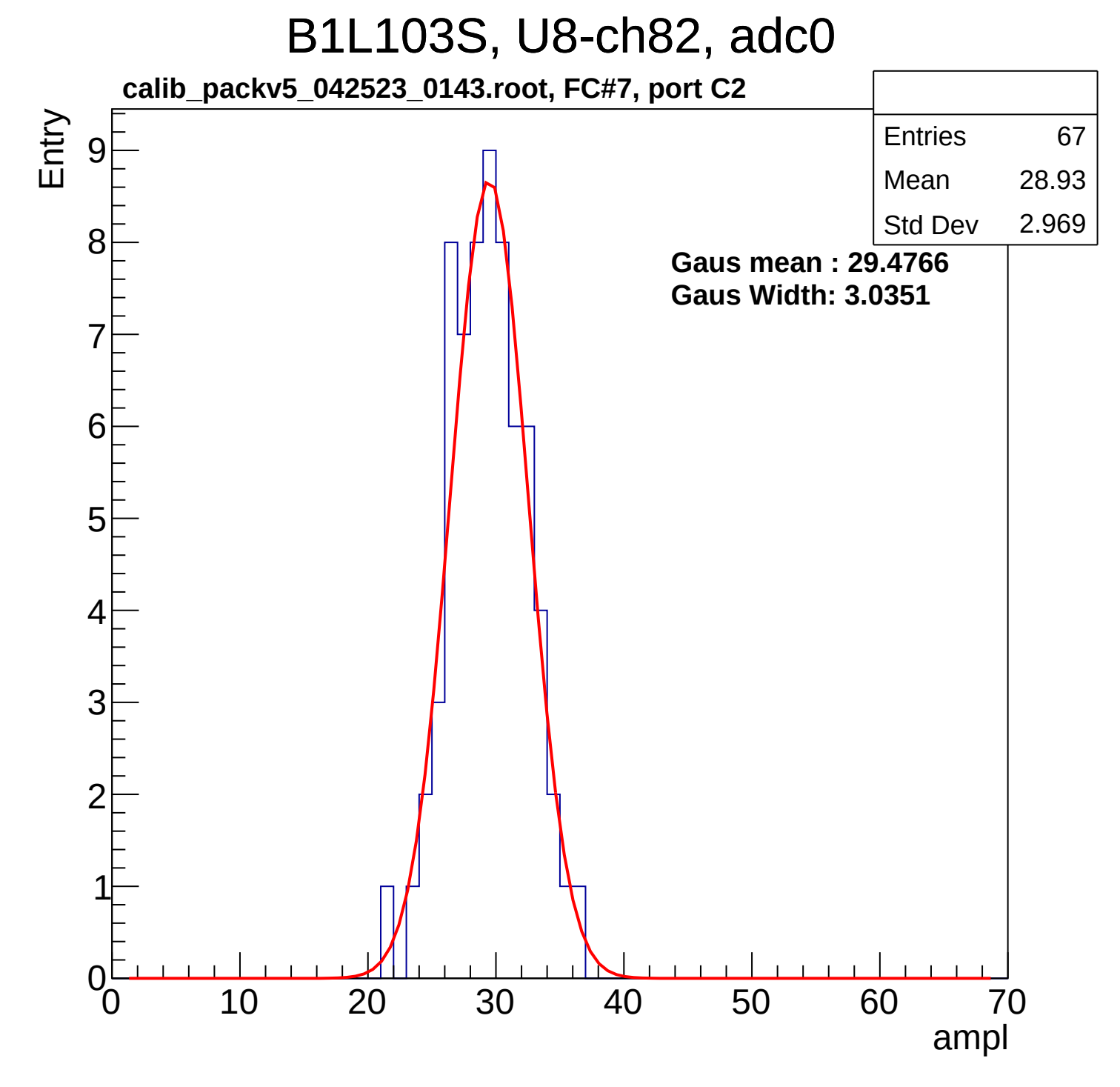

B1L103S, U8-ch81, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 48.7
Std Dev 3.784
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

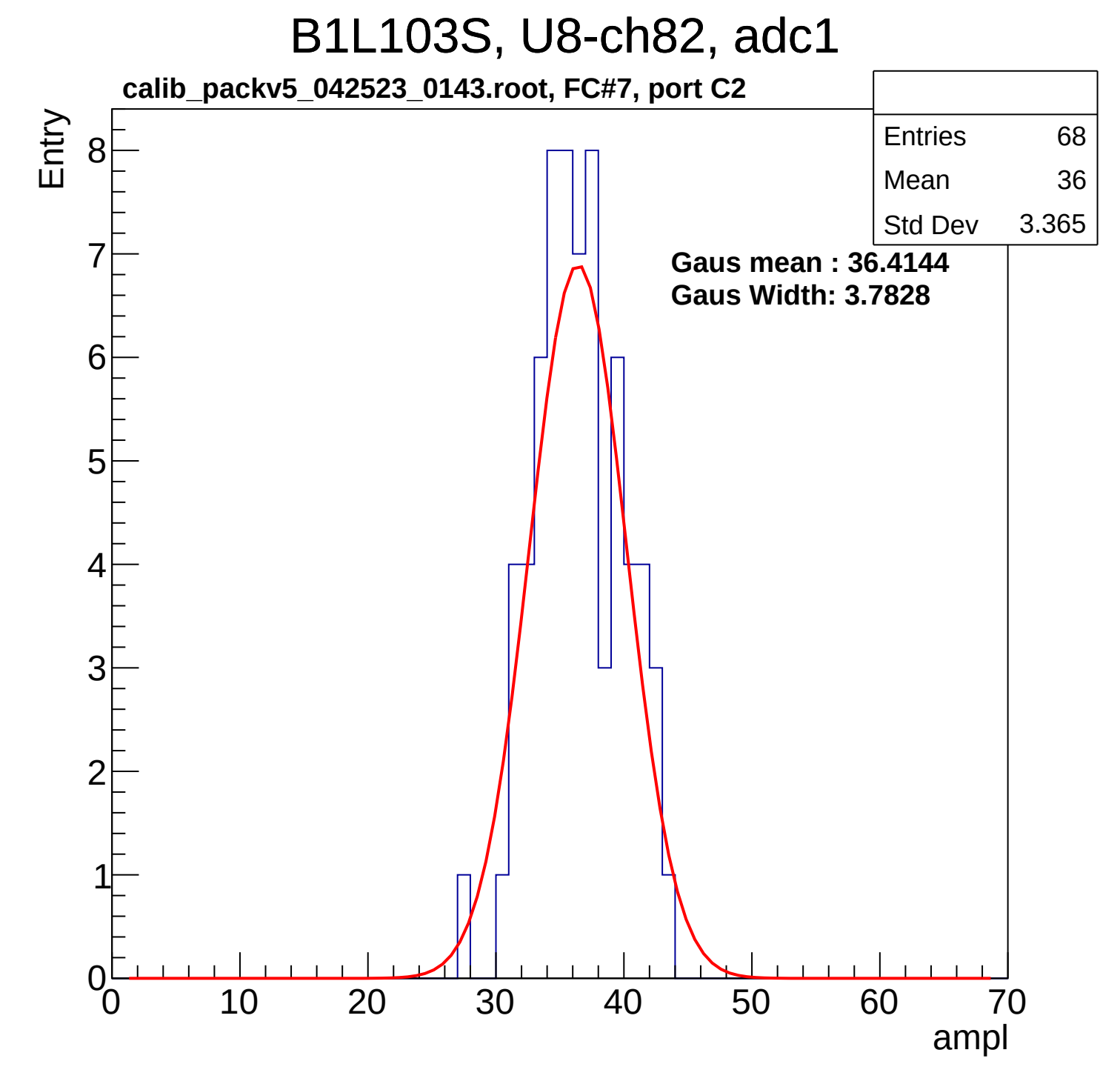

B1L103S, U8-ch81, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 54.84
Std Dev 3.526
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

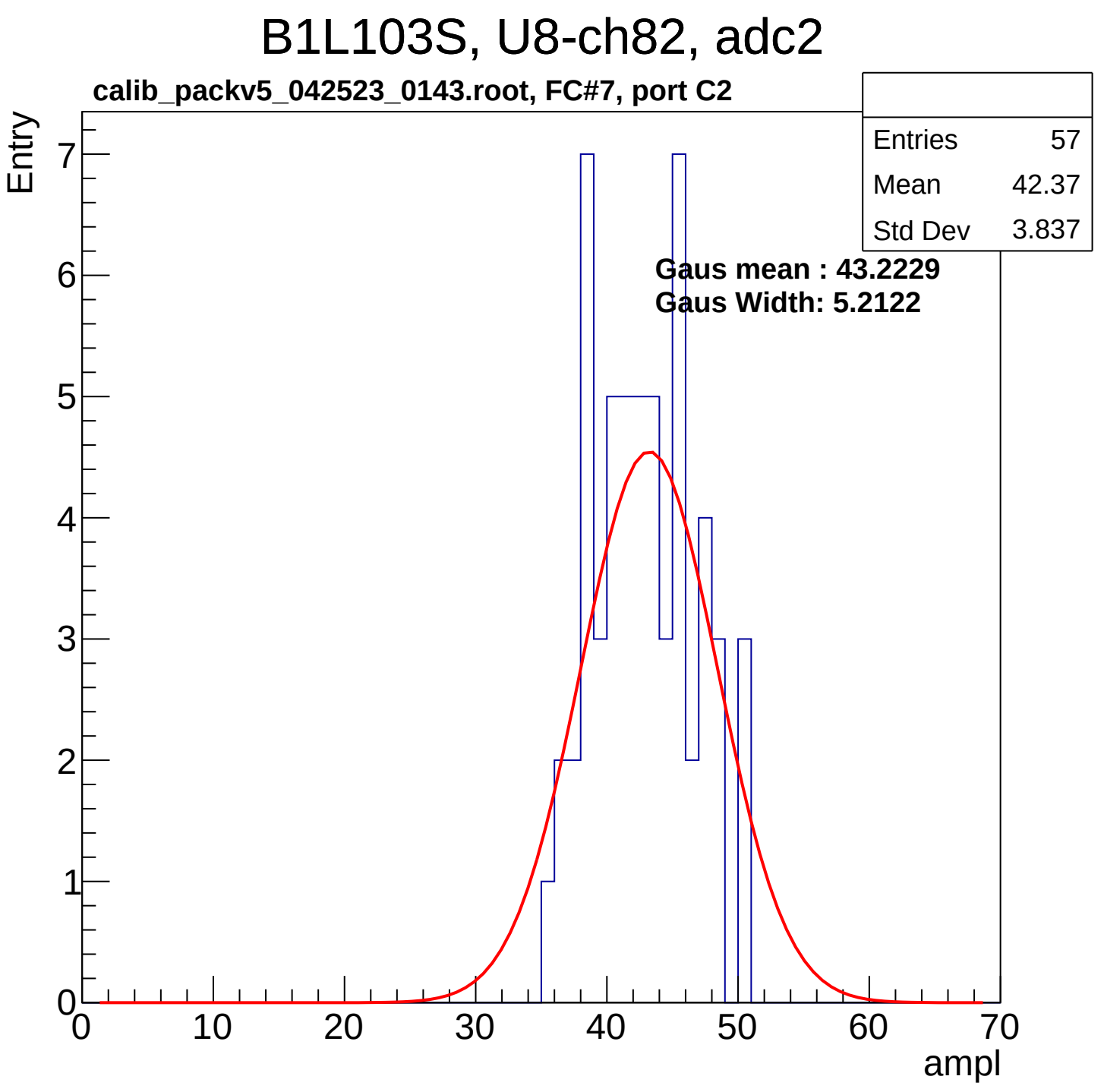

B1L103S, U8-ch81, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 39
Mean 59.05
Std Dev 2.855
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

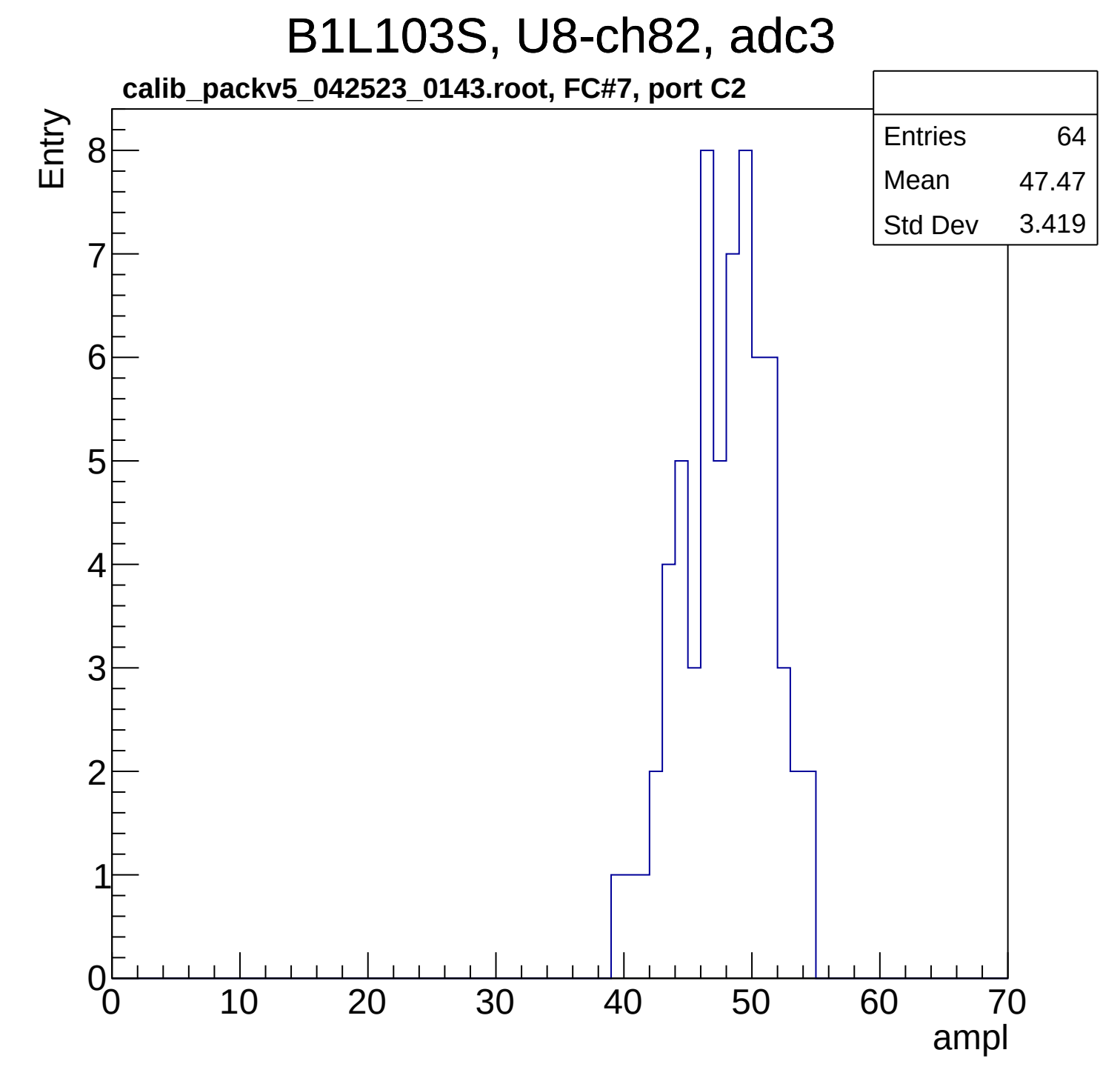

B1L103S, U8-ch81, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 14
Mean 57.57
Std Dev 16.02
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

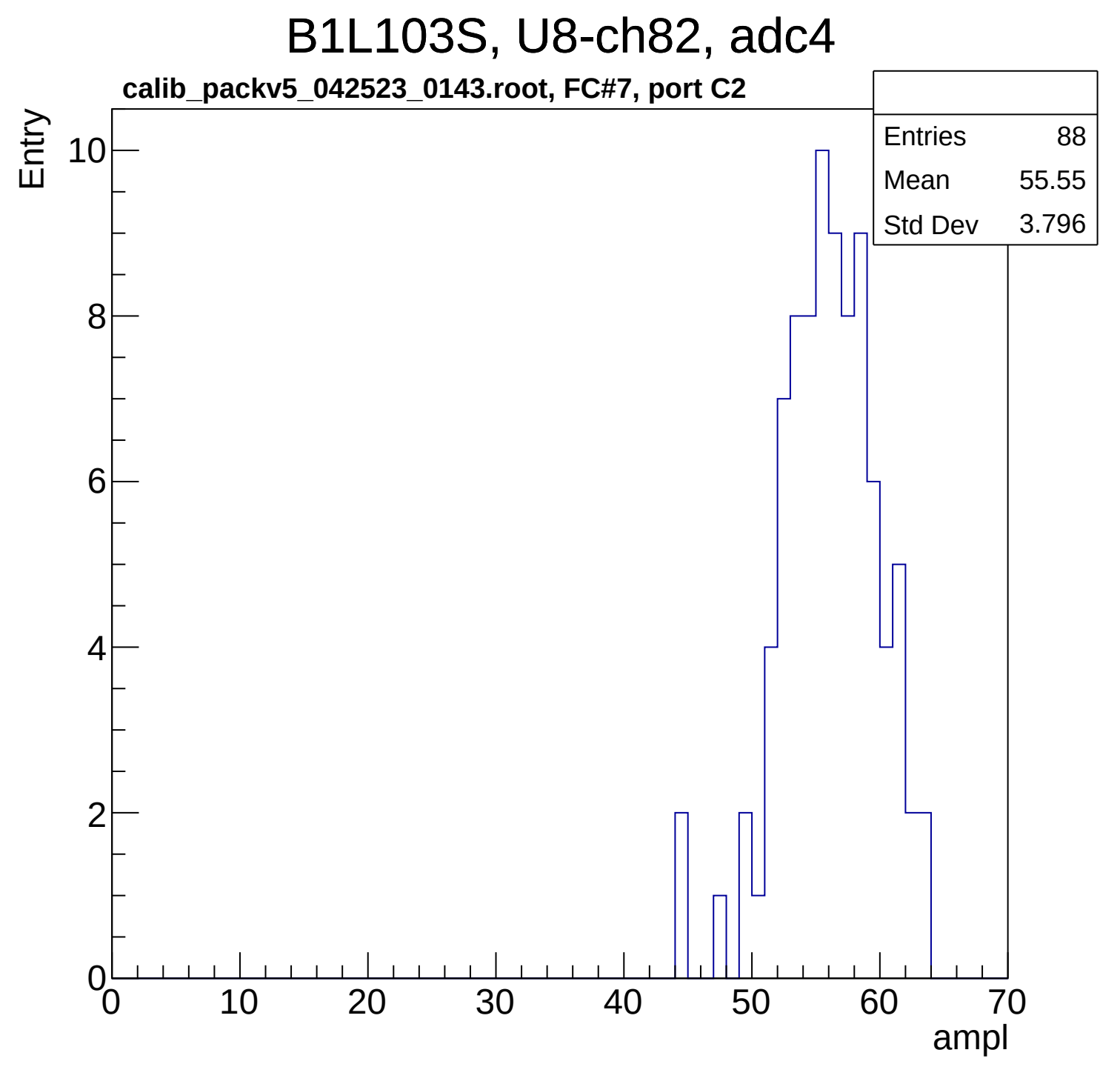

B1L103S, U8-ch81, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 26.33
Std Dev 26.16
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

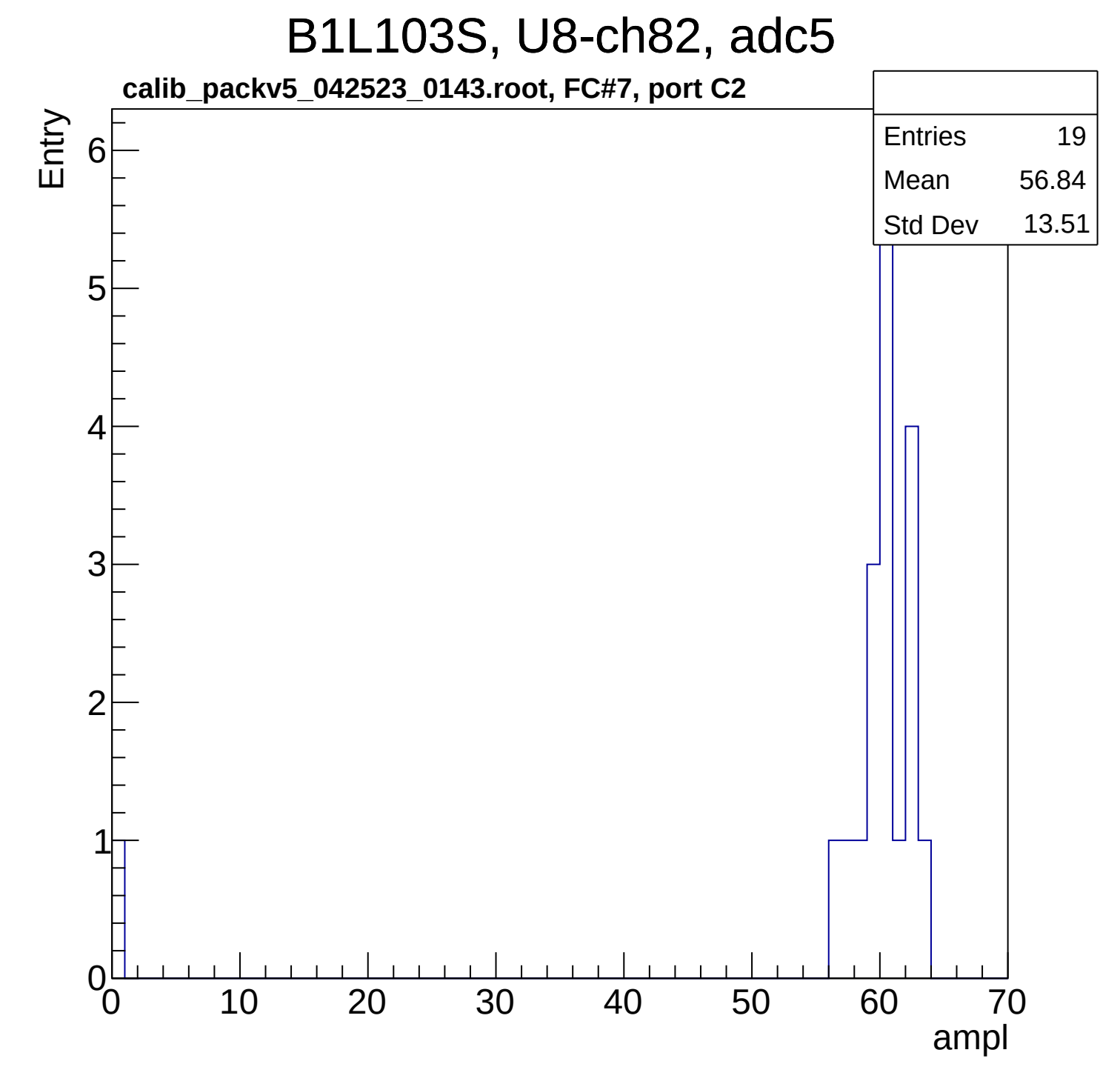

B1L103S, U8-ch82, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 28.93
Std Dev 2.969
Gaus mean : 29.4766
Gaus Width: 3.0351
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

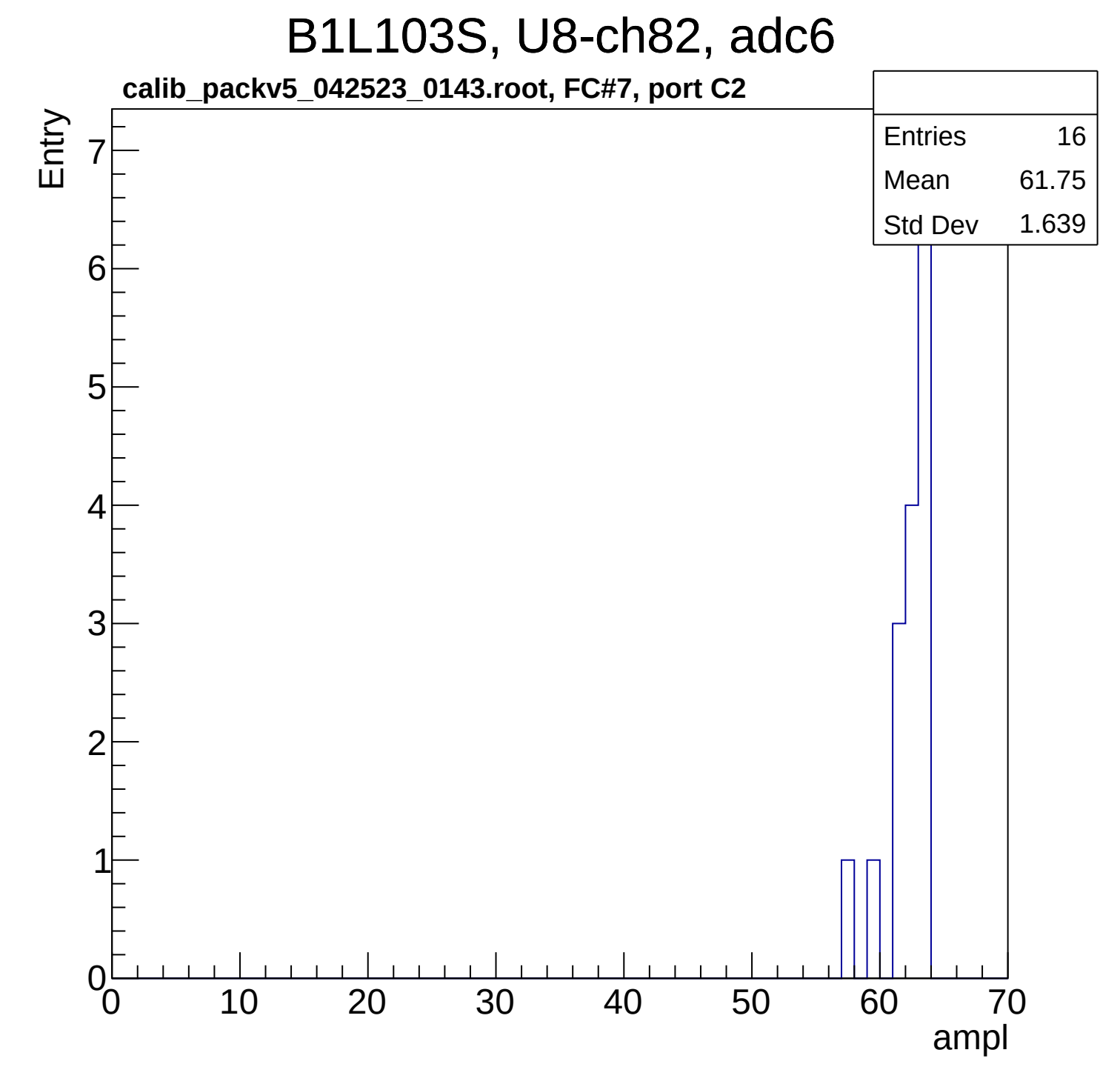

B1L103S, U8-ch82, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 36
Std Dev 3.365
Gaus mean : 36.4144
Gaus Width: 3.7828
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

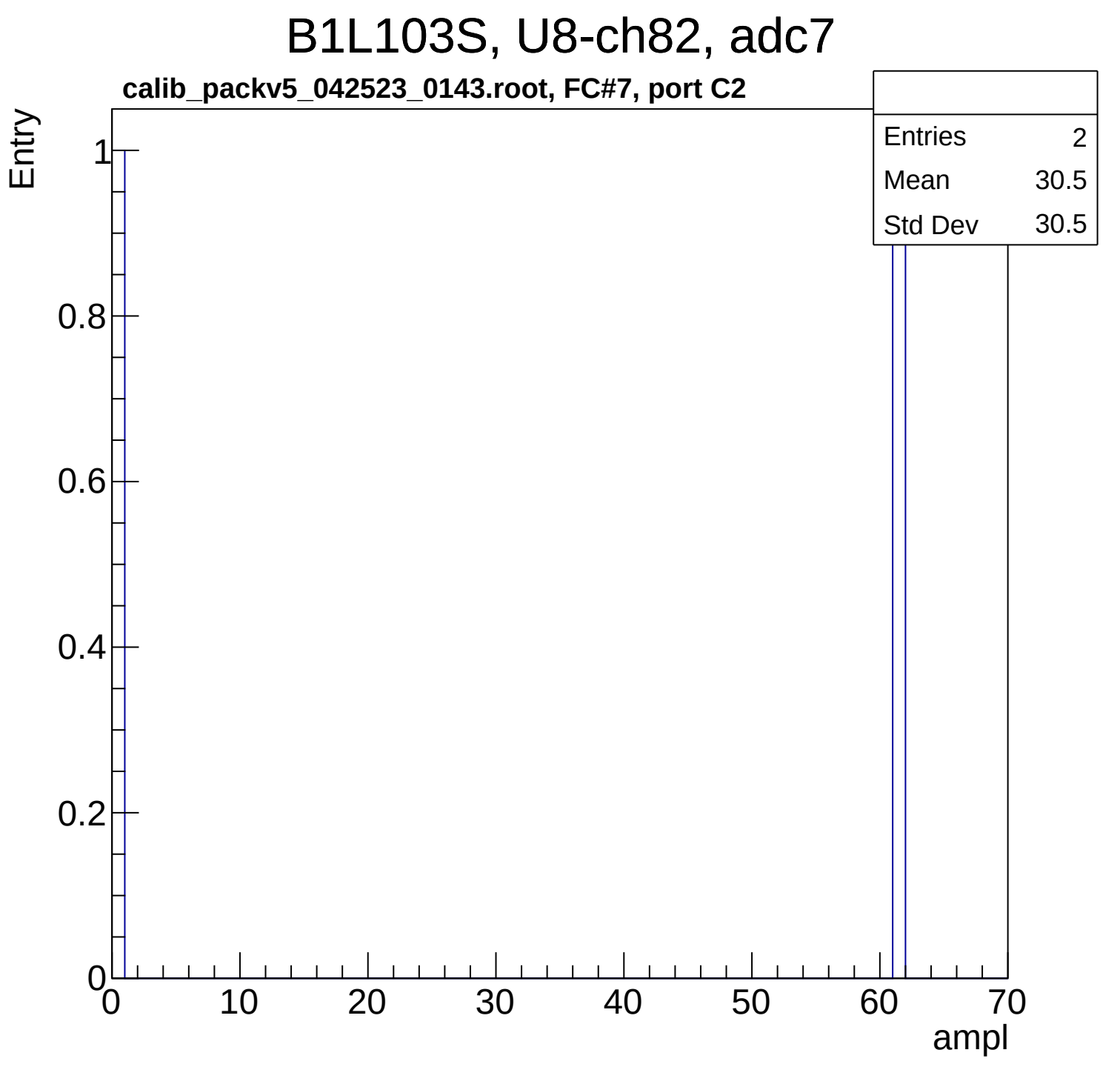

B1L103S, U8-ch82, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 42.37
Std Dev 3.837
Gaus mean : 43.2229
Gaus Width: 5.2122
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

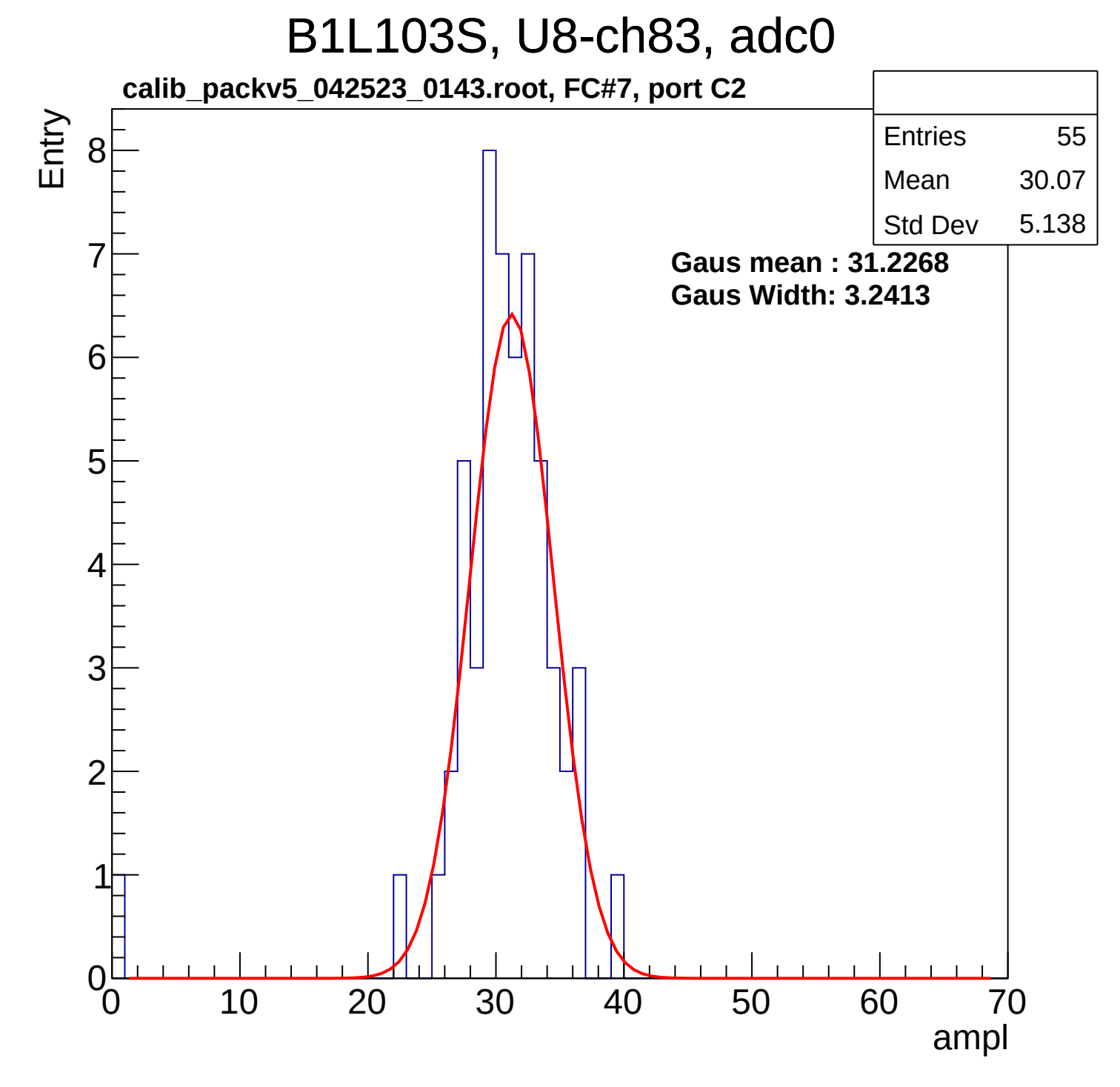

B1L103S, U8-ch82, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 47.47
Std Dev 3.419
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

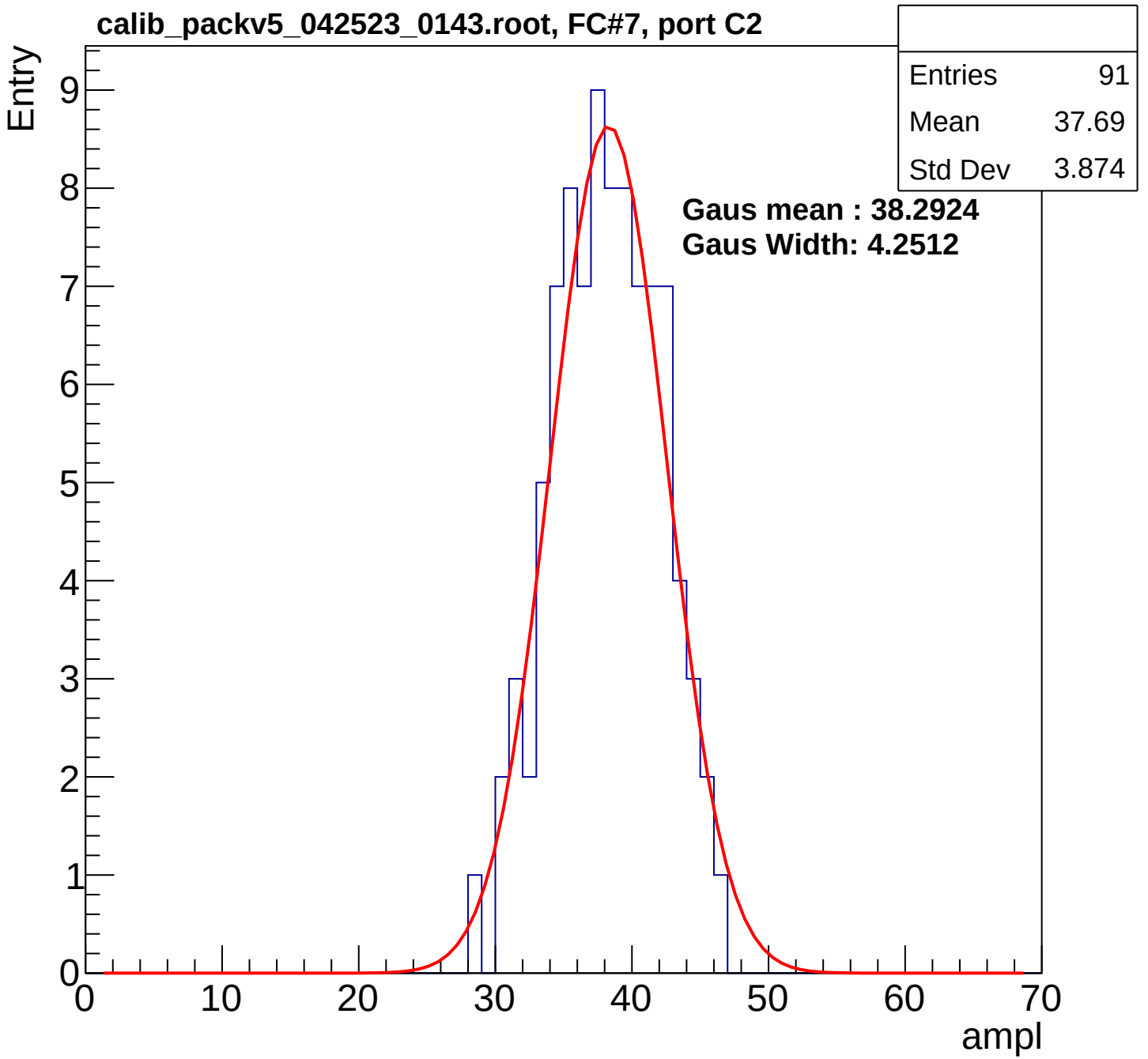

B1L103S, U8-ch82, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 88
Mean 55.55
Std Dev 3.796
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

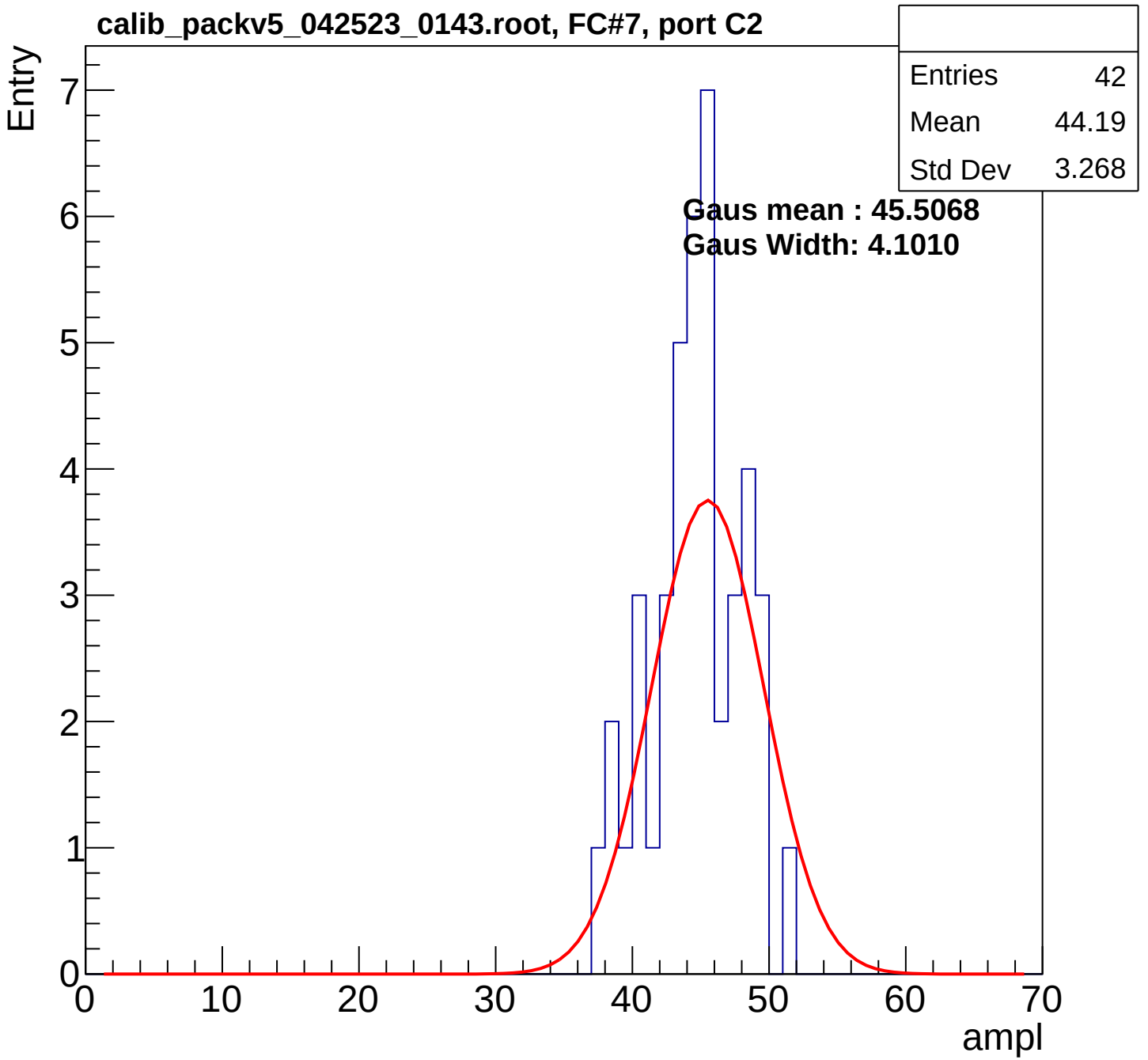

B1L103S, U8-ch82, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 19
Mean 56.84
Std Dev 13.51
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

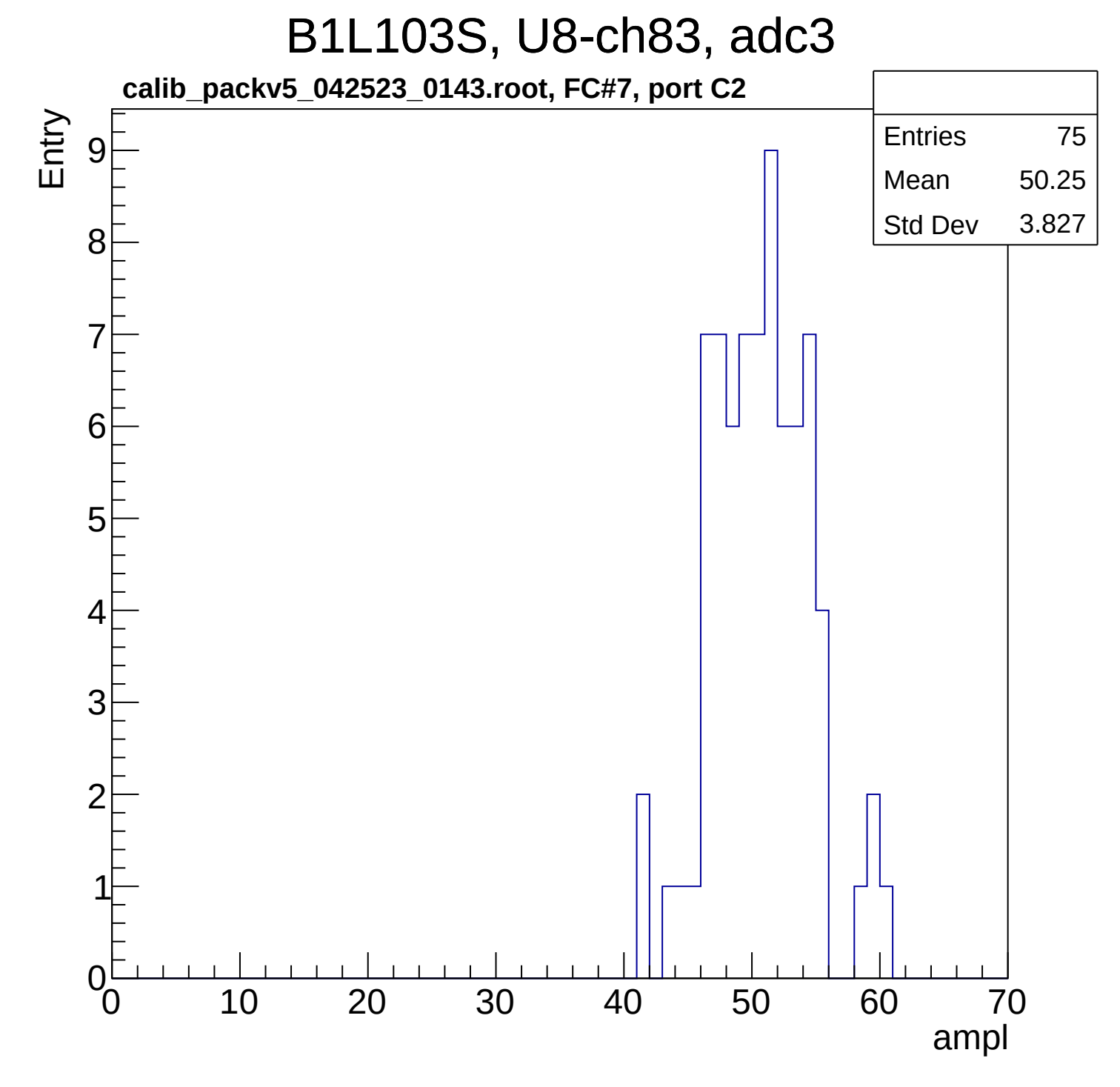

B1L103S, U8-ch82, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 16
Mean 61.75
Std Dev 1.639
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

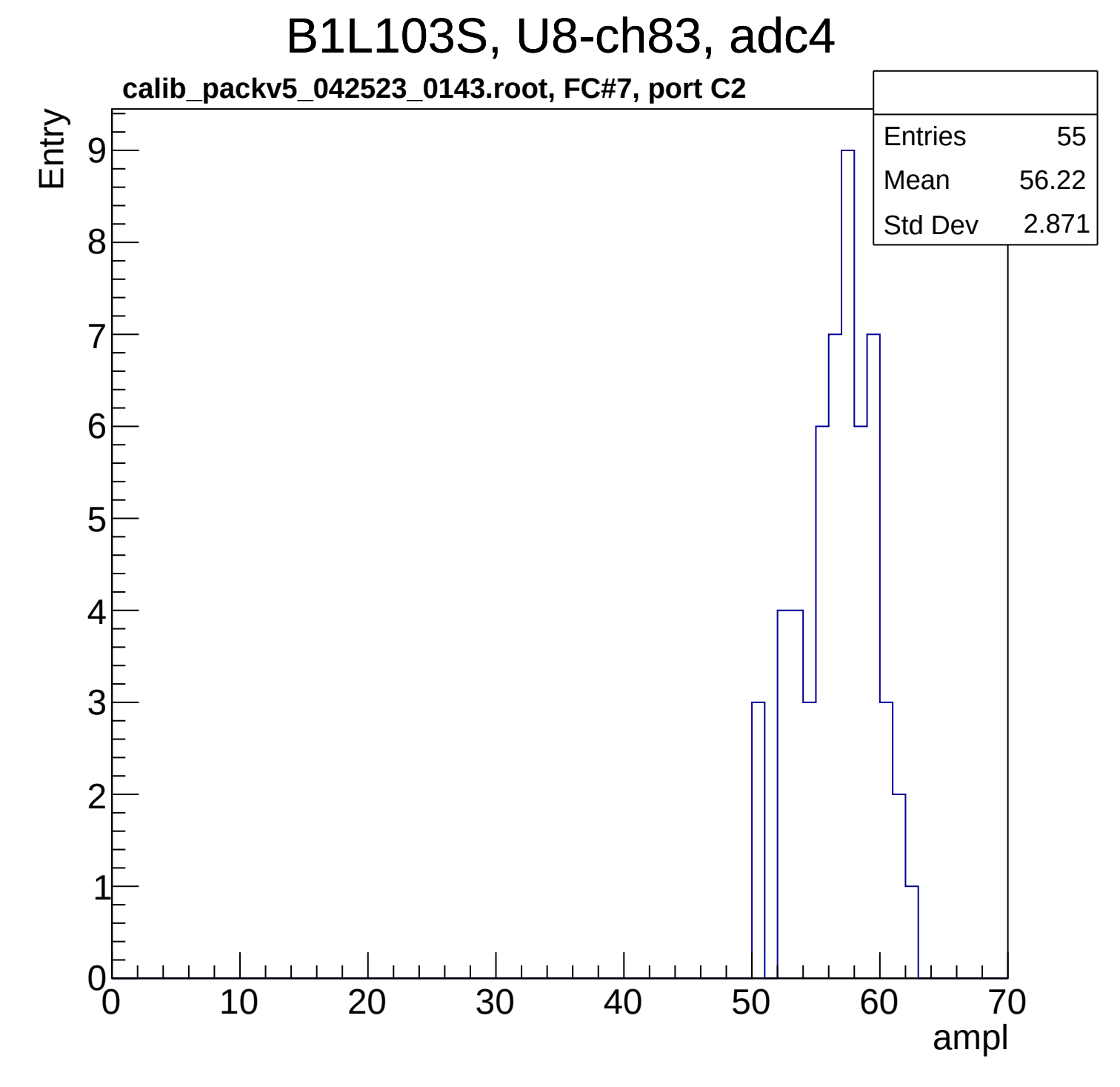

B1L103S, U8-ch82, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 30.5
Std Dev 30.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

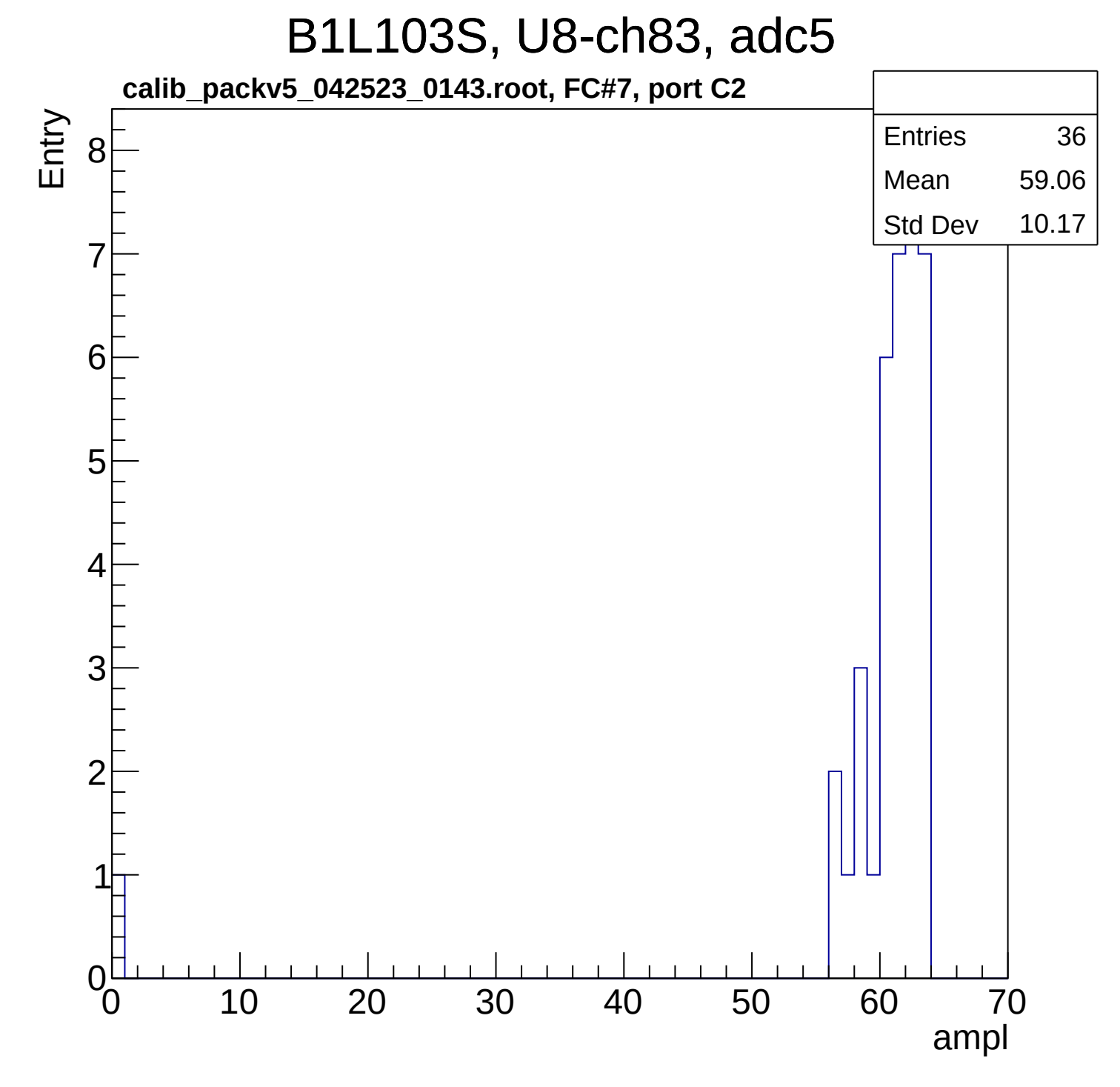

B1L103S, U8-ch83, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 30.07
Std Dev 5.138
Gaus mean : 31.2268
Gaus Width: 3.2413
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

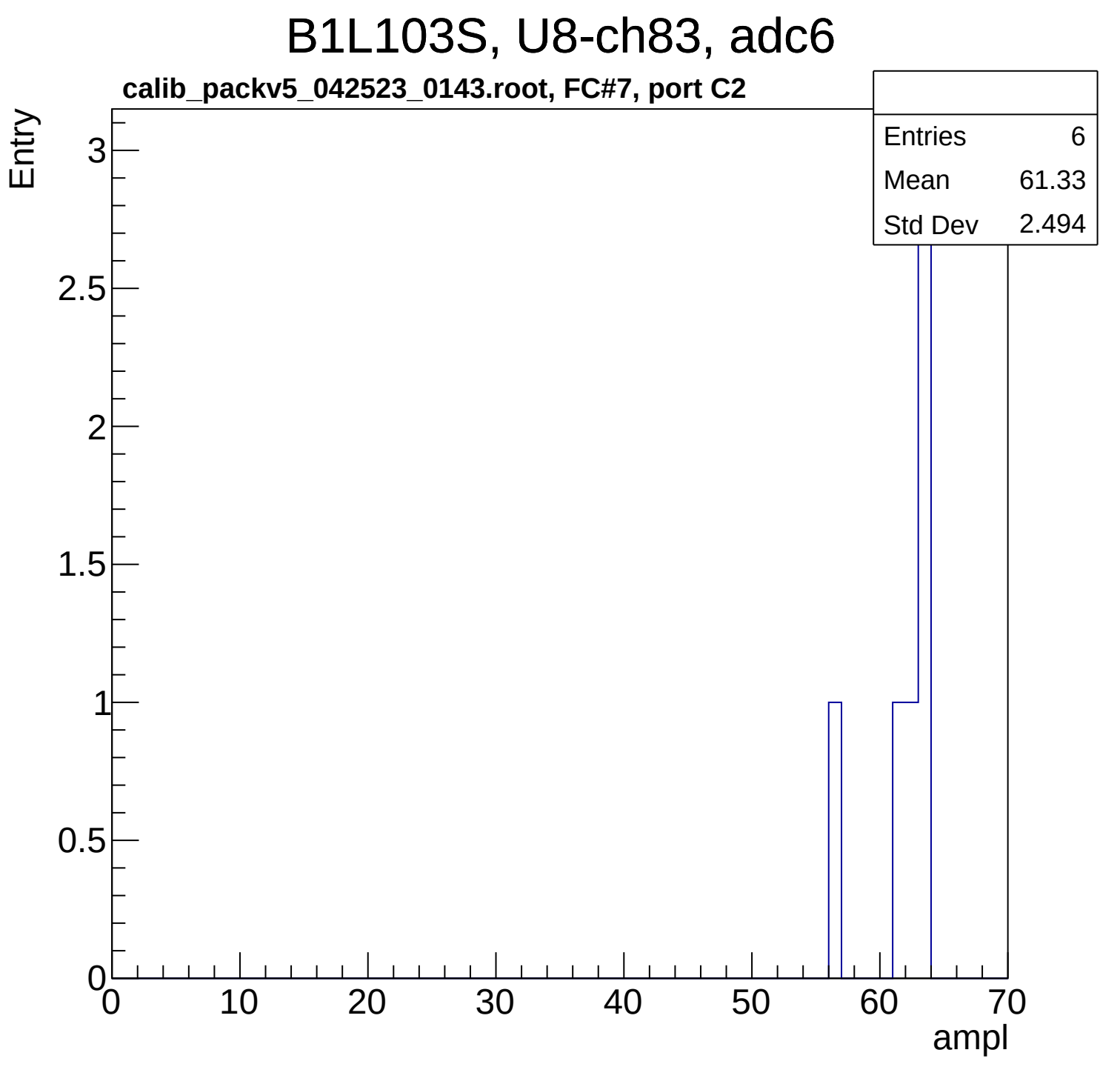

B1L103S, U8-ch83, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 91
Mean 37.69
Std Dev 3.874
Gaus mean : 38.2924
Gaus Width: 4.2512
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

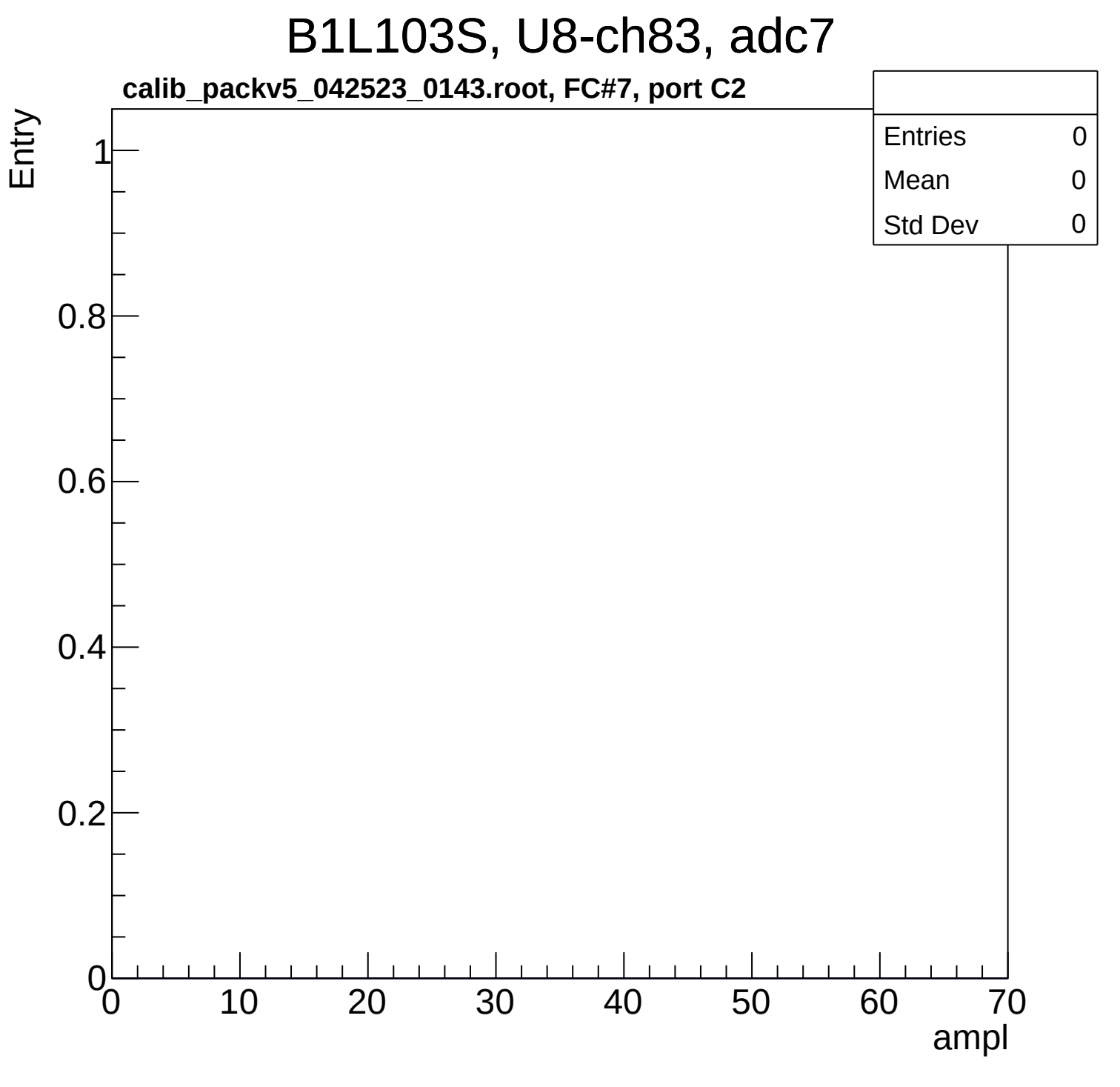

B1L103S, U8-ch83, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 42
Mean 44.19
Std Dev 3.268
Gaus mean : 45.5068
Gaus Width: 4.1010
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

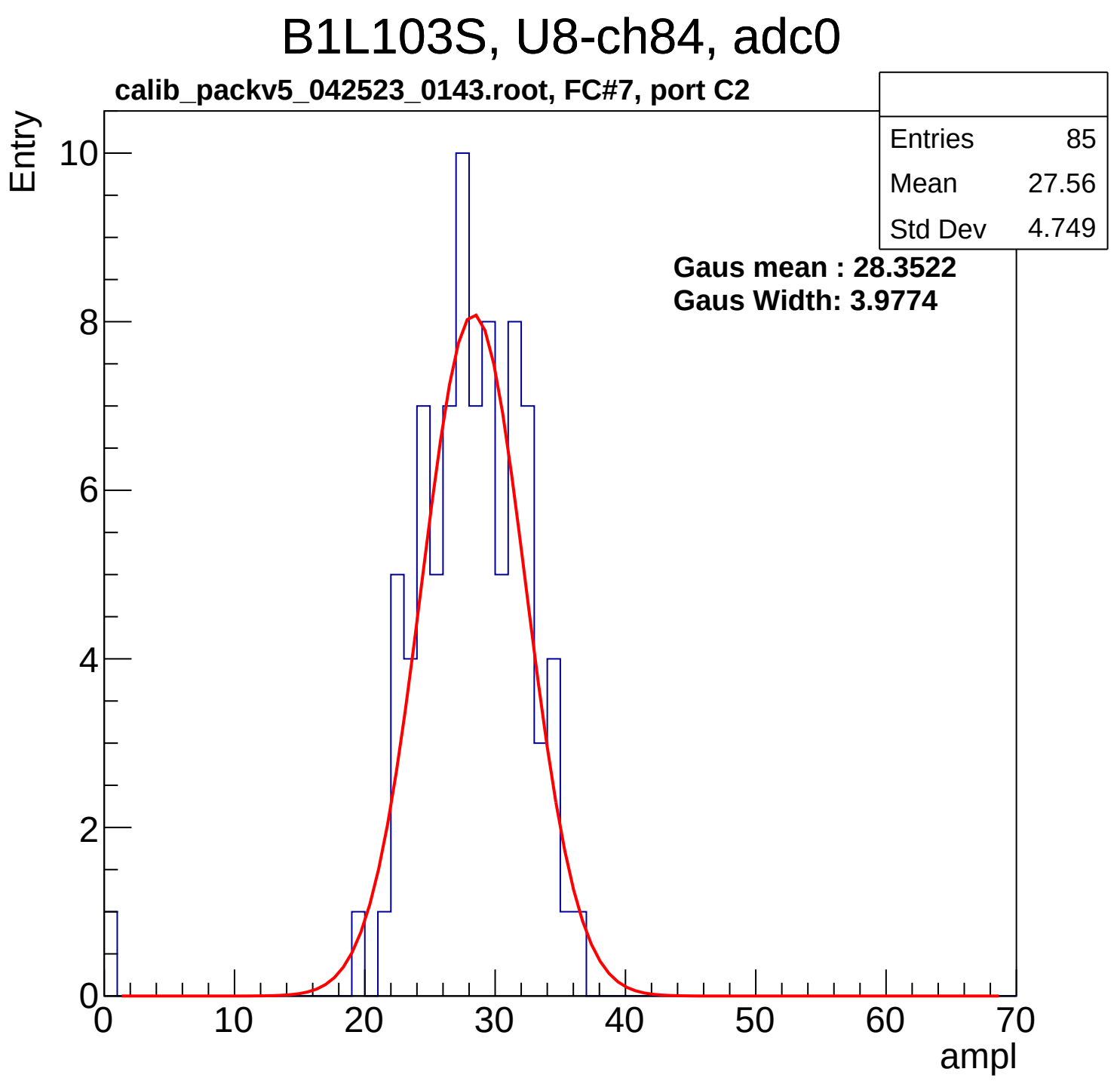

B1L103S, U8-ch83, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 50.25
Std Dev 3.827
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

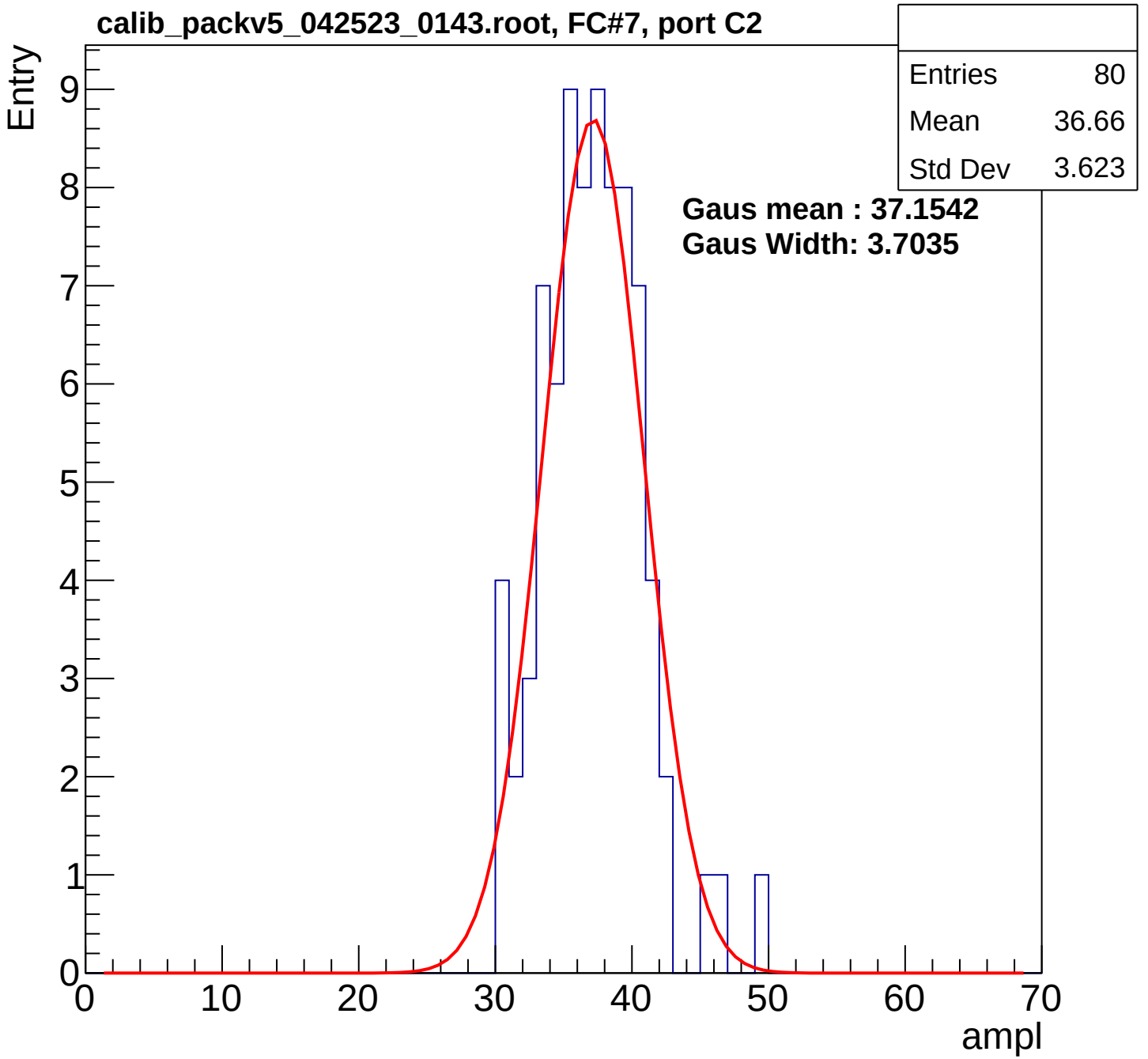

B1L103S, U8-ch83, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 56.22
Std Dev 2.871
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

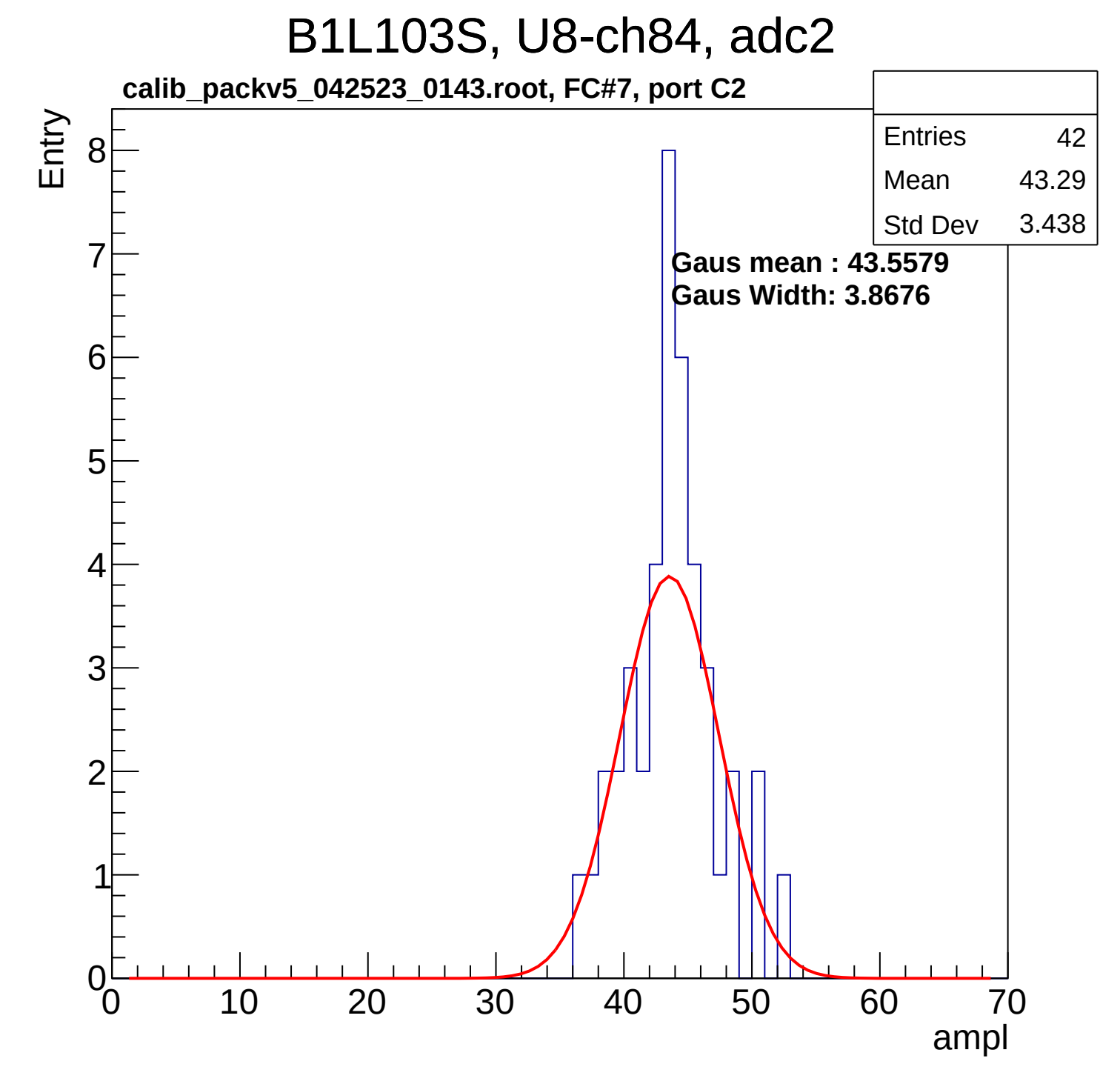

B1L103S, U8-ch83, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 36
Mean 59.06
Std Dev 10.17
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

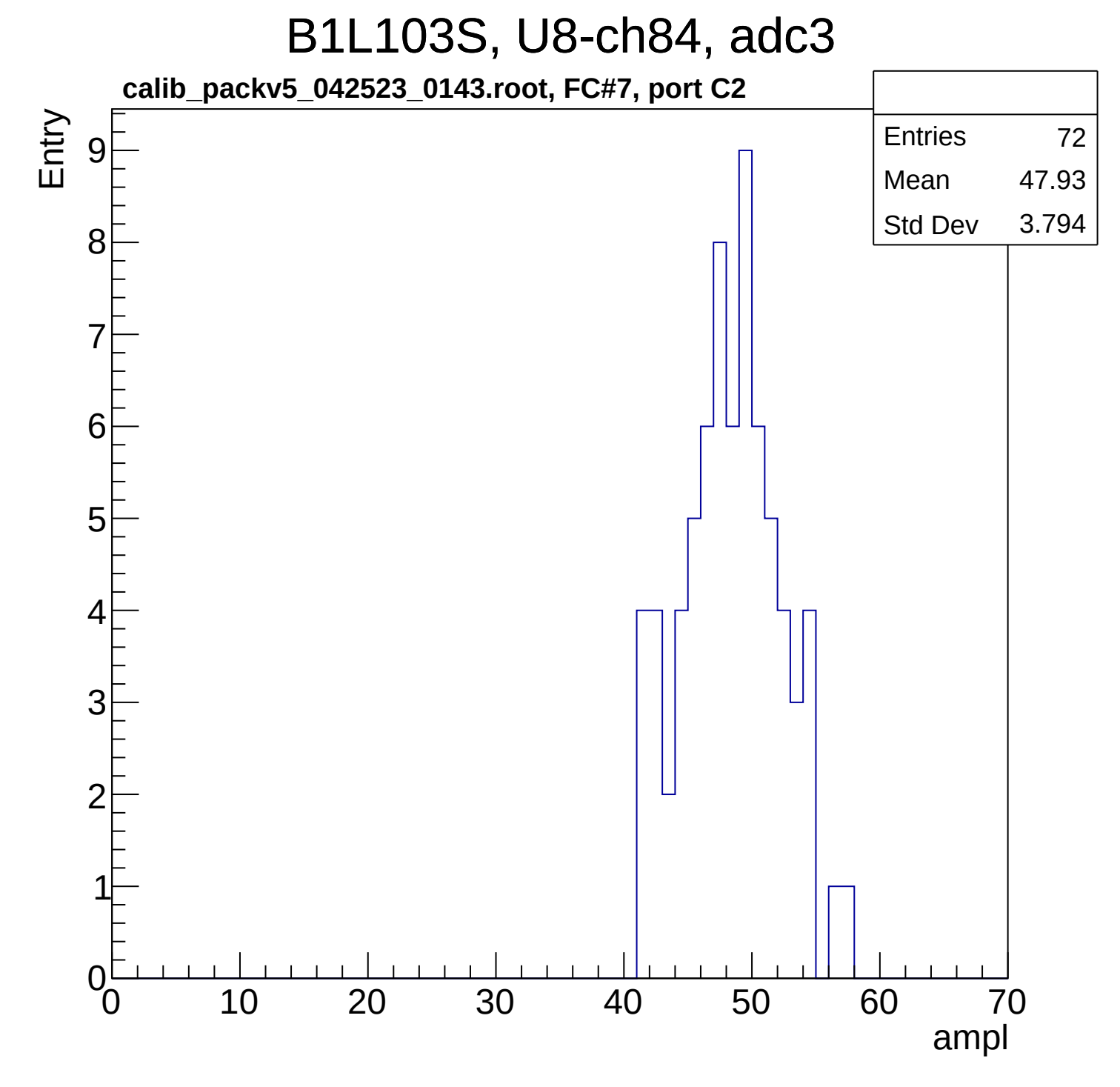

B1L103S, U8-ch83, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 61.33
Std Dev 2.494
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

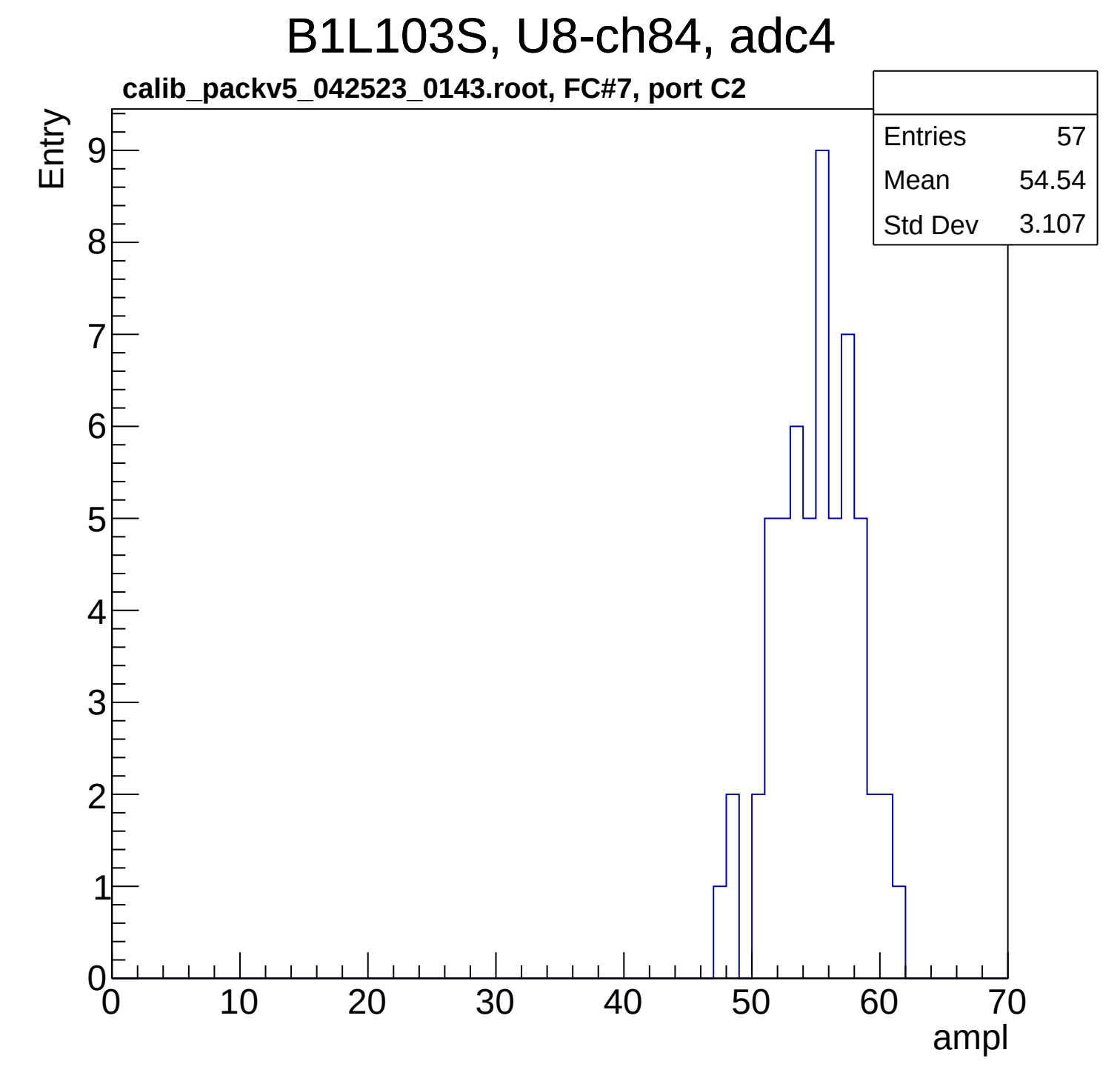

B1L103S, U8-ch83, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

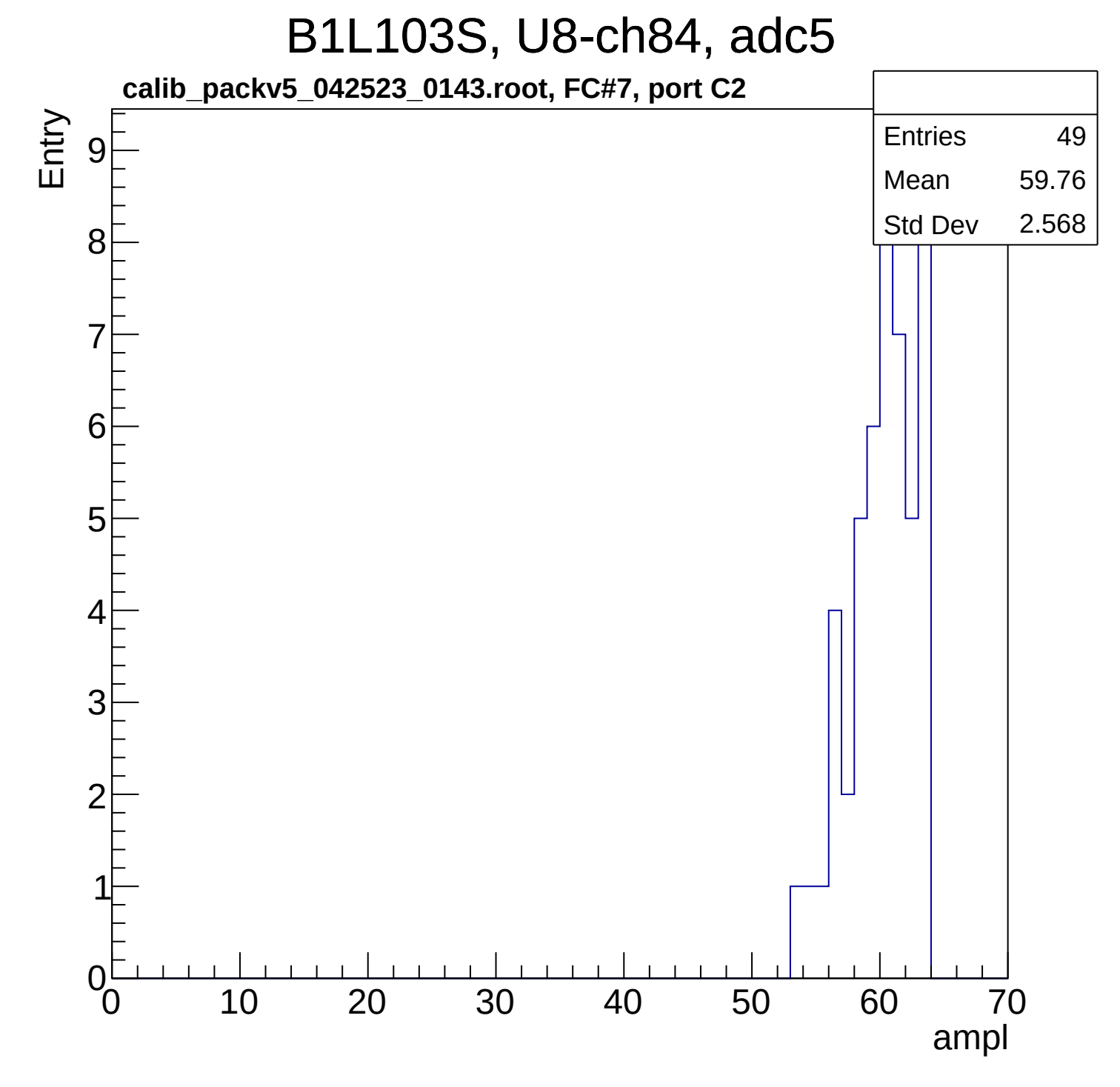

B1L103S, U8-ch84, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 85
Mean 27.56
Std Dev 4.749
Gaus mean : 28.3522
Gaus Width: 3.9774
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

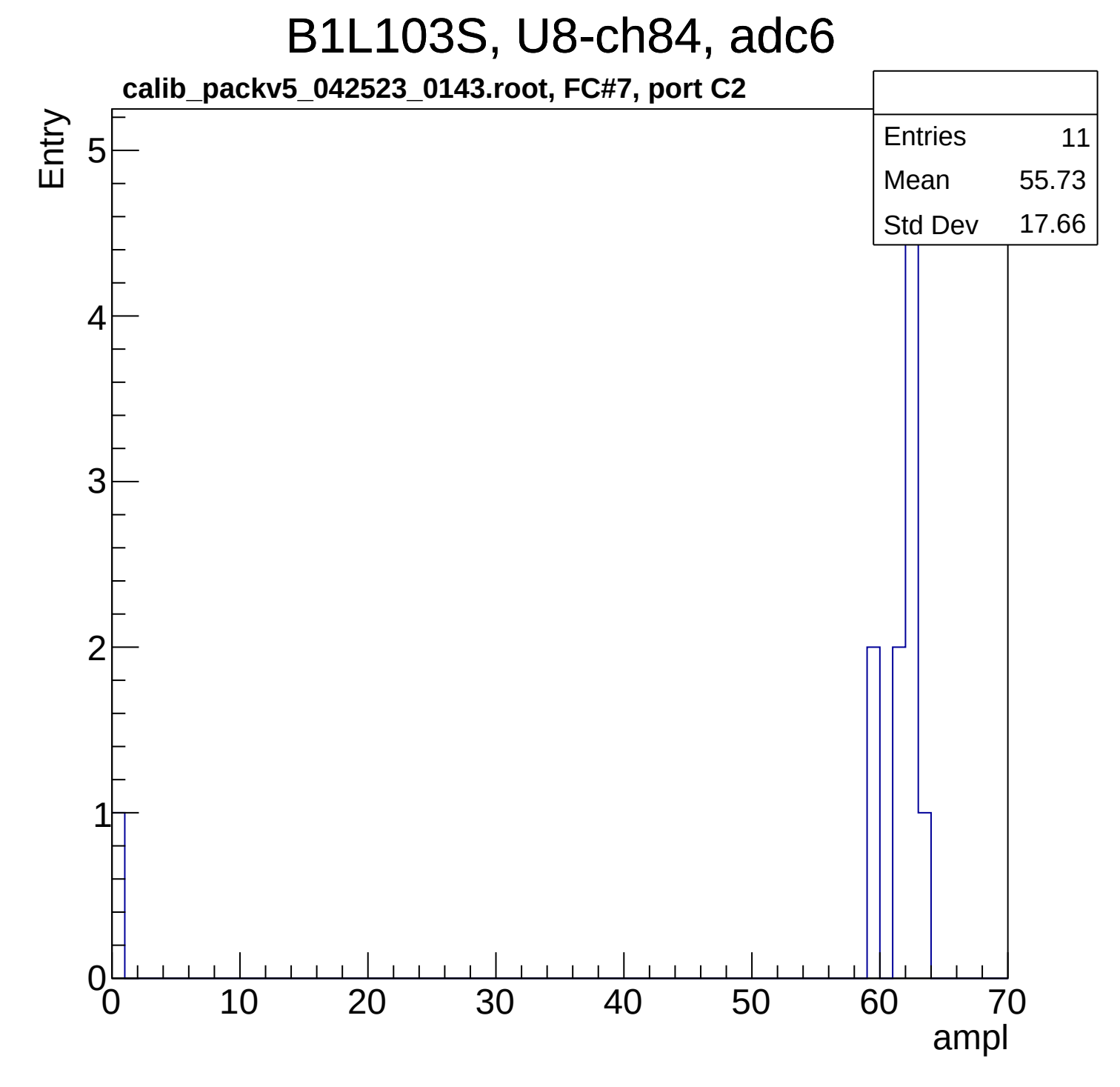

B1L103S, U8-ch84, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 80
Mean 36.66
Std Dev 3.623
Gaus mean : 37.1542
Gaus Width: 3.7035
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

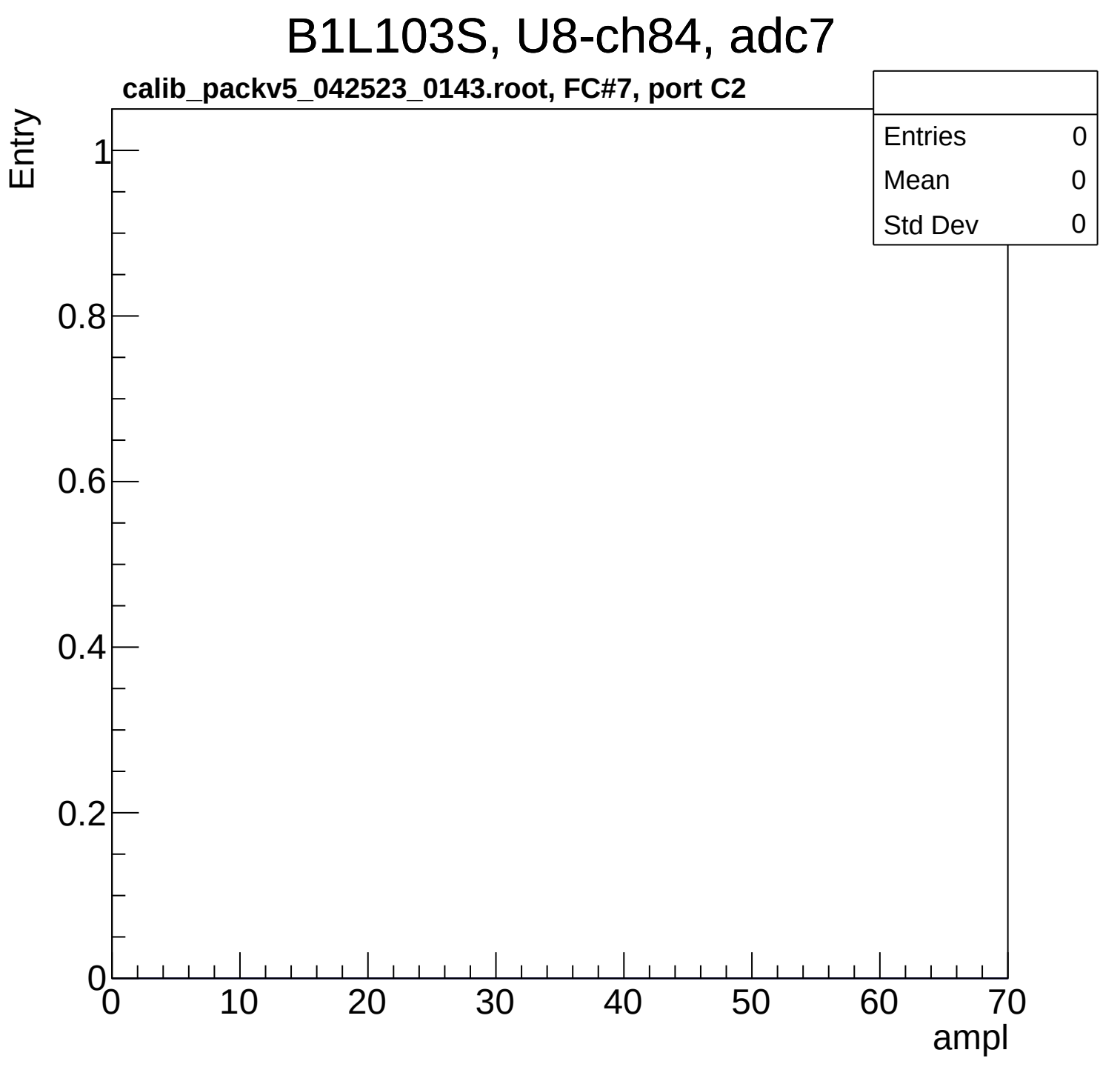

B1L103S, U8-ch84, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 42
Mean 43.29
Std Dev 3.438
Gaus mean : 43.5579
Gaus Width: 3.8676
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

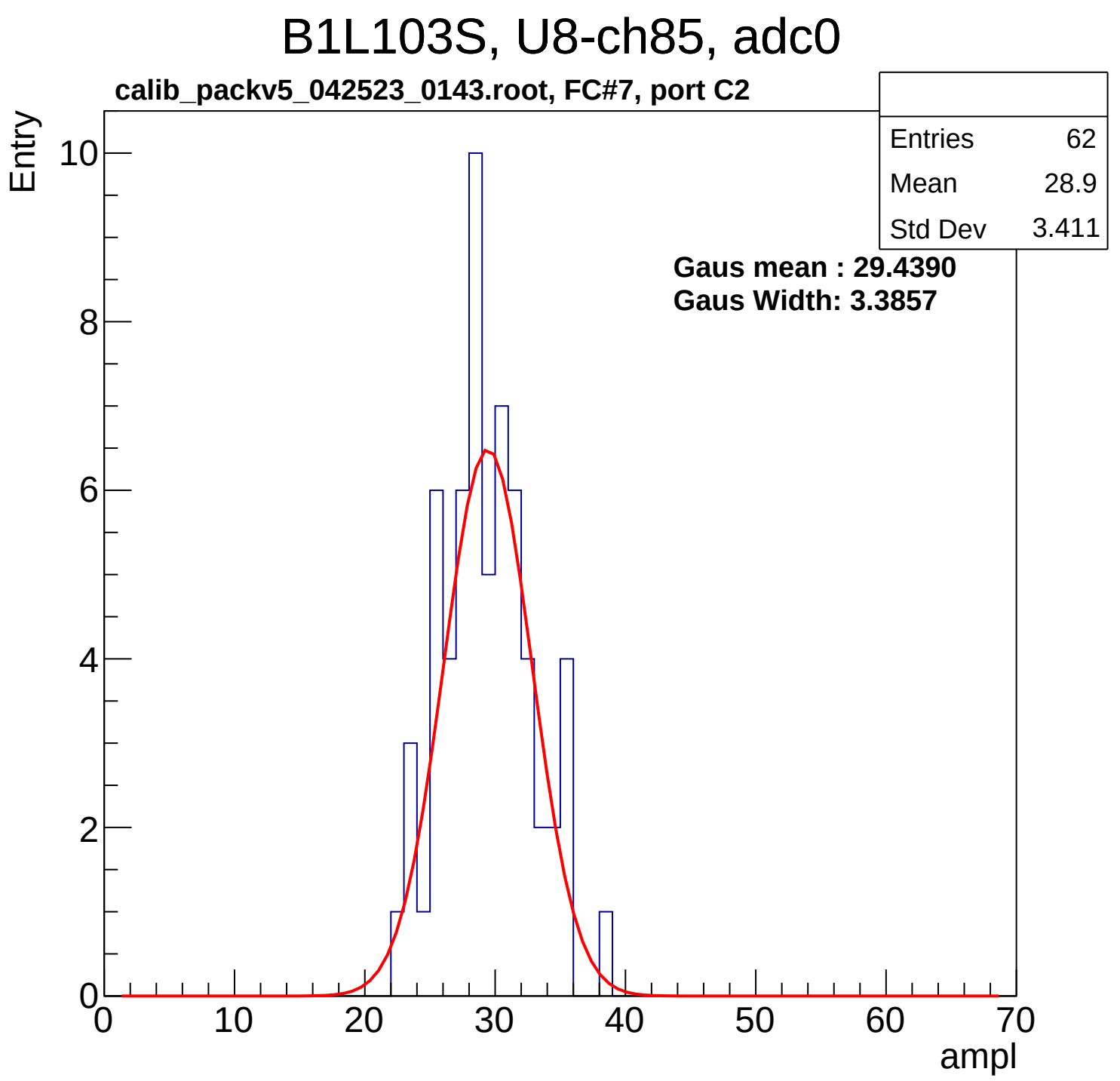

B1L103S, U8-ch84, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 47.93
Std Dev 3.794
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

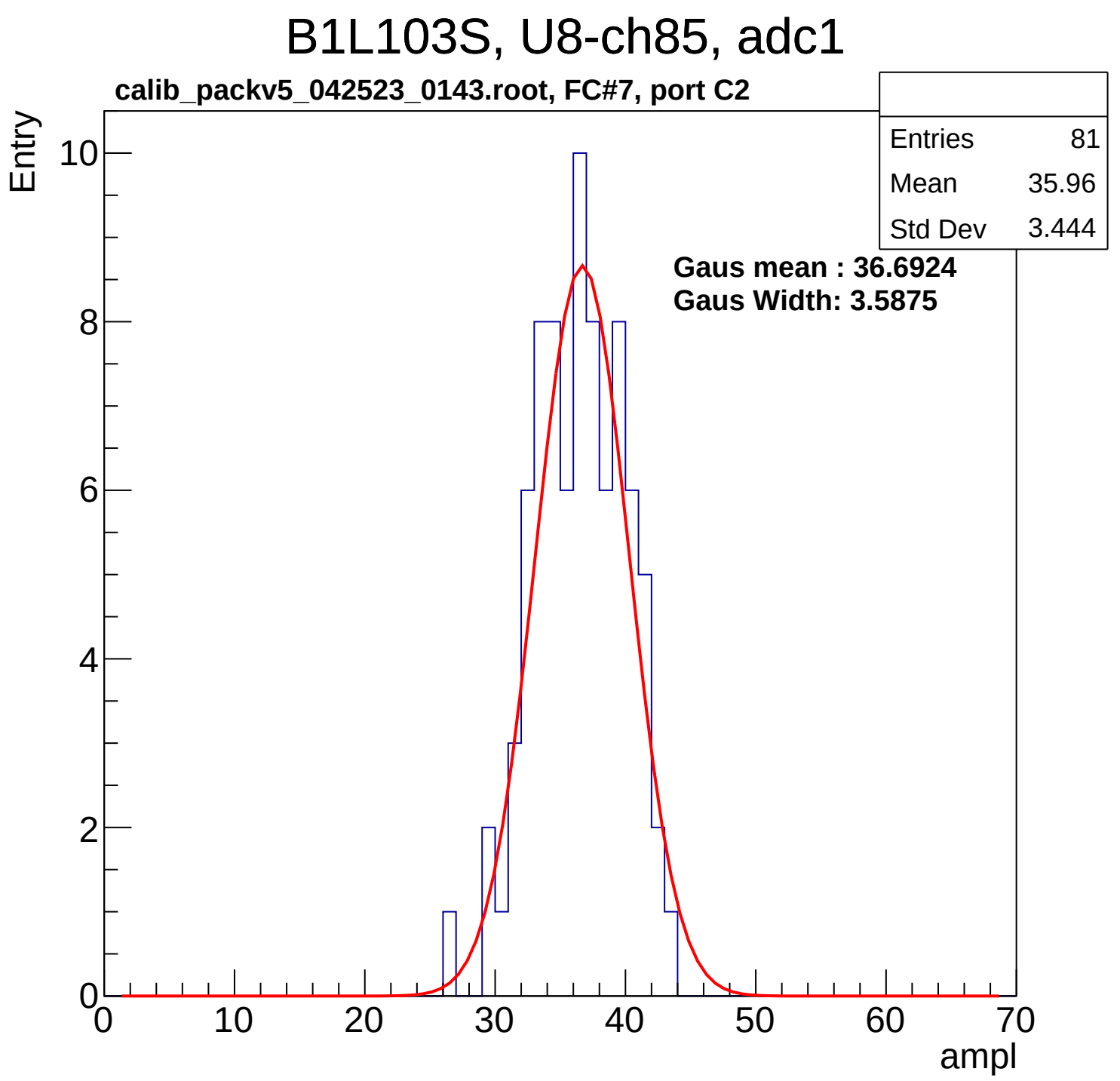

B1L103S, U8-ch84, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 54.54
Std Dev 3.107
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

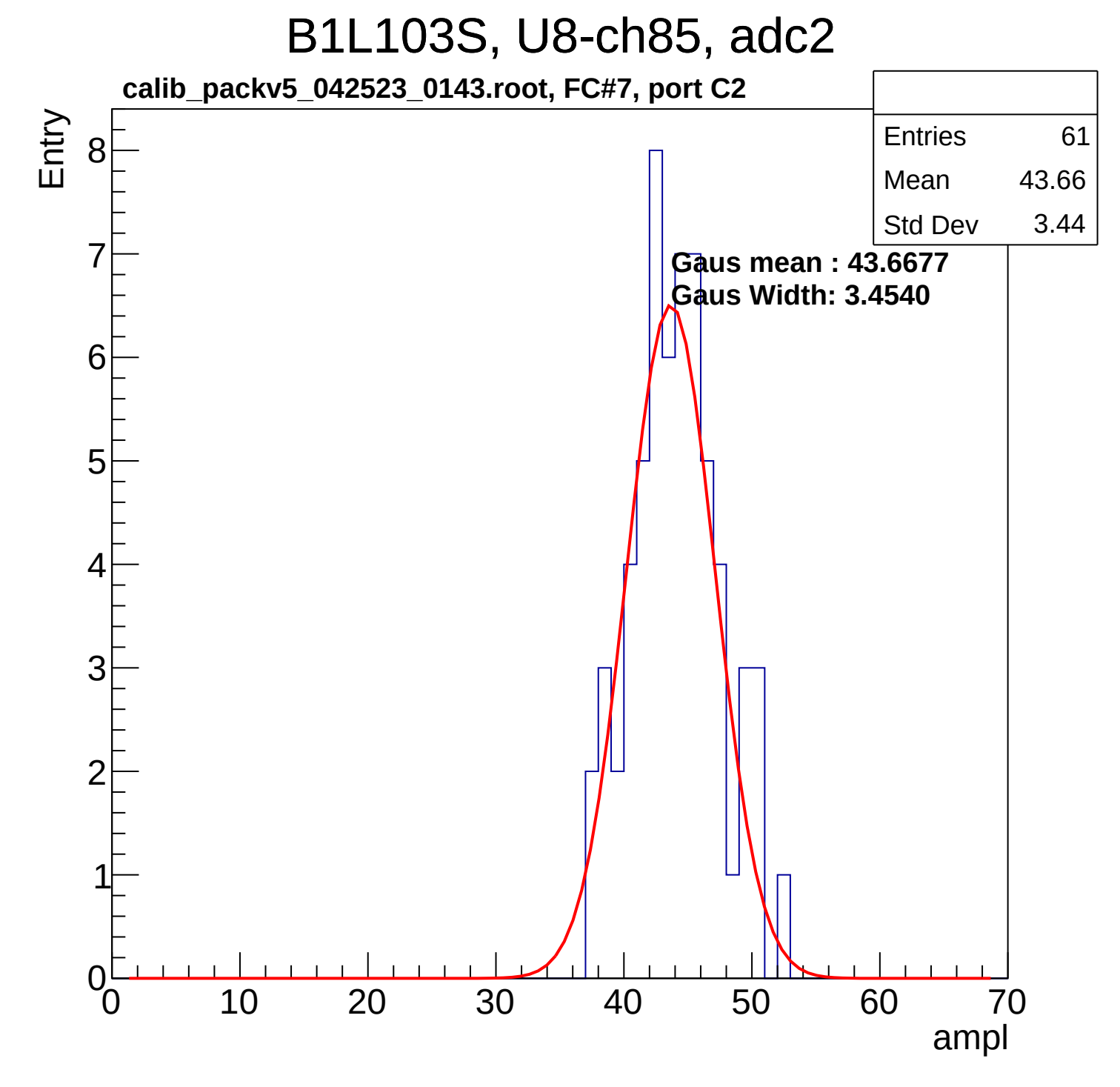

B1L103S, U8-ch84, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 59.76
Std Dev 2.568
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

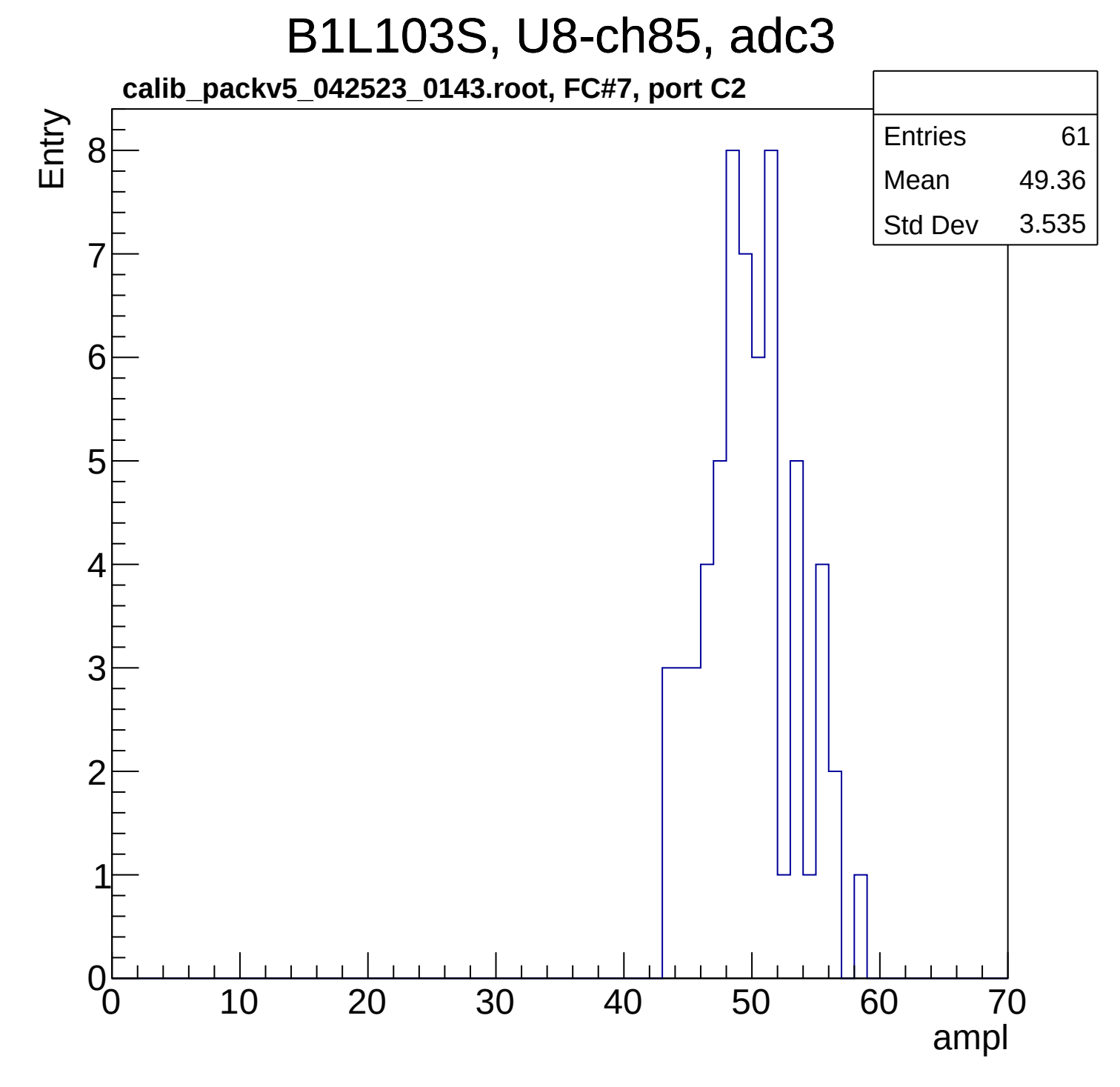

B1L103S, U8-ch84, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 11
Mean 55.73
Std Dev 17.66
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

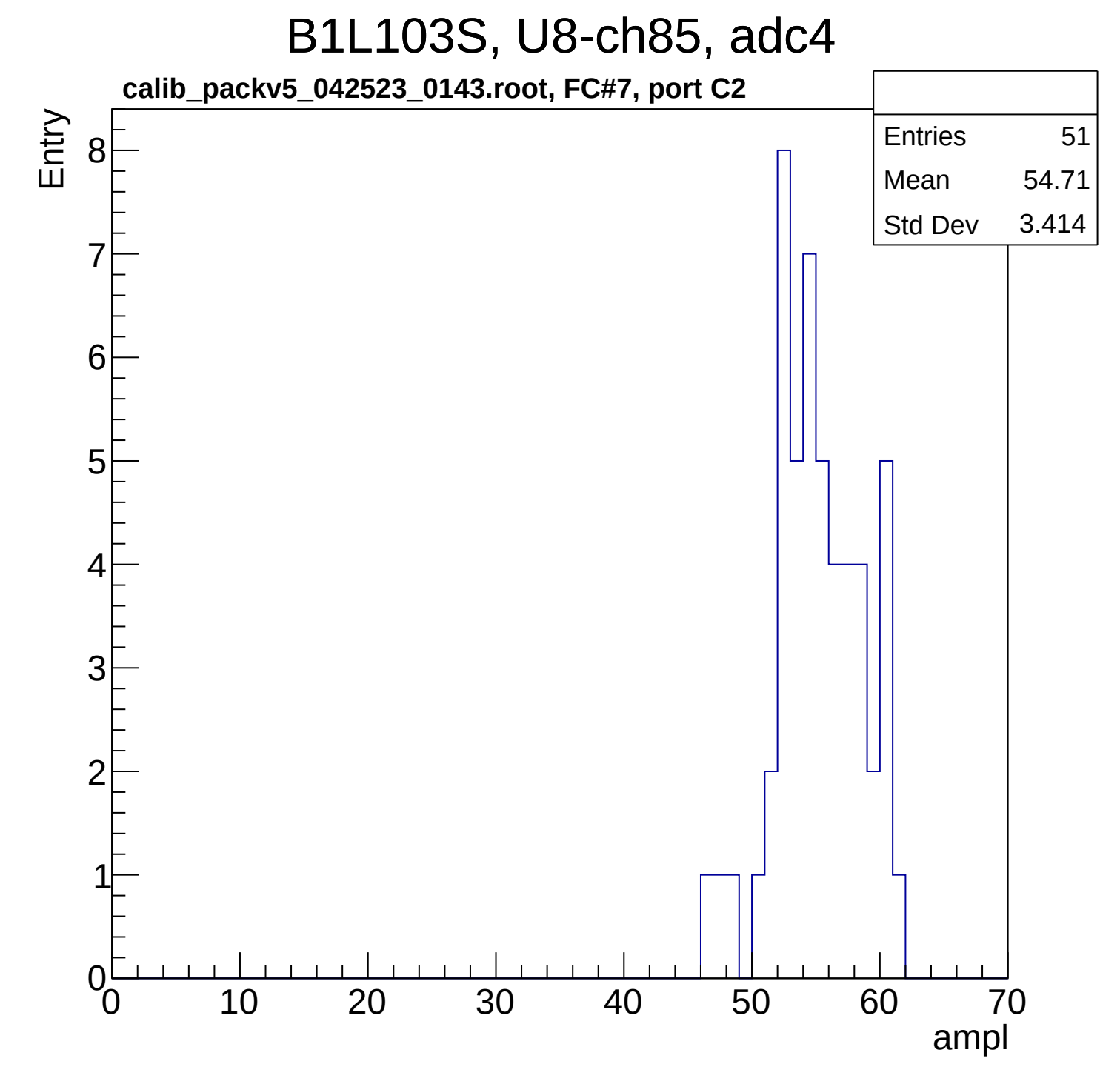

B1L103S, U8-ch84, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

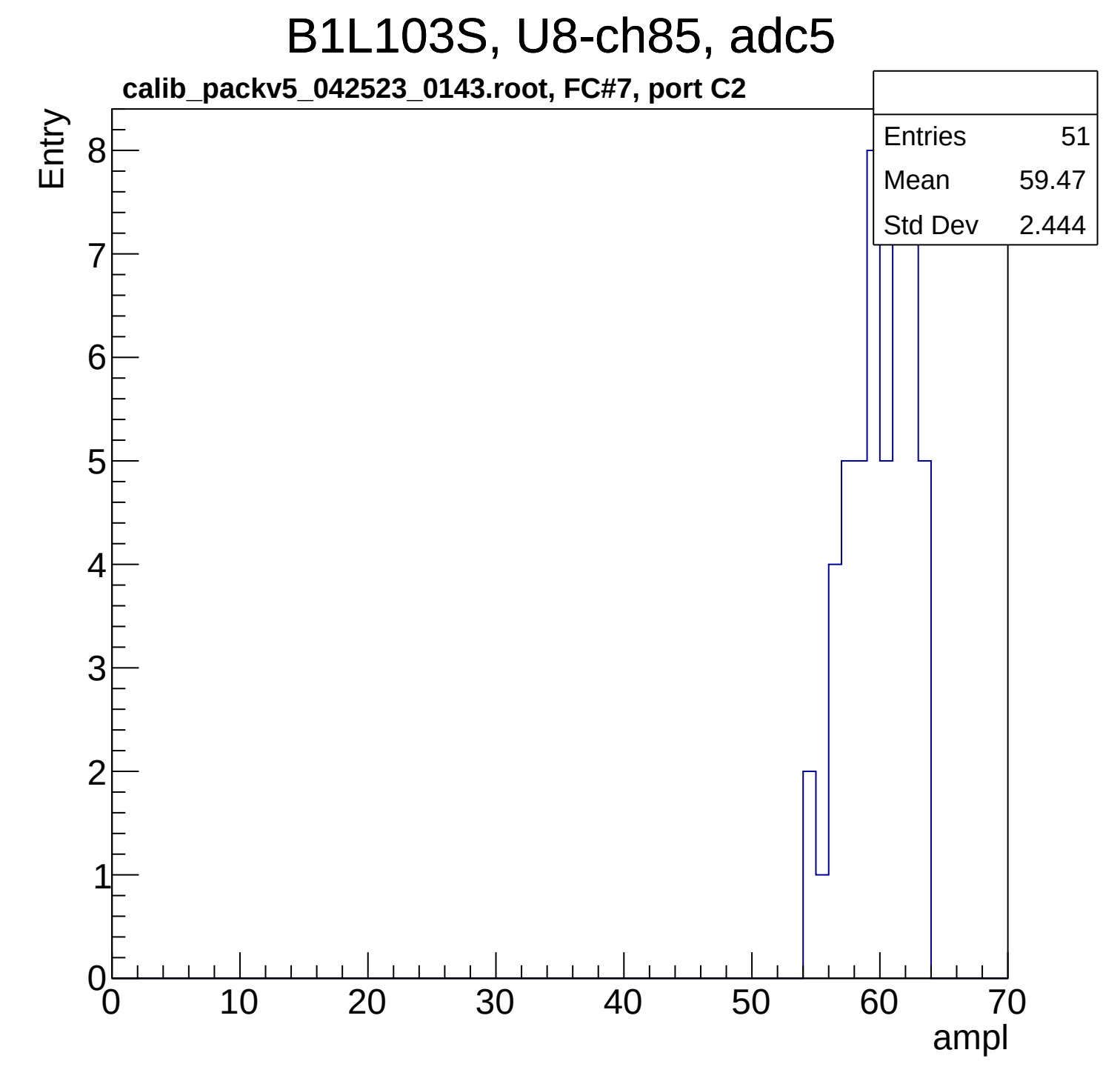

B1L103S, U8-ch85, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 28.9
Std Dev 3.411
Gaus mean : 29.4390
Gaus Width: 3.3857
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

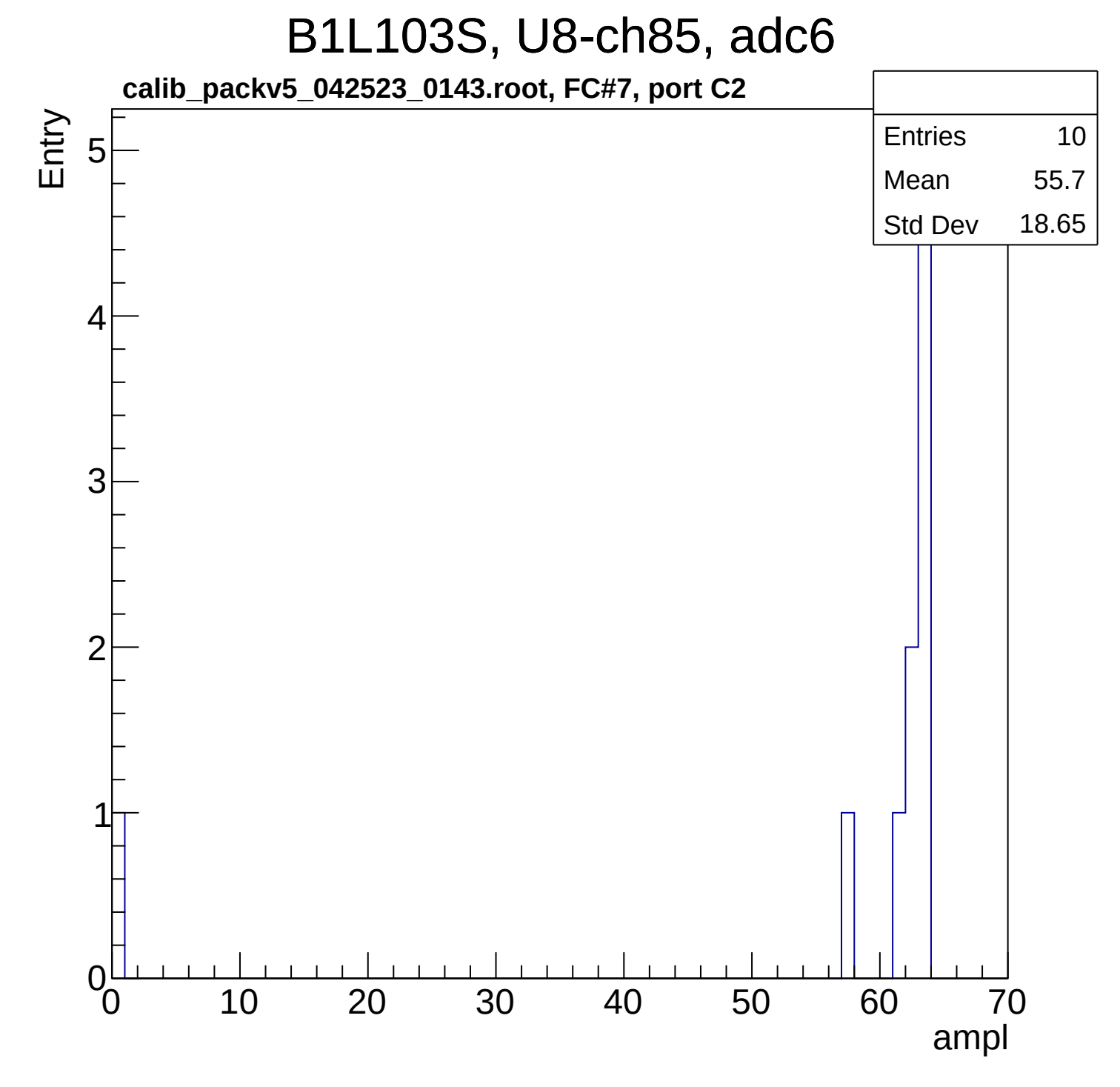

B1L103S, U8-ch85, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 81
Mean 35.96
Std Dev 3.444
Gaus mean : 36.6924
Gaus Width: 3.5875
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

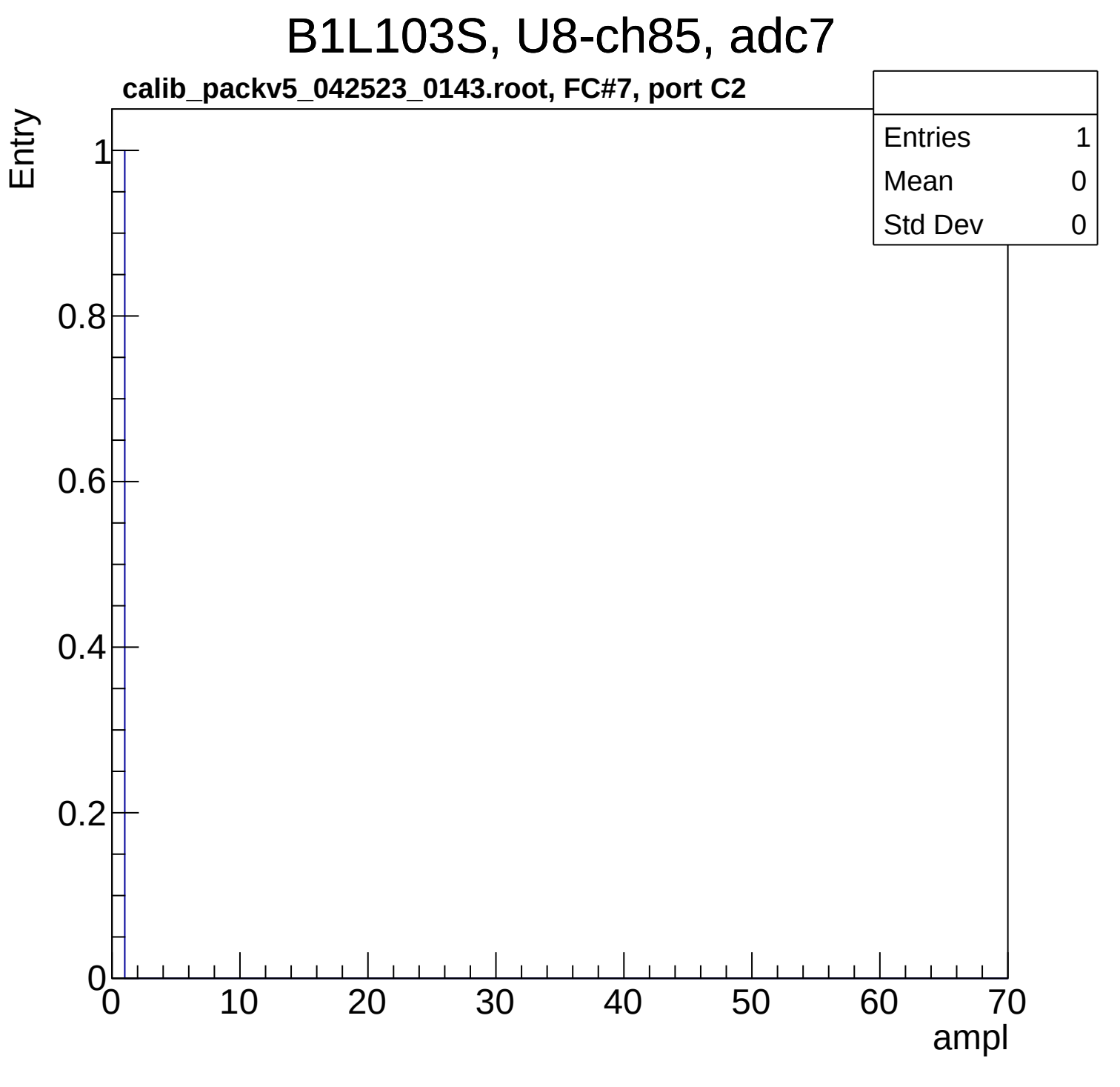

B1L103S, U8-ch85, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 43.66
Std Dev 3.44
Gaus mean : 43.6677
Gaus Width: 3.4540
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

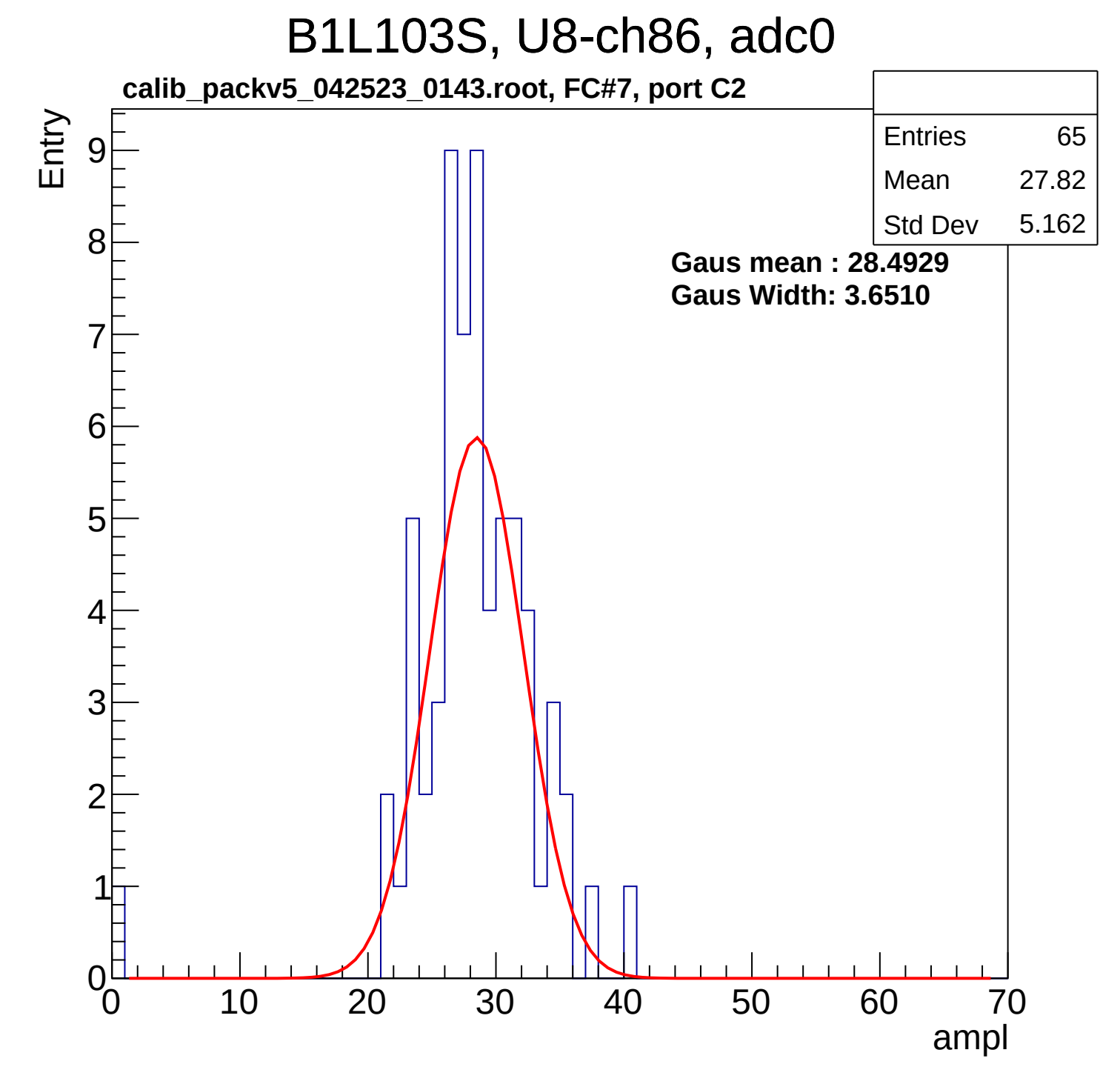

B1L103S, U8-ch85, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 49.36
Std Dev 3.535
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

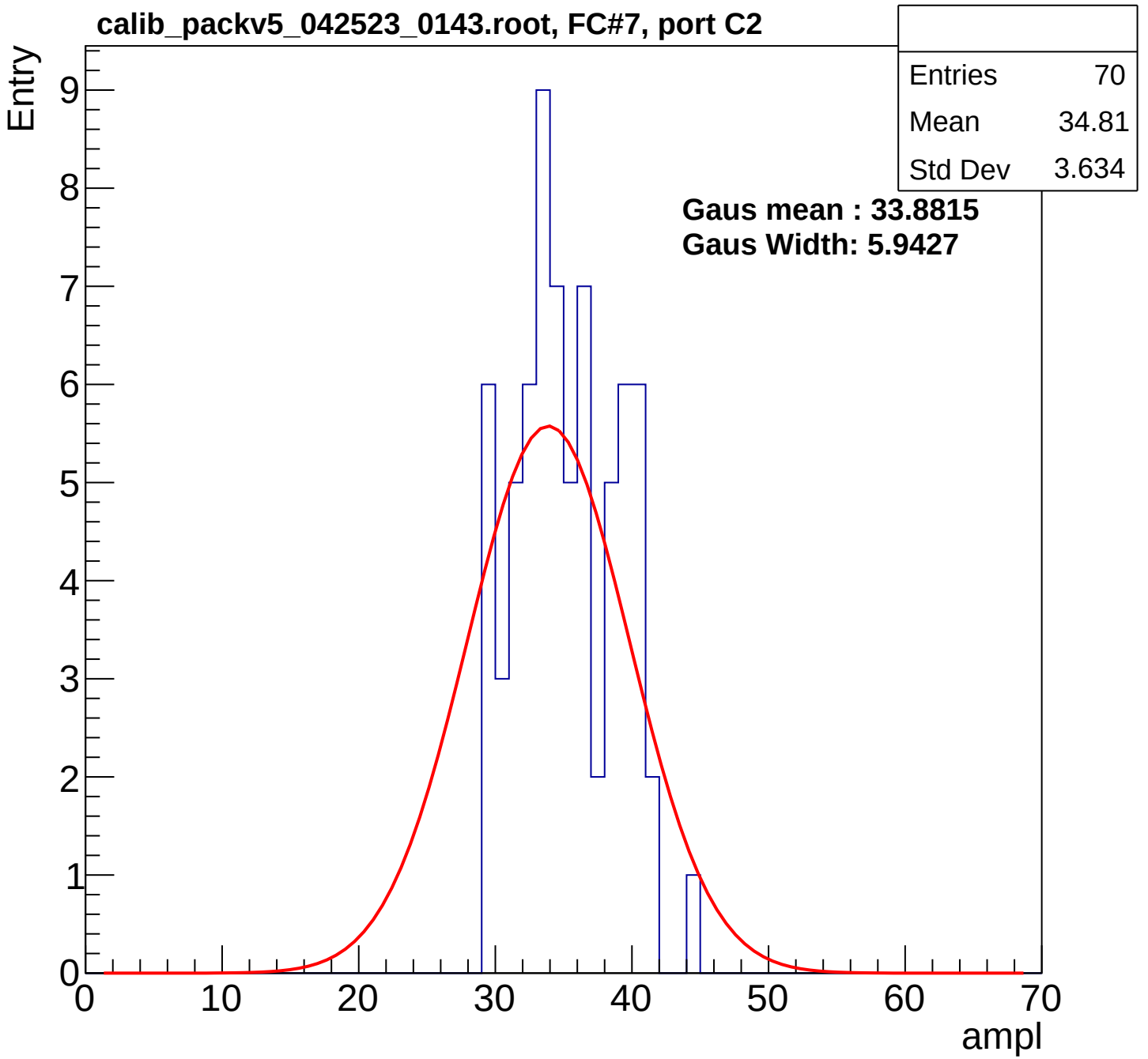

B1L103S, U8-ch85, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 54.71
Std Dev 3.414
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

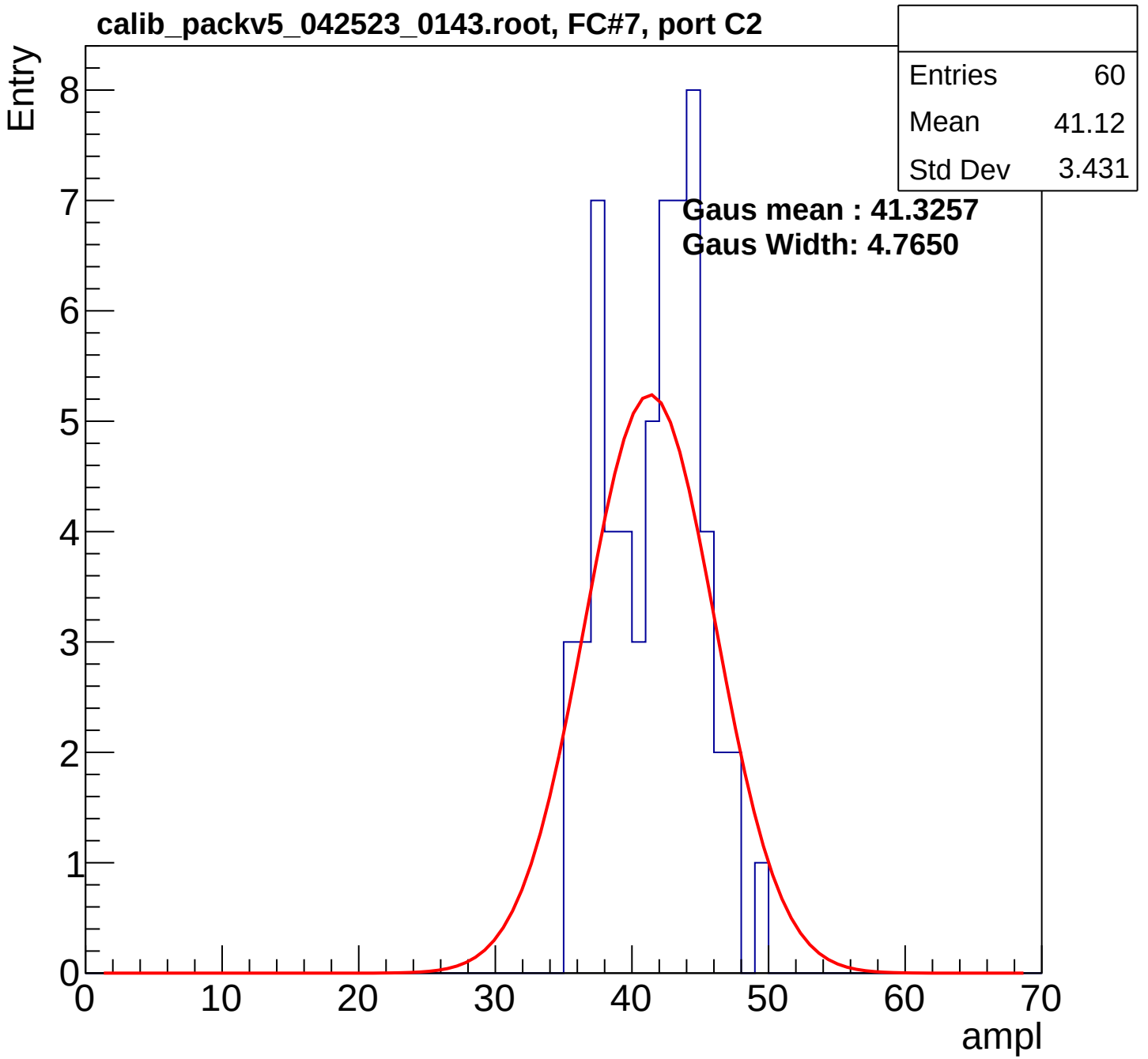

B1L103S, U8-ch85, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 59.47
Std Dev 2.444
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

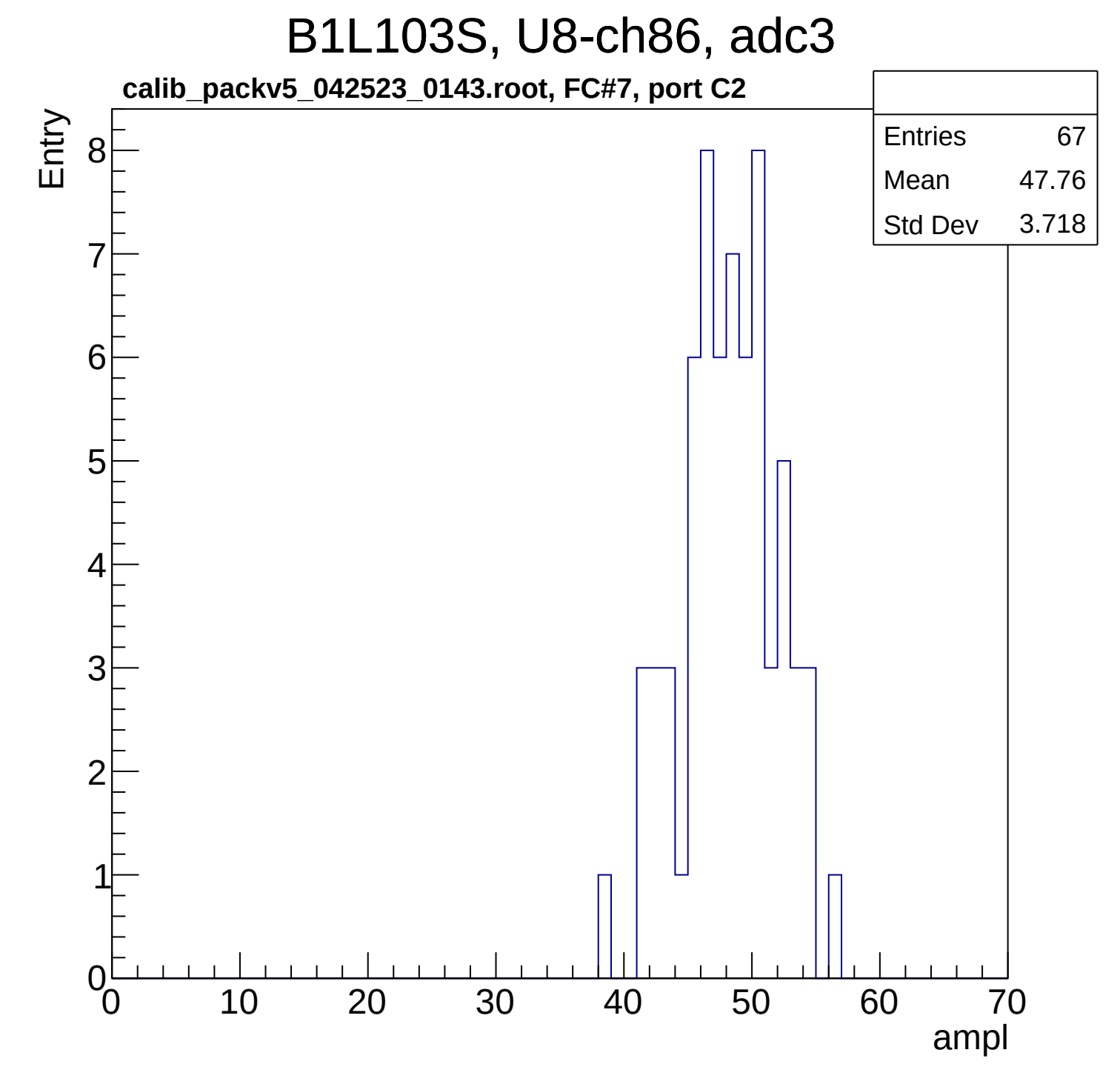

B1L103S, U8-ch85, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 10
Mean 55.7
Std Dev 18.65
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

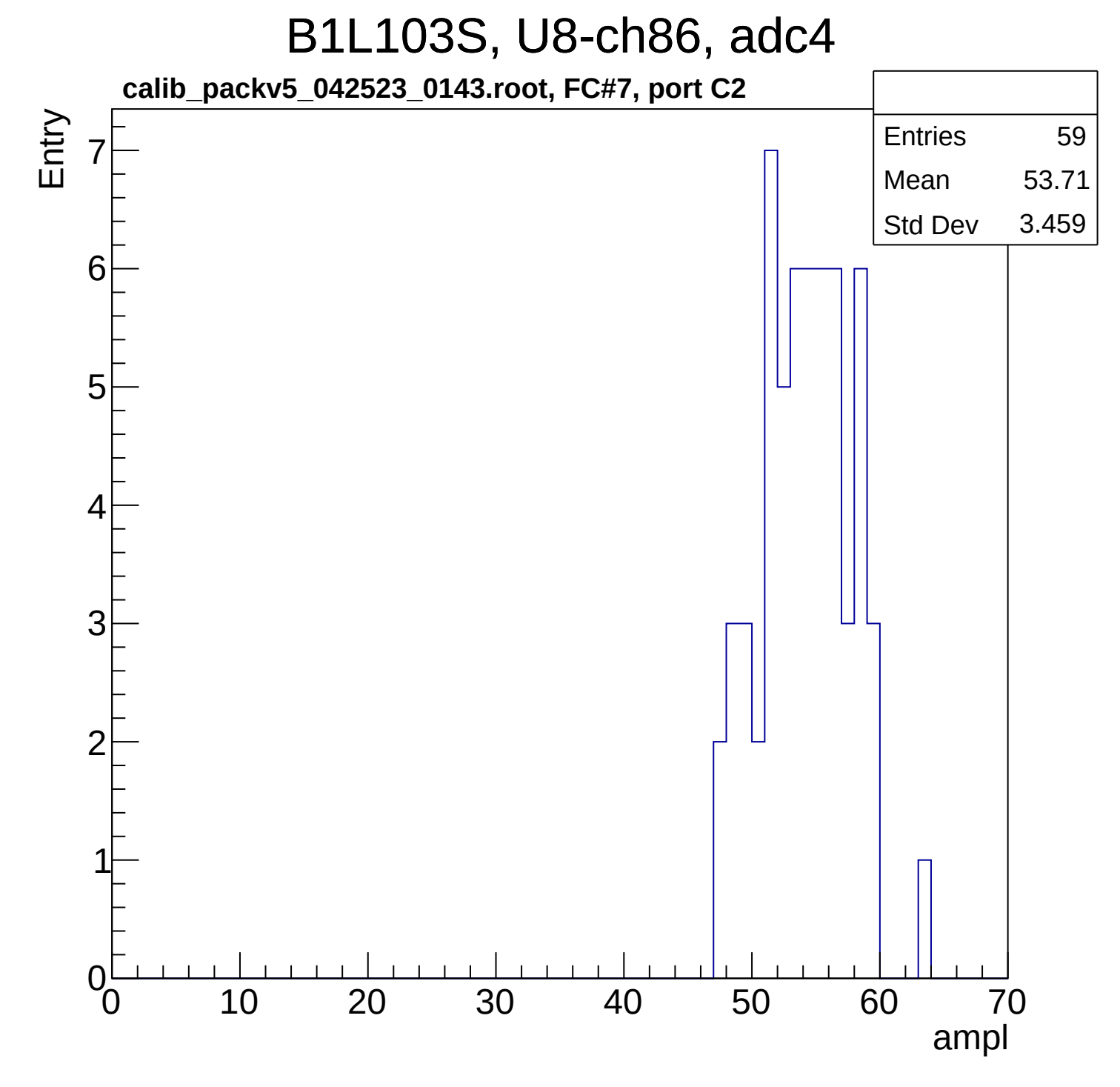

B1L103S, U8-ch85, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

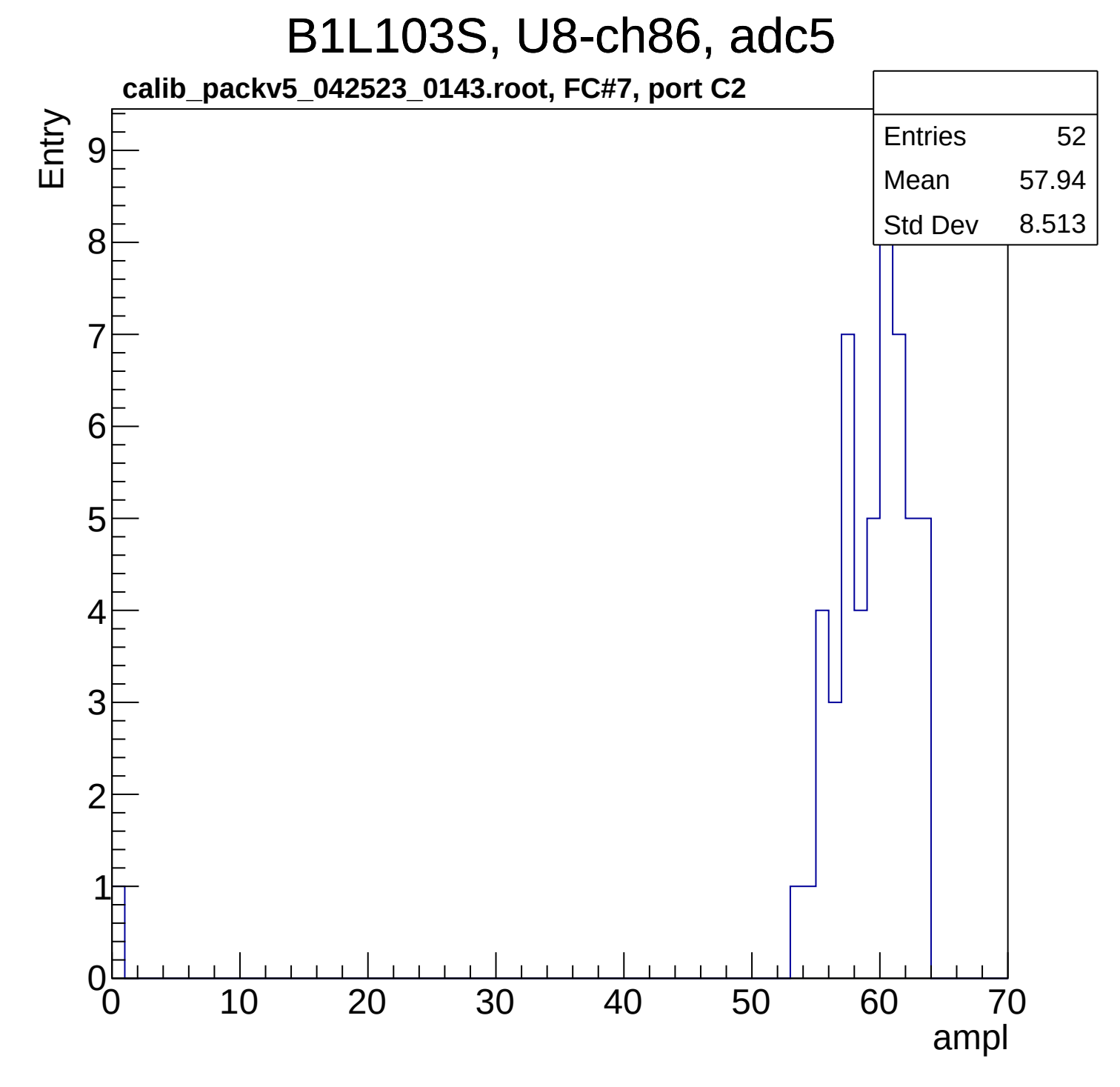

B1L103S, U8-ch86, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 27.82
Std Dev 5.162
Gaus mean : 28.4929
Gaus Width: 3.6510
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

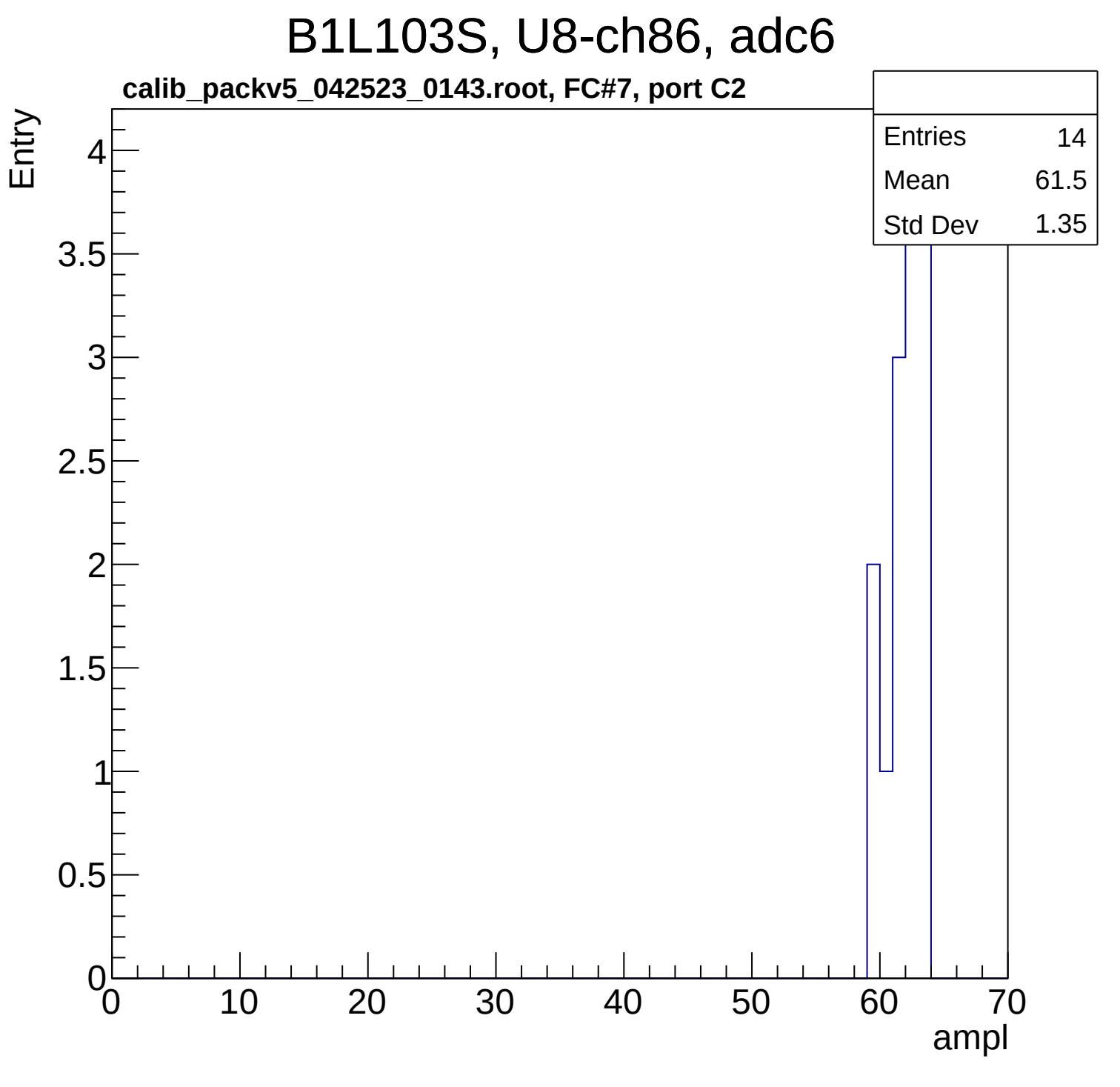

B1L103S, U8-ch86, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 34.81
Std Dev 3.634
Gaus mean : 33.8815
Gaus Width: 5.9427
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

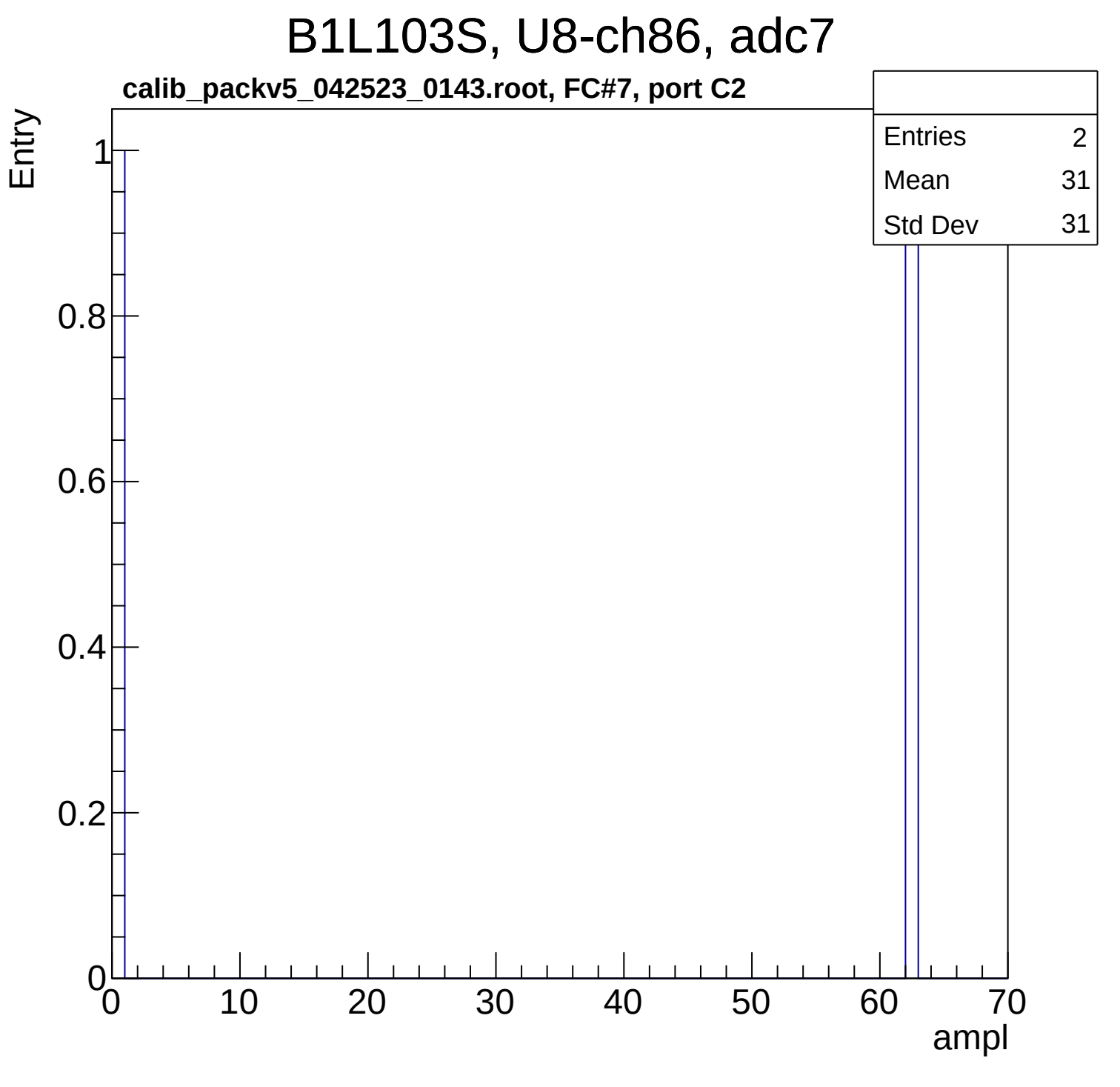

B1L103S, U8-ch86, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 41.12
Std Dev 3.431
Gaus mean : 41.3257
Gaus Width: 4.7650
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

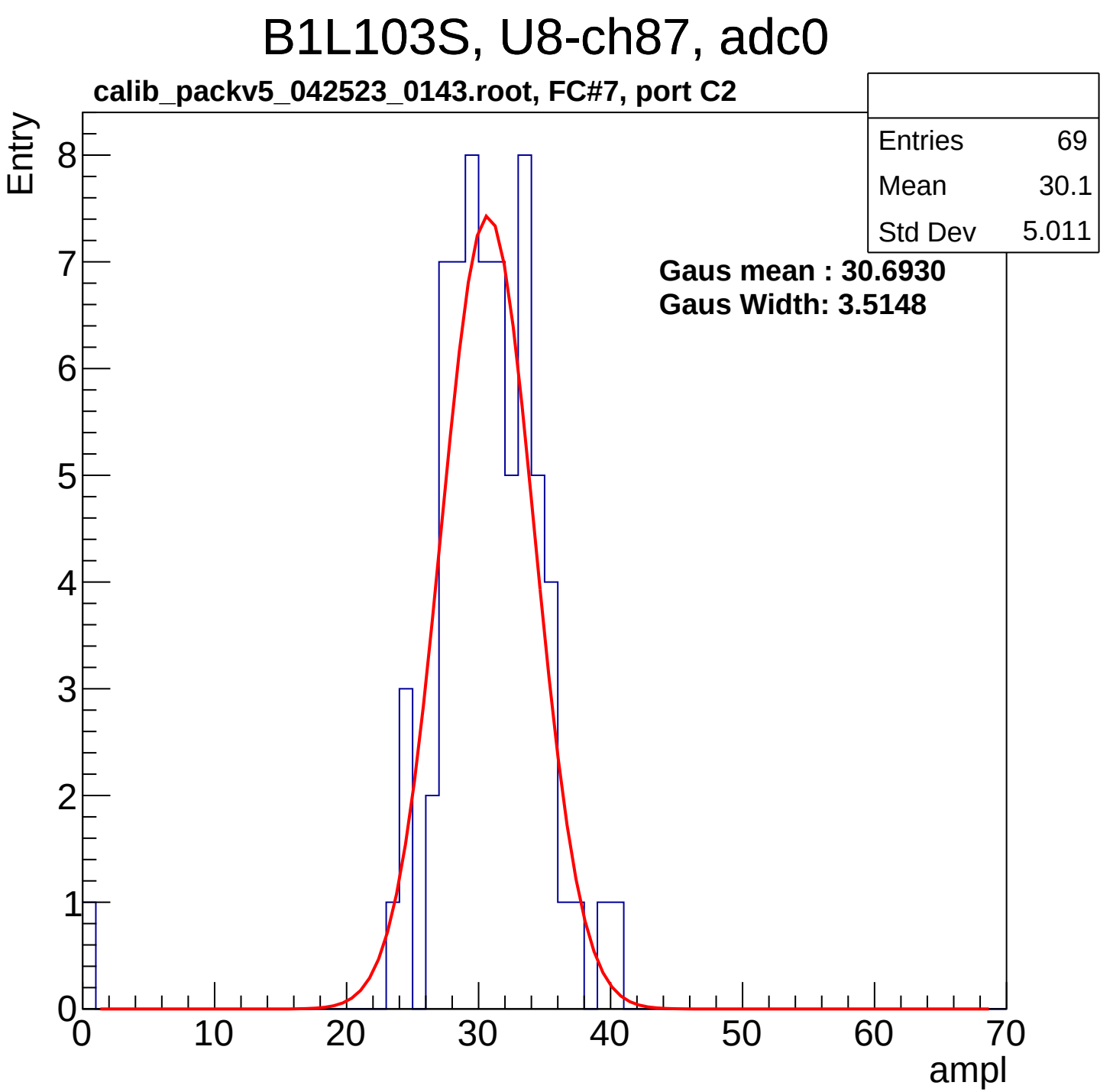

B1L103S, U8-ch86, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 47.76
Std Dev 3.718
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

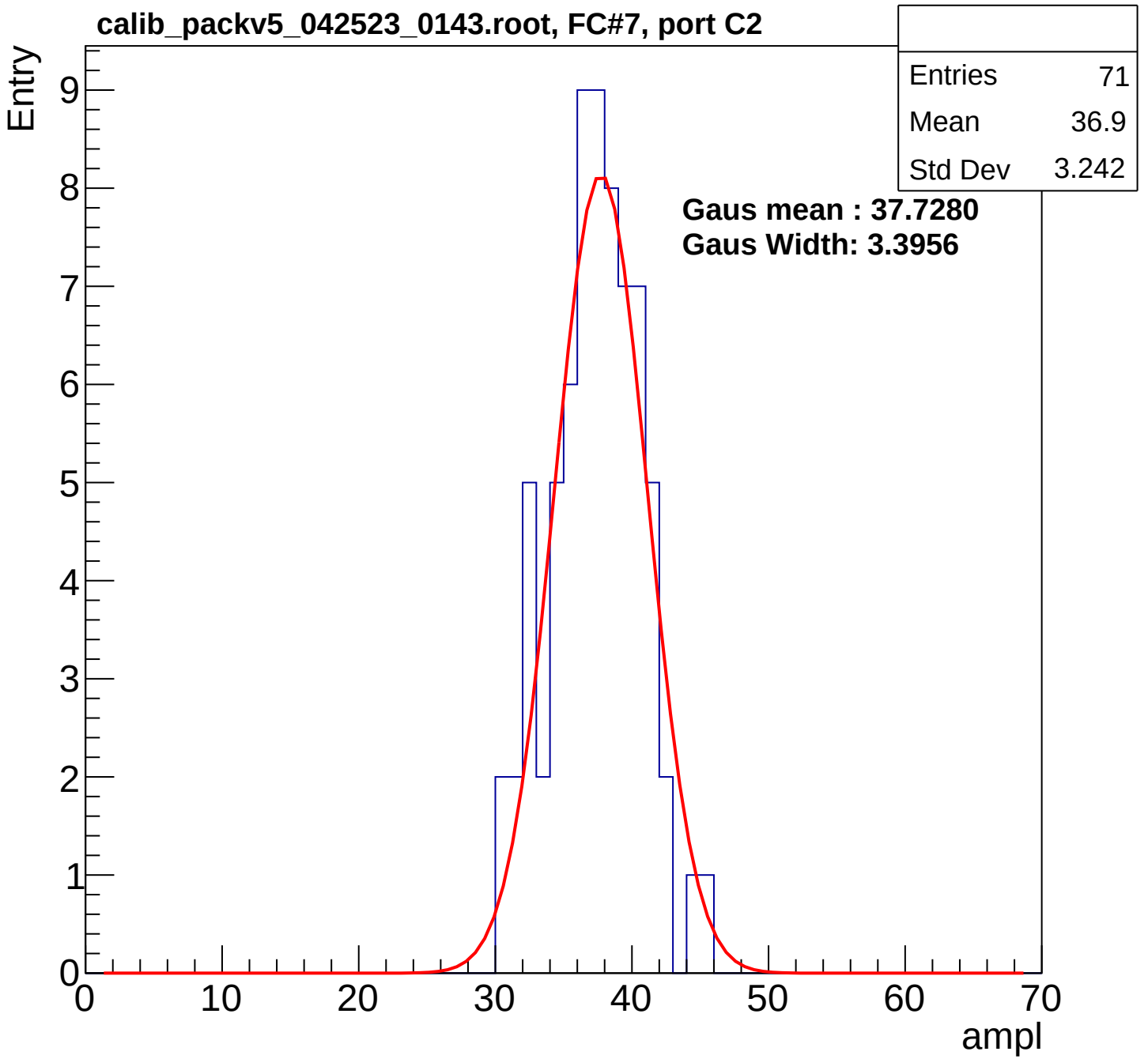

B1L103S, U8-ch86, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 53.71
Std Dev 3.459
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

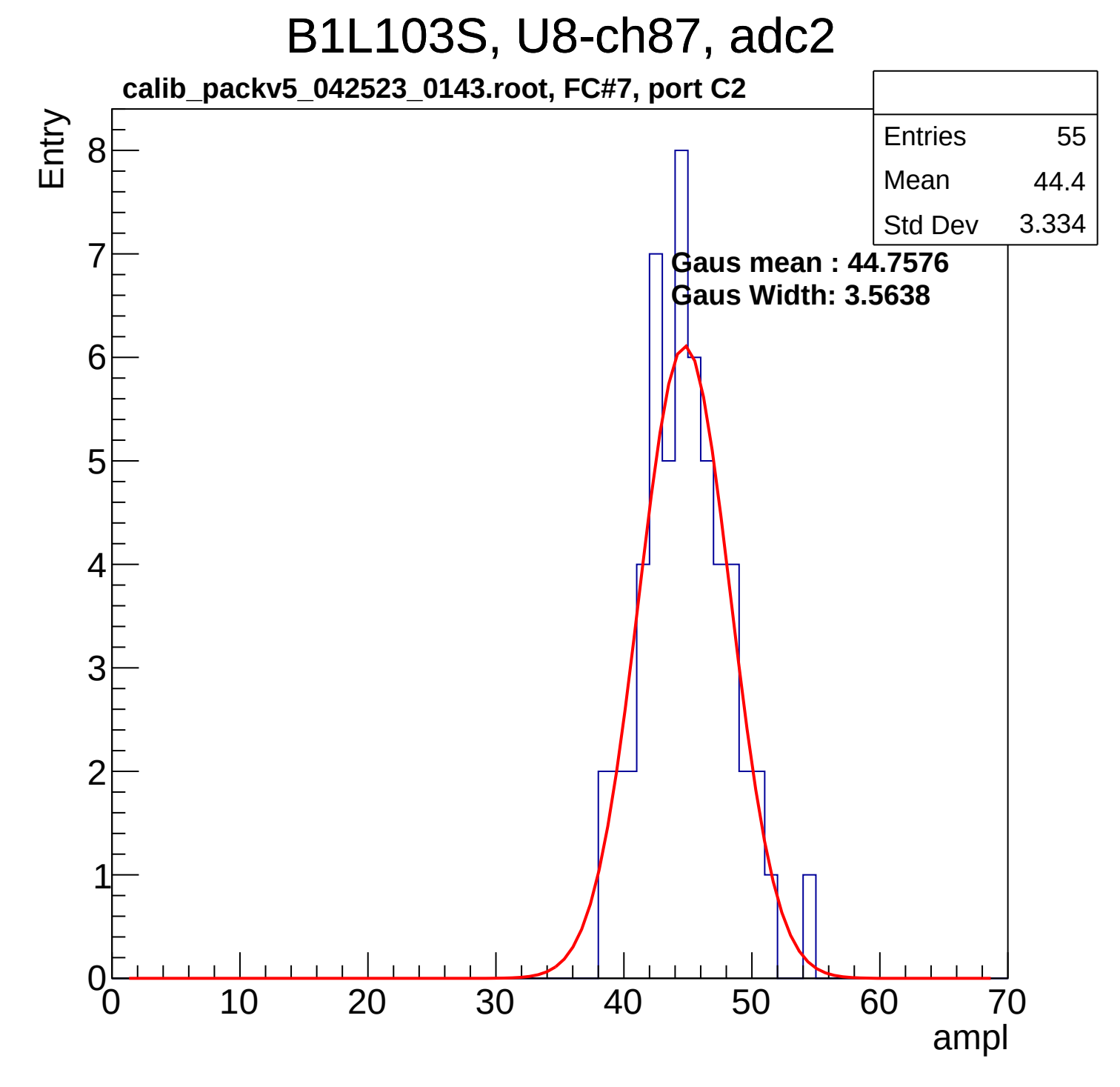

B1L103S, U8-ch86, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 57.94
Std Dev 8.513
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

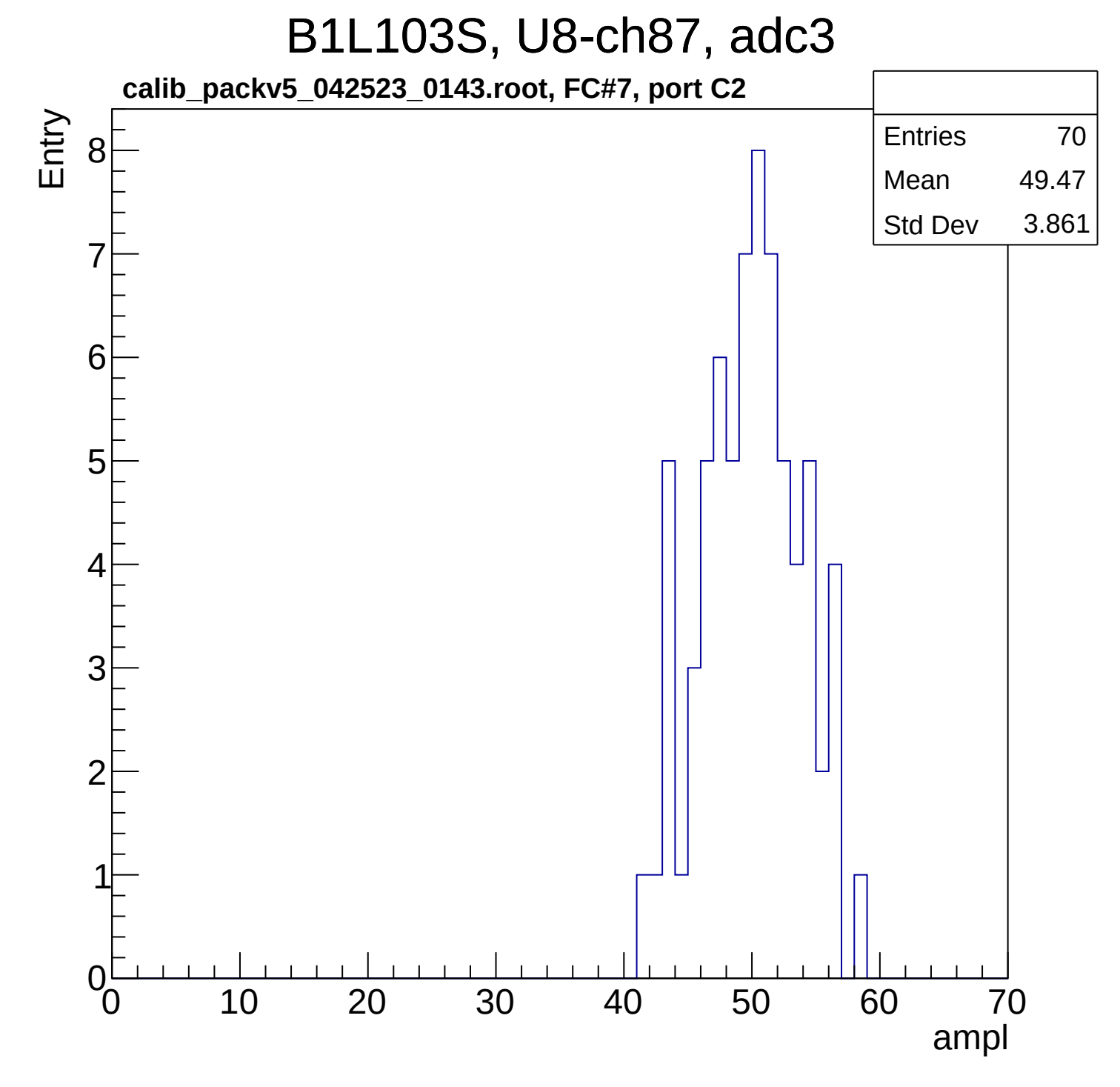

B1L103S, U8-ch86, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 14
Mean 61.5
Std Dev 1.35
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

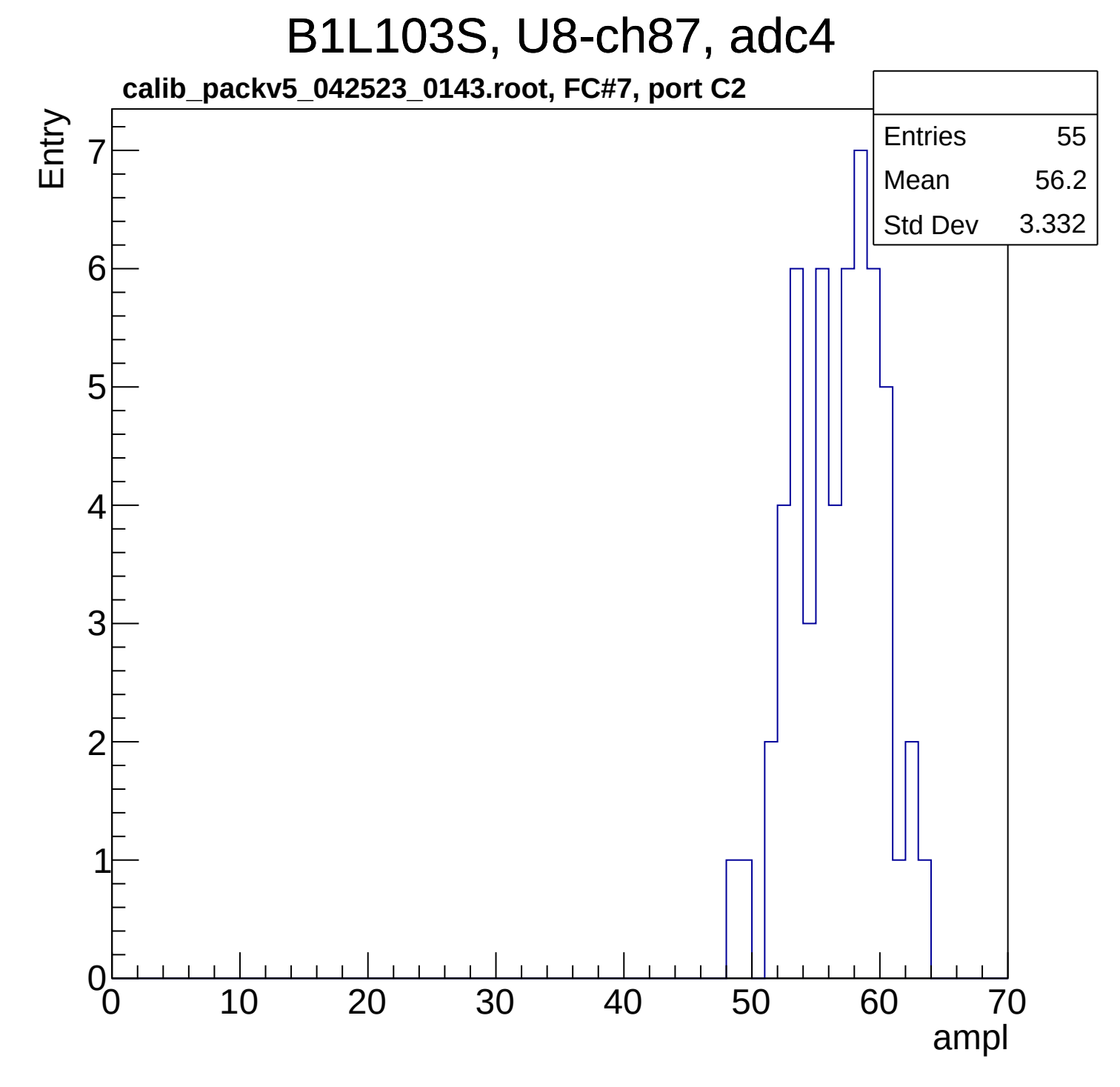

B1L103S, U8-ch86, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 31
Std Dev 31
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

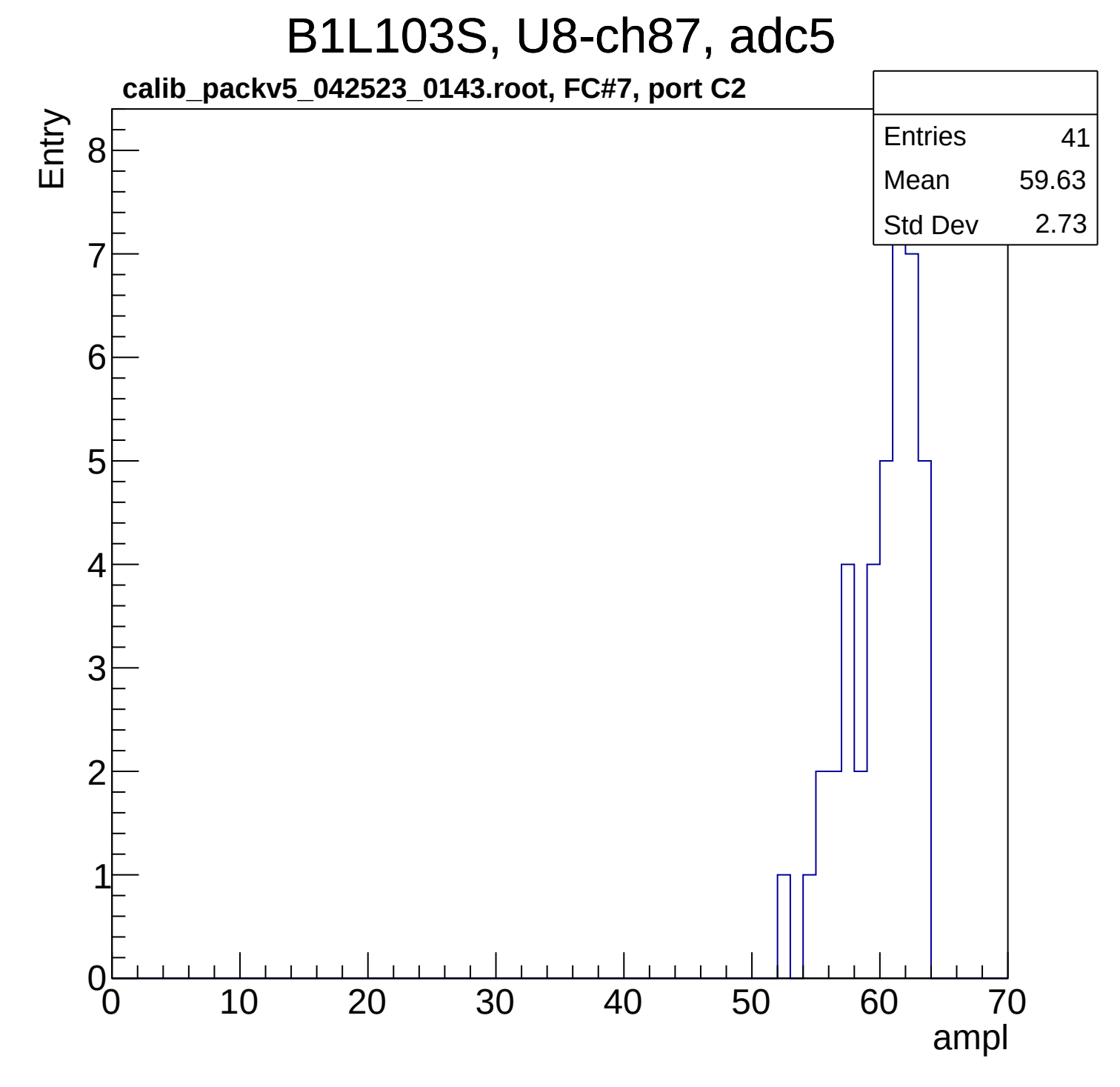

B1L103S, U8-ch87, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 30.1
Std Dev 5.011
Gaus mean : 30.6930
Gaus Width: 3.5148
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

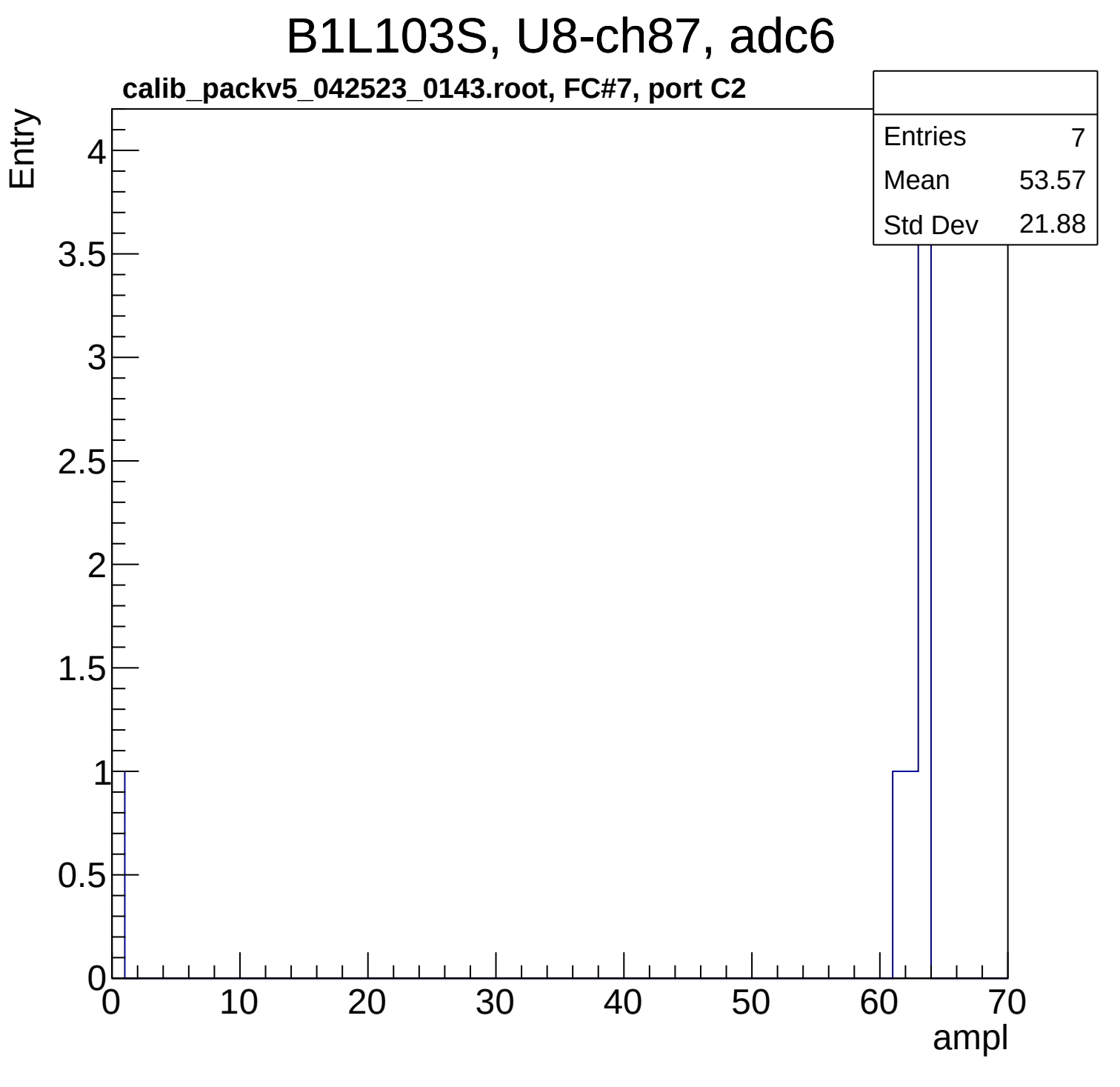

B1L103S, U8-ch87, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 36.9
Std Dev 3.242
Gaus mean : 37.7280
Gaus Width: 3.3956
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

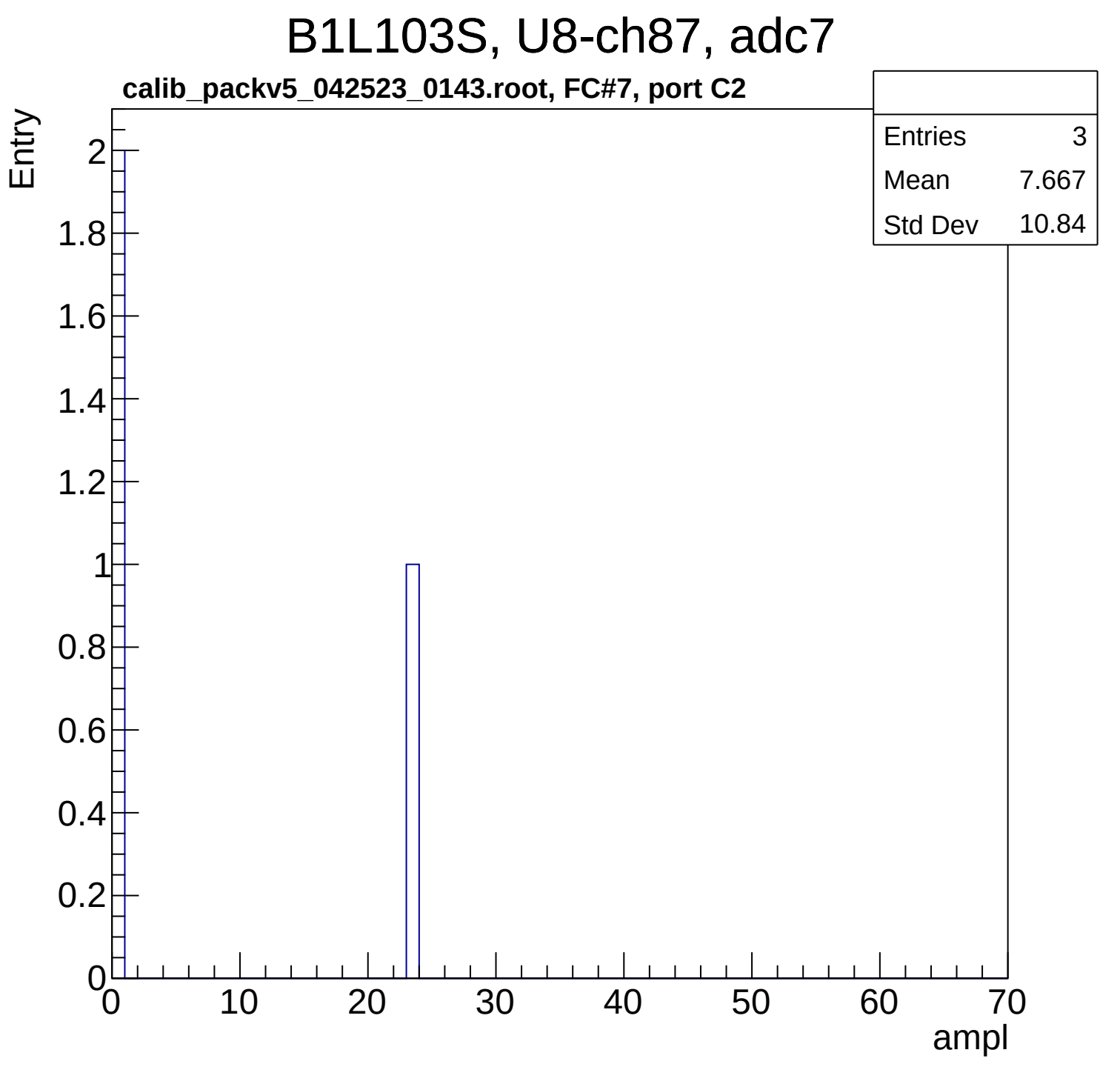

B1L103S, U8-ch87, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 44.4
Std Dev 3.334
Gaus mean : 44.7576
Gaus Width: 3.5638
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

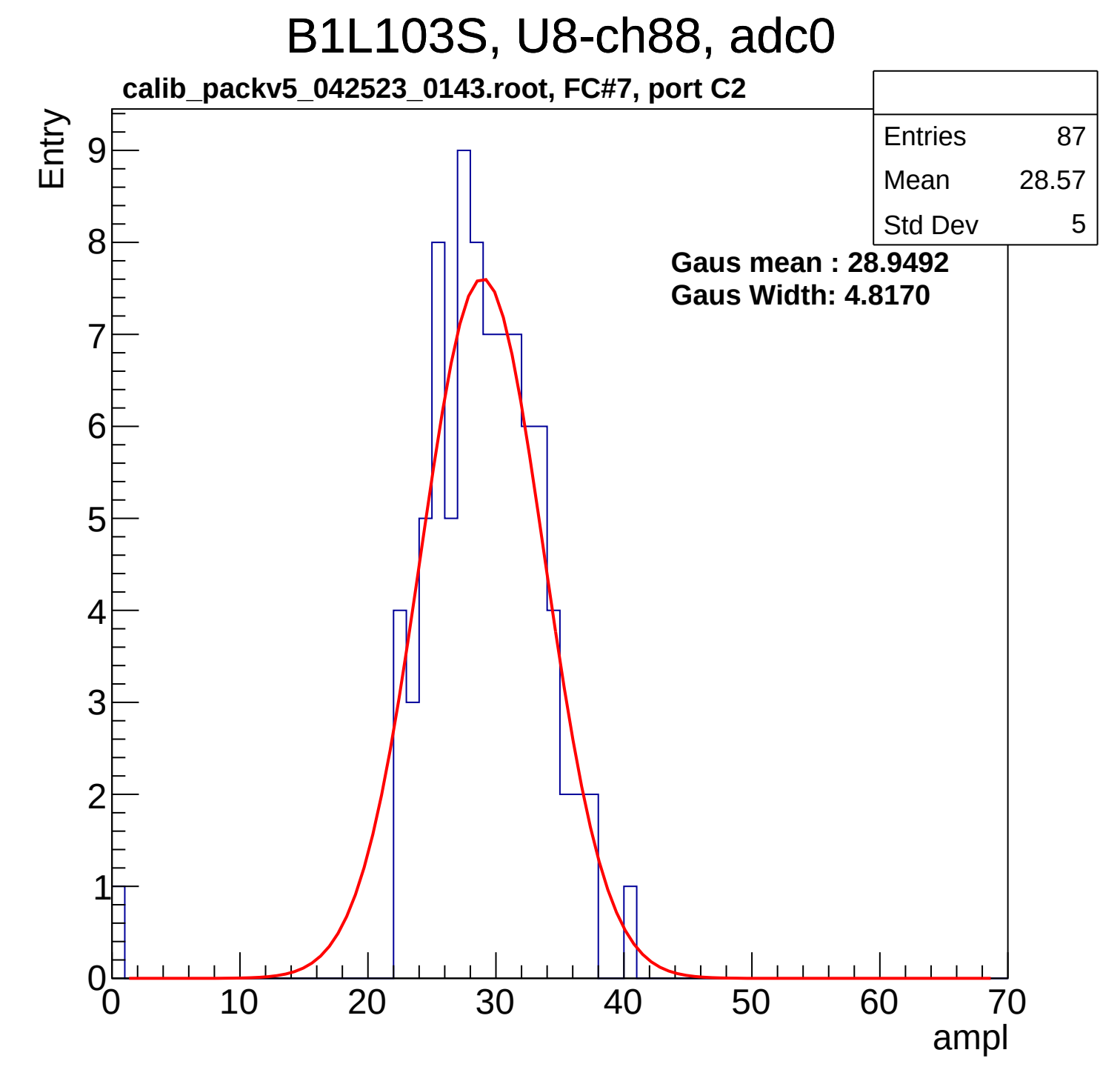

B1L103S, U8-ch87, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 49.47
Std Dev 3.861
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

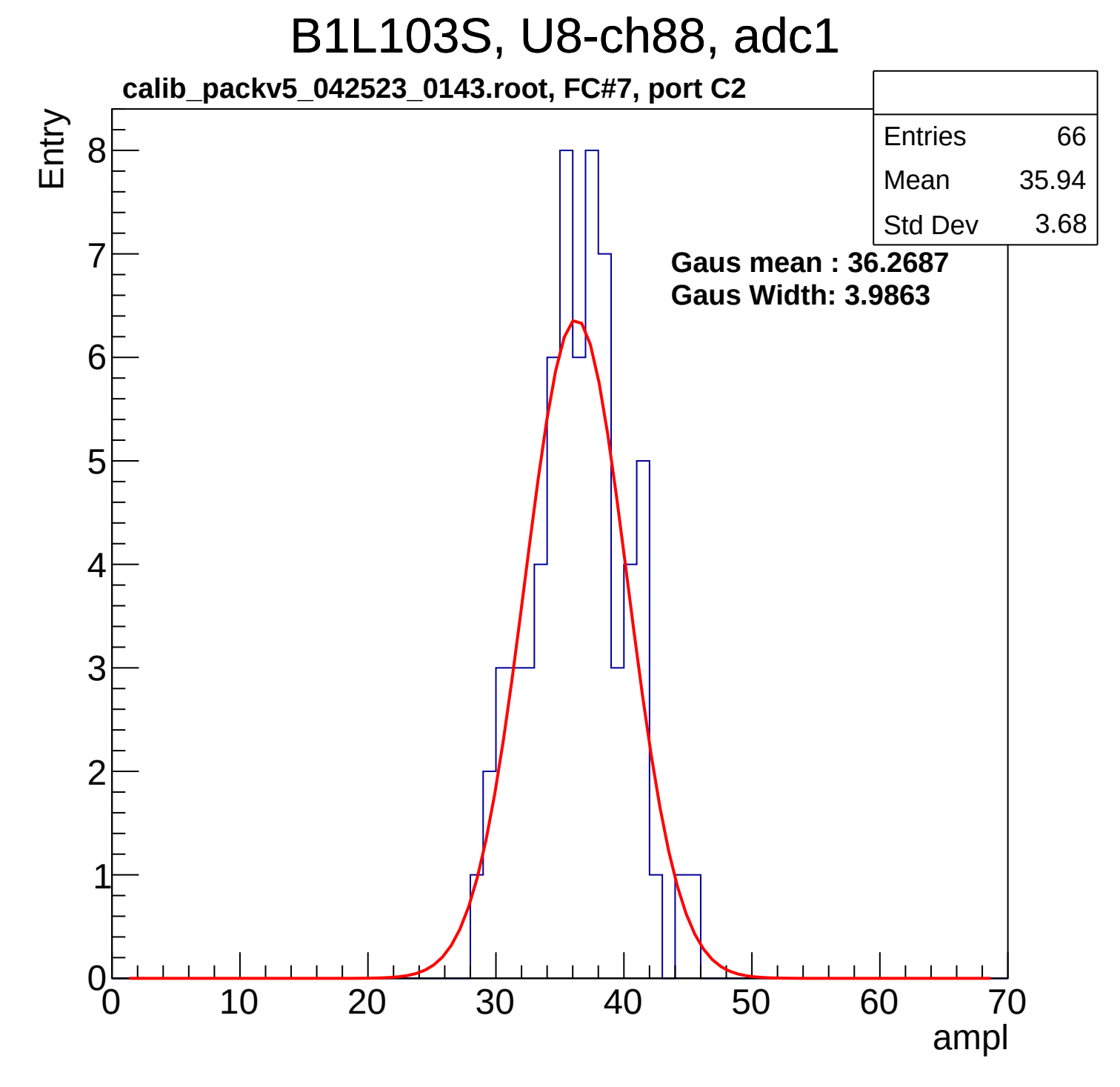

B1L103S, U8-ch87, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 56.2
Std Dev 3.332
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

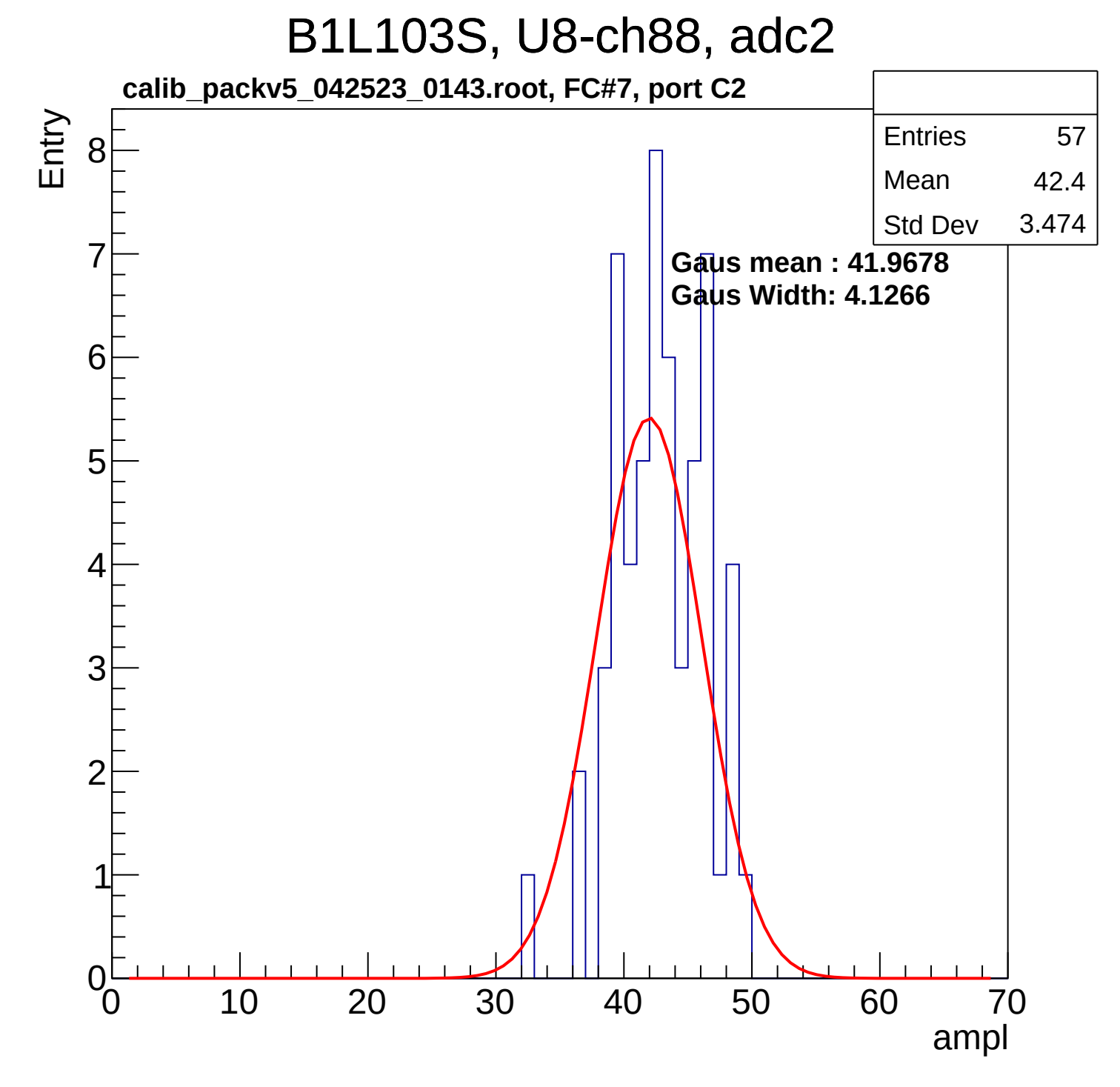

B1L103S, U8-ch87, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 41
Mean 59.63
Std Dev 2.73
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

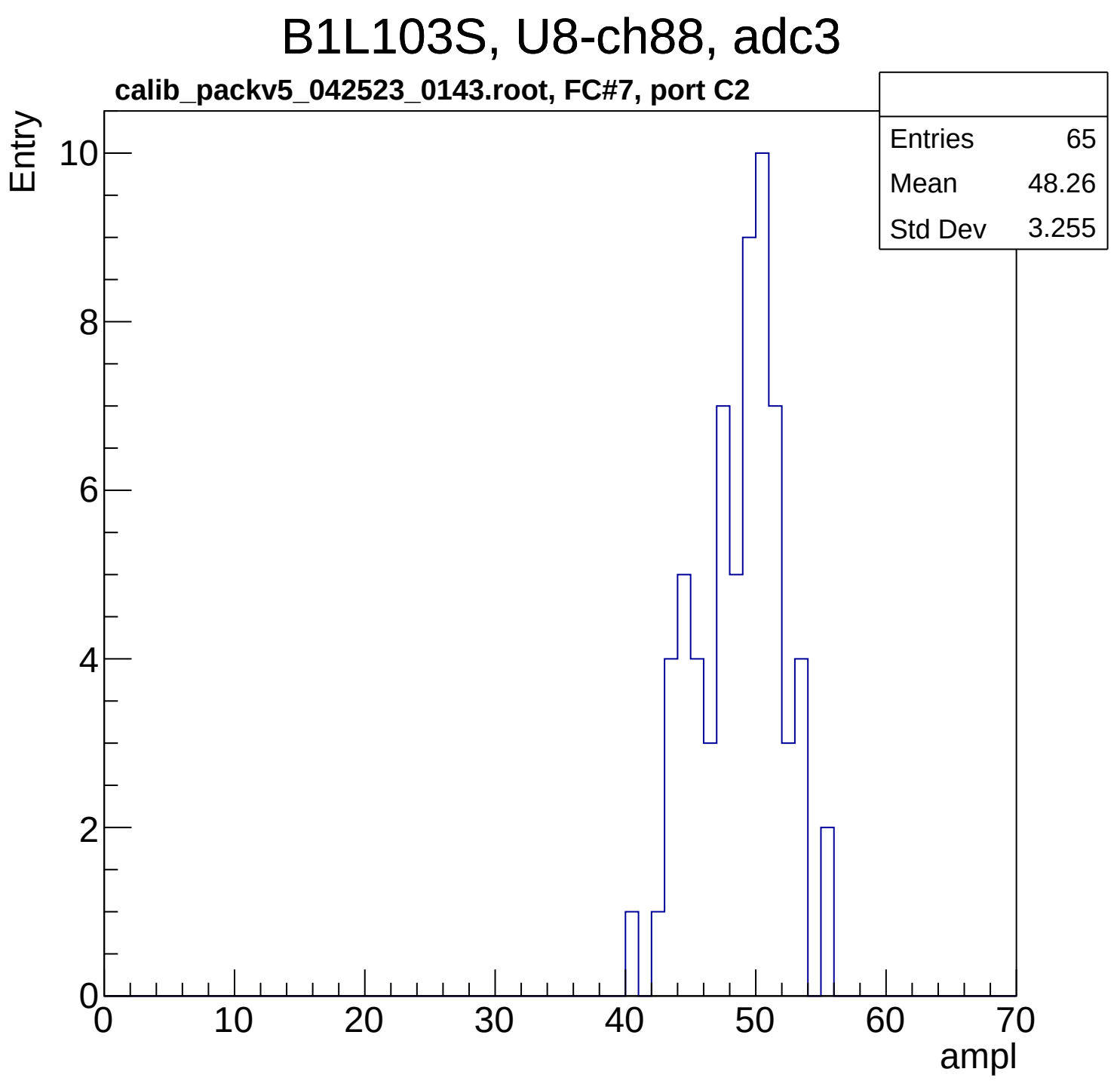

B1L103S, U8-ch87, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 7
Mean 53.57
Std Dev 21.88
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

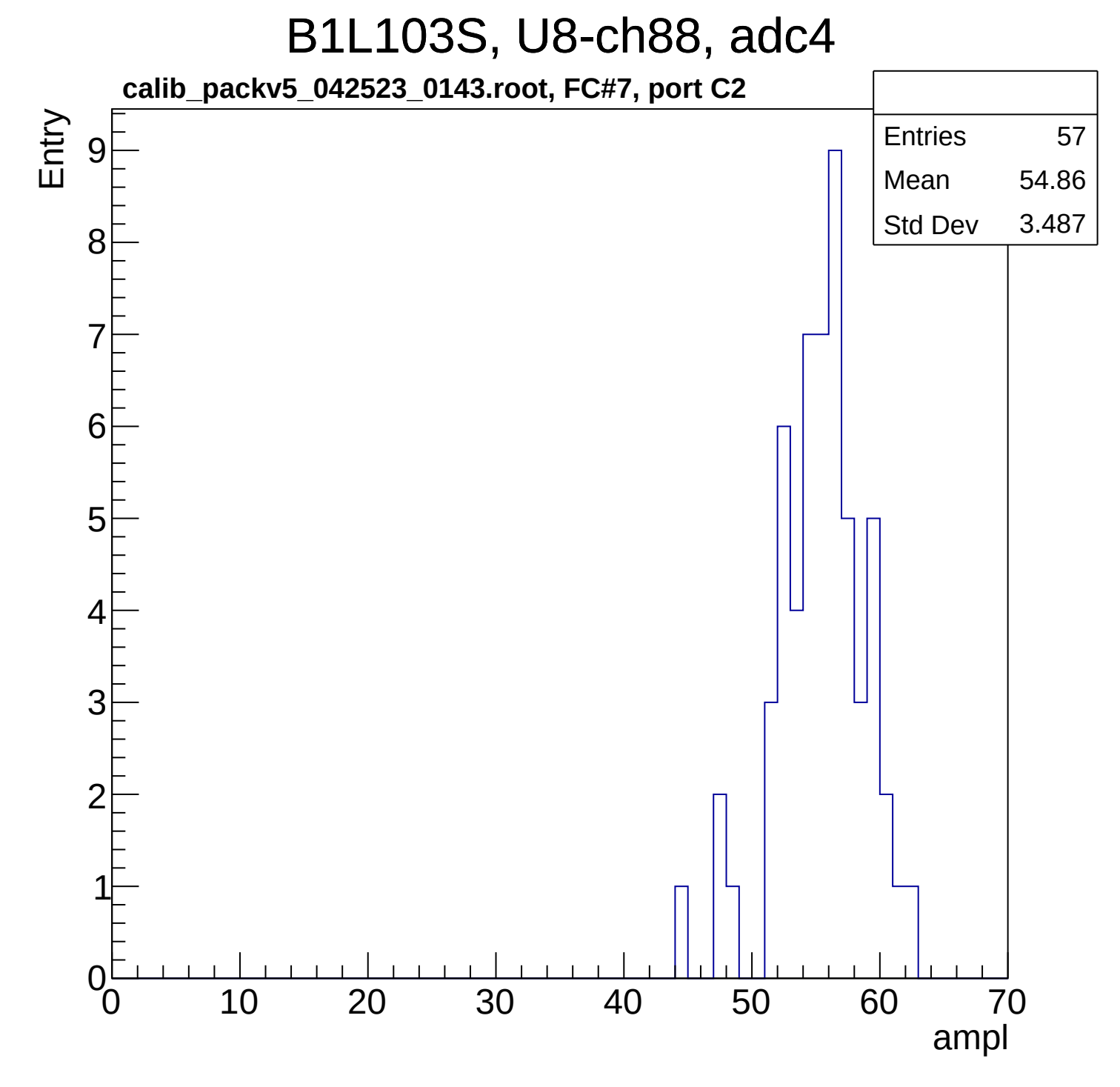

B1L103S, U8-ch87, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 7.667
Std Dev 10.84
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

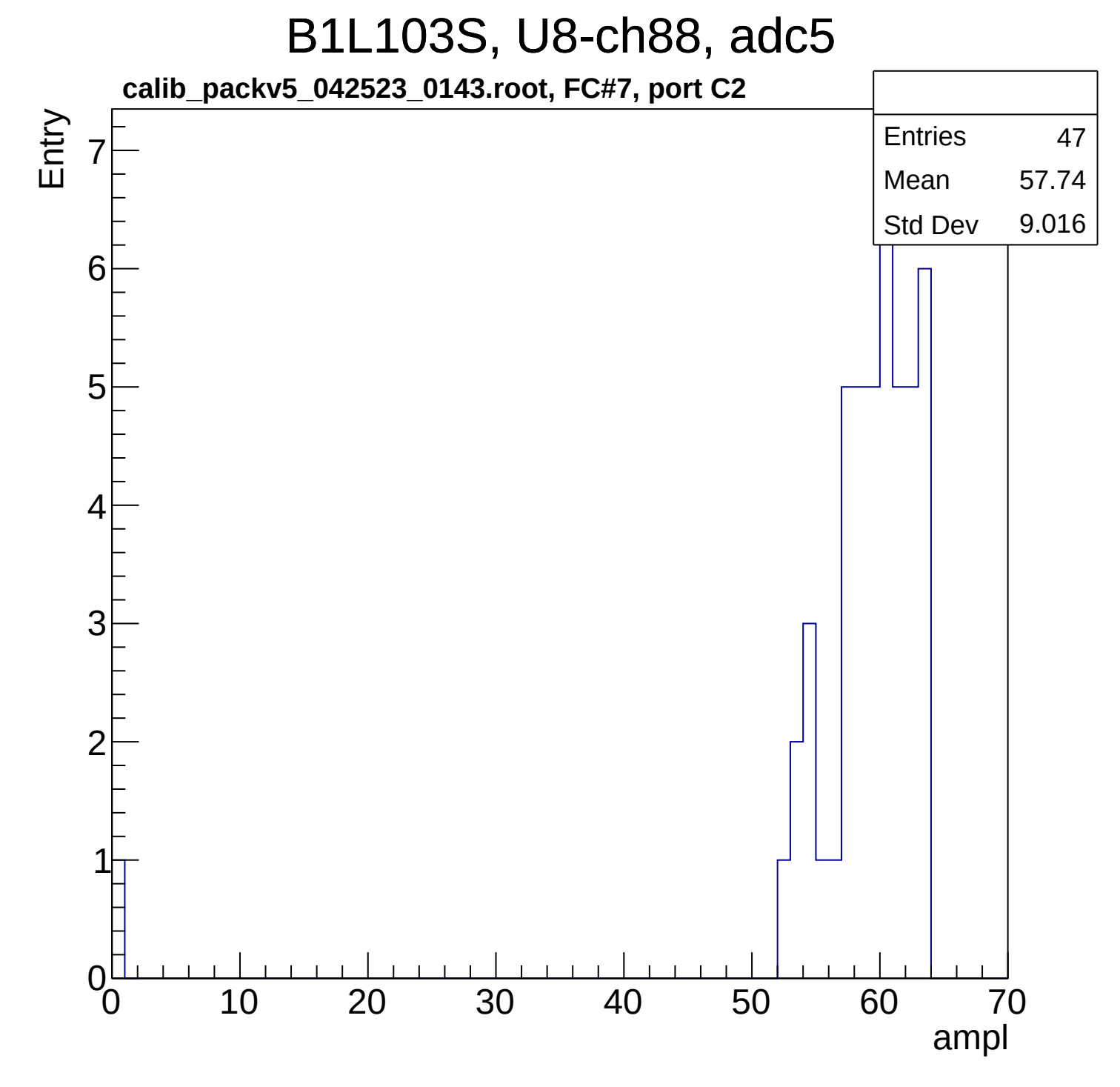

B1L103S, U8-ch88, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 87
Mean 28.57
Std Dev 5
Gaus mean : 28.9492
Gaus Width: 4.8170
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

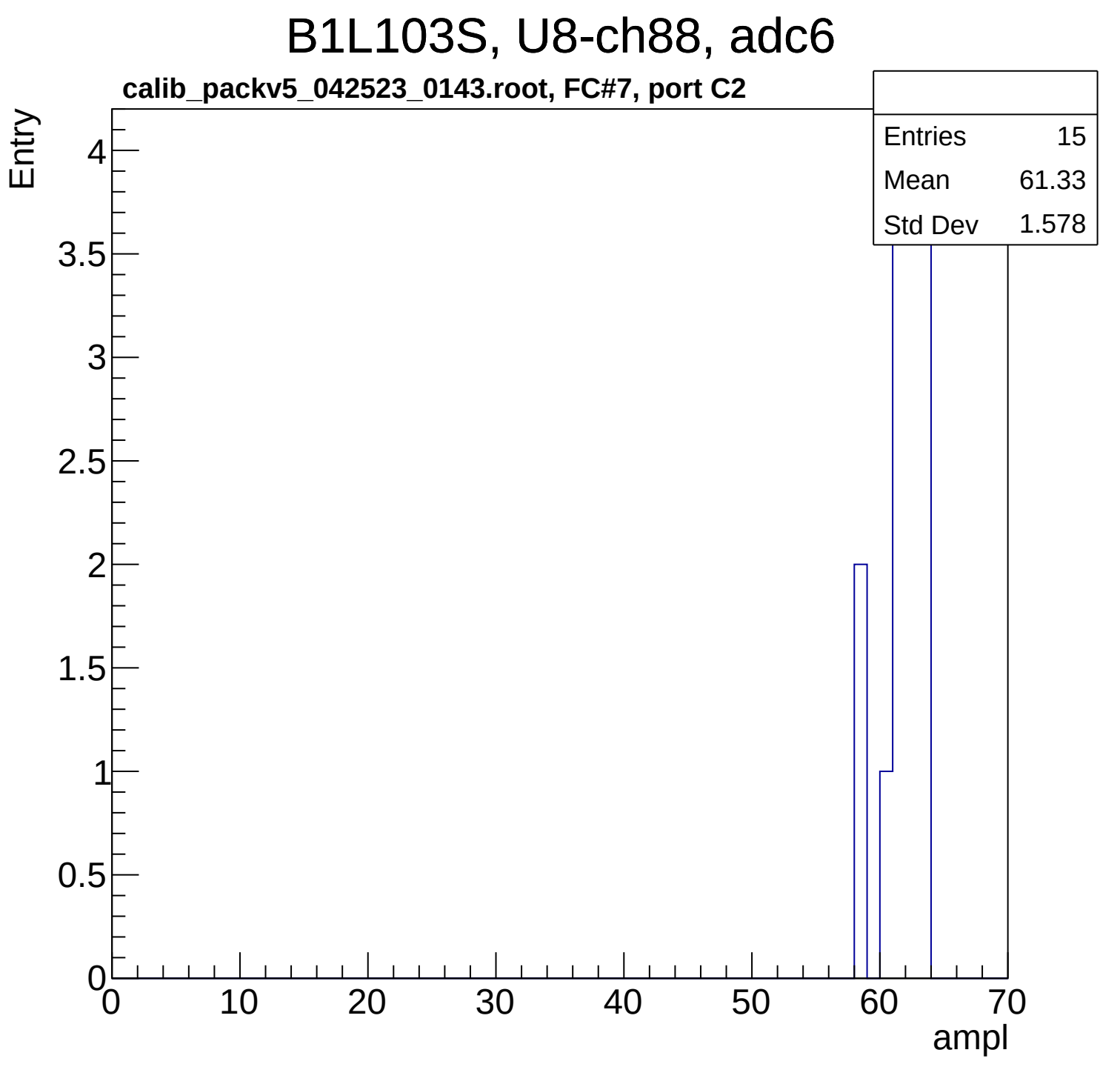

B1L103S, U8-ch88, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 35.94
Std Dev 3.68
Gaus mean : 36.2687
Gaus Width: 3.9863
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

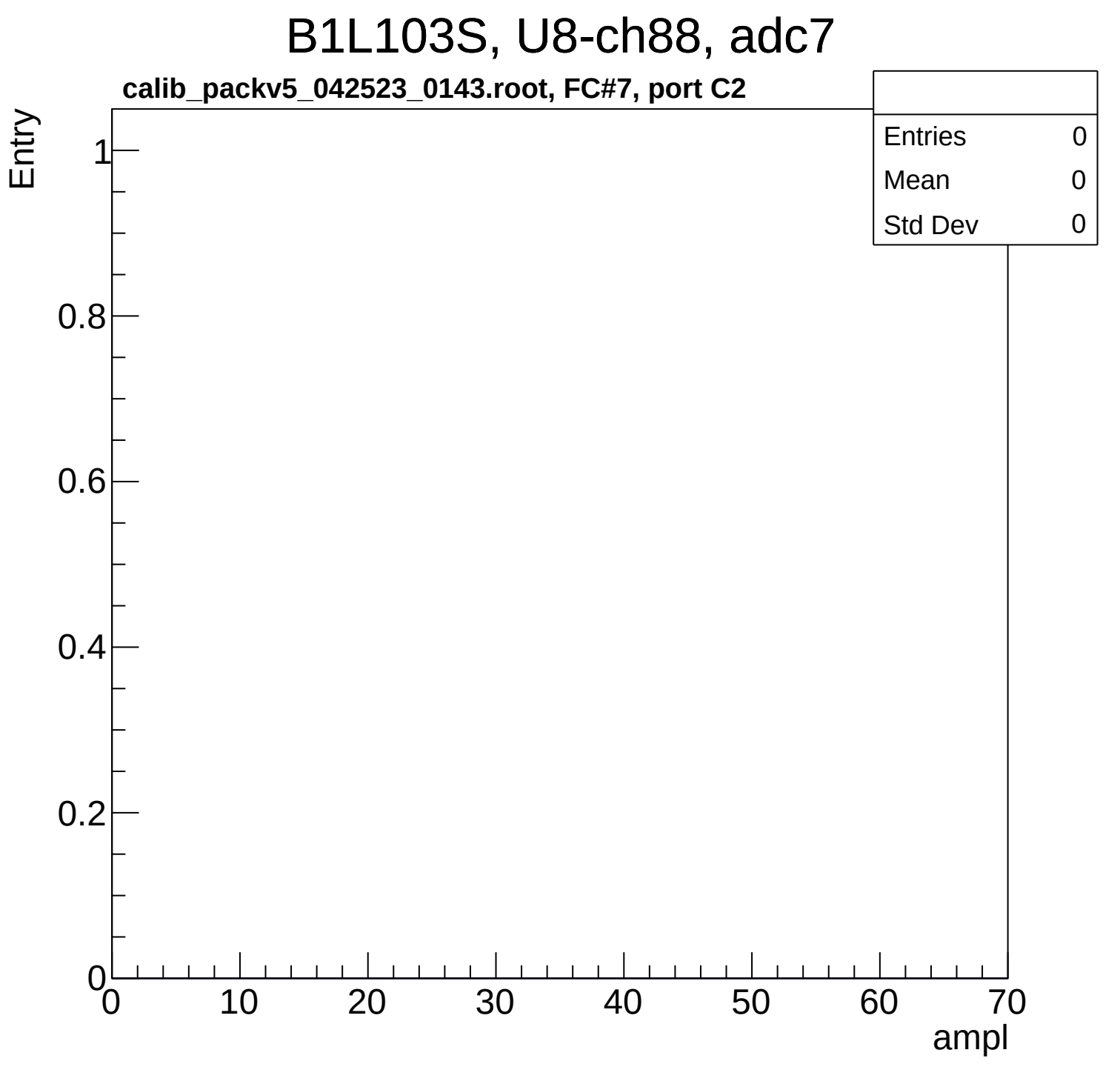

B1L103S, U8-ch88, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 42.4
Std Dev 3.474
Gaus mean : 41.9678
Gaus Width: 4.1266
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

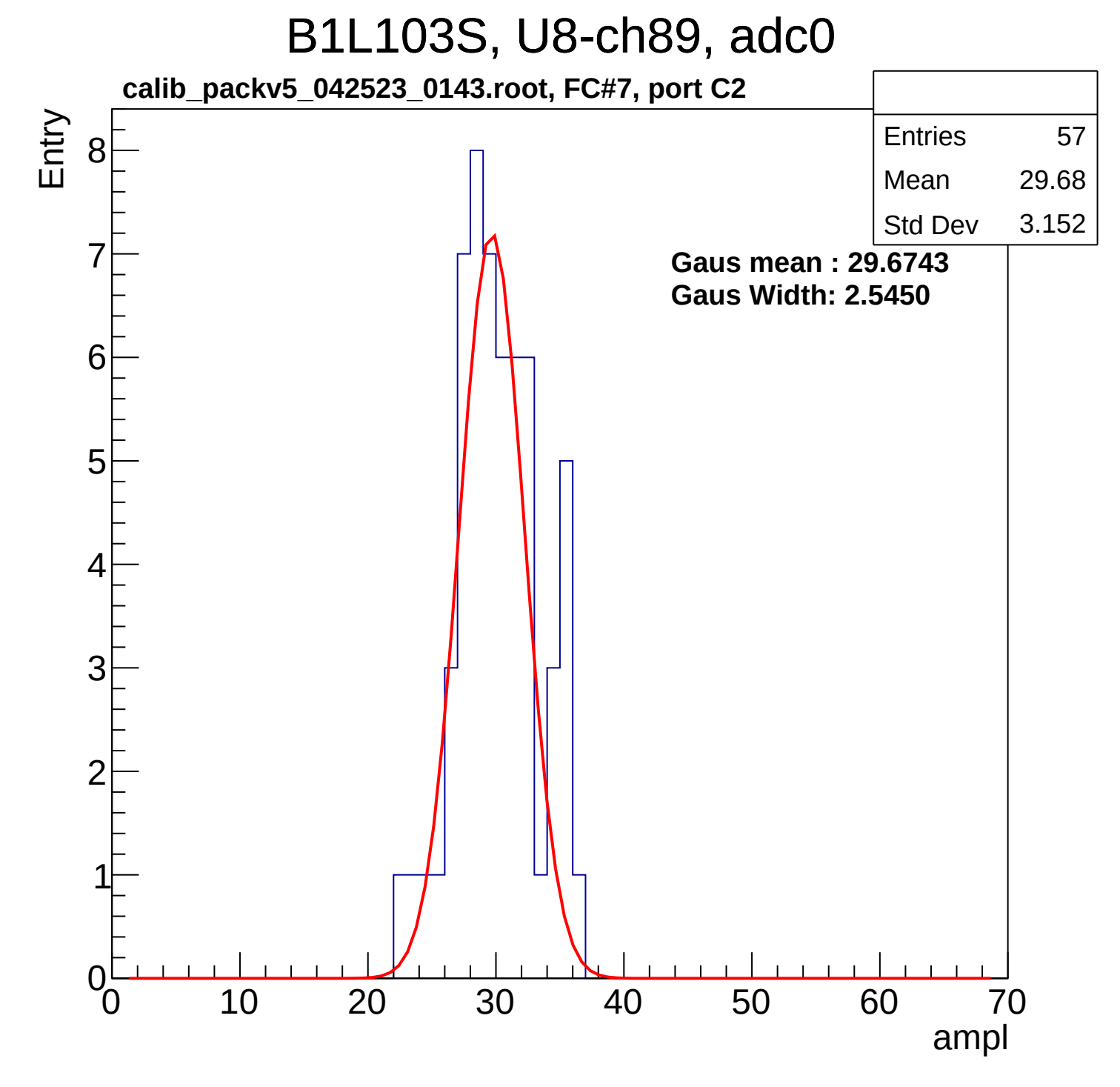

B1L103S, U8-ch88, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 48.26
Std Dev 3.255
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

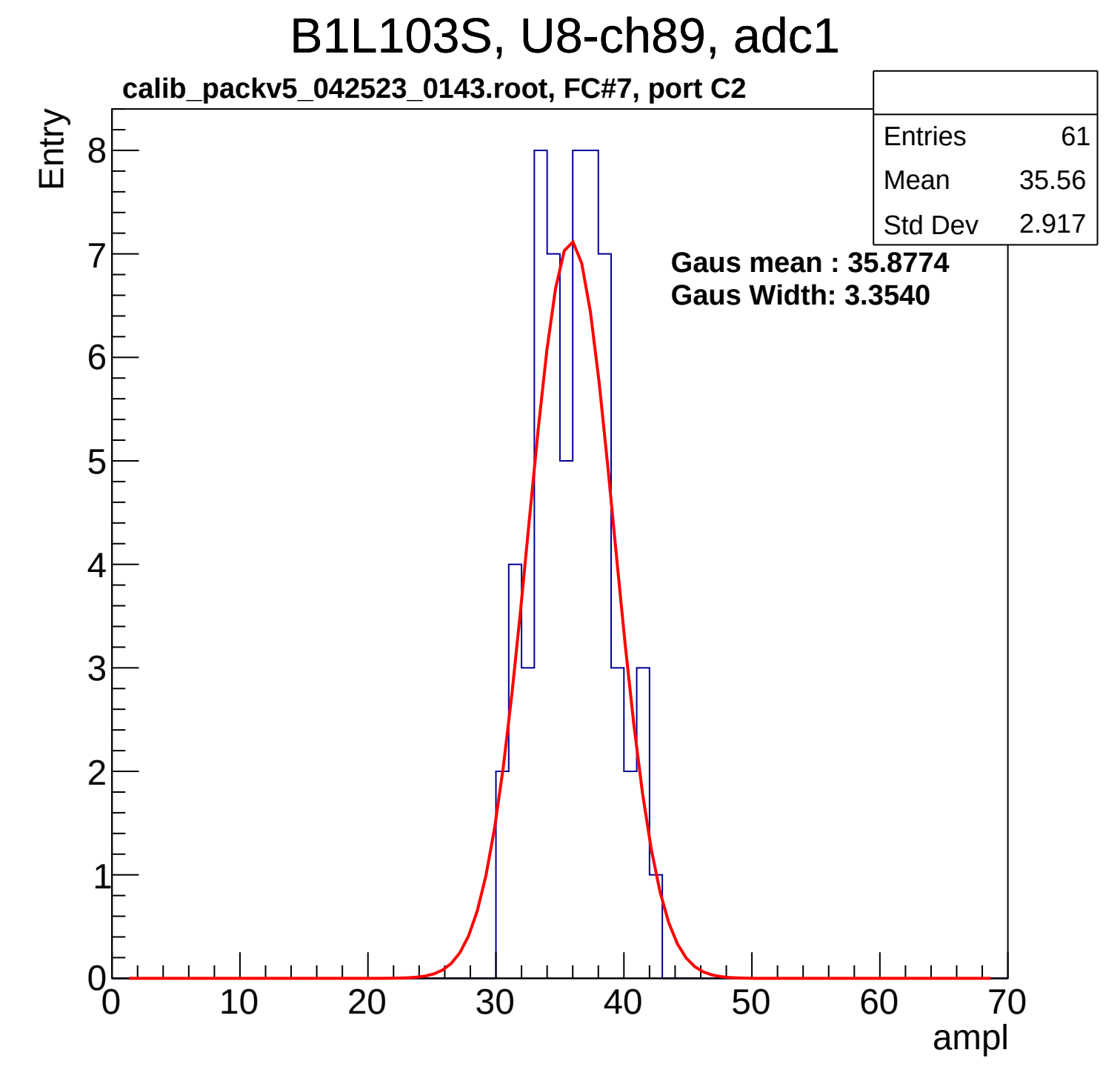

B1L103S, U8-ch88, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 54.86
Std Dev 3.487
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

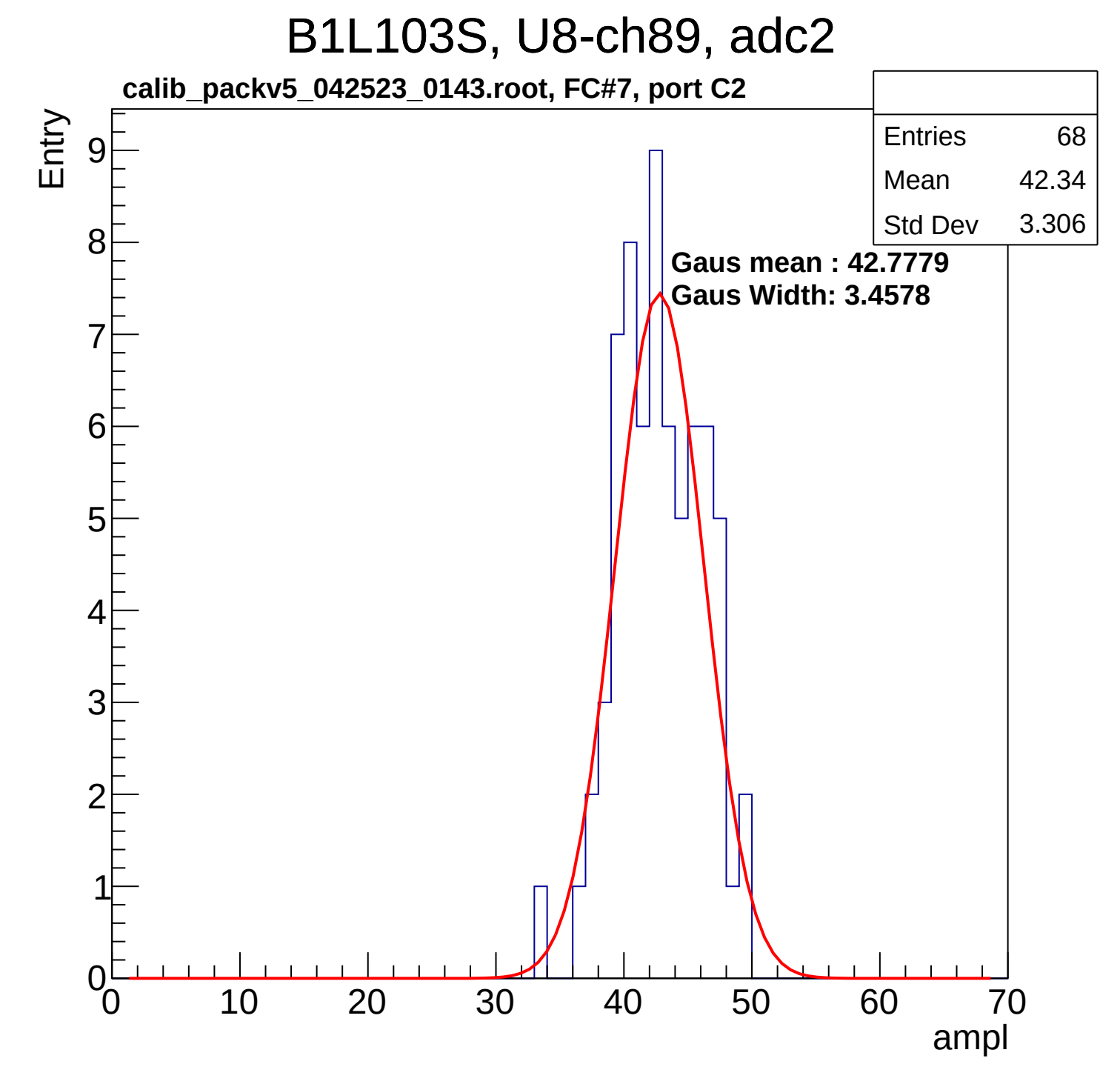

B1L103S, U8-ch88, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 57.74
Std Dev 9.016
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

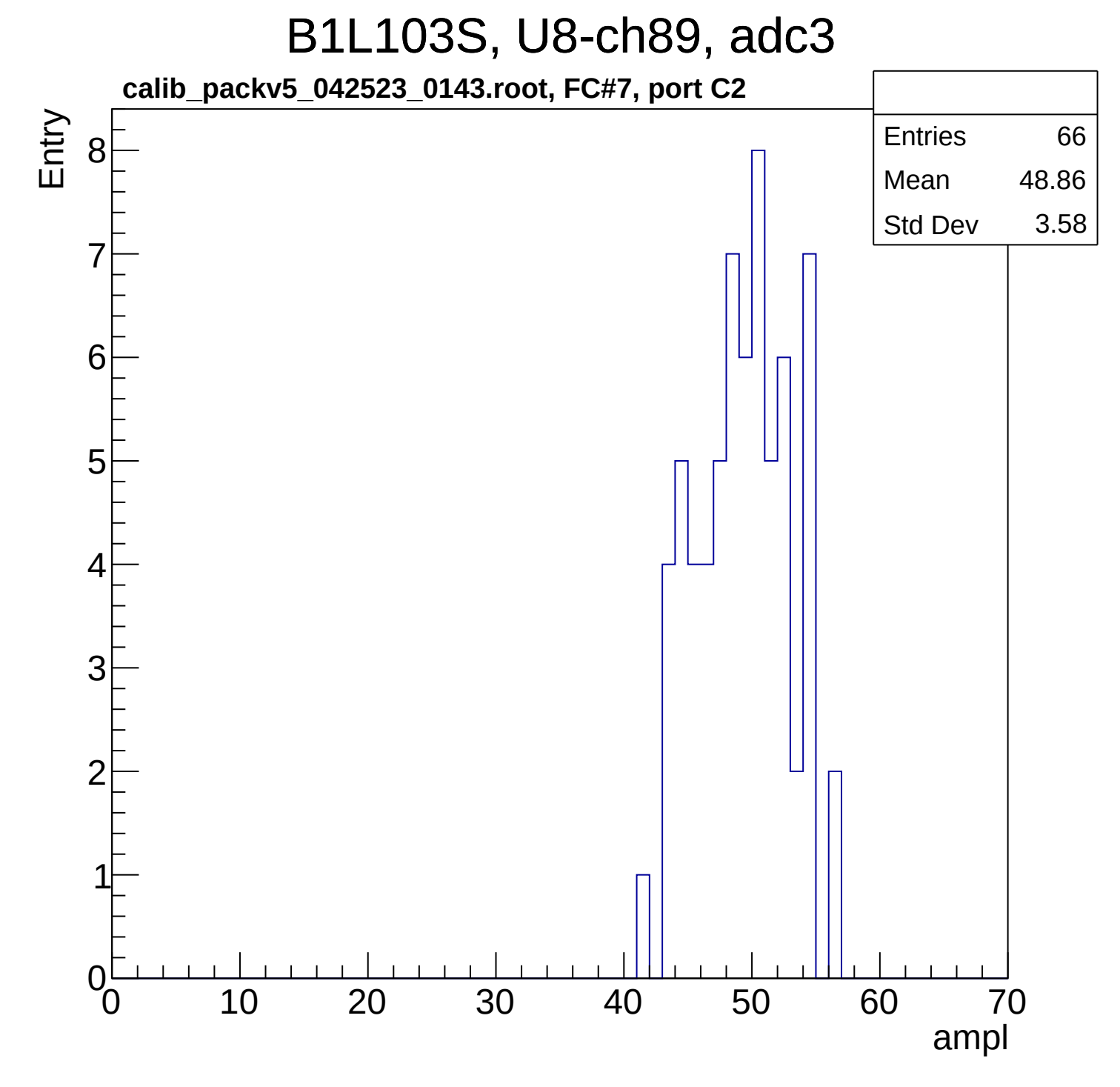

B1L103S, U8-ch88, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 15
Mean 61.33
Std Dev 1.578
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

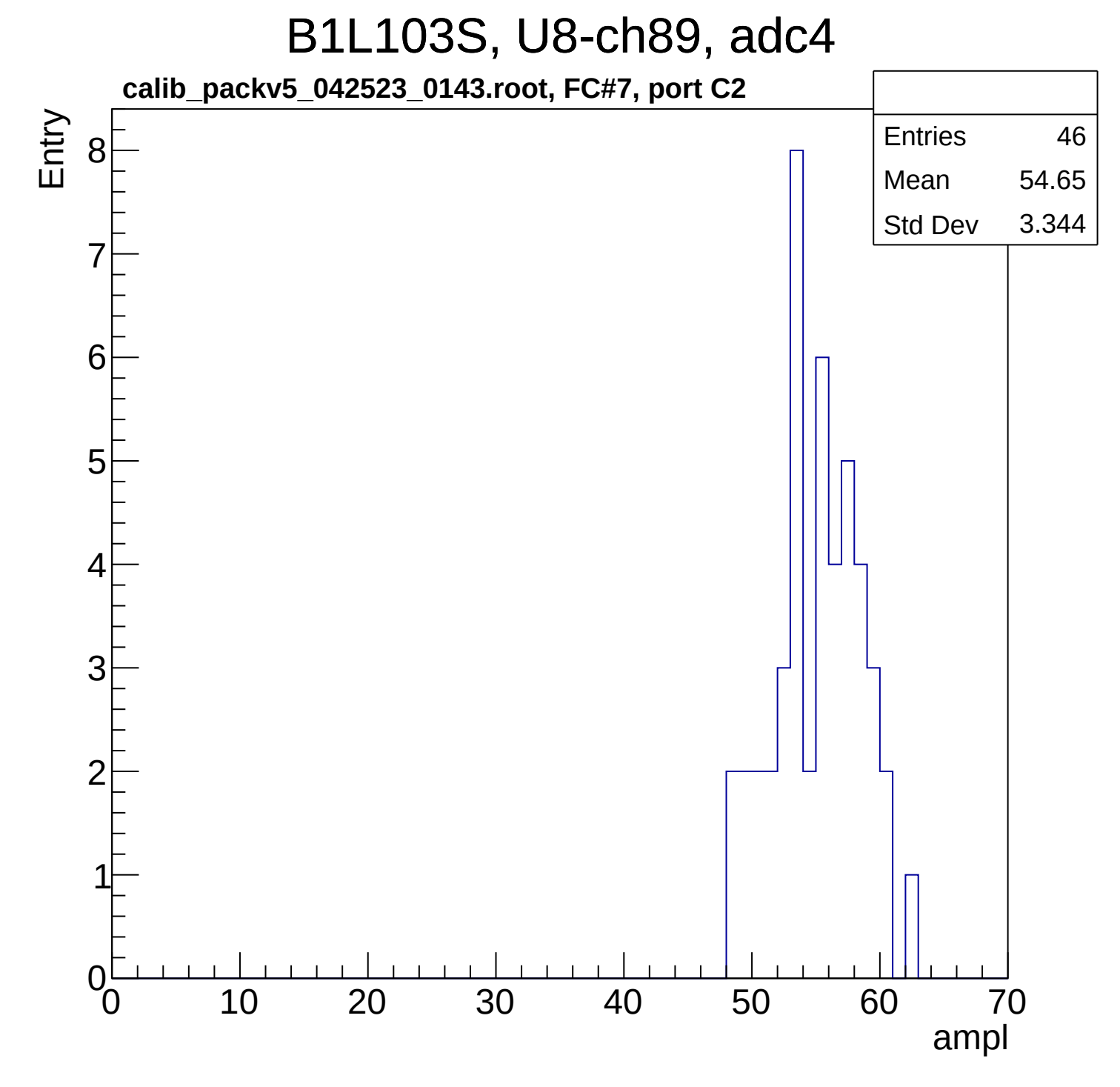

B1L103S, U8-ch88, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

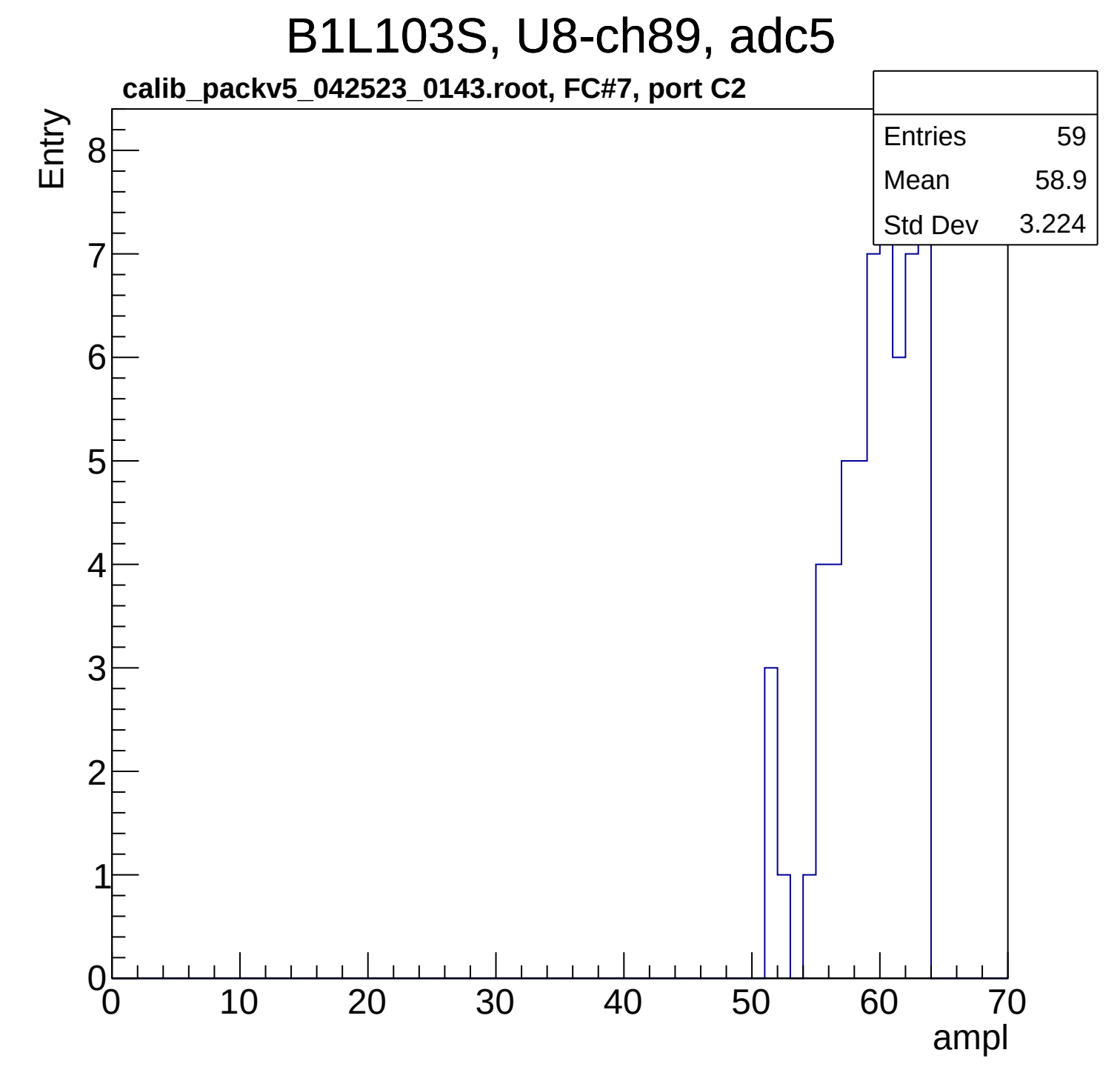

B1L103S, U8-ch89, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 29.68
Std Dev 3.152
Gaus mean : 29.6743
Gaus Width: 2.5450
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

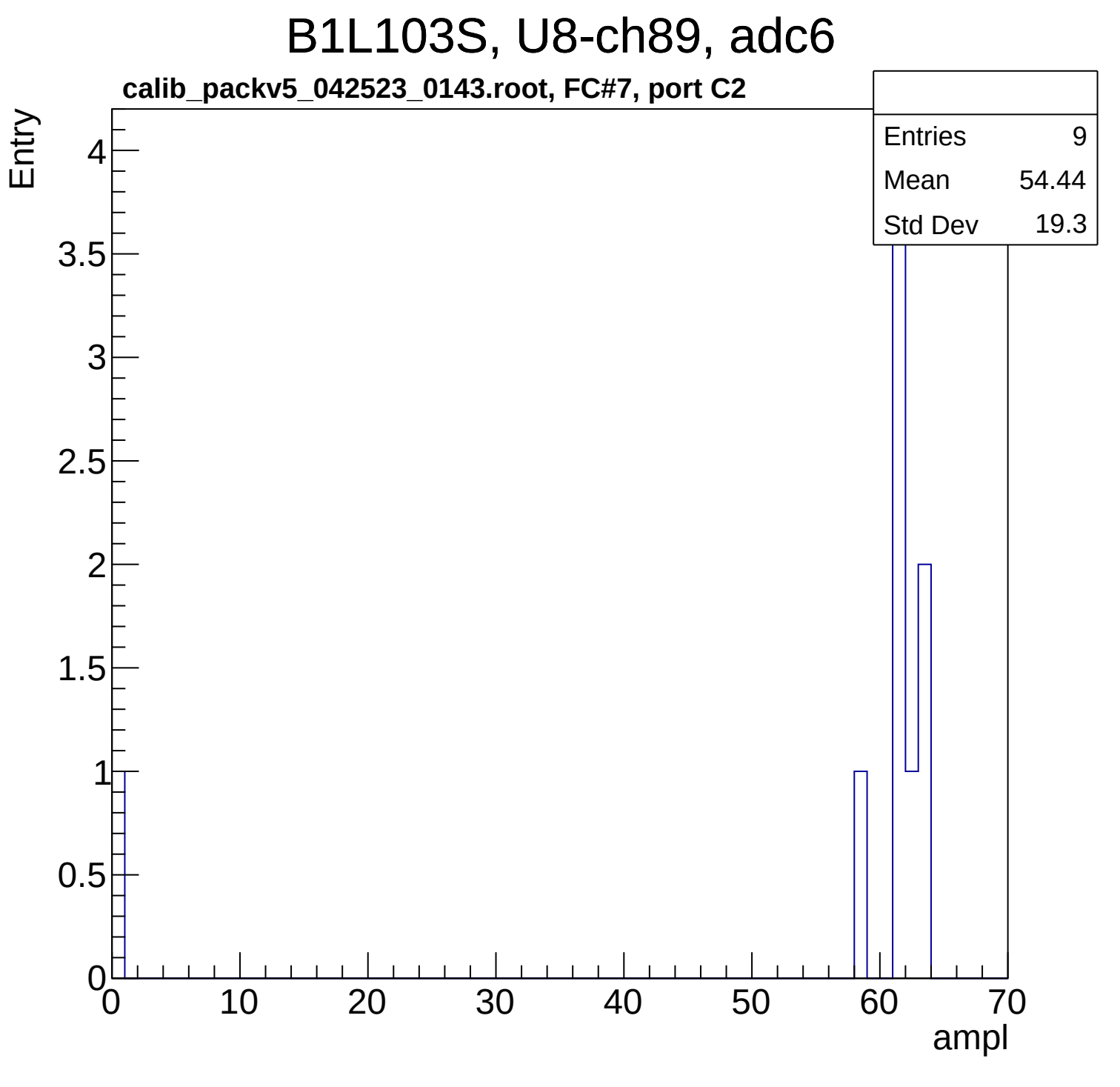

B1L103S, U8-ch89, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 35.56
Std Dev 2.917
Gaus mean : 35.8774
Gaus Width: 3.3540
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

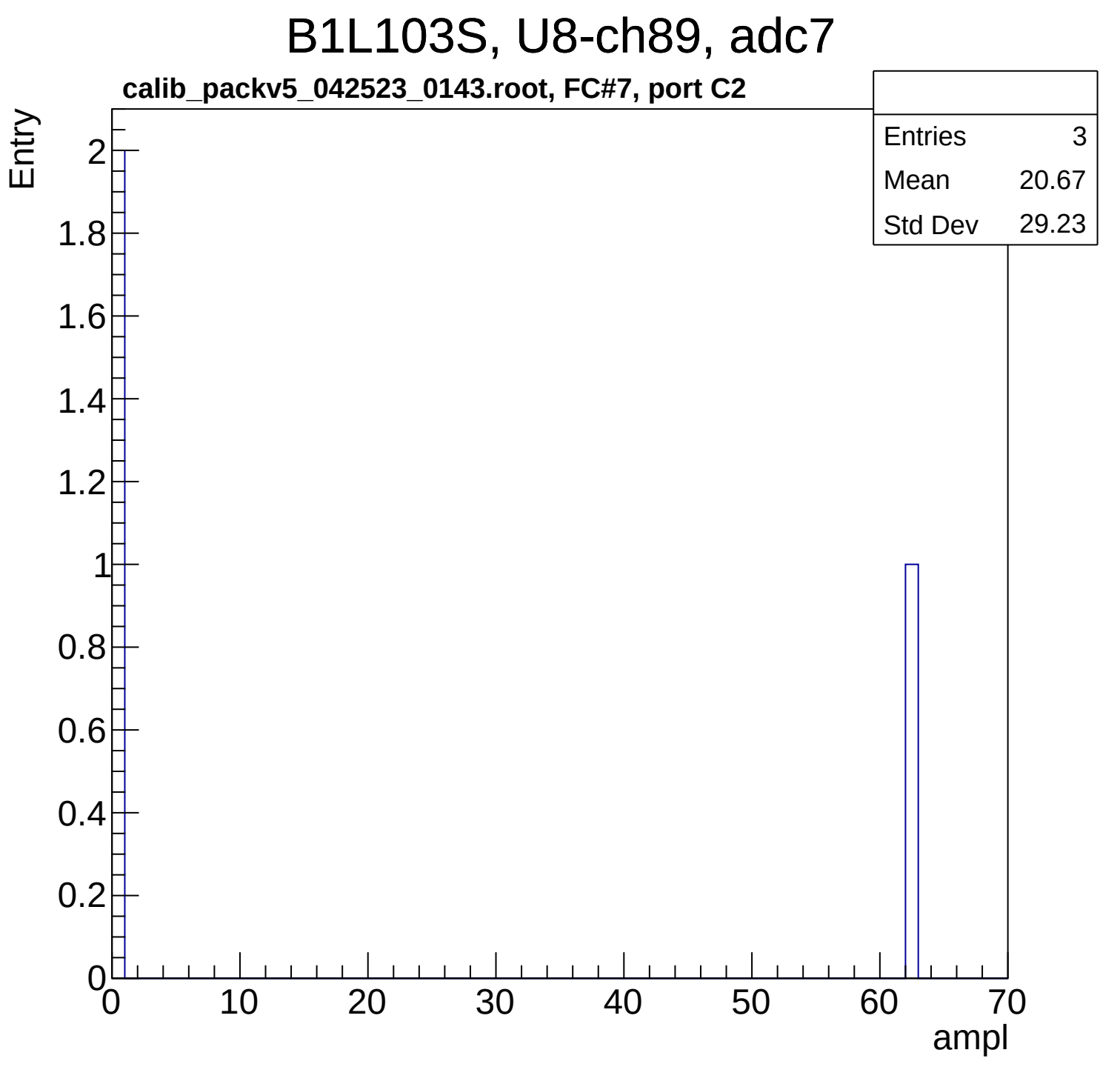

B1L103S, U8-ch89, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 42.34
Std Dev 3.306
Gaus mean : 42.7779
Gaus Width: 3.4578
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

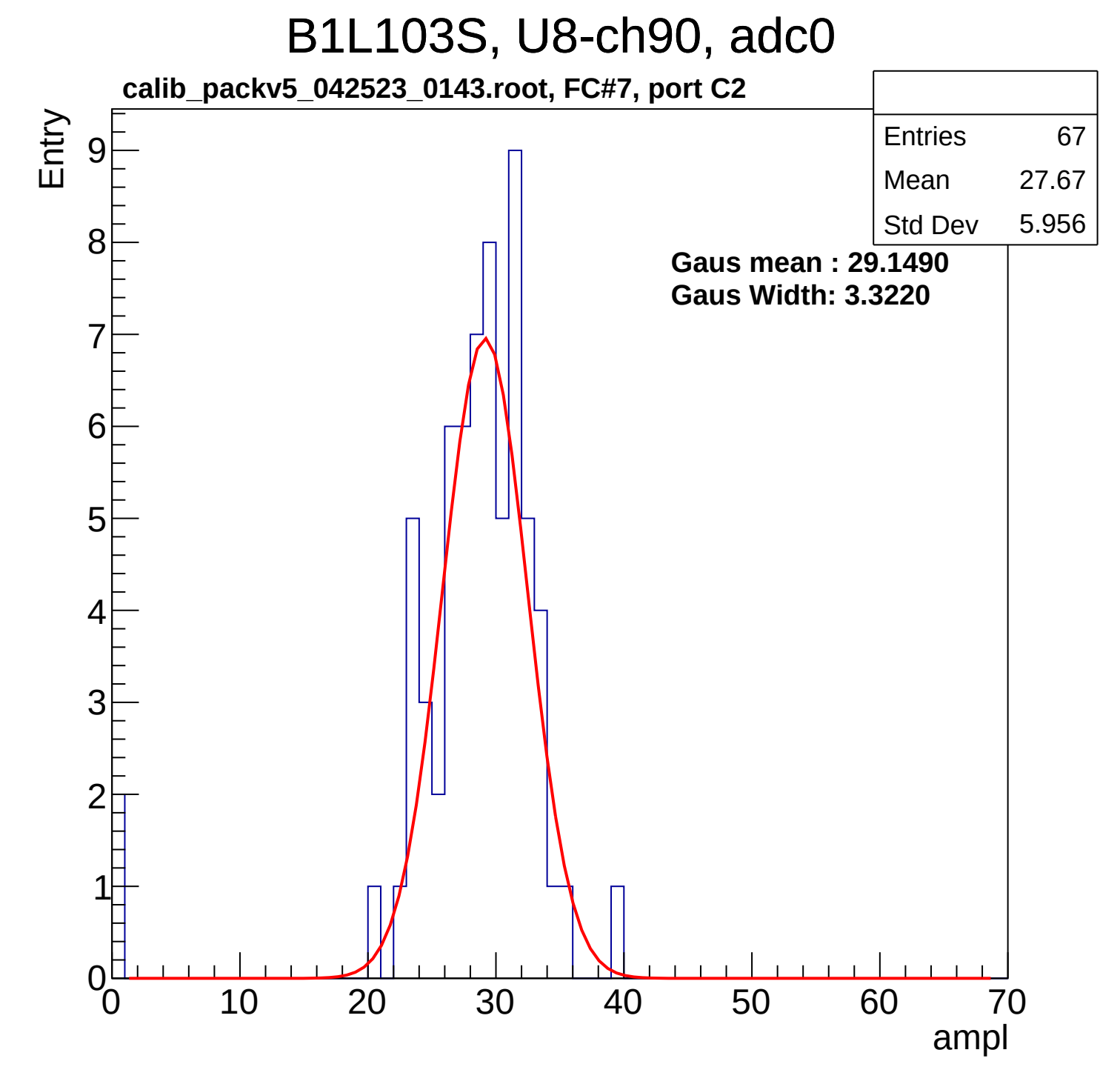

B1L103S, U8-ch89, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 48.86
Std Dev 3.58
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

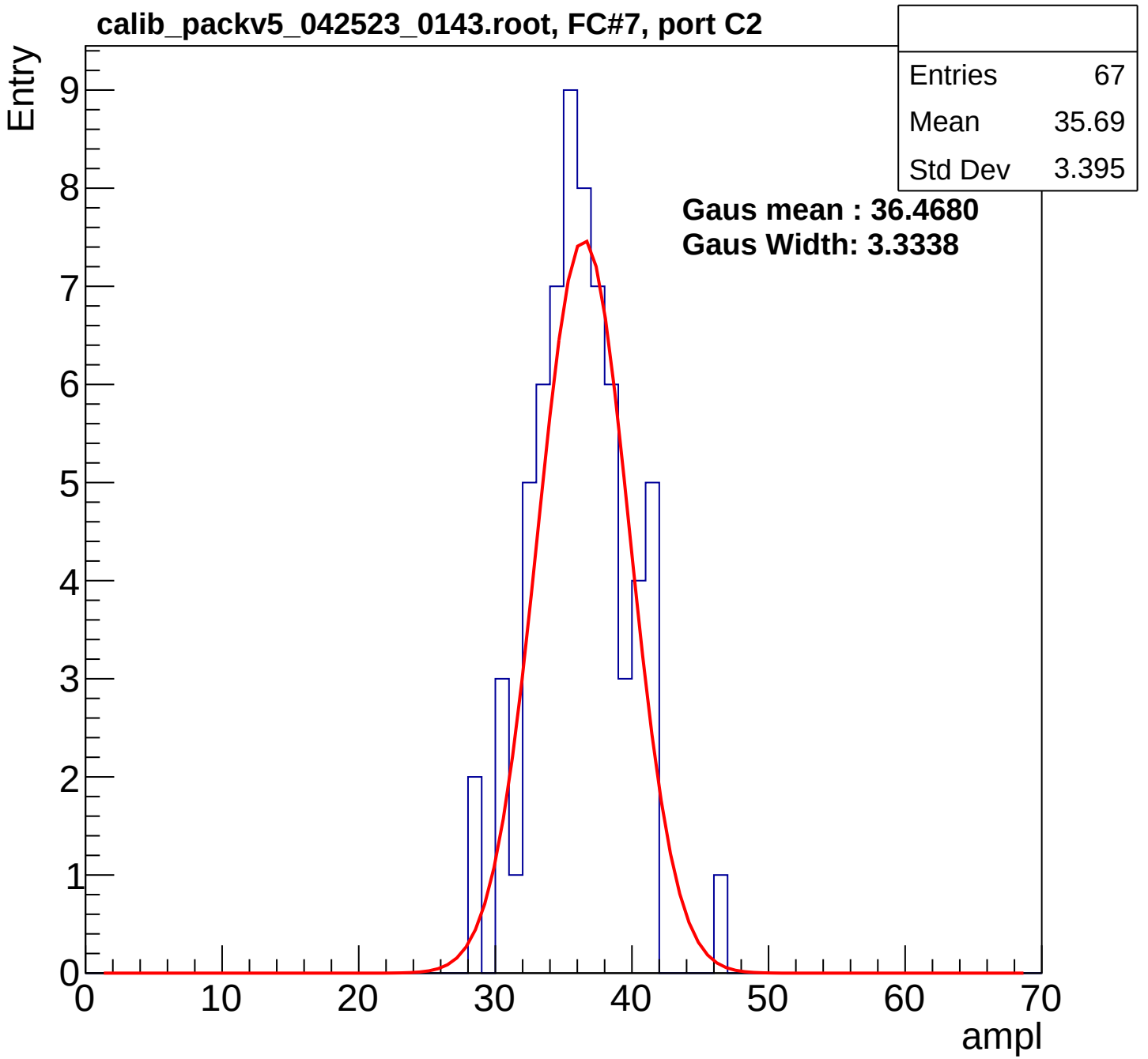

B1L103S, U8-ch89, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 46
Mean 54.65
Std Dev 3.344
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

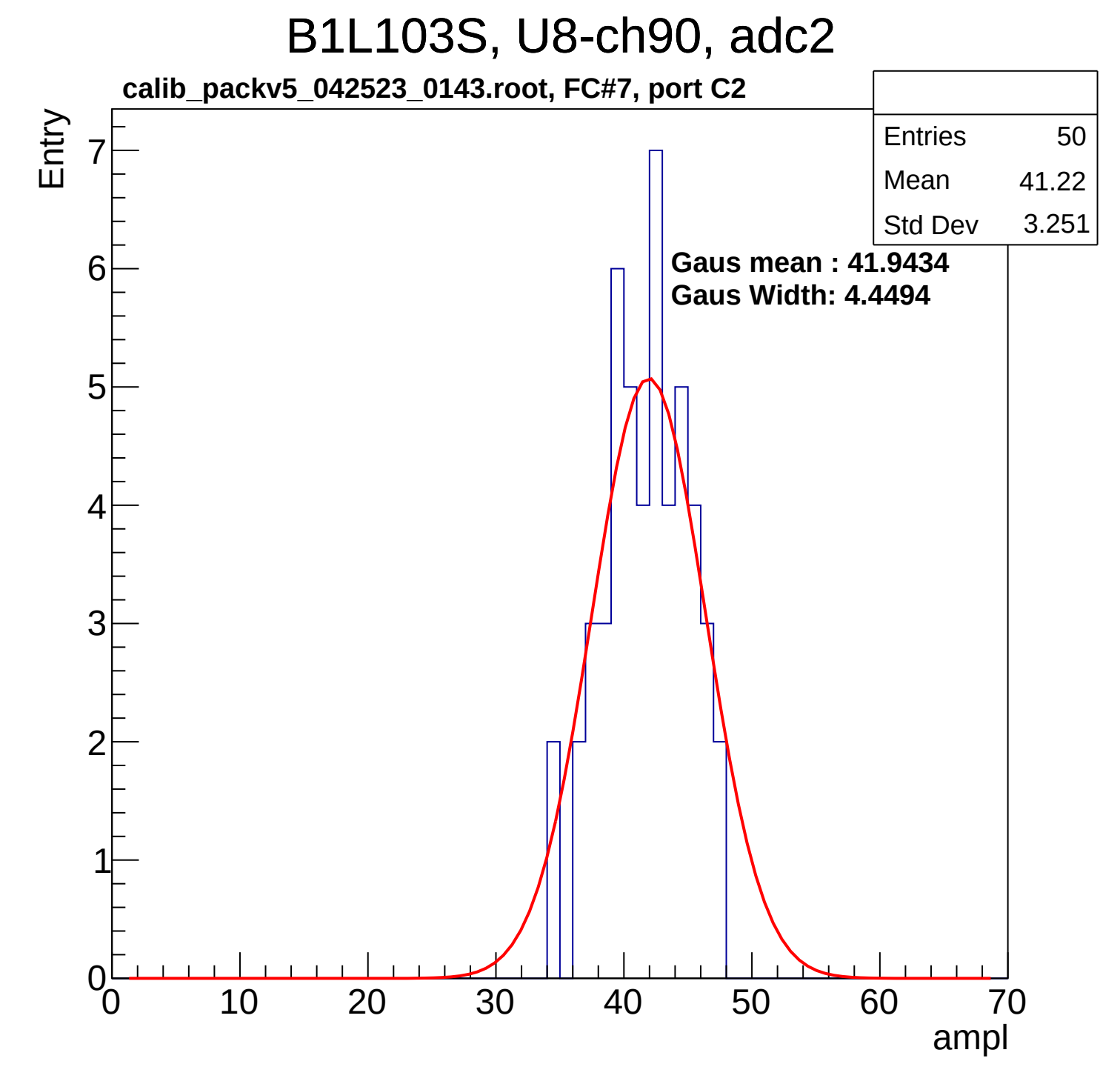

B1L103S, U8-ch89, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 58.9
Std Dev 3.224
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

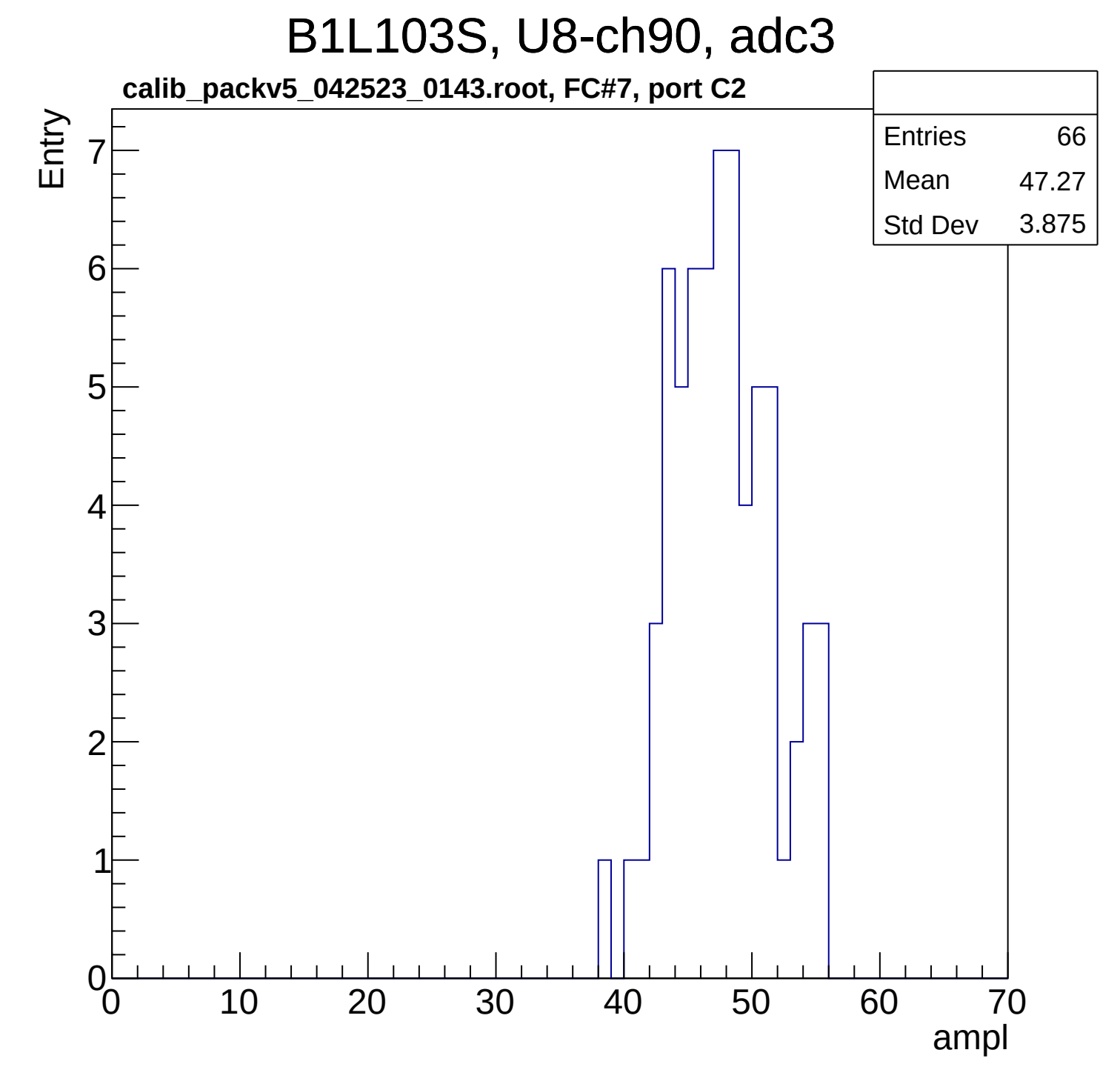

B1L103S, U8-ch89, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 9
Mean 54.44
Std Dev 19.3
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

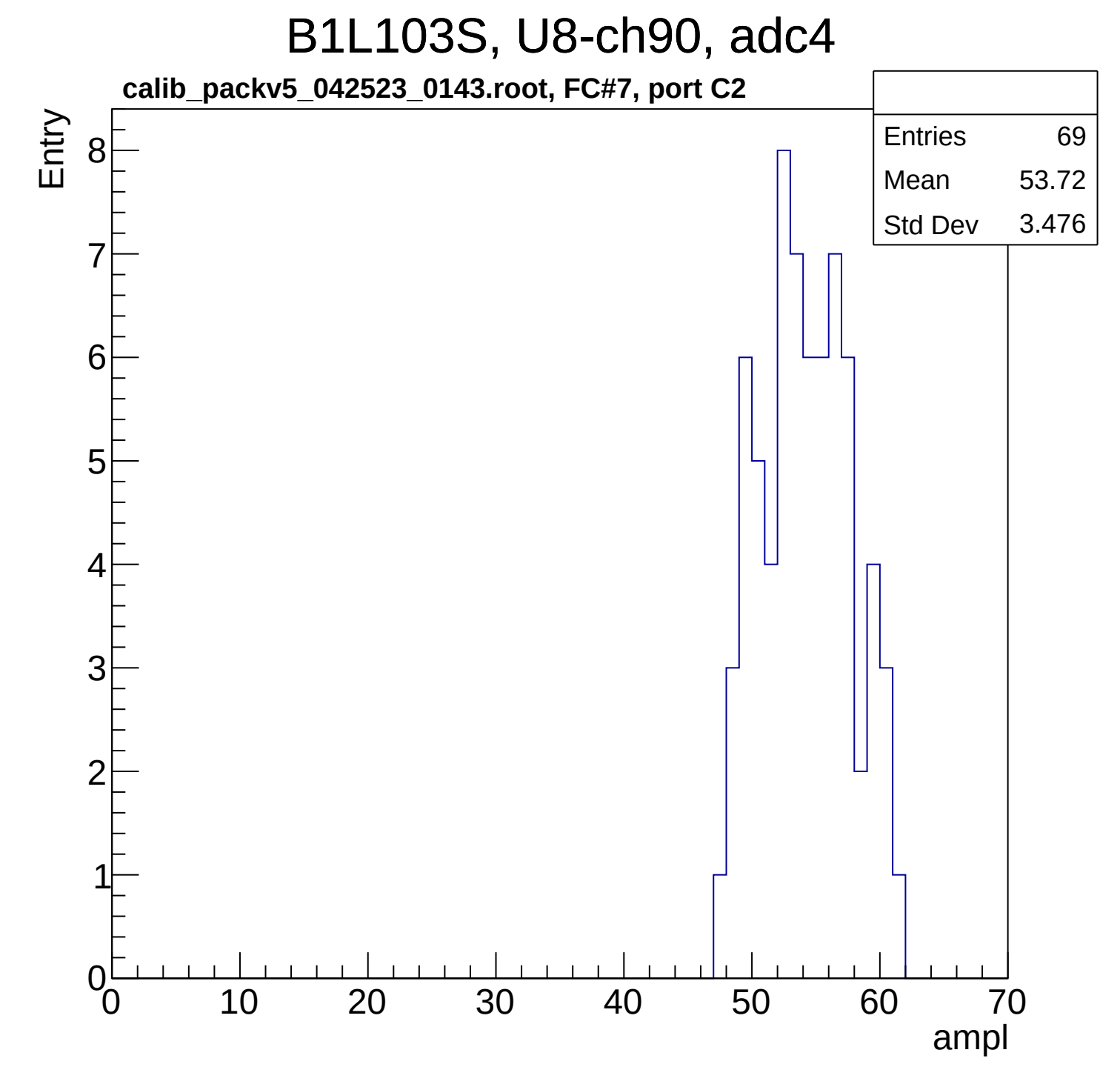

B1L103S, U8-ch89, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 20.67
Std Dev 29.23
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

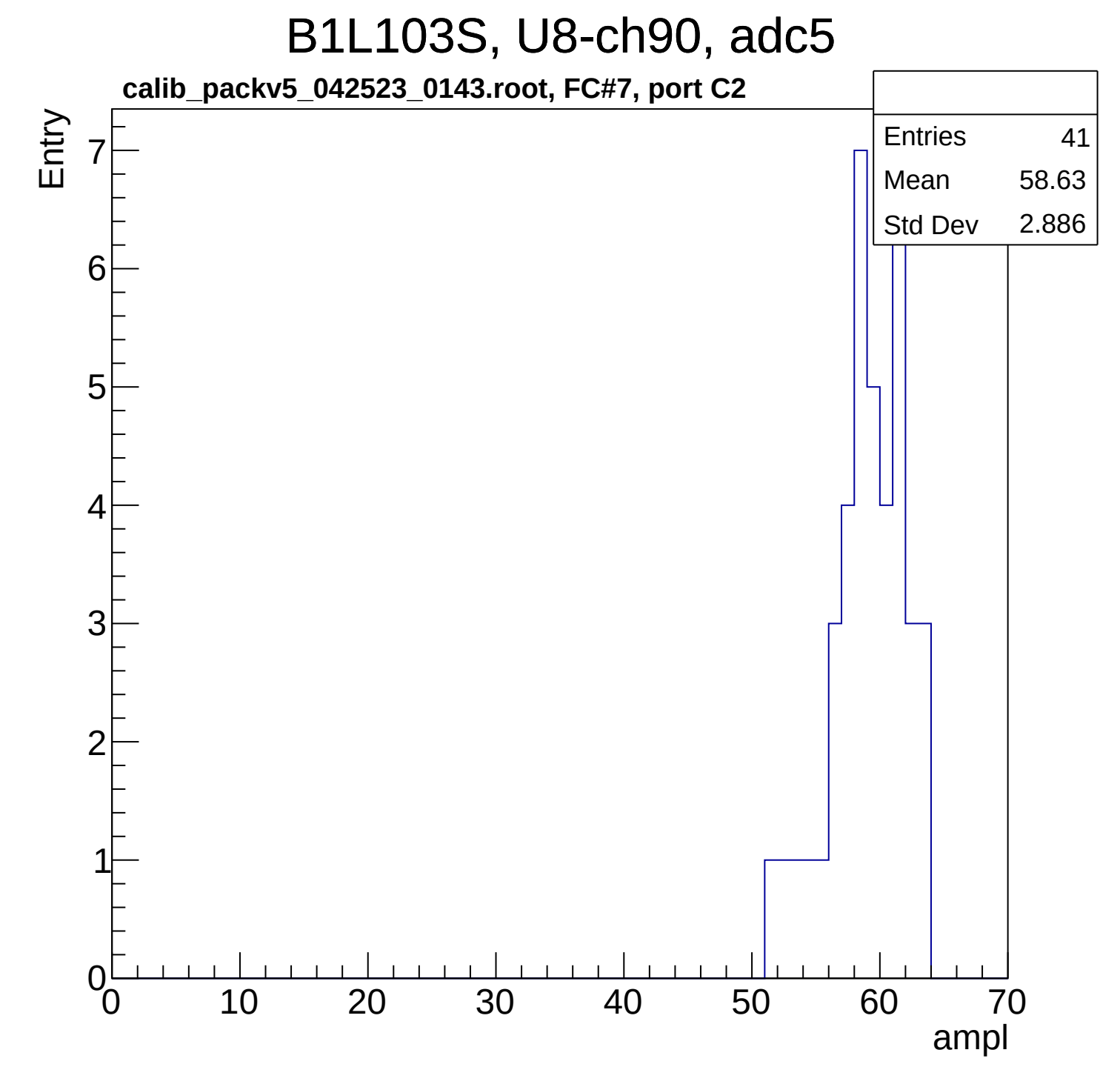

B1L103S, U8-ch90, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 27.67
Std Dev 5.956
Gaus mean : 29.1490
Gaus Width: 3.3220
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

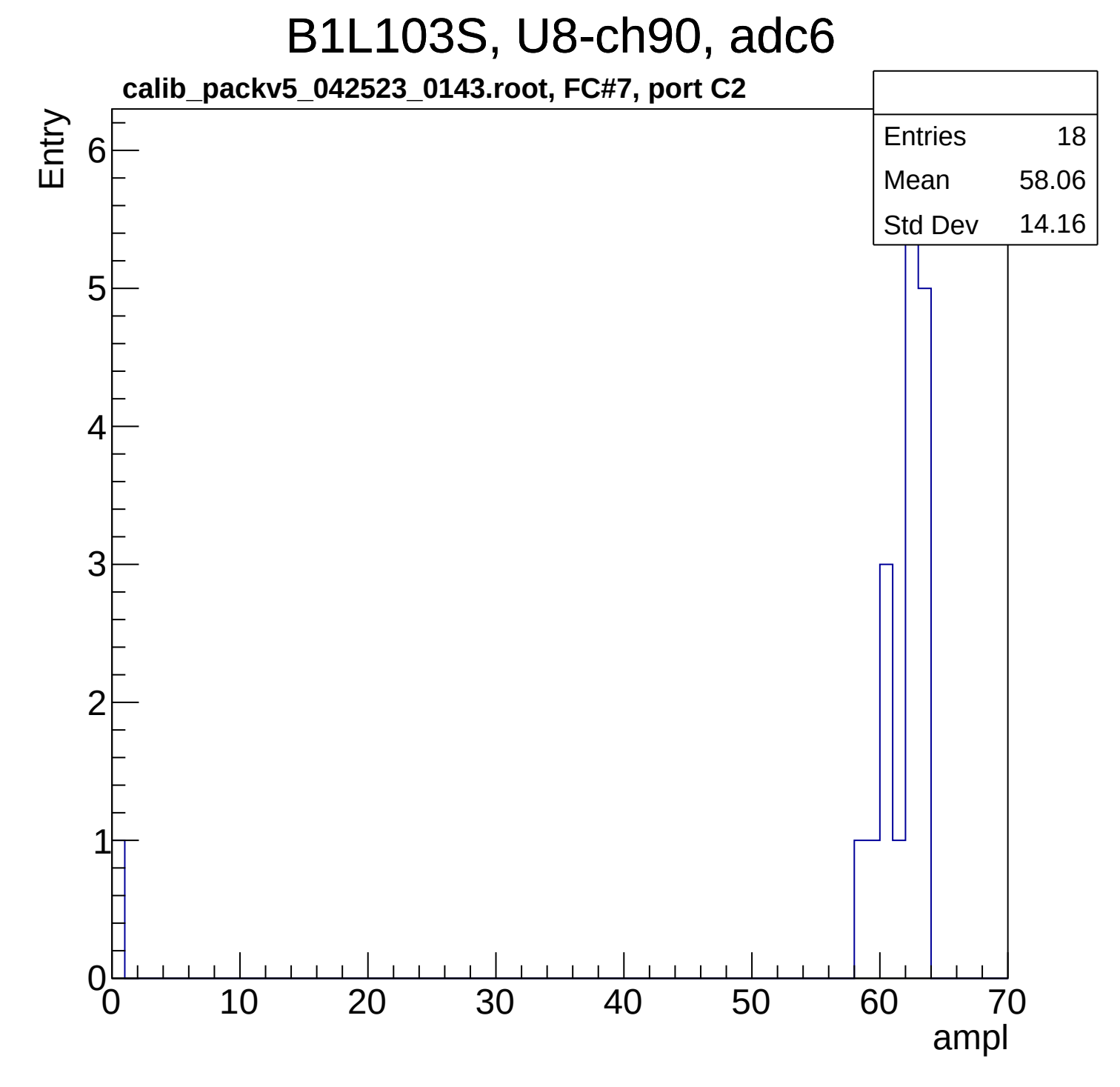

B1L103S, U8-ch90, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 35.69
Std Dev 3.395
Gaus mean : 36.4680
Gaus Width: 3.3338
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

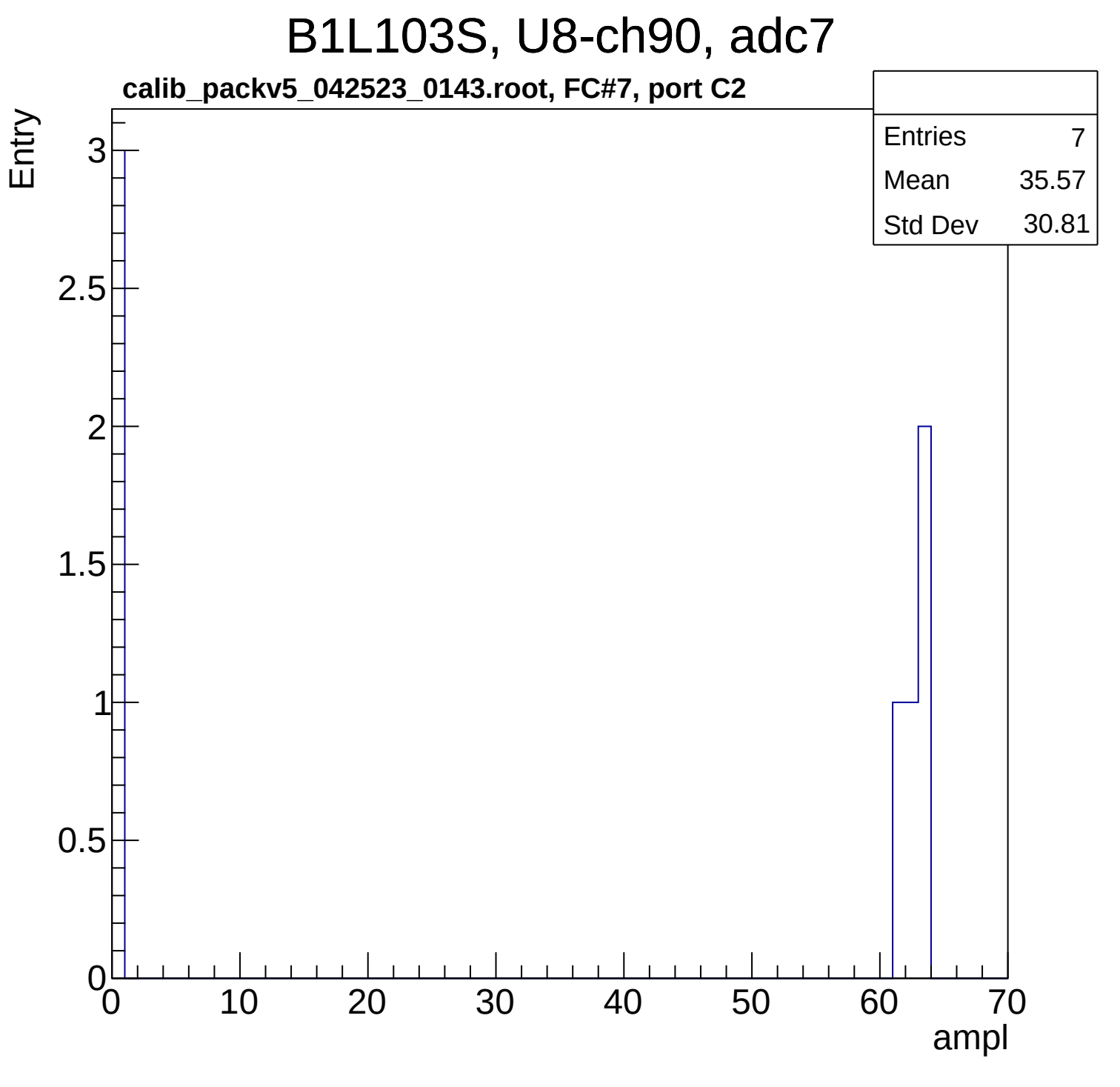

B1L103S, U8-ch90, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 41.22
Std Dev 3.251
Gaus mean : 41.9434
Gaus Width: 4.4494
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

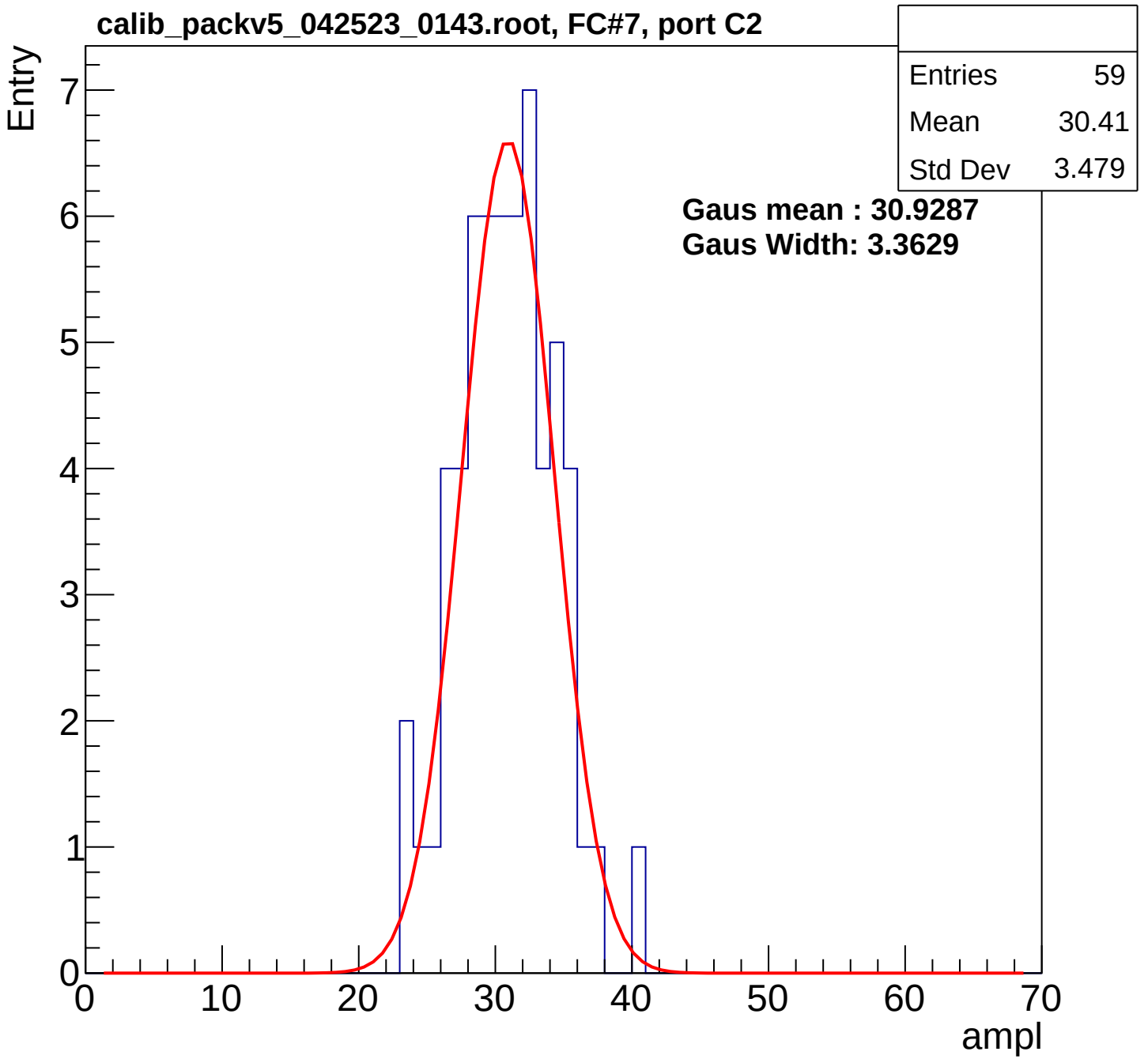

B1L103S, U8-ch90, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 47.27
Std Dev 3.875
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

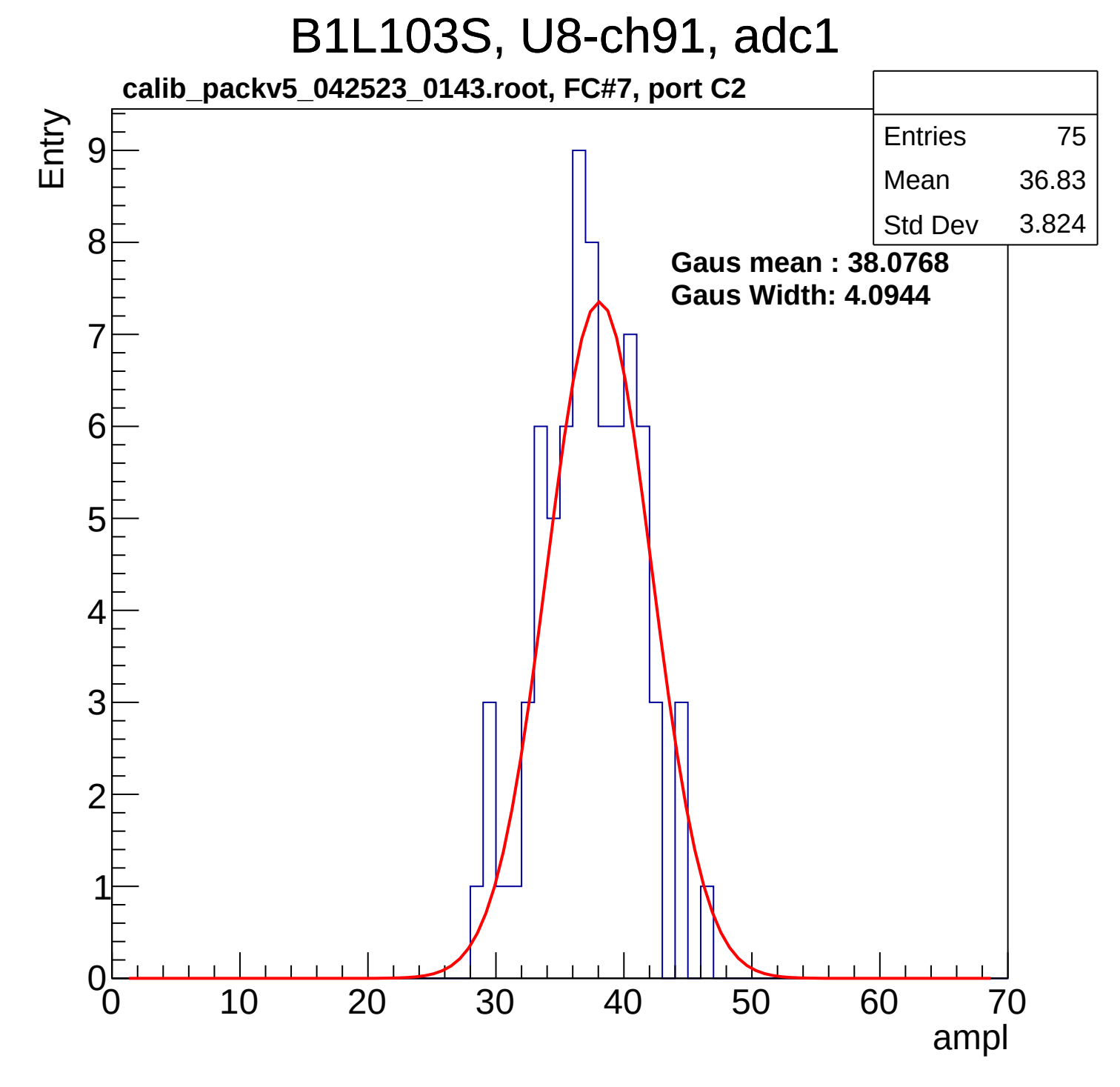

B1L103S, U8-ch90, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 53.72
Std Dev 3.476
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

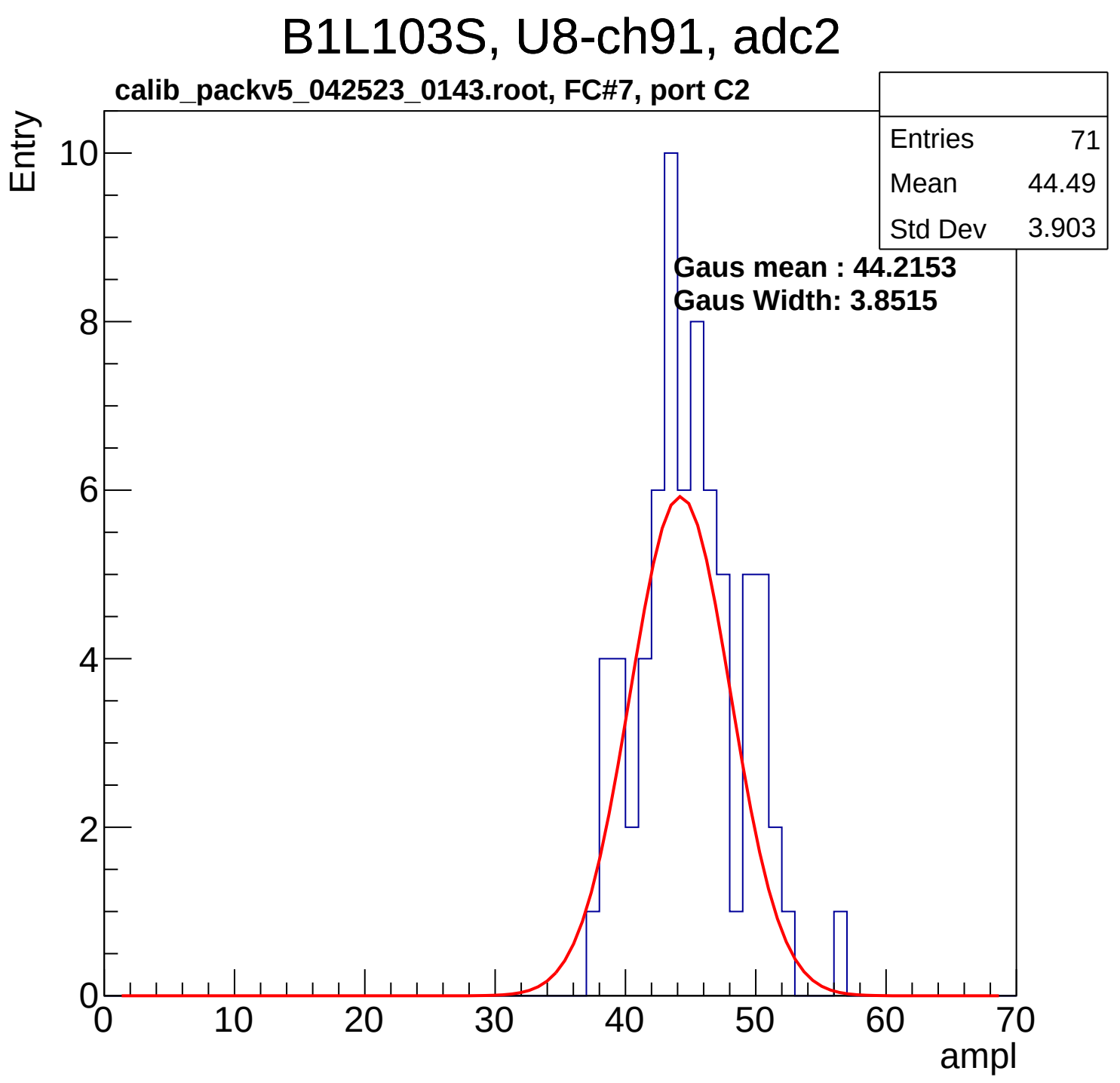

B1L103S, U8-ch90, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 41
Mean 58.63
Std Dev 2.886
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

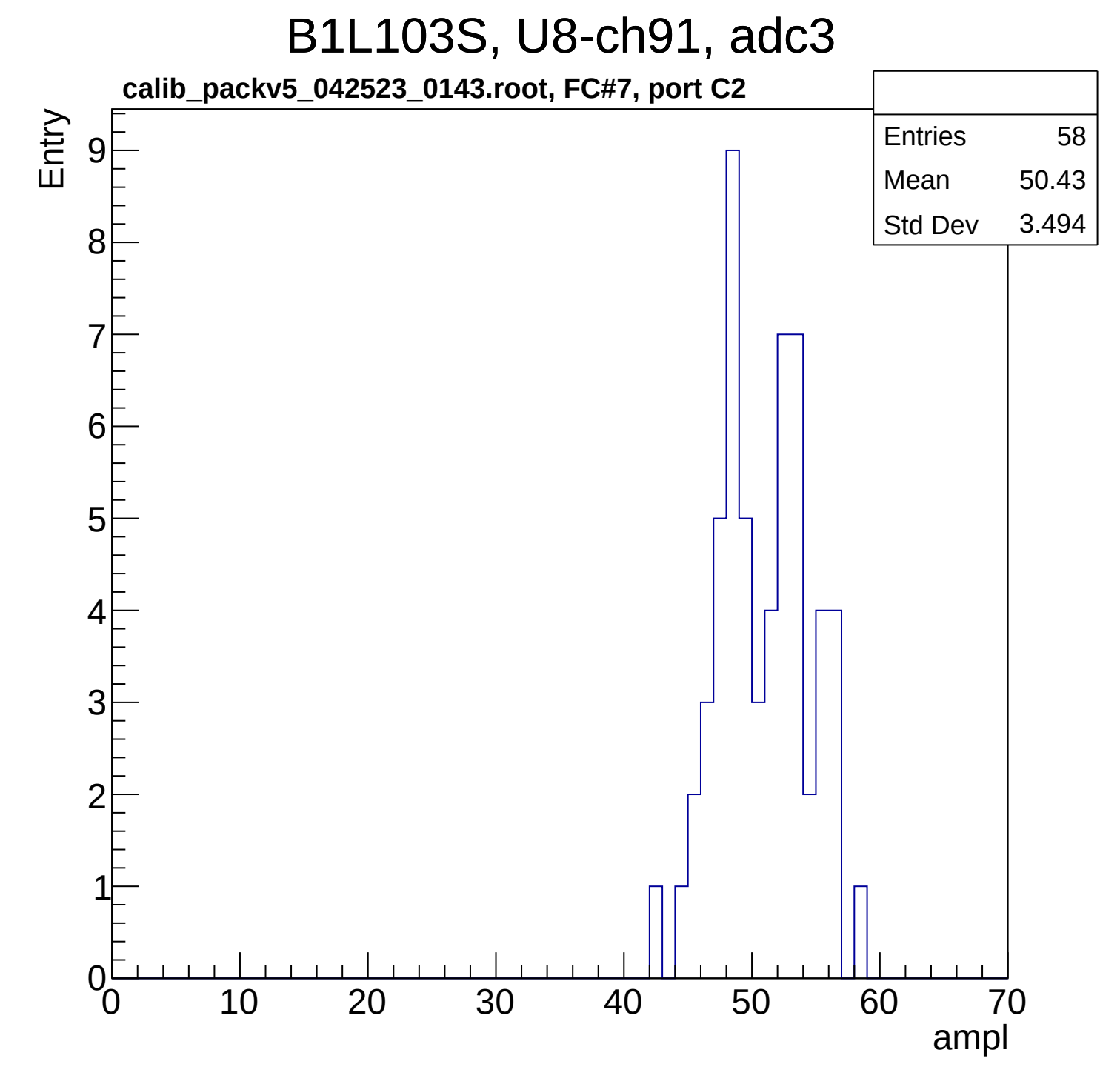

B1L103S, U8-ch90, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 18
Mean 58.06
Std Dev 14.16
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

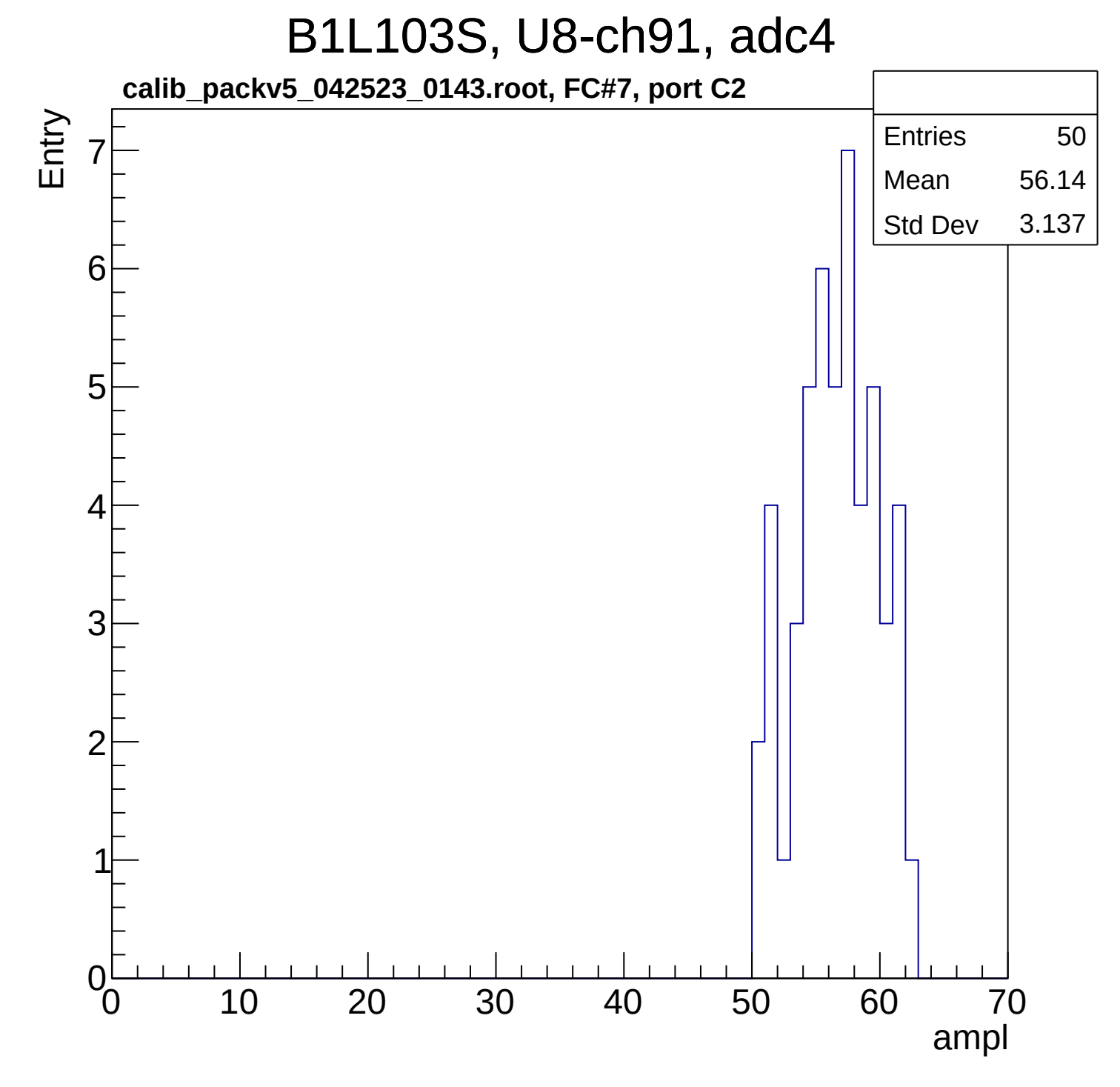

B1L103S, U8-ch90, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 7
Mean 35.57
Std Dev 30.81
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl

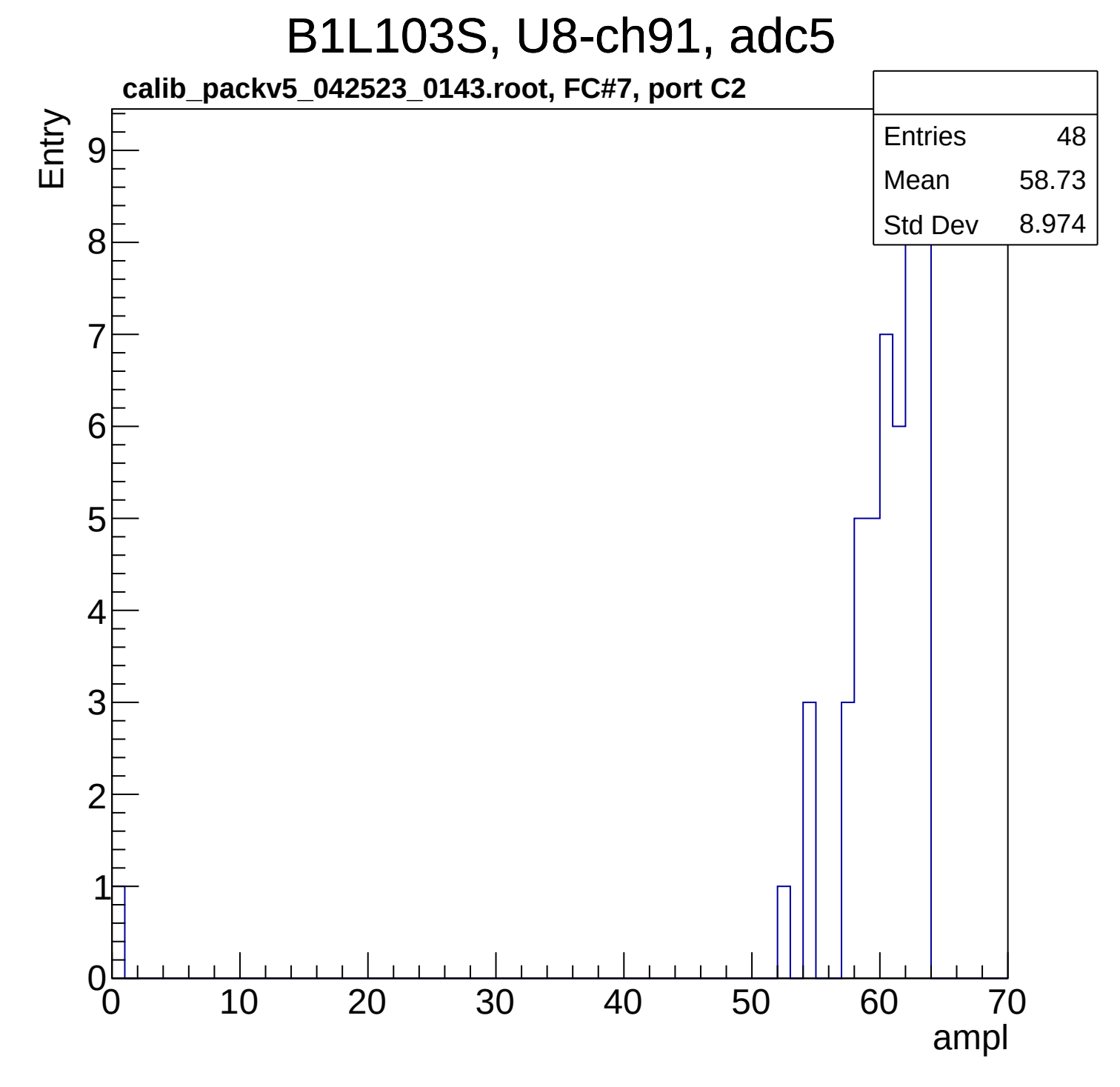

B1L103S, U8-ch91, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 30.41
Std Dev 3.479
Gaus mean : 30.9287
Gaus Width: 3.3629
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

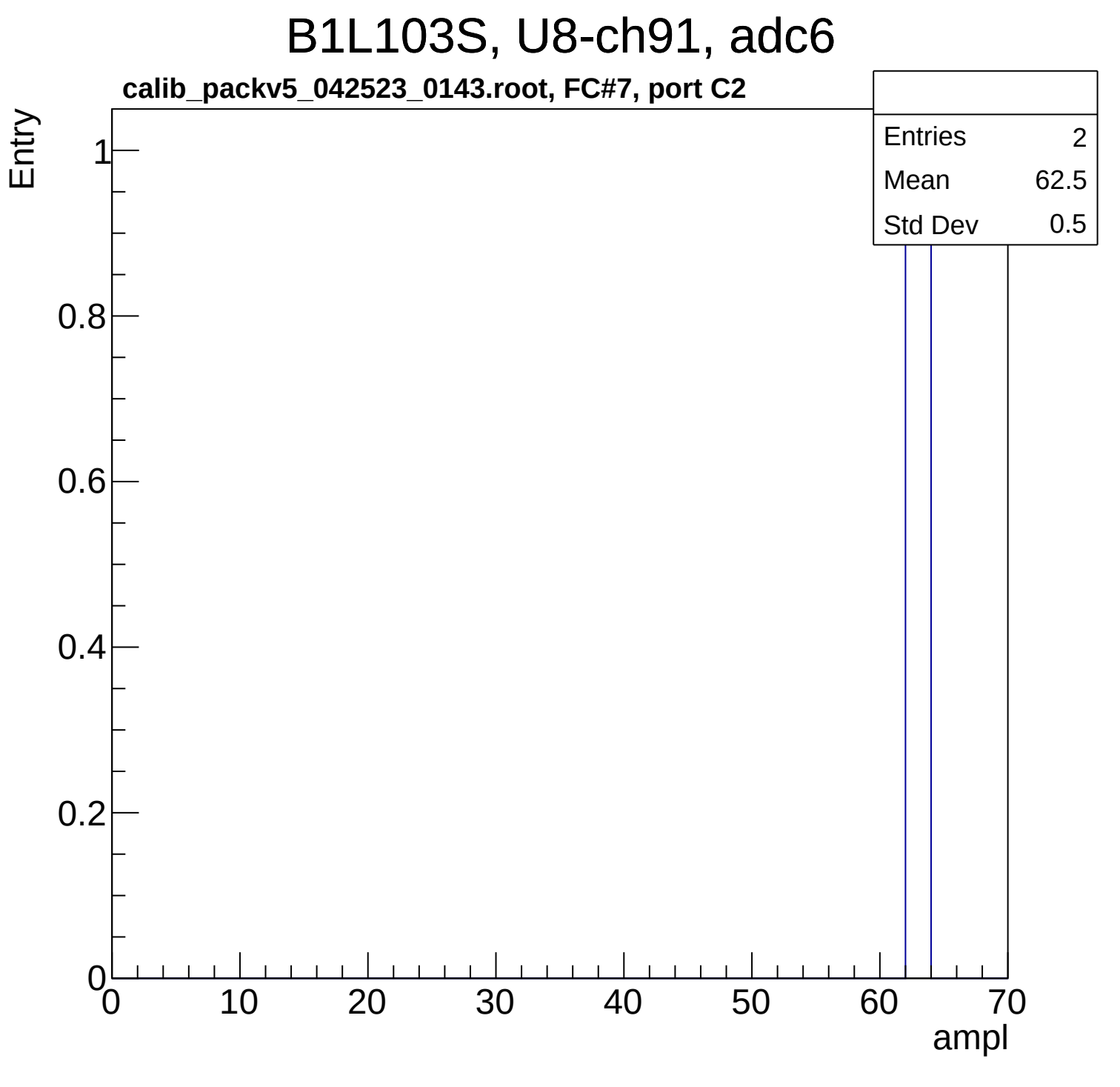

B1L103S, U8-ch91, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 36.83
Std Dev 3.824
Gaus mean : 38.0768
Gaus Width: 4.0944
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

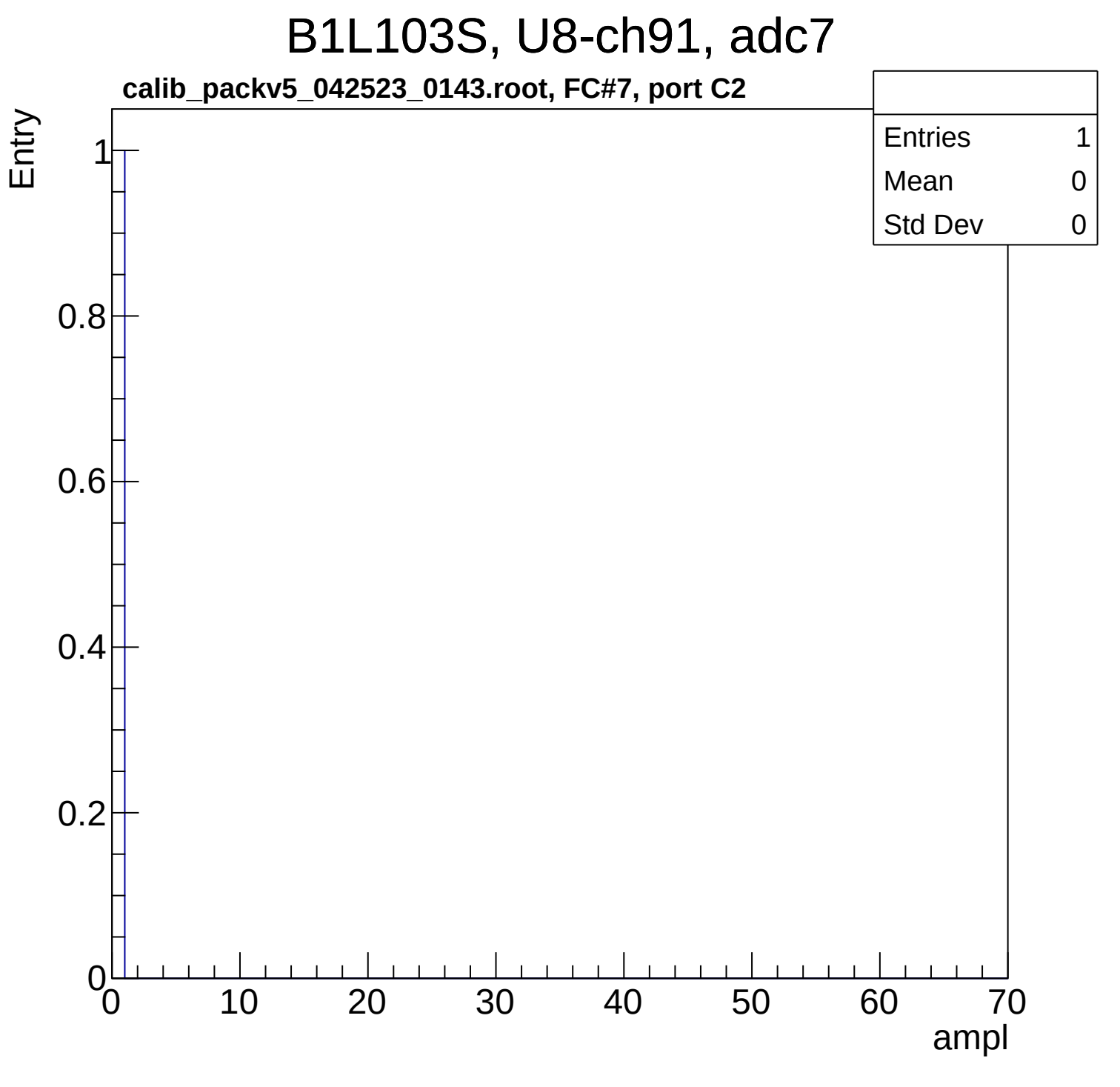

B1L103S, U8-ch91, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 44.49
Std Dev 3.903
Gaus mean : 44.2153
Gaus Width: 3.8515
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

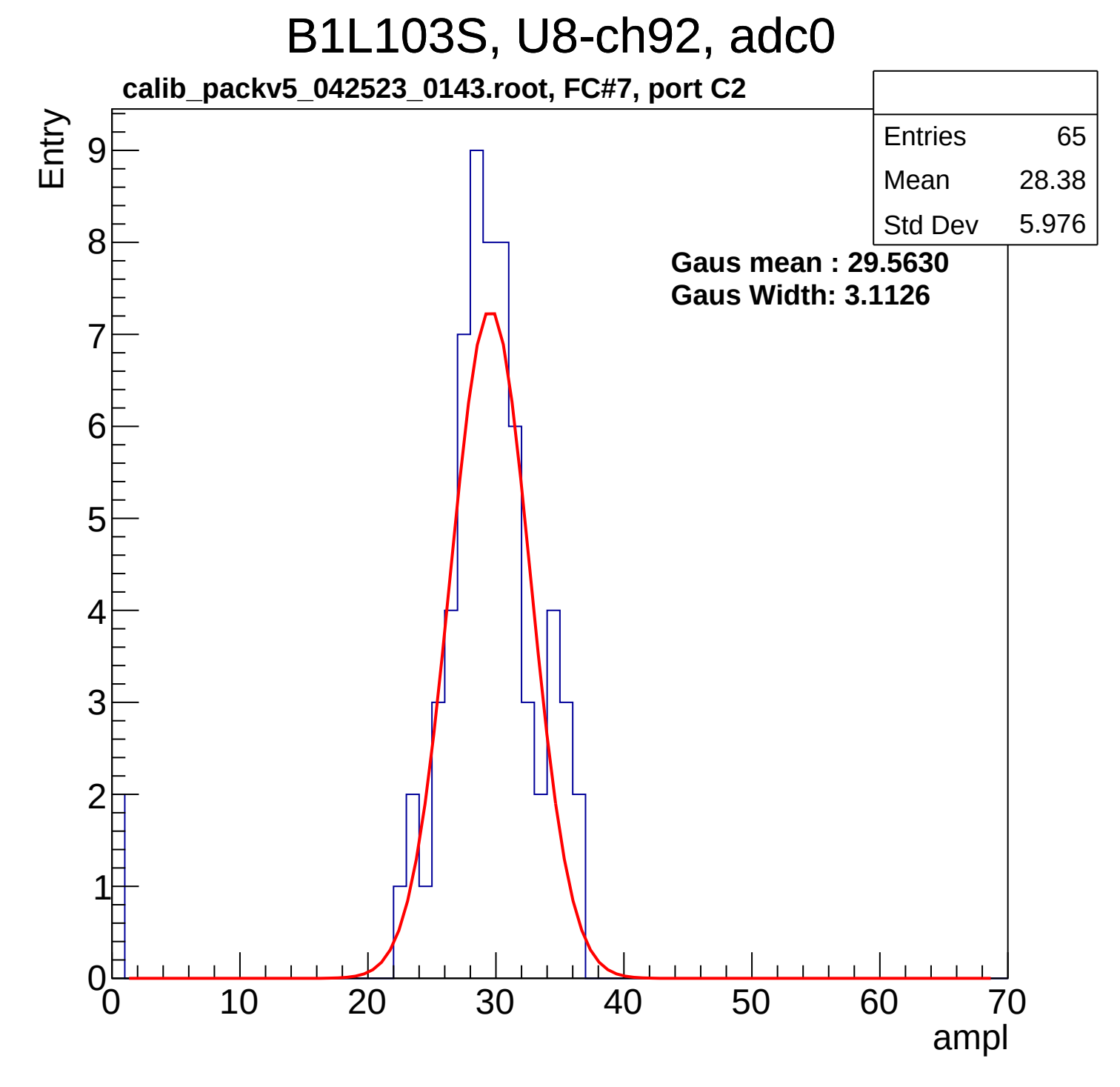

B1L103S, U8-ch91, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 50.43
Std Dev 3.494
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

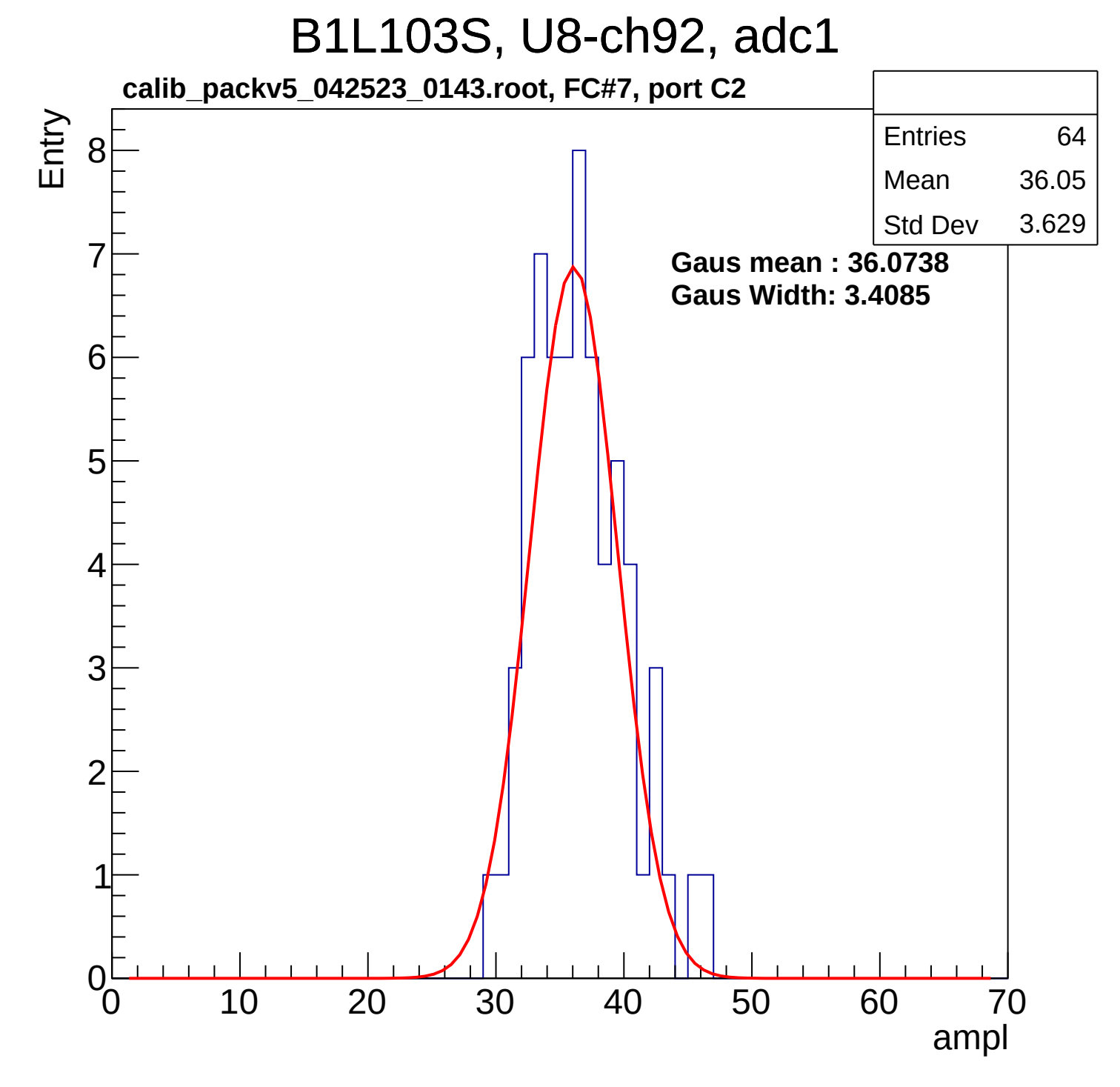

B1L103S, U8-ch91, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 56.14
Std Dev 3.137
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

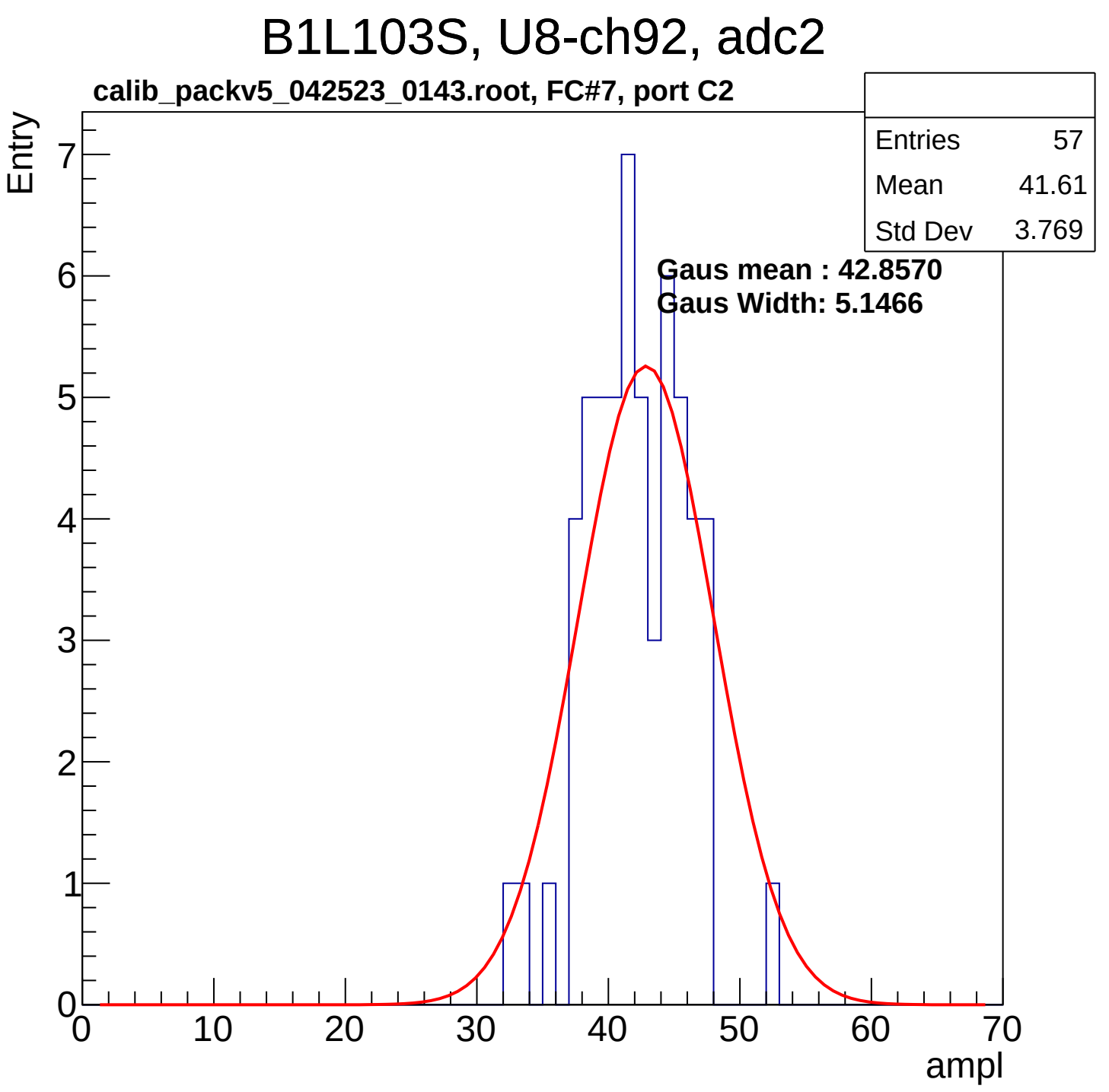

B1L103S, U8-ch91, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 58.73
Std Dev 8.974
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

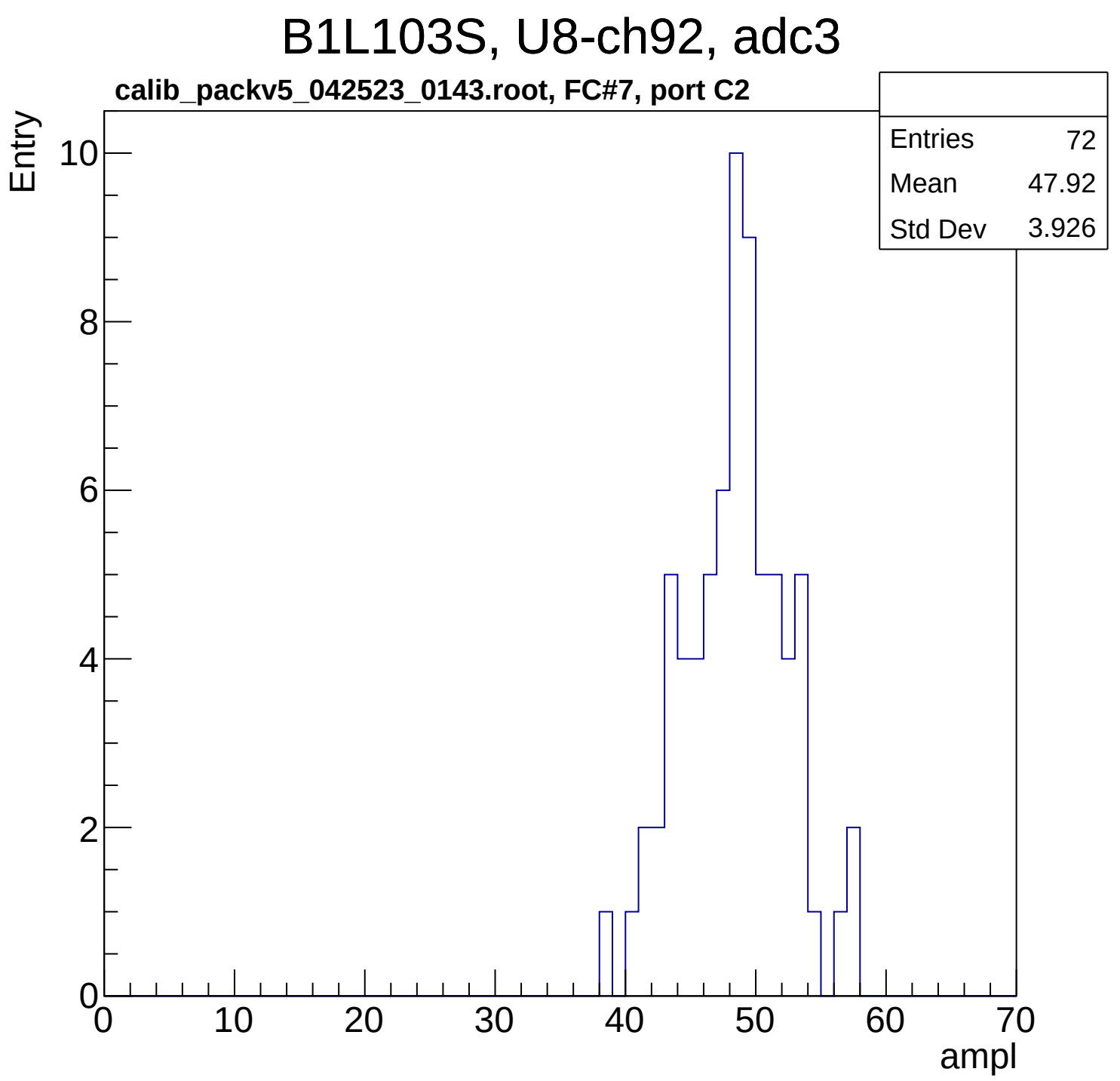

B1L103S, U8-ch91, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

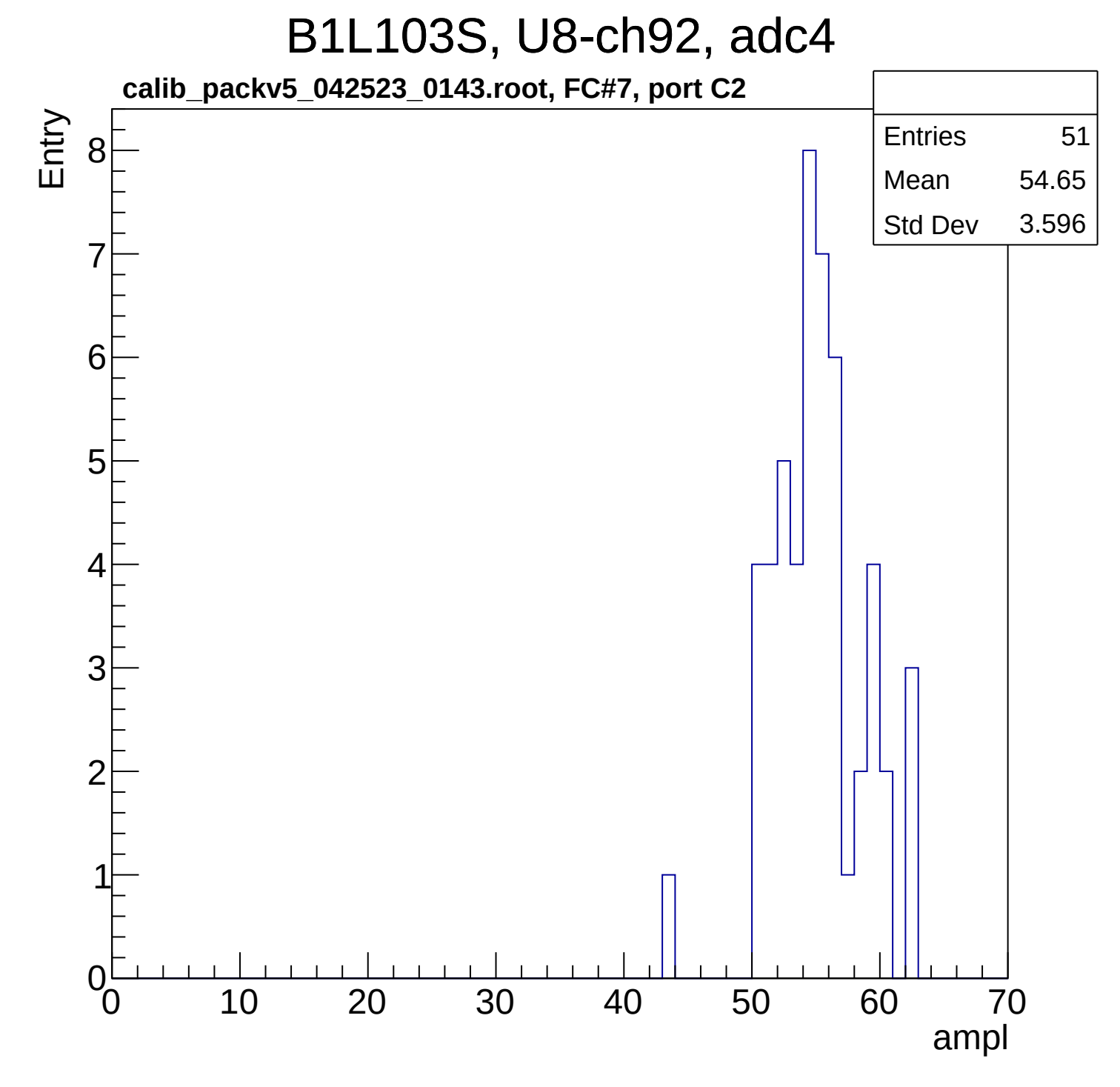

B1L103S, U8-ch91, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

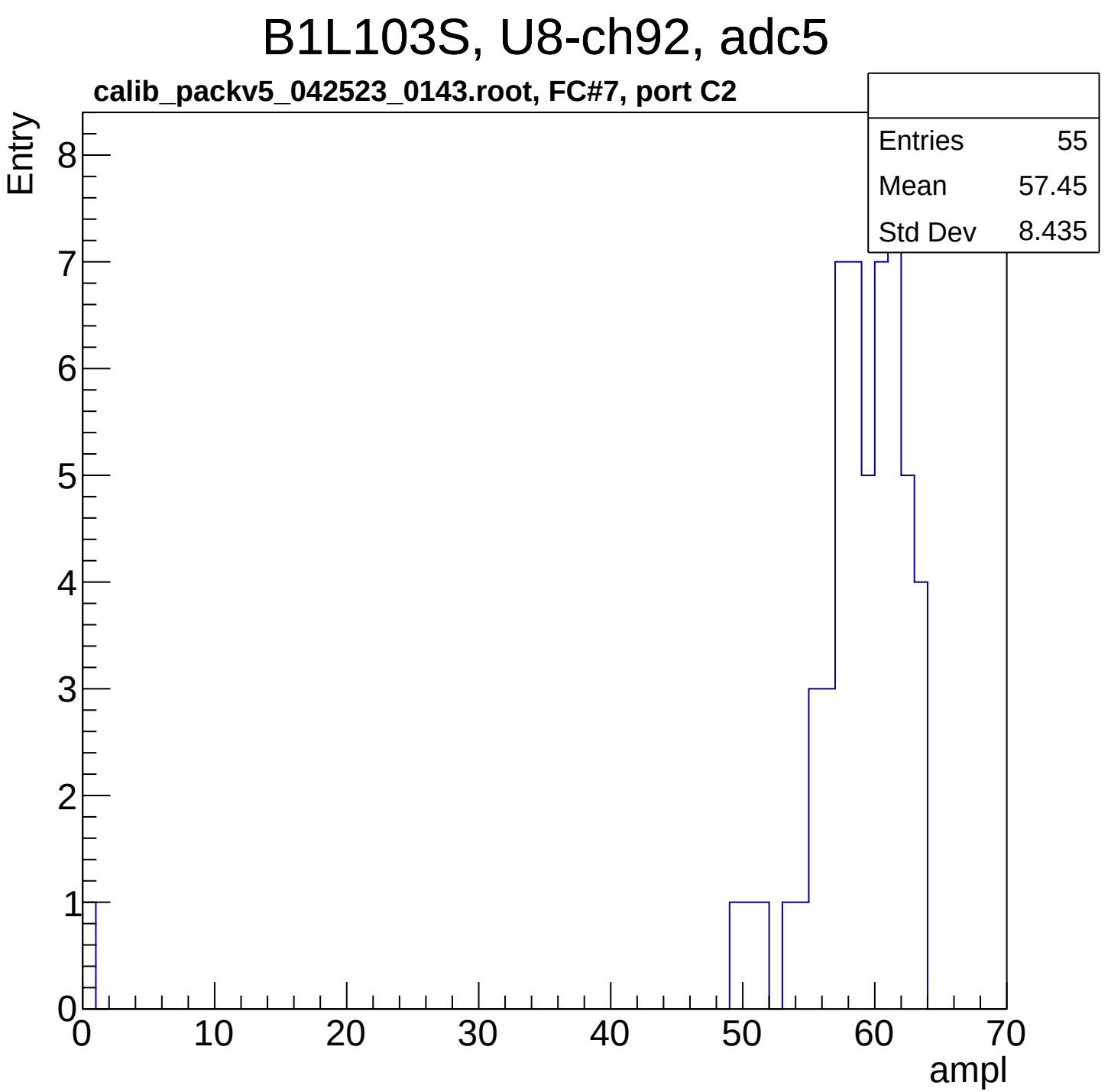

B1L103S, U8-ch92, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 28.38
Std Dev 5.976
Gaus mean : 29.5630
Gaus Width: 3.1126
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

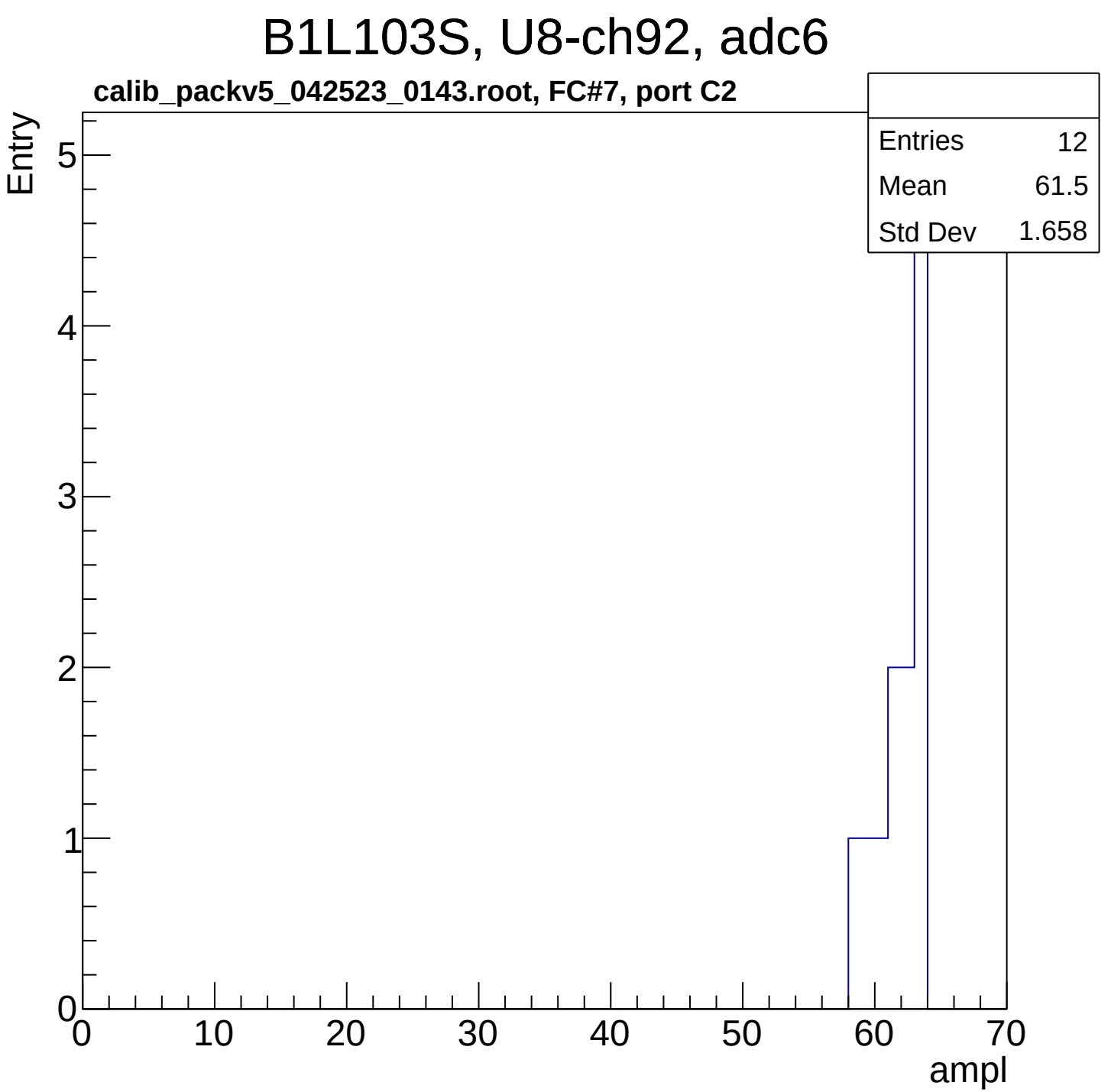

B1L103S, U8-ch92, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 36.05
Std Dev 3.629
Gaus mean : 36.0738
Gaus Width: 3.4085
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

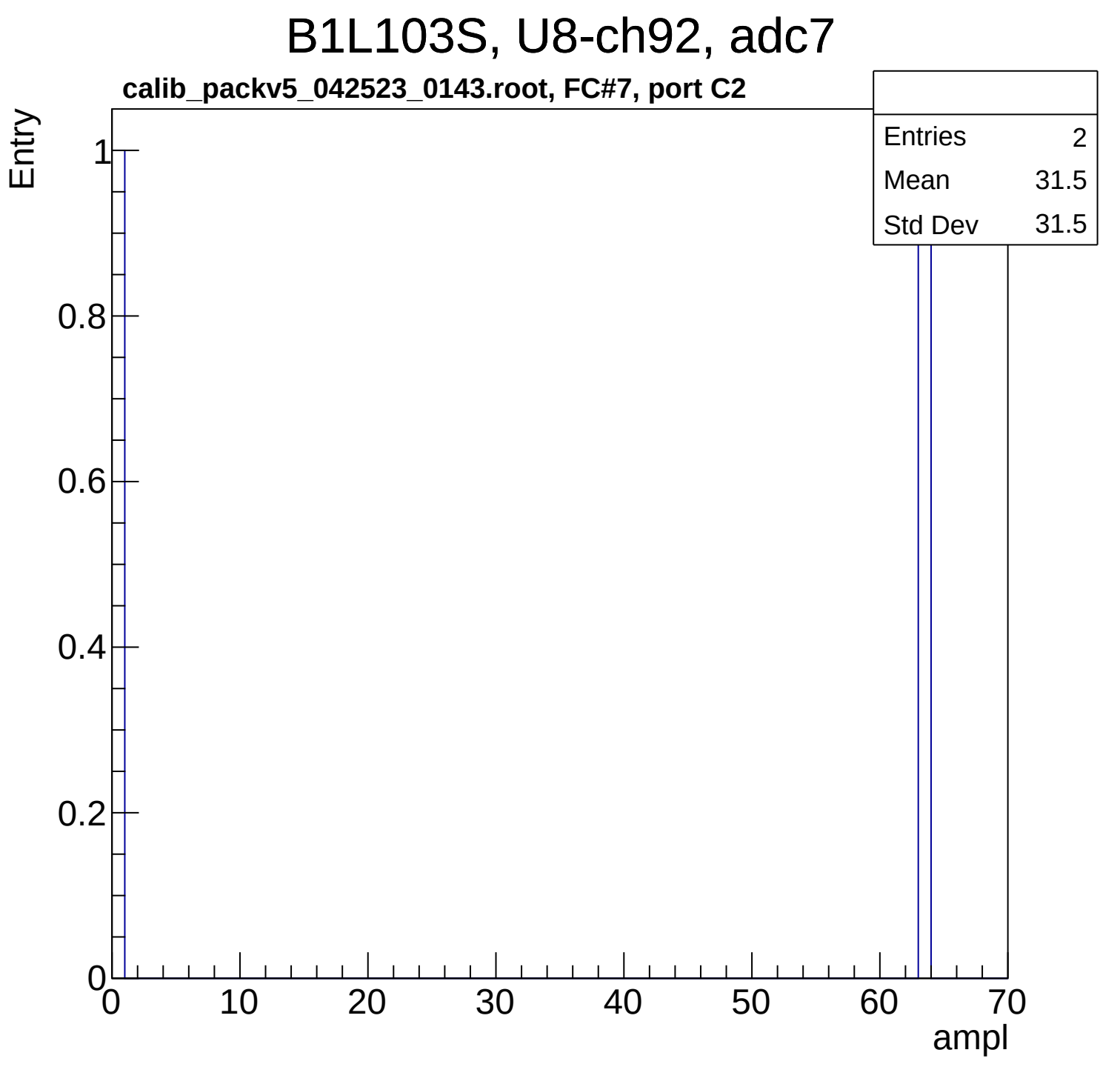

B1L103S, U8-ch92, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 41.61
Std Dev 3.769
Gaus mean : 42.8570
Gaus Width: 5.1466
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

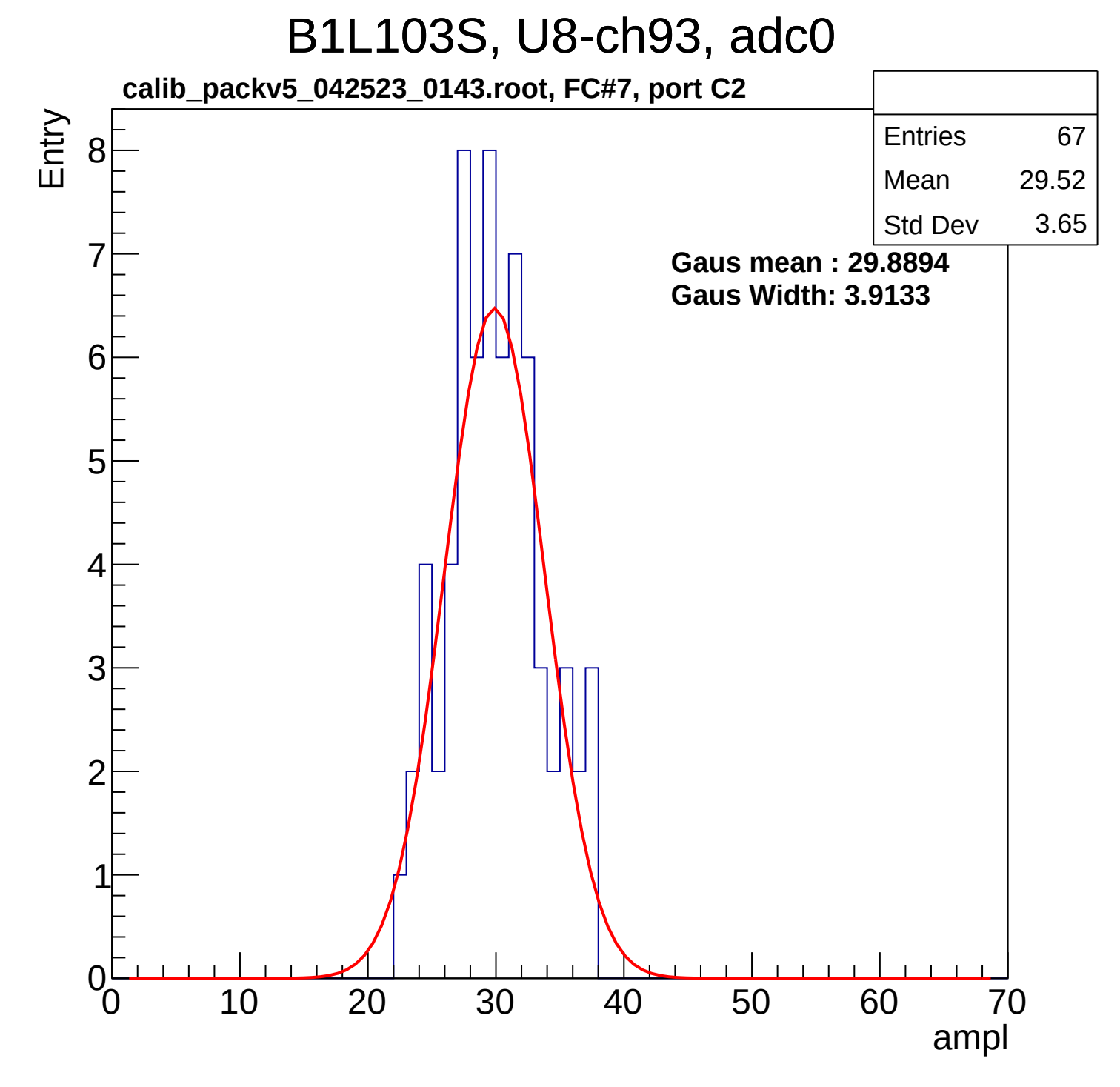

B1L103S, U8-ch92, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 47.92
Std Dev 3.926
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

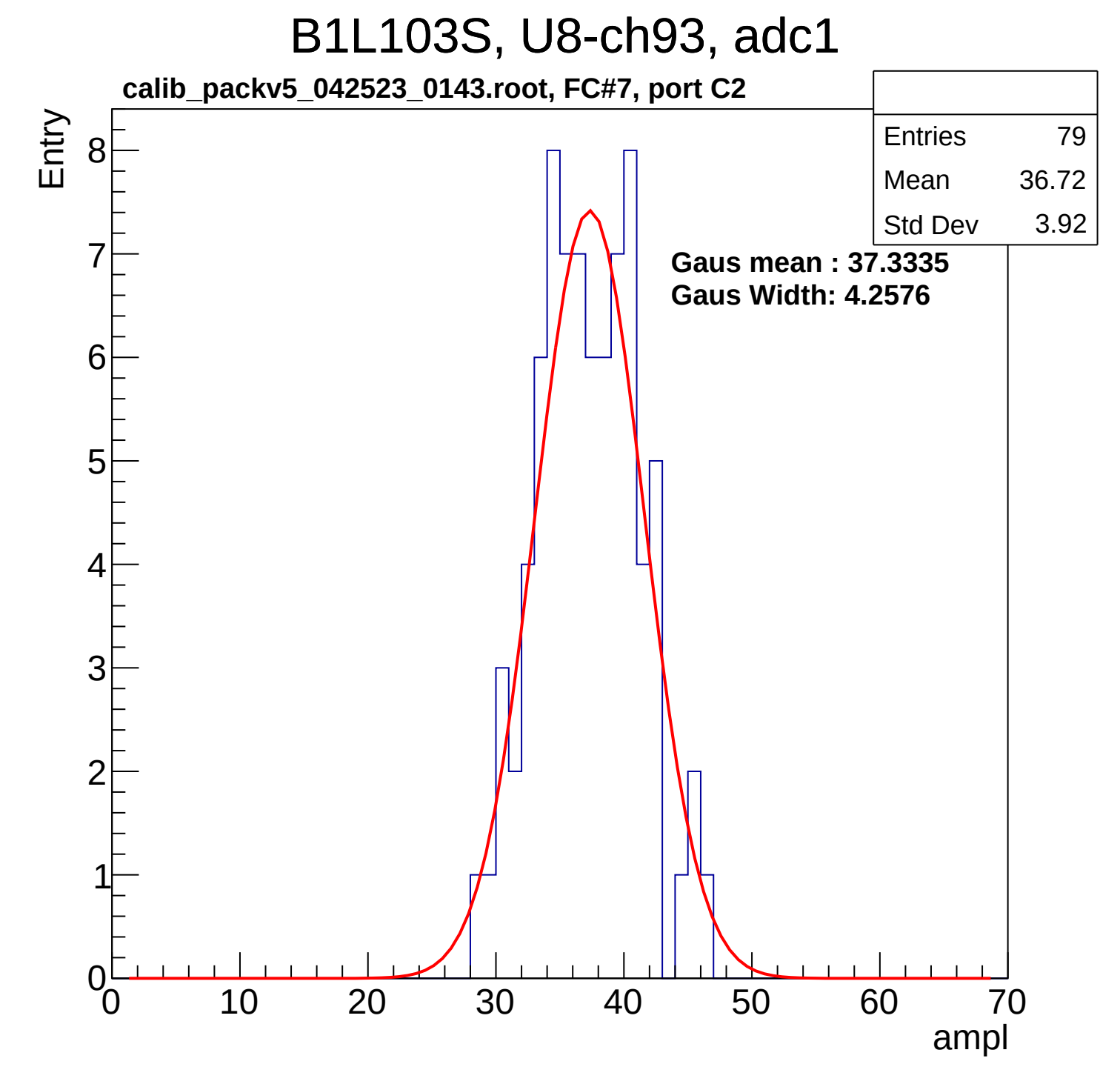

B1L103S, U8-ch92, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 54.65
Std Dev 3.596
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

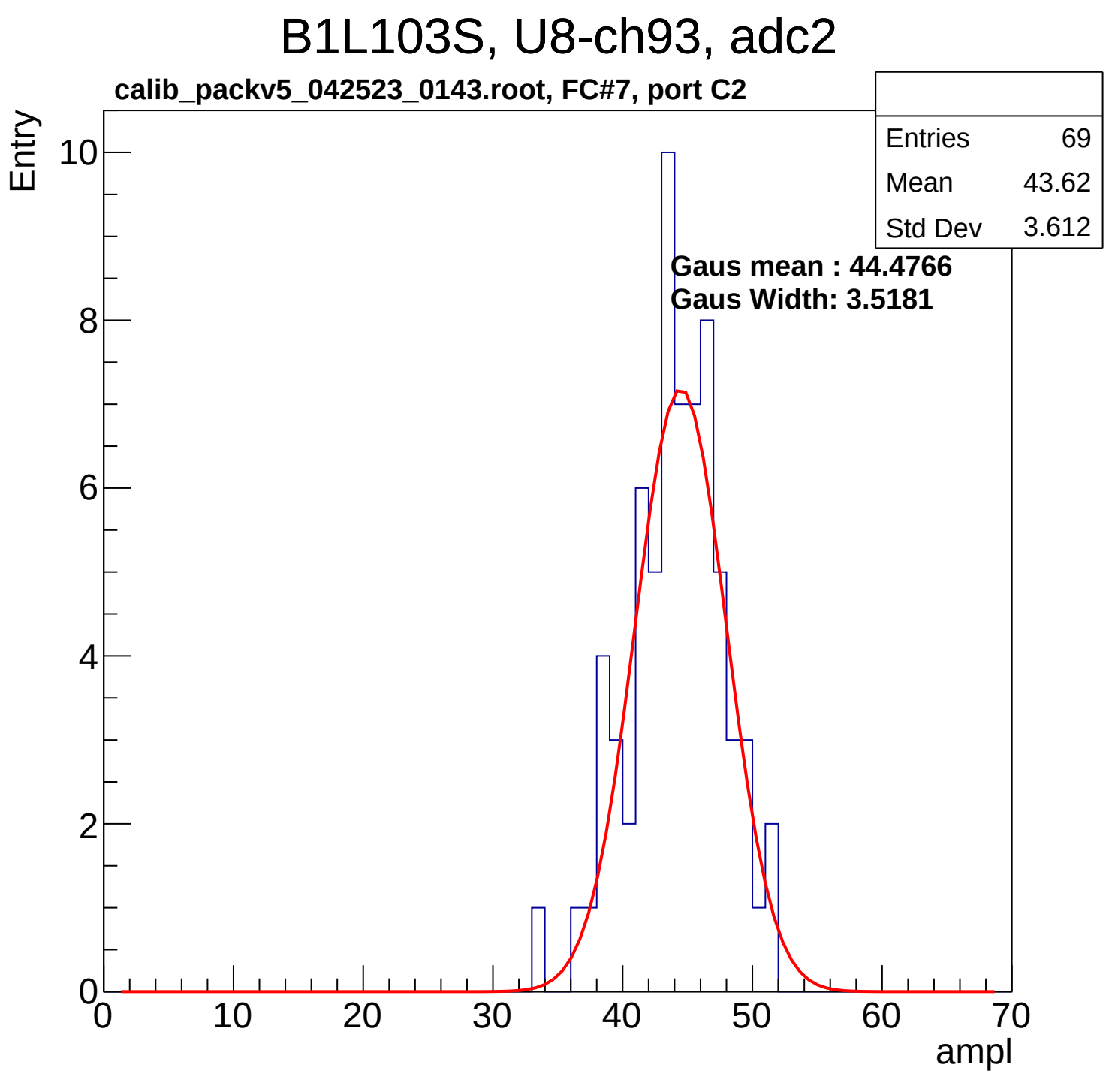

B1L103S, U8-ch92, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 57.45
Std Dev 8.435
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

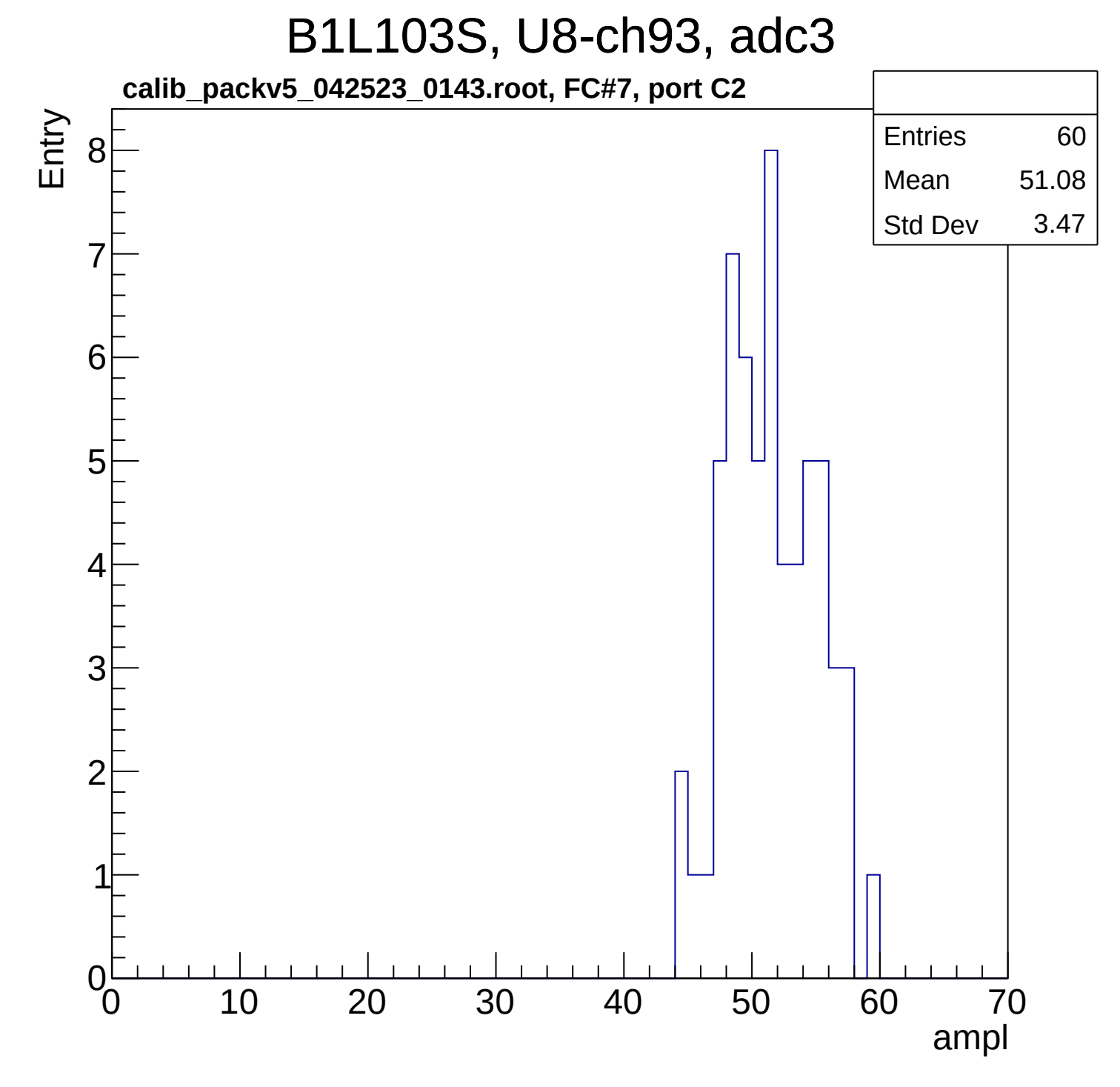

B1L103S, U8-ch92, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 12
Mean 61.5
Std Dev 1.658
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

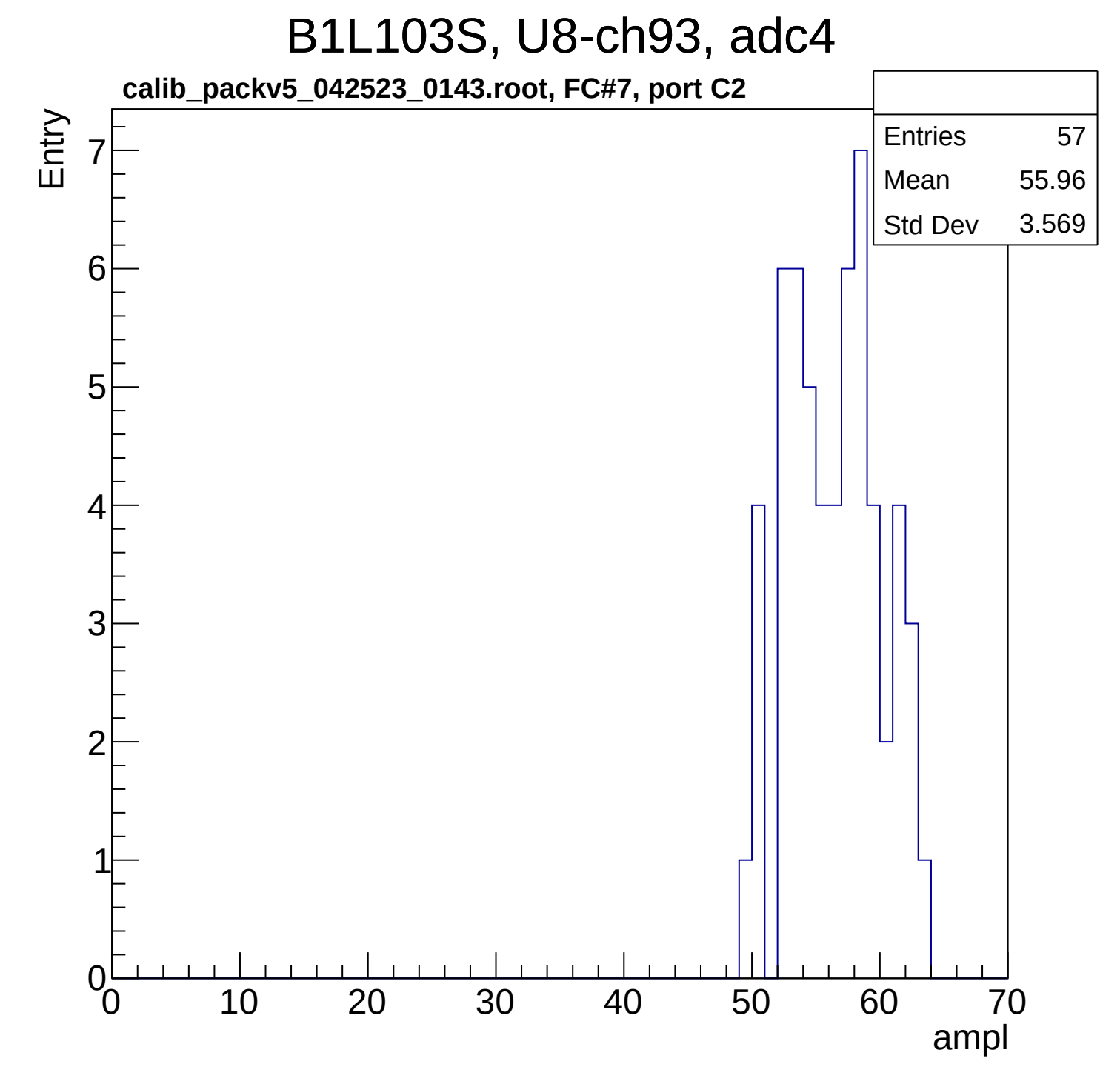

B1L103S, U8-ch92, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

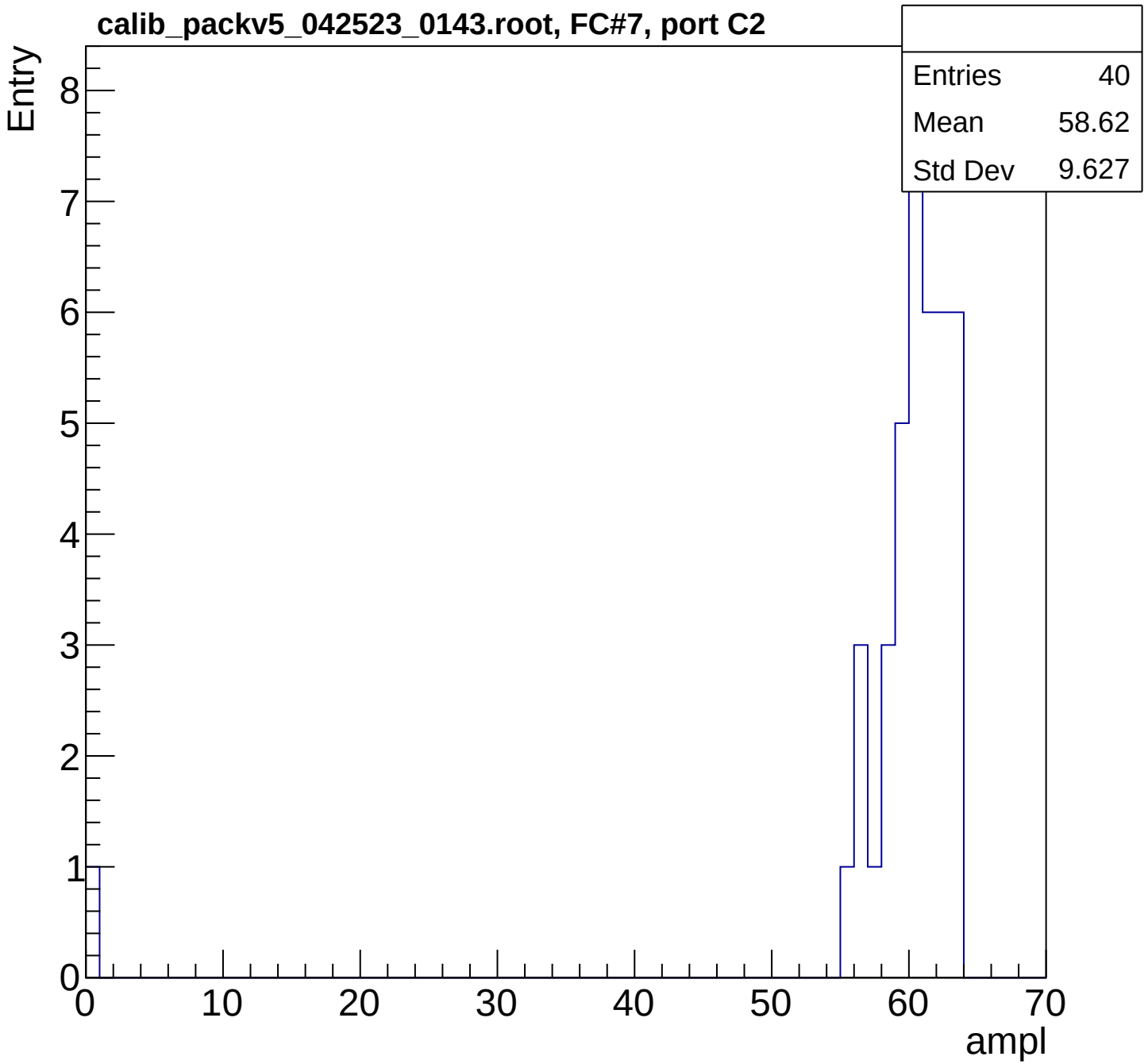

B1L103S, U8-ch93, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 29.52
Std Dev 3.65
Gaus mean : 29.8894
Gaus Width: 3.9133
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

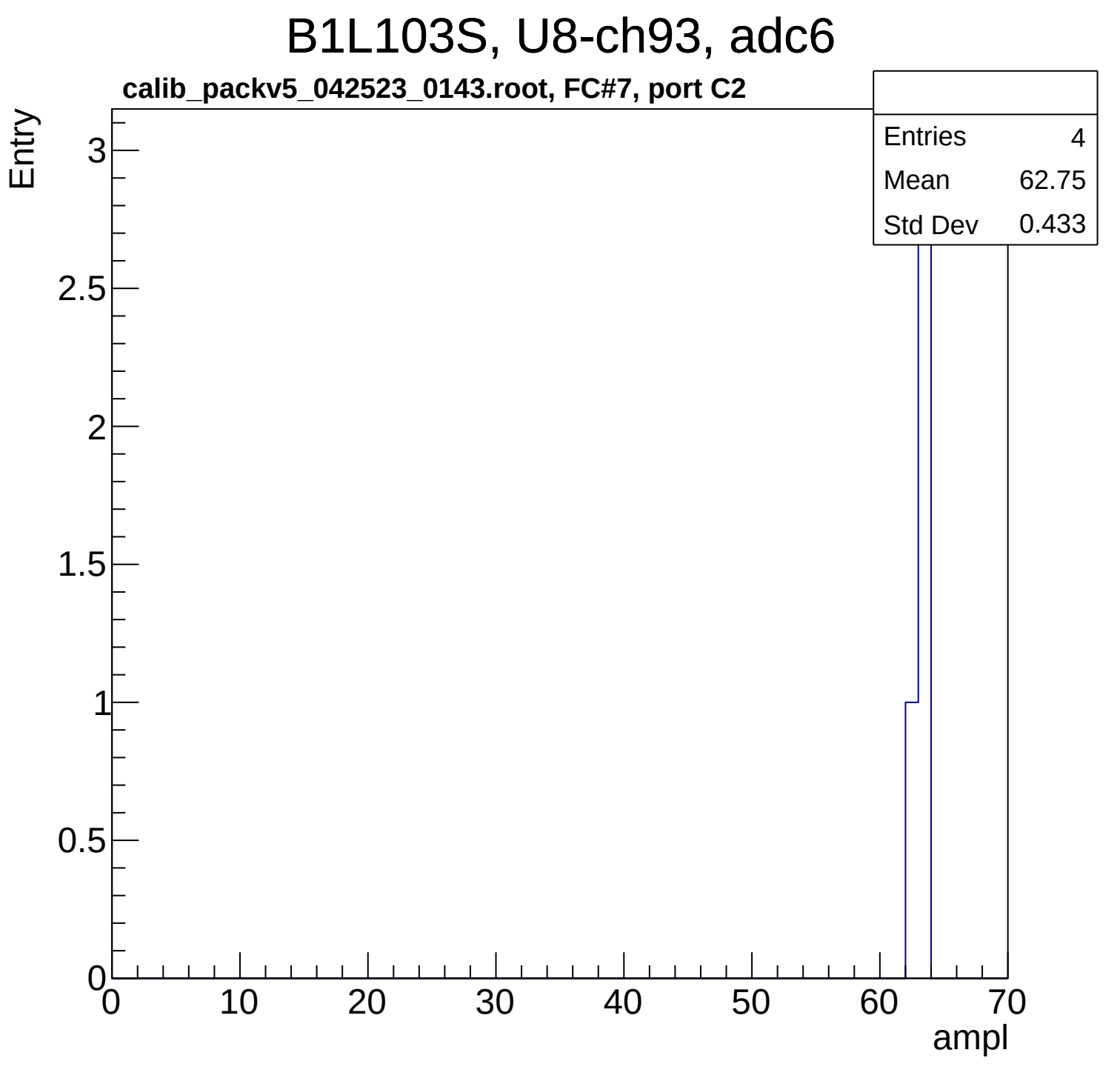

B1L103S, U8-ch93, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 79
Mean 36.72
Std Dev 3.92
Gaus mean : 37.3335
Gaus Width: 4.2576
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

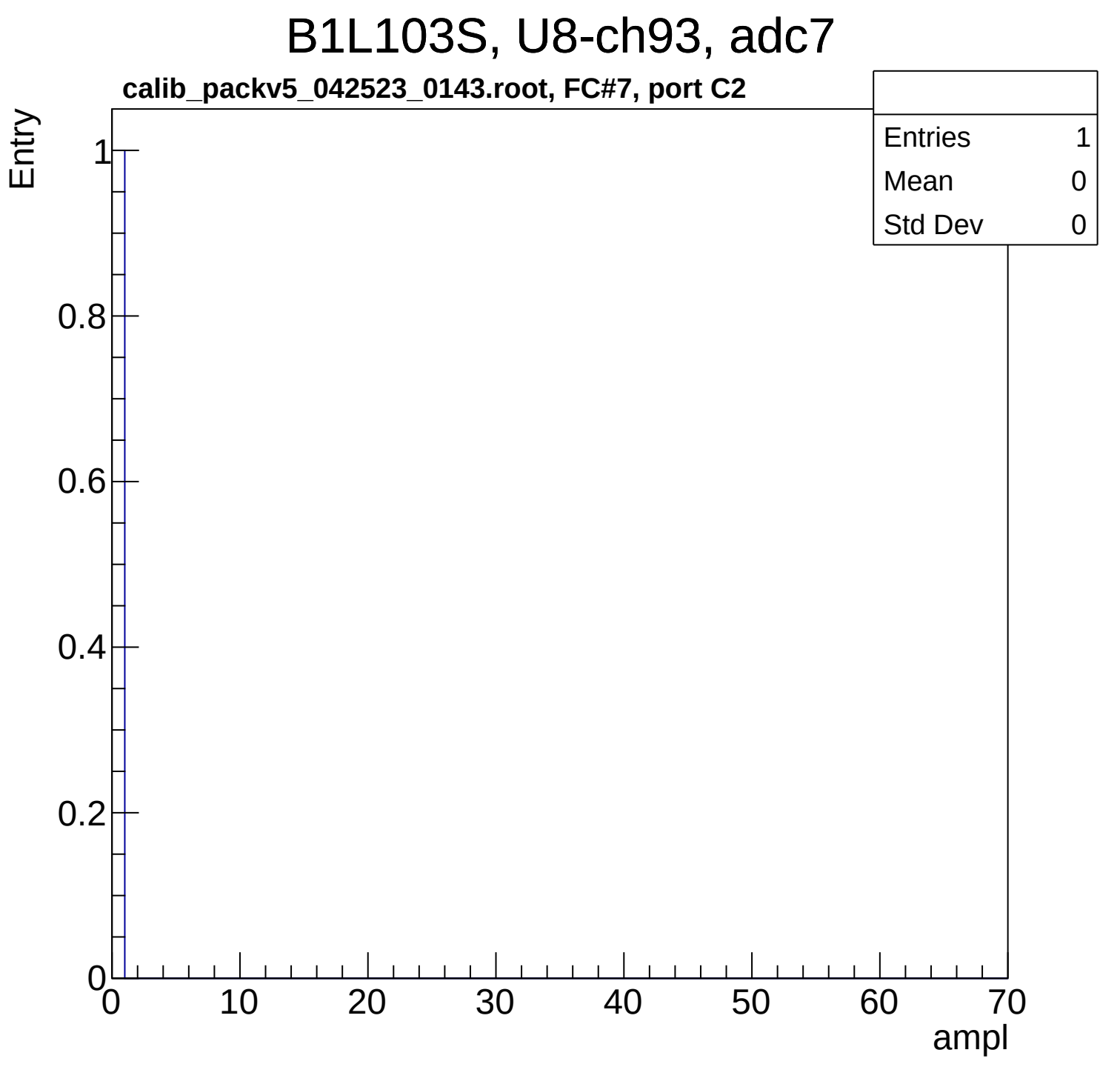

B1L103S, U8-ch93, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 43.62
Std Dev 3.612
Gaus mean : 44.4766
Gaus Width: 3.5181
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

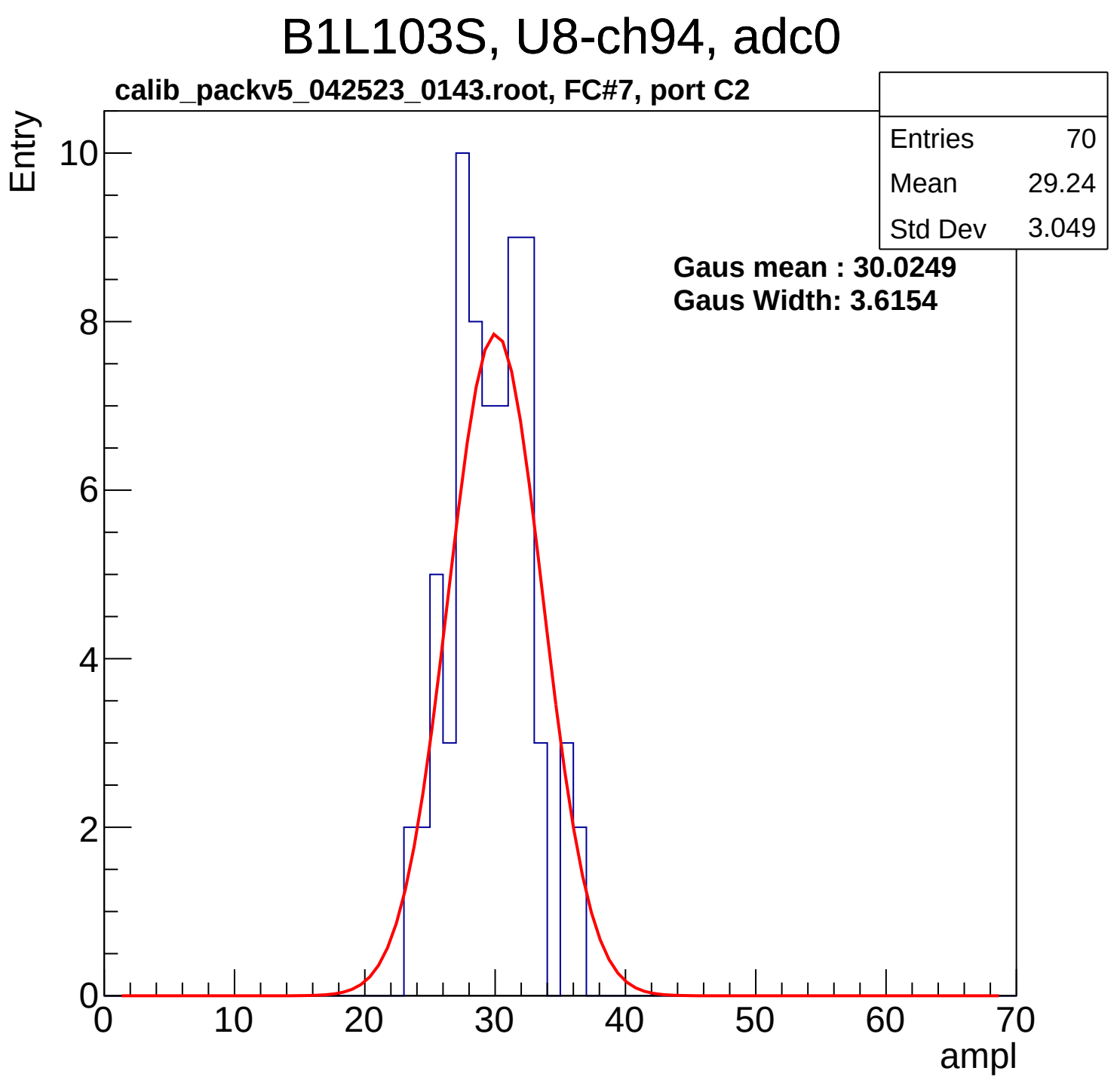

B1L103S, U8-ch93, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 51.08
Std Dev 3.47
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

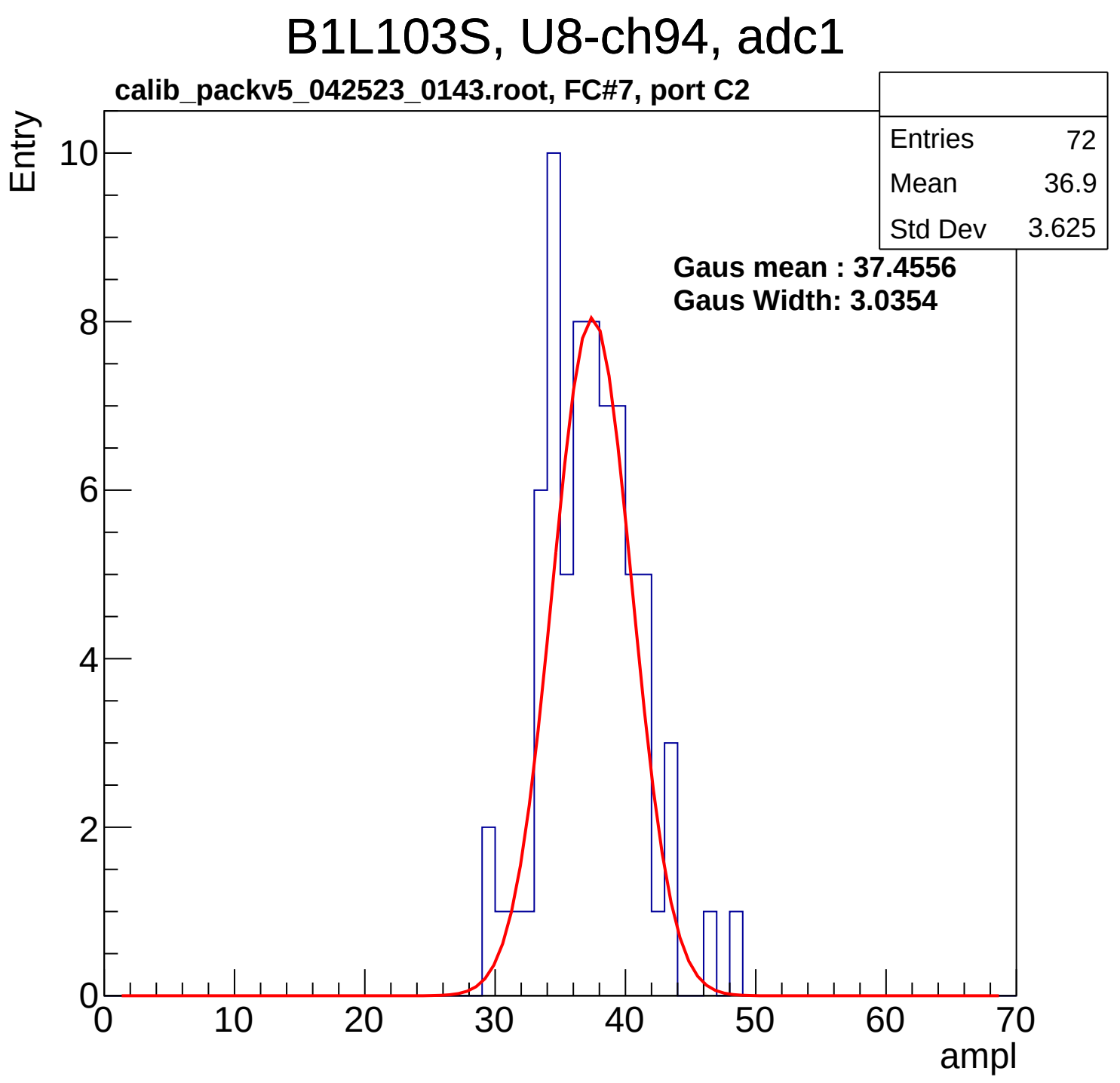

B1L103S, U8-ch93, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 55.96
Std Dev 3.569
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

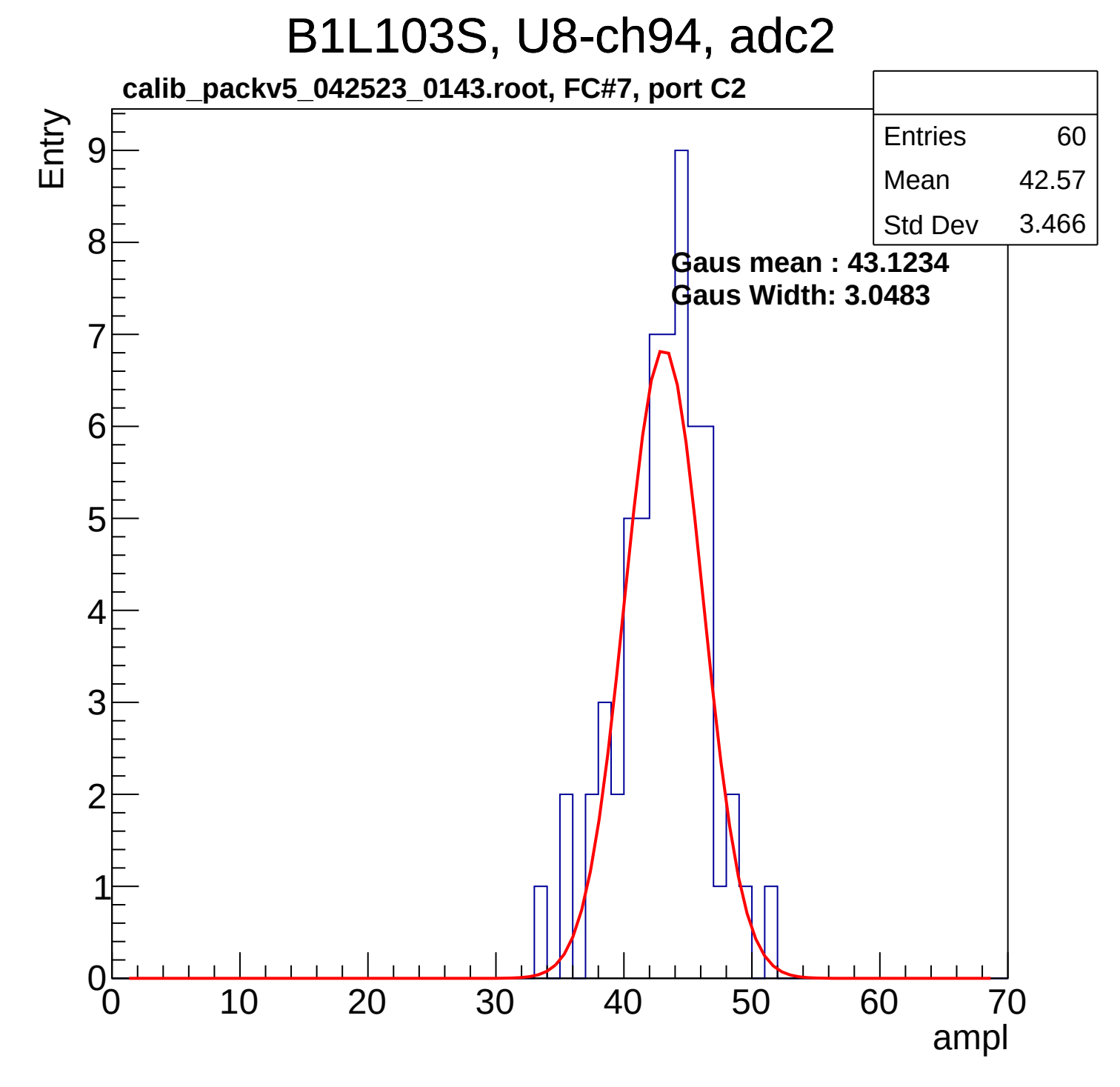

B1L103S, U8-ch93, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 40
Mean 58.62
Std Dev 9.627
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

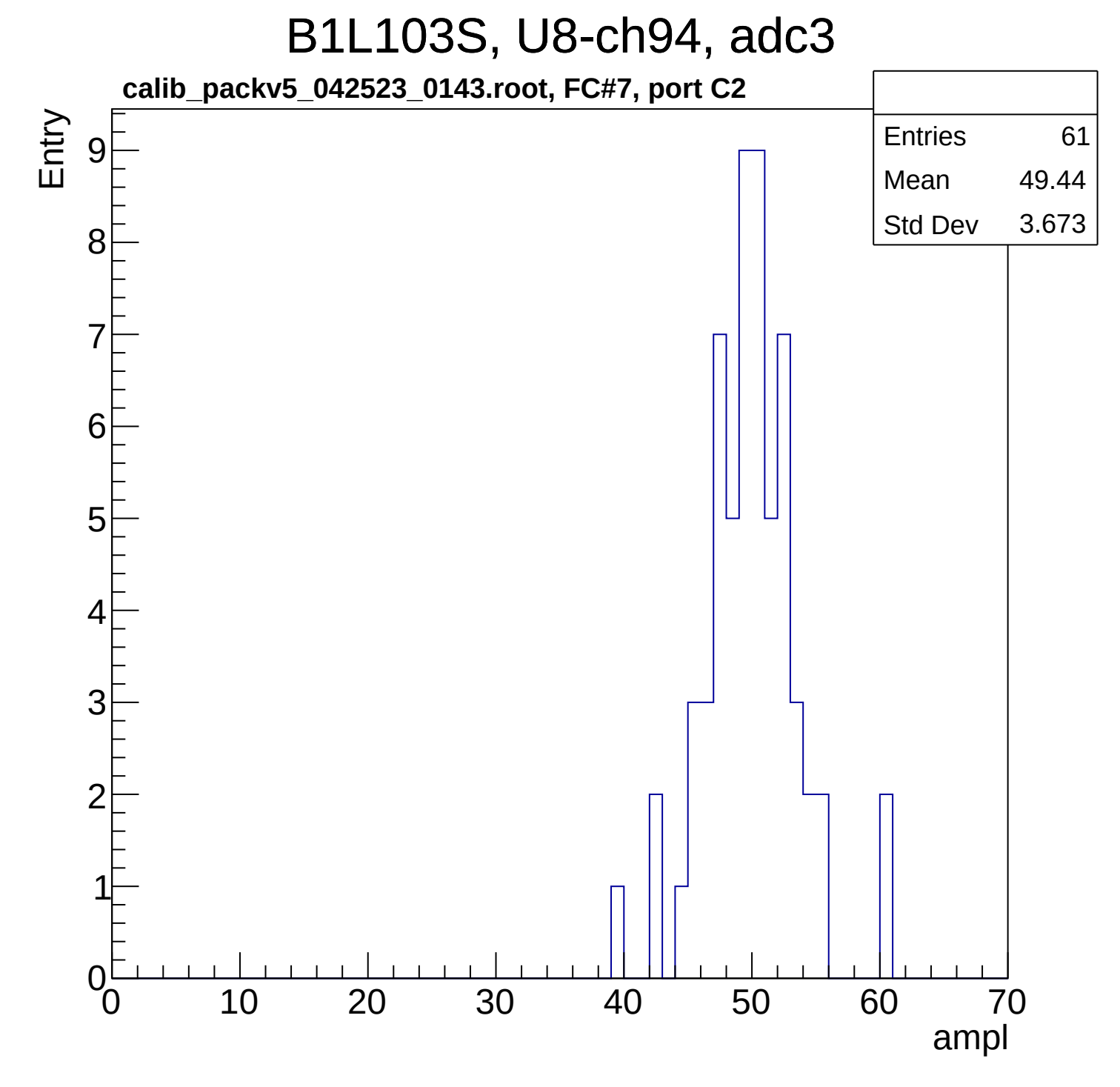

B1L103S, U8-ch93, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 62.75
Std Dev 0.433
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

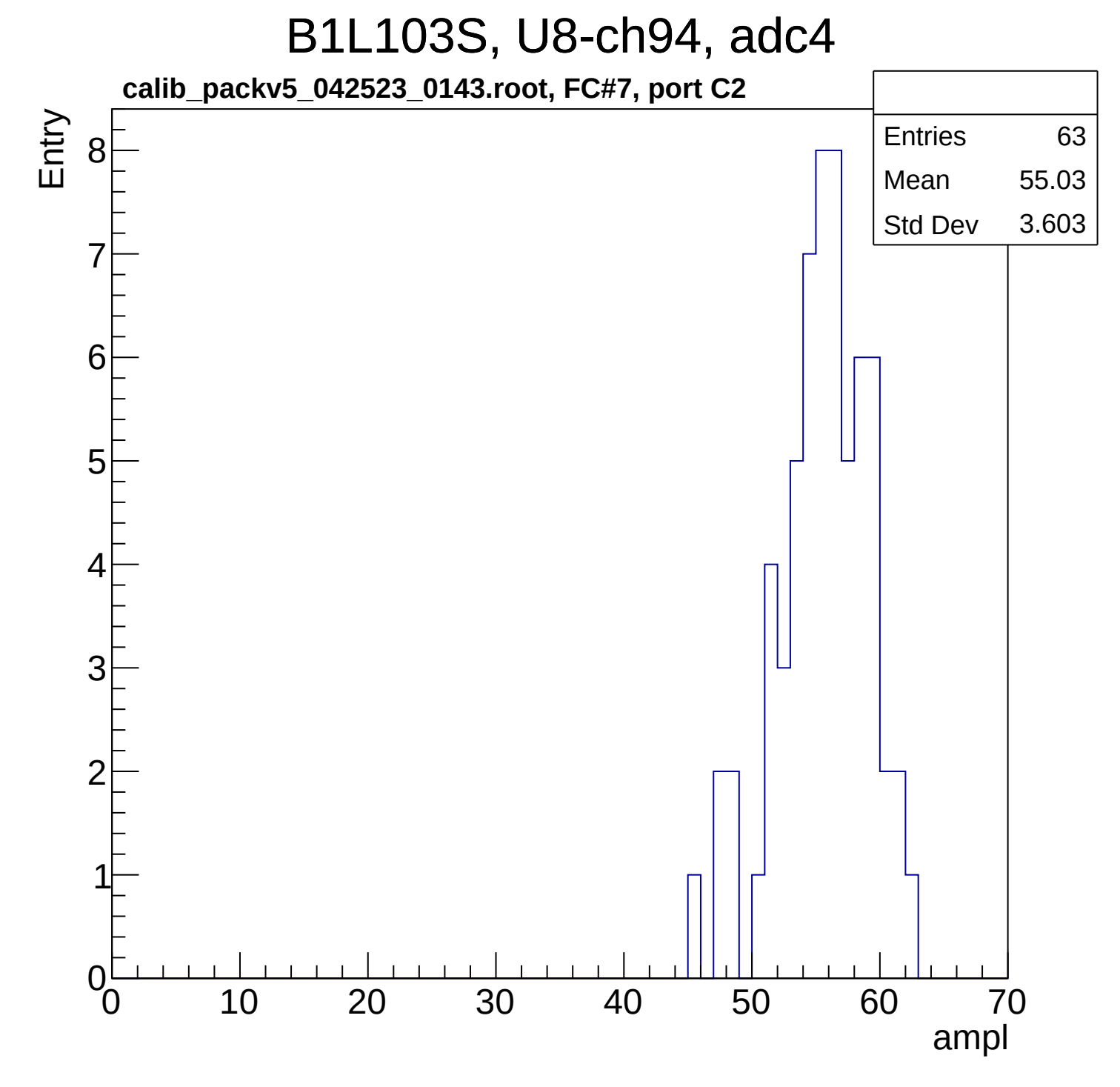

B1L103S, U8-ch93, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

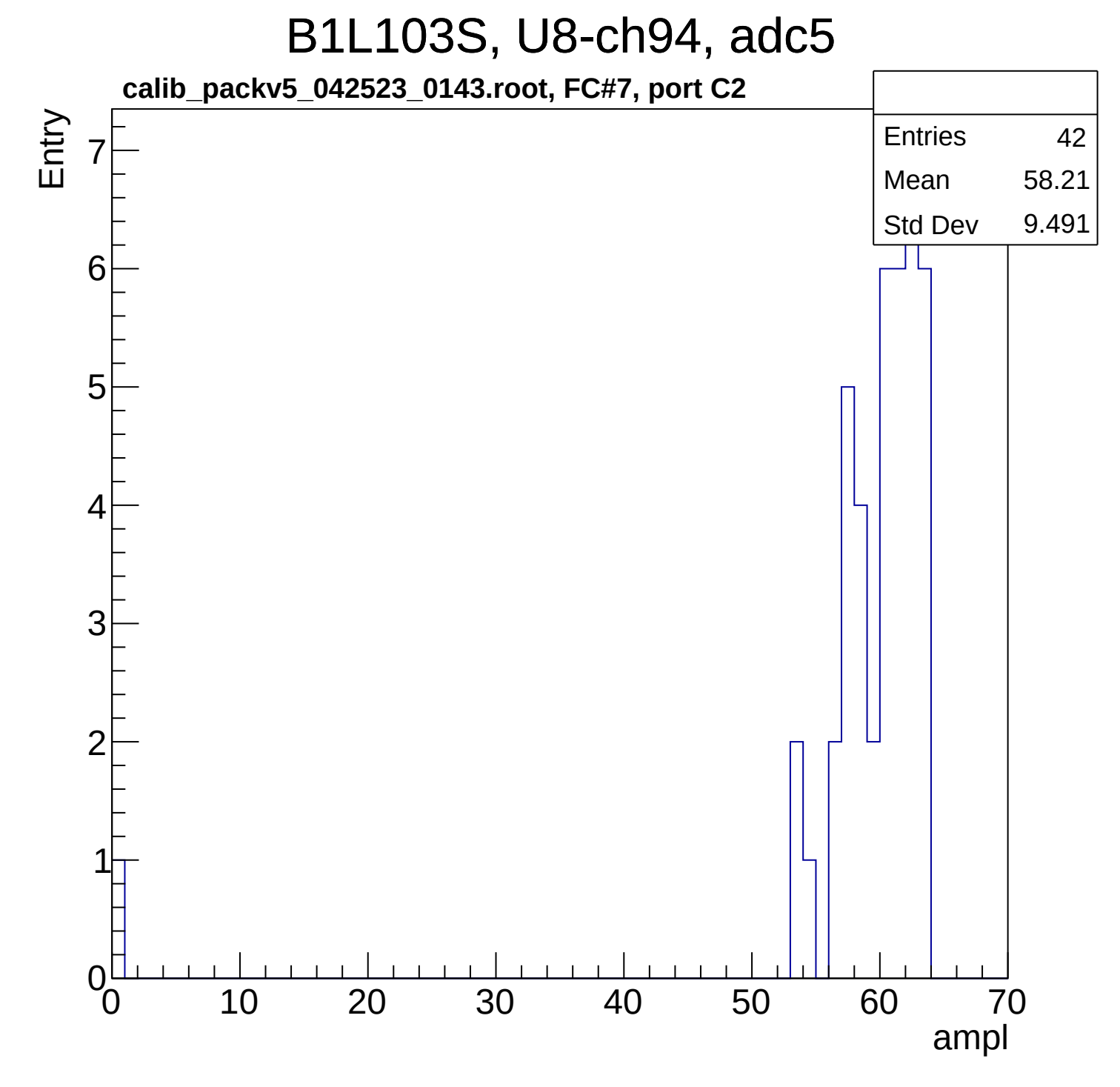

B1L103S, U8-ch94, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 29.24
Std Dev 3.049
Gaus mean : 30.0249
Gaus Width: 3.6154
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

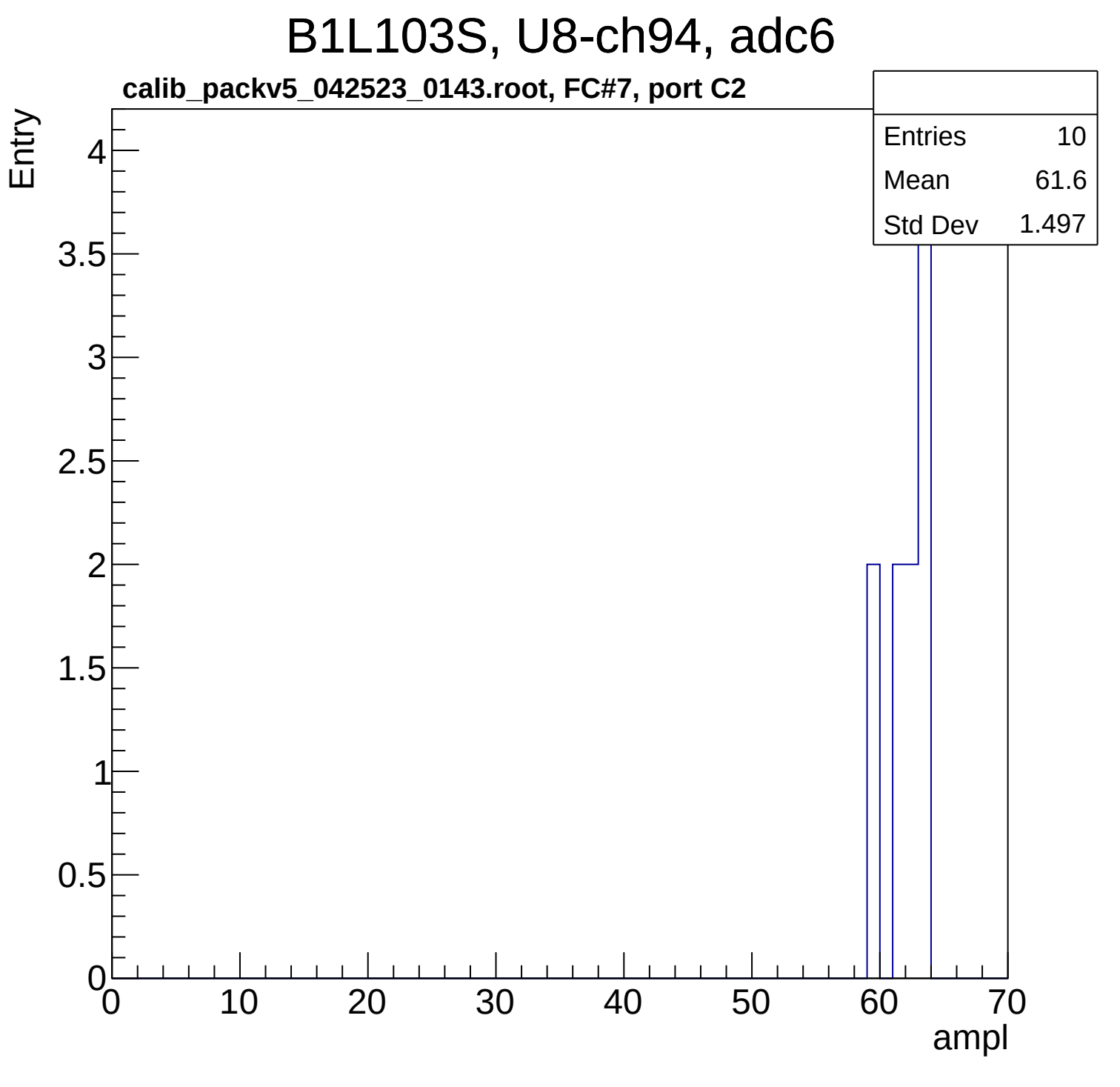

B1L103S, U8-ch94, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 36.9
Std Dev 3.625
Gaus mean : 37.4556
Gaus Width: 3.0354
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

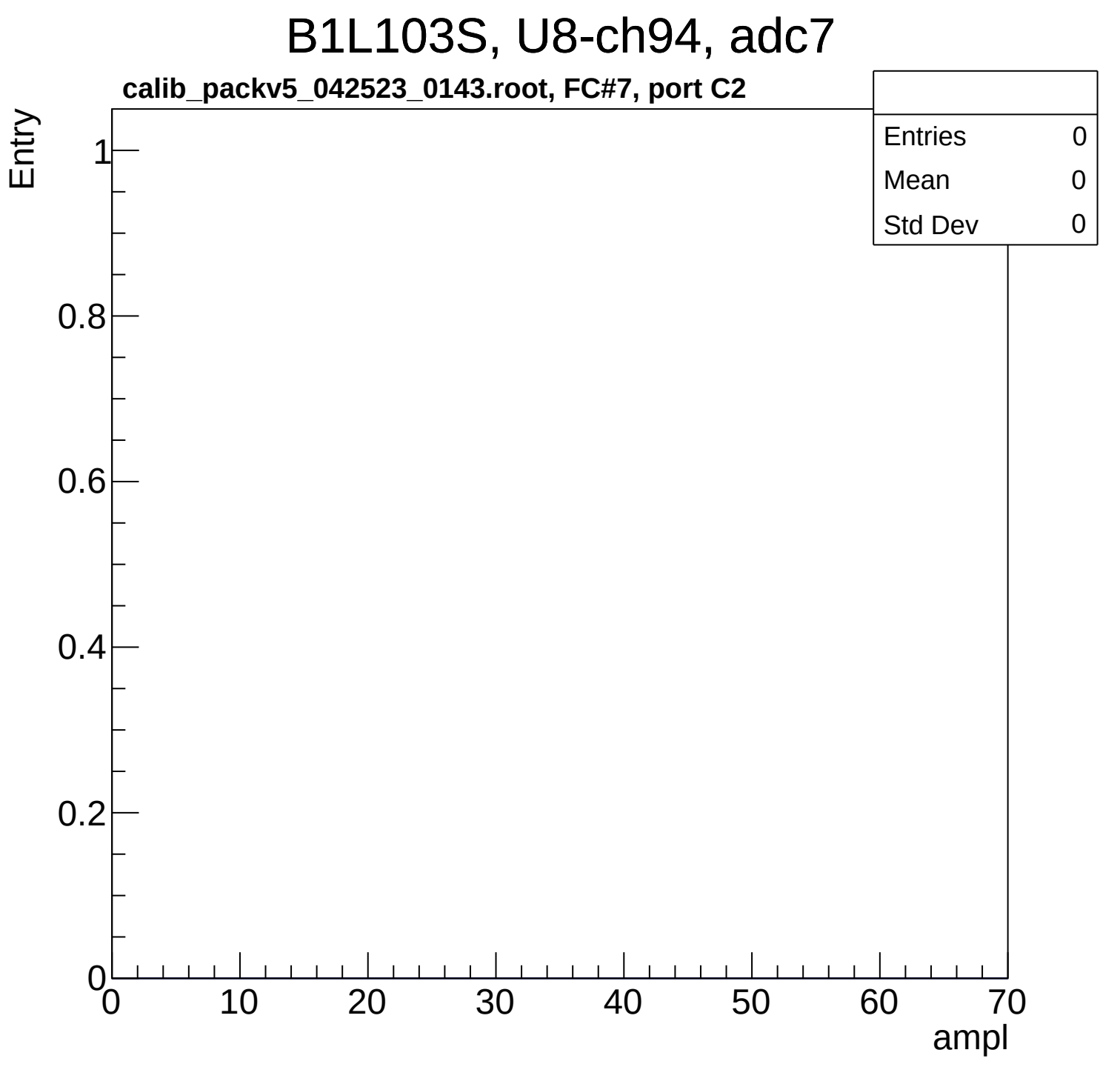

B1L103S, U8-ch94, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 42.57
Std Dev 3.466
Gaus mean : 43.1234
Gaus Width: 3.0483
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

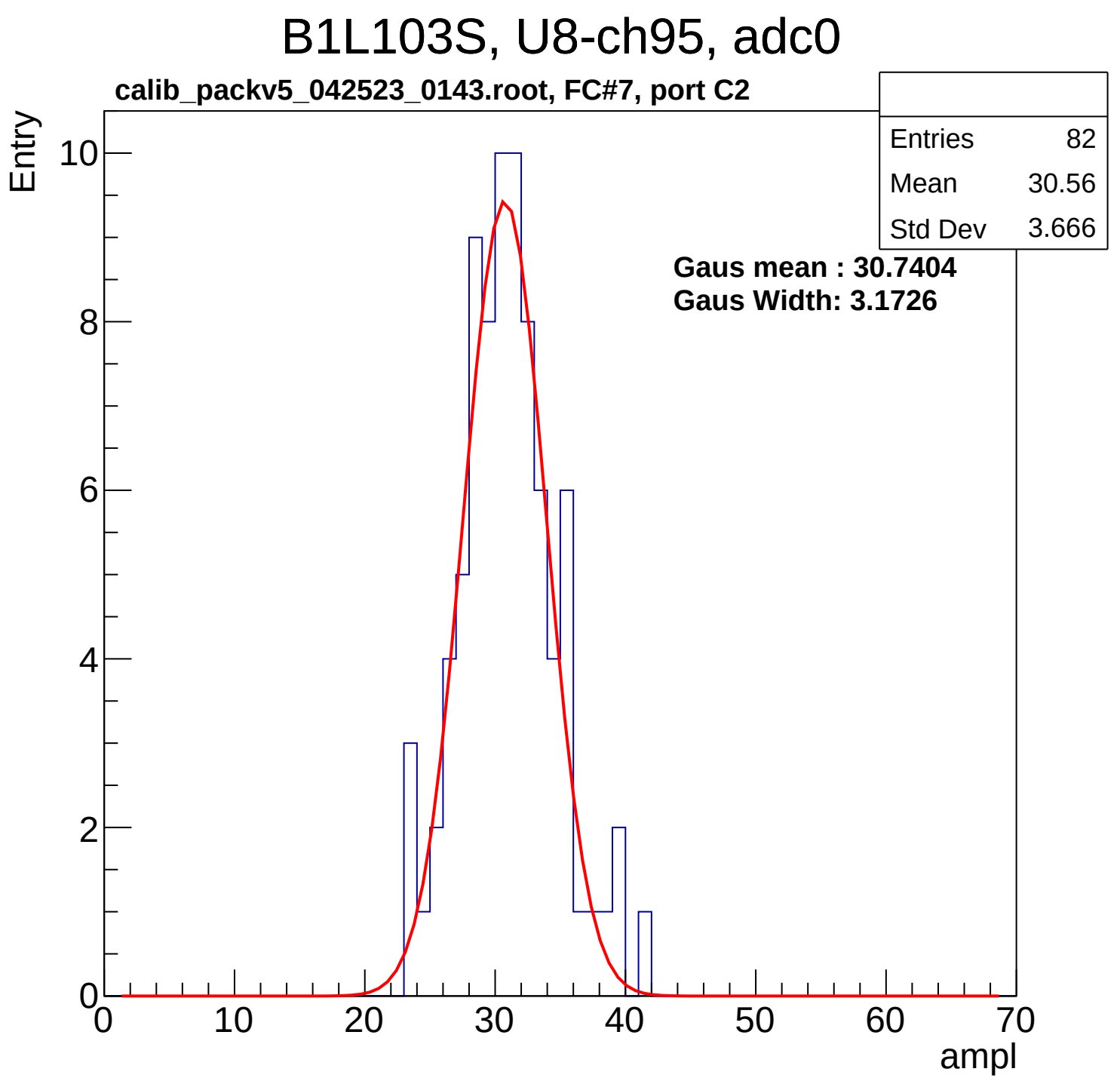

B1L103S, U8-ch94, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 49.44
Std Dev 3.673
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

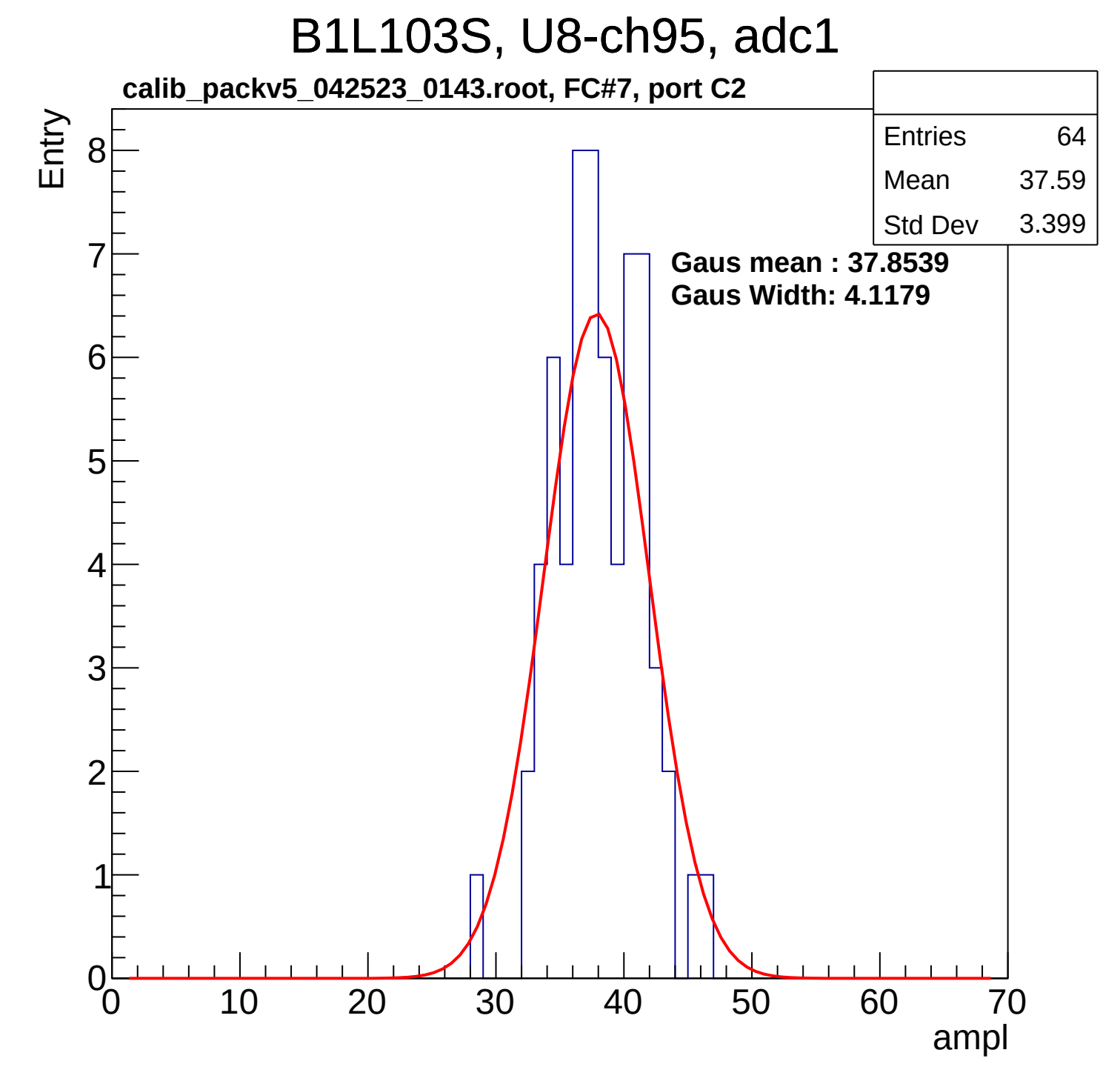

B1L103S, U8-ch94, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 55.03
Std Dev 3.603
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

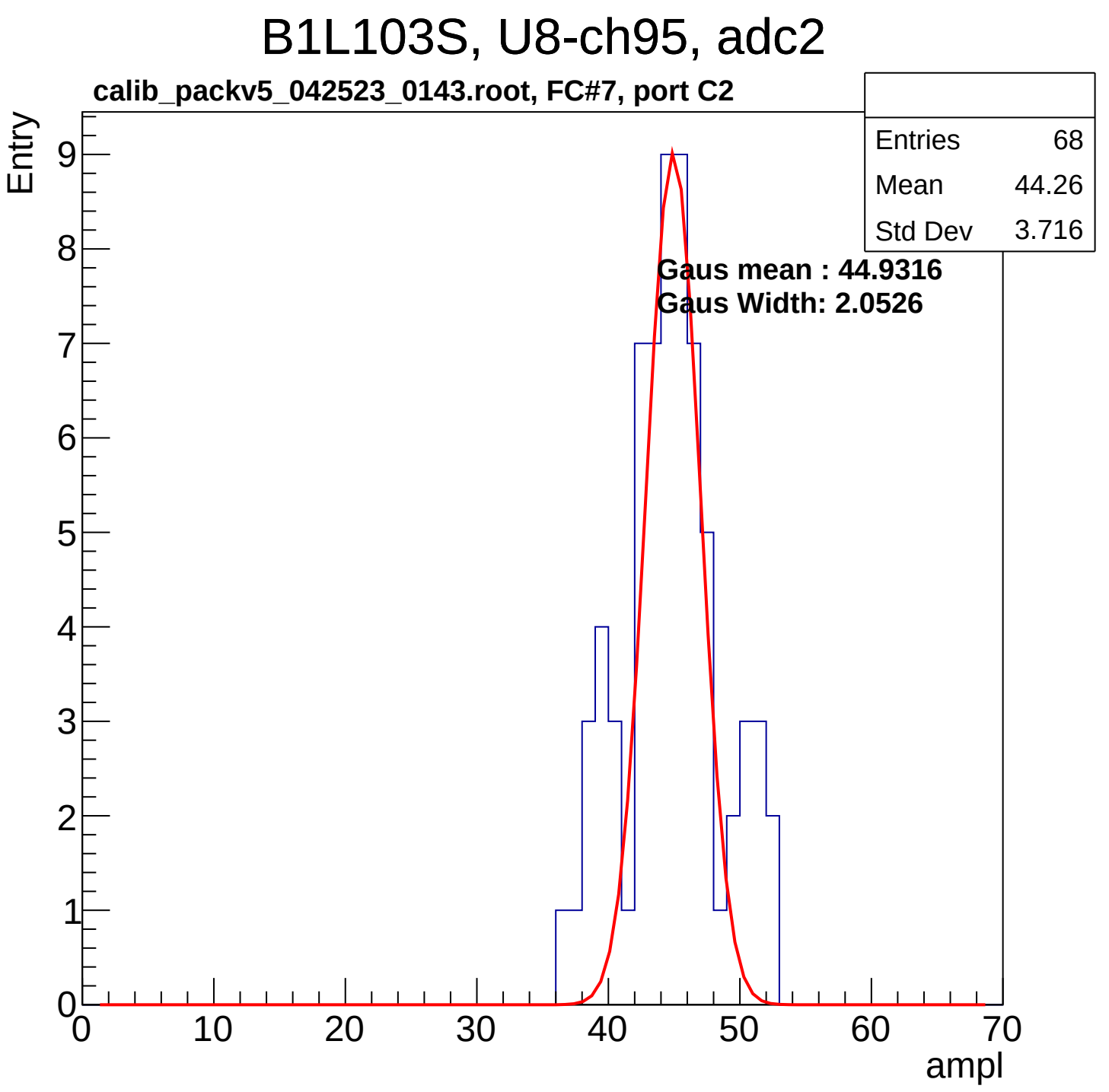

B1L103S, U8-ch94, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 42
Mean 58.21
Std Dev 9.491
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

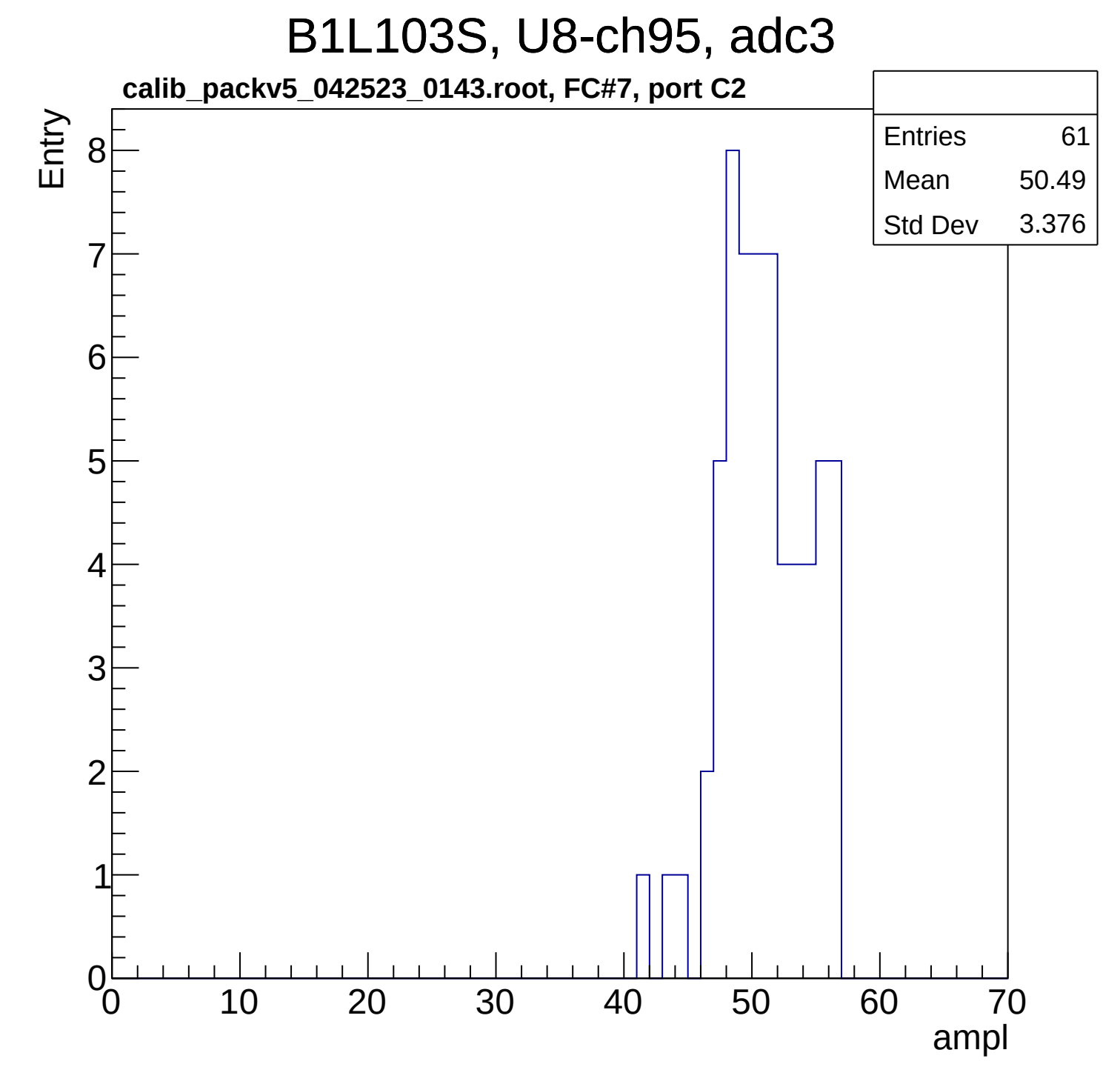

B1L103S, U8-ch94, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 10
Mean 61.6
Std Dev 1.497
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

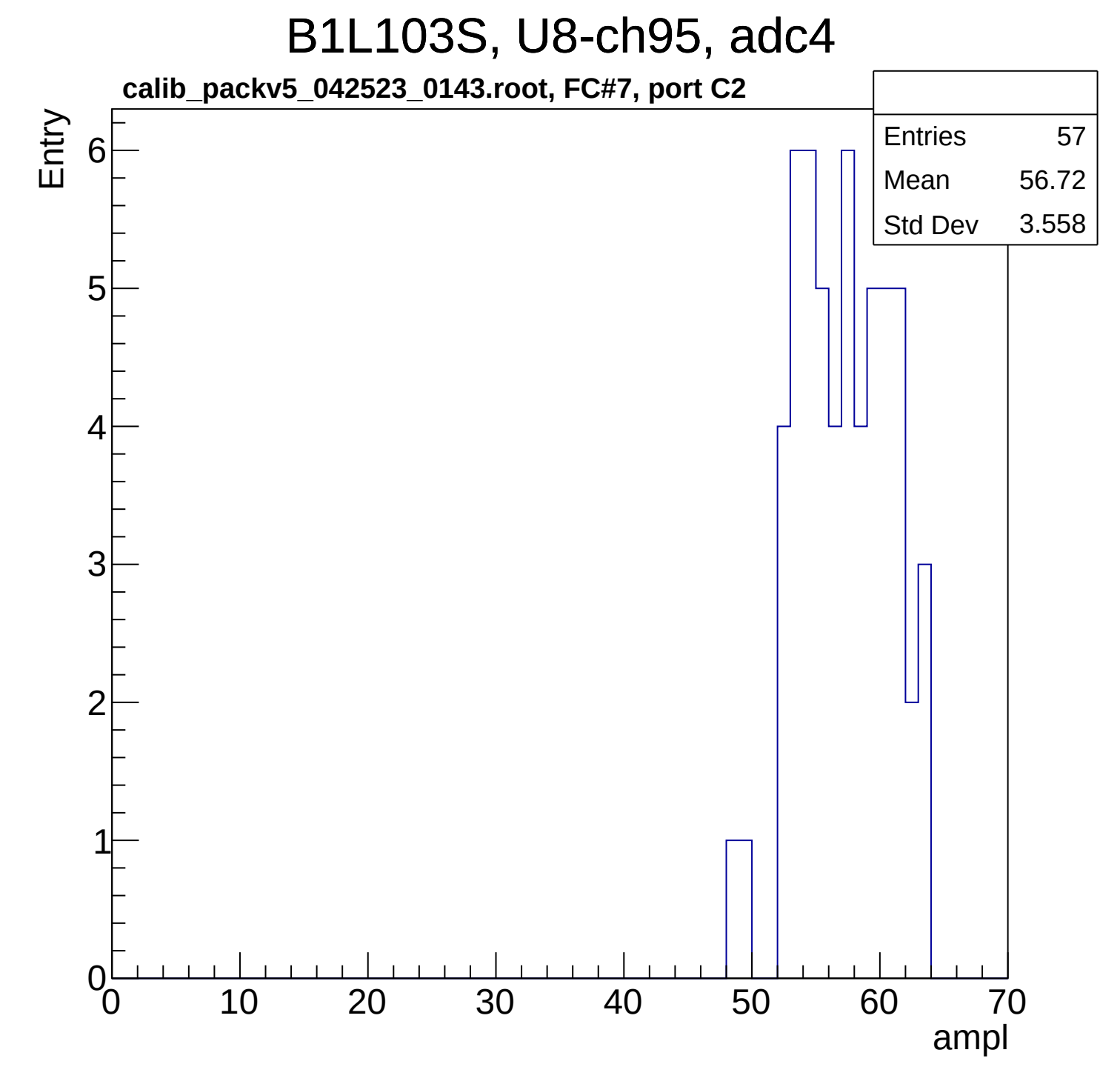

B1L103S, U8-ch94, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

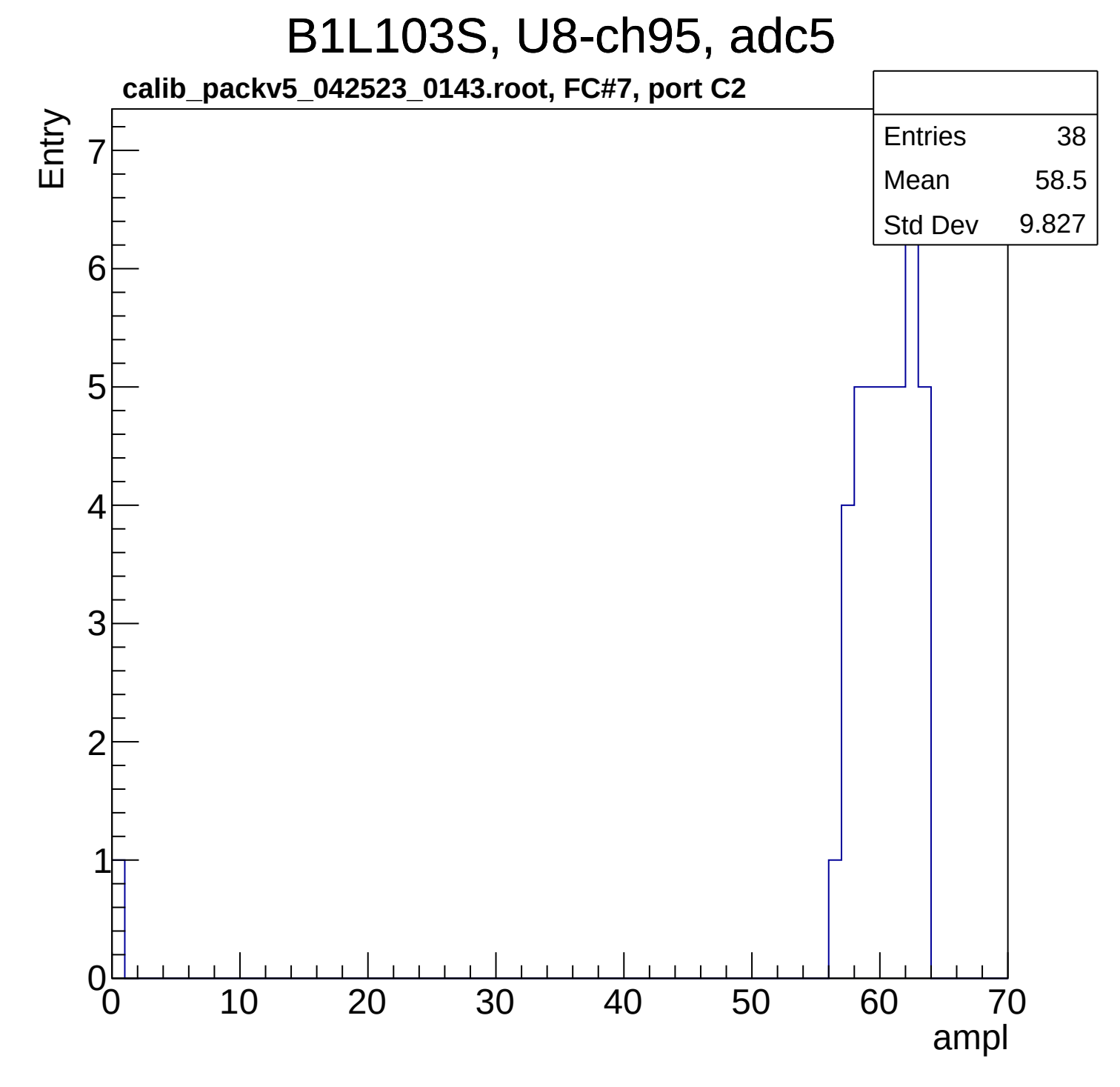

B1L103S, U8-ch95, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 82
Mean 30.56
Std Dev 3.666
Gaus mean : 30.7404
Gaus Width: 3.1726
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

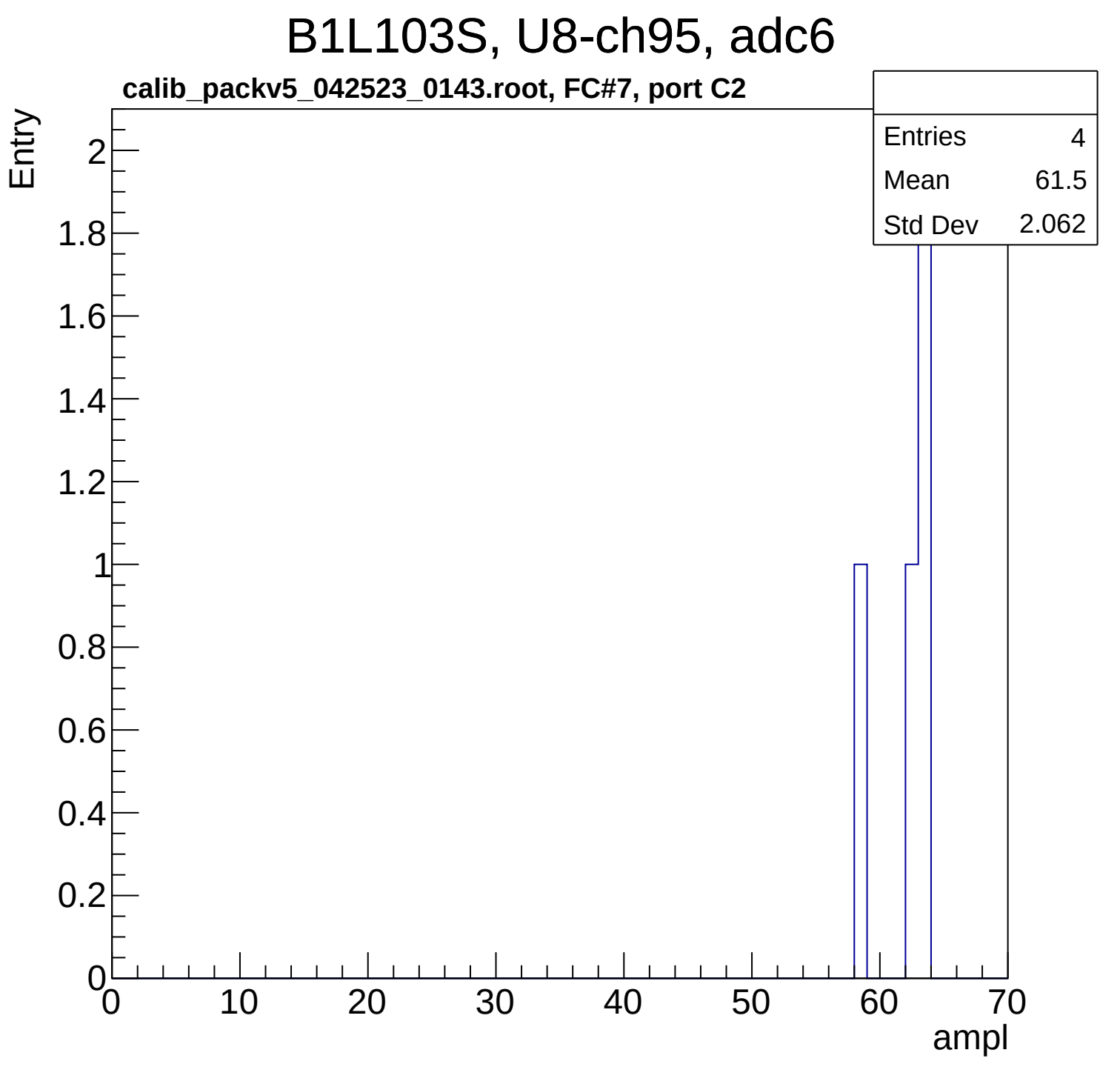

B1L103S, U8-ch95, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 37.59
Std Dev 3.399
Gaus mean : 37.8539
Gaus Width: 4.1179
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

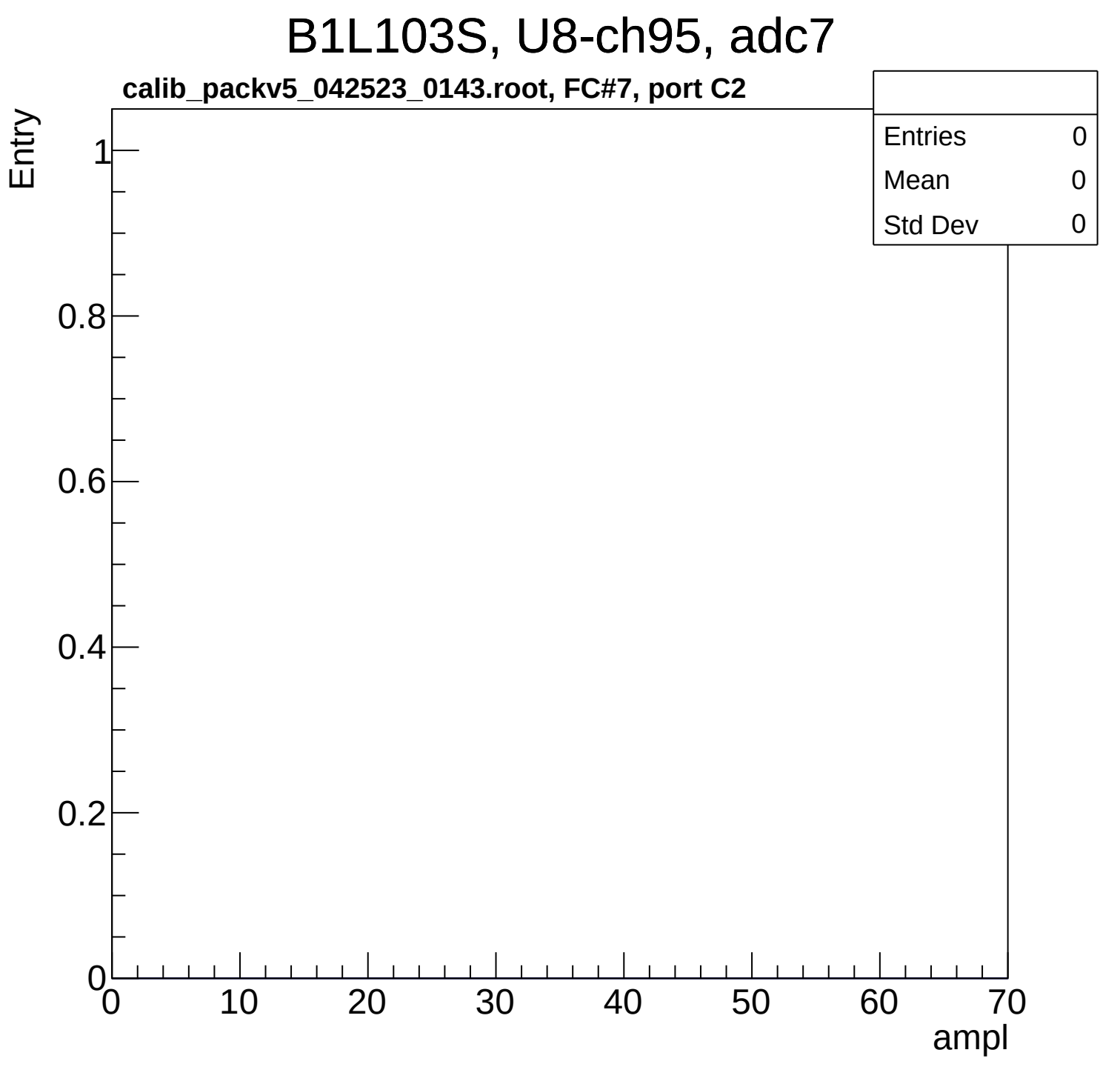

B1L103S, U8-ch95, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 44.26
Std Dev 3.716
Gaus mean : 44.9316
Gaus Width: 2.0526
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

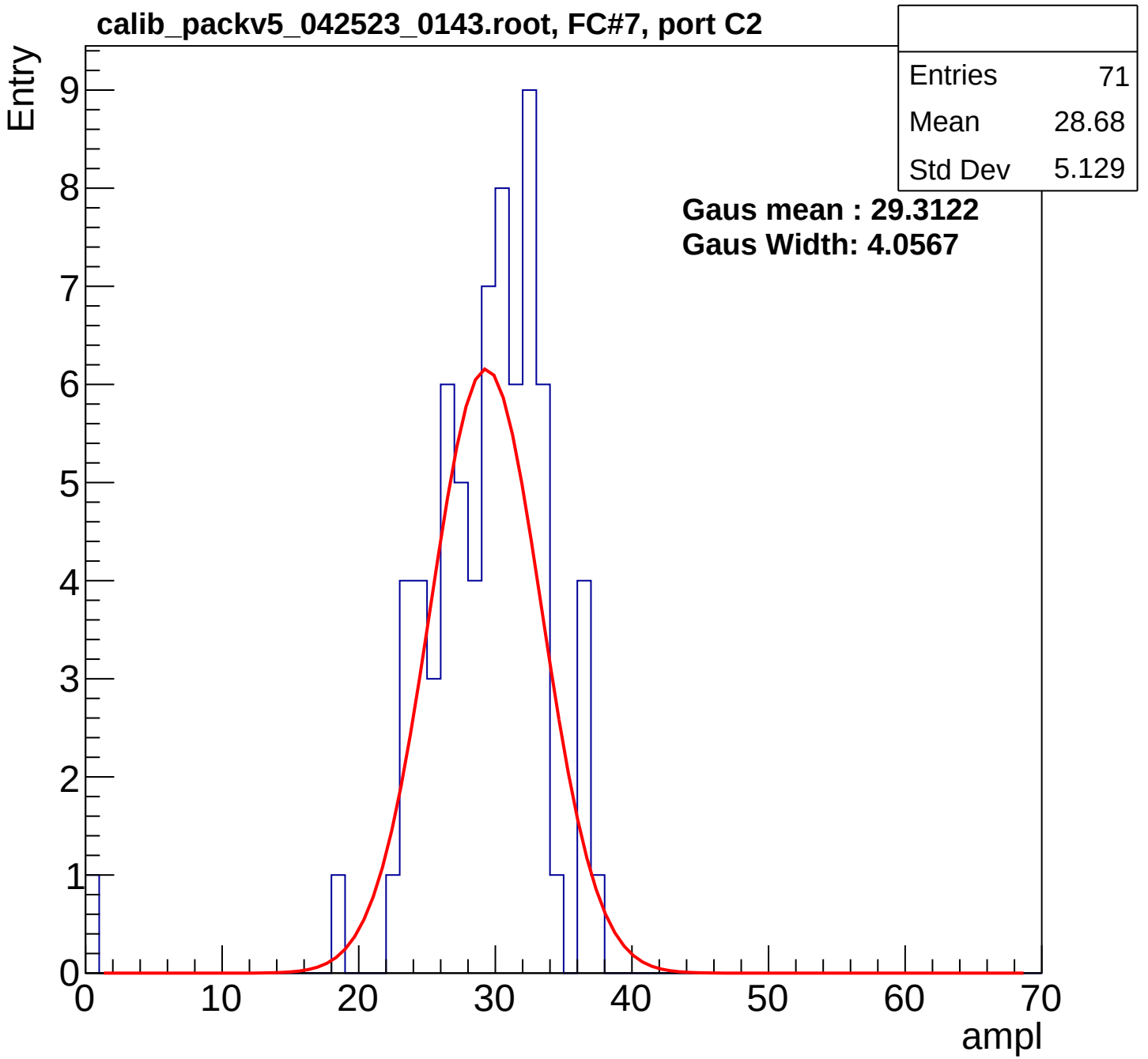

B1L103S, U8-ch95, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 50.49
Std Dev 3.376
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

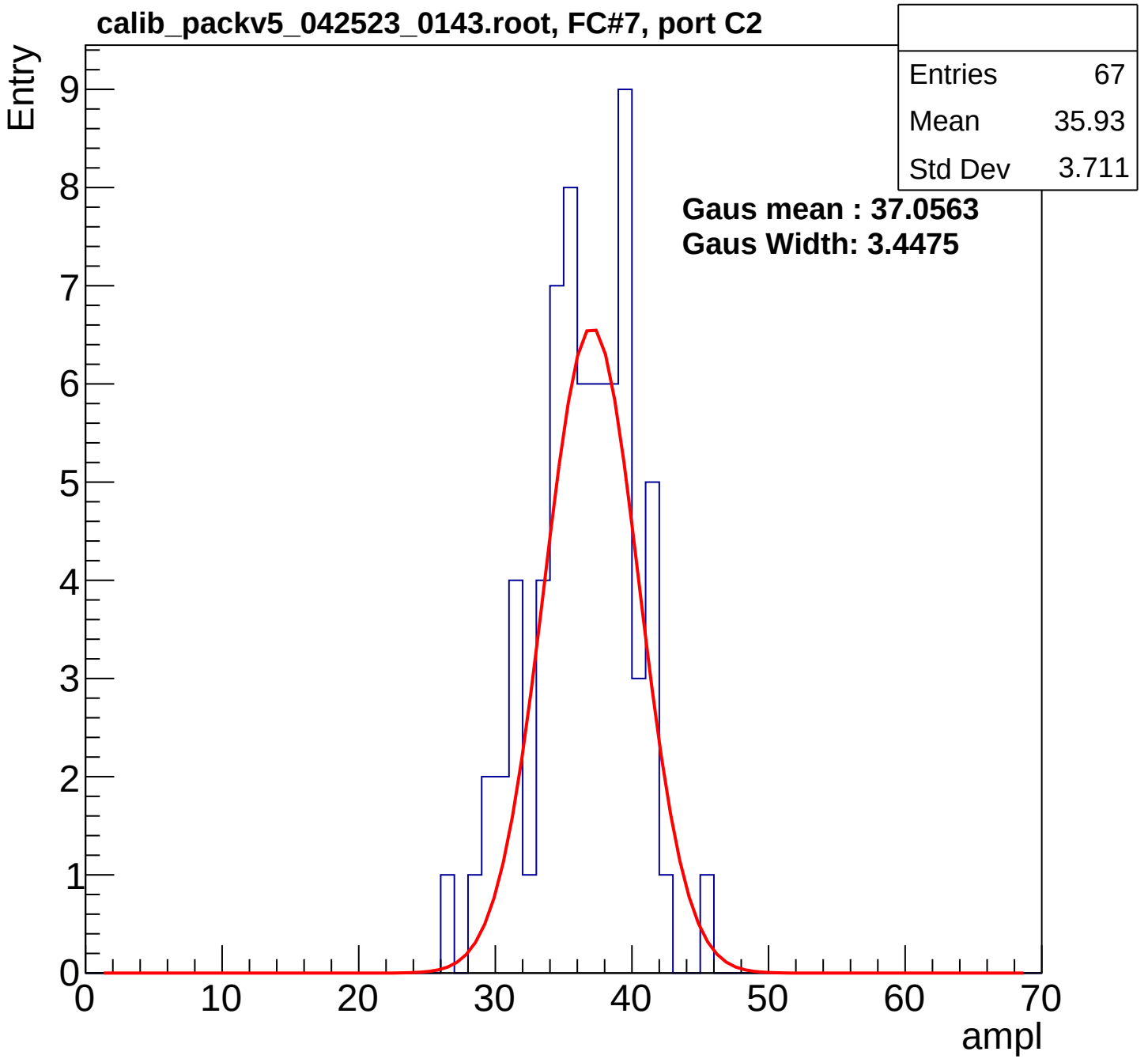

B1L103S, U8-ch95, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 56.72
Std Dev 3.558
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

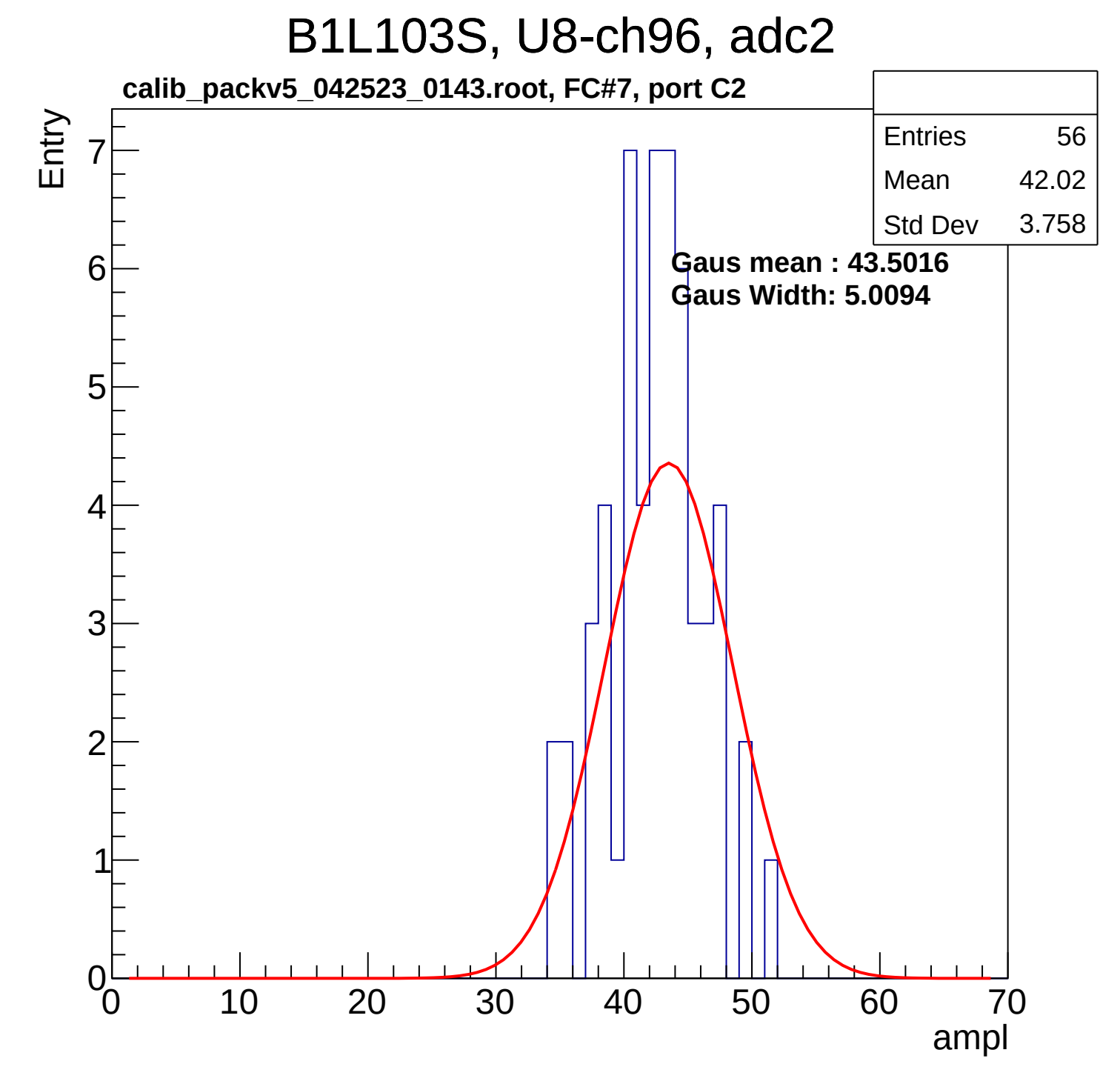

B1L103S, U8-ch95, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 38
Mean 58.5
Std Dev 9.827
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

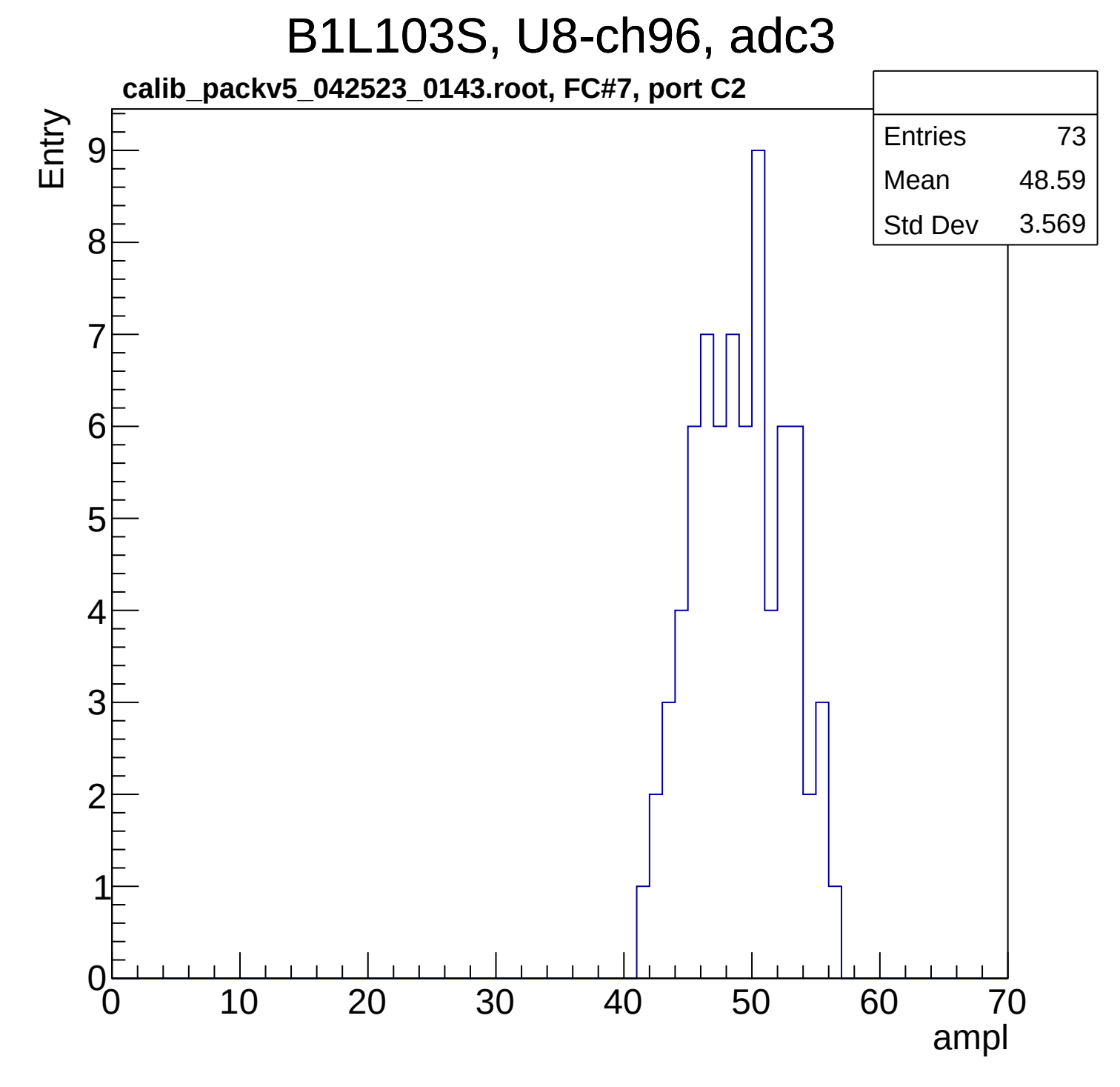

B1L103S, U8-ch95, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 61.5
Std Dev 2.062
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

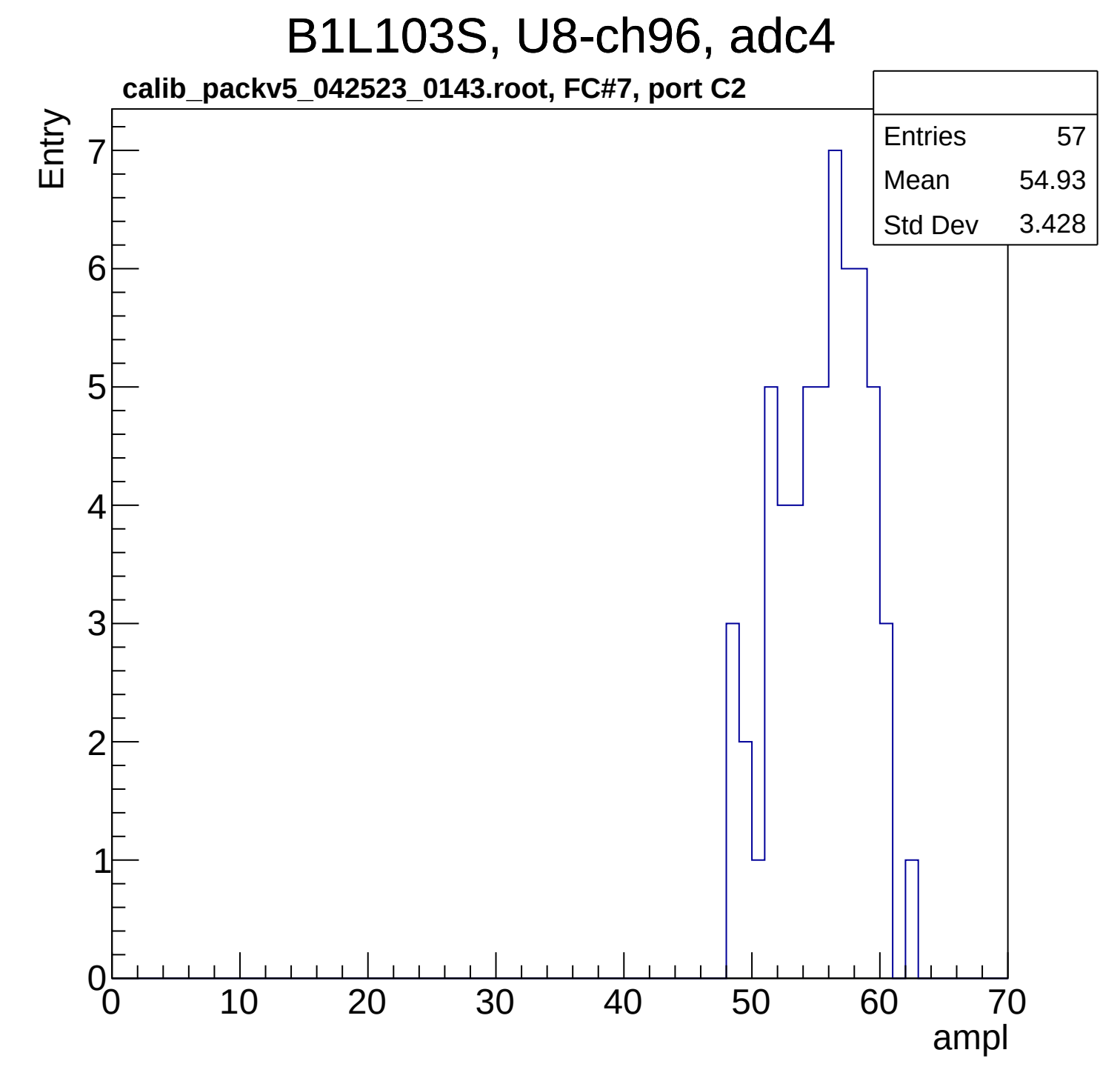

B1L103S, U8-ch95, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

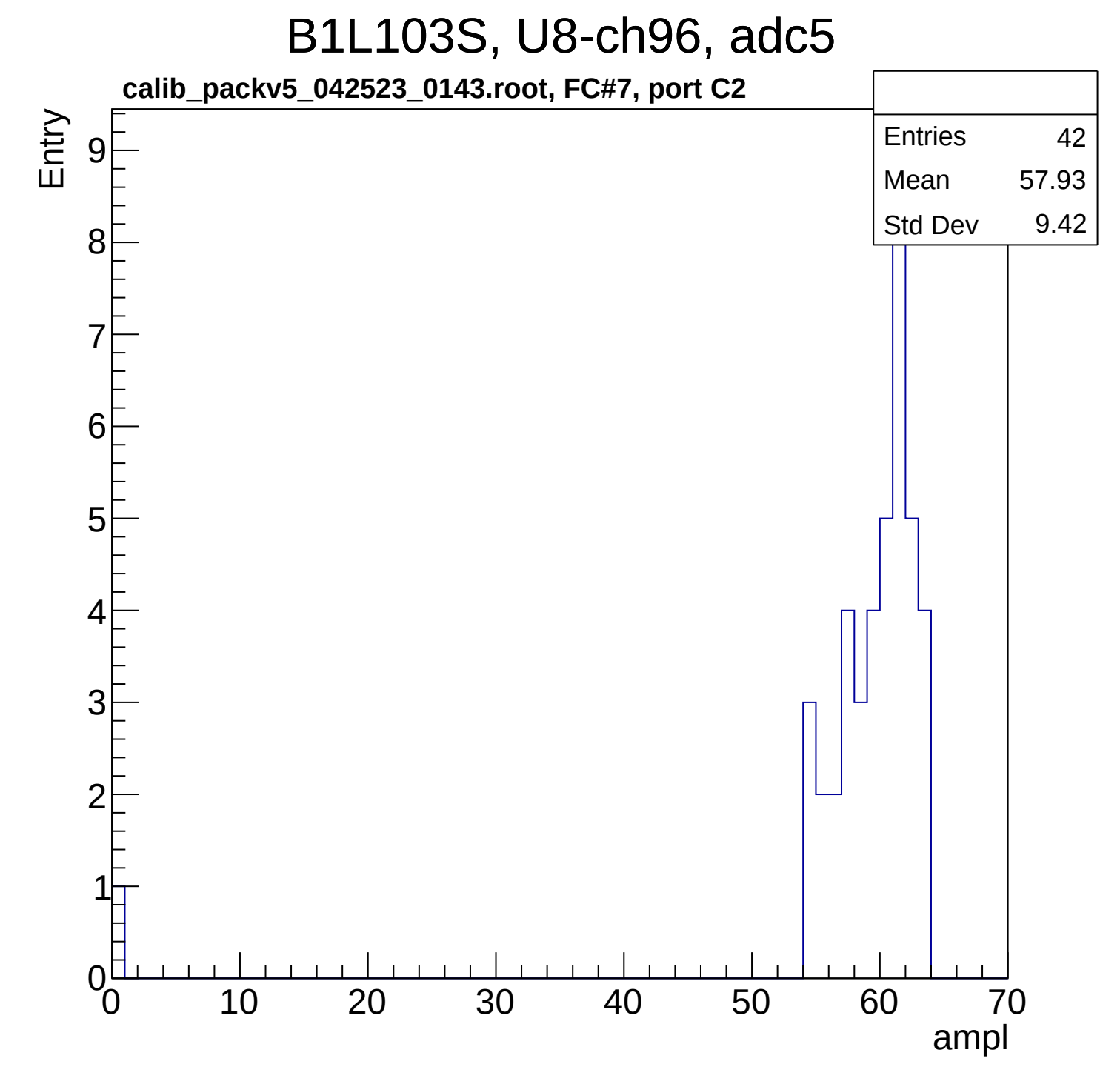

B1L103S, U8-ch96, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 28.68
Std Dev 5.129
Gaus mean : 29.3122
Gaus Width: 4.0567
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

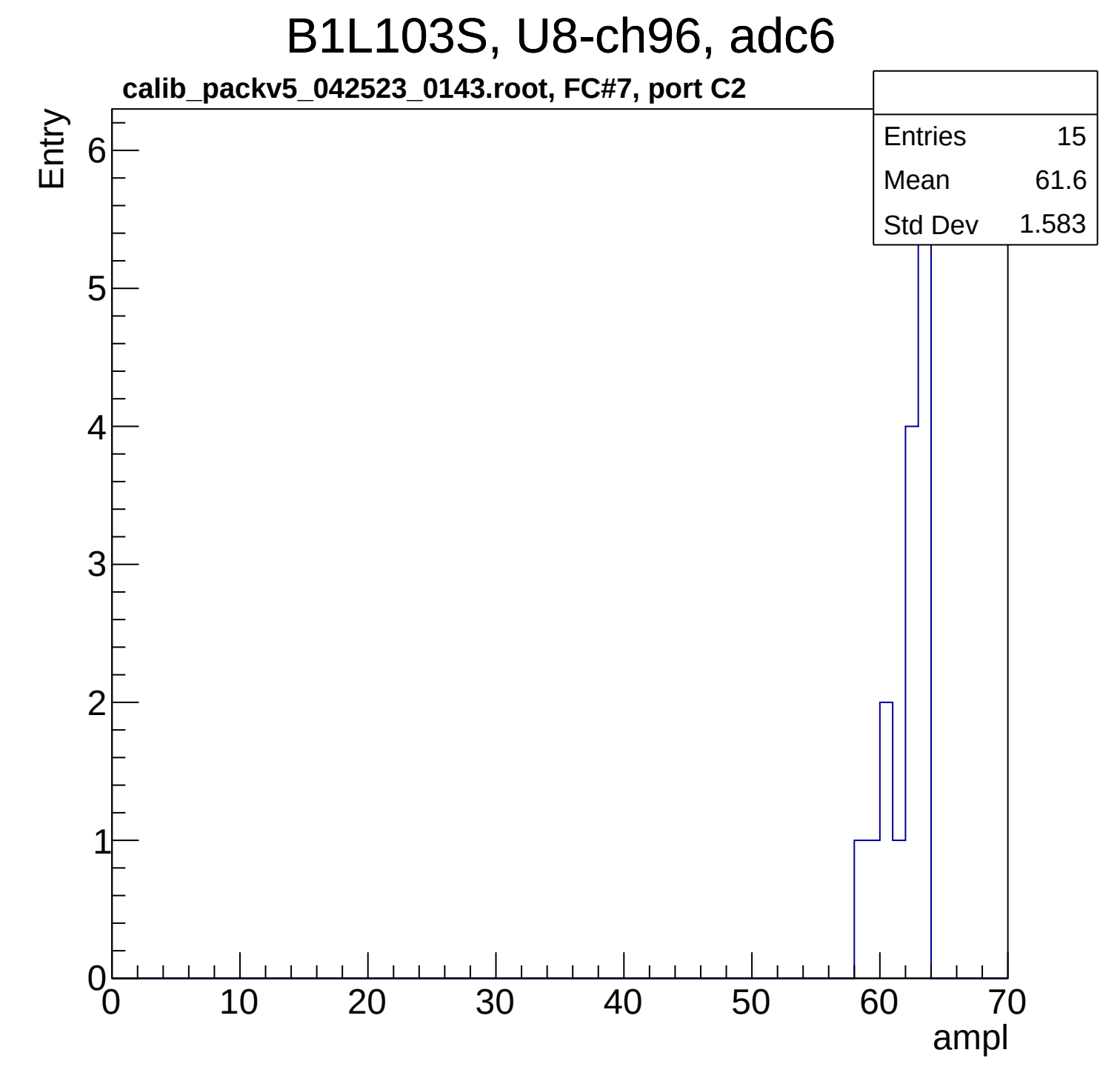

B1L103S, U8-ch96, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 35.93
Std Dev 3.711
Gaus mean : 37.0563
Gaus Width: 3.4475
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

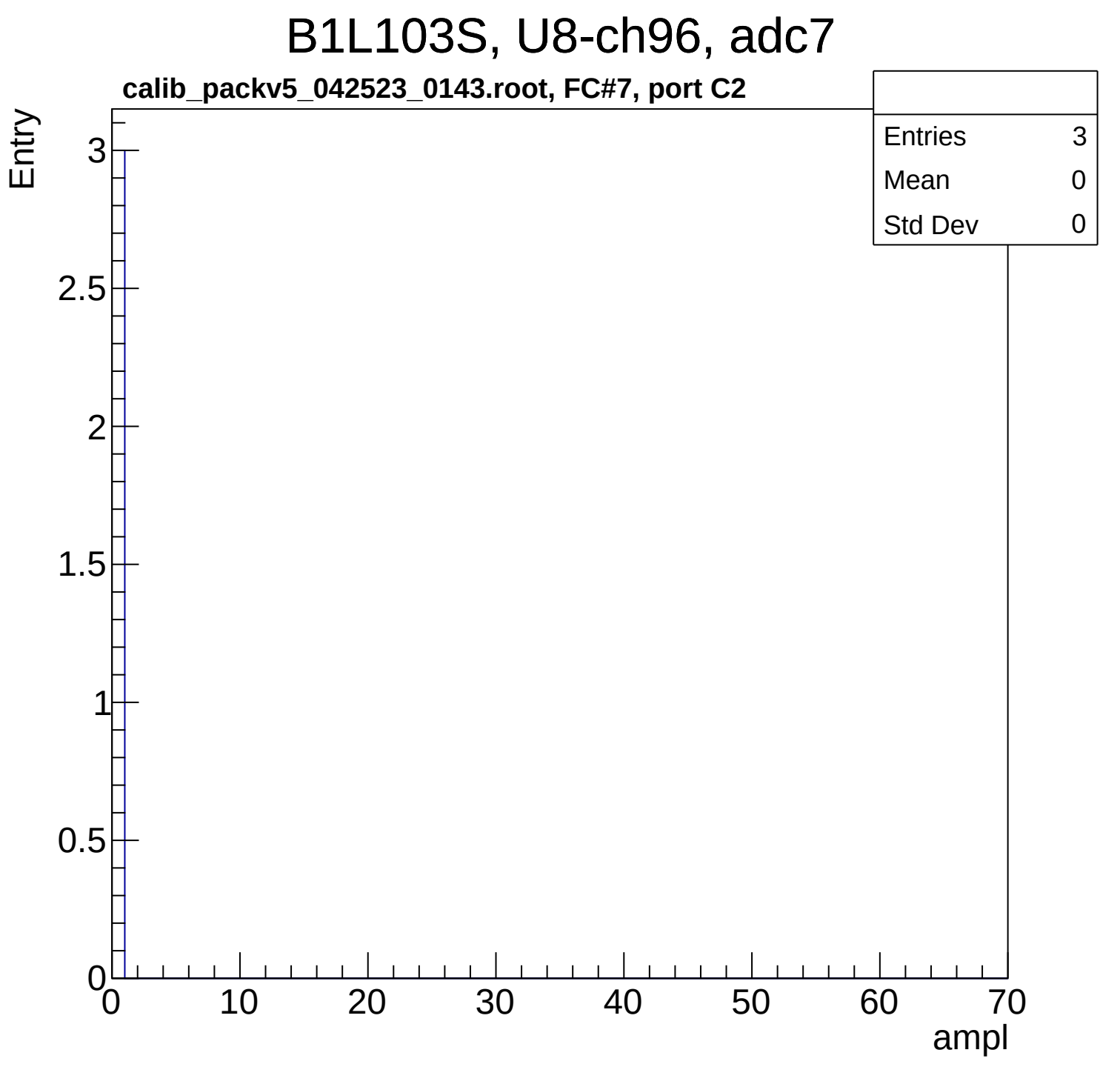

B1L103S, U8-ch96, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 42.02
Std Dev 3.758
Gaus mean : 43.5016
Gaus Width: 5.0094
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

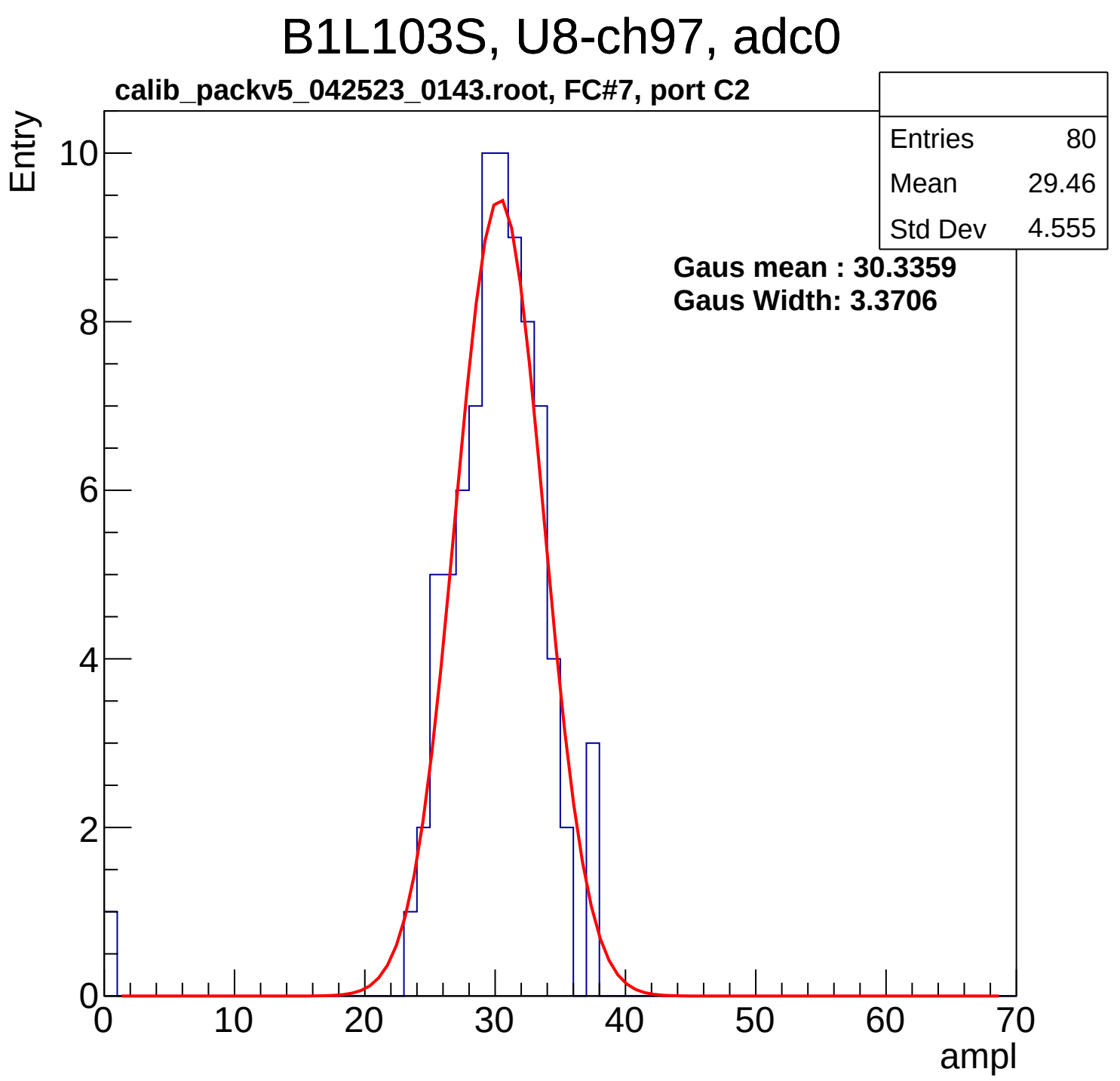

B1L103S, U8-ch96, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 48.59
Std Dev 3.569
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

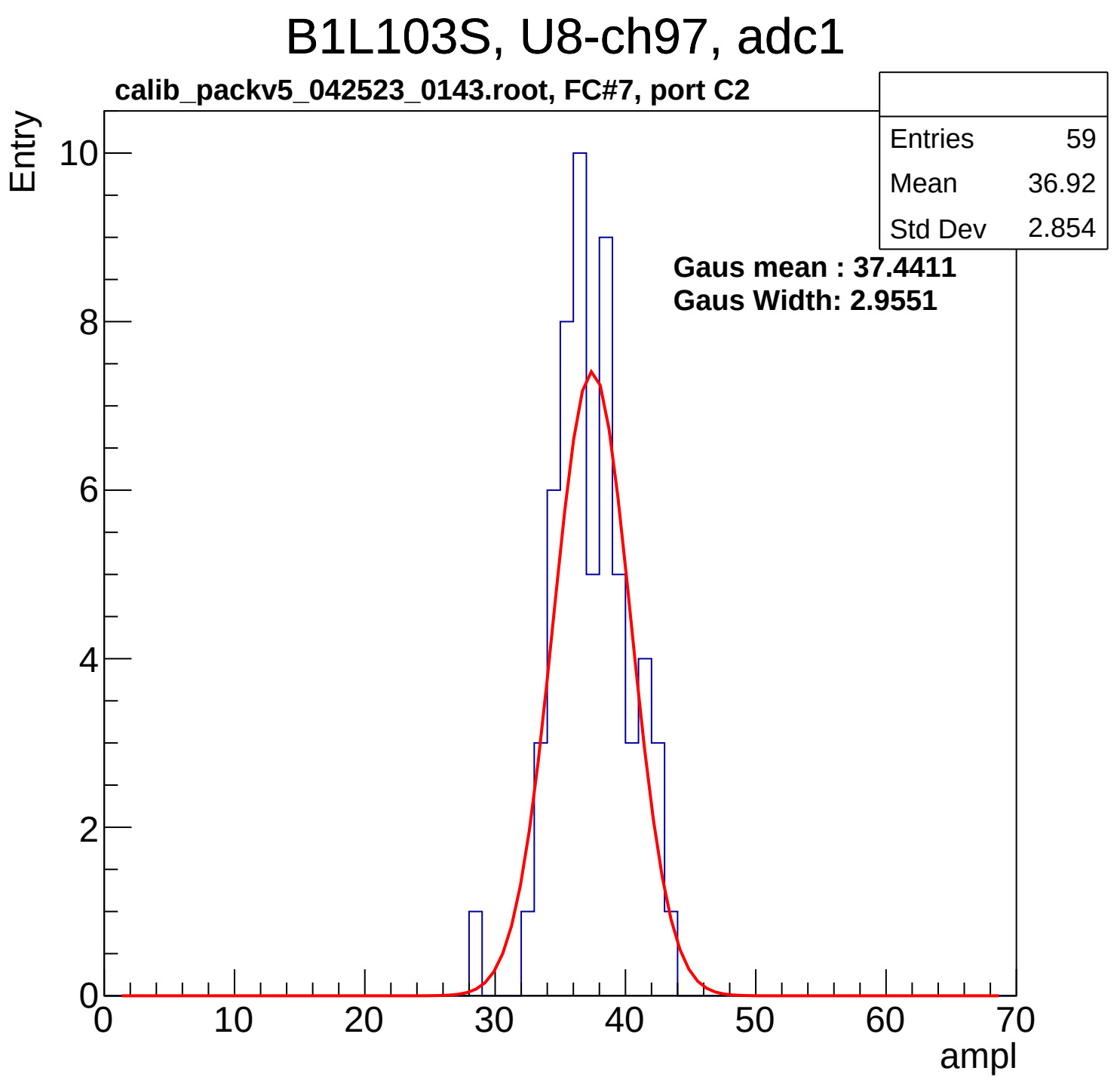

B1L103S, U8-ch96, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 54.93
Std Dev 3.428
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

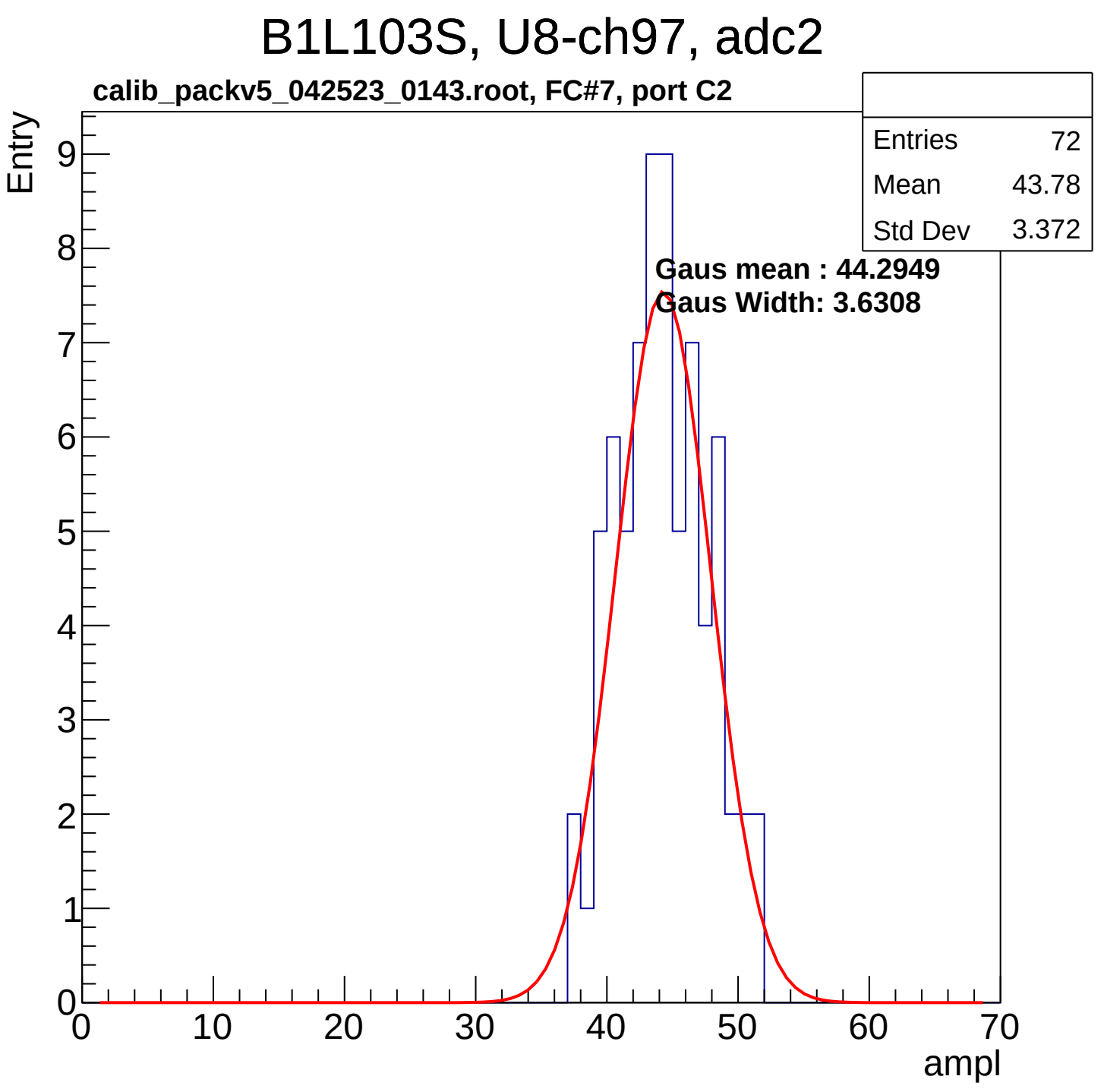

B1L103S, U8-ch96, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 42
Mean 57.93
Std Dev 9.42
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

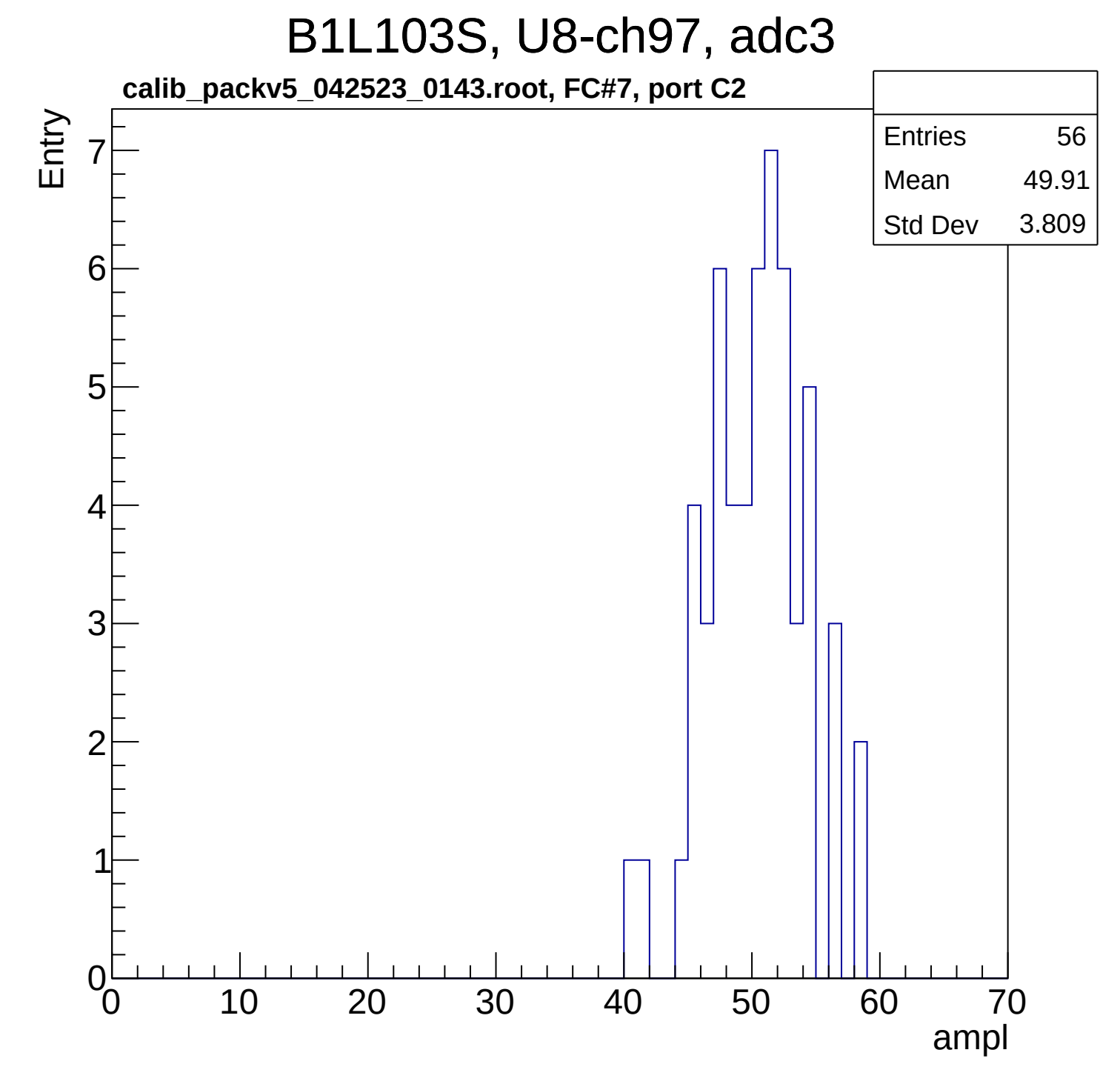

B1L103S, U8-ch96, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 15
Mean 61.6
Std Dev 1.583
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

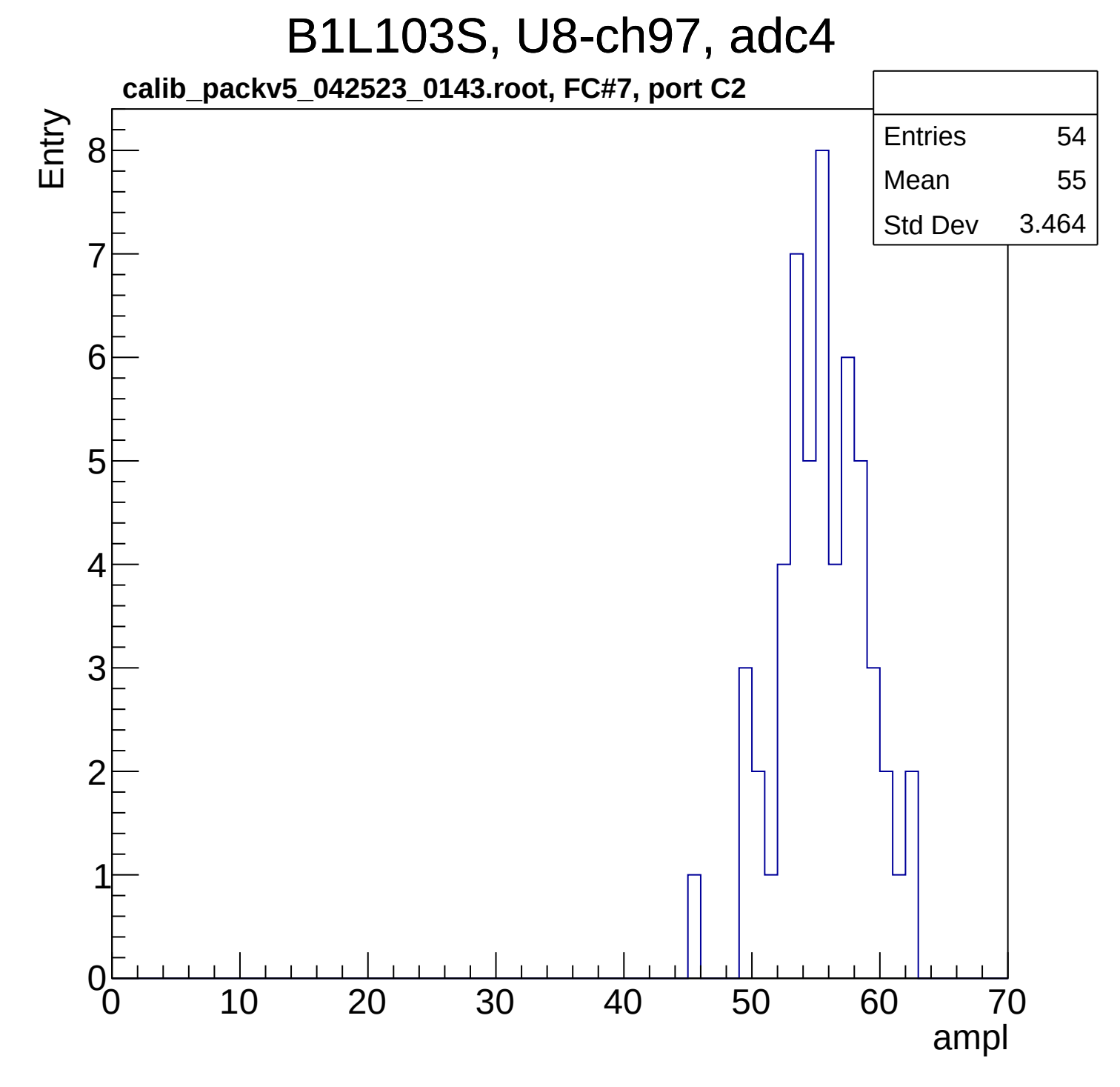

B1L103S, U8-ch96, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 0
Std Dev 0
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl

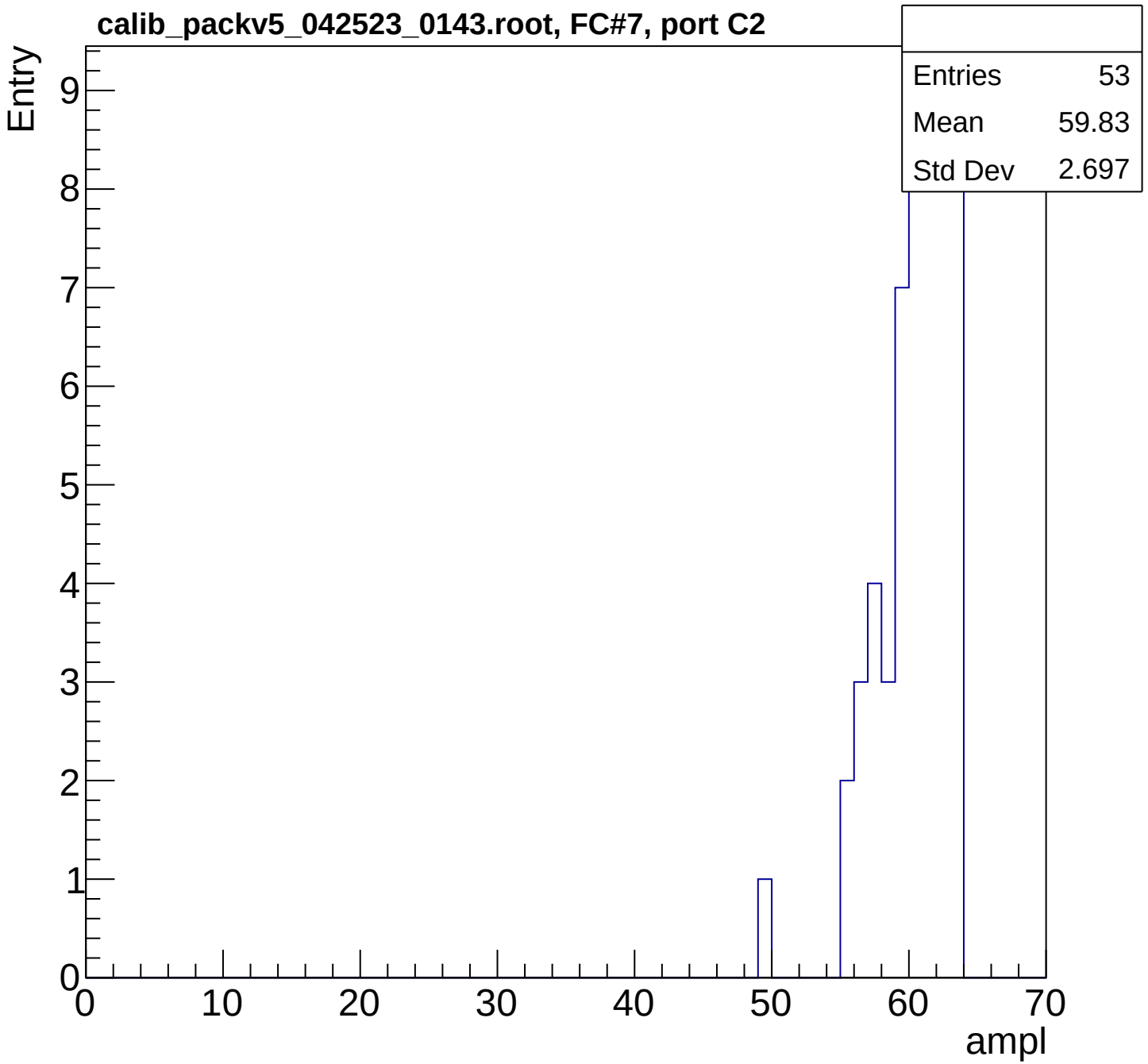

B1L103S, U8-ch97, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 80
Mean 29.46
Std Dev 4.555
Gaus mean : 30.3359
Gaus Width: 3.3706
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

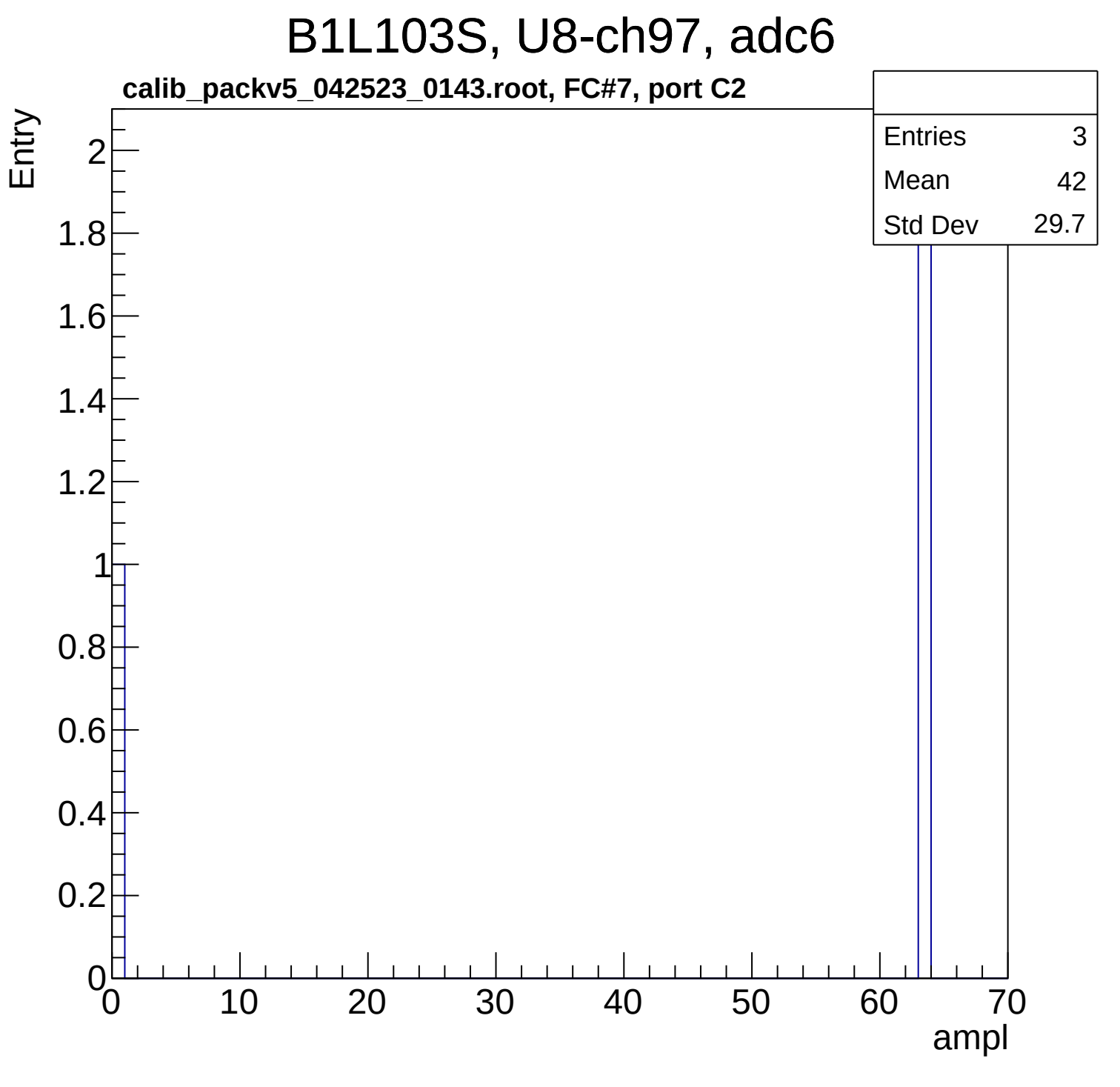

B1L103S, U8-ch97, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 36.92
Std Dev 2.854
Gaus mean : 37.4411
Gaus Width: 2.9551
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

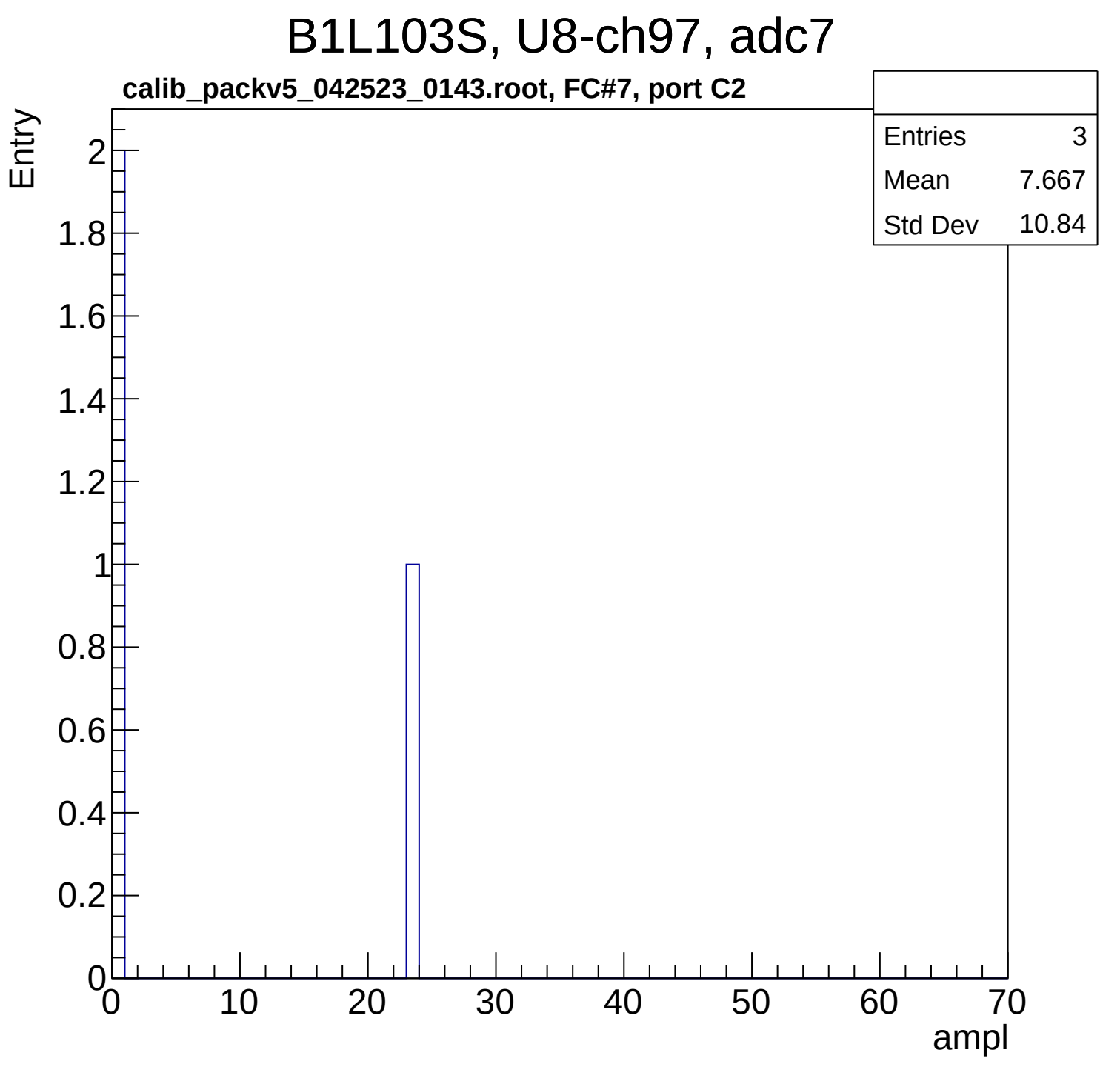

B1L103S, U8-ch97, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 43.78
Std Dev 3.372
Gaus mean : 44.2949
Gaus Width: 3.6308
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

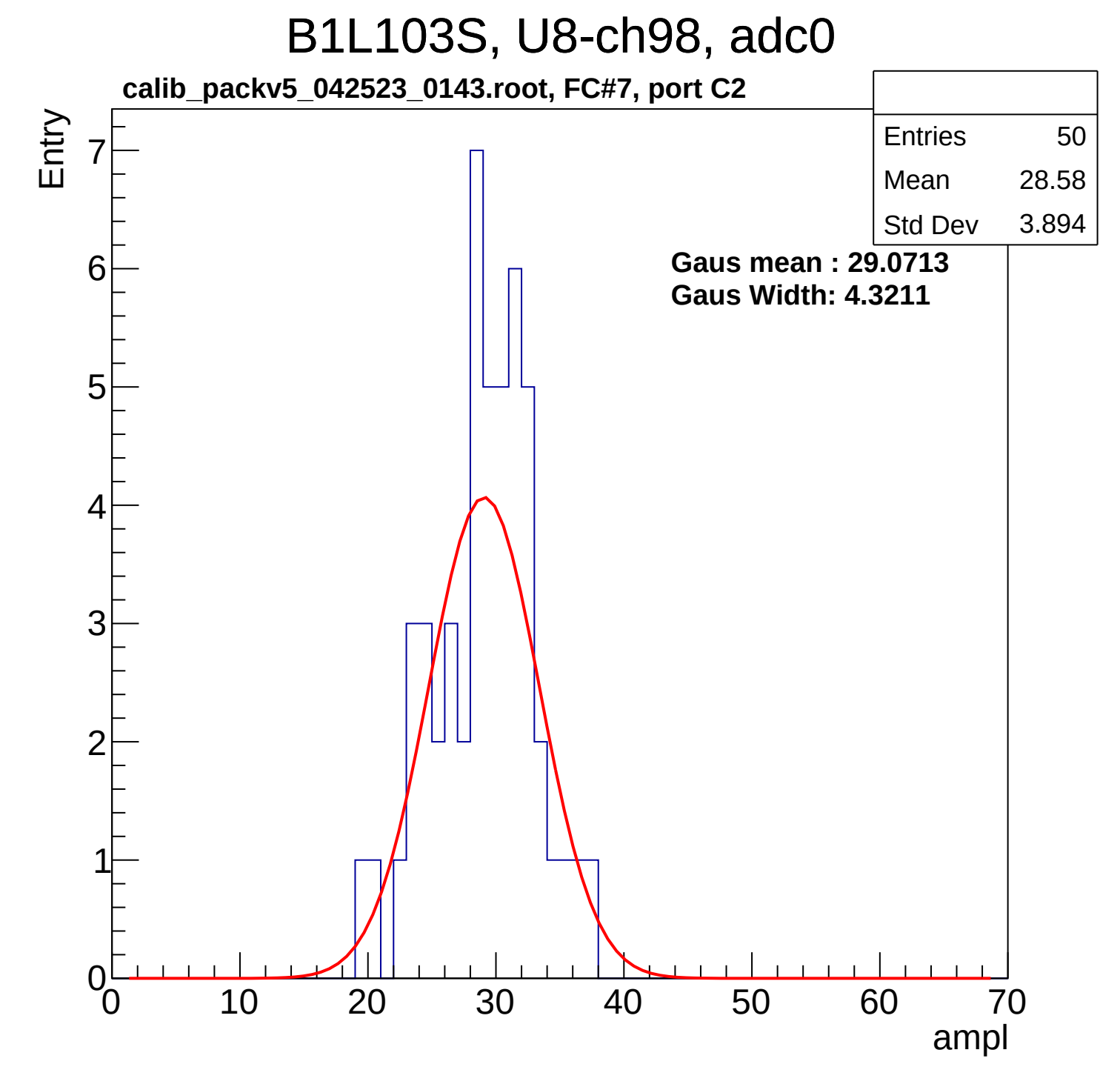

B1L103S, U8-ch97, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 49.91
Std Dev 3.809
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

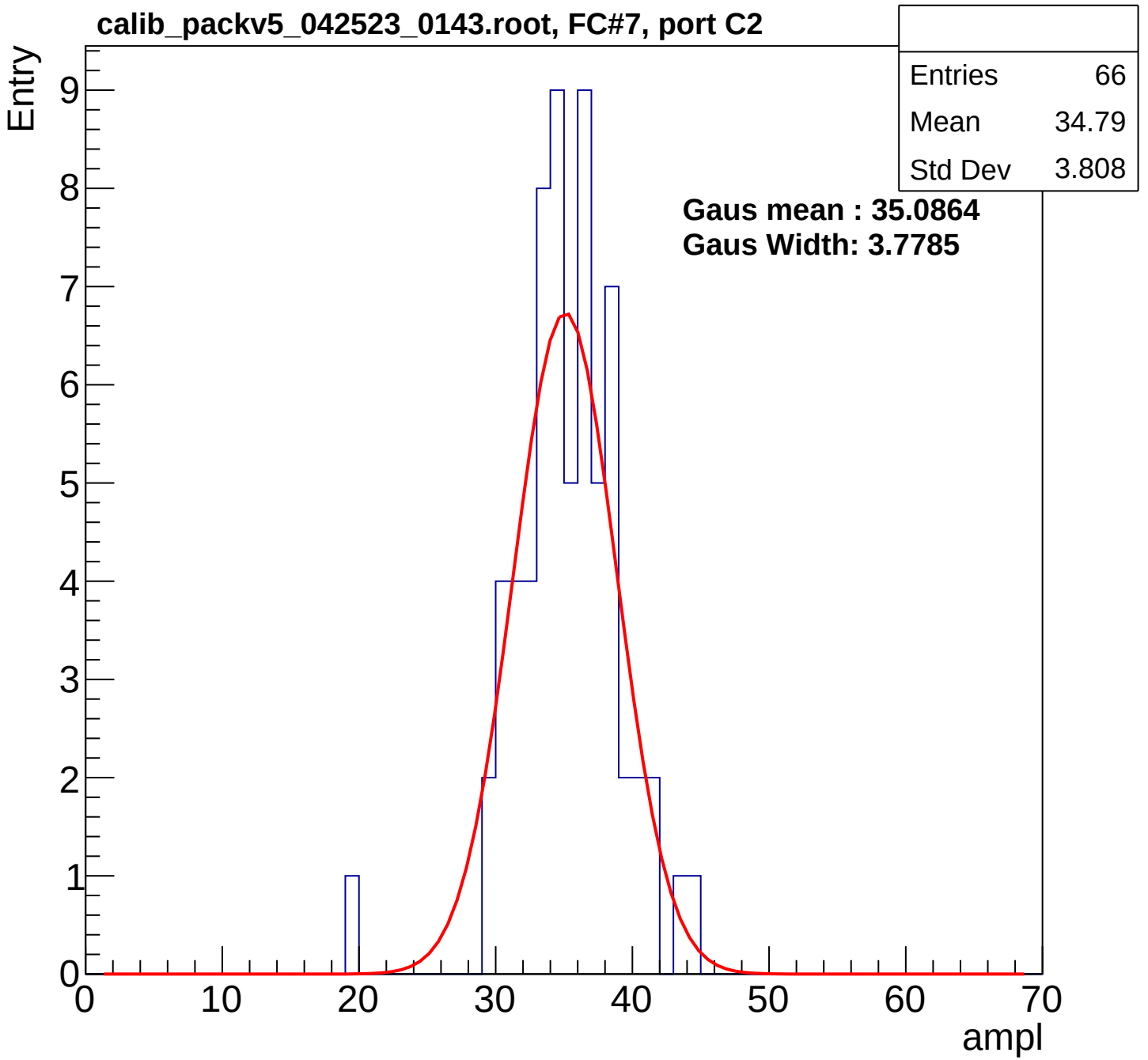

B1L103S, U8-ch97, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 55
Std Dev 3.464
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

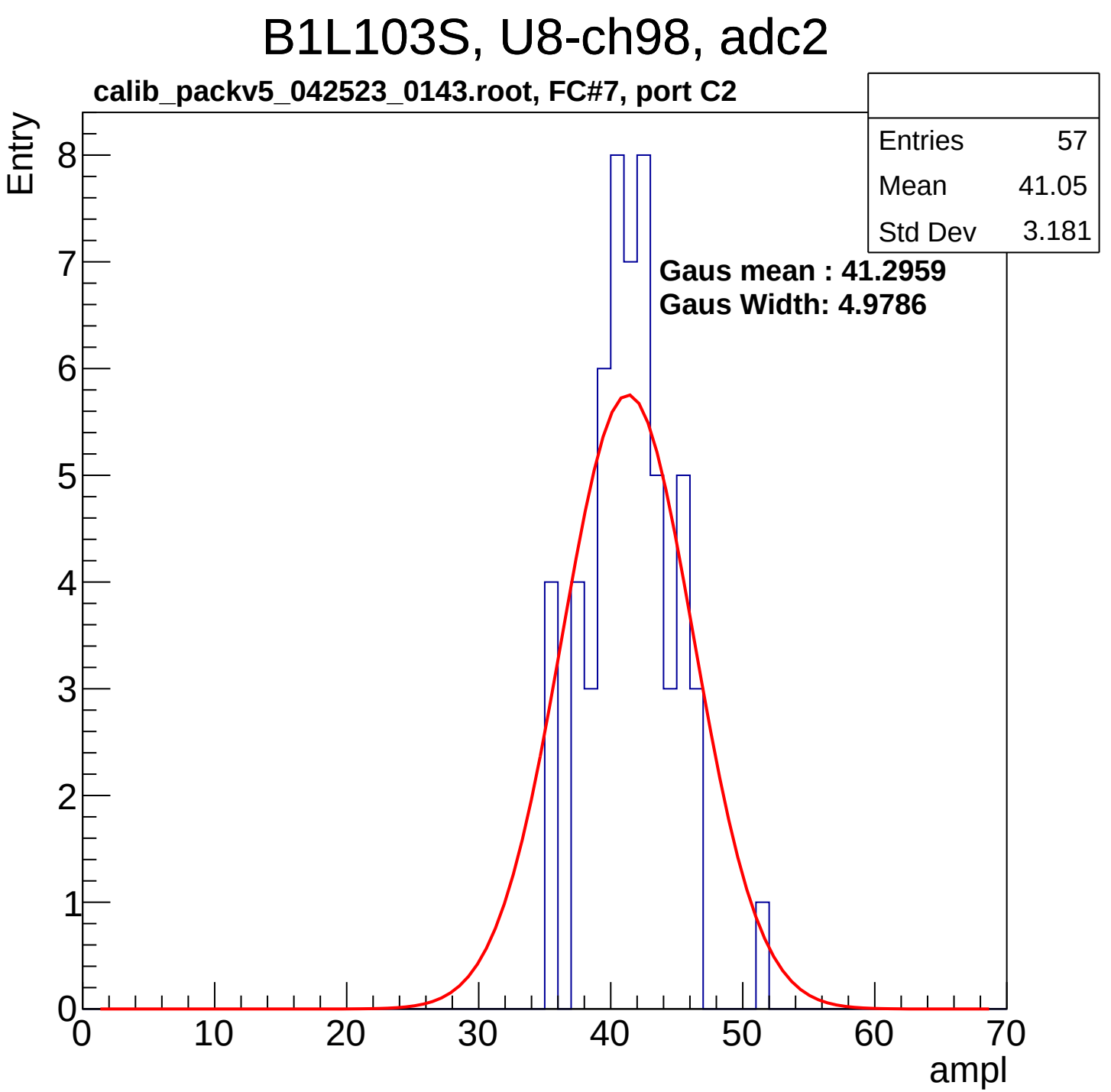

B1L103S, U8-ch97, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 59.83
Std Dev 2.697
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

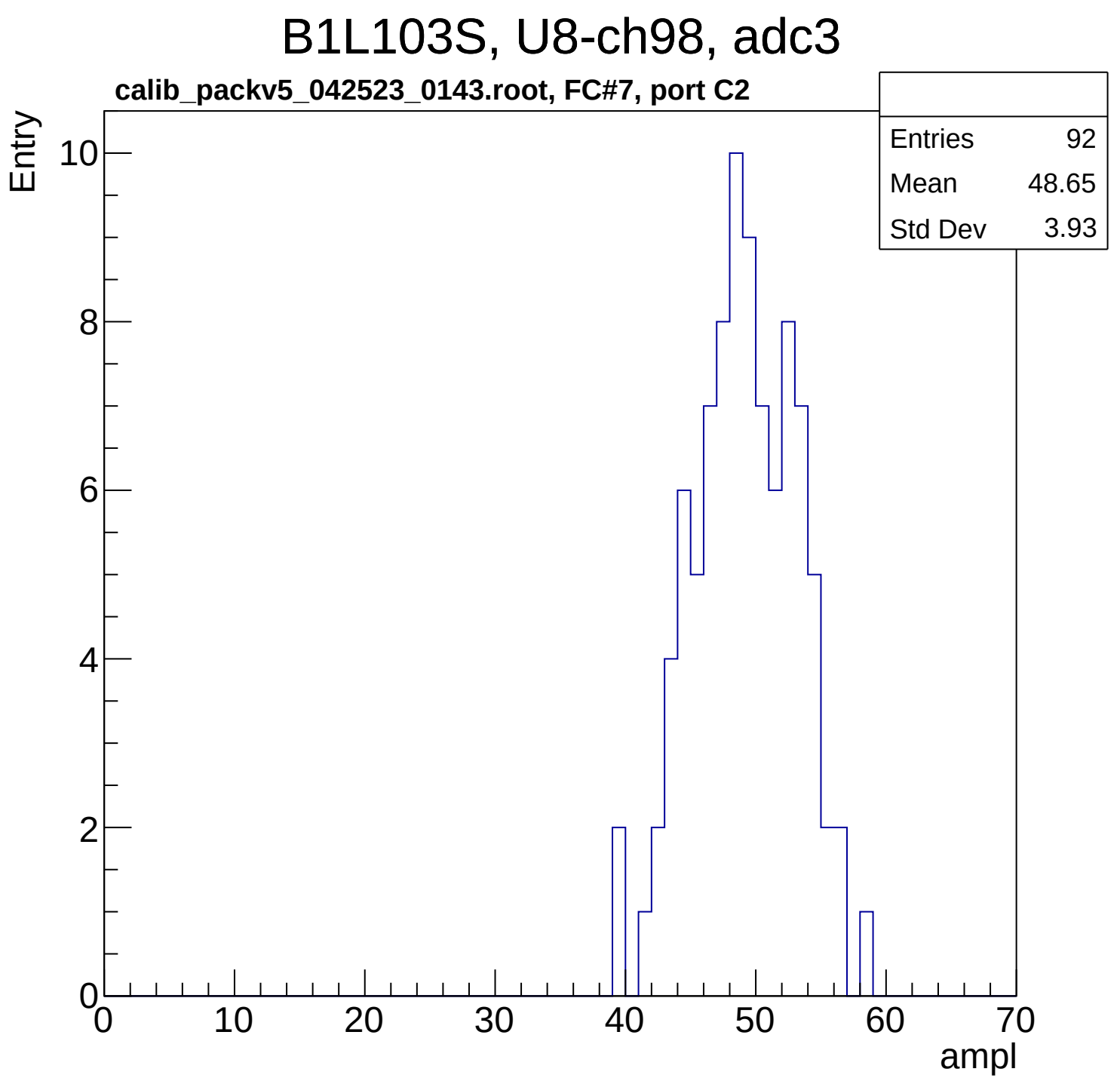

B1L103S, U8-ch97, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 42
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

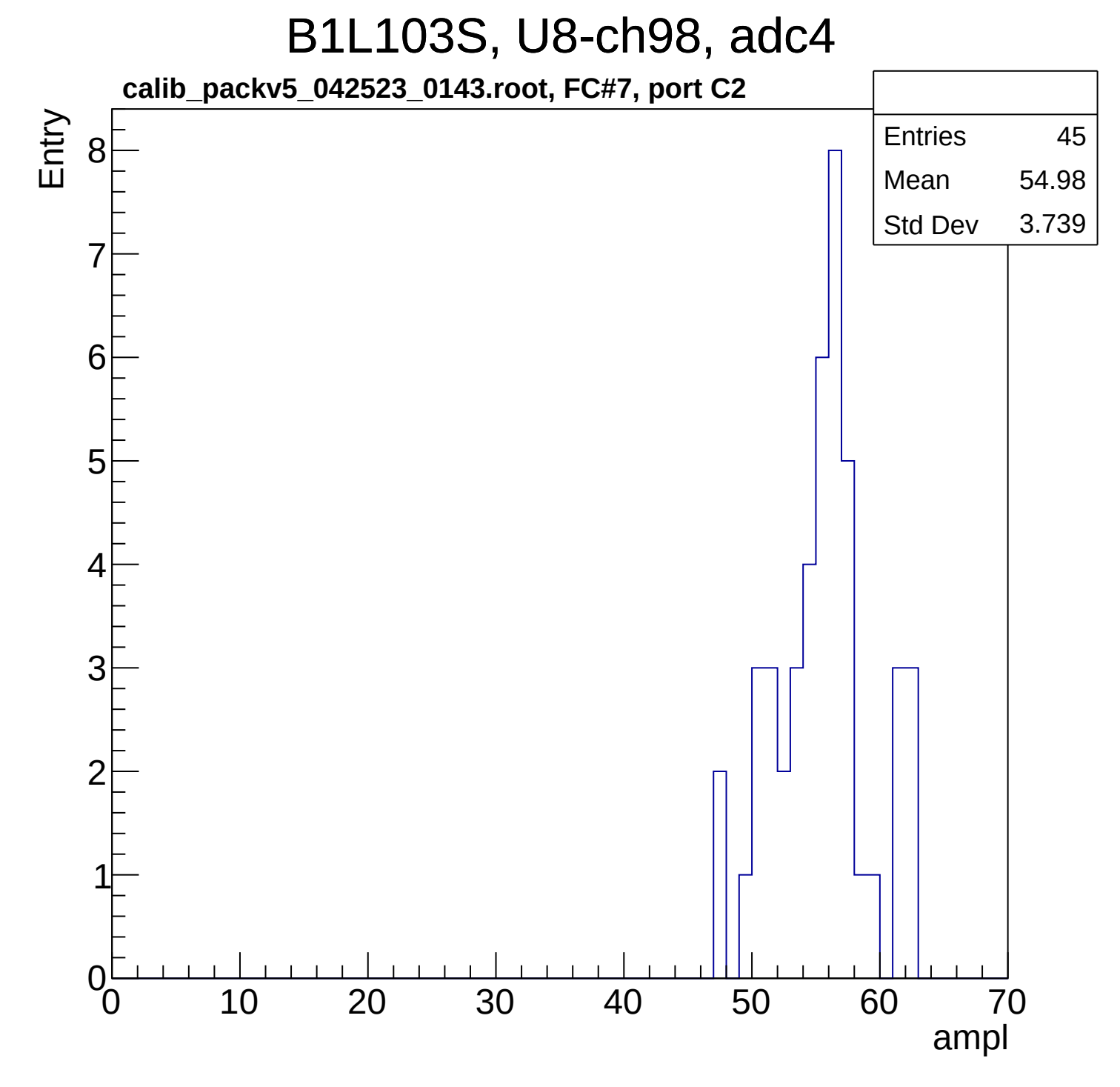

B1L103S, U8-ch97, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 7.667
Std Dev 10.84
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

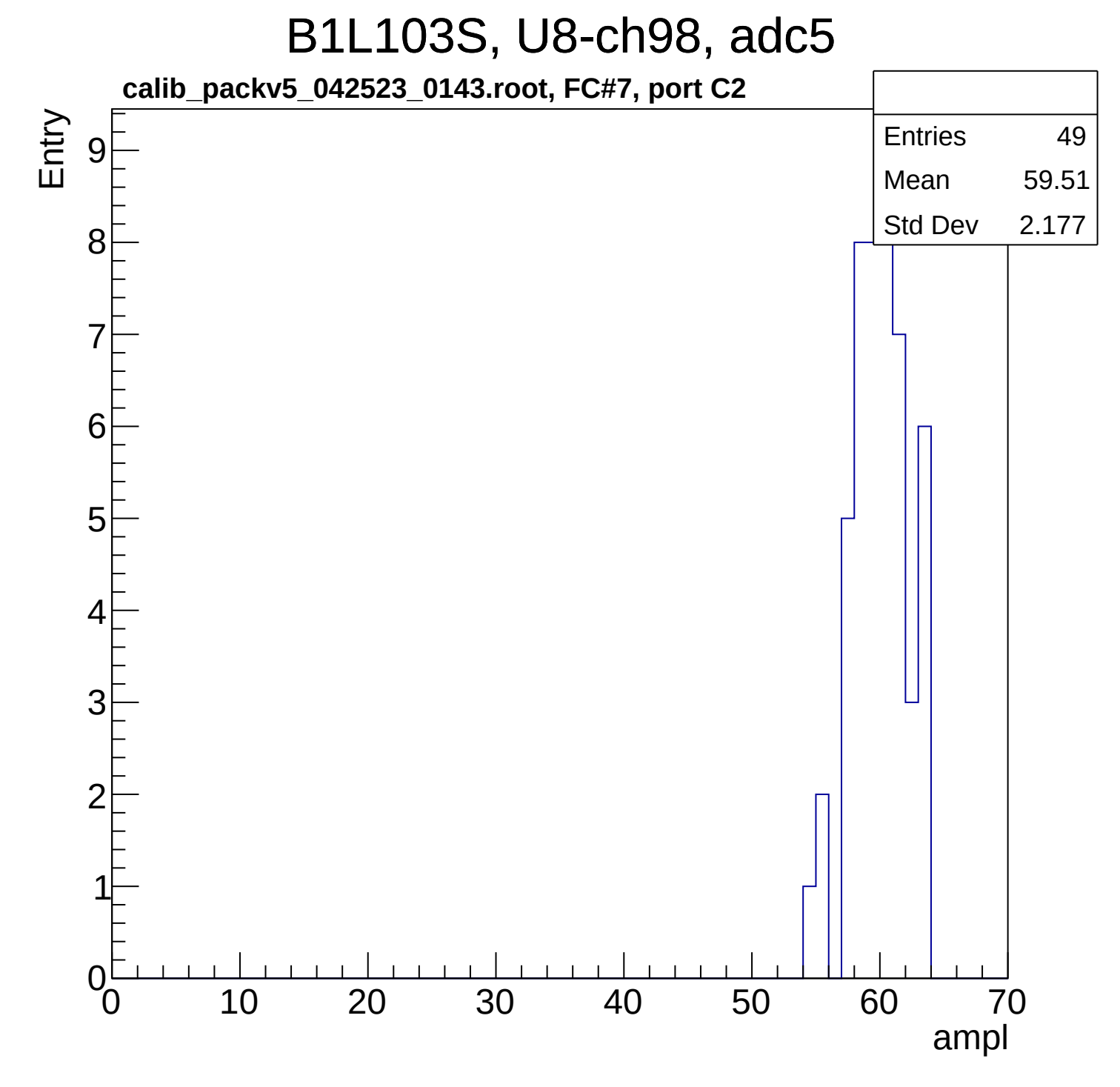

B1L103S, U8-ch98, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 28.58
Std Dev 3.894
Gaus mean : 29.0713
Gaus Width: 4.3211
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

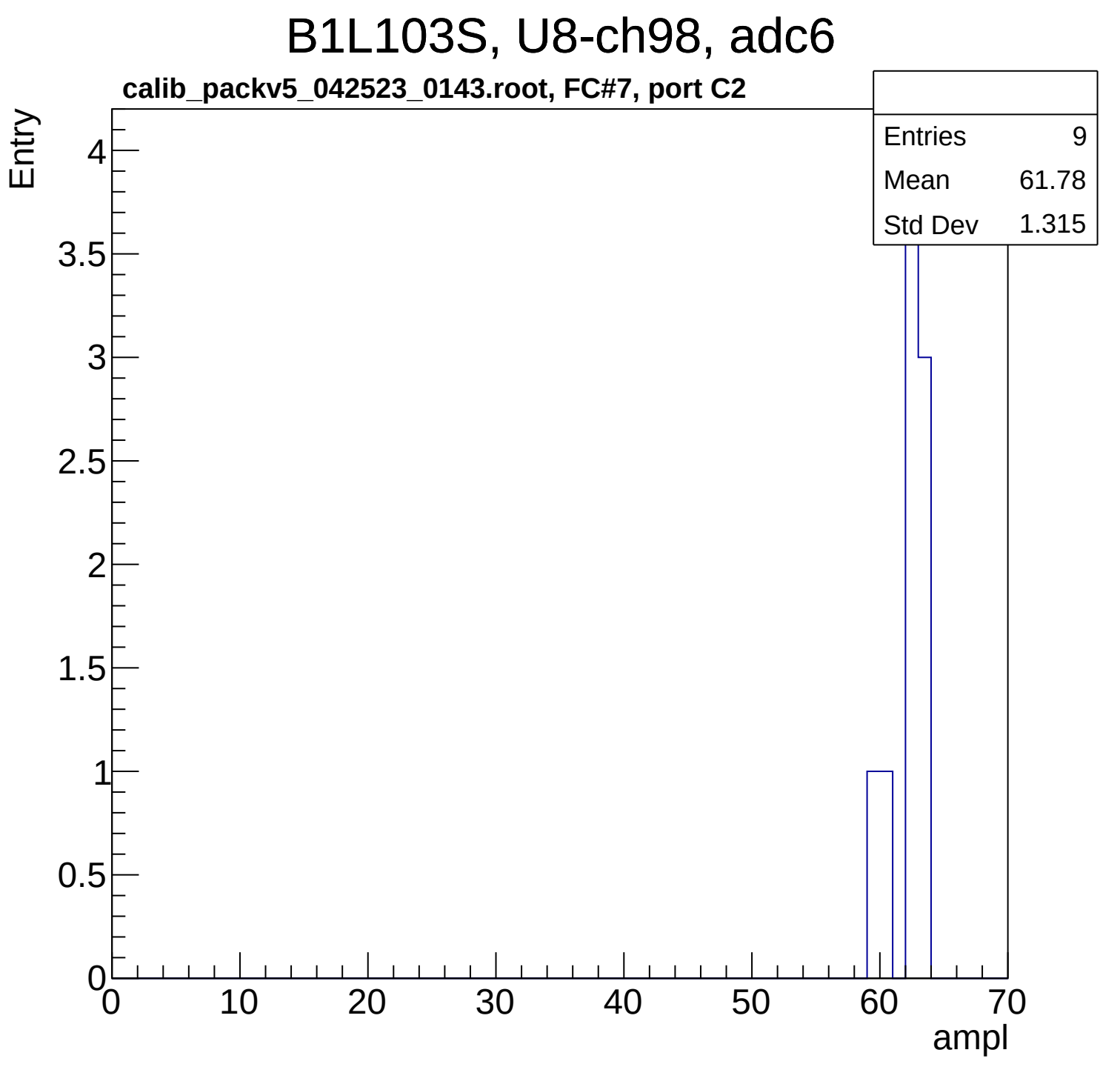

B1L103S, U8-ch98, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 34.79
Std Dev 3.808
Gaus mean : 35.0864
Gaus Width: 3.7785
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

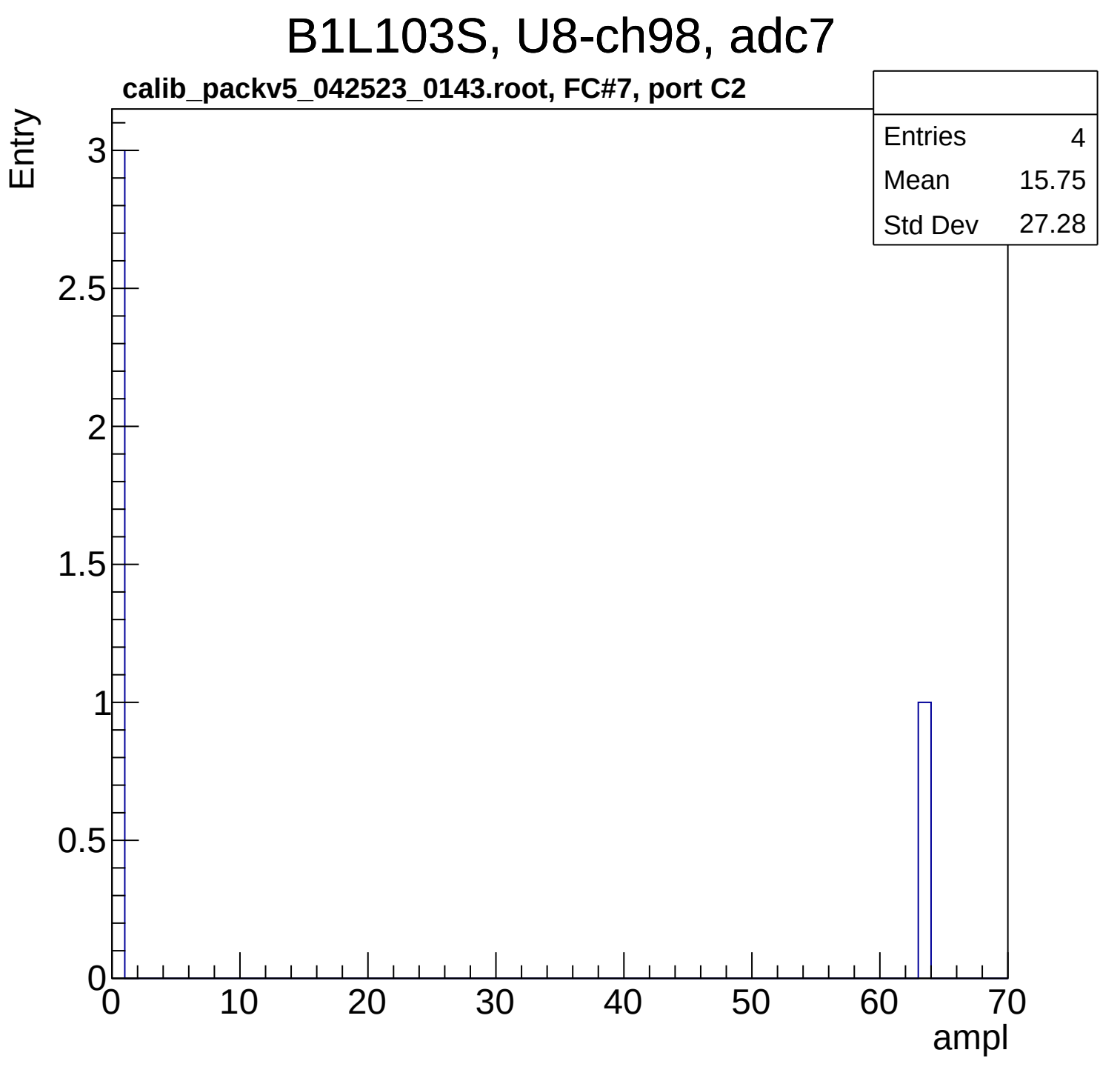

B1L103S, U8-ch98, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 41.05
Std Dev 3.181
Gaus mean : 41.2959
Gaus Width: 4.9786
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

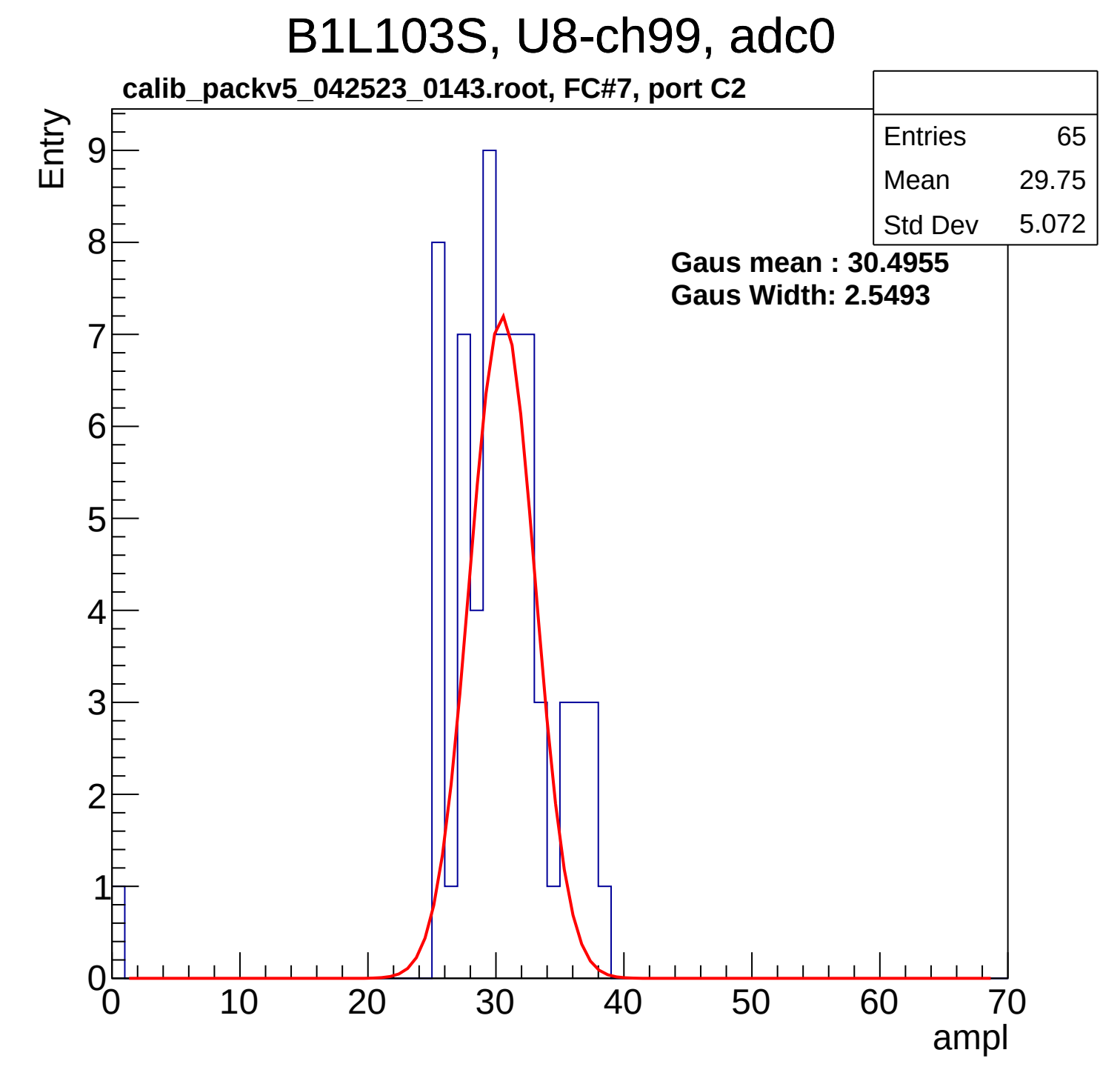

B1L103S, U8-ch98, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 92
Mean 48.65
Std Dev 3.93
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

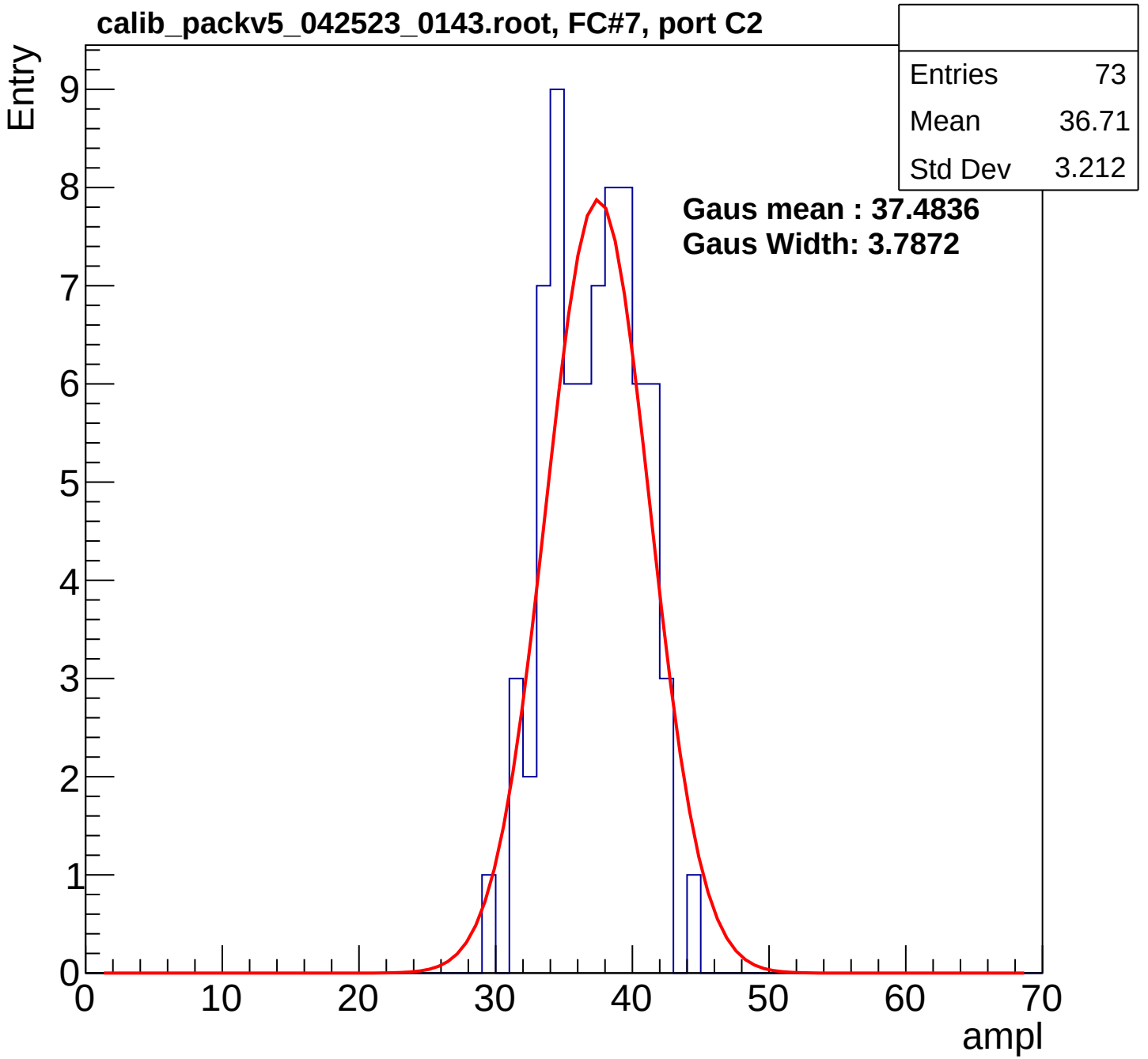

B1L103S, U8-ch98, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 45
Mean 54.98
Std Dev 3.739
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

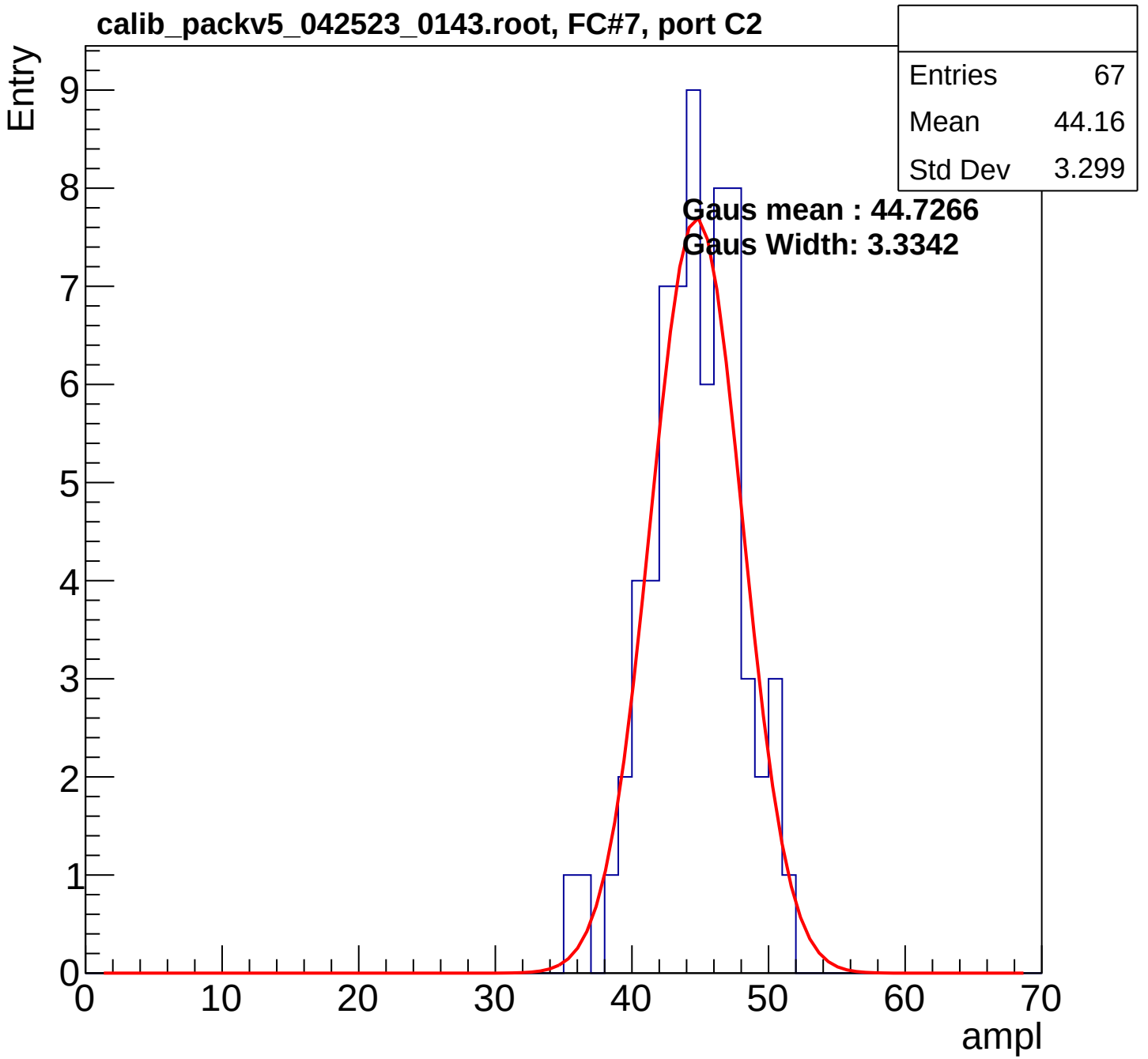

B1L103S, U8-ch98, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 59.51
Std Dev 2.177
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

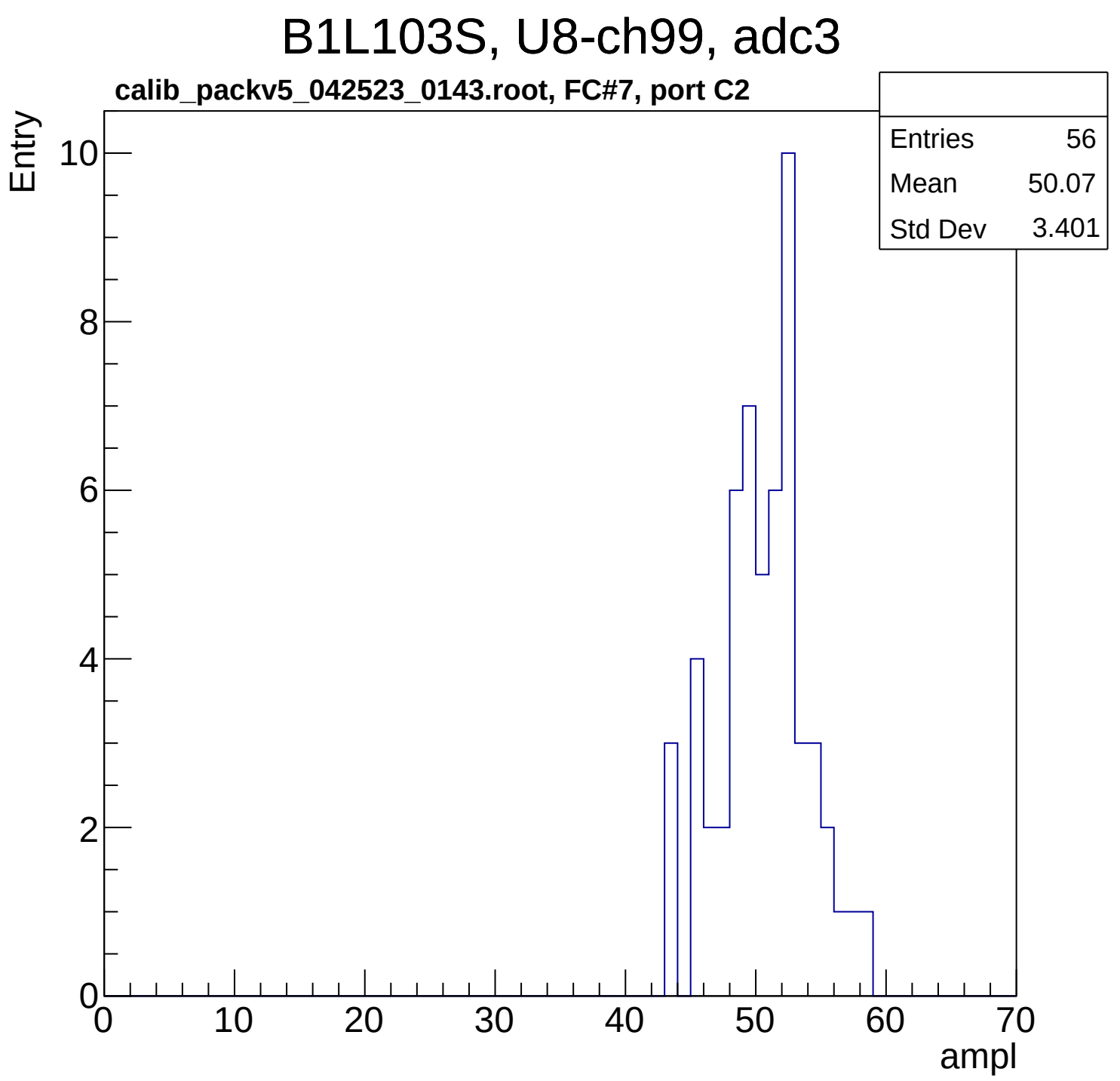

B1L103S, U8-ch98, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 9
Mean 61.78
Std Dev 1.315
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

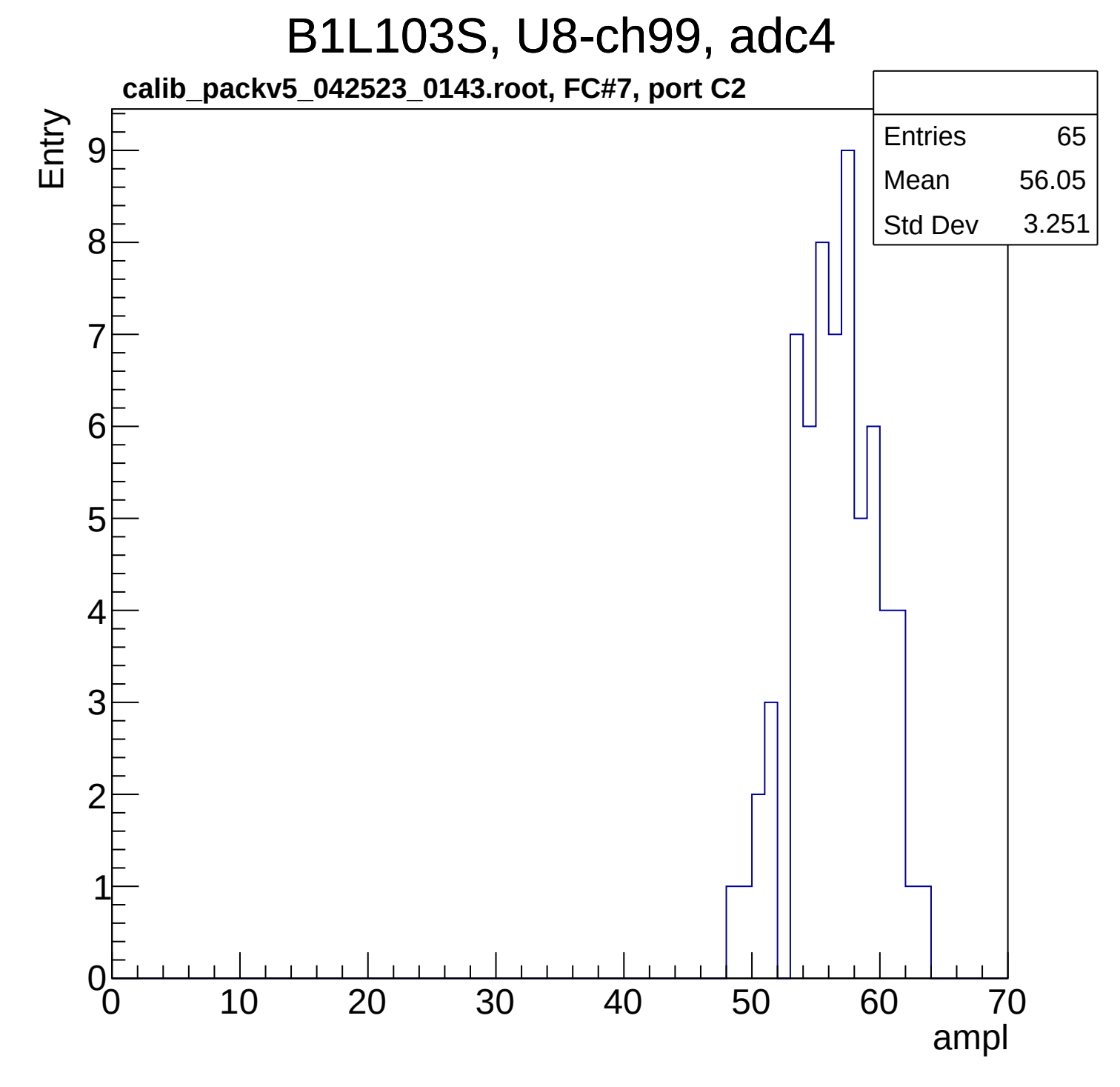

B1L103S, U8-ch98, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 15.75
Std Dev 27.28
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl

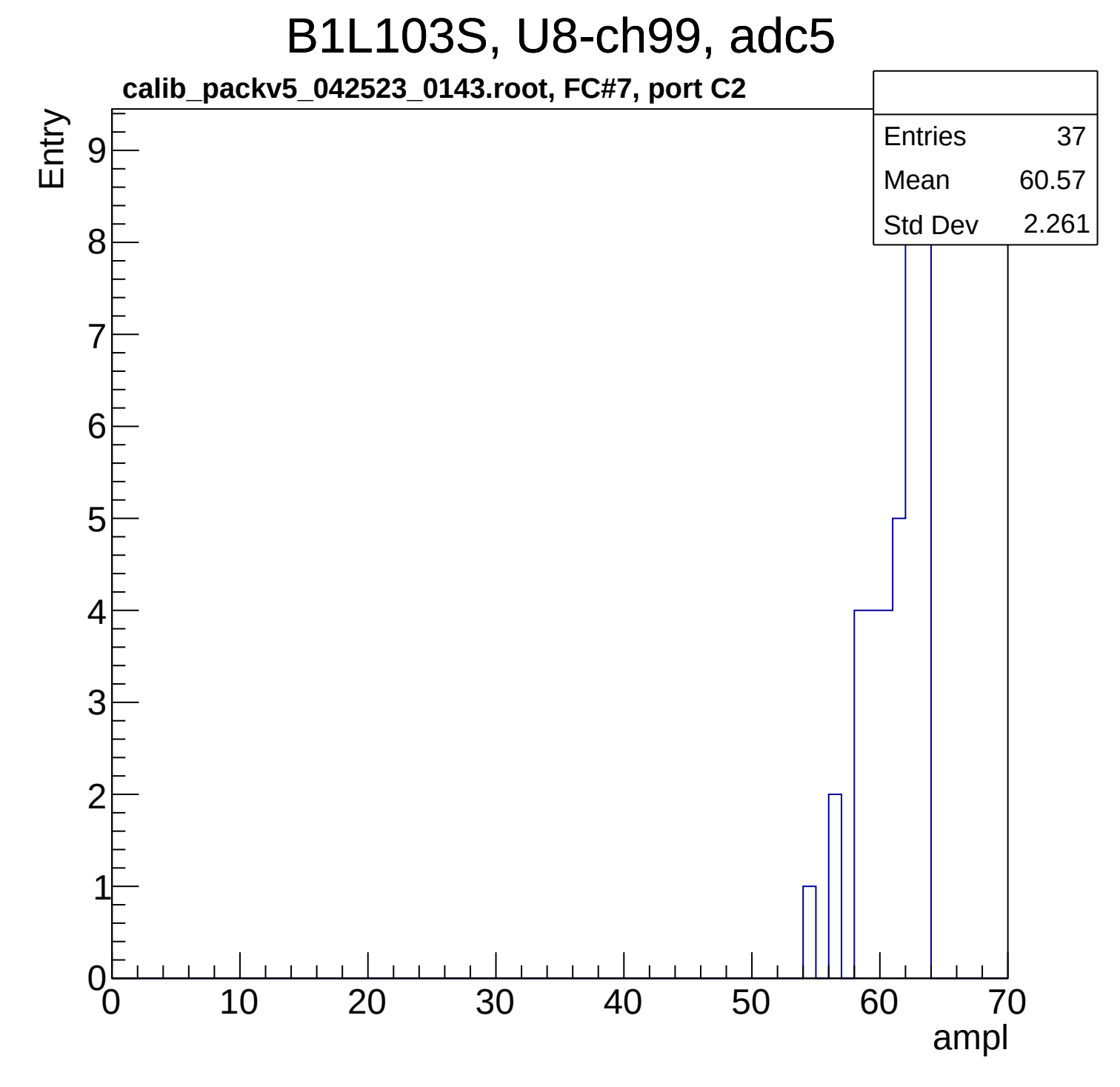

B1L103S, U8-ch99, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 29.75
Std Dev 5.072
Gaus mean : 30.4955
Gaus Width: 2.5493
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

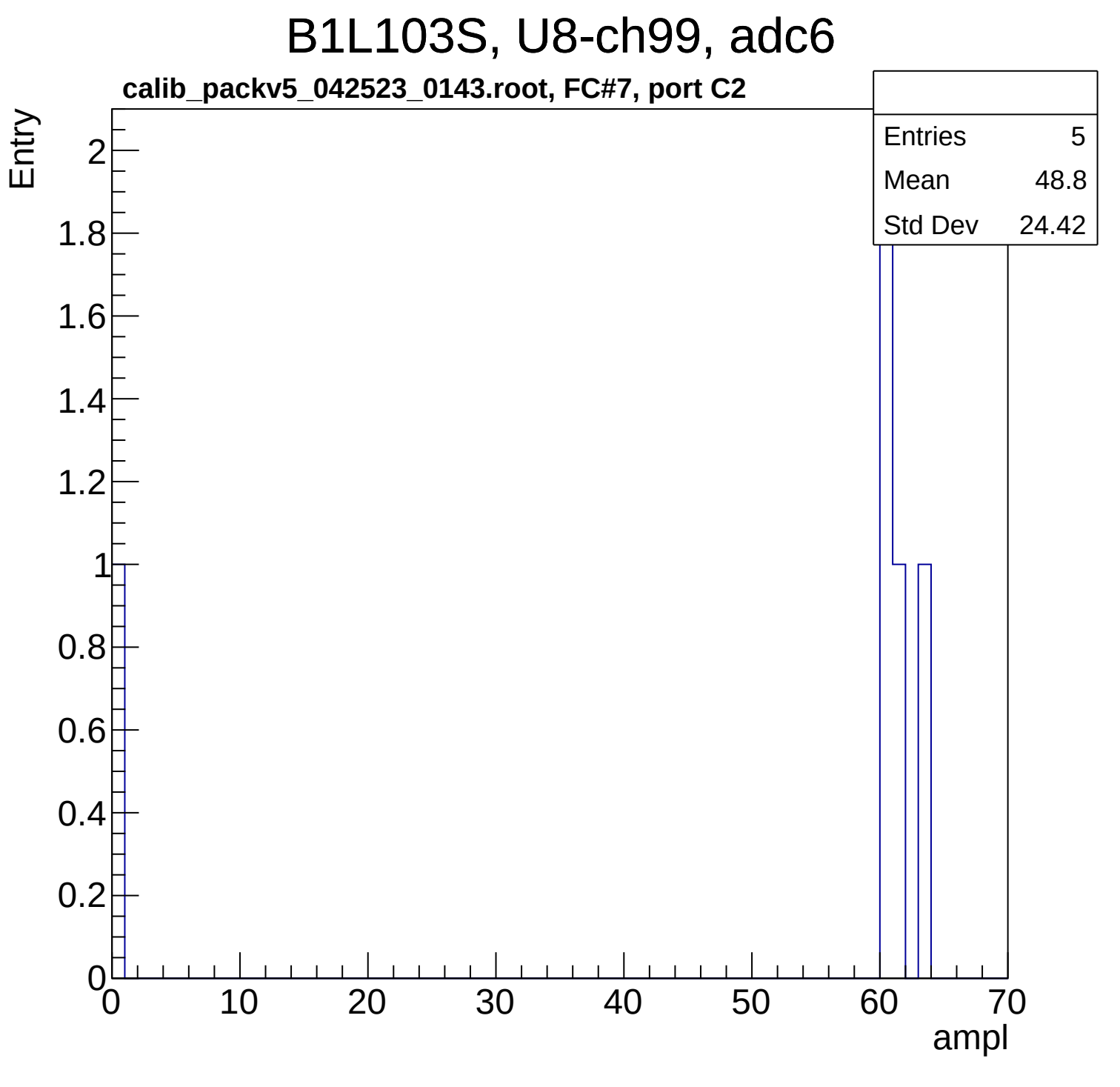

B1L103S, U8-ch99, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 36.71
Std Dev 3.212
Gaus mean : 37.4836
Gaus Width: 3.7872
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

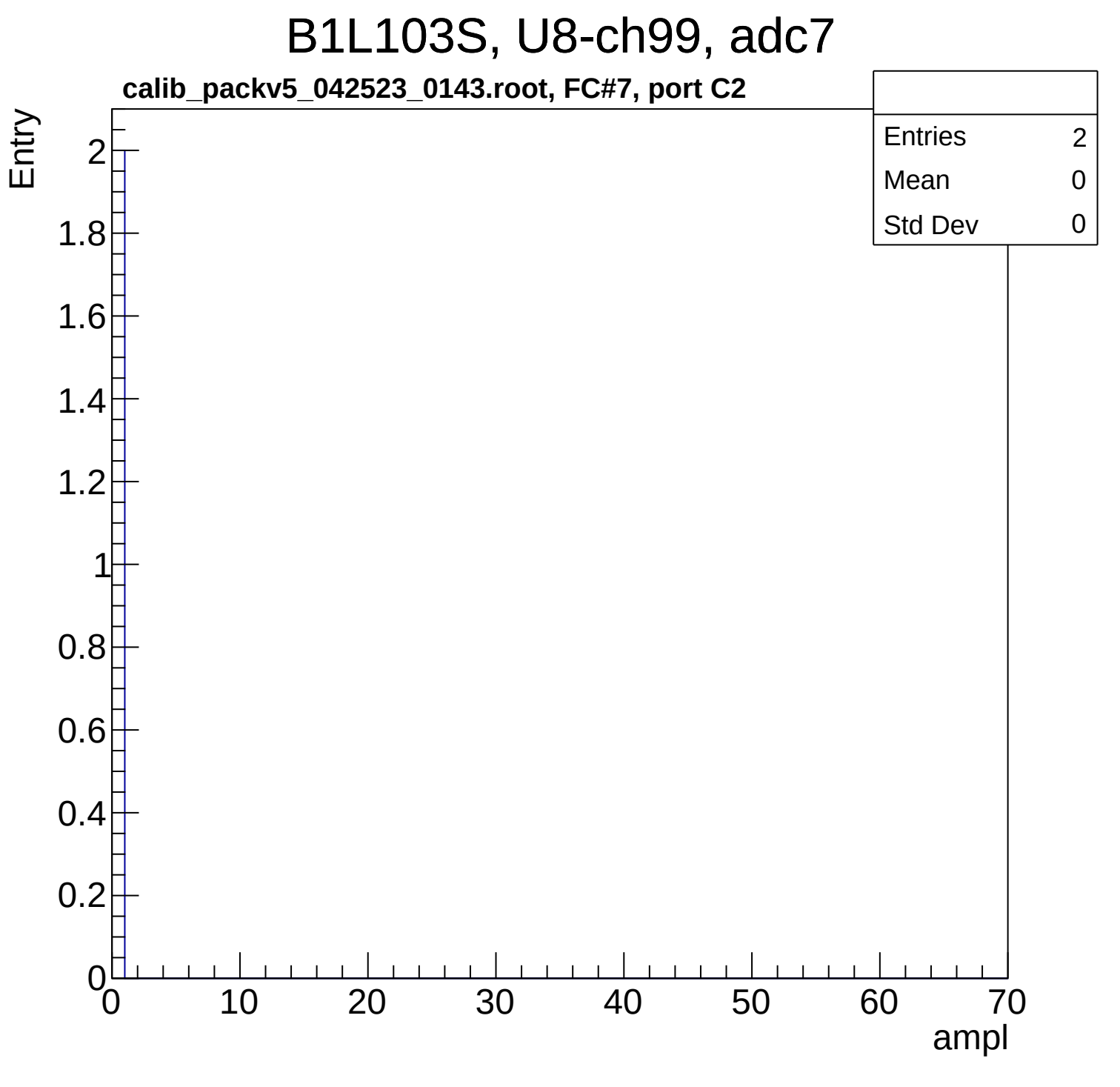

B1L103S, U8-ch99, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 44.16
Std Dev 3.299
Gaus mean : 44.7266
Gaus Width: 3.3342
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

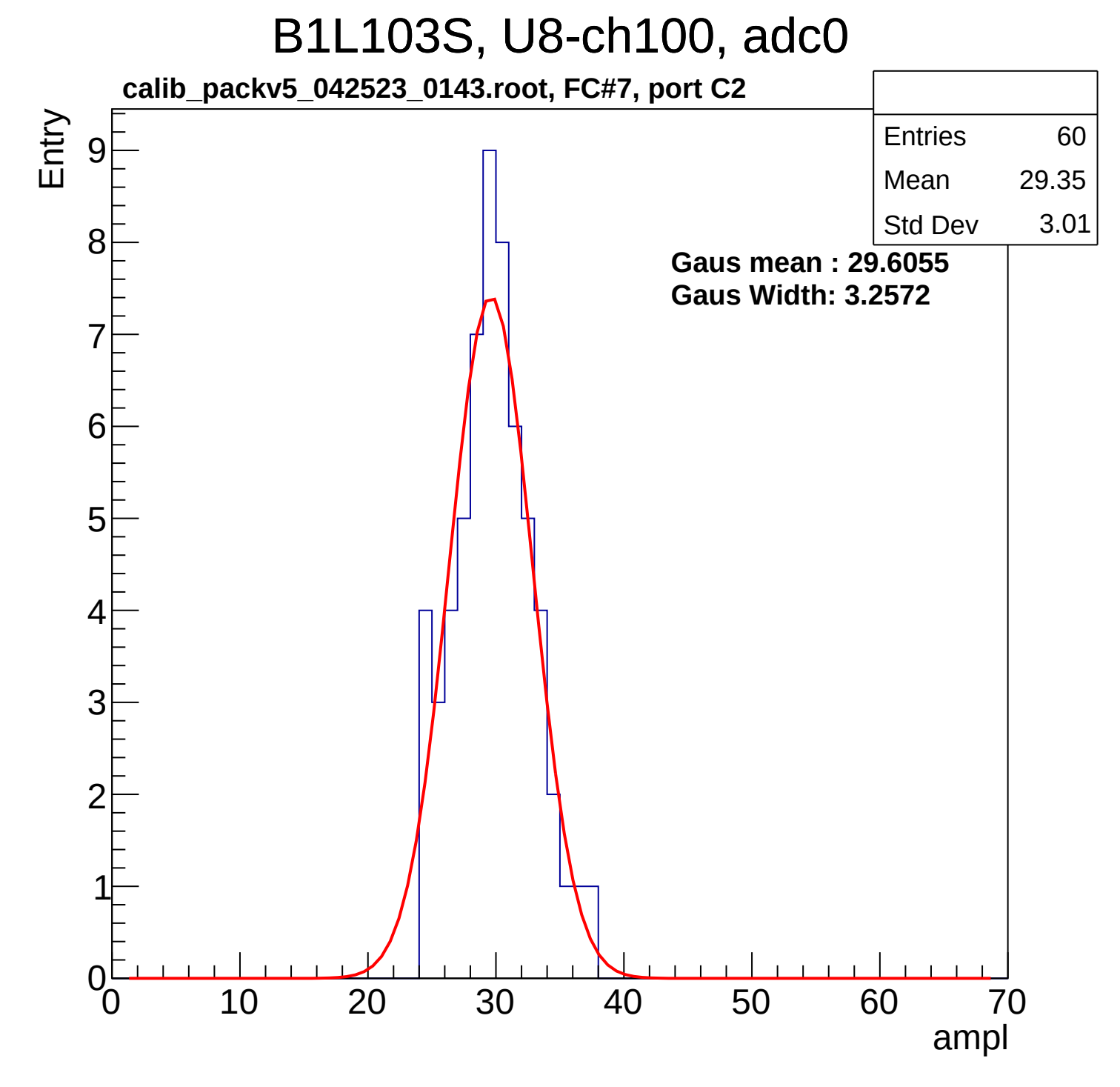

B1L103S, U8-ch99, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 50.07
Std Dev 3.401
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

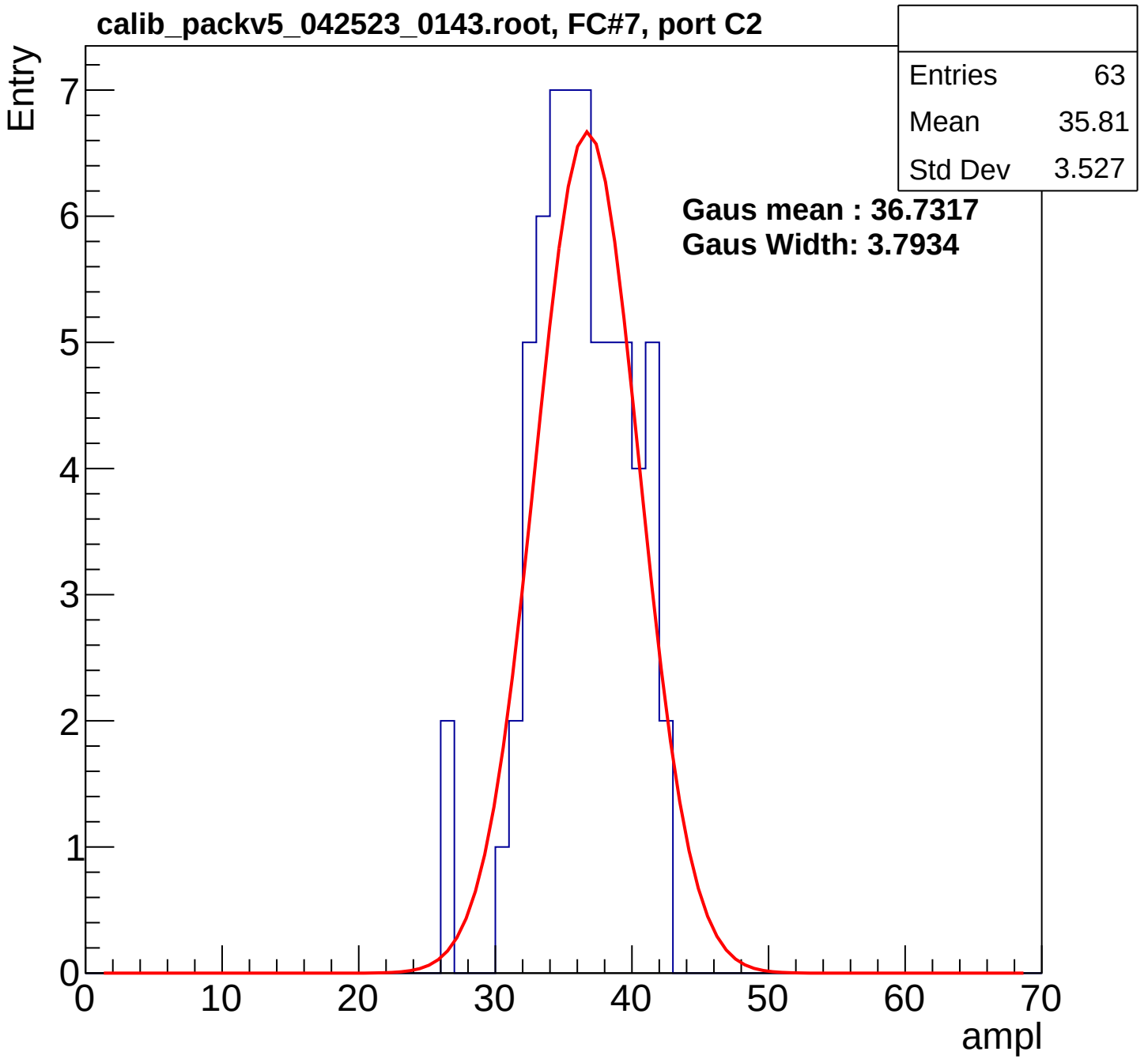

B1L103S, U8-ch99, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 56.05
Std Dev 3.251
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

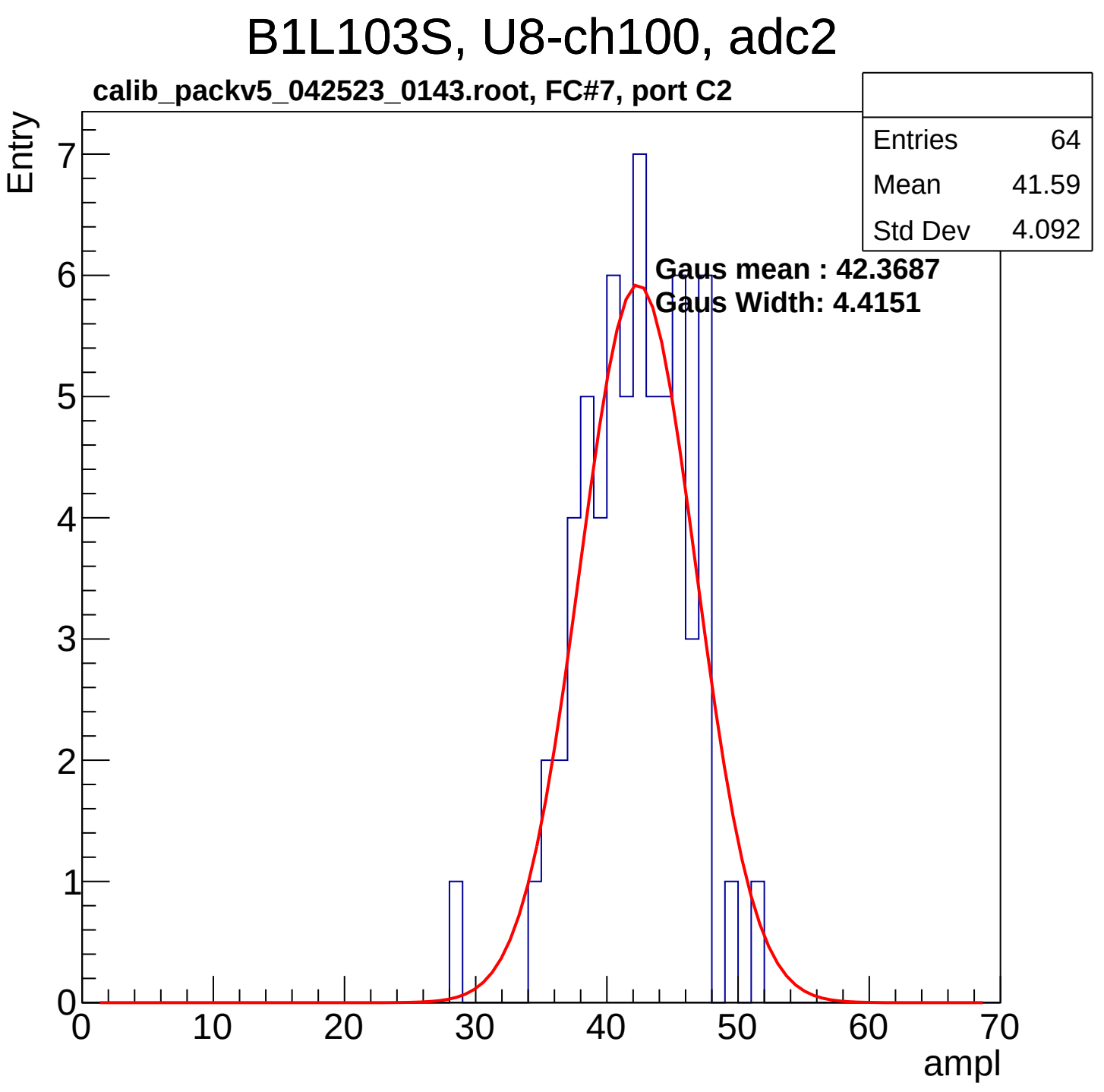

B1L103S, U8-ch99, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 37
Mean 60.57
Std Dev 2.261
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

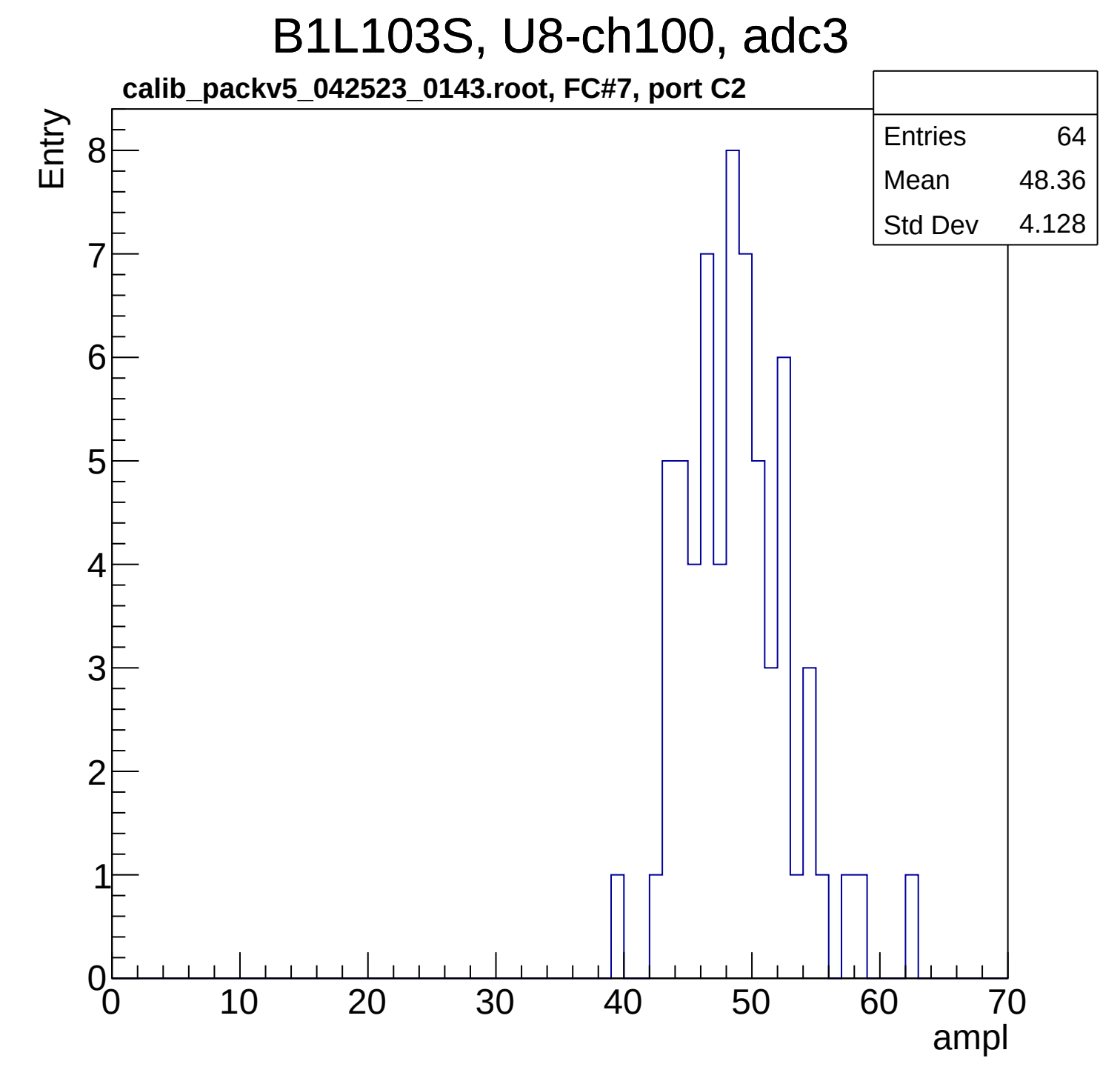

B1L103S, U8-ch99, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 48.8
Std Dev 24.42
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

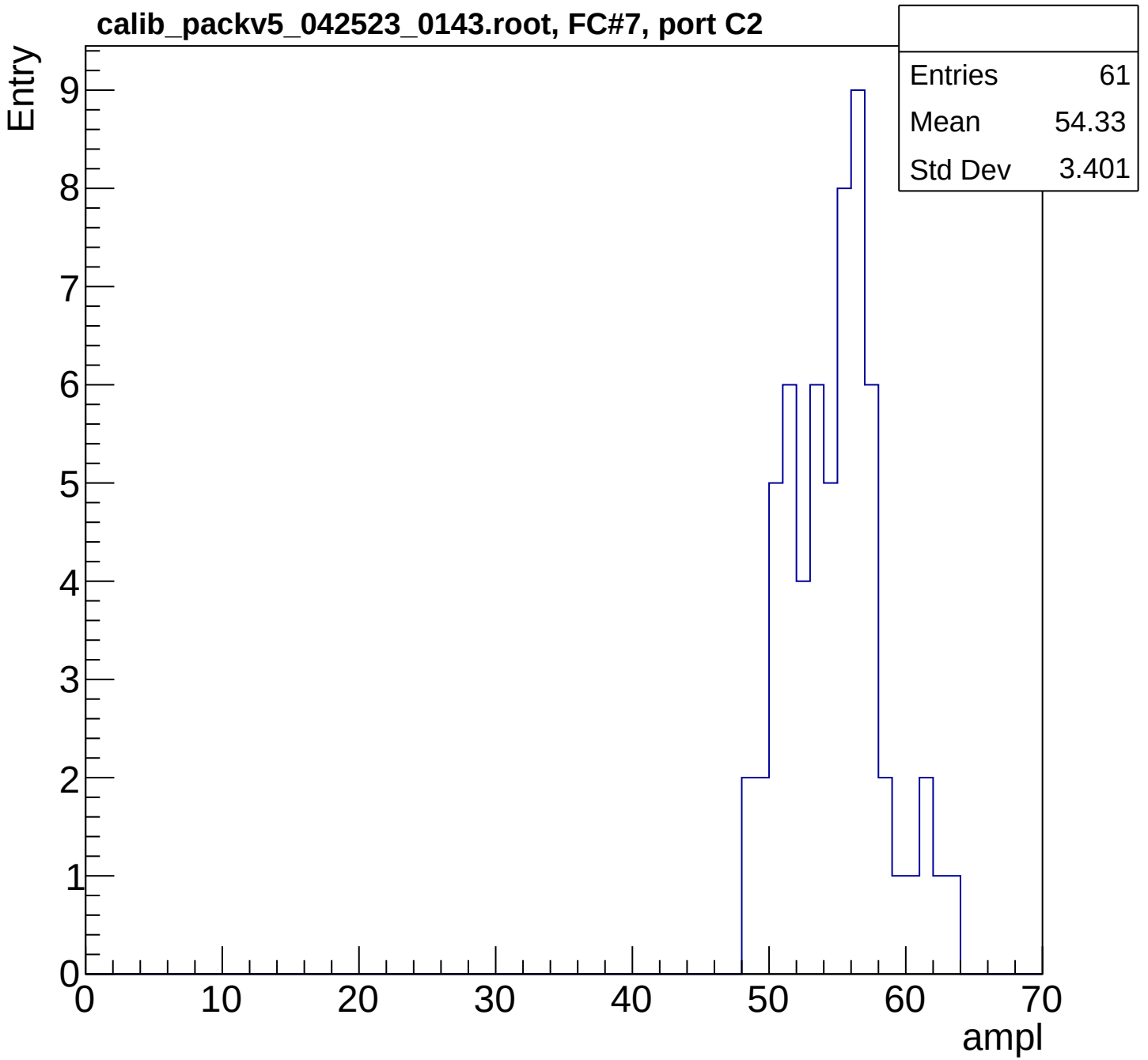

B1L103S, U8-ch99, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

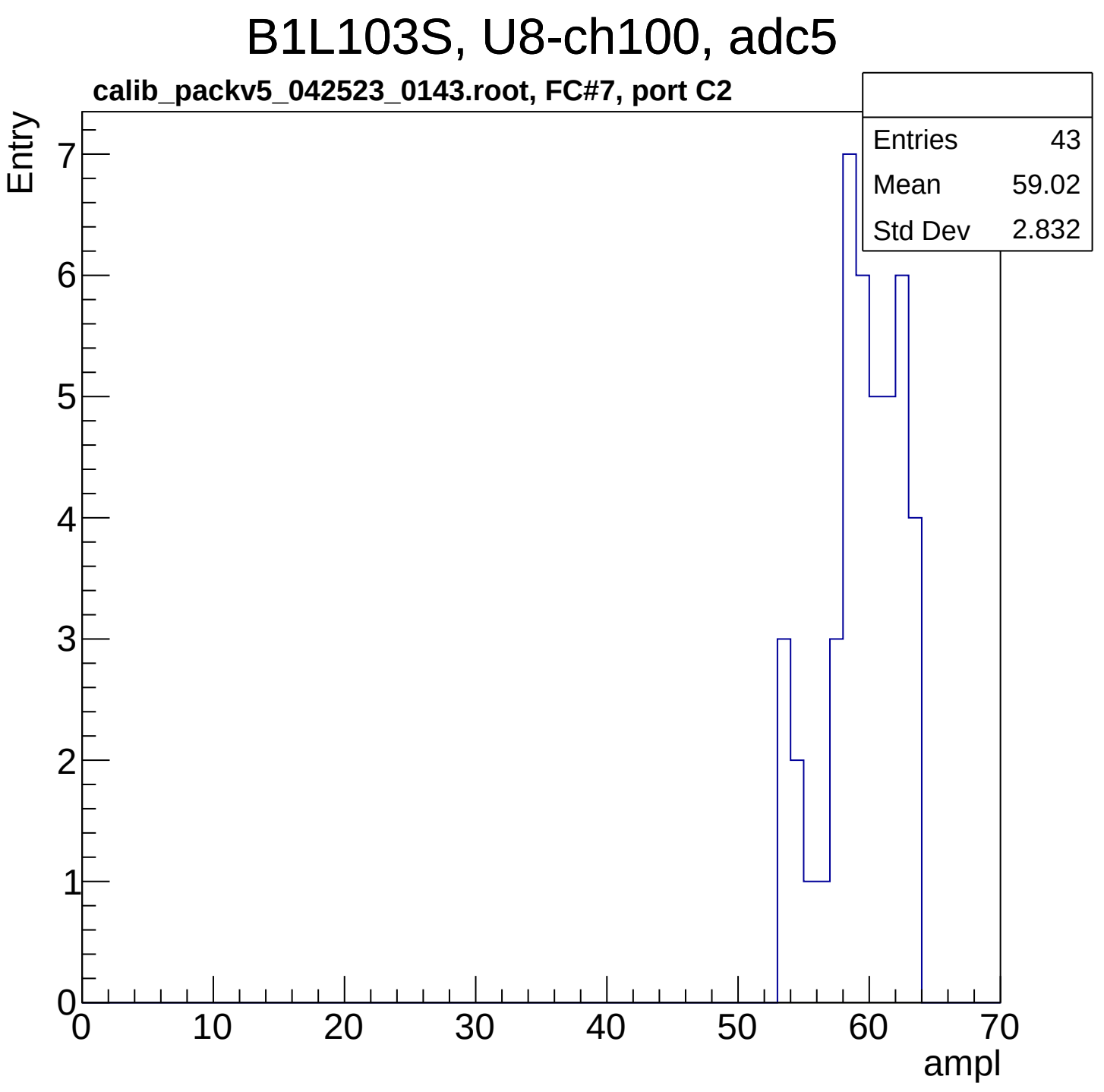

B1L103S, U8-ch100, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 29.35
Std Dev 3.01
Gaus mean : 29.6055
Gaus Width: 3.2572
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

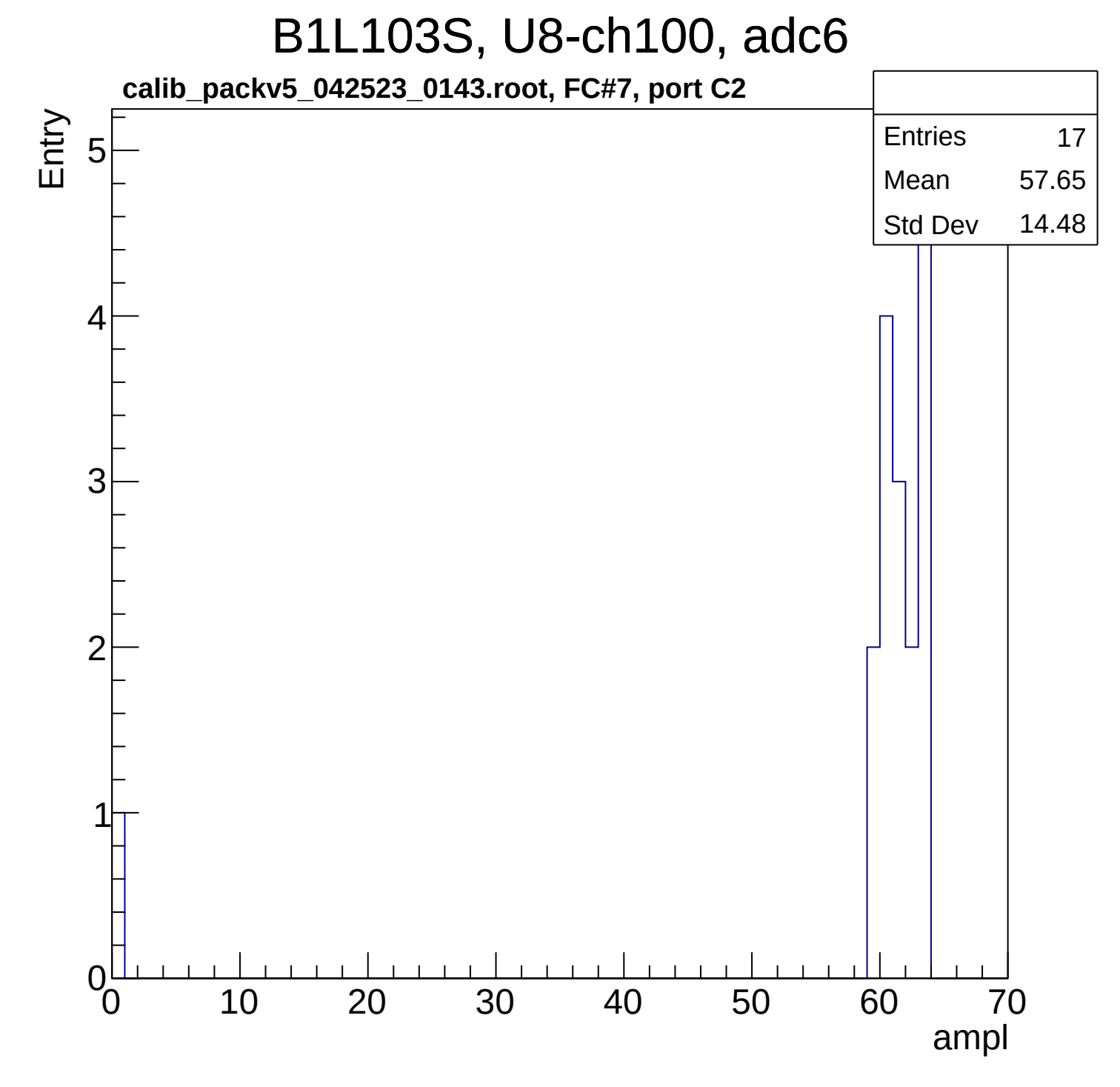

B1L103S, U8-ch100, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 35.81
Std Dev 3.527
Gaus mean : 36.7317
Gaus Width: 3.7934
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

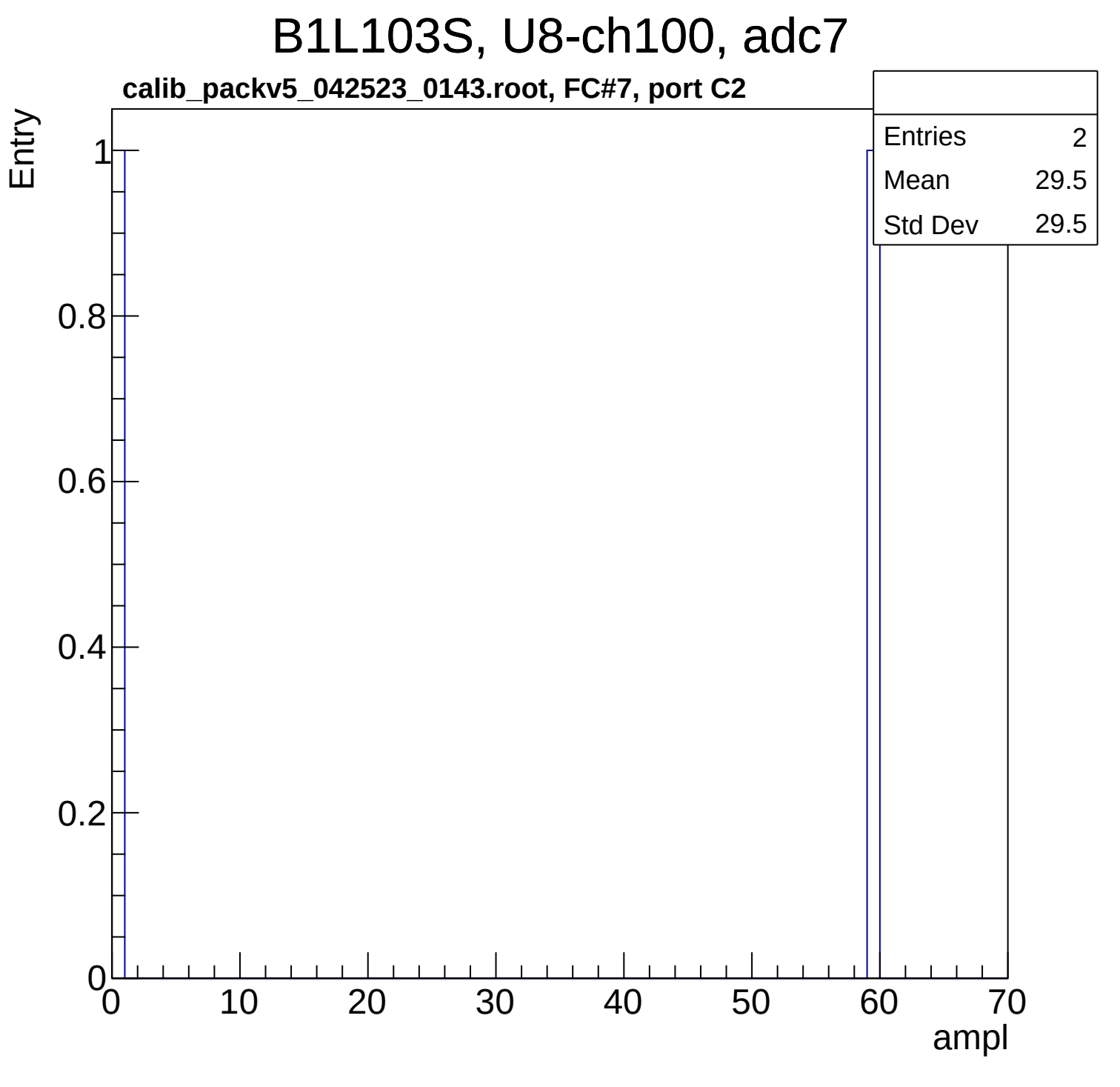

B1L103S, U8-ch100, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 41.59
Std Dev 4.092
Gaus mean : 42.3687
Gaus Width: 4.4151
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

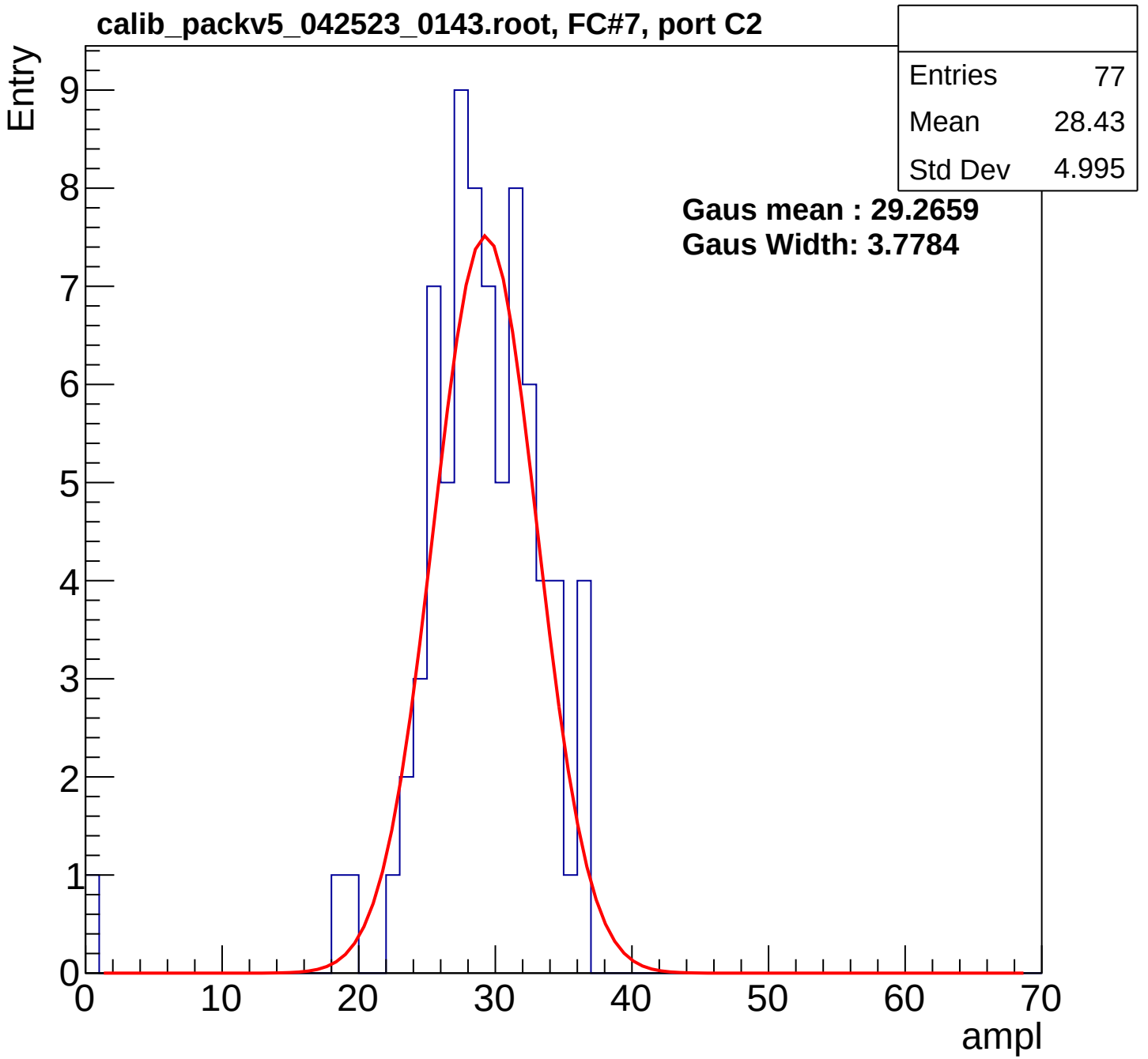

B1L103S, U8-ch100, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 48.36
Std Dev 4.128
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

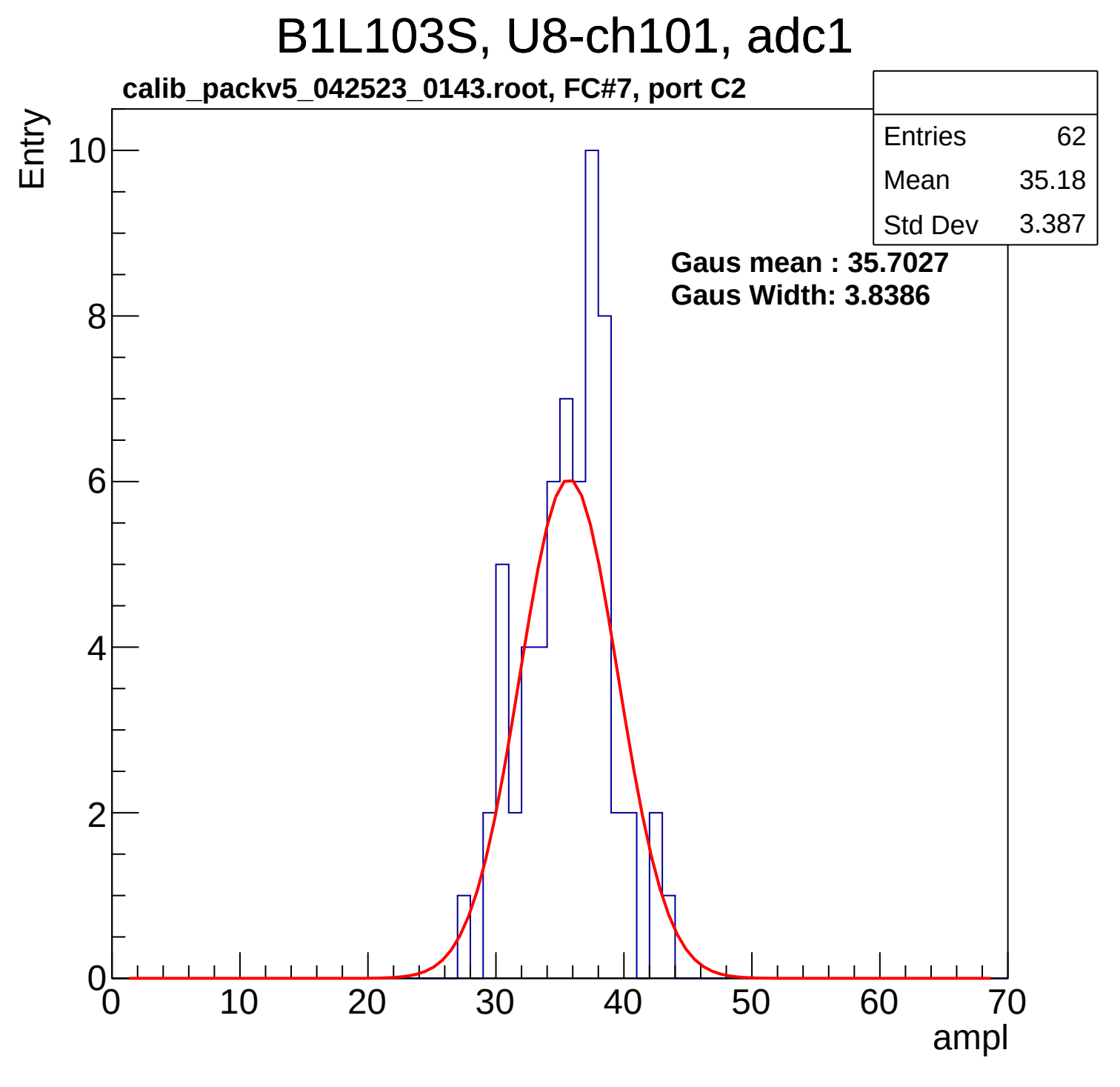

B1L103S, U8-ch100, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 54.33
Std Dev 3.401
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

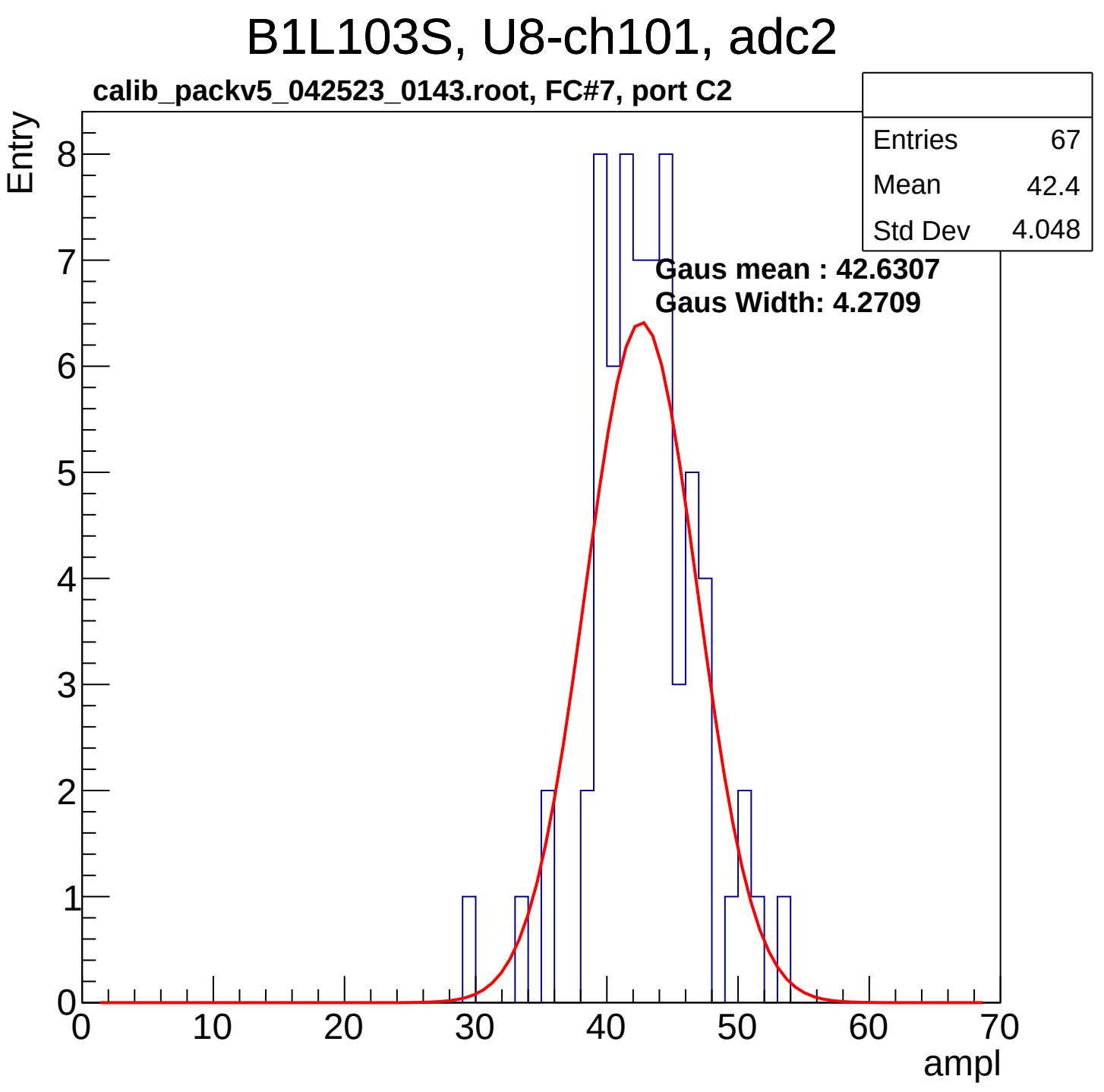

B1L103S, U8-ch100, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 43
Mean 59.02
Std Dev 2.832
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

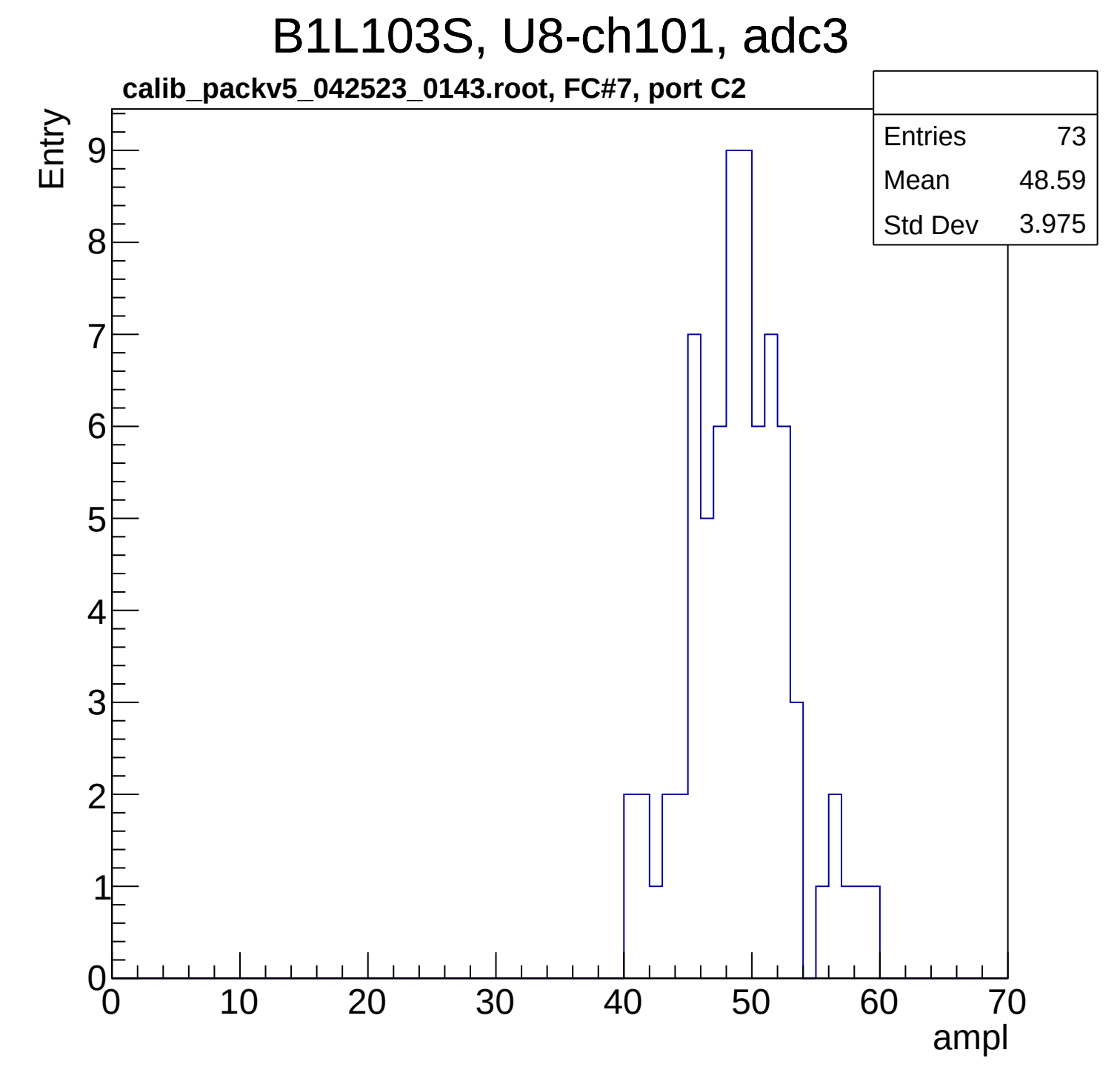

B1L103S, U8-ch100, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 17
Mean 57.65
Std Dev 14.48
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

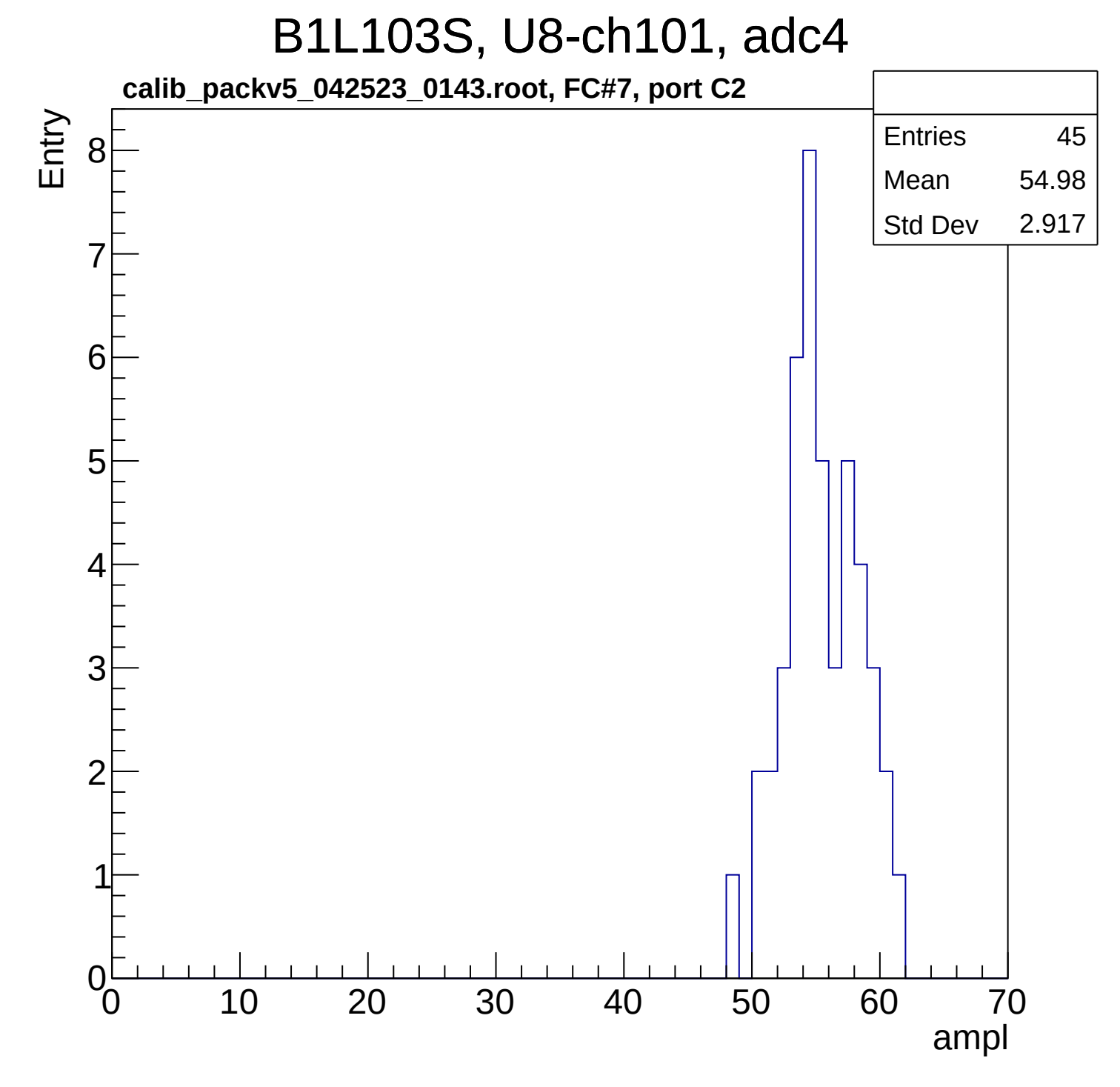

B1L103S, U8-ch100, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 29.5
Std Dev 29.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

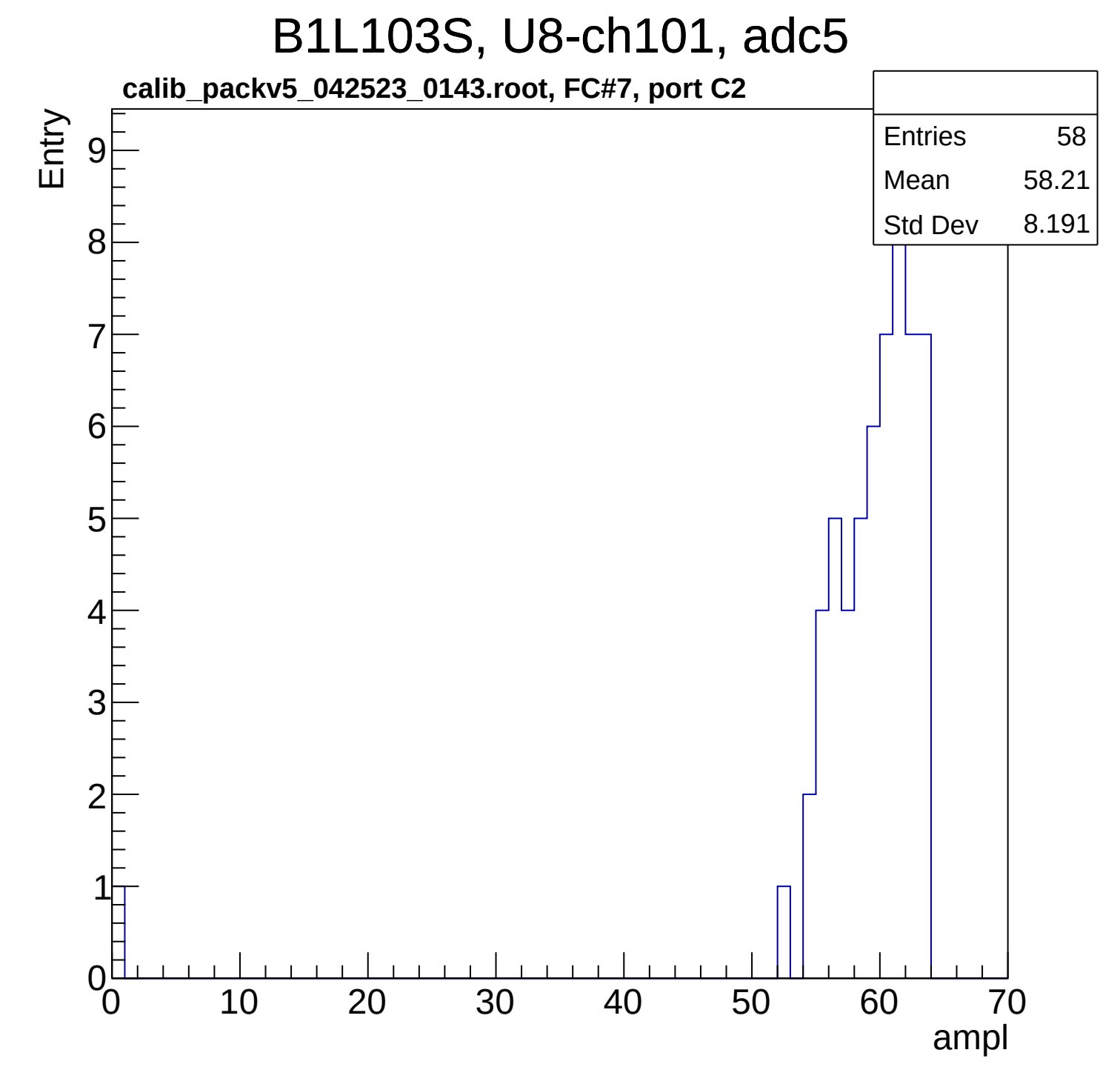

B1L103S, U8-ch101, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 28.43
Std Dev 4.995
Gaus mean : 29.2659
Gaus Width: 3.7784
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

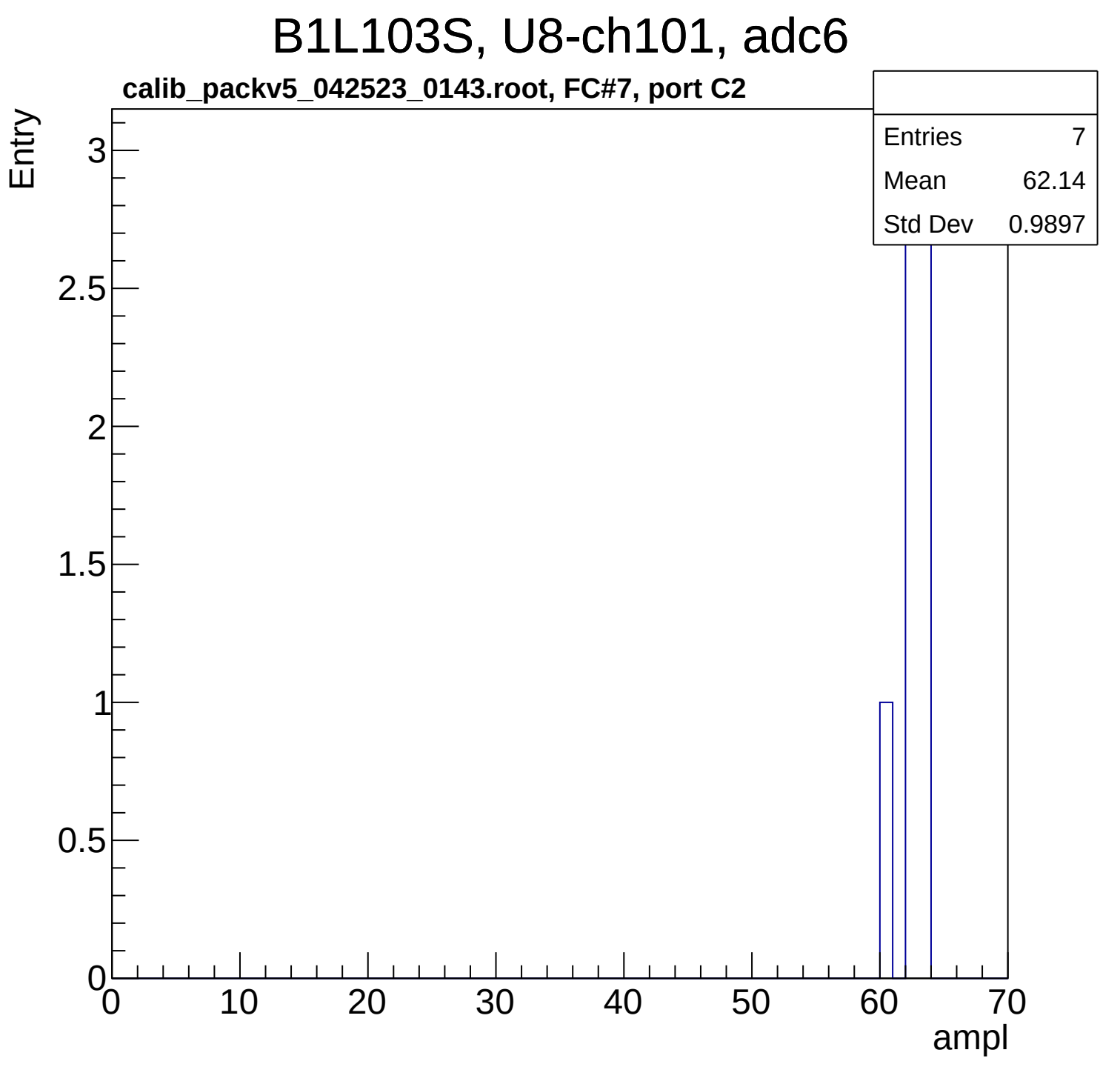

B1L103S, U8-ch101, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 35.18
Std Dev 3.387
Gaus mean : 35.7027
Gaus Width: 3.8386
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

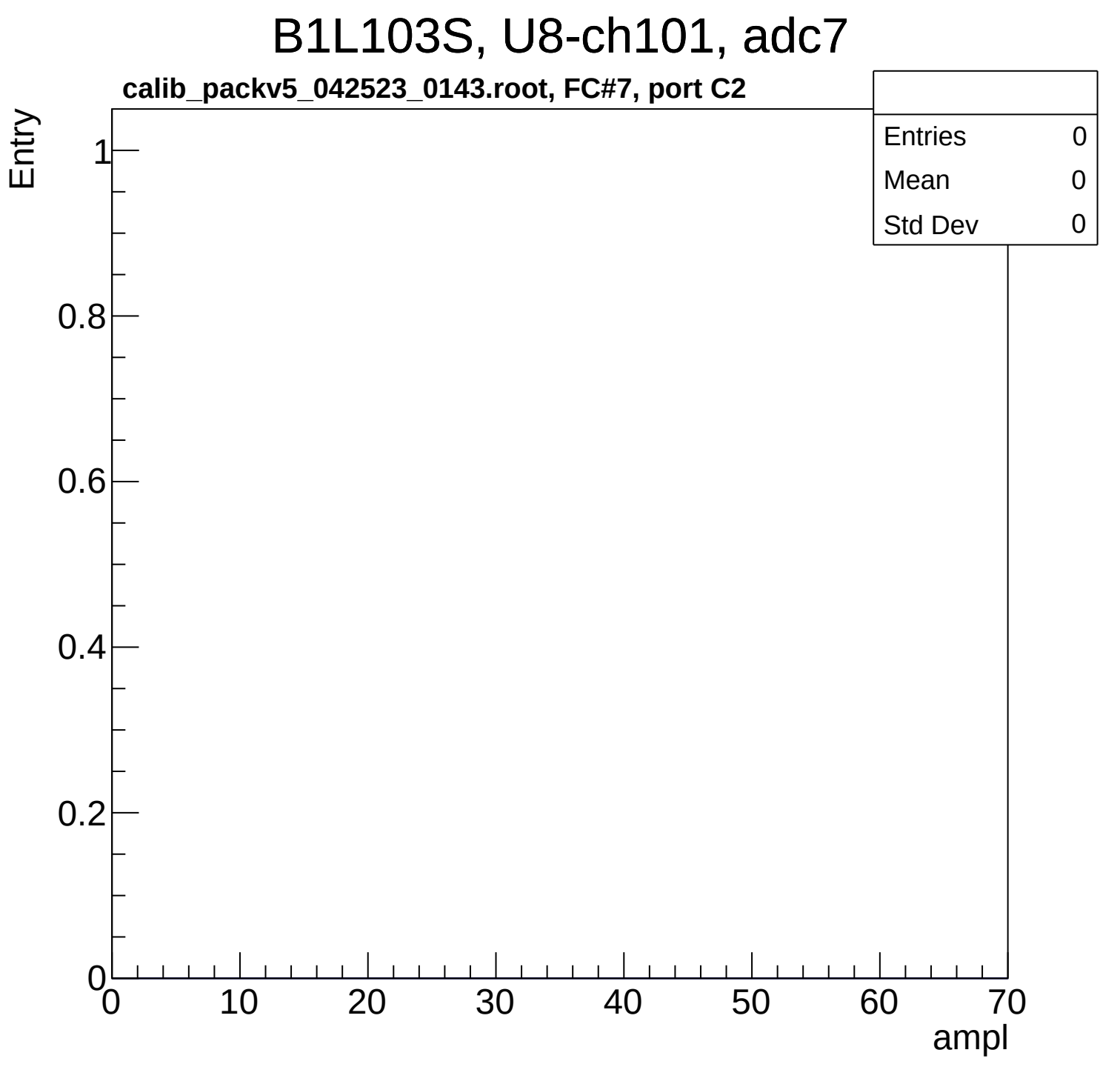

B1L103S, U8-ch101, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 42.4
Std Dev 4.048
Gaus mean : 42.6307
Gaus Width: 4.2709
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

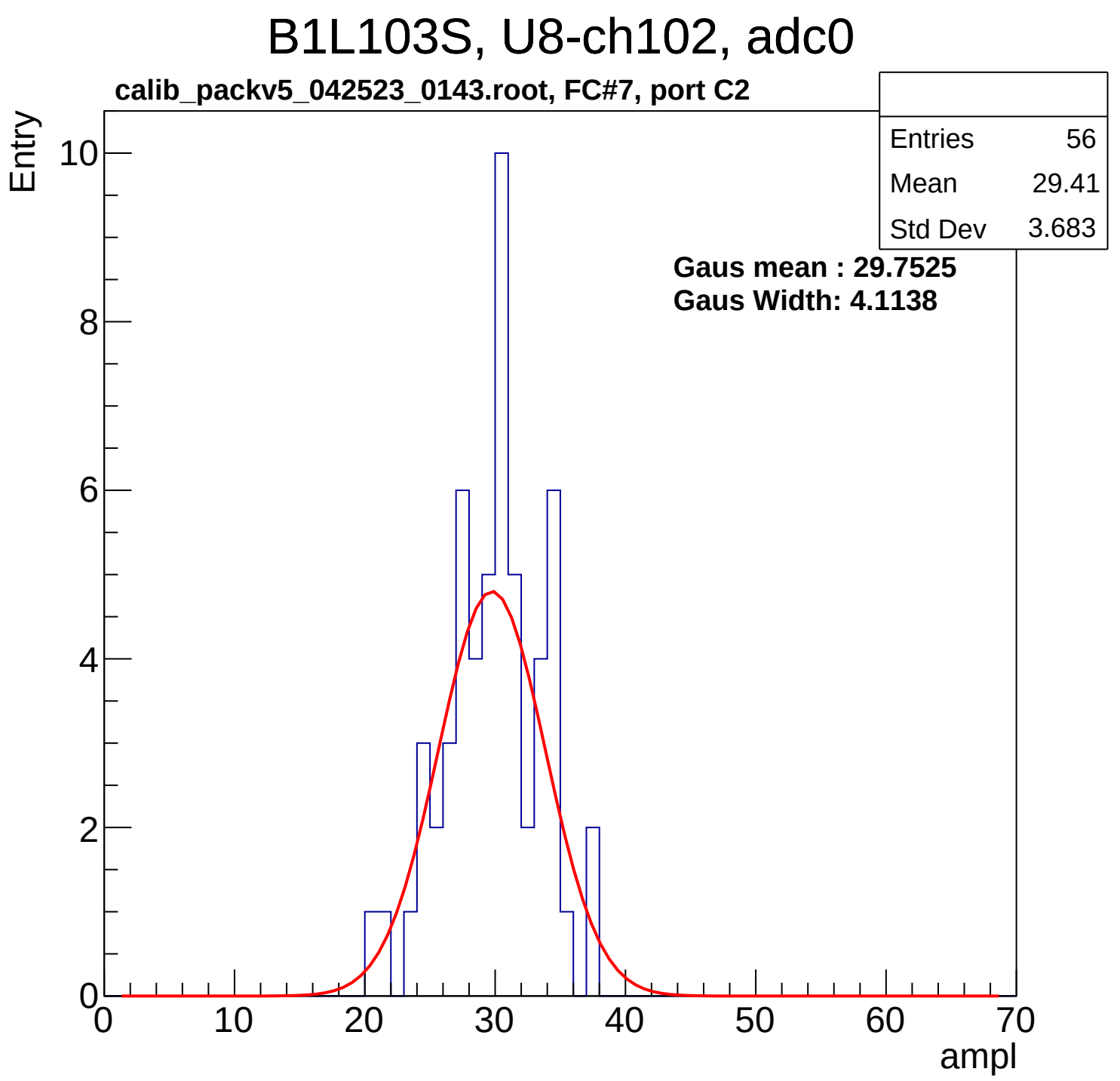

B1L103S, U8-ch101, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 48.59
Std Dev 3.975
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

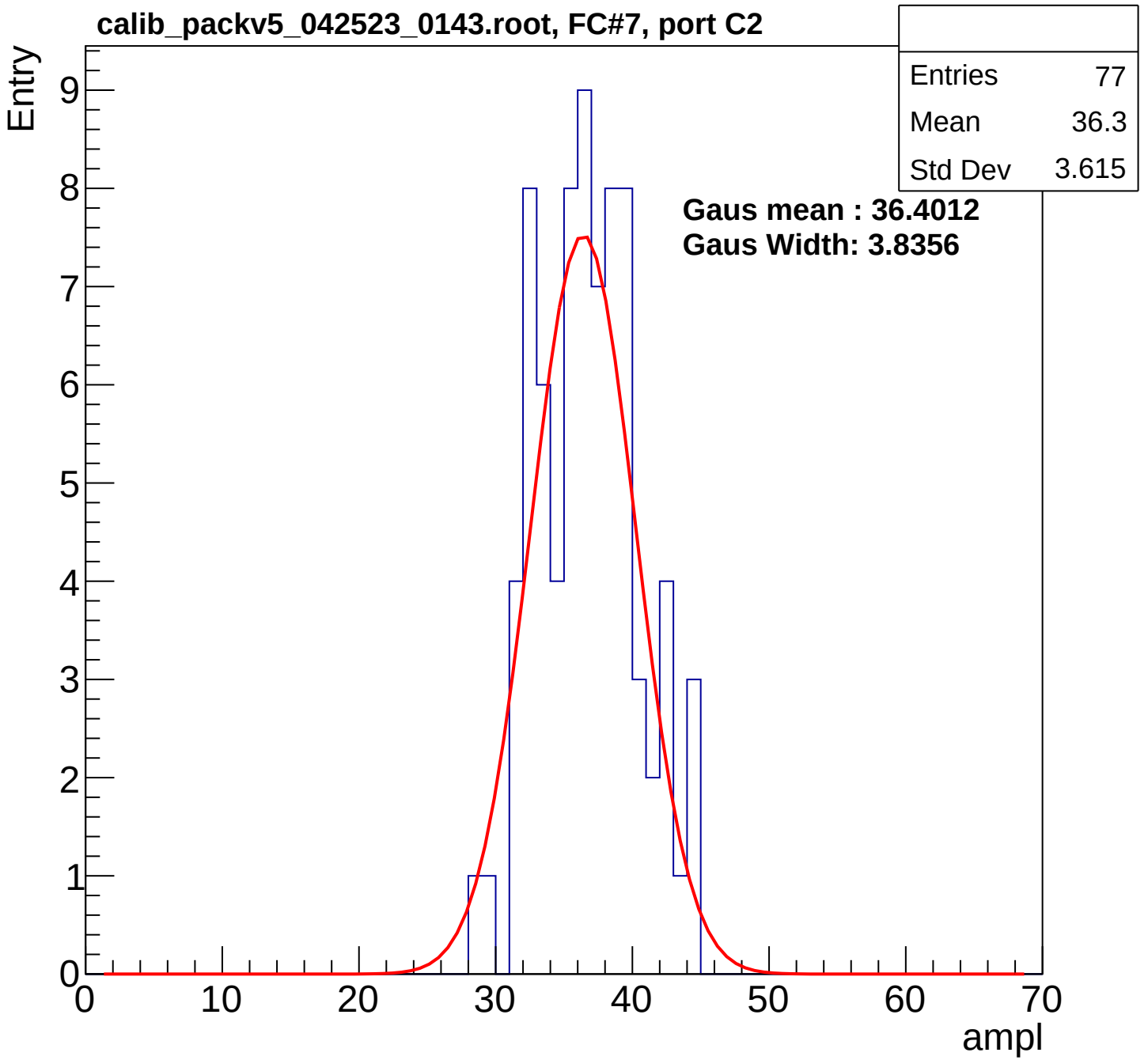

B1L103S, U8-ch101, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 45
Mean 54.98
Std Dev 2.917
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

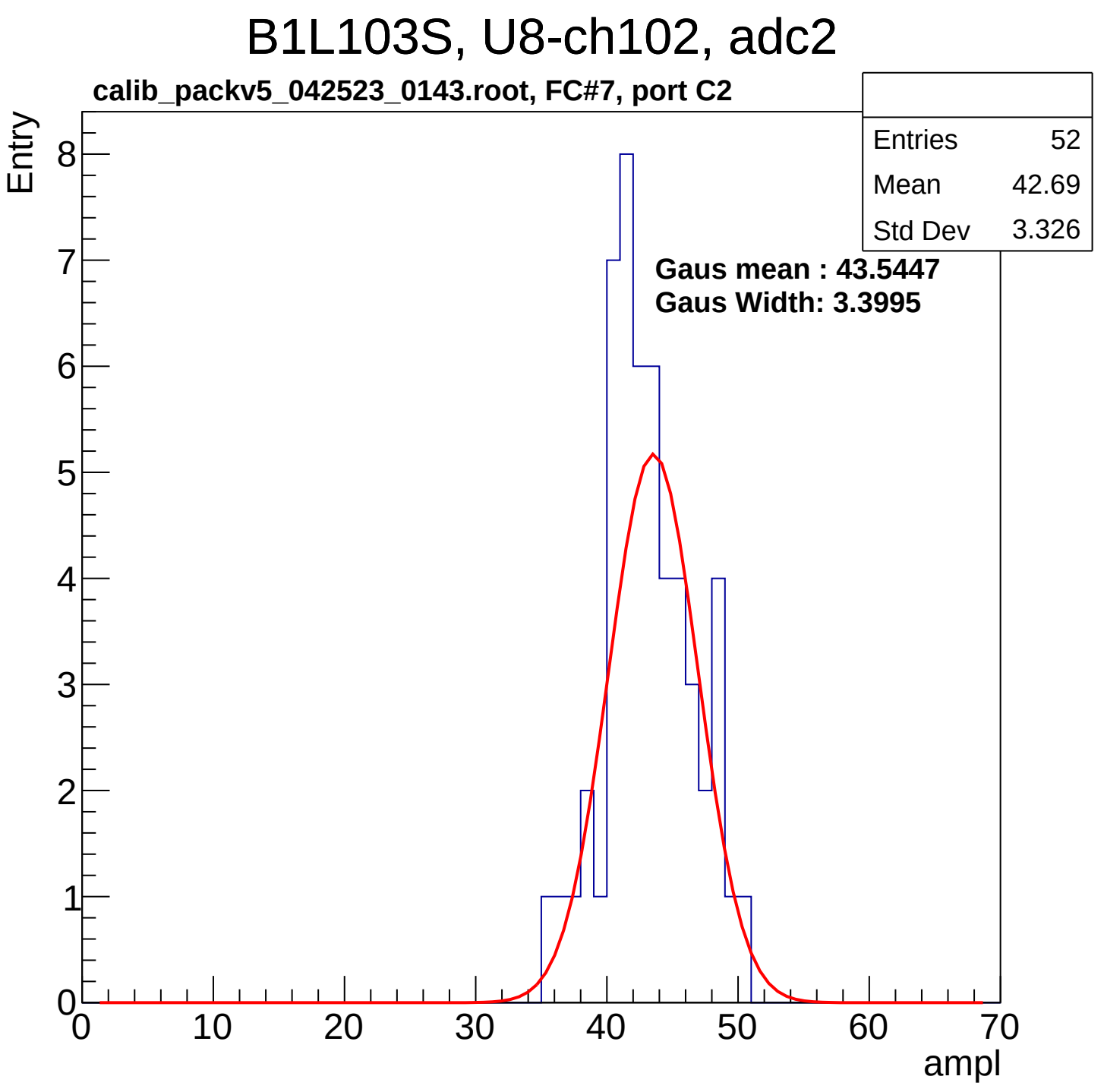

B1L103S, U8-ch101, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 58.21
Std Dev 8.191
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

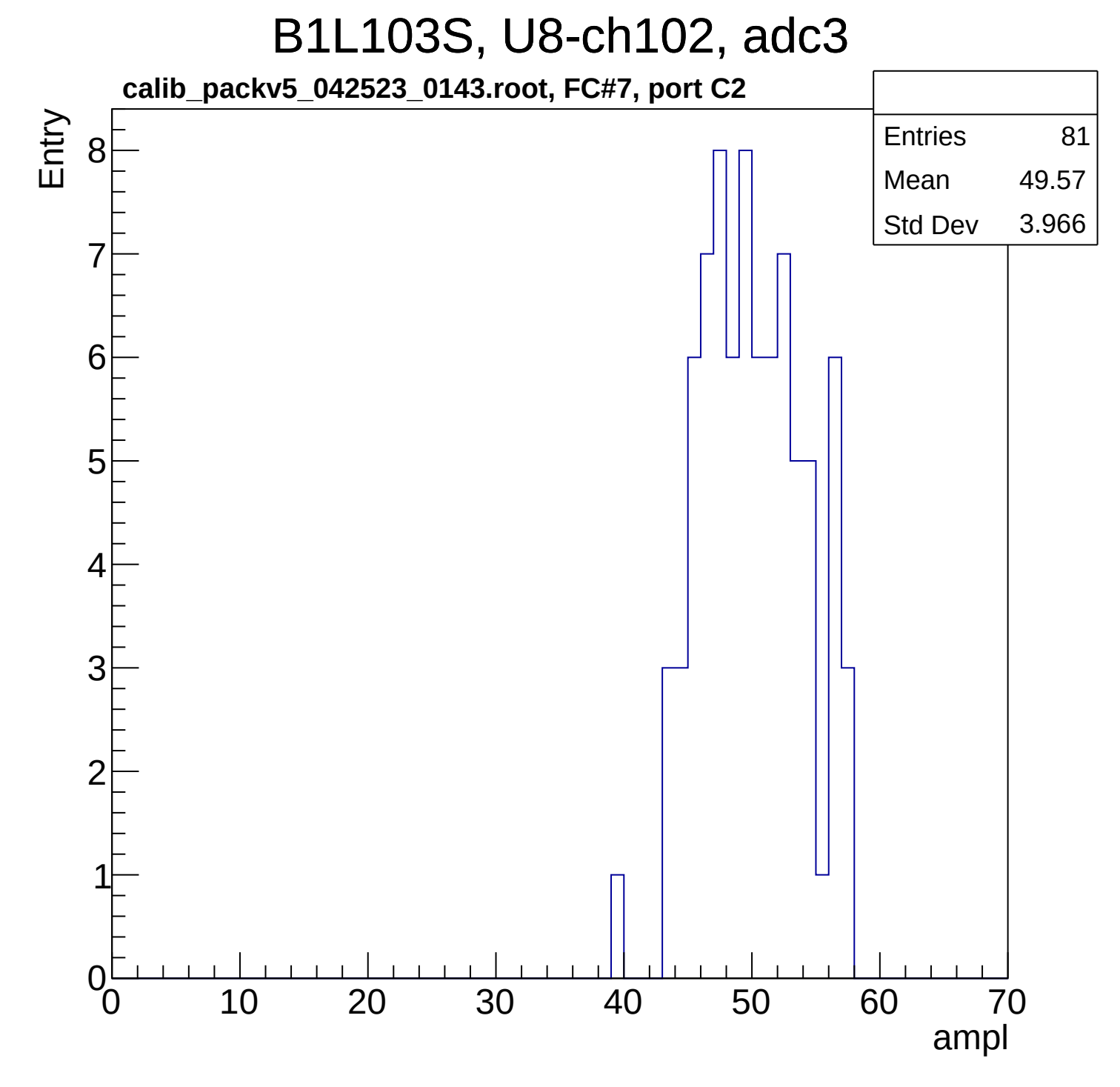

B1L103S, U8-ch101, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 7
Mean 62.14
Std Dev 0.9897
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

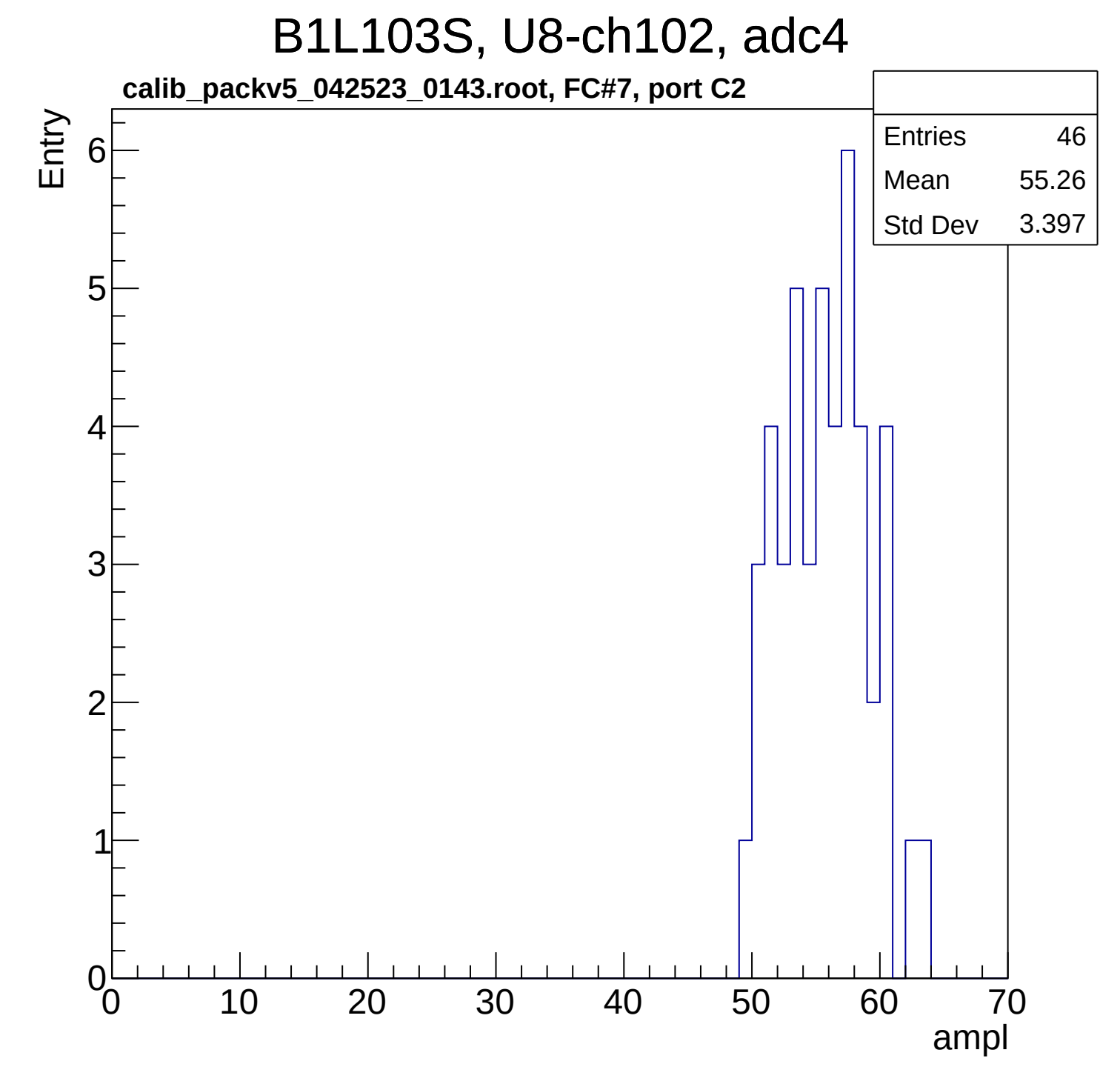

B1L103S, U8-ch101, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

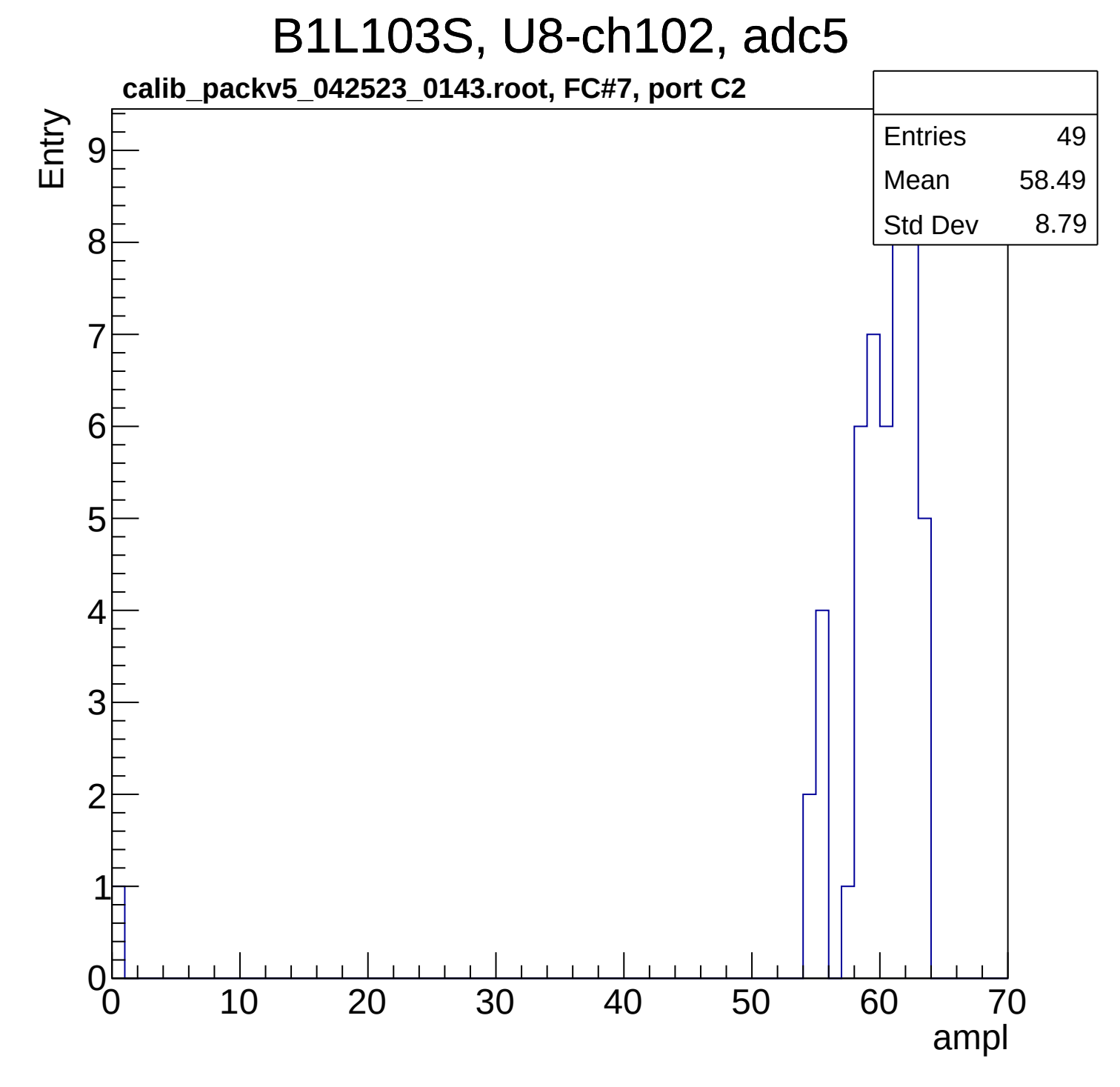

B1L103S, U8-ch102, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 29.41
Std Dev 3.683
Gaus mean : 29.7525
Gaus Width: 4.1138
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

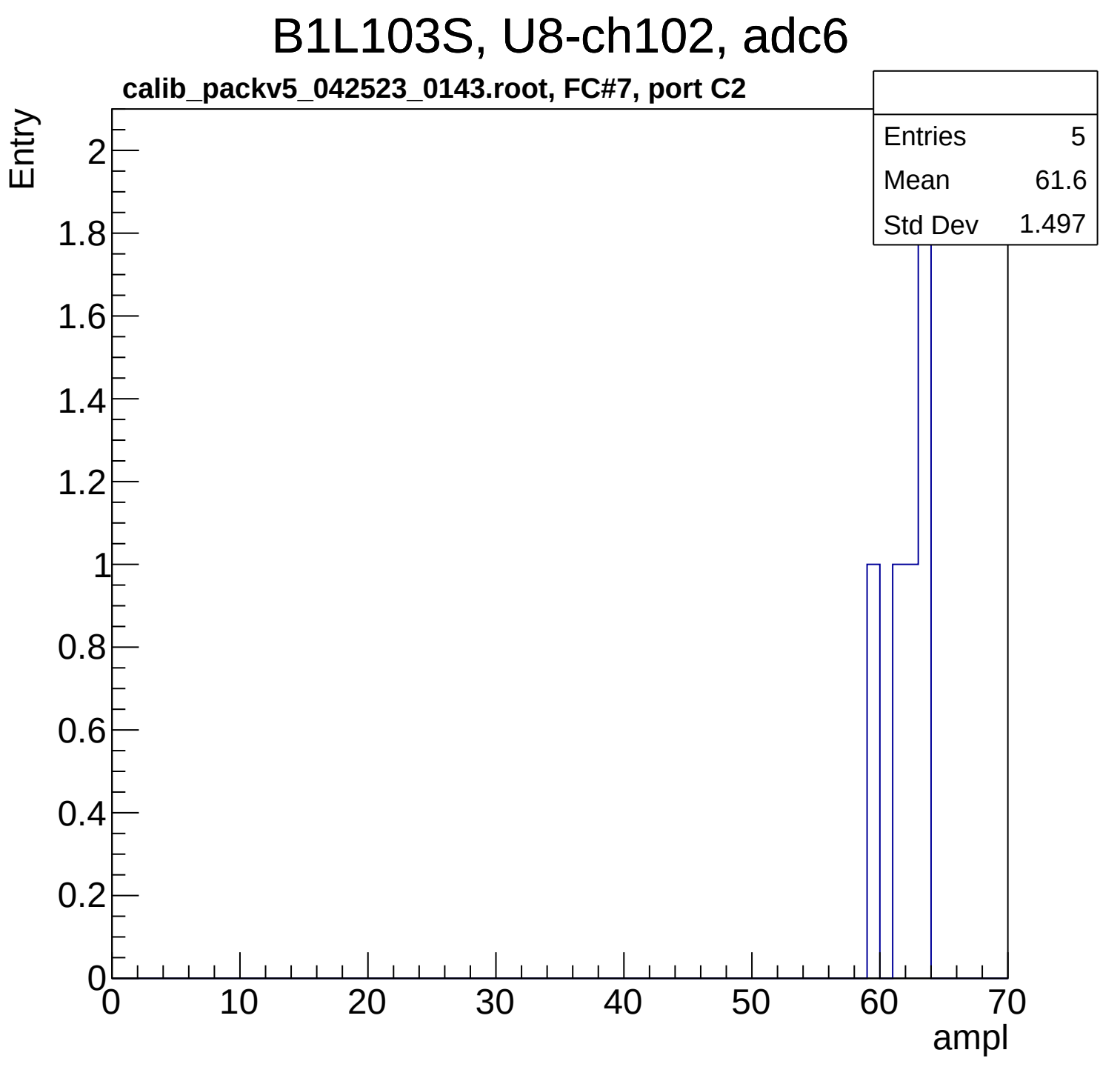

B1L103S, U8-ch102, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 36.3
Std Dev 3.615
Gaus mean : 36.4012
Gaus Width: 3.8356
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

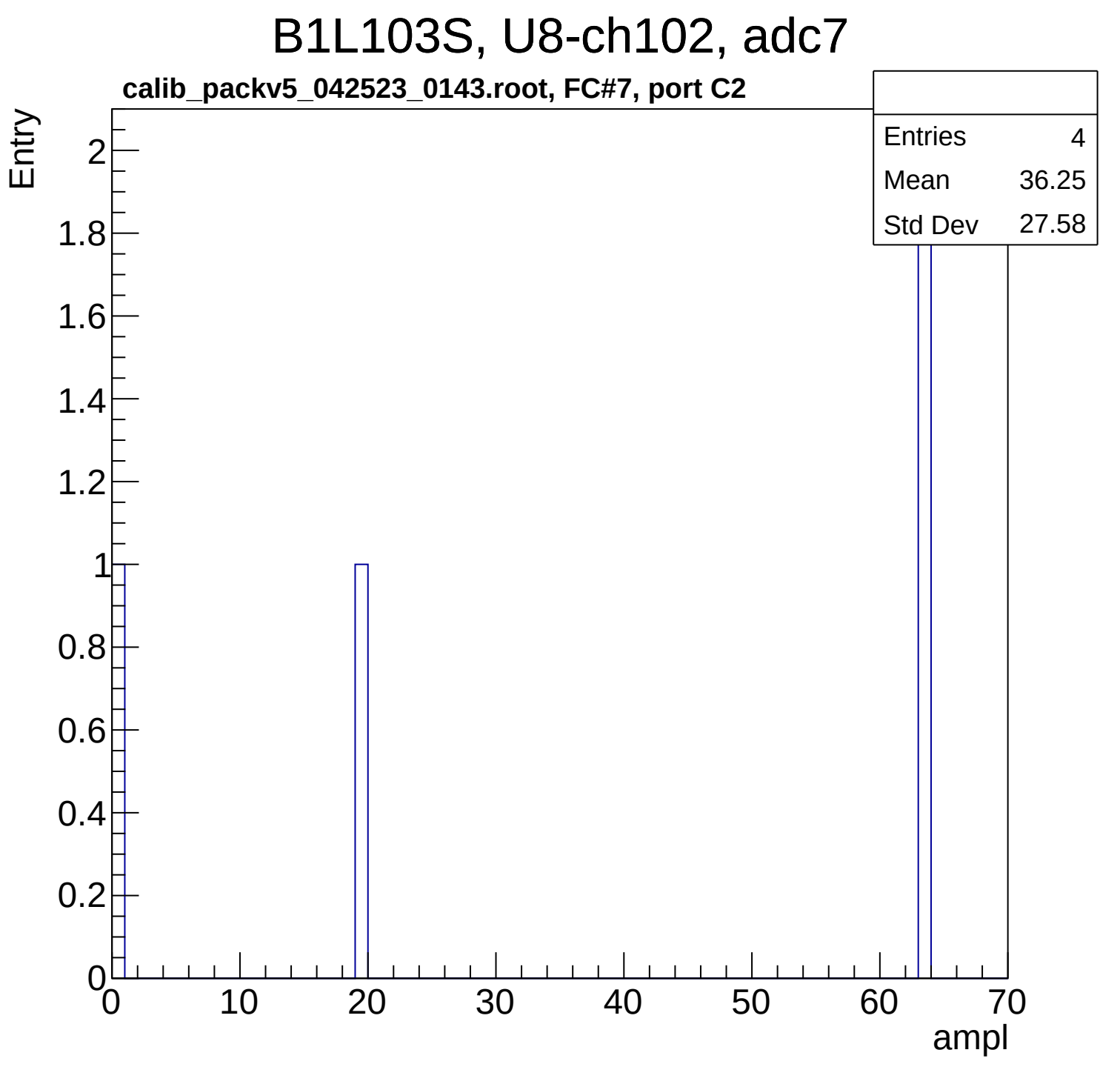

B1L103S, U8-ch102, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 42.69
Std Dev 3.326
Gaus mean : 43.5447
Gaus Width: 3.3995
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

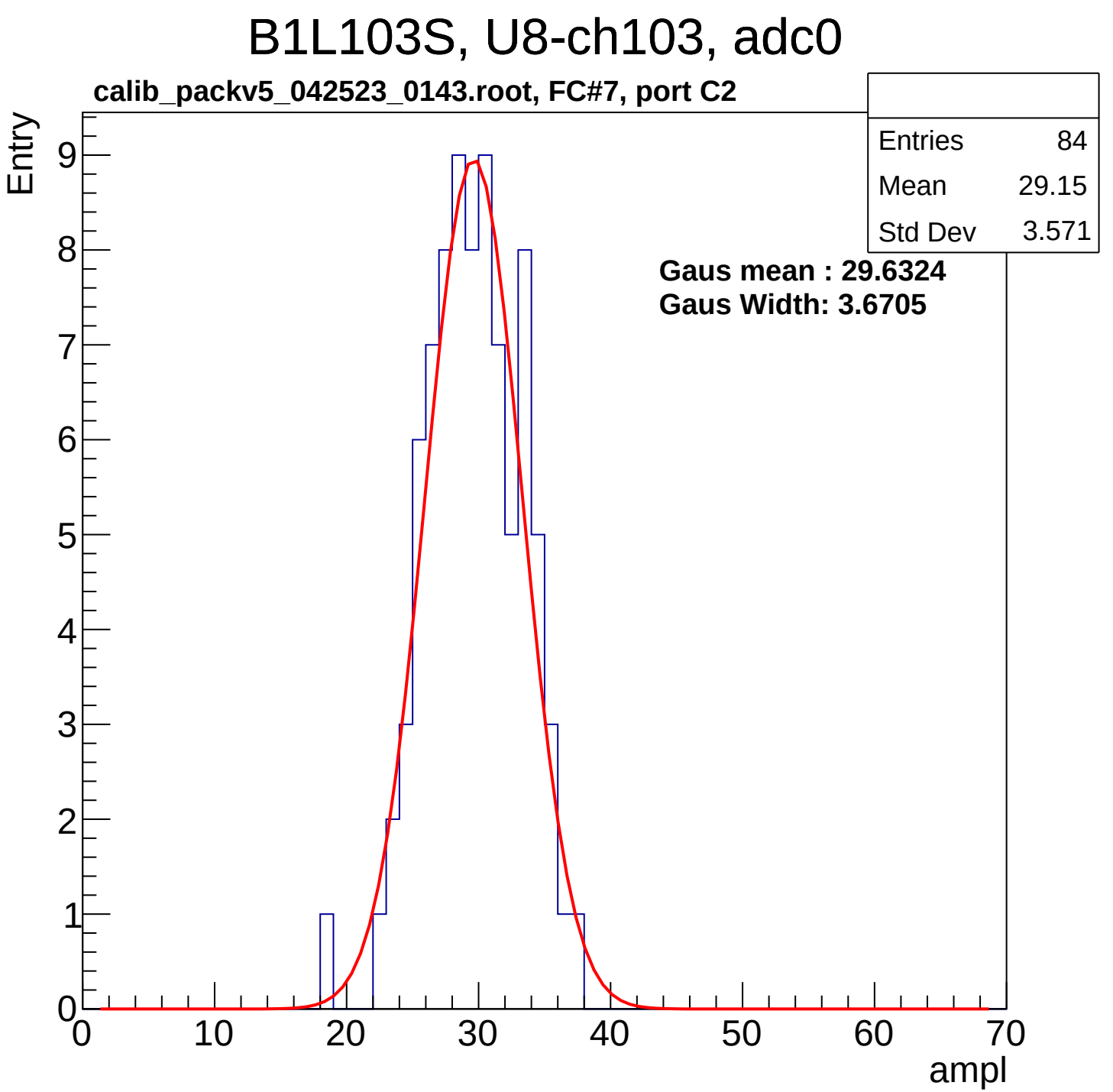

B1L103S, U8-ch102, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 81
Mean 49.57
Std Dev 3.966
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

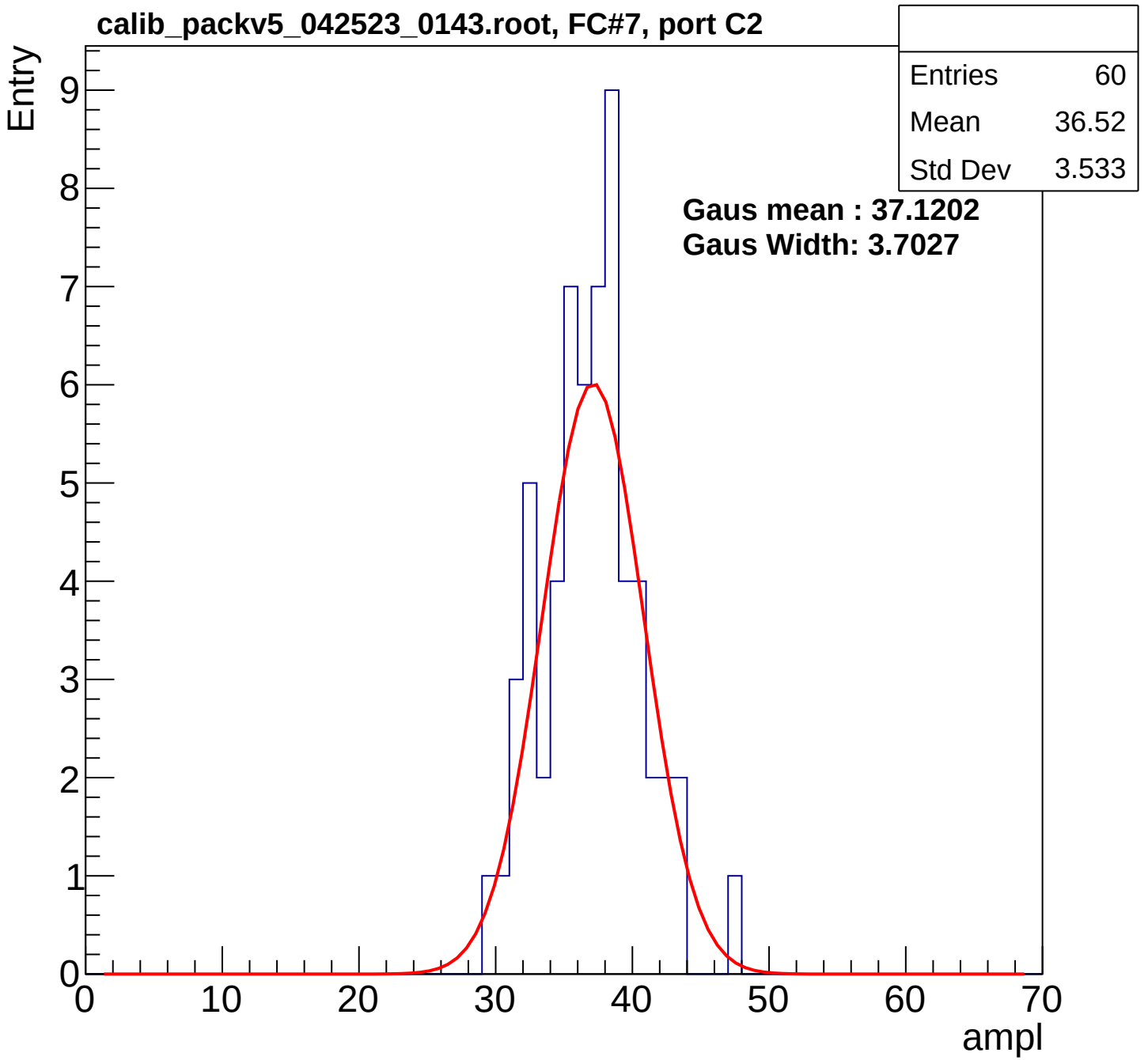

B1L103S, U8-ch102, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 46
Mean 55.26
Std Dev 3.397
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

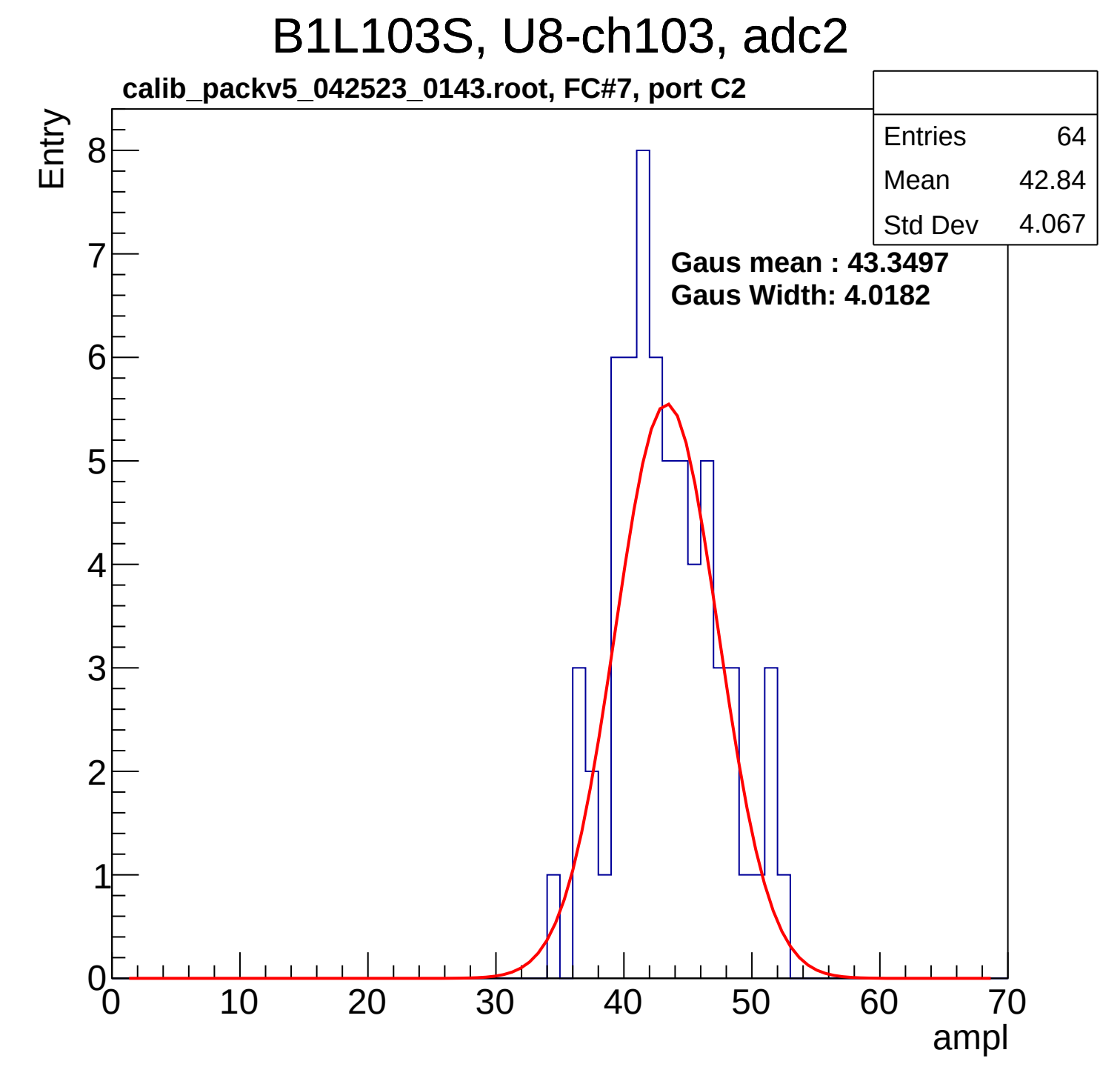

B1L103S, U8-ch102, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 58.49
Std Dev 8.79
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

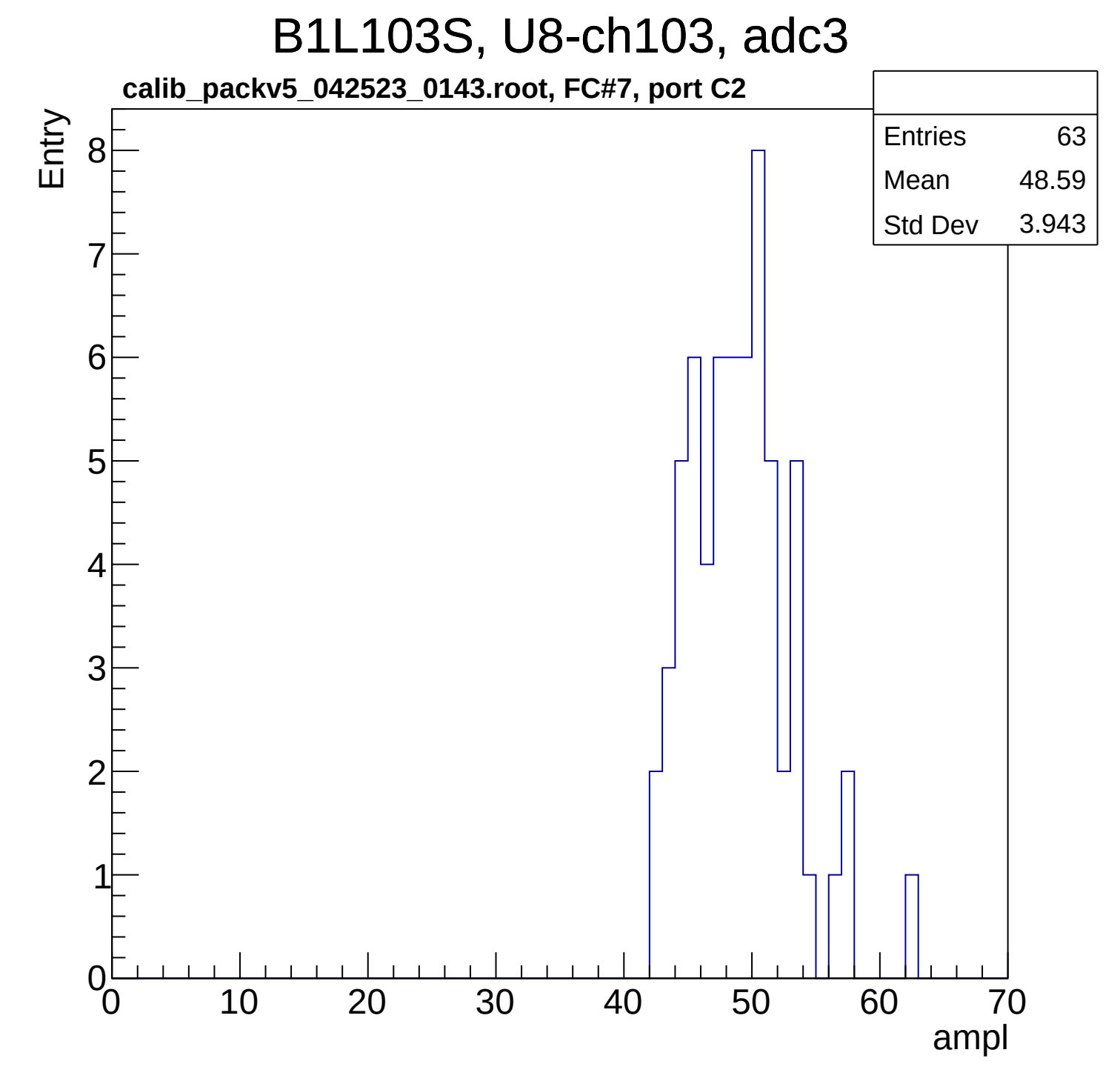

B1L103S, U8-ch102, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 61.6
Std Dev 1.497
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

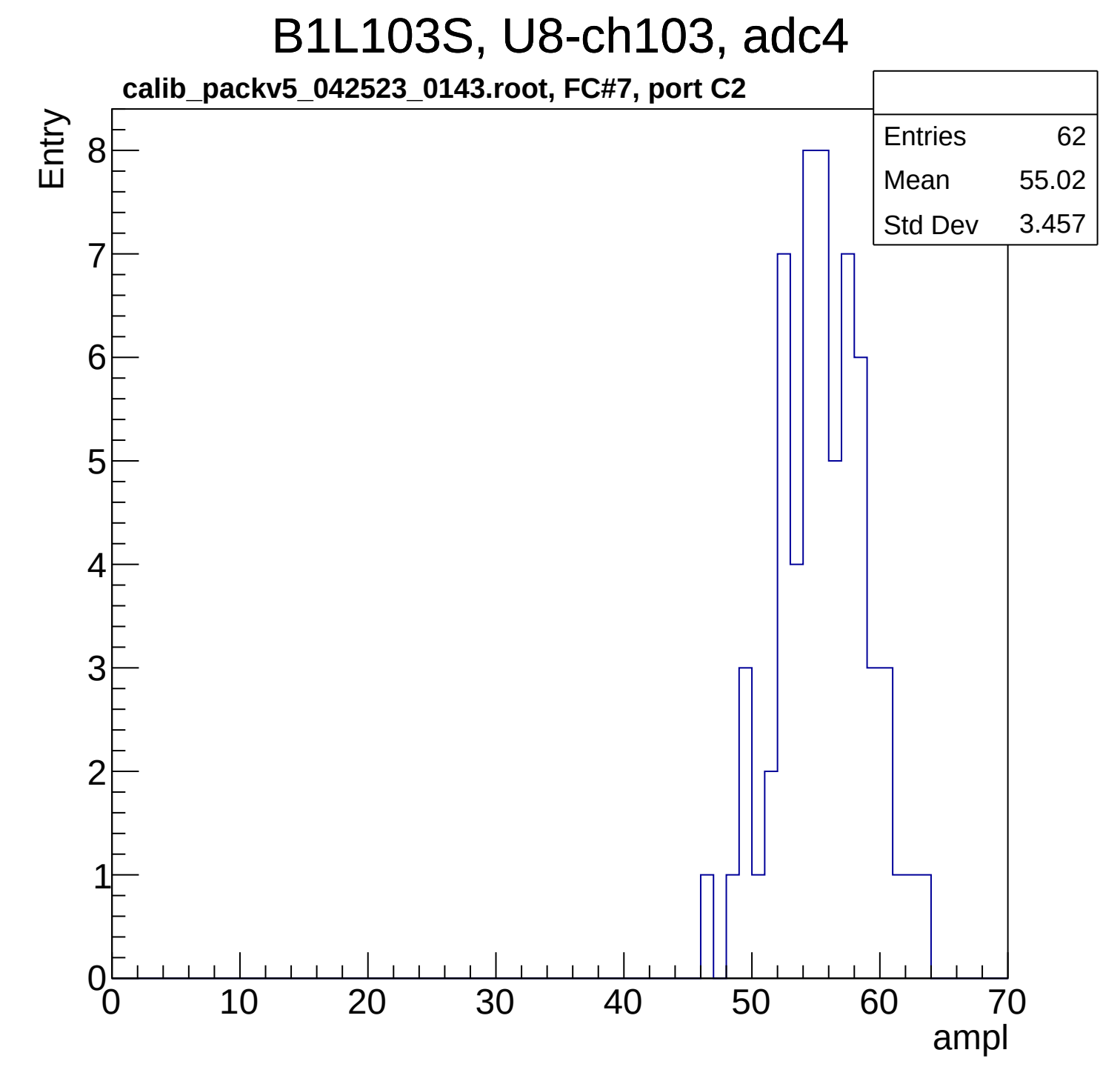

B1L103S, U8-ch102, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 36.25
Std Dev 27.58
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

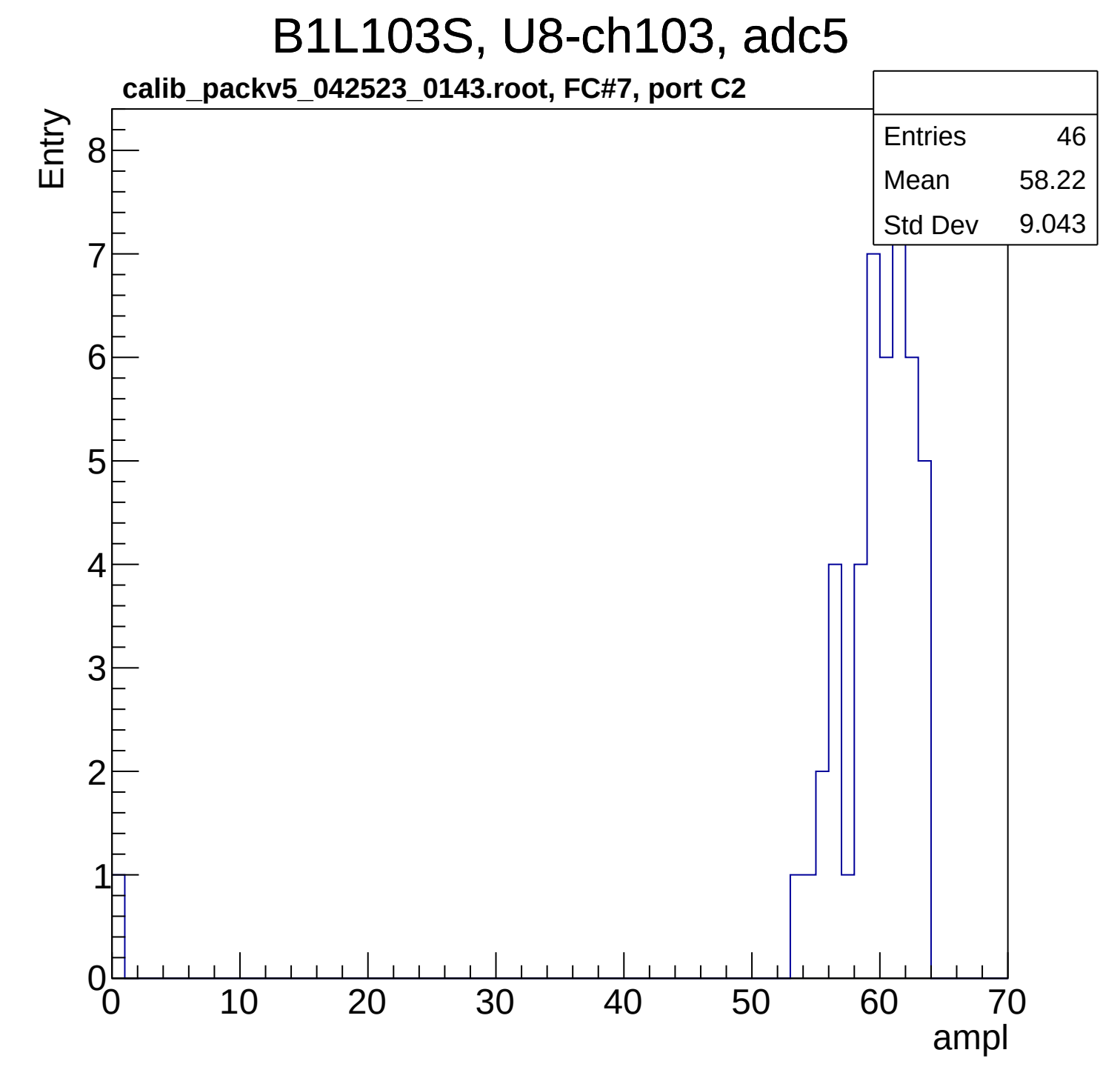

B1L103S, U8-ch103, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 84
Mean 29.15
Std Dev 3.571
Gaus mean : 29.6324
Gaus Width: 3.6705
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

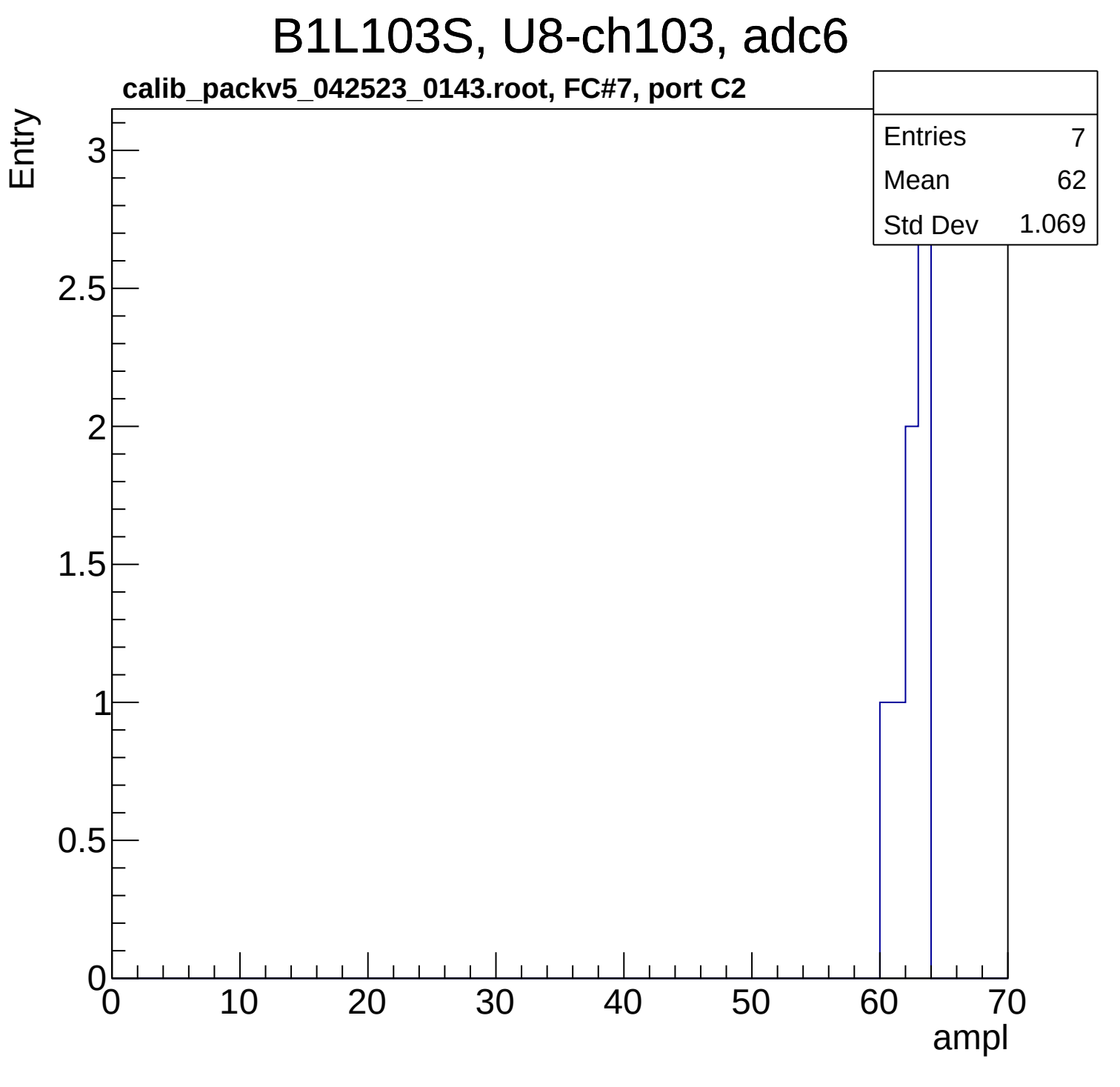

B1L103S, U8-ch103, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 36.52
Std Dev 3.533
Gaus mean : 37.1202
Gaus Width: 3.7027
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

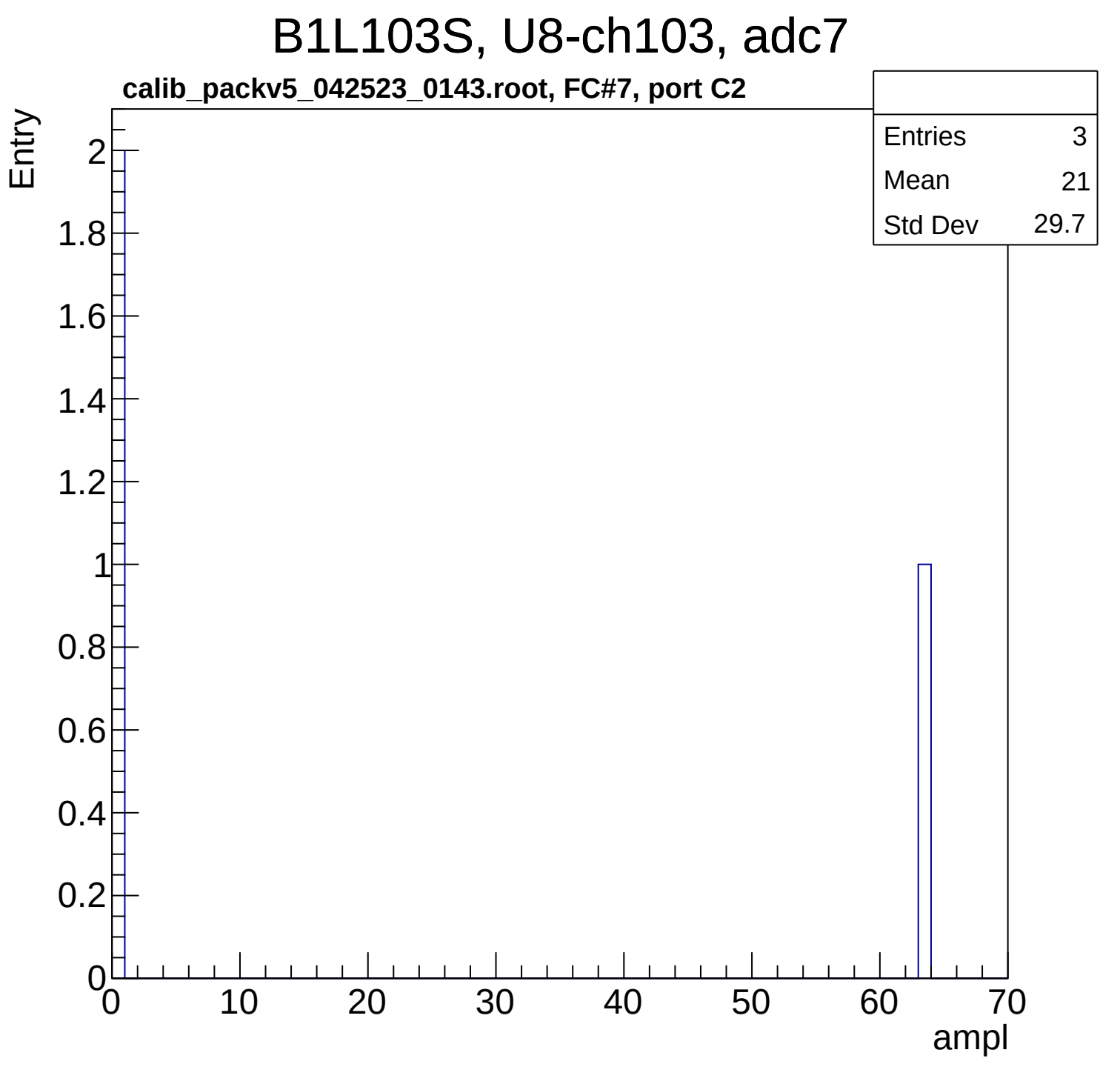

B1L103S, U8-ch103, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 42.84
Std Dev 4.067
Gaus mean : 43.3497
Gaus Width: 4.0182
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

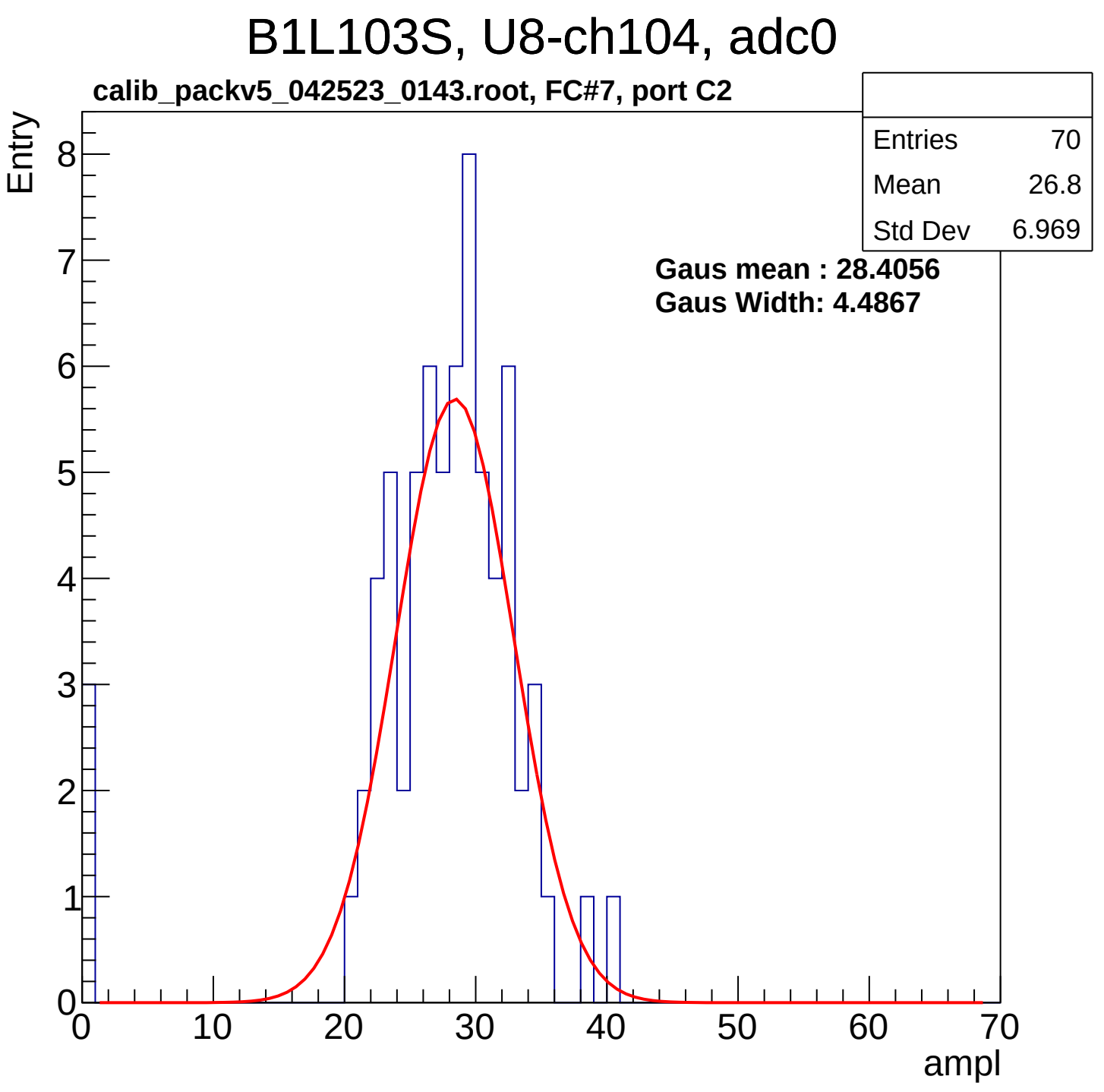

B1L103S, U8-ch103, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 48.59
Std Dev 3.943
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

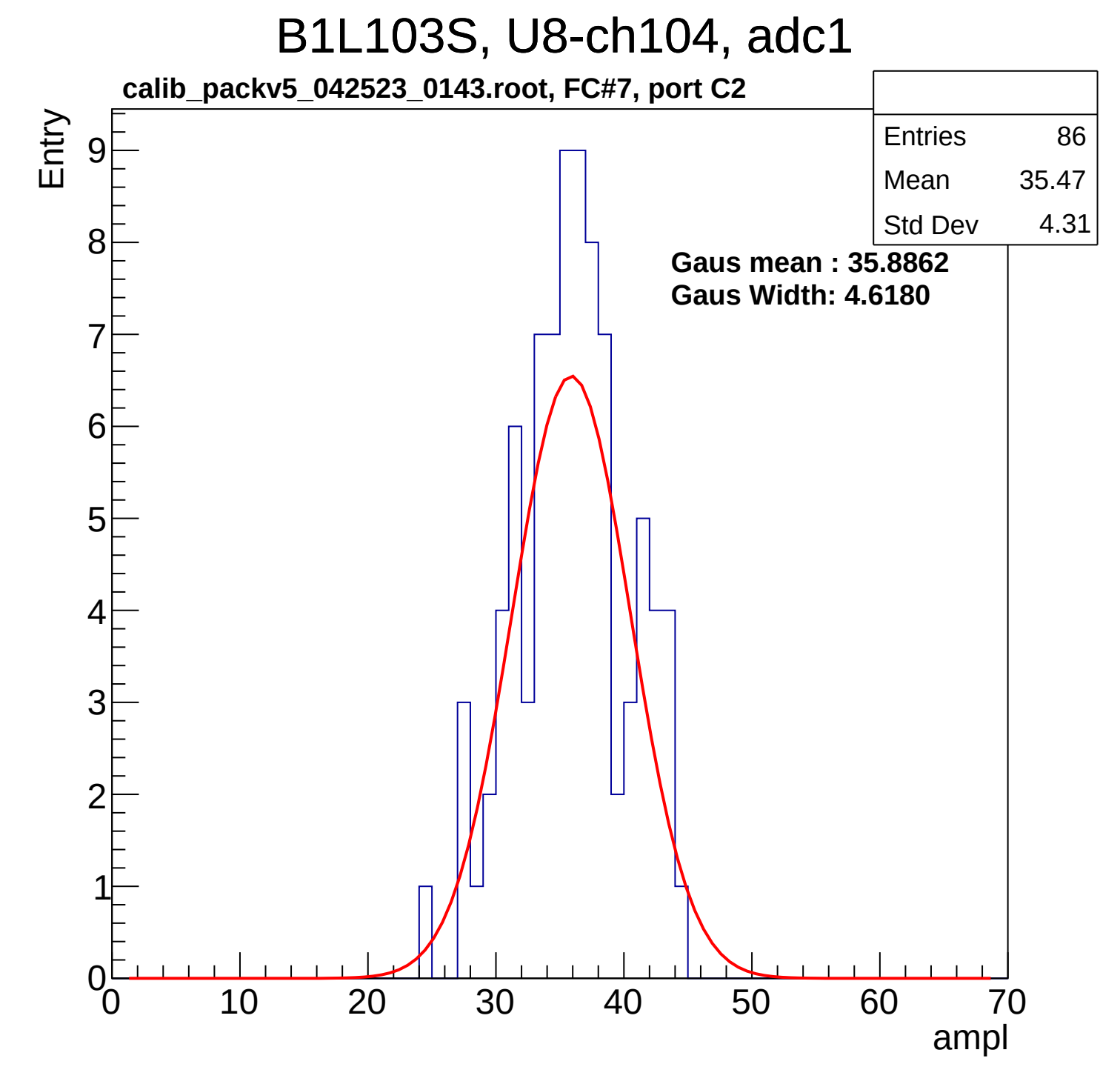

B1L103S, U8-ch103, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 55.02
Std Dev 3.457
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

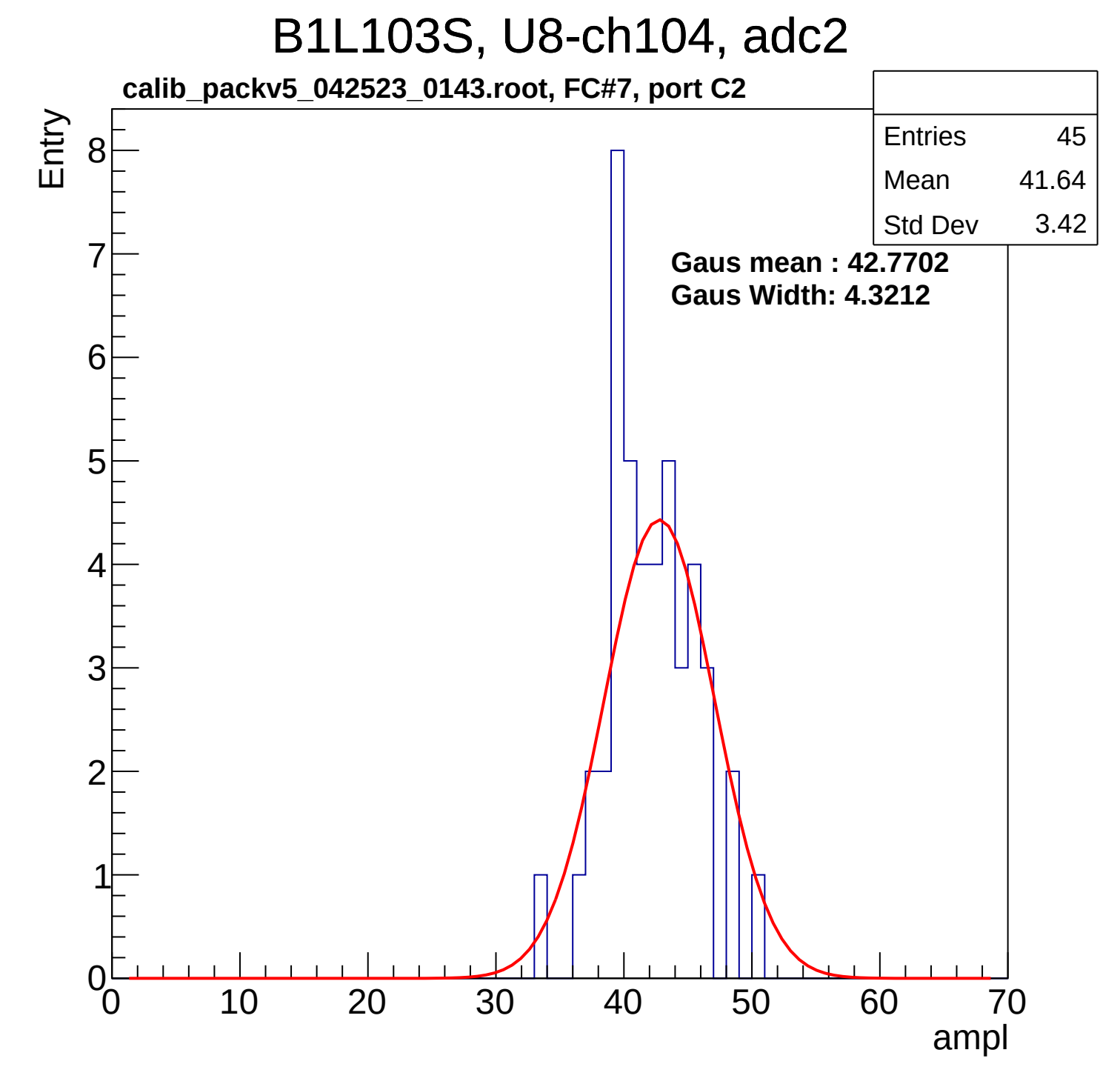

B1L103S, U8-ch103, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 46
Mean 58.22
Std Dev 9.043
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

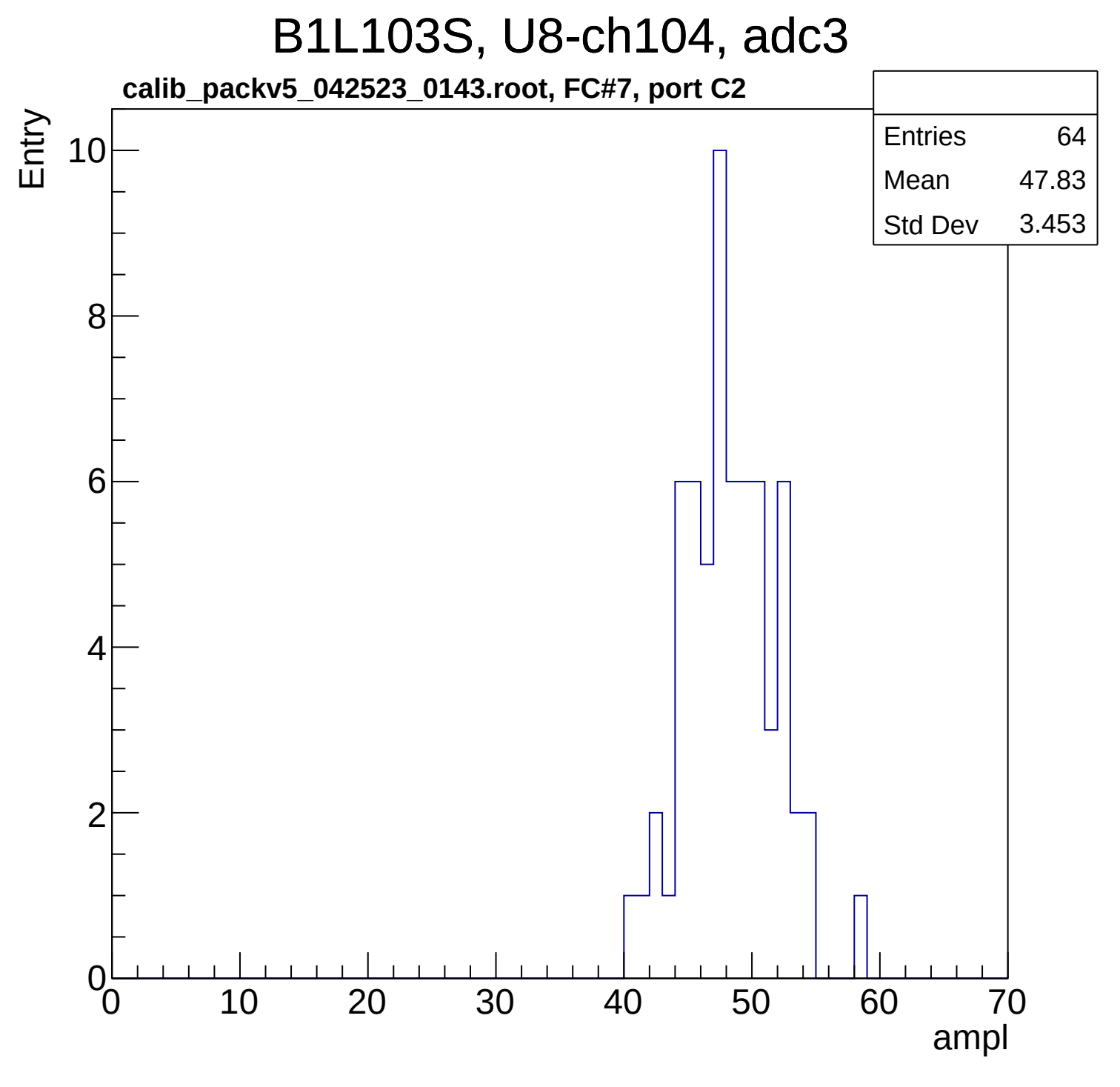

B1L103S, U8-ch103, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 7
Mean 62
Std Dev 1.069
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

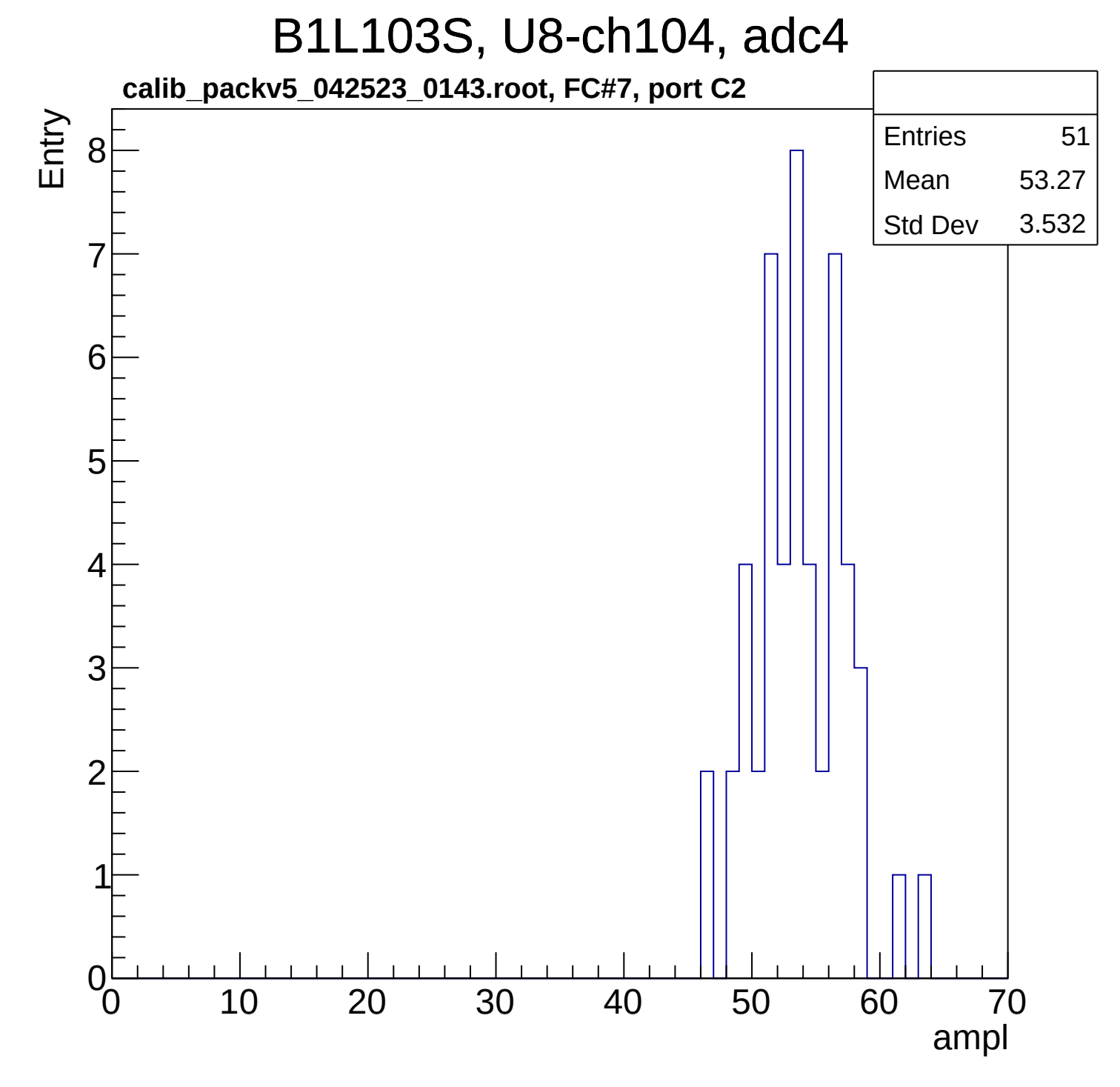

B1L103S, U8-ch103, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 21
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

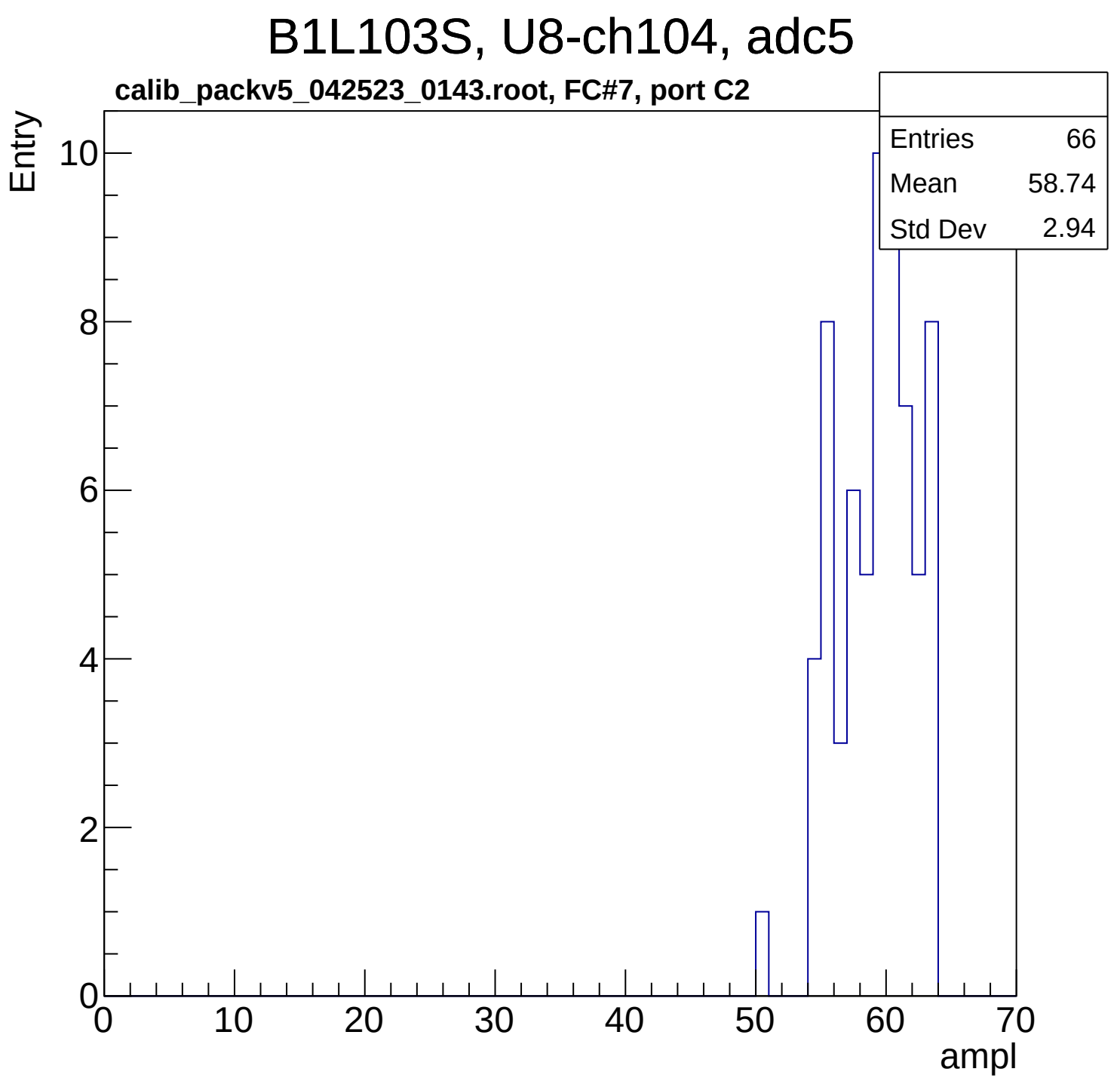

B1L103S, U8-ch104, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 26.8
Std Dev 6.969
Gaus mean : 28.4056
Gaus Width: 4.4867
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

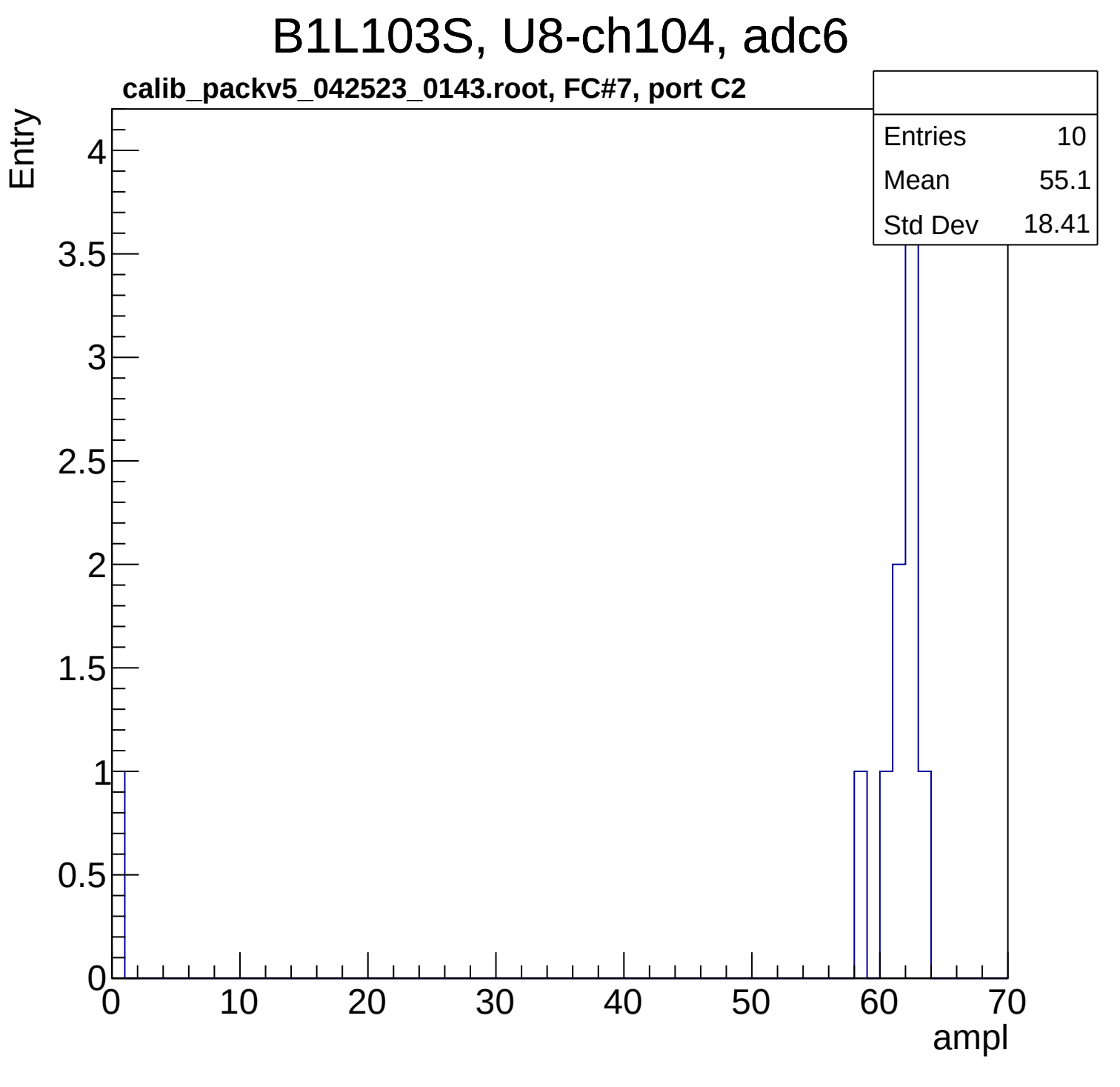

B1L103S, U8-ch104, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 86
Mean 35.47
Std Dev 4.31
Gaus mean : 35.8862
Gaus Width: 4.6180
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

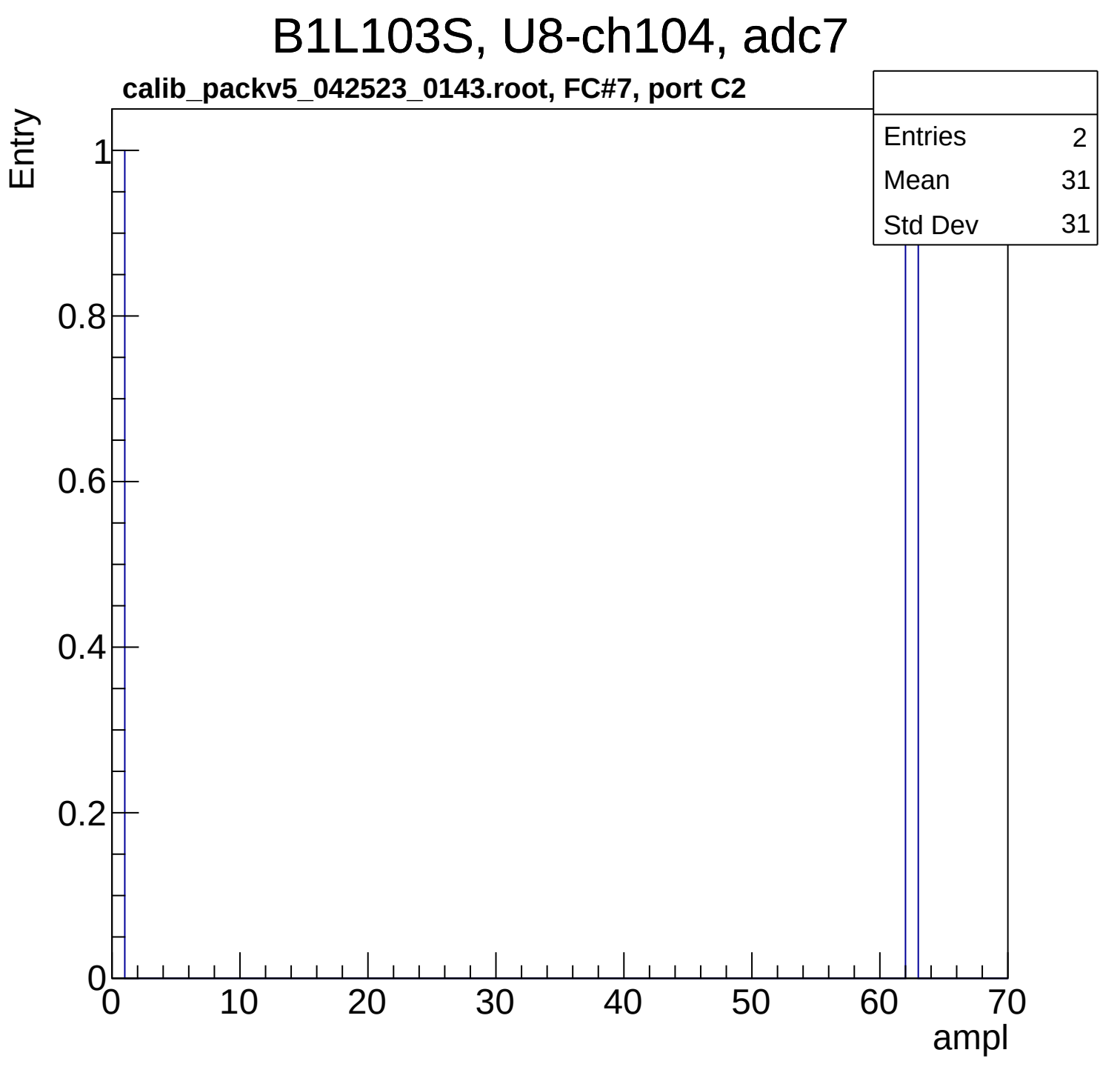

B1L103S, U8-ch104, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 45
Mean 41.64
Std Dev 3.42
Gaus mean : 42.7702
Gaus Width: 4.3212
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

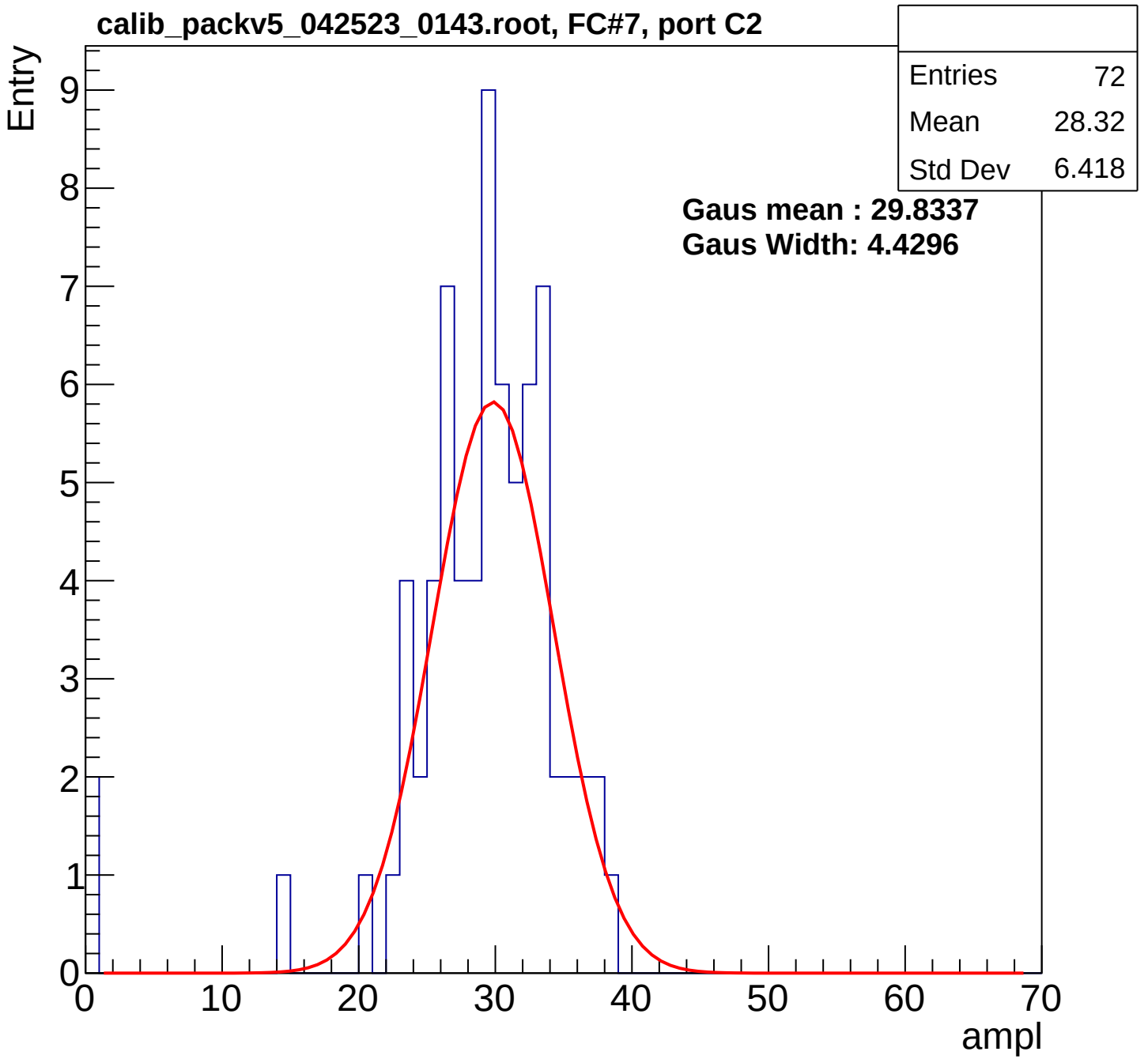

B1L103S, U8-ch104, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 47.83
Std Dev 3.453
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

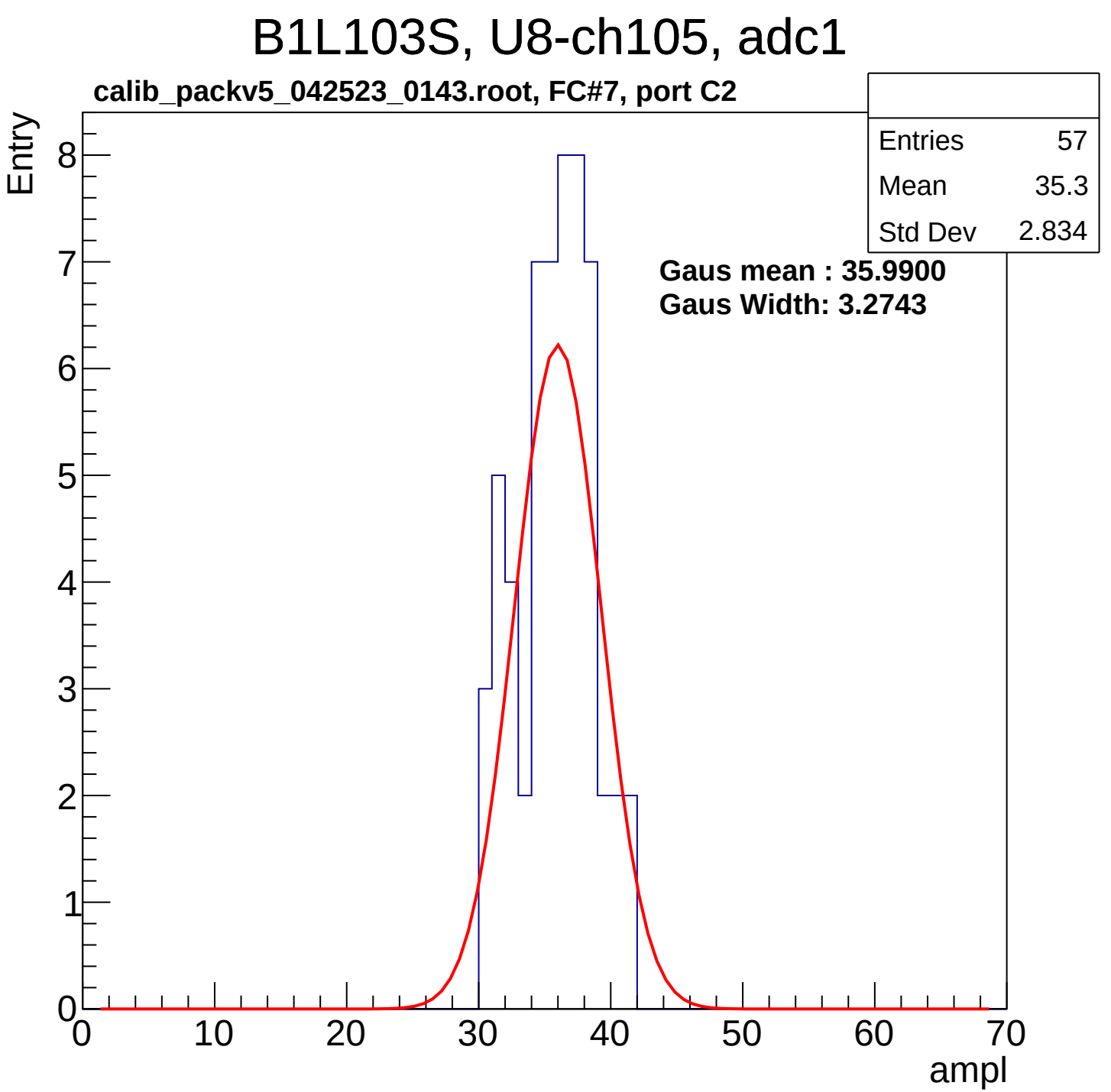

B1L103S, U8-ch104, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 53.27
Std Dev 3.532
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

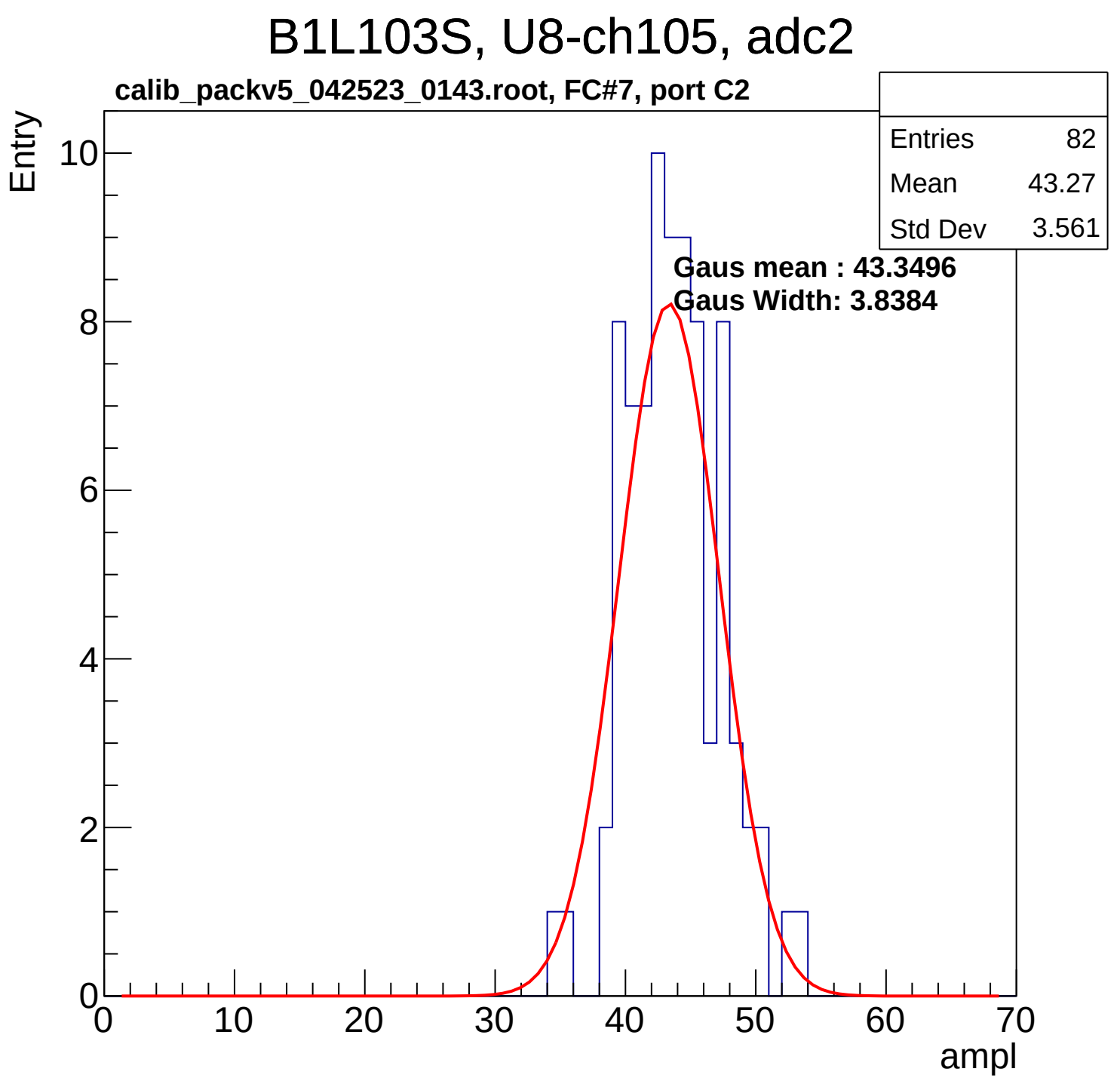

B1L103S, U8-ch104, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 58.74
Std Dev 2.94
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

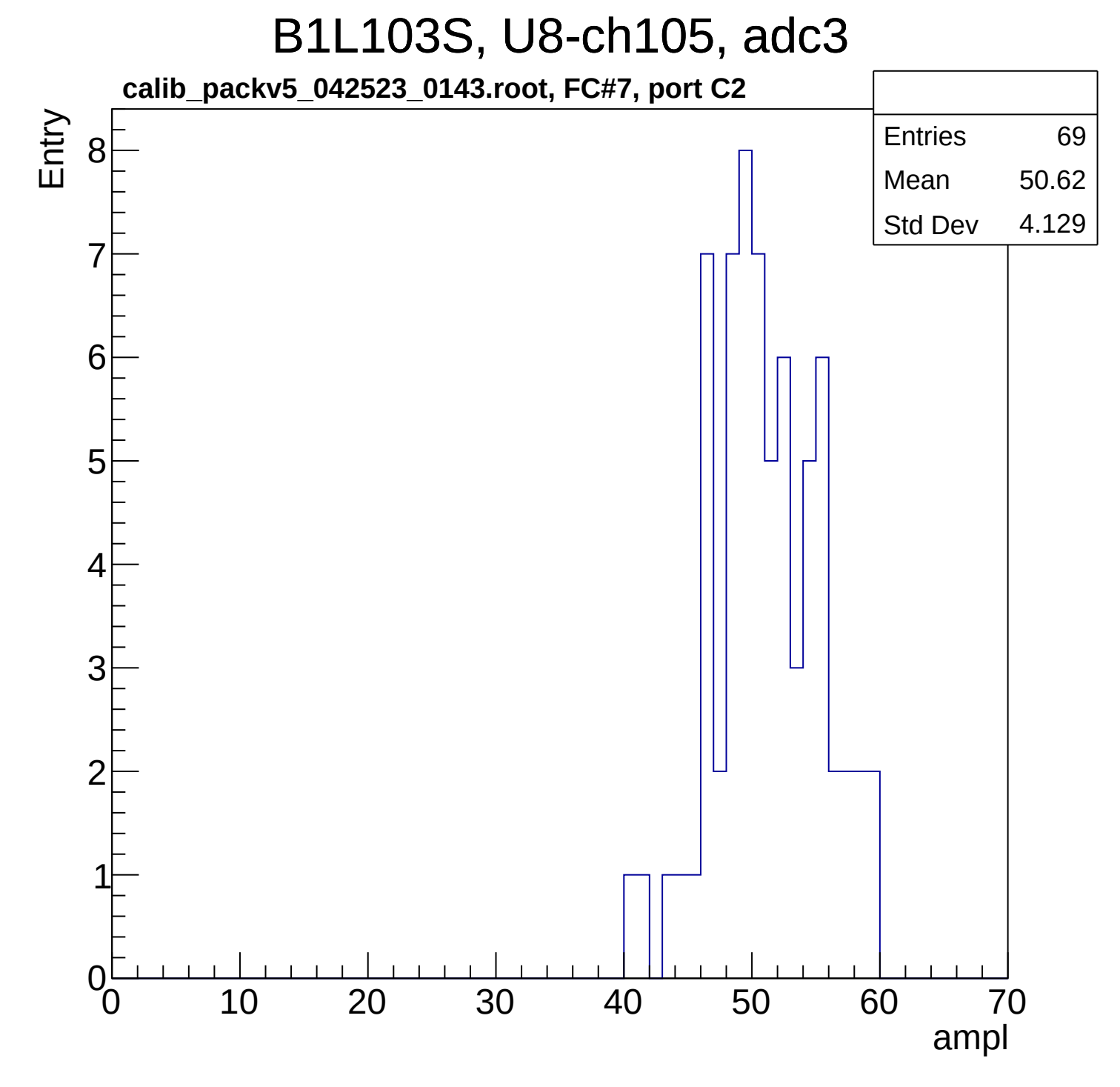

B1L103S, U8-ch104, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 10
Mean 55.1
Std Dev 18.41
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

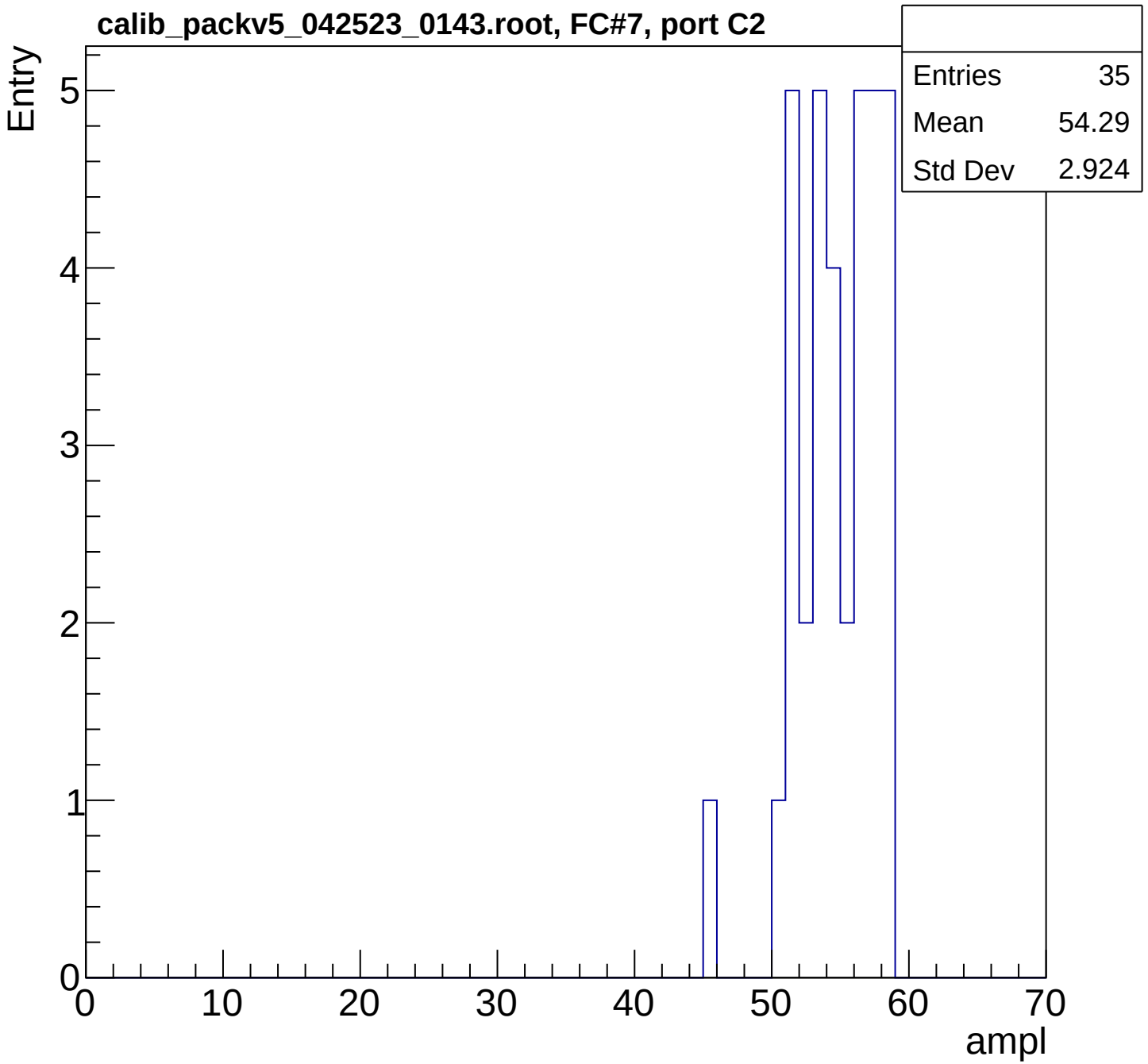

B1L103S, U8-ch104, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 31
Std Dev 31
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

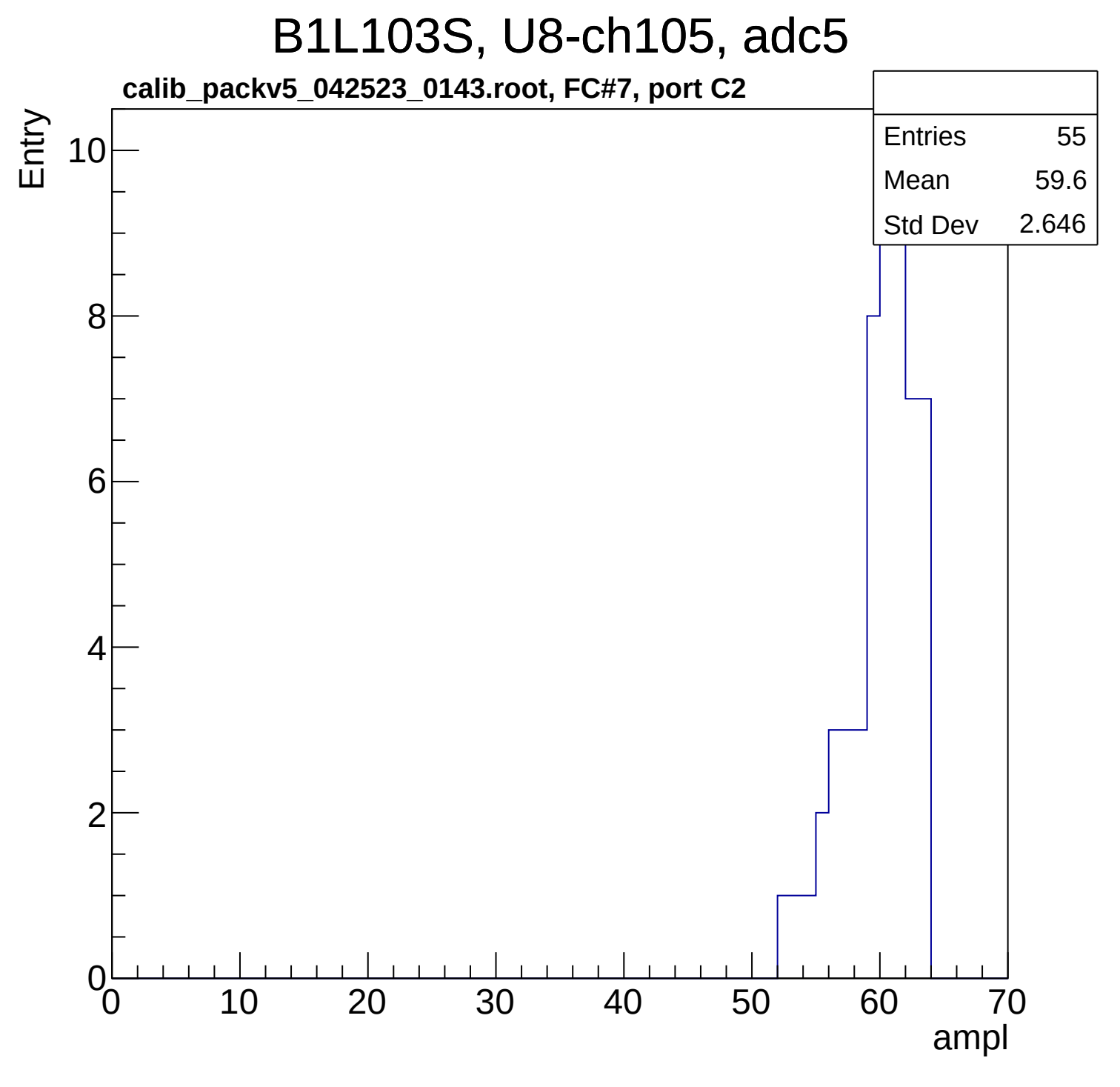

B1L103S, U8-ch105, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 28.32
Std Dev 6.418
Gaus mean : 29.8337
Gaus Width: 4.4296
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

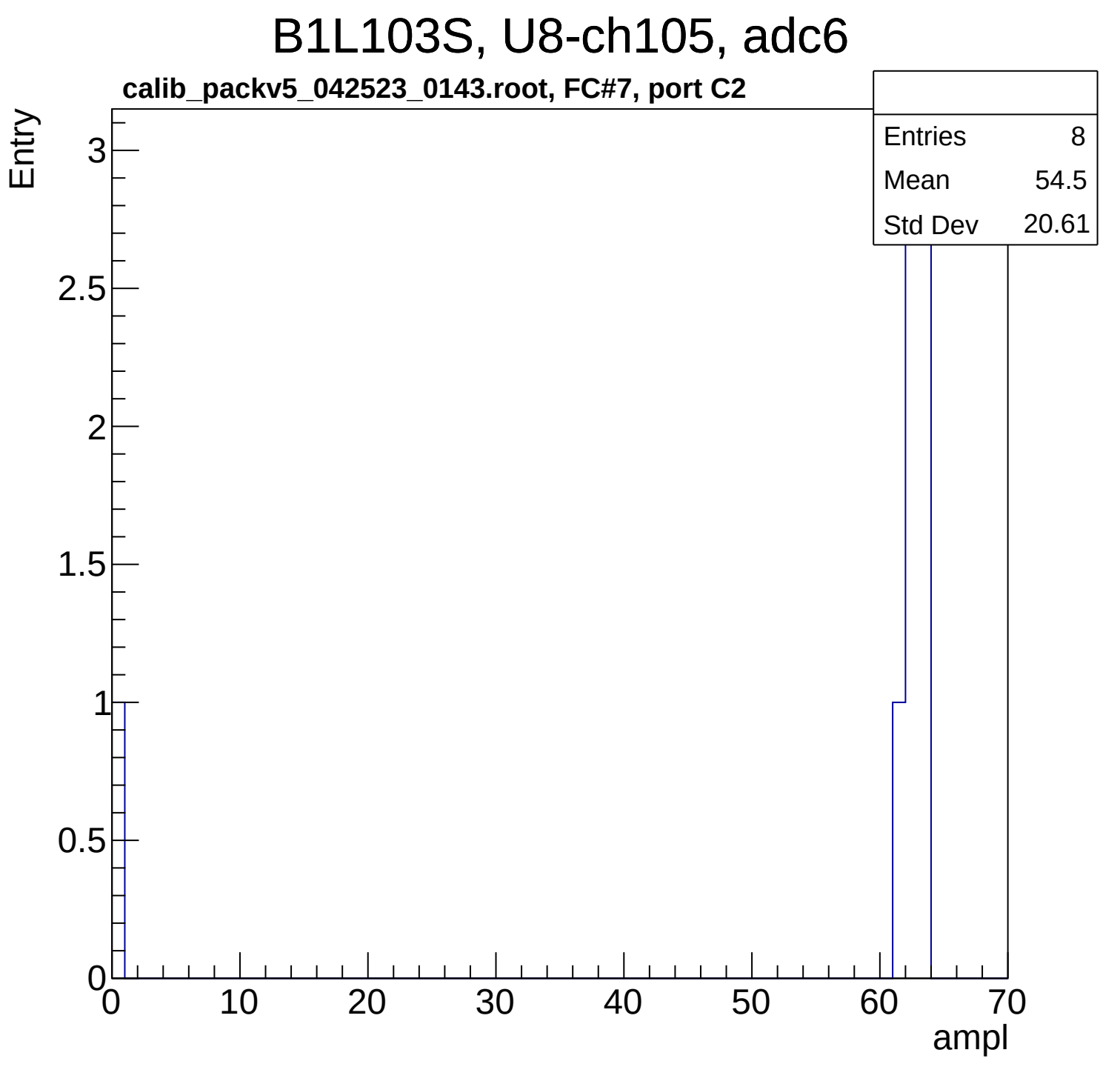

B1L103S, U8-ch105, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 35.3
Std Dev 2.834
Gaus mean : 35.9900
Gaus Width: 3.2743
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

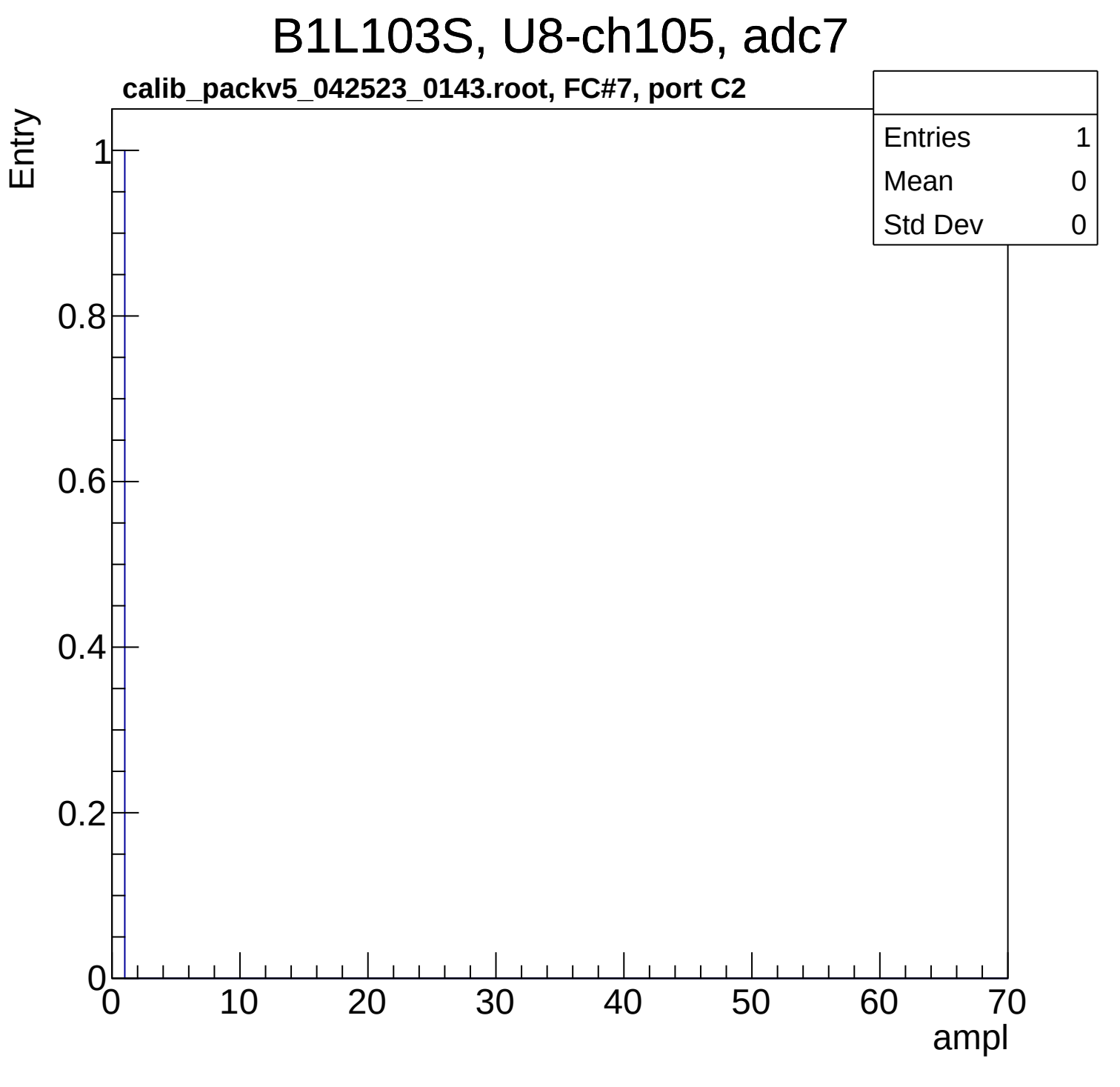

B1L103S, U8-ch105, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 82
Mean 43.27
Std Dev 3.561
Gaus mean : 43.3496
Gaus Width: 3.8384
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

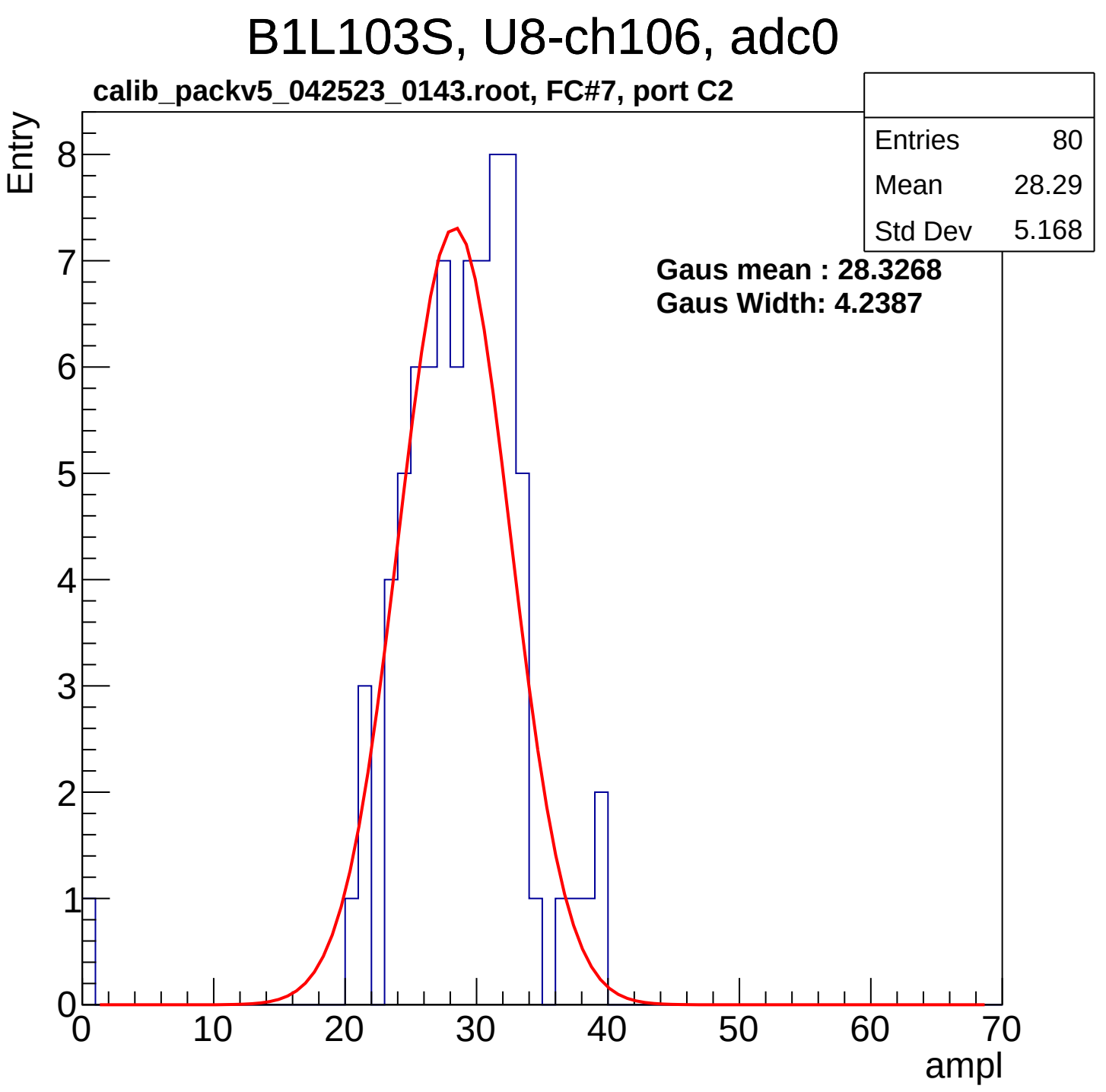

B1L103S, U8-ch105, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 50.62
Std Dev 4.129
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

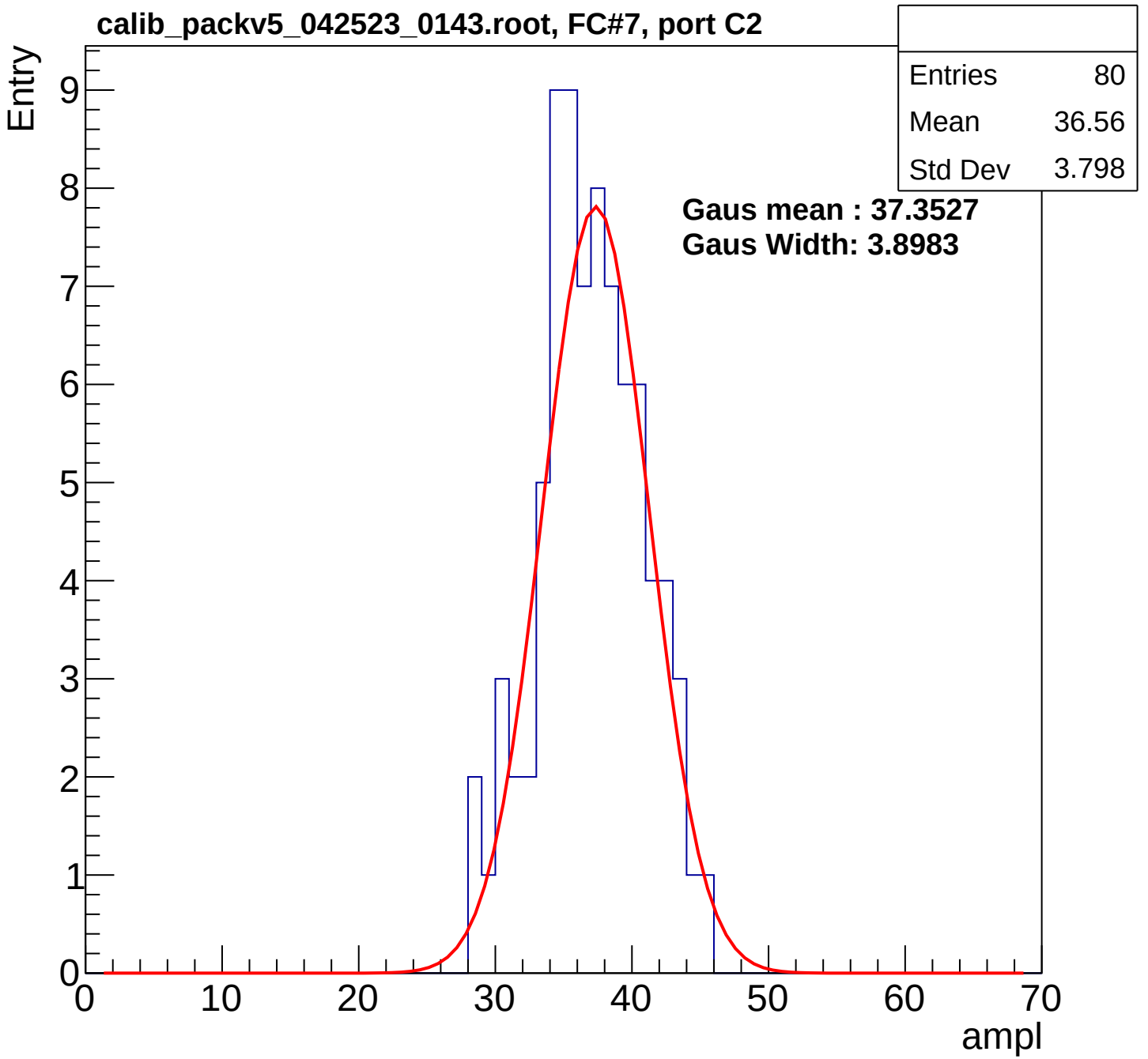

B1L103S, U8-ch105, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 35
Mean 54.29
Std Dev 2.924
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

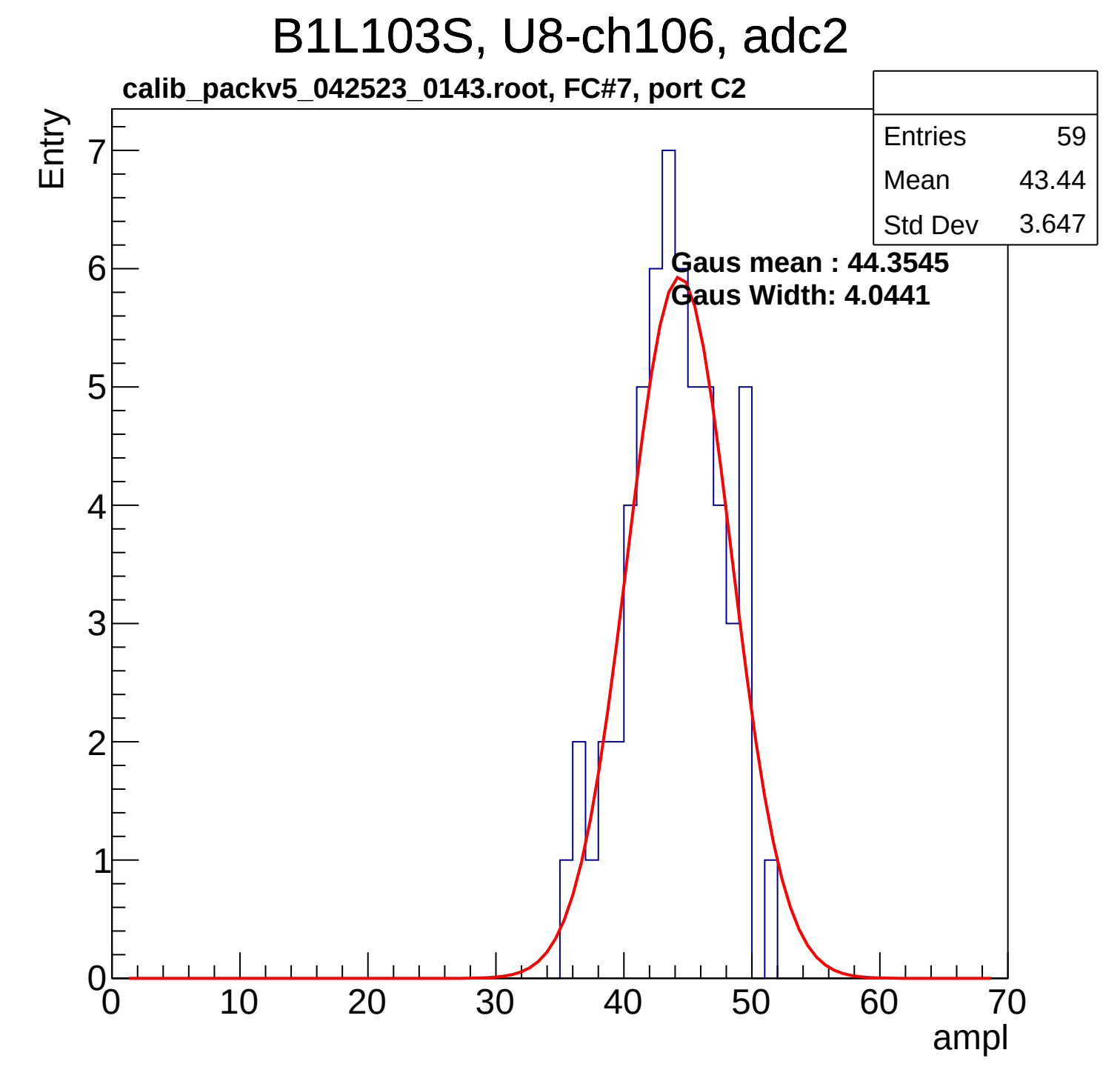

B1L103S, U8-ch105, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 59.6
Std Dev 2.646
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

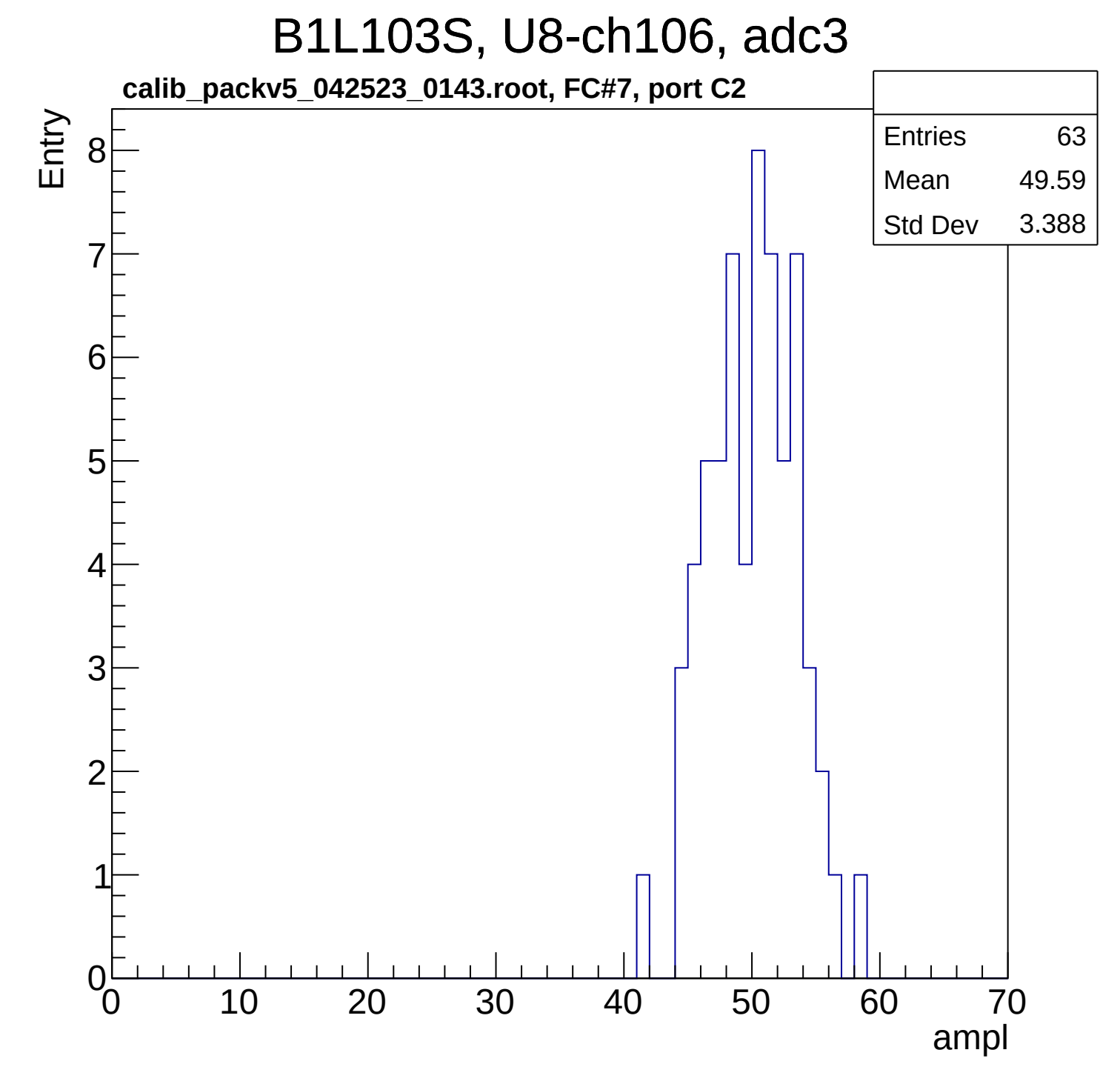

B1L103S, U8-ch105, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 8
Mean 54.5
Std Dev 20.61
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

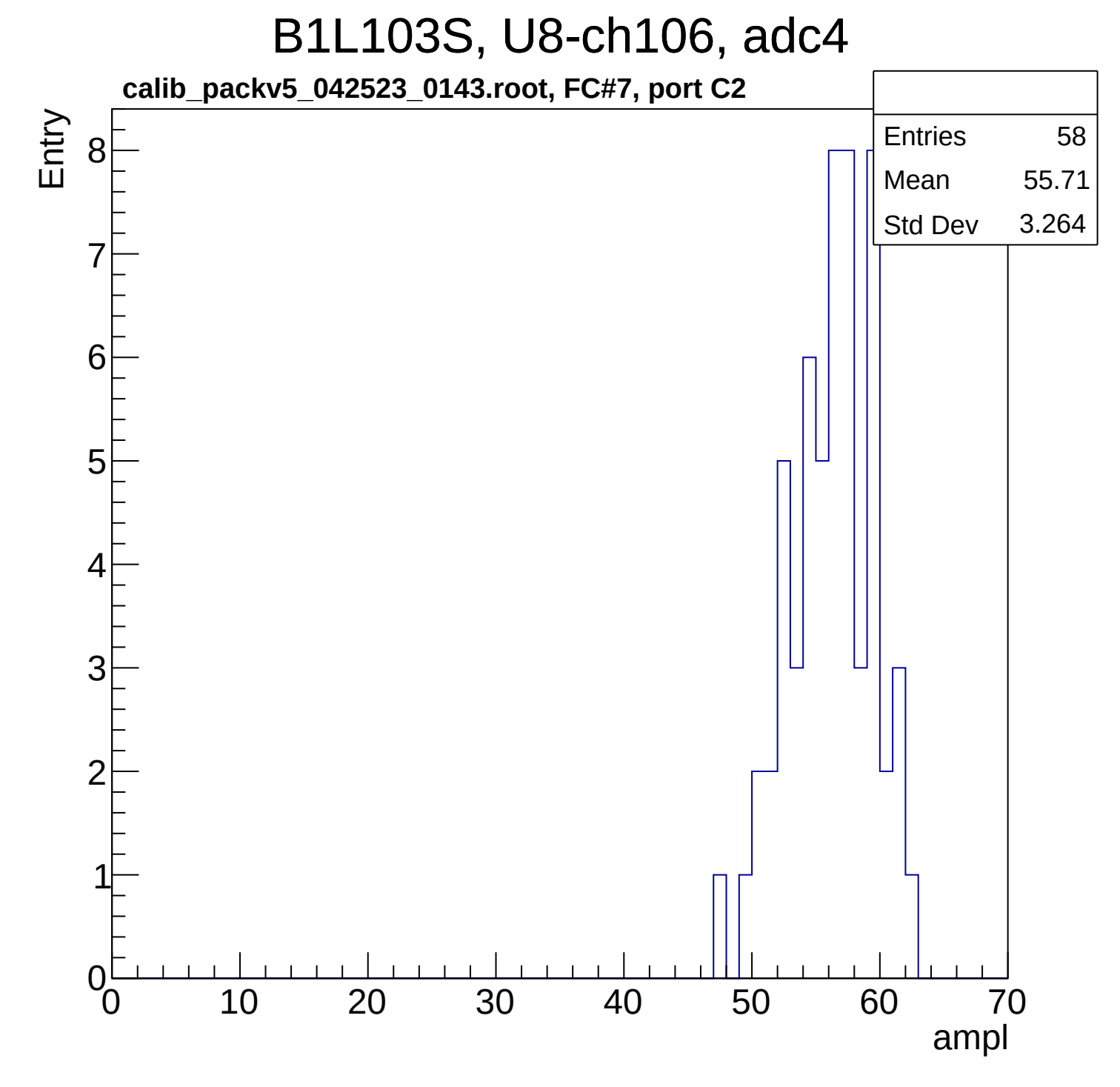

B1L103S, U8-ch105, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

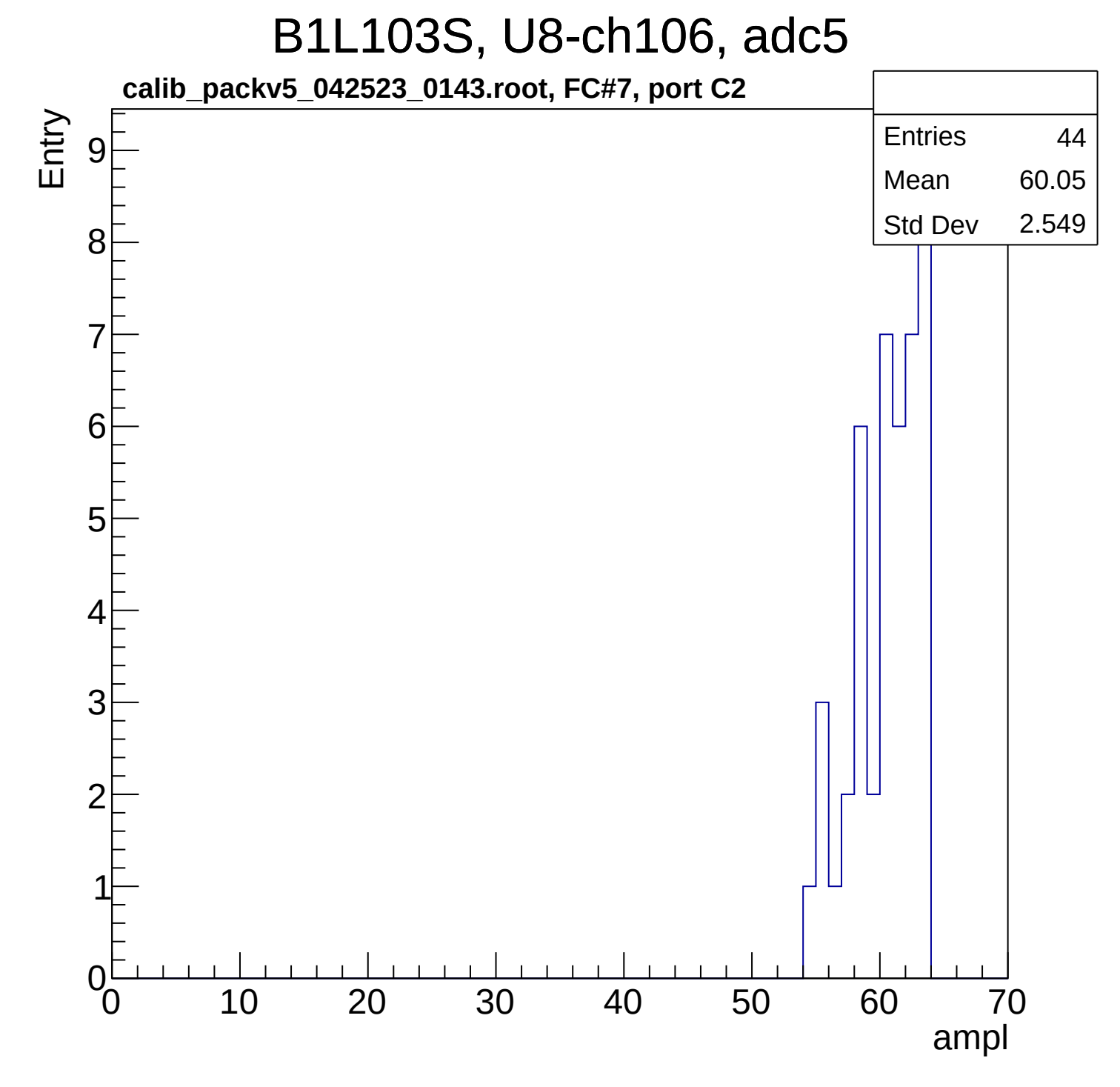

B1L103S, U8-ch106, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 80
Mean 28.29
Std Dev 5.168
Gaus mean : 28.3268
Gaus Width: 4.2387
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

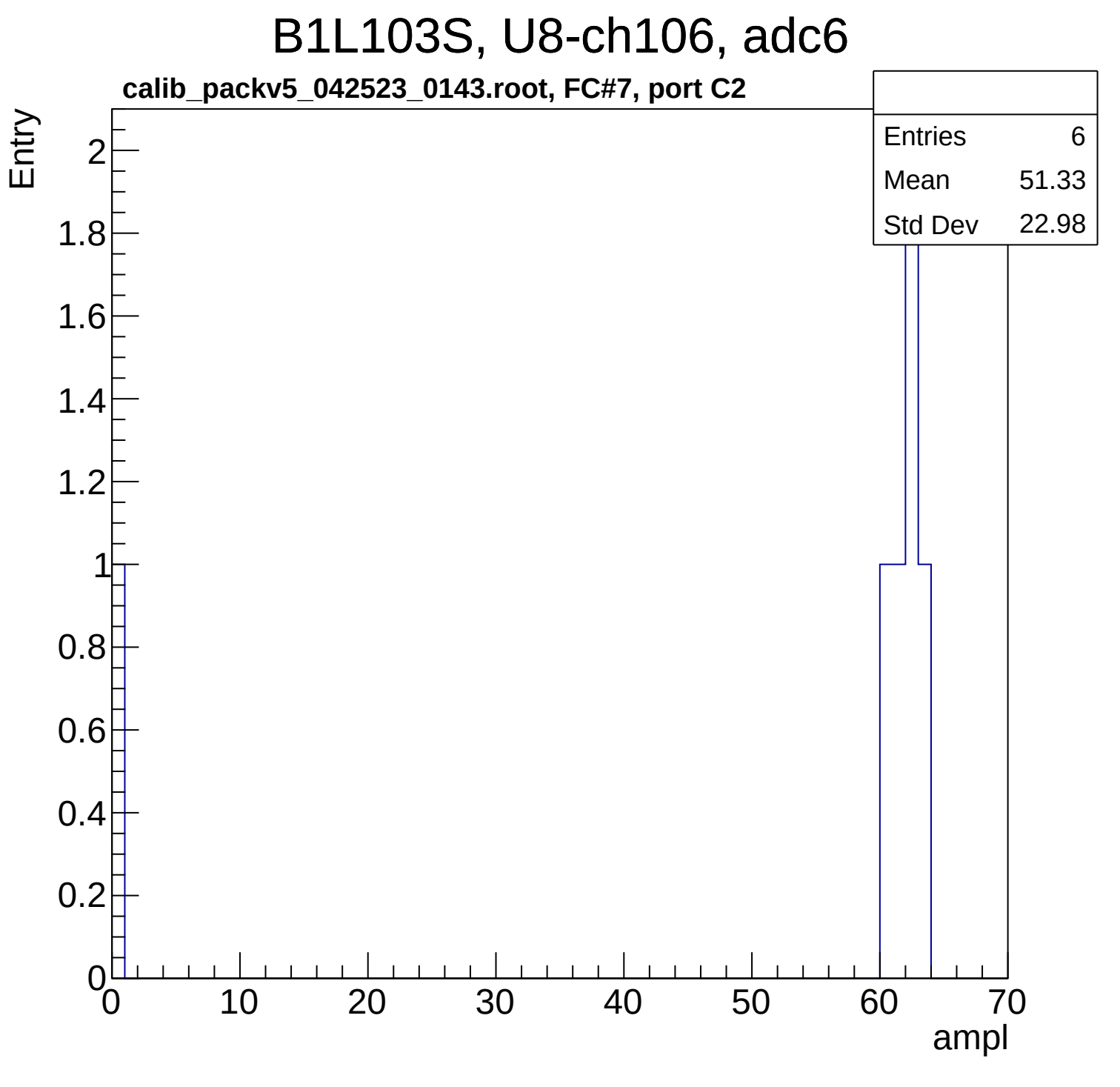

B1L103S, U8-ch106, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 80
Mean 36.56
Std Dev 3.798
Gaus mean : 37.3527
Gaus Width: 3.8983
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

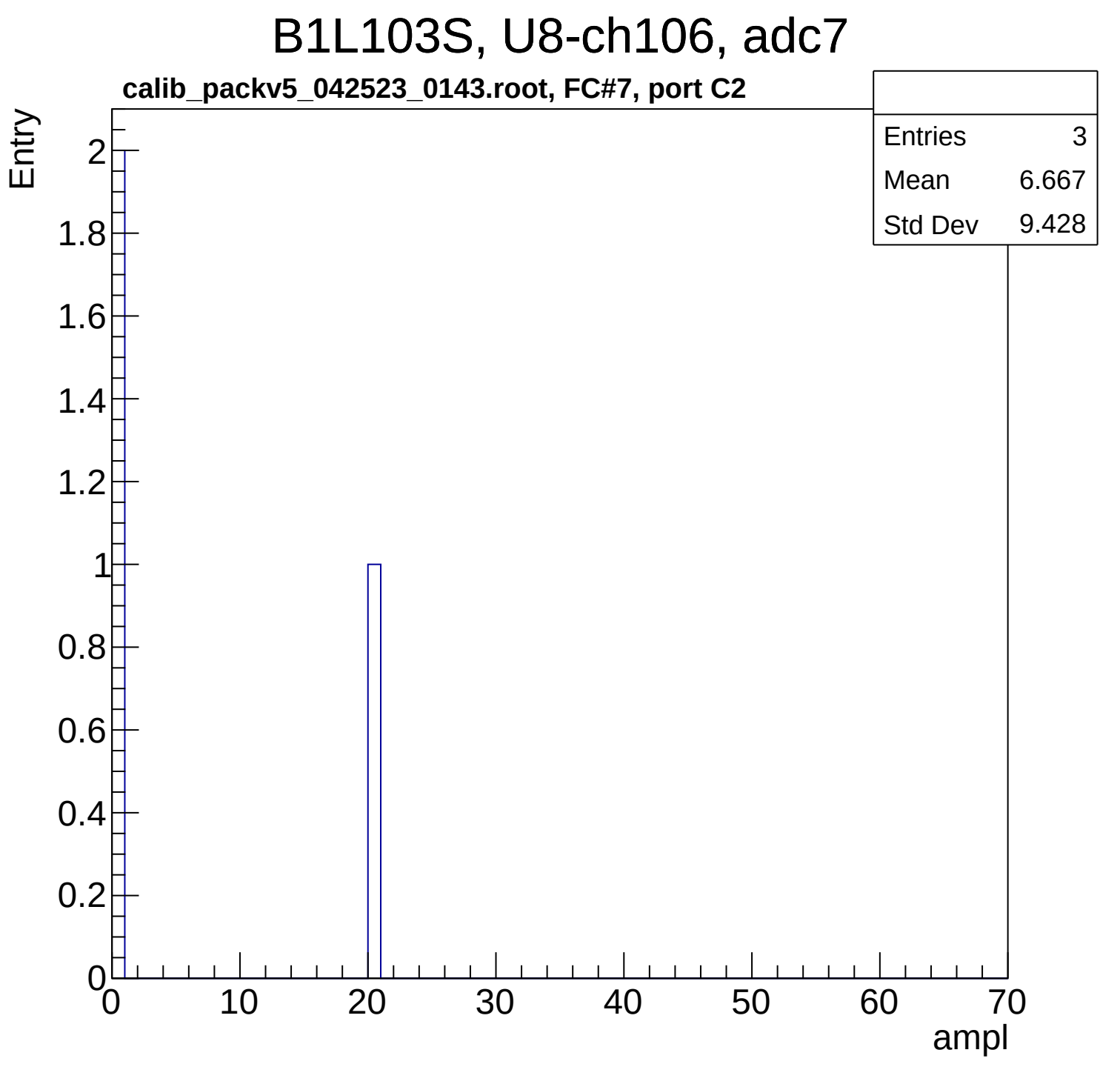

B1L103S, U8-ch106, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 43.44
Std Dev 3.647
Gaus mean : 44.3545
Gaus Width: 4.0441
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

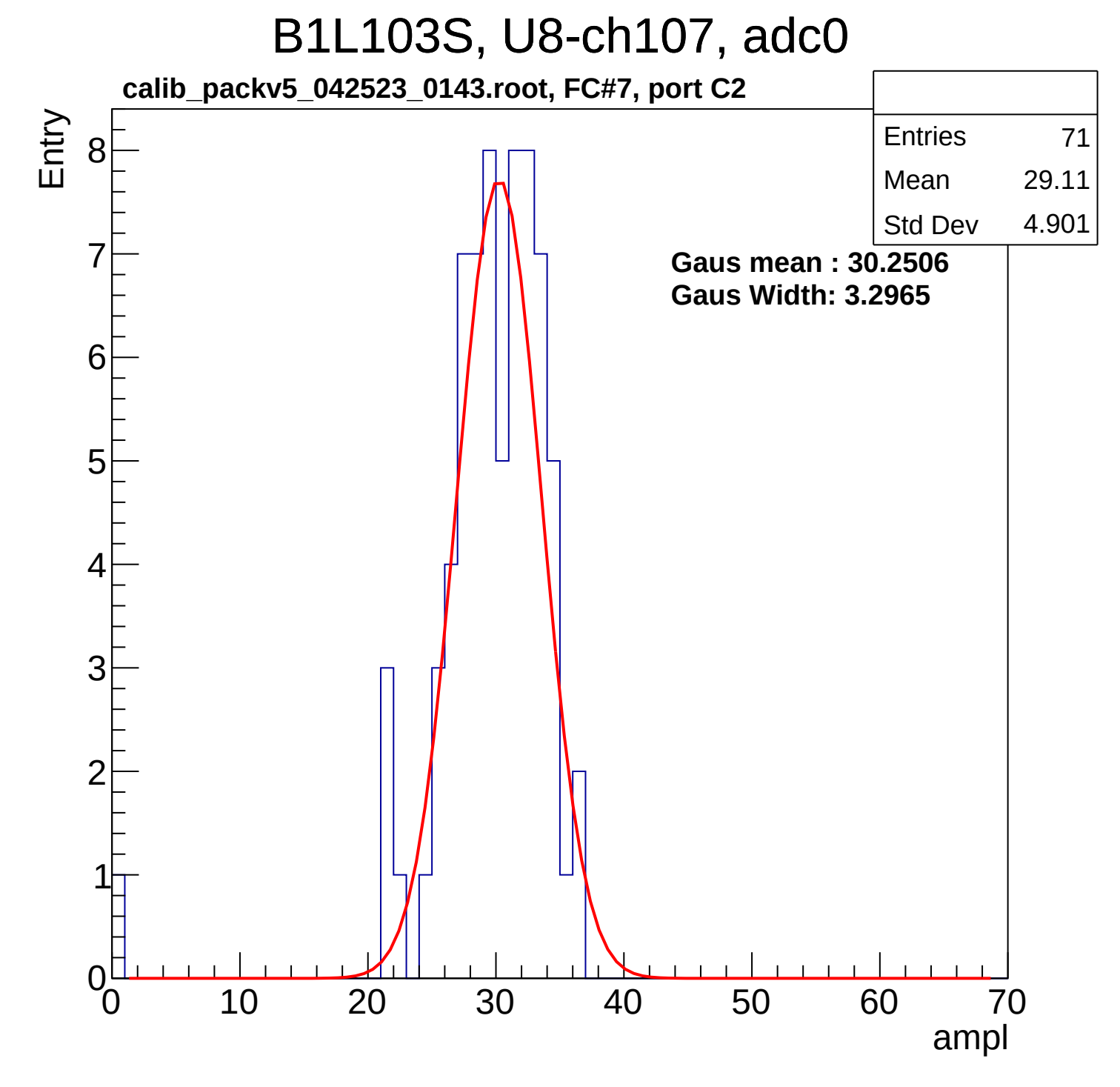

B1L103S, U8-ch106, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 49.59
Std Dev 3.388
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

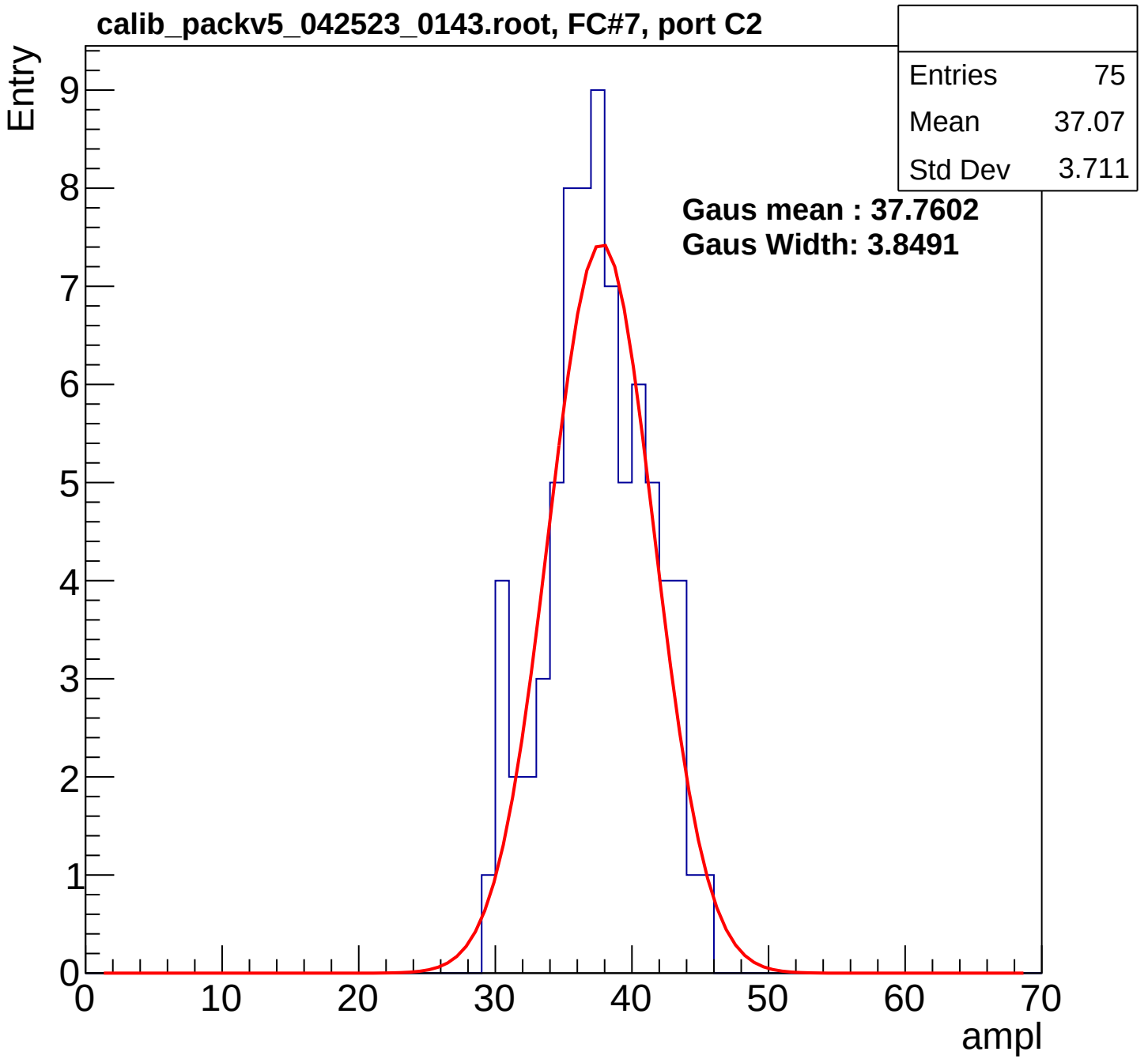

B1L103S, U8-ch106, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 55.71
Std Dev 3.264
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

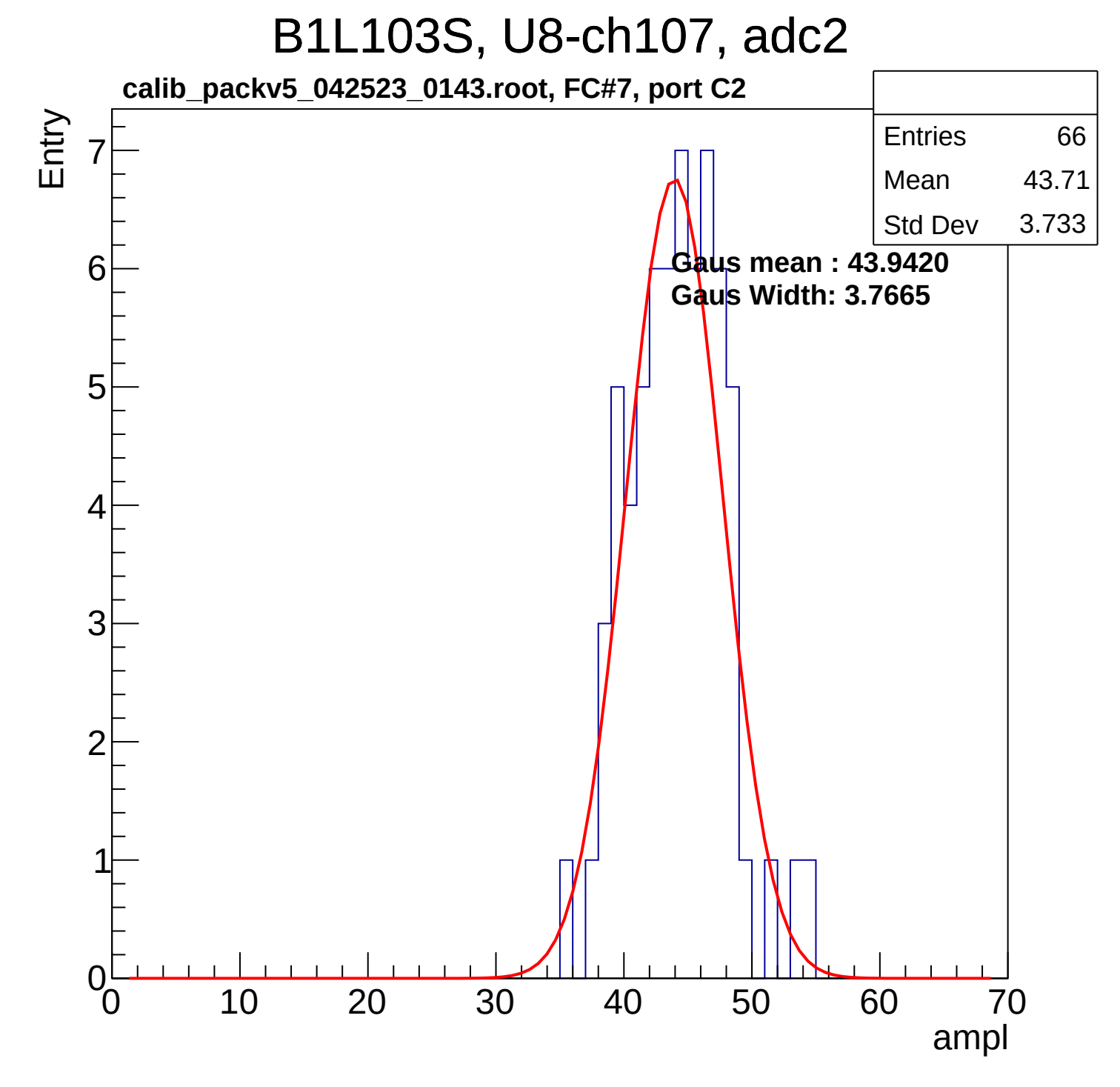

B1L103S, U8-ch106, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 44
Mean 60.05
Std Dev 2.549
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

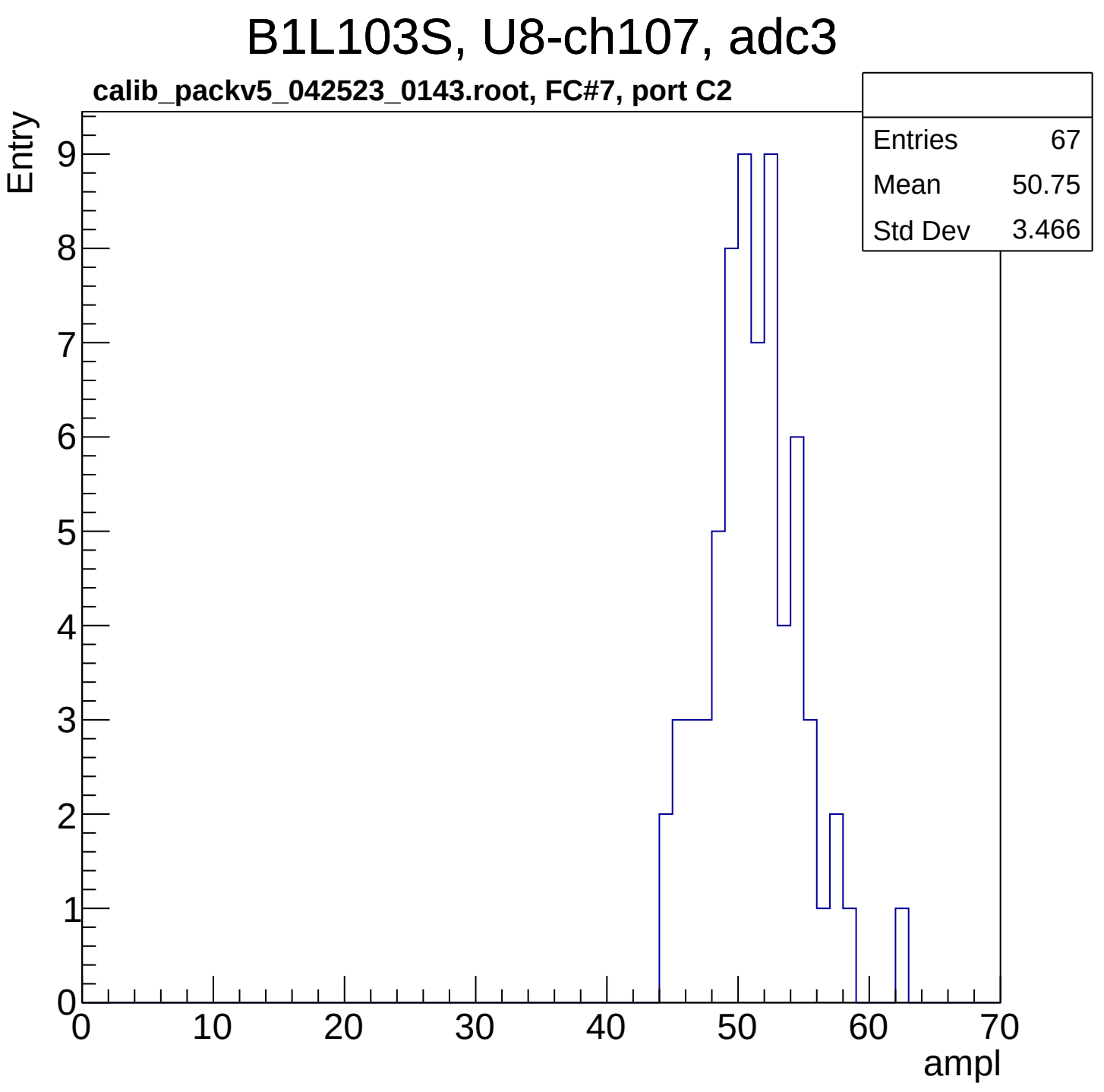

B1L103S, U8-ch106, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 51.33
Std Dev 22.98
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

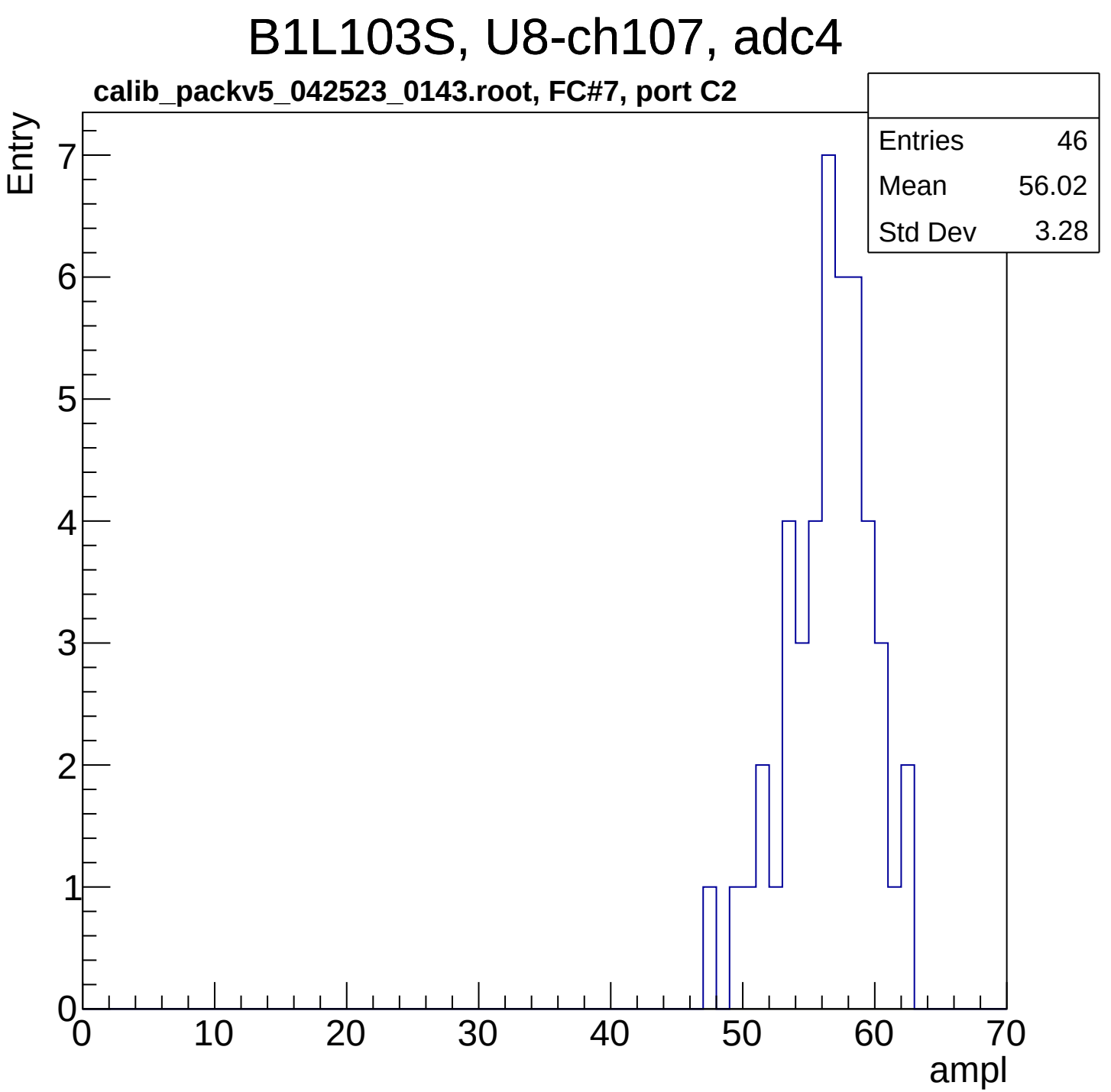

B1L103S, U8-ch106, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 6.667
Std Dev 9.428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

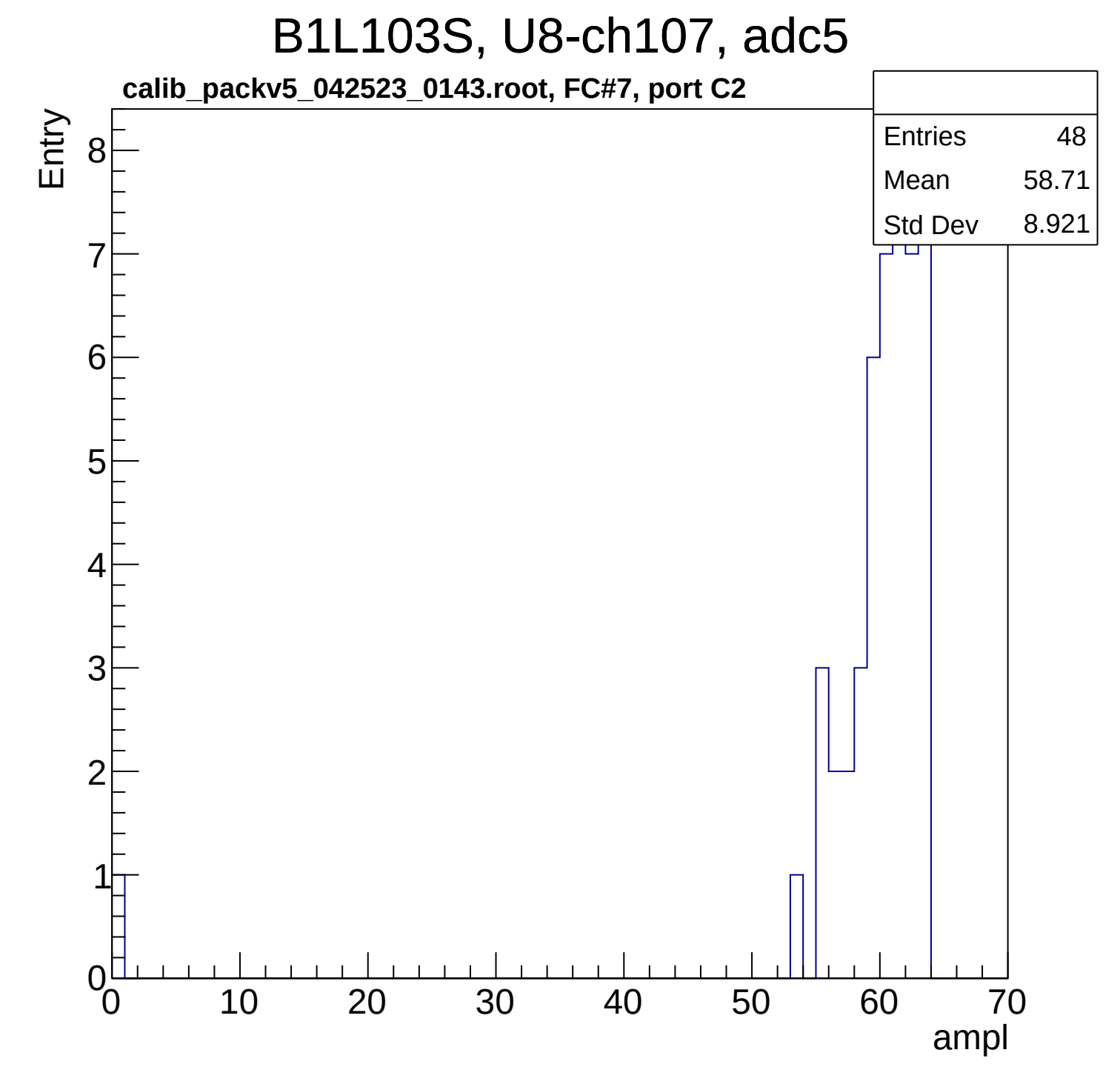

B1L103S, U8-ch107, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 29.11
Std Dev 4.901
Gaus mean : 30.2506
Gaus Width: 3.2965
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

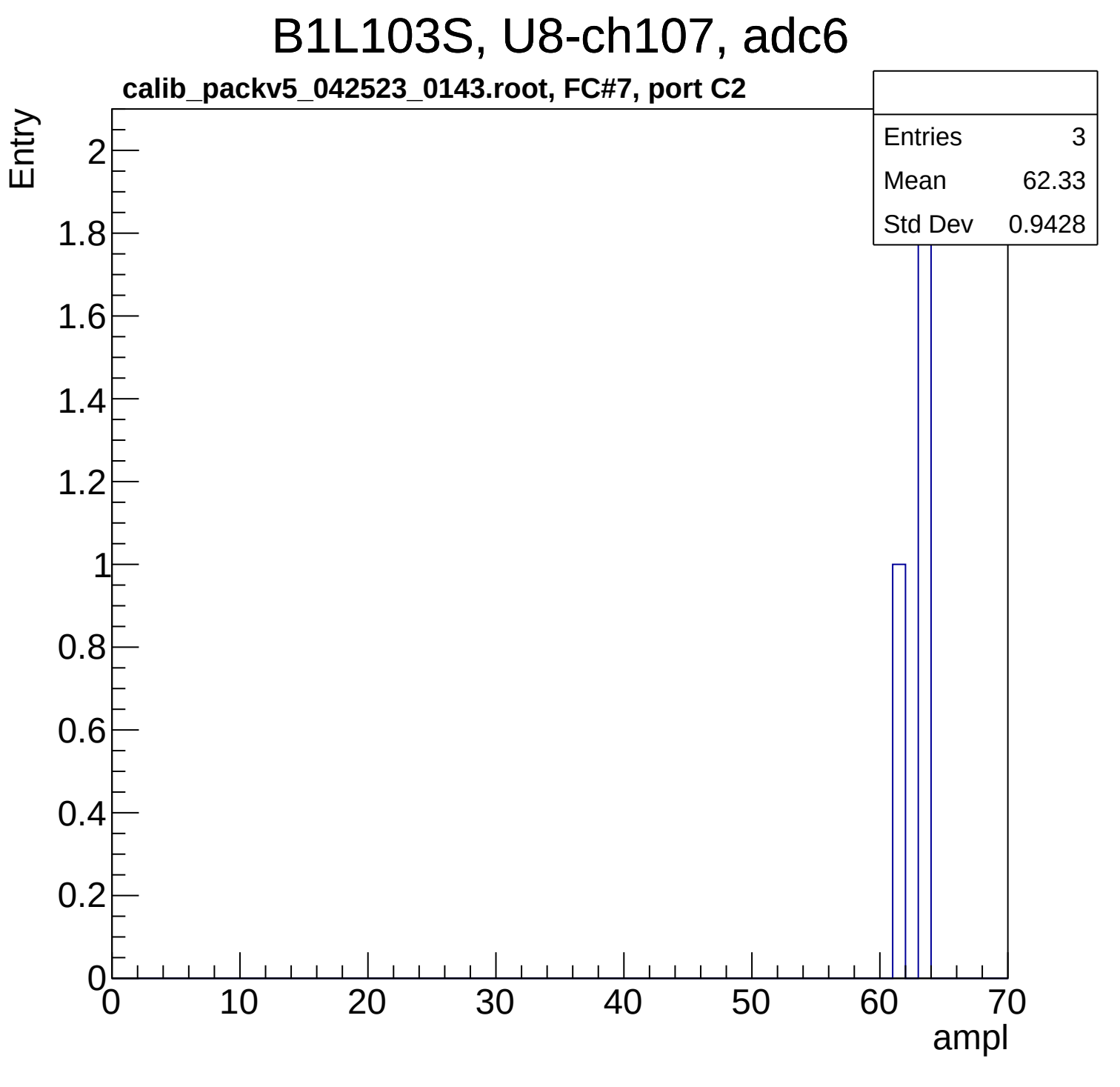

B1L103S, U8-ch107, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 37.07
Std Dev 3.711
Gaus mean : 37.7602
Gaus Width: 3.8491
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

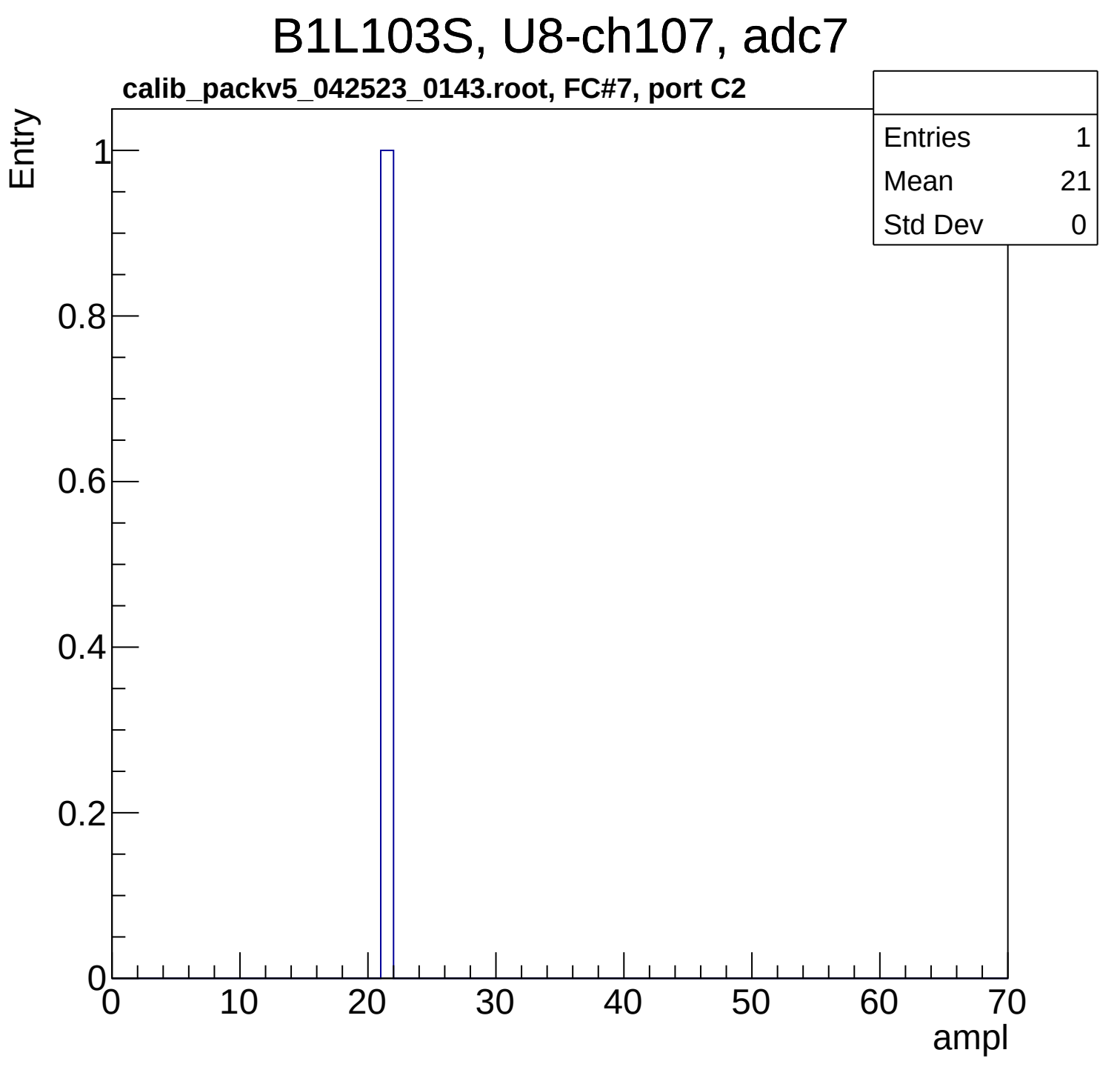

B1L103S, U8-ch107, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 43.71
Std Dev 3.733
Gaus mean : 43.9420
Gaus Width: 3.7665
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

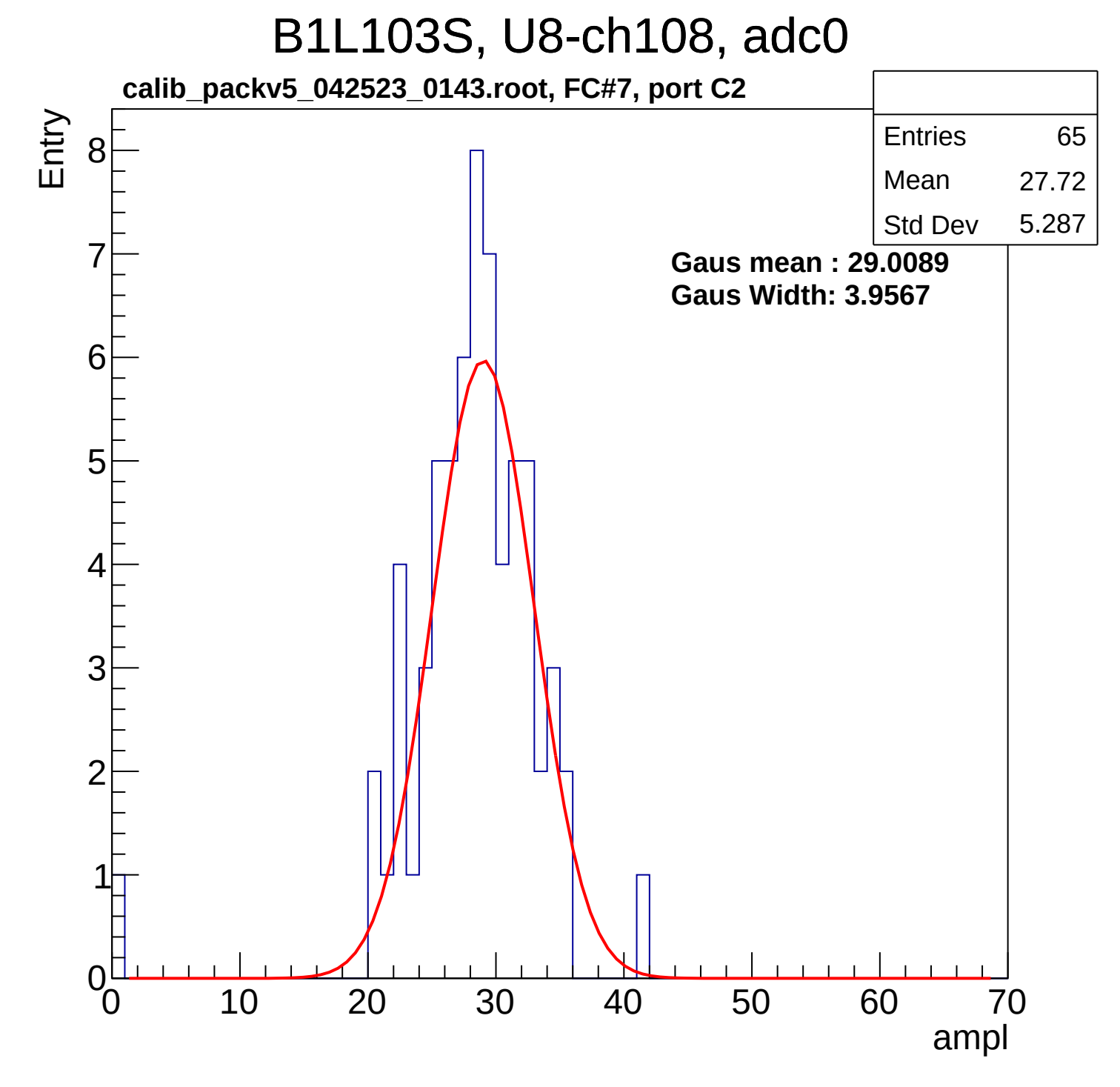

B1L103S, U8-ch107, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 50.75
Std Dev 3.466
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

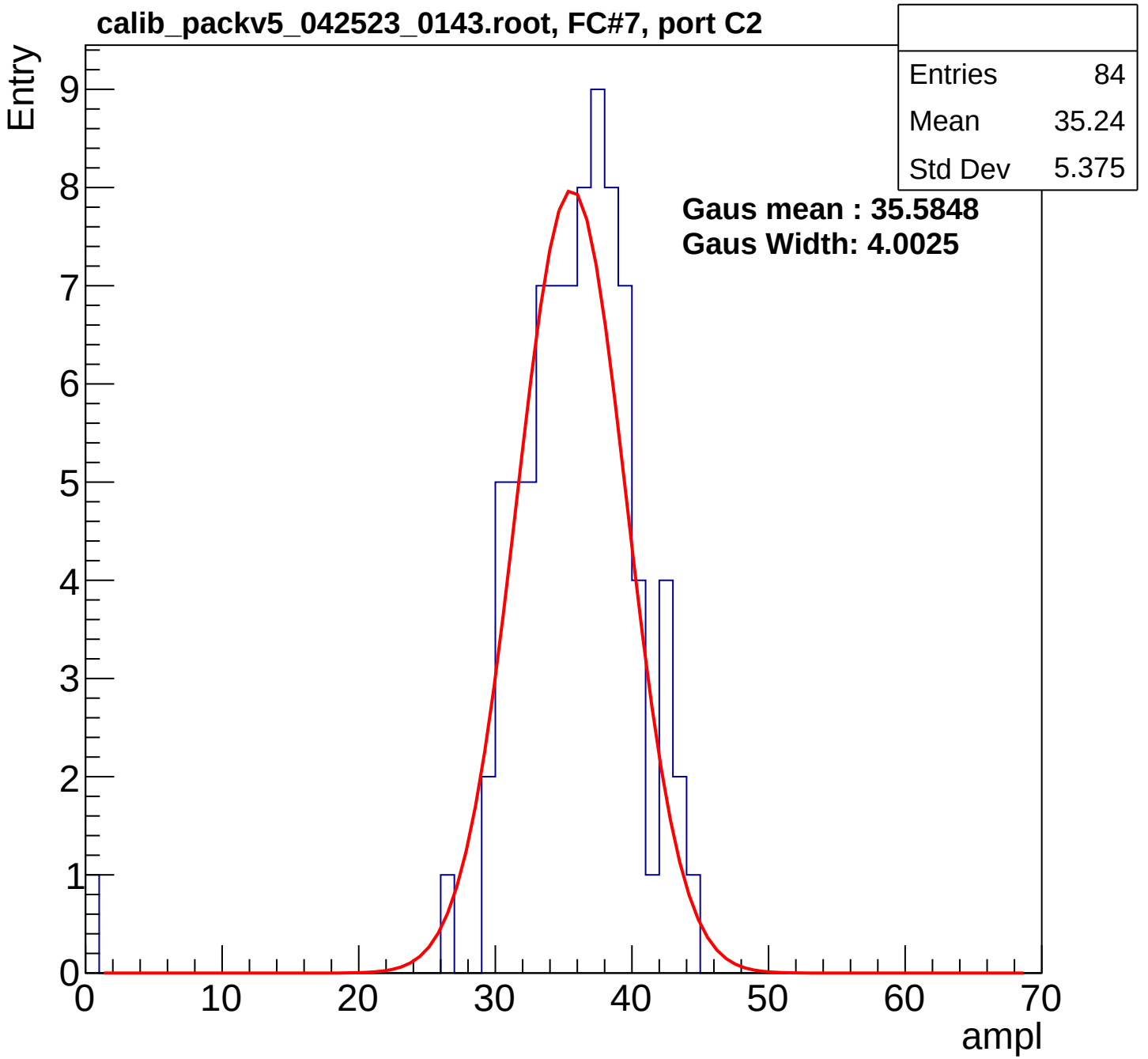

B1L103S, U8-ch107, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 46
Mean 56.02
Std Dev 3.28
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

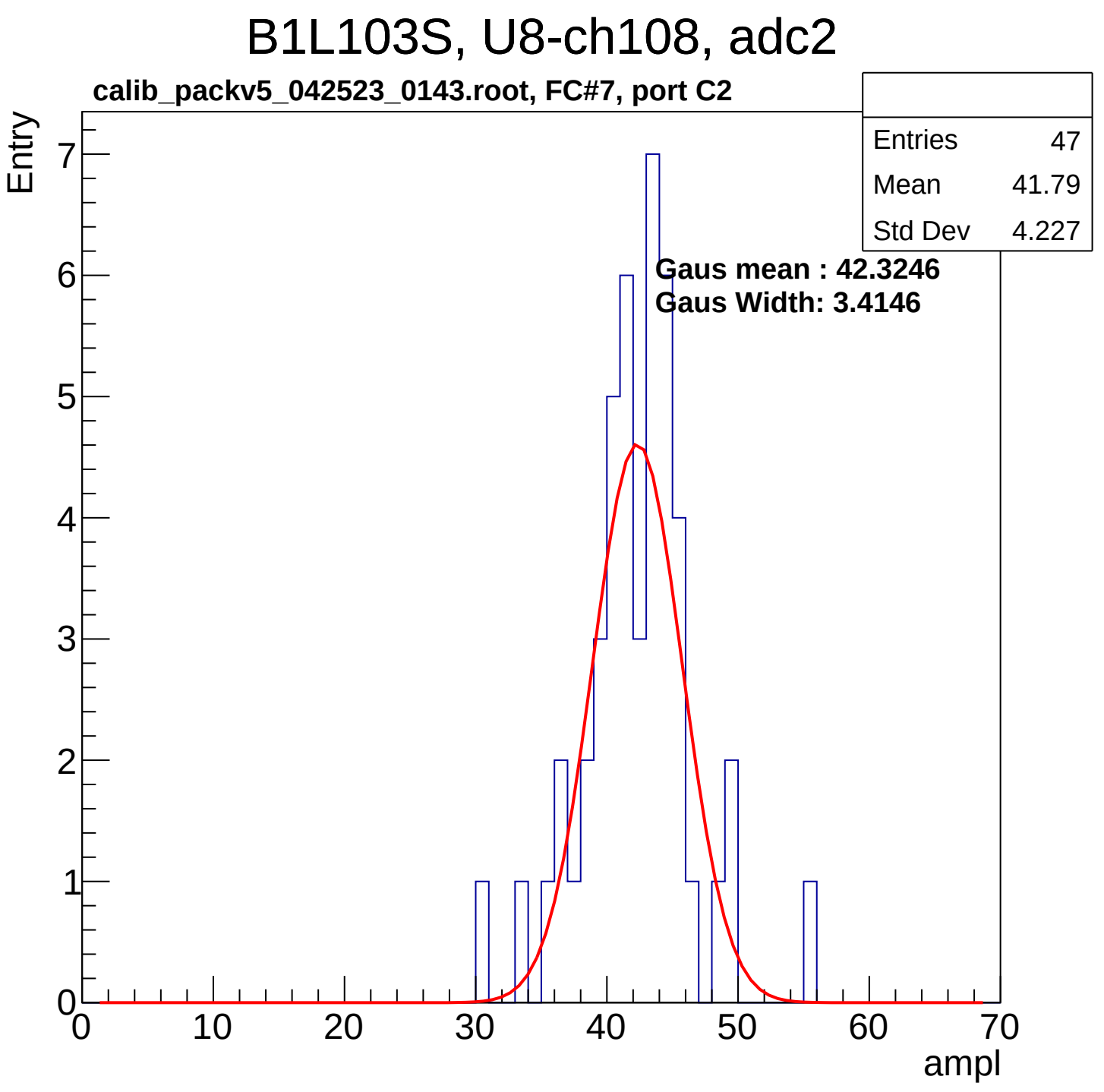

B1L103S, U8-ch107, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 58.71
Std Dev 8.921
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

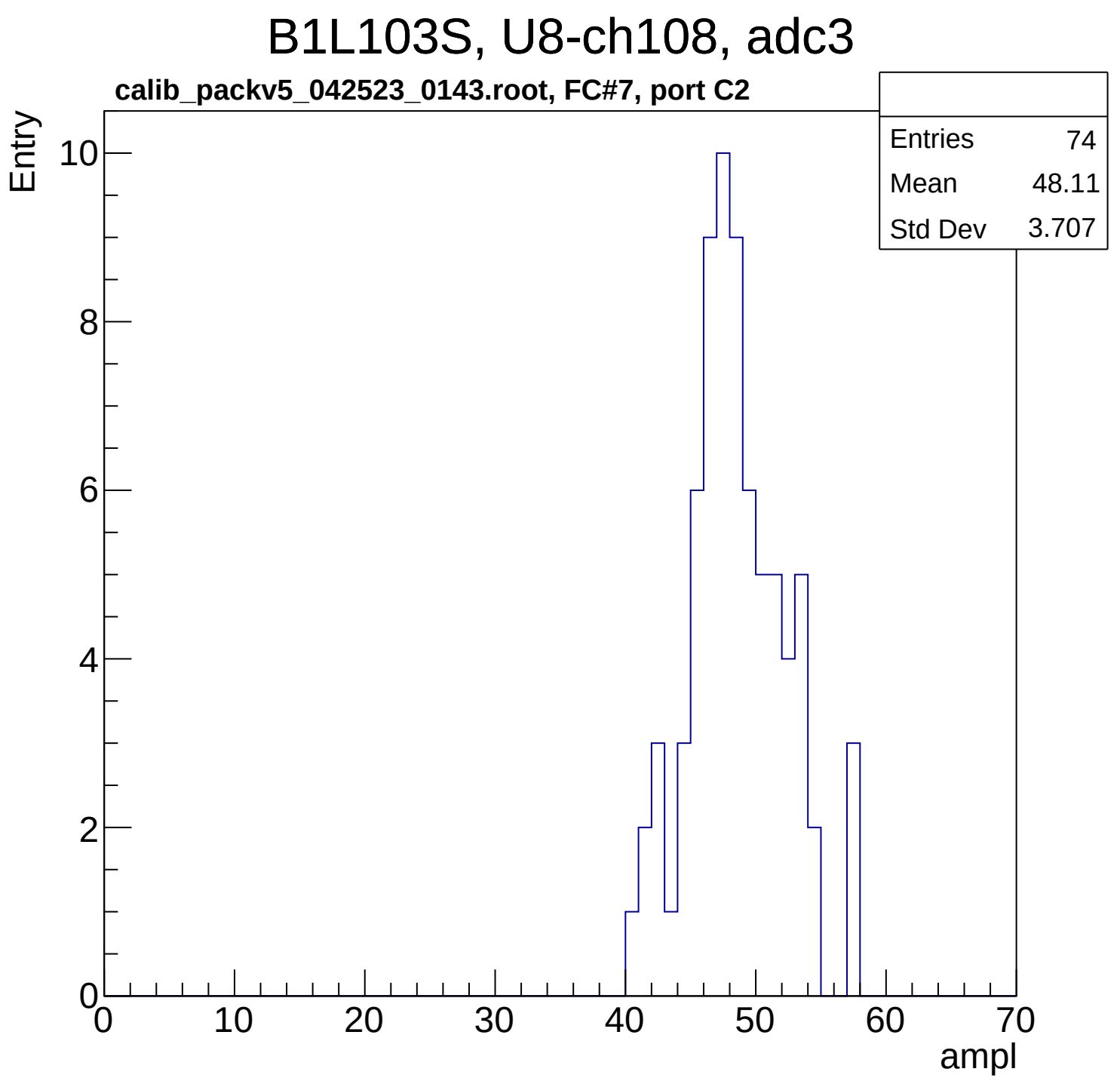

B1L103S, U8-ch107, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 62.33
Std Dev 0.9428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

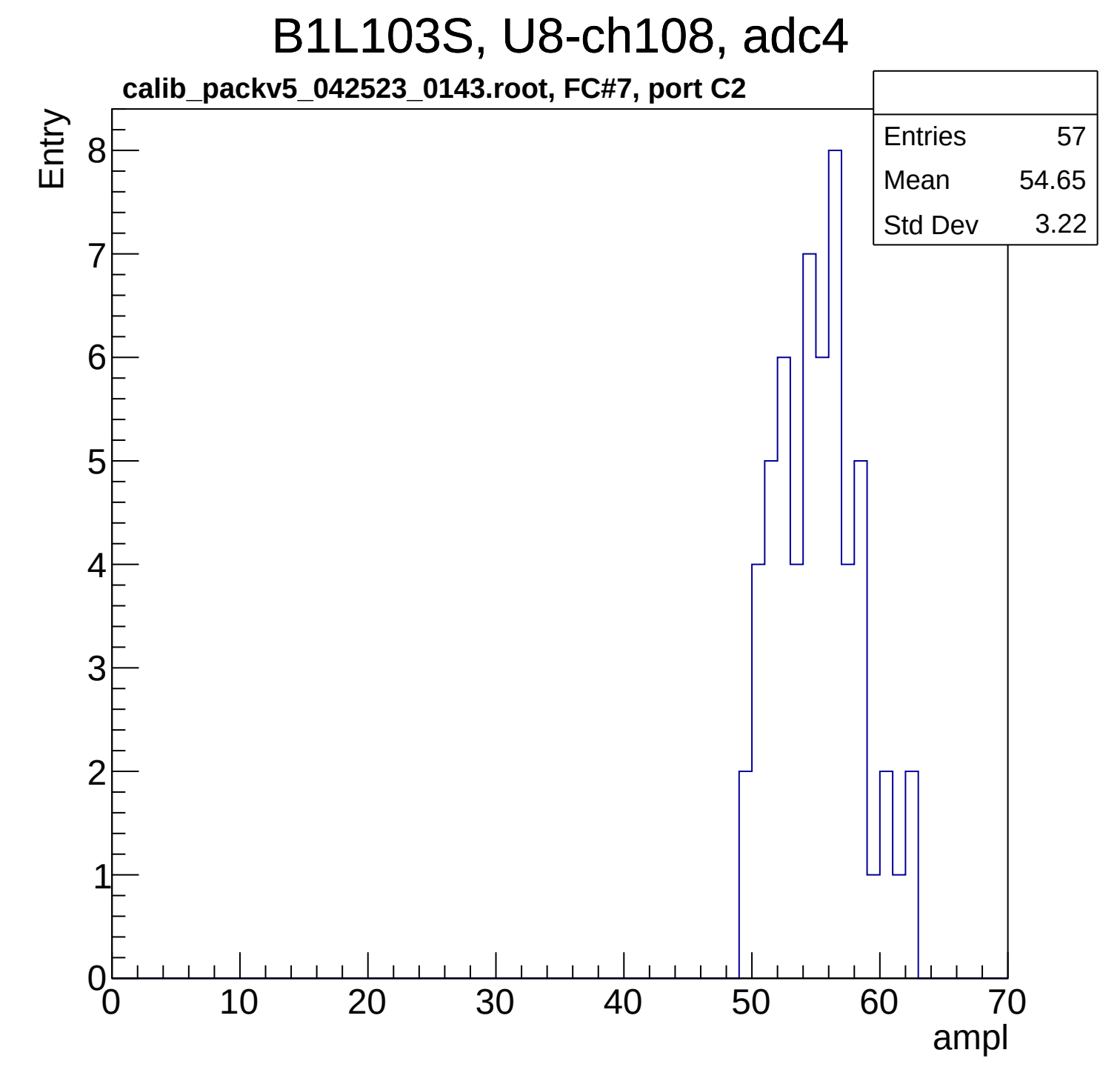

B1L103S, U8-ch107, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 21
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

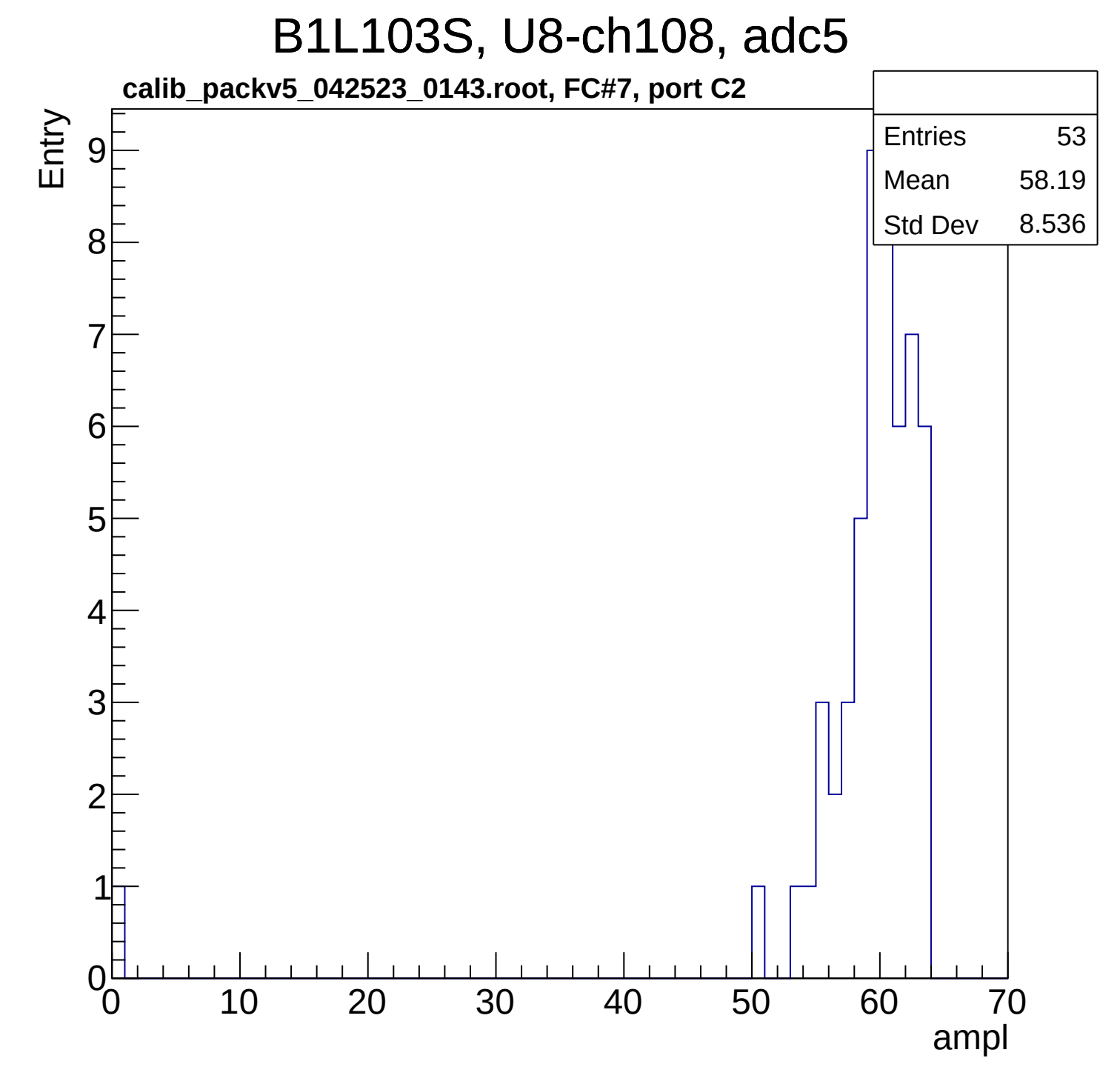

B1L103S, U8-ch108, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 27.72
Std Dev 5.287
Gaus mean : 29.0089
Gaus Width: 3.9567
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

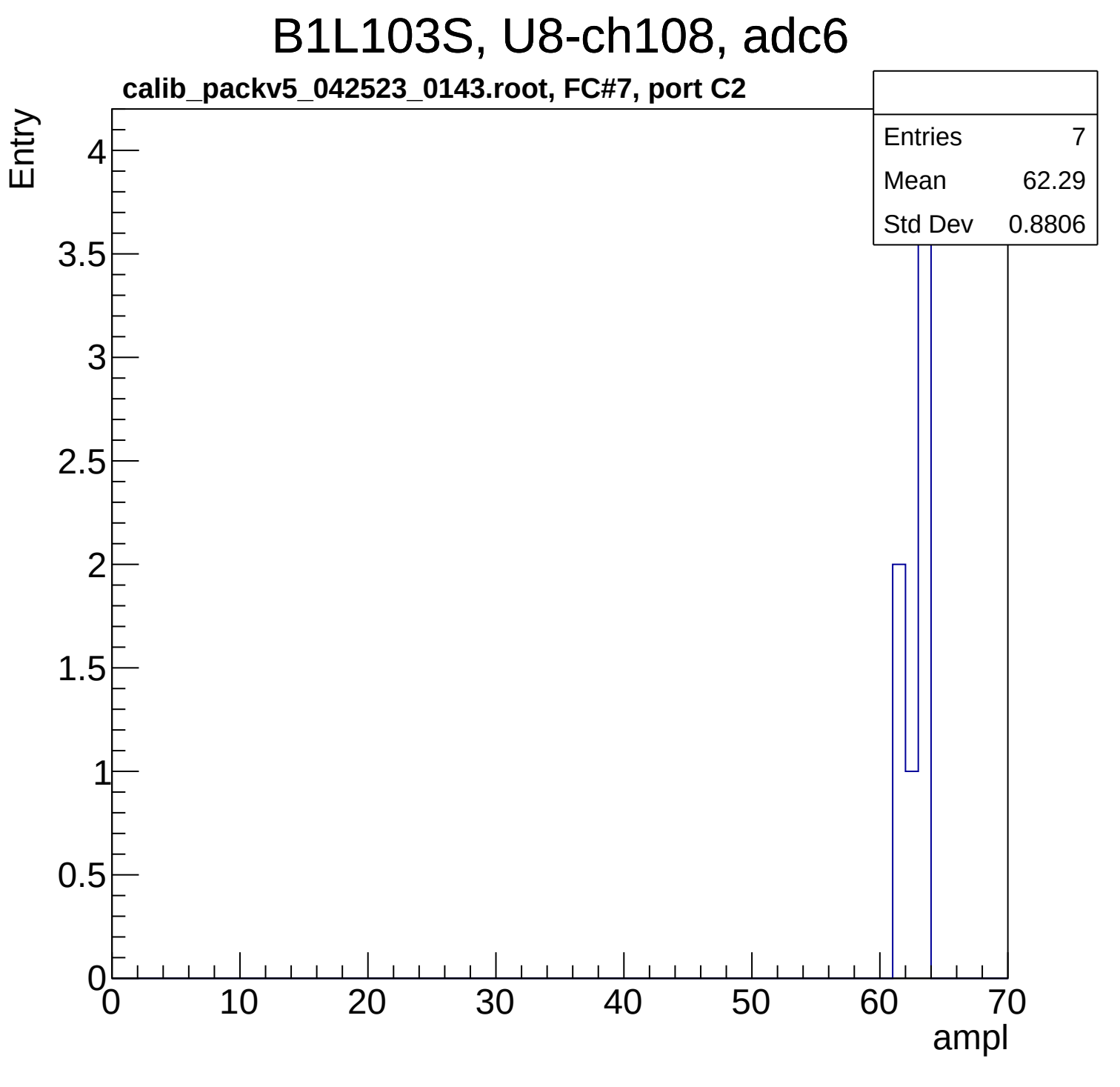

B1L103S, U8-ch108, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 84
Mean 35.24
Std Dev 5.375
Gaus mean : 35.5848
Gaus Width: 4.0025
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

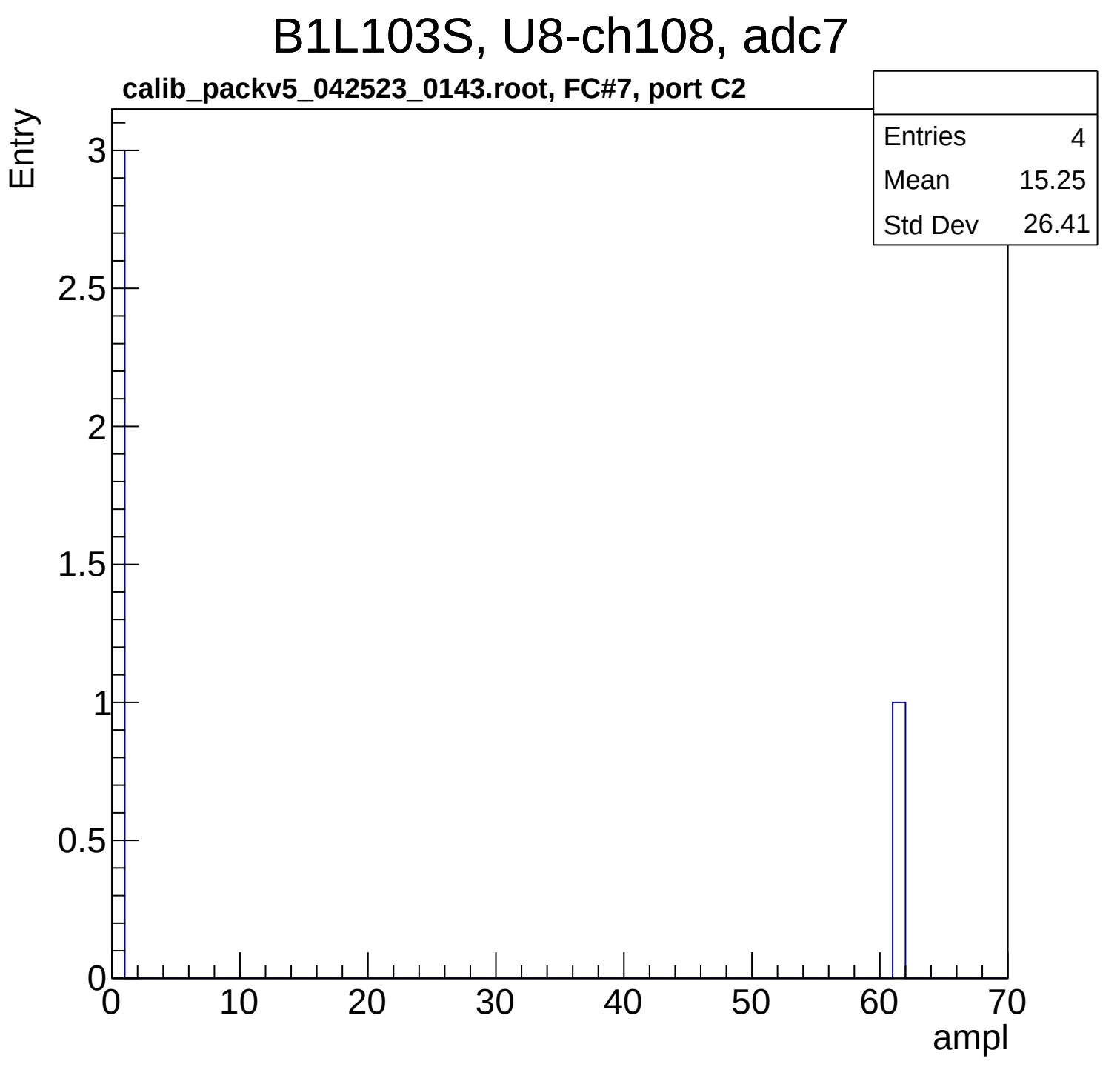

B1L103S, U8-ch108, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 47
Mean 41.79
Std Dev 4.227
Gaus mean : 42.3246
Gaus Width: 3.4146
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

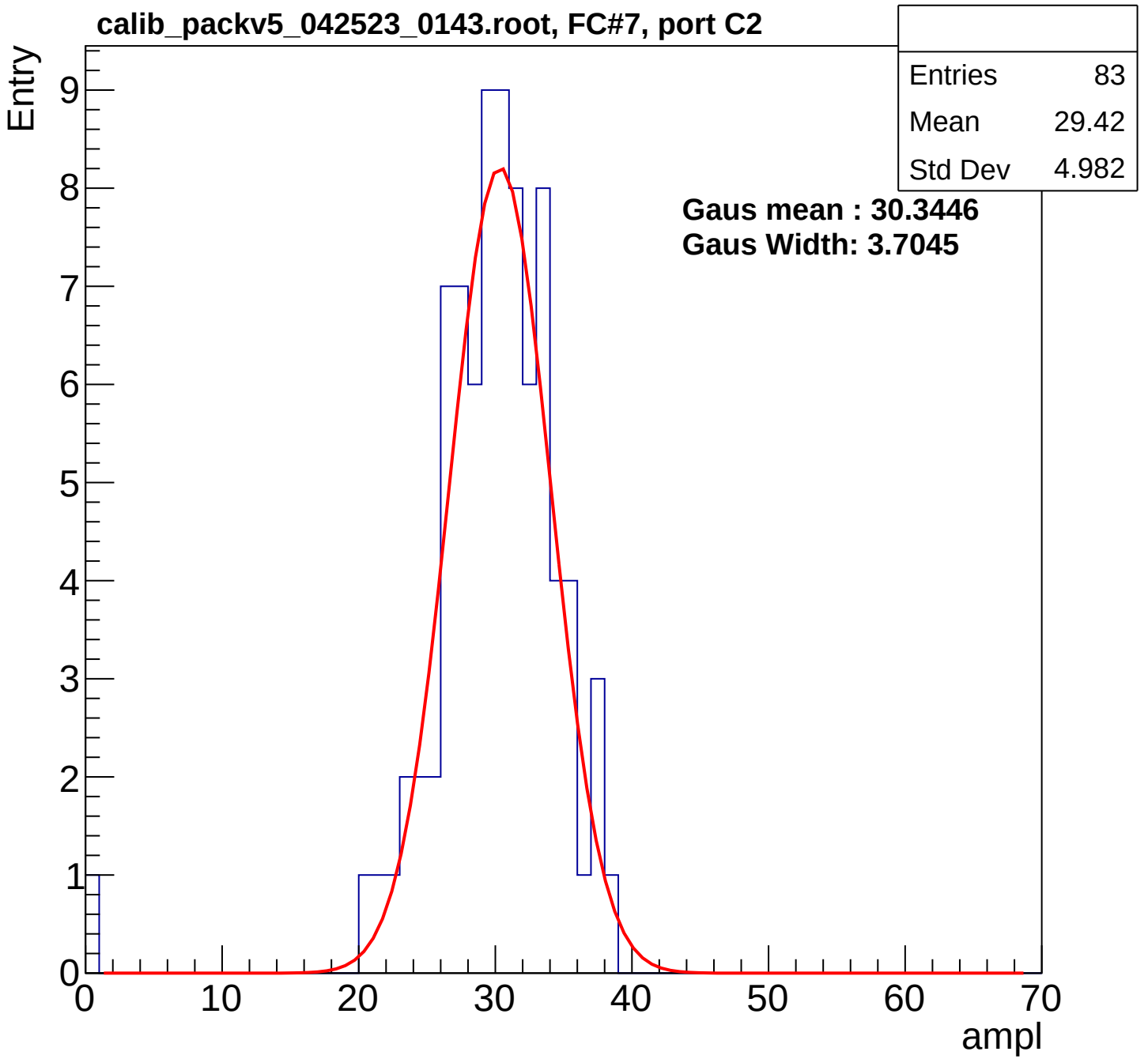

B1L103S, U8-ch108, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 48.11
Std Dev 3.707
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

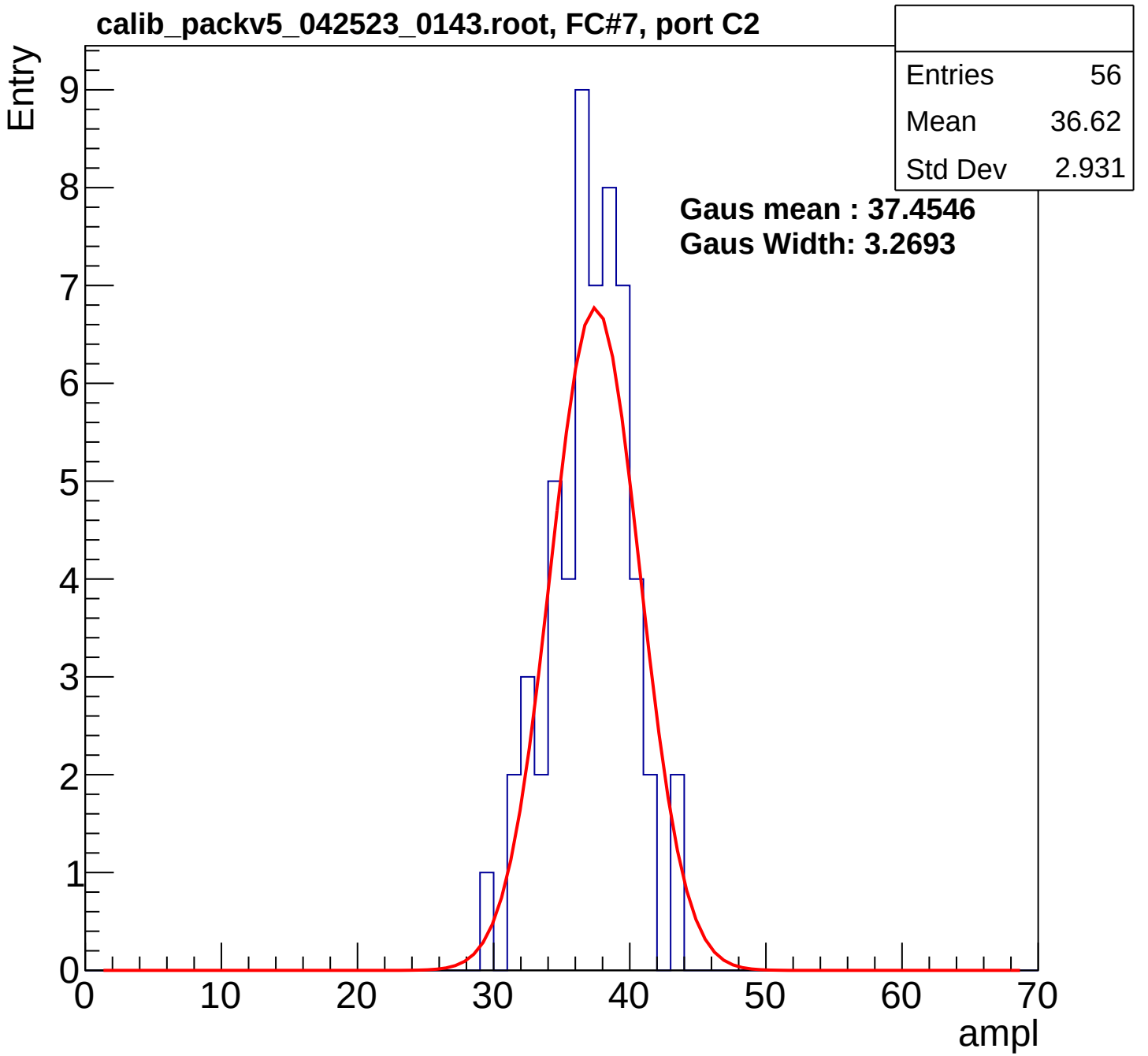

B1L103S, U8-ch108, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 54.65
Std Dev 3.22
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

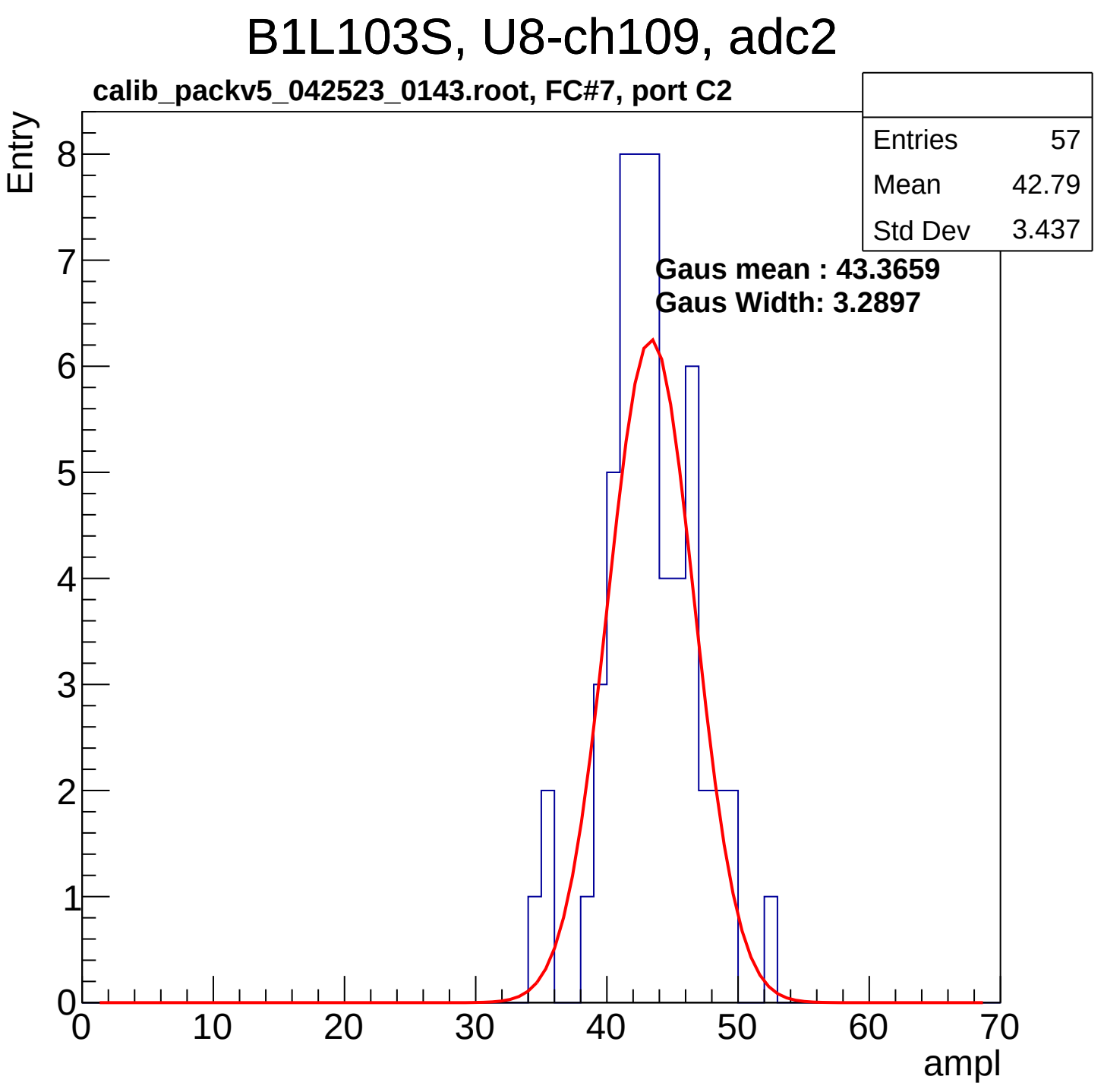

B1L103S, U8-ch108, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 58.19
Std Dev 8.536
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

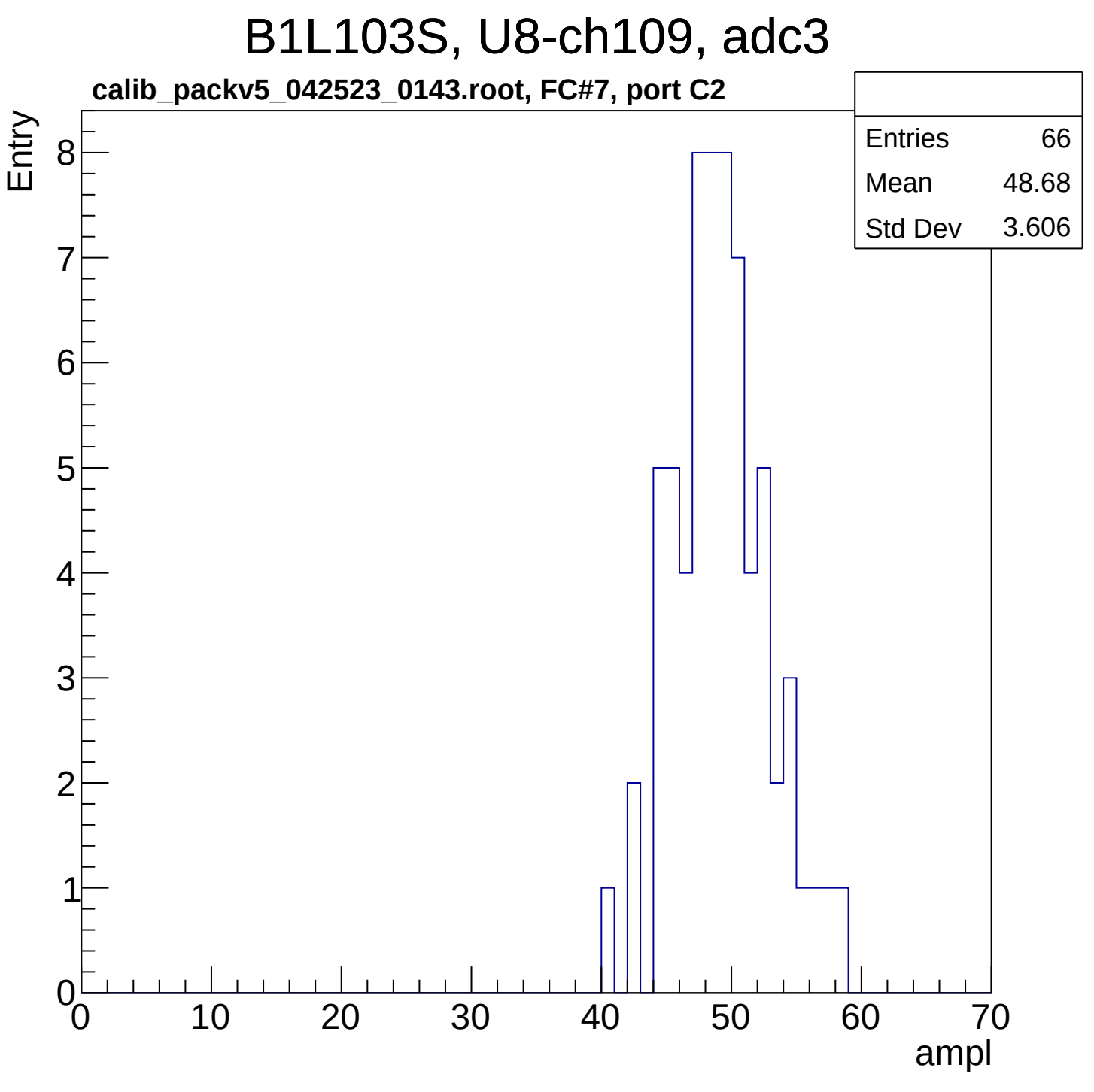

B1L103S, U8-ch108, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 7
Mean 62.29
Std Dev 0.8806
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

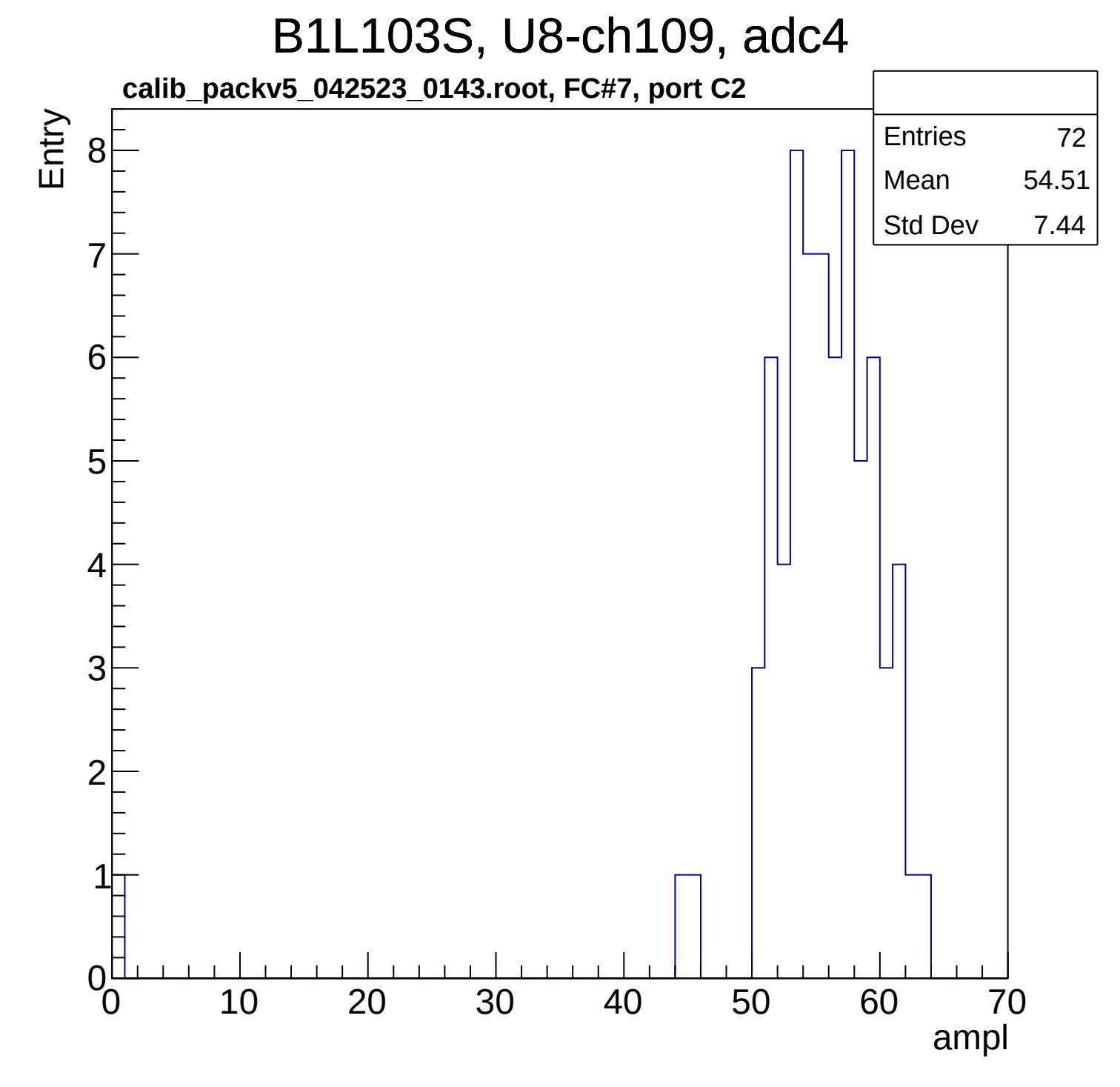

B1L103S, U8-ch108, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 15.25
Std Dev 26.41
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

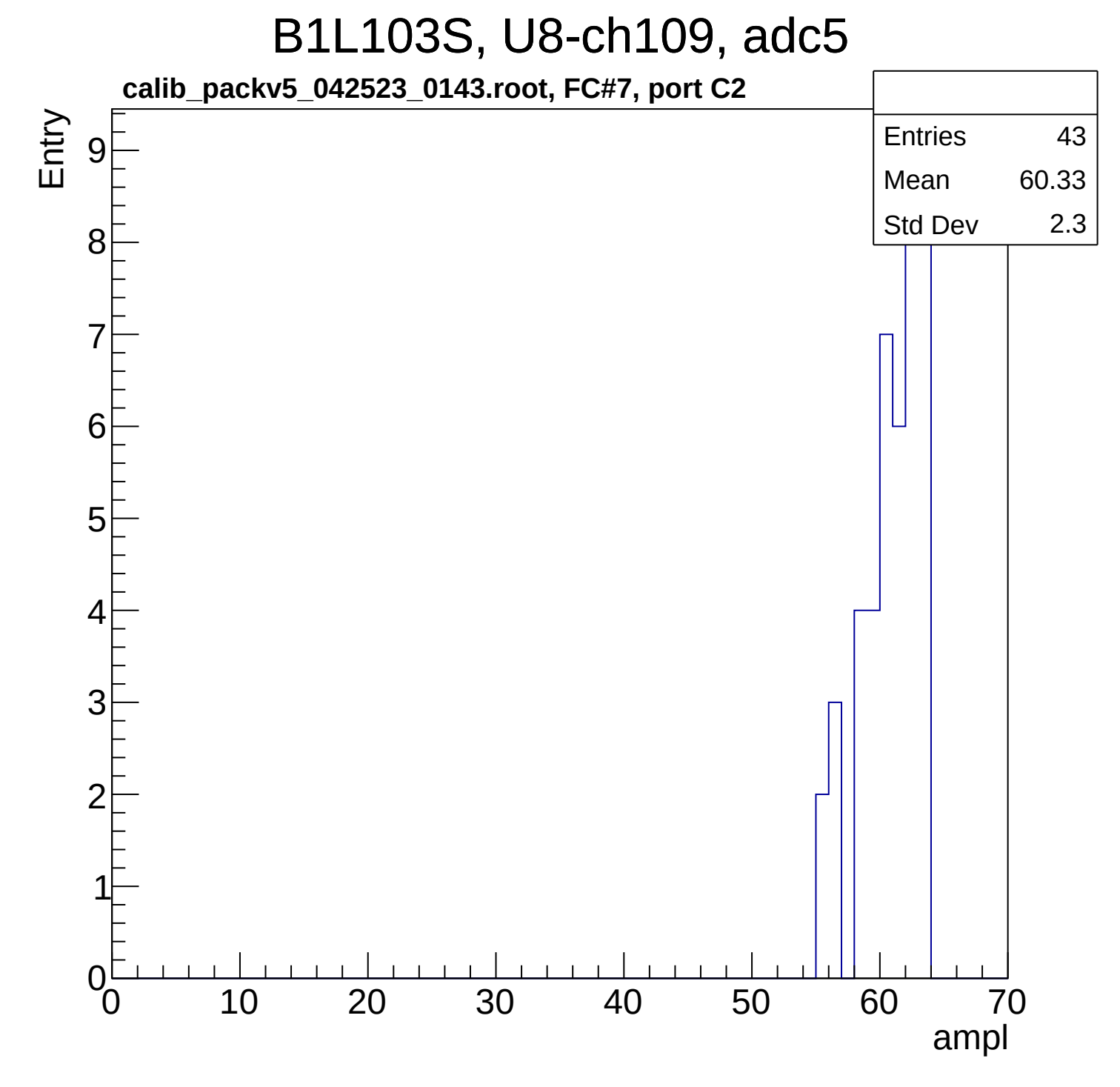

B1L103S, U8-ch109, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 83
Mean 29.42
Std Dev 4.982
Gaus mean : 30.3446
Gaus Width: 3.7045
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

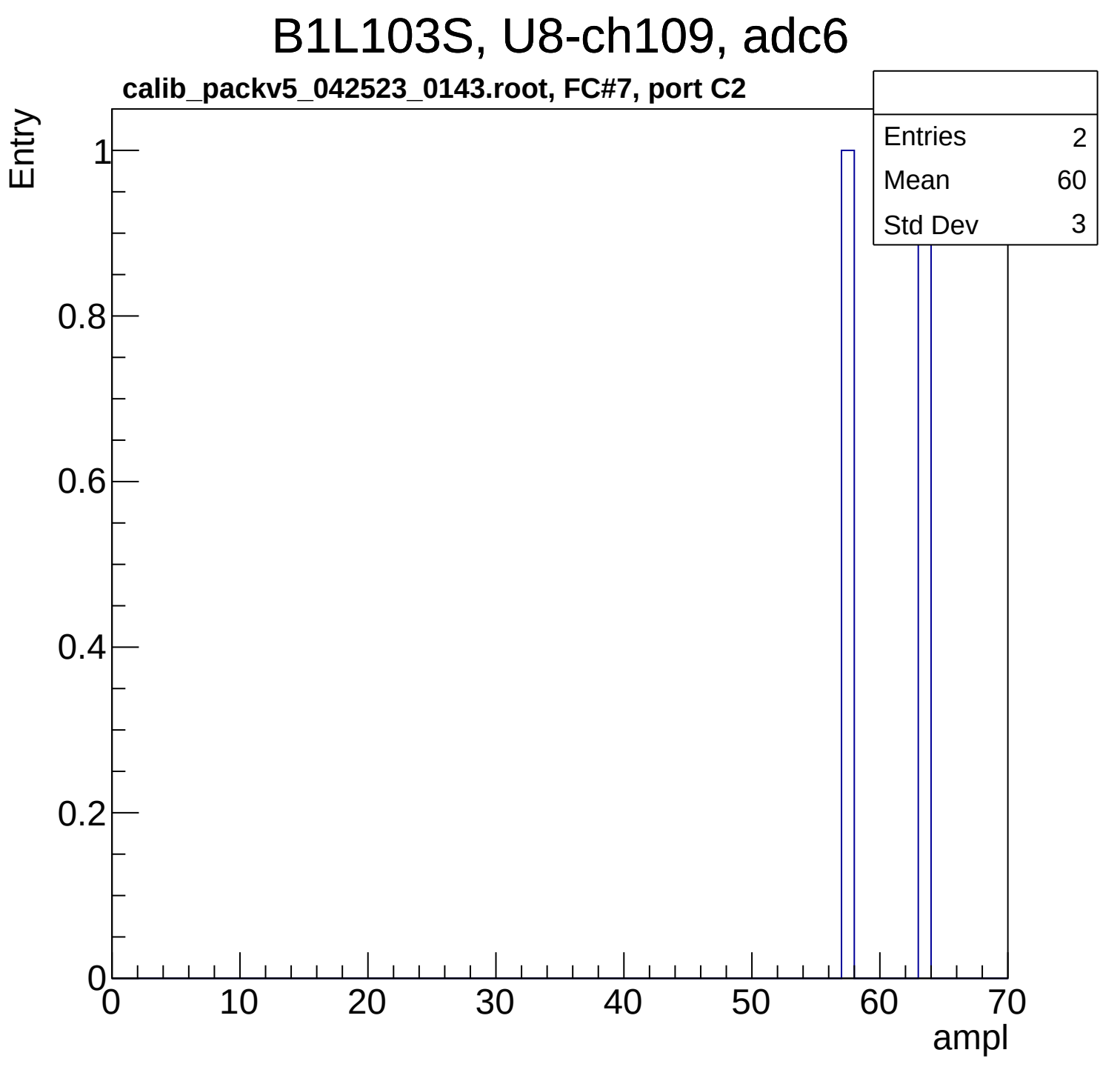

B1L103S, U8-ch109, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 36.62
Std Dev 2.931
Gaus mean : 37.4546
Gaus Width: 3.2693
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

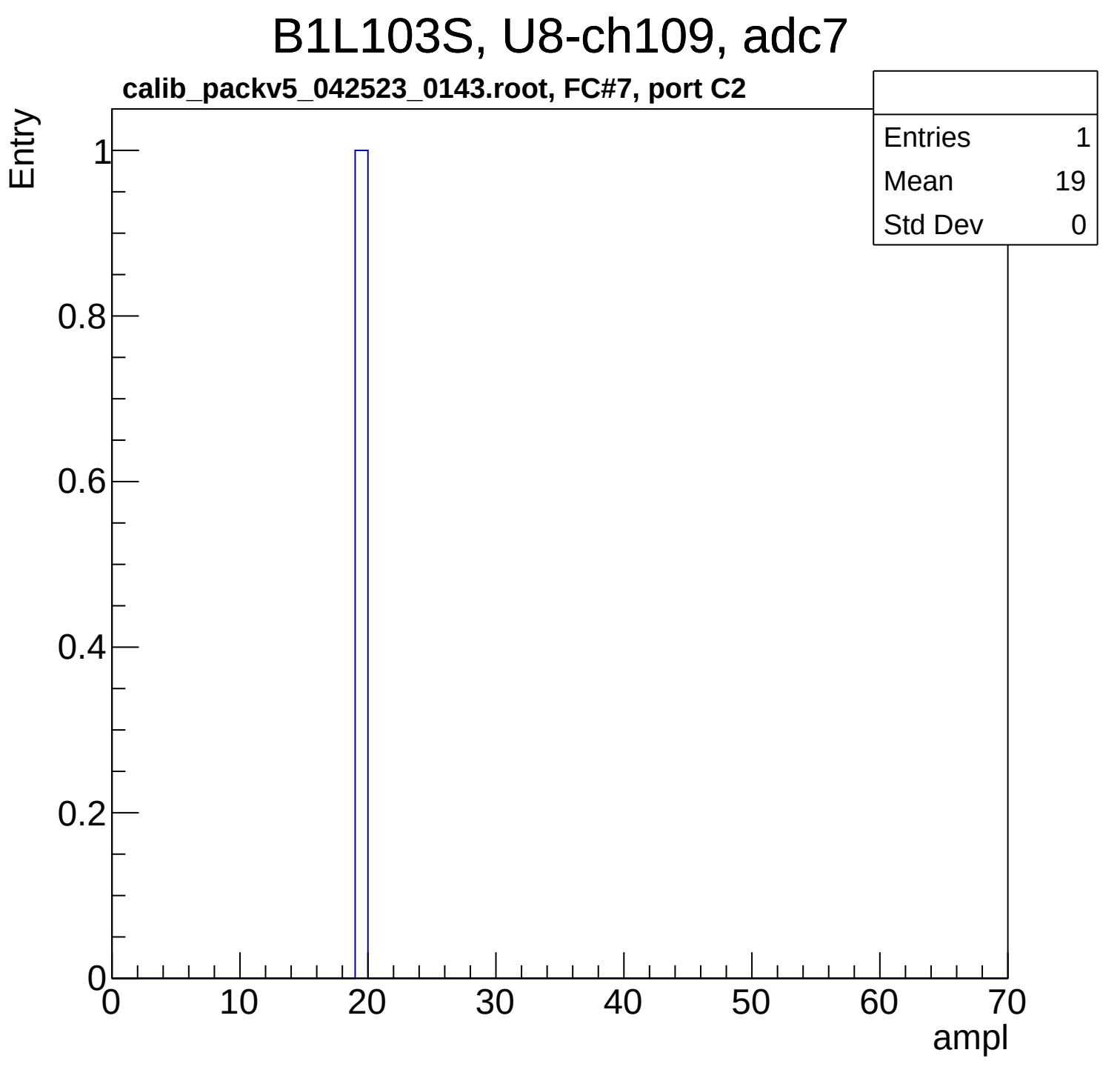

B1L103S, U8-ch109, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 42.79
Std Dev 3.437
Gaus mean : 43.3659
Gaus Width: 3.2897
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

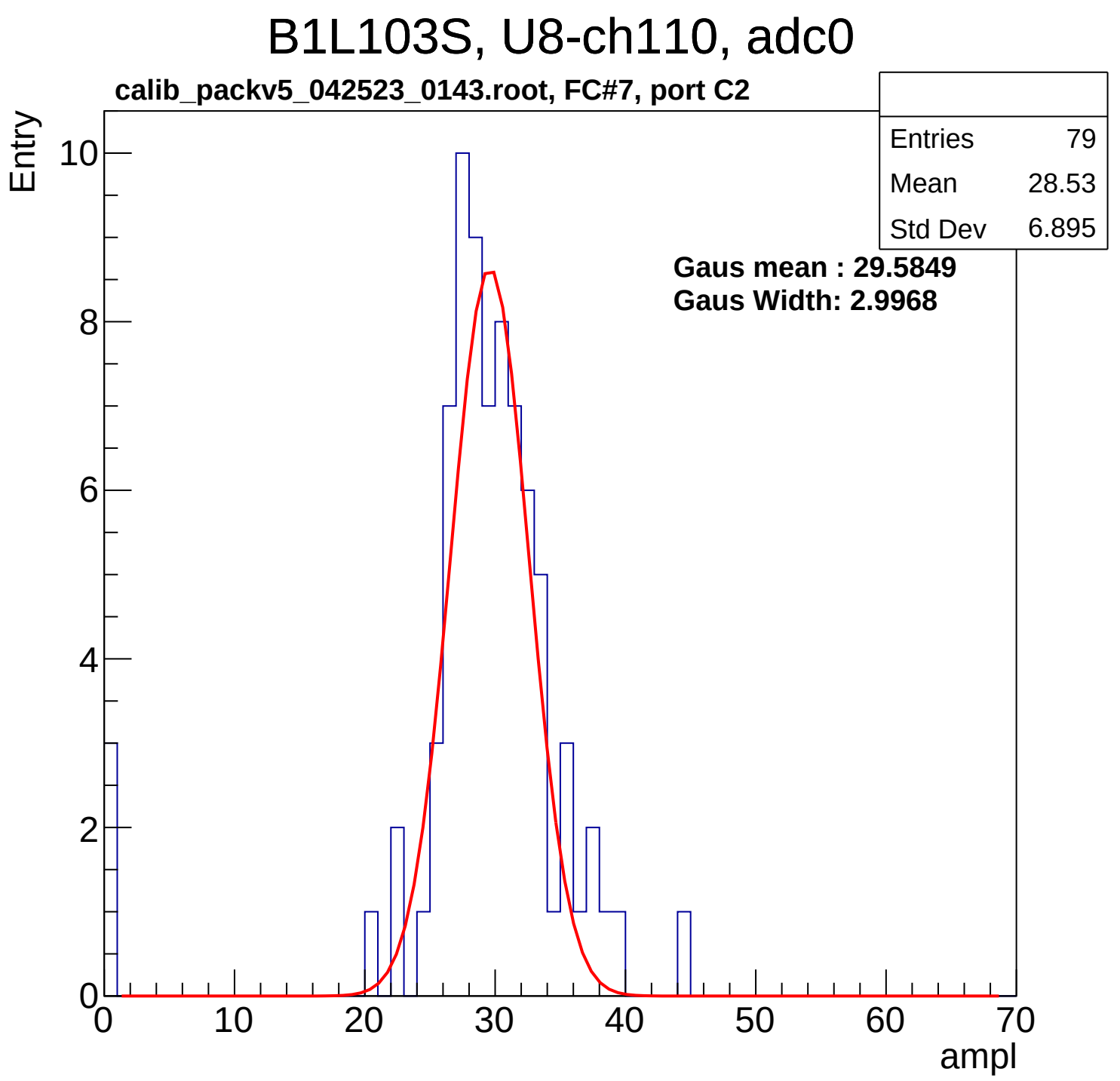

B1L103S, U8-ch109, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 48.68
Std Dev 3.606
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

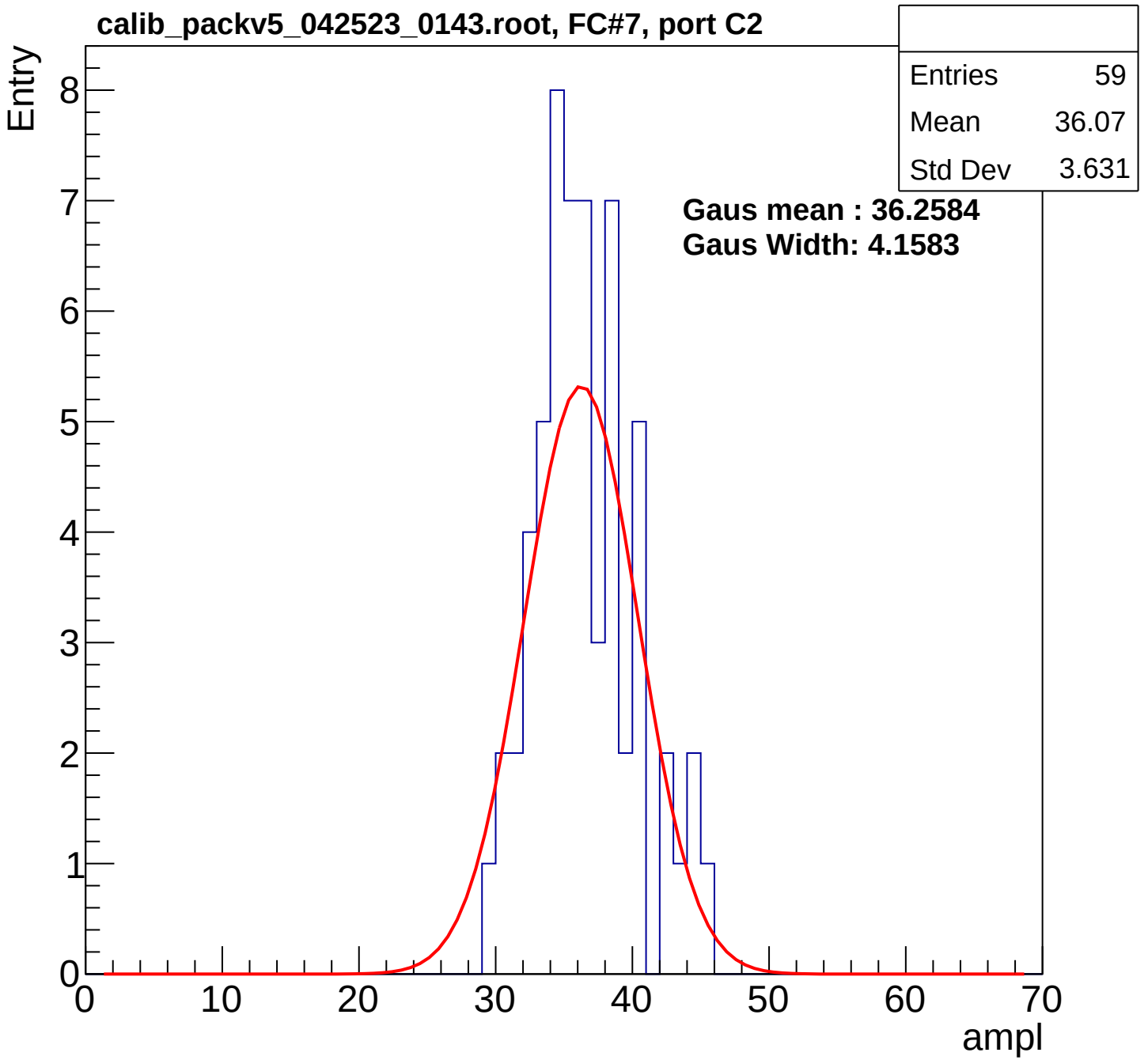

B1L103S, U8-ch109, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 54.51
Std Dev 7.44
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

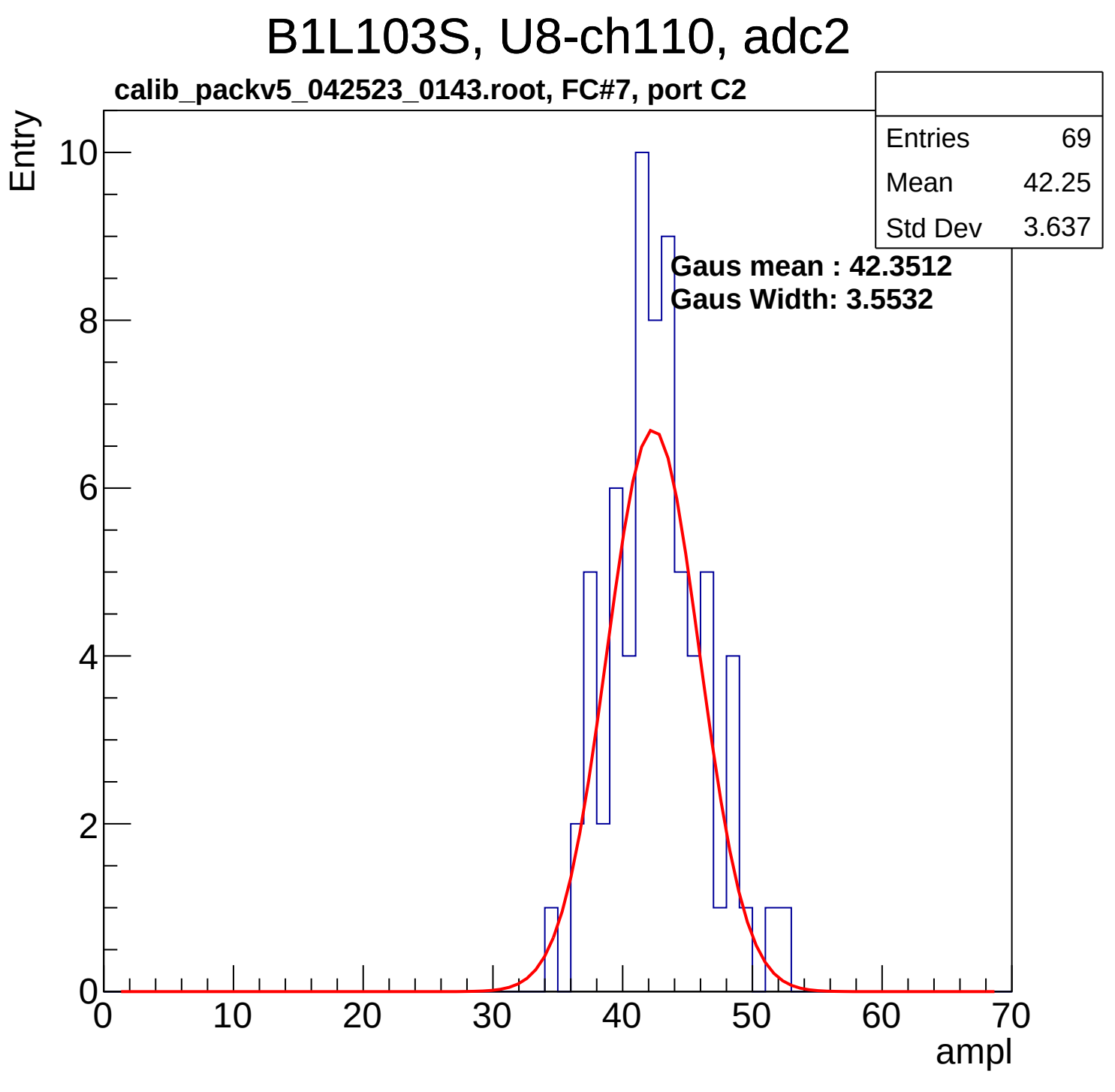

B1L103S, U8-ch109, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 43
Mean 60.33
Std Dev 2.3
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

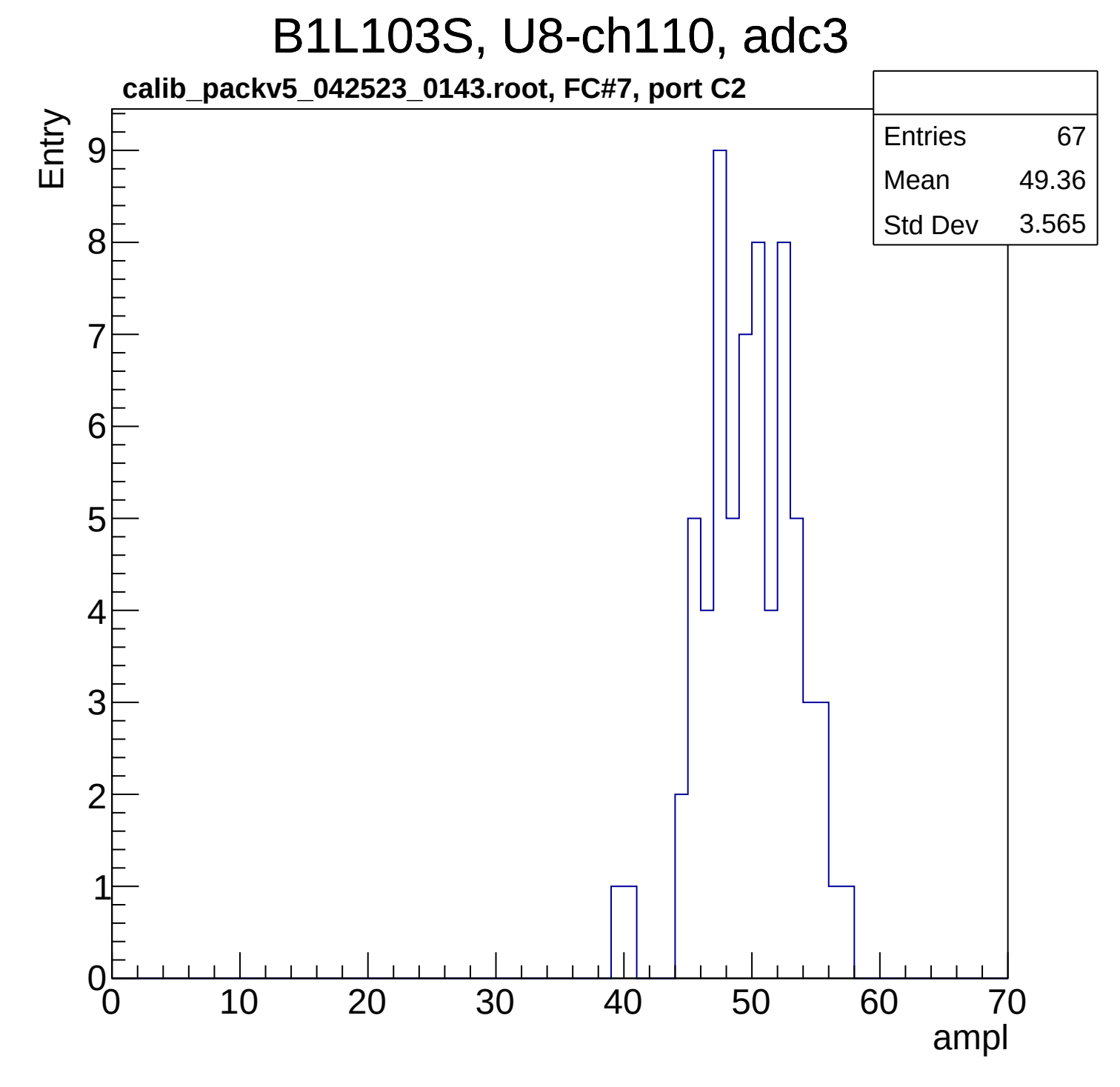

B1L103S, U8-ch109, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 60
Std Dev 3
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

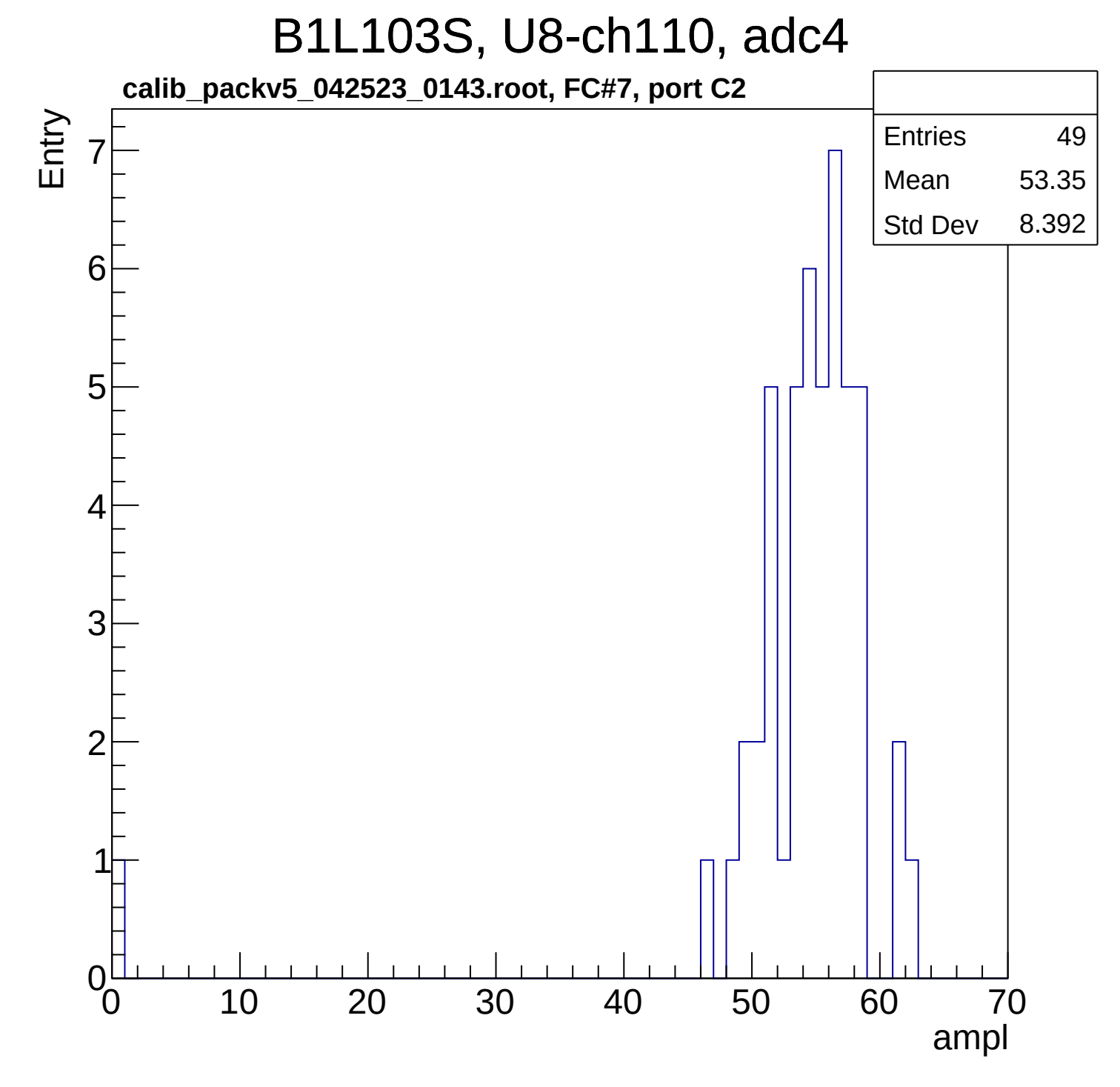

B1L103S, U8-ch109, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 19
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

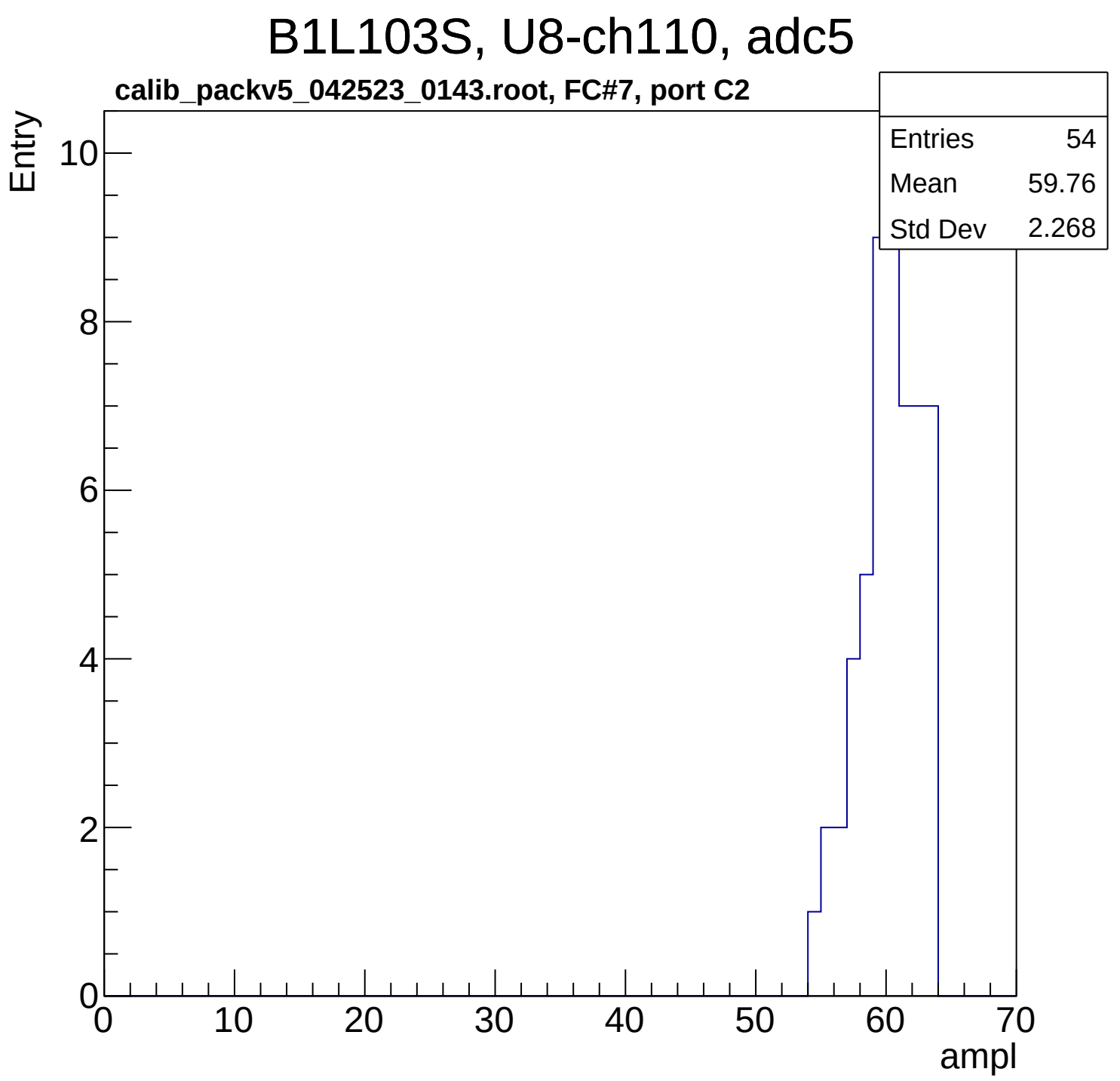

B1L103S, U8-ch110, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 79
Mean 28.53
Std Dev 6.895
Gaus mean : 29.5849
Gaus Width: 2.9968
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

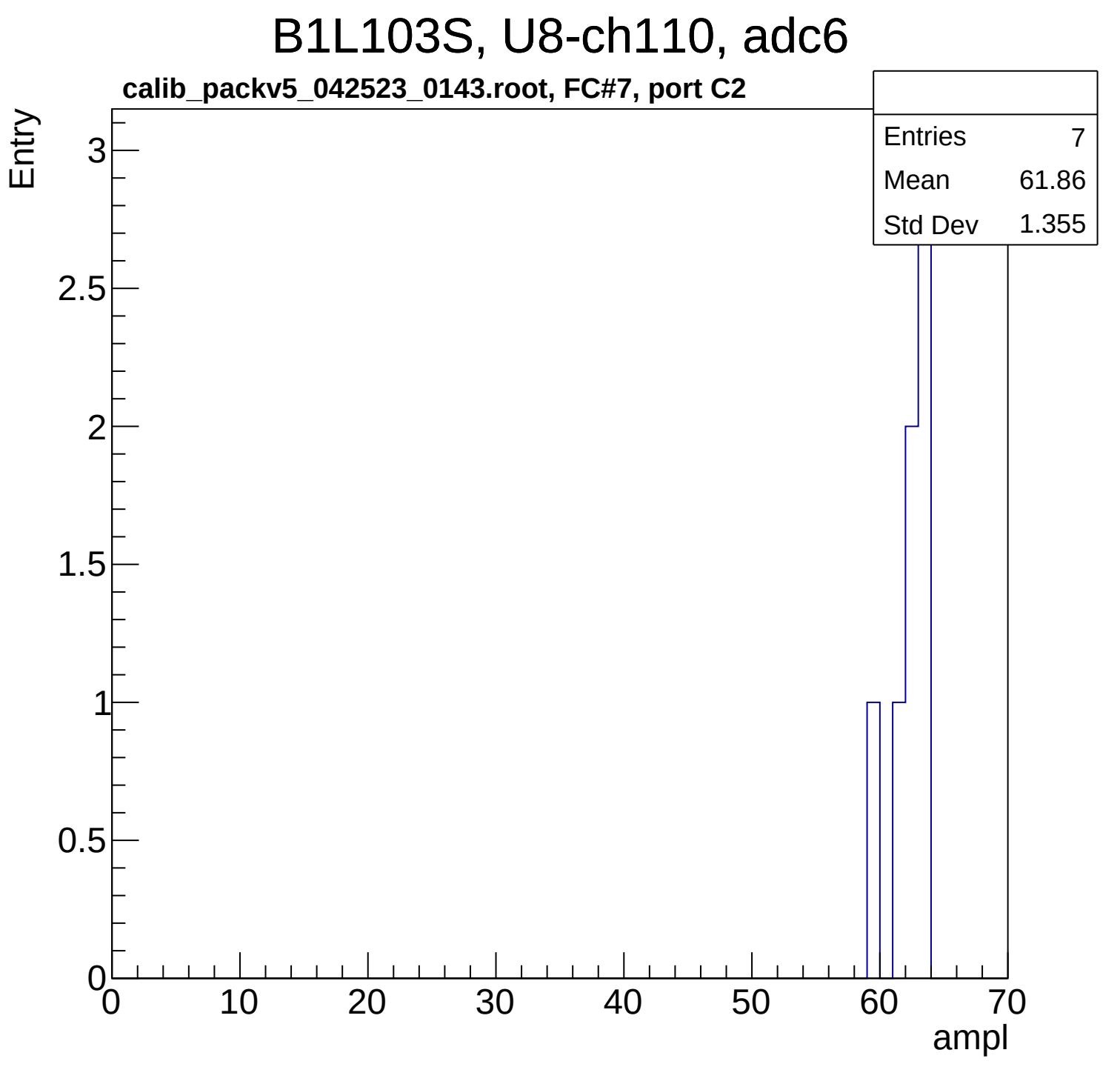

B1L103S, U8-ch110, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 36.07
Std Dev 3.631
Gaus mean : 36.2584
Gaus Width: 4.1583
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

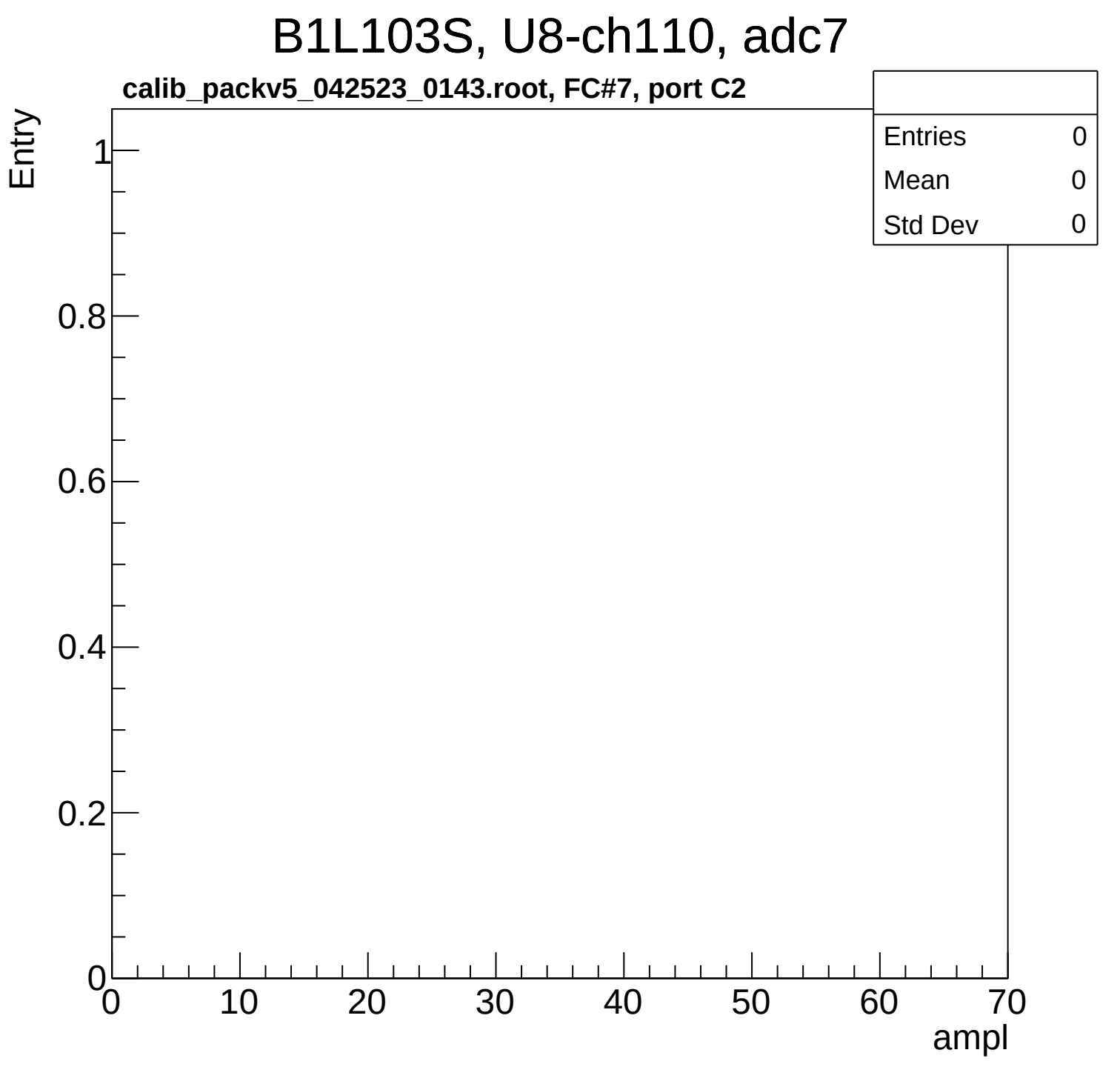

B1L103S, U8-ch110, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 42.25
Std Dev 3.637
Gaus mean : 42.3512
Gaus Width: 3.5532
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

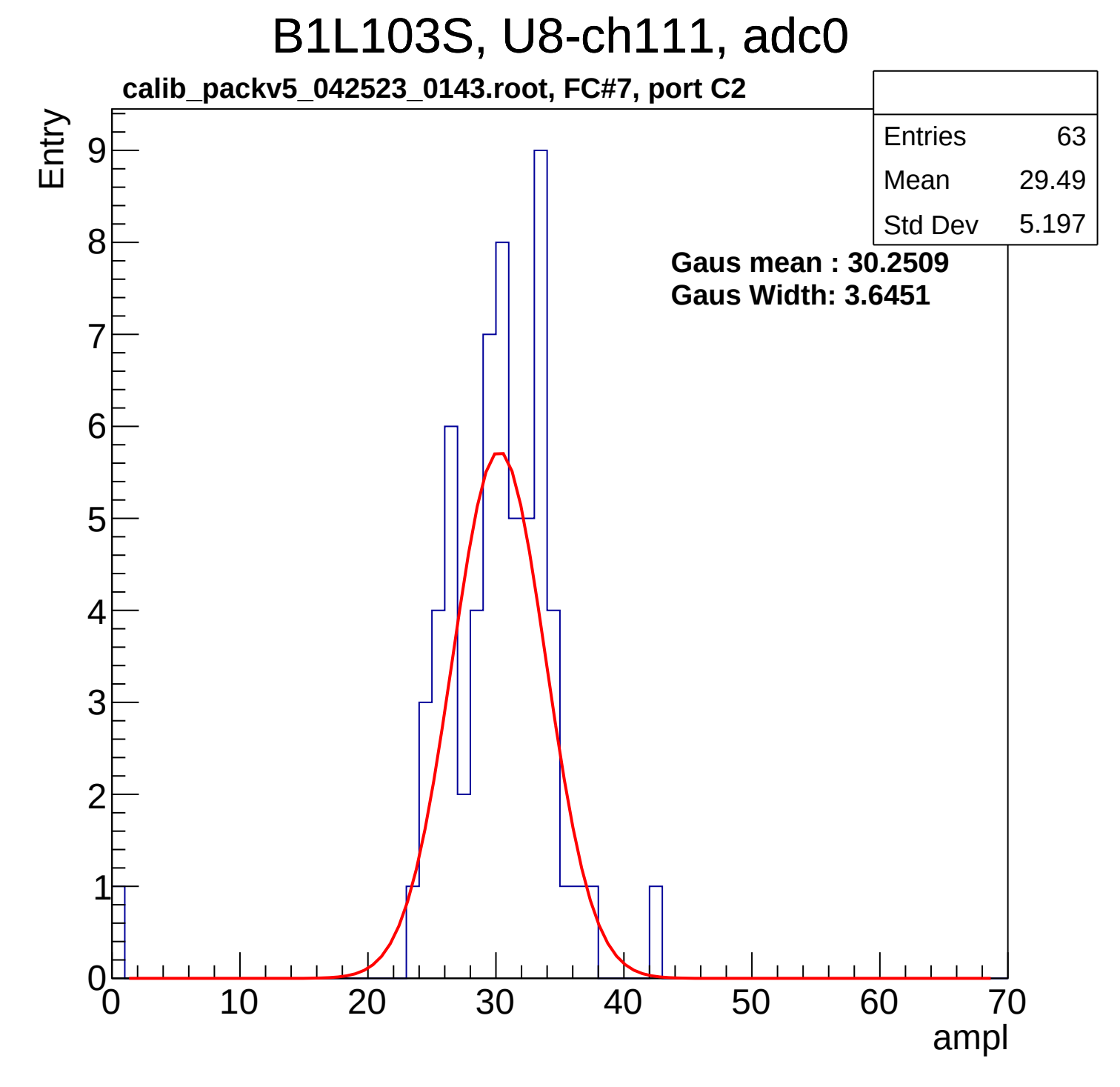

B1L103S, U8-ch110, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 49.36
Std Dev 3.565
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

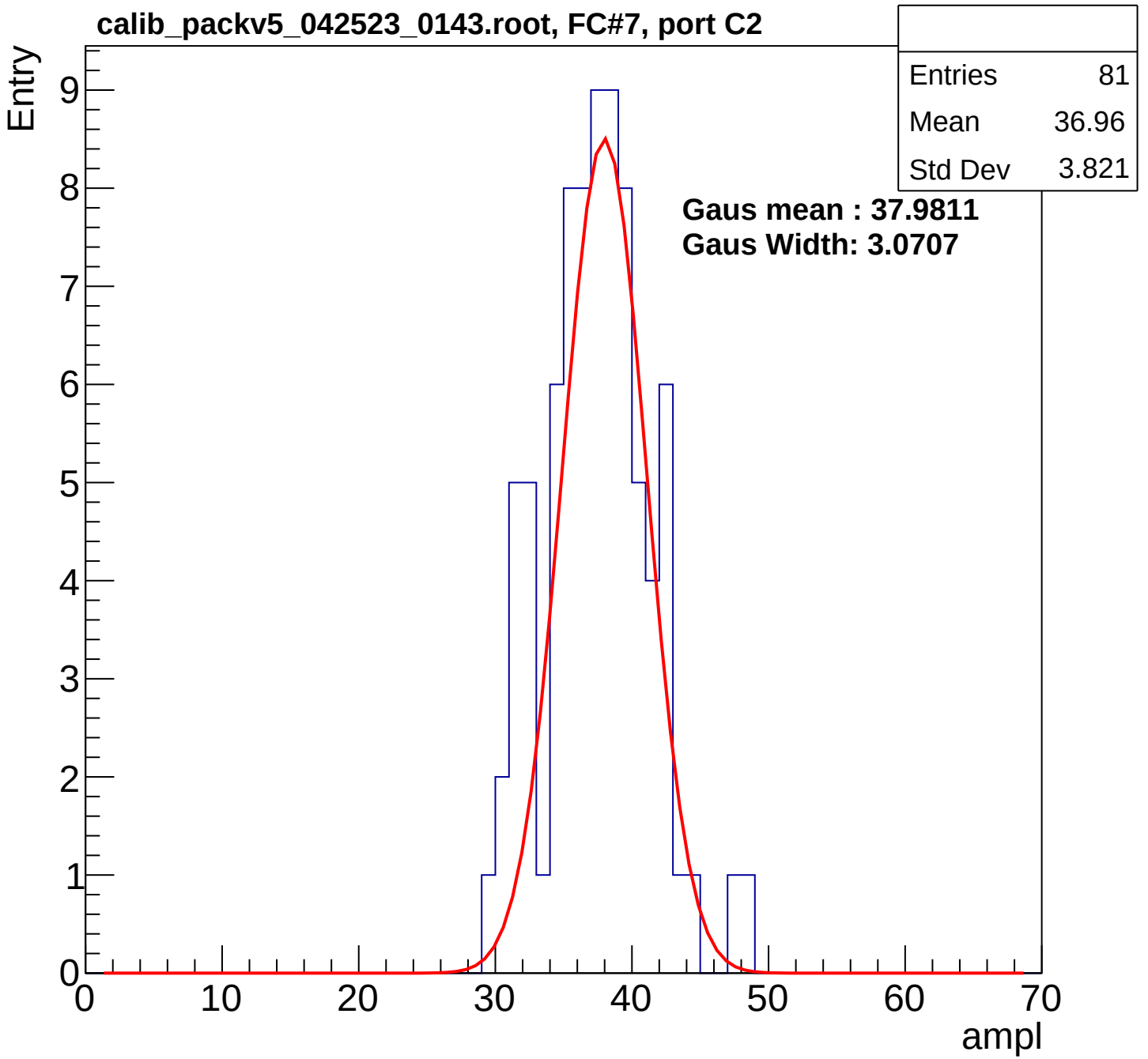

B1L103S, U8-ch110, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 53.35
Std Dev 8.392
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

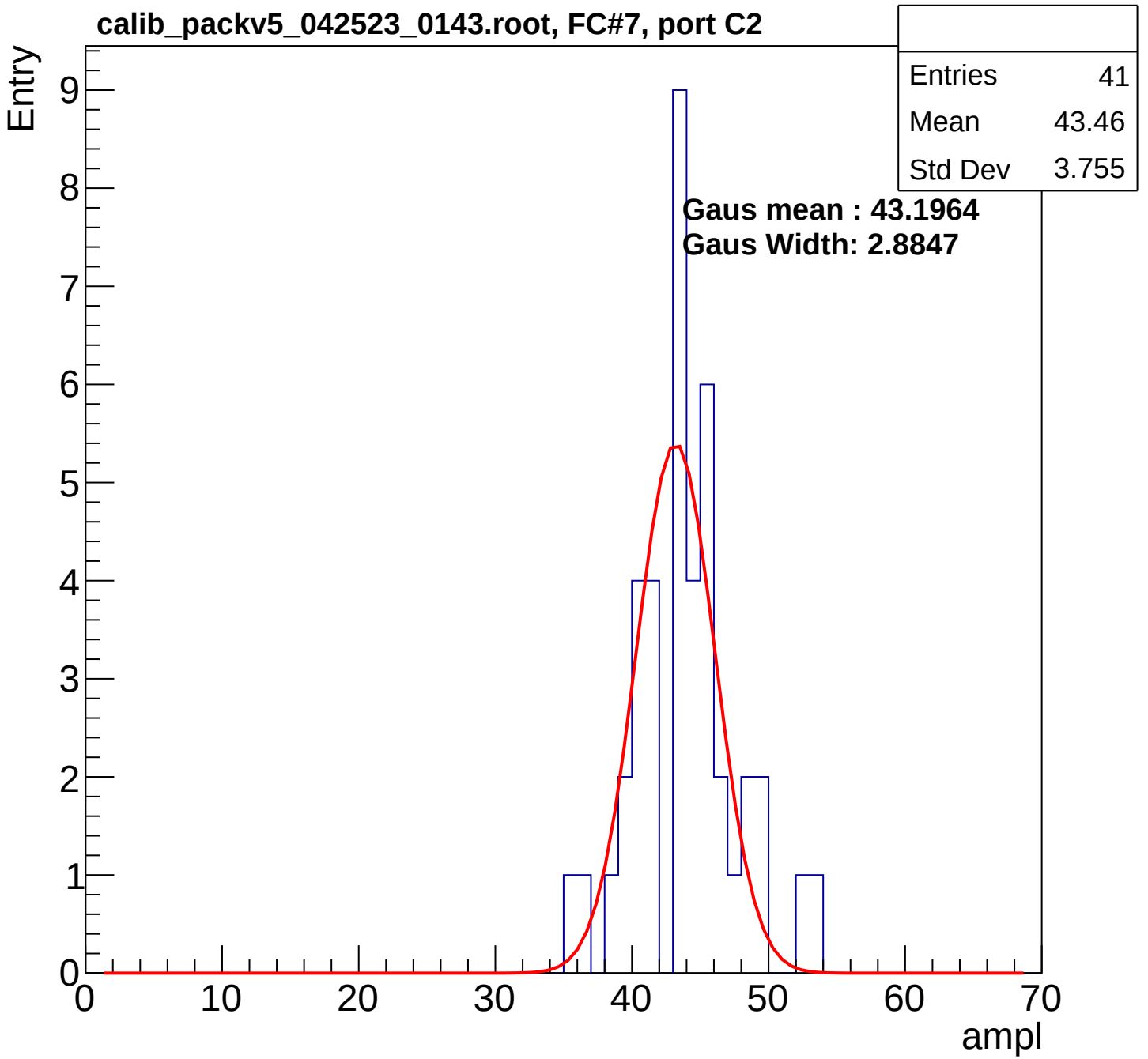

B1L103S, U8-ch110, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 59.76
Std Dev 2.268
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

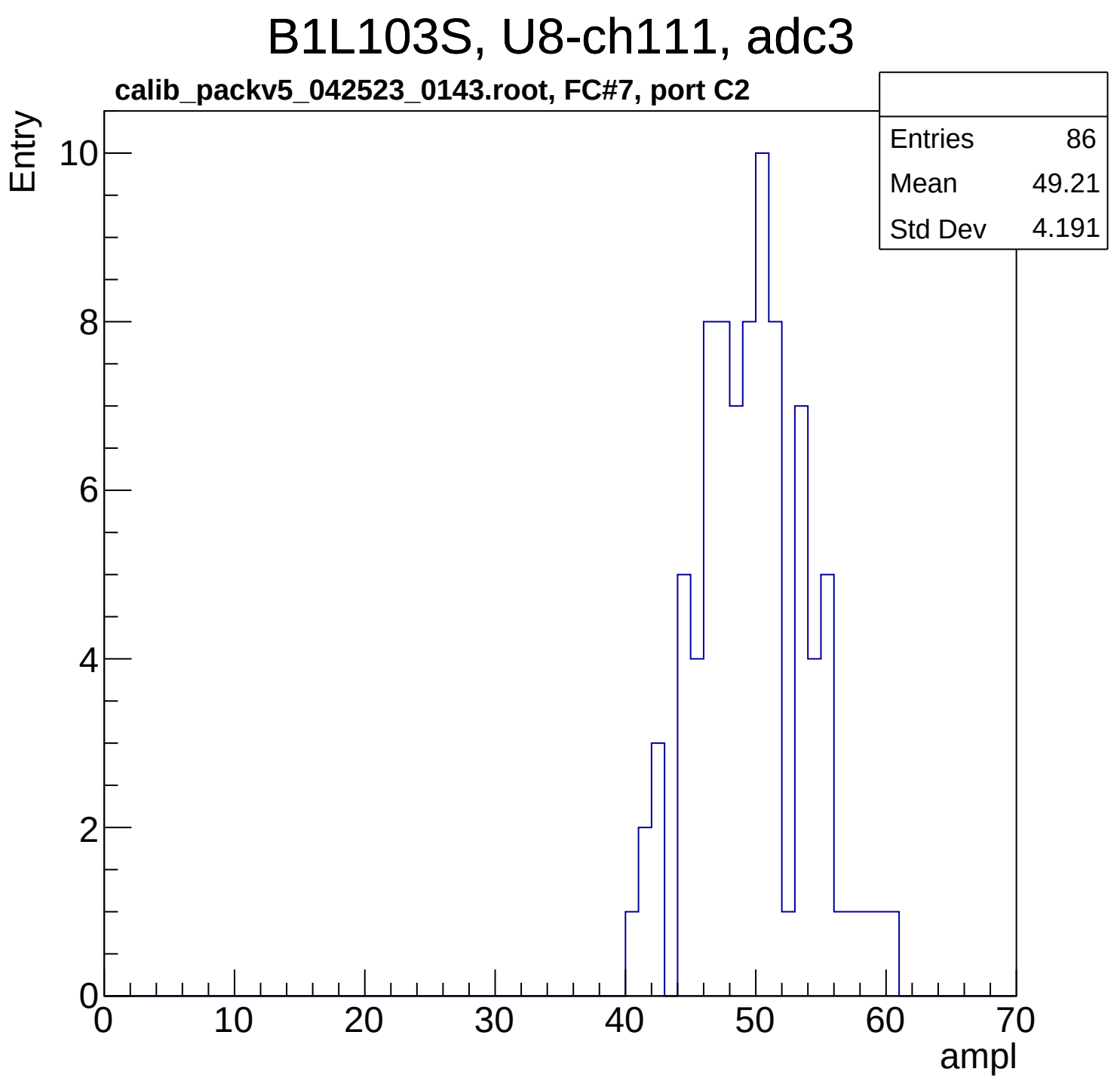

B1L103S, U8-ch110, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 7
Mean 61.86
Std Dev 1.355
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

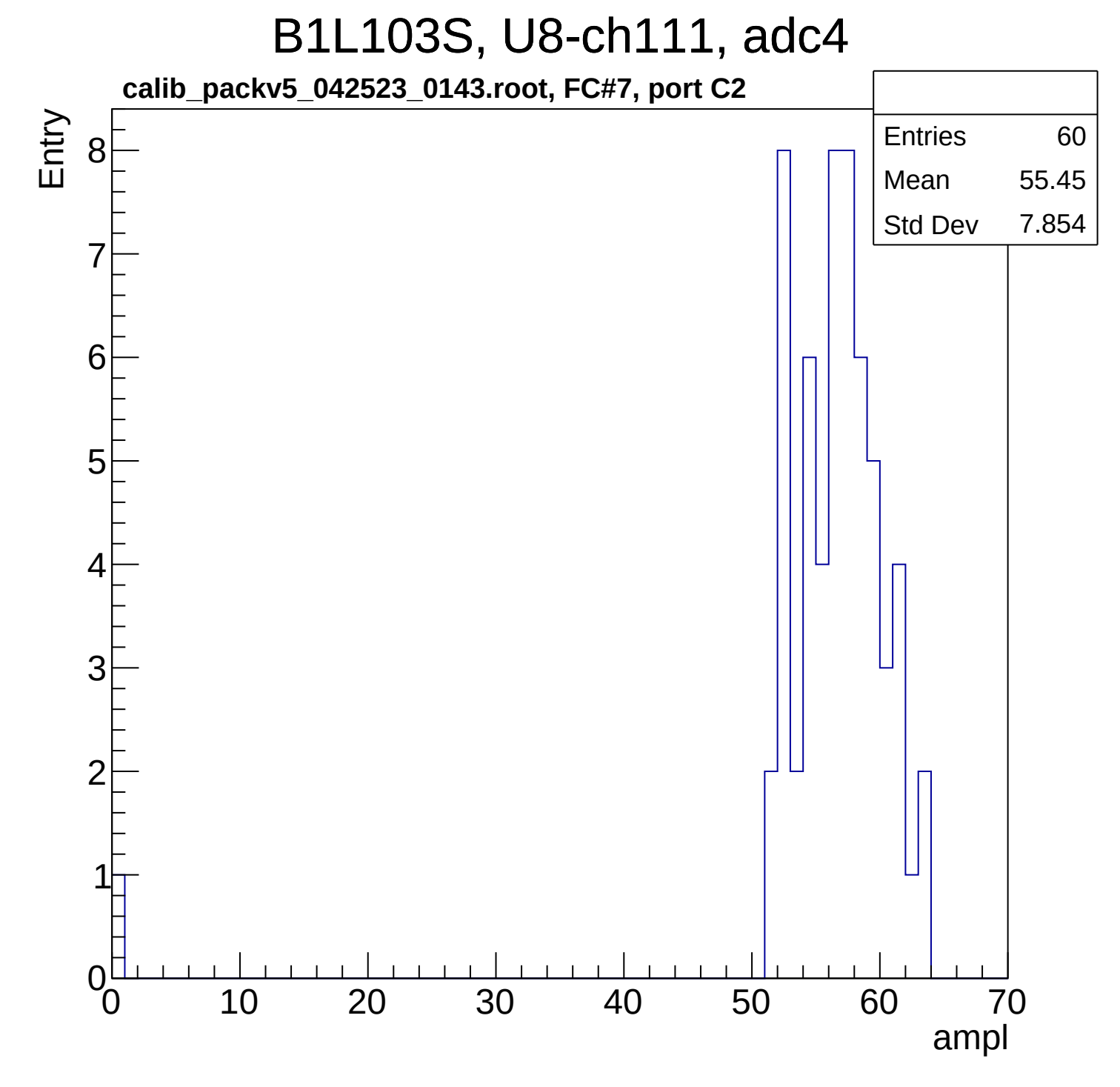

B1L103S, U8-ch110, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

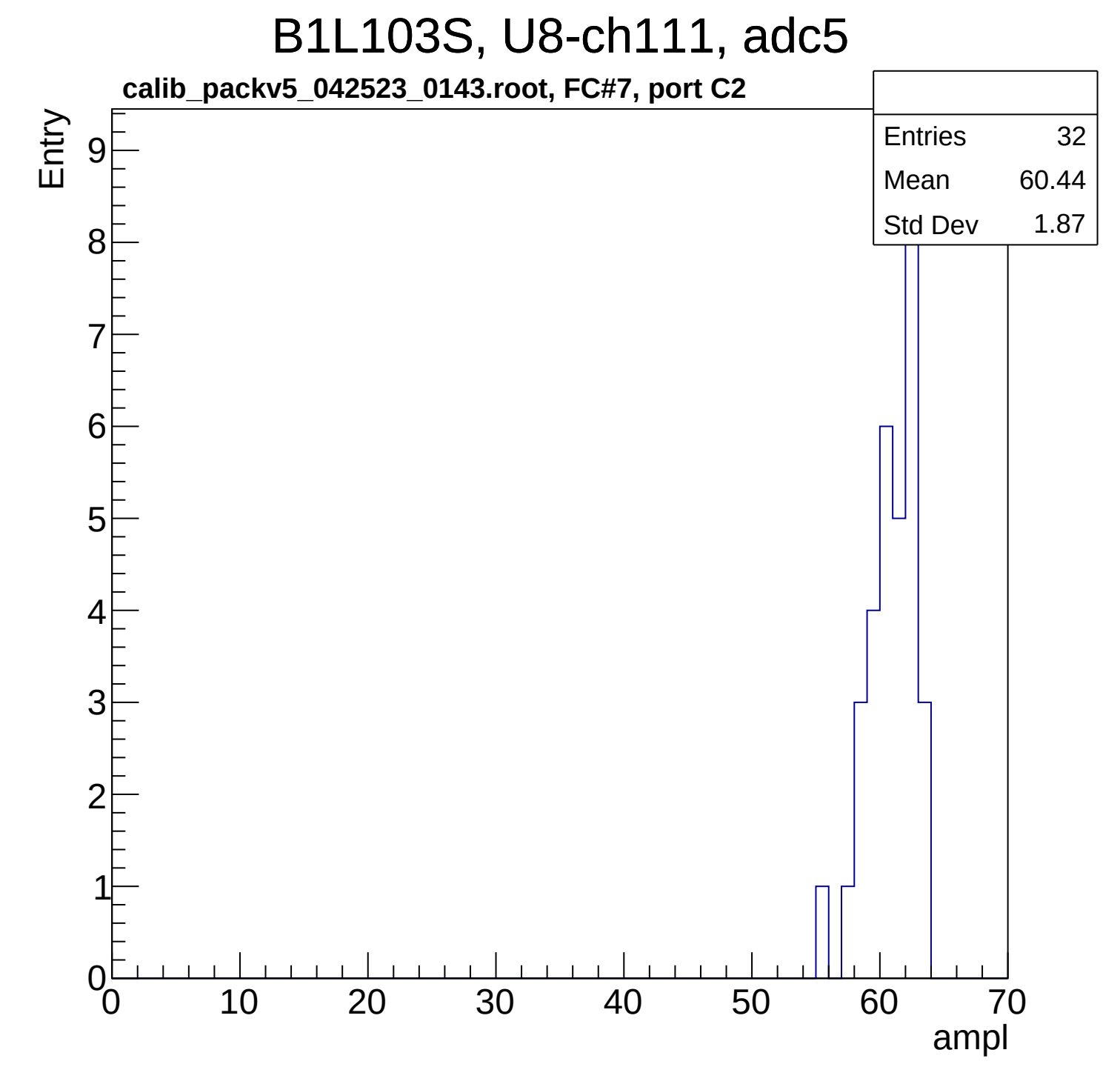

B1L103S, U8-ch111, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 29.49
Std Dev 5.197
Gaus mean : 30.2509
Gaus Width: 3.6451
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

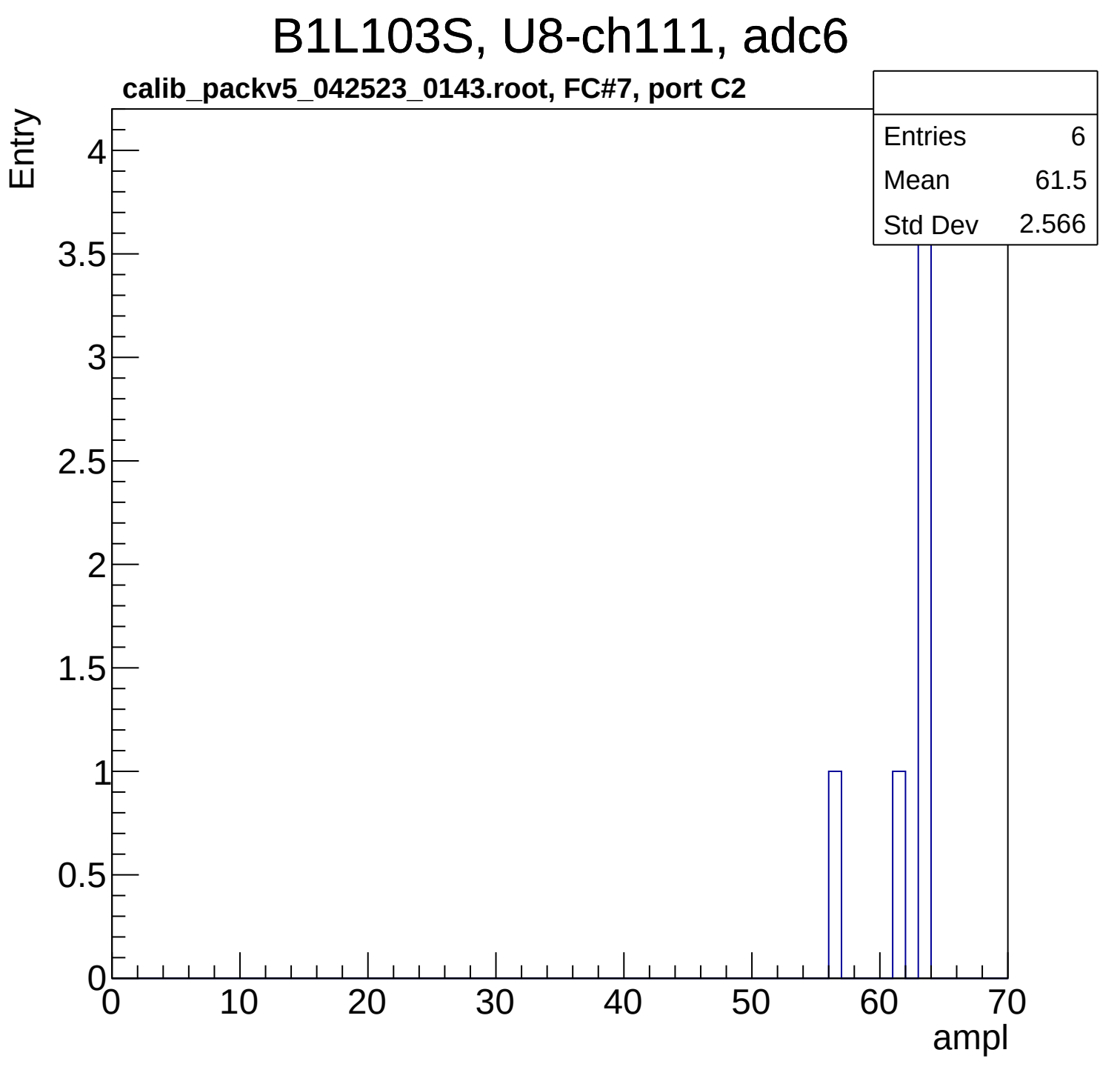

B1L103S, U8-ch111, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 81
Mean 36.96
Std Dev 3.821
Gaus mean : 37.9811
Gaus Width: 3.0707
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

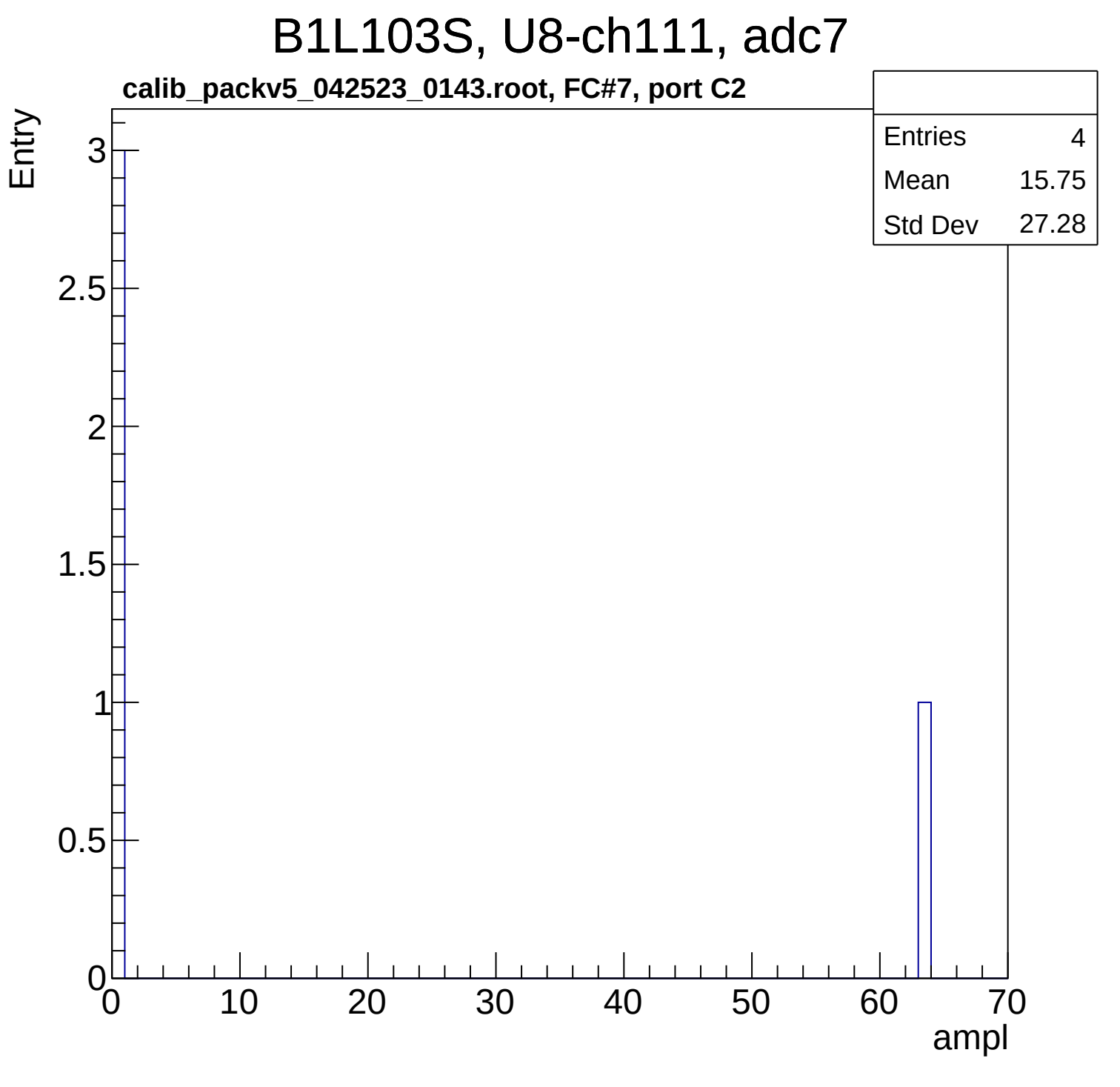

B1L103S, U8-ch111, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 41
Mean 43.46
Std Dev 3.755
Gaus mean : 43.1964
Gaus Width: 2.8847
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

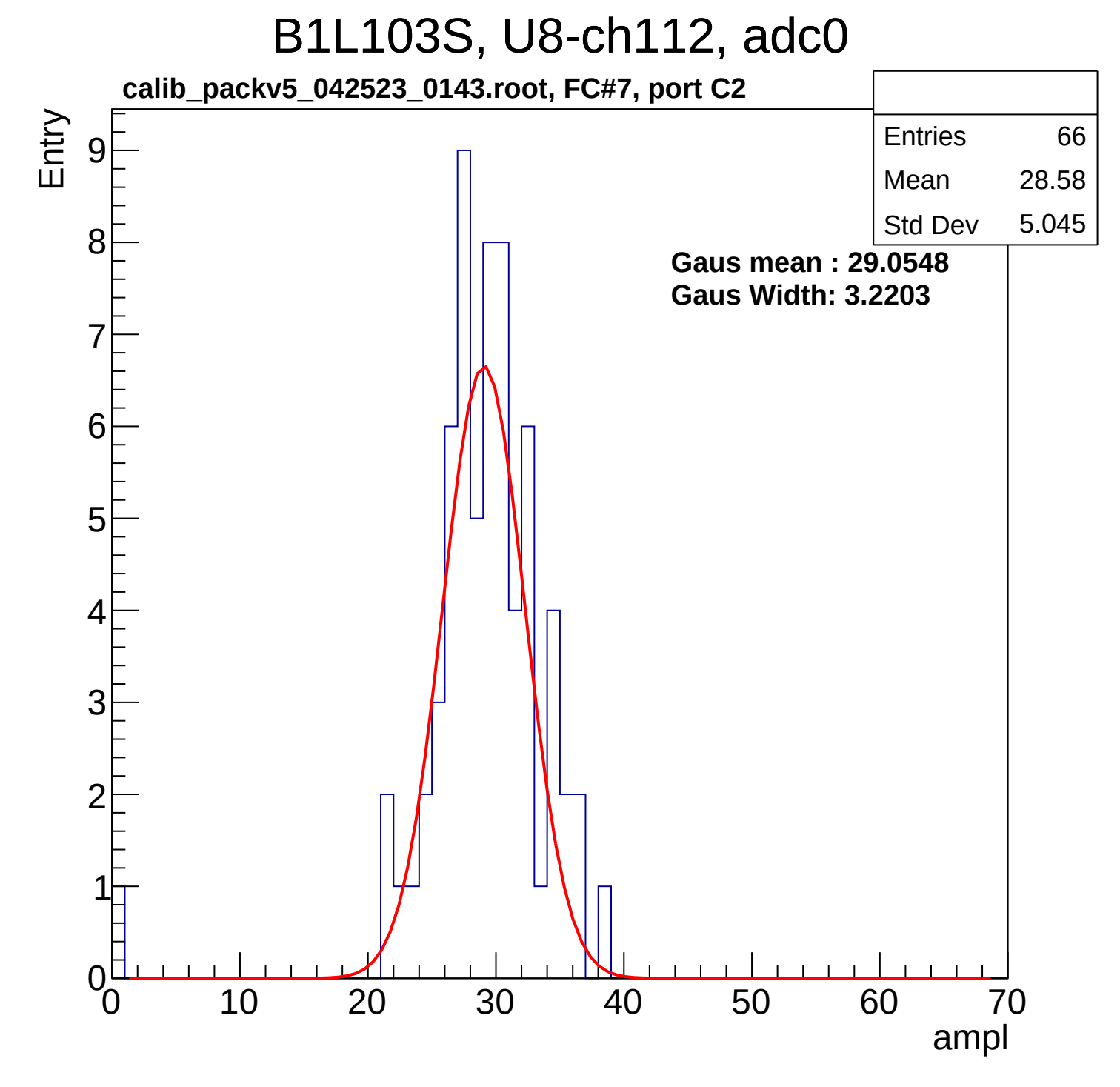

B1L103S, U8-ch111, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 86
Mean 49.21
Std Dev 4.191
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

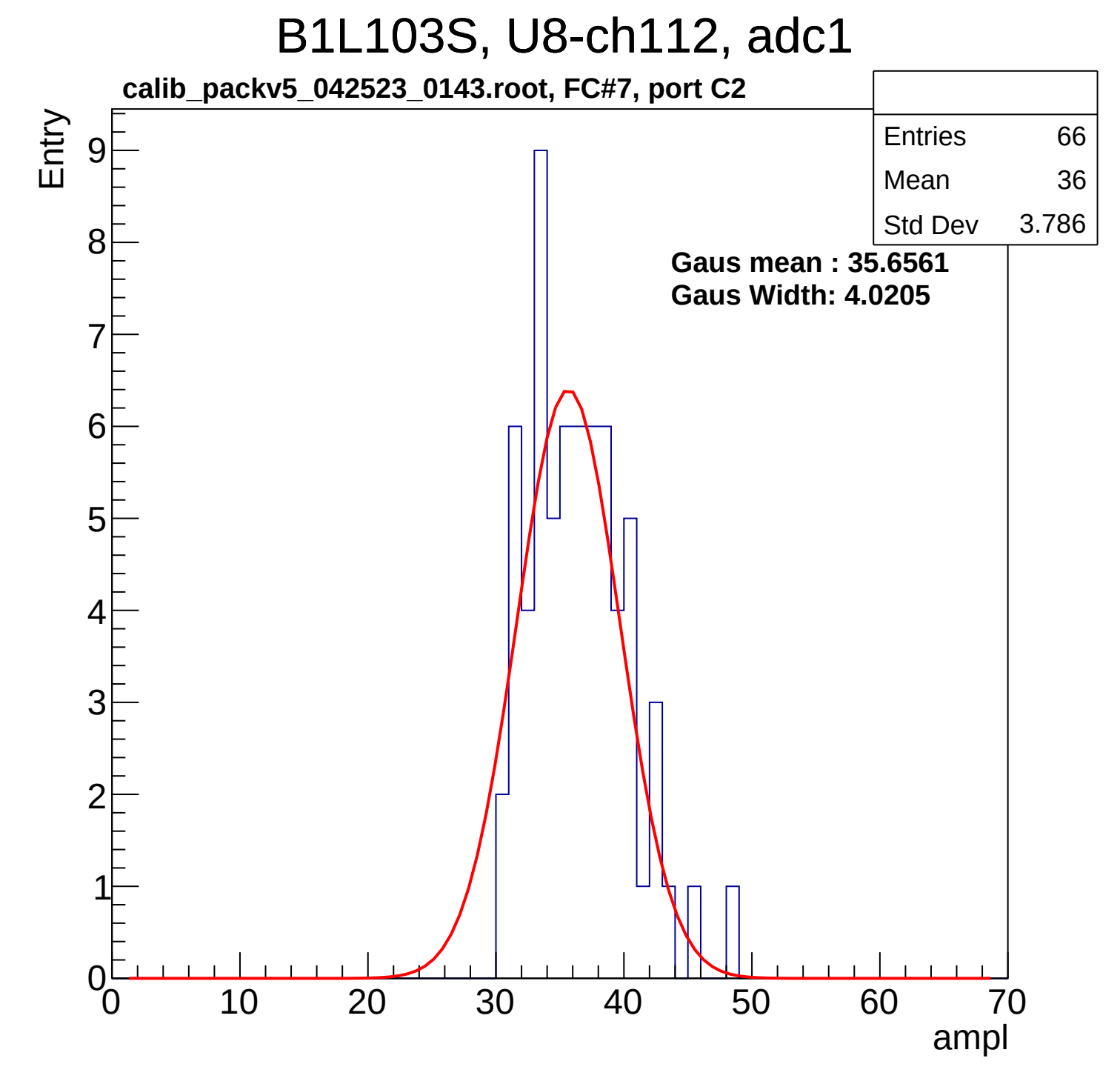

B1L103S, U8-ch111, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 55.45
Std Dev 7.854
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

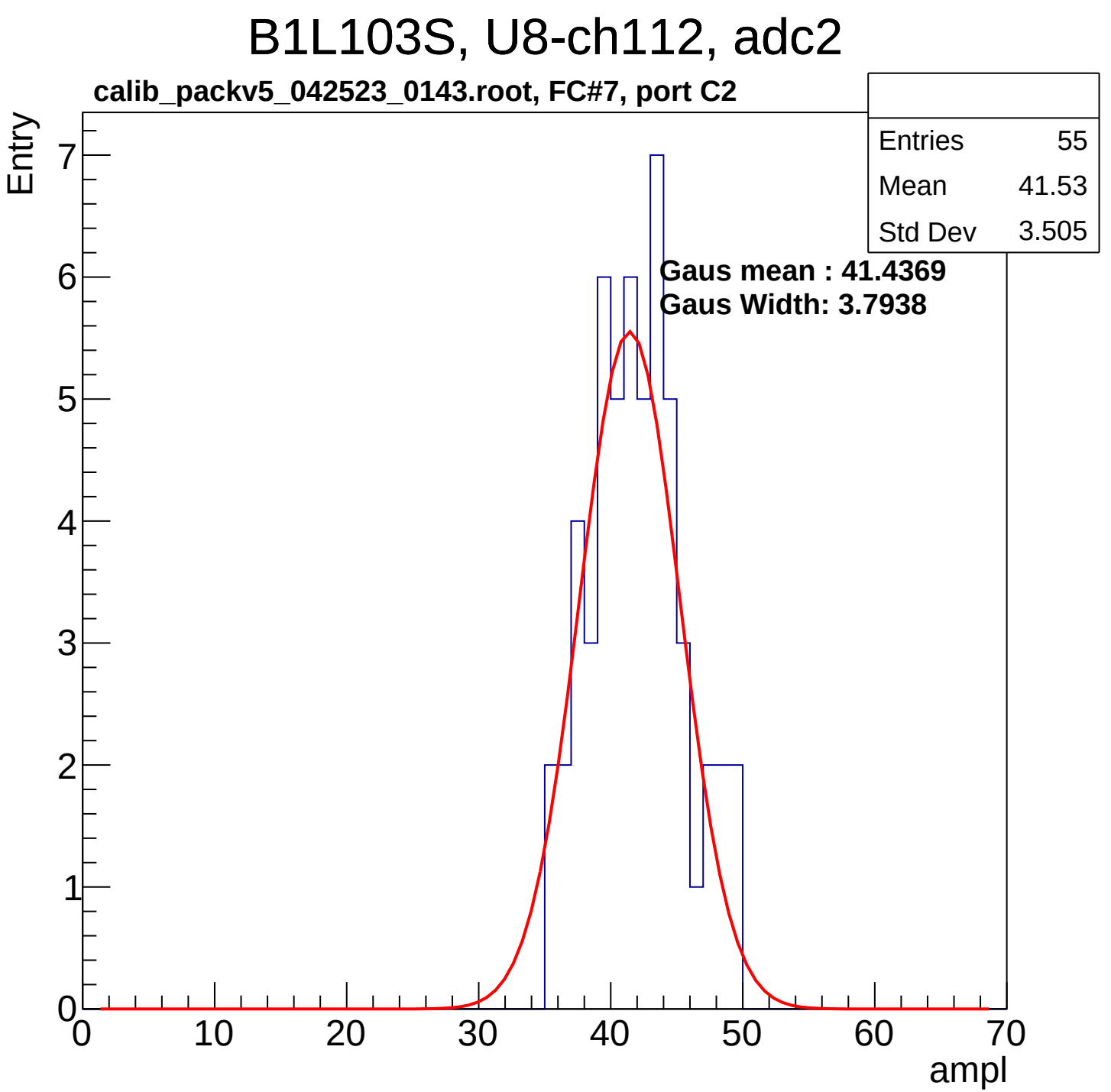

B1L103S, U8-ch111, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 32
Mean 60.44
Std Dev 1.87
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

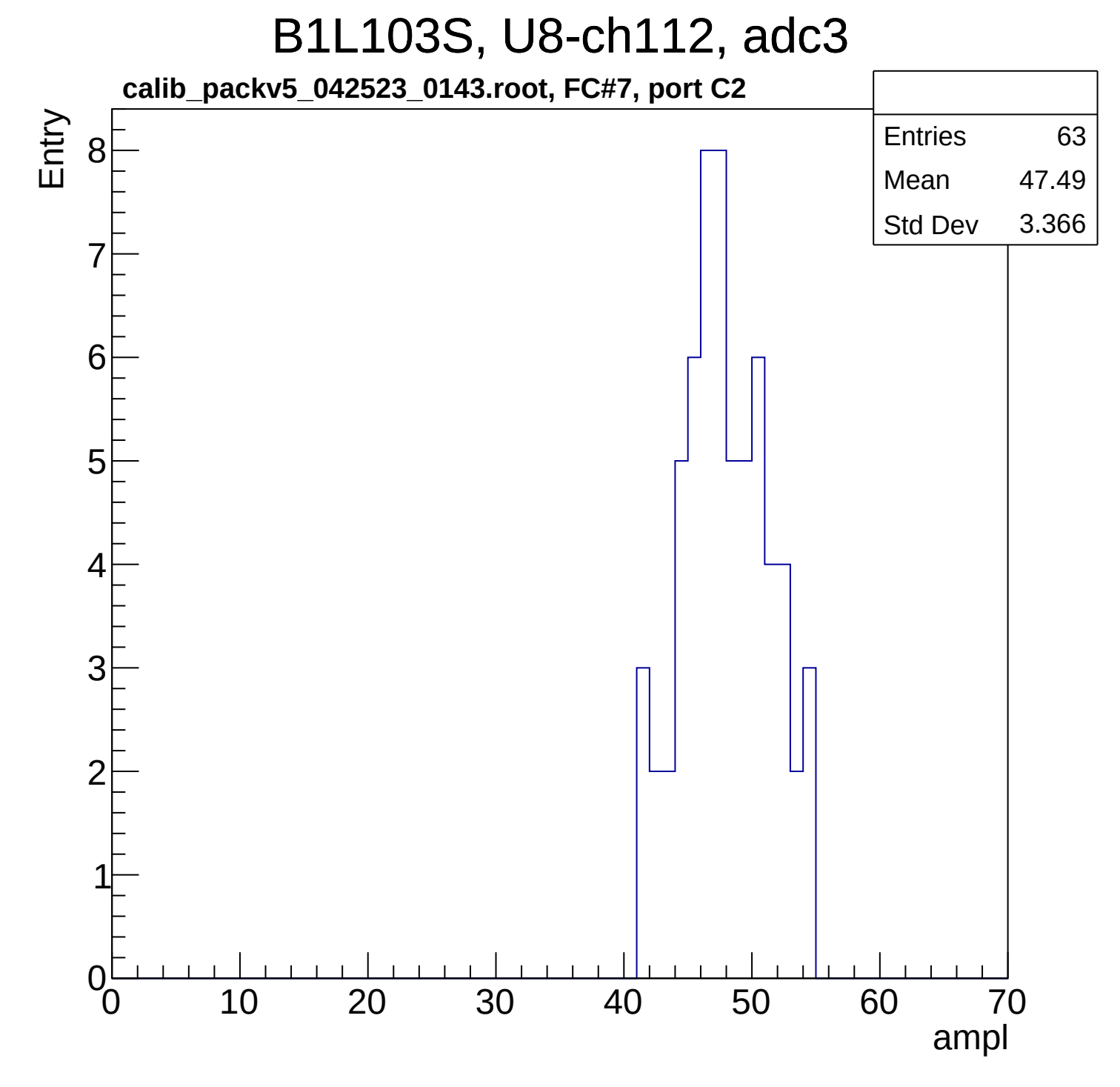

B1L103S, U8-ch111, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 6
Mean 61.5
Std Dev 2.566
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

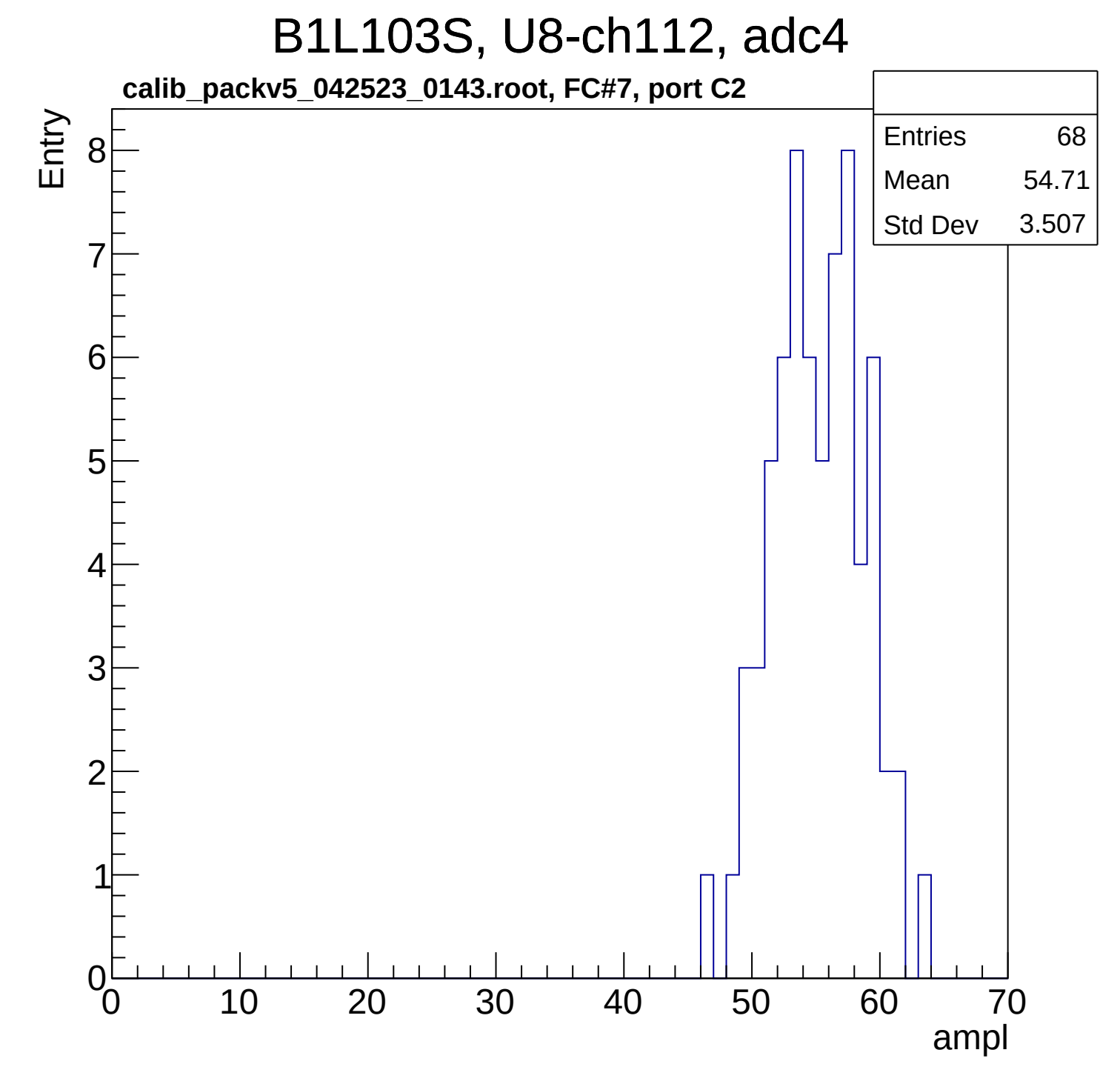

B1L103S, U8-ch111, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 15.75
Std Dev 27.28
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl

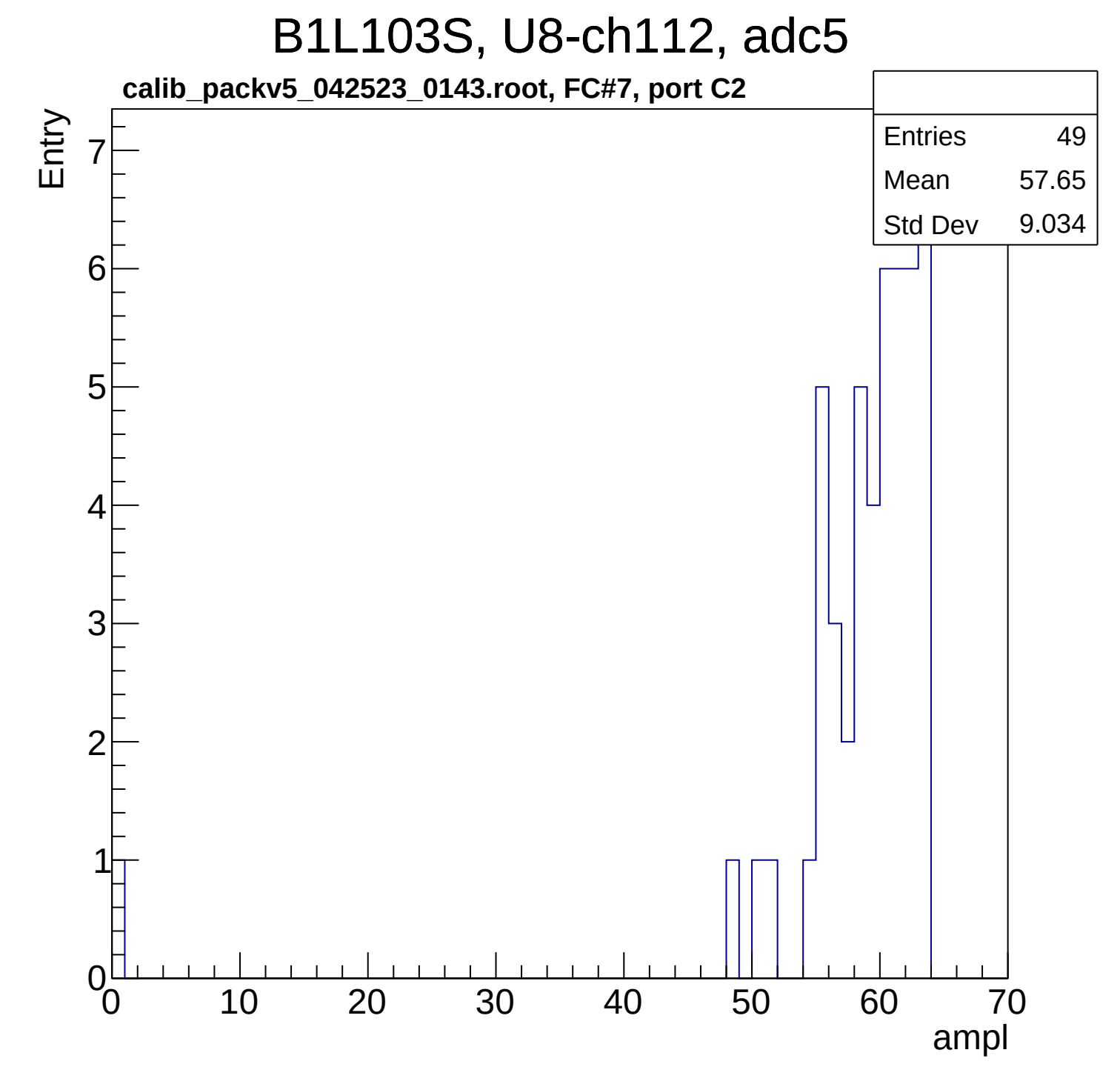

B1L103S, U8-ch112, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 28.58
Std Dev 5.045
Gaus mean : 29.0548
Gaus Width: 3.2203
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

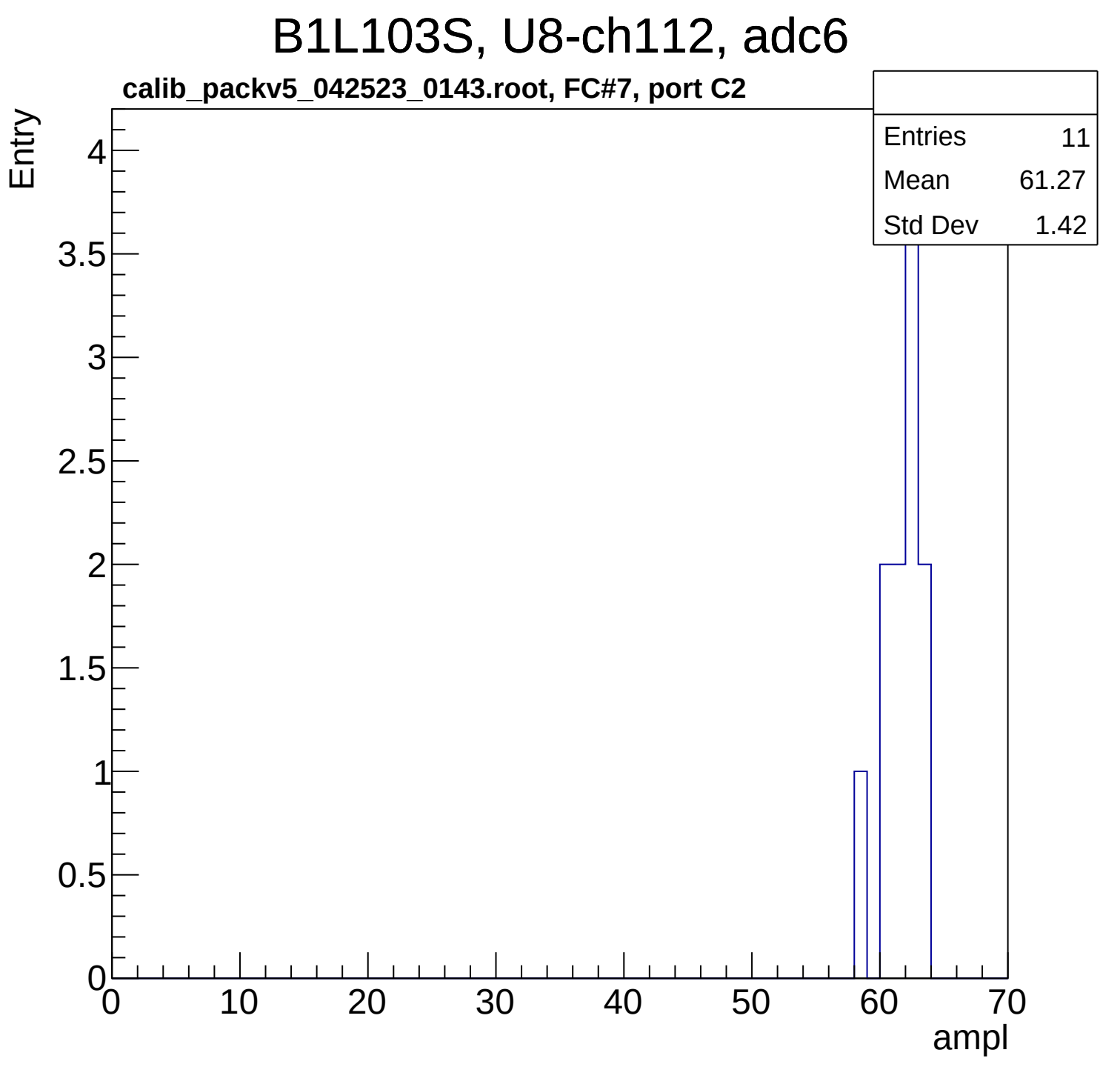

B1L103S, U8-ch112, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 36
Std Dev 3.786
Gaus mean : 35.6561
Gaus Width: 4.0205
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

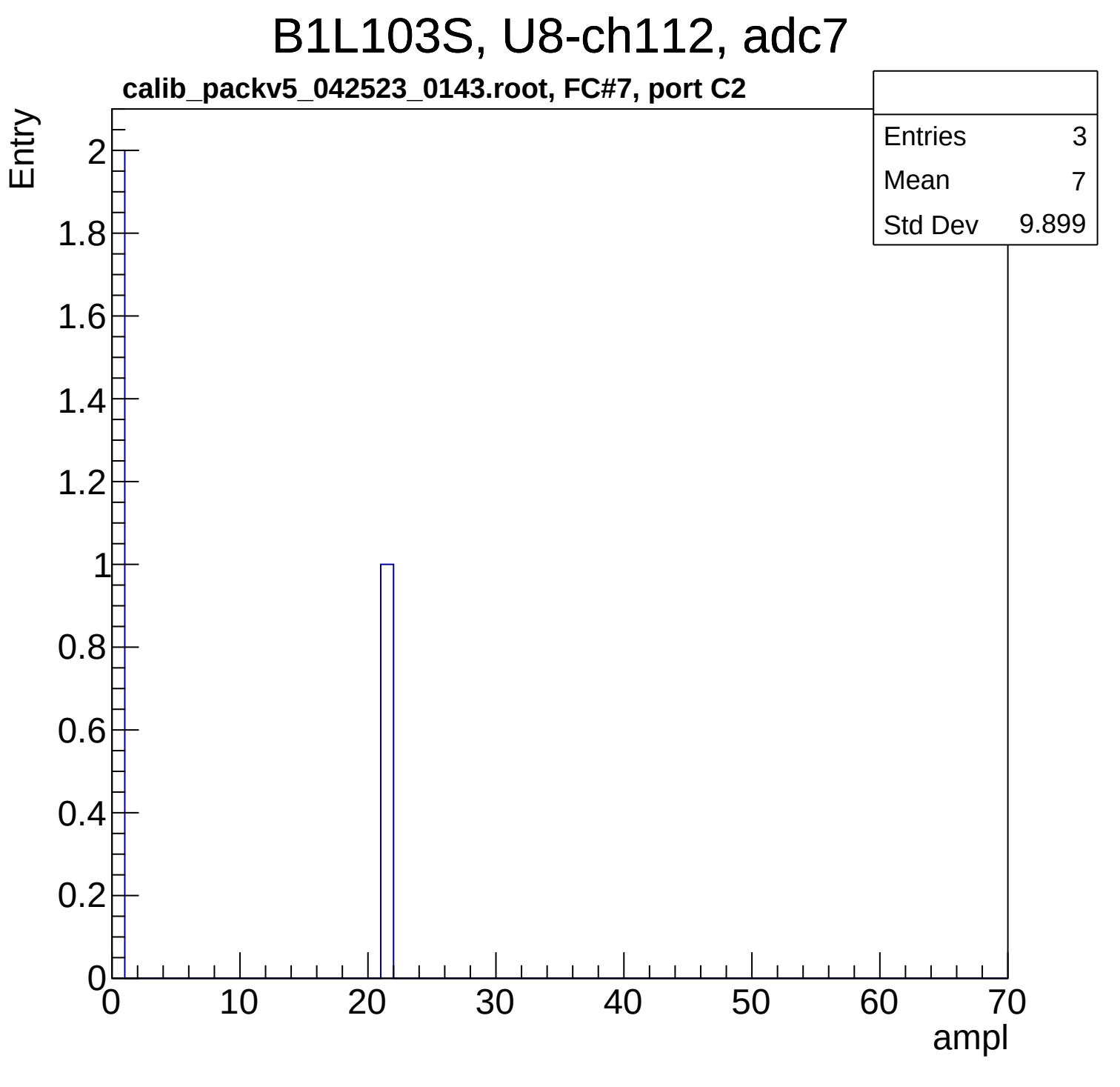

B1L103S, U8-ch112, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 55
Mean 41.53
Std Dev 3.505
Gaus mean : 41.4369
Gaus Width: 3.7938
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

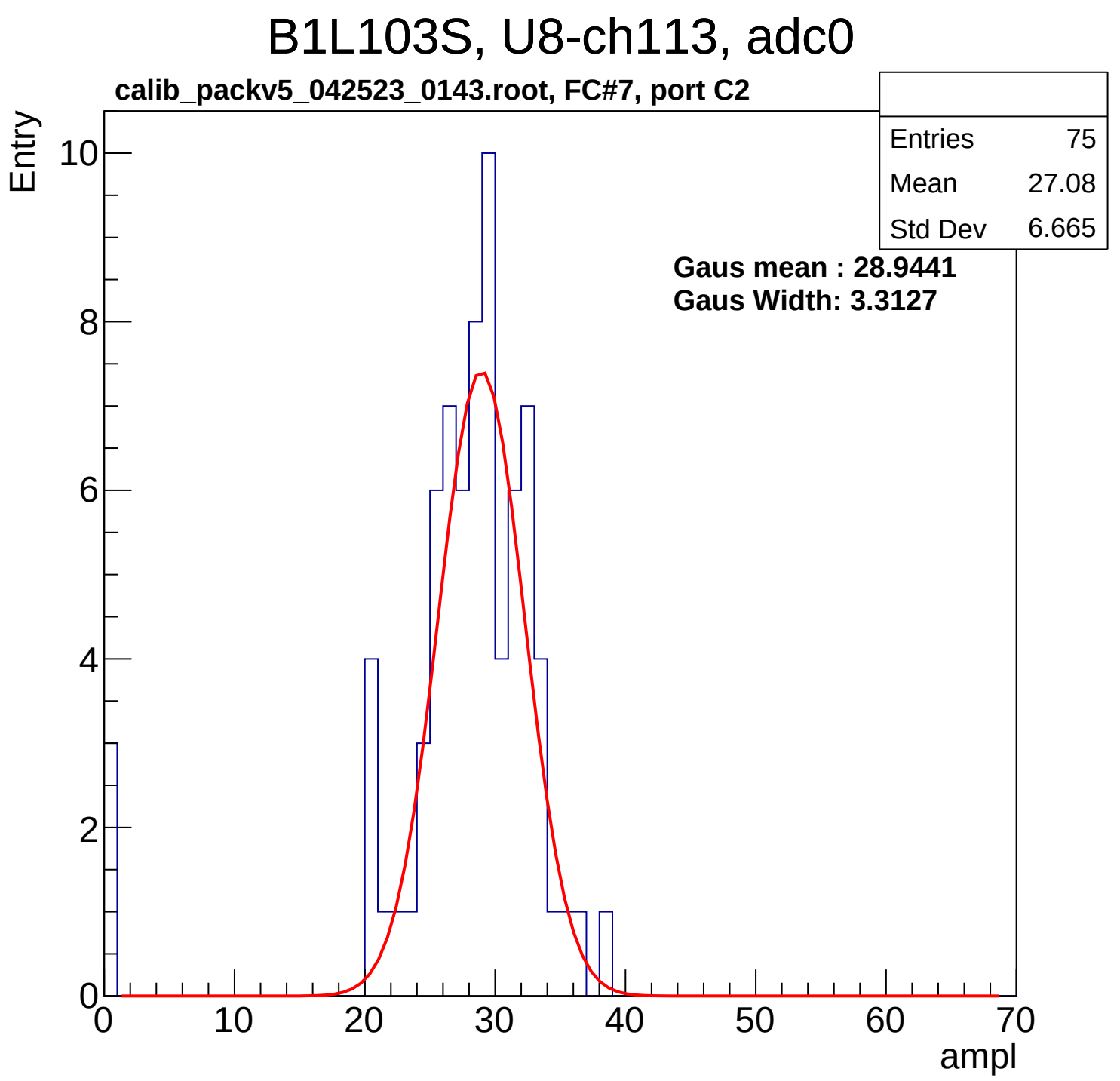

B1L103S, U8-ch112, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 47.49
Std Dev 3.366
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

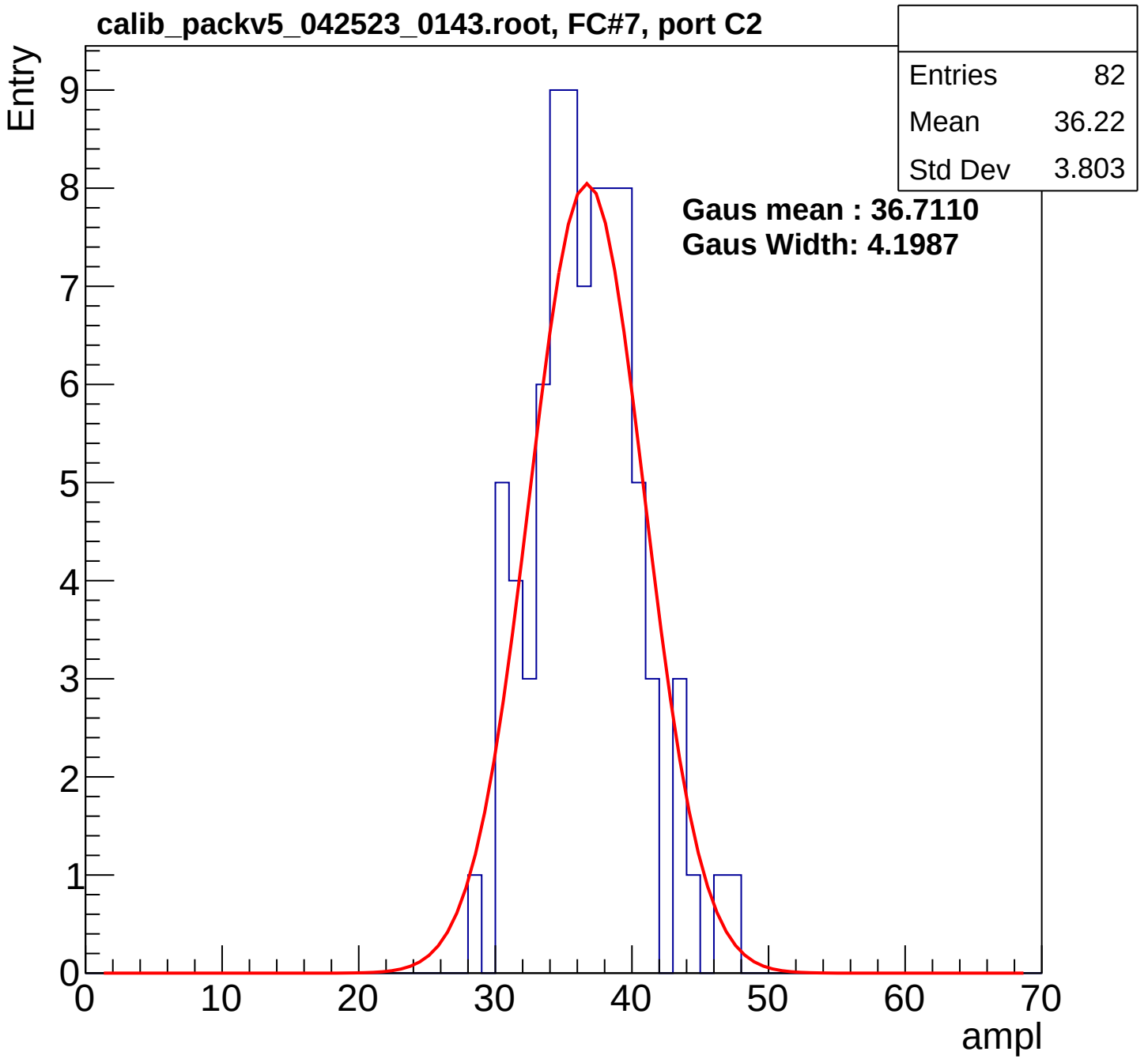

B1L103S, U8-ch112, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 54.71
Std Dev 3.507
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

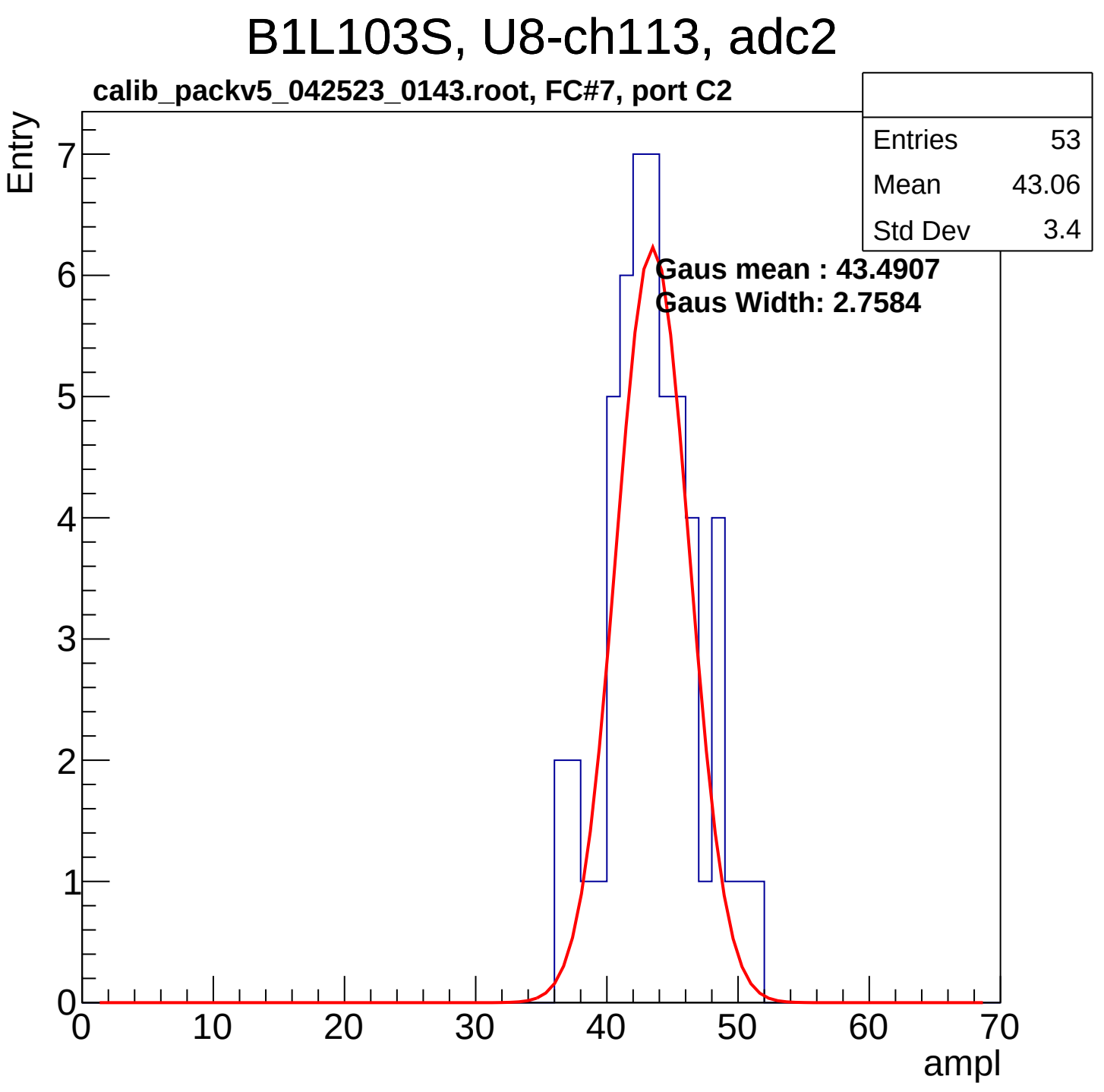

B1L103S, U8-ch112, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 57.65
Std Dev 9.034
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

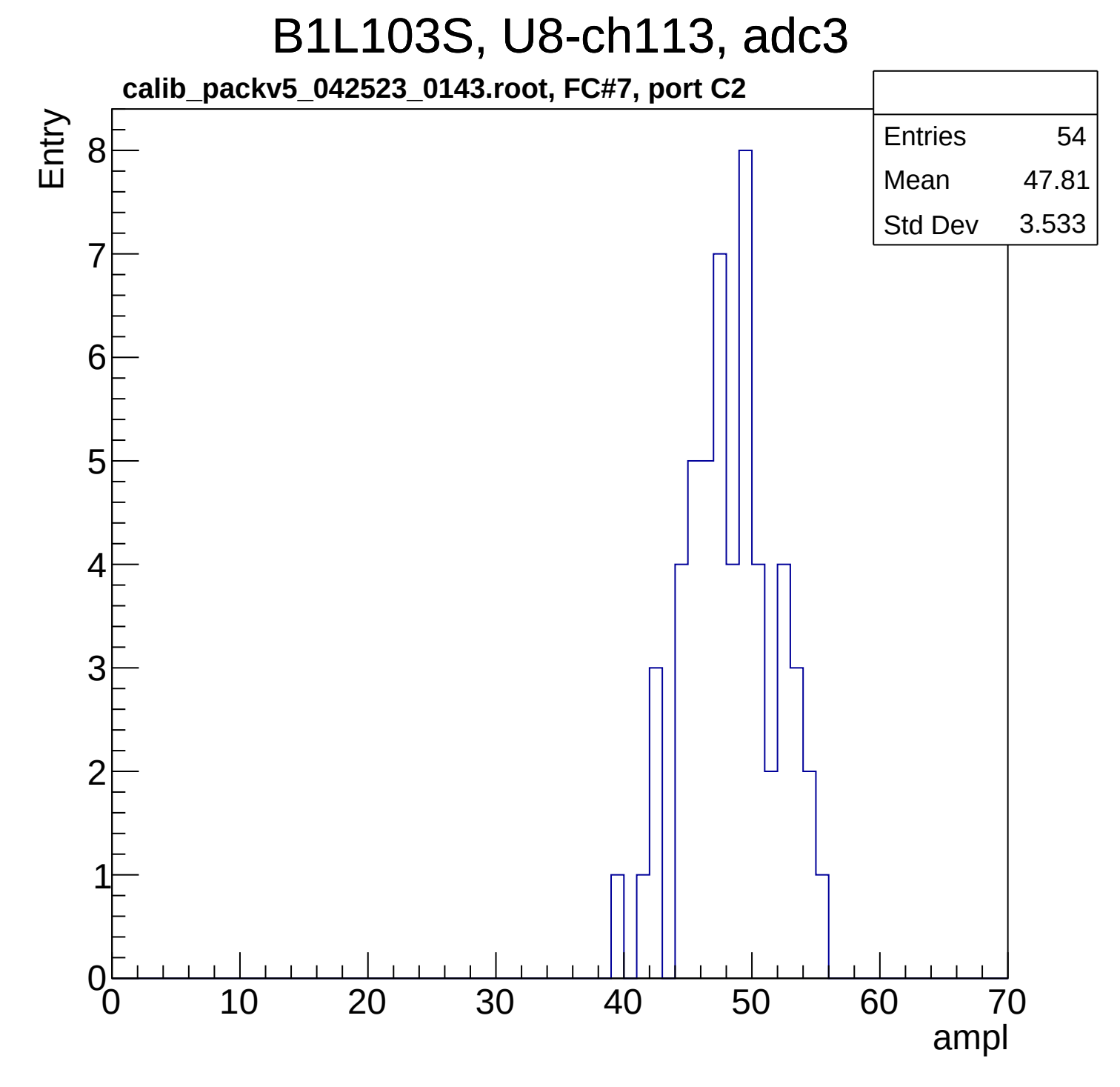

B1L103S, U8-ch112, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 11
Mean 61.27
Std Dev 1.42
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

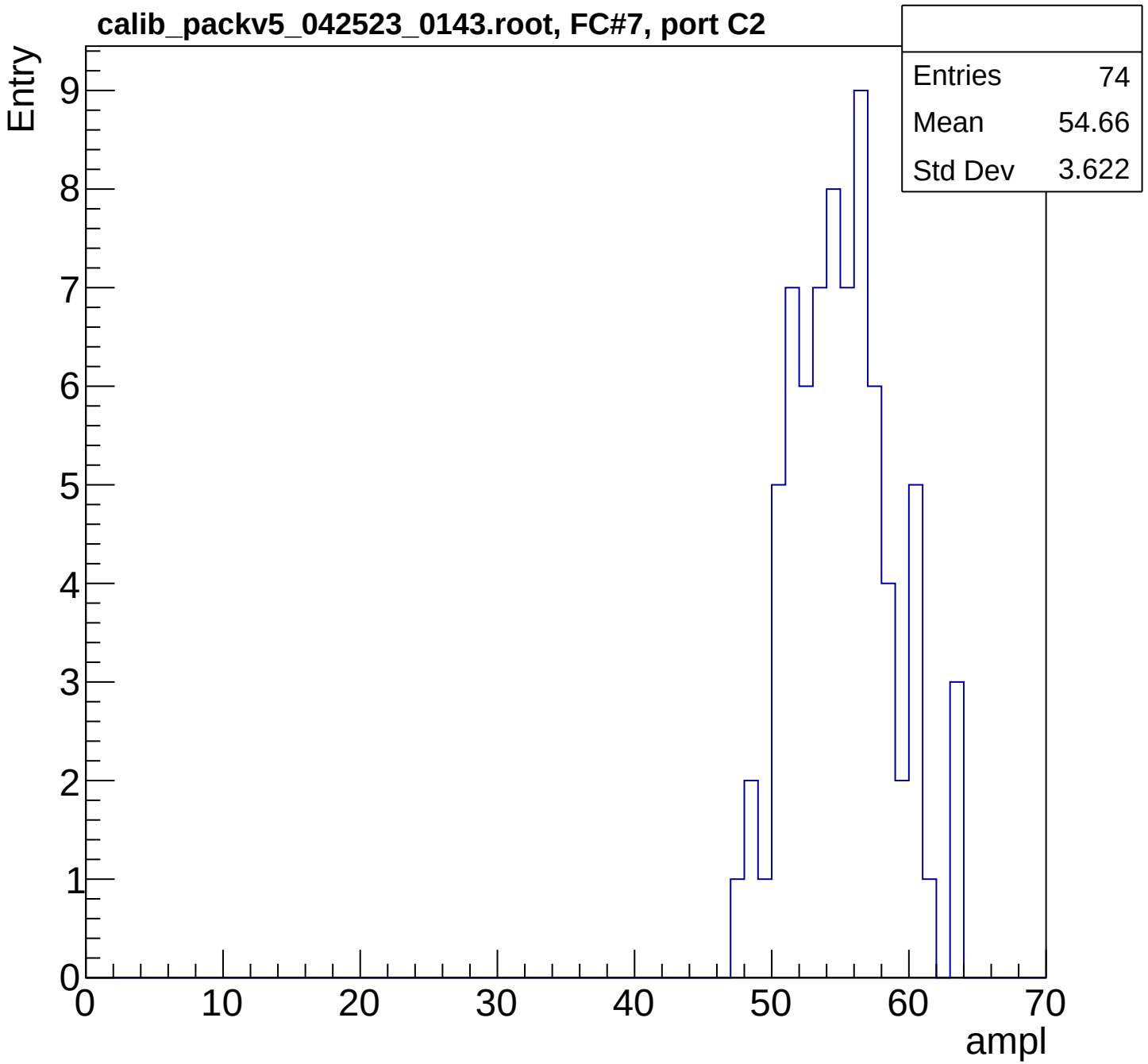

B1L103S, U8-ch112, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 7
Std Dev 9.899
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

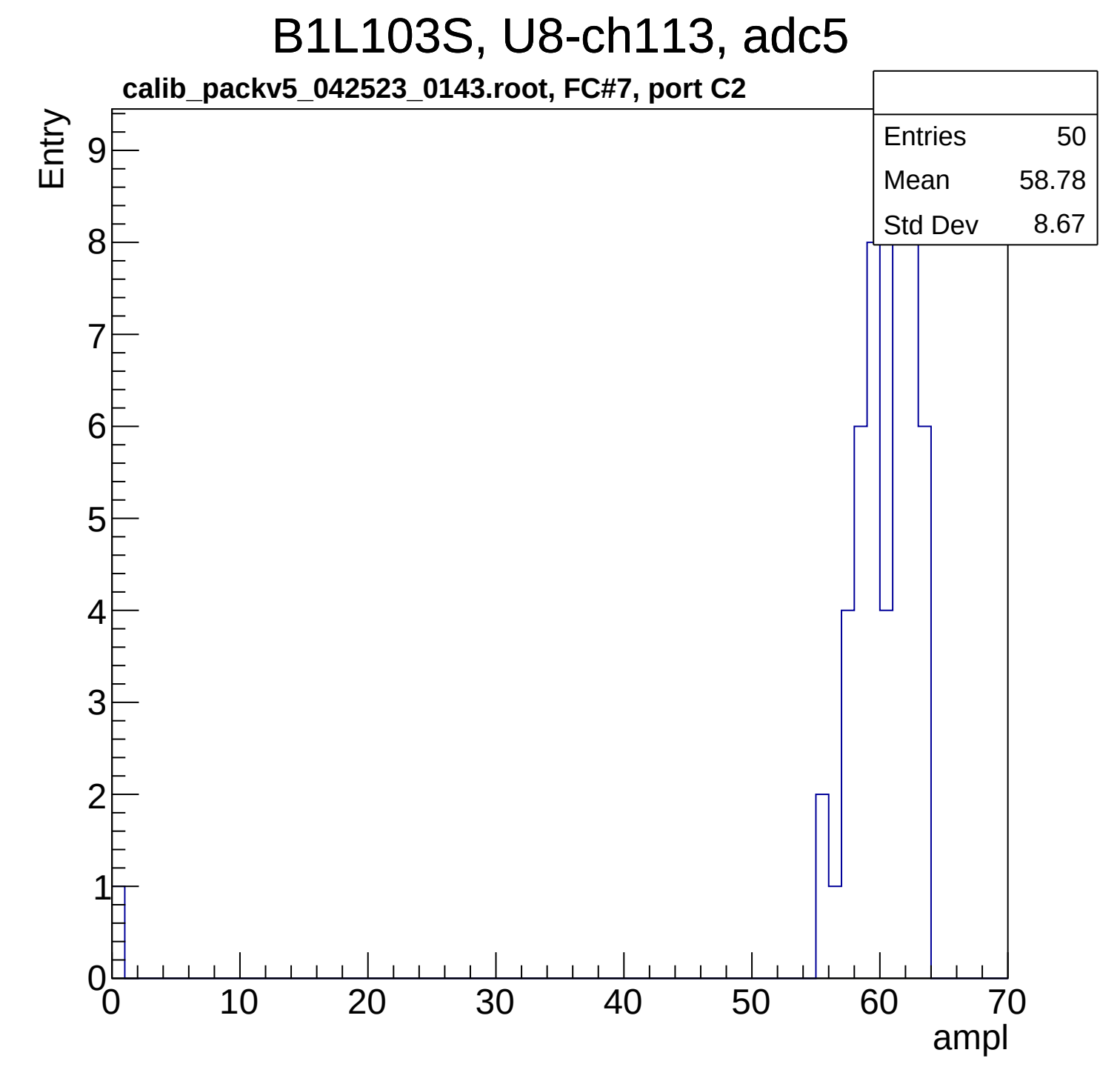

B1L103S, U8-ch113, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 27.08
Std Dev 6.665
Gaus mean : 28.9441
Gaus Width: 3.3127
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

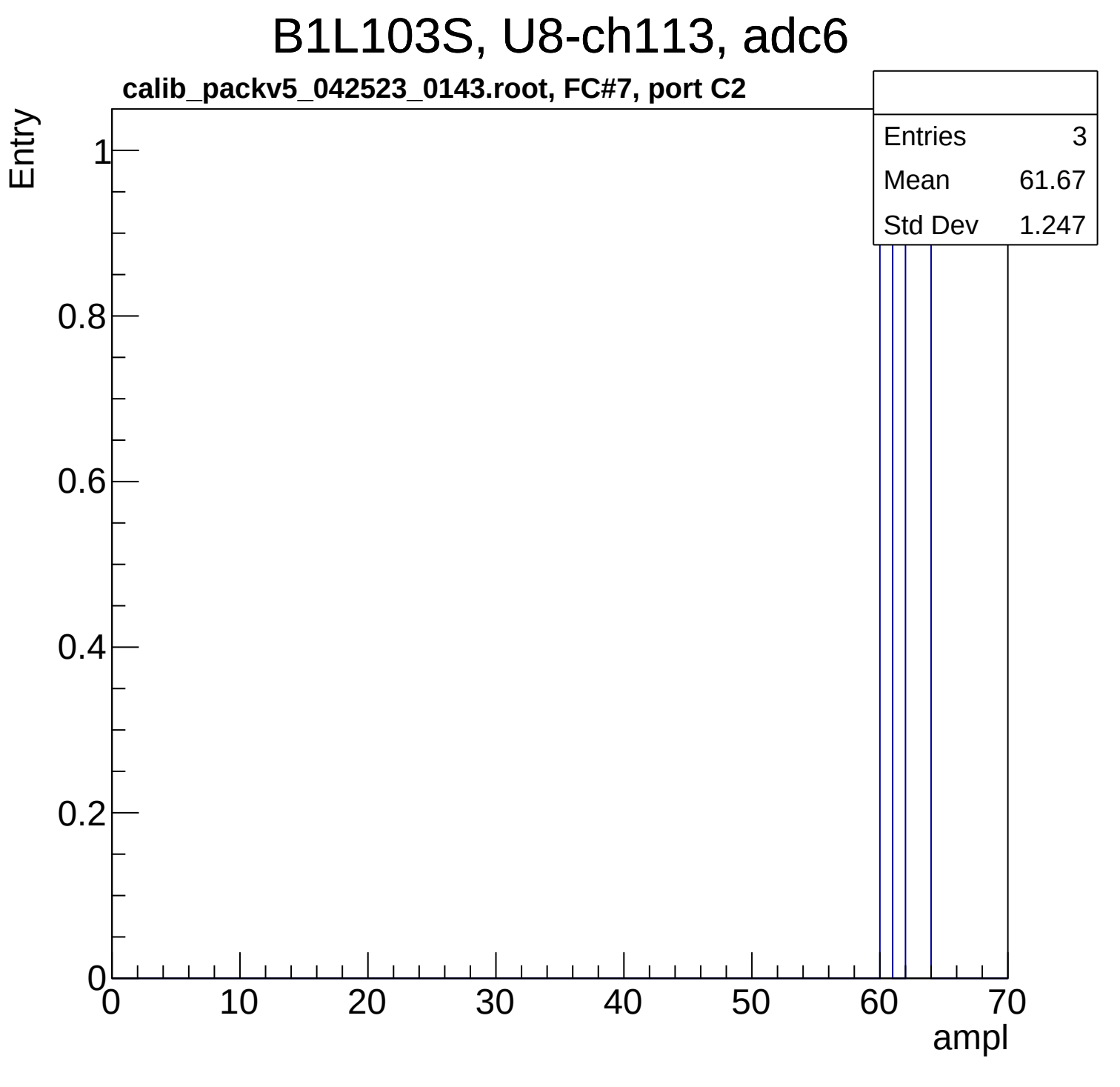

B1L103S, U8-ch113, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 82
Mean 36.22
Std Dev 3.803
Gaus mean : 36.7110
Gaus Width: 4.1987
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

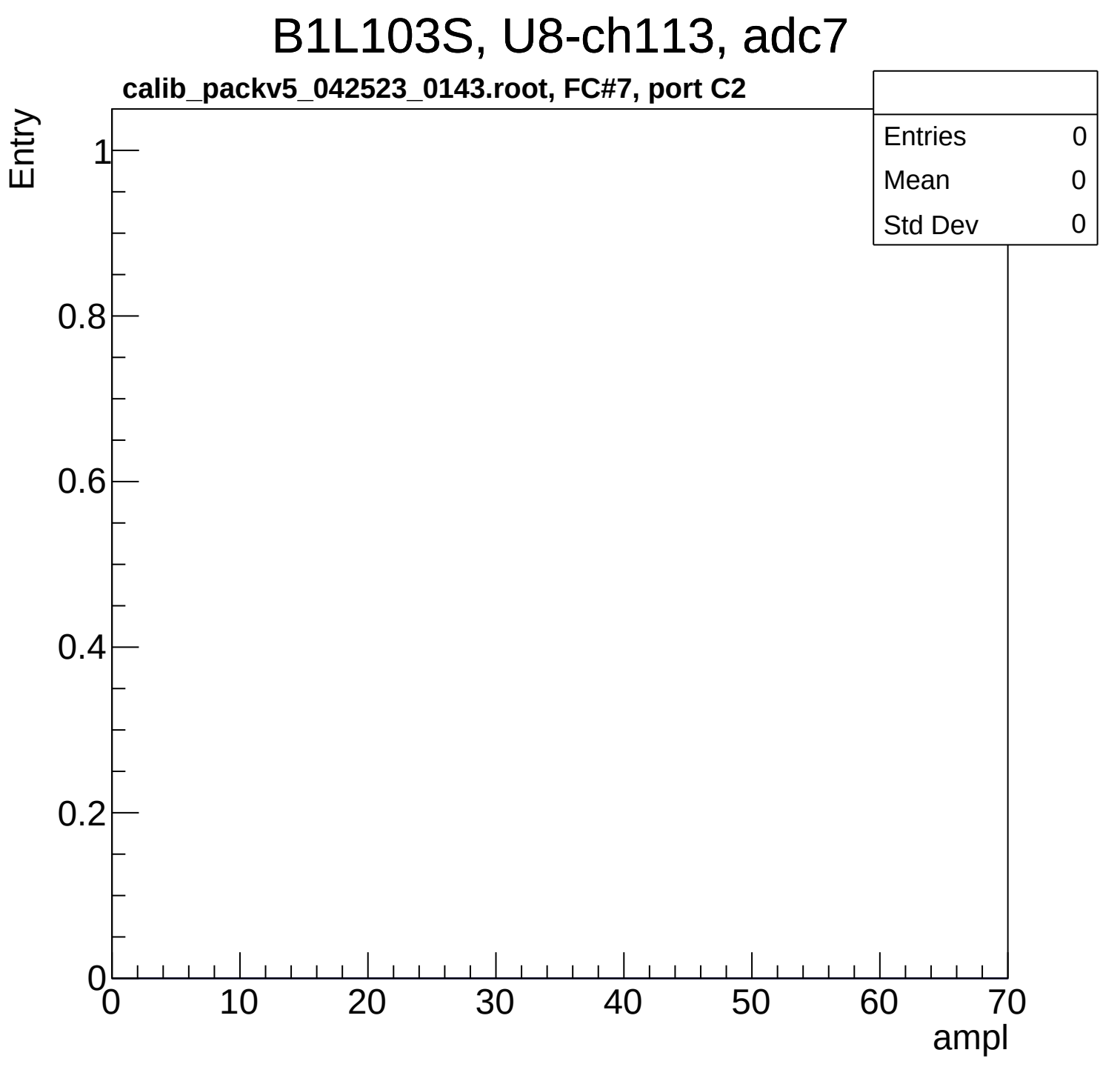

B1L103S, U8-ch113, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 43.06
Std Dev 3.4
Gaus mean : 43.4907
Gaus Width: 2.7584
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

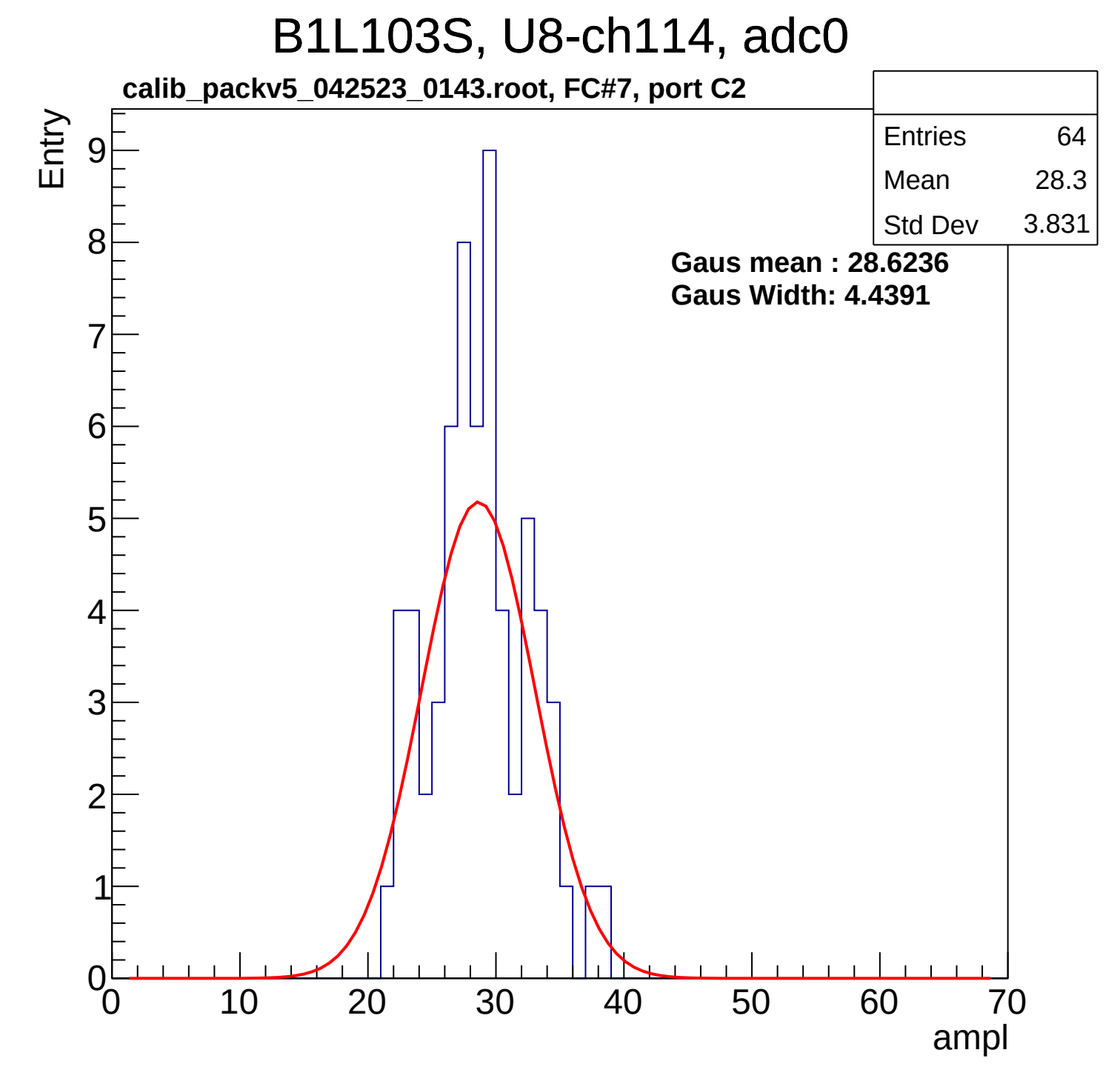

B1L103S, U8-ch113, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 47.81
Std Dev 3.533
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

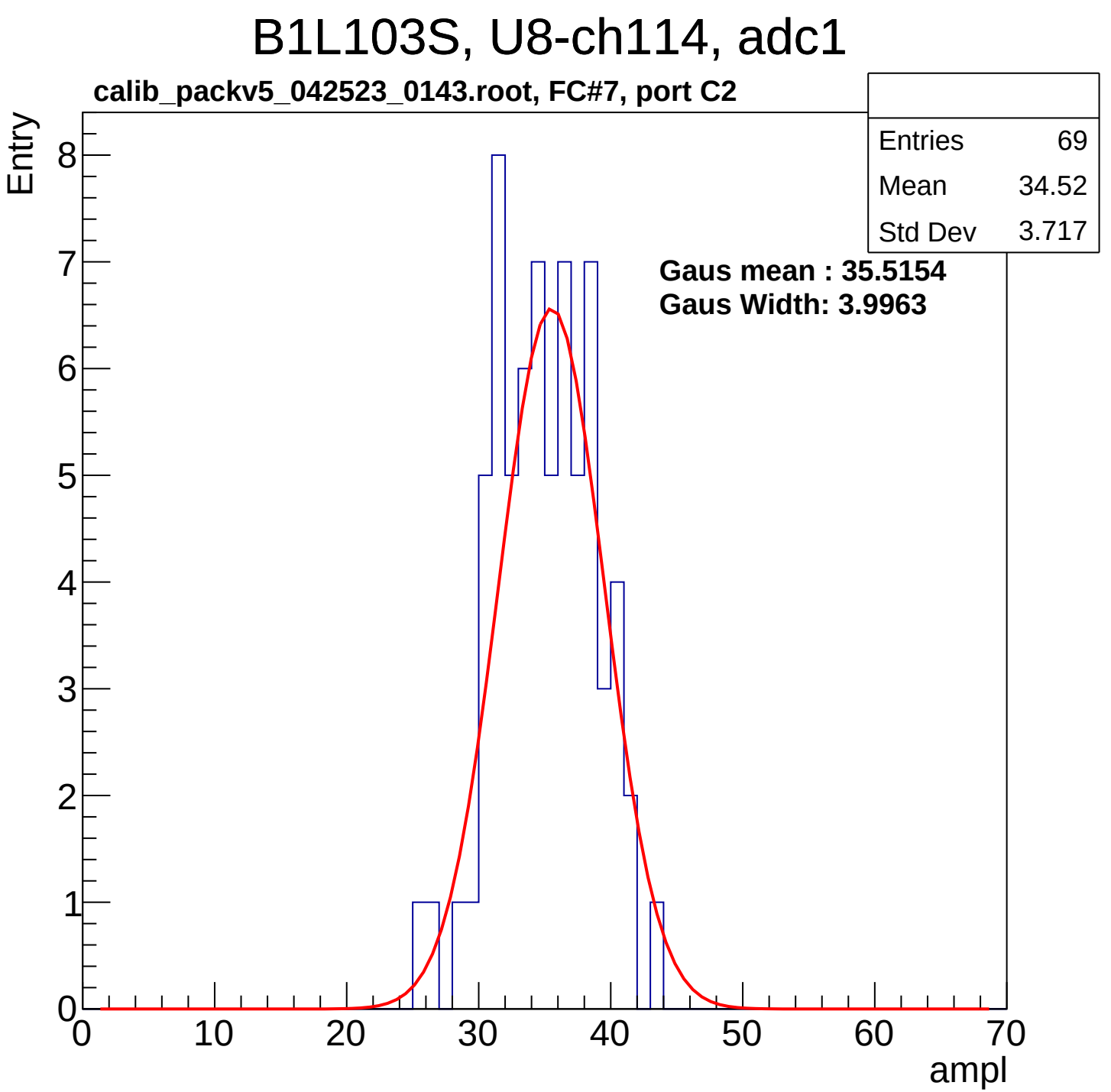

B1L103S, U8-ch113, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 54.66
Std Dev 3.622
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

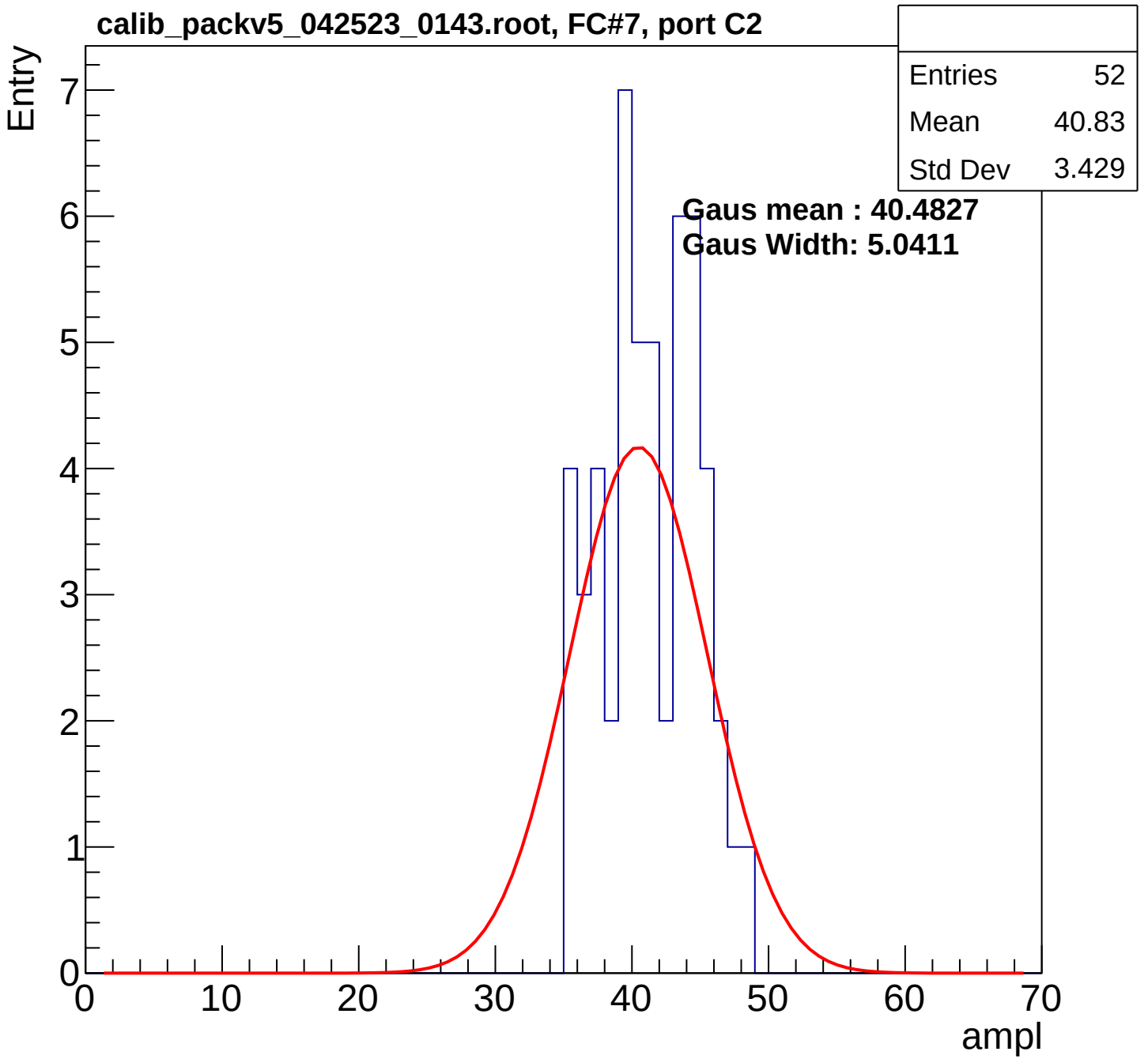

B1L103S, U8-ch113, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 58.78
Std Dev 8.67
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

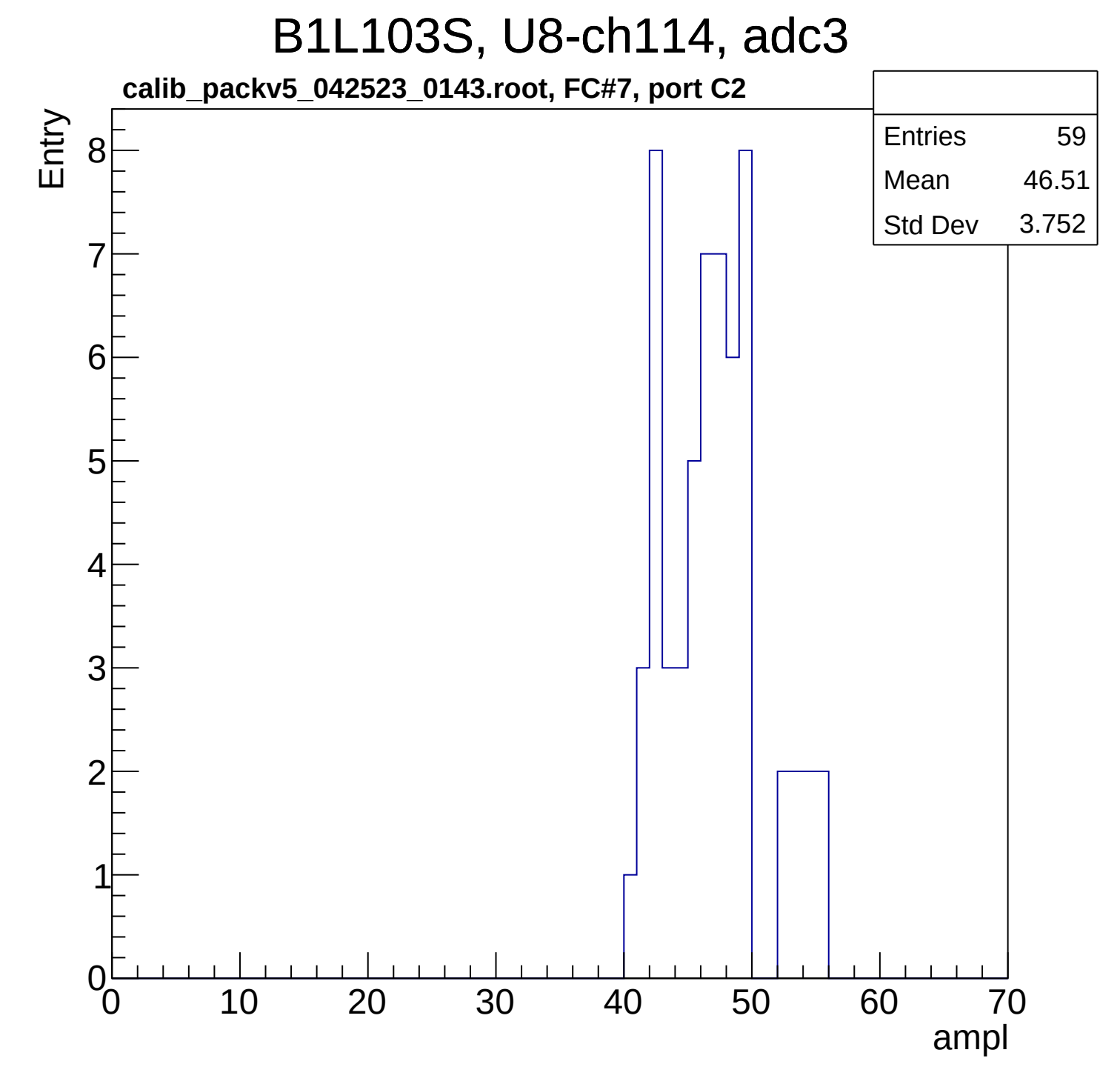

B1L103S, U8-ch113, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 61.67
Std Dev 1.247
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

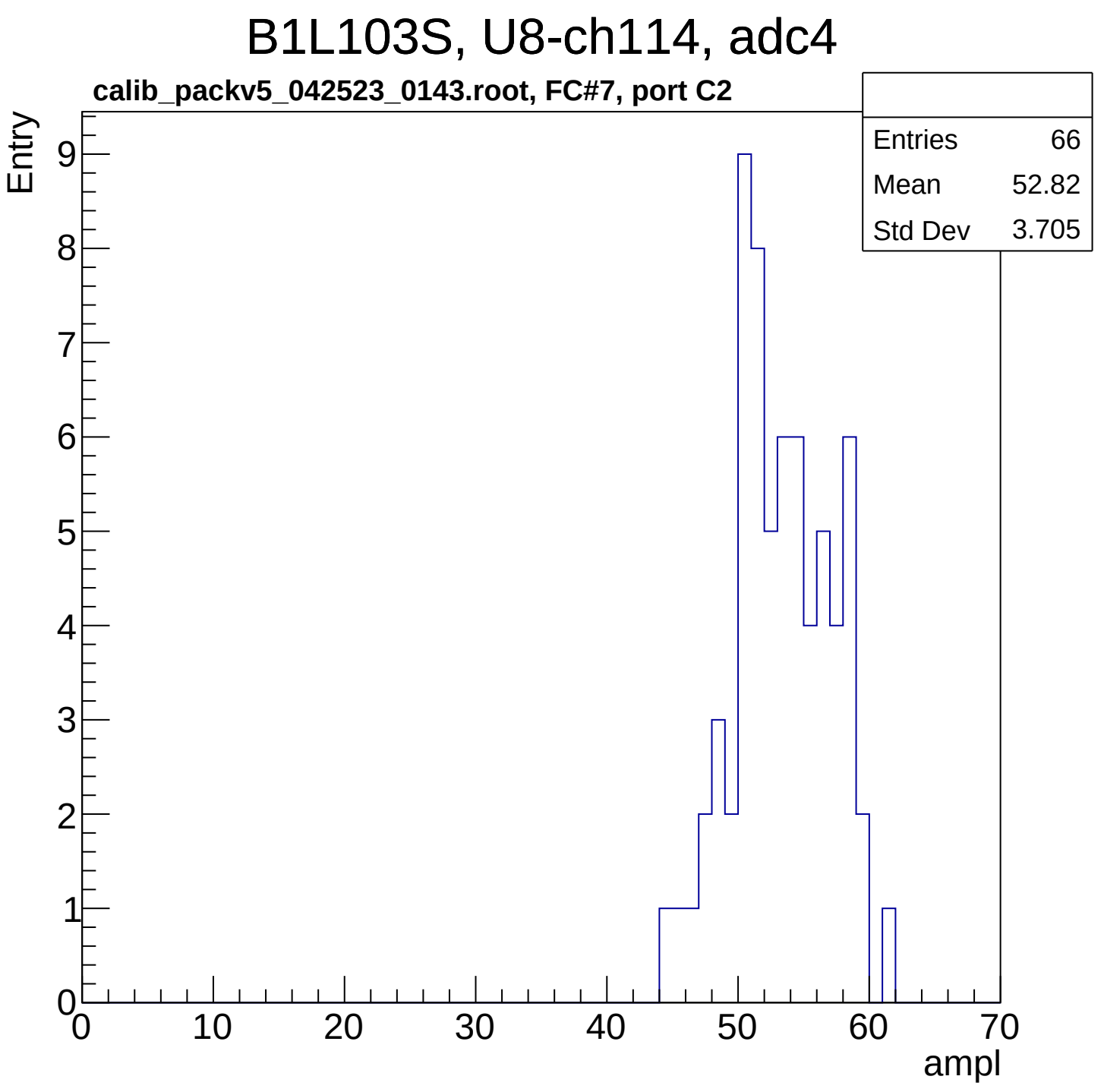

B1L103S, U8-ch113, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

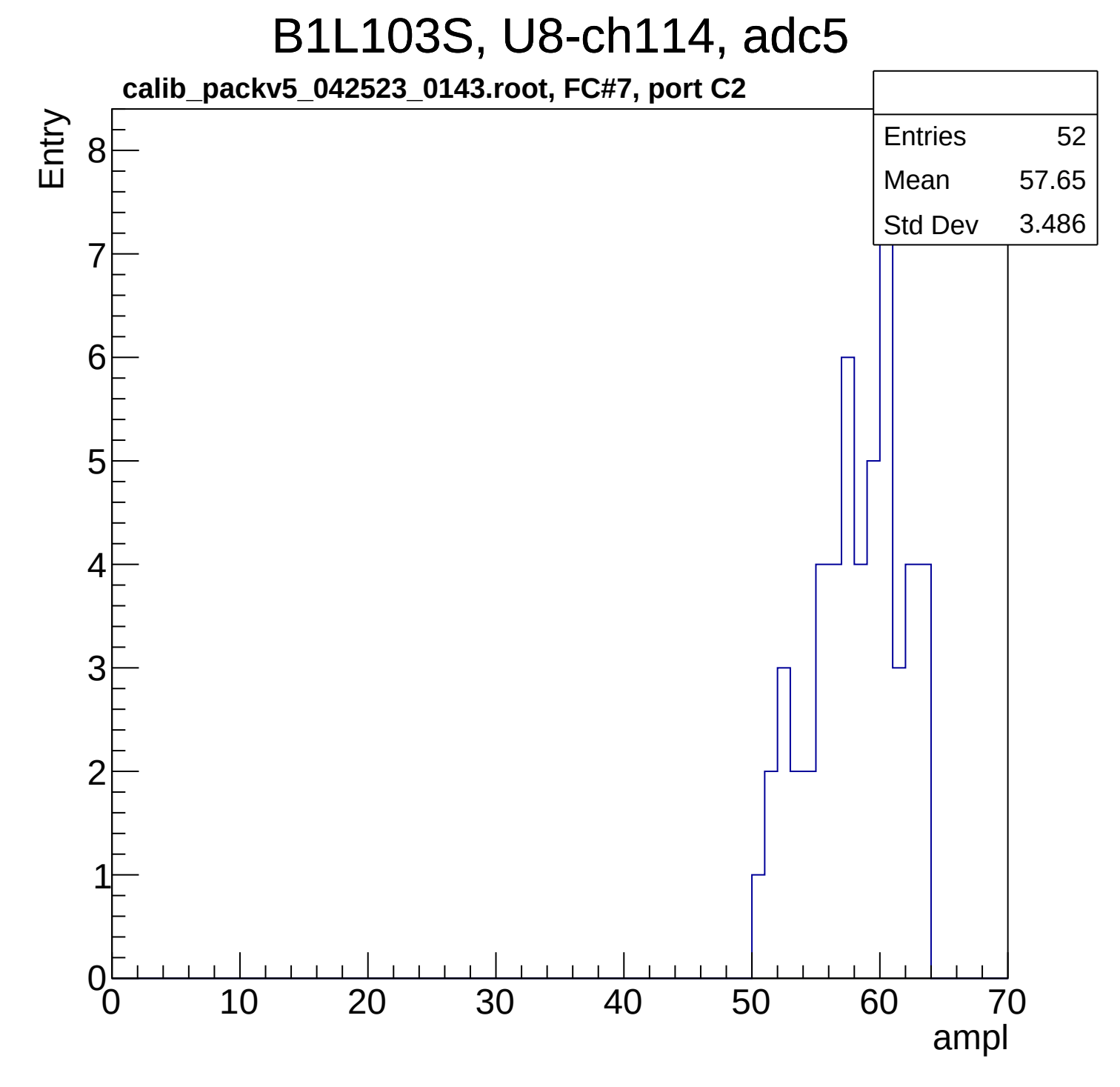

B1L103S, U8-ch114, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 28.3
Std Dev 3.831
Gaus mean : 28.6236
Gaus Width: 4.4391
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

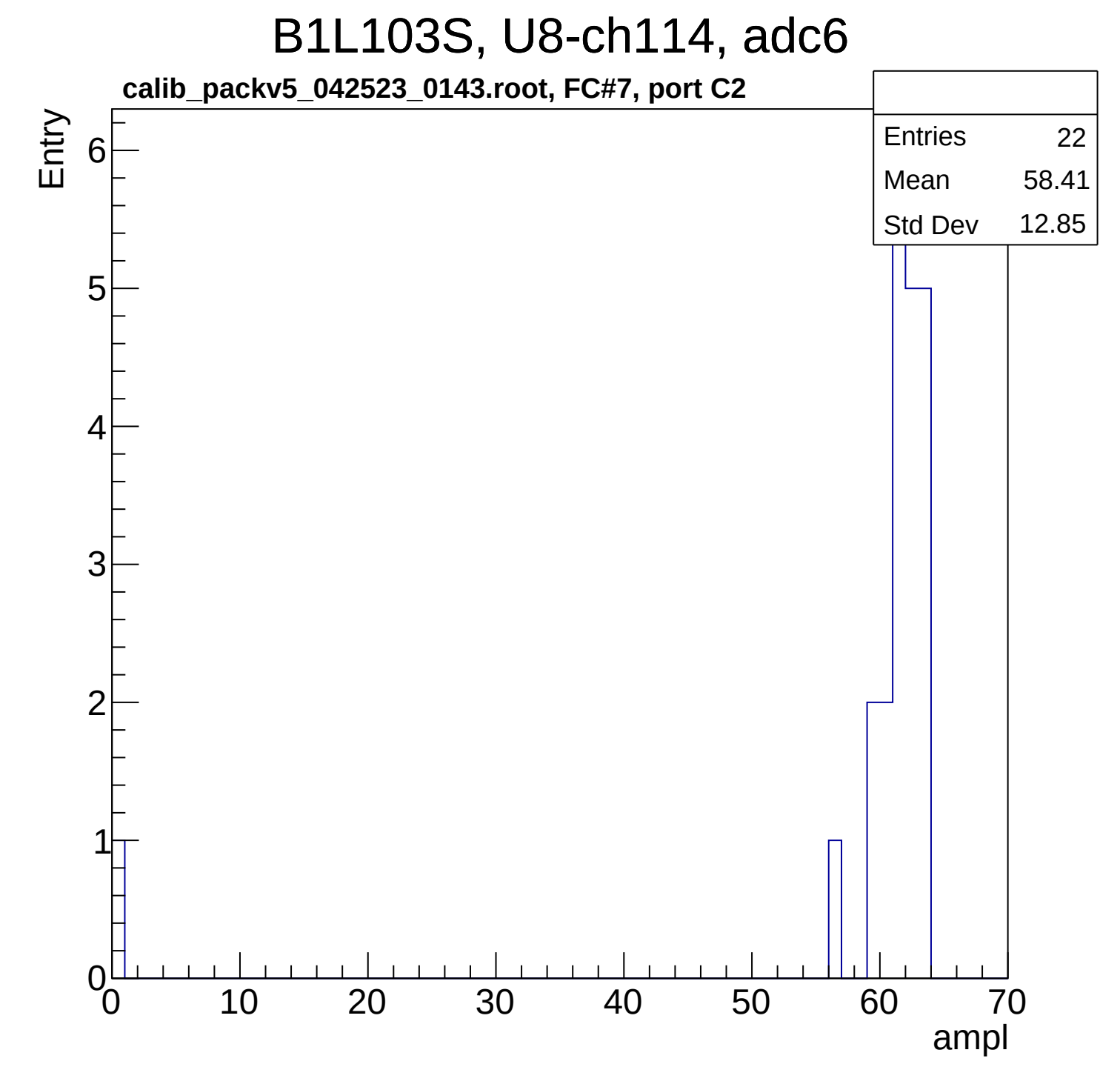

B1L103S, U8-ch114, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 34.52
Std Dev 3.717
Gaus mean : 35.5154
Gaus Width: 3.9963
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

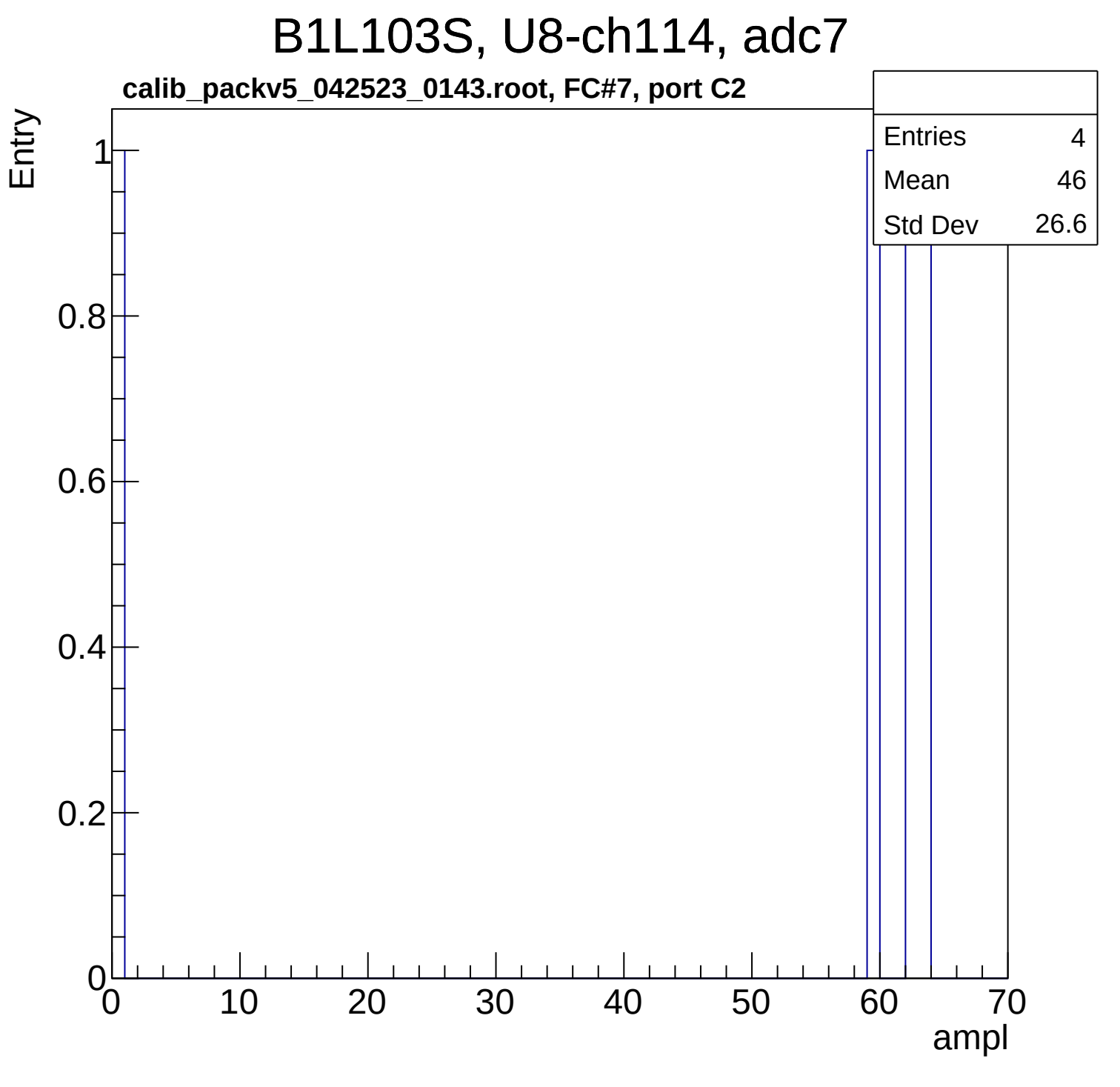

B1L103S, U8-ch114, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 40.83
Std Dev 3.429
Gaus mean : 40.4827
Gaus Width: 5.0411
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

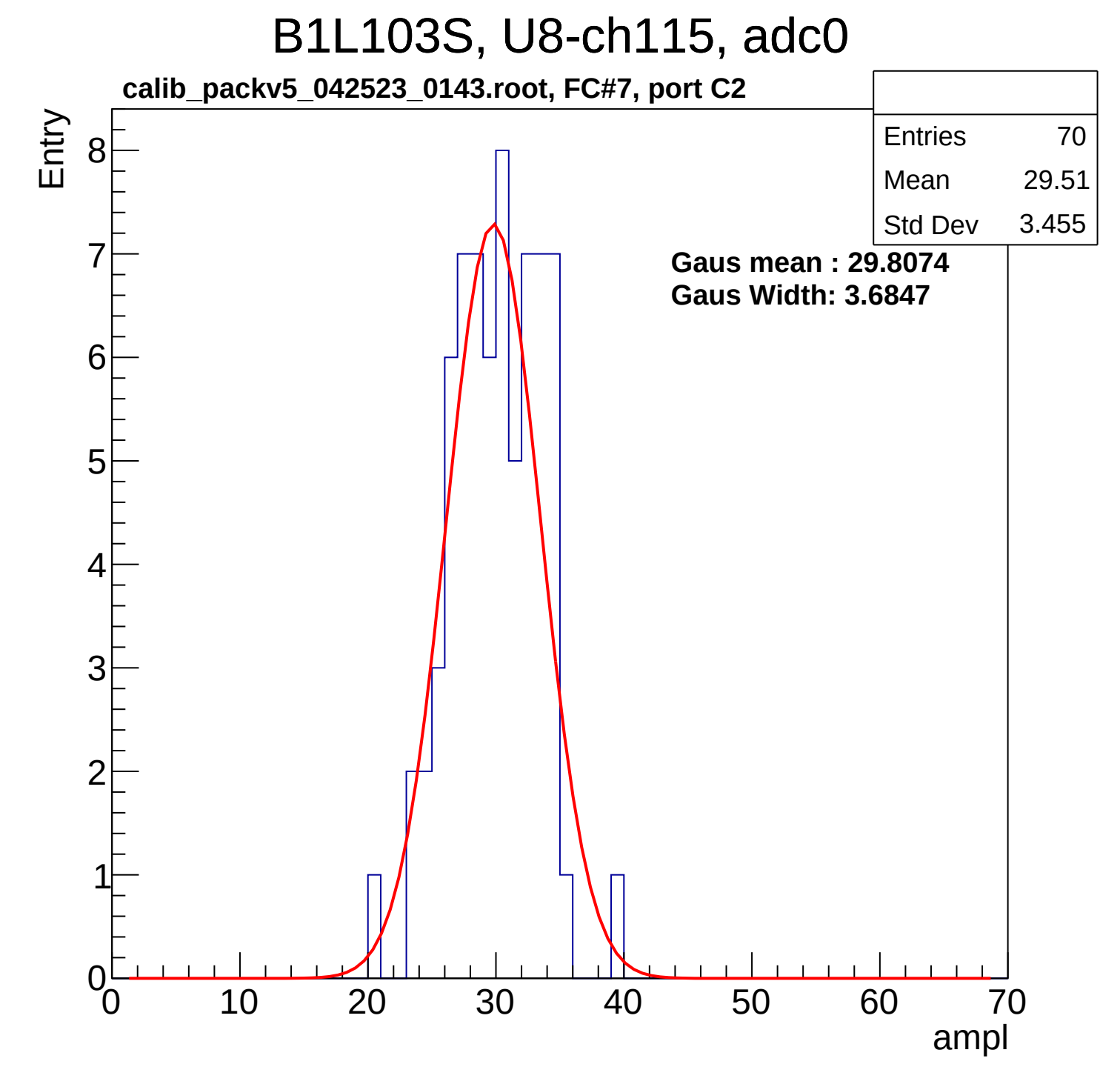

B1L103S, U8-ch114, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 59
Mean 46.51
Std Dev 3.752
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

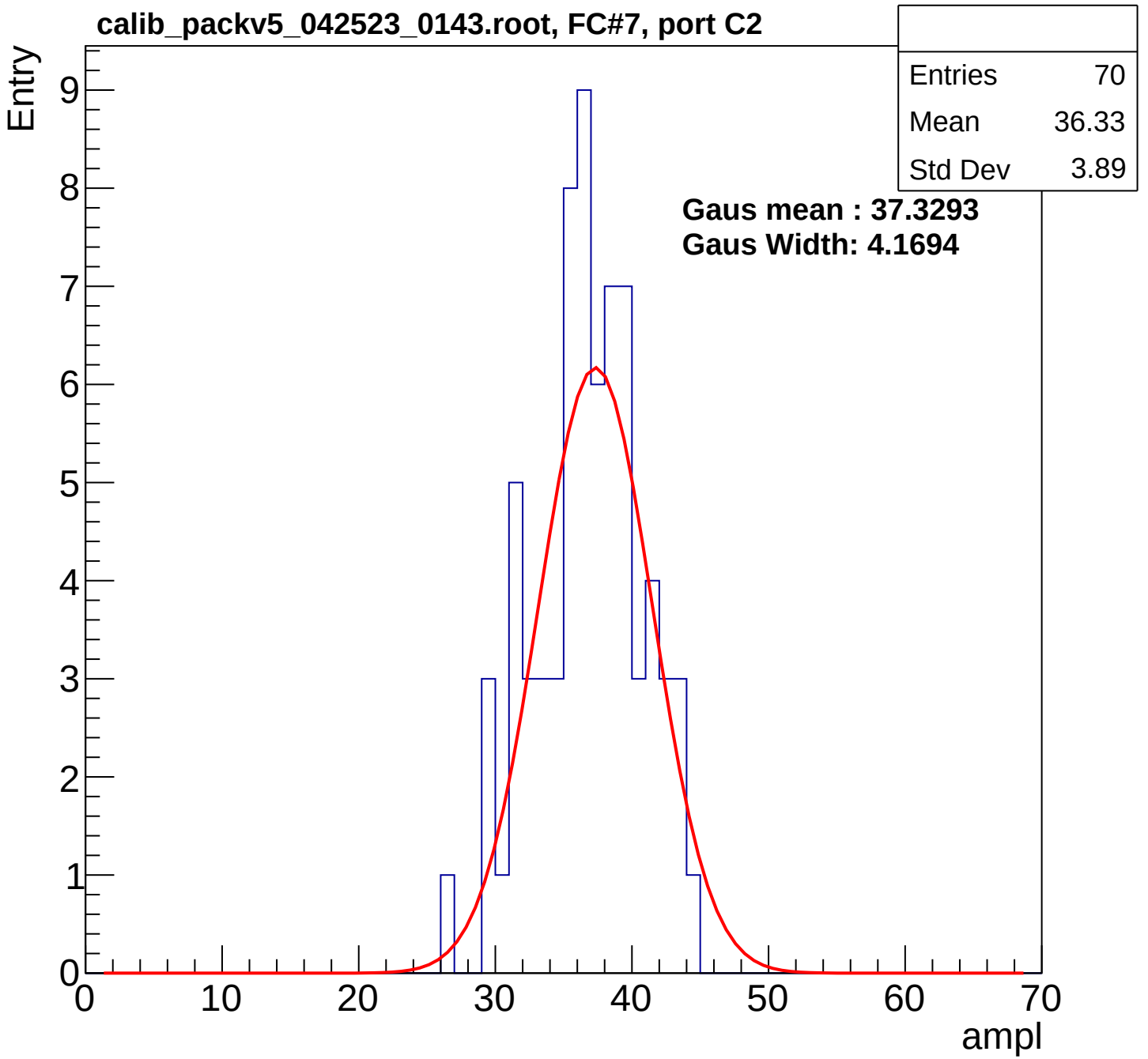

B1L103S, U8-ch114, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 52.82
Std Dev 3.705
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

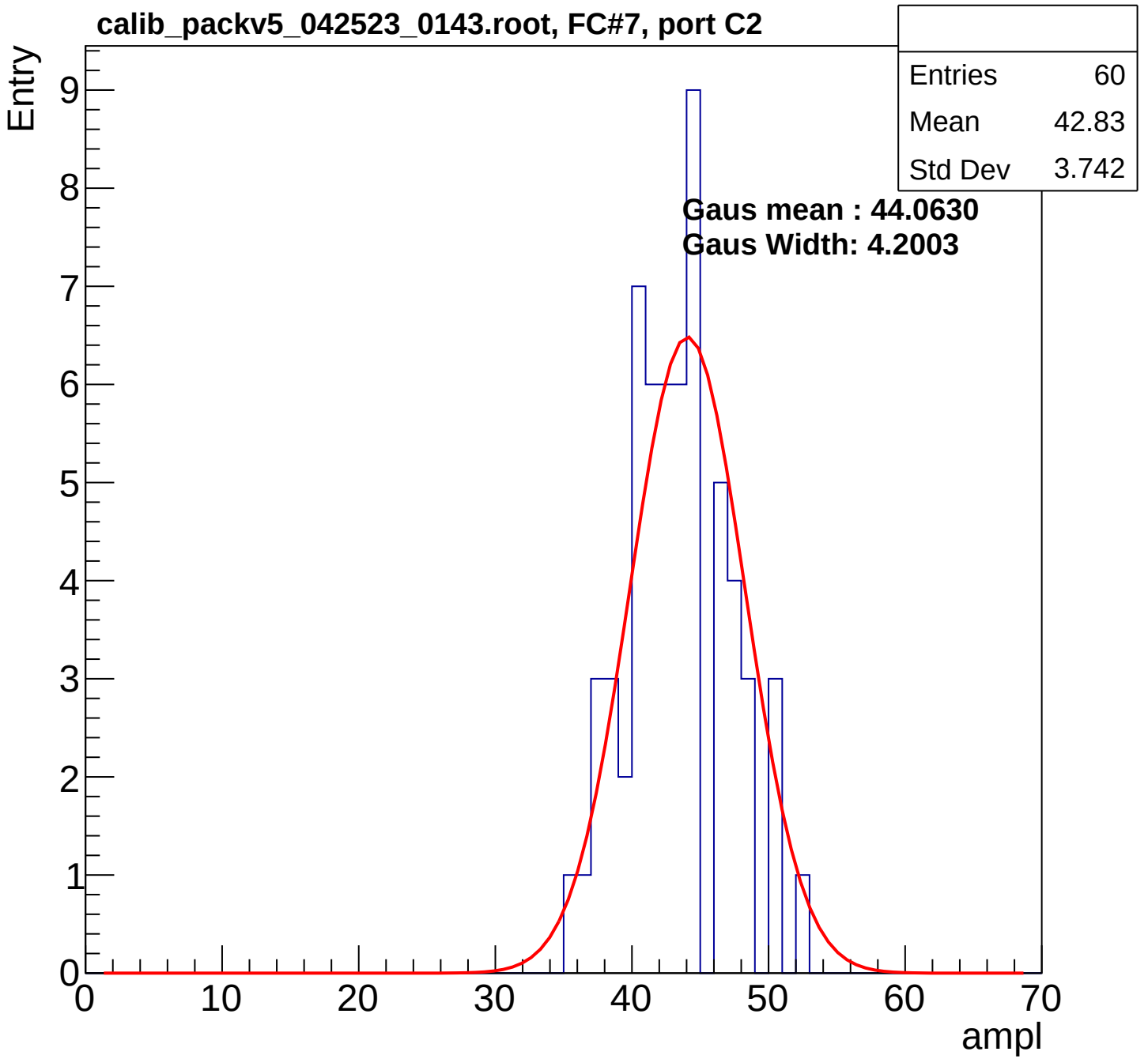

B1L103S, U8-ch114, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 57.65
Std Dev 3.486
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

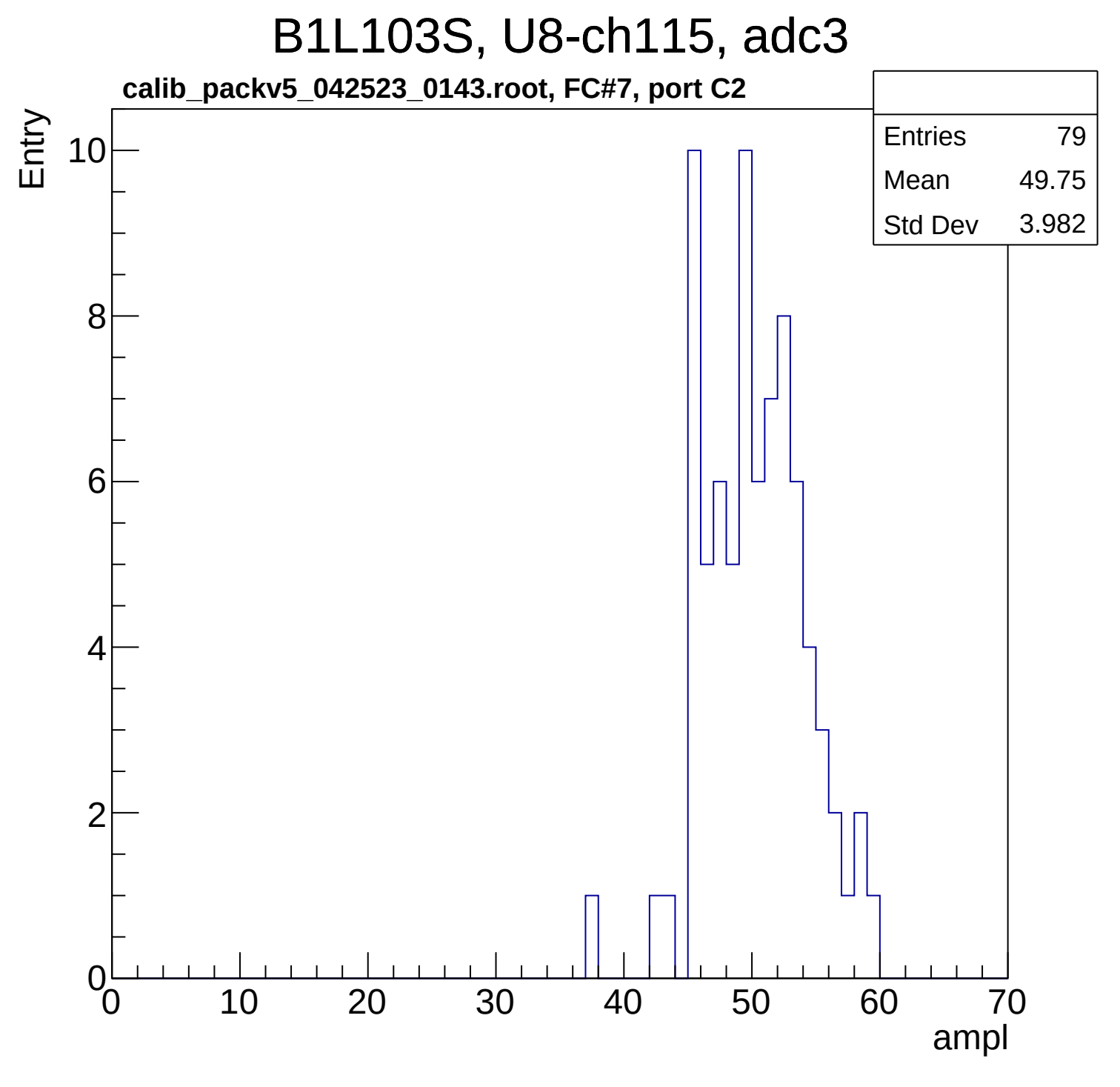

B1L103S, U8-ch114, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 22
Mean 58.41
Std Dev 12.85
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

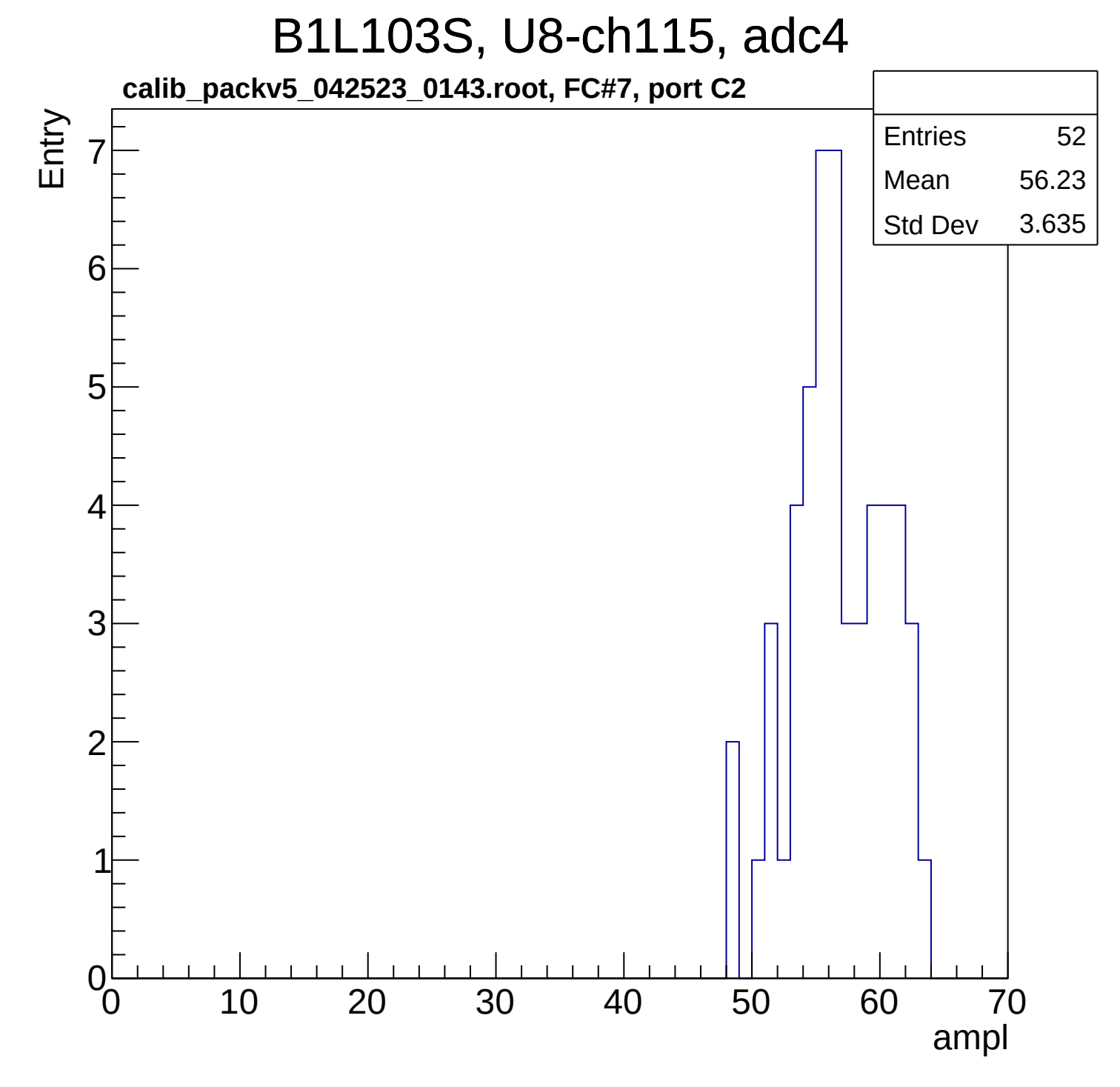

B1L103S, U8-ch114, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 46
Std Dev 26.6
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

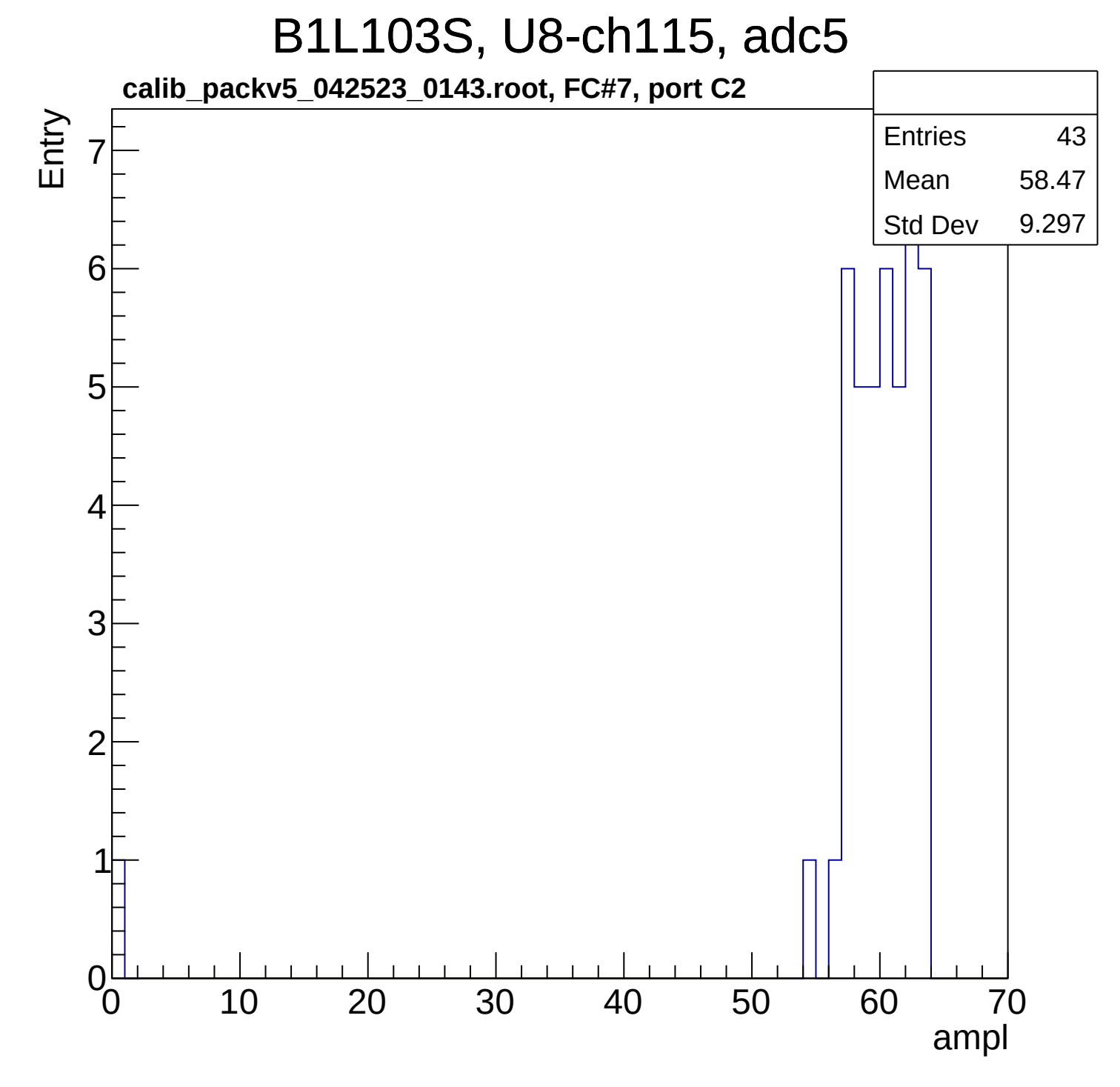

B1L103S, U8-ch115, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 29.51
Std Dev 3.455
Gaus mean : 29.8074
Gaus Width: 3.6847
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

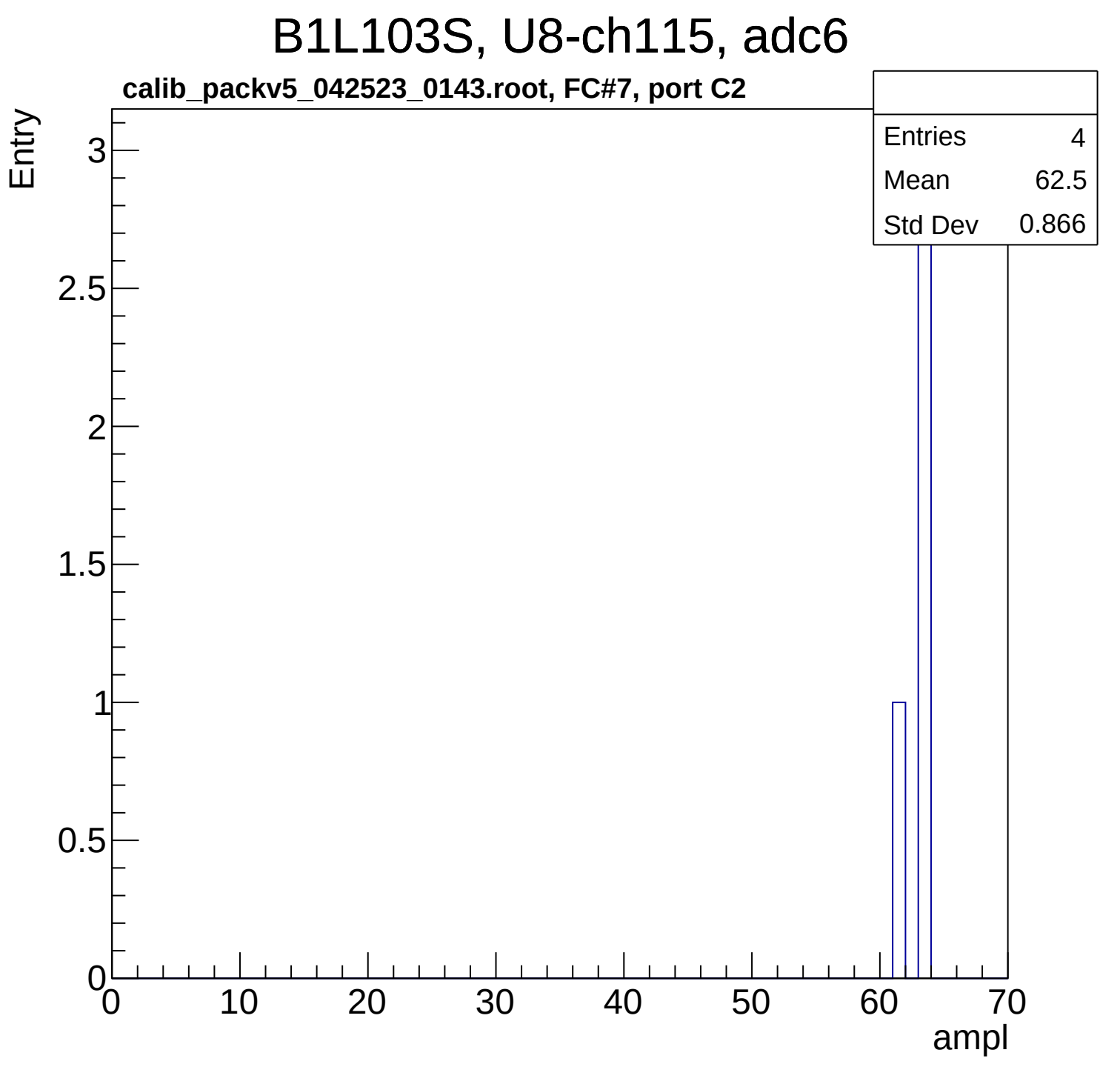

B1L103S, U8-ch115, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 70
Mean 36.33
Std Dev 3.89
Gaus mean : 37.3293
Gaus Width: 4.1694
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

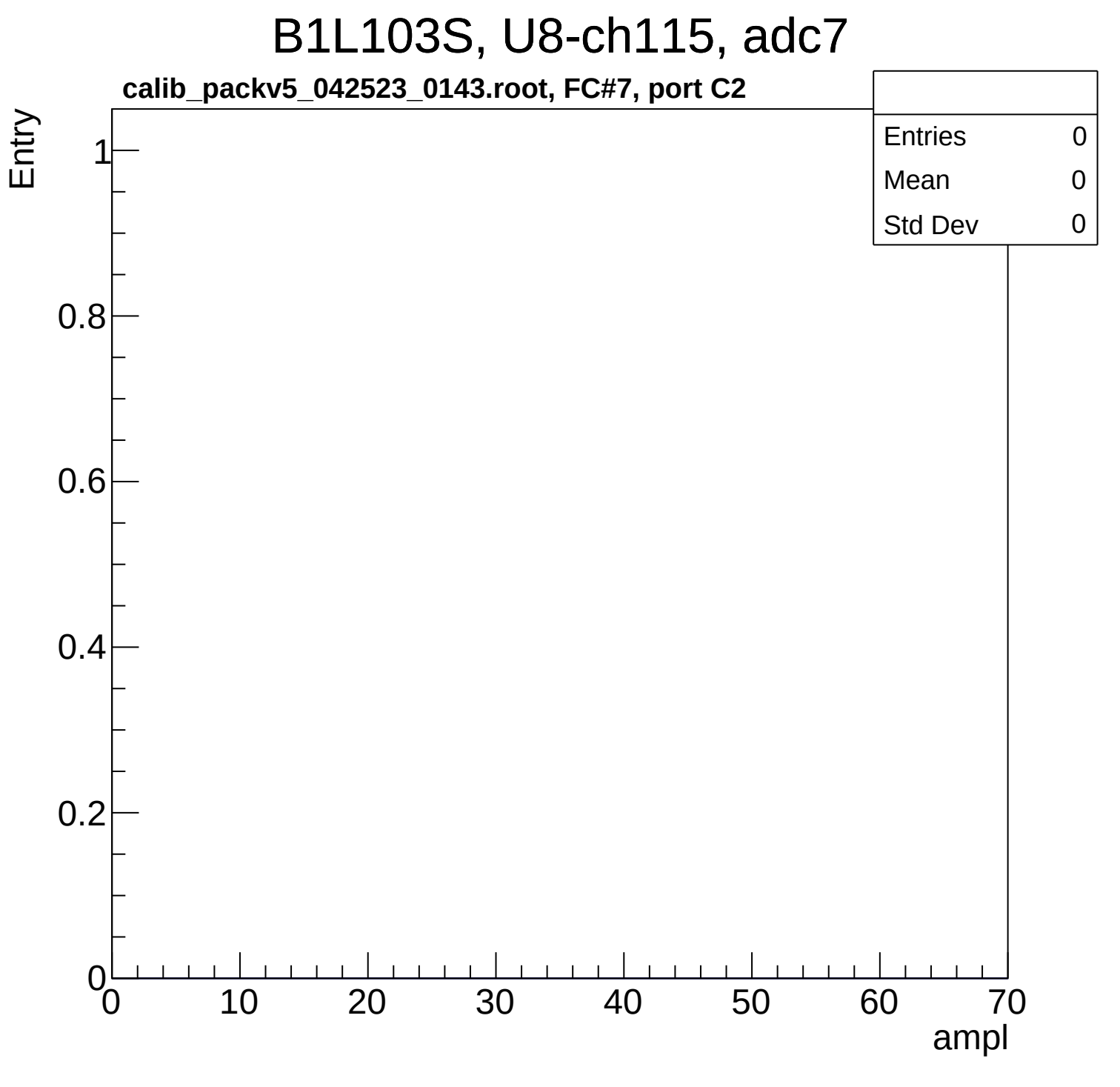

B1L103S, U8-ch115, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 42.83
Std Dev 3.742
Gaus mean : 44.0630
Gaus Width: 4.2003
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

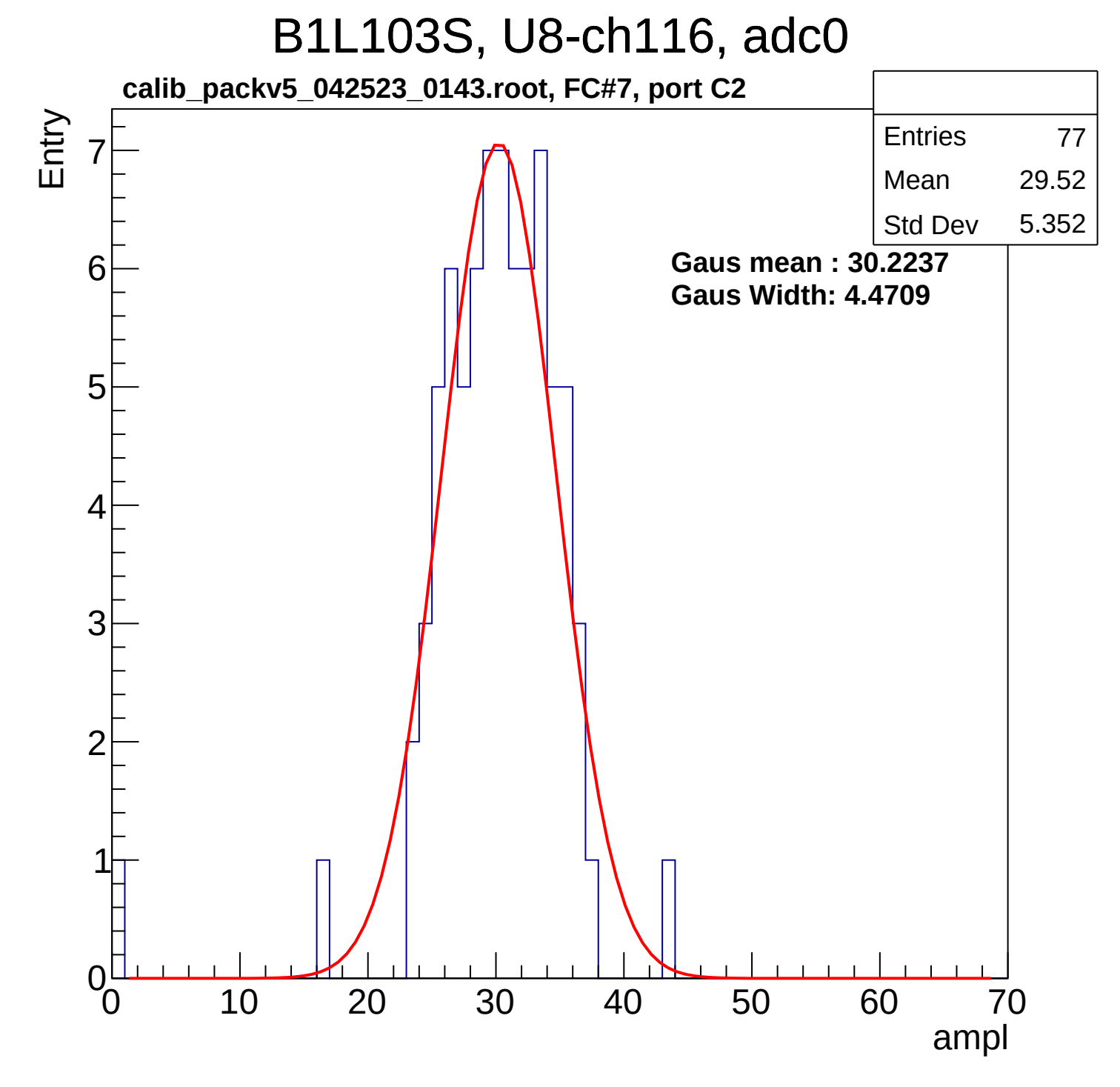

B1L103S, U8-ch115, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 79
Mean 49.75
Std Dev 3.982
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

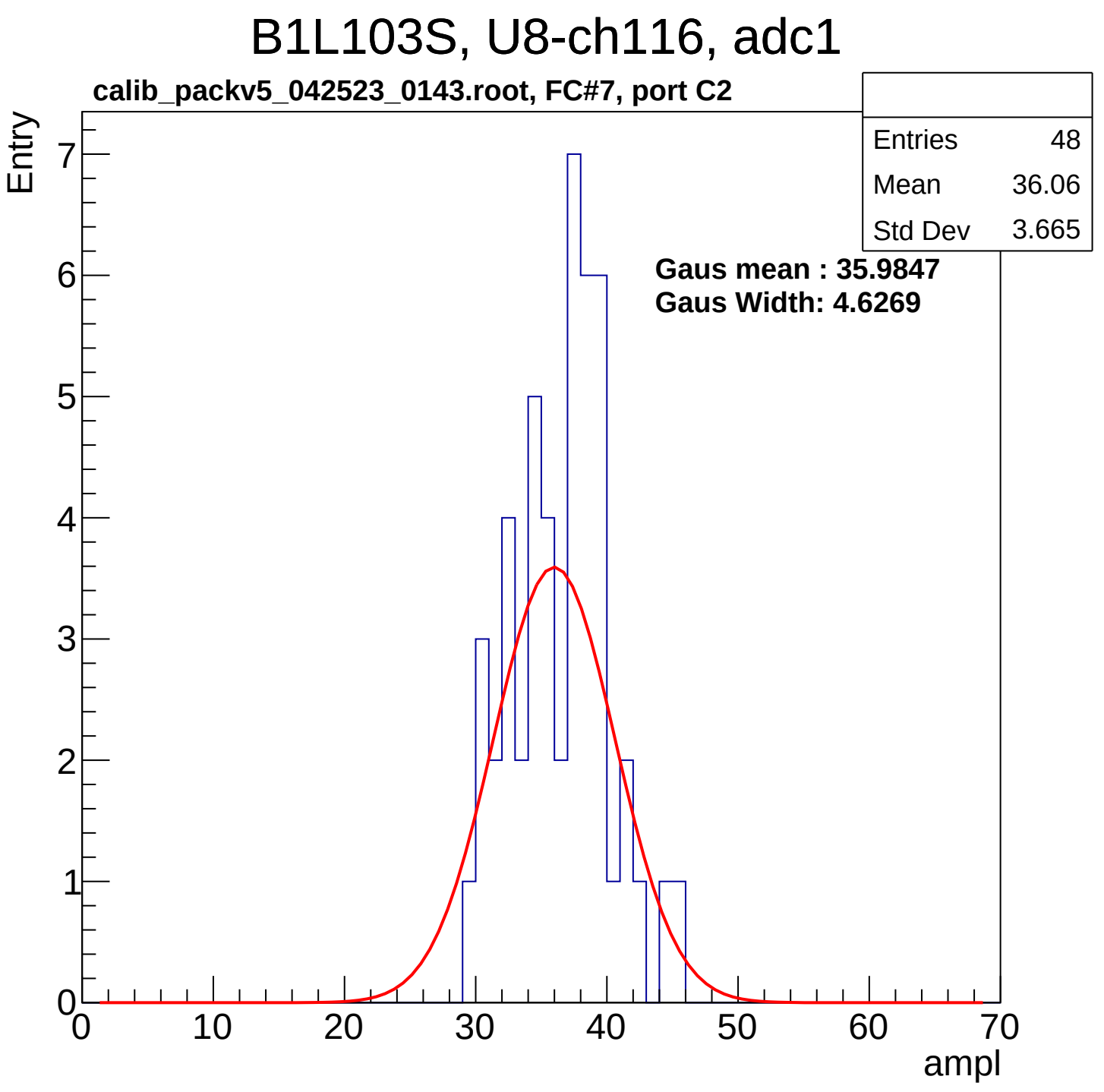

B1L103S, U8-ch115, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 56.23
Std Dev 3.635
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

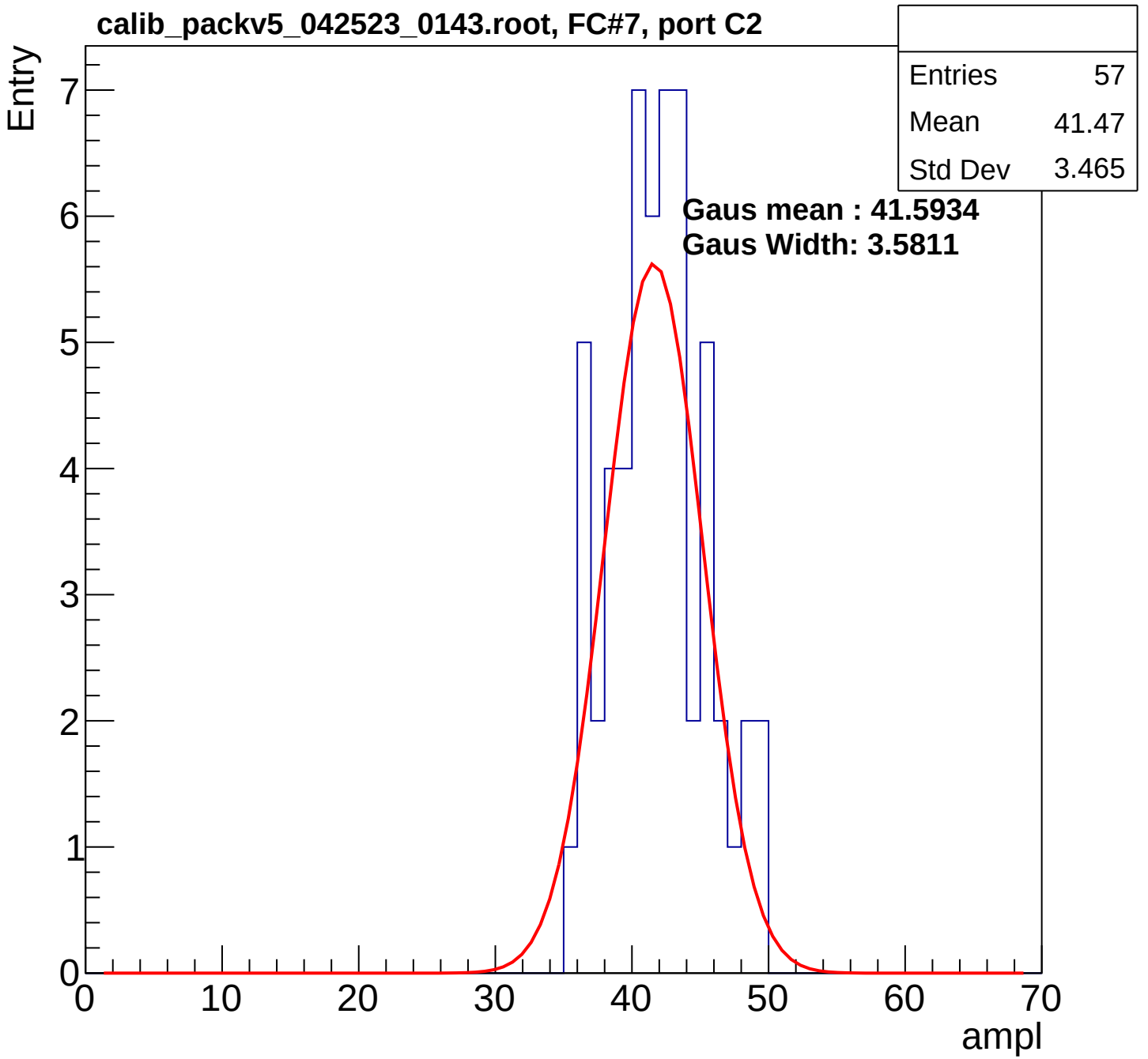

B1L103S, U8-ch115, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 43
Mean 58.47
Std Dev 9.297
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

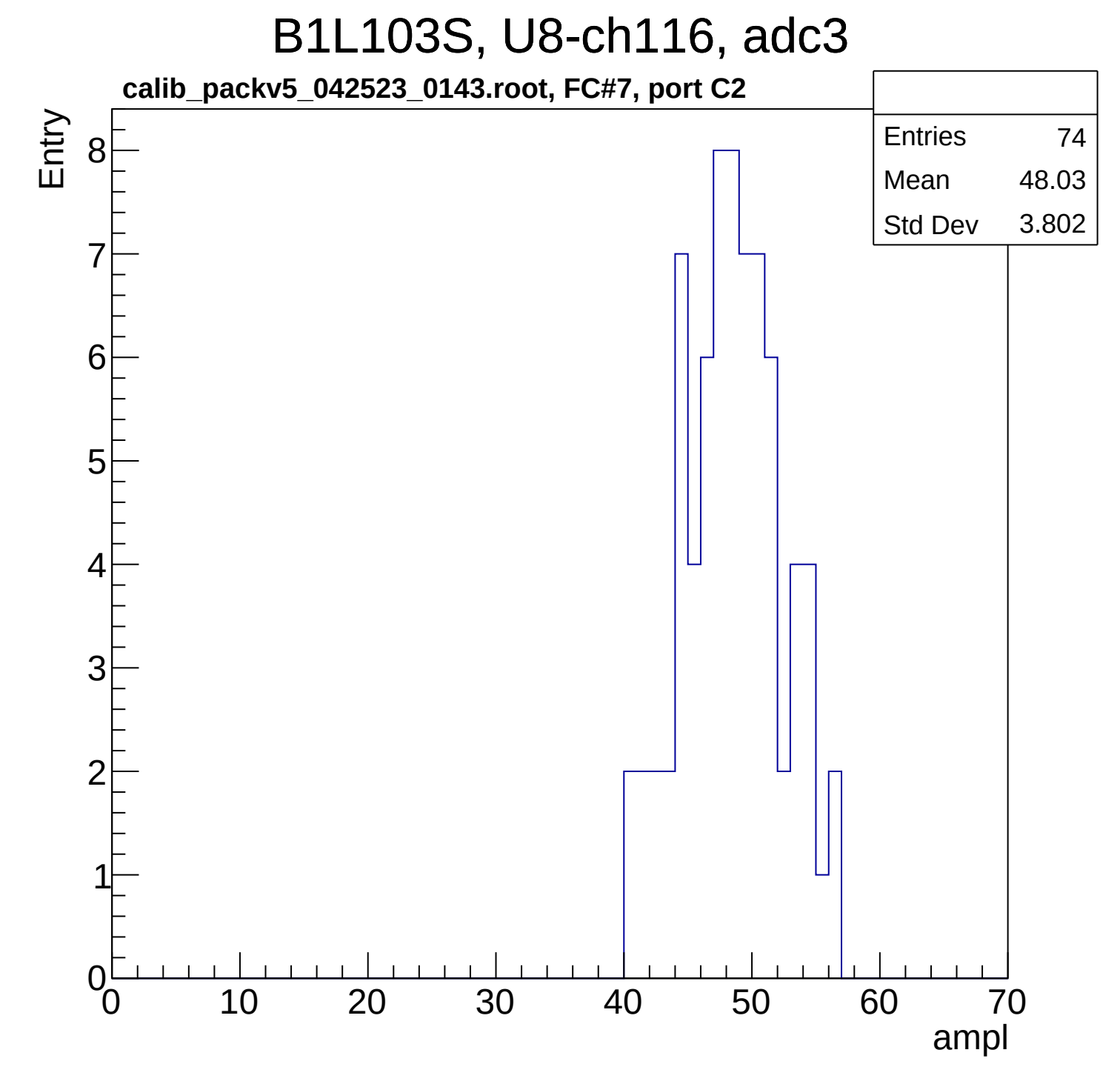

B1L103S, U8-ch115, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 62.5
Std Dev 0.866
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

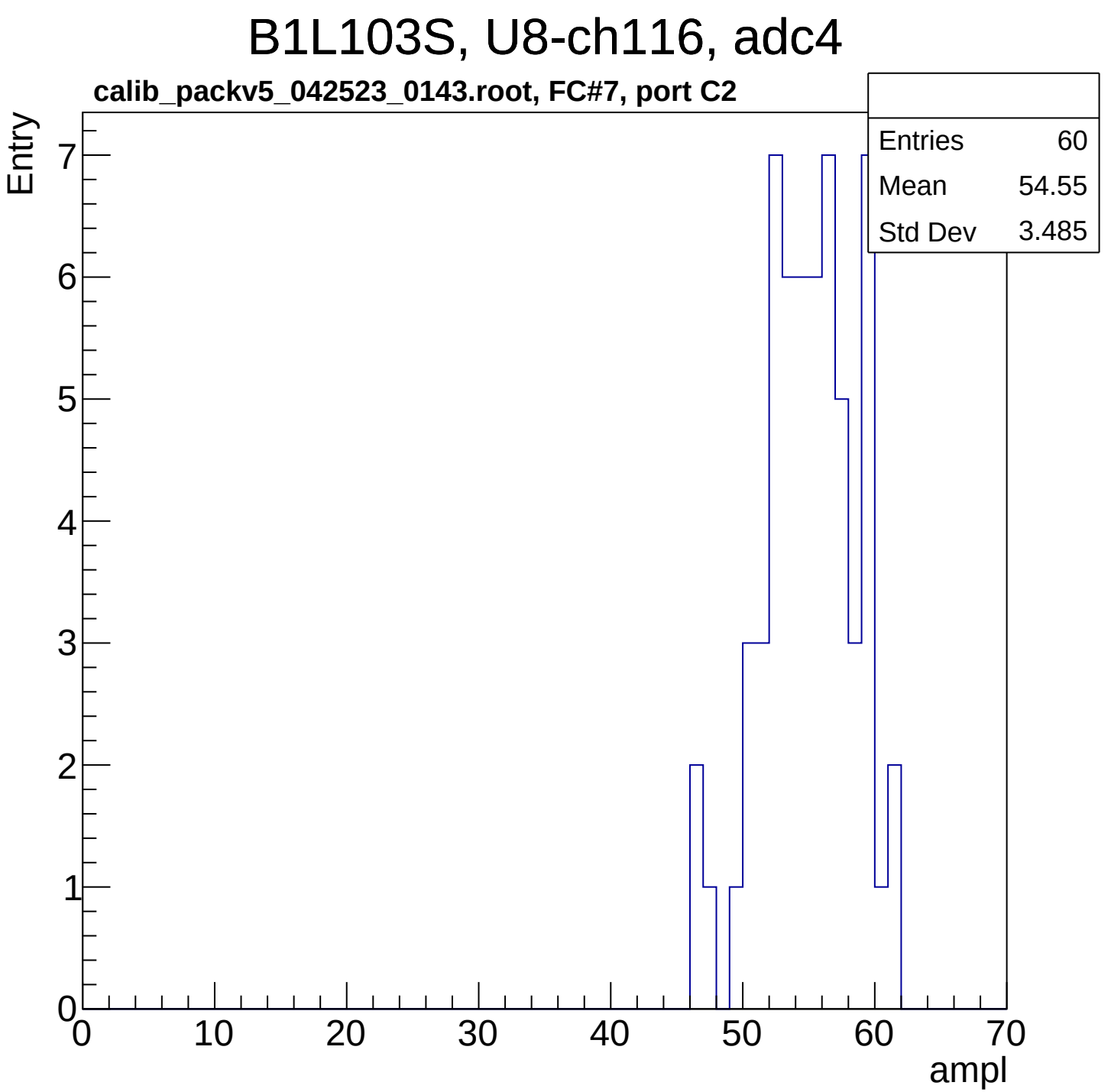

B1L103S, U8-ch115, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

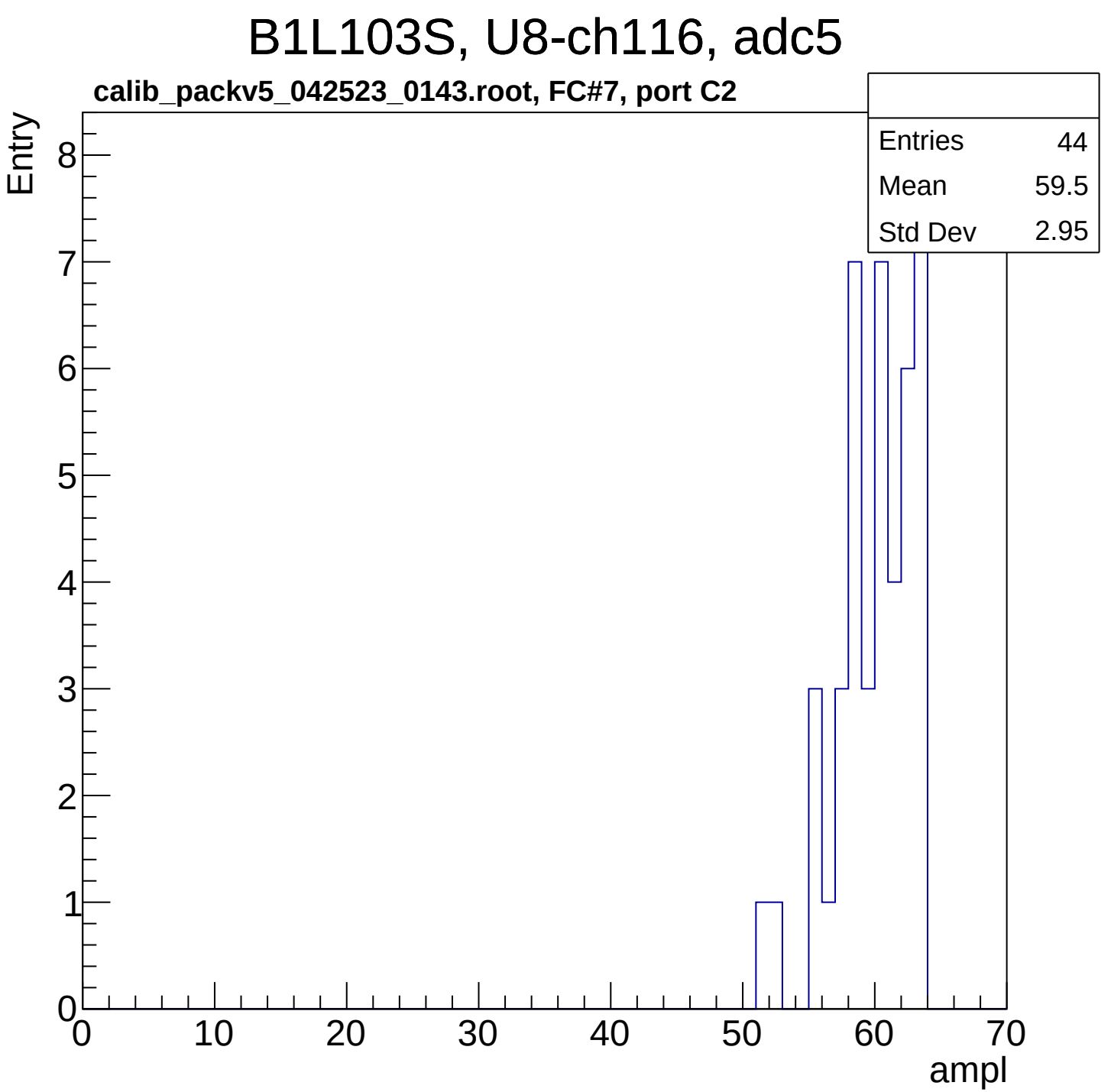

B1L103S, U8-ch116, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 29.52
Std Dev 5.352
Gaus mean : 30.2237
Gaus Width: 4.4709
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

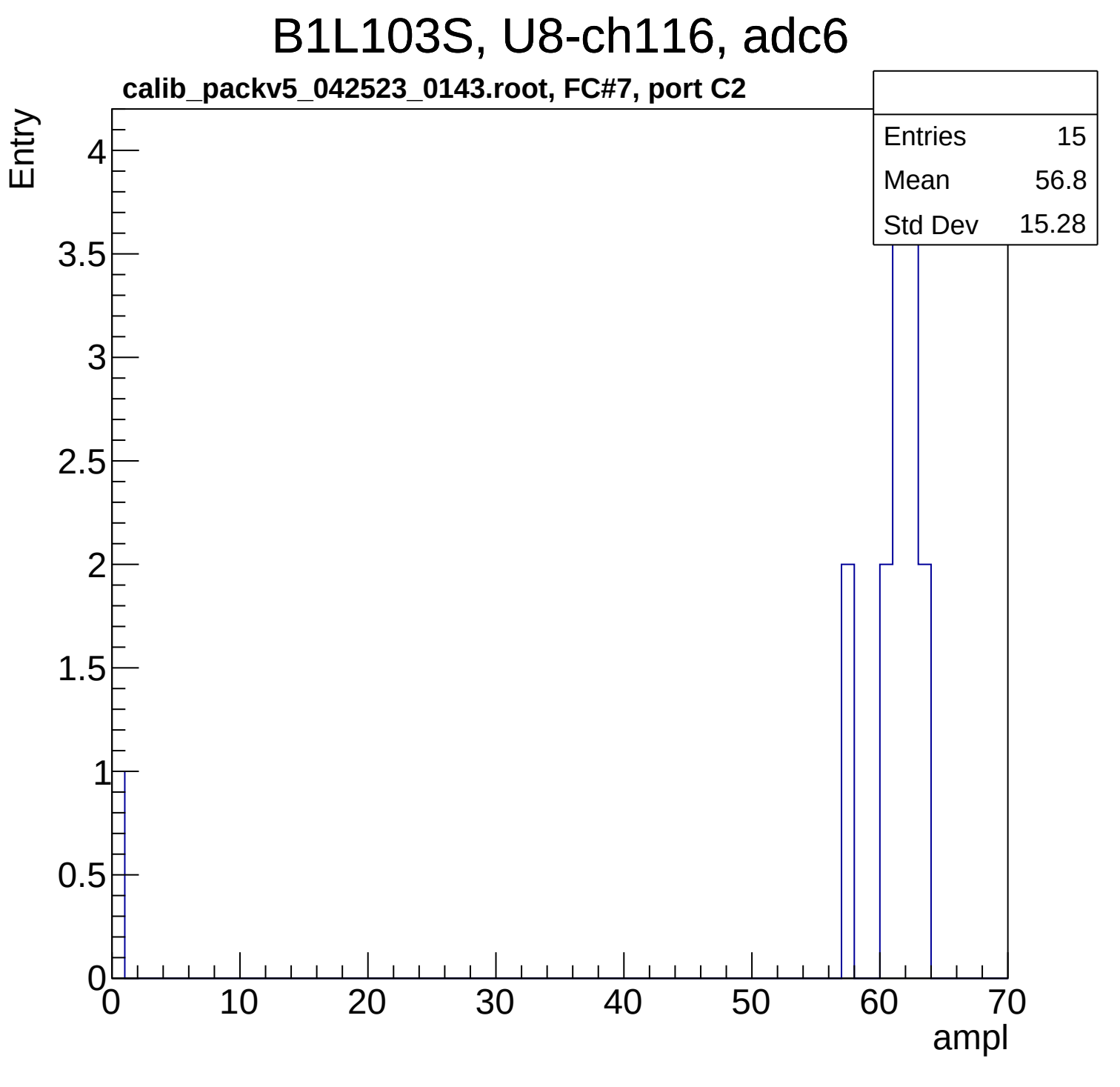

B1L103S, U8-ch116, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 36.06
Std Dev 3.665
Gaus mean : 35.9847
Gaus Width: 4.6269
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

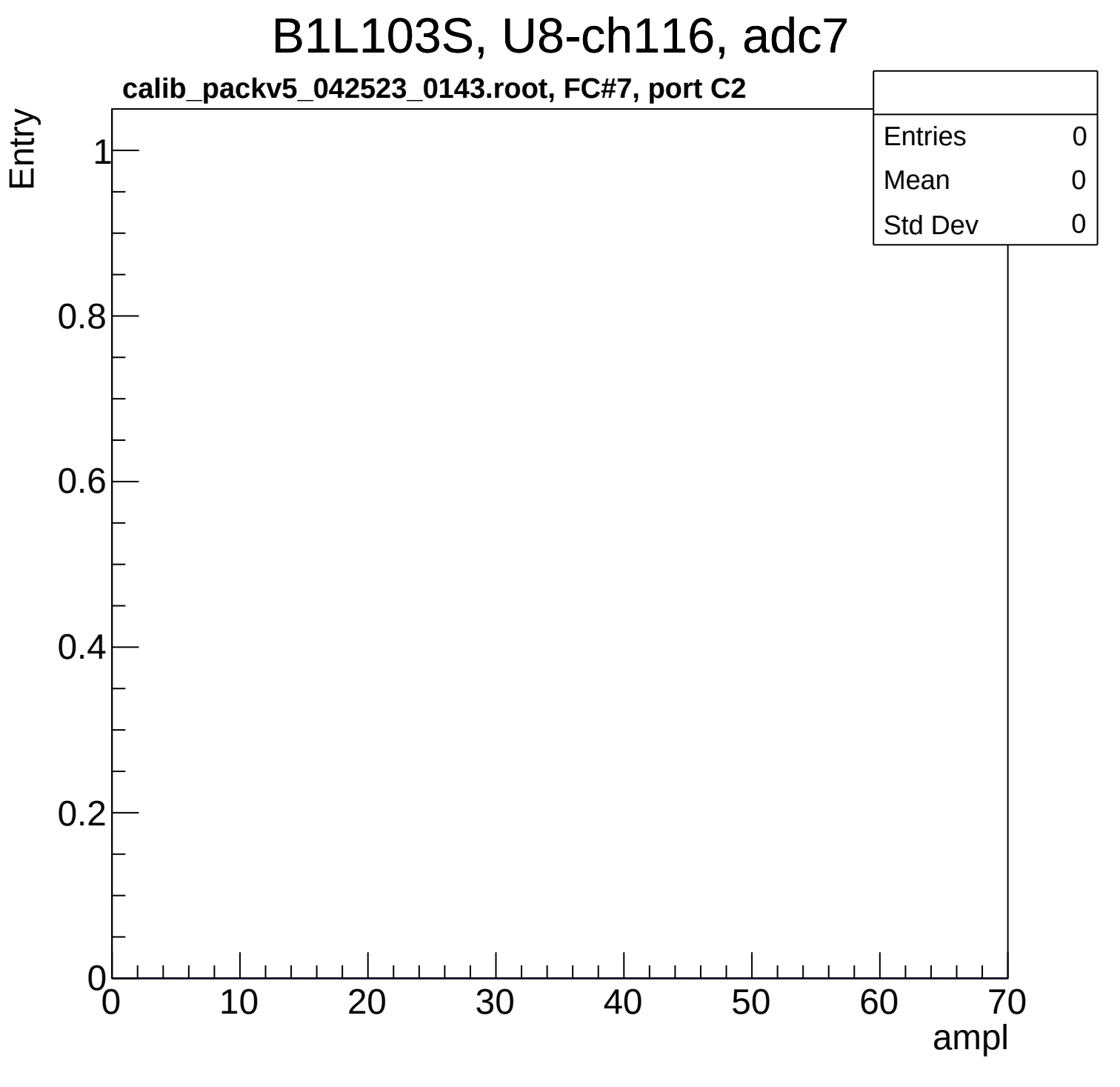

B1L103S, U8-ch116, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 41.47
Std Dev 3.465
Gaus mean : 41.5934
Gaus Width: 3.5811
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

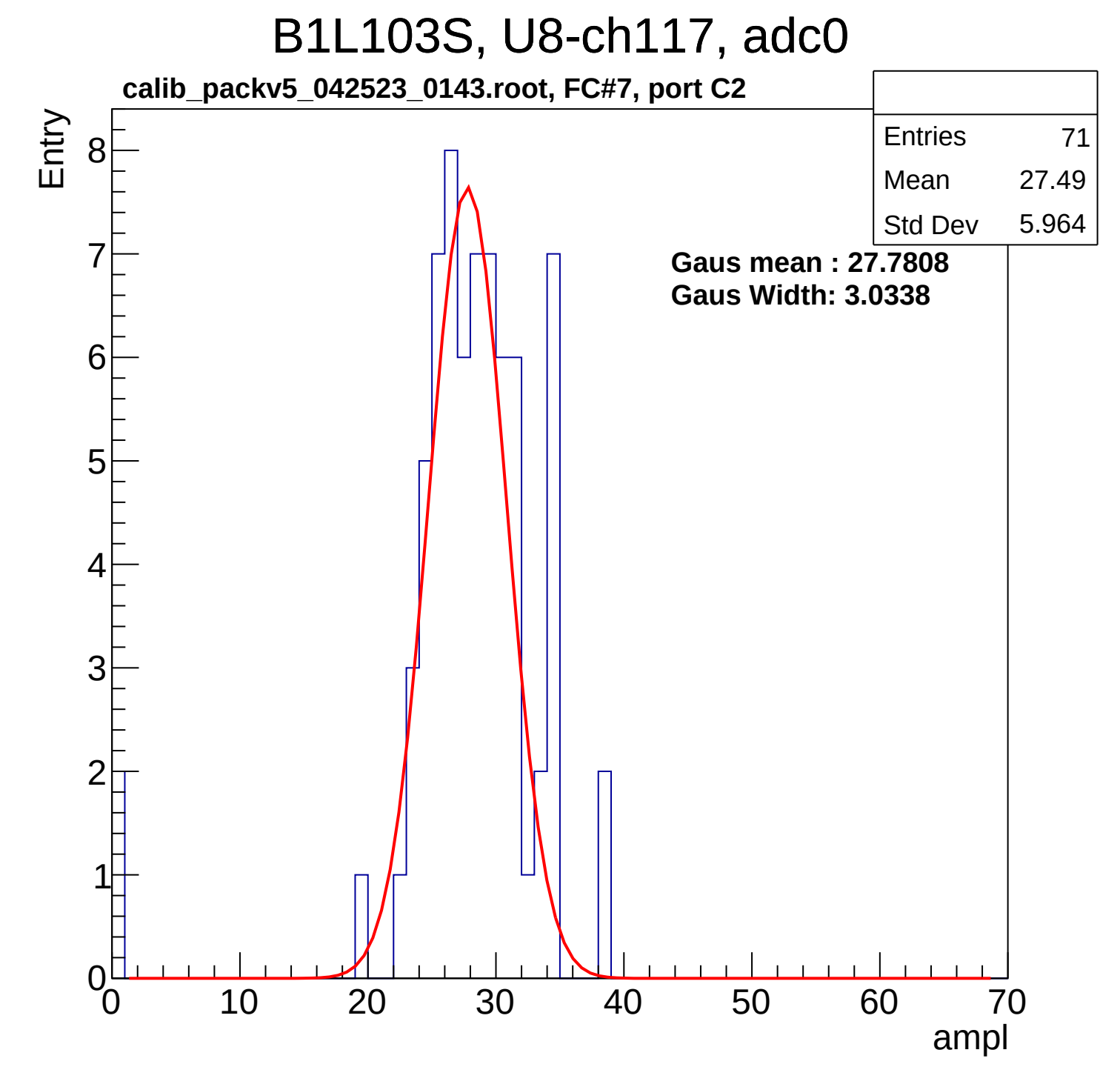

B1L103S, U8-ch116, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 74
Mean 48.03
Std Dev 3.802
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

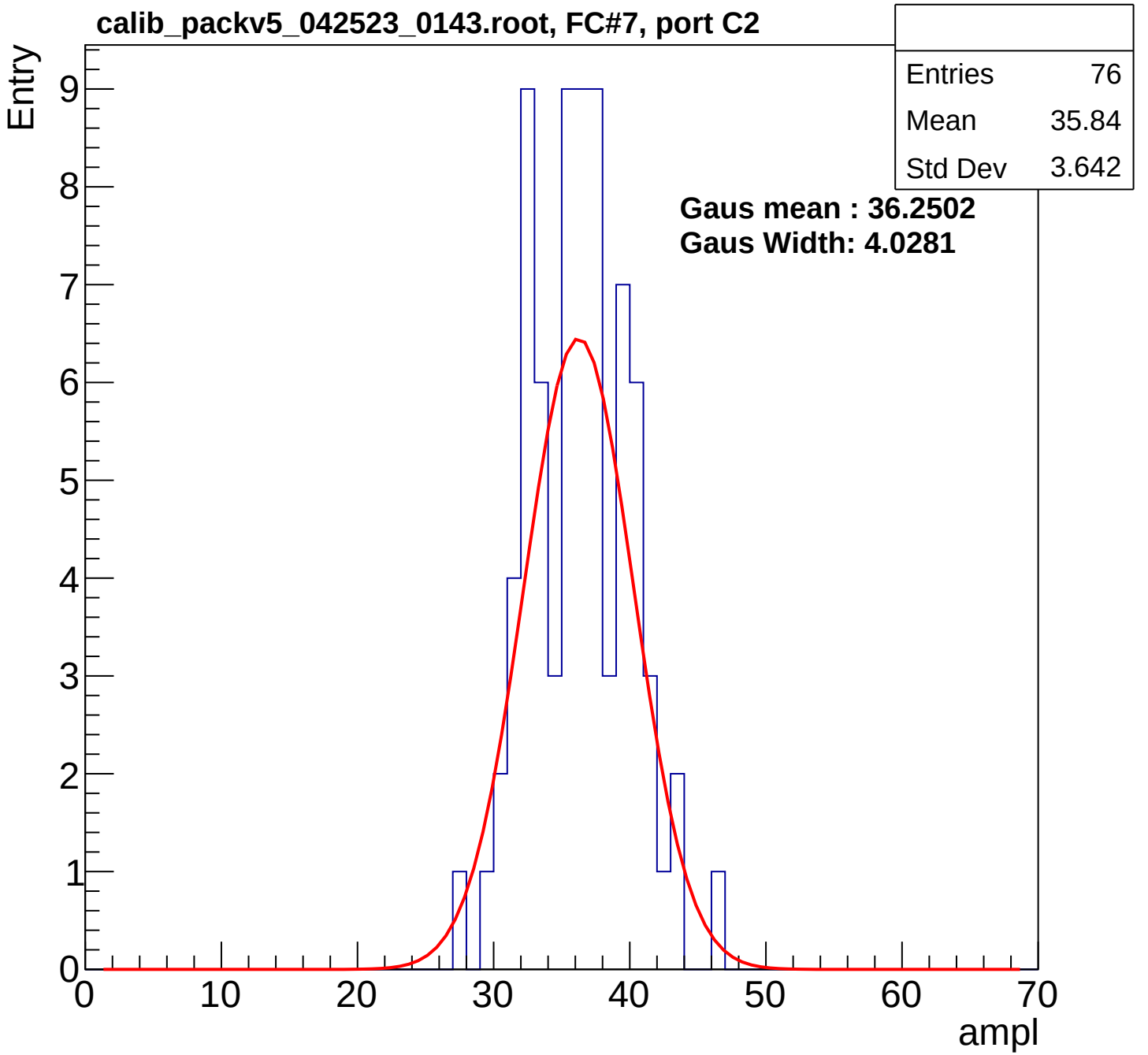

B1L103S, U8-ch116, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 54.55
Std Dev 3.485
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

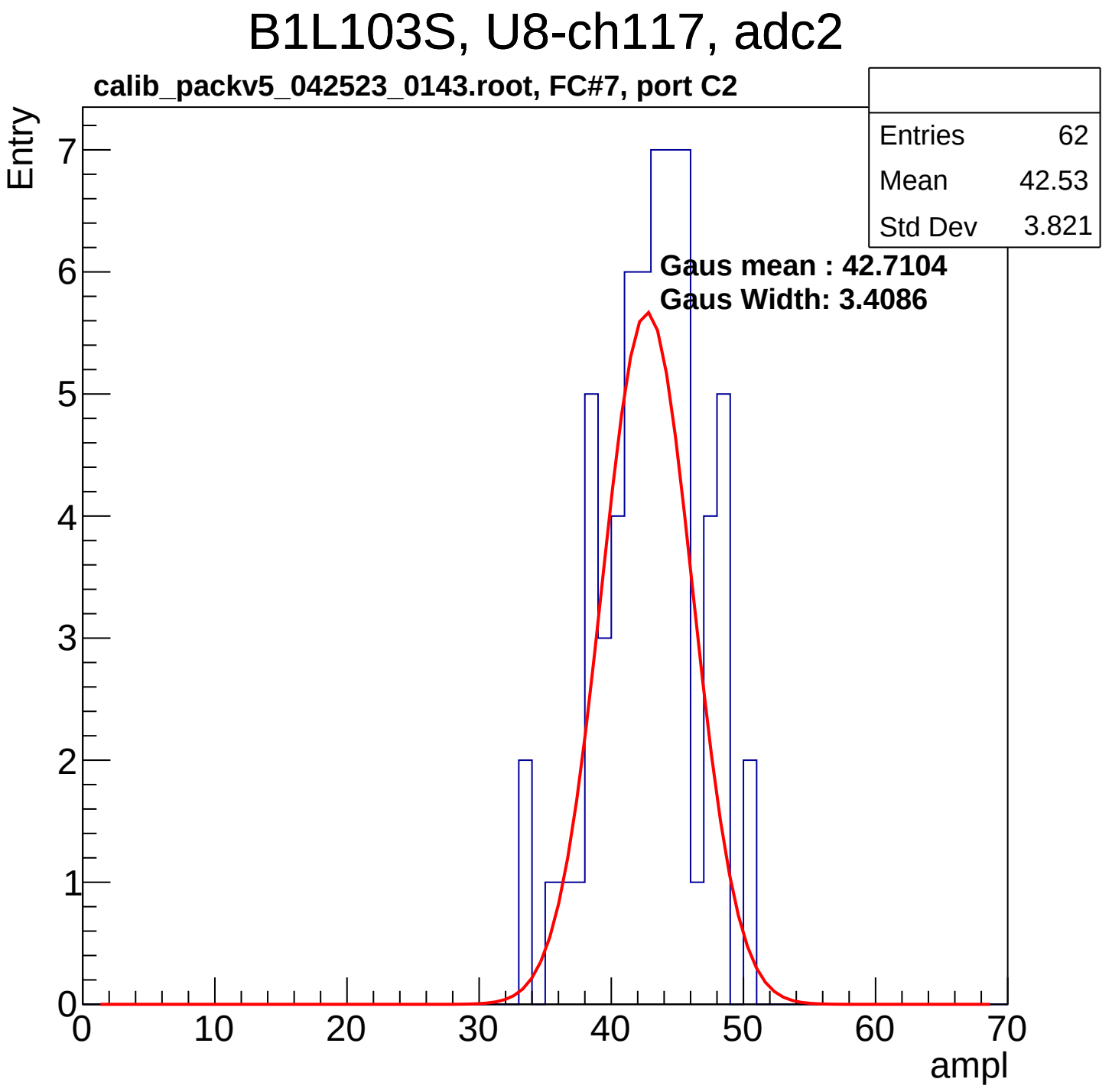

B1L103S, U8-ch116, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 44
Mean 59.5
Std Dev 2.95
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

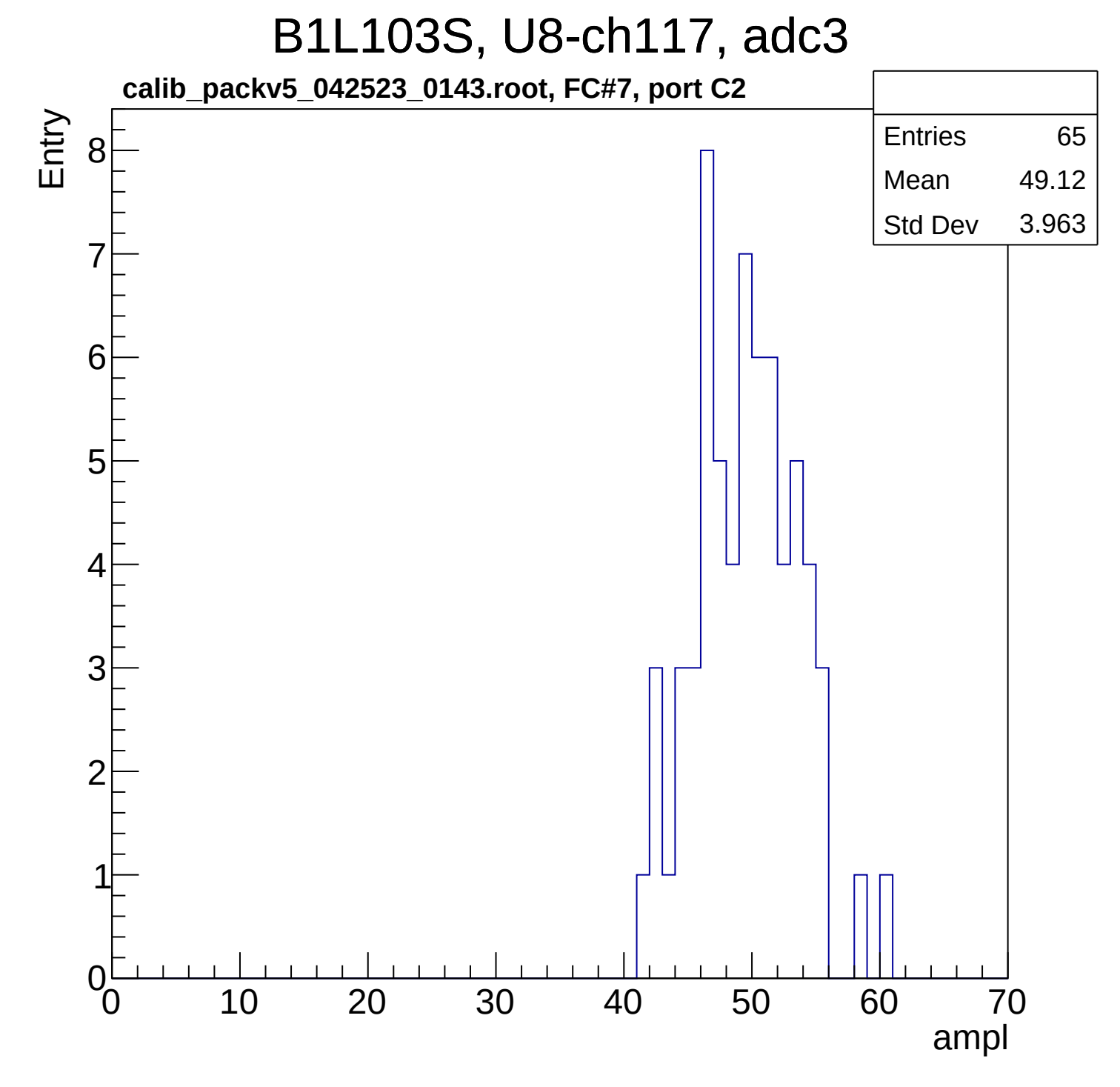

B1L103S, U8-ch116, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 15
Mean 56.8
Std Dev 15.28
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

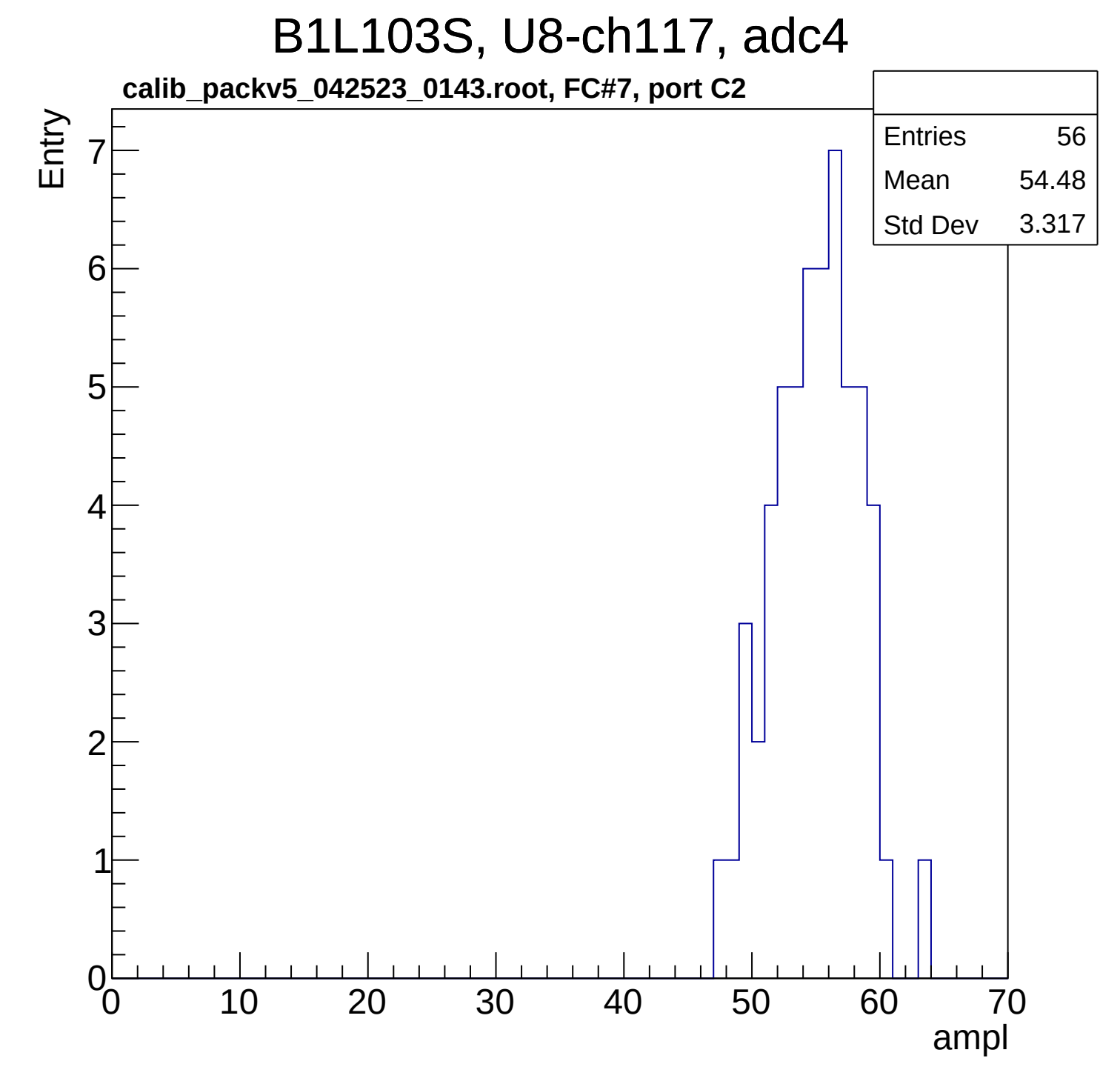

B1L103S, U8-ch116, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

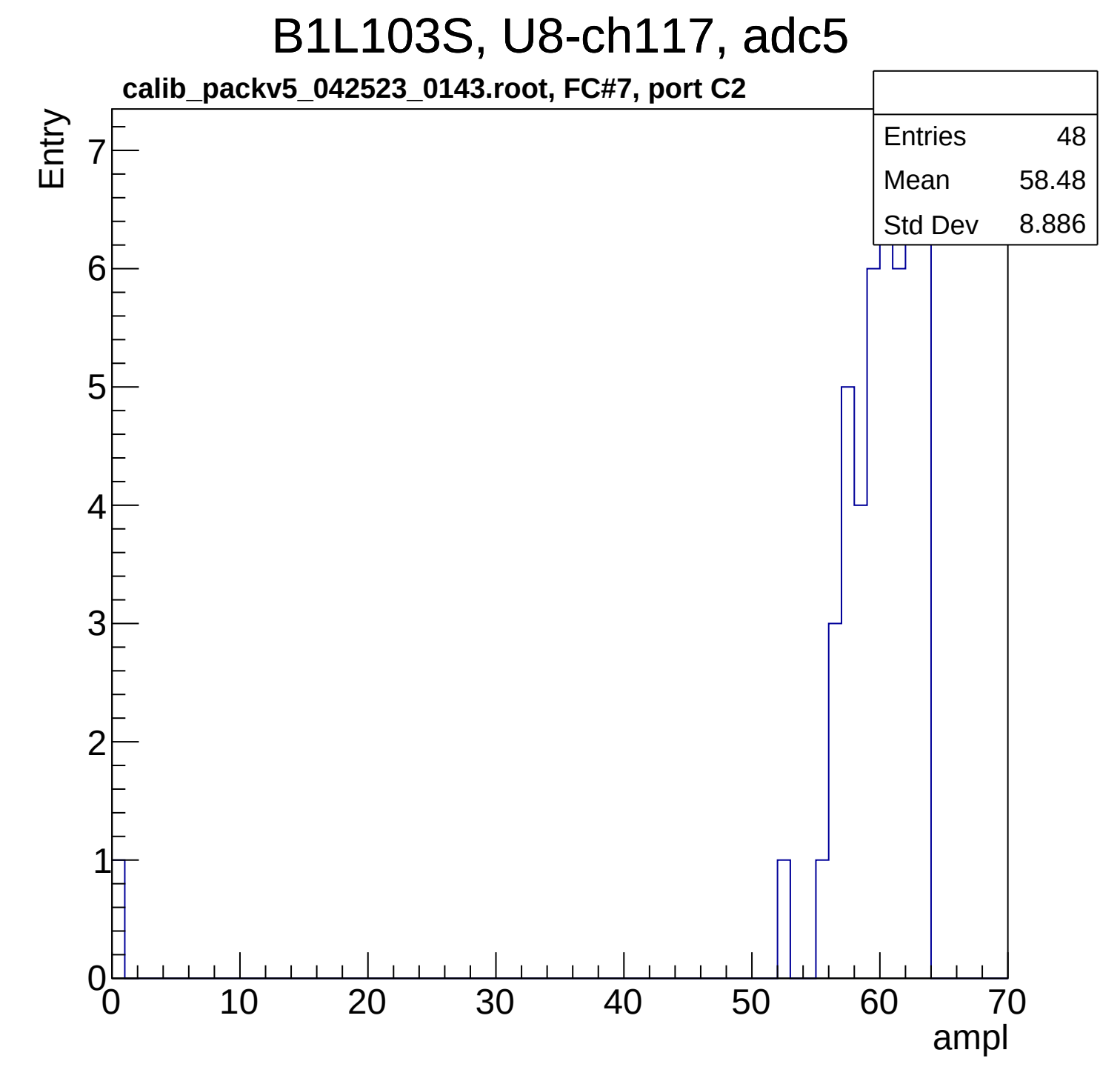

B1L103S, U8-ch117, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 27.49
Std Dev 5.964
Gaus mean : 27.7808
Gaus Width: 3.0338
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

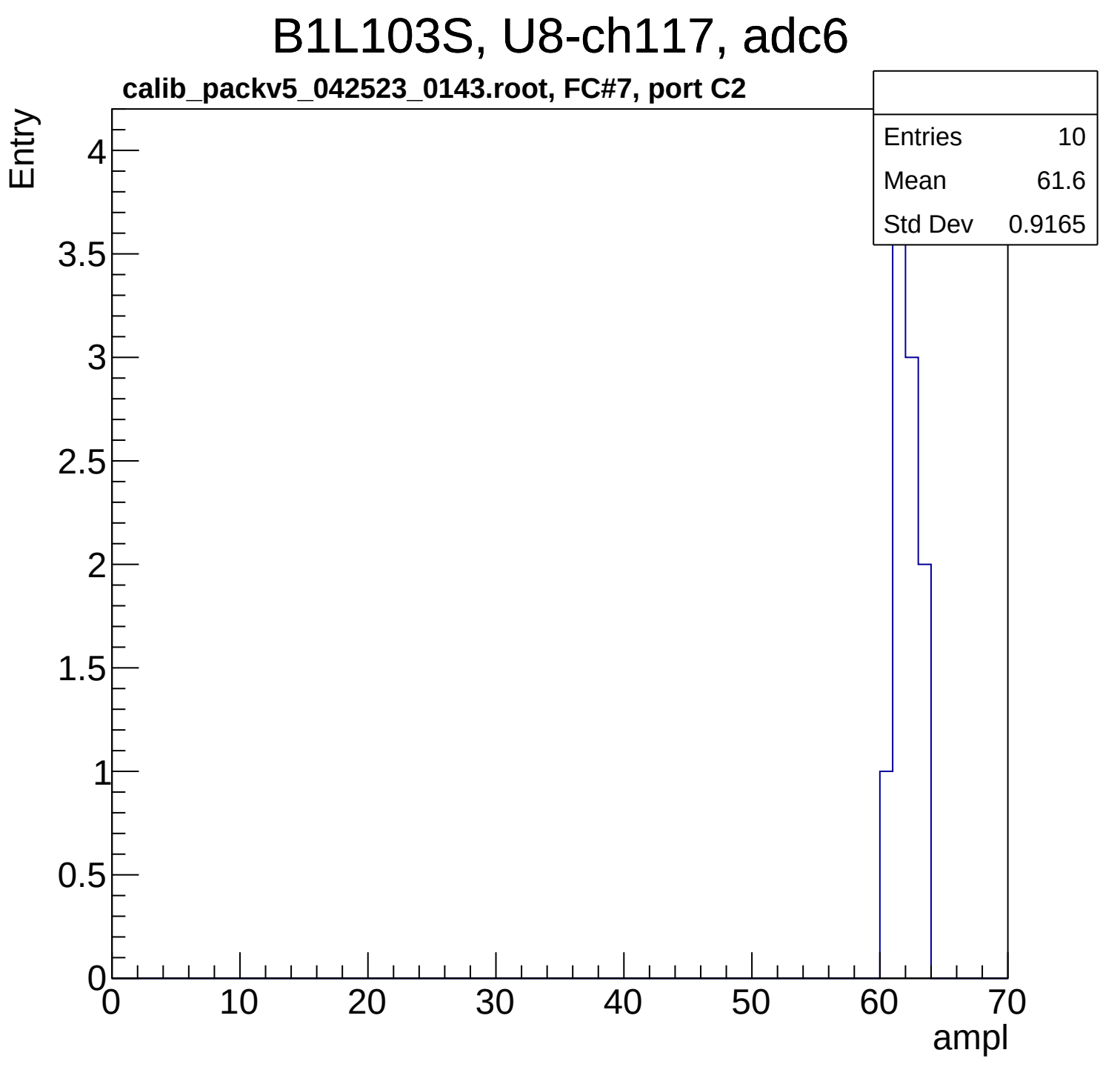

B1L103S, U8-ch117, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 76
Mean 35.84
Std Dev 3.642
Gaus mean : 36.2502
Gaus Width: 4.0281
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

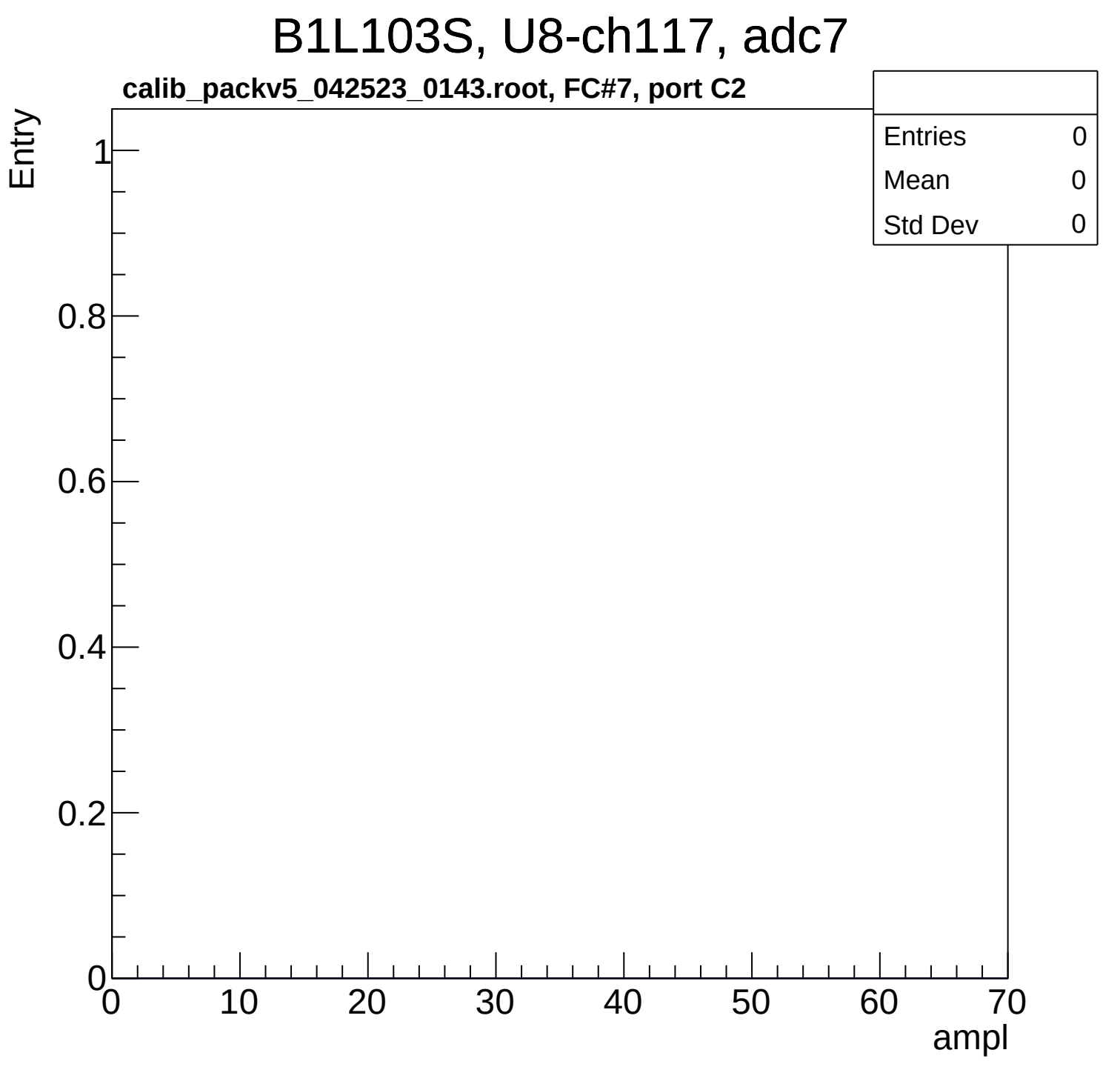

B1L103S, U8-ch117, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 42.53
Std Dev 3.821
Gaus mean : 42.7104
Gaus Width: 3.4086
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

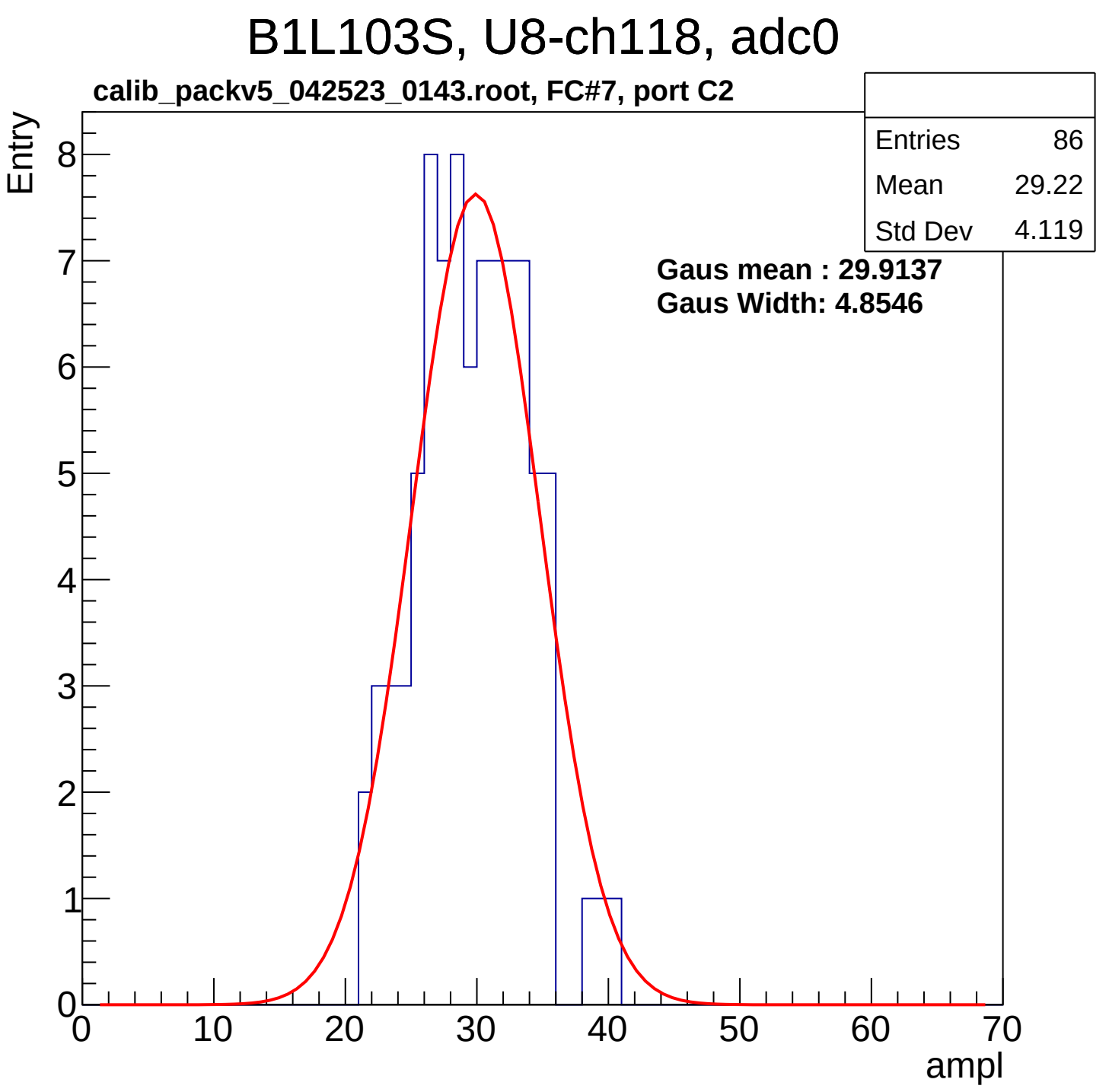

B1L103S, U8-ch117, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 49.12
Std Dev 3.963
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

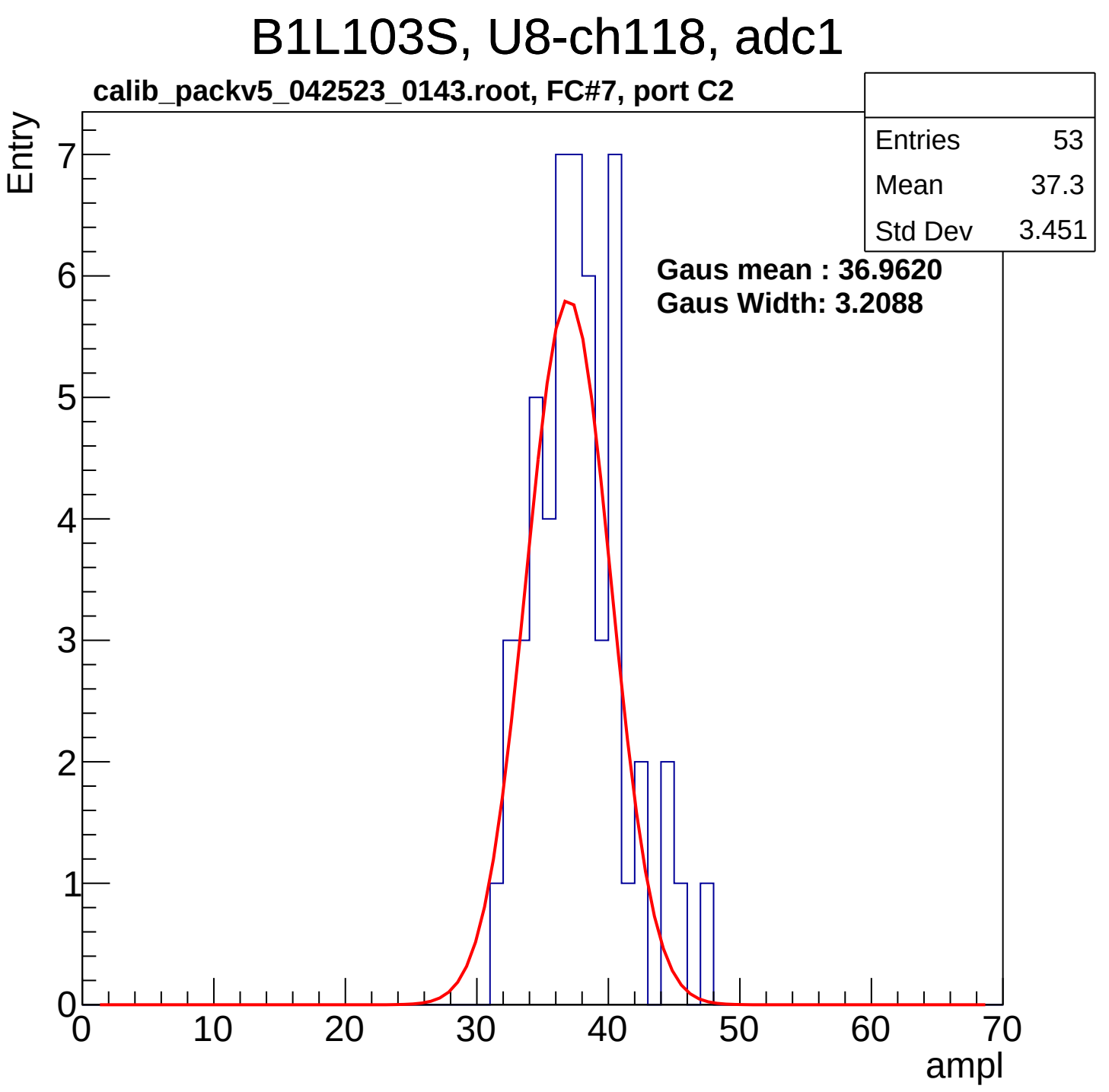

B1L103S, U8-ch117, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 54.48
Std Dev 3.317
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

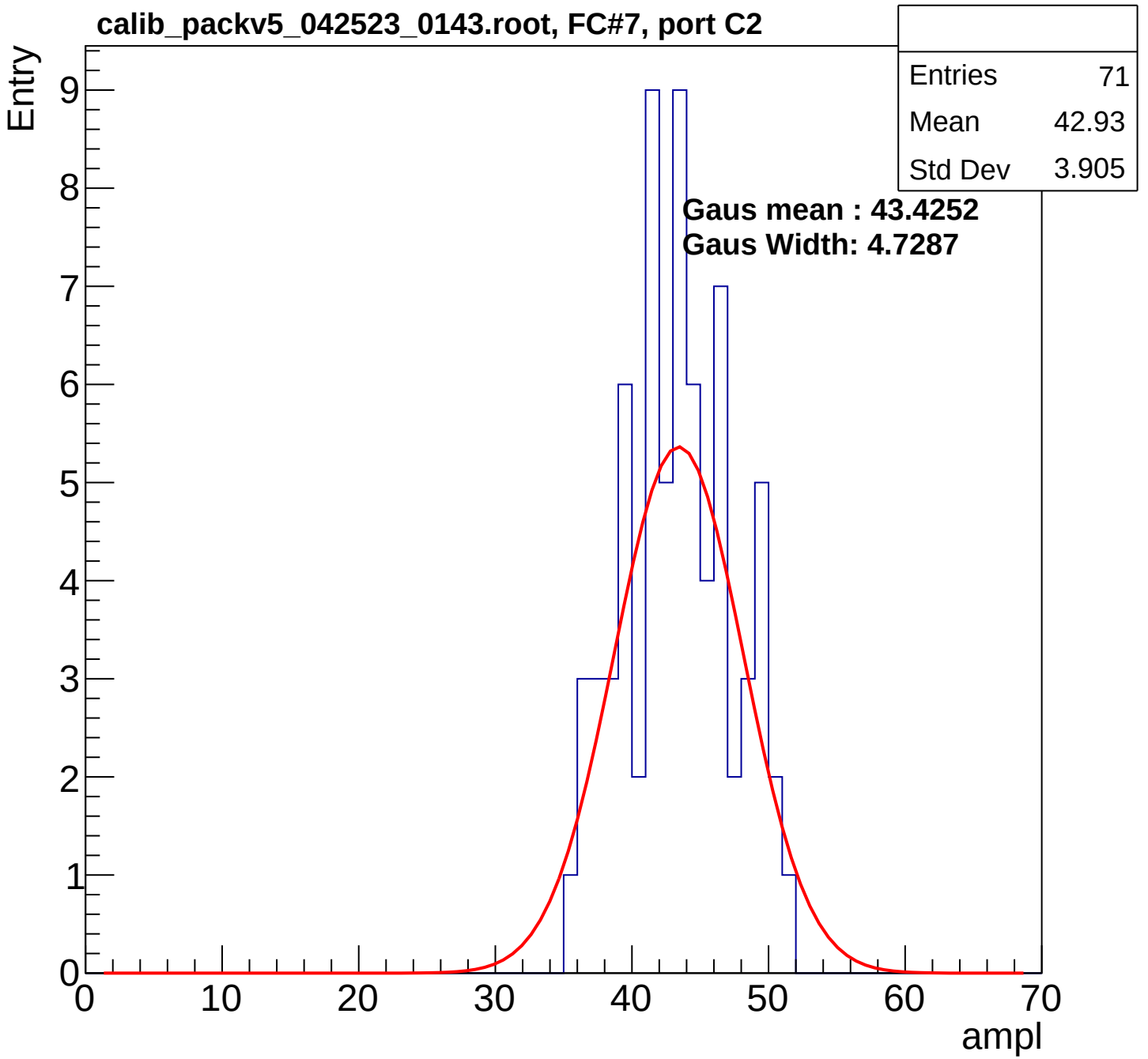

B1L103S, U8-ch117, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 48
Mean 58.48
Std Dev 8.886
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

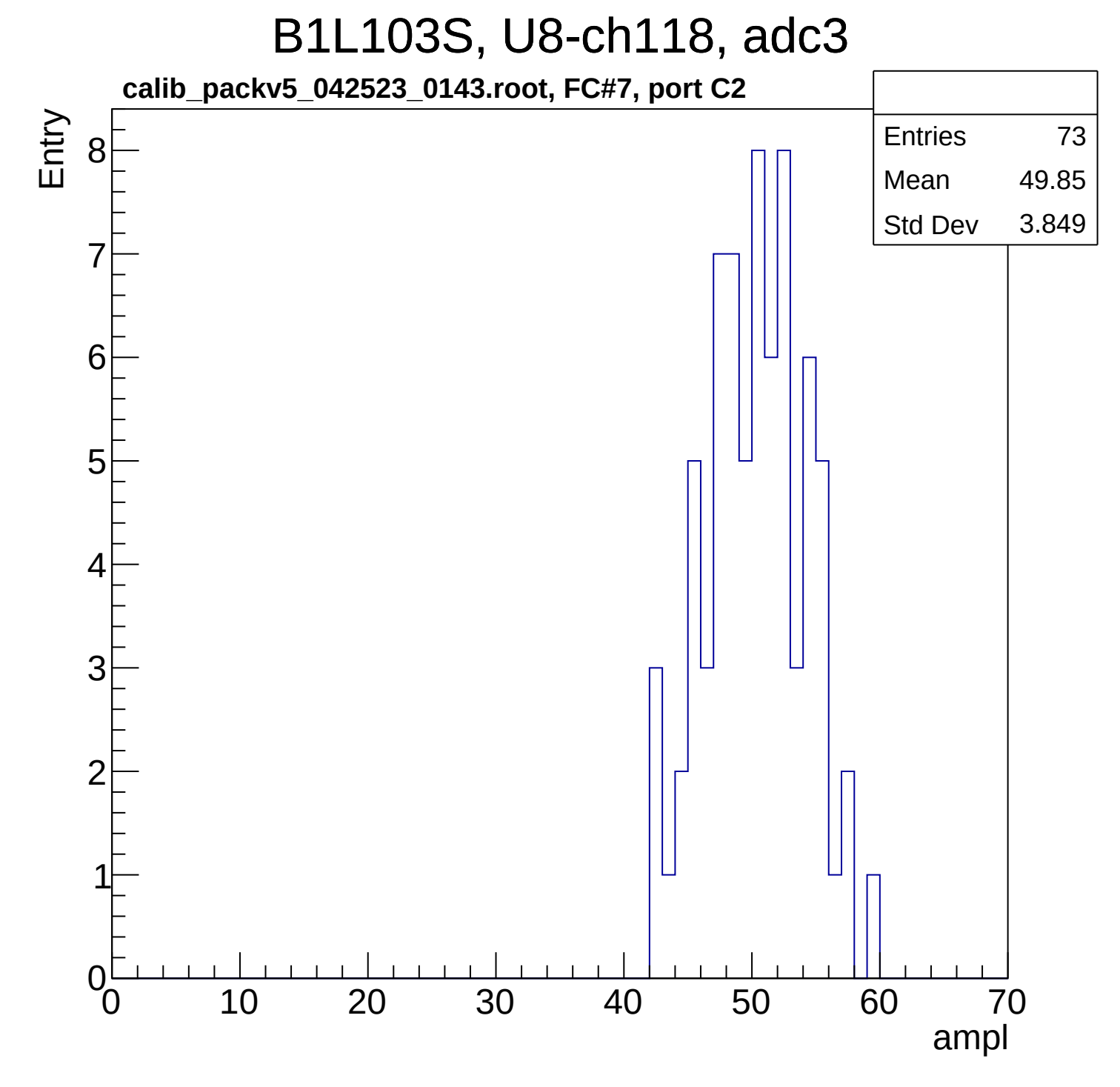

B1L103S, U8-ch117, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 10
Mean 61.6
Std Dev 0.9165
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

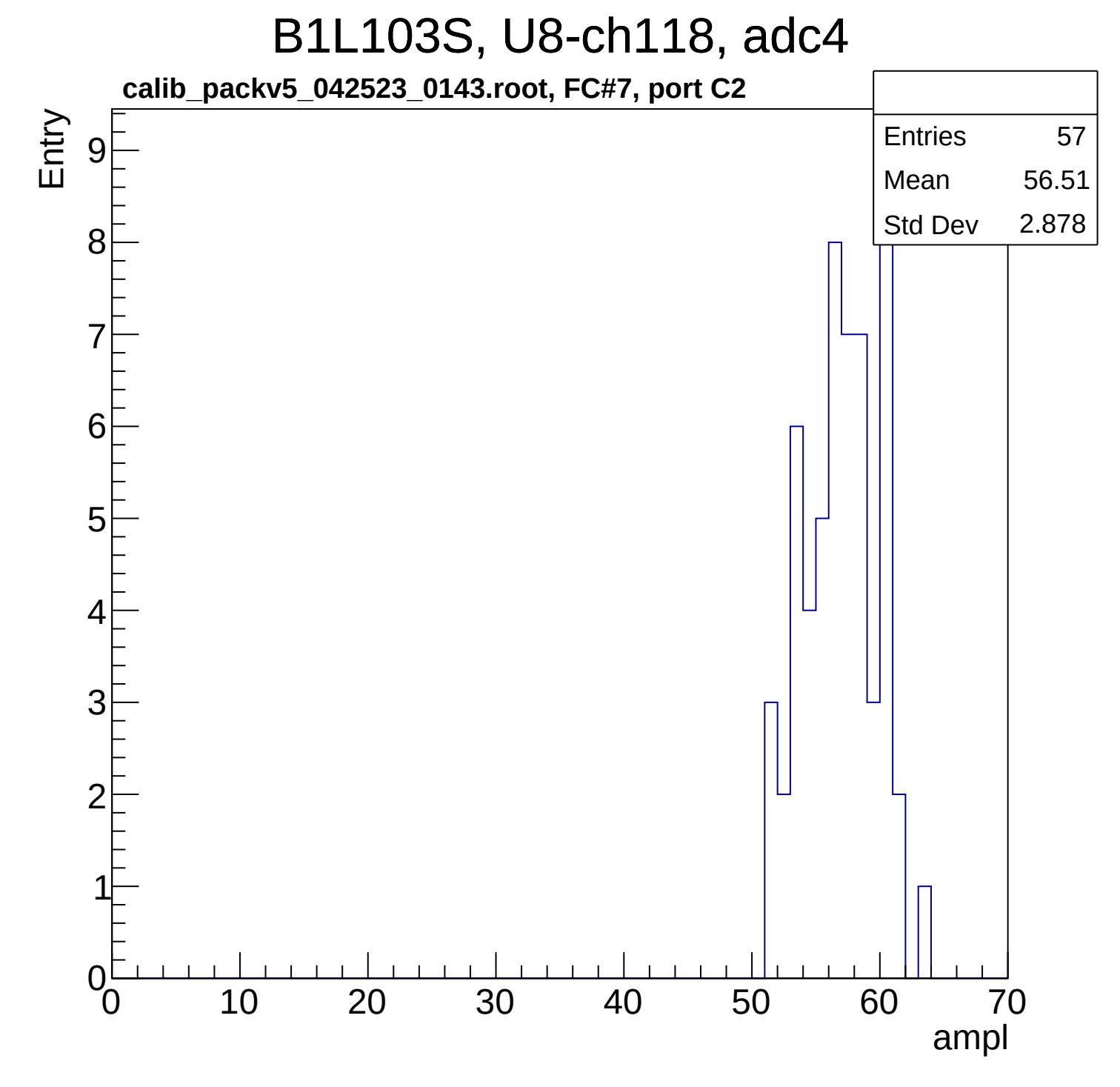

B1L103S, U8-ch117, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

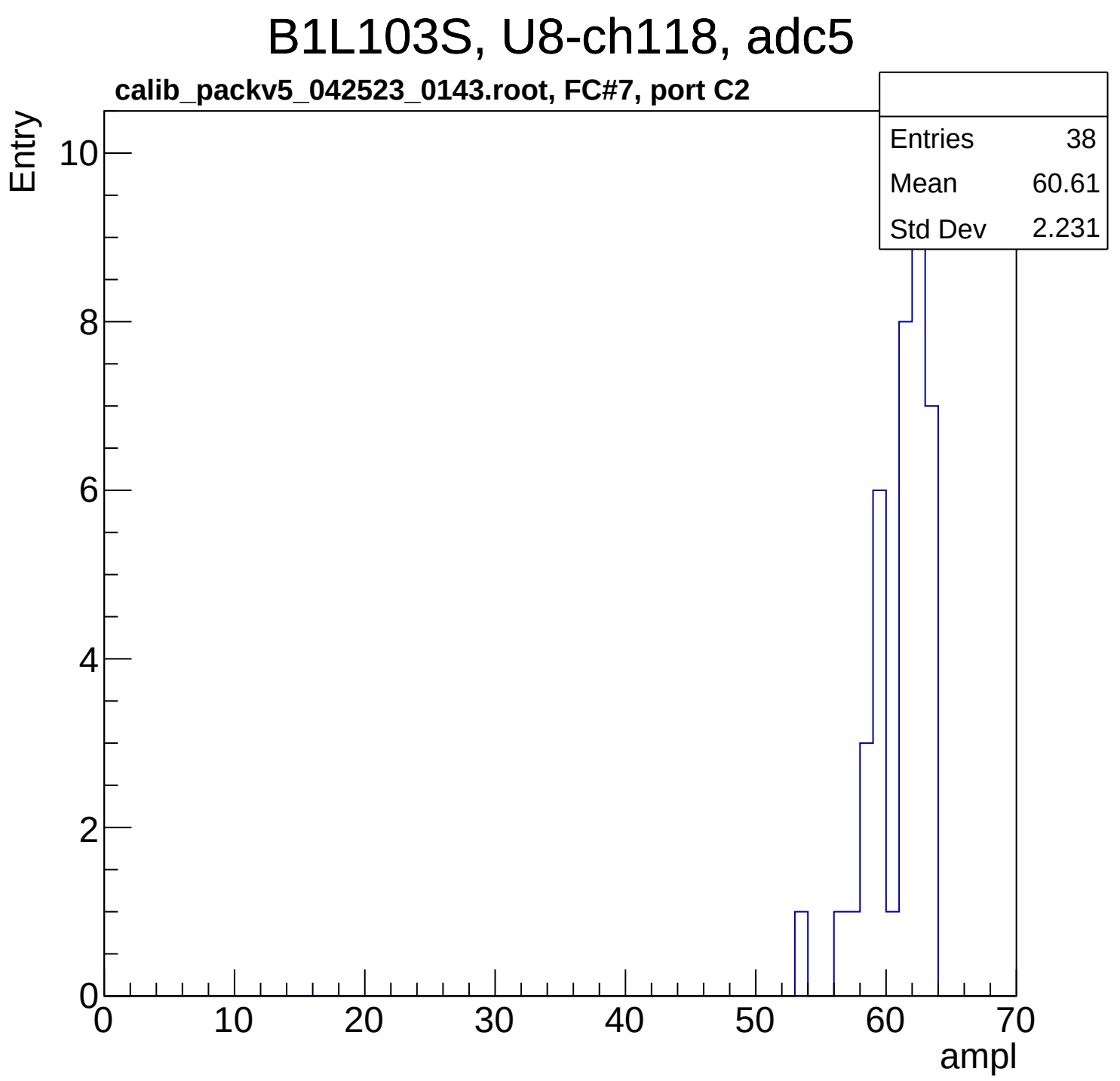

B1L103S, U8-ch118, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 86
Mean 29.22
Std Dev 4.119
Gaus mean : 29.9137
Gaus Width: 4.8546
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

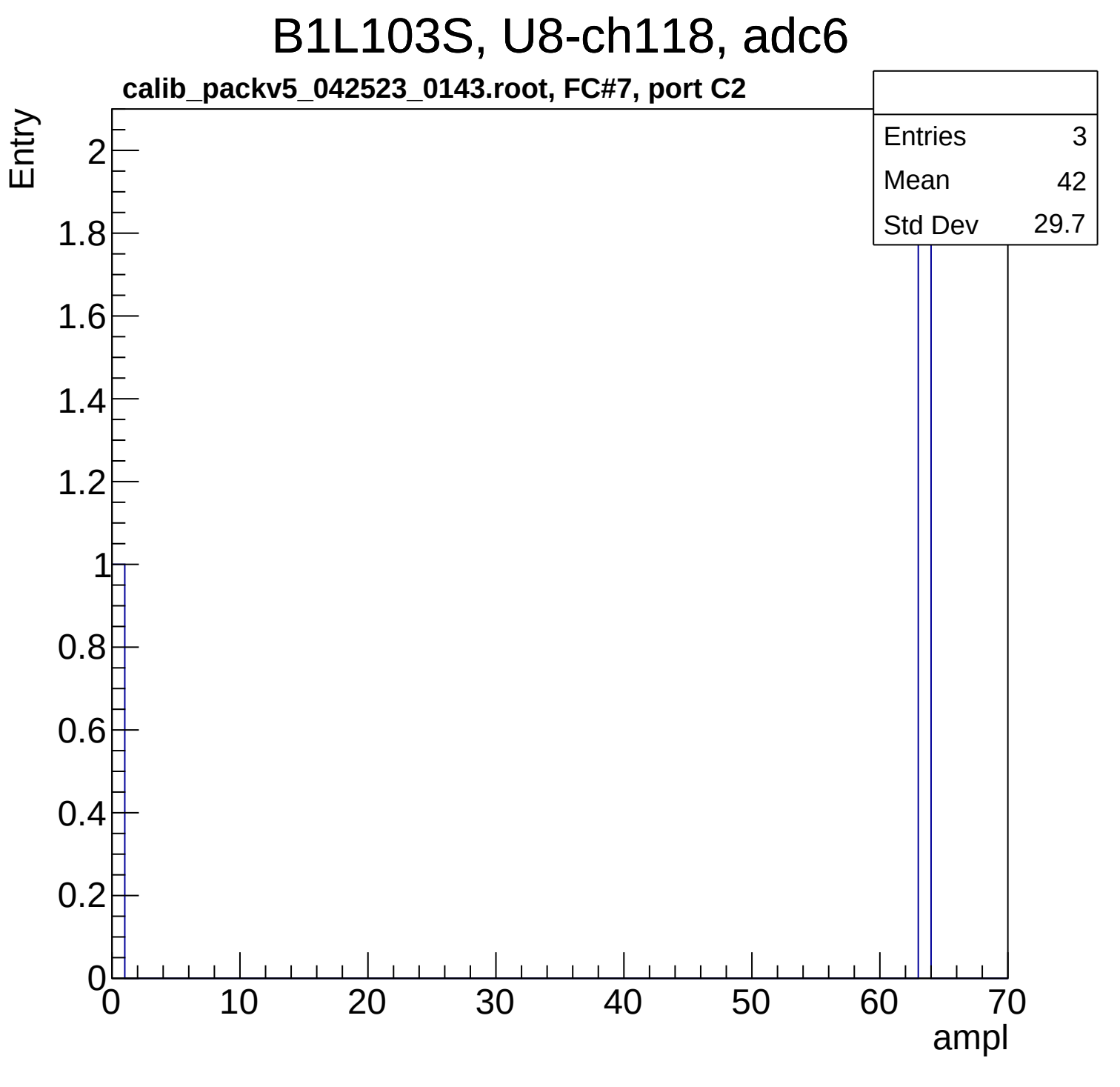

B1L103S, U8-ch118, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 37.3
Std Dev 3.451
Gaus mean : 36.9620
Gaus Width: 3.2088
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

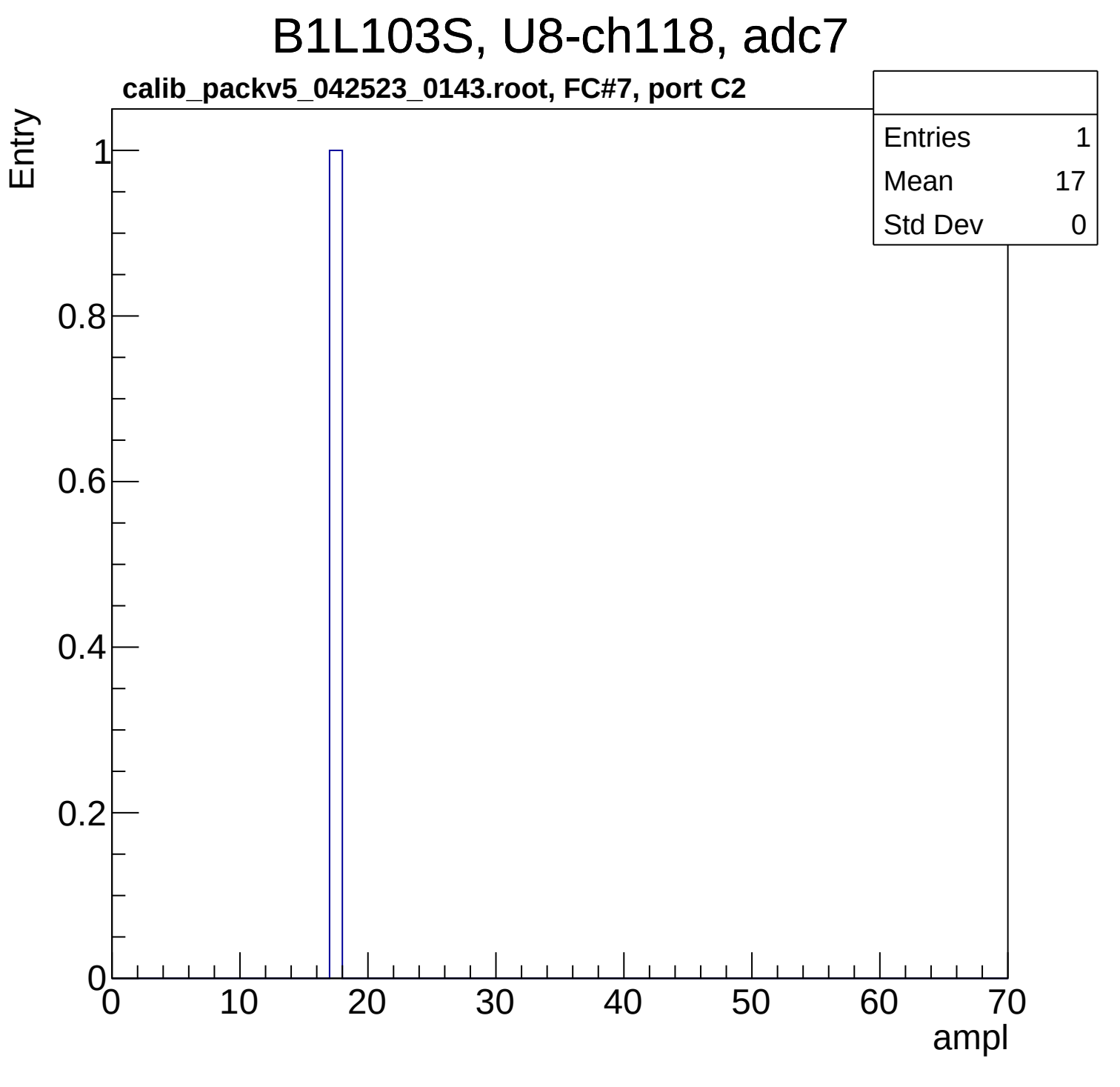

B1L103S, U8-ch118, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 71
Mean 42.93
Std Dev 3.905
Gaus mean : 43.4252
Gaus Width: 4.7287
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

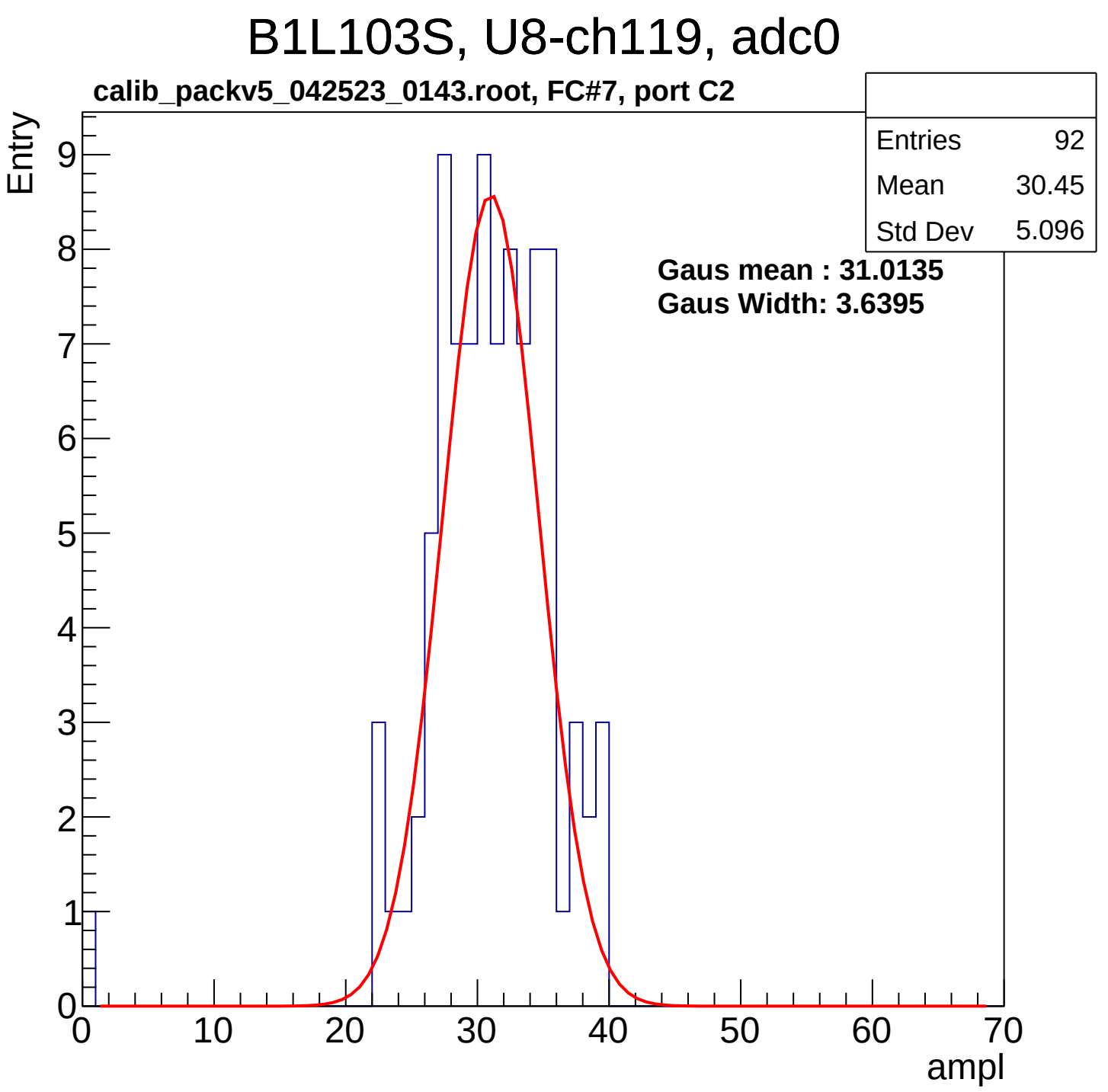

B1L103S, U8-ch118, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 49.85
Std Dev 3.849
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

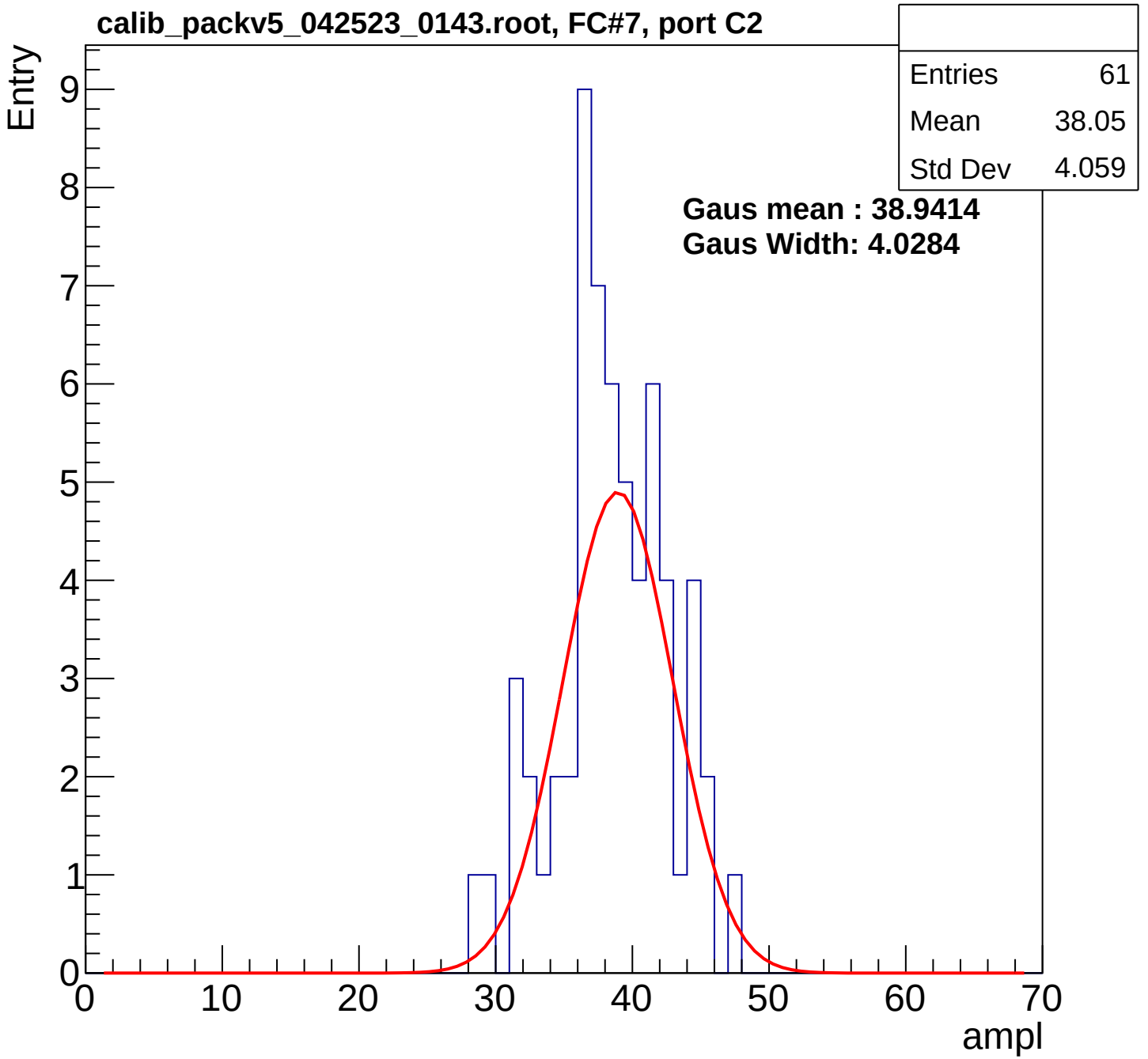

B1L103S, U8-ch118, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 56.51
Std Dev 2.878
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

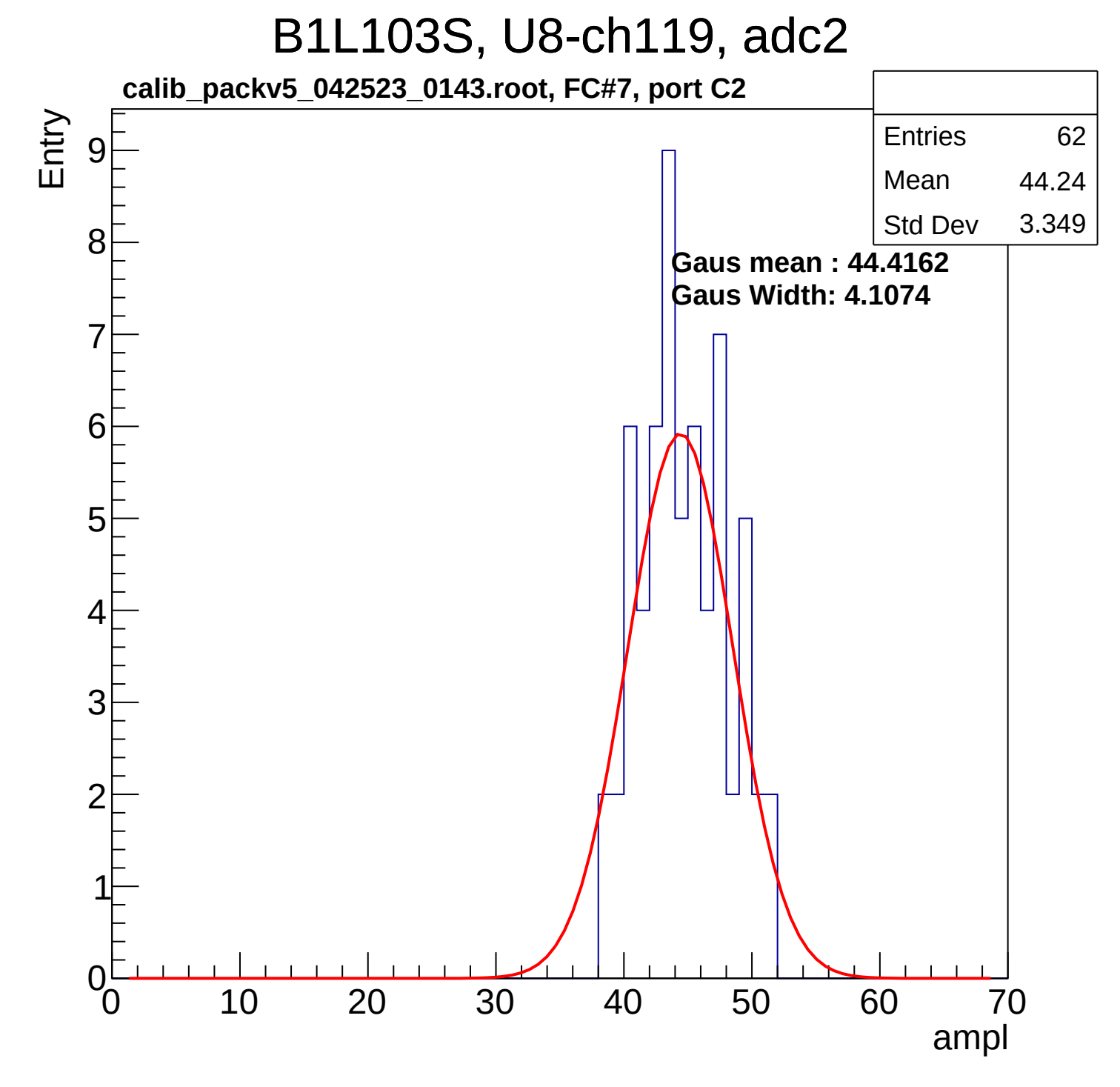

B1L103S, U8-ch118, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 38
Mean 60.61
Std Dev 2.231
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

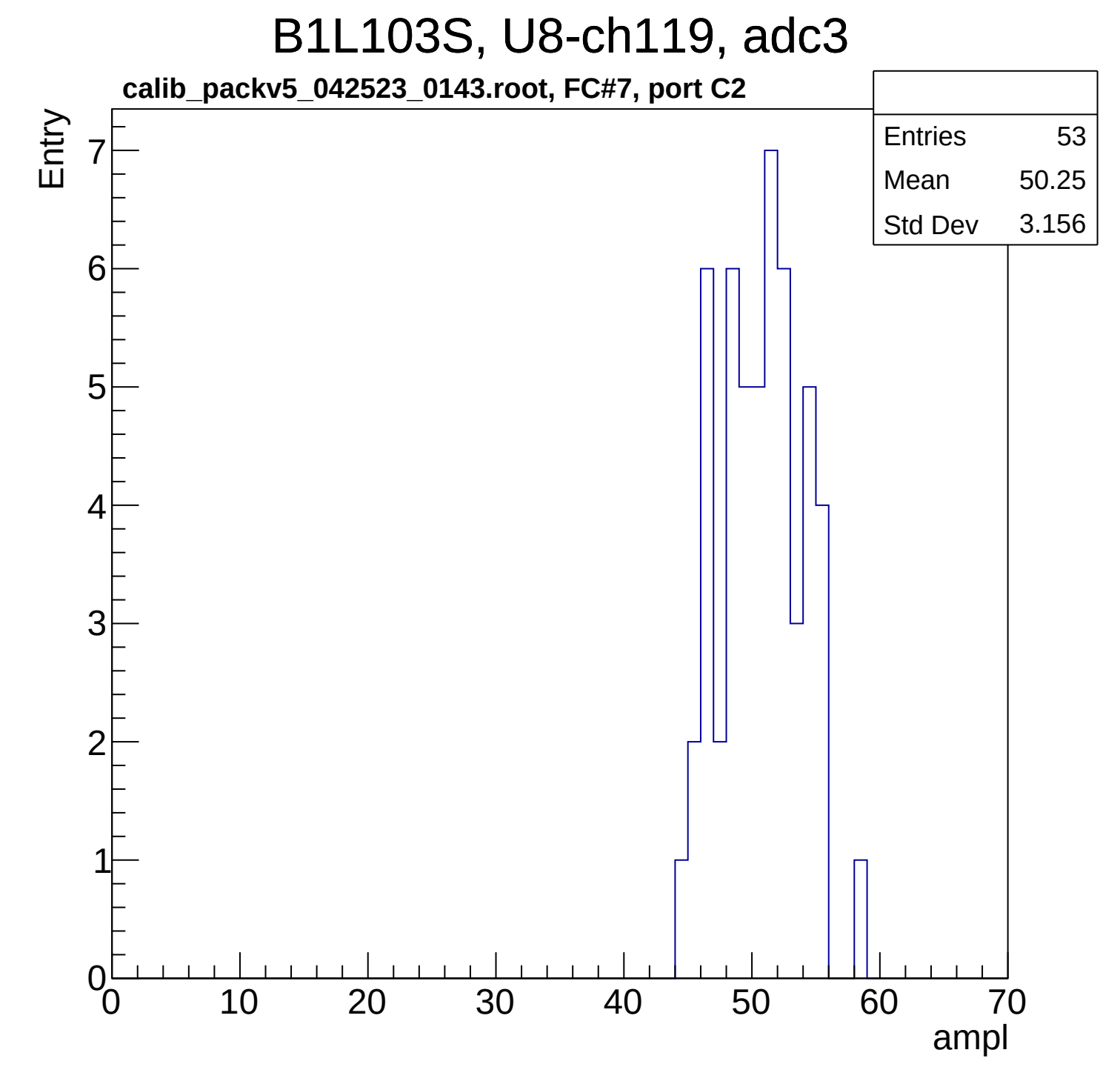

B1L103S, U8-ch118, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 42
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

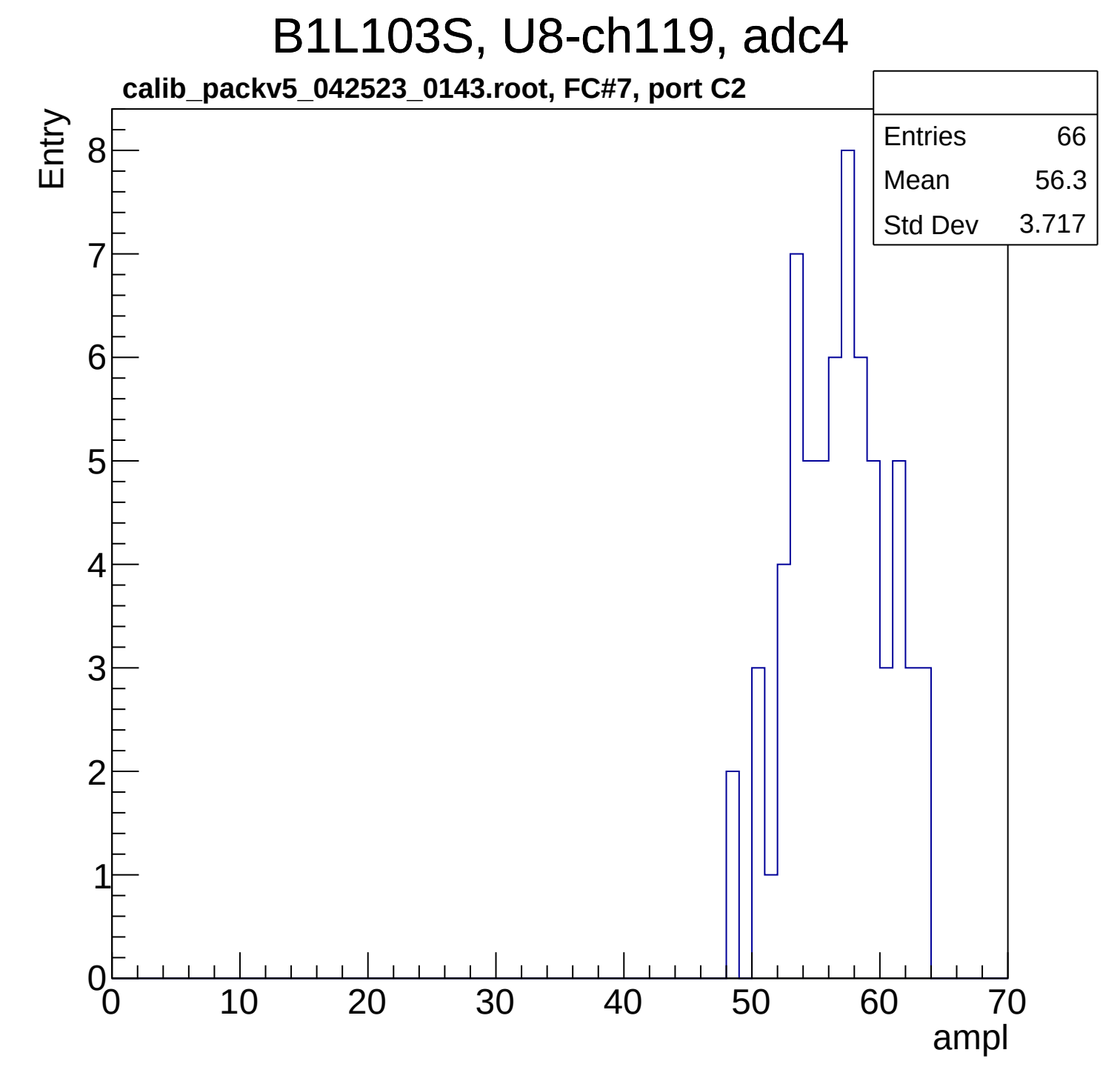

B1L103S, U8-ch118, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 17
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

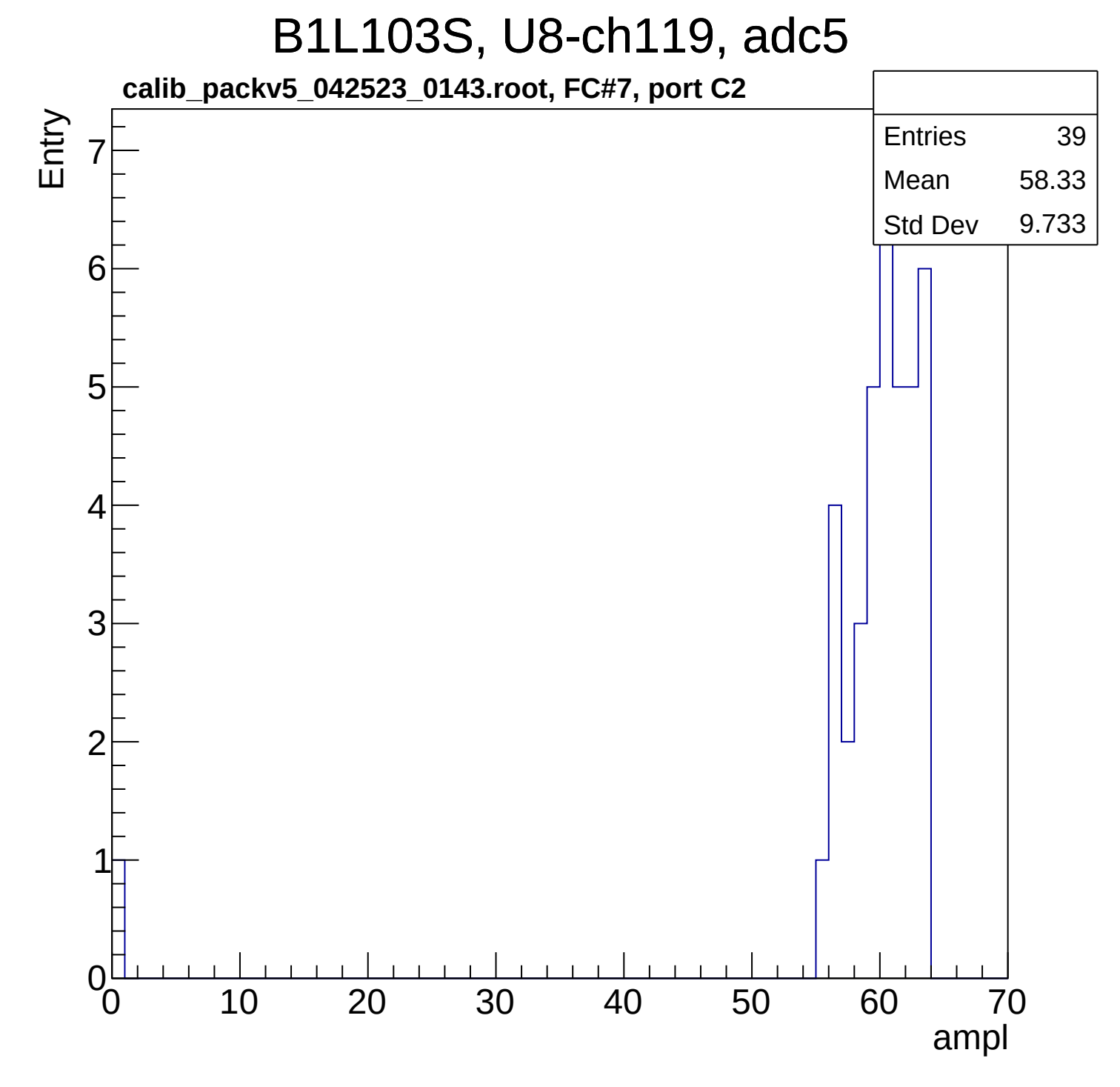

B1L103S, U8-ch119, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 92
Mean 30.45
Std Dev 5.096
Gaus mean : 31.0135
Gaus Width: 3.6395
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

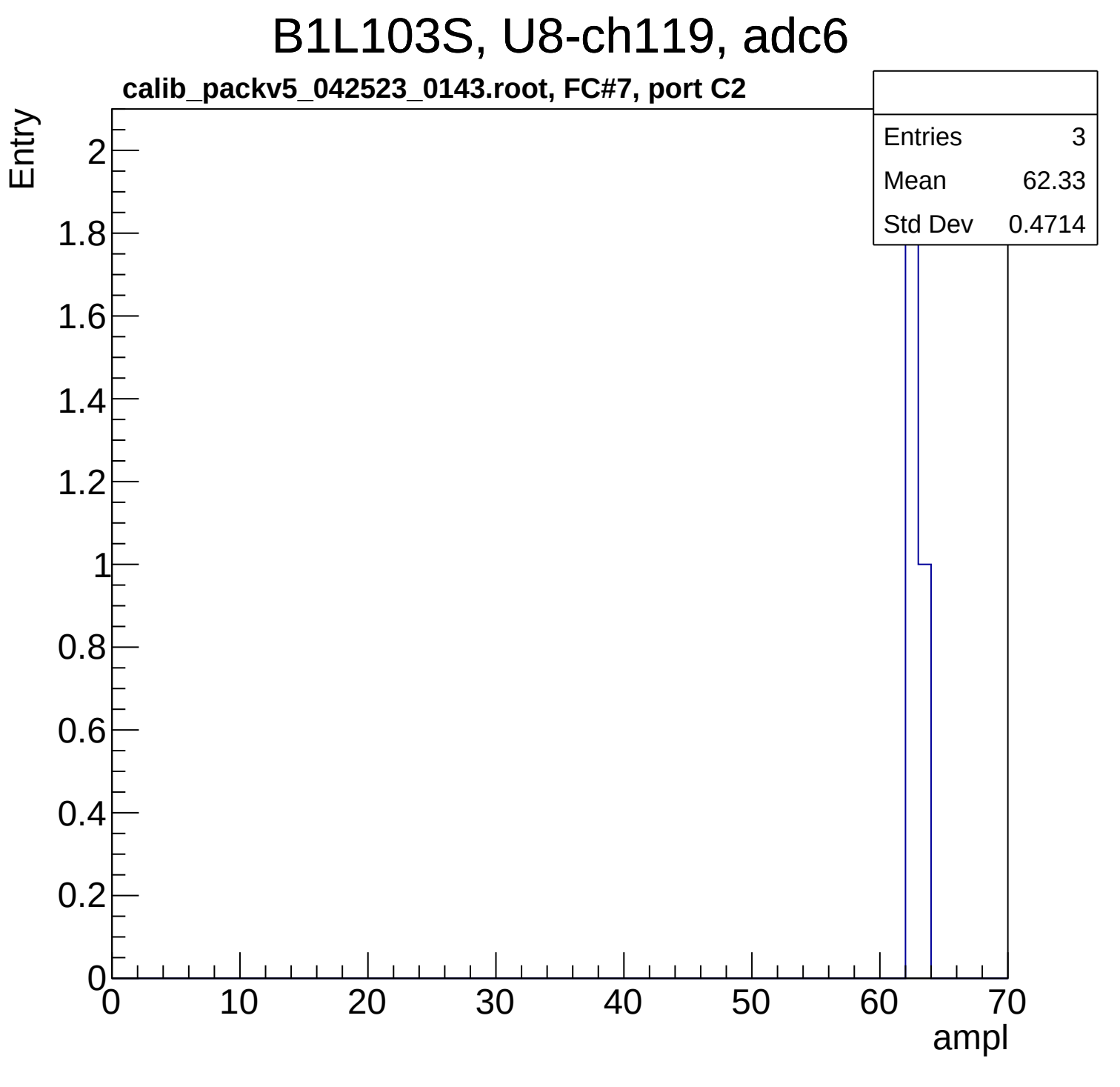

B1L103S, U8-ch119, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 61
Mean 38.05
Std Dev 4.059
Gaus mean : 38.9414
Gaus Width: 4.0284
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

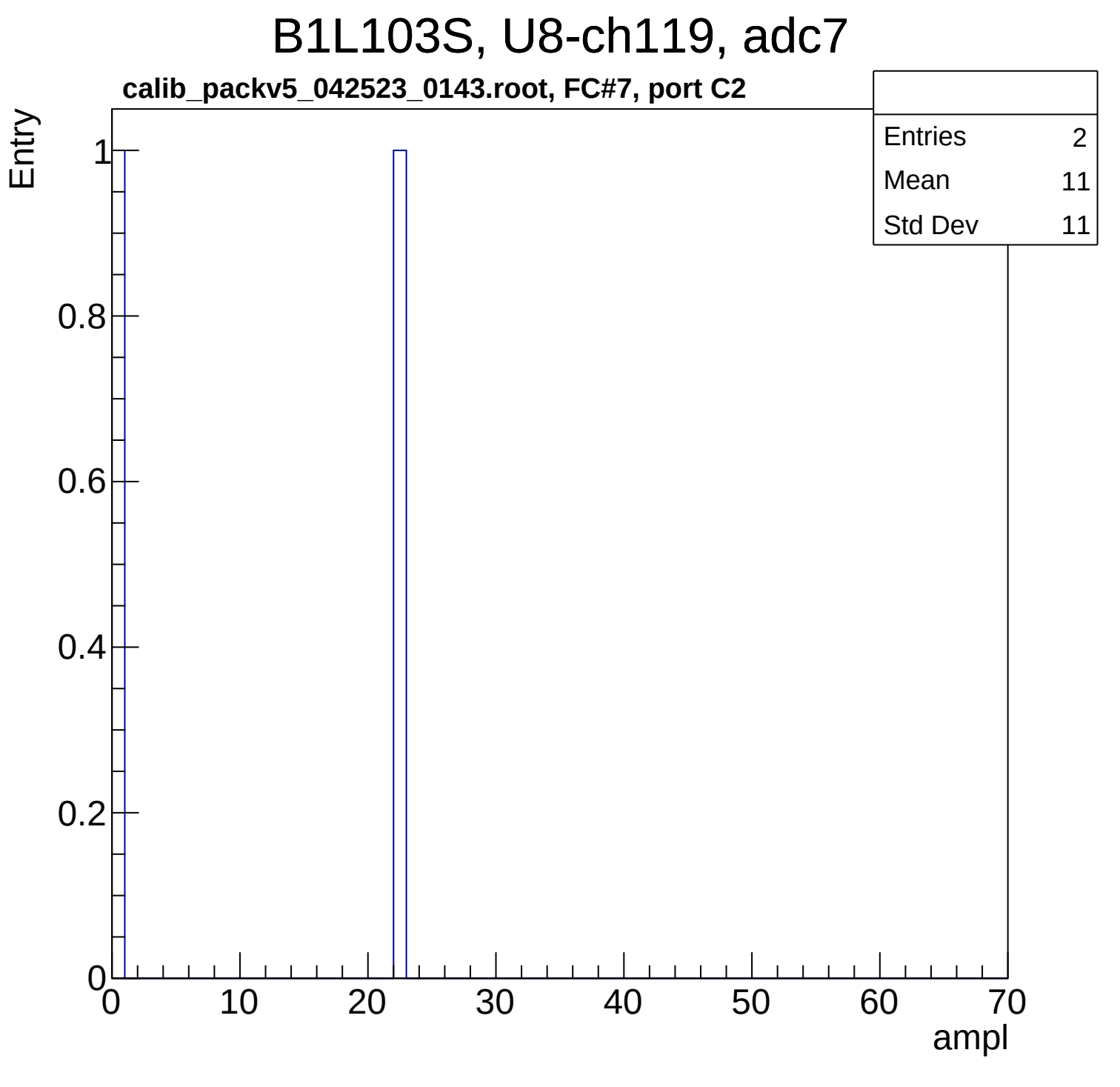

B1L103S, U8-ch119, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 44.24
Std Dev 3.349
Gaus mean : 44.4162
Gaus Width: 4.1074
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

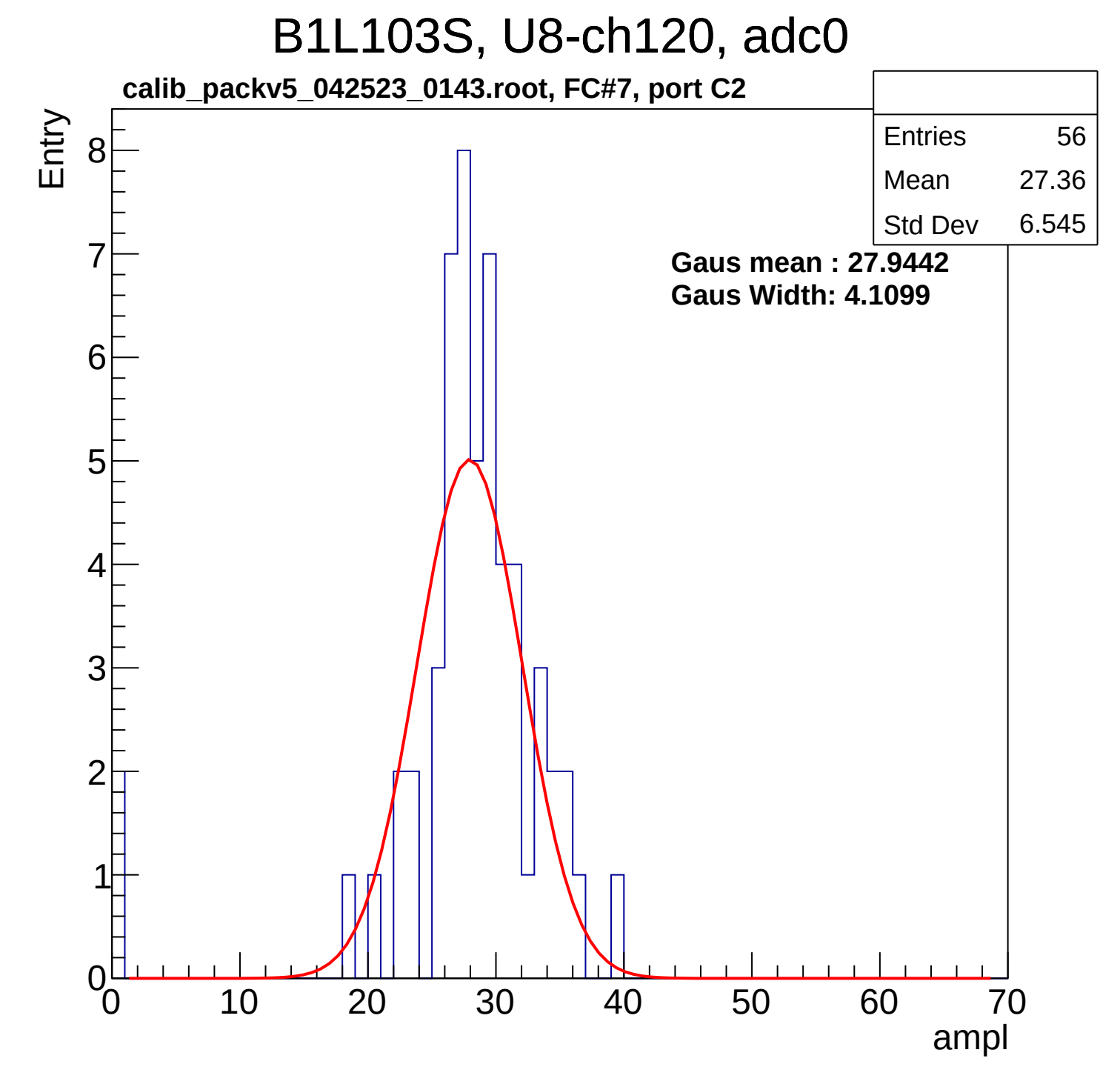

B1L103S, U8-ch119, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 53
Mean 50.25
Std Dev 3.156
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

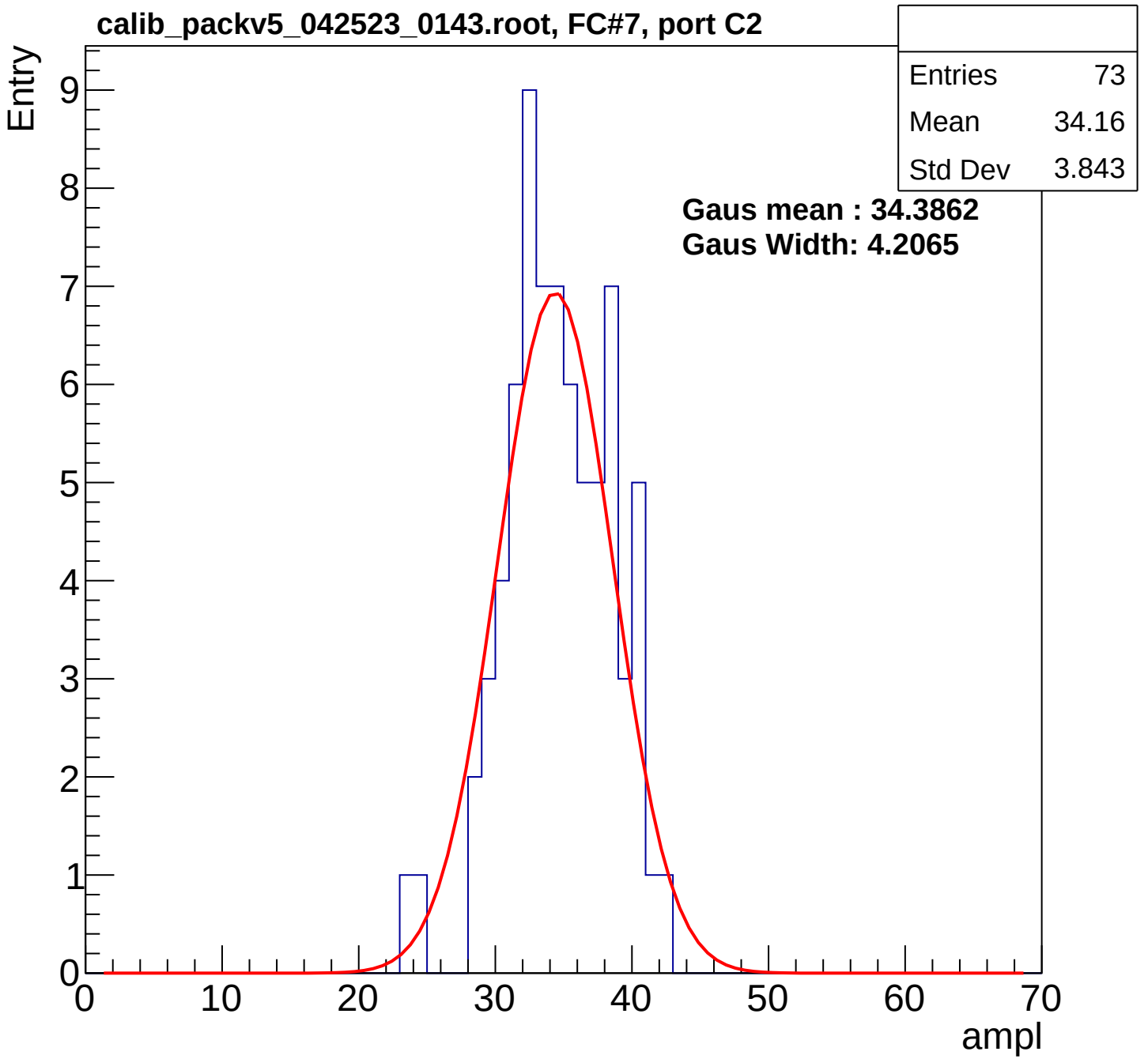

B1L103S, U8-ch119, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 56.3
Std Dev 3.717
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

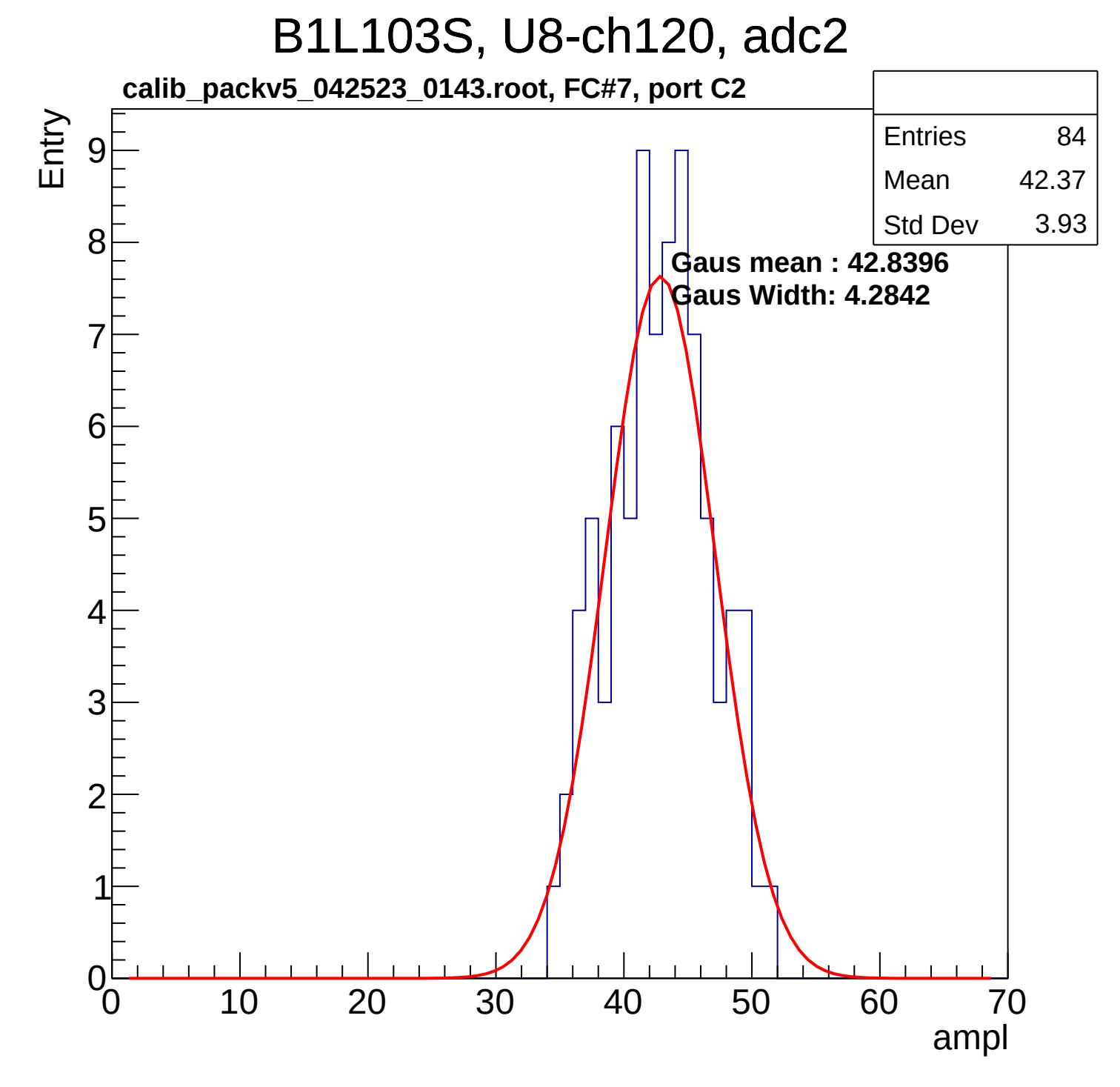

B1L103S, U8-ch119, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 39
Mean 58.33
Std Dev 9.733
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

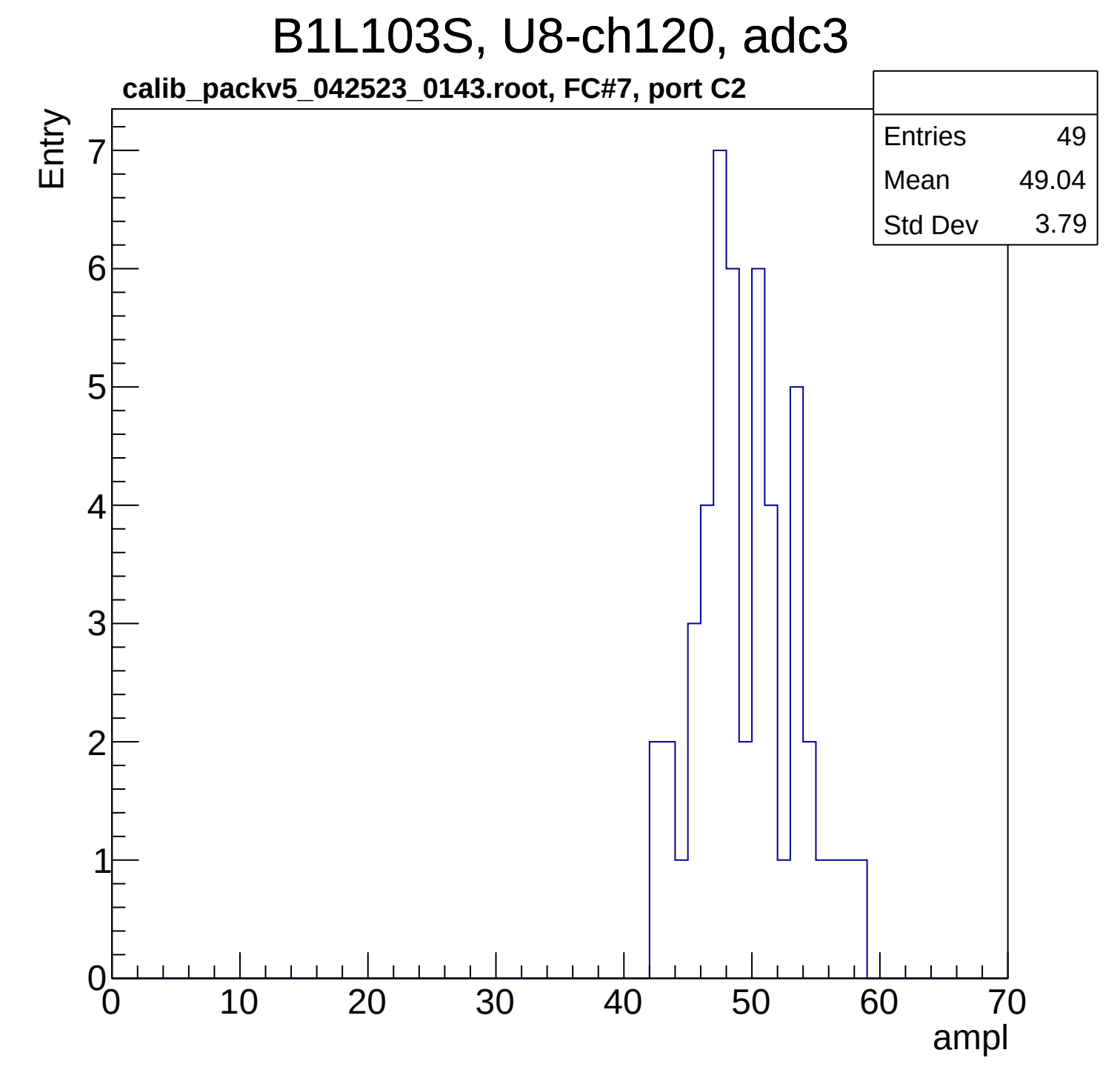

B1L103S, U8-ch119, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

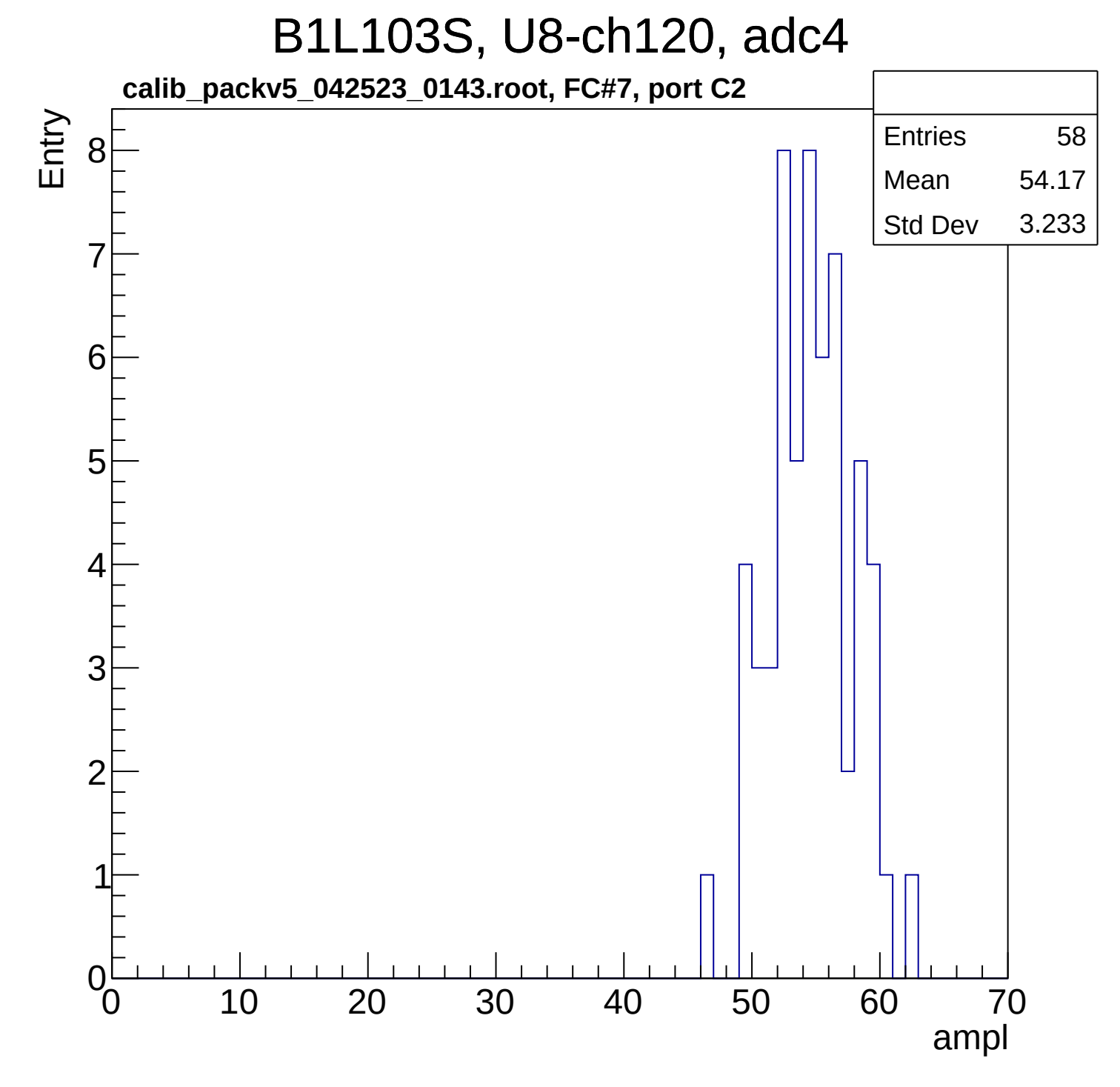

B1L103S, U8-ch119, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 11
Std Dev 11
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

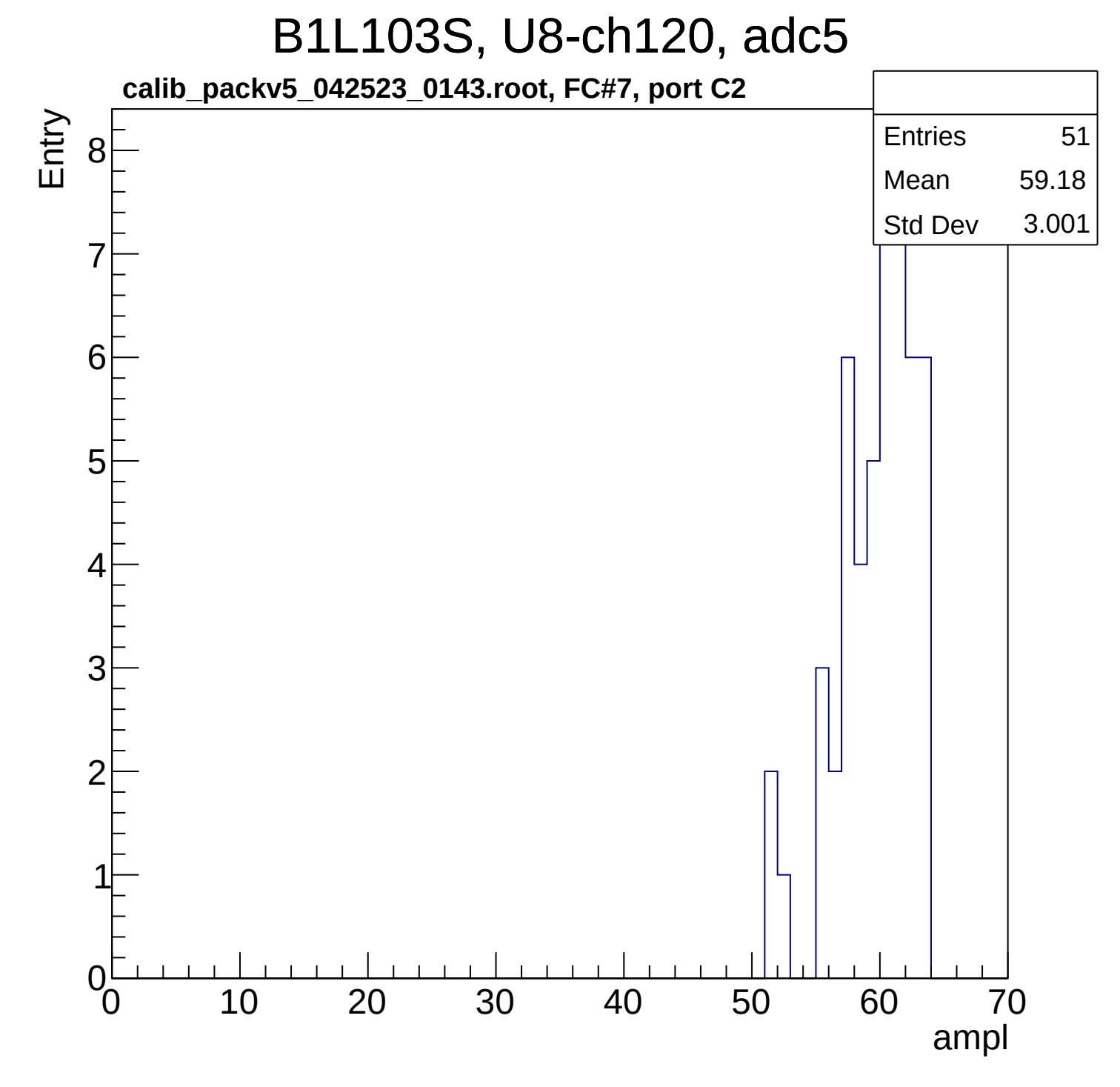

B1L103S, U8-ch120, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 56
Mean 27.36
Std Dev 6.545
Gaus mean : 27.9442
Gaus Width: 4.1099
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

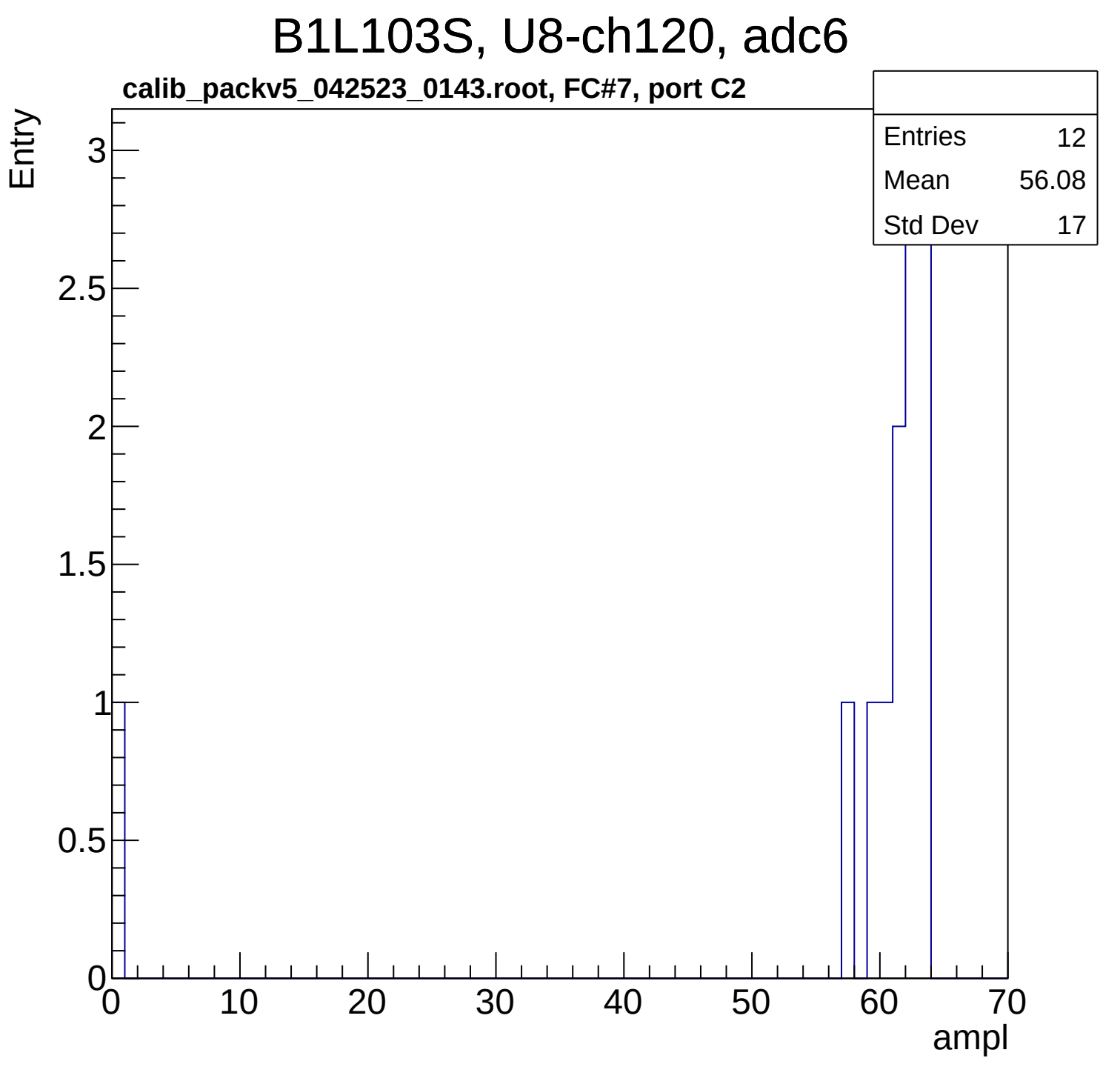

B1L103S, U8-ch120, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 73
Mean 34.16
Std Dev 3.843
Gaus mean : 34.3862
Gaus Width: 4.2065
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

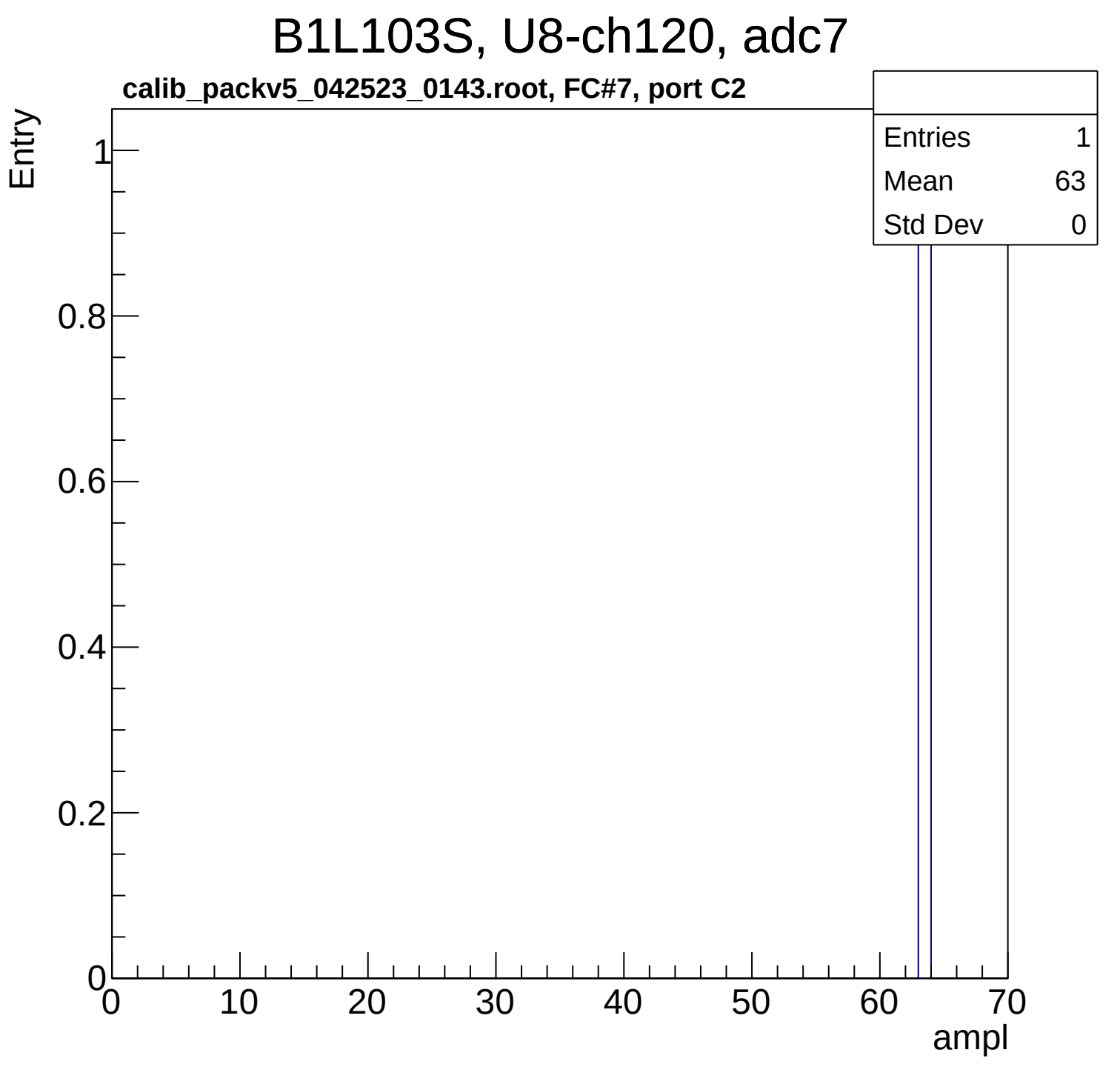

B1L103S, U8-ch120, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 84
Mean 42.37
Std Dev 3.93
Gaus mean : 42.8396
Gaus Width: 4.2842
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

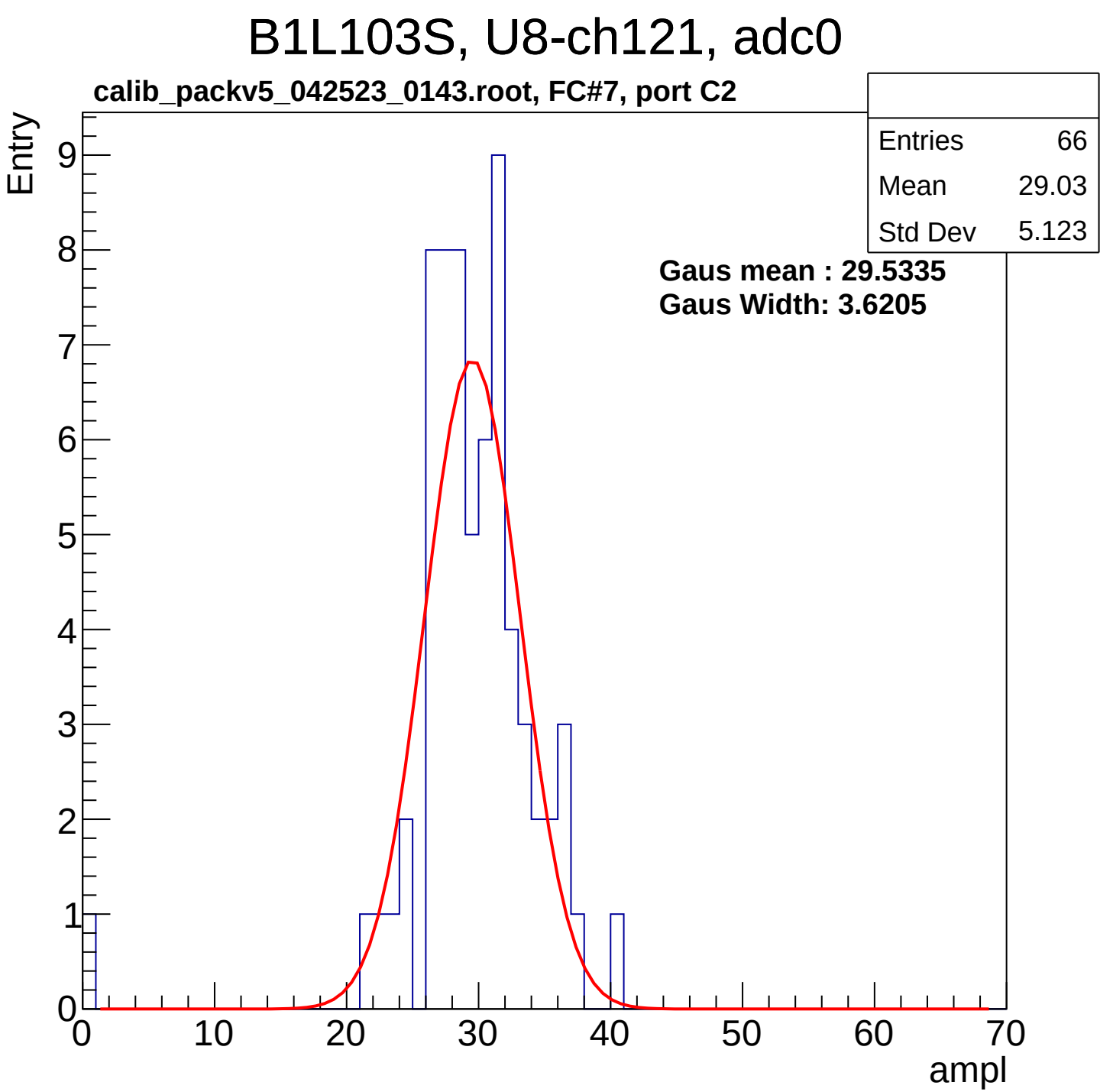

B1L103S, U8-ch120, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 49
Mean 49.04
Std Dev 3.79
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

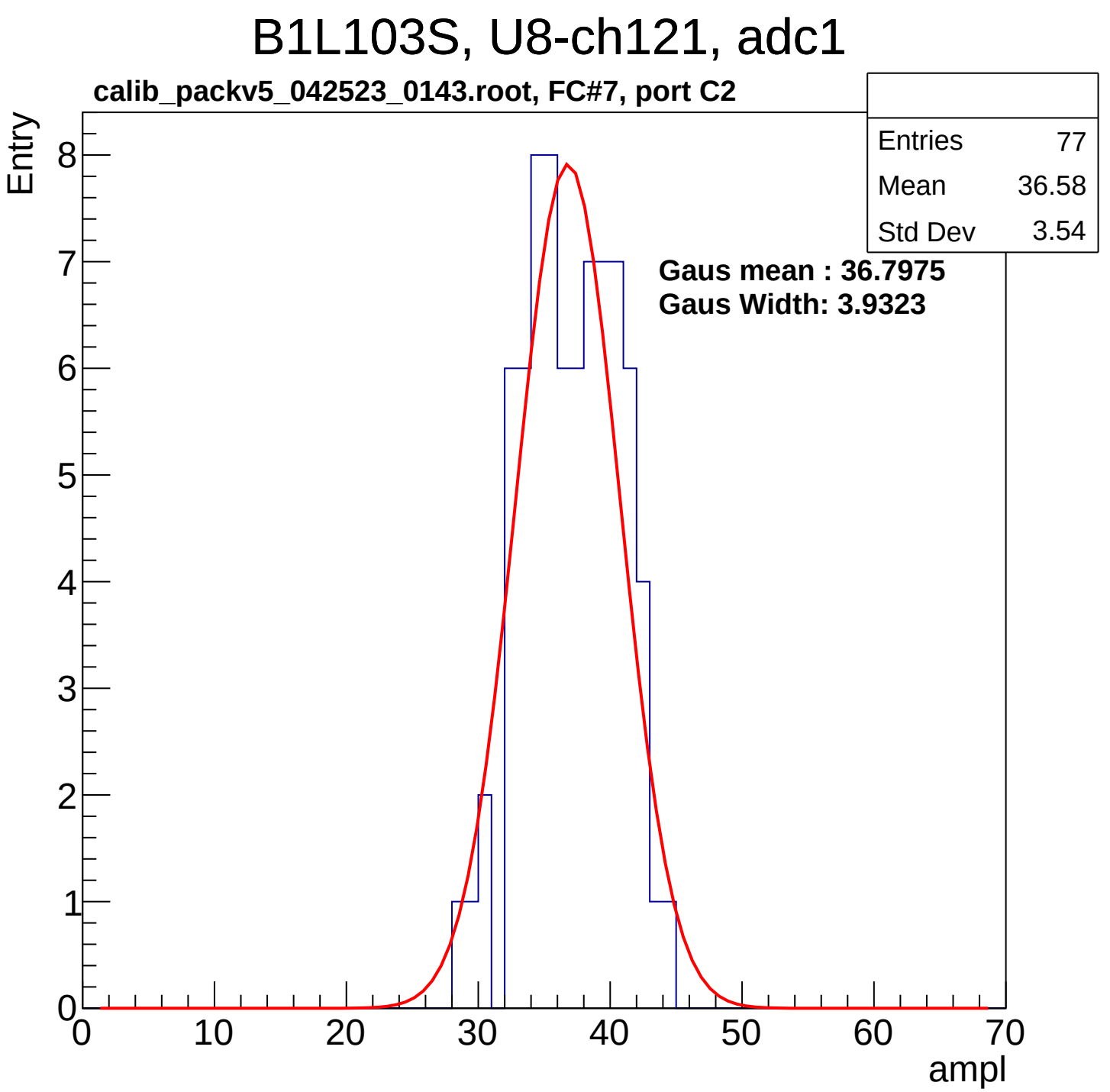

B1L103S, U8-ch120, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 54.17
Std Dev 3.233
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

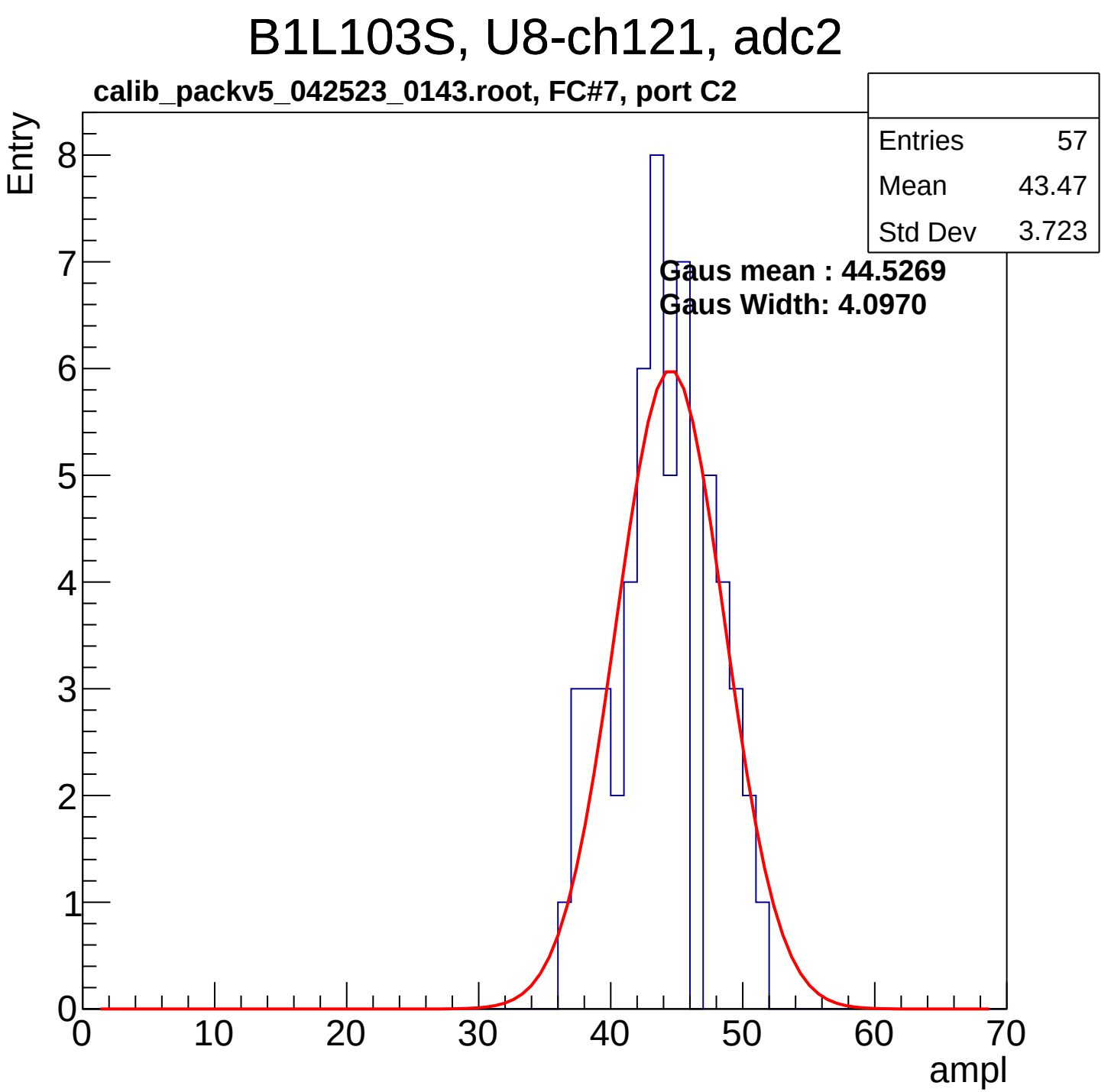

B1L103S, U8-ch120, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 59.18
Std Dev 3.001
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

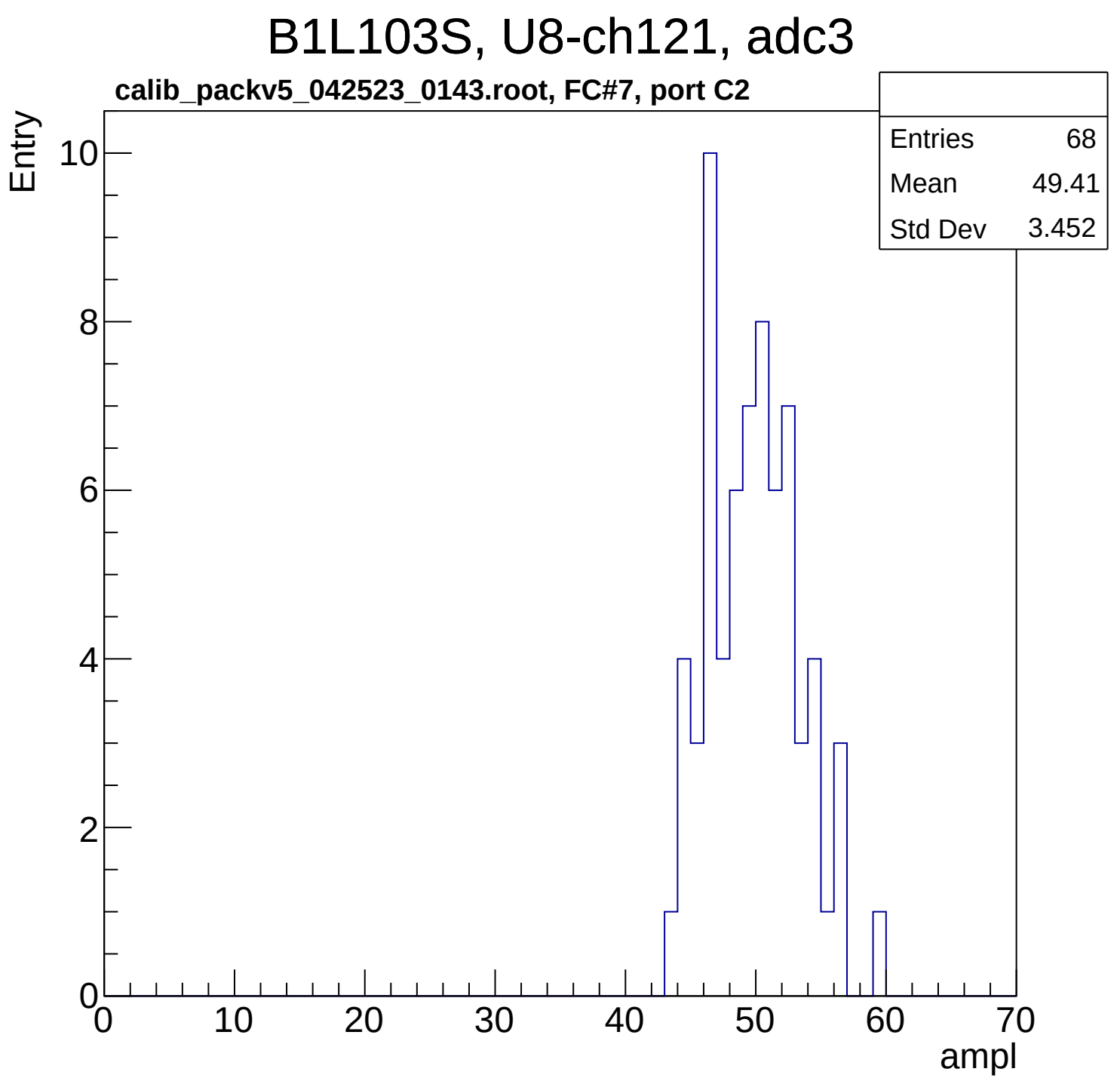

B1L103S, U8-ch120, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 12
Mean 56.08
Std Dev 17
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

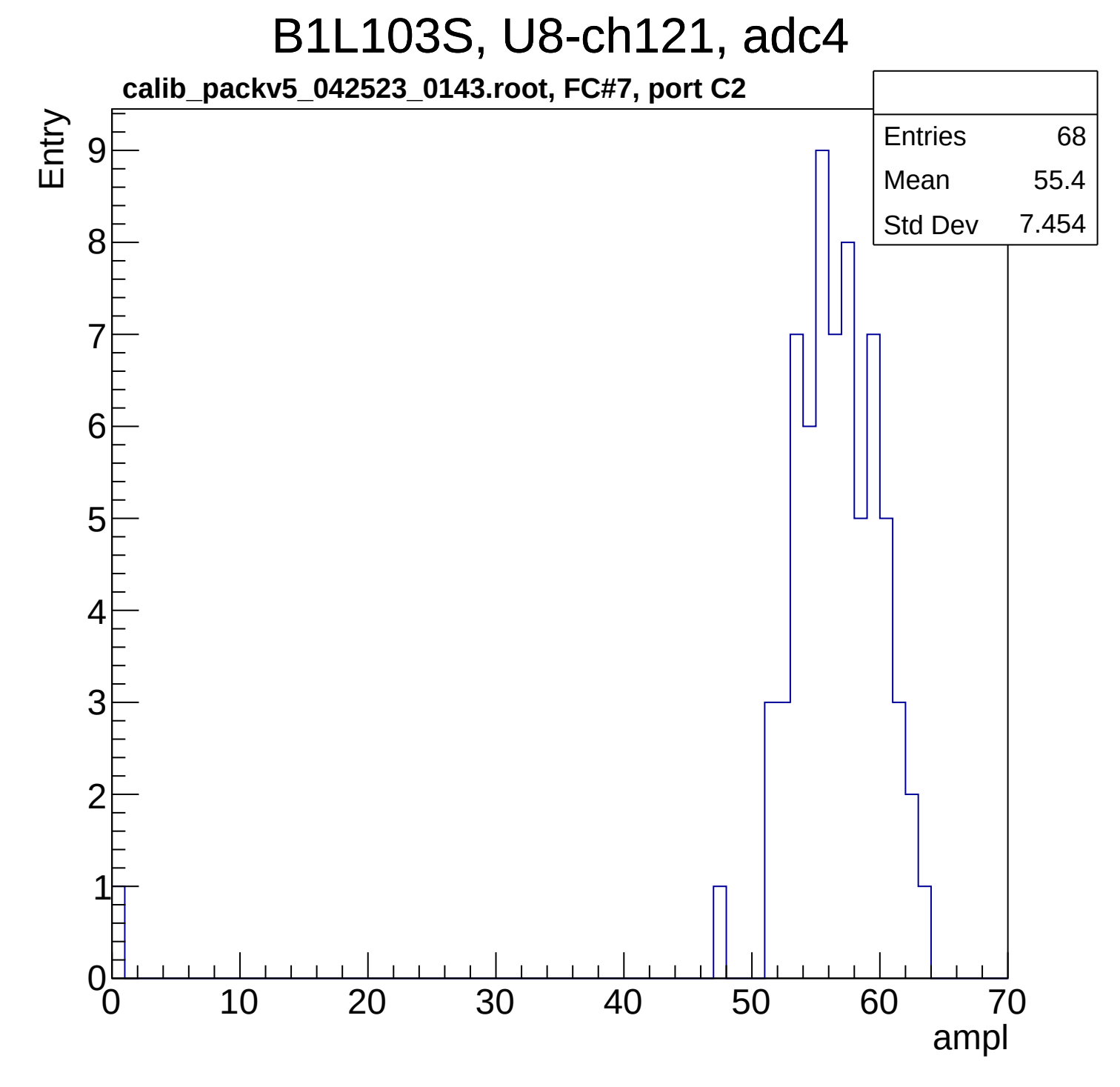

B1L103S, U8-ch120, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

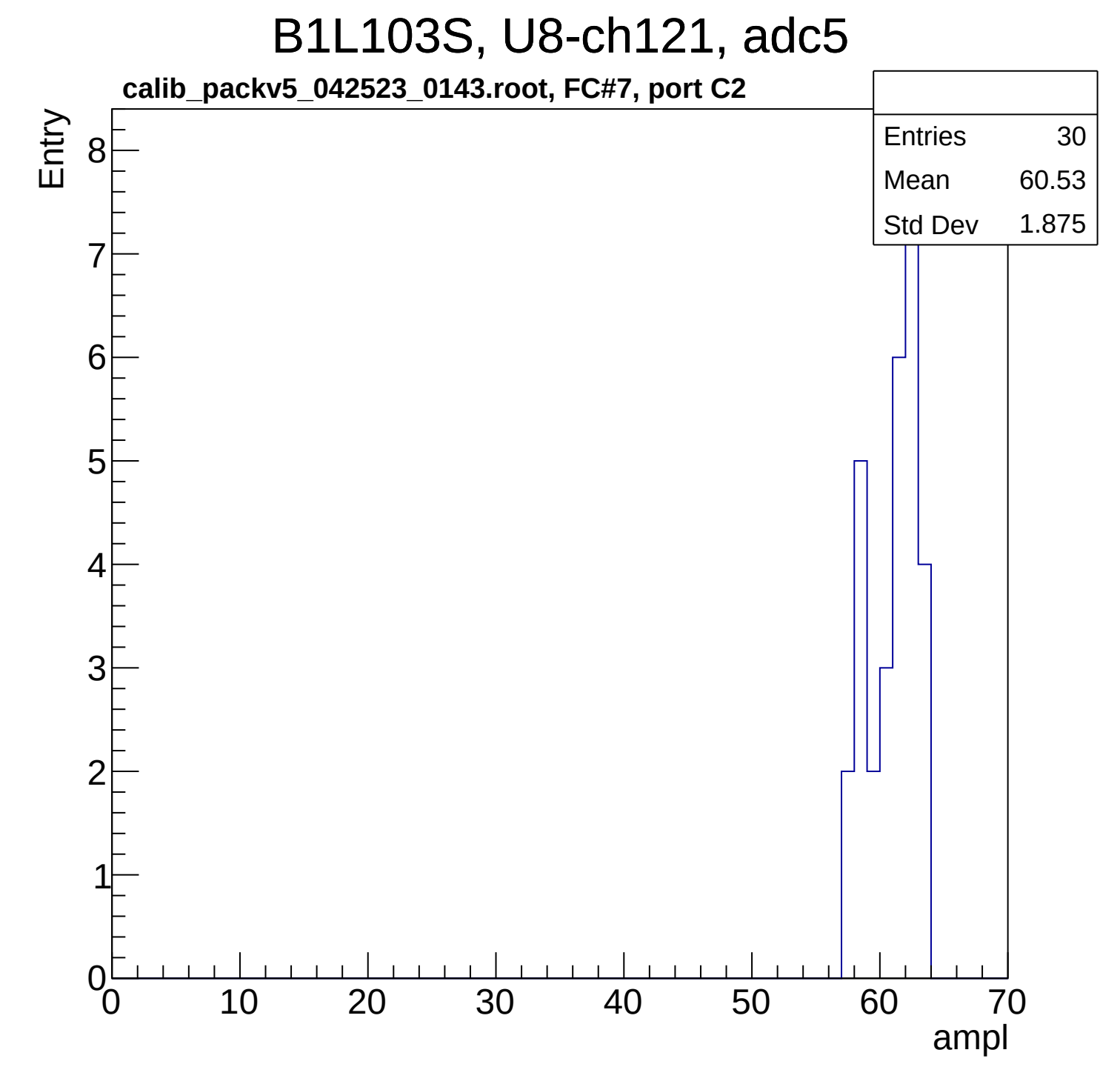

B1L103S, U8-ch121, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 29.03
Std Dev 5.123
Gaus mean : 29.5335
Gaus Width: 3.6205
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

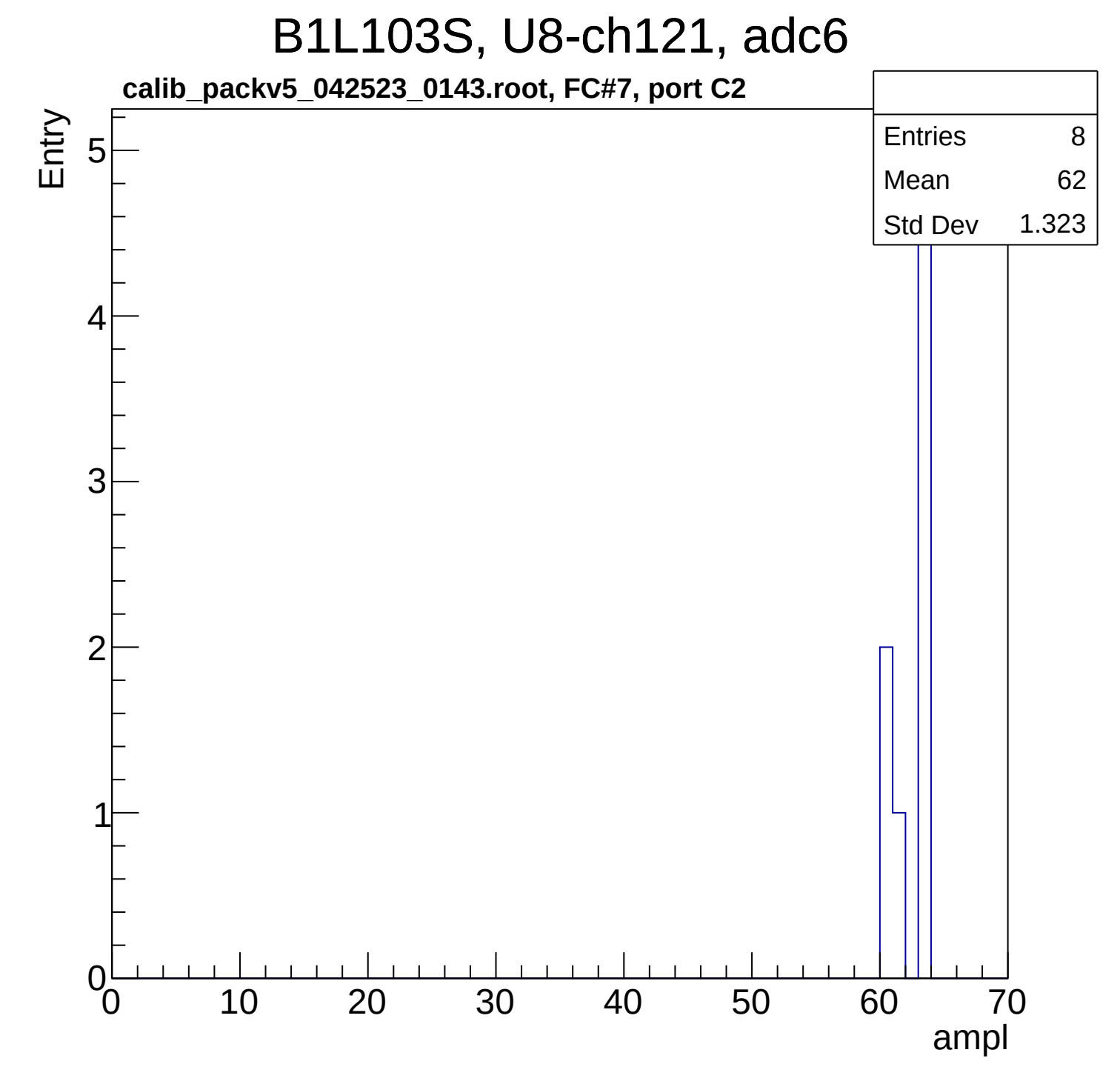

B1L103S, U8-ch121, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 36.58
Std Dev 3.54
Gaus mean : 36.7975
Gaus Width: 3.9323
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

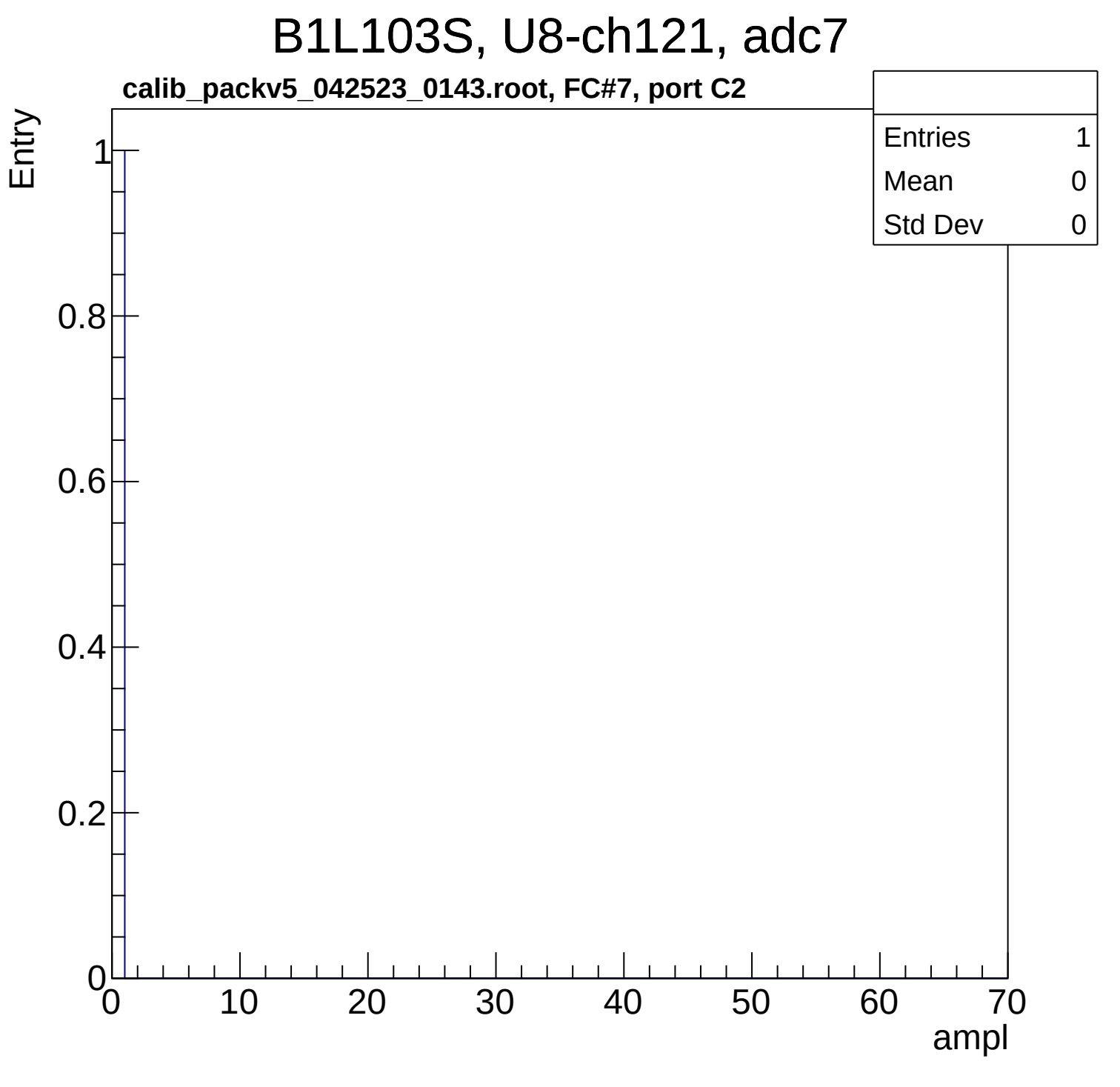

B1L103S, U8-ch121, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 43.47
Std Dev 3.723
Gaus mean : 44.5269
Gaus Width: 4.0970
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

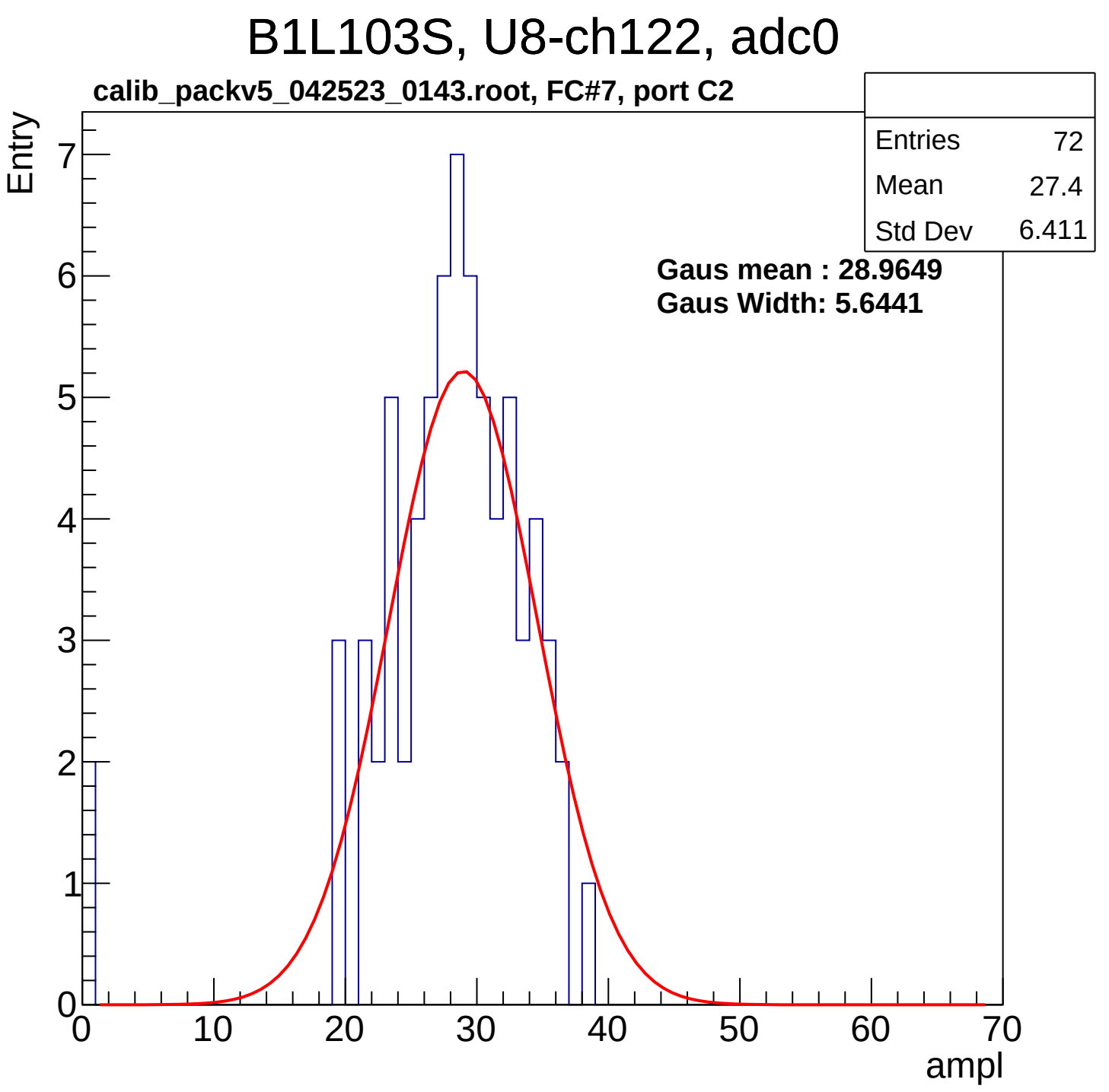

B1L103S, U8-ch121, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 49.41
Std Dev 3.452
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

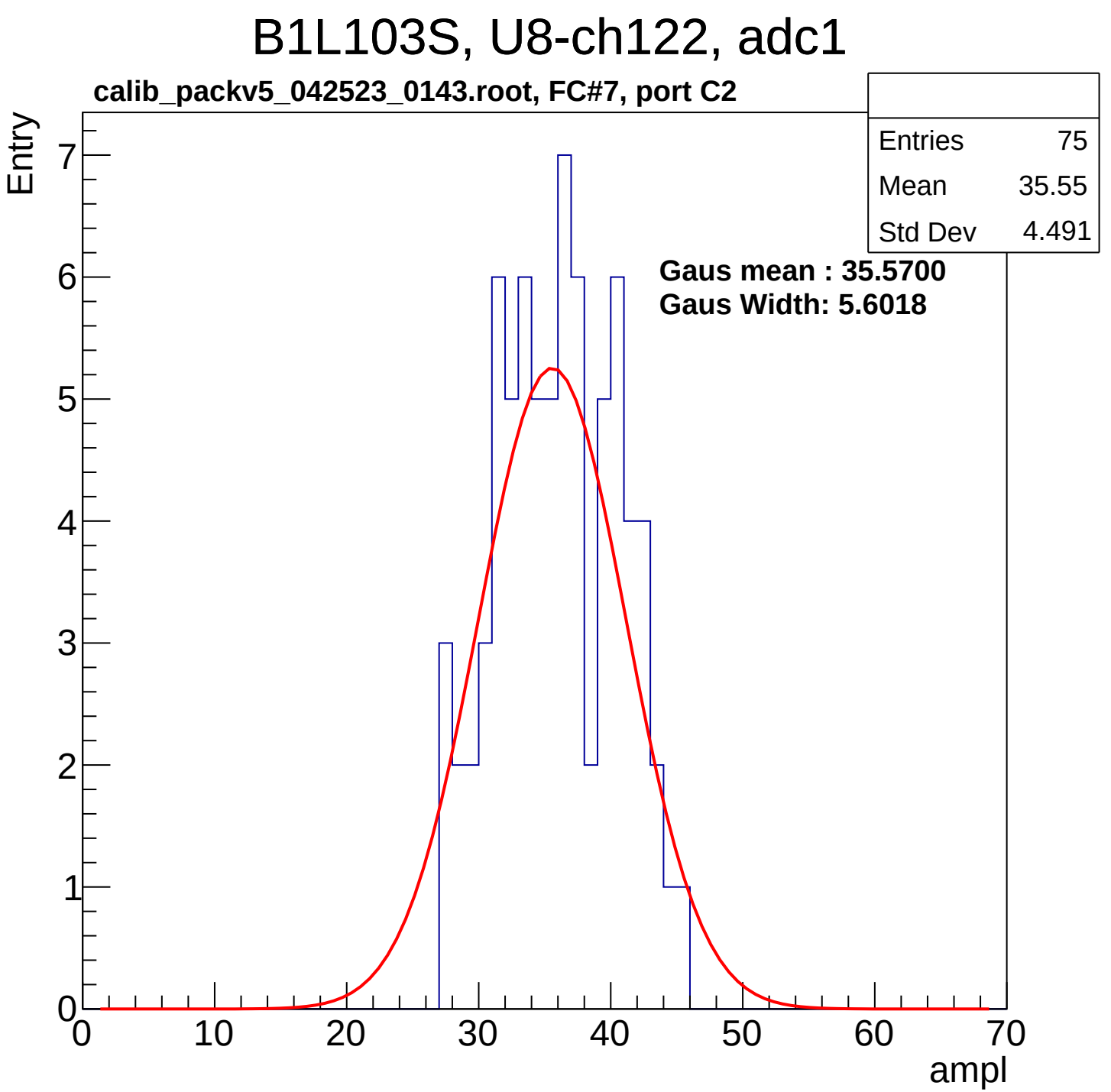

B1L103S, U8-ch121, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 68
Mean 55.4
Std Dev 7.454
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

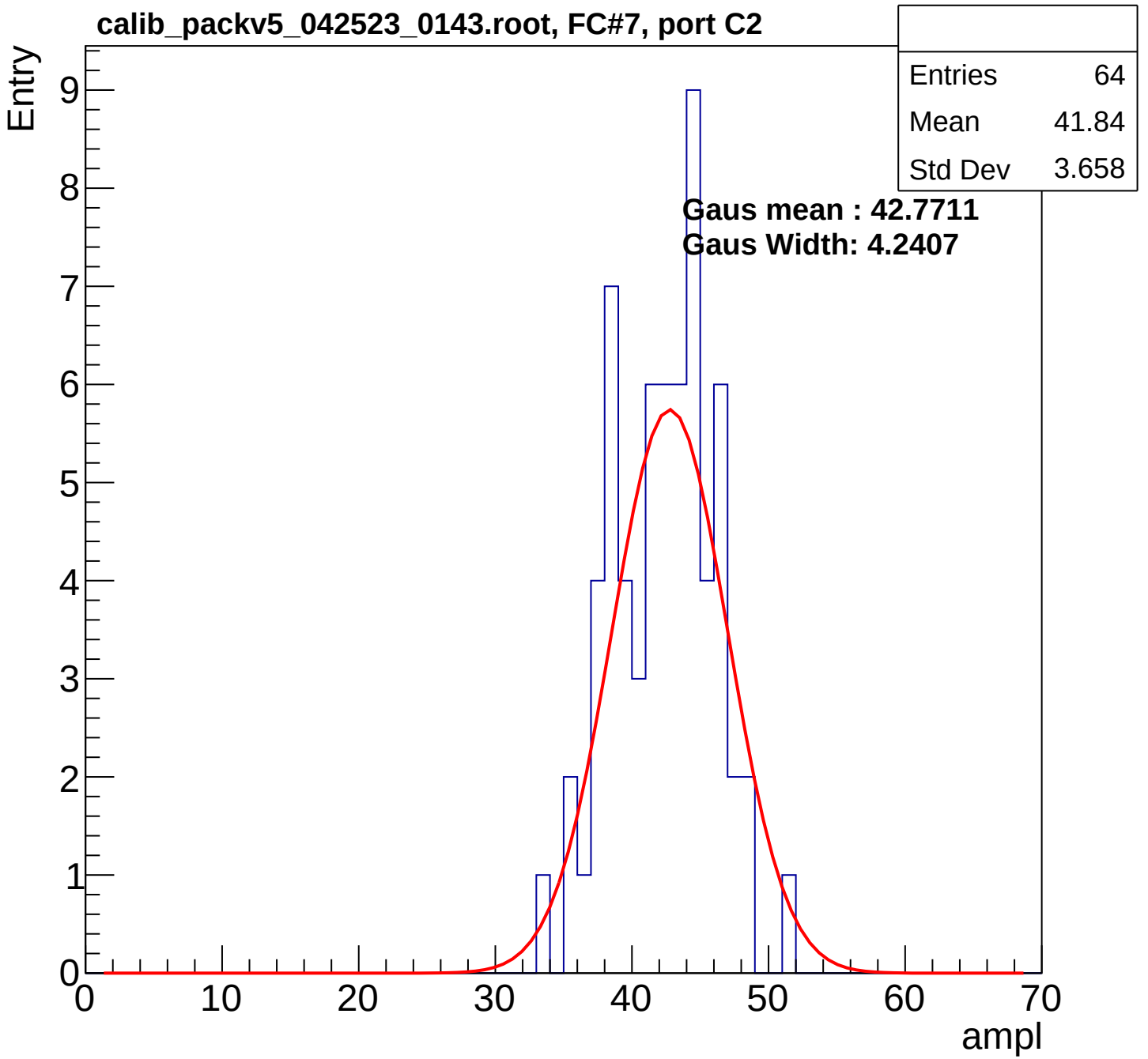

B1L103S, U8-ch121, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 30
Mean 60.53
Std Dev 1.875
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

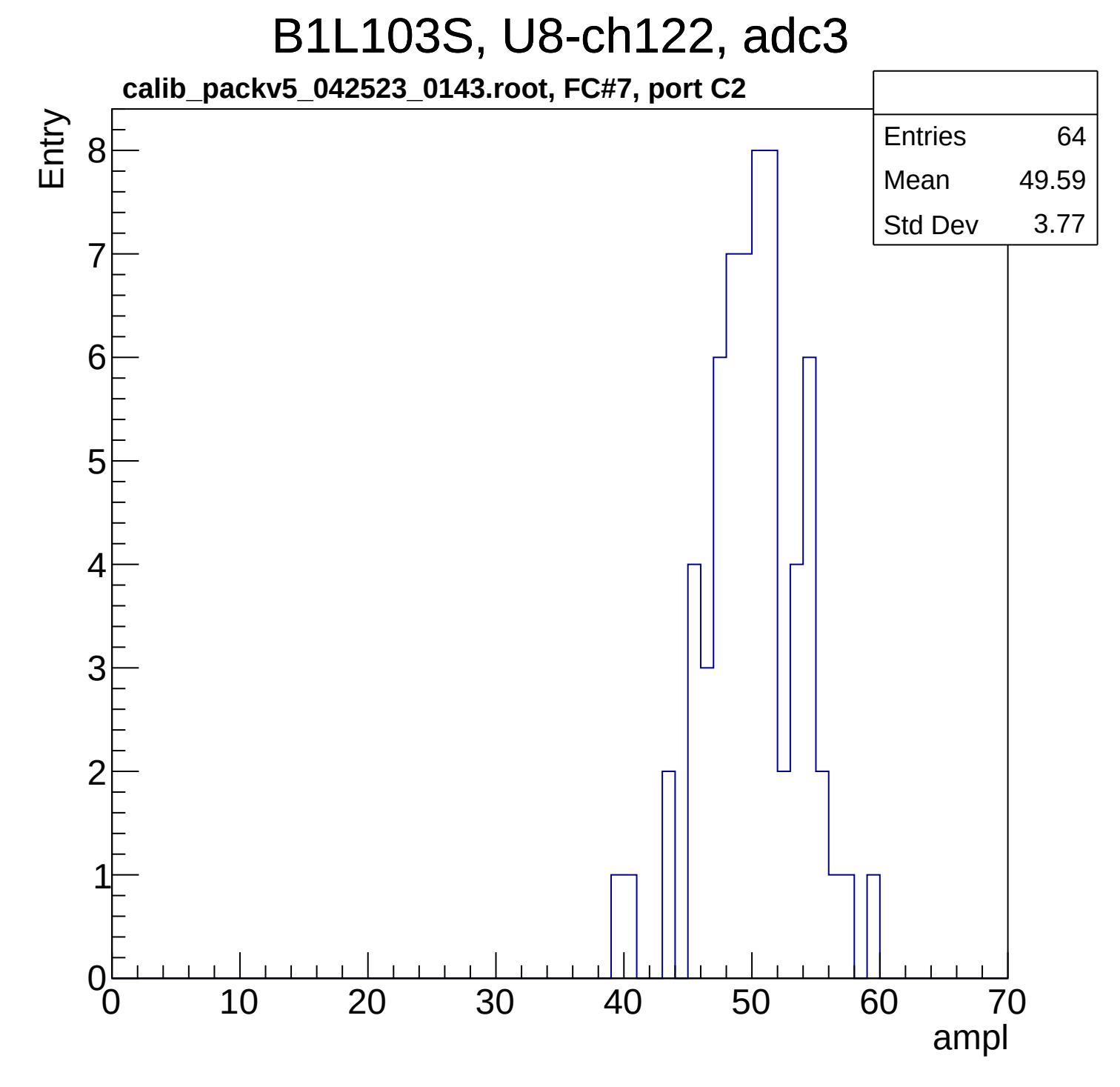

B1L103S, U8-ch121, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 8
Mean 62
Std Dev 1.323
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

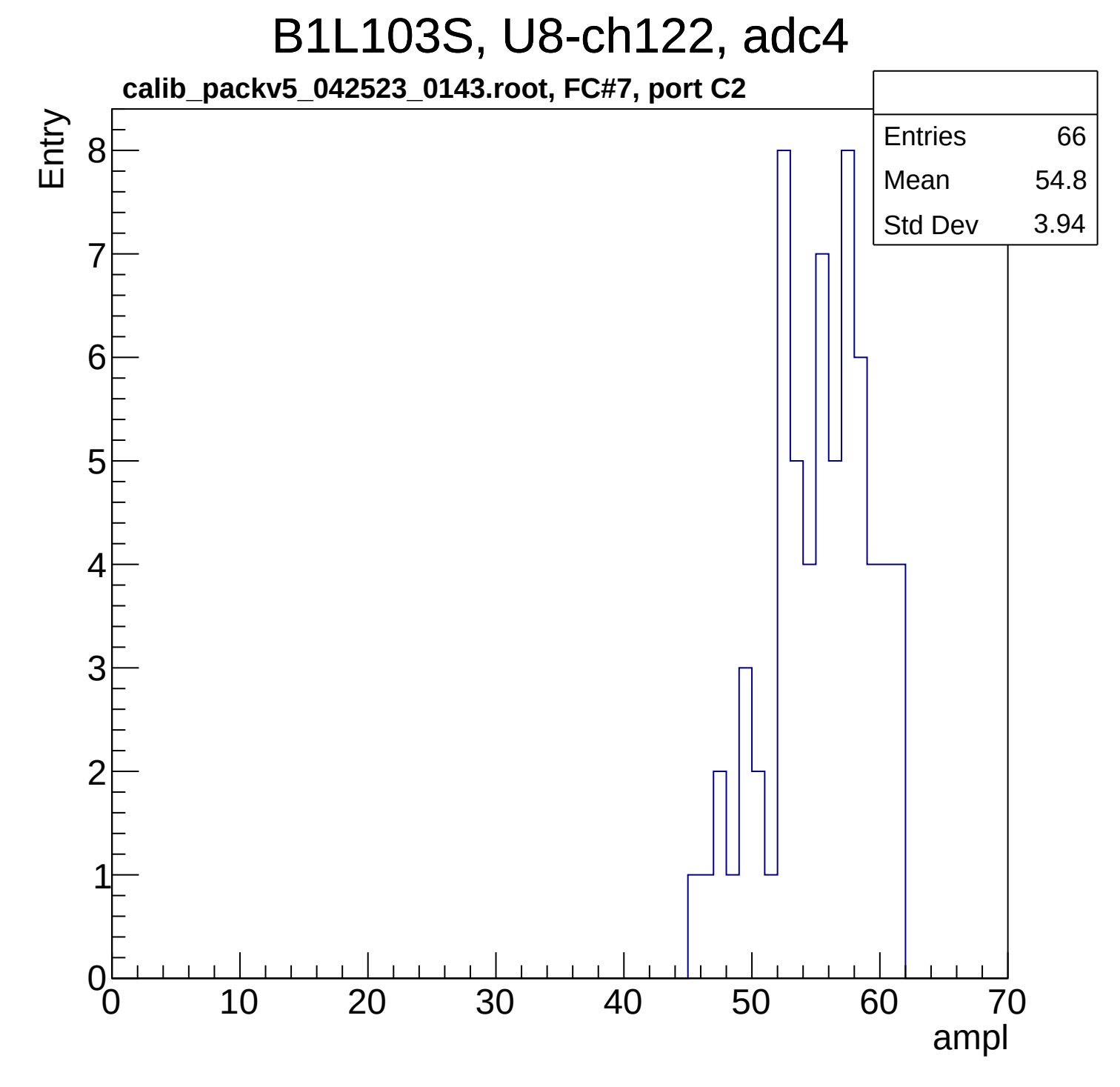

B1L103S, U8-ch121, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

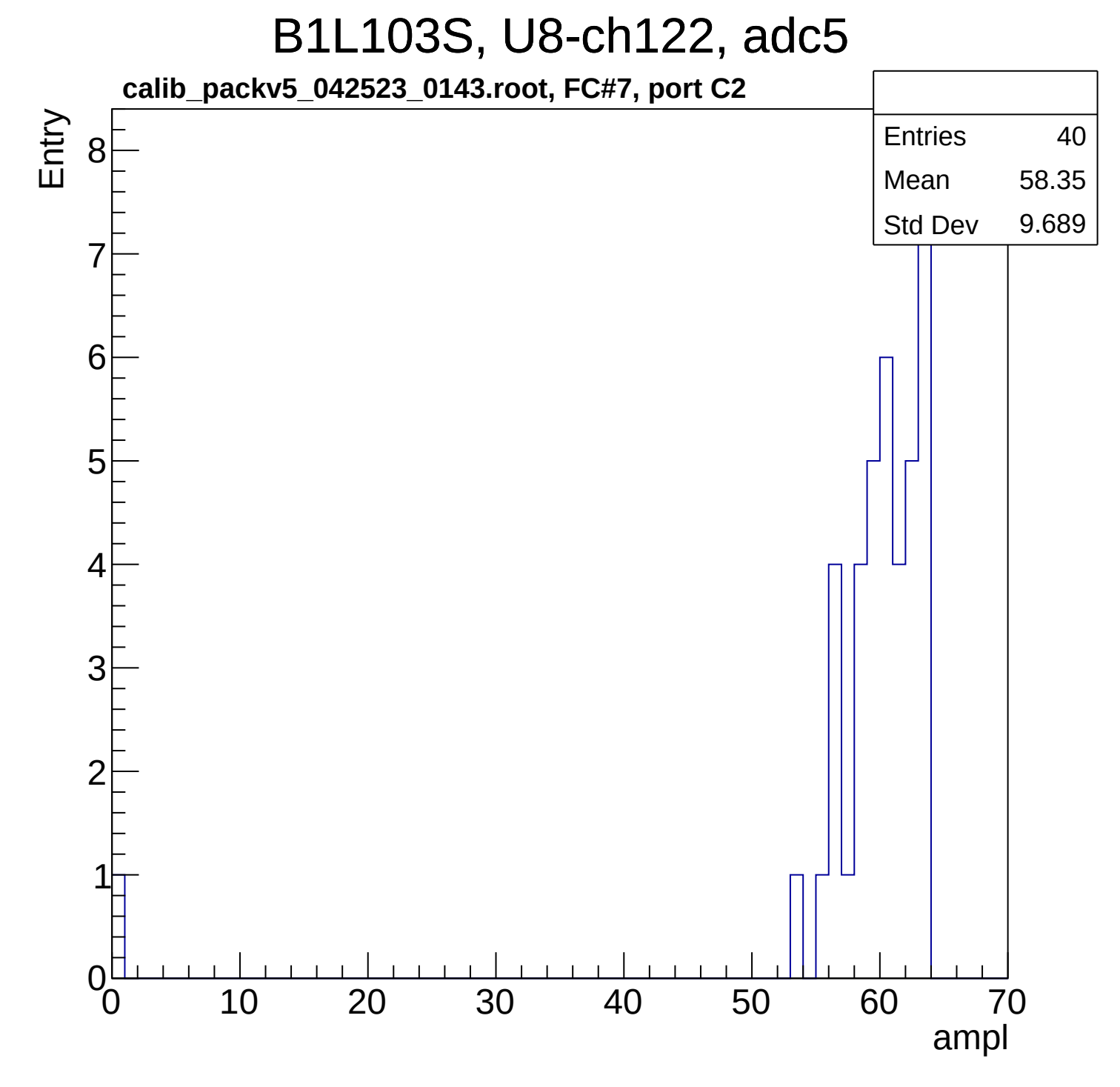

B1L103S, U8-ch122, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 72
Mean 27.4
Std Dev 6.411
Gaus mean : 28.9649
Gaus Width: 5.6441
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

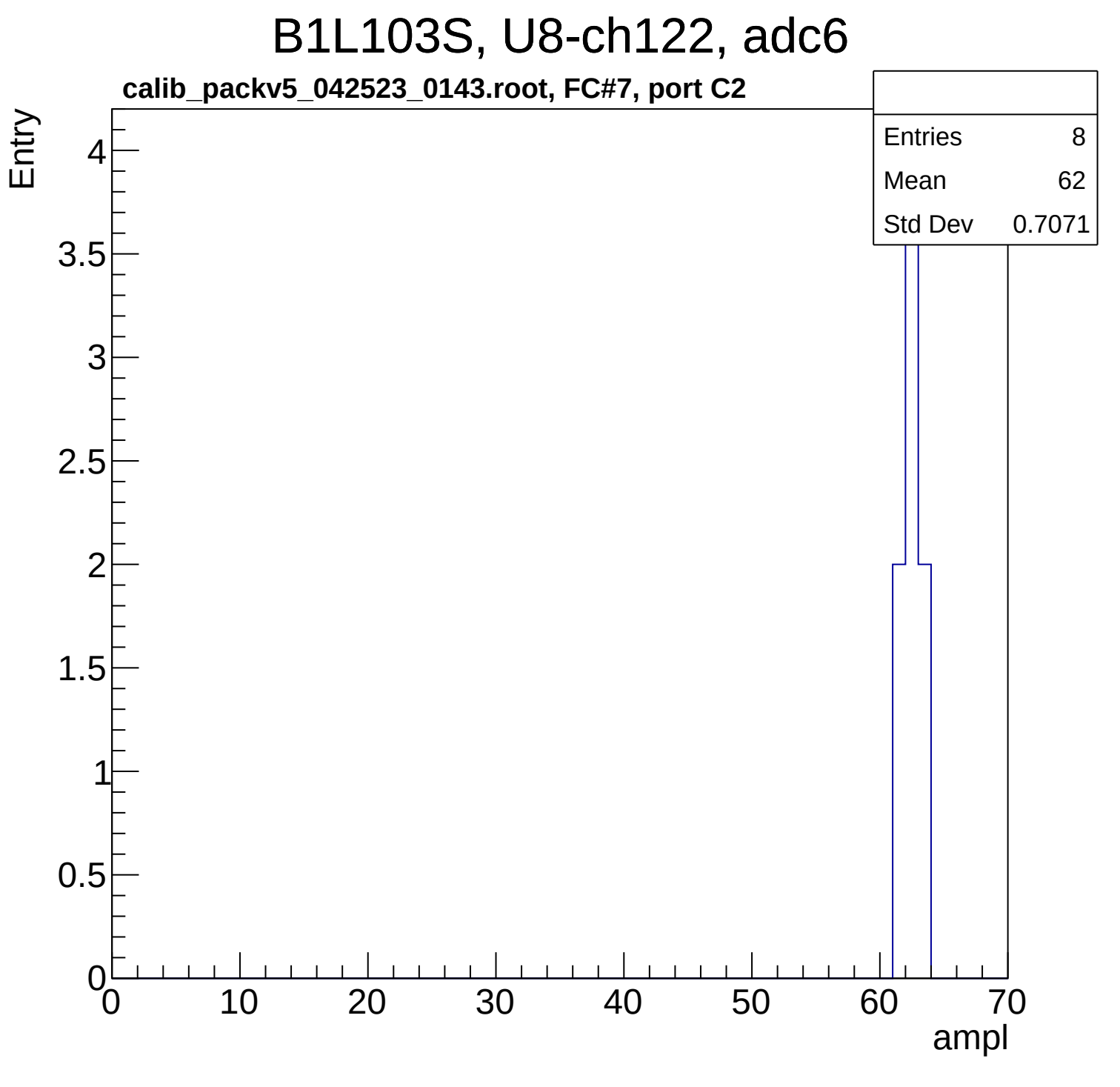

B1L103S, U8-ch122, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 75
Mean 35.55
Std Dev 4.491
Gaus mean : 35.5700
Gaus Width: 5.6018
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

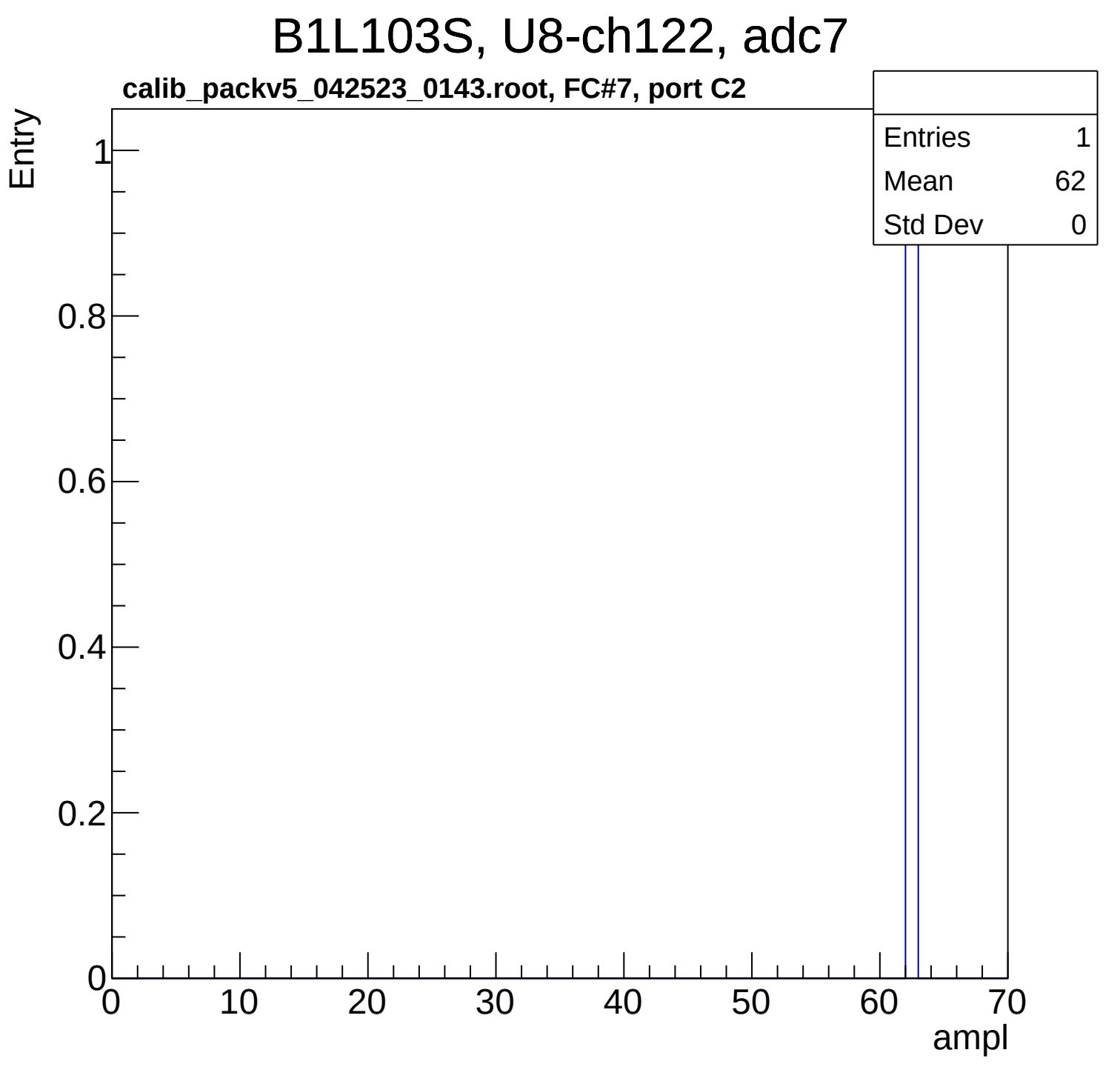

B1L103S, U8-ch122, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 41.84
Std Dev 3.658
Gaus mean : 42.7711
Gaus Width: 4.2407
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

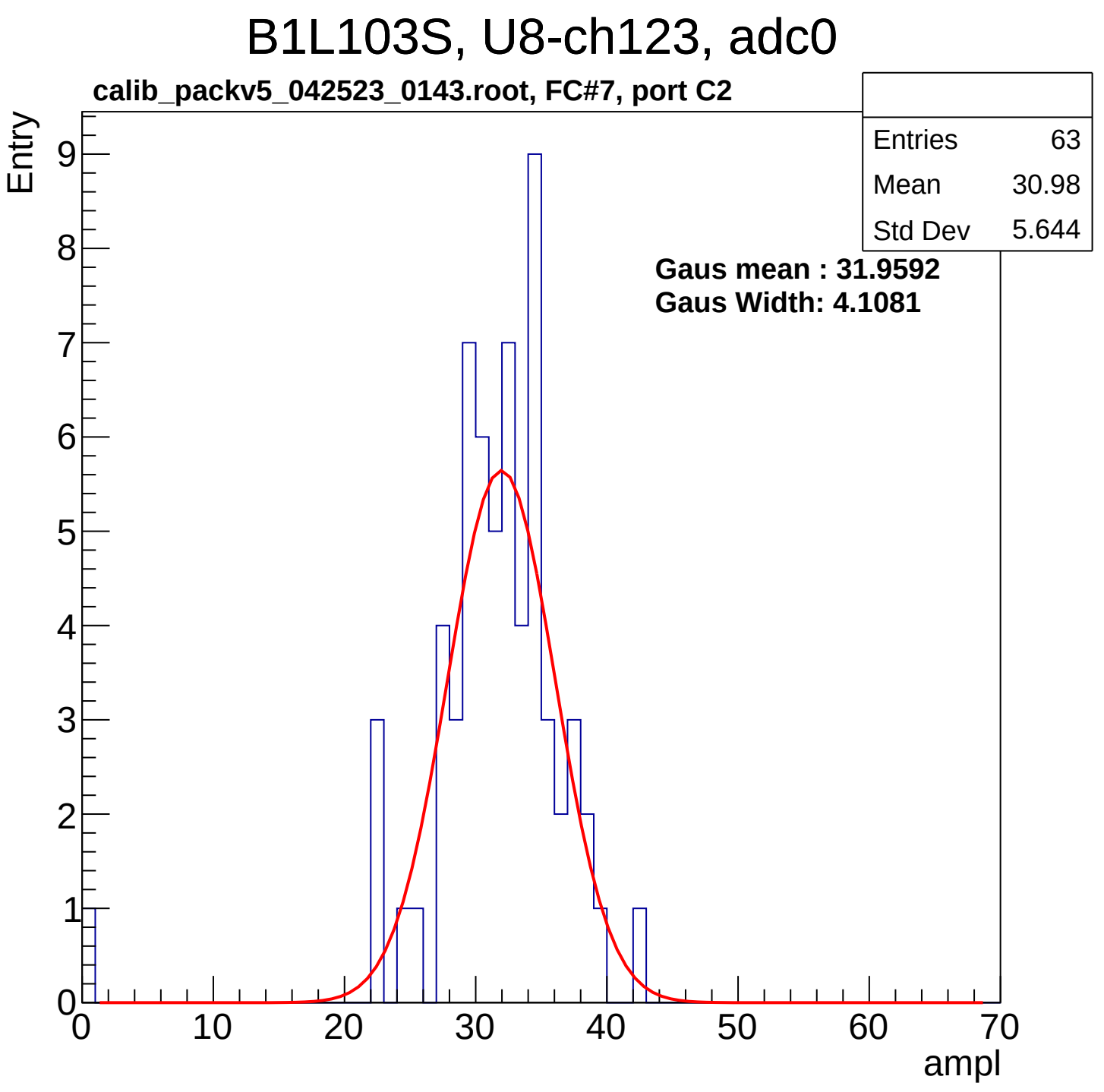

B1L103S, U8-ch122, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 49.59
Std Dev 3.77
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

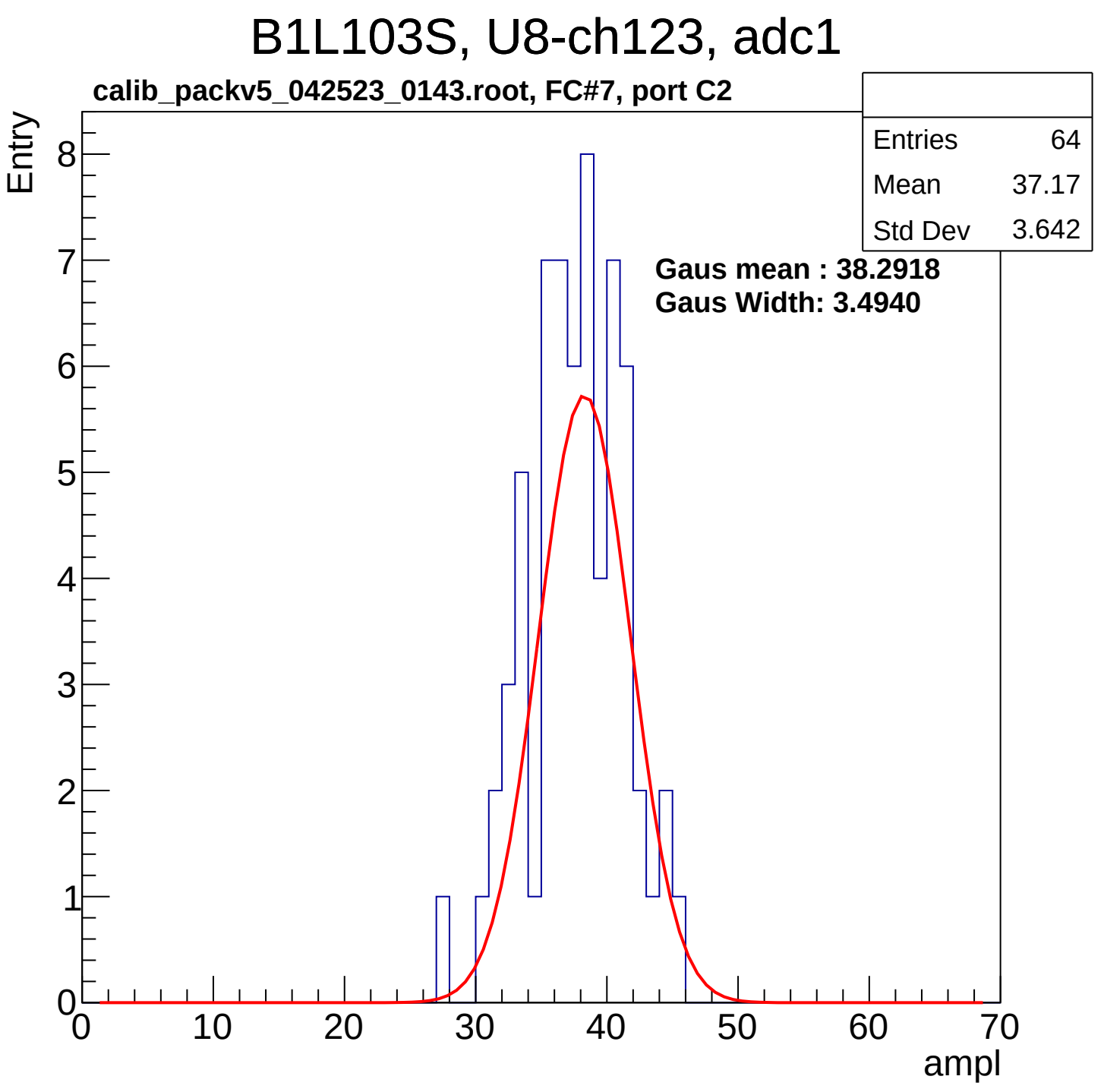

B1L103S, U8-ch122, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 66
Mean 54.8
Std Dev 3.94
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

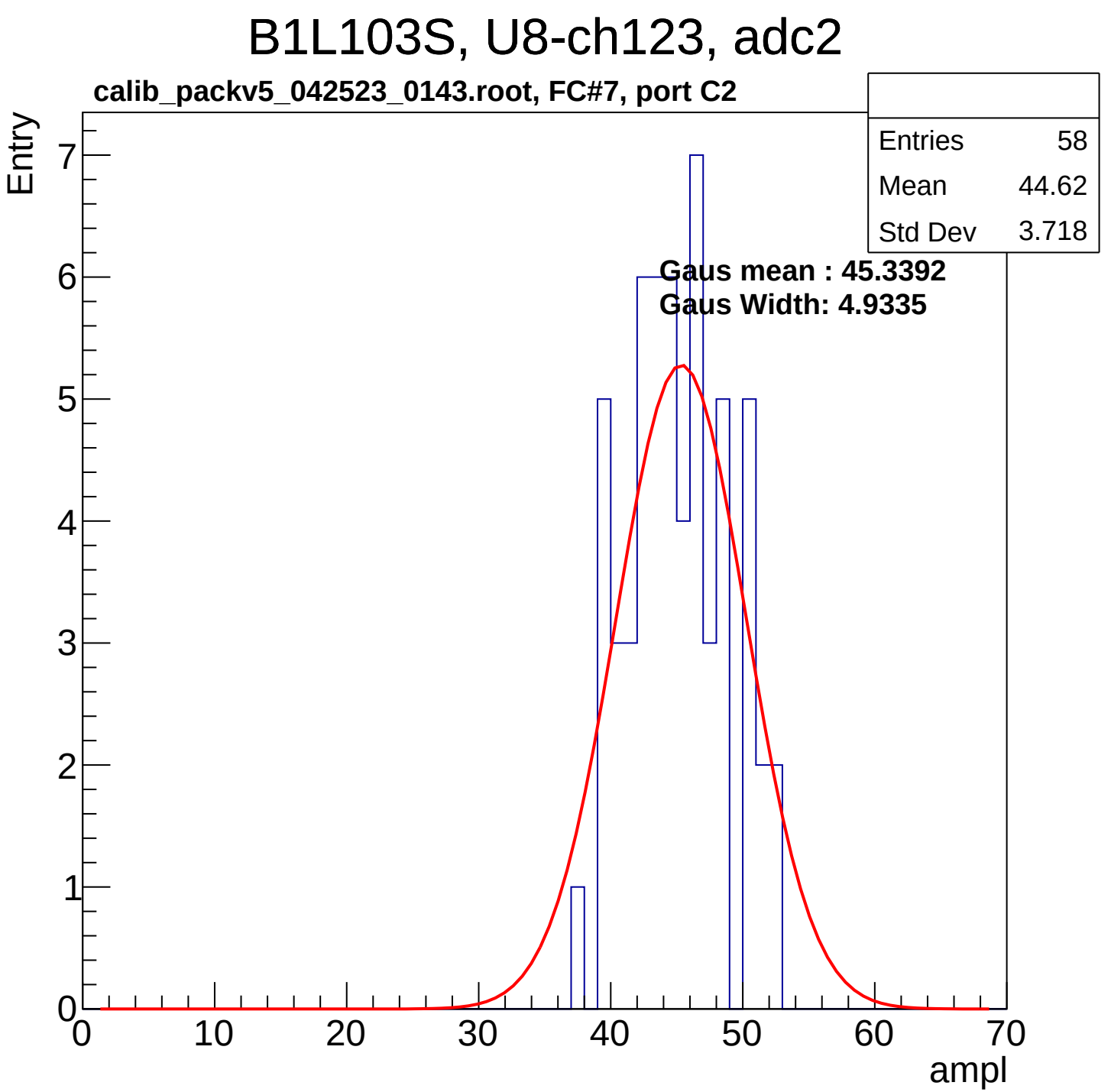

B1L103S, U8-ch122, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 40
Mean 58.35
Std Dev 9.689
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

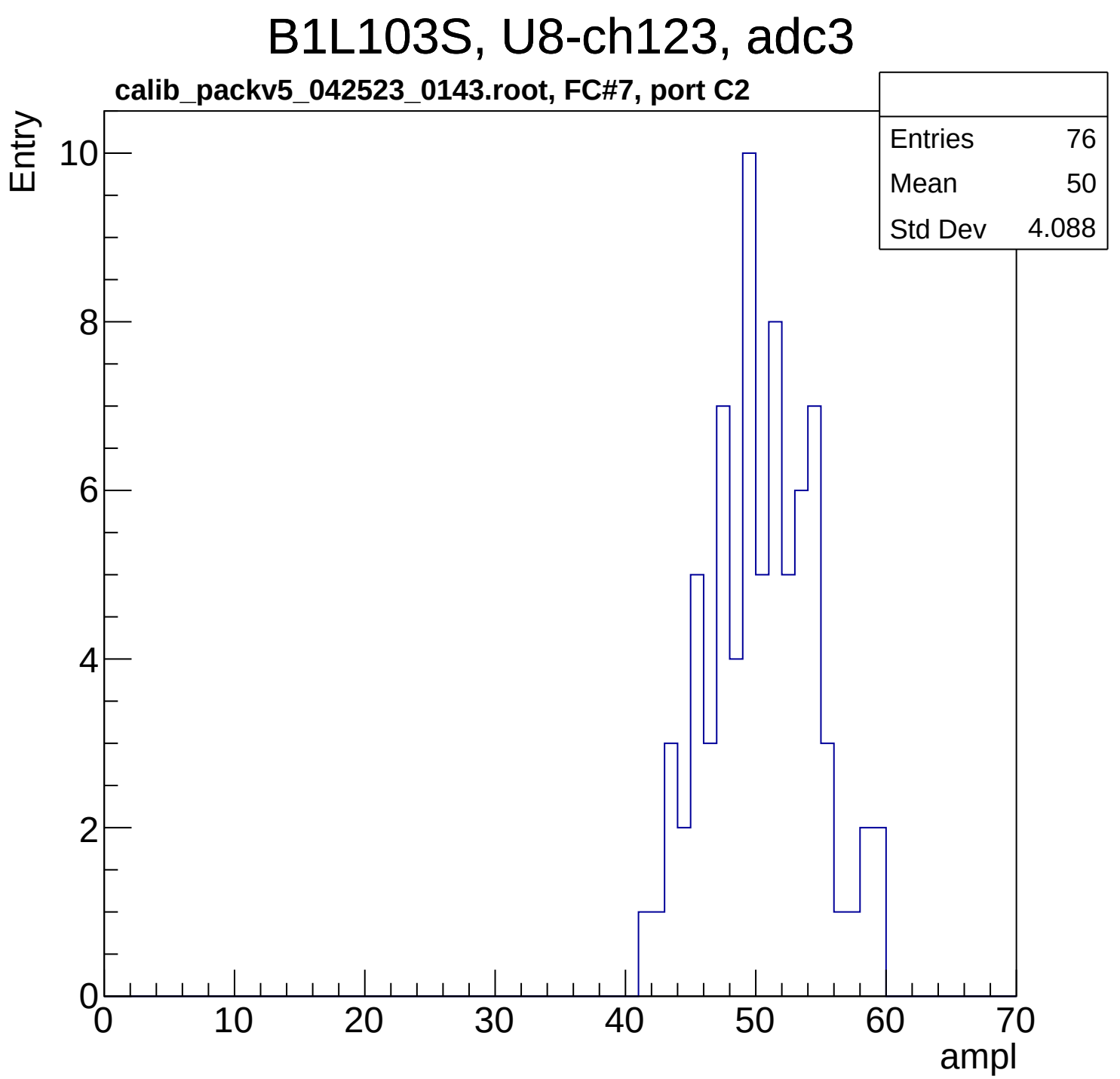

B1L103S, U8-ch122, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 8
Mean 62
Std Dev 0.7071
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

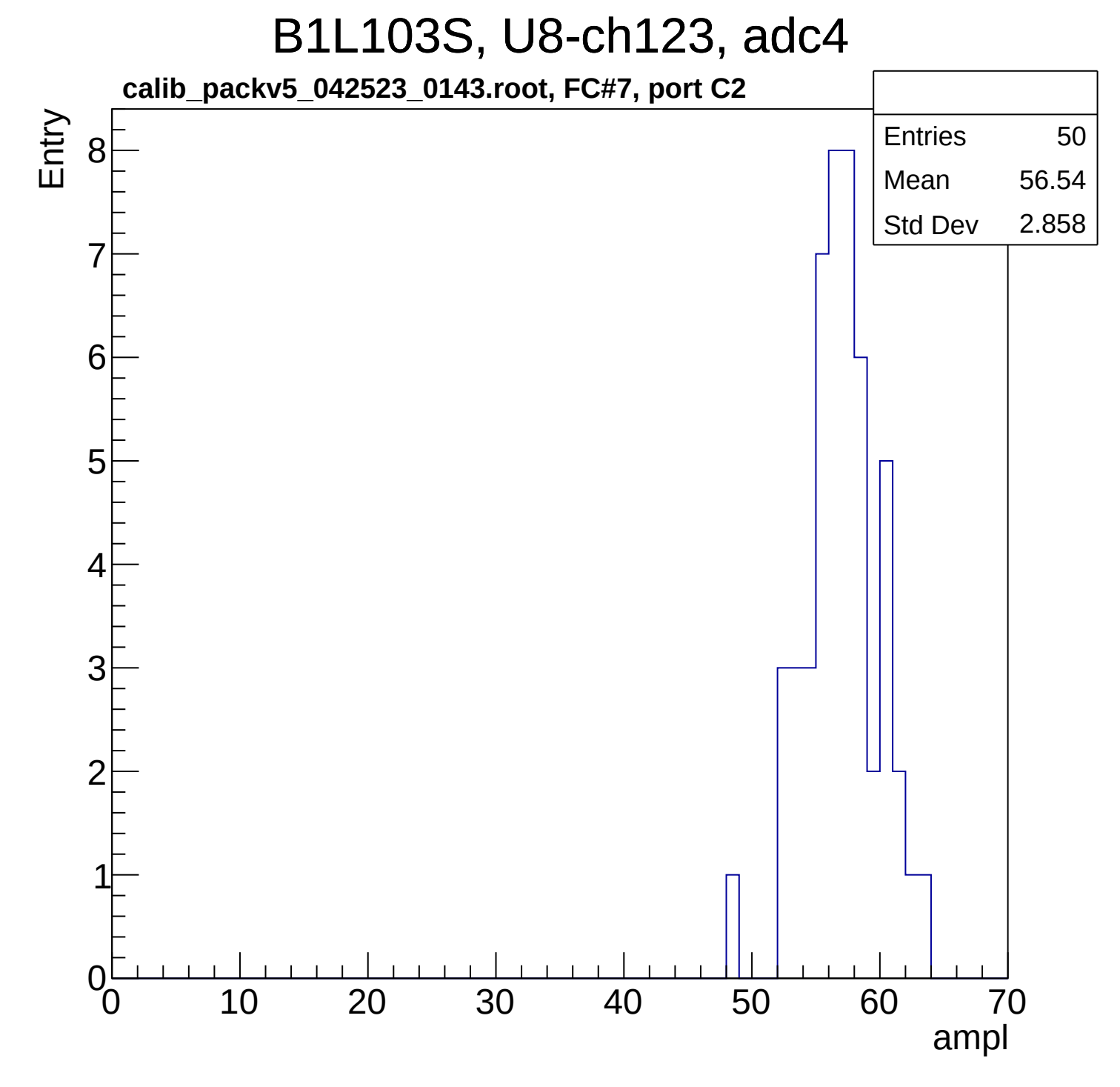

B1L103S, U8-ch122, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

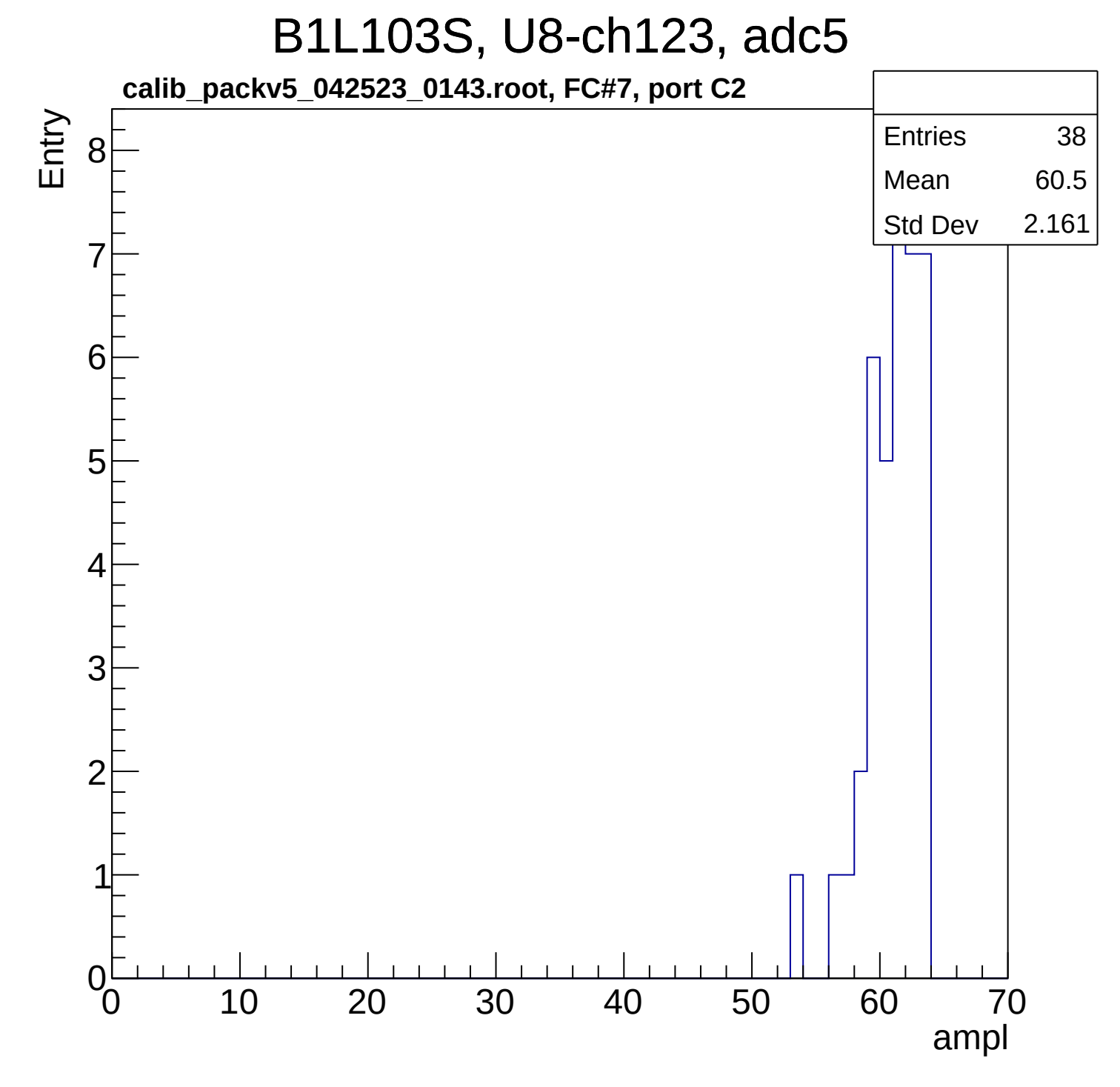

B1L103S, U8-ch123, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 63
Mean 30.98
Std Dev 5.644
Gaus mean : 31.9592
Gaus Width: 4.1081
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

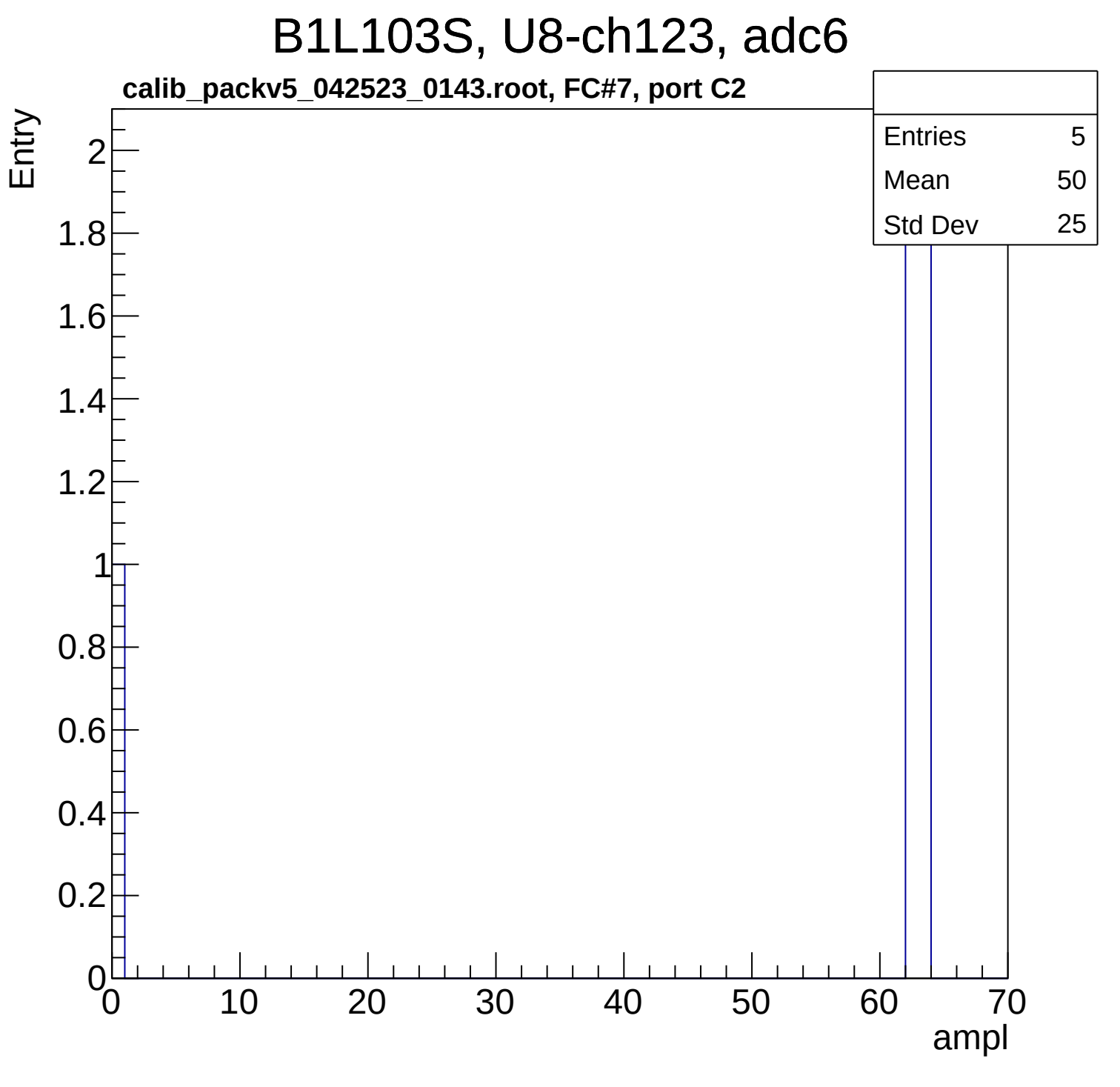

B1L103S, U8-ch123, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 37.17
Std Dev 3.642
Gaus mean : 38.2918
Gaus Width: 3.4940
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

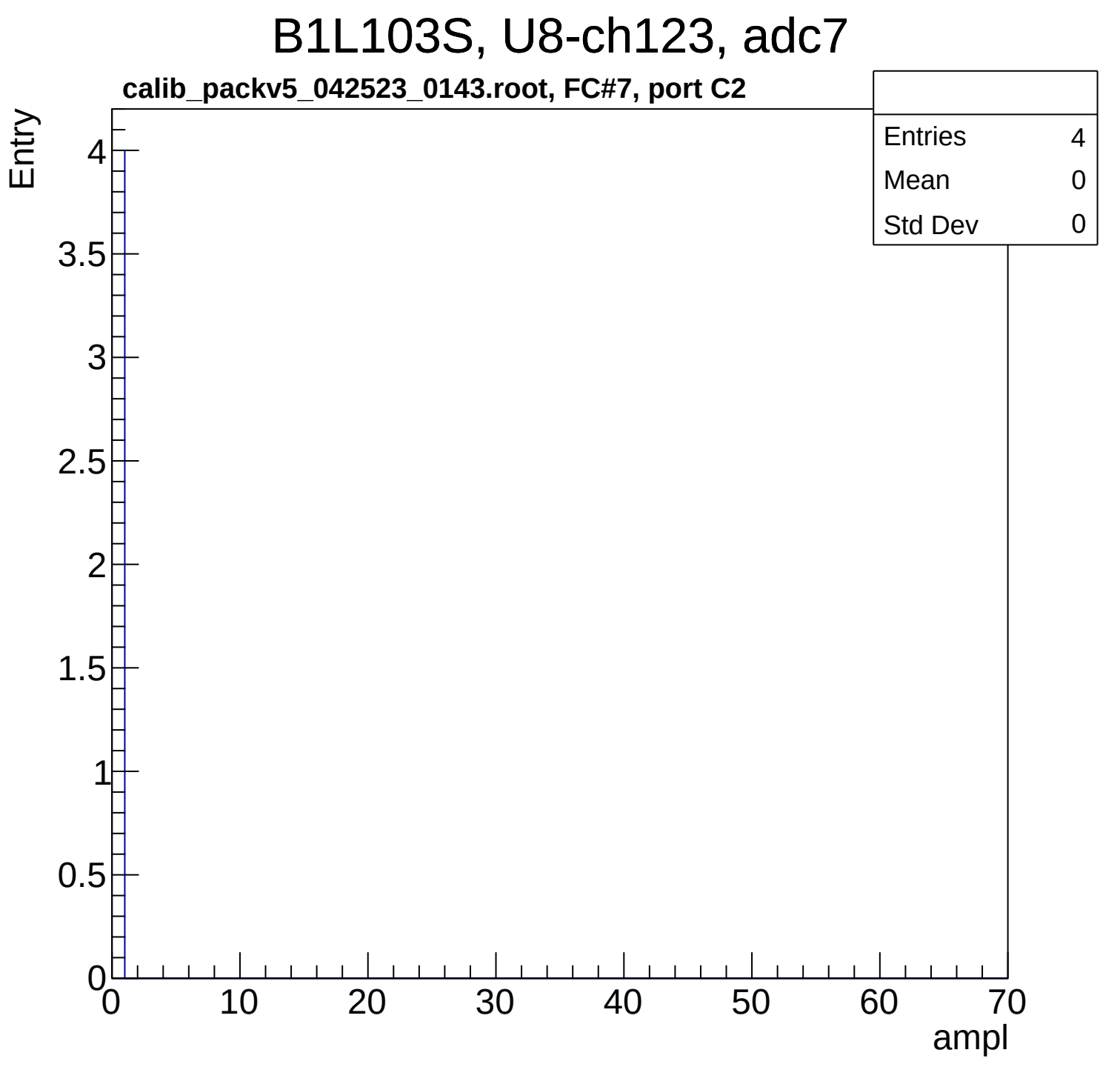

B1L103S, U8-ch123, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 44.62
Std Dev 3.718
Gaus mean : 45.3392
Gaus Width: 4.9335
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

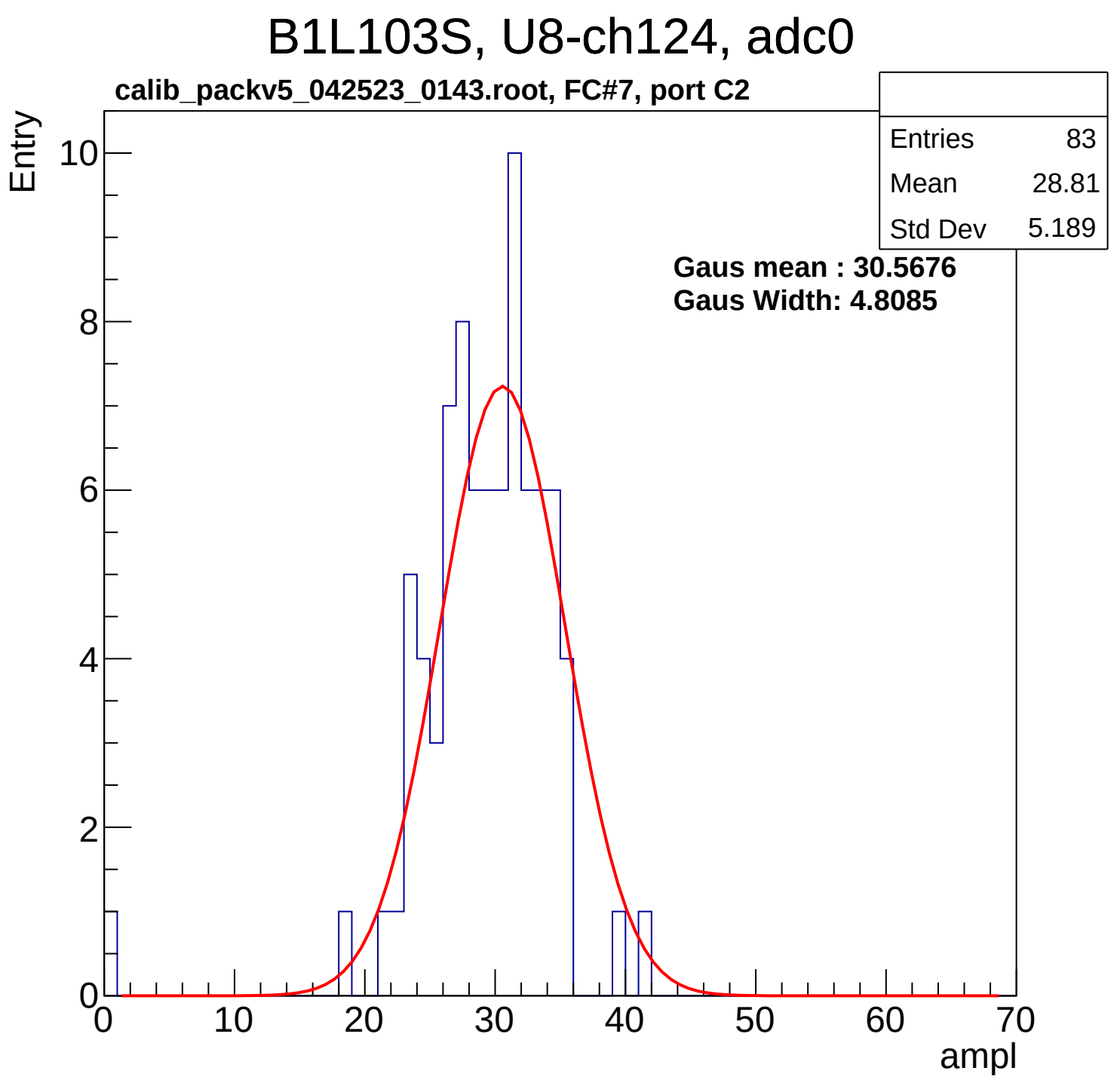

B1L103S, U8-ch123, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 76
Mean 50
Std Dev 4.088
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

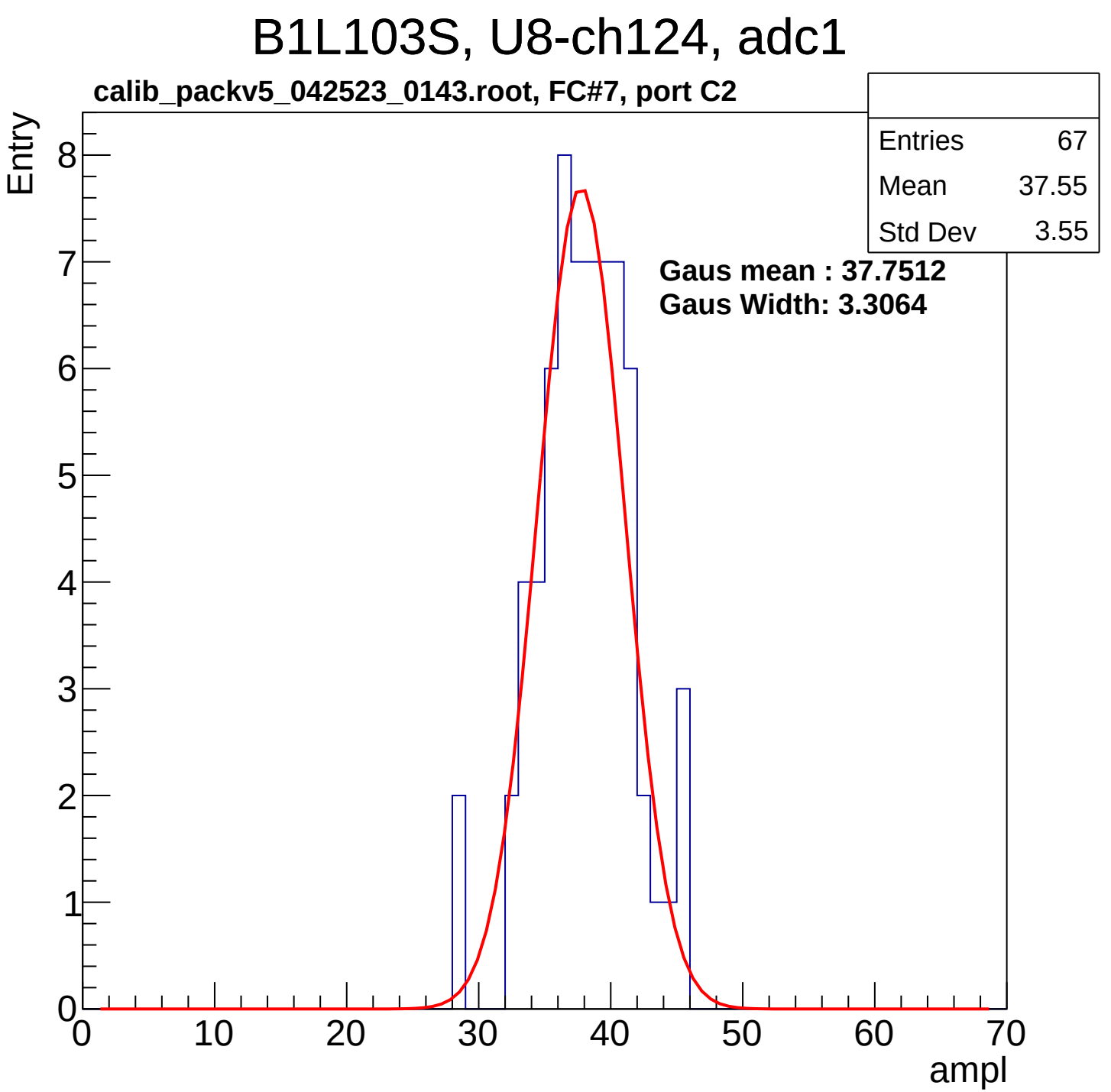

B1L103S, U8-ch123, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 50
Mean 56.54
Std Dev 2.858
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

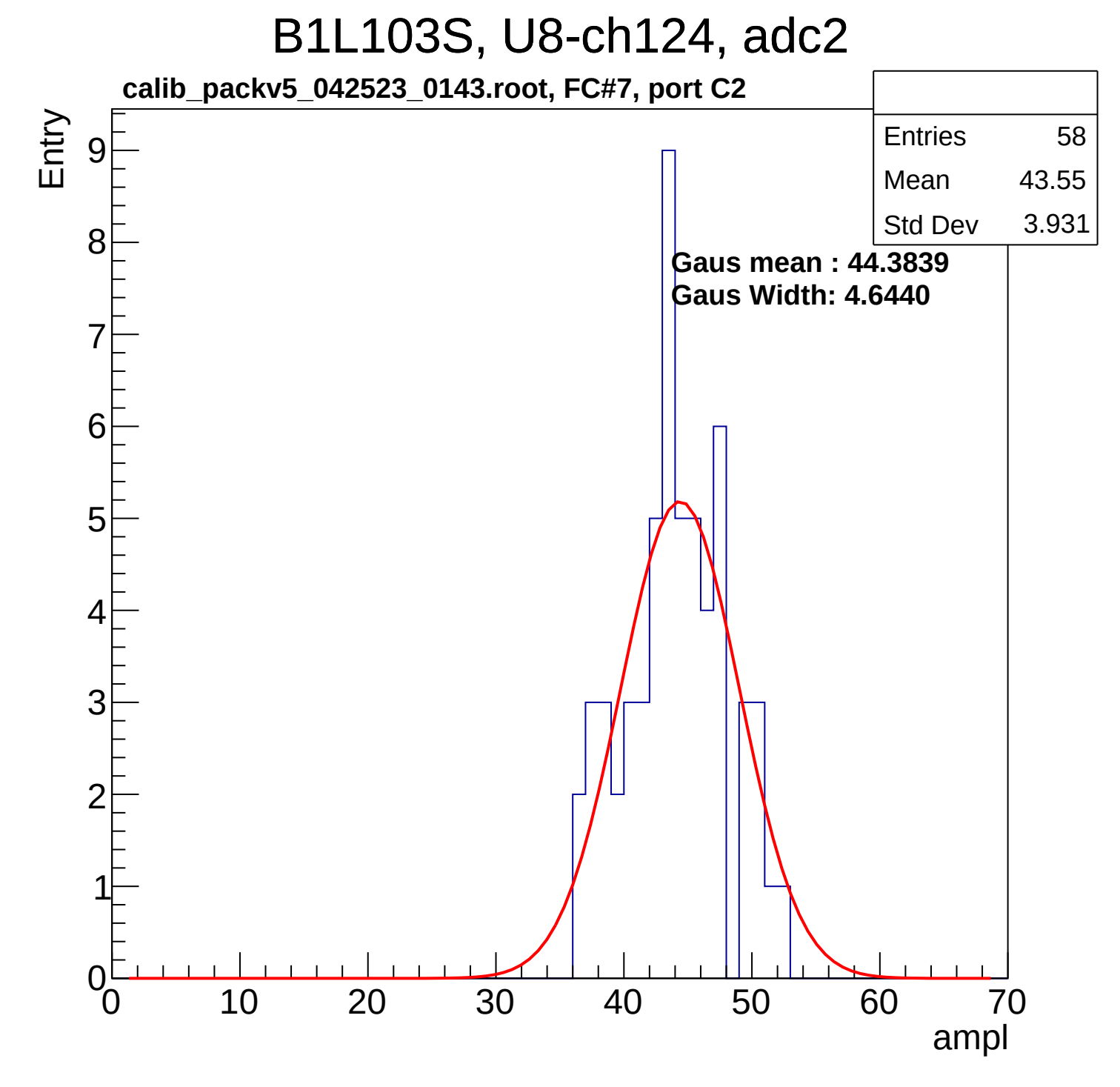

B1L103S, U8-ch123, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 38
Mean 60.5
Std Dev 2.161
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

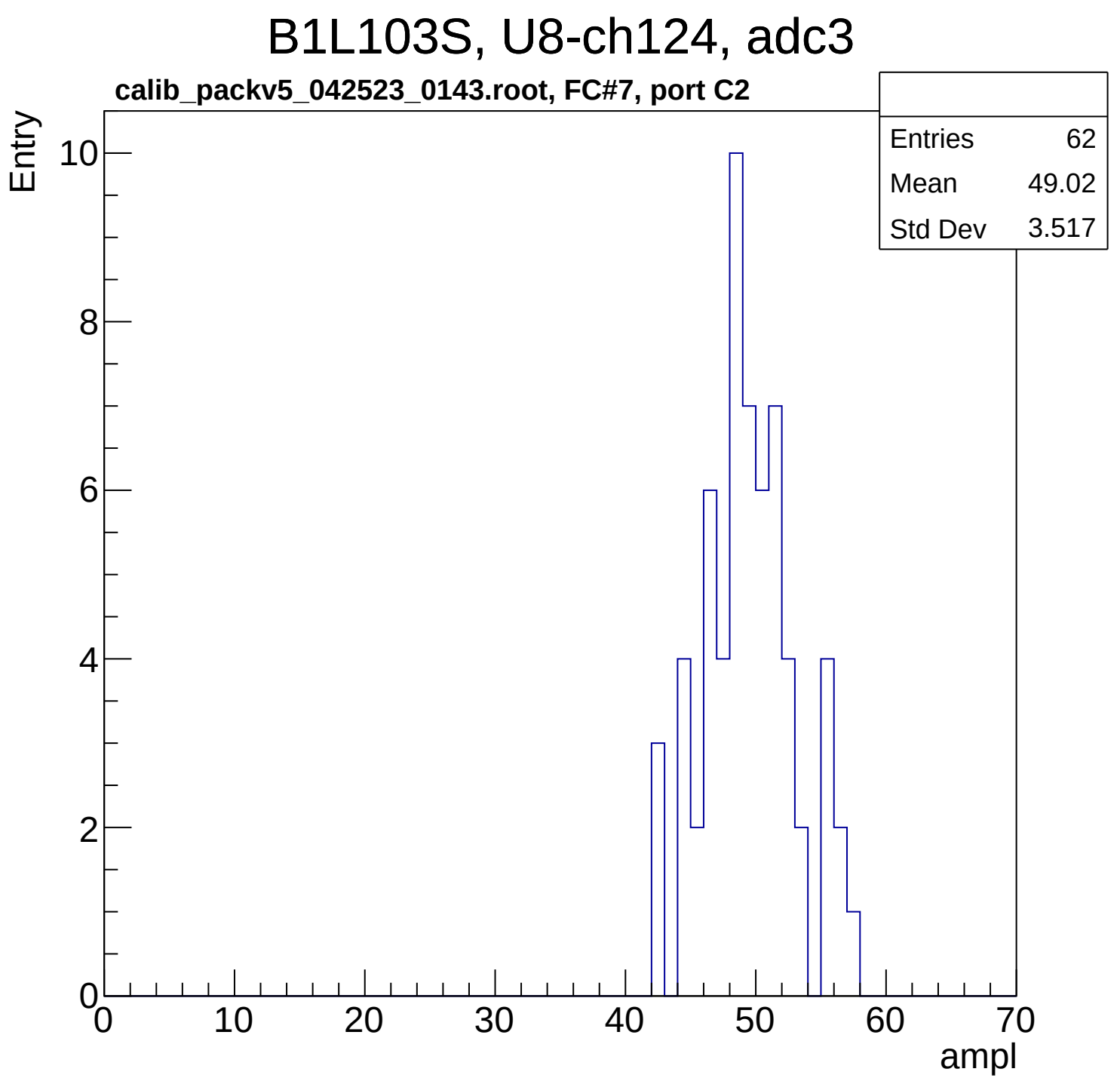

B1L103S, U8-ch123, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 5
Mean 50
Std Dev 25
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

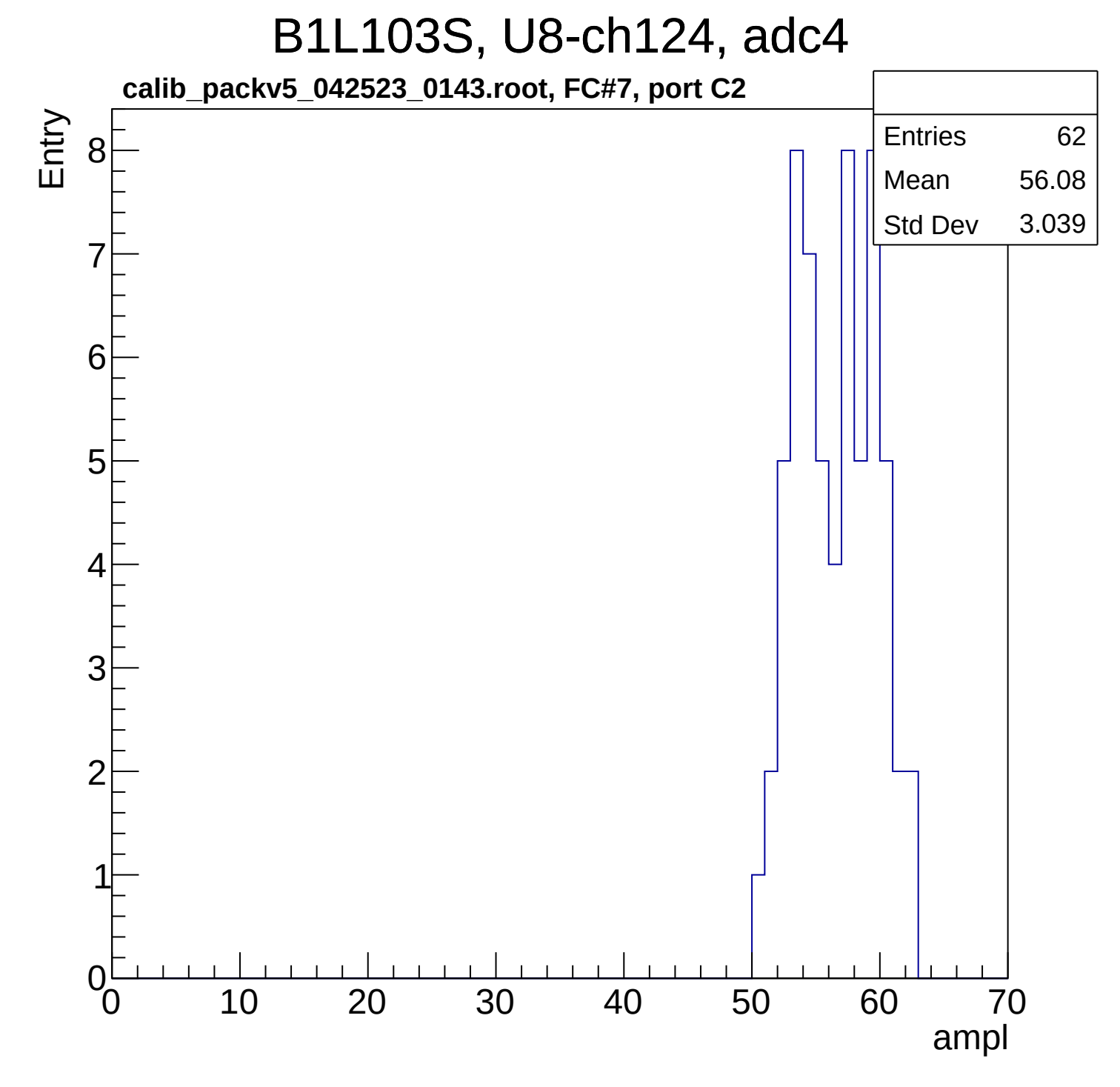

B1L103S, U8-ch123, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 4
Mean 0
Std Dev 0
Entry
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70
ampl

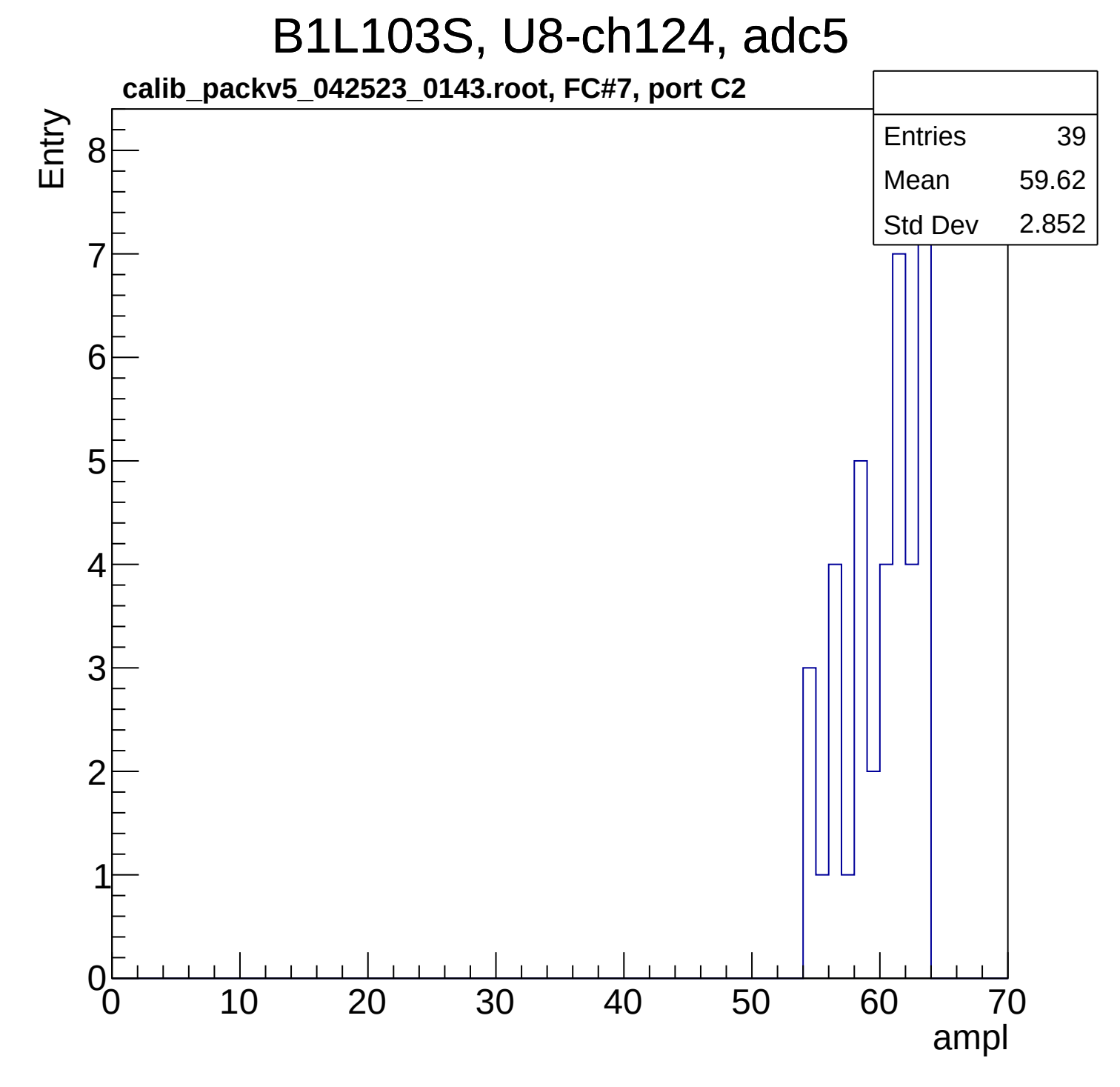

B1L103S, U8-ch124, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 83
Mean 28.81
Std Dev 5.189
Gaus mean : 30.5676
Gaus Width: 4.8085
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

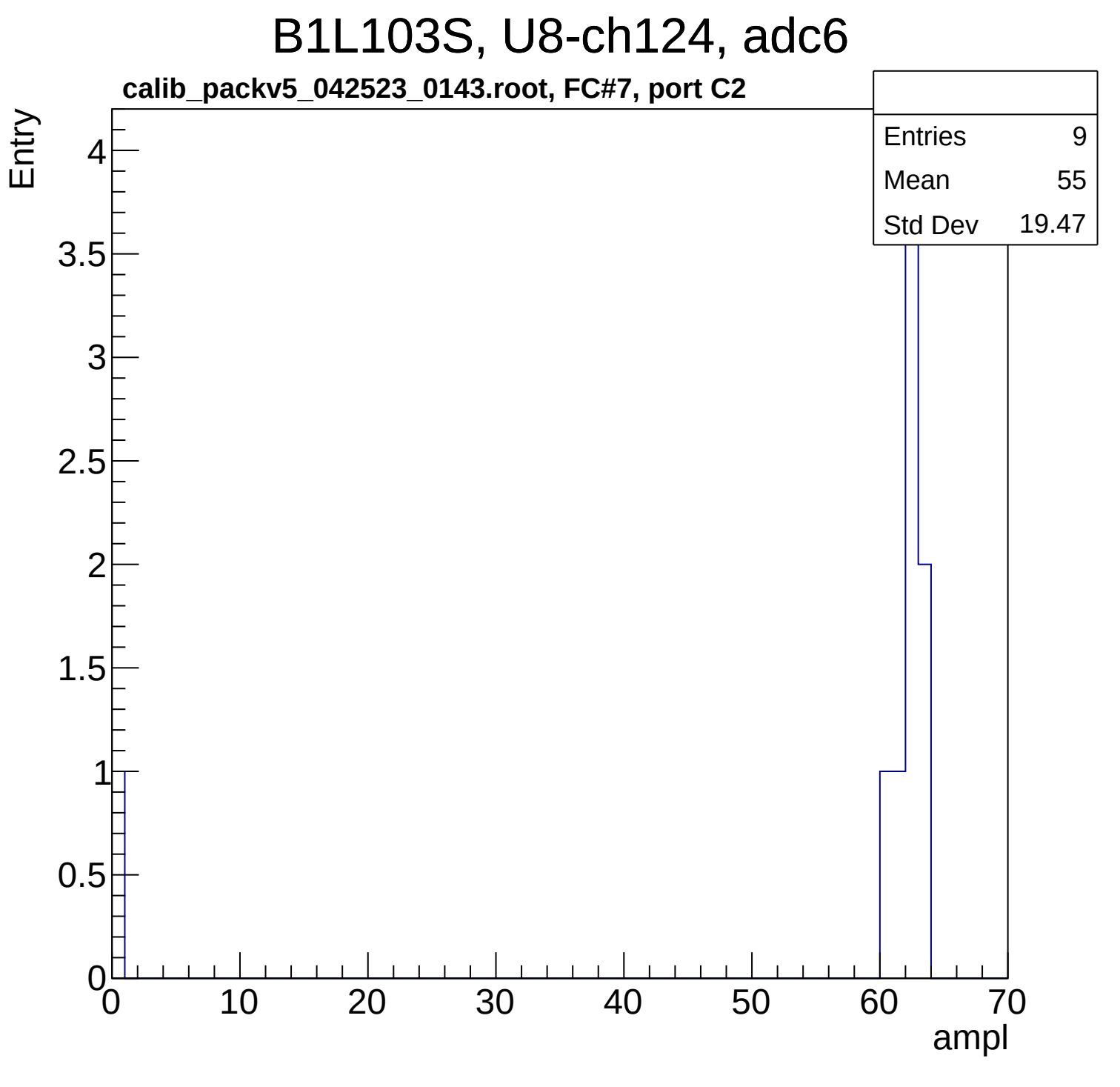

B1L103S, U8-ch124, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 67
Mean 37.55
Std Dev 3.55
Gaus mean : 37.7512
Gaus Width: 3.3064
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

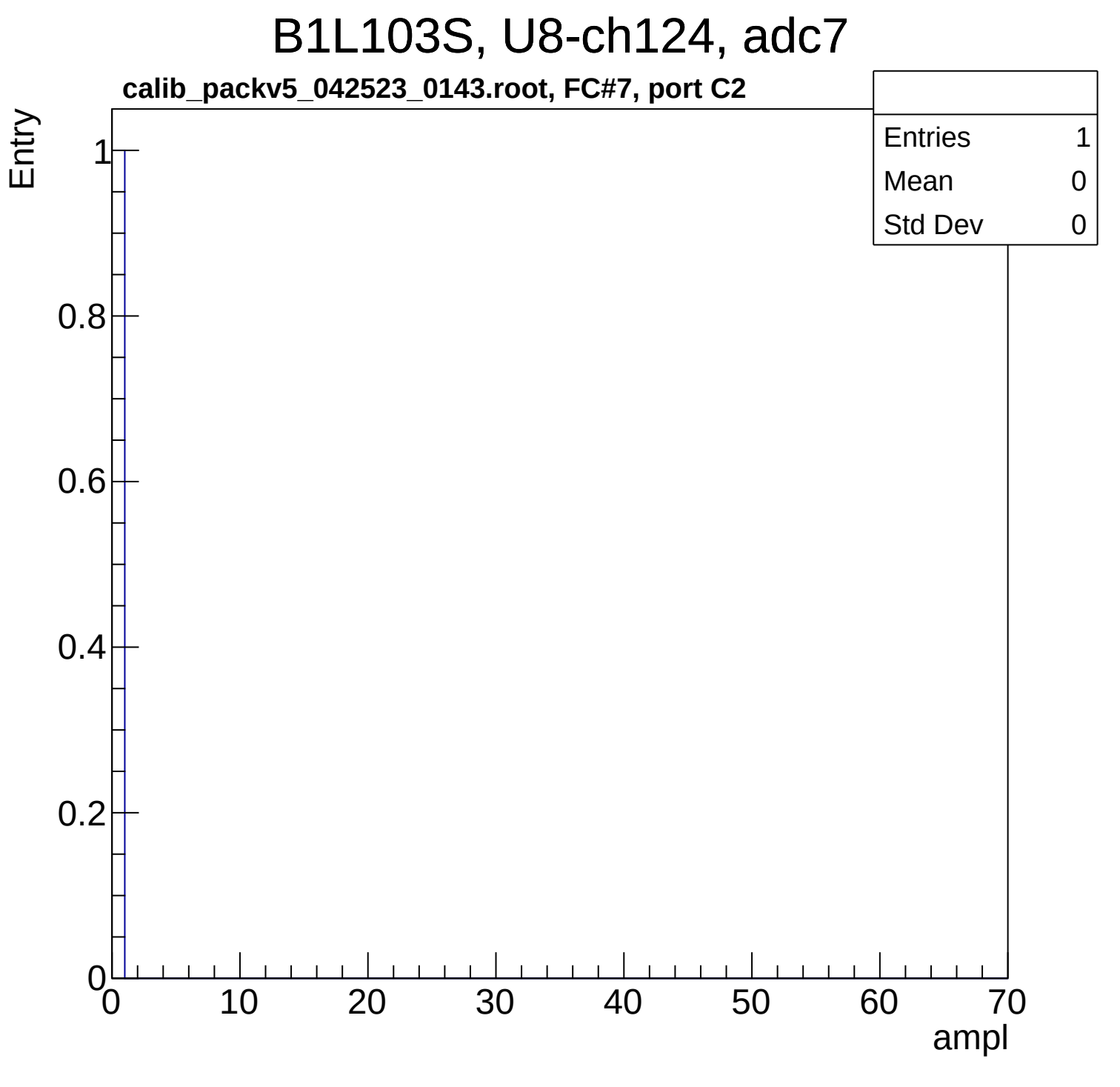

B1L103S, U8-ch124, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 58
Mean 43.55
Std Dev 3.931
Gaus mean : 44.3839
Gaus Width: 4.6440
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

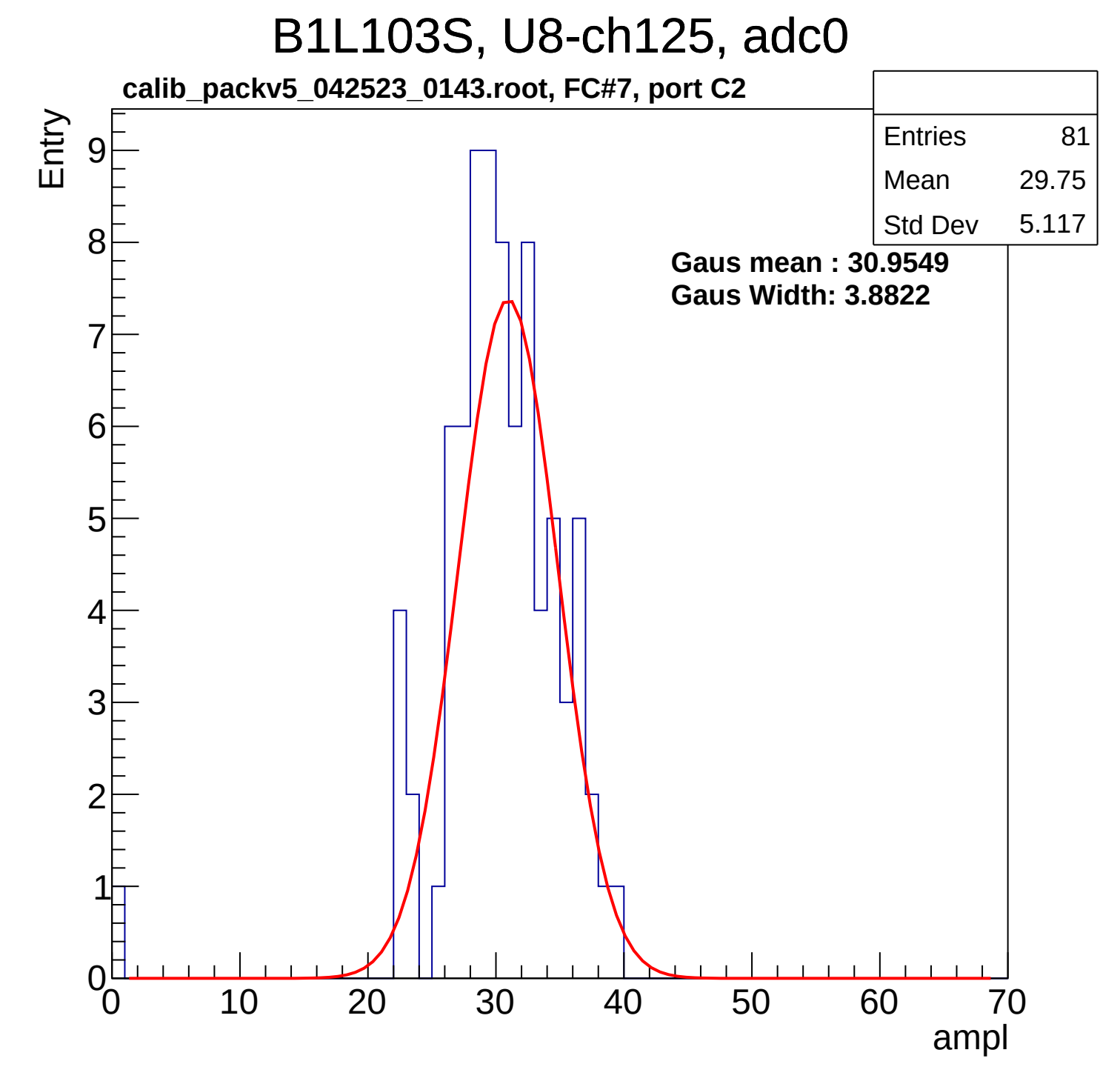

B1L103S, U8-ch124, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 49.02
Std Dev 3.517
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

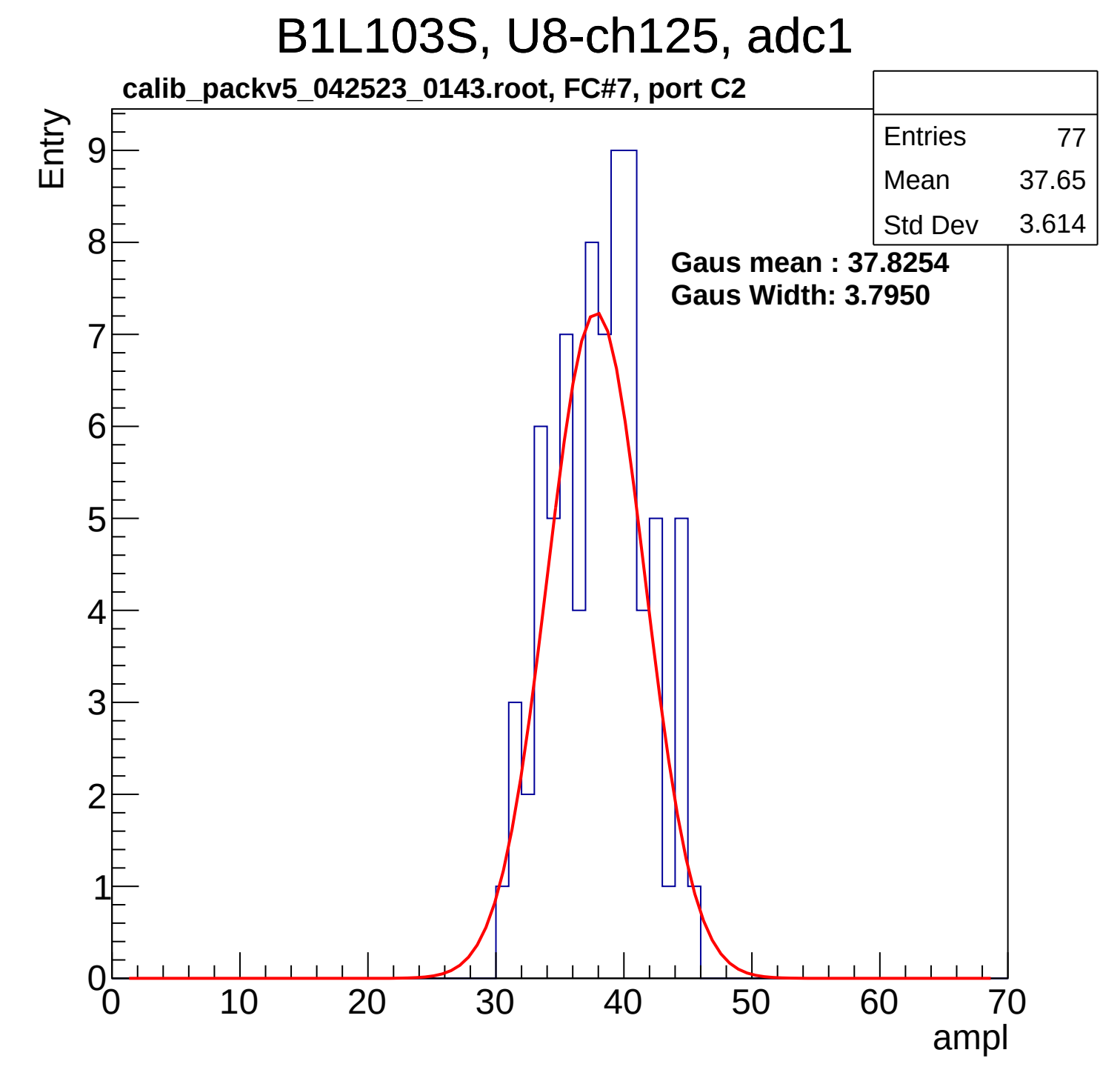

B1L103S, U8-ch124, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 56.08
Std Dev 3.039
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

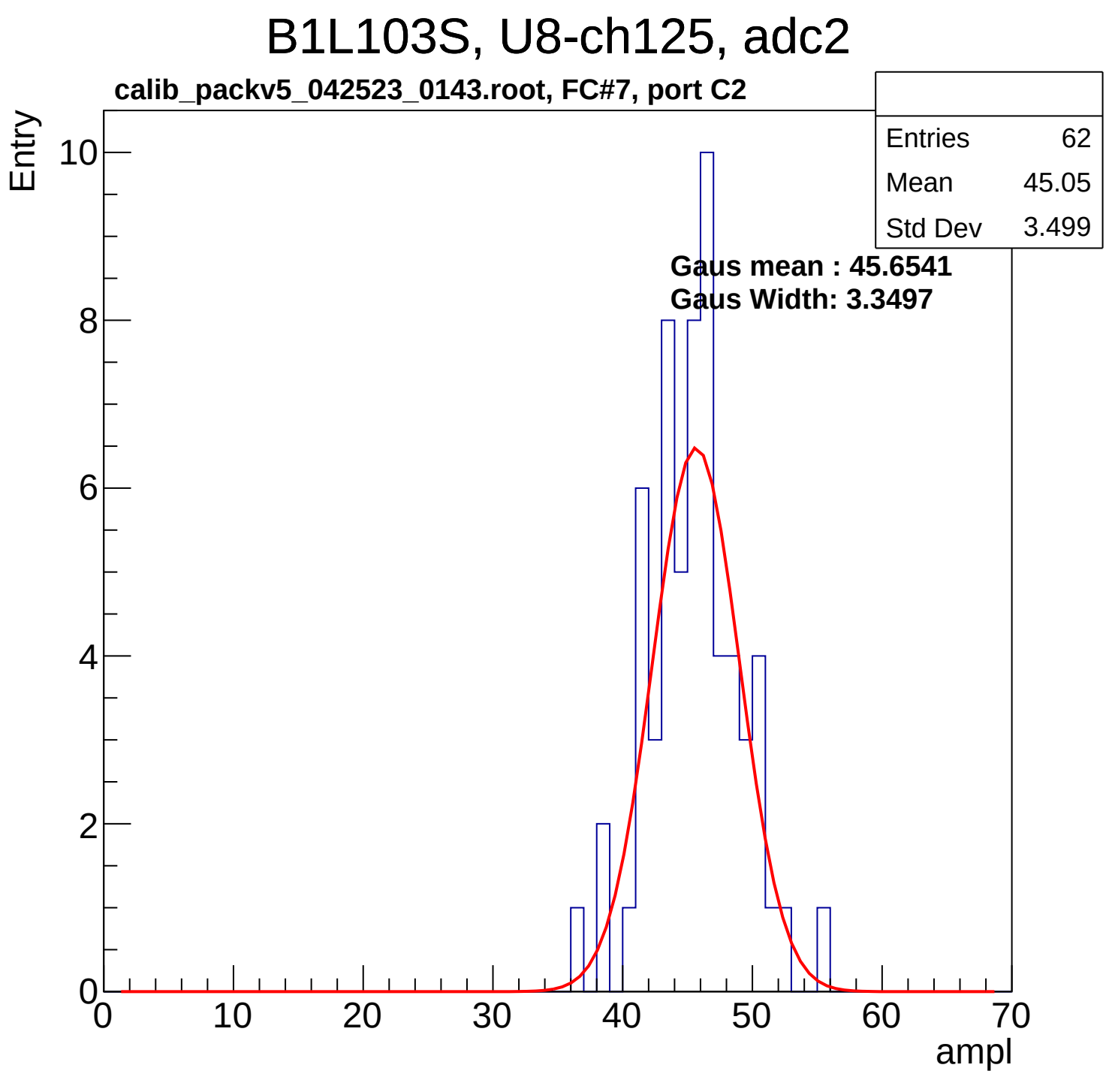

B1L103S, U8-ch124, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 39
Mean 59.62
Std Dev 2.852
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

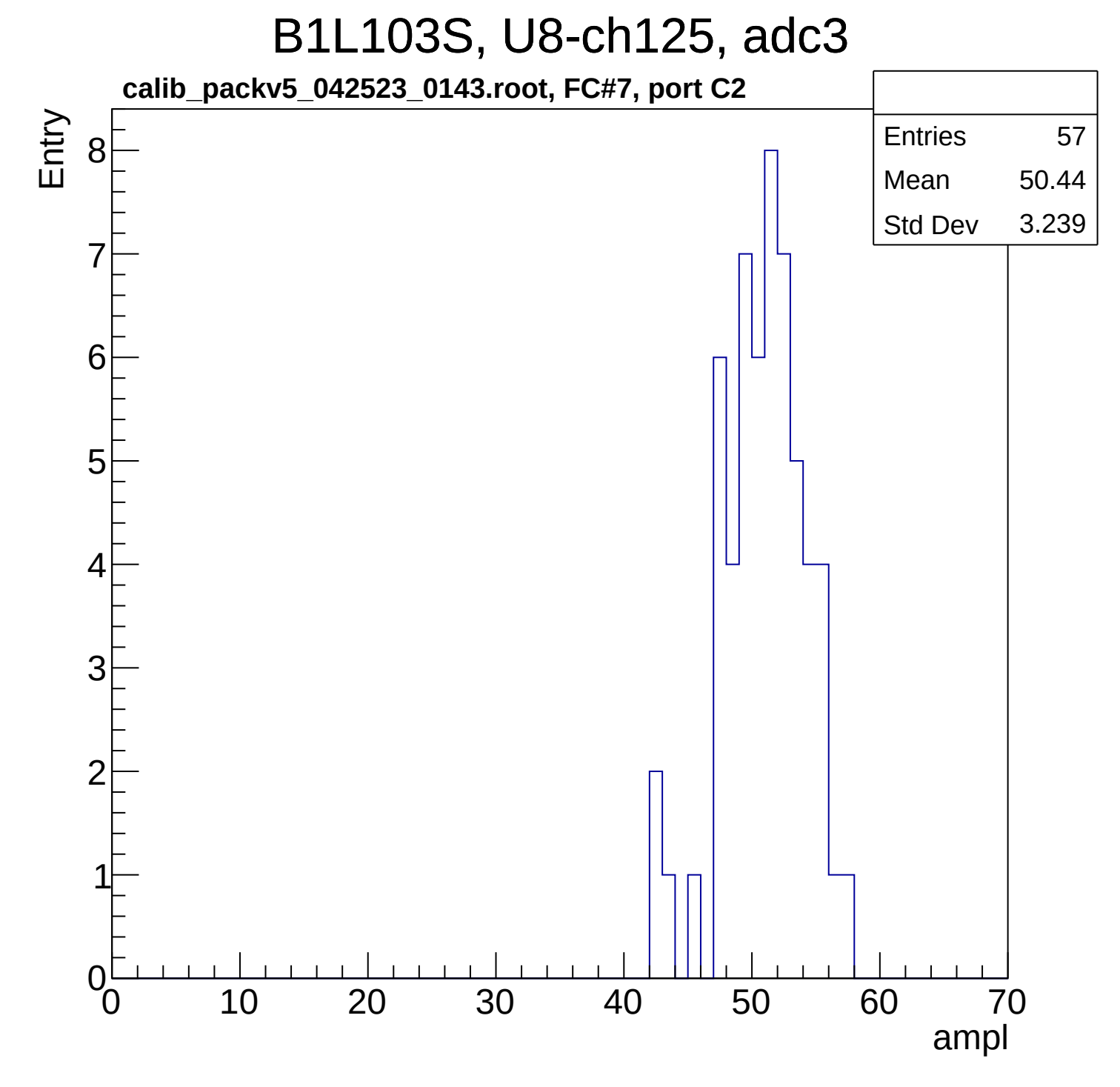

B1L103S, U8-ch124, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 9
Mean 55
Std Dev 19.47
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

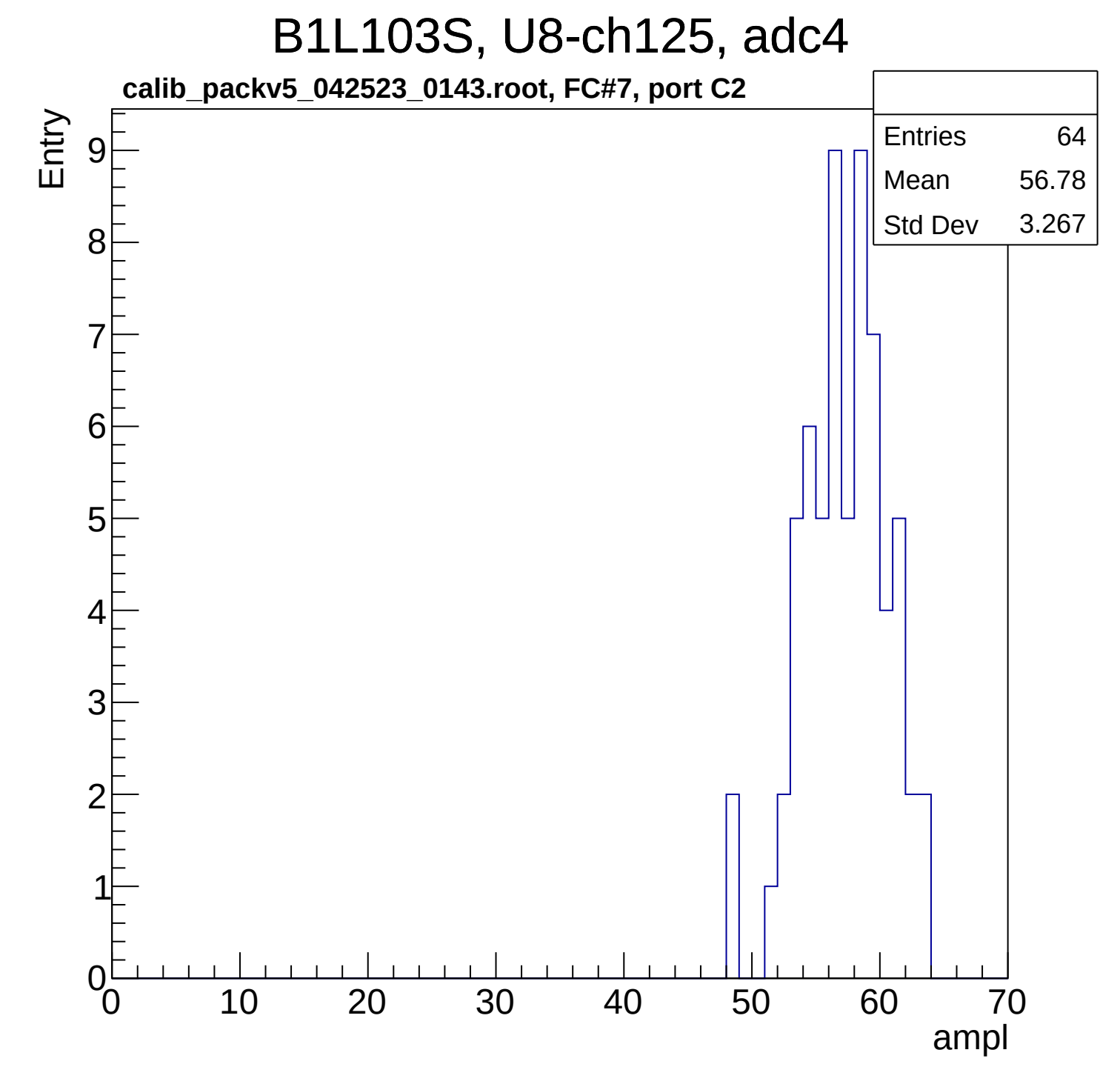

B1L103S, U8-ch124, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

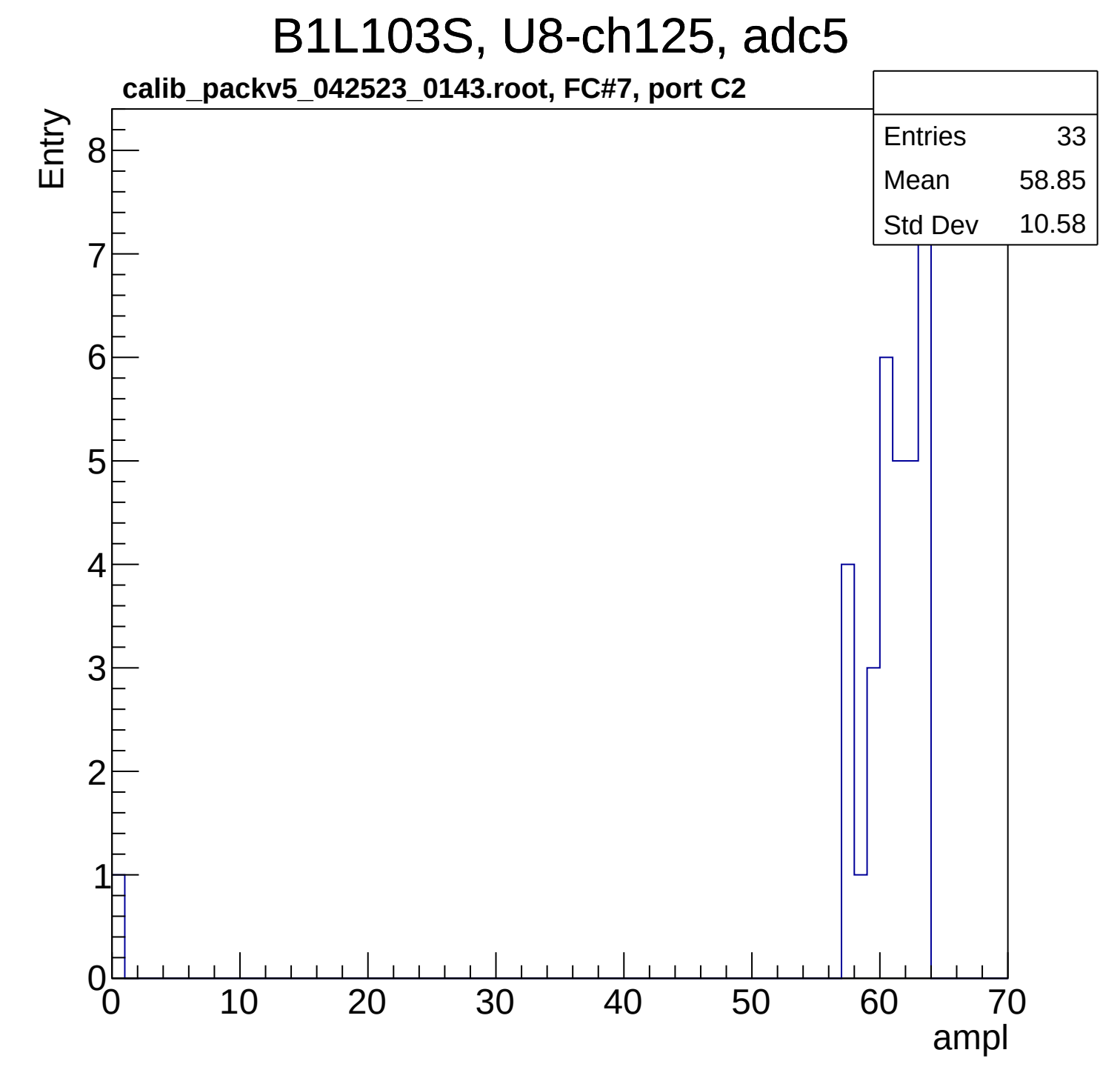

B1L103S, U8-ch125, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 81
Mean 29.75
Std Dev 5.117
Gaus mean : 30.9549
Gaus Width: 3.8822
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

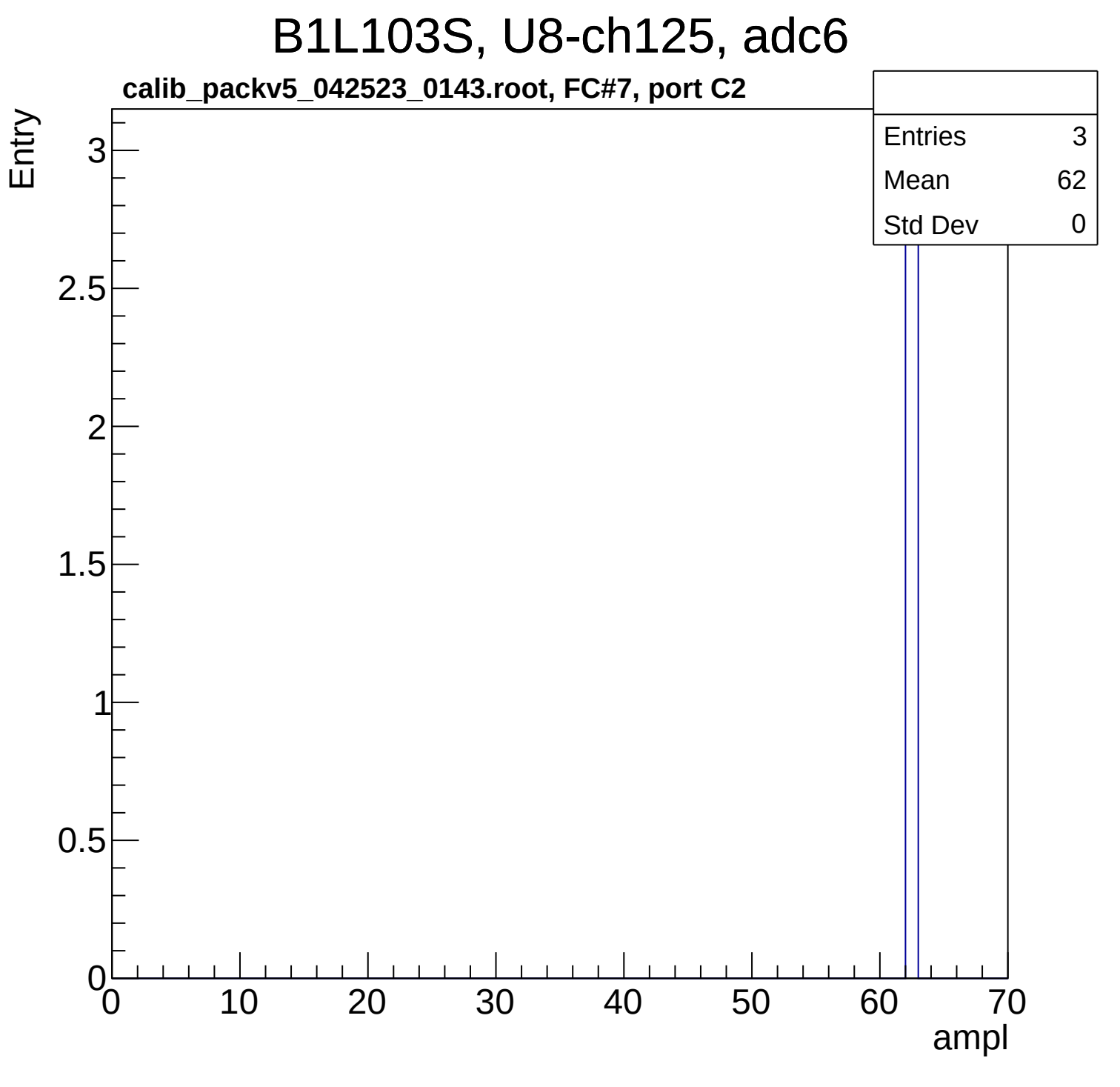

B1L103S, U8-ch125, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 37.65
Std Dev 3.614
Gaus mean : 37.8254
Gaus Width: 3.7950
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

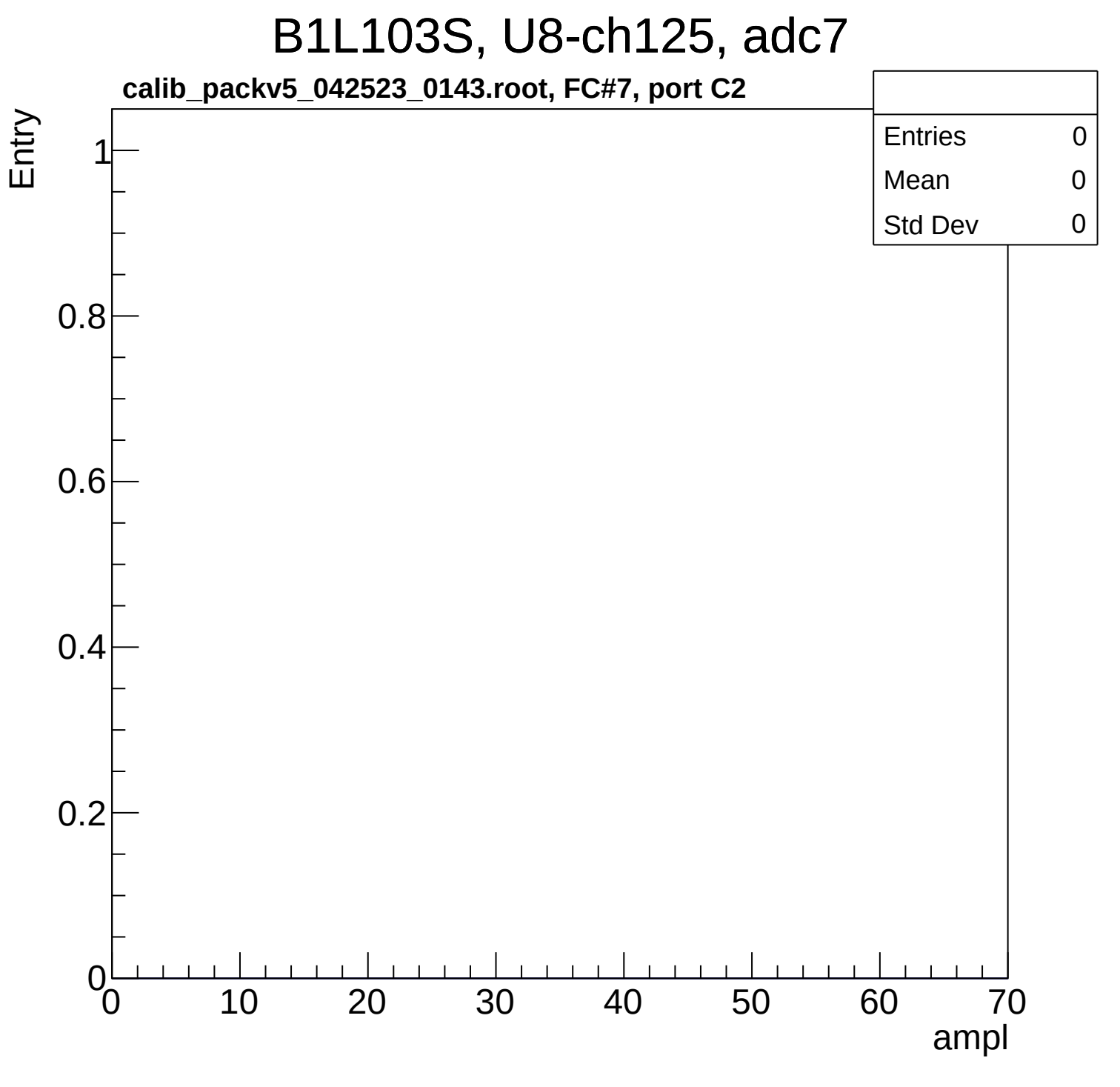

B1L103S, U8-ch125, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 62
Mean 45.05
Std Dev 3.499
Gaus mean : 45.6541
Gaus Width: 3.3497
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

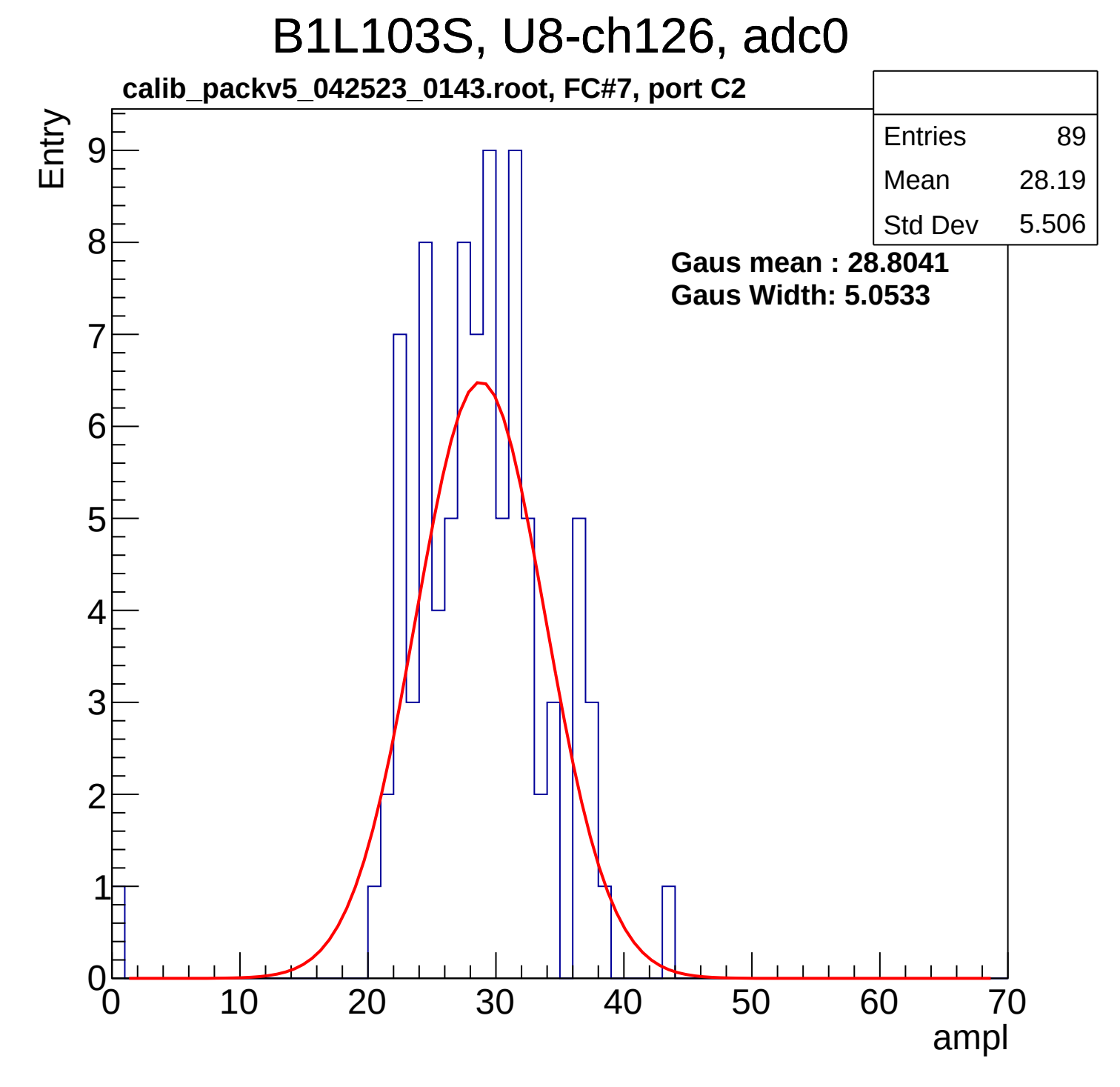

B1L103S, U8-ch125, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 57
Mean 50.44
Std Dev 3.239
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

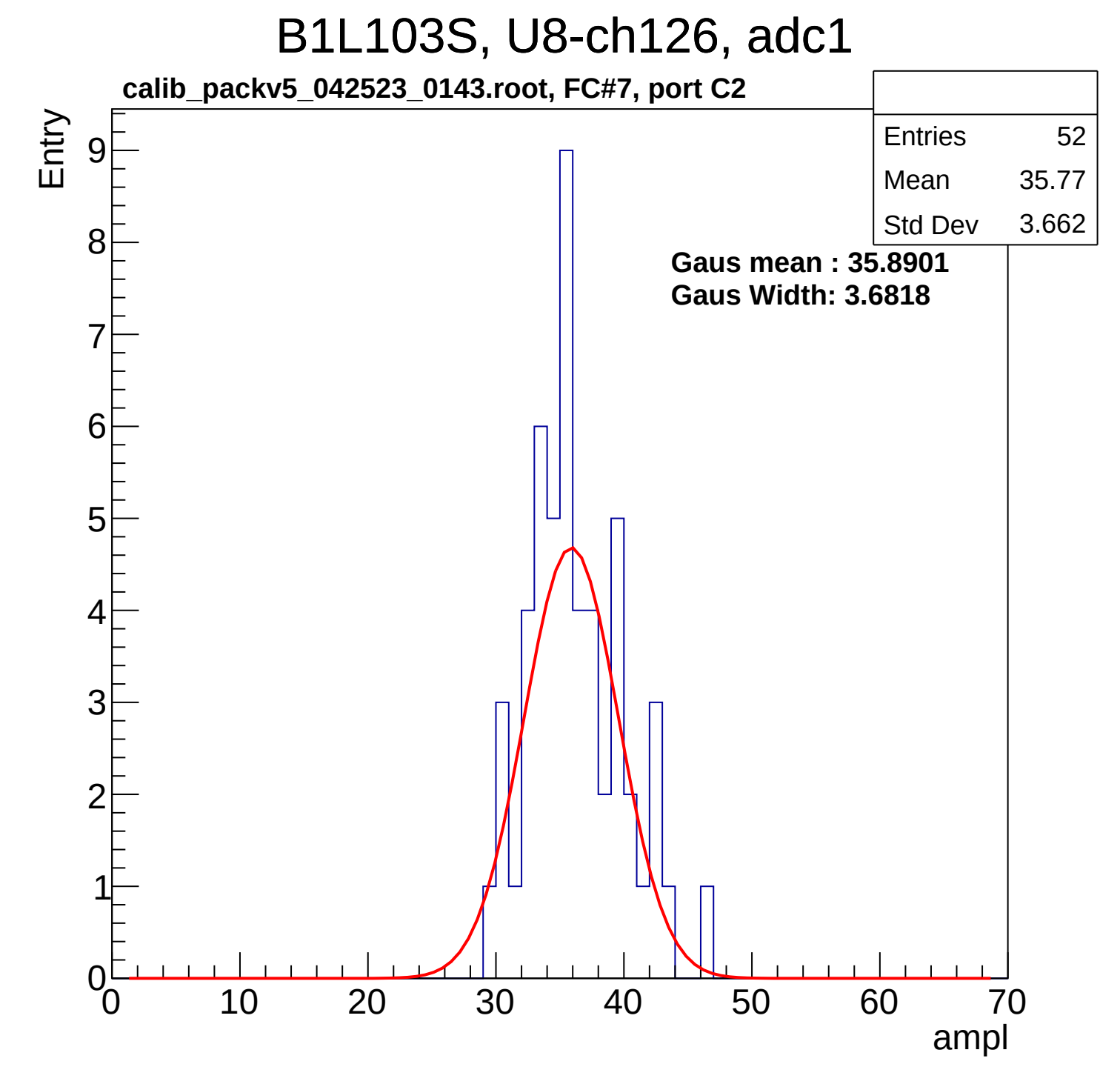

B1L103S, U8-ch125, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 56.78
Std Dev 3.267
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

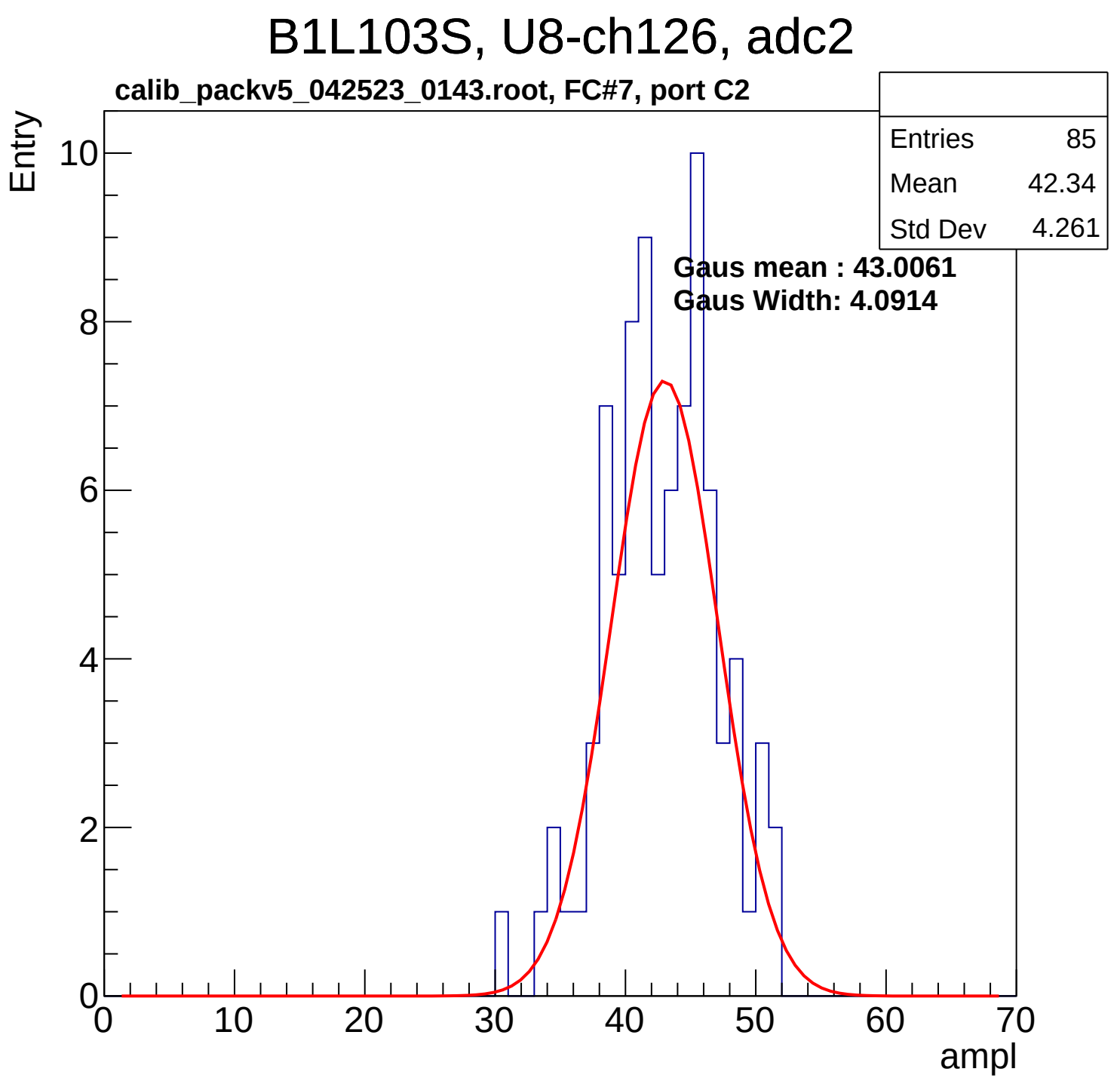

B1L103S, U8-ch125, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 33
Mean 58.85
Std Dev 10.58
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

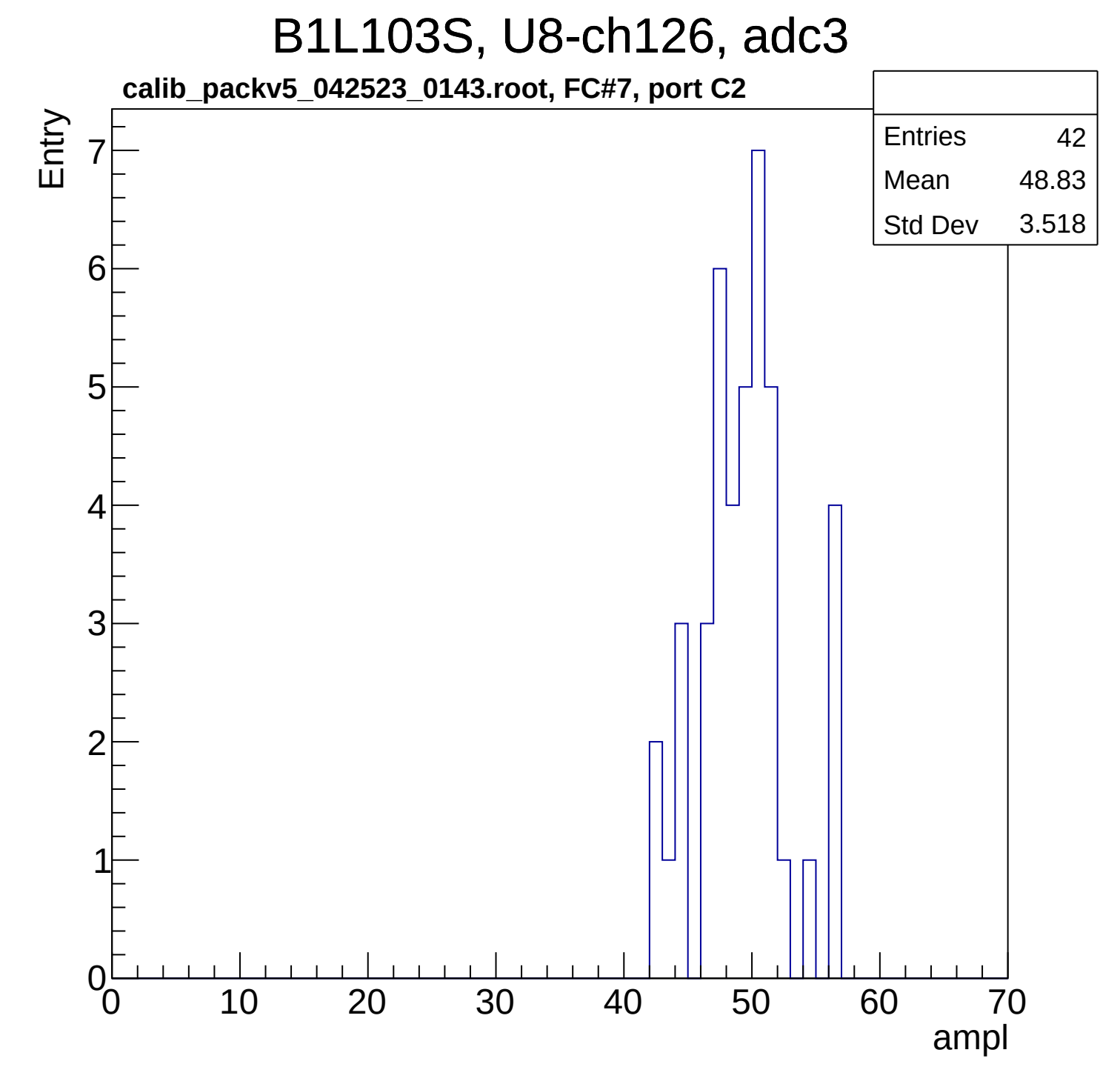

B1L103S, U8-ch125, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 3
Mean 62
Std Dev 0
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

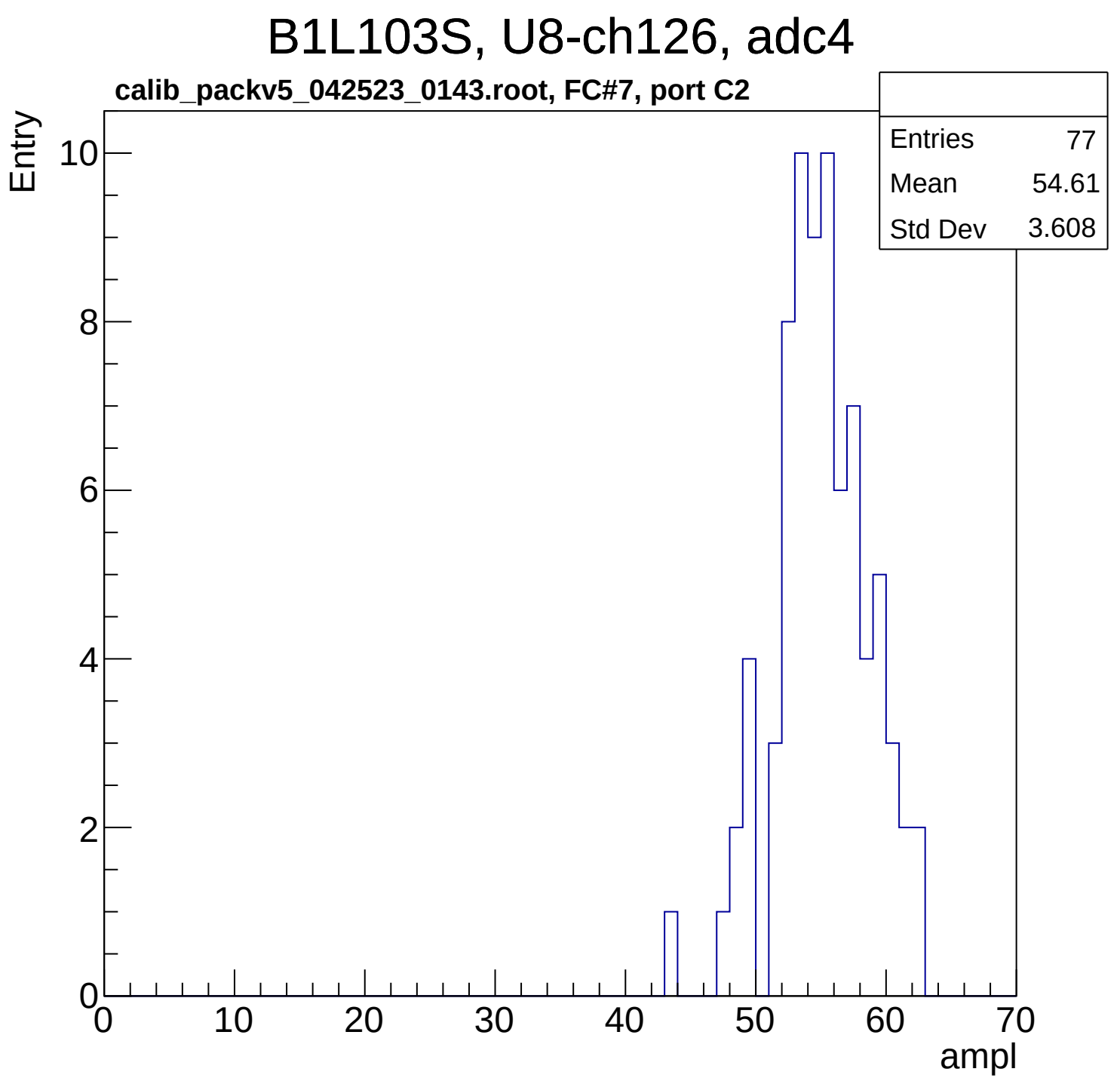

B1L103S, U8-ch125, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

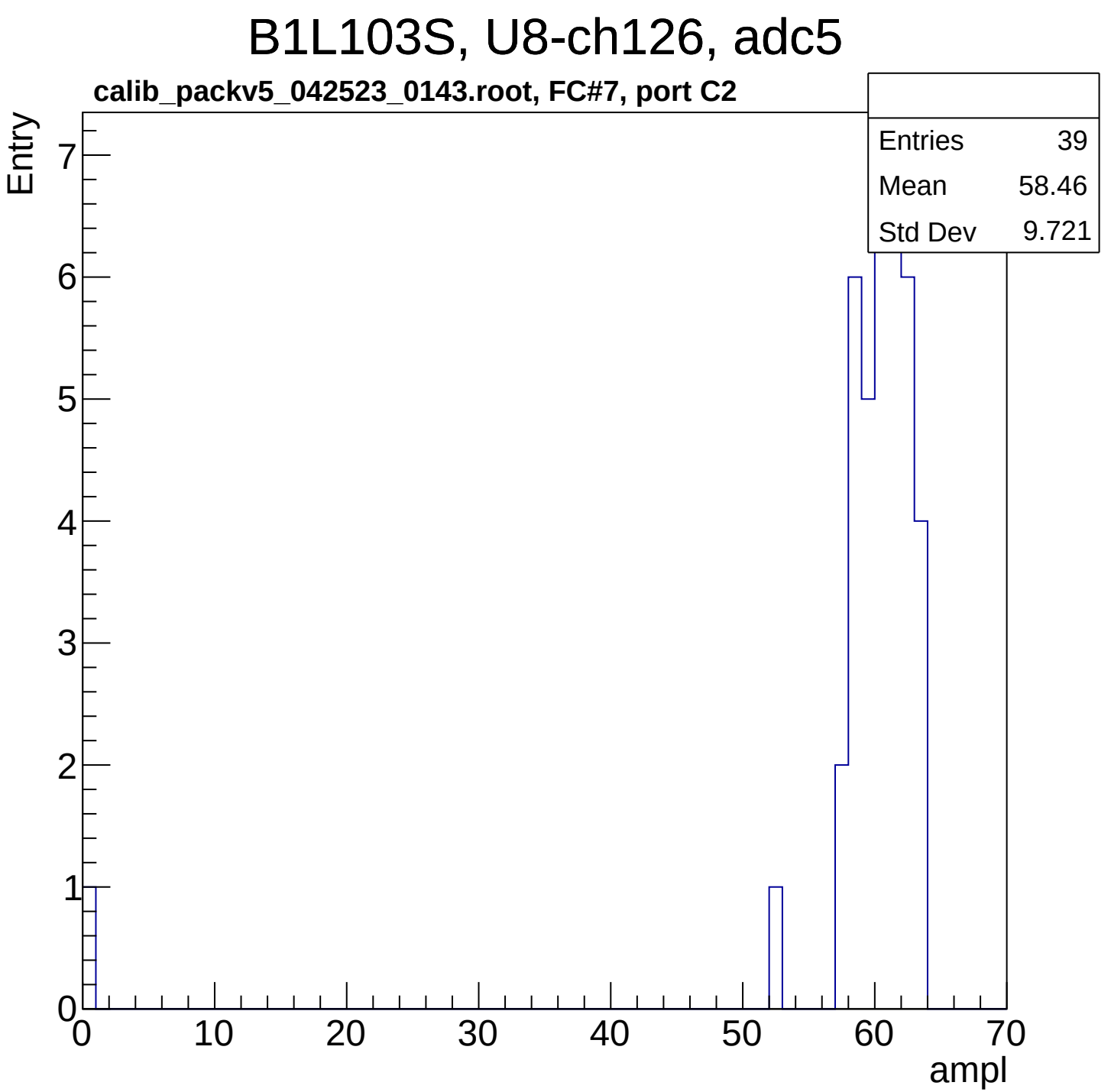

B1L103S, U8-ch126, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 89
Mean 28.19
Std Dev 5.506
Gaus mean : 28.8041
Gaus Width: 5.0533
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

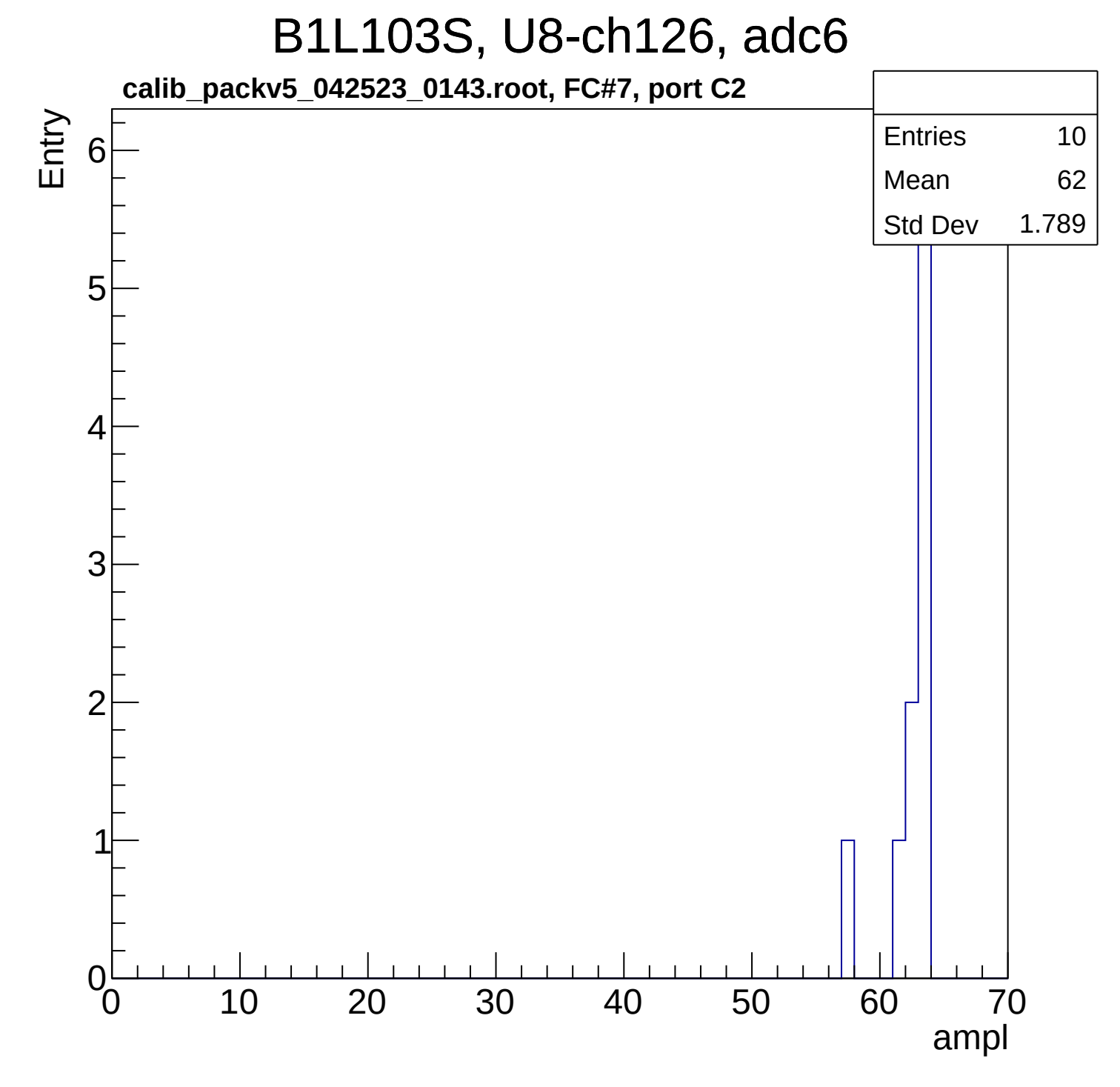

B1L103S, U8-ch126, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 52
Mean 35.77
Std Dev 3.662
Gaus mean : 35.8901
Gaus Width: 3.6818
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

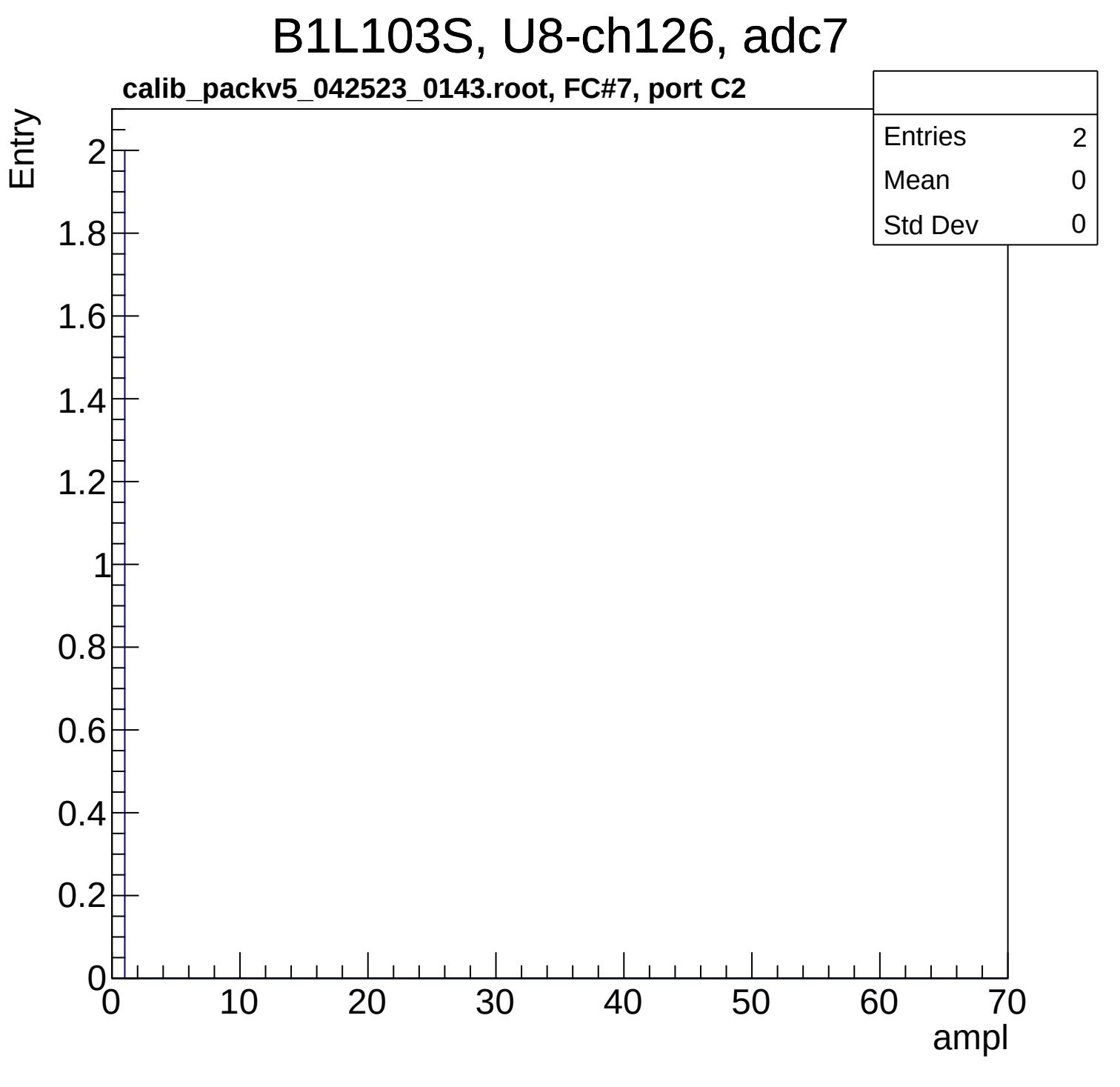

B1L103S, U8-ch126, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 85
Mean 42.34
Std Dev 4.261
Gaus mean : 43.0061
Gaus Width: 4.0914
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

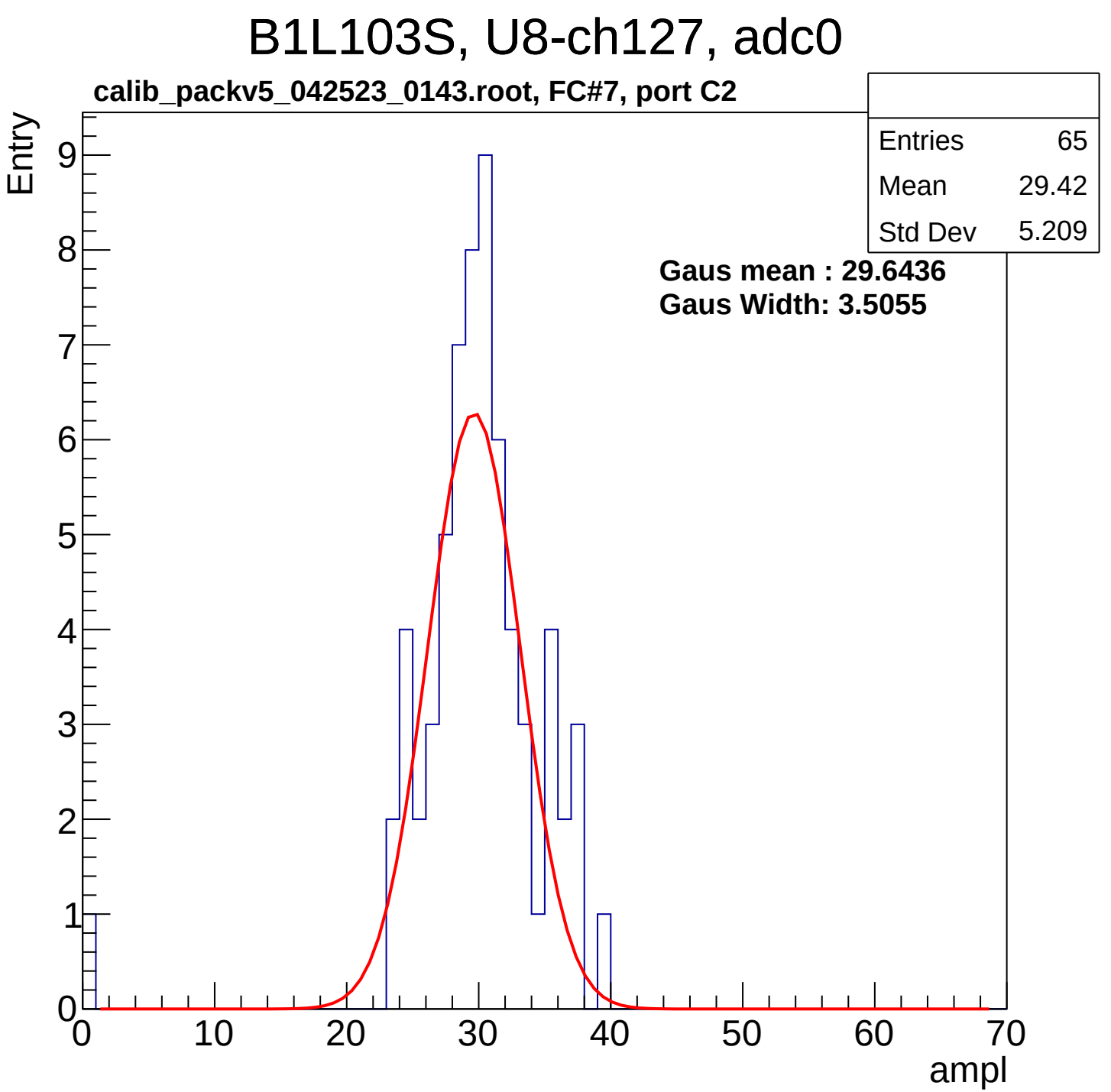

B1L103S, U8-ch126, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 42
Mean 48.83
Std Dev 3.518
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

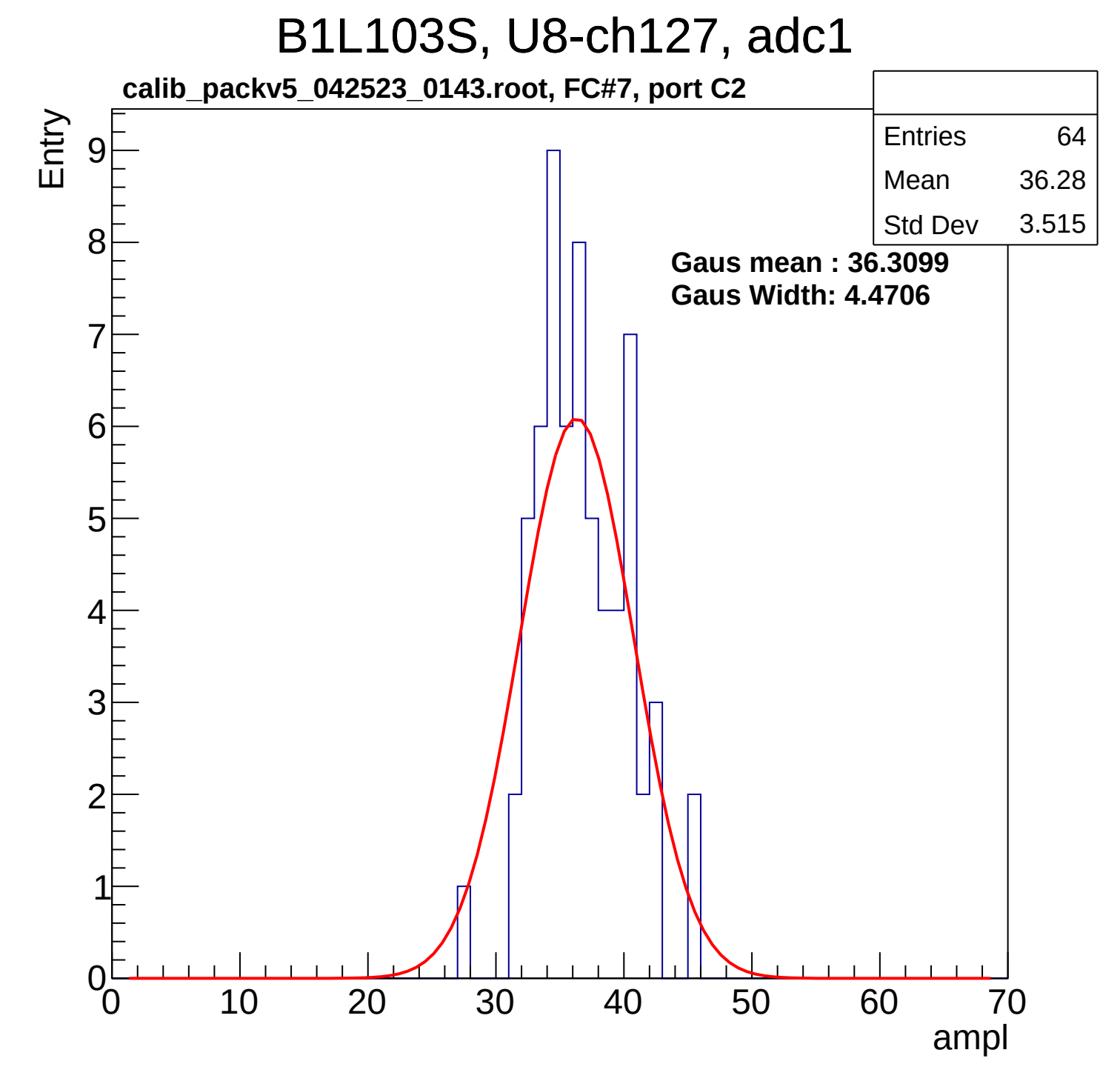

B1L103S, U8-ch126, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 77
Mean 54.61
Std Dev 3.608
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

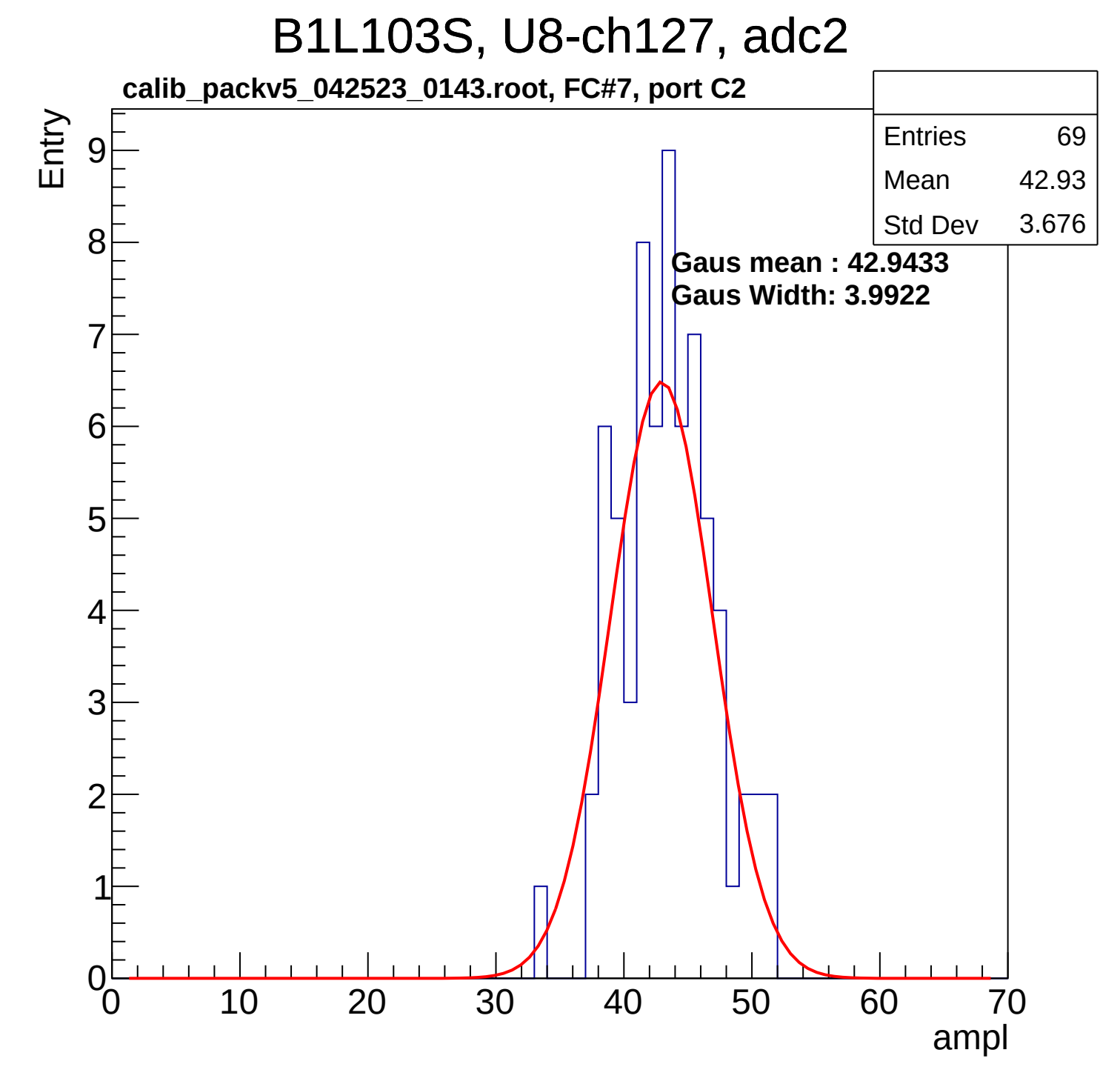

B1L103S, U8-ch126, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 39
Mean 58.46
Std Dev 9.721
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

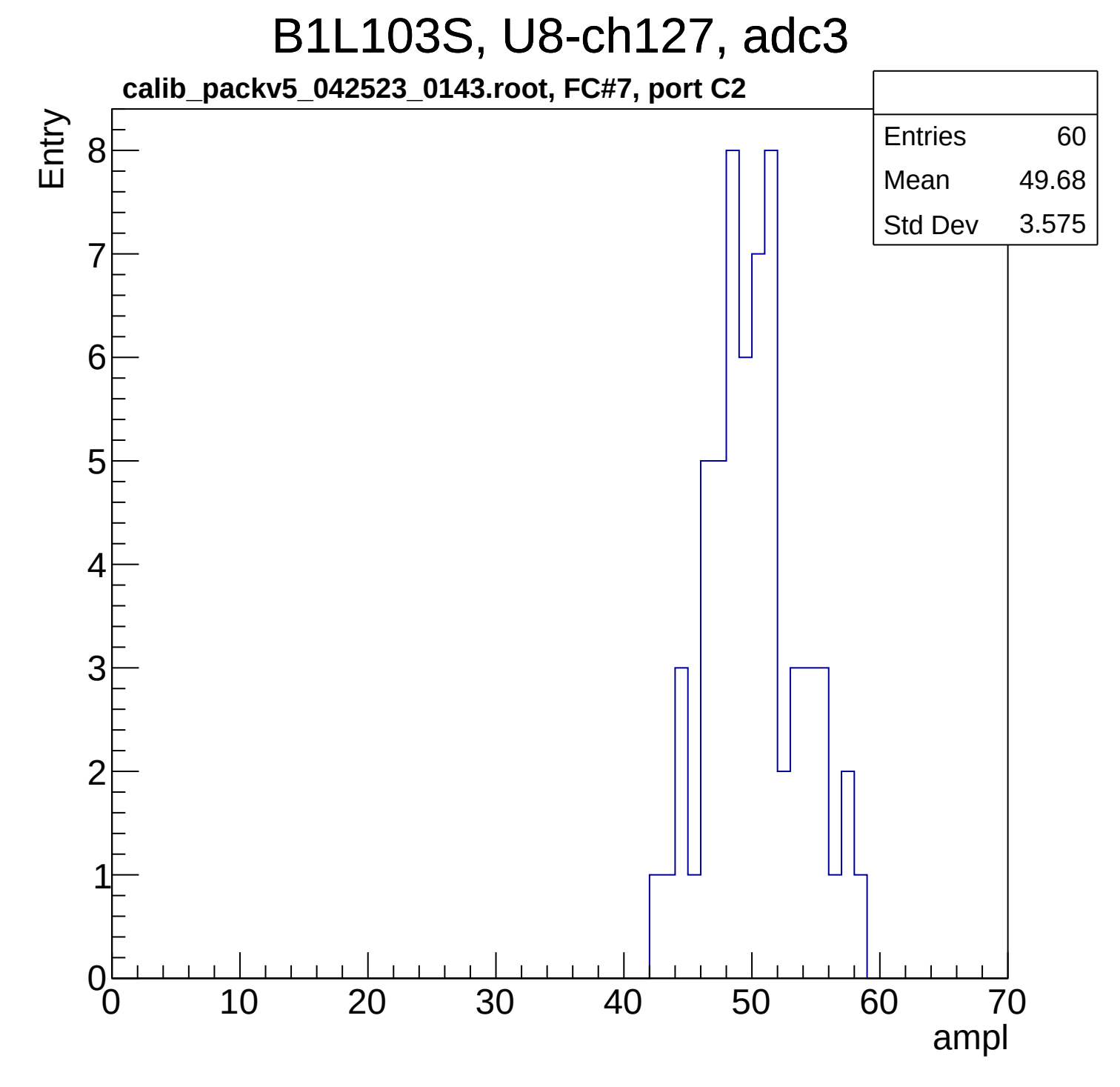

B1L103S, U8-ch126, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 10
Mean 62
Std Dev 1.789
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

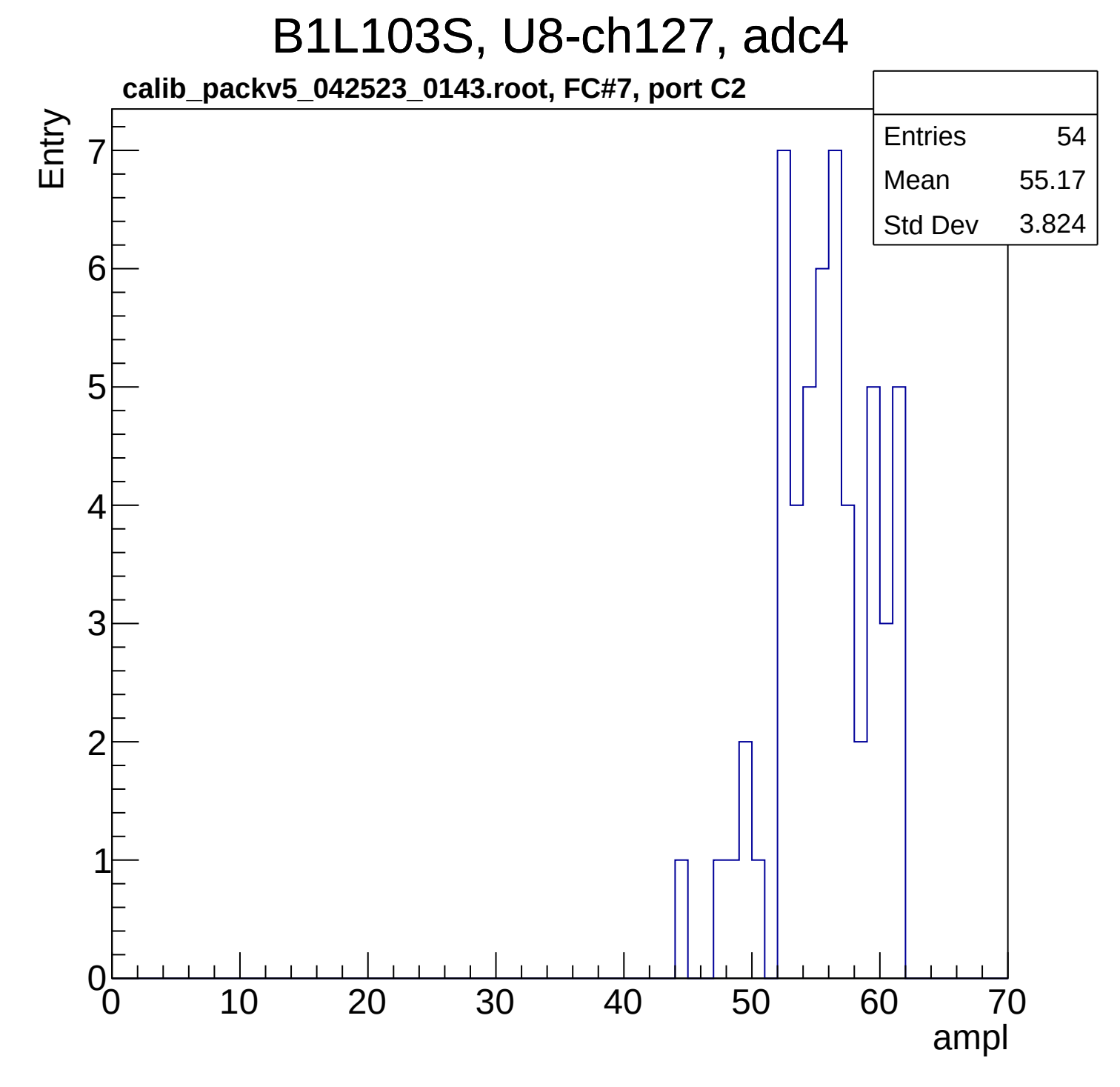

B1L103S, U8-ch126, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

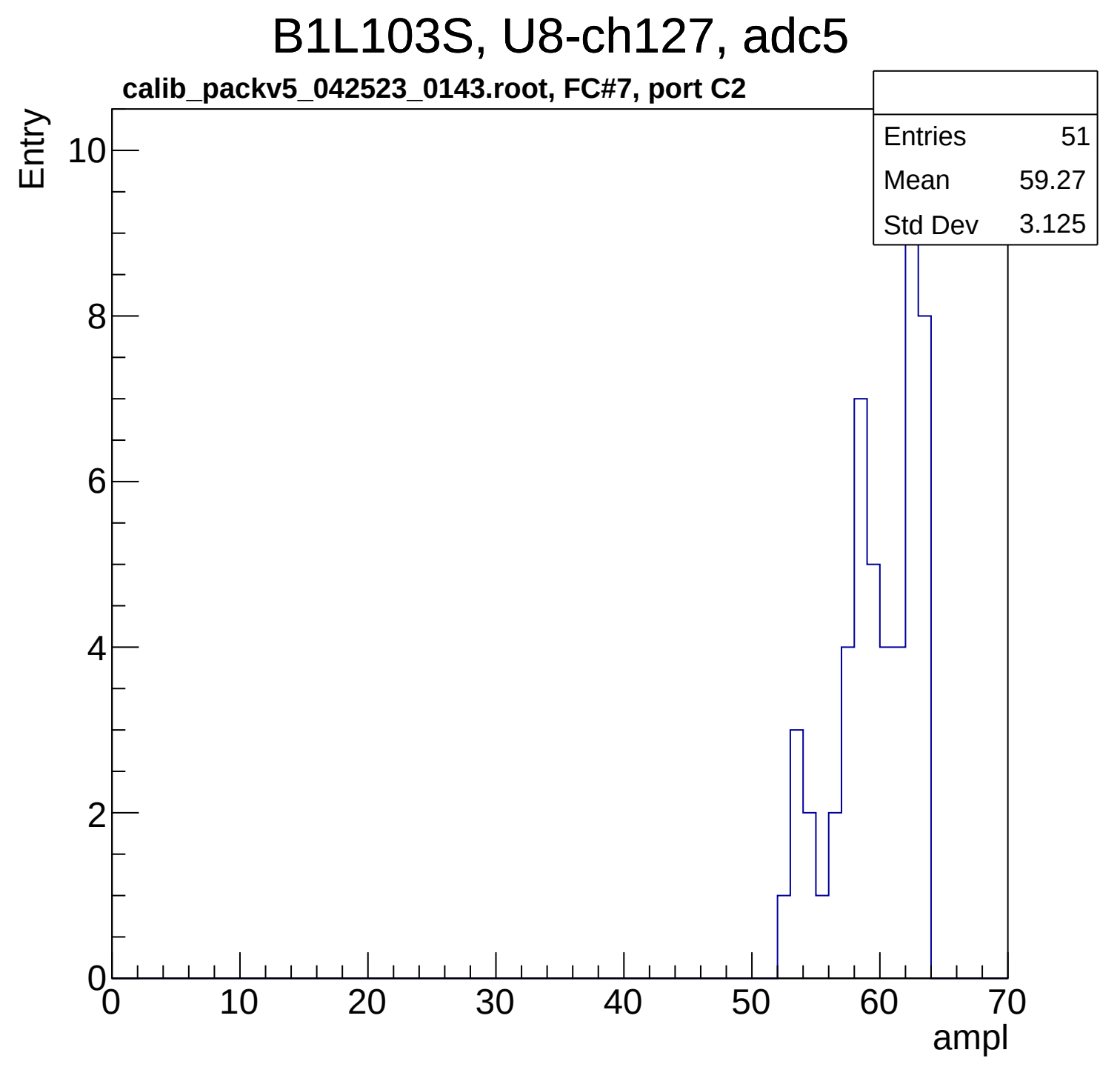

B1L103S, U8-ch127, adc0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 65
Mean 29.42
Std Dev 5.209
Gaus mean : 29.6436
Gaus Width: 3.5055
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

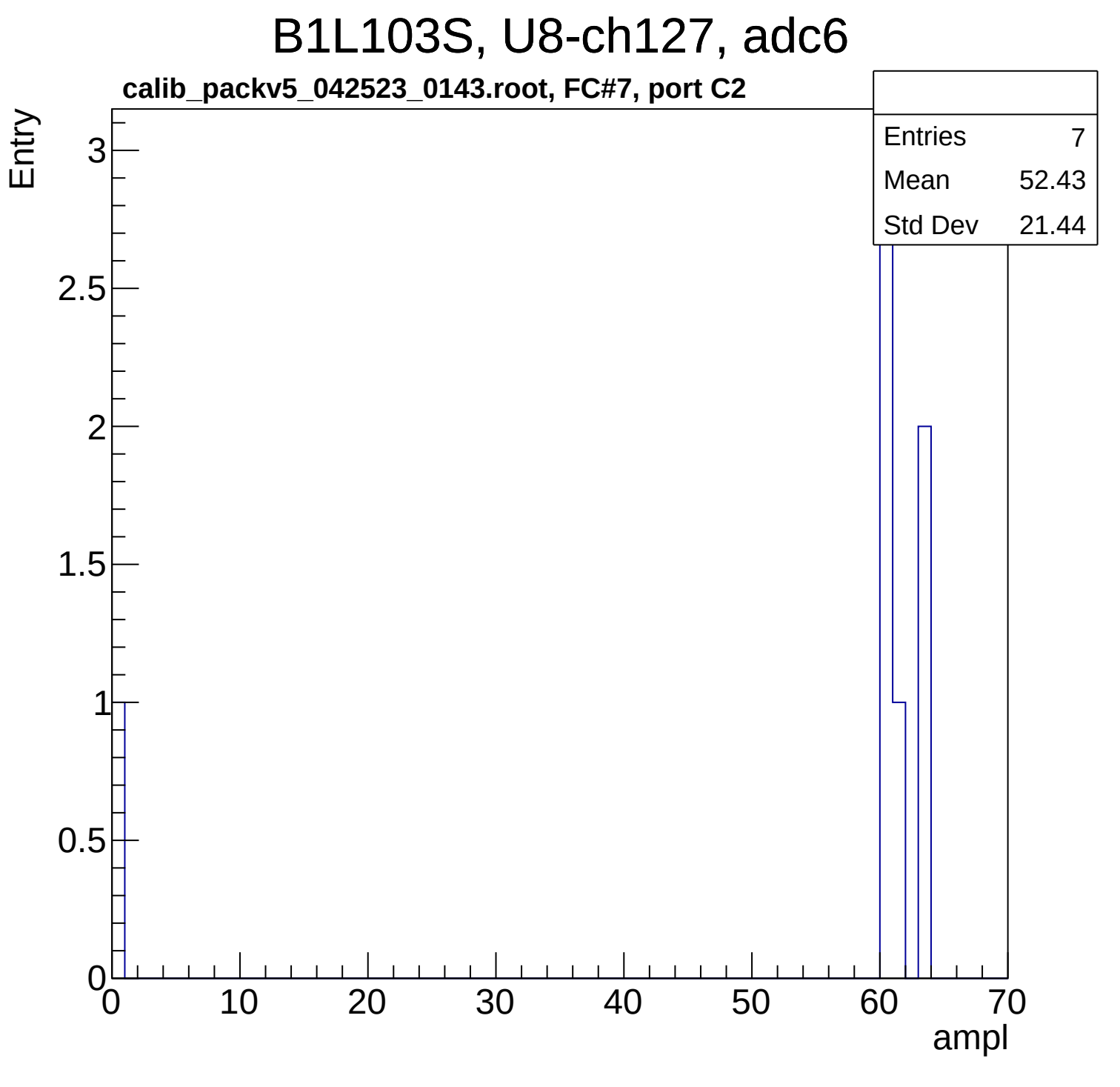

B1L103S, U8-ch127, adc1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 64
Mean 36.28
Std Dev 3.515
Gaus mean : 36.3099
Gaus Width: 4.4706
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

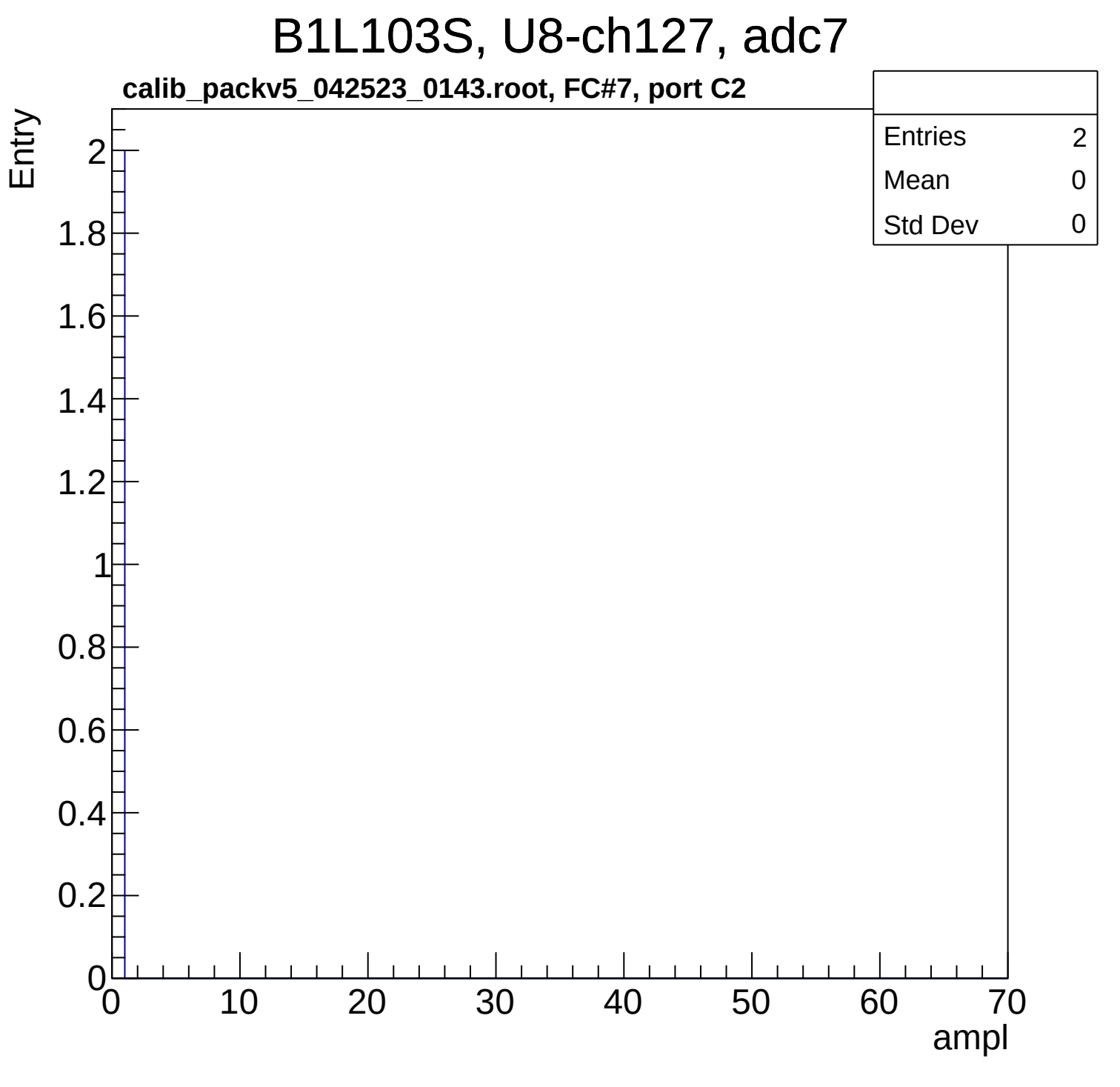

B1L103S, U8-ch127, adc2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 69
Mean 42.93
Std Dev 3.676
Gaus mean : 42.9433
Gaus Width: 3.9922
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

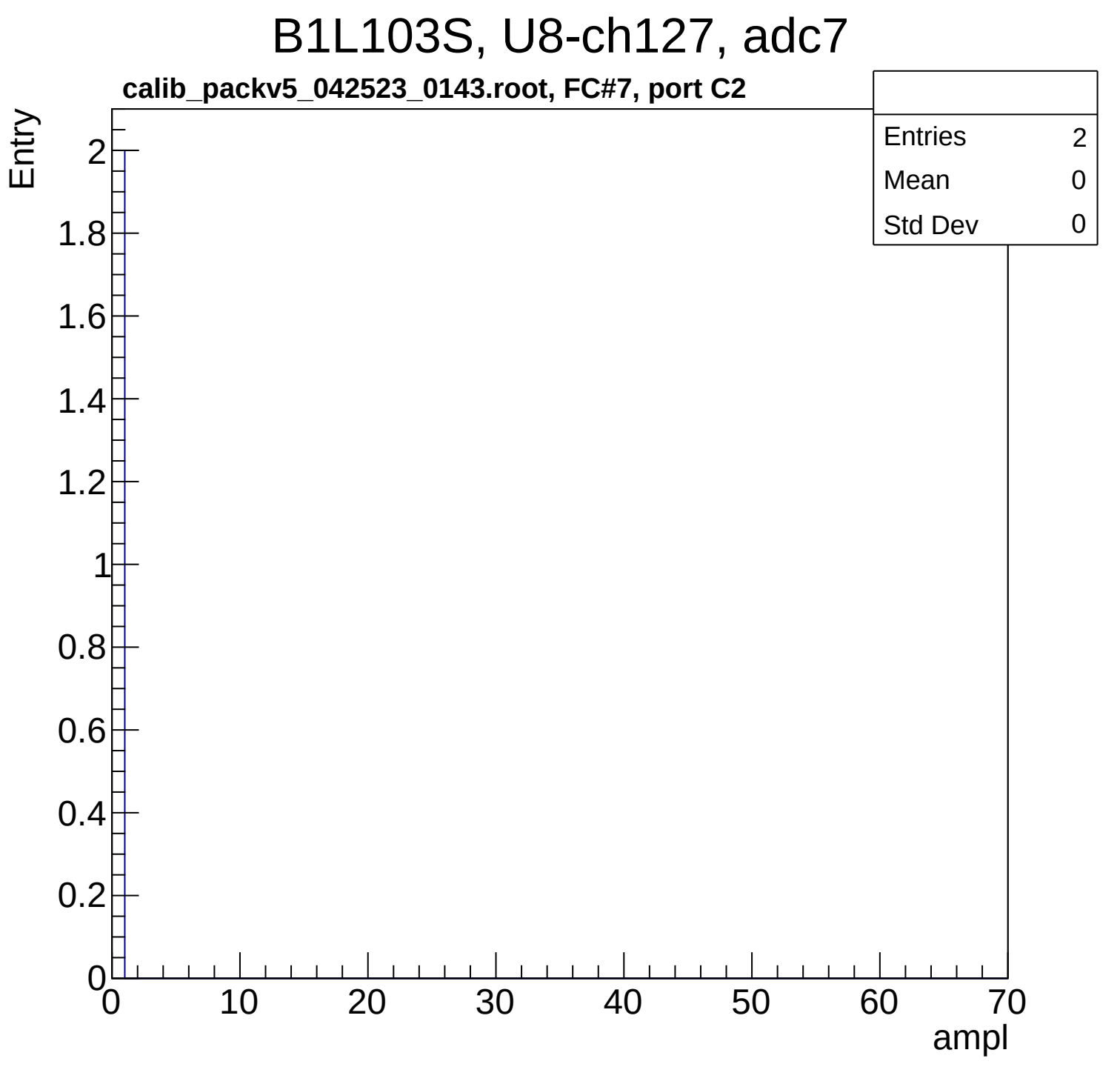

B1L103S, U8-ch127, adc3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 60
Mean 49.68
Std Dev 3.575
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U8-ch127, adc4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 54
Mean 55.17
Std Dev 3.824
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U8-ch127, adc5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 51
Mean 59.27
Std Dev 3.125
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U8-ch127, adc6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 7
Mean 52.43
Std Dev 21.44
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U8-ch127, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U8-ch127, adc7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl