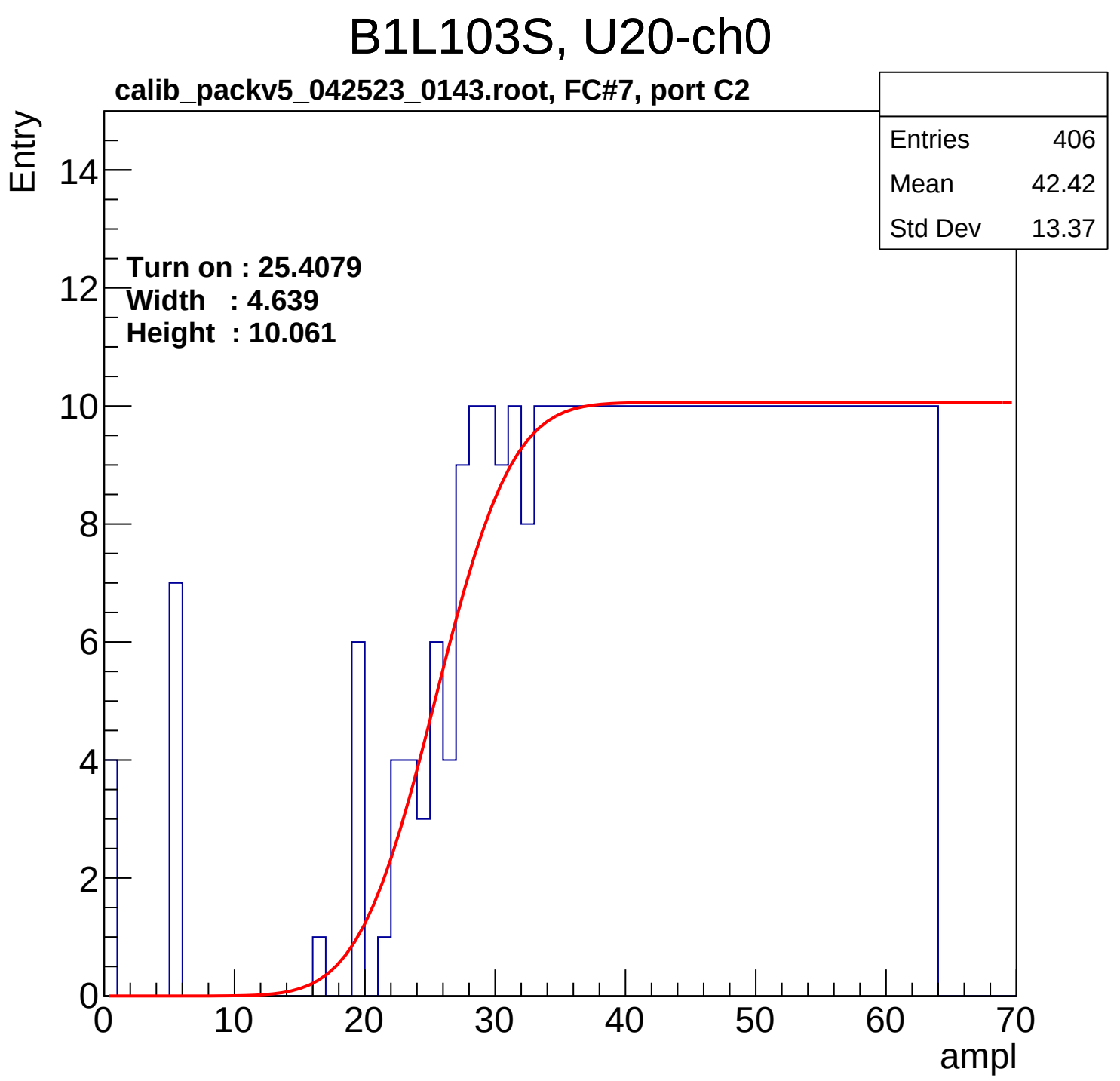
B1L103S, U20-ch0
calib_packv5_042523_0143.root, FC#7, port C2
Entries 406
Mean 42.42
Std Dev 13.37
Turn on : 25.4079
Width : 4.639
Height : 10.061
Entry
ampl
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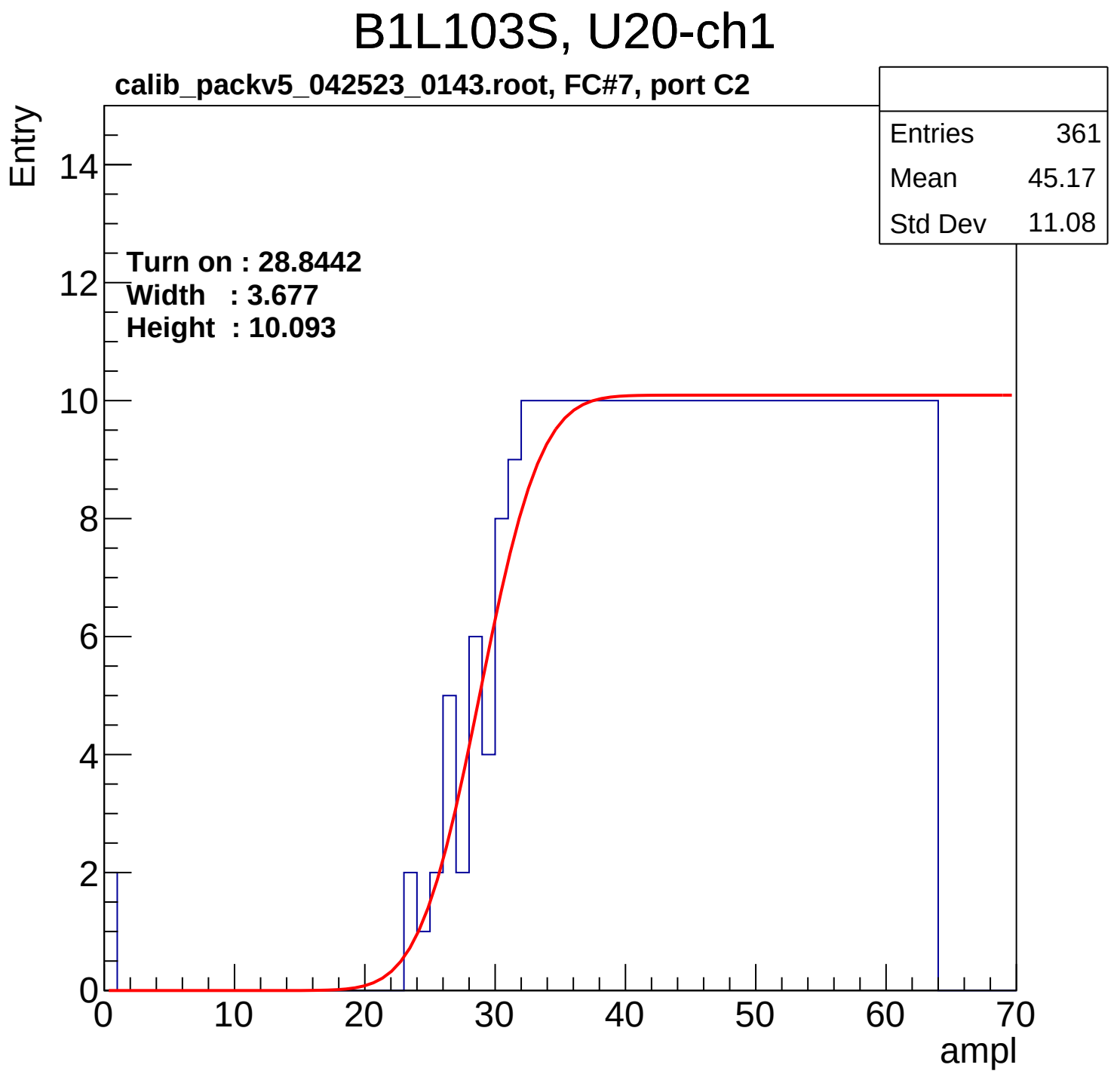
B1L103S, U20-ch1
calib_packv5_042523_0143.root, FC#7, port C2
Entries 361
Mean 45.17
Std Dev 11.08
Turn on : 28.8442
Width : 3.677
Height : 10.093
Entry
ampl
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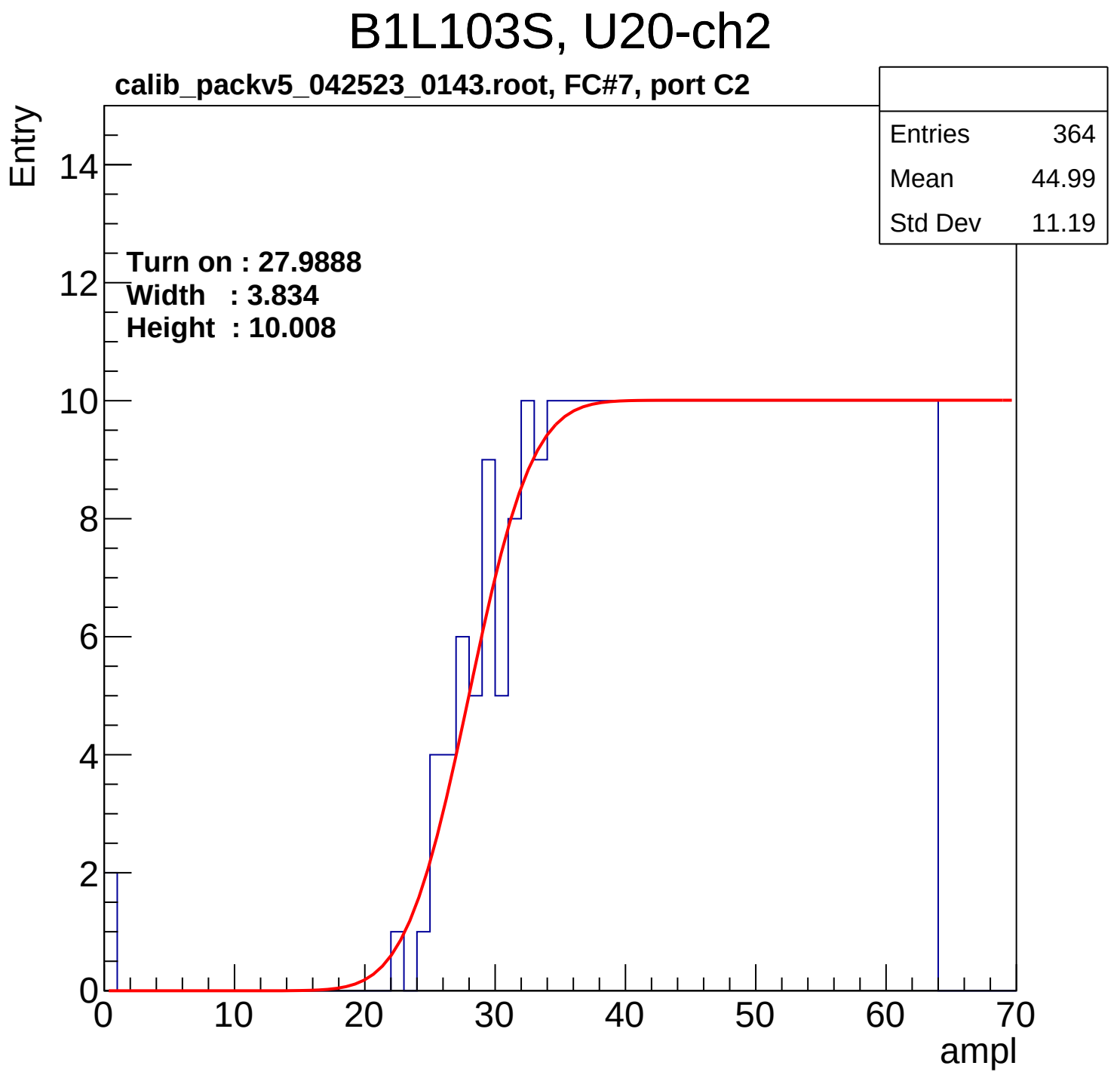
B1L103S, U20-ch2
calib_packv5_042523_0143.root, FC#7, port C2
Entries 364
Mean 44.99
Std Dev 11.19
Turn on : 27.9888
Width : 3.834
Height : 10.008
Entry
ampl
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2
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6
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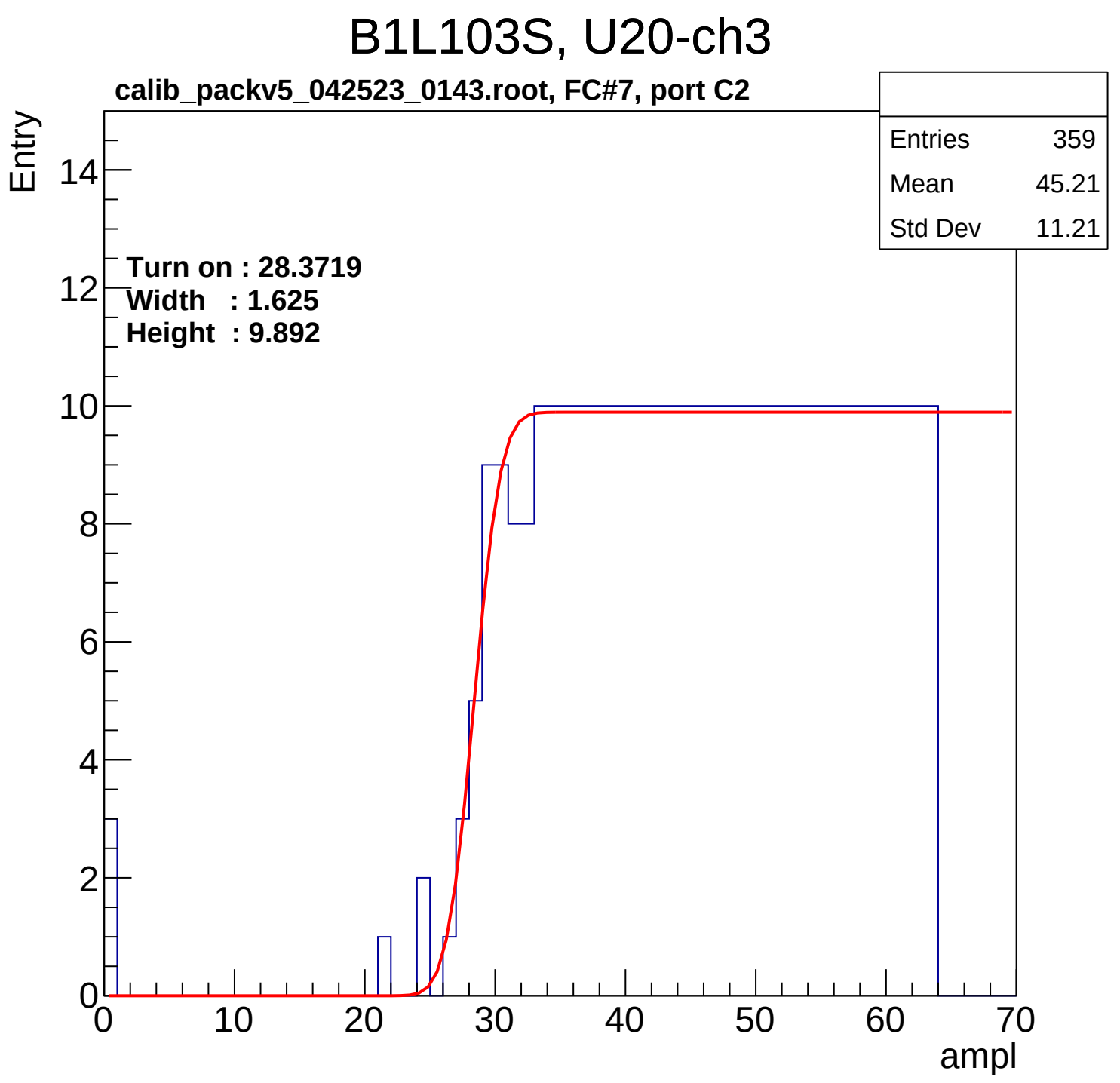
B1L103S, U20-ch3
calib_packv5_042523_0143.root, FC#7, port C2
Entries 359
Mean 45.21
Std Dev 11.21
Turn on : 28.3719
Width : 1.625
Height : 9.892
Entry
ampl
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2
4
6
8
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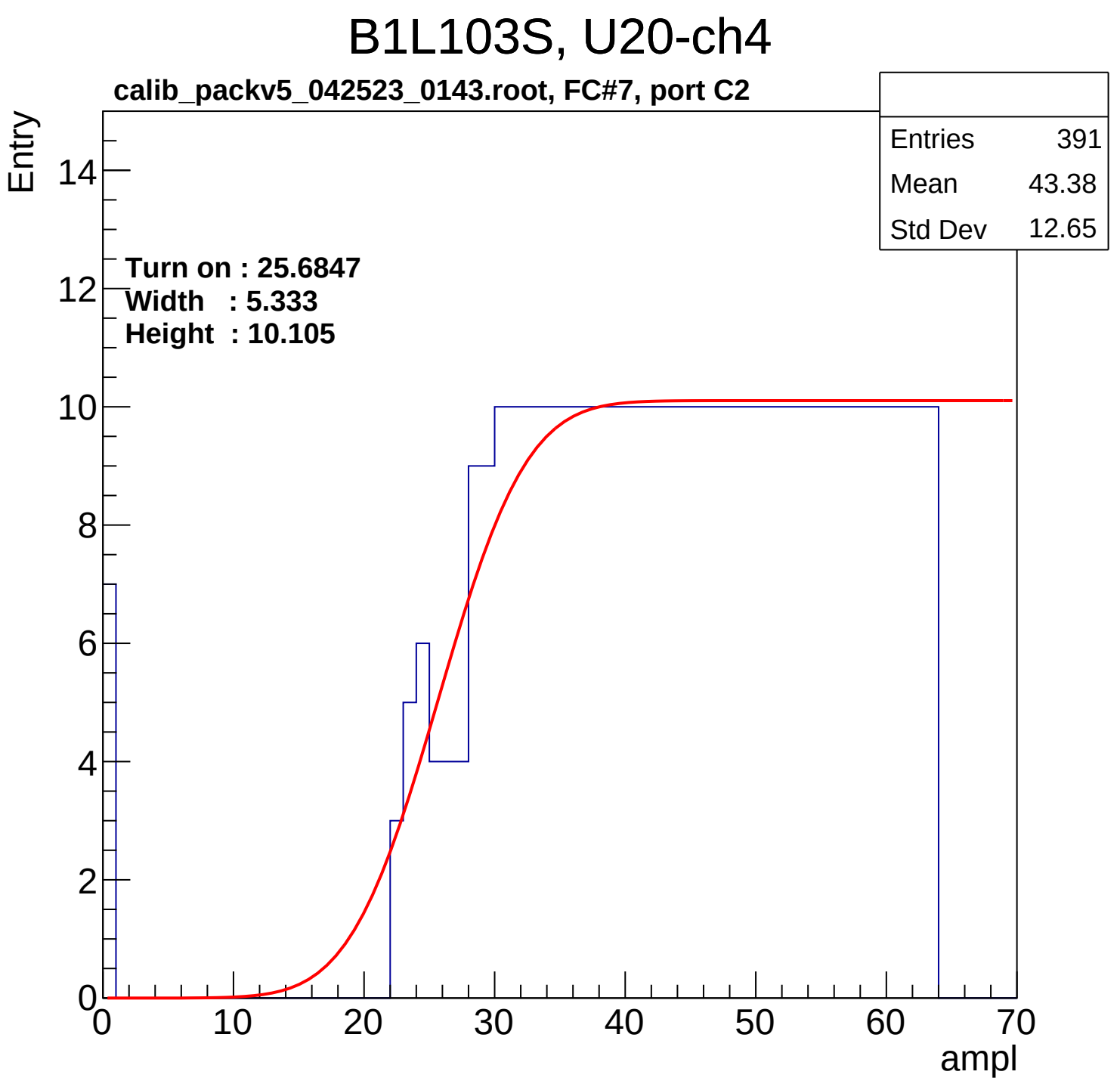
B1L103S, U20-ch4
calib_packv5_042523_0143.root, FC#7, port C2
Entries 391
Mean 43.38
Std Dev 12.65
Turn on : 25.6847
Width : 5.333
Height : 10.105
Entry
ampl
0
2
4
6
8
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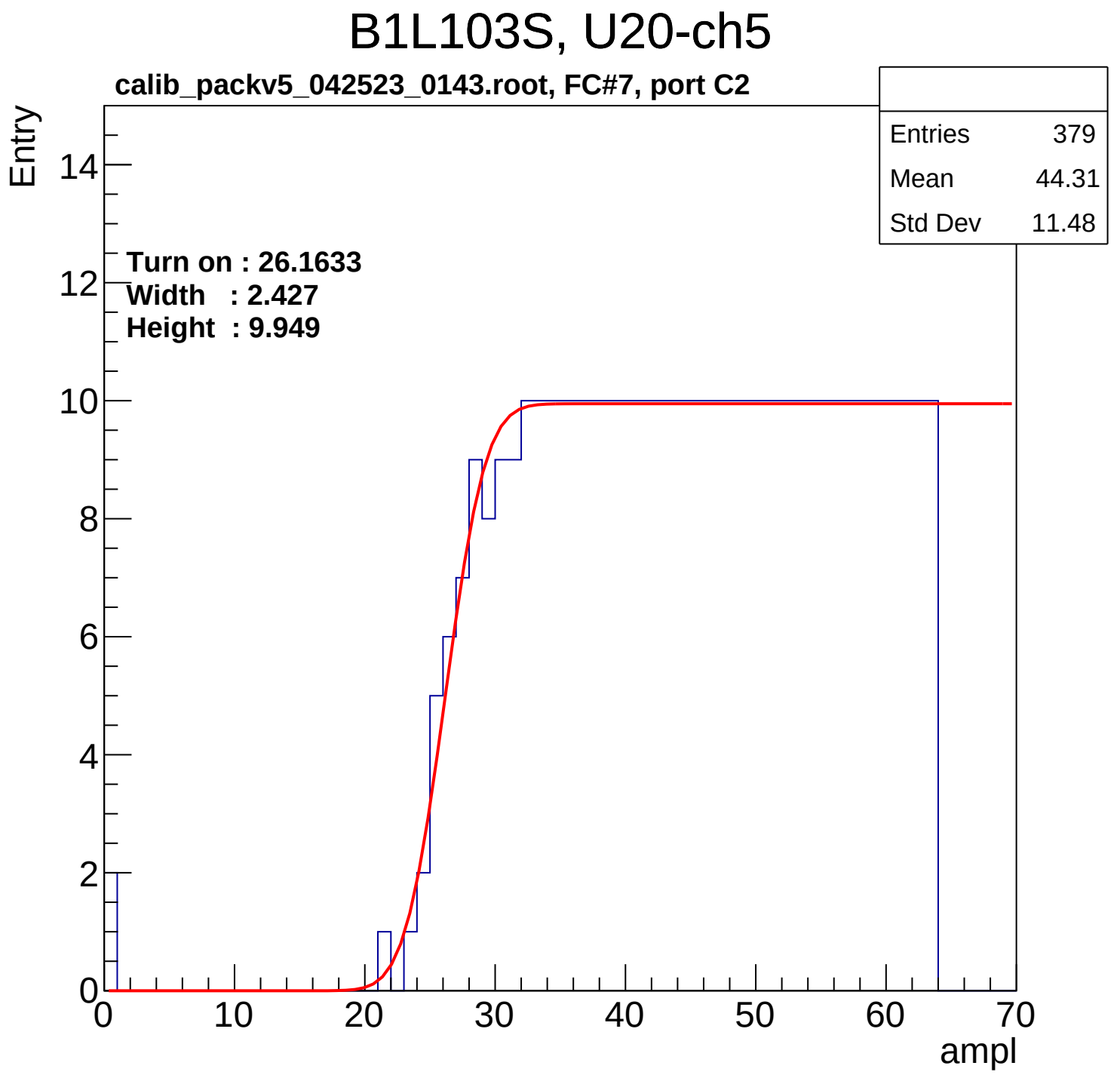
B1L103S, U20-ch5
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.31
Std Dev 11.48
Turn on : 26.1633
Width : 2.427
Height : 9.949
Entry
ampl
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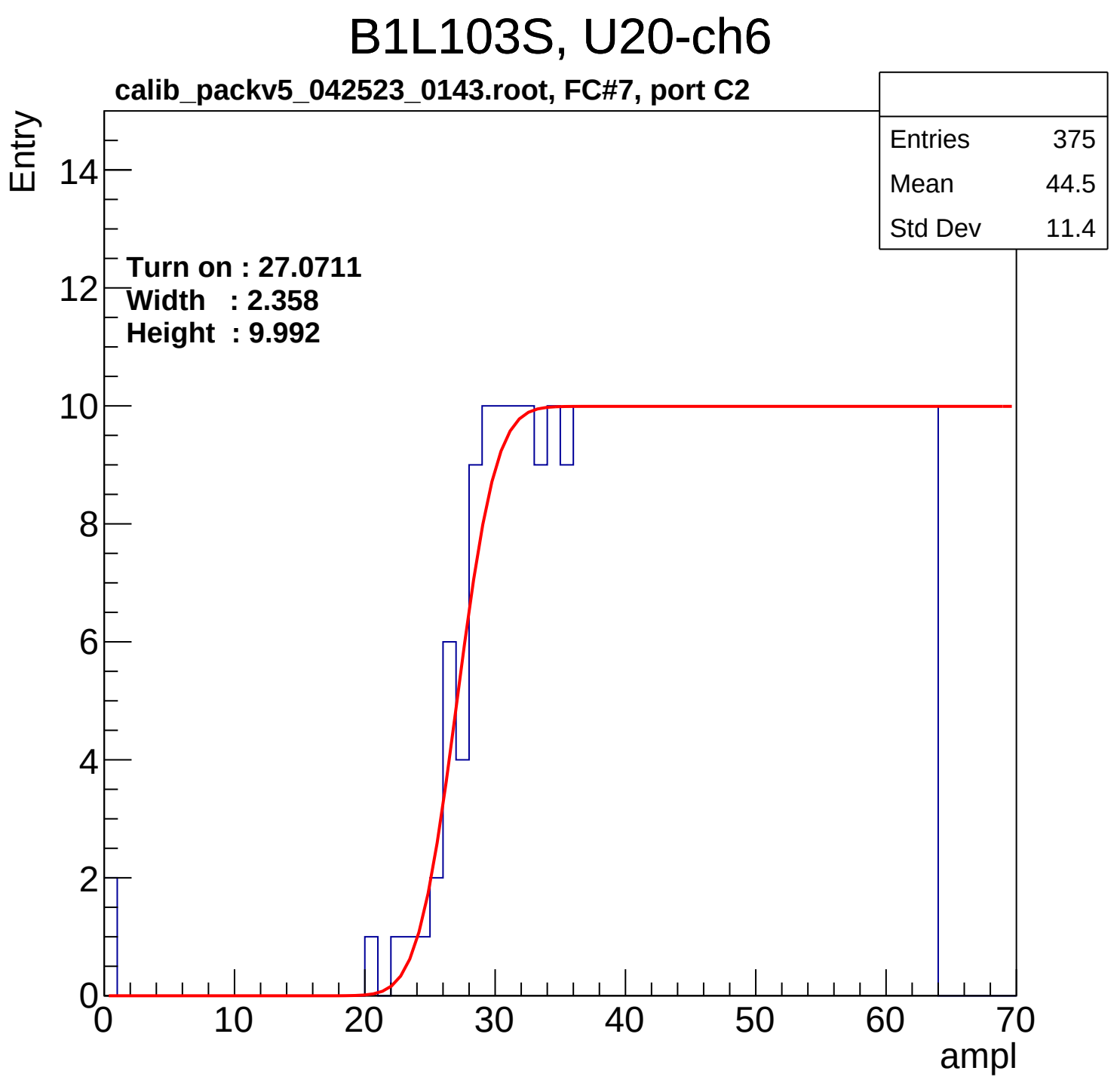
B1L103S, U20-ch6
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.5
Std Dev 11.4
Turn on : 27.0711
Width : 2.358
Height : 9.992
Entry
ampl
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2
4
6
8
10
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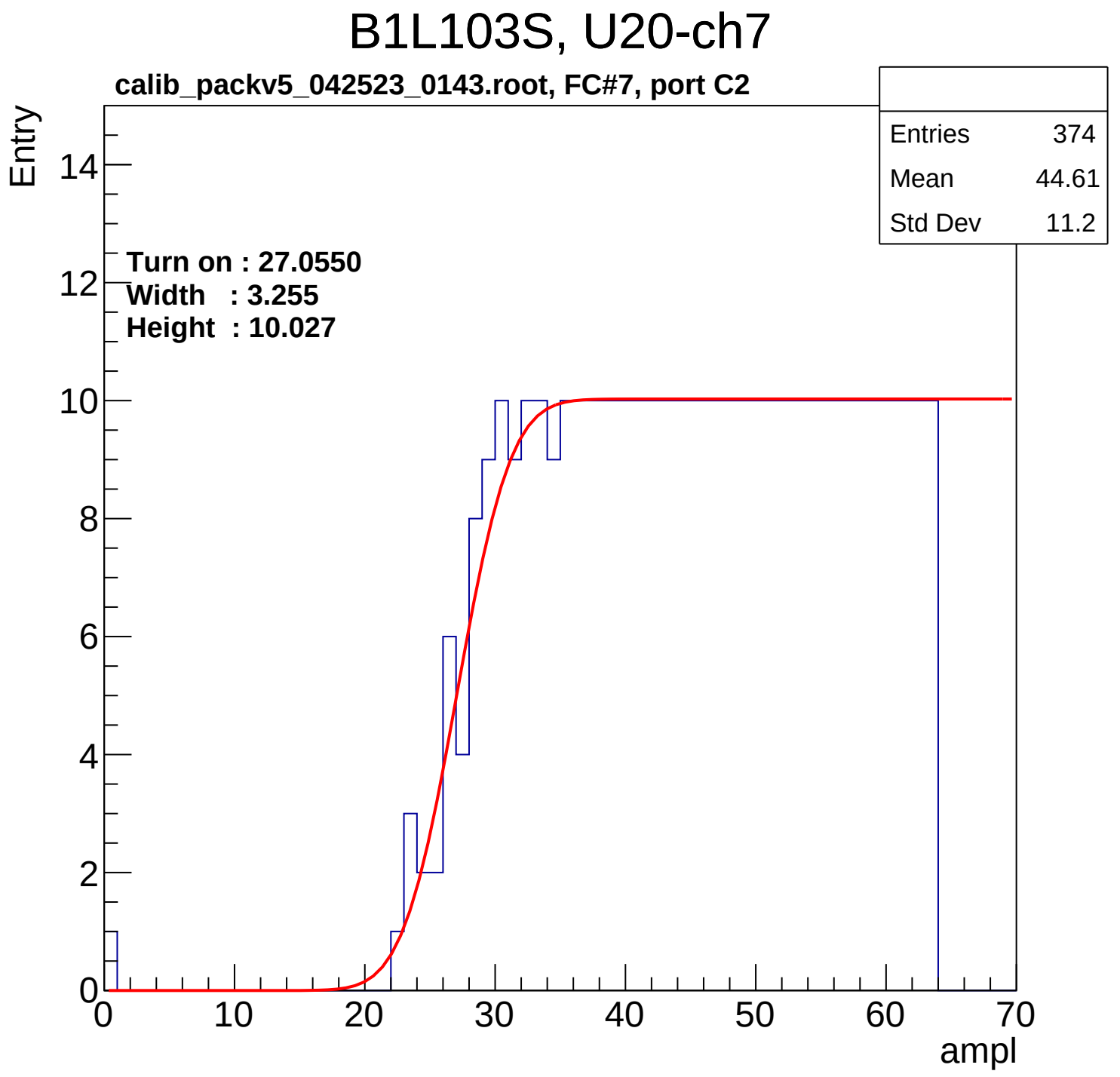
B1L103S, U20-ch7
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.61
Std Dev 11.2
Turn on : 27.0550
Width : 3.255
Height : 10.027
Entry
ampl
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2
4
6
8
10
12
14
0
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60
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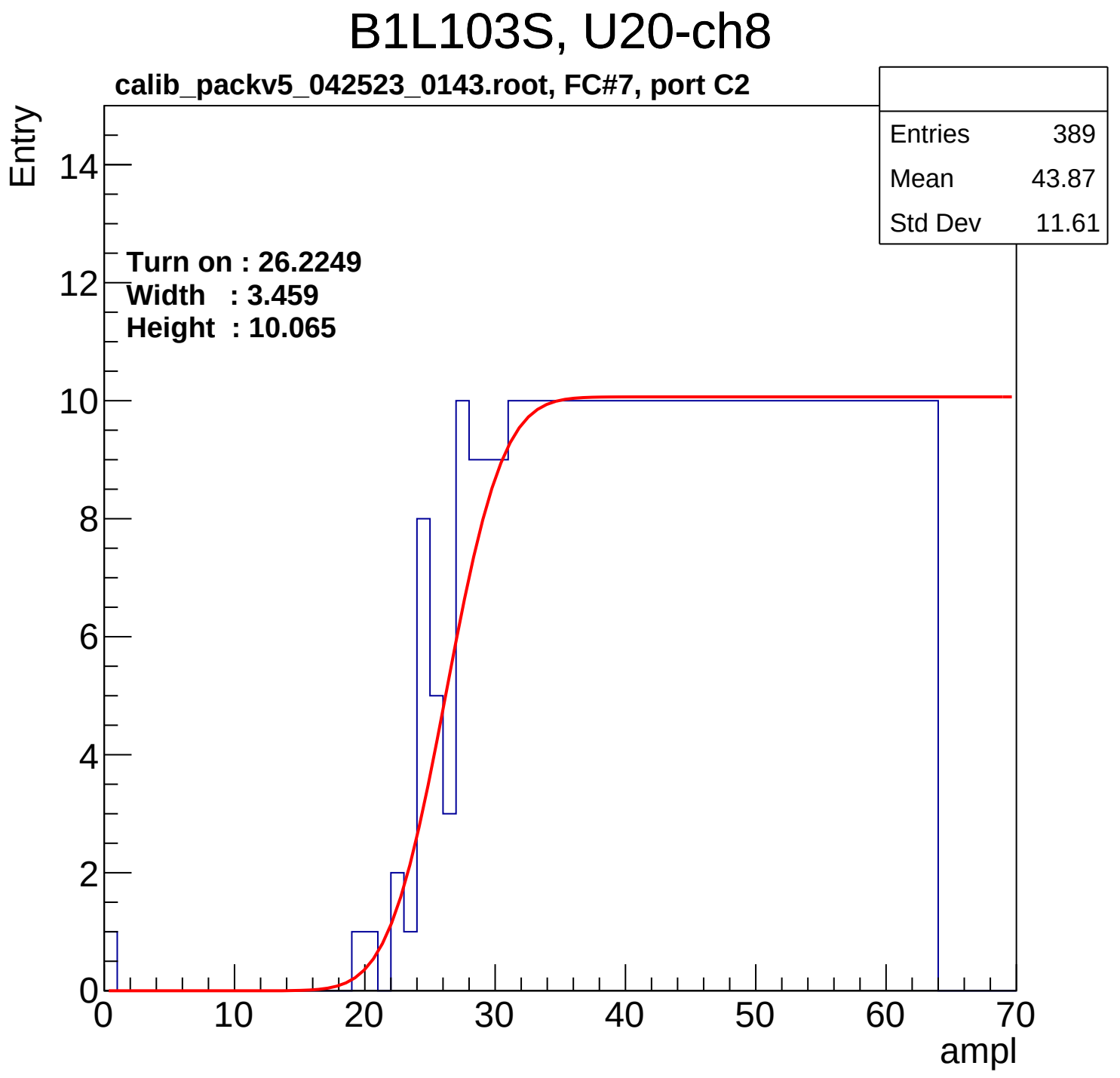
B1L103S, U20-ch8
calib_packv5_042523_0143.root, FC#7, port C2
Entries 389
Mean 43.87
Std Dev 11.61
Turn on : 26.2249
Width : 3.459
Height : 10.065
Entry
ampl
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6
8
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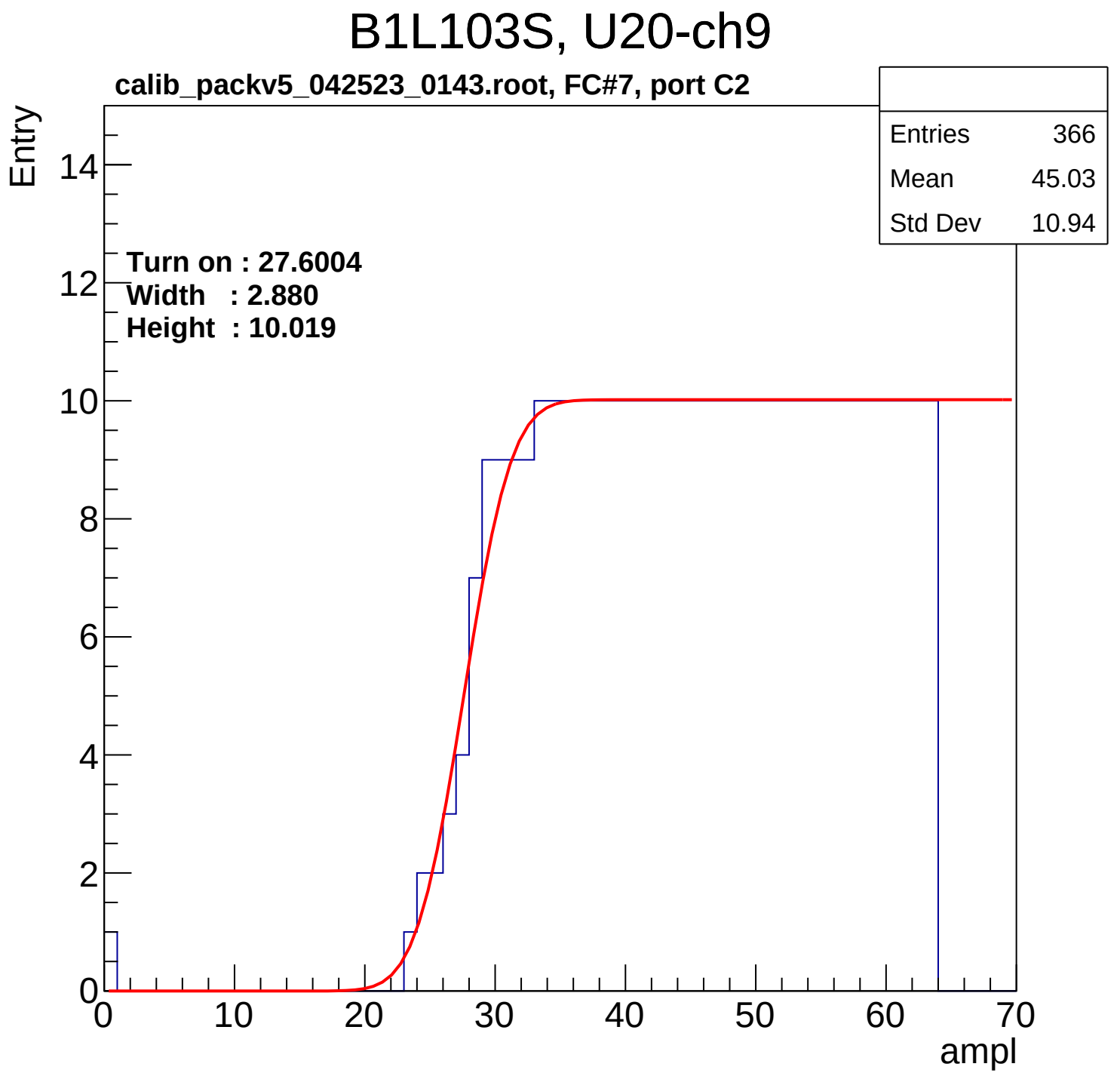
B1L103S, U20-ch9
calib_packv5_042523_0143.root, FC#7, port C2
Entries 366
Mean 45.03
Std Dev 10.94
Turn on : 27.6004
Width : 2.880
Height : 10.019
Entry
ampl
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2
4
6
8
10
12
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20
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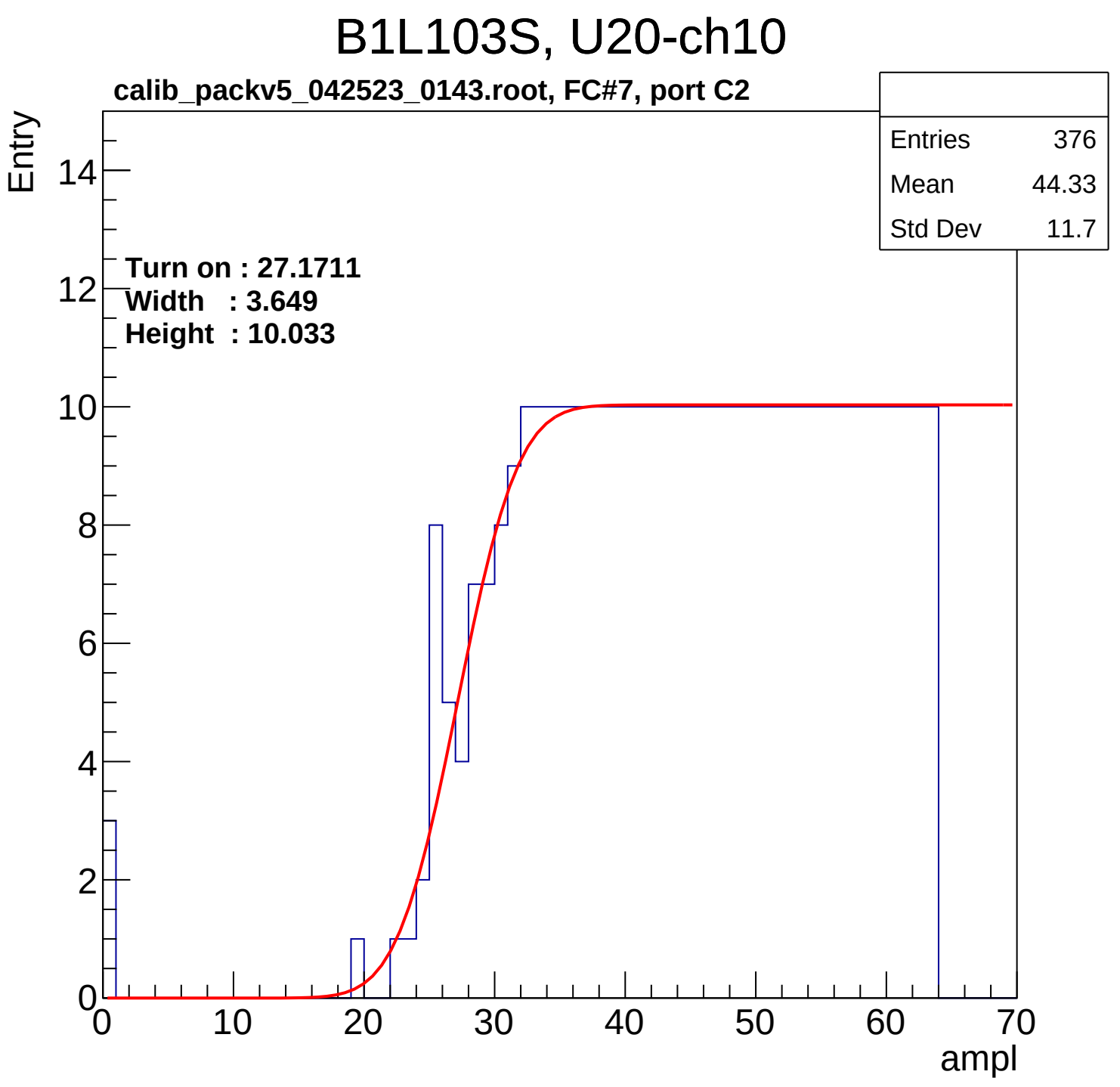
B1L103S, U20-ch10
calib_packv5_042523_0143.root, FC#7, port C2
Entries 376
Mean 44.33
Std Dev 11.7
Turn on : 27.1711
Width : 3.649
Height : 10.033
Entry
ampl
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6
8
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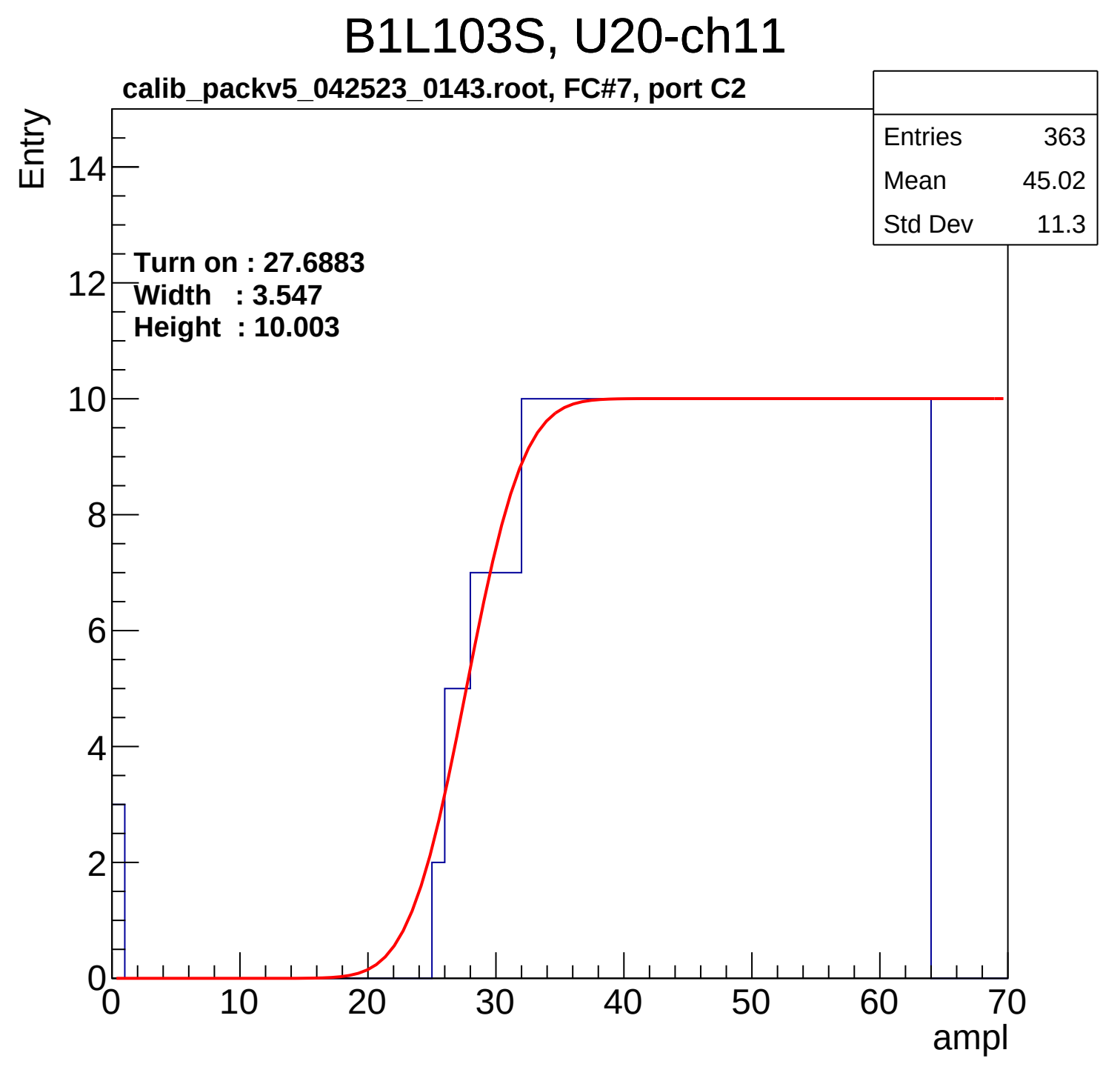
B1L103S, U20-ch11
calib_packv5_042523_0143.root, FC#7, port C2
Entries 363
Mean 45.02
Std Dev 11.3
Turn on : 27.6883
Width : 3.547
Height : 10.003
Entry
ampl
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6
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10
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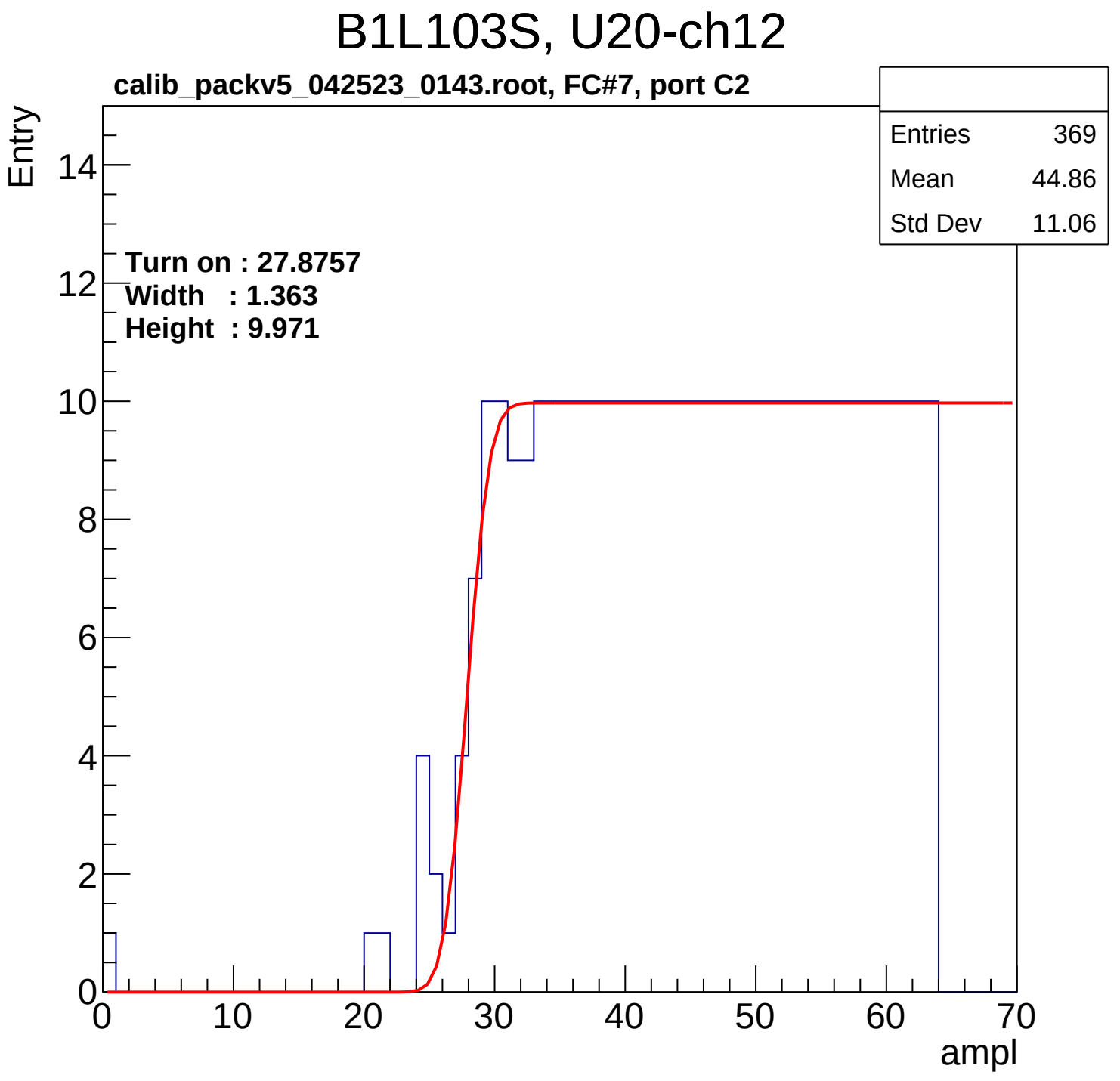
B1L103S, U20-ch12
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.86
Std Dev 11.06
Turn on : 27.8757
Width : 1.363
Height : 9.971
Entry
ampl
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6
8
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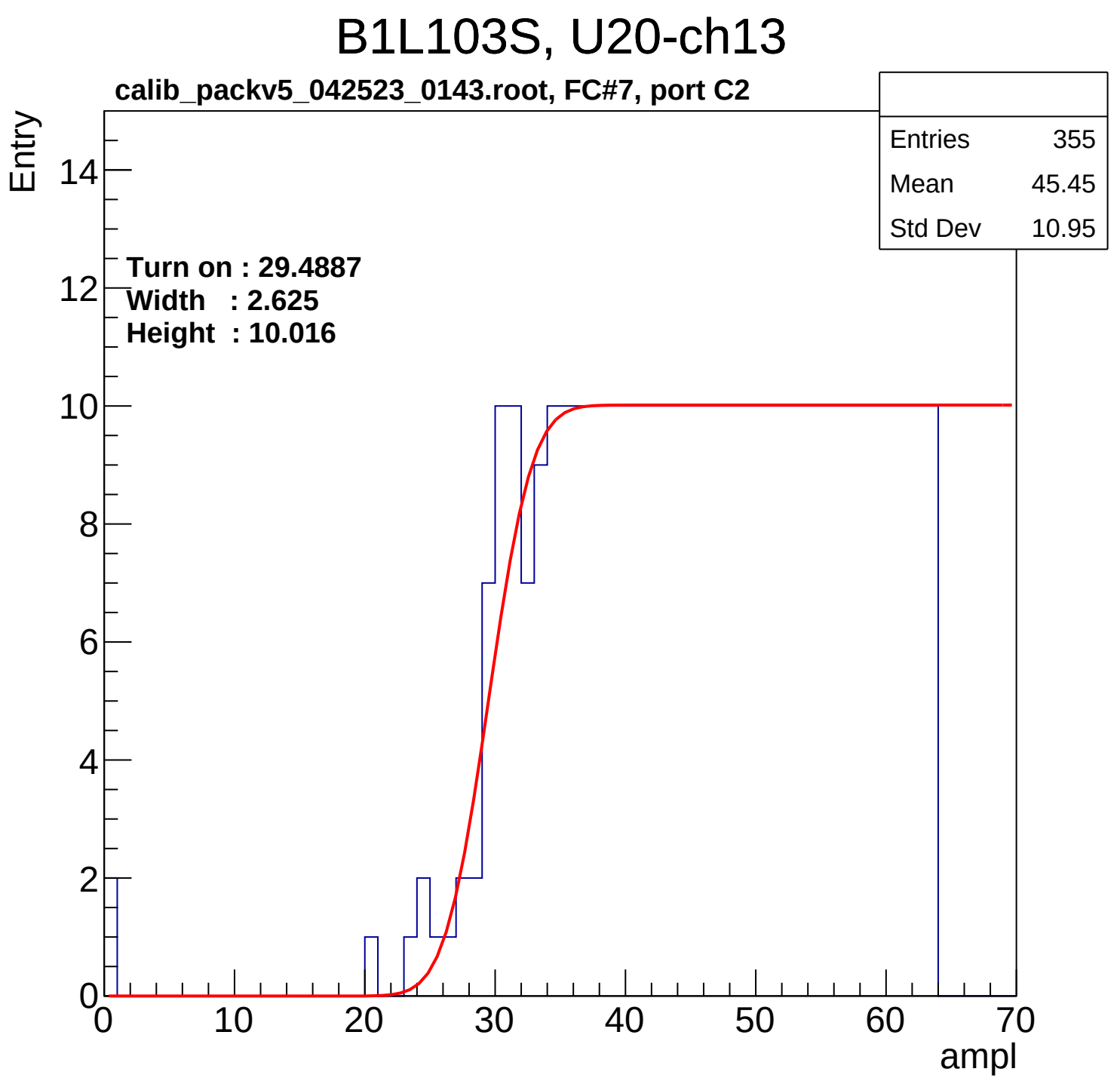
B1L103S, U20-ch13
calib_packv5_042523_0143.root, FC#7, port C2
Entries 355
Mean 45.45
Std Dev 10.95
Turn on : 29.4887
Width : 2.625
Height : 10.016
Entry
ampl
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2
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6
8
10
12
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0
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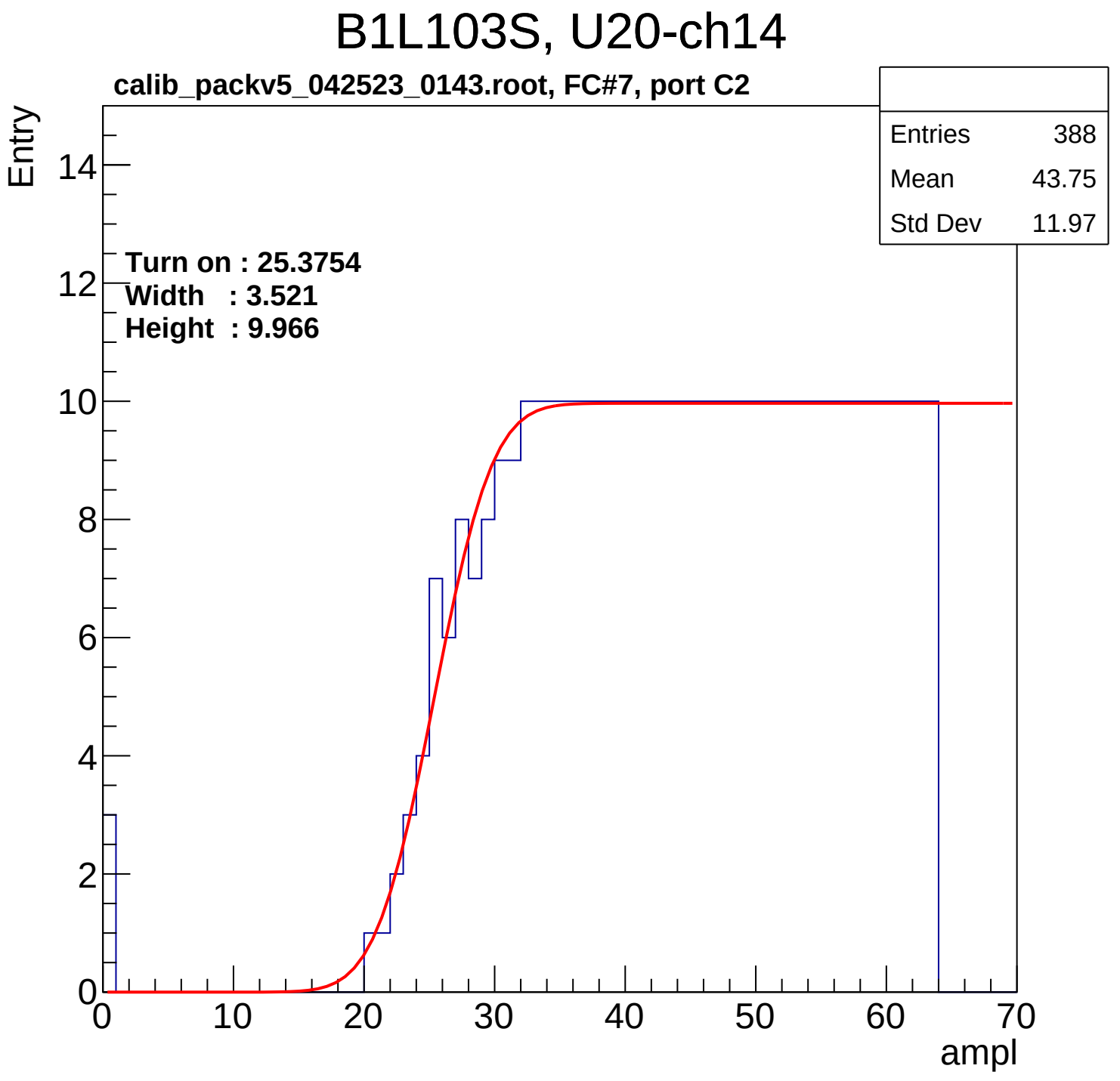
B1L103S, U20-ch14
calib_packv5_042523_0143.root, FC#7, port C2
Entries 388
Mean 43.75
Std Dev 11.97
Turn on : 25.3754
Width : 3.521
Height : 9.966
Entry
ampl
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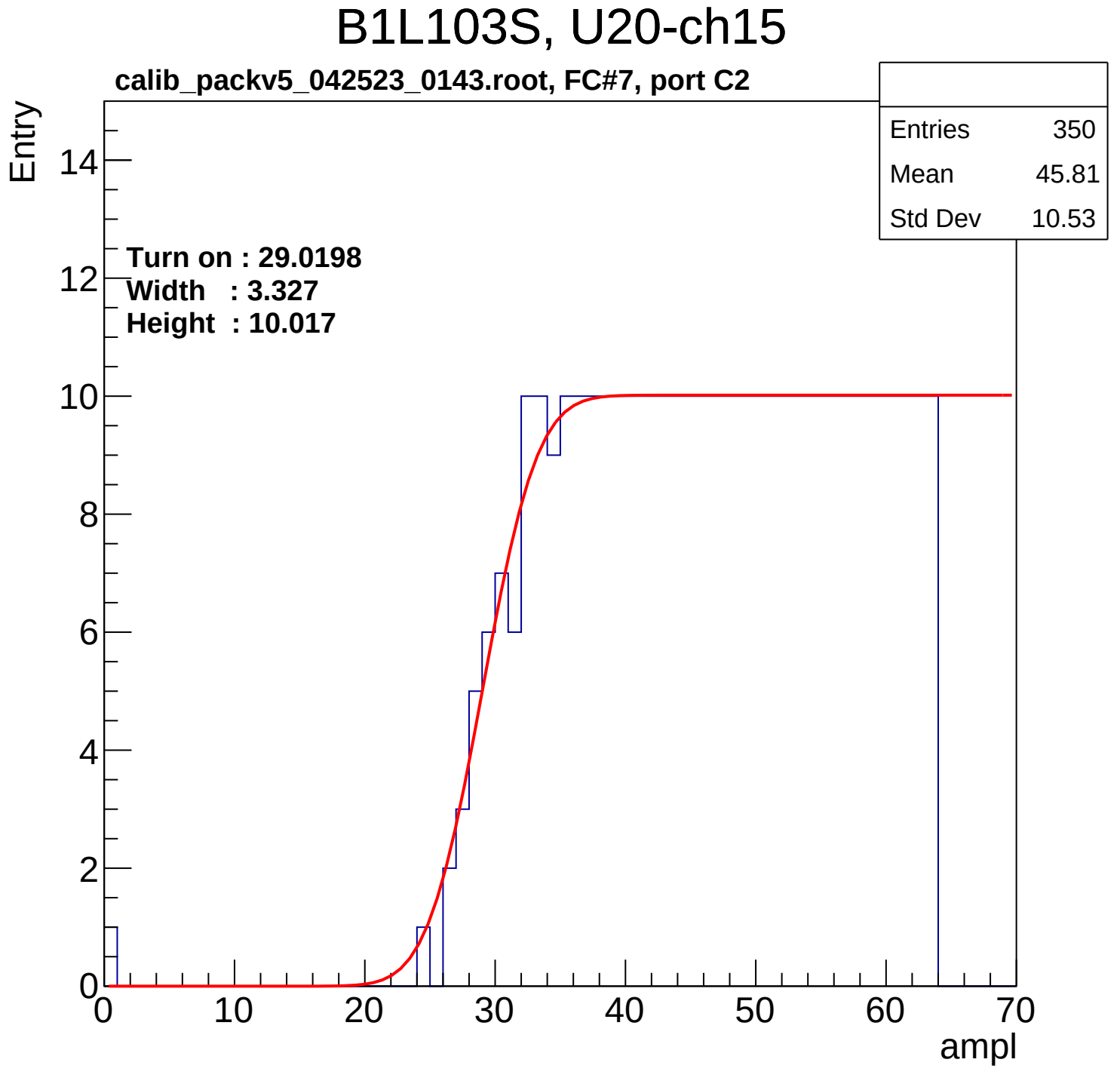
B1L103S, U20-ch15
calib_packv5_042523_0143.root, FC#7, port C2
Entries 350
Mean 45.81
Std Dev 10.53
Turn on : 29.0198
Width : 3.327
Height : 10.017
Entry
ampl
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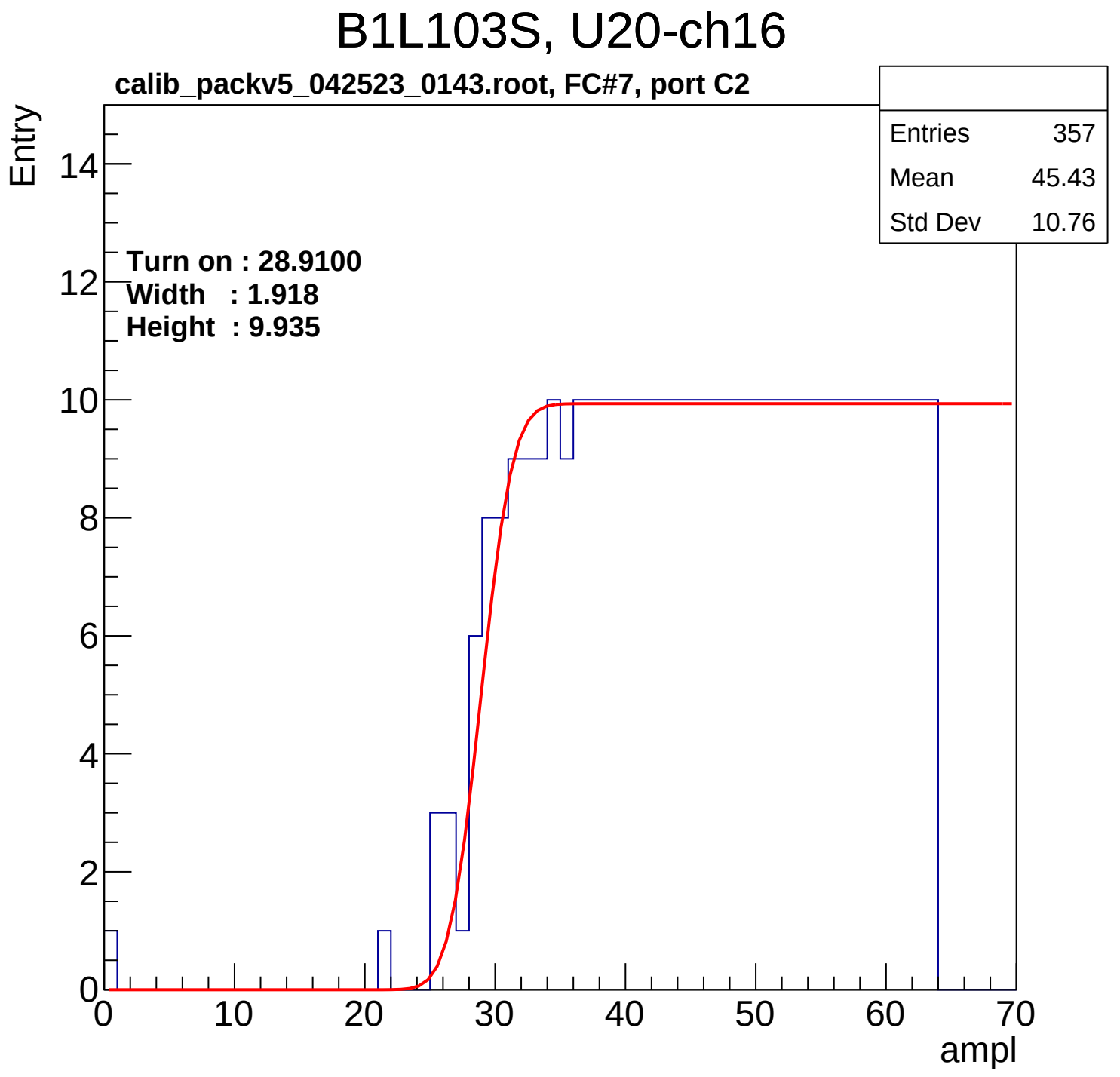
B1L103S, U20-ch16
calib_packv5_042523_0143.root, FC#7, port C2
Entries 357
Mean 45.43
Std Dev 10.76
Turn on : 28.9100
Width : 1.918
Height : 9.935
Entry
ampl
0
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8
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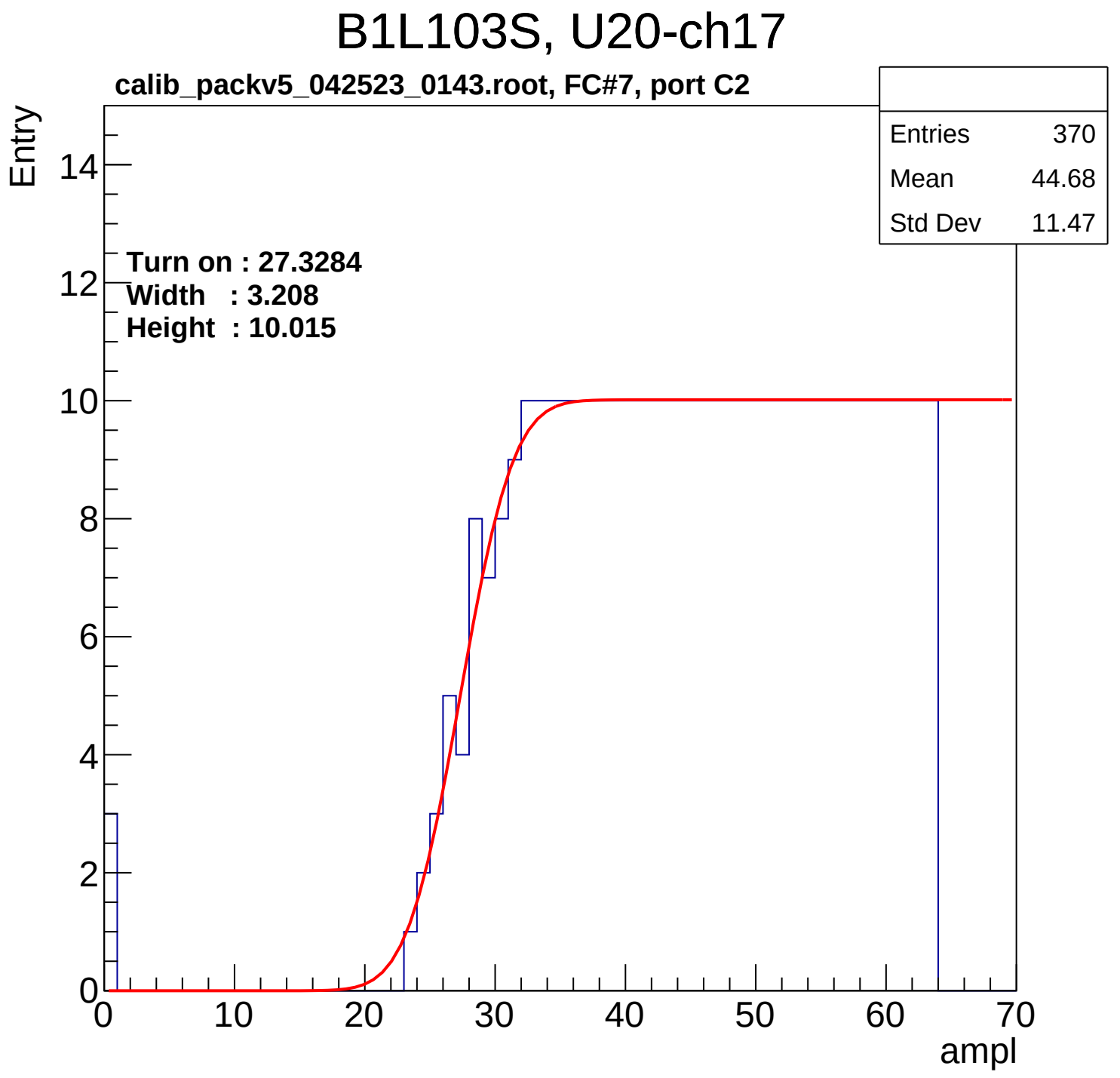
B1L103S, U20-ch17
calib_packv5_042523_0143.root, FC#7, port C2
Entries 370
Mean 44.68
Std Dev 11.47
Turn on : 27.3284
Width : 3.208
Height : 10.015
Entry
ampl
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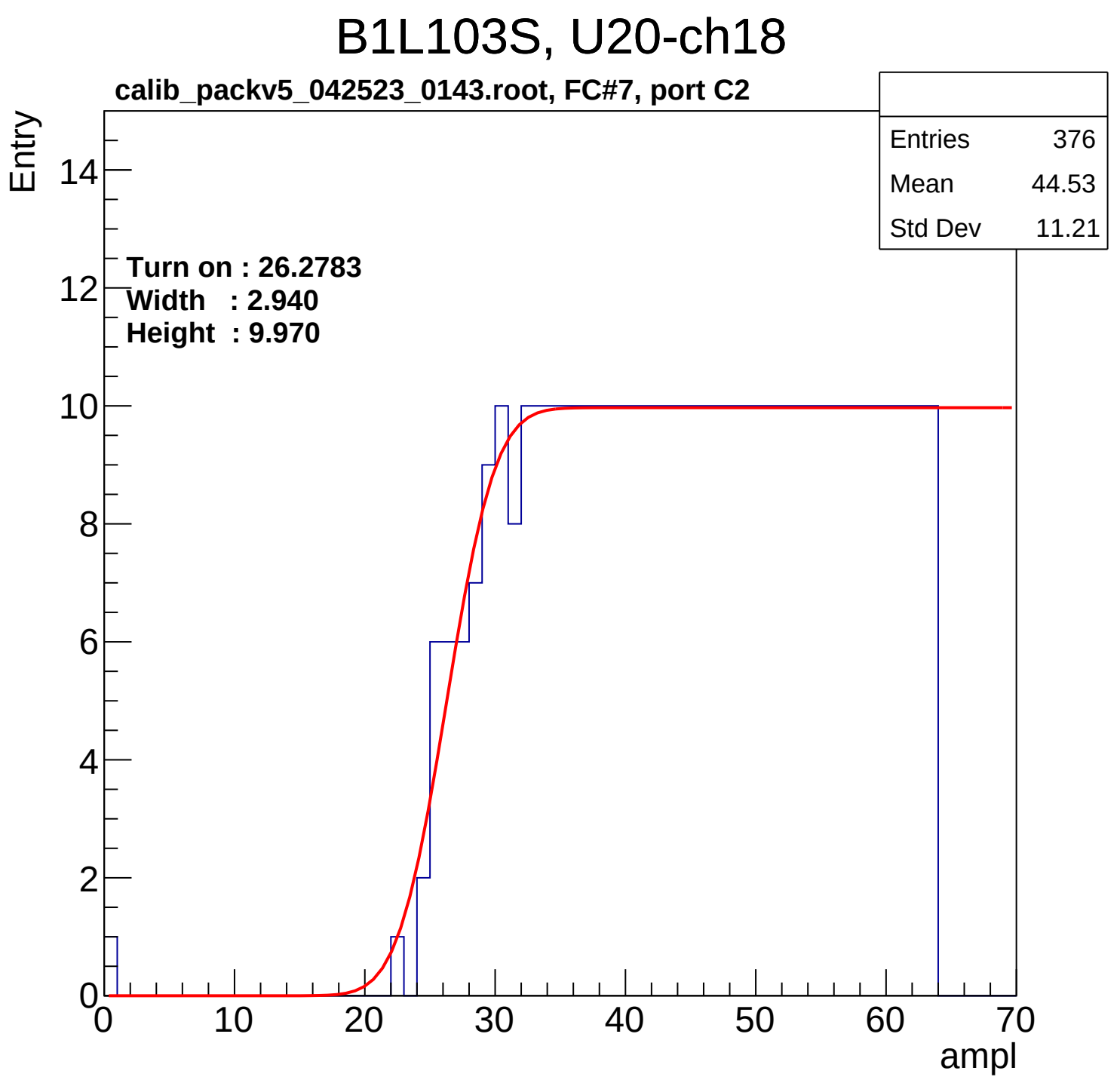
B1L103S, U20-ch18
calib_packv5_042523_0143.root, FC#7, port C2
Entries 376
Mean 44.53
Std Dev 11.21
Turn on : 26.2783
Width : 2.940
Height : 9.970
Entry
ampl
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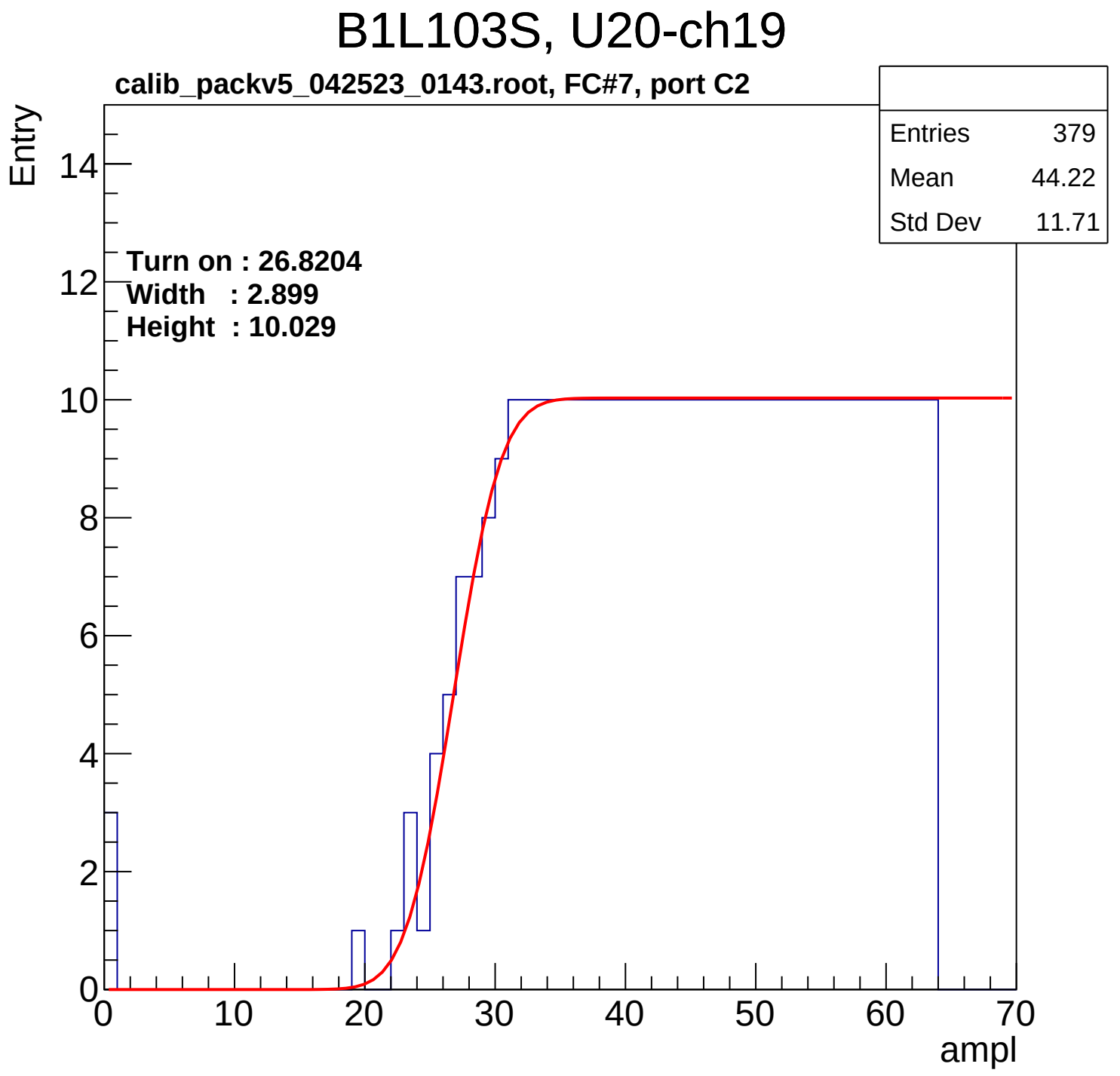
B1L103S, U20-ch19
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.22
Std Dev 11.71
Turn on : 26.8204
Width : 2.899
Height : 10.029
Entry
ampl
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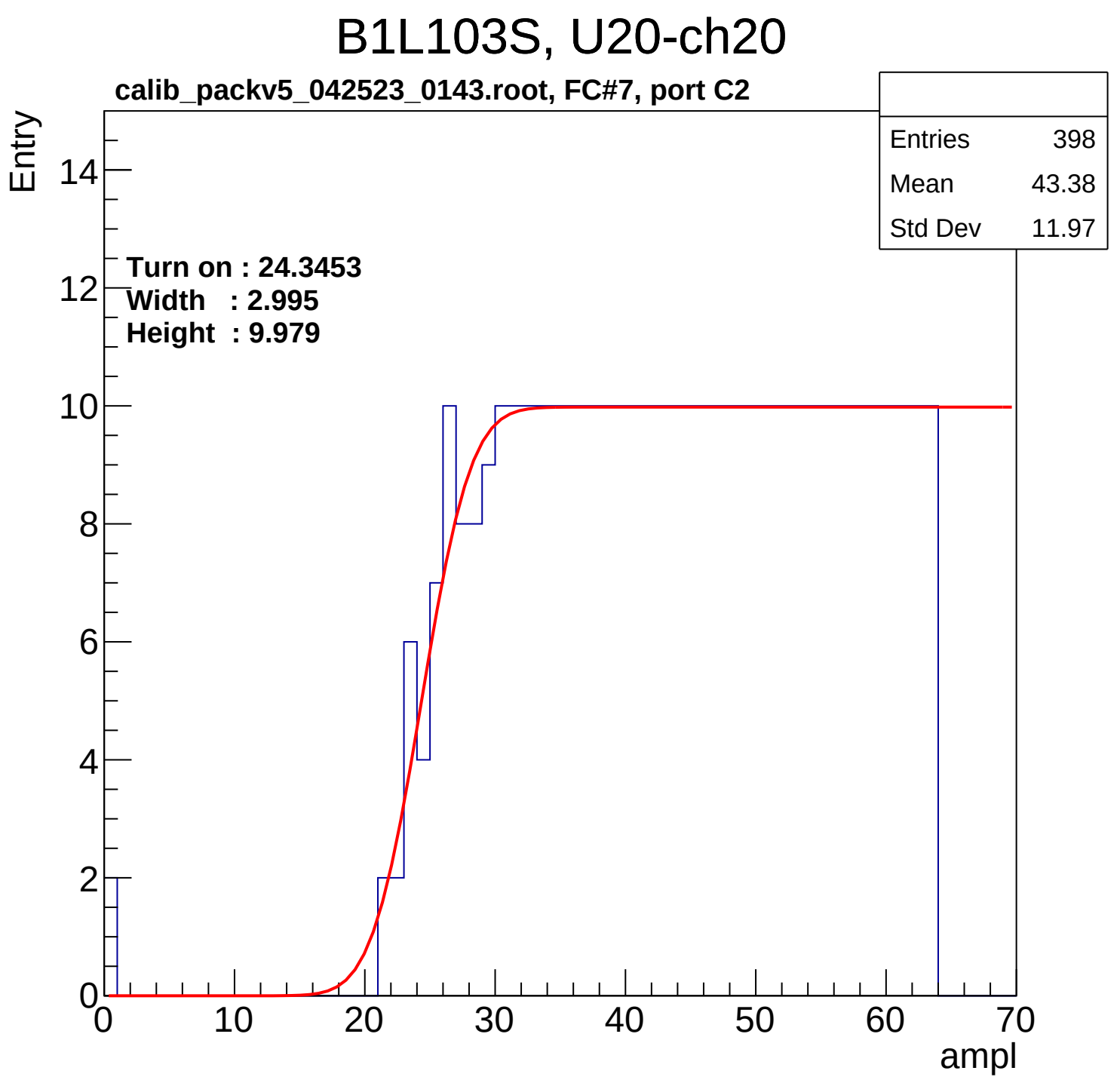
B1L103S, U20-ch20
calib_packv5_042523_0143.root, FC#7, port C2
Entries 398
Mean 43.38
Std Dev 11.97
Turn on : 24.3453
Width : 2.995
Height : 9.979
Entry
ampl
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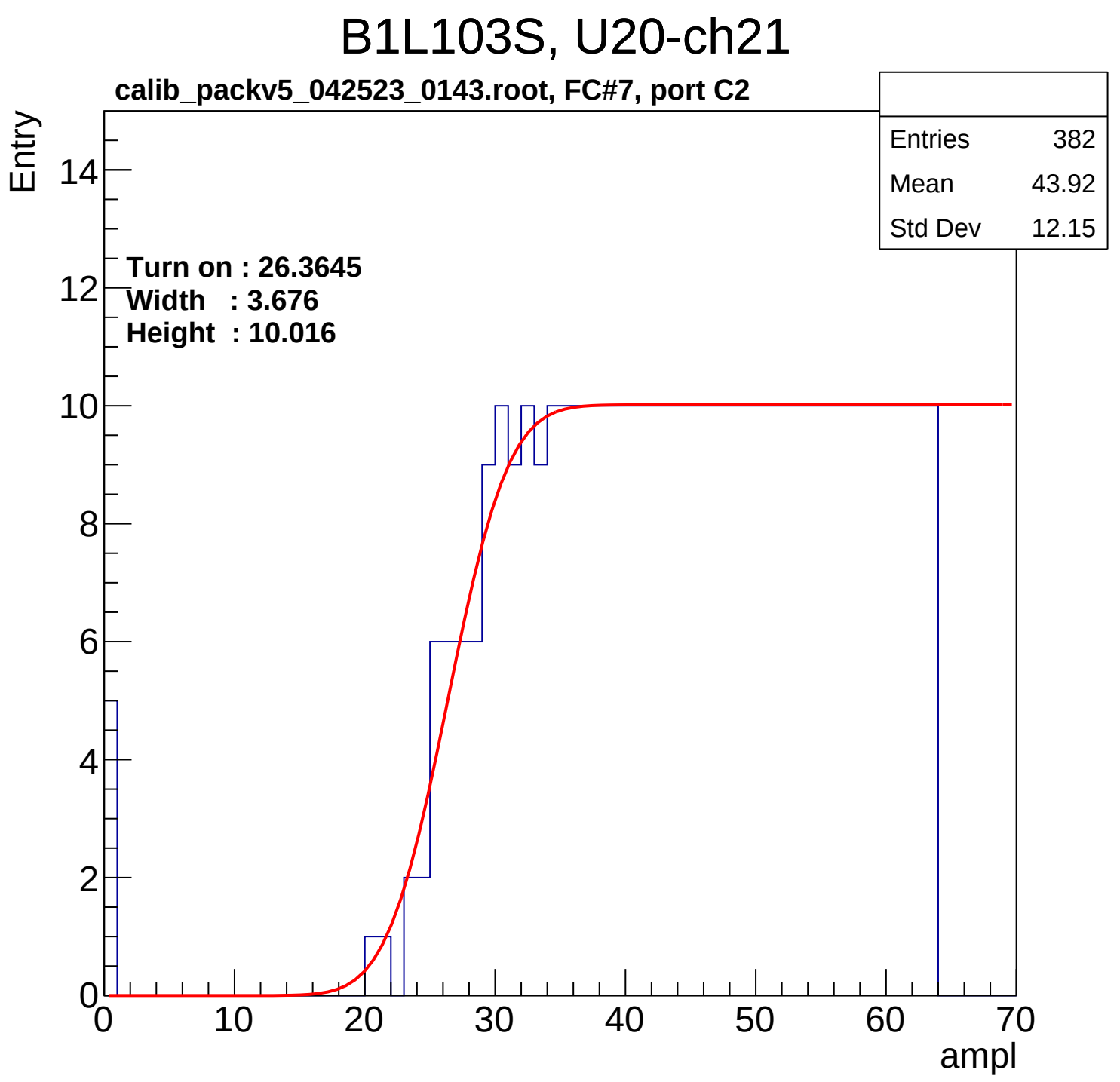
B1L103S, U20-ch21
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 43.92
Std Dev 12.15
Turn on : 26.3645
Width : 3.676
Height : 10.016
Entry
ampl
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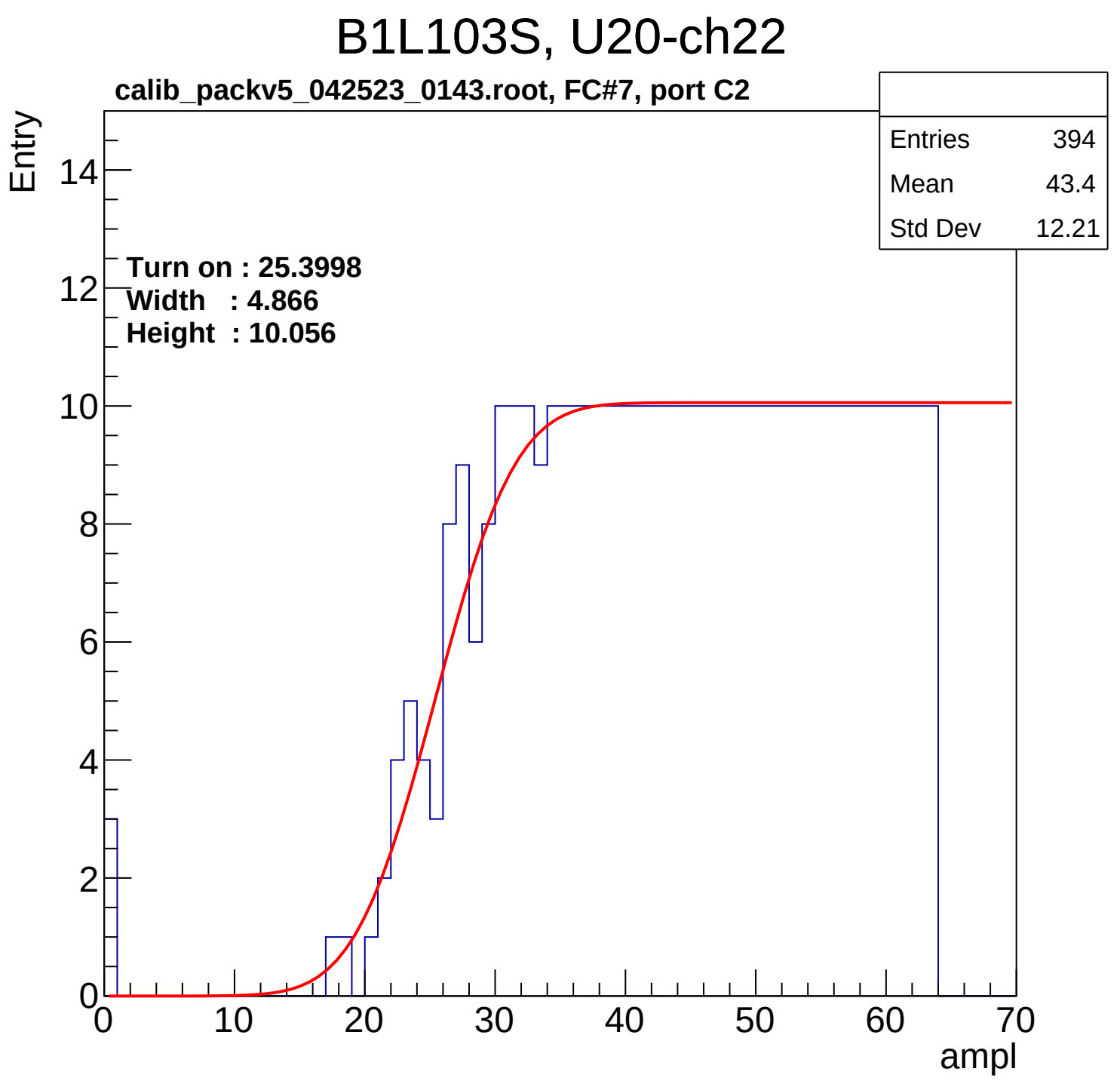
B1L103S, U20-ch22
calib_packv5_042523_0143.root, FC#7, port C2
Entries 394
Mean 43.4
Std Dev 12.21
Turn on : 25.3998
Width : 4.866
Height : 10.056
Entry
ampl
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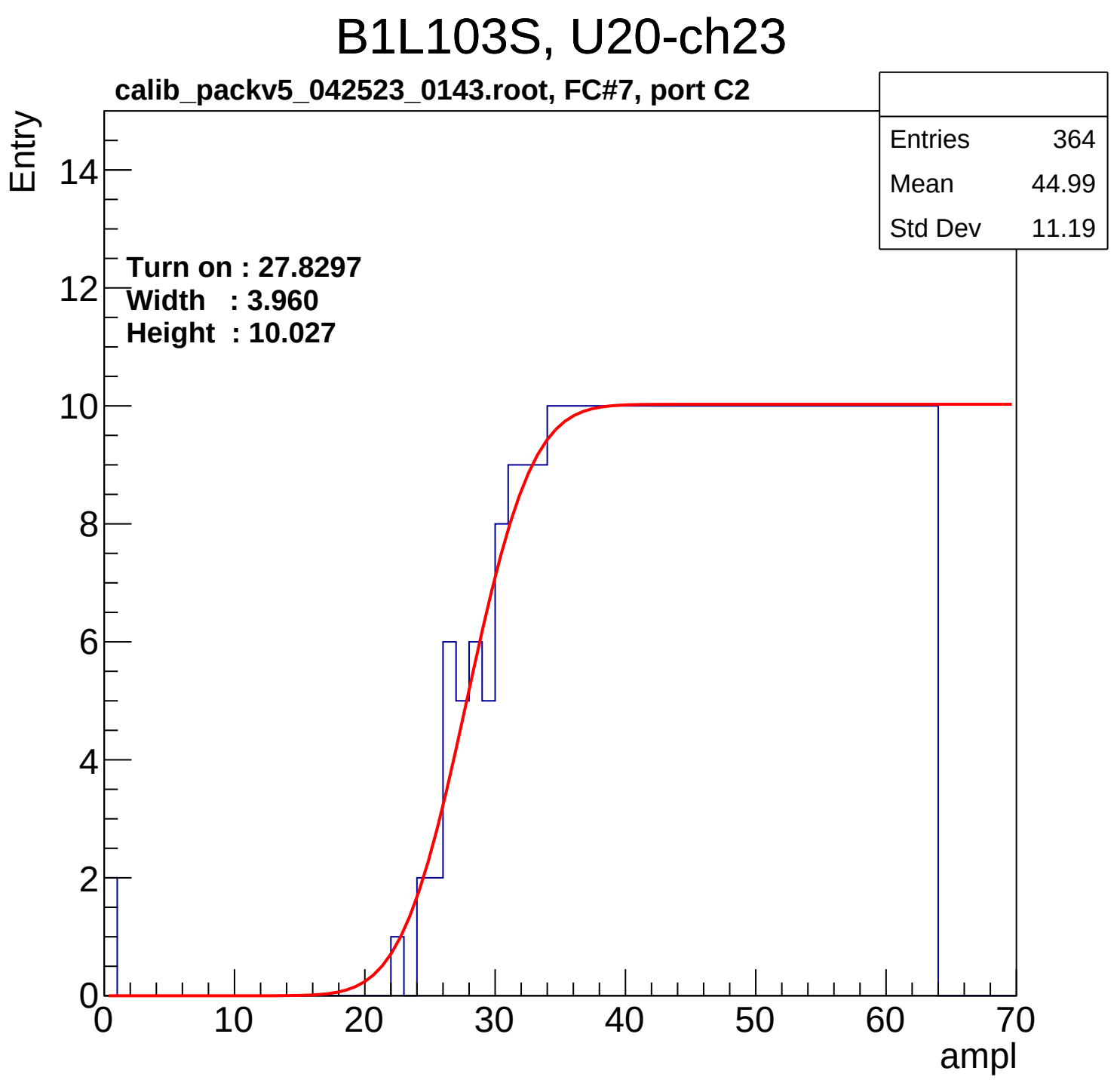
B1L103S, U20-ch23
calib_packv5_042523_0143.root, FC#7, port C2
Entries 364
Mean 44.99
Std Dev 11.19
Turn on : 27.8297
Width : 3.960
Height : 10.027
Entry
ampl
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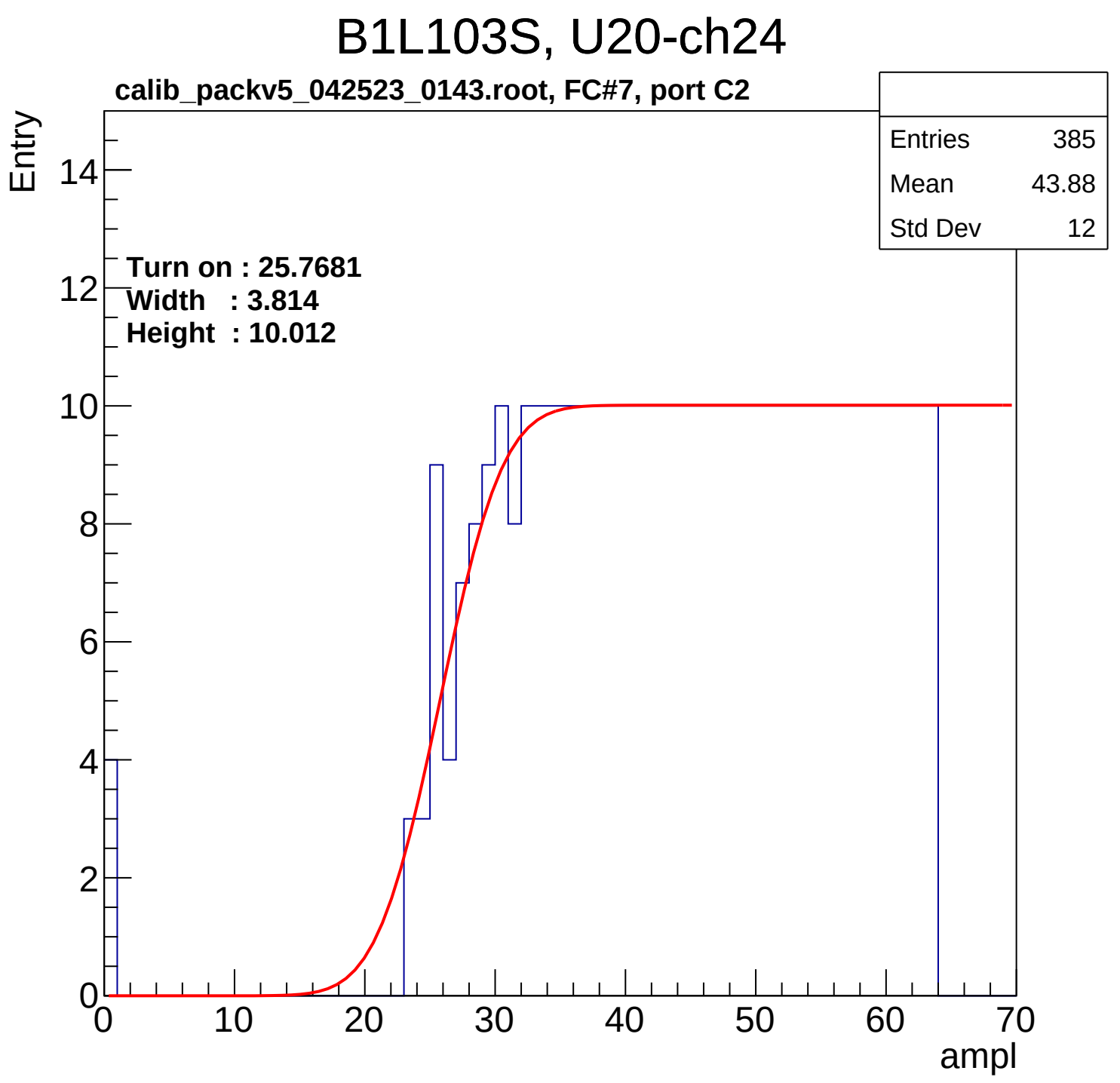
B1L103S, U20-ch24
calib_packv5_042523_0143.root, FC#7, port C2
Entries 385
Mean 43.88
Std Dev 12
Turn on : 25.7681
Width : 3.814
Height : 10.012
Entry
ampl
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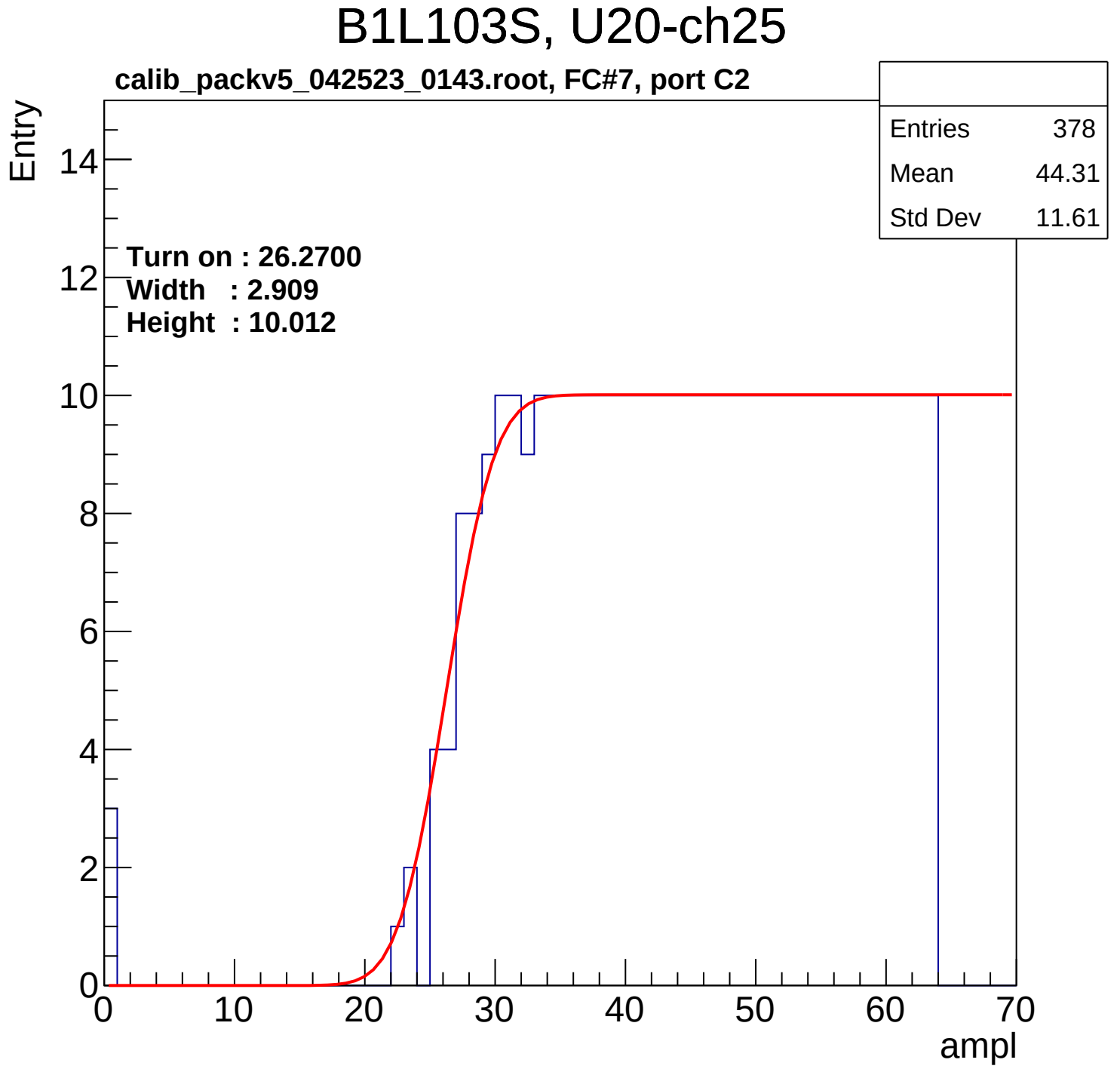
B1L103S, U20-ch25
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.31
Std Dev 11.61
Turn on : 26.2700
Width : 2.909
Height : 10.012
Entry
ampl
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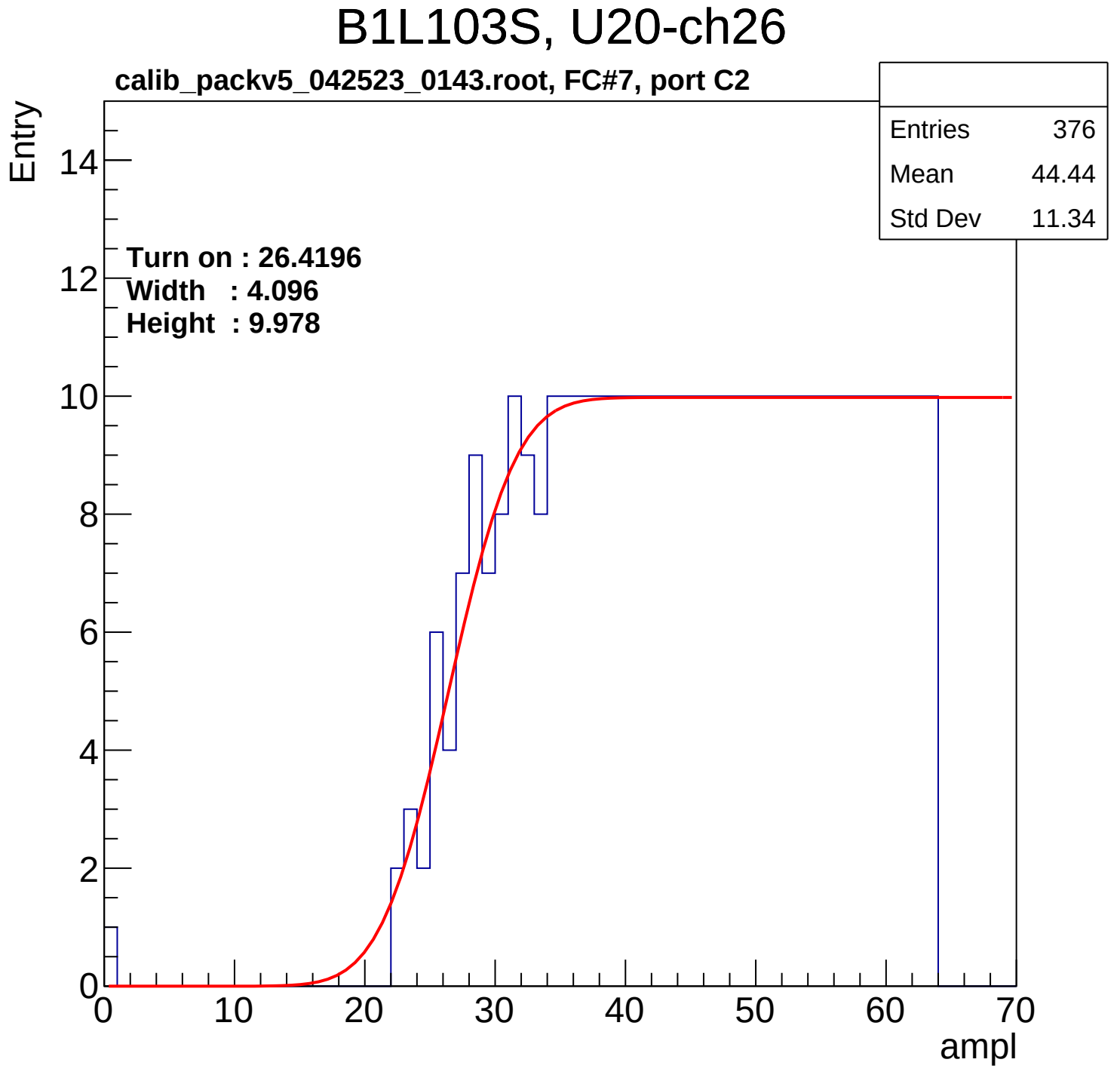
B1L103S, U20-ch26
calib_packv5_042523_0143.root, FC#7, port C2
Entries 376
Mean 44.44
Std Dev 11.34
Turn on : 26.4196
Width : 4.096
Height : 9.978
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ampl
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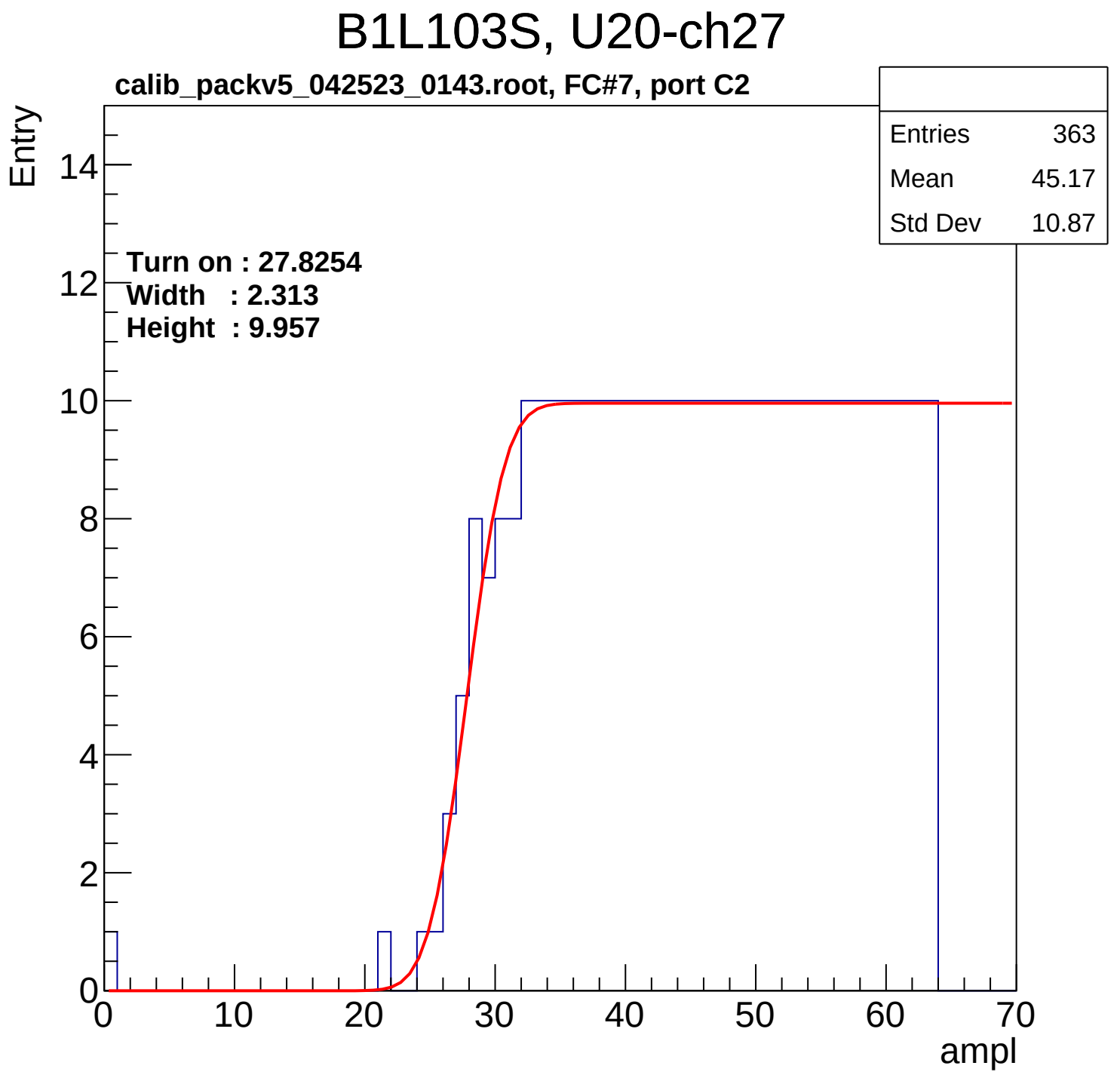
B1L103S, U20-ch27
calib_packv5_042523_0143.root, FC#7, port C2
Entries 363
Mean 45.17
Std Dev 10.87
Turn on : 27.8254
Width : 2.313
Height : 9.957
Entry
ampl
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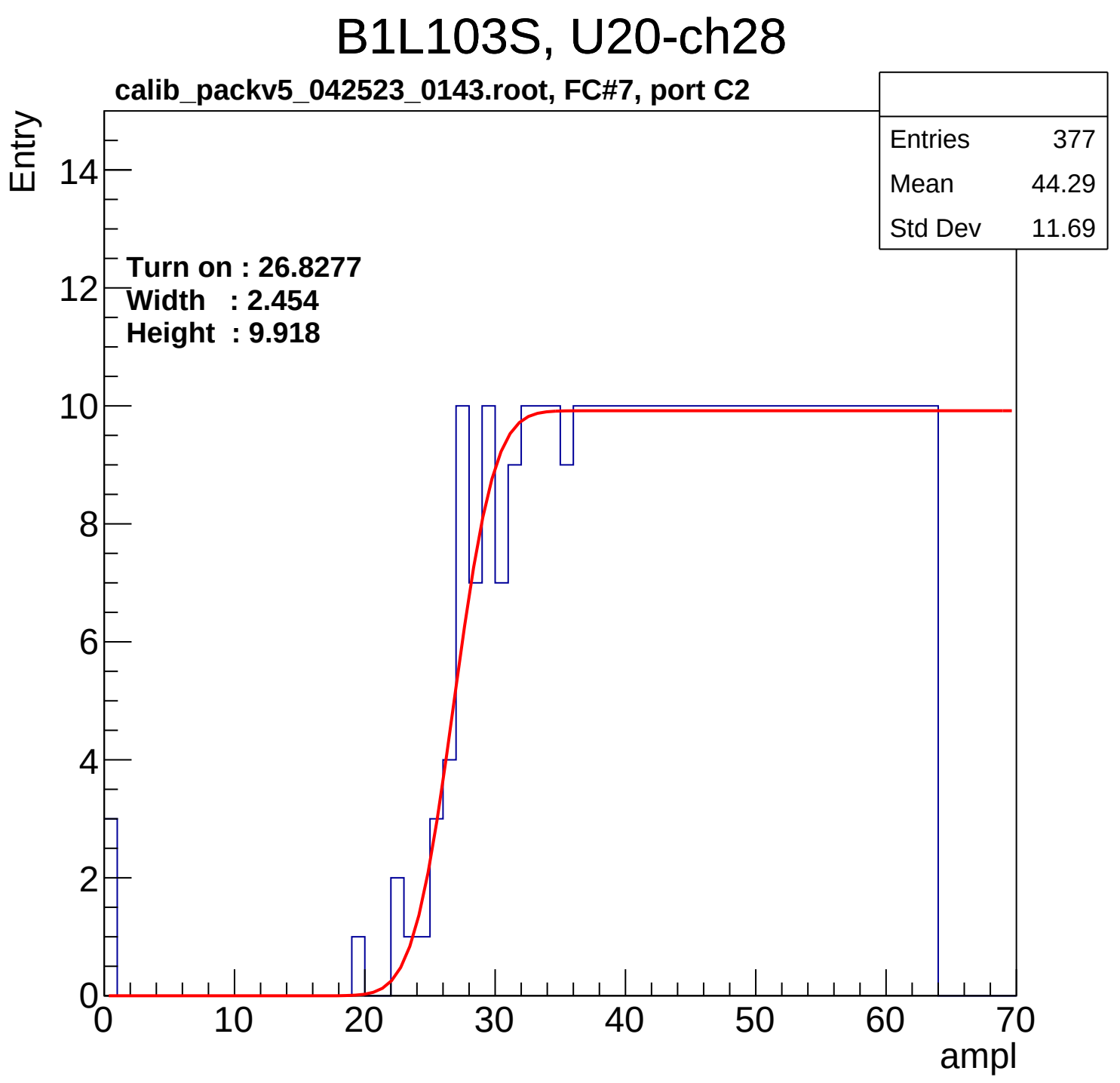
B1L103S, U20-ch28
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.29
Std Dev 11.69
Turn on : 26.8277
Width : 2.454
Height : 9.918
Entry
ampl
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4
6
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12
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20
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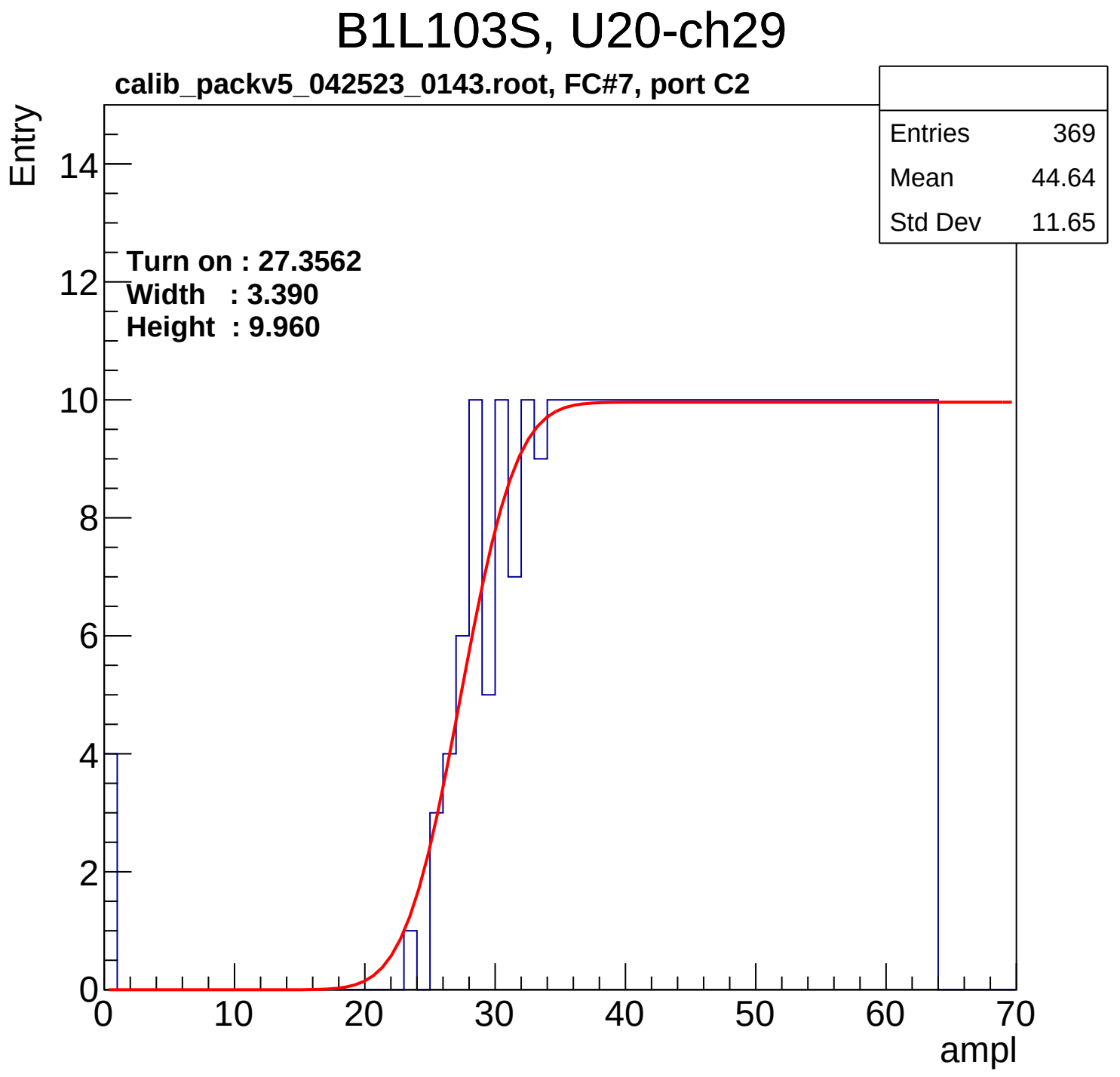
B1L103S, U20-ch29
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.64
Std Dev 11.65
Turn on : 27.3562
Width : 3.390
Height : 9.960
Entry
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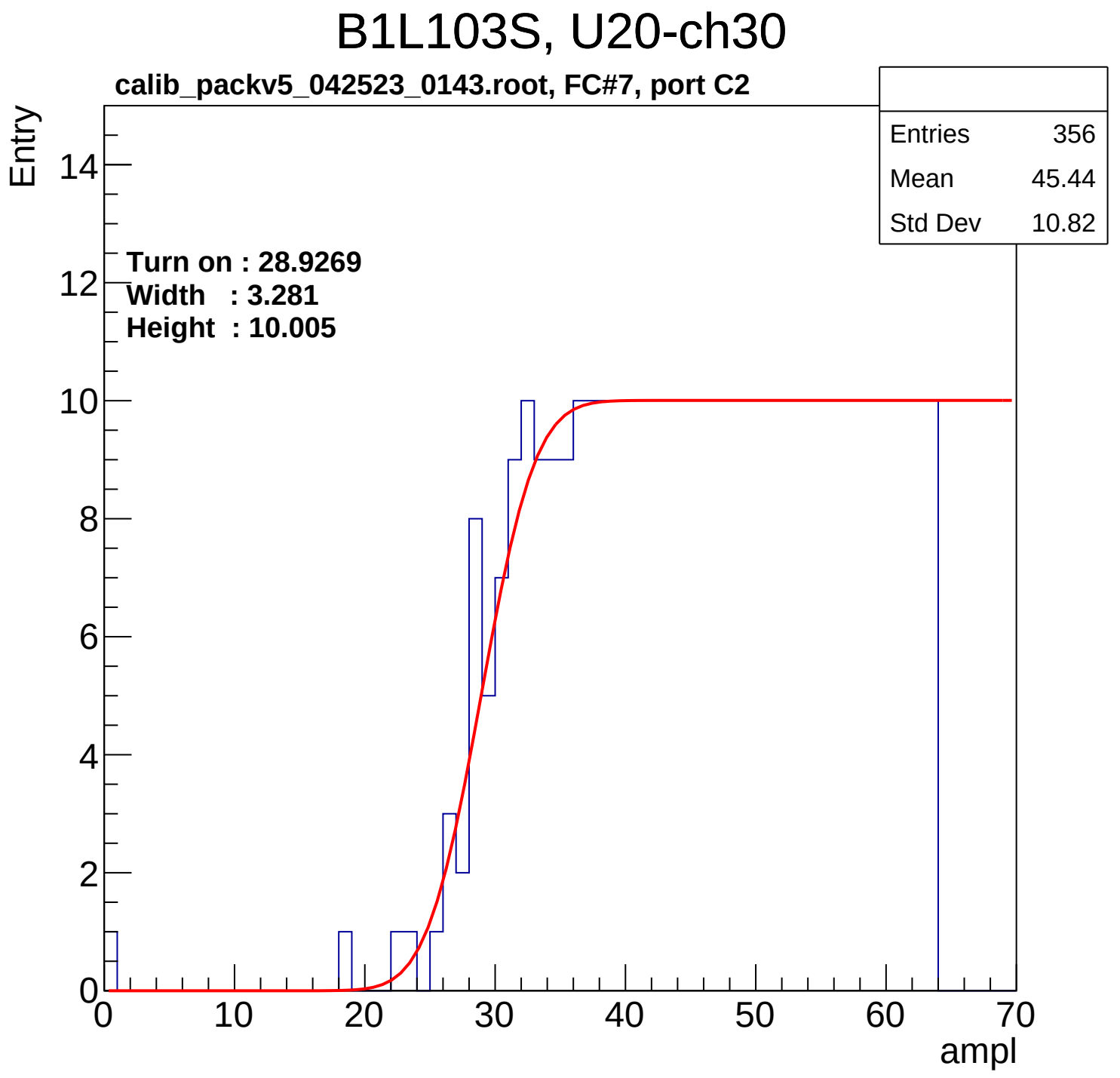
B1L103S, U20-ch30
calib_packv5_042523_0143.root, FC#7, port C2
Entries 356
Mean 45.44
Std Dev 10.82
Turn on : 28.9269
Width : 3.281
Height : 10.005
Entry
ampl
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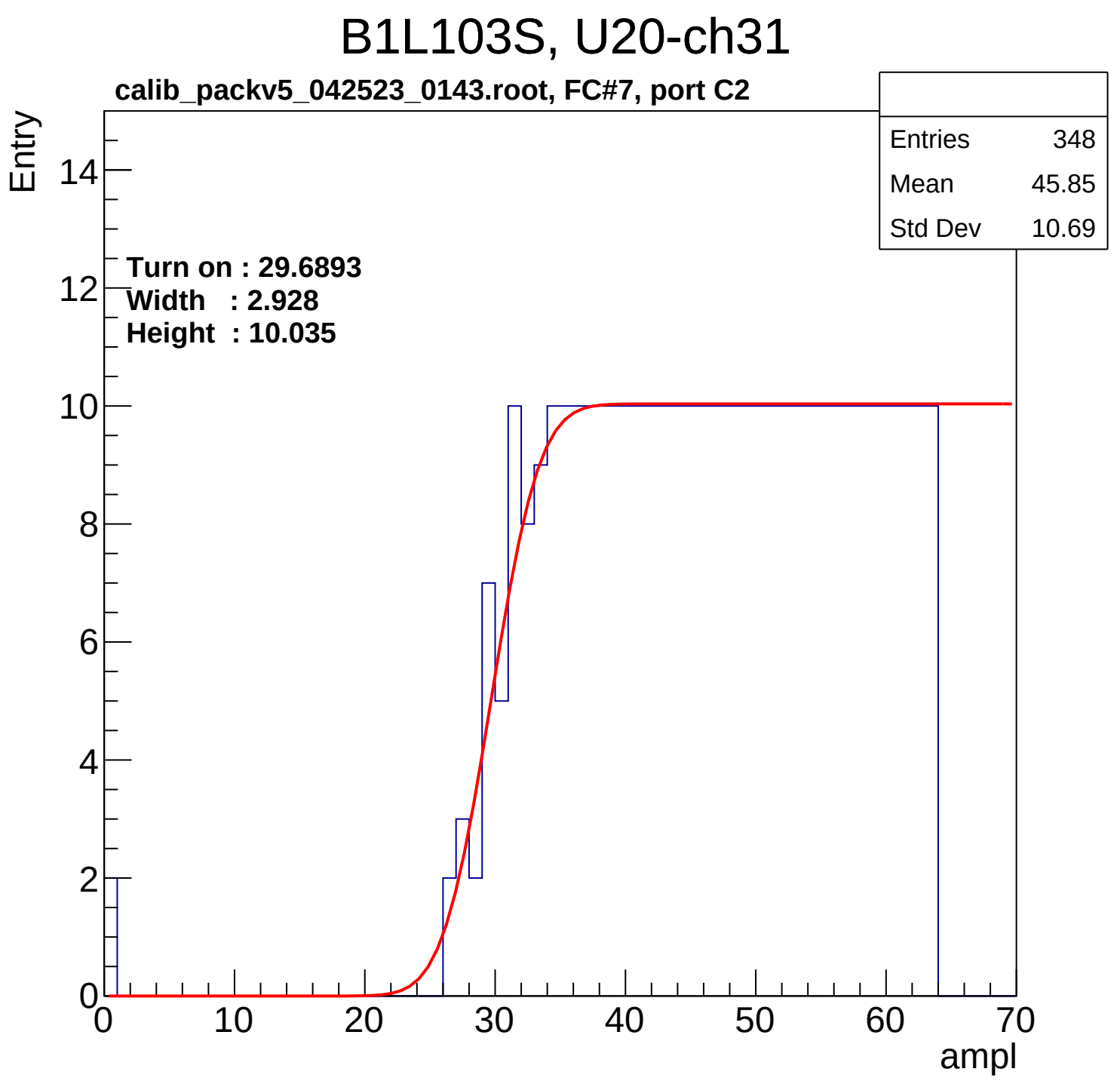
B1L103S, U20-ch31
calib_packv5_042523_0143.root, FC#7, port C2
Entries 348
Mean 45.85
Std Dev 10.69
Turn on : 29.6893
Width : 2.928
Height : 10.035
Entry
ampl
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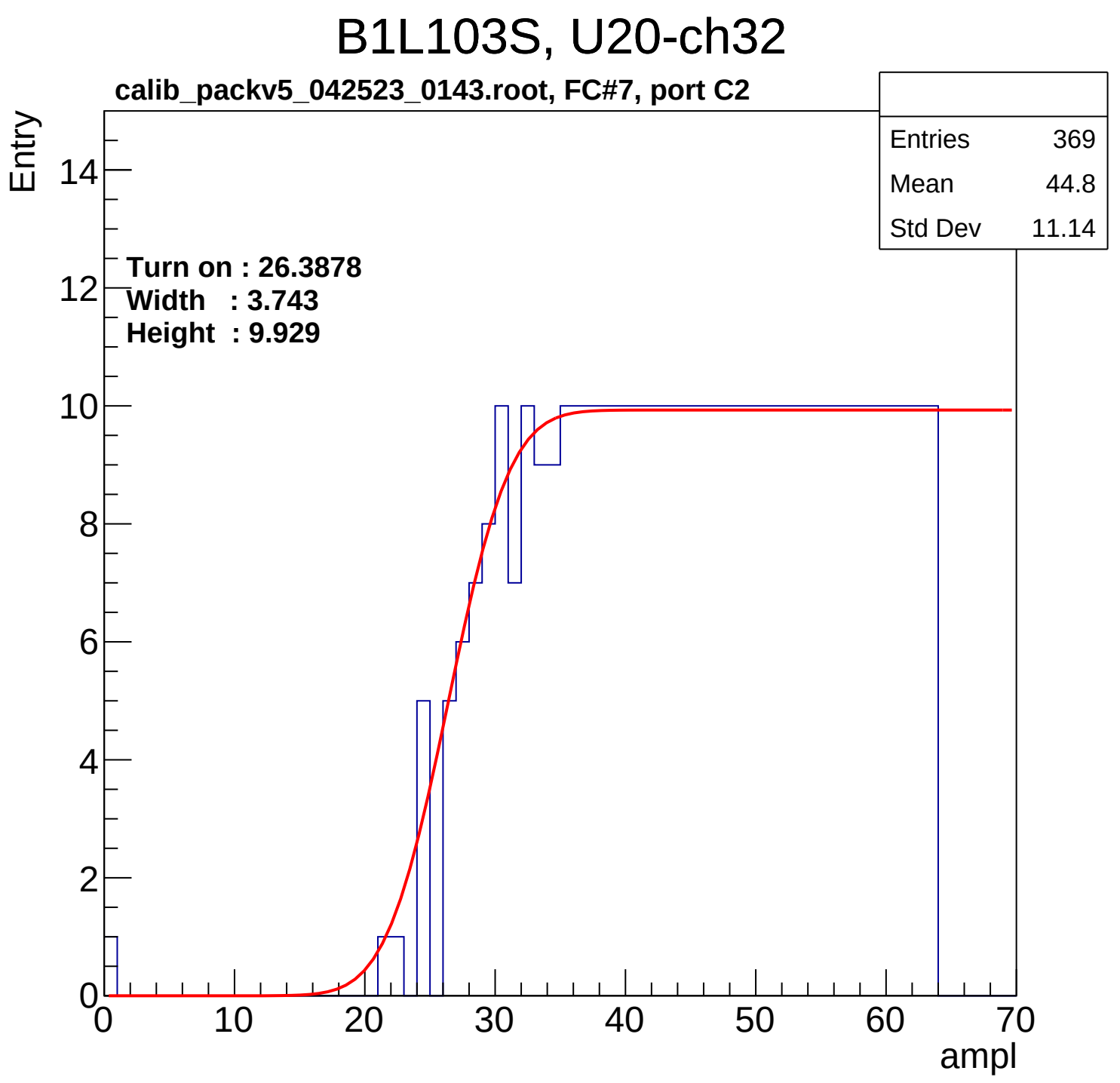
B1L103S, U20-ch32
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.8
Std Dev 11.14
Turn on : 26.3878
Width : 3.743
Height : 9.929
Entry
ampl
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4
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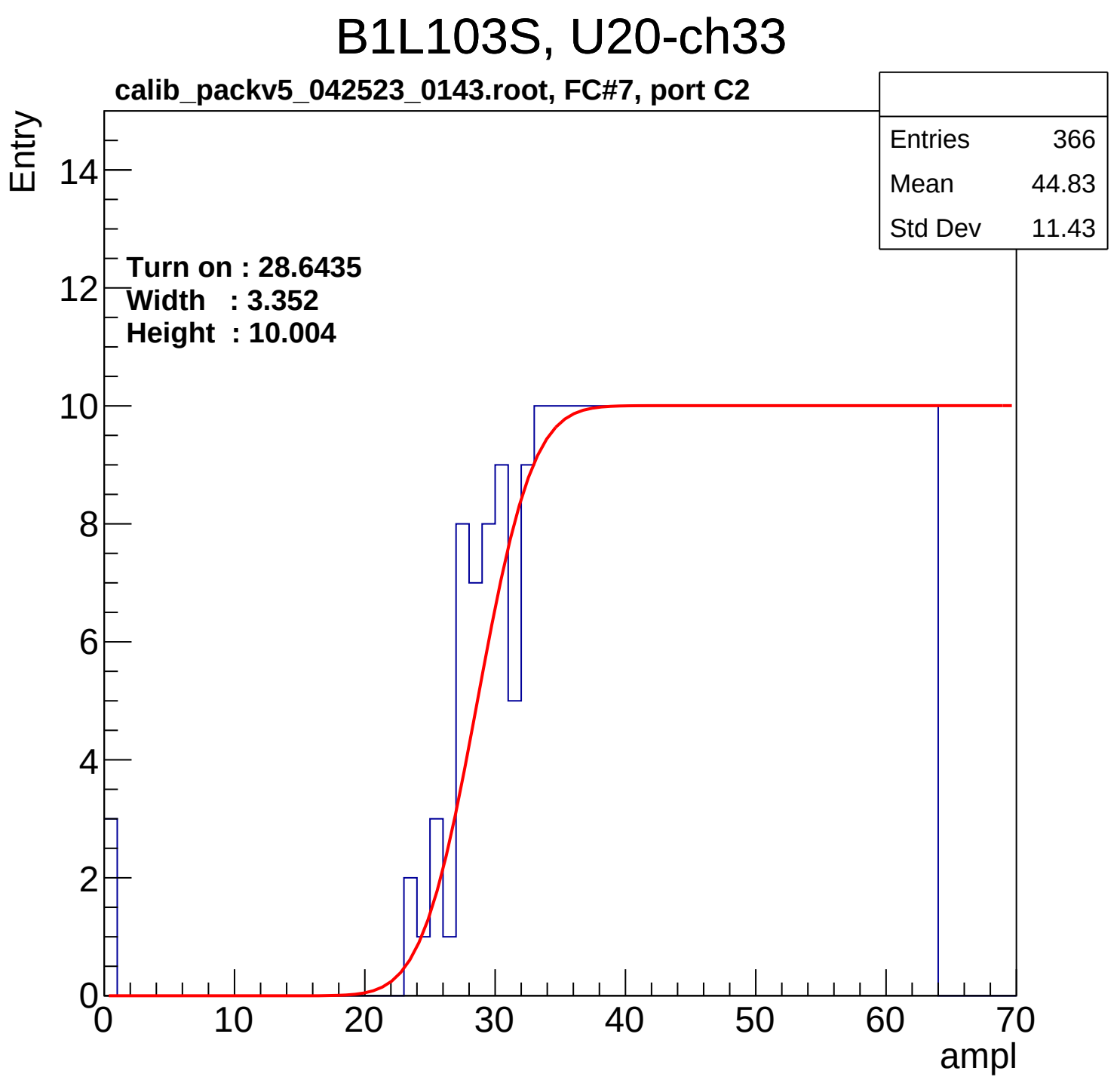
B1L103S, U20-ch33
calib_packv5_042523_0143.root, FC#7, port C2
Entries 366
Mean 44.83
Std Dev 11.43
Turn on : 28.6435
Width : 3.352
Height : 10.004
Entry
ampl
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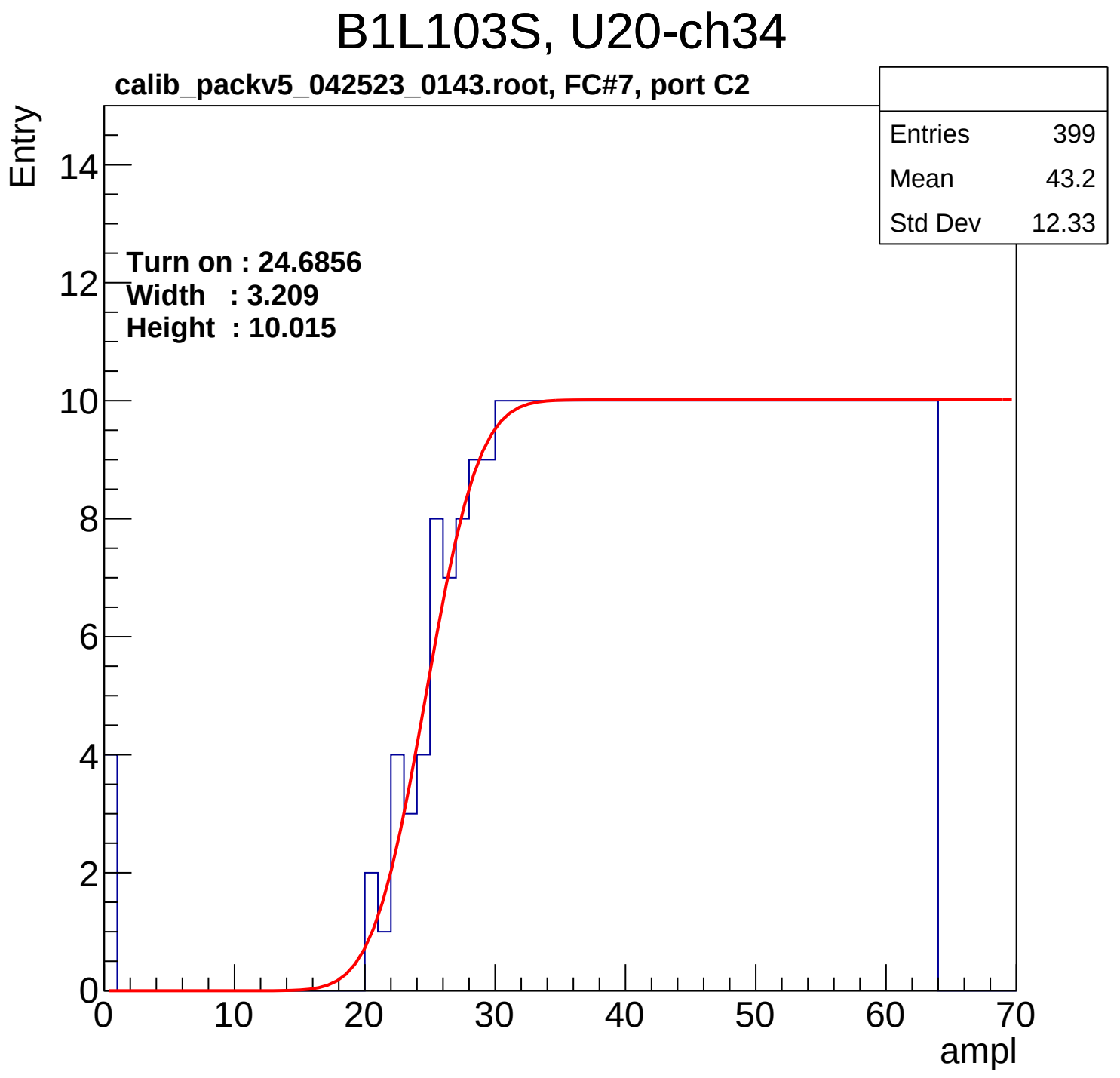
B1L103S, U20-ch34
calib_packv5_042523_0143.root, FC#7, port C2
Entries 399
Mean 43.2
Std Dev 12.33
Turn on : 24.6856
Width : 3.209
Height : 10.015
Entry
ampl
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2
4
6
8
10
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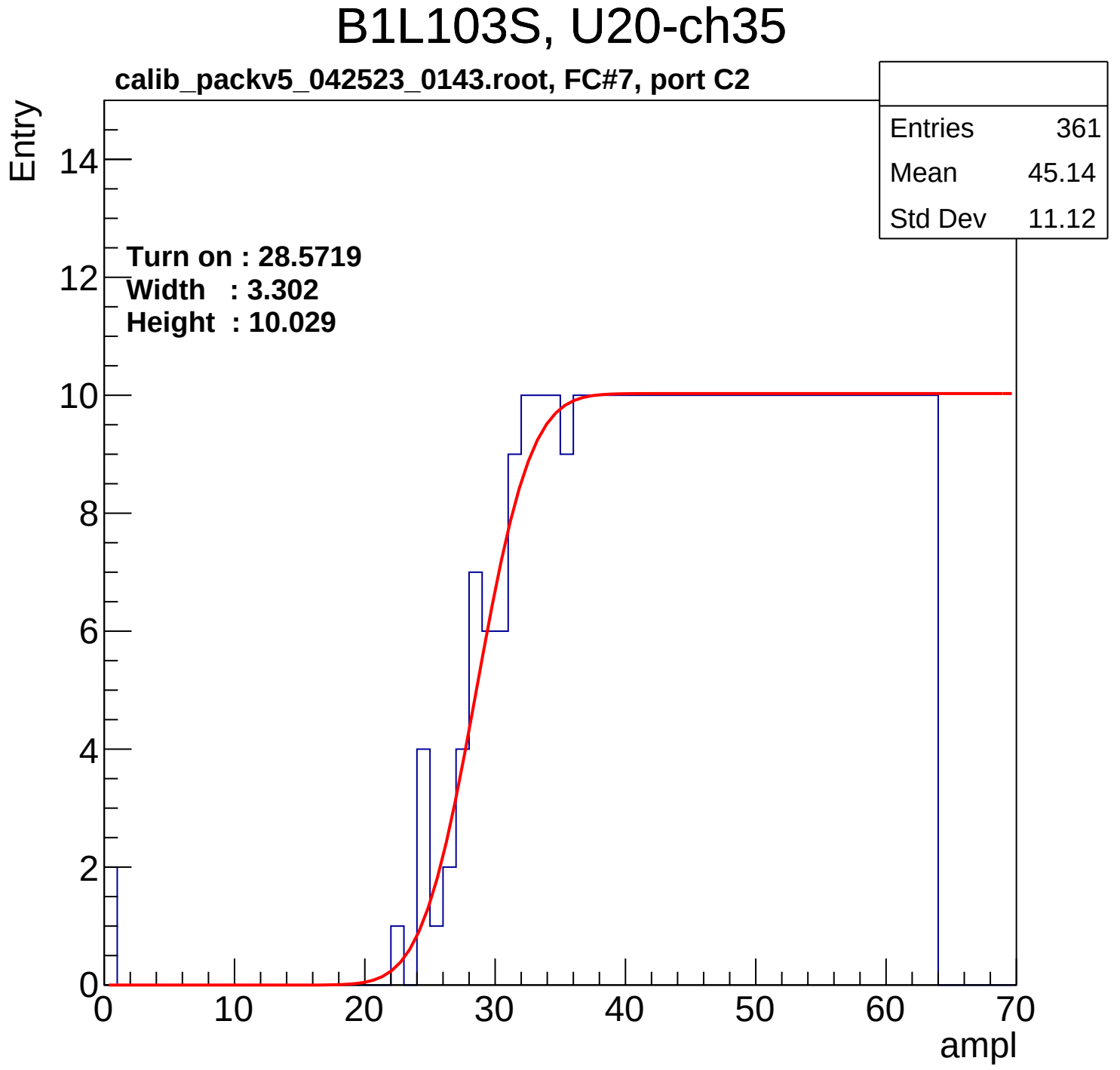
B1L103S, U20-ch35
calib_packv5_042523_0143.root, FC#7, port C2
Entries 361
Mean 45.14
Std Dev 11.12
Turn on : 28.5719
Width : 3.302
Height : 10.029
Entry
ampl
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8
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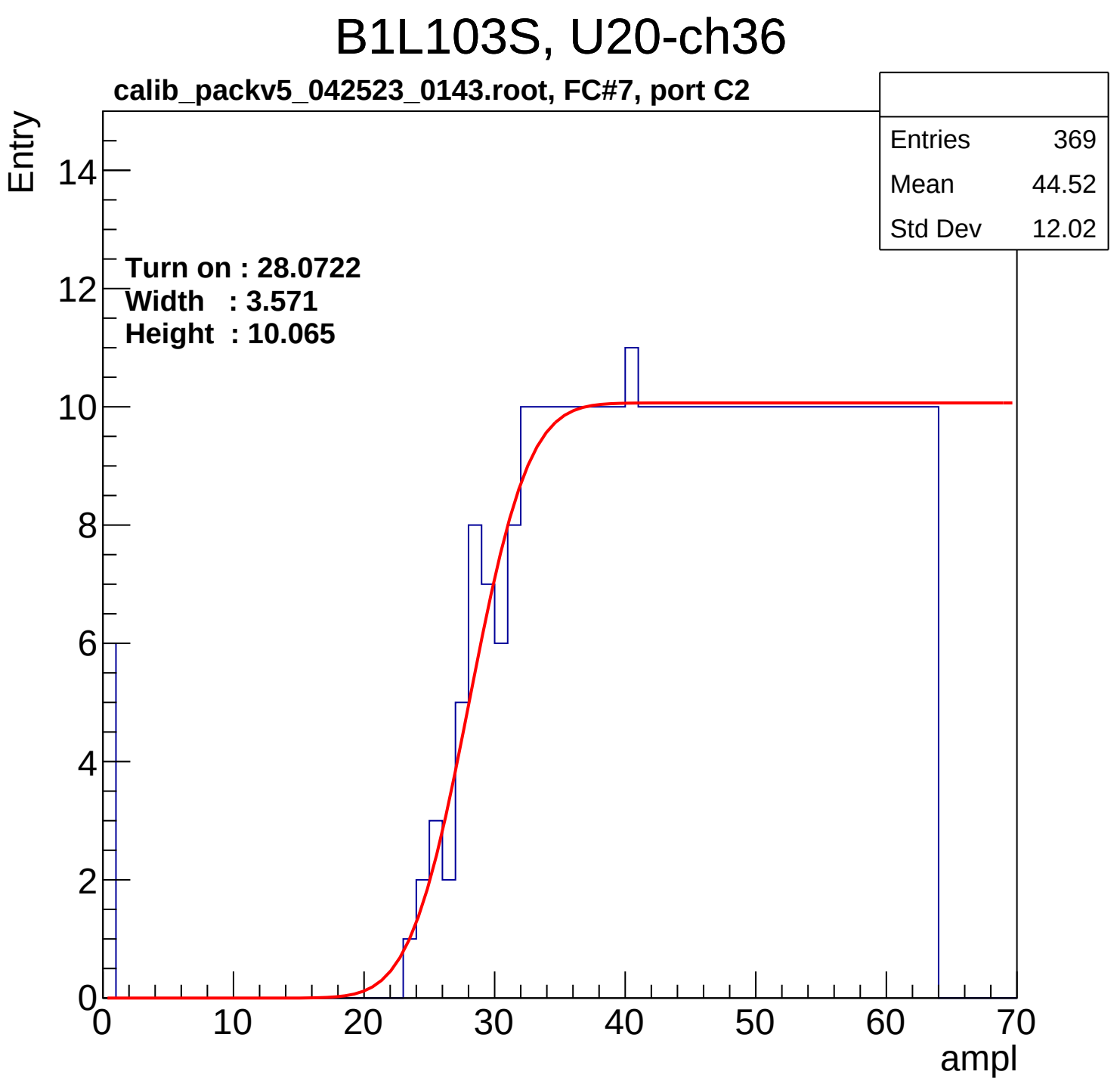
B1L103S, U20-ch36
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.52
Std Dev 12.02
Turn on : 28.0722
Width : 3.571
Height : 10.065
Entry
ampl
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2
4
6
8
10
12
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0
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60
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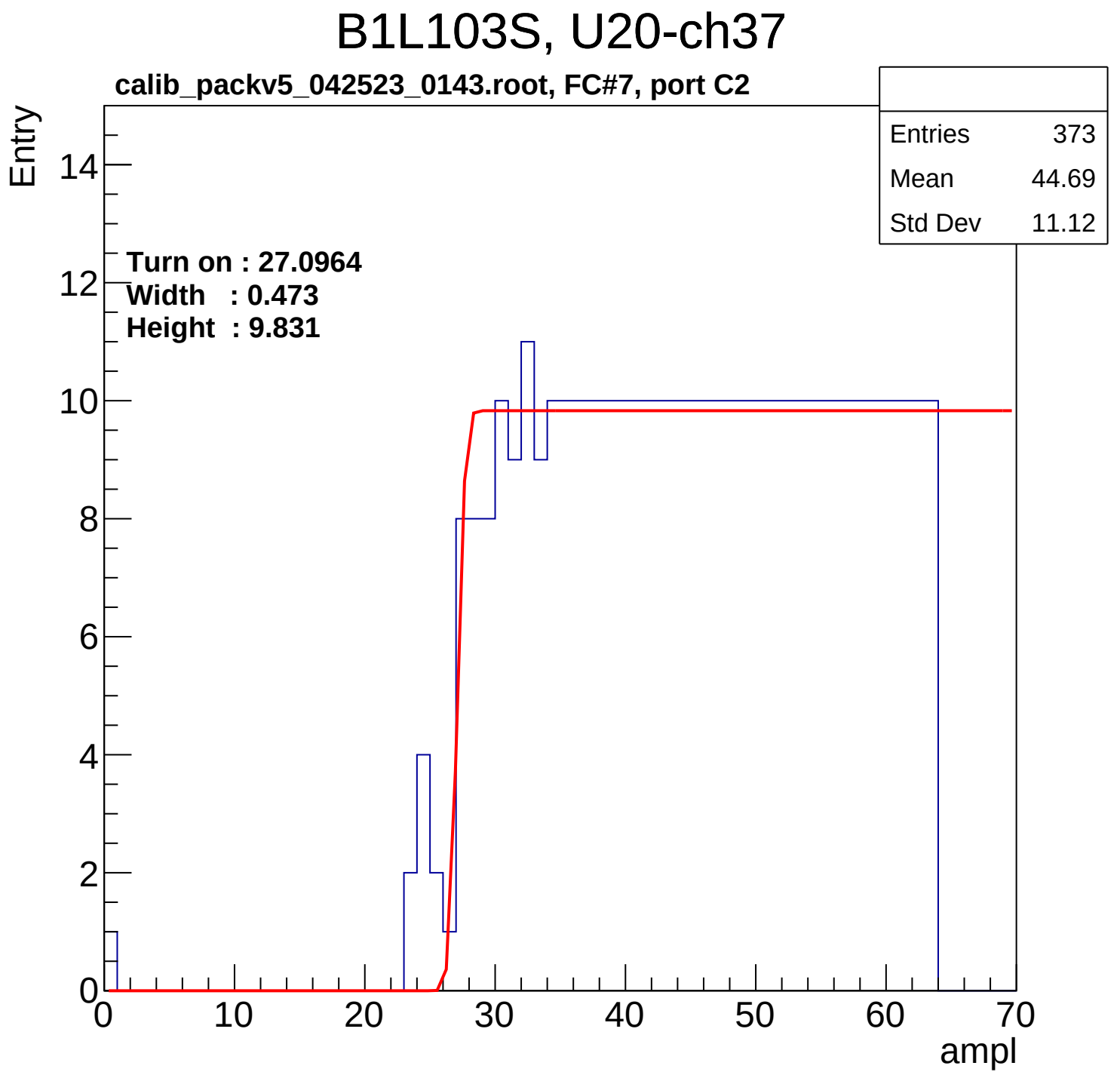
B1L103S, U20-ch37
calib_packv5_042523_0143.root, FC#7, port C2
Entries 373
Mean 44.69
Std Dev 11.12
Turn on : 27.0964
Width : 0.473
Height : 9.831
Entry
ampl
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2
4
6
8
10
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0
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20
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60
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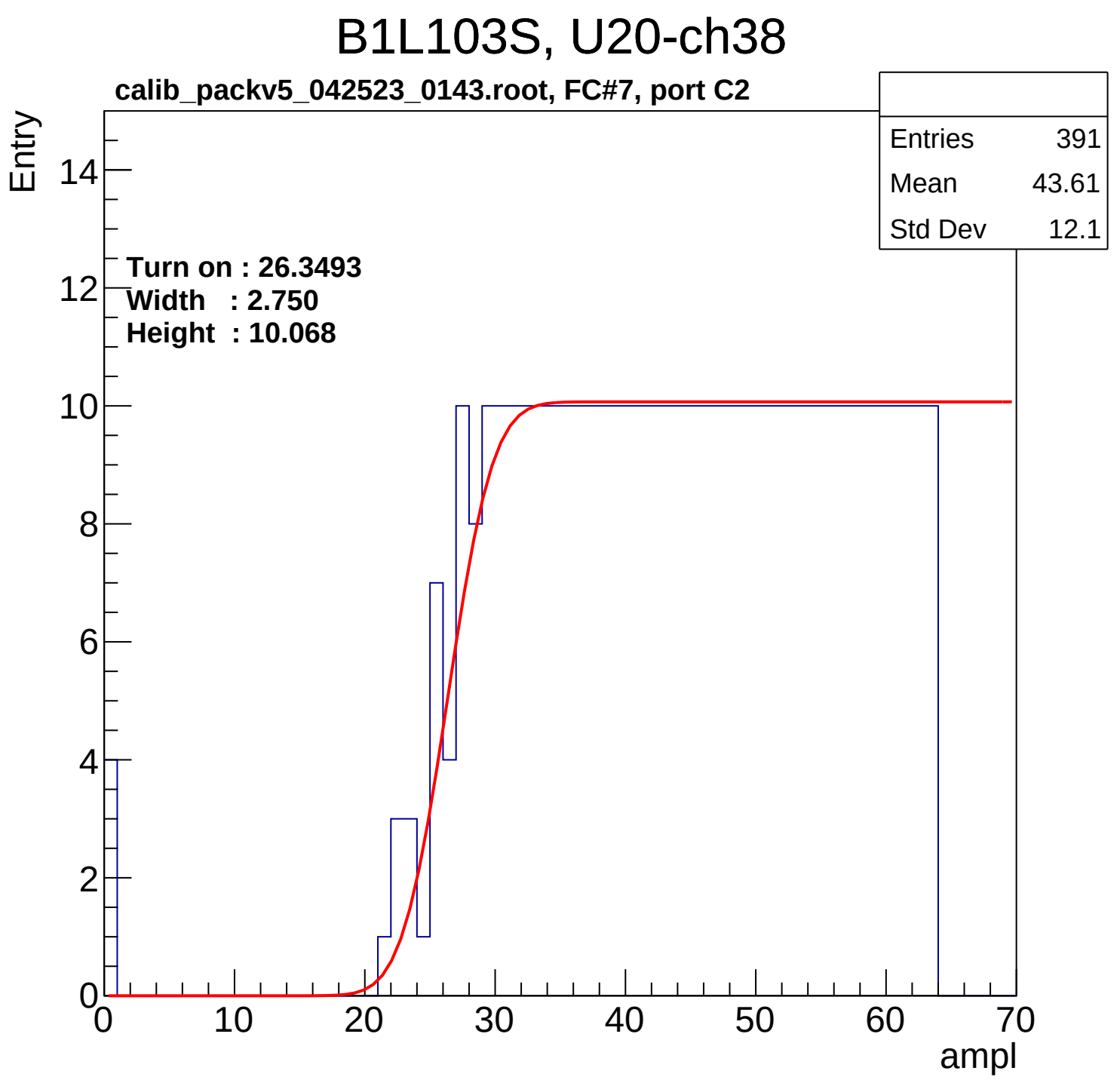
B1L103S, U20-ch38
calib_packv5_042523_0143.root, FC#7, port C2
Entries 391
Mean 43.61
Std Dev 12.1
Turn on : 26.3493
Width : 2.750
Height : 10.068
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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40
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60
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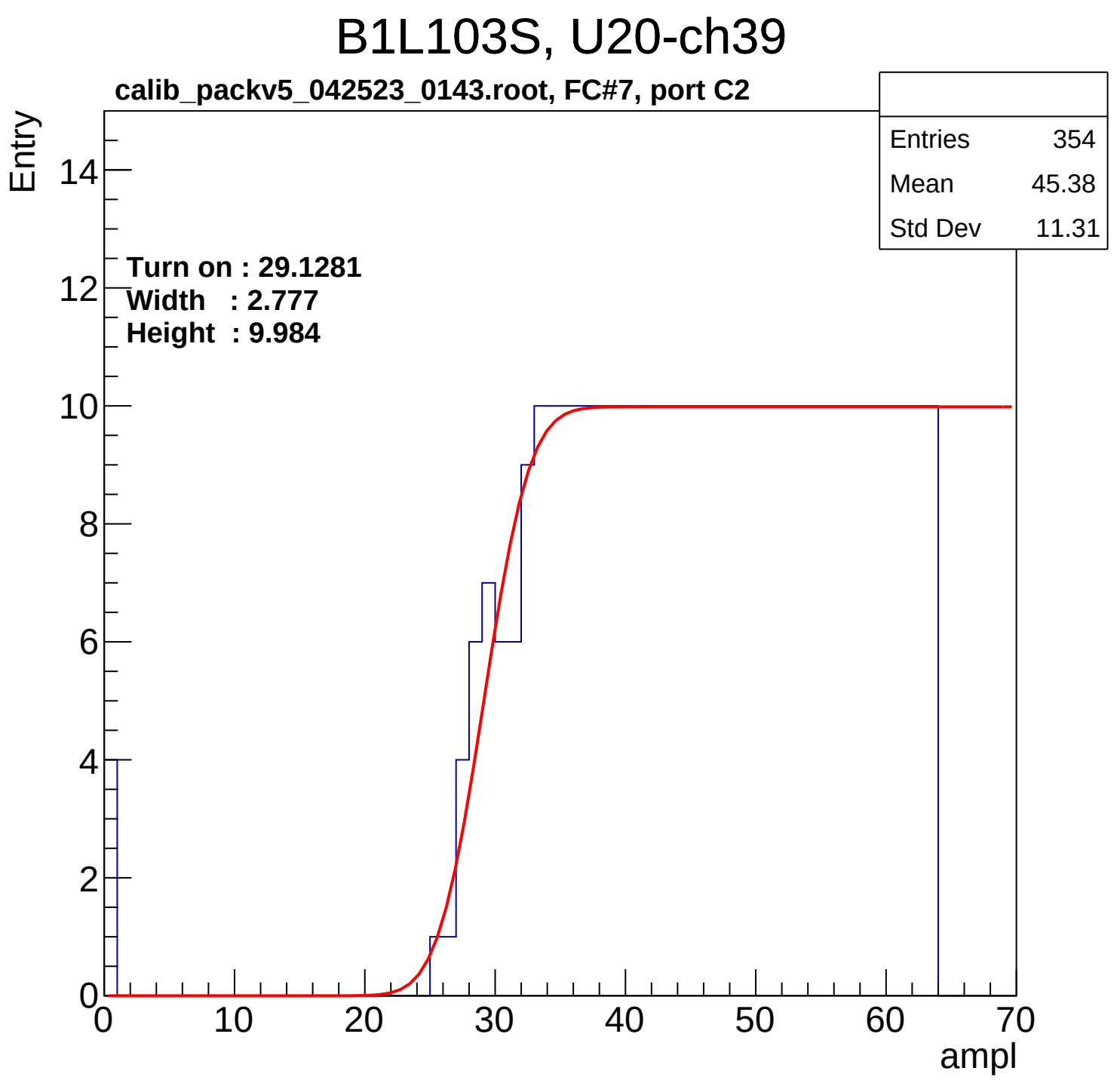
B1L103S, U20-ch39
calib_packv5_042523_0143.root, FC#7, port C2
Entries 354
Mean 45.38
Std Dev 11.31
Turn on : 29.1281
Width : 2.777
Height : 9.984
Entry
ampl
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2
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6
8
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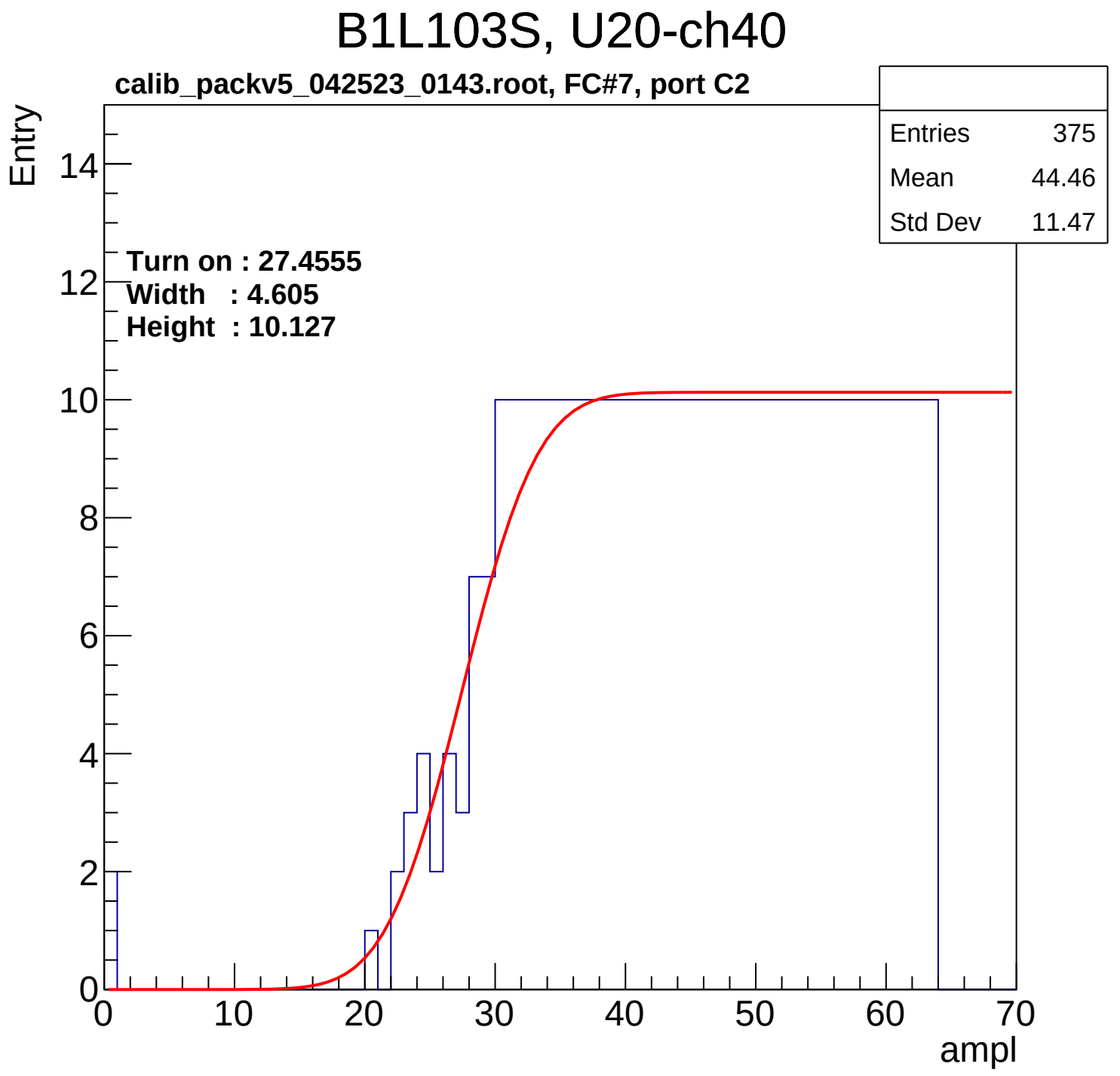
B1L103S, U20-ch40
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.46
Std Dev 11.47
Turn on : 27.4555
Width : 4.605
Height : 10.127
Entry
ampl
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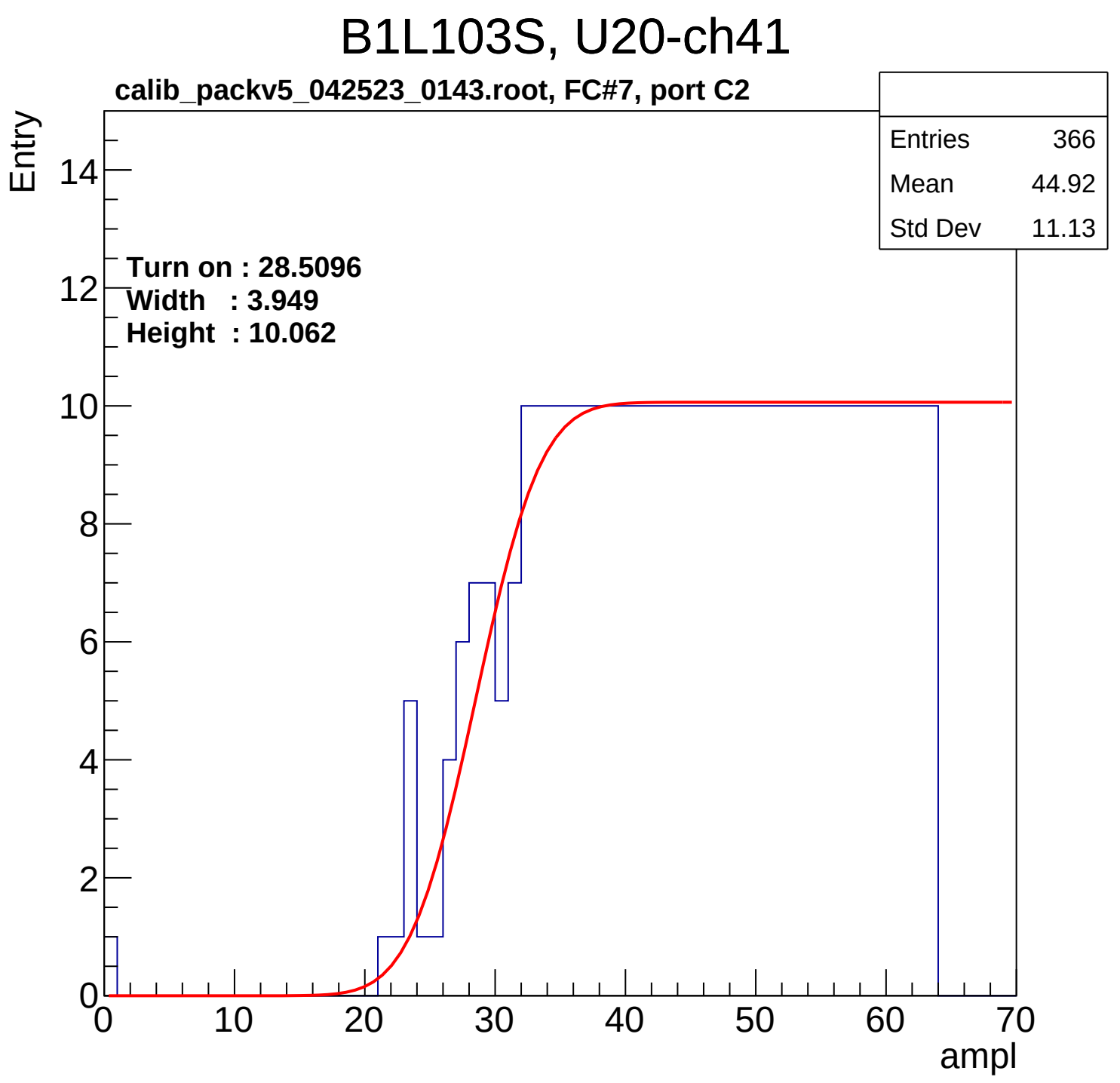
B1L103S, U20-ch41
calib_packv5_042523_0143.root, FC#7, port C2
Entries 366
Mean 44.92
Std Dev 11.13
Turn on : 28.5096
Width : 3.949
Height : 10.062
Entry
ampl
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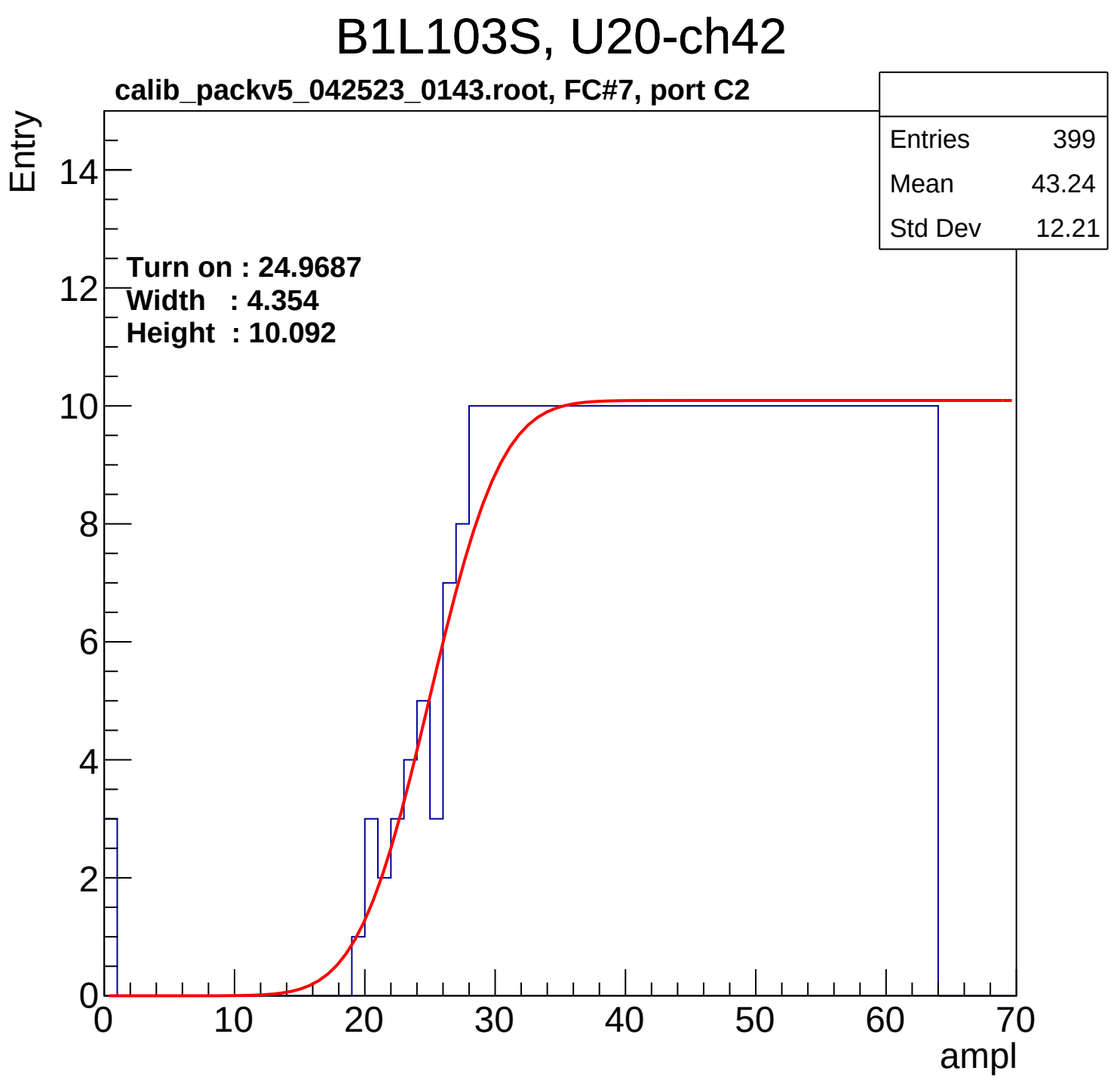
B1L103S, U20-ch42
calib_packv5_042523_0143.root, FC#7, port C2
Entries 399
Mean 43.24
Std Dev 12.21
Turn on : 24.9687
Width : 4.354
Height : 10.092
Entry
ampl
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6
8
10
12
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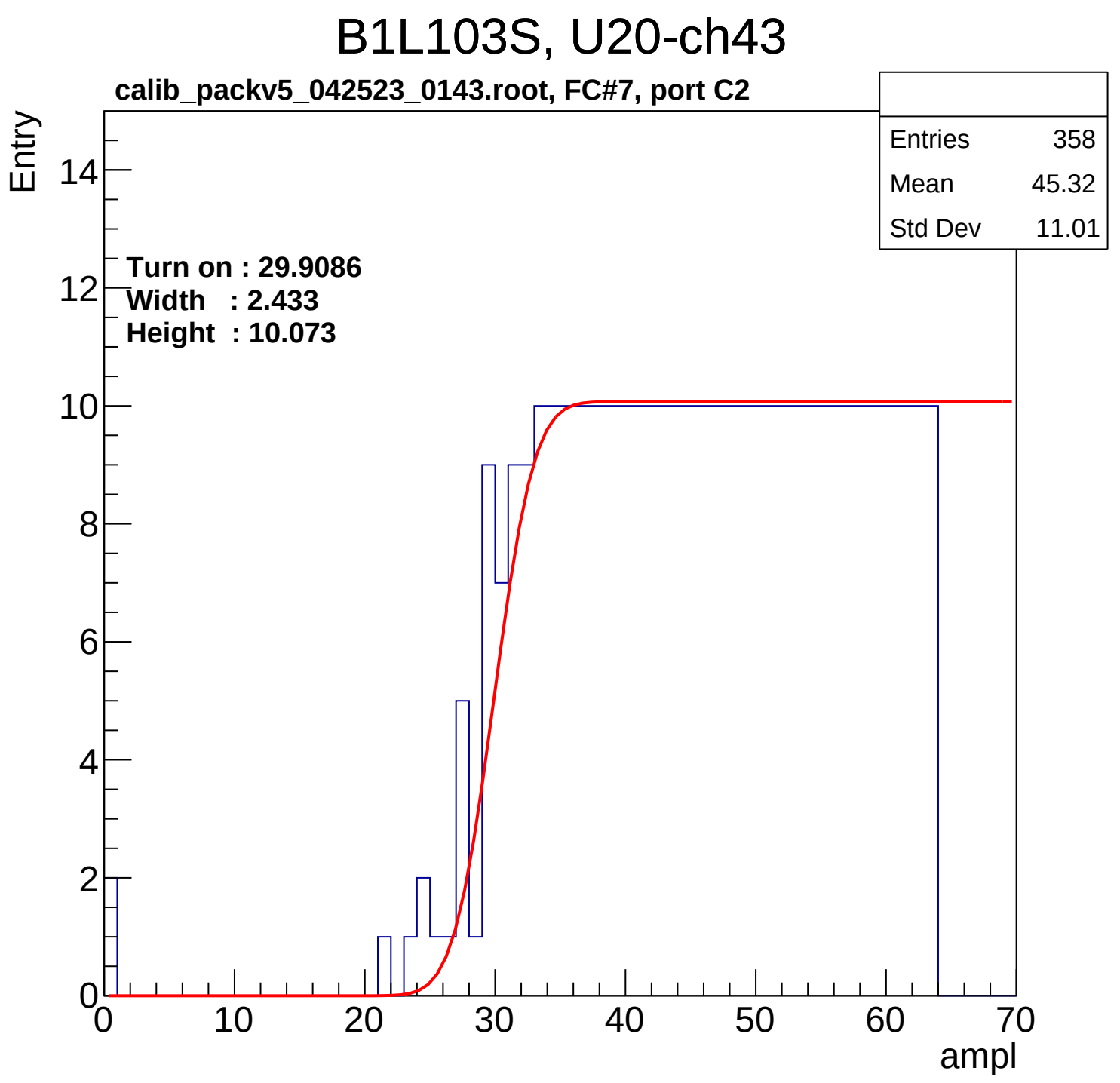
B1L103S, U20-ch43
calib_packv5_042523_0143.root, FC#7, port C2
Entries 358
Mean 45.32
Std Dev 11.01
Turn on : 29.9086
Width : 2.433
Height : 10.073
Entry
ampl
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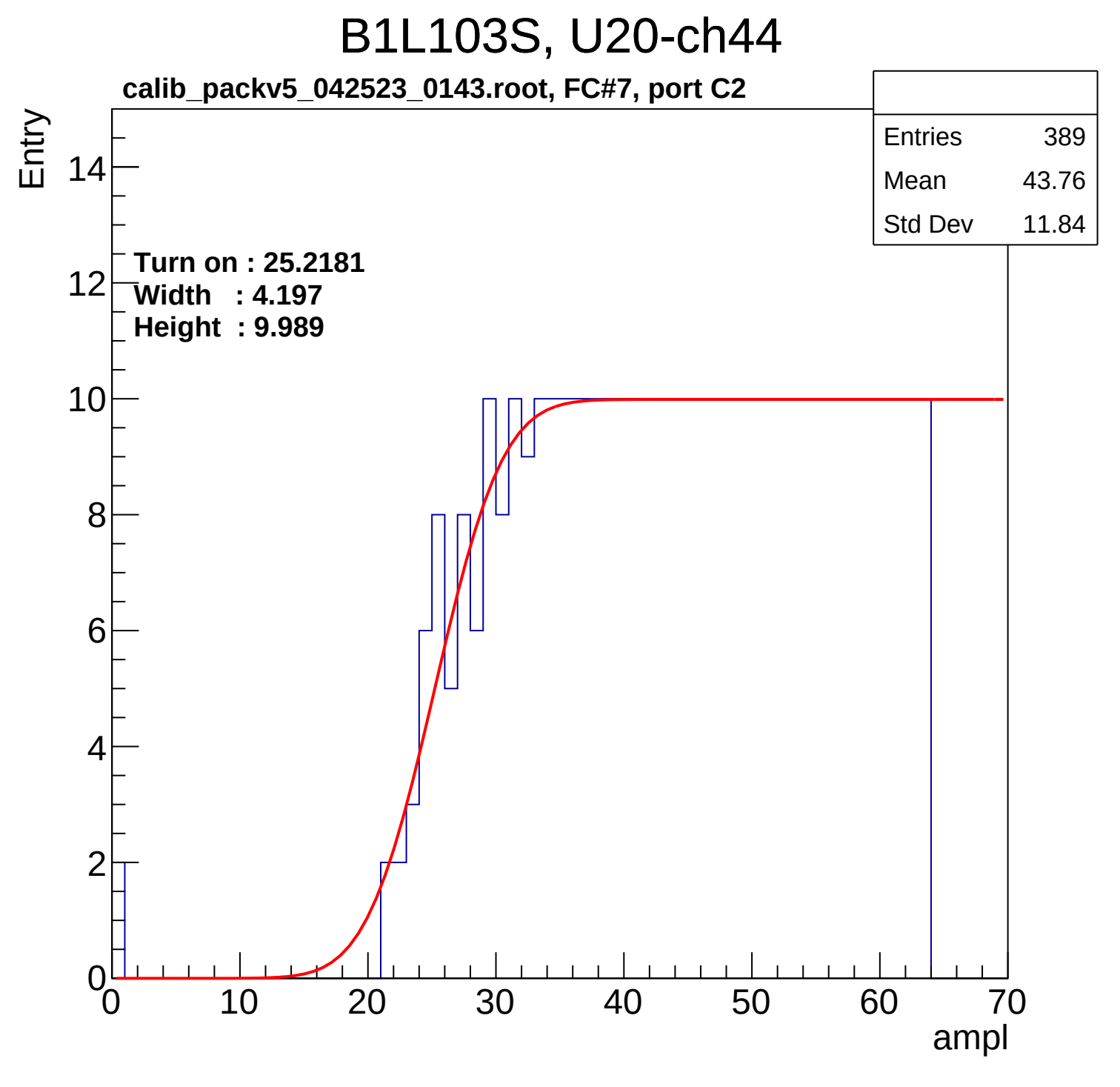
B1L103S, U20-ch44
calib_packv5_042523_0143.root, FC#7, port C2
Entries 389
Mean 43.76
Std Dev 11.84
Turn on : 25.2181
Width : 4.197
Height : 9.989
Entry
ampl
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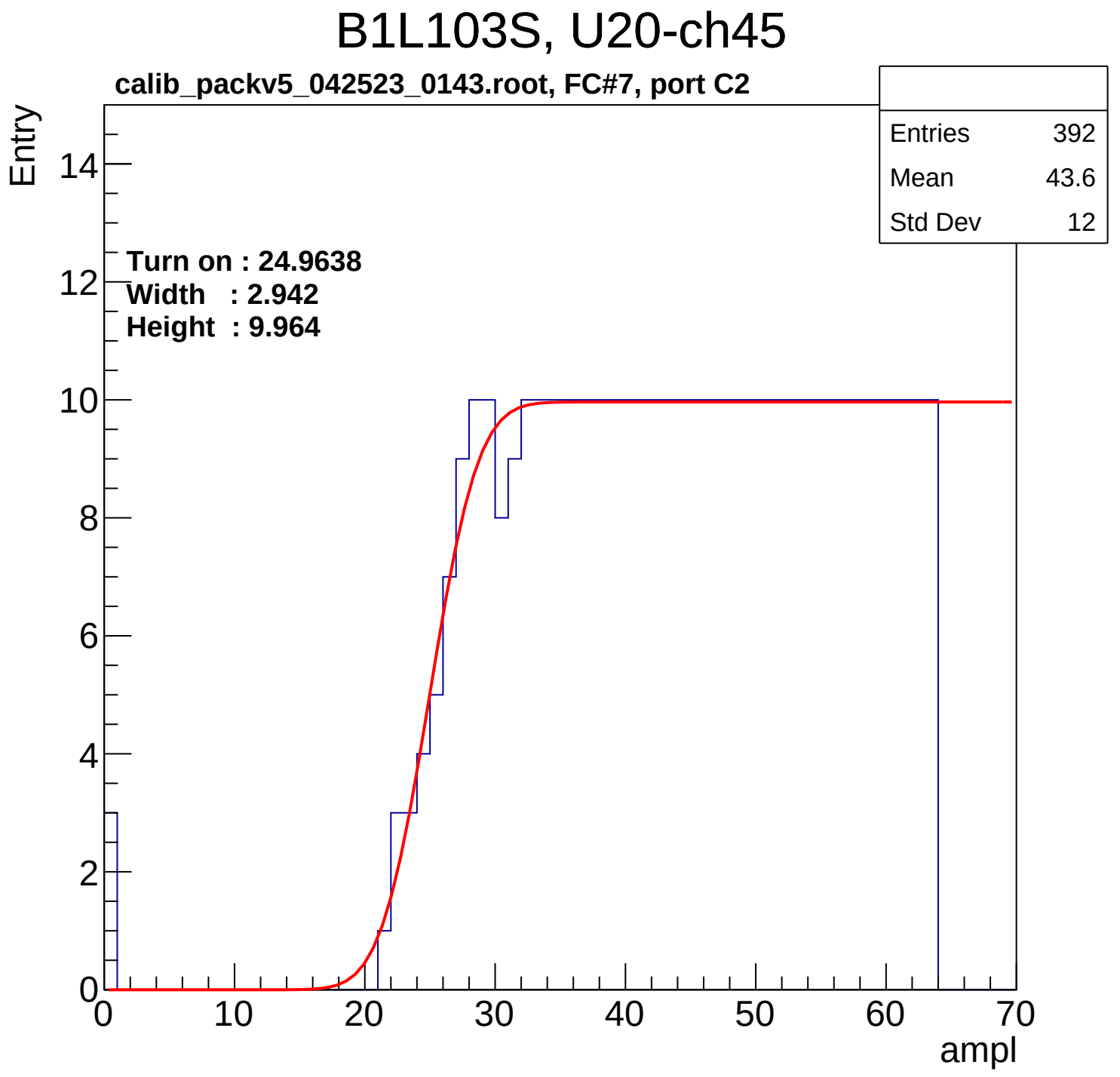
B1L103S, U20-ch45
calib_packv5_042523_0143.root, FC#7, port C2
Entries 392
Mean 43.6
Std Dev 12
Turn on : 24.9638
Width : 2.942
Height : 9.964
Entry
ampl
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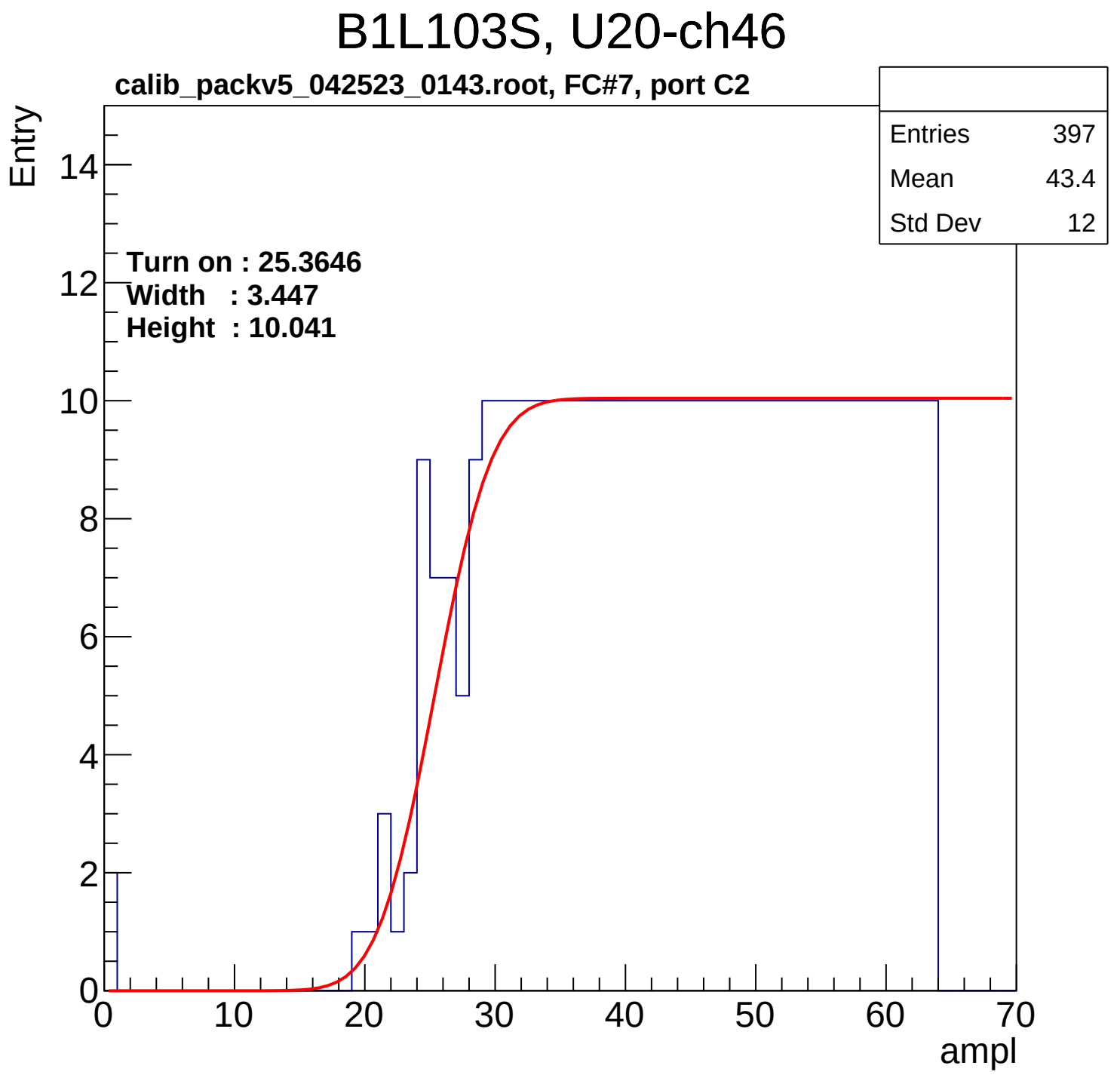
B1L103S, U20-ch46
calib_packv5_042523_0143.root, FC#7, port C2
Entries 397
Mean 43.4
Std Dev 12
Turn on : 25.3646
Width : 3.447
Height : 10.041
Entry
ampl
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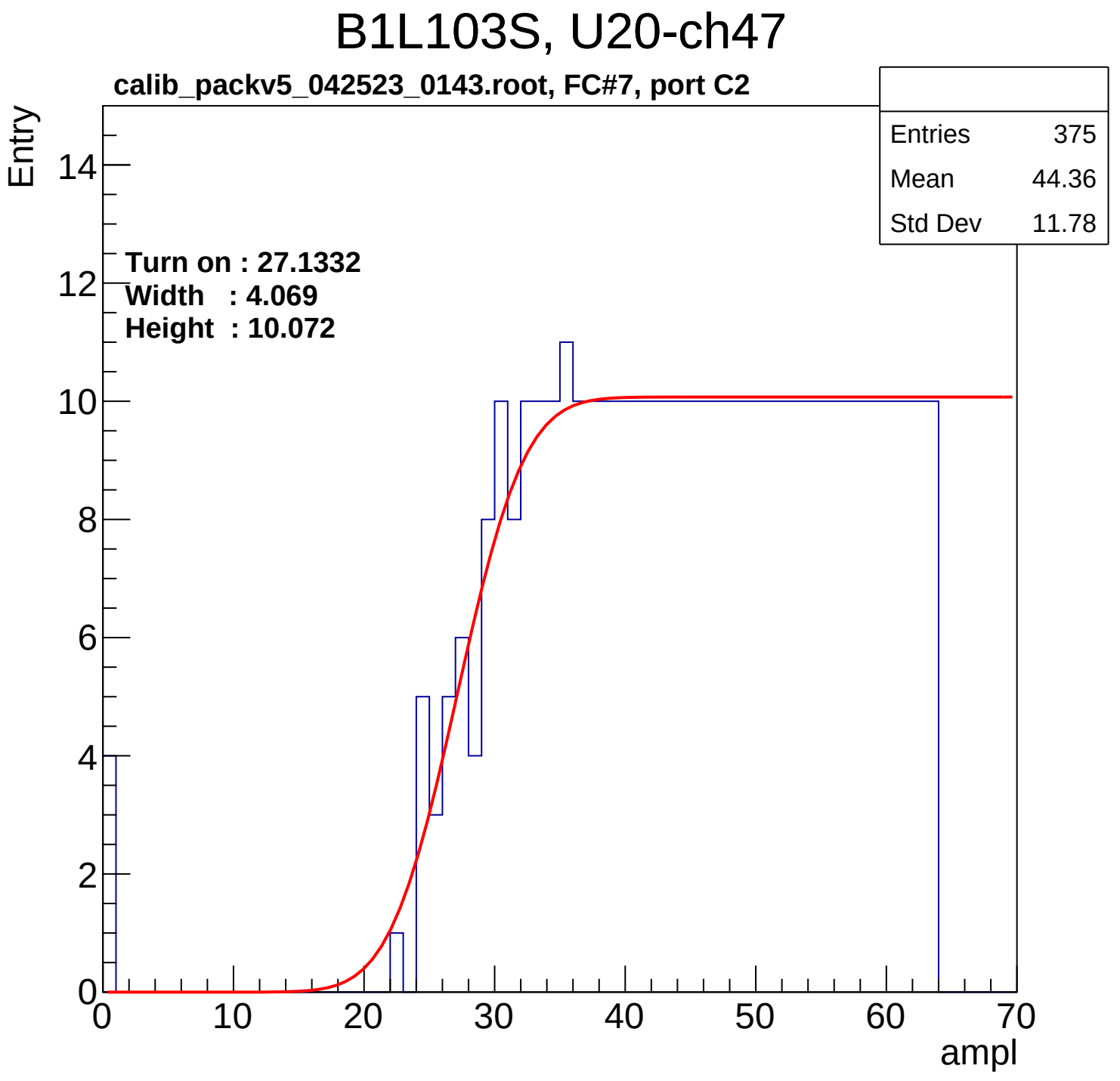
B1L103S, U20-ch47
calib_packv5_042523_0143.root, FC#7, port C2
Entries 375
Mean 44.36
Std Dev 11.78
Turn on : 27.1332
Width : 4.069
Height : 10.072
Entry
ampl
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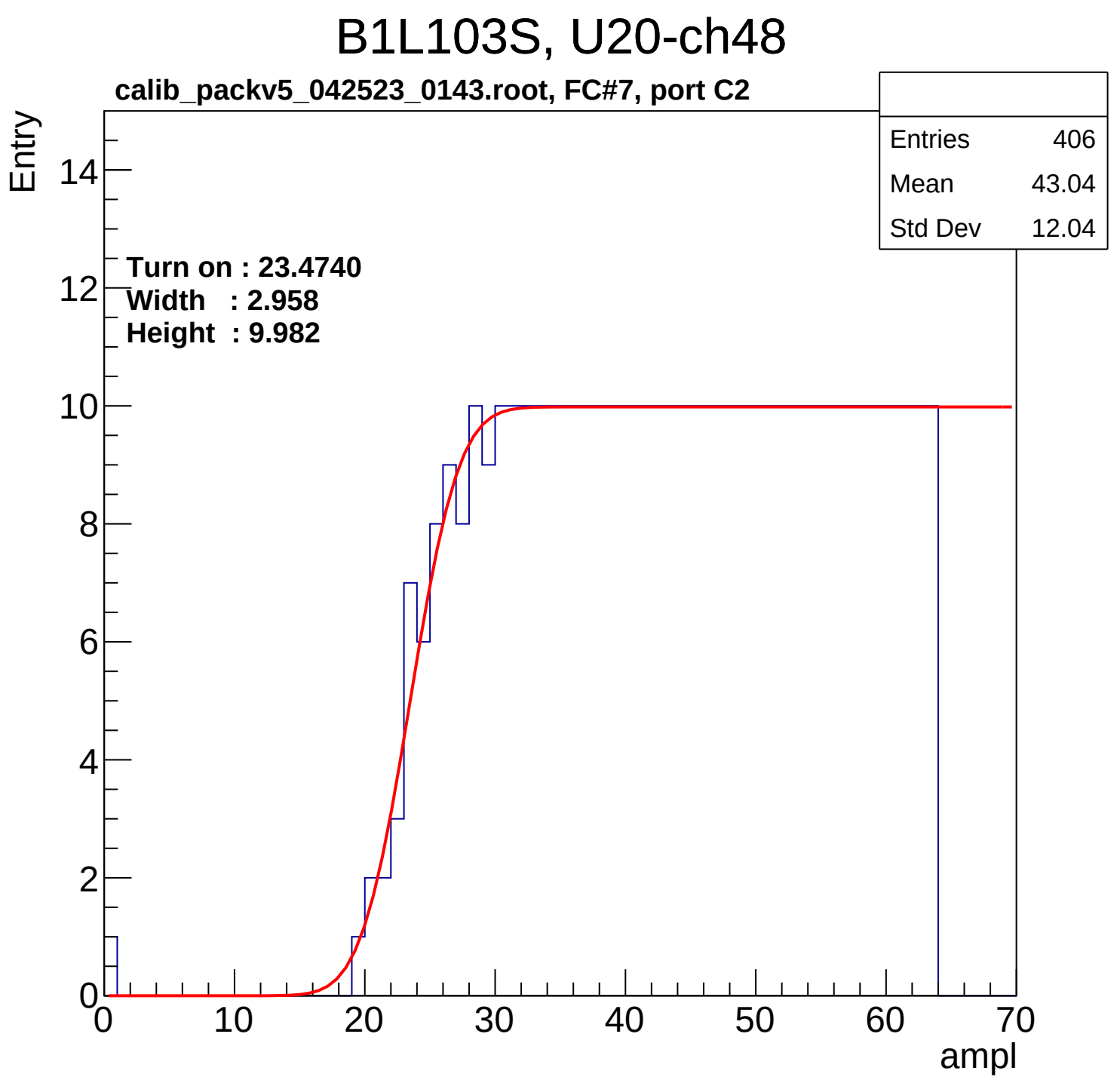
B1L103S, U20-ch48
calib_packv5_042523_0143.root, FC#7, port C2
Entries 406
Mean 43.04
Std Dev 12.04
Turn on : 23.4740
Width : 2.958
Height : 9.982
Entry
ampl
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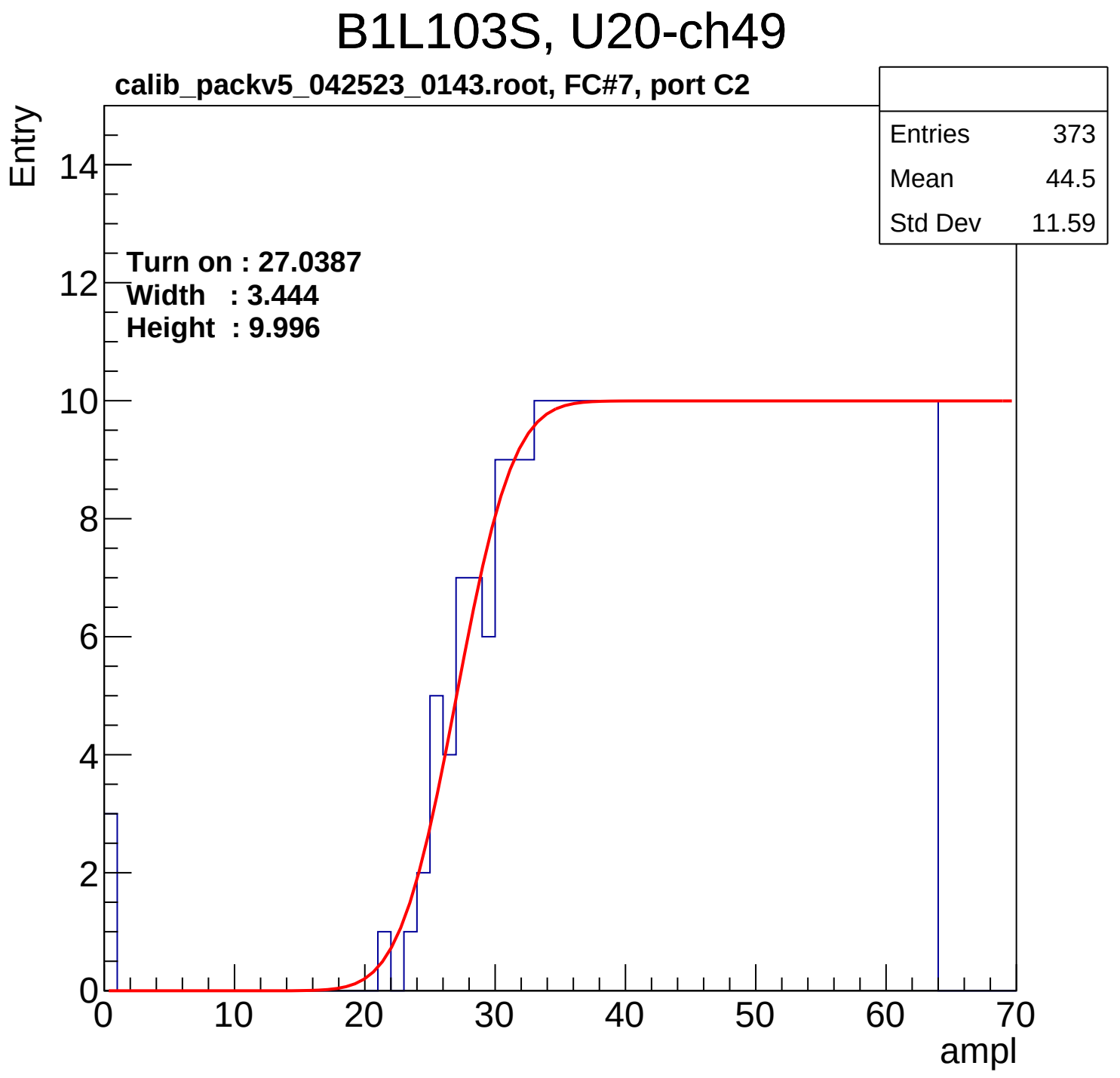
B1L103S, U20-ch49
calib_packv5_042523_0143.root, FC#7, port C2
Entries 373
Mean 44.5
Std Dev 11.59
Turn on : 27.0387
Width : 3.444
Height : 9.996
Entry
ampl
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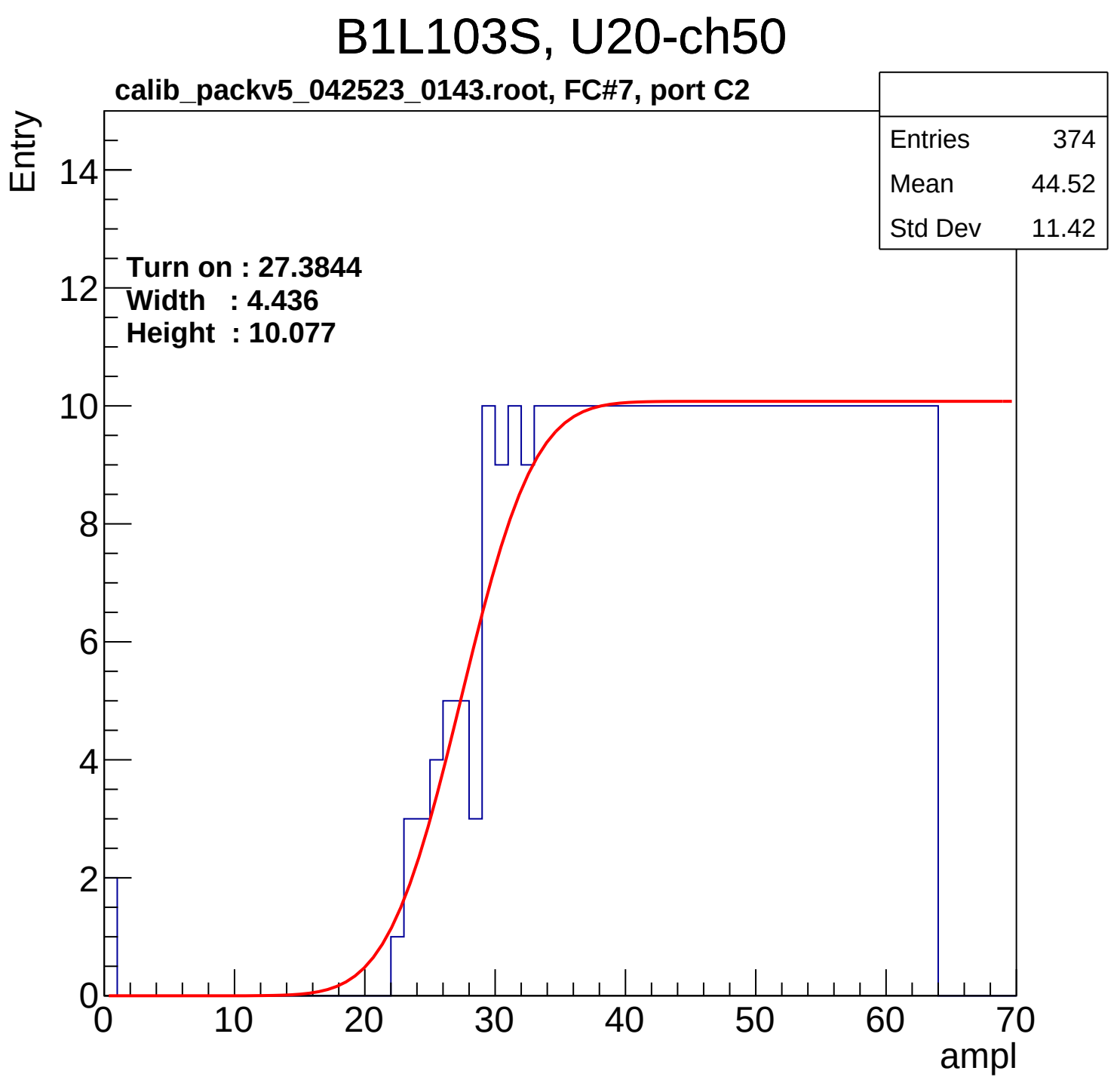
B1L103S, U20-ch50
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.52
Std Dev 11.42
Turn on : 27.3844
Width : 4.436
Height : 10.077
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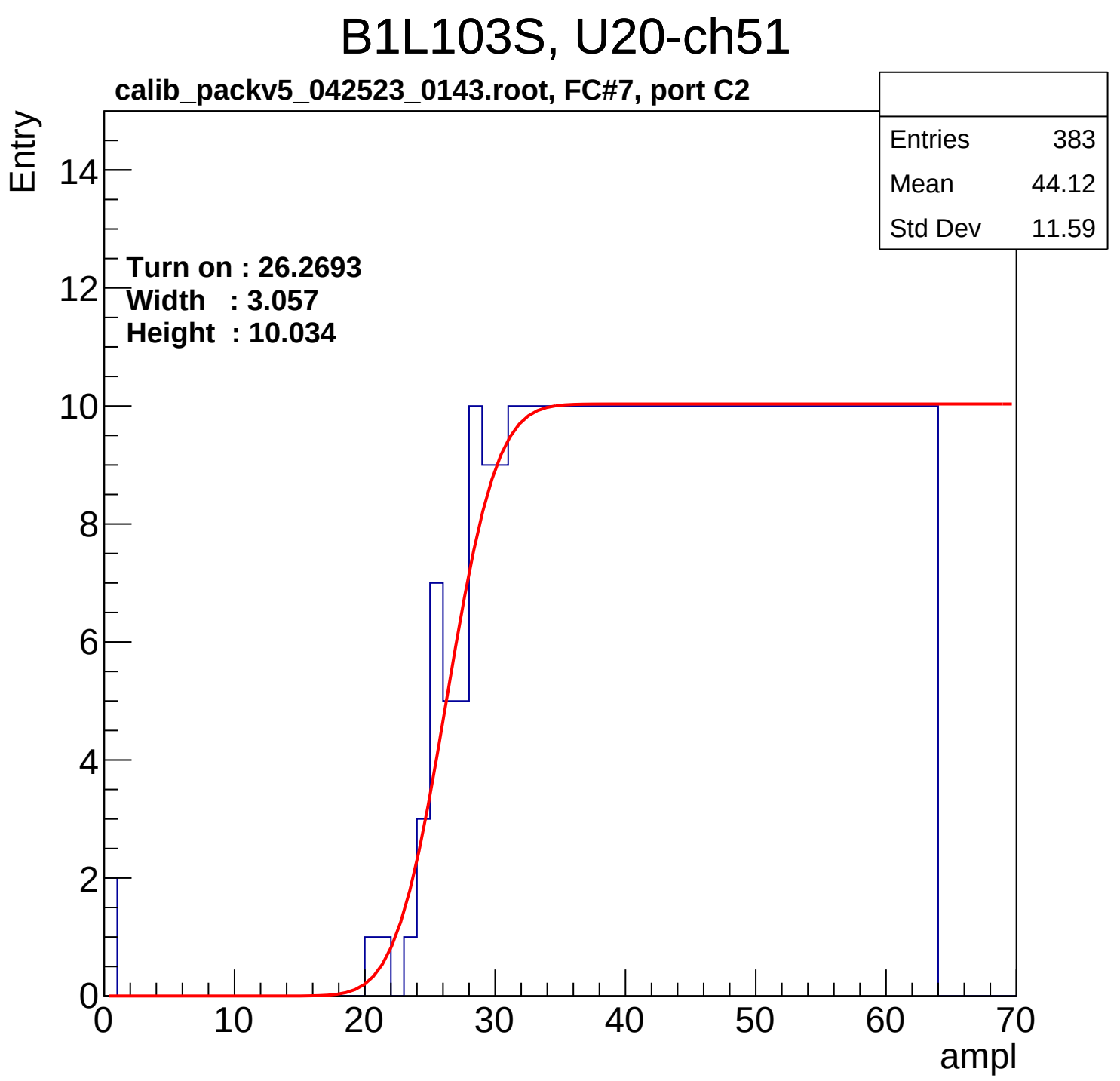
B1L103S, U20-ch51
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 44.12
Std Dev 11.59
Turn on : 26.2693
Width : 3.057
Height : 10.034
Entry
ampl
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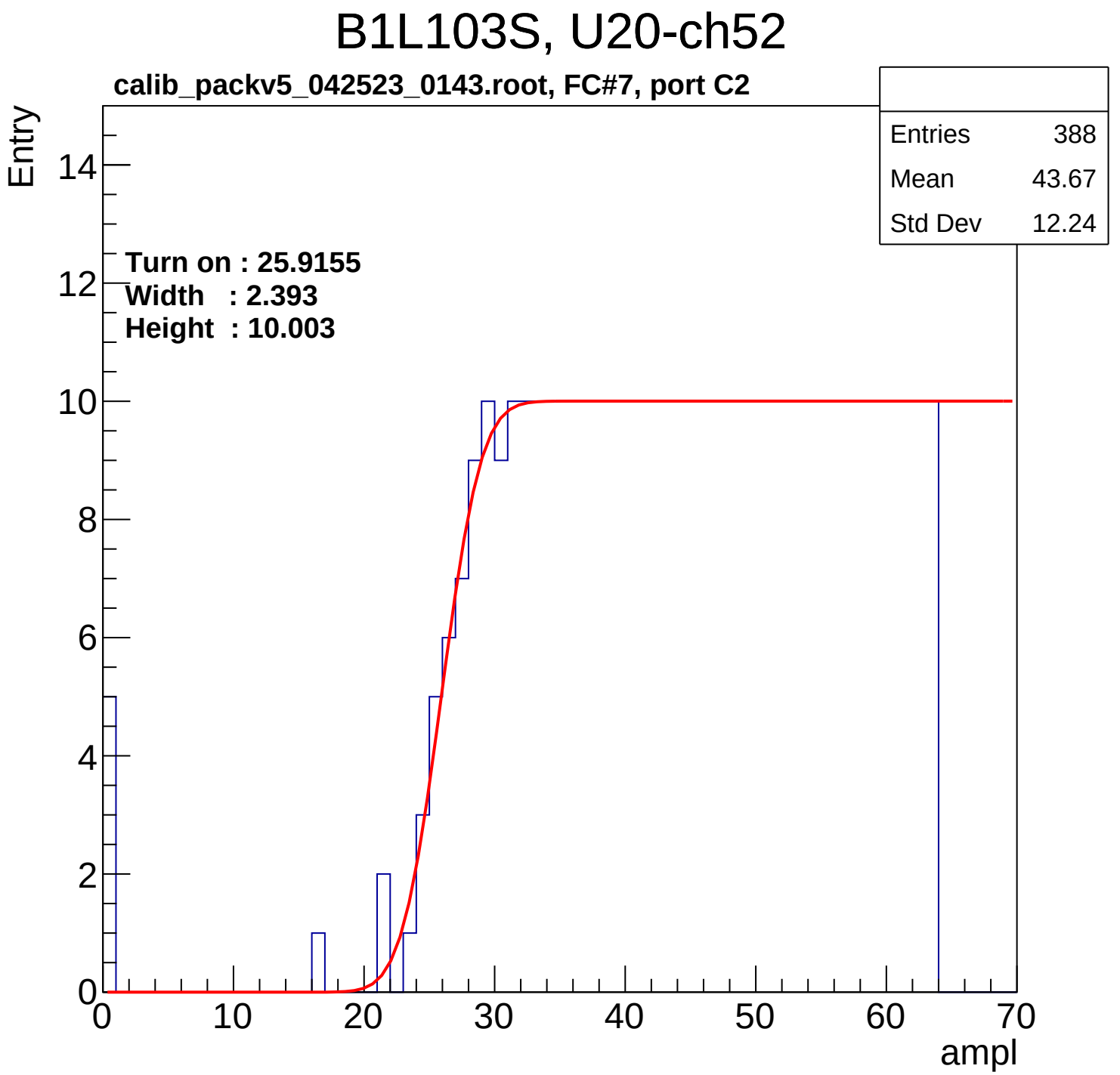
B1L103S, U20-ch52
calib_packv5_042523_0143.root, FC#7, port C2
Entries 388
Mean 43.67
Std Dev 12.24
Turn on : 25.9155
Width : 2.393
Height : 10.003
Entry
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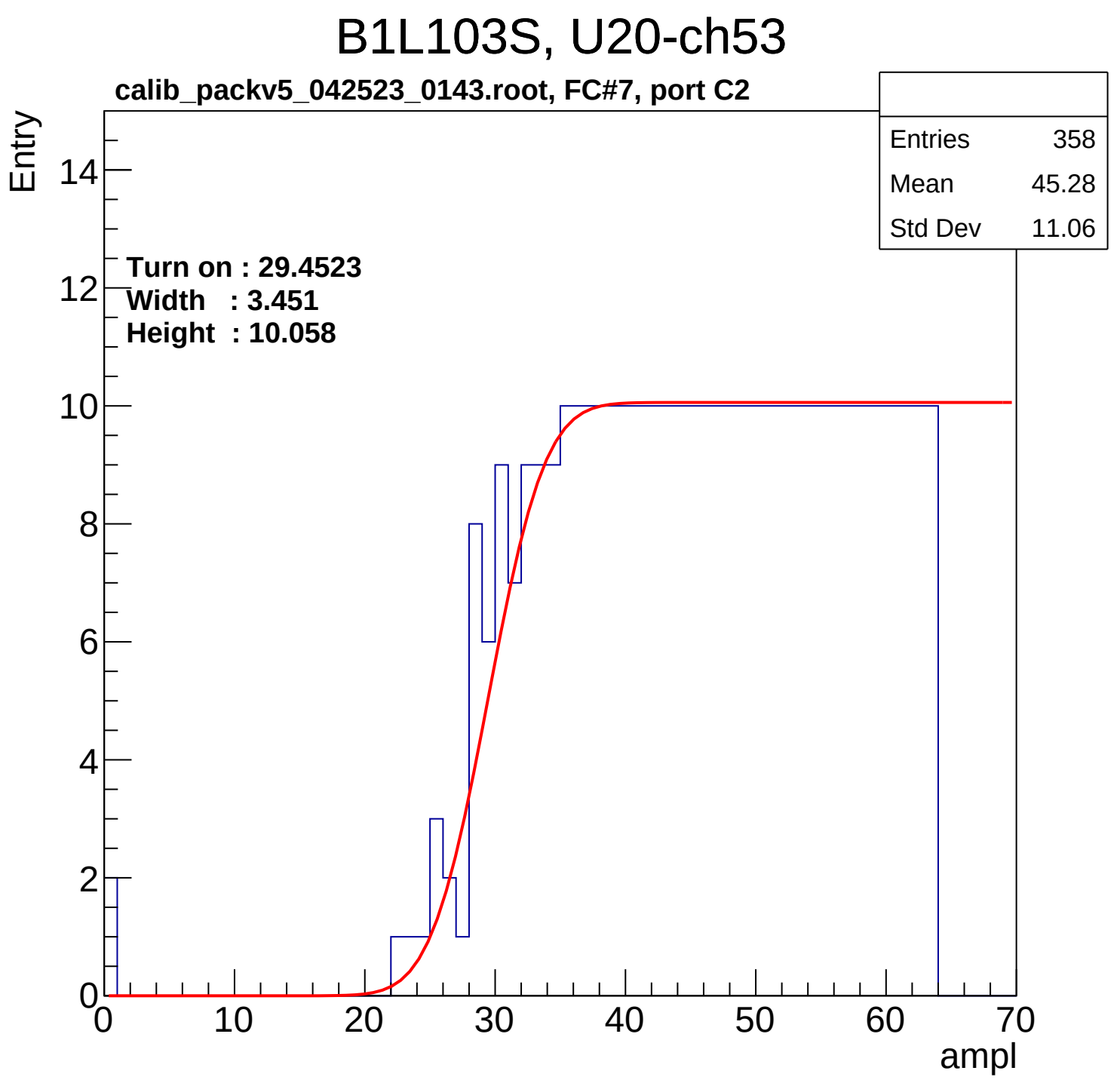
B1L103S, U20-ch53
calib_packv5_042523_0143.root, FC#7, port C2
Entries 358
Mean 45.28
Std Dev 11.06
Turn on : 29.4523
Width : 3.451
Height : 10.058
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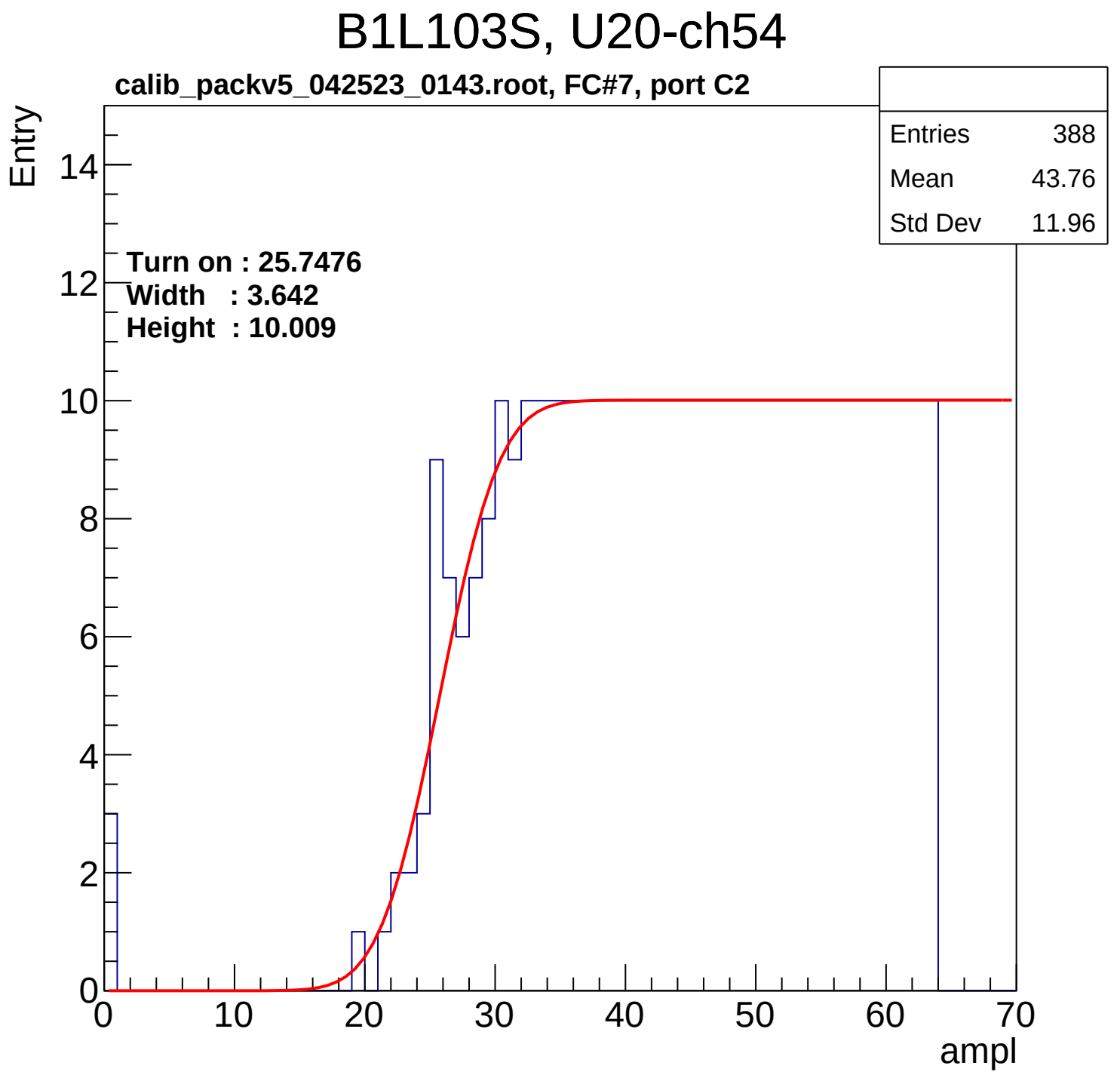
B1L103S, U20-ch54
calib_packv5_042523_0143.root, FC#7, port C2
Entries 388
Mean 43.76
Std Dev 11.96
Turn on : 25.7476
Width : 3.642
Height : 10.009
Entry
ampl
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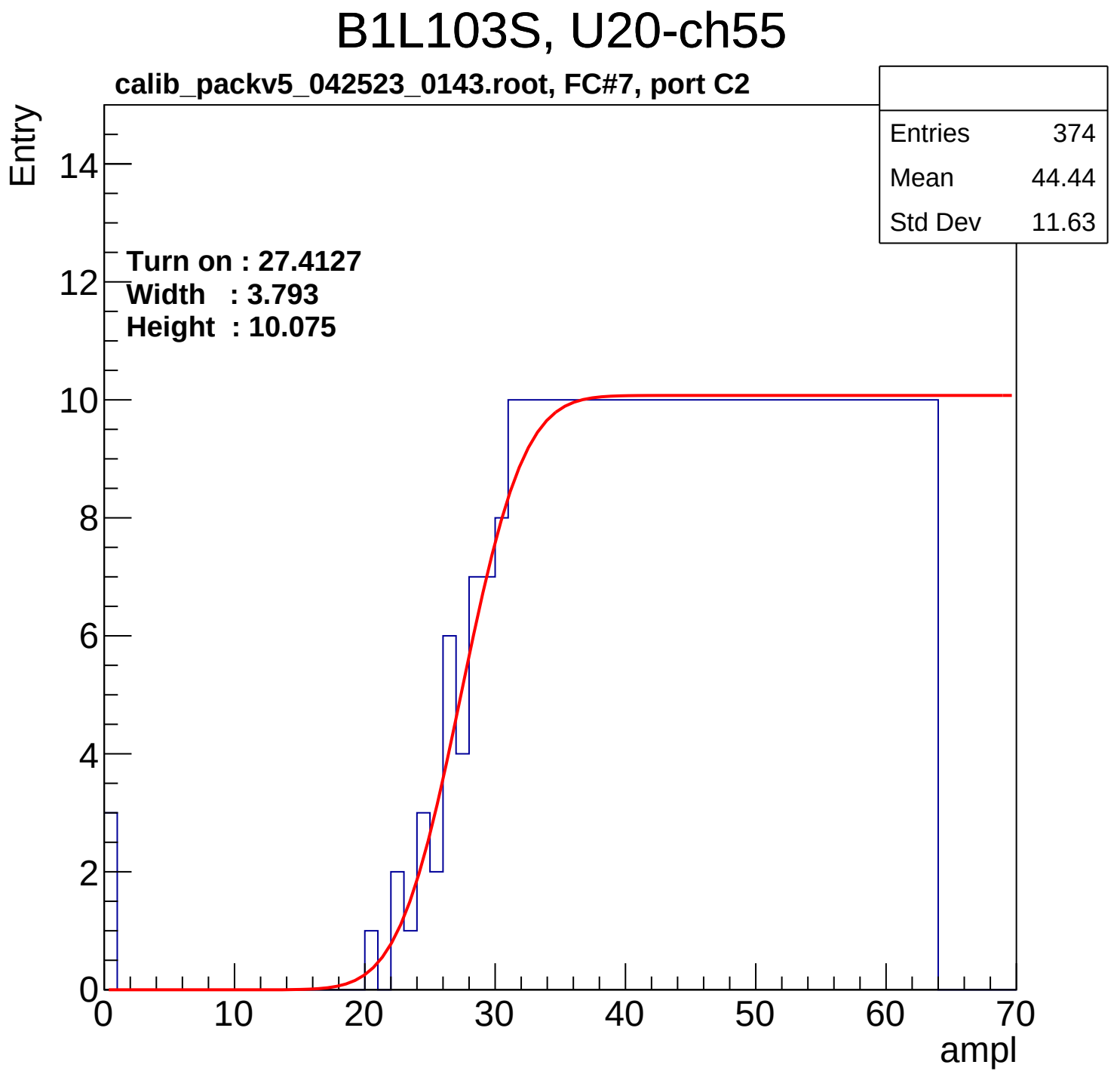
B1L103S, U20-ch55
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.44
Std Dev 11.63
Turn on : 27.4127
Width : 3.793
Height : 10.075
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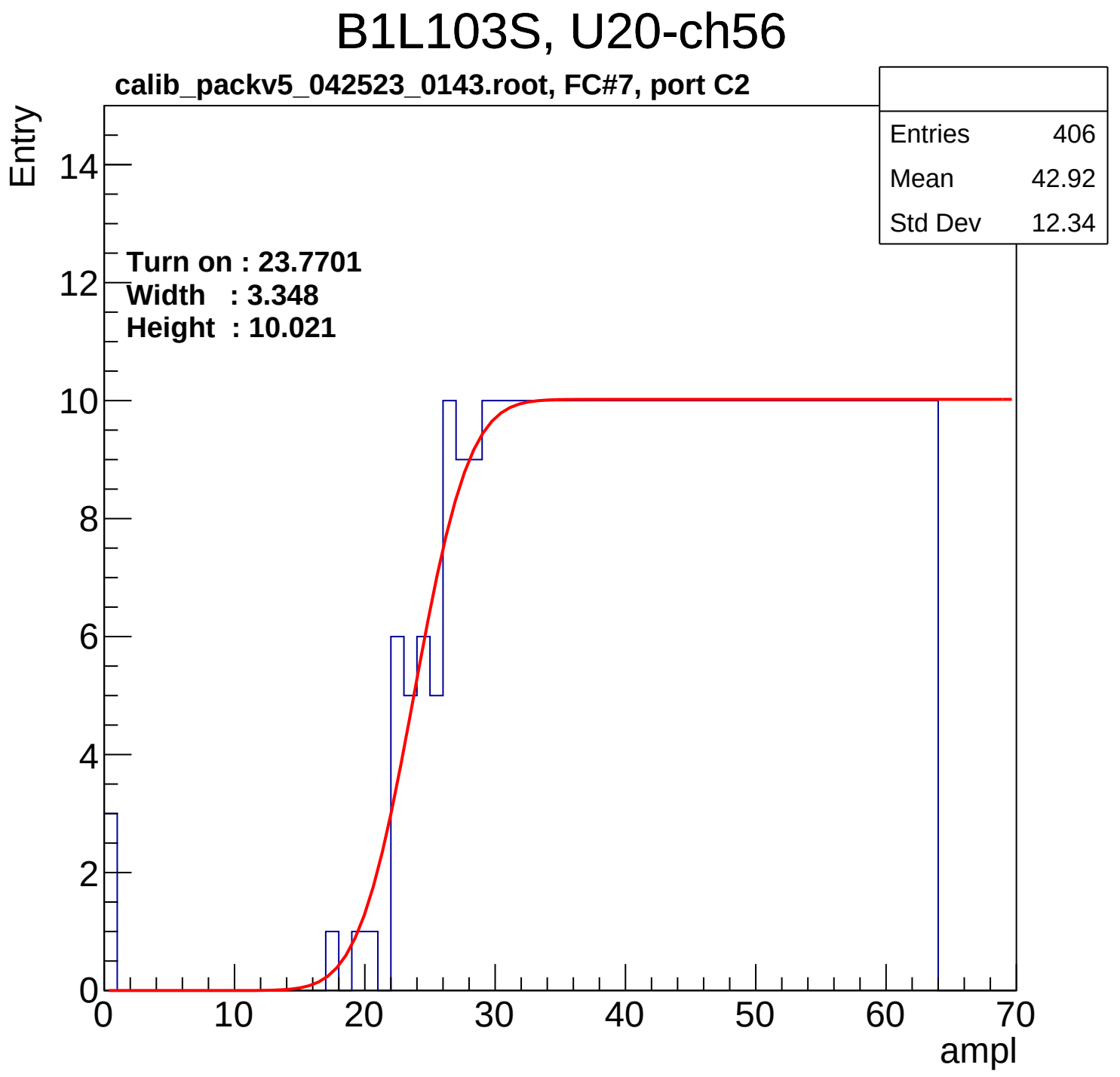
B1L103S, U20-ch56
calib_packv5_042523_0143.root, FC#7, port C2
Entries 406
Mean 42.92
Std Dev 12.34
Turn on : 23.7701
Width : 3.348
Height : 10.021
Entry
ampl
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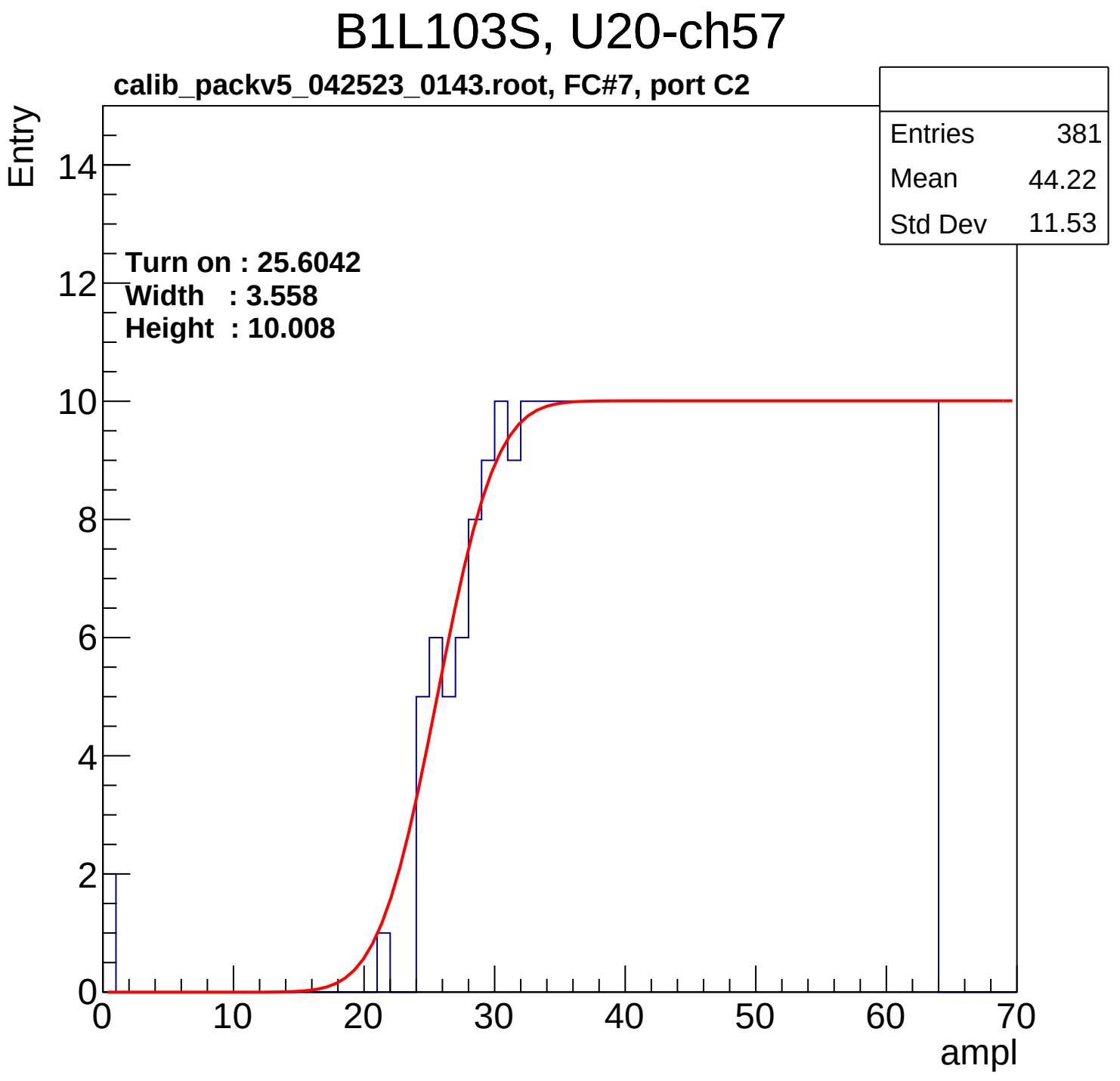
B1L103S, U20-ch57
calib_packv5_042523_0143.root, FC#7, port C2
Entries 381
Mean 44.22
Std Dev 11.53
Turn on : 25.6042
Width : 3.558
Height : 10.008
Entry
ampl
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6
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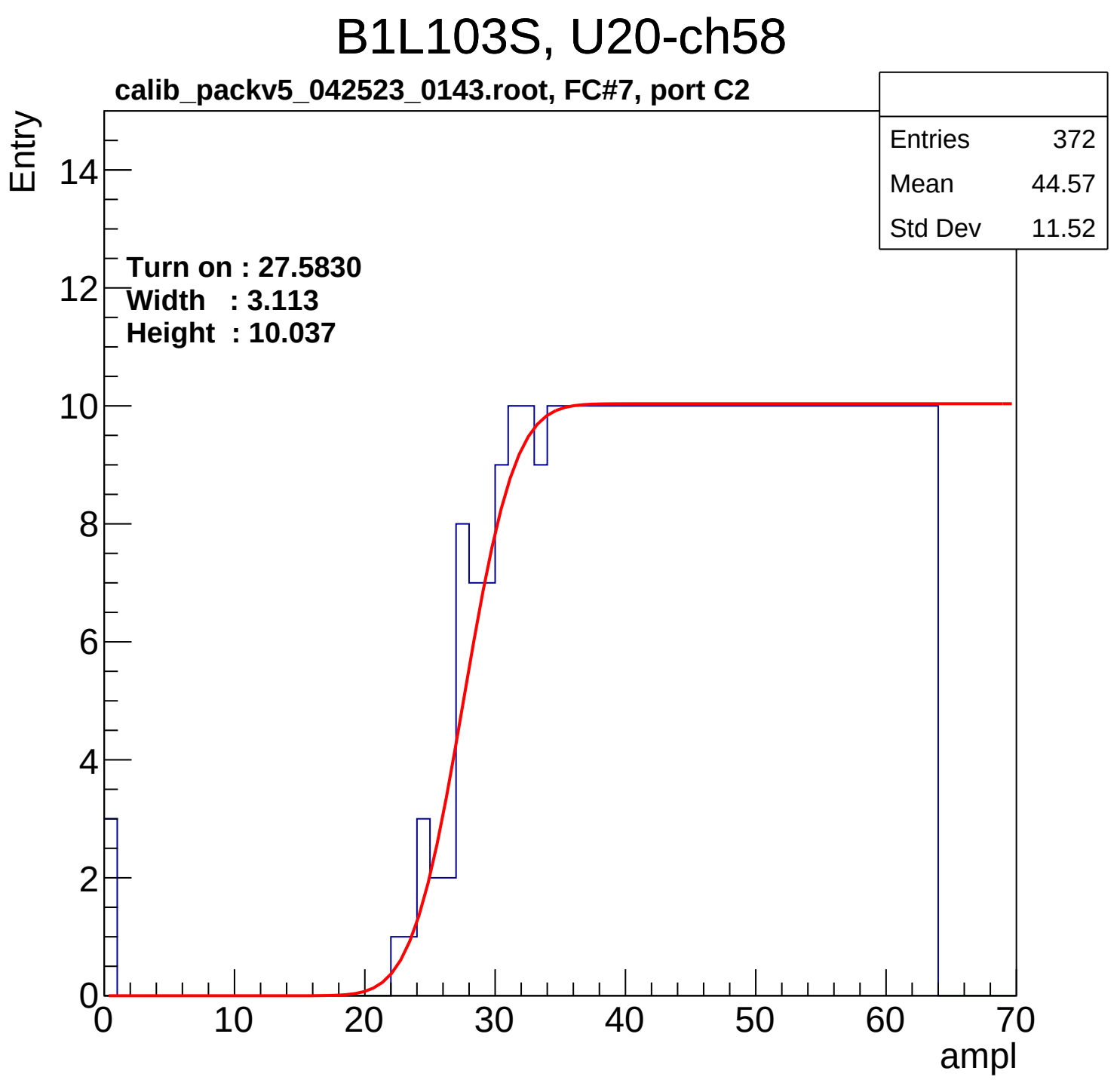
B1L103S, U20-ch58
calib_packv5_042523_0143.root, FC#7, port C2
Entries 372
Mean 44.57
Std Dev 11.52
Turn on : 27.5830
Width : 3.113
Height : 10.037
Entry
ampl
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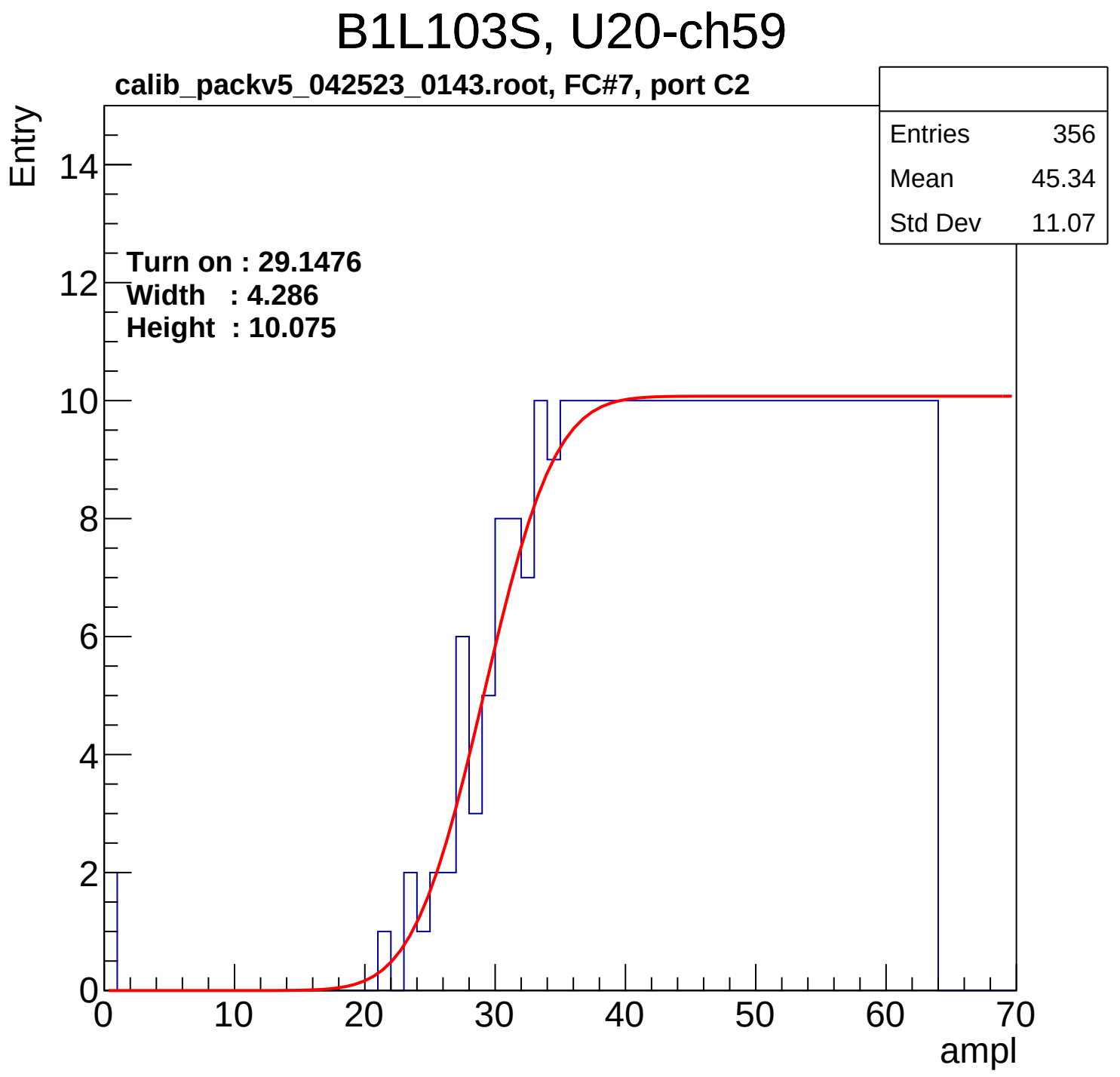
B1L103S, U20-ch59
calib_packv5_042523_0143.root, FC#7, port C2
Entries 356
Mean 45.34
Std Dev 11.07
Turn on : 29.1476
Width : 4.286
Height : 10.075
Entry
ampl
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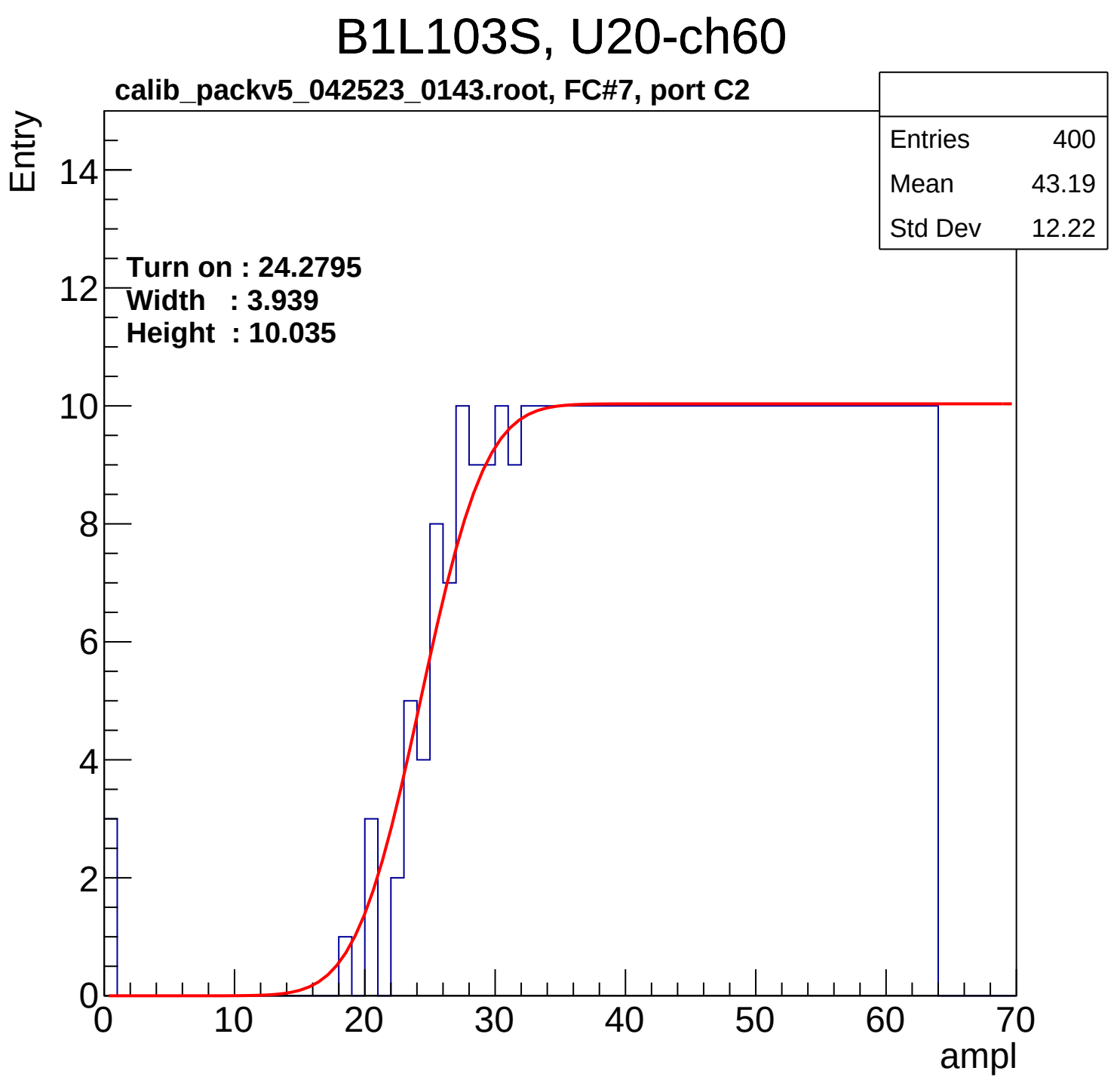
B1L103S, U20-ch60
calib_packv5_042523_0143.root, FC#7, port C2
Entries 400
Mean 43.19
Std Dev 12.22
Turn on : 24.2795
Width : 3.939
Height : 10.035
Entry
ampl
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2
4
6
8
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0
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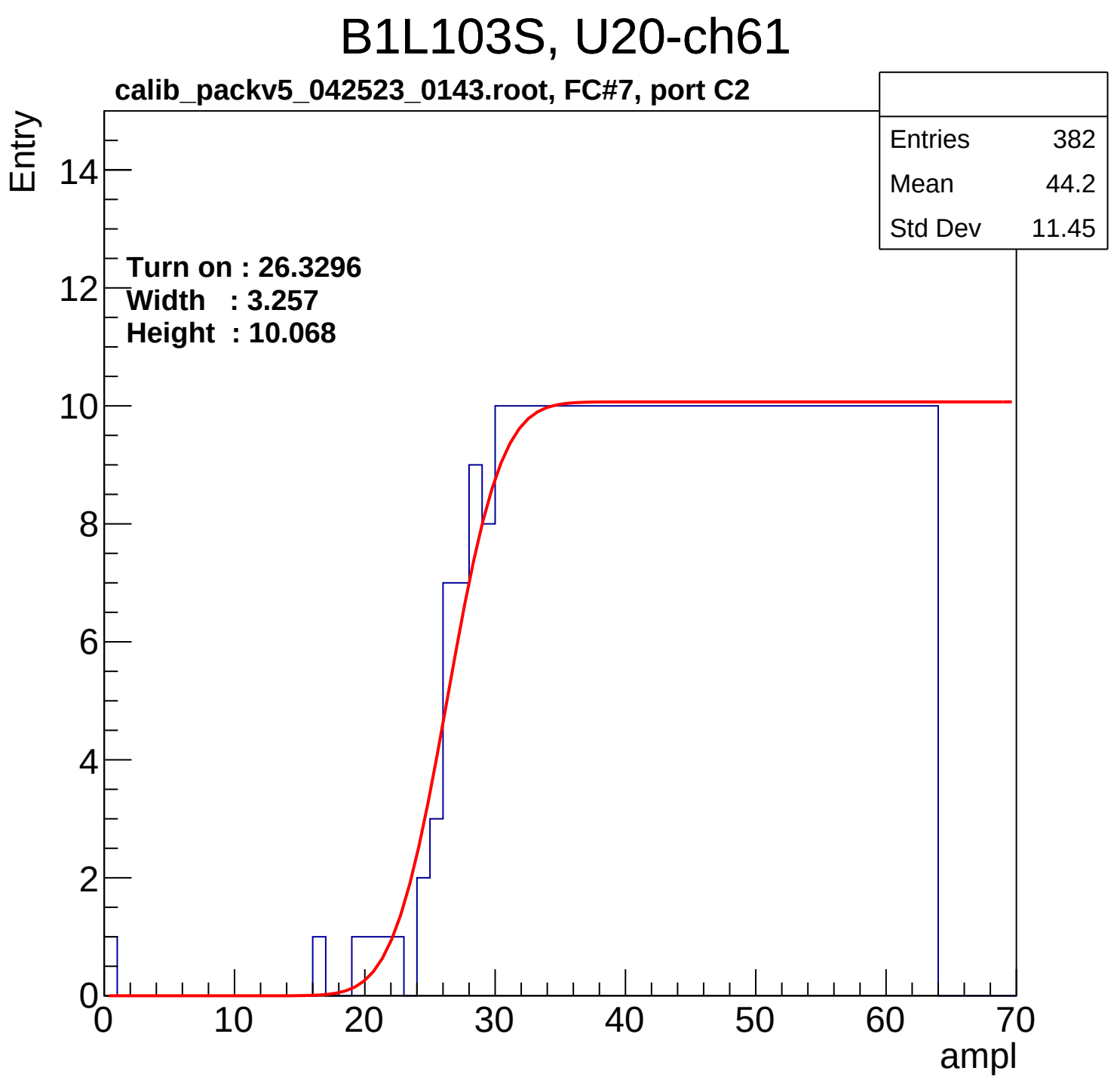
B1L103S, U20-ch61
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 44.2
Std Dev 11.45
Turn on : 26.3296
Width : 3.257
Height : 10.068
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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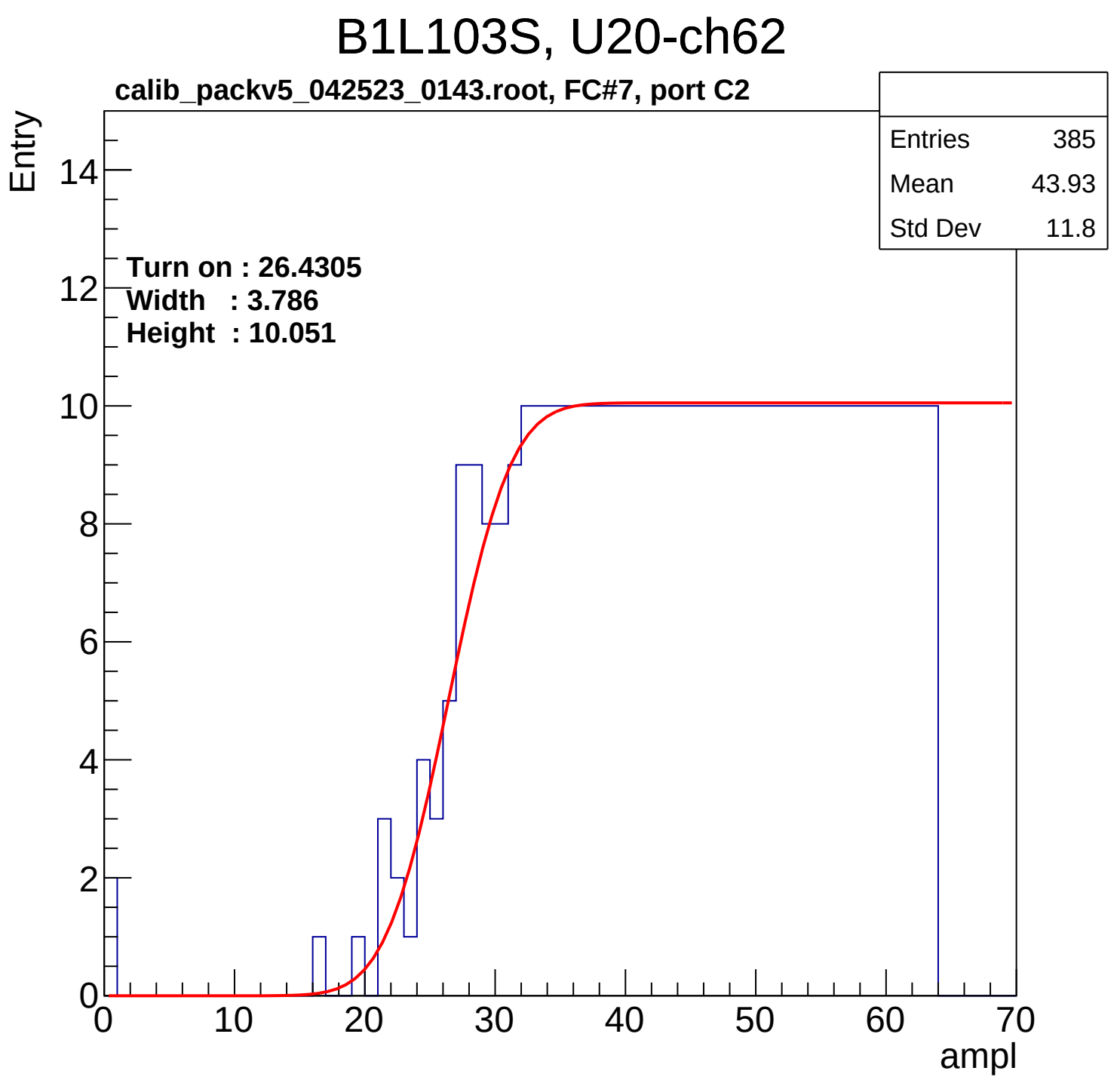
B1L103S, U20-ch62
calib_packv5_042523_0143.root, FC#7, port C2
Entries 385
Mean 43.93
Std Dev 11.8
Turn on : 26.4305
Width : 3.786
Height : 10.051
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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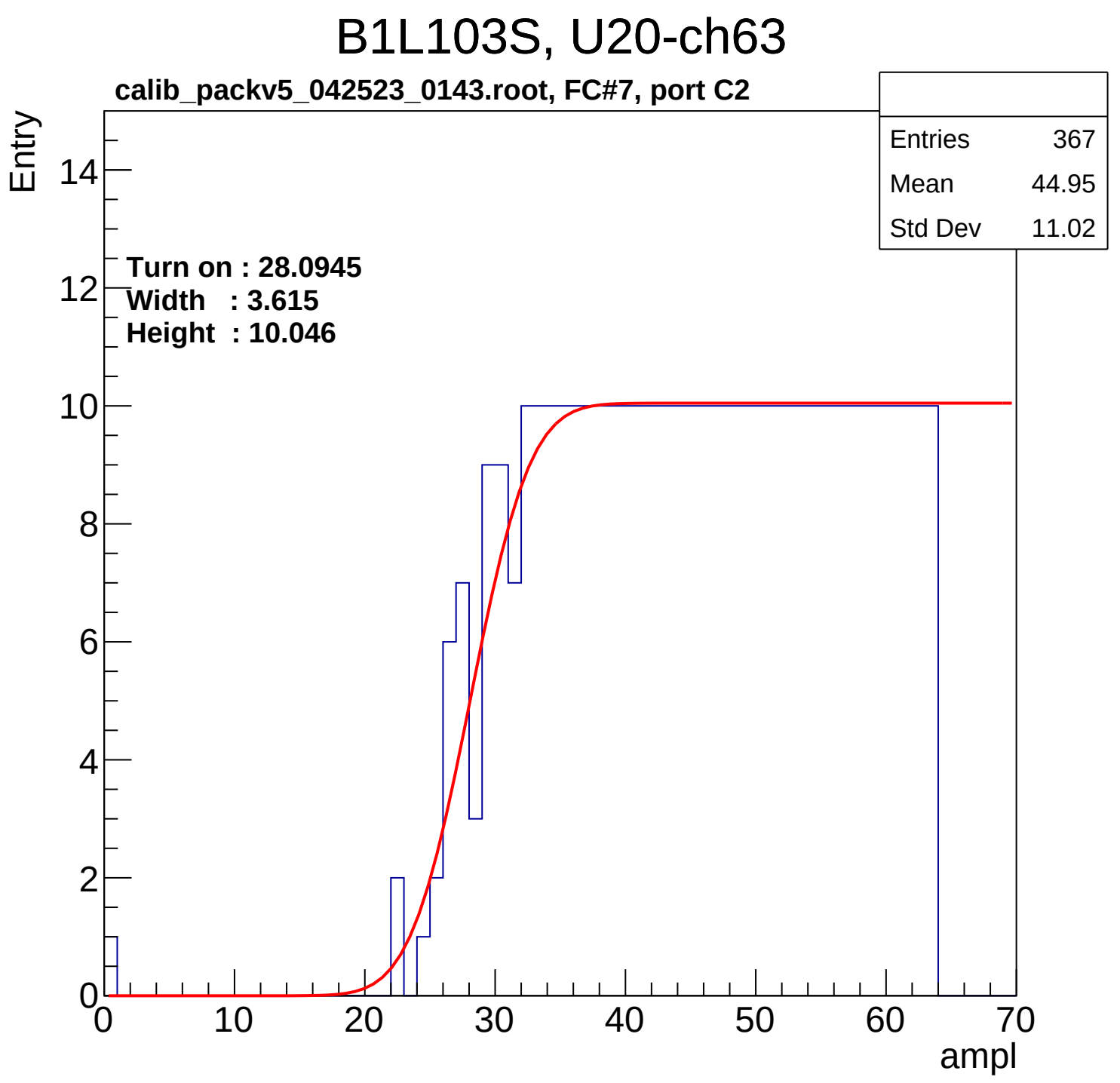
B1L103S, U20-ch63
calib_packv5_042523_0143.root, FC#7, port C2
Entries 367
Mean 44.95
Std Dev 11.02
Turn on : 28.0945
Width : 3.615
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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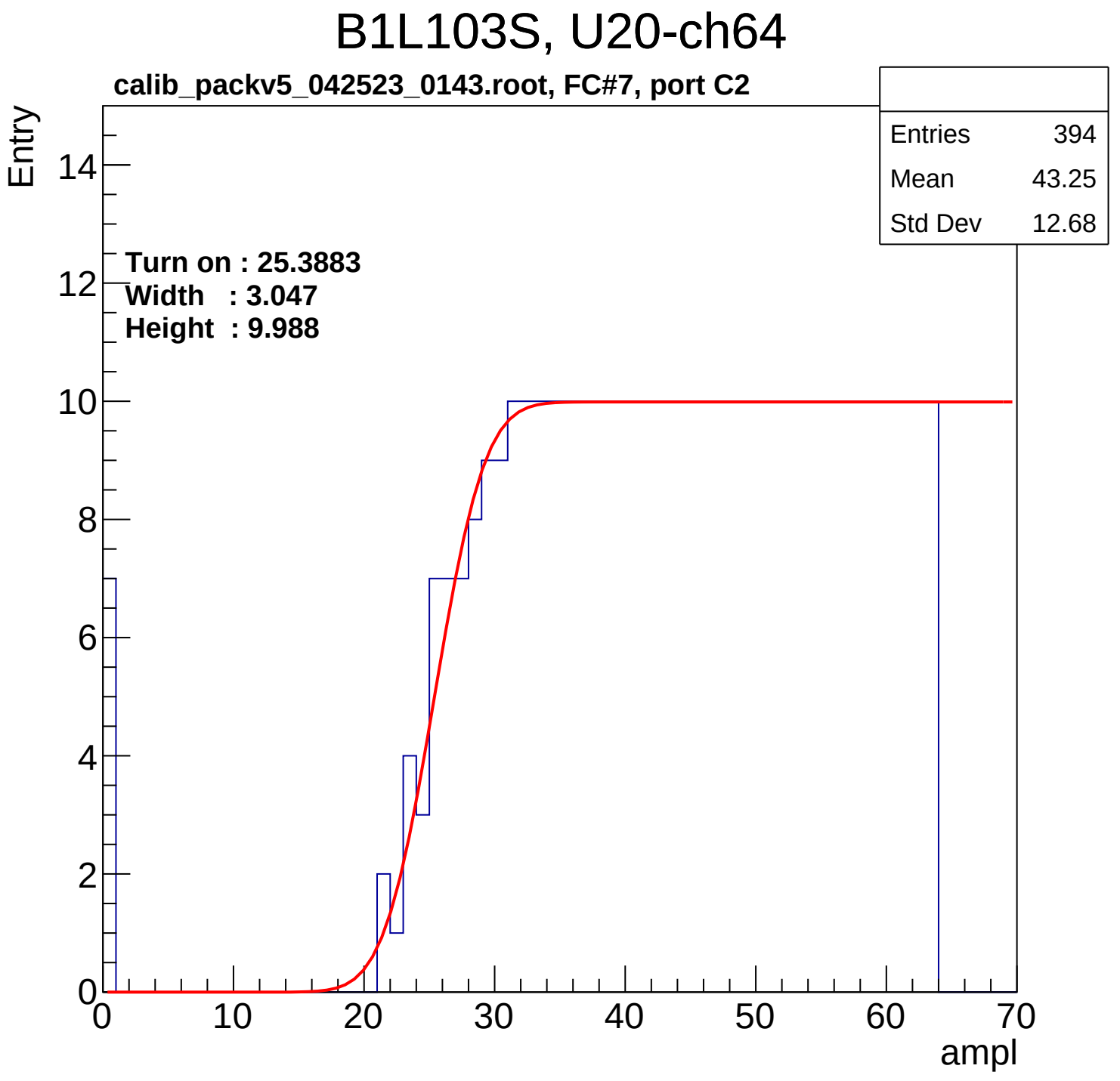
B1L103S, U20-ch64
calib_packv5_042523_0143.root, FC#7, port C2
Entries 394
Mean 43.25
Std Dev 12.68
Turn on : 25.3883
Width : 3.047
Height : 9.988
Entry
ampl
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4
6
8
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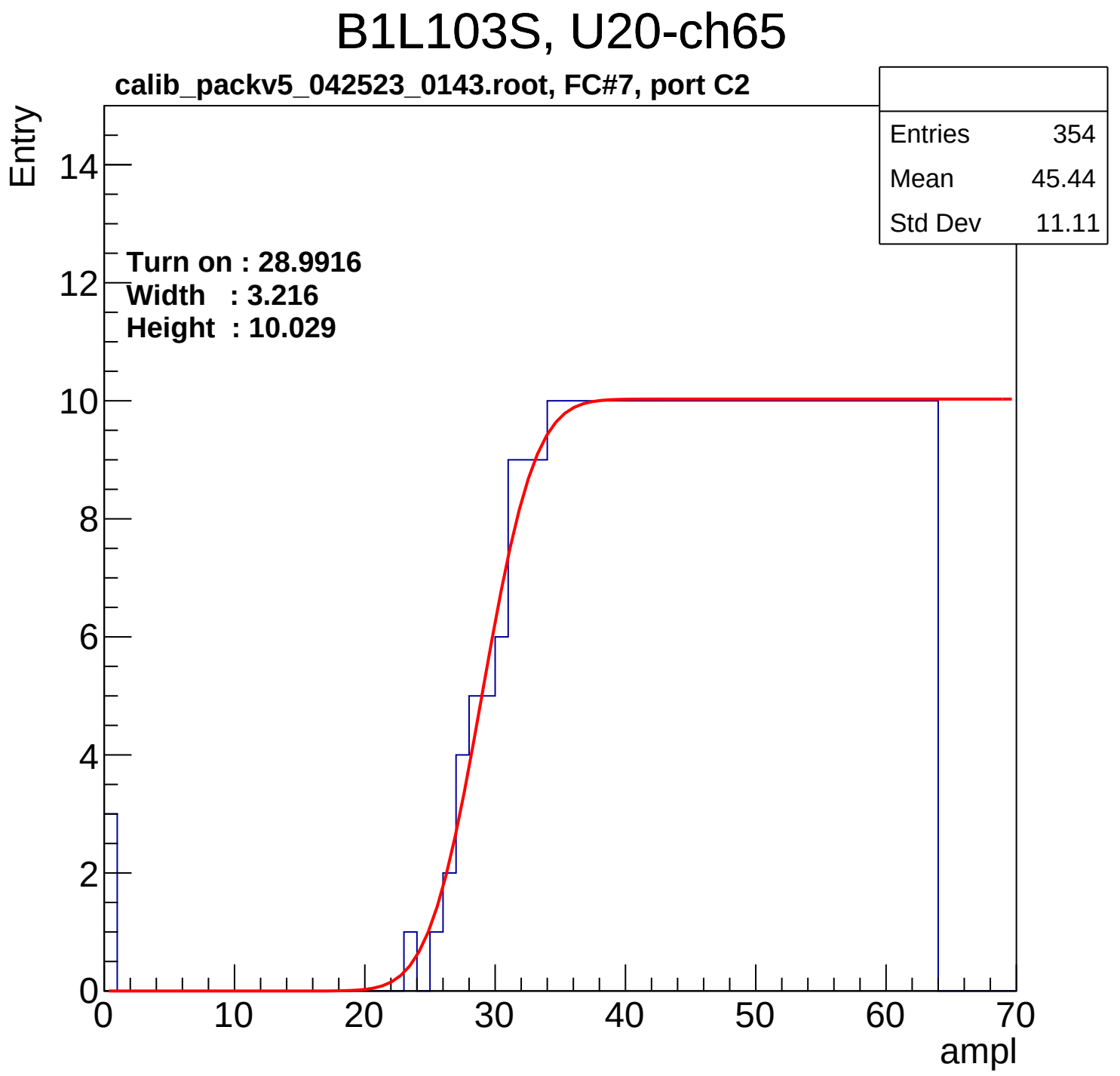
B1L103S, U20-ch65
calib_packv5_042523_0143.root, FC#7, port C2
Entries 354
Mean 45.44
Std Dev 11.11
Turn on : 28.9916
Width : 3.216
Height : 10.029
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
50
60
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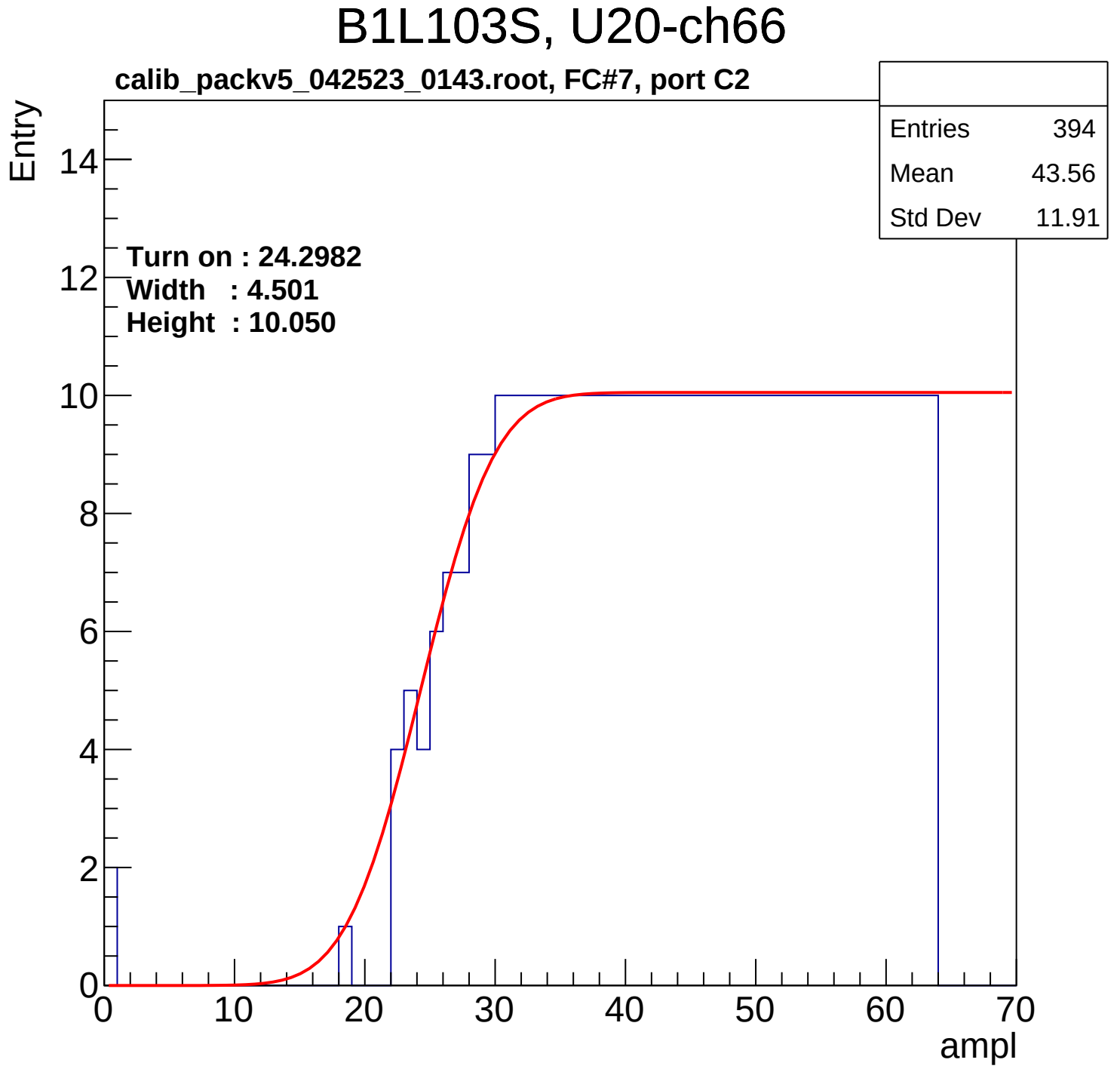
B1L103S, U20-ch66
calib_packv5_042523_0143.root, FC#7, port C2
Entries 394
Mean 43.56
Std Dev 11.91
Turn on : 24.2982
Width : 4.501
Height : 10.050
Entry
ampl
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2
4
6
8
10
12
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0
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60
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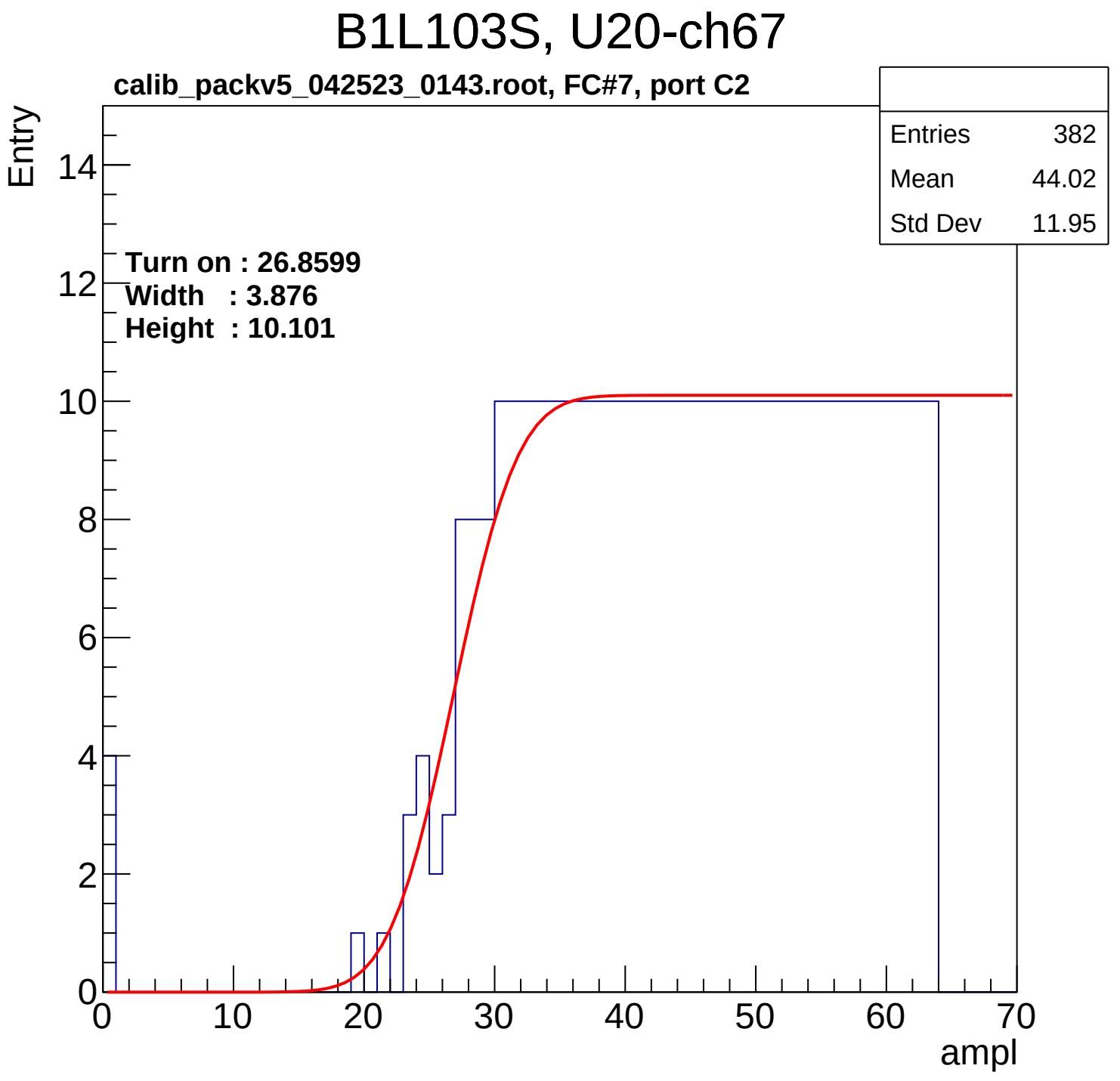
B1L103S, U20-ch67
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 44.02
Std Dev 11.95
Turn on : 26.8599
Width : 3.876
Height : 10.101
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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60
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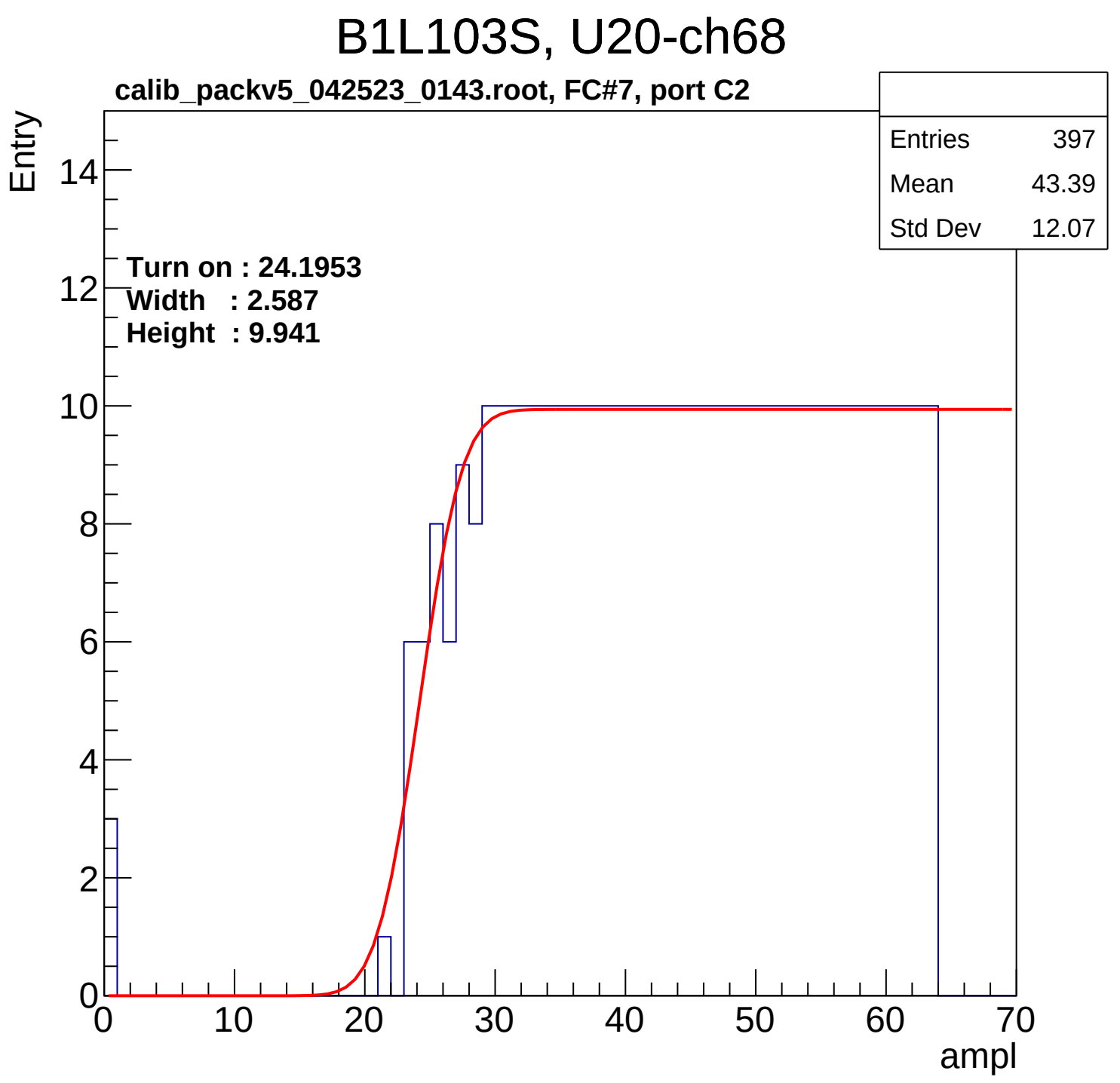
B1L103S, U20-ch68
calib_packv5_042523_0143.root, FC#7, port C2
Entries 397
Mean 43.39
Std Dev 12.07
Turn on : 24.1953
Width : 2.587
Height : 9.941
Entry
ampl
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4
6
8
10
12
14
0
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60
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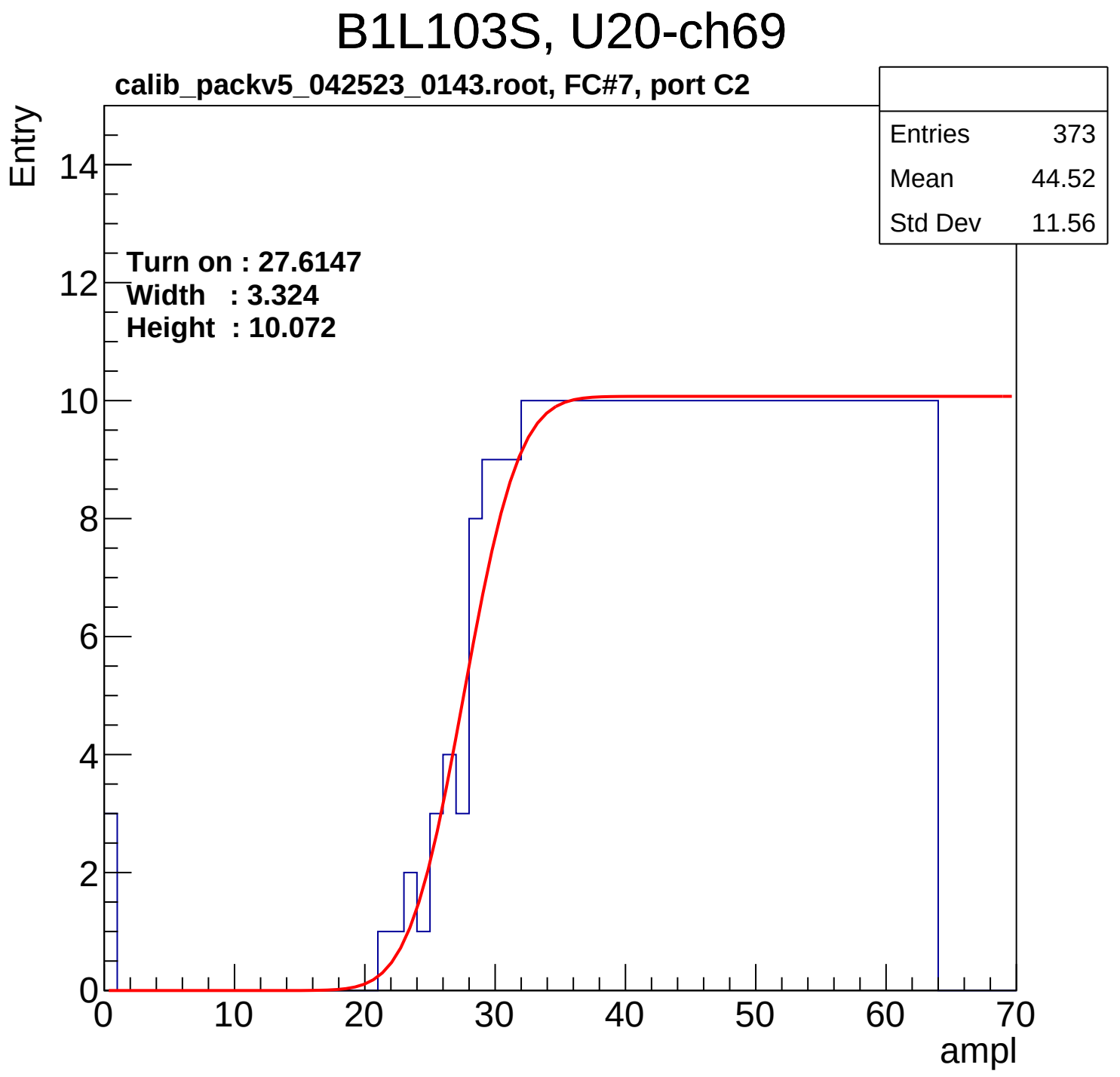
B1L103S, U20-ch69
calib_packv5_042523_0143.root, FC#7, port C2
Entries 373
Mean 44.52
Std Dev 11.56
Turn on : 27.6147
Width : 3.324
Height : 10.072
Entry
ampl
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6
8
10
12
14
0
10
20
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40
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60
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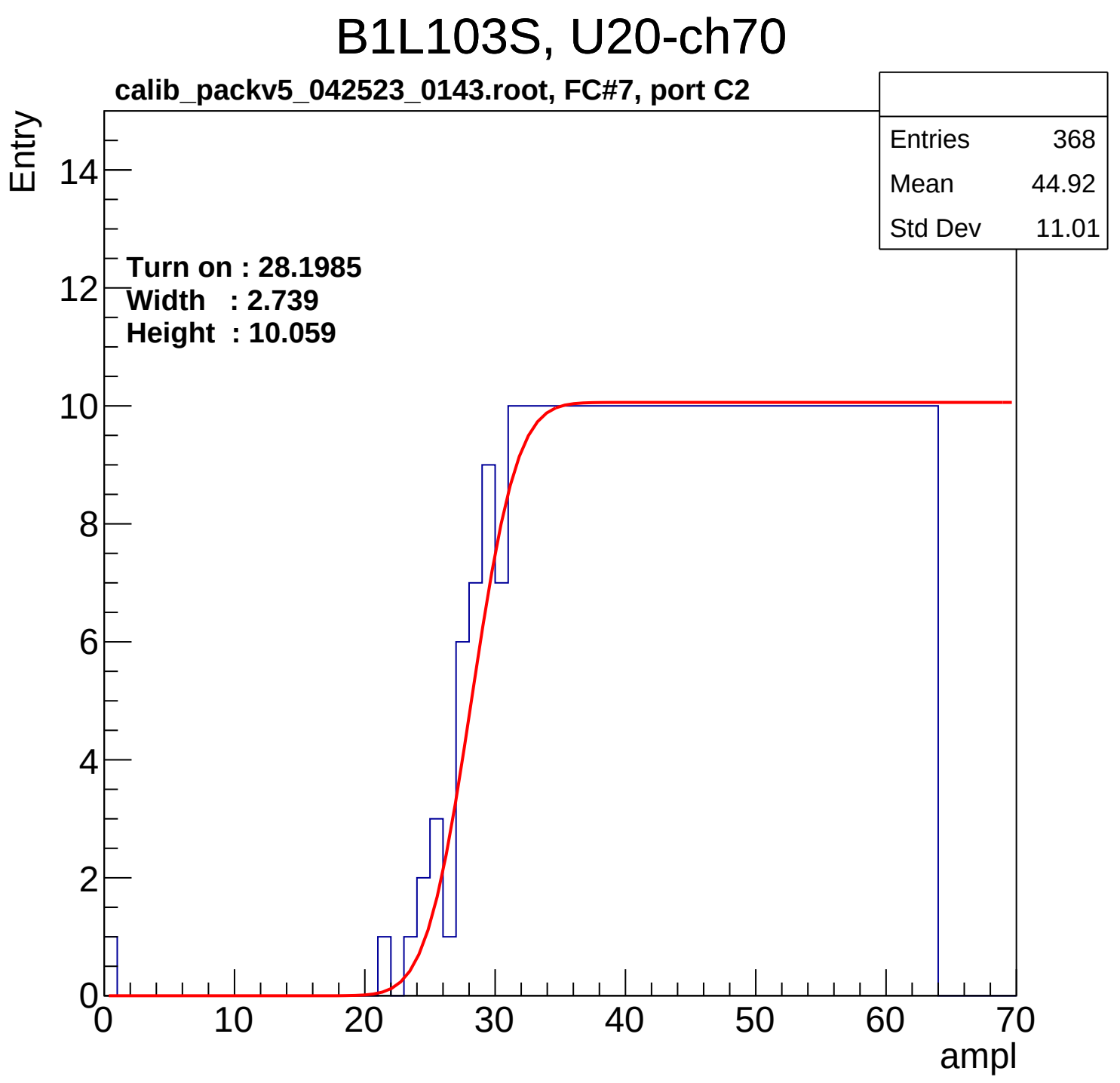
B1L103S, U20-ch70
calib_packv5_042523_0143.root, FC#7, port C2
Entries 368
Mean 44.92
Std Dev 11.01
Turn on : 28.1985
Width : 2.739
Height : 10.059
Entry
ampl
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2
4
6
8
10
12
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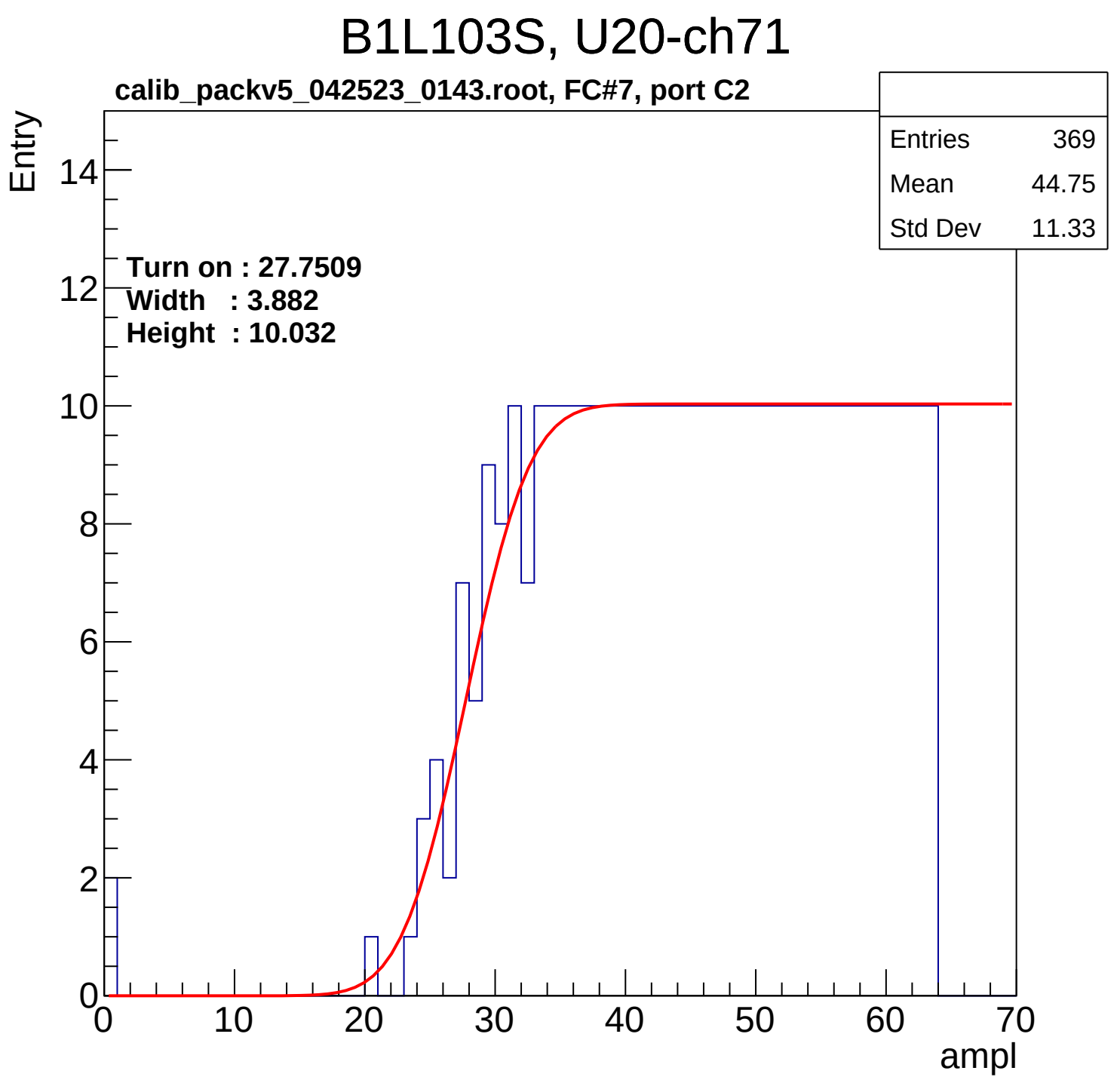
B1L103S, U20-ch71
calib_packv5_042523_0143.root, FC#7, port C2
Entries 369
Mean 44.75
Std Dev 11.33
Turn on : 27.7509
Width : 3.882
Height : 10.032
Entry
ampl
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4
6
8
10
12
14
0
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20
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60
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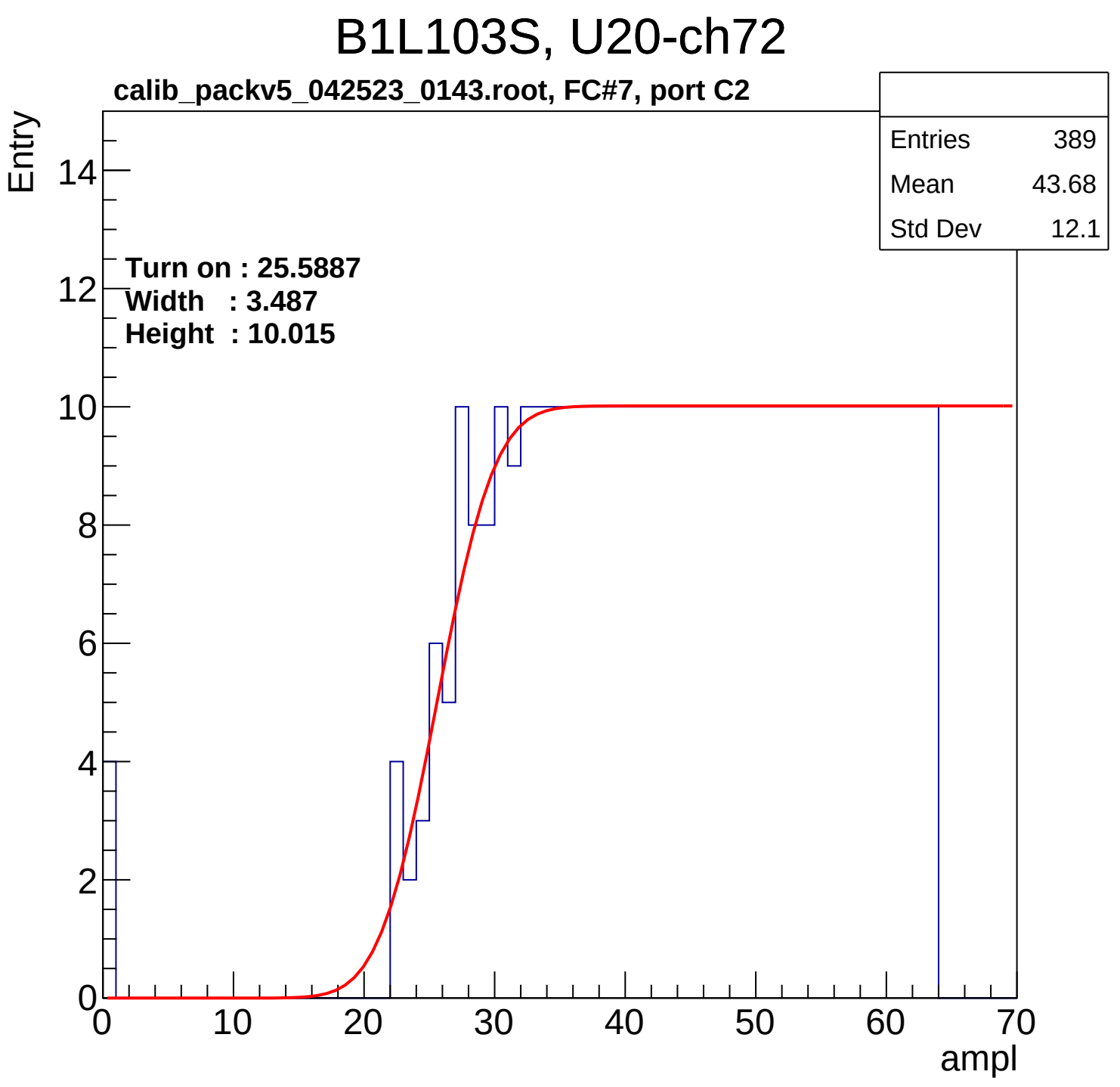
B1L103S, U20-ch72
calib_packv5_042523_0143.root, FC#7, port C2
Entries 389
Mean 43.68
Std Dev 12.1
Turn on : 25.5887
Width : 3.487
Height : 10.015
Entry
ampl
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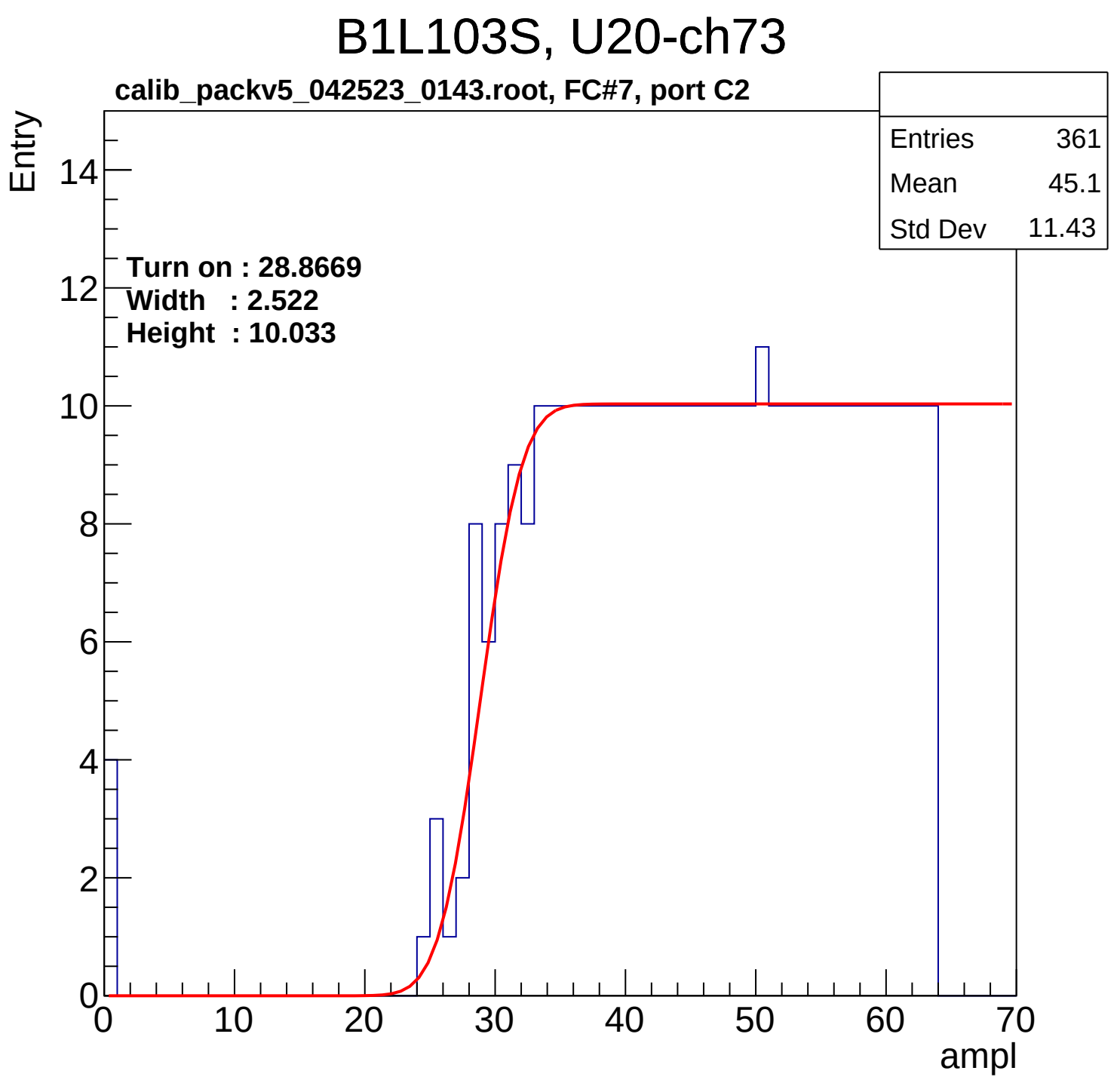
B1L103S, U20-ch73
calib_packv5_042523_0143.root, FC#7, port C2
Entries 361
Mean 45.1
Std Dev 11.43
Turn on : 28.8669
Width : 2.522
Height : 10.033
Entry
ampl
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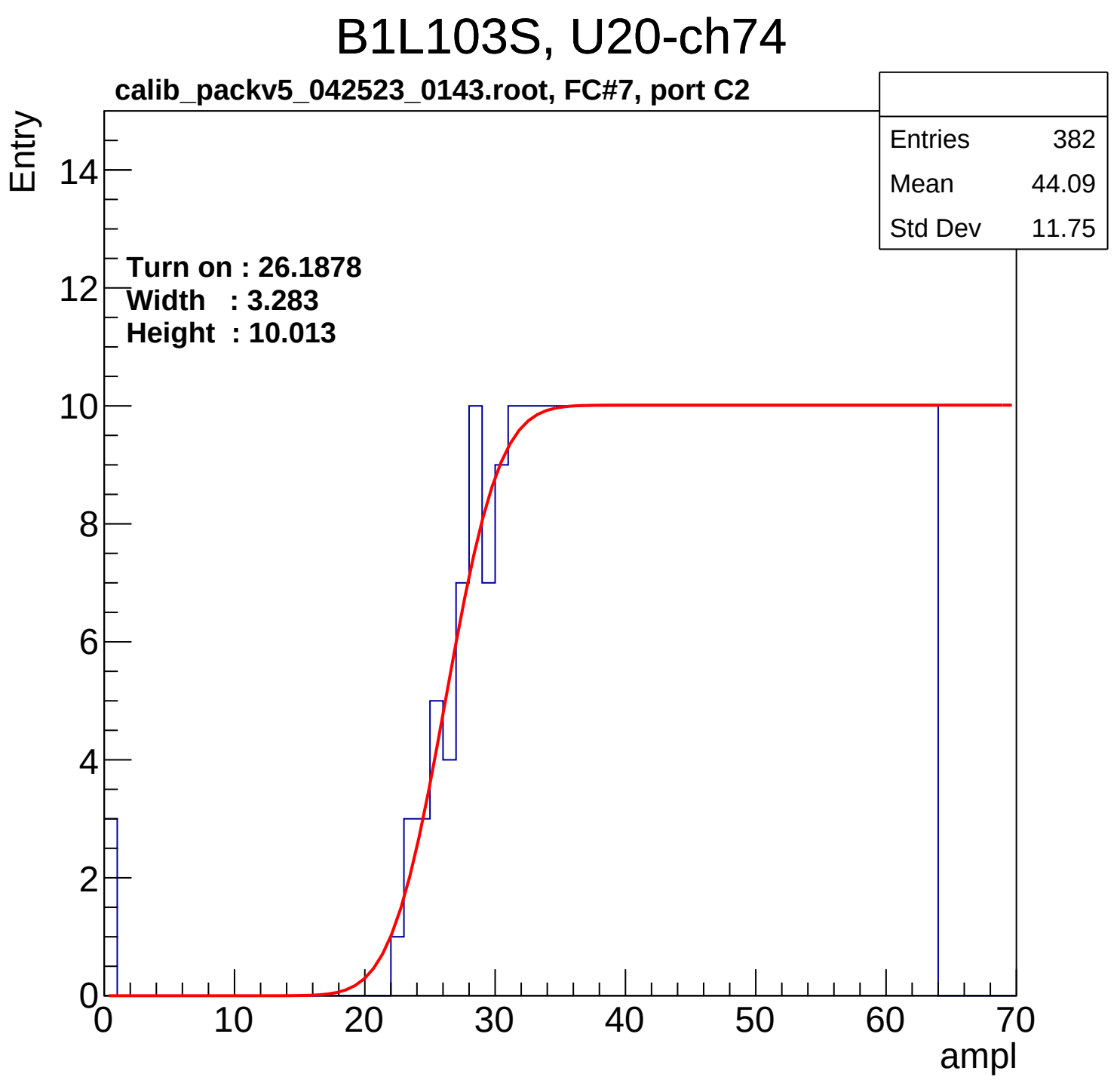
B1L103S, U20-ch74
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 44.09
Std Dev 11.75
Turn on : 26.1878
Width : 3.283
Height : 10.013
Entry
ampl
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6
8
10
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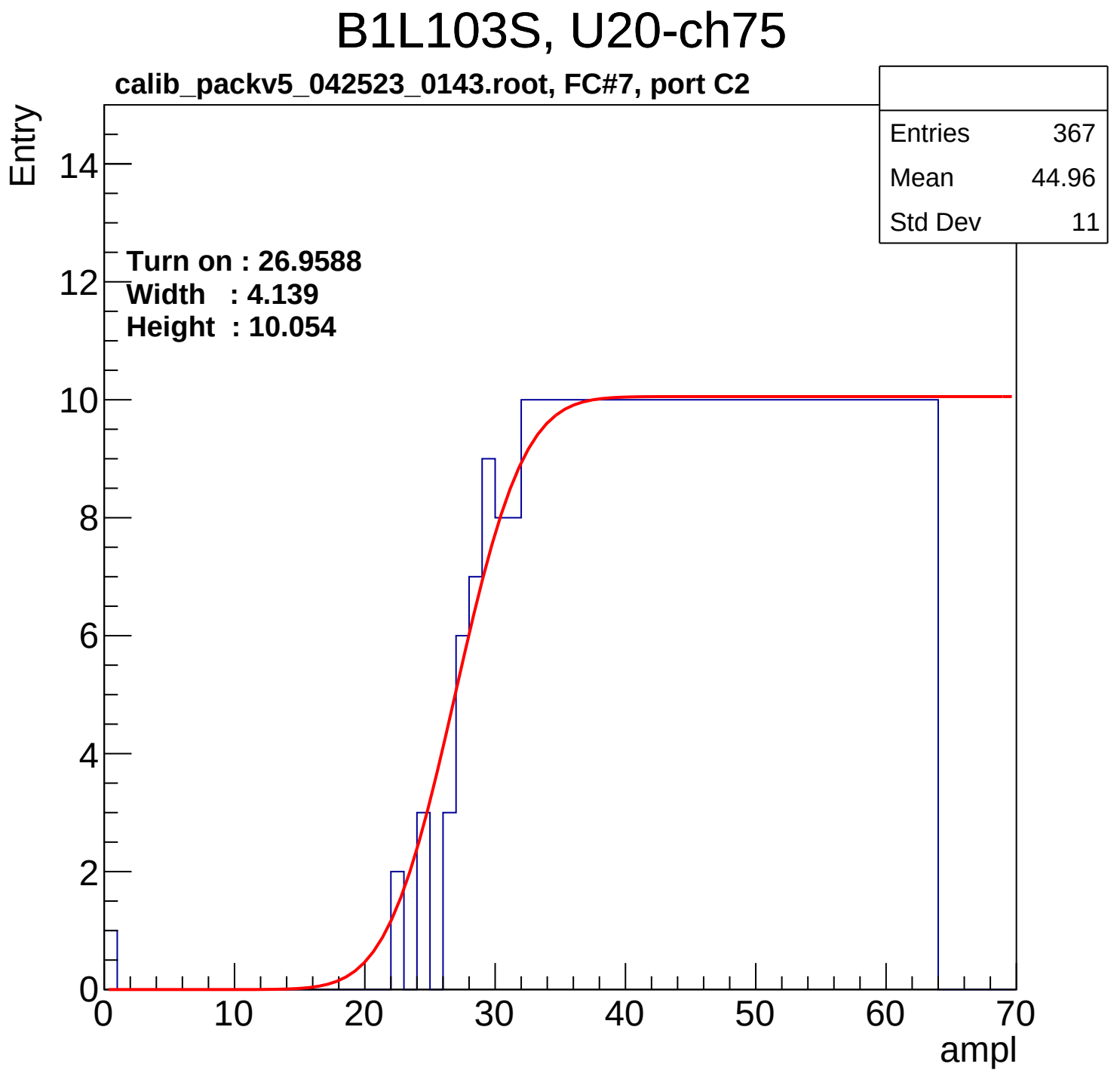
B1L103S, U20-ch75
calib_packv5_042523_0143.root, FC#7, port C2
Entries 367
Mean 44.96
Std Dev 11
Turn on : 26.9588
Width : 4.139
Height : 10.054
Entry
ampl
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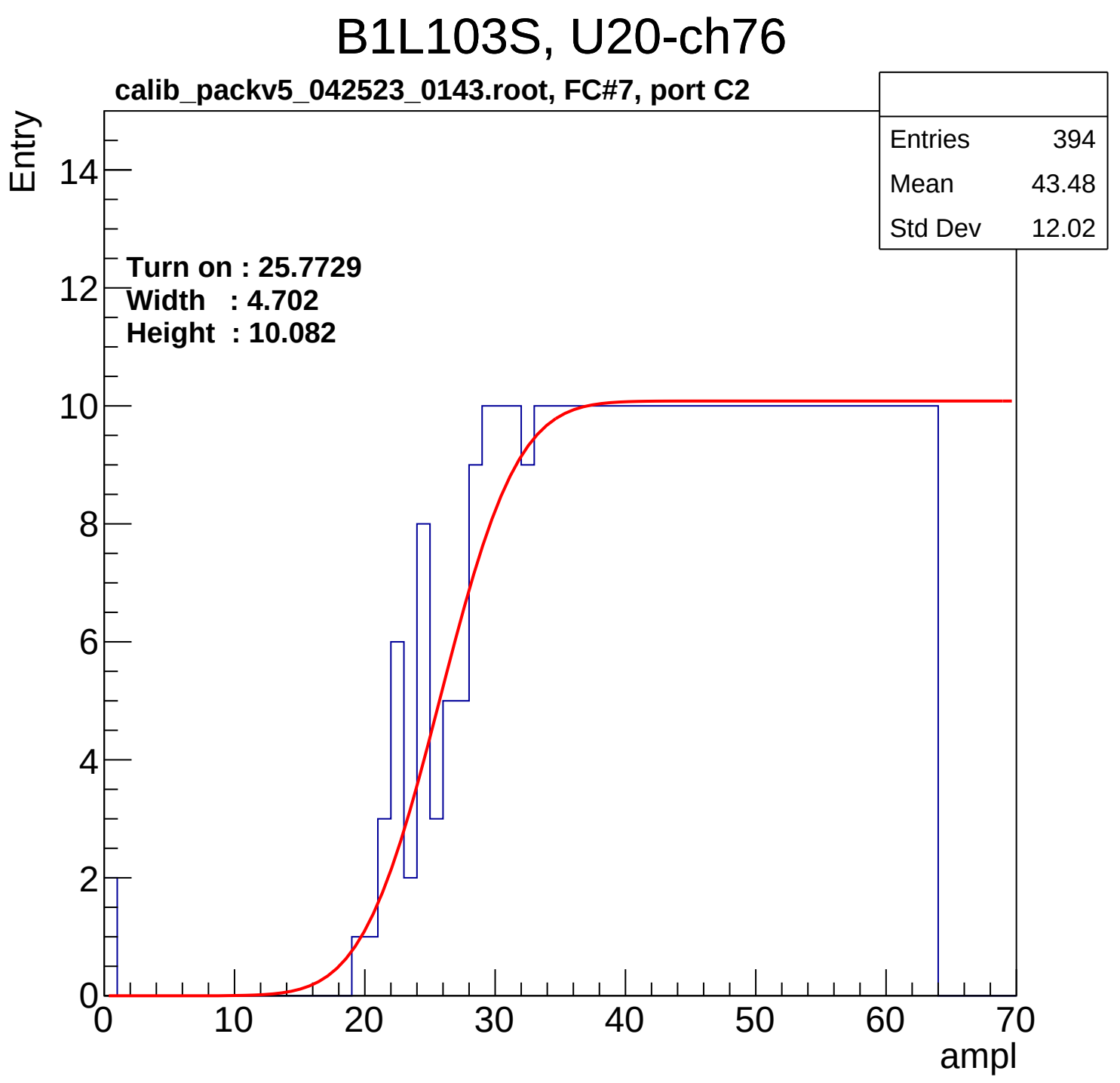
B1L103S, U20-ch76
calib_packv5_042523_0143.root, FC#7, port C2
Entries 394
Mean 43.48
Std Dev 12.02
Turn on : 25.7729
Width : 4.702
Height : 10.082
Entry
ampl
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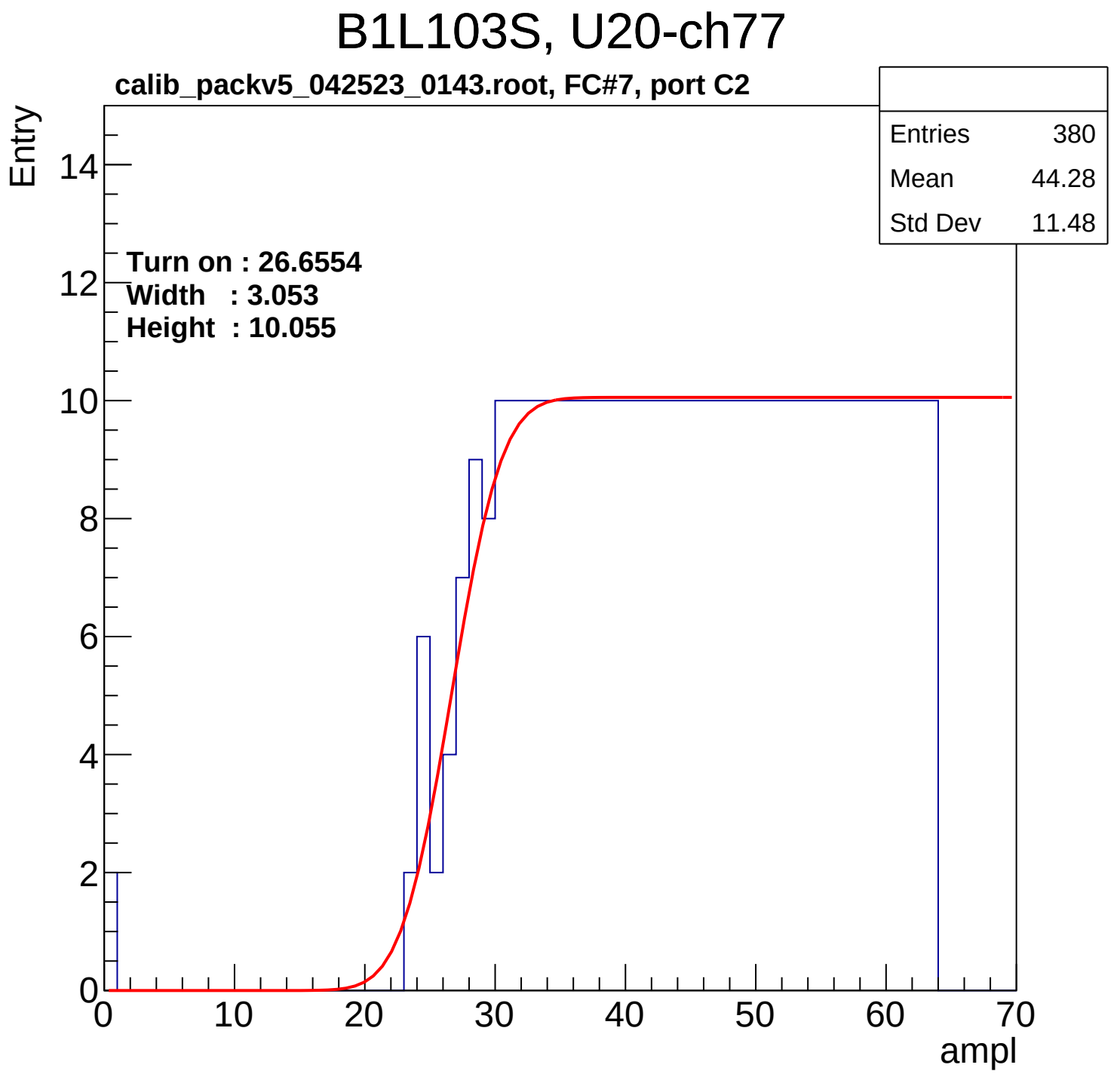
B1L103S, U20-ch77
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.28
Std Dev 11.48
Turn on : 26.6554
Width : 3.053
Height : 10.055
Entry
ampl
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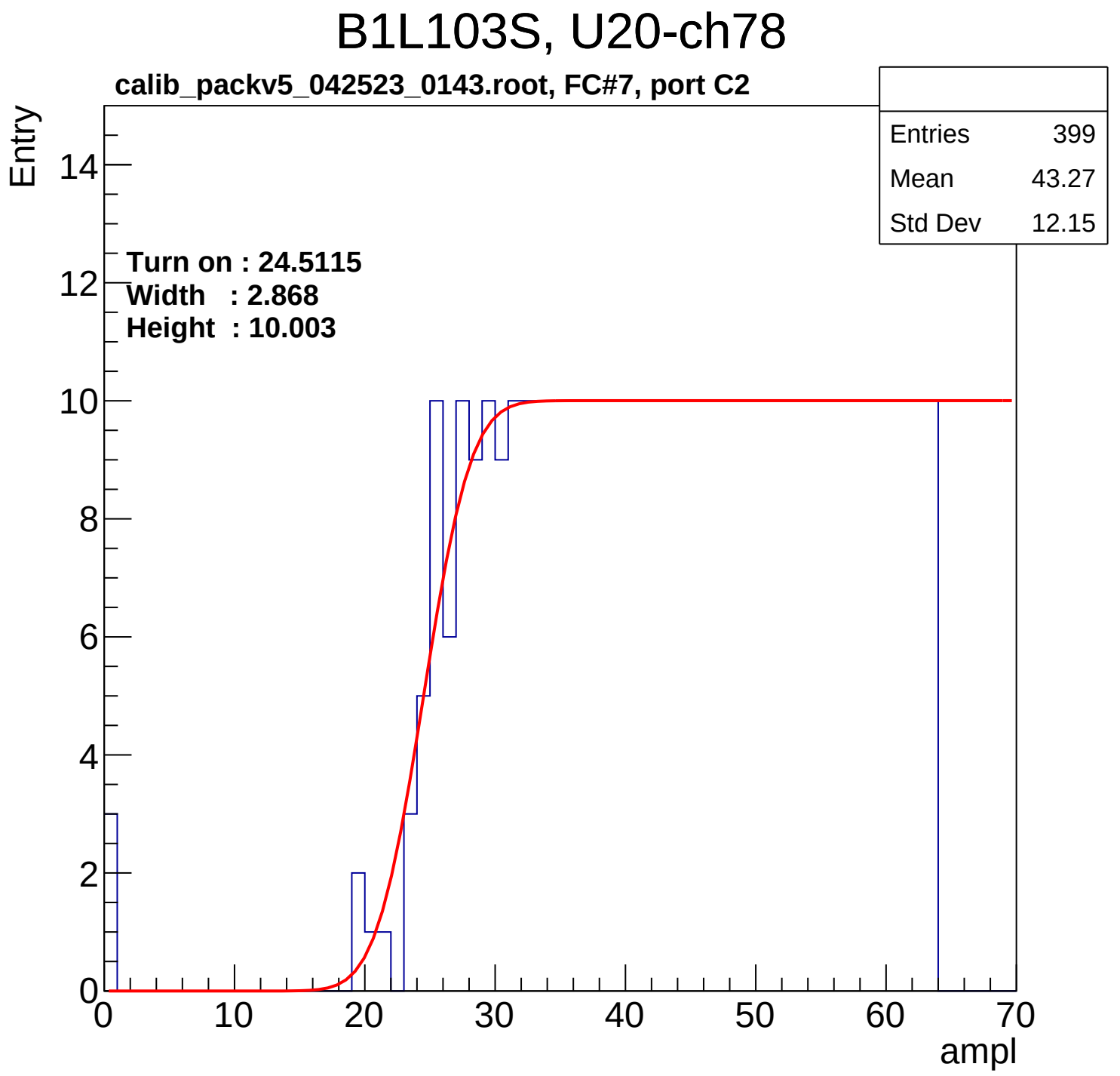
B1L103S, U20-ch78
calib_packv5_042523_0143.root, FC#7, port C2
Entries 399
Mean 43.27
Std Dev 12.15
Turn on : 24.5115
Width : 2.868
Height : 10.003
Entry
ampl
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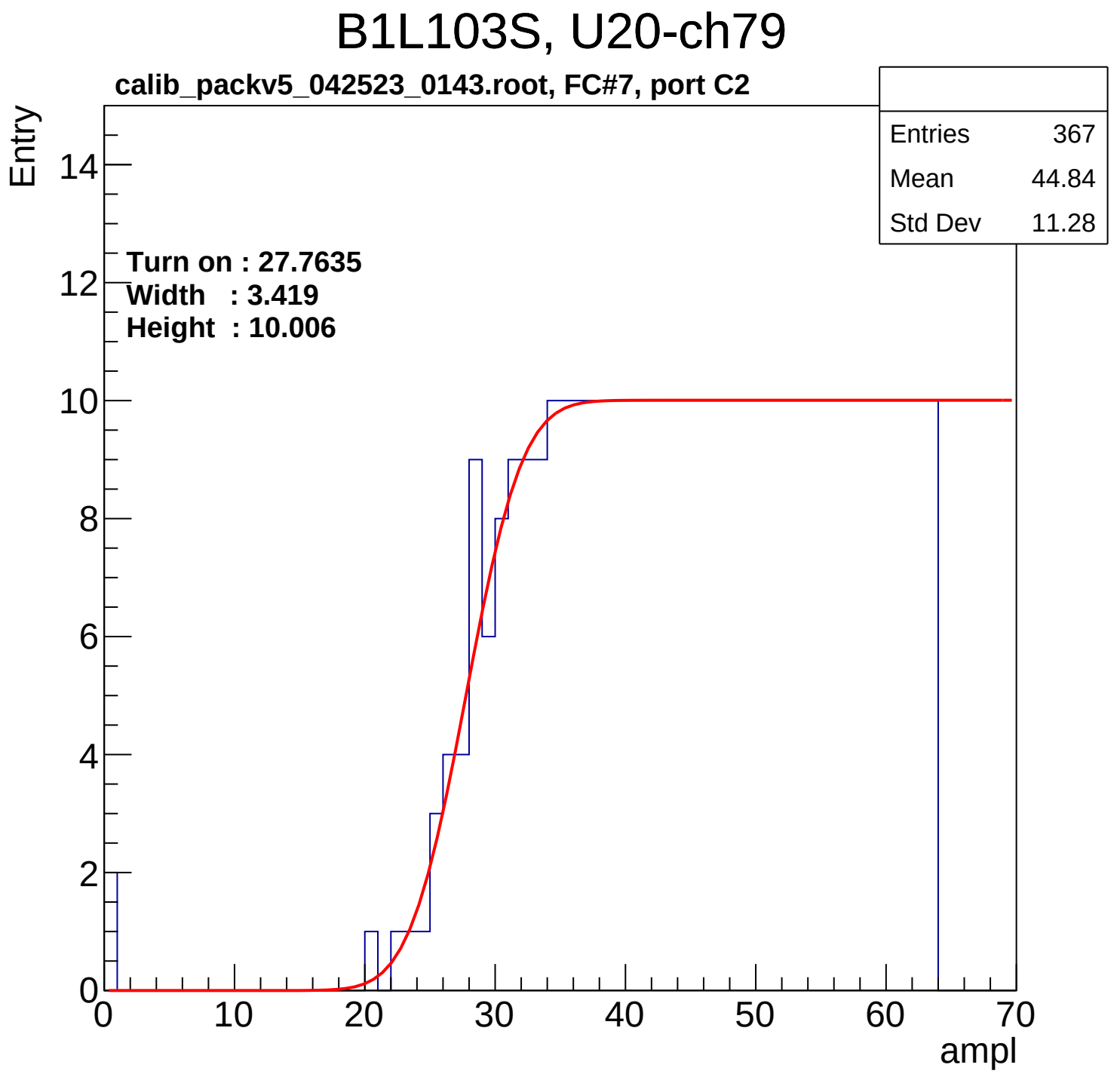
B1L103S, U20-ch79
calib_packv5_042523_0143.root, FC#7, port C2
Entries 367
Mean 44.84
Std Dev 11.28
Turn on : 27.7635
Width : 3.419
Height : 10.006
Entry
ampl
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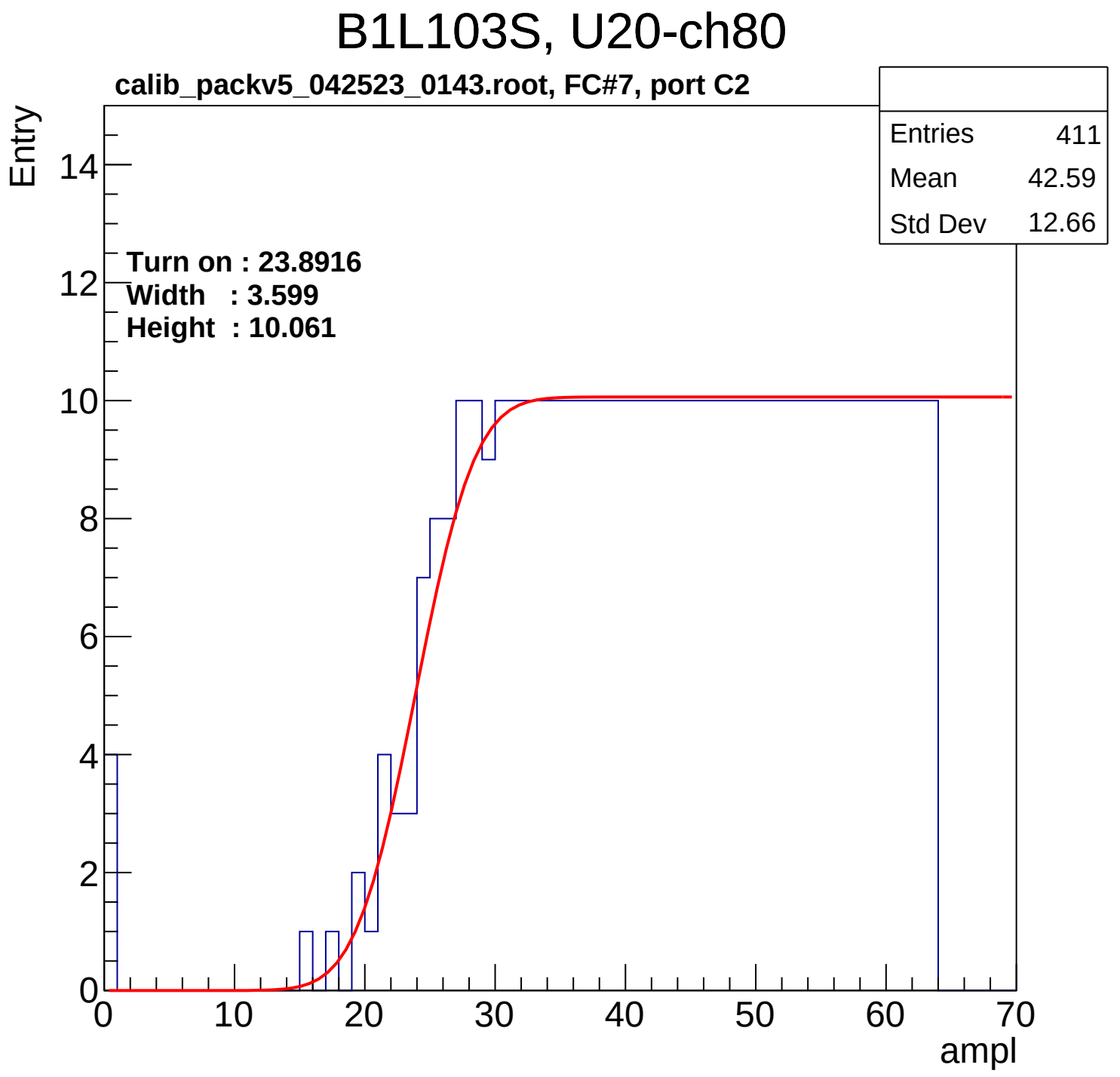
B1L103S, U20-ch80
calib_packv5_042523_0143.root, FC#7, port C2
Entries 411
Mean 42.59
Std Dev 12.66
Turn on : 23.8916
Width : 3.599
Height : 10.061
Entry
ampl
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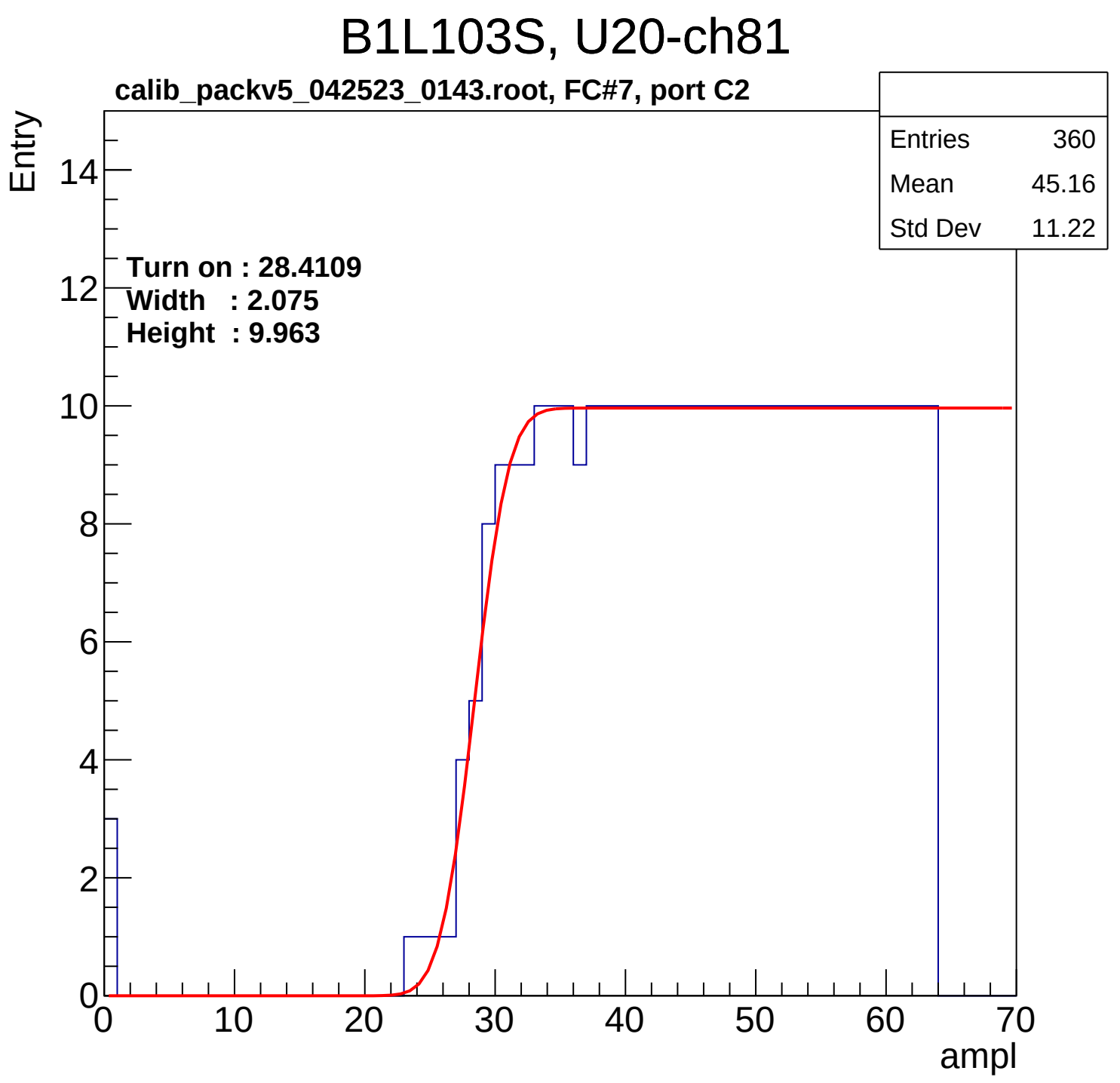
B1L103S, U20-ch81
calib_packv5_042523_0143.root, FC#7, port C2
Entries 360
Mean 45.16
Std Dev 11.22
Turn on : 28.4109
Width : 2.075
Height : 9.963
Entry
ampl
0
2
4
6
8
10
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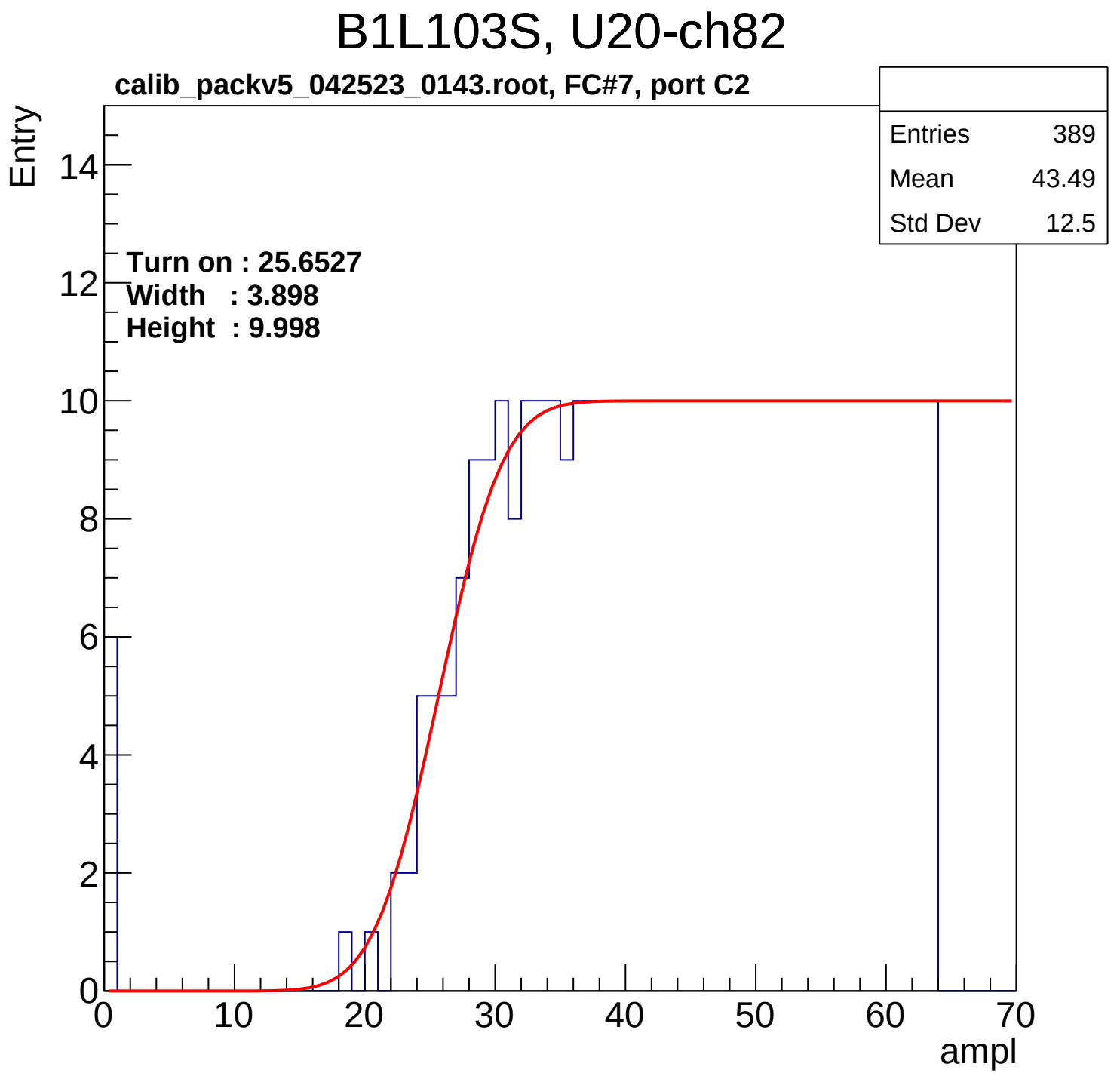
B1L103S, U20-ch82
calib_packv5_042523_0143.root, FC#7, port C2
Entries 389
Mean 43.49
Std Dev 12.5
Turn on : 25.6527
Width : 3.898
Height : 9.998
Entry
ampl
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2
4
6
8
10
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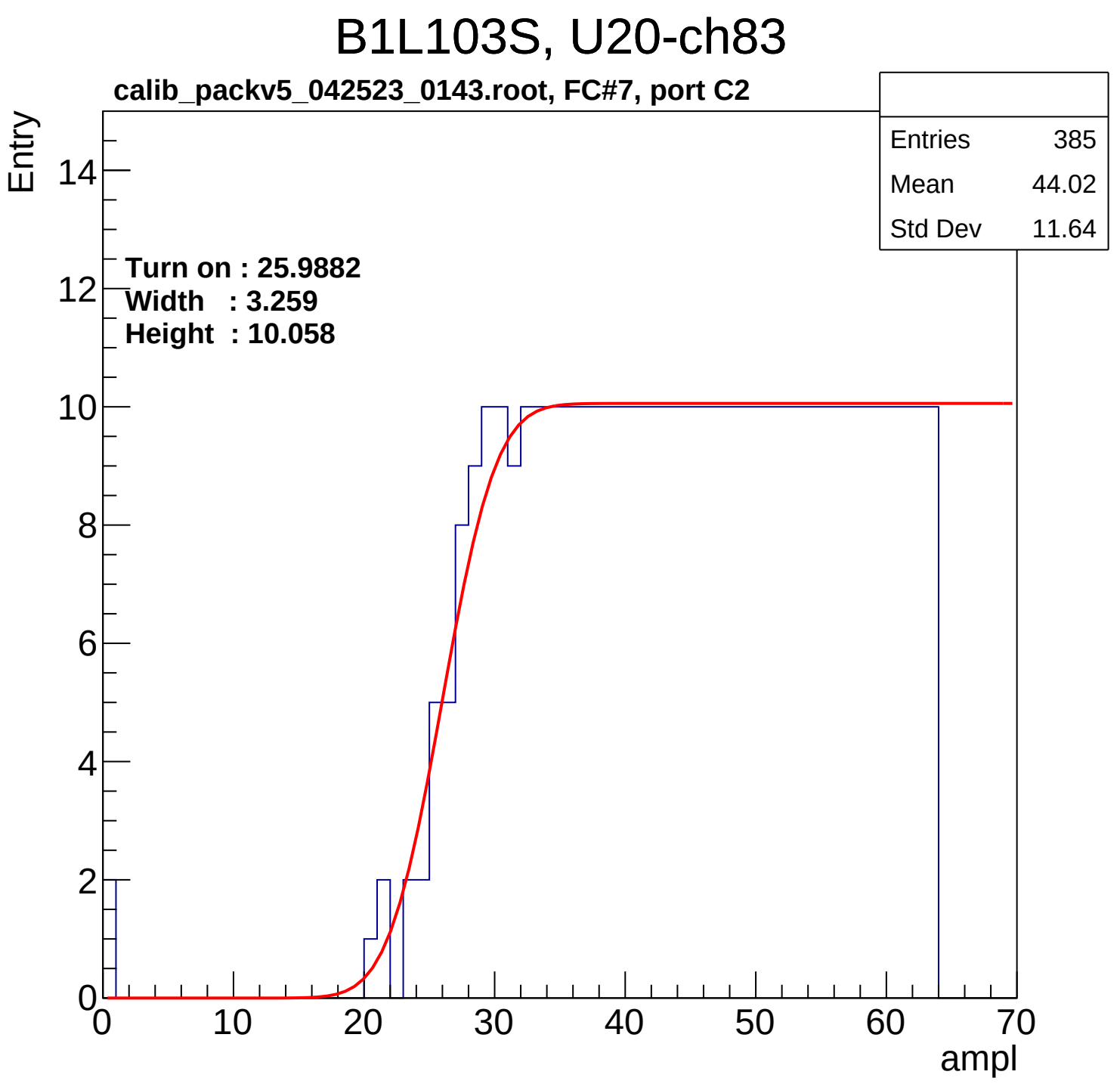
B1L103S, U20-ch83
calib_packv5_042523_0143.root, FC#7, port C2
Entries 385
Mean 44.02
Std Dev 11.64
Turn on : 25.9882
Width : 3.259
Height : 10.058
Entry
ampl
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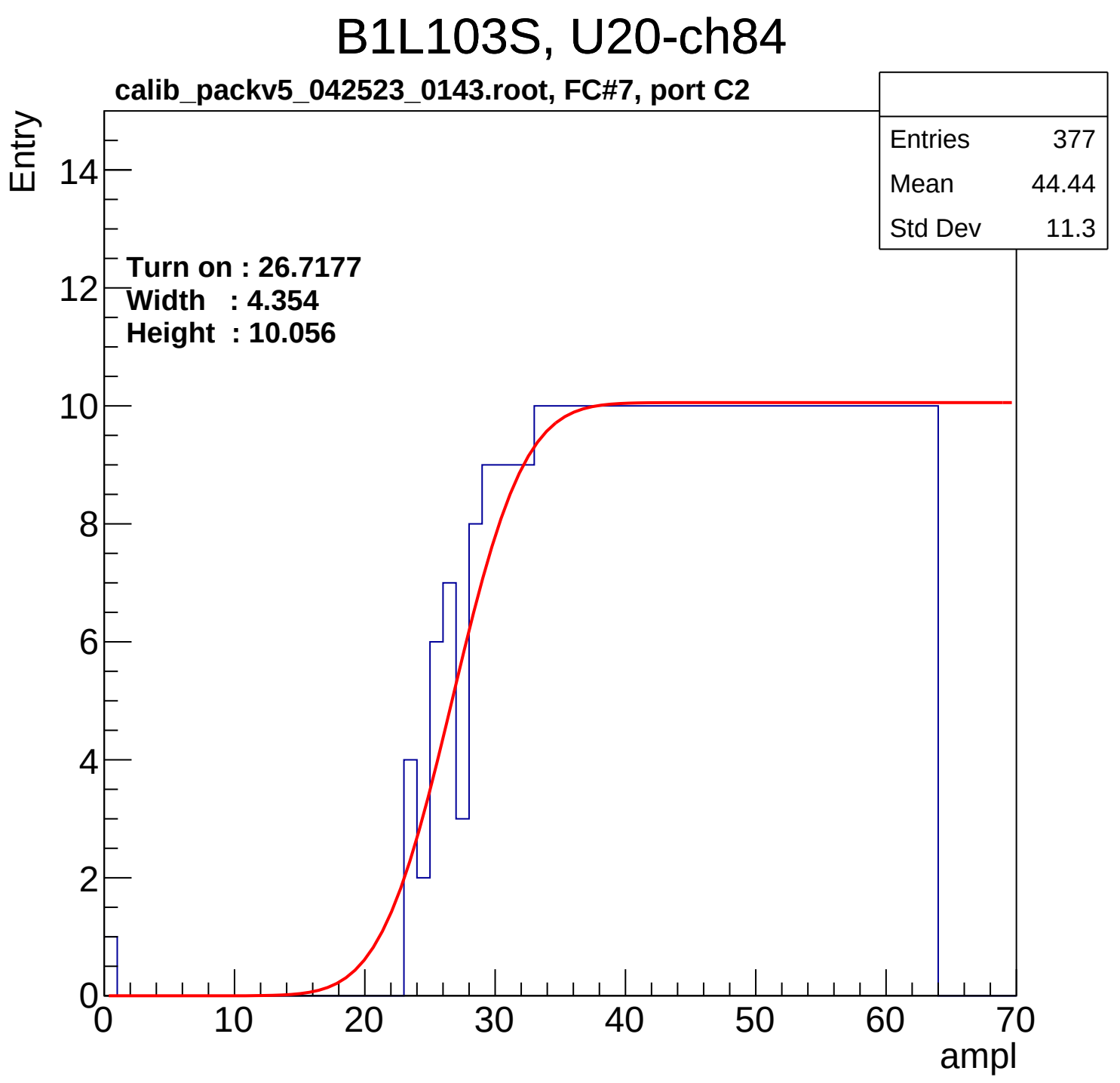
B1L103S, U20-ch84
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.44
Std Dev 11.3
Turn on : 26.7177
Width : 4.354
Height : 10.056
Entry
ampl
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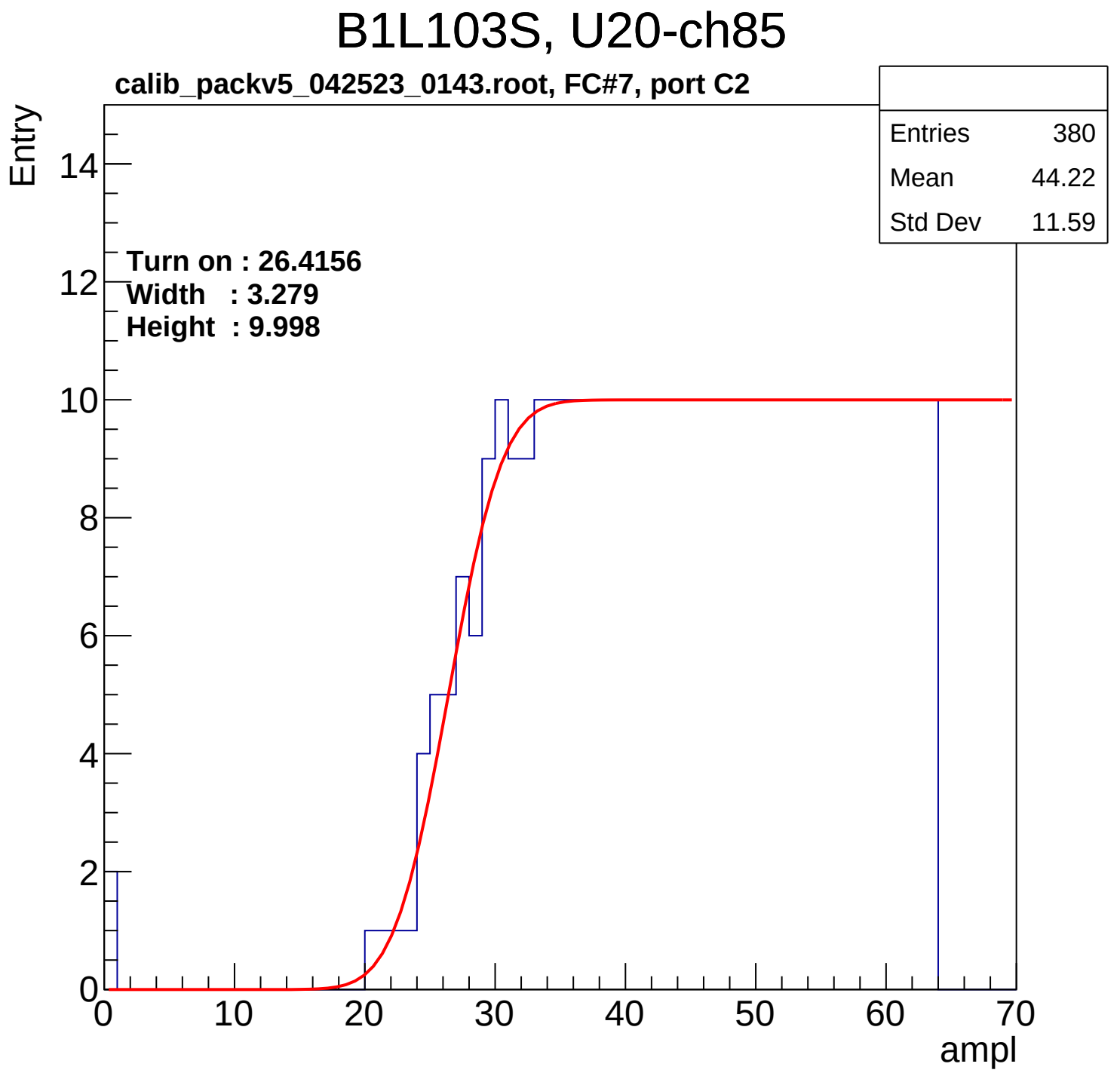
B1L103S, U20-ch85
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.22
Std Dev 11.59
Turn on : 26.4156
Width : 3.279
Height : 9.998
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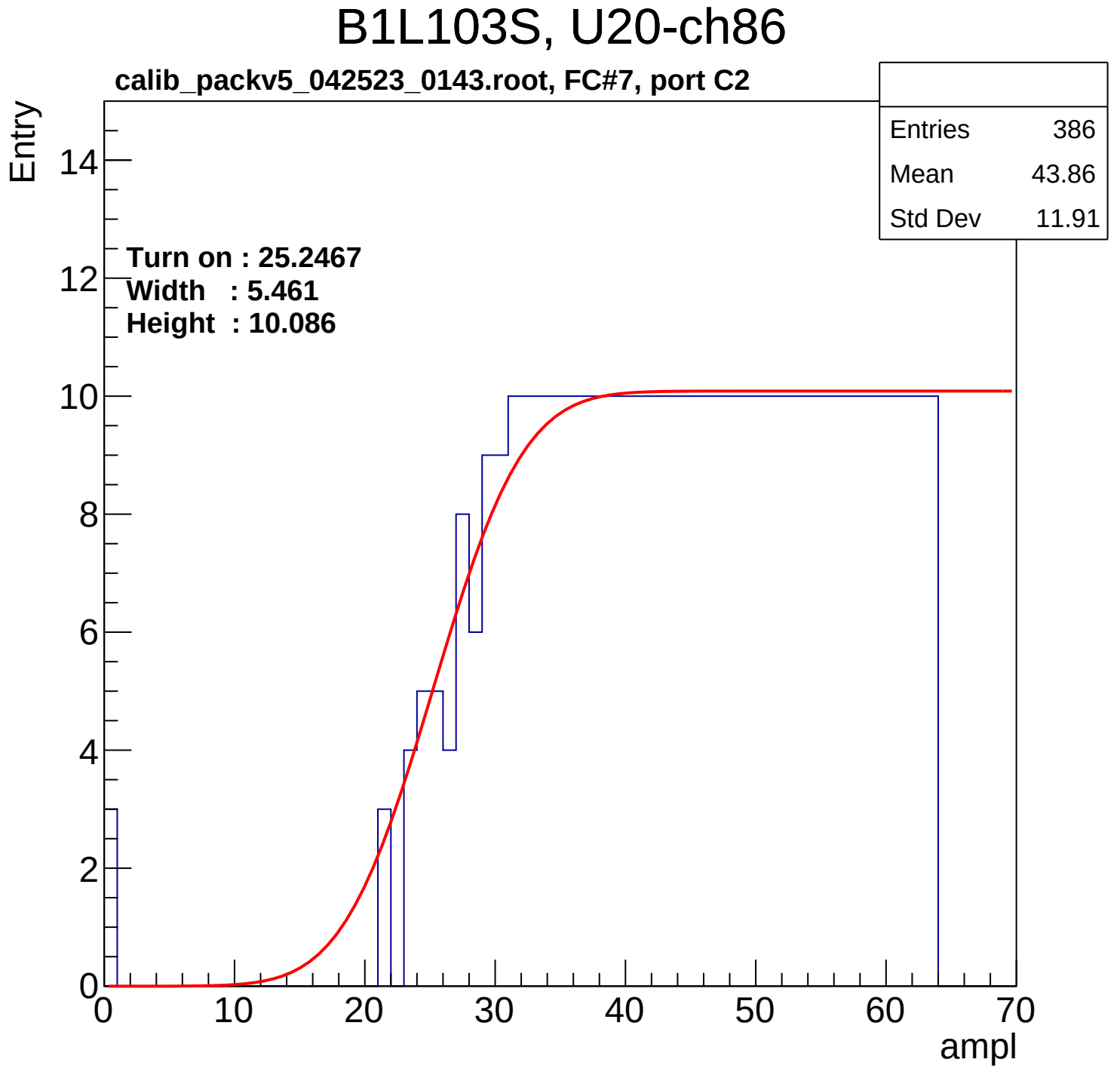
B1L103S, U20-ch86
calib_packv5_042523_0143.root, FC#7, port C2
Entries 386
Mean 43.86
Std Dev 11.91
Turn on : 25.2467
Width : 5.461
Height : 10.086
Entry
ampl
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4
6
8
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12
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20
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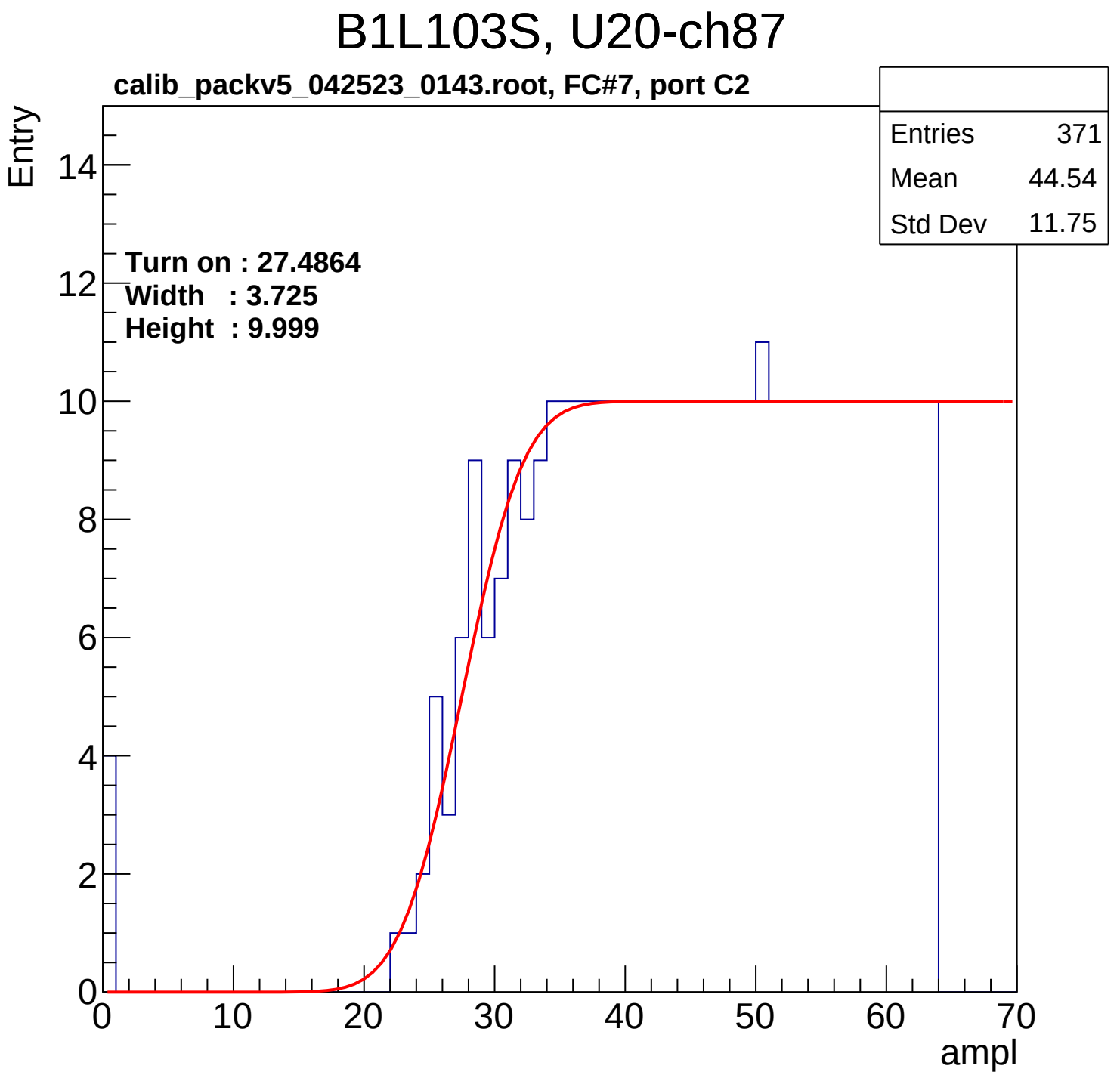
B1L103S, U20-ch87
calib_packv5_042523_0143.root, FC#7, port C2
Entries 371
Mean 44.54
Std Dev 11.75
Turn on : 27.4864
Width : 3.725
Height : 9.999
Entry
ampl
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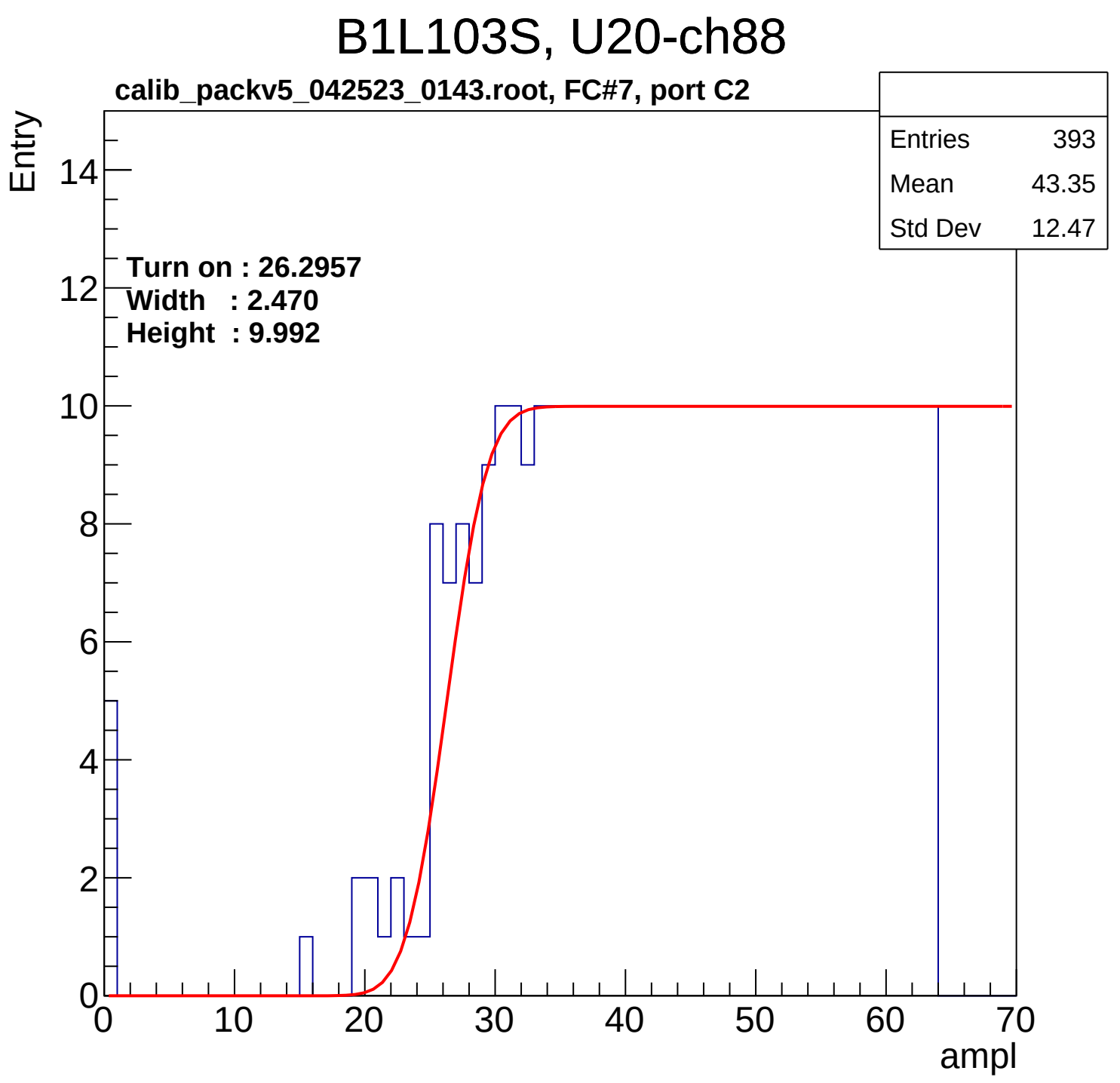
B1L103S, U20-ch88
calib_packv5_042523_0143.root, FC#7, port C2
Entries 393
Mean 43.35
Std Dev 12.47
Turn on : 26.2957
Width : 2.470
Height : 9.992
Entry
ampl
0
2
4
6
8
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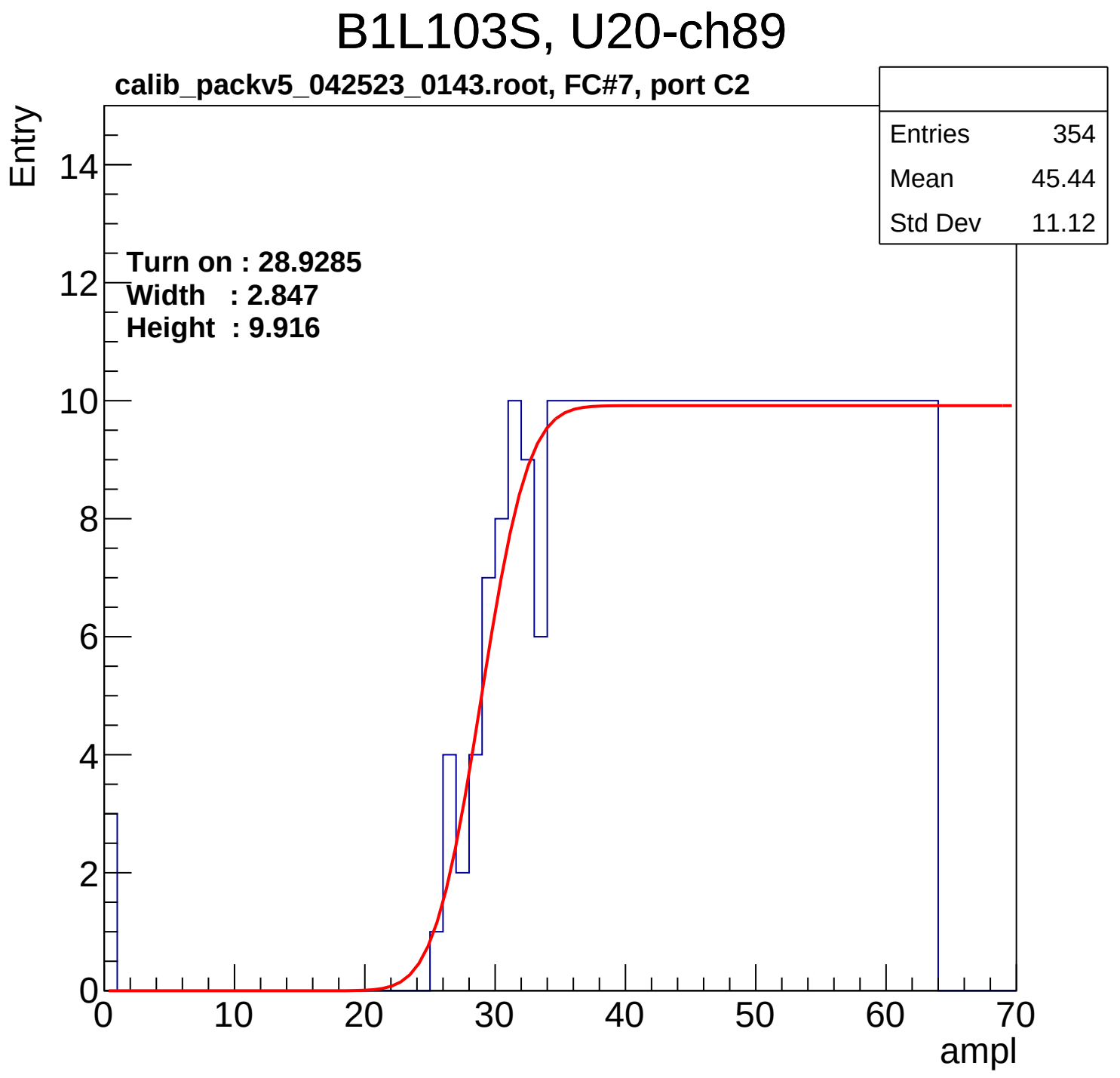
B1L103S, U20-ch89
calib_packv5_042523_0143.root, FC#7, port C2
Entries 354
Mean 45.44
Std Dev 11.12
Turn on : 28.9285
Width : 2.847
Height : 9.916
Entry
ampl
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2
4
6
8
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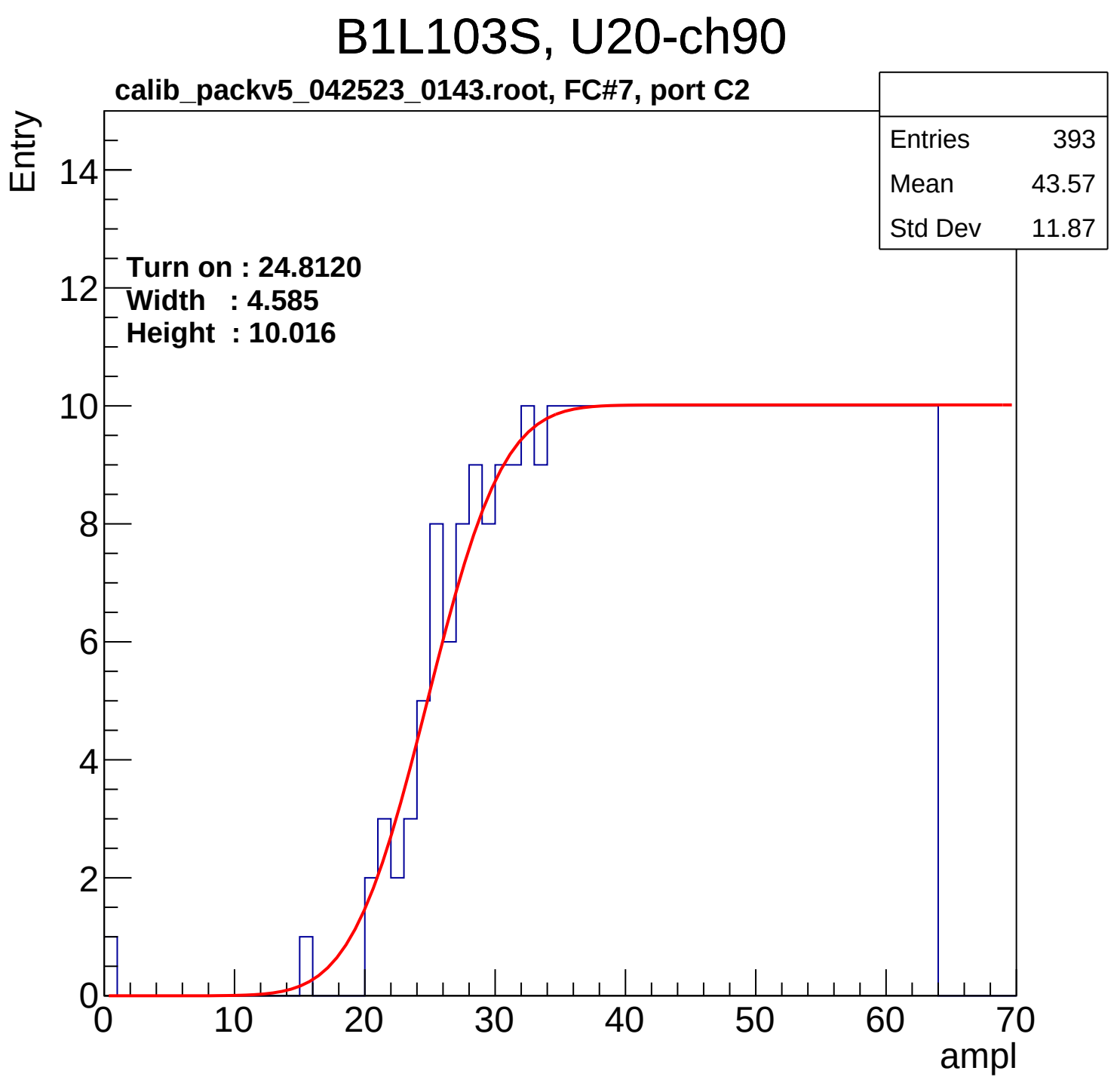
B1L103S, U20-ch90
calib_packv5_042523_0143.root, FC#7, port C2
Entries 393
Mean 43.57
Std Dev 11.87
Turn on : 24.8120
Width : 4.585
Height : 10.016
Entry
ampl
0
2
4
6
8
10
12
14
0
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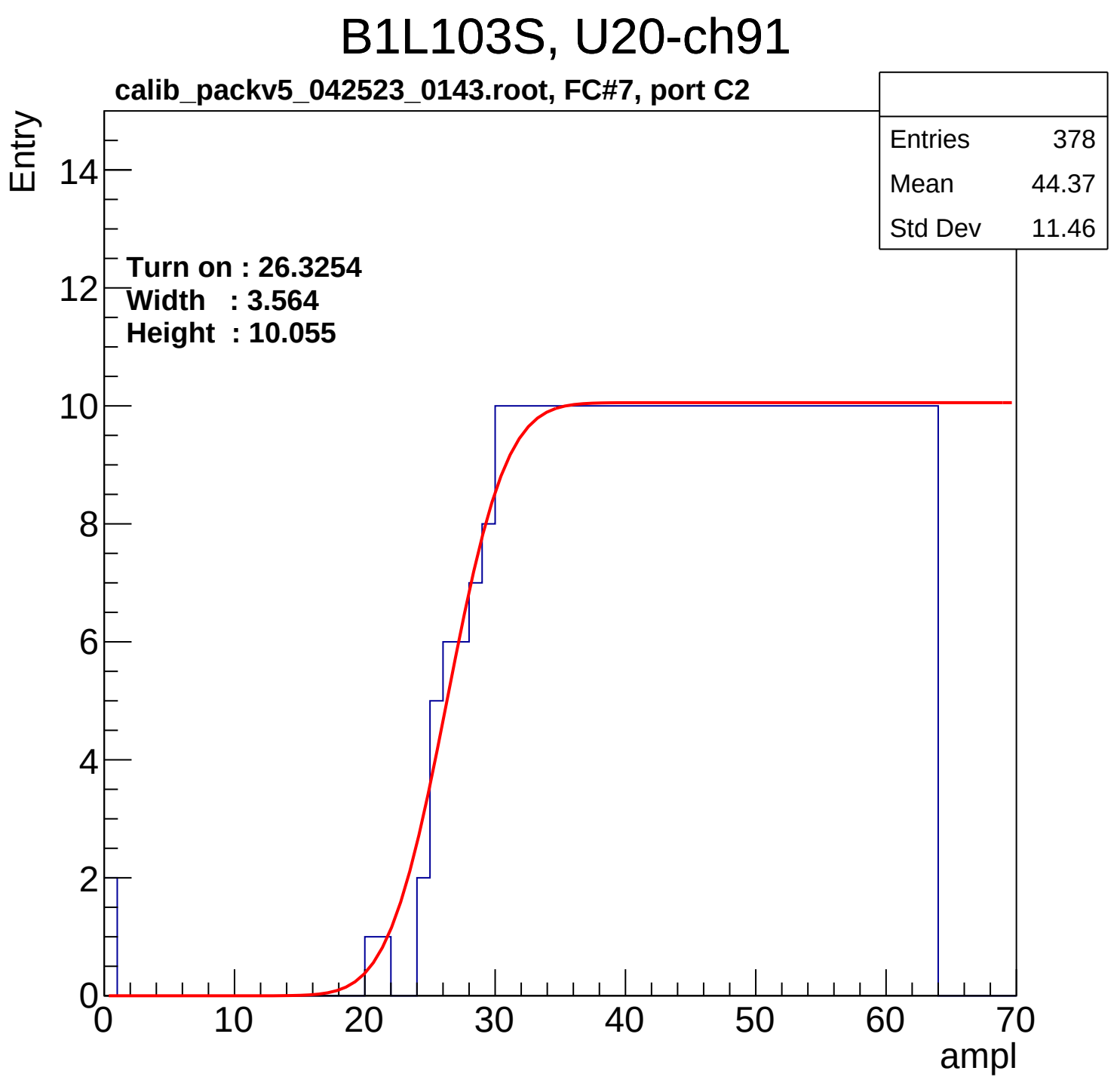
B1L103S, U20-ch91
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.37
Std Dev 11.46
Turn on : 26.3254
Width : 3.564
Height : 10.055
Entry
ampl
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6
8
10
12
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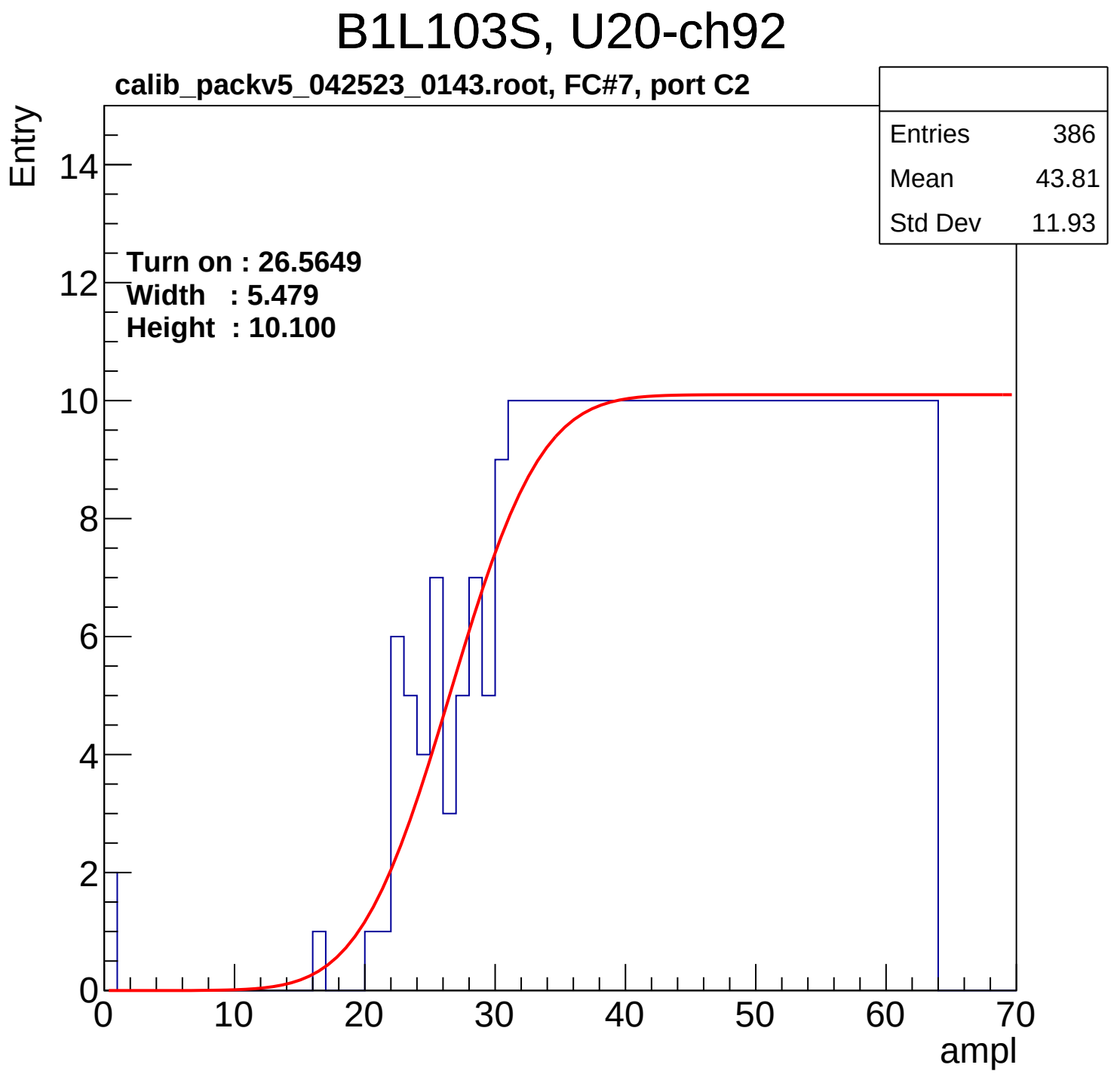
B1L103S, U20-ch92
calib_packv5_042523_0143.root, FC#7, port C2
Entries 386
Mean 43.81
Std Dev 11.93
Turn on : 26.5649
Width : 5.479
Height : 10.100
Entry
ampl
0
2
4
6
8
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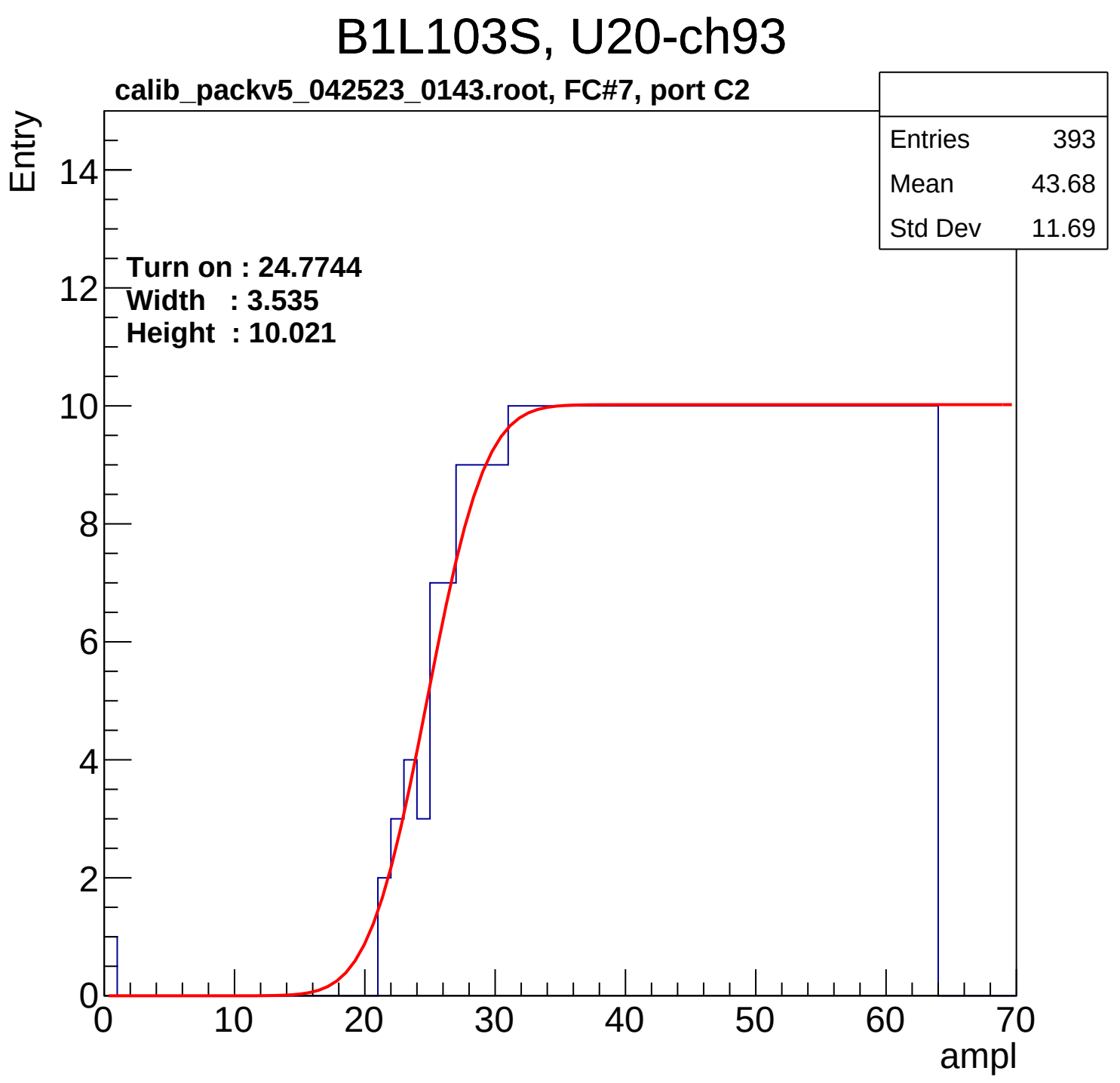
B1L103S, U20-ch93
calib_packv5_042523_0143.root, FC#7, port C2
Entries 393
Mean 43.68
Std Dev 11.69
Turn on : 24.7744
Width : 3.535
Height : 10.021
Entry
ampl
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2
4
6
8
10
12
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0
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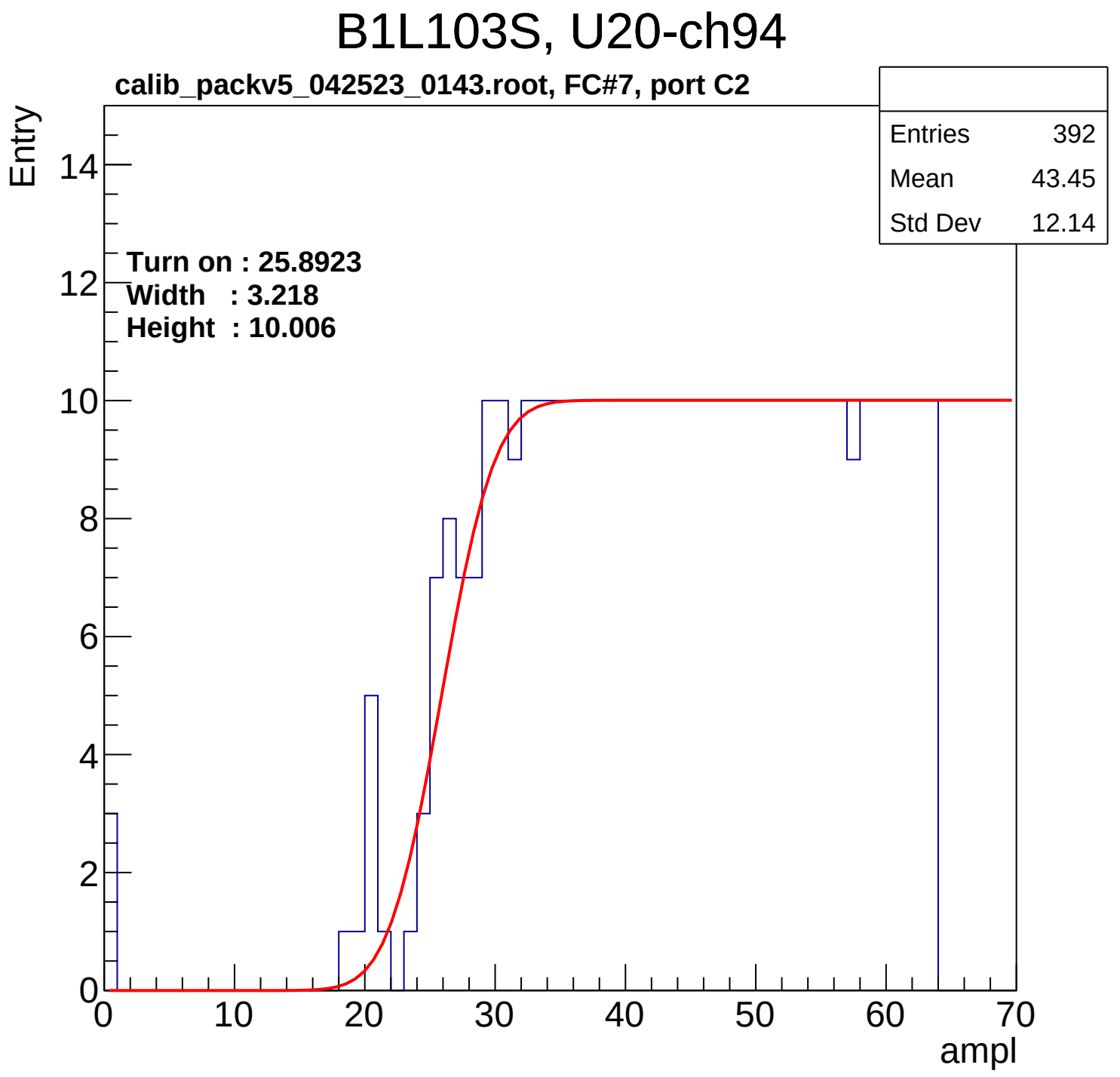
B1L103S, U20-ch94
calib_packv5_042523_0143.root, FC#7, port C2
Entries 392
Mean 43.45
Std Dev 12.14
Turn on : 25.8923
Width : 3.218
Height : 10.006
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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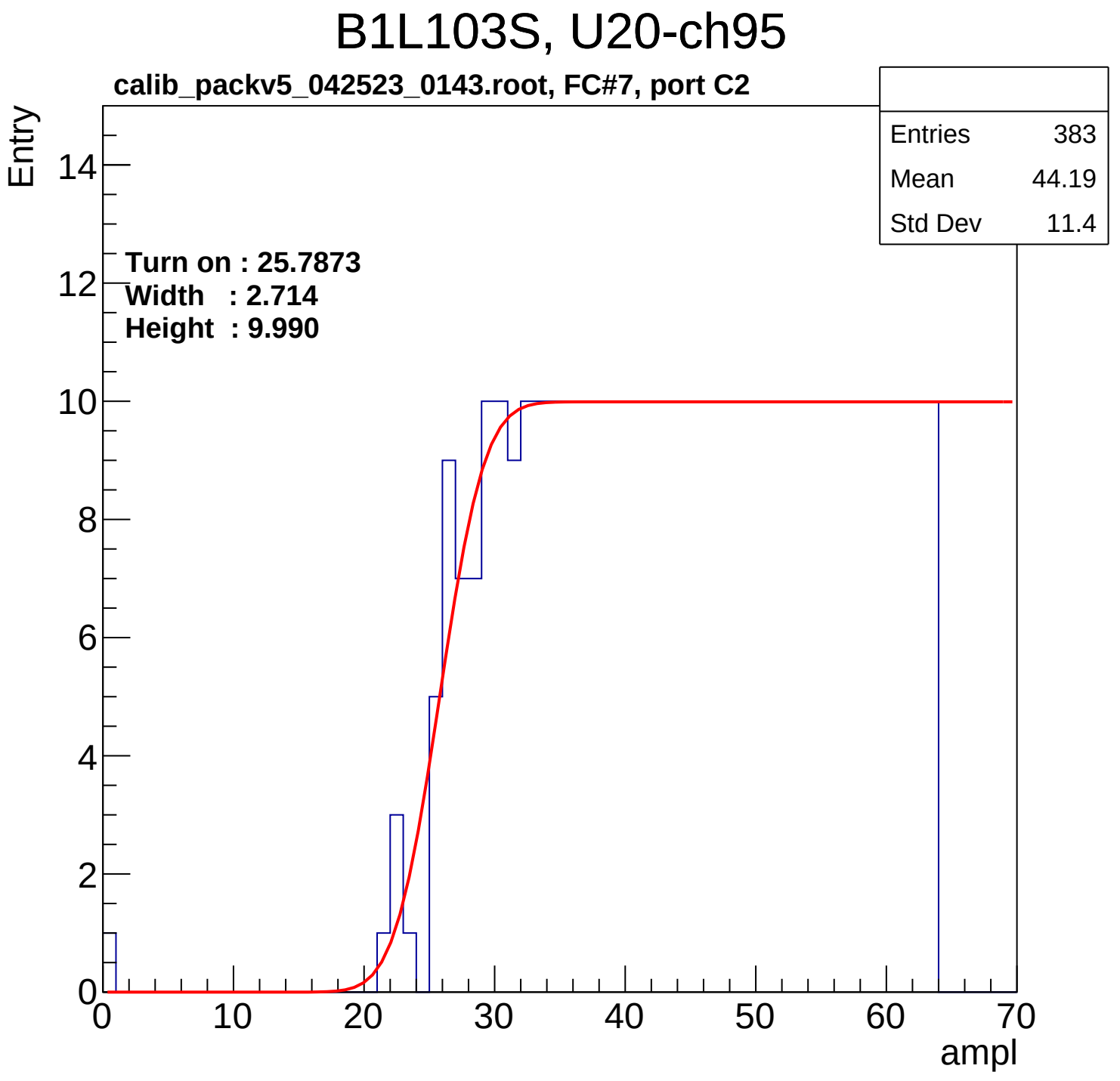
B1L103S, U20-ch95
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 44.19
Std Dev 11.4
Turn on : 25.7873
Width : 2.714
Height : 9.990
Entry
ampl
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2
4
6
8
10
12
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0
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60
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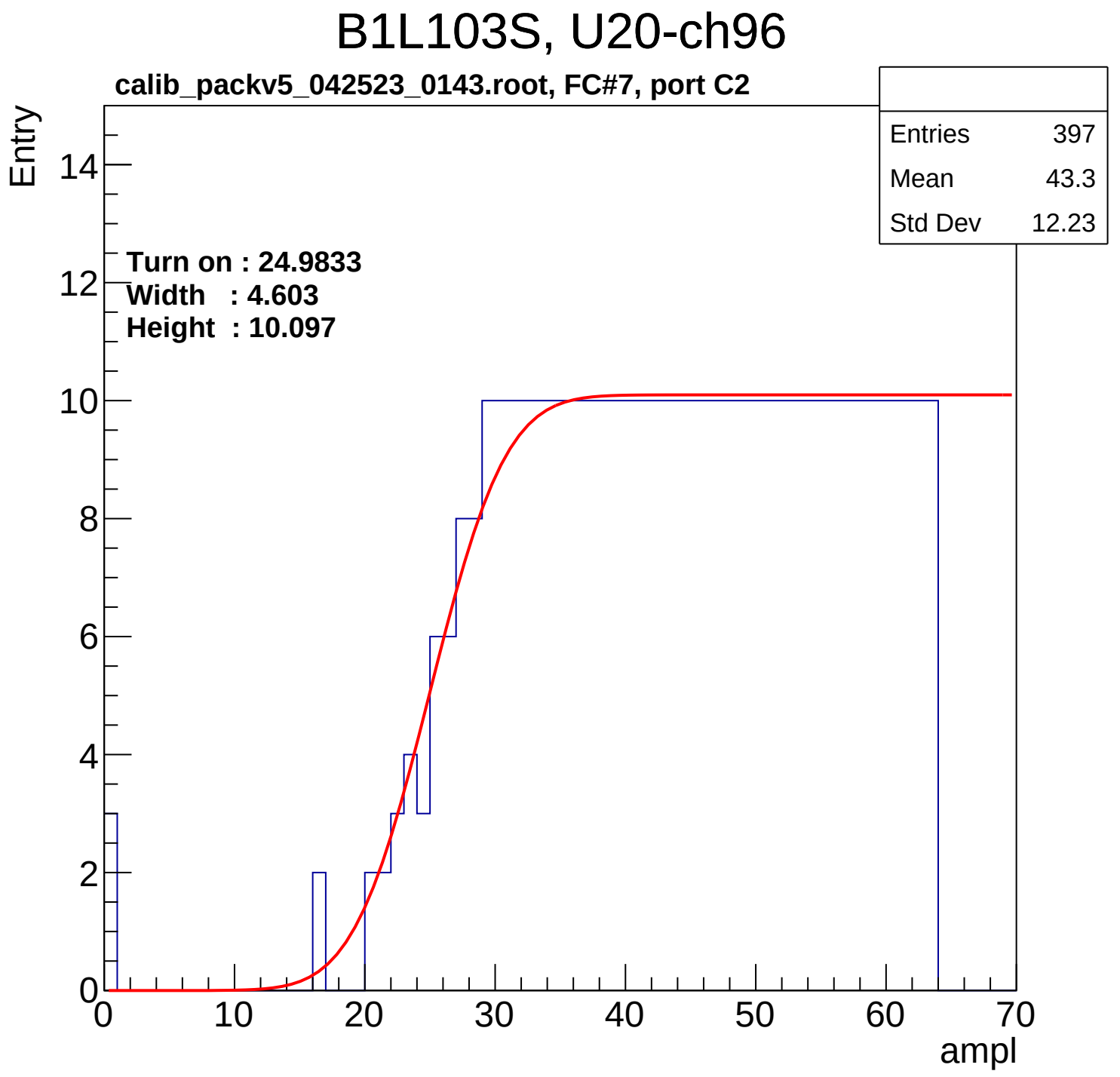
B1L103S, U20-ch96
calib_packv5_042523_0143.root, FC#7, port C2
Entries 397
Mean 43.3
Std Dev 12.23
Turn on : 24.9833
Width : 4.603
Height : 10.097
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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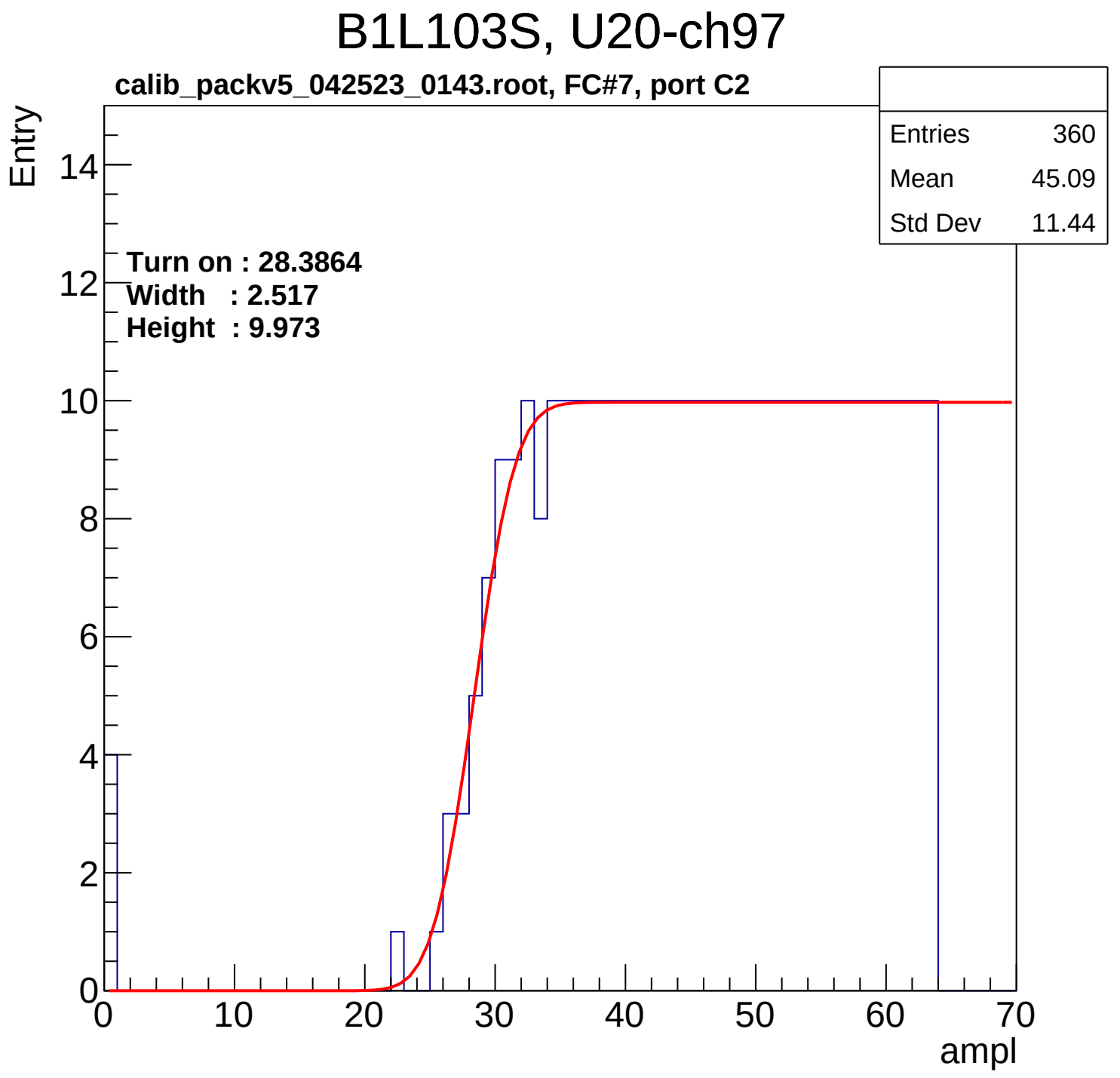
40
50
60
70


B1L103S, U20-ch97
calib_packv5_042523_0143.root, FC#7, port C2
Entries 360
Mean 45.09
Std Dev 11.44
Turn on : 28.3864
Width : 2.517
Height : 9.973
Entry
ampl
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4
6
8
10
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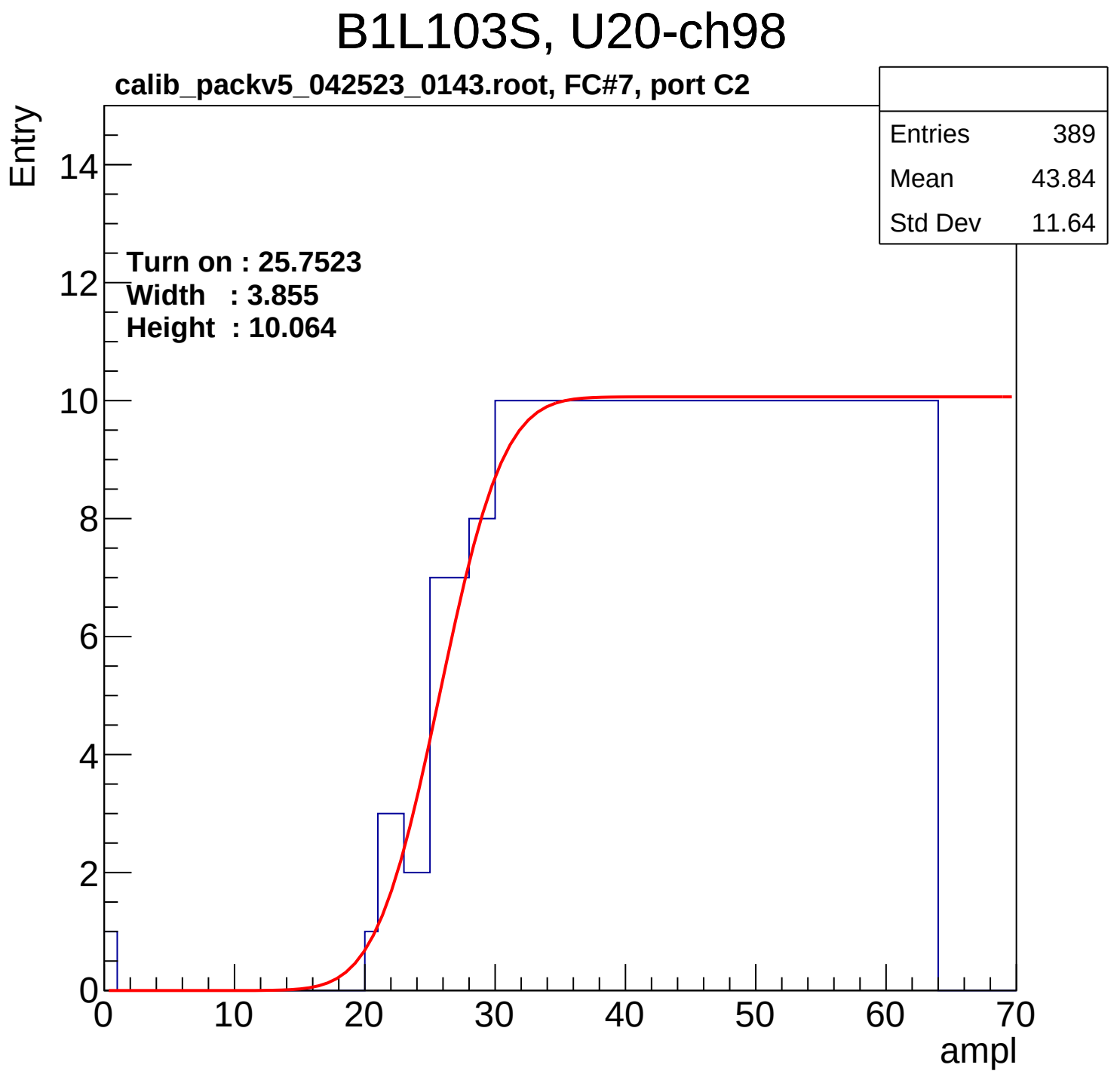
B1L103S, U20-ch98
calib_packv5_042523_0143.root, FC#7, port C2
Entries 389
Mean 43.84
Std Dev 11.64
Turn on : 25.7523
Width : 3.855
Height : 10.064
Entry
ampl
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2
4
6
8
10
12
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20
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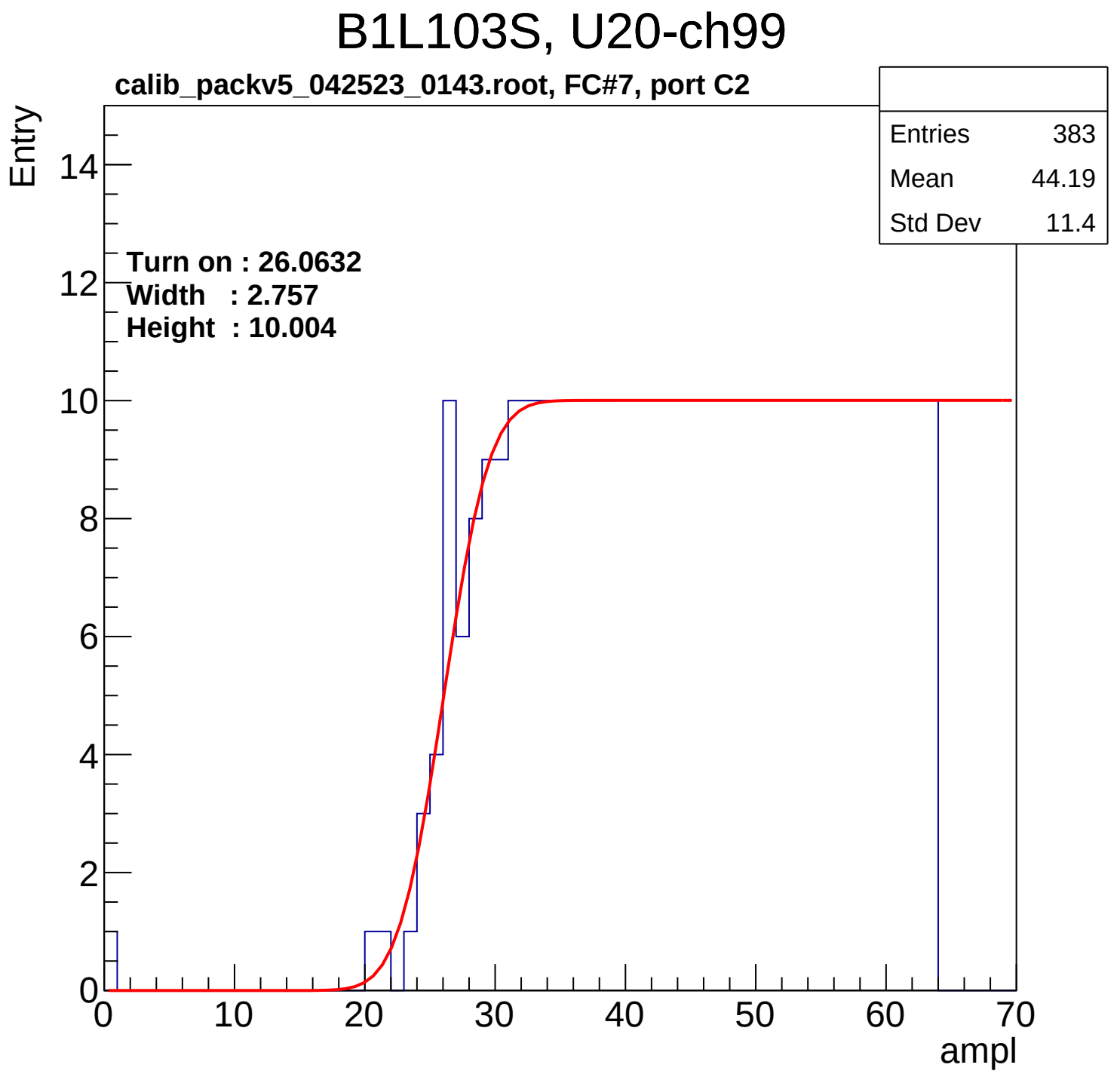
B1L103S, U20-ch99
calib_packv5_042523_0143.root, FC#7, port C2
Entries 383
Mean 44.19
Std Dev 11.4
Turn on : 26.0632
Width : 2.757
Height : 10.004
Entry
ampl
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4
6
8
10
12
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0
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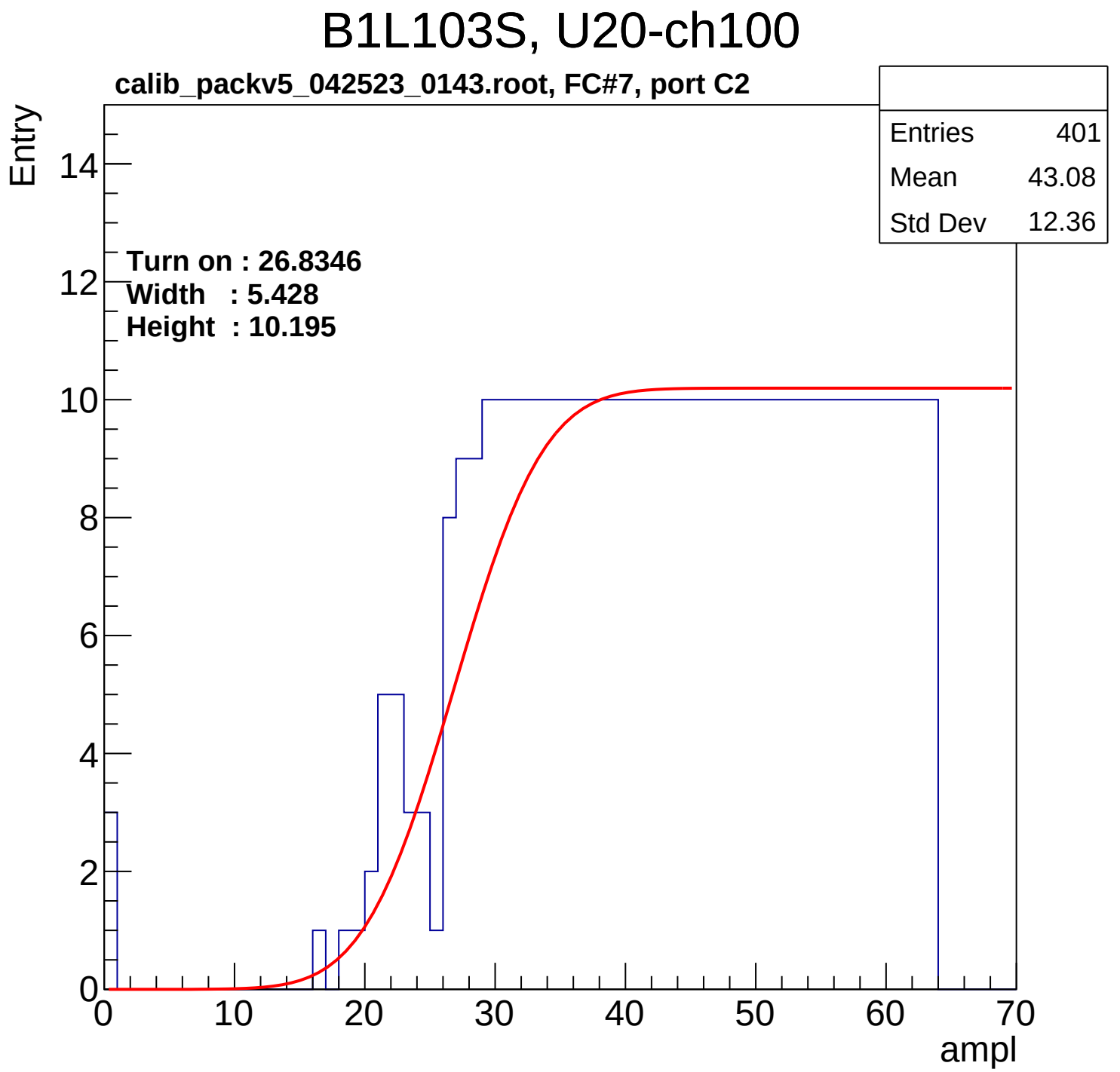
B1L103S, U20-ch100
calib_packv5_042523_0143.root, FC#7, port C2
Entries 401
Mean 43.08
Std Dev 12.36
Turn on : 26.8346
Width : 5.428
Height : 10.195
Entry
ampl
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4
6
8
10
12
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0
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20
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60
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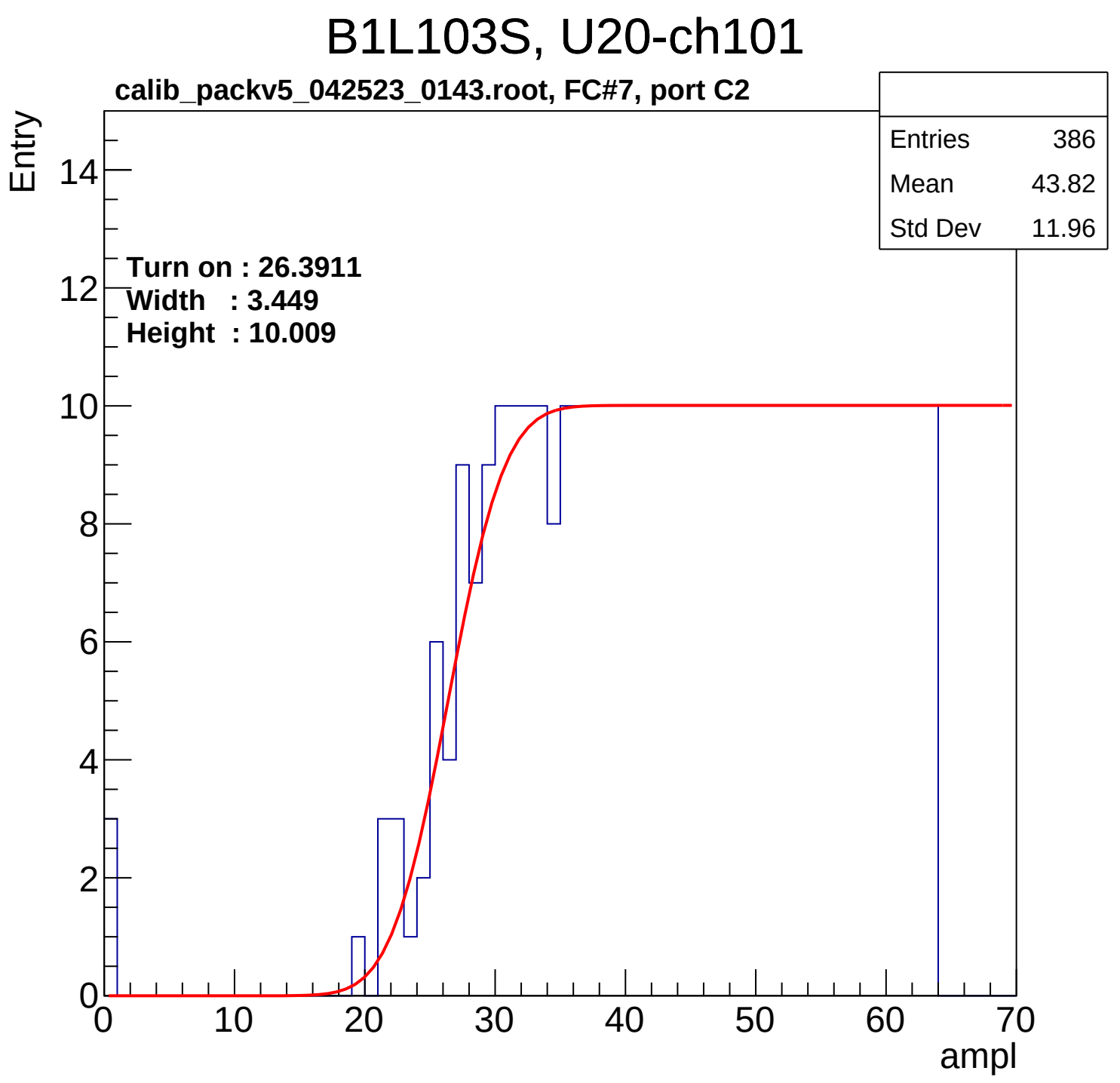
B1L103S, U20-ch101
calib_packv5_042523_0143.root, FC#7, port C2
Entries 386
Mean 43.82
Std Dev 11.96
Turn on : 26.3911
Width : 3.449
Height : 10.009
Entry
ampl
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6
8
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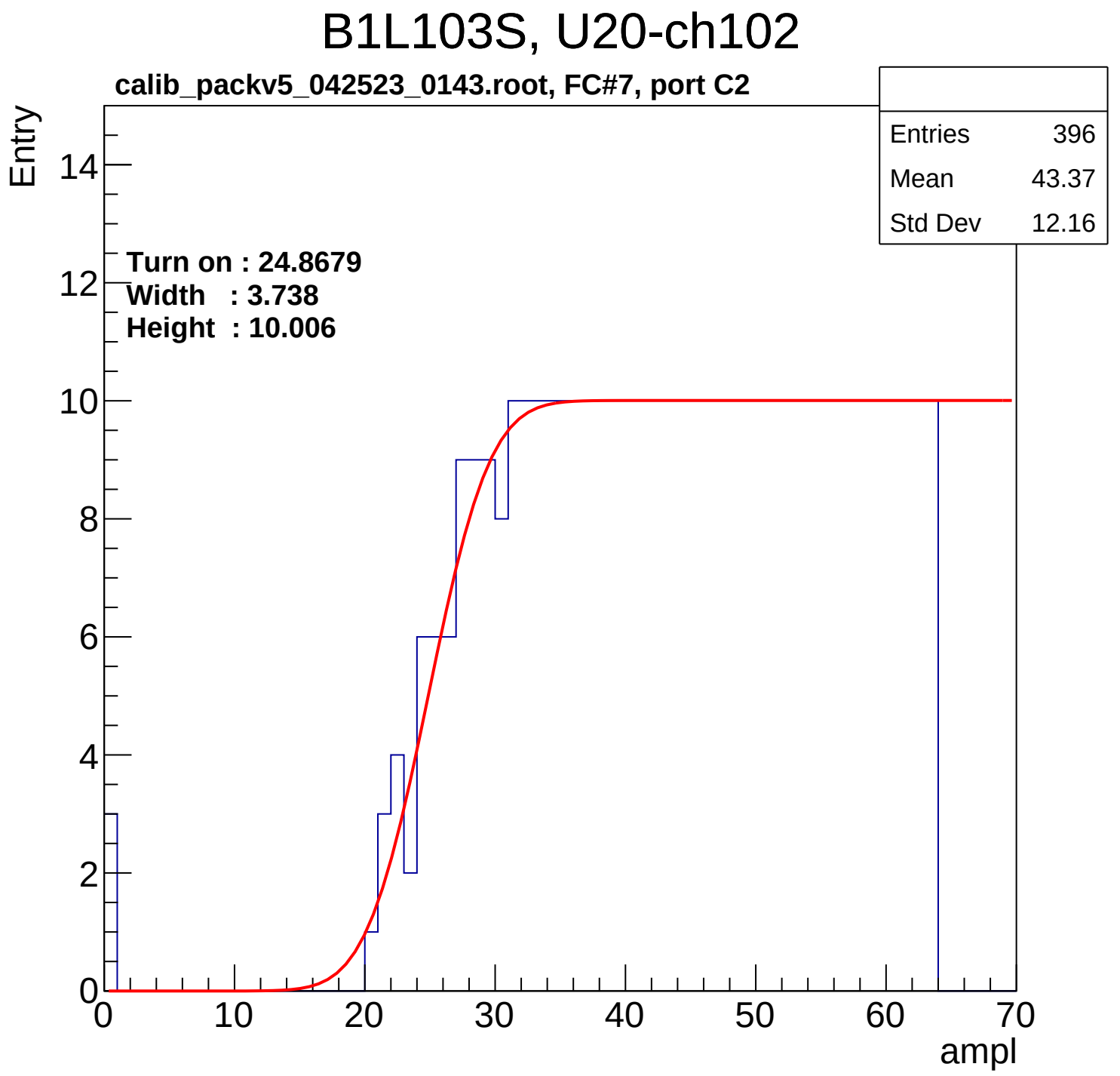
B1L103S, U20-ch102
calib_packv5_042523_0143.root, FC#7, port C2
Entries 396
Mean 43.37
Std Dev 12.16
Turn on : 24.8679
Width : 3.738
Height : 10.006
Entry
ampl
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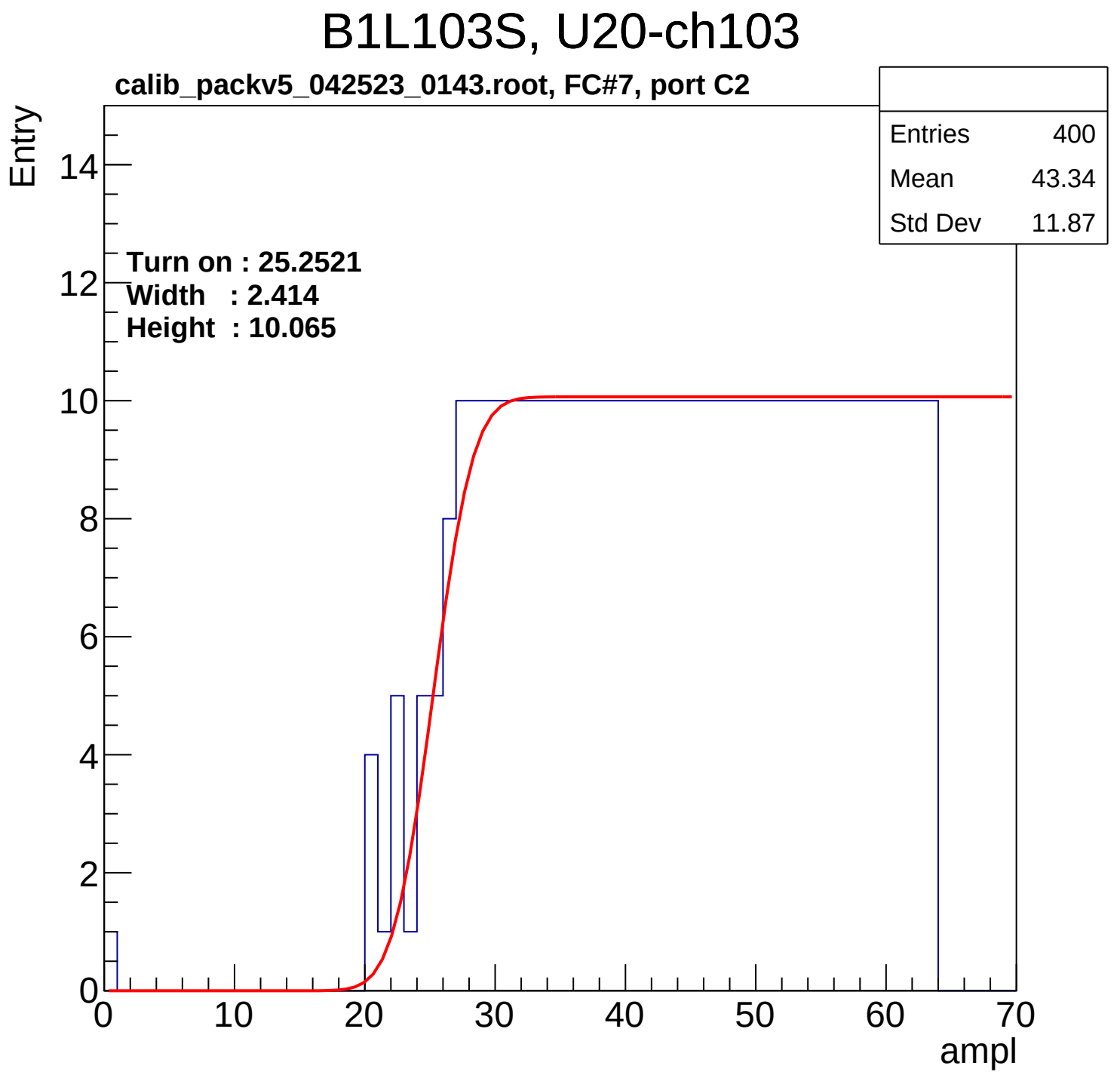
B1L103S, U20-ch103
calib_packv5_042523_0143.root, FC#7, port C2
Entries 400
Mean 43.34
Std Dev 11.87
Turn on : 25.2521
Width : 2.414
Height : 10.065
Entry
ampl
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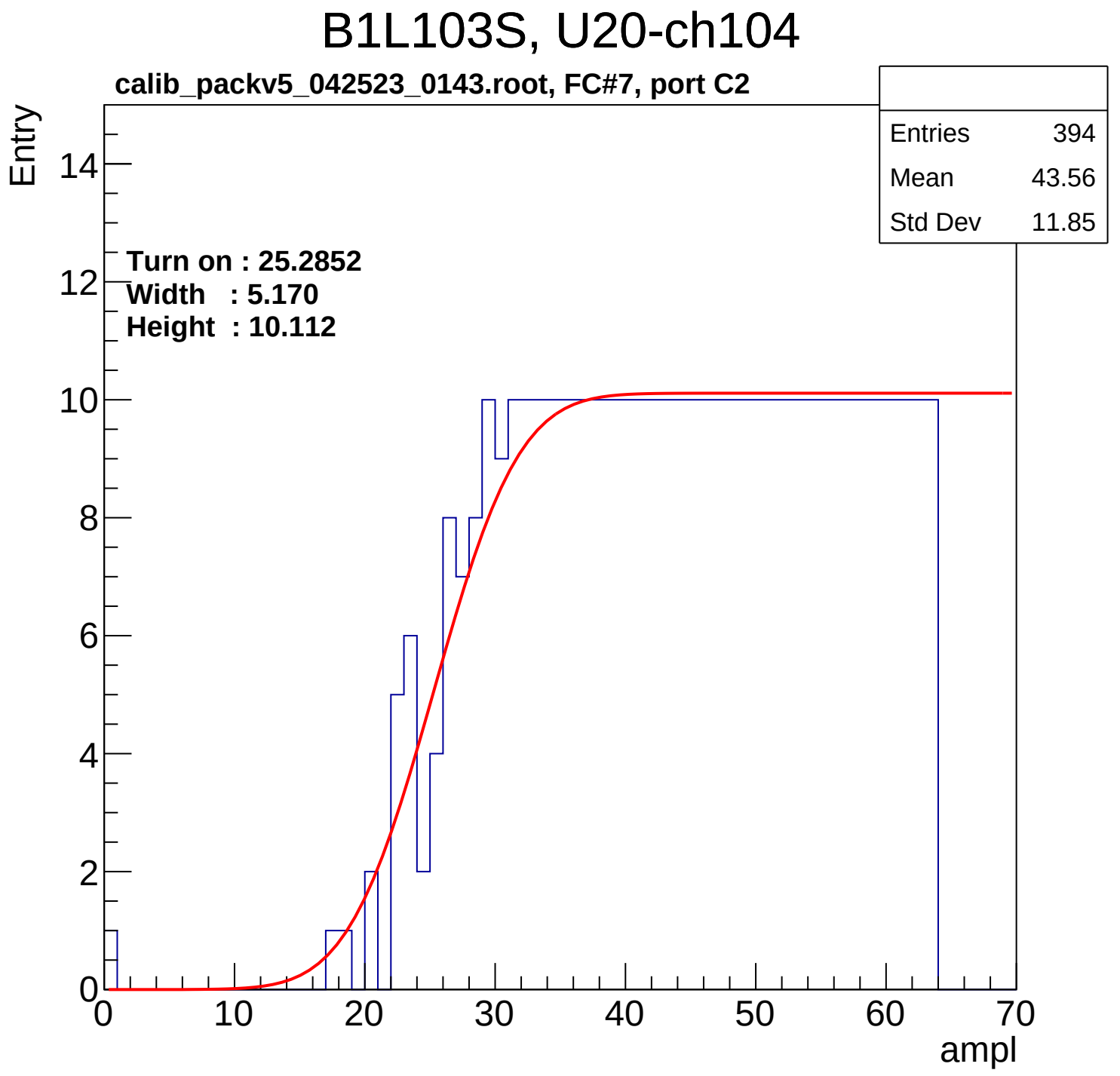
B1L103S, U20-ch104
calib_packv5_042523_0143.root, FC#7, port C2
Entries 394
Mean 43.56
Std Dev 11.85
Turn on : 25.2852
Width : 5.170
Height : 10.112
Entry
ampl
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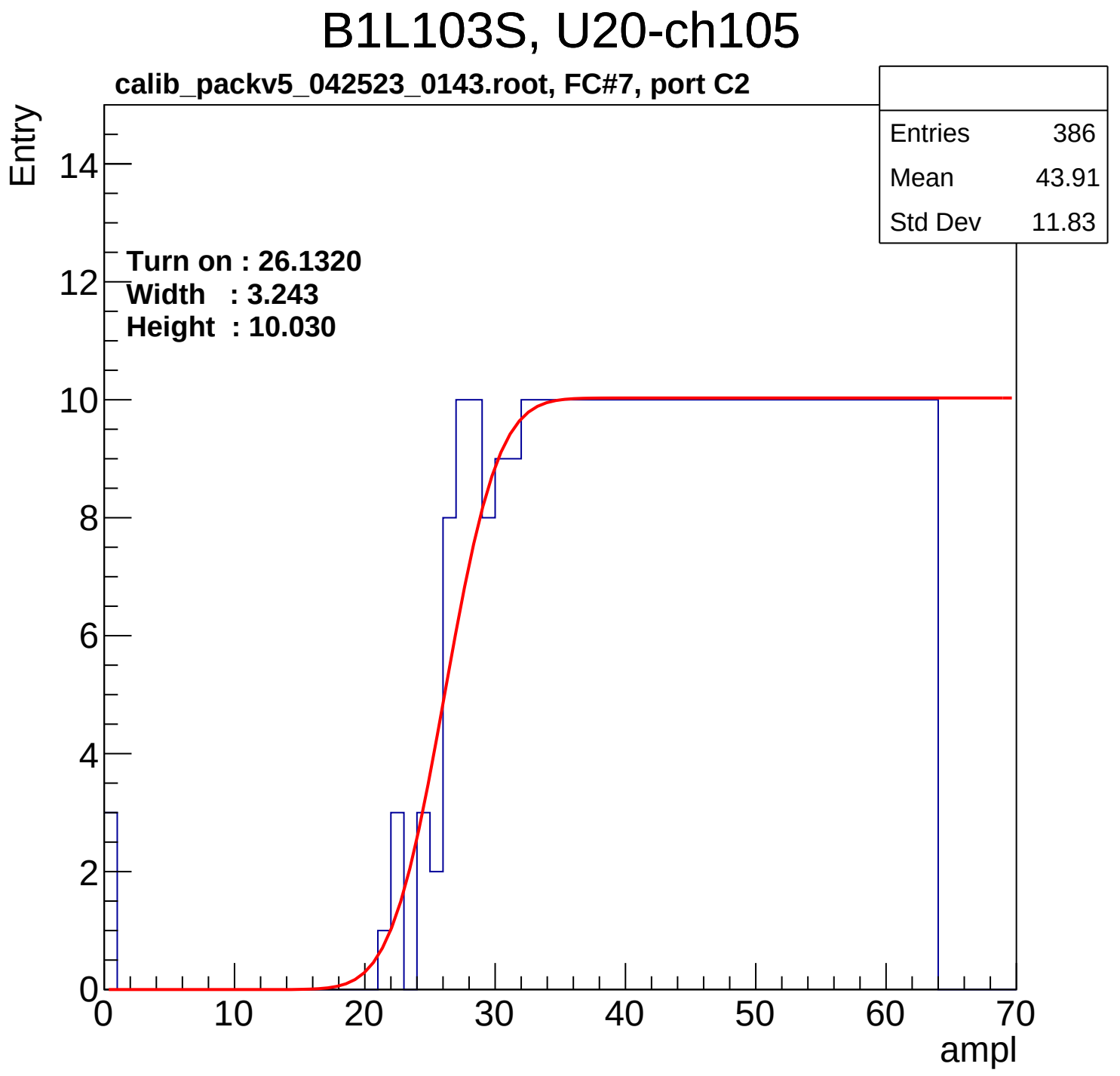
B1L103S, U20-ch105
calib_packv5_042523_0143.root, FC#7, port C2
Entries 386
Mean 43.91
Std Dev 11.83
Turn on : 26.1320
Width : 3.243
Height : 10.030
Entry
ampl
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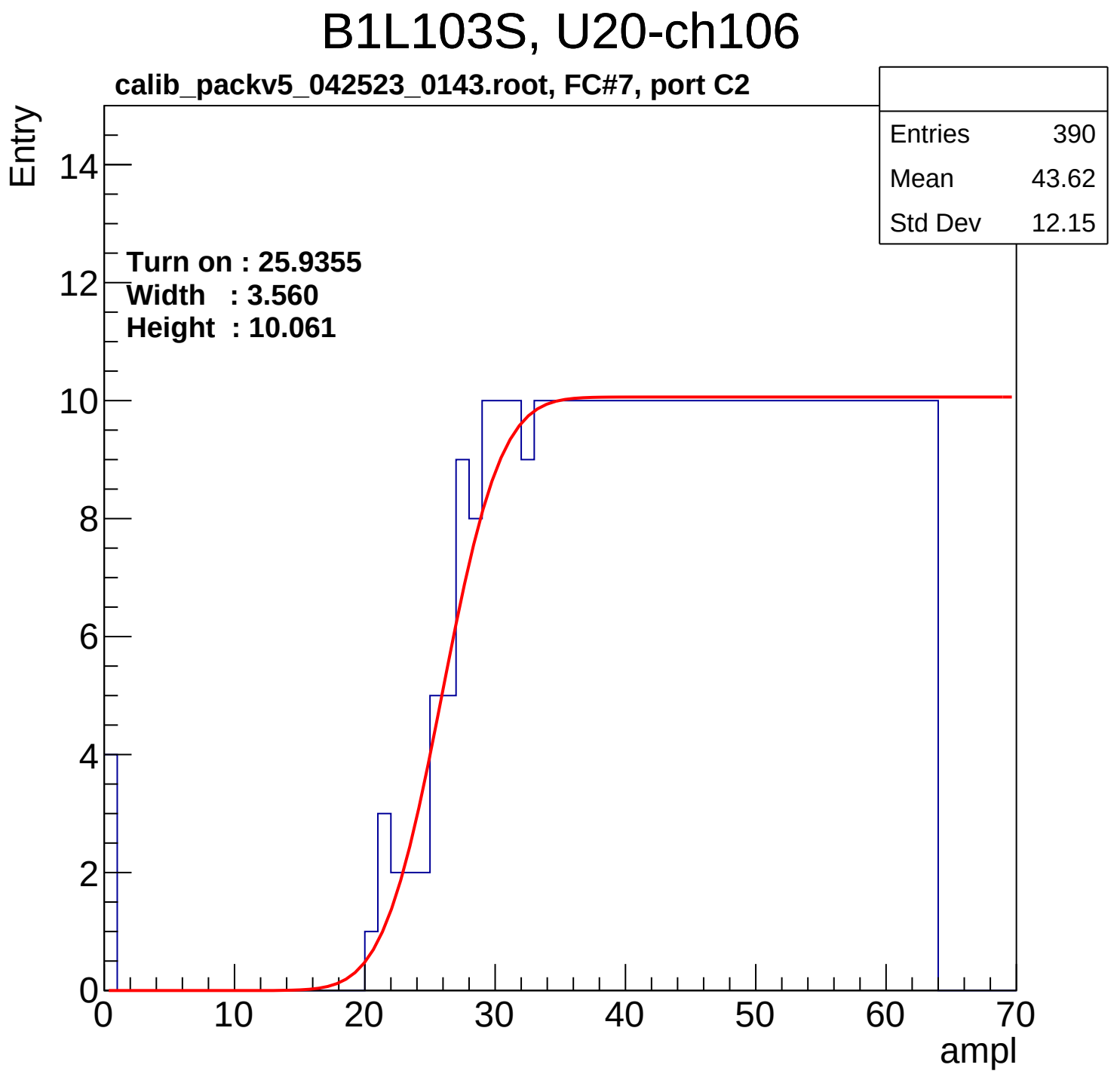
B1L103S, U20-ch106
calib_packv5_042523_0143.root, FC#7, port C2
Entries 390
Mean 43.62
Std Dev 12.15
Turn on : 25.9355
Width : 3.560
Height : 10.061
Entry
ampl
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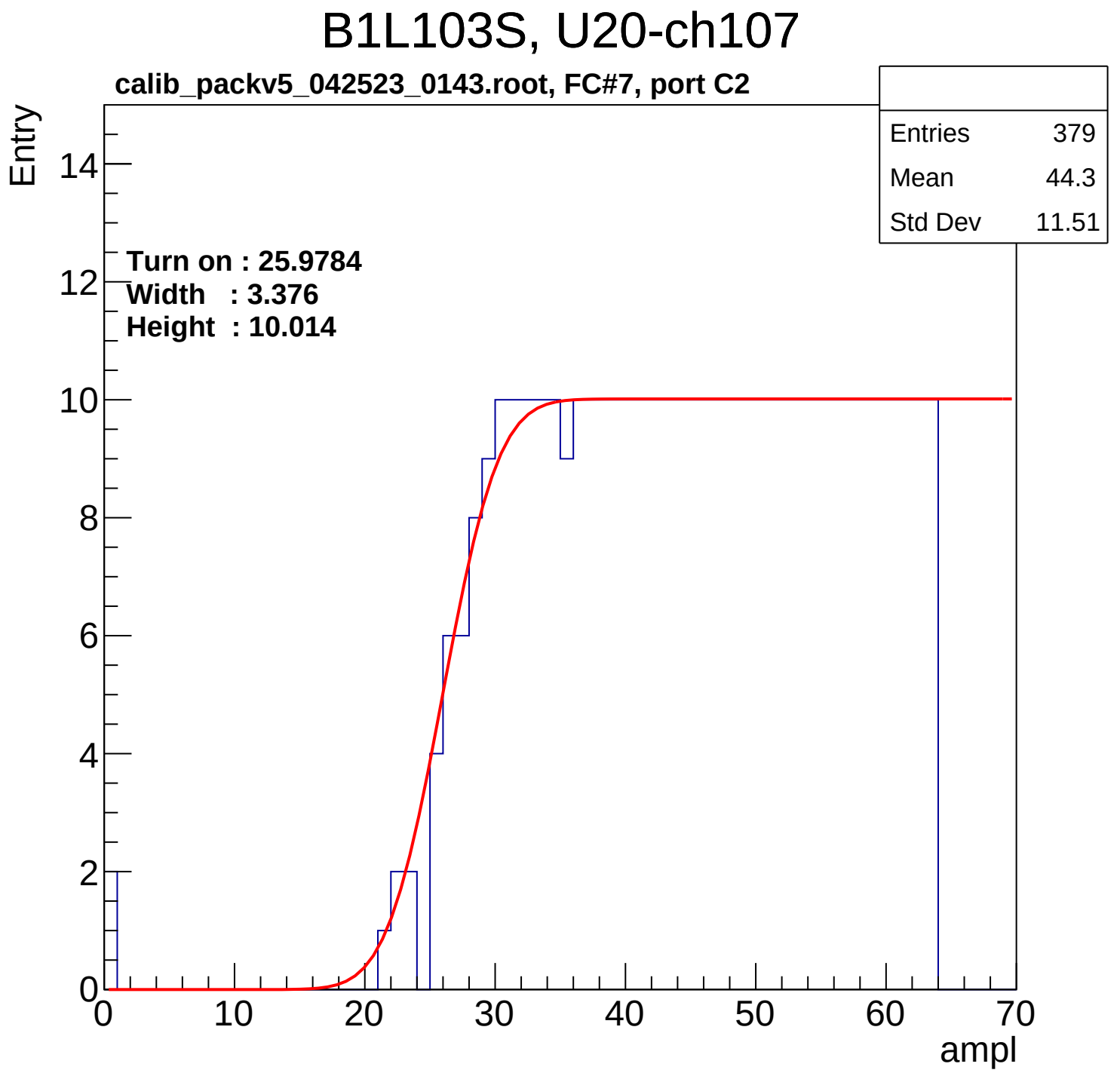
B1L103S, U20-ch107
calib_packv5_042523_0143.root, FC#7, port C2
Entries 379
Mean 44.3
Std Dev 11.51
Turn on : 25.9784
Width : 3.376
Height : 10.014
Entry
ampl
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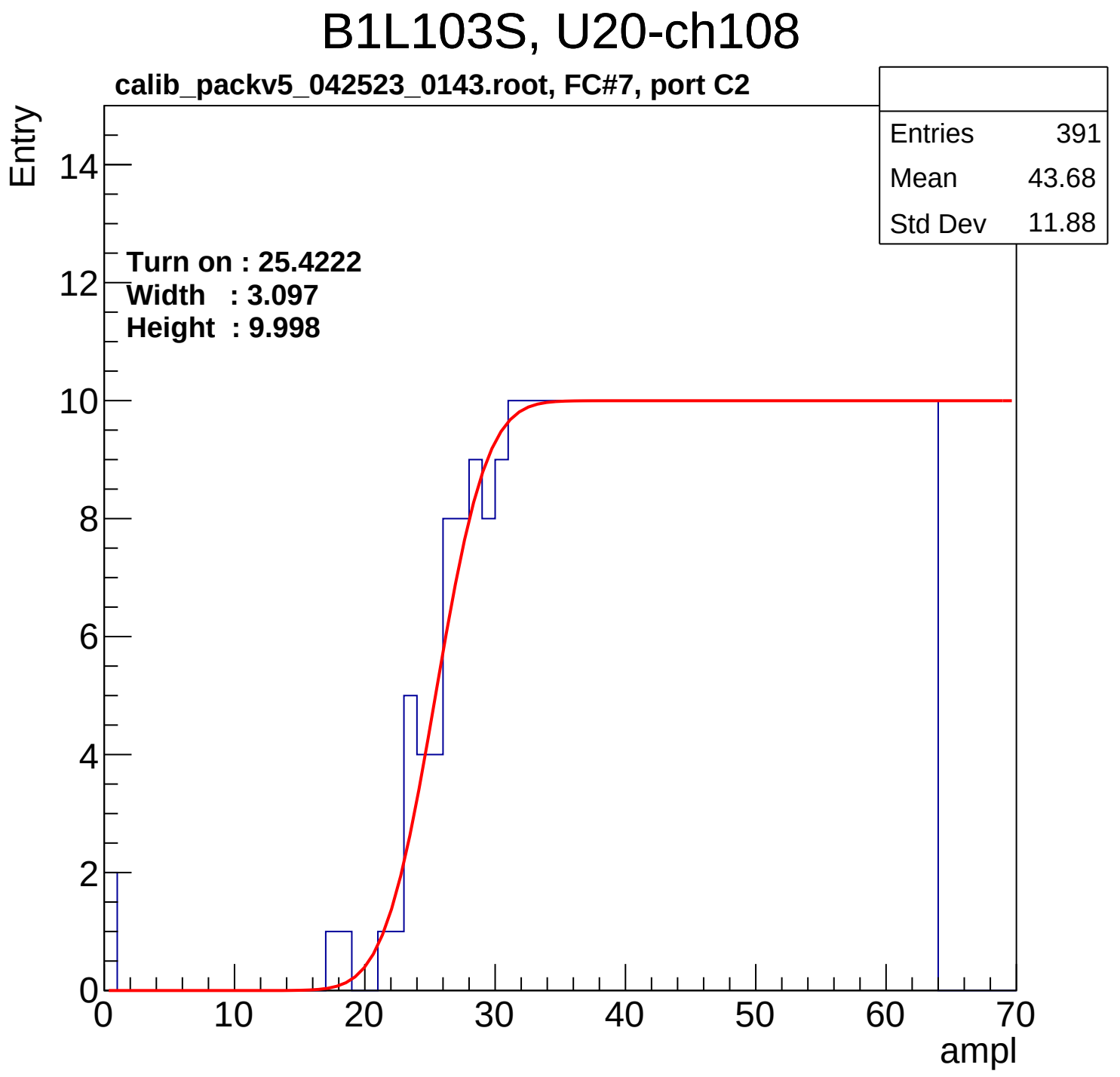
B1L103S, U20-ch108
calib_packv5_042523_0143.root, FC#7, port C2
Entries 391
Mean 43.68
Std Dev 11.88
Turn on : 25.4222
Width : 3.097
Height : 9.998
Entry
ampl
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2
4
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8
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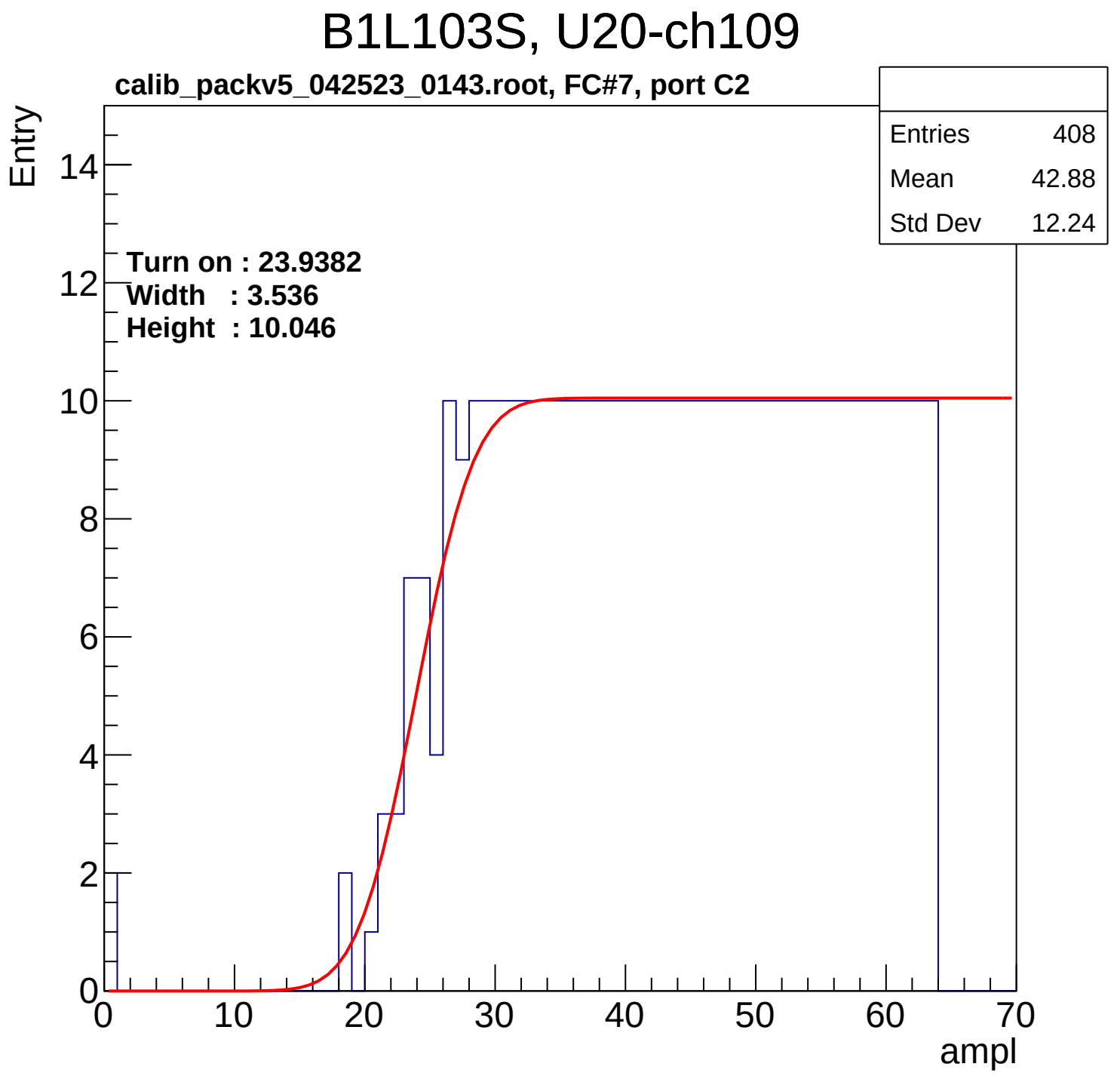
B1L103S, U20-ch109
calib_packv5_042523_0143.root, FC#7, port C2
Entries 408
Mean 42.88
Std Dev 12.24
Turn on : 23.9382
Width : 3.536
Height : 10.046
Entry
ampl
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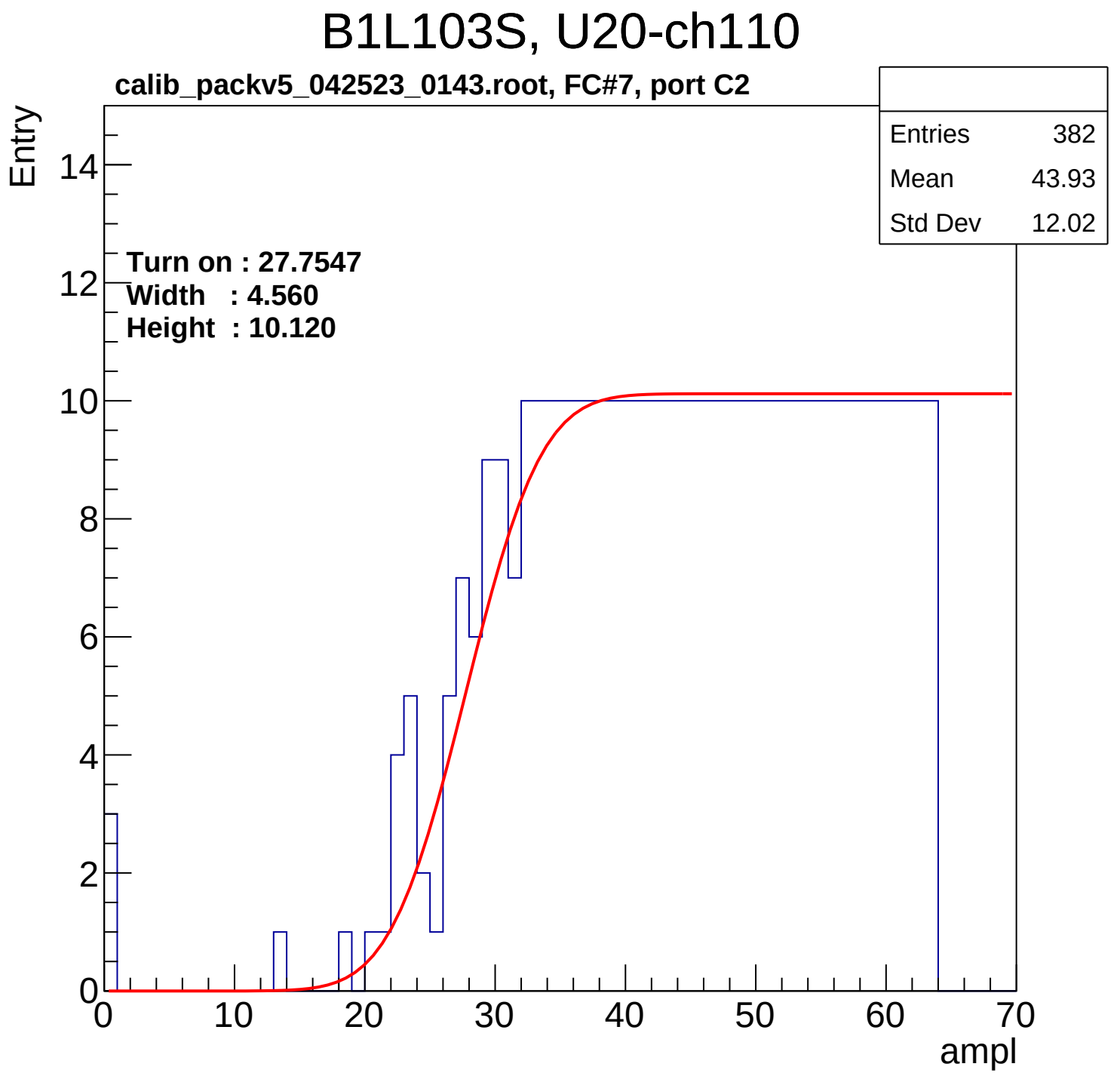
B1L103S, U20-ch110
calib_packv5_042523_0143.root, FC#7, port C2
Entries 382
Mean 43.93
Std Dev 12.02
Turn on : 27.7547
Width : 4.560
Height : 10.120
Entry
ampl
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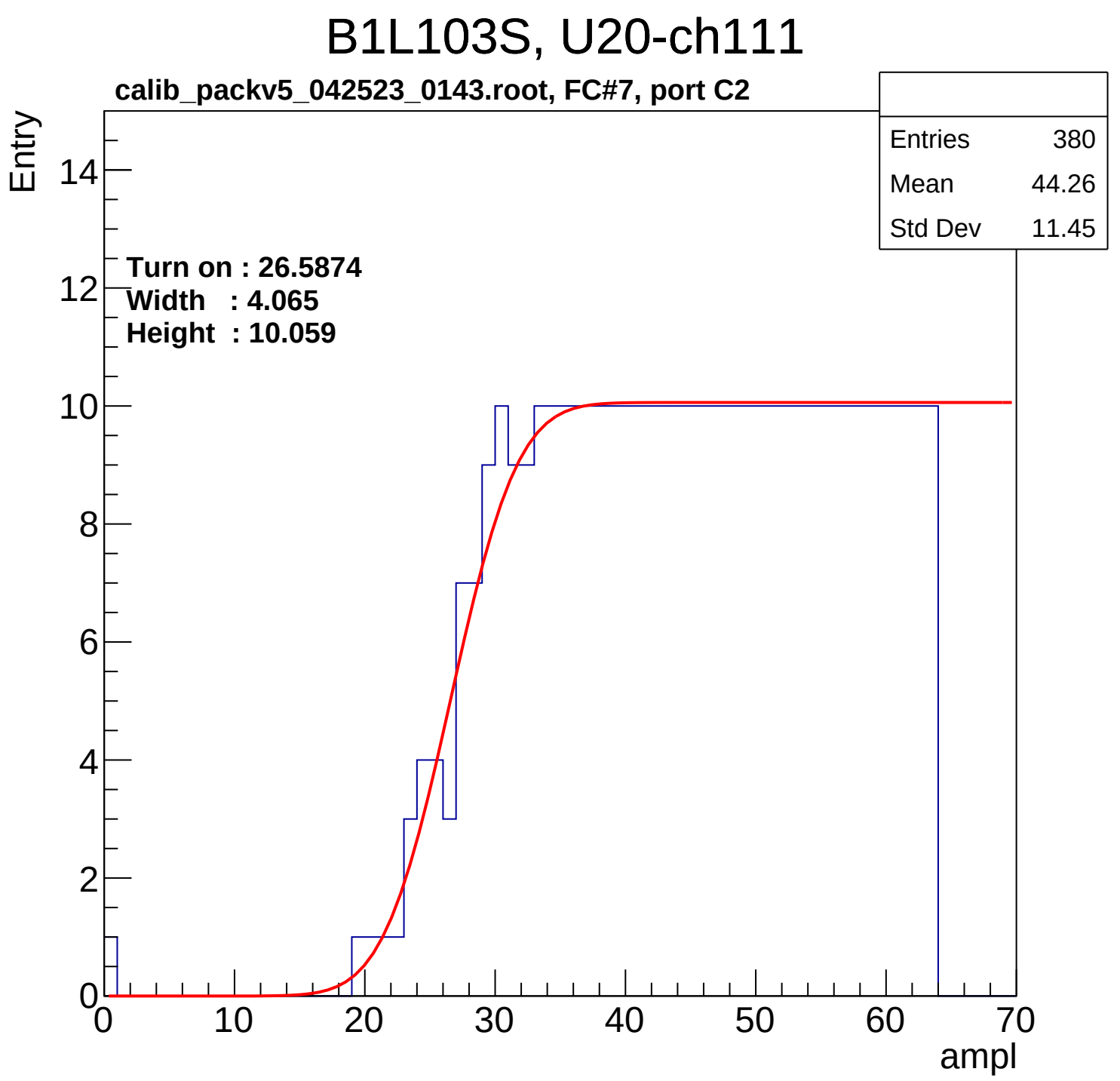
B1L103S, U20-ch111
calib_packv5_042523_0143.root, FC#7, port C2
Entries 380
Mean 44.26
Std Dev 11.45
Turn on : 26.5874
Width : 4.065
Height : 10.059
Entry
ampl
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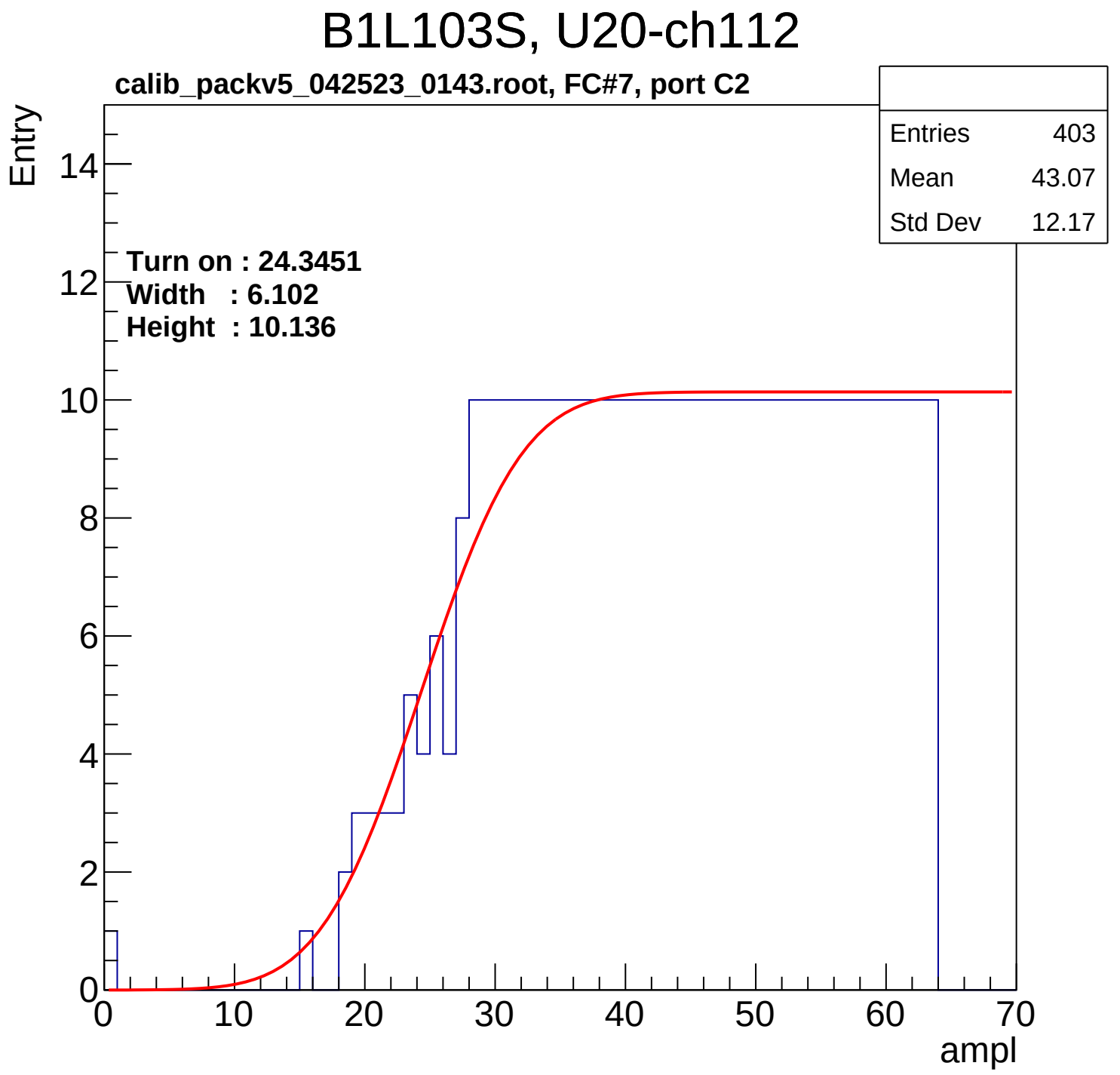
B1L103S, U20-ch112
calib_packv5_042523_0143.root, FC#7, port C2
Entries 403
Mean 43.07
Std Dev 12.17
Turn on : 24.3451
Width : 6.102
Height : 10.136
Entry
ampl
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2
4
6
8
10
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0
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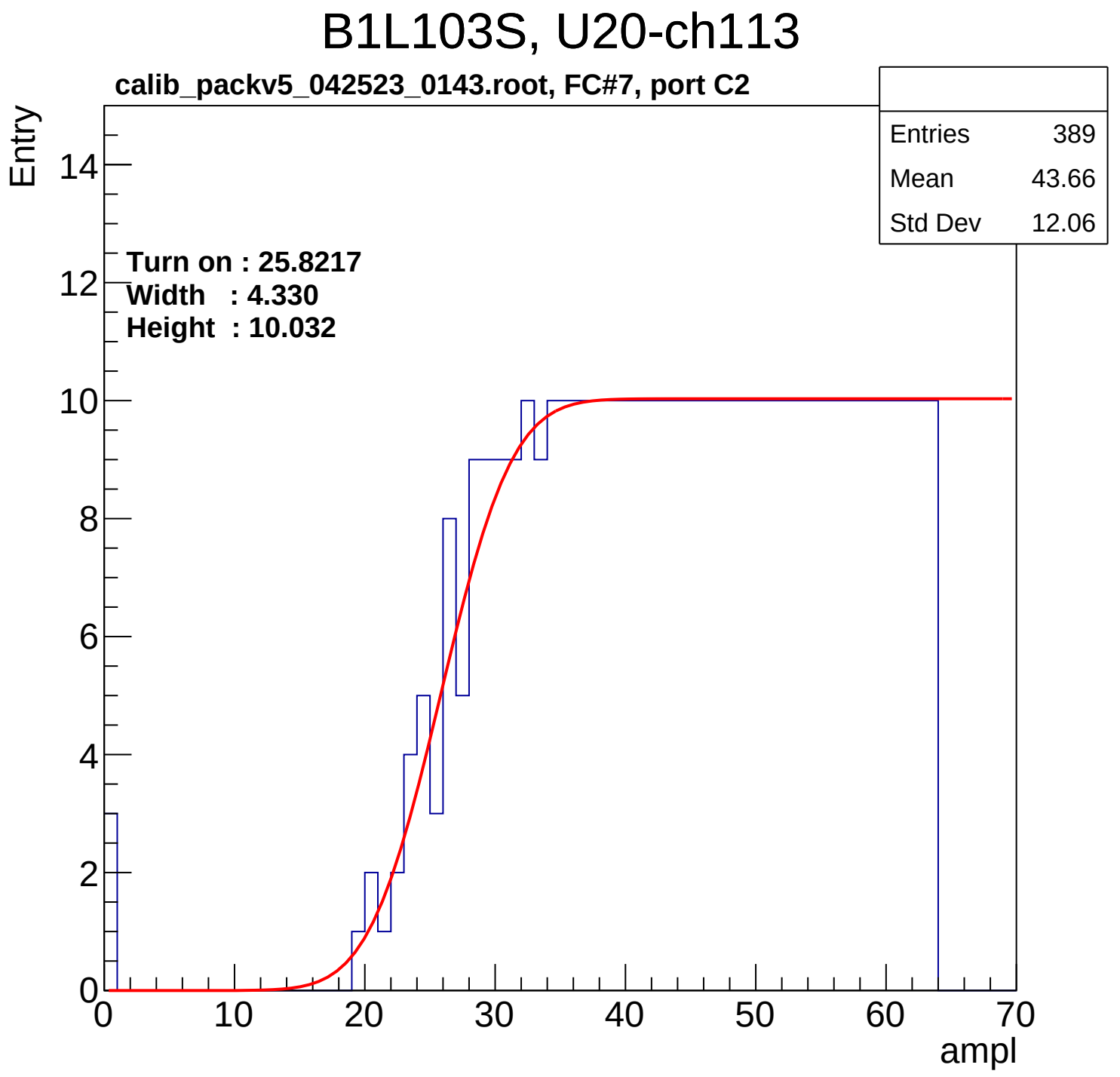
B1L103S, U20-ch113
calib_packv5_042523_0143.root, FC#7, port C2
Entries 389
Mean 43.66
Std Dev 12.06
Turn on : 25.8217
Width : 4.330
Height : 10.032
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ampl
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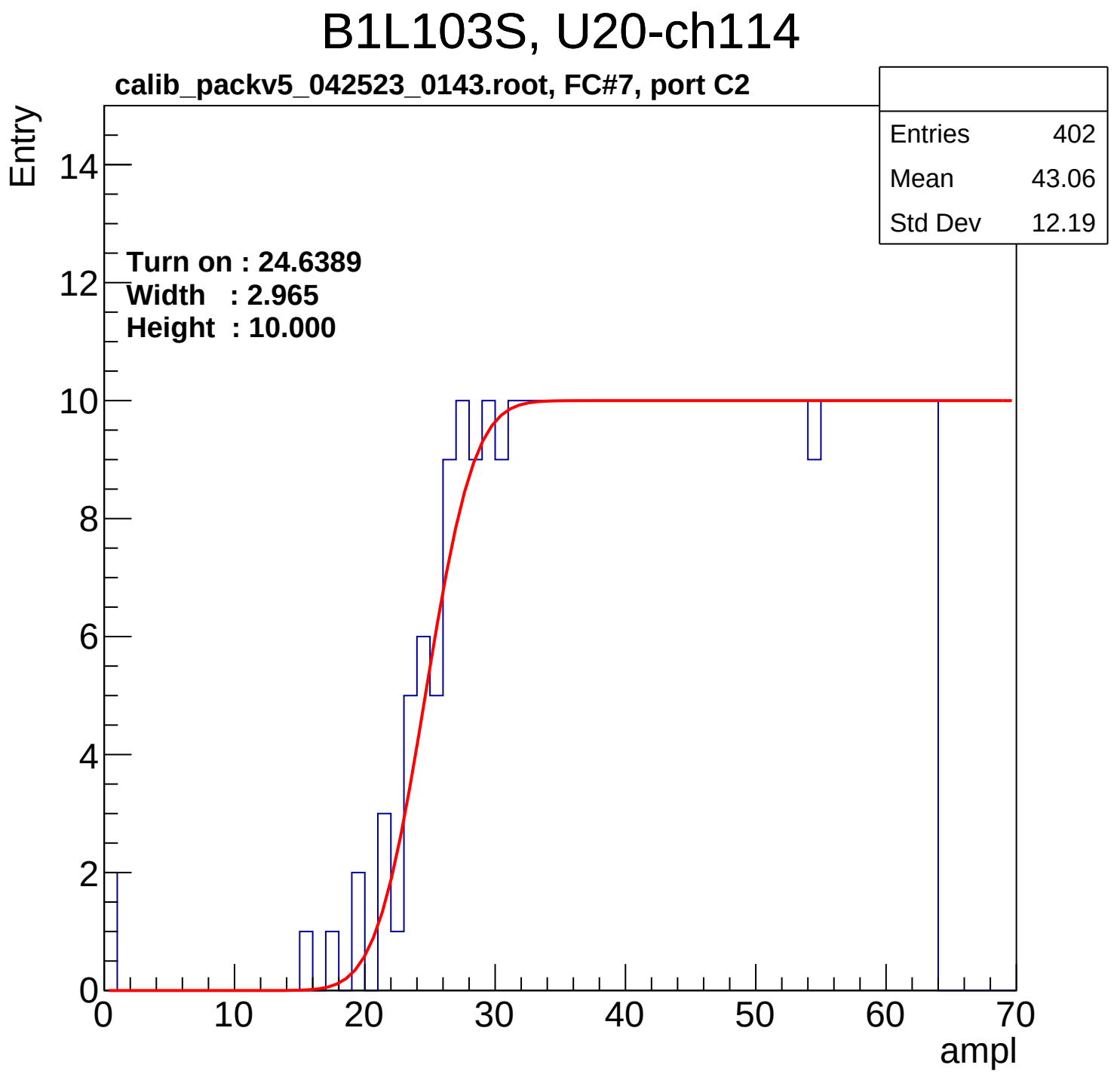
B1L103S, U20-ch114
calib_packv5_042523_0143.root, FC#7, port C2
Entries 402
Mean 43.06
Std Dev 12.19
Turn on : 24.6389
Width : 2.965
Height : 10.000
Entry
ampl
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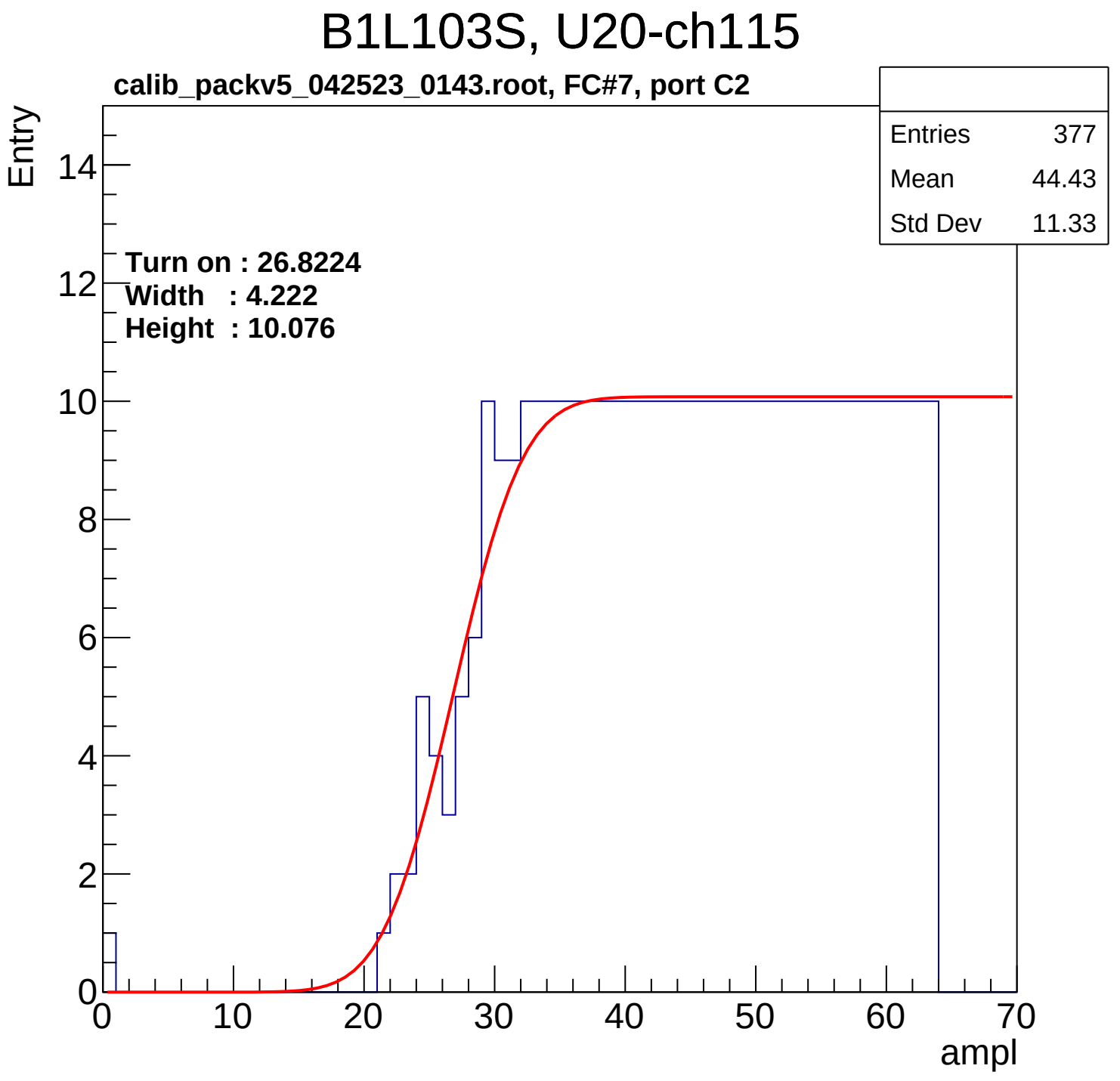
B1L103S, U20-ch115
calib_packv5_042523_0143.root, FC#7, port C2
Entries 377
Mean 44.43
Std Dev 11.33
Turn on : 26.8224
Width : 4.222
Height : 10.076
Entry
ampl
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4
6
8
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12
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10
20
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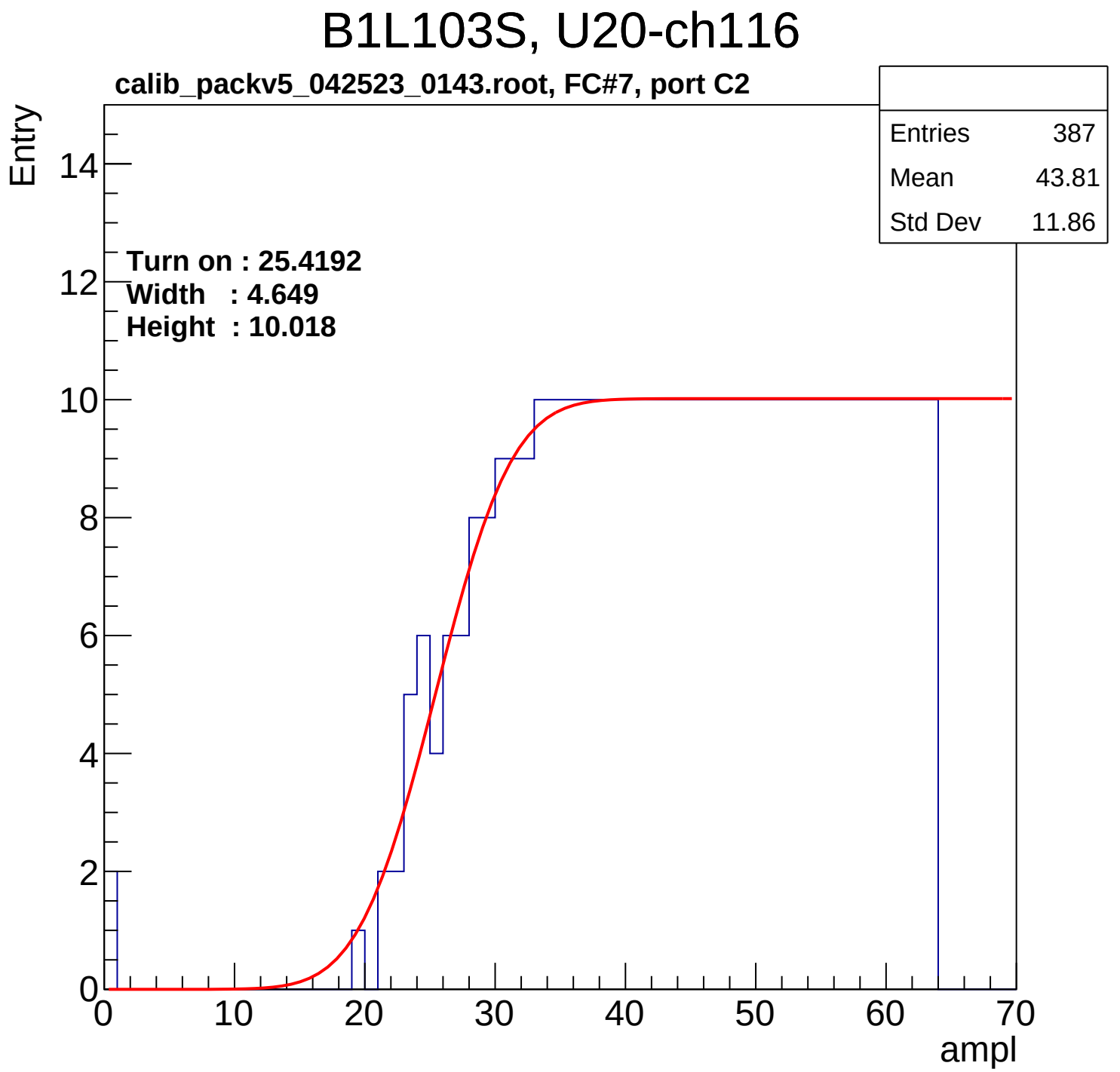
B1L103S, U20-ch116
calib_packv5_042523_0143.root, FC#7, port C2
Entries 387
Mean 43.81
Std Dev 11.86
Turn on : 25.4192
Width : 4.649
Height : 10.018
Entry
ampl
0
2
4
6
8
10
12
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0
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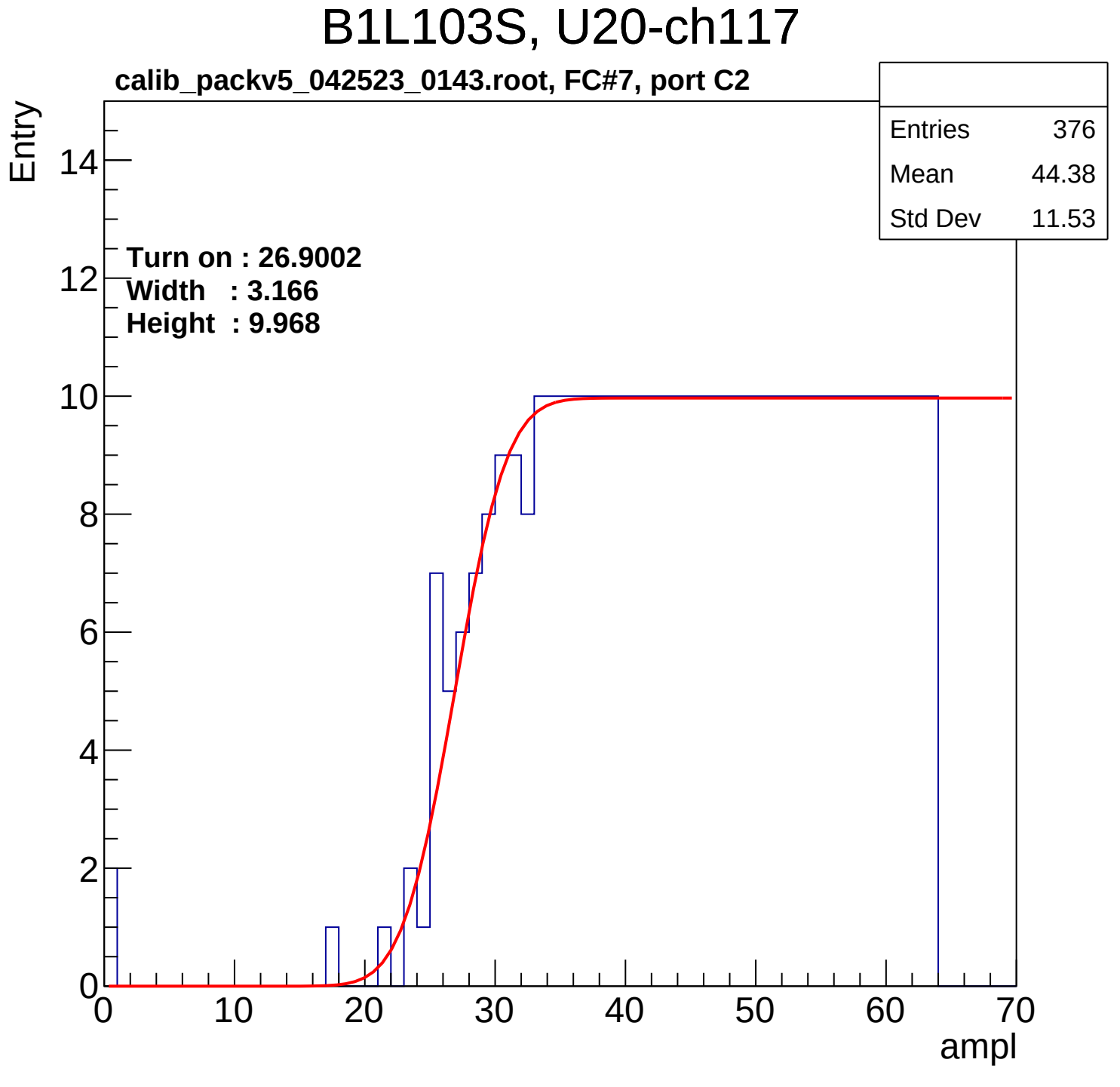
B1L103S, U20-ch117
calib_packv5_042523_0143.root, FC#7, port C2
Entries 376
Mean 44.38
Std Dev 11.53
Turn on : 26.9002
Width : 3.166
Height : 9.968
Entry
ampl
0
2
4
6
8
10
12
14
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20
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40
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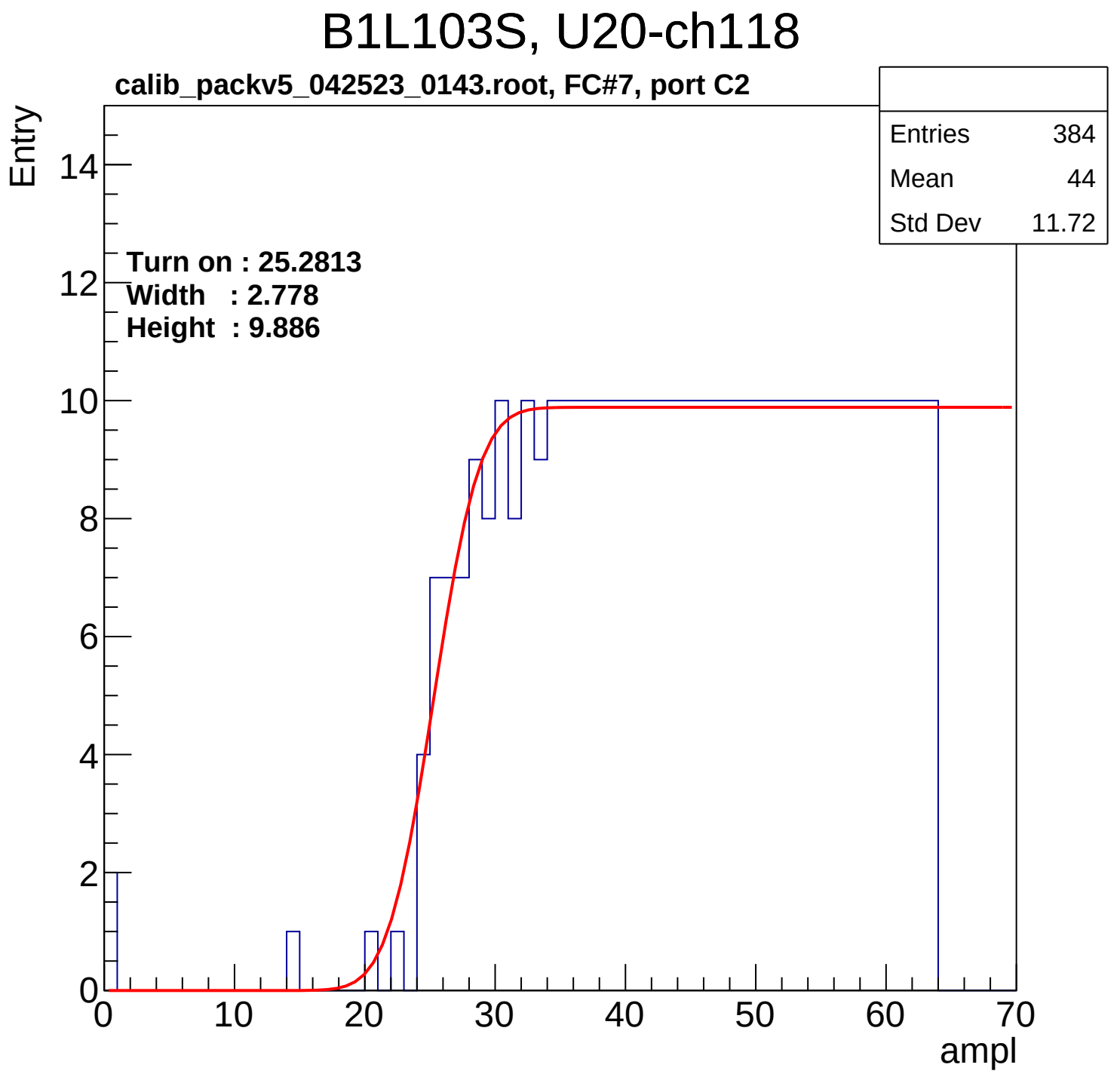
B1L103S, U20-ch118
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 44
Std Dev 11.72
Turn on : 25.2813
Width : 2.778
Height : 9.886
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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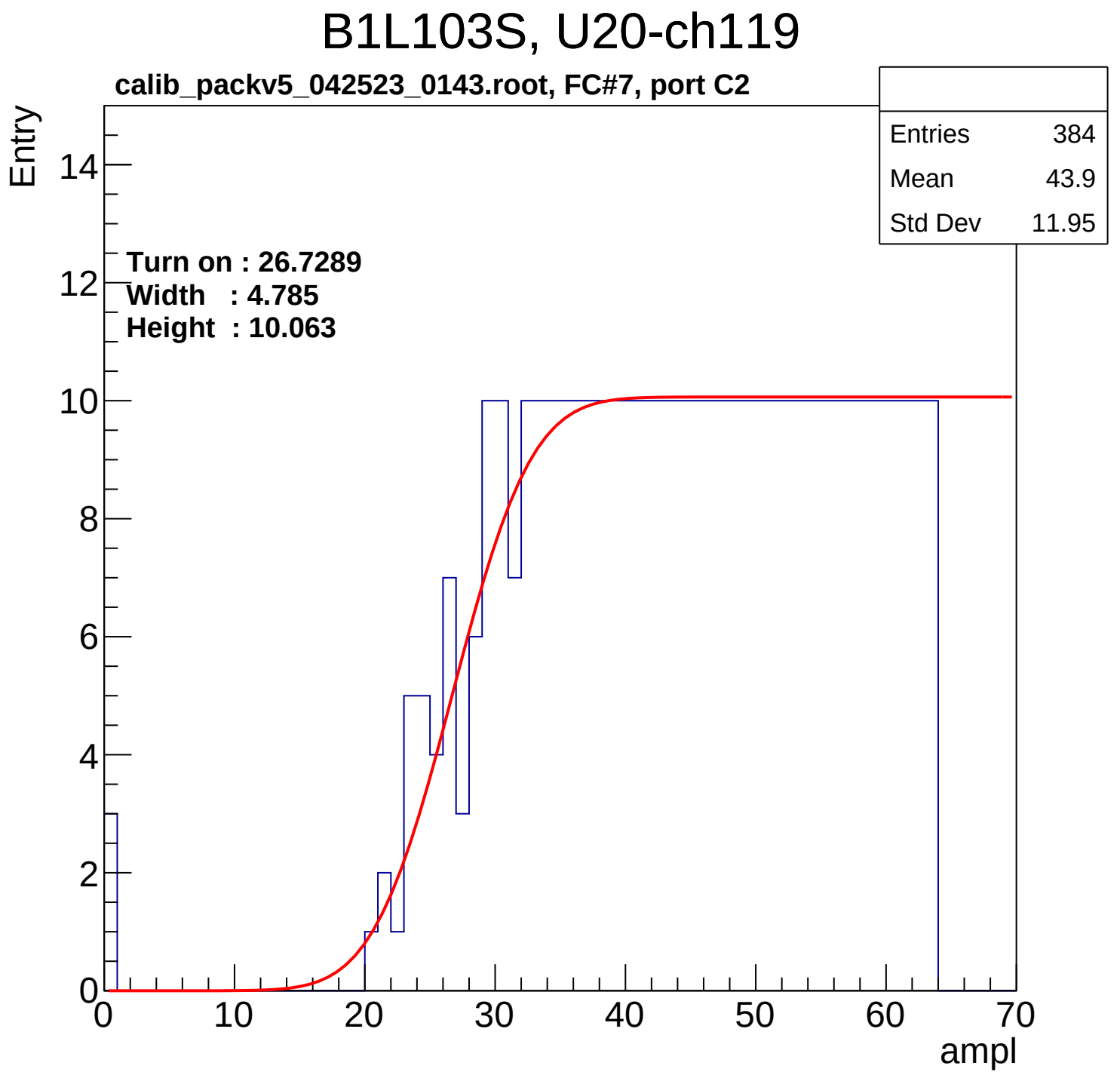
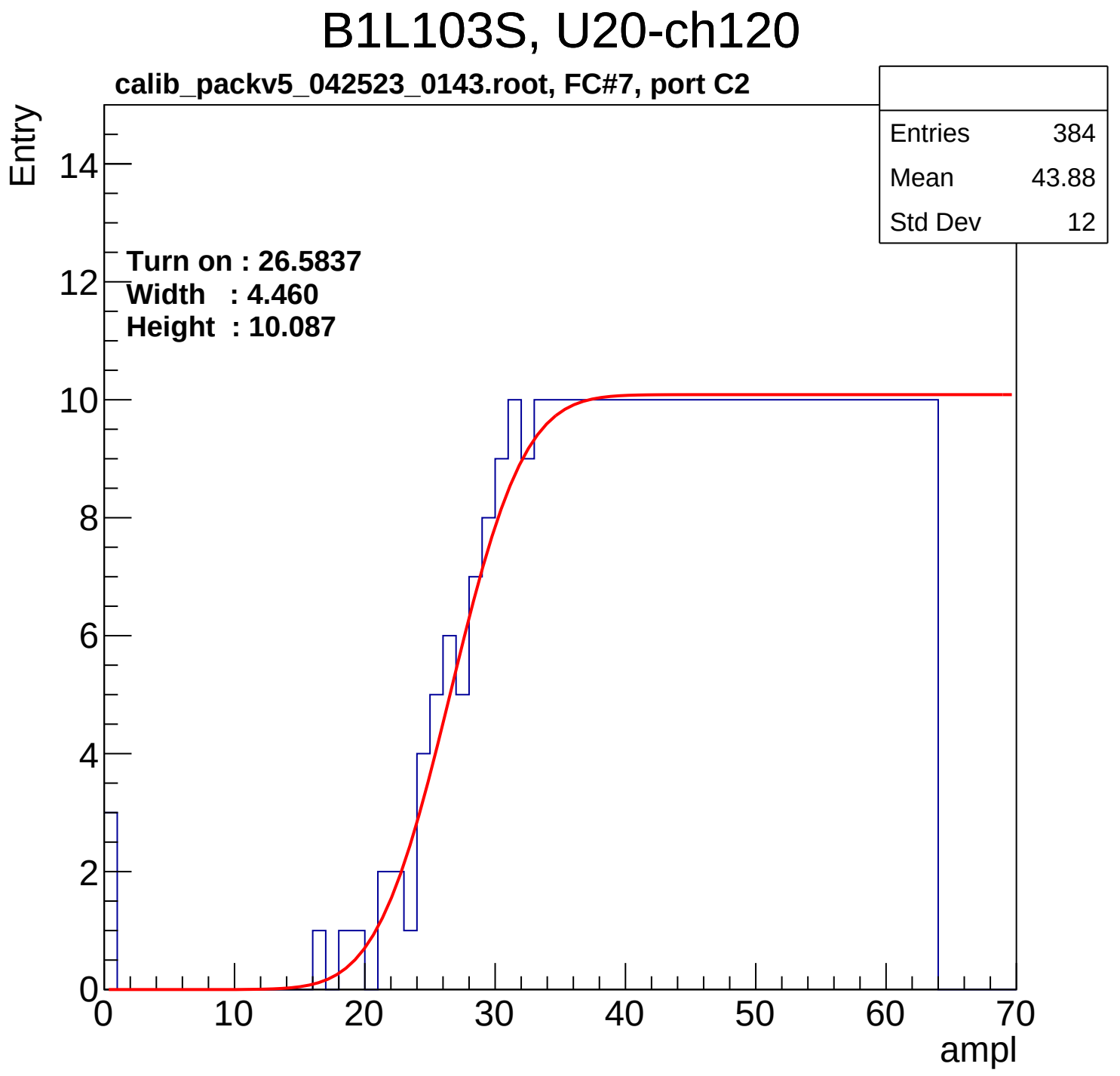

B1L103S, U20-ch119
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 43.9
Std Dev 11.95
Turn on : 26.7289
Width : 4.785
Height : 10.063
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U20-ch120
calib_packv5_042523_0143.root, FC#7, port C2
Entries 384
Mean 43.88
Std Dev 12
Turn on : 26.5837
Width : 4.460
Height : 10.087
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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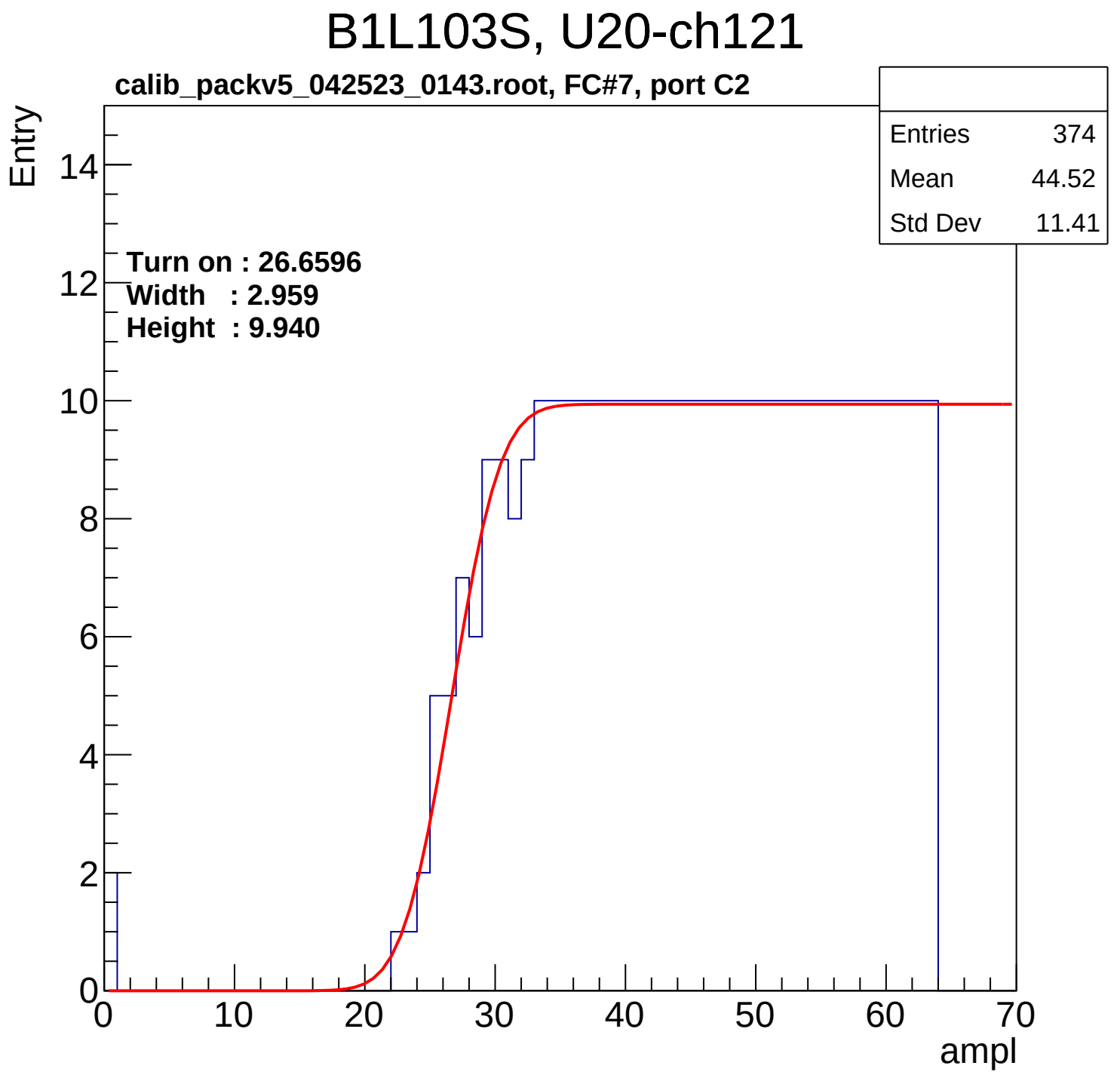
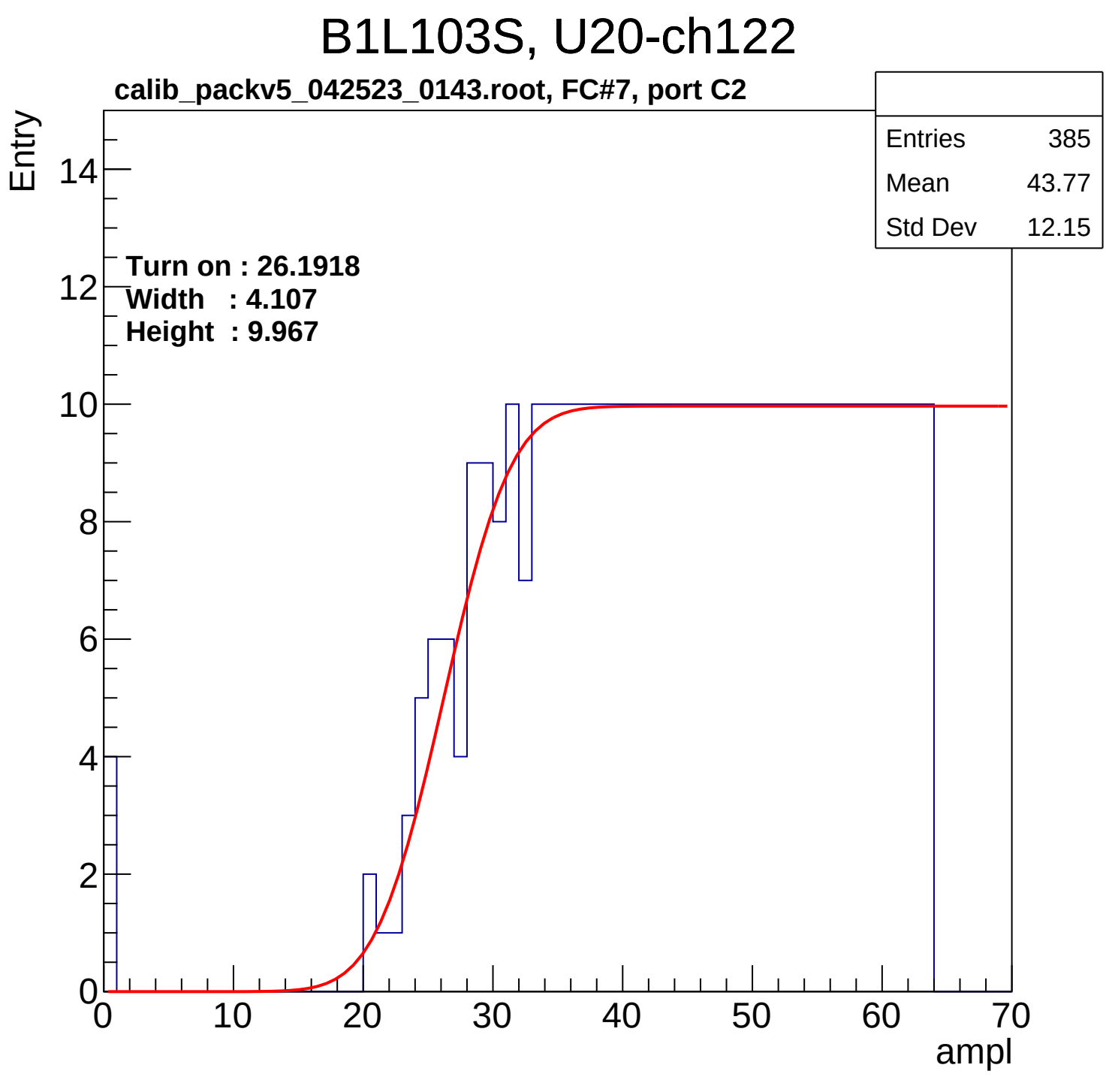
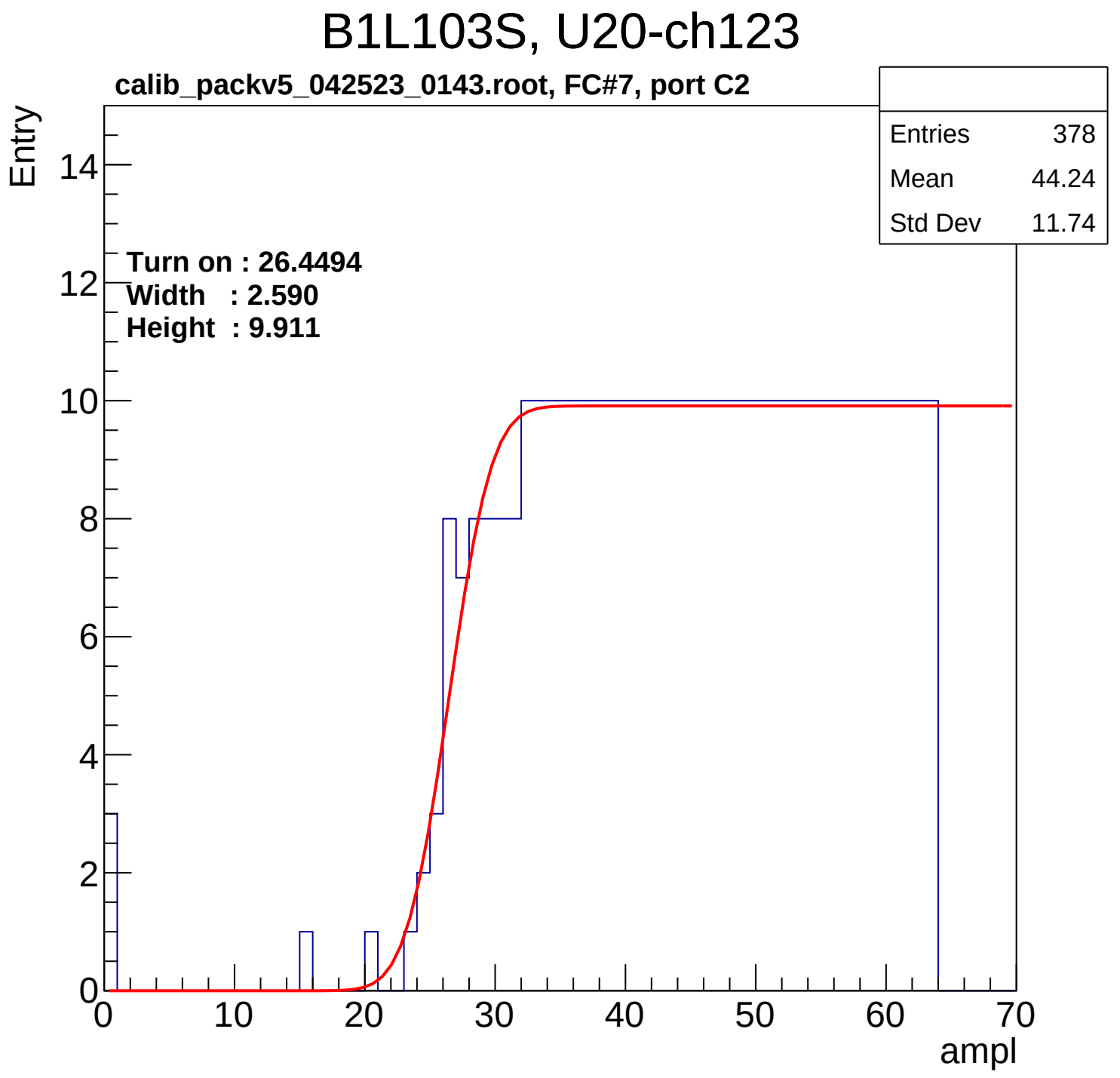
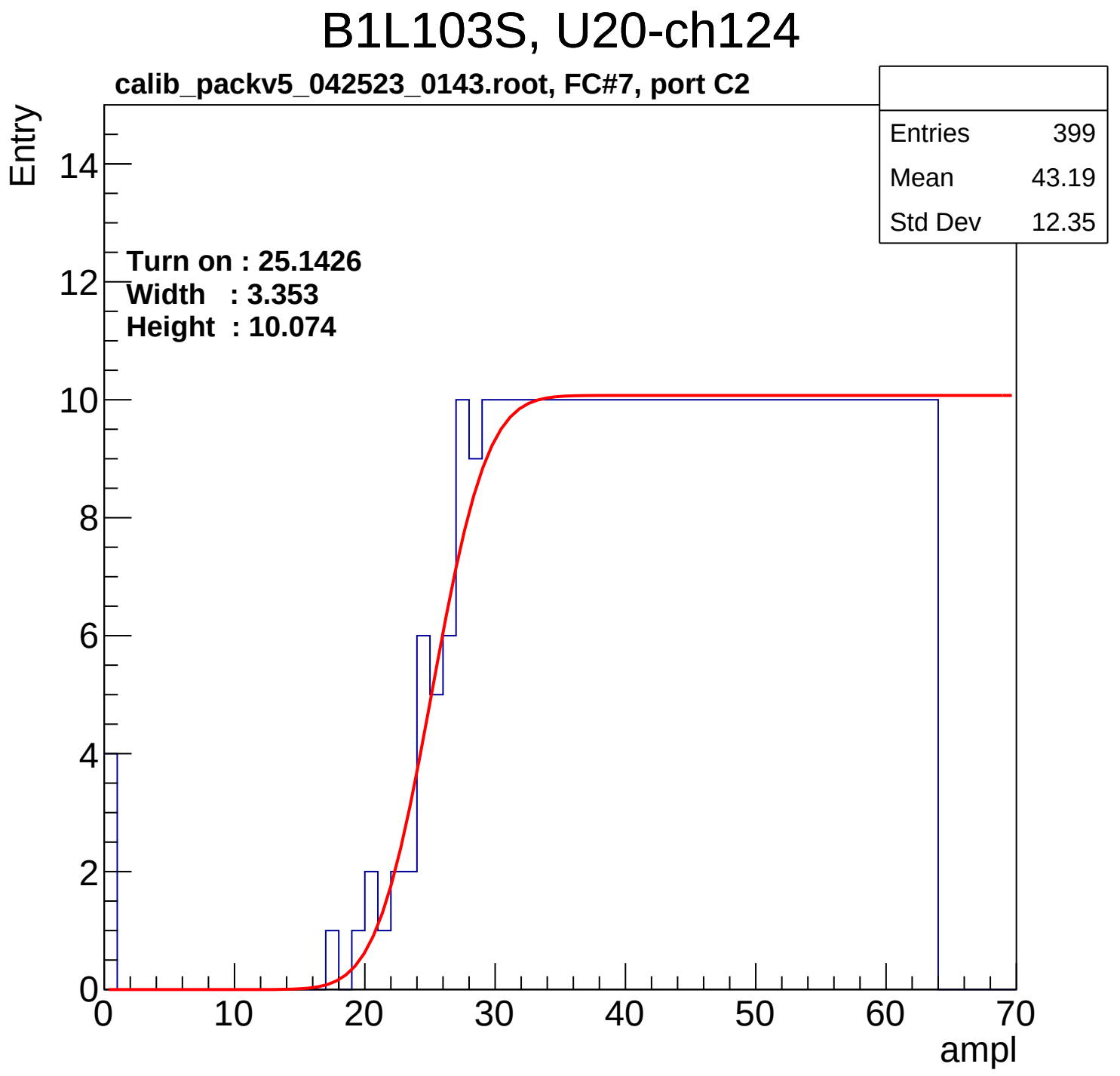

B1L103S, U20-ch121
calib_packv5_042523_0143.root, FC#7, port C2
Entries 374
Mean 44.52
Std Dev 11.41
Turn on : 26.6596
Width : 2.959
Height : 9.940
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U20-ch122
calib_packv5_042523_0143.root, FC#7, port C2
Entries 385
Mean 43.77
Std Dev 12.15
Turn on : 26.1918
Width : 4.107
Height : 9.967
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U20-ch123
calib_packv5_042523_0143.root, FC#7, port C2
Entries 378
Mean 44.24
Std Dev 11.74
Turn on : 26.4494
Width : 2.590
Height : 9.911
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U20-ch124
calib_packv5_042523_0143.root, FC#7, port C2
Entries 399
Mean 43.19
Std Dev 12.35
Turn on : 25.1426
Width : 3.353
Height : 10.074
Entry
ampl
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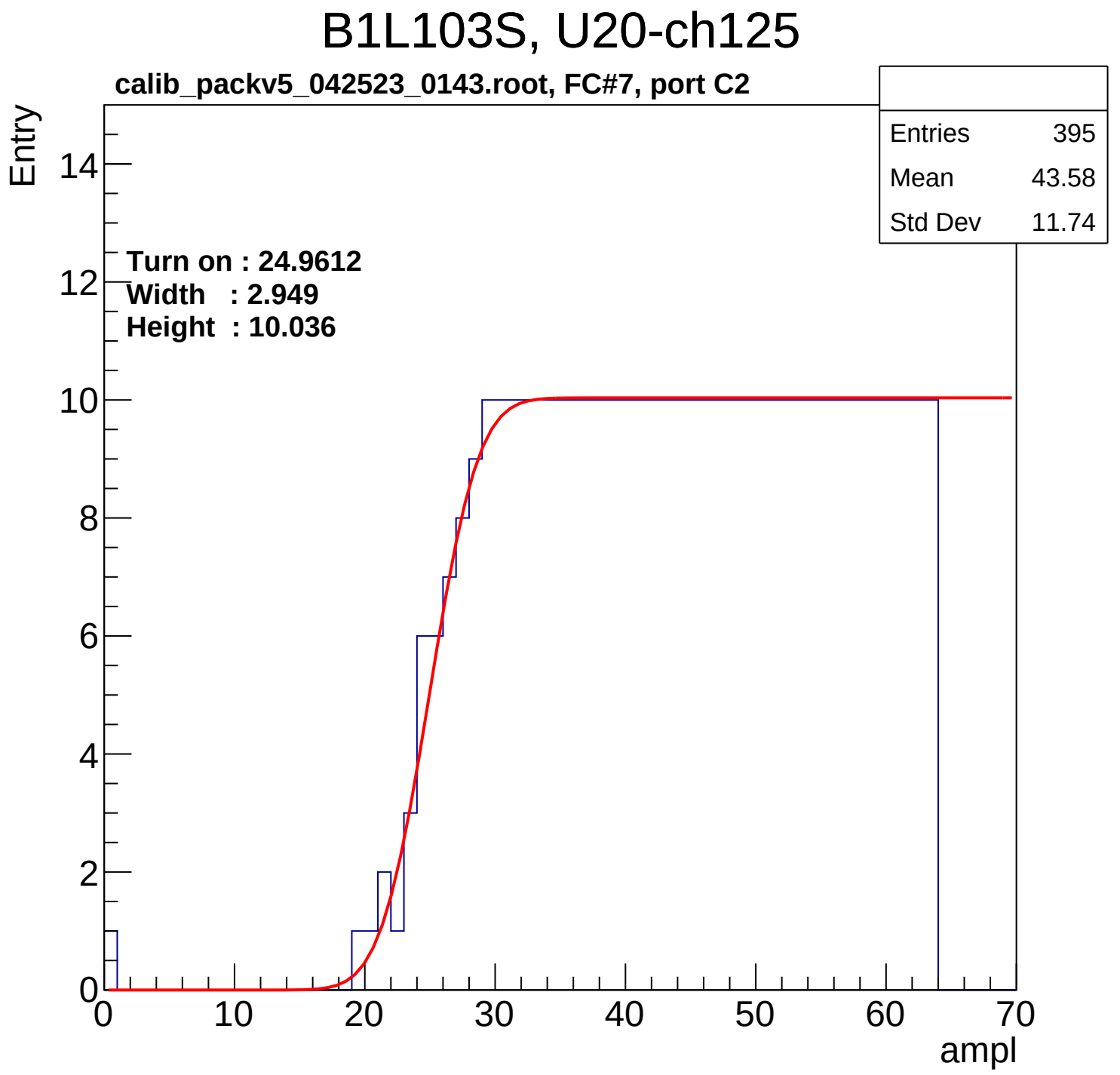
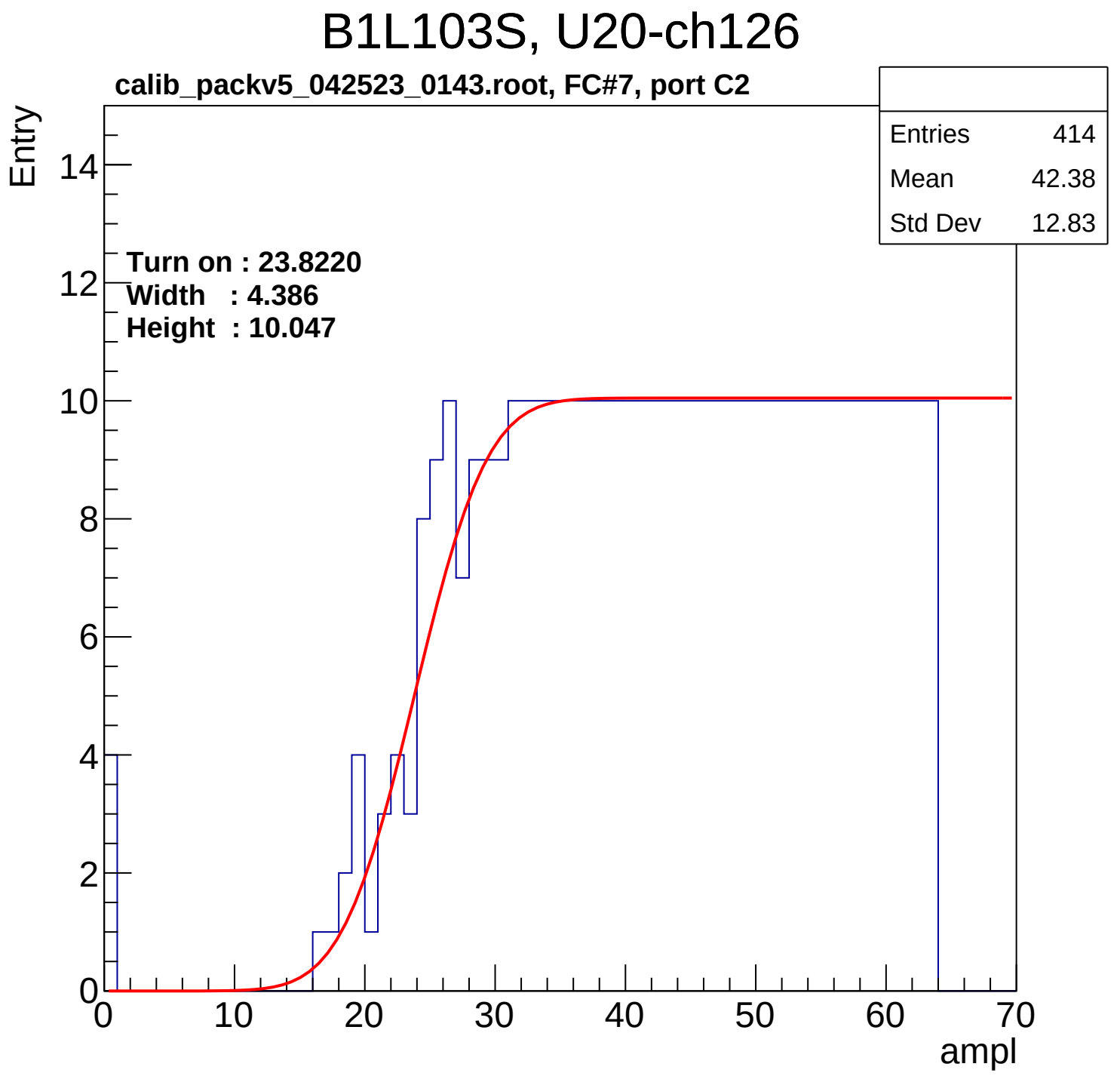
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U20-ch125
calib_packv5_042523_0143.root, FC#7, port C2
Entries 395
Mean 43.58
Std Dev 11.74
Turn on : 24.9612
Width : 2.949
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U20-ch126
calib_packv5_042523_0143.root, FC#7, port C2
Entries 414
Mean 42.38
Std Dev 12.83
Turn on : 23.8220
Width : 4.386
Height : 10.047
Entry
ampl
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4
6
8
10
12
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0
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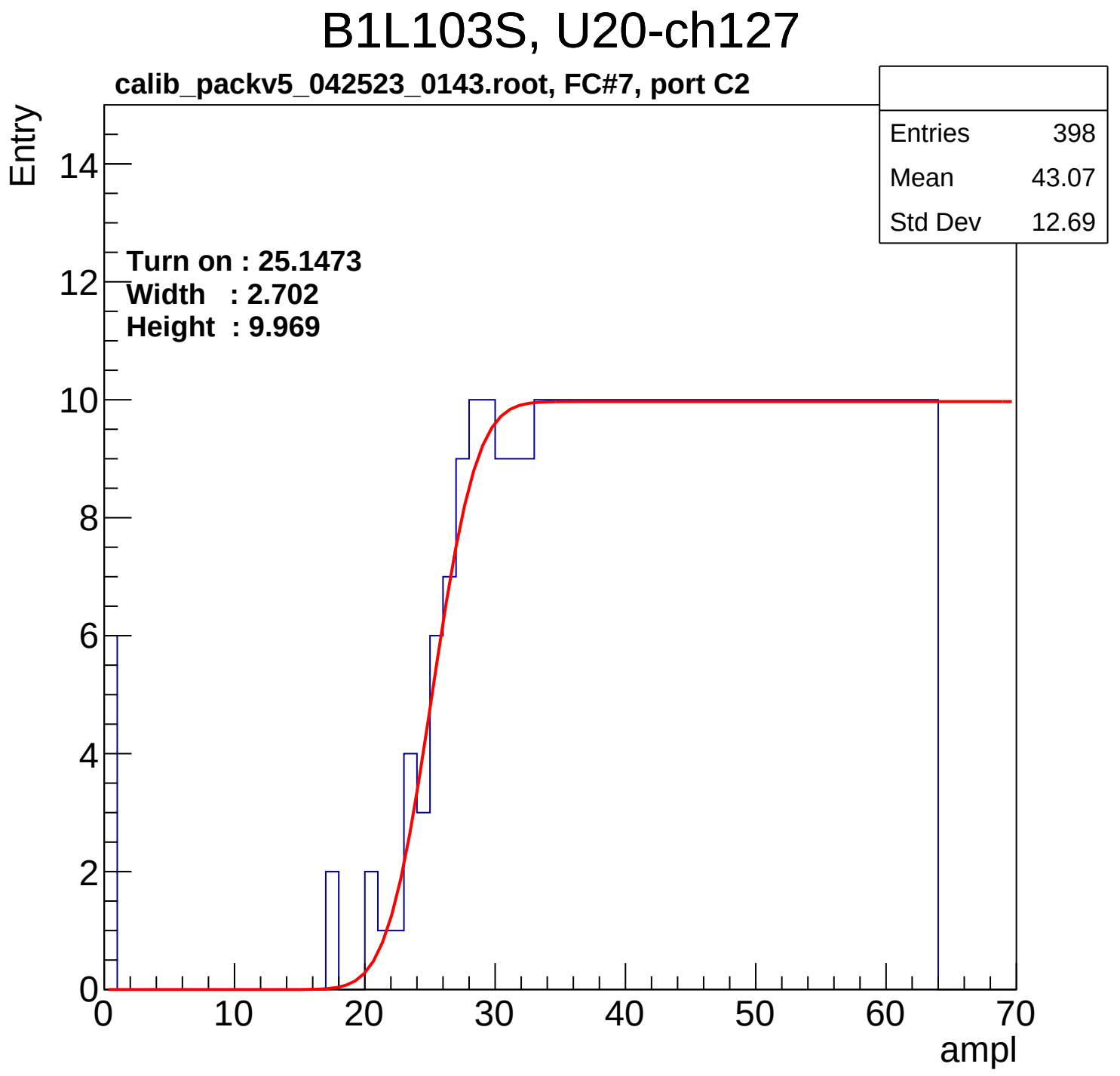
B1L103S, U20-ch127
calib_packv5_042523_0143.root, FC#7, port C2
Entries 398
Mean 43.07
Std Dev 12.69
Turn on : 25.1473
Width : 2.702
Height : 9.969
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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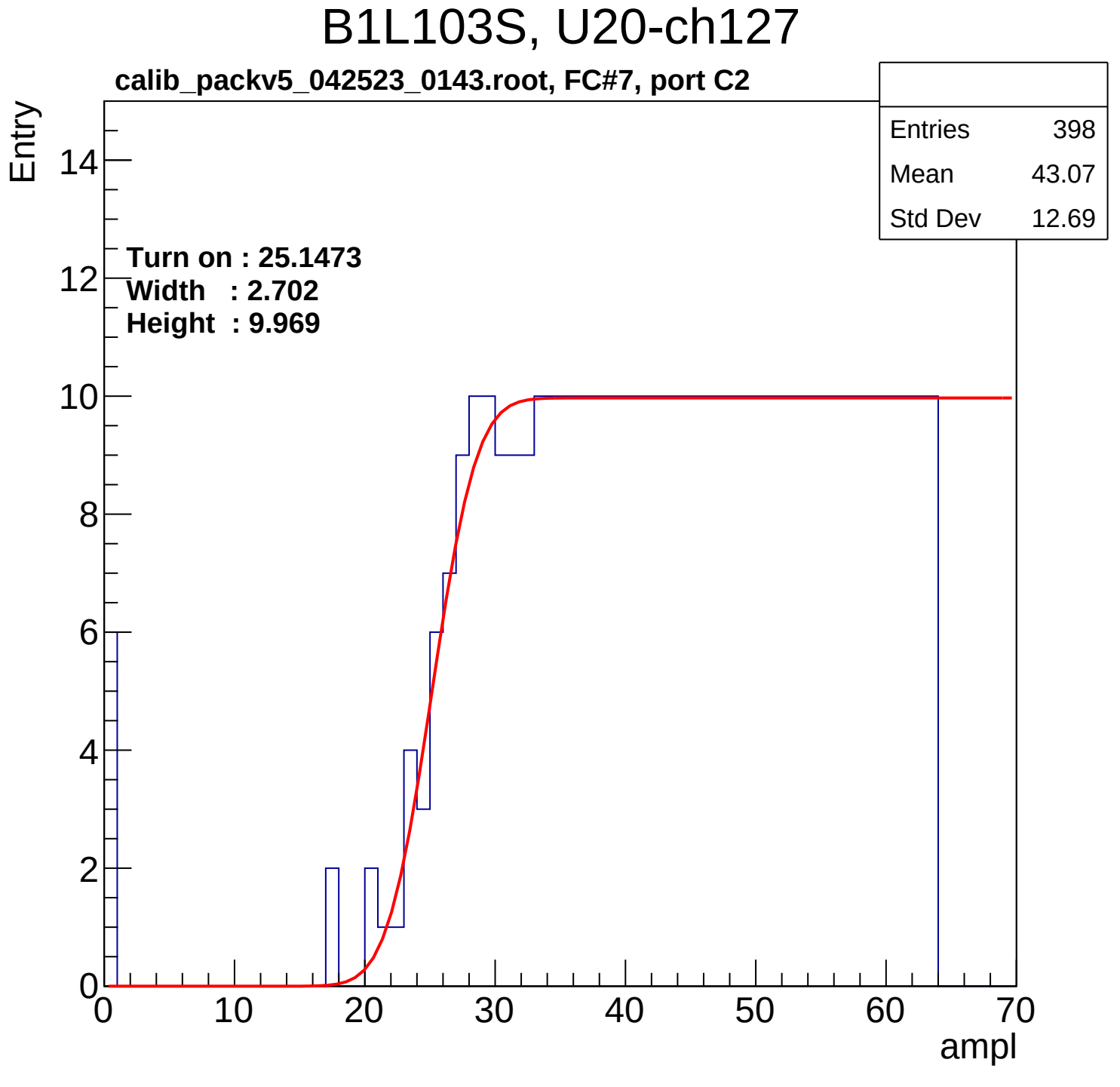
B1L103S, U20-ch127
calib_packv5_042523_0143.root, FC#7, port C2
Entries 398
Mean 43.07
Std Dev 12.69
Turn on : 25.1473
Width : 2.702
Height : 9.969
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
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70