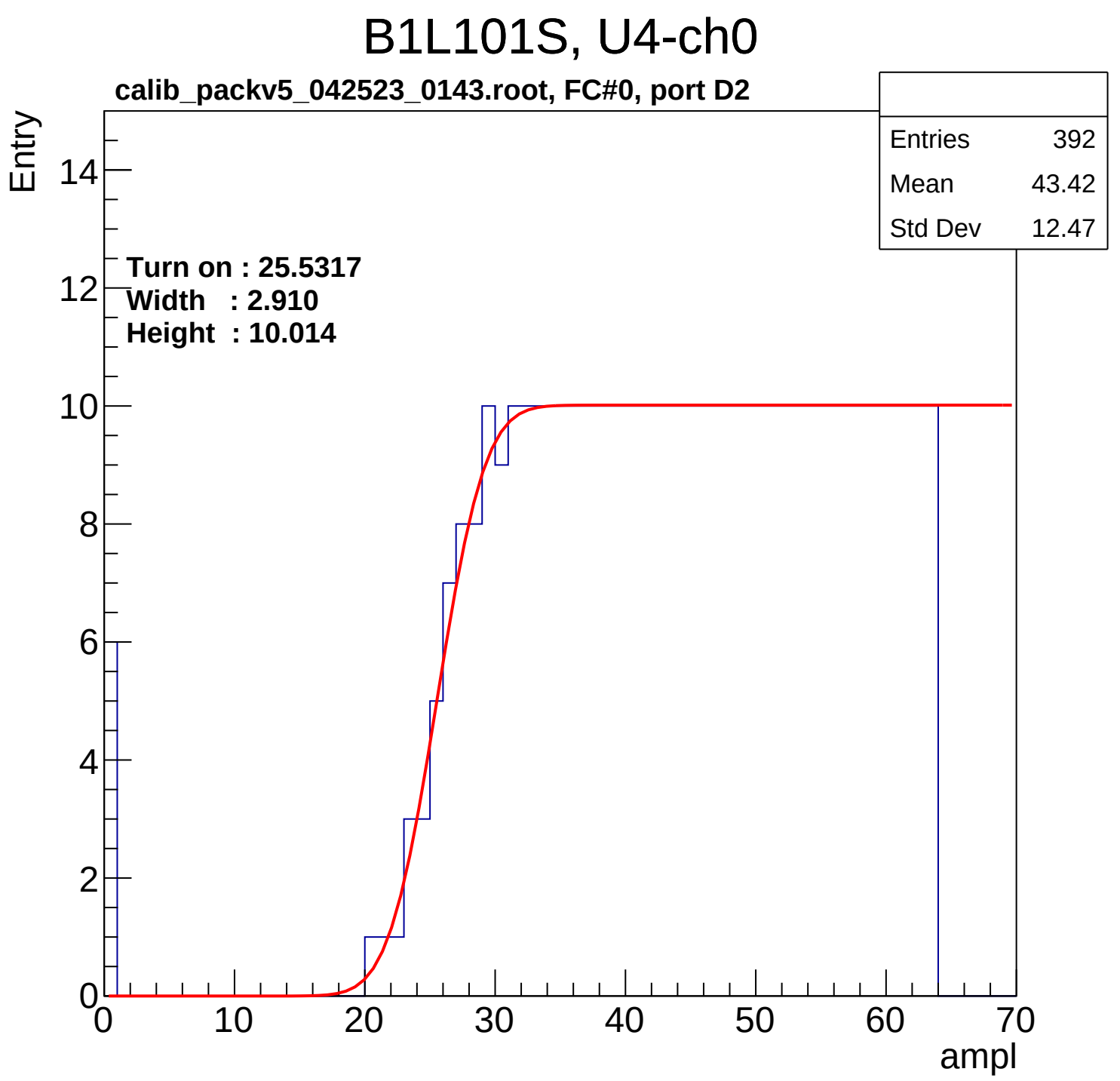
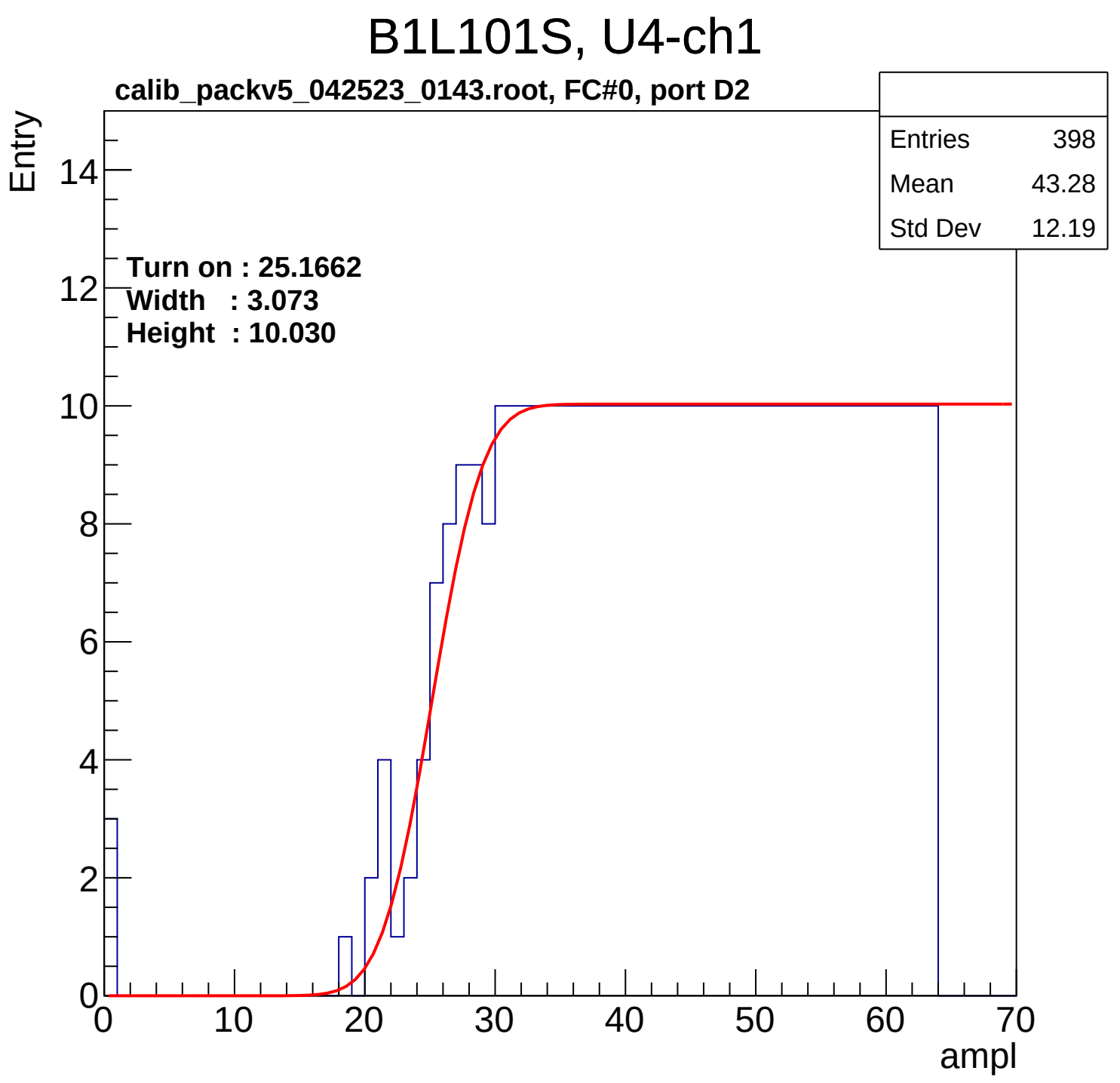
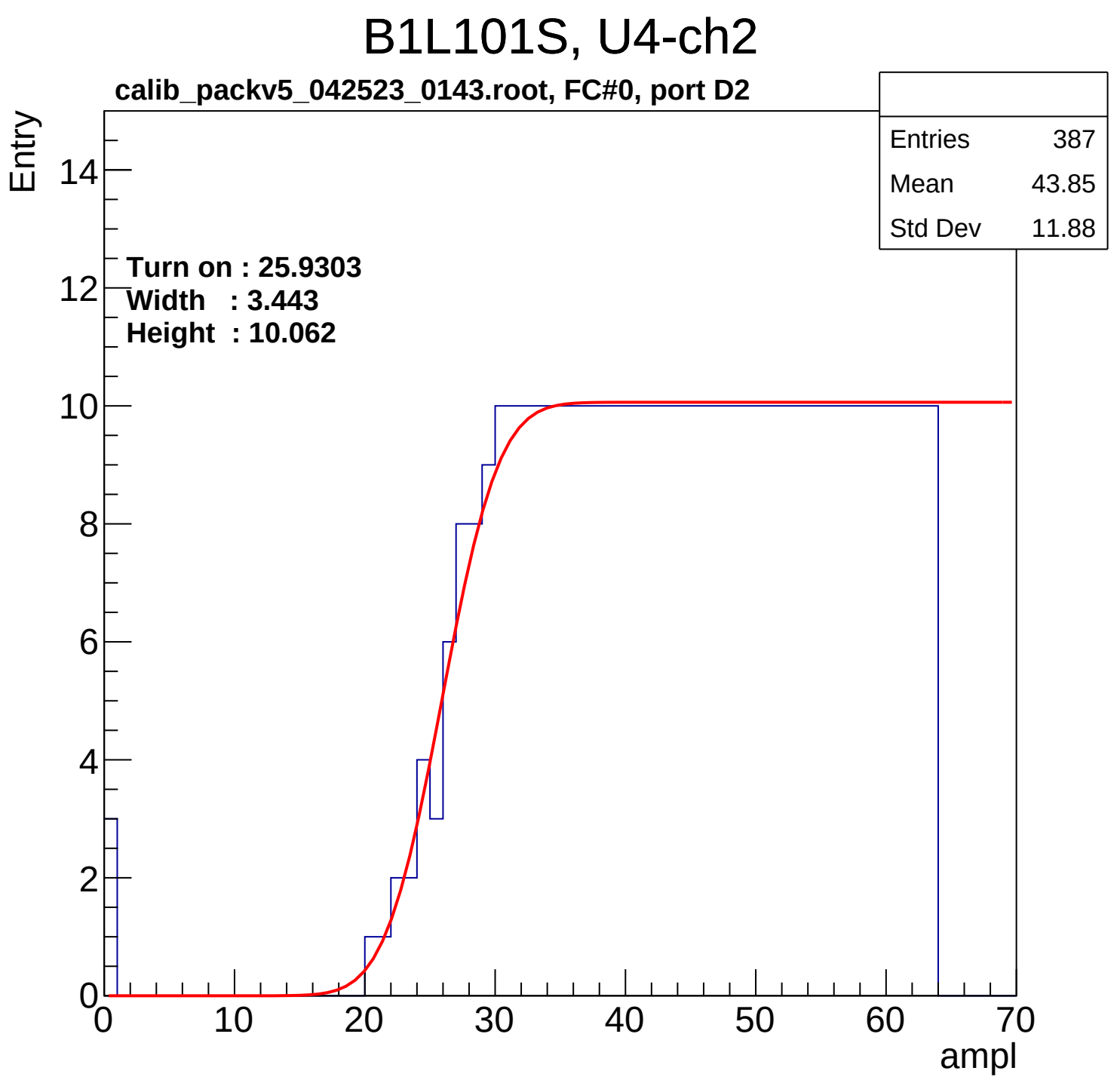
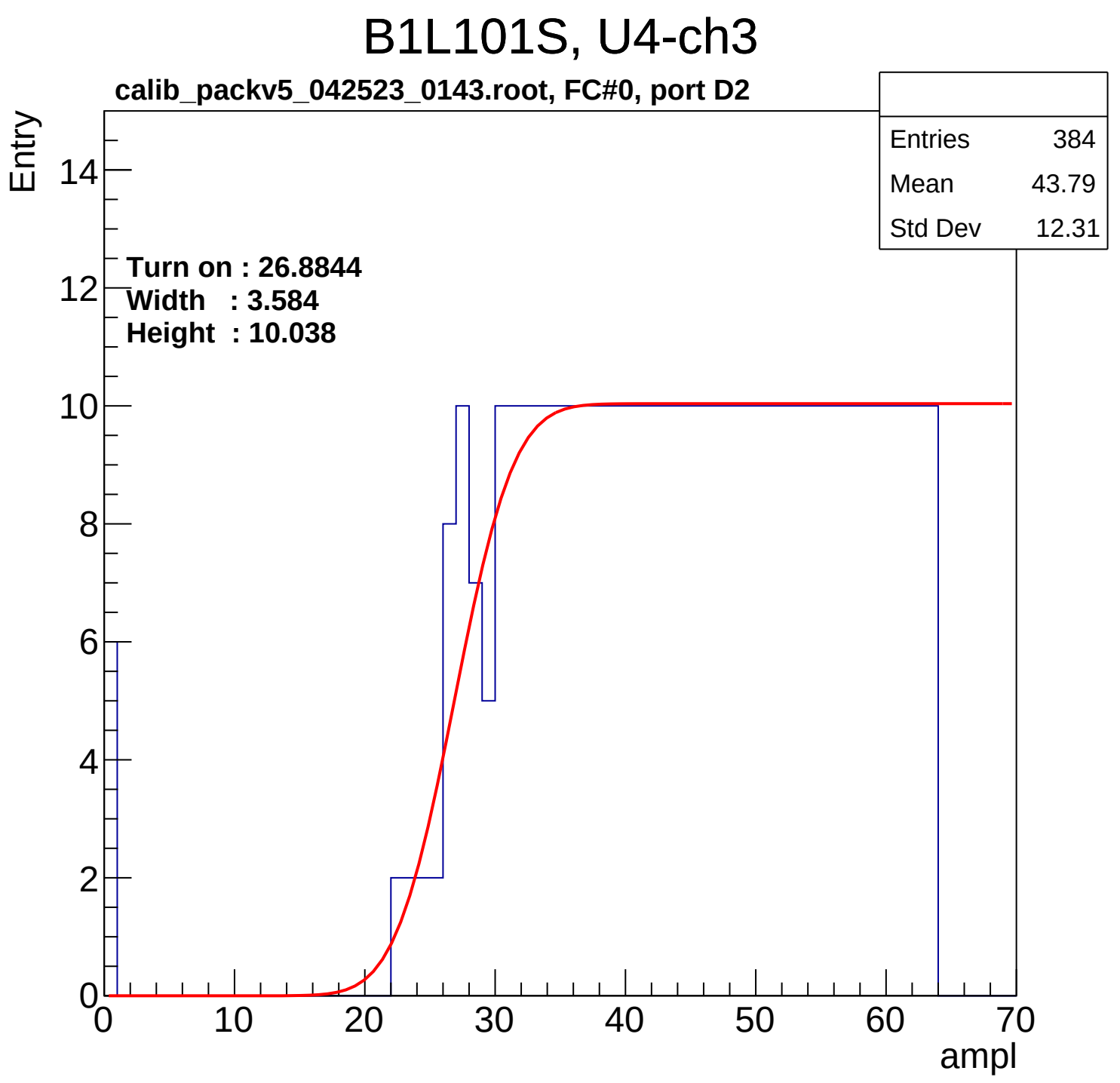
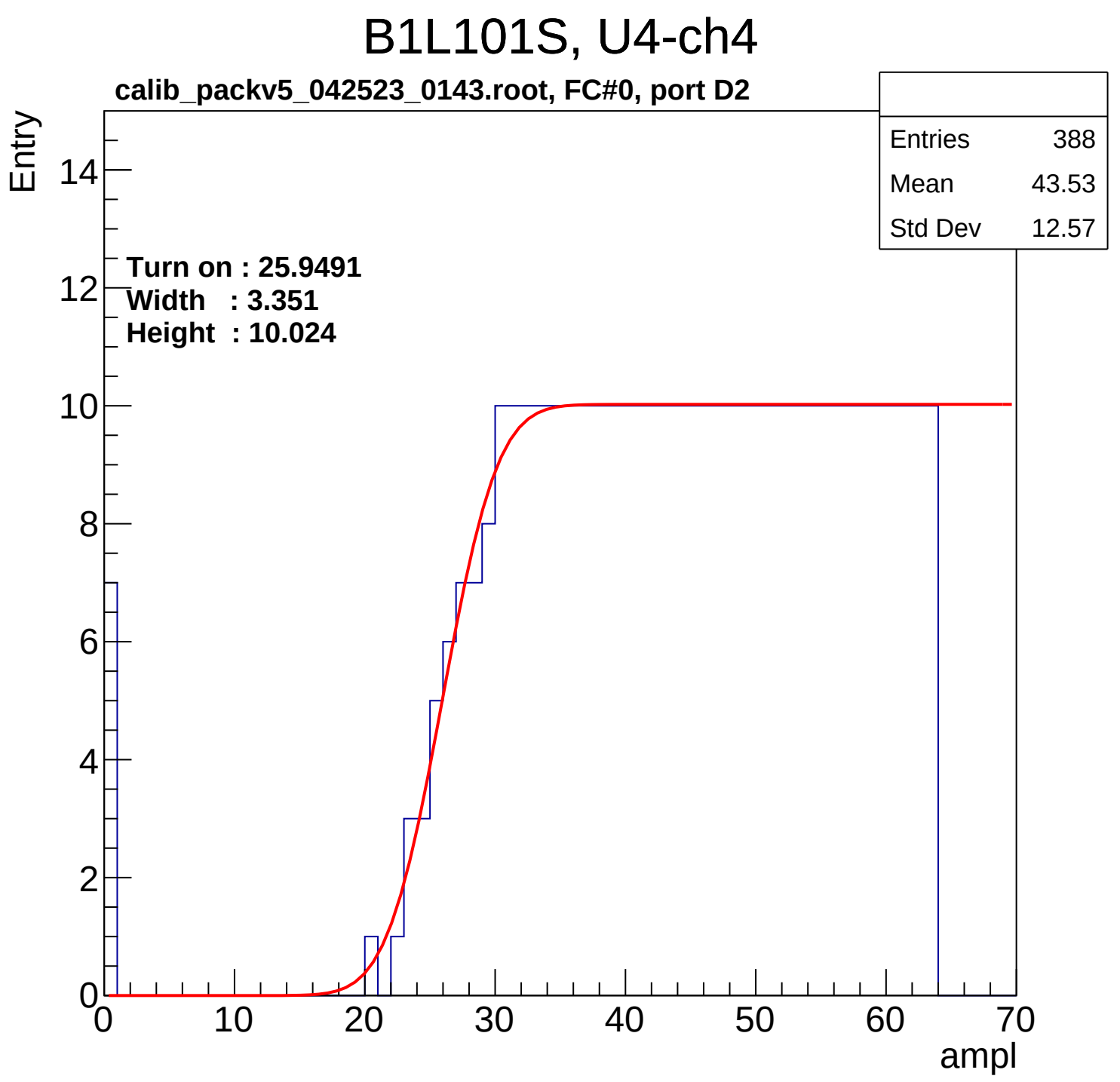
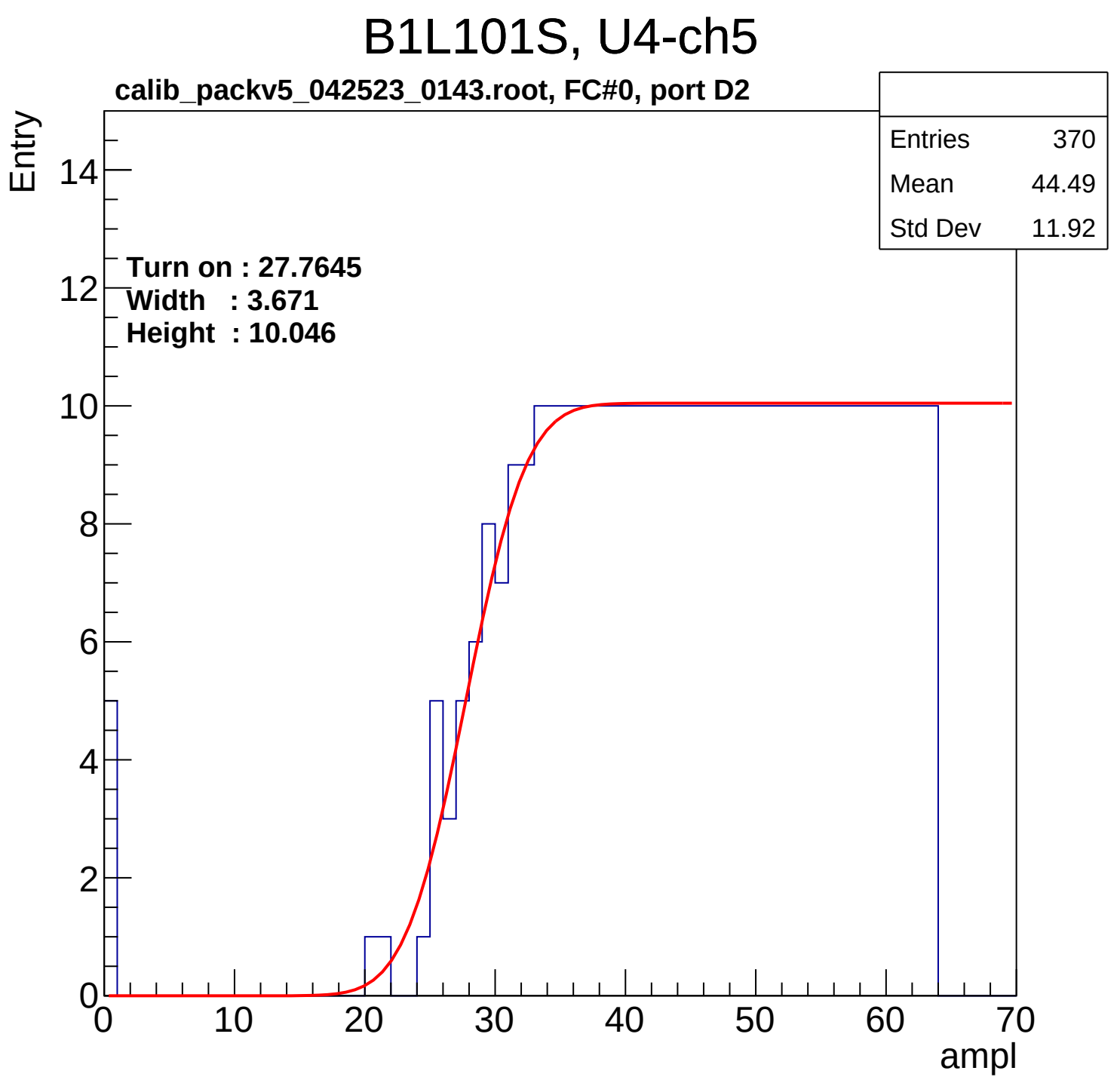

B1L101S, U4-ch0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 392
Mean 43.42
Std Dev 12.47
Turn on : 25.5317
Width : 2.910
Height : 10.014
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

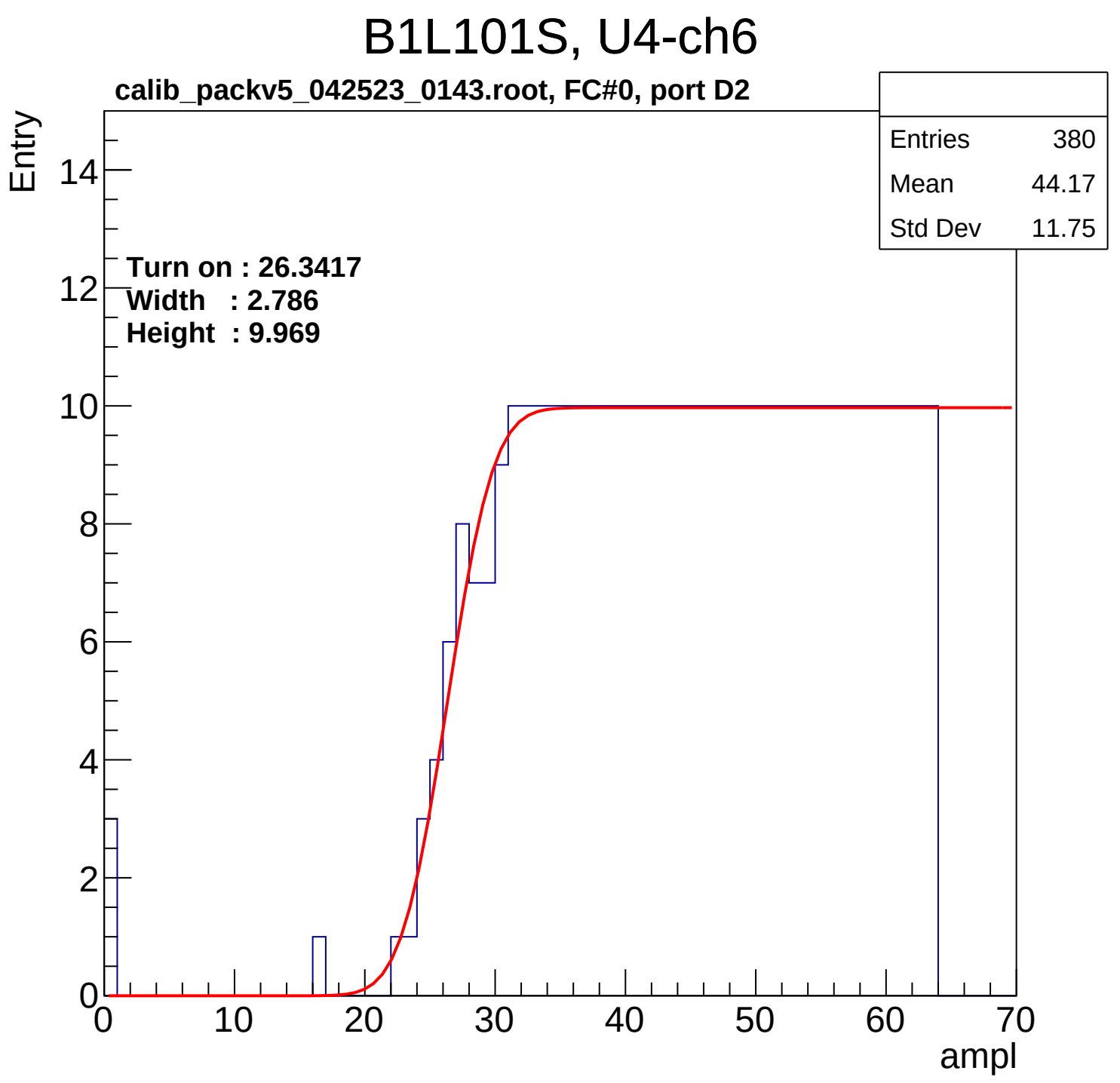

B1L101S, U4-ch1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 398
Mean 43.28
Std Dev 12.19
Turn on : 25.1662
Width : 3.073
Height : 10.030
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

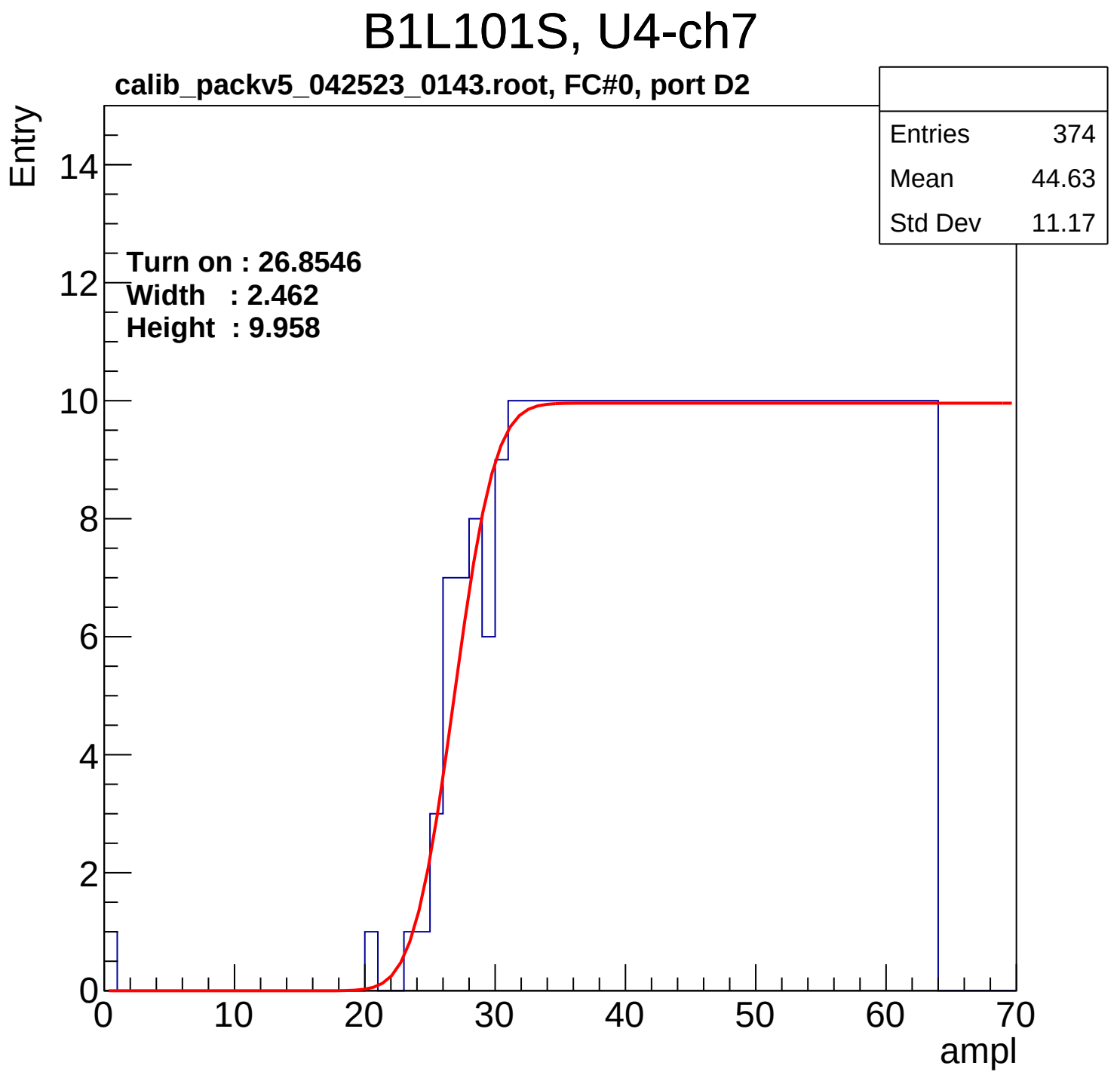

B1L101S, U4-ch2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.85
Std Dev 11.88
Turn on : 25.9303
Width : 3.443
Height : 10.062
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

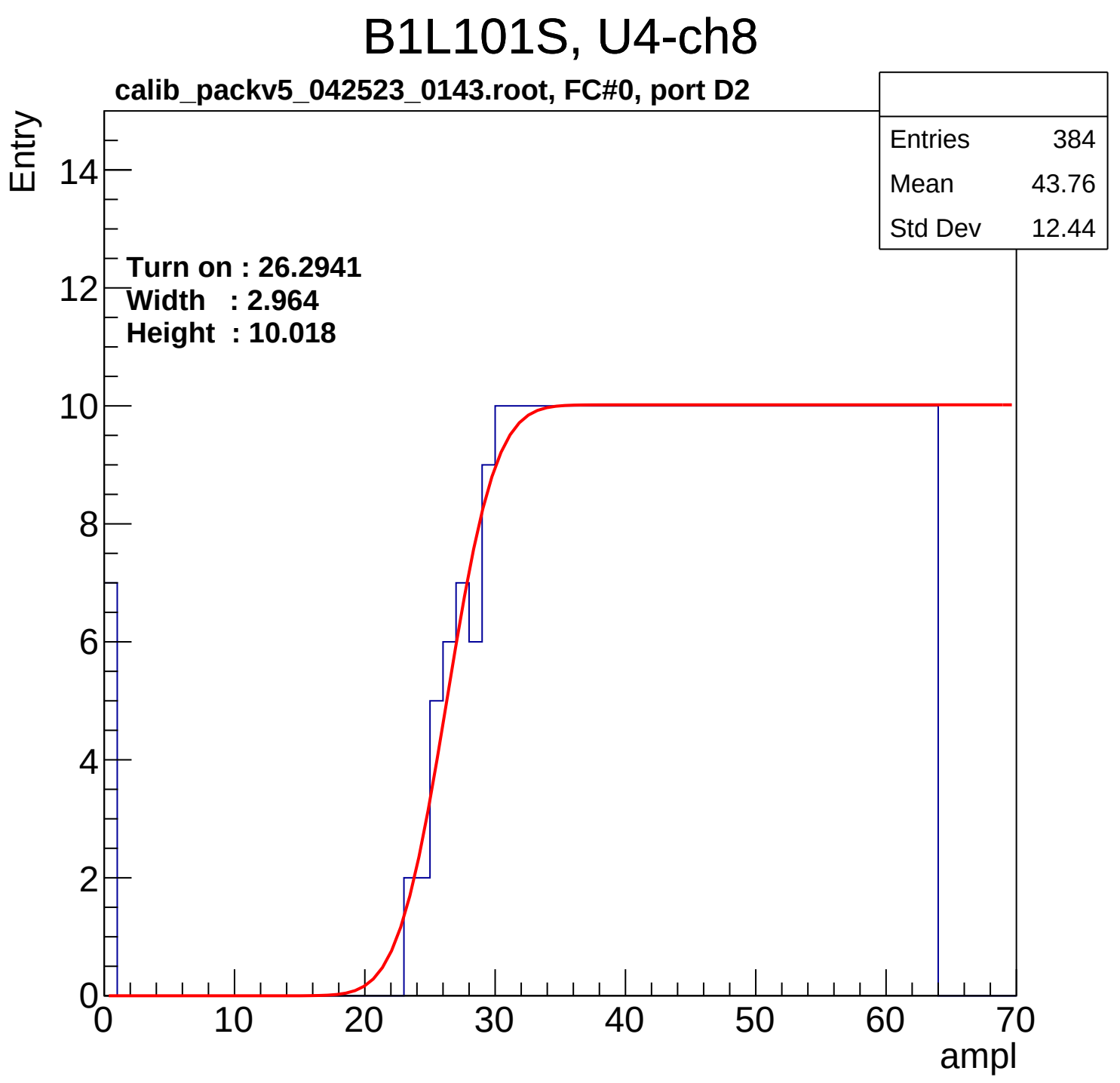

B1L101S, U4-ch3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 384
Mean 43.79
Std Dev 12.31
Turn on : 26.8844
Width : 3.584
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

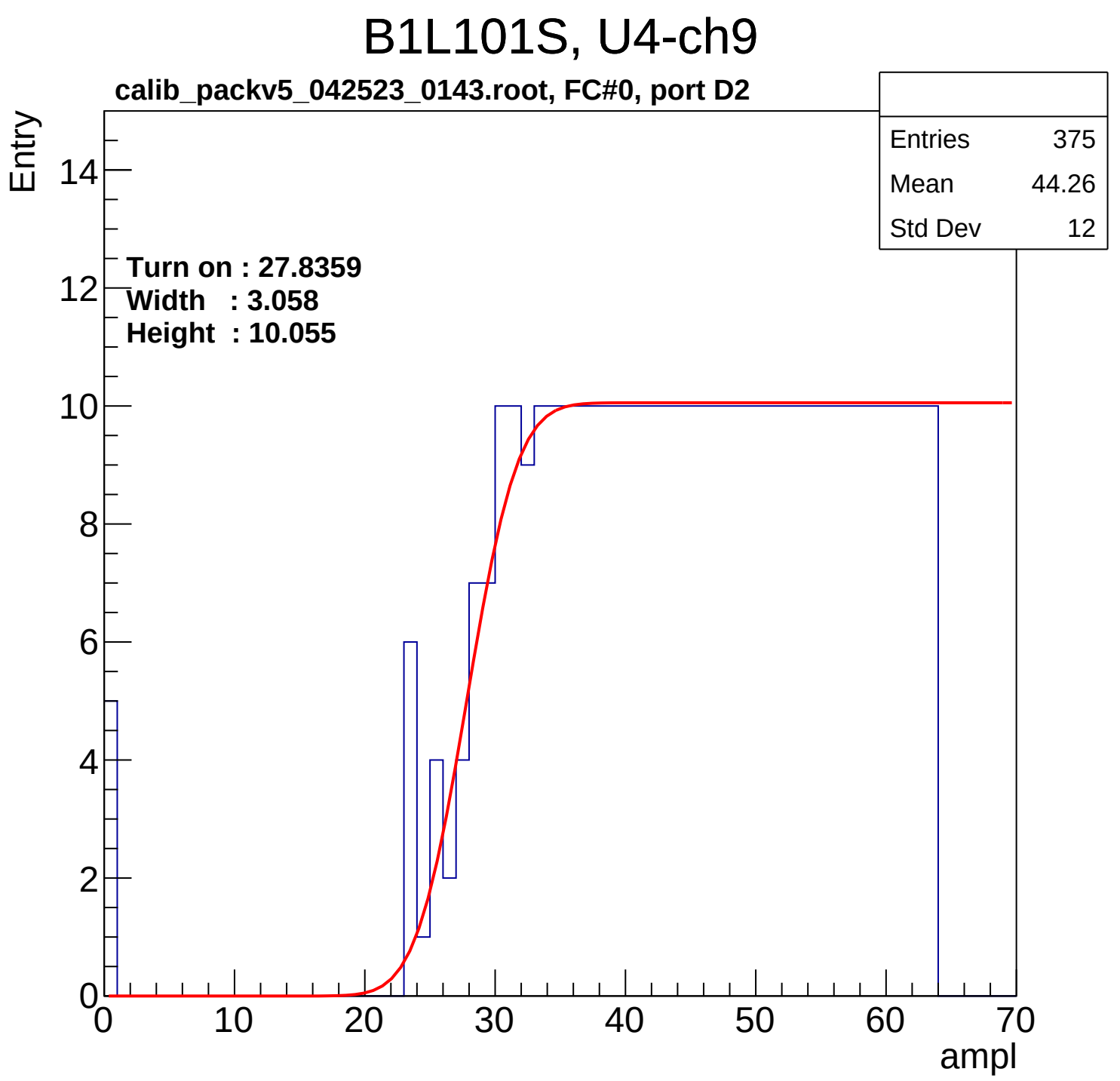

B1L101S, U4-ch4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 388
Mean 43.53
Std Dev 12.57
Turn on : 25.9491
Width : 3.351
Height : 10.024
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

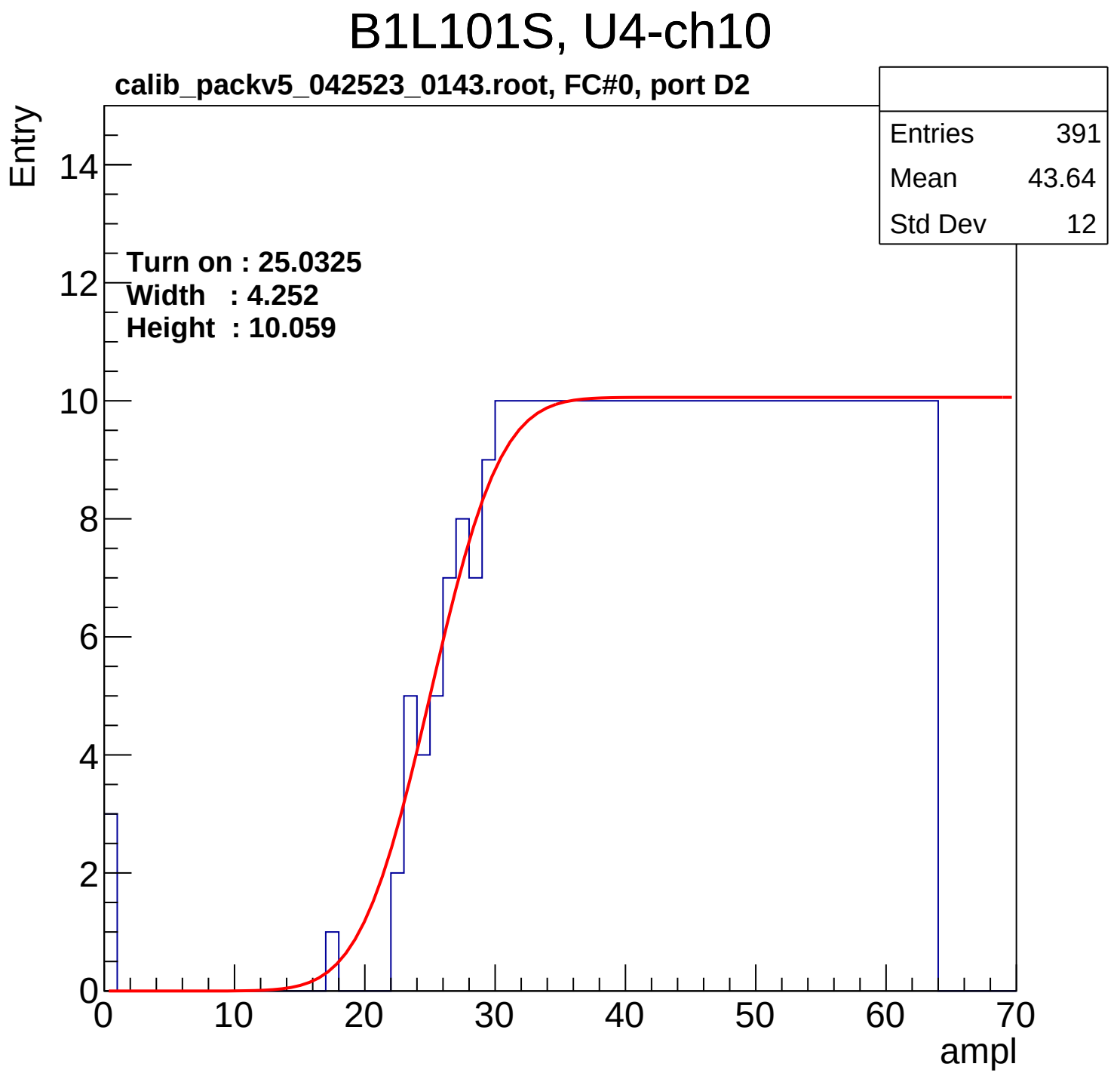

B1L101S, U4-ch5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.49
Std Dev 11.92
Turn on : 27.7645
Width : 3.671
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

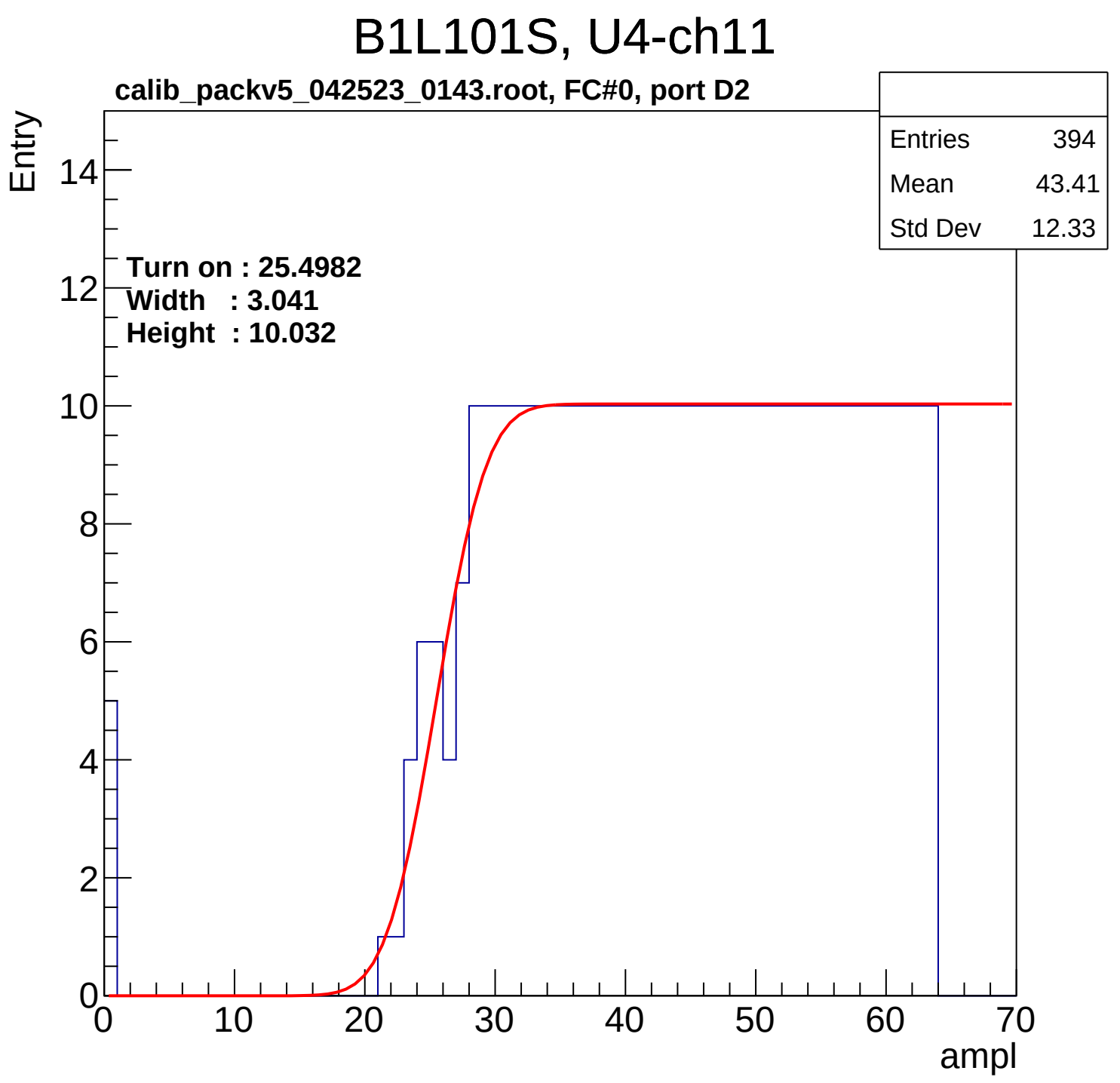

B1L101S, U4-ch6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 380
Mean 44.17
Std Dev 11.75
Turn on : 26.3417
Width : 2.786
Height : 9.969
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

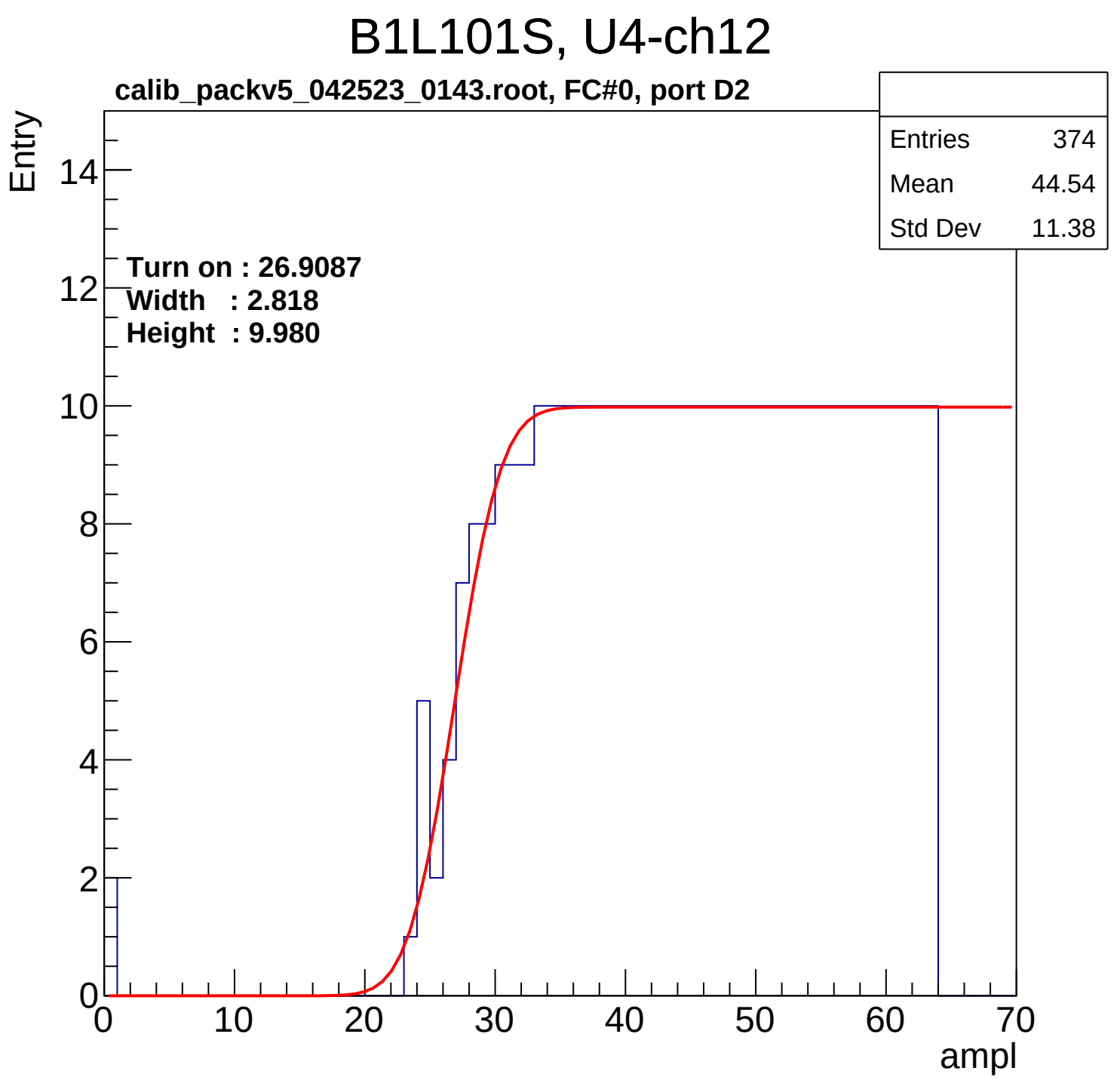

B1L101S, U4-ch7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.63
Std Dev 11.17
Turn on : 26.8546
Width : 2.462
Height : 9.958
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

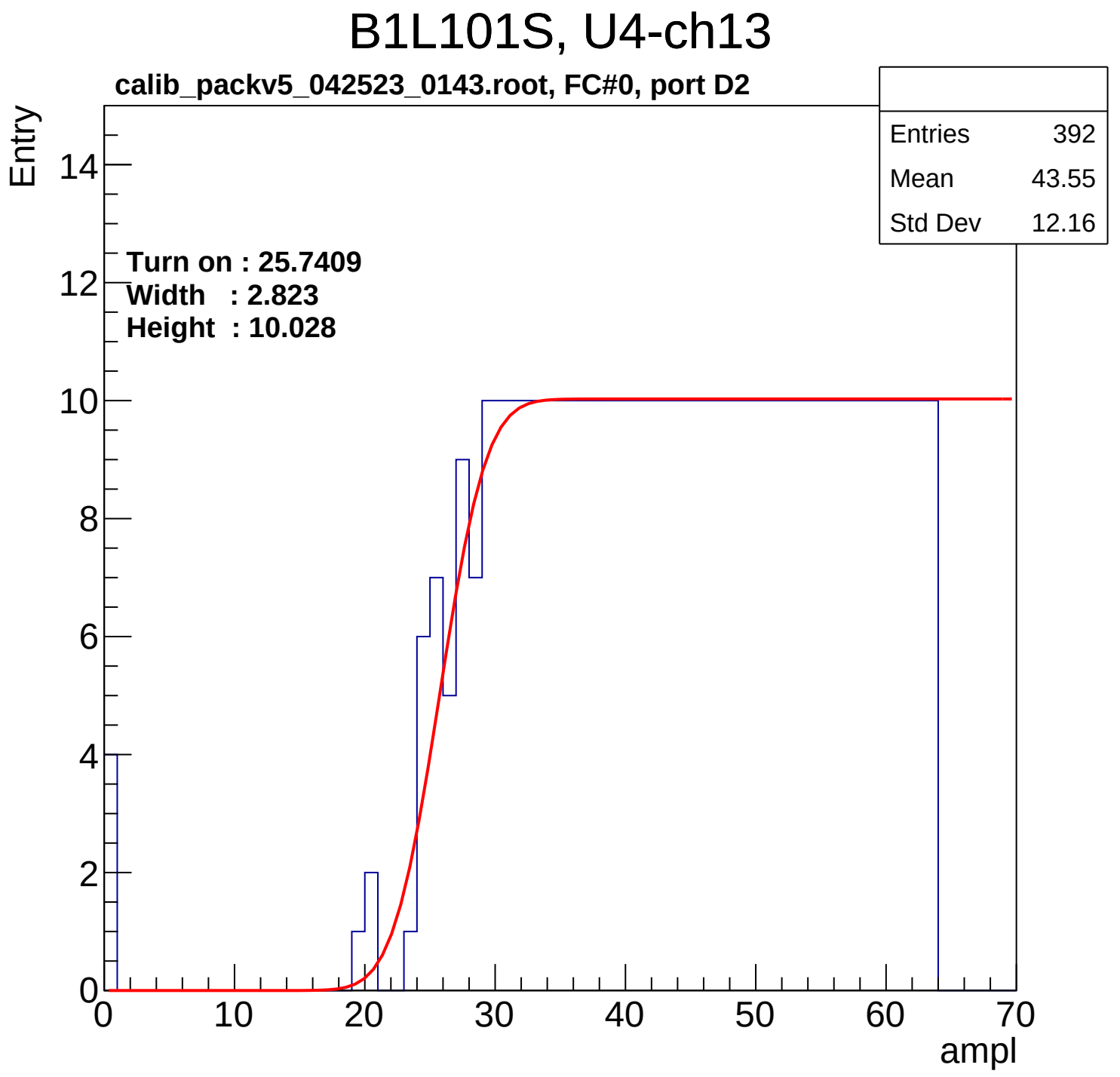

B1L101S, U4-ch8
calib_packv5_042523_0143.root, FC#0, port D2
Entries 384
Mean 43.76
Std Dev 12.44
Turn on : 26.2941
Width : 2.964
Height : 10.018
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

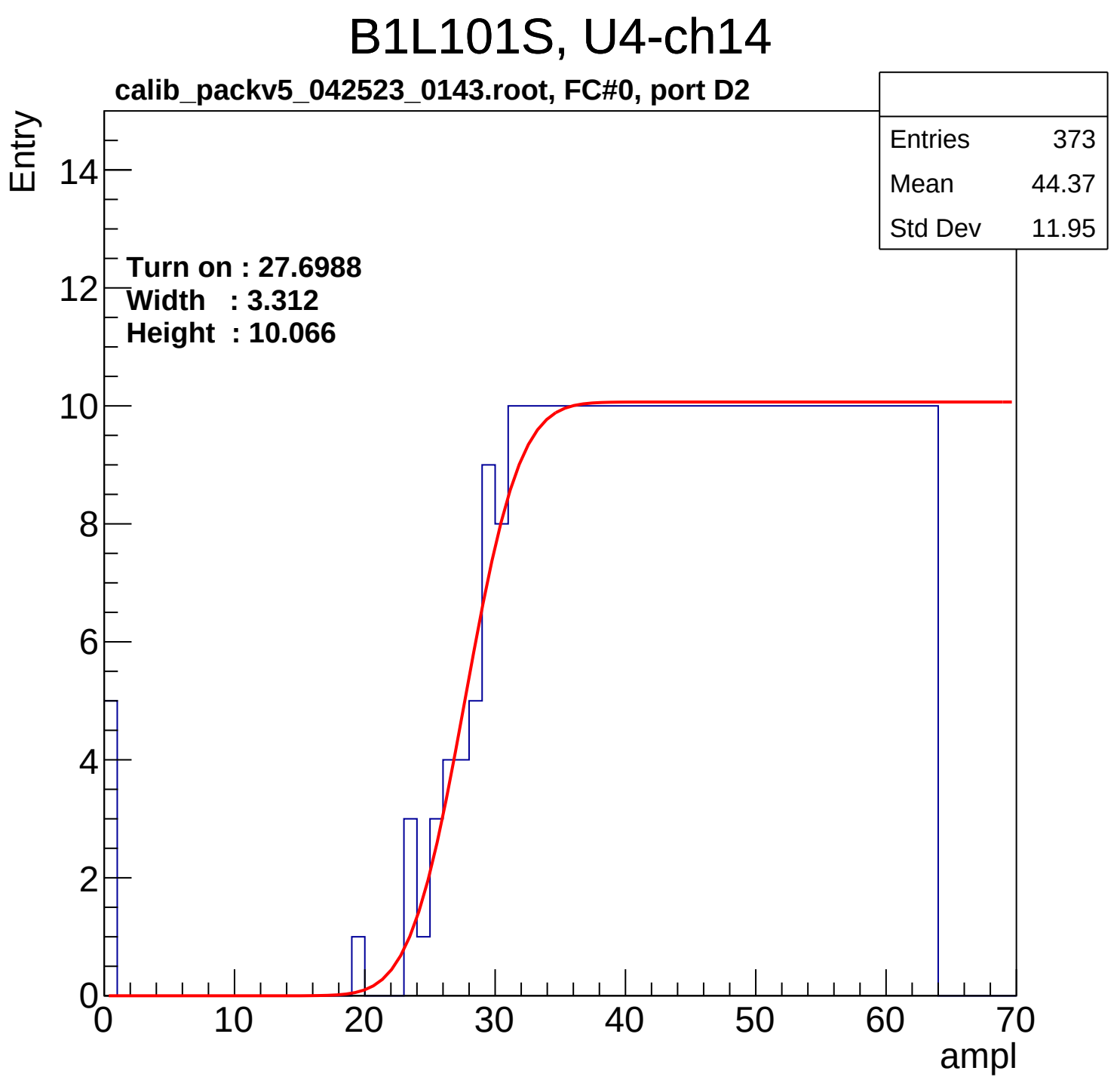

B1L101S, U4-ch9
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.26
Std Dev 12
Turn on : 27.8359
Width : 3.058
Height : 10.055
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

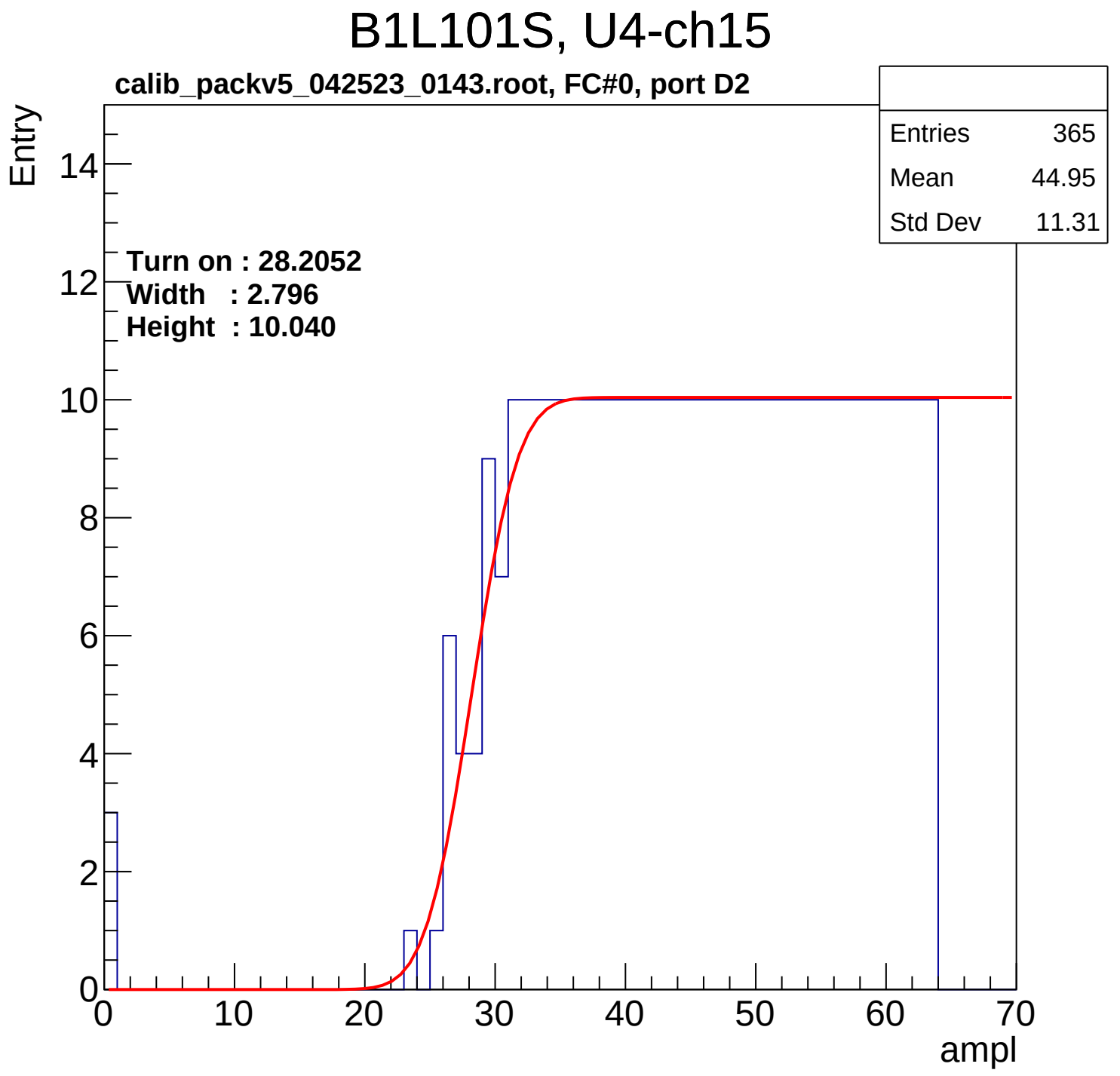

B1L101S, U4-ch10
calib_packv5_042523_0143.root, FC#0, port D2
Entries 391
Mean 43.64
Std Dev 12
Turn on : 25.0325
Width : 4.252
Height : 10.059
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

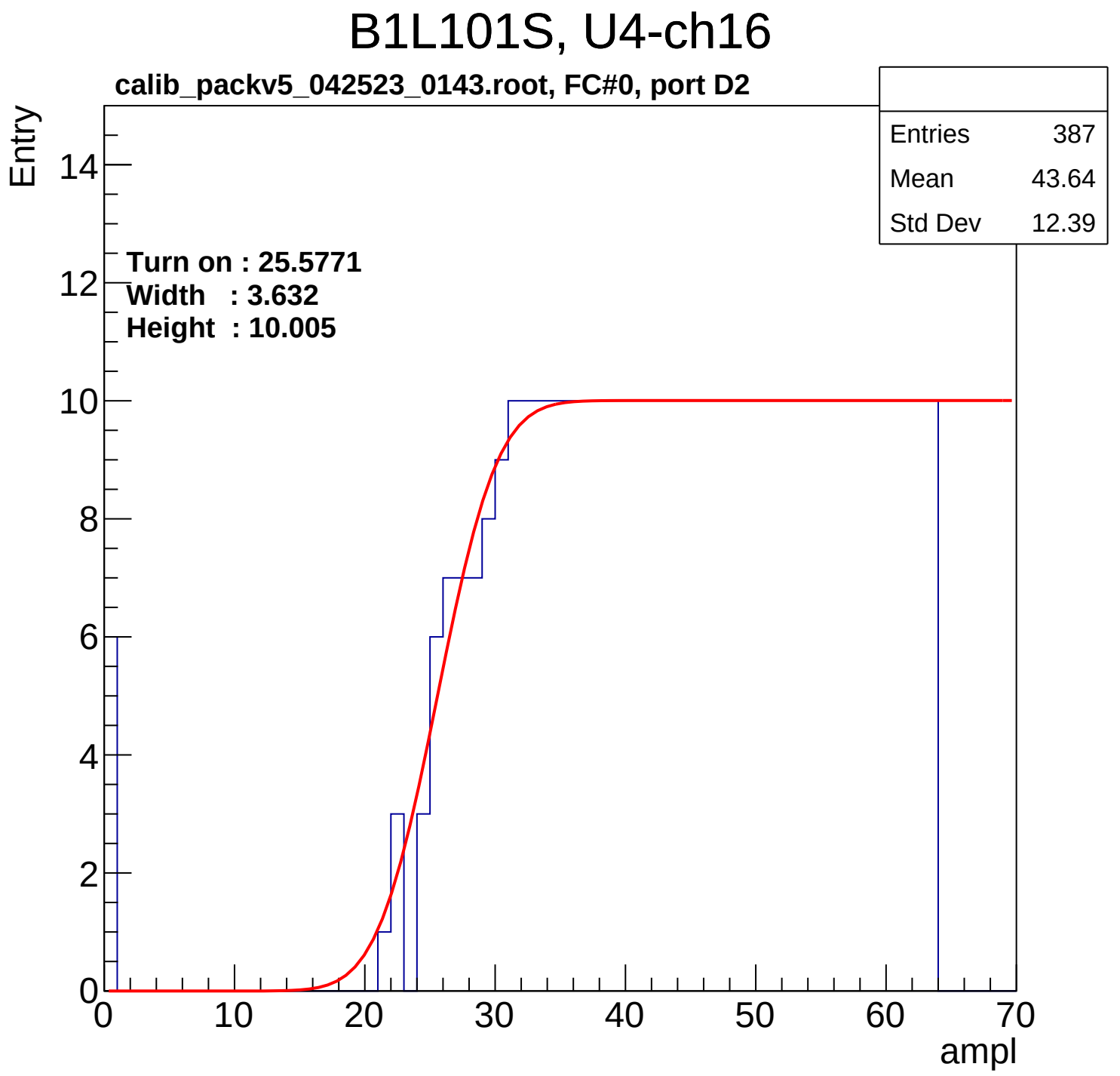

B1L101S, U4-ch11
calib_packv5_042523_0143.root, FC#0, port D2
Entries 394
Mean 43.41
Std Dev 12.33
Turn on : 25.4982
Width : 3.041
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

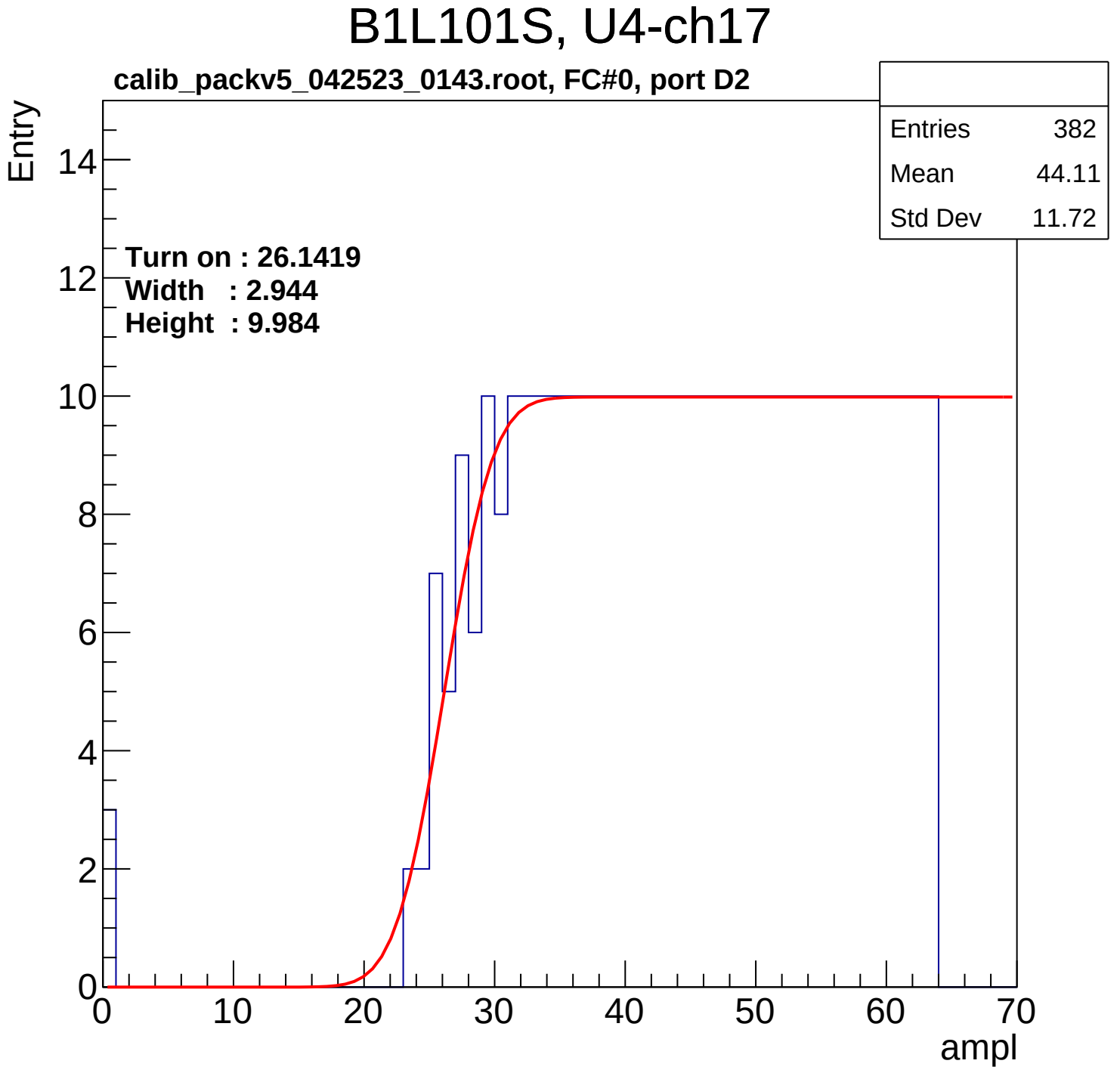

B1L101S, U4-ch12
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.54
Std Dev 11.38
Turn on : 26.9087
Width : 2.818
Height : 9.980
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

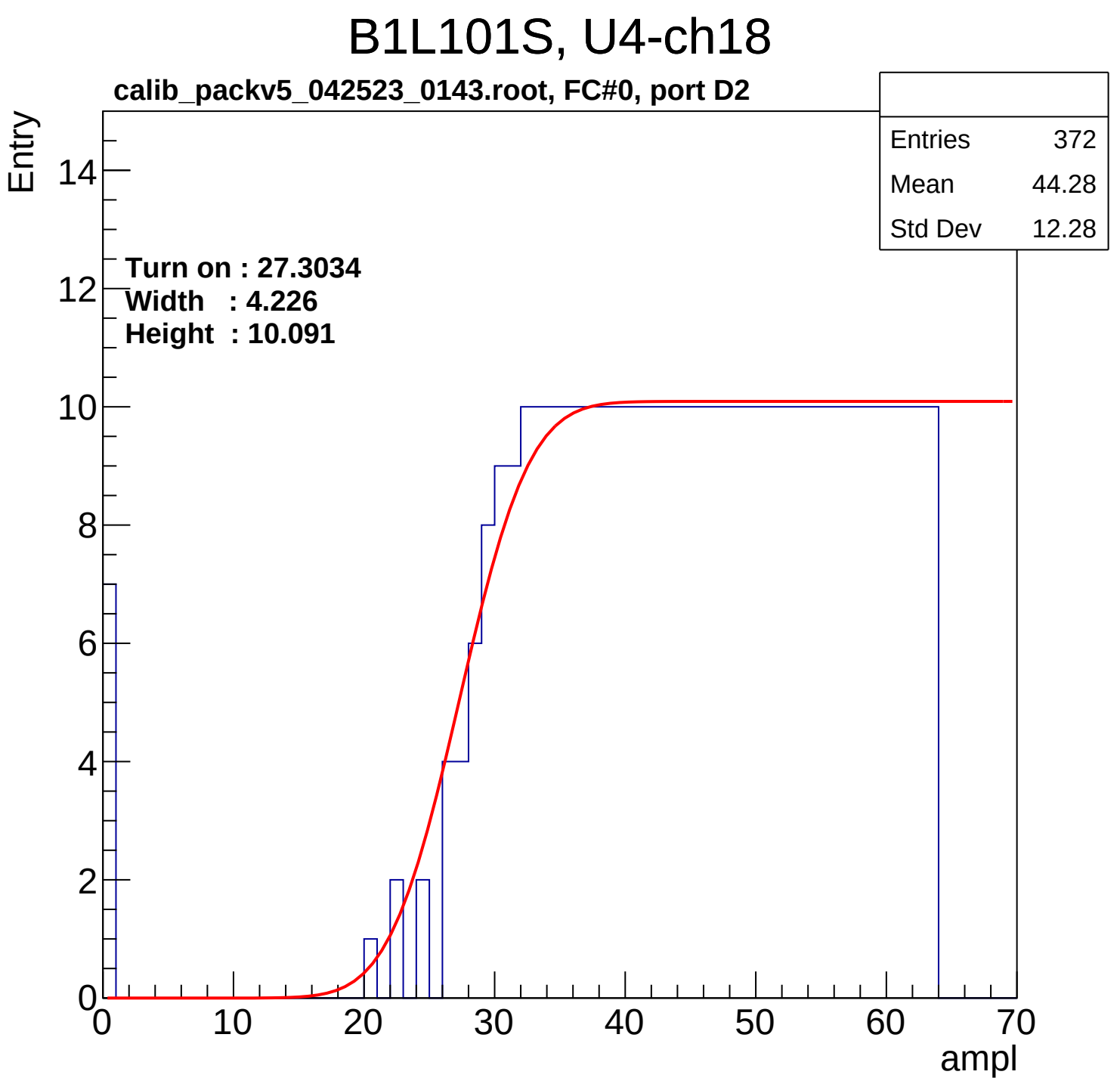

B1L101S, U4-ch13
calib_packv5_042523_0143.root, FC#0, port D2
Entries 392
Mean 43.55
Std Dev 12.16
Turn on : 25.7409
Width : 2.823
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

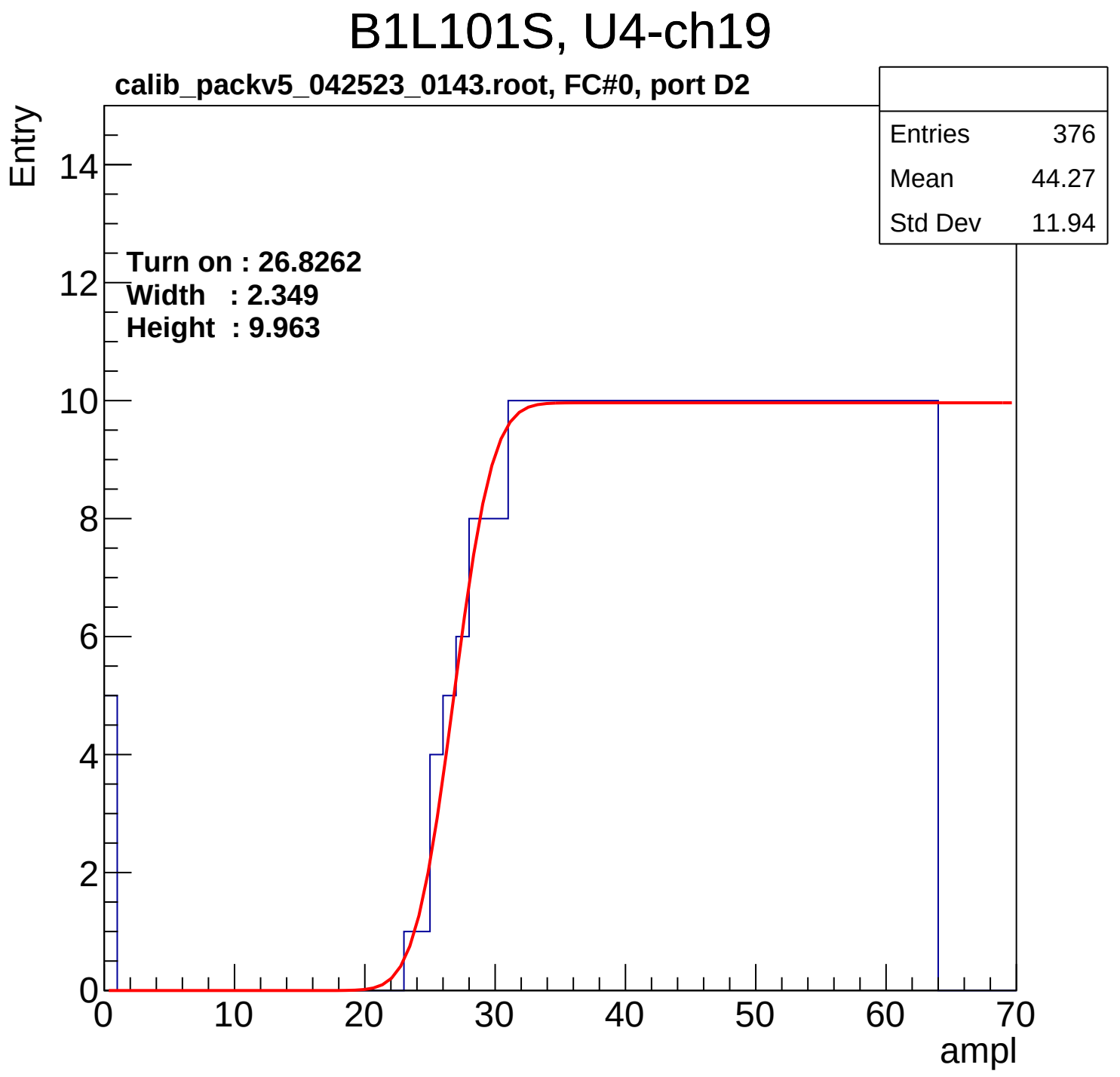

B1L101S, U4-ch14
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.37
Std Dev 11.95
Turn on : 27.6988
Width : 3.312
Height : 10.066
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

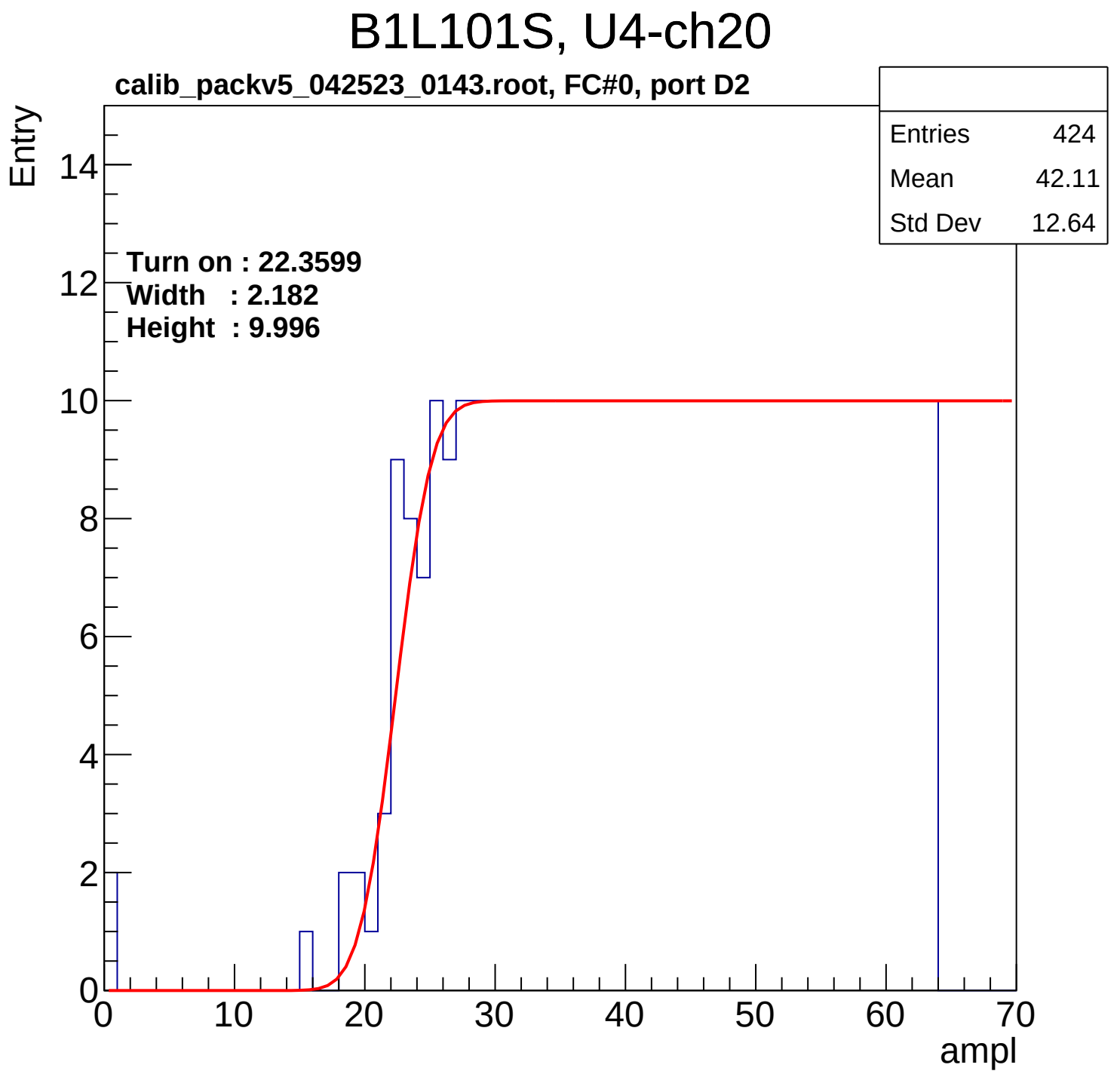

B1L101S, U4-ch15
calib_packv5_042523_0143.root, FC#0, port D2
Entries 365
Mean 44.95
Std Dev 11.31
Turn on : 28.2052
Width : 2.796
Height : 10.040
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

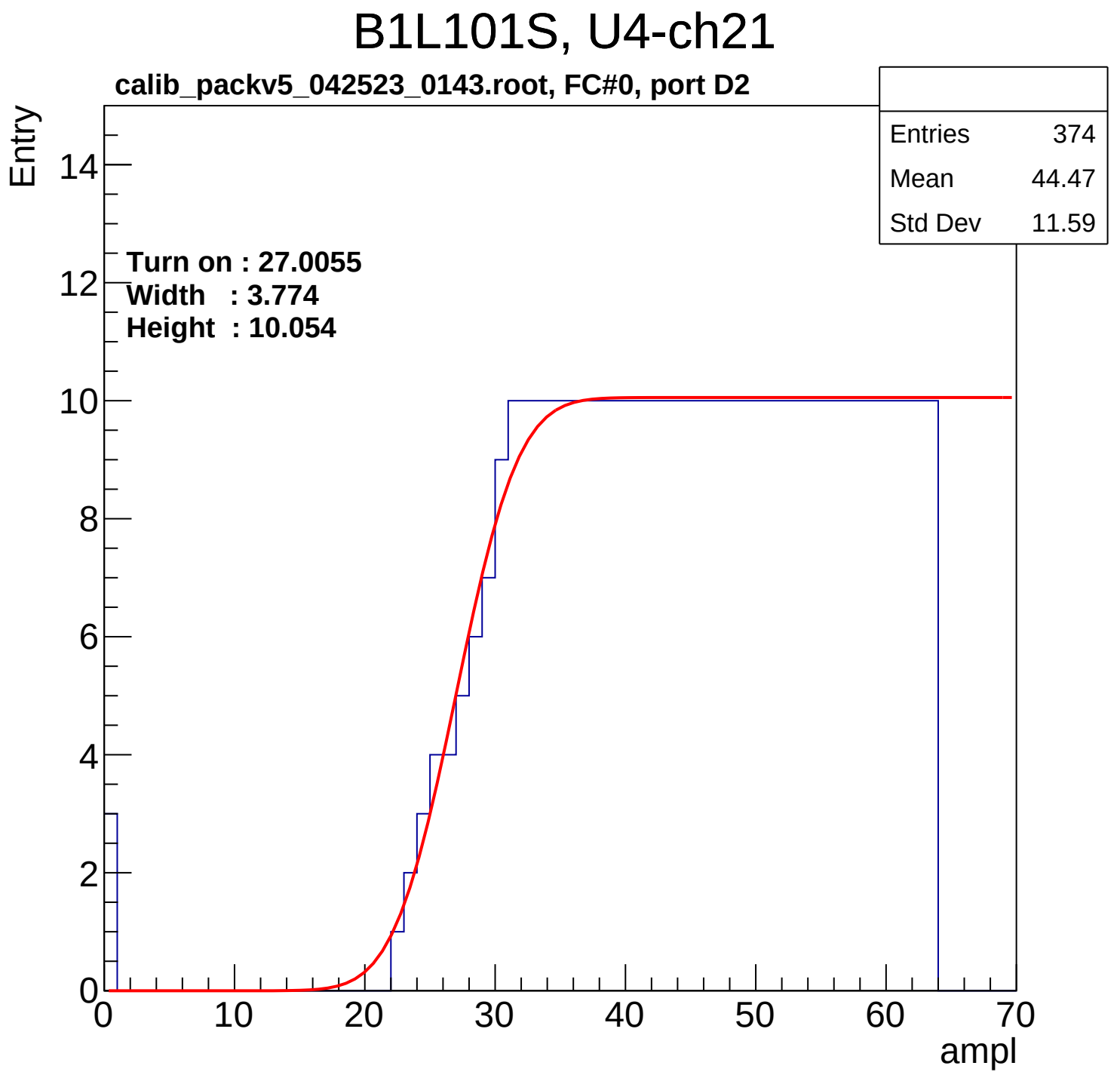

B1L101S, U4-ch16
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.64
Std Dev 12.39
Turn on : 25.5771
Width : 3.632
Height : 10.005
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

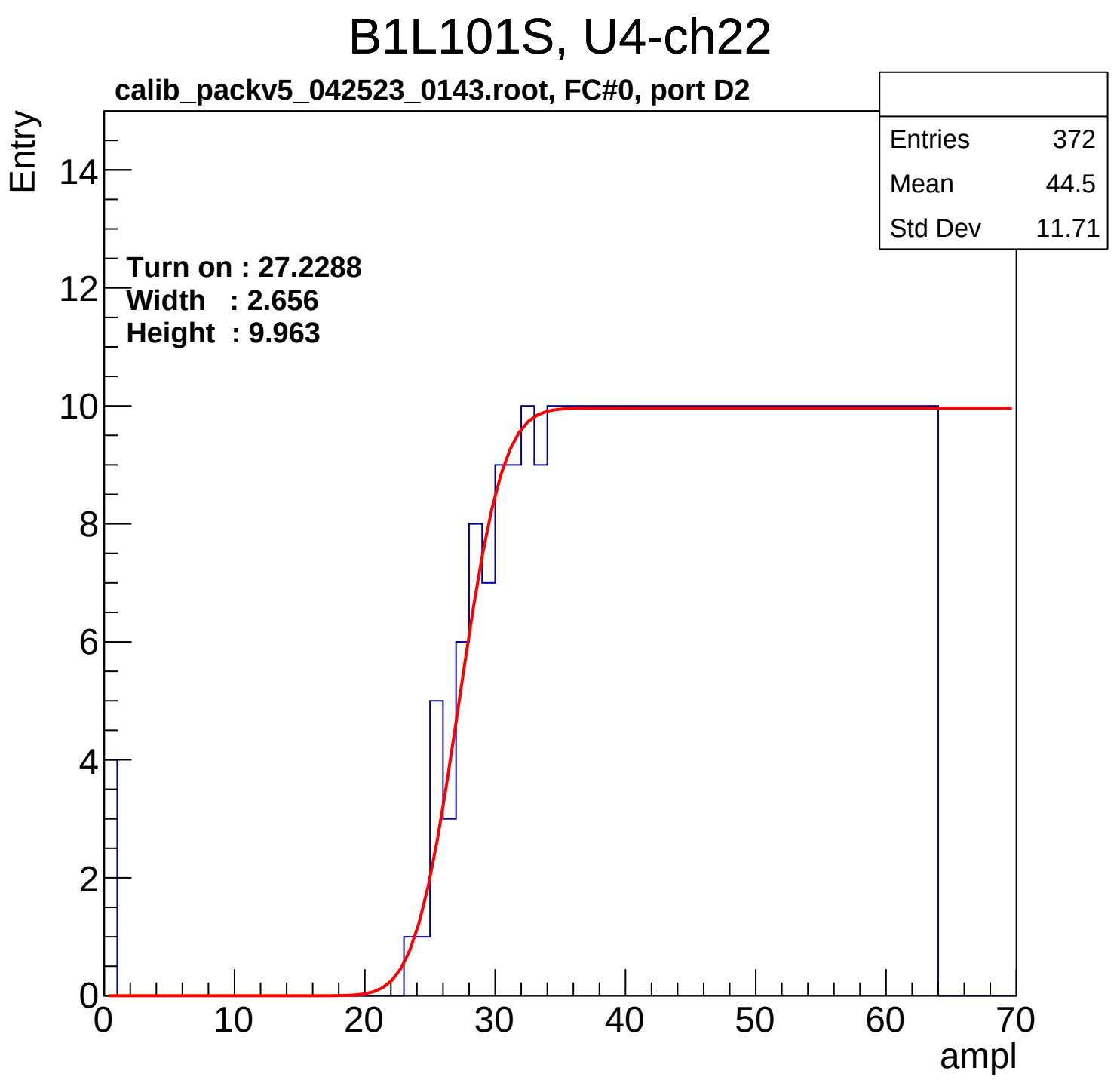

B1L101S, U4-ch17
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 44.11
Std Dev 11.72
Turn on : 26.1419
Width : 2.944
Height : 9.984
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

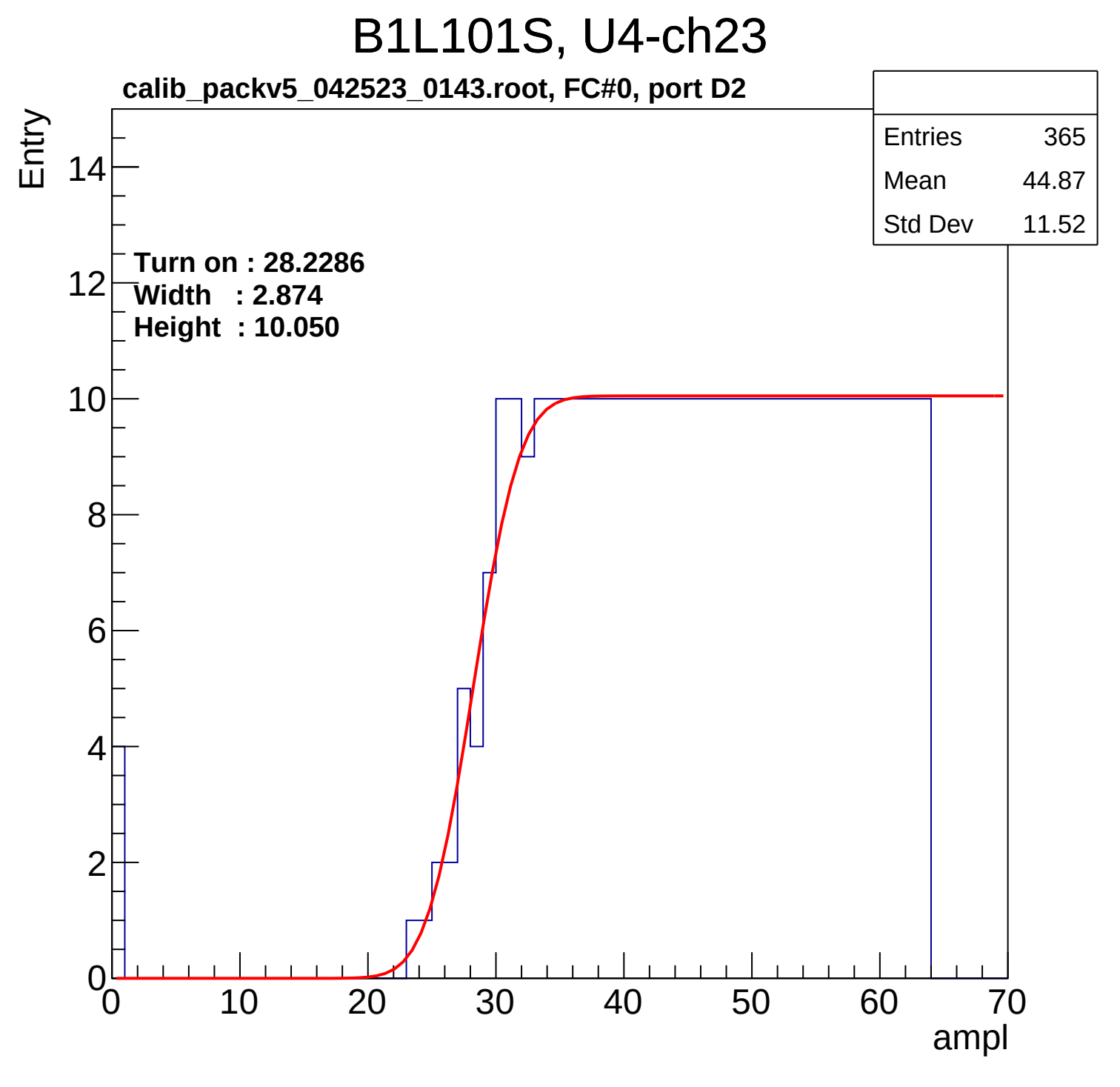

B1L101S, U4-ch18
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.28
Std Dev 12.28
Turn on : 27.3034
Width : 4.226
Height : 10.091
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

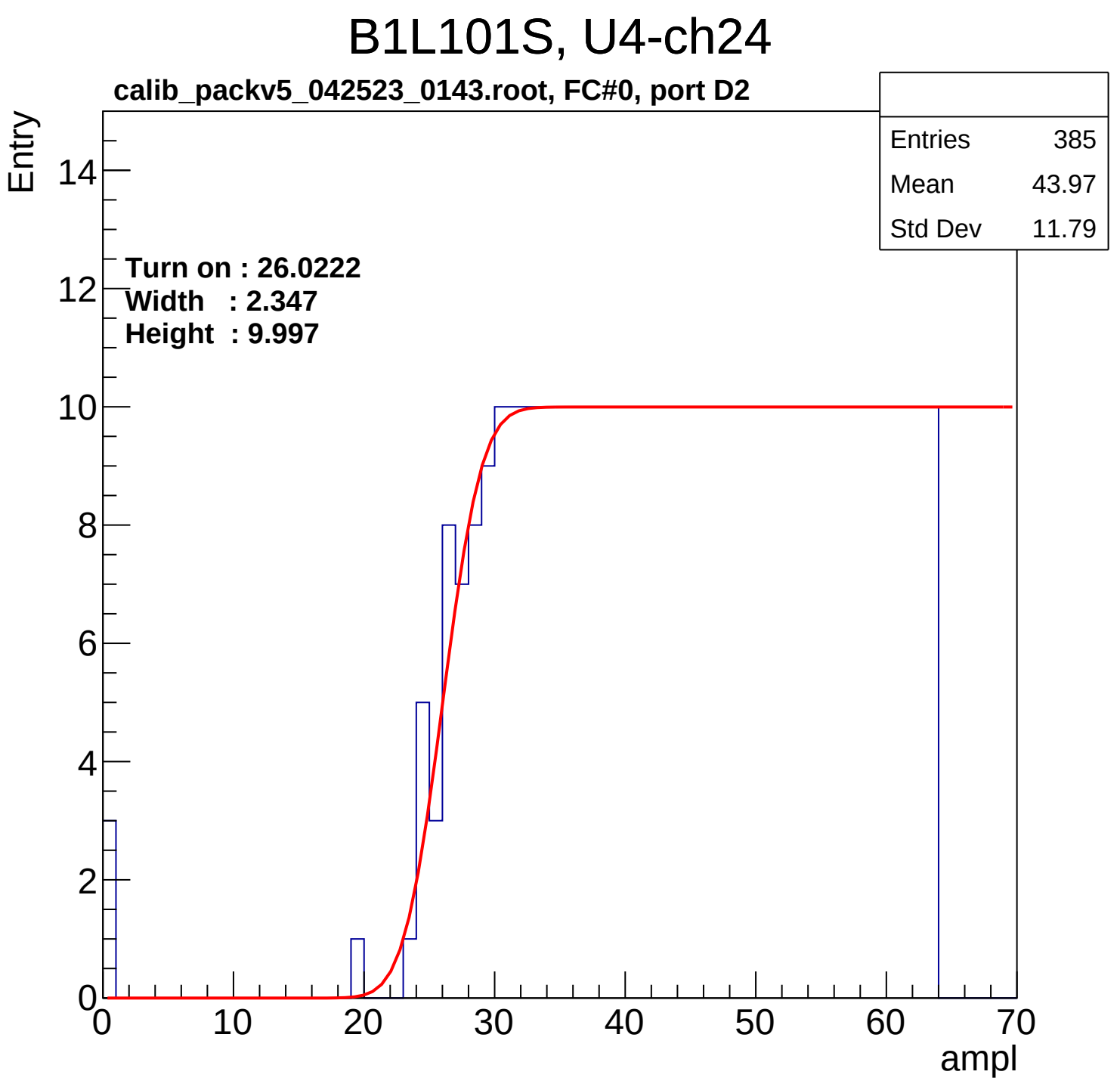

B1L101S, U4-ch19
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.27
Std Dev 11.94
Turn on : 26.8262
Width : 2.349
Height : 9.963
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

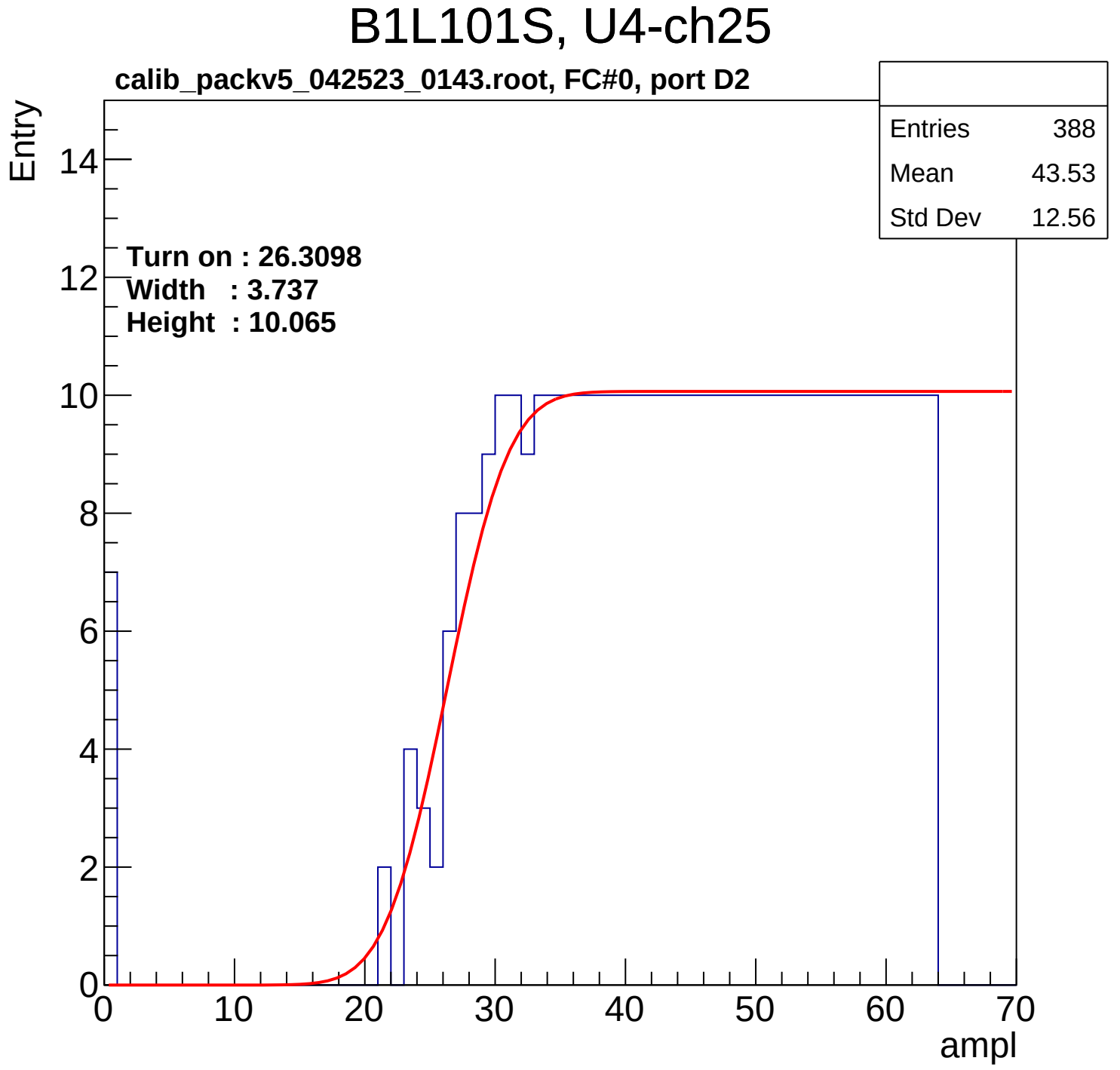

B1L101S, U4-ch20
calib_packv5_042523_0143.root, FC#0, port D2
Entries 424
Mean 42.11
Std Dev 12.64
Turn on : 22.3599
Width : 2.182
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

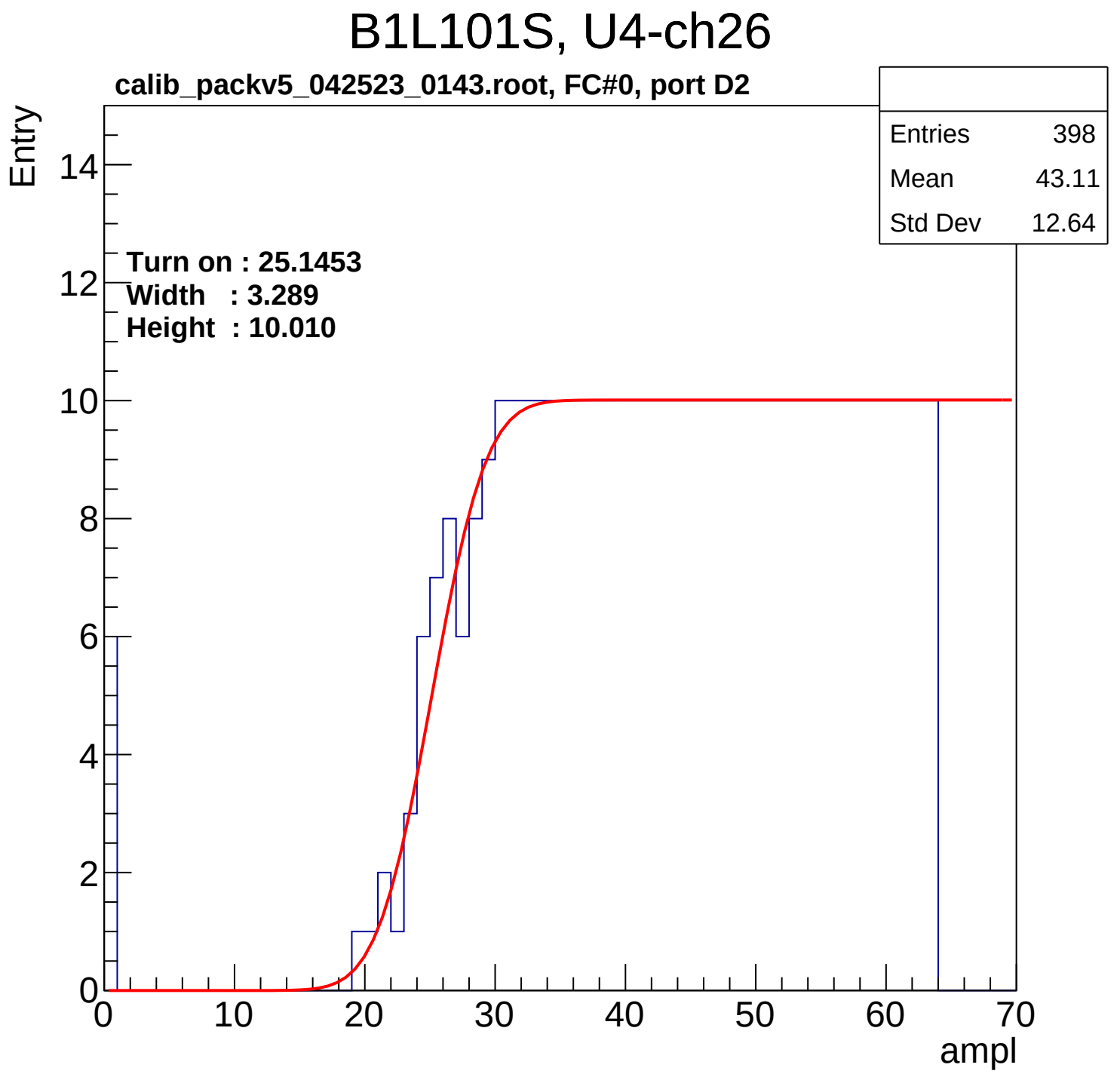

B1L101S, U4-ch21
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.47
Std Dev 11.59
Turn on : 27.0055
Width : 3.774
Height : 10.054
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

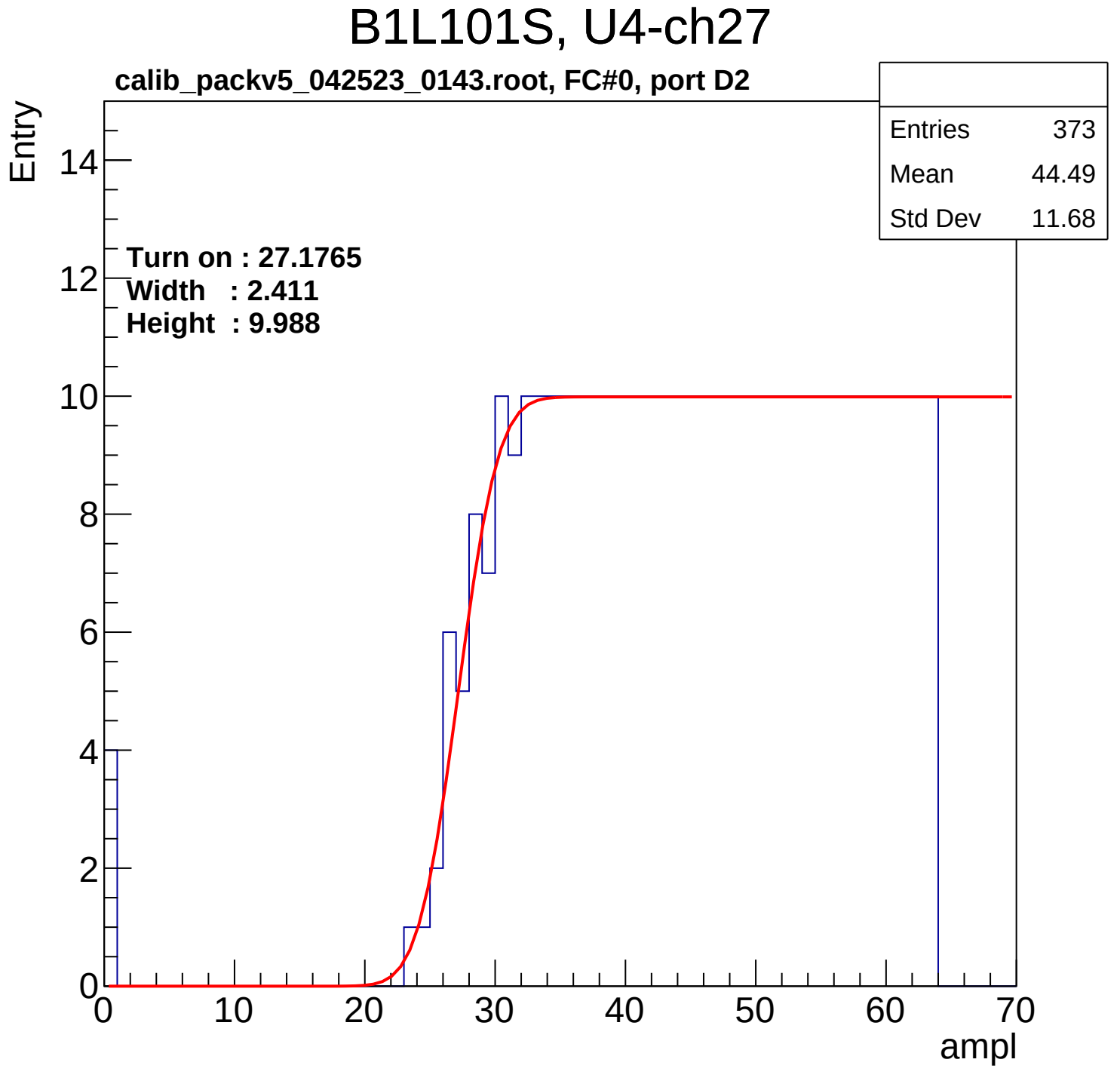

B1L101S, U4-ch22
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.5
Std Dev 11.71
Turn on : 27.2288
Width : 2.656
Height : 9.963
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

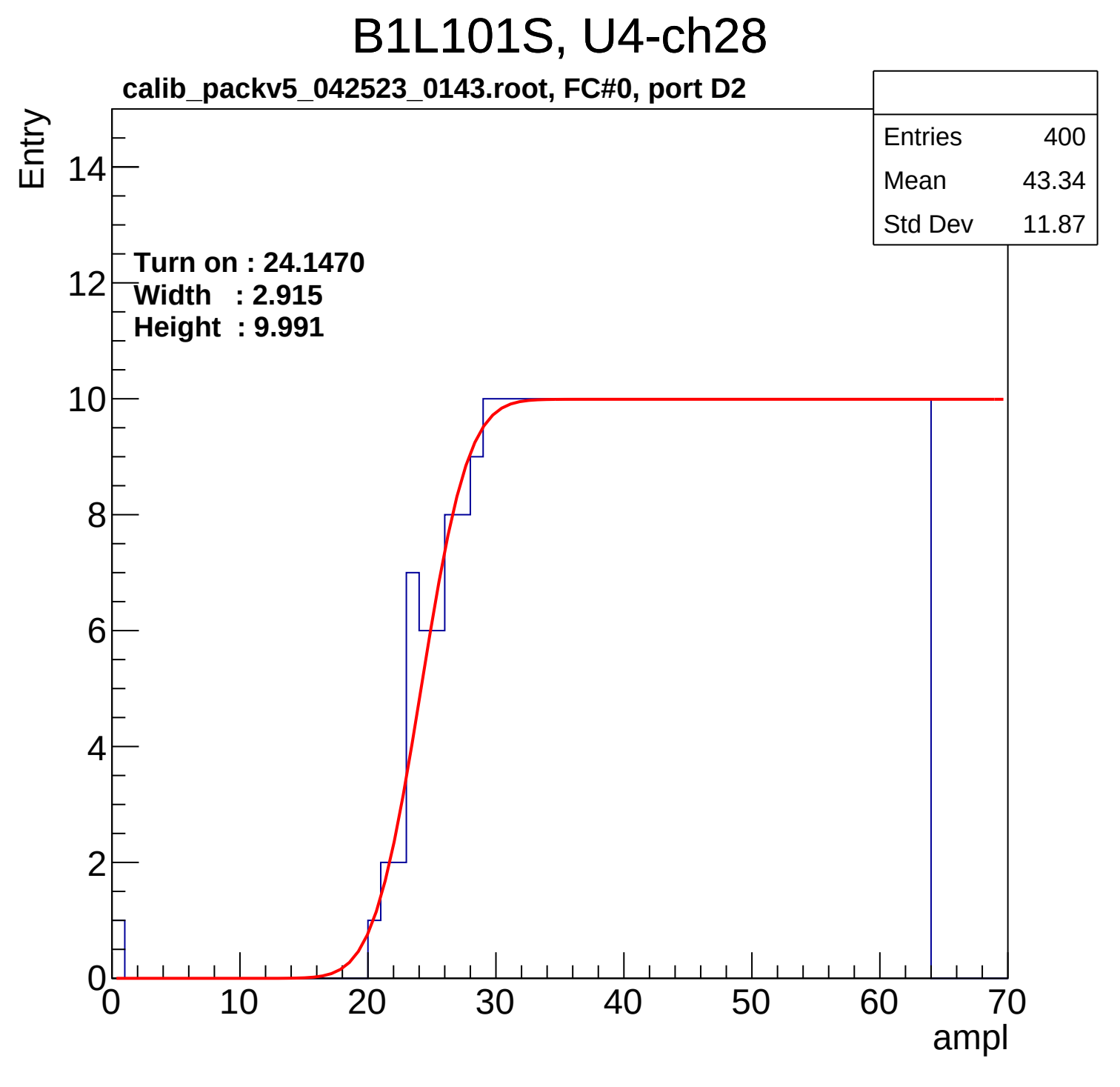

B1L101S, U4-ch23
calib_packv5_042523_0143.root, FC#0, port D2
Entries 365
Mean 44.87
Std Dev 11.52
Turn on : 28.2286
Width : 2.874
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

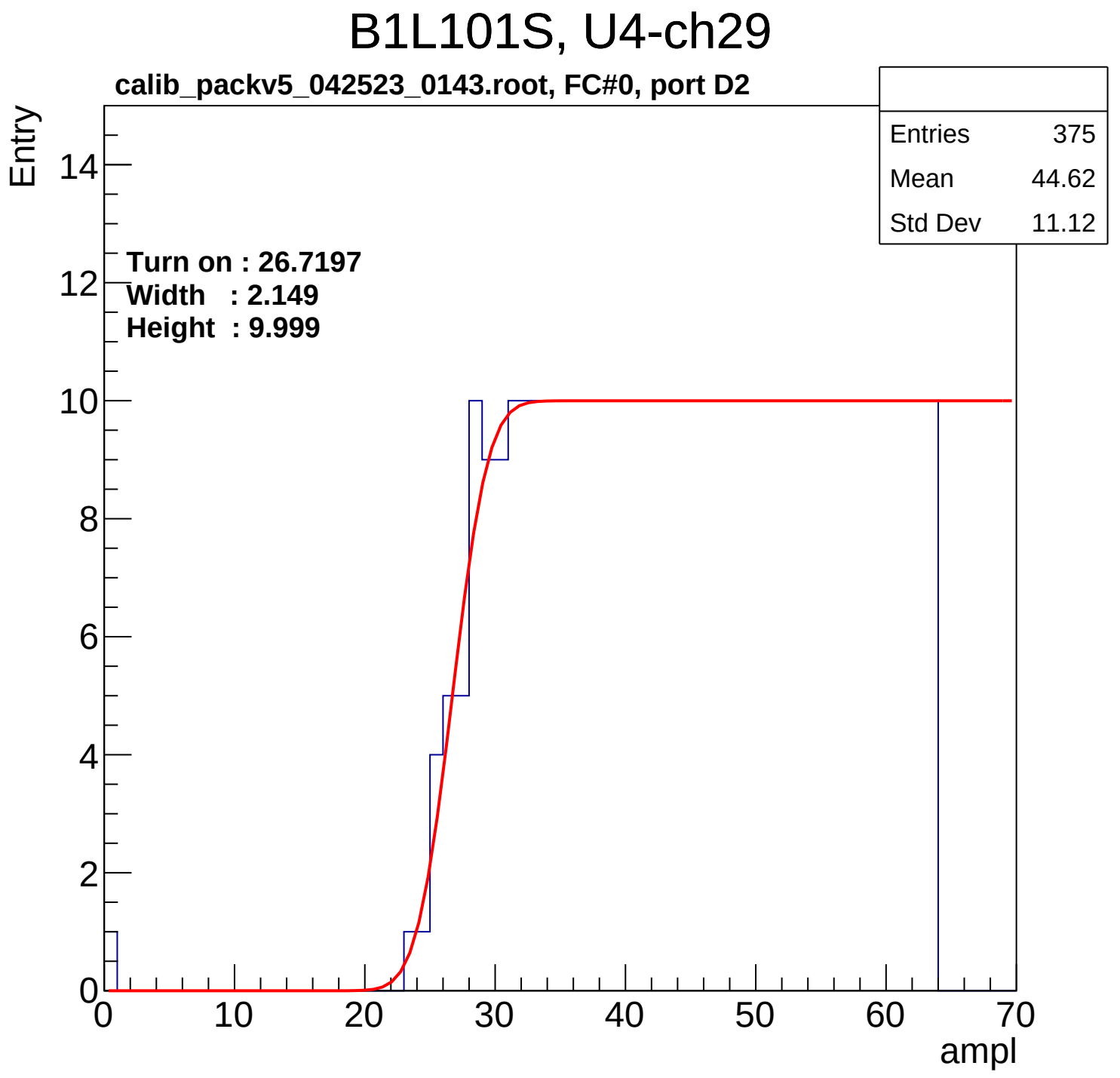

B1L101S, U4-ch24
calib_packv5_042523_0143.root, FC#0, port D2
Entries 385
Mean 43.97
Std Dev 11.79
Turn on : 26.0222
Width : 2.347
Height : 9.997
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

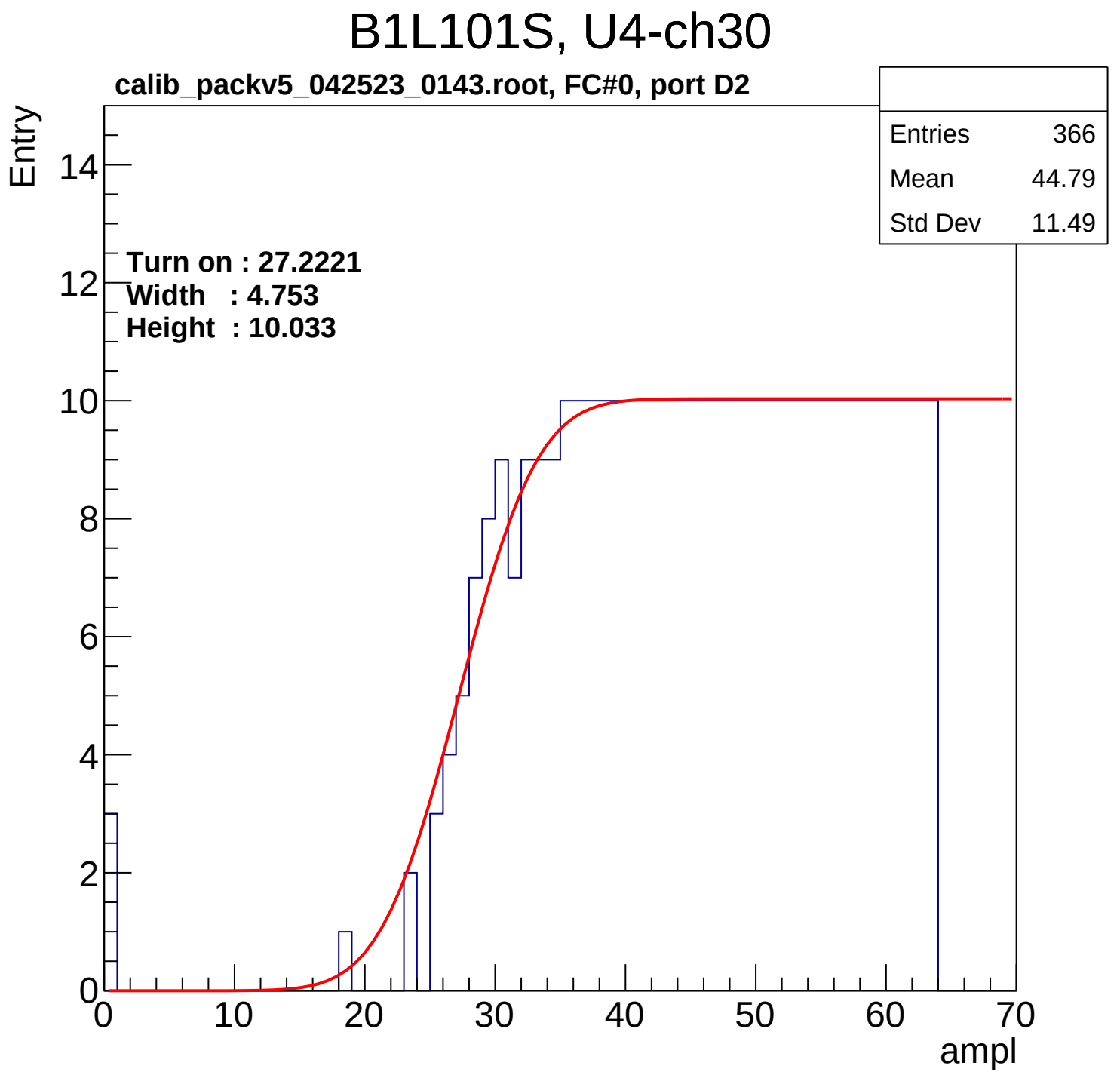

B1L101S, U4-ch25
calib_packv5_042523_0143.root, FC#0, port D2
Entries 388
Mean 43.53
Std Dev 12.56
Turn on : 26.3098
Width : 3.737
Height : 10.065
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

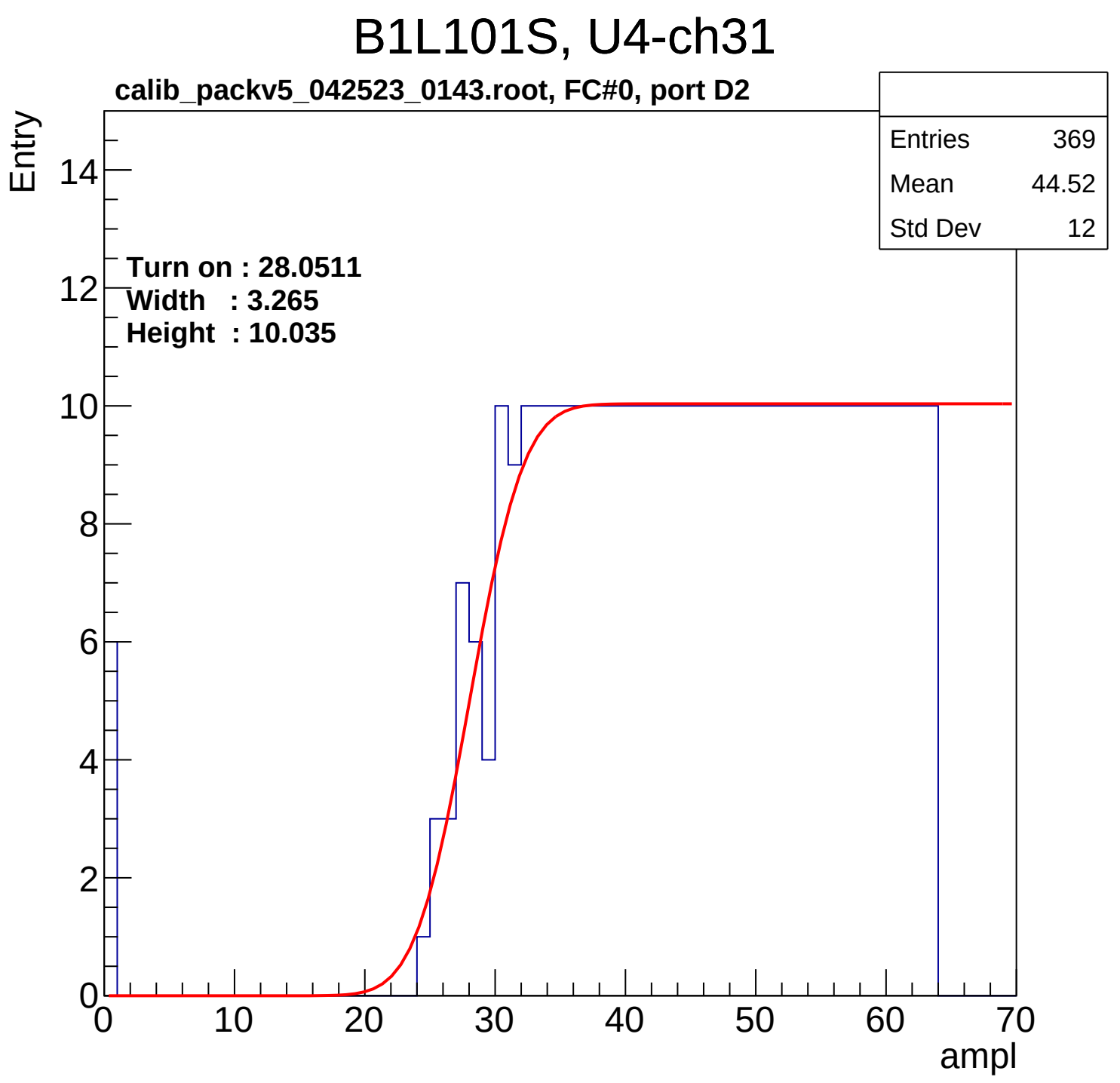

B1L101S, U4-ch26
calib_packv5_042523_0143.root, FC#0, port D2
Entries 398
Mean 43.11
Std Dev 12.64
Turn on : 25.1453
Width : 3.289
Height : 10.010
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

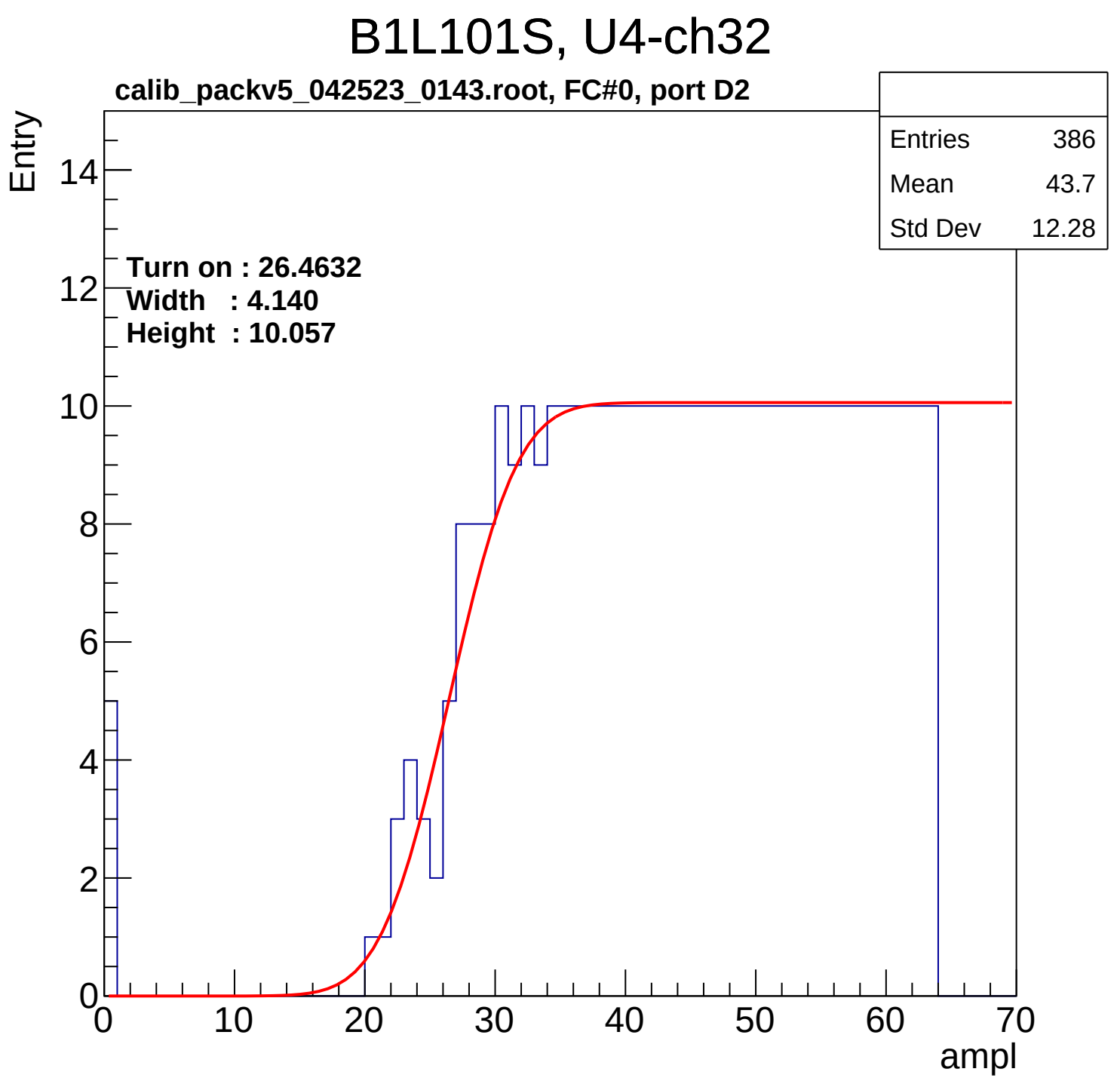

B1L101S, U4-ch27
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.49
Std Dev 11.68
Turn on : 27.1765
Width : 2.411
Height : 9.988
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

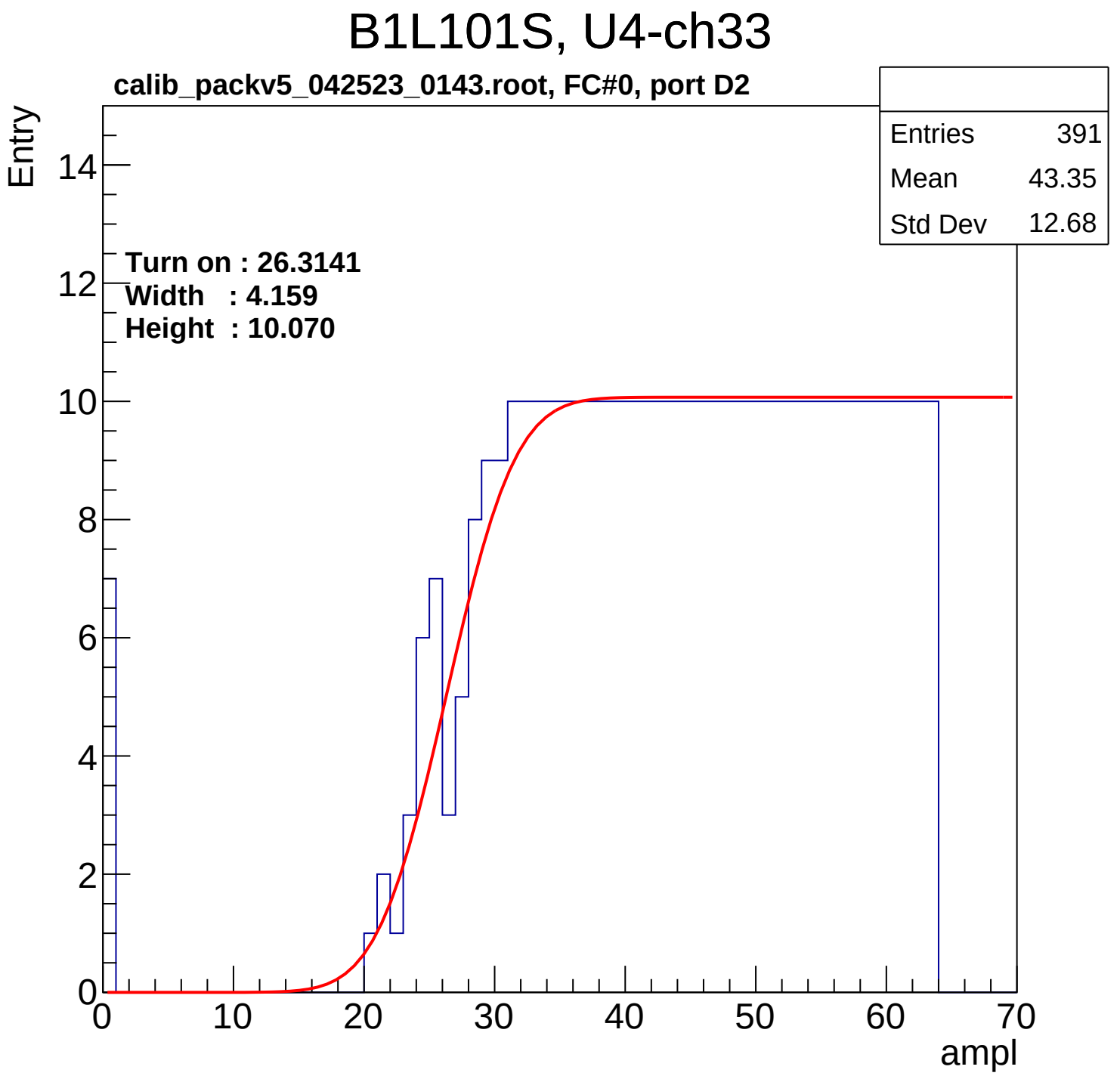

B1L101S, U4-ch28
calib_packv5_042523_0143.root, FC#0, port D2
Entries 400
Mean 43.34
Std Dev 11.87
Turn on : 24.1470
Width : 2.915
Height : 9.991
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

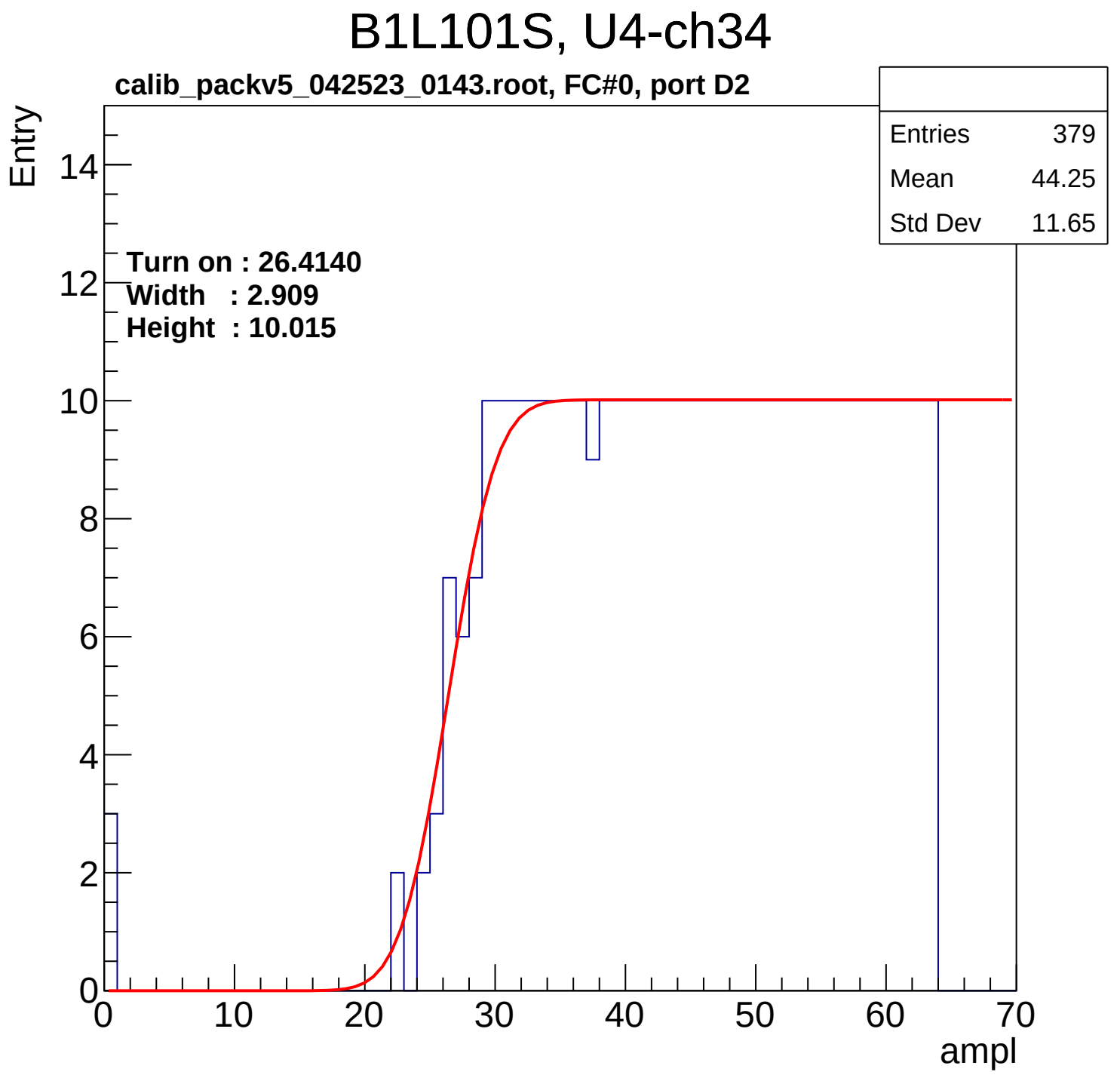

B1L101S, U4-ch29
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.62
Std Dev 11.12
Turn on : 26.7197
Width : 2.149
Height : 9.999
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

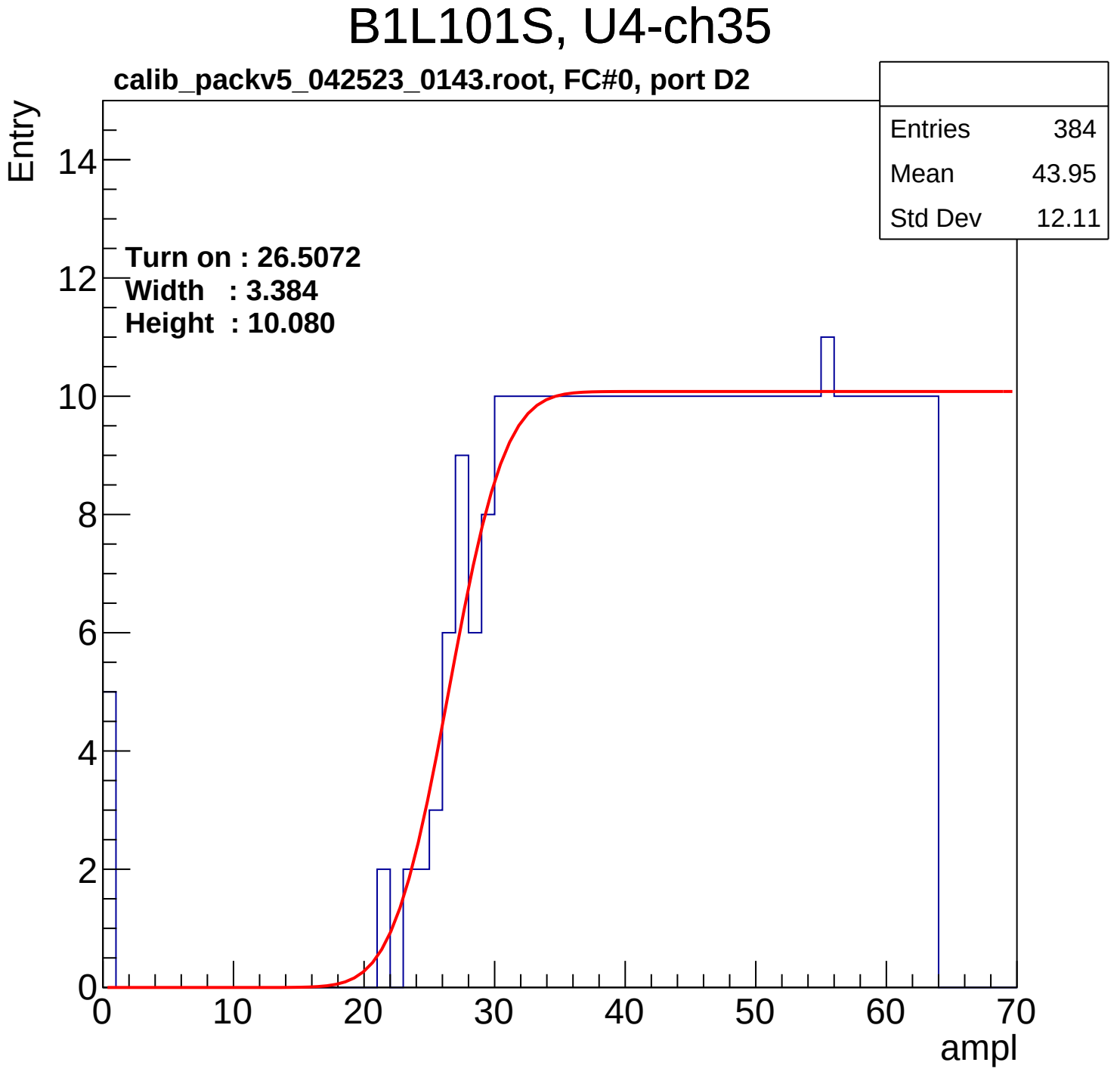

B1L101S, U4-ch30
calib_packv5_042523_0143.root, FC#0, port D2
Entries 366
Mean 44.79
Std Dev 11.49
Turn on : 27.2221
Width : 4.753
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

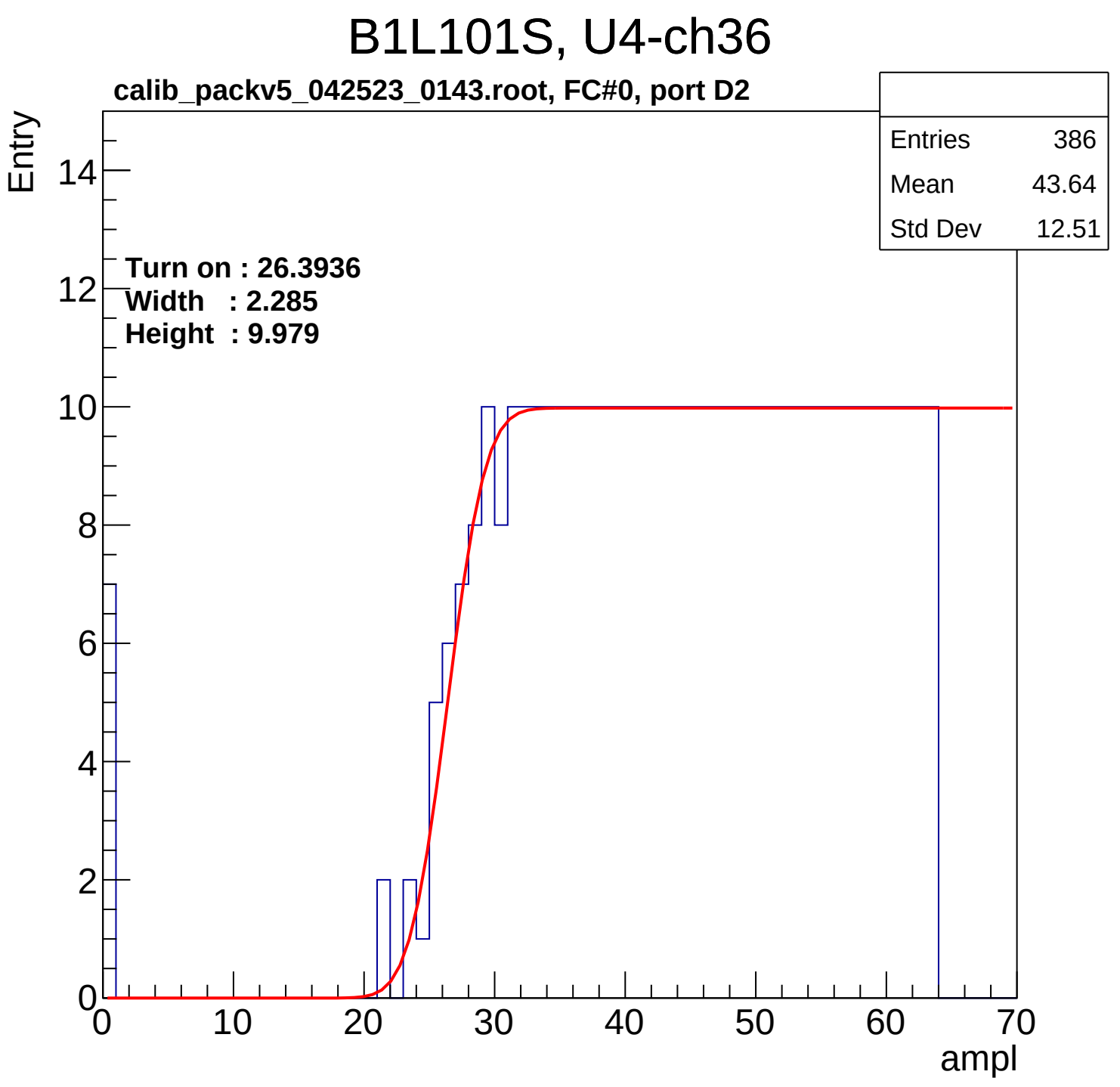

B1L101S, U4-ch31
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.52
Std Dev 12
Turn on : 28.0511
Width : 3.265
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

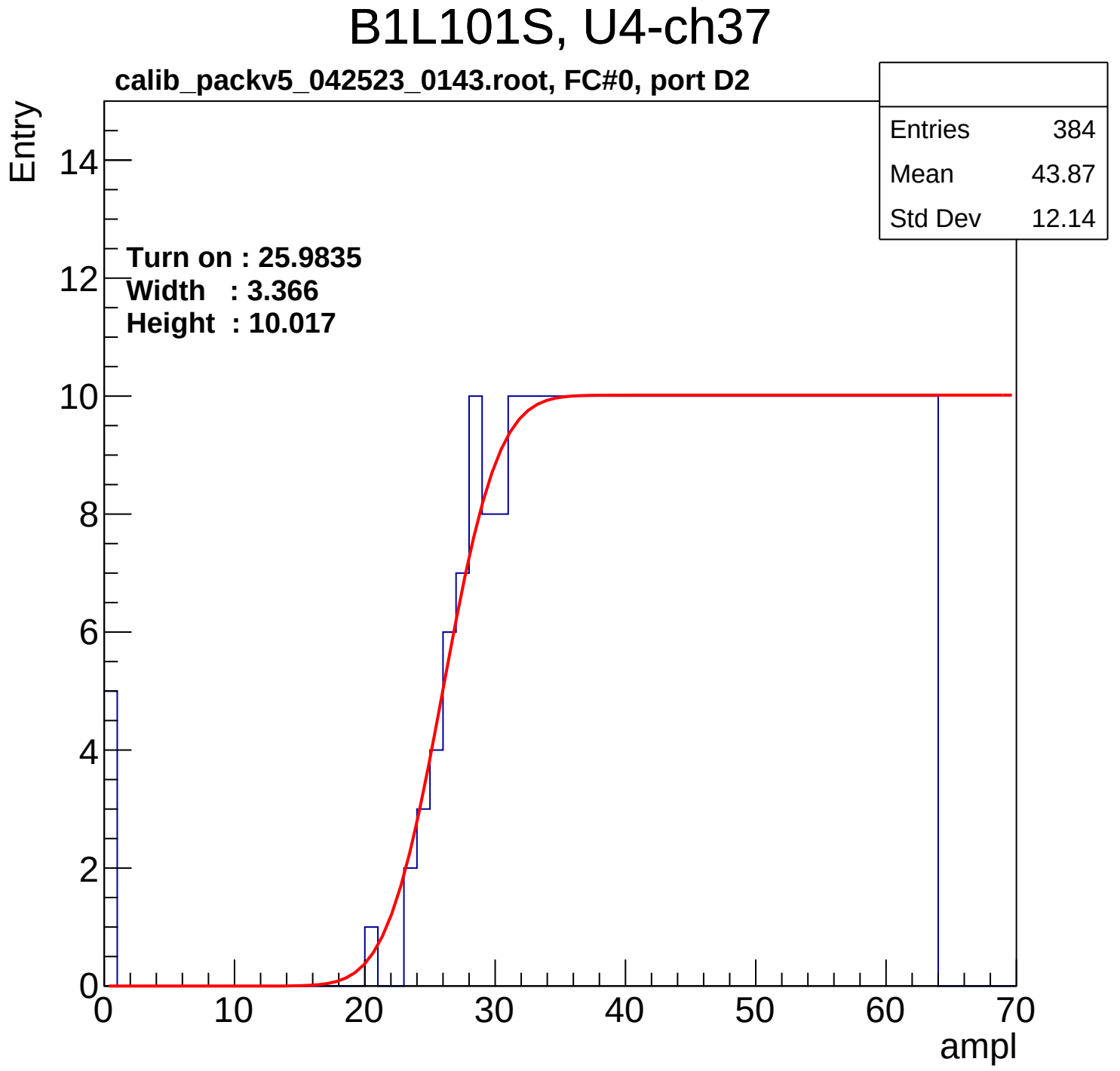

B1L101S, U4-ch32
calib_packv5_042523_0143.root, FC#0, port D2
Entries 386
Mean 43.7
Std Dev 12.28
Turn on : 26.4632
Width : 4.140
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

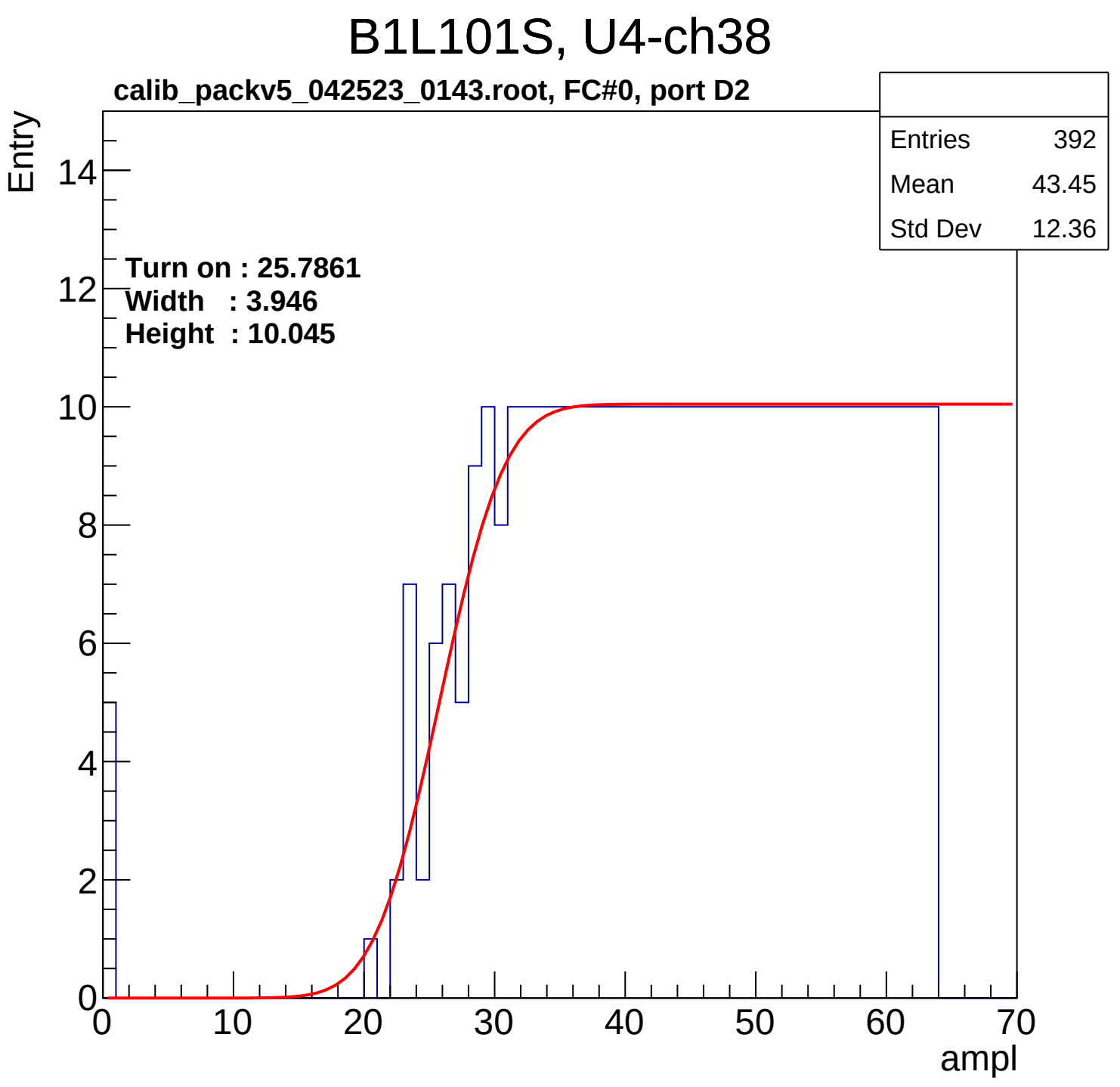

B1L101S, U4-ch33
calib_packv5_042523_0143.root, FC#0, port D2
Entries 391
Mean 43.35
Std Dev 12.68
Turn on : 26.3141
Width : 4.159
Height : 10.070
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

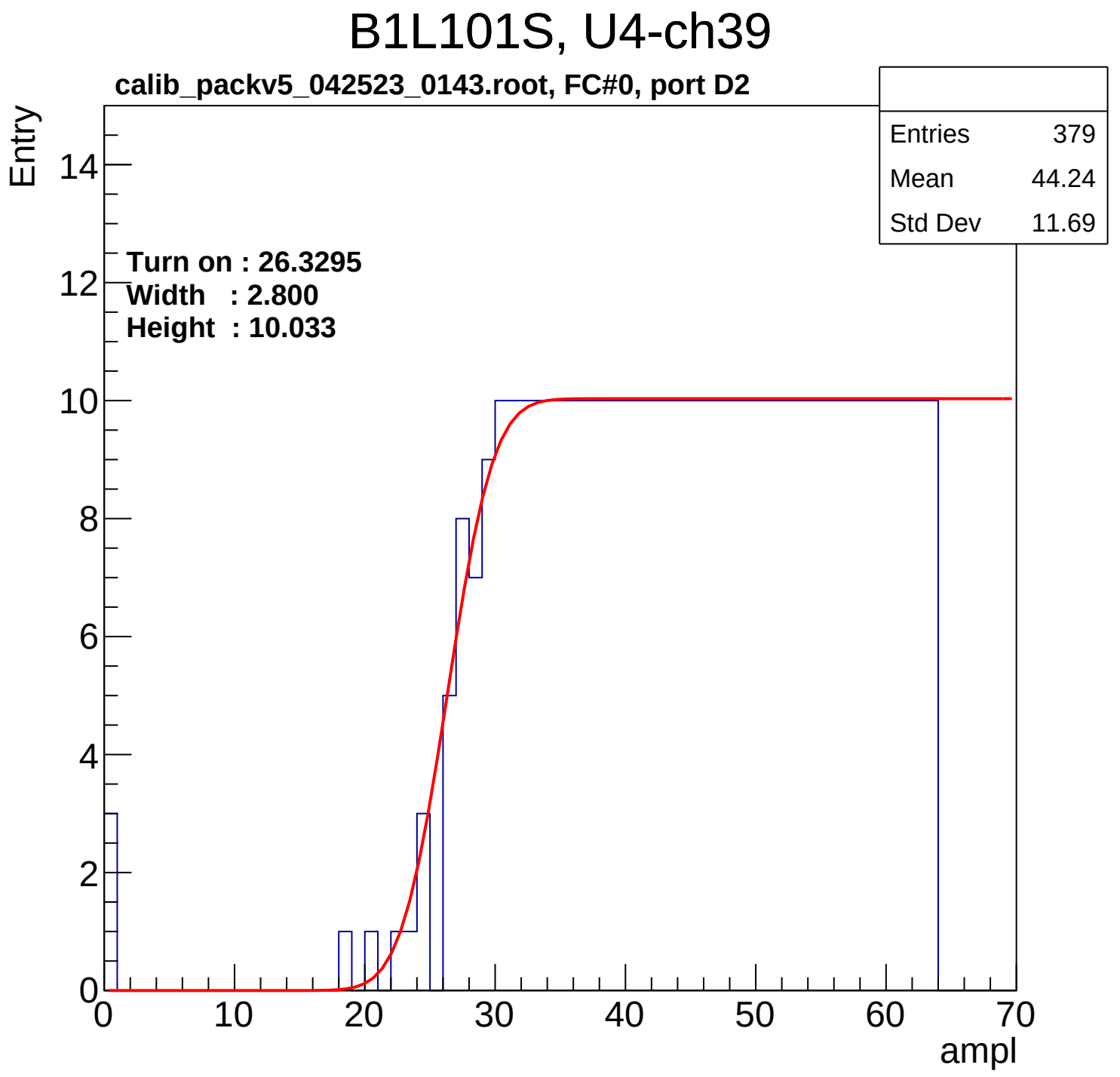

B1L101S, U4-ch34
calib_packv5_042523_0143.root, FC#0, port D2
Entries 379
Mean 44.25
Std Dev 11.65
Turn on : 26.4140
Width : 2.909
Height : 10.015
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

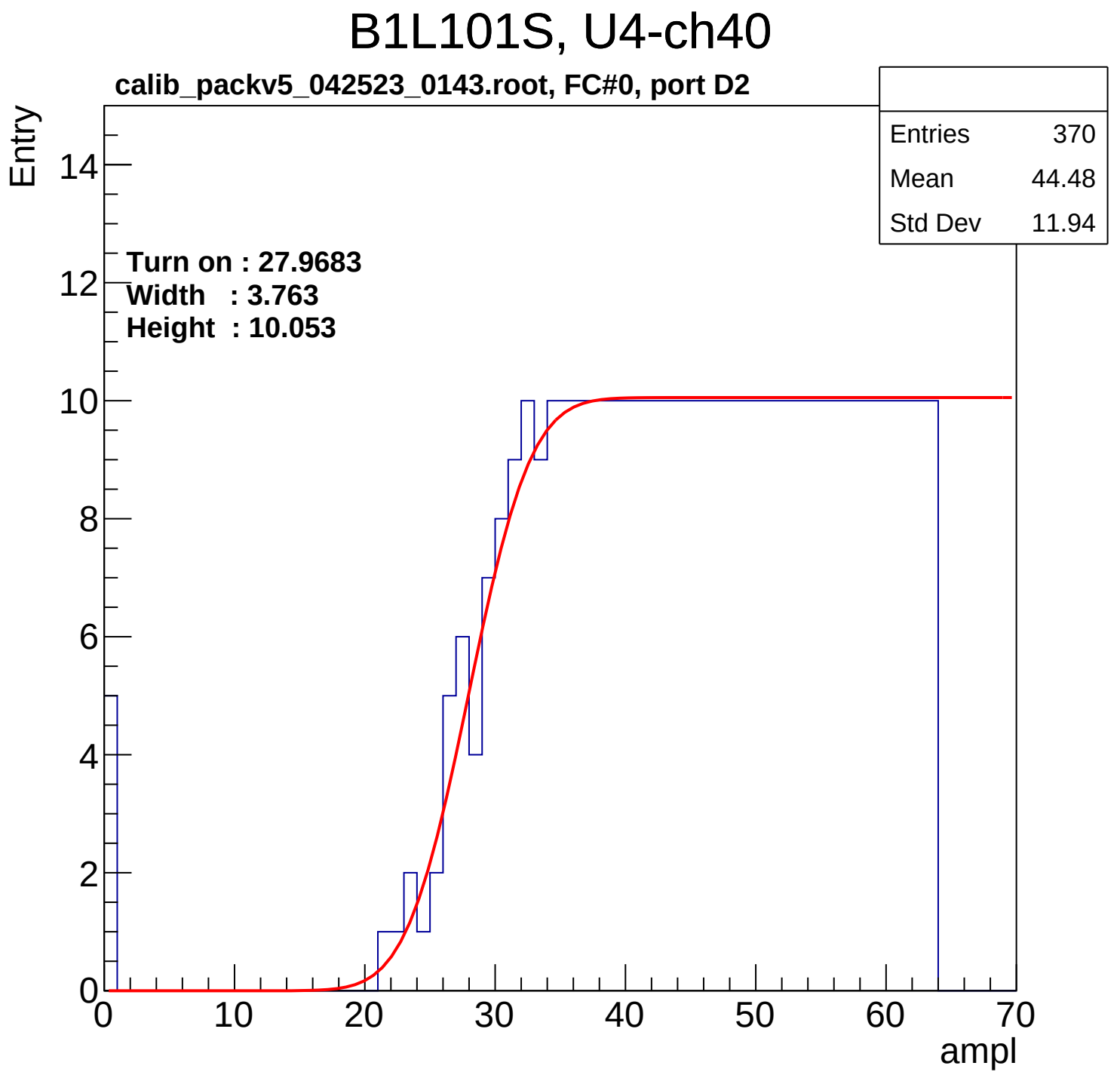

B1L101S, U4-ch35
calib_packv5_042523_0143.root, FC#0, port D2
Entries 384
Mean 43.95
Std Dev 12.11
Turn on : 26.5072
Width : 3.384
Height : 10.080
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

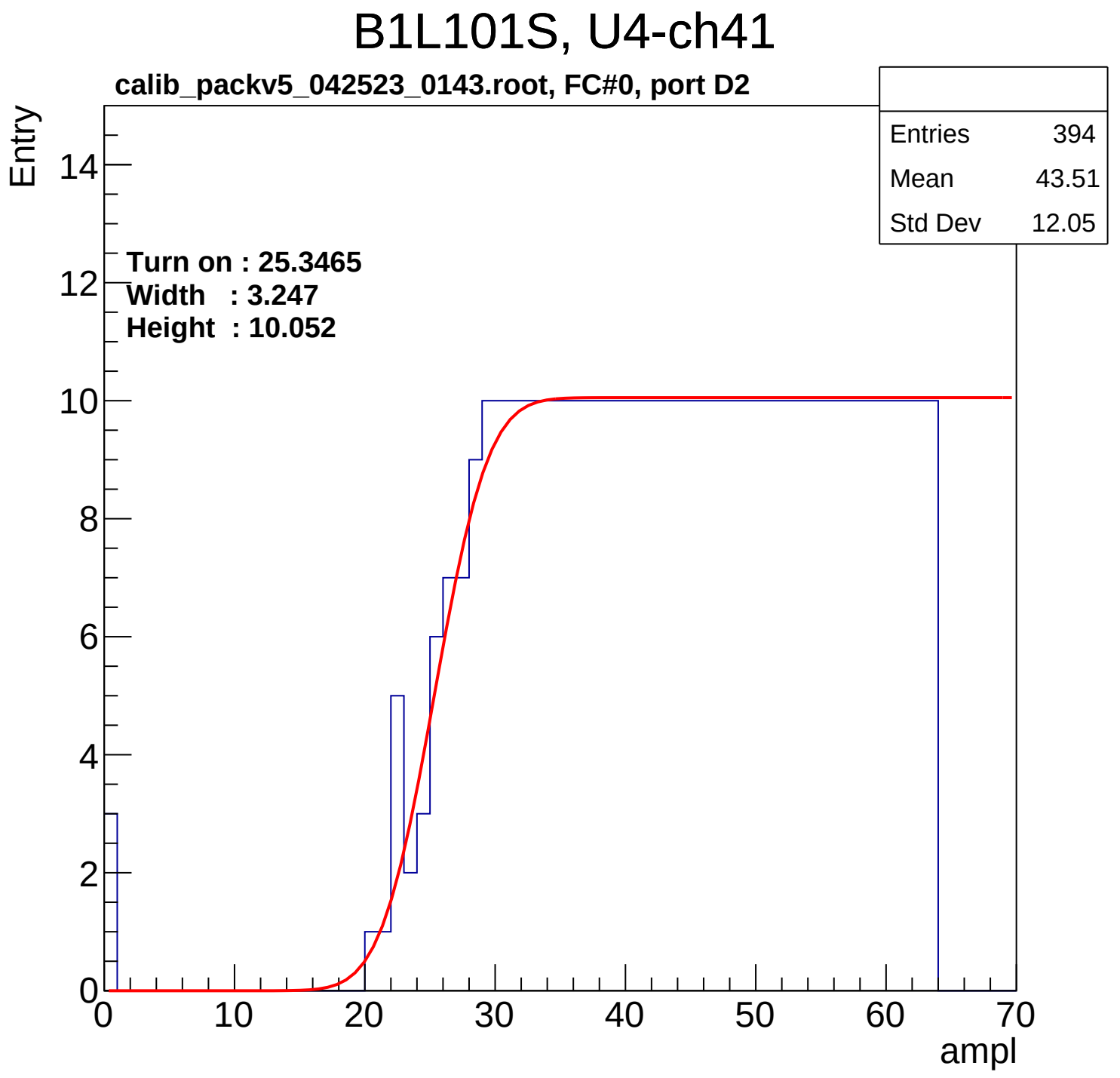

B1L101S, U4-ch36
calib_packv5_042523_0143.root, FC#0, port D2
Entries 386
Mean 43.64
Std Dev 12.51
Turn on : 26.3936
Width : 2.285
Height : 9.979
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

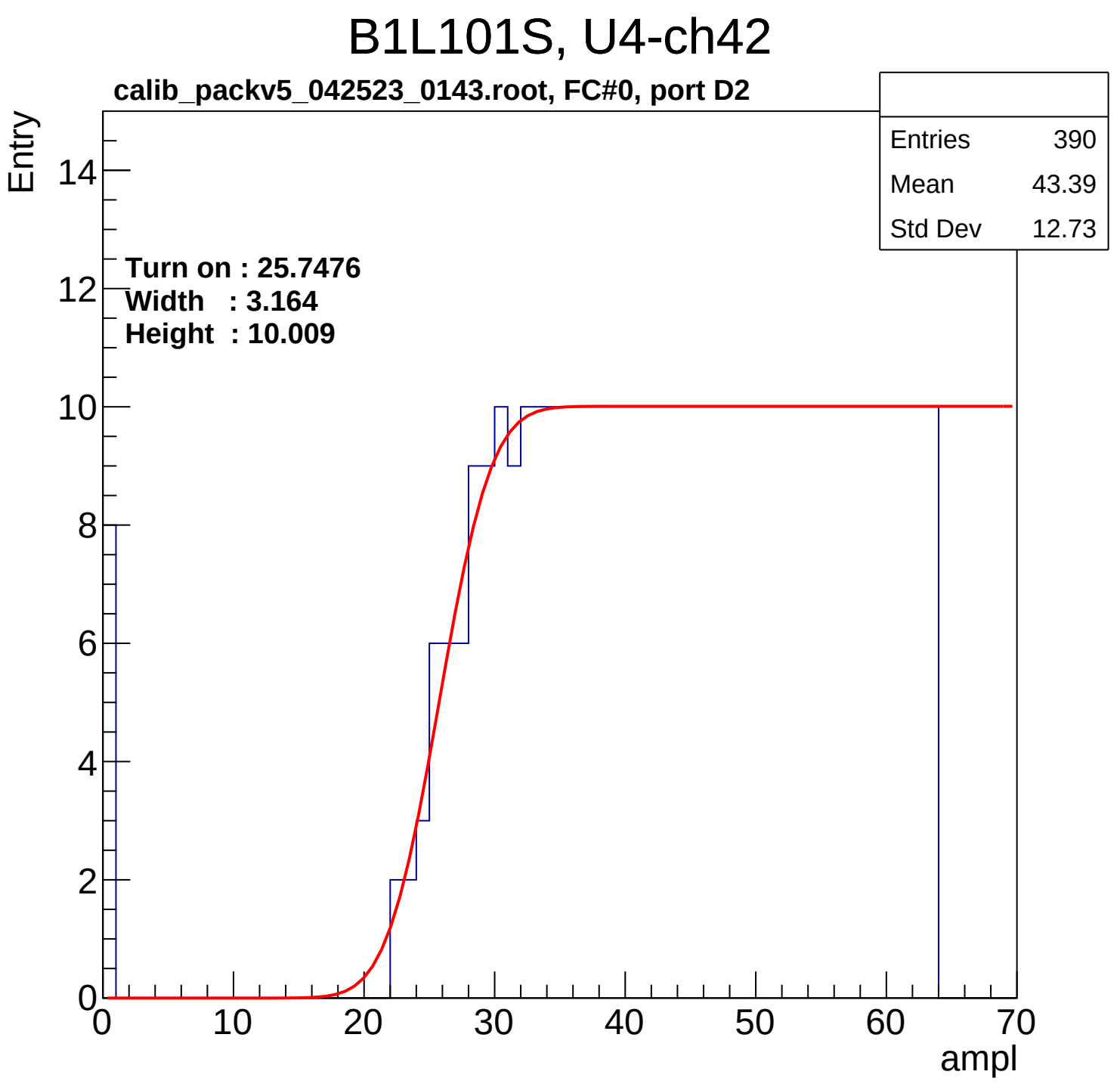

B1L101S, U4-ch37
calib_packv5_042523_0143.root, FC#0, port D2
Entries 384
Mean 43.87
Std Dev 12.14
Turn on : 25.9835
Width : 3.366
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

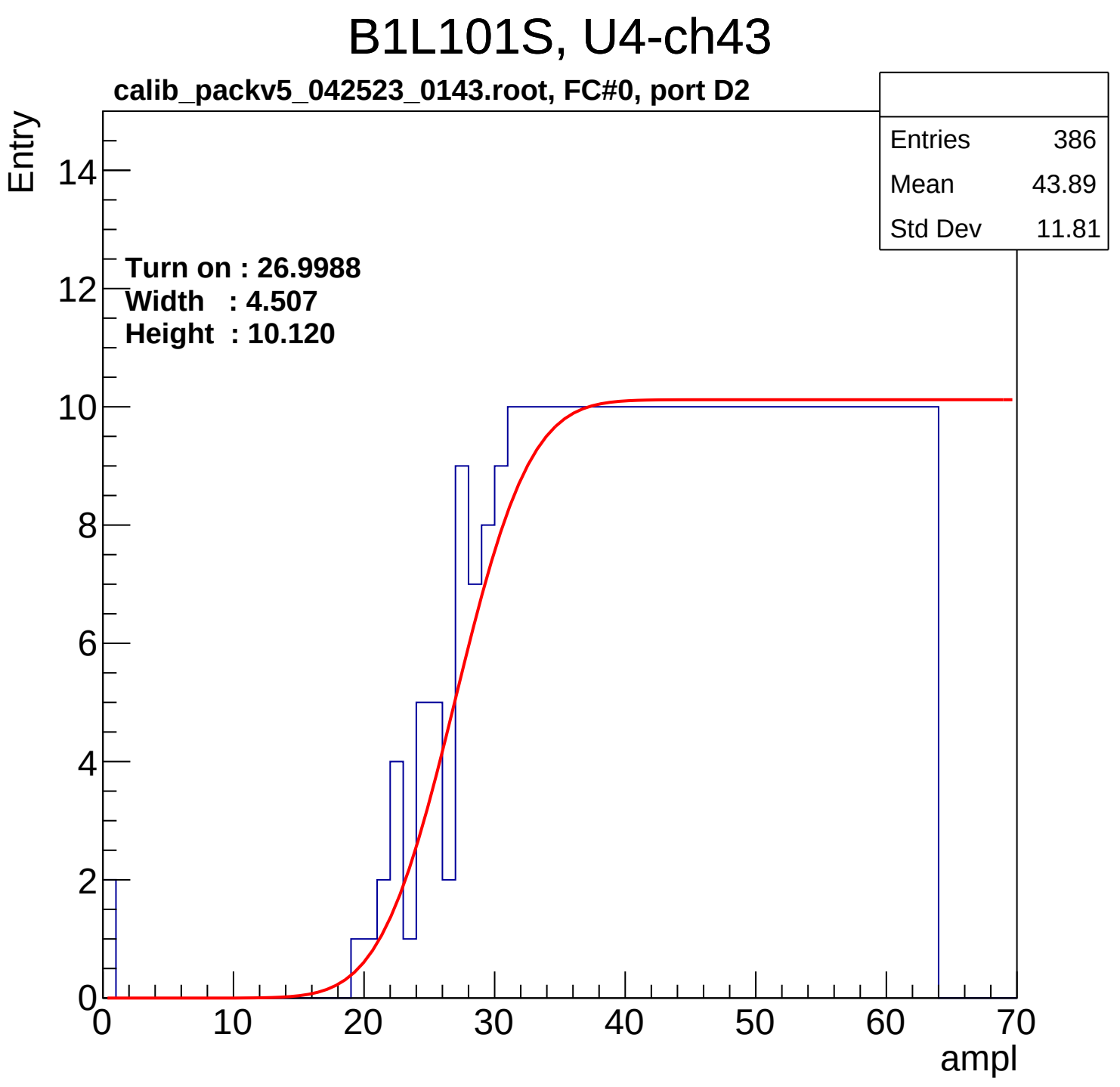

B1L101S, U4-ch38
calib_packv5_042523_0143.root, FC#0, port D2
Entries 392
Mean 43.45
Std Dev 12.36
Turn on : 25.7861
Width : 3.946
Height : 10.045
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

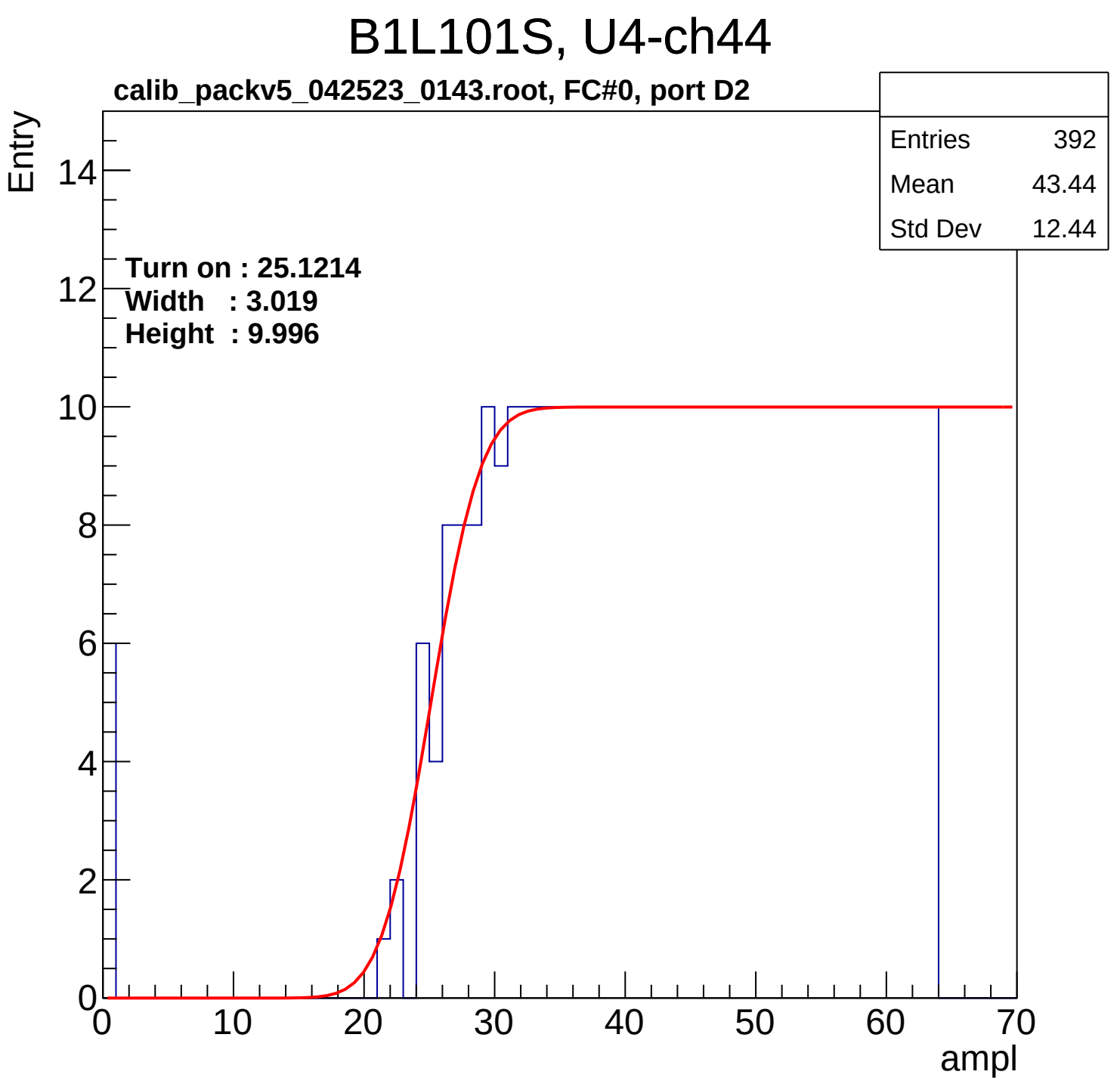

B1L101S, U4-ch39
calib_packv5_042523_0143.root, FC#0, port D2
Entries 379
Mean 44.24
Std Dev 11.69
Turn on : 26.3295
Width : 2.800
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

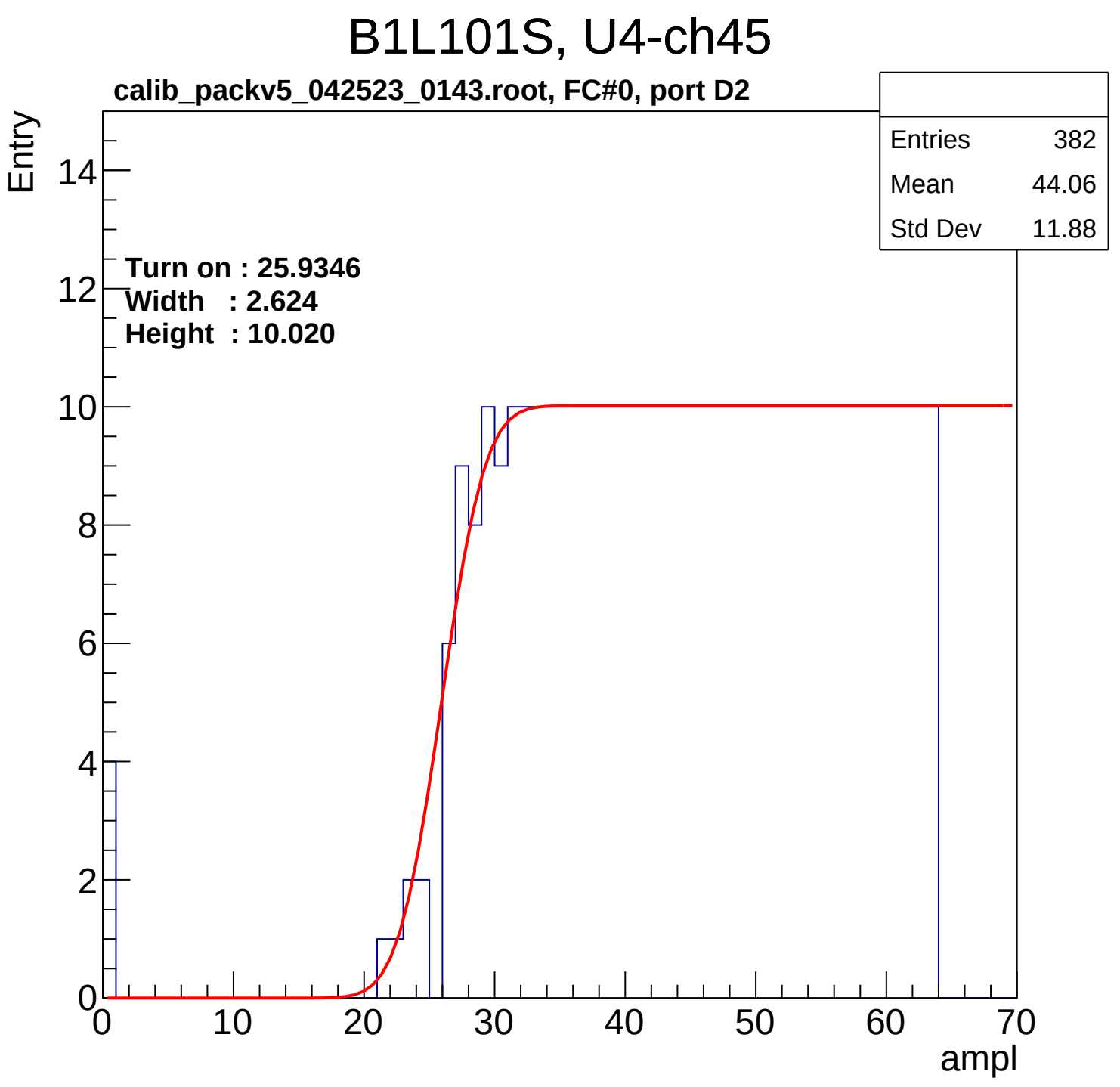

B1L101S, U4-ch40
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.48
Std Dev 11.94
Turn on : 27.9683
Width : 3.763
Height : 10.053
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

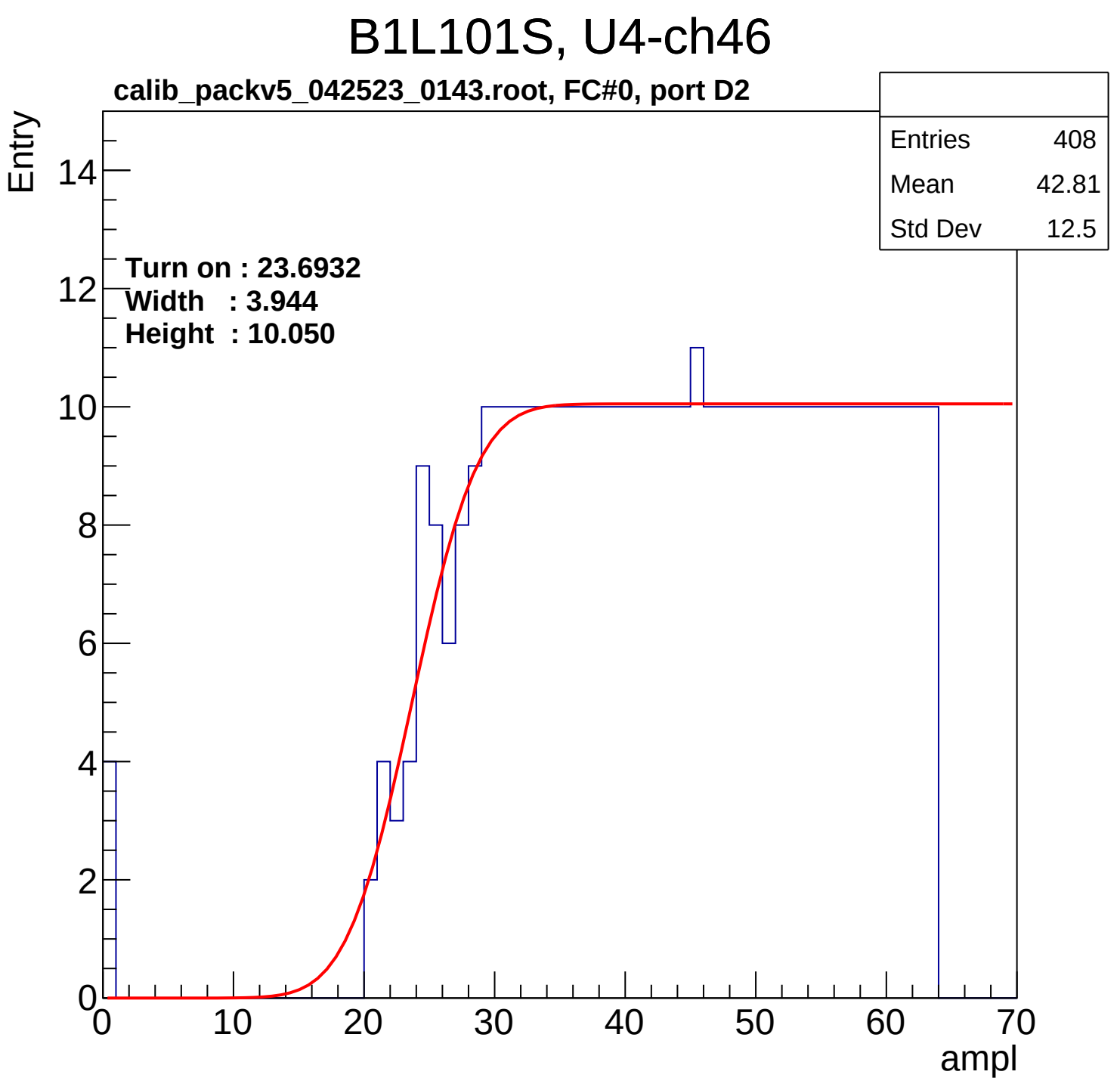

B1L101S, U4-ch41
calib_packv5_042523_0143.root, FC#0, port D2
Entries 394
Mean 43.51
Std Dev 12.05
Turn on : 25.3465
Width : 3.247
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

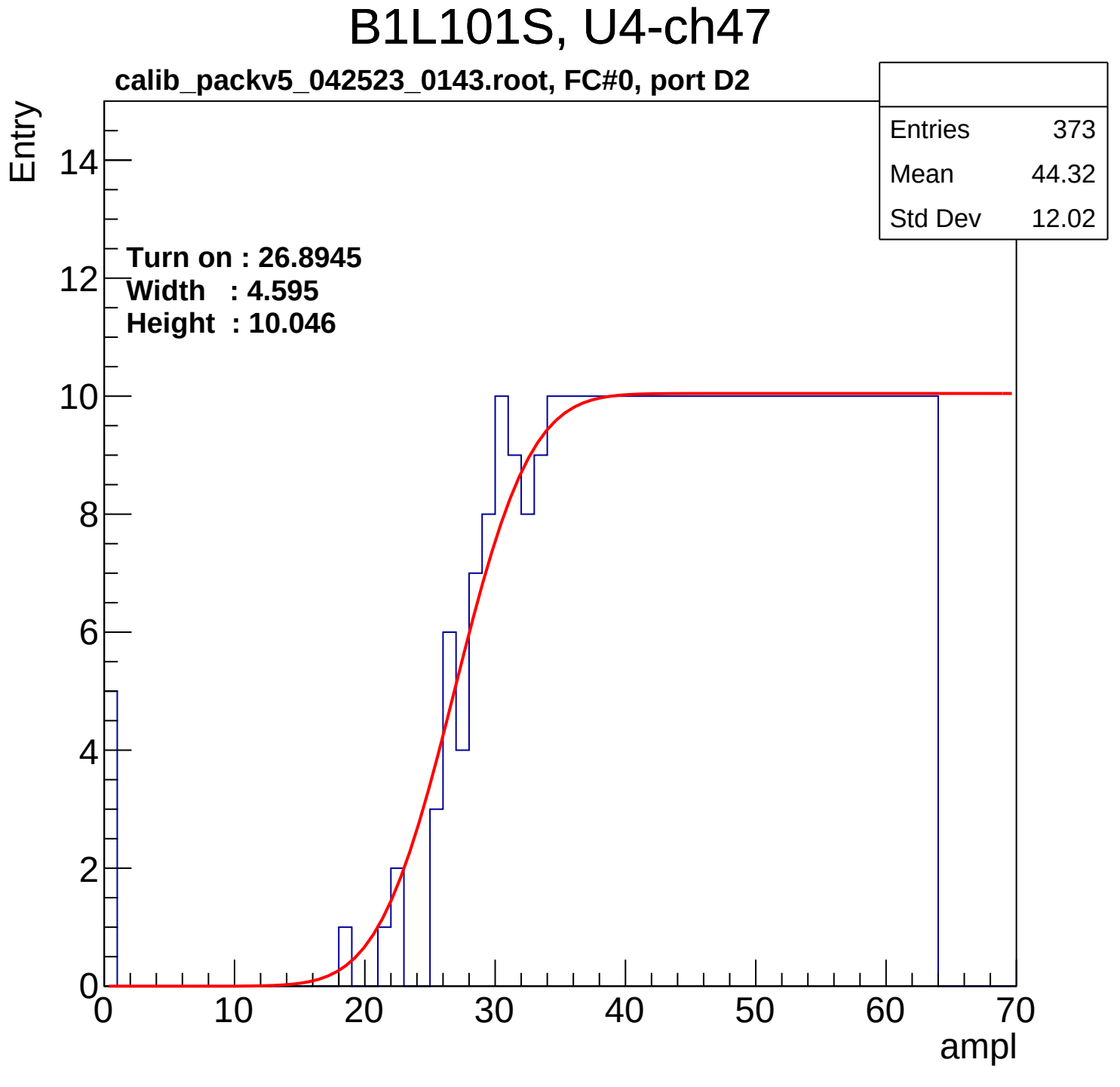

B1L101S, U4-ch42
calib_packv5_042523_0143.root, FC#0, port D2
Entries 390
Mean 43.39
Std Dev 12.73
Turn on : 25.7476
Width : 3.164
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

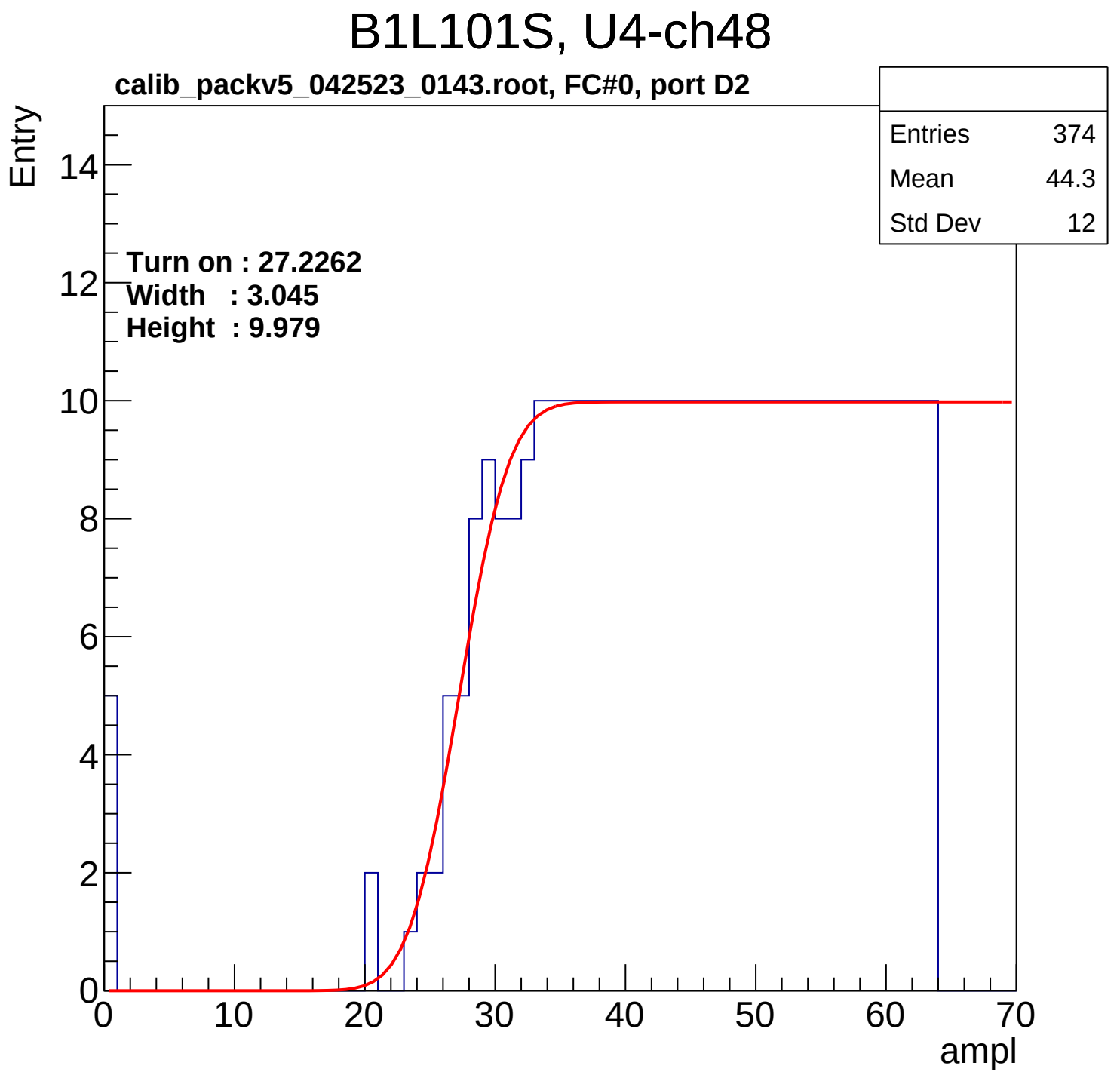

B1L101S, U4-ch43
calib_packv5_042523_0143.root, FC#0, port D2
Entries 386
Mean 43.89
Std Dev 11.81
Turn on : 26.9988
Width : 4.507
Height : 10.120
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

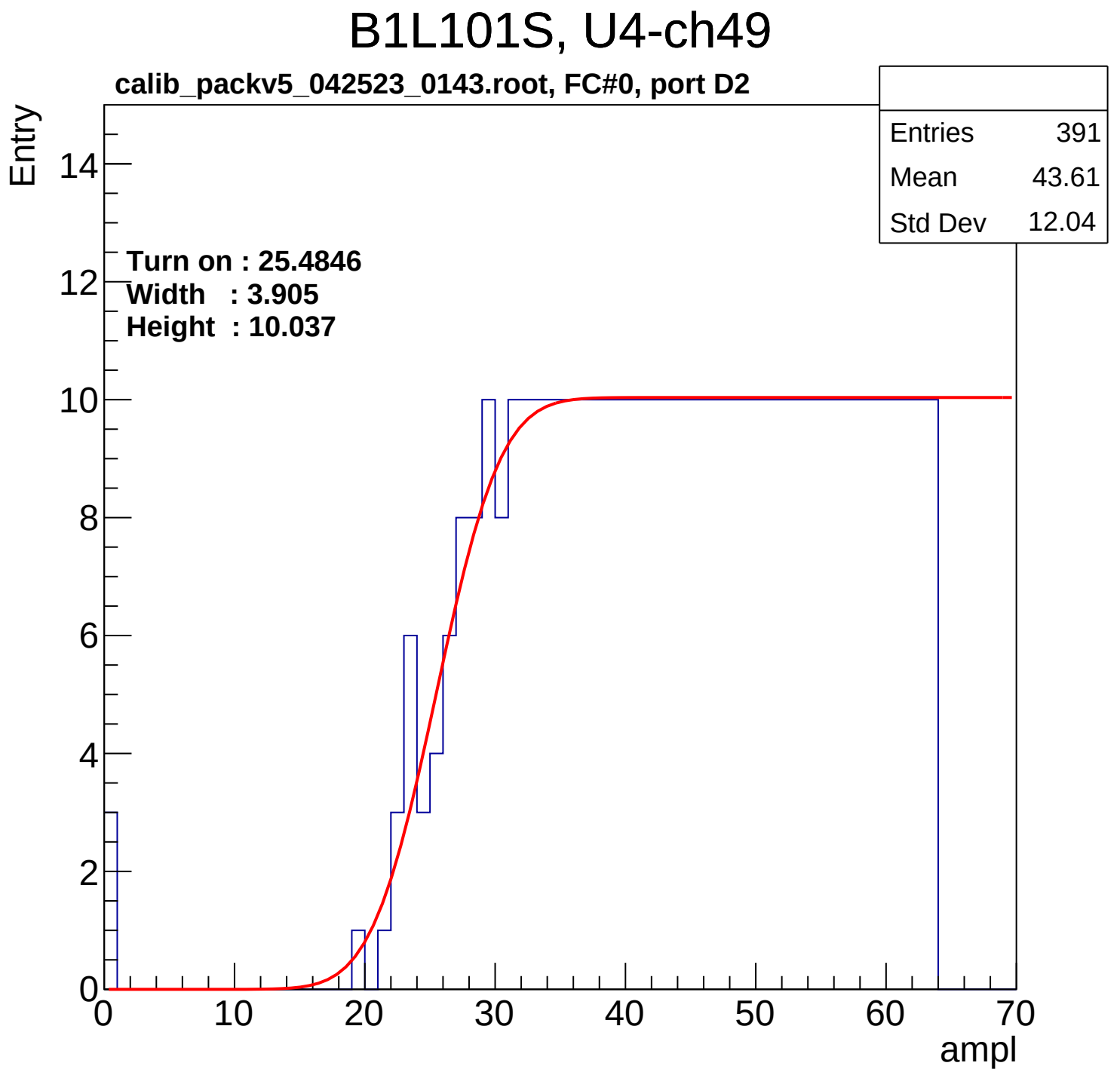

B1L101S, U4-ch44
calib_packv5_042523_0143.root, FC#0, port D2
Entries 392
Mean 43.44
Std Dev 12.44
Turn on : 25.1214
Width : 3.019
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

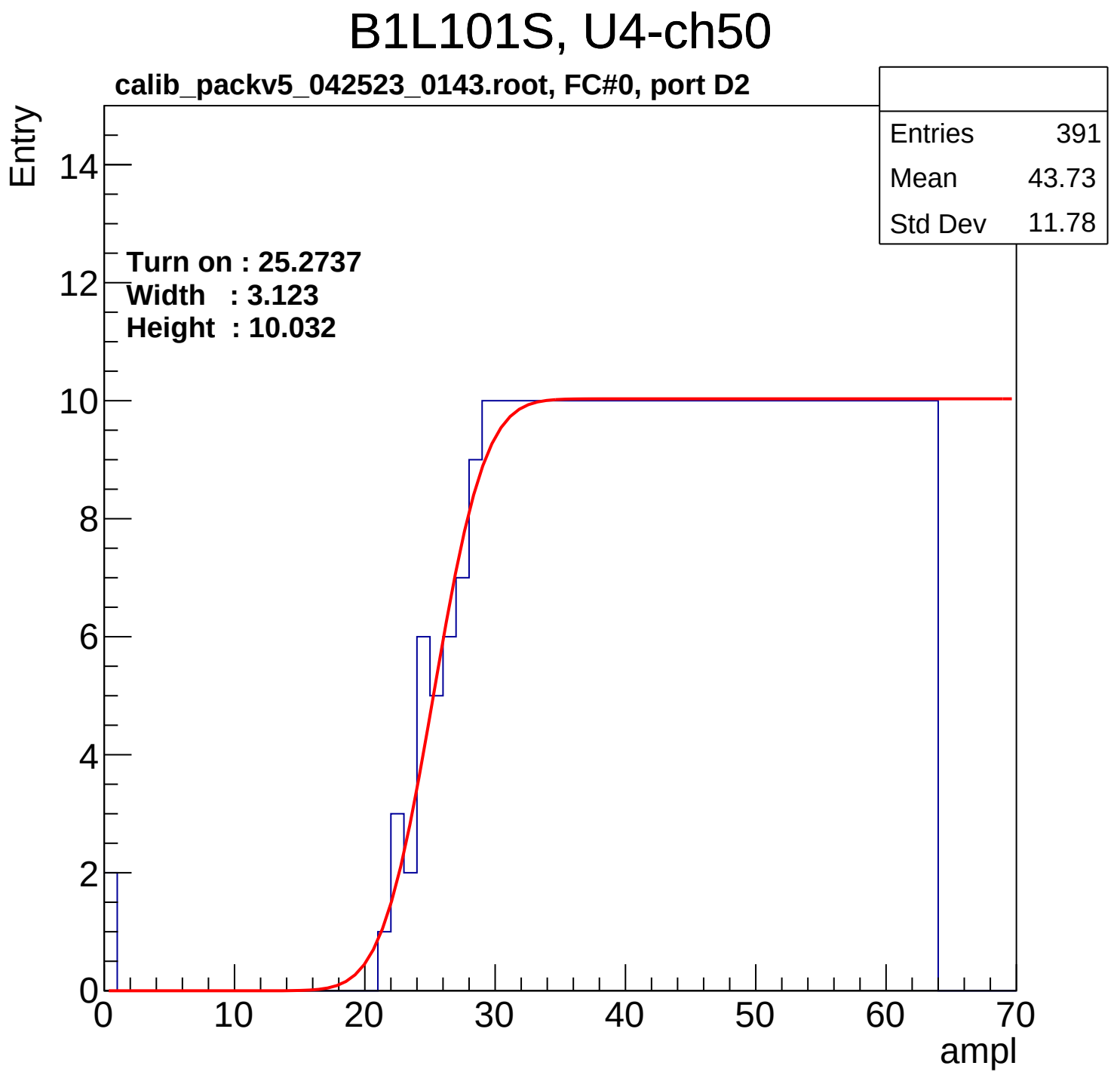

B1L101S, U4-ch45
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 44.06
Std Dev 11.88
Turn on : 25.9346
Width : 2.624
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

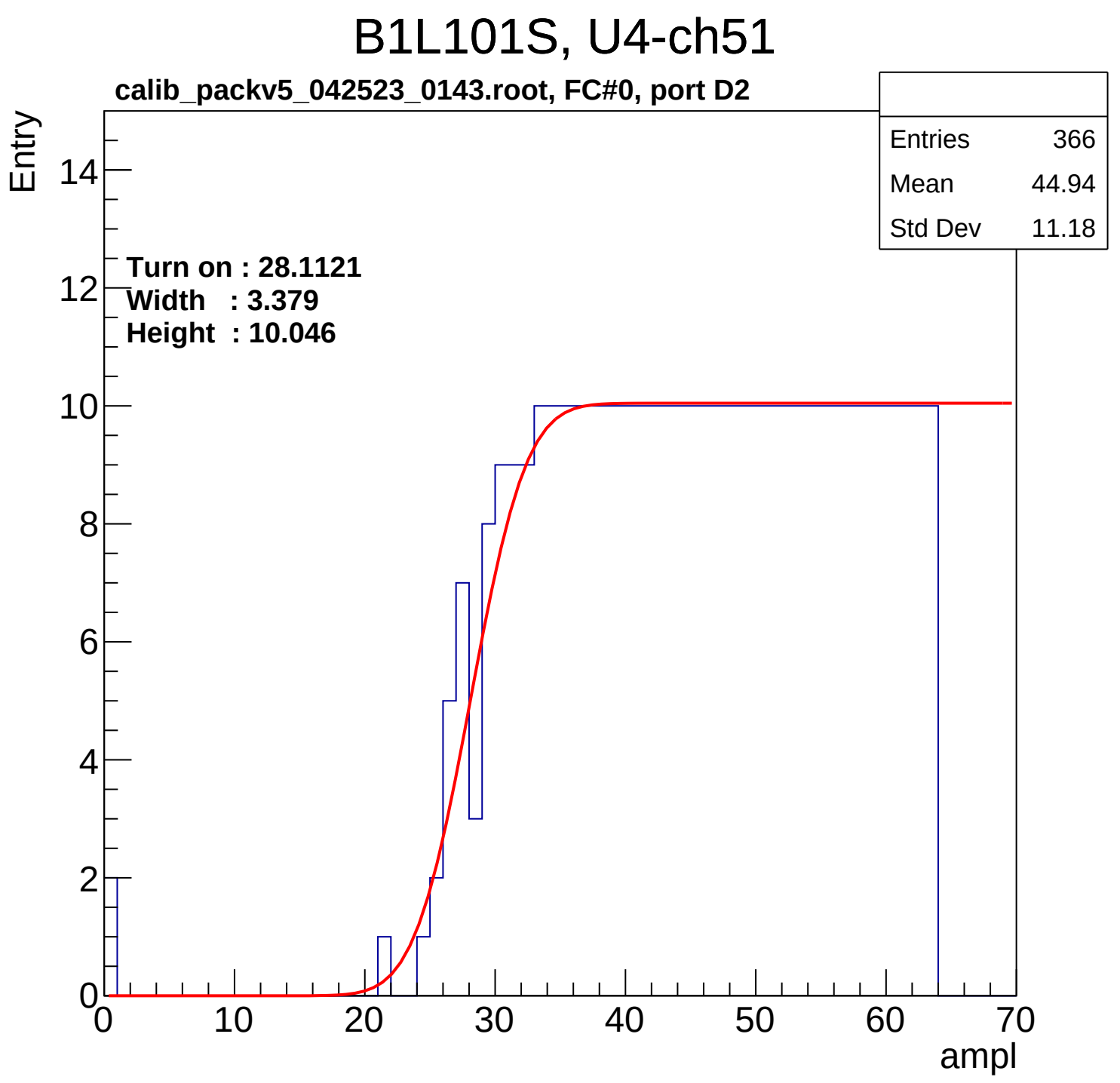

B1L101S, U4-ch46
calib_packv5_042523_0143.root, FC#0, port D2
Entries 408
Mean 42.81
Std Dev 12.5
Turn on : 23.6932
Width : 3.944
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

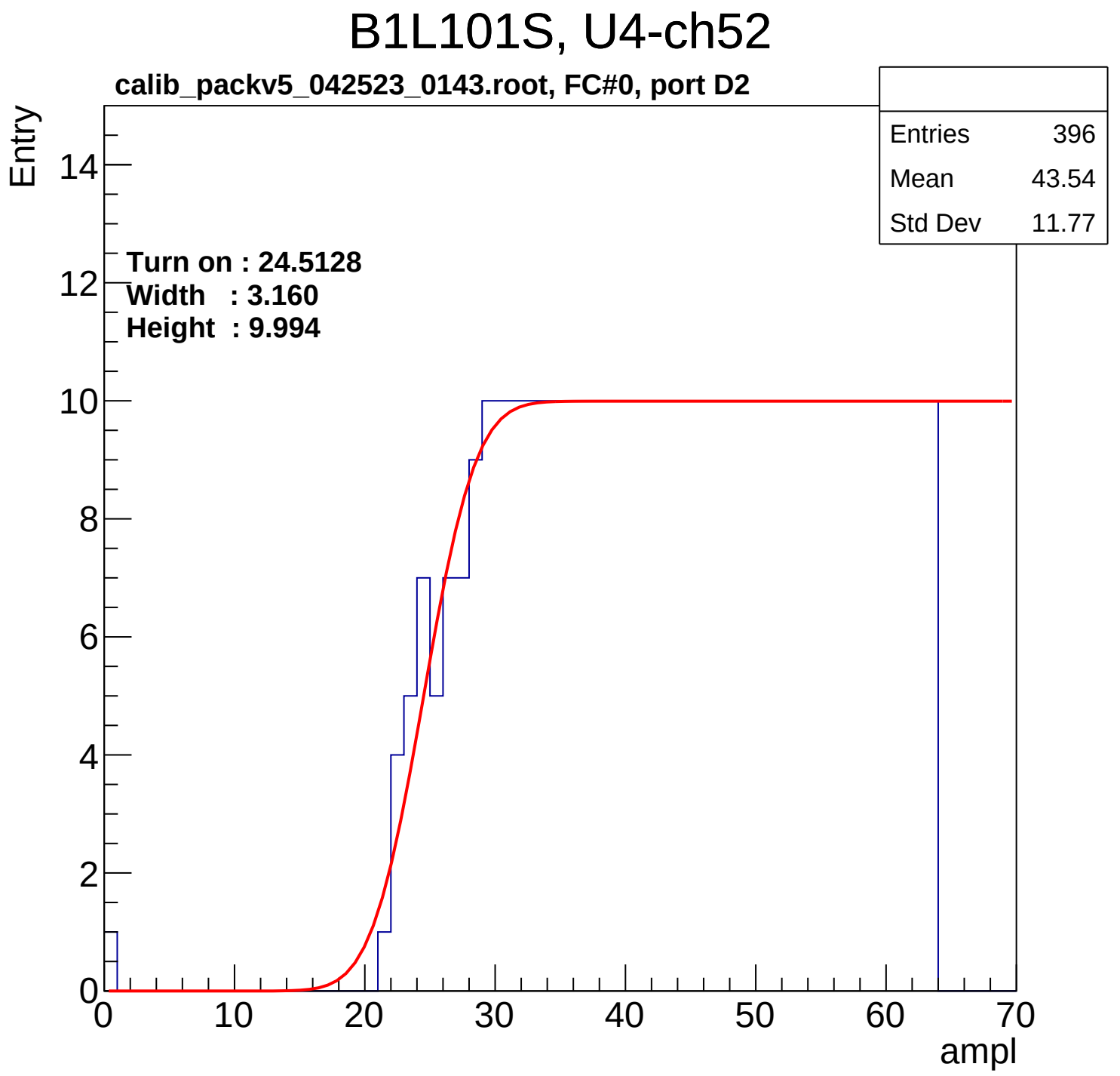

B1L101S, U4-ch47
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.32
Std Dev 12.02
Turn on : 26.8945
Width : 4.595
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

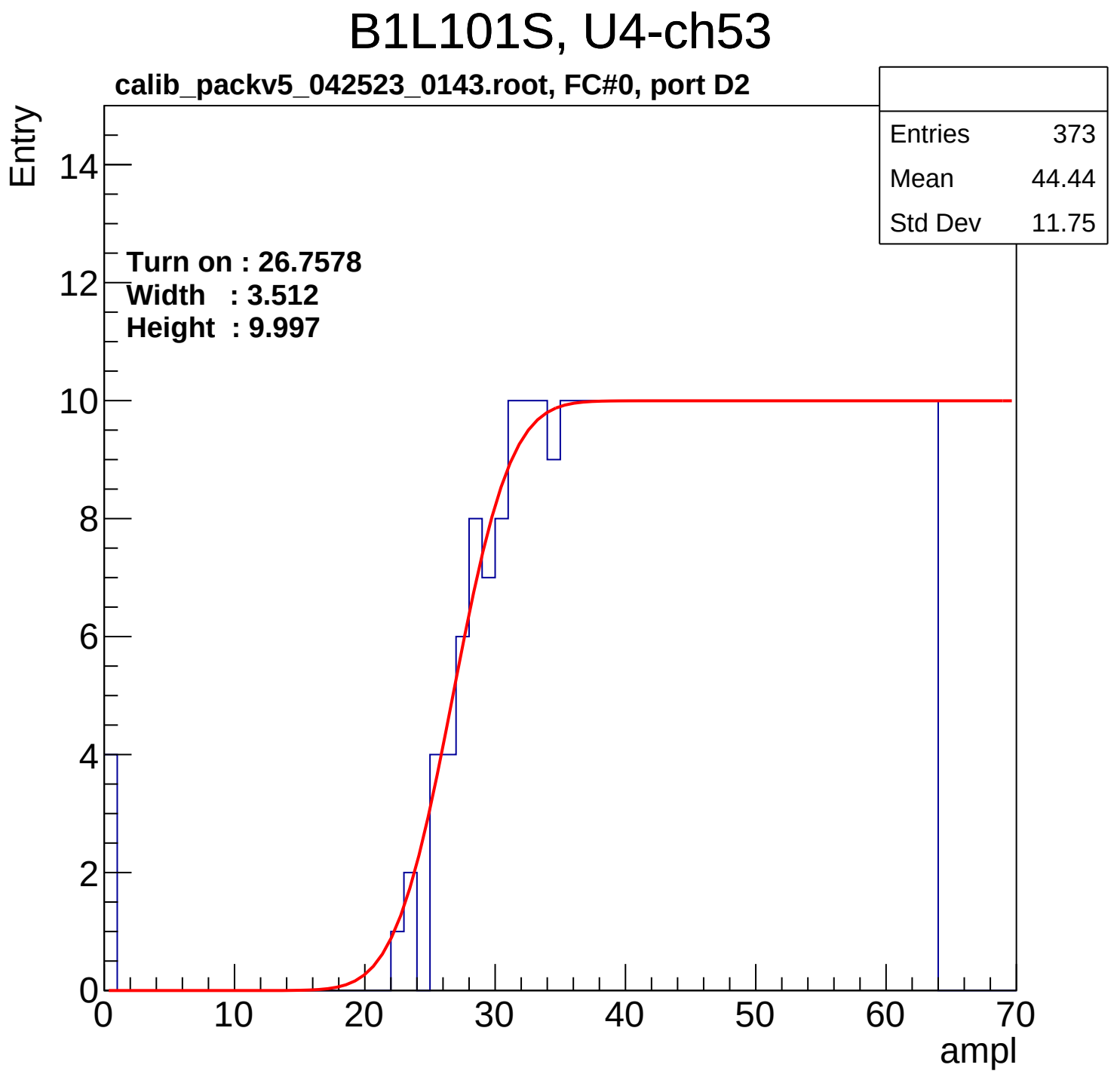

B1L101S, U4-ch48
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.3
Std Dev 12
Turn on : 27.2262
Width : 3.045
Height : 9.979
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

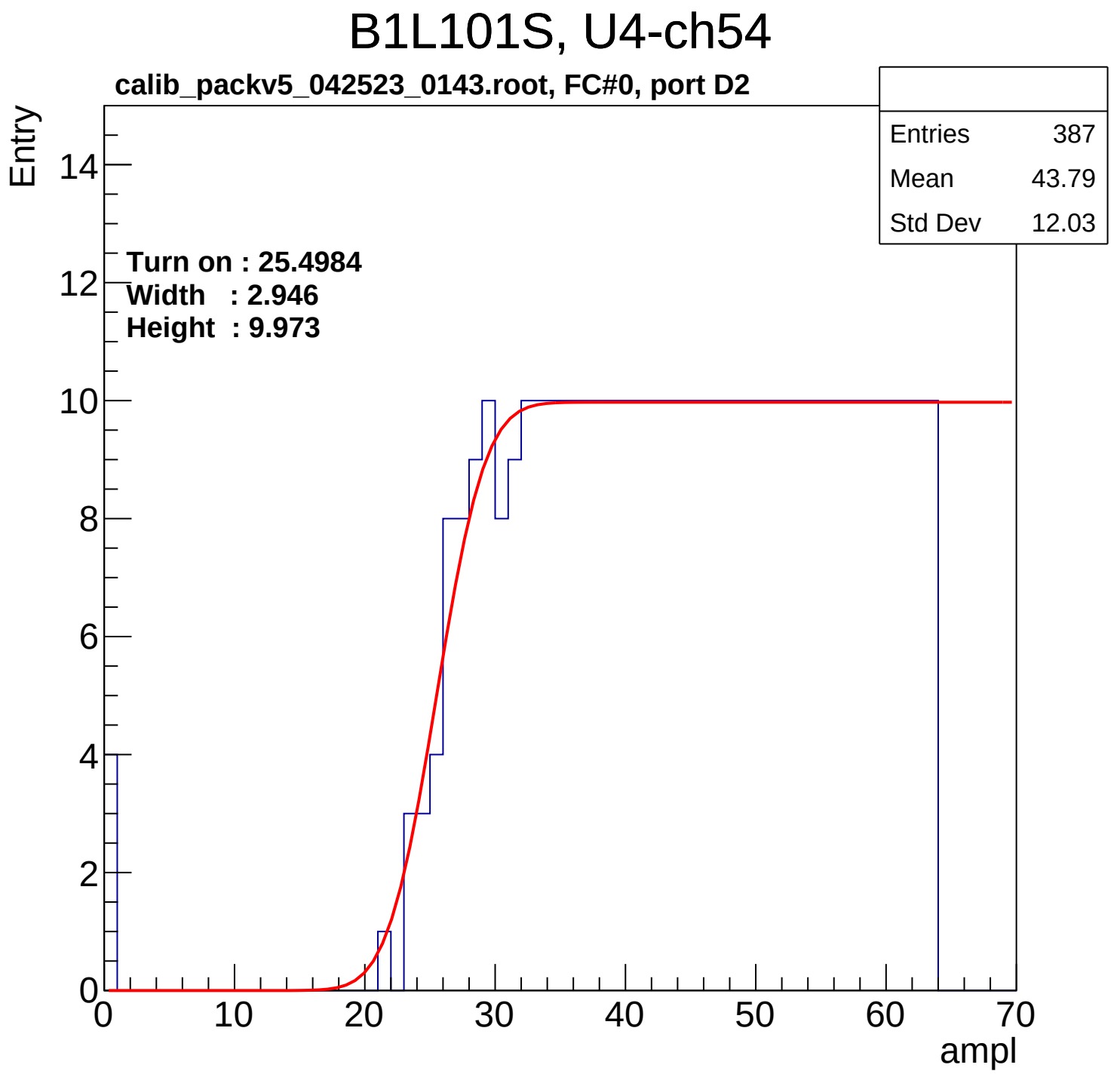

B1L101S, U4-ch49
calib_packv5_042523_0143.root, FC#0, port D2
Entries 391
Mean 43.61
Std Dev 12.04
Turn on : 25.4846
Width : 3.905
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

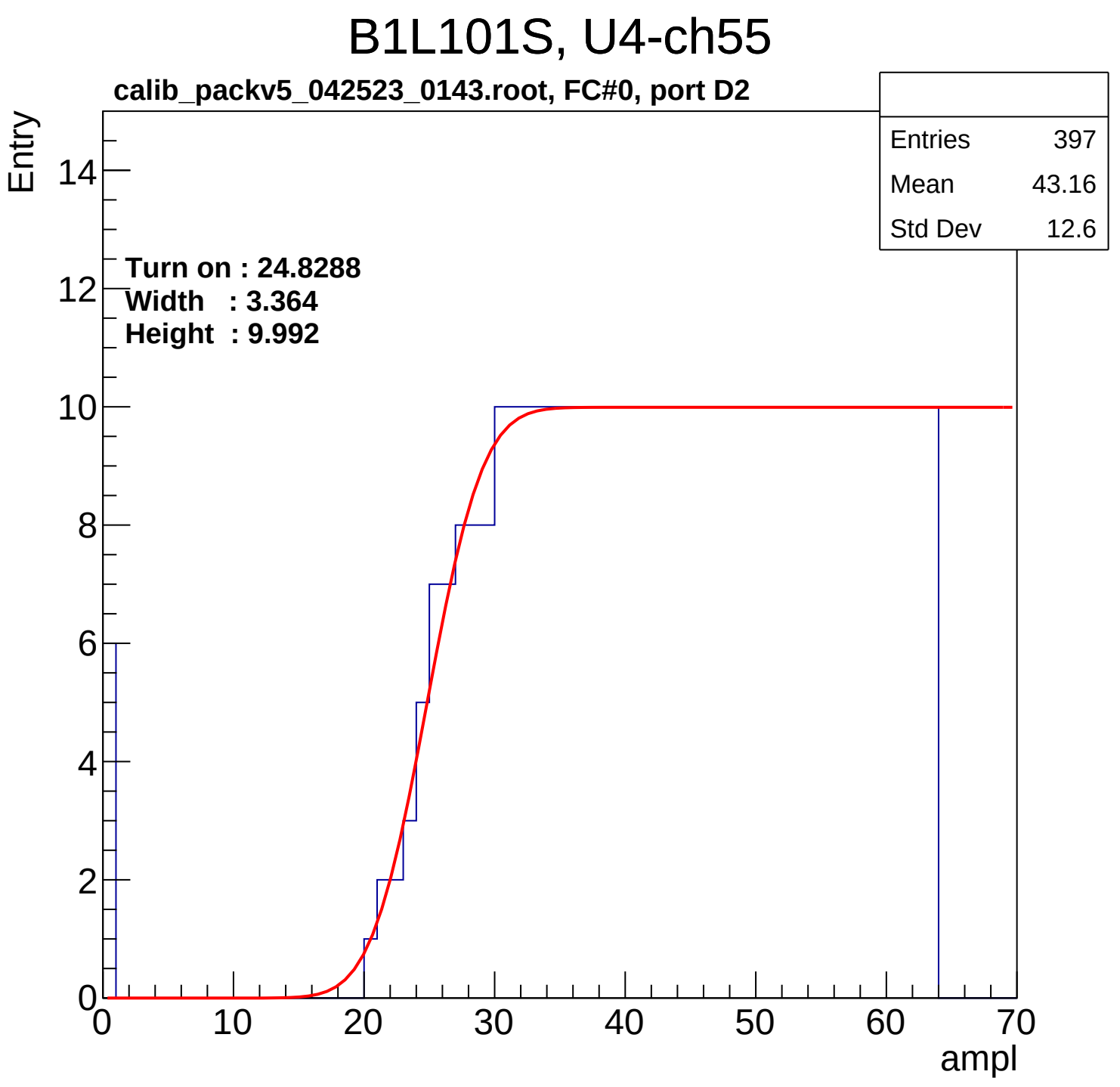

B1L101S, U4-ch50
calib_packv5_042523_0143.root, FC#0, port D2
Entries 391
Mean 43.73
Std Dev 11.78
Turn on : 25.2737
Width : 3.123
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

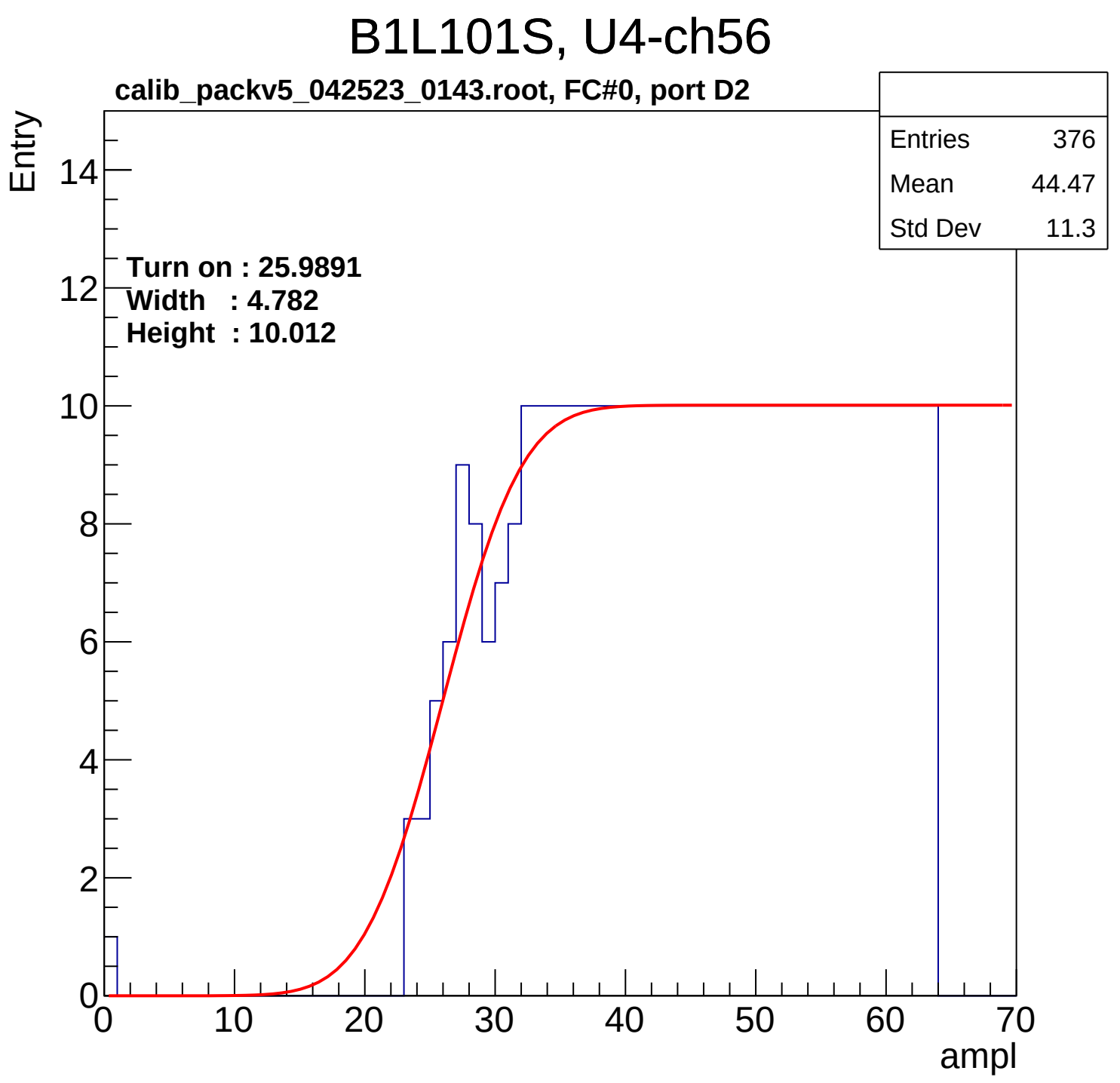

B1L101S, U4-ch51
calib_packv5_042523_0143.root, FC#0, port D2
Entries 366
Mean 44.94
Std Dev 11.18
Turn on : 28.1121
Width : 3.379
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

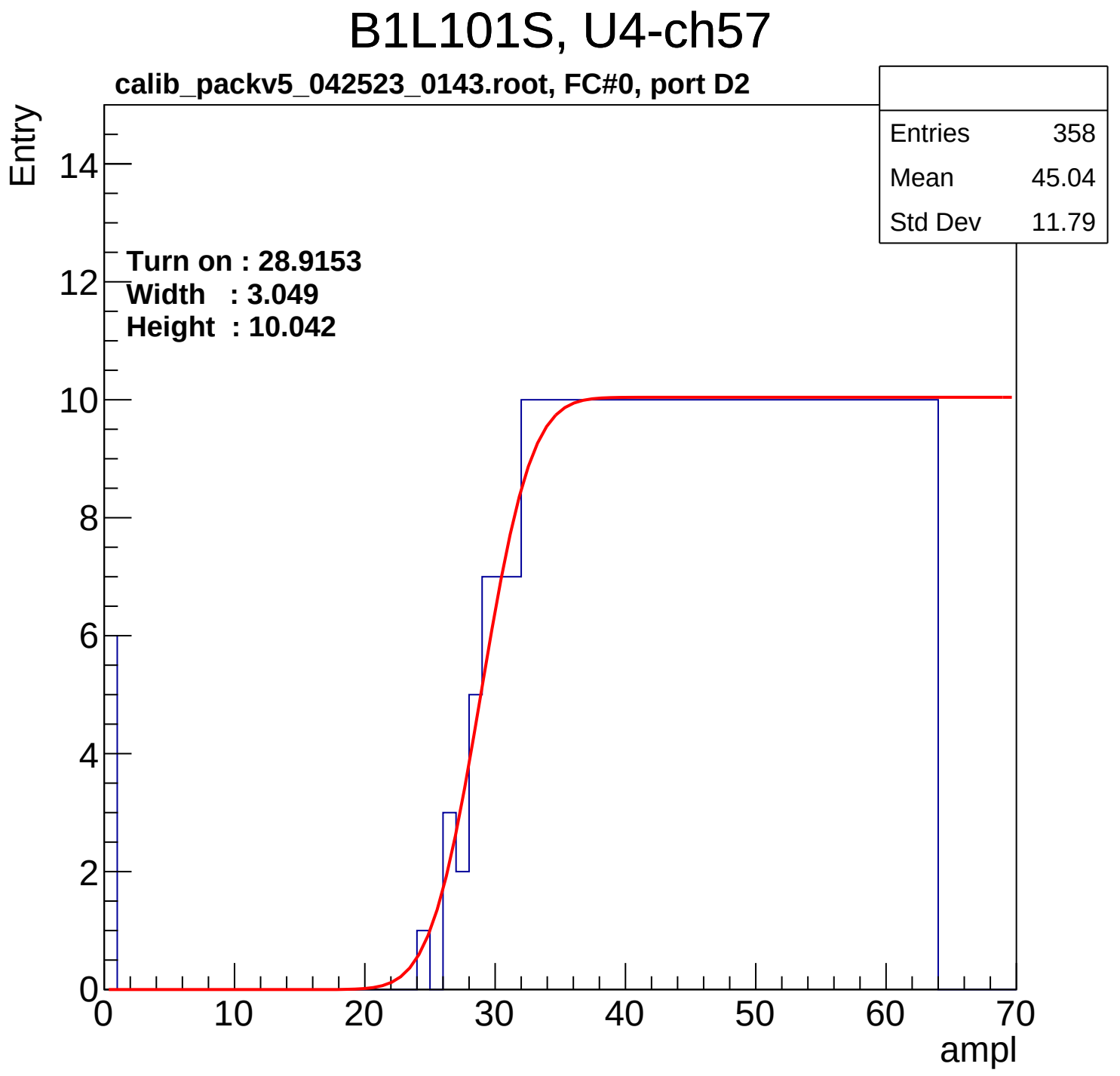

B1L101S, U4-ch52
calib_packv5_042523_0143.root, FC#0, port D2
Entries 396
Mean 43.54
Std Dev 11.77
Turn on : 24.5128
Width : 3.160
Height : 9.994
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

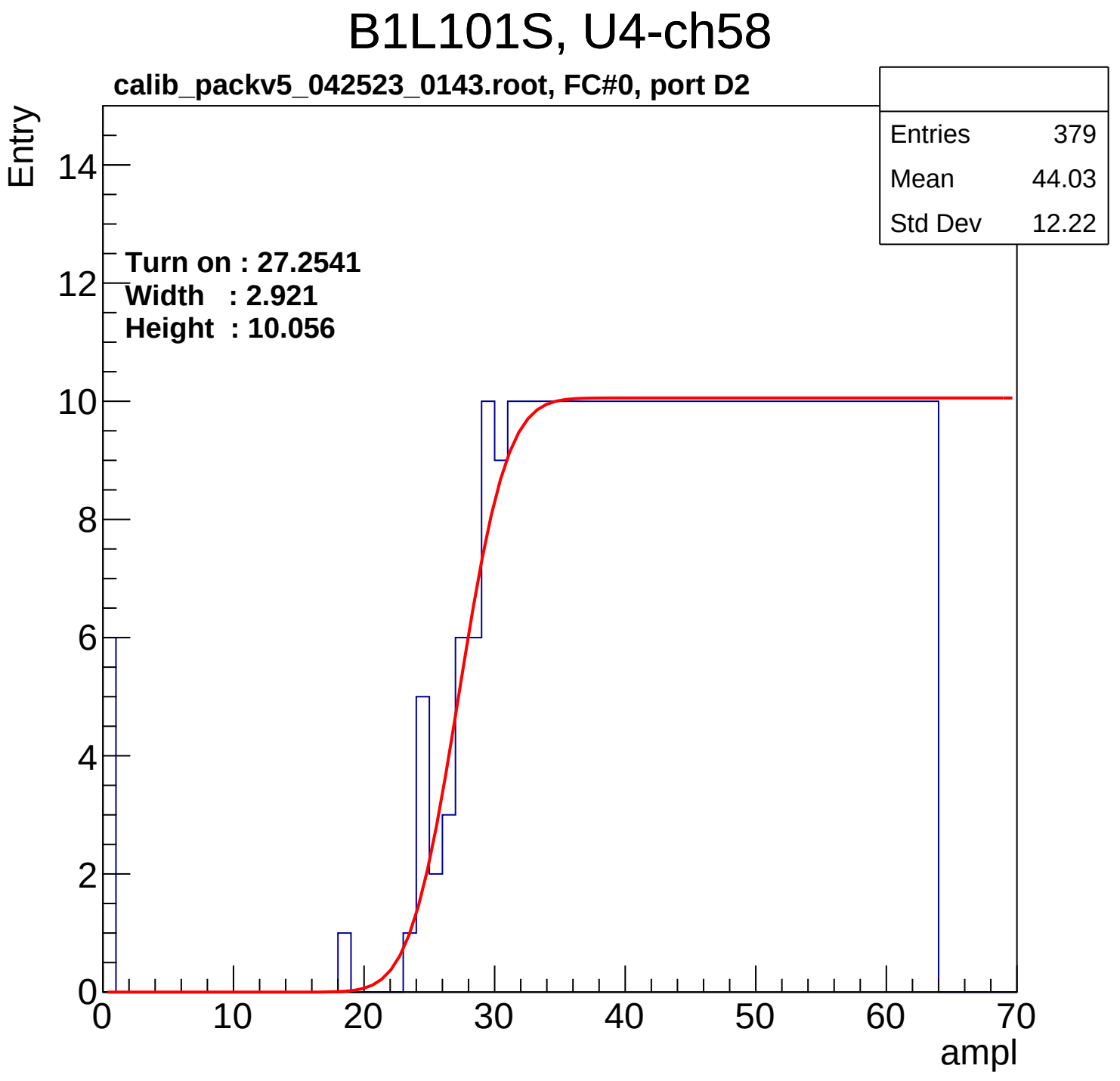

B1L101S, U4-ch53
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.44
Std Dev 11.75
Turn on : 26.7578
Width : 3.512
Height : 9.997
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

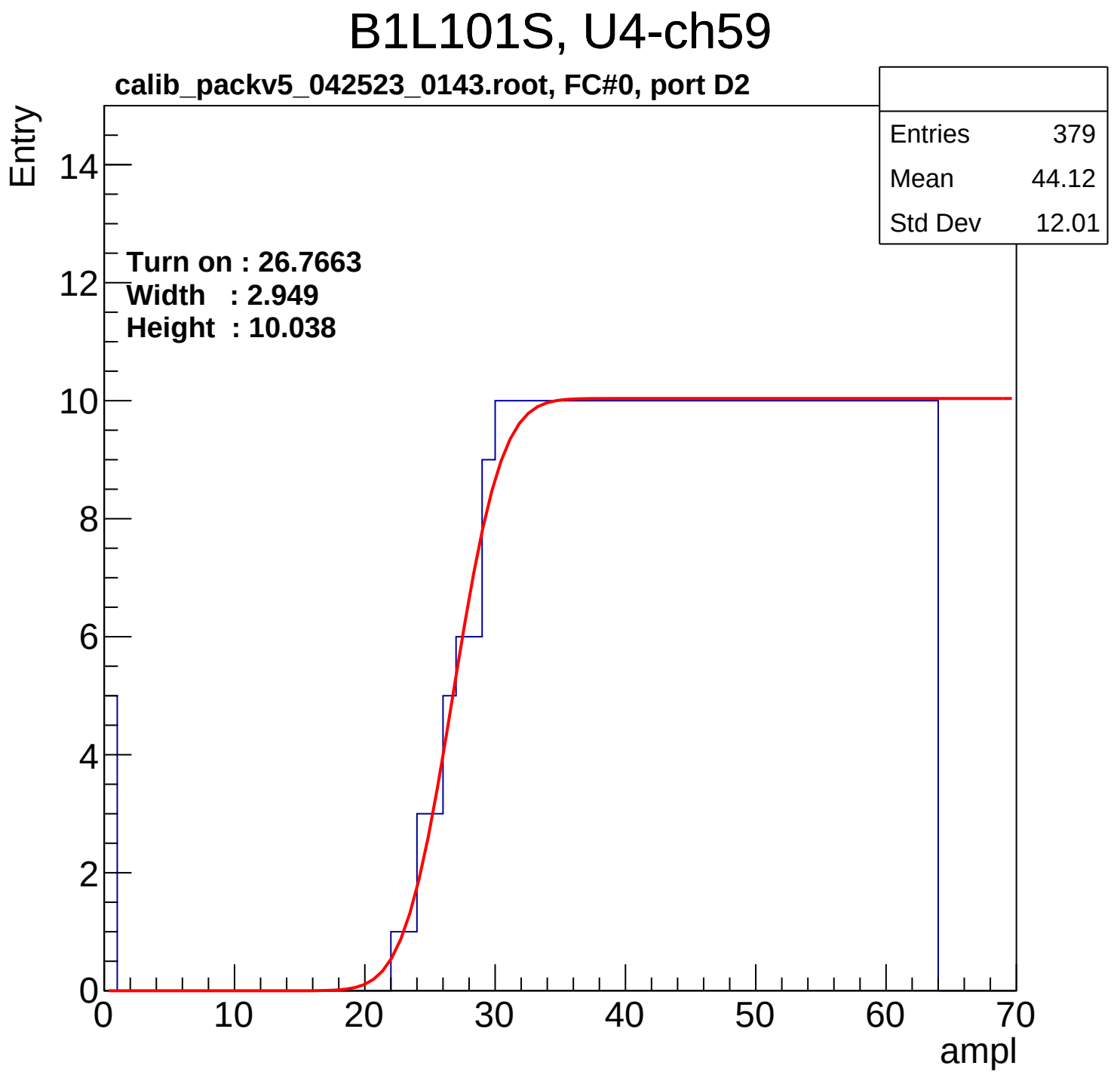

B1L101S, U4-ch54
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.79
Std Dev 12.03
Turn on : 25.4984
Width : 2.946
Height : 9.973
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

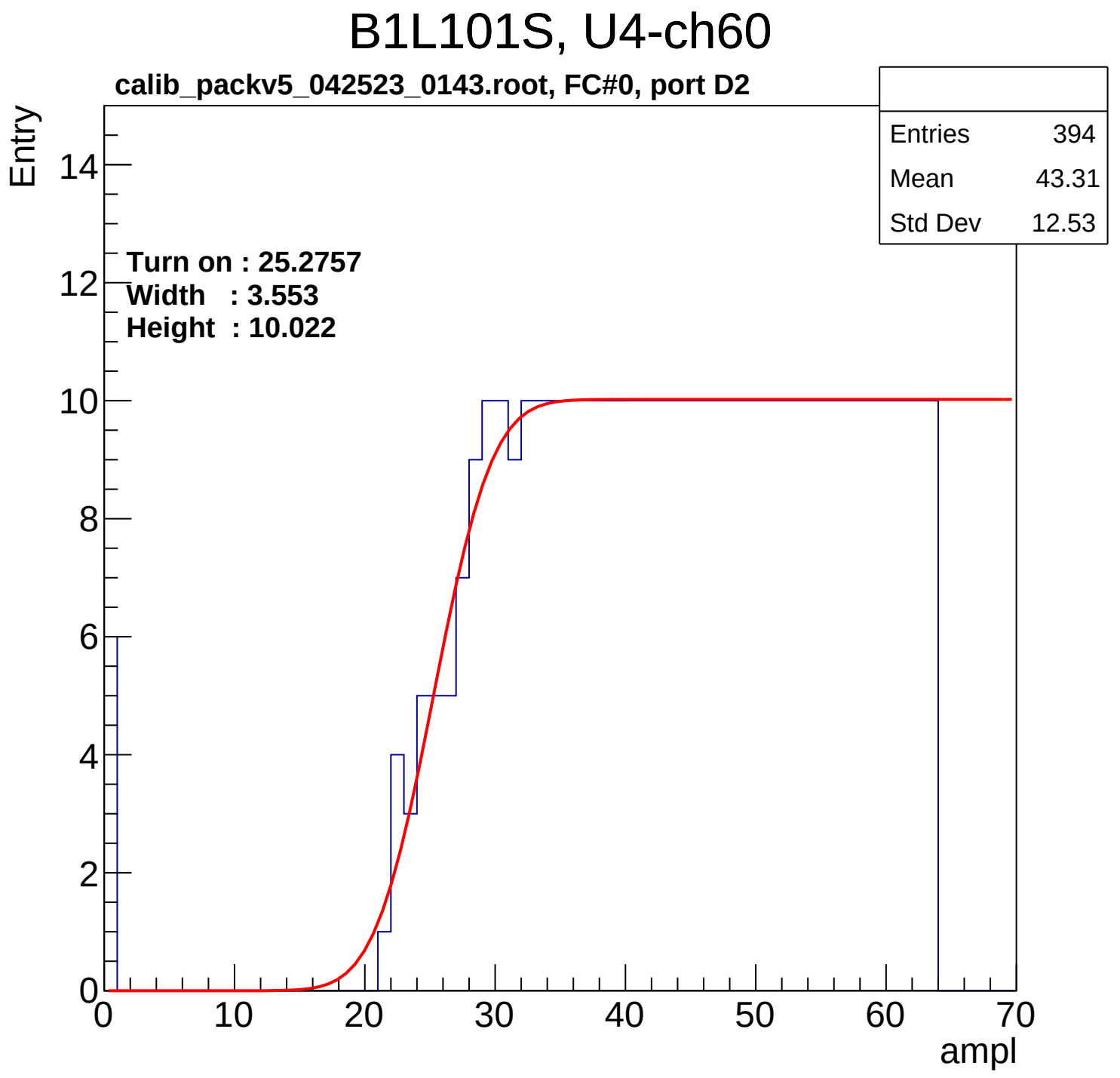

B1L101S, U4-ch55
calib_packv5_042523_0143.root, FC#0, port D2
Entries 397
Mean 43.16
Std Dev 12.6
Turn on : 24.8288
Width : 3.364
Height : 9.992
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

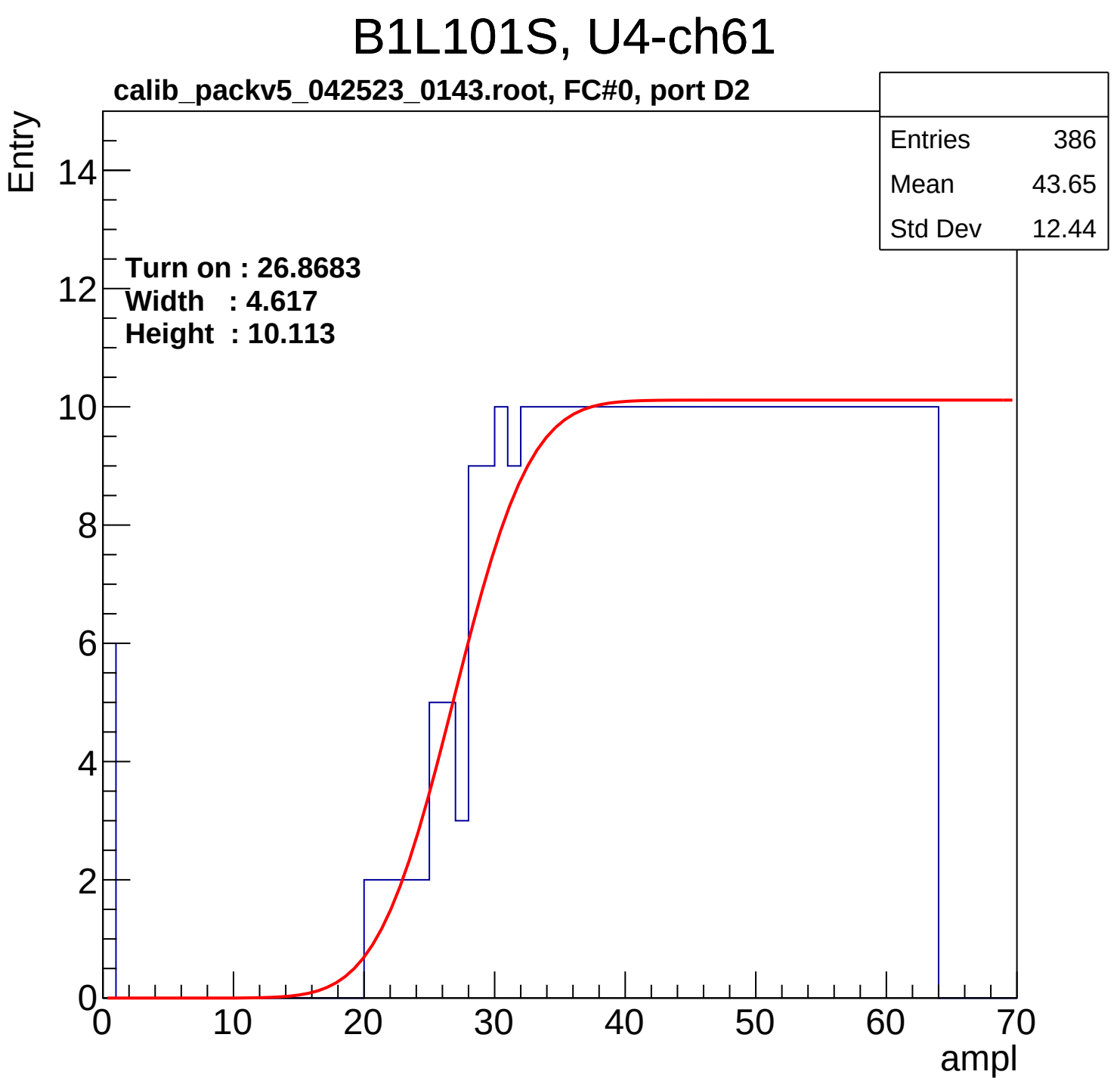

B1L101S, U4-ch56
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.47
Std Dev 11.3
Turn on : 25.9891
Width : 4.782
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

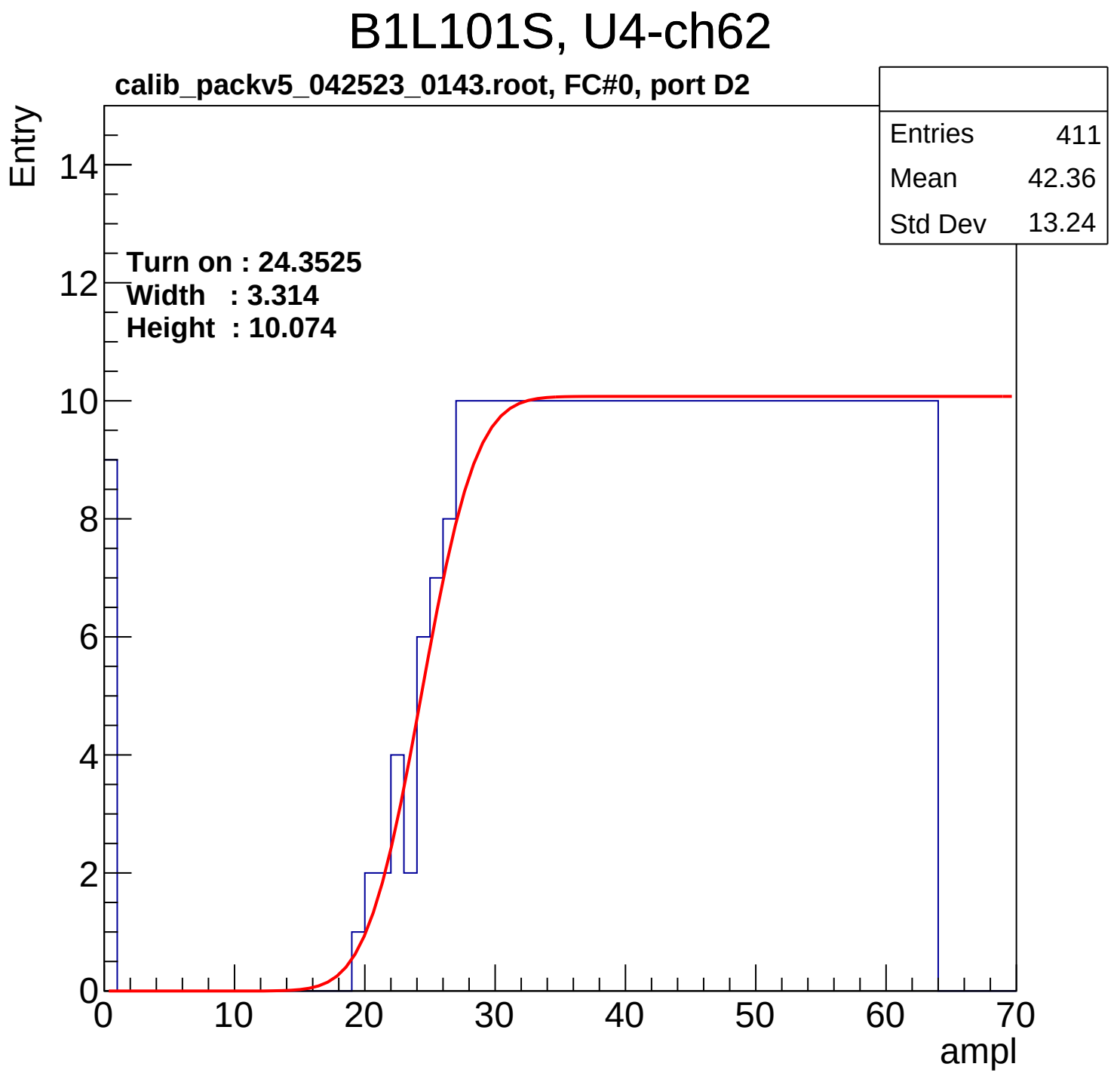

B1L101S, U4-ch57
calib_packv5_042523_0143.root, FC#0, port D2
Entries 358
Mean 45.04
Std Dev 11.79
Turn on : 28.9153
Width : 3.049
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

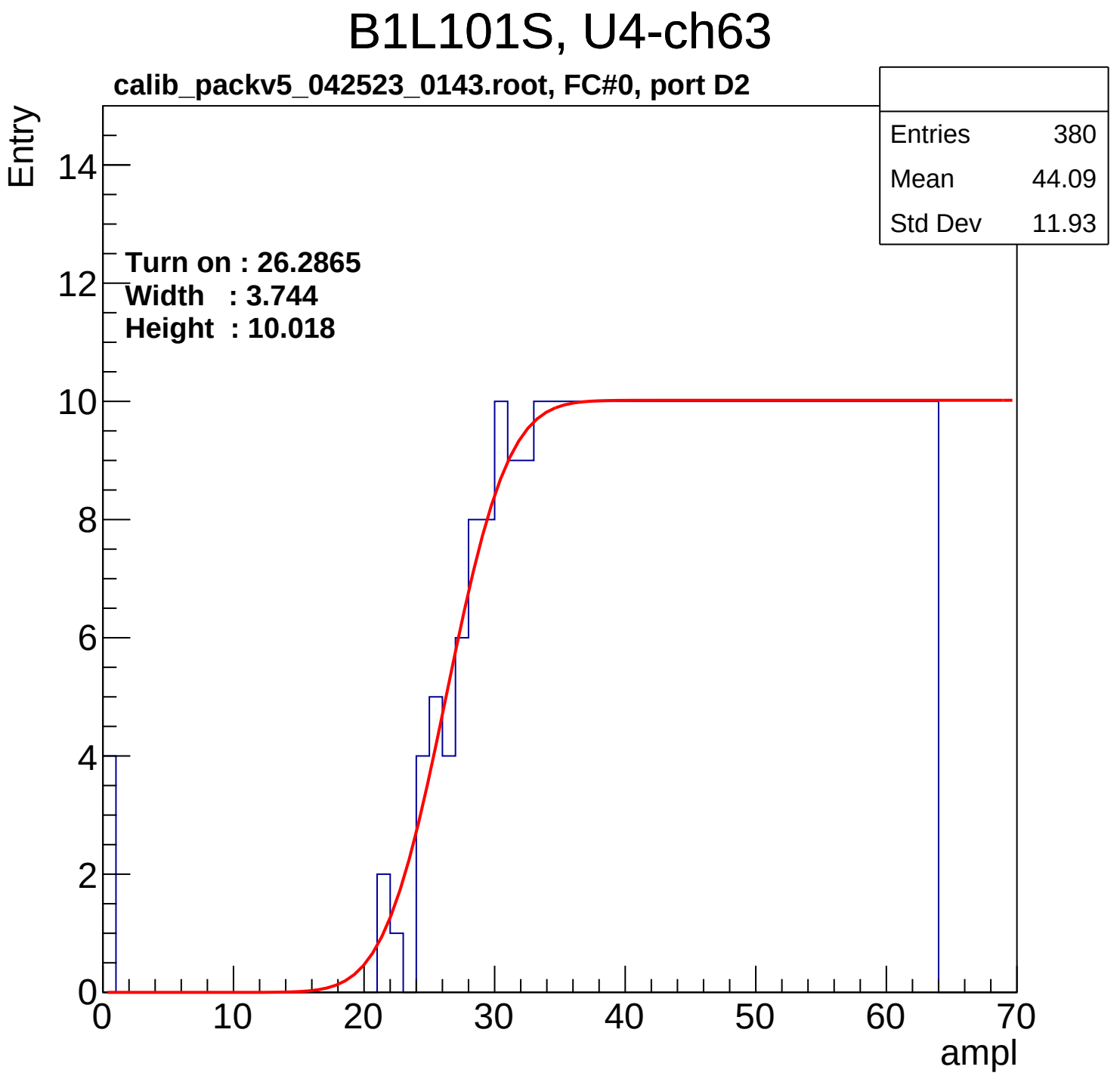

B1L101S, U4-ch58
calib_packv5_042523_0143.root, FC#0, port D2
Entries 379
Mean 44.03
Std Dev 12.22
Turn on : 27.2541
Width : 2.921
Height : 10.056
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

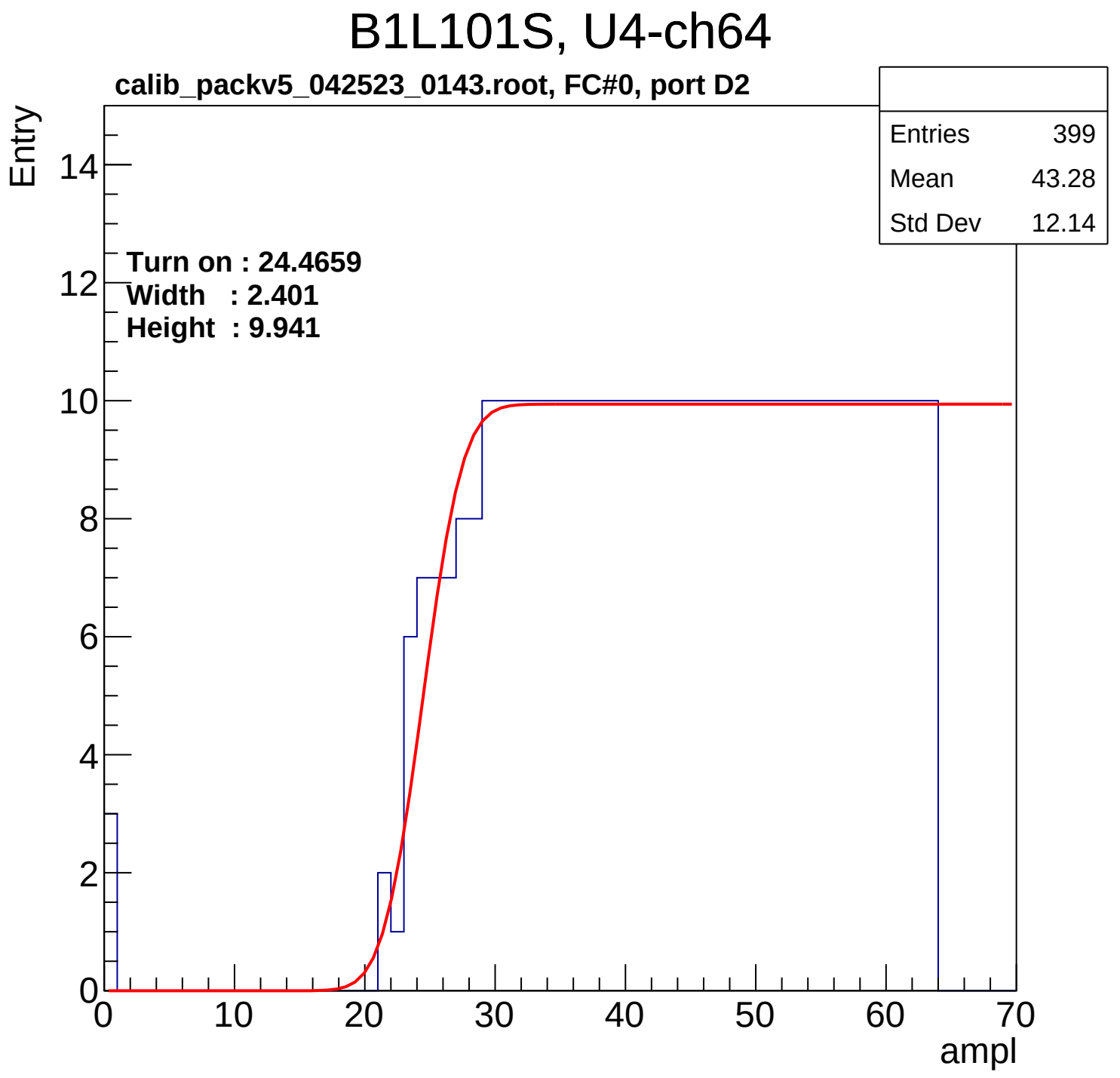

B1L101S, U4-ch59
calib_packv5_042523_0143.root, FC#0, port D2
Entries 379
Mean 44.12
Std Dev 12.01
Turn on : 26.7663
Width : 2.949
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

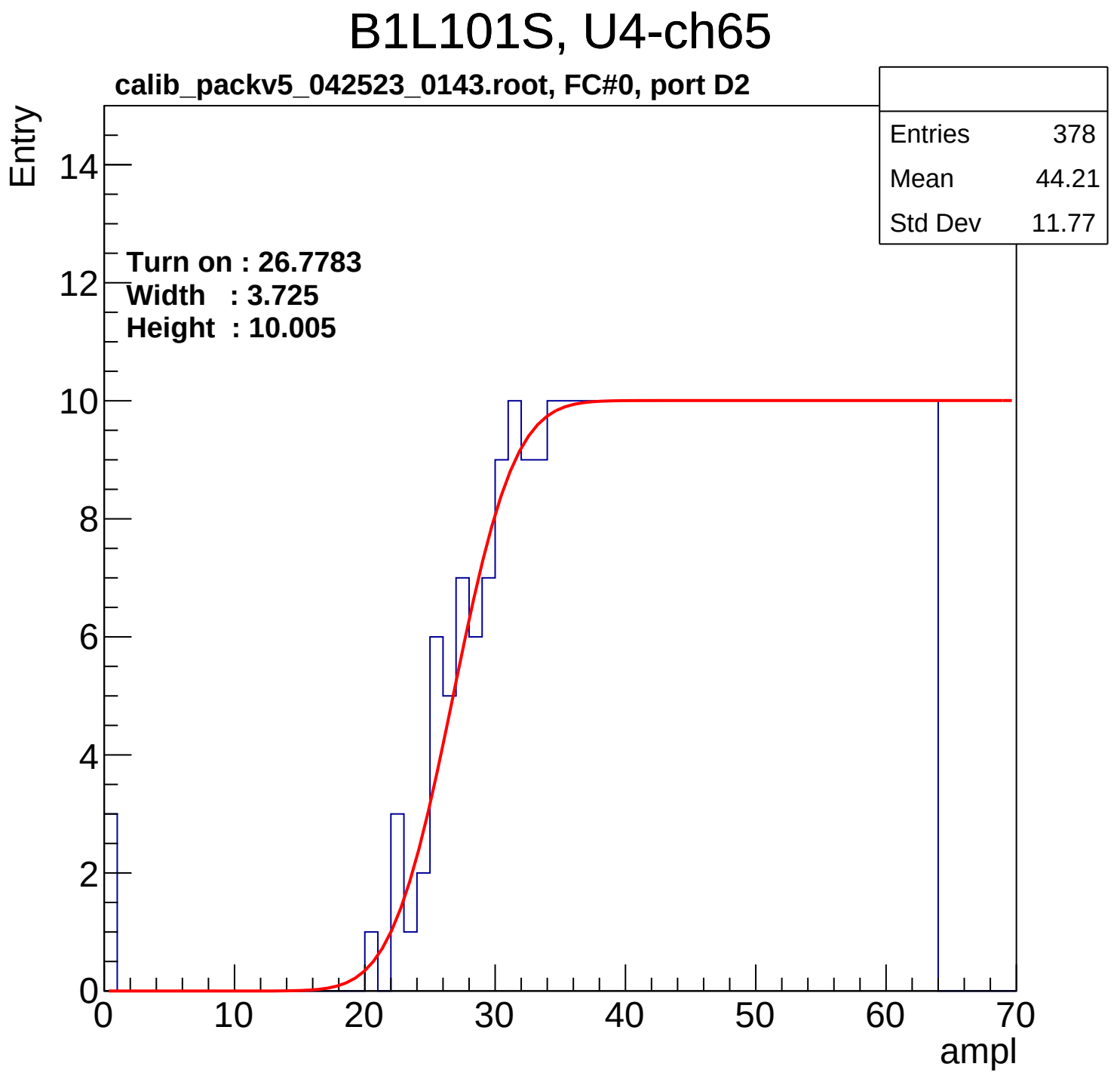

B1L101S, U4-ch60
calib_packv5_042523_0143.root, FC#0, port D2
Entries 394
Mean 43.31
Std Dev 12.53
Turn on : 25.2757
Width : 3.553
Height : 10.022
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

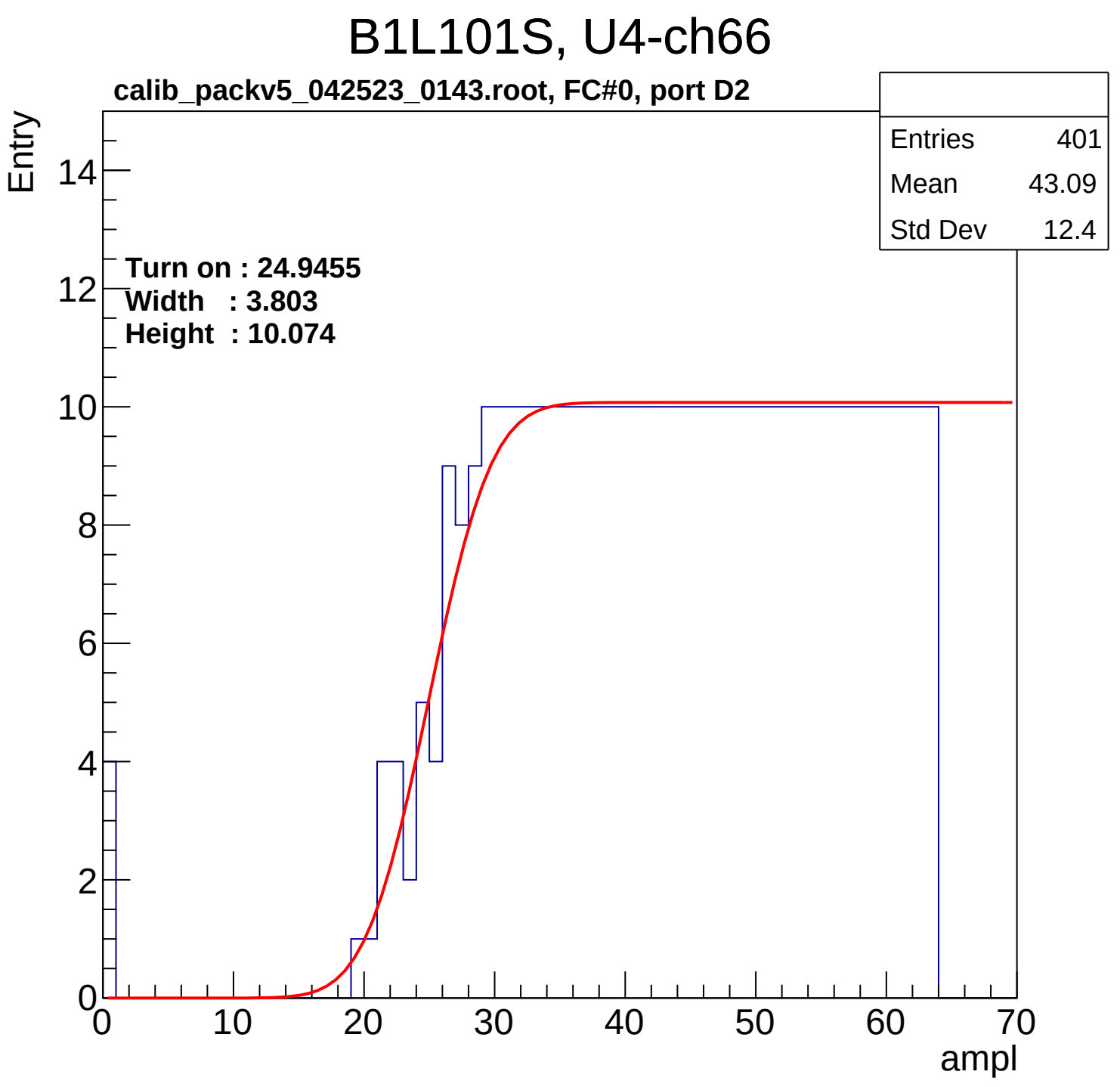

B1L101S, U4-ch61
calib_packv5_042523_0143.root, FC#0, port D2
Entries 386
Mean 43.65
Std Dev 12.44
Turn on : 26.8683
Width : 4.617
Height : 10.113
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

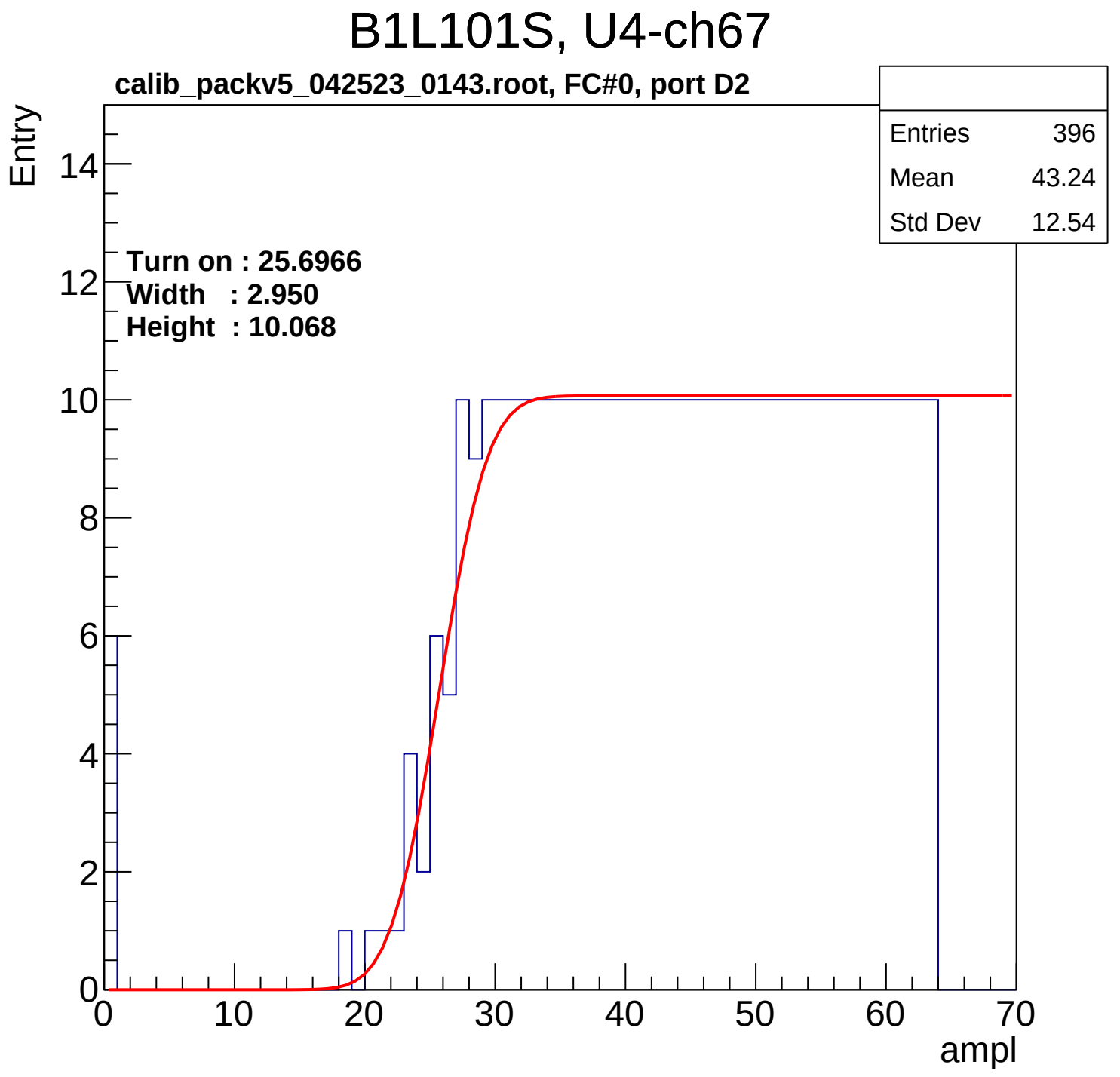

B1L101S, U4-ch62
calib_packv5_042523_0143.root, FC#0, port D2
Entries 411
Mean 42.36
Std Dev 13.24
Turn on : 24.3525
Width : 3.314
Height : 10.074
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

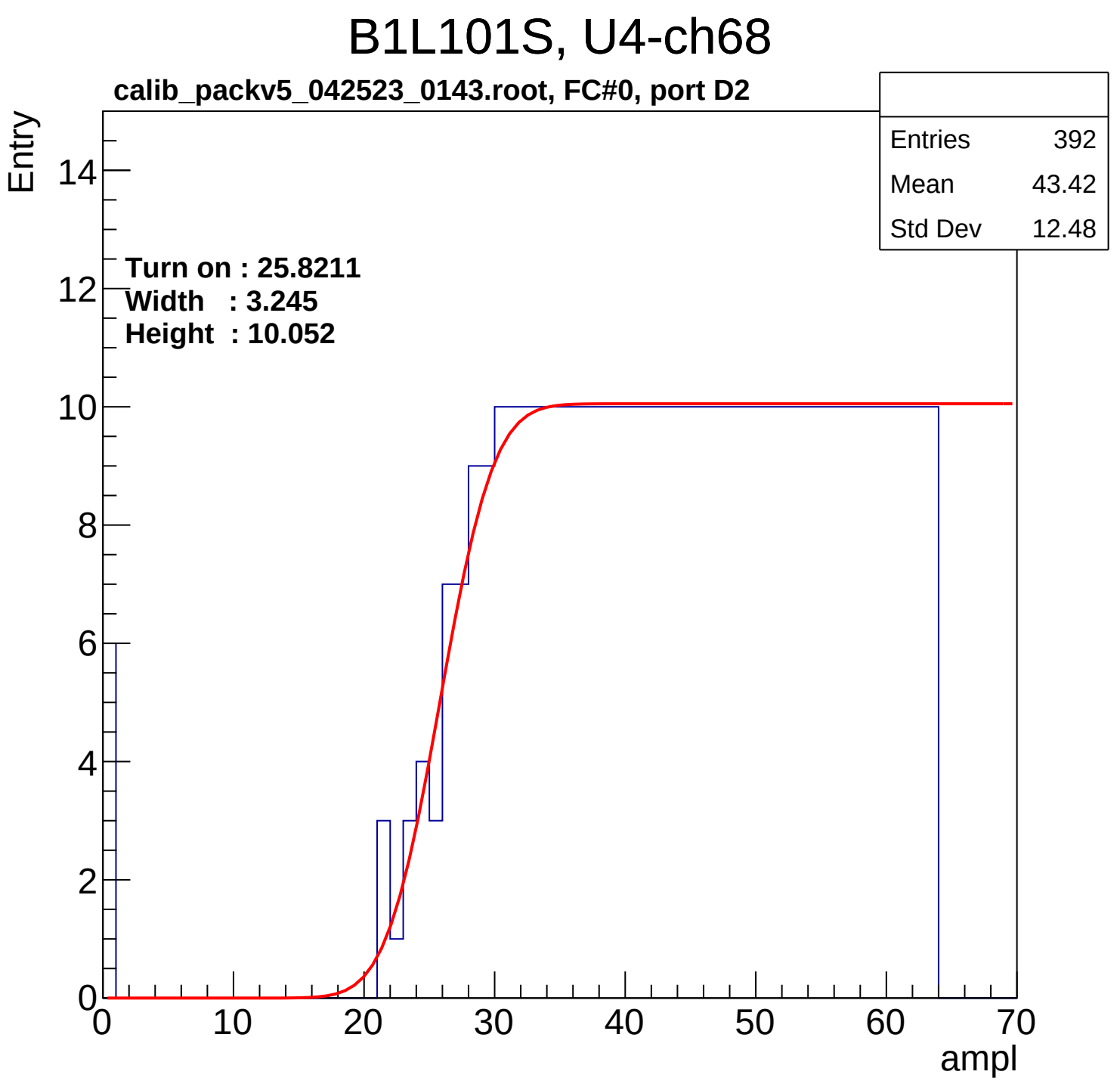

B1L101S, U4-ch63
calib_packv5_042523_0143.root, FC#0, port D2
Entries 380
Mean 44.09
Std Dev 11.93
Turn on : 26.2865
Width : 3.744
Height : 10.018
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

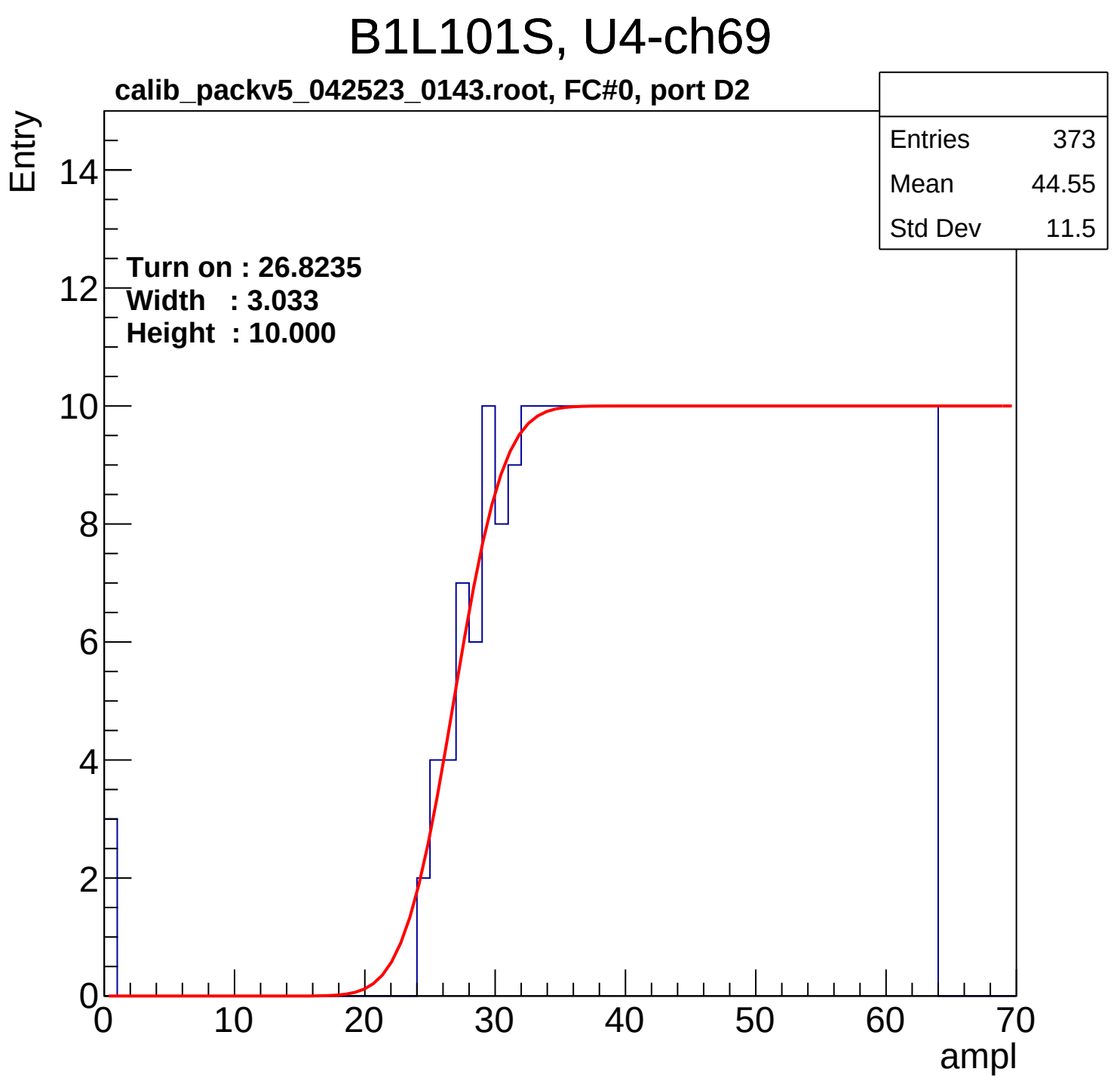

B1L101S, U4-ch64
calib_packv5_042523_0143.root, FC#0, port D2
Entries 399
Mean 43.28
Std Dev 12.14
Turn on : 24.4659
Width : 2.401
Height : 9.941
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

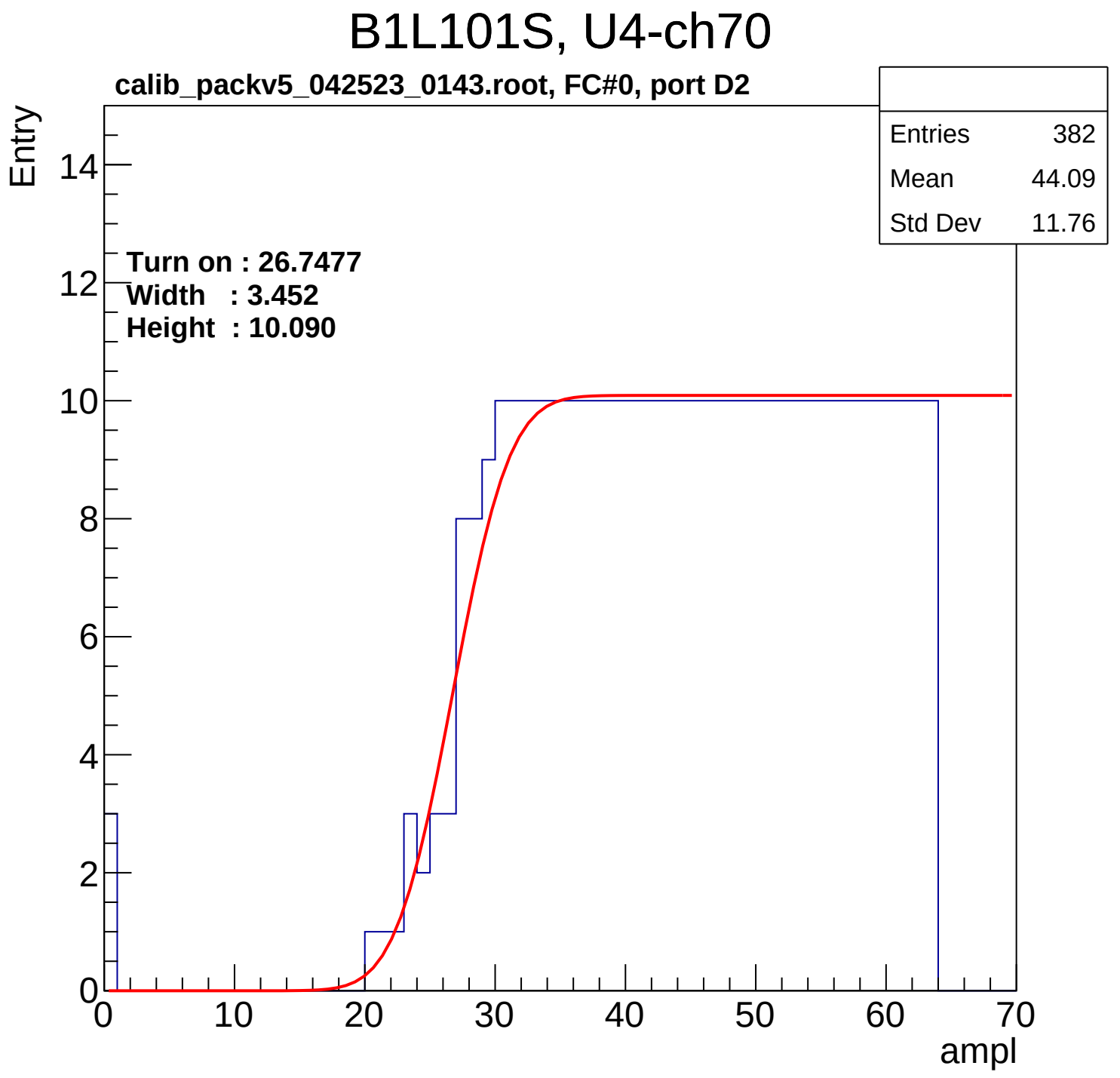

B1L101S, U4-ch65
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.21
Std Dev 11.77
Turn on : 26.7783
Width : 3.725
Height : 10.005
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

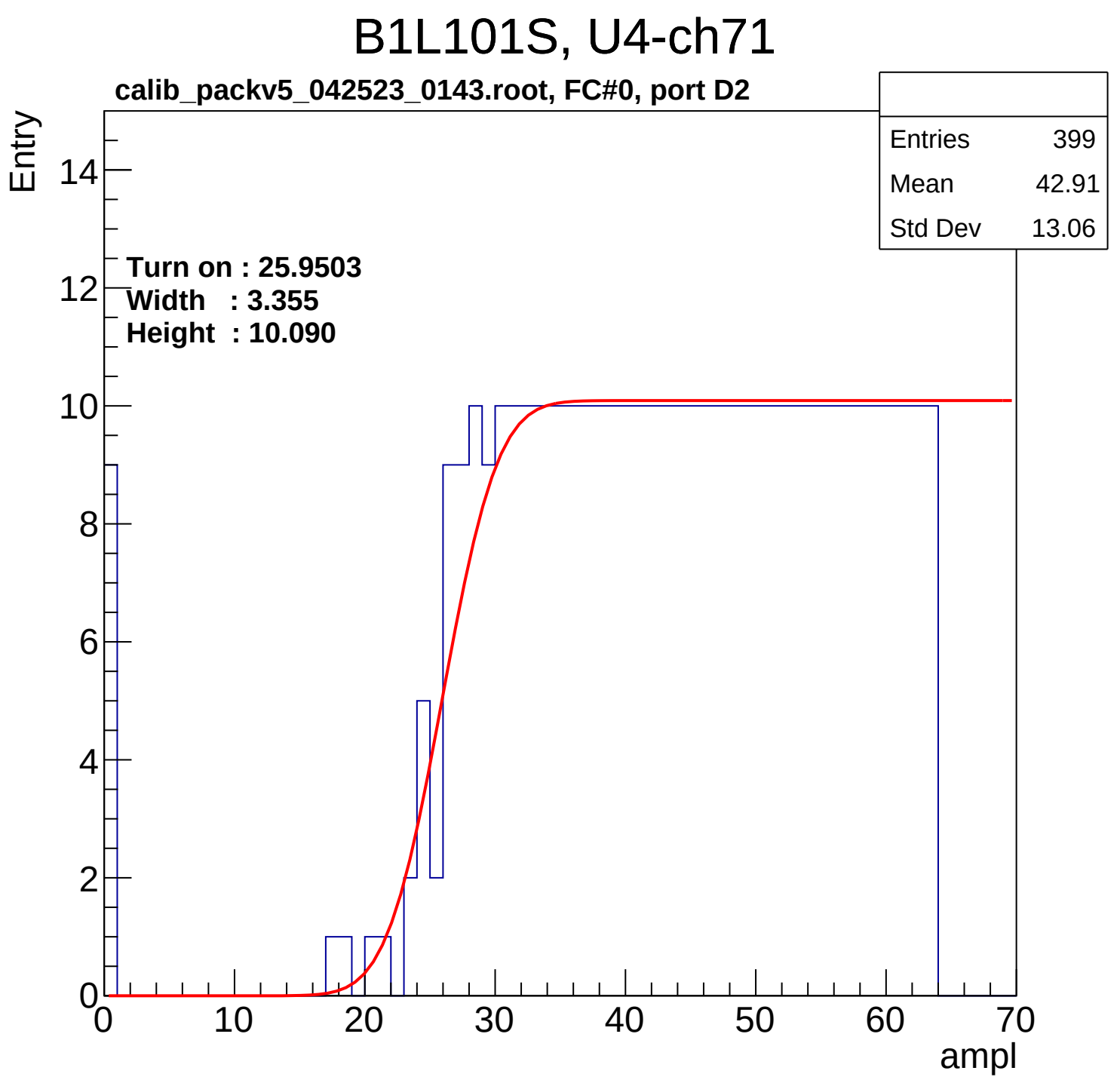

B1L101S, U4-ch66
calib_packv5_042523_0143.root, FC#0, port D2
Entries 401
Mean 43.09
Std Dev 12.4
Turn on : 24.9455
Width : 3.803
Height : 10.074
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

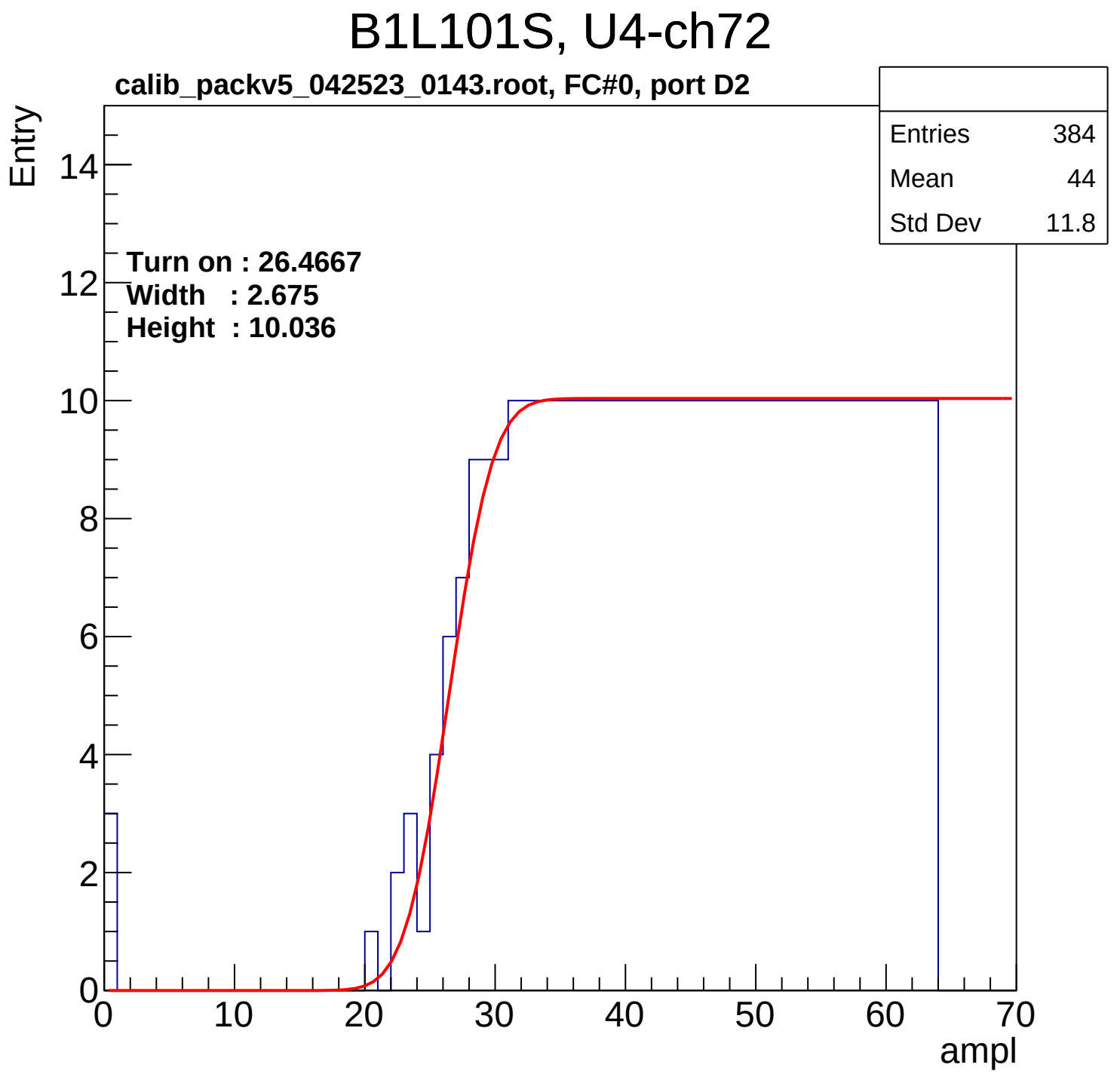

B1L101S, U4-ch67
calib_packv5_042523_0143.root, FC#0, port D2
Entries 396
Mean 43.24
Std Dev 12.54
Turn on : 25.6966
Width : 2.950
Height : 10.068
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

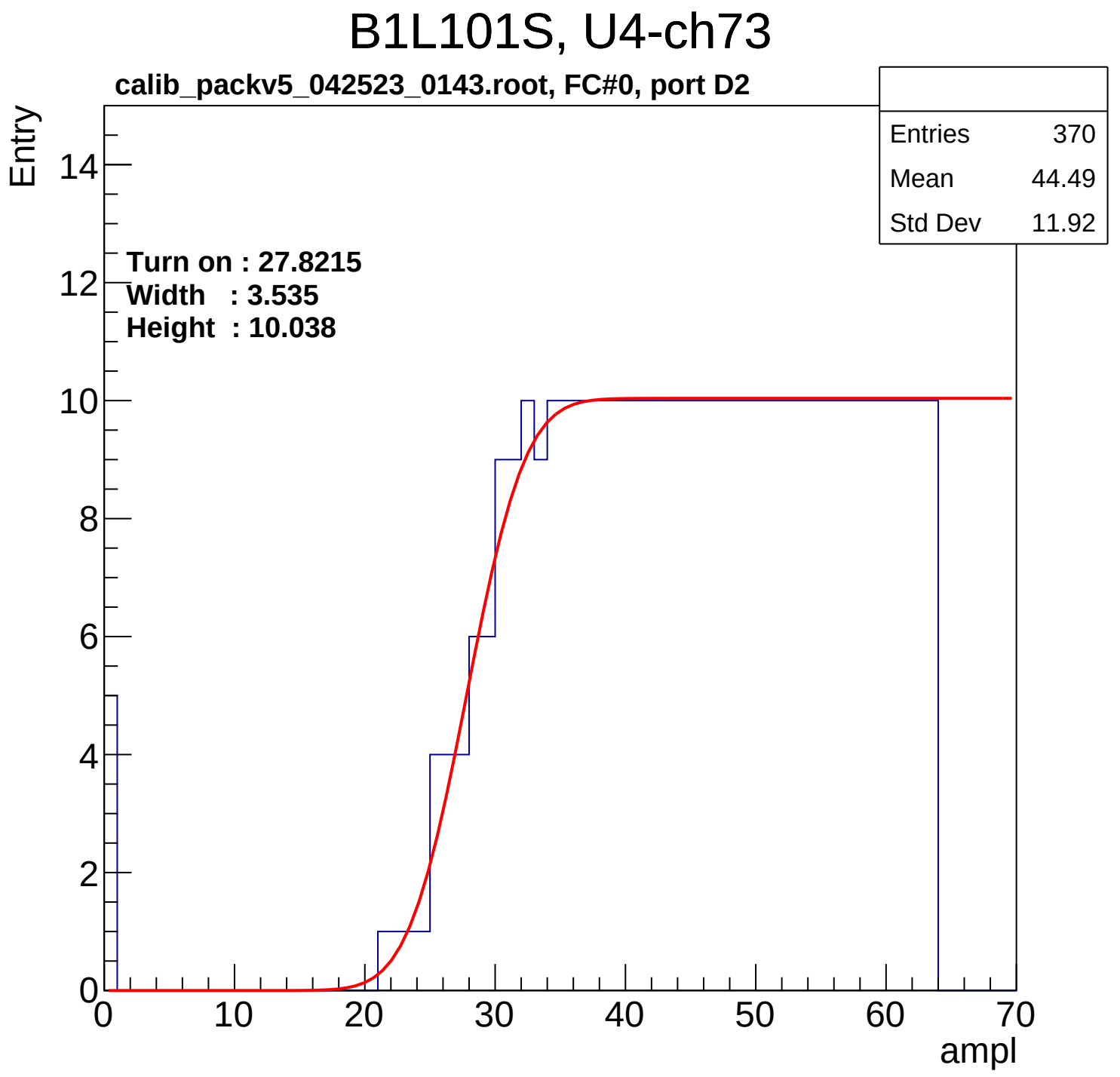

B1L101S, U4-ch68
calib_packv5_042523_0143.root, FC#0, port D2
Entries 392
Mean 43.42
Std Dev 12.48
Turn on : 25.8211
Width : 3.245
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

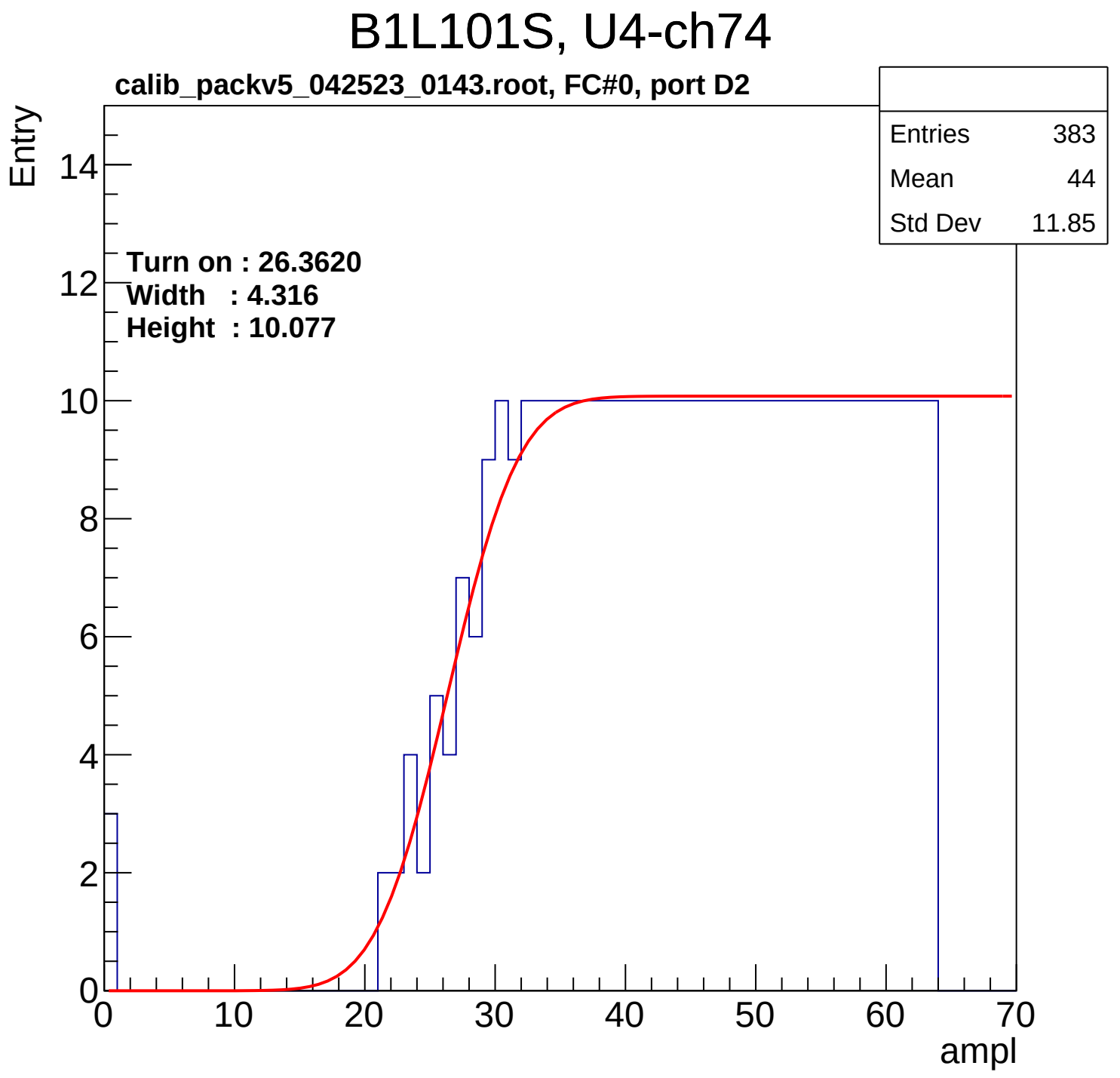

B1L101S, U4-ch69
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.55
Std Dev 11.5
Turn on : 26.8235
Width : 3.033
Height : 10.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

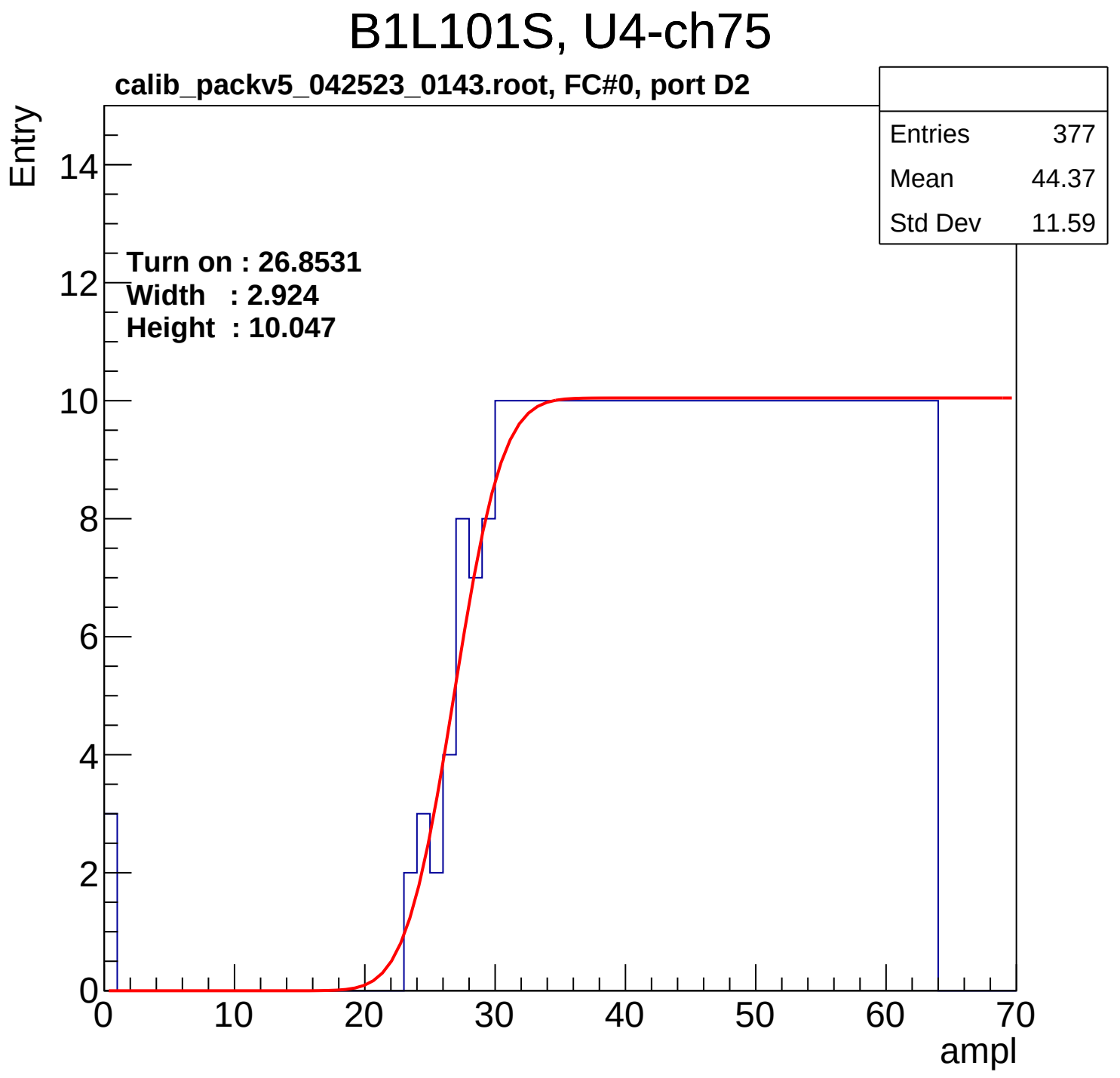

B1L101S, U4-ch70
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 44.09
Std Dev 11.76
Turn on : 26.7477
Width : 3.452
Height : 10.090
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

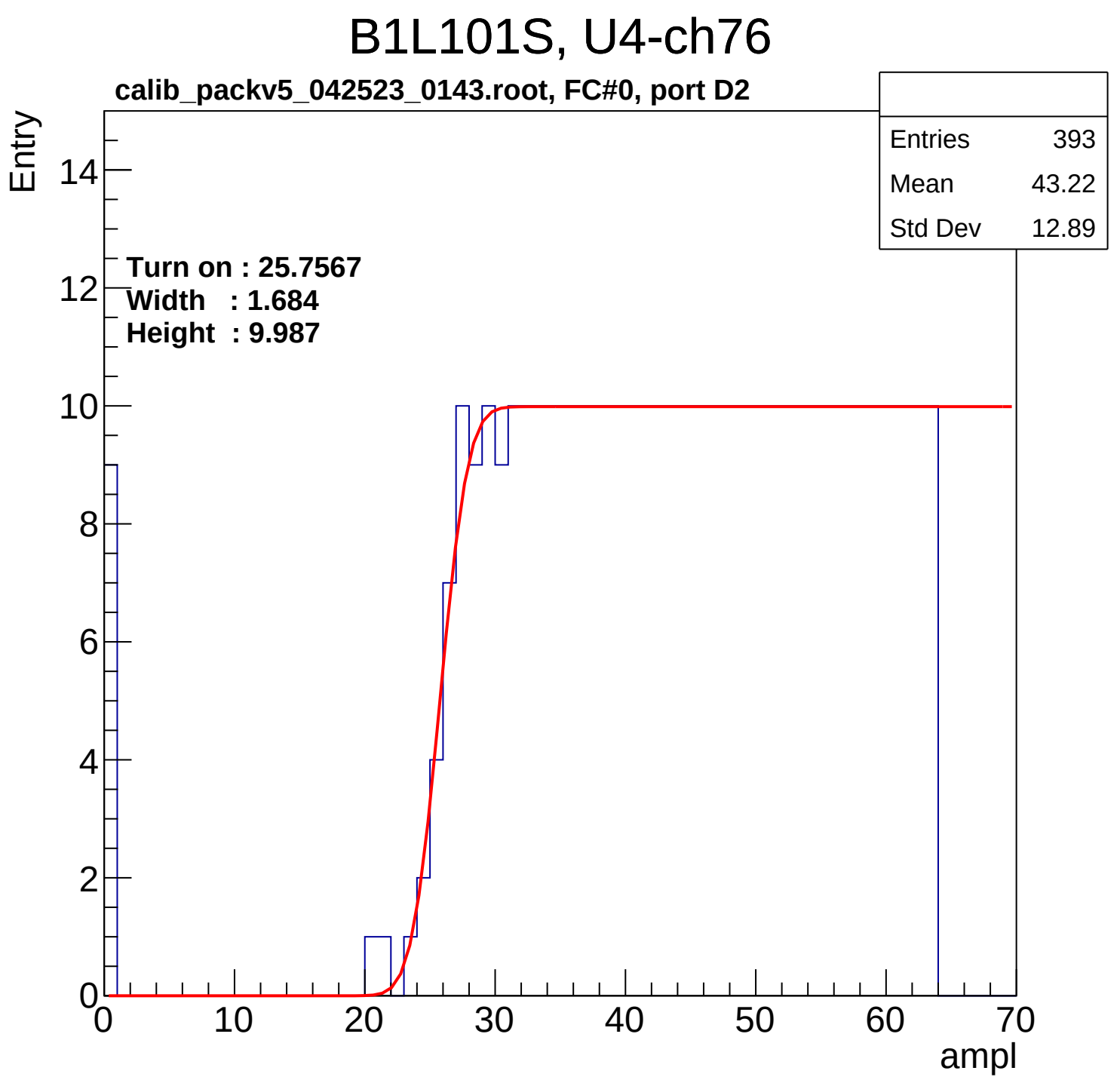

B1L101S, U4-ch71
calib_packv5_042523_0143.root, FC#0, port D2
Entries 399
Mean 42.91
Std Dev 13.06
Turn on : 25.9503
Width : 3.355
Height : 10.090
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

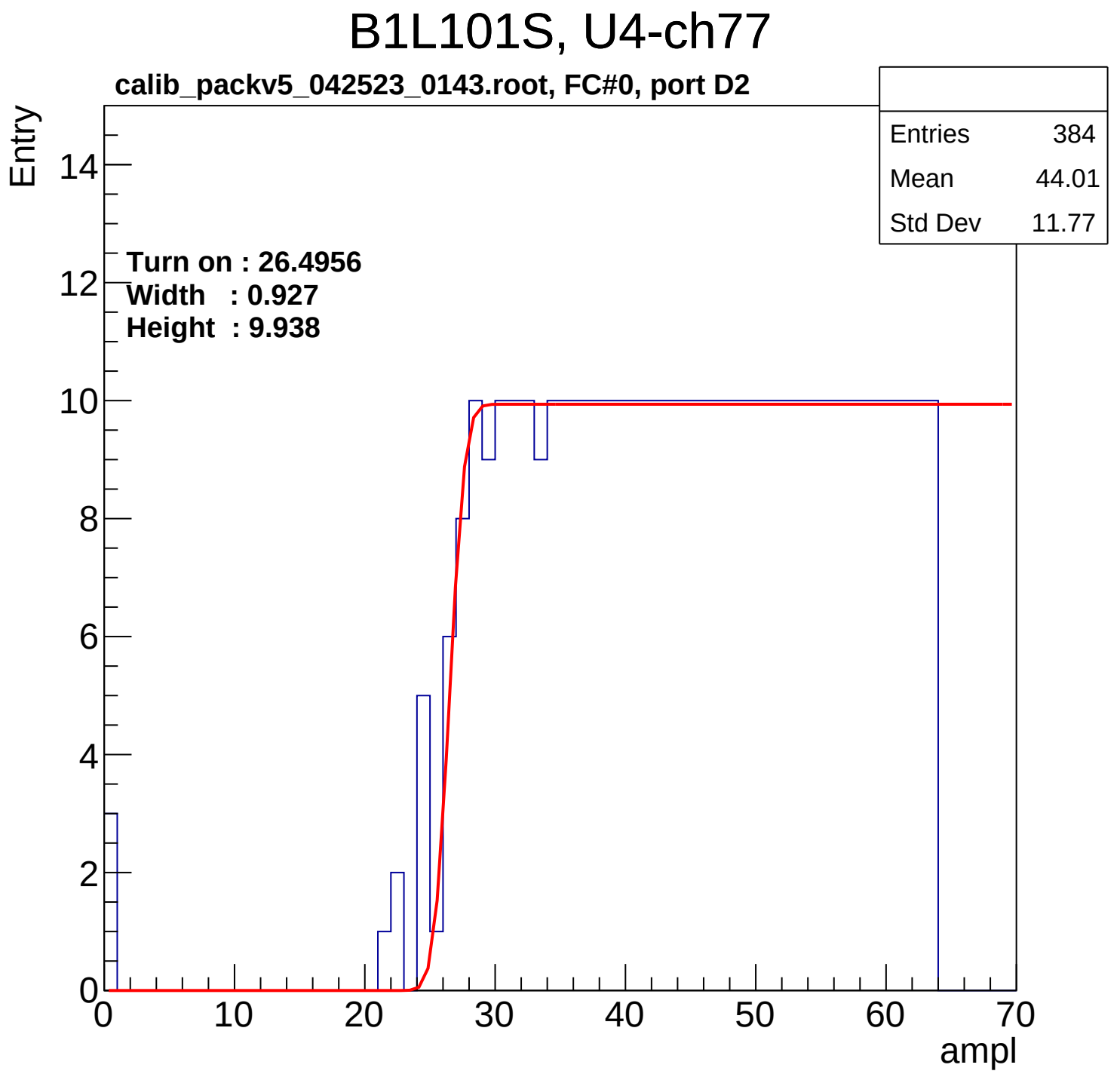

B1L101S, U4-ch72
calib_packv5_042523_0143.root, FC#0, port D2
Entries 384
Mean 44
Std Dev 11.8
Turn on : 26.4667
Width : 2.675
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

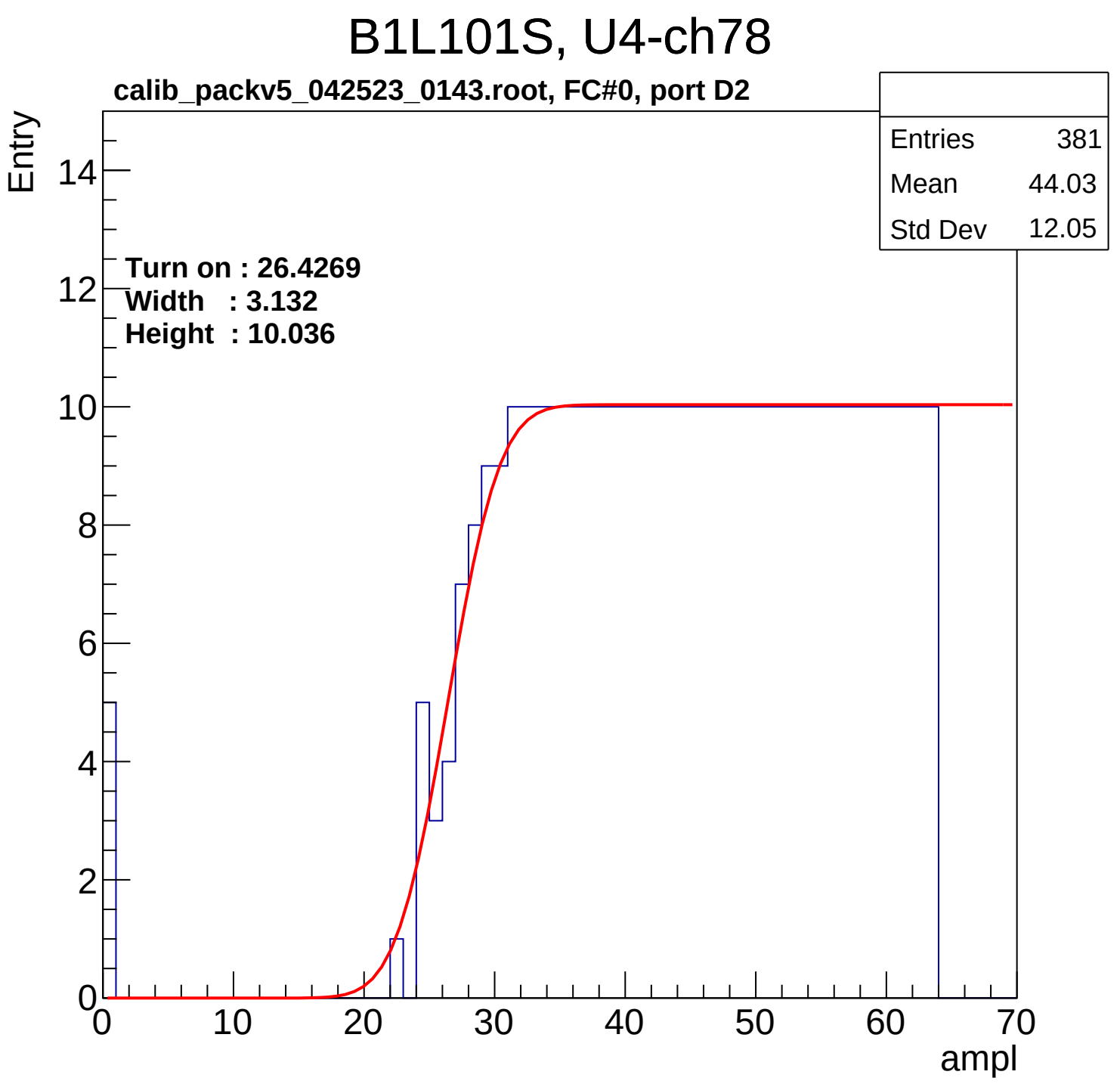

B1L101S, U4-ch73
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.49
Std Dev 11.92
Turn on : 27.8215
Width : 3.535
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

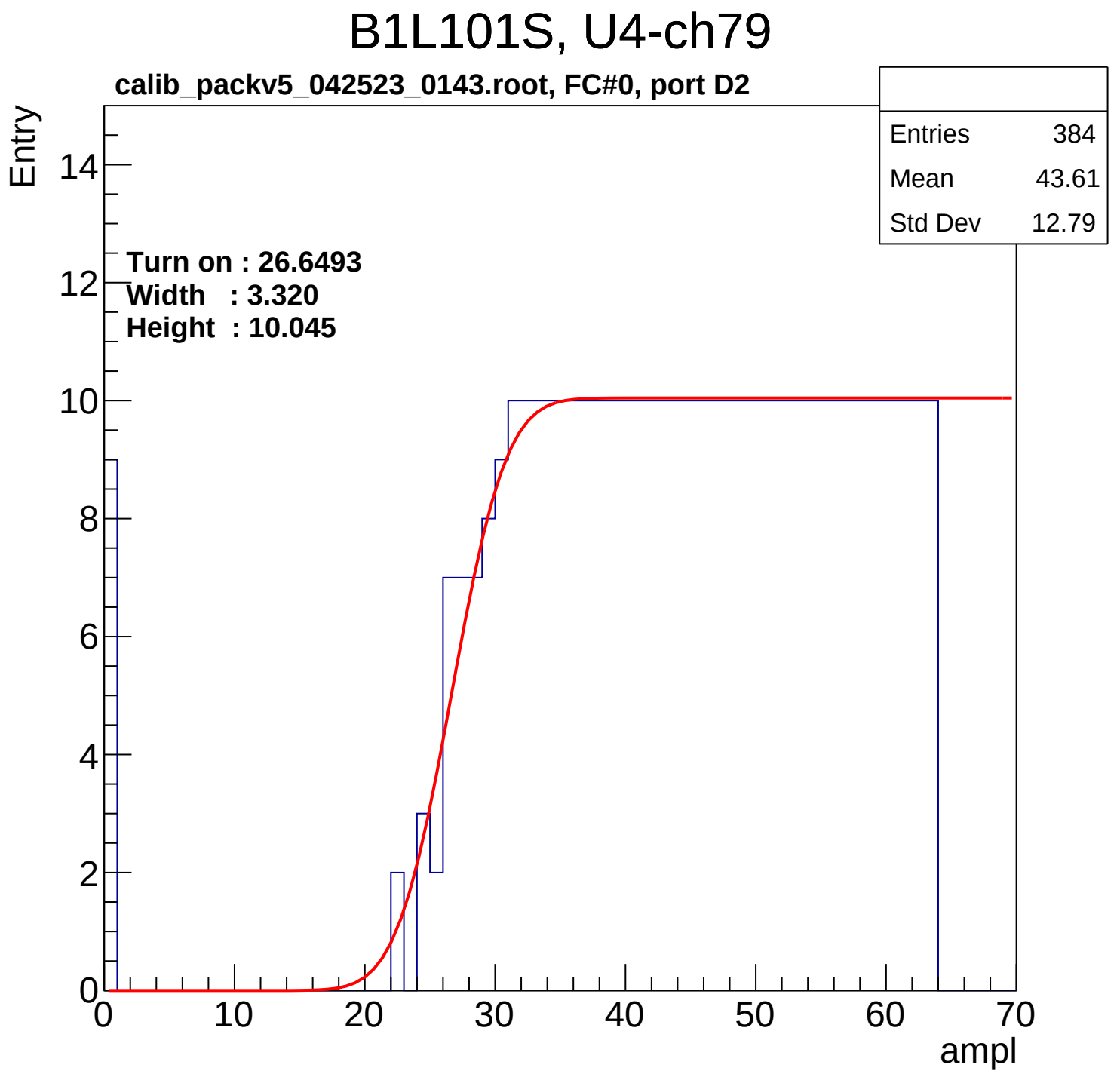

B1L101S, U4-ch74
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 44
Std Dev 11.85
Turn on : 26.3620
Width : 4.316
Height : 10.077
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

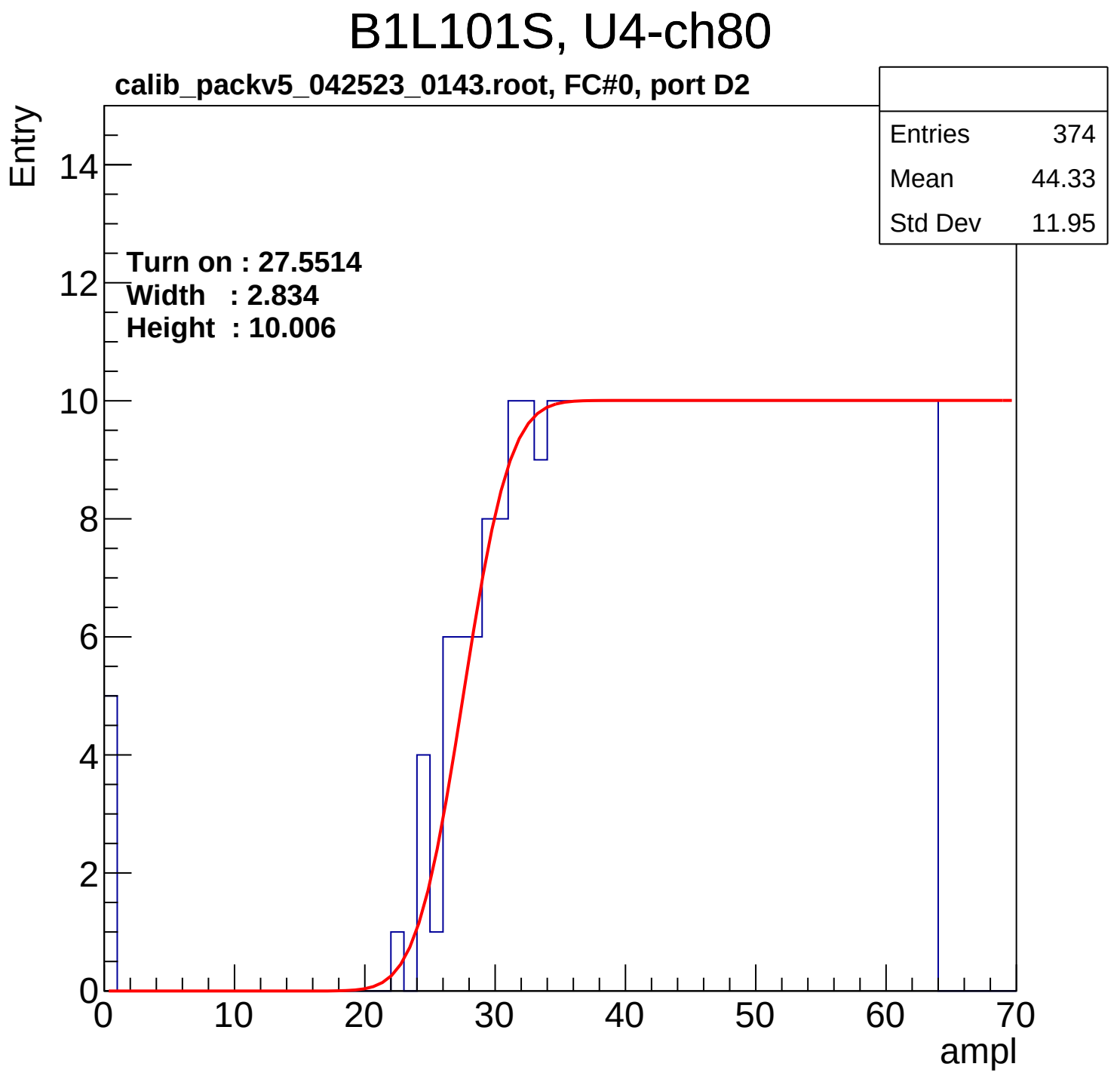

B1L101S, U4-ch75
calib_packv5_042523_0143.root, FC#0, port D2
Entries 377
Mean 44.37
Std Dev 11.59
Turn on : 26.8531
Width : 2.924
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

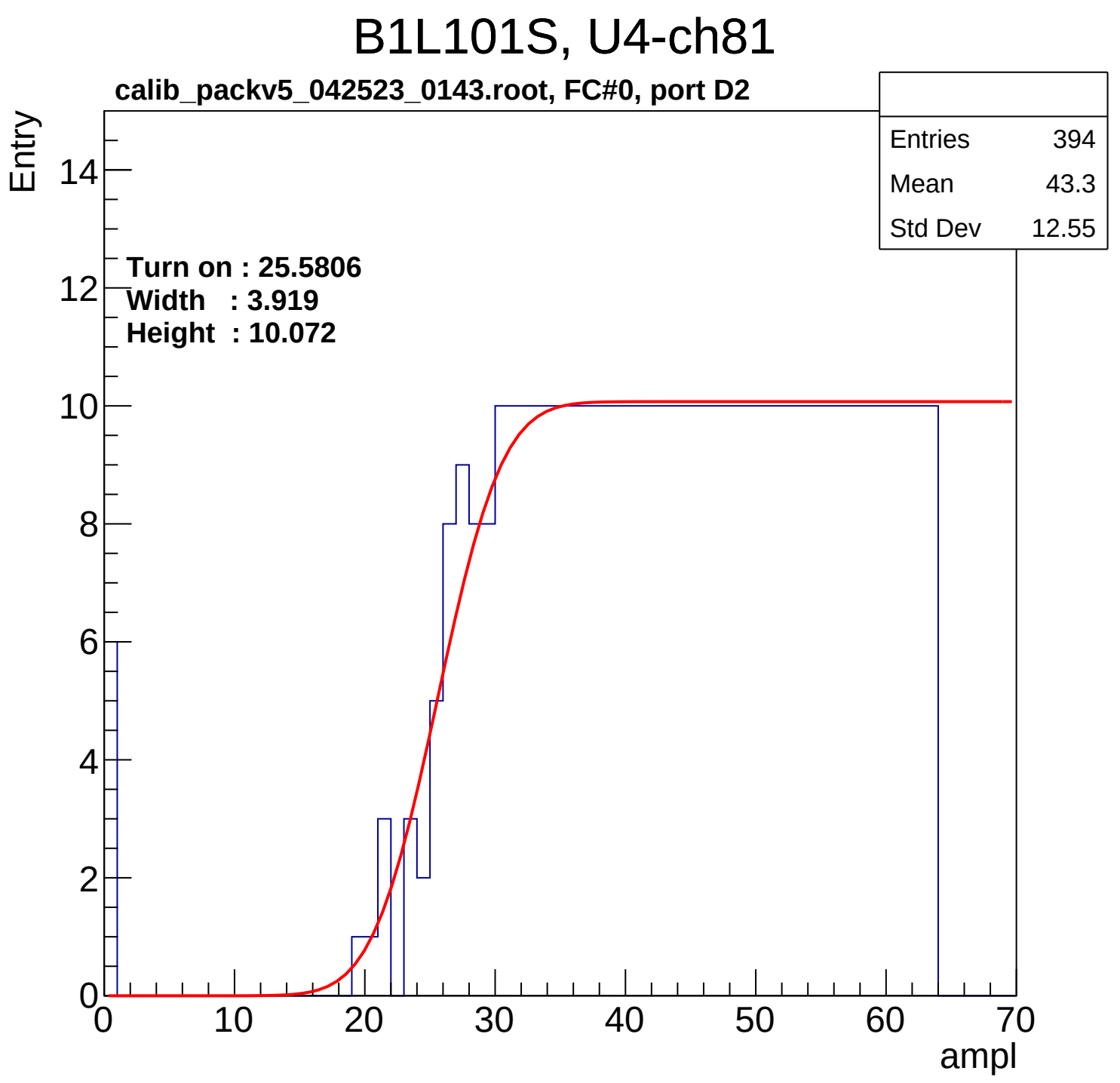

B1L101S, U4-ch76
calib_packv5_042523_0143.root, FC#0, port D2
Entries 393
Mean 43.22
Std Dev 12.89
Turn on : 25.7567
Width : 1.684
Height : 9.987
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

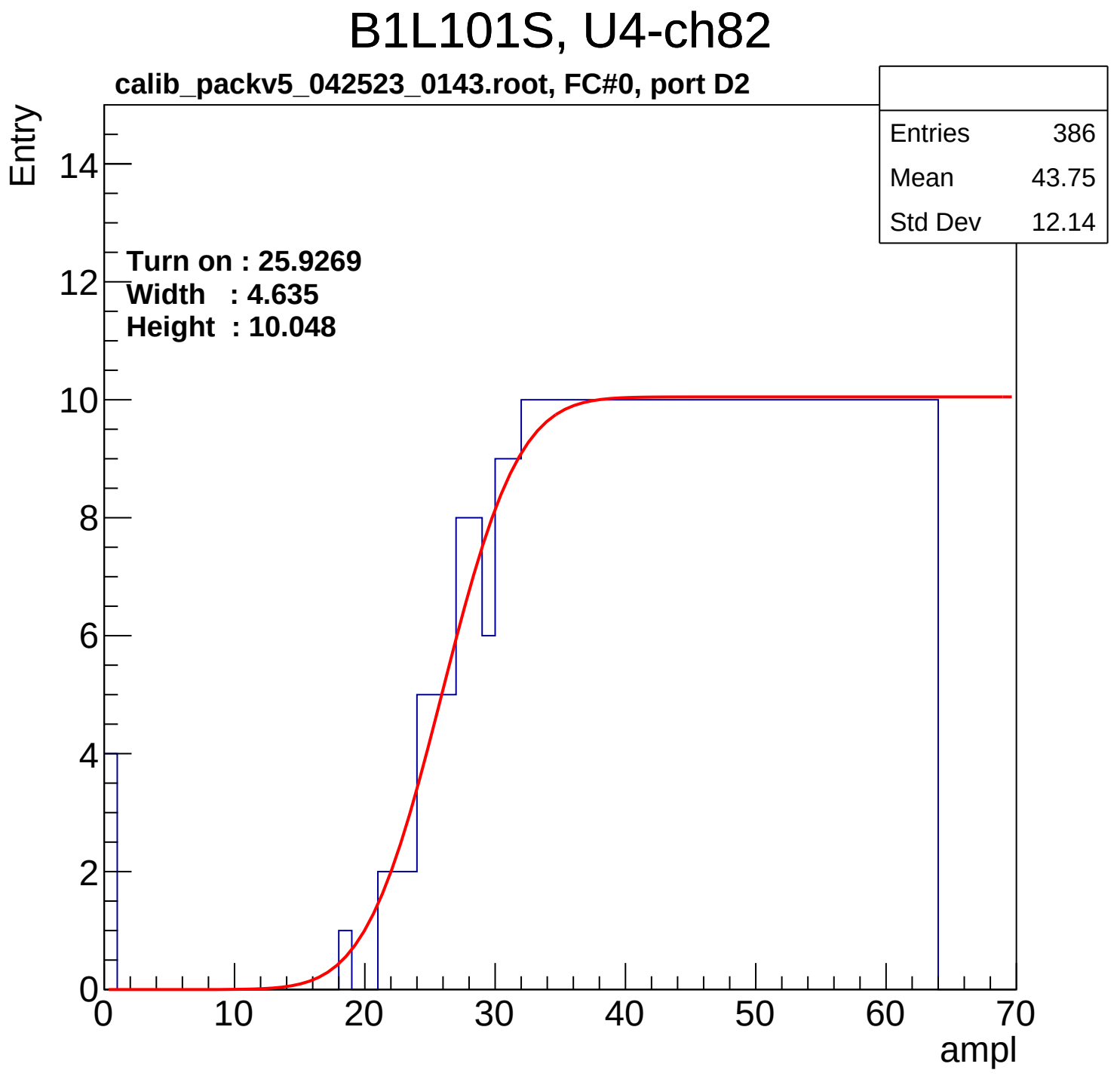

B1L101S, U4-ch77
calib_packv5_042523_0143.root, FC#0, port D2
Entries 384
Mean 44.01
Std Dev 11.77
Turn on : 26.4956
Width : 0.927
Height : 9.938
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

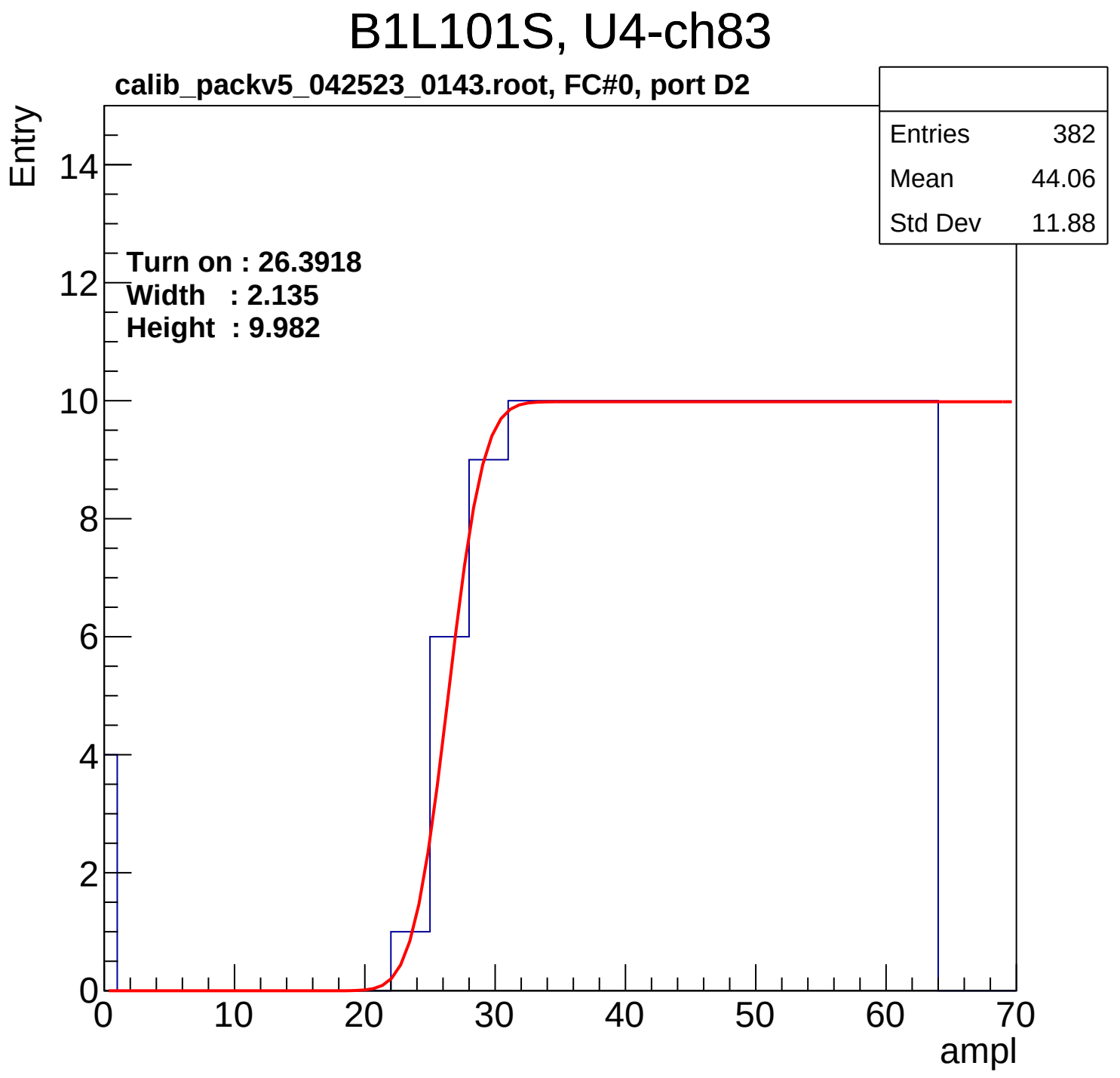

B1L101S, U4-ch78
calib_packv5_042523_0143.root, FC#0, port D2
Entries 381
Mean 44.03
Std Dev 12.05
Turn on : 26.4269
Width : 3.132
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

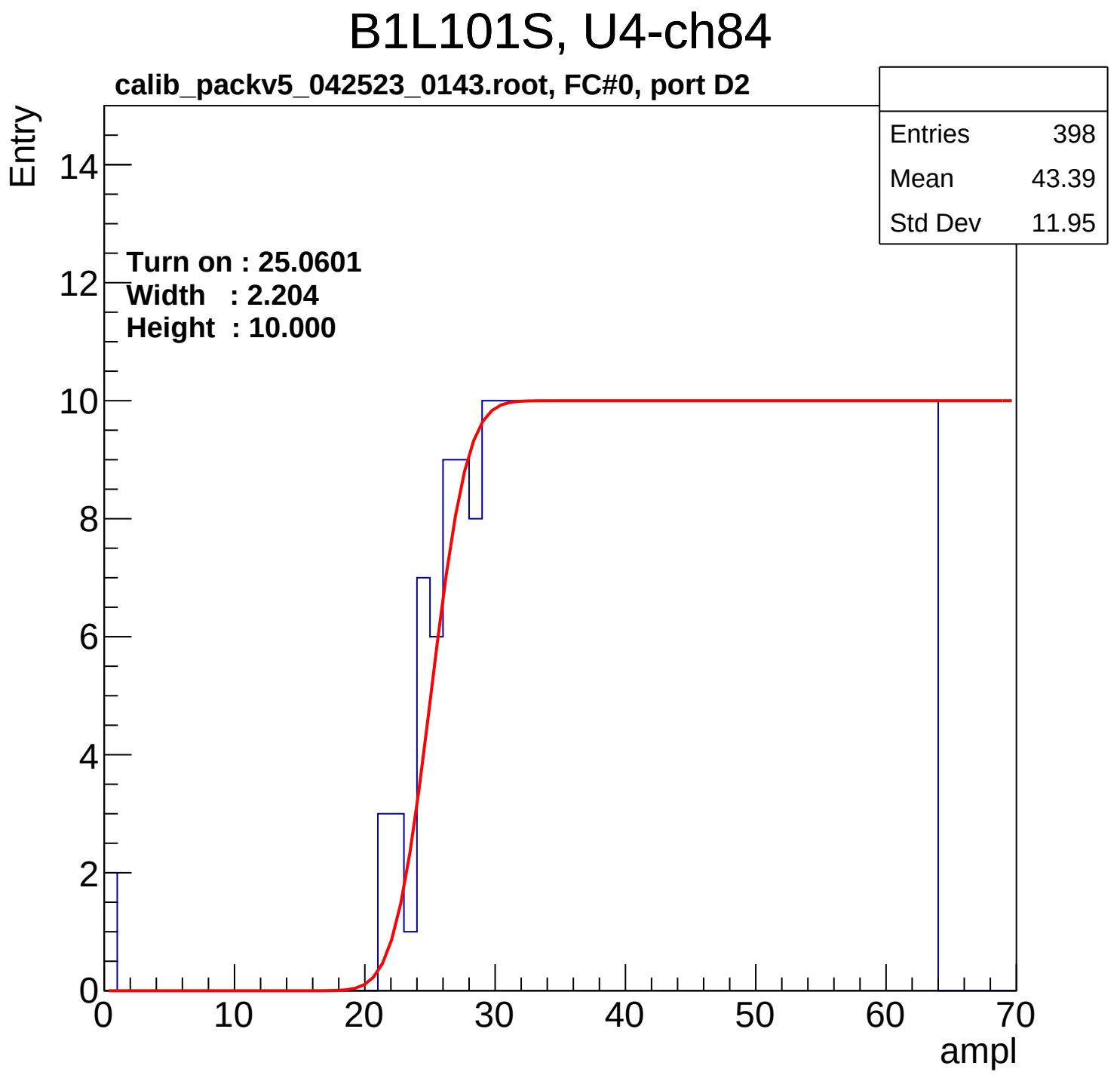

B1L101S, U4-ch79
calib_packv5_042523_0143.root, FC#0, port D2
Entries 384
Mean 43.61
Std Dev 12.79
Turn on : 26.6493
Width : 3.320
Height : 10.045
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

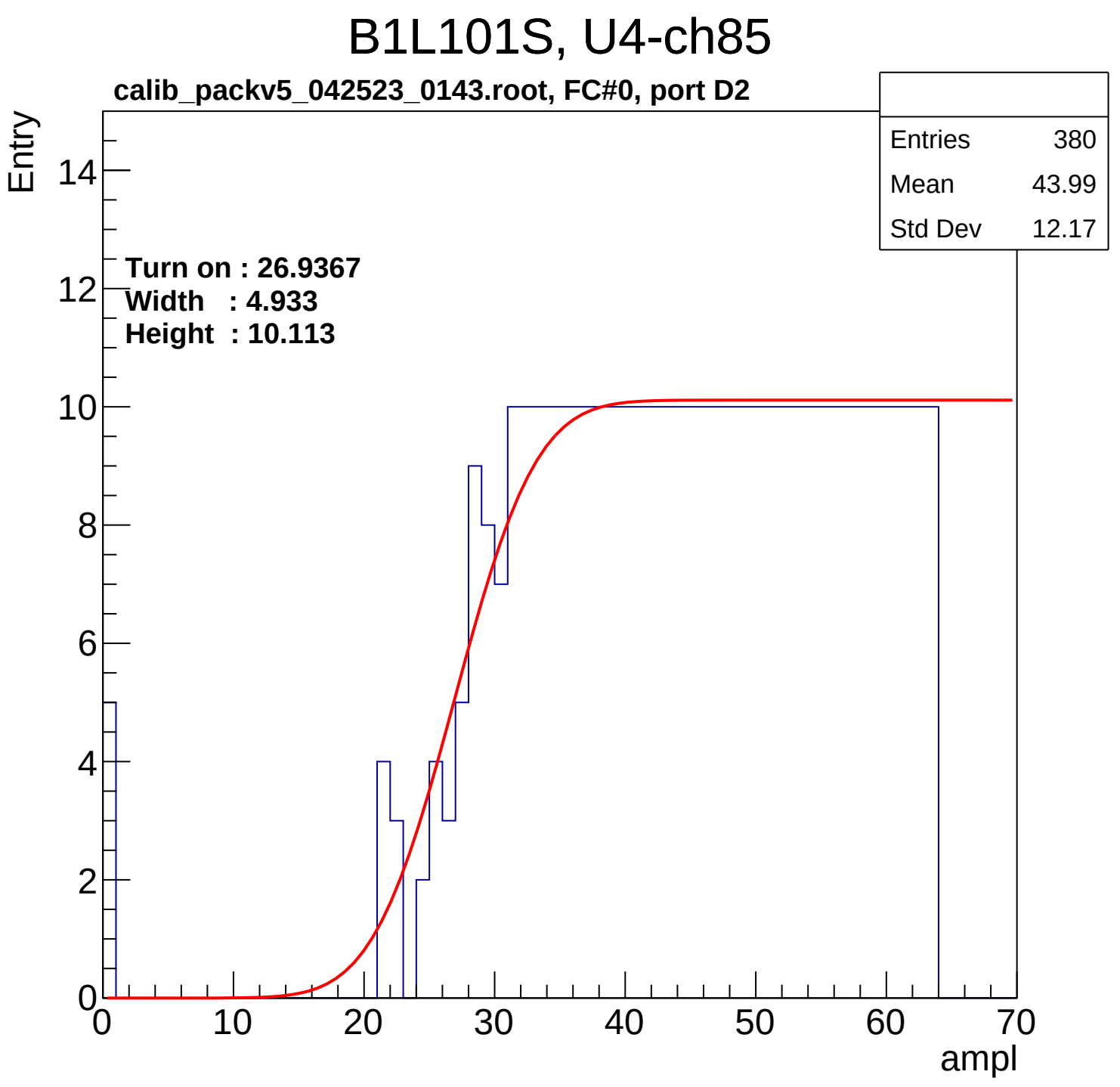

B1L101S, U4-ch80
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.33
Std Dev 11.95
Turn on : 27.5514
Width : 2.834
Height : 10.006
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

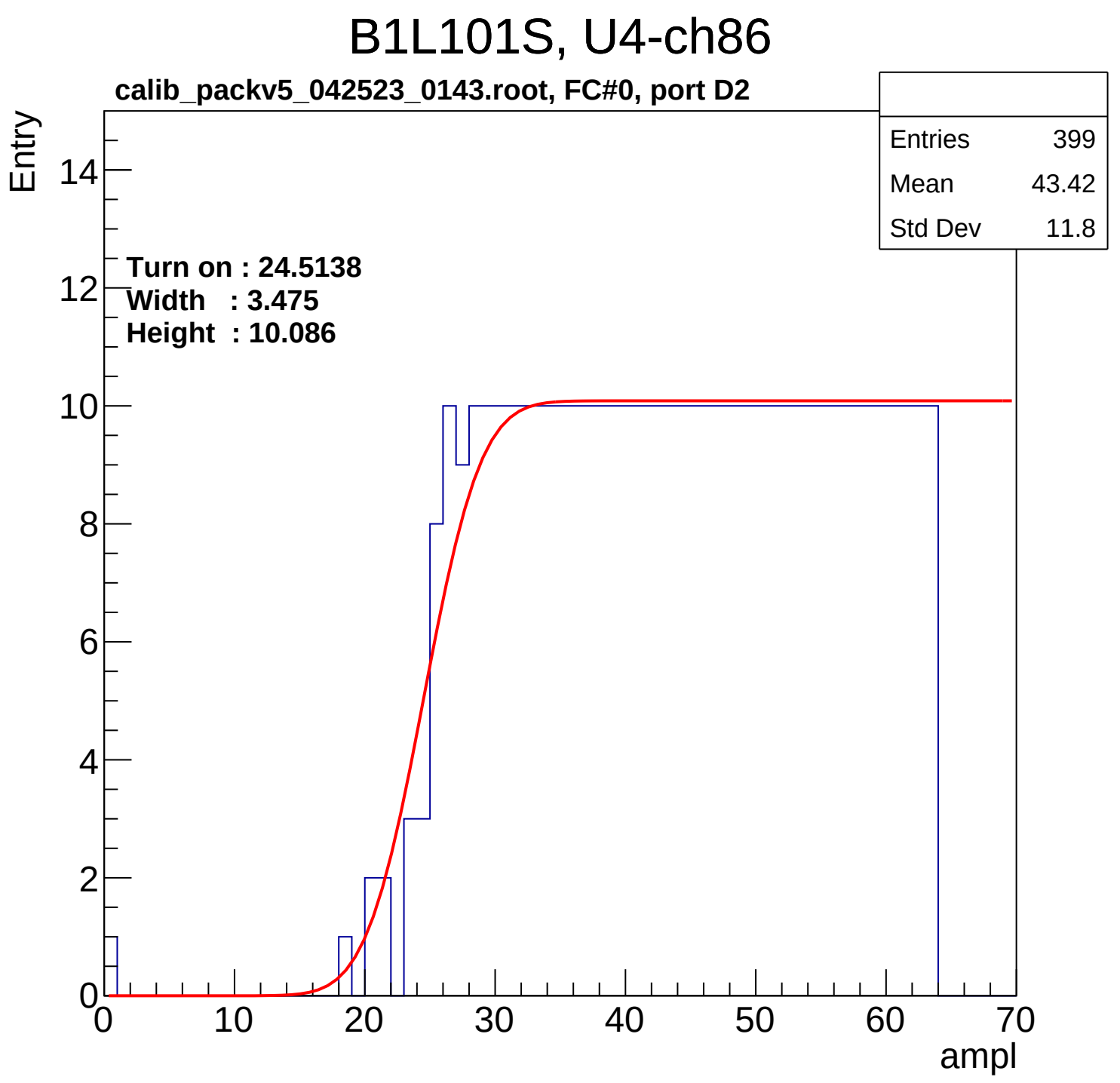

B1L101S, U4-ch81
calib_packv5_042523_0143.root, FC#0, port D2
Entries 394
Mean 43.3
Std Dev 12.55
Turn on : 25.5806
Width : 3.919
Height : 10.072
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

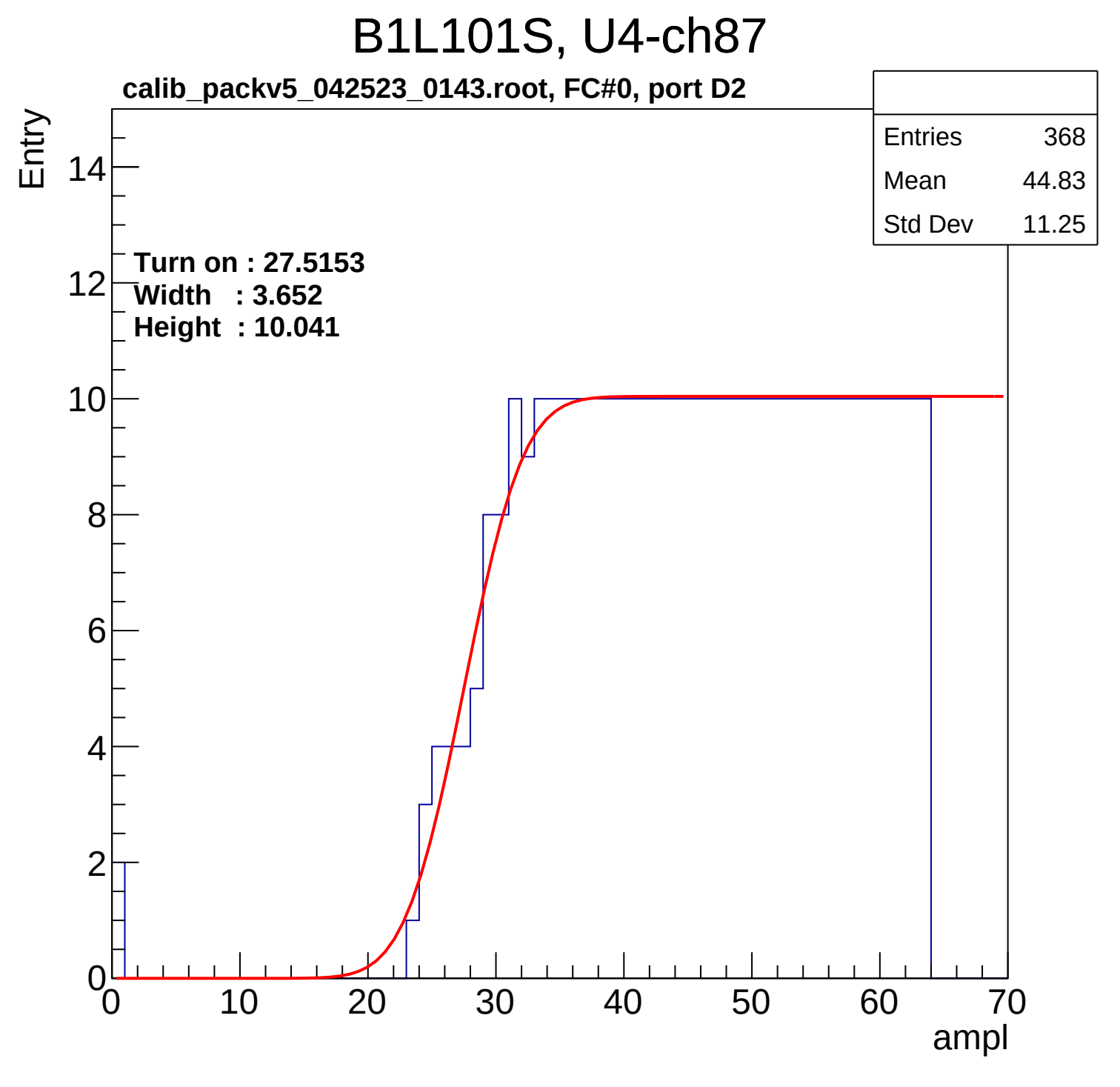

B1L101S, U4-ch82
calib_packv5_042523_0143.root, FC#0, port D2
Entries 386
Mean 43.75
Std Dev 12.14
Turn on : 25.9269
Width : 4.635
Height : 10.048
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

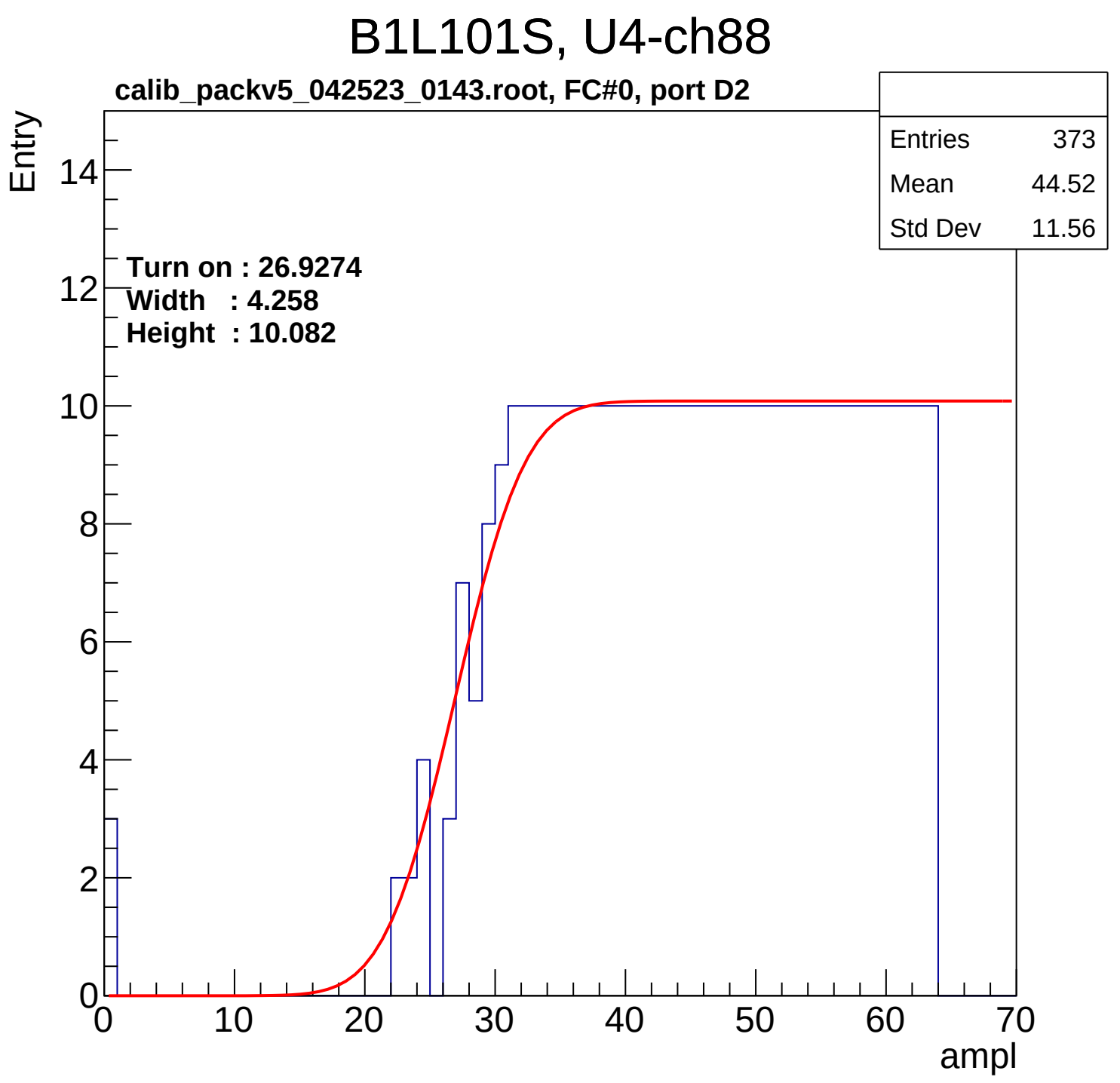

B1L101S, U4-ch83
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 44.06
Std Dev 11.88
Turn on : 26.3918
Width : 2.135
Height : 9.982
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

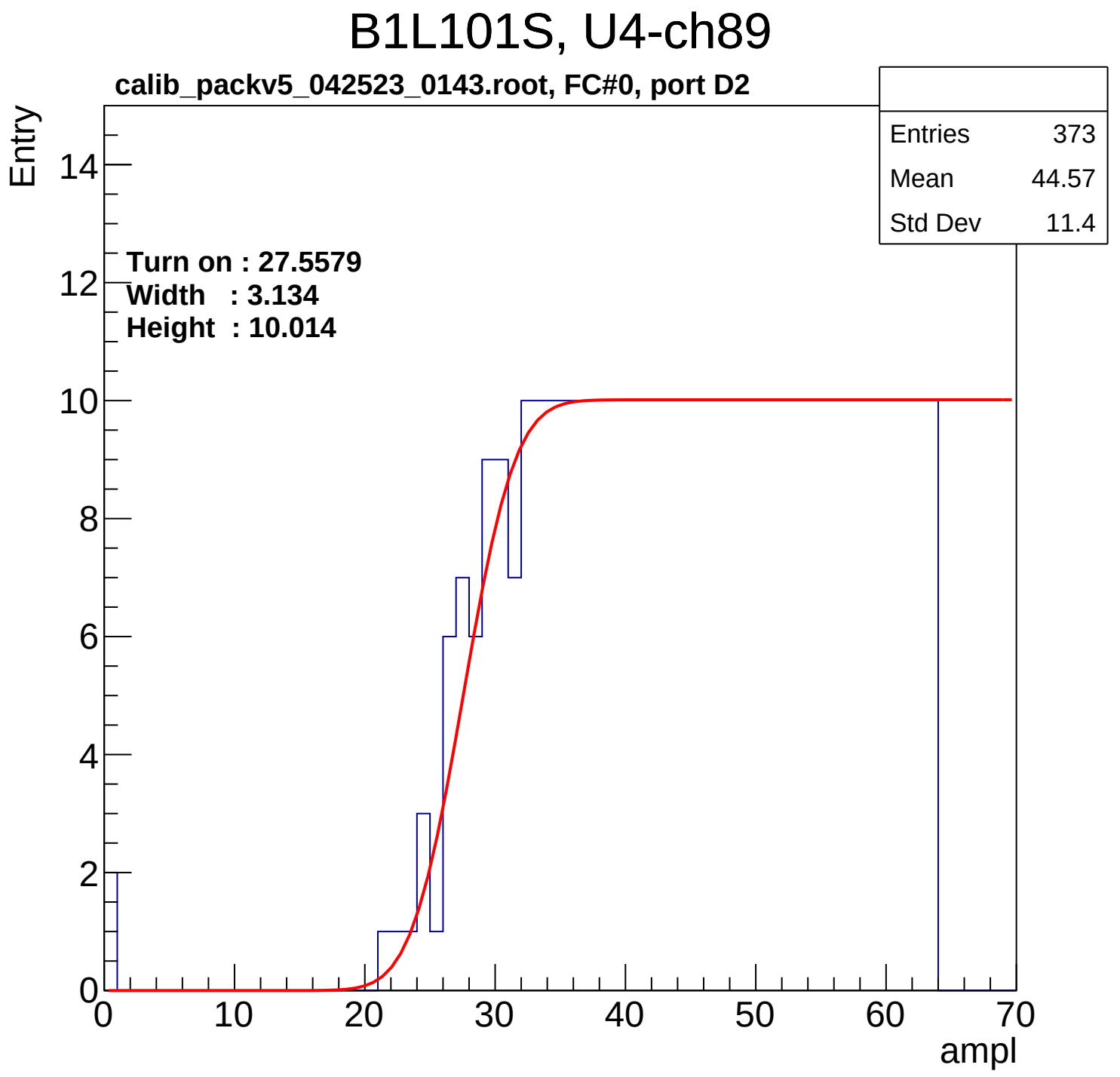

B1L101S, U4-ch84
calib_packv5_042523_0143.root, FC#0, port D2
Entries 398
Mean 43.39
Std Dev 11.95
Turn on : 25.0601
Width : 2.204
Height : 10.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

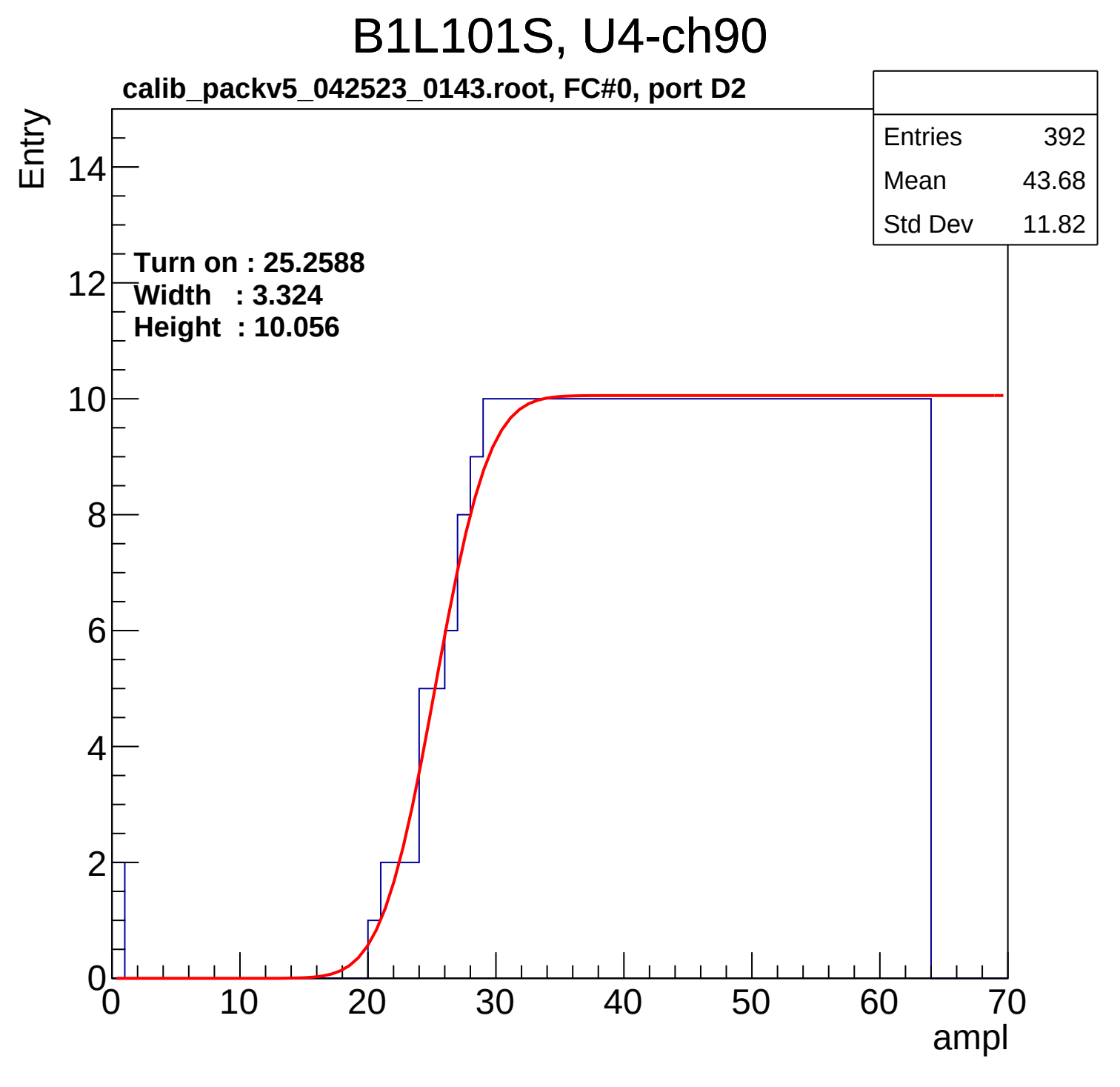

B1L101S, U4-ch85
calib_packv5_042523_0143.root, FC#0, port D2
Entries 380
Mean 43.99
Std Dev 12.17
Turn on : 26.9367
Width : 4.933
Height : 10.113
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

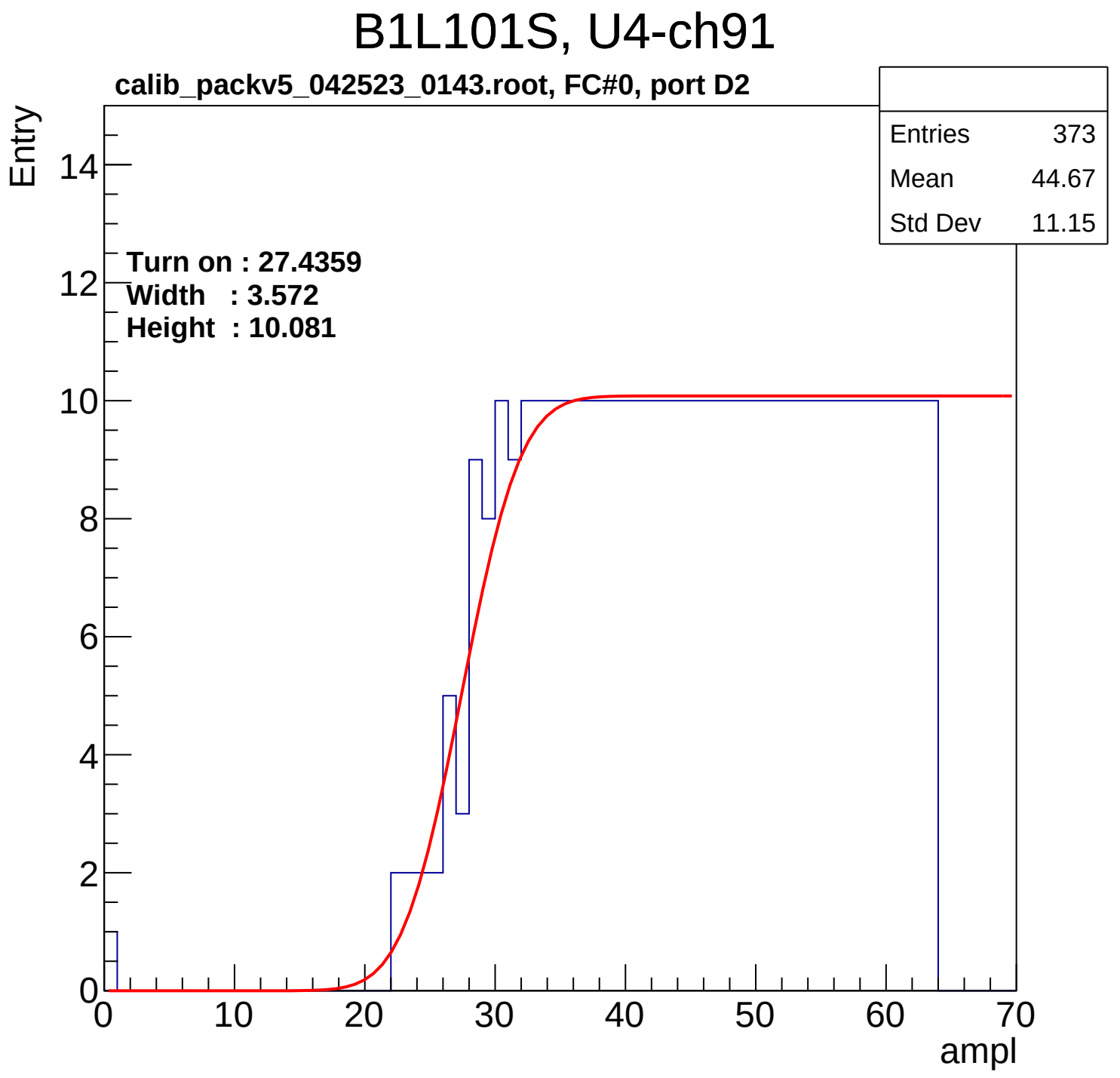

B1L101S, U4-ch86
calib_packv5_042523_0143.root, FC#0, port D2
Entries 399
Mean 43.42
Std Dev 11.8
Turn on : 24.5138
Width : 3.475
Height : 10.086
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

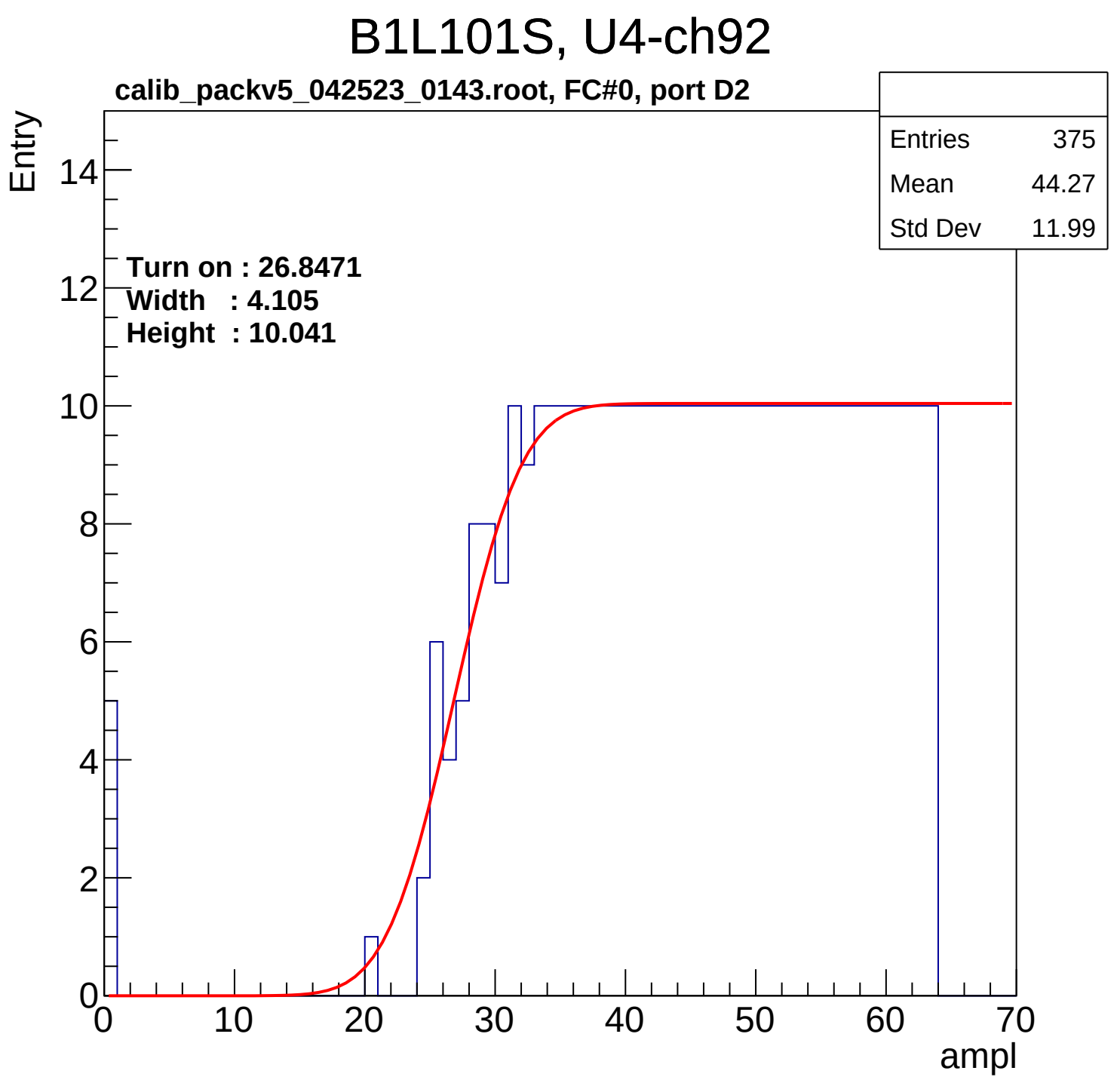

B1L101S, U4-ch87
calib_packv5_042523_0143.root, FC#0, port D2
Entries 368
Mean 44.83
Std Dev 11.25
Turn on : 27.5153
Width : 3.652
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

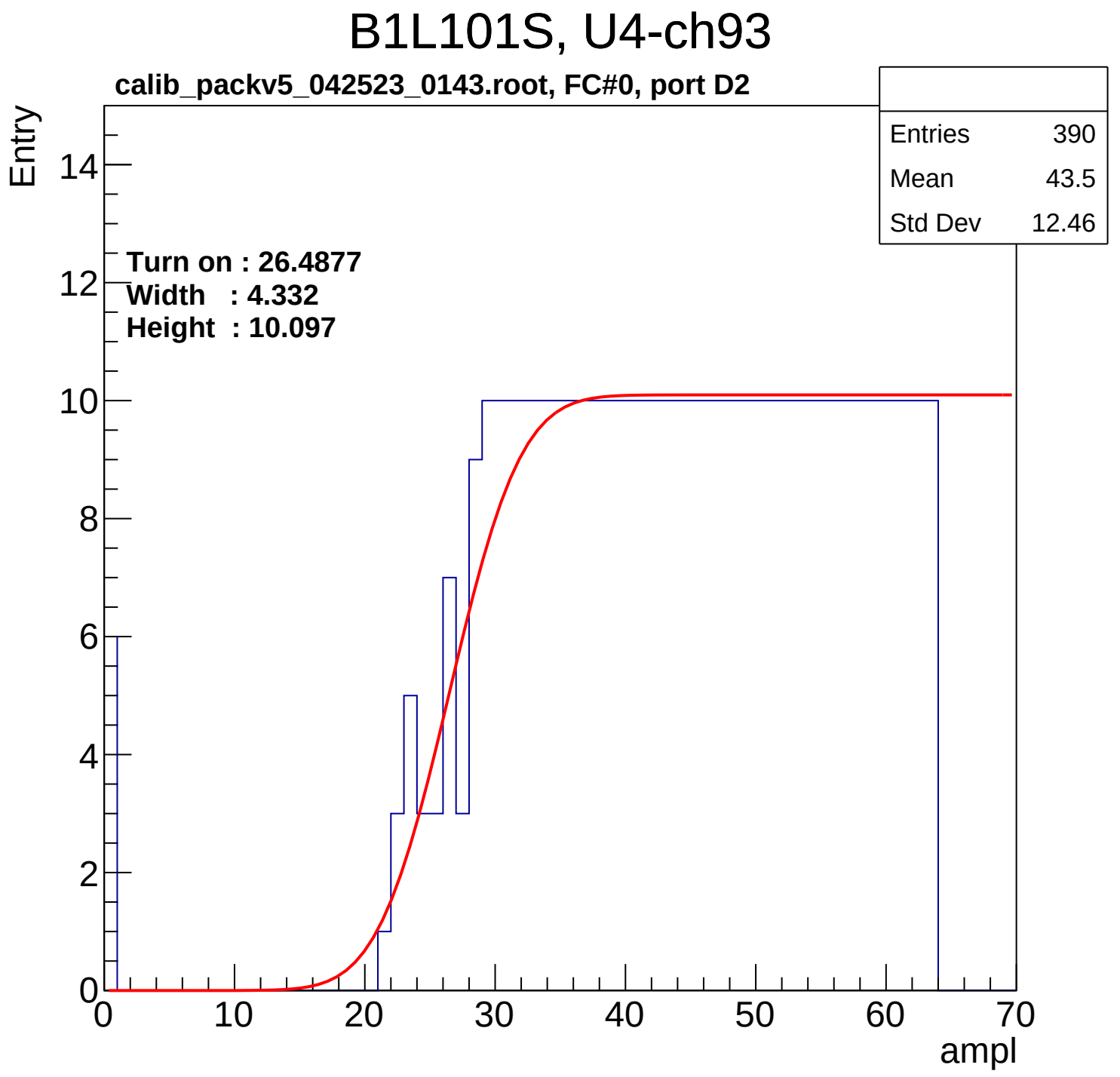

B1L101S, U4-ch88
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.52
Std Dev 11.56
Turn on : 26.9274
Width : 4.258
Height : 10.082
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

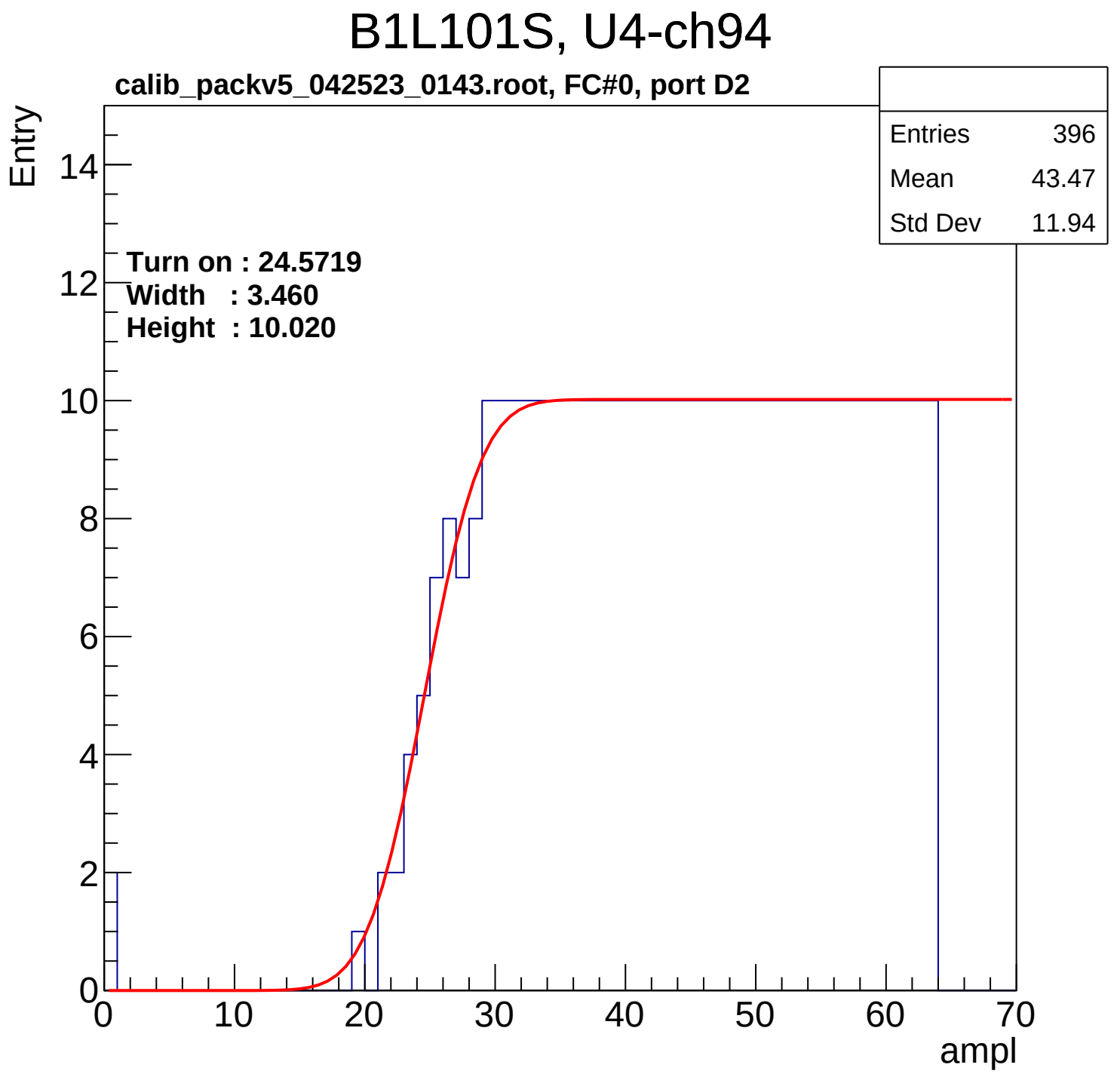

B1L101S, U4-ch89
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.57
Std Dev 11.4
Turn on : 27.5579
Width : 3.134
Height : 10.014
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

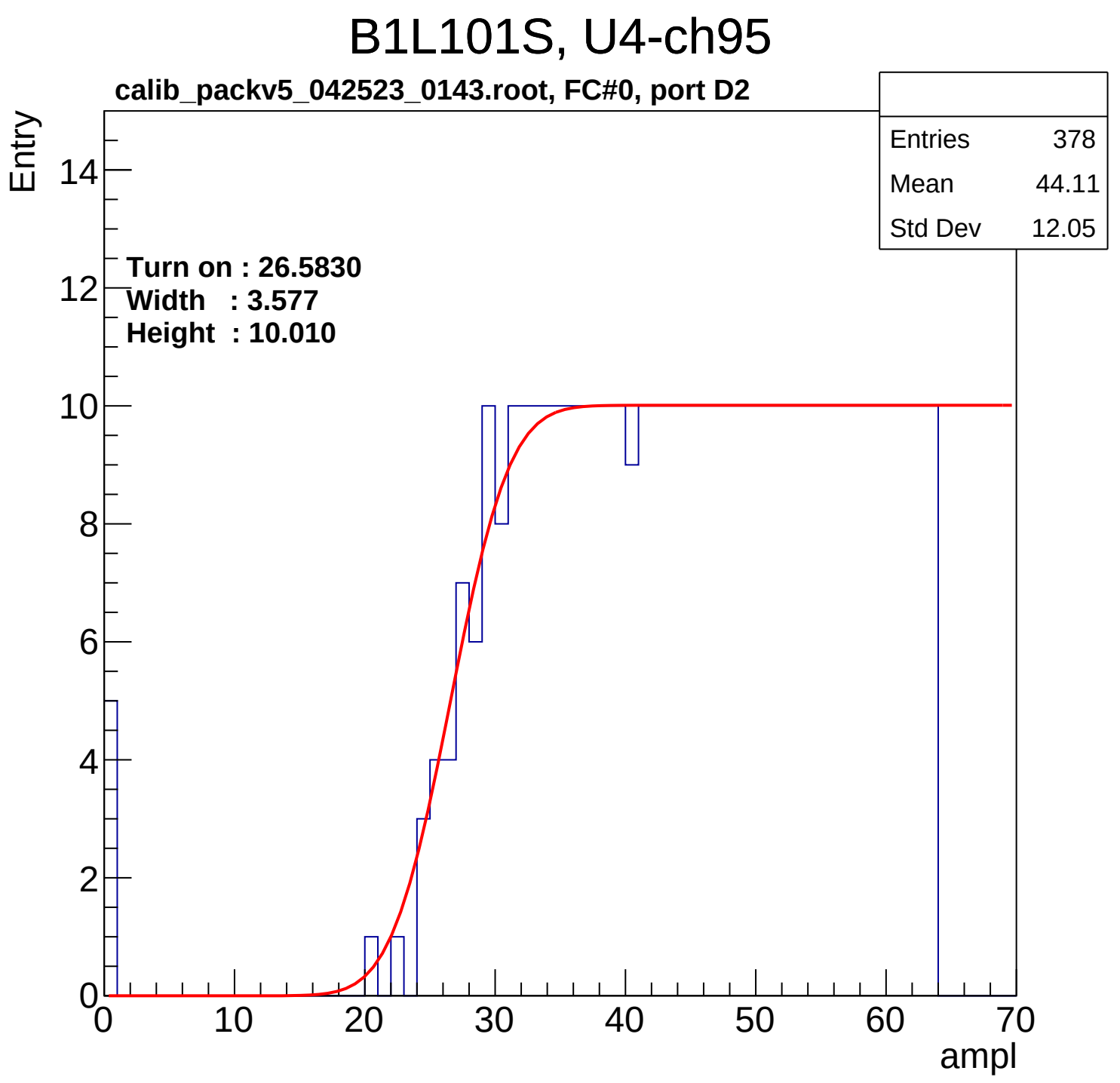

B1L101S, U4-ch90
calib_packv5_042523_0143.root, FC#0, port D2
Entries 392
Mean 43.68
Std Dev 11.82
Turn on : 25.2588
Width : 3.324
Height : 10.056
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

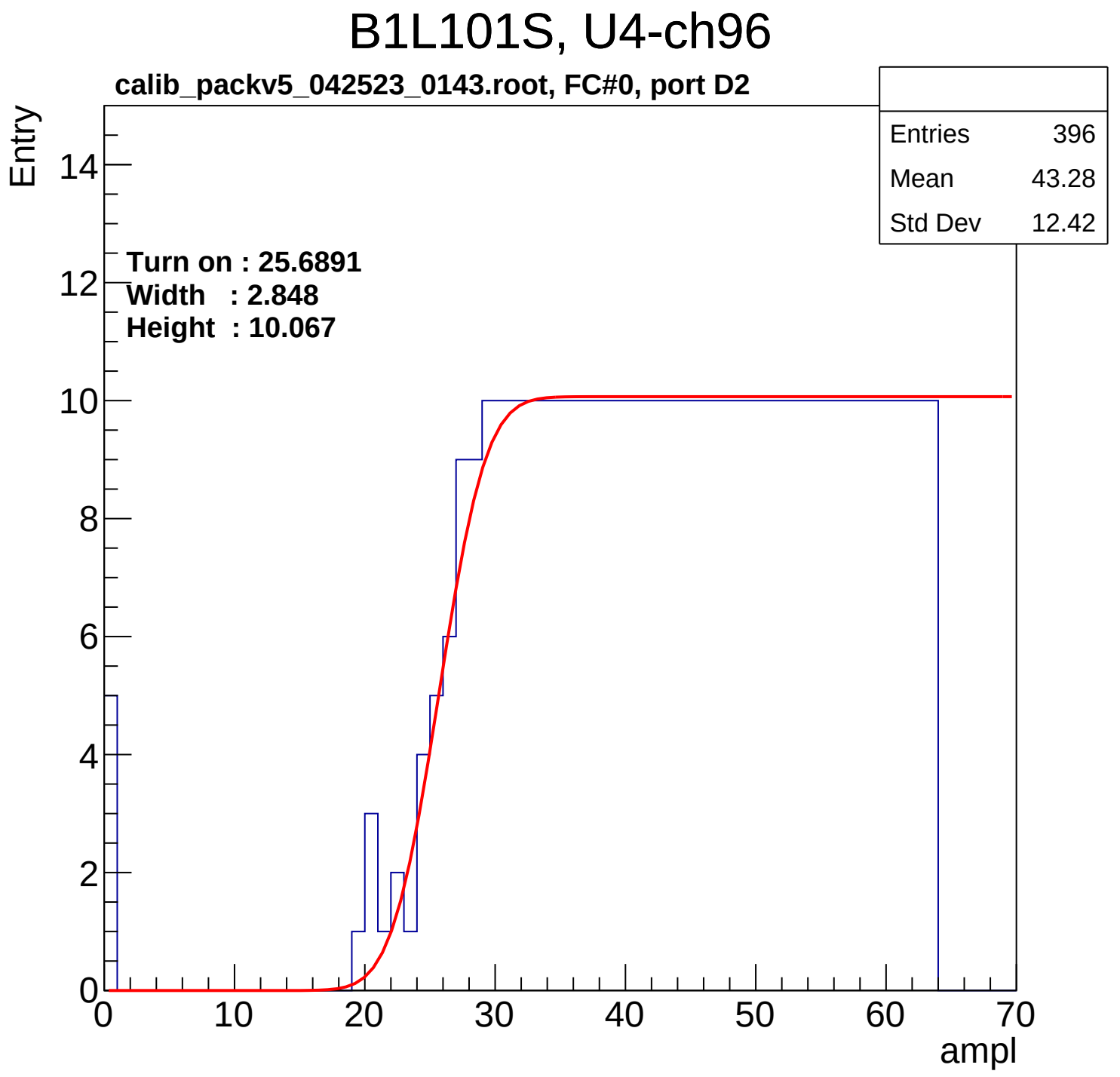

B1L101S, U4-ch91
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.67
Std Dev 11.15
Turn on : 27.4359
Width : 3.572
Height : 10.081
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

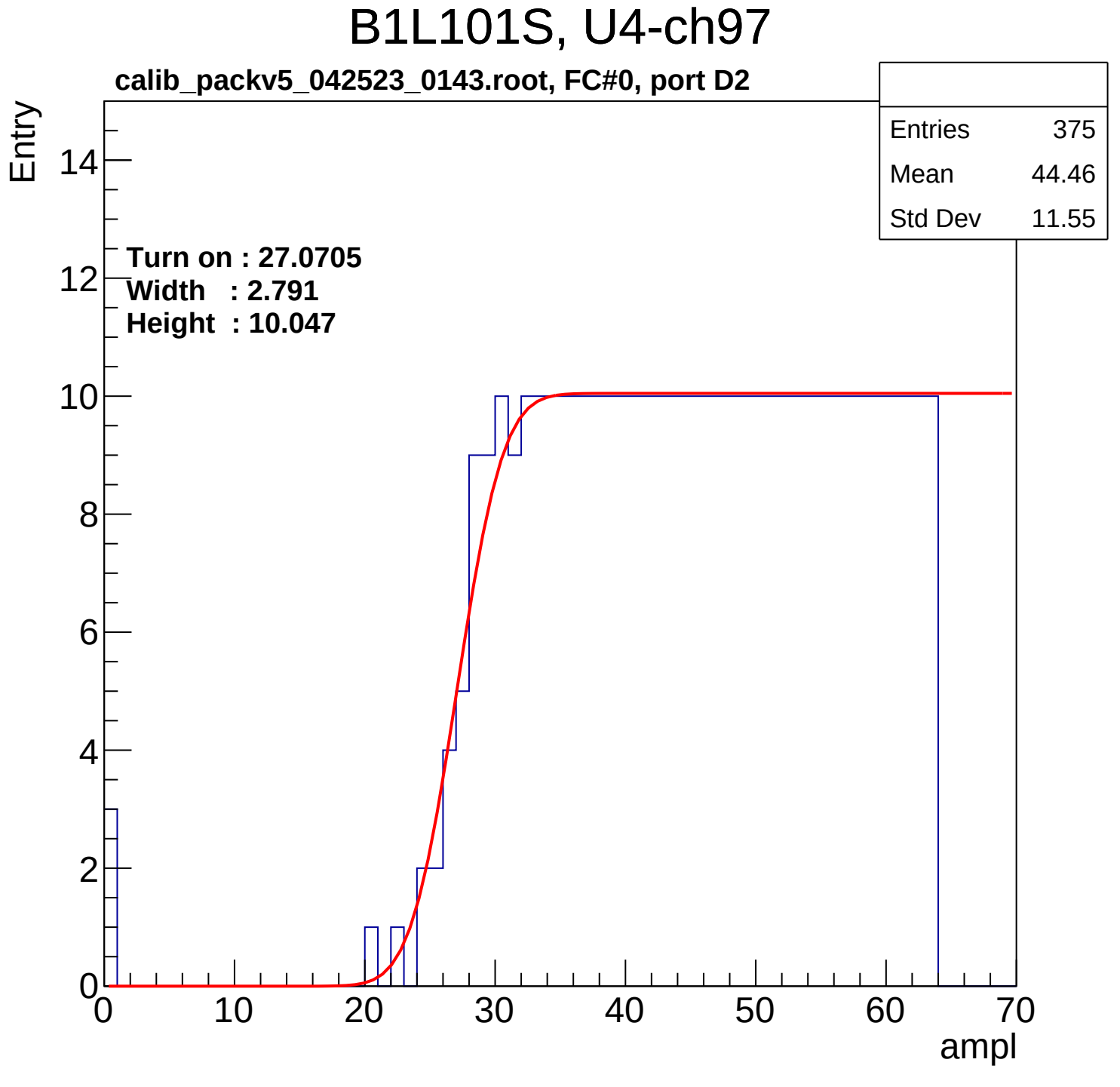

B1L101S, U4-ch92
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.27
Std Dev 11.99
Turn on : 26.8471
Width : 4.105
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

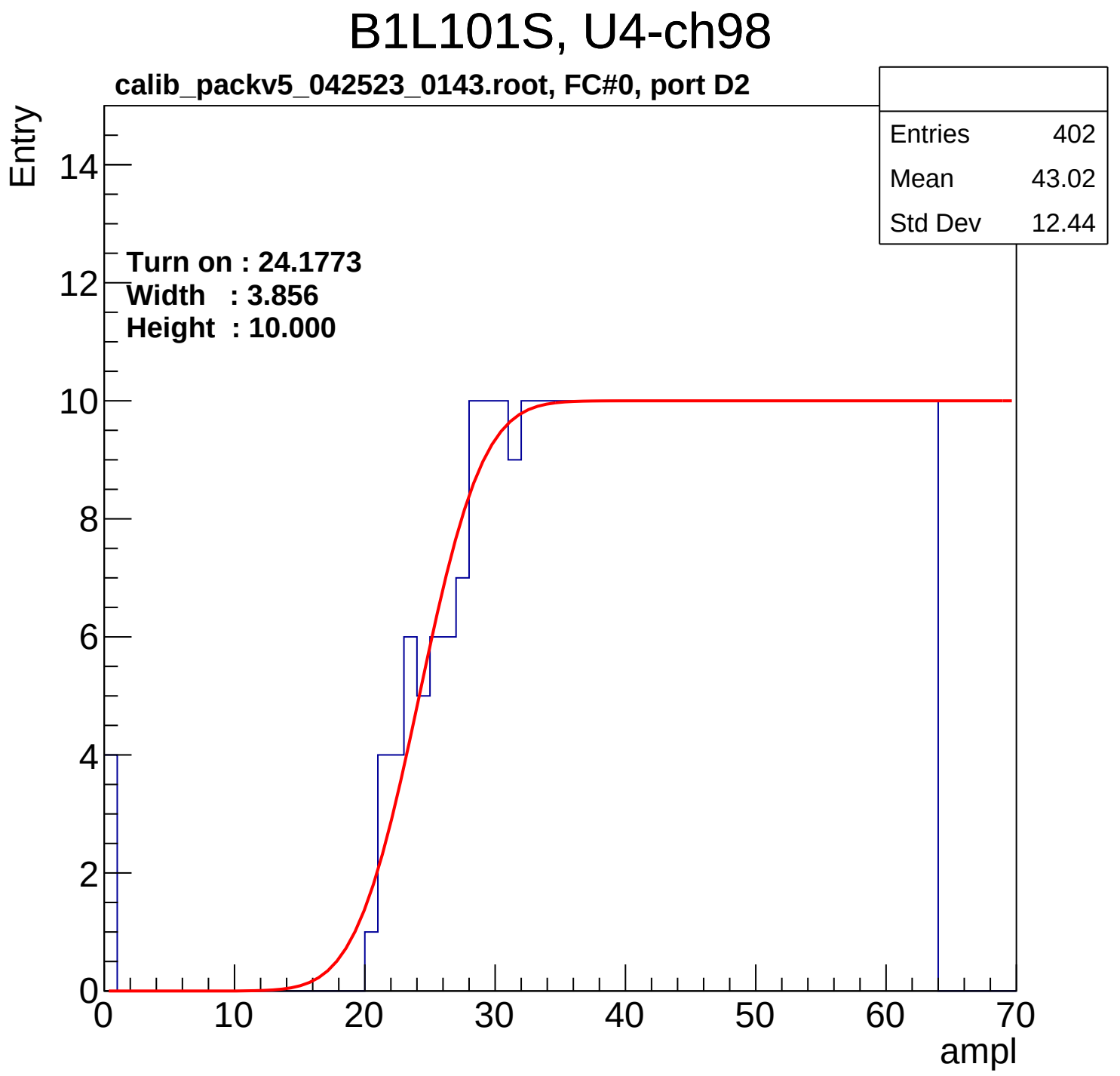

B1L101S, U4-ch93
calib_packv5_042523_0143.root, FC#0, port D2
Entries 390
Mean 43.5
Std Dev 12.46
Turn on : 26.4877
Width : 4.332
Height : 10.097
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

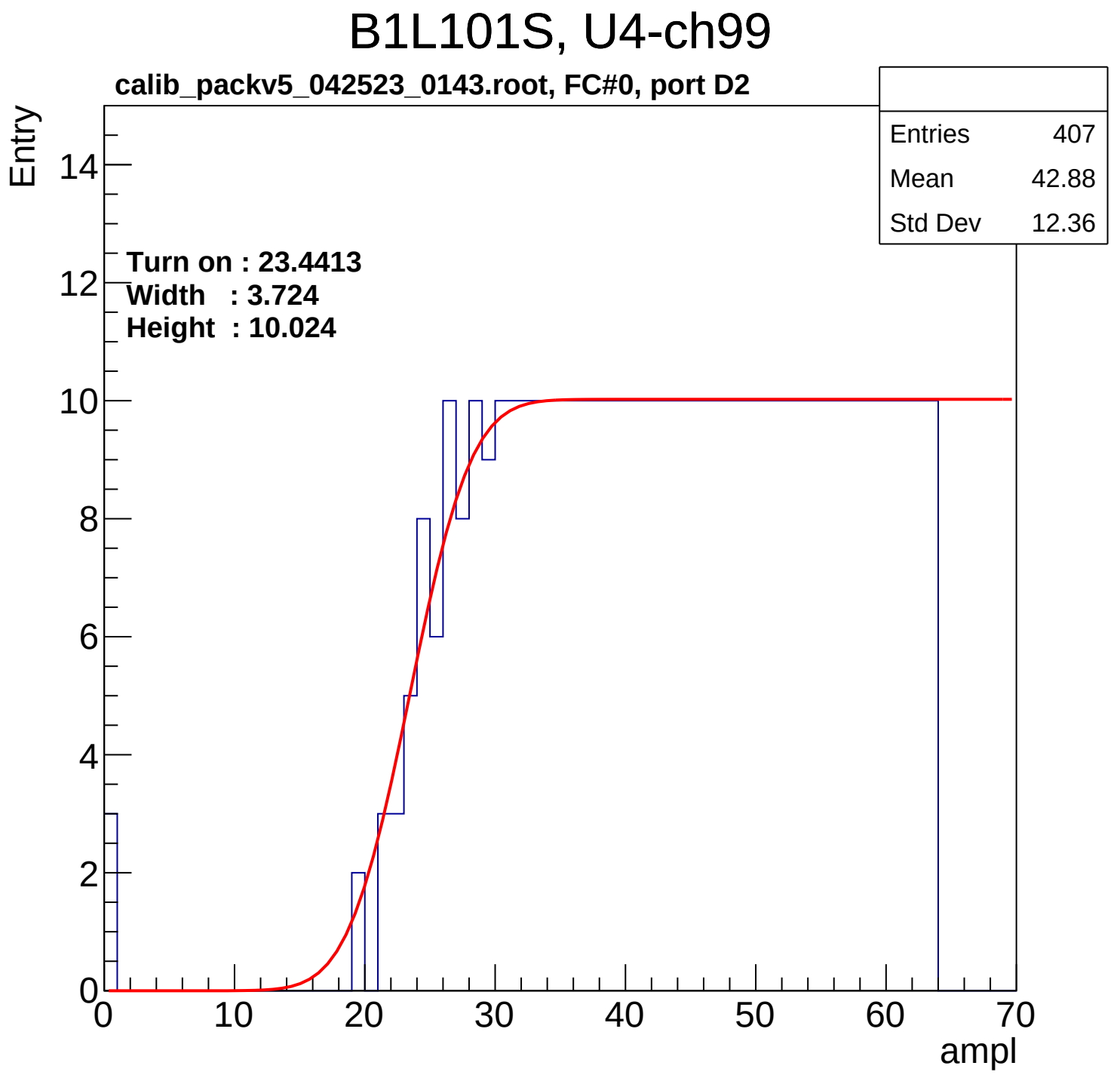

B1L101S, U4-ch94
calib_packv5_042523_0143.root, FC#0, port D2
Entries 396
Mean 43.47
Std Dev 11.94
Turn on : 24.5719
Width : 3.460
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

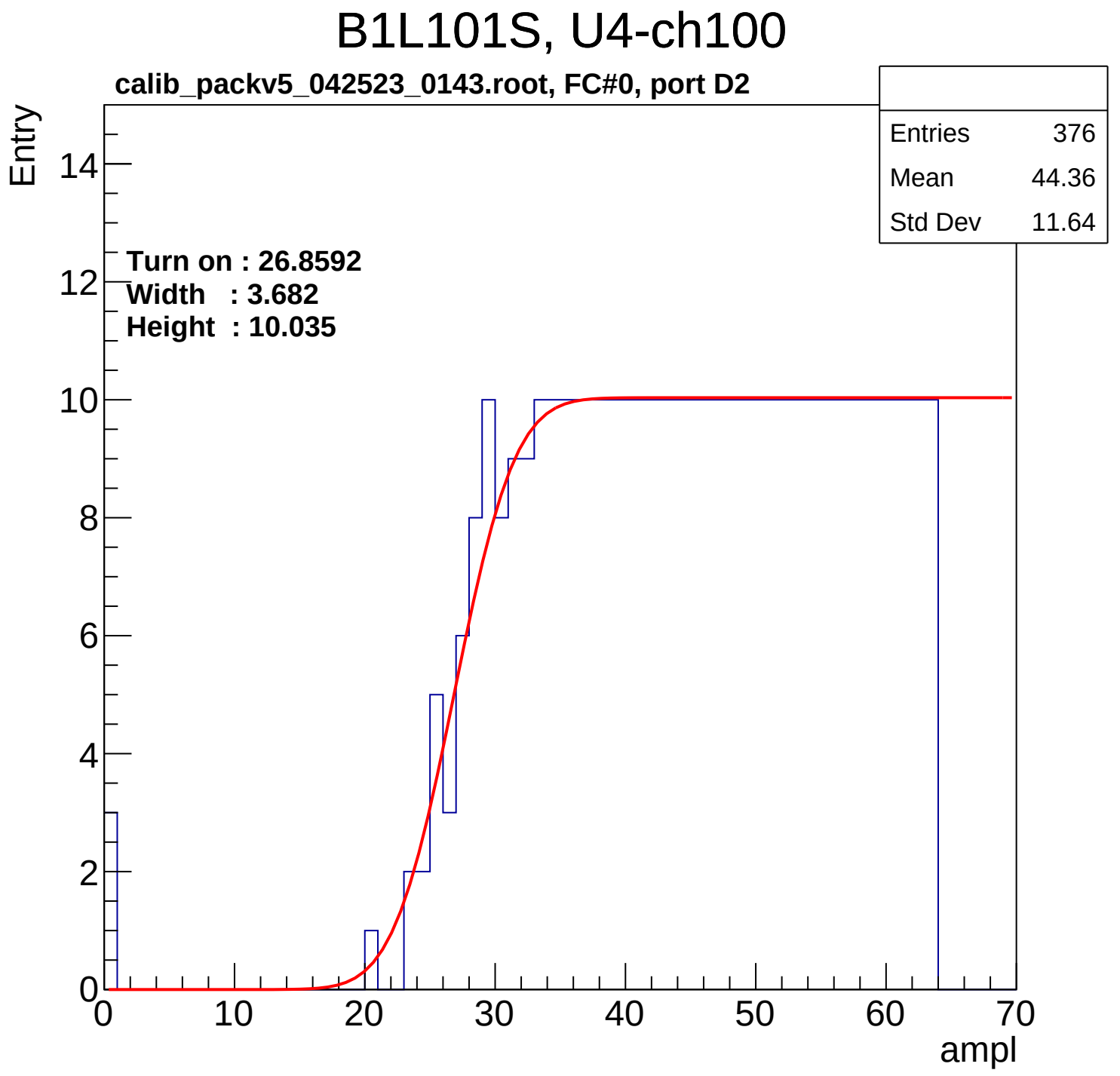

B1L101S, U4-ch95
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.11
Std Dev 12.05
Turn on : 26.5830
Width : 3.577
Height : 10.010
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

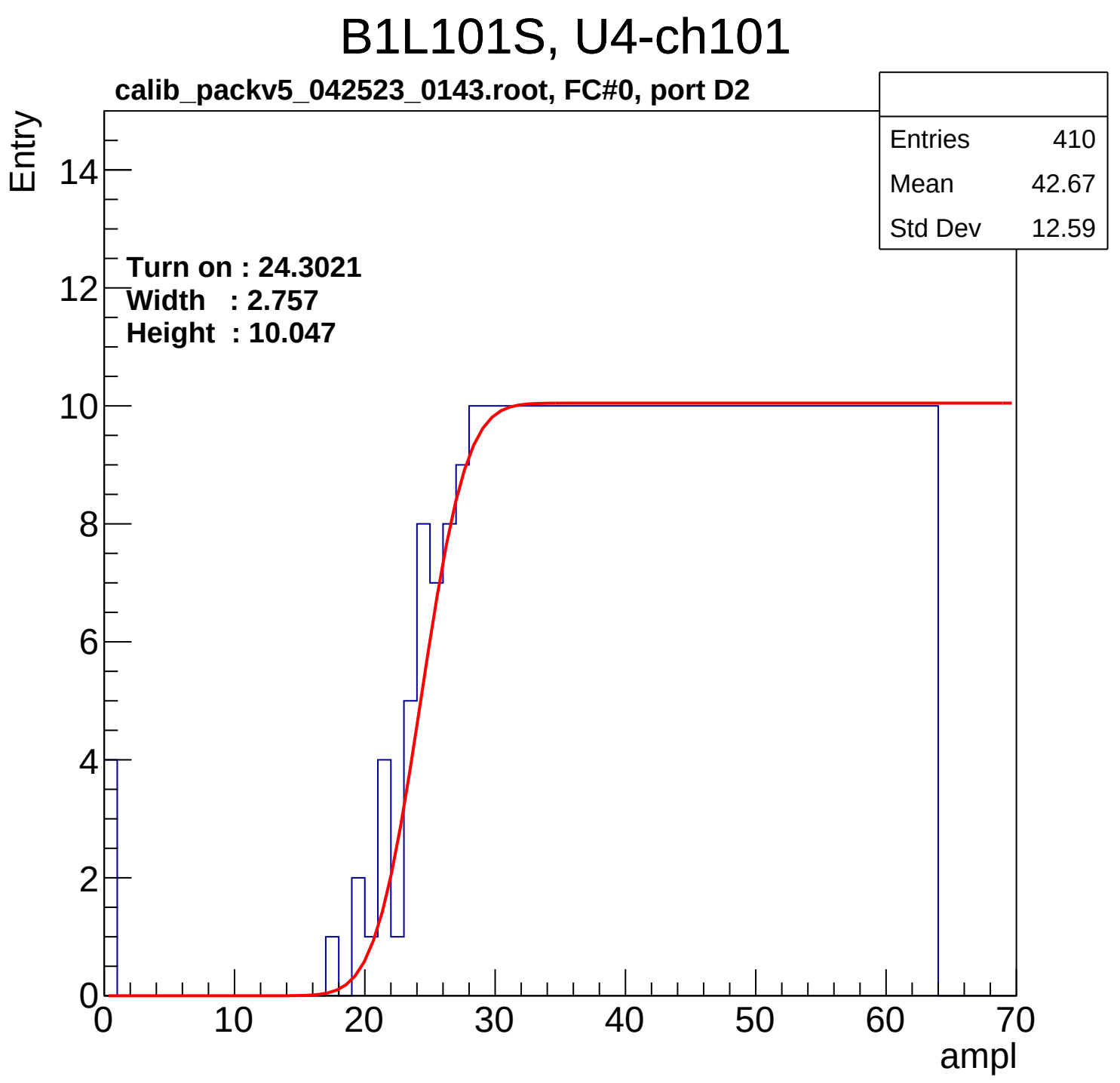

B1L101S, U4-ch96
calib_packv5_042523_0143.root, FC#0, port D2
Entries 396
Mean 43.28
Std Dev 12.42
Turn on : 25.6891
Width : 2.848
Height : 10.067
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

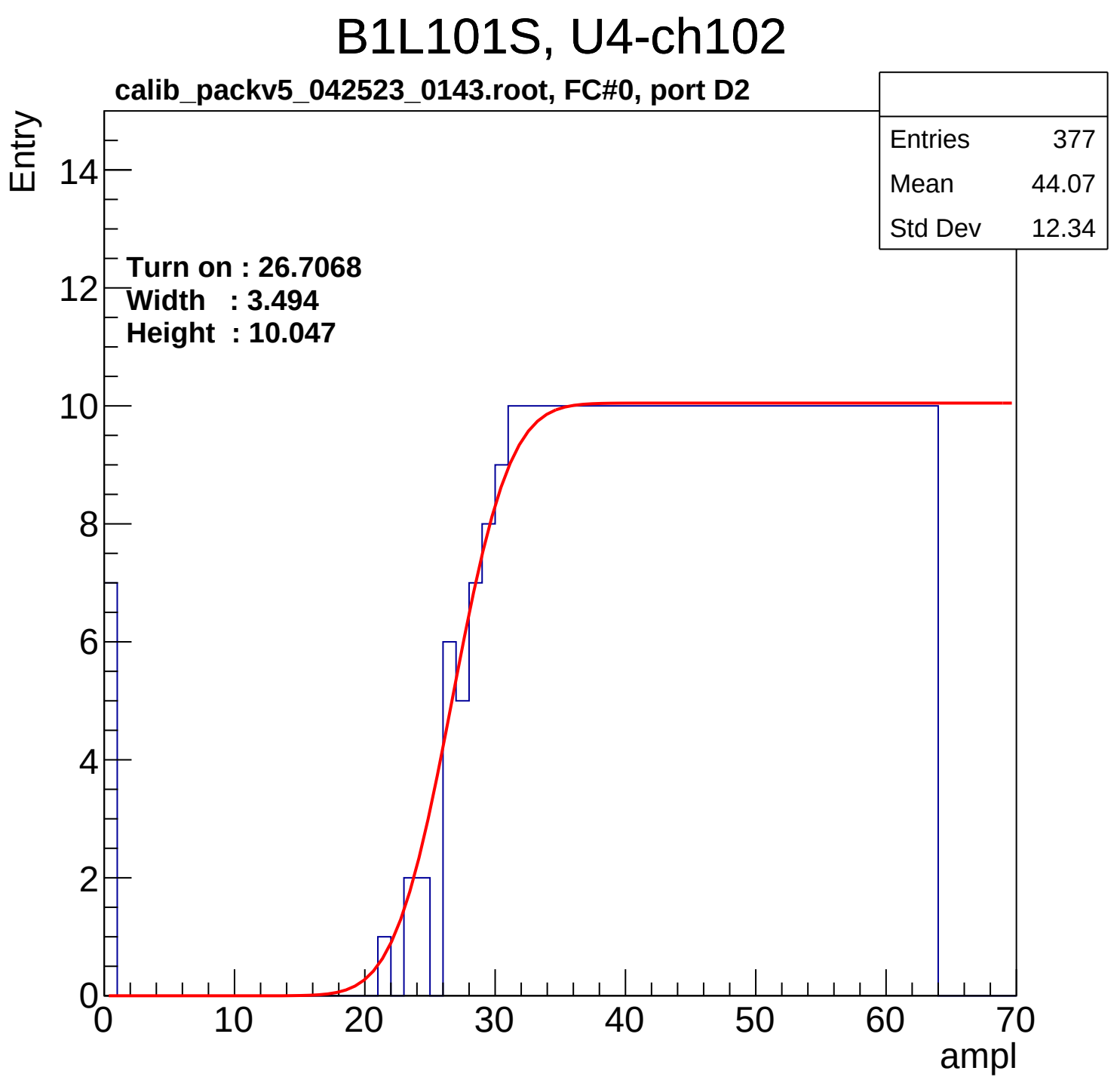

B1L101S, U4-ch97
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.46
Std Dev 11.55
Turn on : 27.0705
Width : 2.791
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

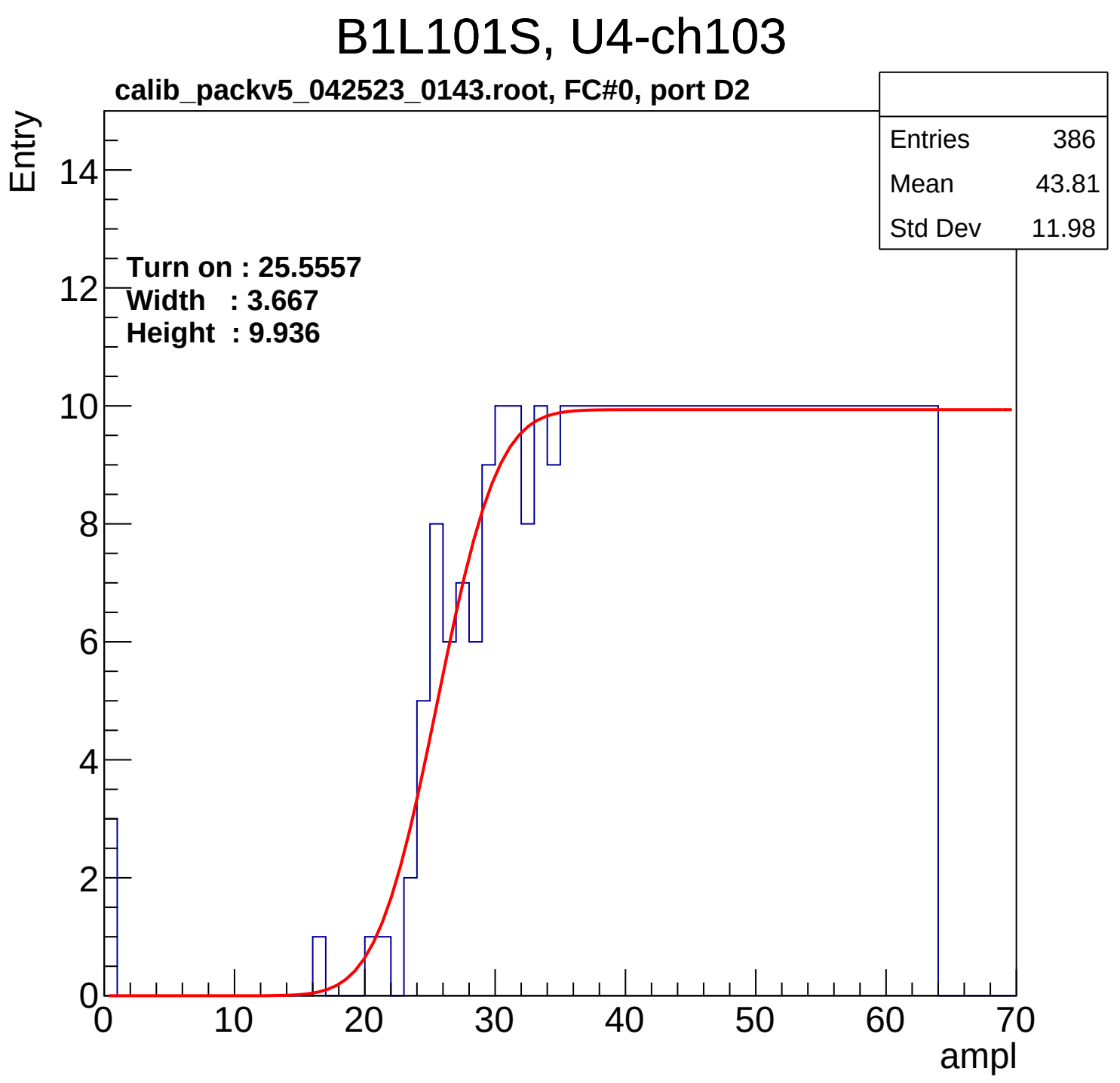

B1L101S, U4-ch98
calib_packv5_042523_0143.root, FC#0, port D2
Entries 402
Mean 43.02
Std Dev 12.44
Turn on : 24.1773
Width : 3.856
Height : 10.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

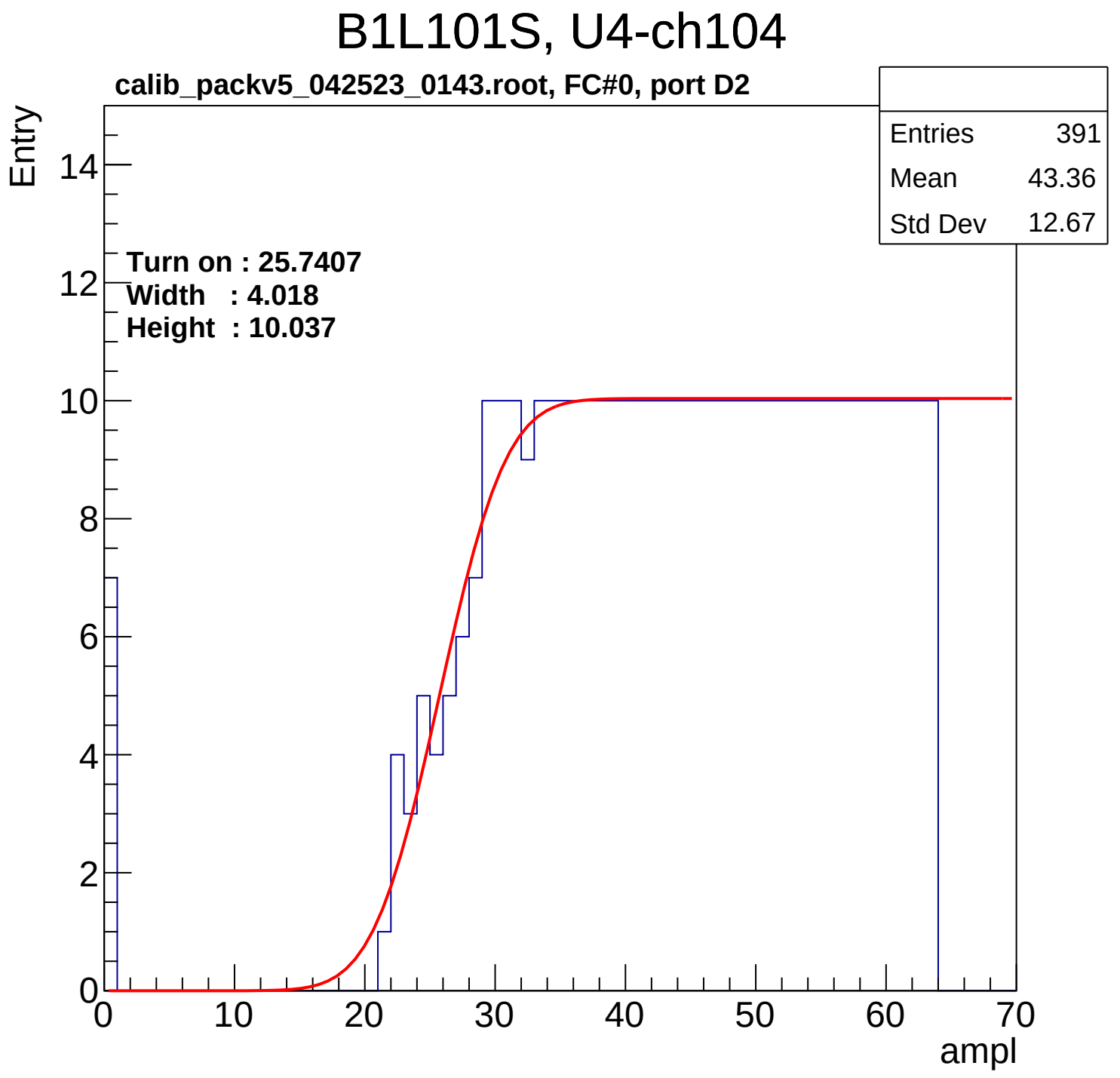

B1L101S, U4-ch99
calib_packv5_042523_0143.root, FC#0, port D2
Entries 407
Mean 42.88
Std Dev 12.36
Turn on : 23.4413
Width : 3.724
Height : 10.024
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

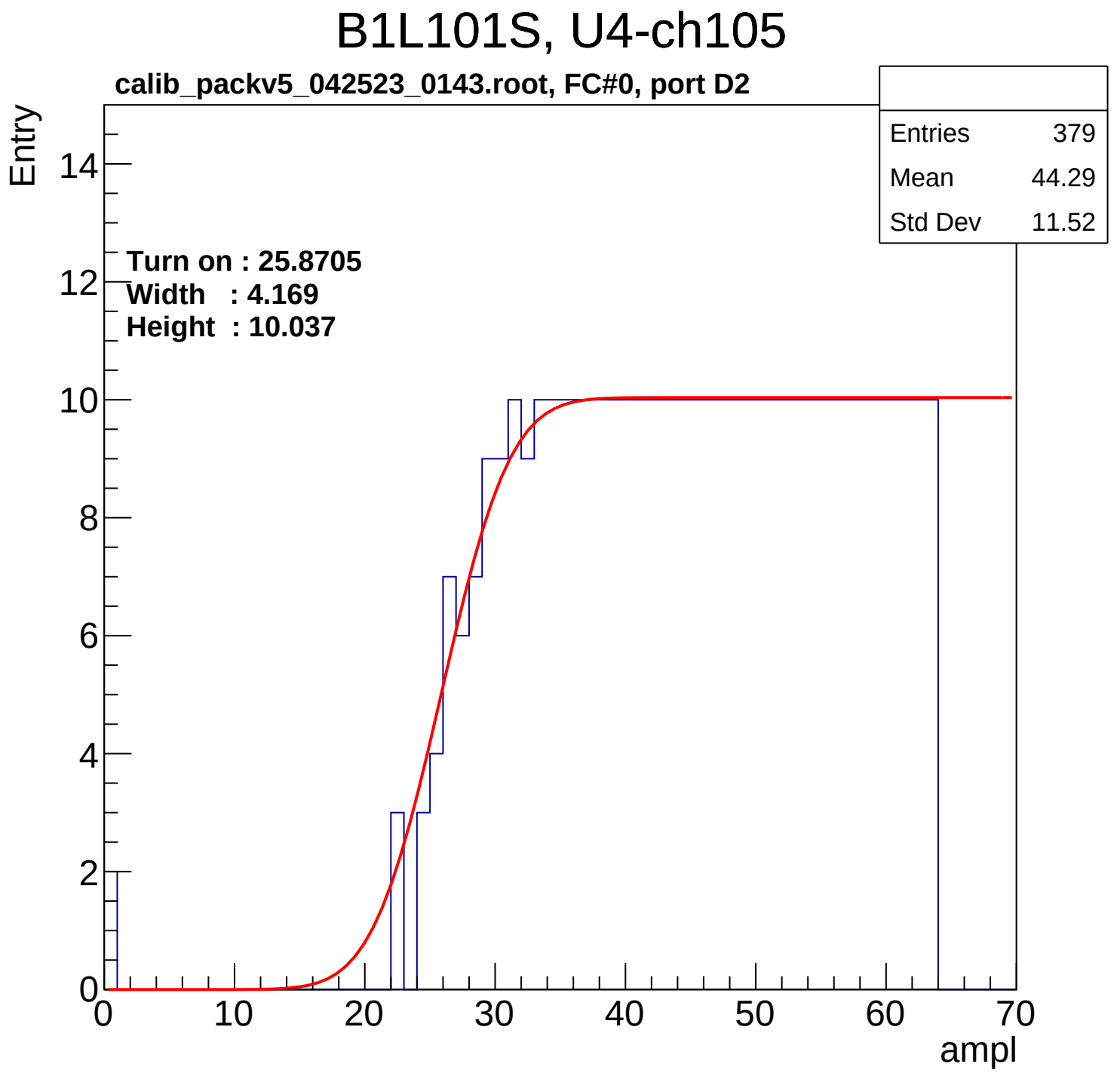

B1L101S, U4-ch100
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.36
Std Dev 11.64
Turn on : 26.8592
Width : 3.682
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

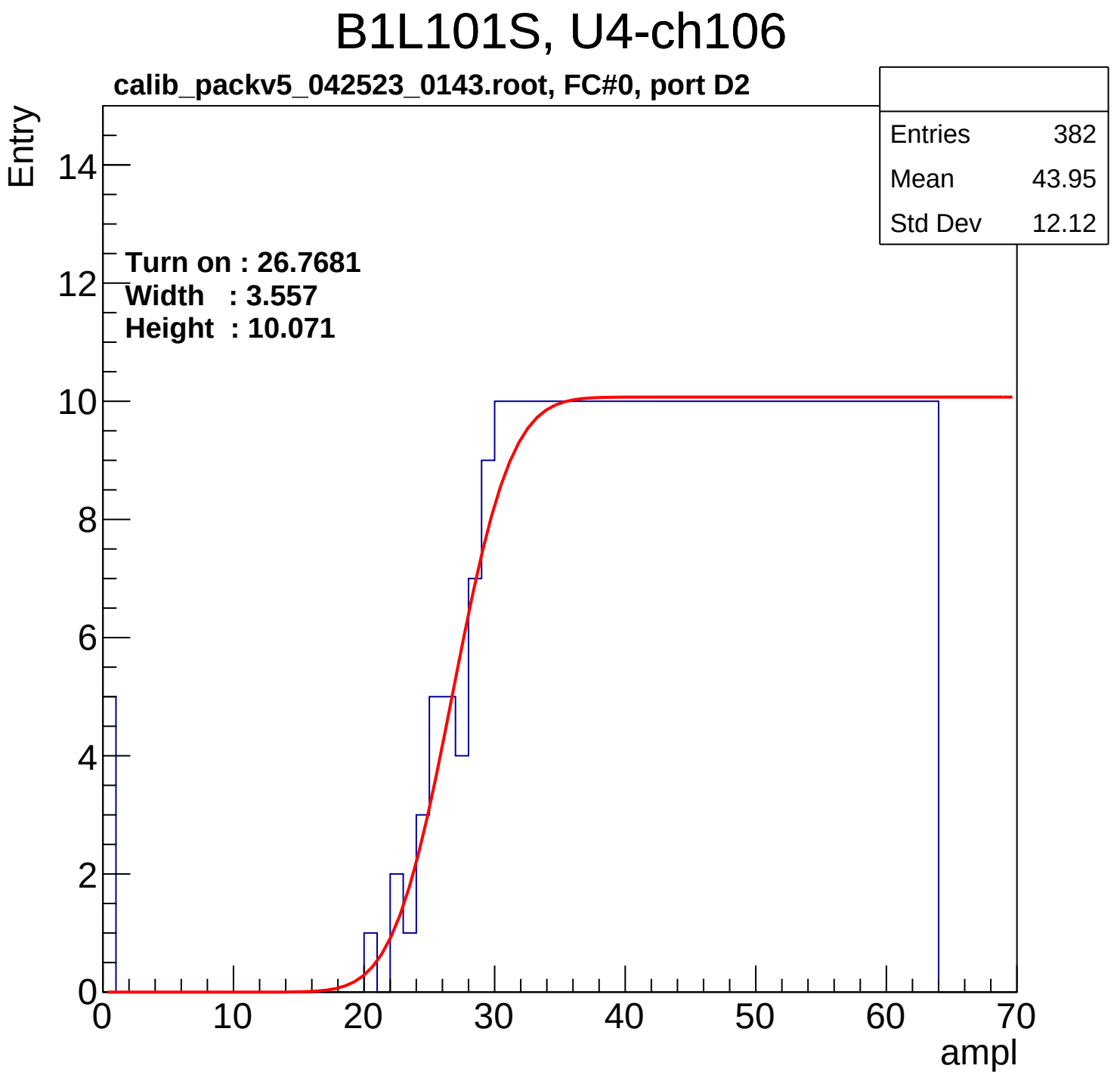

B1L101S, U4-ch101
calib_packv5_042523_0143.root, FC#0, port D2
Entries 410
Mean 42.67
Std Dev 12.59
Turn on : 24.3021
Width : 2.757
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

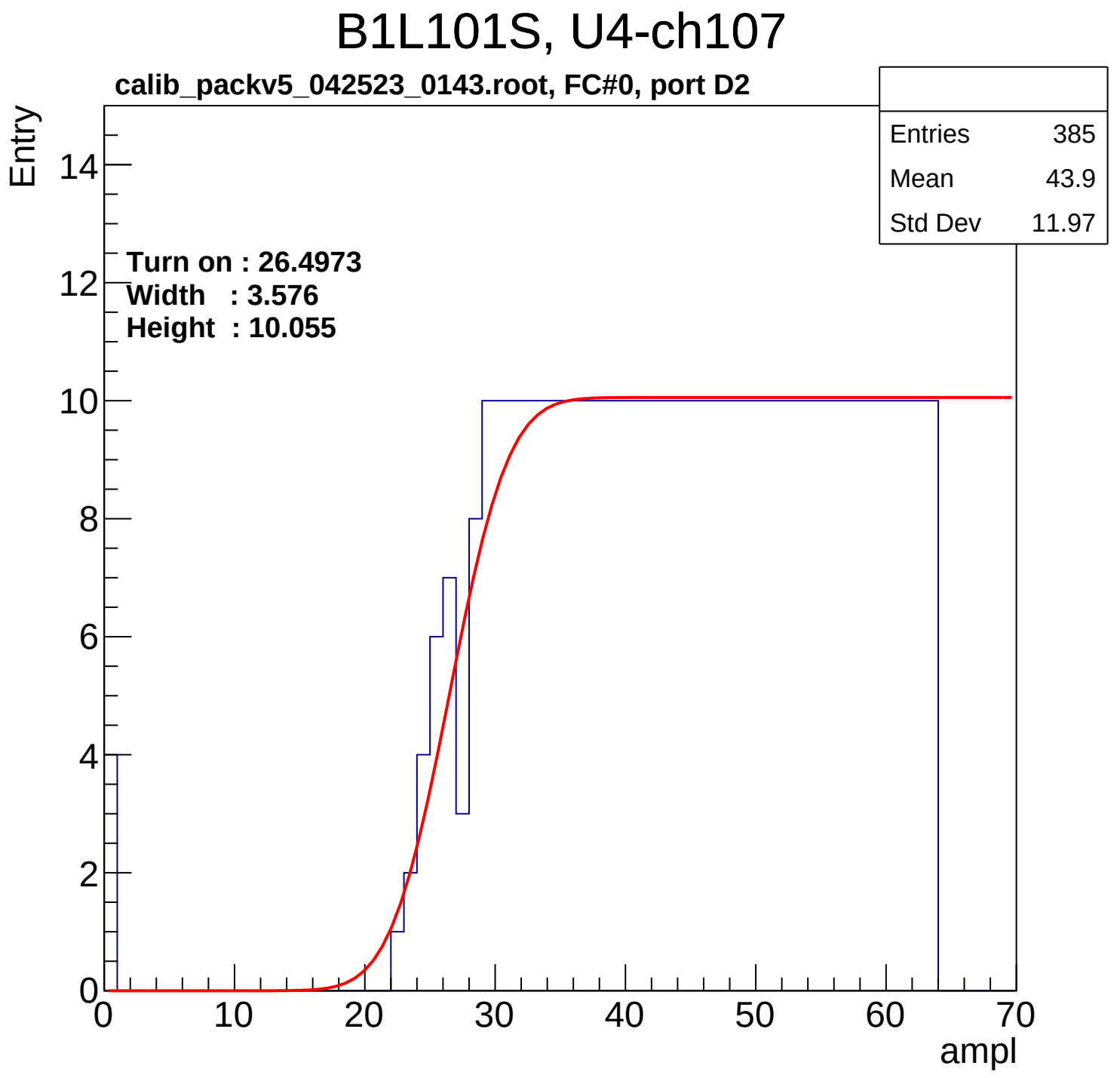

B1L101S, U4-ch102
calib_packv5_042523_0143.root, FC#0, port D2
Entries 377
Mean 44.07
Std Dev 12.34
Turn on : 26.7068
Width : 3.494
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

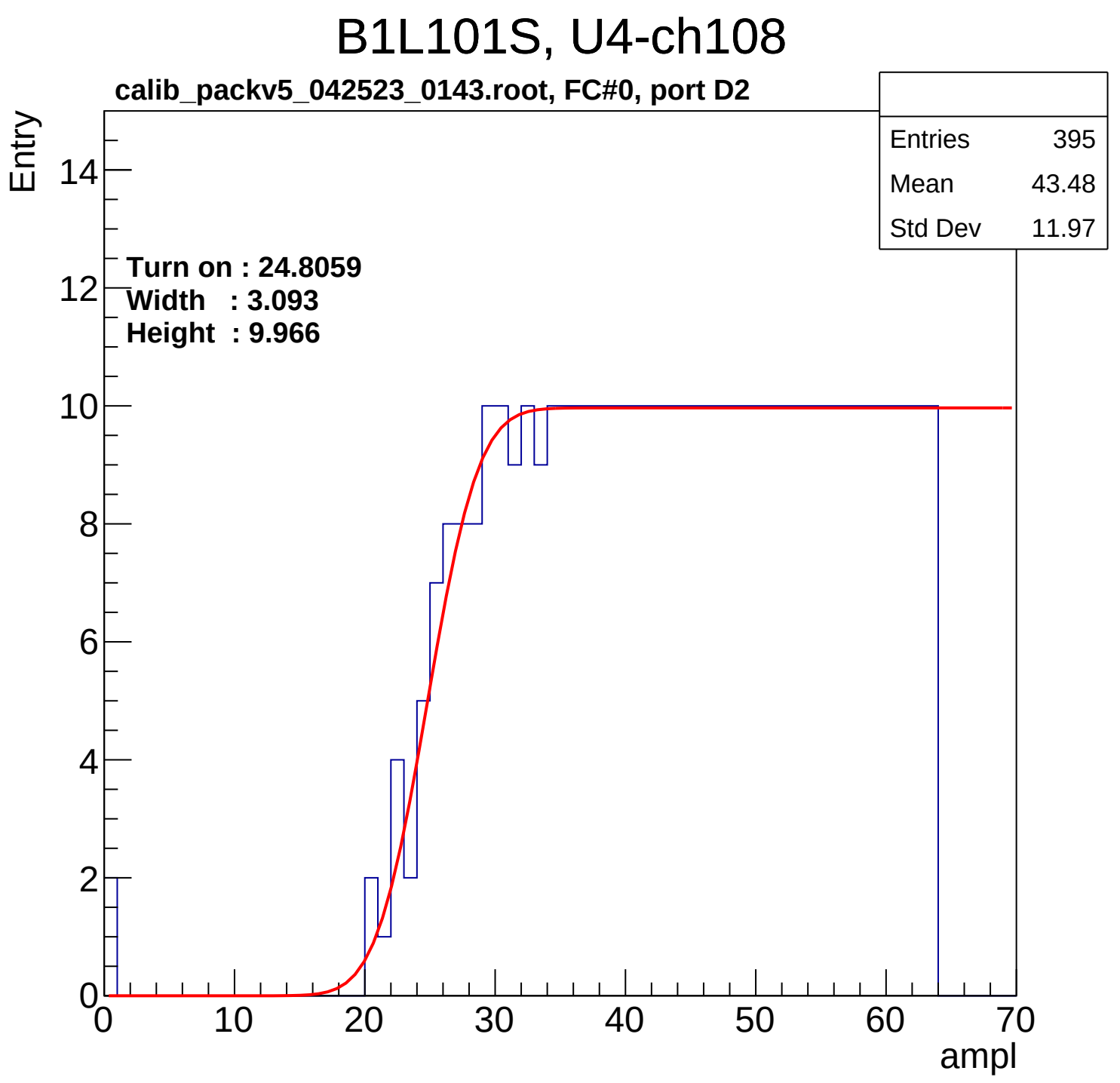

B1L101S, U4-ch103
calib_packv5_042523_0143.root, FC#0, port D2
Entries 386
Mean 43.81
Std Dev 11.98
Turn on : 25.5557
Width : 3.667
Height : 9.936
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

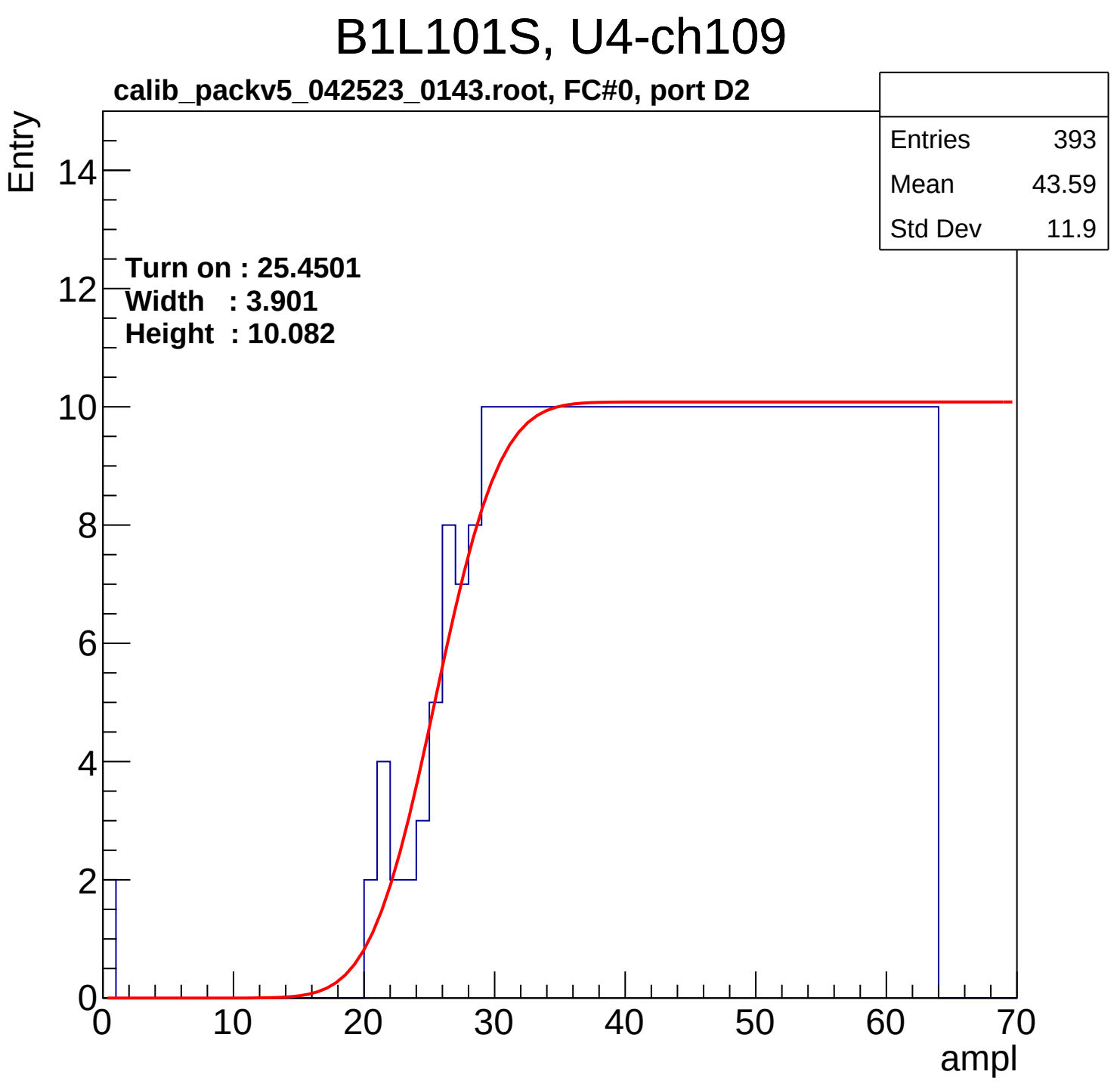

B1L101S, U4-ch104
calib_packv5_042523_0143.root, FC#0, port D2
Entries 391
Mean 43.36
Std Dev 12.67
Turn on : 25.7407
Width : 4.018
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

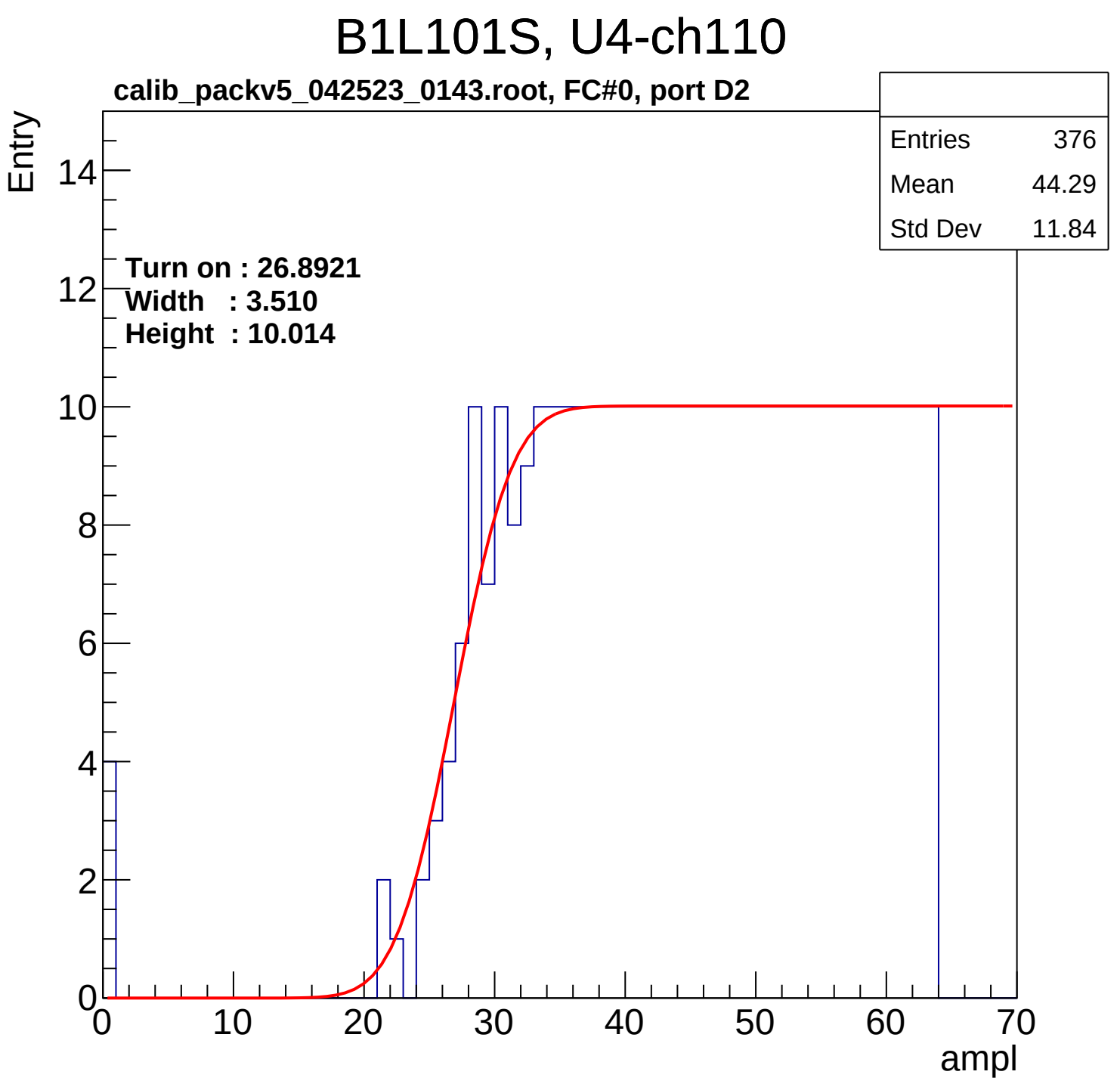

B1L101S, U4-ch105
calib_packv5_042523_0143.root, FC#0, port D2
Entries 379
Mean 44.29
Std Dev 11.52
Turn on : 25.8705
Width : 4.169
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

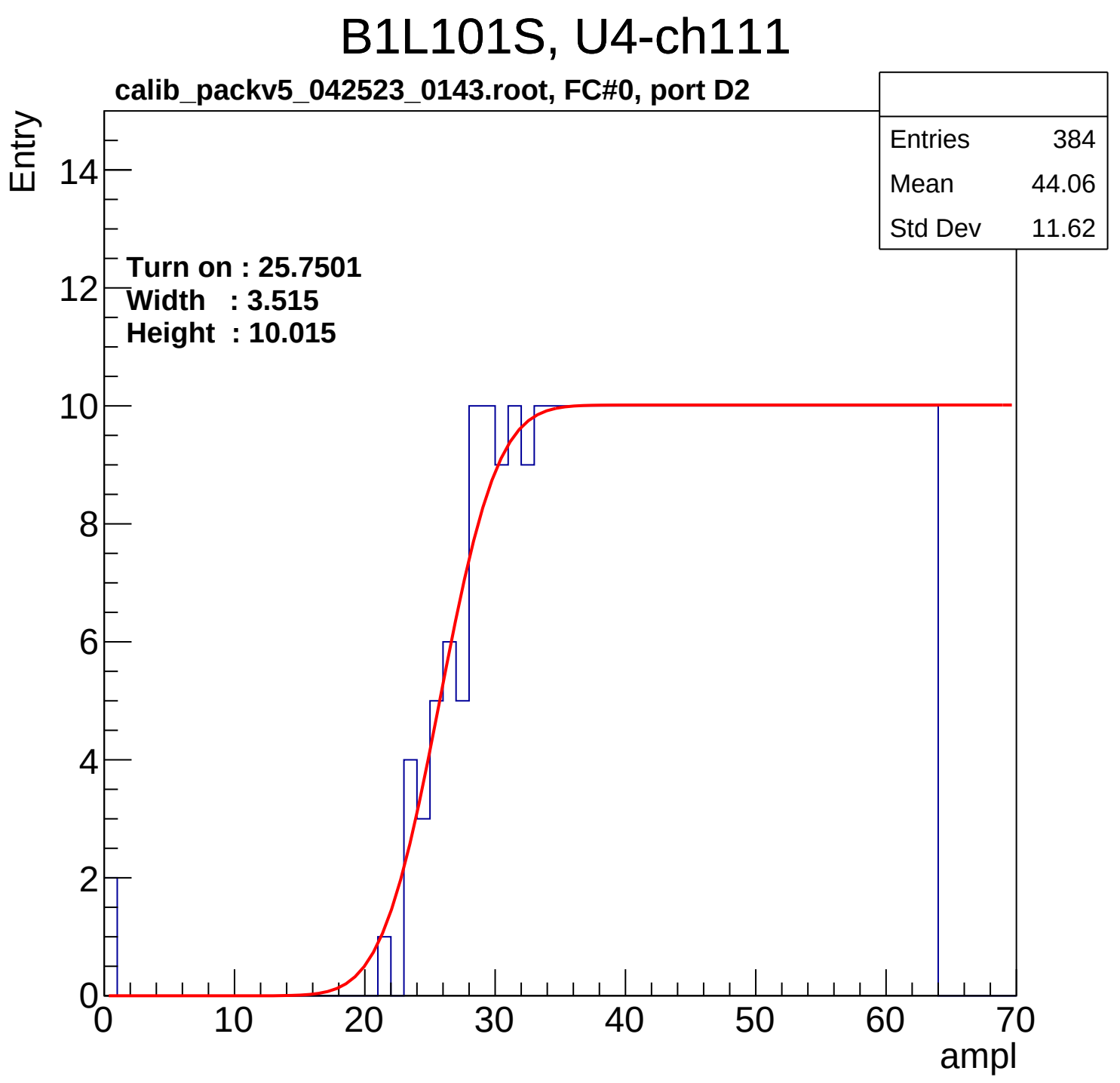

B1L101S, U4-ch106
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 43.95
Std Dev 12.12
Turn on : 26.7681
Width : 3.557
Height : 10.071
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

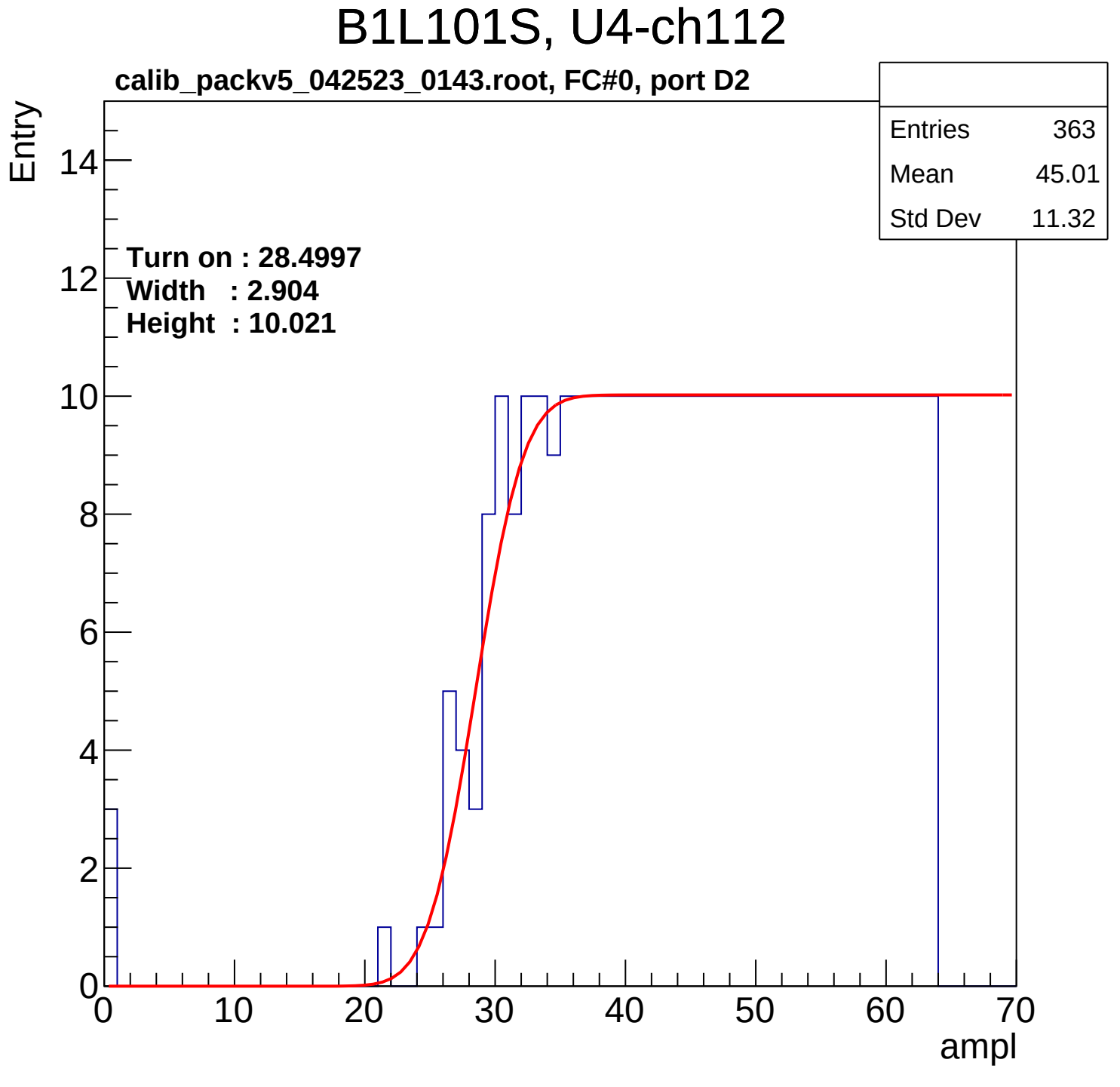

B1L101S, U4-ch107
calib_packv5_042523_0143.root, FC#0, port D2
Entries 385
Mean 43.9
Std Dev 11.97
Turn on : 26.4973
Width : 3.576
Height : 10.055
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

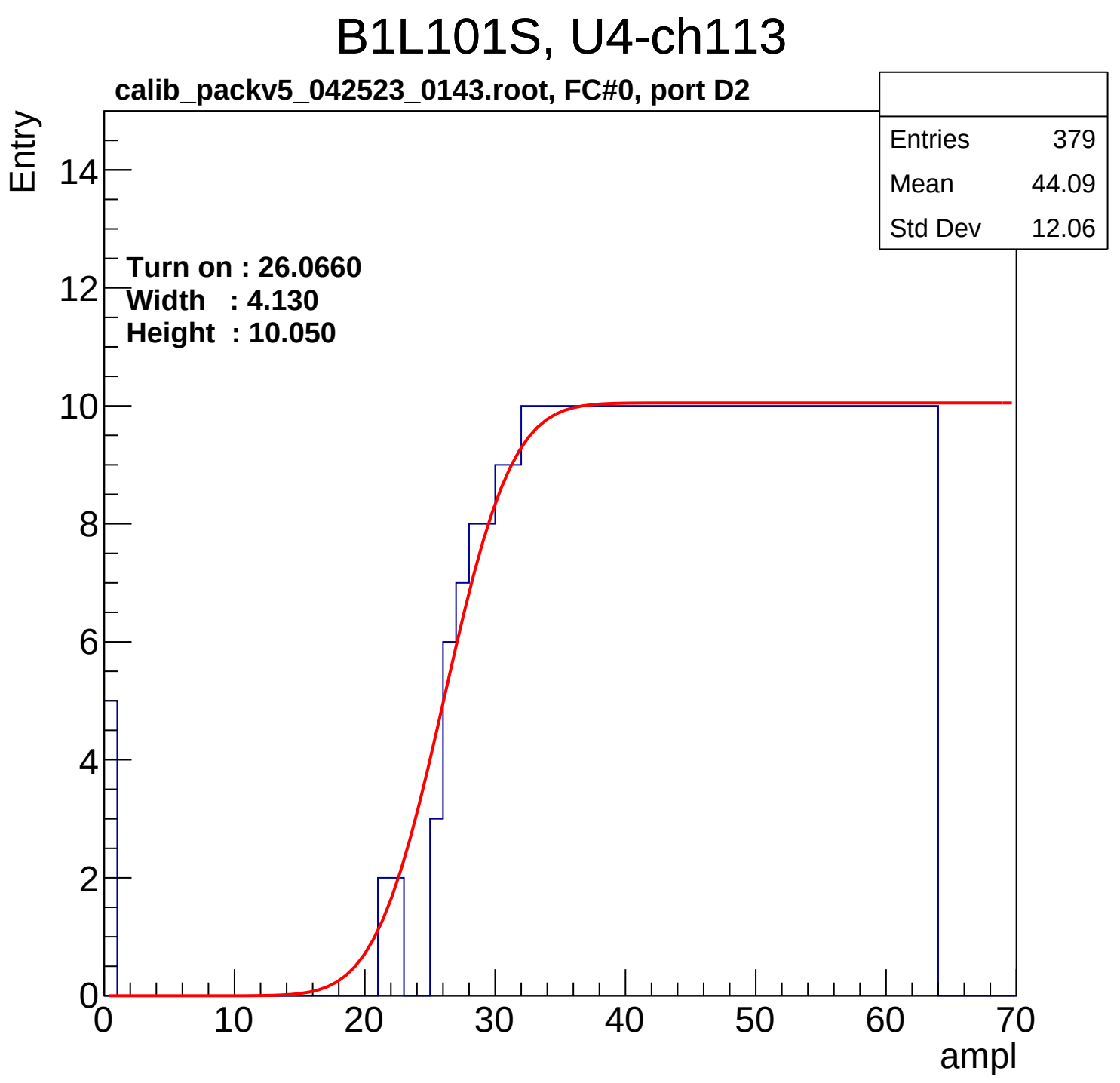

B1L101S, U4-ch108
calib_packv5_042523_0143.root, FC#0, port D2
Entries 395
Mean 43.48
Std Dev 11.97
Turn on : 24.8059
Width : 3.093
Height : 9.966
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

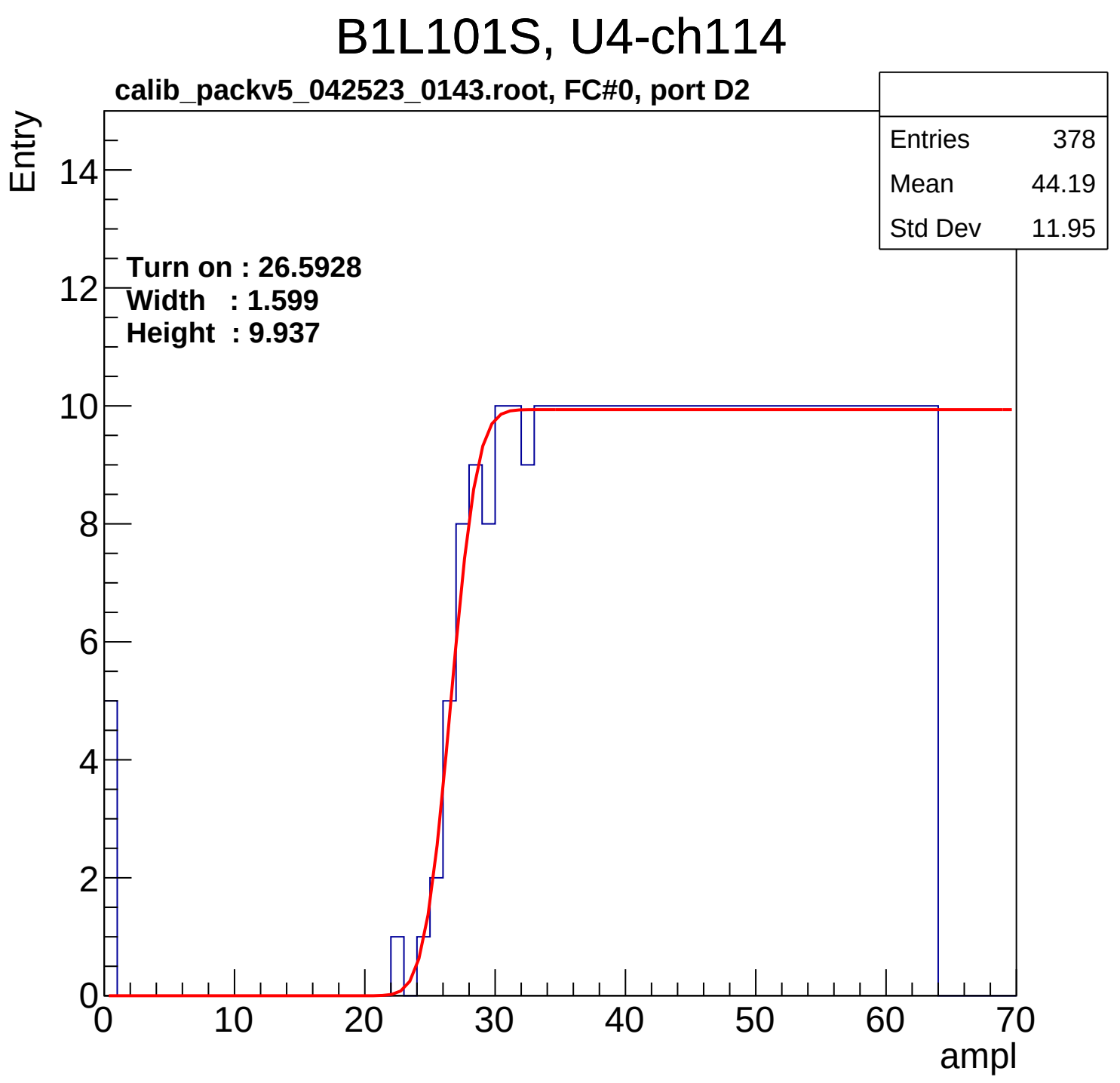

B1L101S, U4-ch109
calib_packv5_042523_0143.root, FC#0, port D2
Entries 393
Mean 43.59
Std Dev 11.9
Turn on : 25.4501
Width : 3.901
Height : 10.082
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

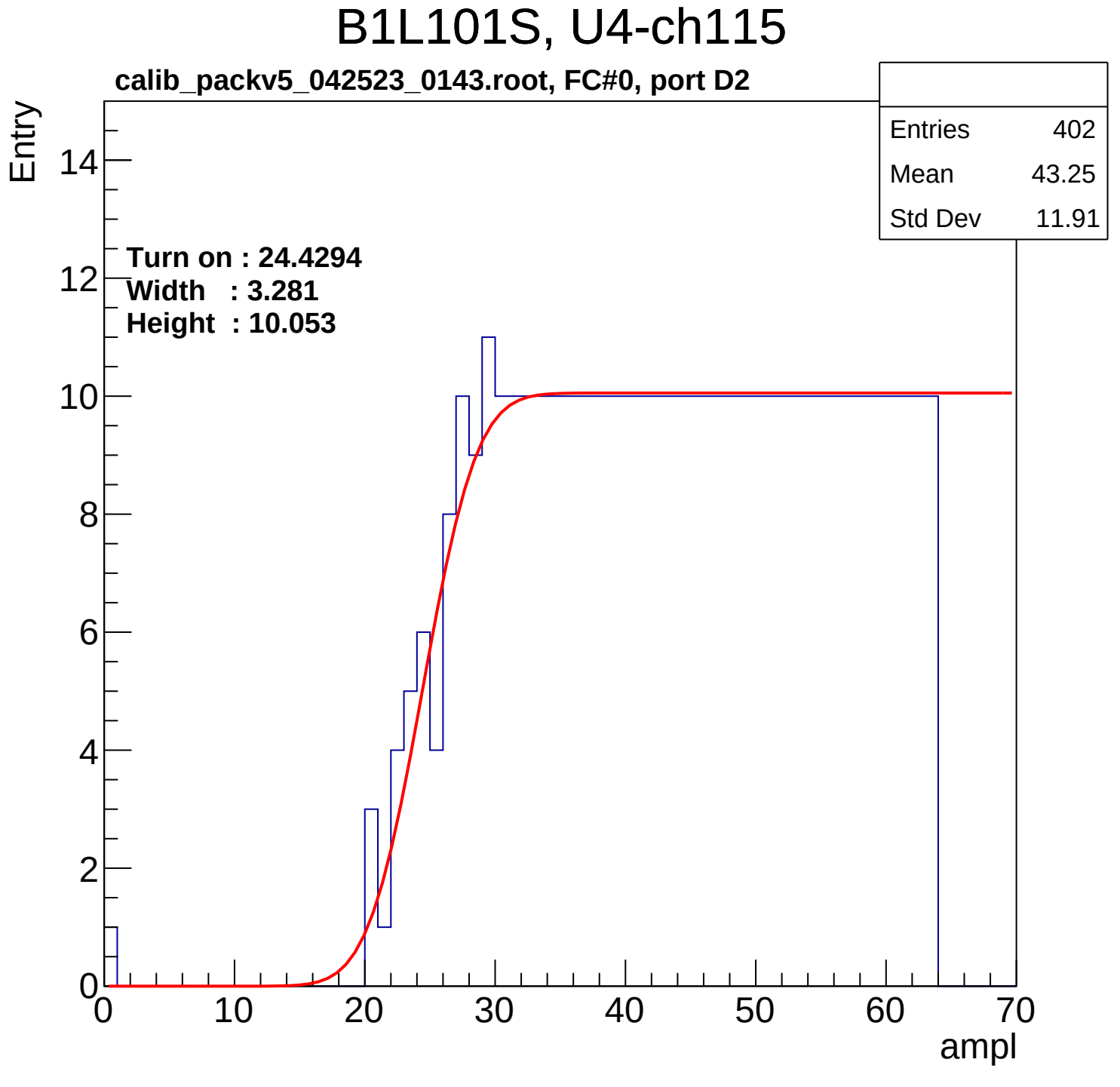

B1L101S, U4-ch110
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.29
Std Dev 11.84
Turn on : 26.8921
Width : 3.510
Height : 10.014
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

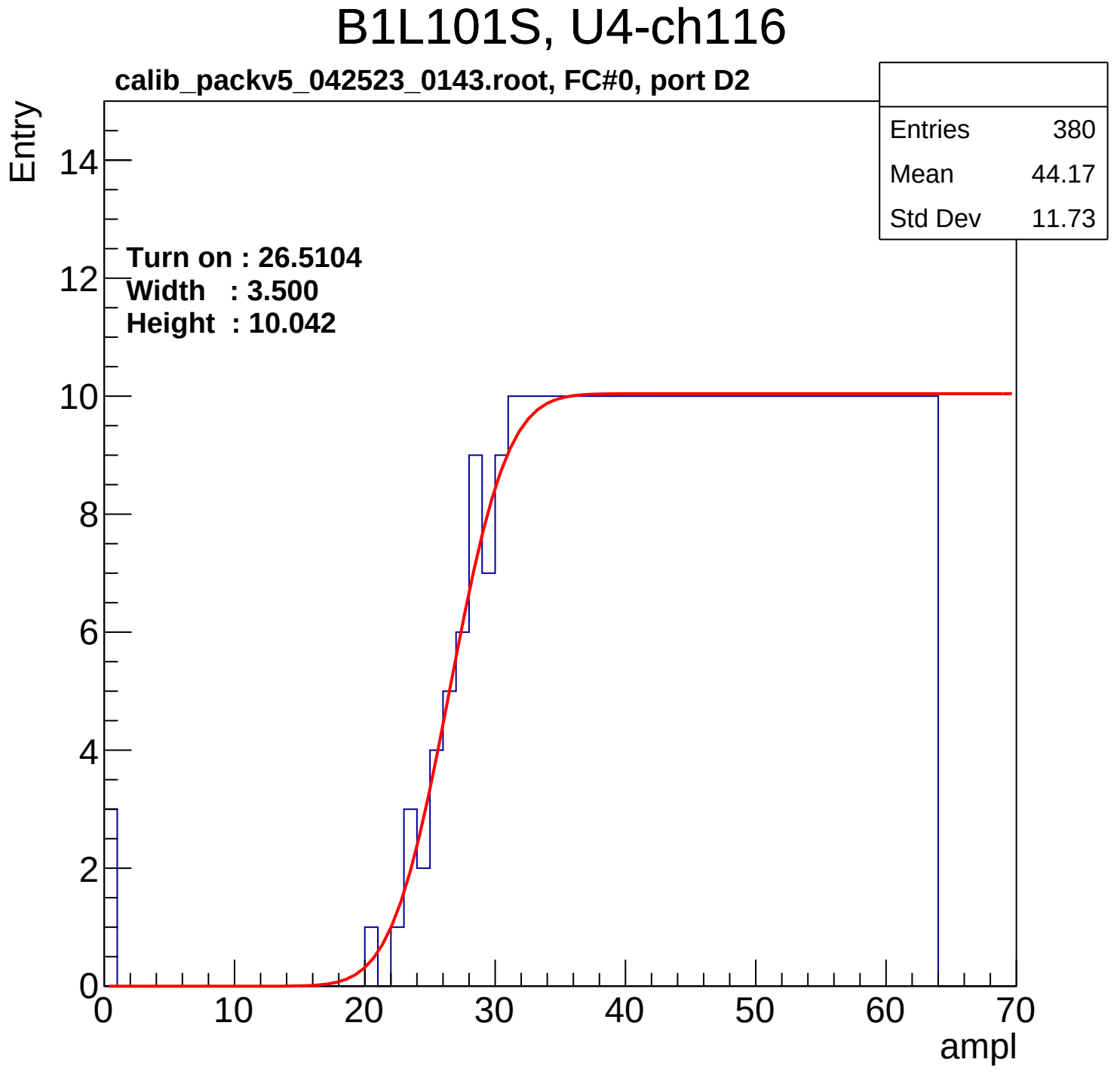

B1L101S, U4-ch111
calib_packv5_042523_0143.root, FC#0, port D2
Entries 384
Mean 44.06
Std Dev 11.62
Turn on : 25.7501
Width : 3.515
Height : 10.015
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

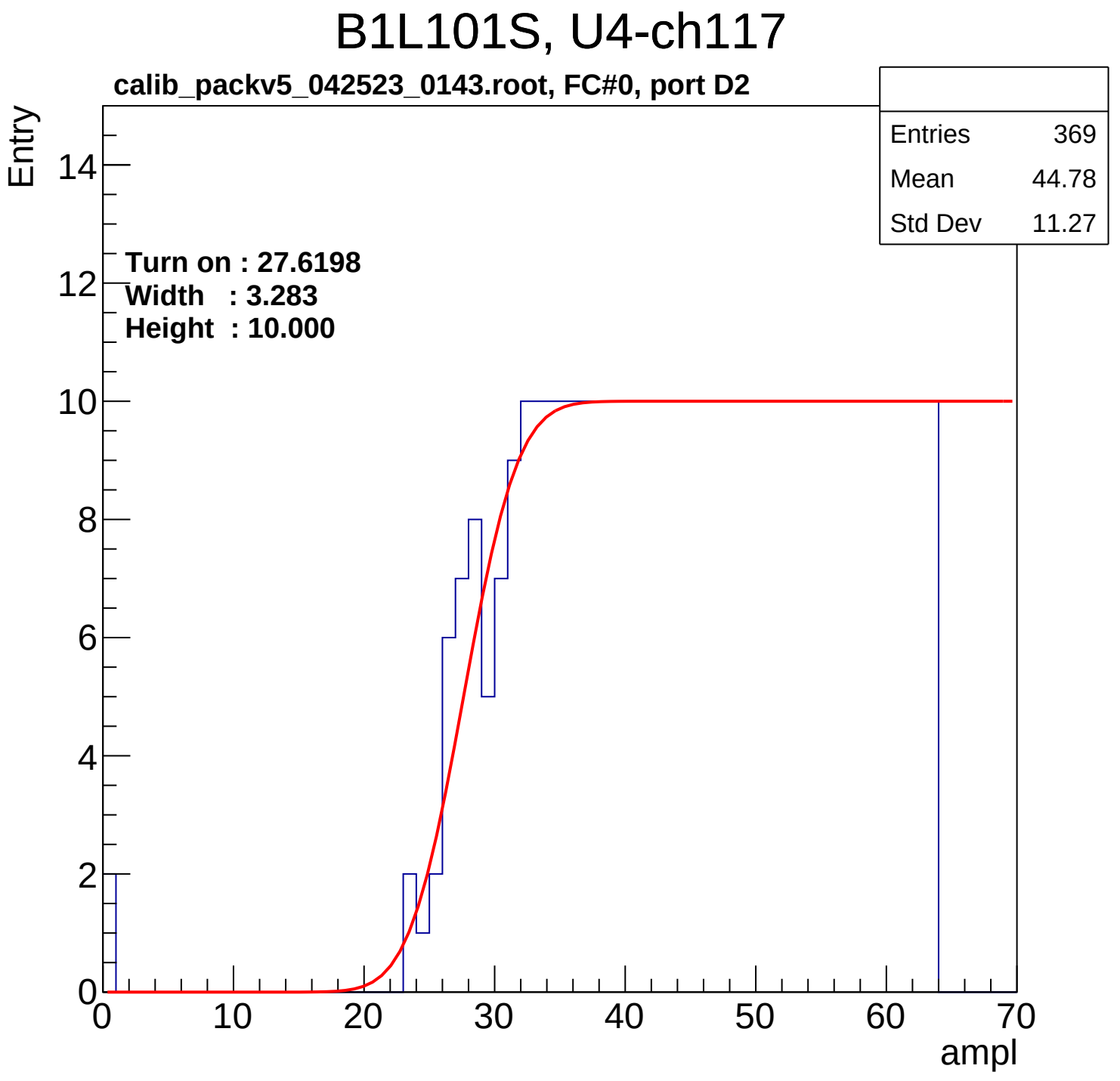

B1L101S, U4-ch112
calib_packv5_042523_0143.root, FC#0, port D2
Entries 363
Mean 45.01
Std Dev 11.32
Turn on : 28.4997
Width : 2.904
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

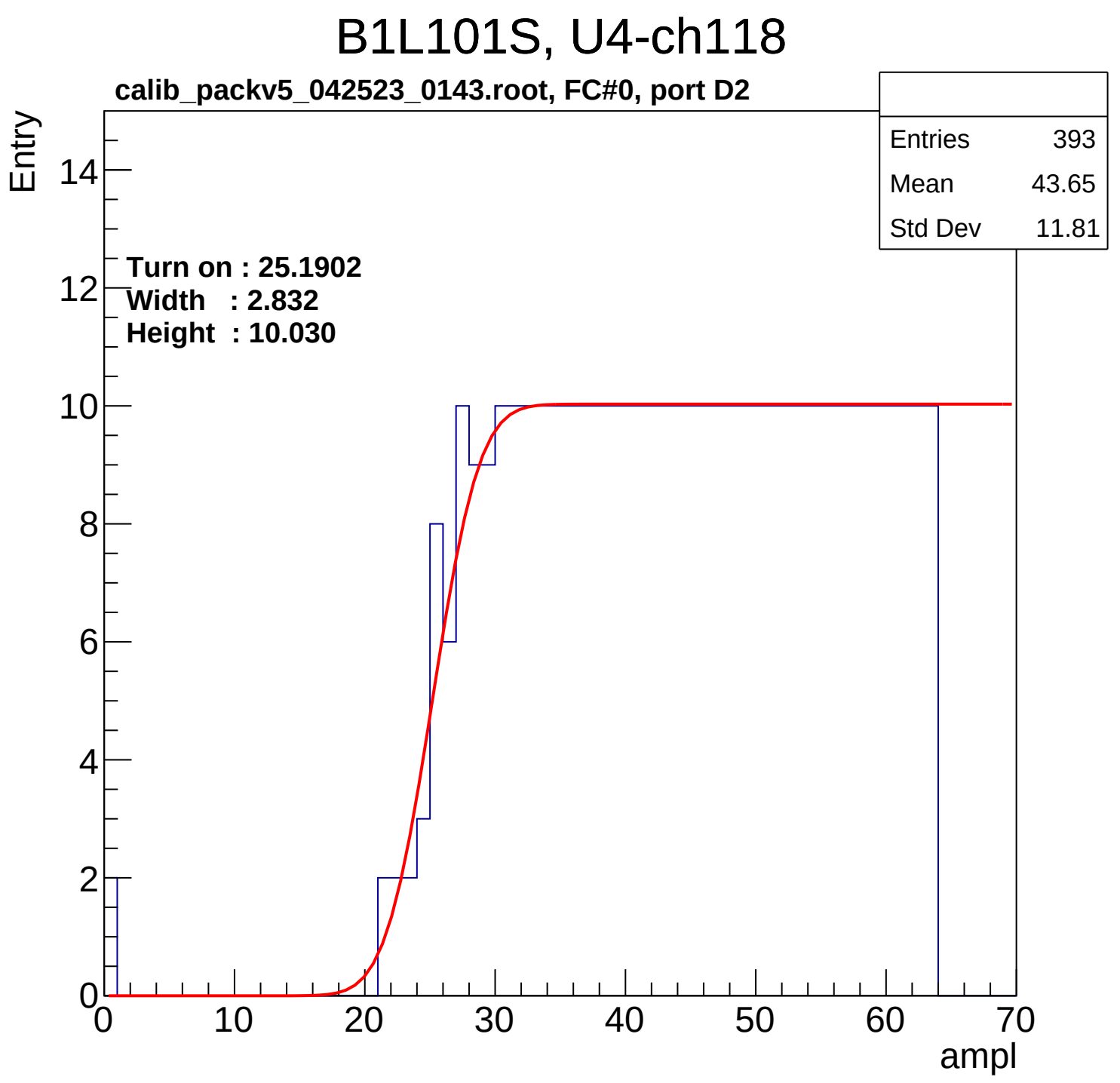

B1L101S, U4-ch113
calib_packv5_042523_0143.root, FC#0, port D2
Entries 379
Mean 44.09
Std Dev 12.06
Turn on : 26.0660
Width : 4.130
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

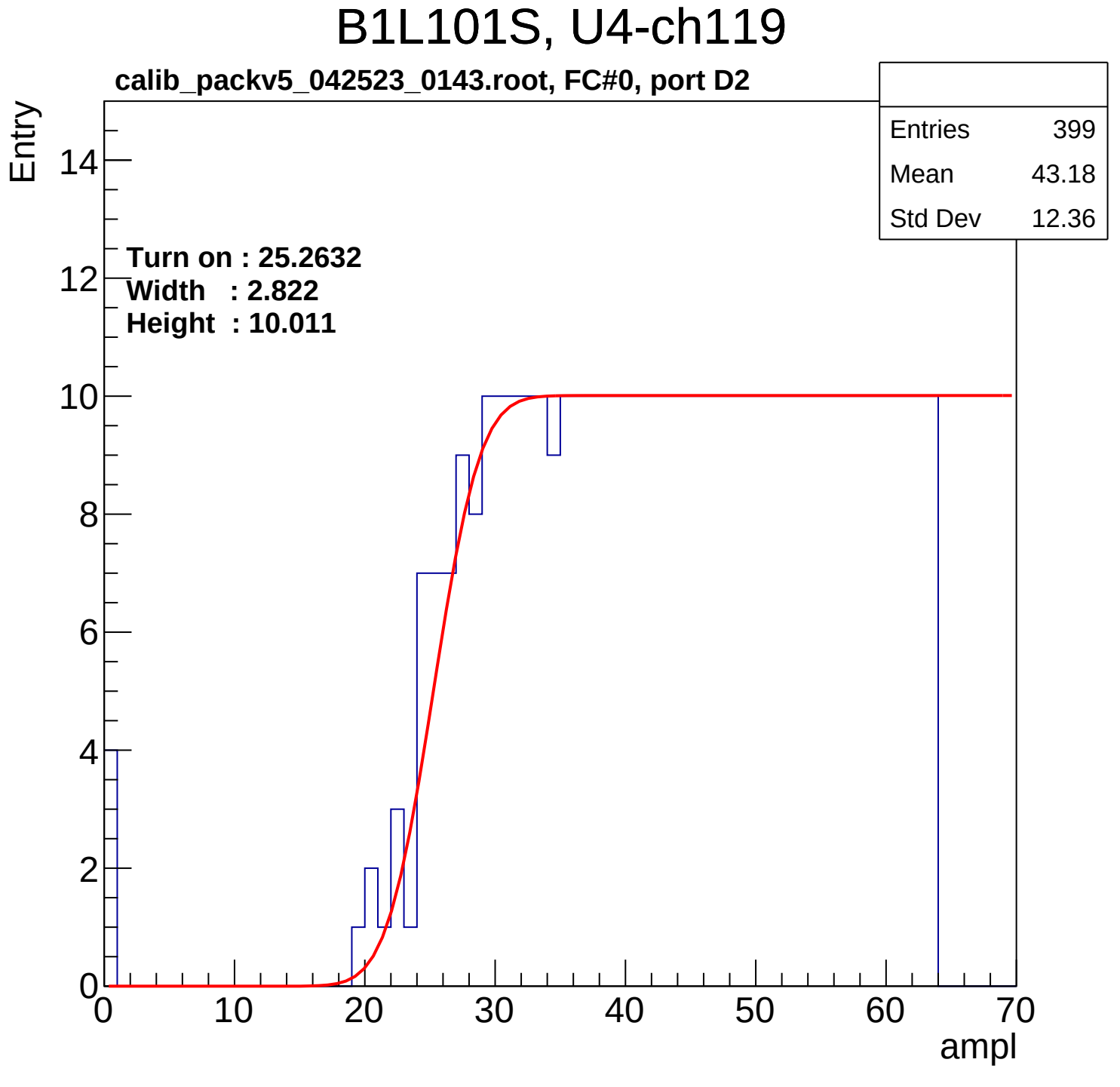

B1L101S, U4-ch114
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.19
Std Dev 11.95
Turn on : 26.5928
Width : 1.599
Height : 9.937
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

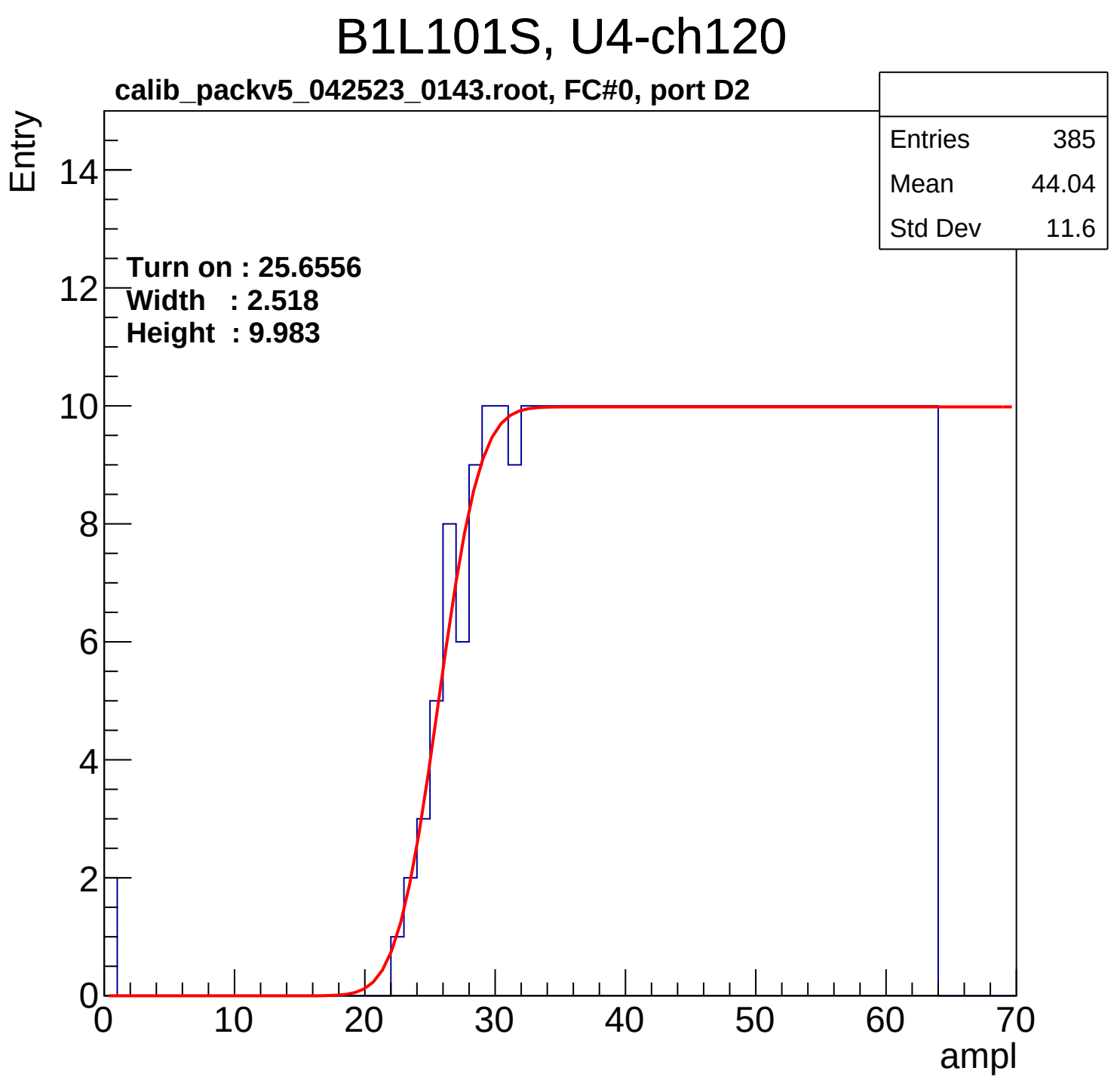

B1L101S, U4-ch115
calib_packv5_042523_0143.root, FC#0, port D2
Entries 402
Mean 43.25
Std Dev 11.91
Turn on : 24.4294
Width : 3.281
Height : 10.053
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

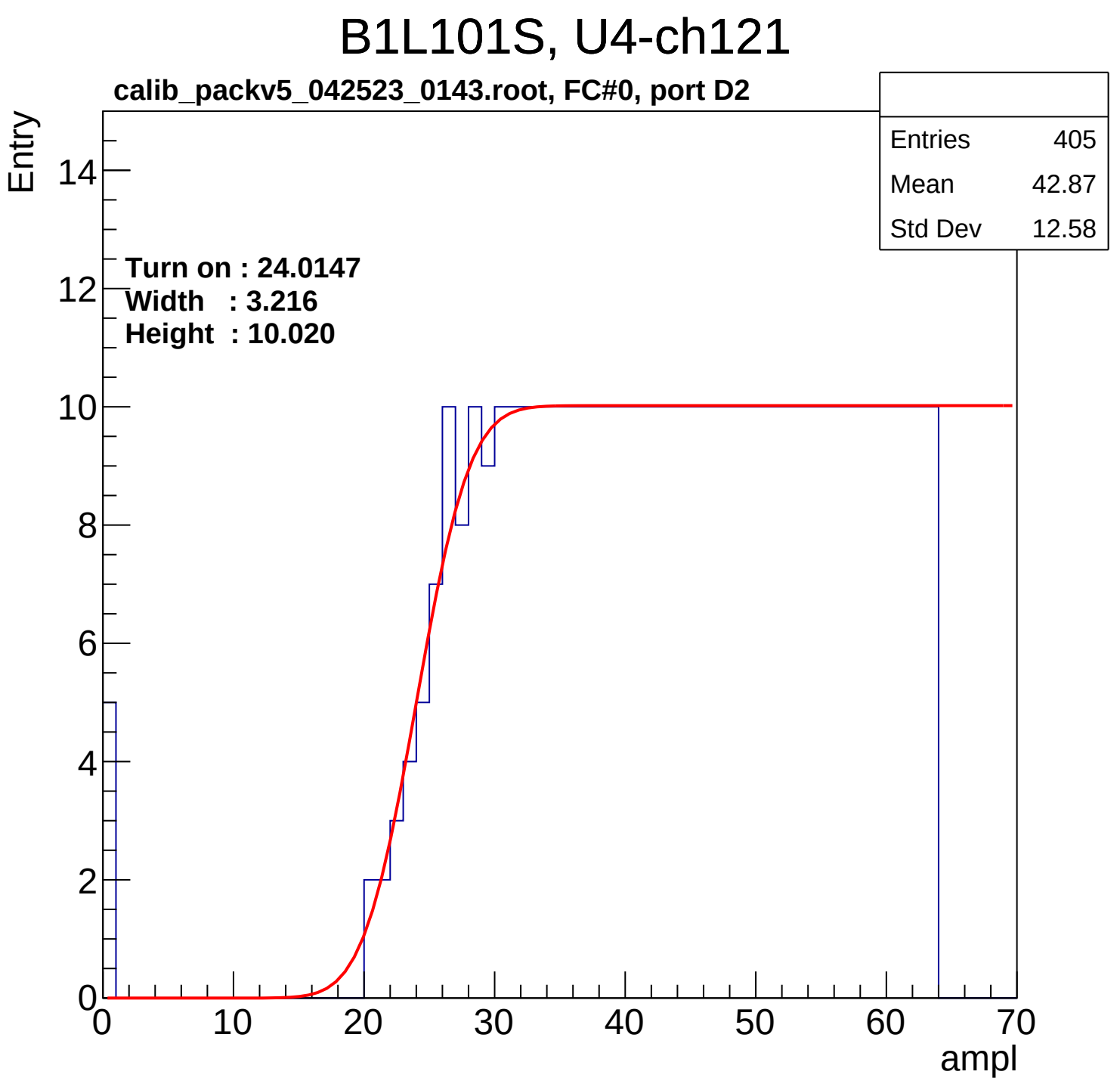

B1L101S, U4-ch116
calib_packv5_042523_0143.root, FC#0, port D2
Entries 380
Mean 44.17
Std Dev 11.73
Turn on : 26.5104
Width : 3.500
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

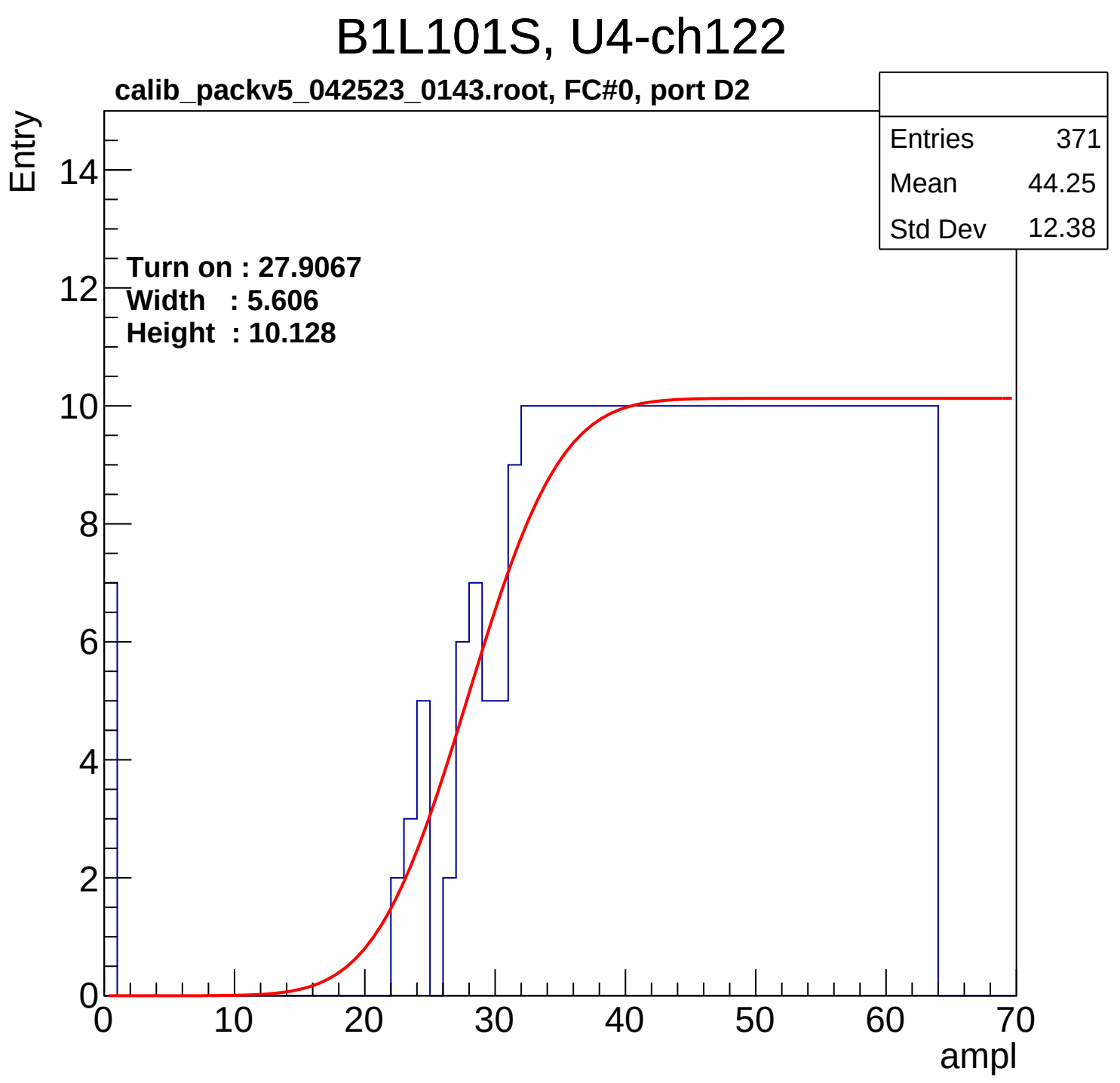

B1L101S, U4-ch117
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.78
Std Dev 11.27
Turn on : 27.6198
Width : 3.283
Height : 10.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

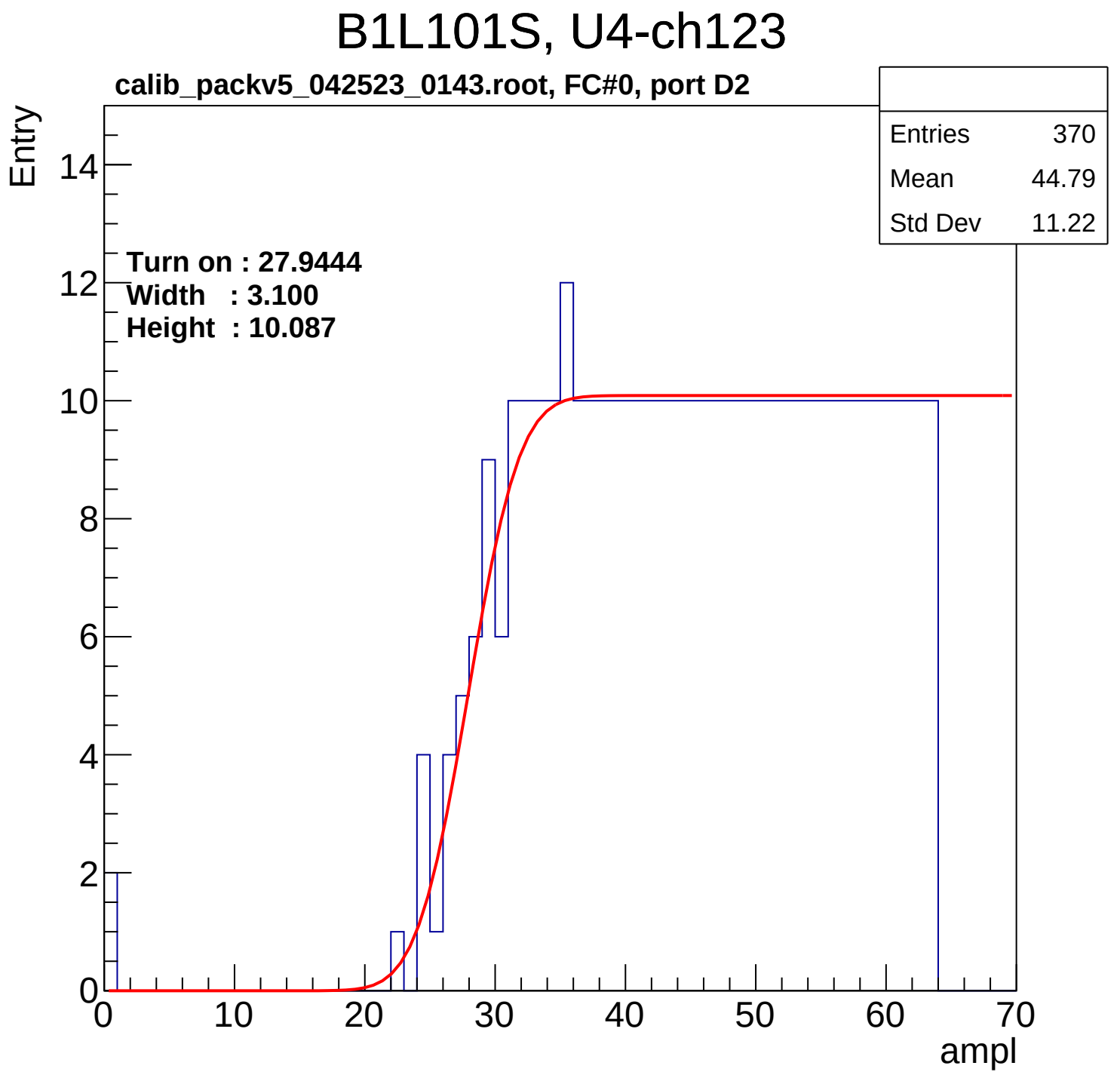

B1L101S, U4-ch118
calib_packv5_042523_0143.root, FC#0, port D2
Entries 393
Mean 43.65
Std Dev 11.81
Turn on : 25.1902
Width : 2.832
Height : 10.030
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

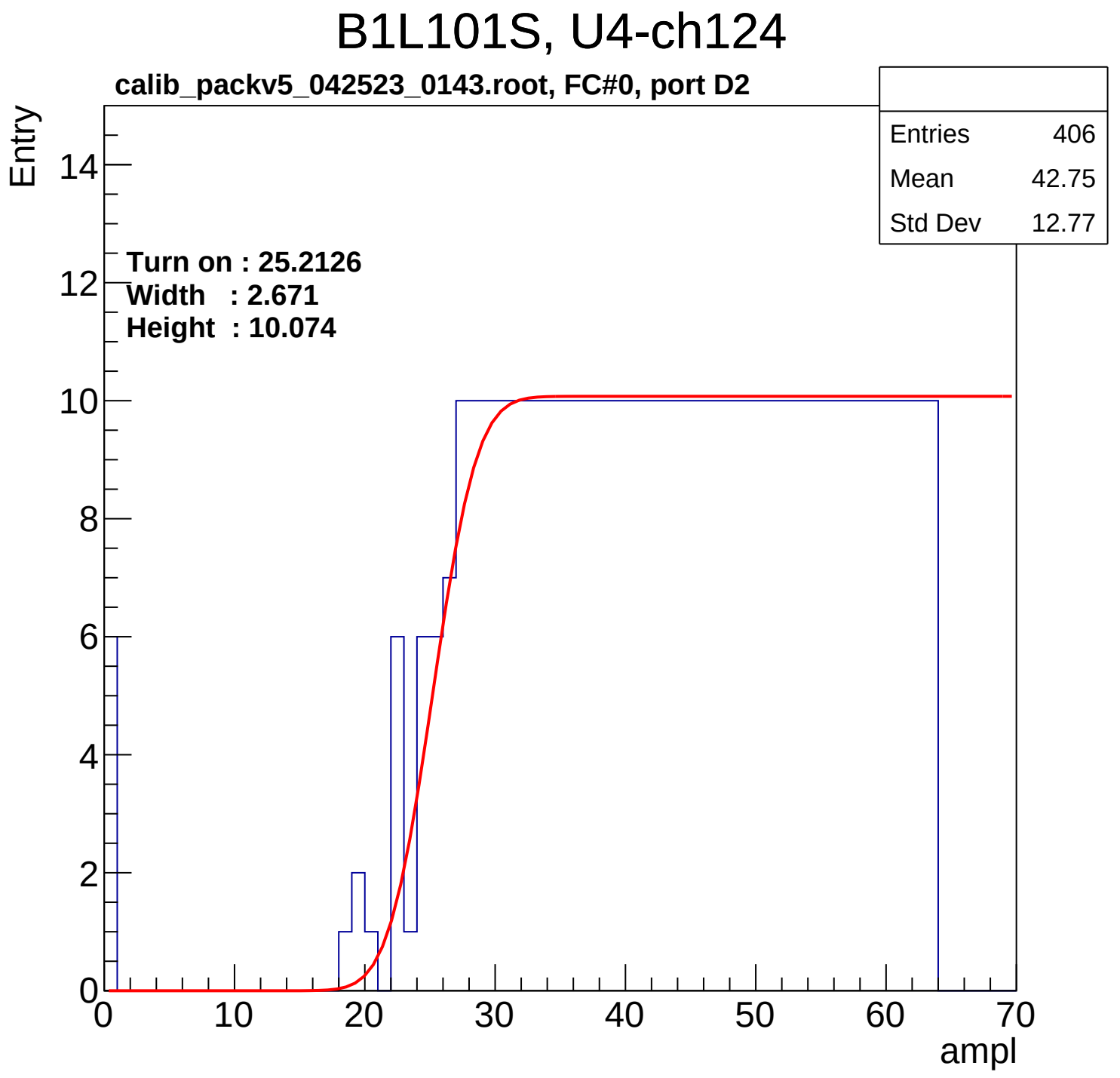

B1L101S, U4-ch119
calib_packv5_042523_0143.root, FC#0, port D2
Entries 399
Mean 43.18
Std Dev 12.36
Turn on : 25.2632
Width : 2.822
Height : 10.011
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

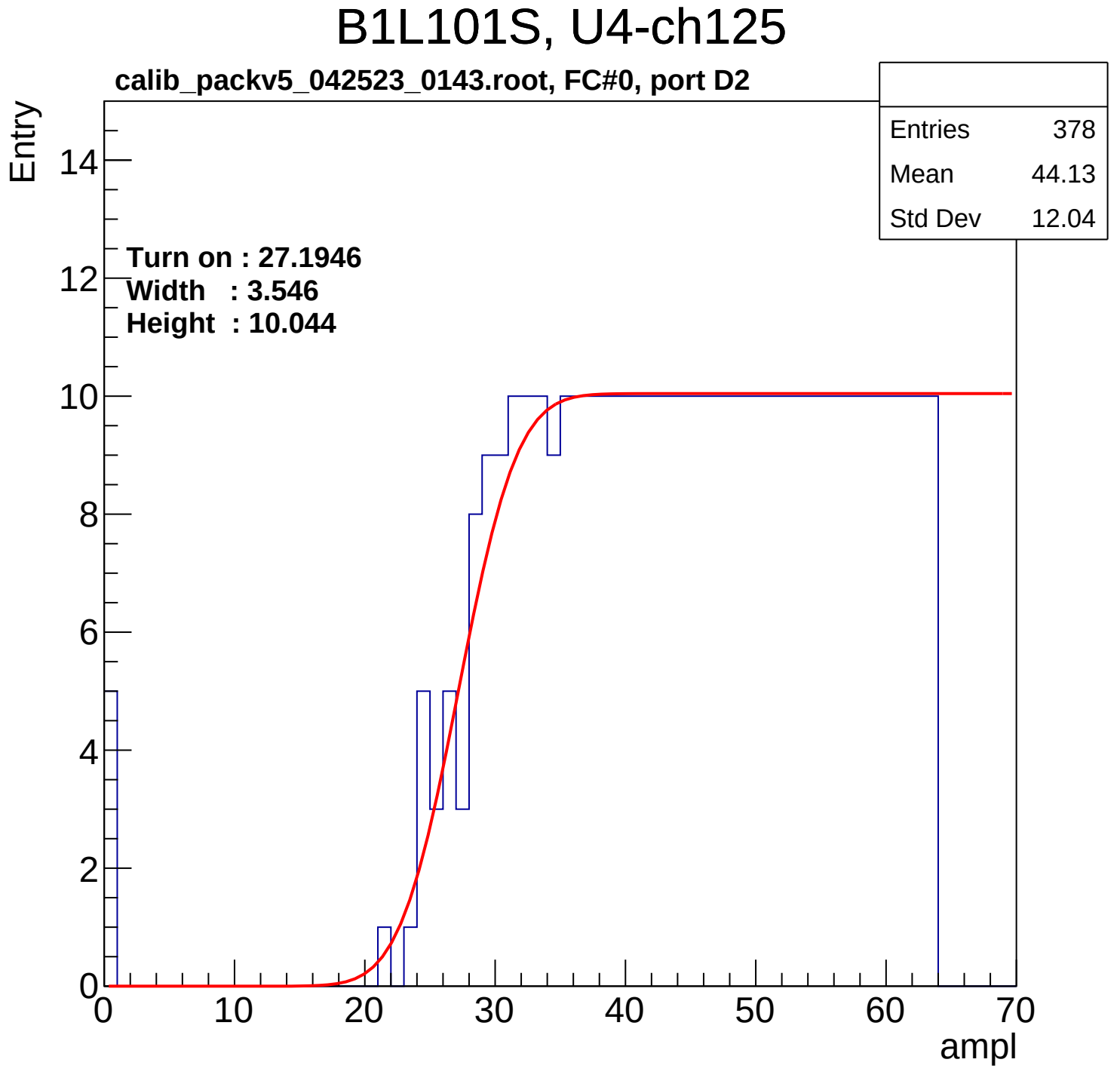

B1L101S, U4-ch120
calib_packv5_042523_0143.root, FC#0, port D2
Entries 385
Mean 44.04
Std Dev 11.6
Turn on : 25.6556
Width : 2.518
Height : 9.983
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

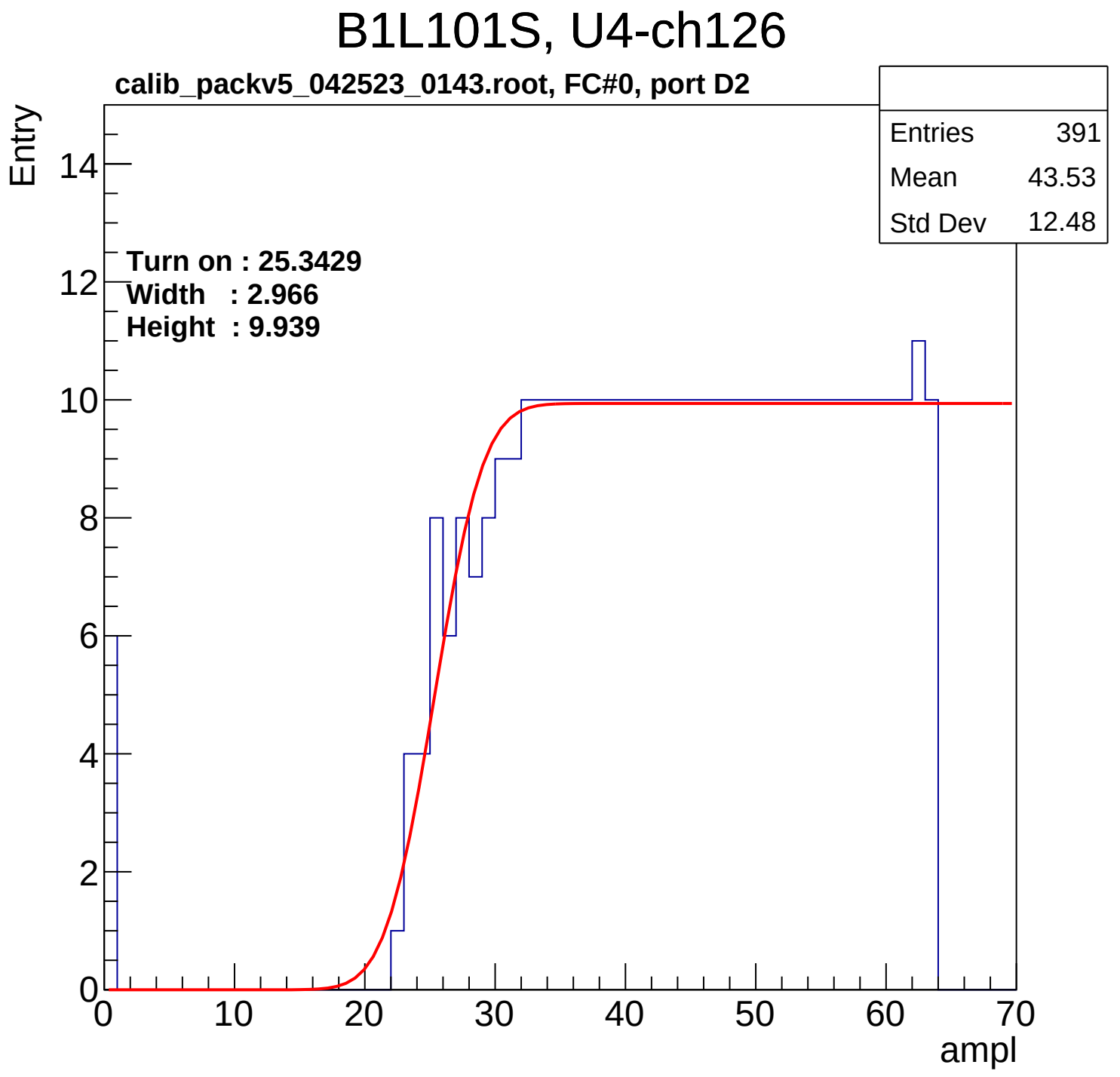

B1L101S, U4-ch121
calib_packv5_042523_0143.root, FC#0, port D2
Entries 405
Mean 42.87
Std Dev 12.58
Turn on : 24.0147
Width : 3.216
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

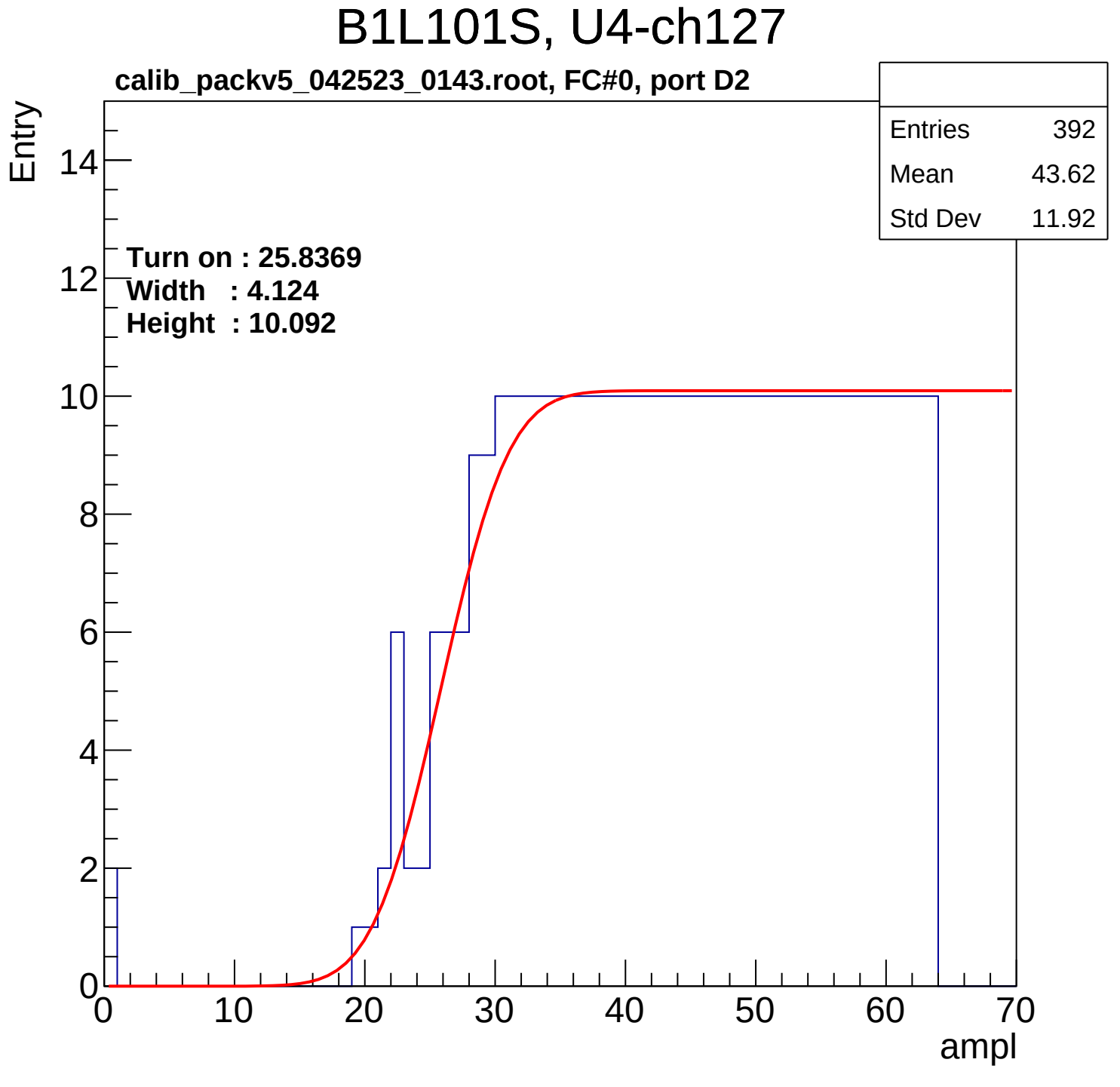

B1L101S, U4-ch122
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.25
Std Dev 12.38
Turn on : 27.9067
Width : 5.606
Height : 10.128
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

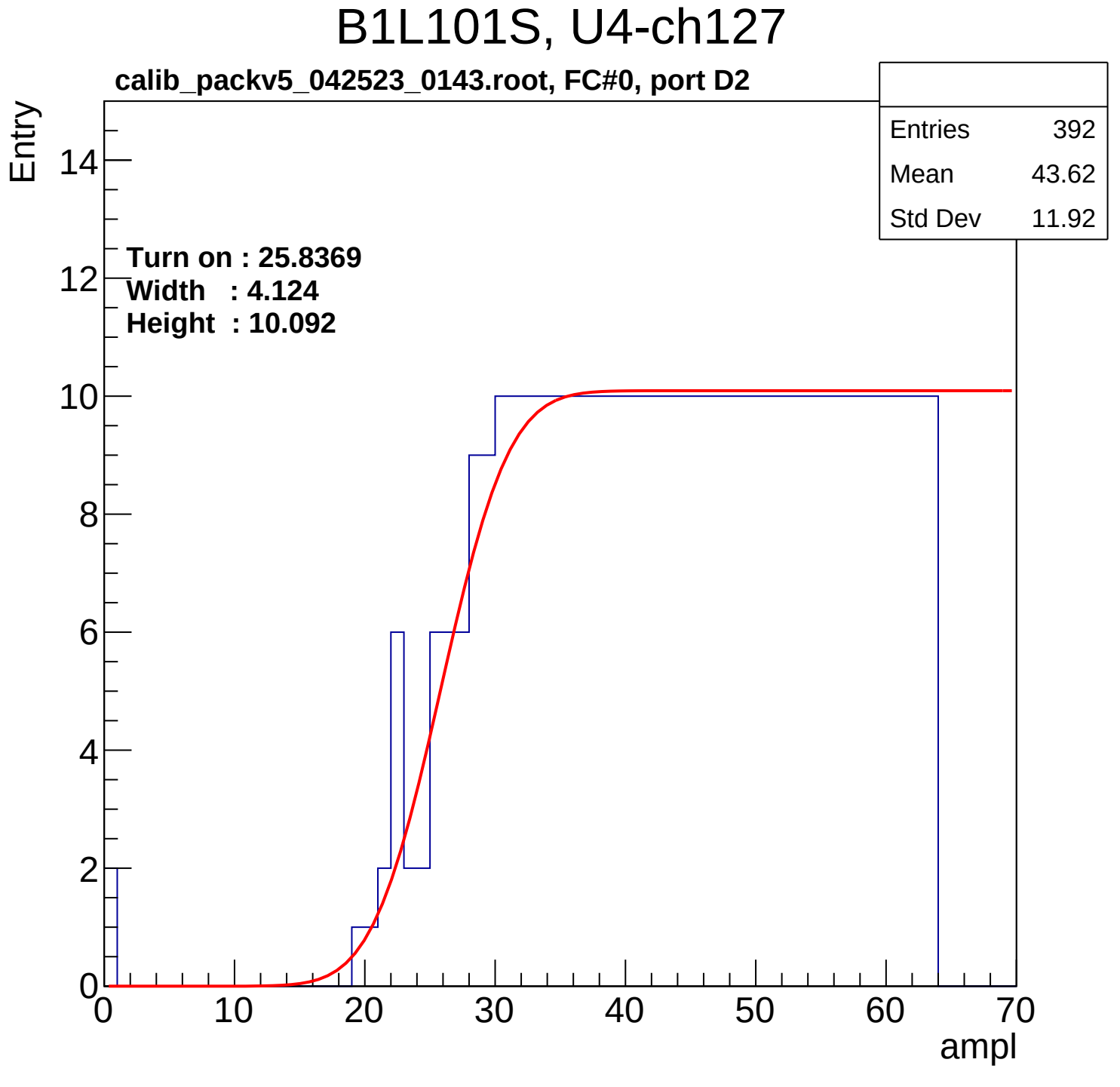

B1L101S, U4-ch123
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.79
Std Dev 11.22
Turn on : 27.9444
Width : 3.100
Height : 10.087
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U4-ch124
calib_packv5_042523_0143.root, FC#0, port D2
Entries 406
Mean 42.75
Std Dev 12.77
Turn on : 25.2126
Width : 2.671
Height : 10.074
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U4-ch125
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.13
Std Dev 12.04
Turn on : 27.1946
Width : 3.546
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U4-ch126
calib_packv5_042523_0143.root, FC#0, port D2
Entries 391
Mean 43.53
Std Dev 12.48
Turn on : 25.3429
Width : 2.966
Height : 9.939
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U4-ch127
calib_packv5_042523_0143.root, FC#0, port D2
Entries 392
Mean 43.62
Std Dev 11.92
Turn on : 25.8369
Width : 4.124
Height : 10.092
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U4-ch127
calib_packv5_042523_0143.root, FC#0, port D2
Entries 392
Mean 43.62
Std Dev 11.92
Turn on : 25.8369
Width : 4.124
Height : 10.092
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70