

B0L103S, U11-ch23

calib_packv5_040323_1717.root, FC#2, Port C3

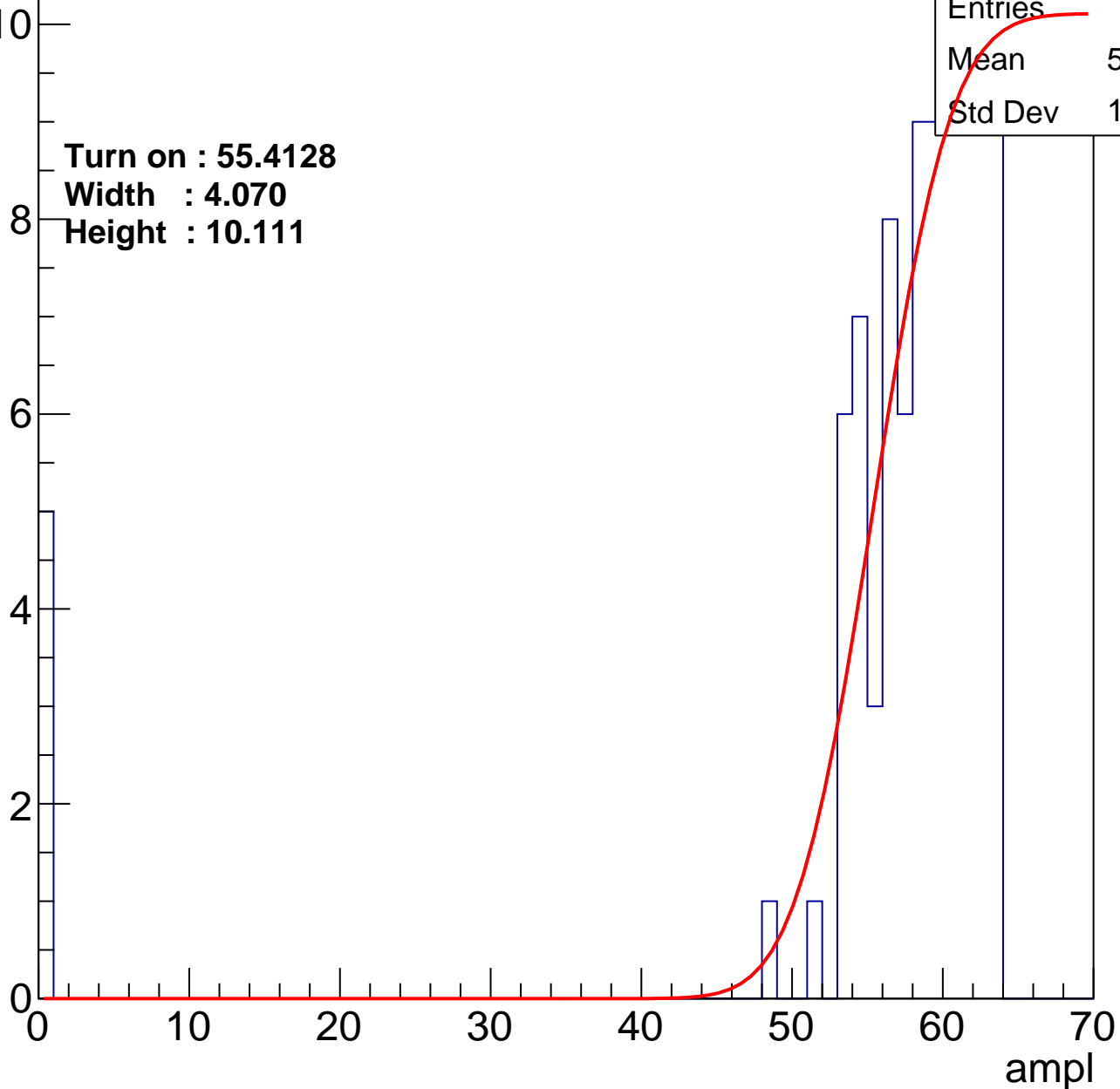
Entry

Entries	93
Mean	55.27
Std Dev	13.57

Turn on : 55.4128

Width : 4.070

Height : 10.111



B0L103S, U15-ch0

calib_packv5_040323_1717.root, FC#2, Port C3

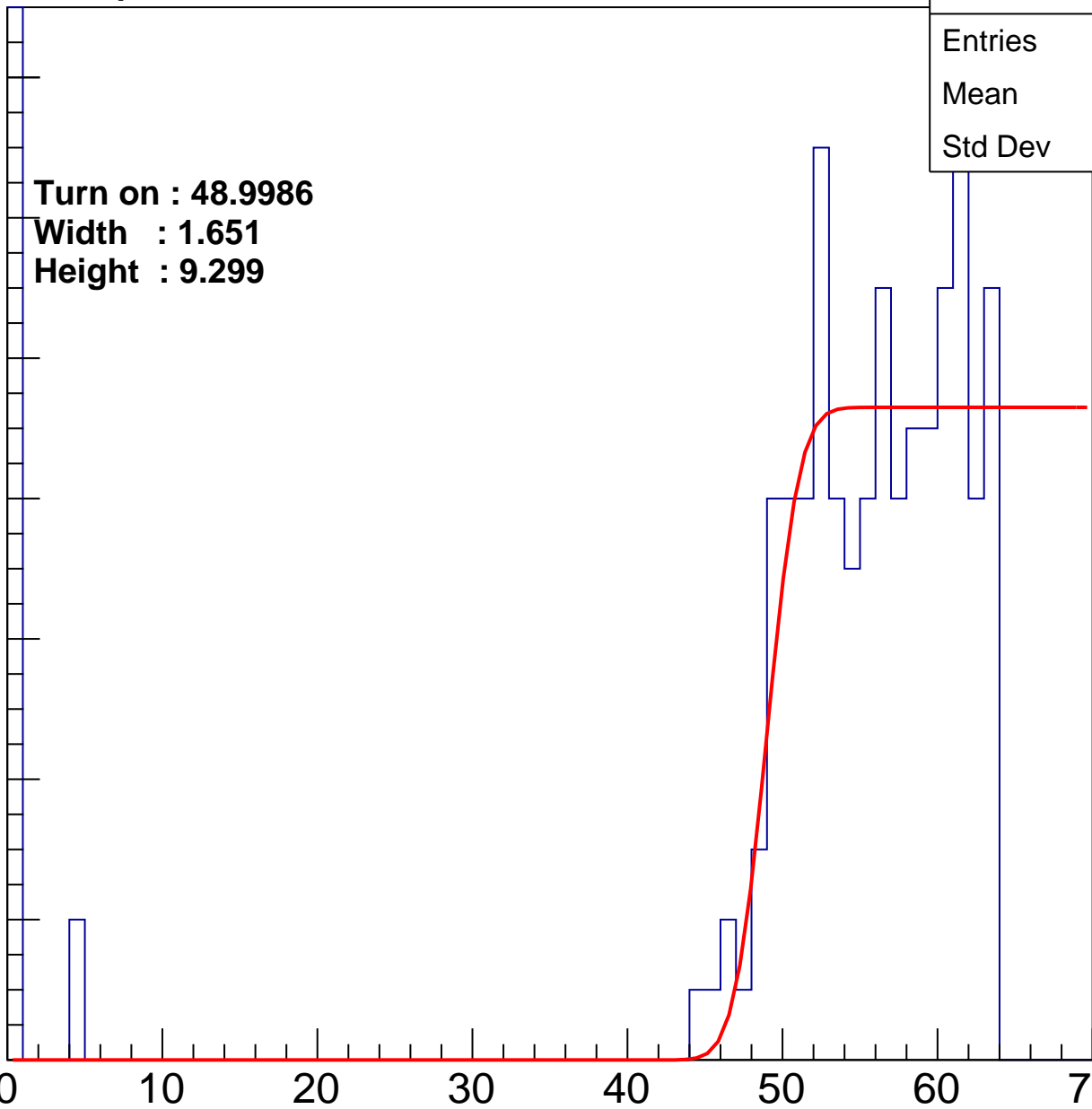
Entry

14
12
10
8
6
4
2
0

Turn on : 48.9986
Width : 1.651
Height : 9.299

Entries	245
Mean	33.73
Std Dev	27.5

ampl



B0L103S, U15-ch1

calib_packv5_040323_1717.root, FC#2, Port C3

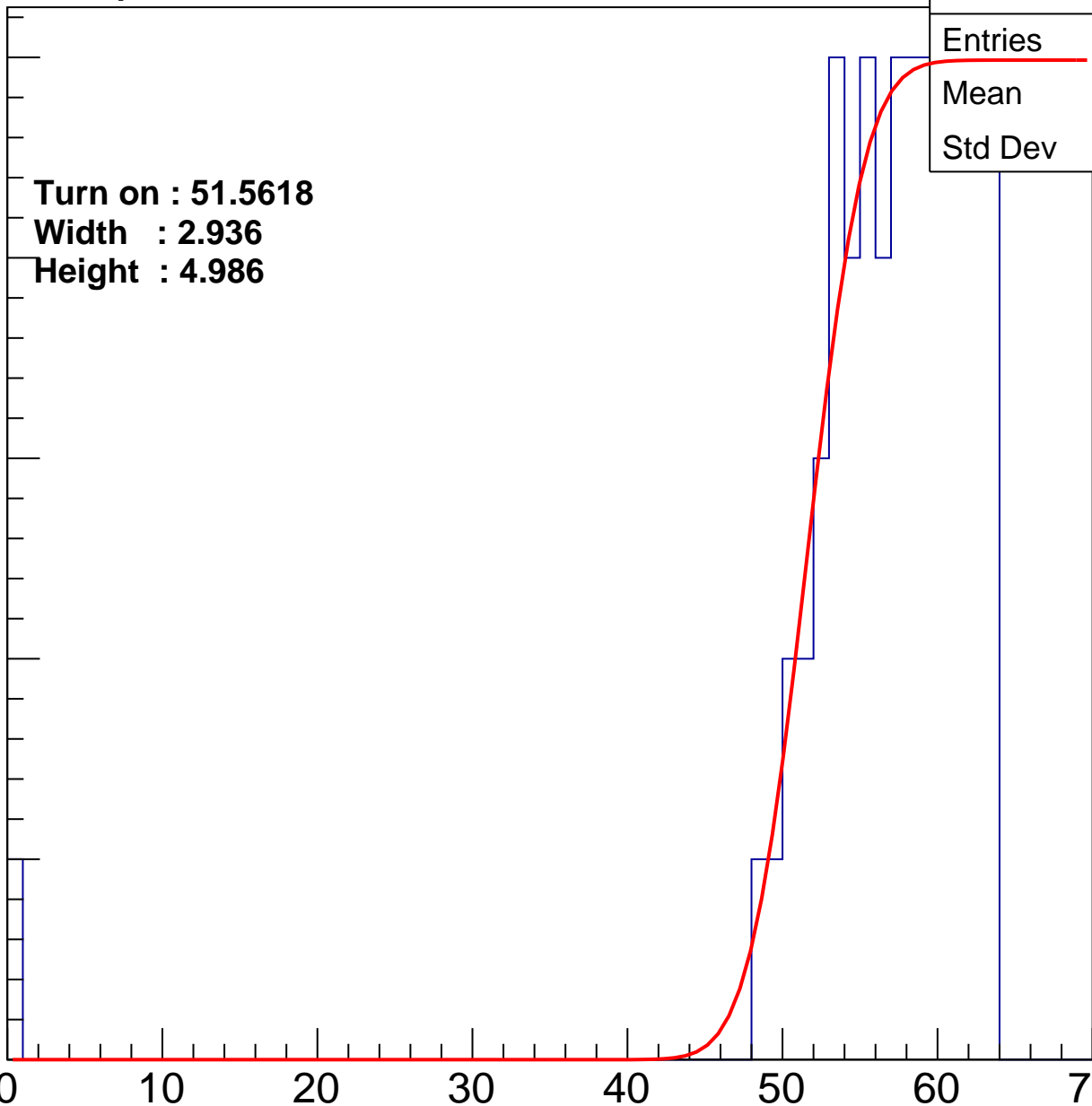
Entry

5
4
3
2
1
0

Turn on : 51.5618
Width : 2.936
Height : 4.986

Entries	63
Mean	56.11
Std Dev	8.15

ampl



B0L103S, U15-ch2

calib_packv5_040323_1717.root, FC#2, Port C3

Entry

5

4

3

2

1

0

Turn on : 49.8522

Width : 3.526

Height : 5.147

Entries	76
Mean	54.39
Std Dev	10.06

ampl

0

10

20

30

40

50

60

70

B0L103S, U15-ch3

calib_packv5_040323_1717.root, FC#2, Port C3

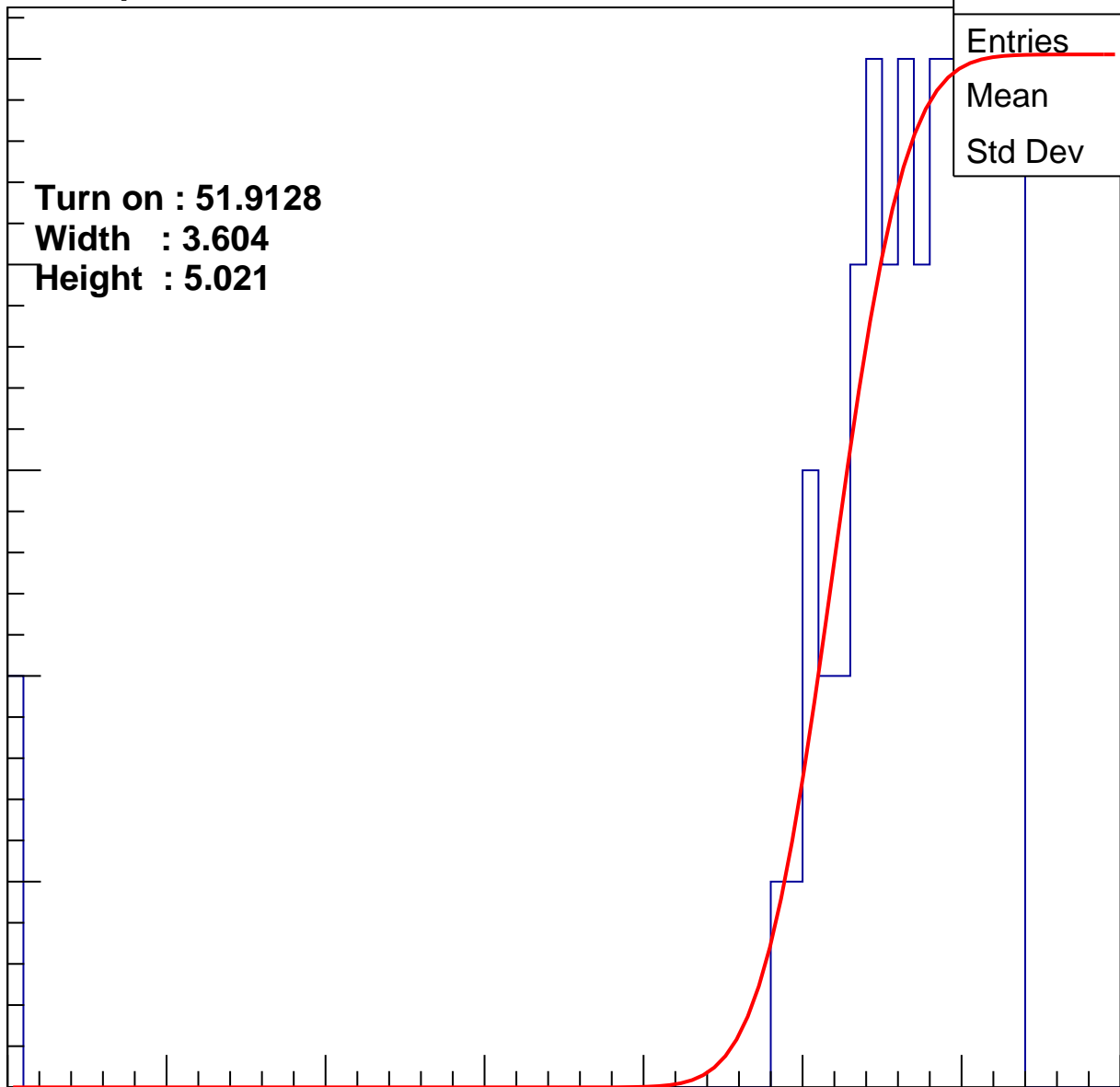
Entry

5
4
3
2
1
0

Turn on : 51.9128
Width : 3.604
Height : 5.021

Entries	63
Mean	55.21
Std Dev	10.76

ampl



B0L103S, U15-ch4

calib_packv5_040323_1717.root, FC#2, Port C3

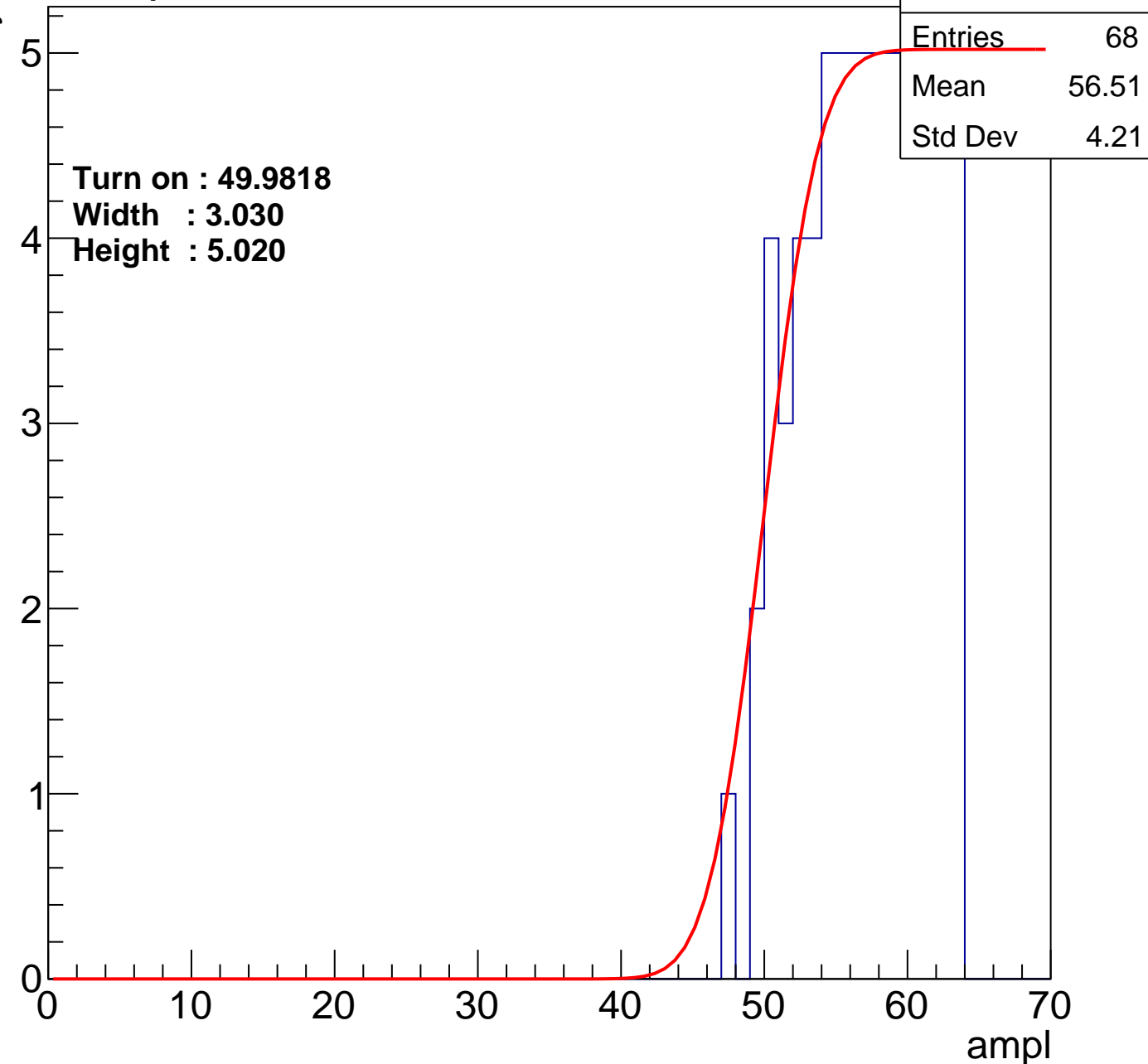
Entry

5
4
3
2
1
0

Turn on : 49.9818
Width : 3.030
Height : 5.020

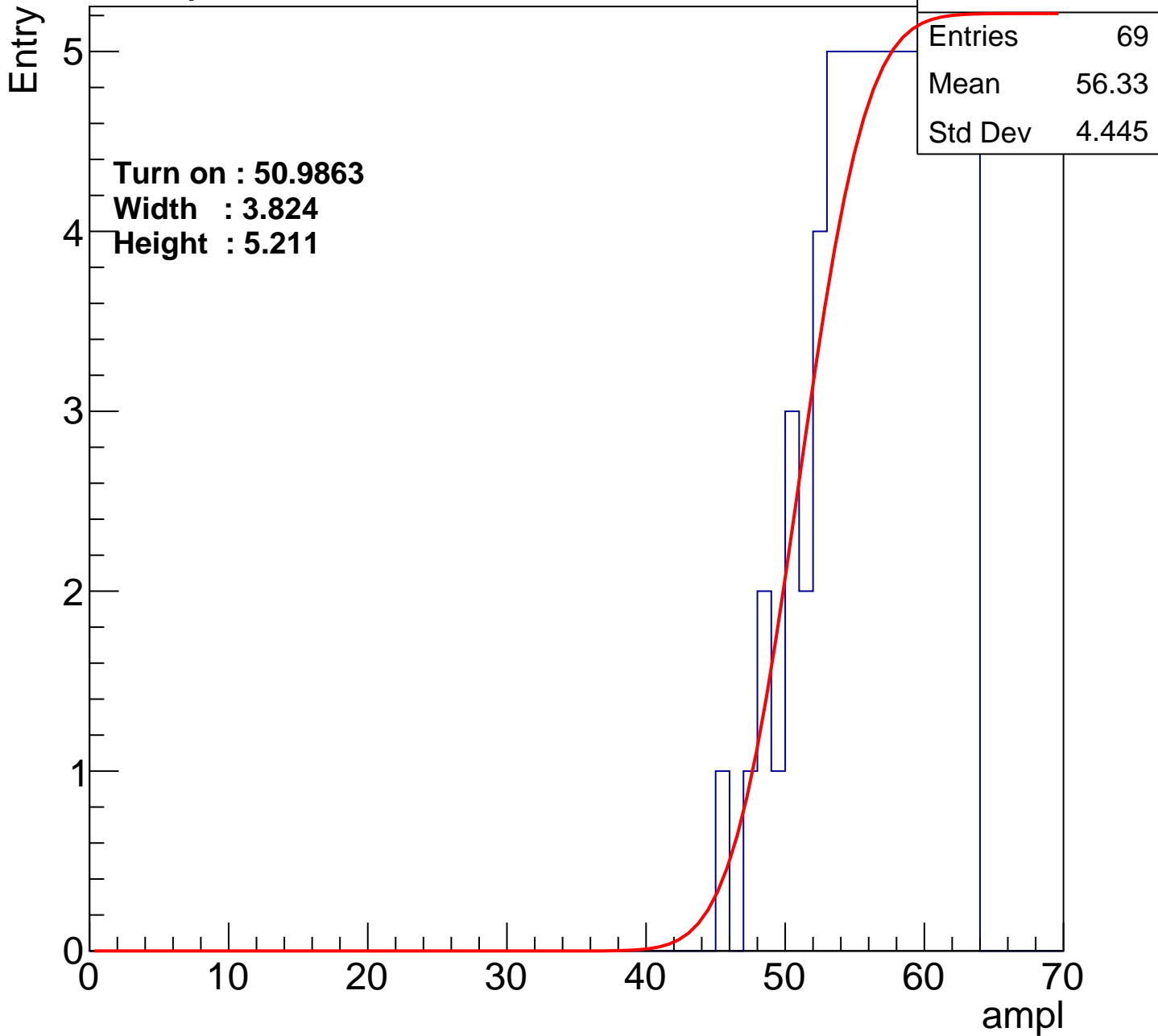
Entries	68
Mean	56.51
Std Dev	4.21

ampl



B0L103S, U15-ch5

calib_packv5_040323_1717.root, FC#2, Port C3



B0L103S, U15-ch6

calib_packv5_040323_1717.root, FC#2, Port C3

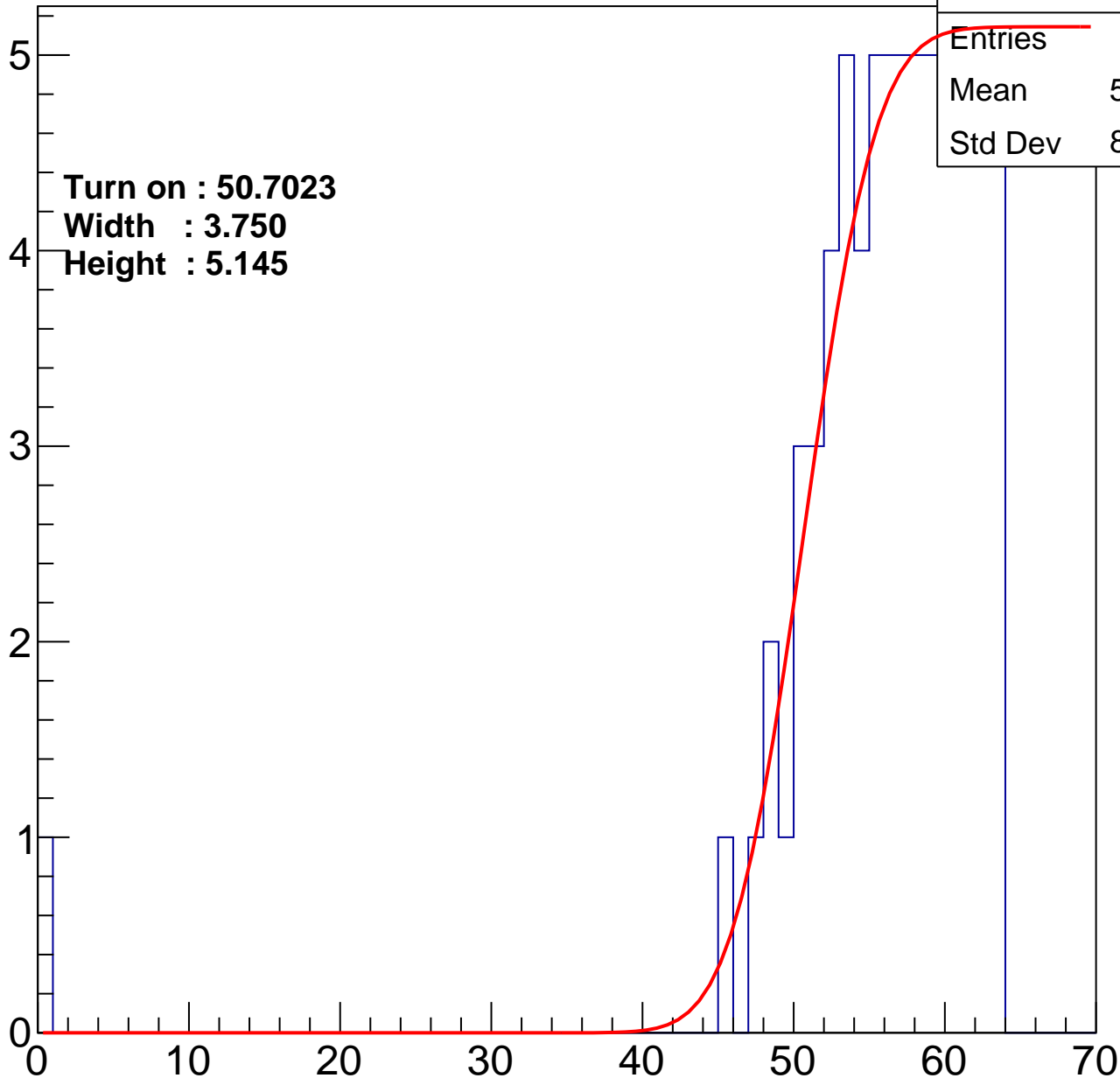
Entry

5
4
3
2
1
0

Turn on : 50.7023
Width : 3.750
Height : 5.145

Entries	70
Mean	55.49
Std Dev	8.026

ampl



B0L103S, U15-ch7

calib_packv5_040323_1717.root, FC#2, Port C3

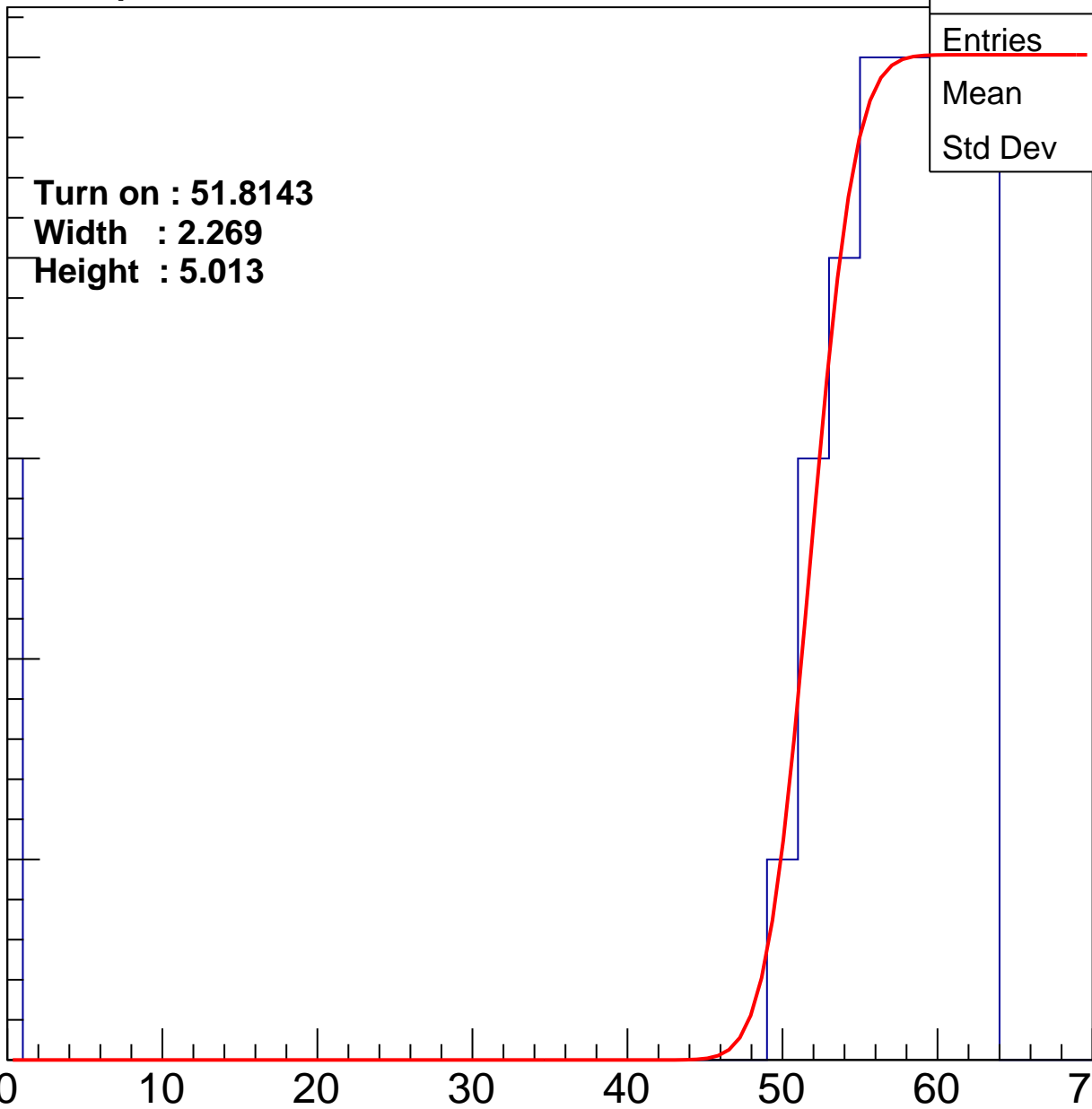
Entry

5
4
3
2
1
0

Turn on : 51.8143
Width : 2.269
Height : 5.013

Entries	64
Mean	54.55
Std Dev	12.65

ampl



B0L103S, U15-ch8

calib_packv5_040323_1717.root, FC#2, Port C3

Entry

5

4

3

2

1

0

Turn on : 51.1852

Width : 2.709

Height : 5.104

Entries 66

Mean 55.98

Std Dev 8.007

5

4

3

2

1

0

5

4

3

2

1

0

5

4

3

2

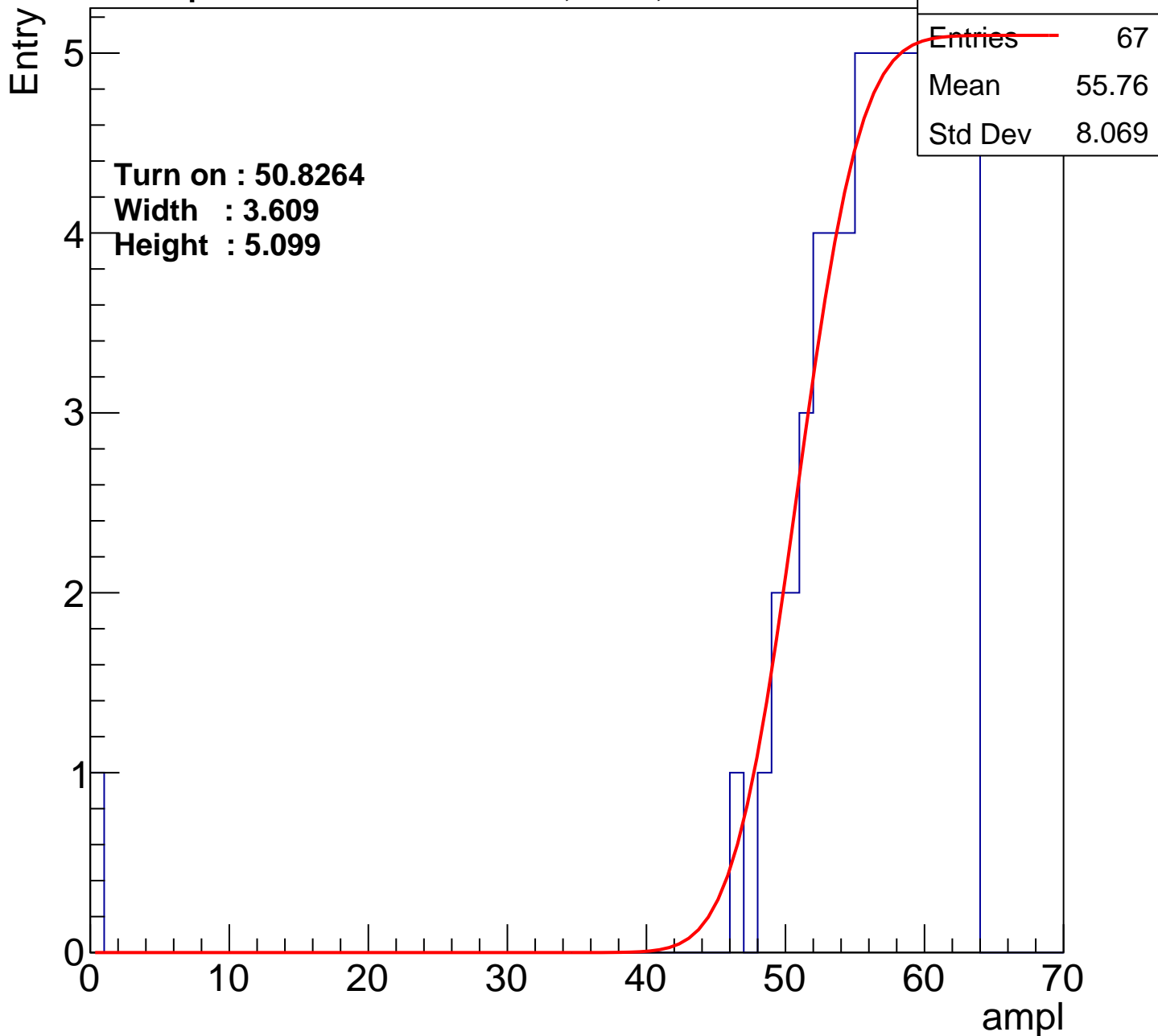
1

0

ampl

B0L103S, U15-ch9

calib_packv5_040323_1717.root, FC#2, Port C3



B0L103S, U15-ch10

calib_packv5_040323_1717.root, FC#2, Port C3

Entry

5

4

3

2

1

0

Turn on : 50.7299

Width : 3.978

Height : 5.190

Entries	68
Mean	55.72
Std Dev	8.04

ampl

0

10

20

30

40

50

60

70

B0L103S, U15-ch11

calib_packv5_040323_1717.root, FC#2, Port C3

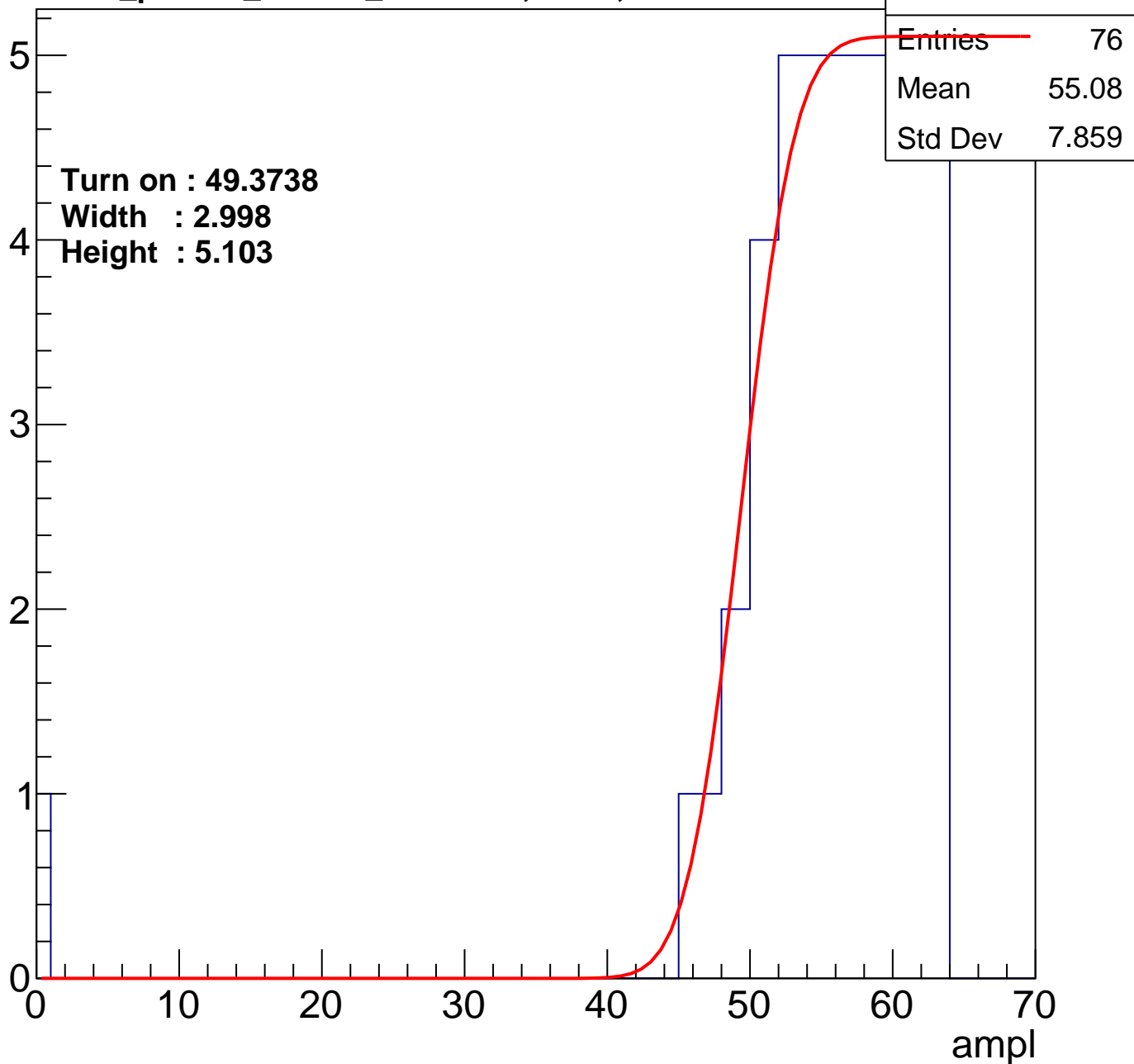
Entry

5
4
3
2
1
0

Turn on : 49.3738
Width : 2.998
Height : 5.103

Entries	76
Mean	55.08
Std Dev	7.859

ampl



B0L103S, U15-ch12

calib_packv5_040323_1717.root, FC#2, Port C3

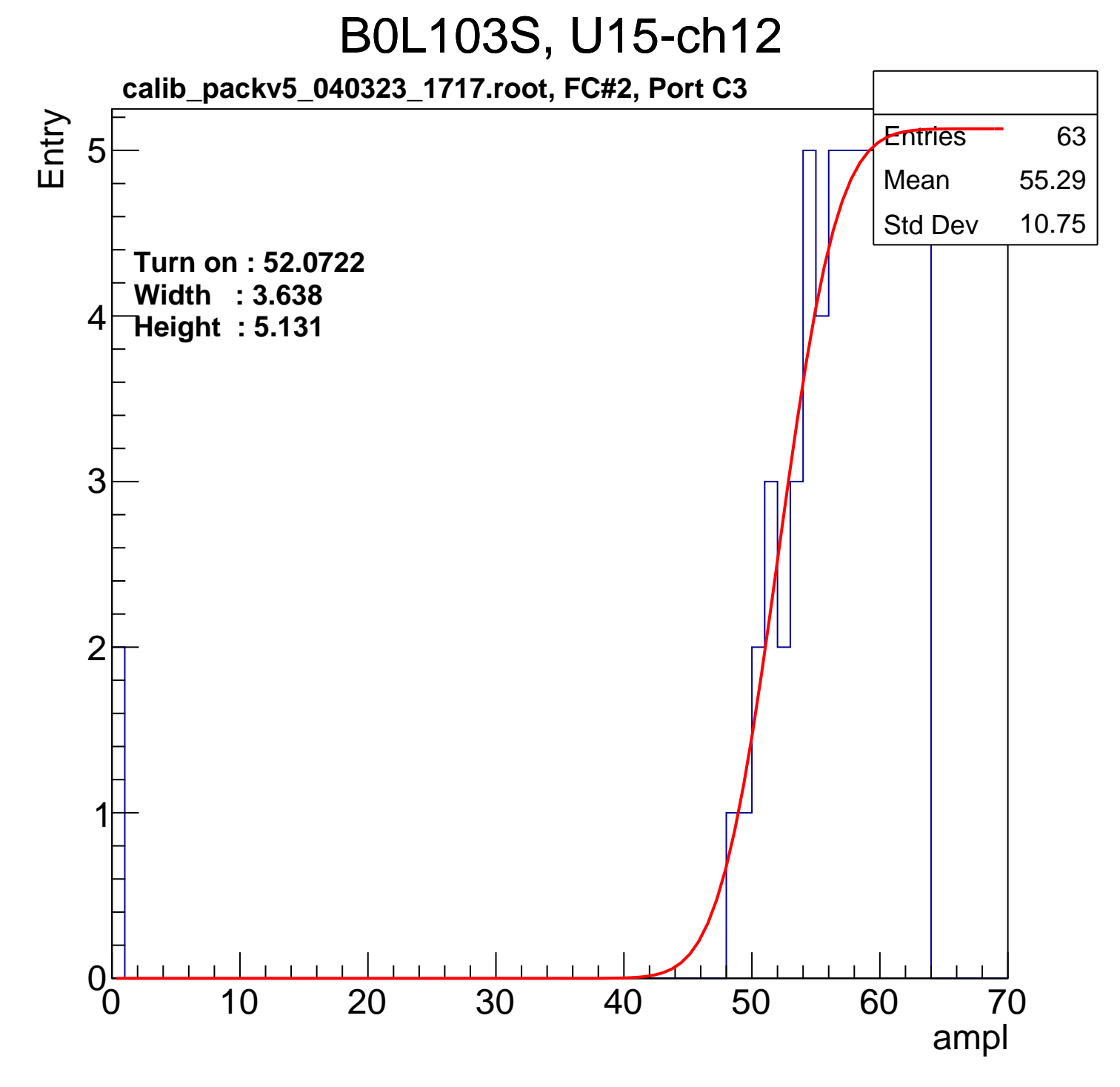
Entry

5
4
3
2
1
0

Turn on : 52.0722
Width : 3.638
Height : 5.131

Entries	63
Mean	55.29
Std Dev	10.75

ampl



B0L103S, U15-ch13

calib_packv5_040323_1717.root, FC#2, Port C3

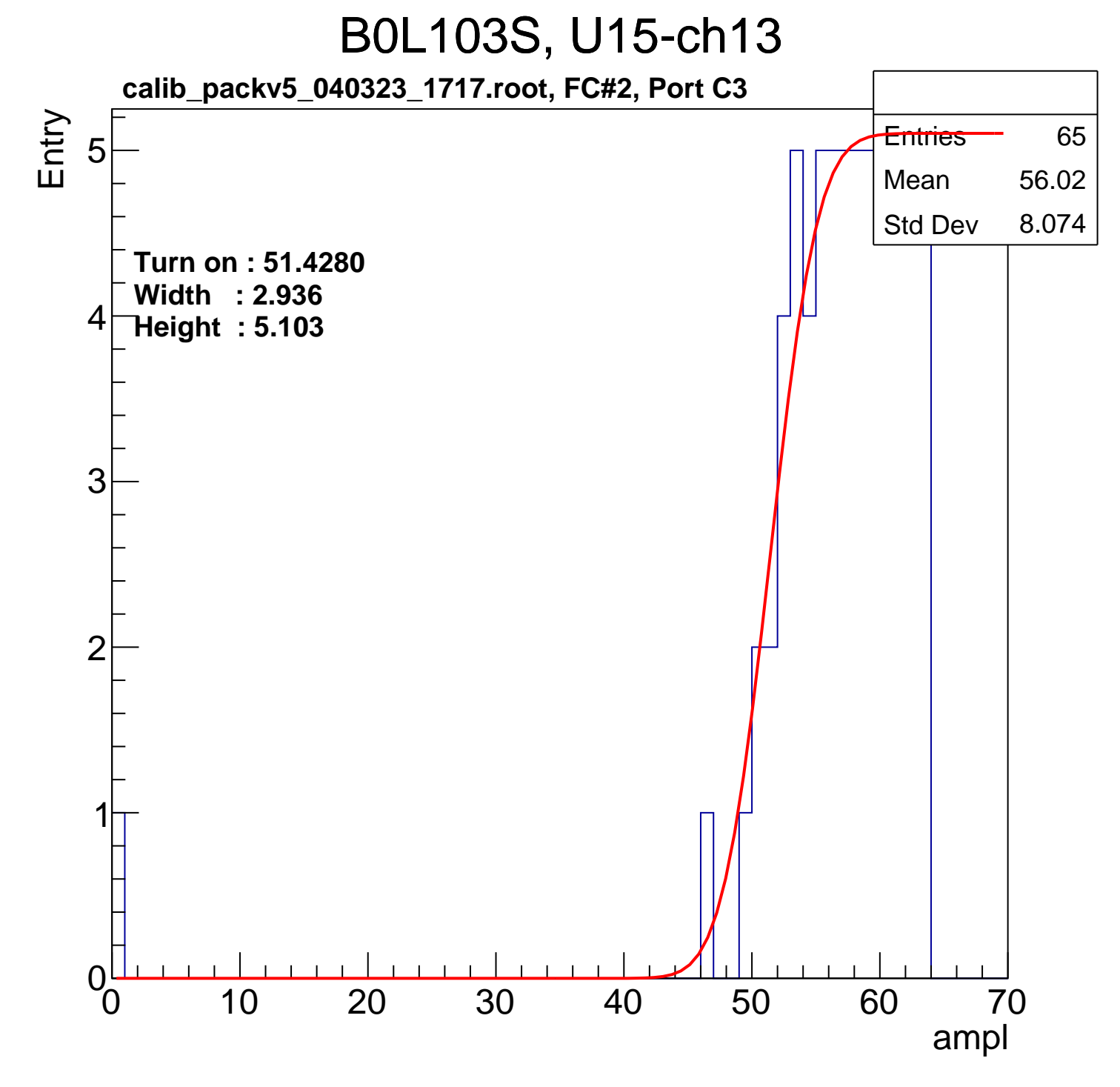
Entry

5
4
3
2
1
0

Turn on : 51.4280
Width : 2.936
Height : 5.103

Entries	65
Mean	56.02
Std Dev	8.074

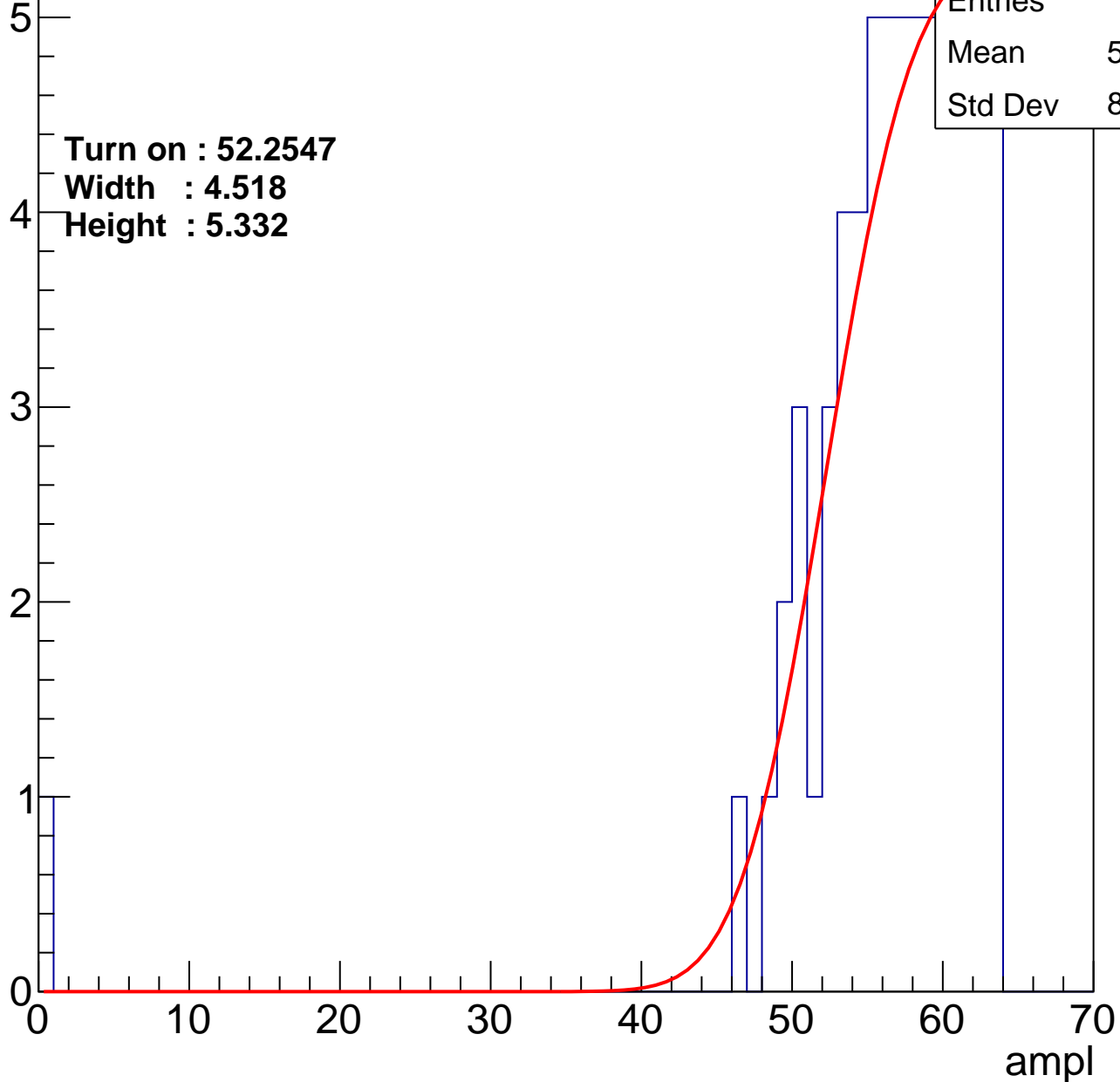
ampl



B0L103S, U15-ch14

calib_packv5_040323_1717.root, FC#2, Port C3

Entry



B0L103S, U15-ch15

calib_packv5_040323_1717.root, FC#2, Port C3

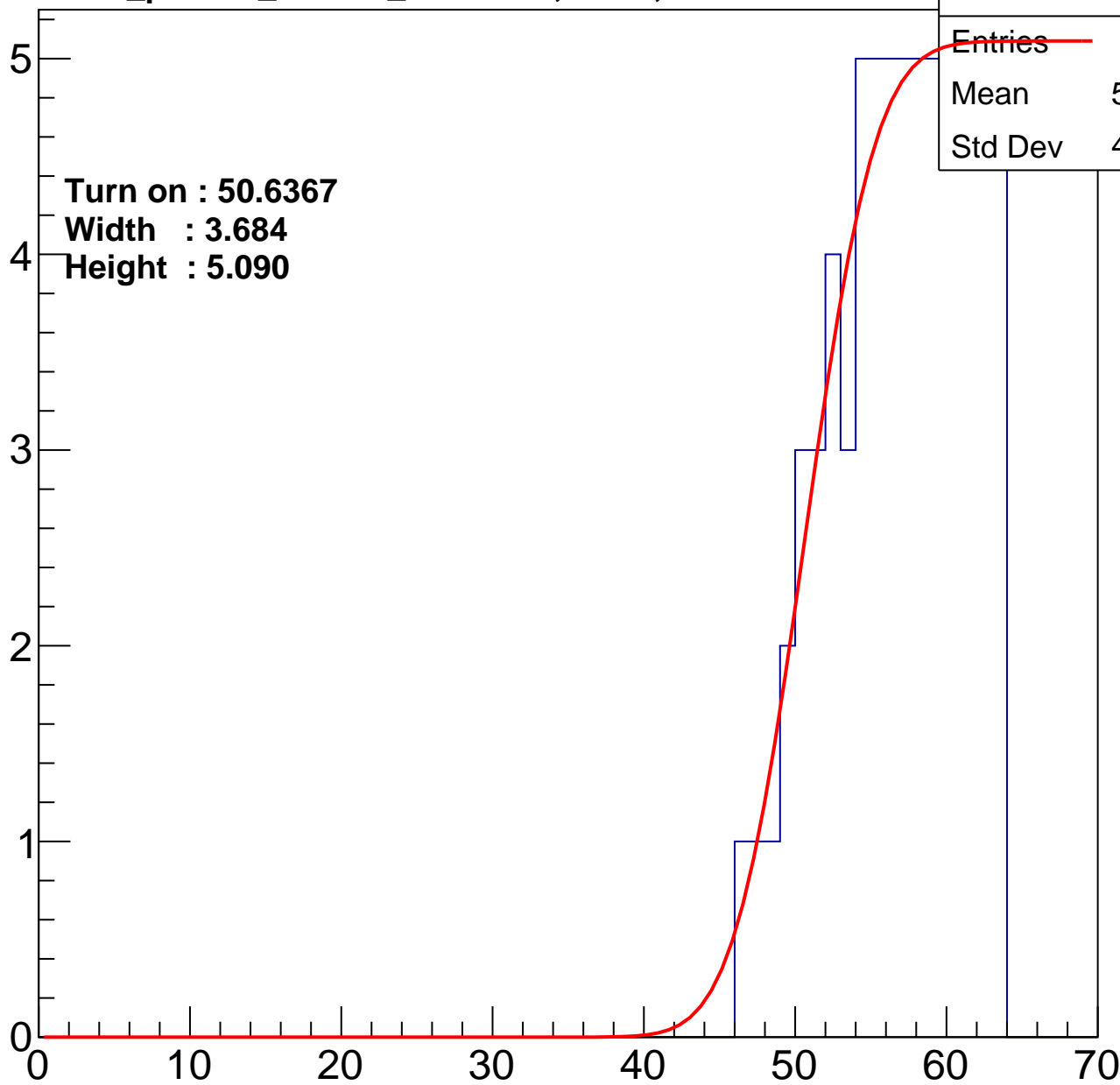
Entry

5
4
3
2
1
0

Turn on : 50.6367
Width : 3.684
Height : 5.090

Entries	68
Mean	56.38
Std Dev	4.426

ampl



B0L103S, U15-ch16

calib_packv5_040323_1717.root, FC#2, Port C3

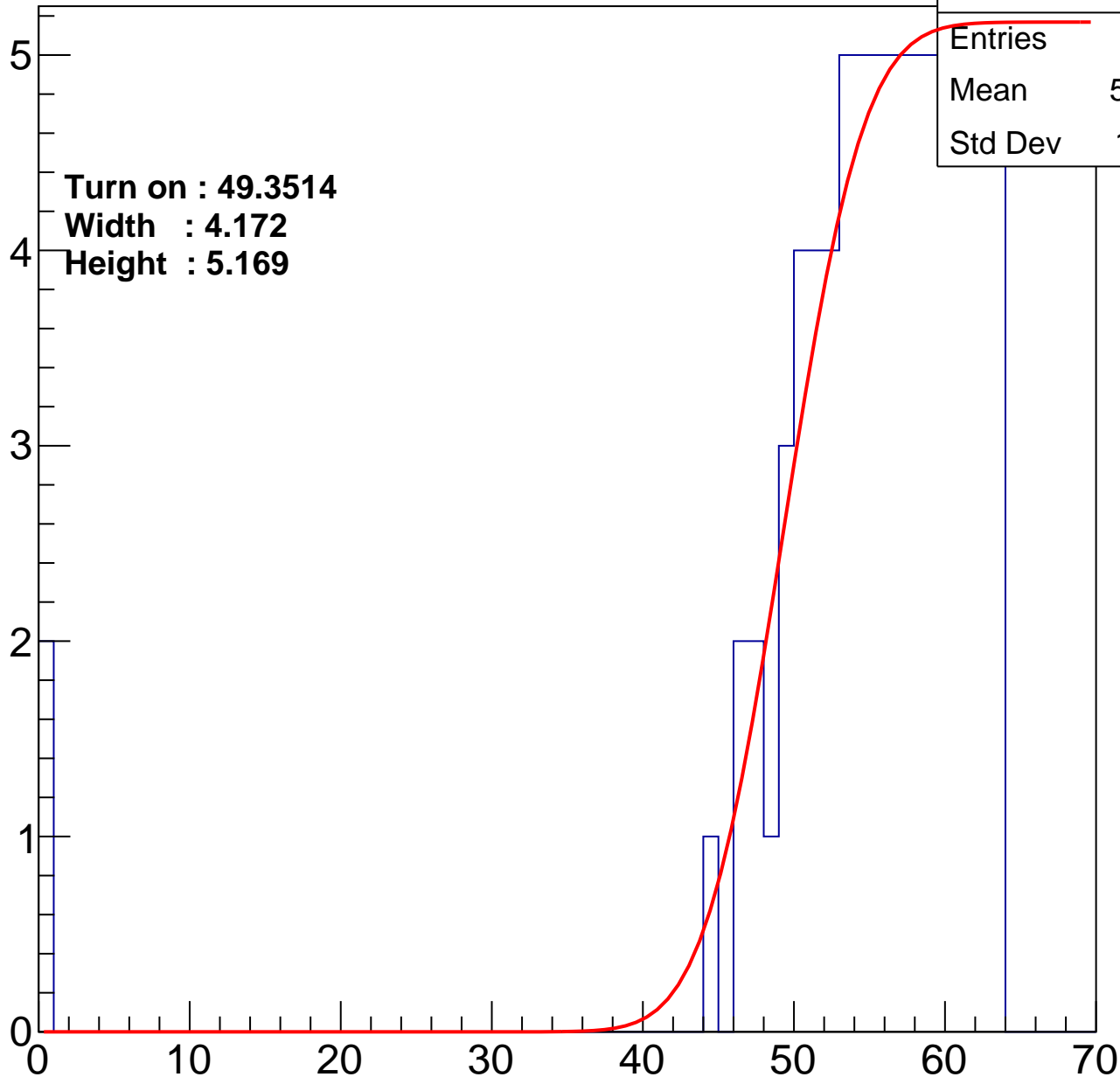
Entry

5
4
3
2
1
0

Turn on : 49.3514
Width : 4.172
Height : 5.169

Entries	78
Mean	54.19
Std Dev	10.01

ampl



B0L103S, U15-ch17

calib_packv5_040323_1717.root, FC#2, Port C3

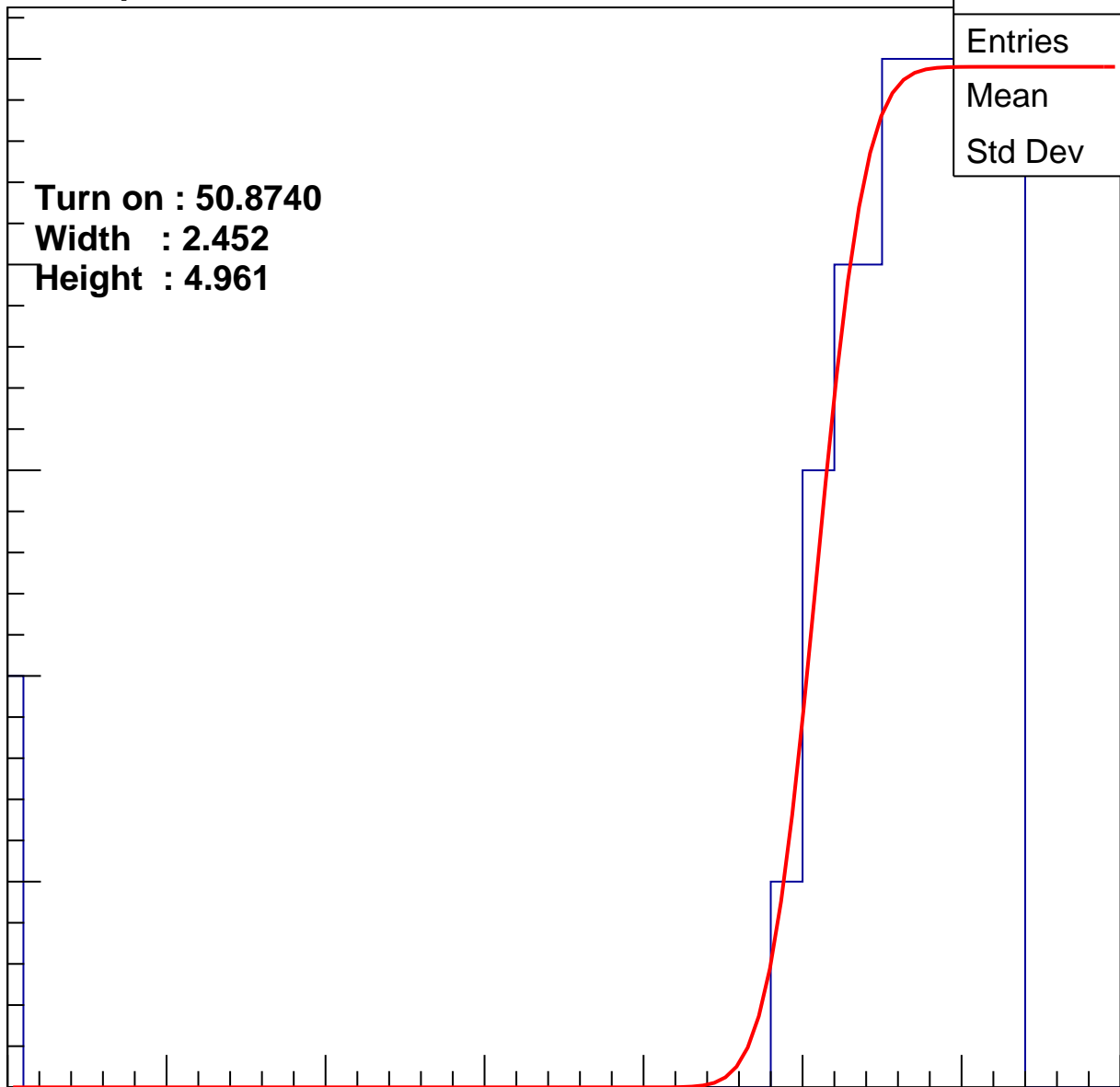
Entry

5
4
3
2
1
0

Turn on : 50.8740
Width : 2.452
Height : 4.961

Entries	67
Mean	55.09
Std Dev	10.46

ampl



B0L103S, U15-ch18

calib_packv5_040323_1717.root, FC#2, Port C3

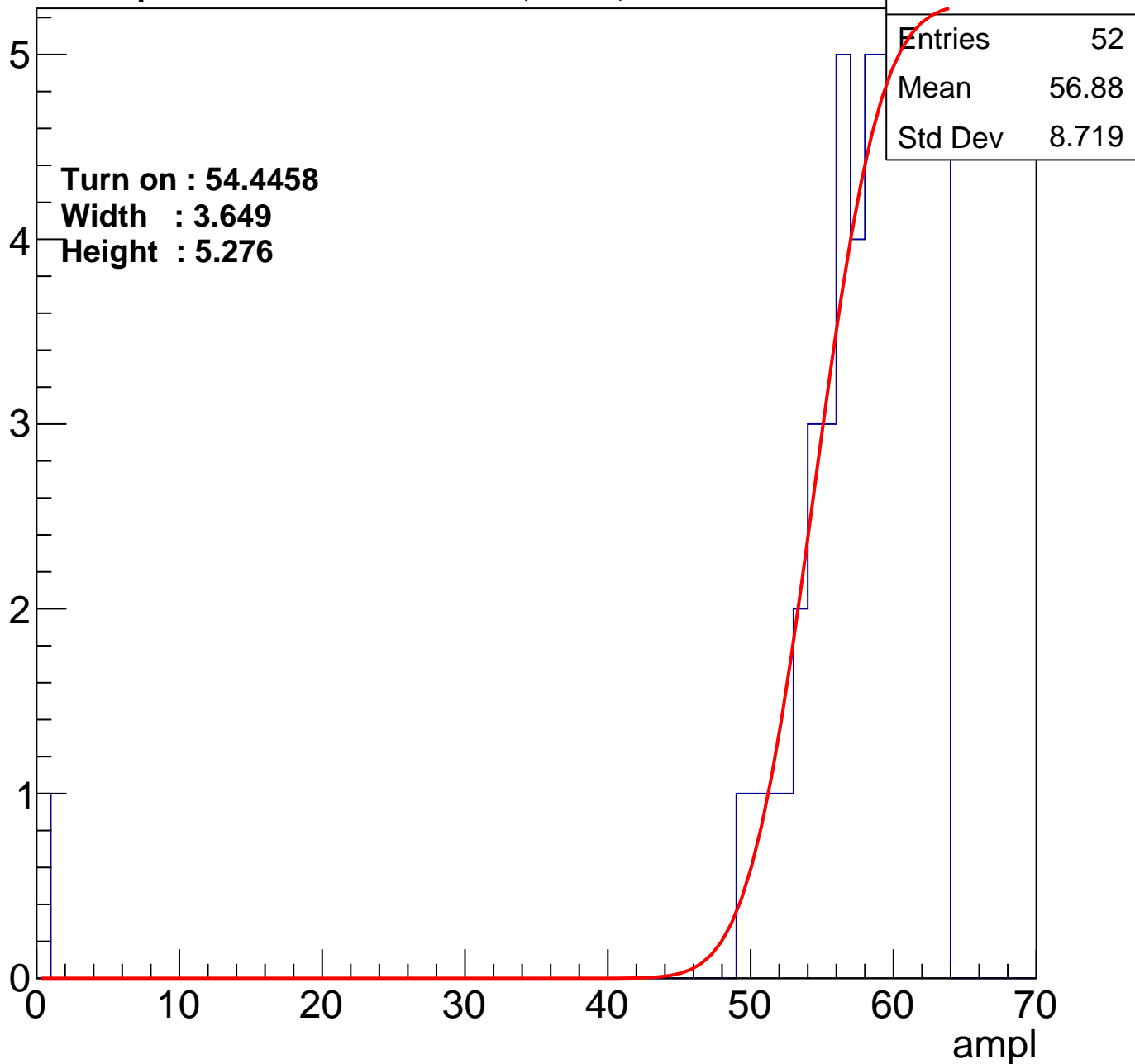
Entry

5
4
3
2
1
0

Turn on : 54.4458
Width : 3.649
Height : 5.276

Entries	52
Mean	56.88
Std Dev	8.719

ampl



B0L103S, U15-ch19

calib_packv5_040323_1717.root, FC#2, Port C3

Entry

5

4

3

2

1

0

Turn on : 51.9281

Width : 3.838

Height : 5.164

Entries	69
Mean	52.54
Std Dev	15.29

ampl

0

10

20

30

40

50

60

70

B0L103S, U15-ch20

calib_packv5_040323_1717.root, FC#2, Port C3

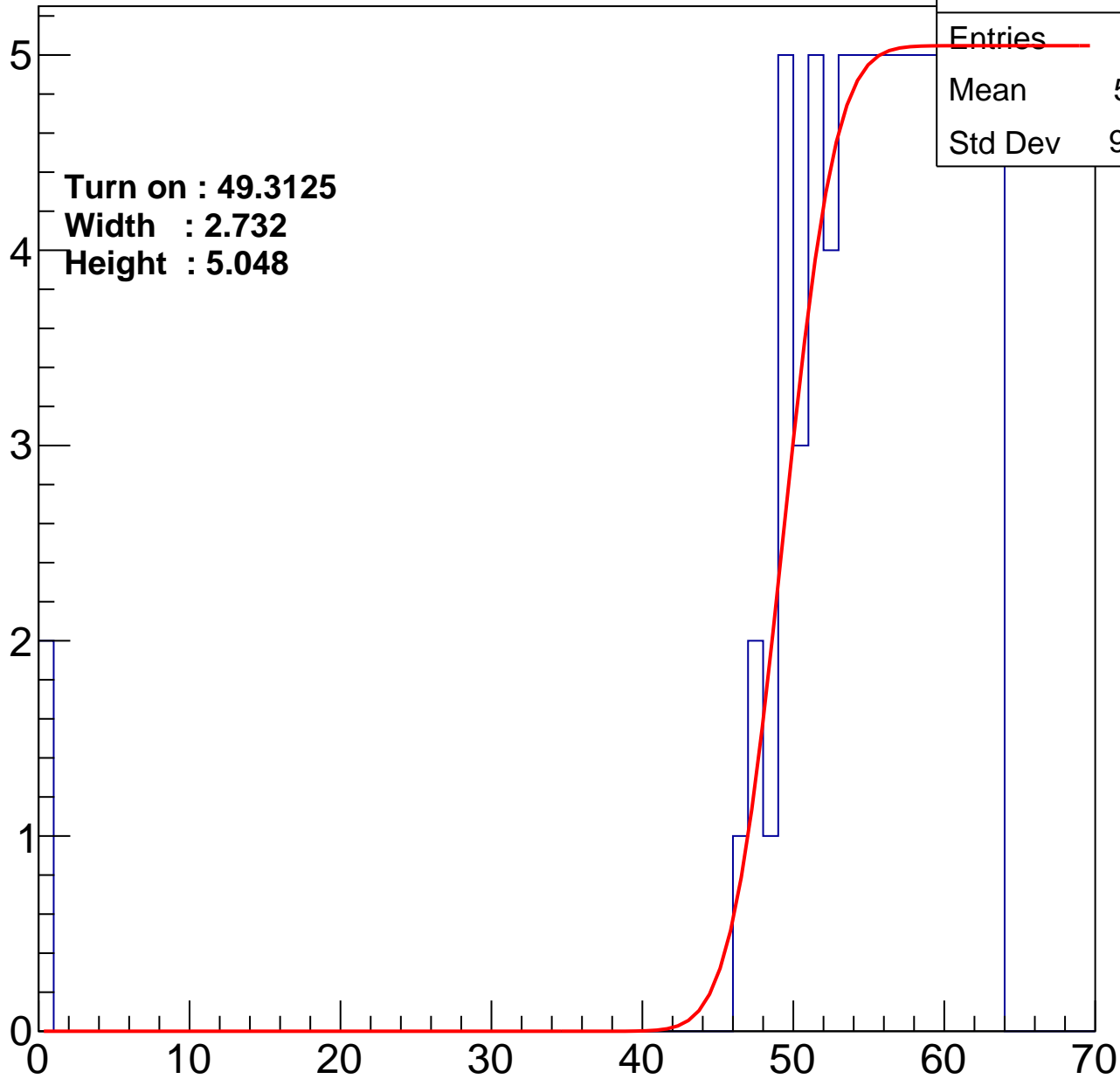
Entry

5
4
3
2
1
0

Turn on : 49.3125
Width : 2.732
Height : 5.048

Entries	78
Mean	54.31
Std Dev	9.927

ampl



B0L103S, U15-ch21

calib_packv5_040323_1717.root, FC#2, Port C3

Entry

5

4

3

2

1

0

Turn on : 53.6922

Width : 3.962

Height : 5.309

Entries	58
Mean	55.57
Std Dev	11.14

ampl

0

10

20

30

40

50

60

70

B0L103S, U15-ch22

calib_packv5_040323_1717.root, FC#2, Port C3

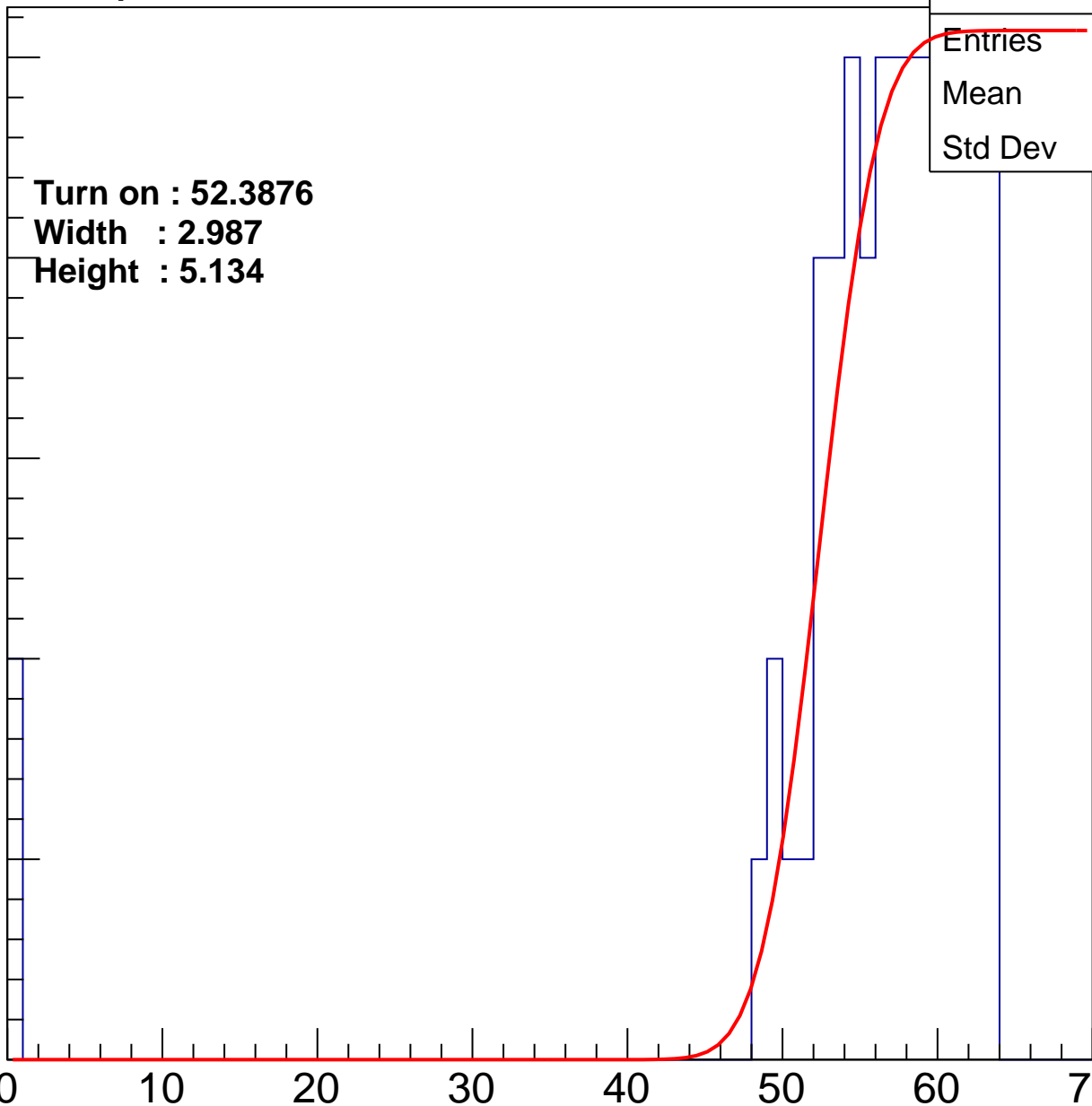
Entry

5
4
3
2
1
0

Turn on : 52.3876
Width : 2.987
Height : 5.134

Entries	64
Mean	55.27
Std Dev	10.67

ampl



B0L103S, U15-ch23

calib_packv5_040323_1717.root, FC#2, Port C3

Entry

5

4

3

2

1

0

Turn on : 50.4760

Width : 4.768

Height : 5.217

Entries	69
Mean	56.23
Std Dev	4.569

ampl

0

10

20

30

40

50

60

70

B0L103S, U15-ch24

calib_packv5_040323_1717.root, FC#2, Port C3

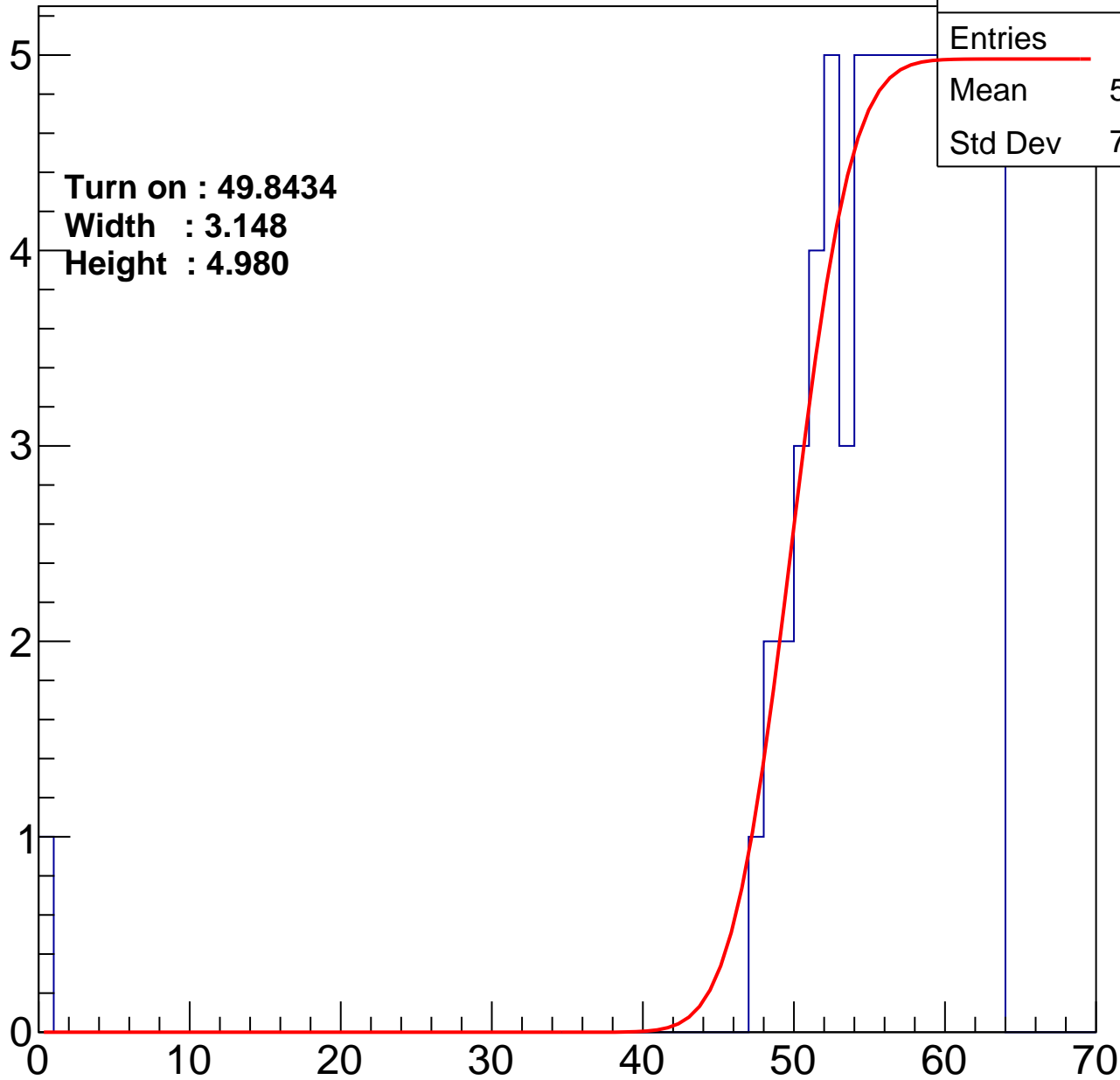
Entry

5
4
3
2
1
0

Turn on : 49.8434
Width : 3.148
Height : 4.980

Entries	71
Mean	55.48
Std Dev	7.929

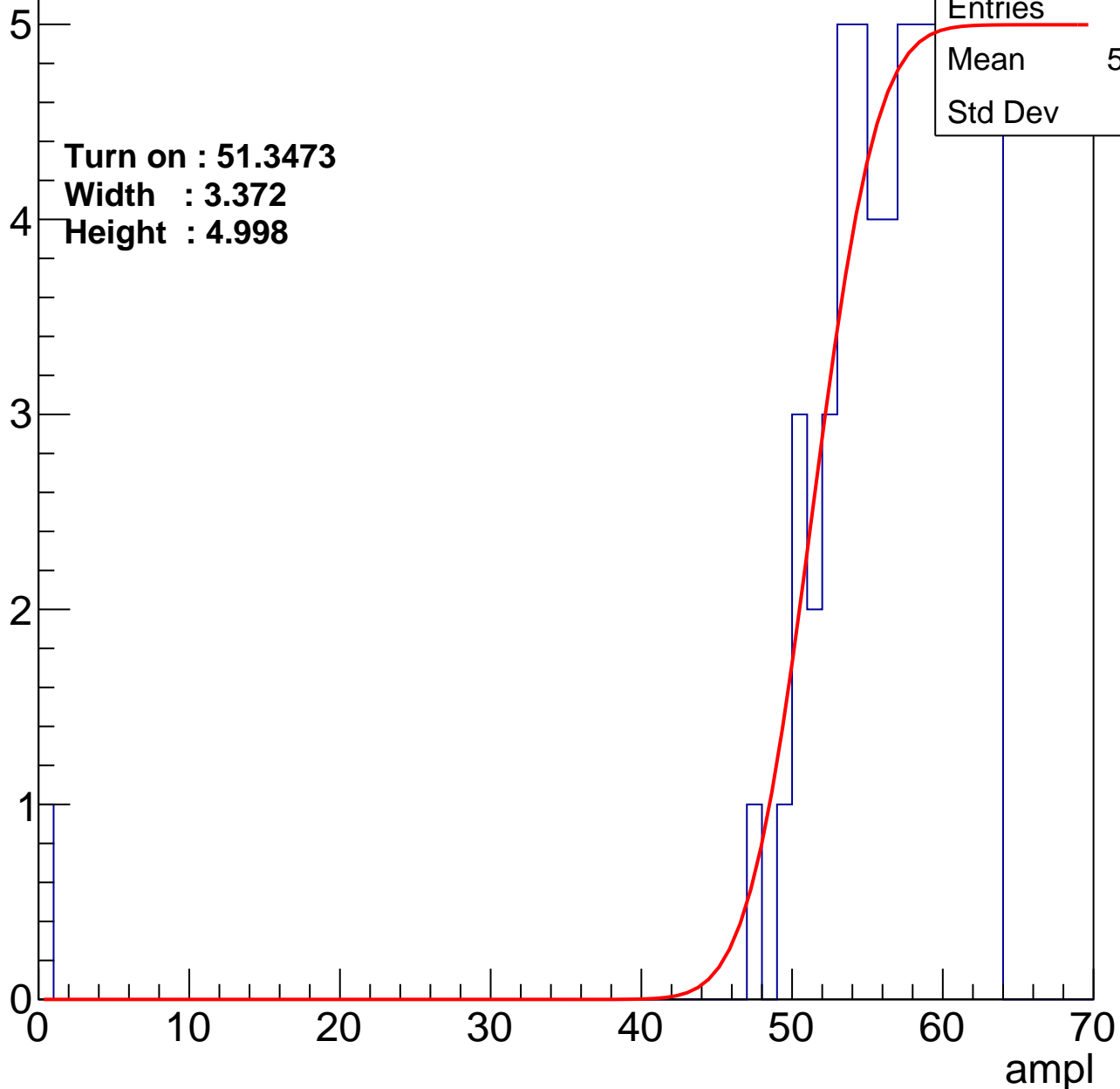
ampl



B0L103S, U15-ch25

calib_packv5_040323_1717.root, FC#2, Port C3

Entry



B0L103S, U15-ch26

calib_packv5_040323_1717.root, FC#2, Port C3

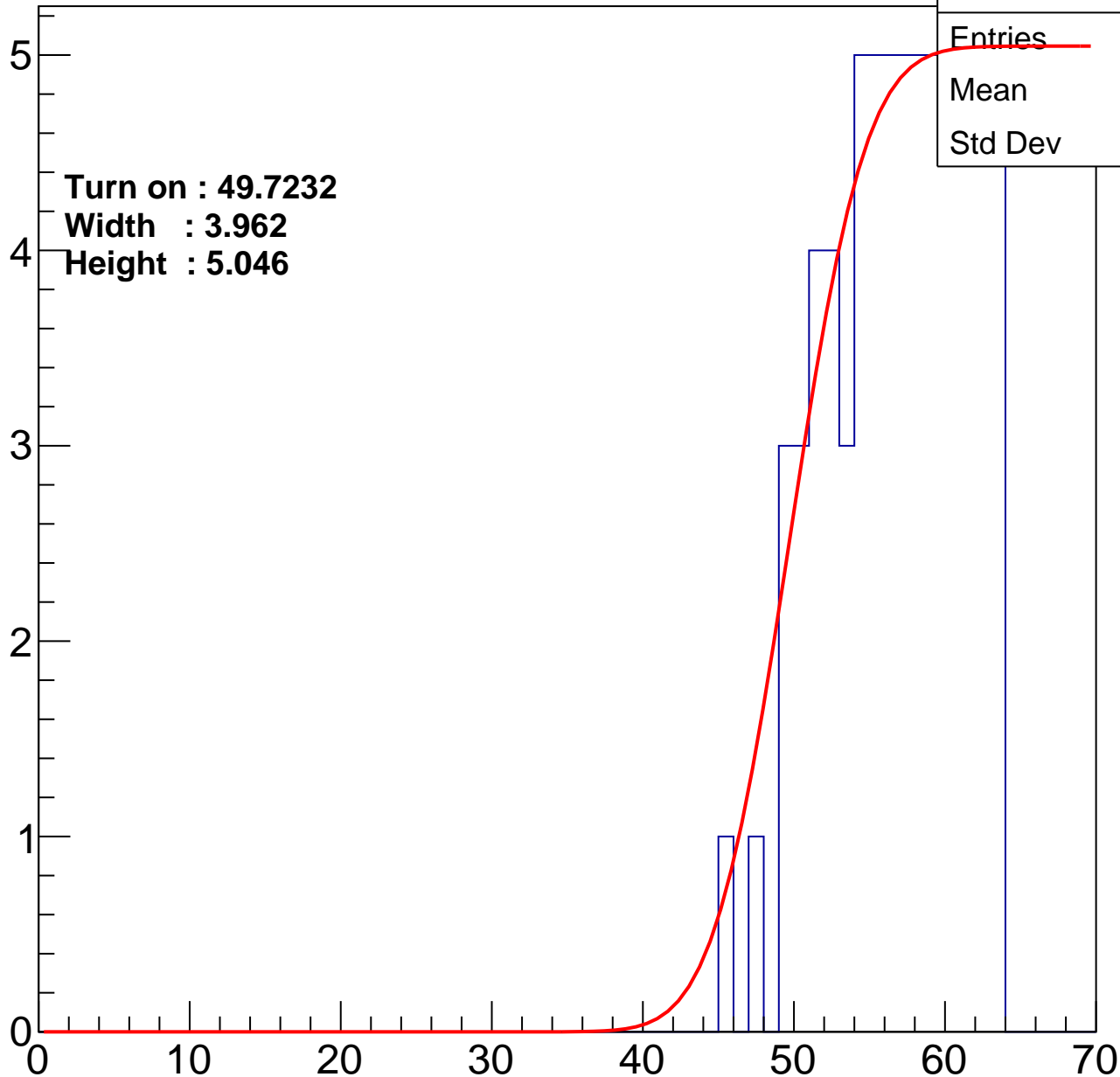
Entry

5
4
3
2
1
0

Turn on : 49.7232
Width : 3.962
Height : 5.046

Entries	69
Mean	56.3
Std Dev	4.45

ampl



B0L103S, U15-ch27

calib_packv5_040323_1717.root, FC#2, Port C3

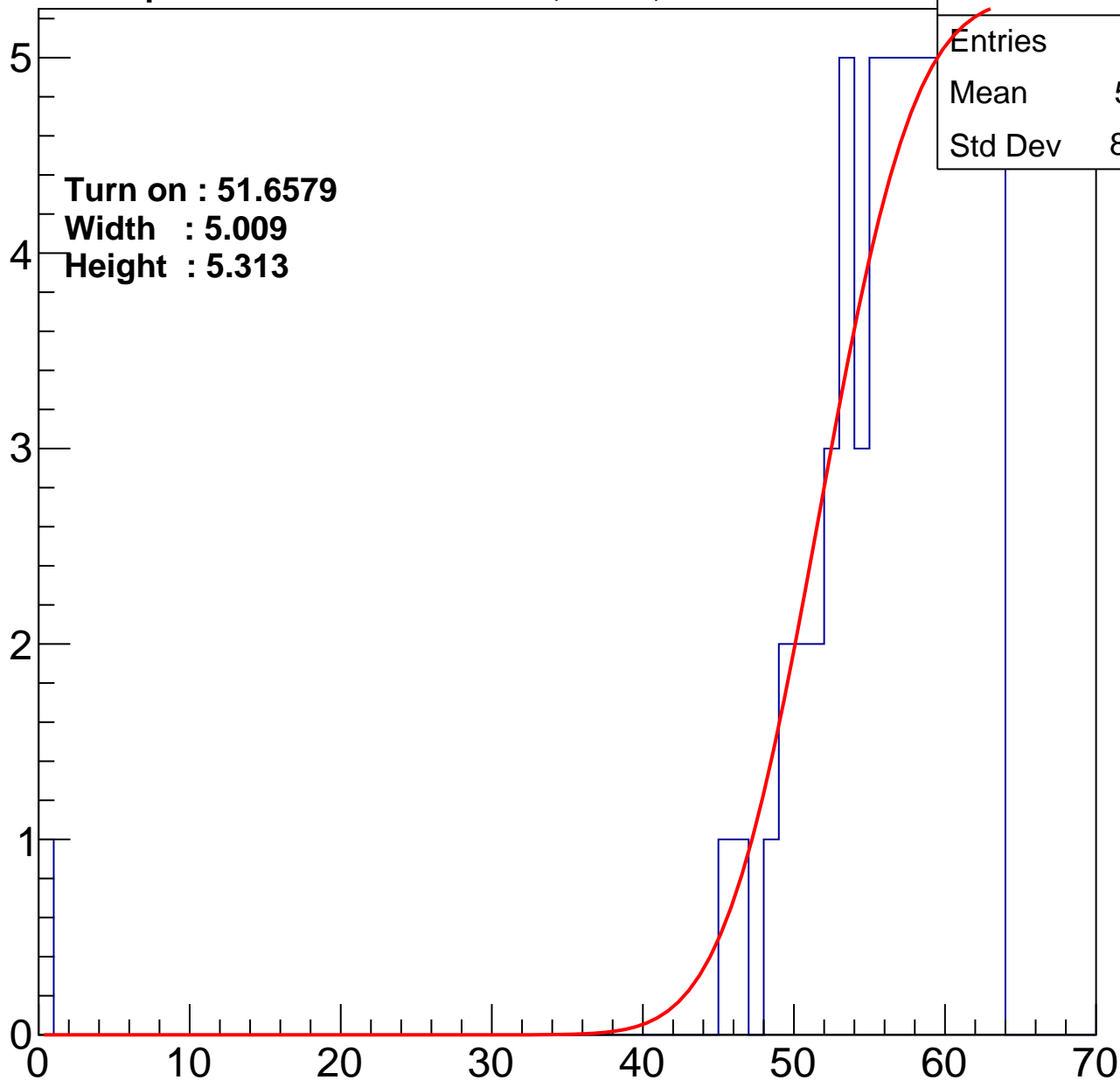
Entry

5
4
3
2
1
0

Turn on : 51.6579
Width : 5.009
Height : 5.313

Entries	66
Mean	55.71
Std Dev	8.207

ampl



B0L103S, U15-ch28

calib_packv5_040323_1717.root, FC#2, Port C3

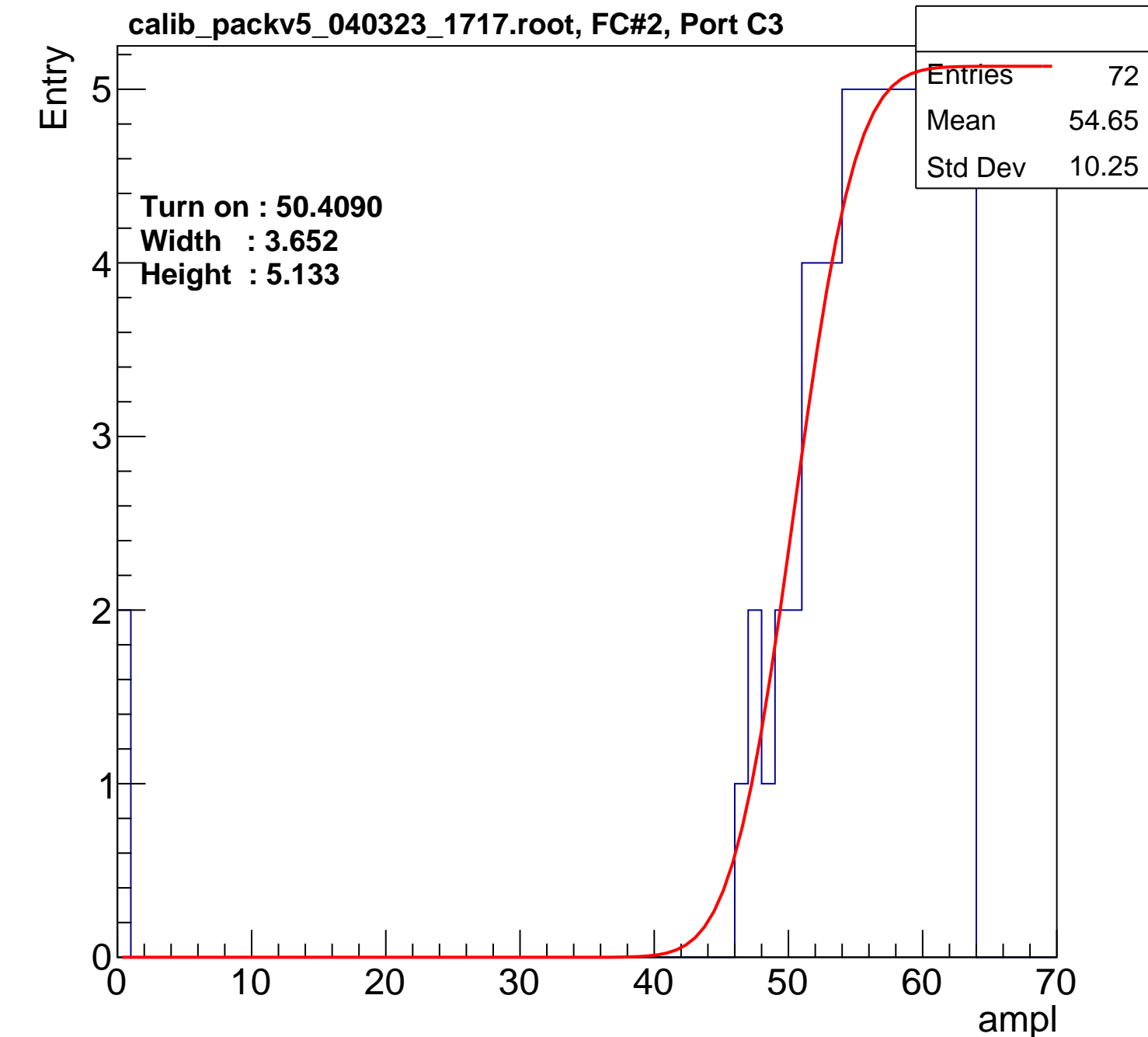
Entry

5
4
3
2
1
0

Turn on : 50.4090
Width : 3.652
Height : 5.133

Entries	72
Mean	54.65
Std Dev	10.25

ampl



B0L103S, U15-ch29

calib_packv5_040323_1717.root, FC#2, Port C3

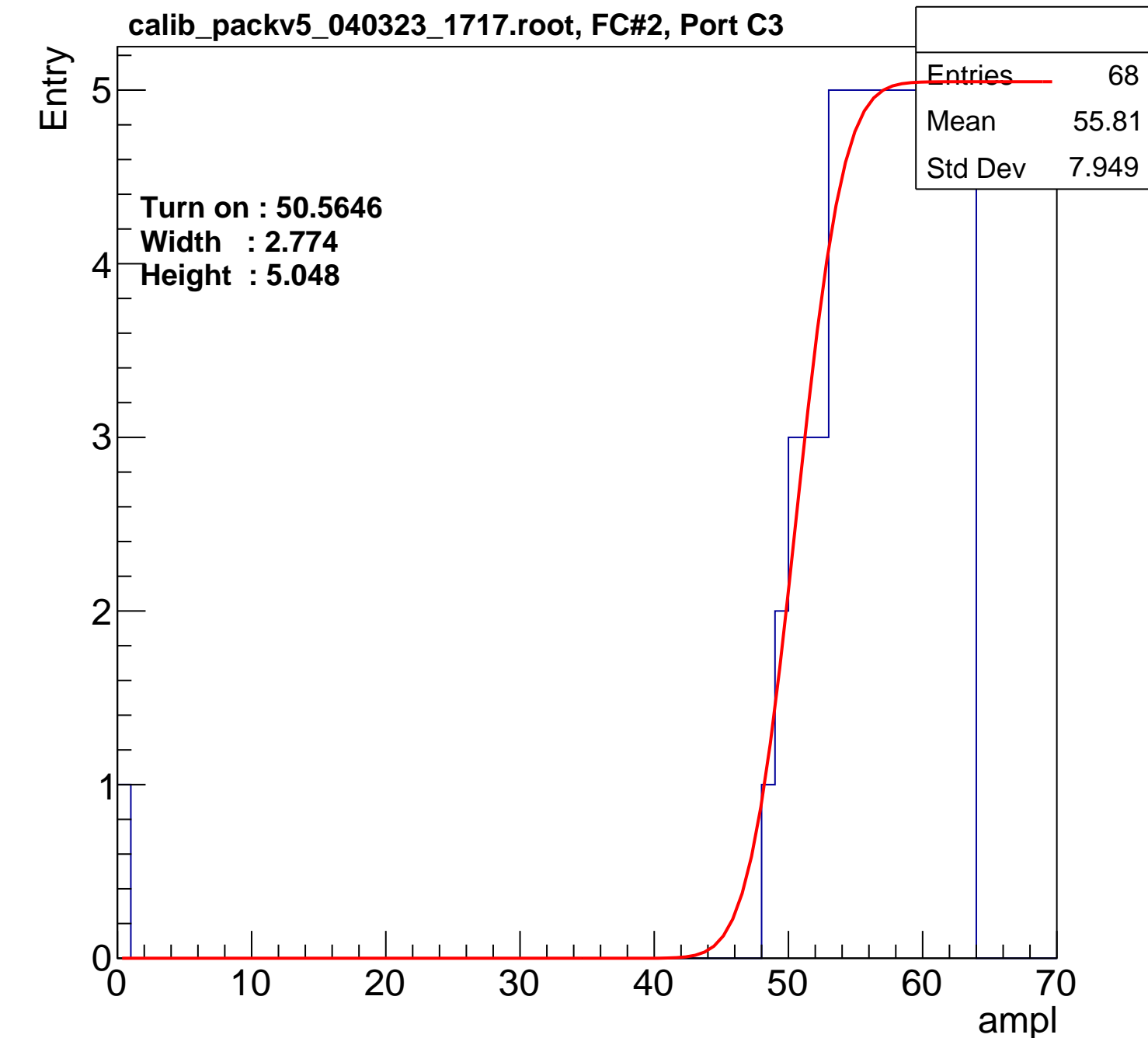
Entry

5
4
3
2
1
0

Turn on : 50.5646
Width : 2.774
Height : 5.048

Entries	68
Mean	55.81
Std Dev	7.949

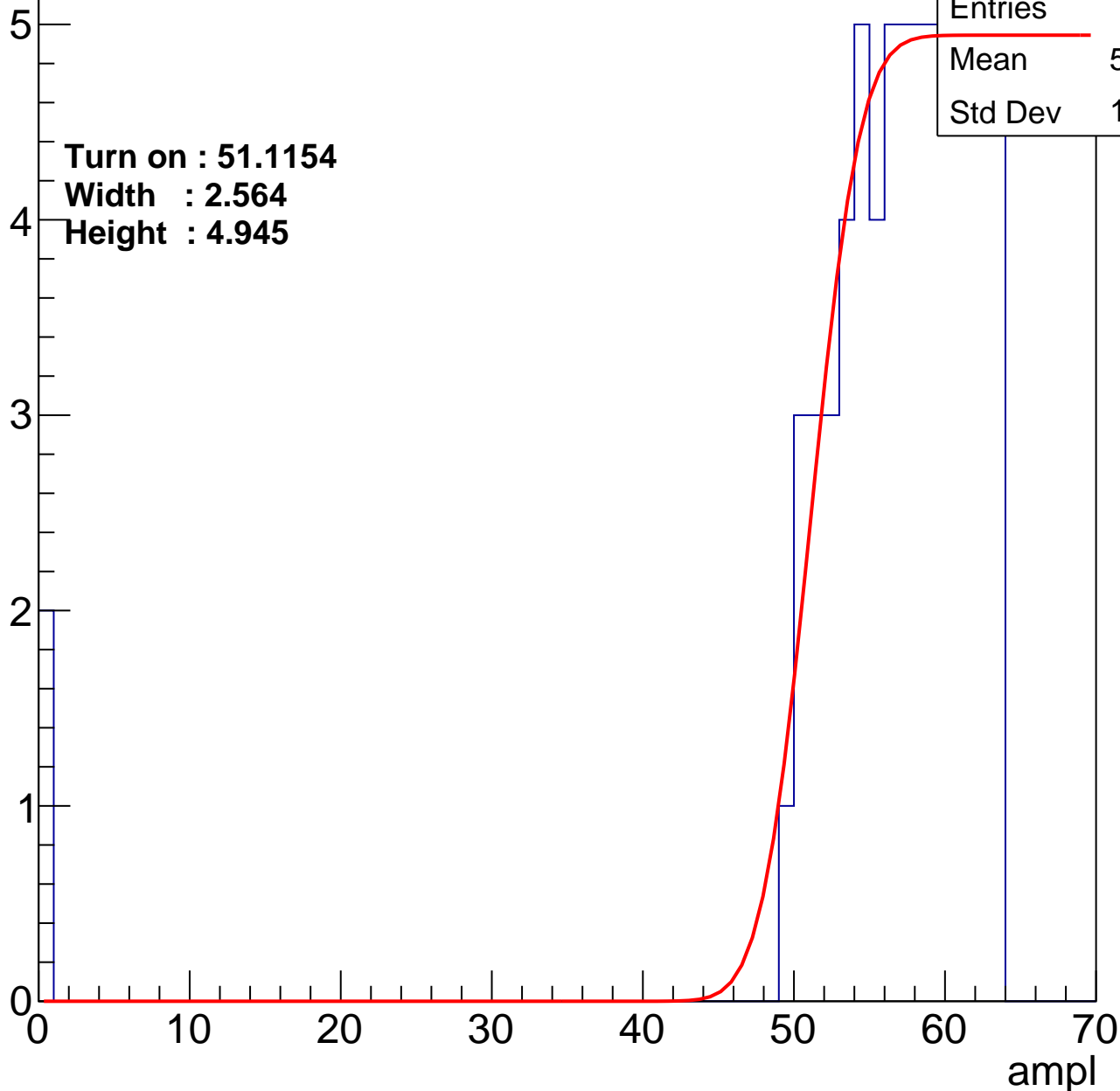
ampl



B0L103S, U15-ch30

calib_packv5_040323_1717.root, FC#2, Port C3

Entry



B0L103S, U15-ch31

calib_packv5_040323_1717.root, FC#2, Port C3

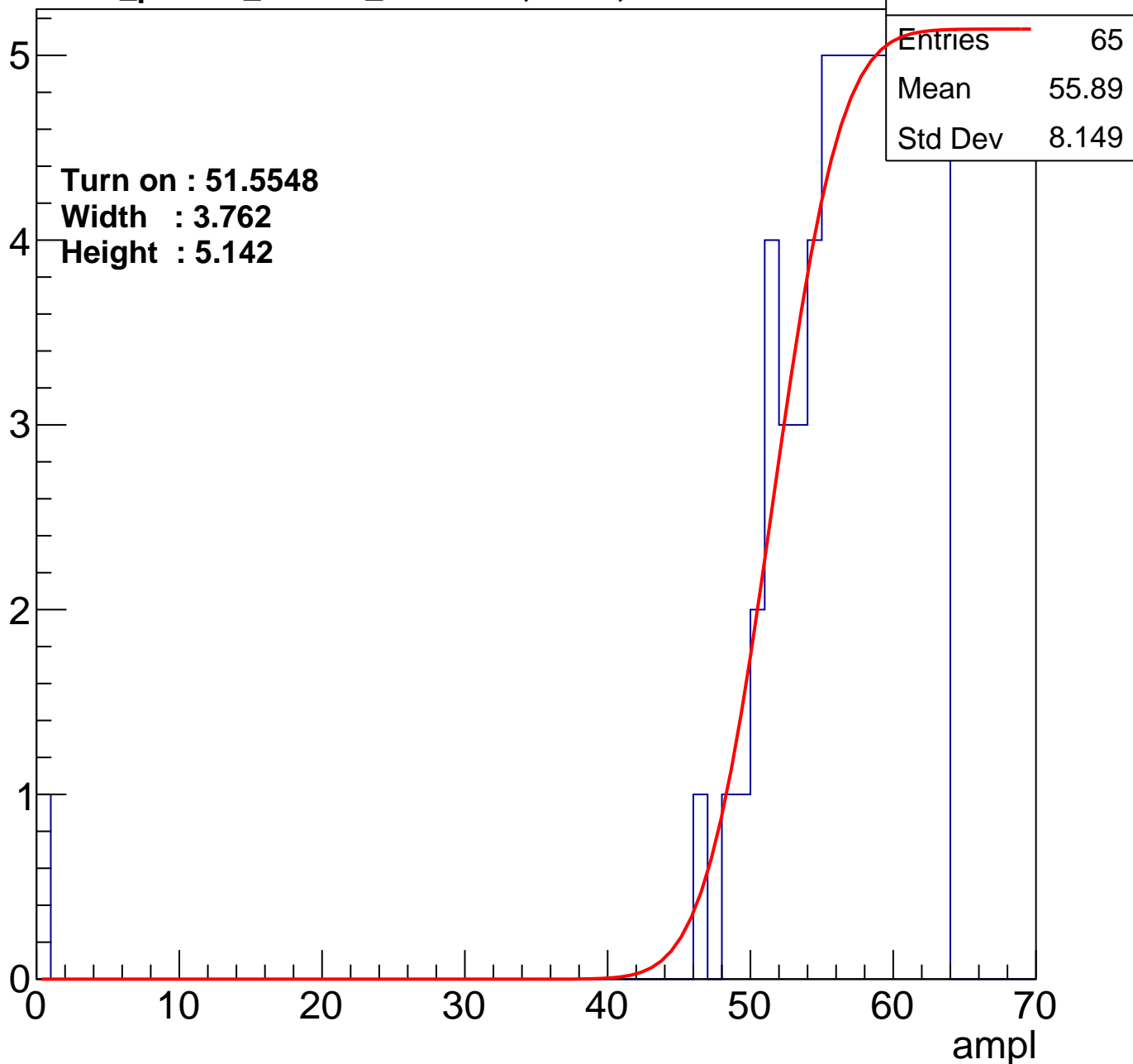
Entry

5
4
3
2
1
0

Turn on : 51.5548
Width : 3.762
Height : 5.142

Entries	65
Mean	55.89
Std Dev	8.149

ampl



B0L103S, U15-ch32

calib_packv5_040323_1717.root, FC#2, Port C3

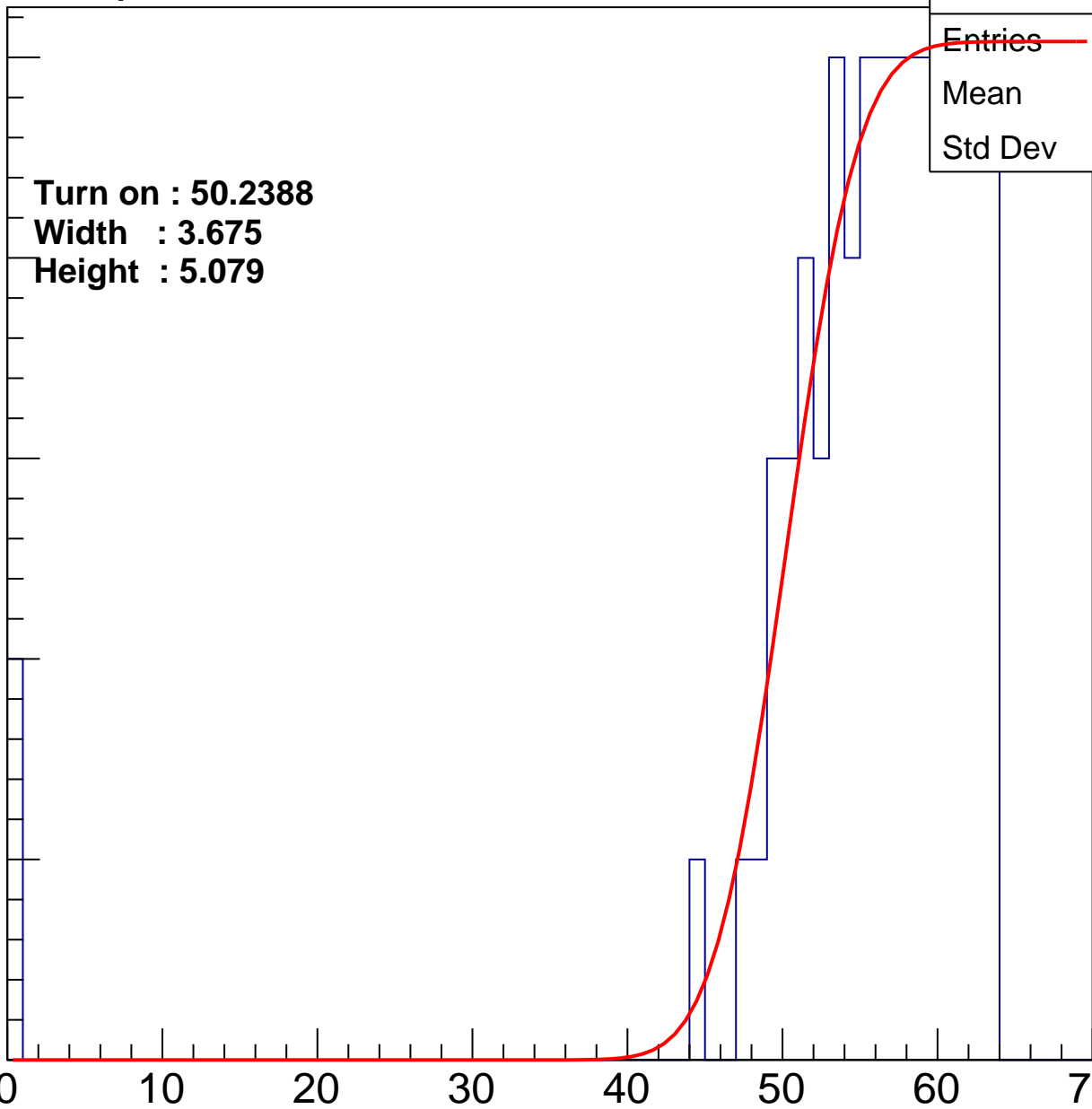
Entry

5
4
3
2
1
0

Turn on : 50.2388
Width : 3.675
Height : 5.079

Entries	72
Mean	54.61
Std Dev	10.27

ampl



B0L103S, U15-ch33

calib_packv5_040323_1717.root, FC#2, Port C3

Entry

5

4

3

2

1

0

Turn on : 51.1185

Width : 4.254

Height : 5.220

Entries	70
Mean	54.8
Std Dev	10.34

ampl

0

10

20

30

40

50

60

70

B0L103S, U15-ch34

calib_packv5_040323_1717.root, FC#2, Port C3

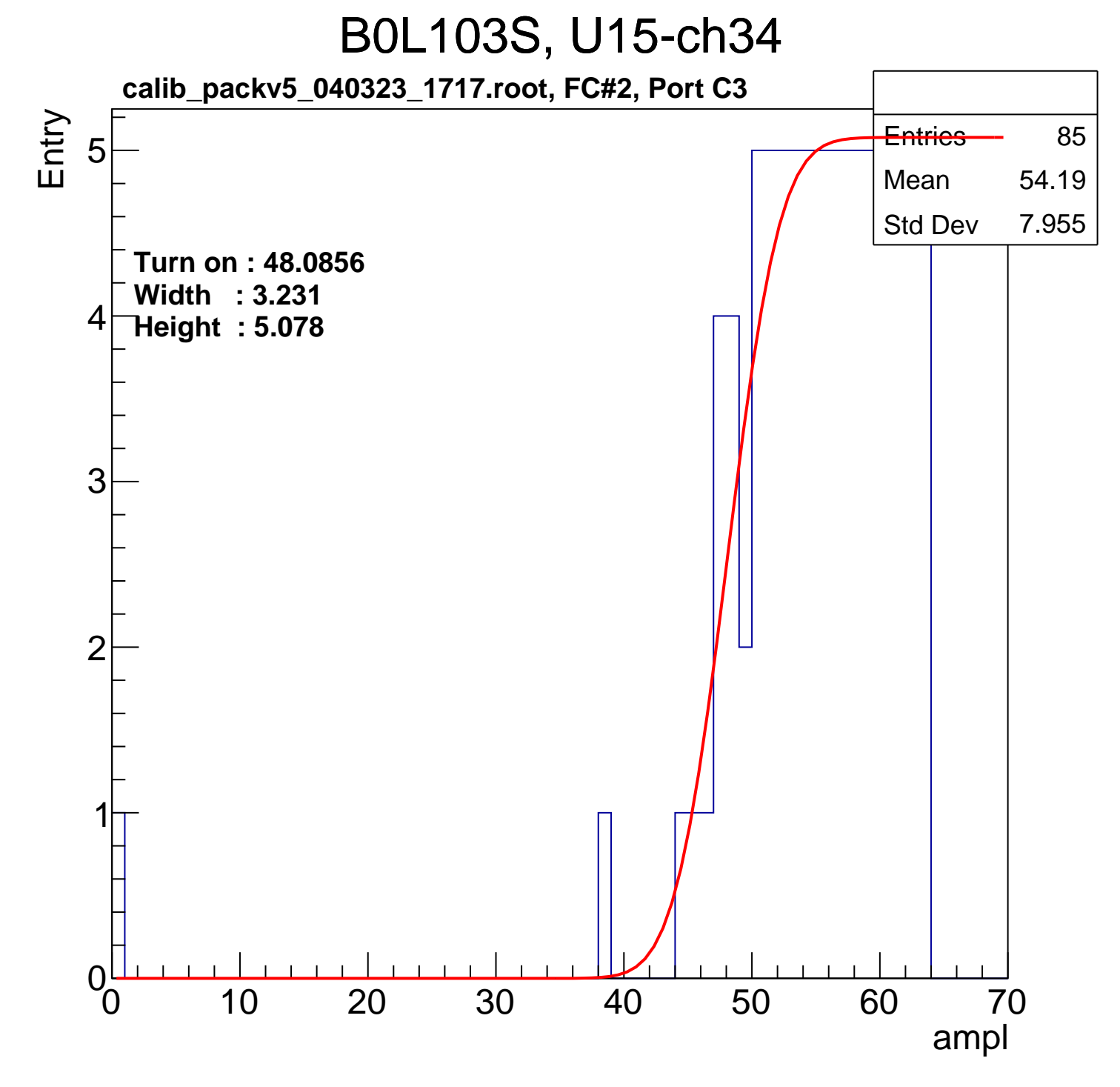
Entry

5
4
3
2
1
0

Turn on : 48.0856
Width : 3.231
Height : 5.078

Entries	85
Mean	54.19
Std Dev	7.955

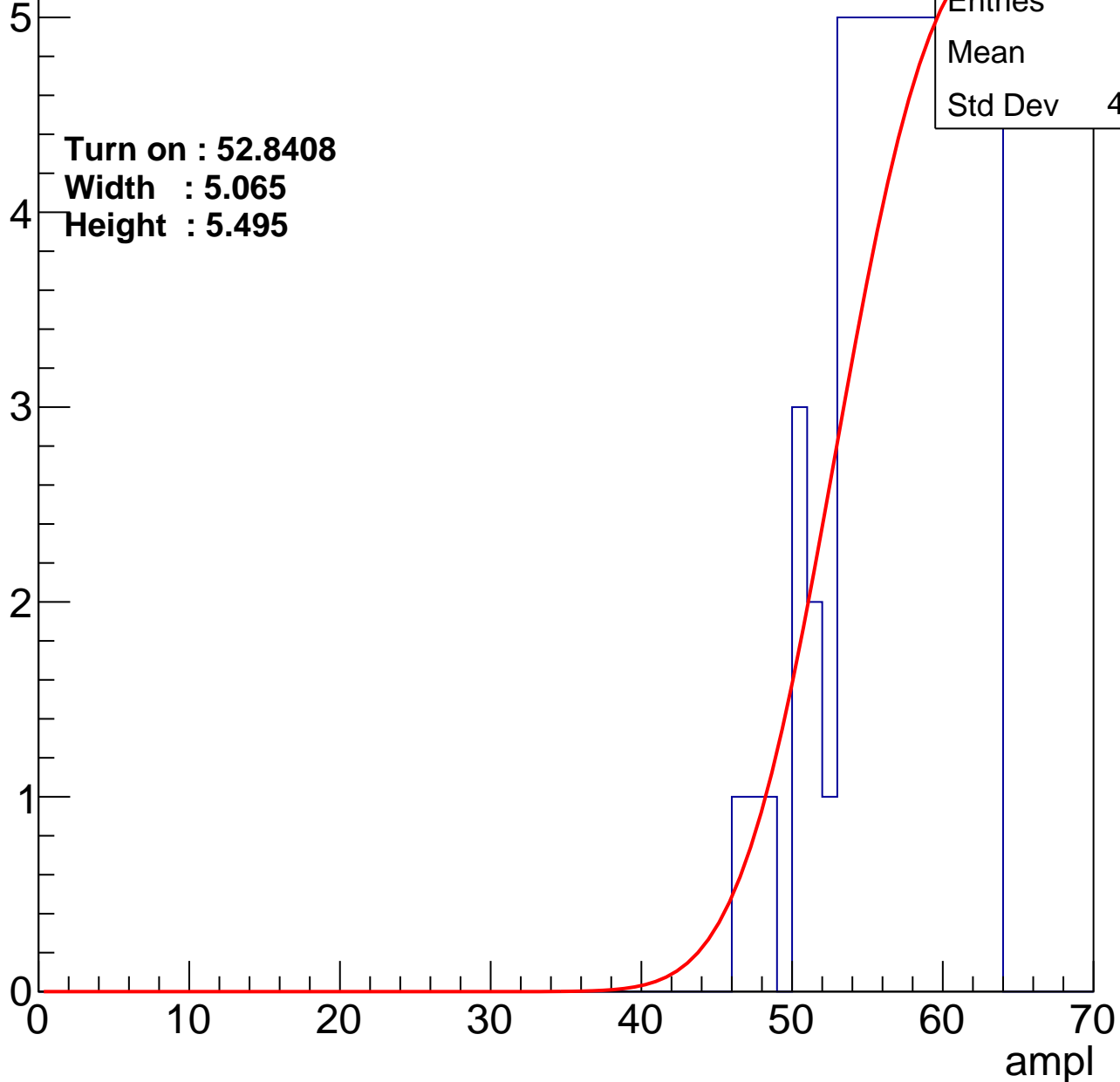
ampl



B0L103S, U15-ch35

calib_packv5_040323_1717.root, FC#2, Port C3

Entry



B0L103S, U15-ch36

calib_packv5_040323_1717.root, FC#2, Port C3

Entry

5

4

3

2

1

0

Turn on : 48.9080

Width : 2.984

Height : 4.954

Entries	78
Mean	52.4
Std Dev	14.39

ampl

0

10

20

30

40

50

60

70

B0L103S, U15-ch37

calib_packv5_040323_1717.root, FC#2, Port C3

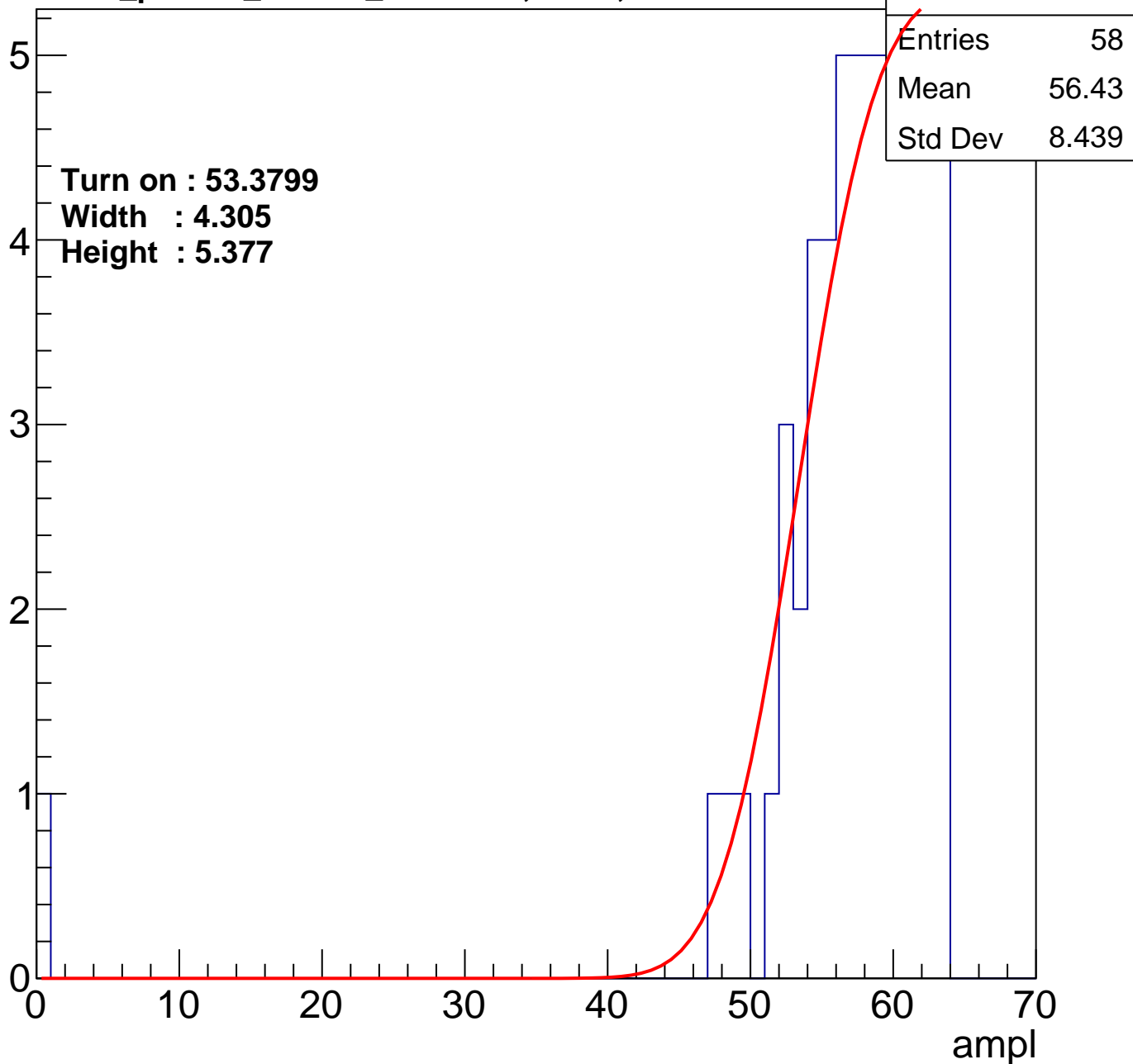
Entry

5
4
3
2
1
0

Turn on : 53.3799
Width : 4.305
Height : 5.377

Entries	58
Mean	56.43
Std Dev	8.439

ampl



B0L103S, U15-ch38

calib_packv5_040323_1717.root, FC#2, Port C3

Entry

5

4

3

2

1

0

Turn on : 50.4161

Width : 4.414

Height : 5.170

Entries	71
Mean	54.65
Std Dev	10.34

ampl

0

10

20

30

40

50

60

70

B0L103S, U15-ch39

calib_packv5_040323_1717.root, FC#2, Port C3

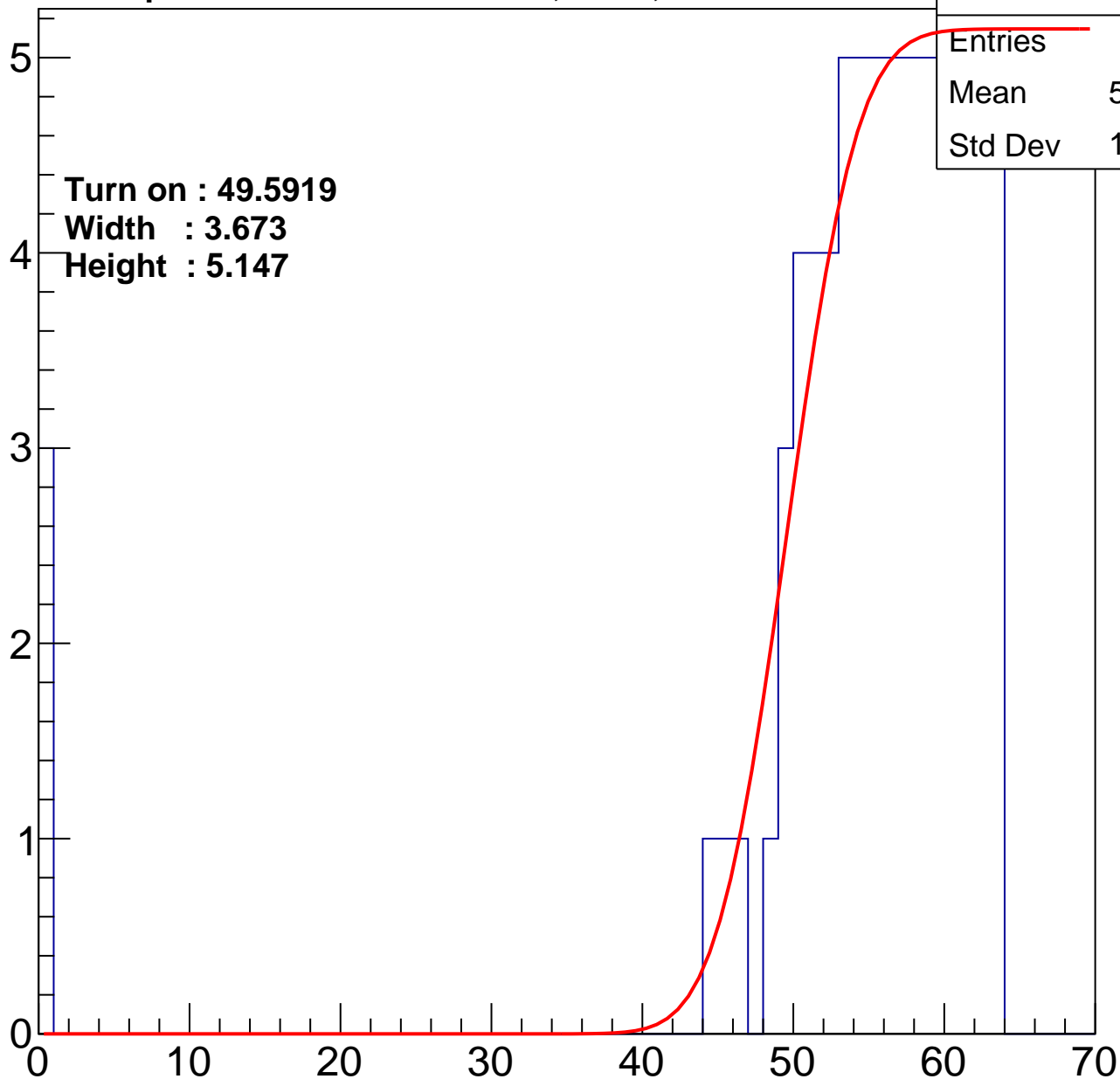
Entry

5
4
3
2
1
0

Turn on : 49.5919
Width : 3.673
Height : 5.147

Entries	77
Mean	53.66
Std Dev	11.76

ampl



B0L103S, U15-ch40

calib_packv5_040323_1717.root, FC#2, Port C3

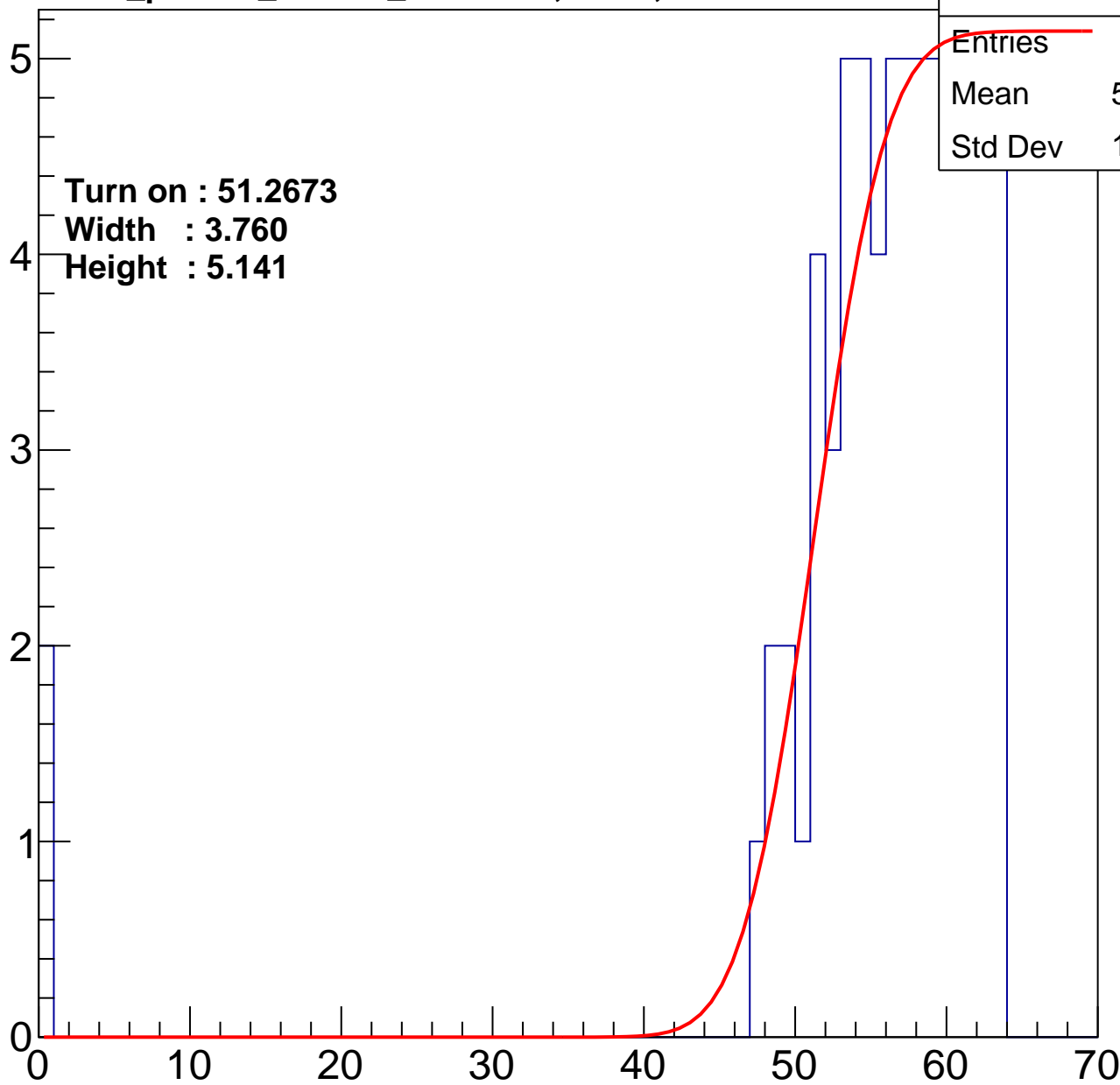
Entry

5
4
3
2
1
0

Turn on : 51.2673
Width : 3.760
Height : 5.141

Entries	69
Mean	54.87
Std Dev	10.39

ampl



B0L103S, U15-ch41

calib_packv5_040323_1717.root, FC#2, Port C3

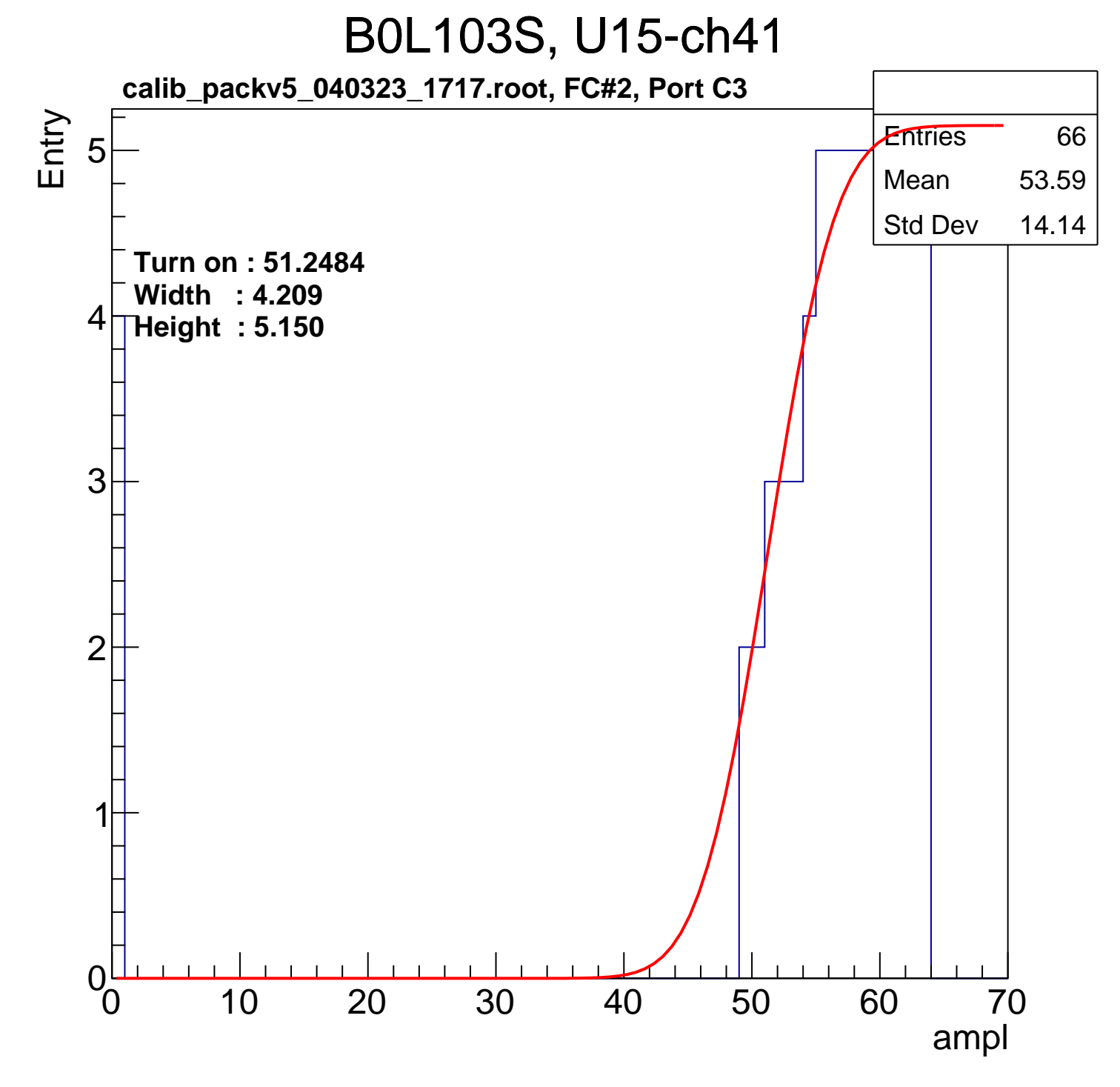
Entry

5
4
3
2
1
0

Turn on : 51.2484
Width : 4.209
Height : 5.150

Entries	66
Mean	53.59
Std Dev	14.14

ampl



B0L103S, U15-ch42

calib_packv5_040323_1717.root, FC#2, Port C3

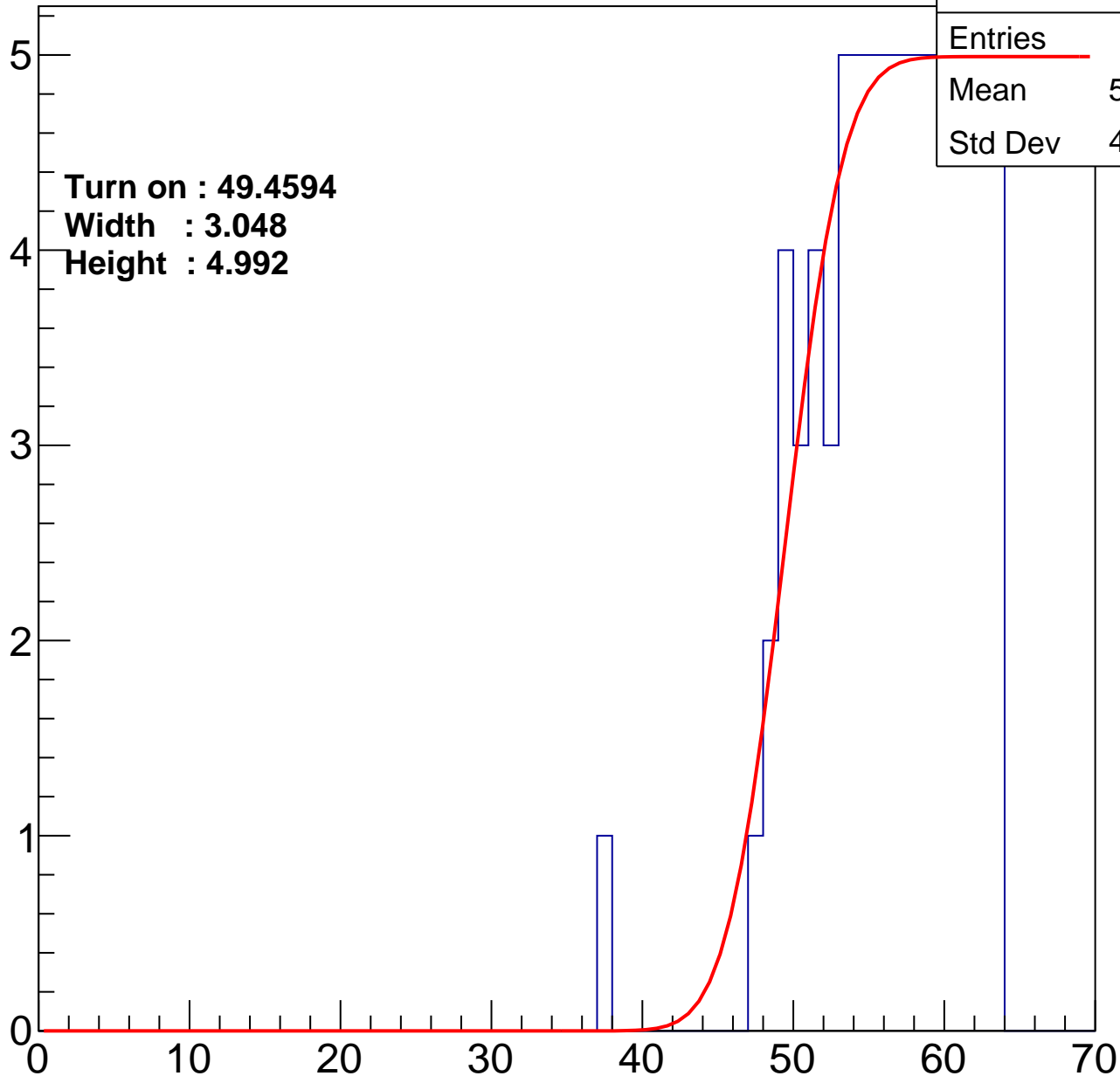
Entry

5
4
3
2
1
0

Turn on : 49.4594
Width : 3.048
Height : 4.992

Entries	73
Mean	55.84
Std Dev	4.952

ampl



B0L103S, U15-ch43

calib_packv5_040323_1717.root, FC#2, Port C3

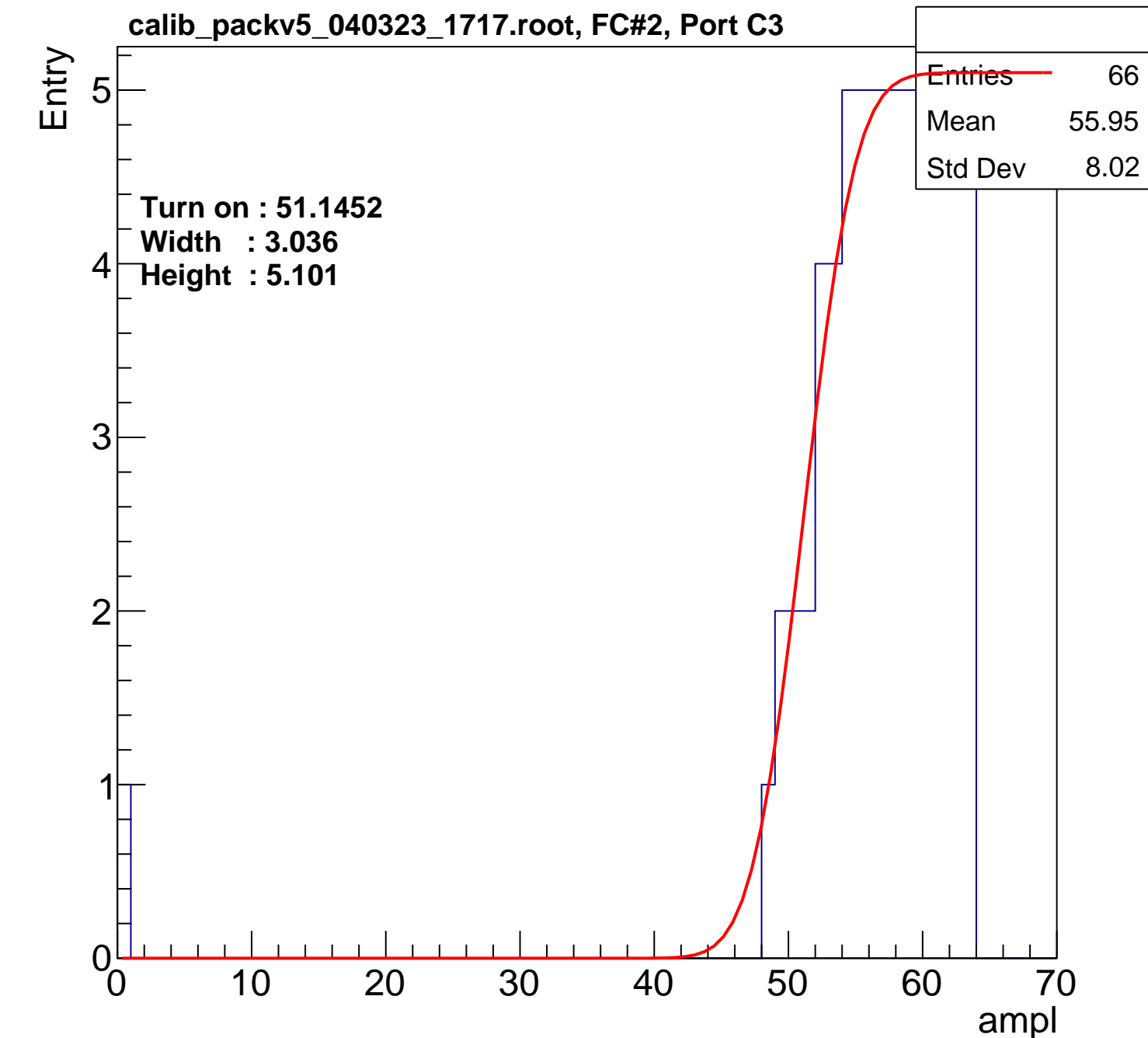
Entry

5
4
3
2
1
0

Turn on : 51.1452
Width : 3.036
Height : 5.101

Entries	66
Mean	55.95
Std Dev	8.02

ampl



B0L103S, U15-ch44

calib_packv5_040323_1717.root, FC#2, Port C3

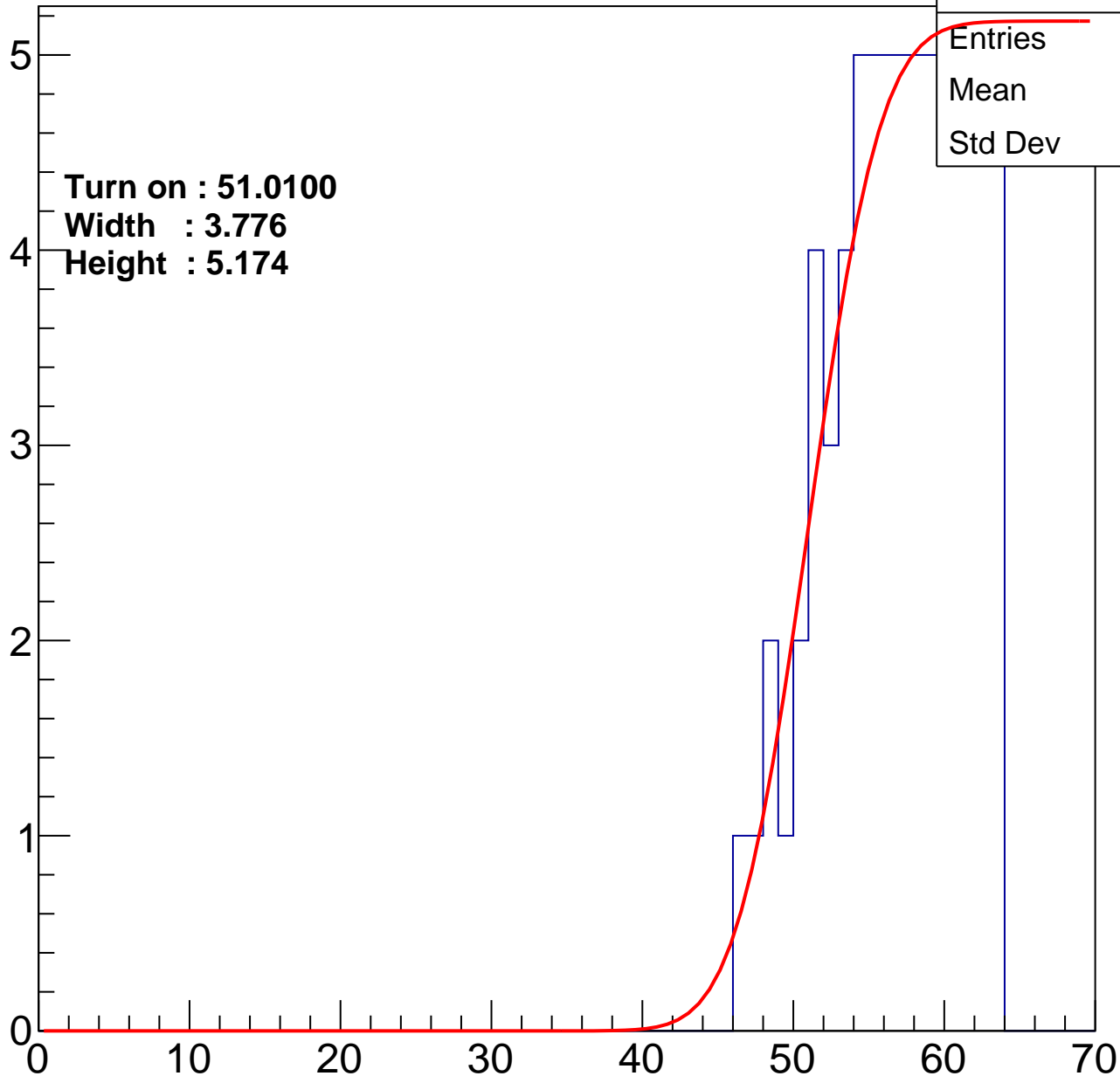
Entry

5
4
3
2
1
0

Turn on : 51.0100
Width : 3.776
Height : 5.174

Entries	68
Mean	56.4
Std Dev	4.42

ampl



B0L103S, U15-ch45

calib_packv5_040323_1717.root, FC#2, Port C3

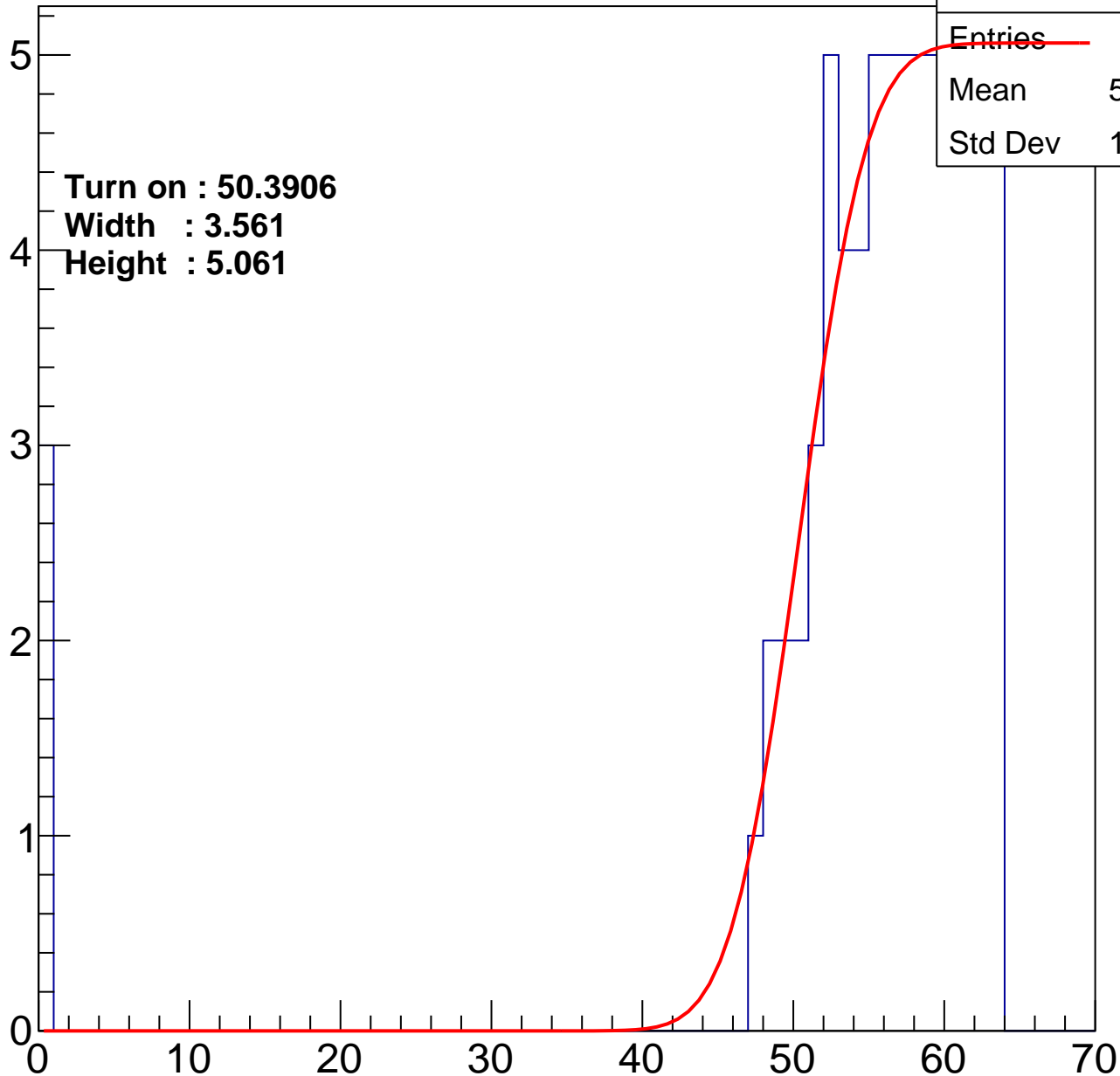
Entry

5
4
3
2
1
0

Turn on : 50.3906
Width : 3.561
Height : 5.061

Entries	71
Mean	54.04
Std Dev	12.12

ampl



B0L103S, U15-ch46

calib_packv5_040323_1717.root, FC#2, Port C3

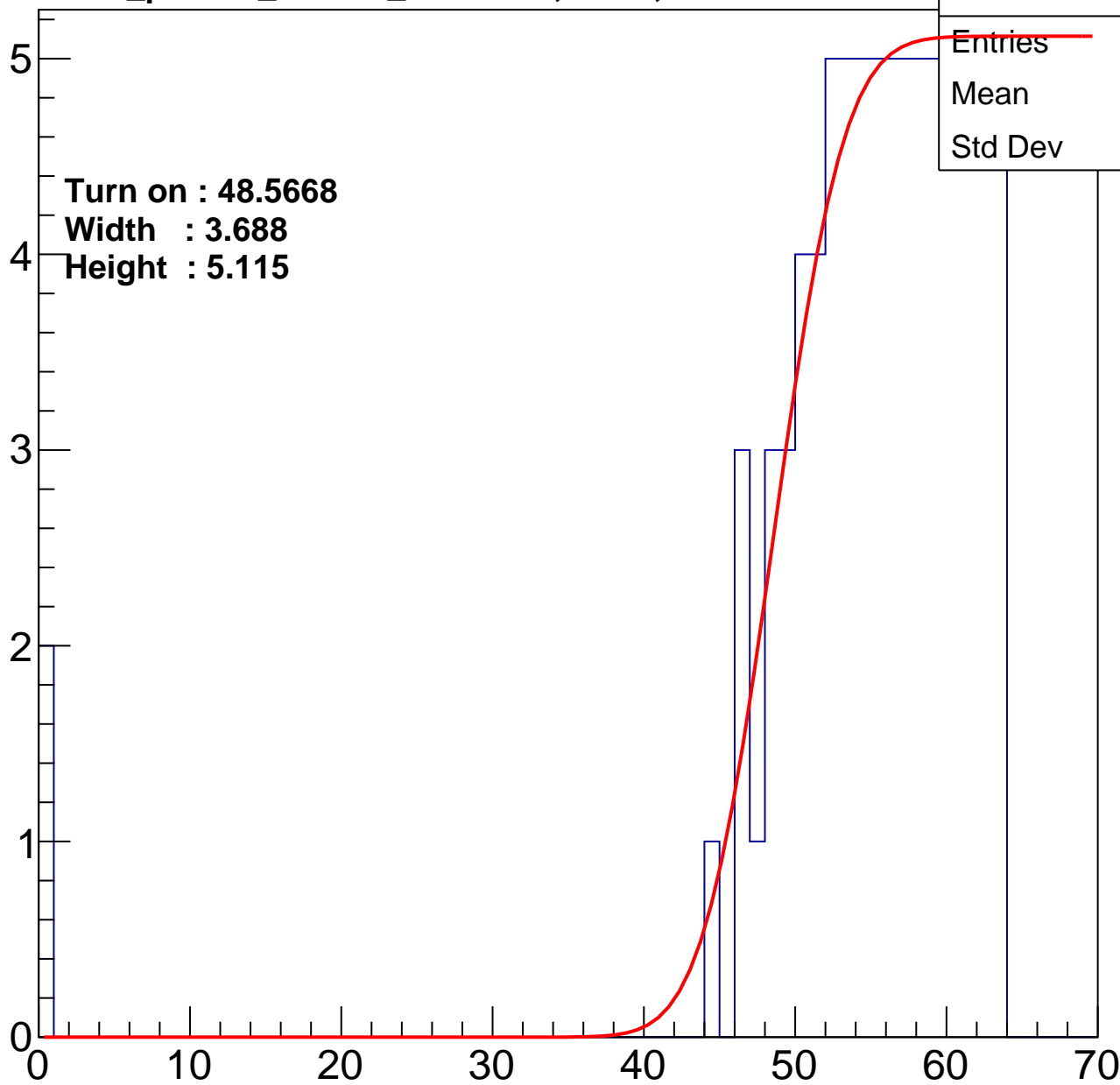
Entry

5
4
3
2
1
0

Turn on : 48.5668
Width : 3.688
Height : 5.115

Entries	81
Mean	54
Std Dev	9.88

ampl



B0L103S, U15-ch47

calib_packv5_040323_1717.root, FC#2, Port C3

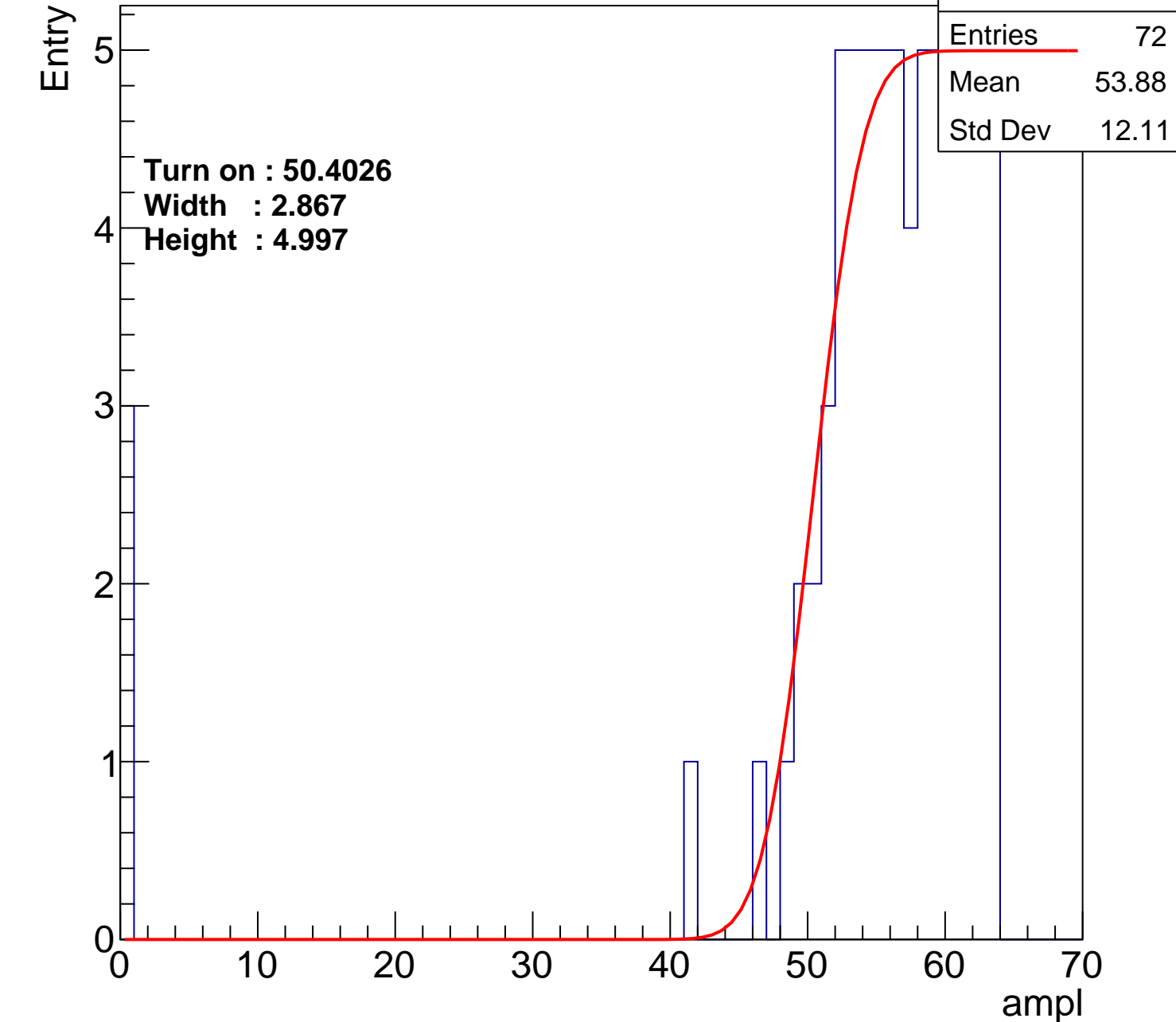
Entry

5
4
3
2
1
0

Turn on : 50.4026
Width : 2.867
Height : 4.997

Entries	72
Mean	53.88
Std Dev	12.11

ampl



B0L103S, U15-ch48

calib_packv5_040323_1717.root, FC#2, Port C3

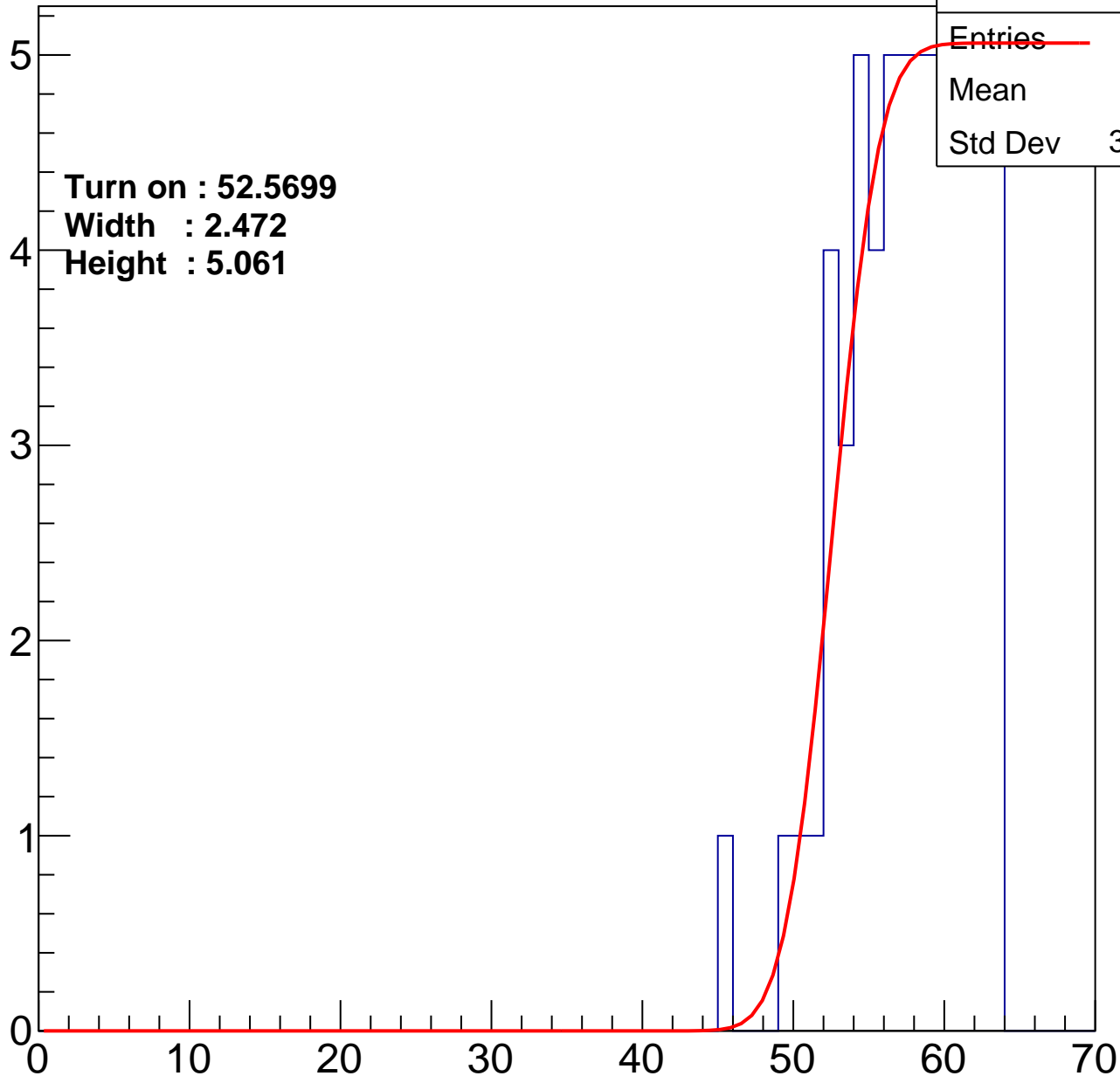
Entry

5
4
3
2
1
0

Turn on : 52.5699
Width : 2.472
Height : 5.061

Entries	60
Mean	57.2
Std Dev	3.999

ampl



B0L103S, U15-ch49

calib_packv5_040323_1717.root, FC#2, Port C3

Entry

Entries	63
Mean	53.59
Std Dev	14.49

Turn on : 54.1425

Width : 4.939

Height : 5.613

4

3

2

1

0

ampl

0

10

20

30

40

50

60

70

B0L103S, U15-ch50

calib_packv5_040323_1717.root, FC#2, Port C3

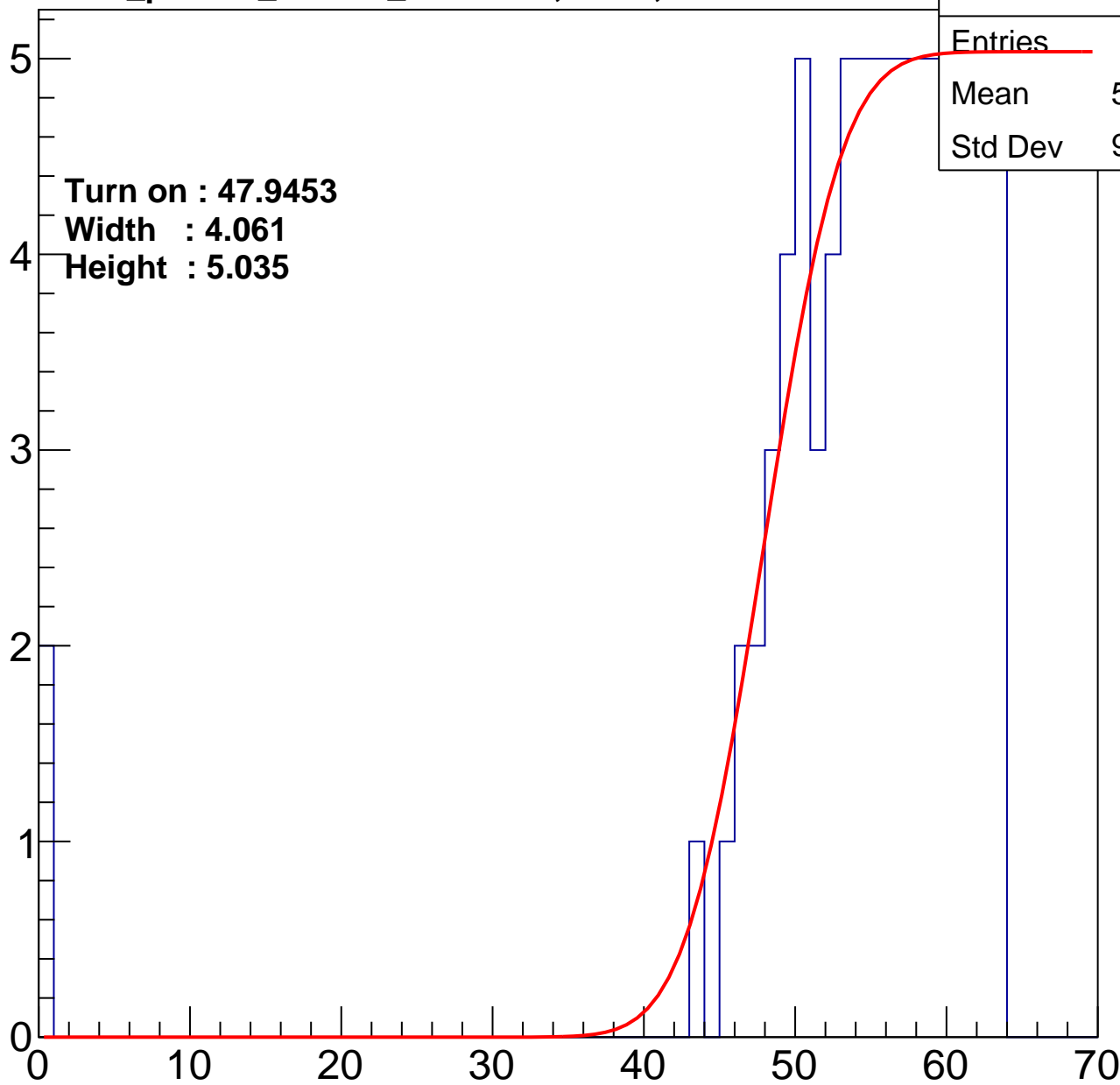
Entry

5
4
3
2
1
0

Turn on : 47.9453
Width : 4.061
Height : 5.035

Entries	82
Mean	53.84
Std Dev	9.889

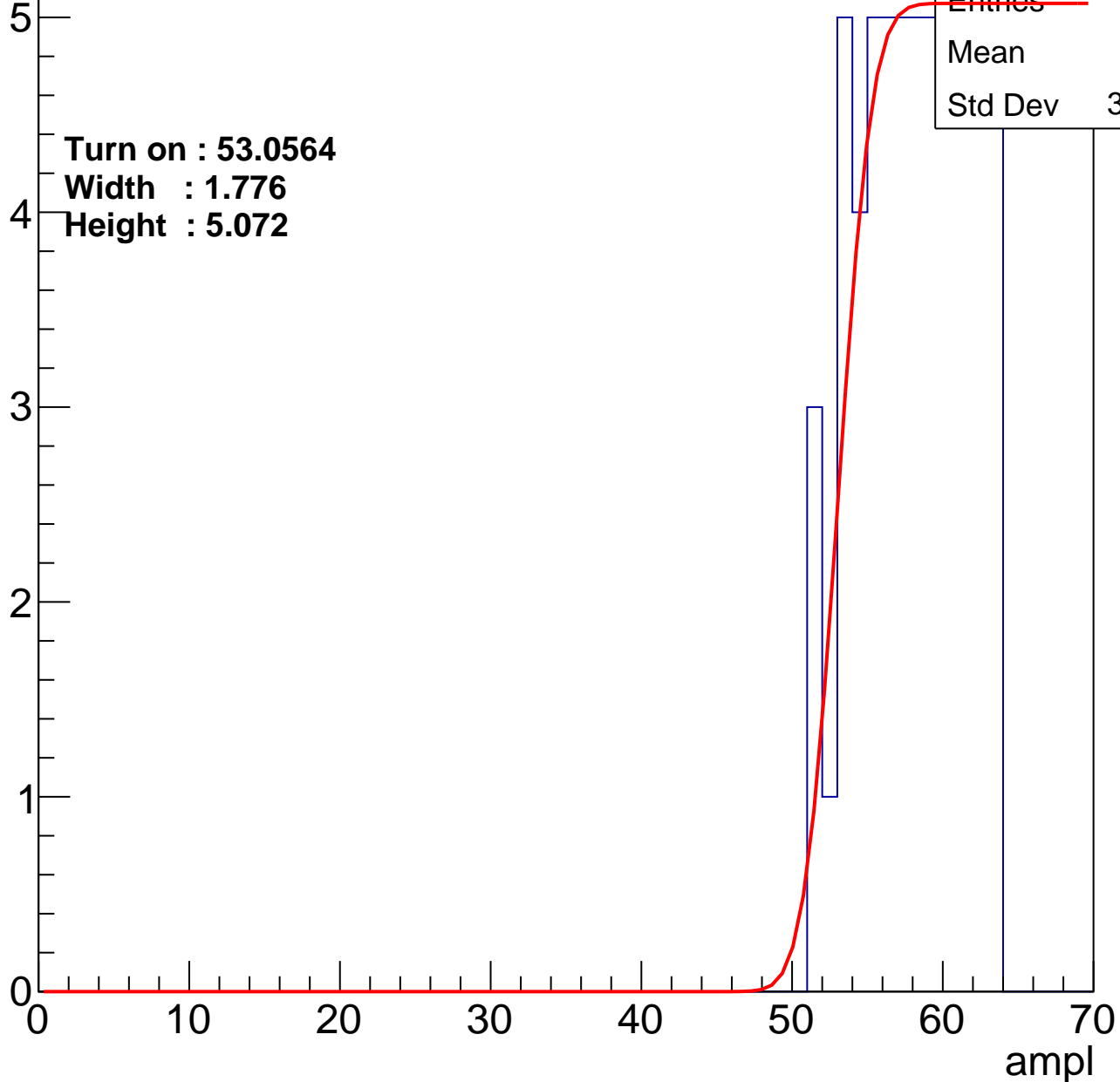
ampl



B0L103S, U15-ch51

calib_packv5_040323_1717.root, FC#2, Port C3

Entry



B0L103S, U15-ch52

calib_packv5_040323_1717.root, FC#2, Port C3

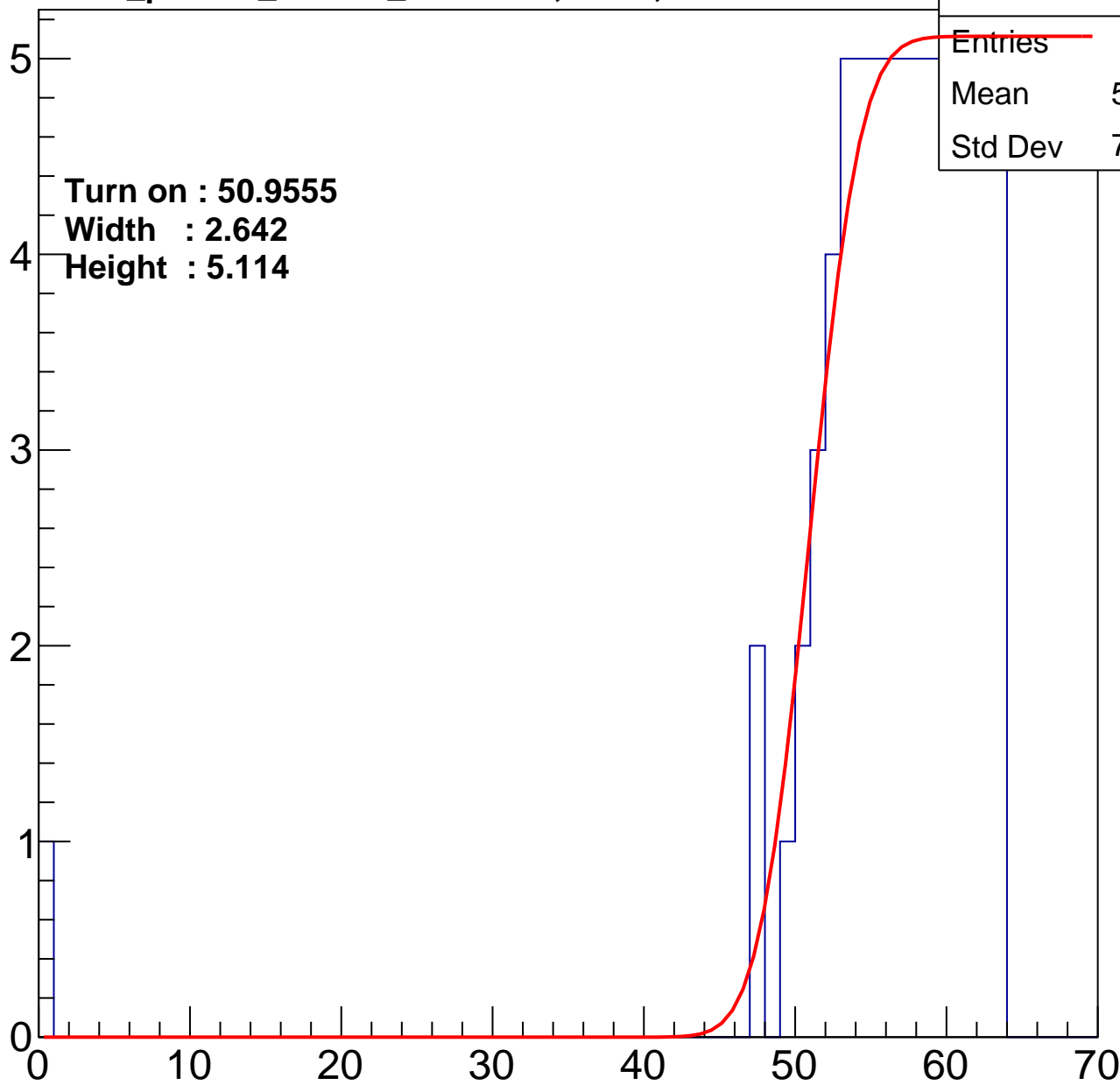
Entry

5
4
3
2
1
0

Turn on : 50.9555
Width : 2.642
Height : 5.114

Entries	68
Mean	55.79
Std Dev	7.975

ampl



B0L103S, U15-ch53

calib_packv5_040323_1717.root, FC#2, Port C3

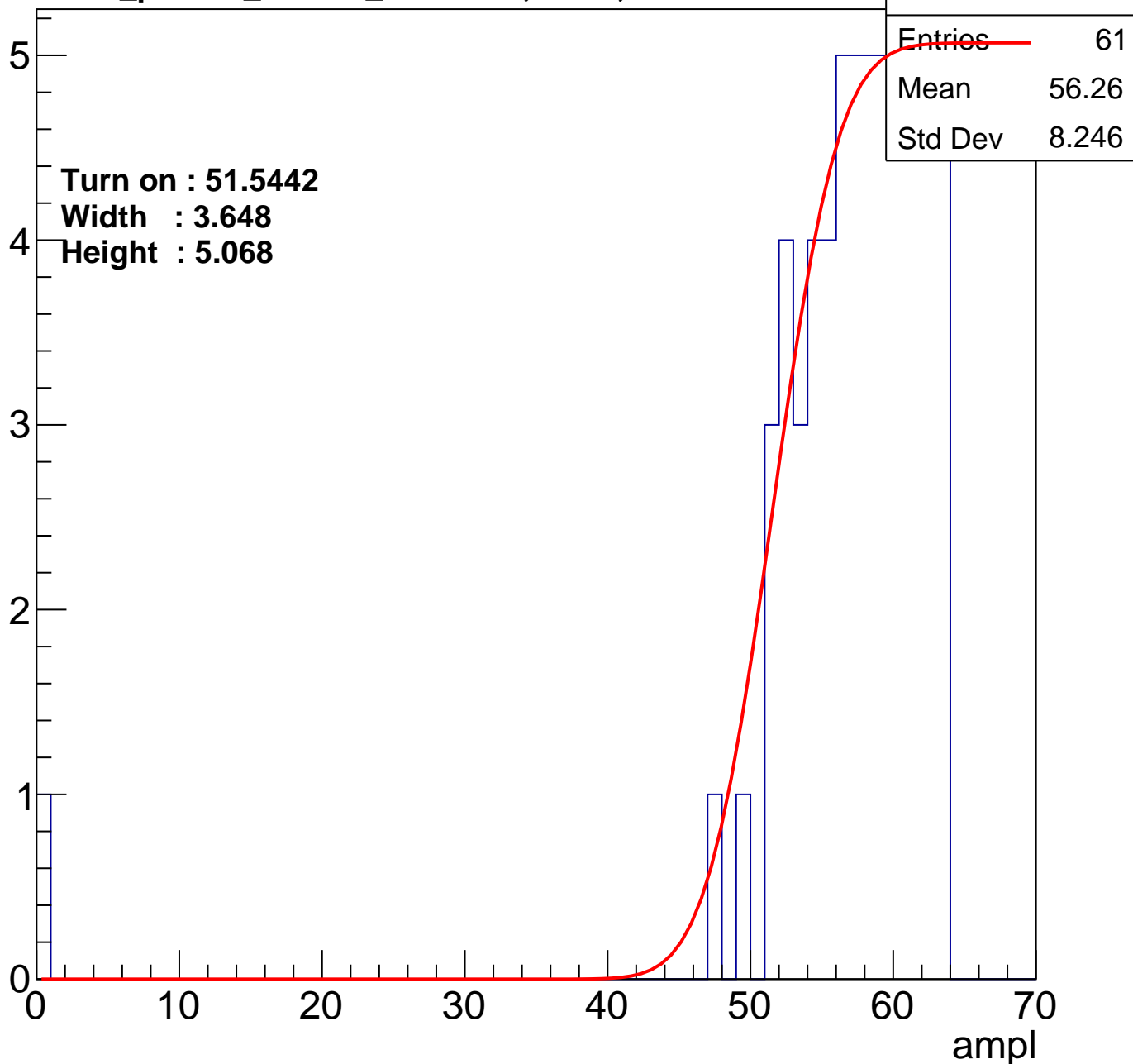
Entry

5
4
3
2
1
0

Turn on : 51.5442
Width : 3.648
Height : 5.068

Entries	61
Mean	56.26
Std Dev	8.246

ampl



B0L103S, U15-ch54

calib_packv5_040323_1717.root, FC#2, Port C3

Entry

5

4

3

2

1

0

Turn on : 51.8304

Width : 4.827

Height : 5.396

Entries	68
Mean	55.54
Std Dev	8.2

ampl

0

10

20

30

40

50

60

70

B0L103S, U15-ch55

calib_packv5_040323_1717.root, FC#2, Port C3

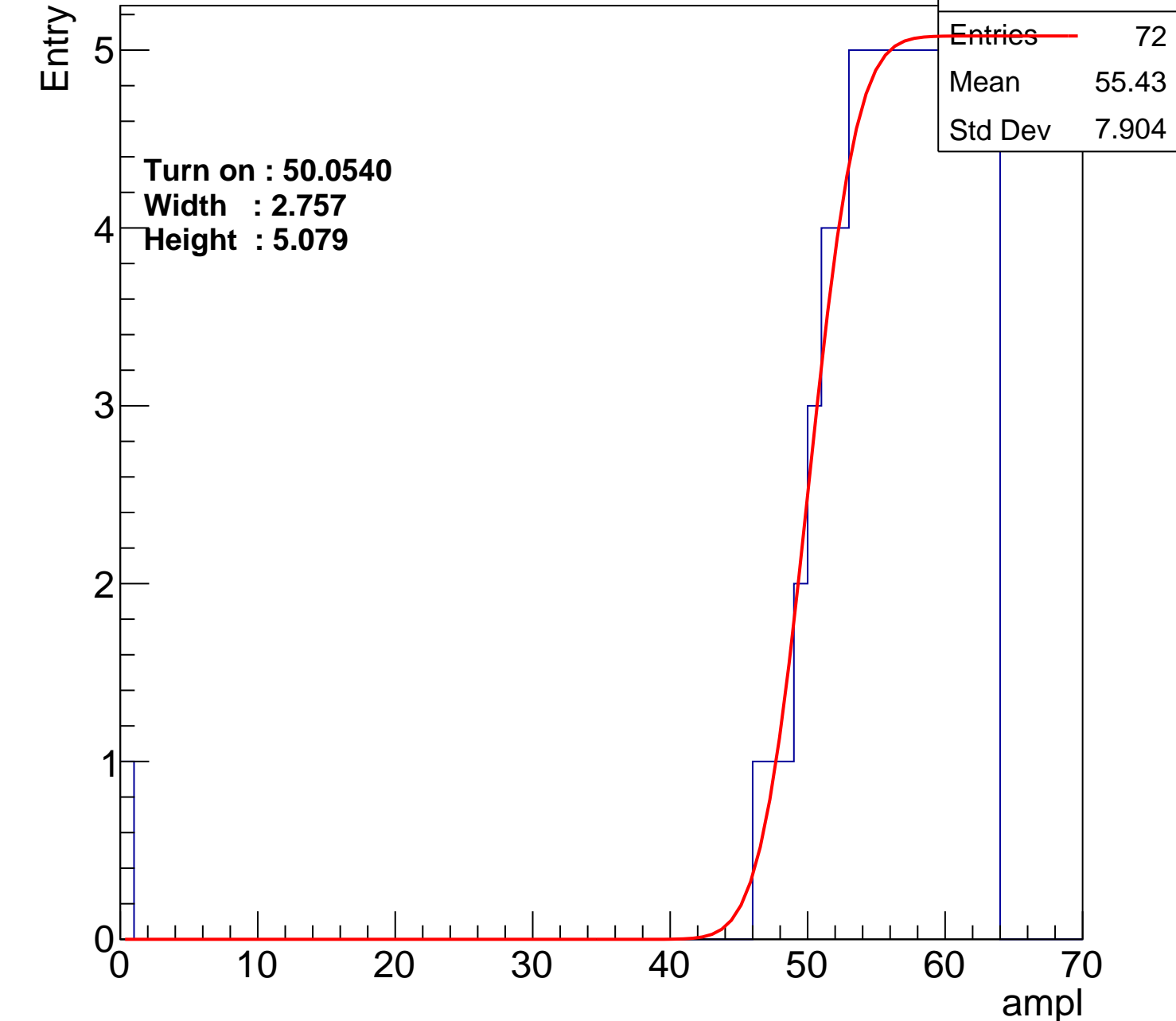
Entry

5
4
3
2
1
0

Turn on : 50.0540
Width : 2.757
Height : 5.079

Entries	72
Mean	55.43
Std Dev	7.904

ampl



B0L103S, U15-ch56

calib_packv5_040323_1717.root, FC#2, Port C3

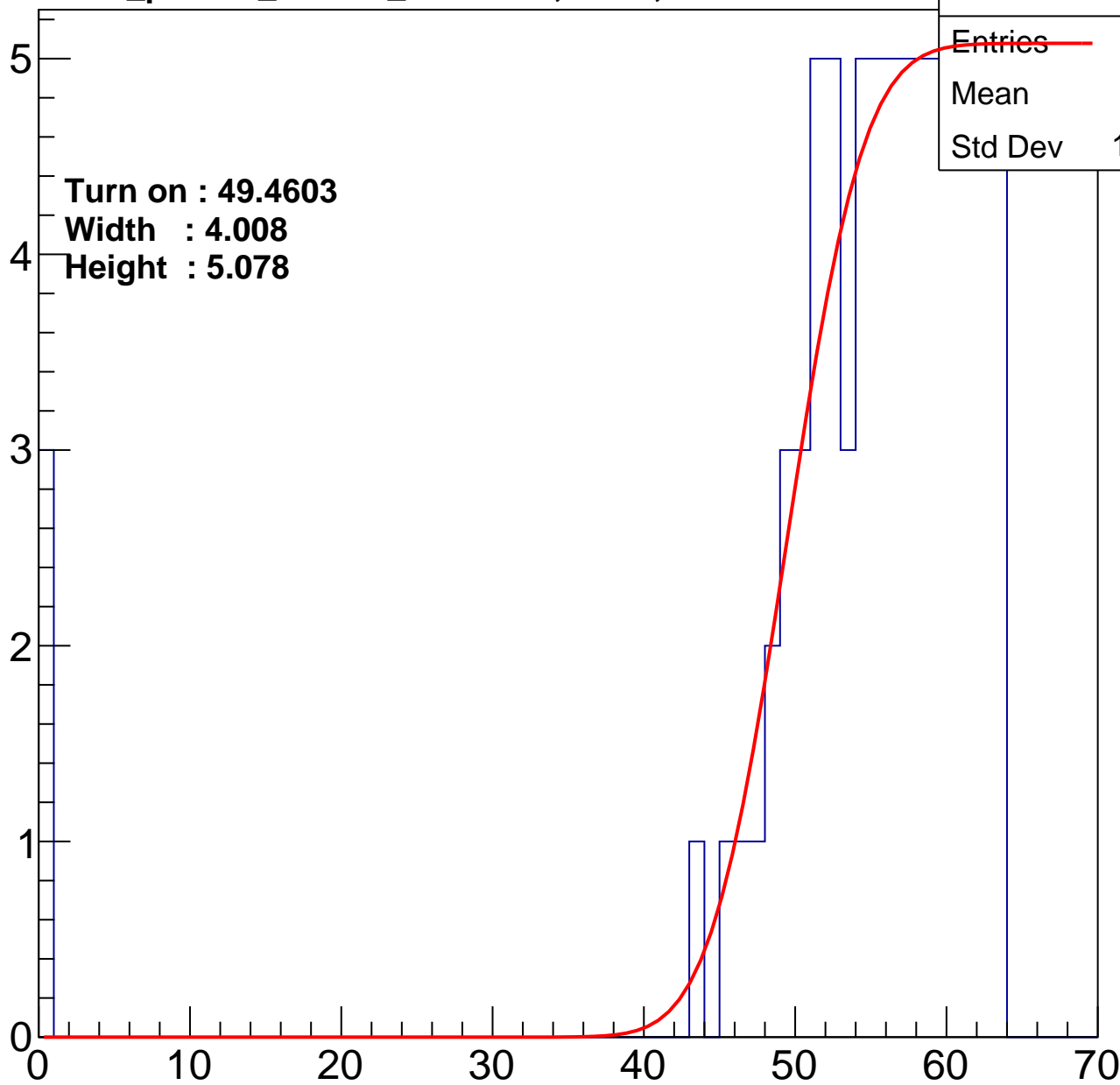
Entry

5
4
3
2
1
0

Turn on : 49.4603
Width : 4.008
Height : 5.078

Entries	78
Mean	53.5
Std Dev	11.73

ampl



B0L103S, U15-ch57

calib_packv5_040323_1717.root, FC#2, Port C3

Entry

5

4

3

2

1

0

Turn on : 50.8615

Width : 4.866

Height : 5.218

Entries	67
Mean	55
Std Dev	10.51

ampl

0

10

20

30

40

50

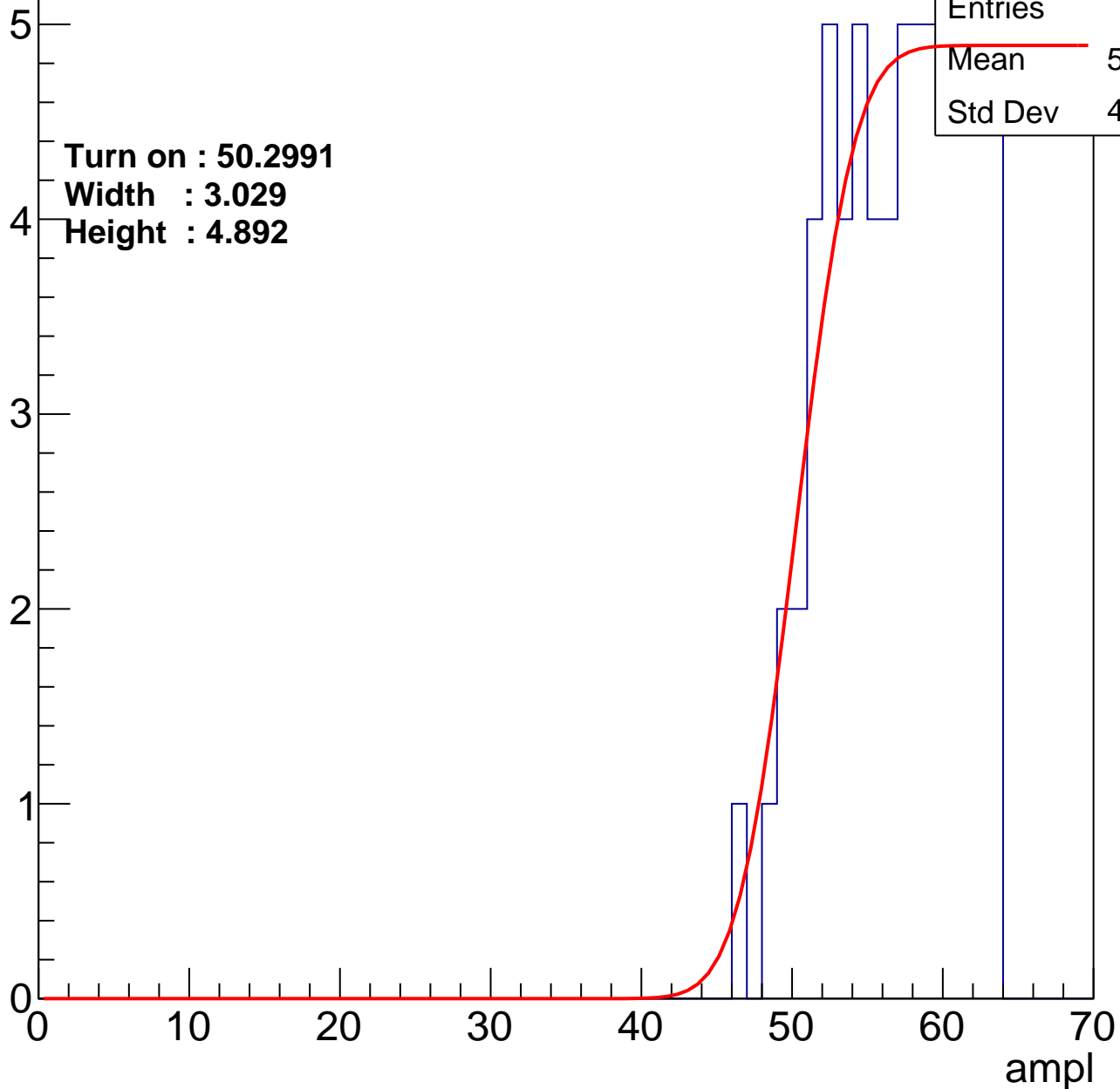
60

70

B0L103S, U15-ch58

calib_packv5_040323_1717.root, FC#2, Port C3

Entry



B0L103S, U15-ch59

calib_packv5_040323_1717.root, FC#2, Port C3

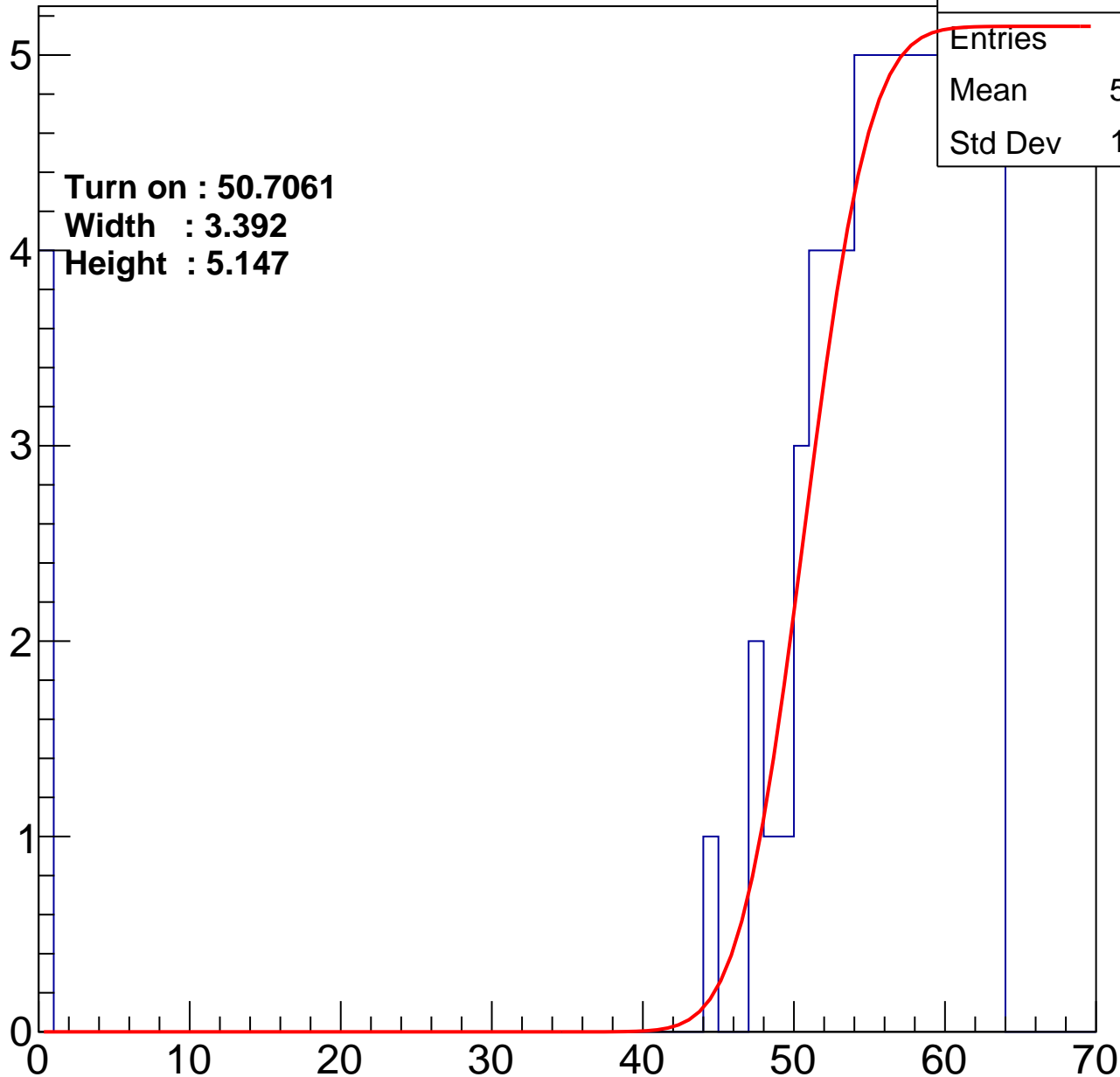
Entry

5
4
3
2
1
0

Turn on : 50.7061
Width : 3.392
Height : 5.147

Entries	74
Mean	53.16
Std Dev	13.46

ampl



B0L103S, U15-ch60

calib_packv5_040323_1717.root, FC#2, Port C3

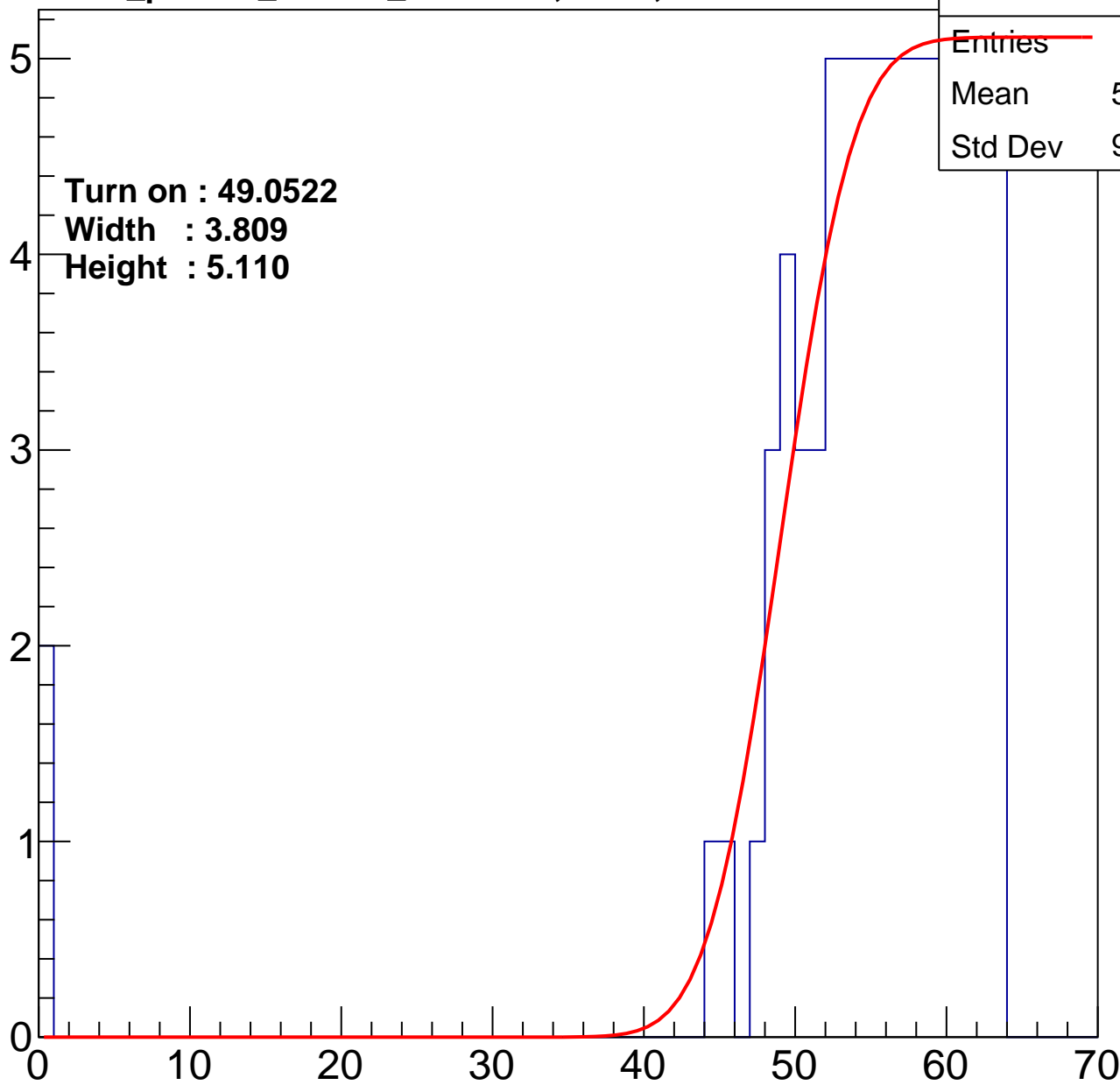
Entry

5
4
3
2
1
0

Turn on : 49.0522
Width : 3.809
Height : 5.110

Entries	78
Mean	54.22
Std Dev	9.994

ampl



B0L103S, U15-ch61

calib_packv5_040323_1717.root, FC#2, Port C3

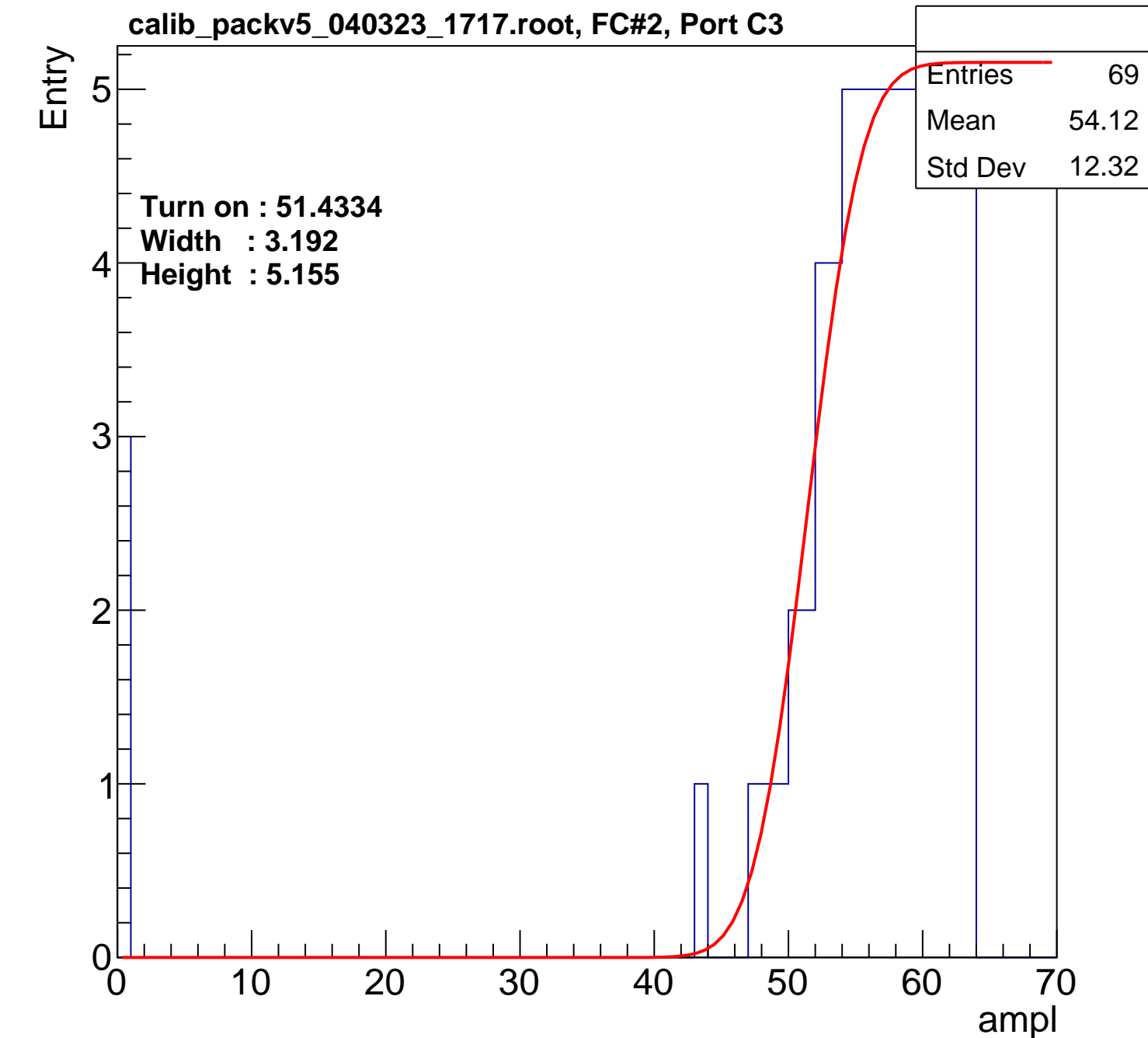
Entry

5
4
3
2
1
0

Turn on : 51.4334
Width : 3.192
Height : 5.155

Entries	69
Mean	54.12
Std Dev	12.32

ampl



B0L103S, U15-ch62

calib_packv5_040323_1717.root, FC#2, Port C3

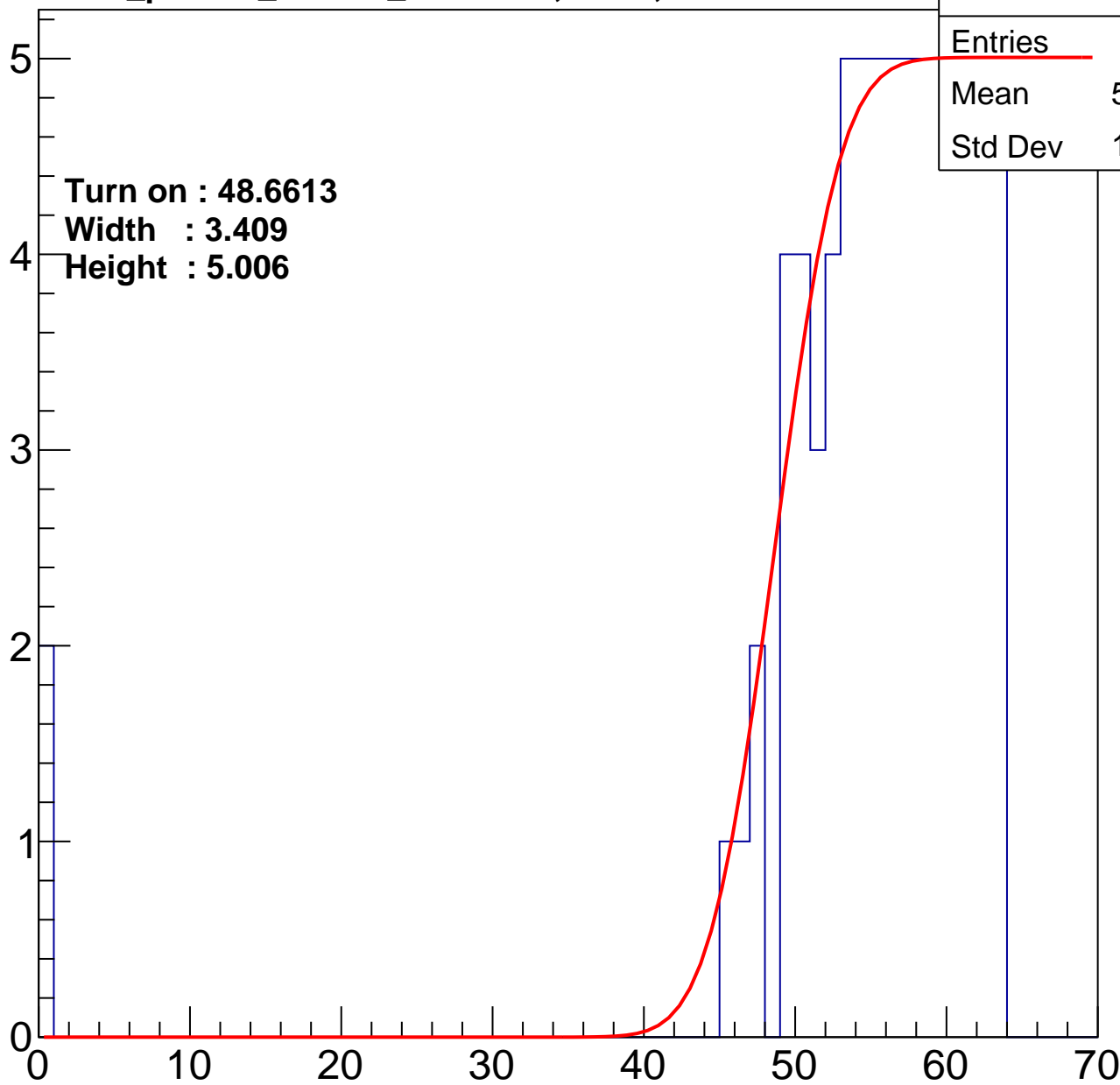
Entry

5
4
3
2
1
0

Turn on : 48.6613
Width : 3.409
Height : 5.006

Entries	76
Mean	54.37
Std Dev	10.07

ampl



B0L103S, U15-ch63

calib_packv5_040323_1717.root, FC#2, Port C3

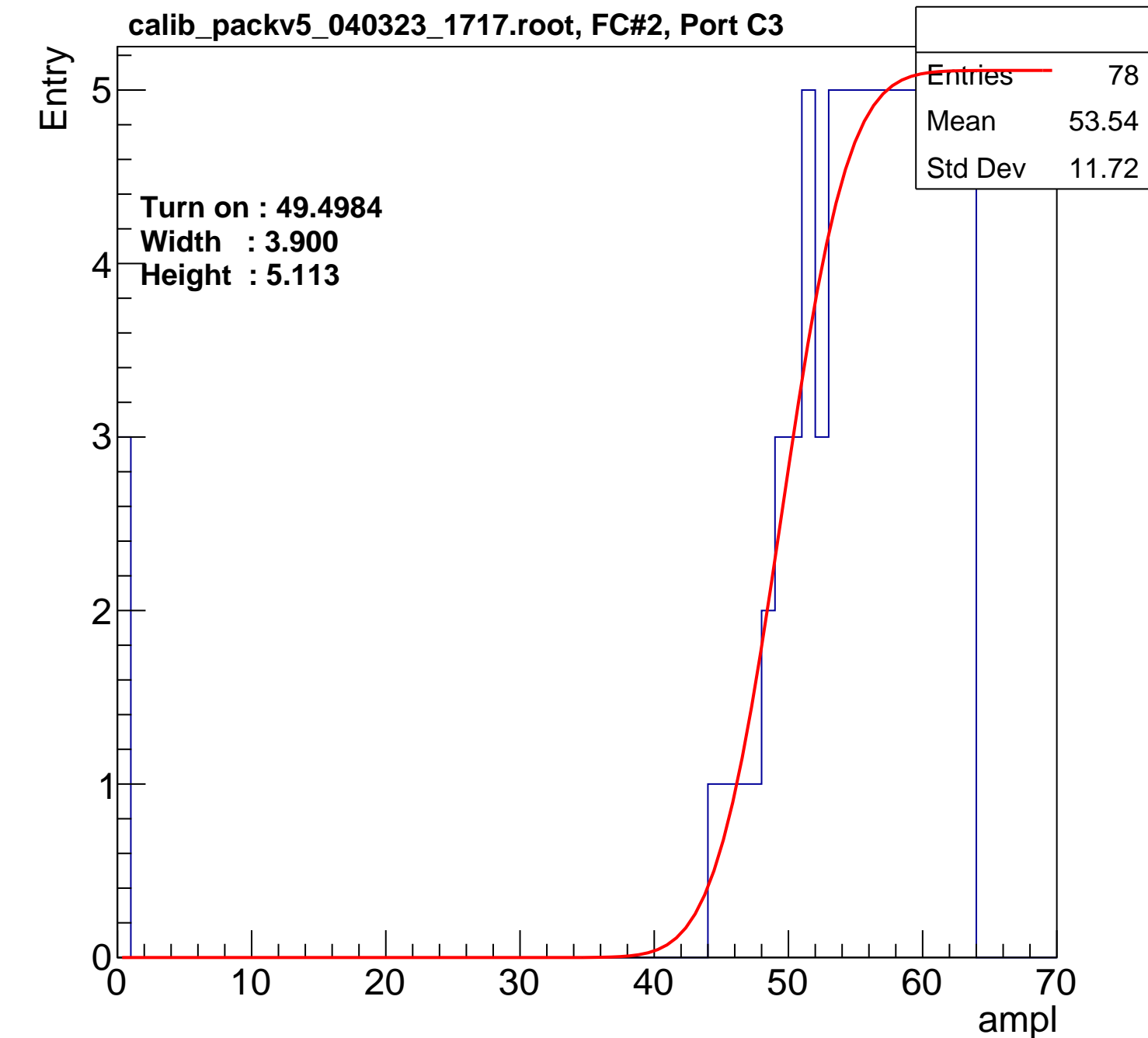
Entry

5
4
3
2
1
0

Turn on : 49.4984
Width : 3.900
Height : 5.113

Entries	78
Mean	53.54
Std Dev	11.72

ampl



B0L103S, U15-ch64

calib_packv5_040323_1717.root, FC#2, Port C3

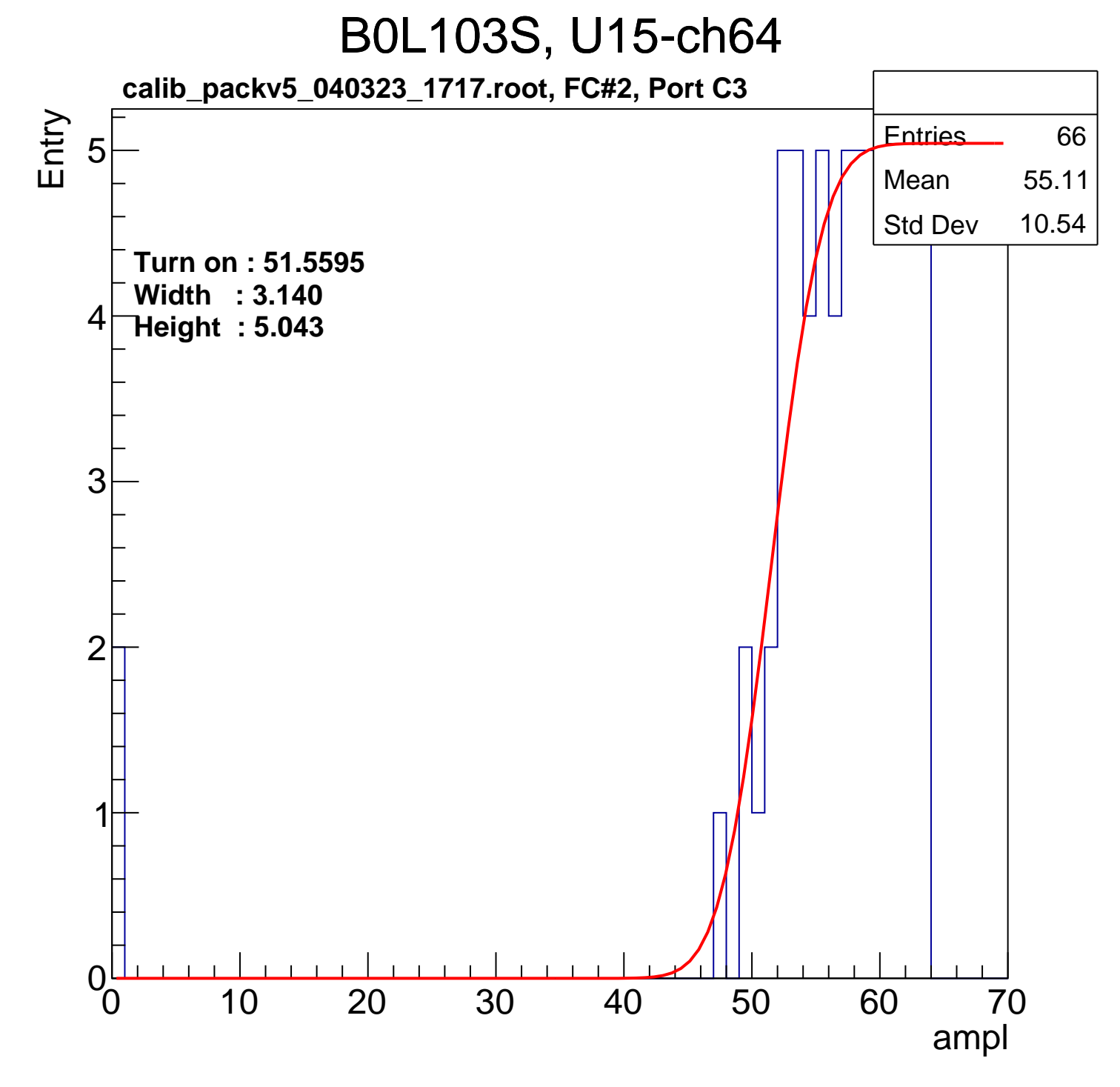
Entry

5
4
3
2
1
0

Turn on : 51.5595
Width : 3.140
Height : 5.043

Entries	66
Mean	55.11
Std Dev	10.54

ampl



B0L103S, U15-ch65

calib_packv5_040323_1717.root, FC#2, Port C3

Entry

5

4

3

2

1

0

Turn on : 52.6713

Width : 3.145

Height : 5.215

Entries	61
Mean	57.15
Std Dev	3.966

ampl

0

10

20

30

40

50

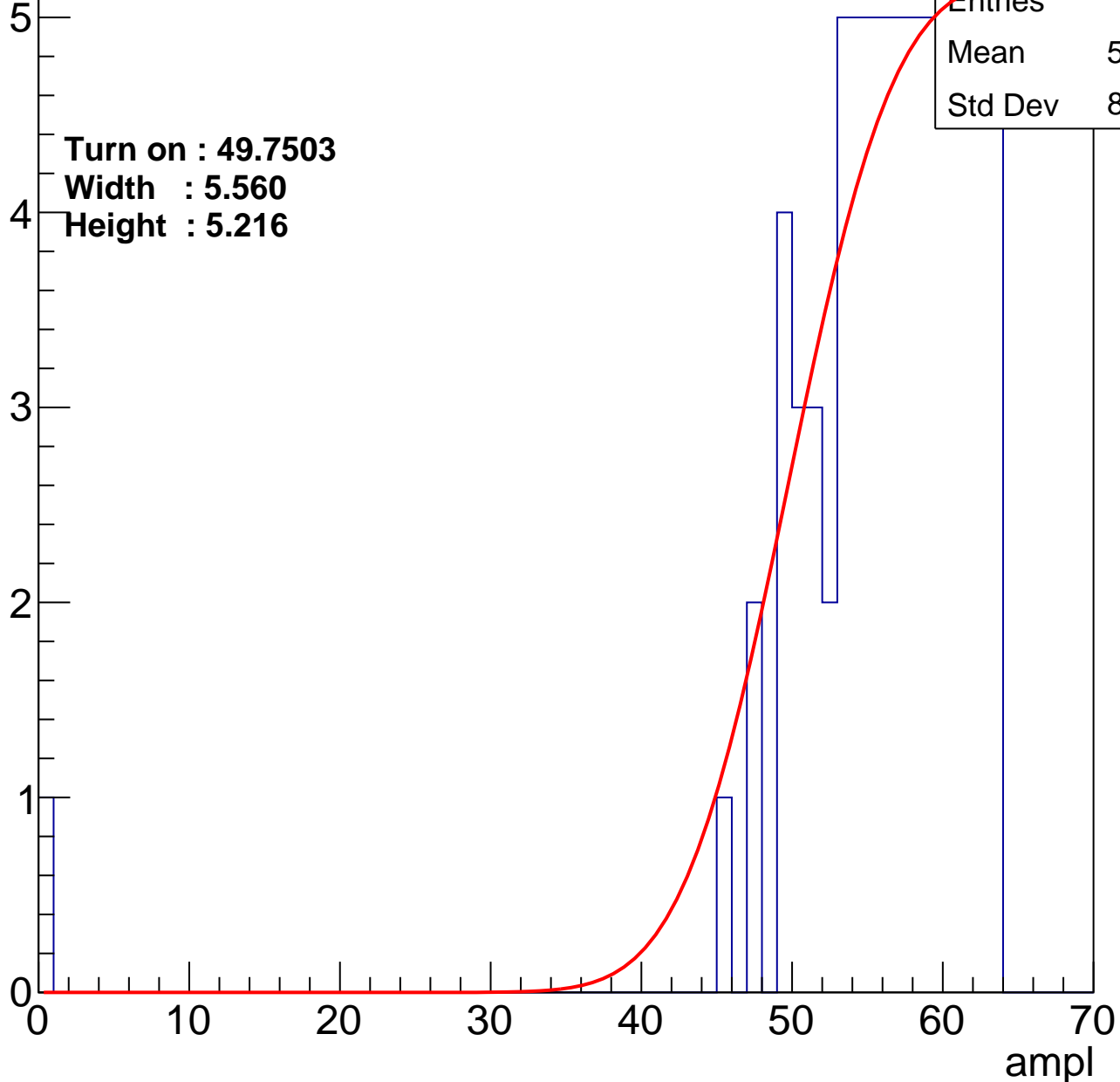
60

70

B0L103S, U15-ch66

calib_packv5_040323_1717.root, FC#2, Port C3

Entry



B0L103S, U15-ch67

calib_packv5_040323_1717.root, FC#2, Port C3

Entry

5

4

3

2

1

0

0

1

2

3

4

5

6

7

8

9

10

11

12

13

14

15

16

17

18

19

20

21

22

23

24

25

26

27

28

Turn on : 52.6366

Width : 4.052

Height : 5.256

Entries	63
Mean	56.81
Std Dev	4.231

ampl

B0L103S, U15-ch68

calib_packv5_040323_1717.root, FC#2, Port C3

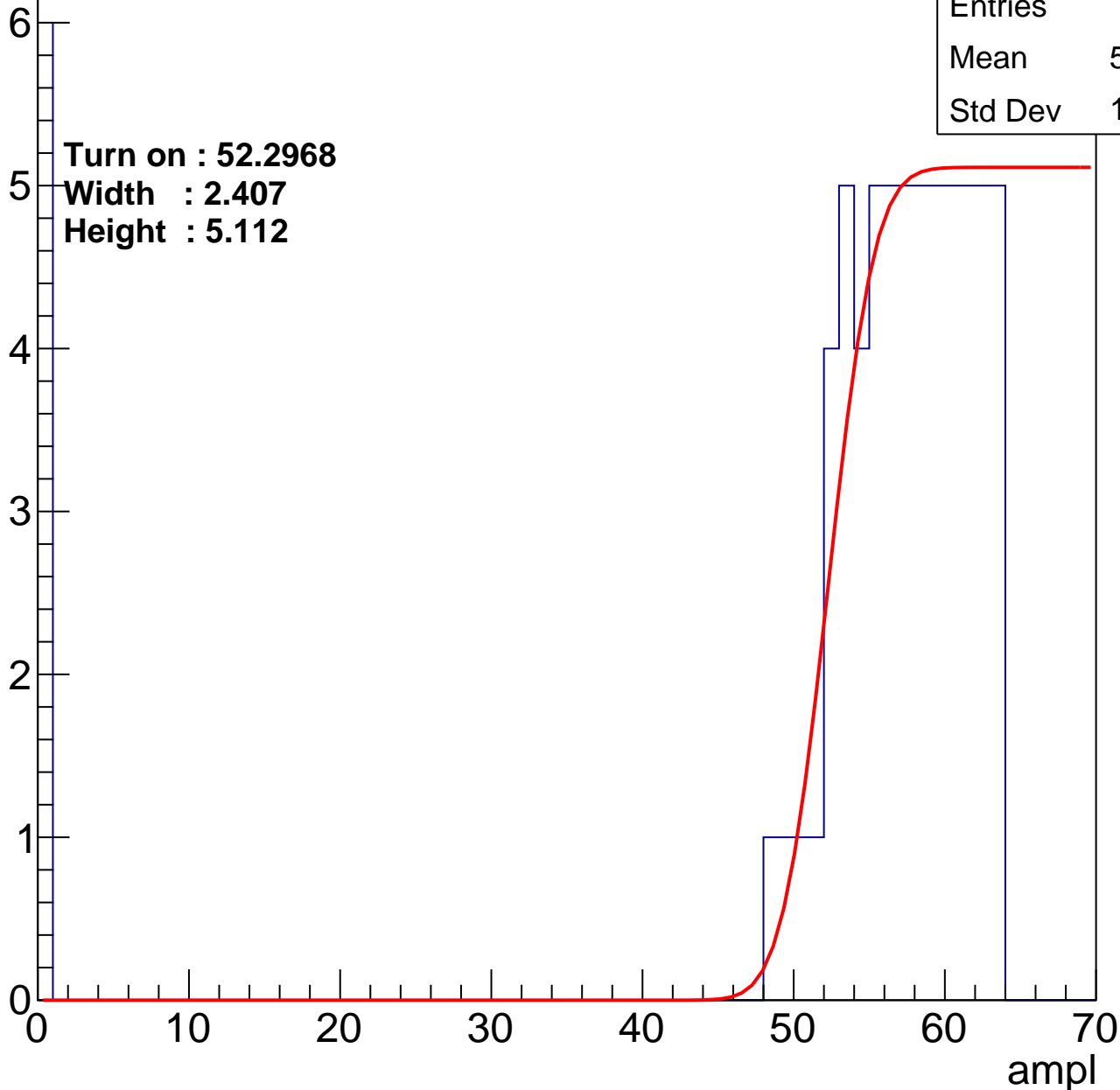
Entry

Entries	68
Mean	52.09
Std Dev	16.62

Turn on : 52.2968

Width : 2.407

Height : 5.112



B0L103S, U15-ch69

calib_packv5_040323_1717.root, FC#2, Port C3

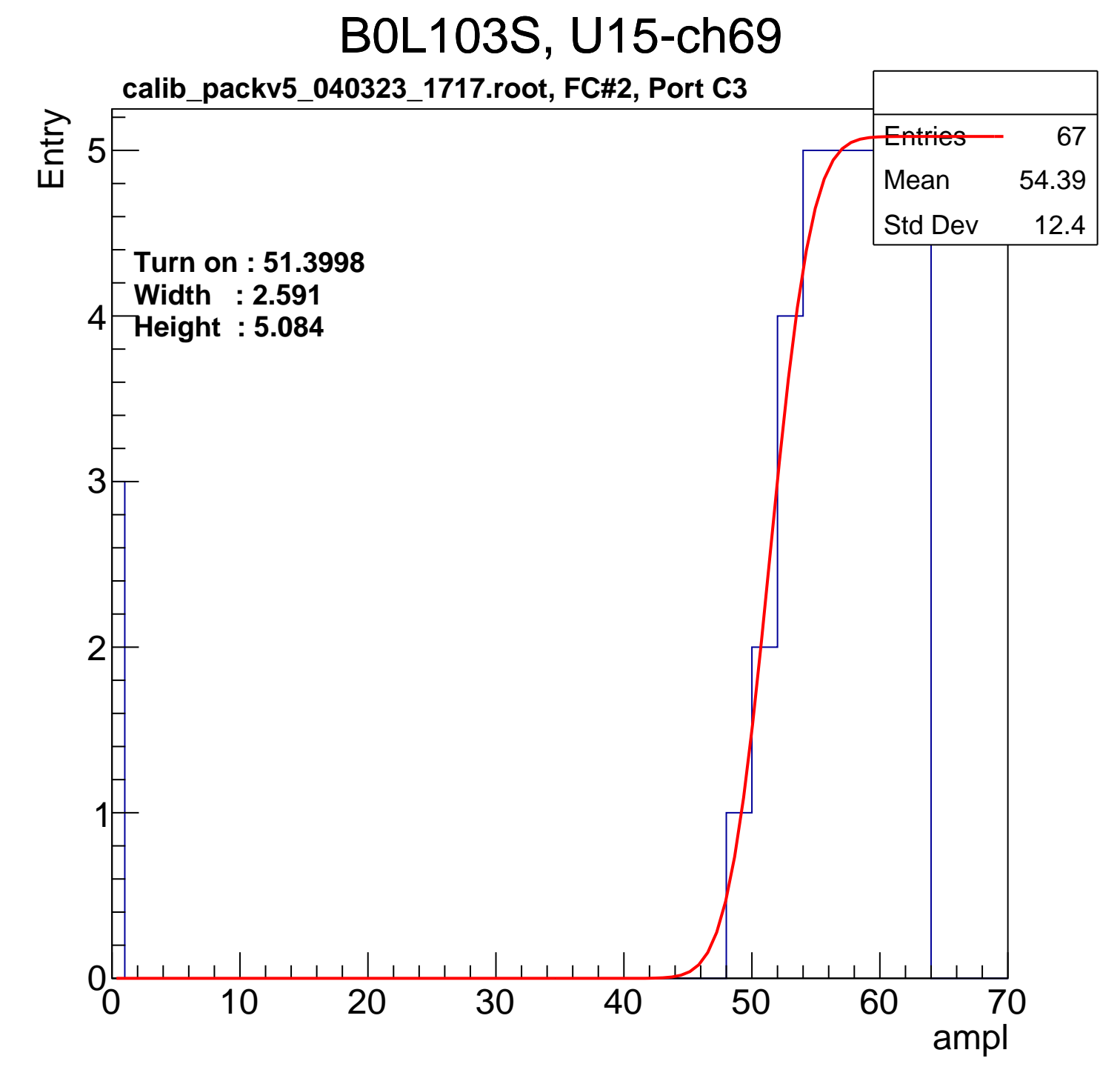
Entry

5
4
3
2
1
0

Turn on : 51.3998
Width : 2.591
Height : 5.084

Entries	67
Mean	54.39
Std Dev	12.4

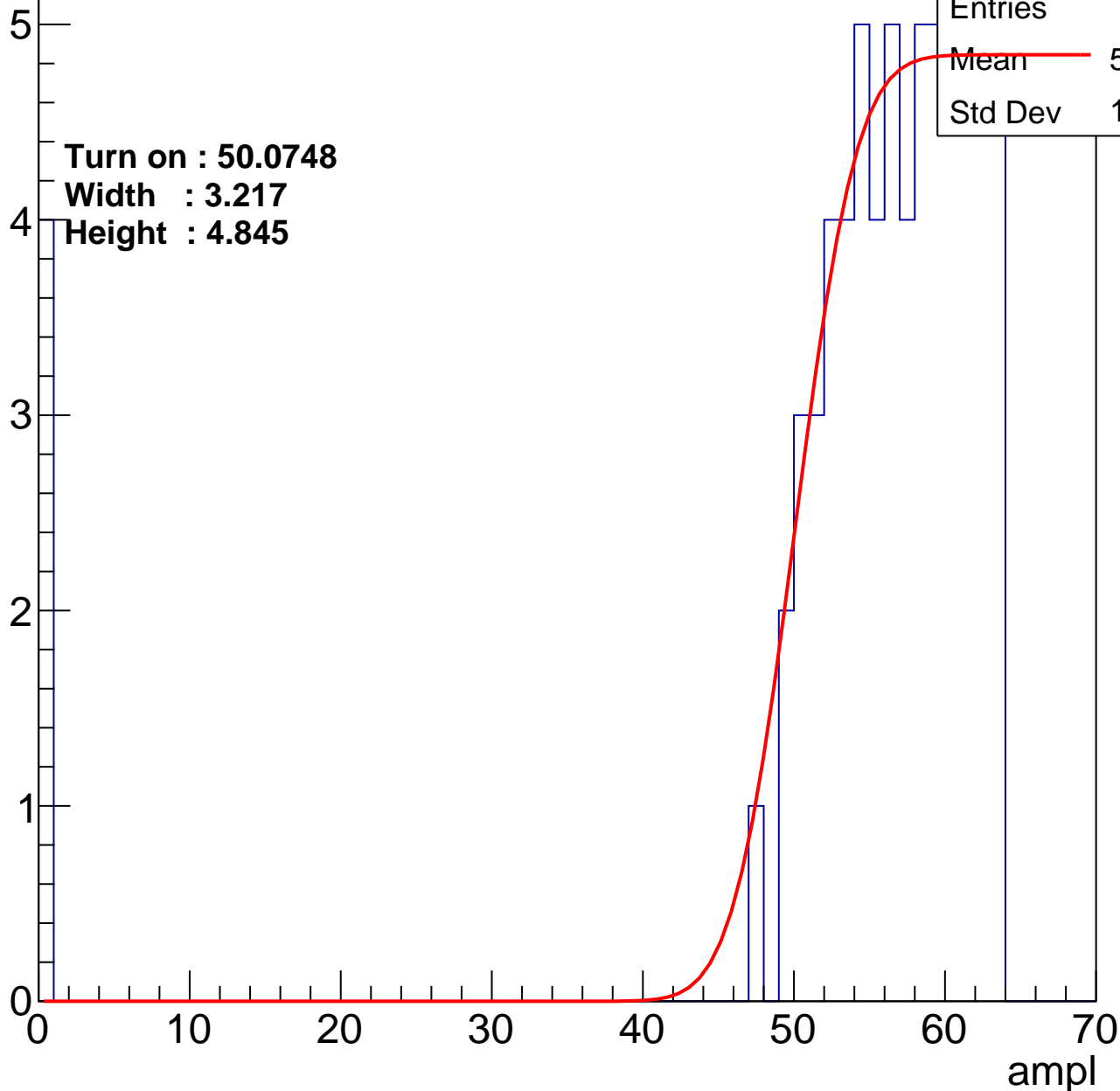
ampl



B0L103S, U15-ch70

calib_packv5_040323_1717.root, FC#2, Port C3

Entry



B0L103S, U15-ch71

calib_packv5_040323_1717.root, FC#2, Port C3

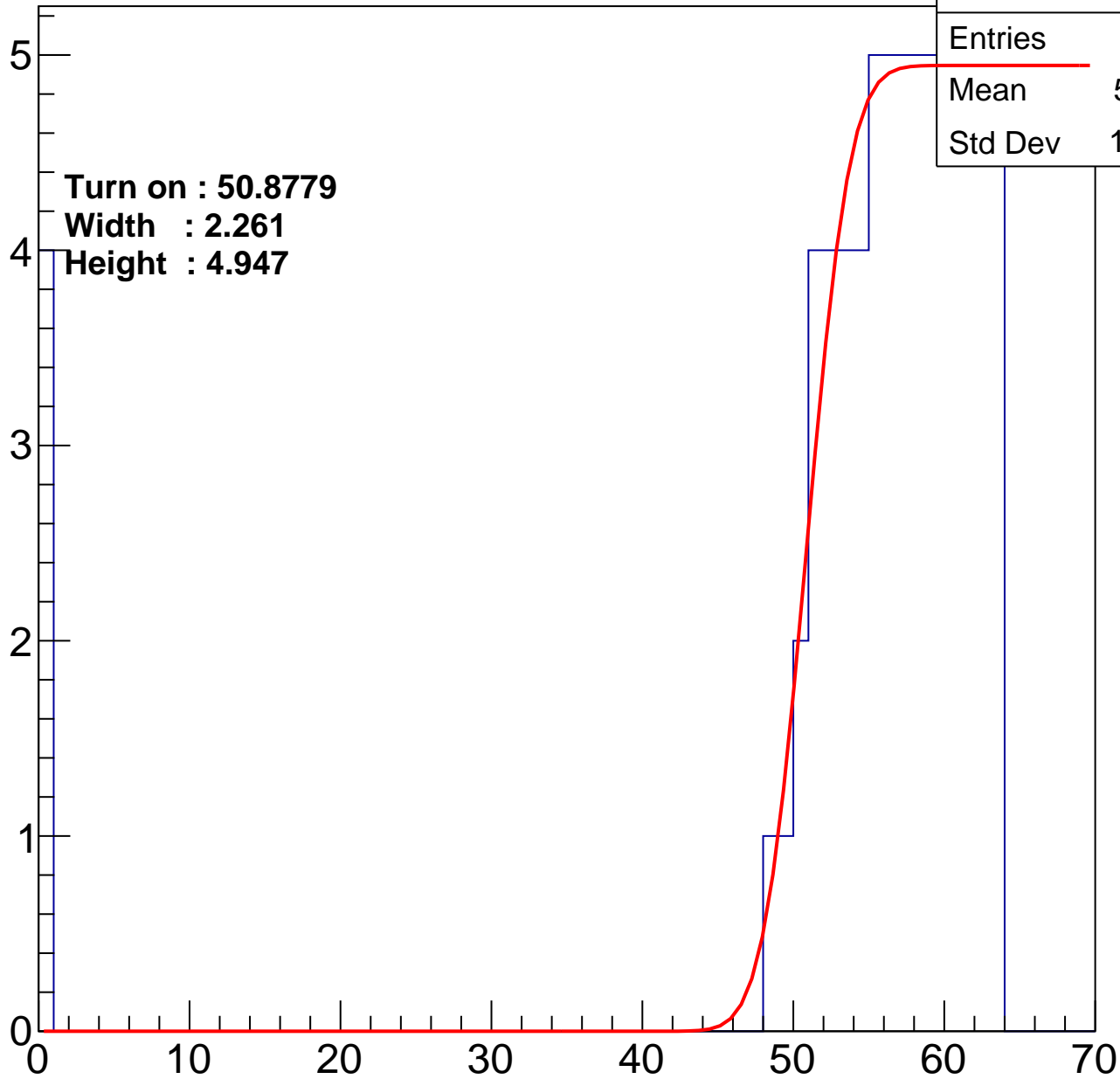
Entry

5
4
3
2
1
0

Turn on : 50.8779
Width : 2.261
Height : 4.947

Entries	69
Mean	53.51
Std Dev	13.84

ampl



B0L103S, U15-ch72

calib_packv5_040323_1717.root, FC#2, Port C3

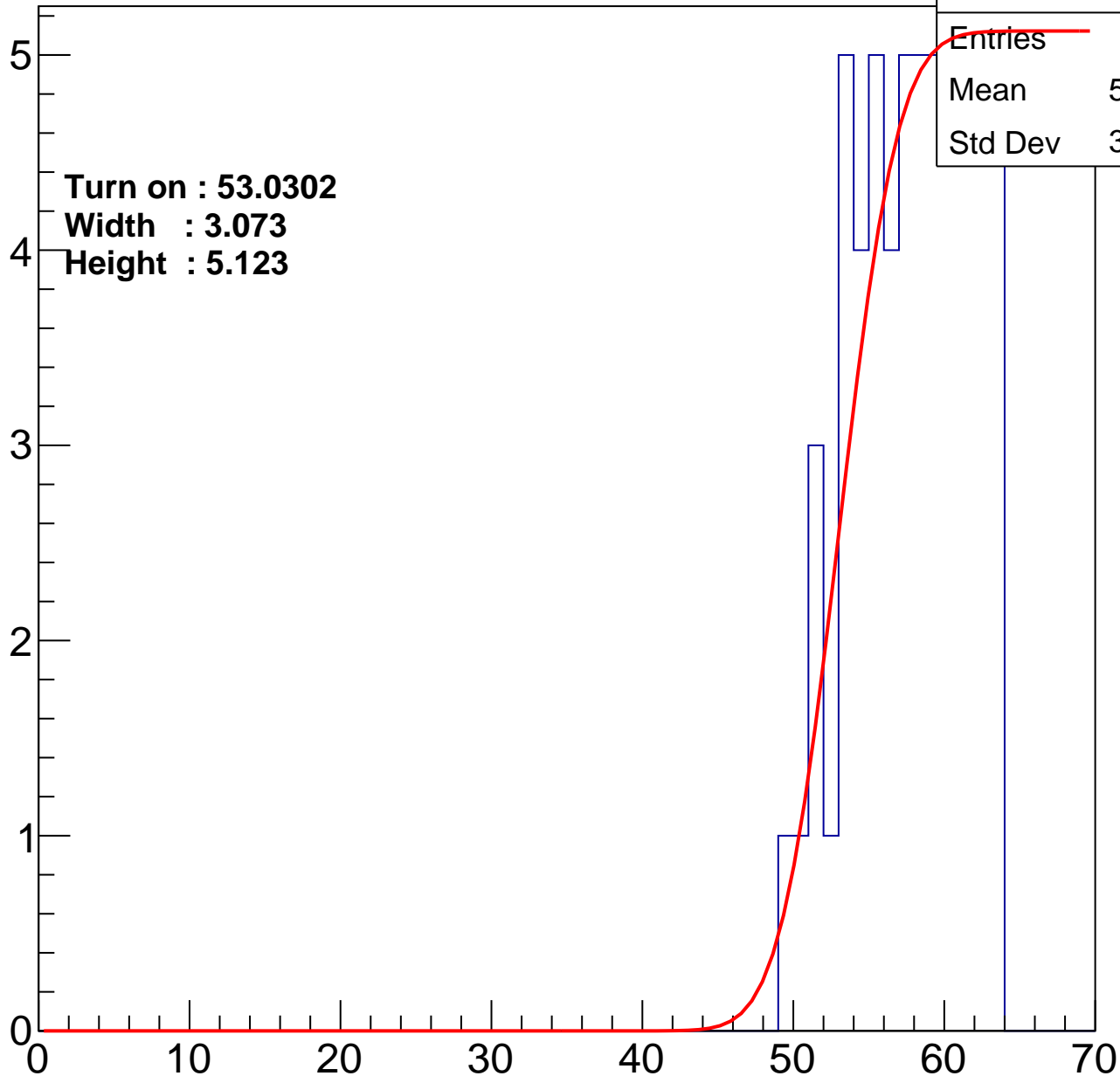
Entry

5
4
3
2
1
0

Turn on : 53.0302
Width : 3.073
Height : 5.123

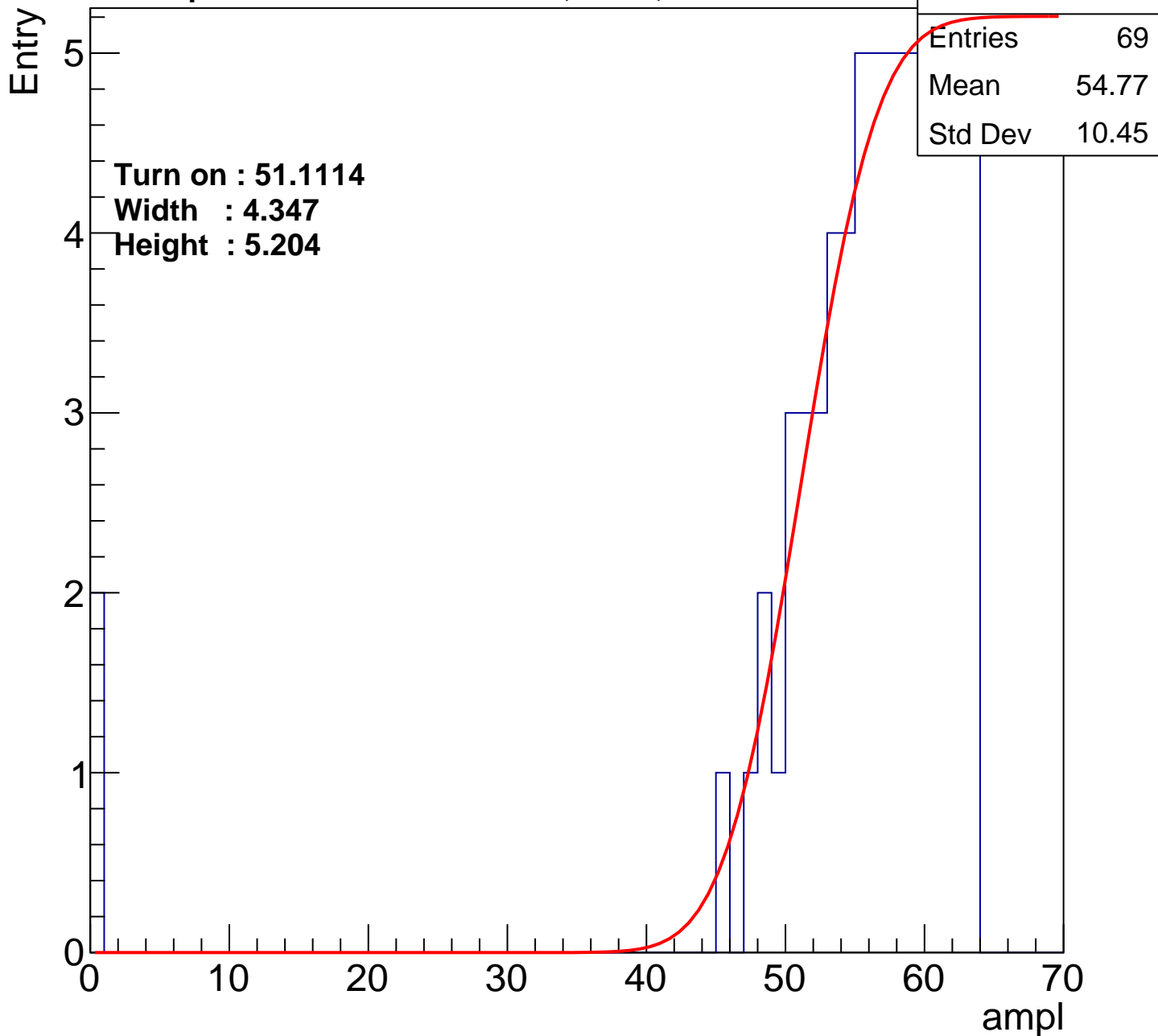
Entries	59
Mean	57.36
Std Dev	3.759

ampl



B0L103S, U15-ch73

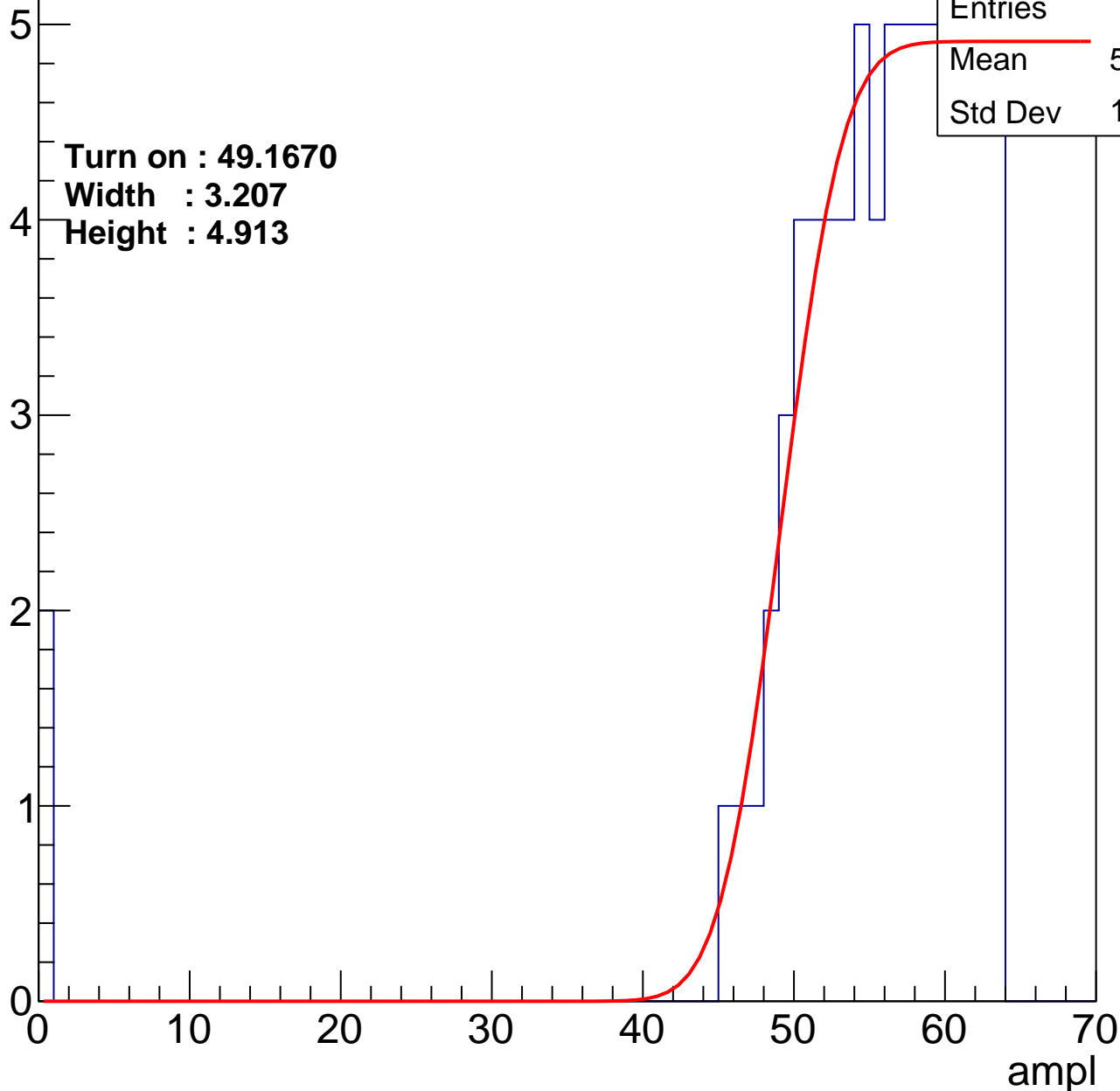
calib_packv5_040323_1717.root, FC#2, Port C3



B0L103S, U15-ch74

calib_packv5_040323_1717.root, FC#2, Port C3

Entry



B0L103S, U15-ch75

calib_packv5_040323_1717.root, FC#2, Port C3

Entry

5

4

3

2

1

0

Turn on : 50.7875

Width : 2.488

Height : 5.060

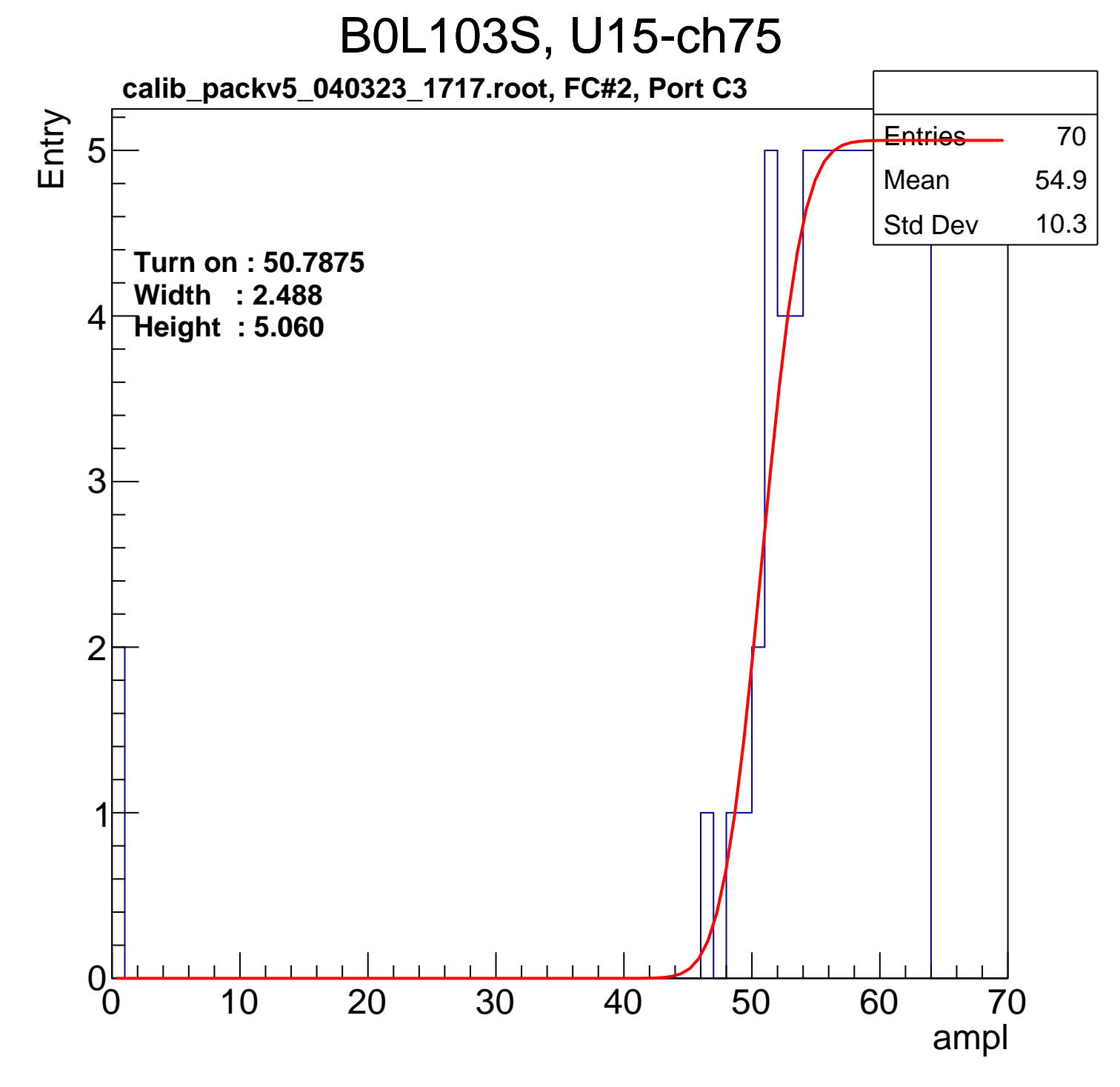
Entries 70

Mean 54.9

Std Dev 10.3

ampl

0 10 20 30 40 50 60 70



B0L103S, U15-ch76

calib_packv5_040323_1717.root, FC#2, Port C3

Entry

5

4

3

2

1

0

Turn on : 51.0546

Width : 3.705

Height : 5.110

Entries	69
Mean	54.12
Std Dev	12.28

ampl

0

10

20

30

40

50

60

70

B0L103S, U15-ch77

calib_packv5_040323_1717.root, FC#2, Port C3

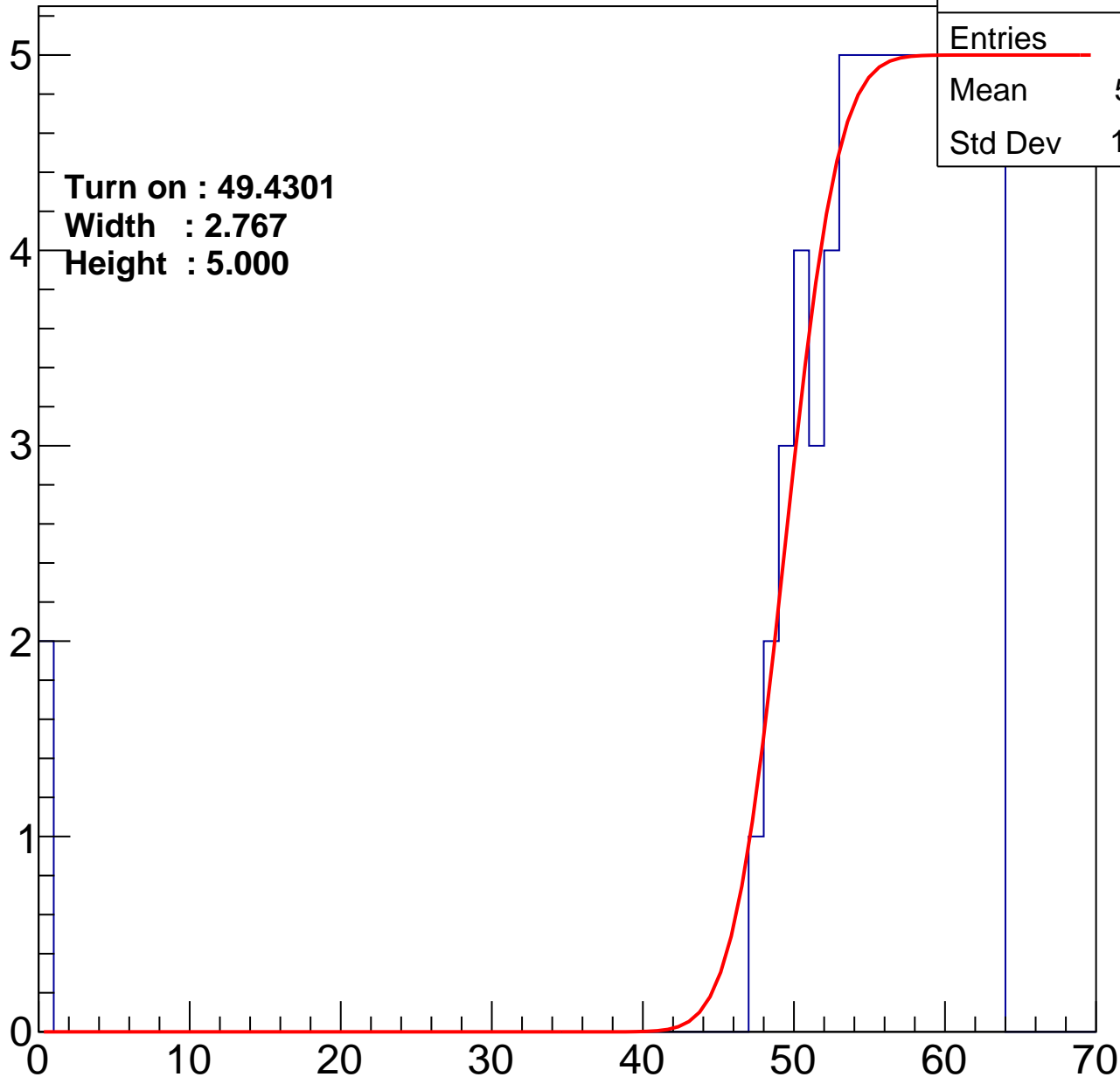
Entry

5
4
3
2
1
0

Turn on : 49.4301
Width : 2.767
Height : 5.000

Entries	74
Mean	54.61
Std Dev	10.09

ampl



B0L103S, U15-ch78

calib_packv5_040323_1717.root, FC#2, Port C3

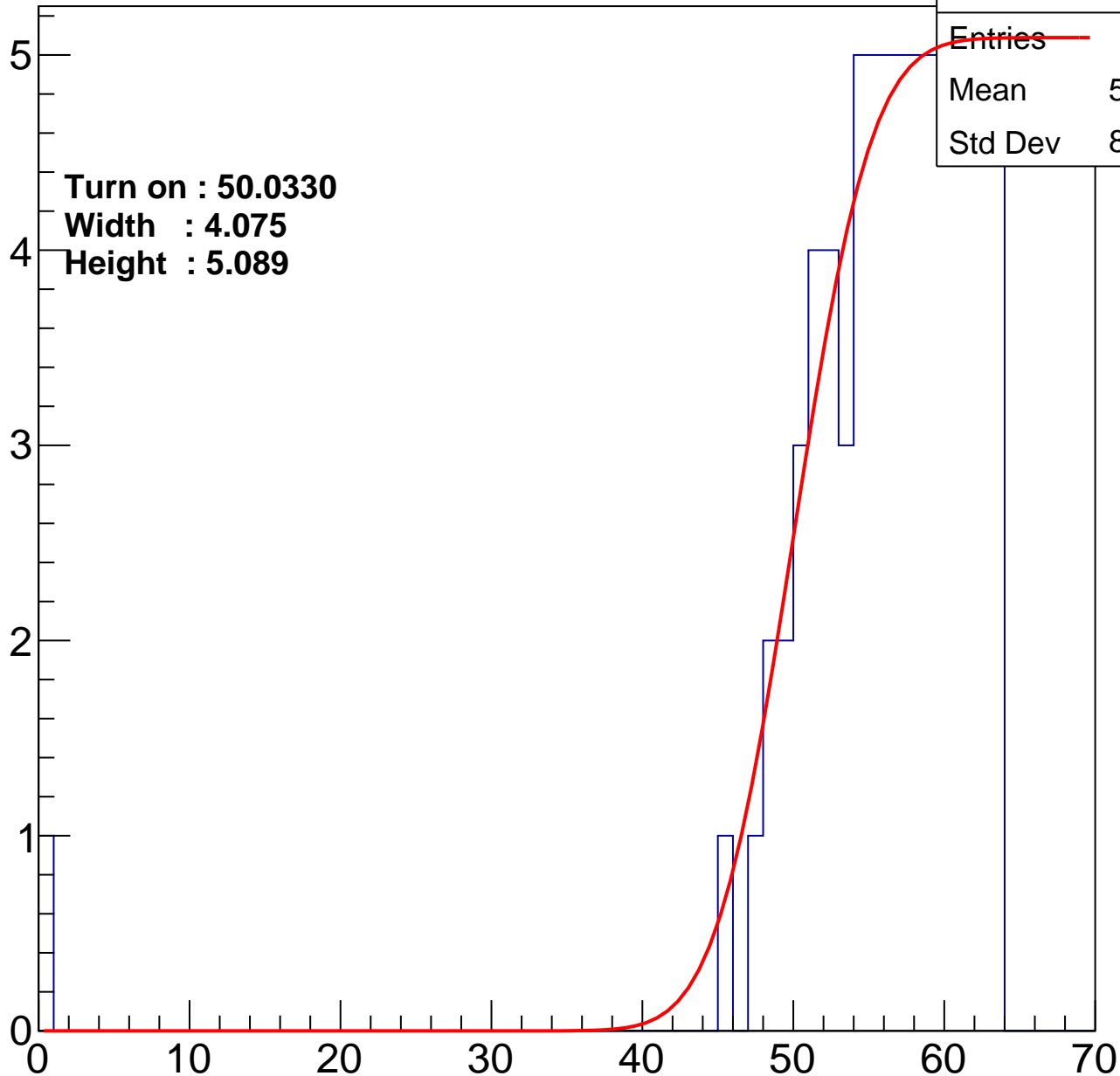
Entry

5
4
3
2
1
0

Turn on : 50.0330
Width : 4.075
Height : 5.089

Entries	71
Mean	55.38
Std Dev	8.015

ampl



B0L103S, U15-ch79

calib_packv5_040323_1717.root, FC#2, Port C3

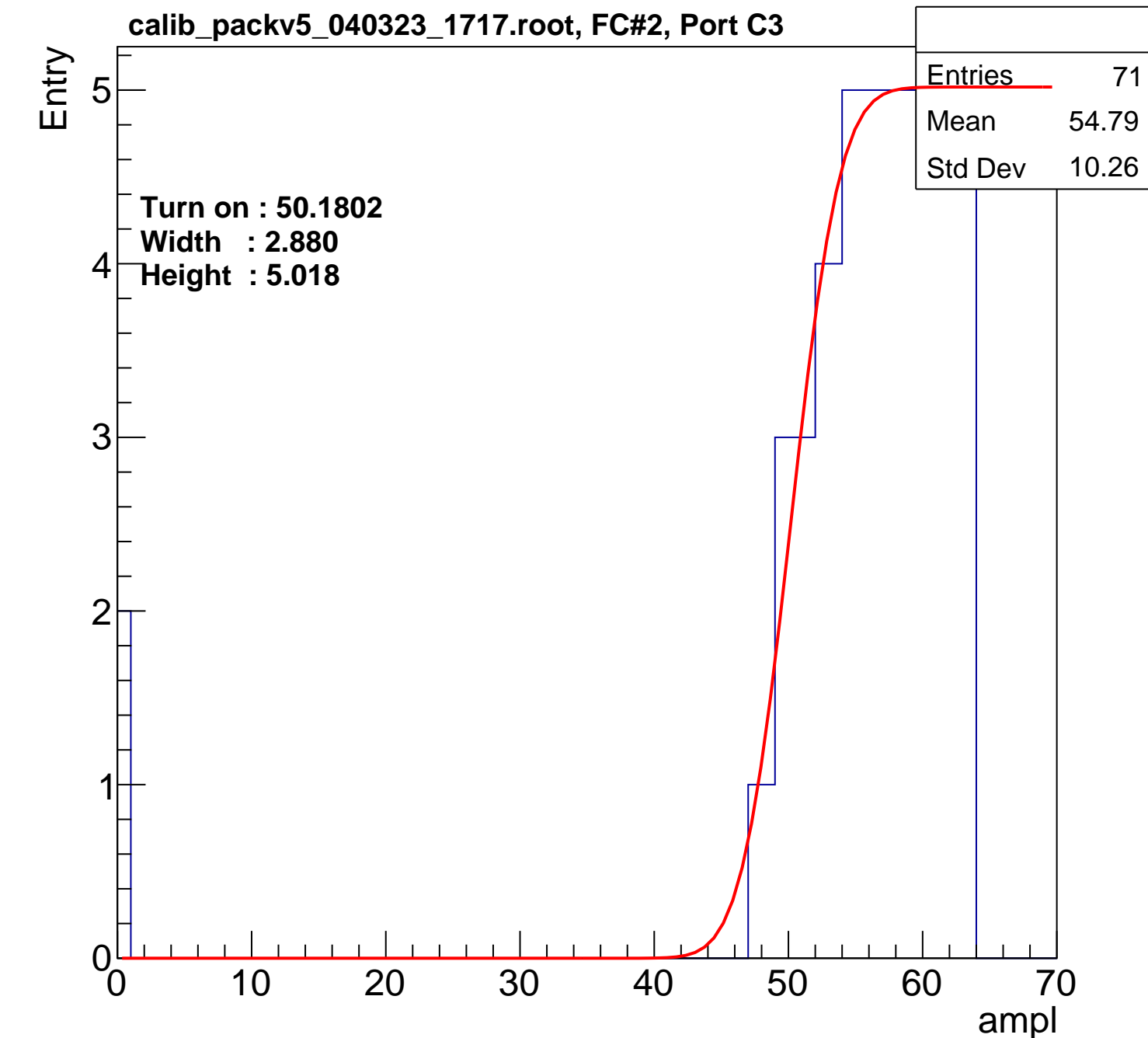
Entry

5
4
3
2
1
0

Turn on : 50.1802
Width : 2.880
Height : 5.018

Entries	71
Mean	54.79
Std Dev	10.26

ampl



B0L103S, U15-ch80

calib_packv5_040323_1717.root, FC#2, Port C3

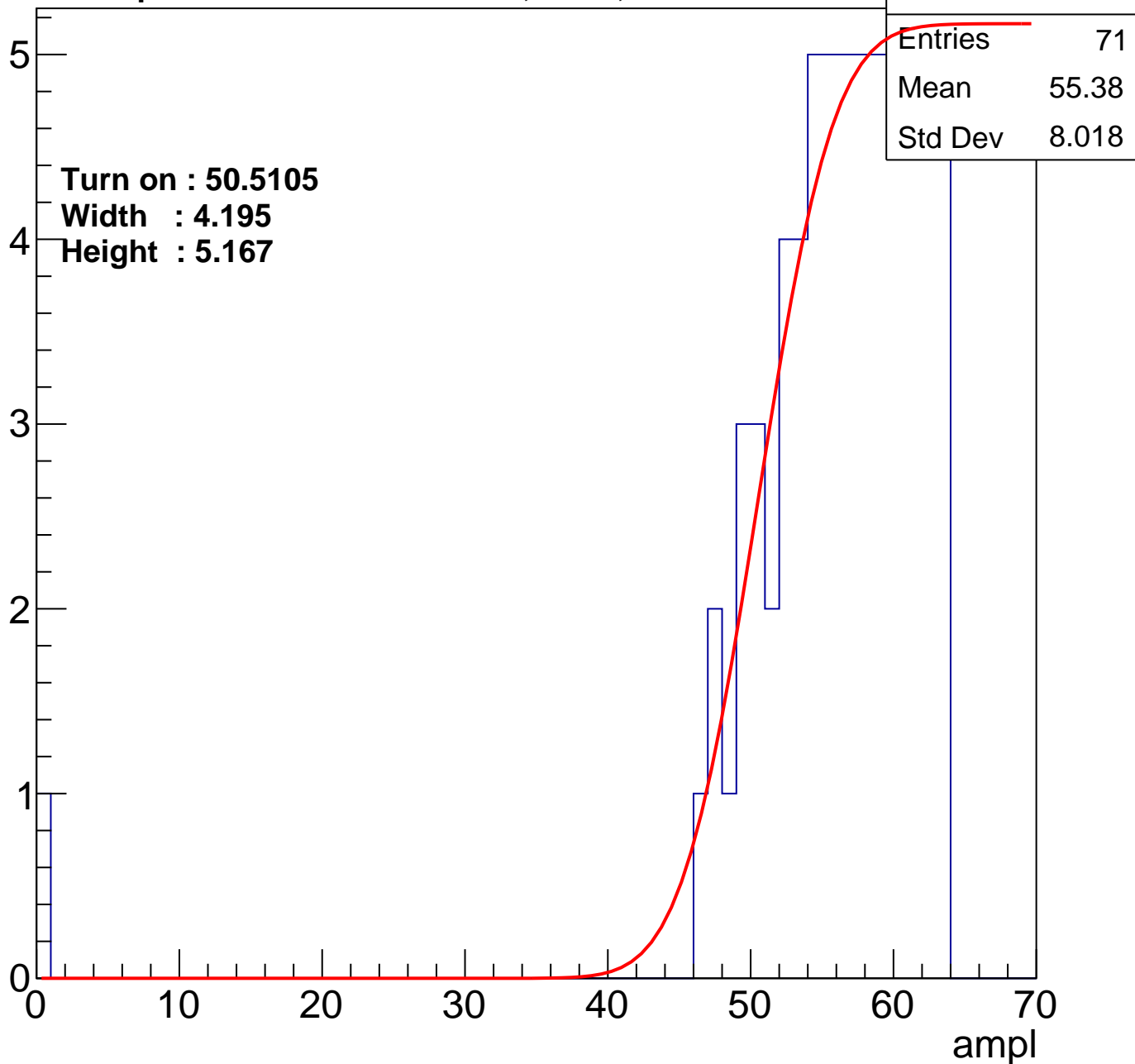
Entry

5
4
3
2
1
0

Turn on : 50.5105
Width : 4.195
Height : 5.167

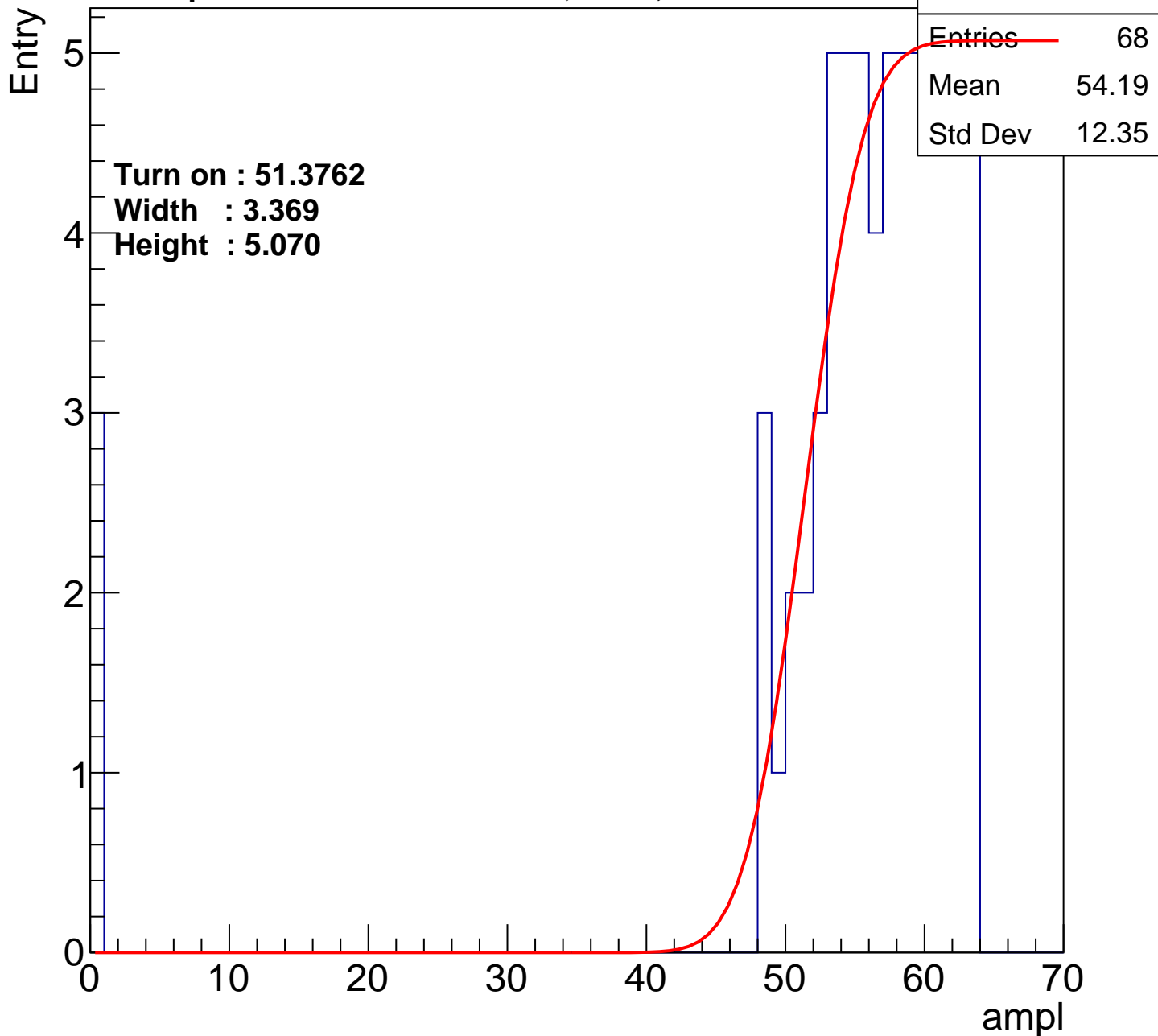
Entries	71
Mean	55.38
Std Dev	8.018

ampl



B0L103S, U15-ch81

calib_packv5_040323_1717.root, FC#2, Port C3



B0L103S, U15-ch82

calib_packv5_040323_1717.root, FC#2, Port C3

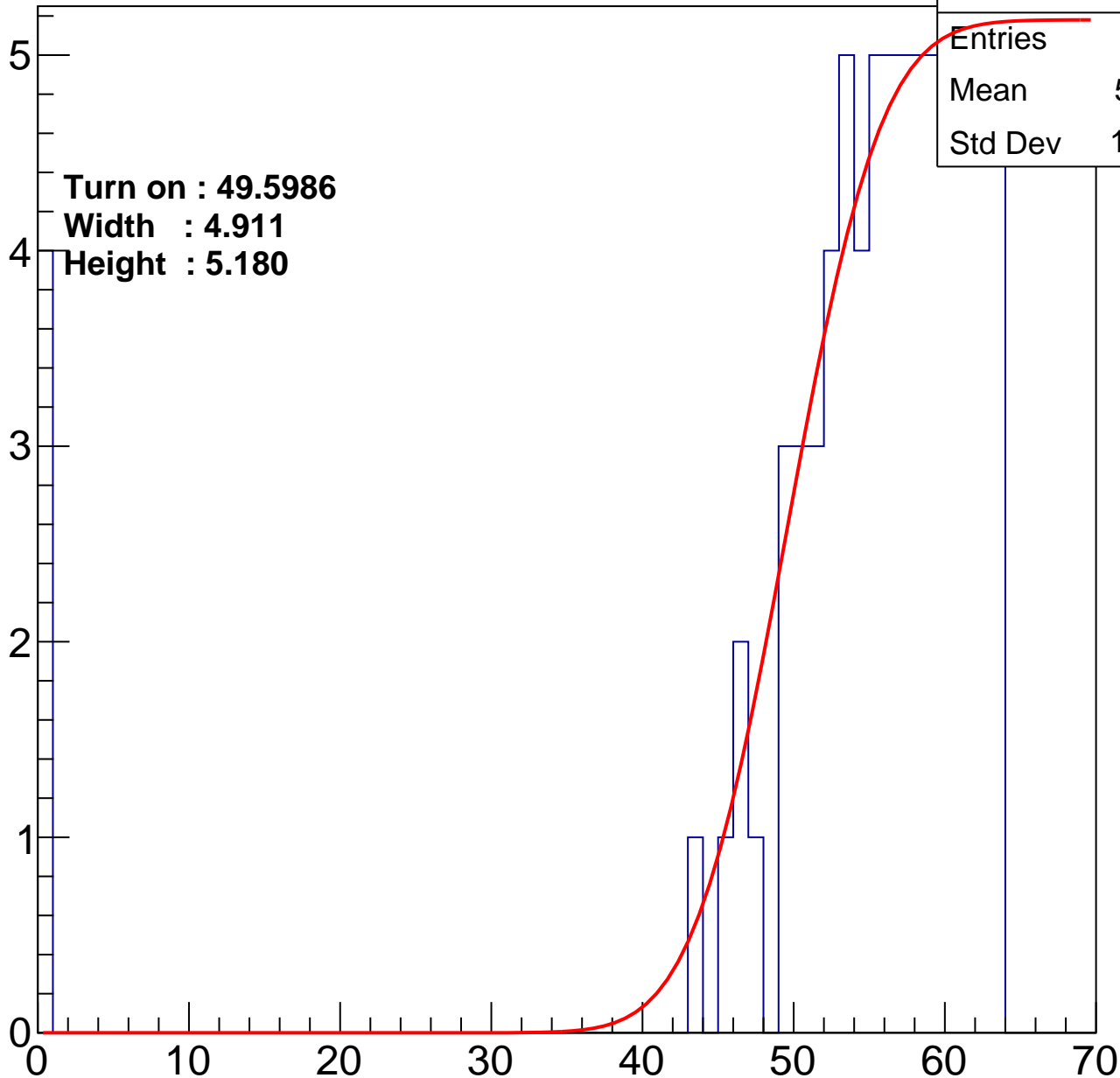
Entry

5
4
3
2
1
0

Turn on : 49.5986
Width : 4.911
Height : 5.180

Entries	76
Mean	52.91
Std Dev	13.35

ampl



B0L103S, U15-ch83

calib_packv5_040323_1717.root, FC#2, Port C3

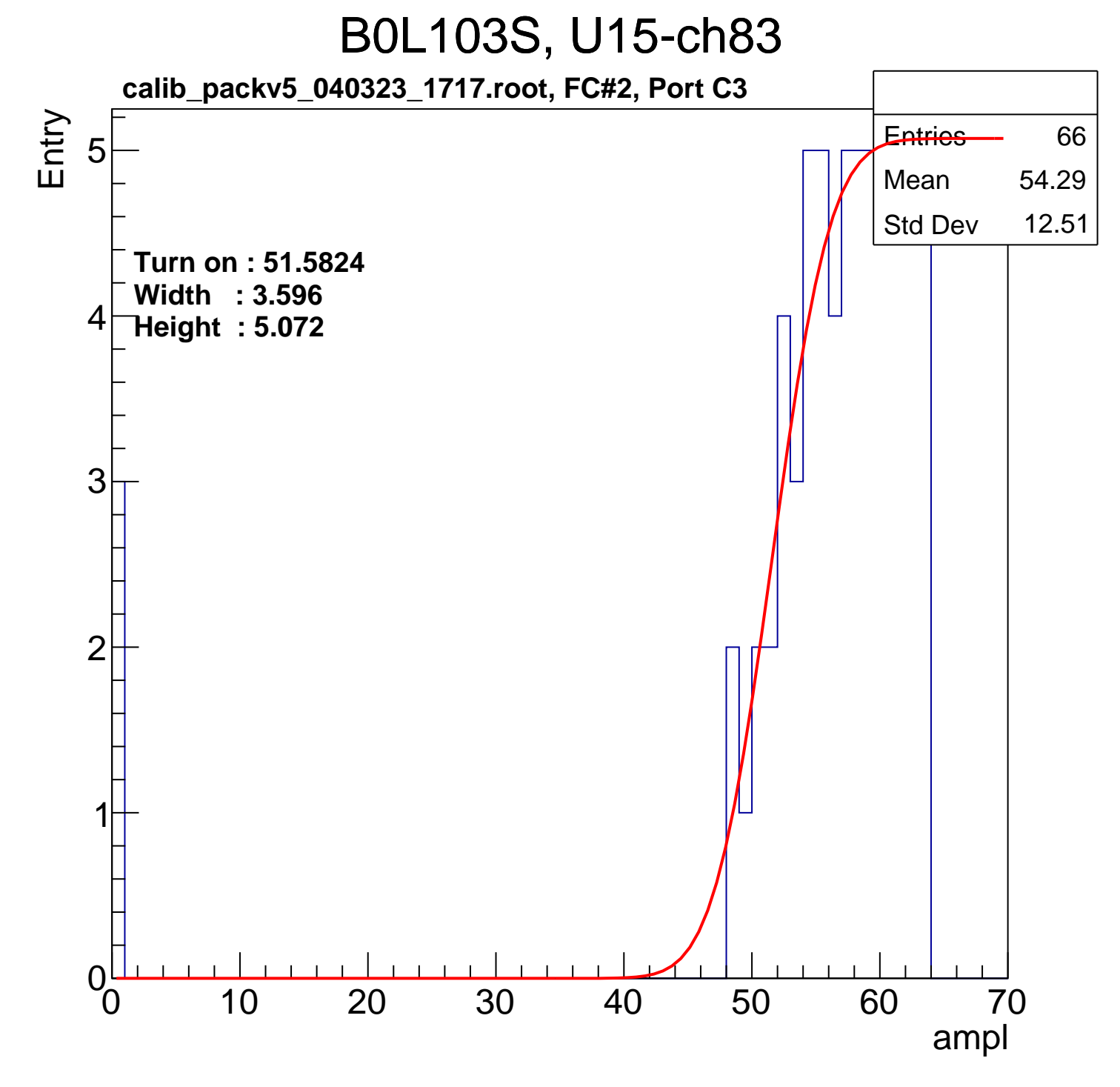
Entry

5
4
3
2
1
0

Turn on : 51.5824
Width : 3.596
Height : 5.072

Entries	66
Mean	54.29
Std Dev	12.51

ampl



B0L103S, U15-ch84

calib_packv5_040323_1717.root, FC#2, Port C3

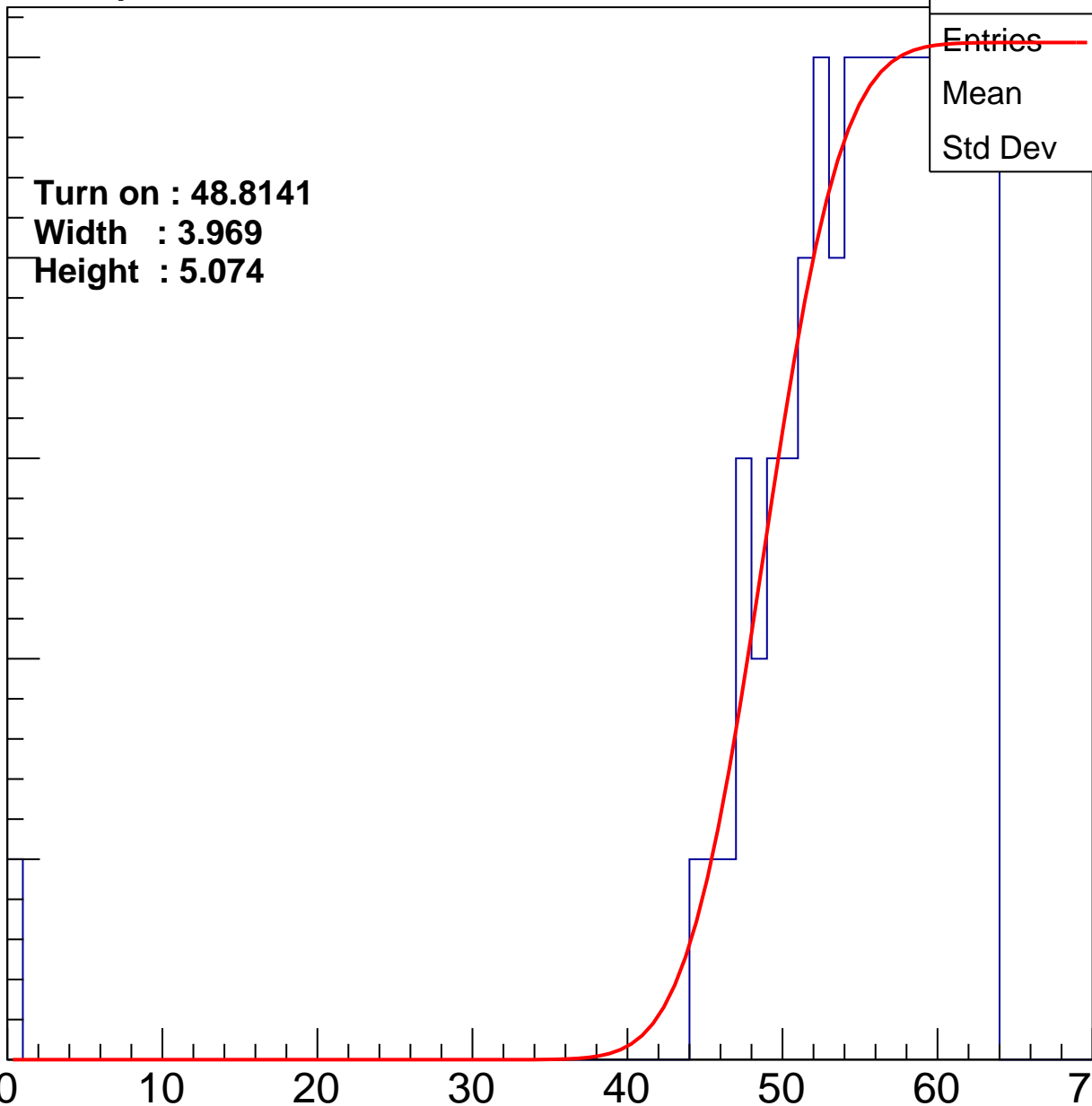
Entry

5
4
3
2
1
0

Turn on : 48.8141
Width : 3.969
Height : 5.074

Entries	78
Mean	54.74
Std Dev	7.962

ampl



B0L103S, U15-ch85

calib_packv5_040323_1717.root, FC#2, Port C3

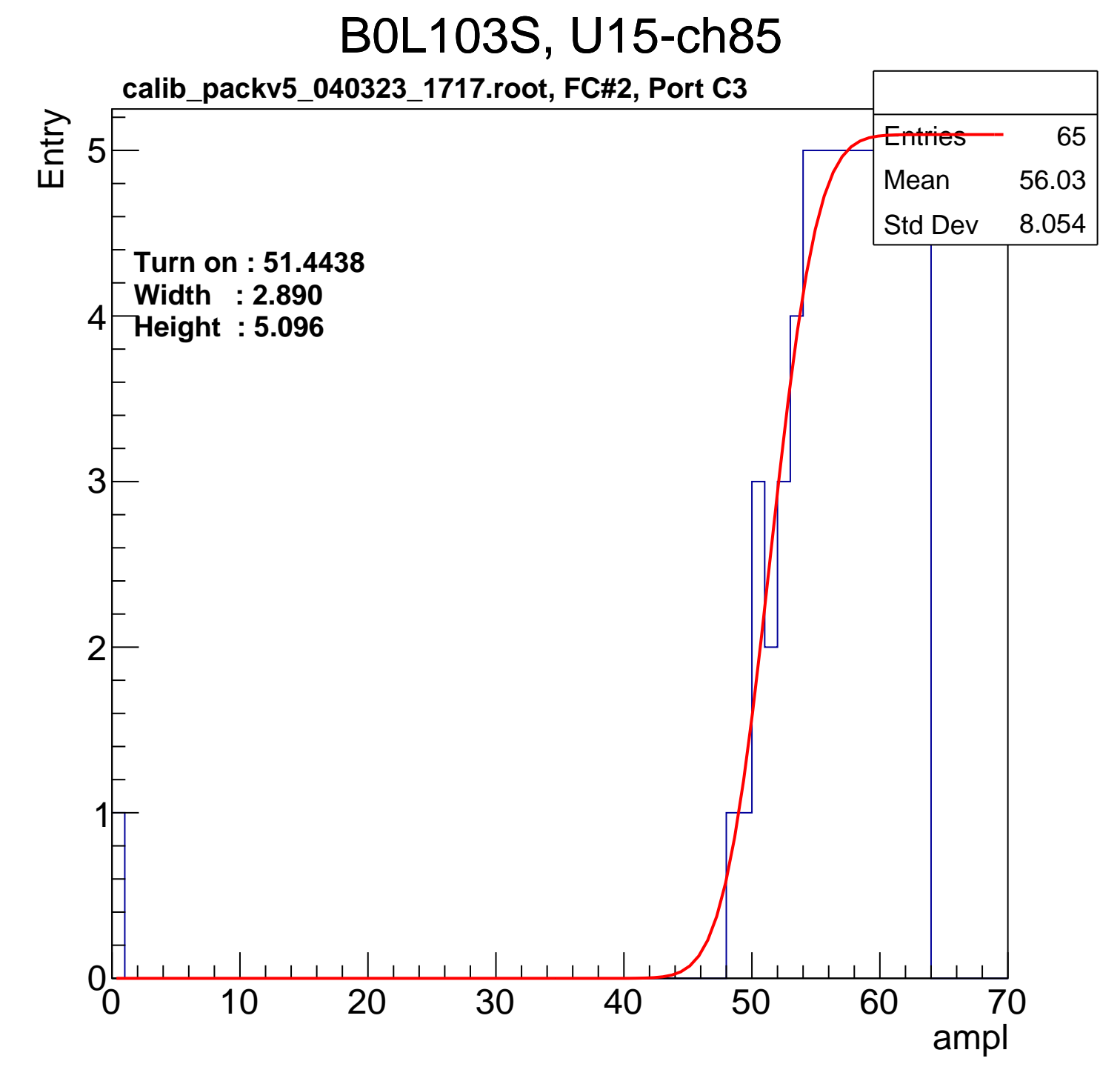
Entry

5
4
3
2
1
0

Turn on : 51.4438
Width : 2.890
Height : 5.096

Entries	65
Mean	56.03
Std Dev	8.054

ampl



B0L103S, U15-ch86

calib_packv5_040323_1717.root, FC#2, Port C3

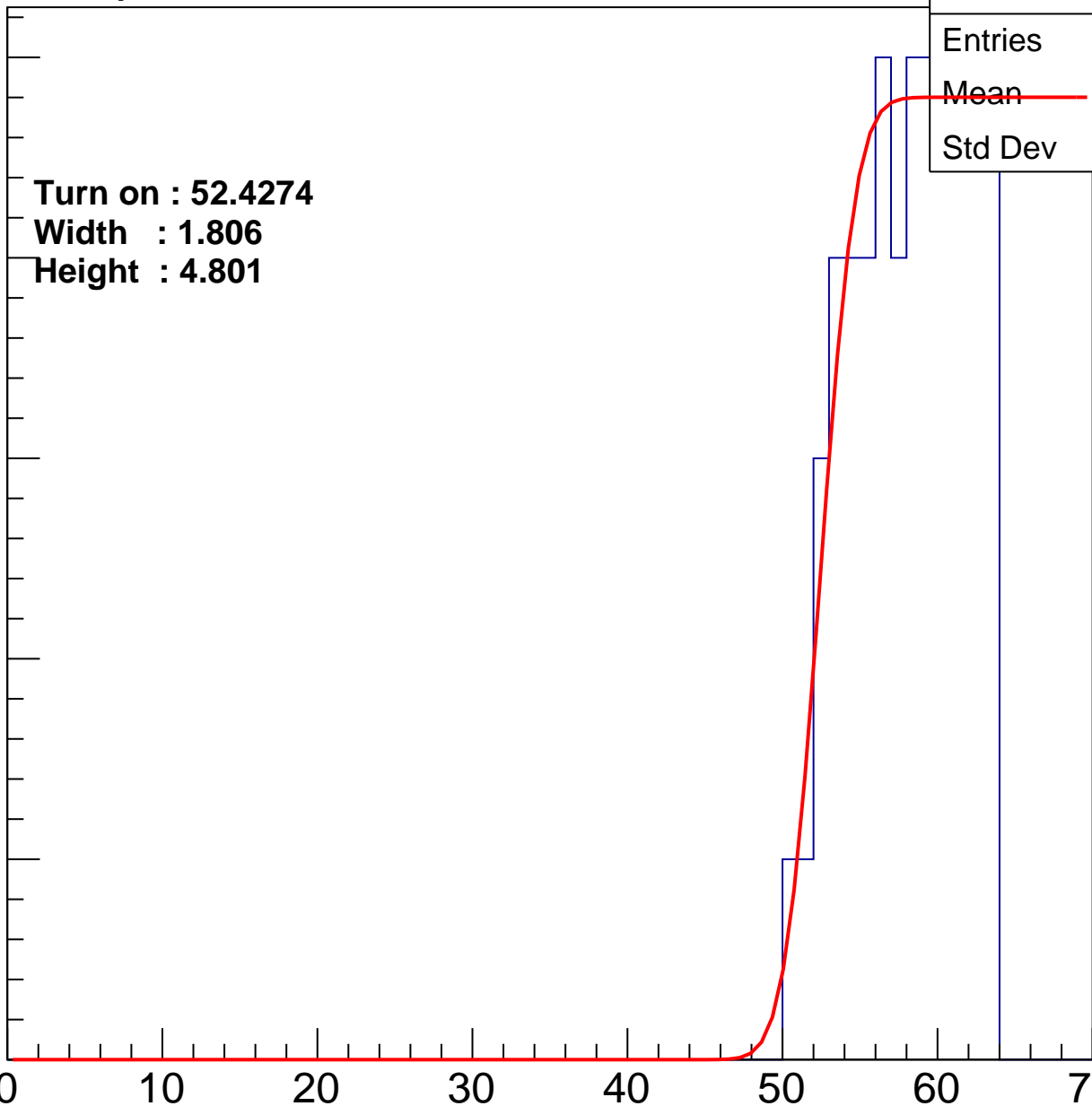
Entry

5
4
3
2
1
0

Turn on : 52.4274
Width : 1.806
Height : 4.801

Entries	56
Mean	57.64
Std Dev	3.568

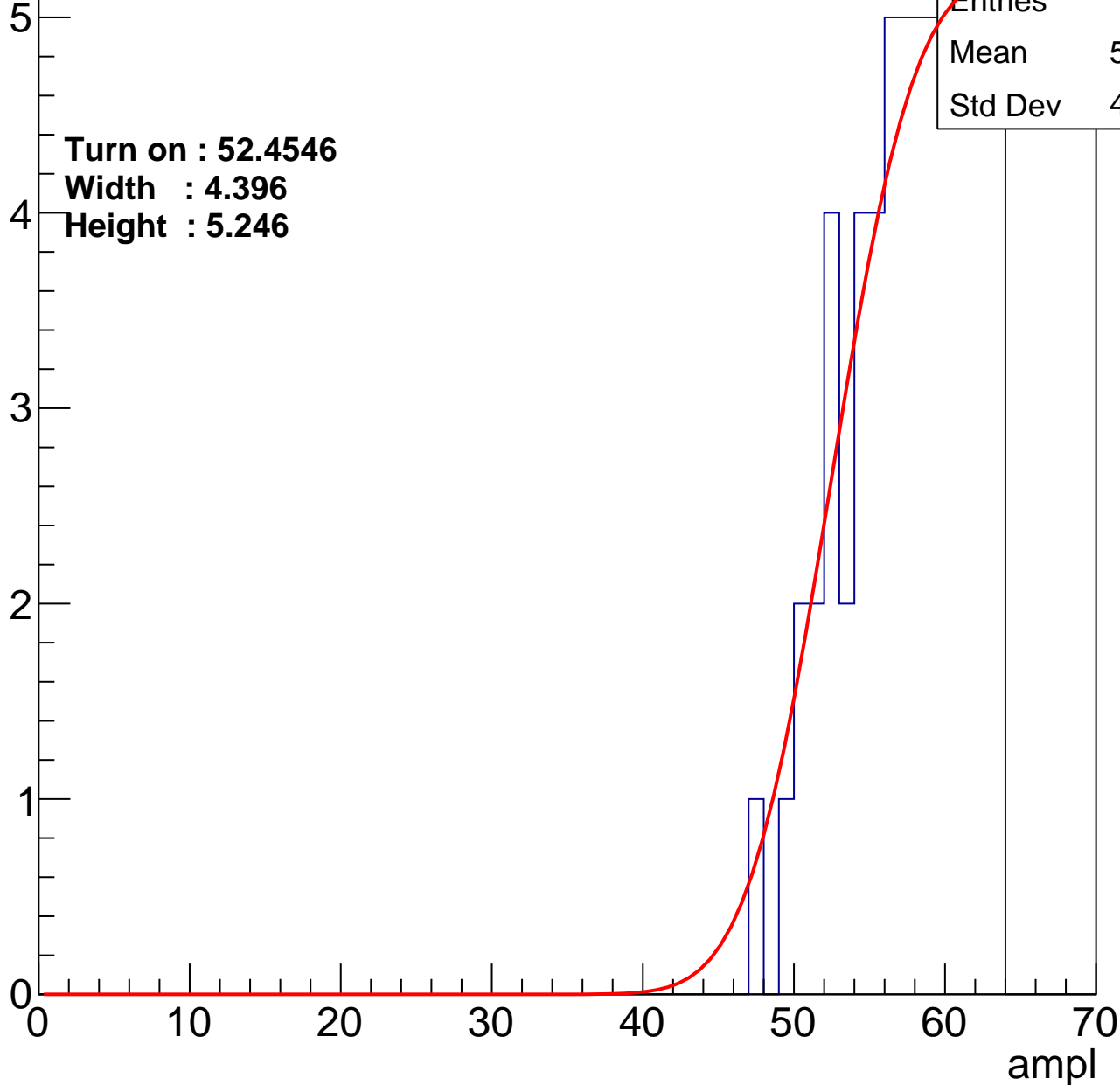
ampl



B0L103S, U15-ch87

calib_packv5_040323_1717.root, FC#2, Port C3

Entry



B0L103S, U15-ch88

calib_packv5_040323_1717.root, FC#2, Port C3

Entry

5

4

3

2

1

0

Turn on : 51.1469

Width : 3.345

Height : 5.017

Entries	67
---------	----

Mean	54.27
------	-------

Std Dev	12.42
---------	-------

ampl

0

10

20

30

40

50

60

70

B0L103S, U15-ch89

calib_packv5_040323_1717.root, FC#2, Port C3

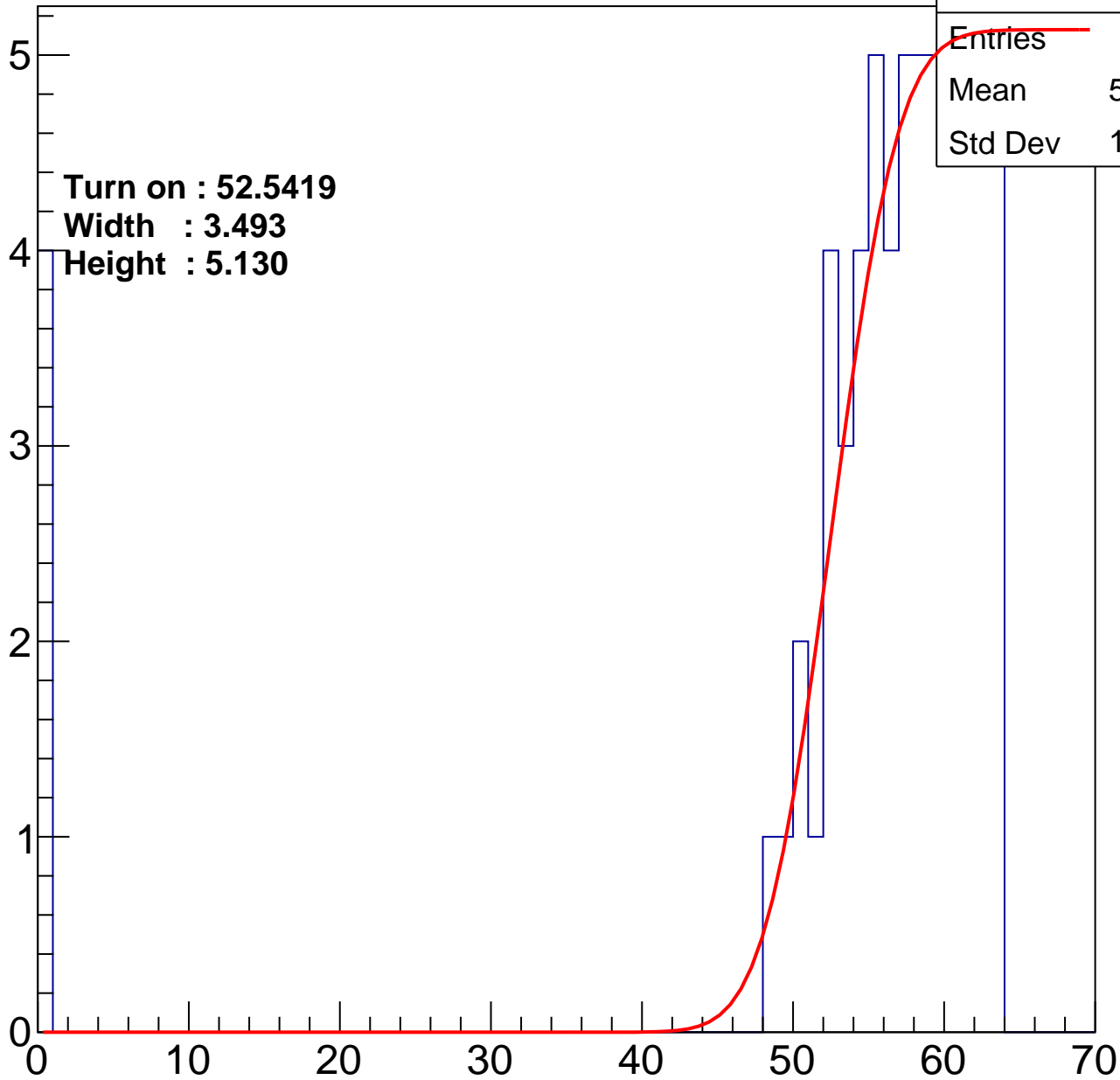
Entry

5
4
3
2
1
0

Turn on : 52.5419
Width : 3.493
Height : 5.130

Entries	64
Mean	53.59
Std Dev	14.36

ampl



B0L103S, U15-ch90

calib_packv5_040323_1717.root, FC#2, Port C3

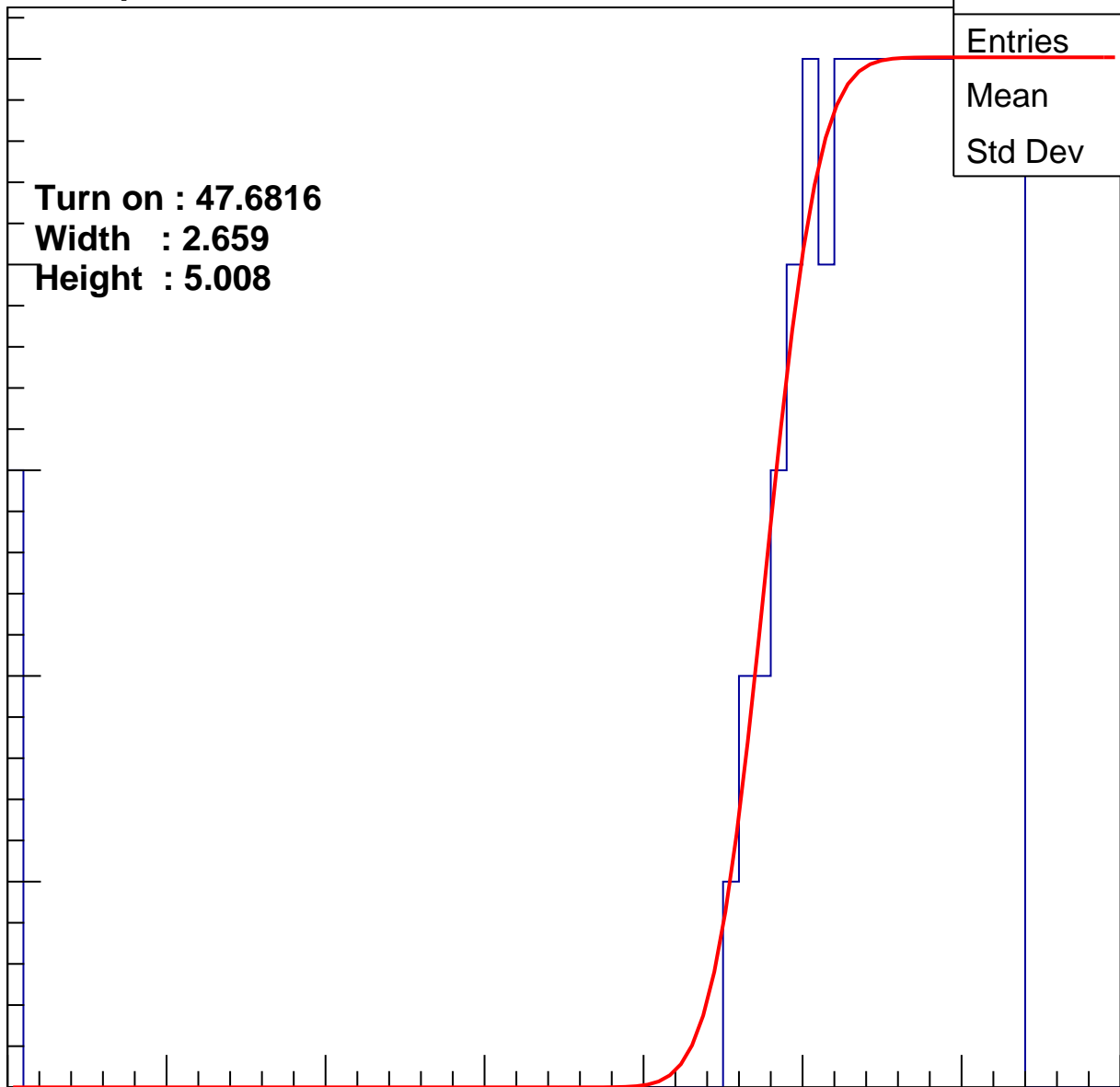
Entry

5
4
3
2
1
0

Turn on : 47.6816
Width : 2.659
Height : 5.008

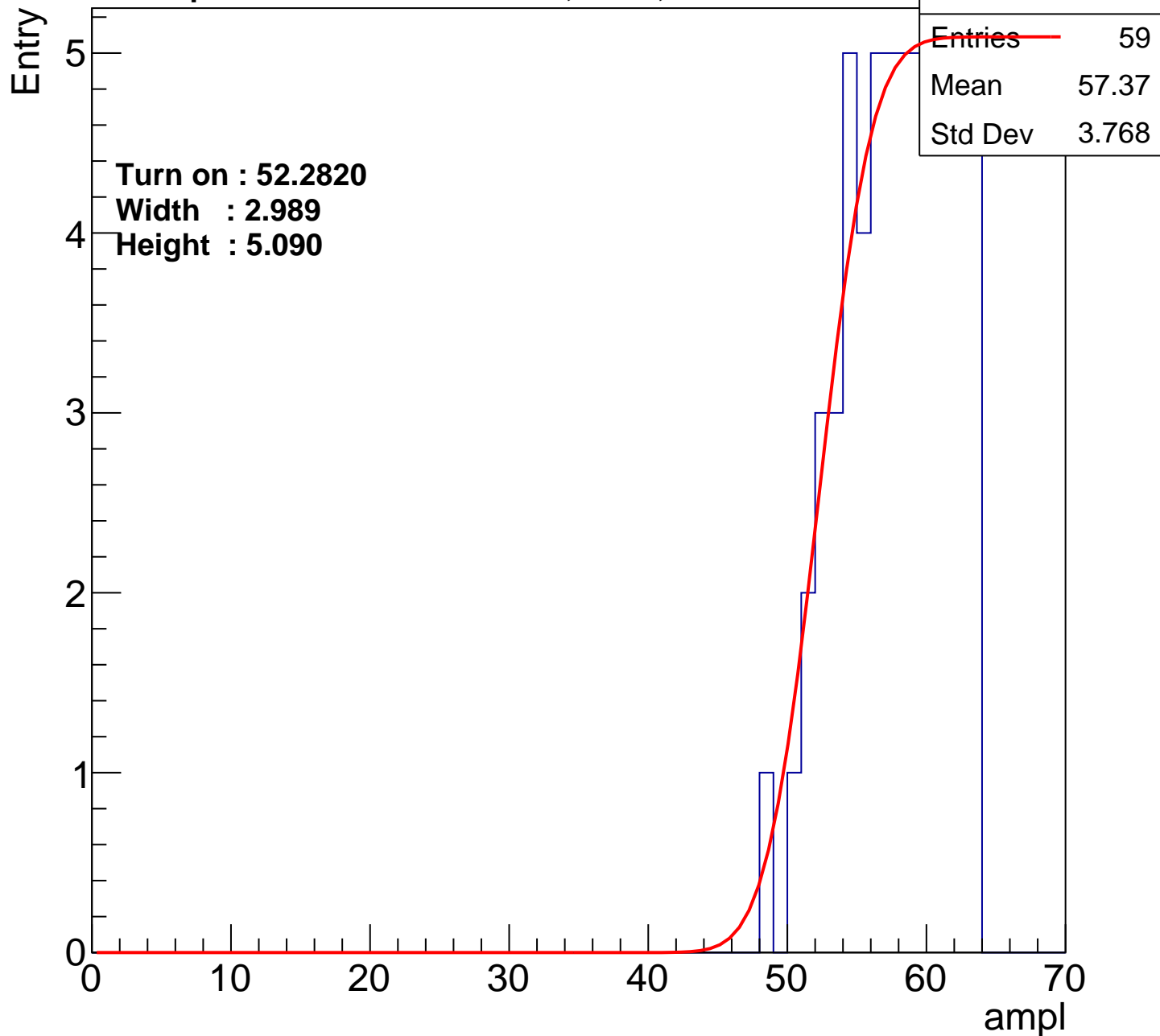
Entries	84
Mean	53.27
Std Dev	11.33

ampl



B0L103S, U15-ch91

calib_packv5_040323_1717.root, FC#2, Port C3



B0L103S, U15-ch92

calib_packv5_040323_1717.root, FC#2, Port C3

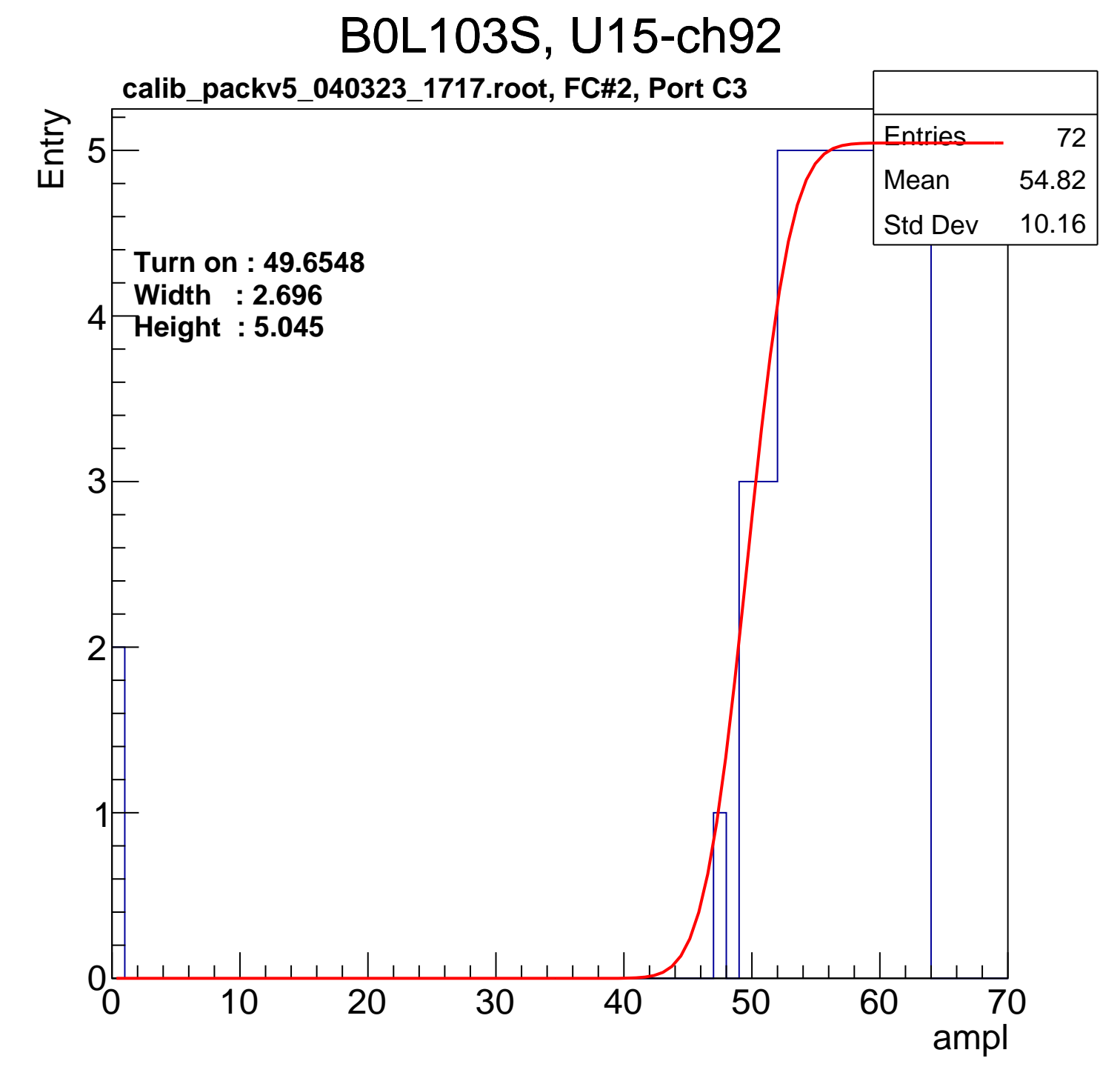
Entry

5
4
3
2
1
0

Turn on : 49.6548
Width : 2.696
Height : 5.045

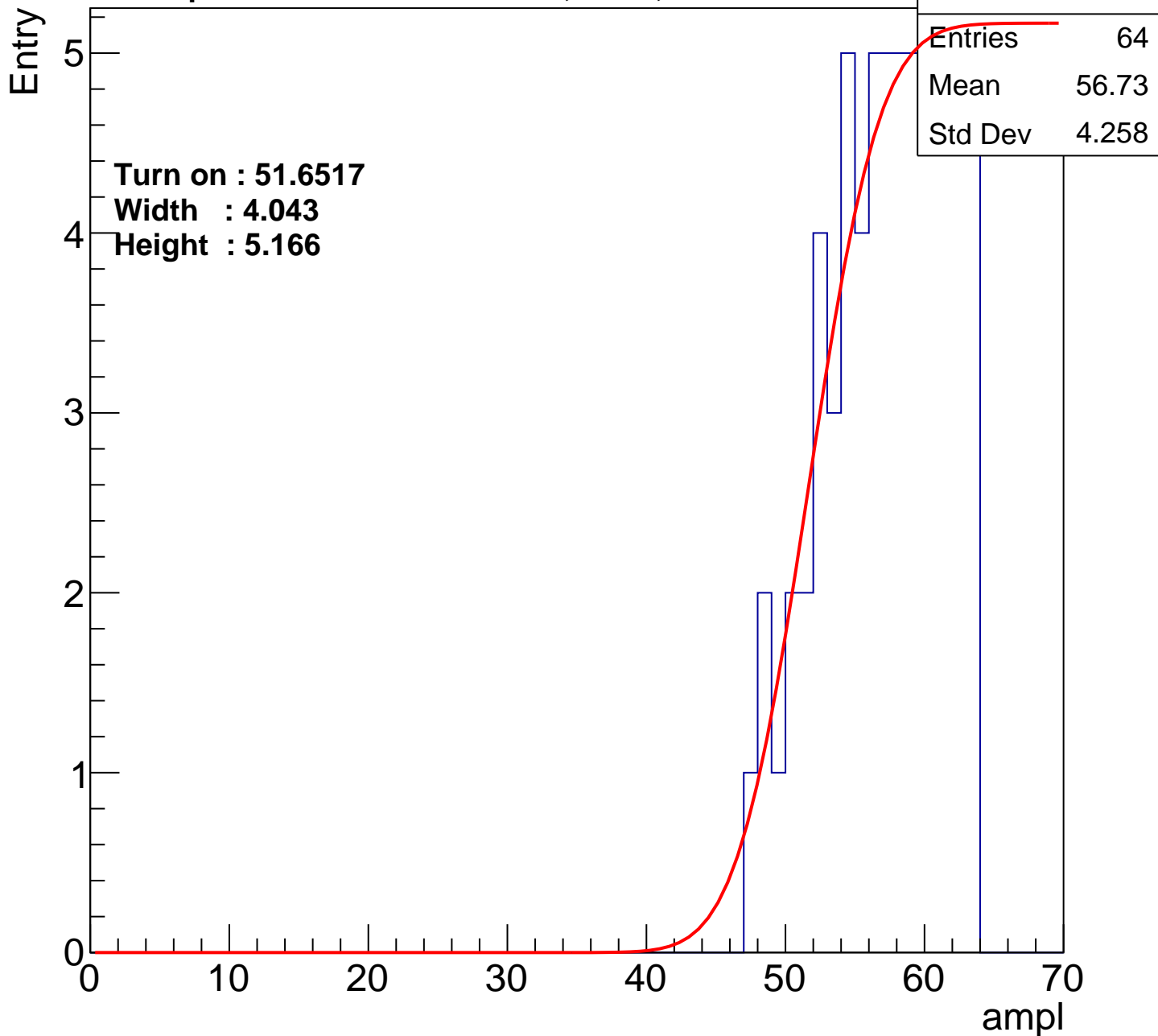
Entries	72
Mean	54.82
Std Dev	10.16

ampl



B0L103S, U15-ch93

calib_packv5_040323_1717.root, FC#2, Port C3



B0L103S, U15-ch94

calib_packv5_040323_1717.root, FC#2, Port C3

Entry

5

4

3

2

1

0

Turn on : 49.5201

Width : 4.577

Height : 5.199

Entries	81
Mean	53.38
Std Dev	11.52

ampl

0

10

20

30

40

50

60

70

B0L103S, U15-ch95

calib_packv5_040323_1717.root, FC#2, Port C3

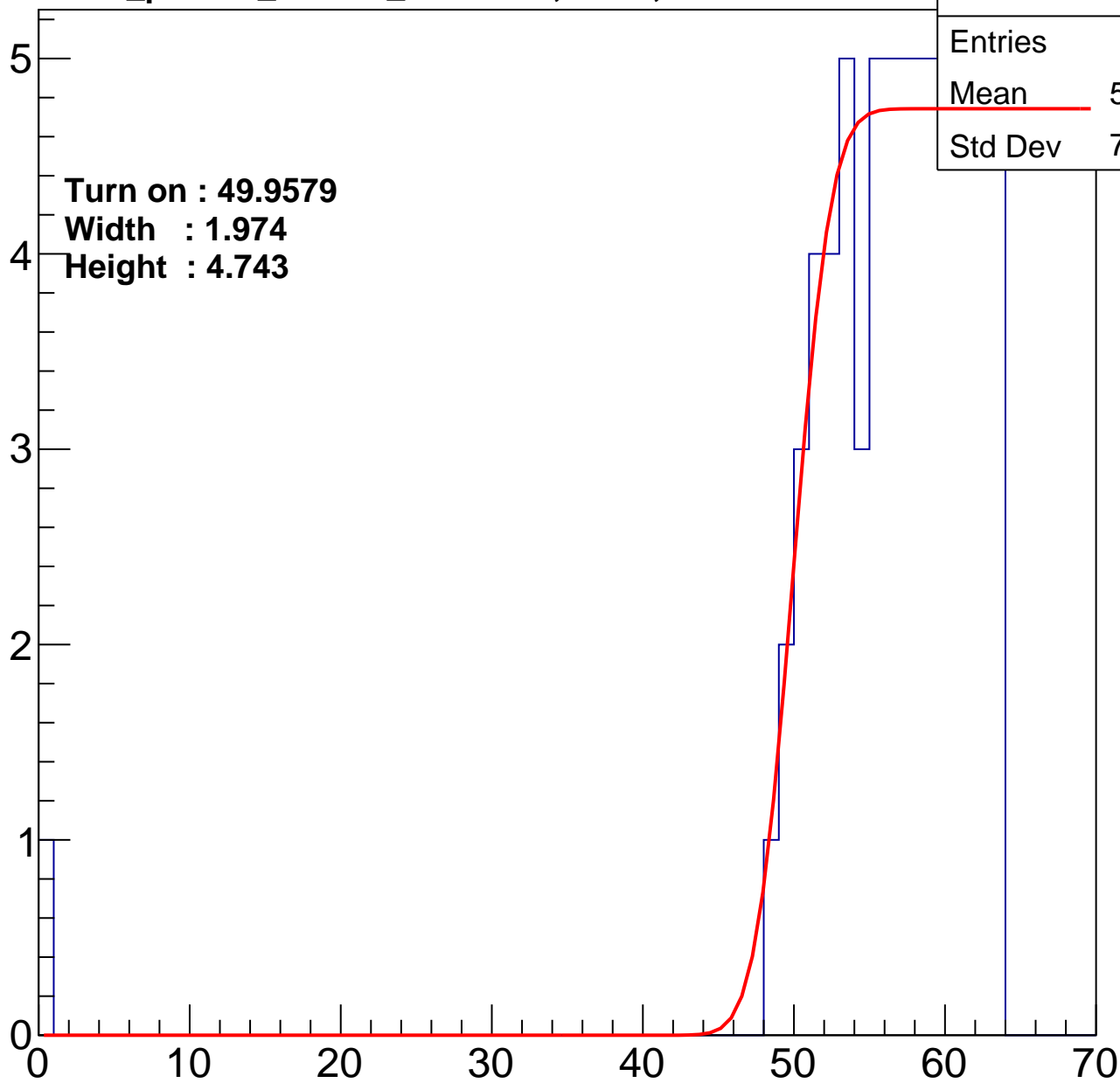
Entry

5
4
3
2
1
0

Turn on : 49.9579
Width : 1.974
Height : 4.743

Entries	68
Mean	55.74
Std Dev	7.977

ampl



B0L103S, U15-ch96

calib_packv5_040323_1717.root, FC#2, Port C3

Entry

5

4

3

2

1

0

Turn on : 51.8753

Width : 4.109

Height : 5.240

Entries	67
Mean	55.63
Std Dev	8.179

ampl

0

10

20

30

40

50

60

70

B0L103S, U15-ch97

calib_packv5_040323_1717.root, FC#2, Port C3

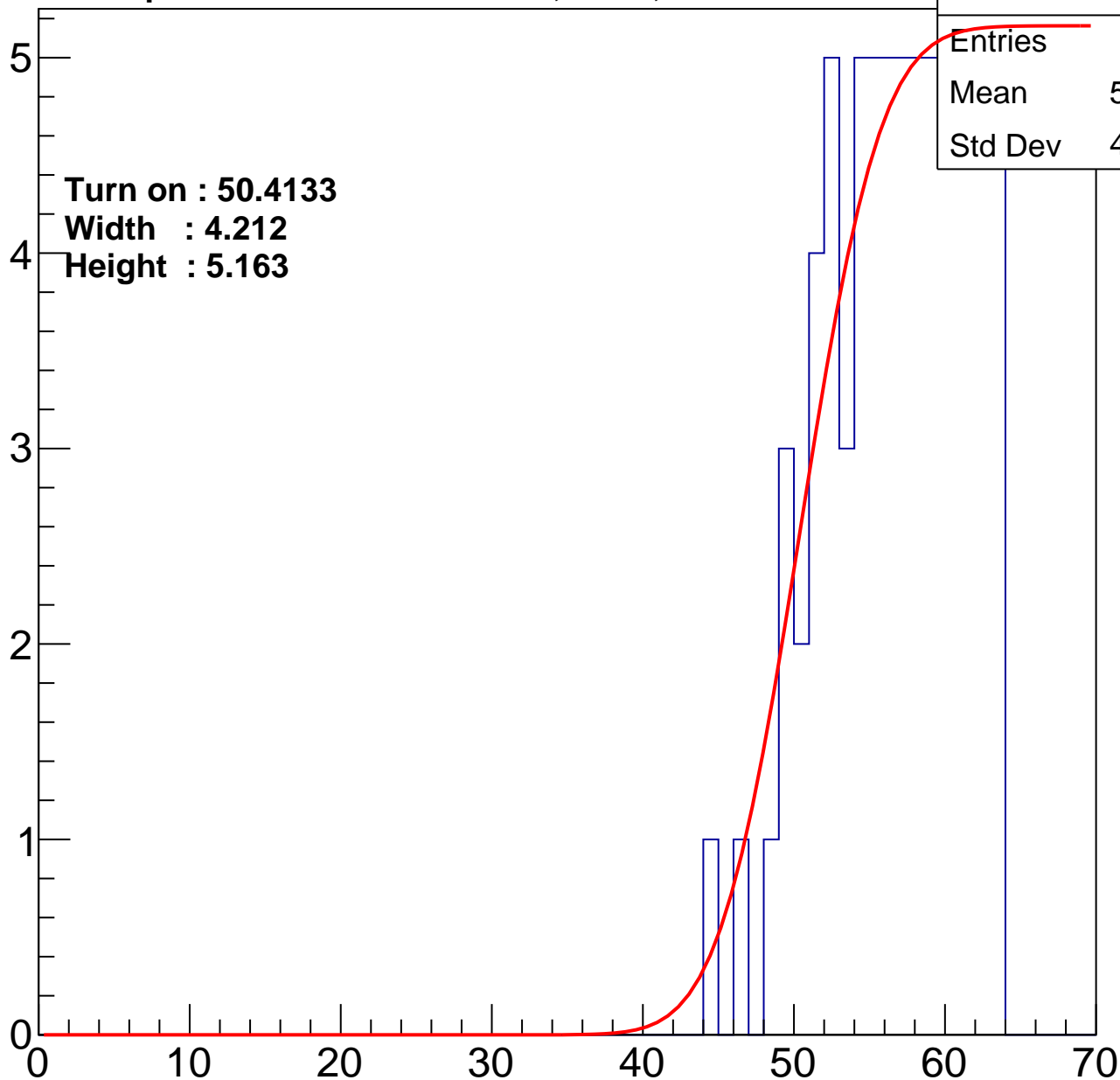
Entry

5
4
3
2
1
0

Turn on : 50.4133
Width : 4.212
Height : 5.163

Entries	70
Mean	56.19
Std Dev	4.562

ampl



B0L103S, U15-ch98

calib_packv5_040323_1717.root, FC#2, Port C3

Entry

5

4

3

2

1

0

Turn on : 48.9654

Width : 3.414

Height : 5.084

Entries 76

Mean 55.66

Std Dev 4.784

ampl

0

10

20

30

40

50

60

70

B0L103S, U15-ch99

calib_packv5_040323_1717.root, FC#2, Port C3

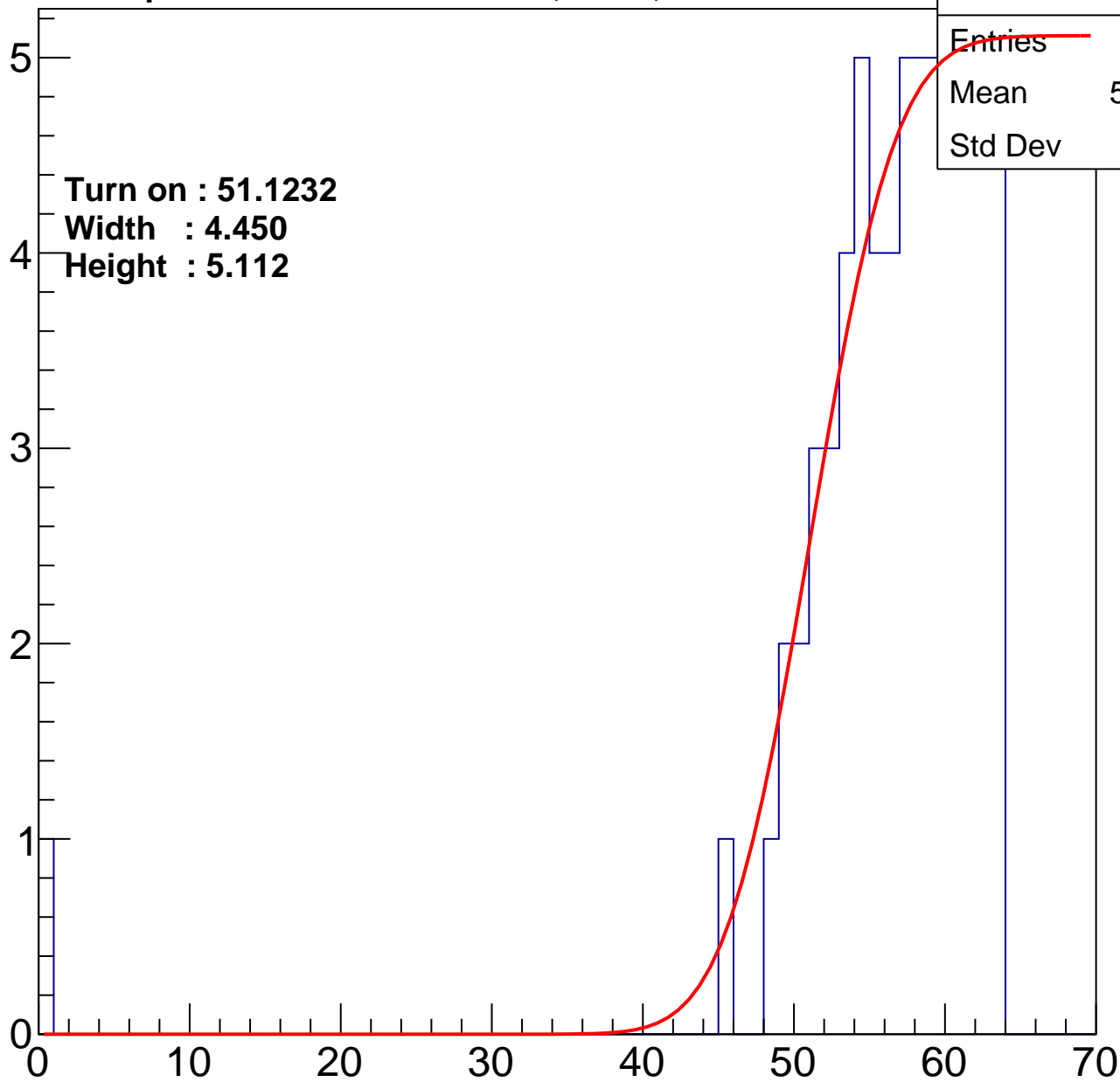
Entry

5
4
3
2
1
0

Turn on : 51.1232
Width : 4.450
Height : 5.112

Entries	65
Mean	55.78
Std Dev	8.2

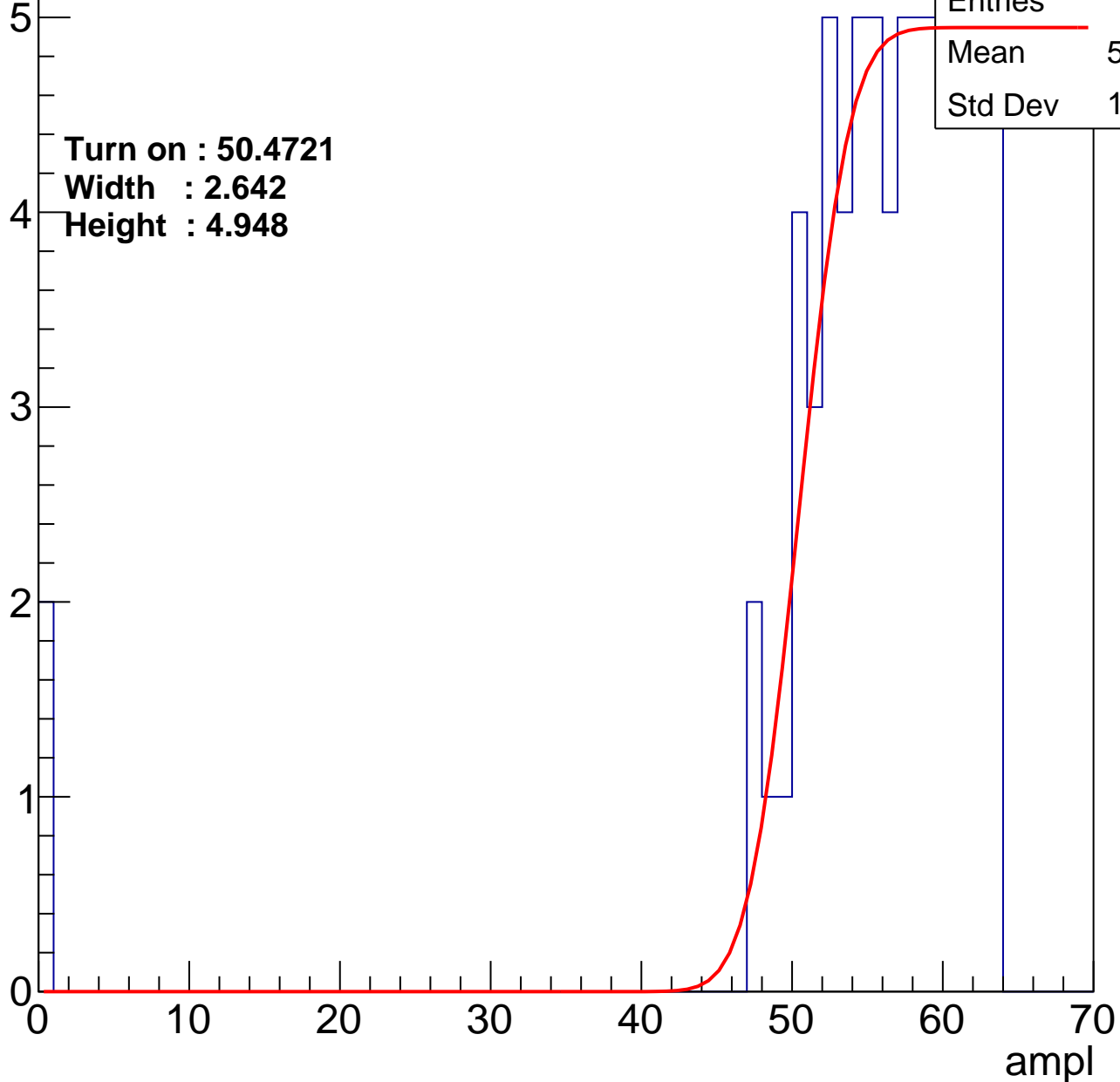
ampl



B0L103S, U15-ch100

calib_packv5_040323_1717.root, FC#2, Port C3

Entry



B0L103S, U15-ch101

calib_packv5_040323_1717.root, FC#2, Port C3

Entry

5

4

3

2

1

0

Turn on : 49.7166

Width : 4.972

Height : 5.238

Entries	79
---------	----

Mean	53.44
------	-------

Std Dev	11.67
---------	-------

ampl

0

10

20

30

40

50

60

70

B0L103S, U15-ch102

calib_packv5_040323_1717.root, FC#2, Port C3

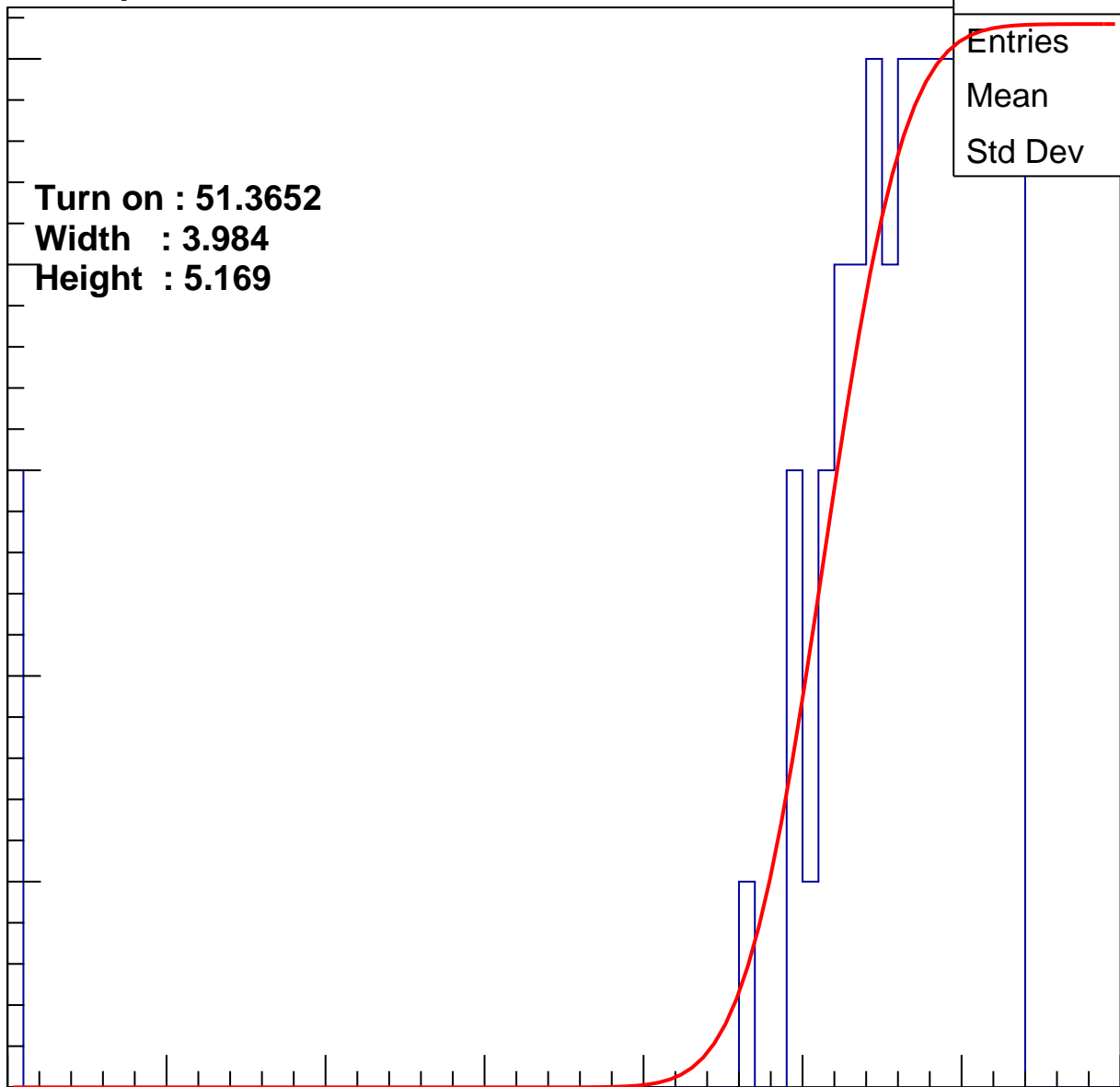
Entry

5
4
3
2
1
0

Turn on : 51.3652
Width : 3.984
Height : 5.169

Entries	68
Mean	54.21
Std Dev	12.35

ampl



B0L103S, U15-ch103

calib_packv5_040323_1717.root, FC#2, Port C3

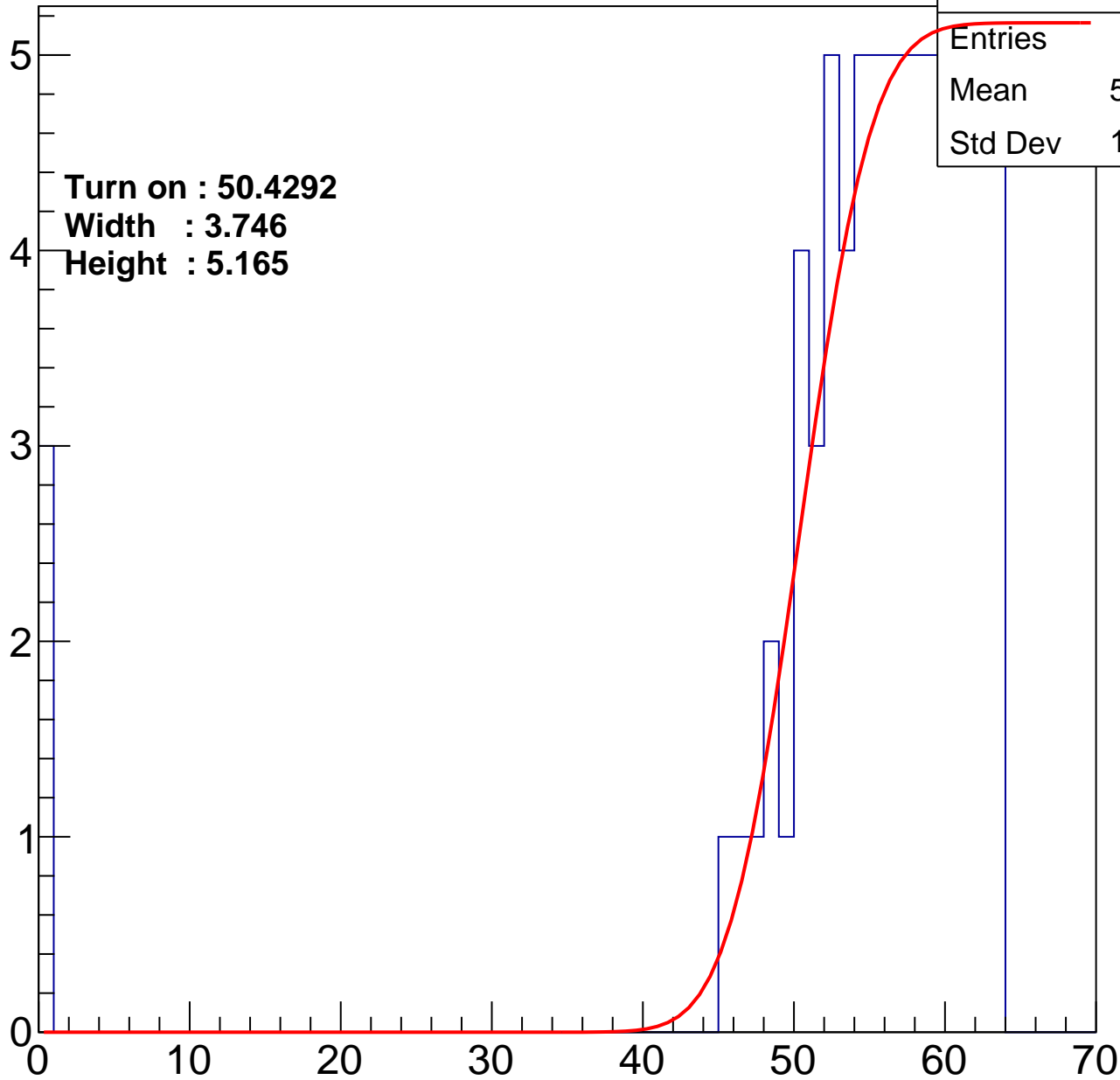
Entry

5
4
3
2
1
0

Turn on : 50.4292
Width : 3.746
Height : 5.165

Entries	75
Mean	53.77
Std Dev	11.87

ampl



B0L103S, U15-ch104

calib_packv5_040323_1717.root, FC#2, Port C3

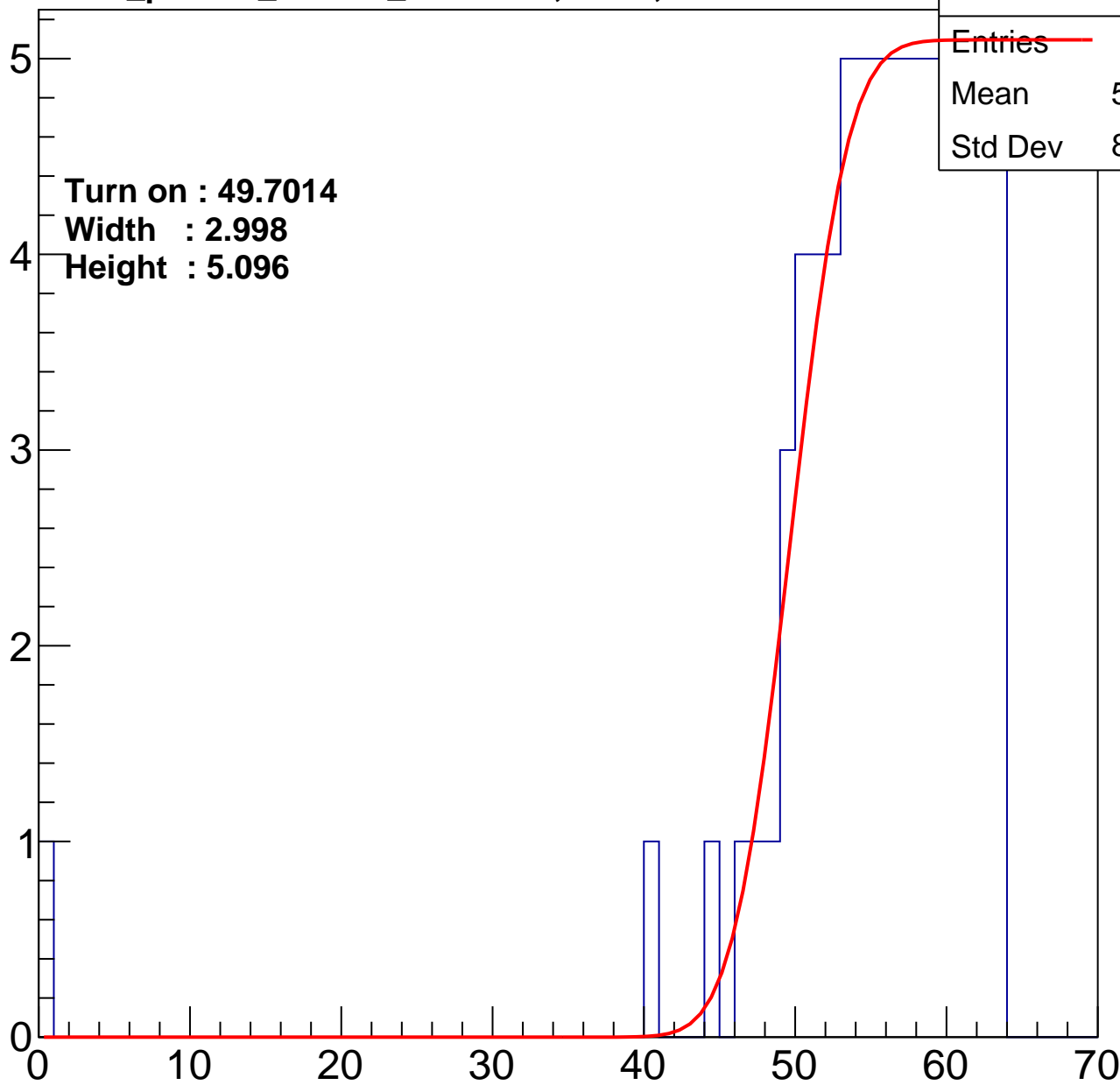
Entry

5
4
3
2
1
0

Turn on : 49.7014
Width : 2.998
Height : 5.096

Entries	76
Mean	54.92
Std Dev	8.044

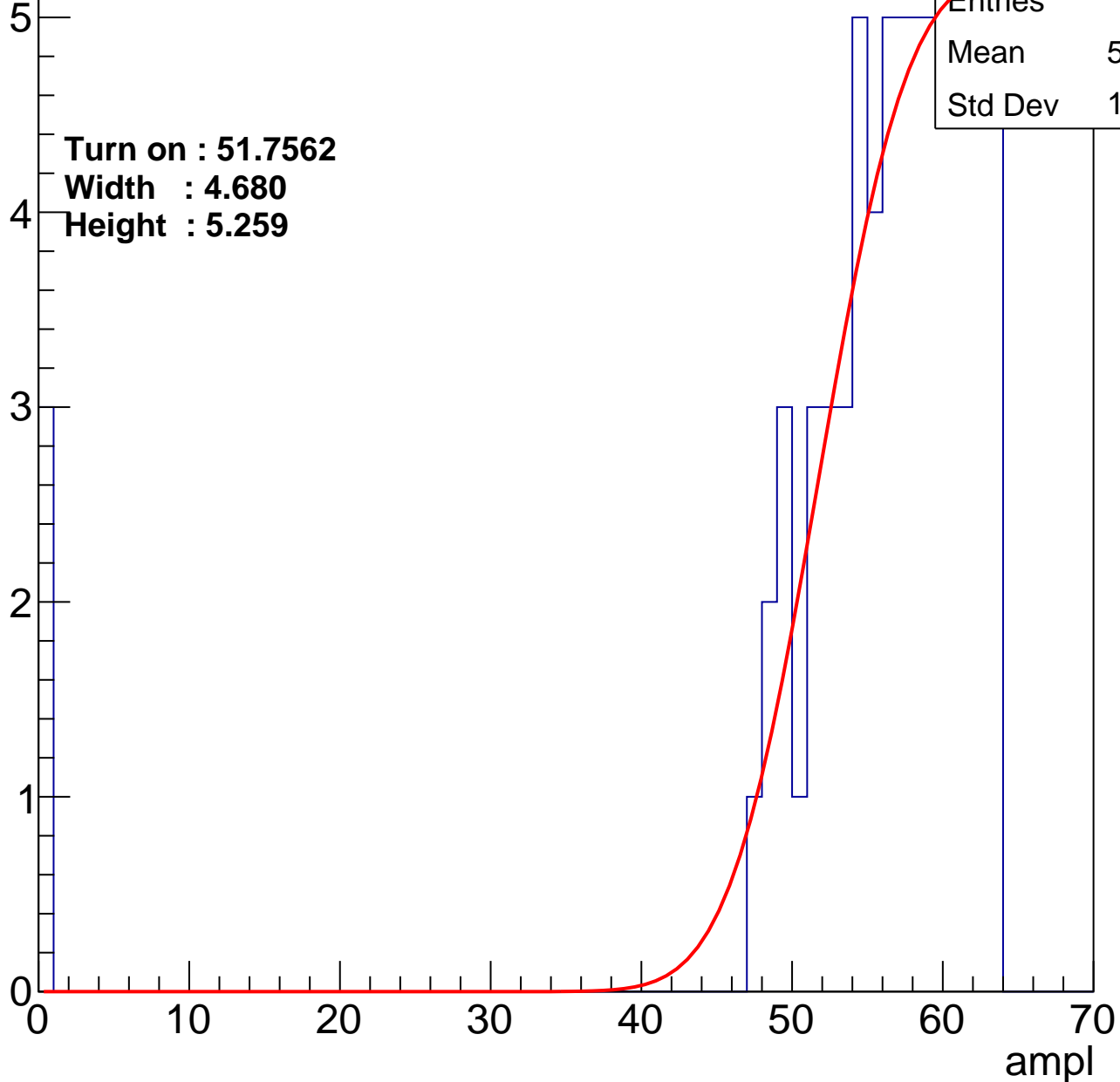
ampl



B0L103S, U15-ch105

calib_packv5_040323_1717.root, FC#2, Port C3

Entry



B0L103S, U15-ch106

calib_packv5_040323_1717.root, FC#2, Port C3

Entry

5

4

3

2

1

0

Turn on : 51.4550

Width : 4.173

Height : 5.218

Entries	65
Mean	56.68
Std Dev	4.286

ampl

0

10

20

30

40

50

60

70

B0L103S, U15-ch107

calib_packv5_040323_1717.root, FC#2, Port C3

Entry

5

4

3

2

1

0

Turn on : 51.9426

Width : 4.352

Height : 5.299

Entries	68
Mean	54.94
Std Dev	10.46

ampl

0

10

20

30

40

50

60

70

B0L103S, U15-ch108

calib_packv5_040323_1717.root, FC#2, Port C3

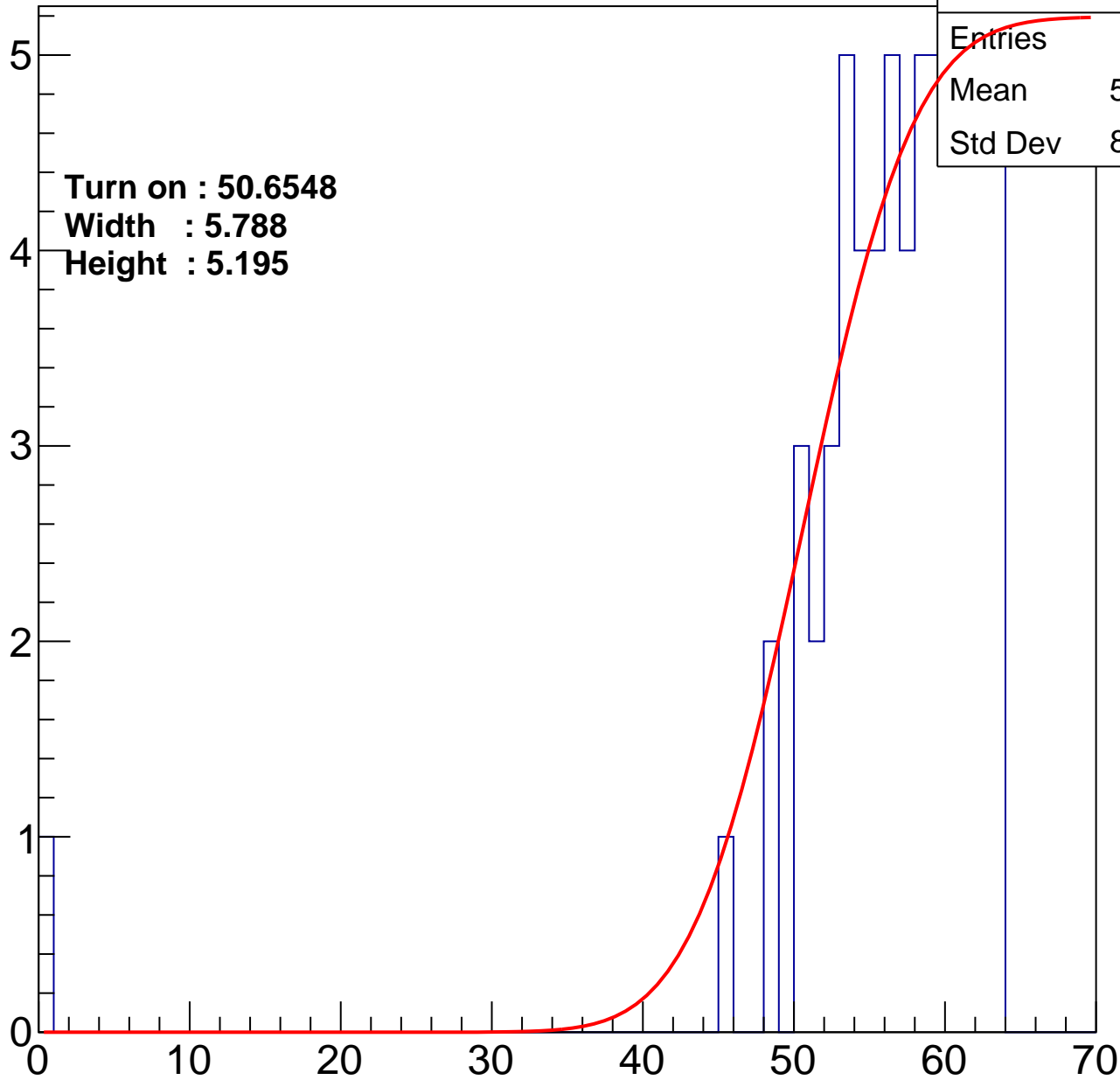
Entry

5
4
3
2
1
0

Turn on : 50.6548
Width : 5.788
Height : 5.195

Entries	64
Mean	55.83
Std Dev	8.247

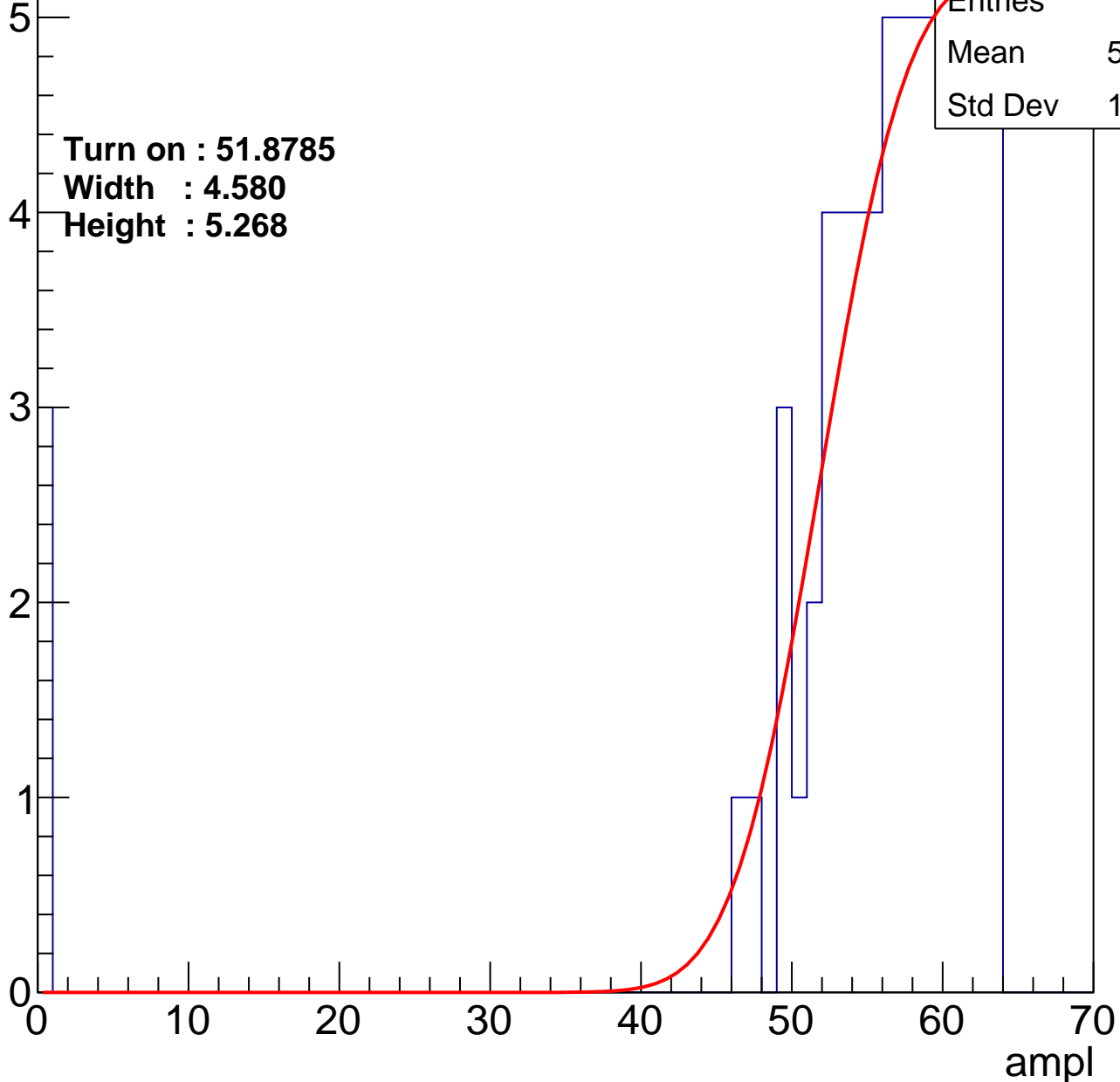
ampl



B0L103S, U15-ch109

calib_packv5_040323_1717.root, FC#2, Port C3

Entry



B0L103S, U15-ch110

calib_packv5_040323_1717.root, FC#2, Port C3

Entry

5

4

3

2

1

0

Turn on : 51.2191

Width : 3.918

Height : 5.178

Entries	71
---------	----

Mean	52.62
------	-------

Std Dev	15.06
---------	-------

ampl

0

10

20

30

40

50

60

70

B0L103S, U15-ch111

calib_packv5_040323_1717.root, FC#2, Port C3

Entry

5

4

3

2

1

0

Turn on : 49.2827

Width : 4.909

Height : 5.206

Entries	78
Mean	54.13
Std Dev	10.05

ampl

0

10

20

30

40

50

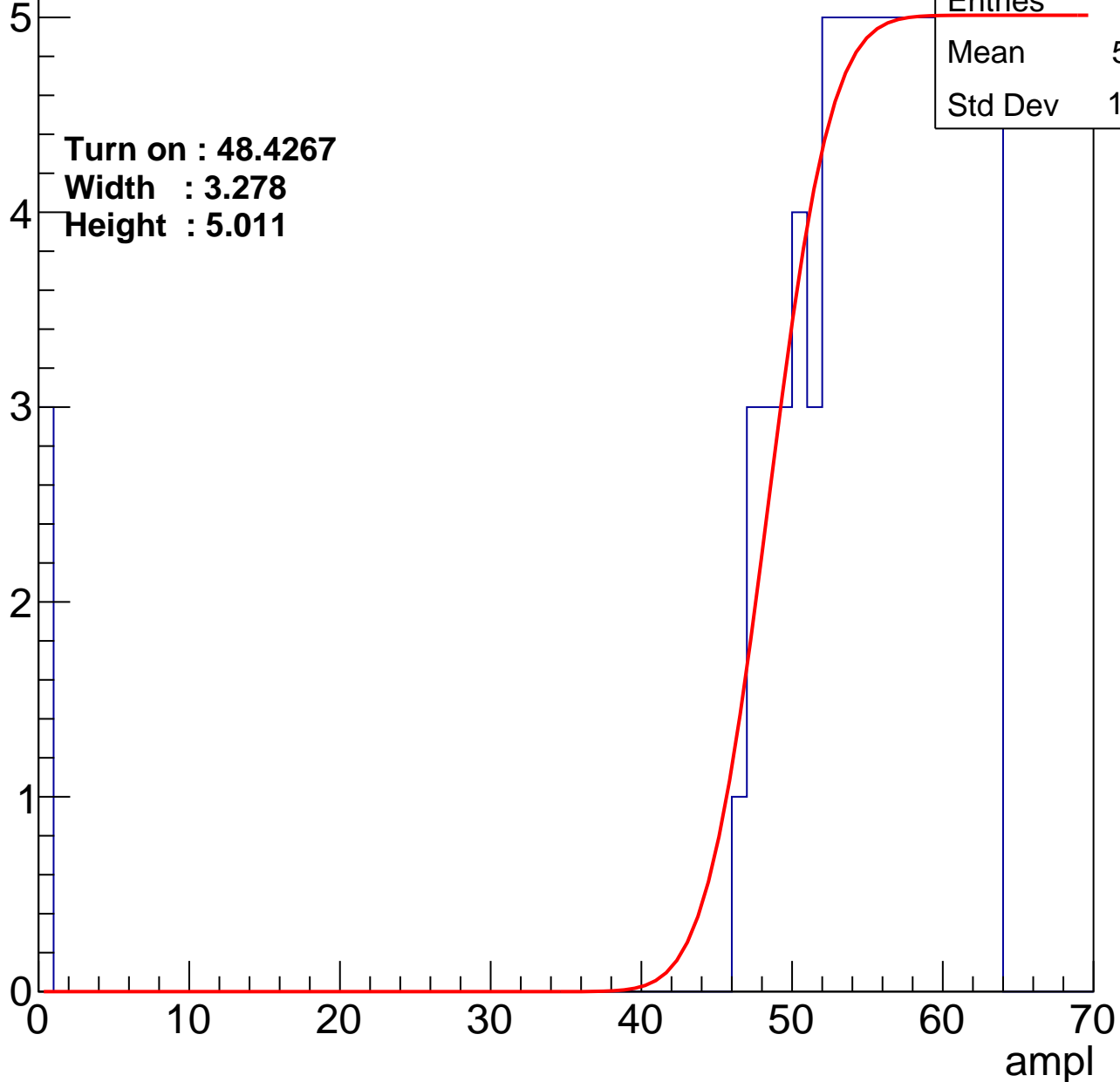
60

70

B0L103S, U15-ch112

calib_packv5_040323_1717.root, FC#2, Port C3

Entry



B0L103S, U15-ch113

calib_packv5_040323_1717.root, FC#2, Port C3

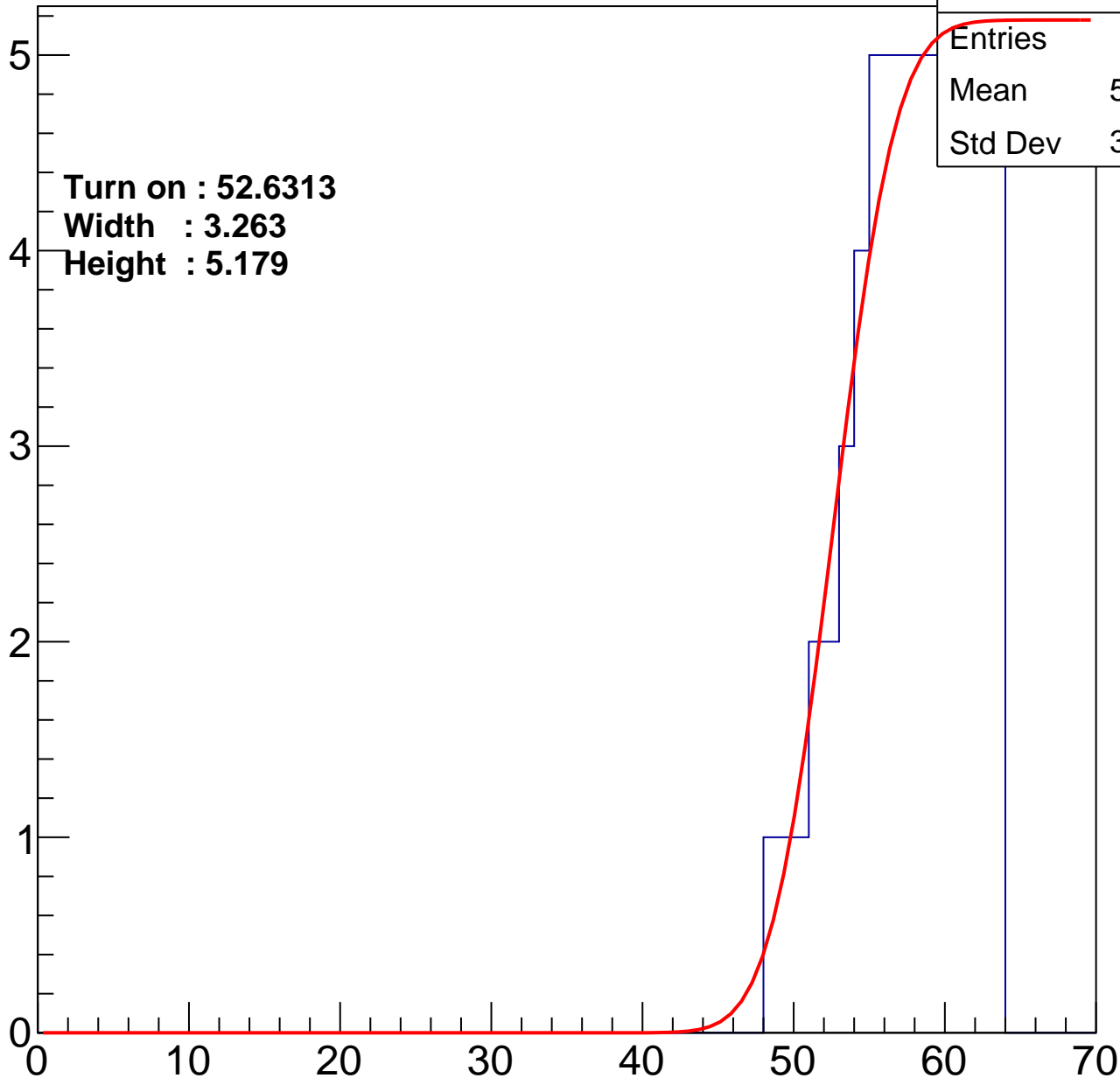
Entry

5
4
3
2
1
0

Turn on : 52.6313
Width : 3.263
Height : 5.179

Entries	59
Mean	57.34
Std Dev	3.847

ampl



B0L103S, U15-ch114

calib_packv5_040323_1717.root, FC#2, Port C3

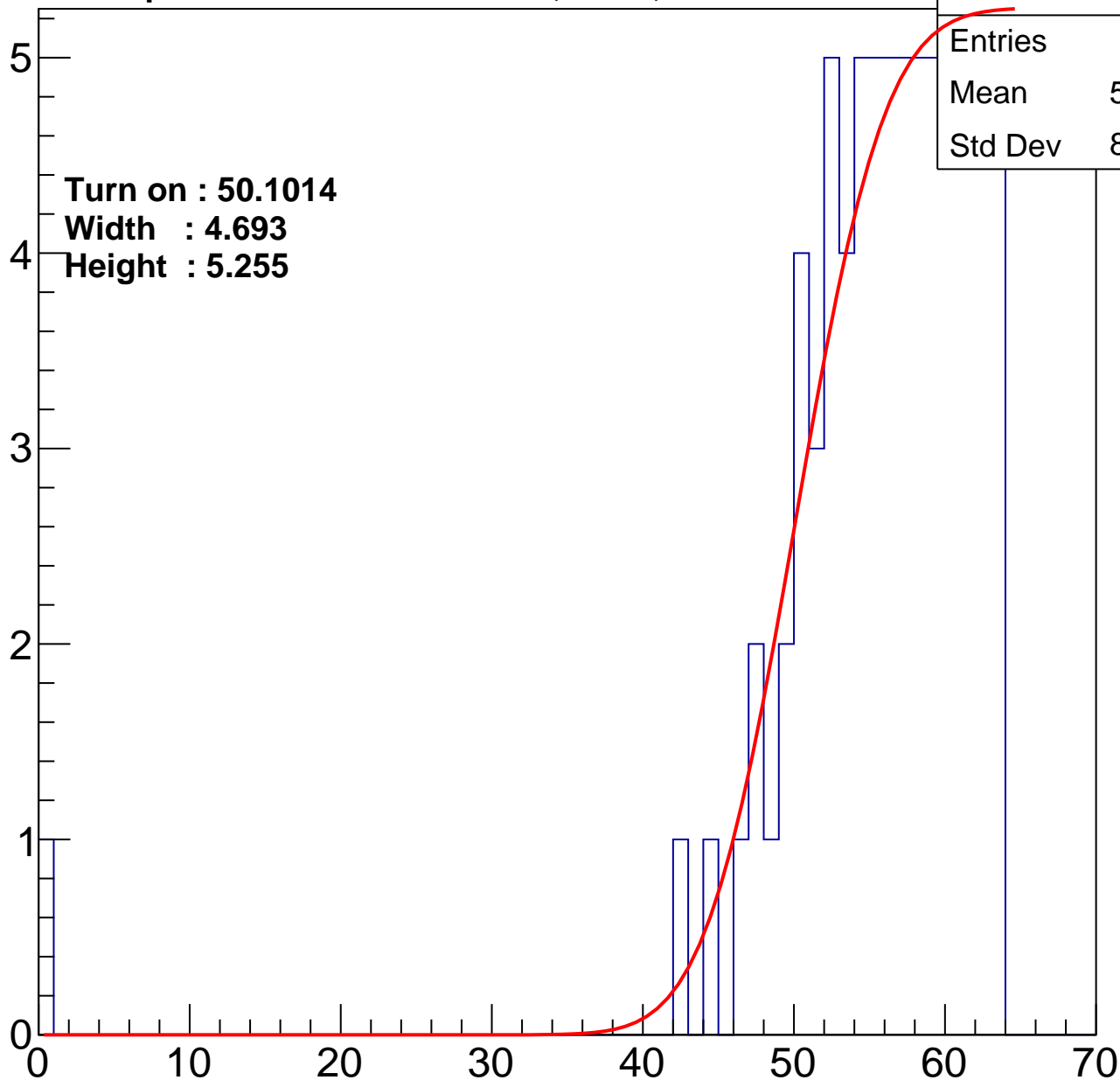
Entry

5
4
3
2
1
0

Turn on : 50.1014
Width : 4.693
Height : 5.255

Entries	75
Mean	54.96
Std Dev	8.065

ampl



B0L103S, U15-ch115

calib_packv5_040323_1717.root, FC#2, Port C3

Entry

5

4

3

2

1

0

Turn on : 50.4976

Width : 5.388

Height : 5.306

Entries	71
Mean	55.97
Std Dev	4.762

ampl

0

10

20

30

40

50

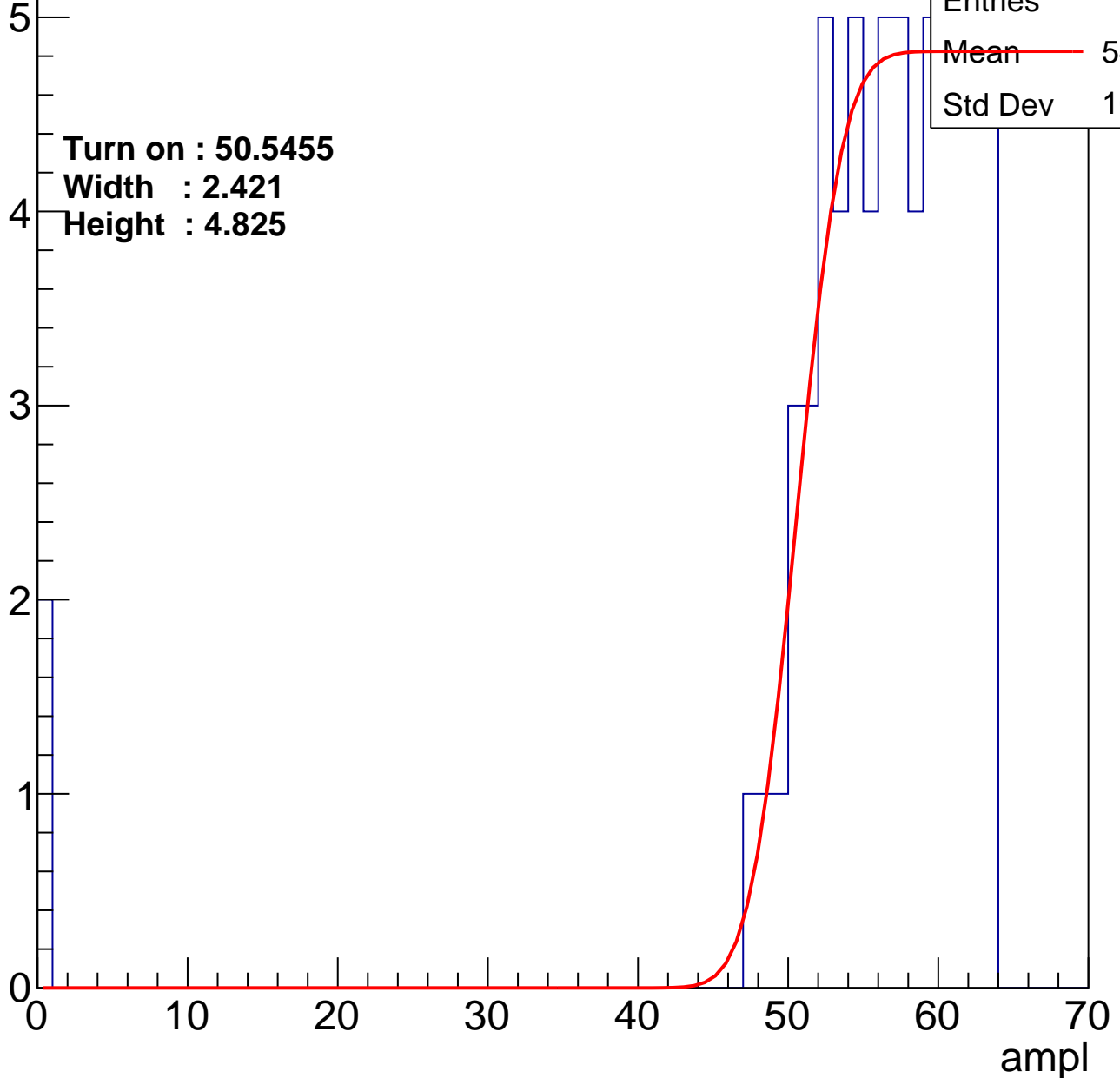
60

70

B0L103S, U15-ch116

calib_packv5_040323_1717.root, FC#2, Port C3

Entry



B0L103S, U15-ch117

calib_packv5_040323_1717.root, FC#2, Port C3

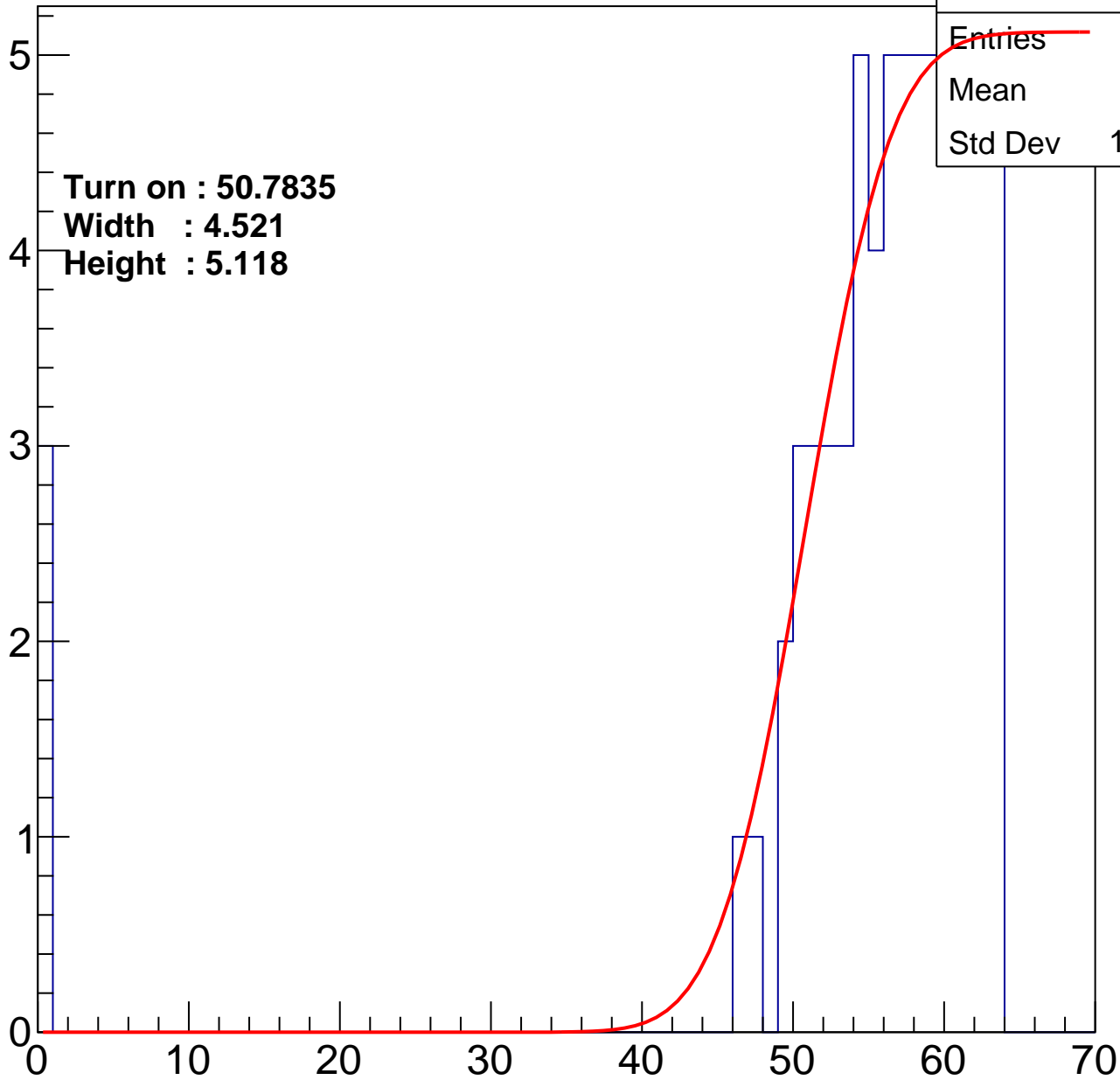
Entry

5
4
3
2
1
0

Turn on : 50.7835
Width : 4.521
Height : 5.118

Entries	68
Mean	54.1
Std Dev	12.38

ampl



B0L103S, U15-ch118

calib_packv5_040323_1717.root, FC#2, Port C3

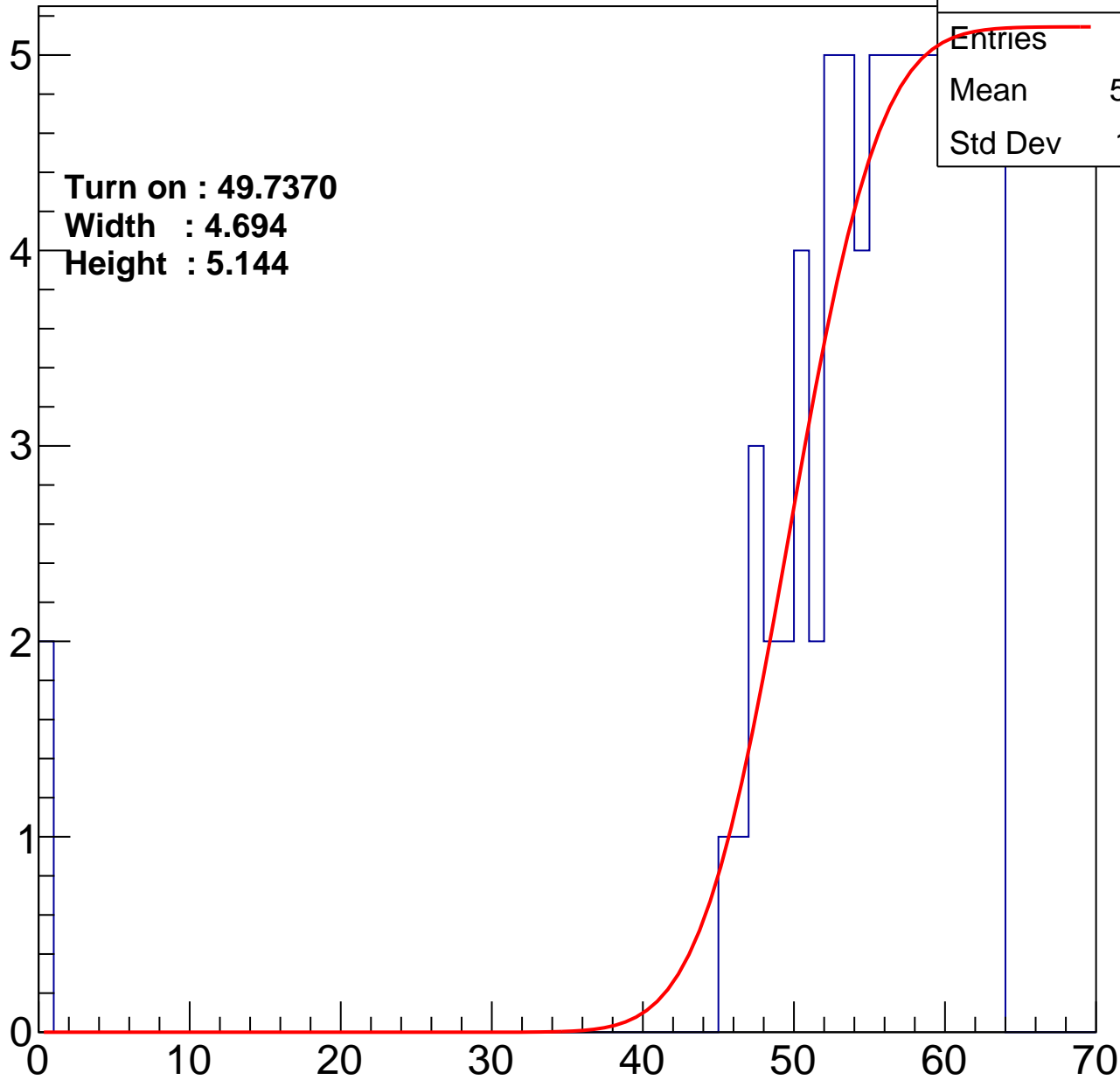
Entry

5
4
3
2
1
0

Turn on : 49.7370
Width : 4.694
Height : 5.144

Entries	76
Mean	54.26
Std Dev	10.11

ampl



B0L103S, U15-ch119

calib_packv5_040323_1717.root, FC#2, Port C3

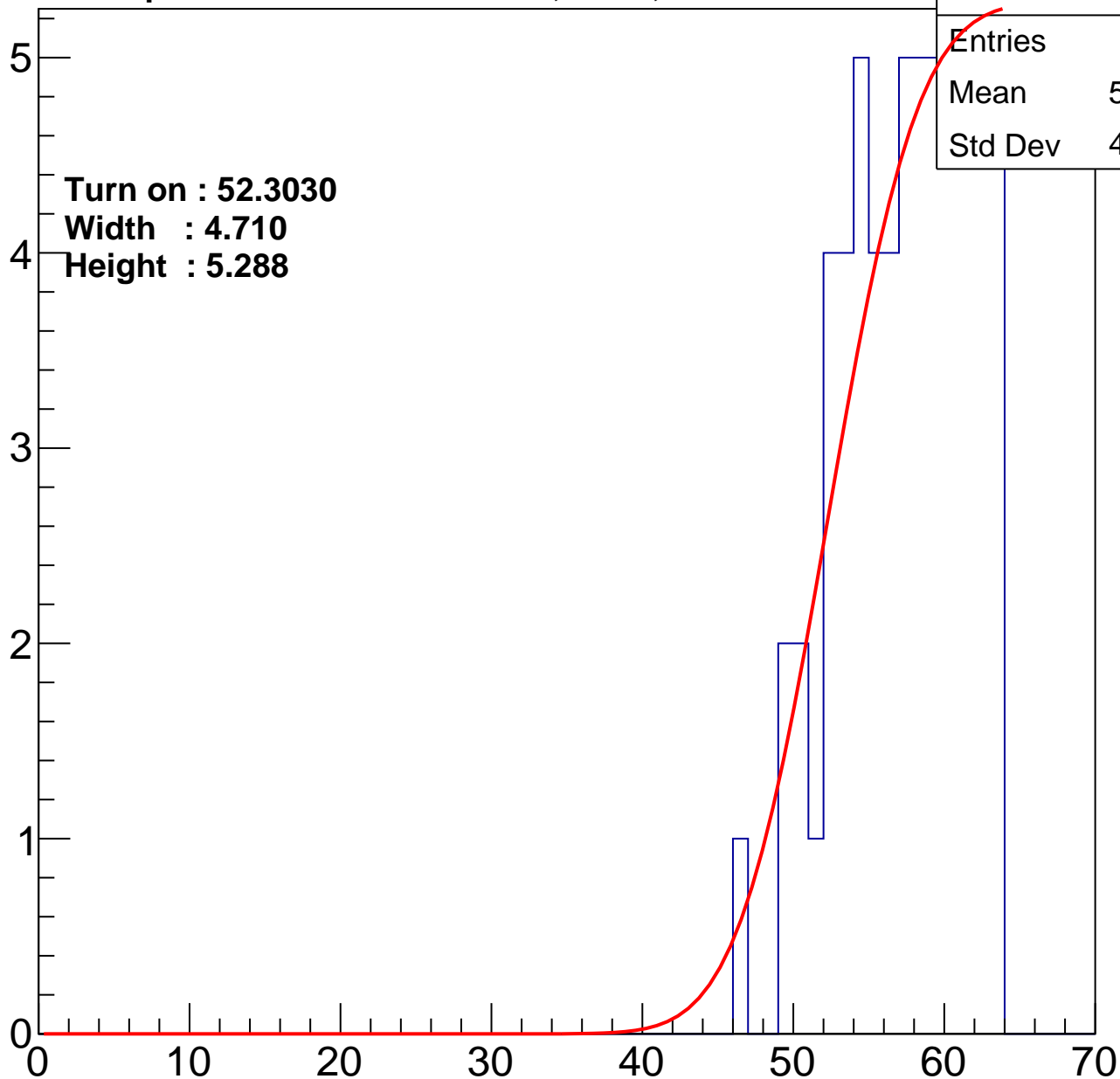
Entry

5
4
3
2
1
0

Turn on : 52.3030
Width : 4.710
Height : 5.288

Entries	62
Mean	56.92
Std Dev	4.148

ampl



B0L103S, U15-ch120

calib_packv5_040323_1717.root, FC#2, Port C3

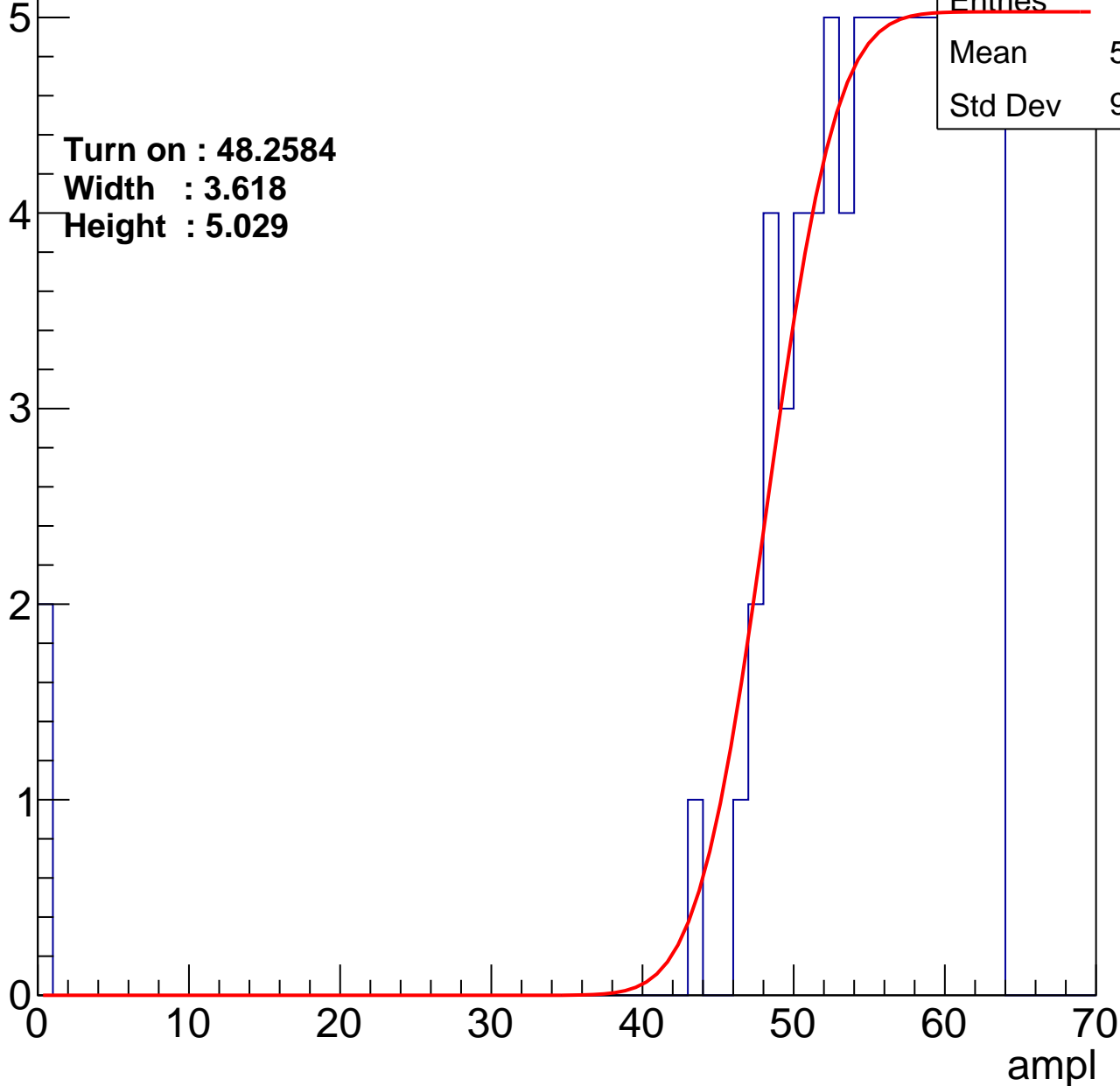
Entry

Entries	80
Mean	54.04
Std Dev	9.927

Turn on : 48.2584

Width : 3.618

Height : 5.029



B0L103S, U15-ch121

calib_packv5_040323_1717.root, FC#2, Port C3

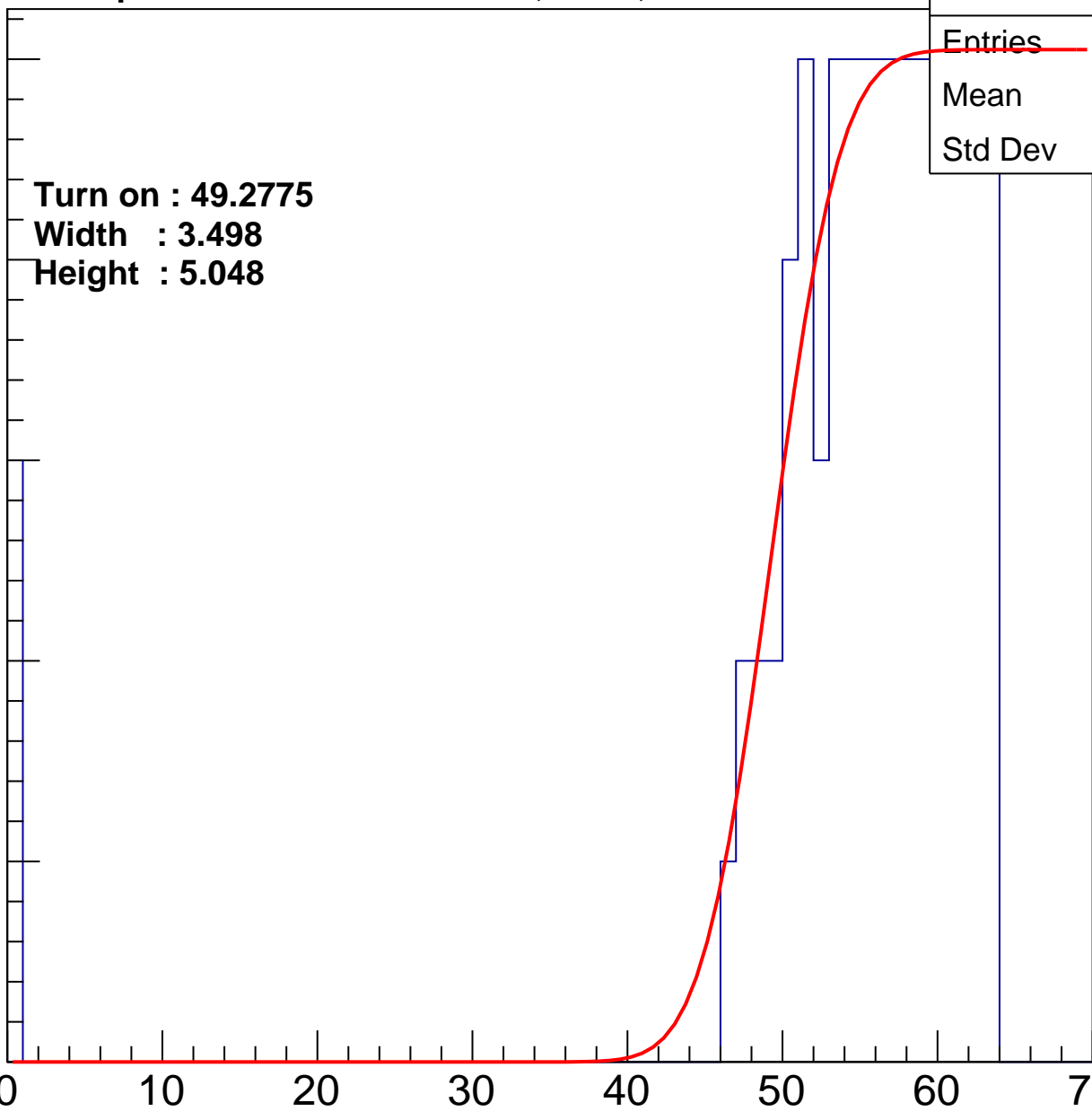
Entry

5
4
3
2
1
0

Turn on : 49.2775
Width : 3.498
Height : 5.048

Entries	77
Mean	53.7
Std Dev	11.72

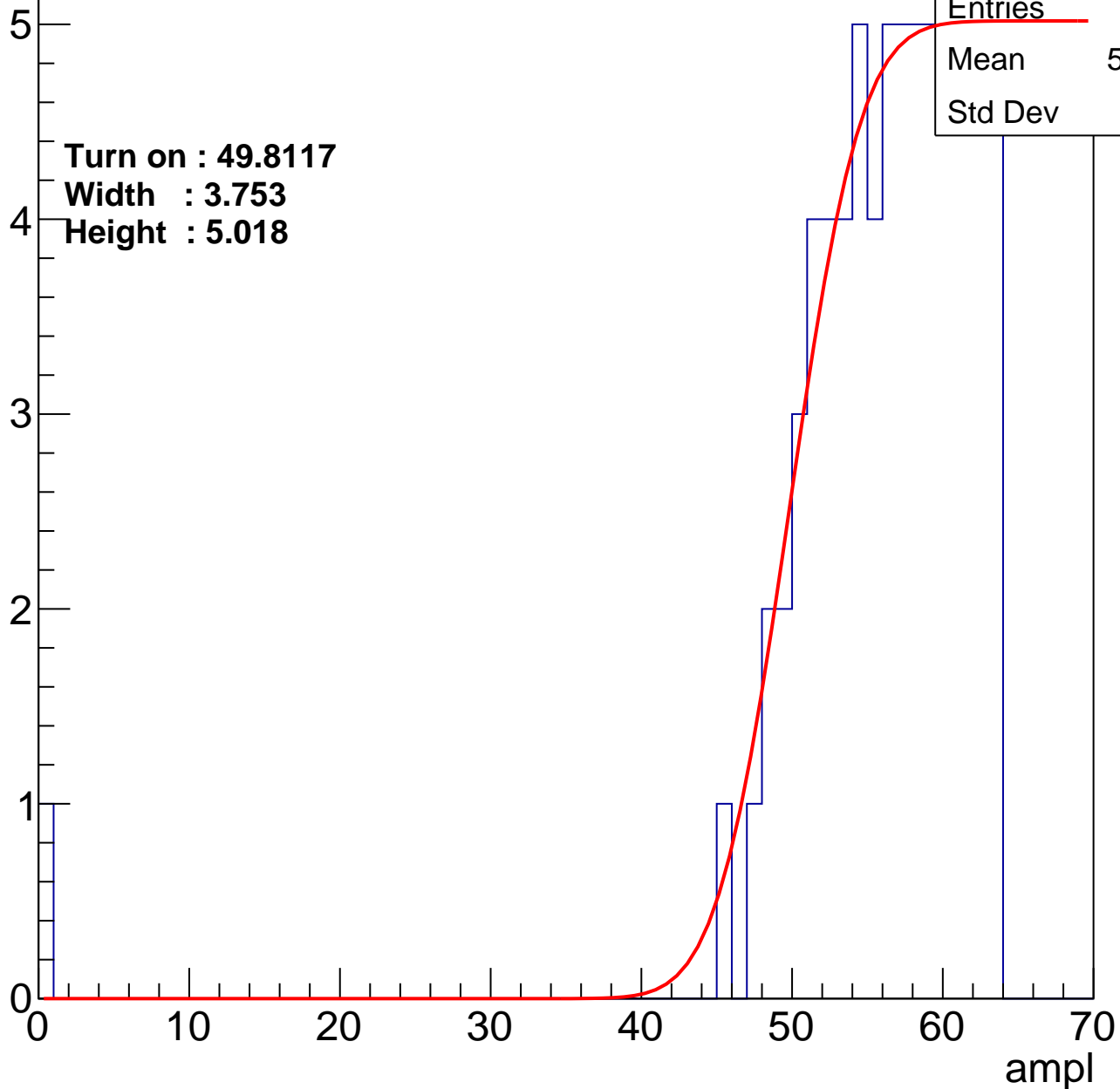
ampl



B0L103S, U15-ch122

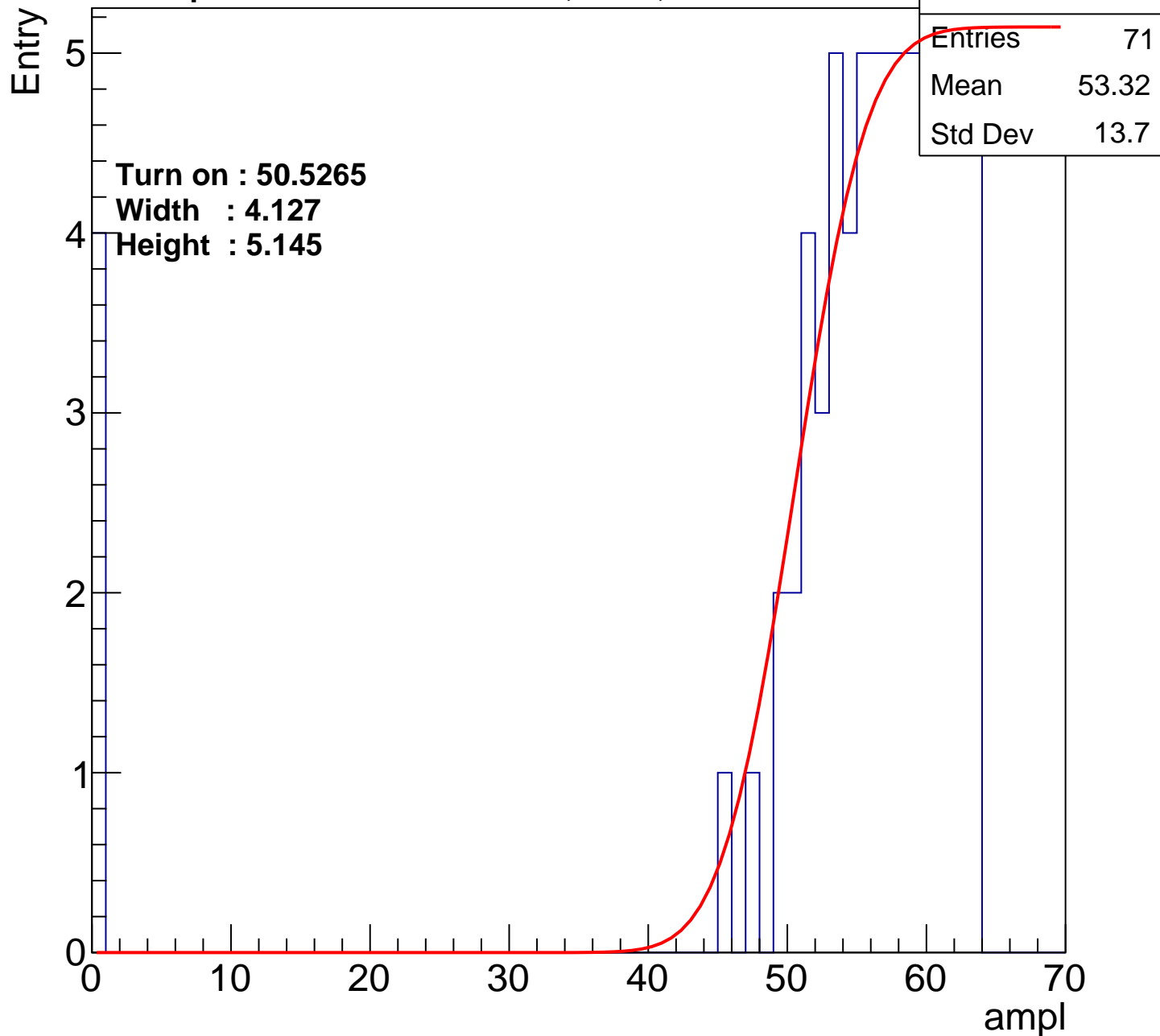
calib_packv5_040323_1717.root, FC#2, Port C3

Entry



B0L103S, U15-ch123

calib_packv5_040323_1717.root, FC#2, Port C3



B0L103S, U15-ch124

calib_packv5_040323_1717.root, FC#2, Port C3

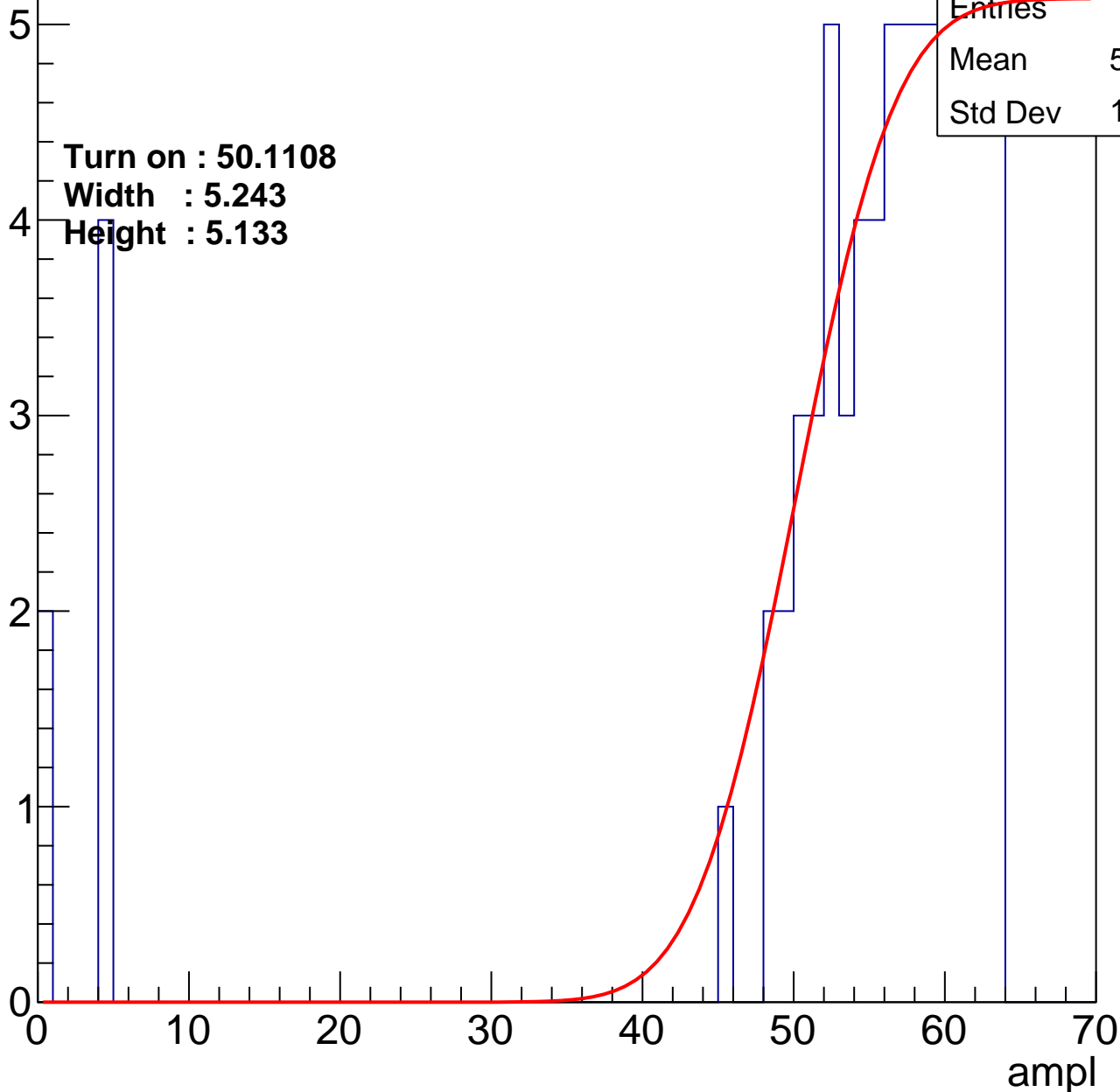
Entry

Entries	73
Mean	51.96
Std Dev	15.37

Turn on : 50.1108

Width : 5.243

Height : 5.133



B0L103S, U15-ch125

calib_packv5_040323_1717.root, FC#2, Port C3

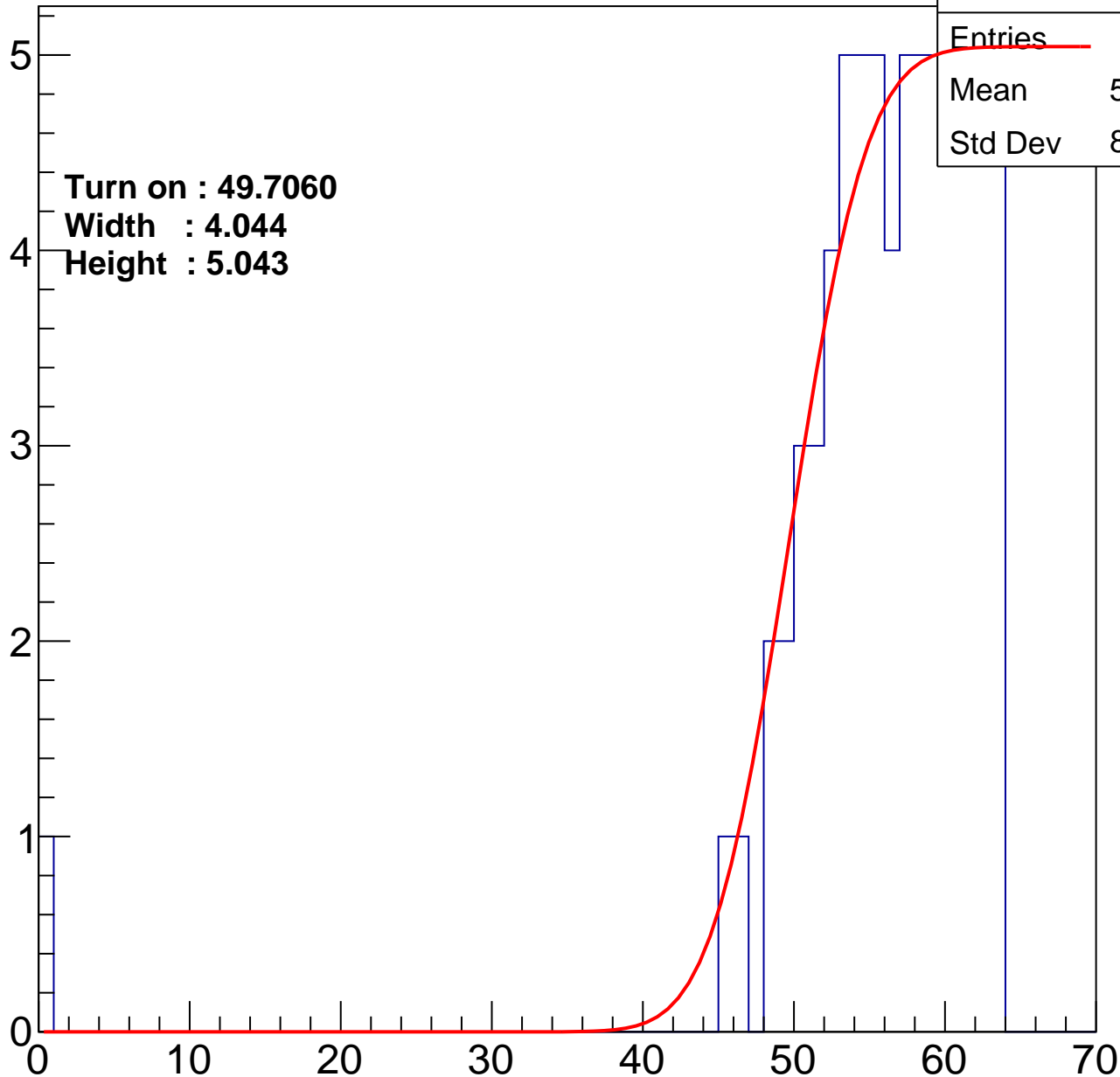
Entry

5
4
3
2
1
0

Turn on : 49.7060
Width : 4.044
Height : 5.043

Entries	71
Mean	55.35
Std Dev	8.023

ampl



B0L103S, U15-ch126

calib_packv5_040323_1717.root, FC#2, Port C3

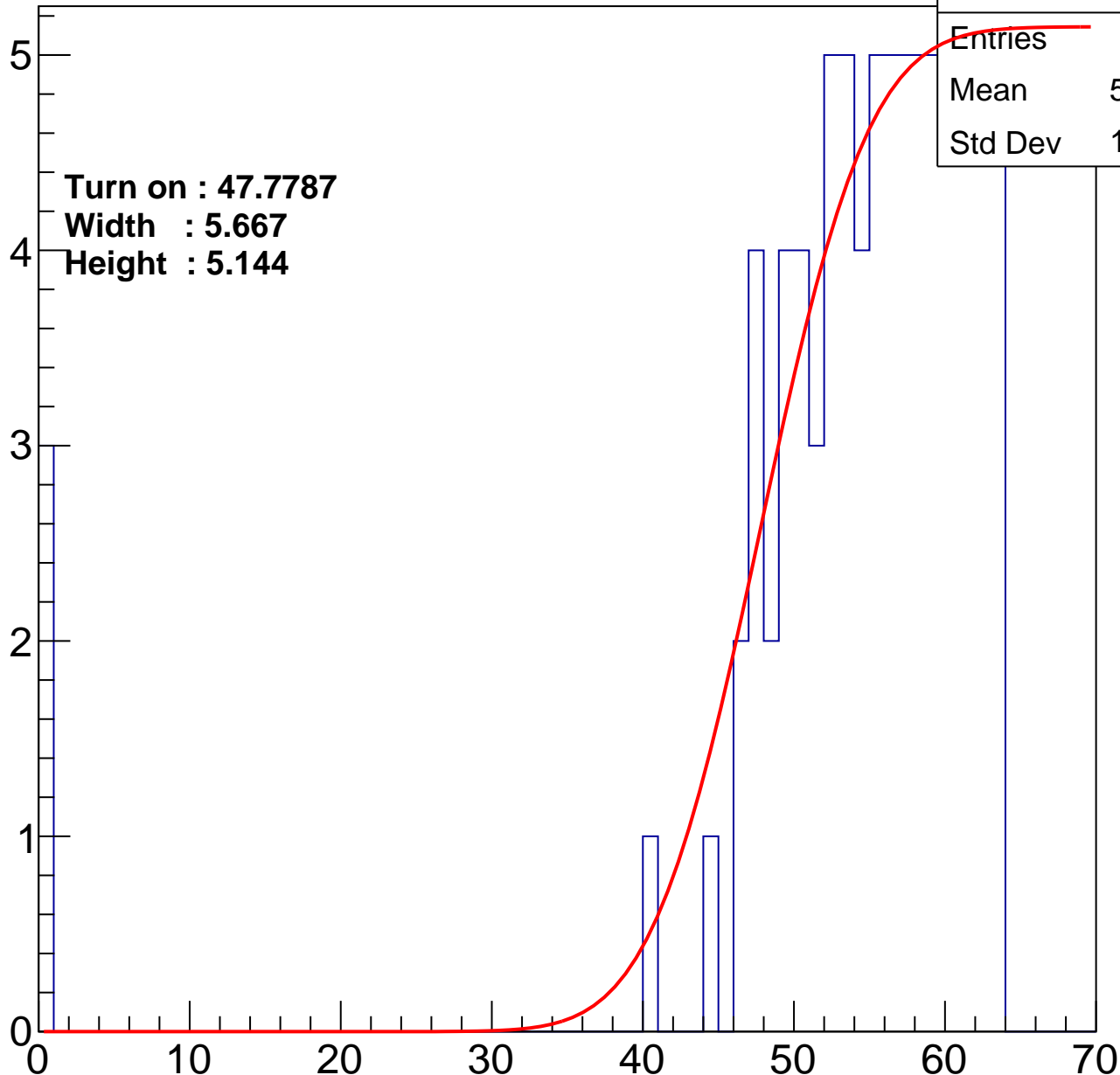
Entry

5
4
3
2
1
0

Turn on : 47.7787
Width : 5.667
Height : 5.144

Entries	83
Mean	53.07
Std Dev	11.52

ampl



B0L103S, U15-ch127

calib_packv5_040323_1717.root, FC#2, Port C3

Entry

5

4

3

2

1

0

Turn on : 50.8423

Width : 4.689

Height : 5.243

Entries	70
Mean	55.43
Std Dev	8.07

ampl

0

10

20

30

40

50

60

70

