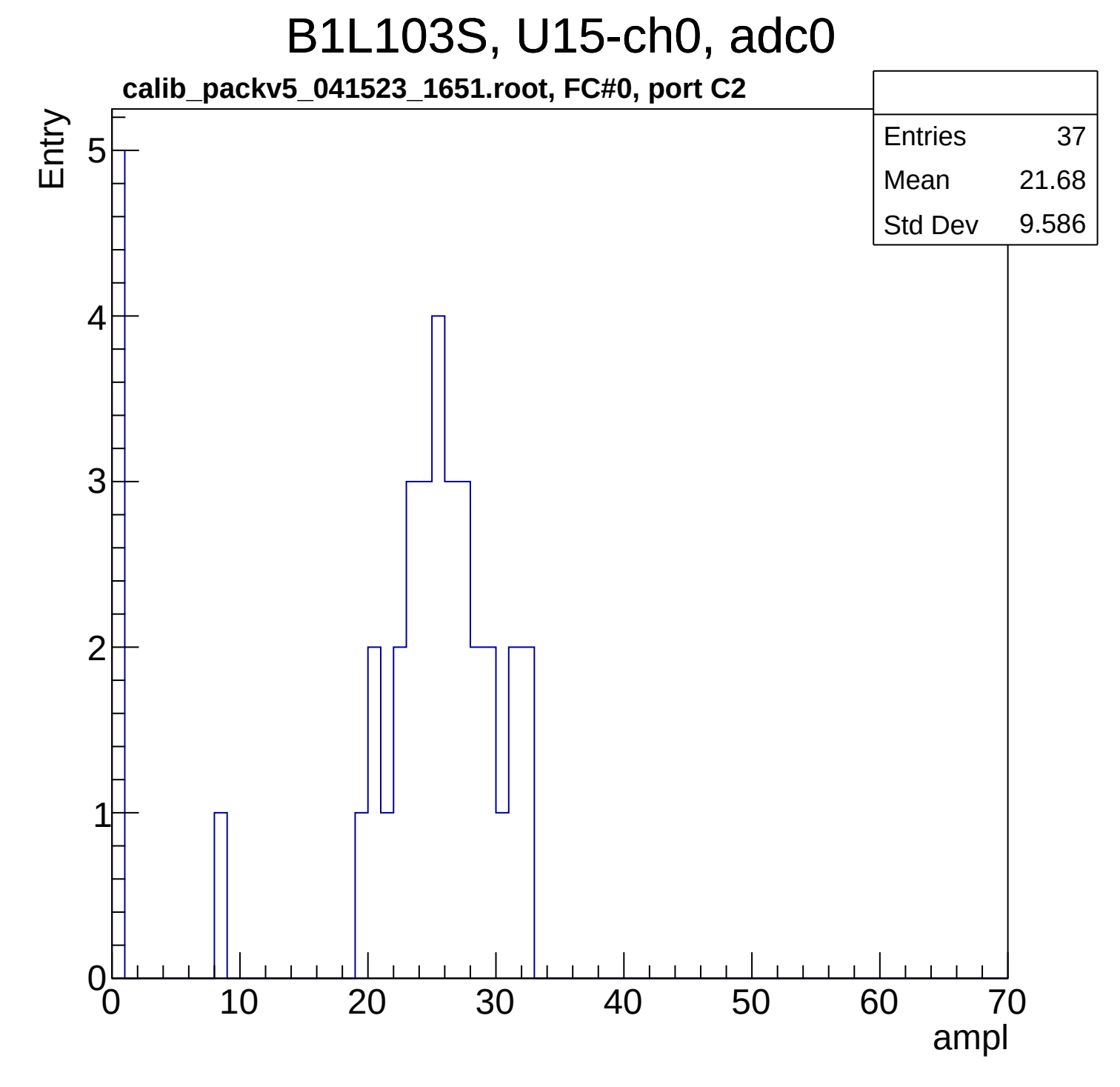
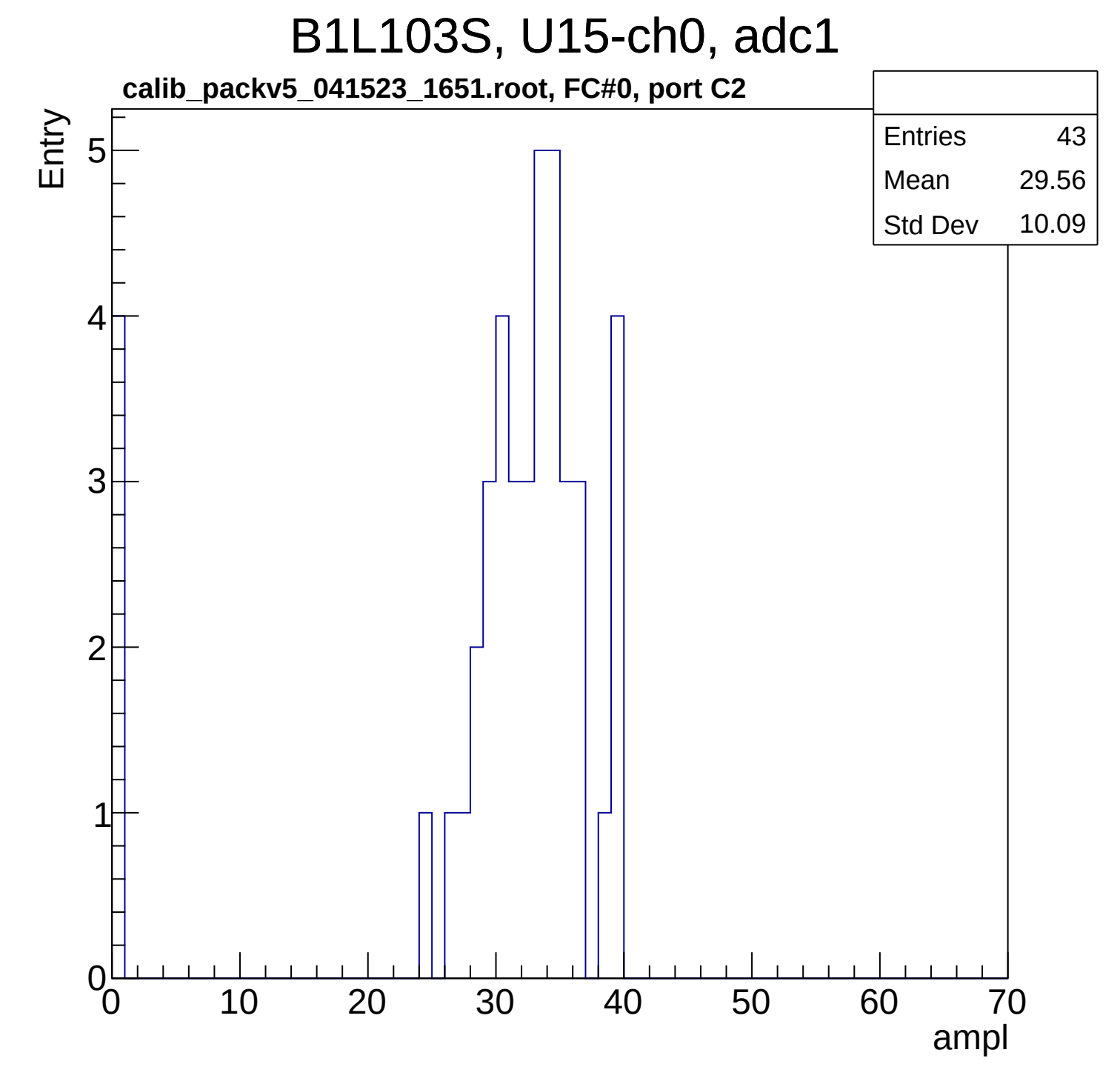
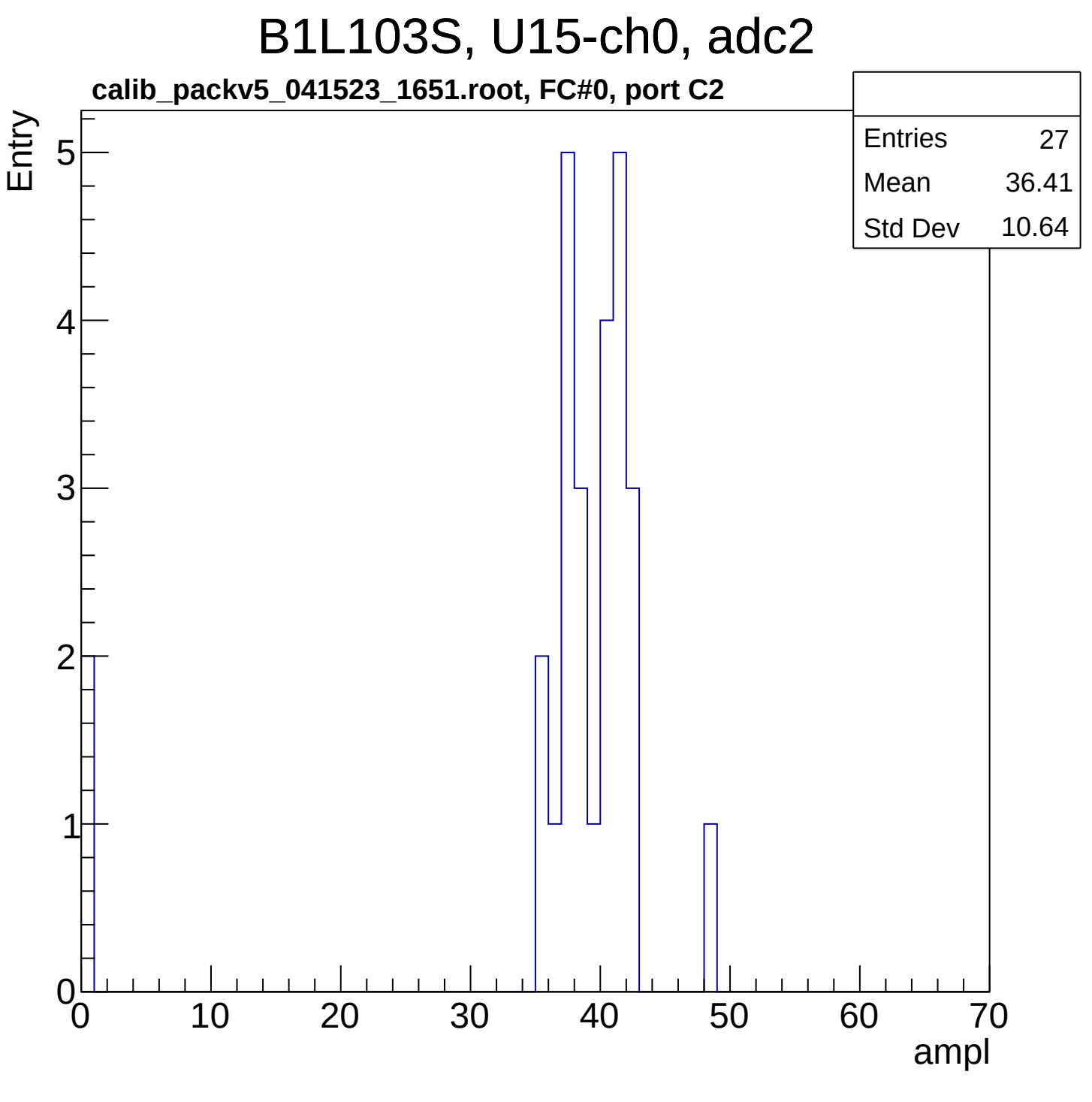
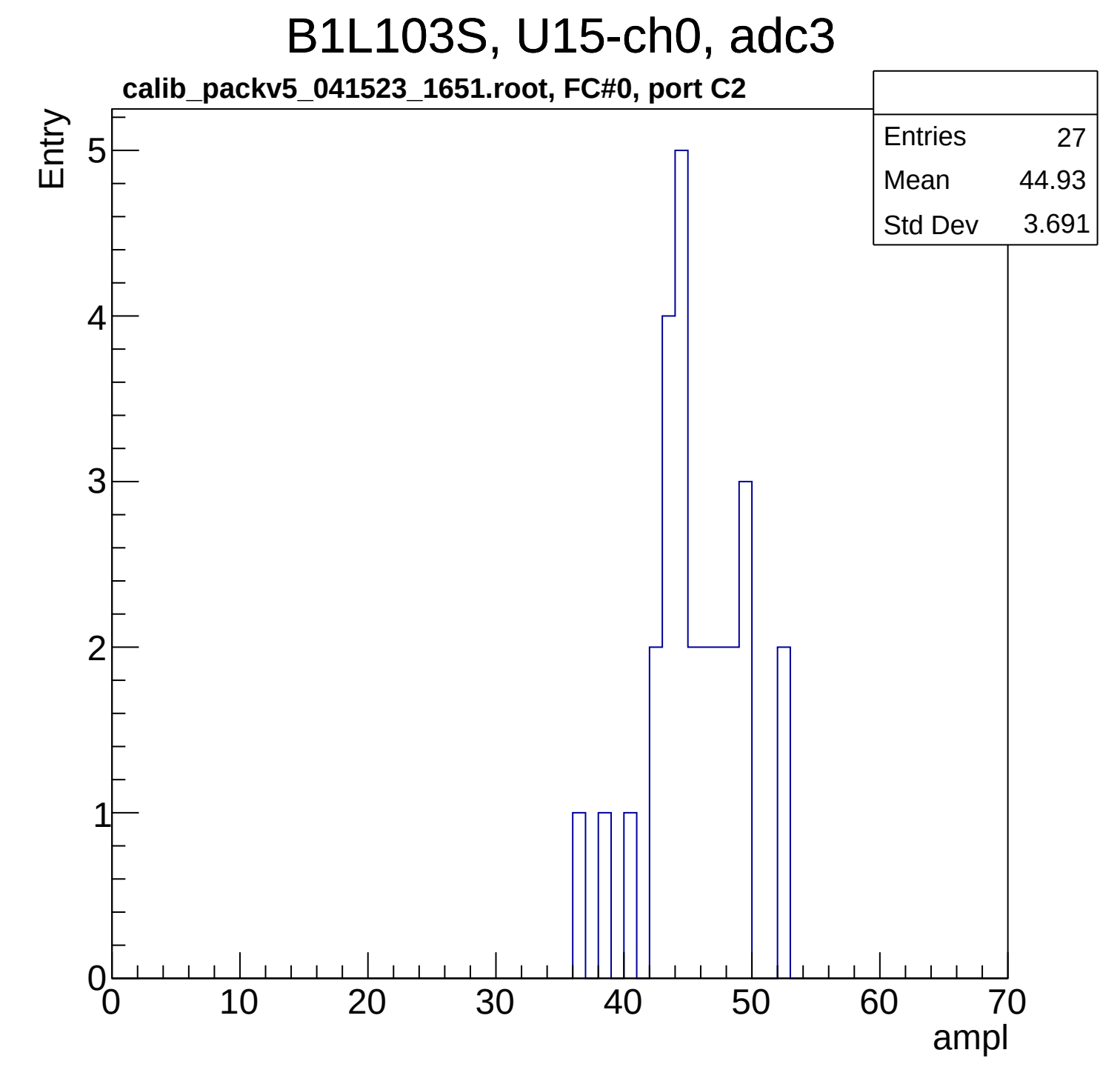
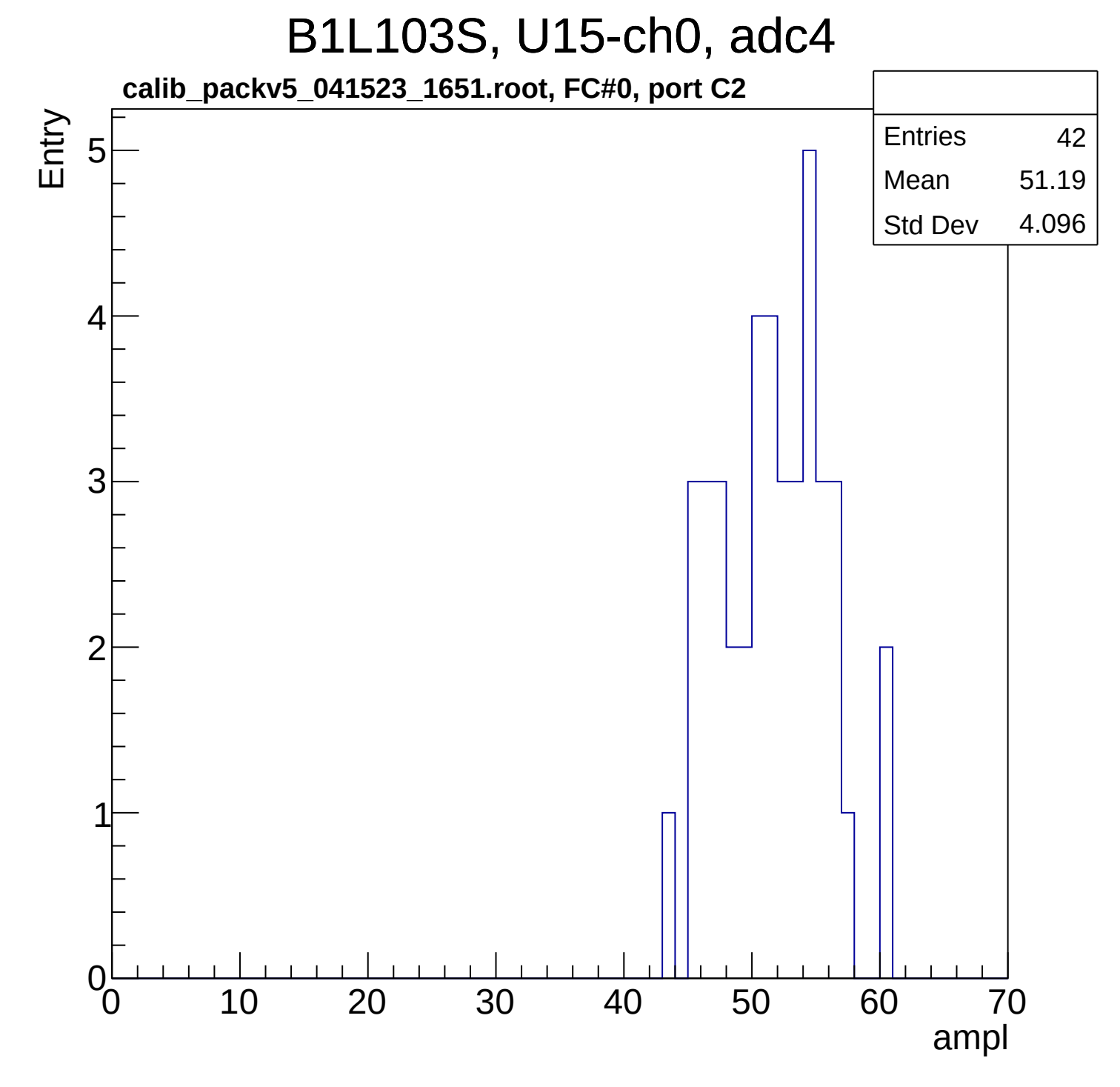
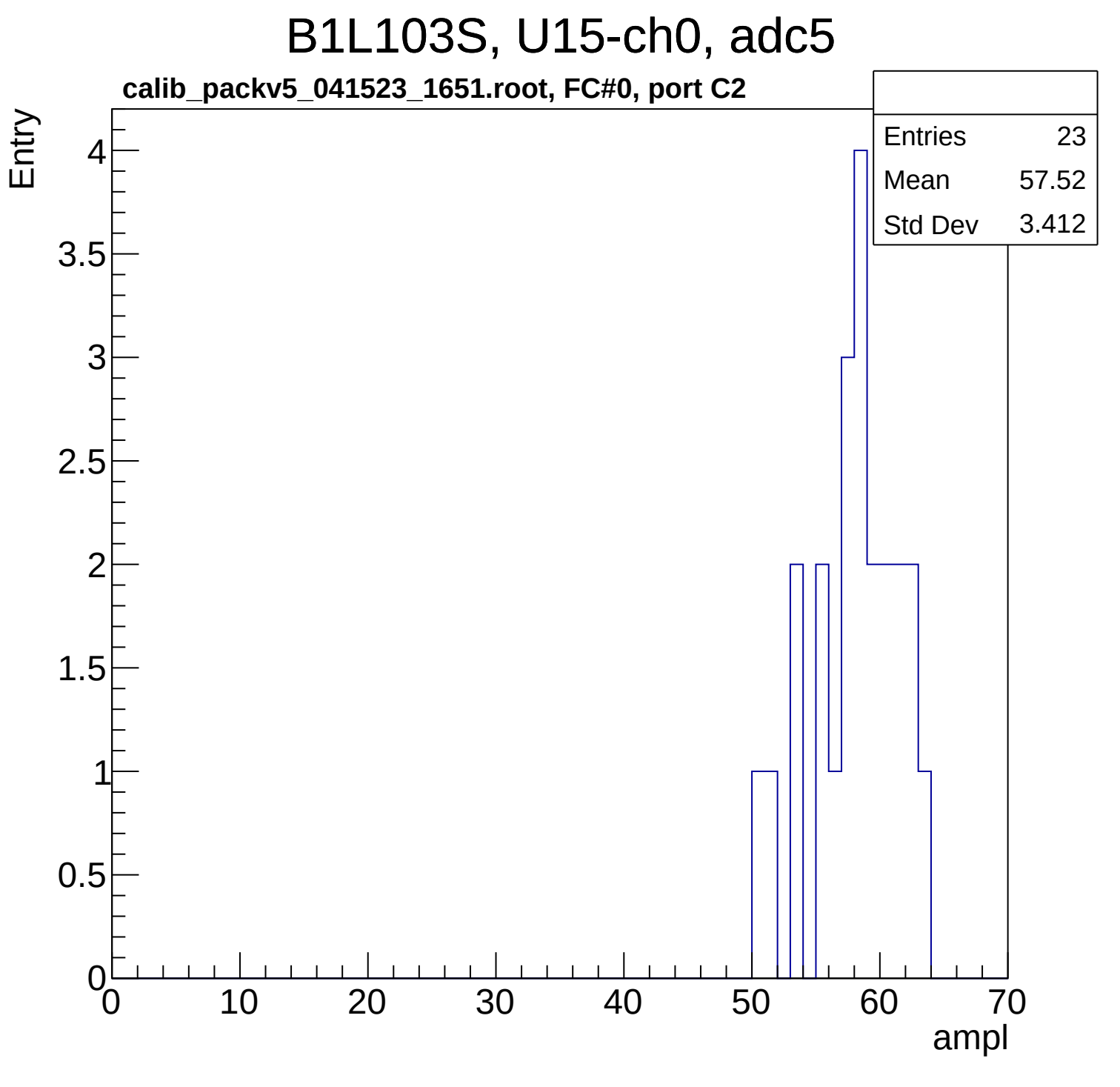

B1L103S, U15-ch0, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 21.68
Std Dev 9.586
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch0, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 29.56
Std Dev 10.09
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch0, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 36.41
Std Dev 10.64
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch0, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 44.93
Std Dev 3.691
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch0, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 51.19
Std Dev 4.096
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch0, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 57.52
Std Dev 3.412
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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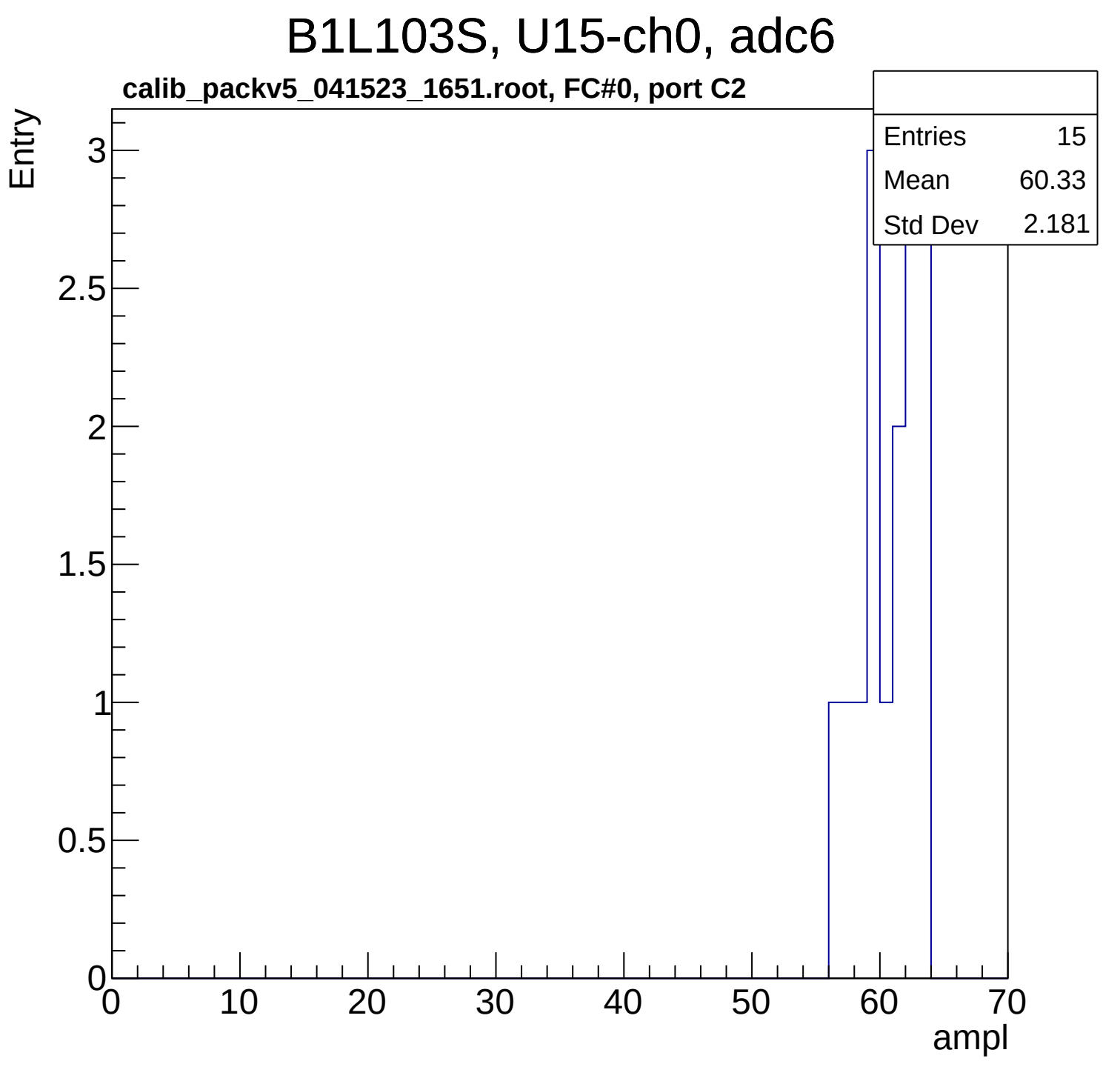
B1L103S, U15-ch0, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 60.33
Std Dev 2.181
Entry
ampl
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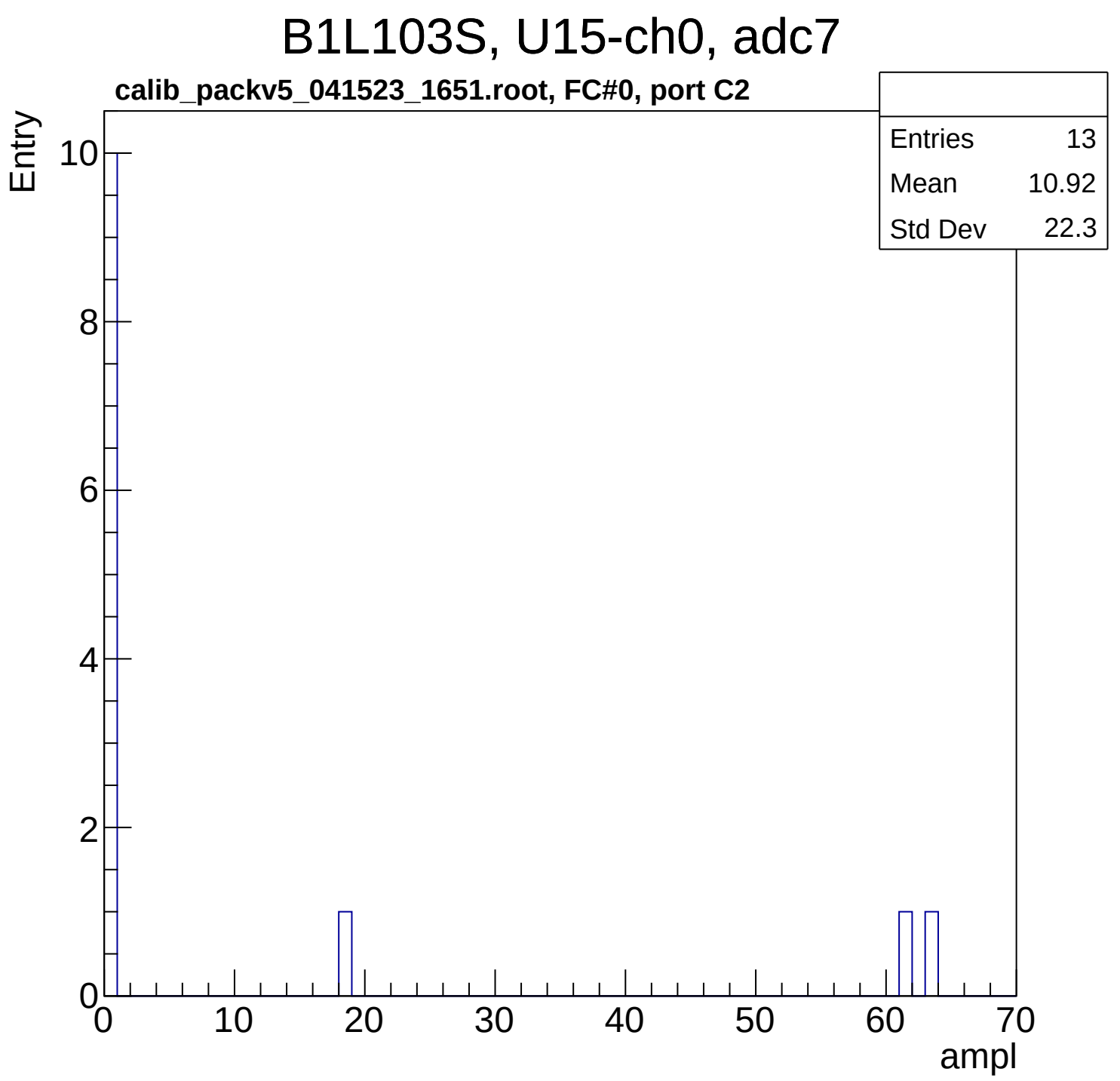
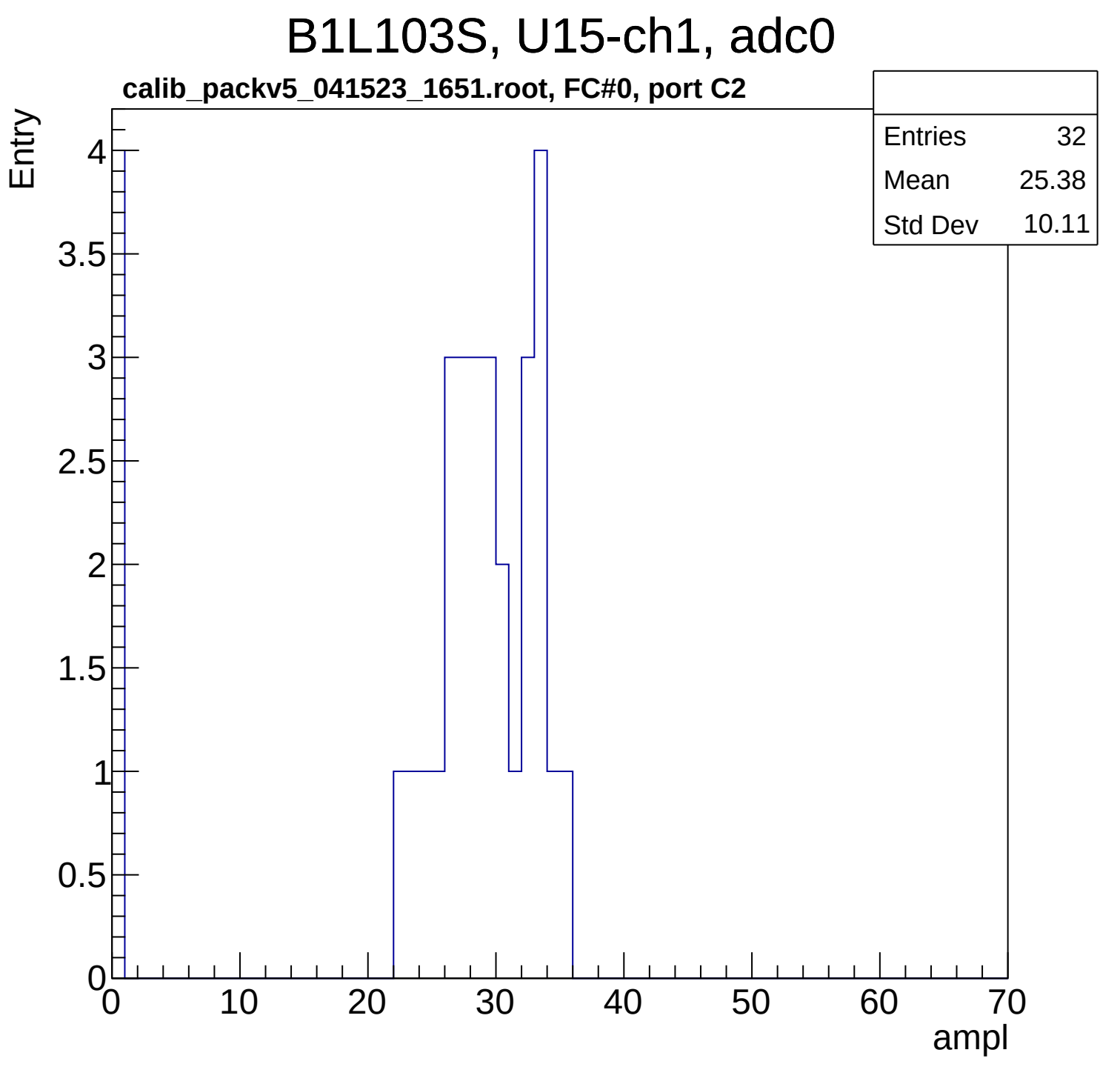
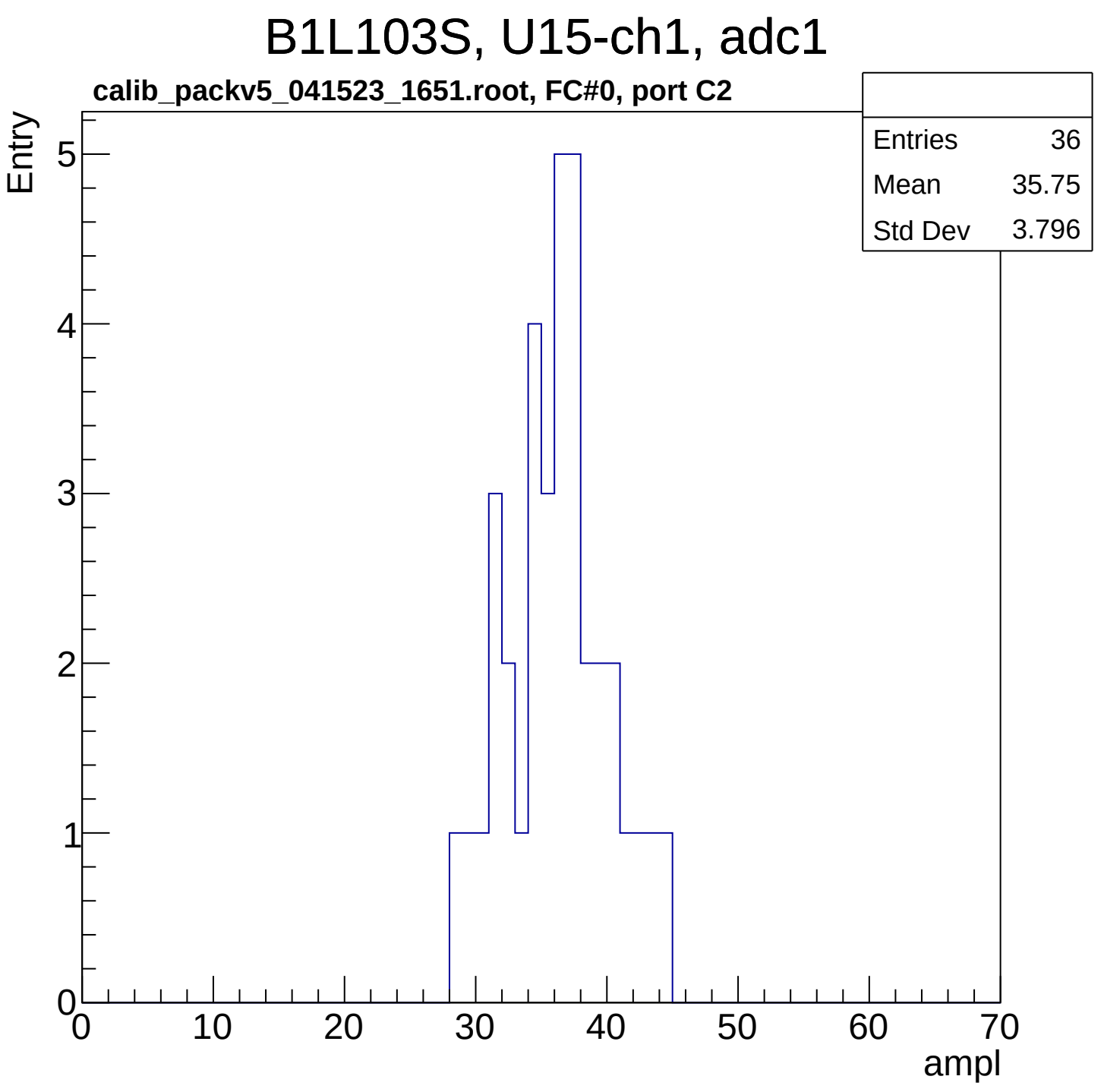
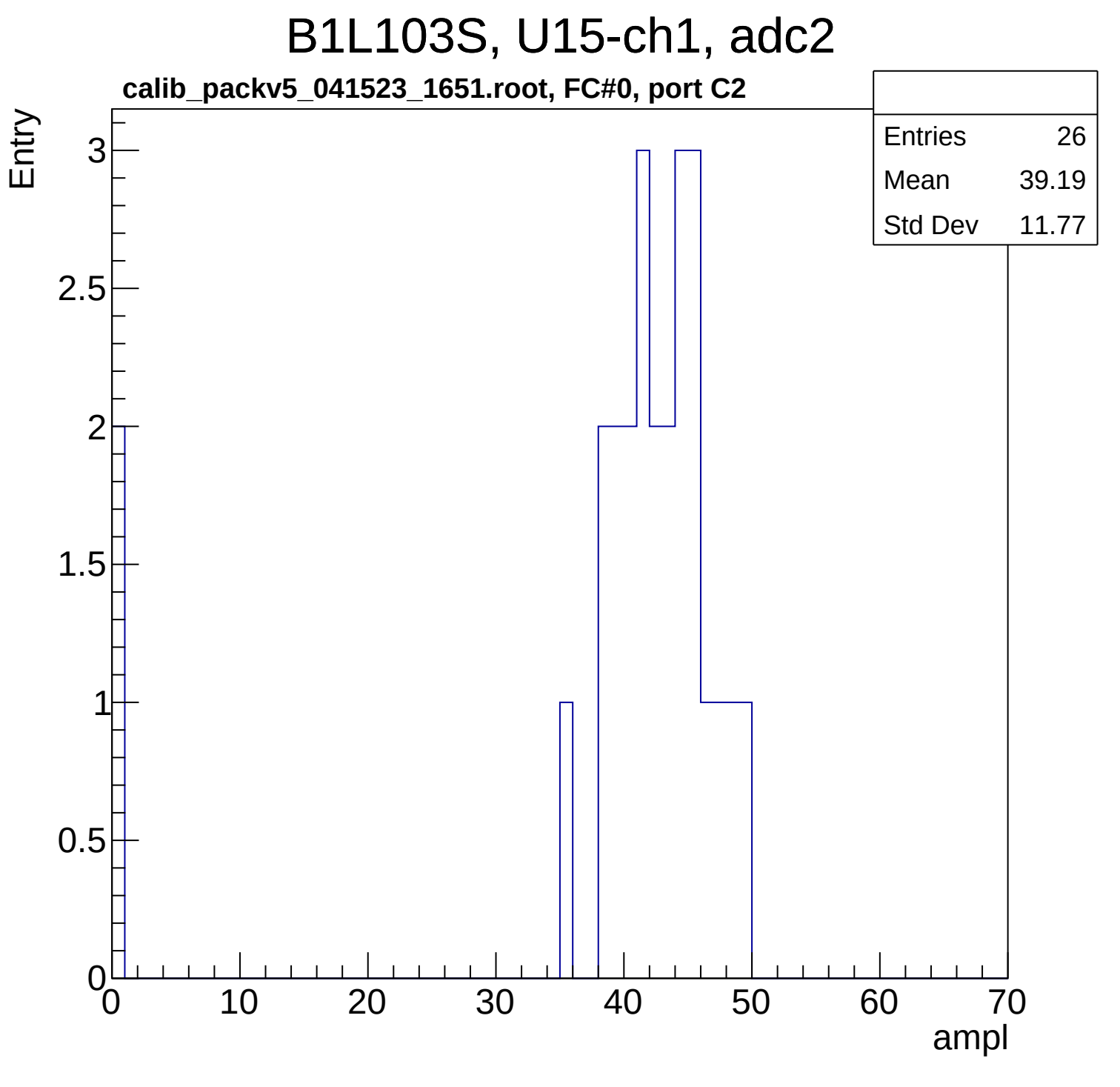
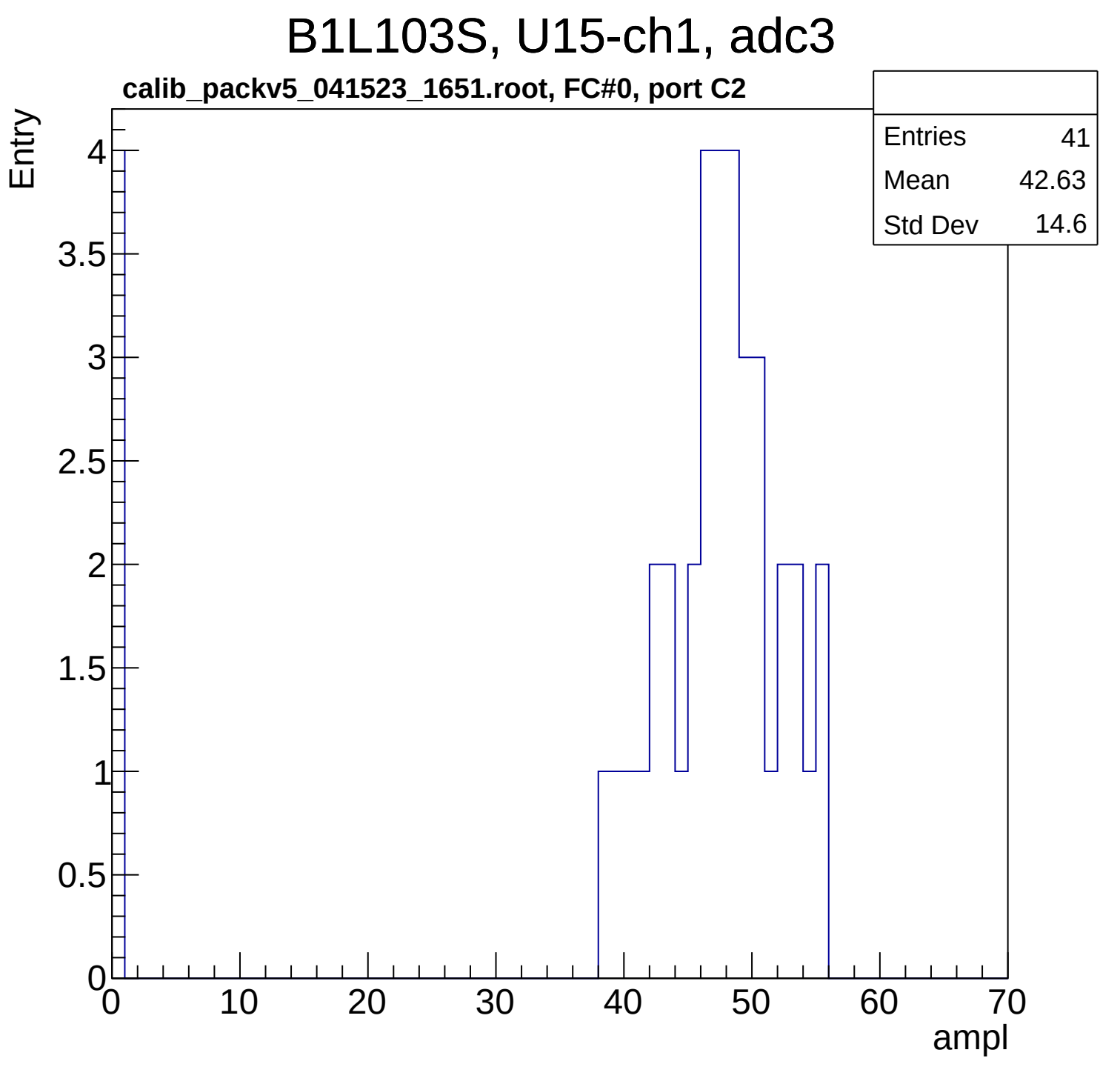
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch0, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 10.92
Std Dev 22.3
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch1, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 25.38
Std Dev 10.11
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch1, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 35.75
Std Dev 3.796
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch1, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 39.19
Std Dev 11.77
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch1, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 42.63
Std Dev 14.6
Entry
ampl
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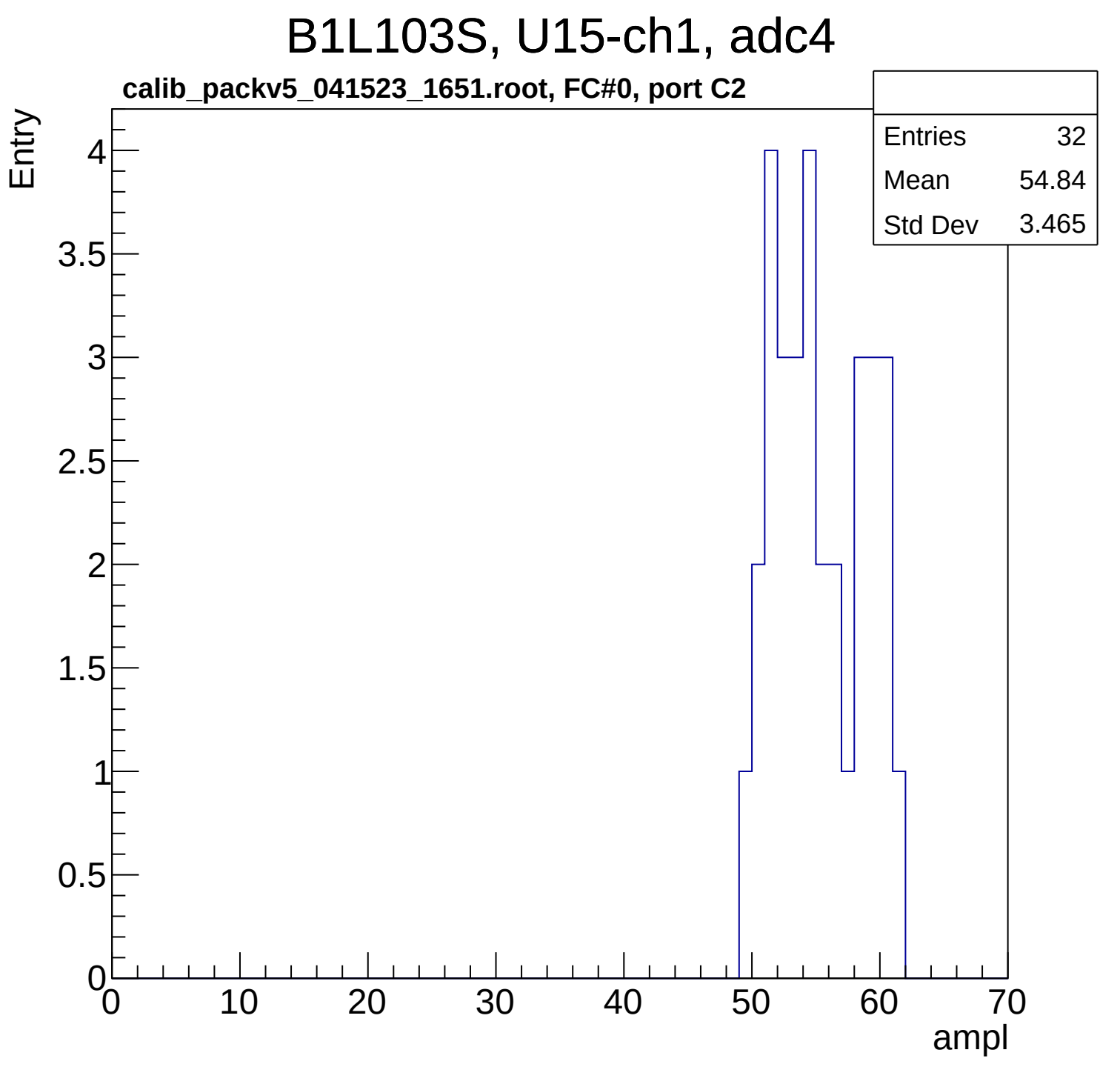
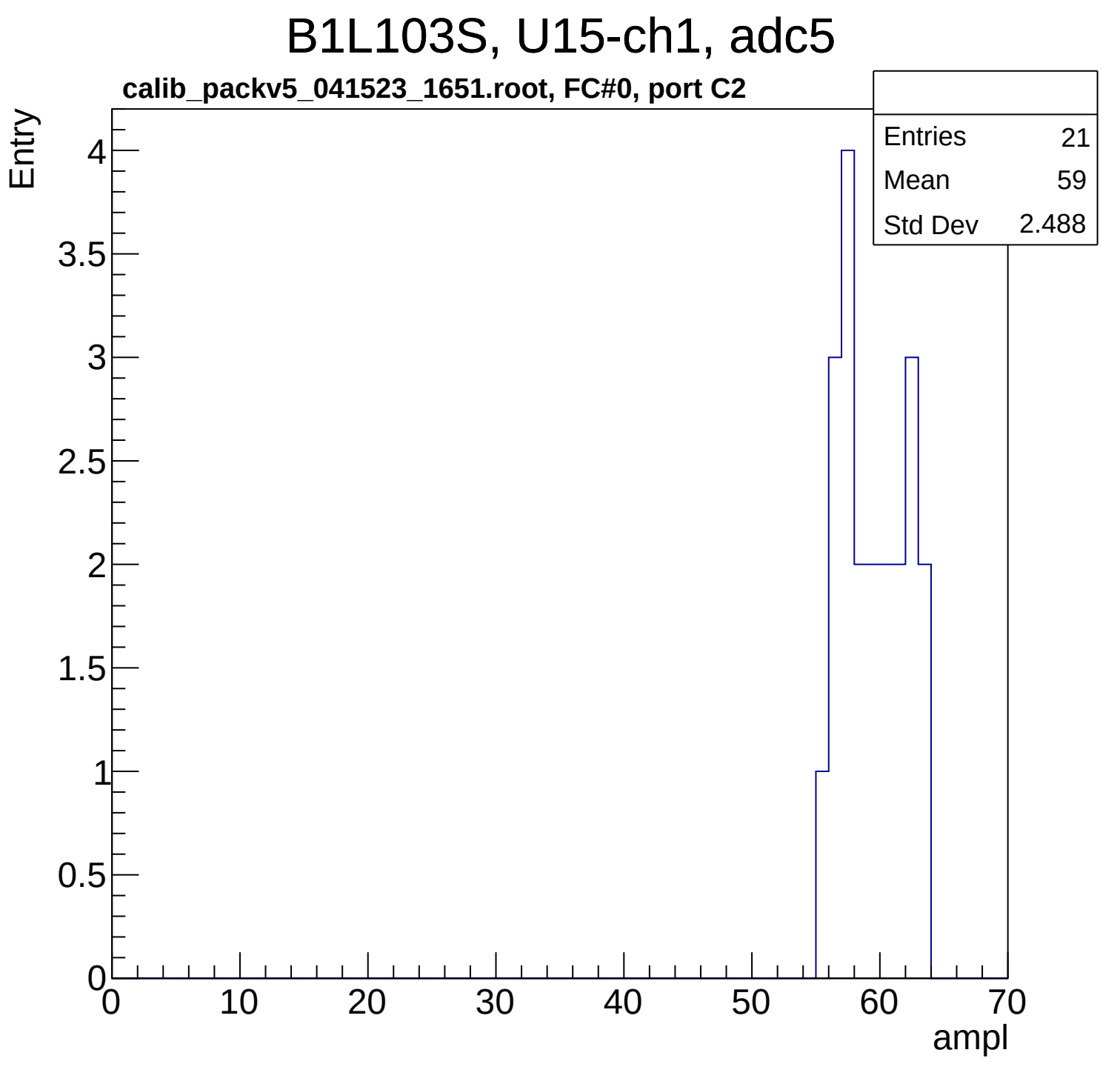
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch1, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 54.84
Std Dev 3.465
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch1, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 59
Std Dev 2.488
Entry
ampl
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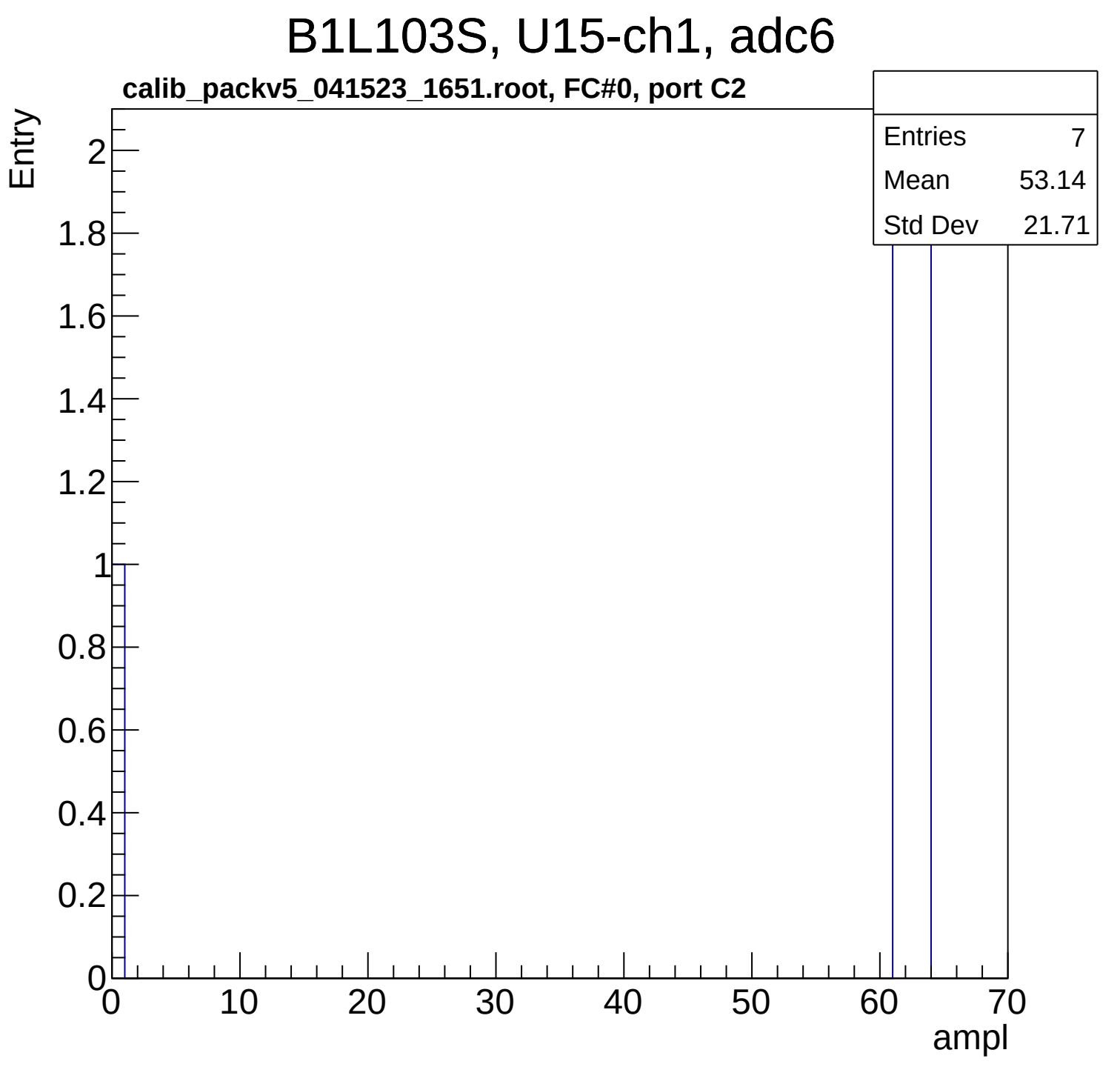
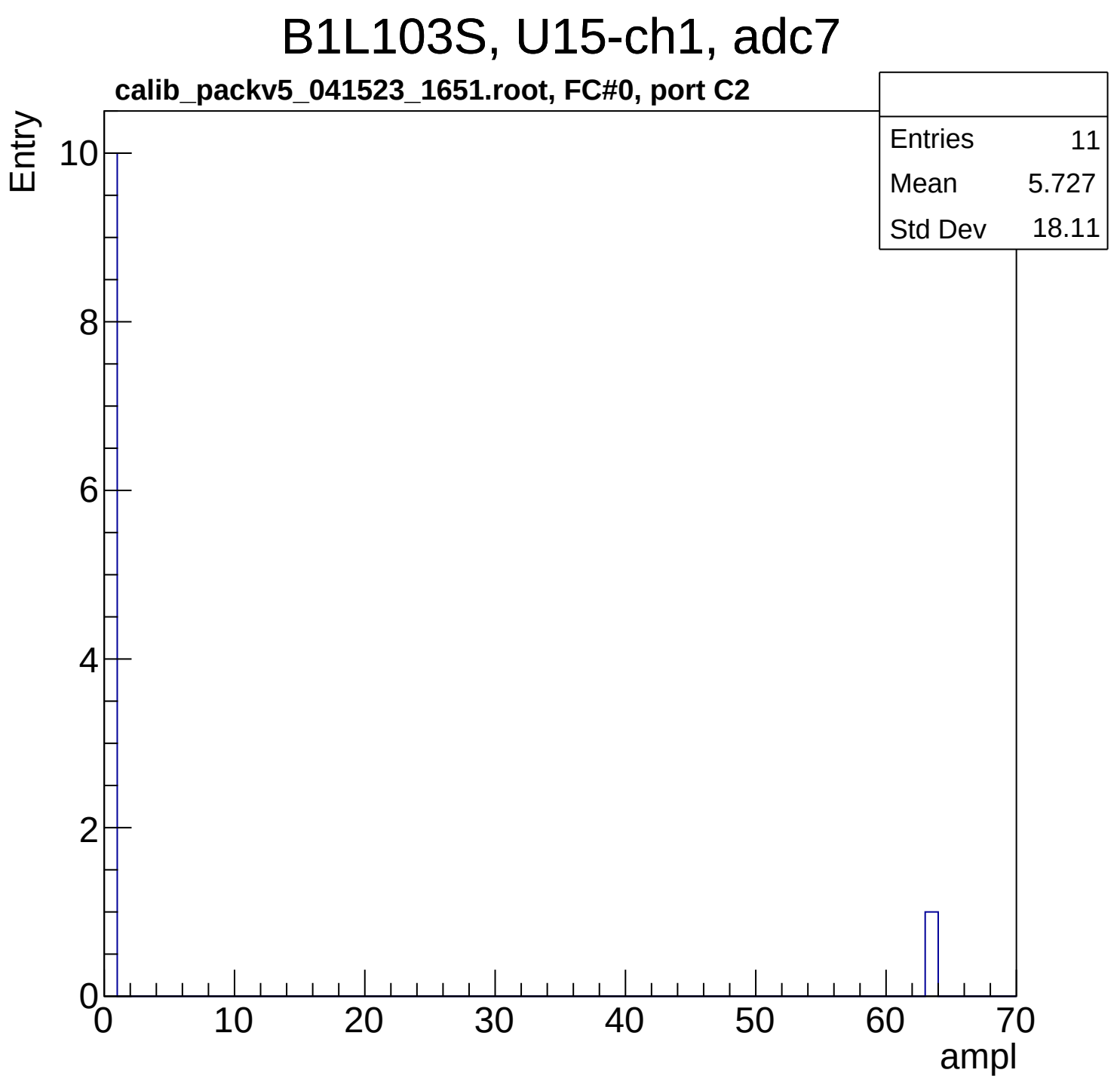
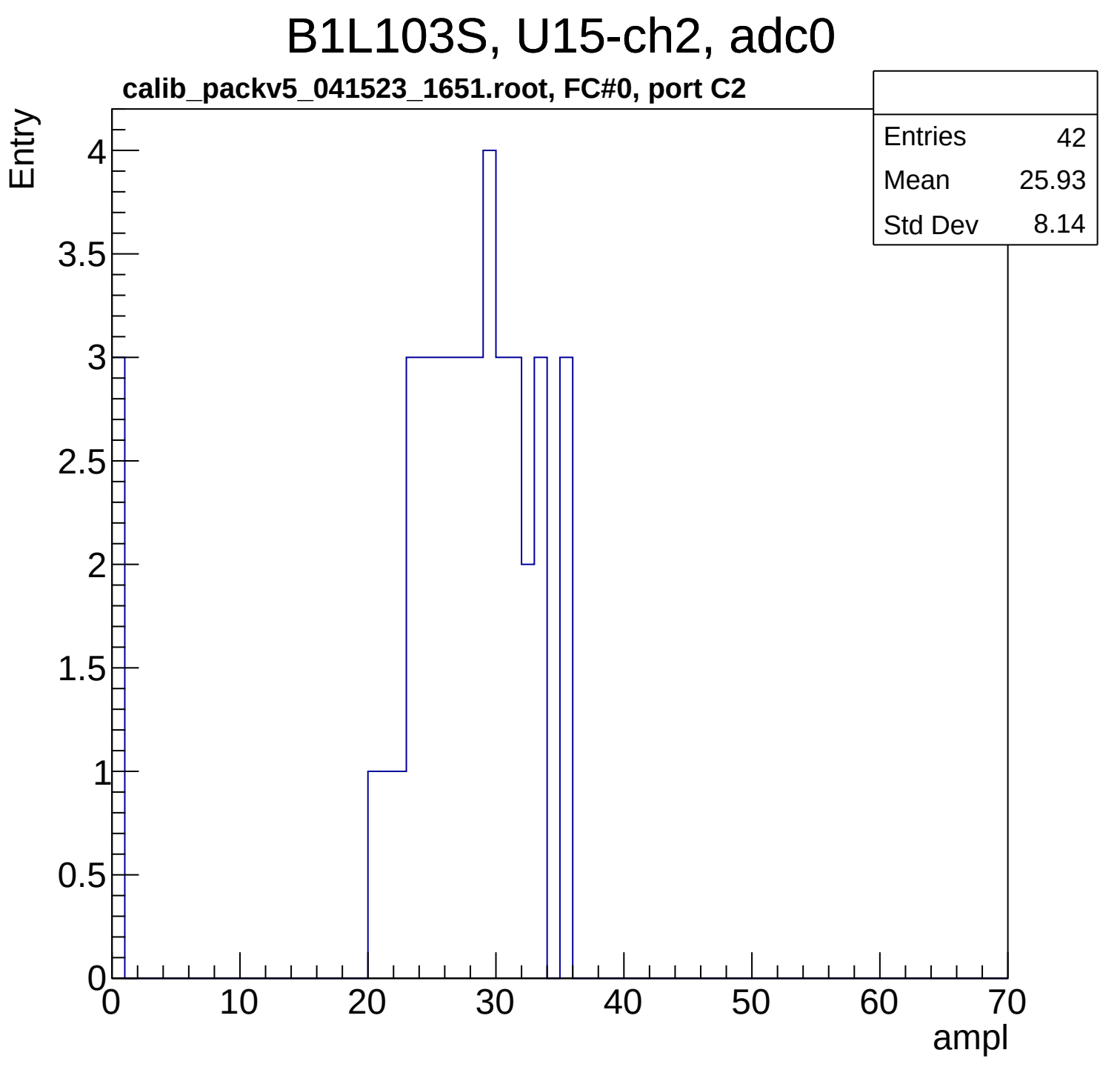
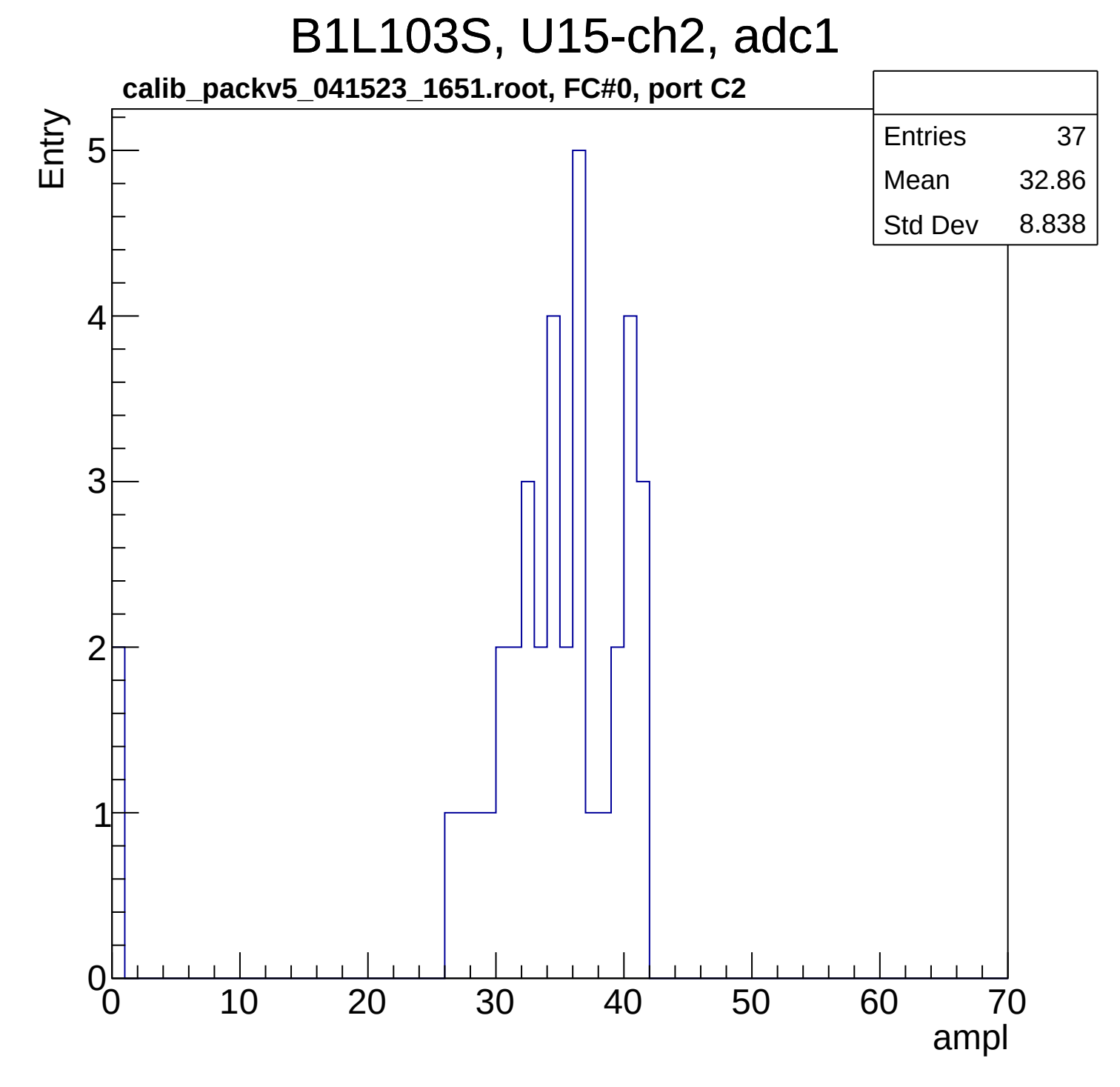
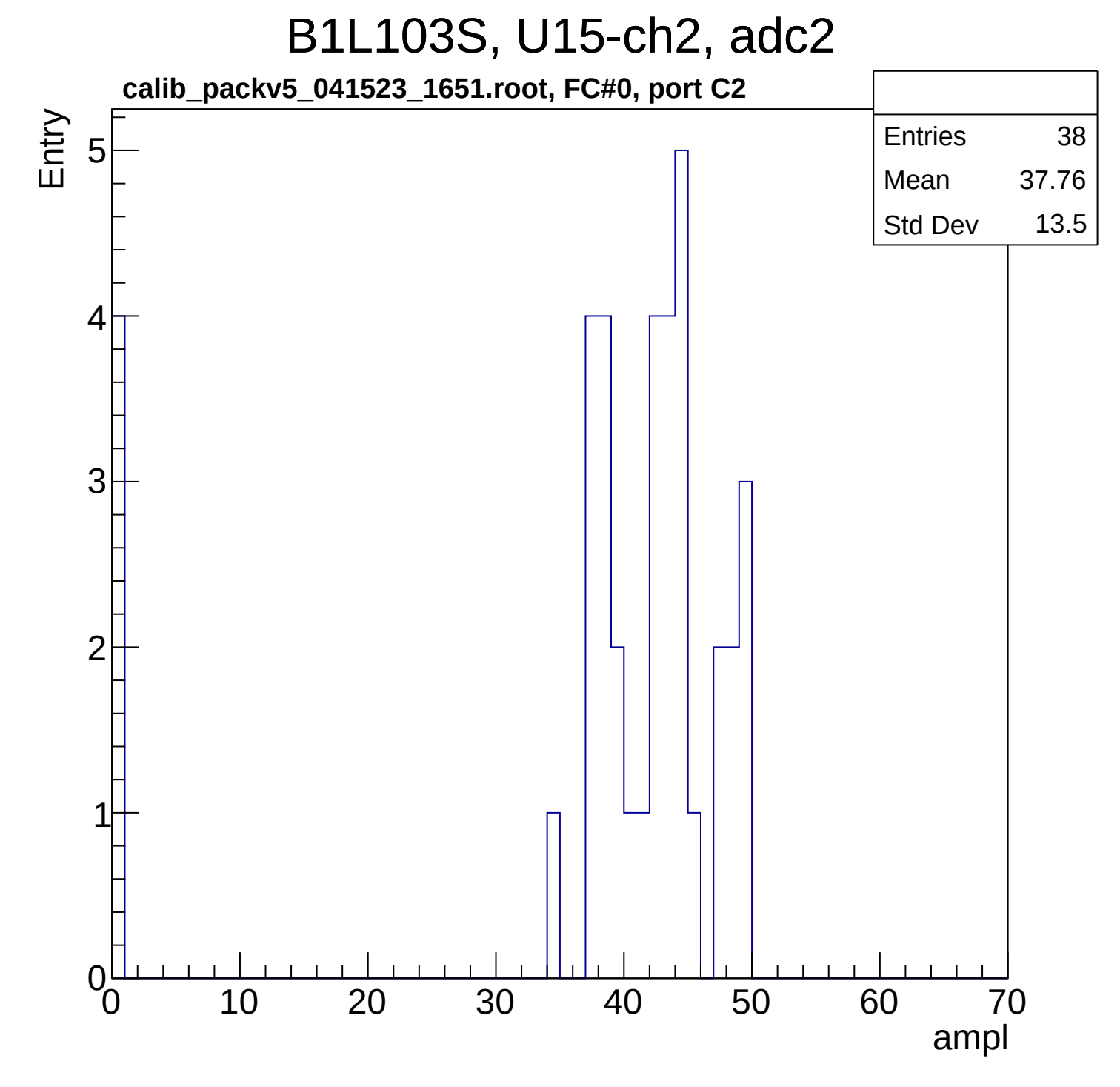
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

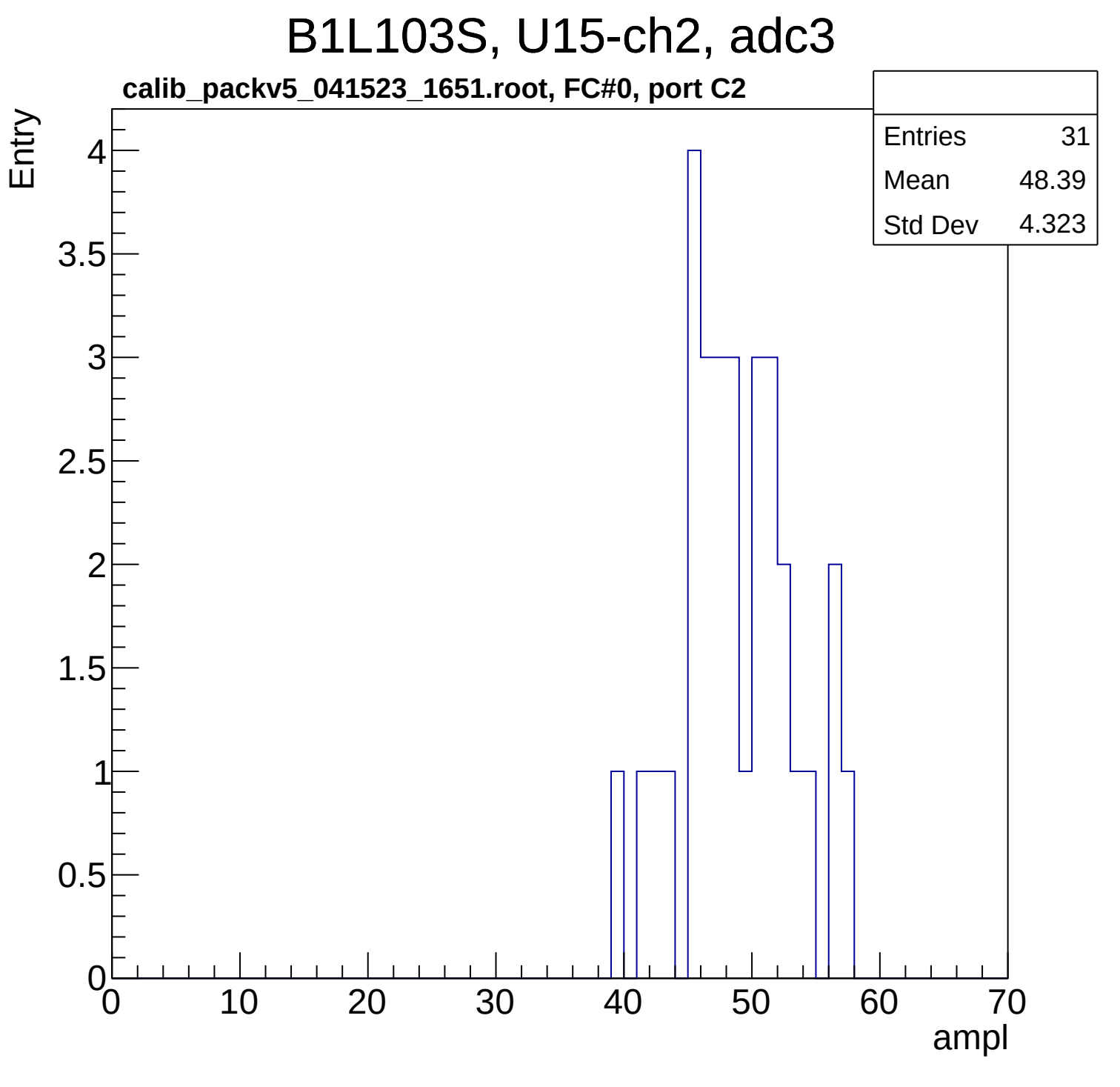

B1L103S, U15-ch1, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 53.14
Std Dev 21.71
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U15-ch1, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 5.727
Std Dev 18.11
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch2, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 25.93
Std Dev 8.14
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch2, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 32.86
Std Dev 8.838
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch2, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 37.76
Std Dev 13.5
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch2, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 48.39
Std Dev 4.323
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
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60
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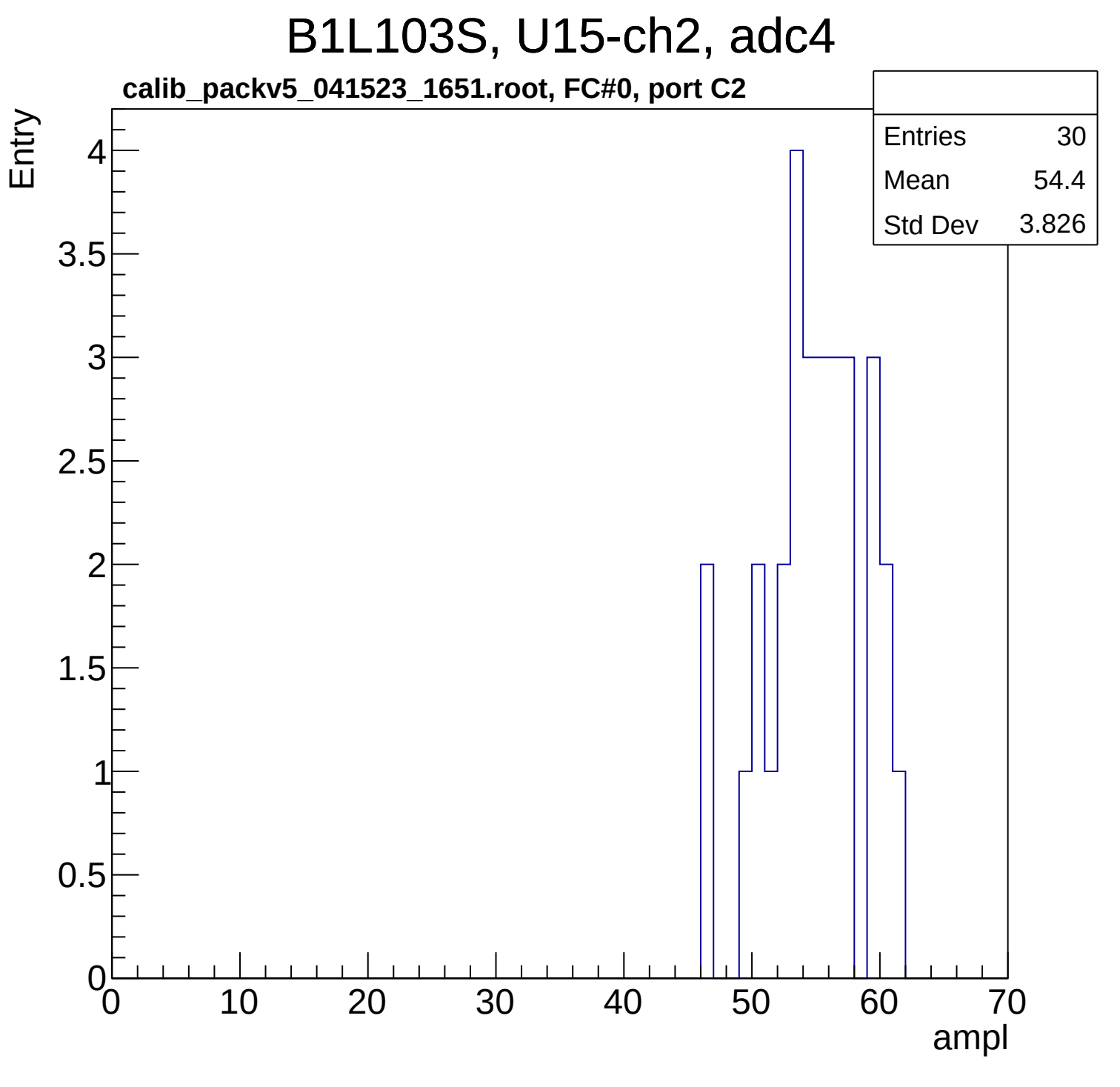
B1L103S, U15-ch2, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 54.4
Std Dev 3.826
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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60
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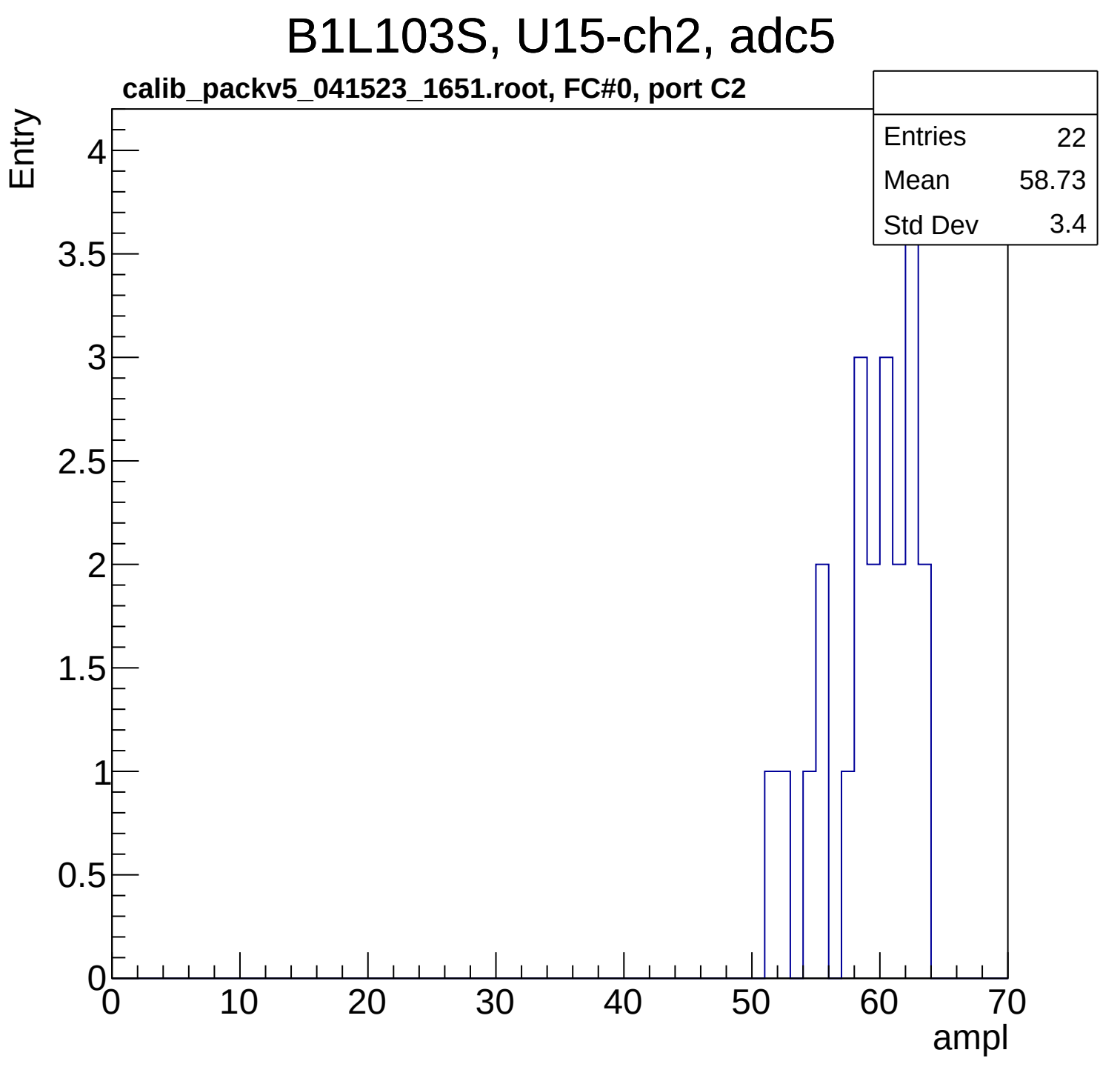
B1L103S, U15-ch2, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.73
Std Dev 3.4
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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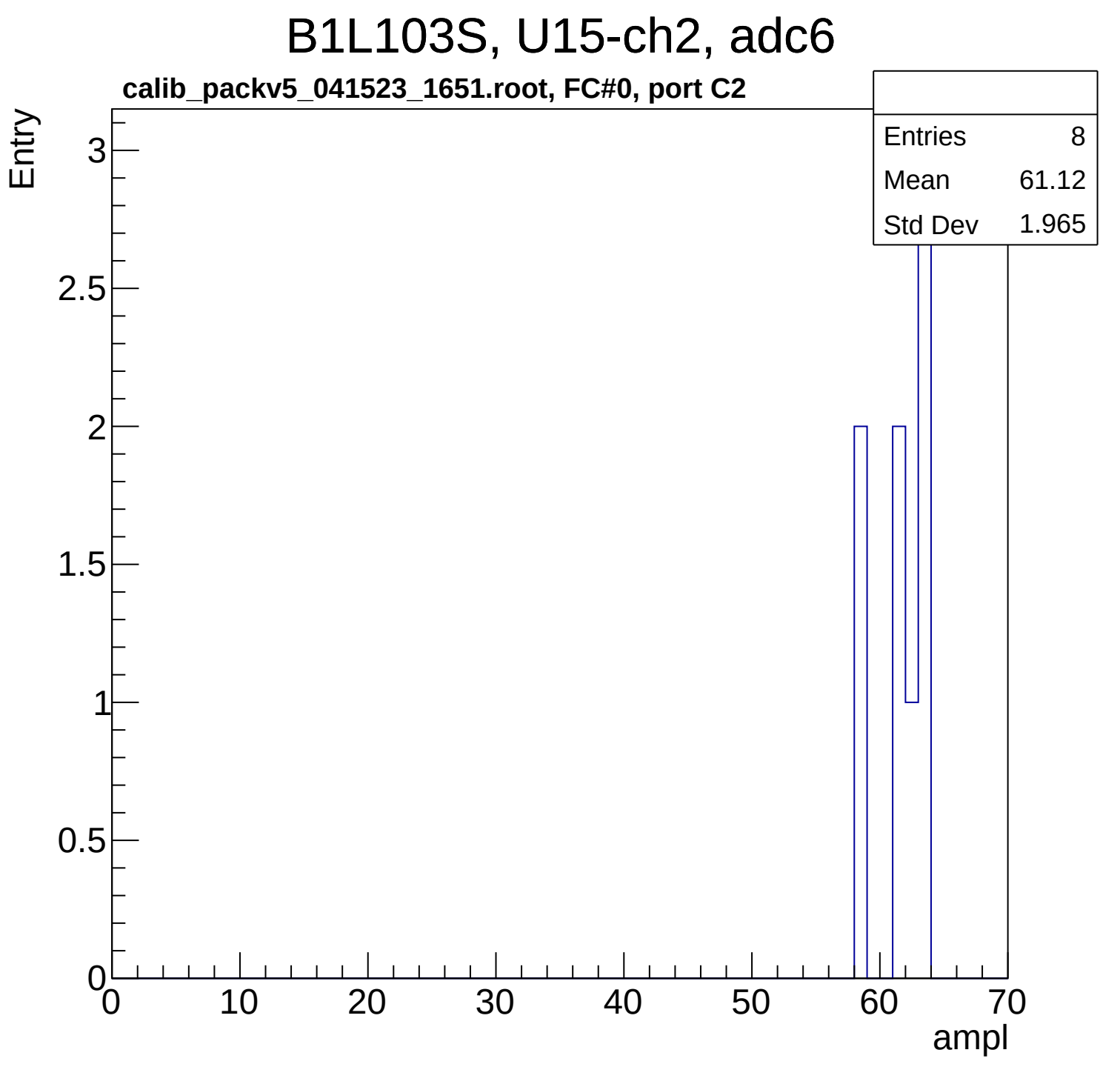
B1L103S, U15-ch2, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.12
Std Dev 1.965
Entry
ampl
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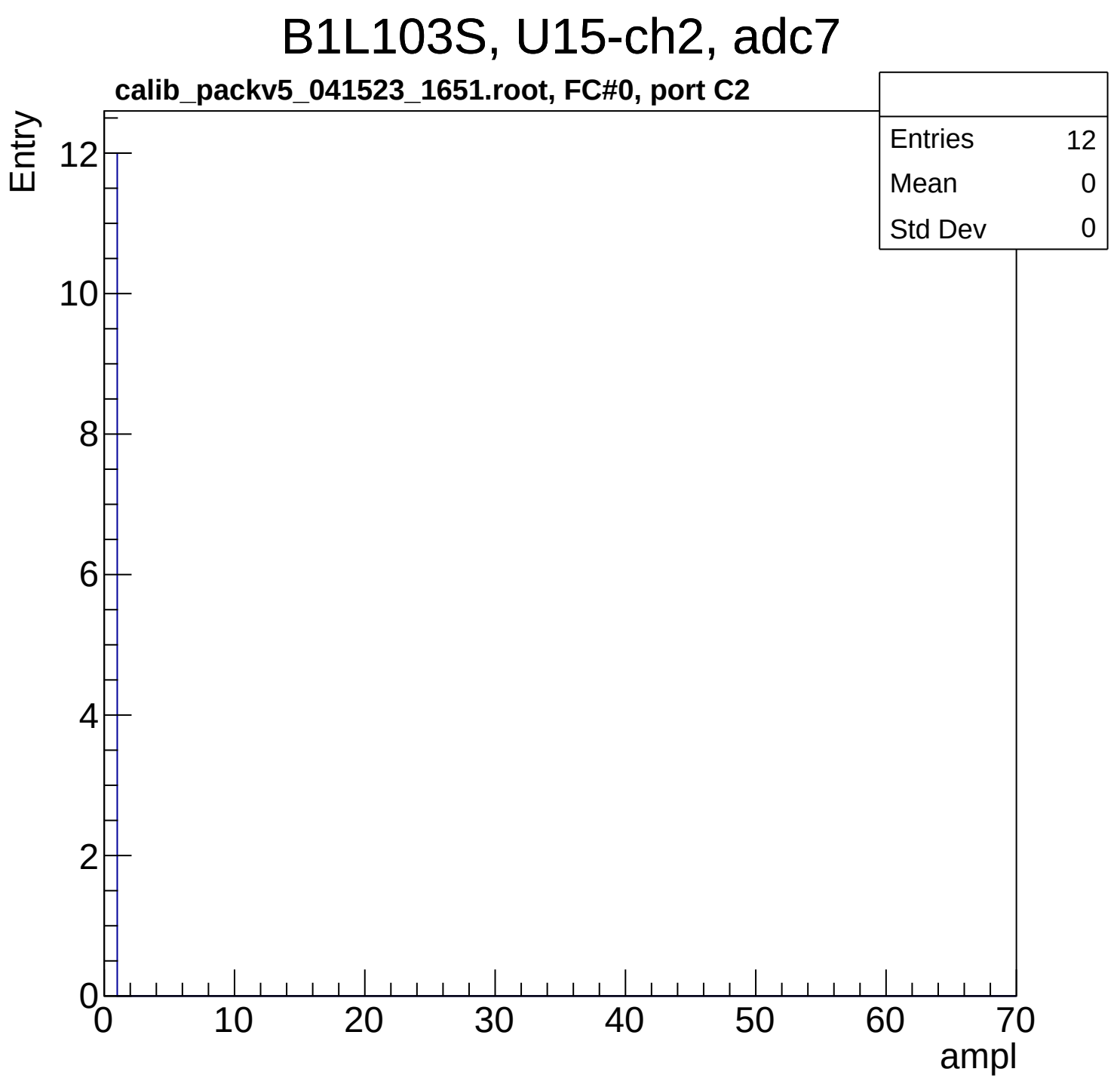
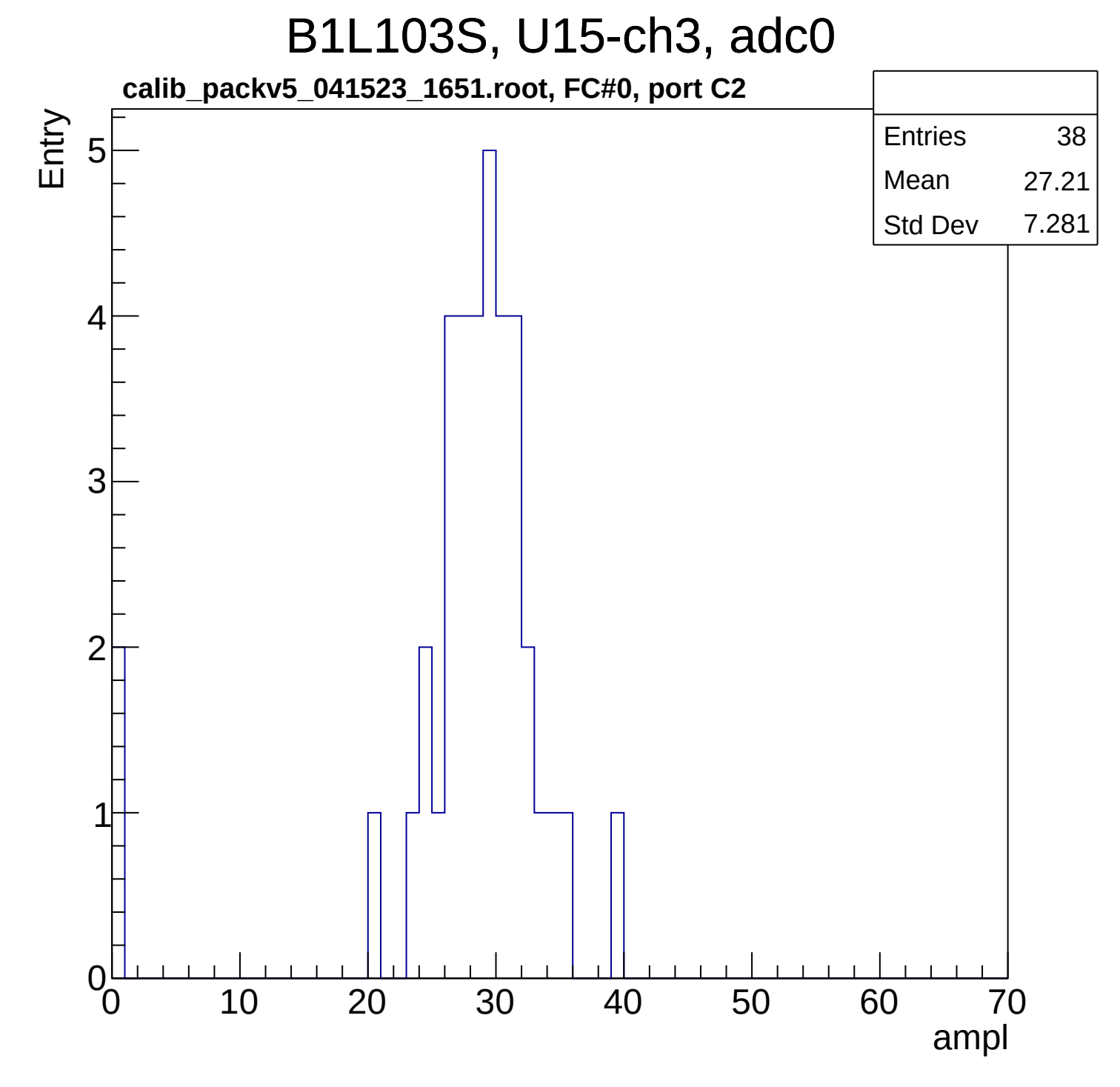
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch2, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch3, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 27.21
Std Dev 7.281
Entry
ampl
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1
2
3
4
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0
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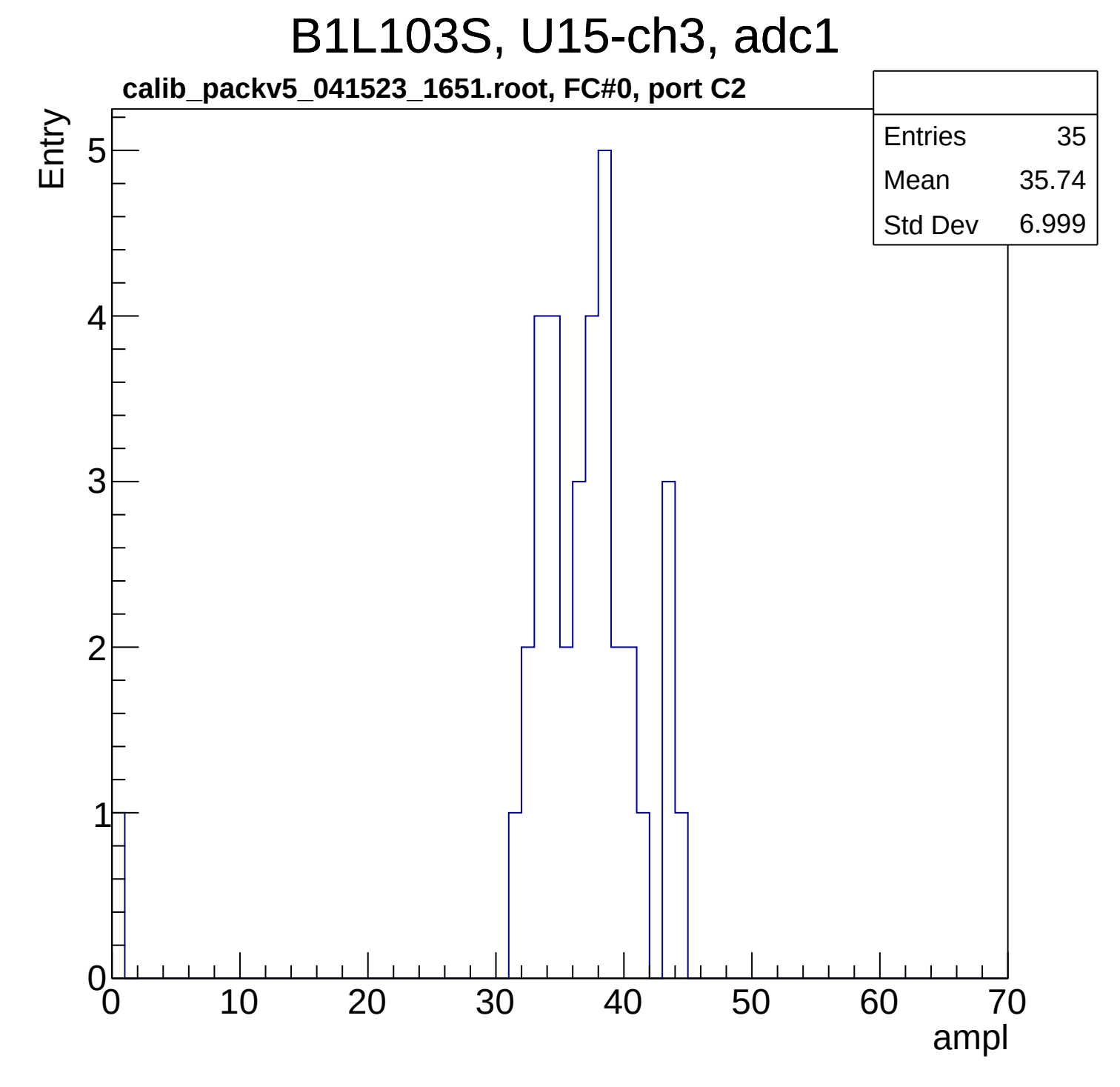
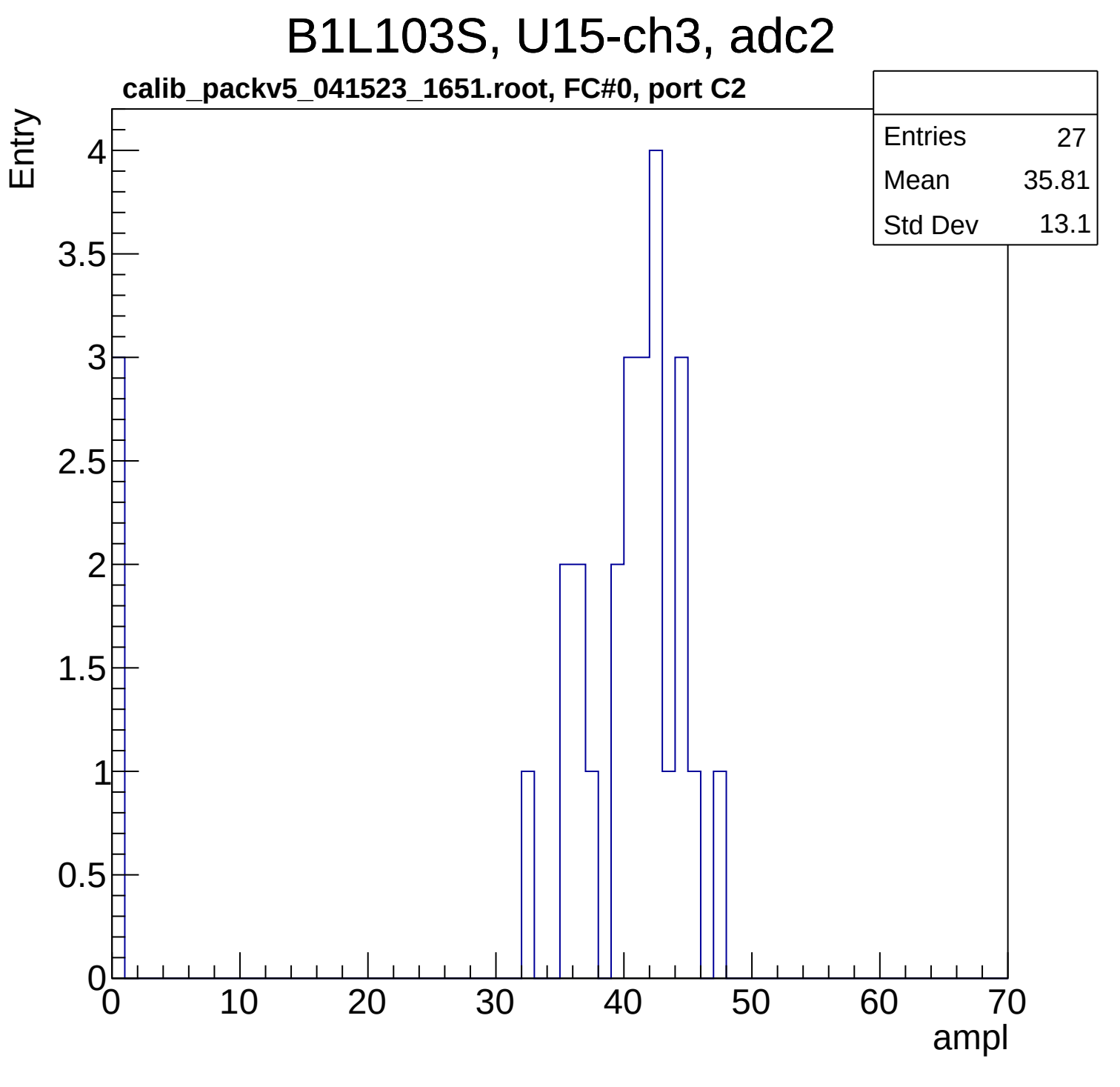
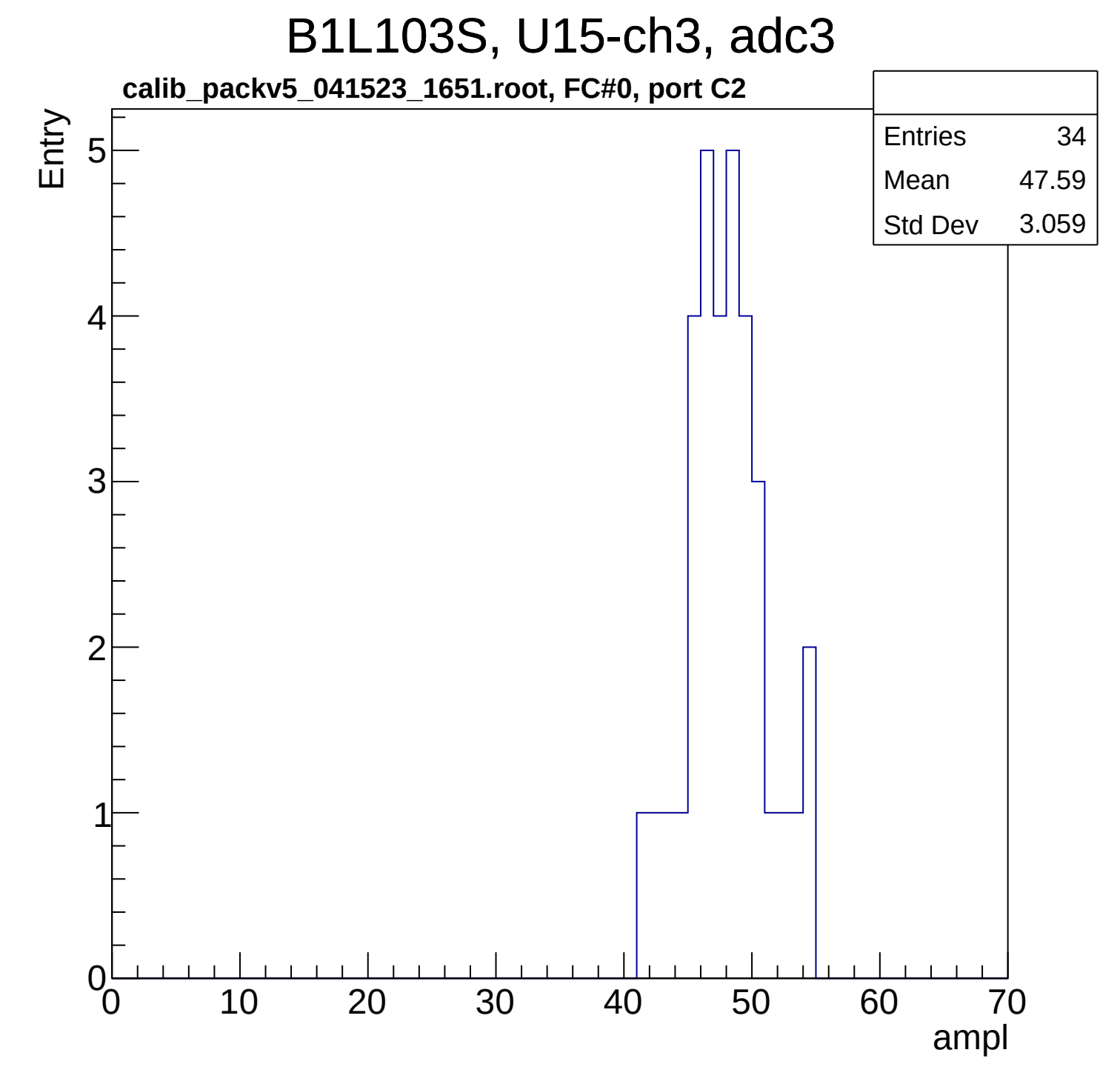
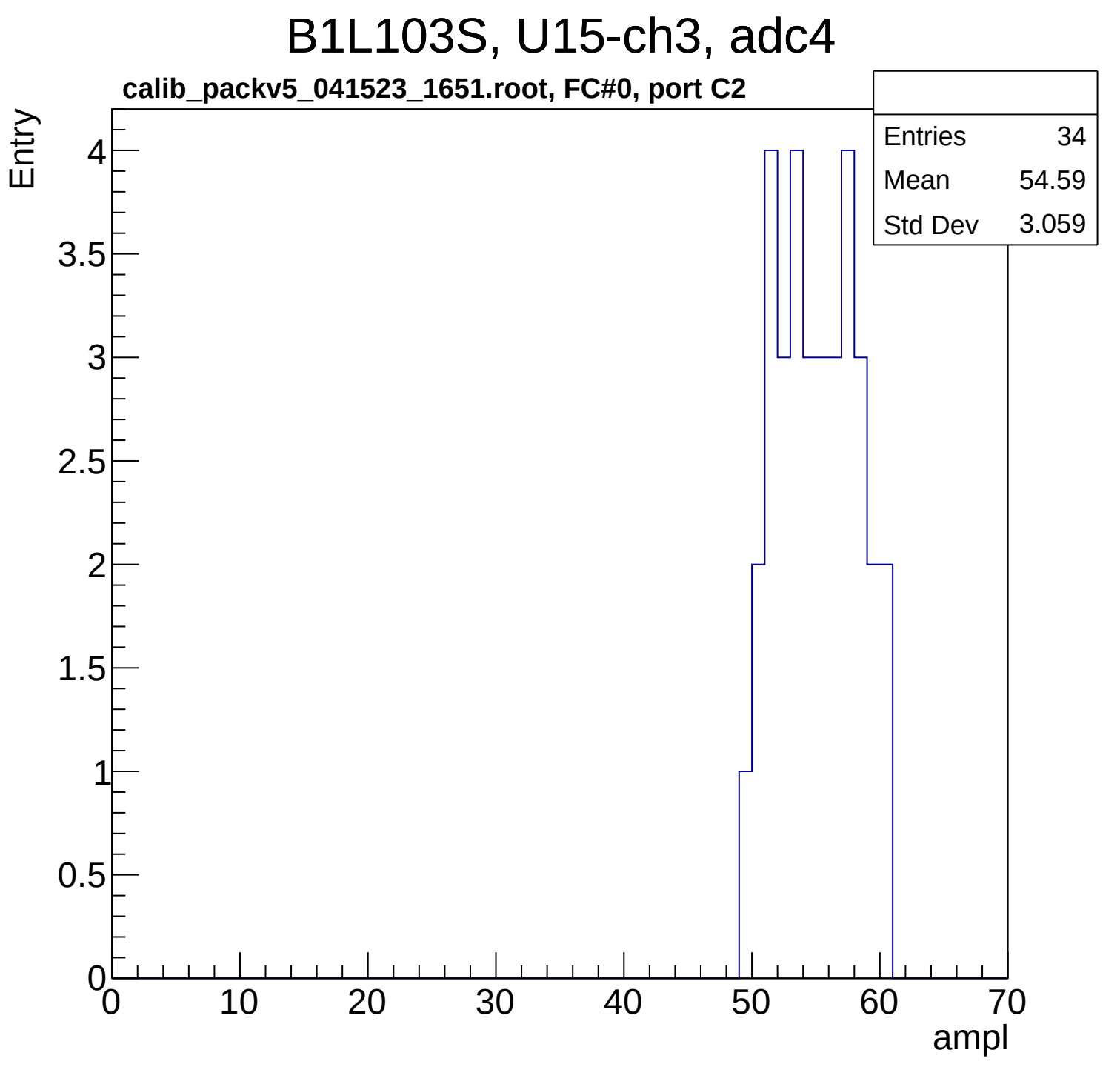
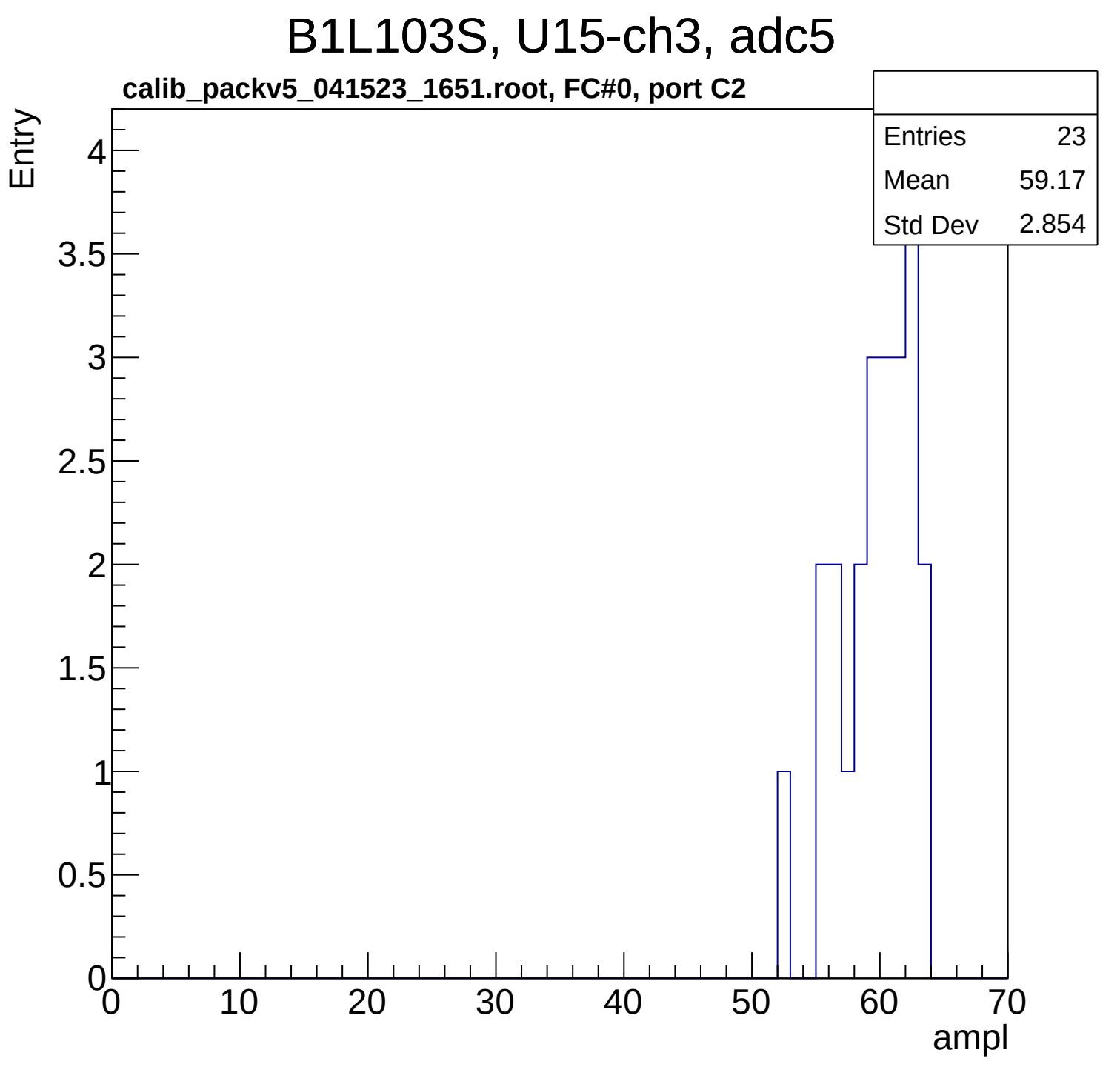
60
70


B1L103S, U15-ch3, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 35.74
Std Dev 6.999
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch3, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 35.81
Std Dev 13.1
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch3, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 47.59
Std Dev 3.059
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch3, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 54.59
Std Dev 3.059
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch3, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 59.17
Std Dev 2.854
Entry
ampl
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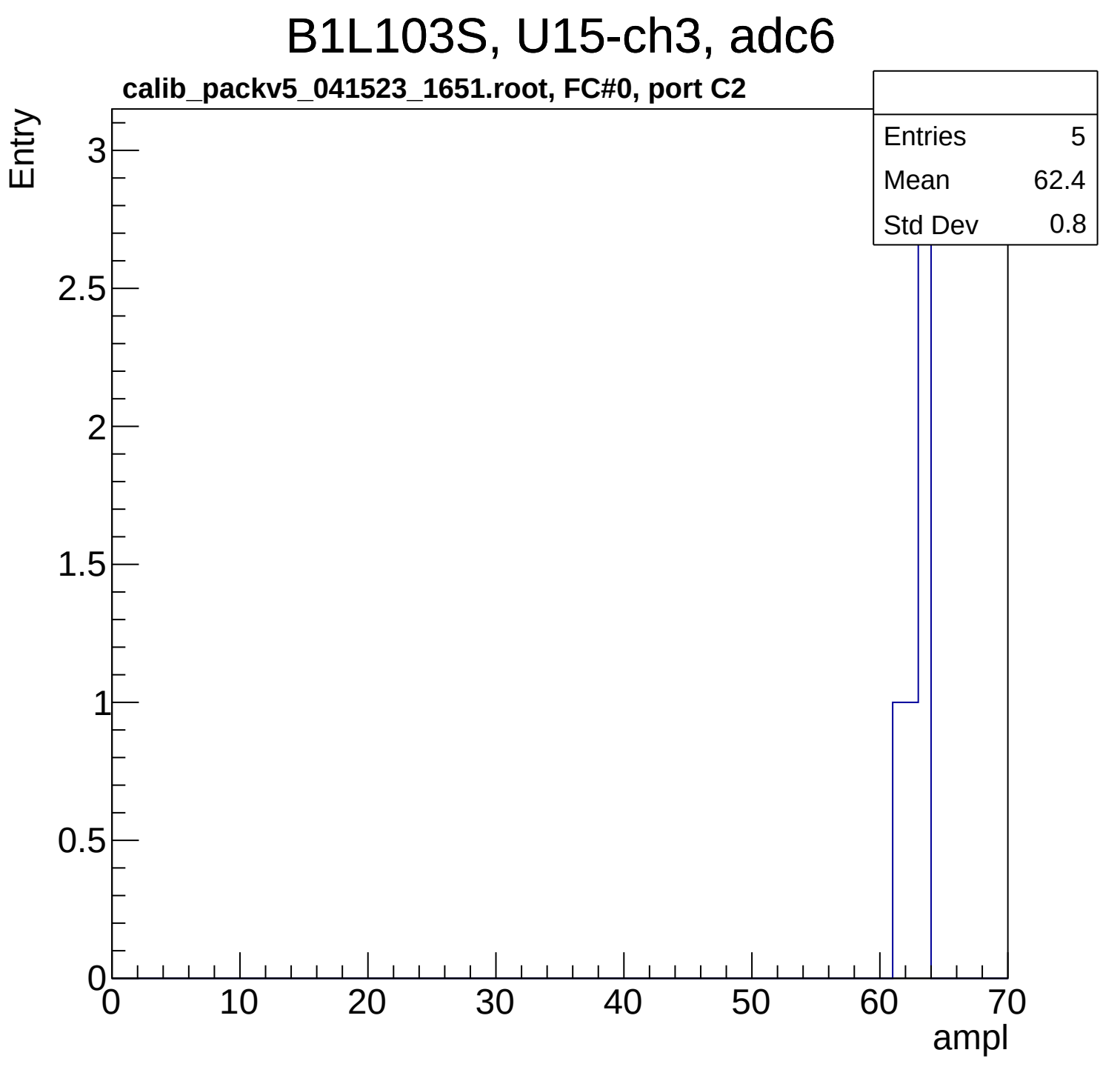
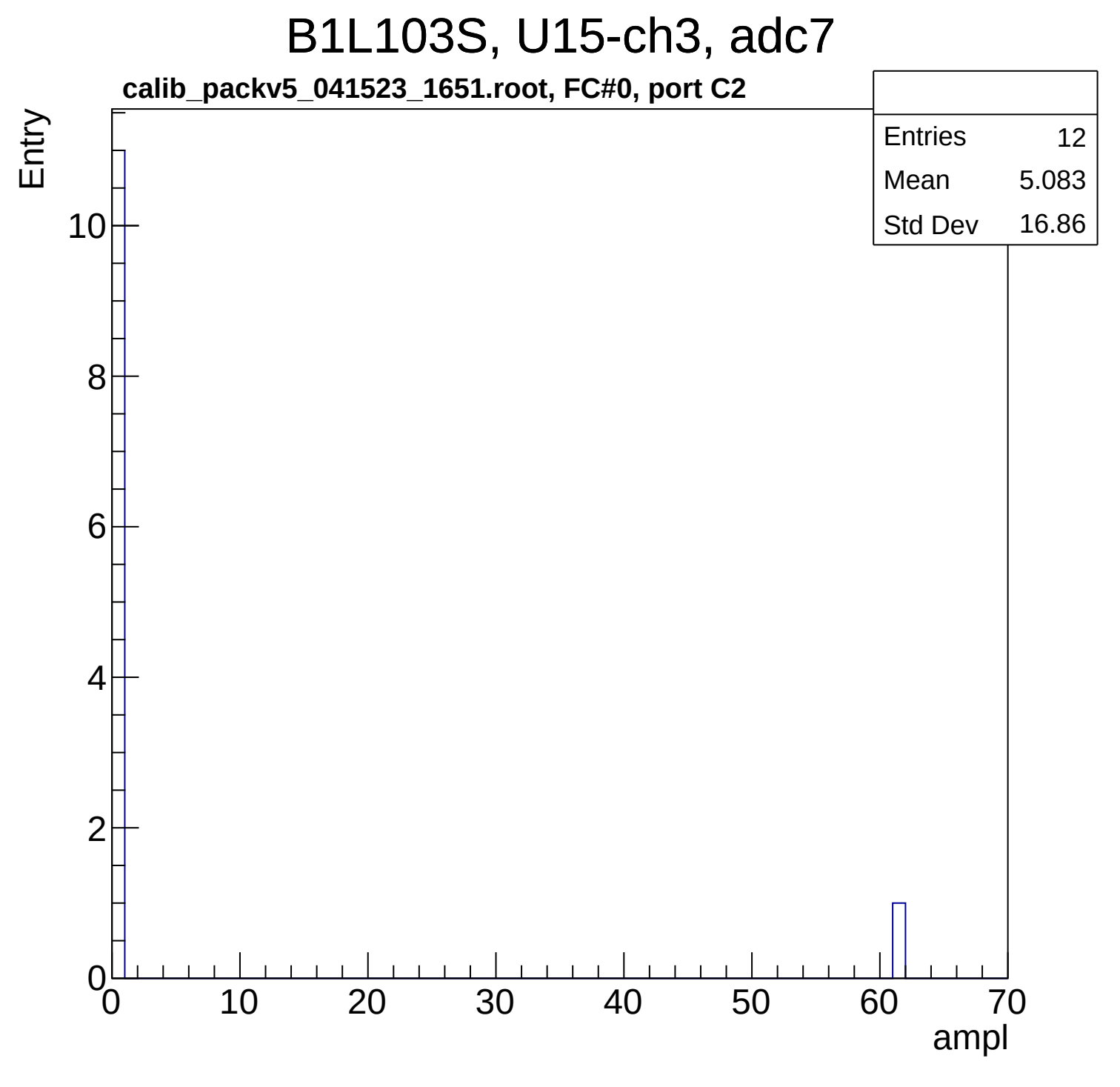
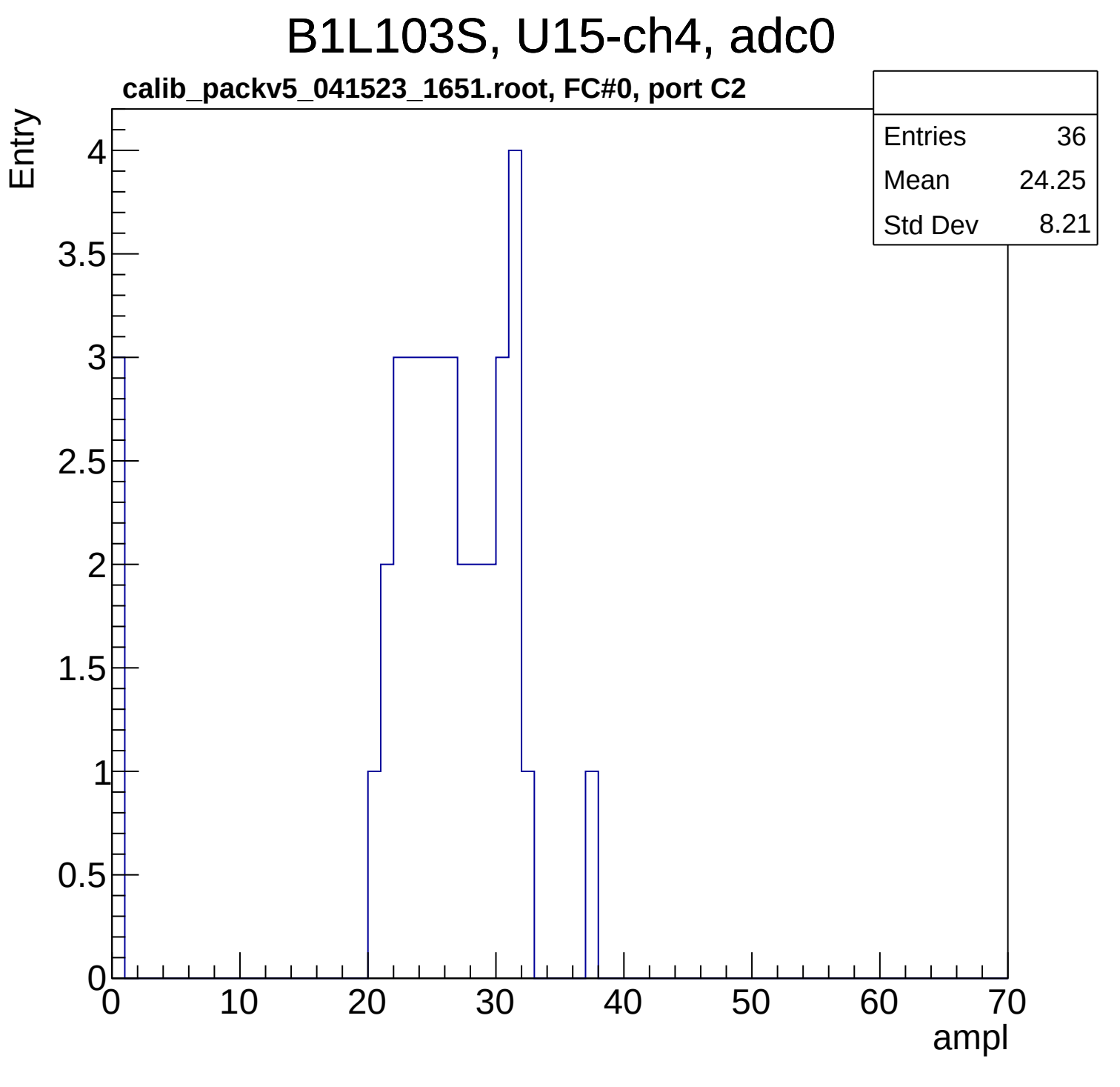
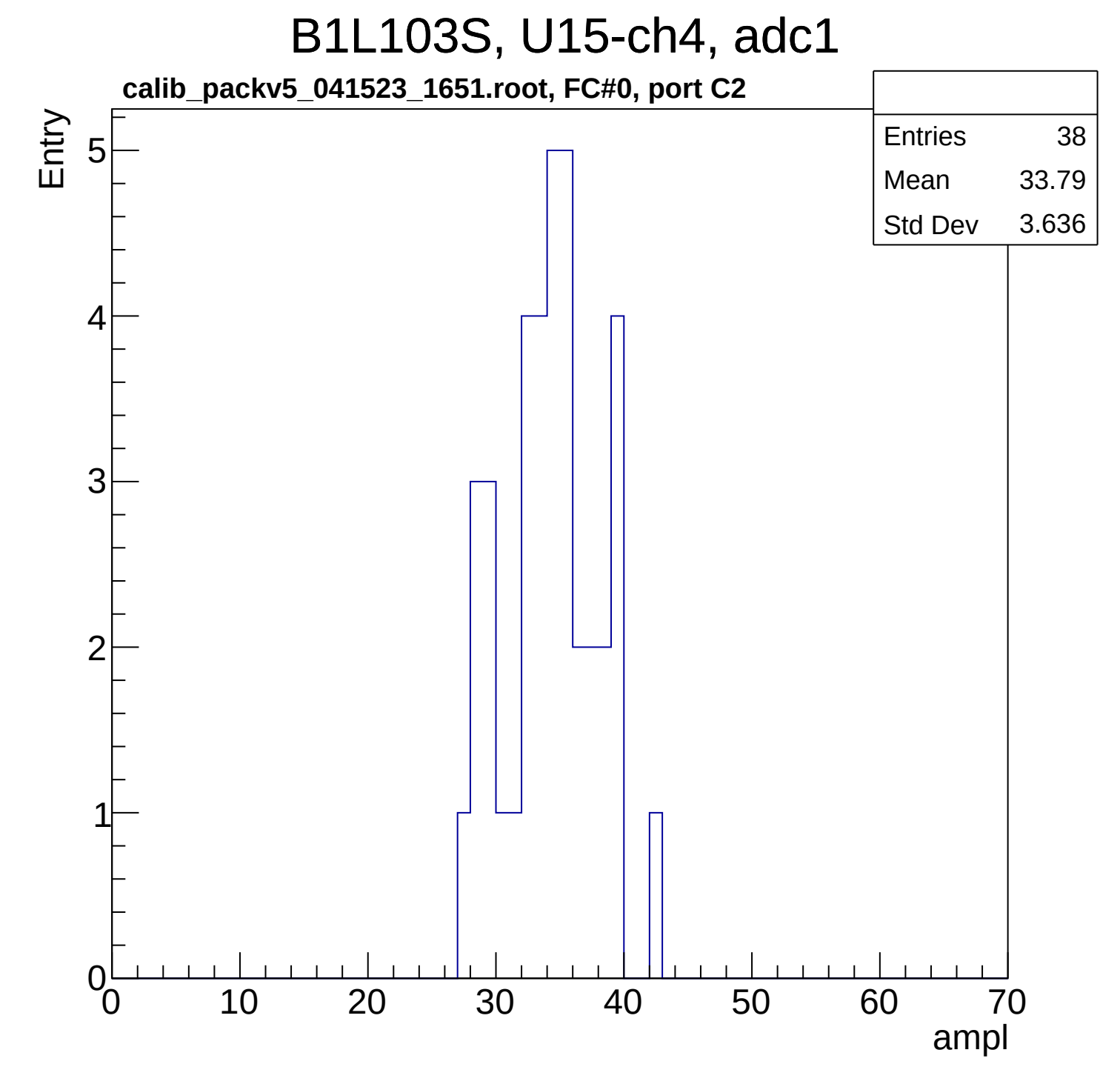
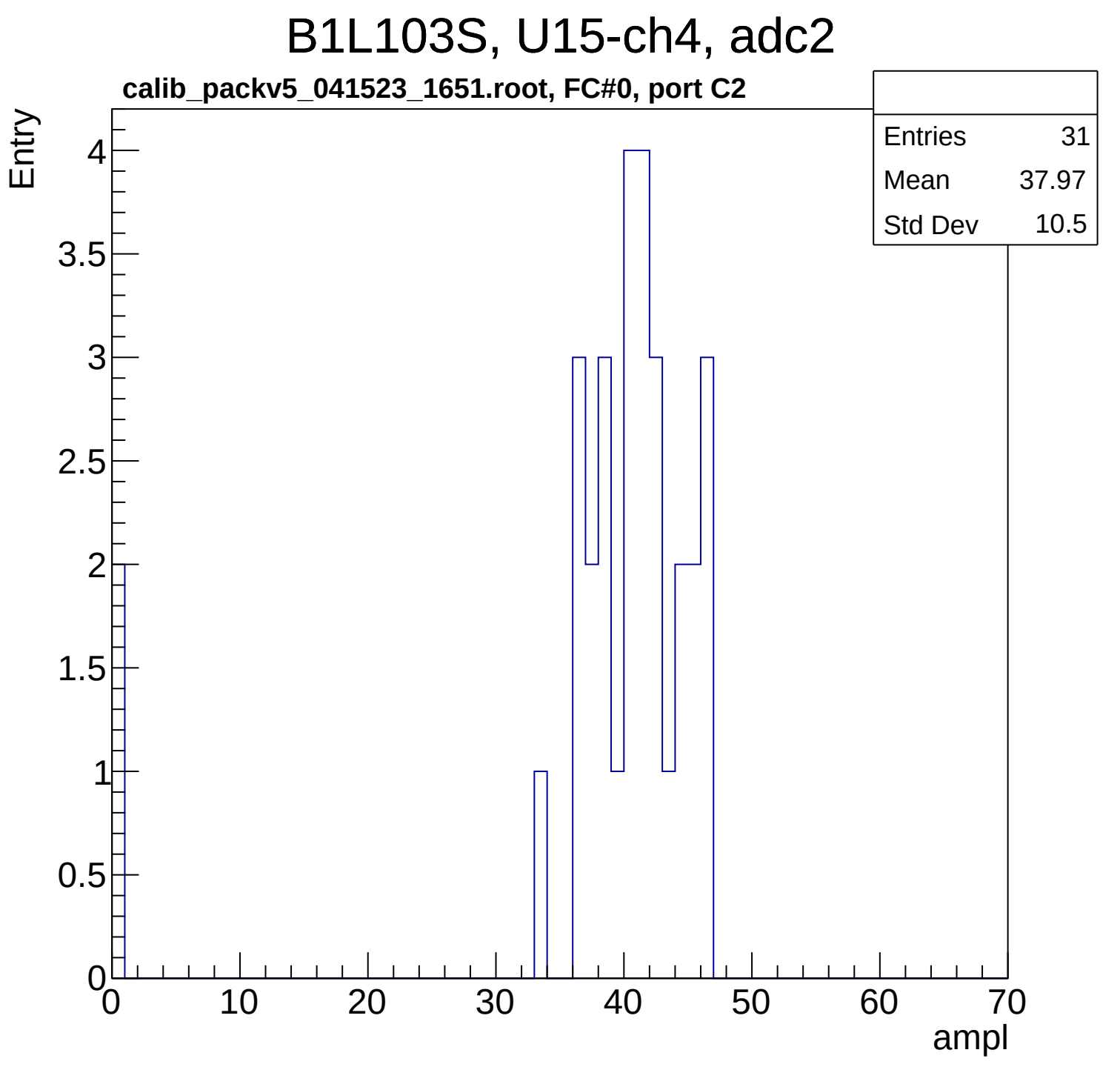
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

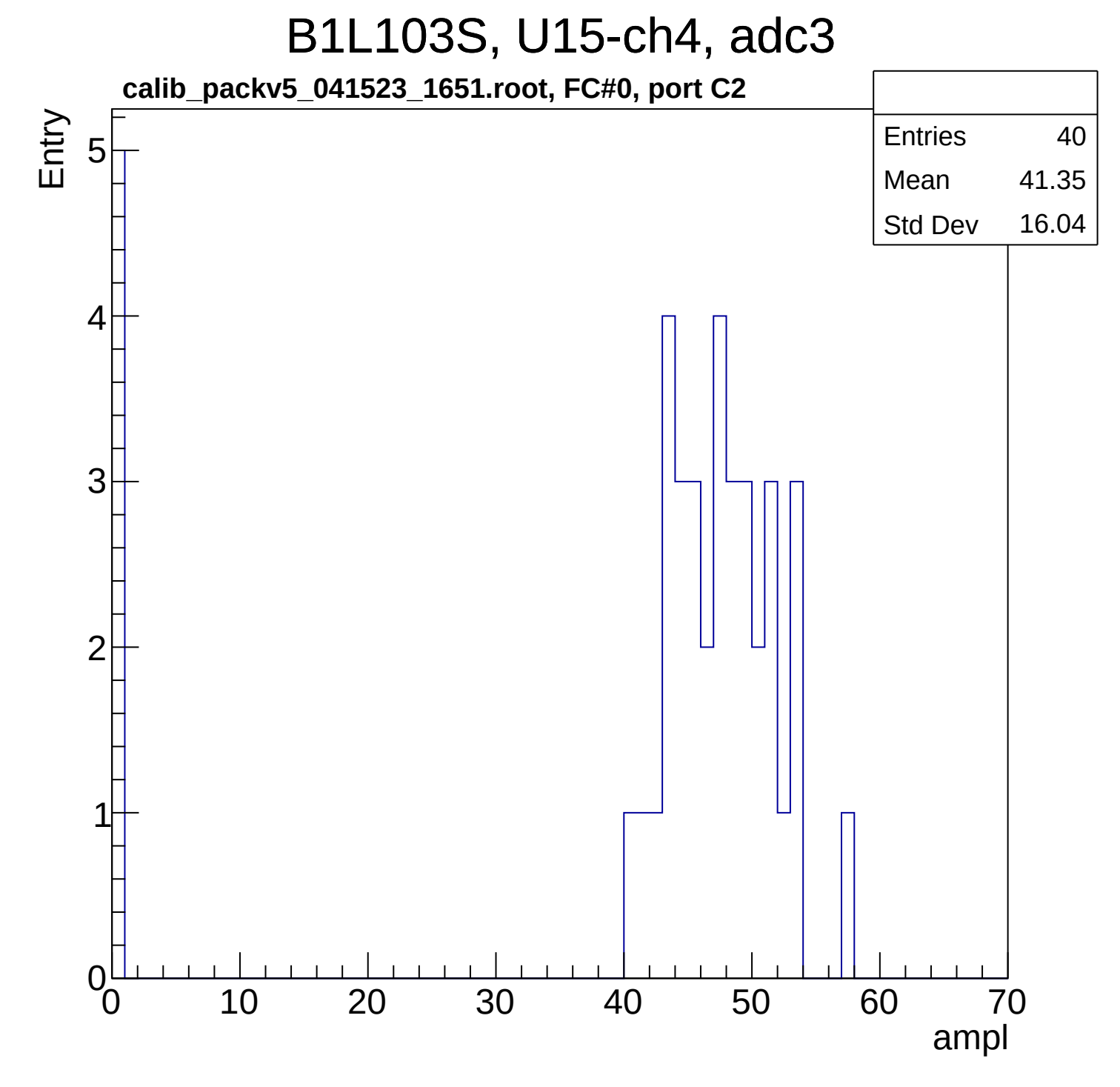

B1L103S, U15-ch3, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.4
Std Dev 0.8
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl

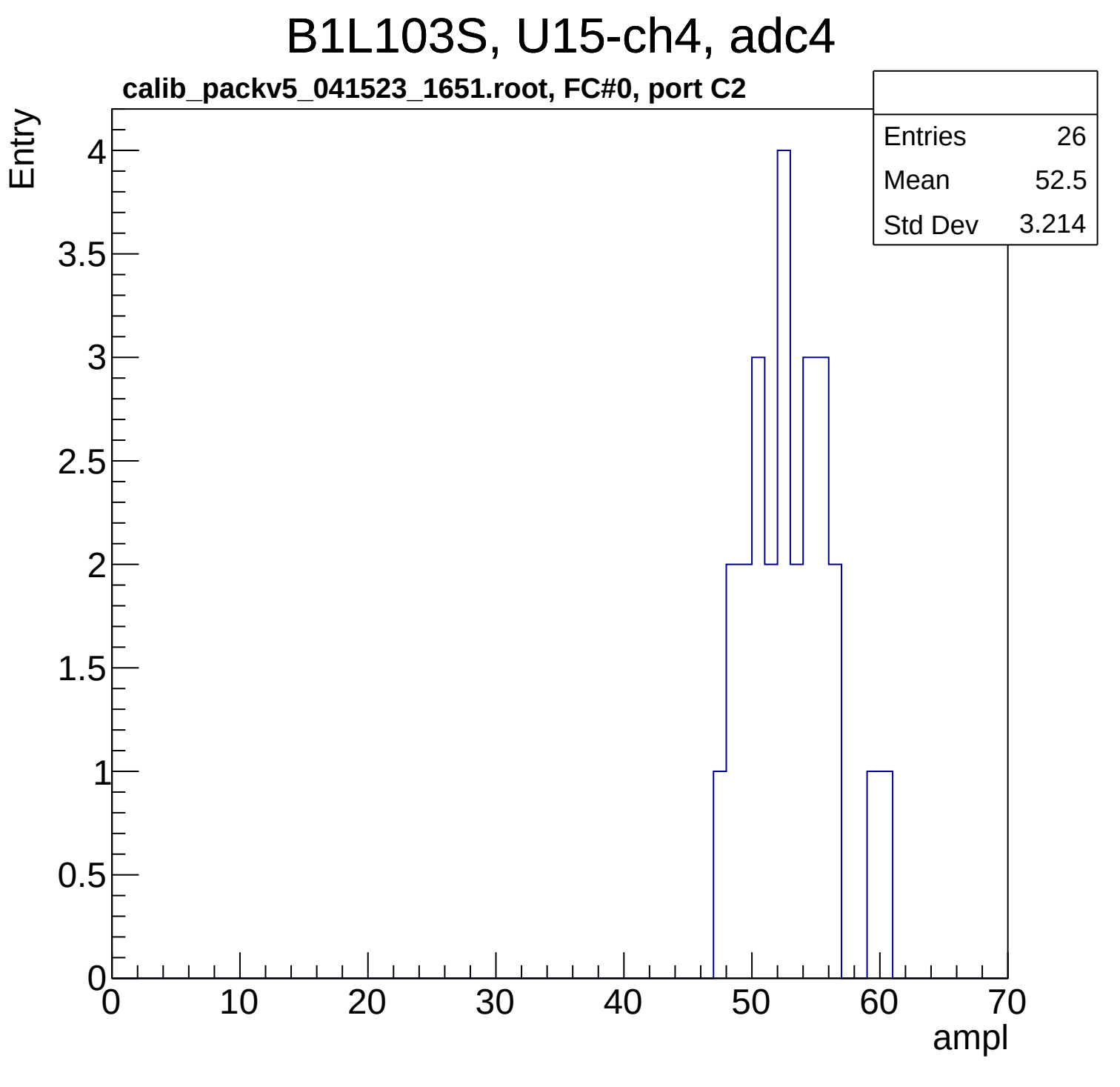

B1L103S, U15-ch3, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 5.083
Std Dev 16.86
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

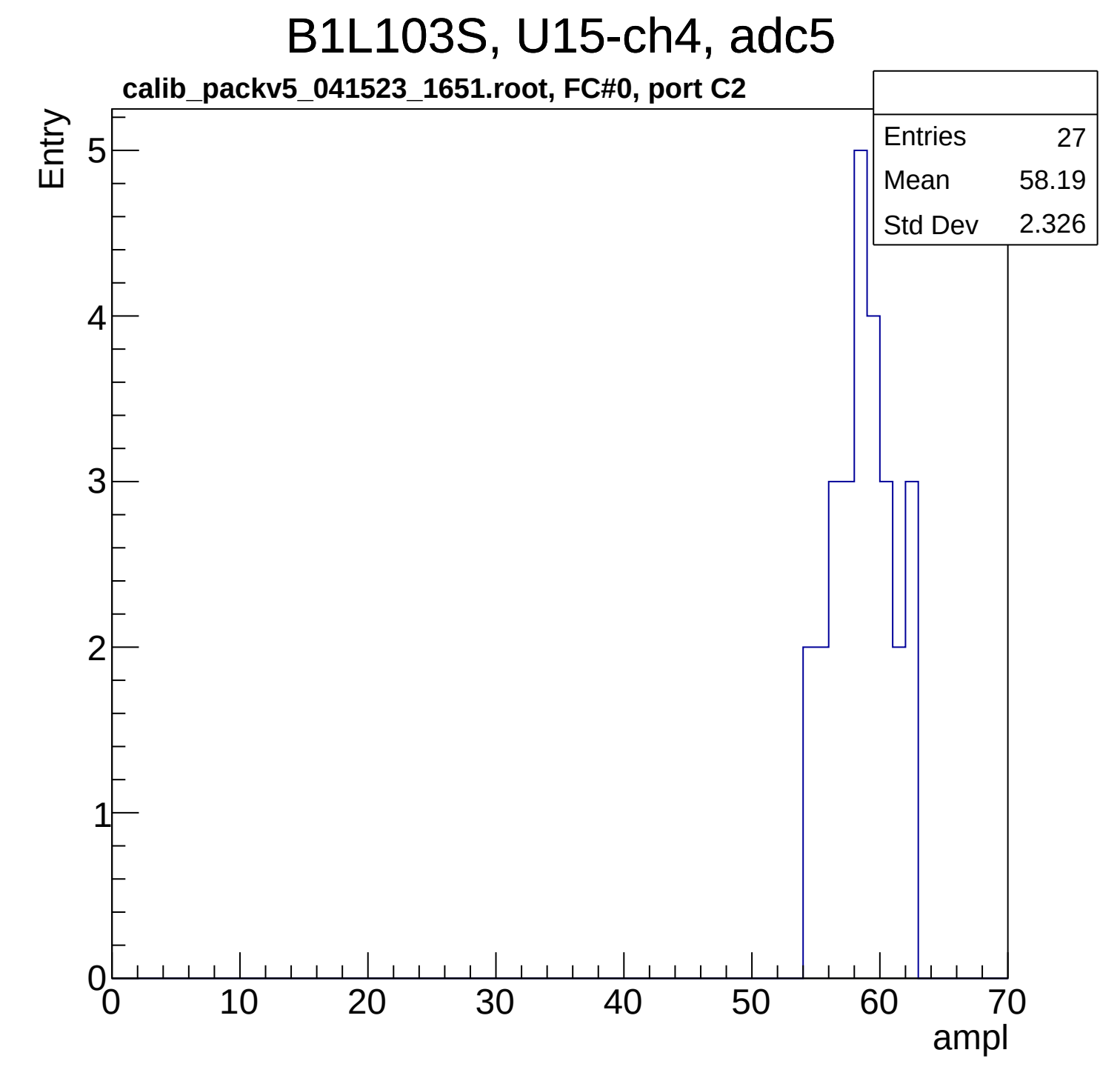

B1L103S, U15-ch4, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 24.25
Std Dev 8.21
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

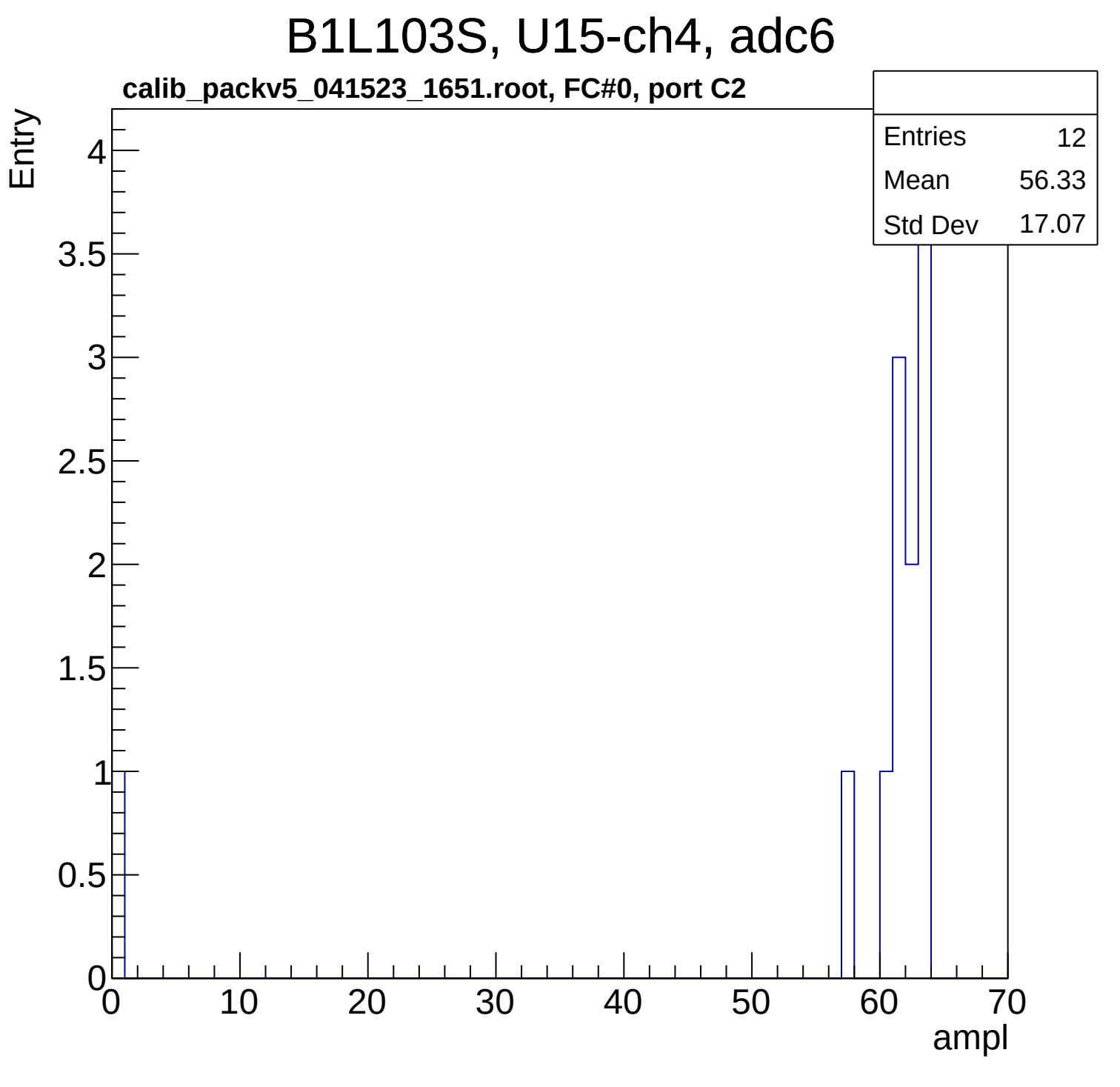

B1L103S, U15-ch4, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 33.79
Std Dev 3.636
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

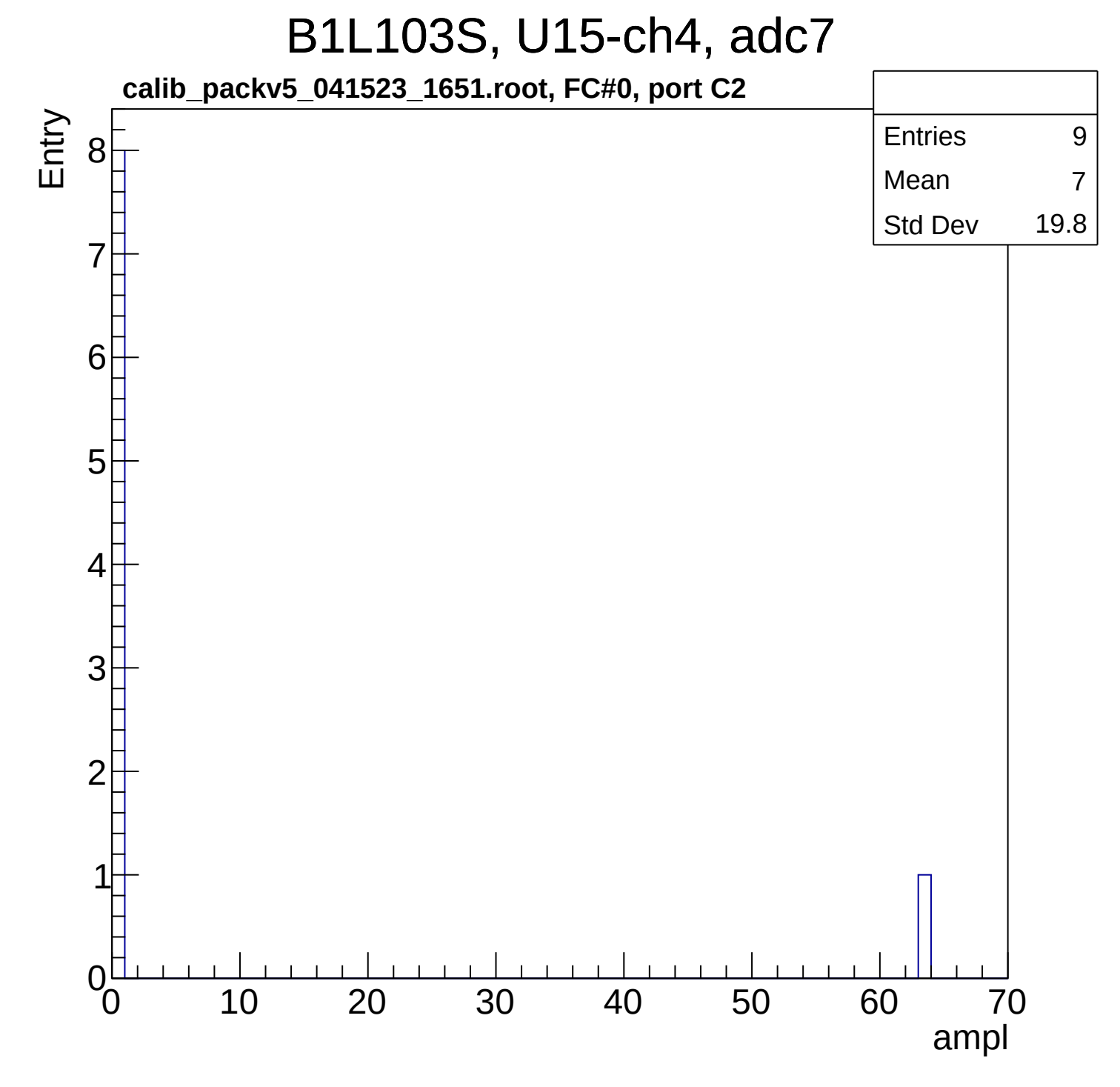

B1L103S, U15-ch4, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 37.97
Std Dev 10.5
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

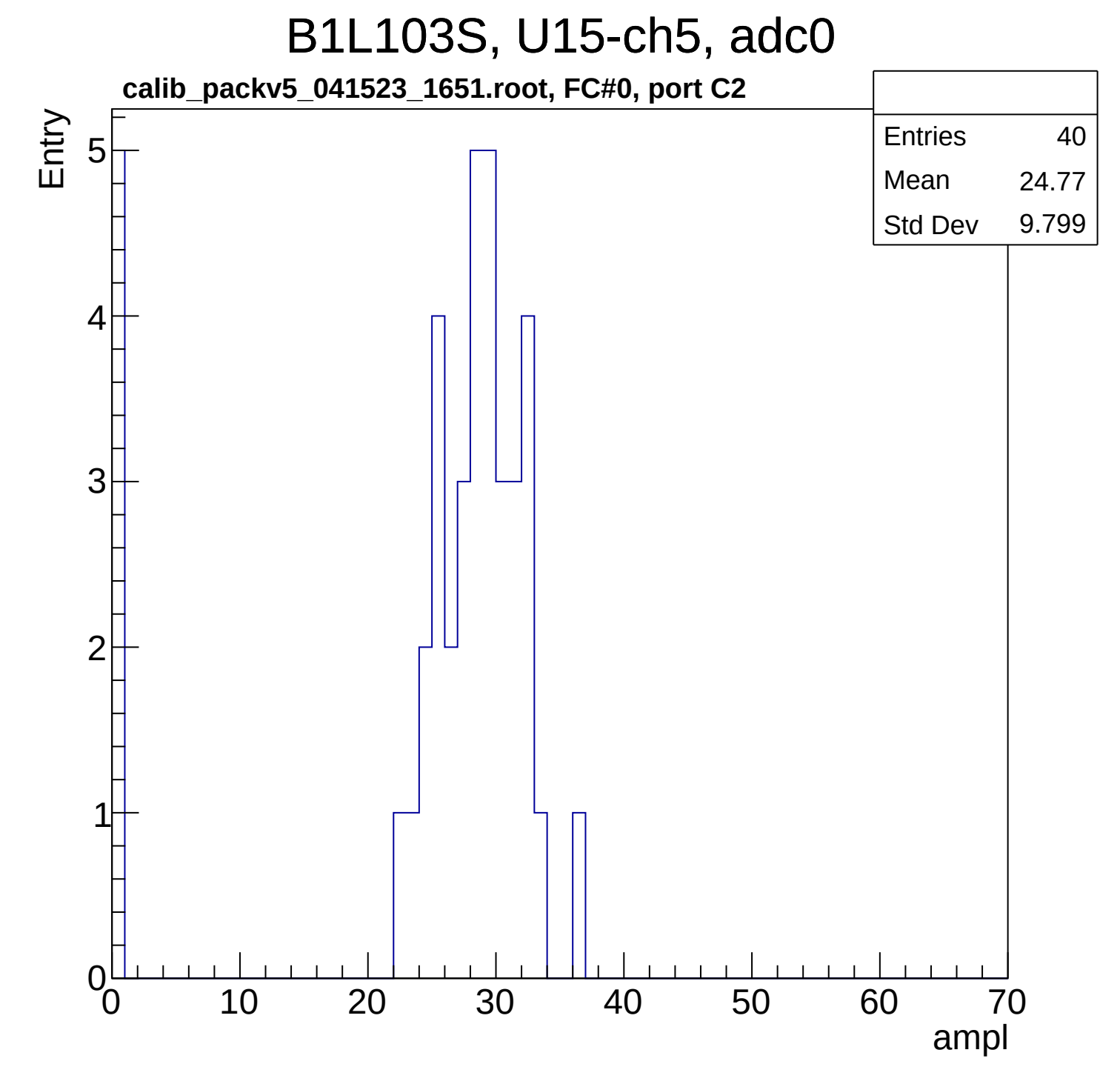

B1L103S, U15-ch4, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 41.35
Std Dev 16.04
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

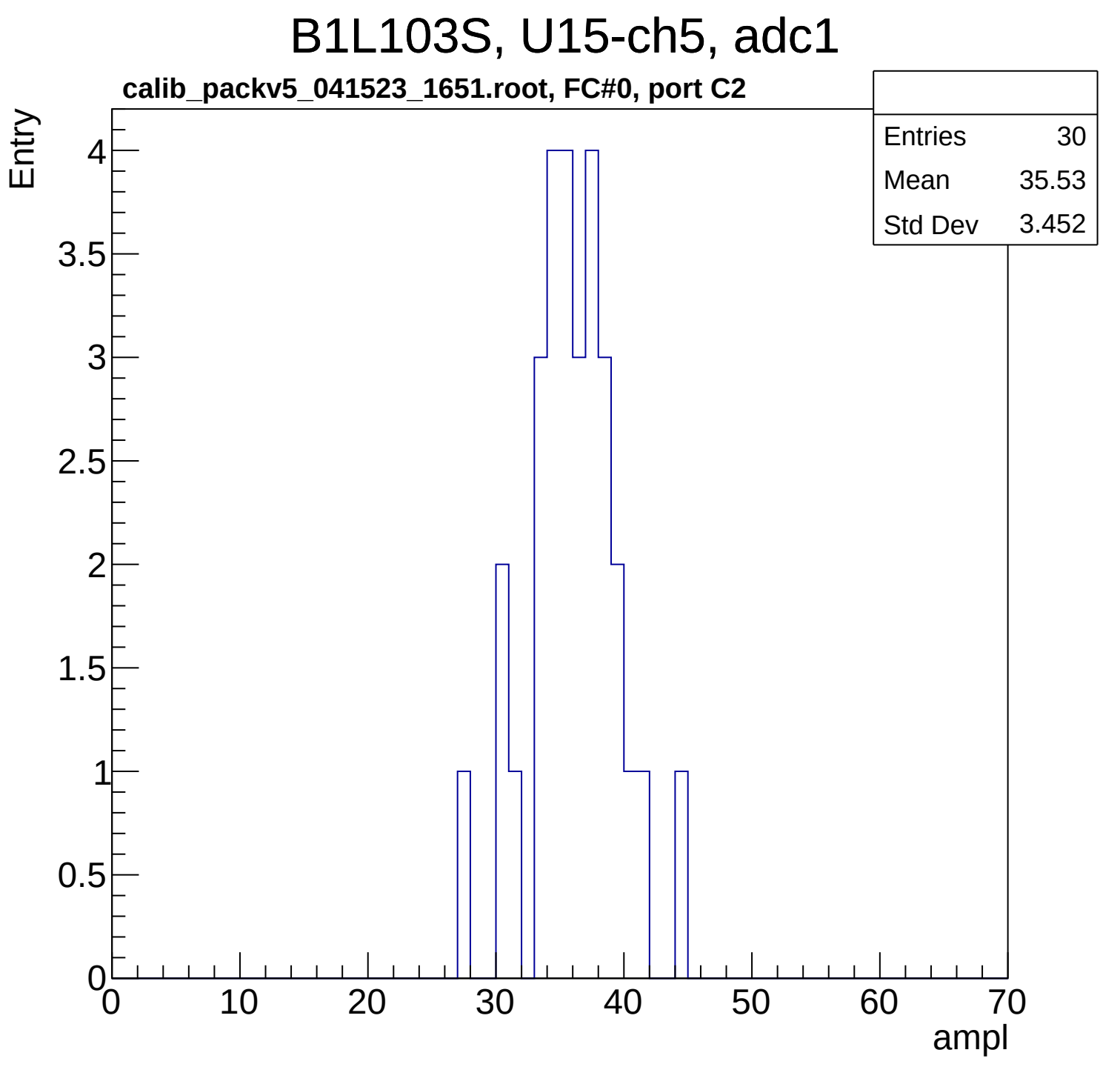

B1L103S, U15-ch4, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 52.5
Std Dev 3.214
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

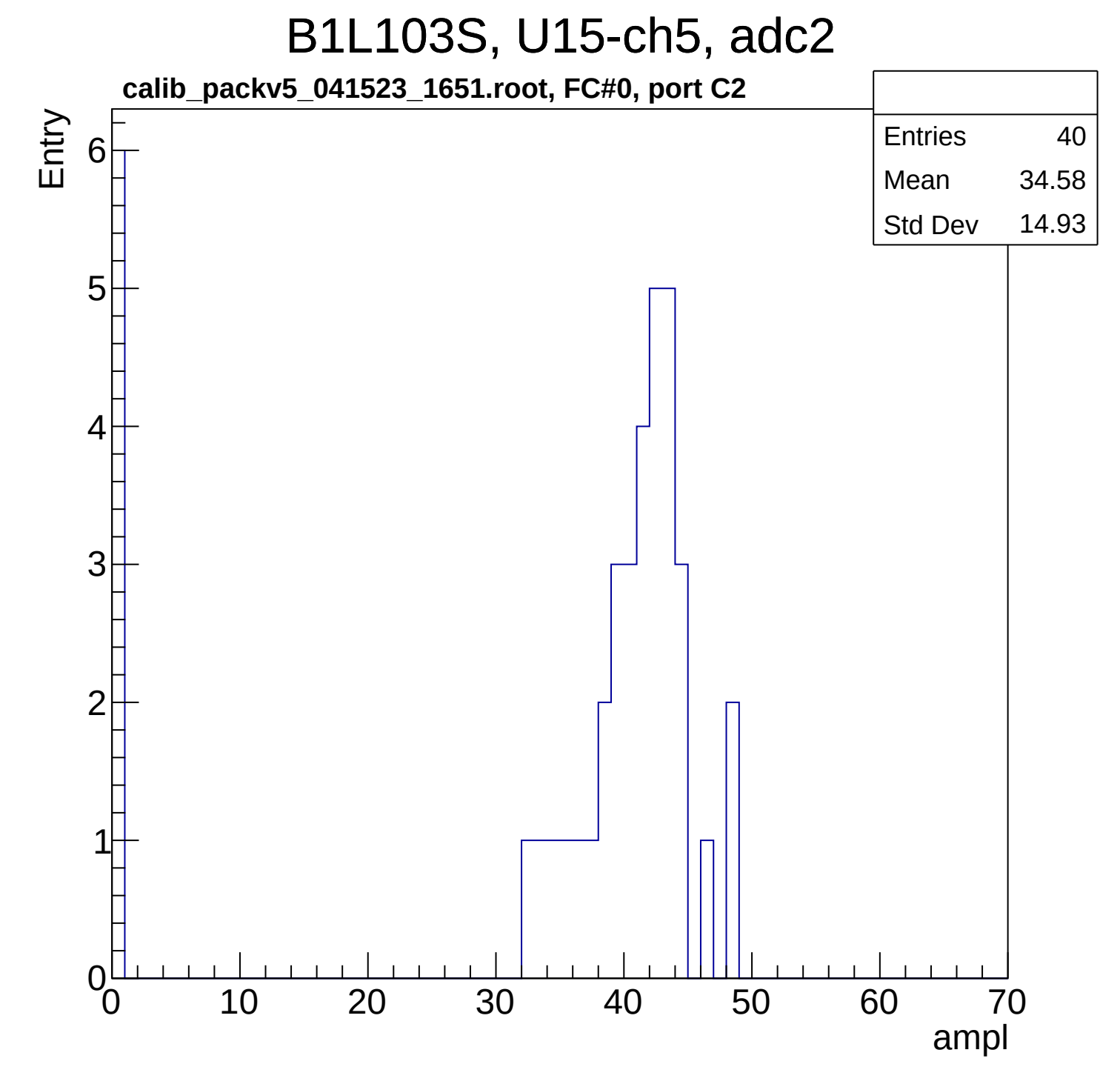

B1L103S, U15-ch4, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 58.19
Std Dev 2.326
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

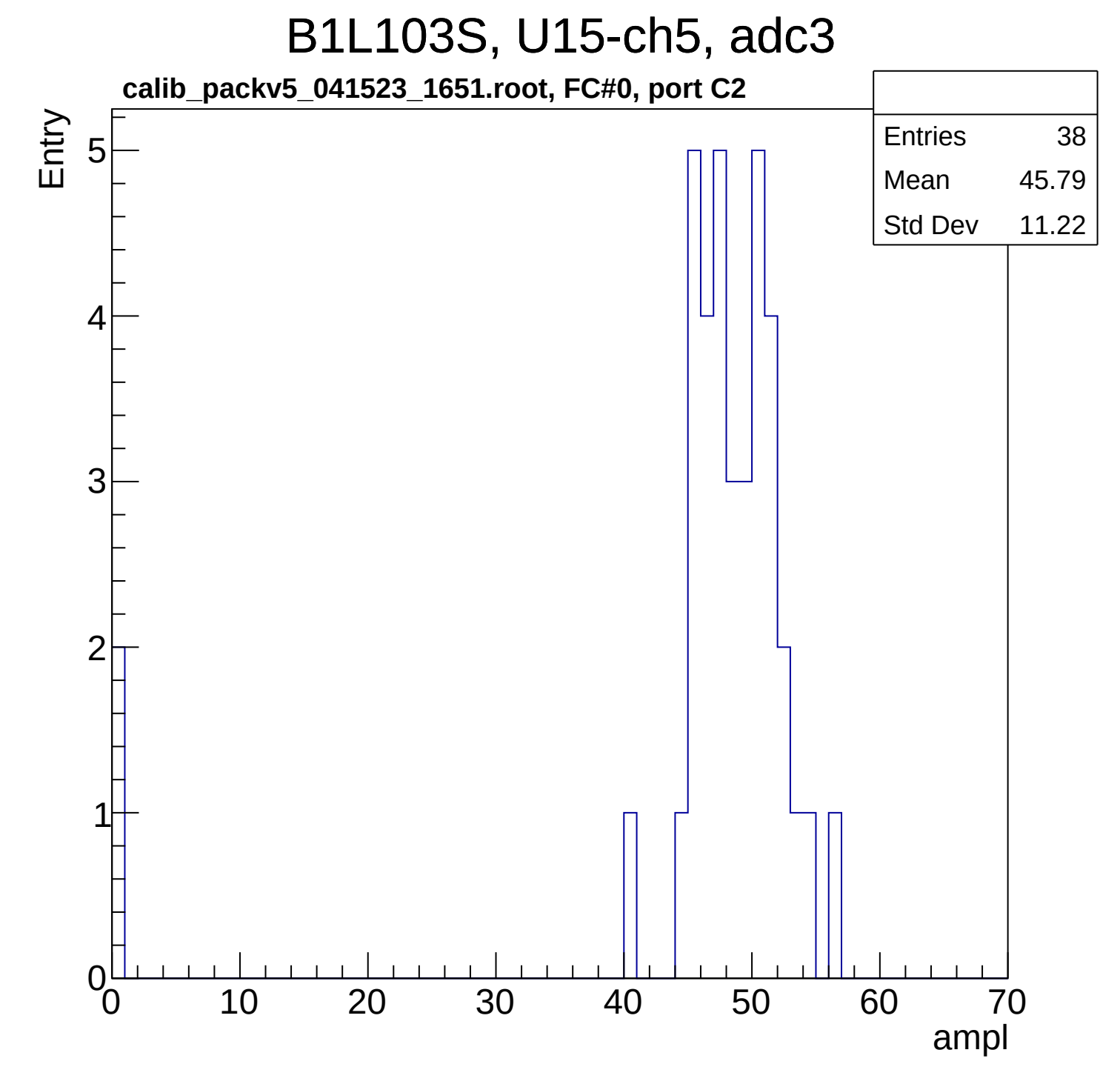

B1L103S, U15-ch4, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.33
Std Dev 17.07
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

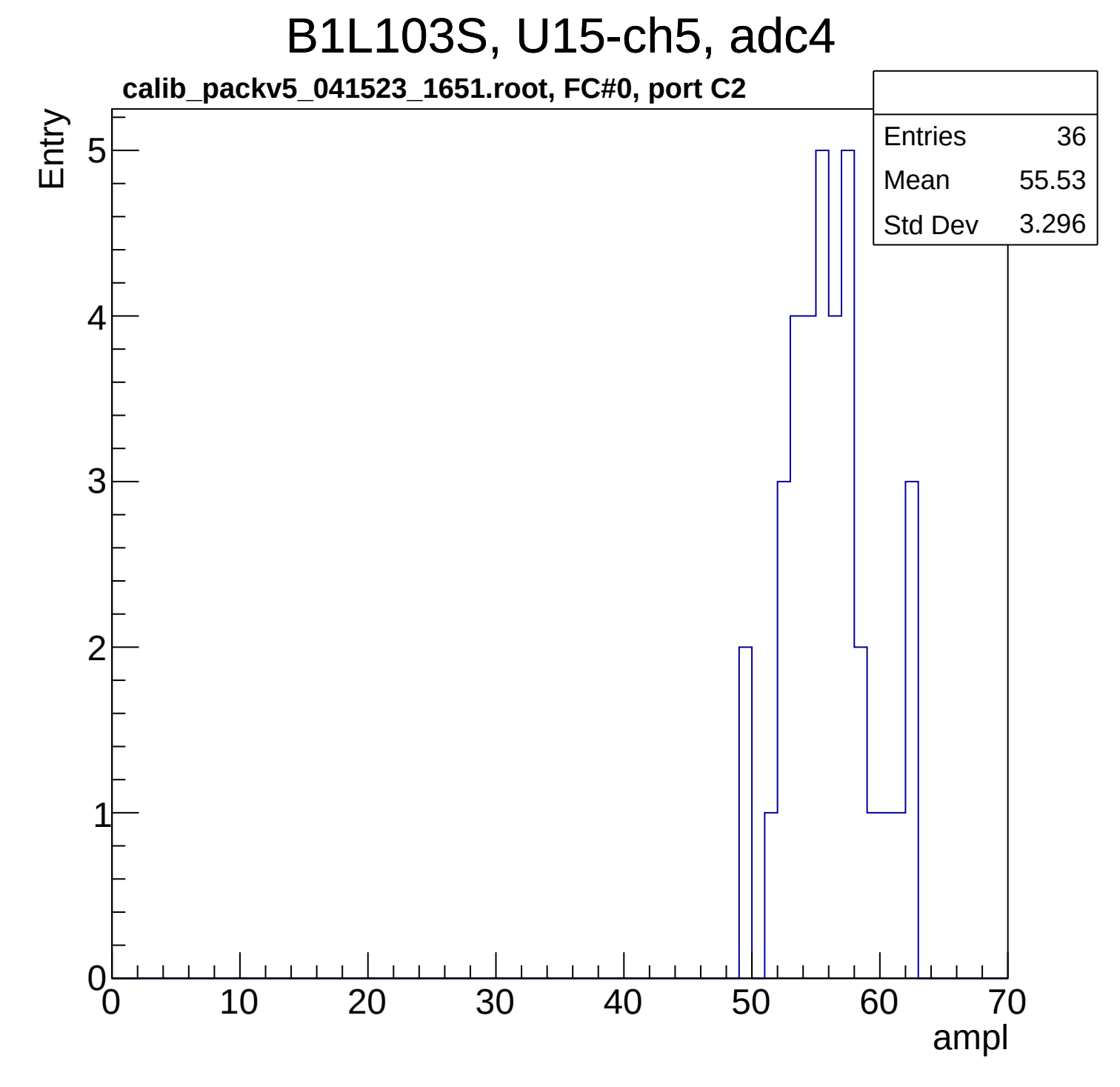

B1L103S, U15-ch4, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 7
Std Dev 19.8
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

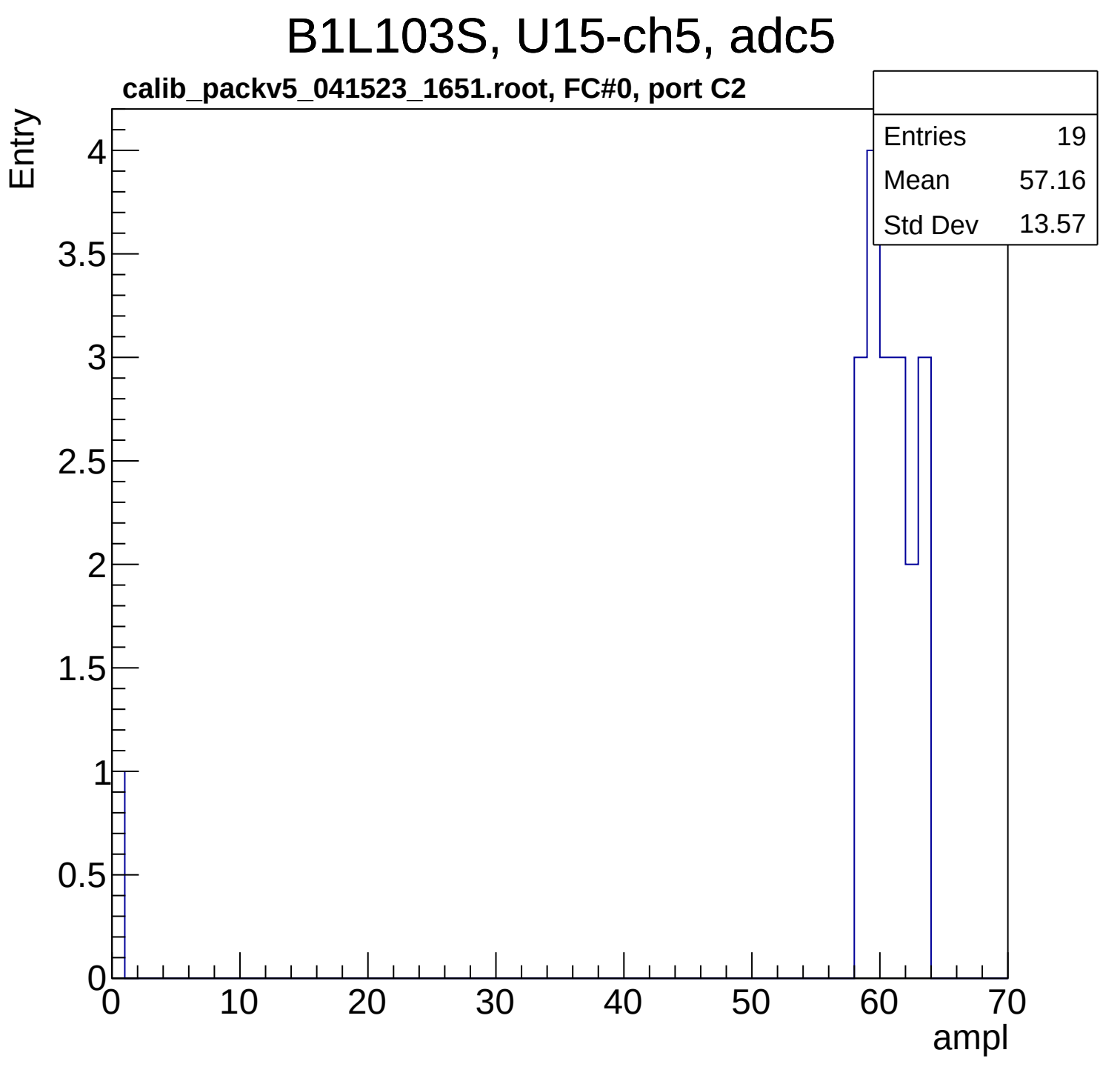

B1L103S, U15-ch5, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 24.77
Std Dev 9.799
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

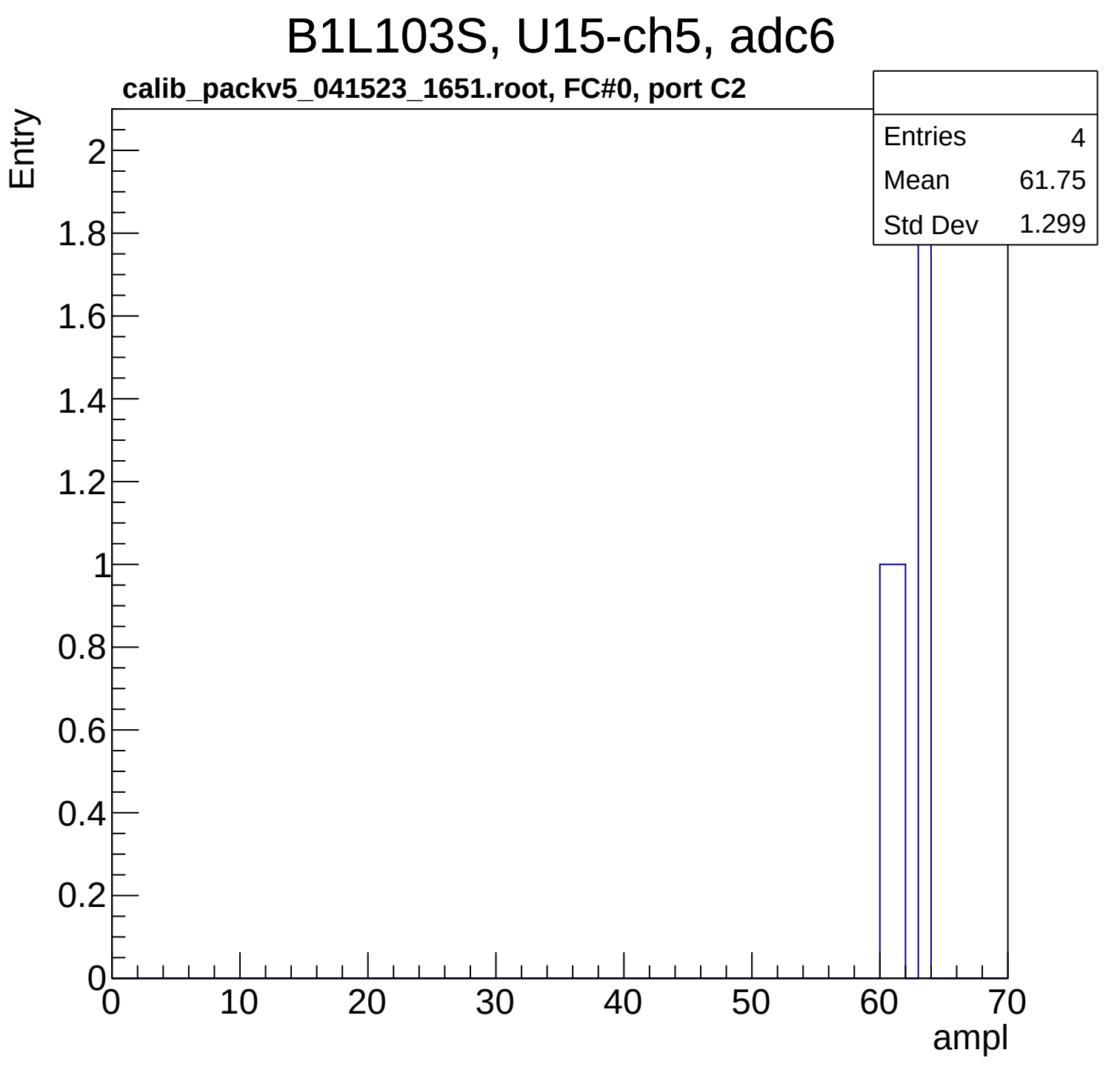

B1L103S, U15-ch5, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 35.53
Std Dev 3.452
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

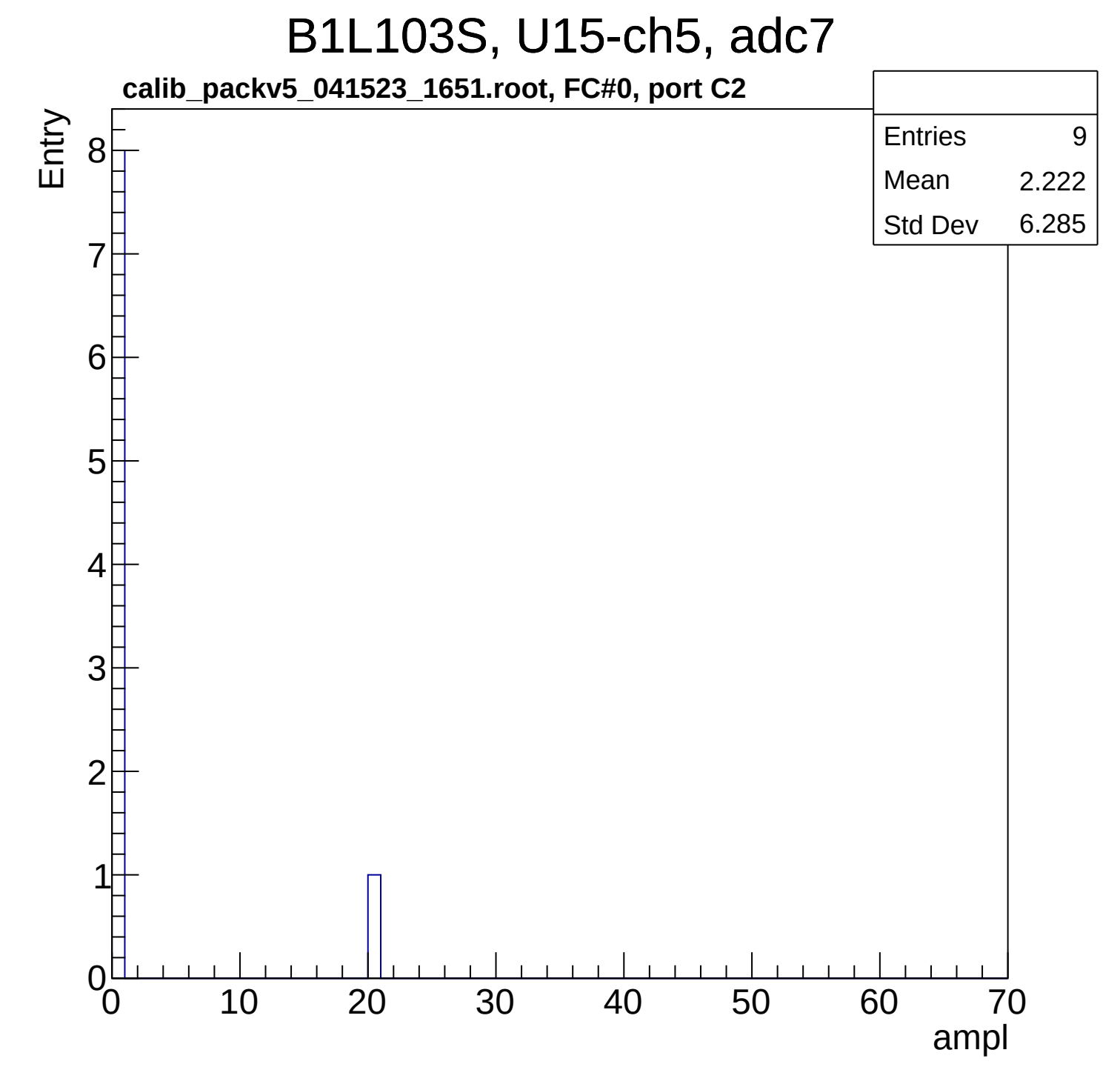

B1L103S, U15-ch5, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 34.58
Std Dev 14.93
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

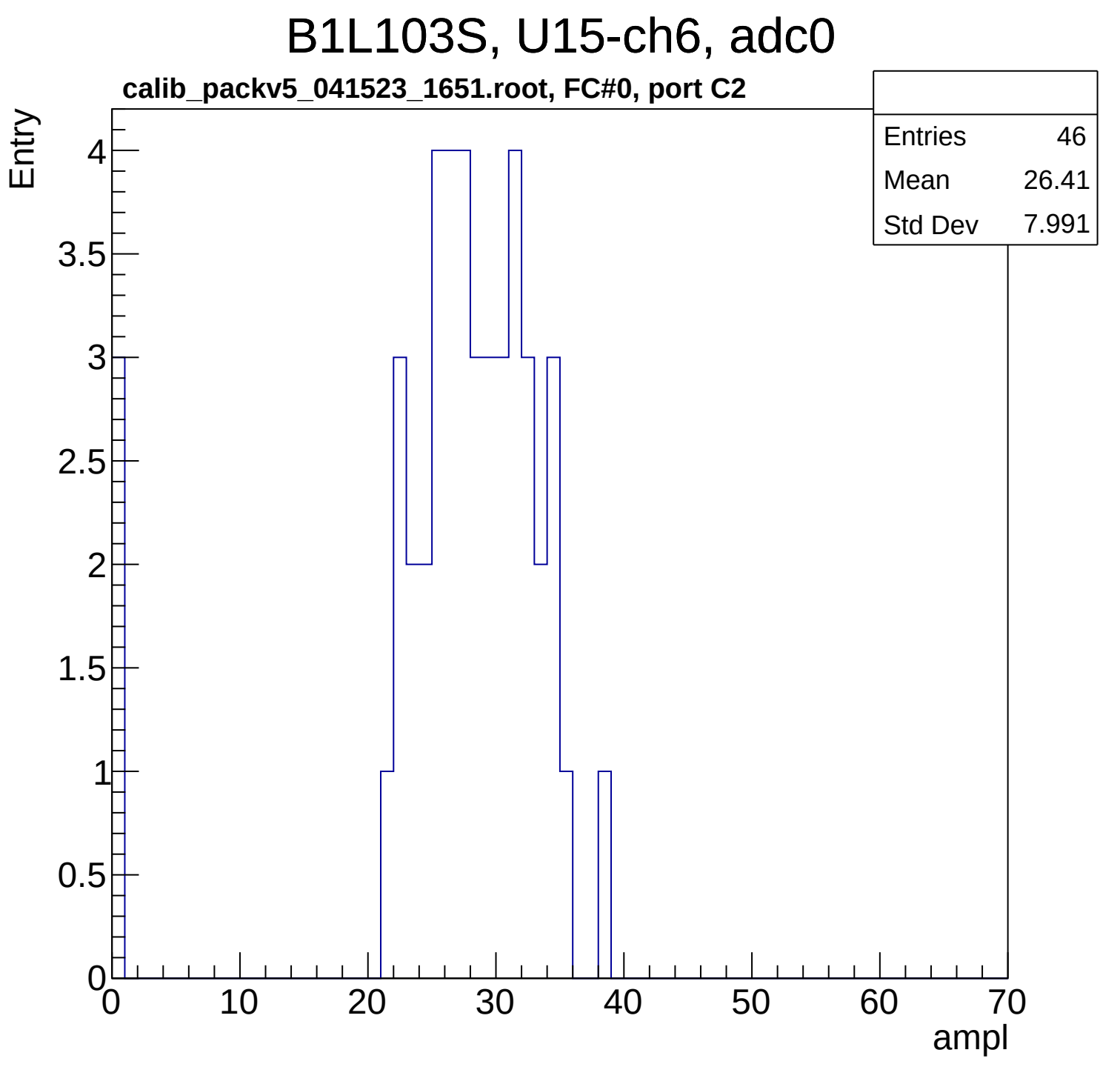

B1L103S, U15-ch5, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 45.79
Std Dev 11.22
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

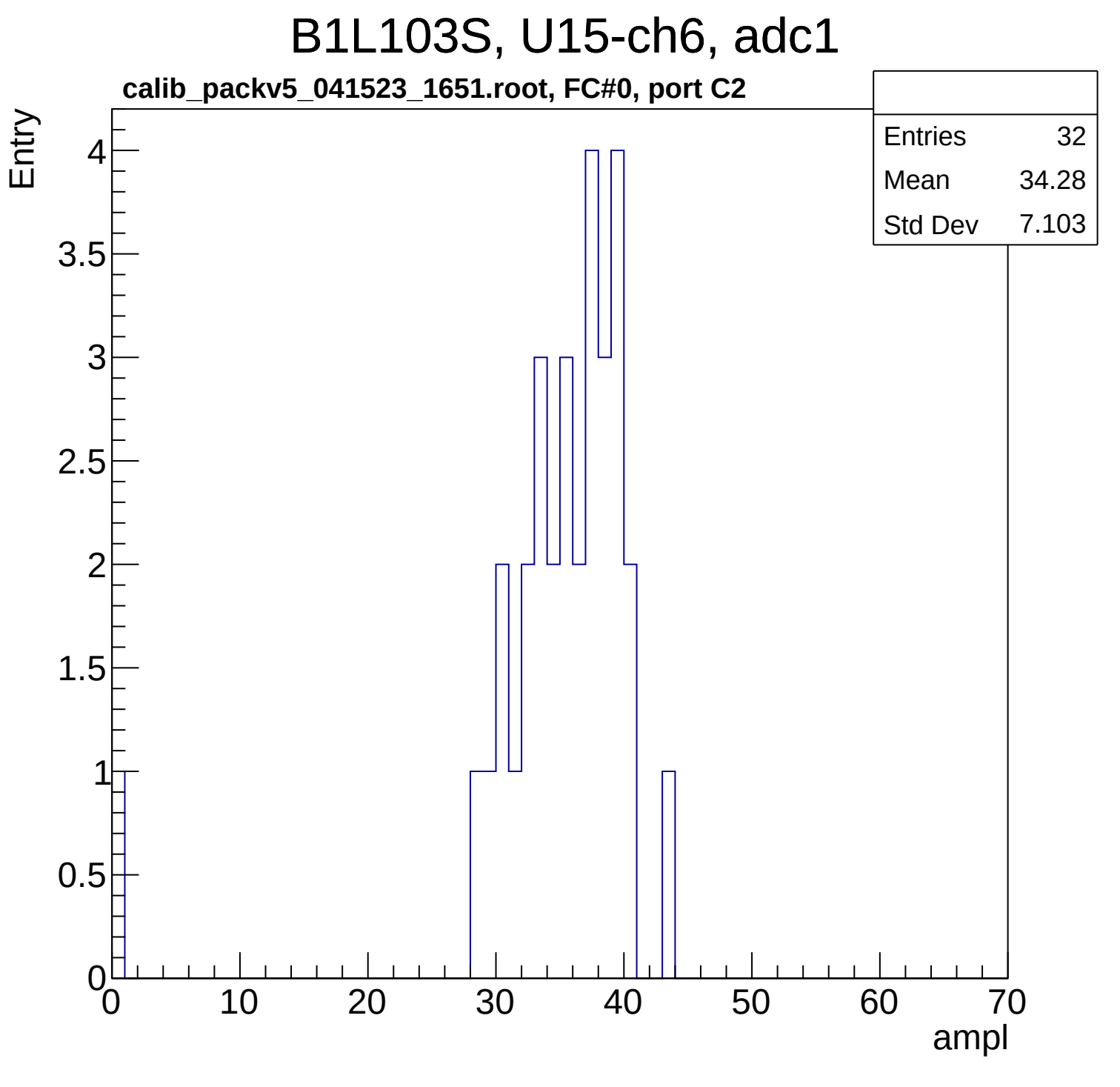

B1L103S, U15-ch5, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 55.53
Std Dev 3.296
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

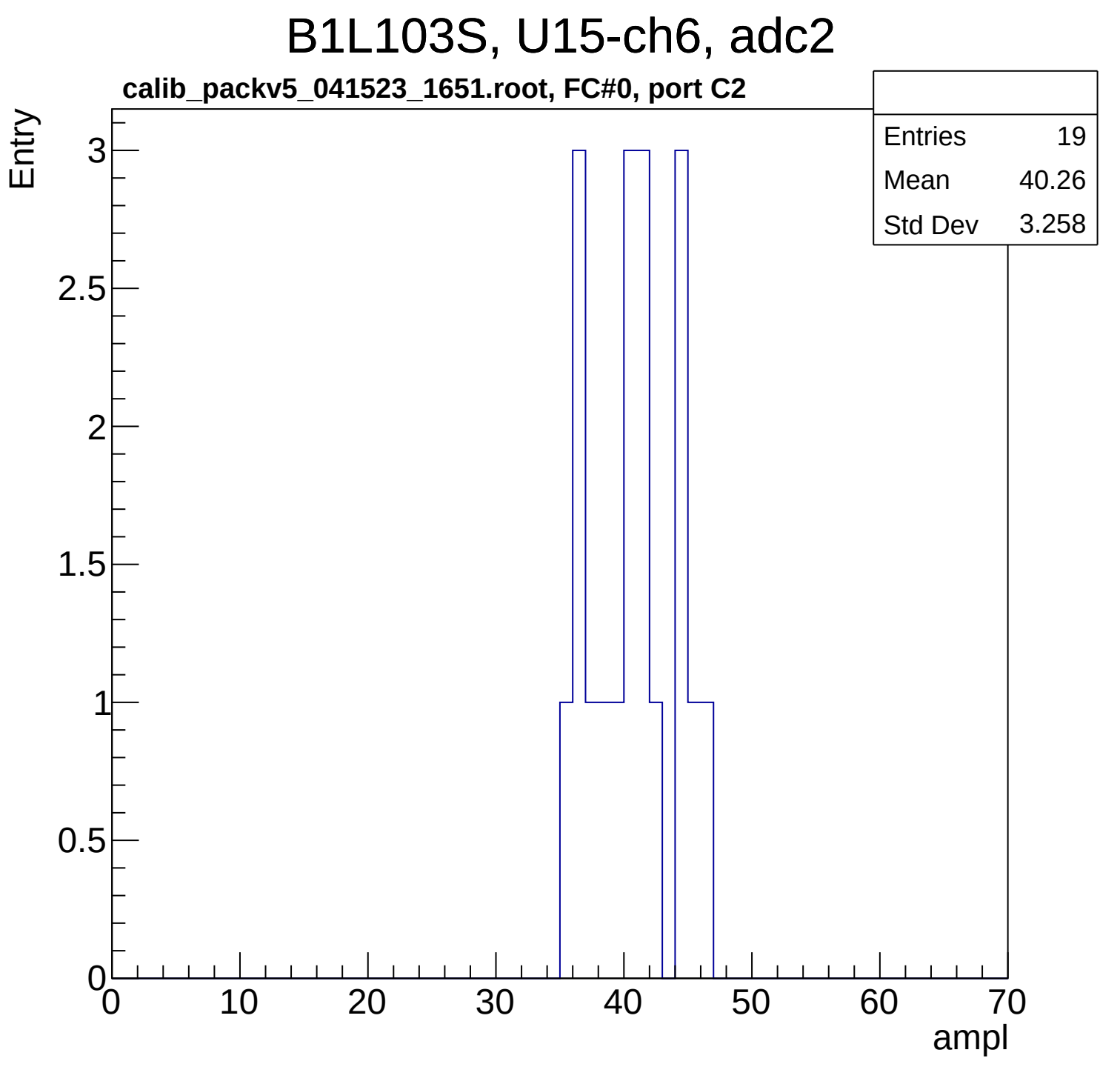

B1L103S, U15-ch5, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 57.16
Std Dev 13.57
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch5, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61.75
Std Dev 1.299
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U15-ch5, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 2.222
Std Dev 6.285
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U15-ch6, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 26.41
Std Dev 7.991
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch6, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 34.28
Std Dev 7.103
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch6, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 40.26
Std Dev 3.258
Entry
ampl
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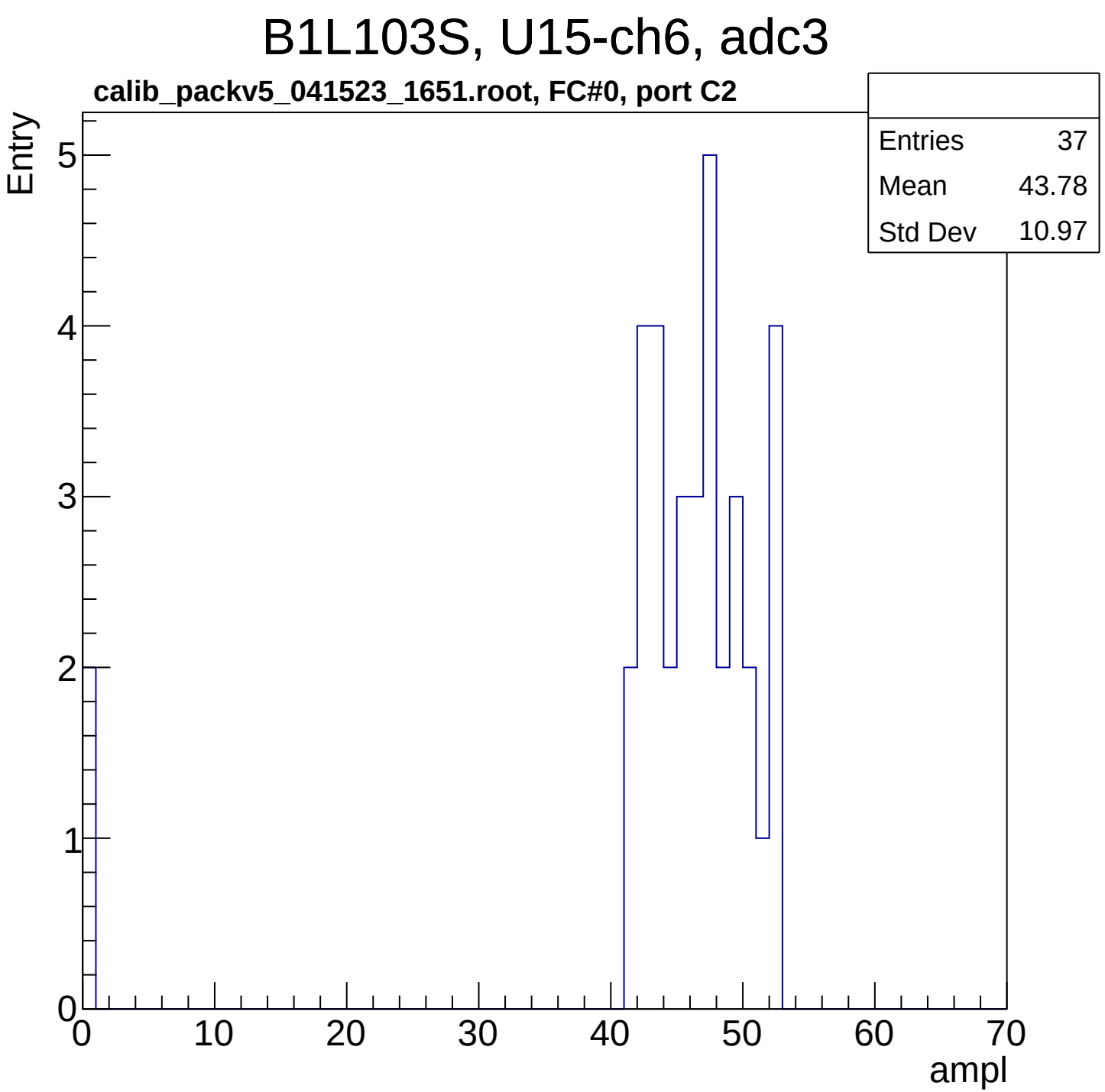
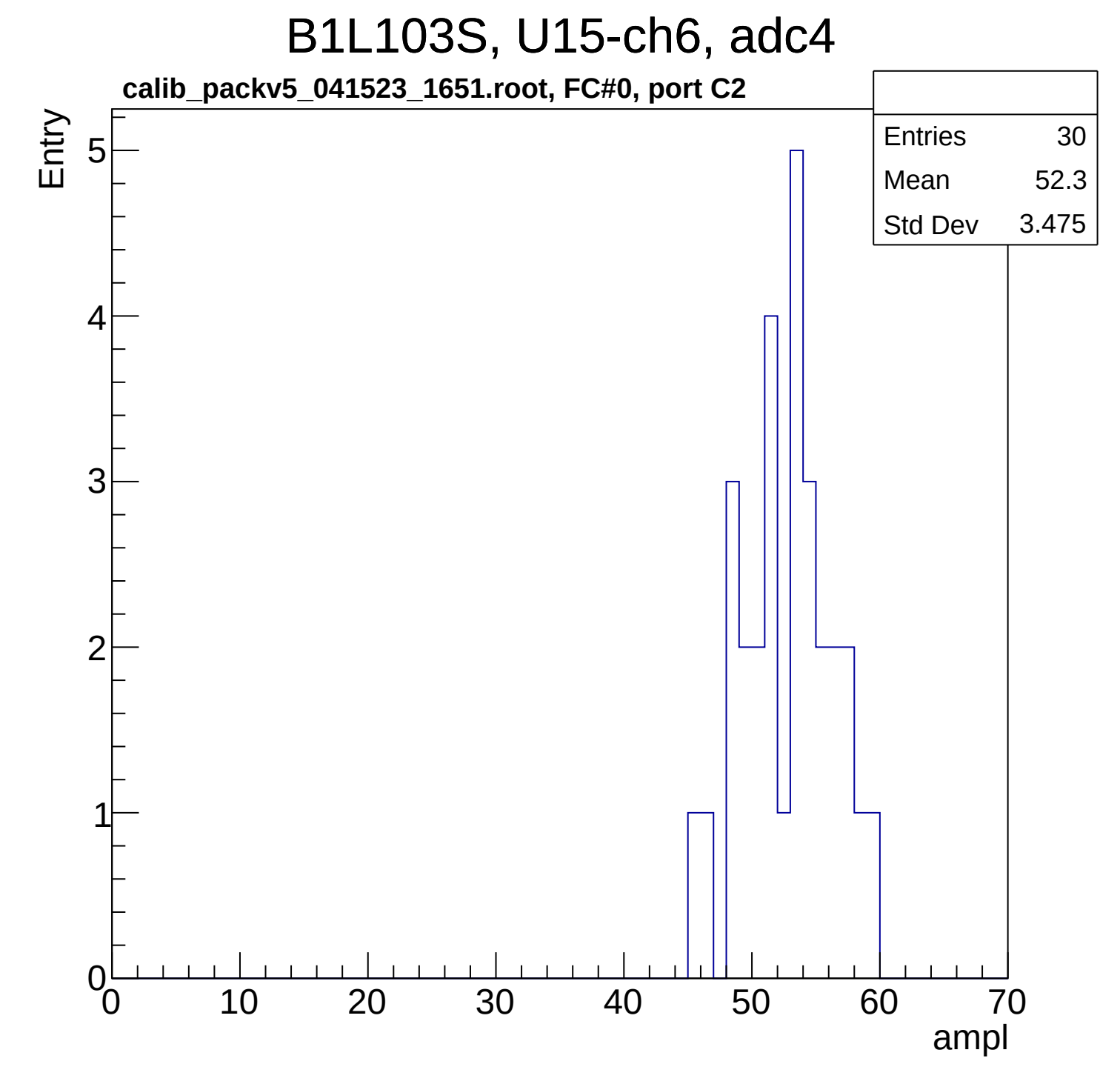
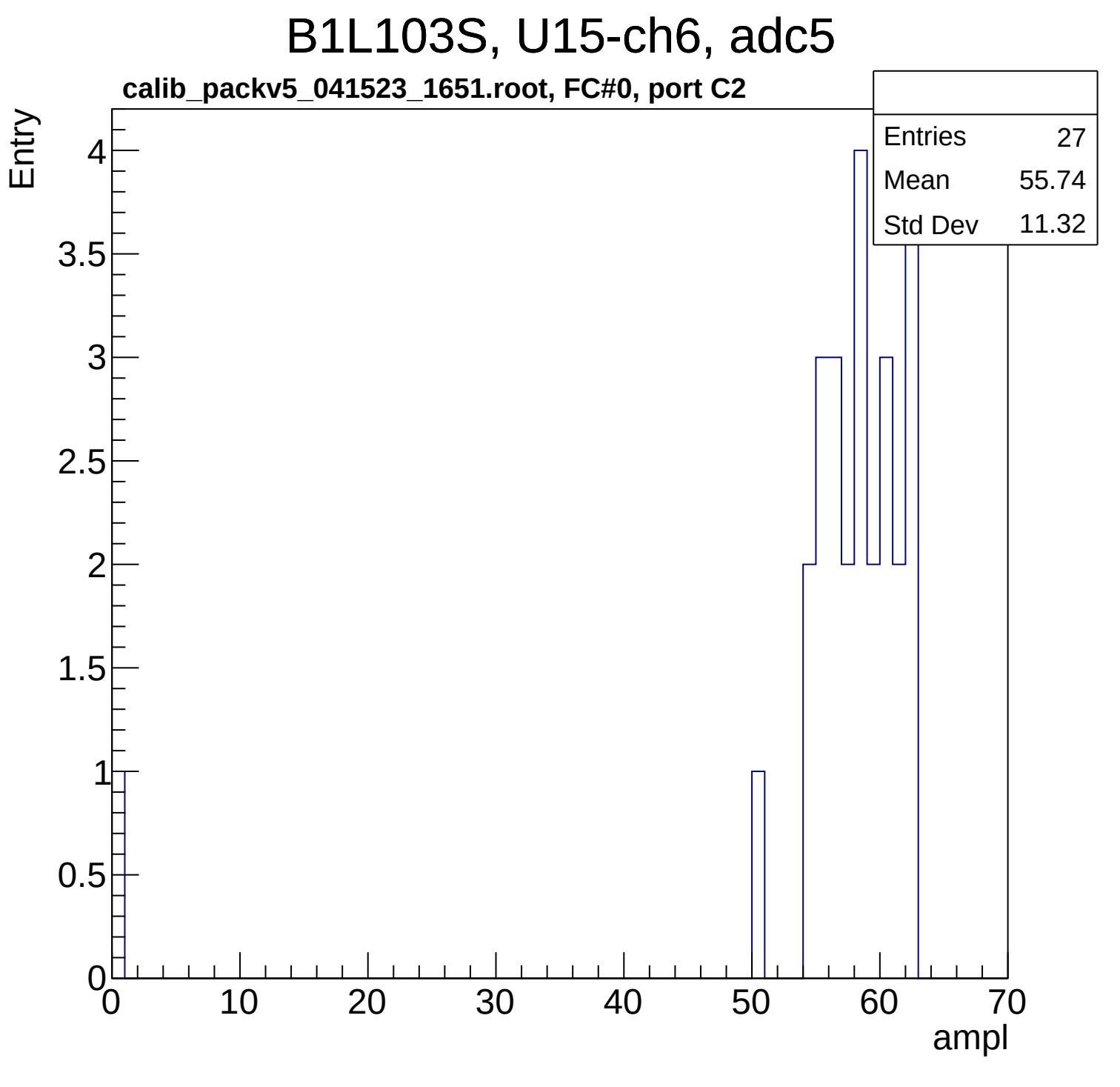
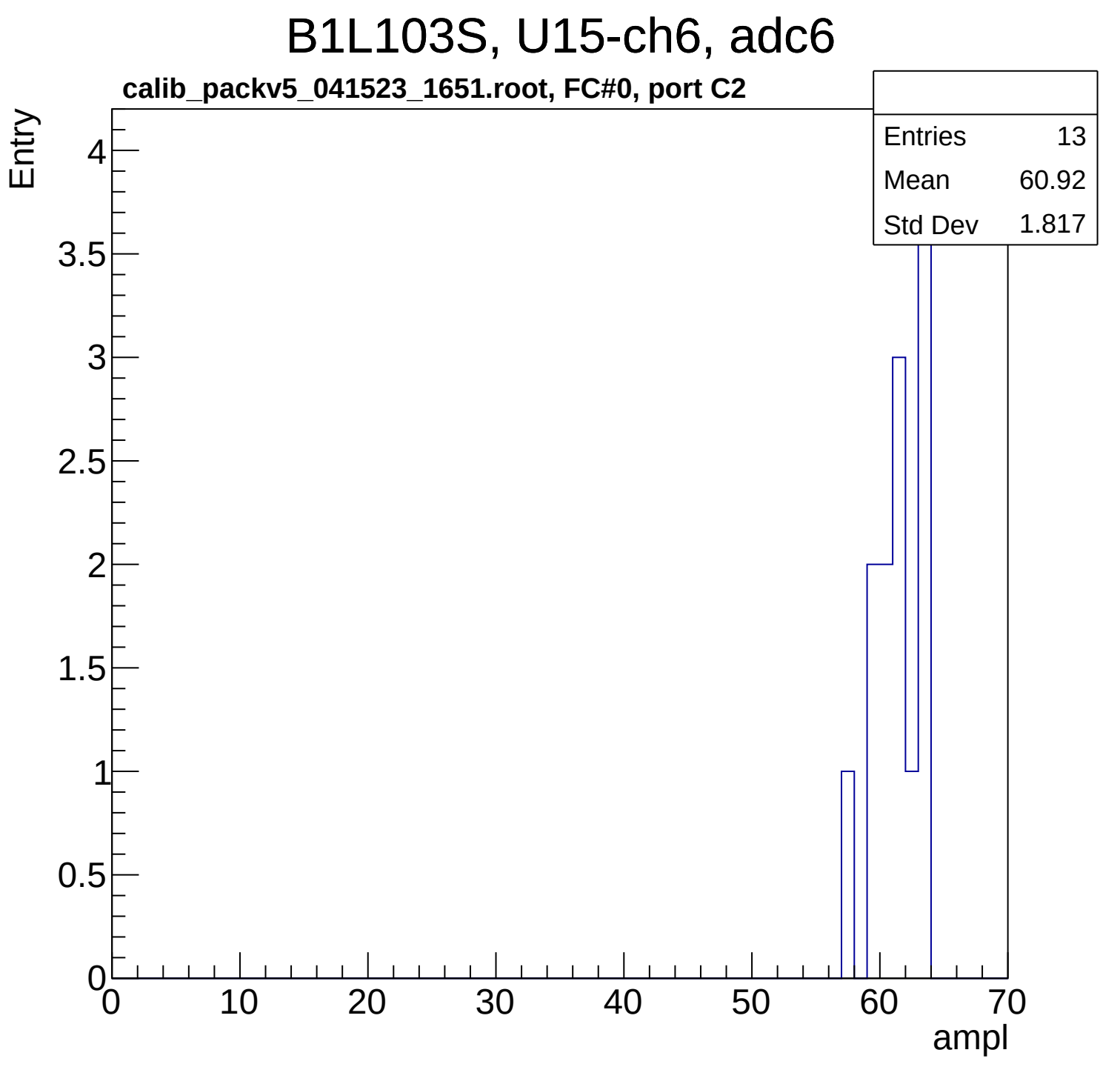
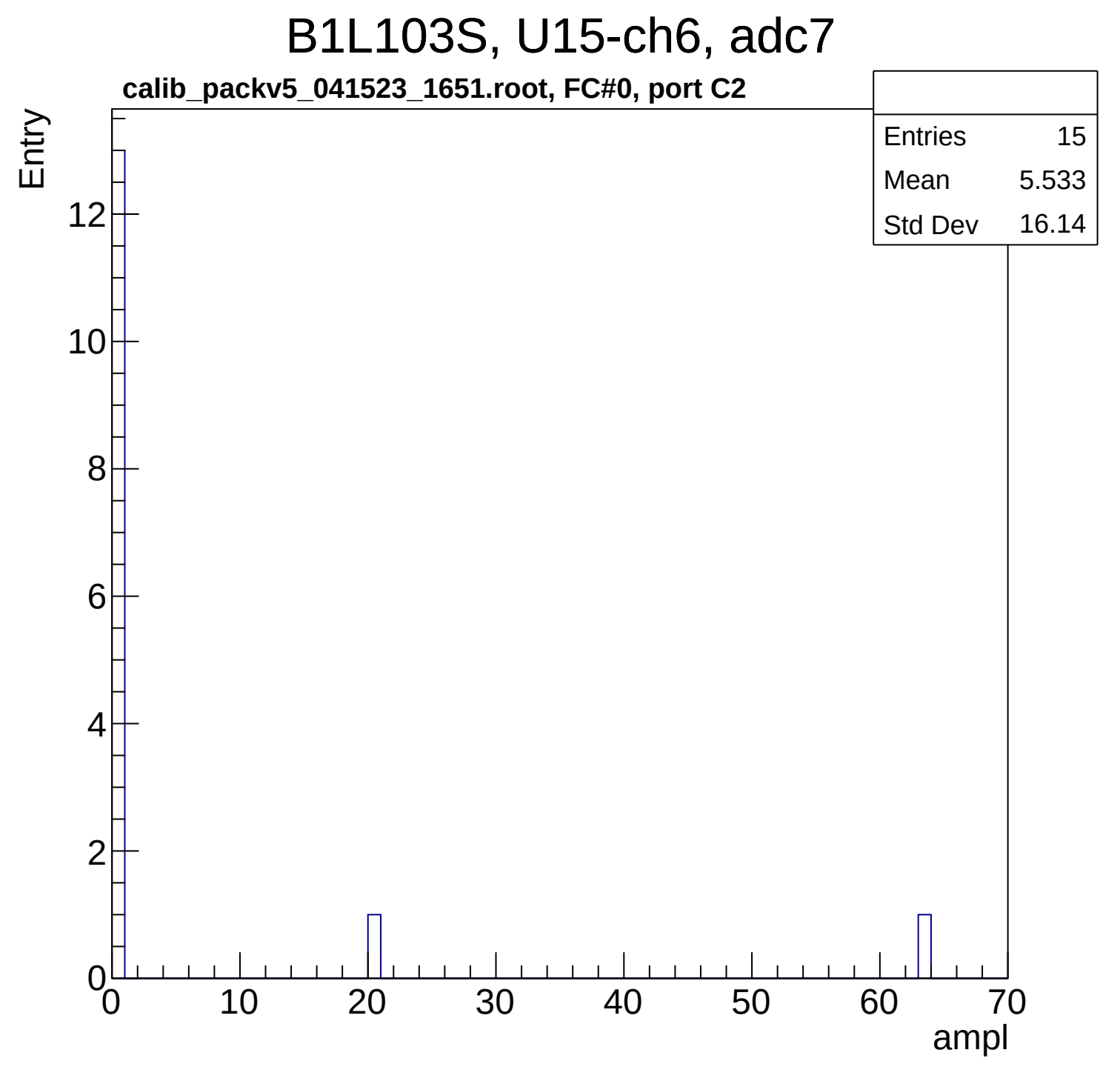
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

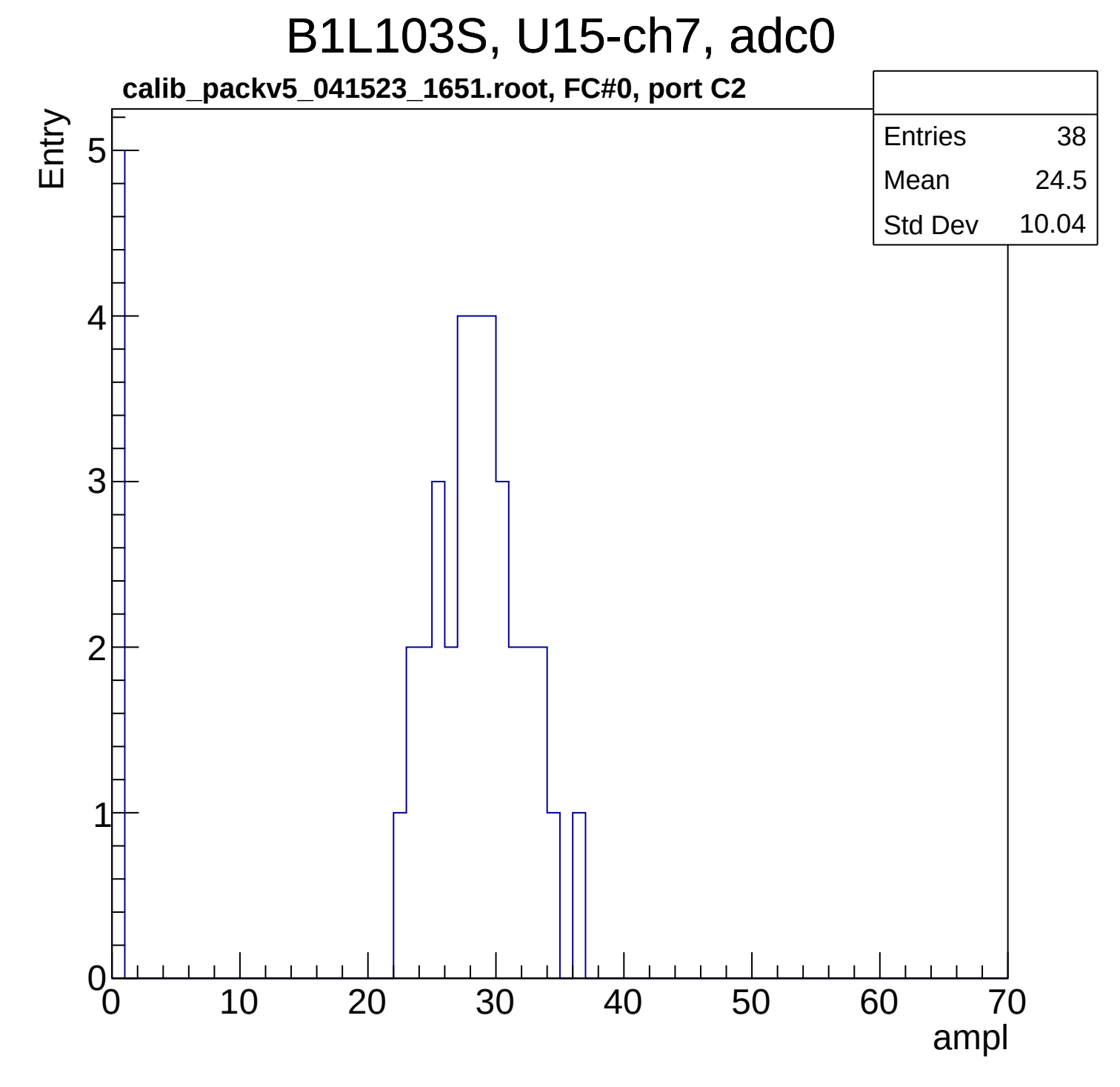

B1L103S, U15-ch6, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 43.78
Std Dev 10.97
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

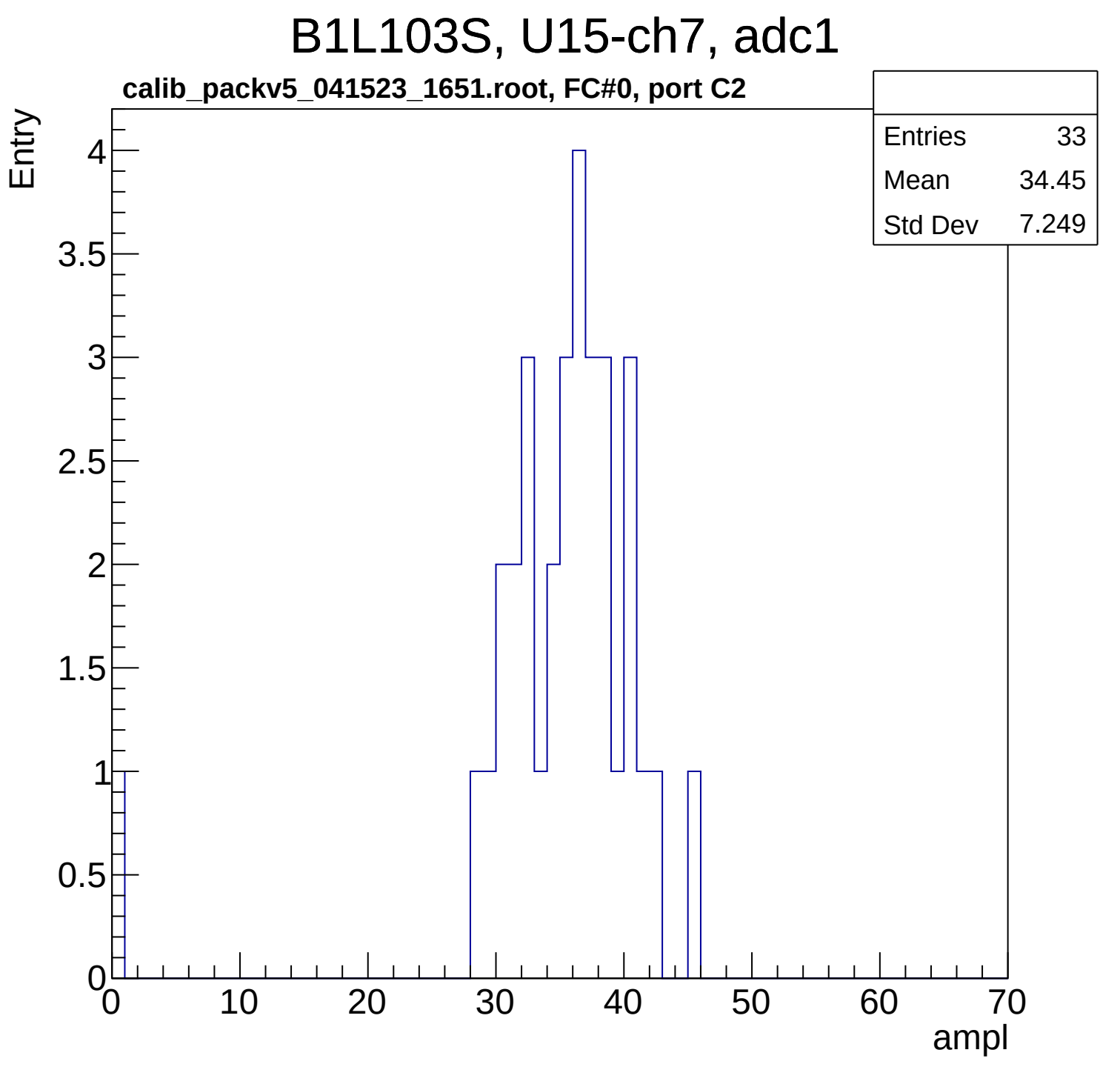

B1L103S, U15-ch6, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 52.3
Std Dev 3.475
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch6, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 55.74
Std Dev 11.32
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch6, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 60.92
Std Dev 1.817
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch6, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 5.533
Std Dev 16.14
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch7, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 24.5
Std Dev 10.04
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch7, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 34.45
Std Dev 7.249
Entry
ampl
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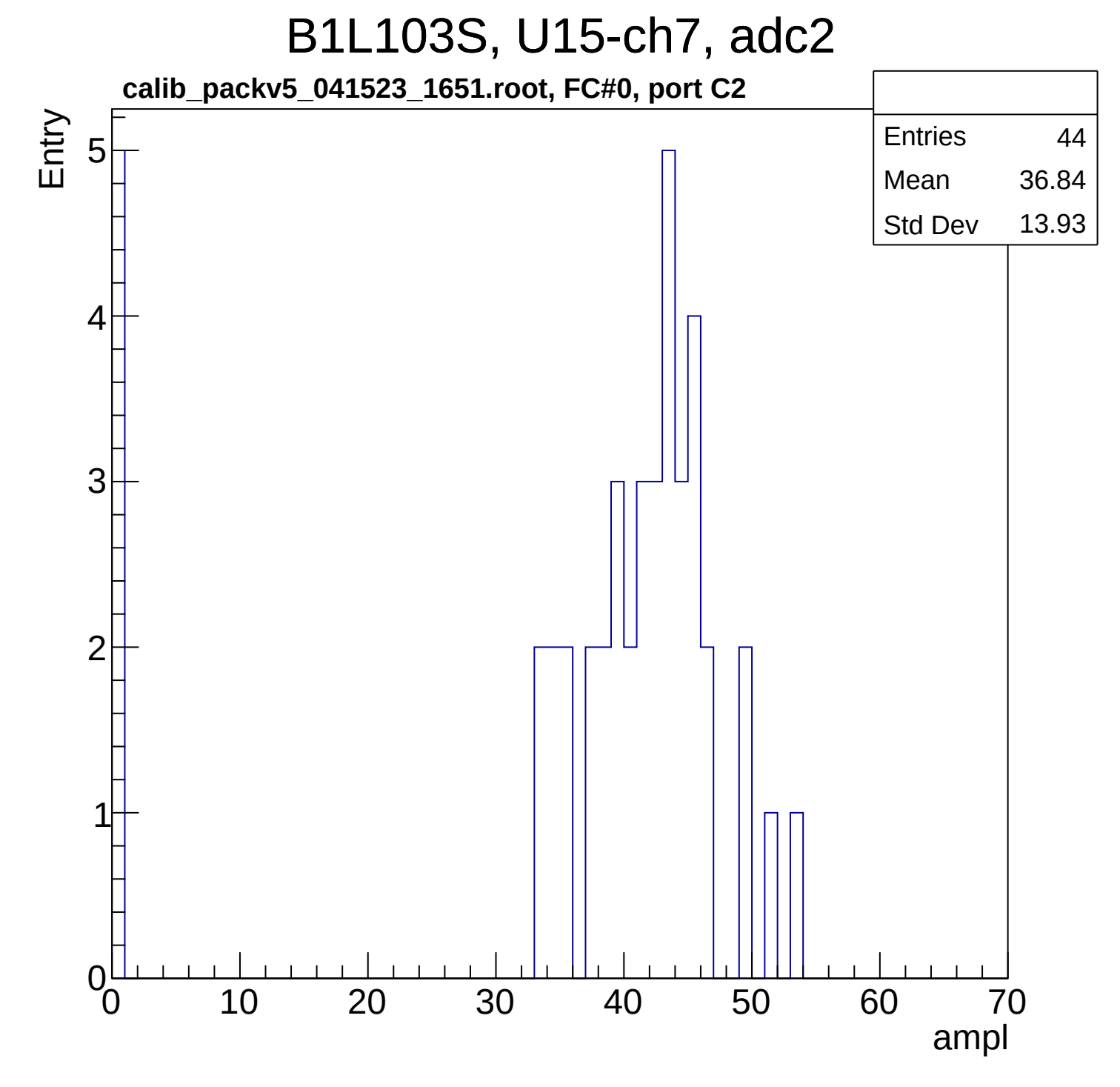
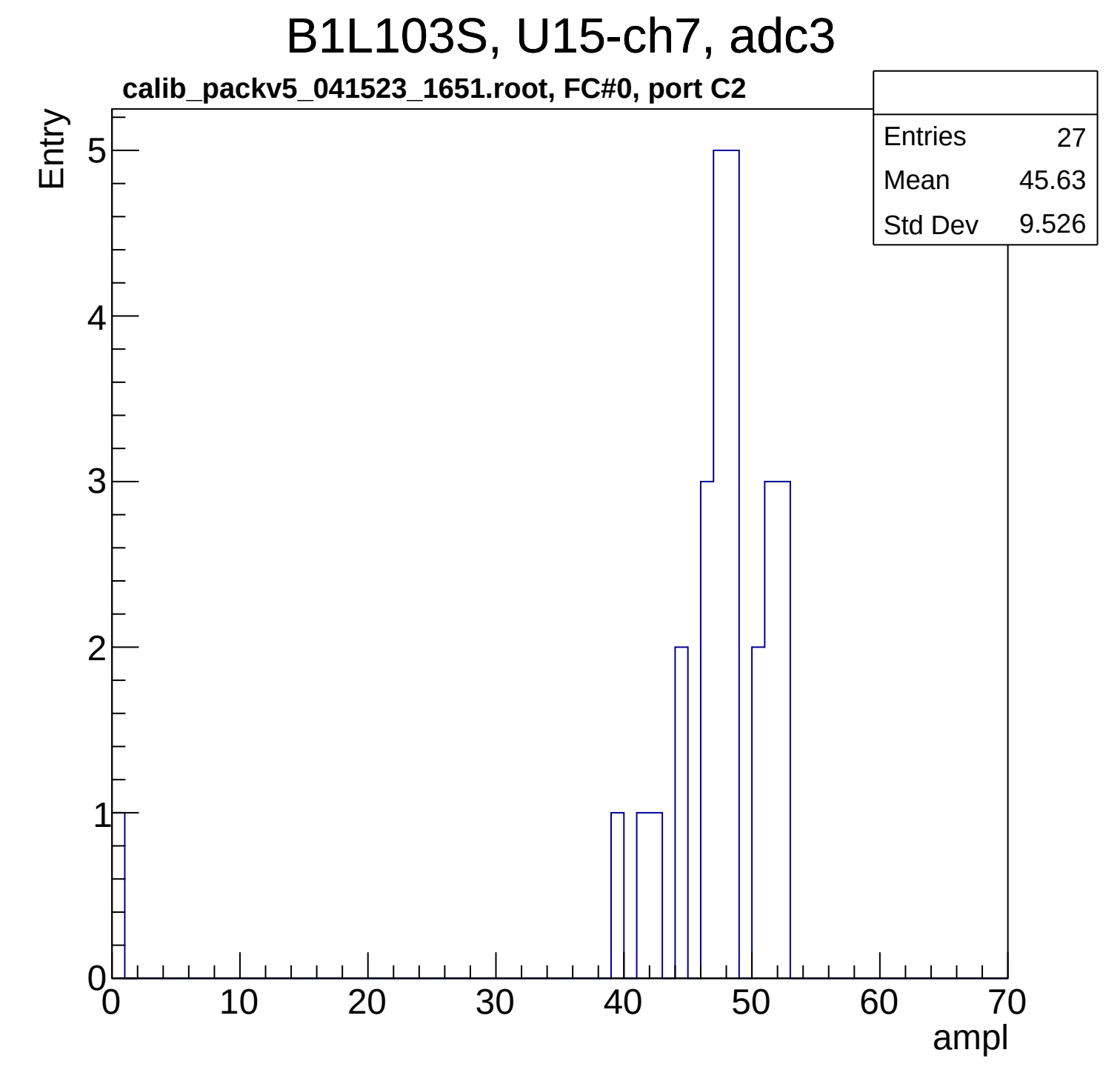
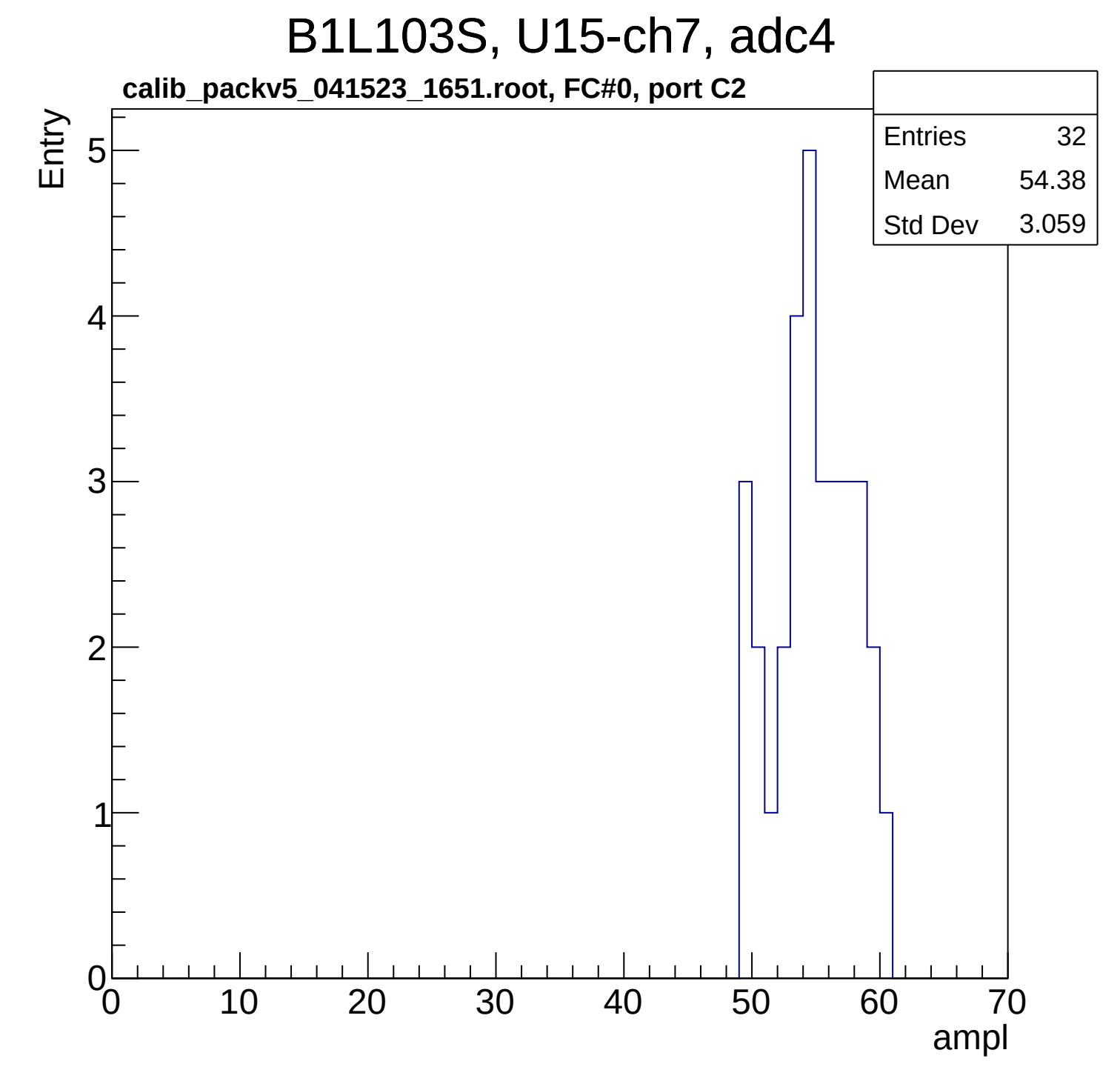
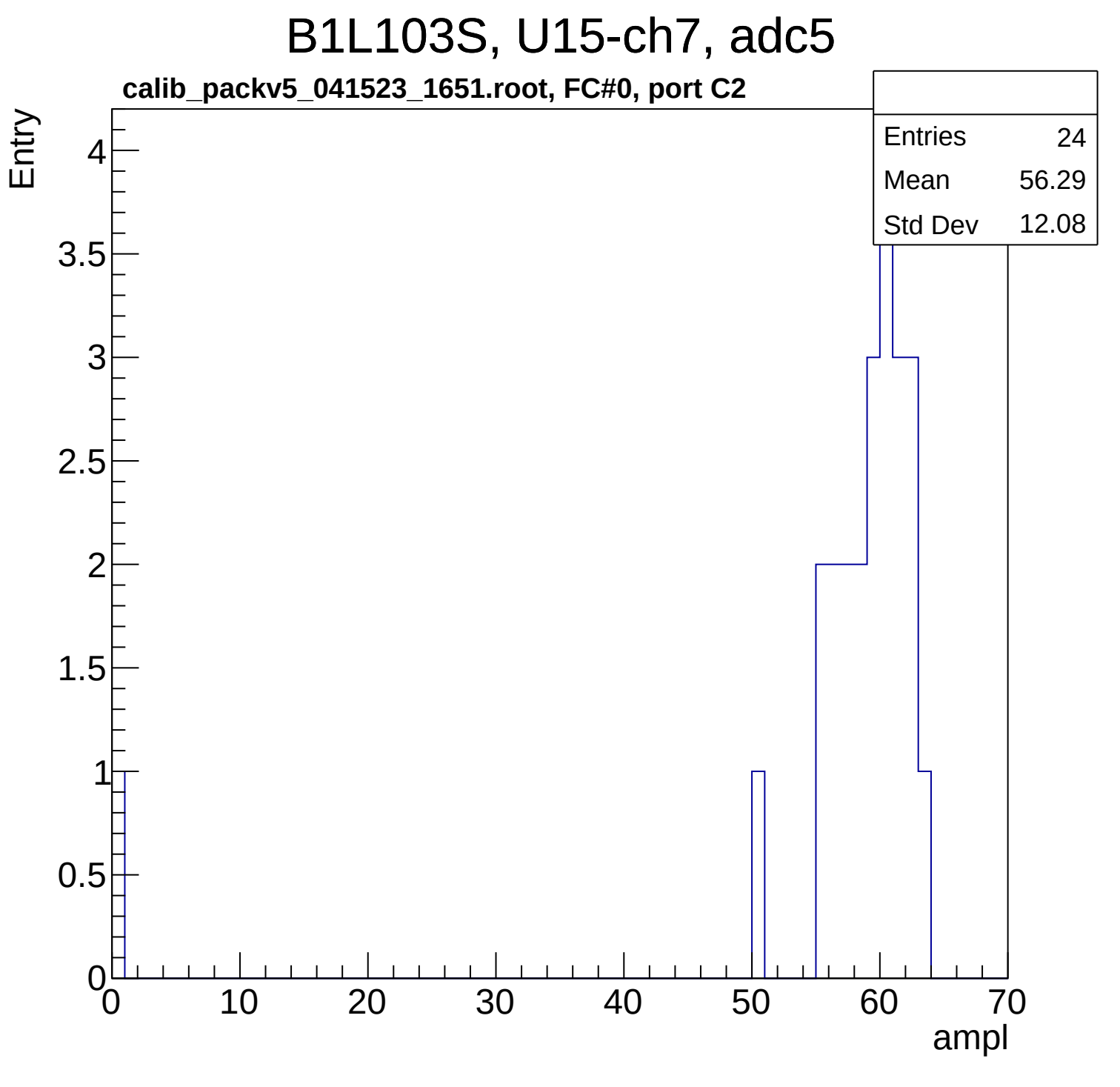
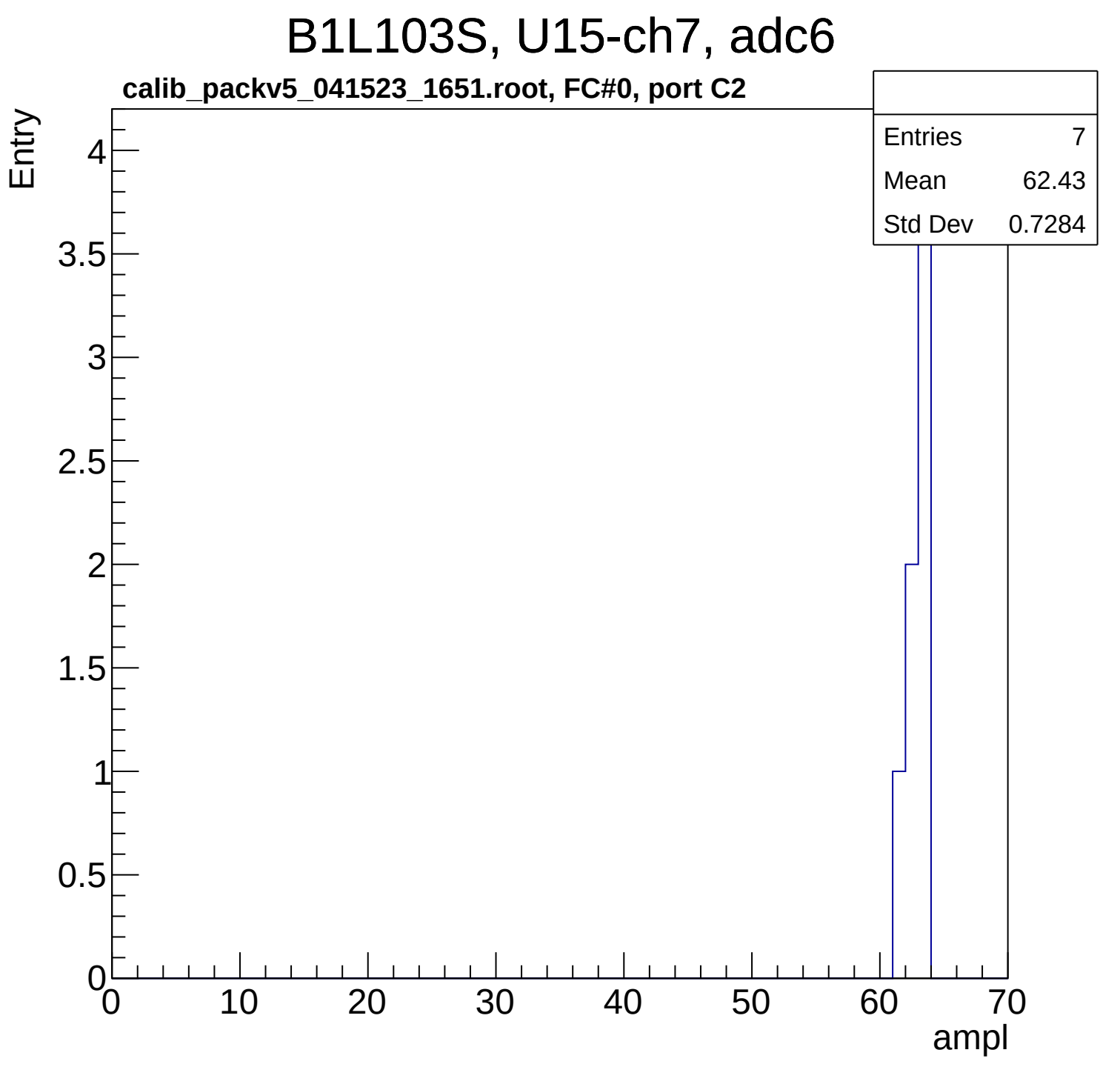
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

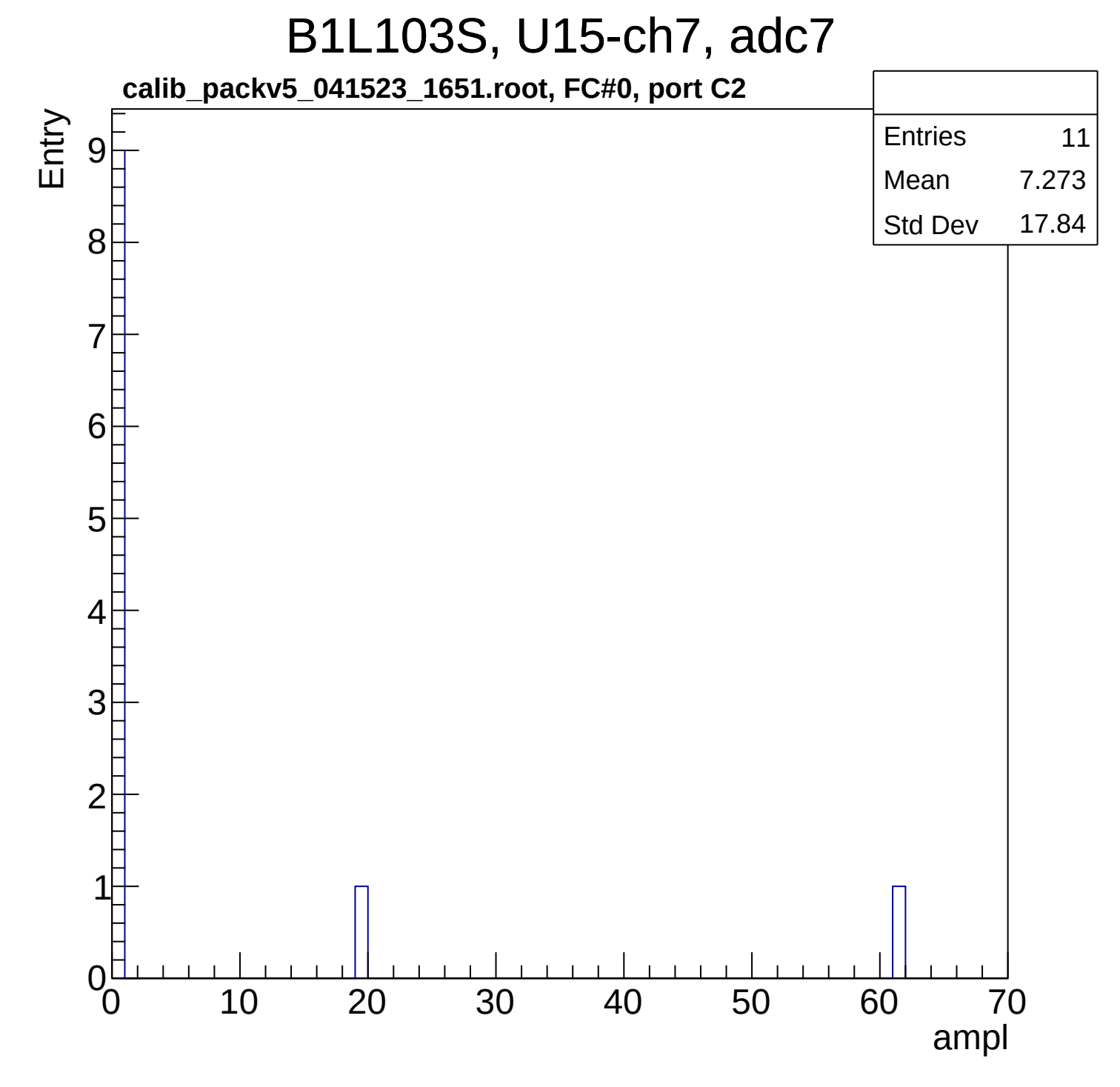

B1L103S, U15-ch7, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 36.84
Std Dev 13.93
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

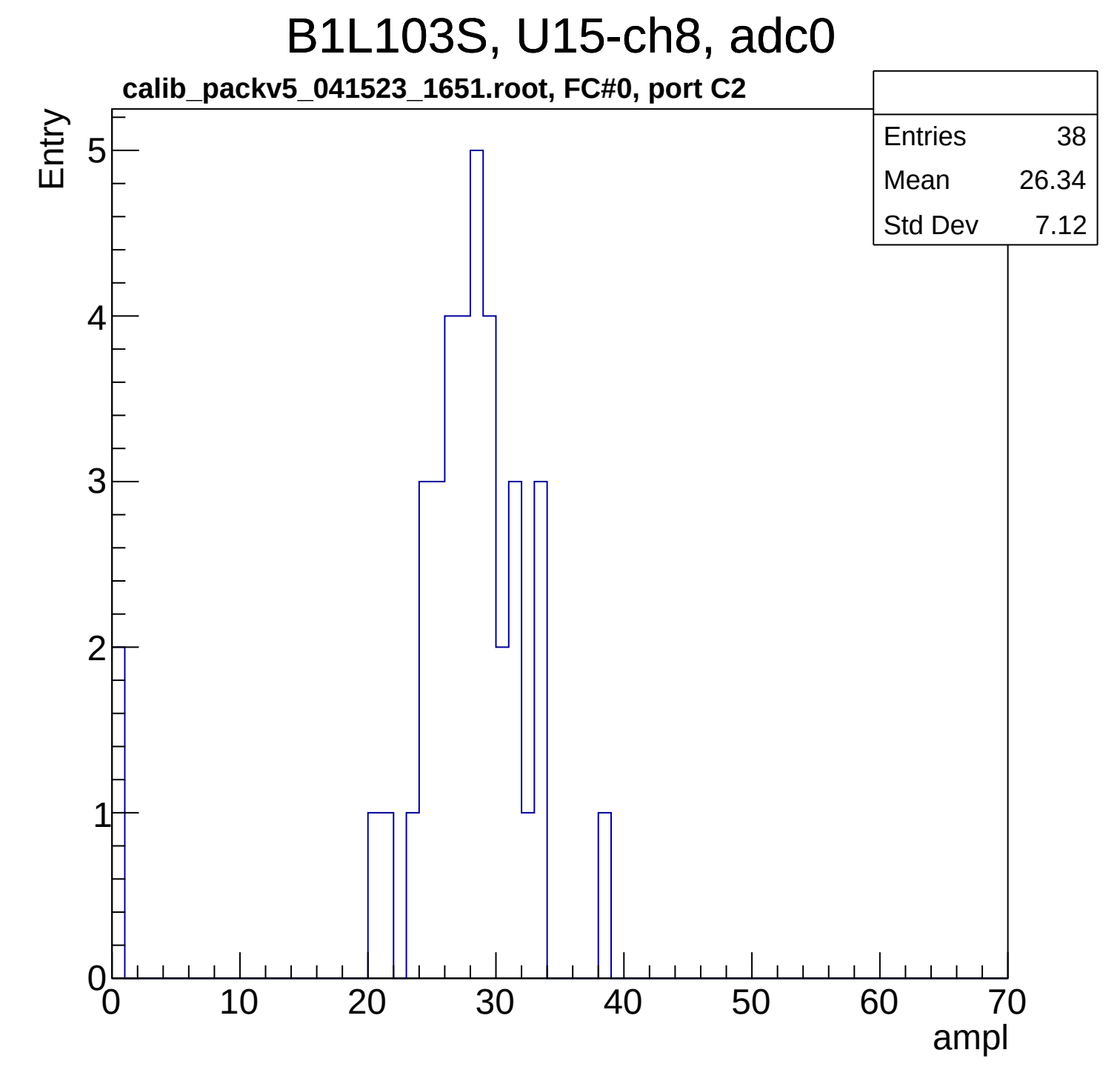

B1L103S, U15-ch7, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 45.63
Std Dev 9.526
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

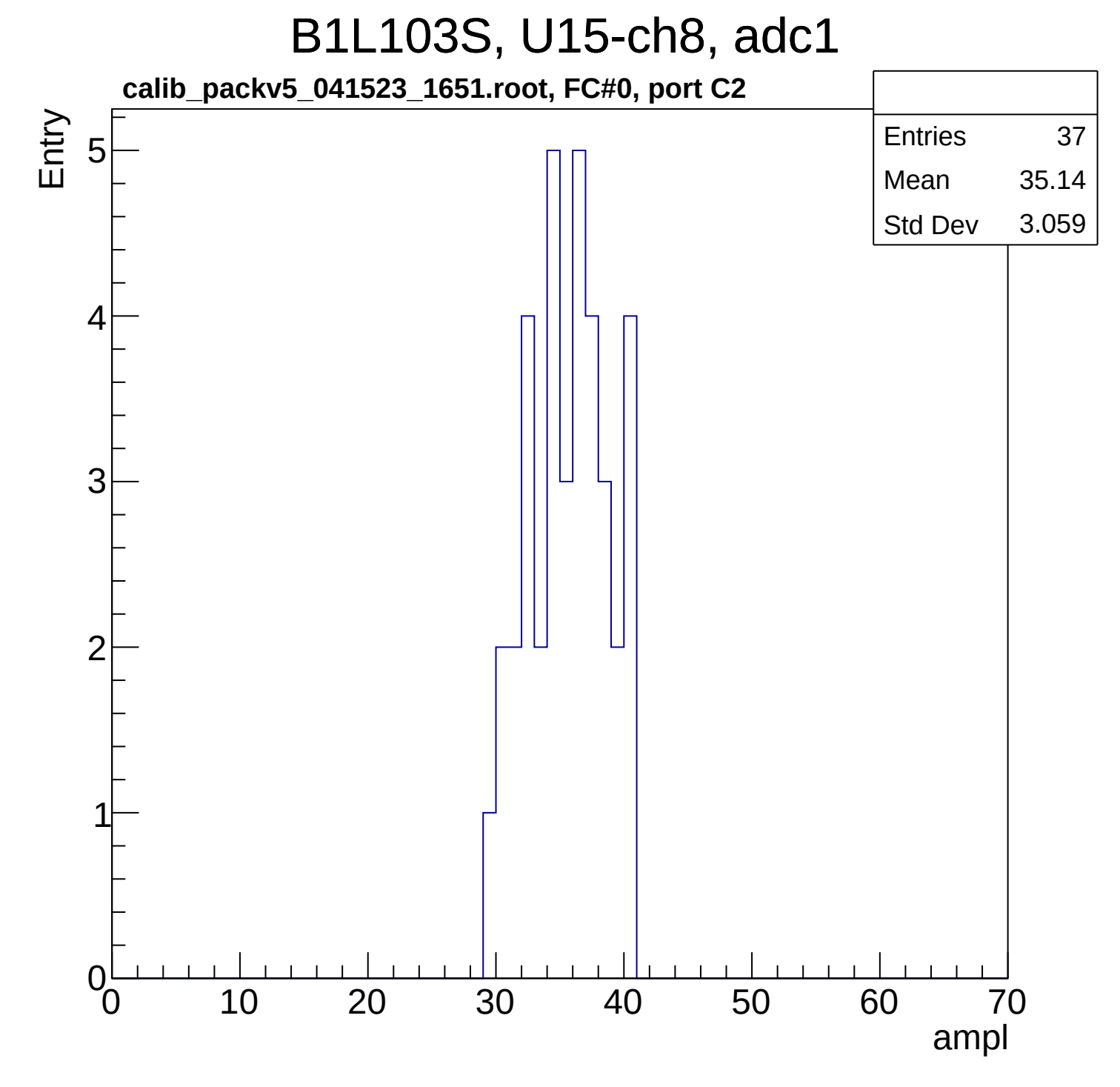

B1L103S, U15-ch7, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 54.38
Std Dev 3.059
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

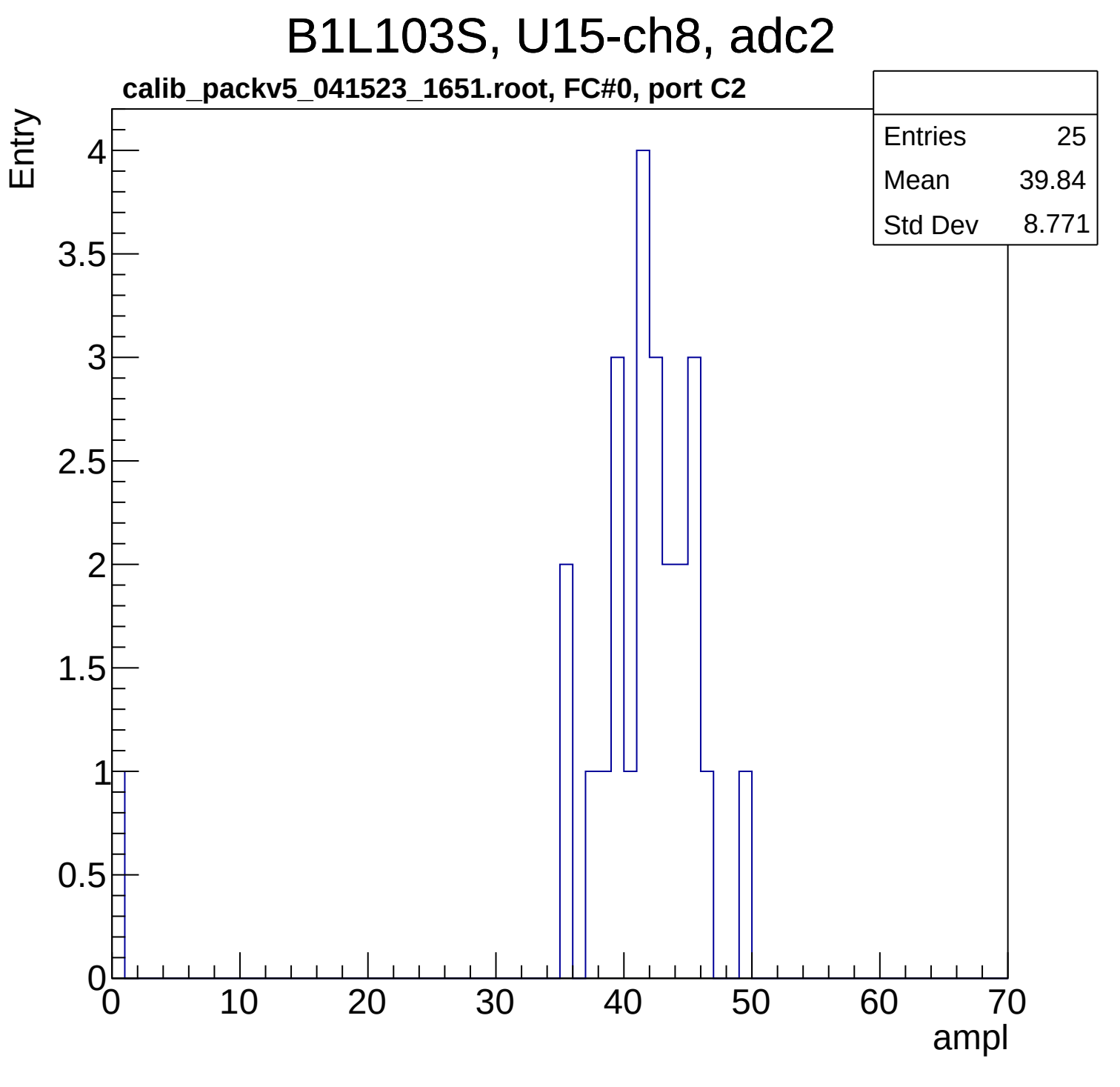

B1L103S, U15-ch7, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 56.29
Std Dev 12.08
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

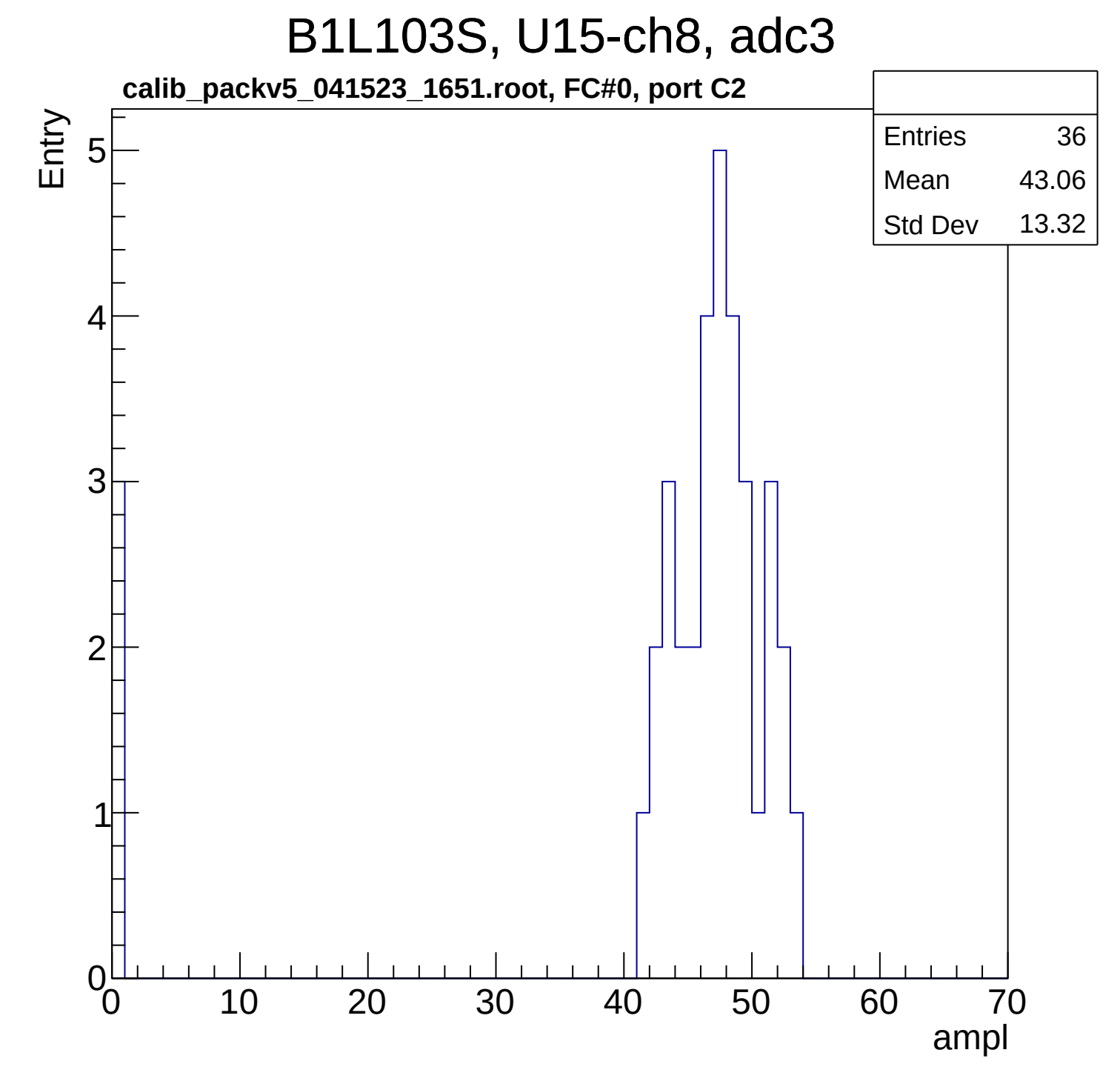

B1L103S, U15-ch7, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62.43
Std Dev 0.7284
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

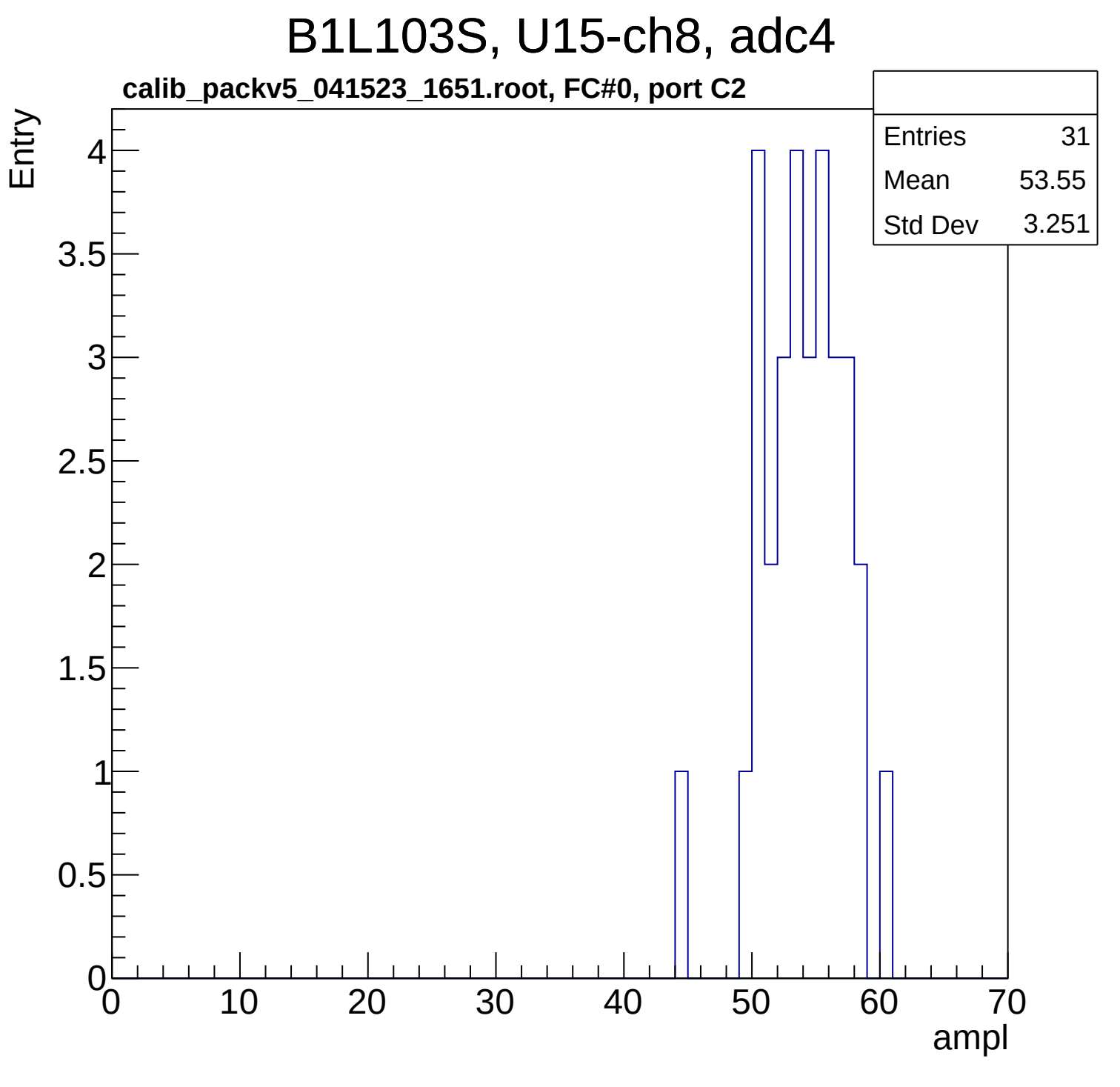

B1L103S, U15-ch7, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 7.273
Std Dev 17.84
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

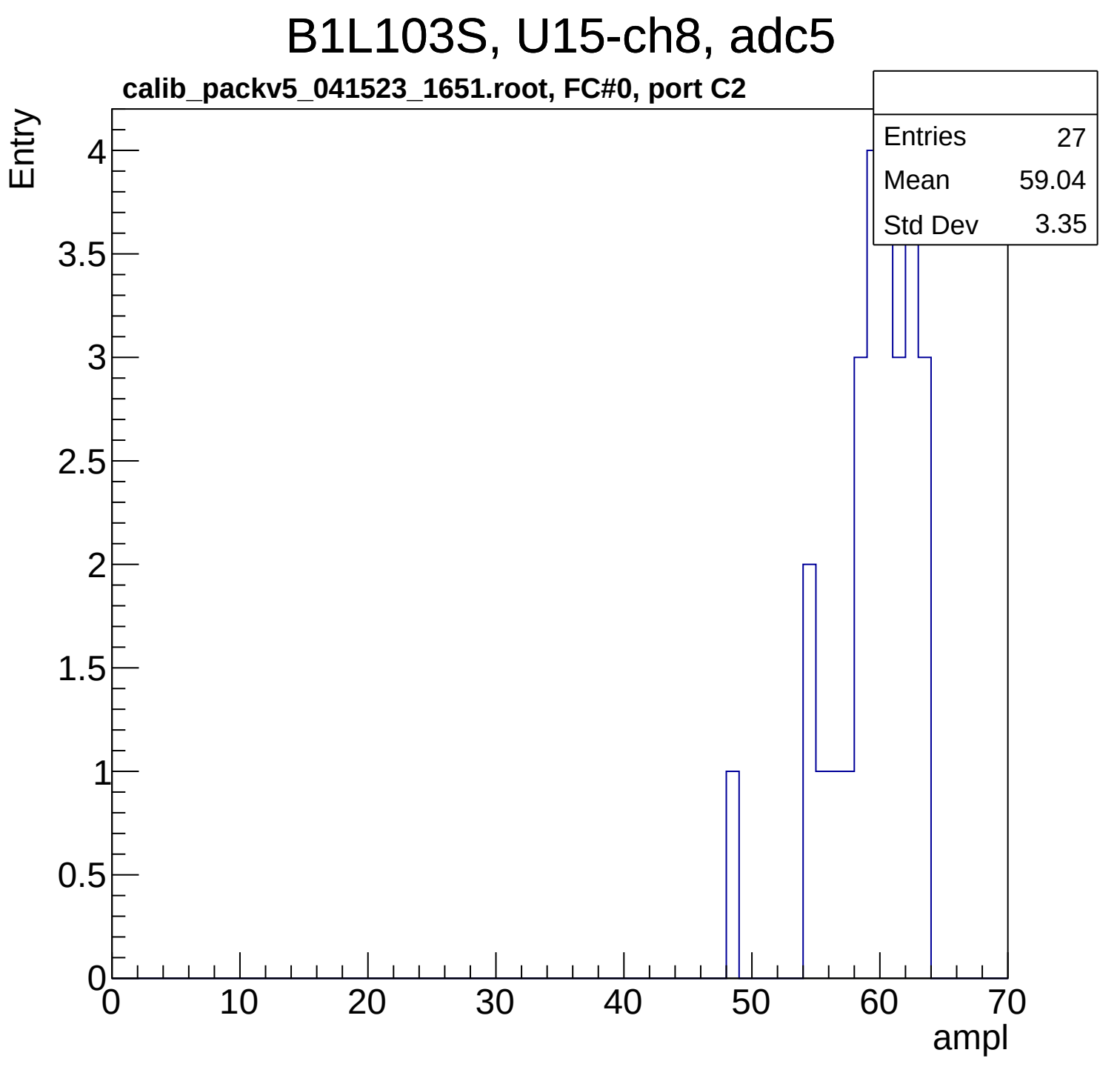

B1L103S, U15-ch8, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 26.34
Std Dev 7.12
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

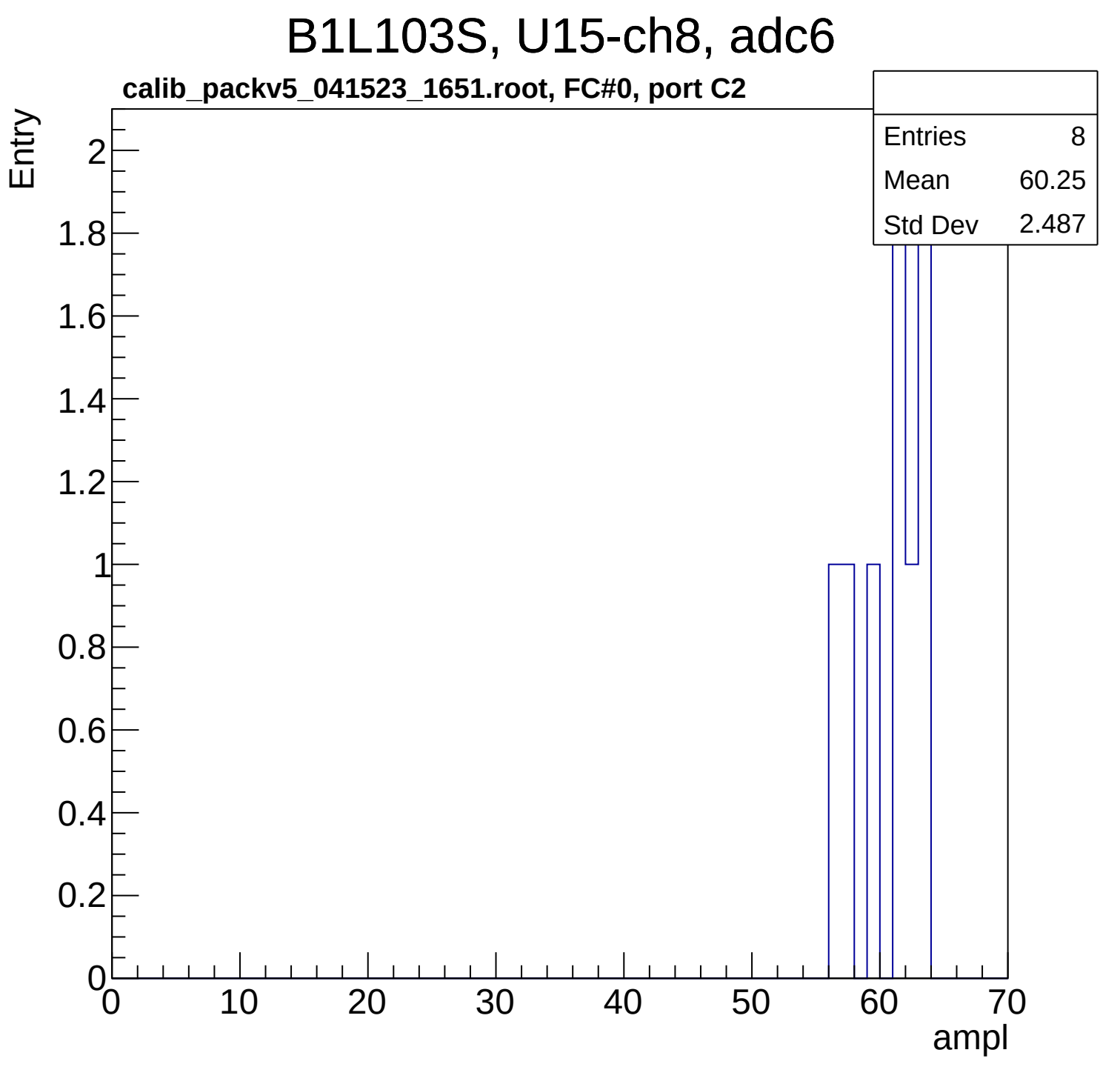

B1L103S, U15-ch8, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 35.14
Std Dev 3.059
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

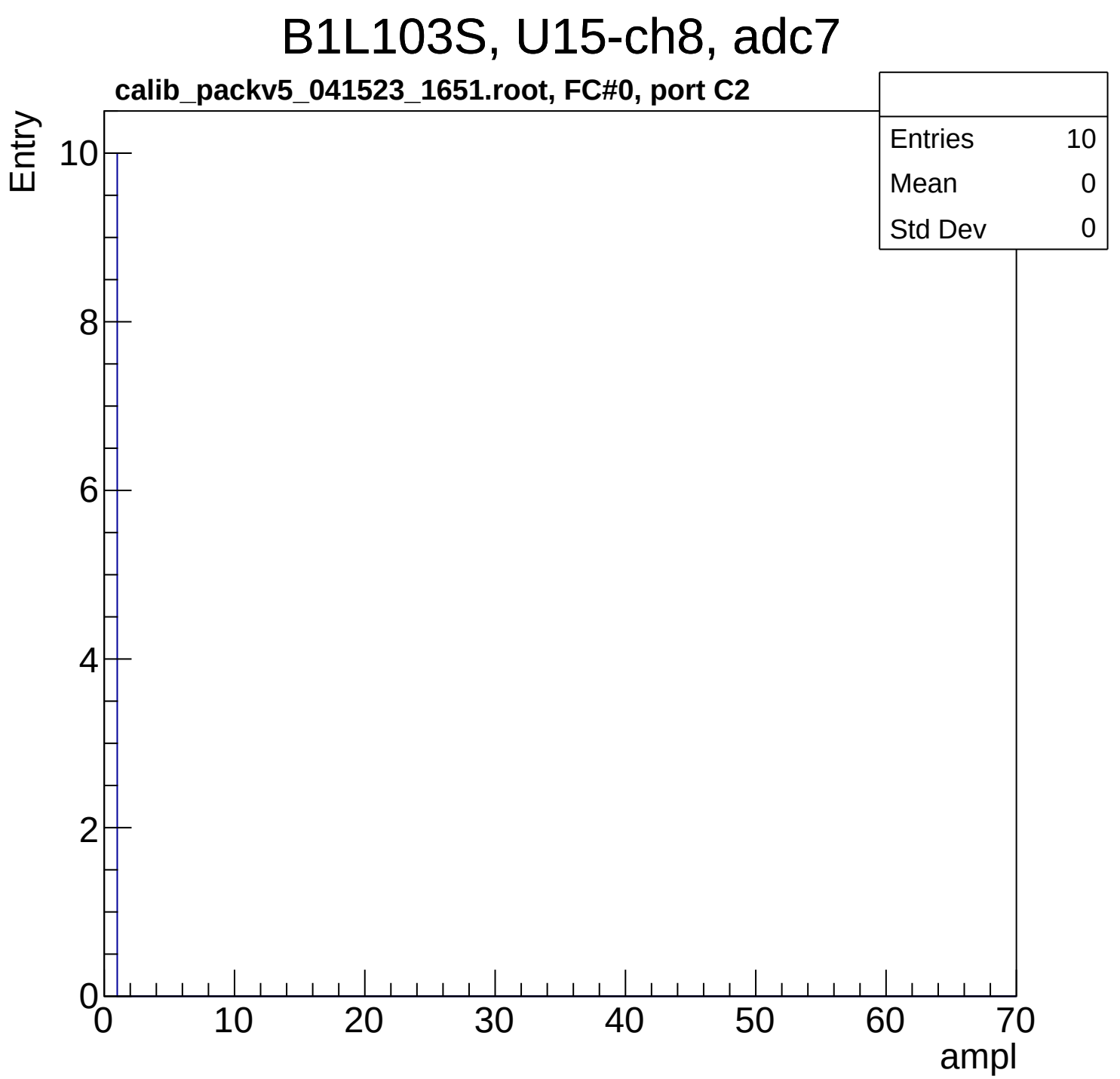

B1L103S, U15-ch8, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 39.84
Std Dev 8.771
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

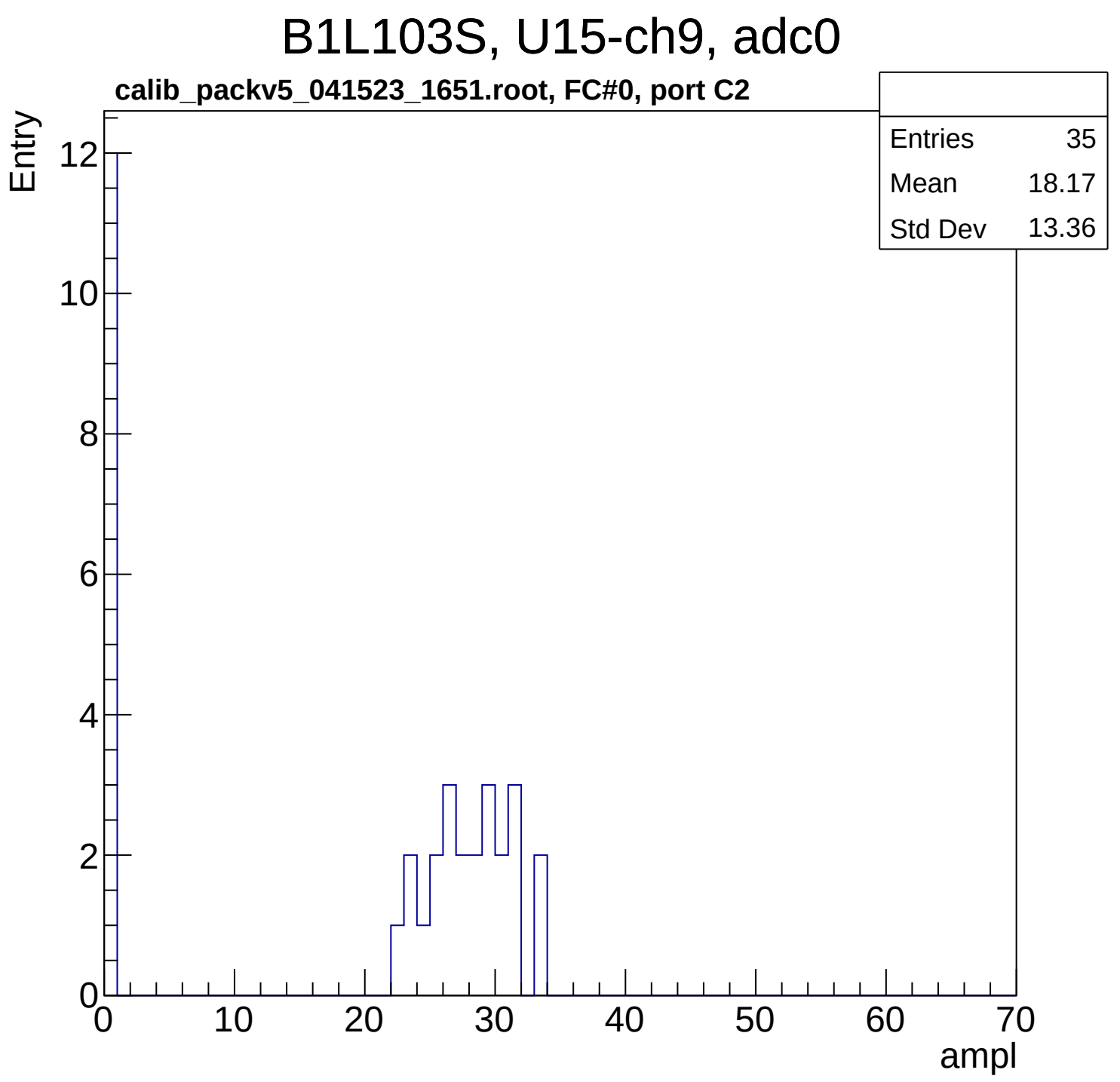

B1L103S, U15-ch8, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 43.06
Std Dev 13.32
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

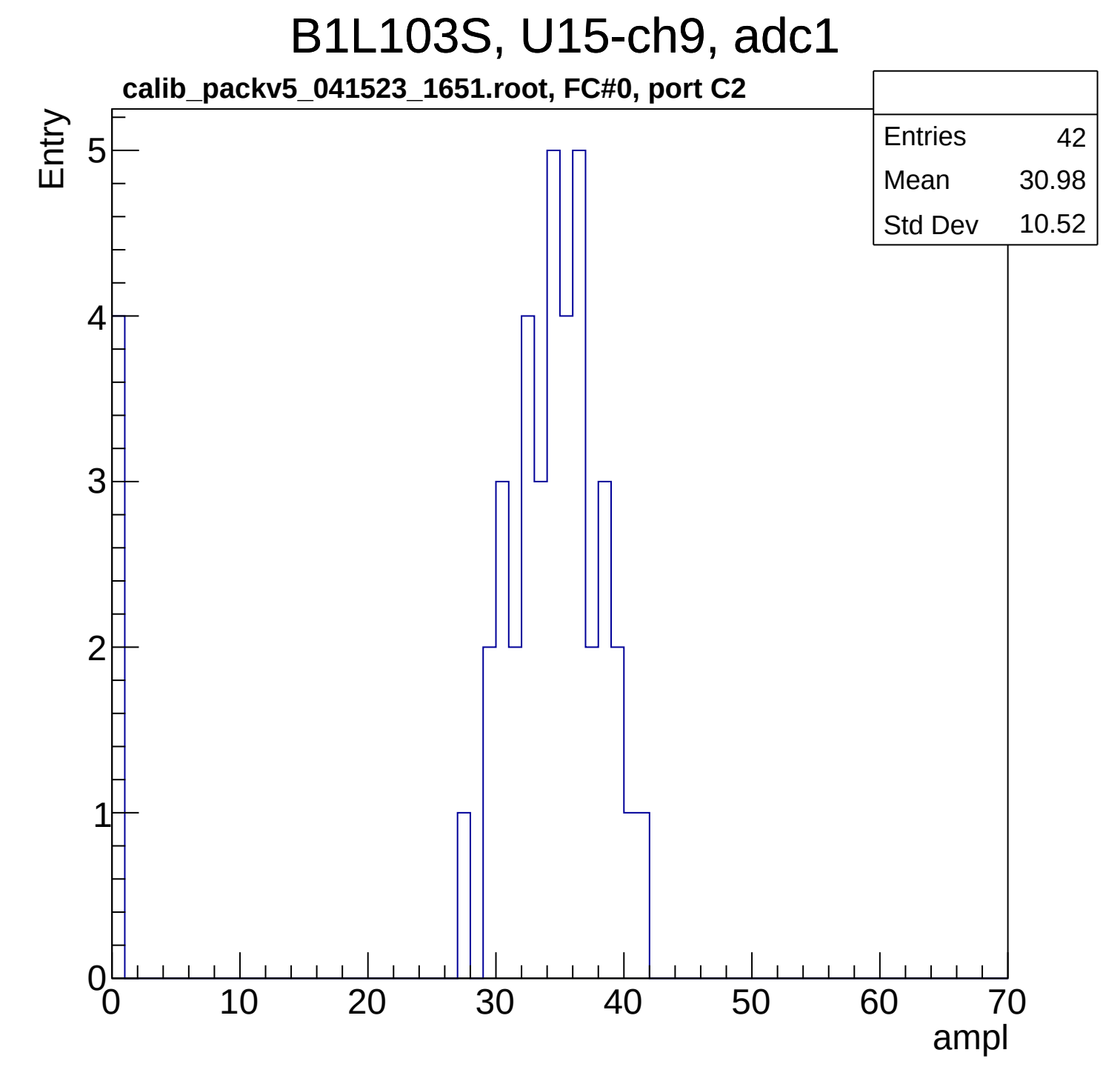

B1L103S, U15-ch8, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 53.55
Std Dev 3.251
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

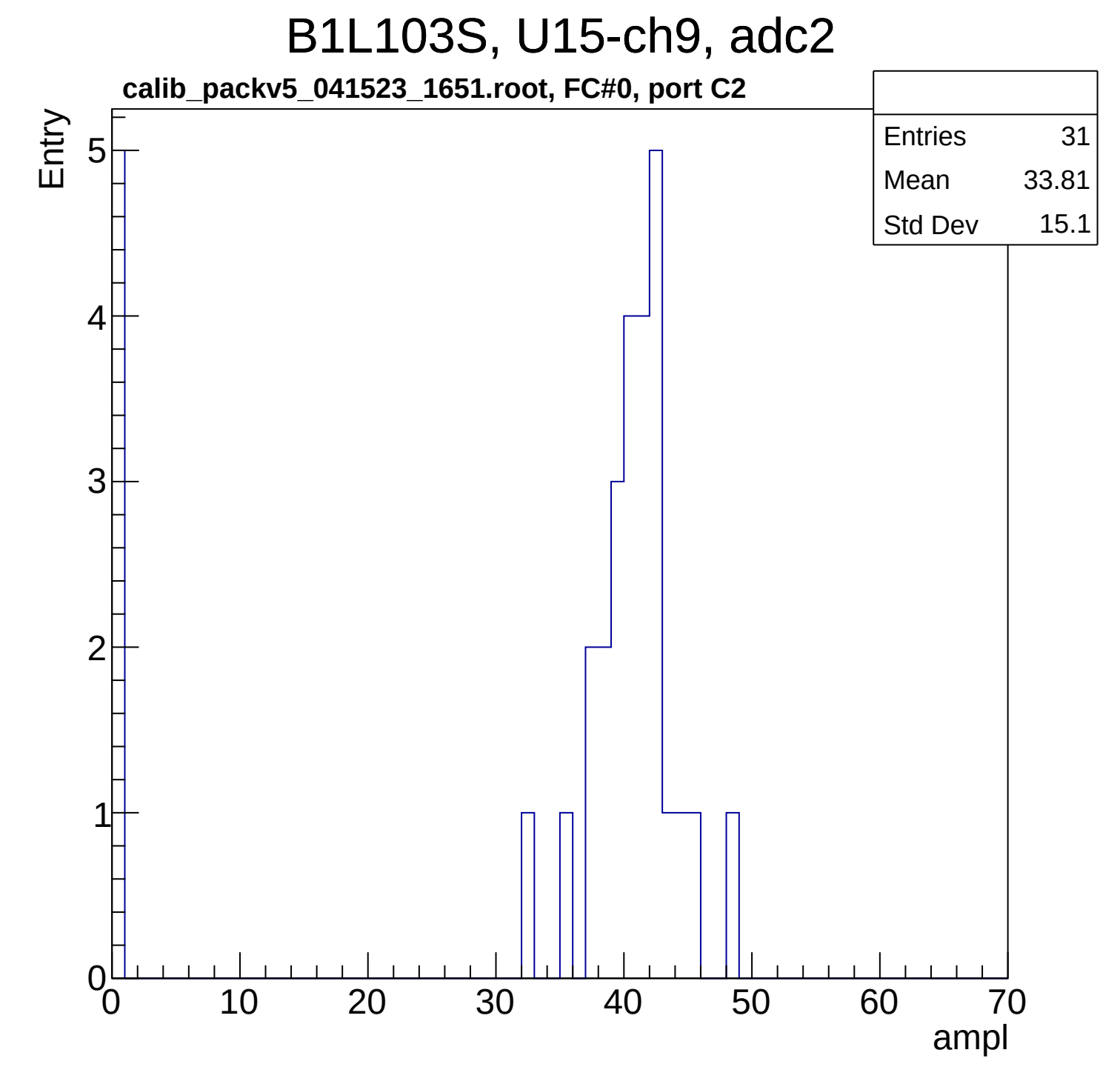

B1L103S, U15-ch8, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 59.04
Std Dev 3.35
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

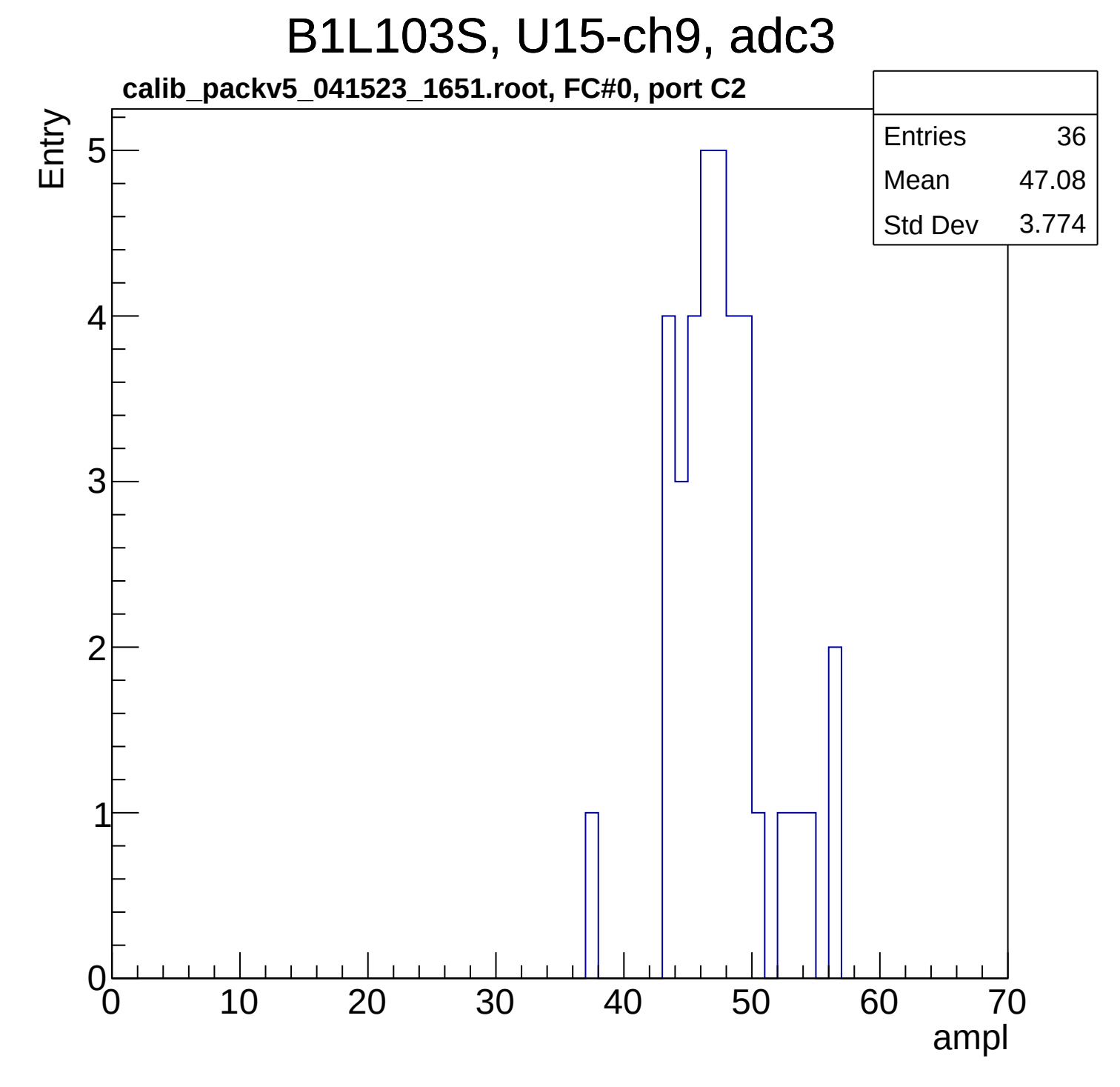

B1L103S, U15-ch8, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 60.25
Std Dev 2.487
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

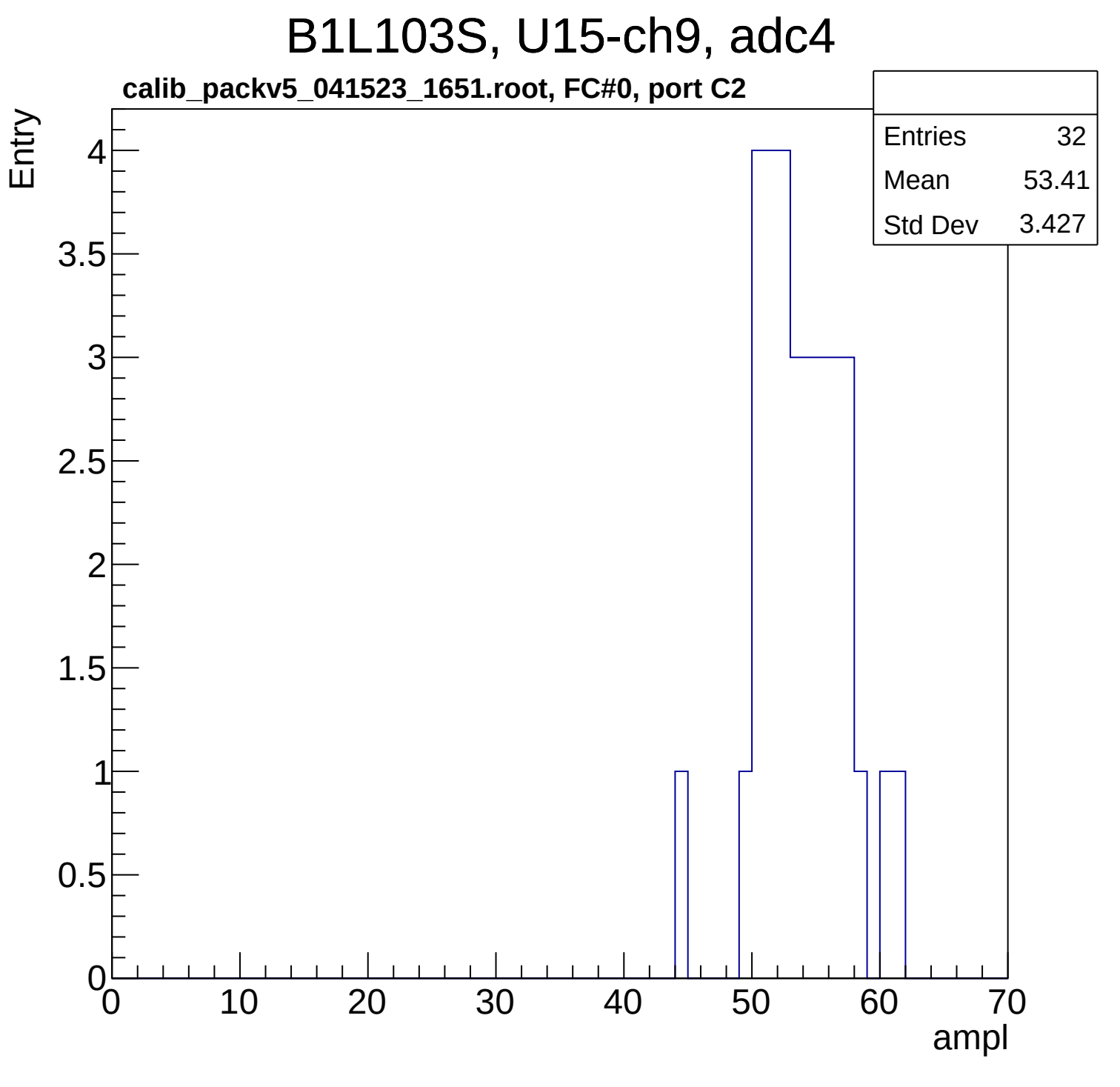

B1L103S, U15-ch8, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch9, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 18.17
Std Dev 13.36
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch9, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 30.98
Std Dev 10.52
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch9, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 33.81
Std Dev 15.1
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch9, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 47.08
Std Dev 3.774
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch9, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 53.41
Std Dev 3.427
Entry
ampl
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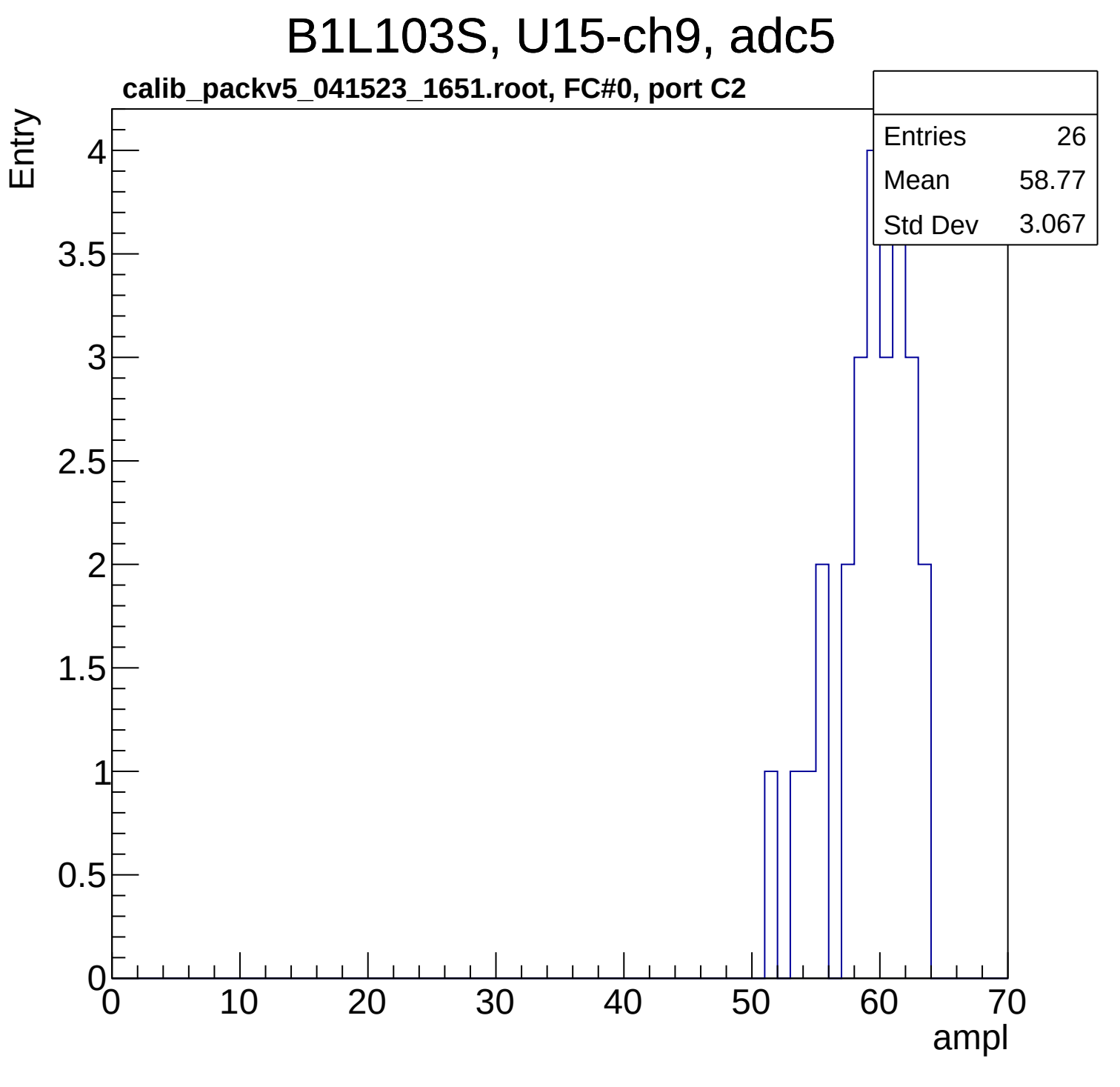
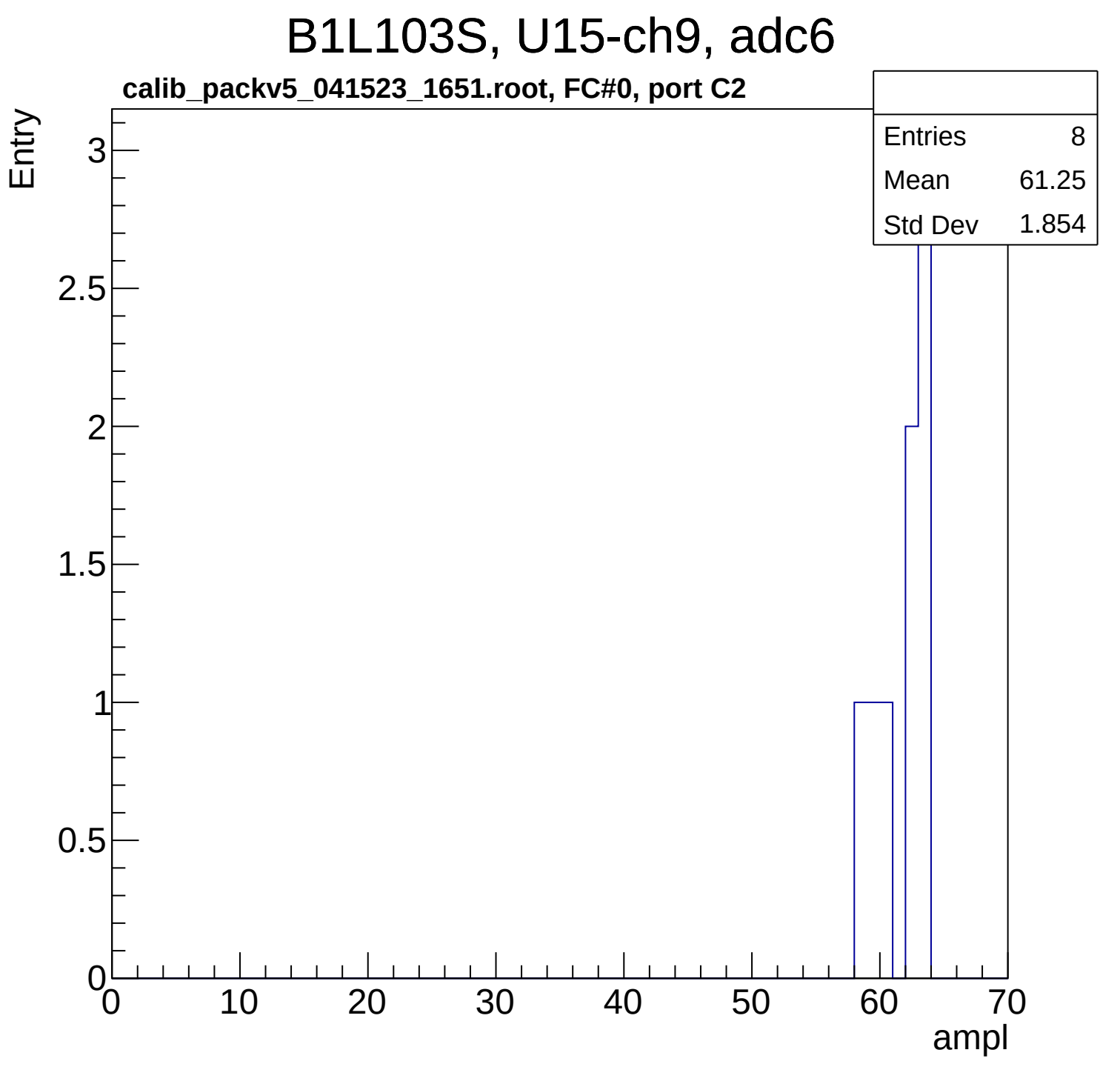
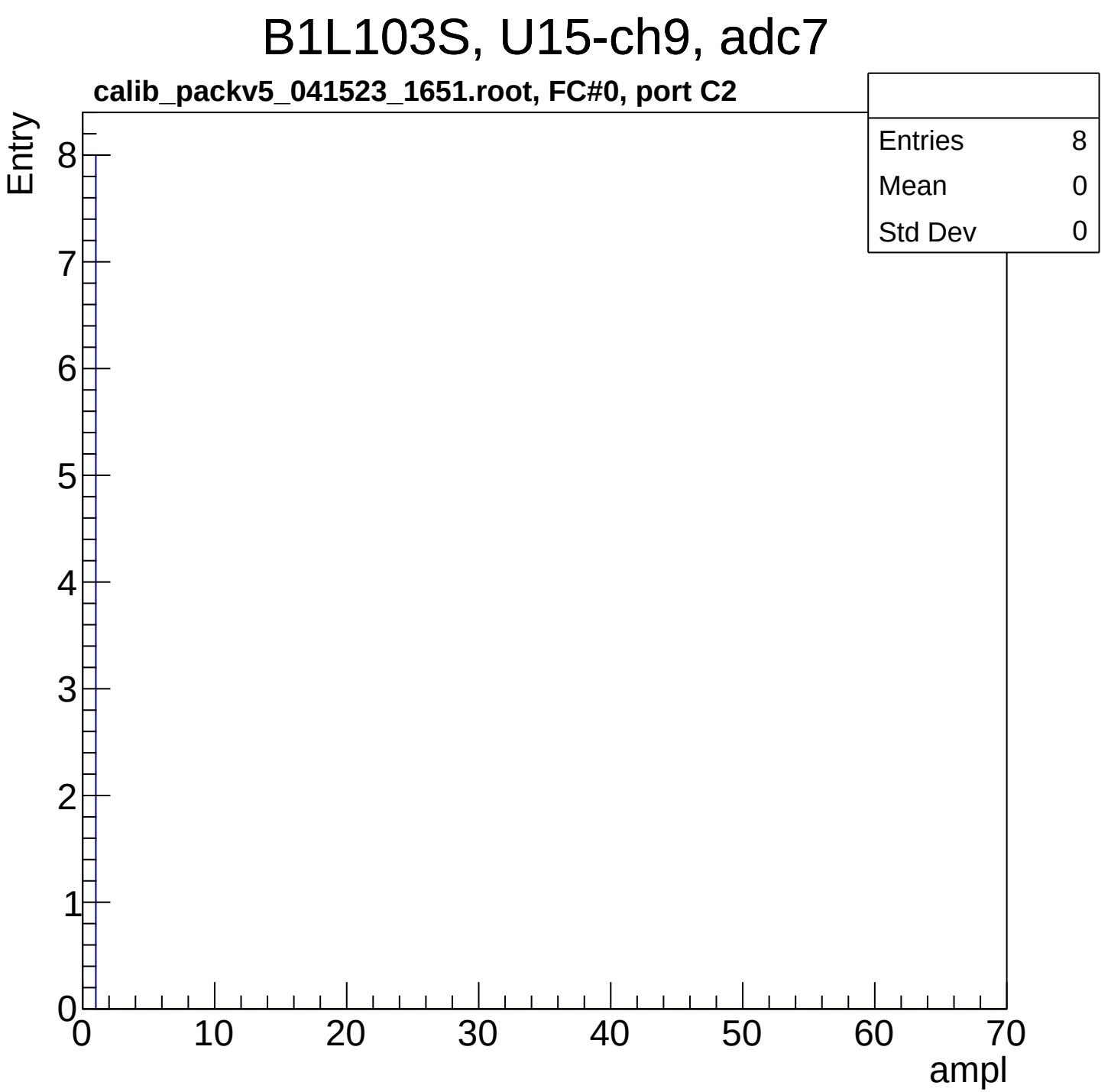
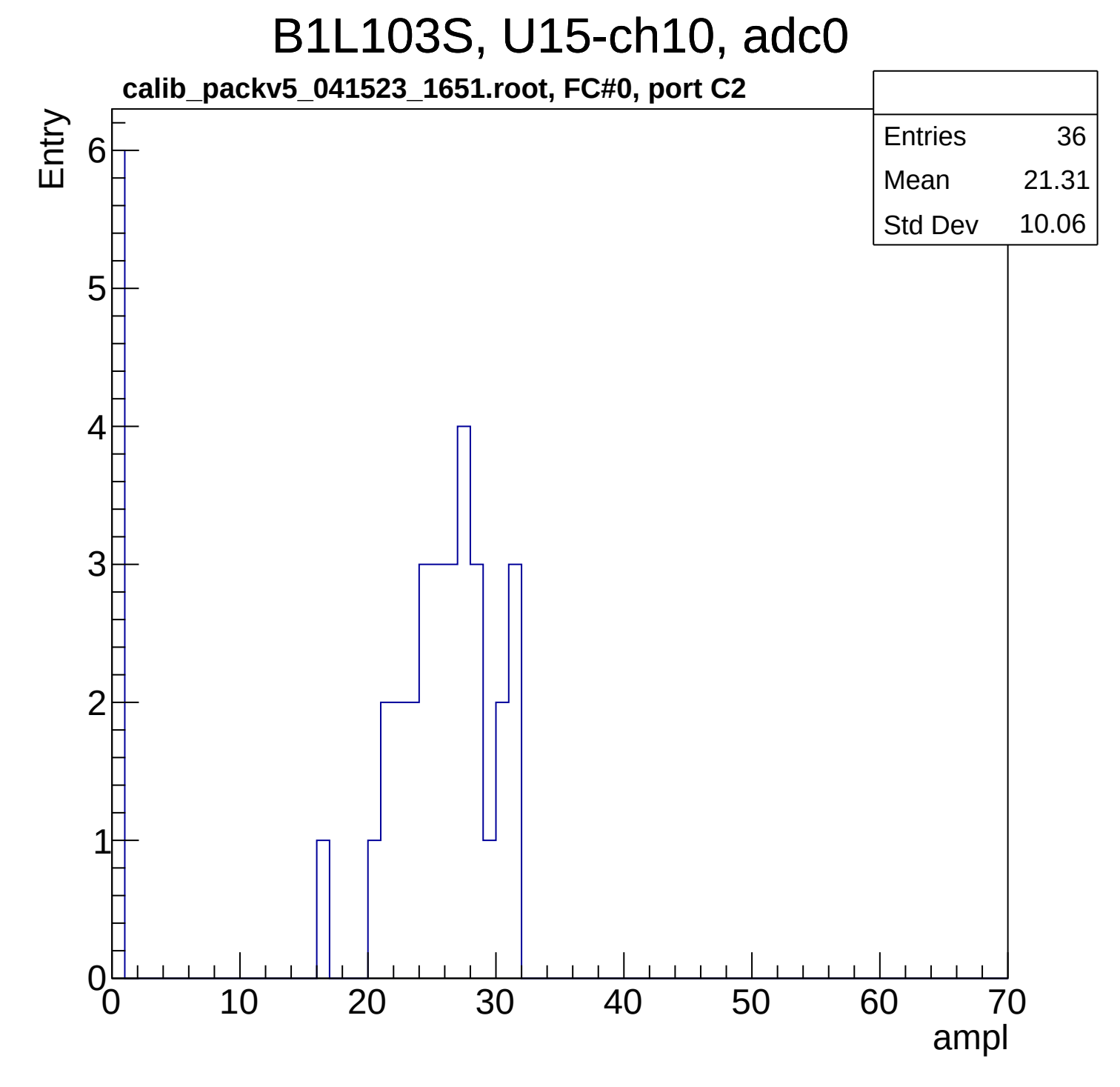
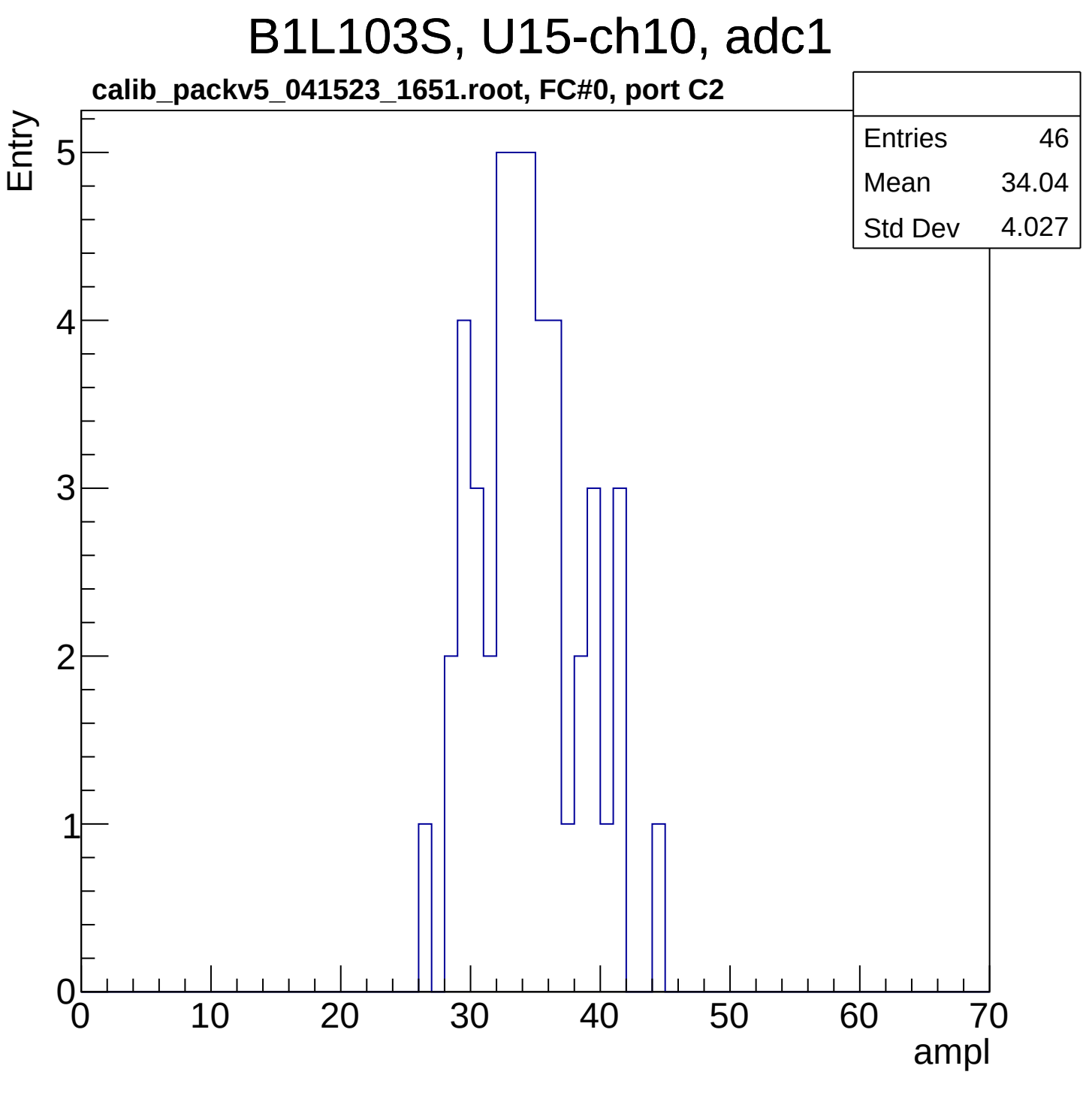
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

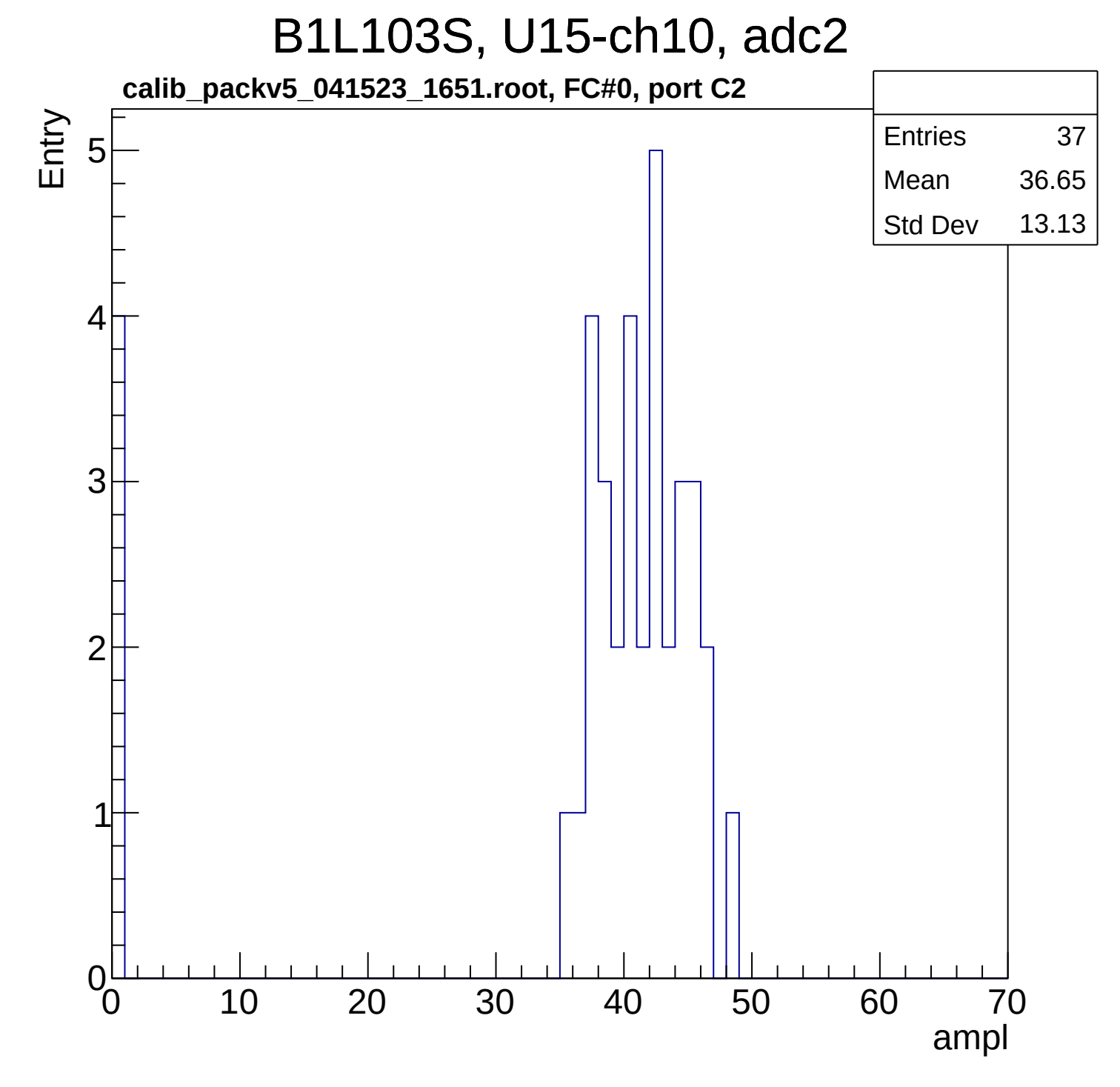

B1L103S, U15-ch9, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 58.77
Std Dev 3.067
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

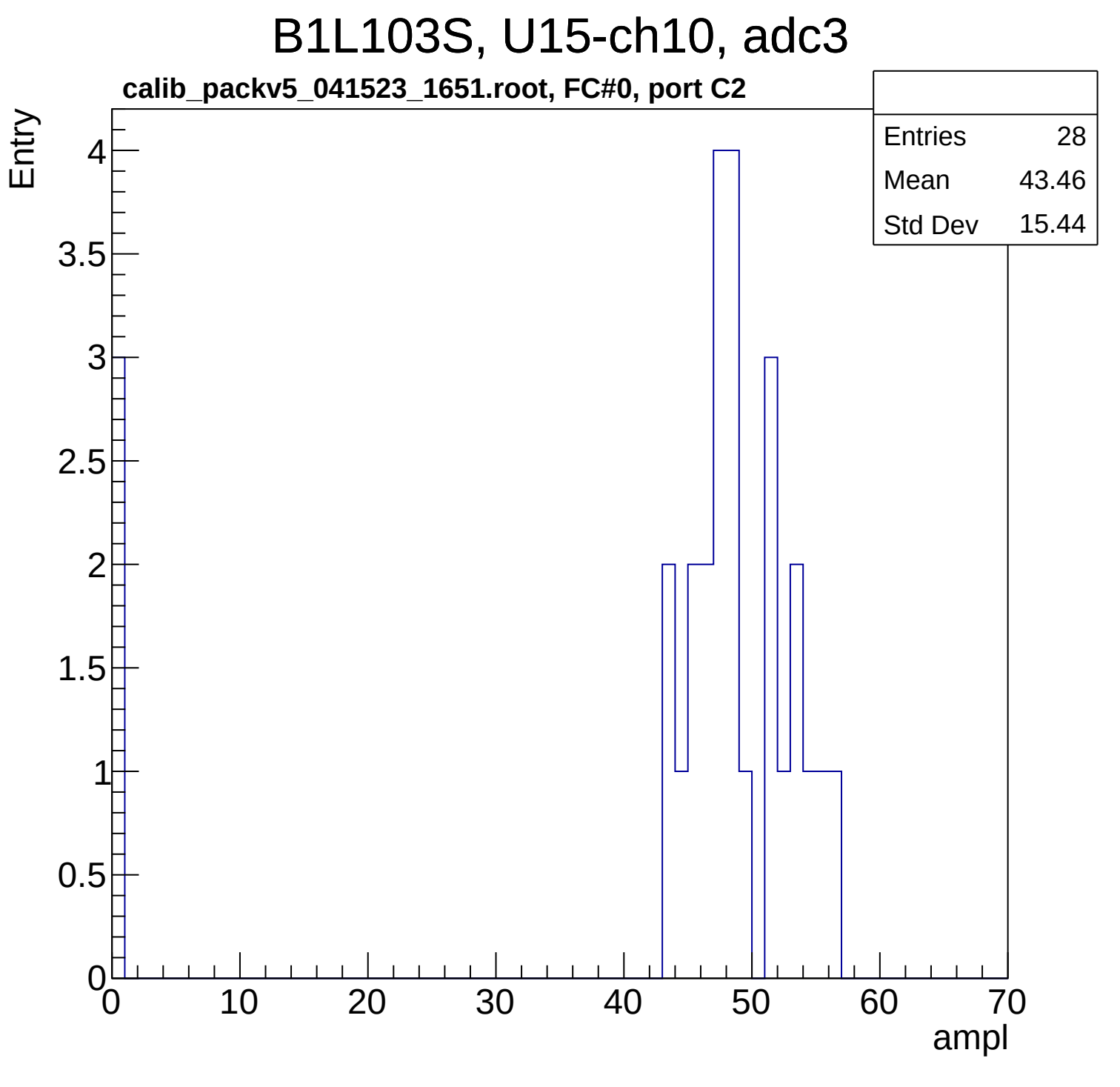

B1L103S, U15-ch9, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.25
Std Dev 1.854
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

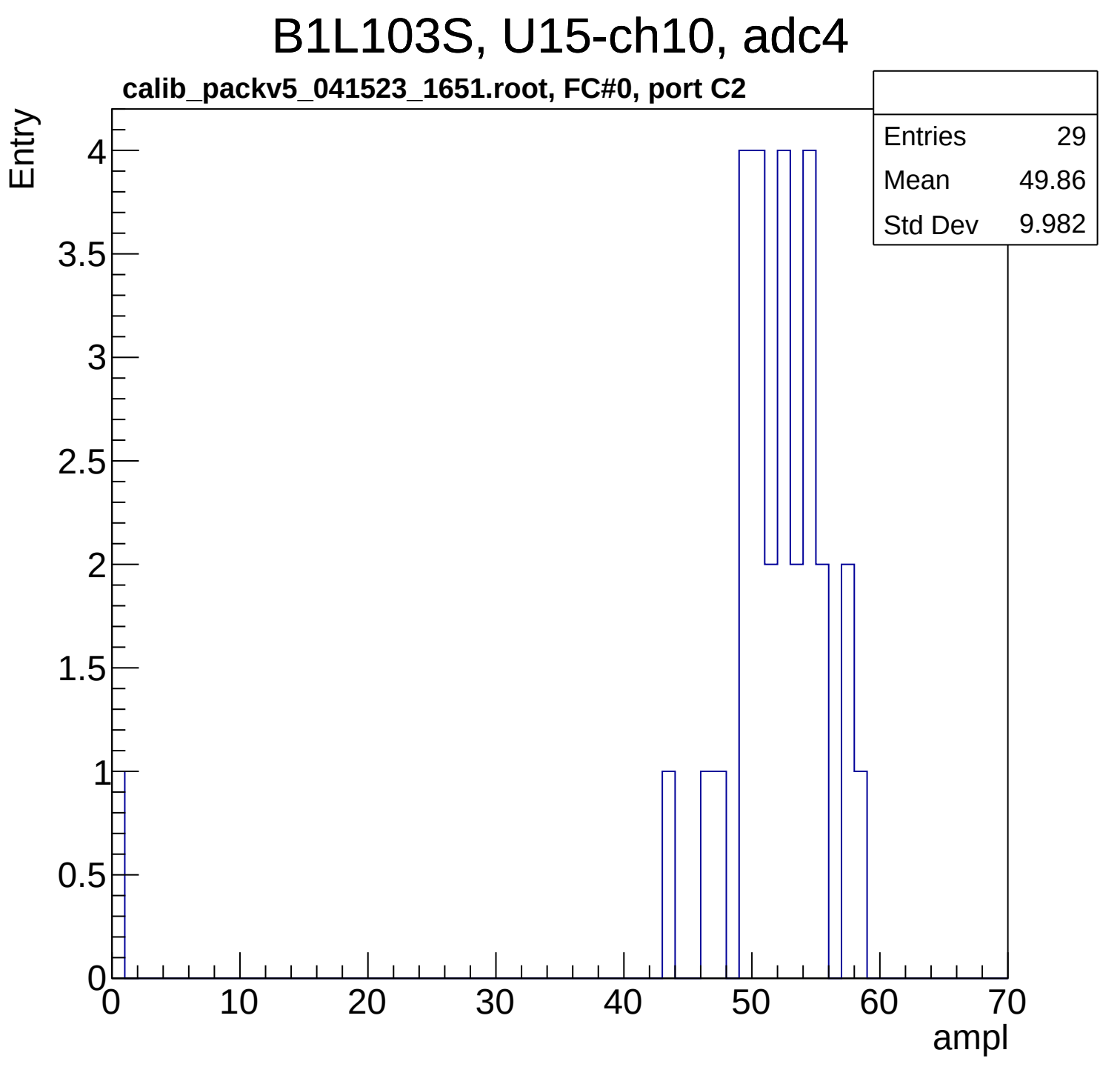

B1L103S, U15-ch9, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 0
Std Dev 0
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch10, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 21.31
Std Dev 10.06
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U15-ch10, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 34.04
Std Dev 4.027
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch10, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 36.65
Std Dev 13.13
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch10, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 43.46
Std Dev 15.44
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch10, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 49.86
Std Dev 9.982
Entry
ampl
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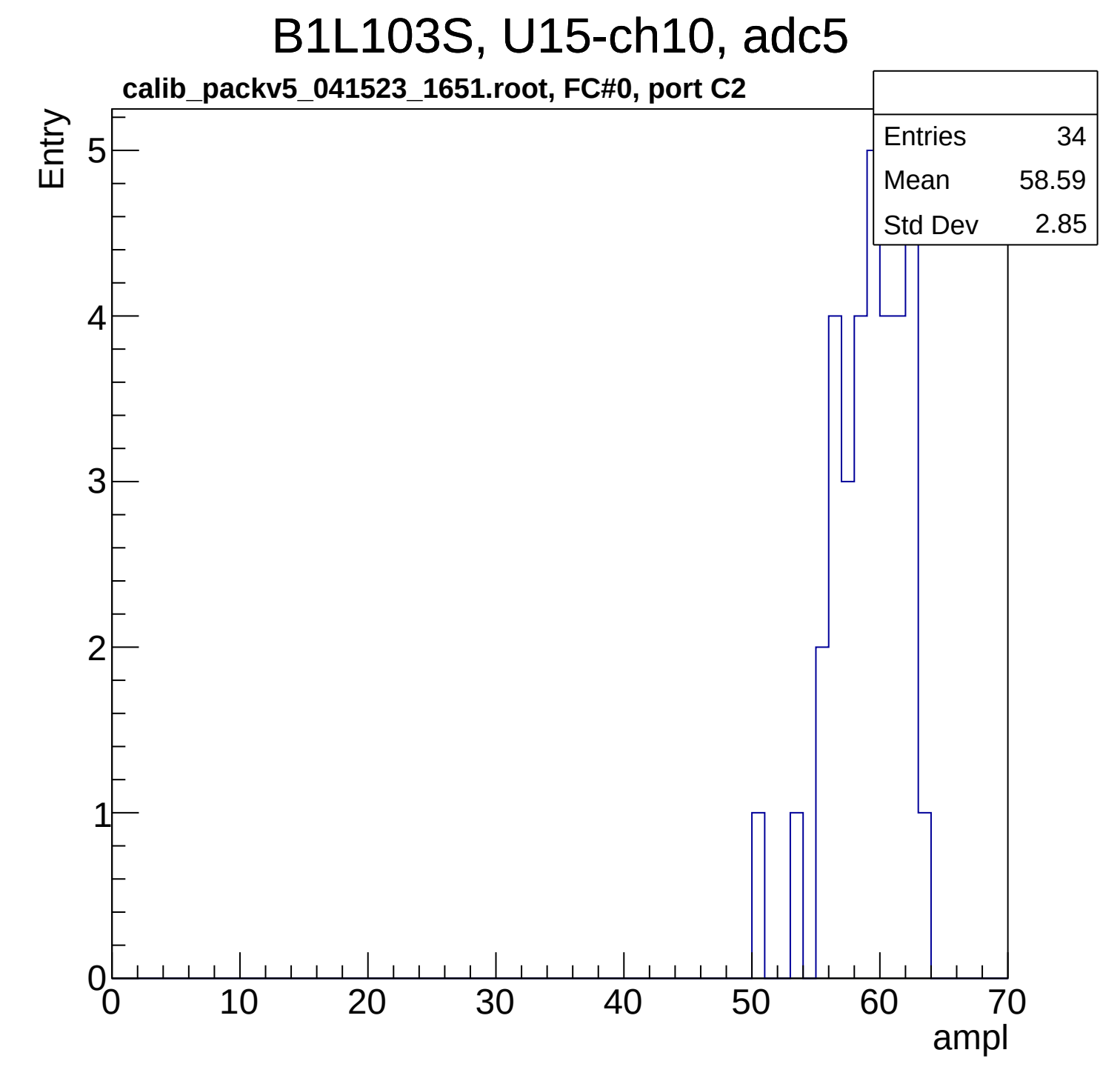
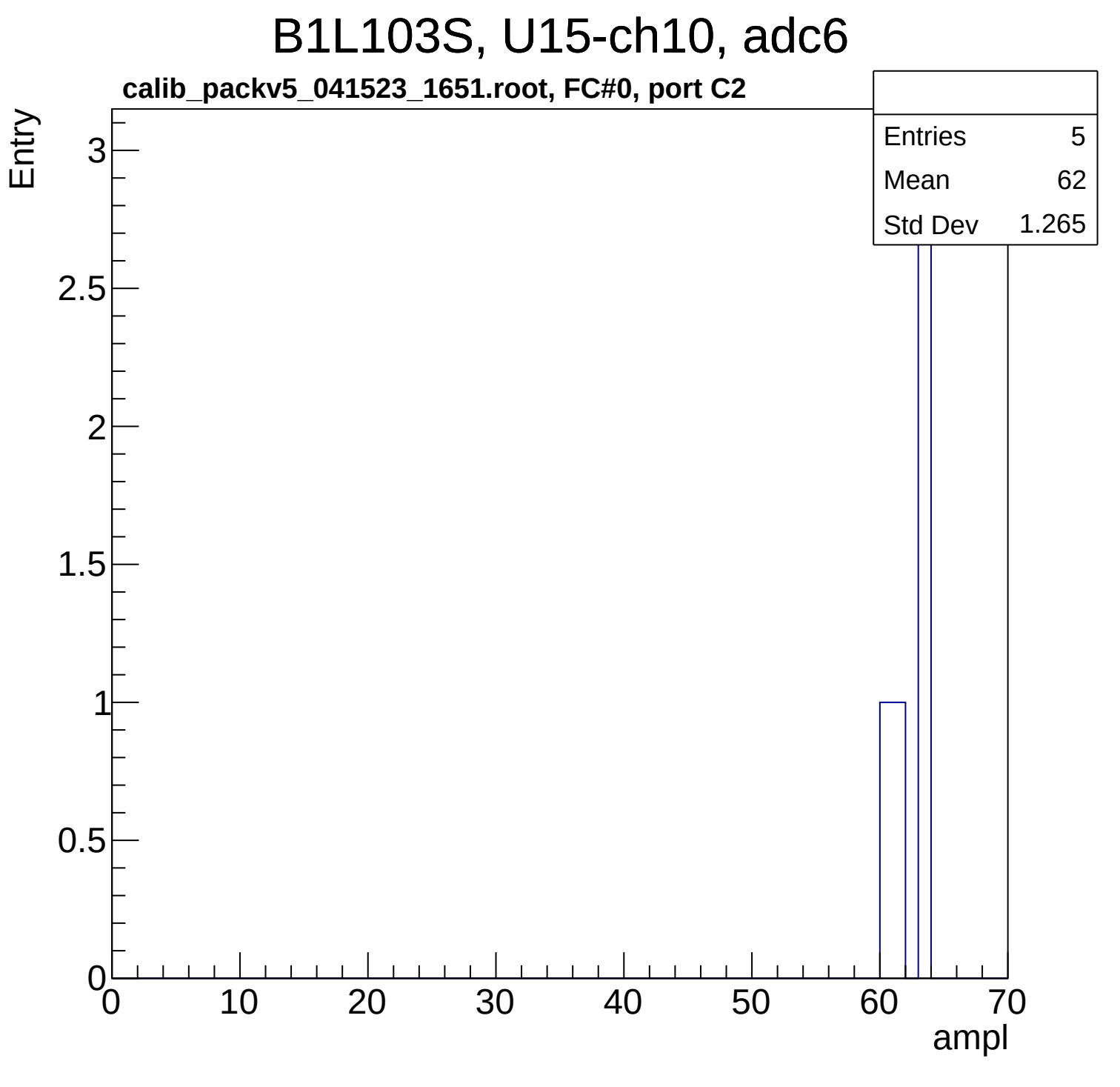
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch10, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 58.59
Std Dev 2.85
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch10, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62
Std Dev 1.265
Entry
ampl
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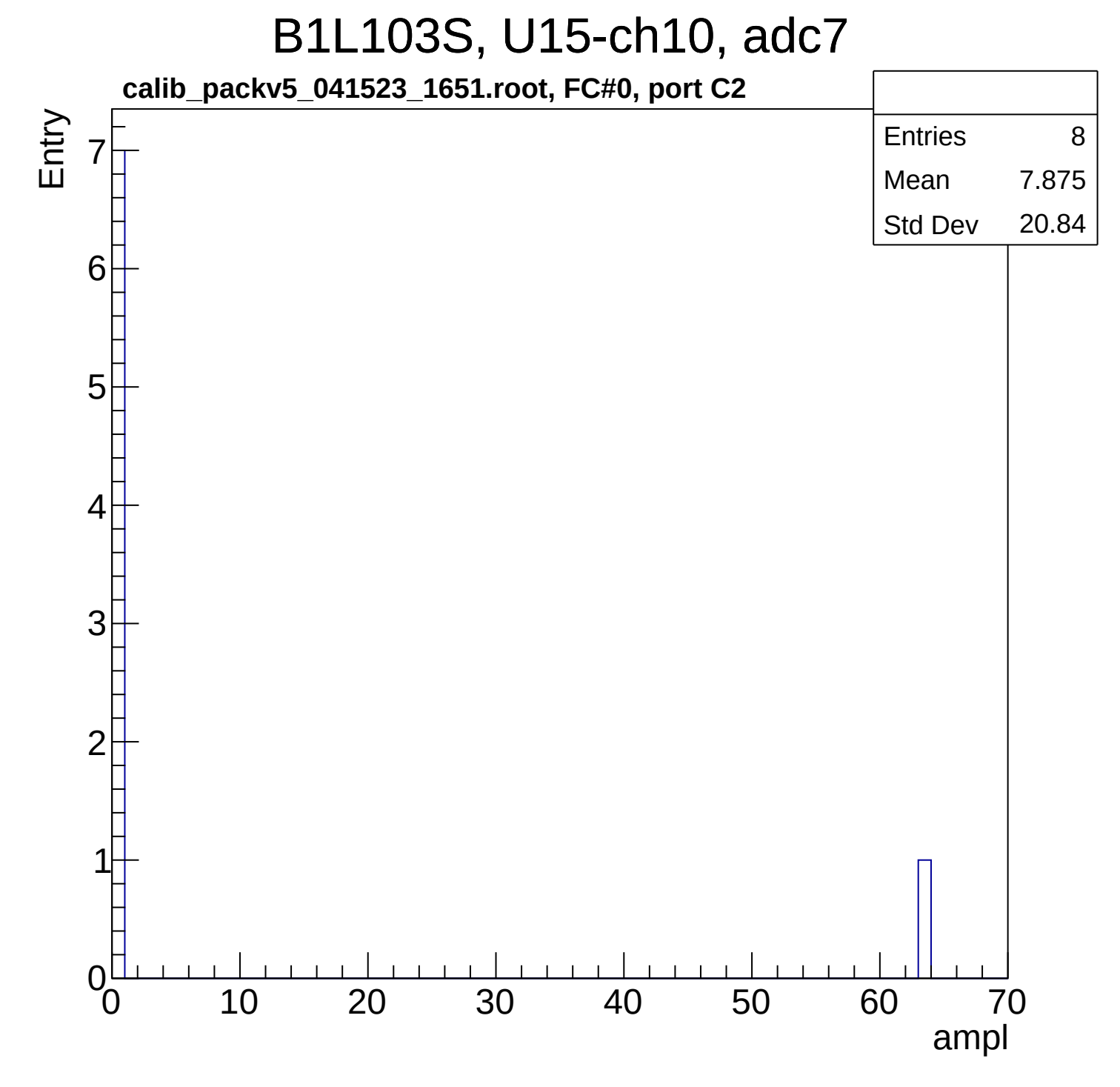
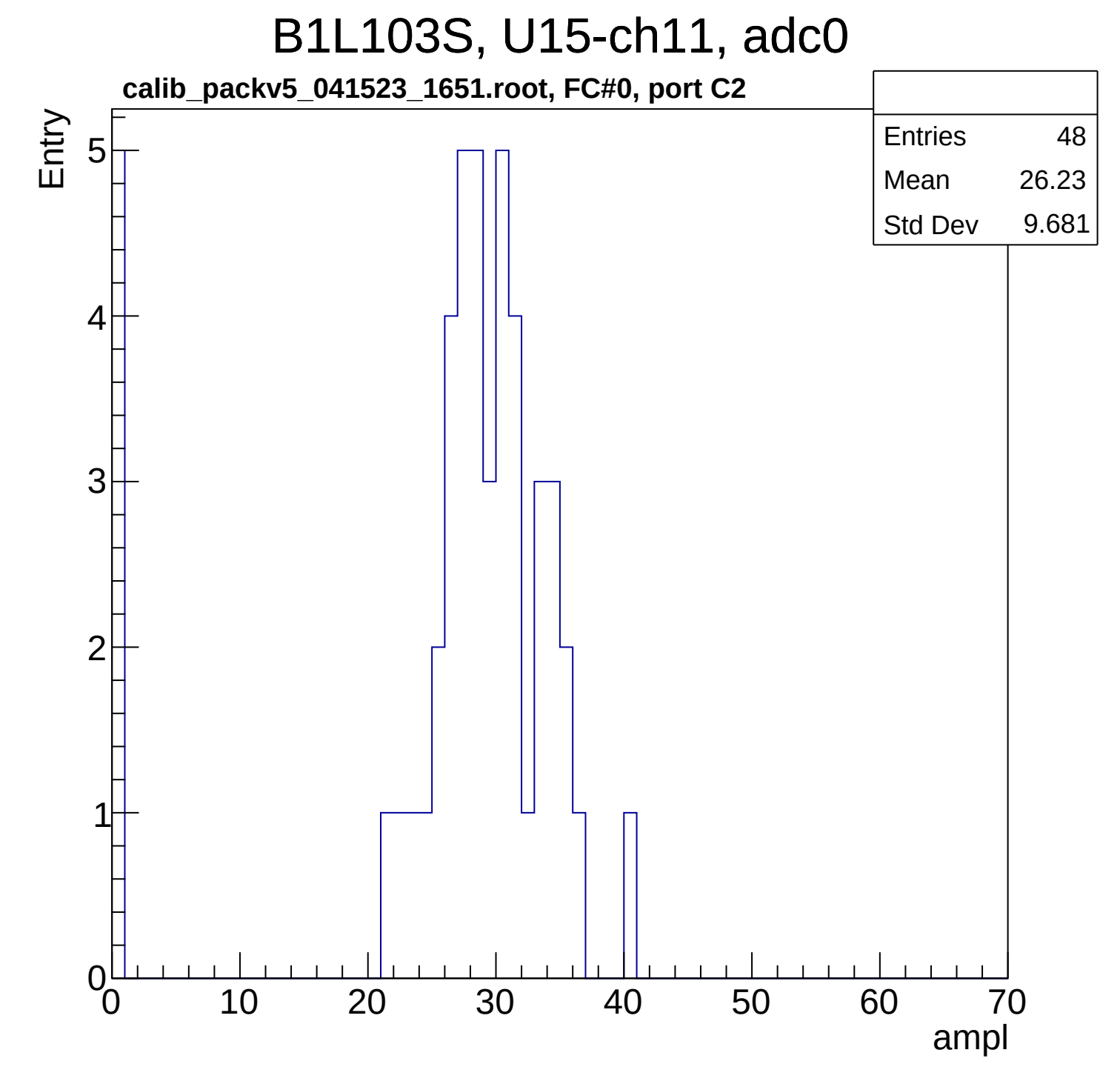
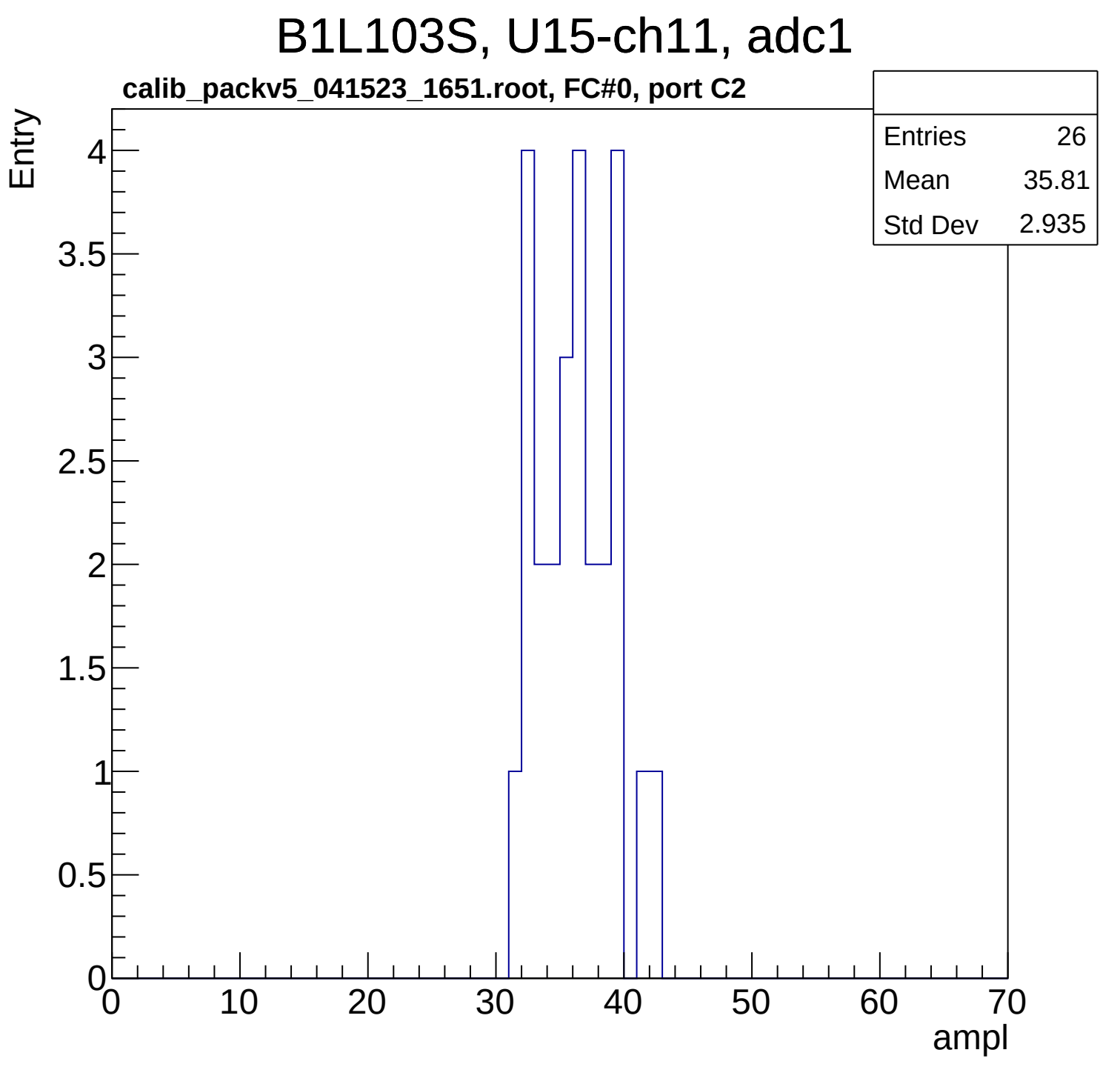
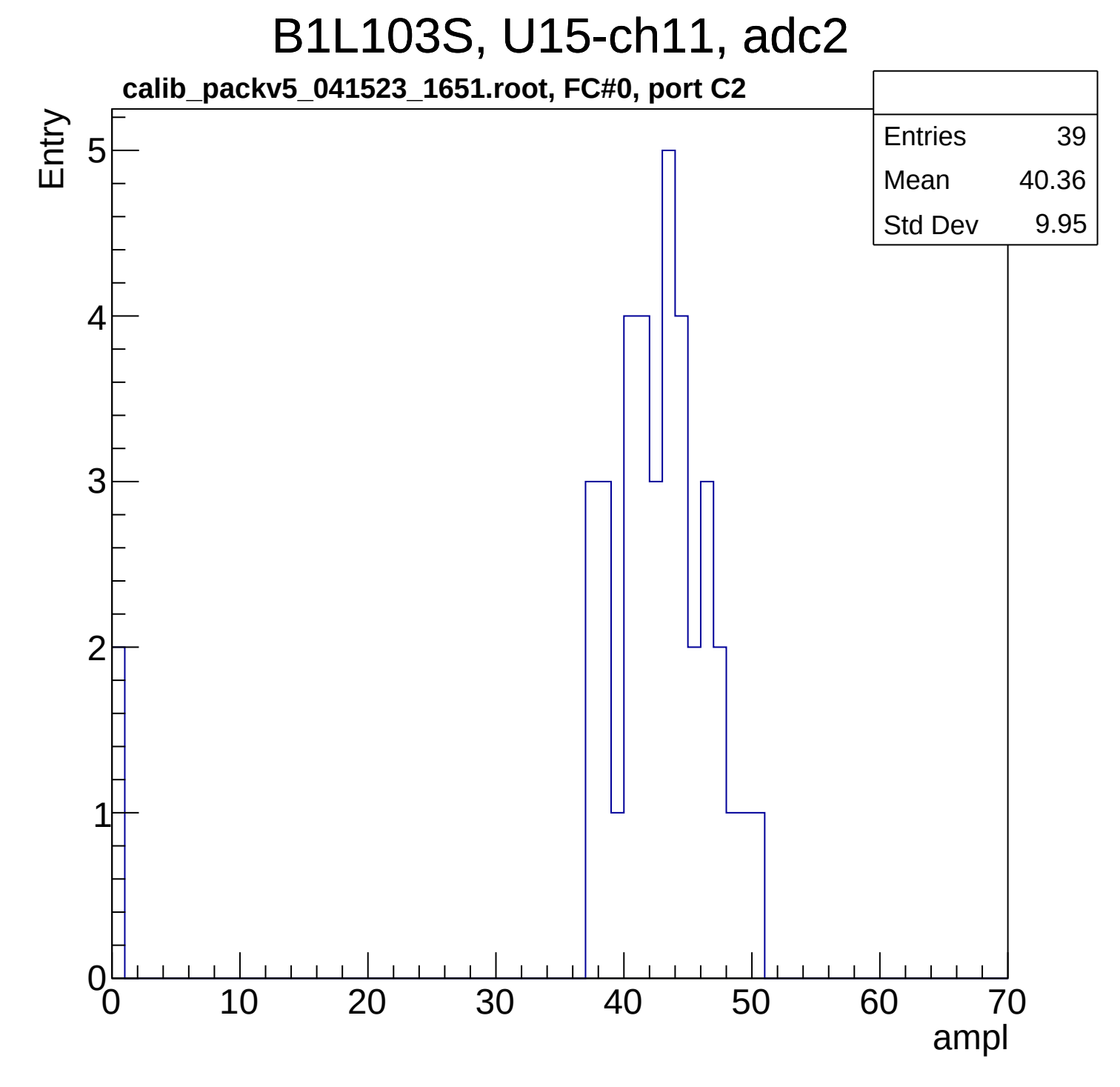
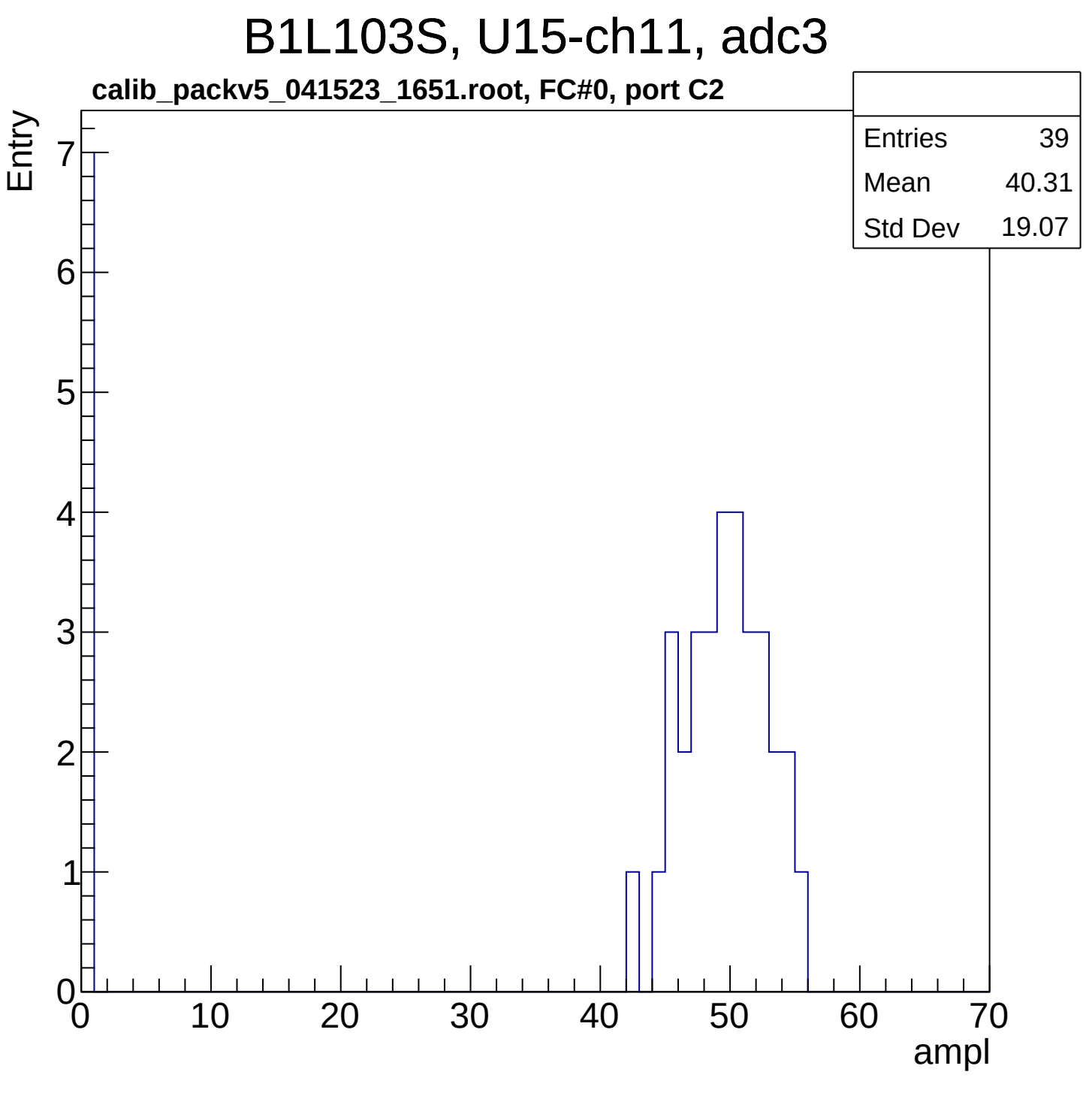
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

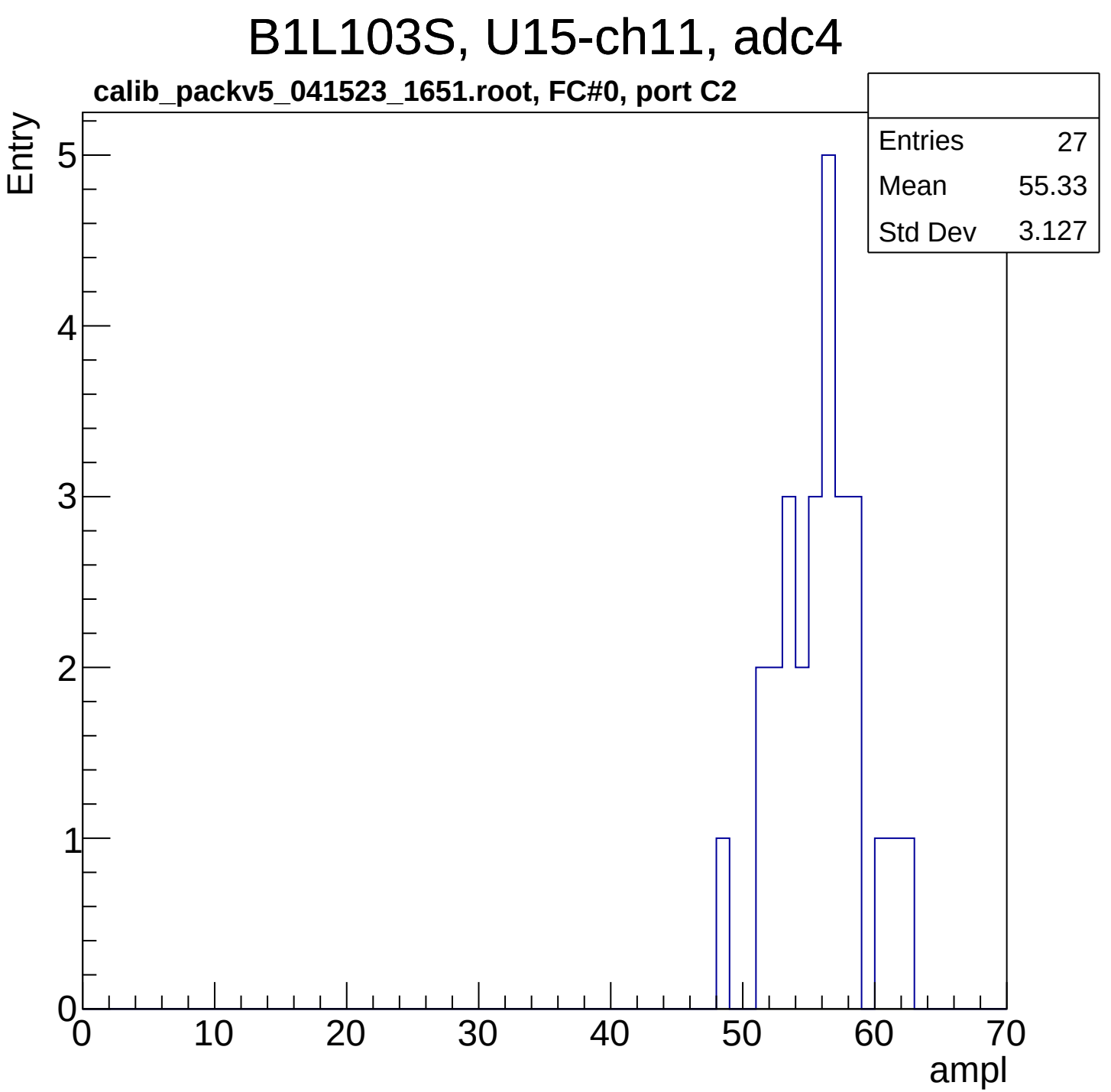

B1L103S, U15-ch10, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 7.875
Std Dev 20.84
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

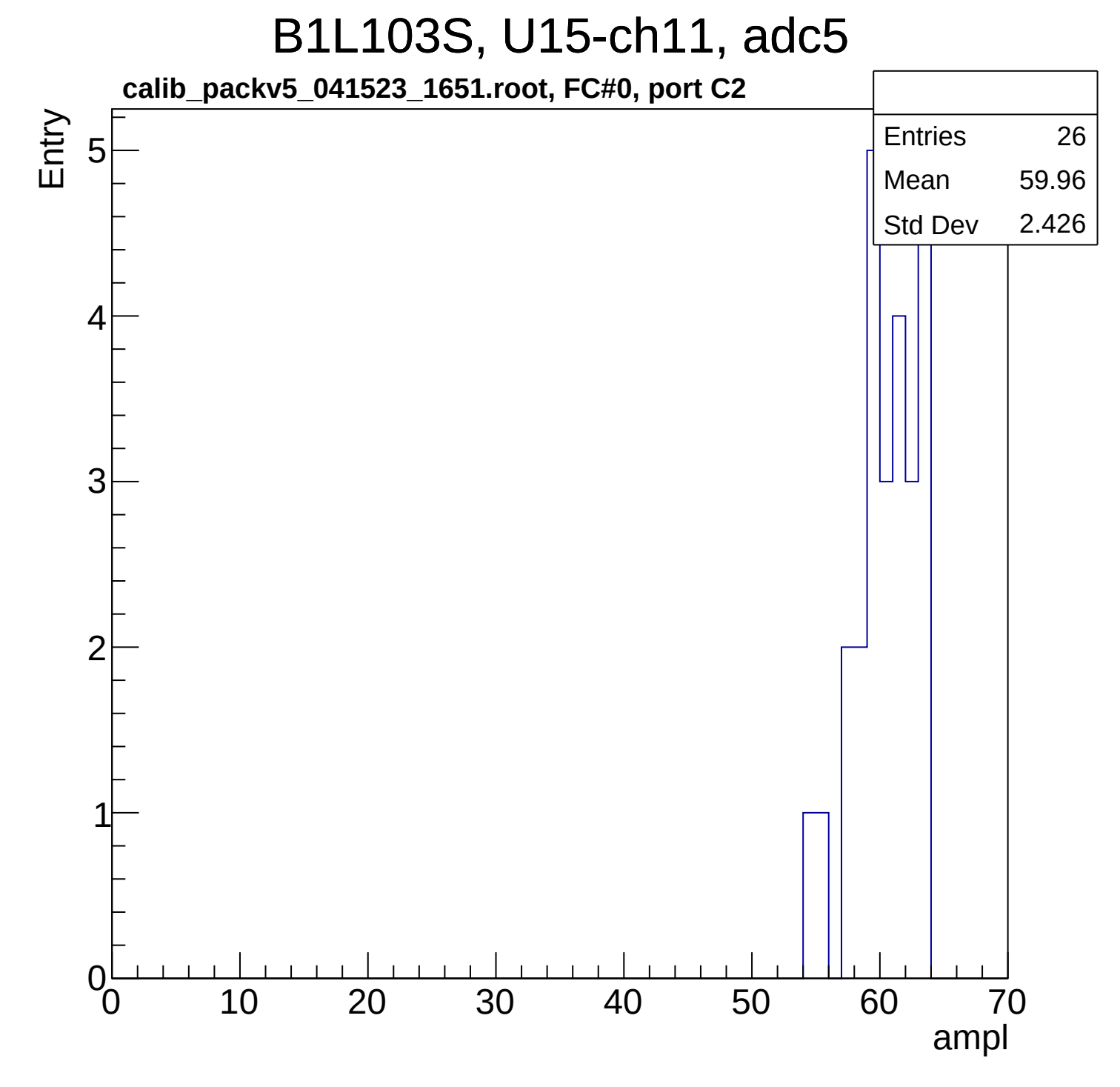

B1L103S, U15-ch11, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 26.23
Std Dev 9.681
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

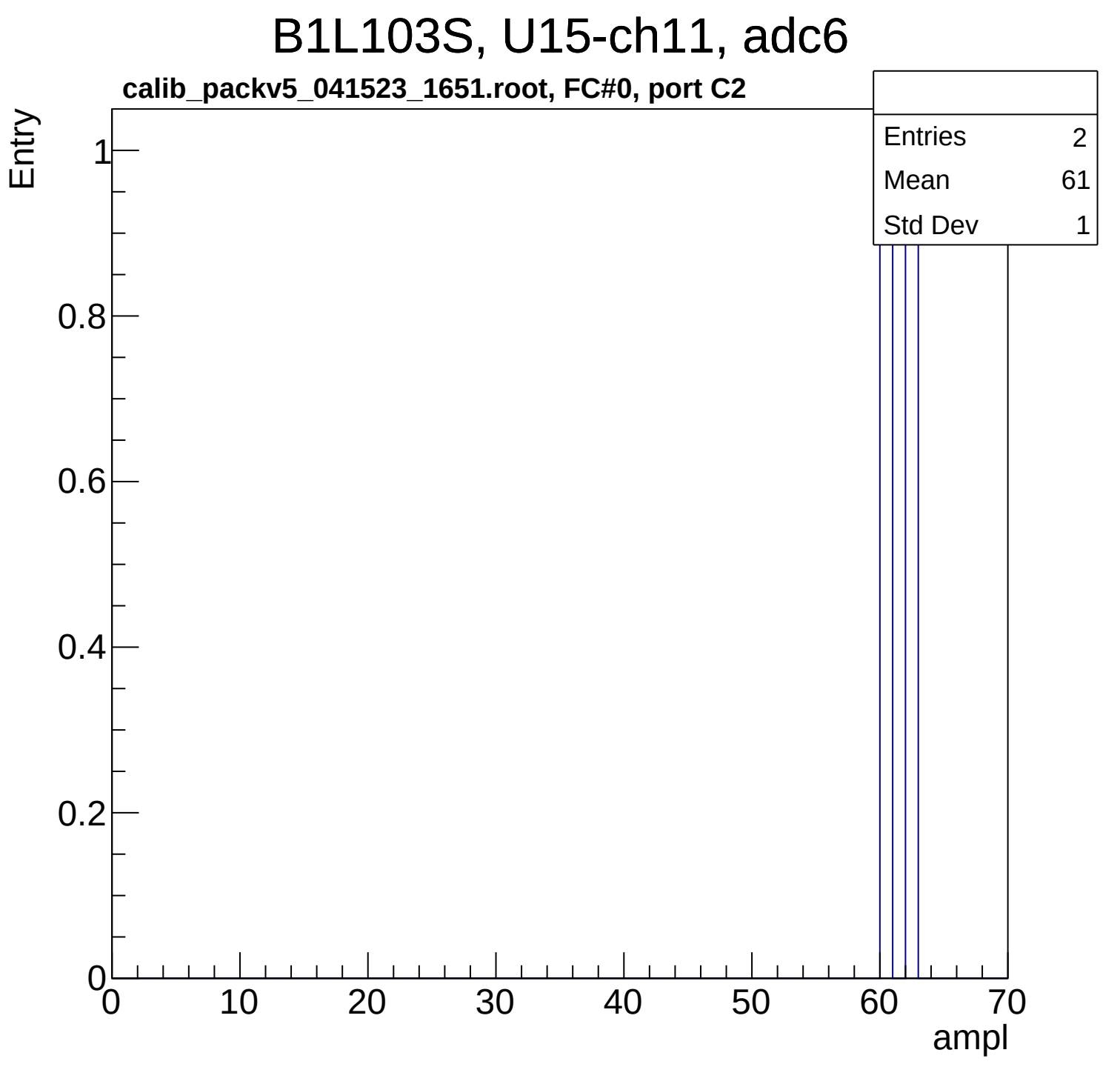

B1L103S, U15-ch11, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 35.81
Std Dev 2.935
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

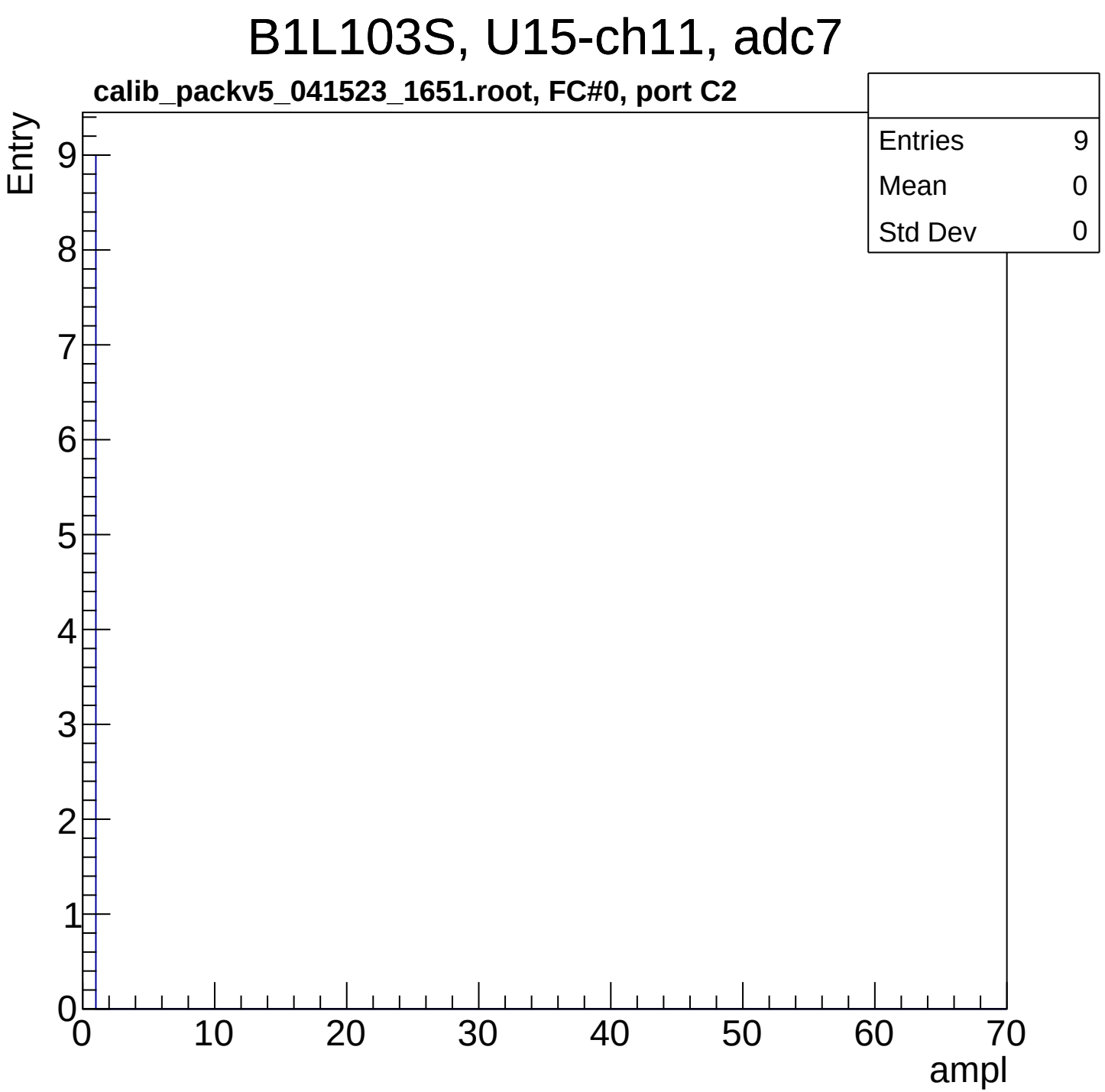

B1L103S, U15-ch11, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 40.36
Std Dev 9.95
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

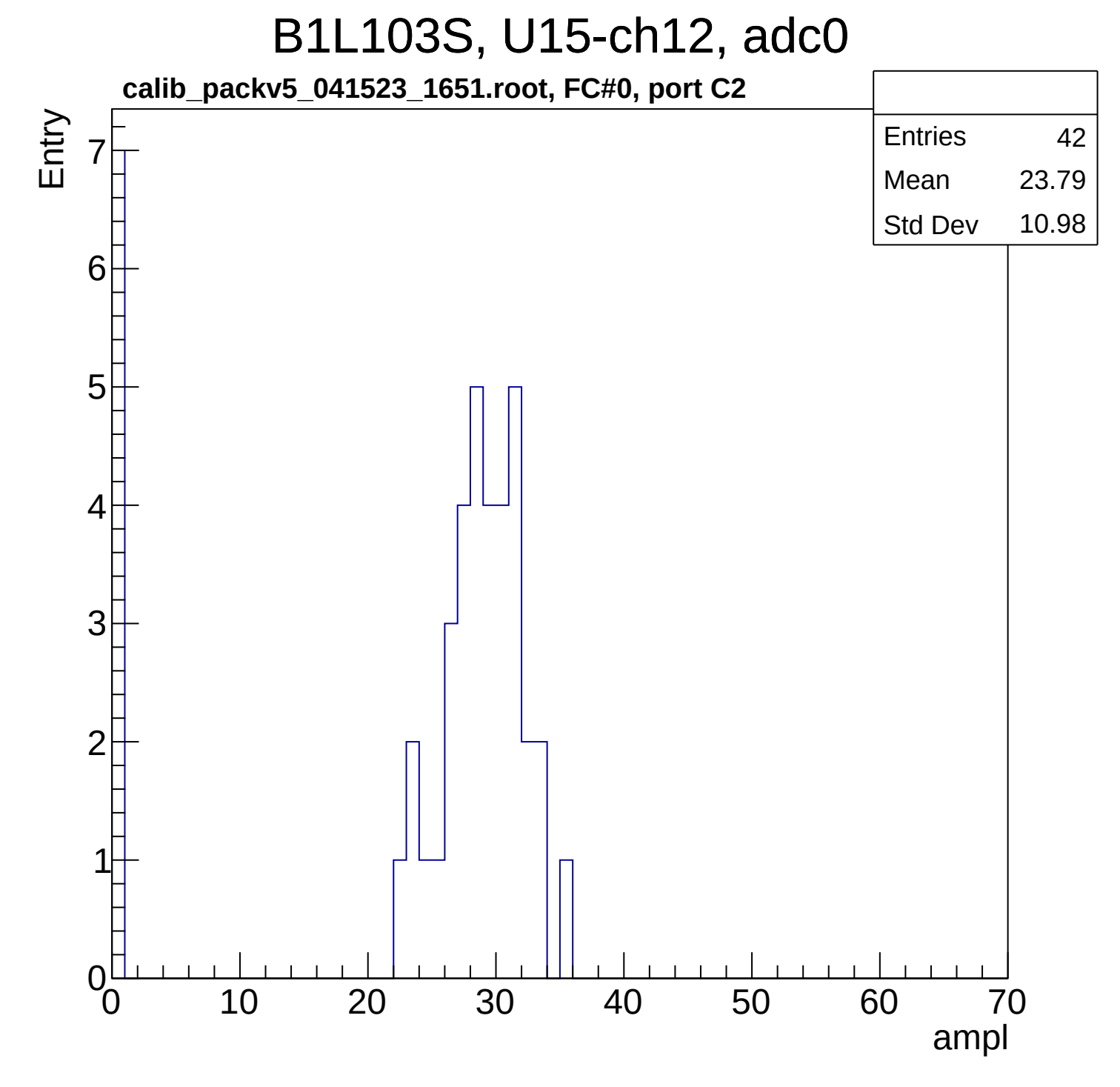

B1L103S, U15-ch11, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 40.31
Std Dev 19.07
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

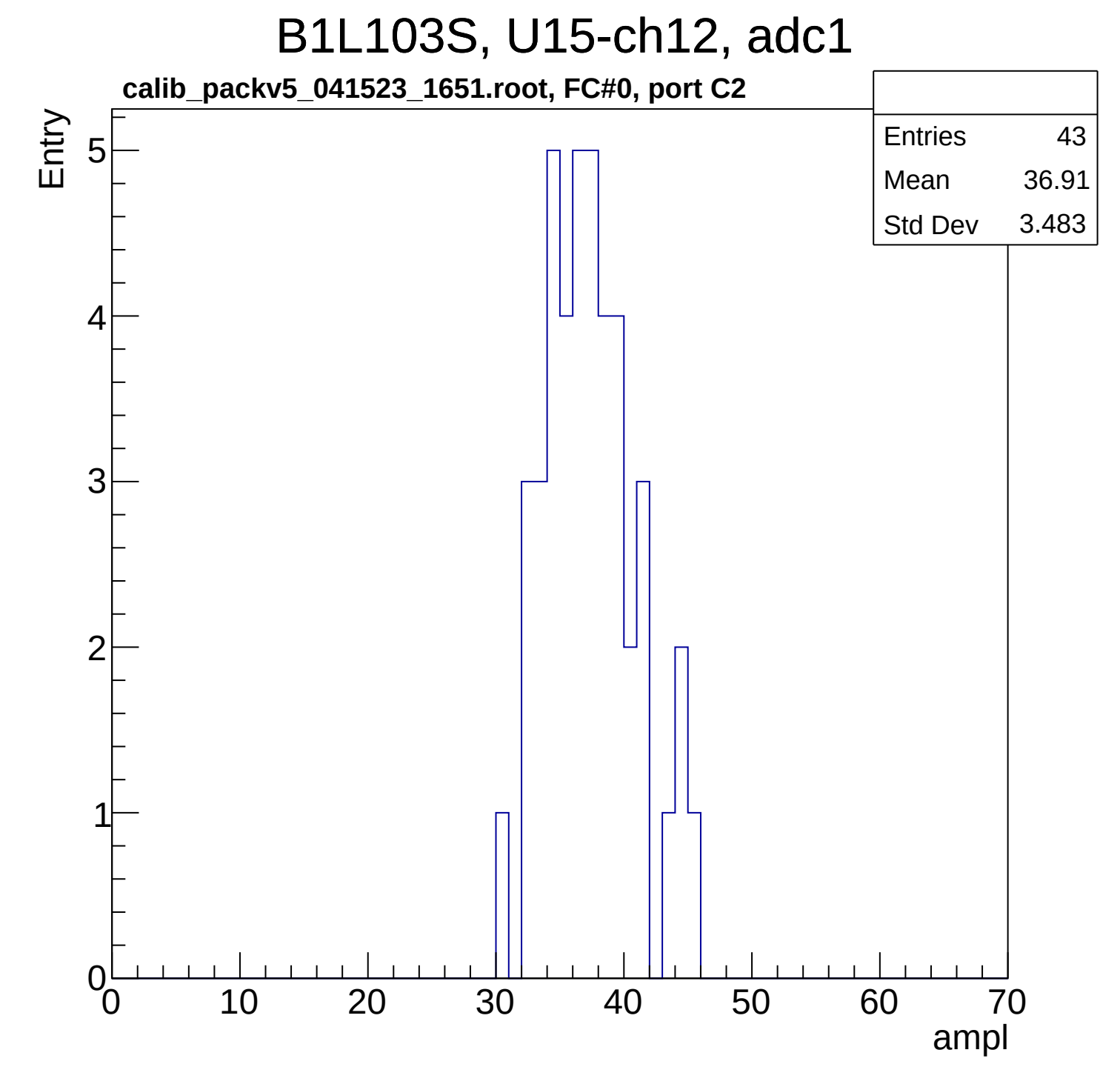

B1L103S, U15-ch11, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 55.33
Std Dev 3.127
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

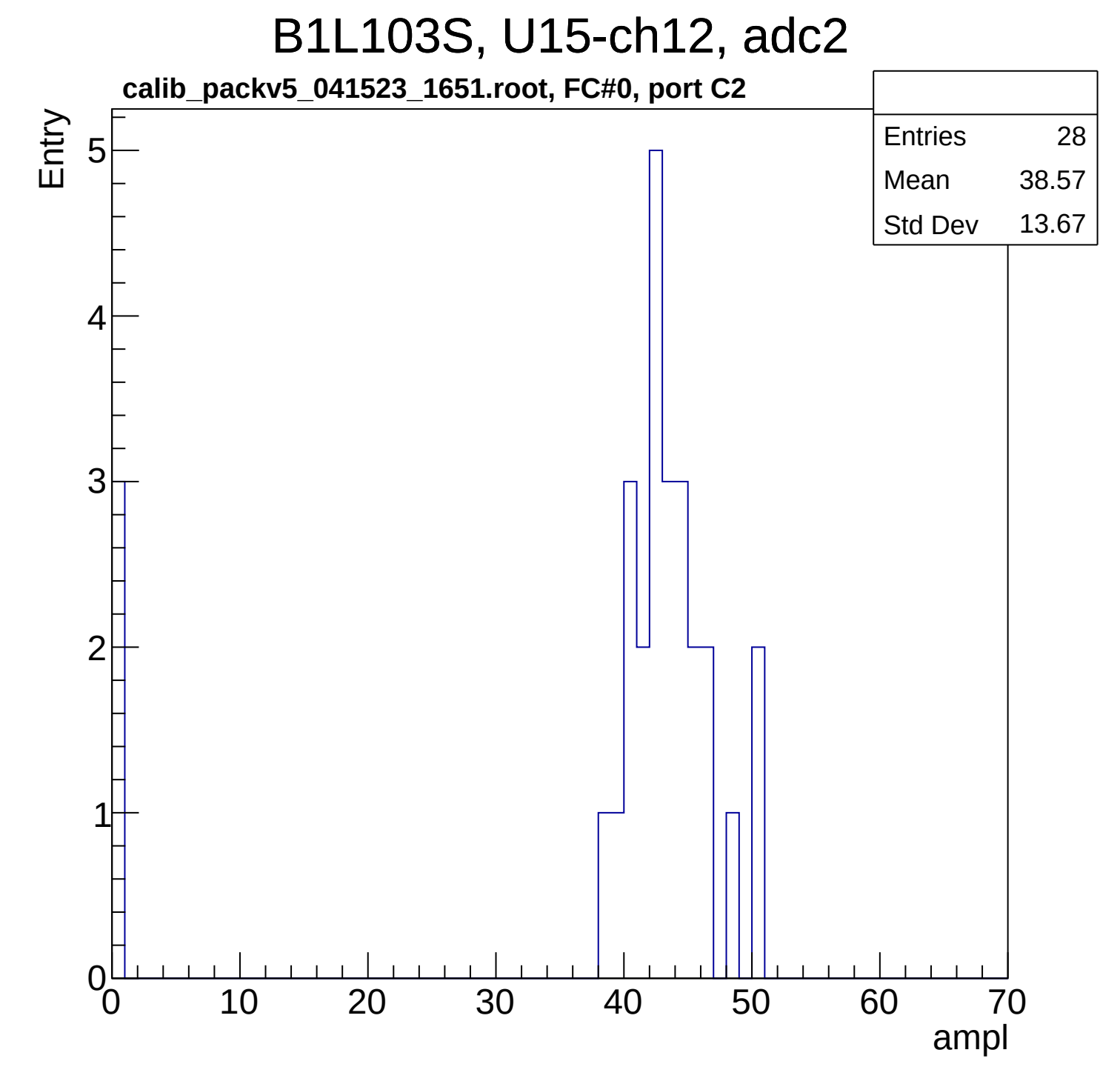

B1L103S, U15-ch11, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 59.96
Std Dev 2.426
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

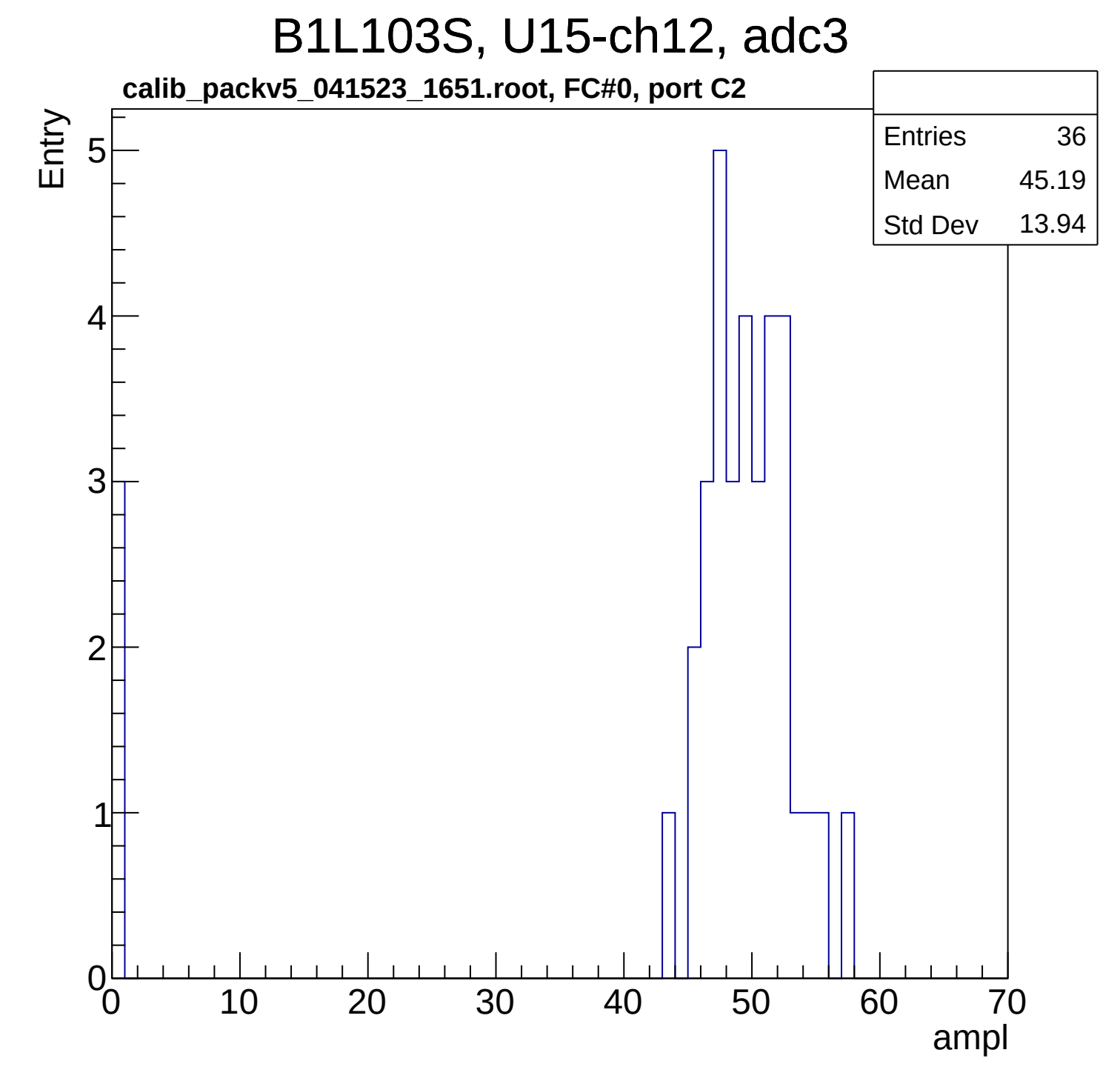

B1L103S, U15-ch11, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 61
Std Dev 1
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

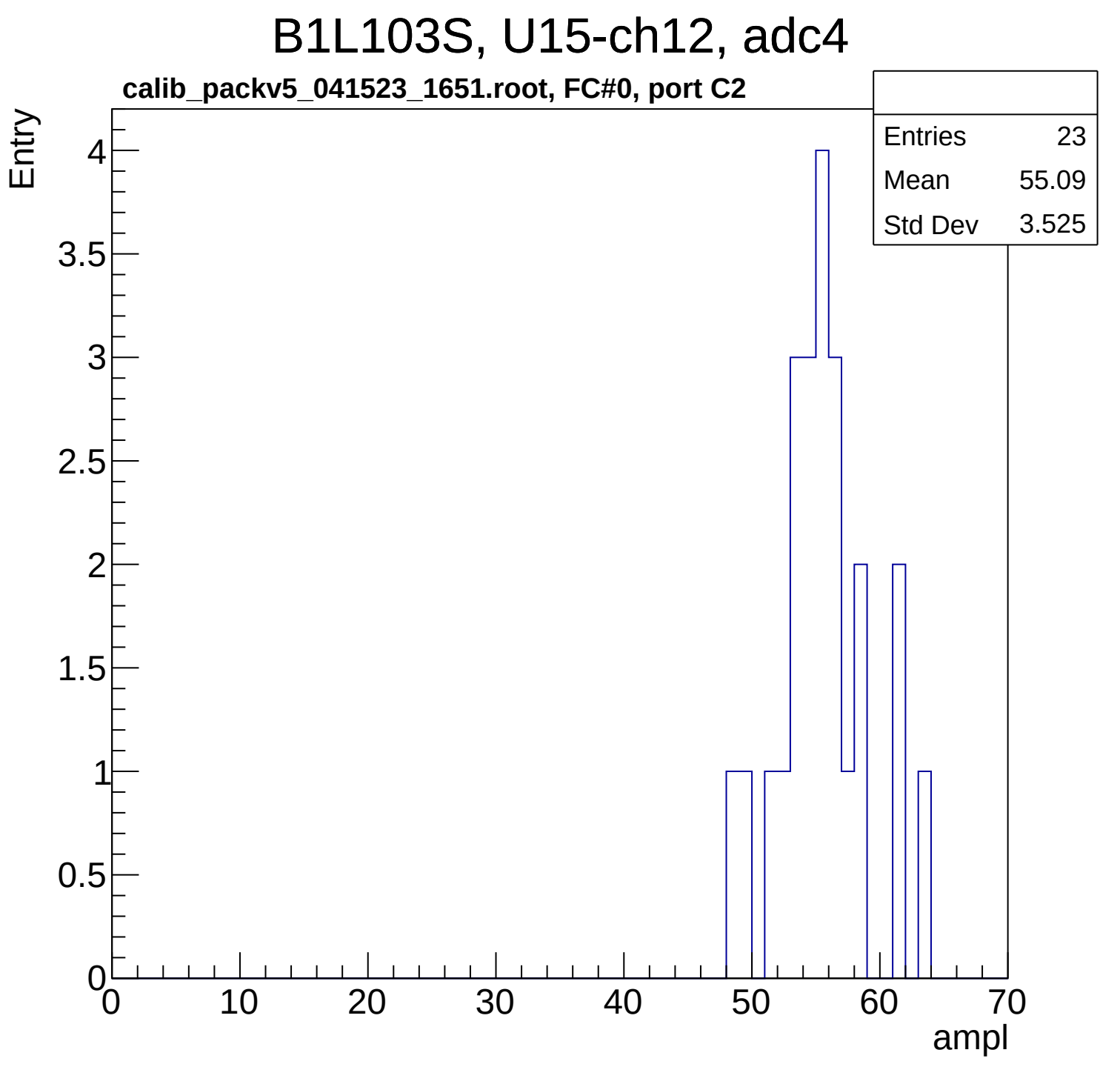

B1L103S, U15-ch11, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 0
Std Dev 0
Entry
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch12, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 23.79
Std Dev 10.98
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U15-ch12, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 36.91
Std Dev 3.483
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch12, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 38.57
Std Dev 13.67
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch12, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 45.19
Std Dev 13.94
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch12, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 55.09
Std Dev 3.525
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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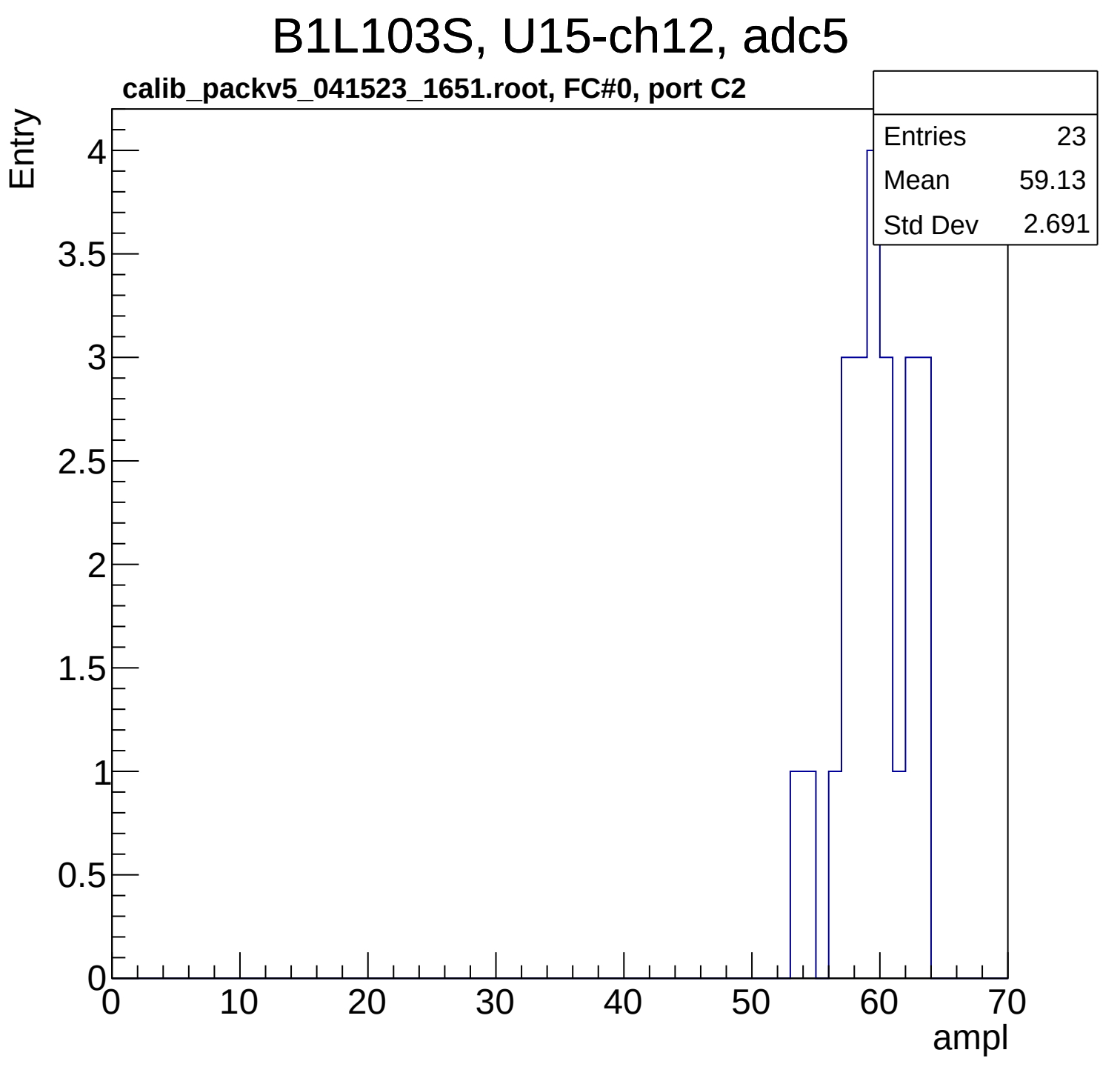
B1L103S, U15-ch12, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 59.13
Std Dev 2.691
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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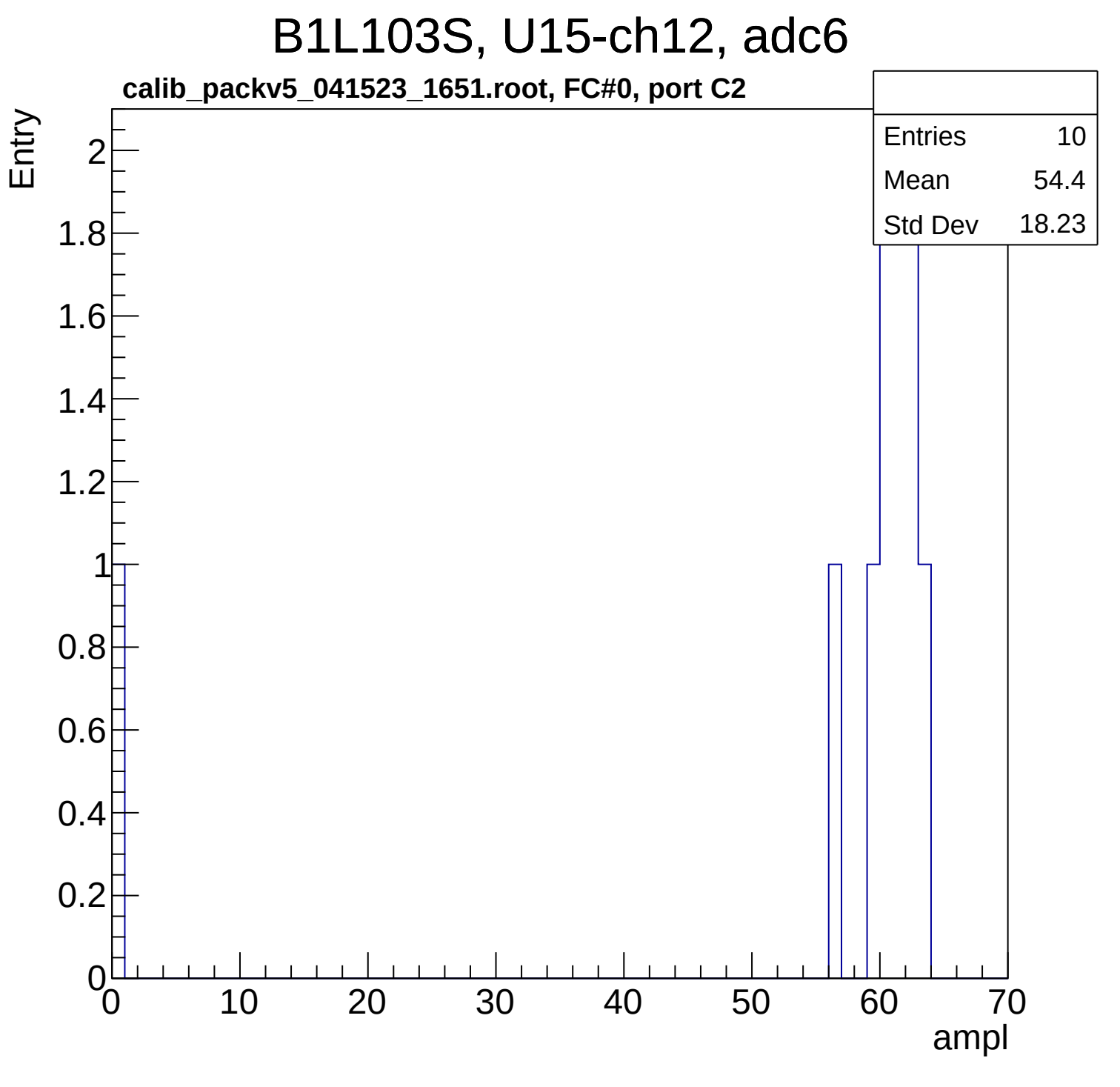
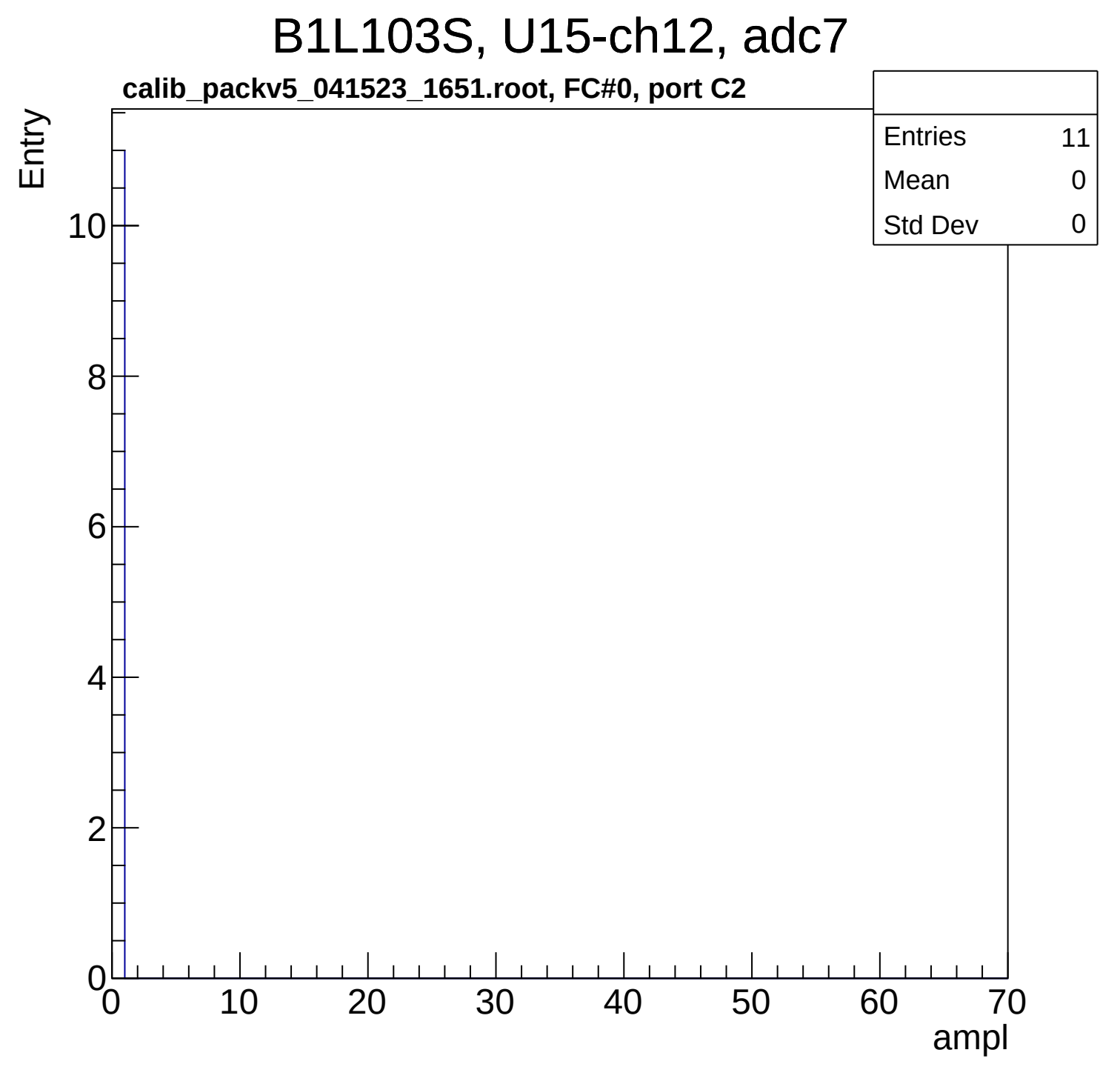
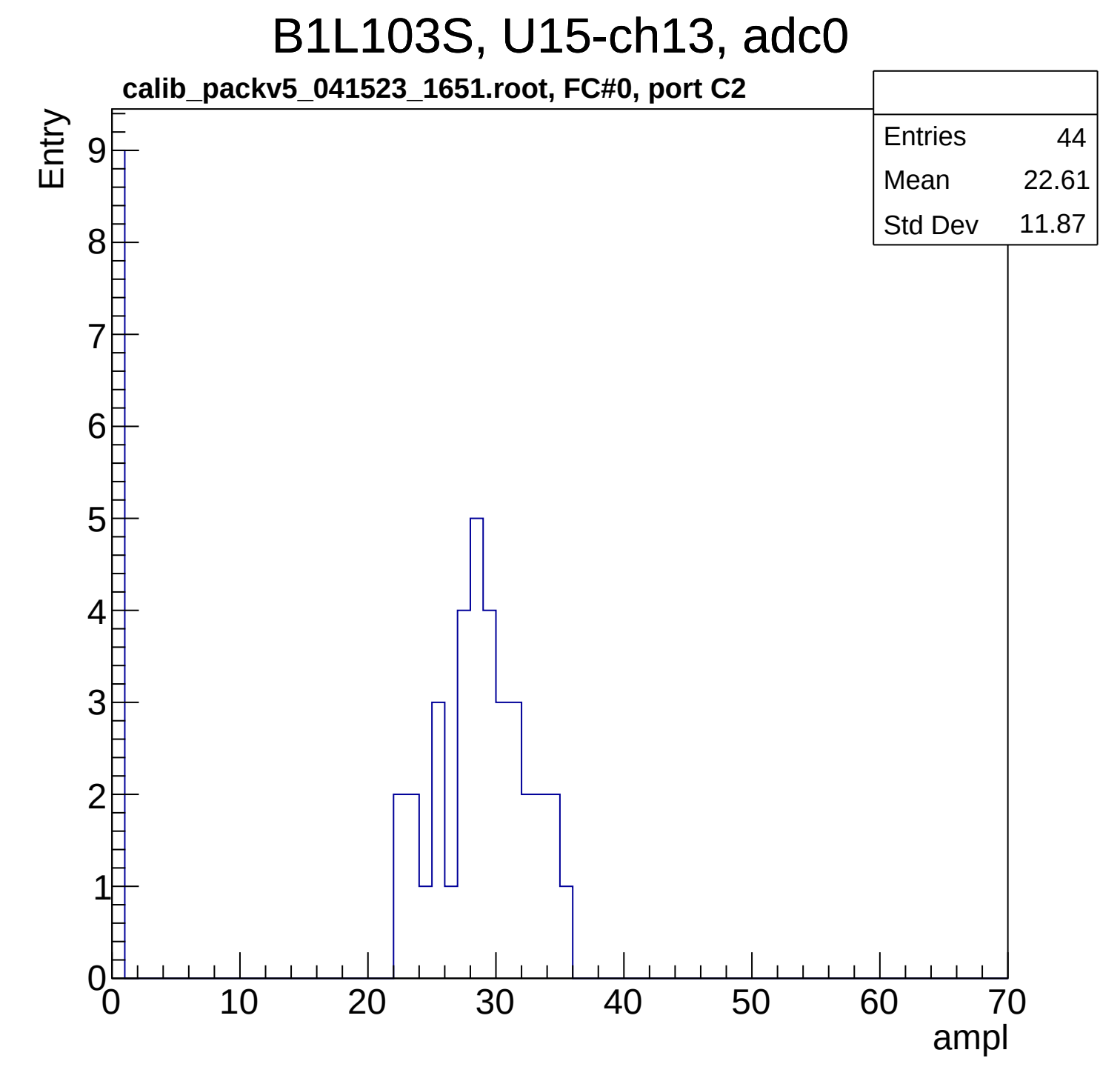
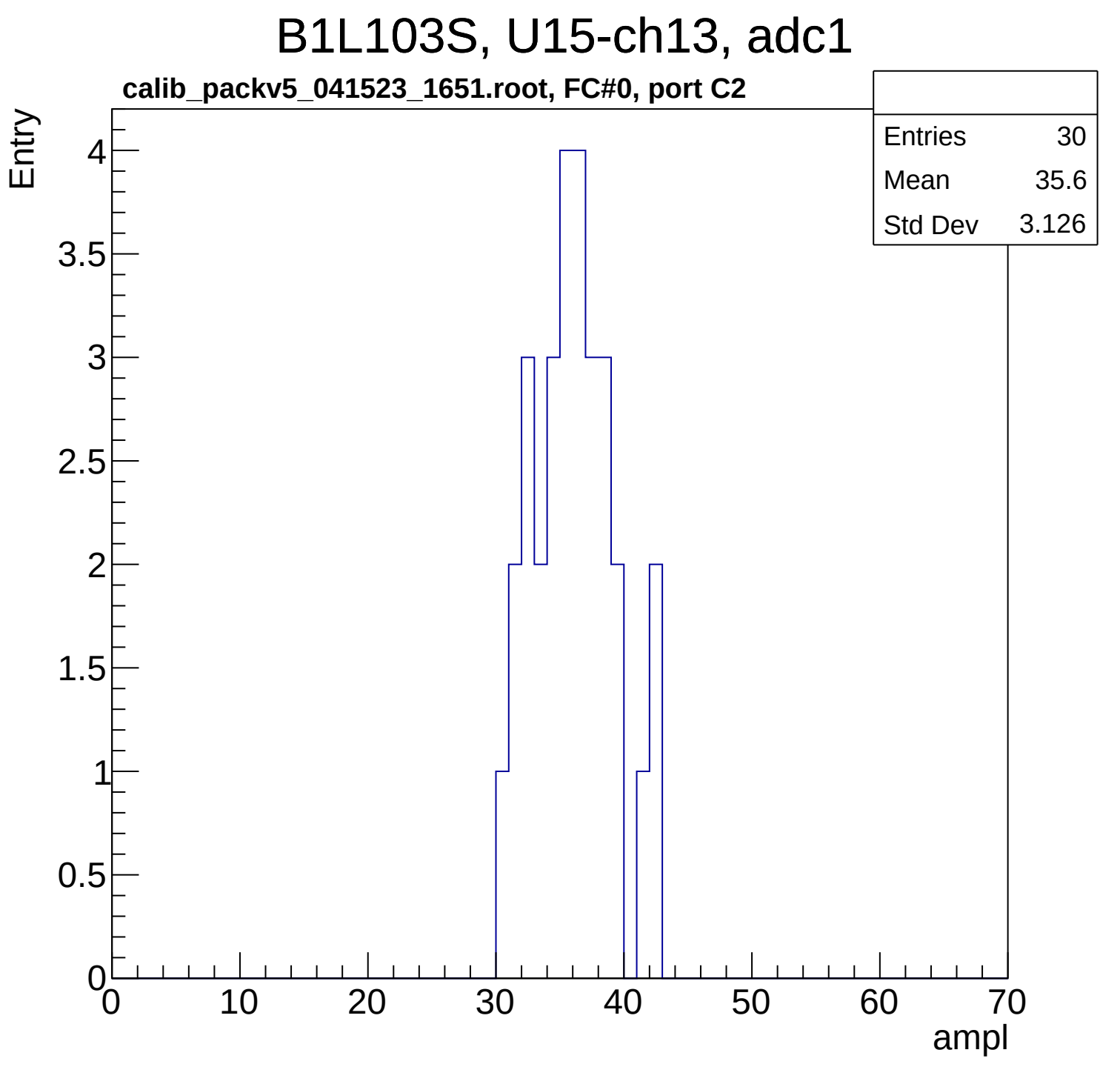
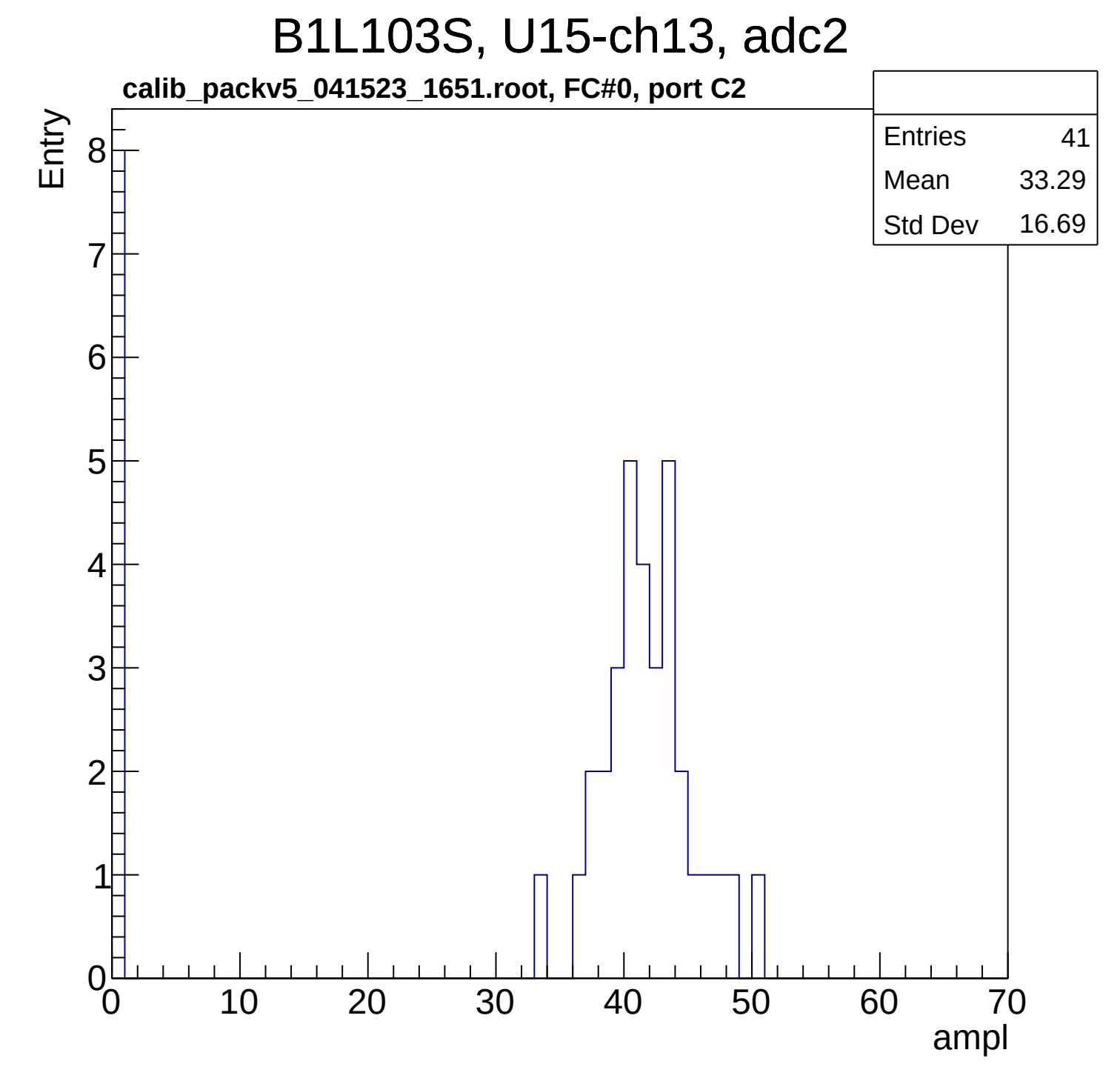
40
50
60
70

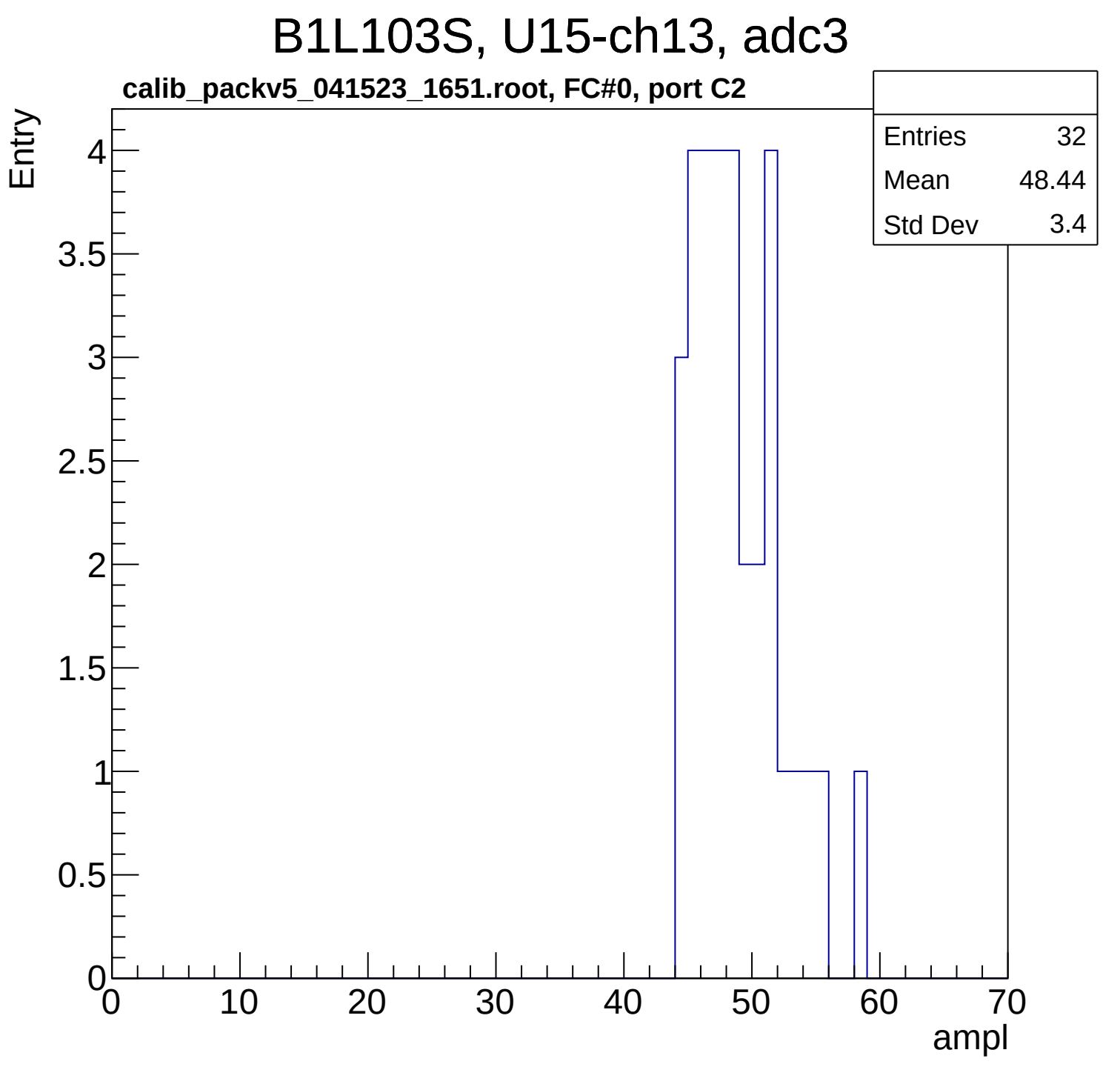

B1L103S, U15-ch12, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 54.4
Std Dev 18.23
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

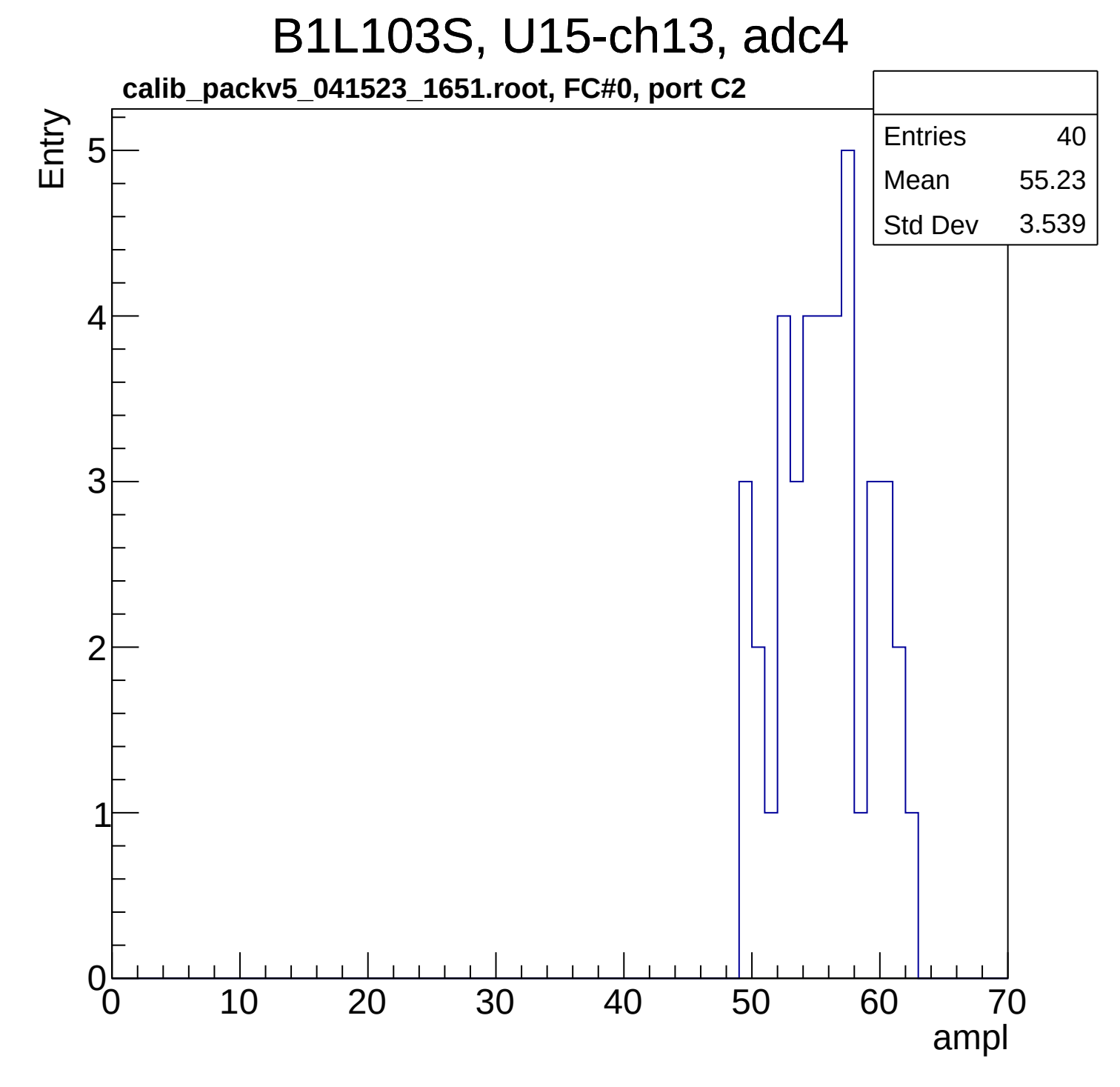

B1L103S, U15-ch12, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

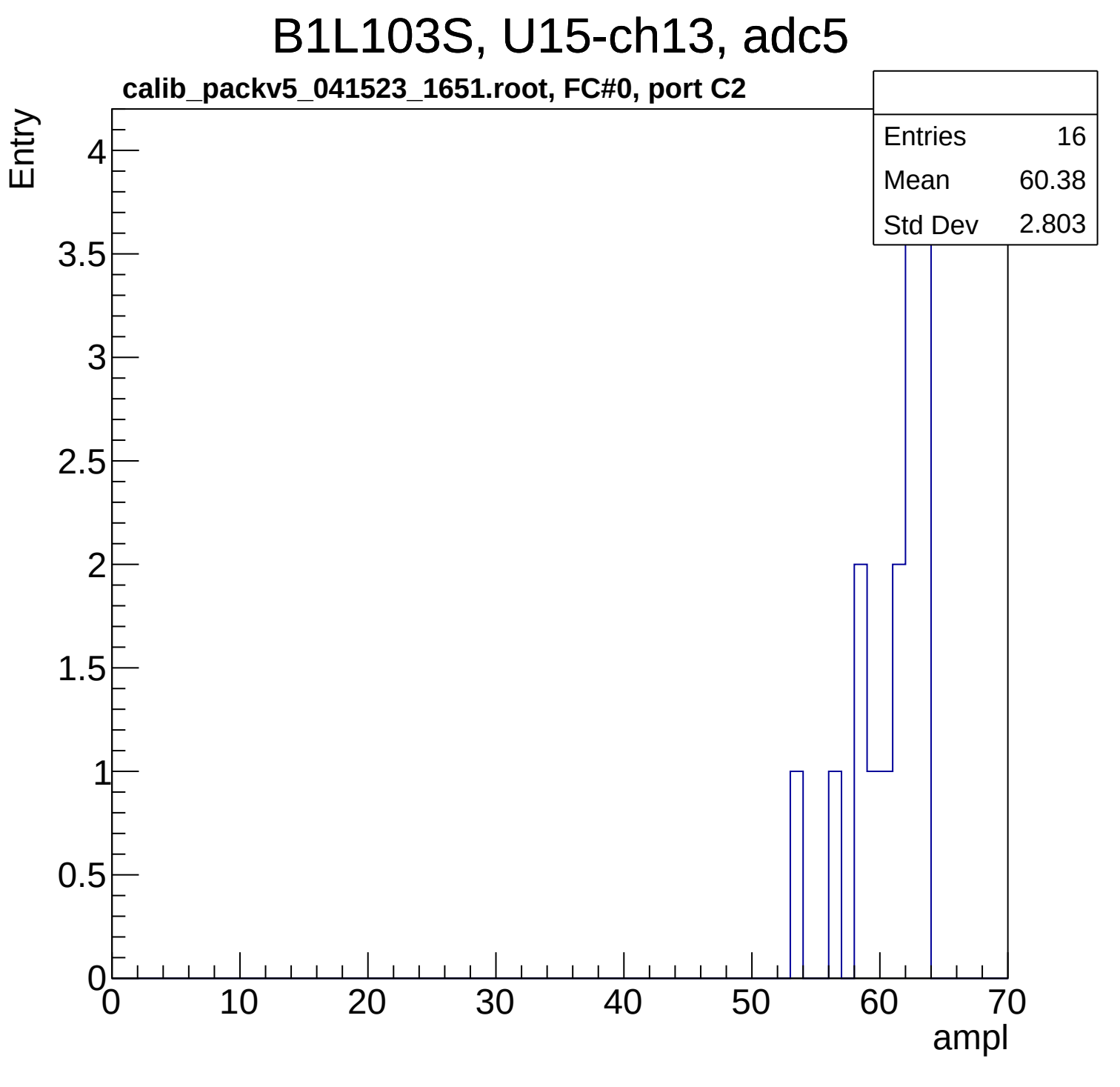

B1L103S, U15-ch13, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 22.61
Std Dev 11.87
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

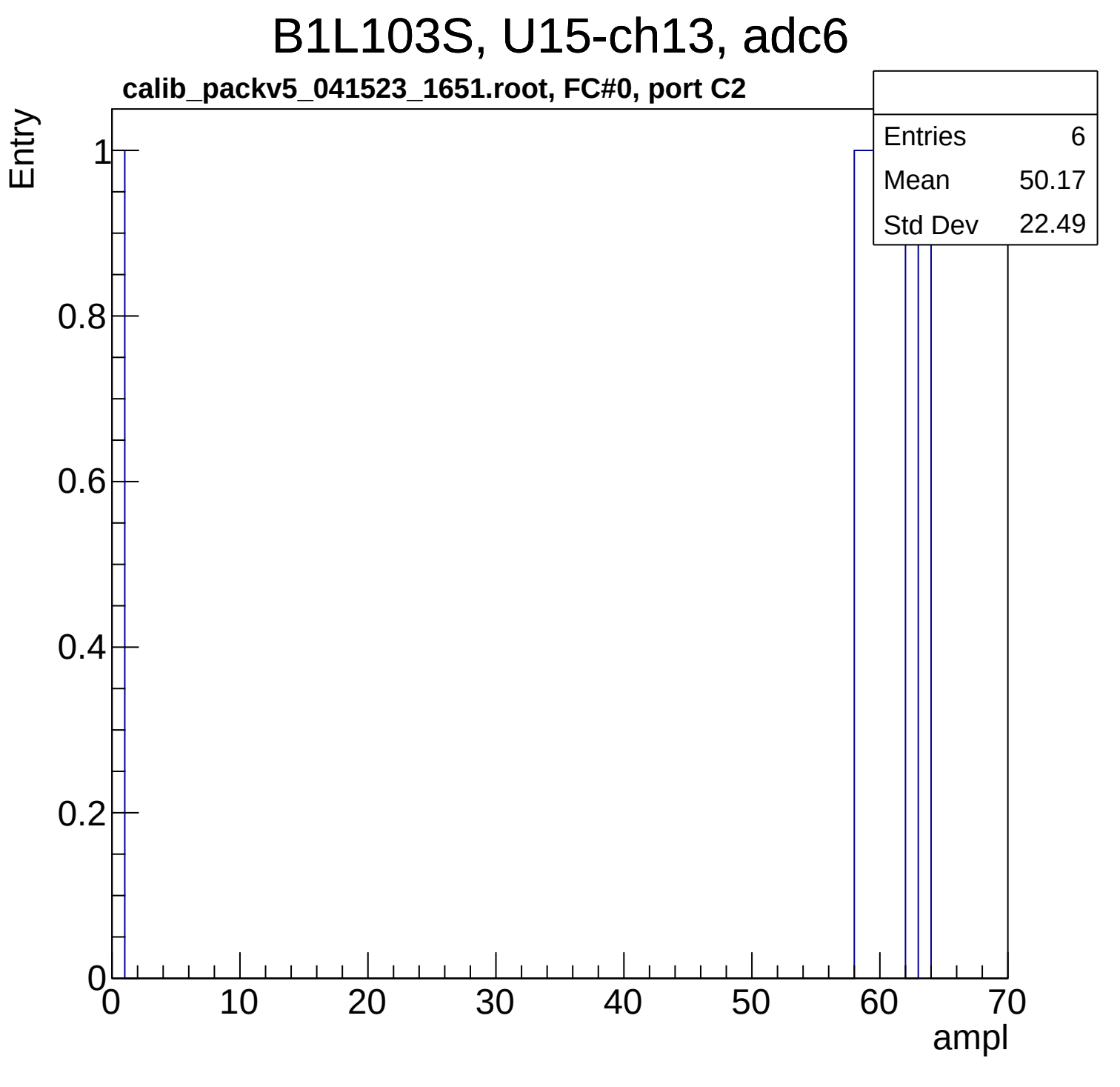

B1L103S, U15-ch13, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 35.6
Std Dev 3.126
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

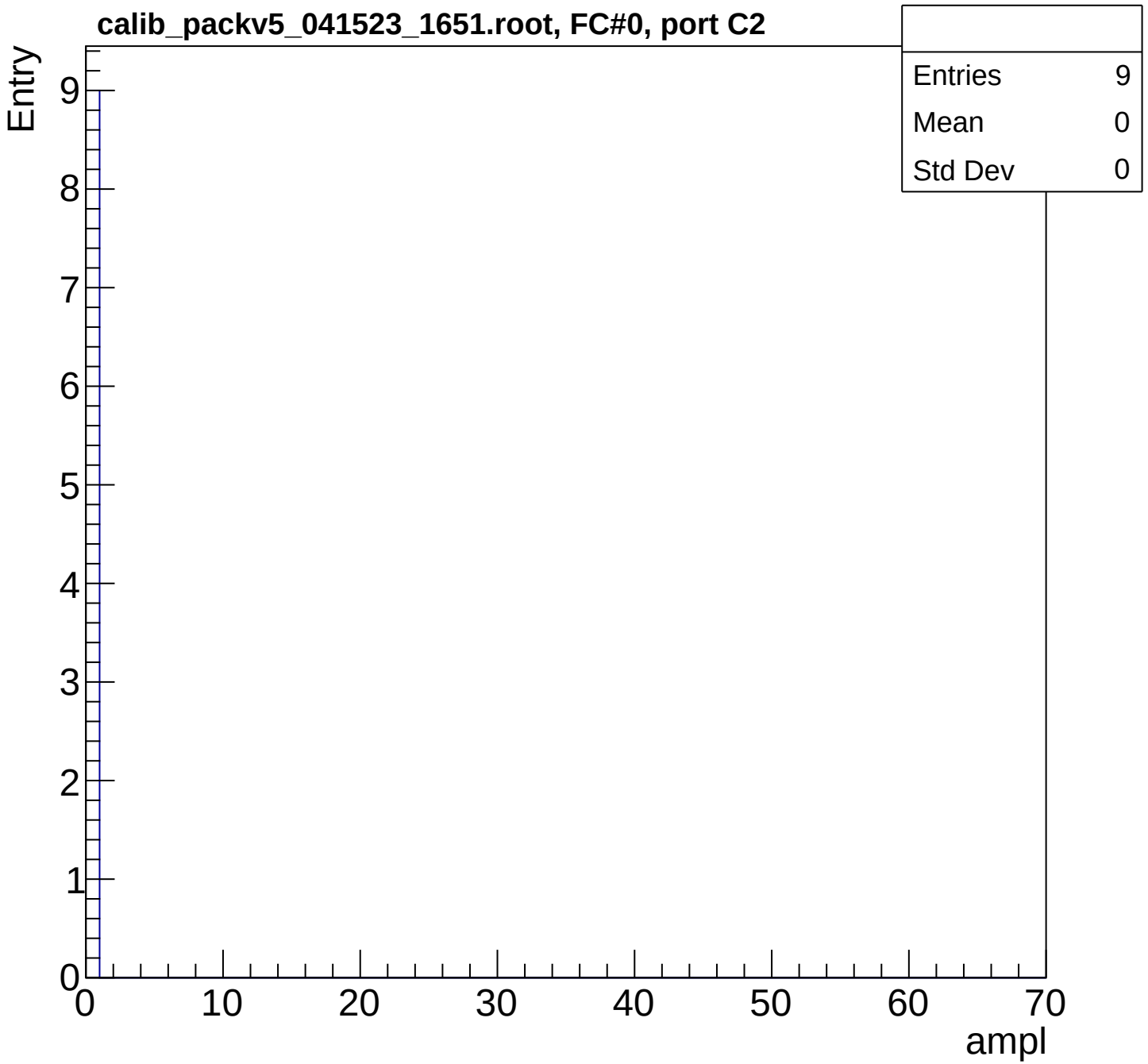

B1L103S, U15-ch13, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 33.29
Std Dev 16.69
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

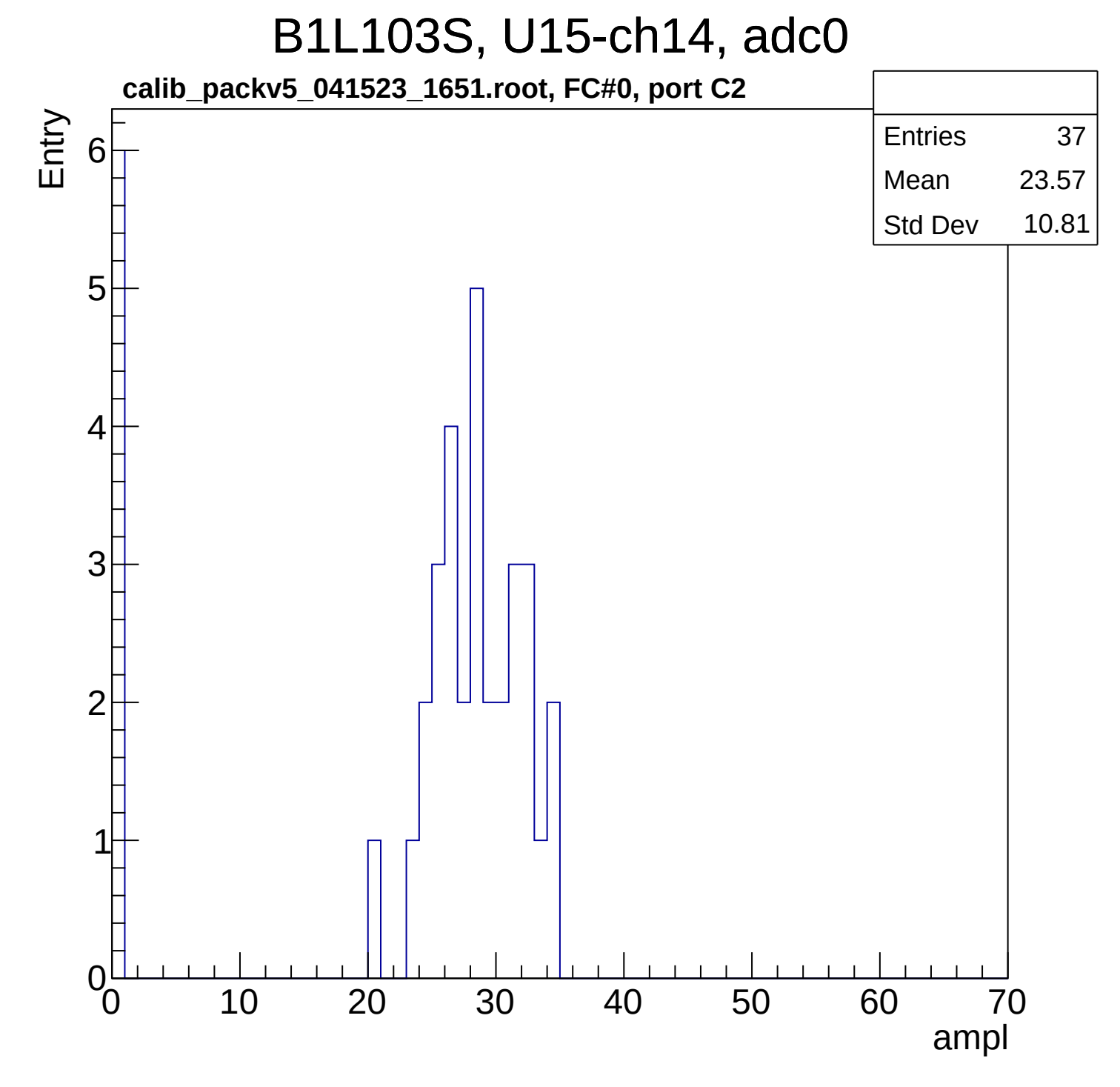

B1L103S, U15-ch13, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 48.44
Std Dev 3.4
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

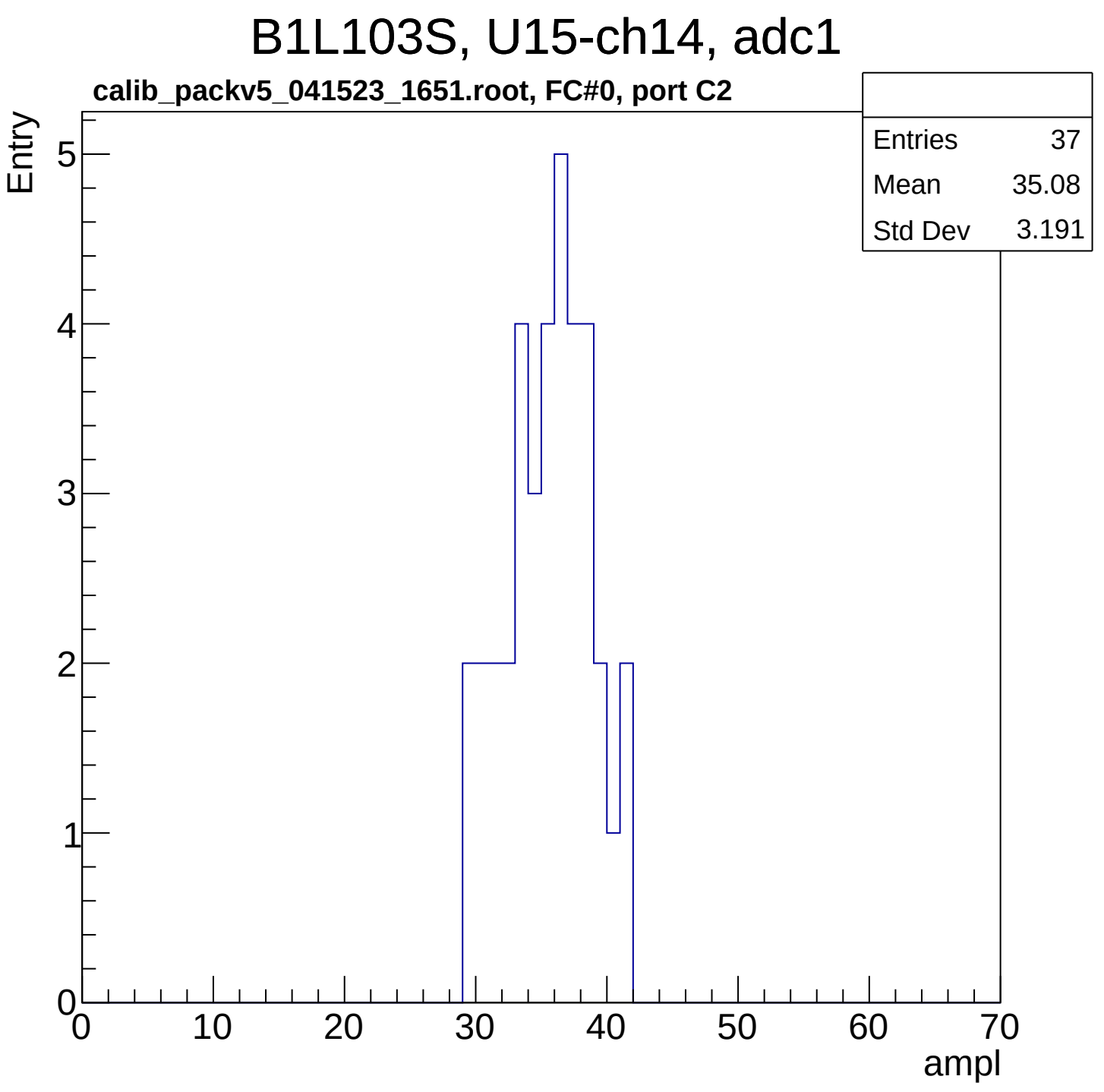

B1L103S, U15-ch13, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 55.23
Std Dev 3.539
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

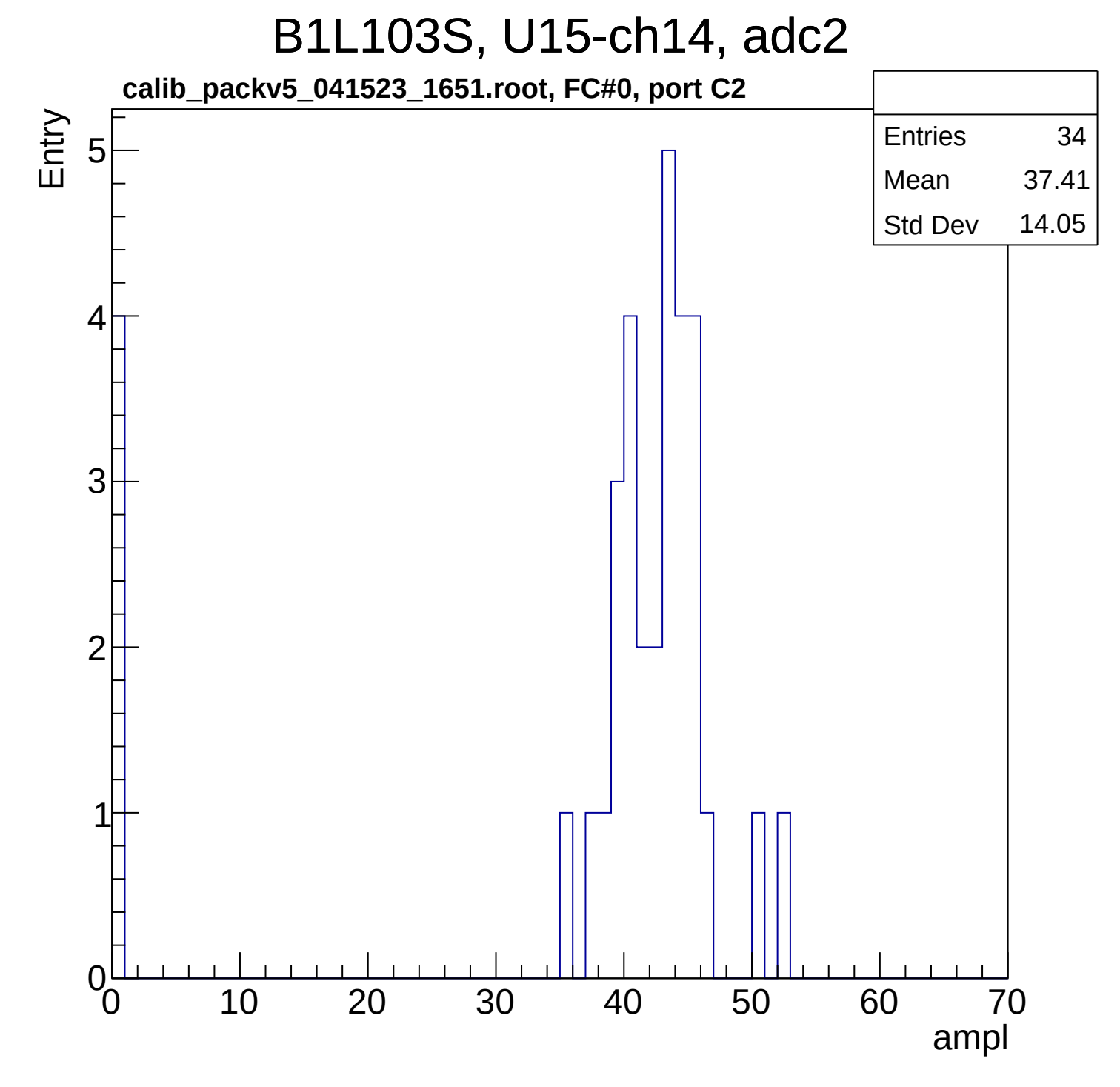

B1L103S, U15-ch13, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 60.38
Std Dev 2.803
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

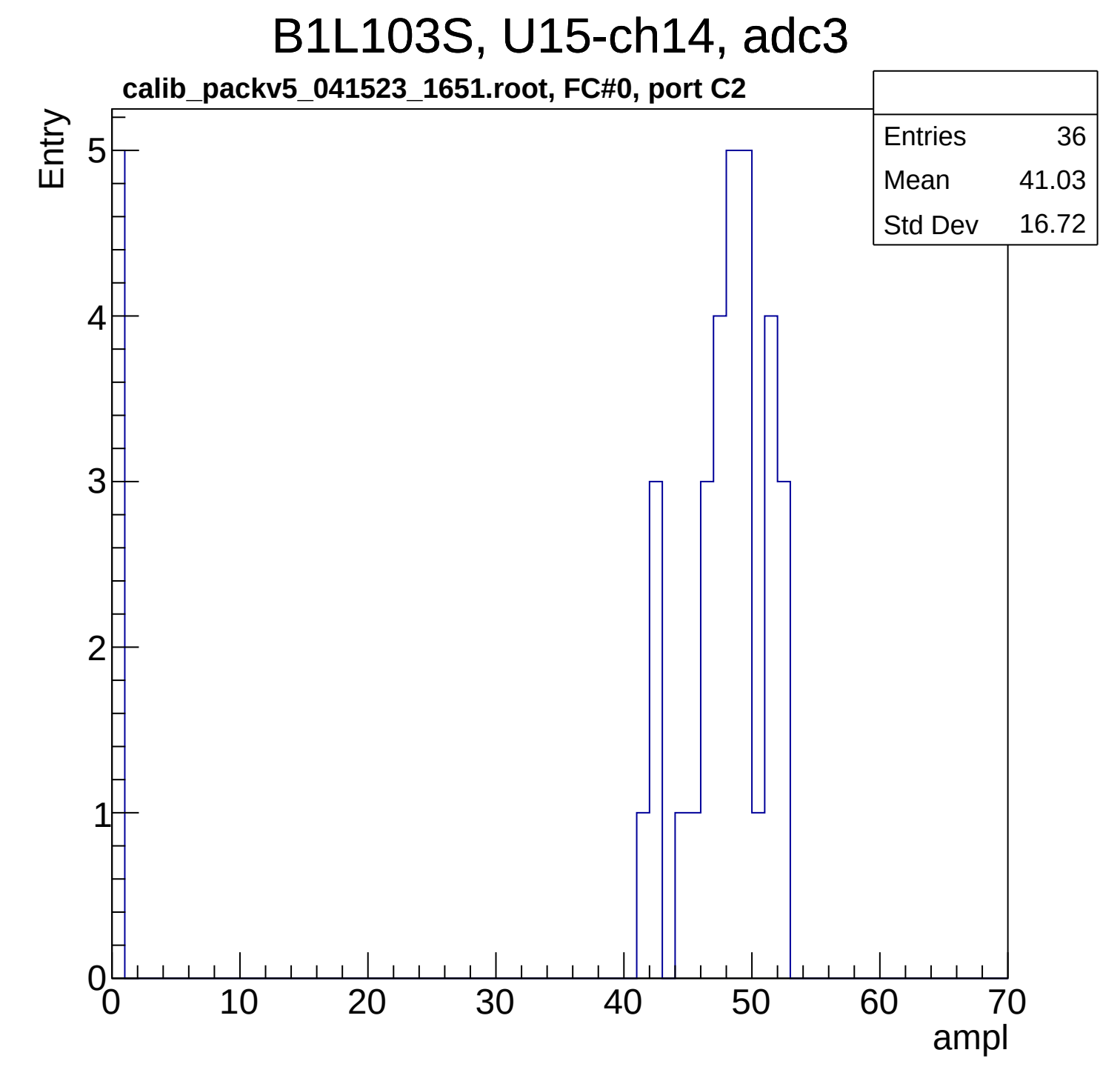

B1L103S, U15-ch13, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 50.17
Std Dev 22.49
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

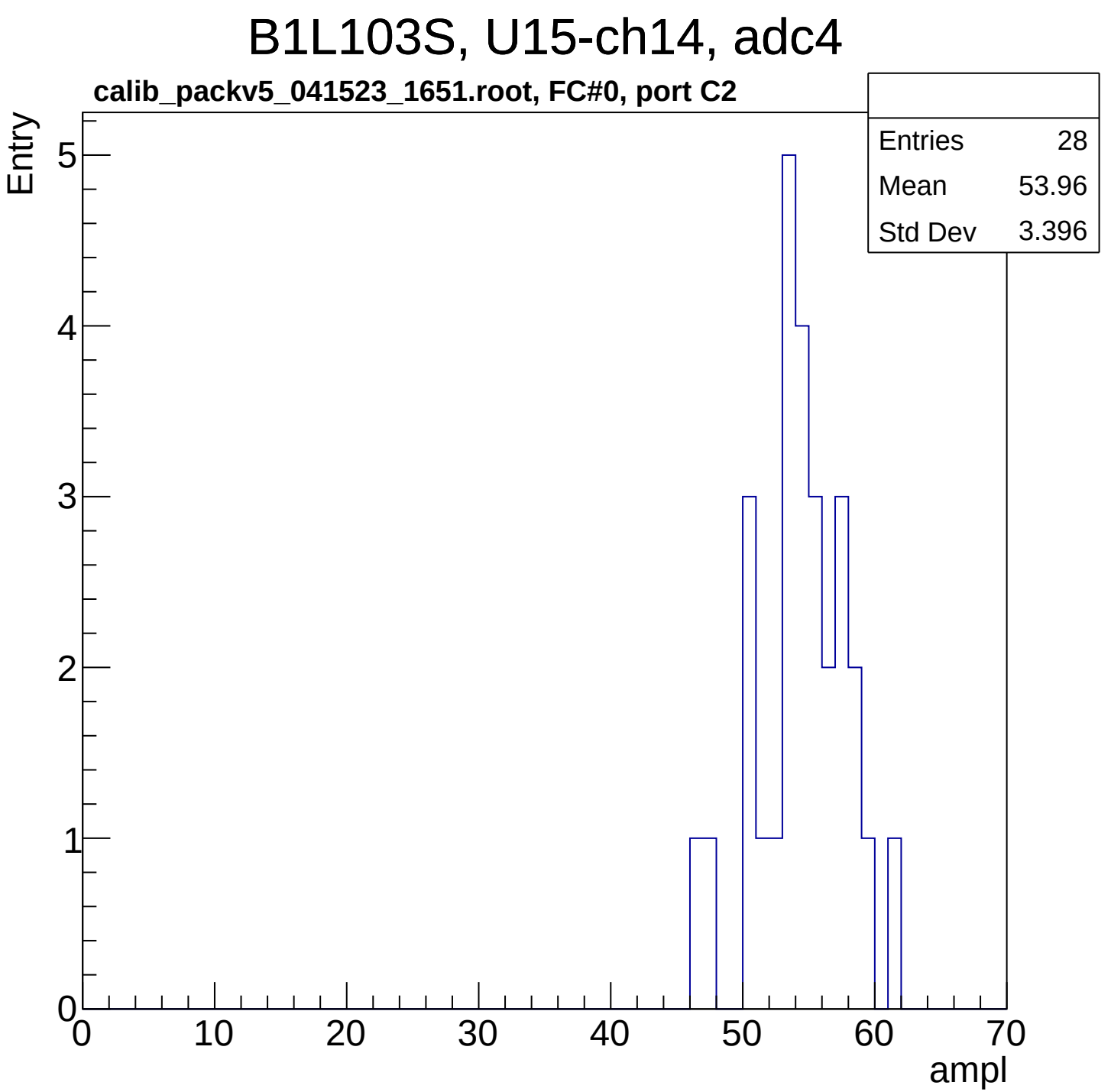

B1L103S, U15-ch13, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 0
Std Dev 0
Entry
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70
ampl

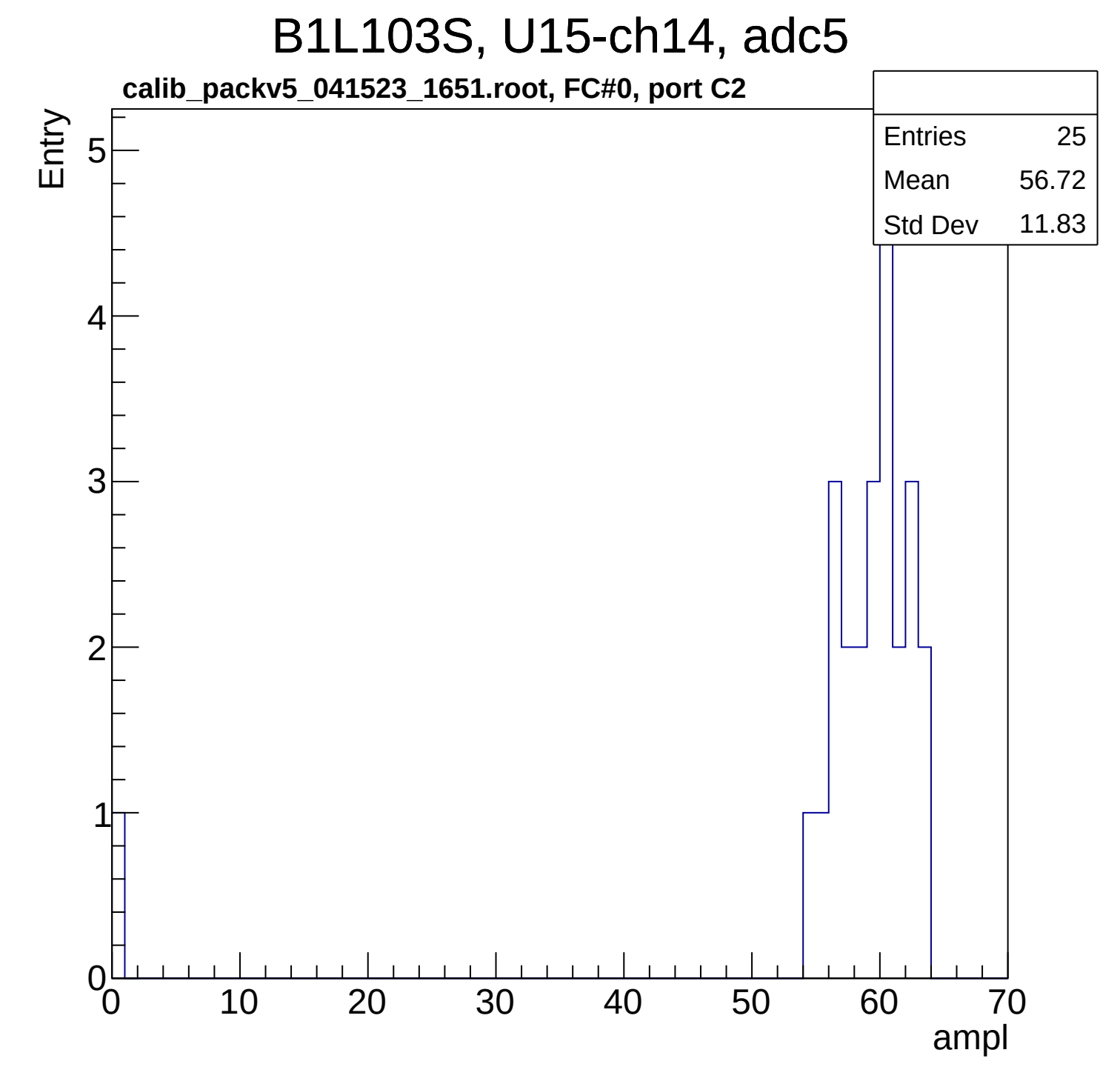

B1L103S, U15-ch14, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 23.57
Std Dev 10.81
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

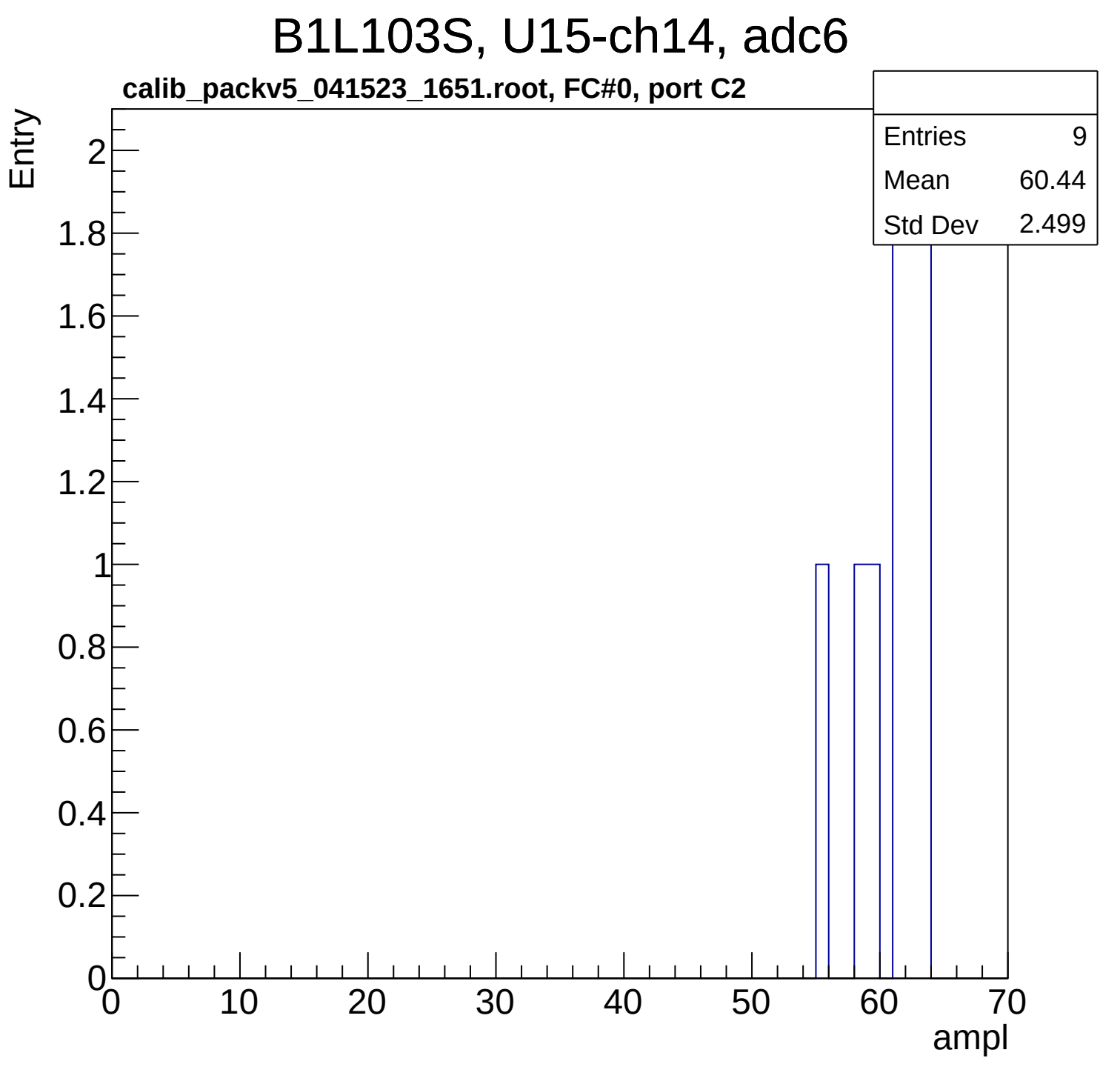

B1L103S, U15-ch14, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 35.08
Std Dev 3.191
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

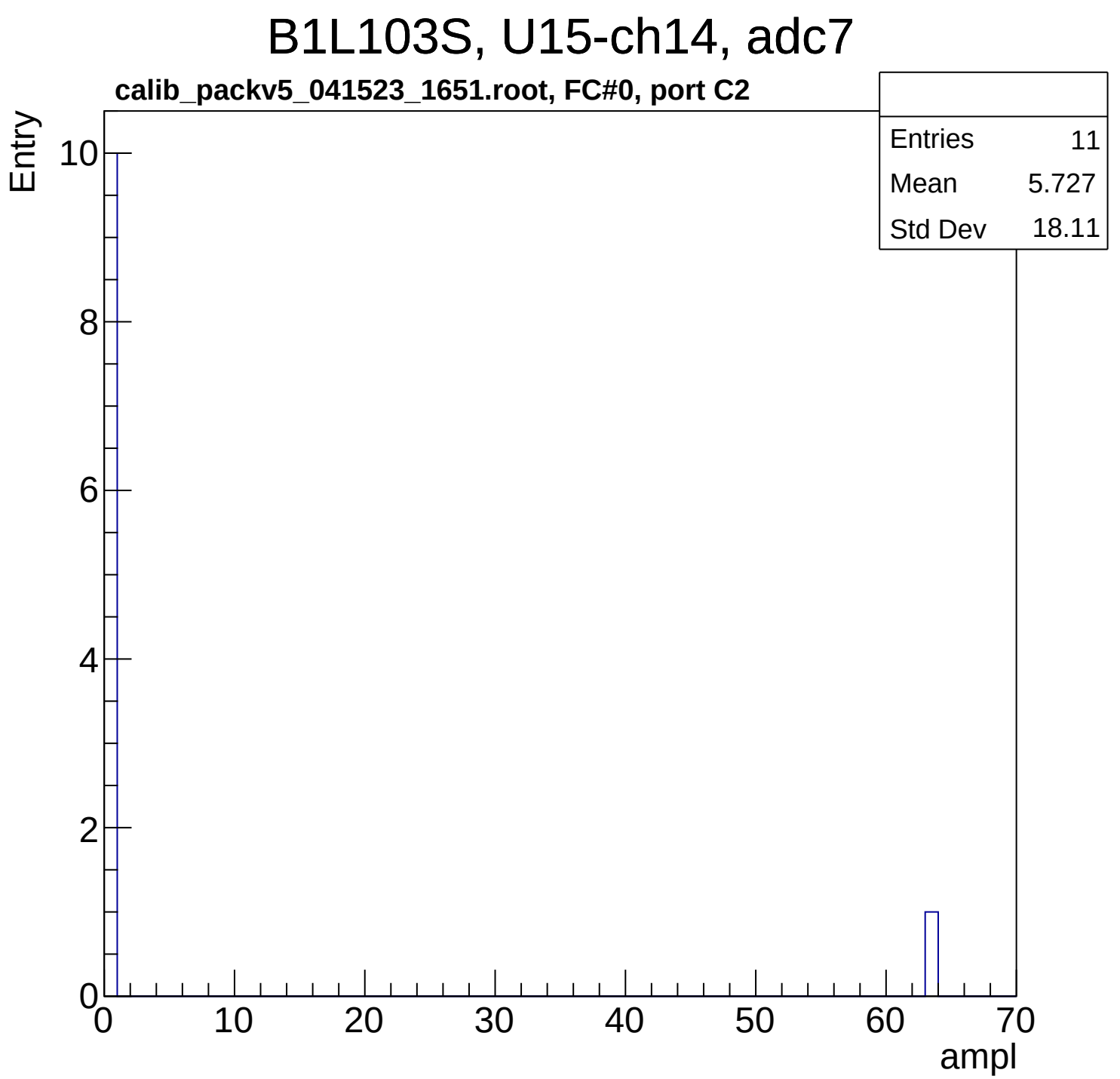

B1L103S, U15-ch14, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 37.41
Std Dev 14.05
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

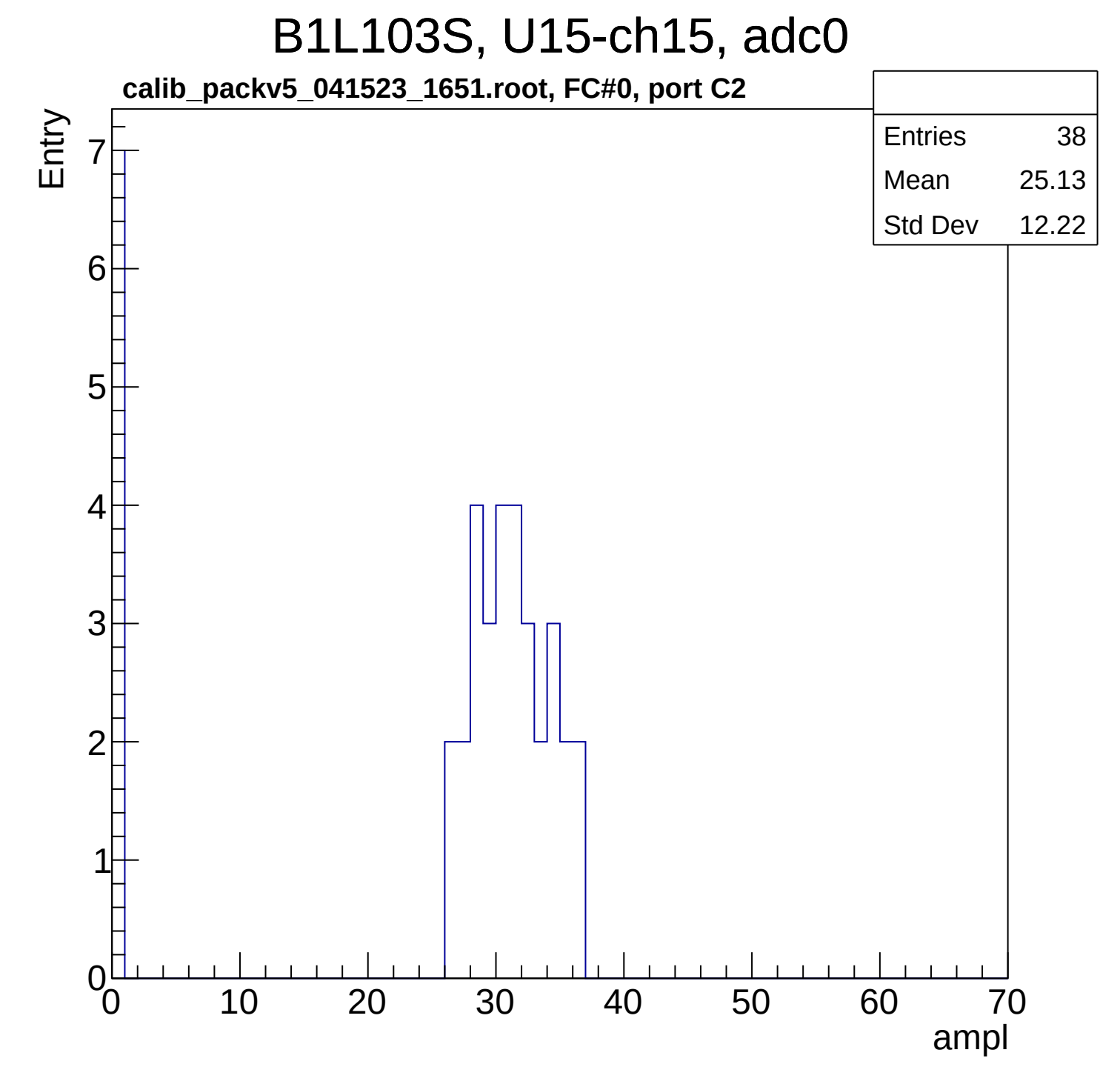

B1L103S, U15-ch14, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 41.03
Std Dev 16.72
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

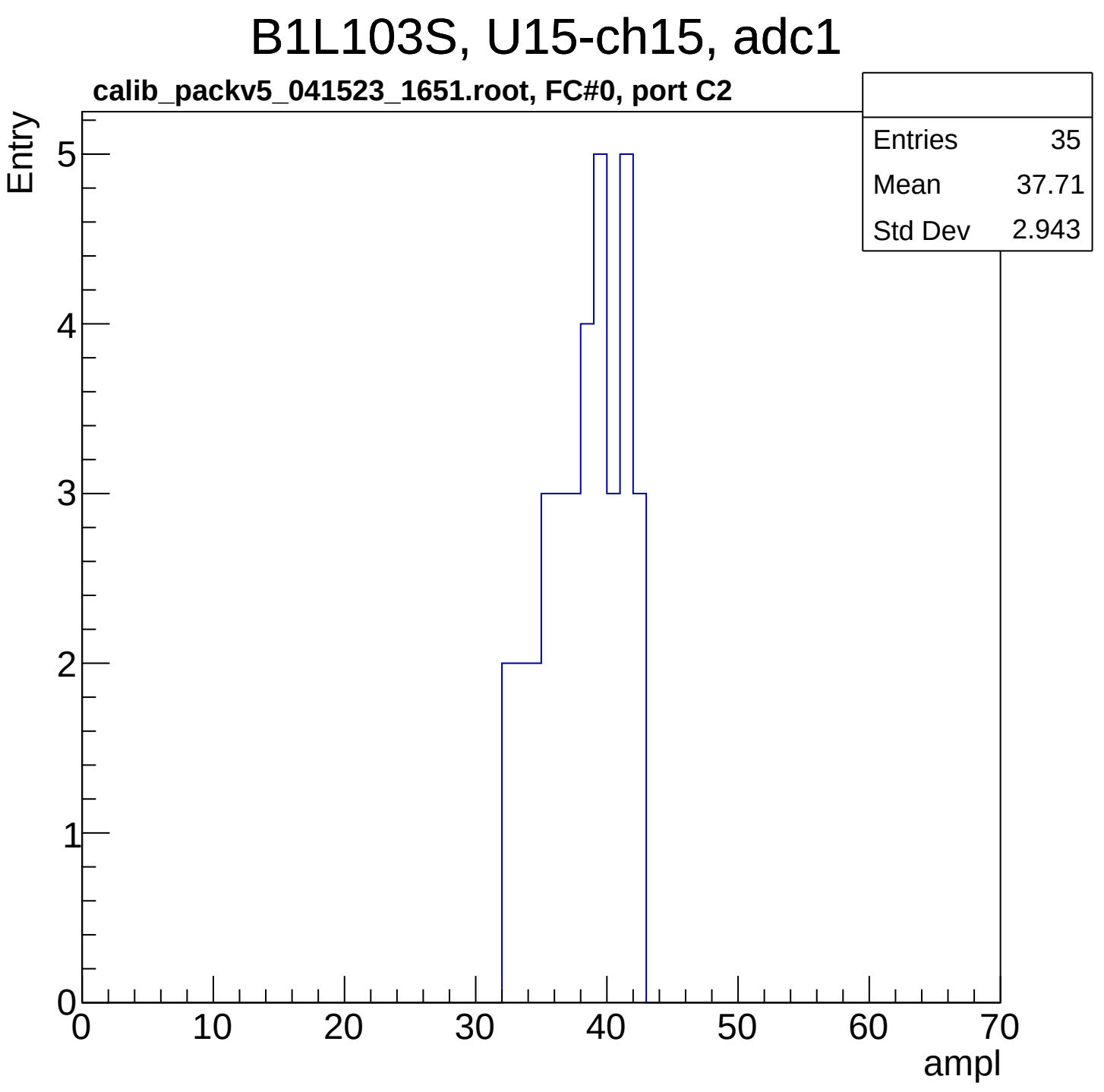

B1L103S, U15-ch14, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 53.96
Std Dev 3.396
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

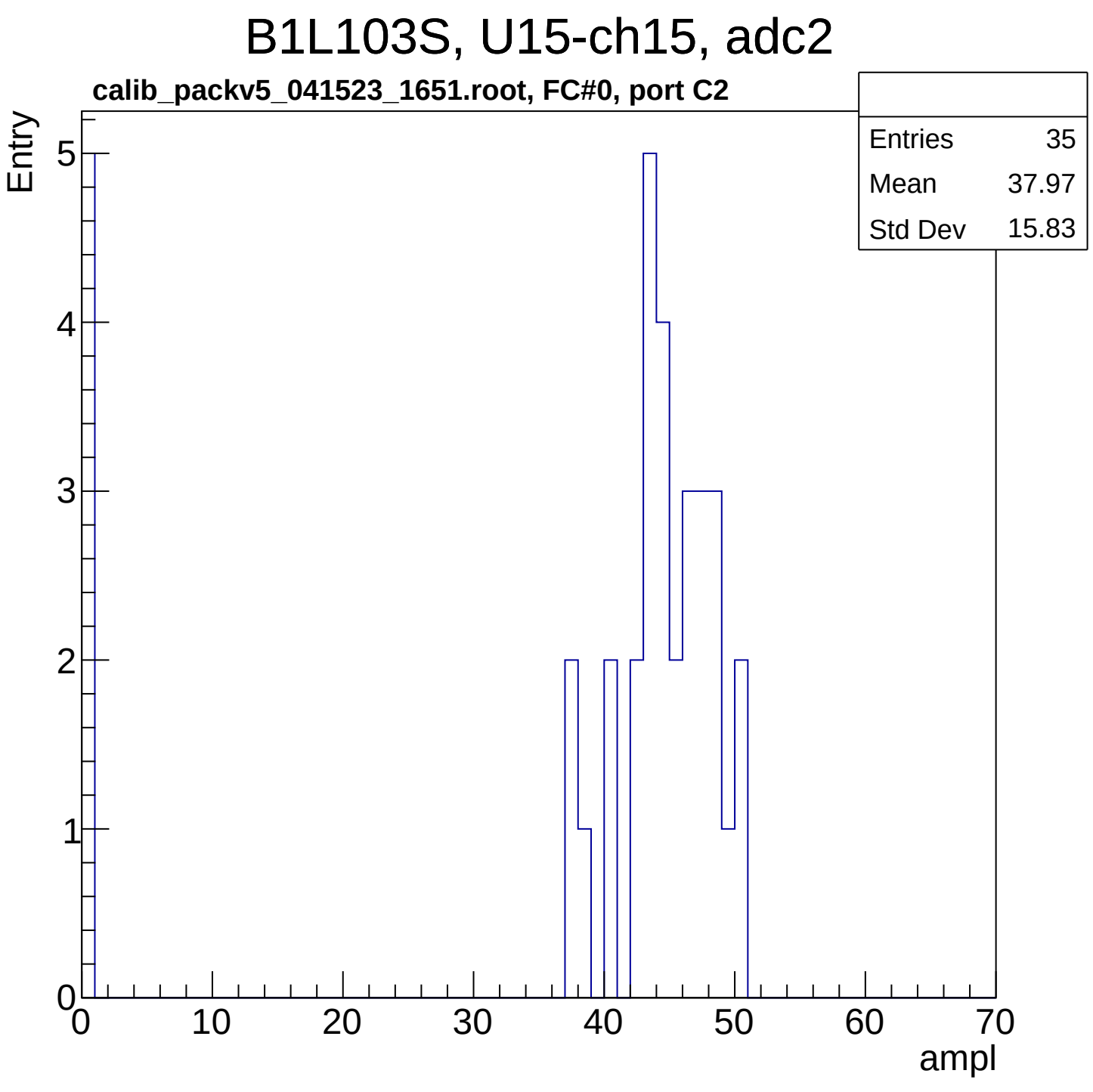

B1L103S, U15-ch14, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 56.72
Std Dev 11.83
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

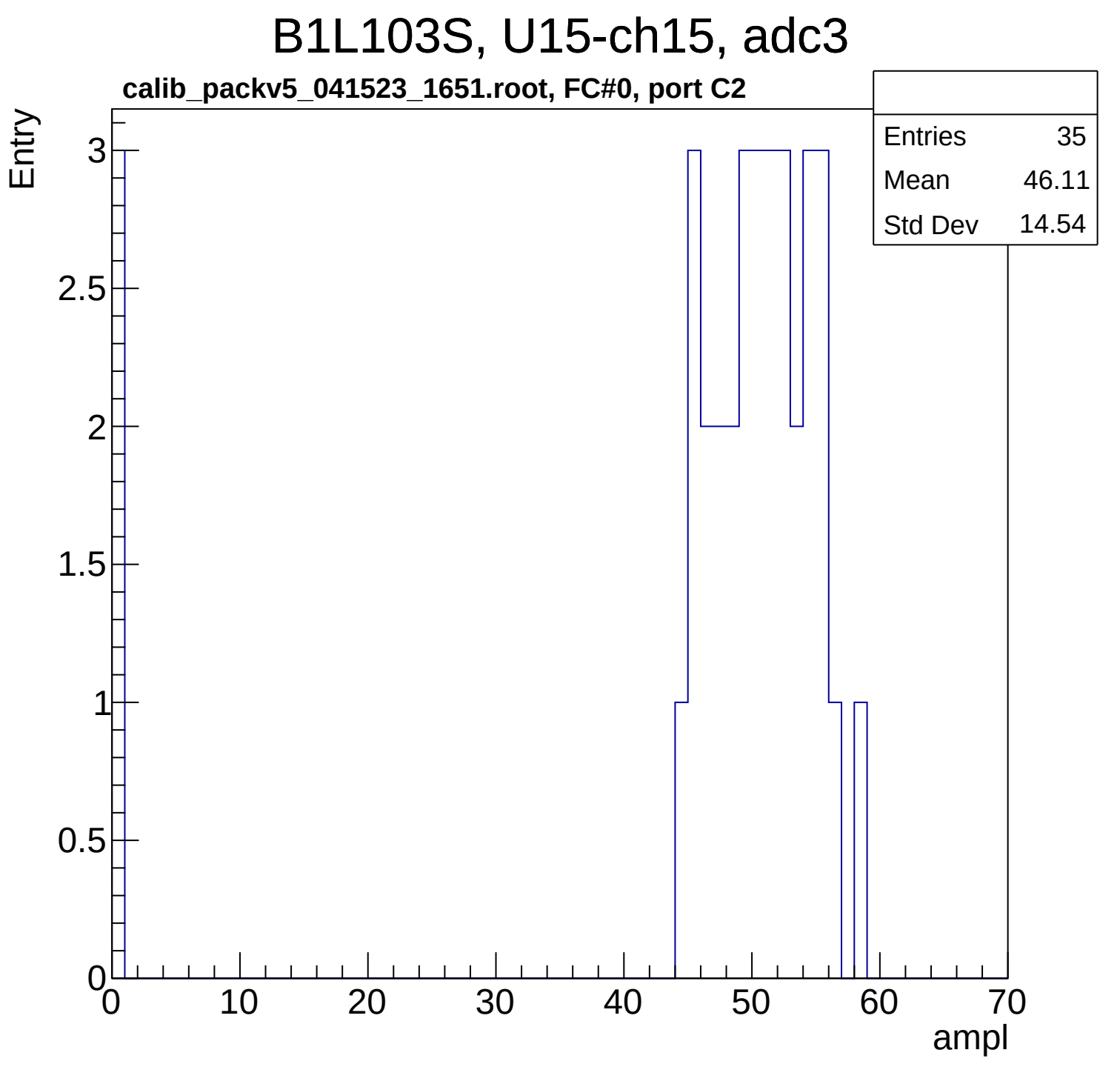

B1L103S, U15-ch14, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 60.44
Std Dev 2.499
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U15-ch14, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 5.727
Std Dev 18.11
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch15, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 25.13
Std Dev 12.22
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U15-ch15, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 37.71
Std Dev 2.943
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch15, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 37.97
Std Dev 15.83
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch15, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 46.11
Std Dev 14.54
Entry
ampl
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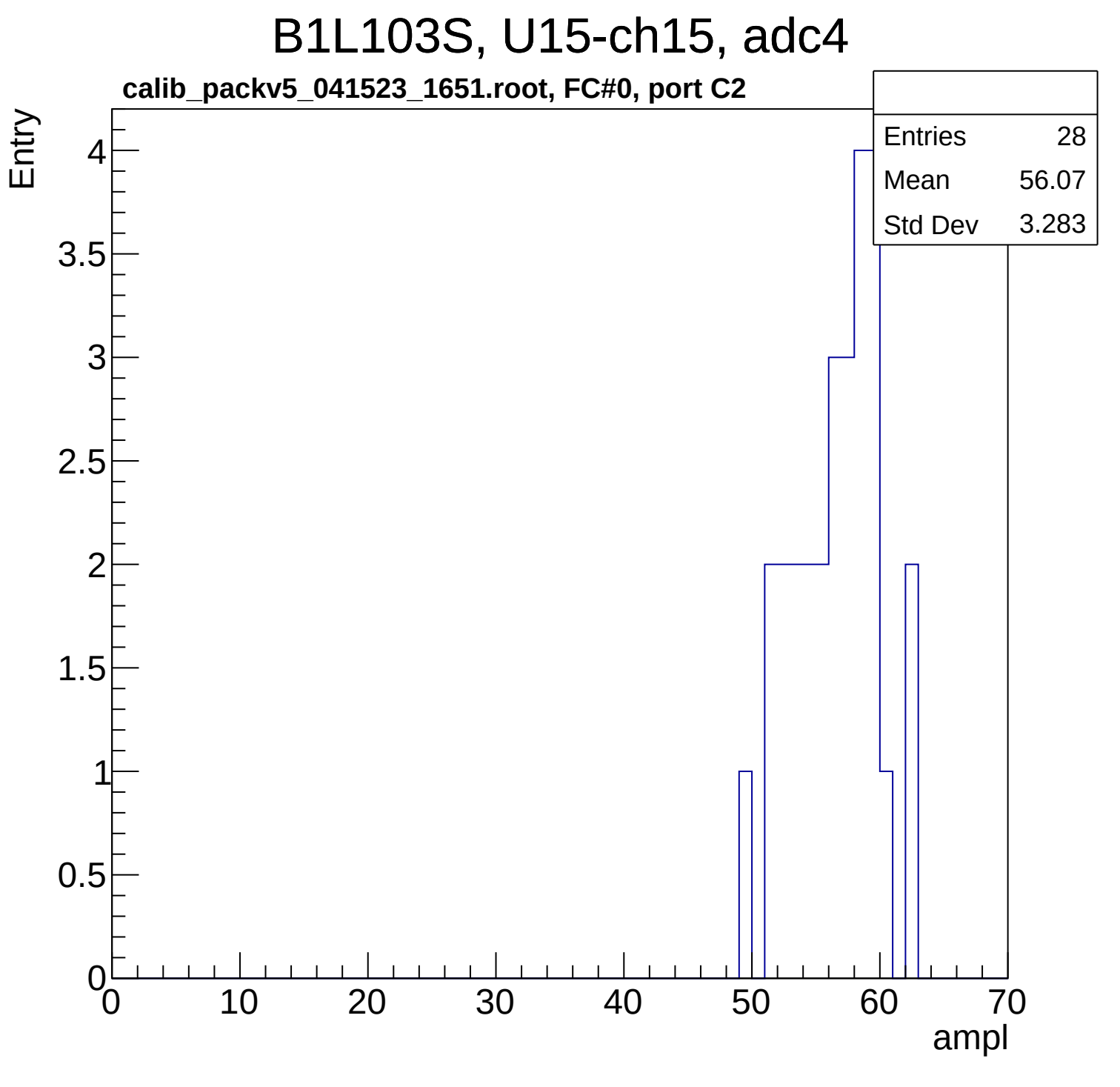
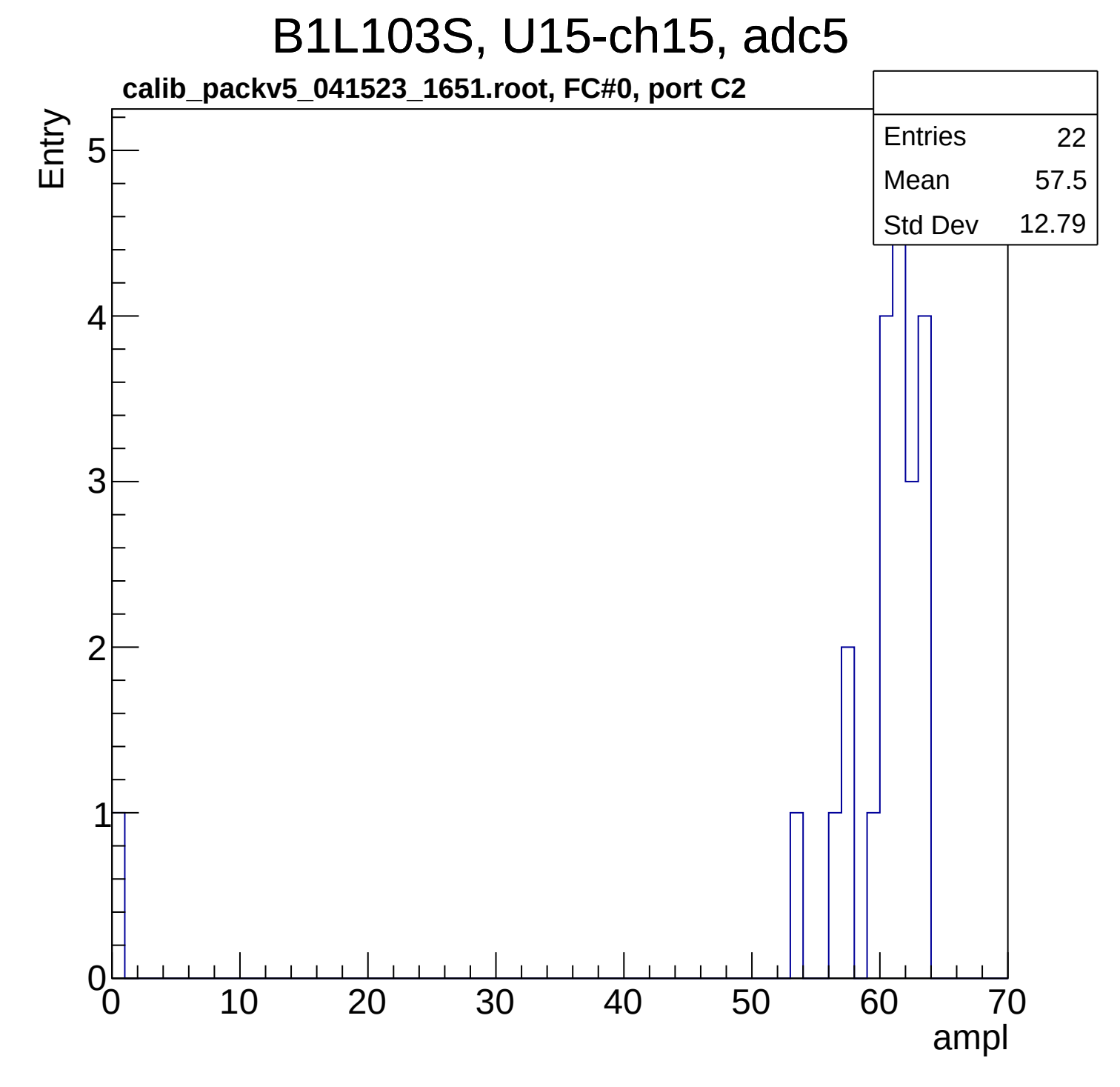
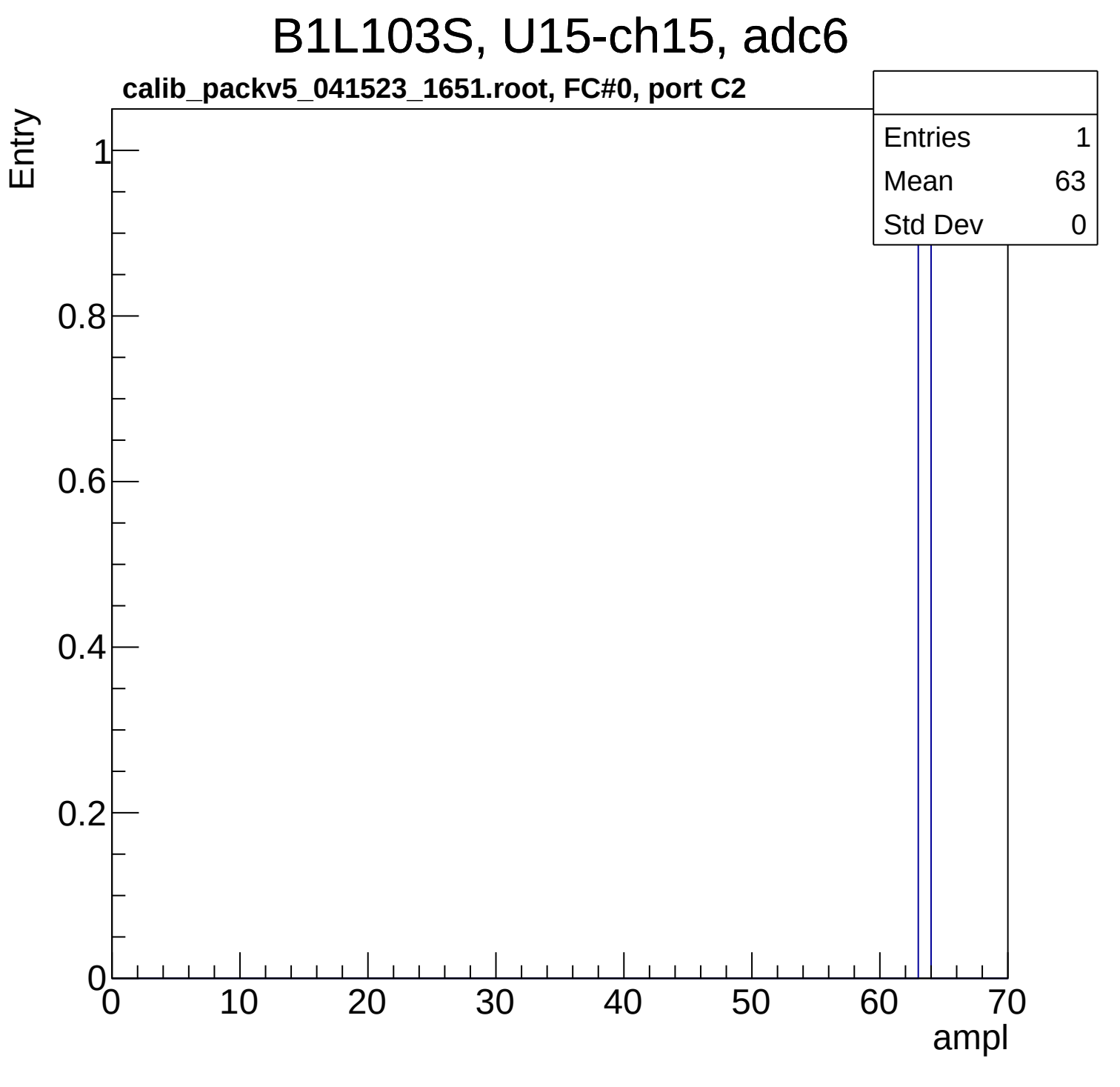
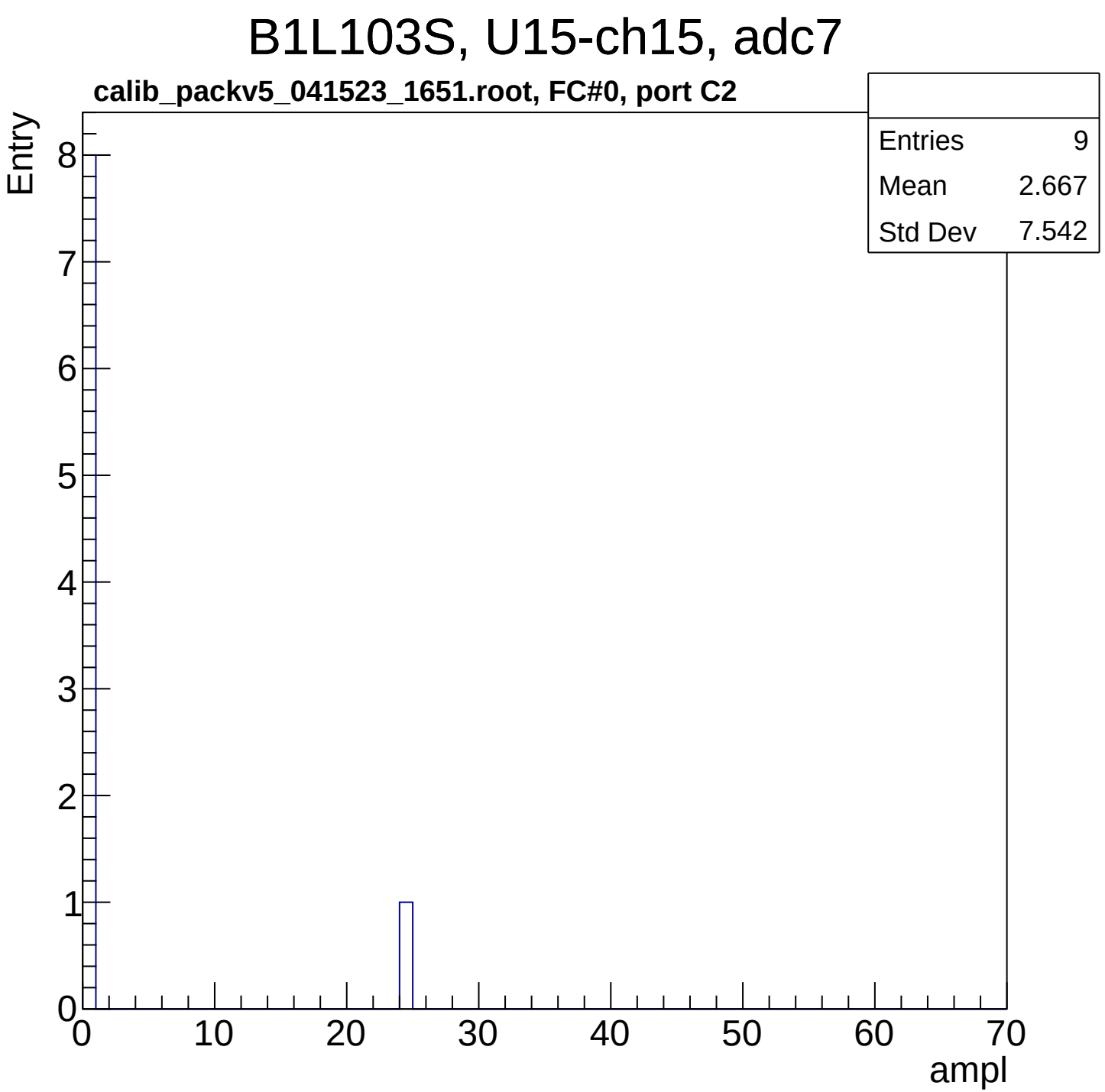
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch15, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 56.07
Std Dev 3.283
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch15, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 57.5
Std Dev 12.79
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch15, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch15, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 2.667
Std Dev 7.542
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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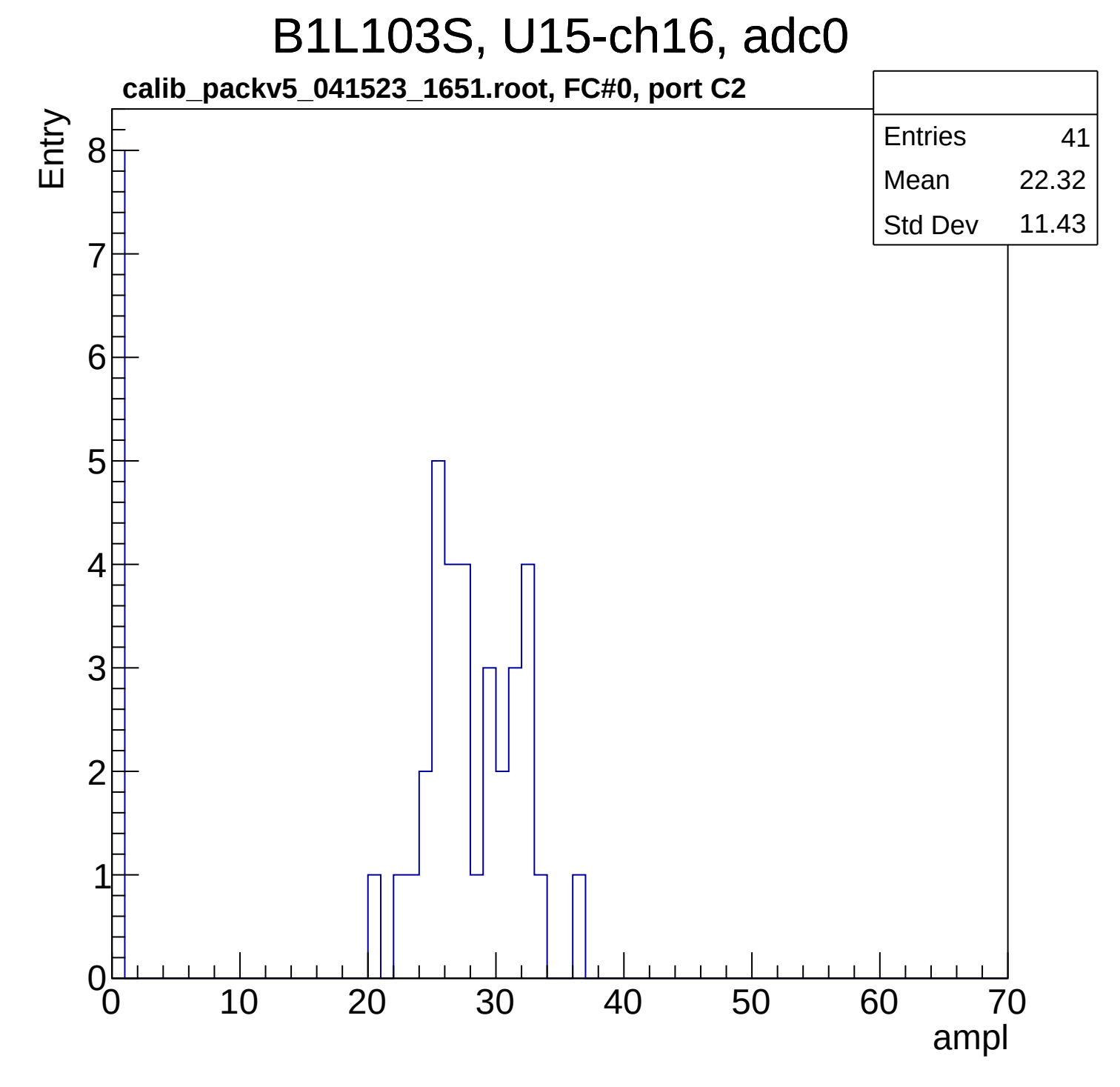
40
50
60
70


B1L103S, U15-ch16, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 22.32
Std Dev 11.43
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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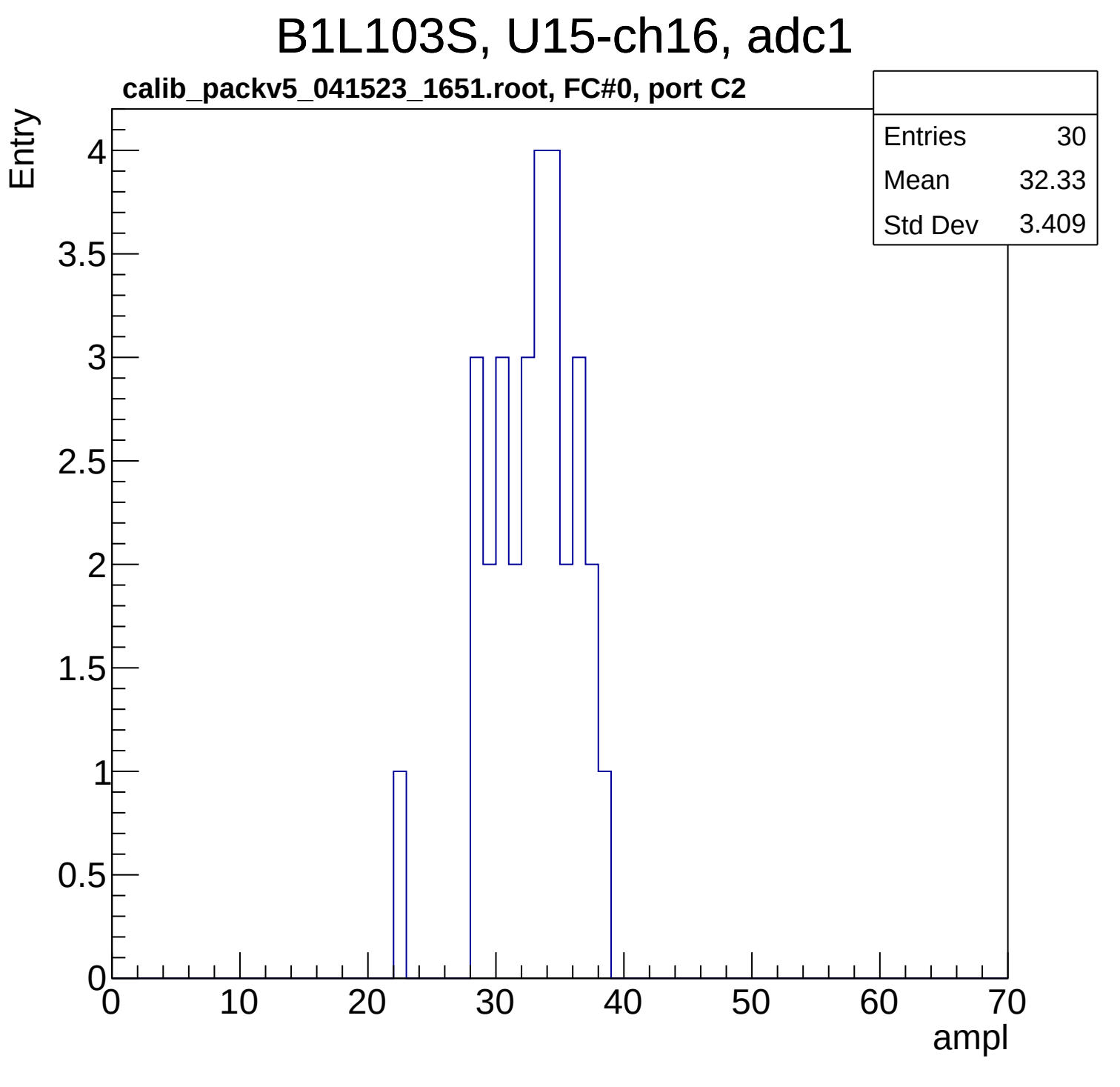
40
50
60
70


B1L103S, U15-ch16, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 32.33
Std Dev 3.409
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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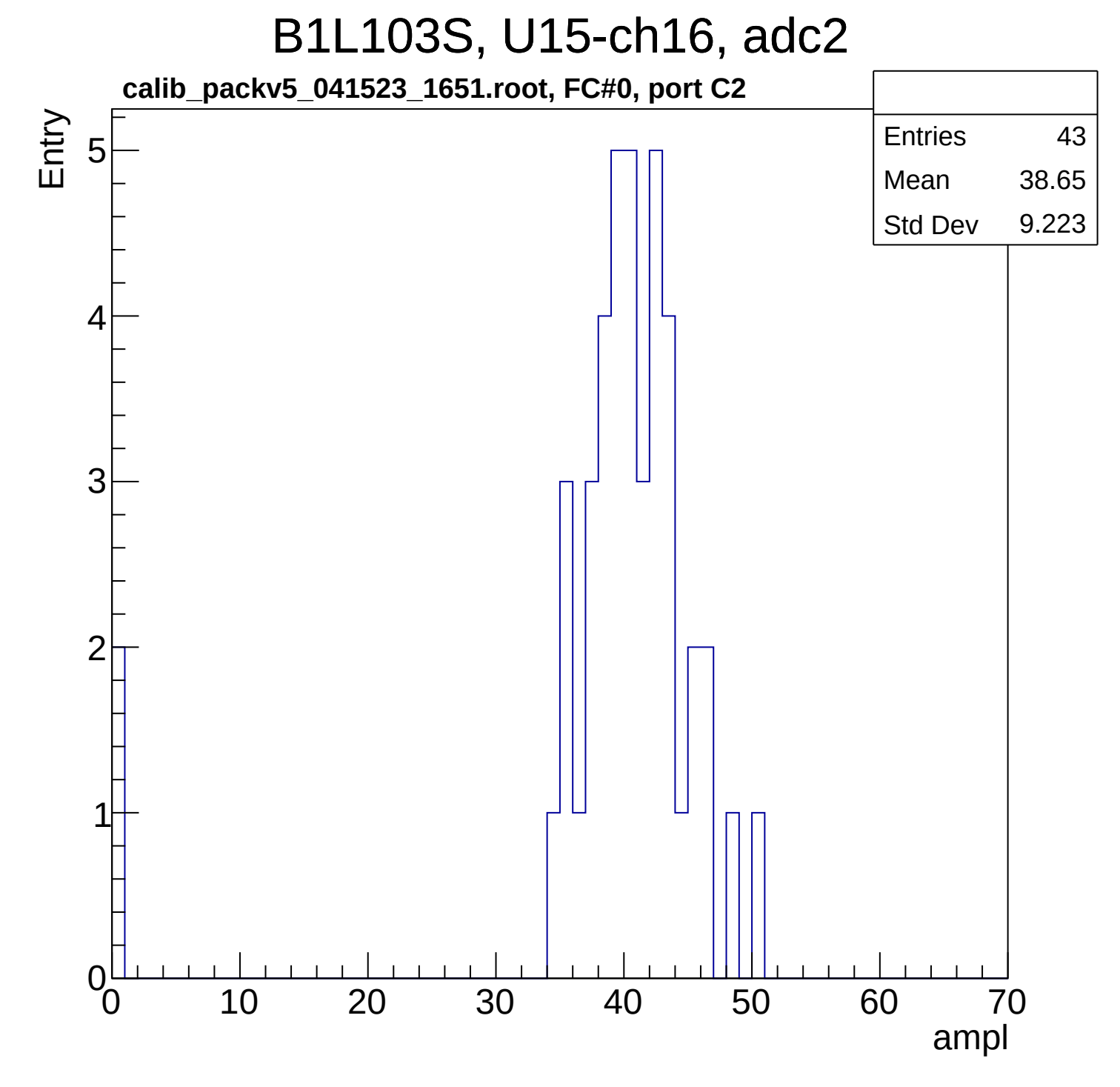
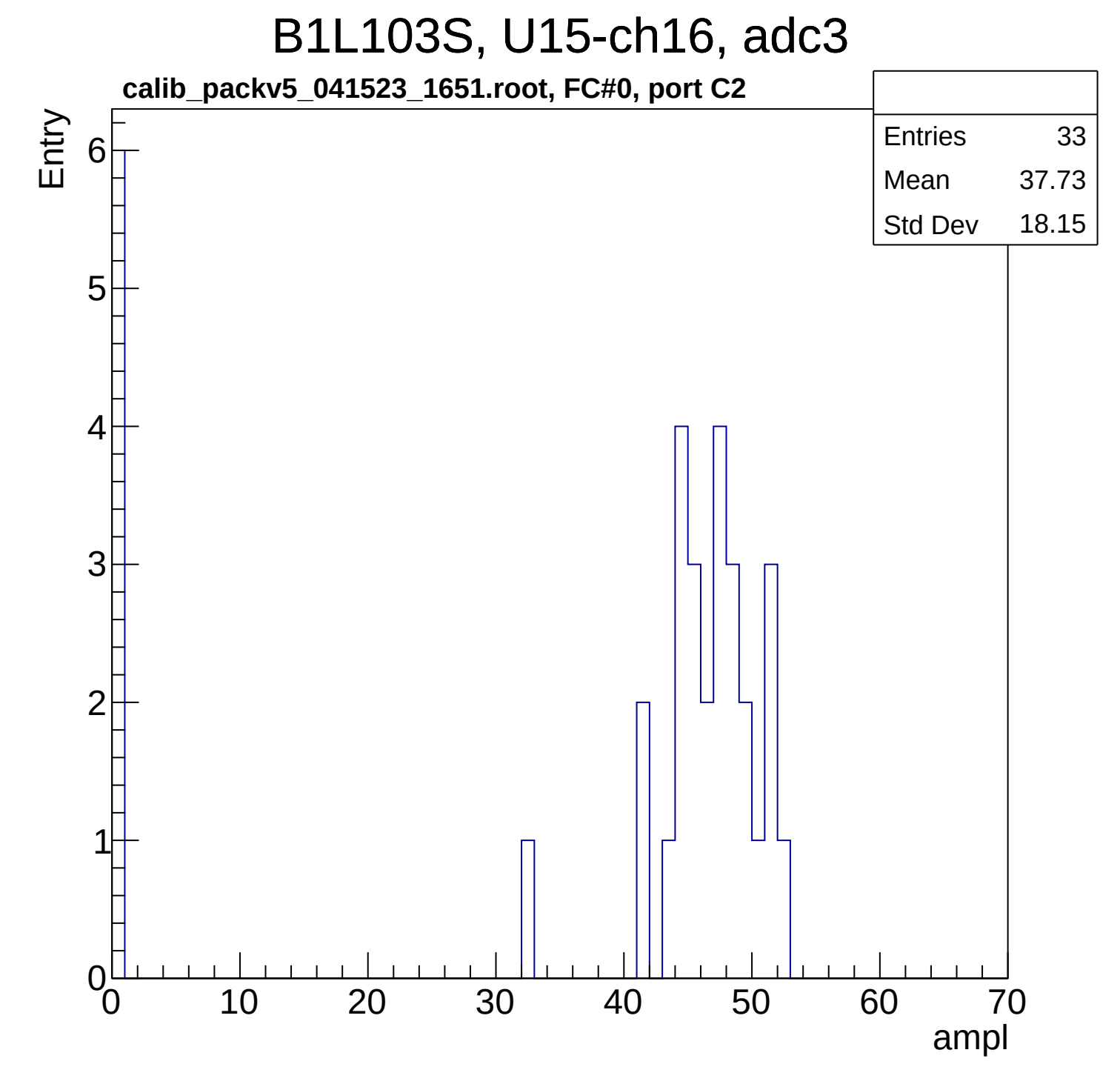
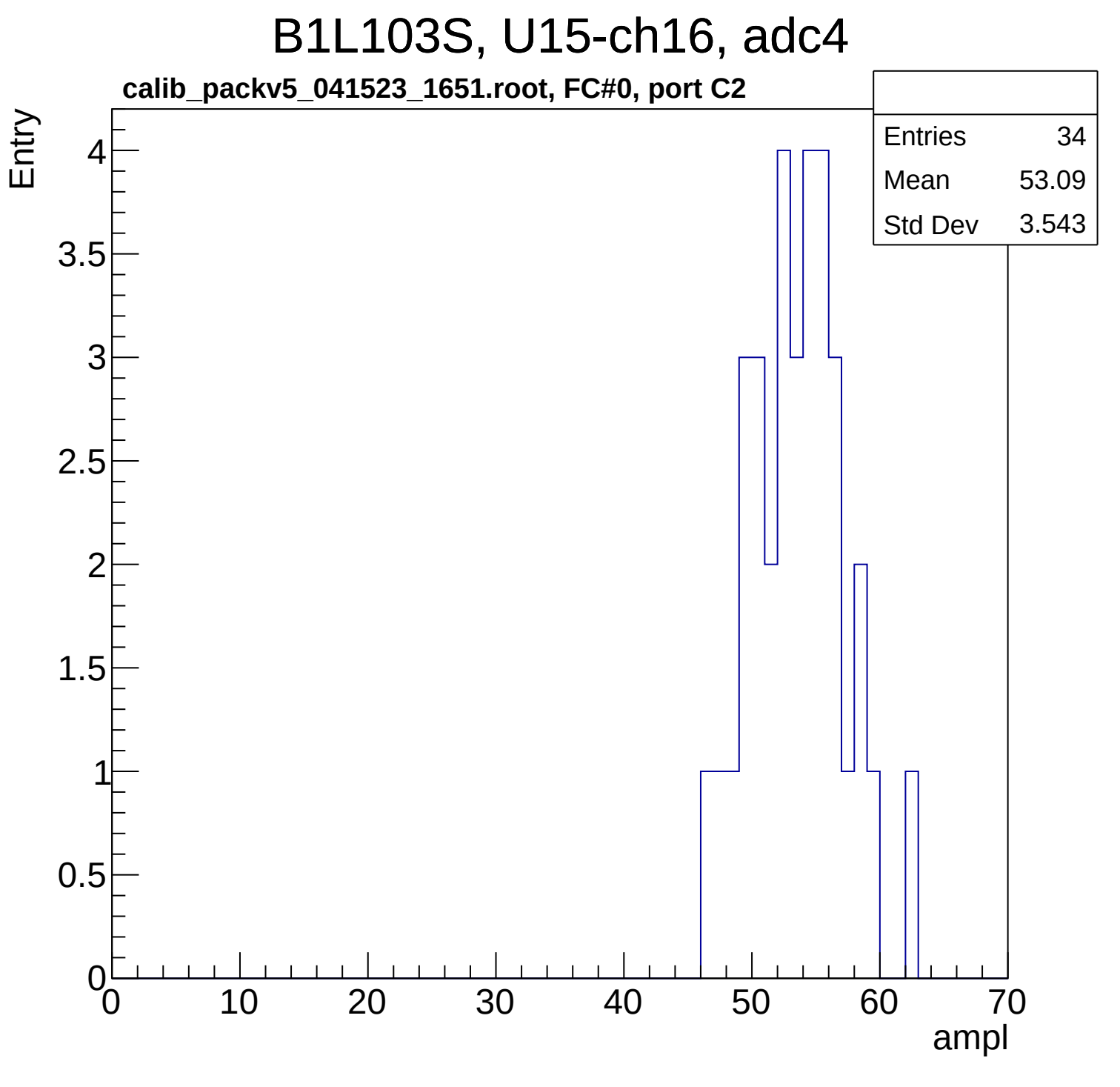
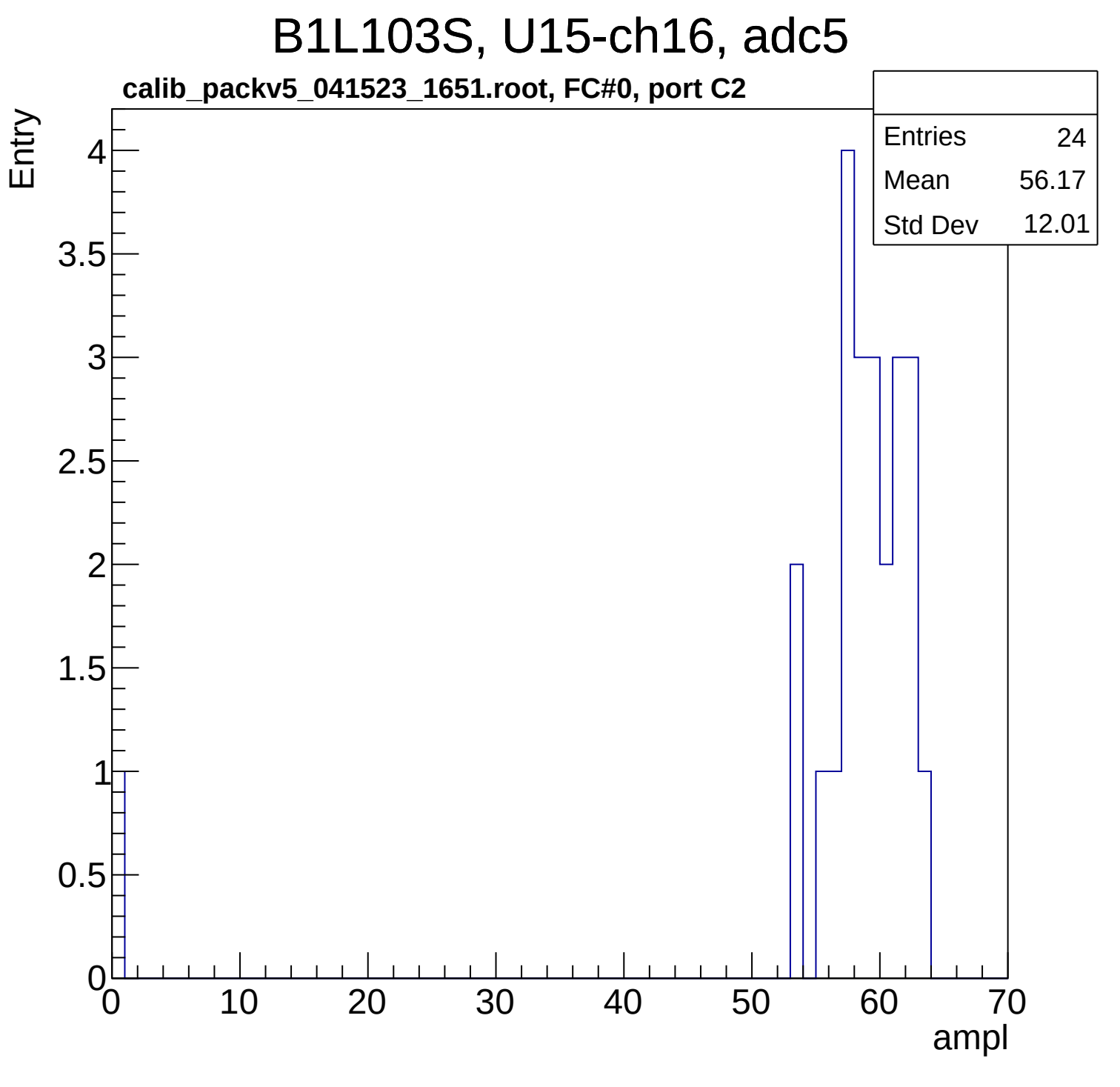
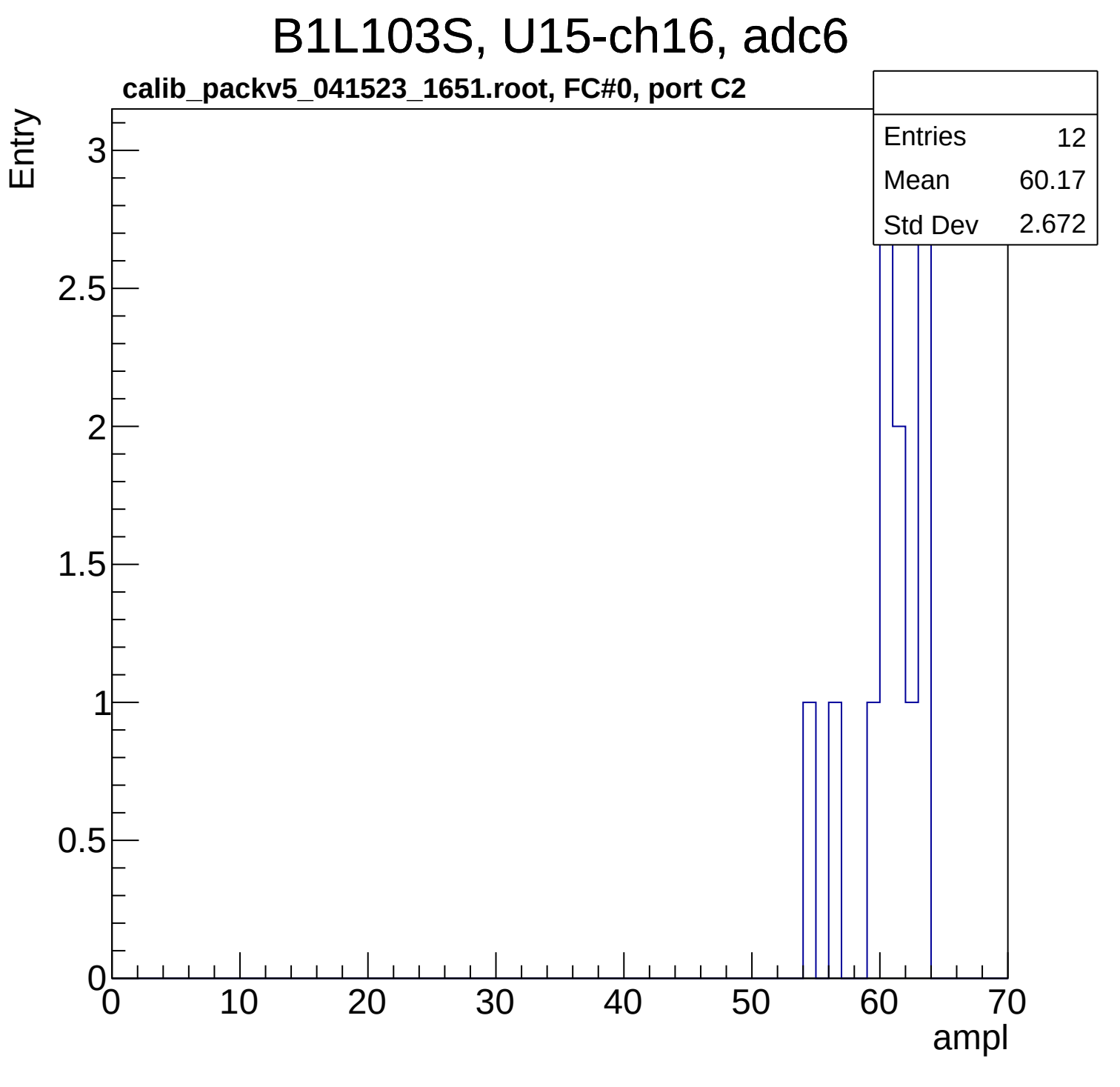
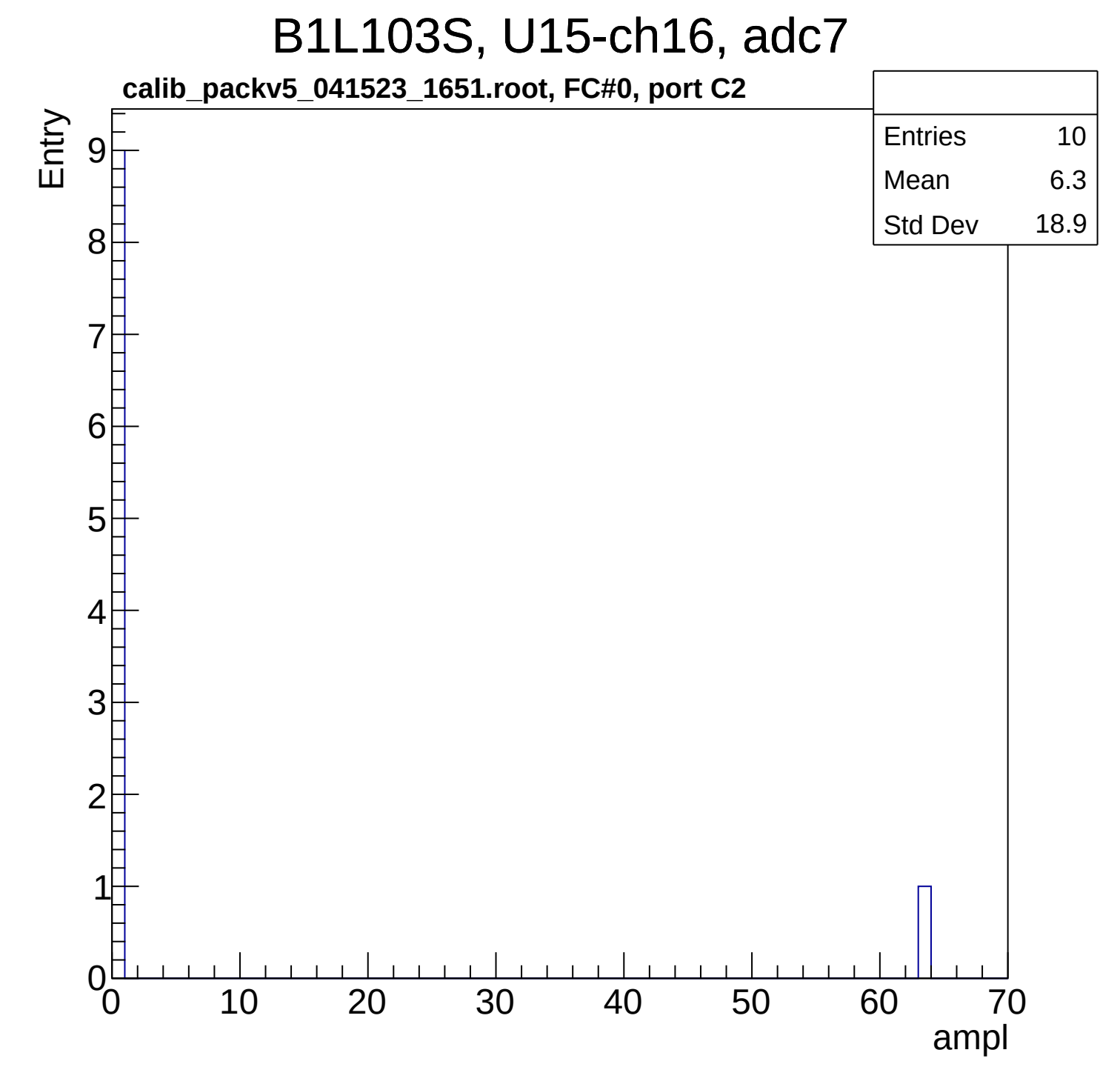

B1L103S, U15-ch16, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 38.65
Std Dev 9.223
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

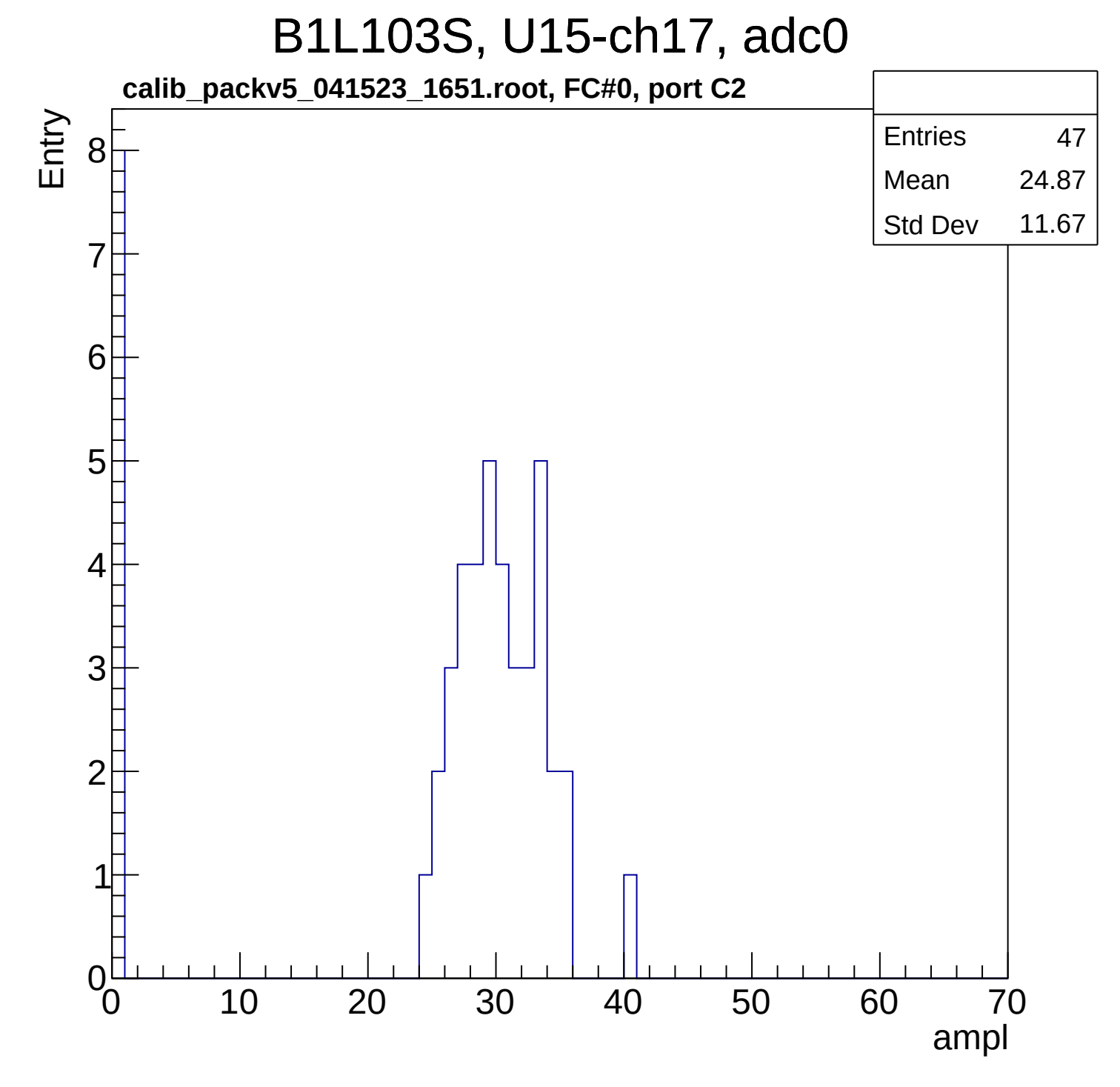

B1L103S, U15-ch16, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 37.73
Std Dev 18.15
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

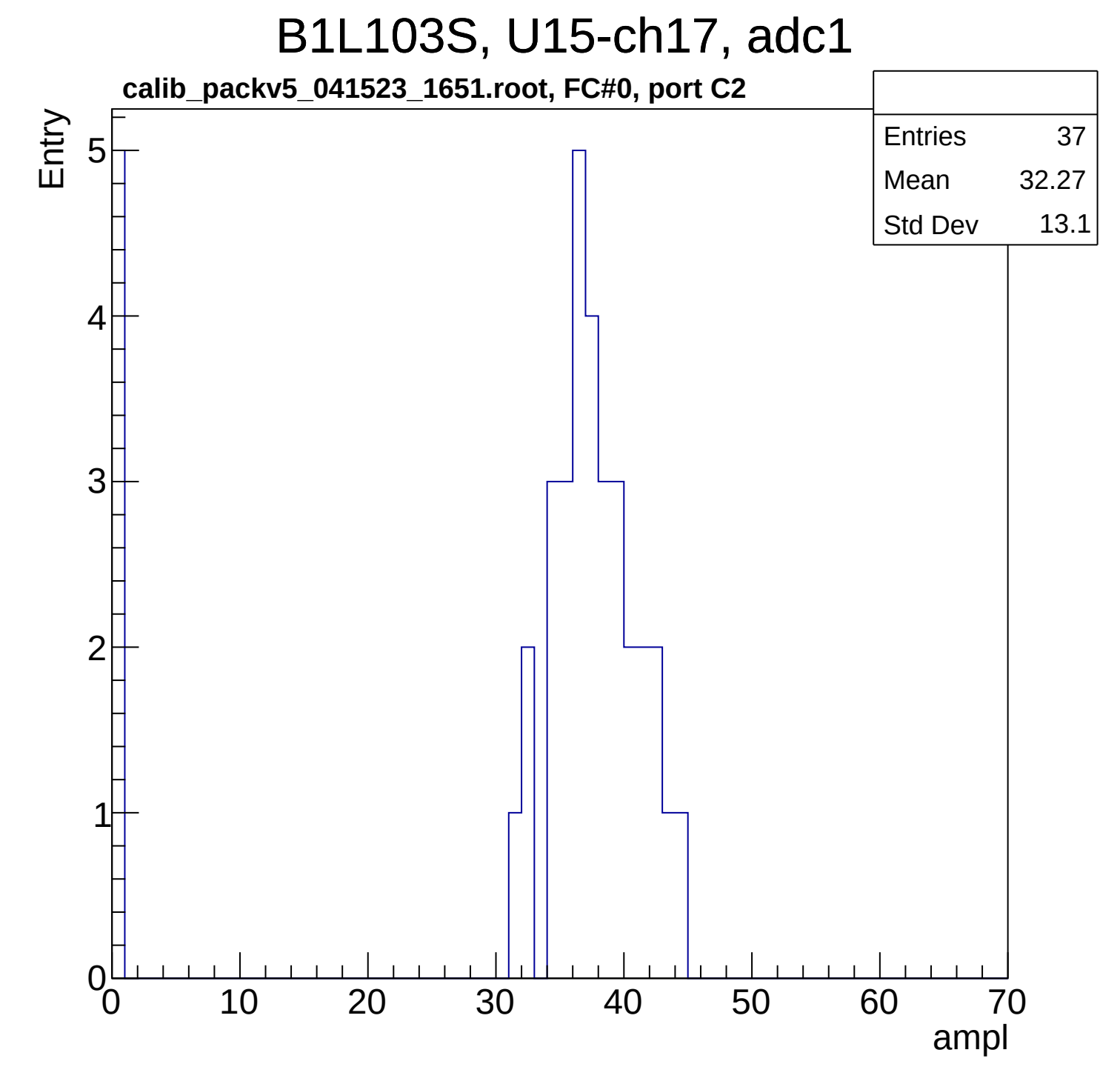

B1L103S, U15-ch16, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 53.09
Std Dev 3.543
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

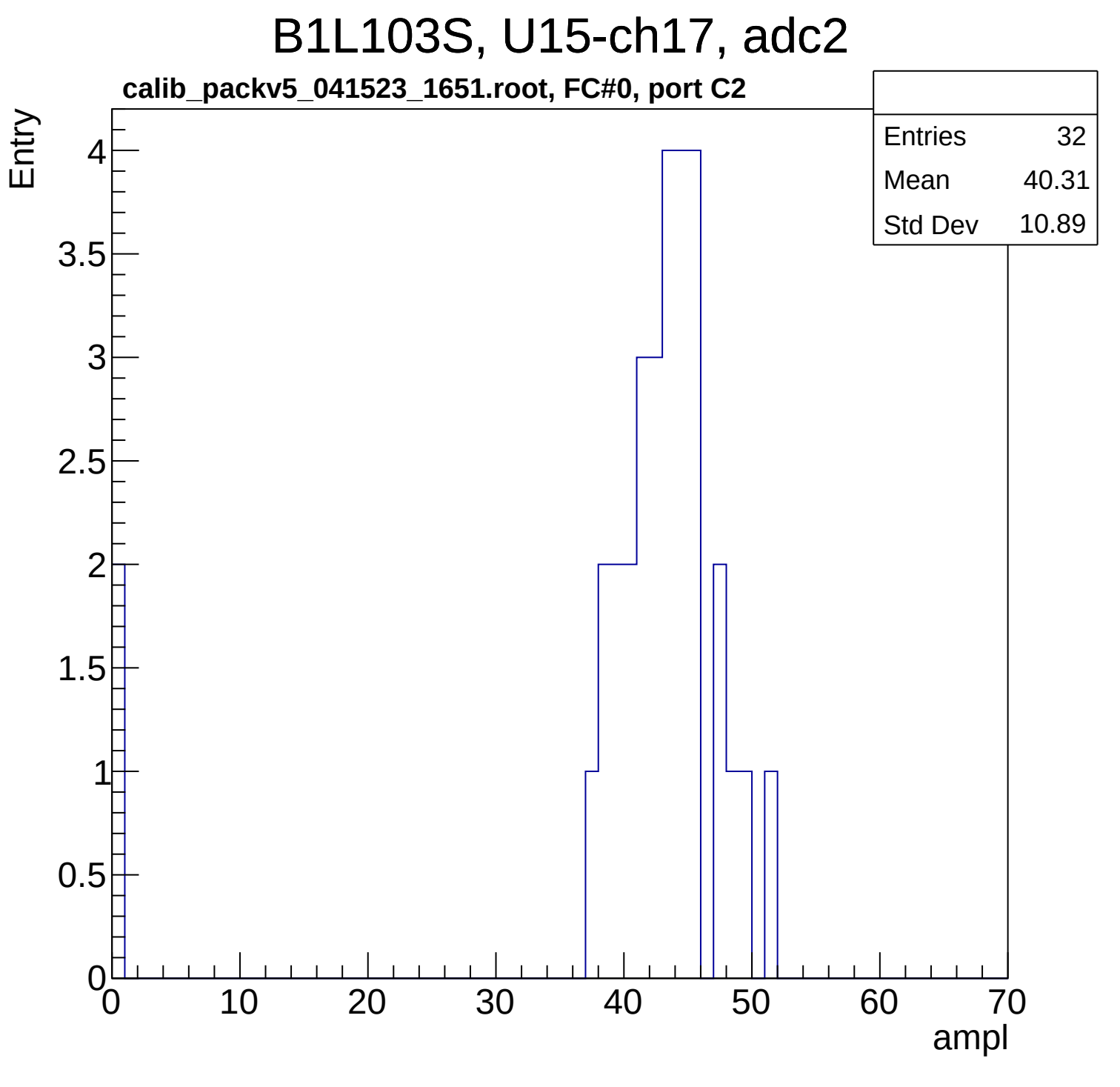

B1L103S, U15-ch16, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 56.17
Std Dev 12.01
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

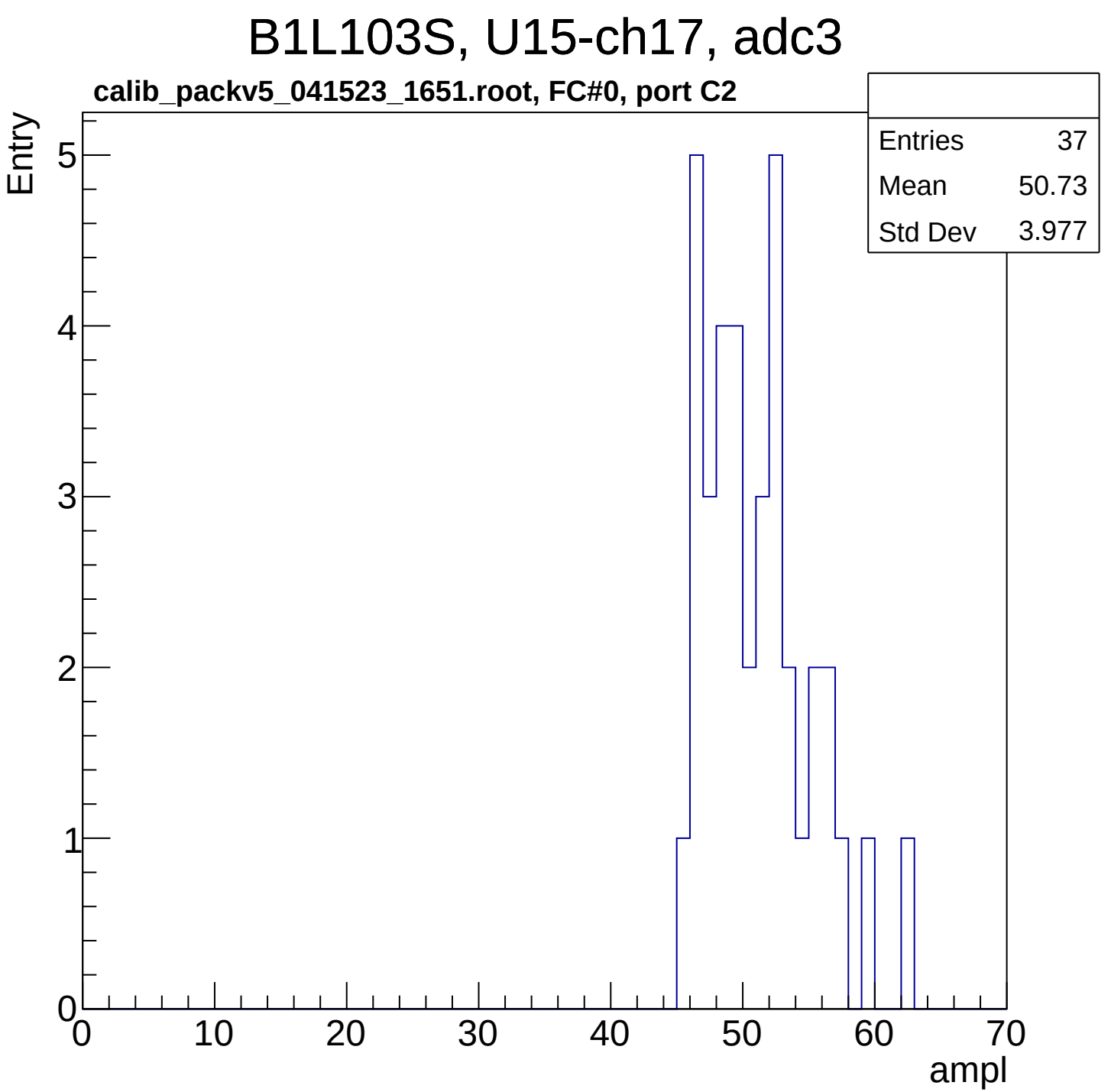

B1L103S, U15-ch16, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 60.17
Std Dev 2.672
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

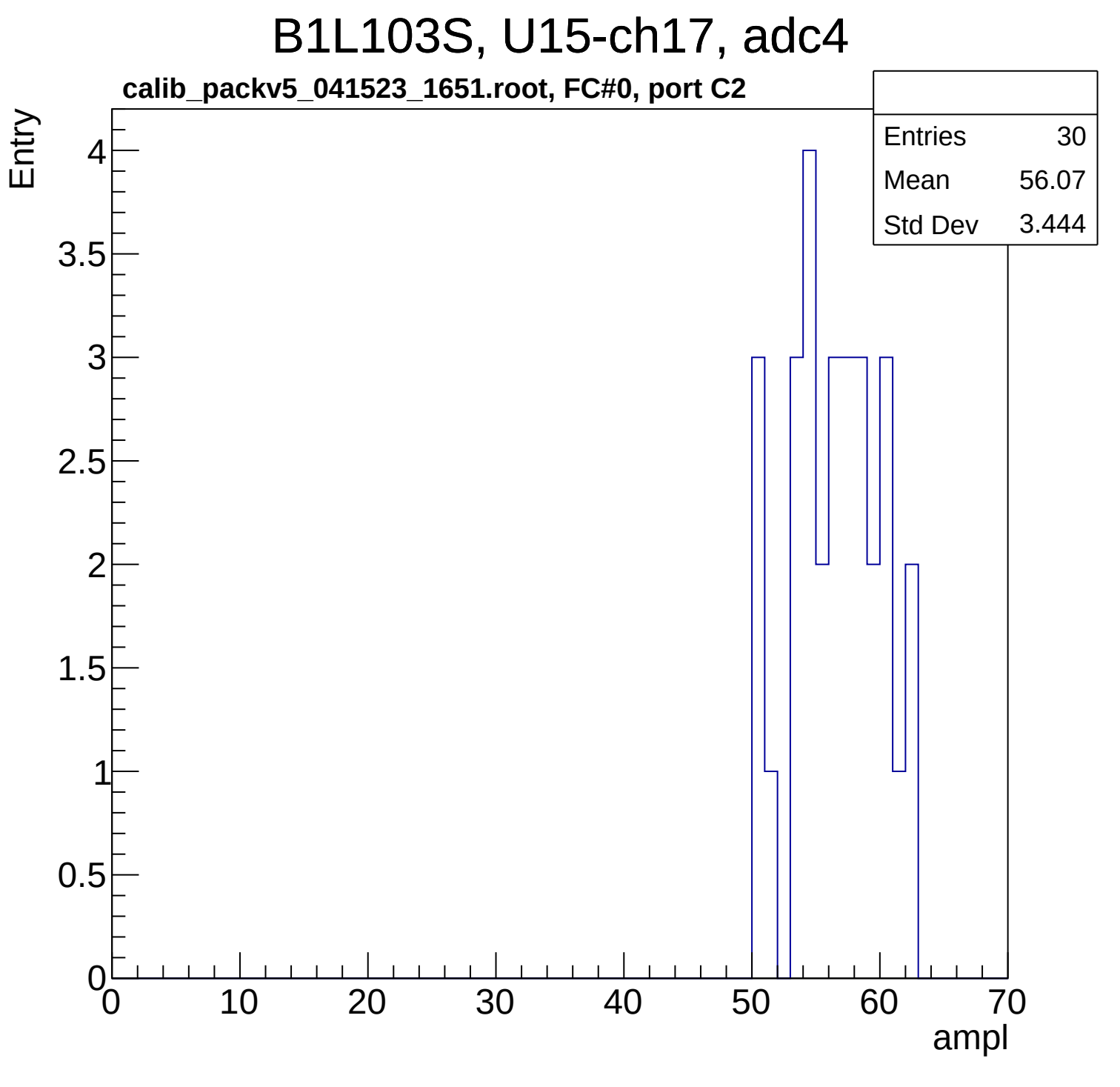

B1L103S, U15-ch16, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 6.3
Std Dev 18.9
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

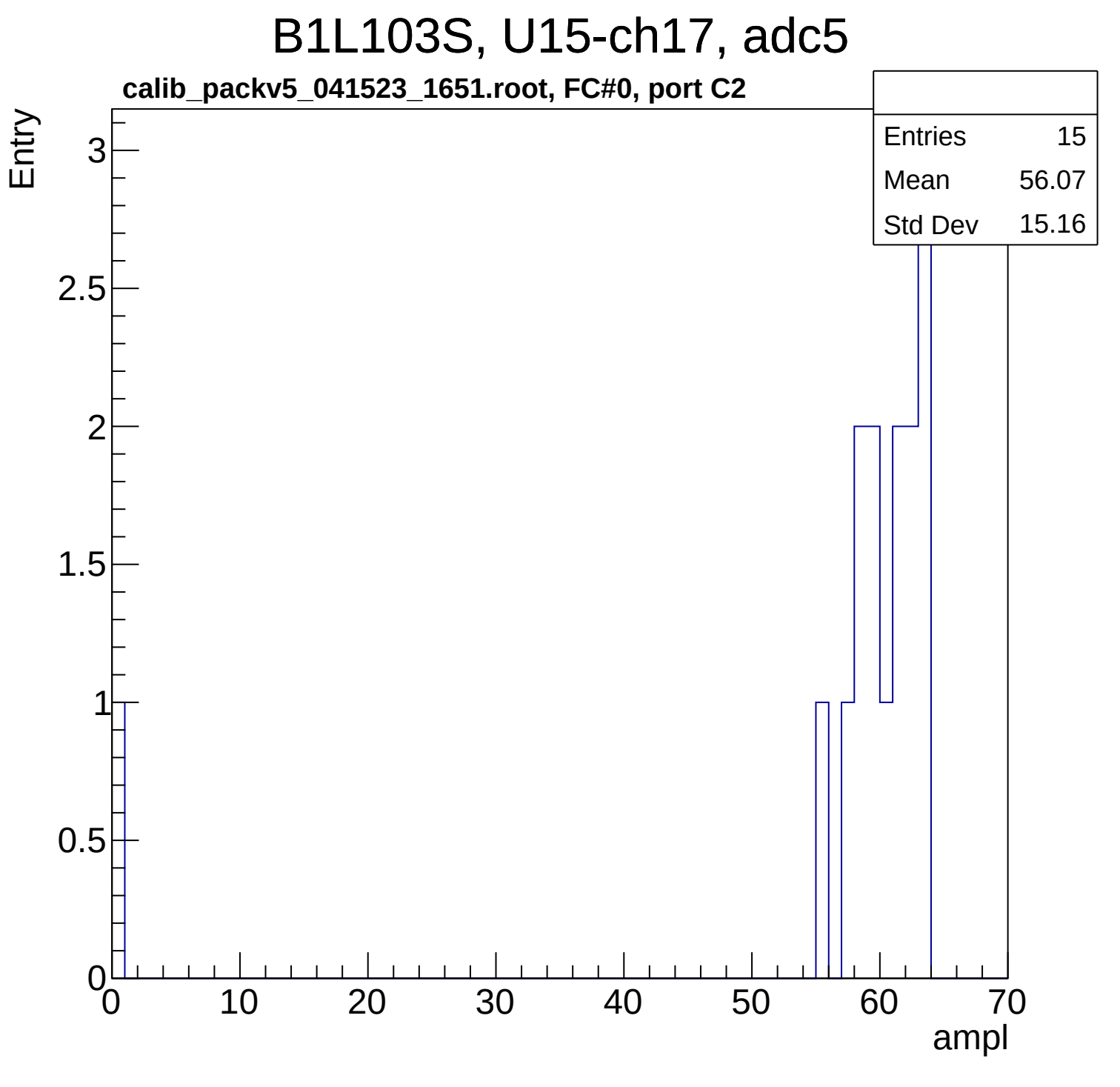

B1L103S, U15-ch17, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 24.87
Std Dev 11.67
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

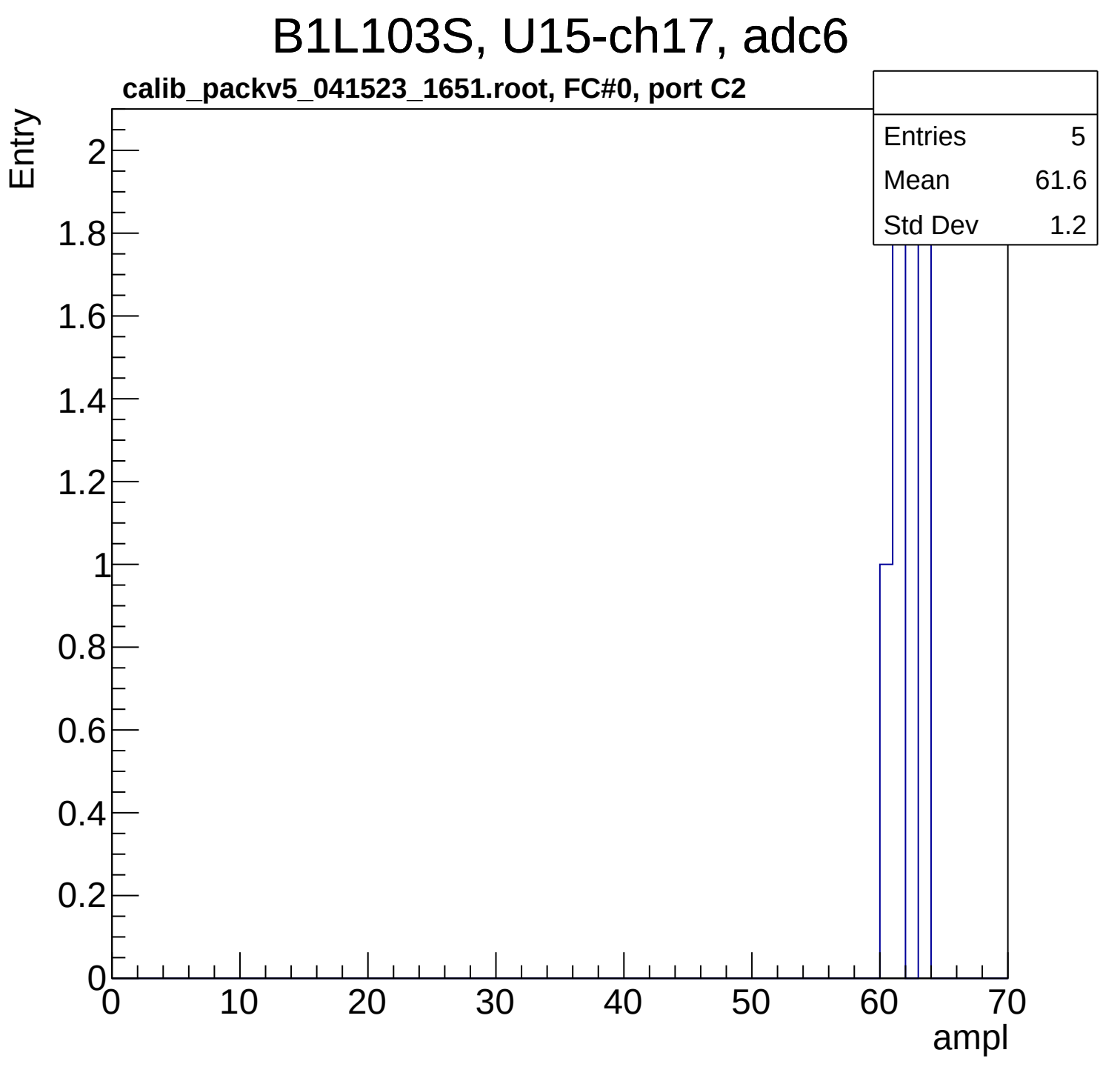

B1L103S, U15-ch17, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 32.27
Std Dev 13.1
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

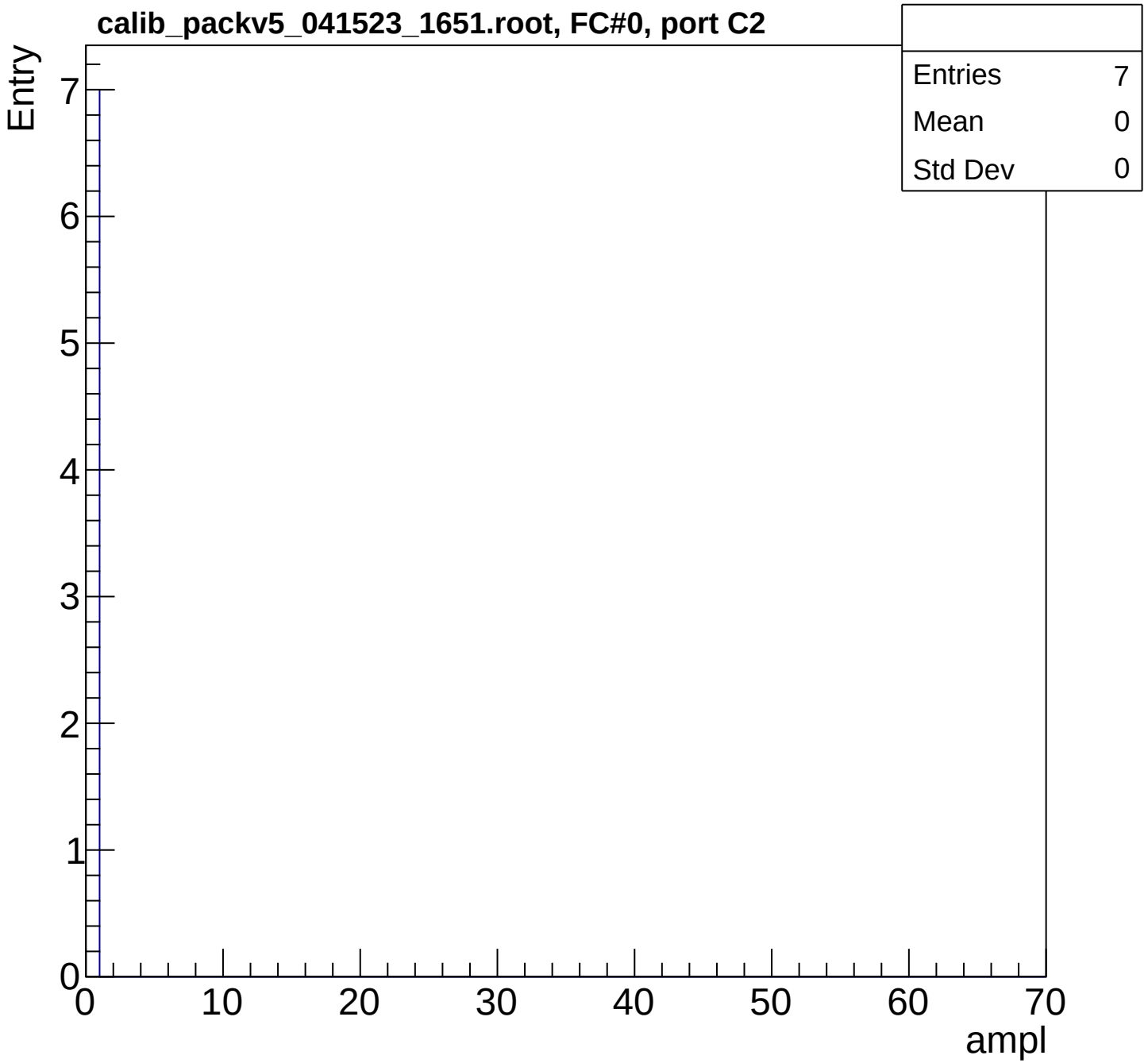

B1L103S, U15-ch17, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 40.31
Std Dev 10.89
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

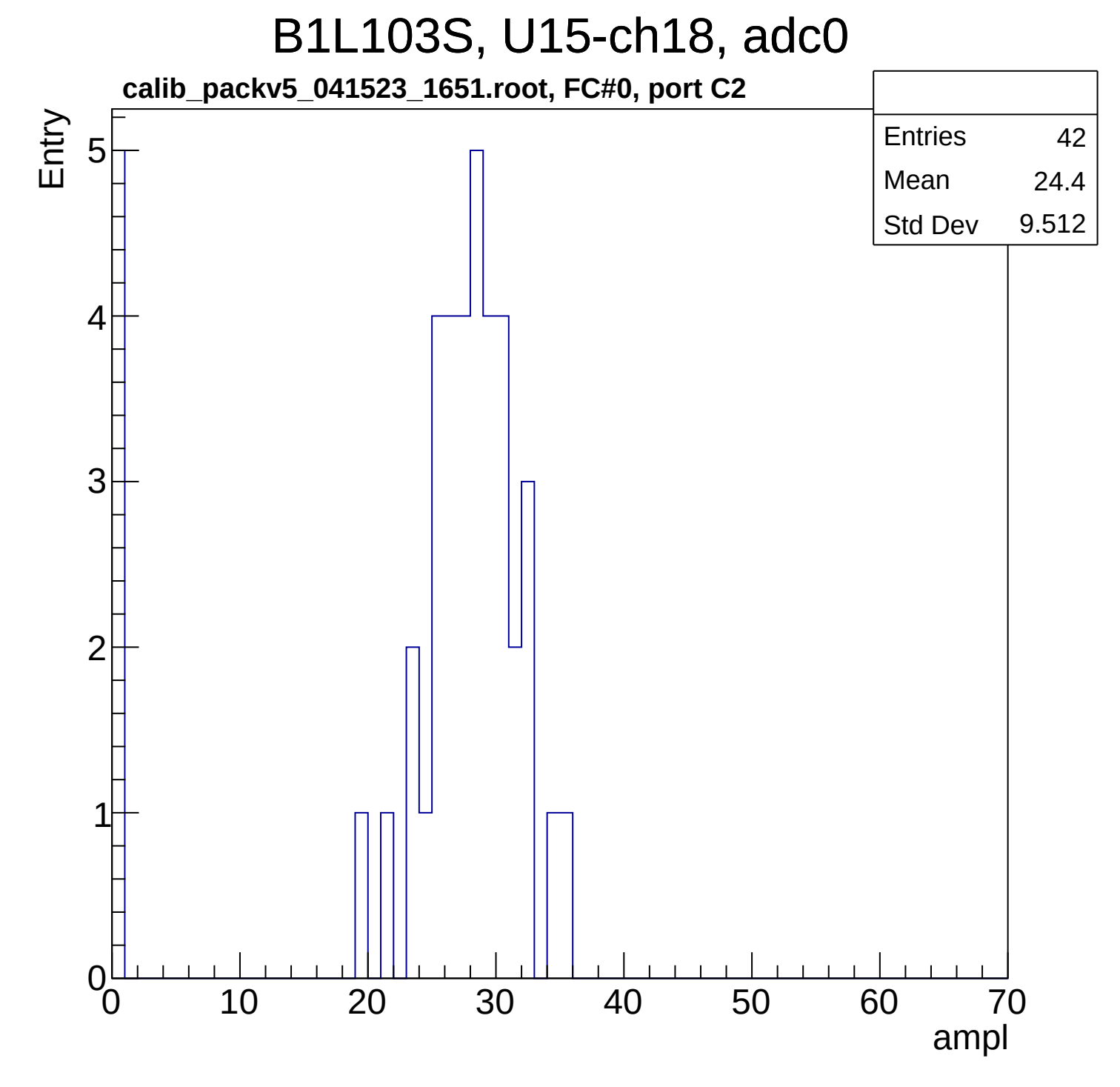

B1L103S, U15-ch17, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 50.73
Std Dev 3.977
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

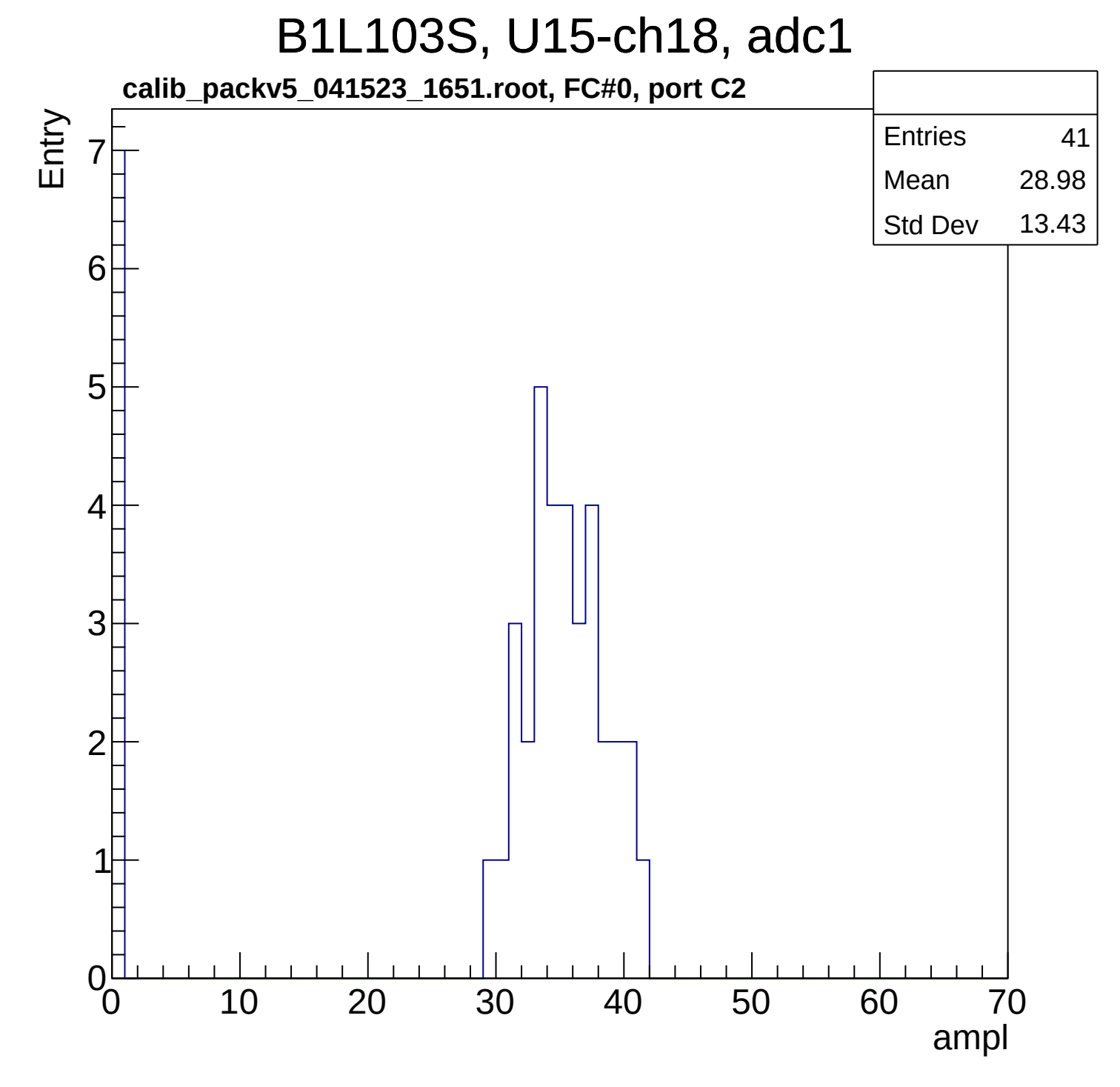

B1L103S, U15-ch17, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 56.07
Std Dev 3.444
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

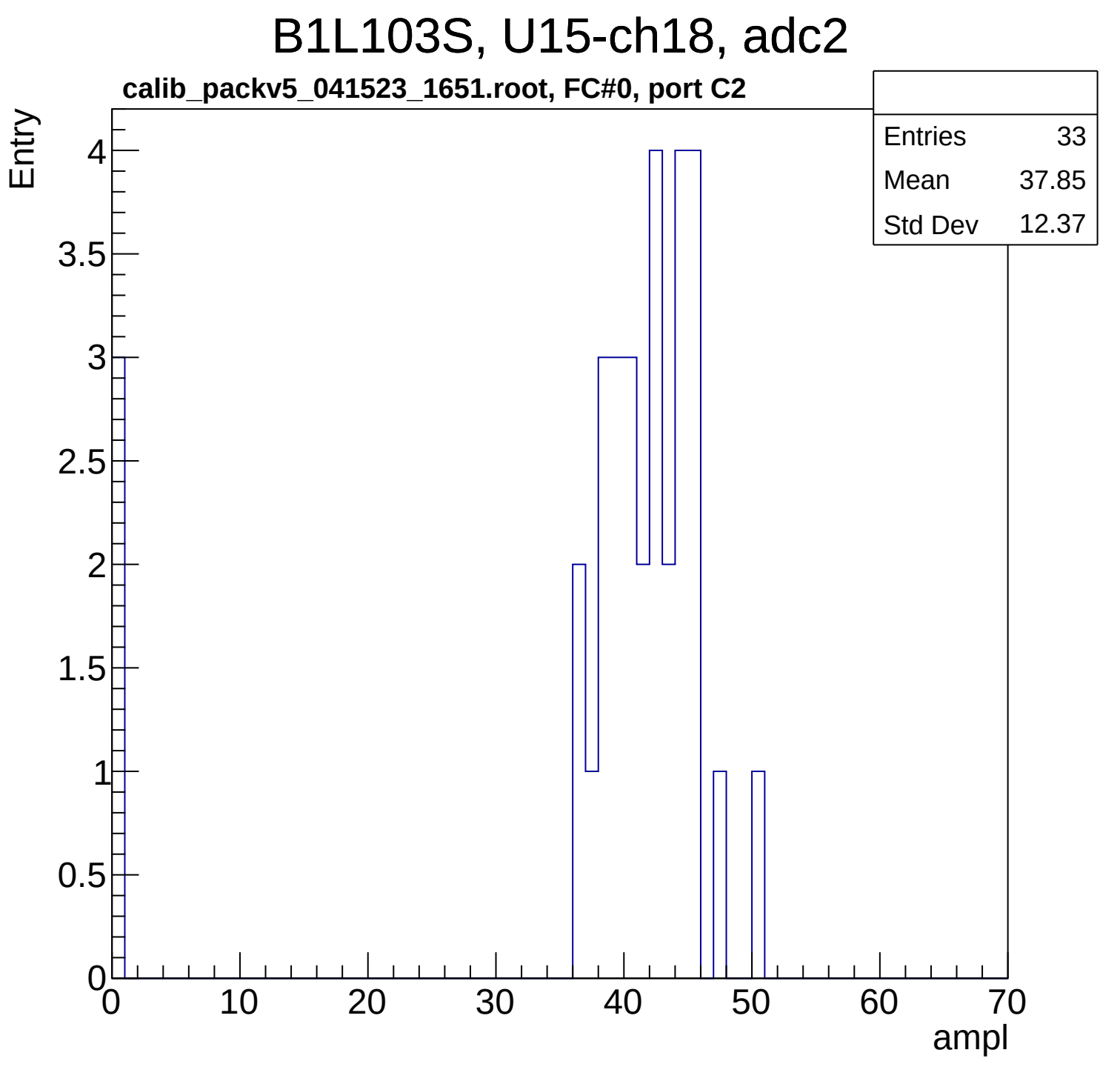

B1L103S, U15-ch17, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 56.07
Std Dev 15.16
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

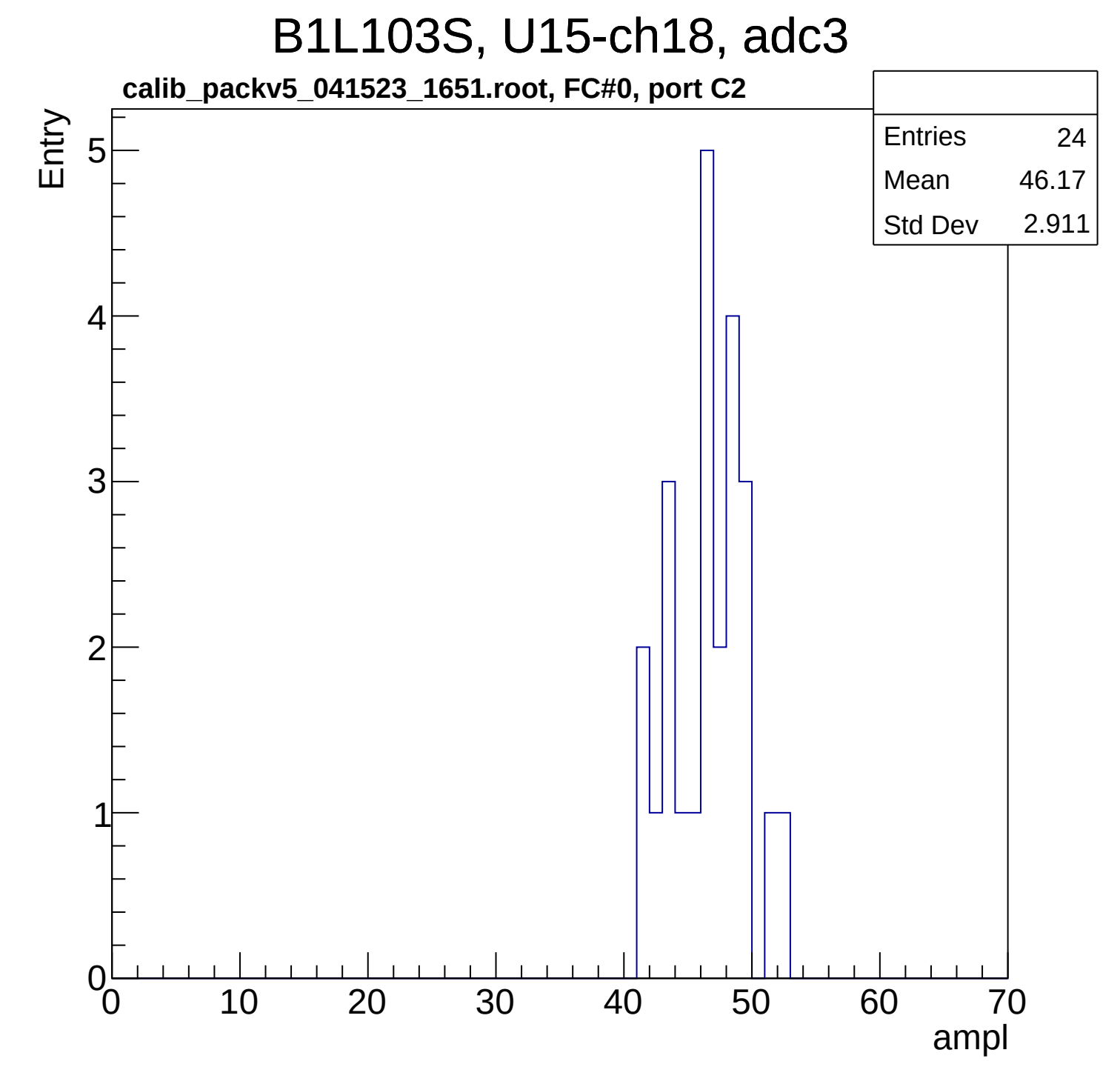

B1L103S, U15-ch17, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.6
Std Dev 1.2
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

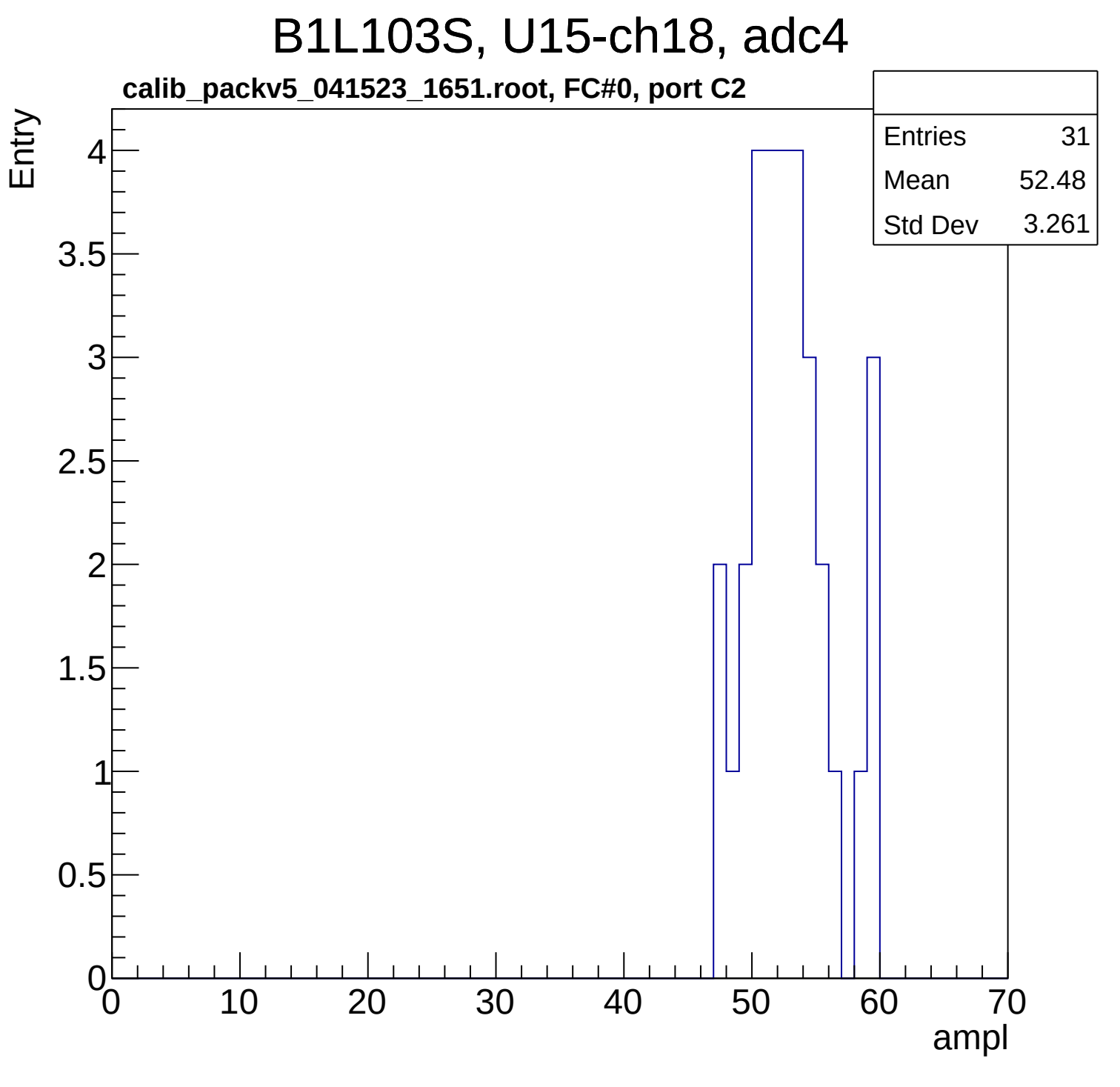

B1L103S, U15-ch17, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 0
Std Dev 0
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

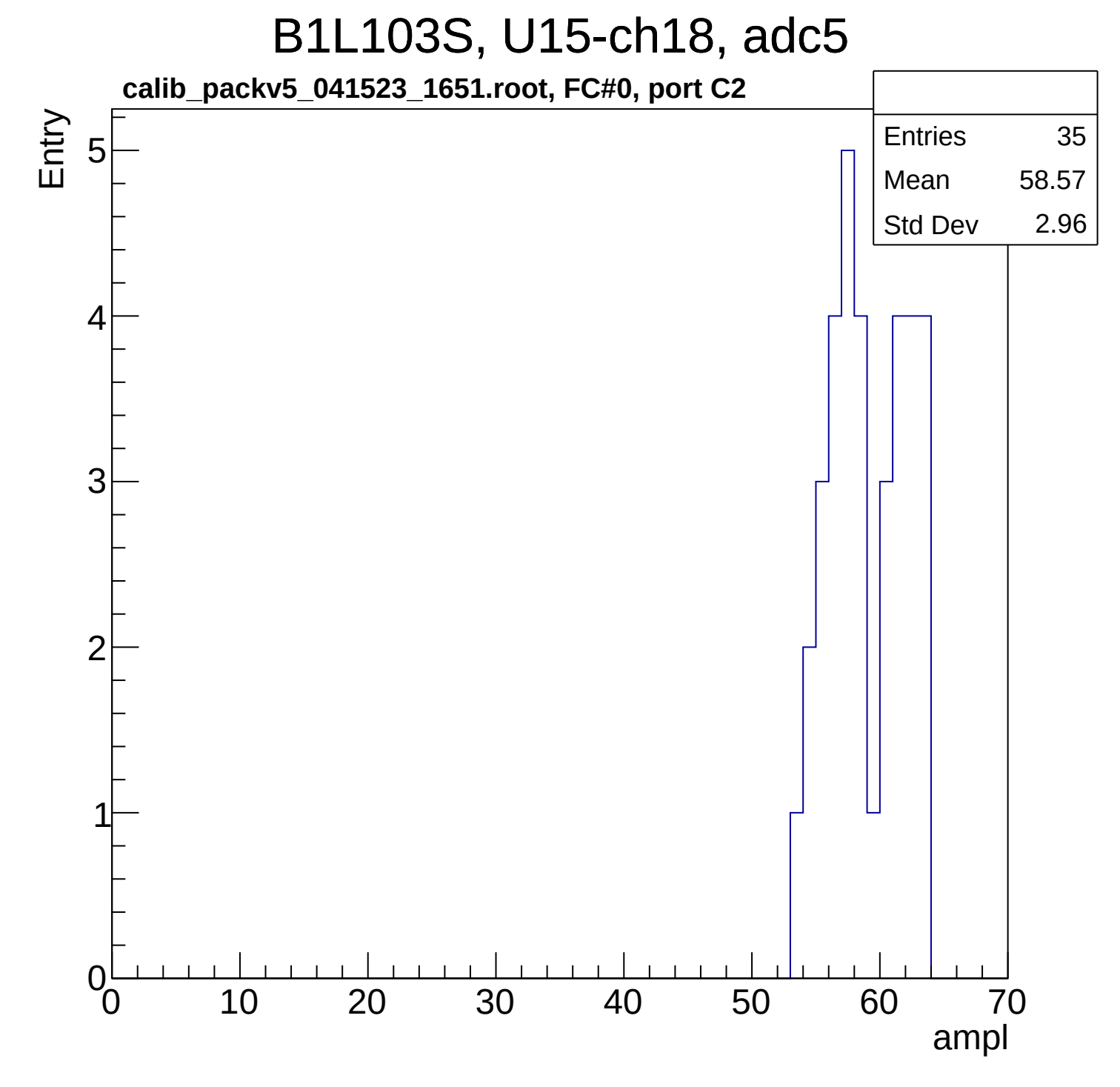

B1L103S, U15-ch18, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 24.4
Std Dev 9.512
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

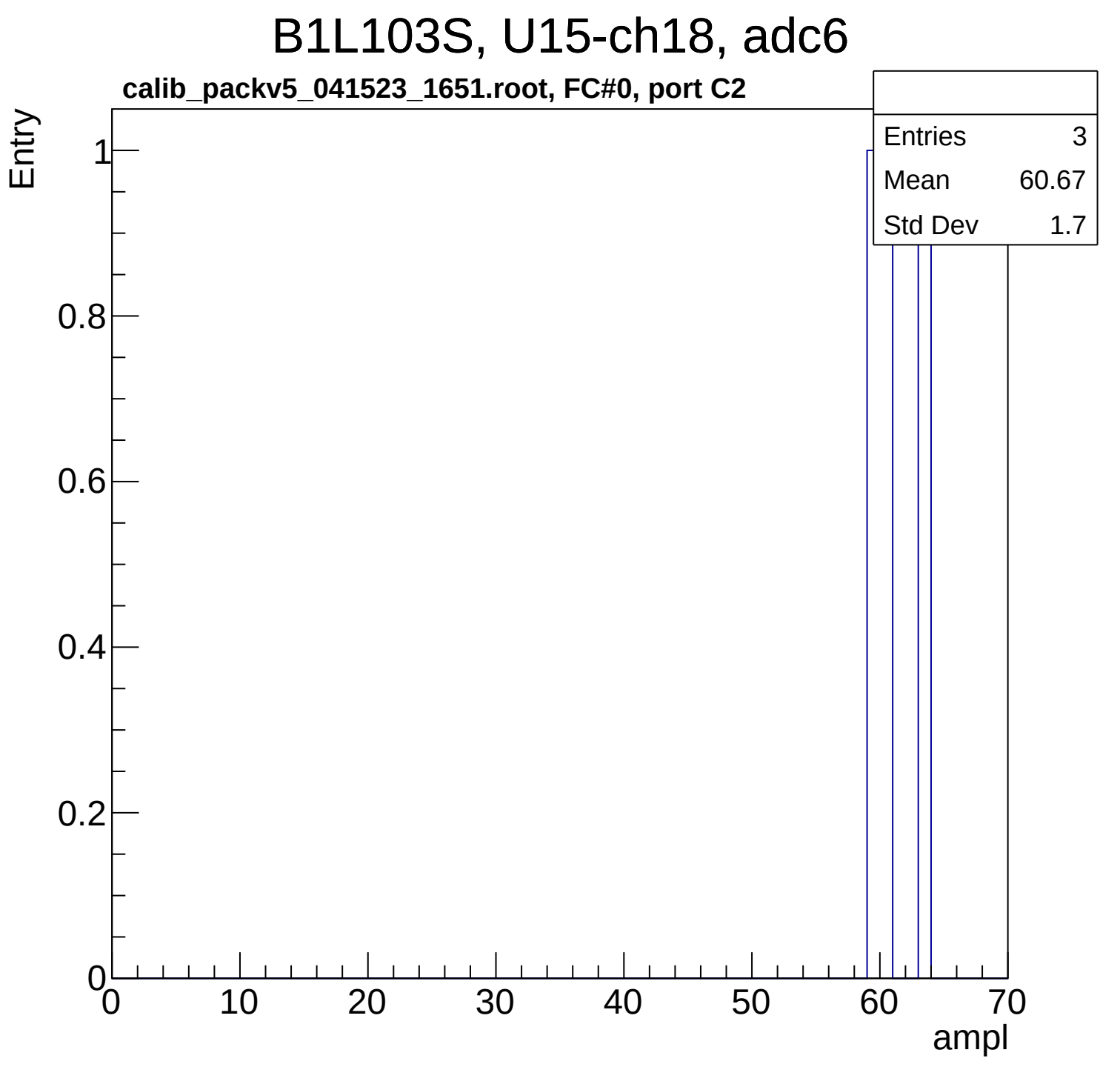

B1L103S, U15-ch18, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 28.98
Std Dev 13.43
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

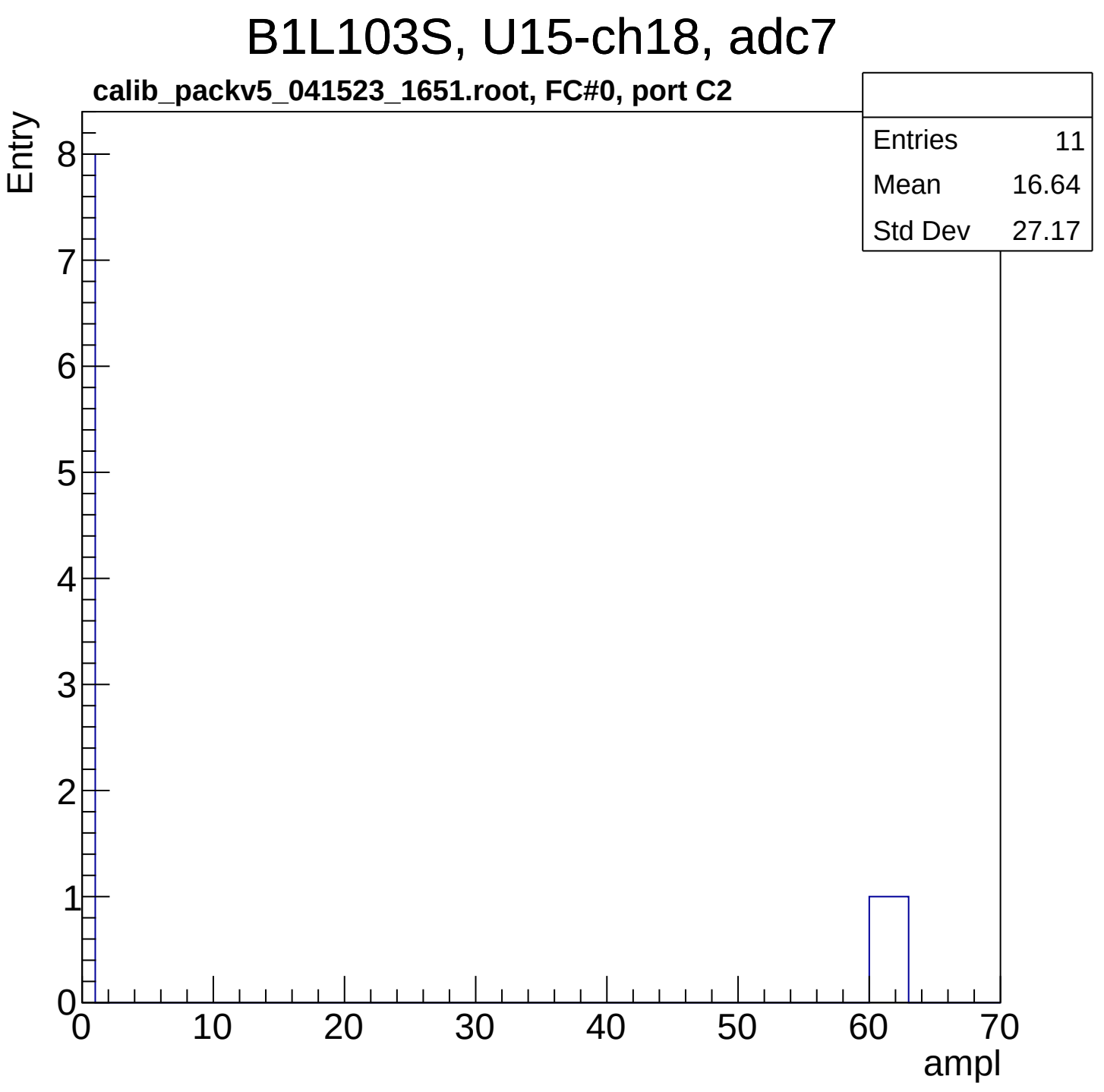

B1L103S, U15-ch18, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 37.85
Std Dev 12.37
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

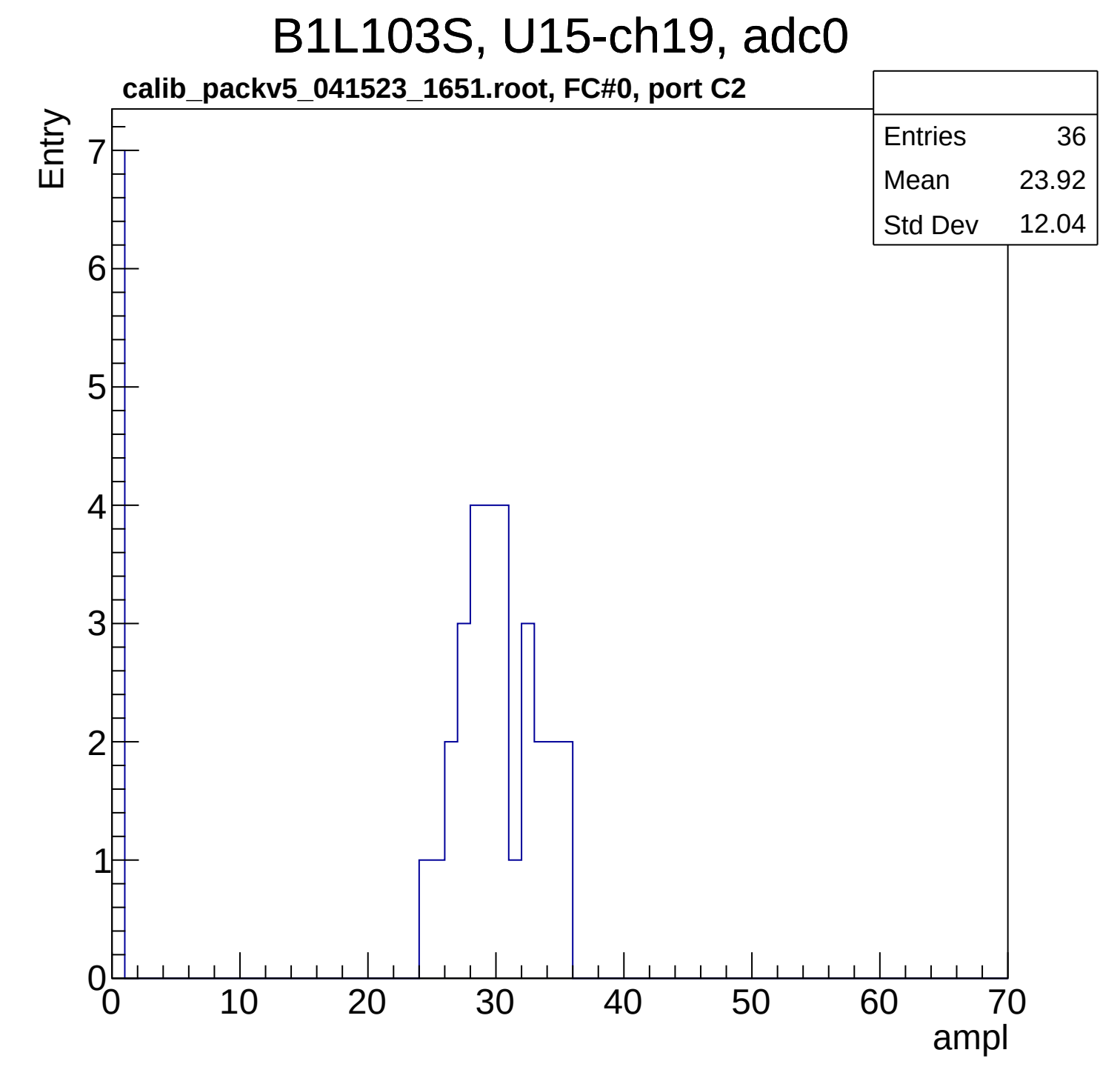

B1L103S, U15-ch18, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 46.17
Std Dev 2.911
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

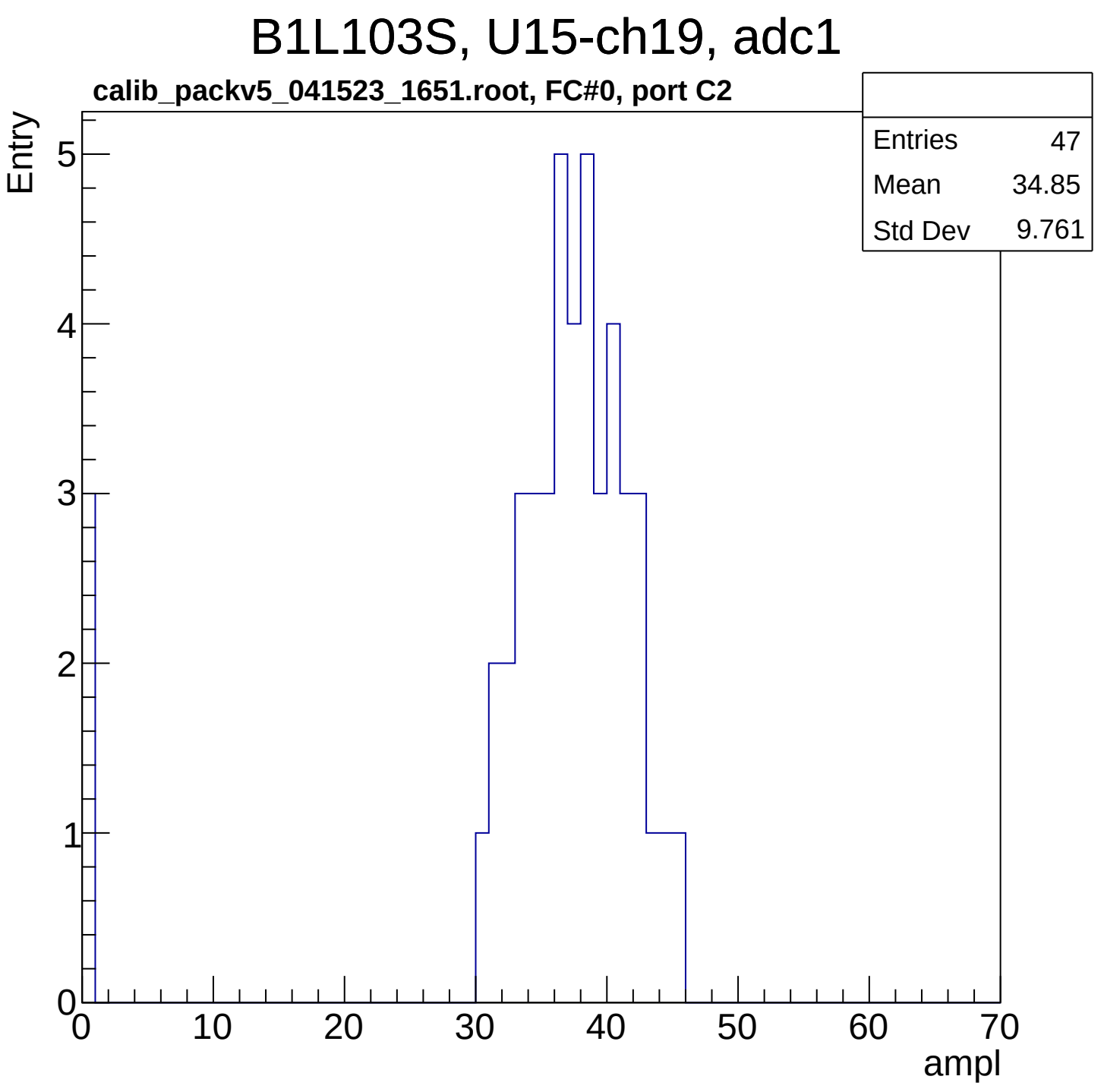

B1L103S, U15-ch18, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 52.48
Std Dev 3.261
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

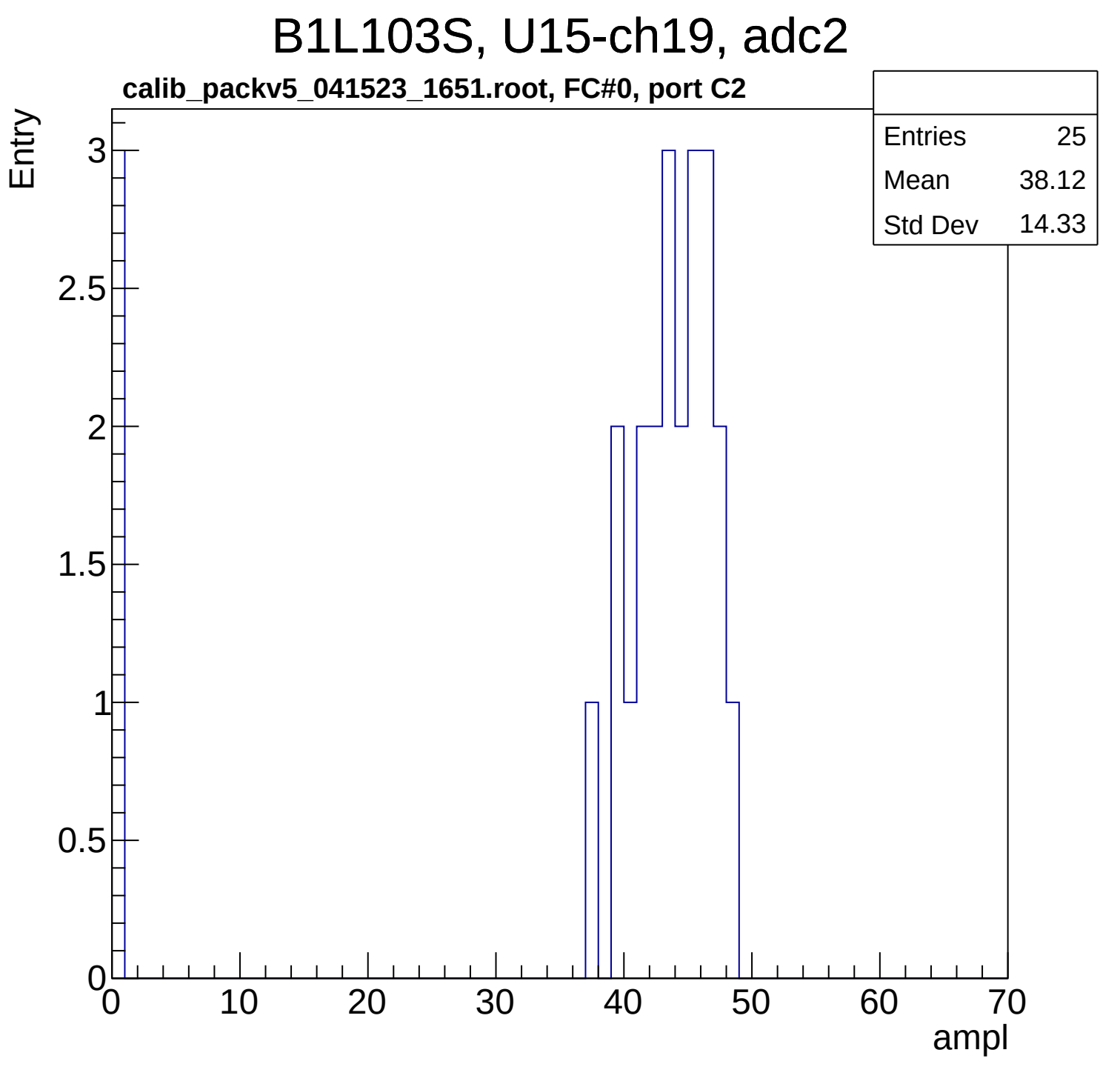

B1L103S, U15-ch18, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 58.57
Std Dev 2.96
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch18, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 60.67
Std Dev 1.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L103S, U15-ch18, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 16.64
Std Dev 27.17
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch19, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 23.92
Std Dev 12.04
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U15-ch19, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 34.85
Std Dev 9.761
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch19, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 38.12
Std Dev 14.33
Entry
ampl
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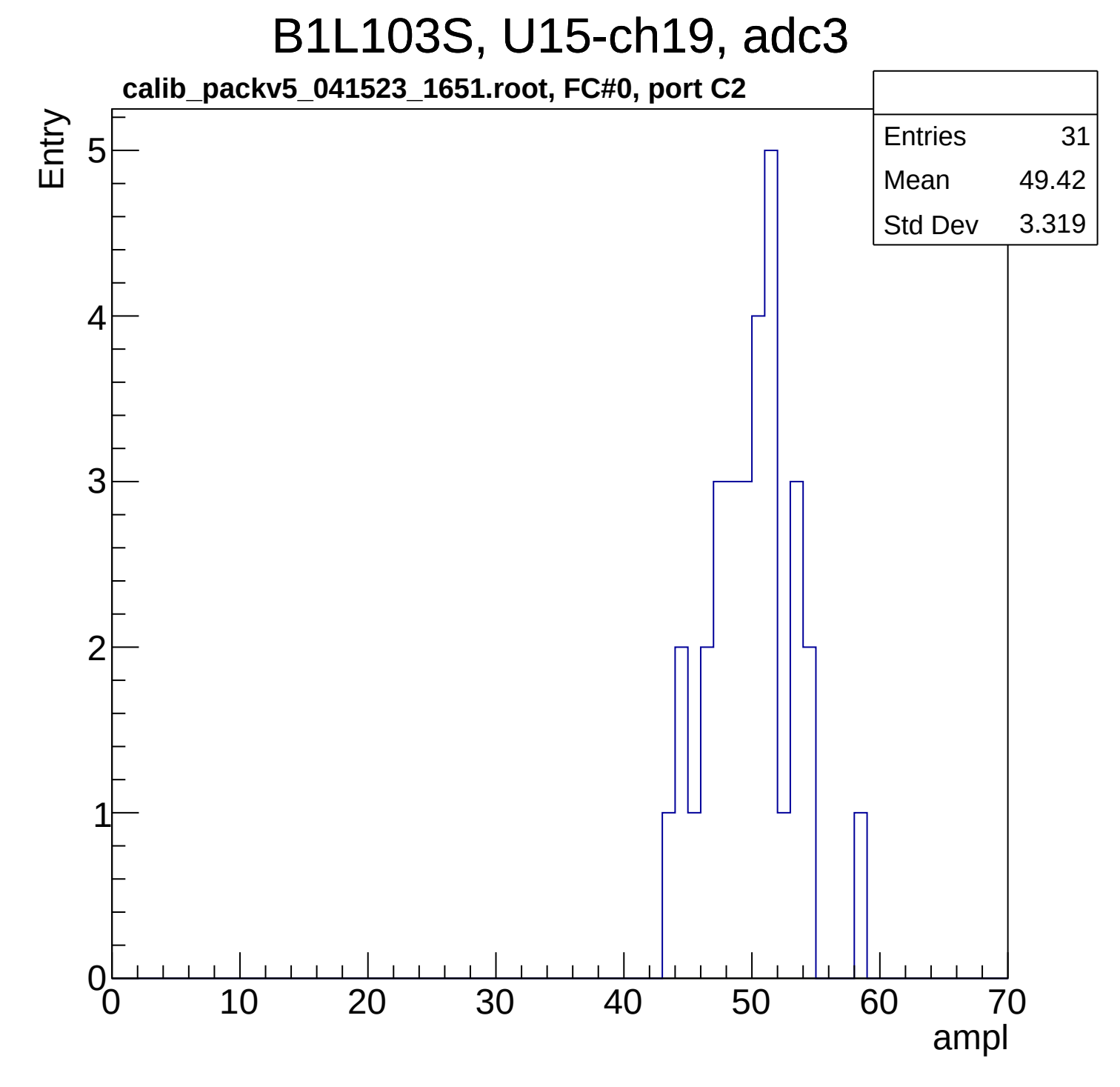
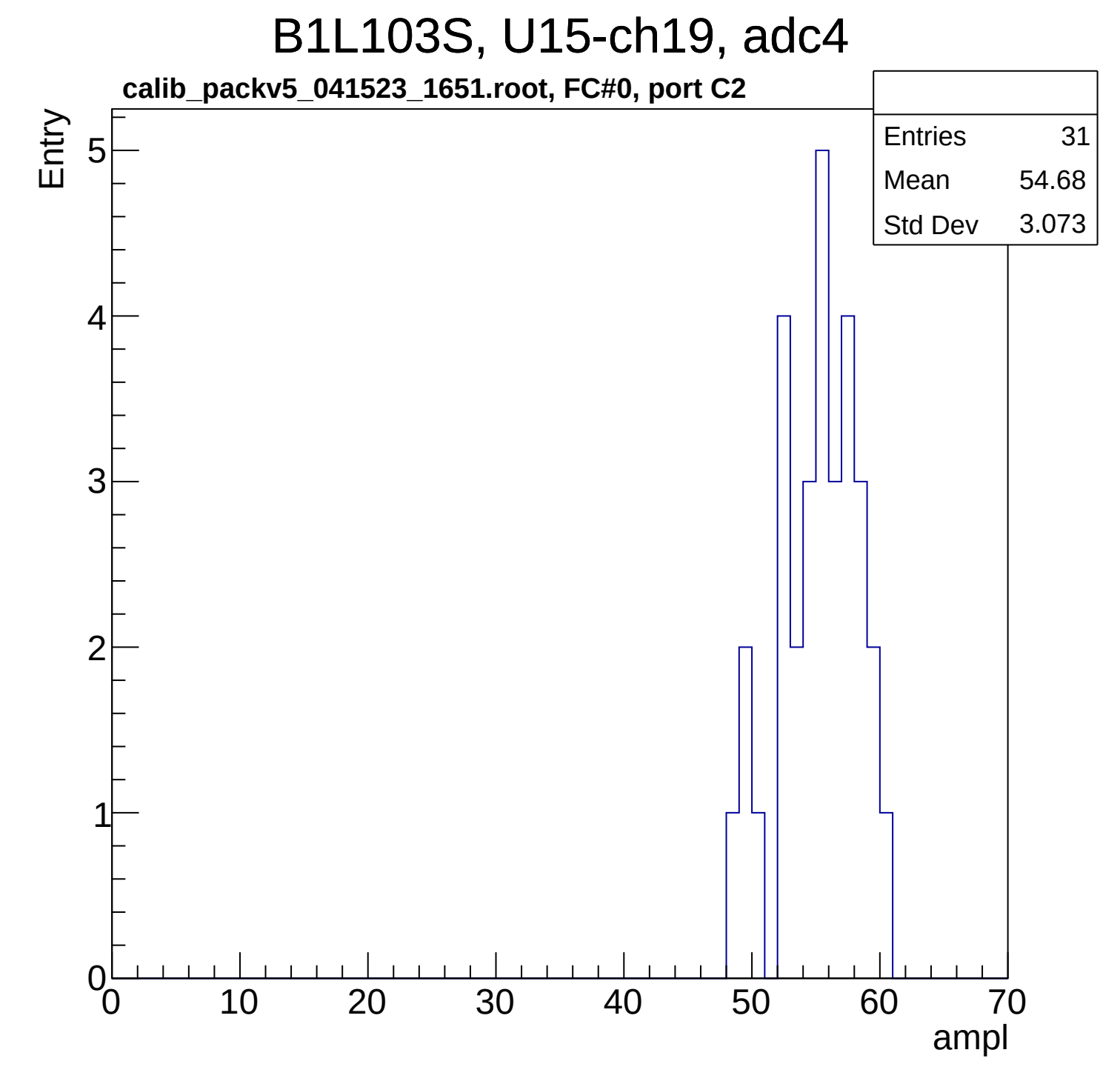
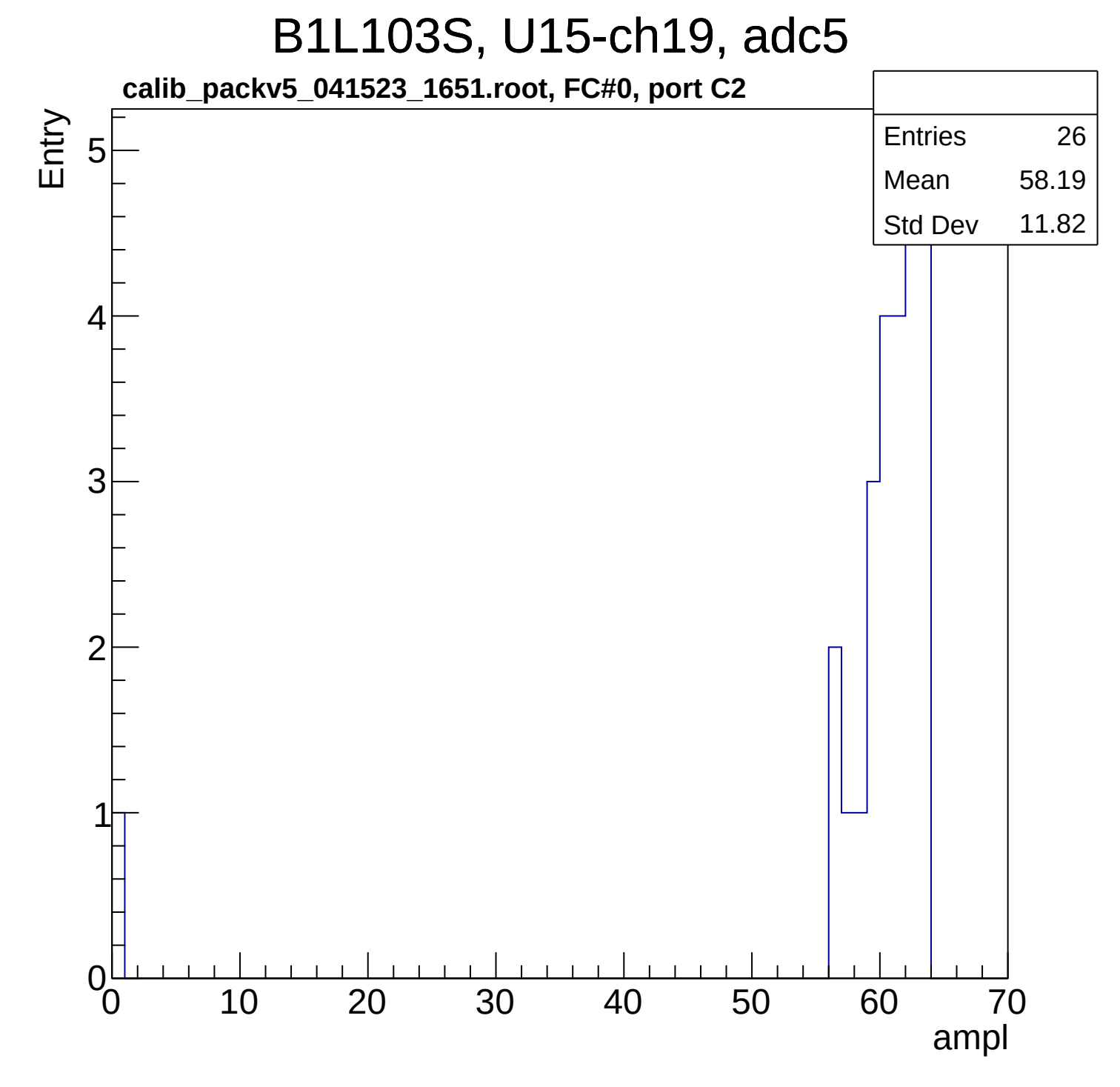
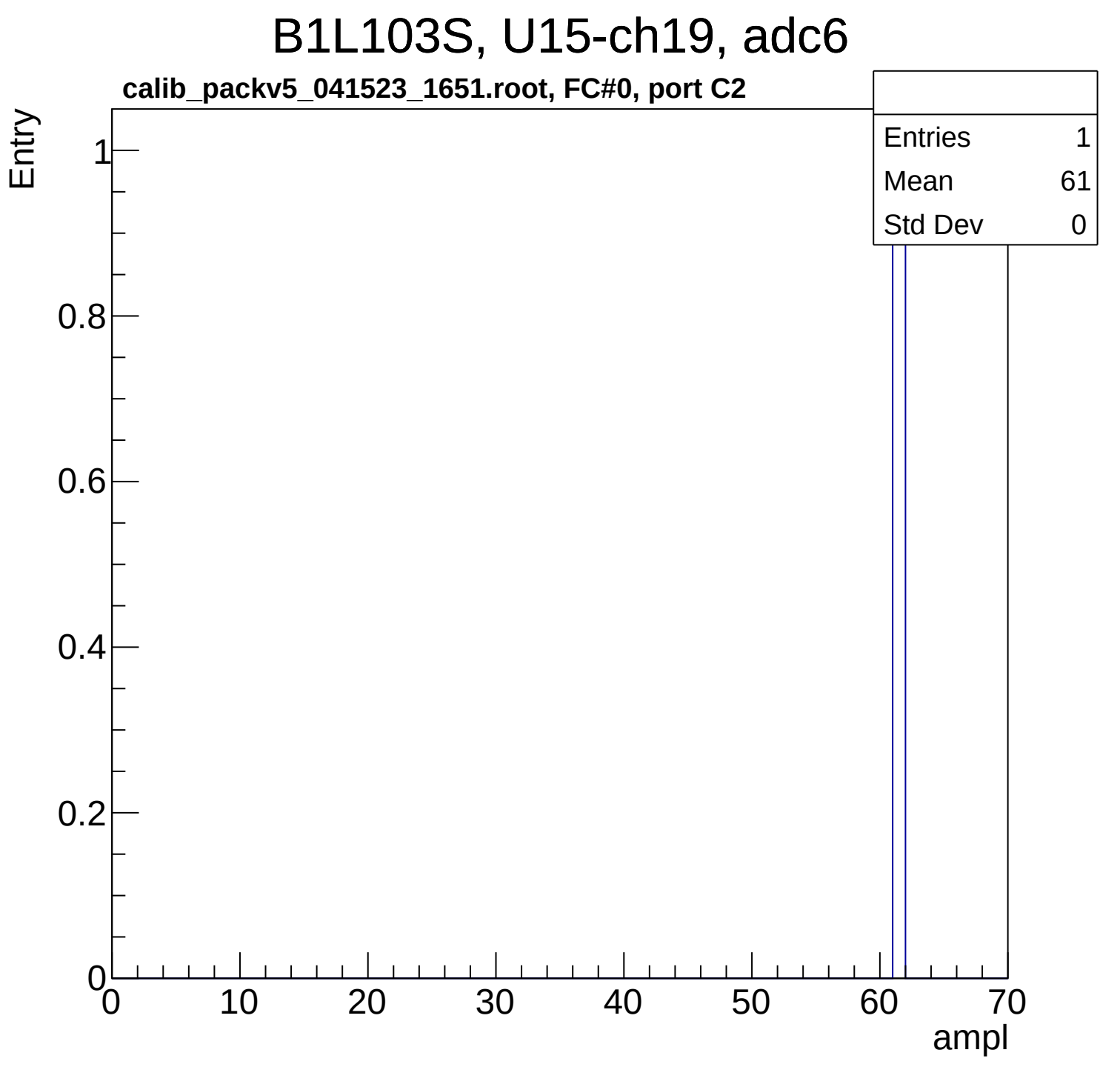
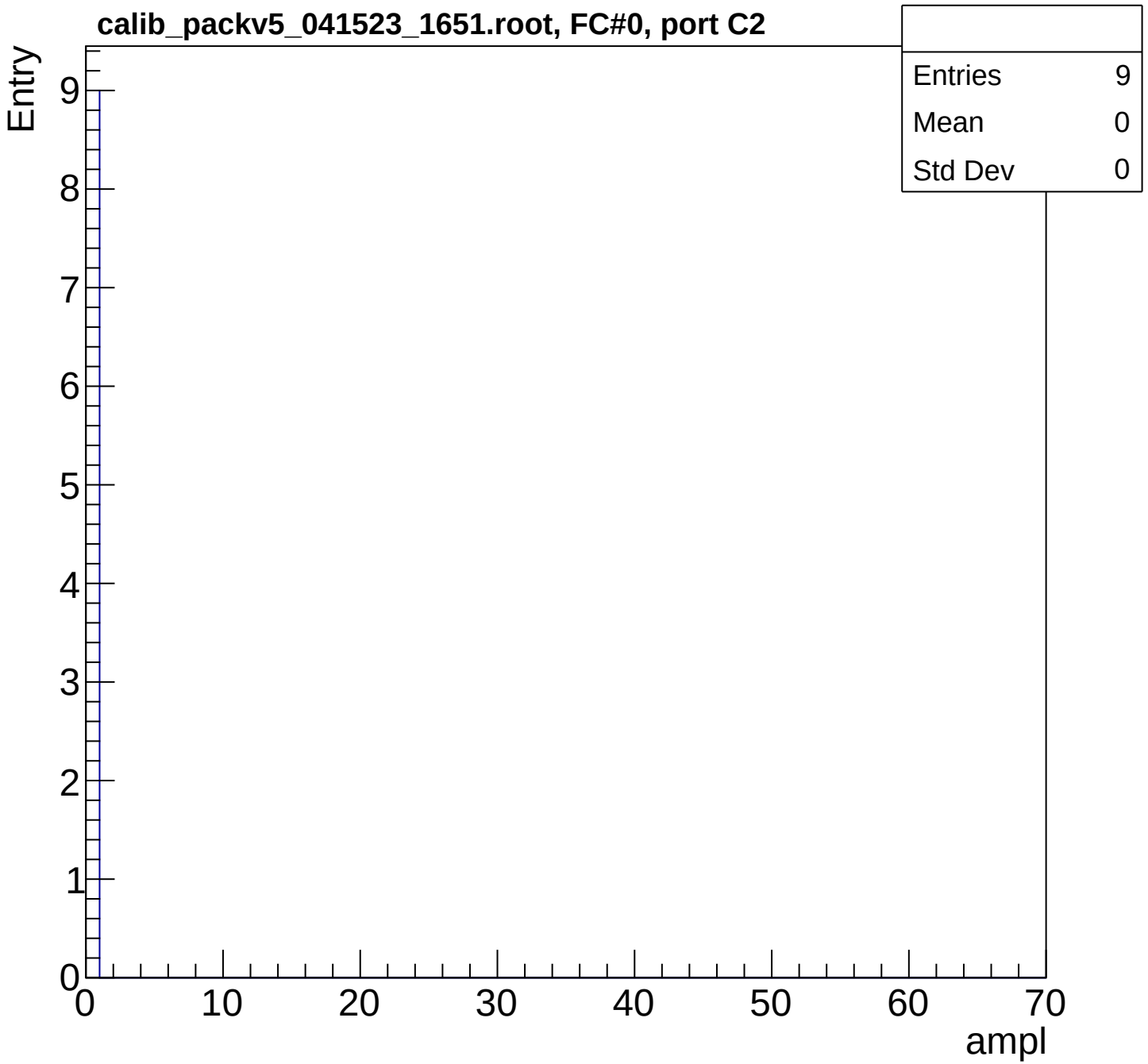
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch19, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 49.42
Std Dev 3.319
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch19, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 54.68
Std Dev 3.073
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch19, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 58.19
Std Dev 11.82
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch19, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 61
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch19, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 0
Std Dev 0
Entry
0
1
2
3
4
5
6
7
8
9
0
10
20
30
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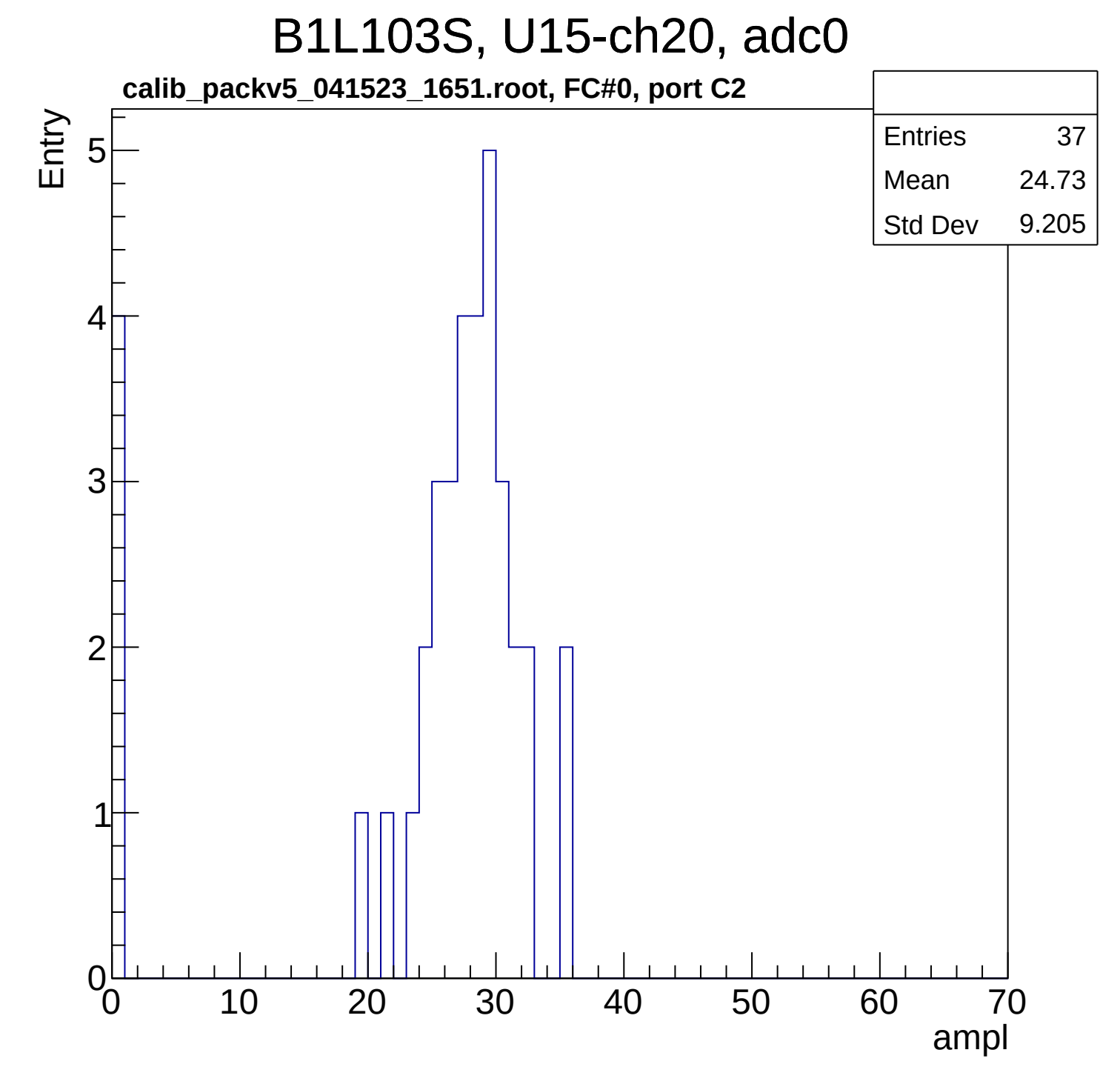
50
60
70
ampl


B1L103S, U15-ch20, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 24.73
Std Dev 9.205
Entry
ampl
0
1
2
3
4
5
0
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40
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60
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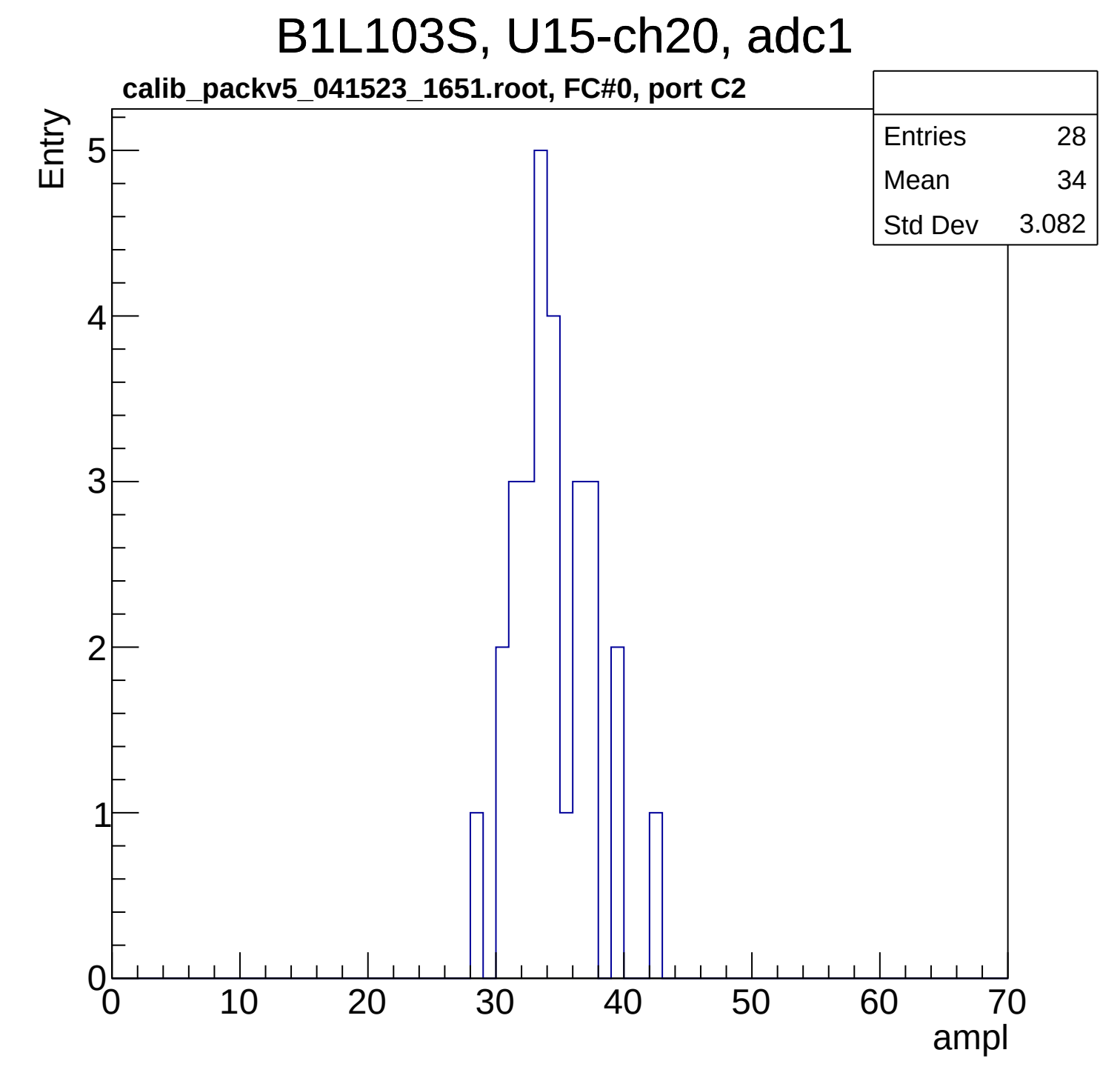
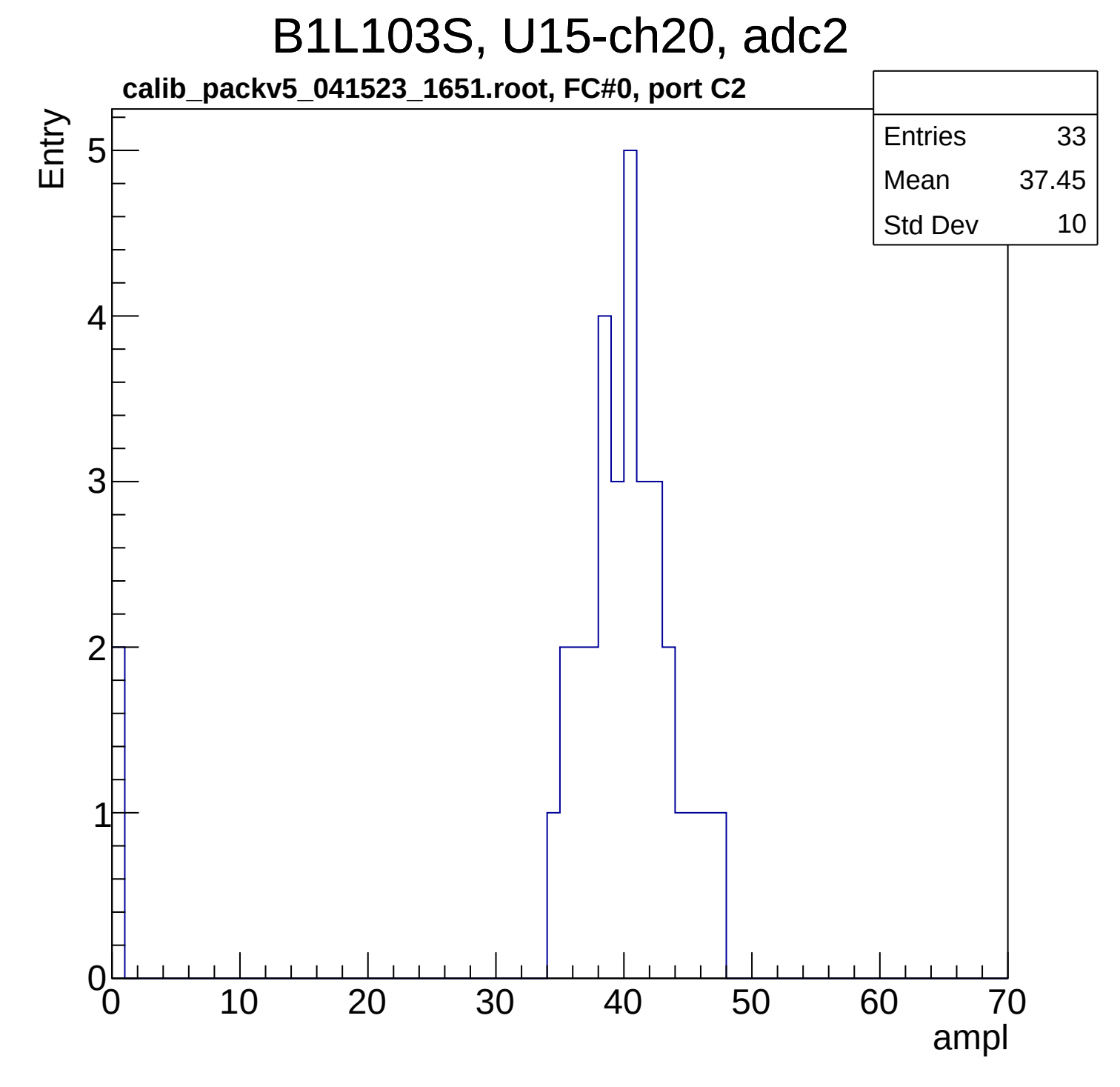
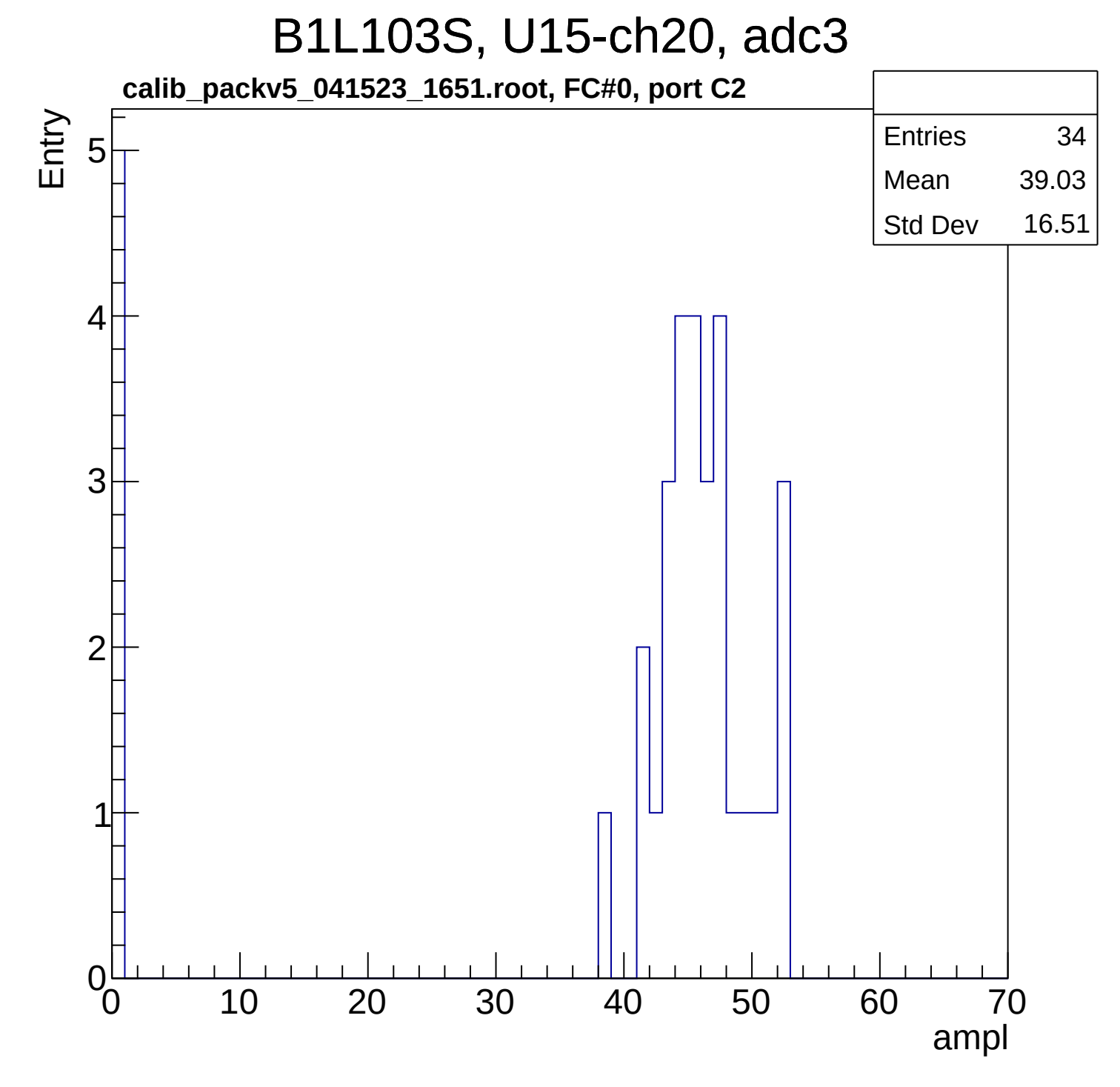

B1L103S, U15-ch20, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 34
Std Dev 3.082
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch20, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 37.45
Std Dev 10
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch20, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 39.03
Std Dev 16.51
Entry
ampl
0
1
2
3
4
5
0
10
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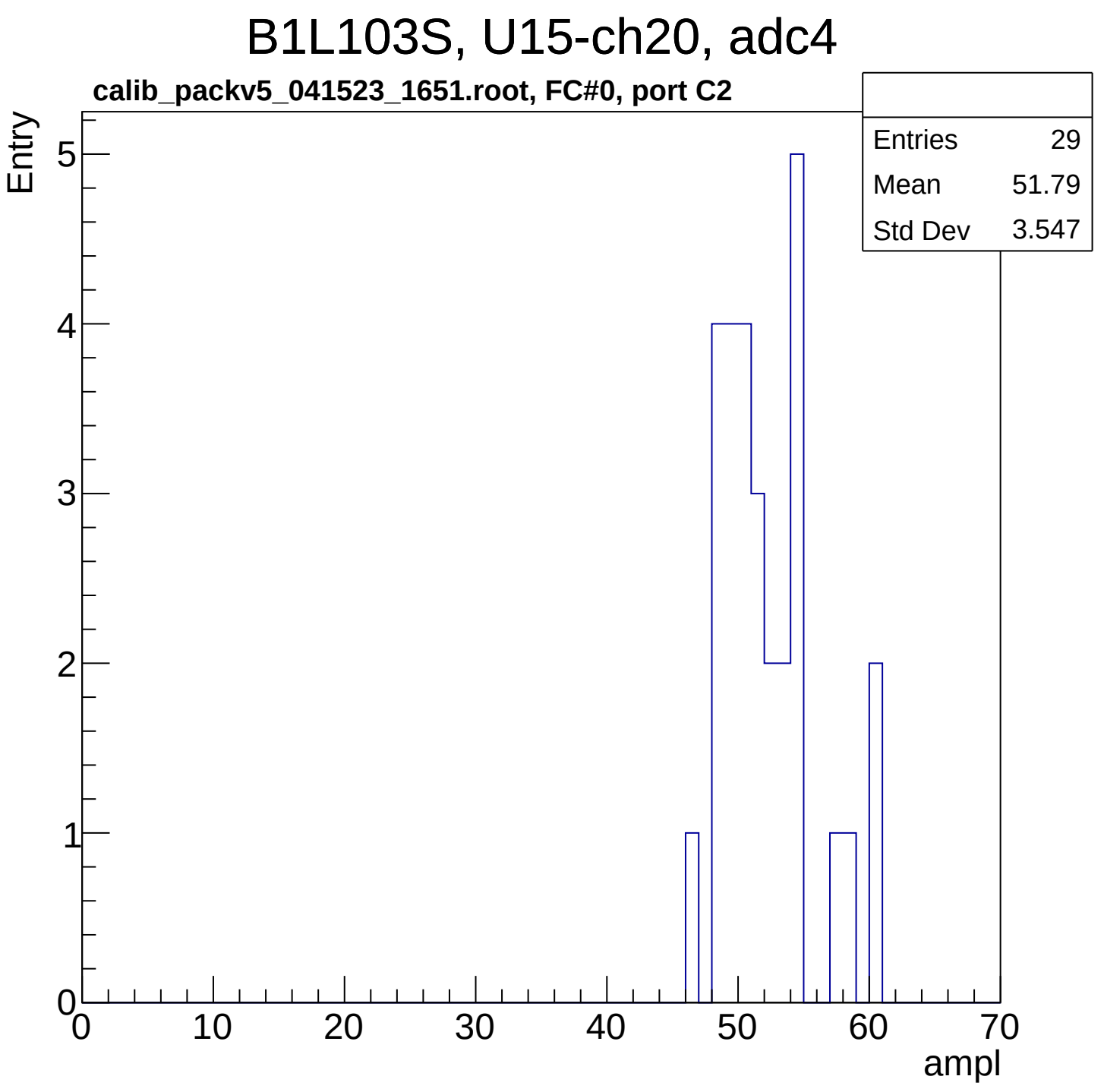
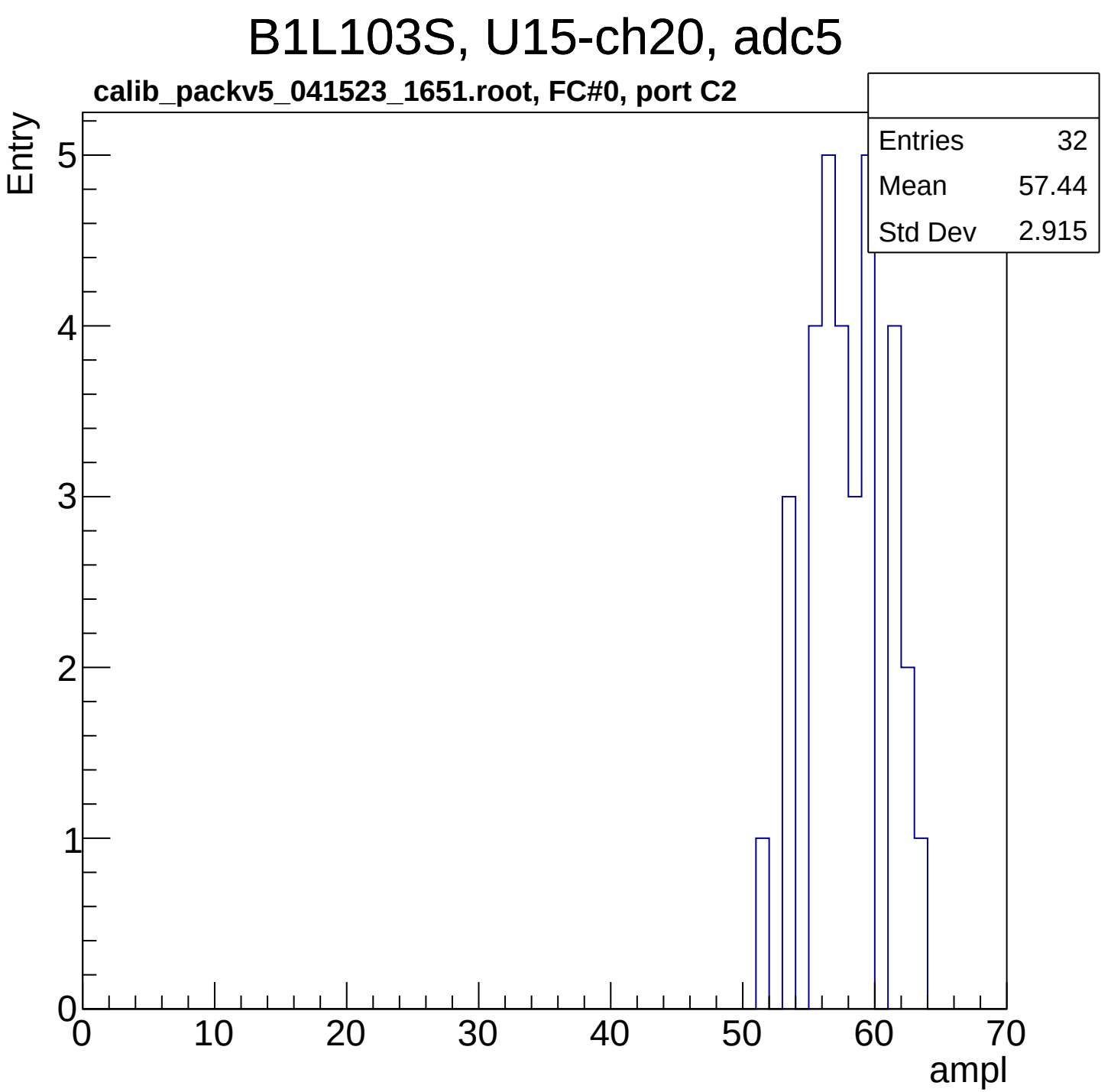
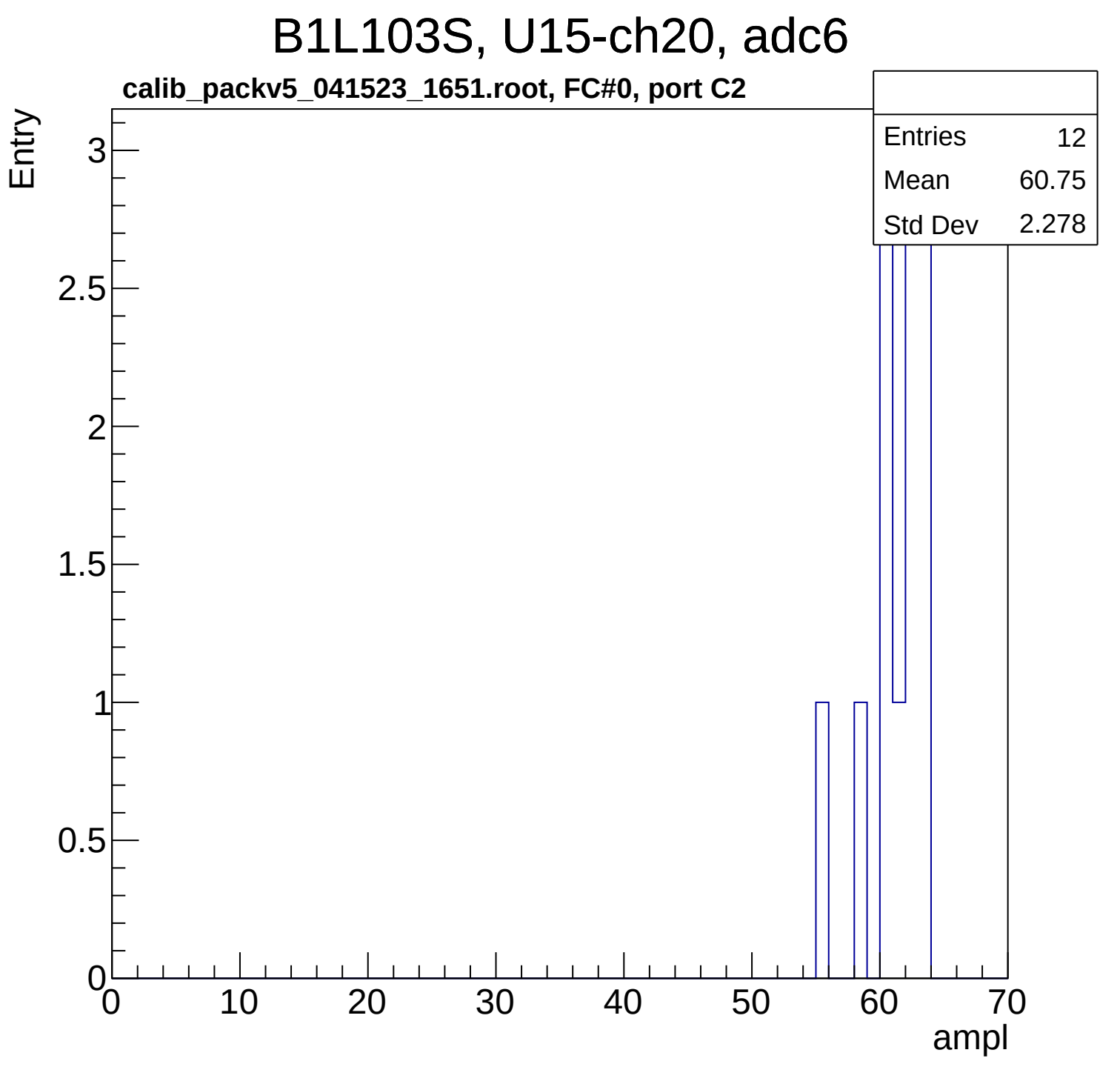
30
40
50
60
70


B1L103S, U15-ch20, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 51.79
Std Dev 3.547
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch20, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 57.44
Std Dev 2.915
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch20, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 60.75
Std Dev 2.278
Entry
ampl
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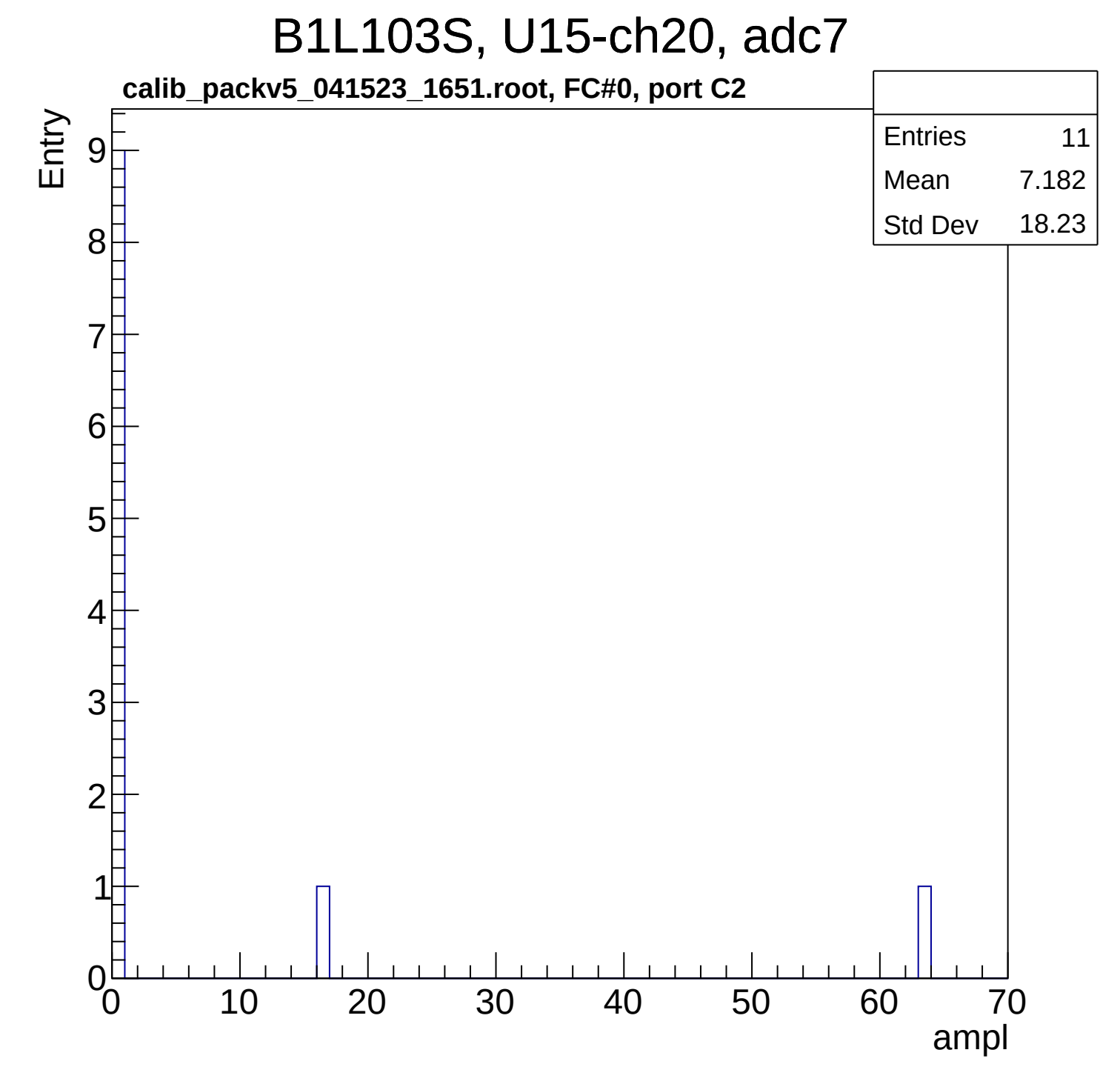
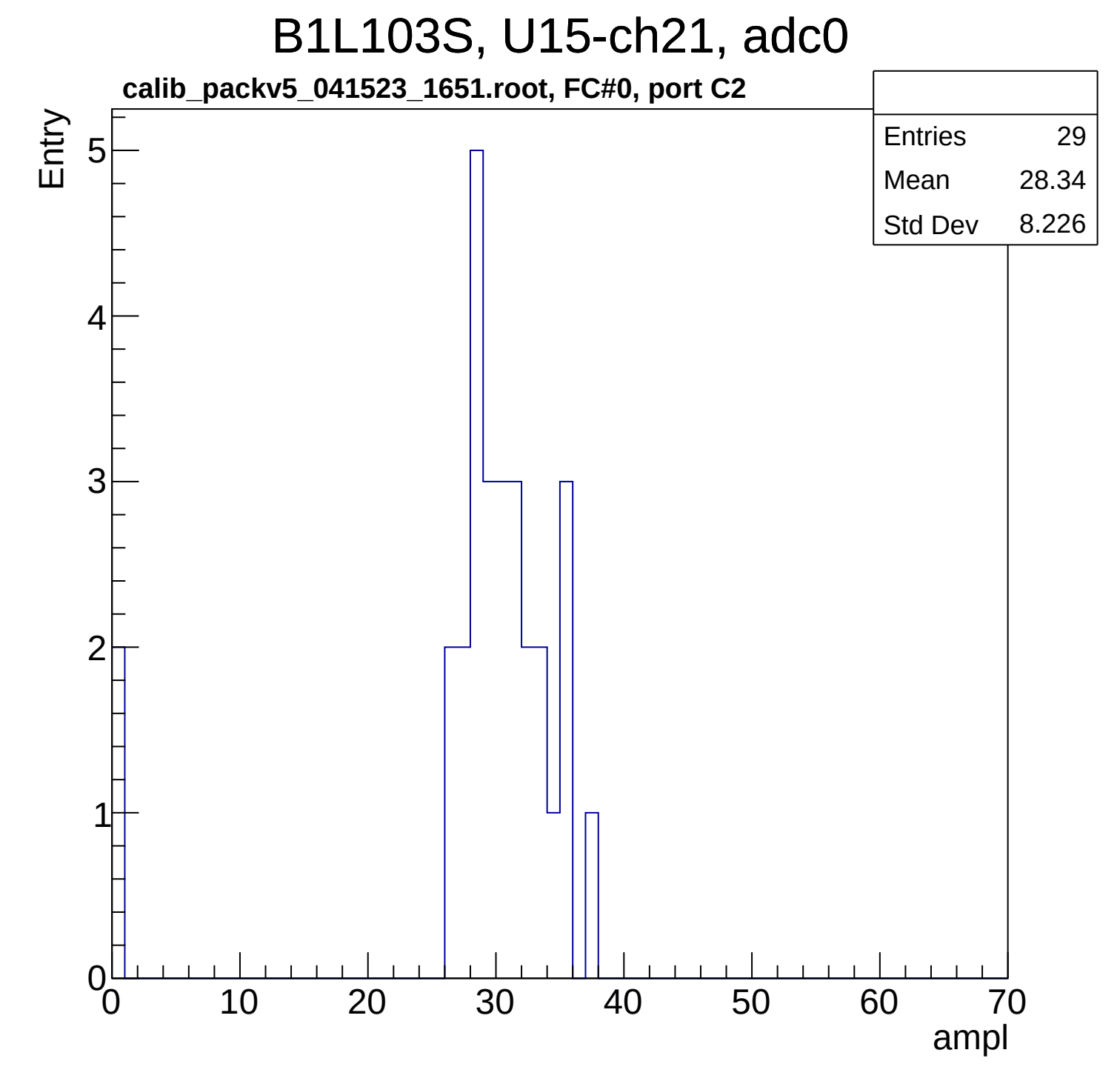
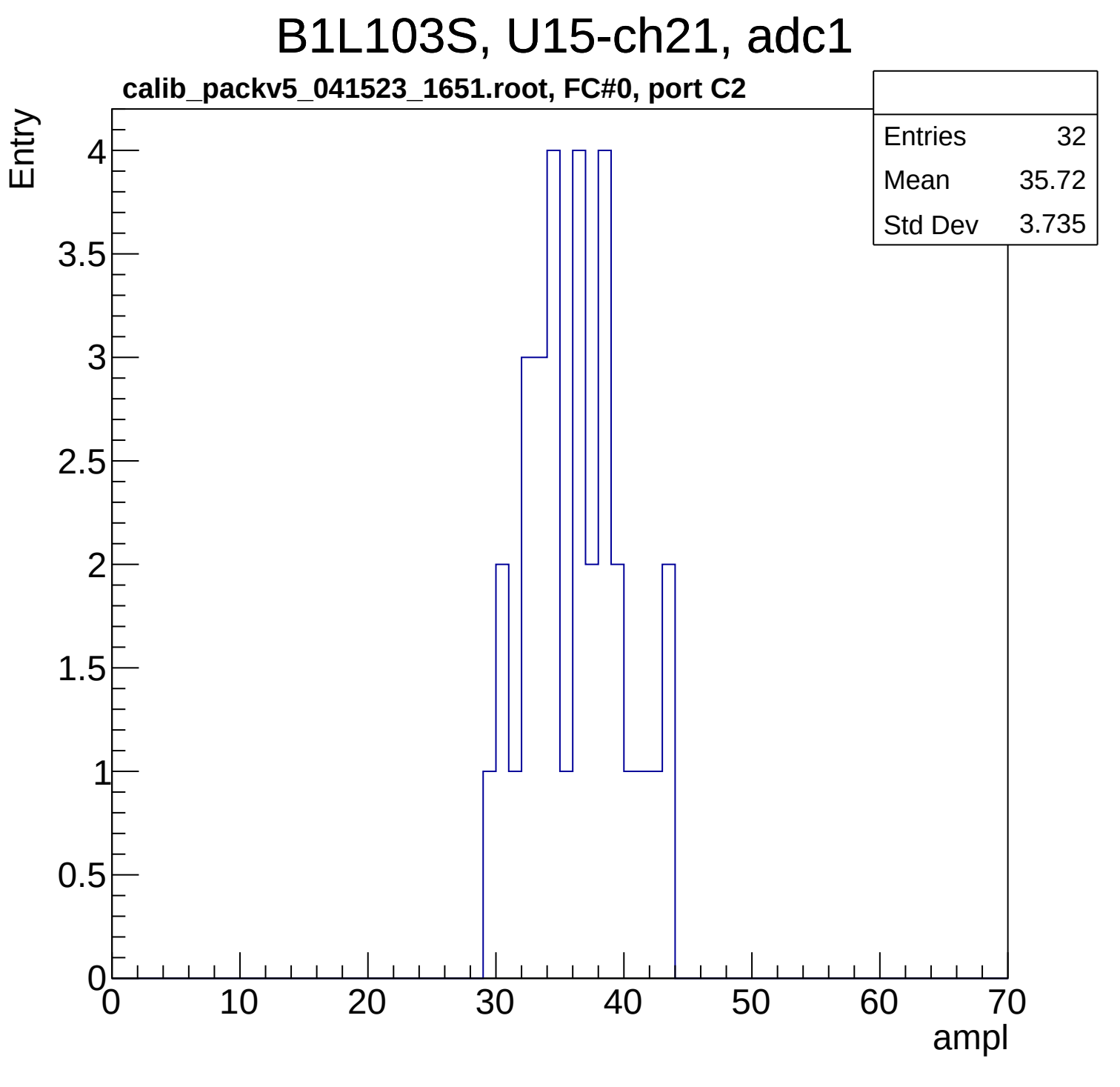
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch20, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 7.182
Std Dev 18.23
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U15-ch21, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 28.34
Std Dev 8.226
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch21, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 35.72
Std Dev 3.735
Entry
ampl
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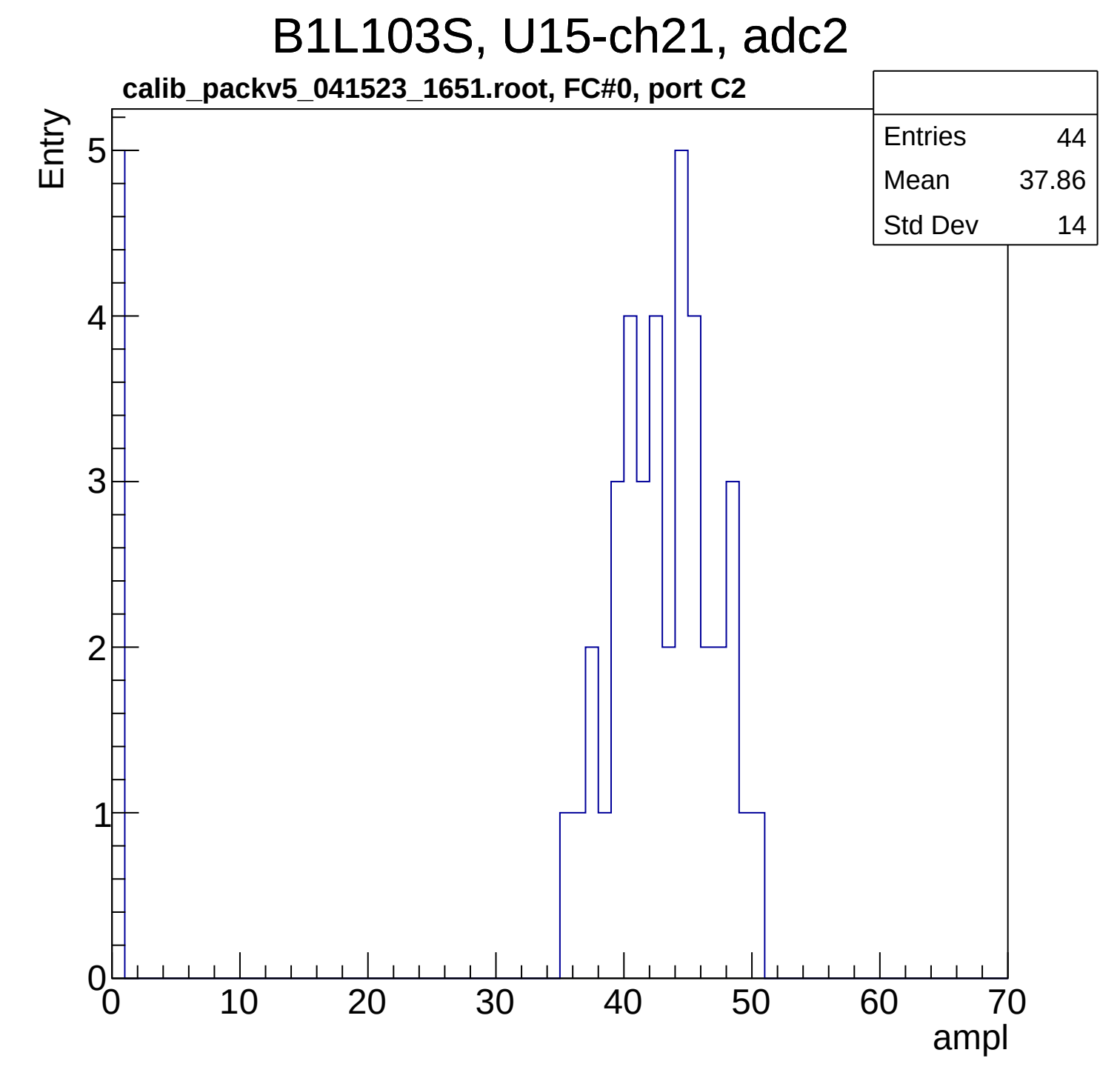
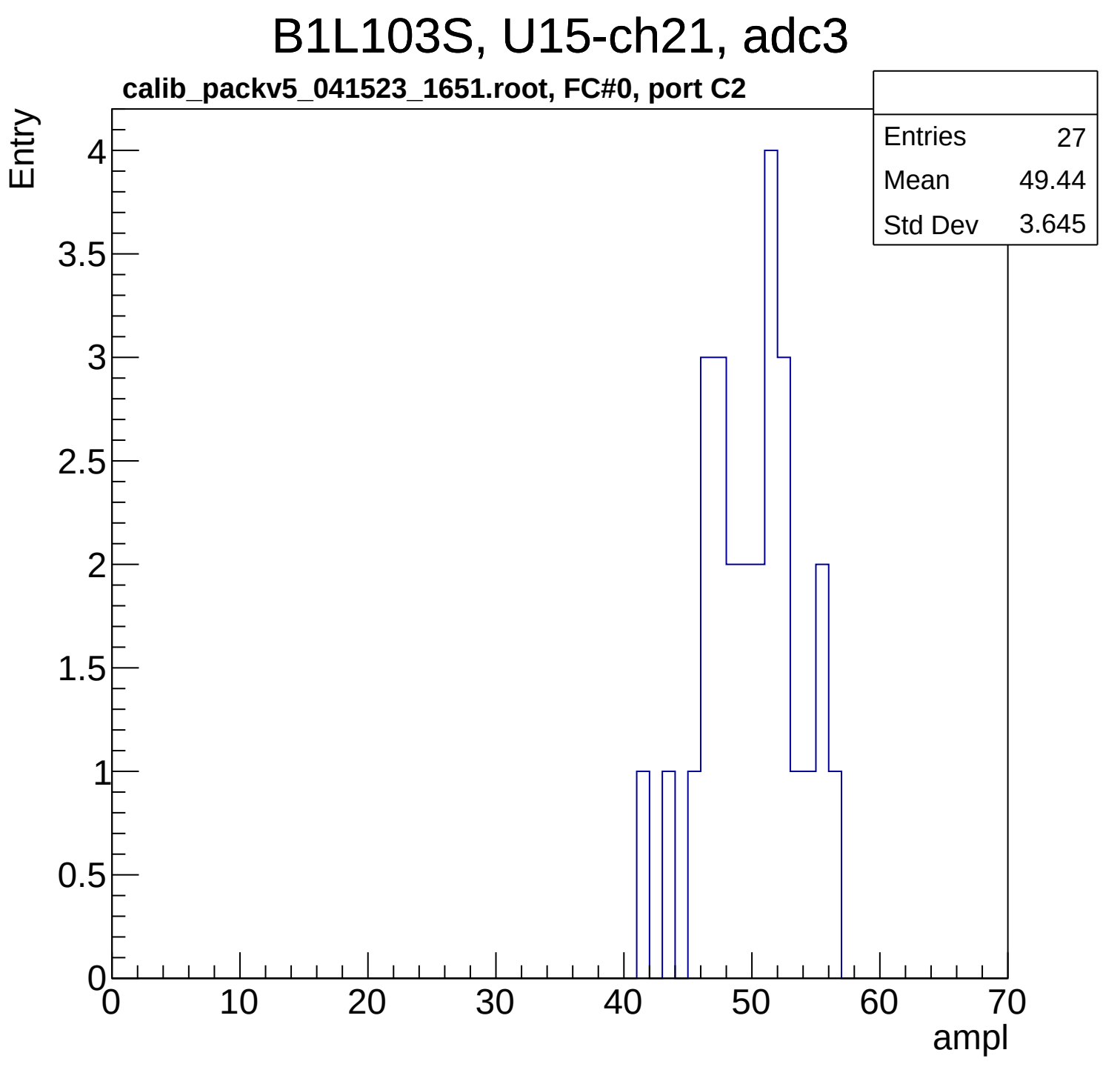
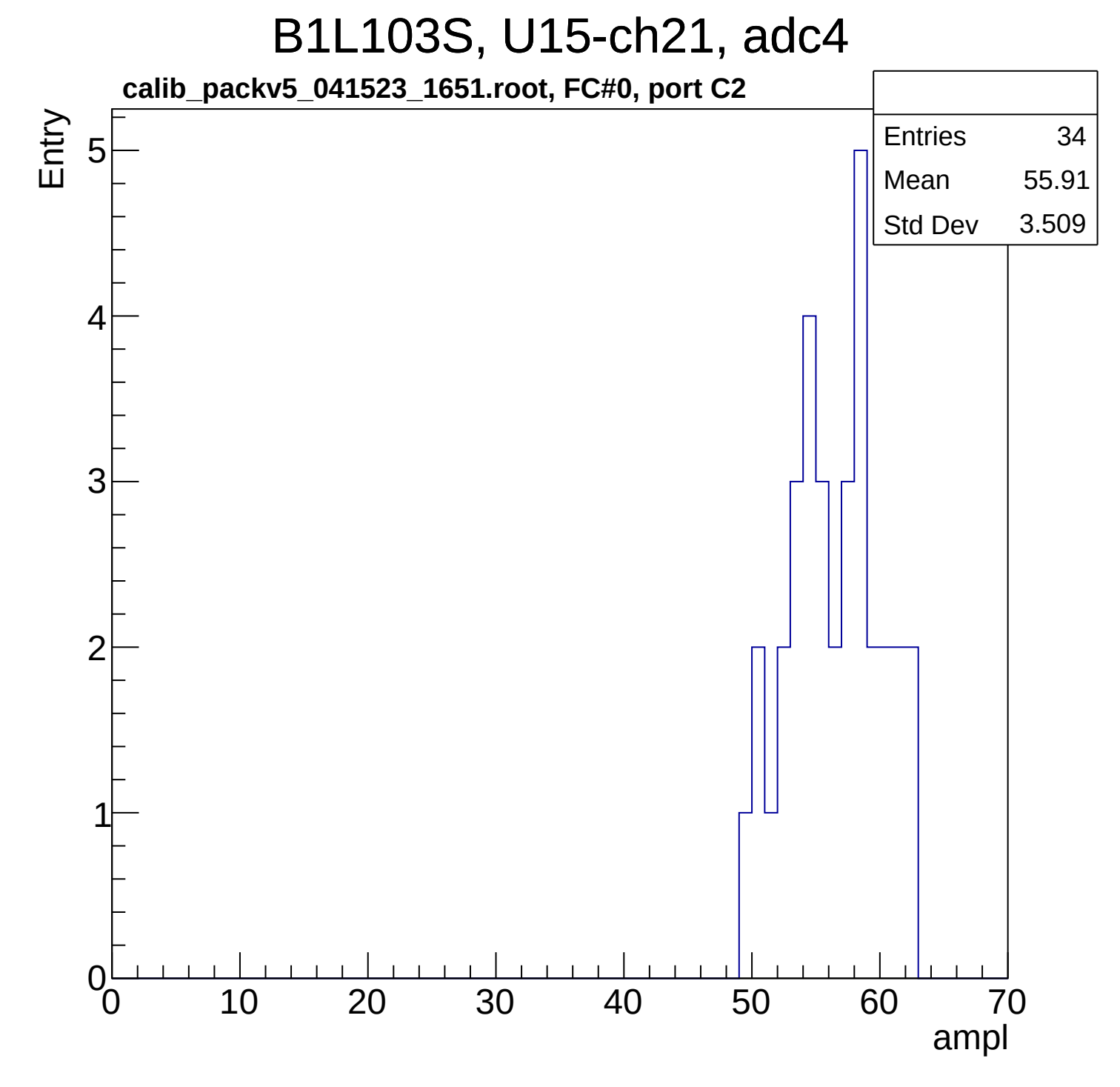
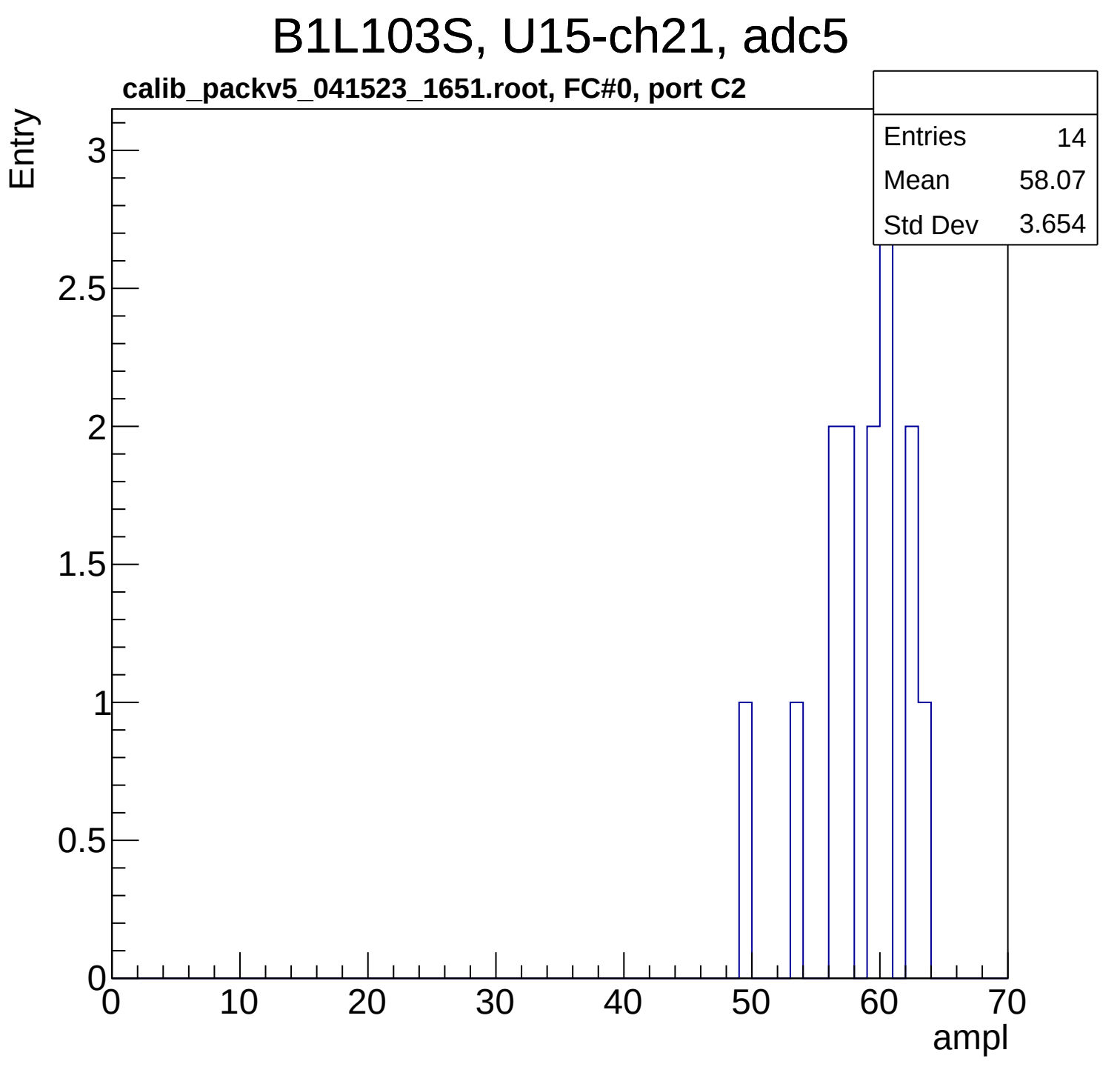
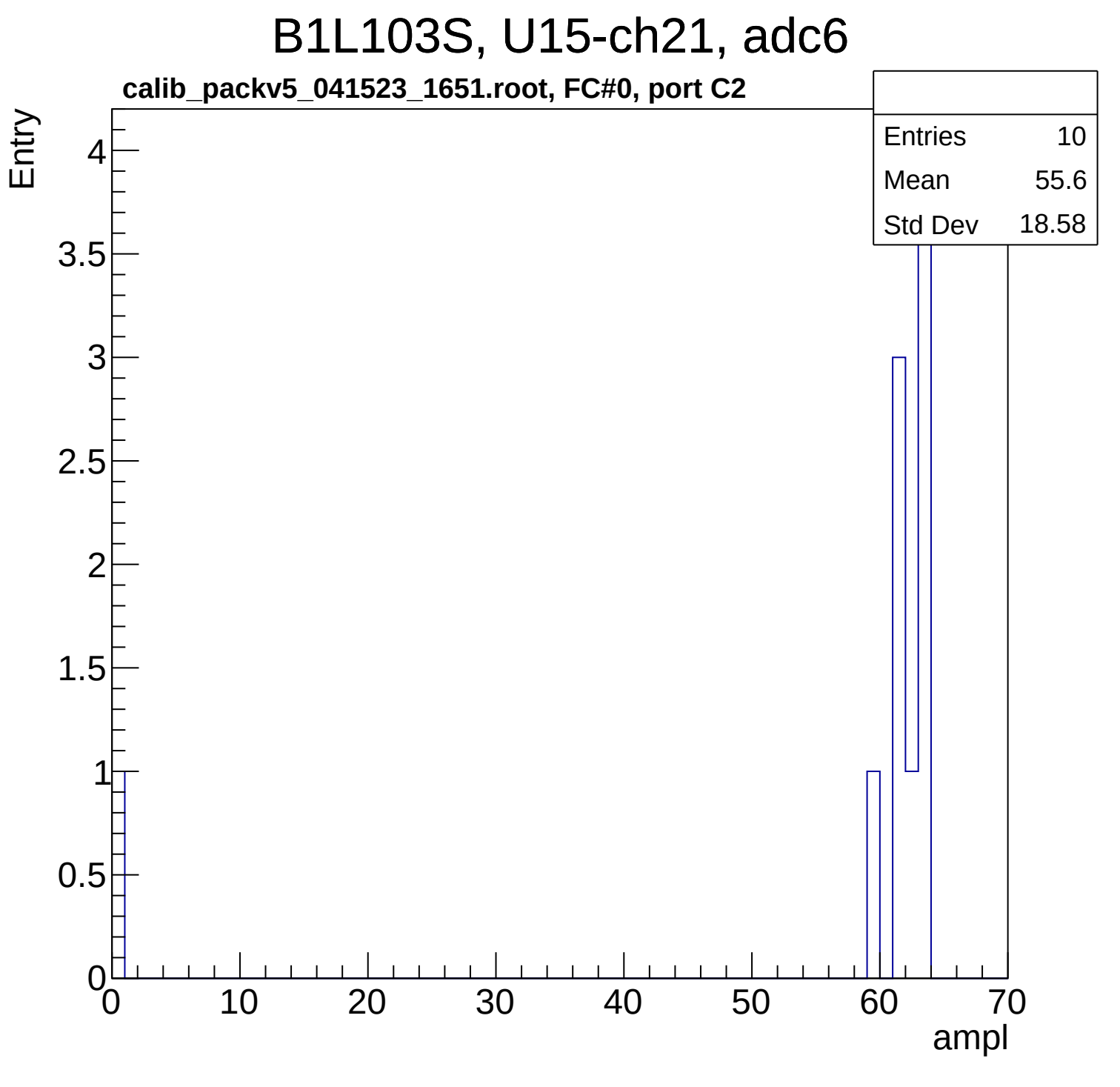
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

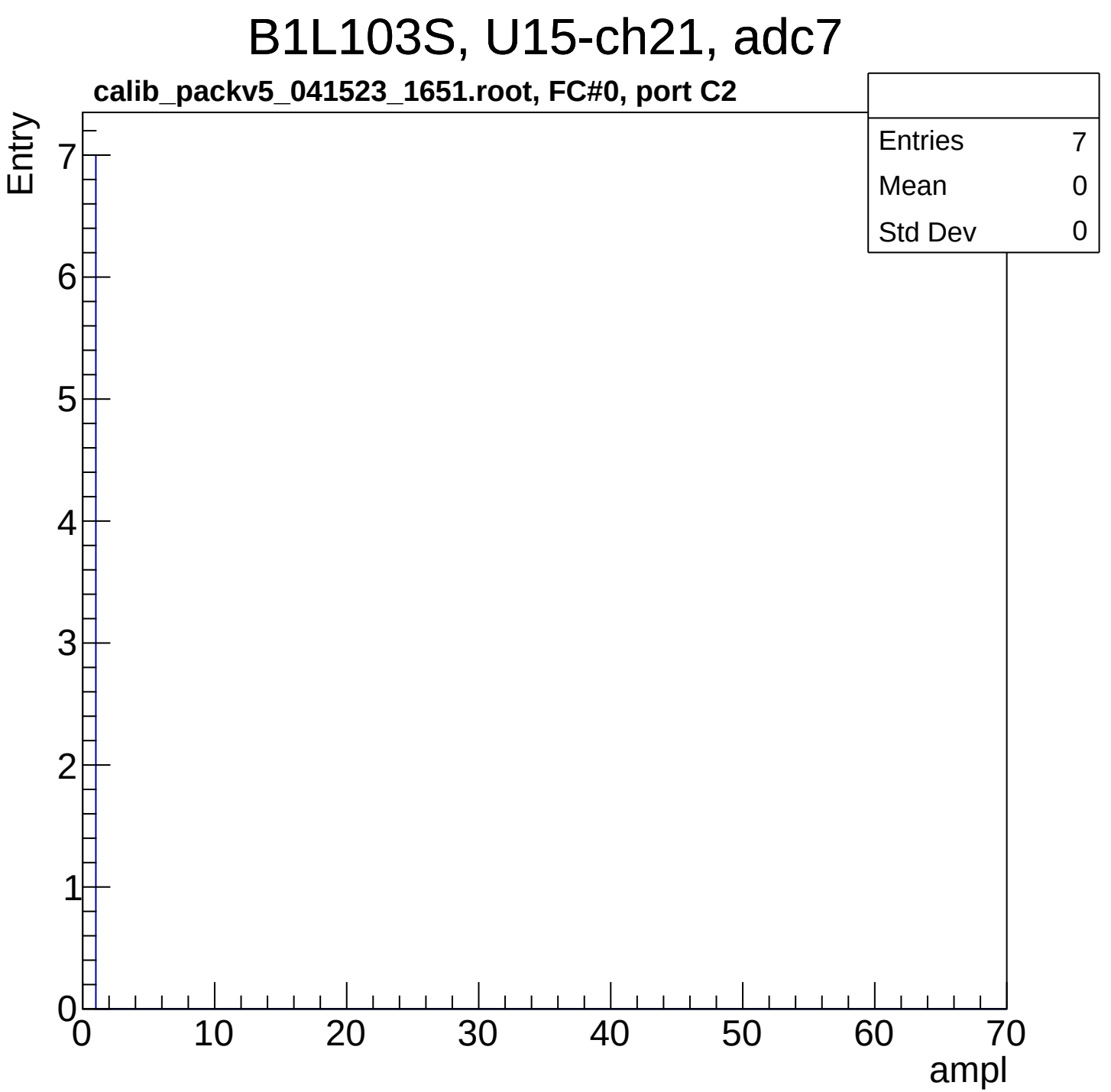

B1L103S, U15-ch21, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 37.86
Std Dev 14
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

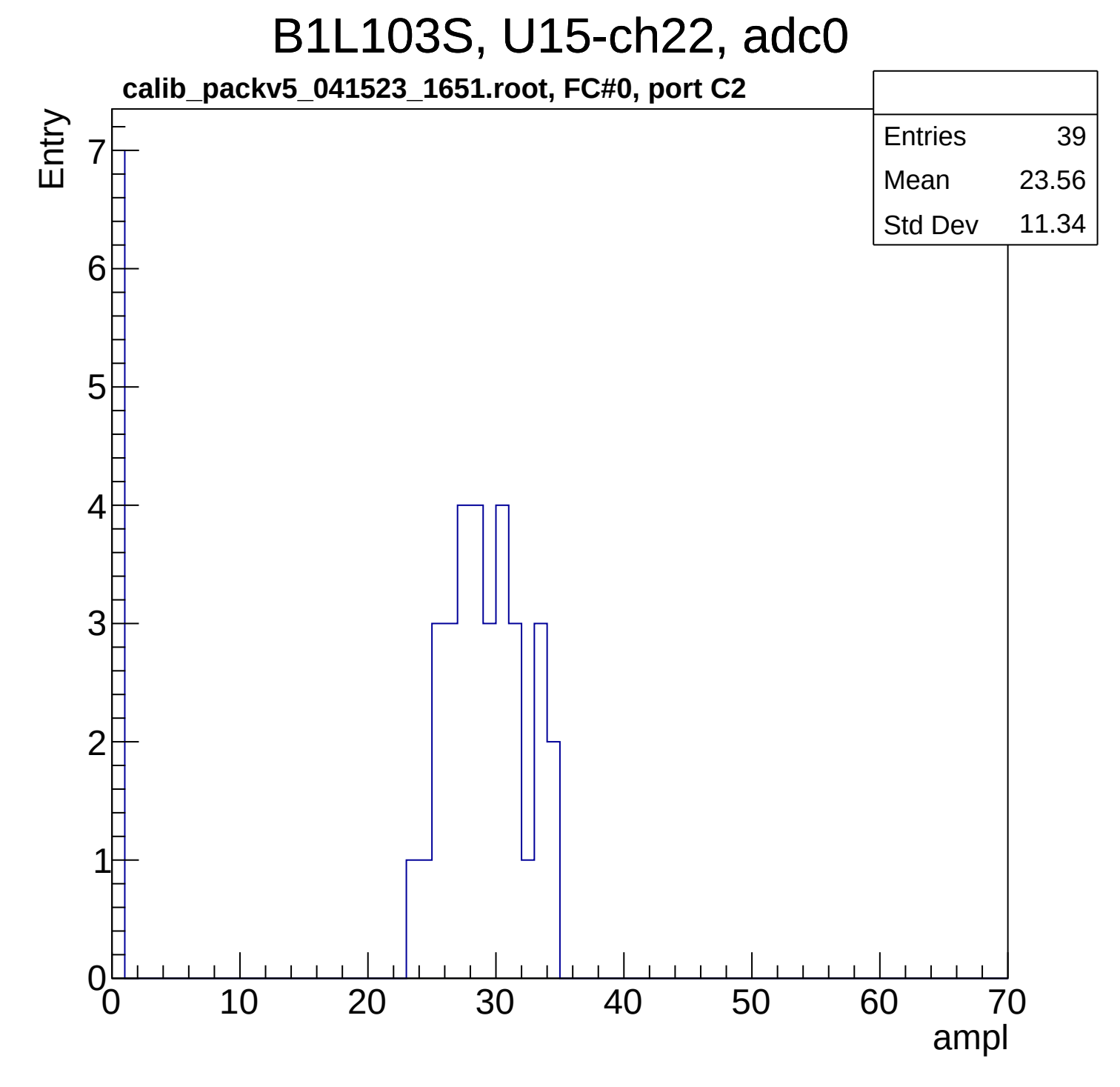

B1L103S, U15-ch21, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 49.44
Std Dev 3.645
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

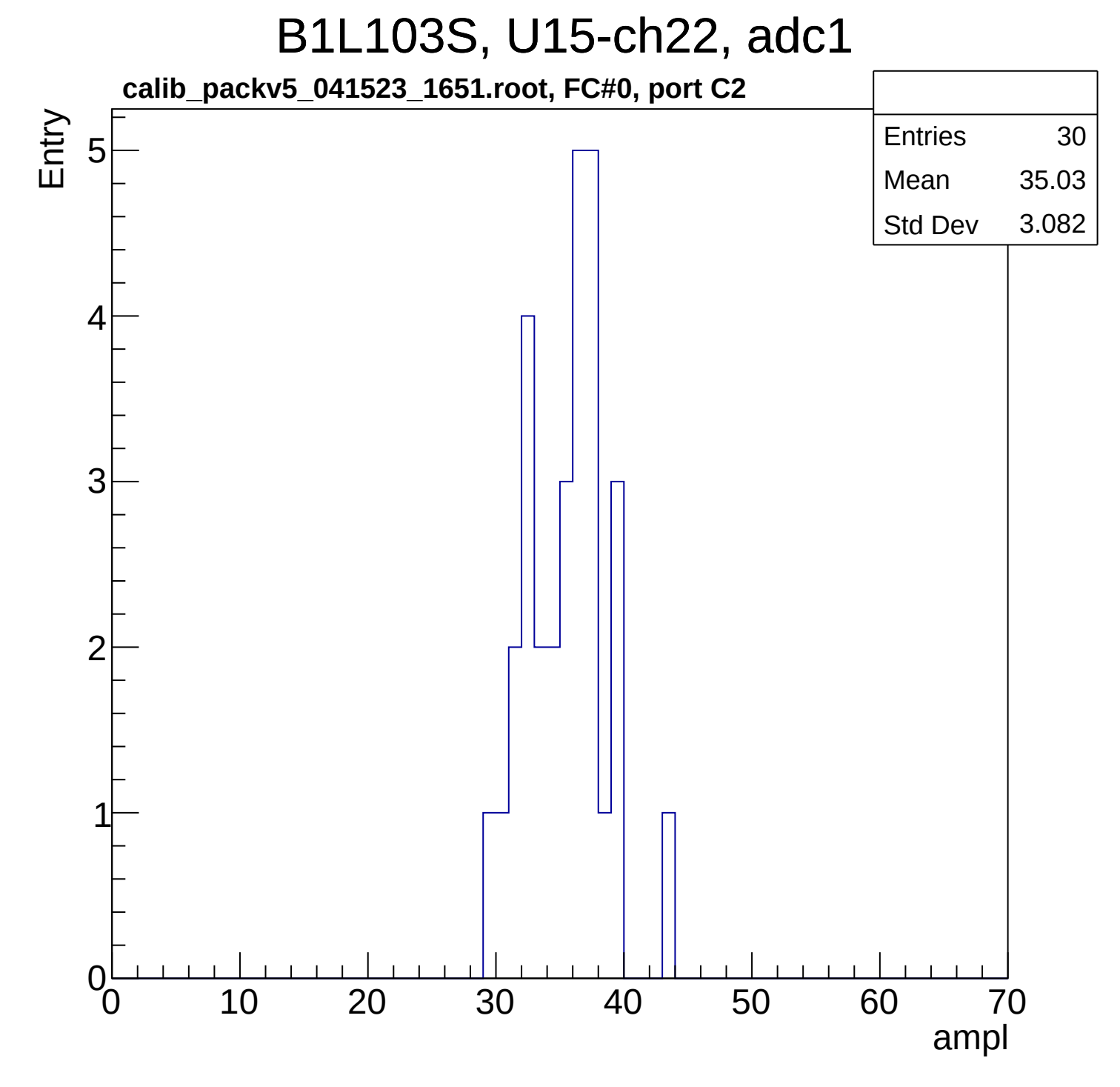

B1L103S, U15-ch21, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 55.91
Std Dev 3.509
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

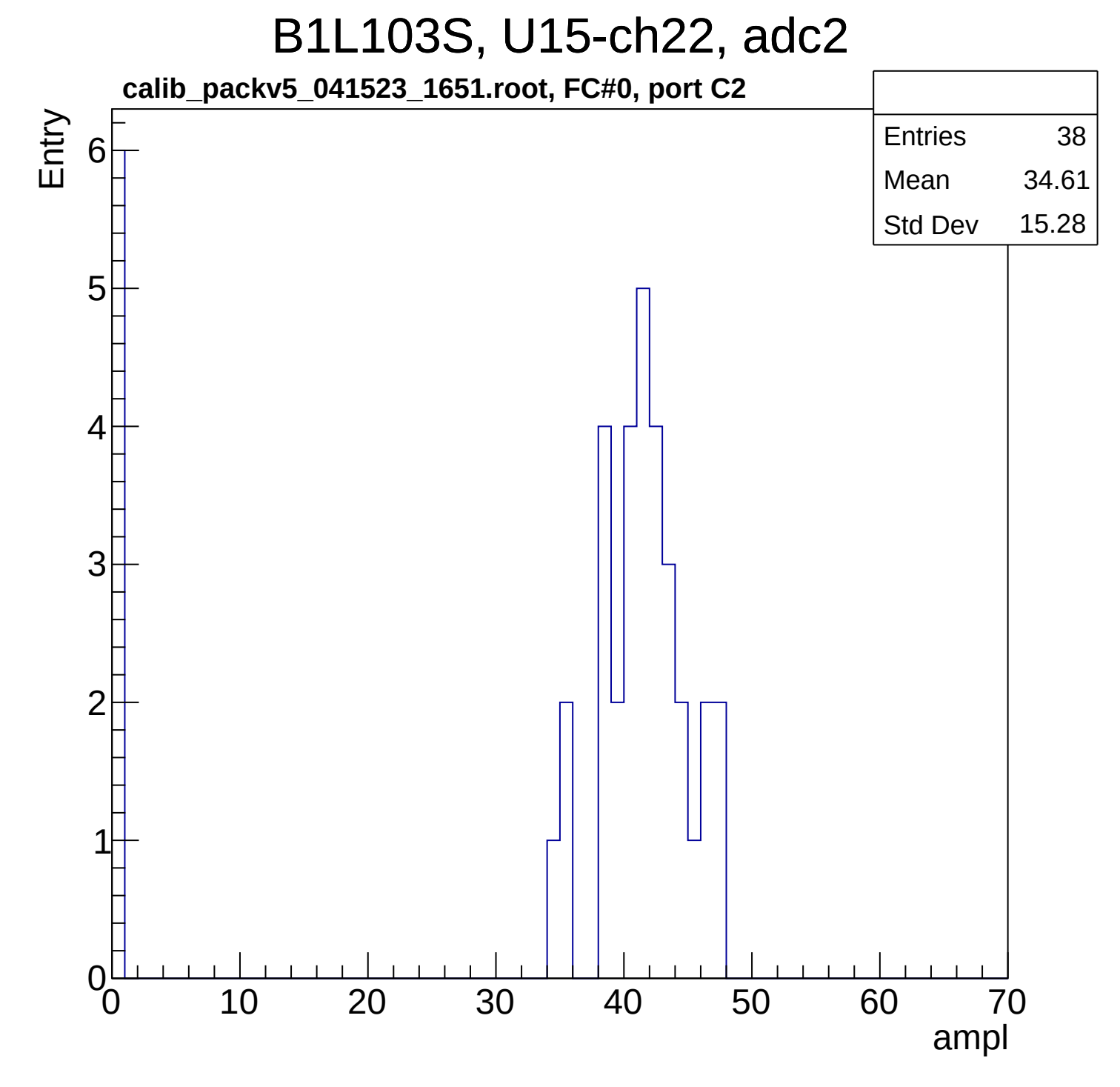

B1L103S, U15-ch21, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 58.07
Std Dev 3.654
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

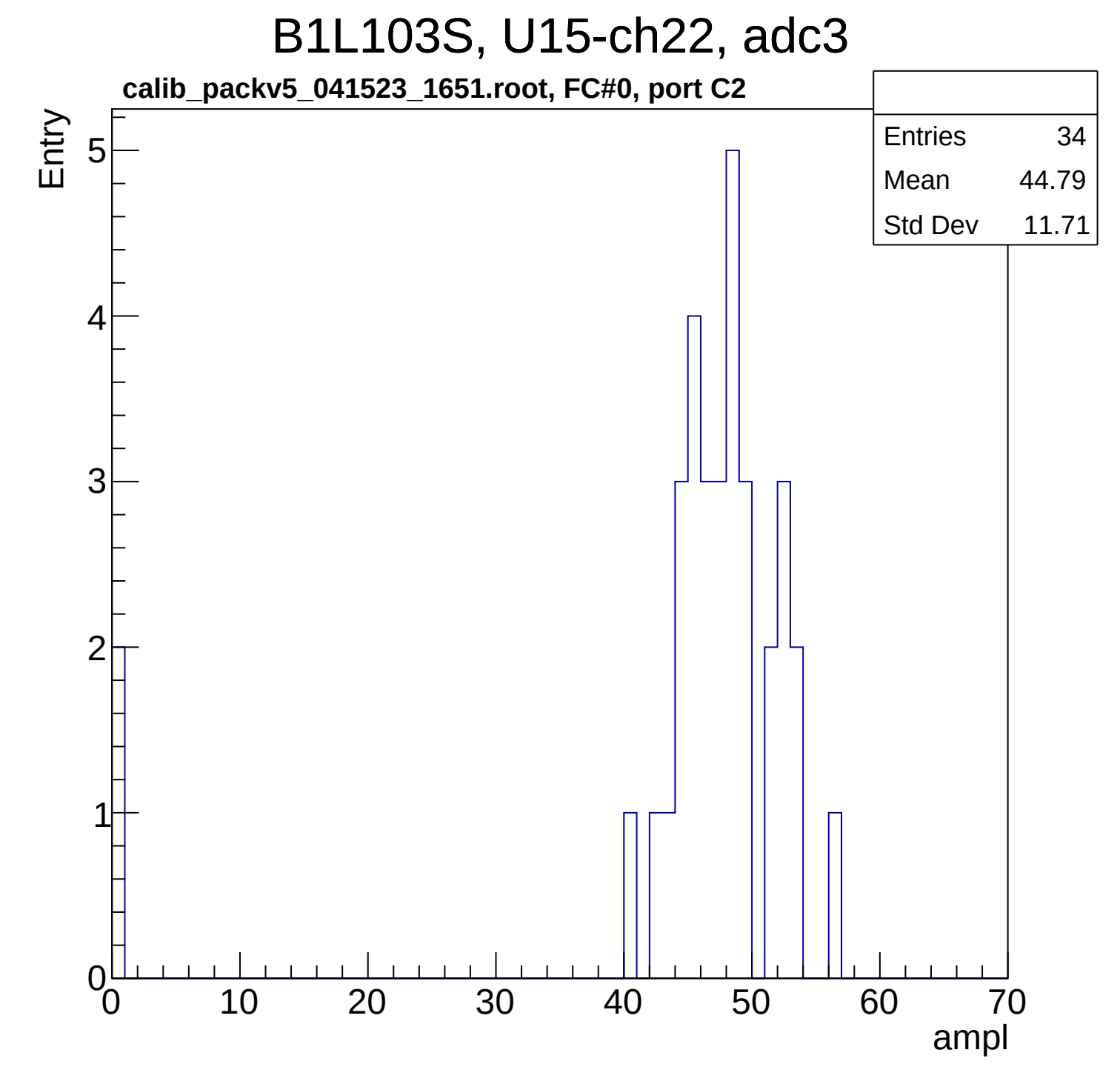

B1L103S, U15-ch21, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.6
Std Dev 18.58
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

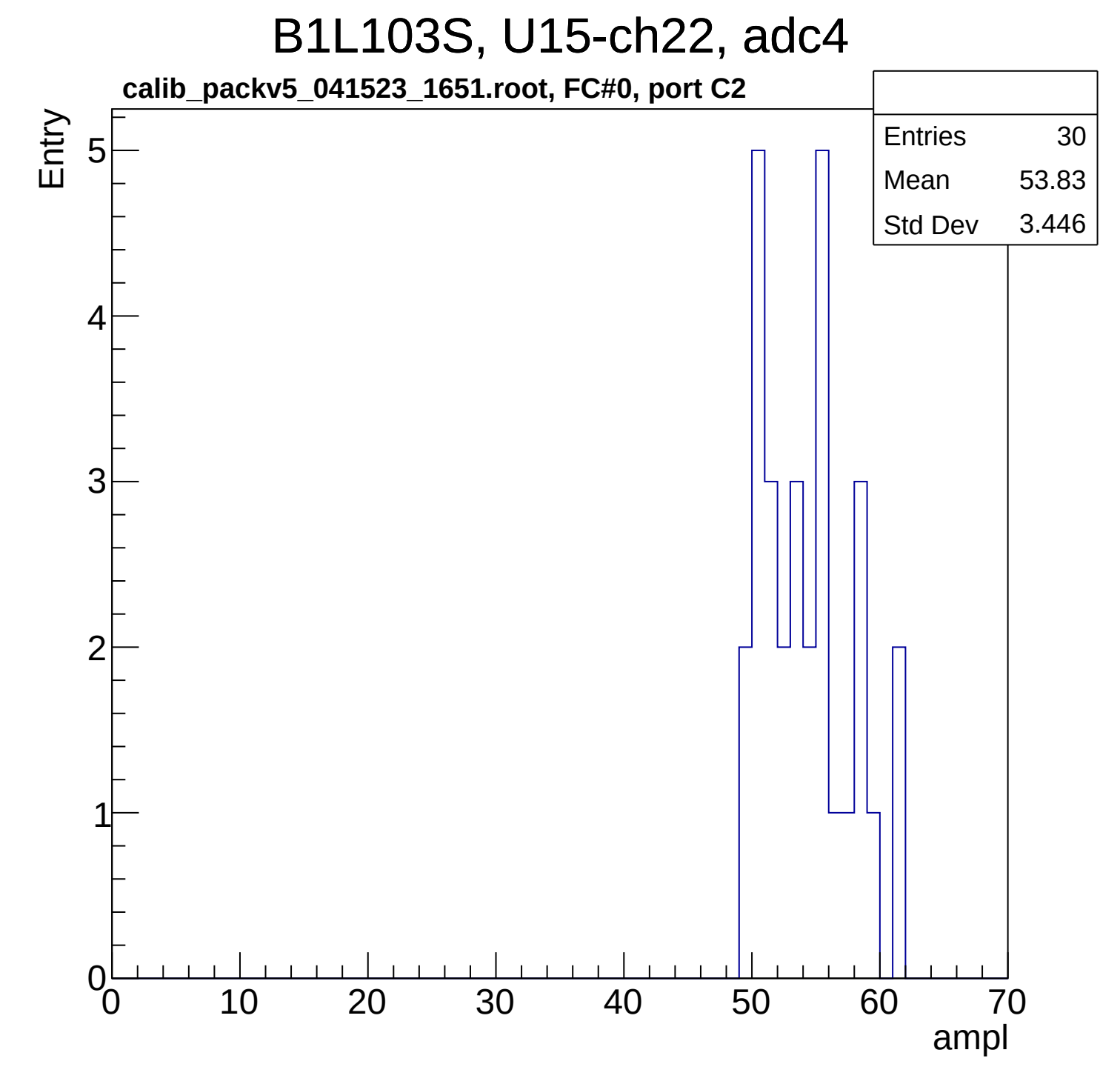

B1L103S, U15-ch21, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 0
Std Dev 0
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

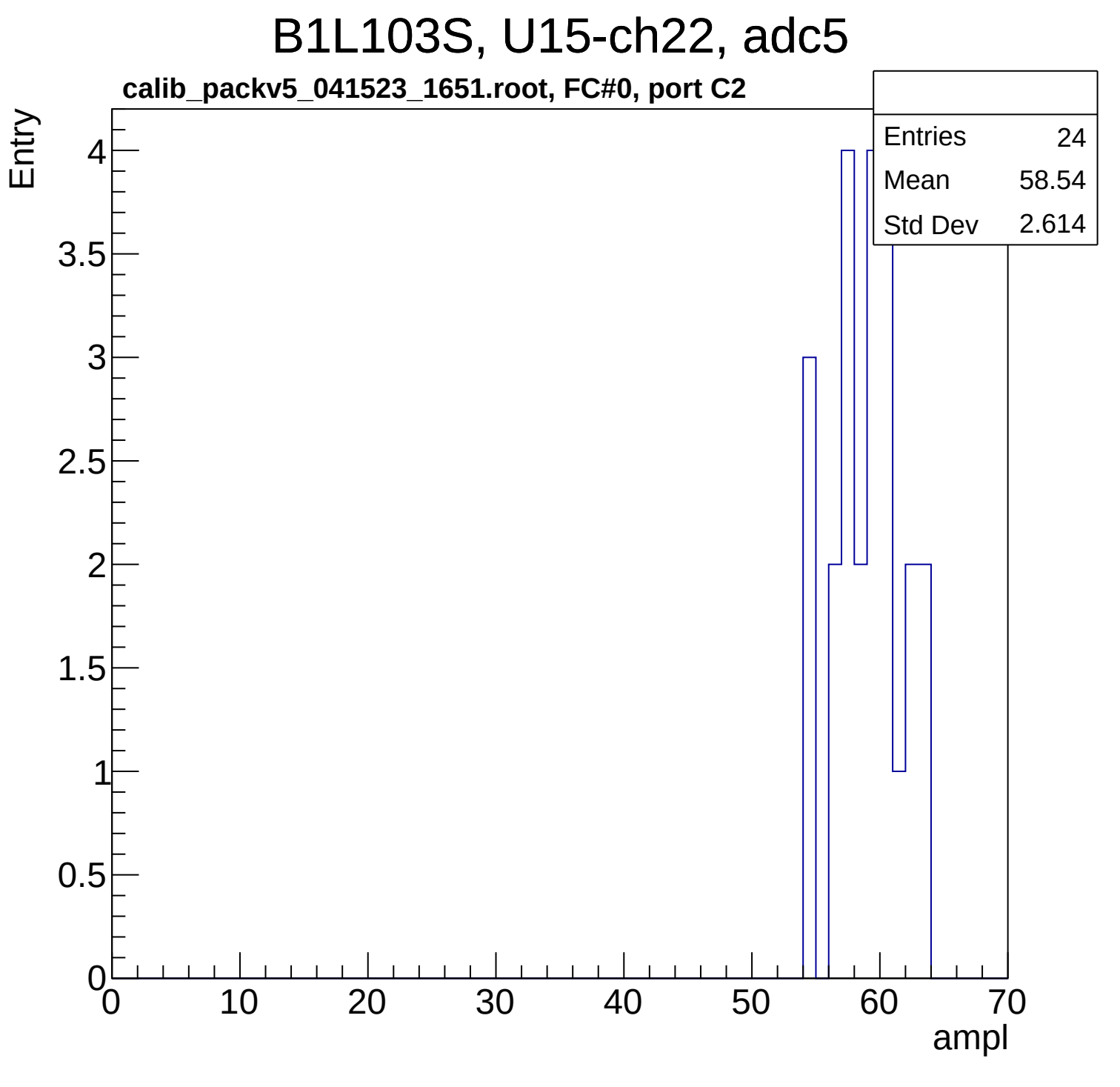

B1L103S, U15-ch22, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 23.56
Std Dev 11.34
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U15-ch22, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 35.03
Std Dev 3.082
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch22, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 34.61
Std Dev 15.28
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch22, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 44.79
Std Dev 11.71
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch22, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 53.83
Std Dev 3.446
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch22, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 58.54
Std Dev 2.614
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
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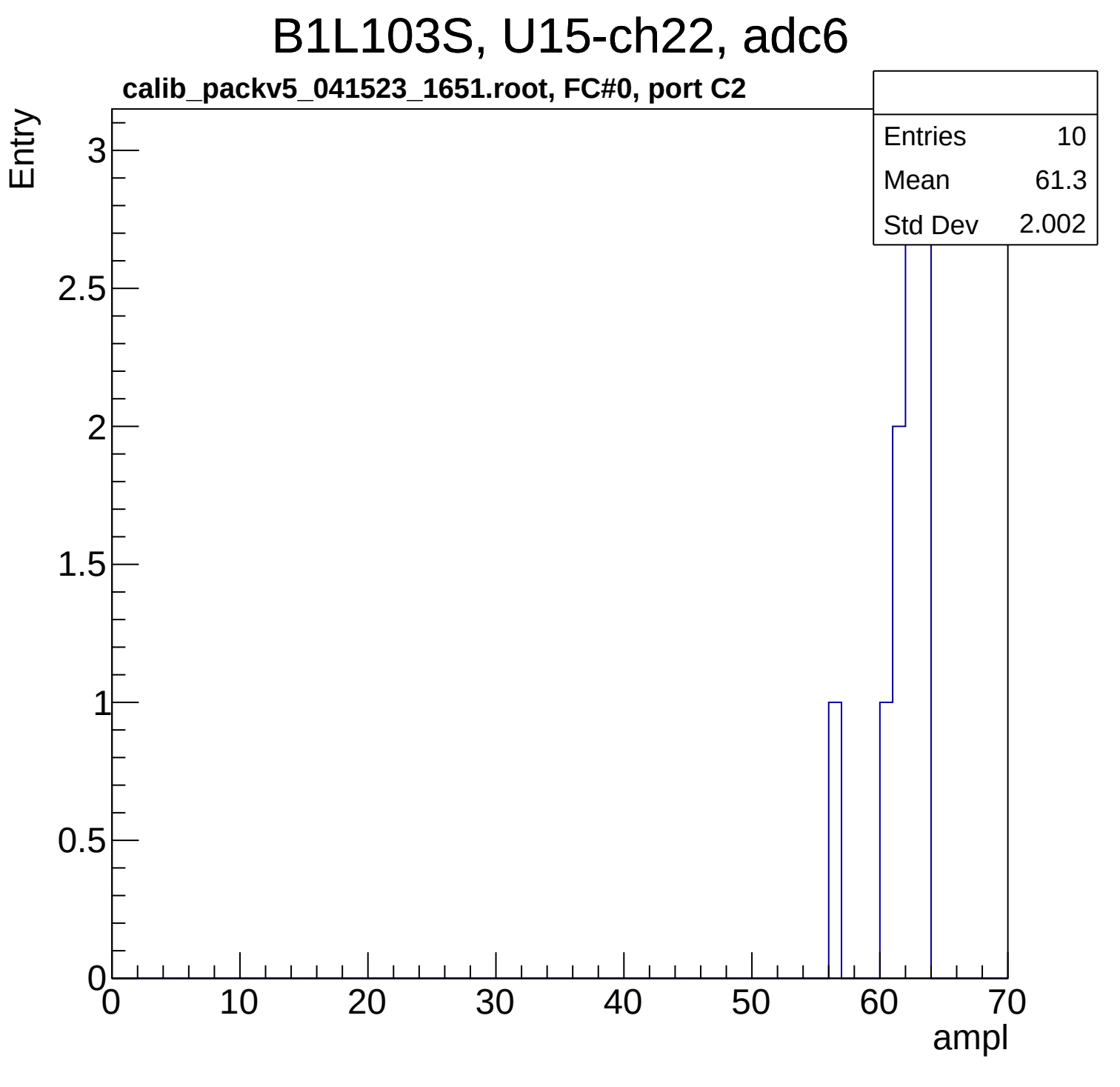
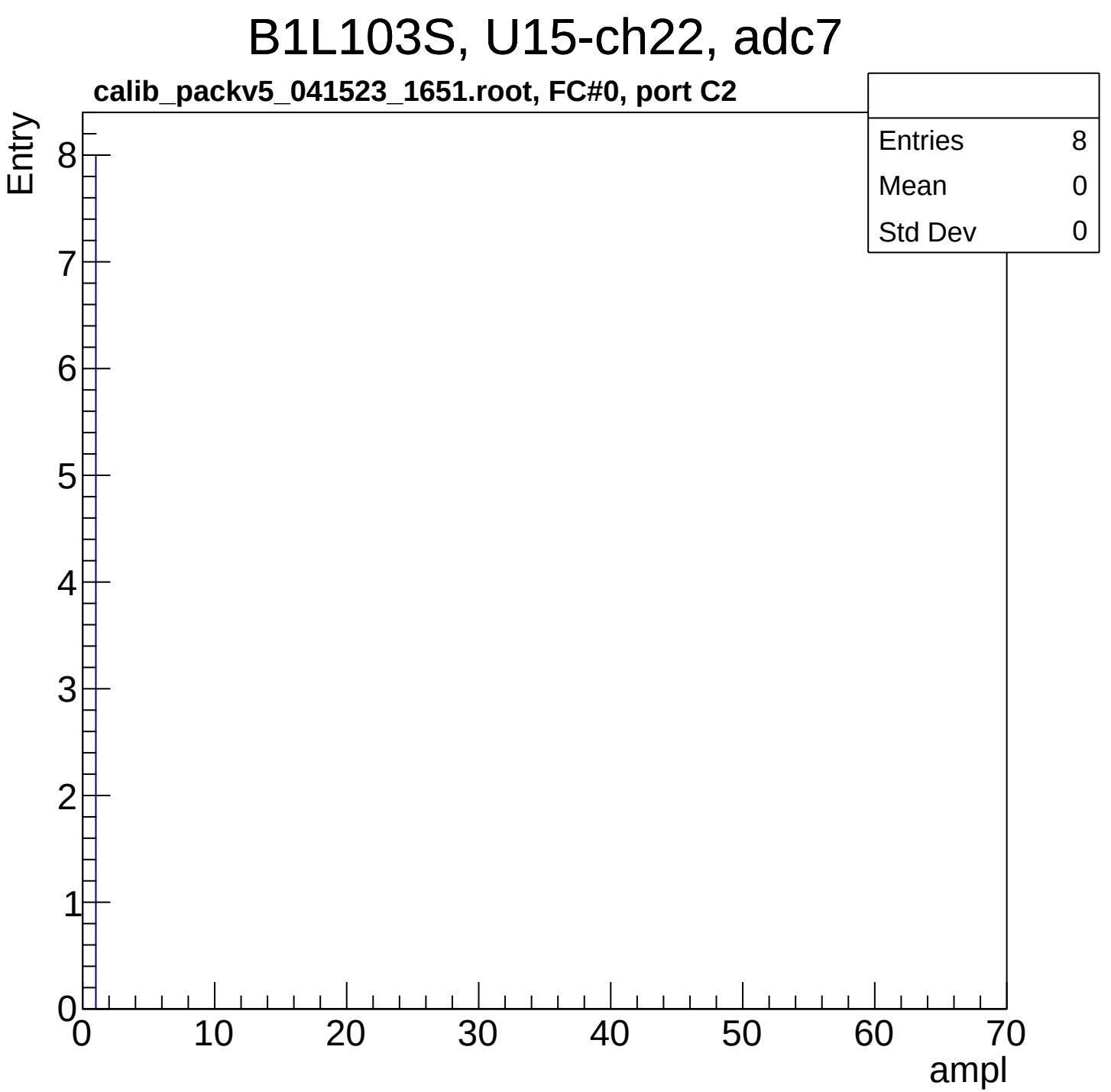
60
70


B1L103S, U15-ch22, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.3
Std Dev 2.002
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch22, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 0
Std Dev 0
Entry
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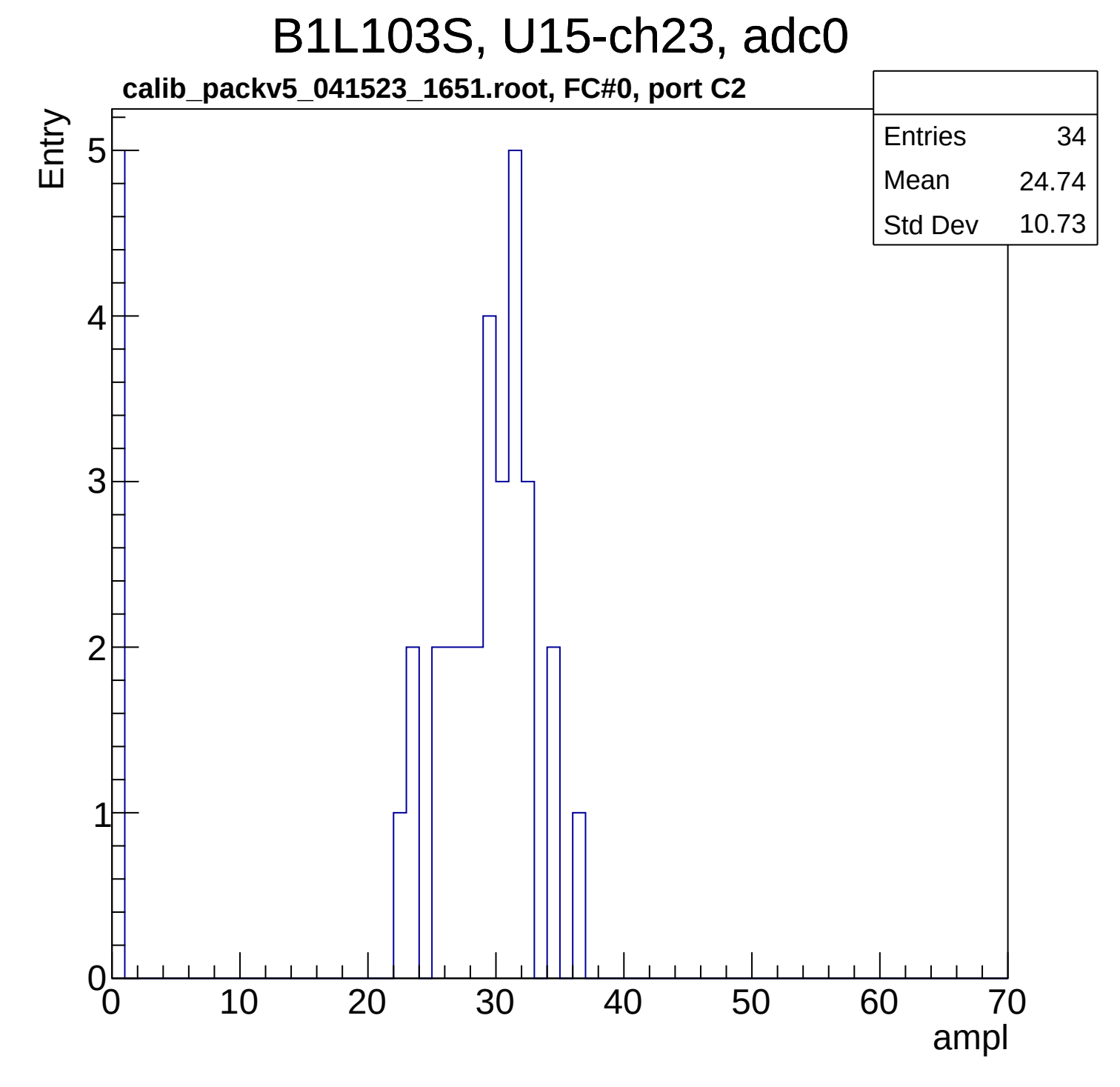
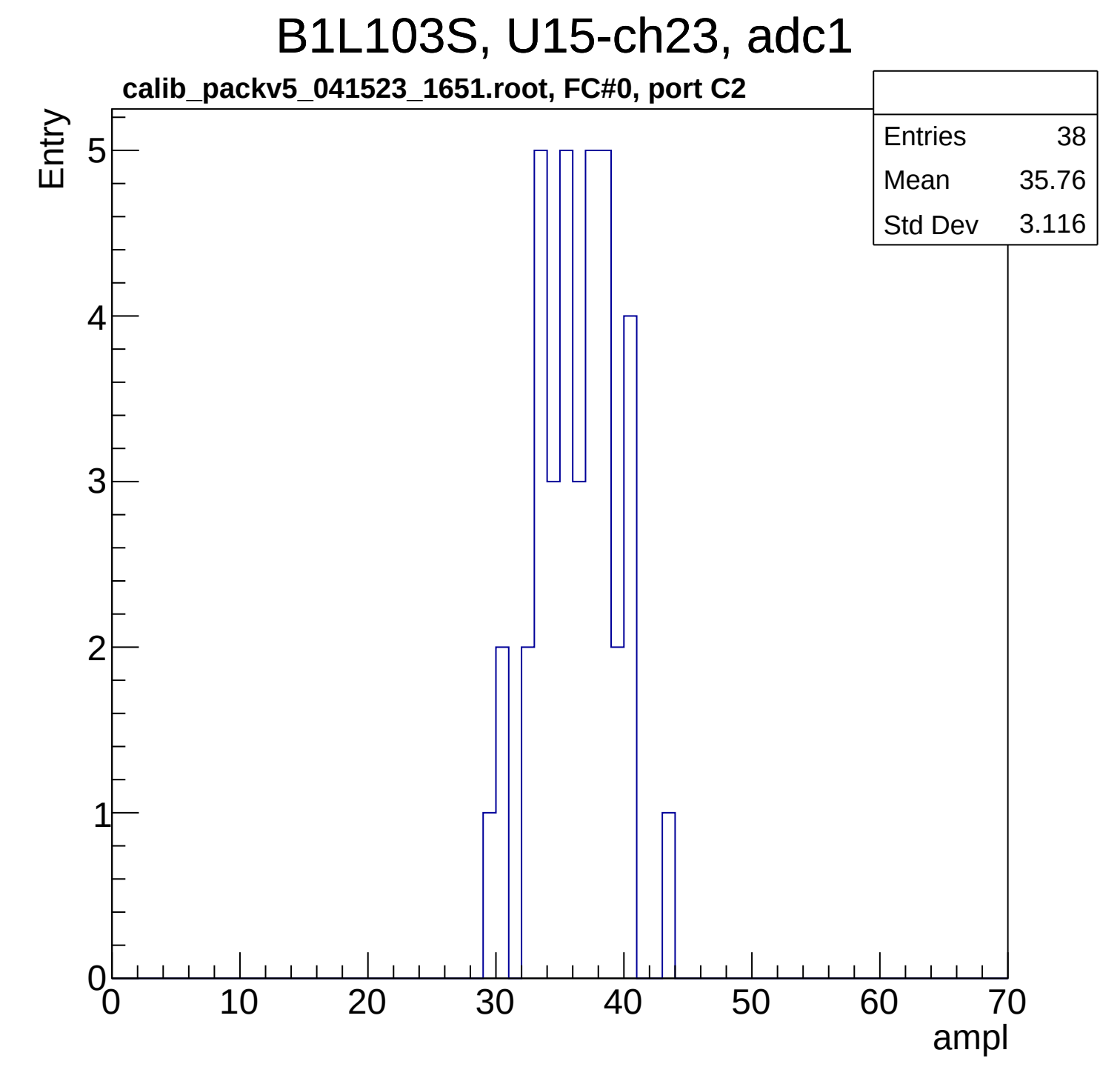
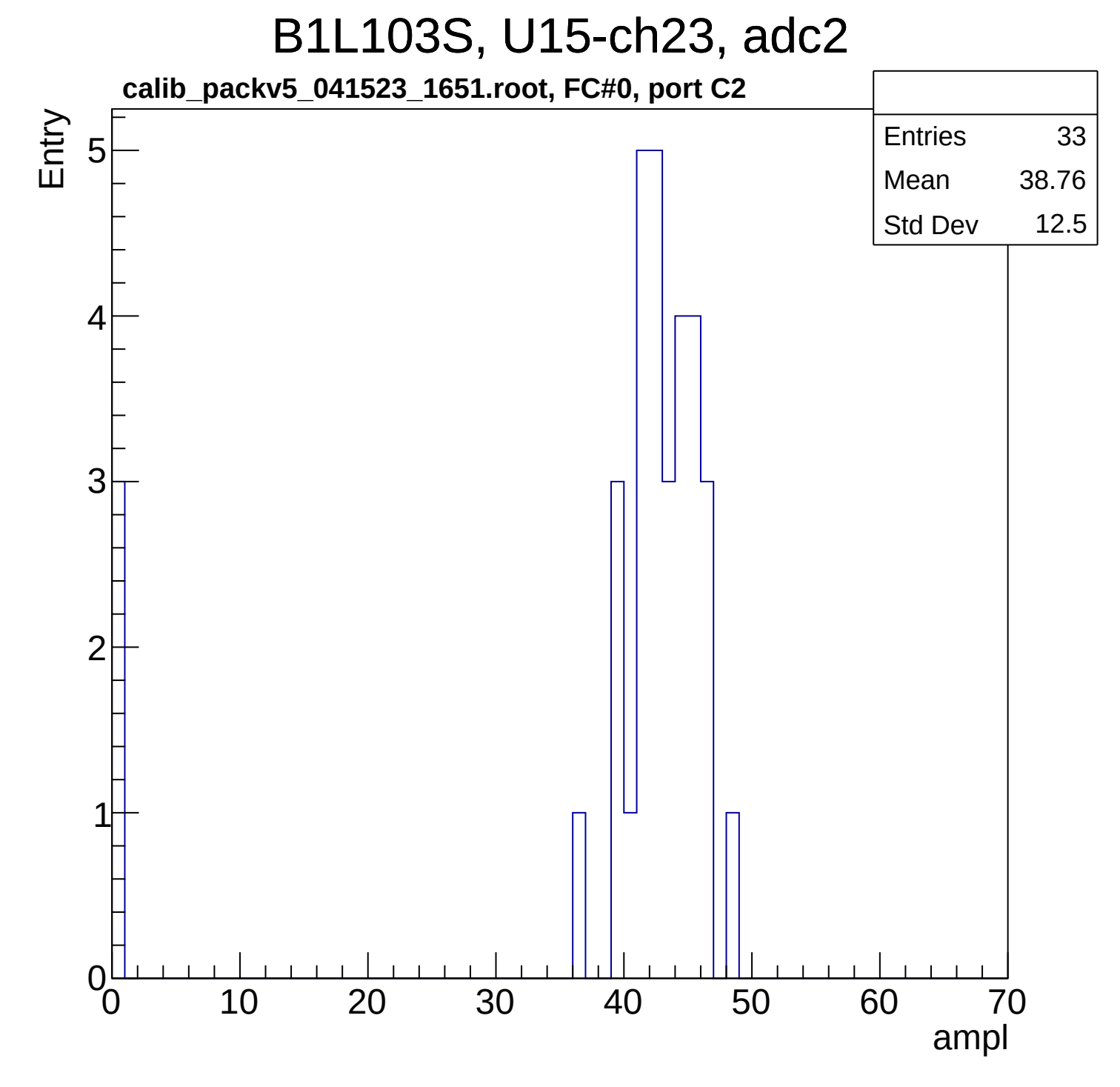
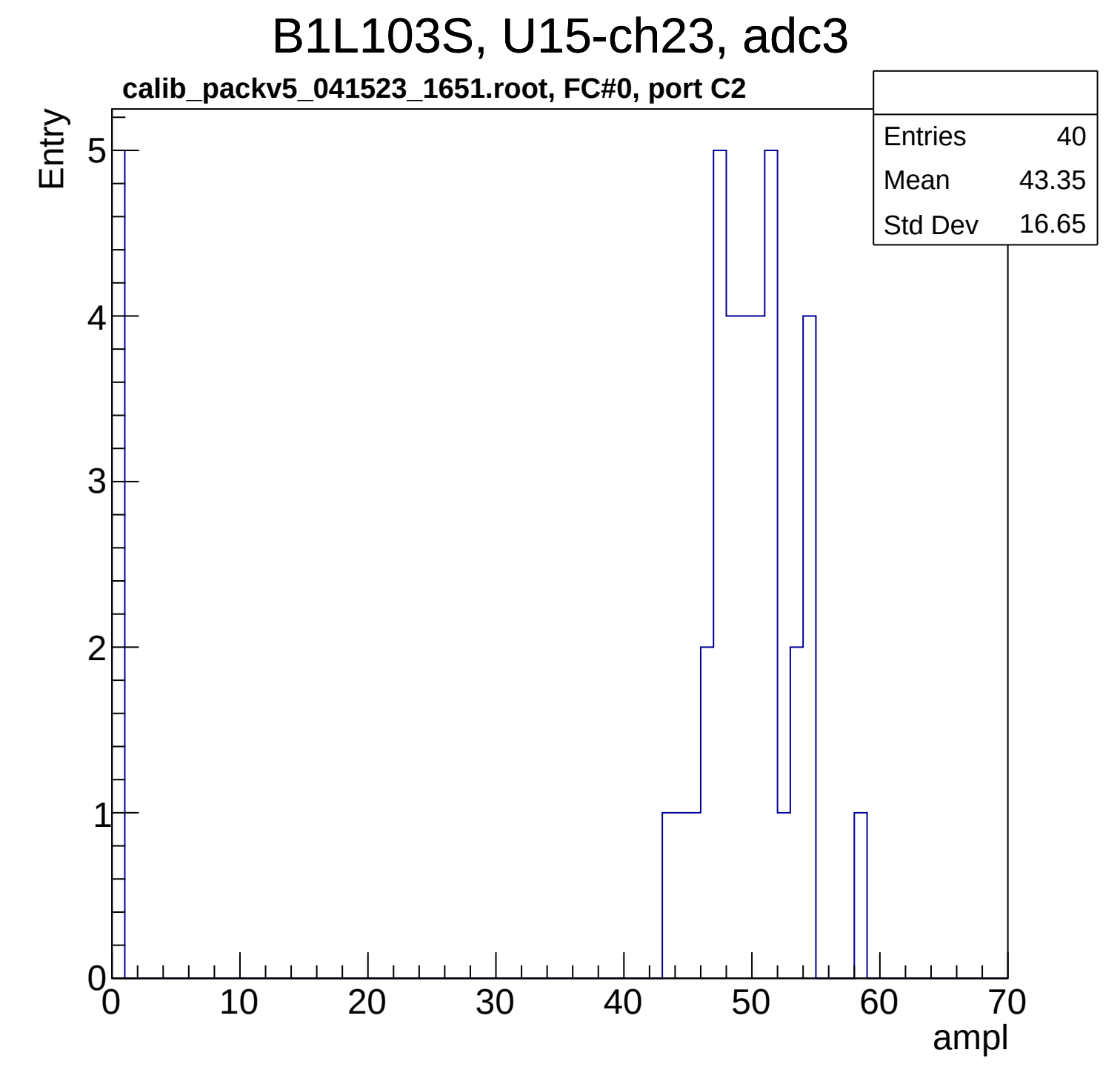
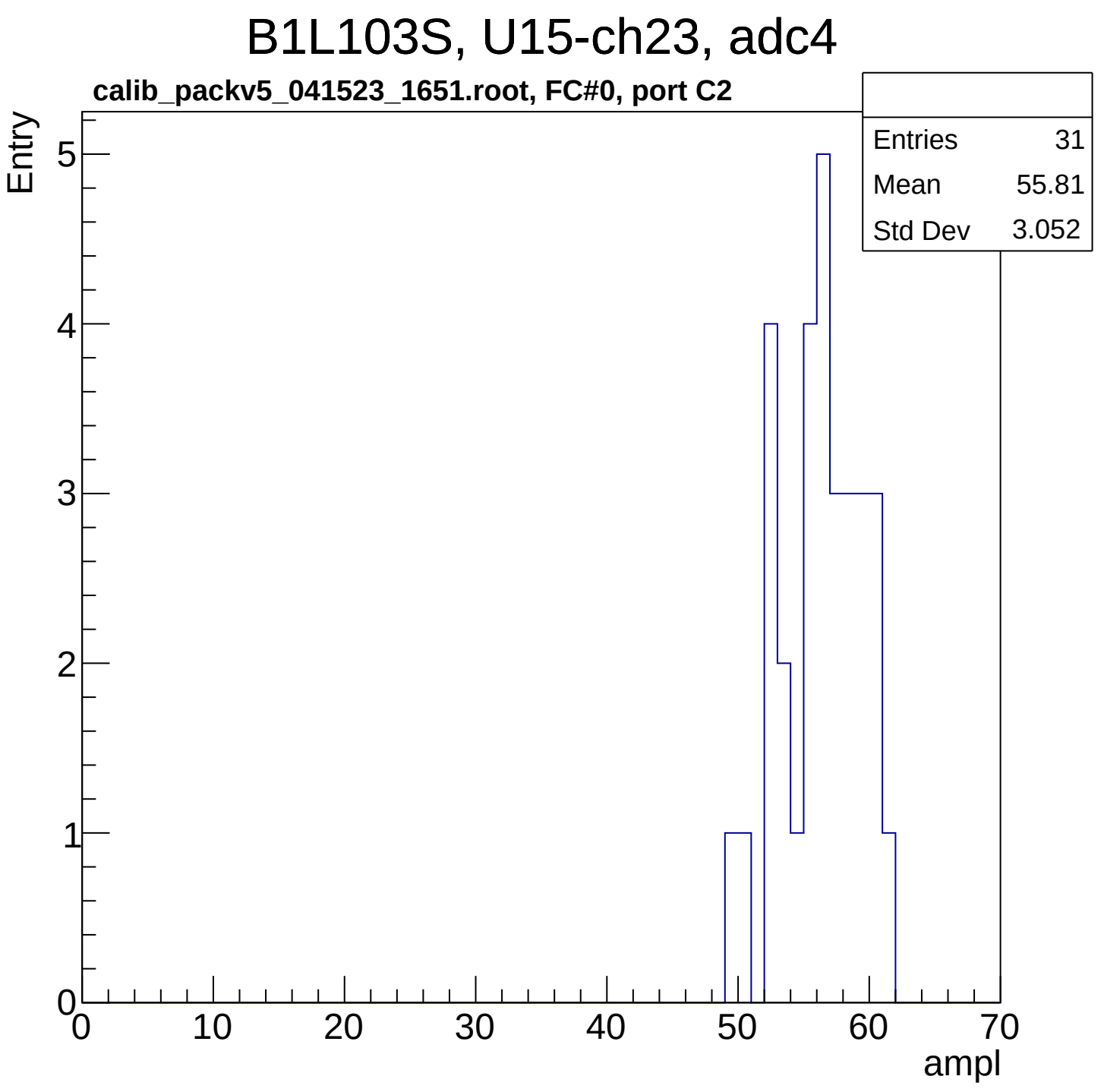
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

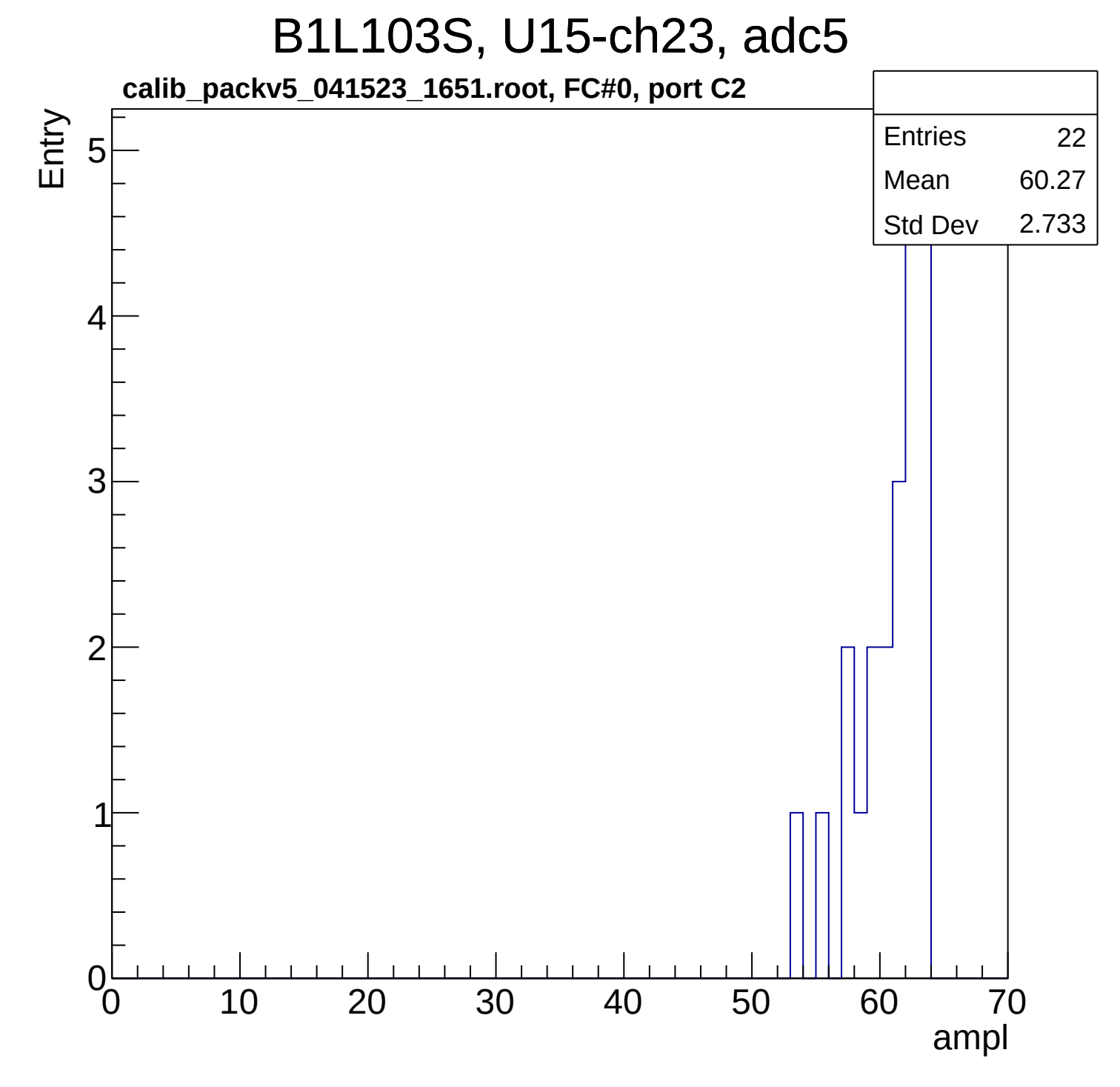

B1L103S, U15-ch23, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 24.74
Std Dev 10.73
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

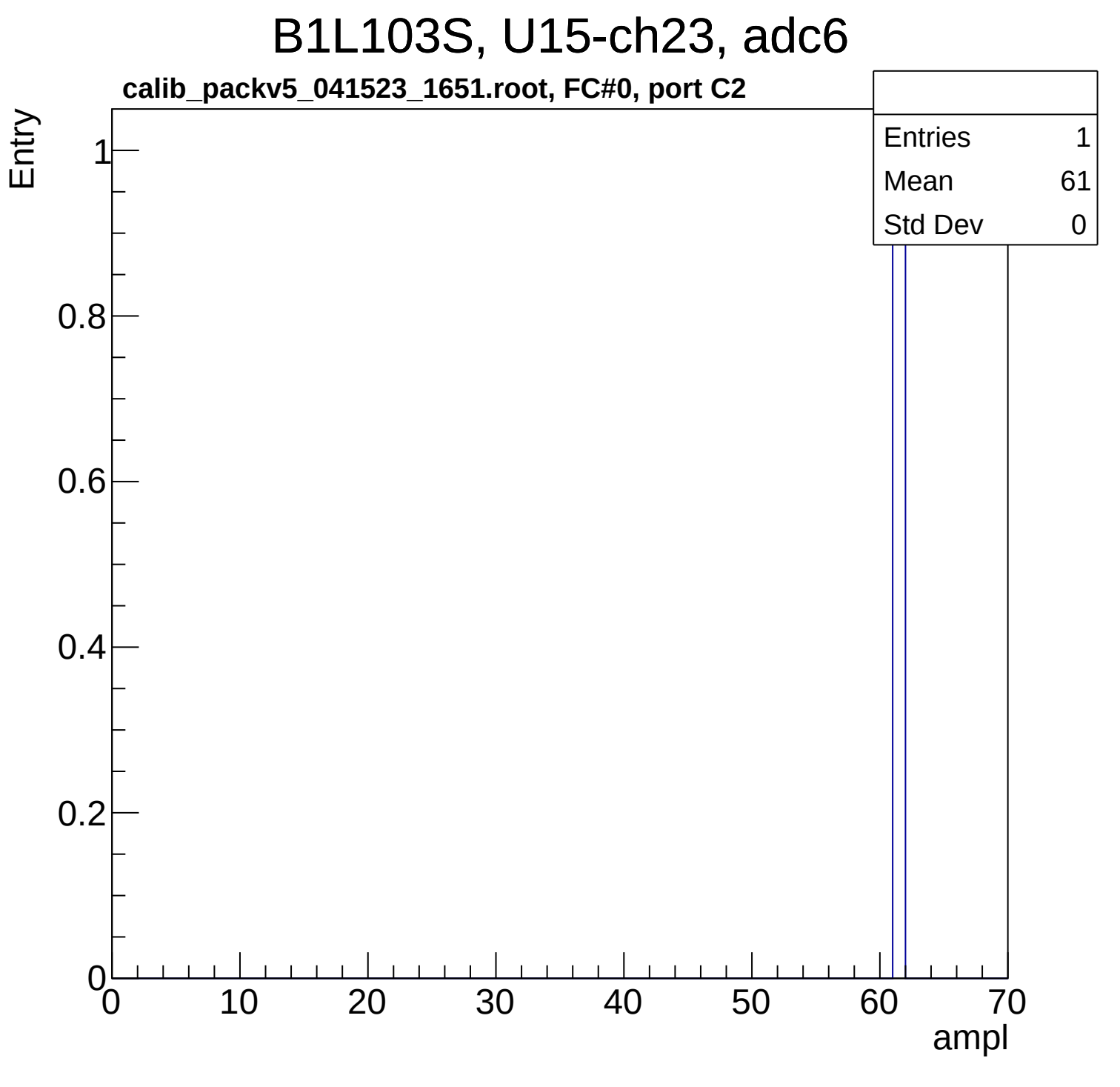

B1L103S, U15-ch23, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 35.76
Std Dev 3.116
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch23, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 38.76
Std Dev 12.5
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch23, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 43.35
Std Dev 16.65
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch23, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 55.81
Std Dev 3.052
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch23, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 60.27
Std Dev 2.733
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch23, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 61
Std Dev 0
Entry
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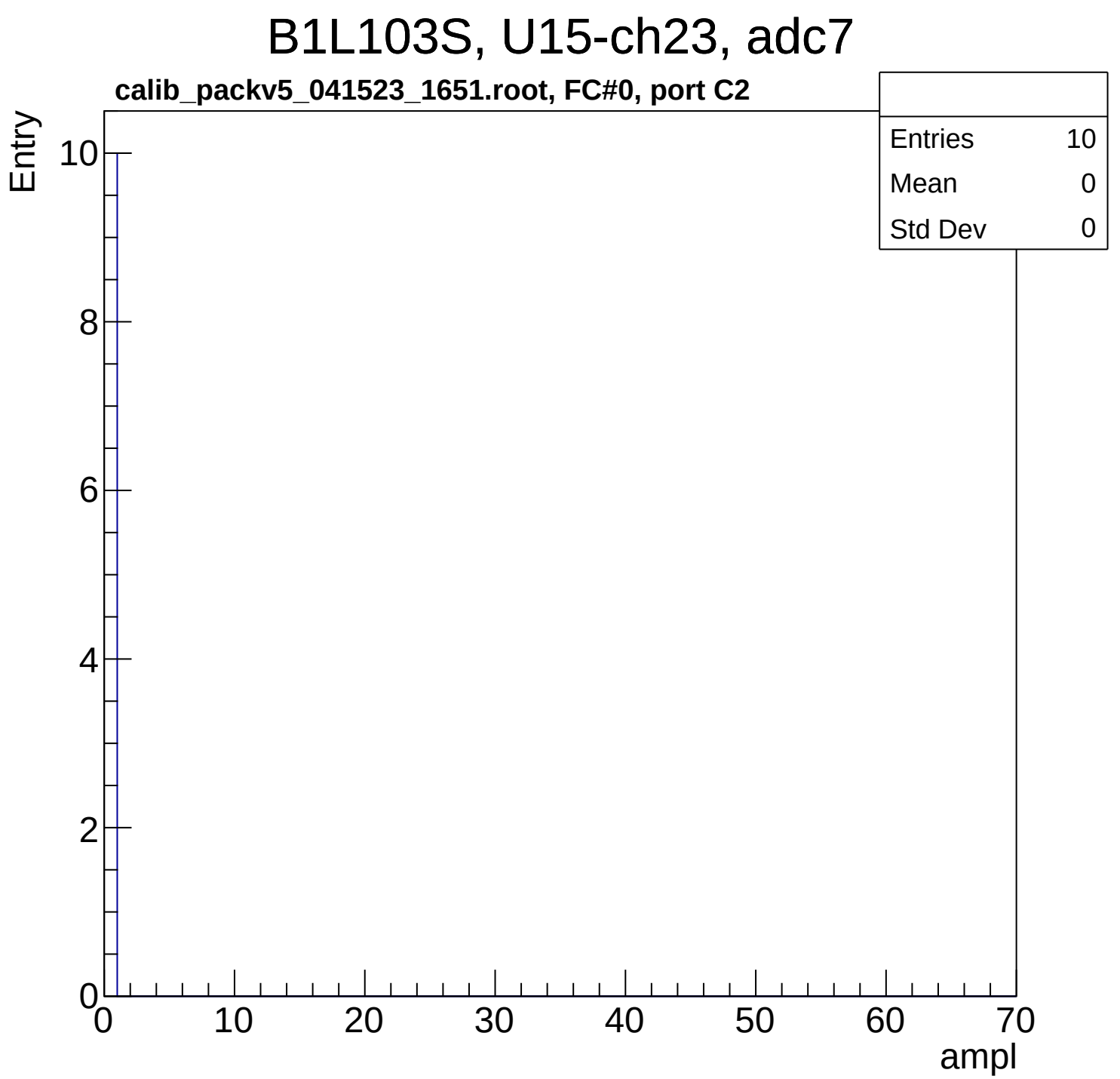
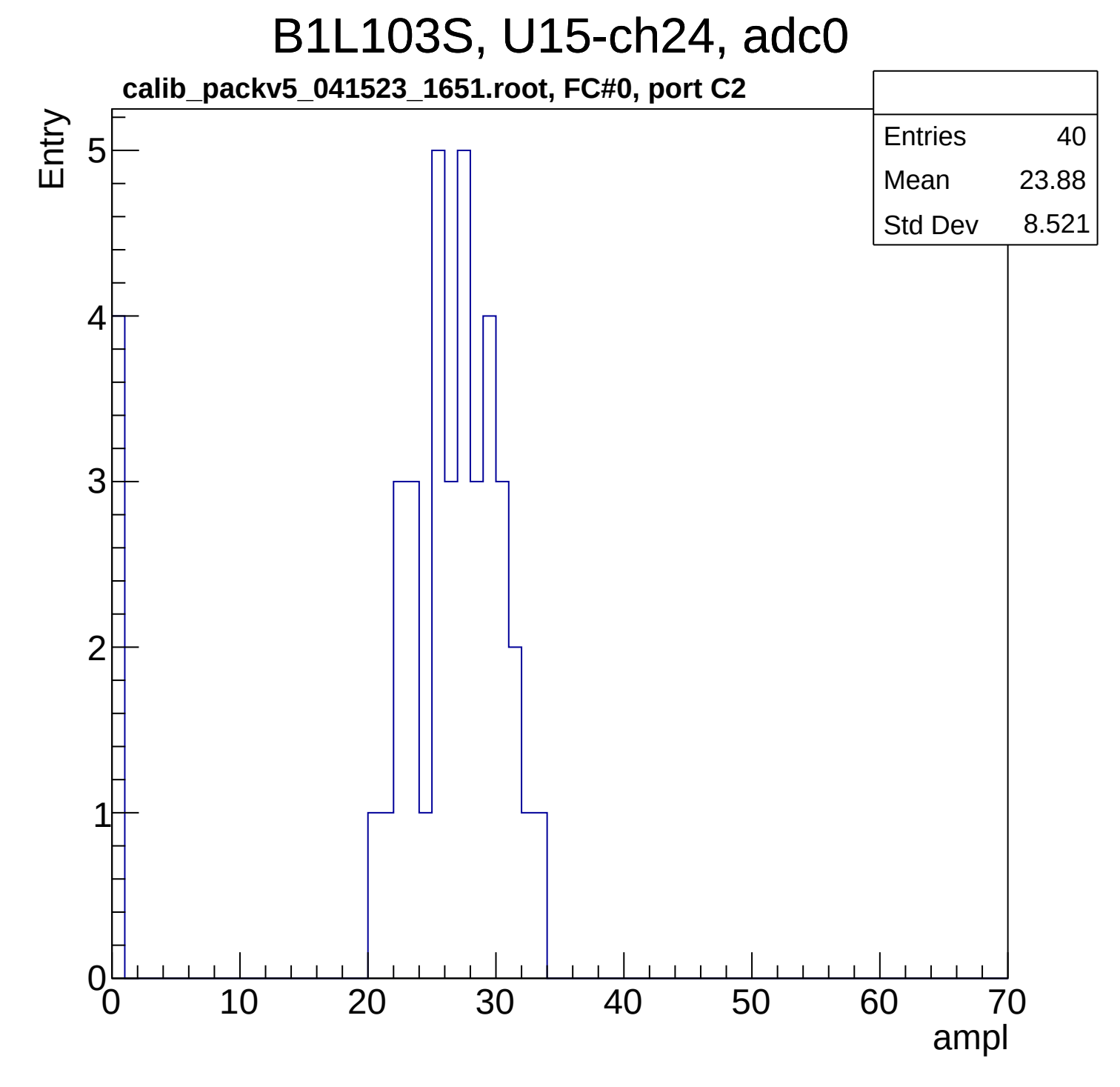
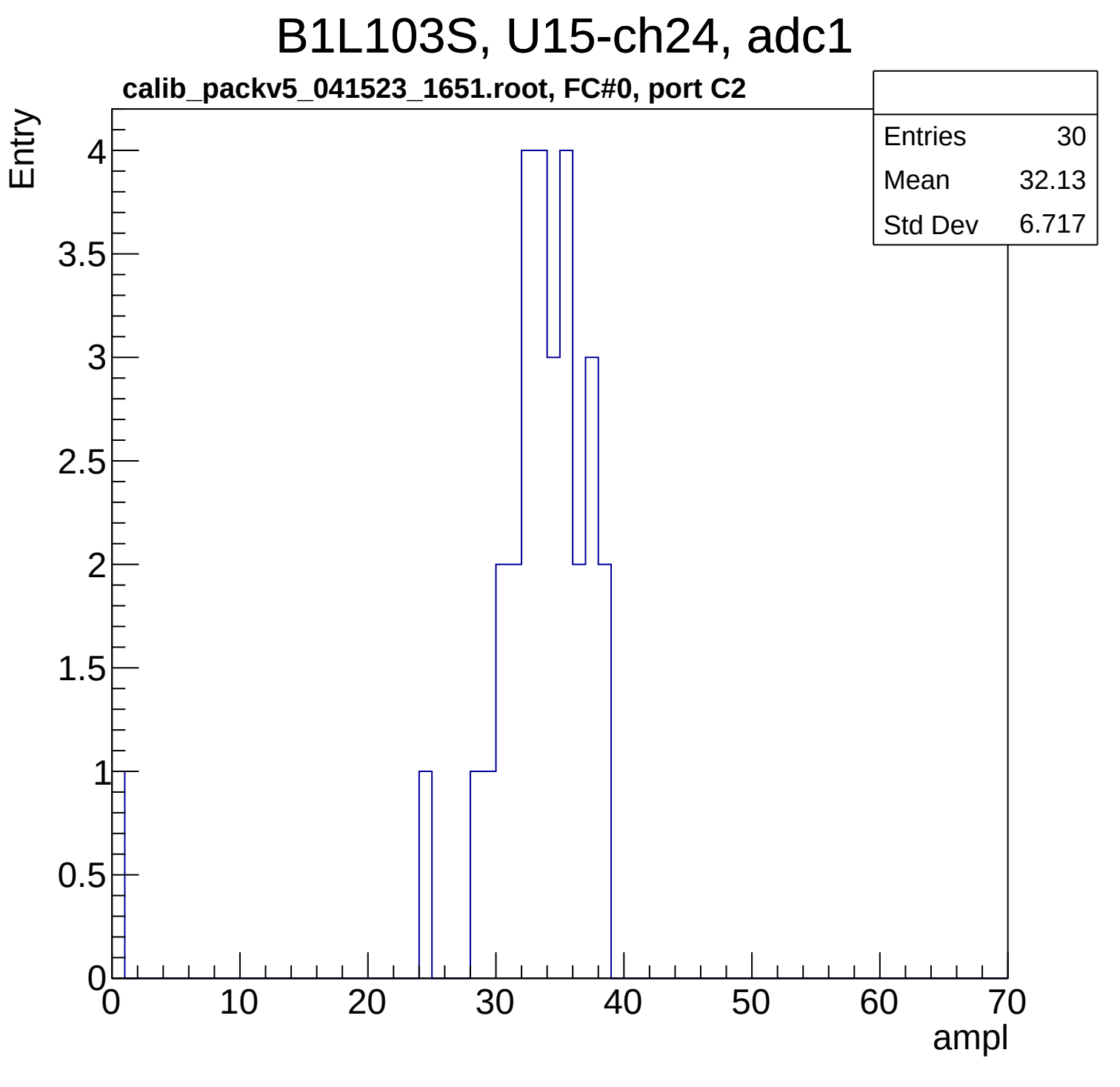
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch23, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch24, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 23.88
Std Dev 8.521
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch24, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 32.13
Std Dev 6.717
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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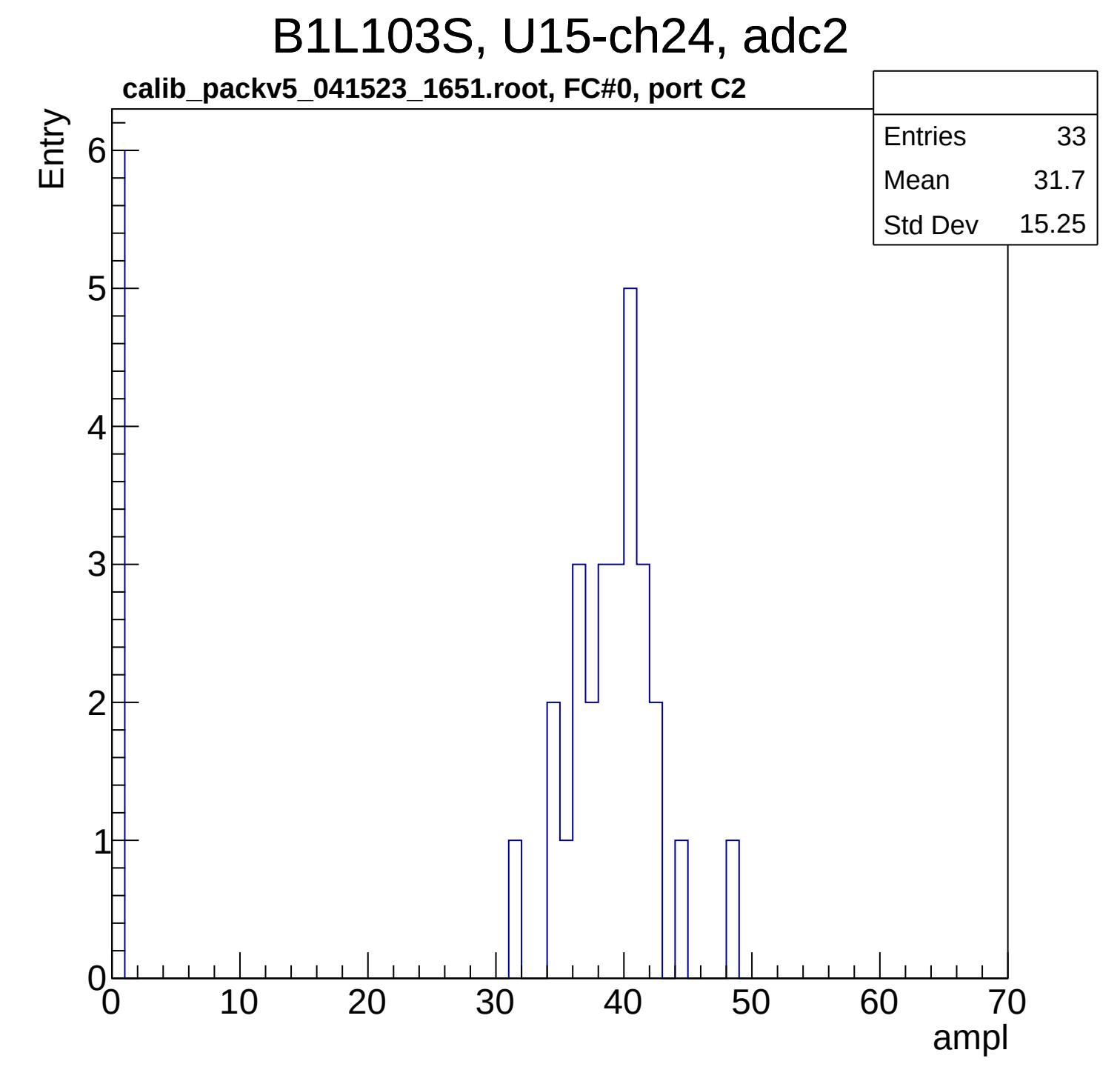
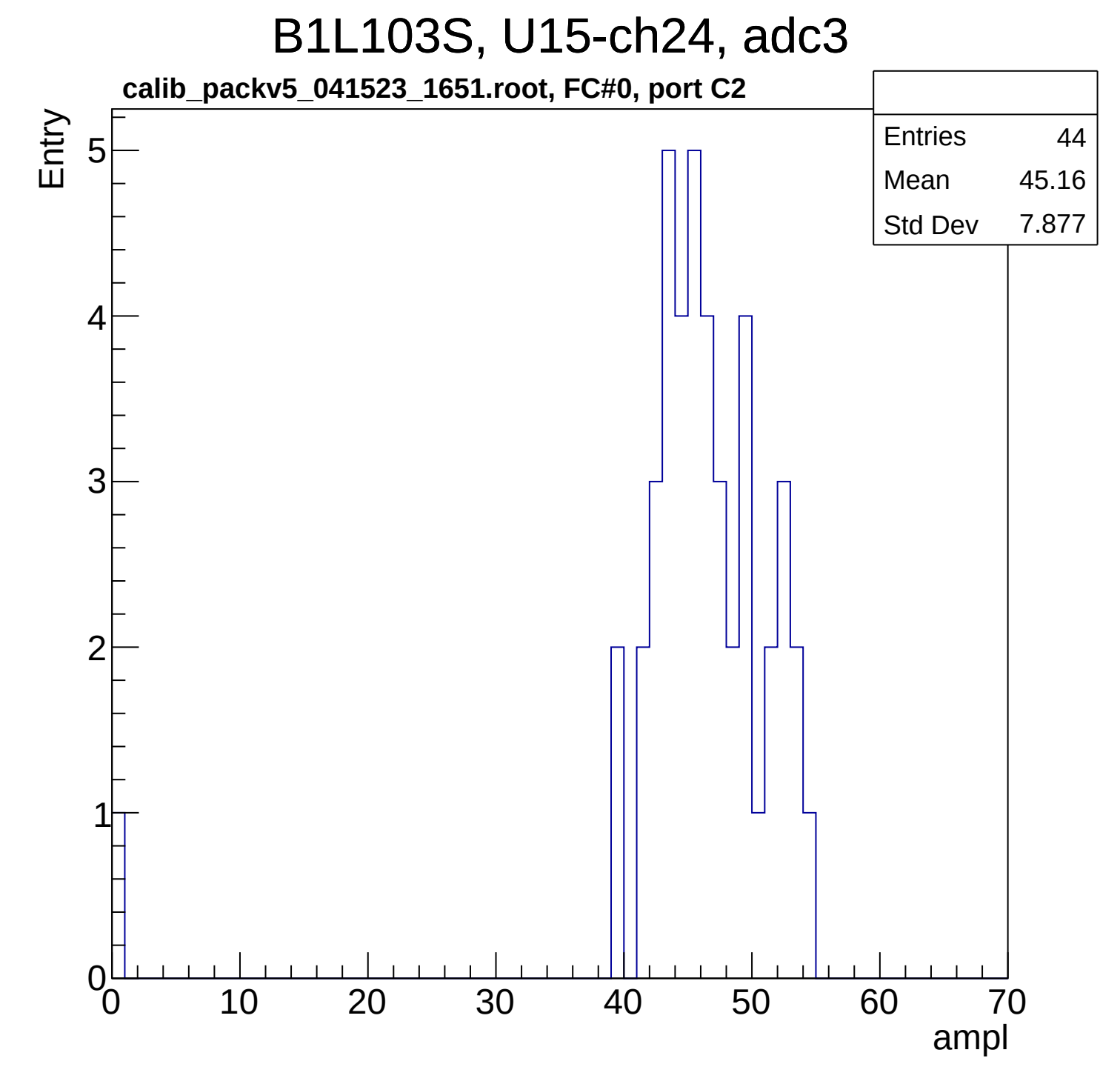
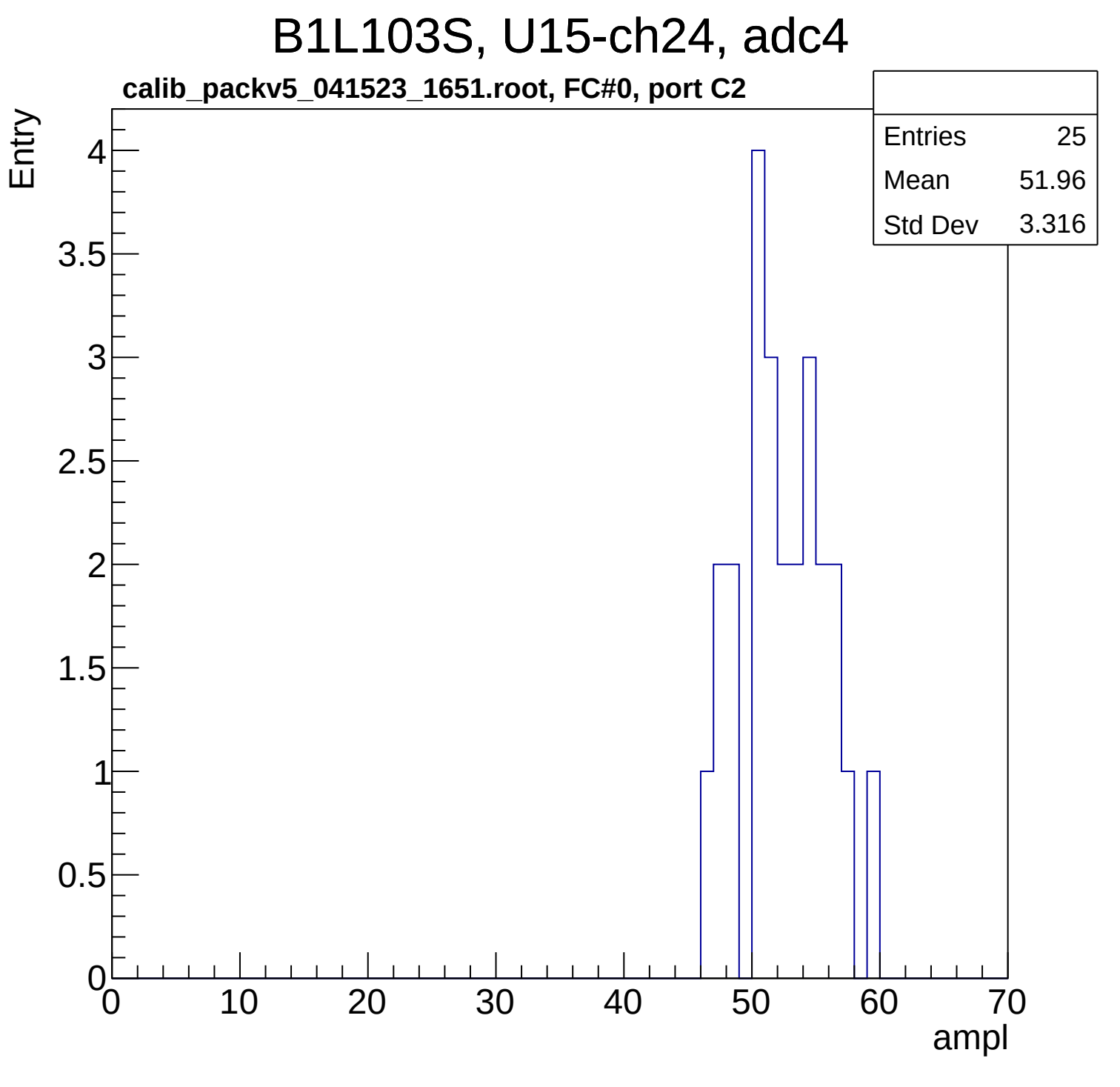

B1L103S, U15-ch24, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 31.7
Std Dev 15.25
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch24, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 45.16
Std Dev 7.877
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch24, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 51.96
Std Dev 3.316
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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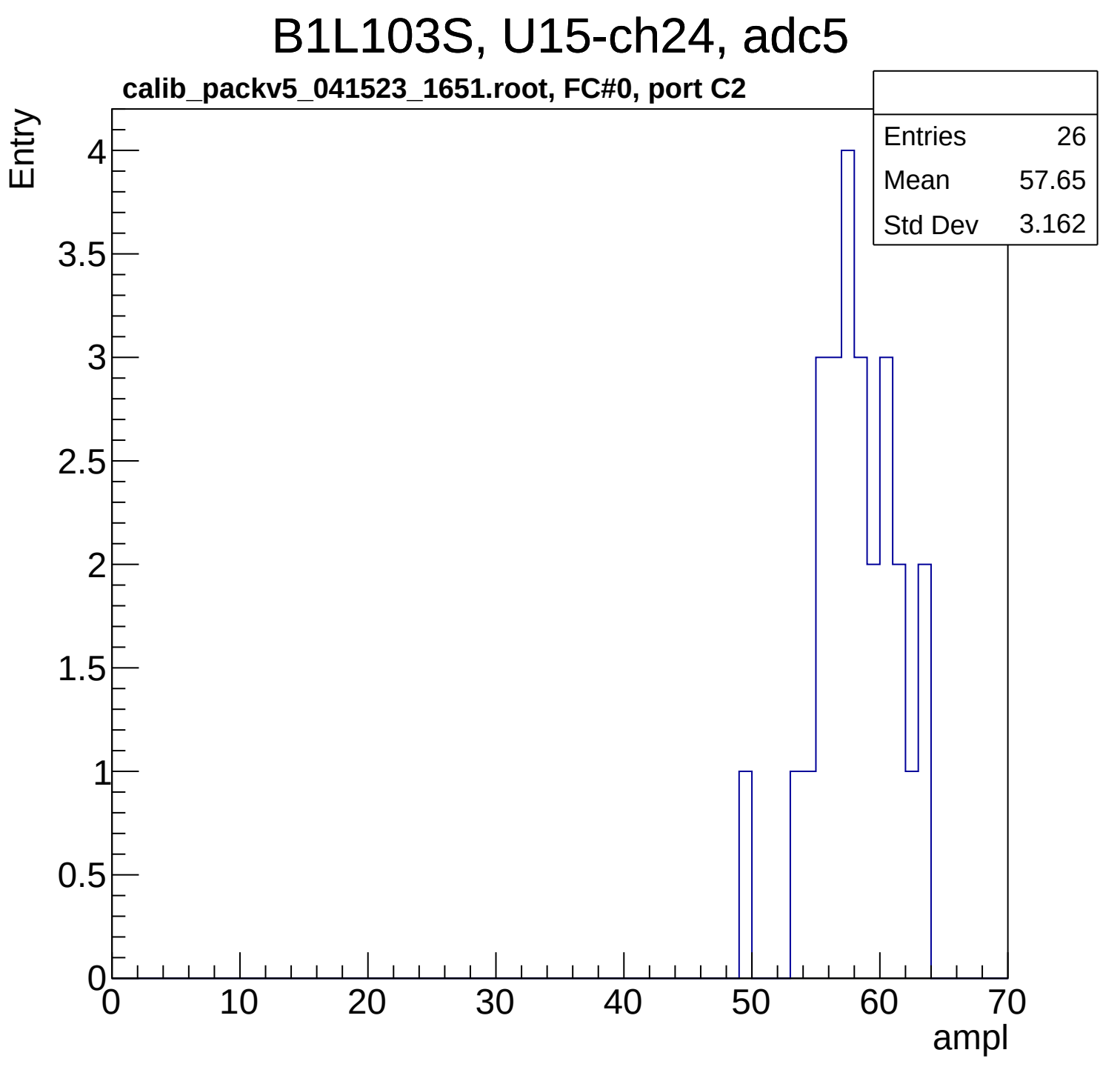
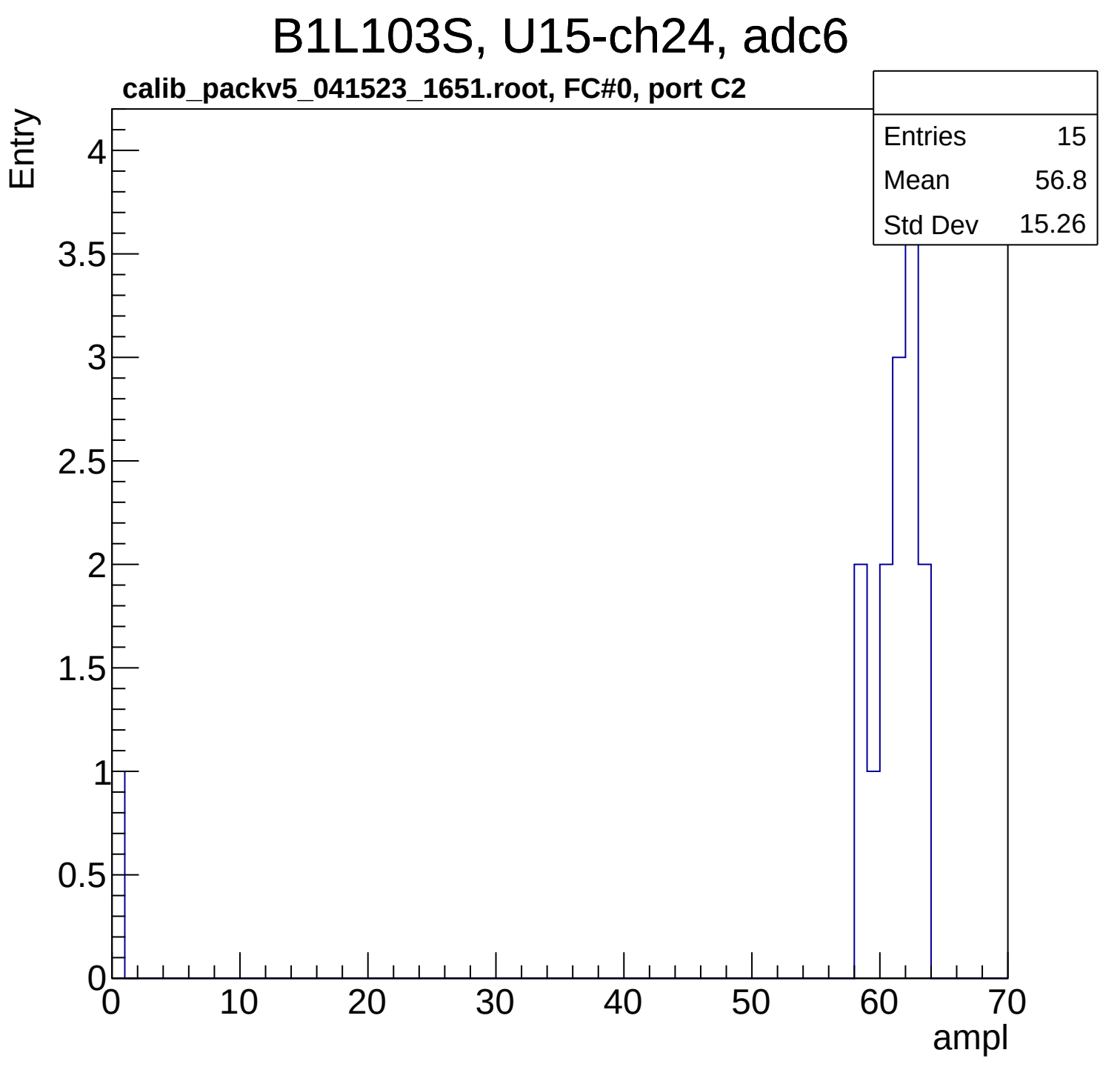
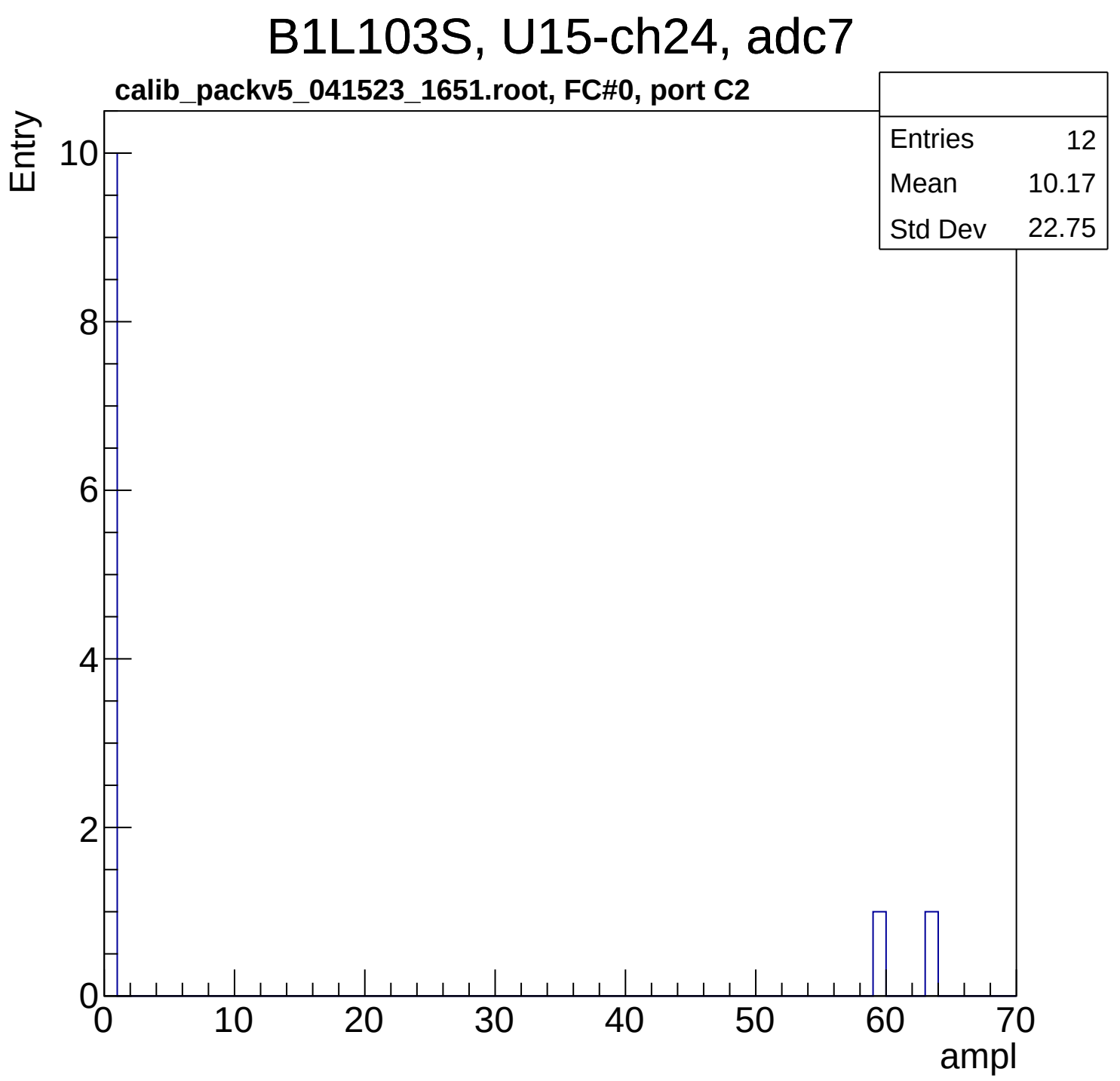
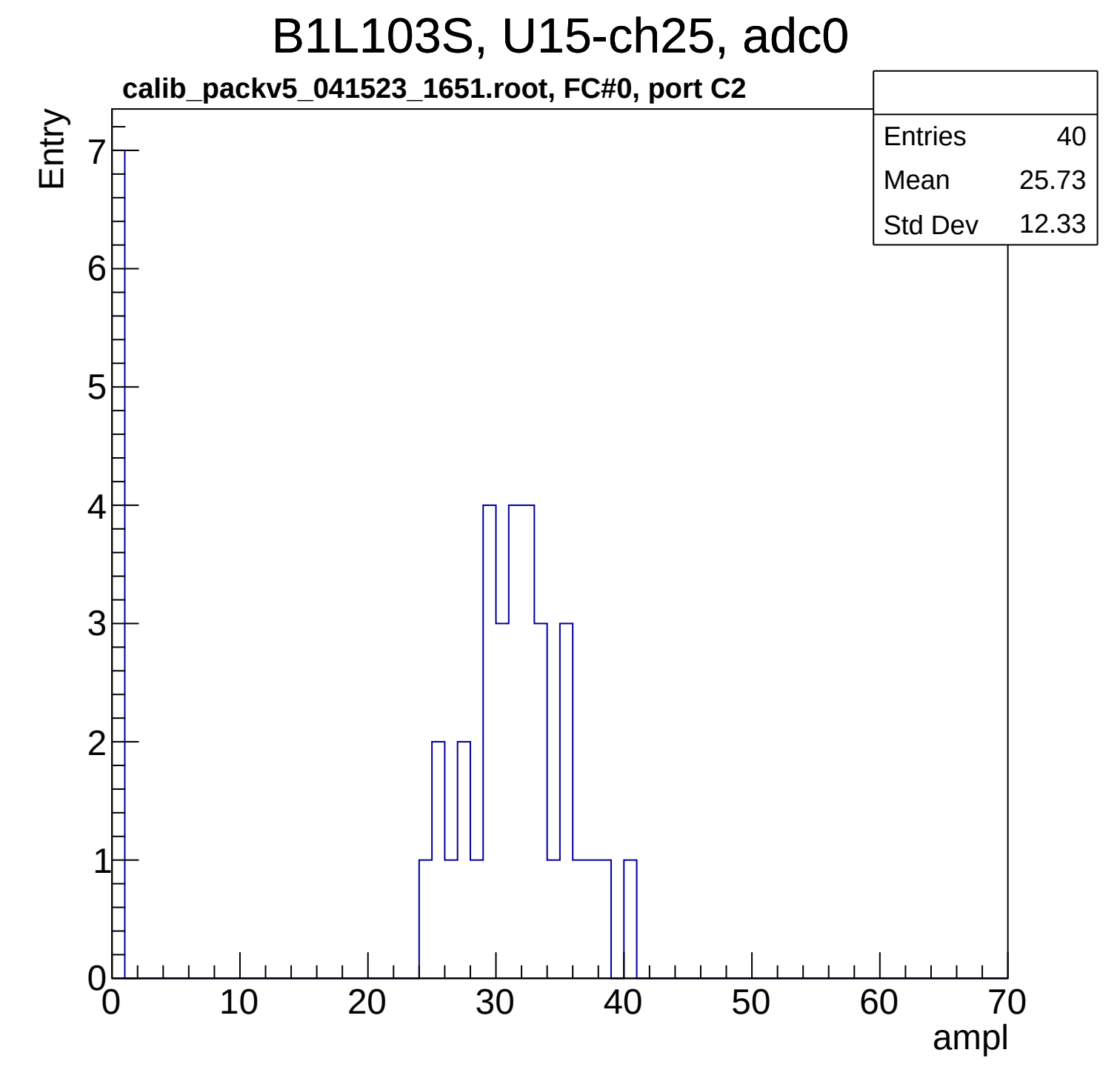
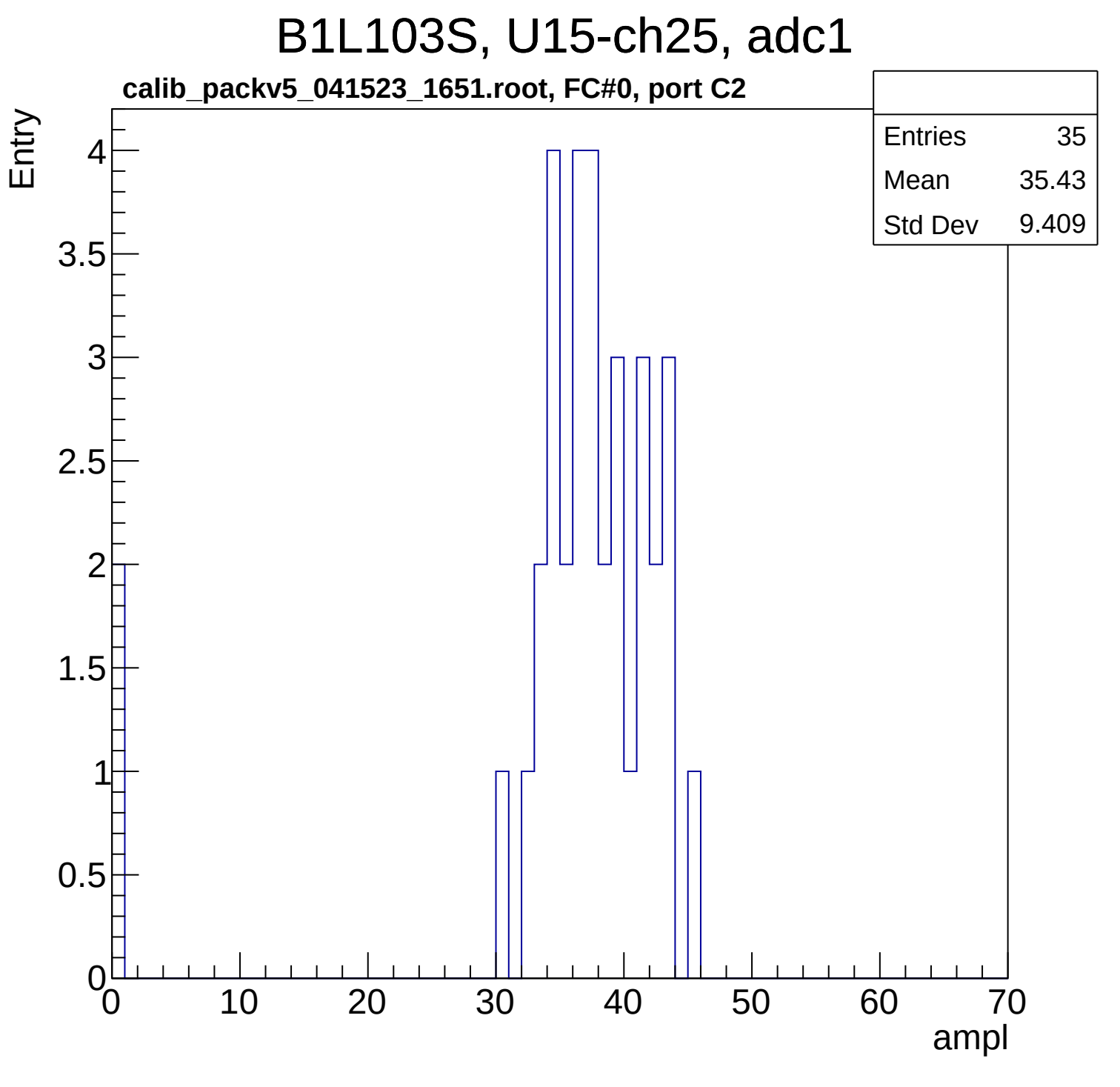
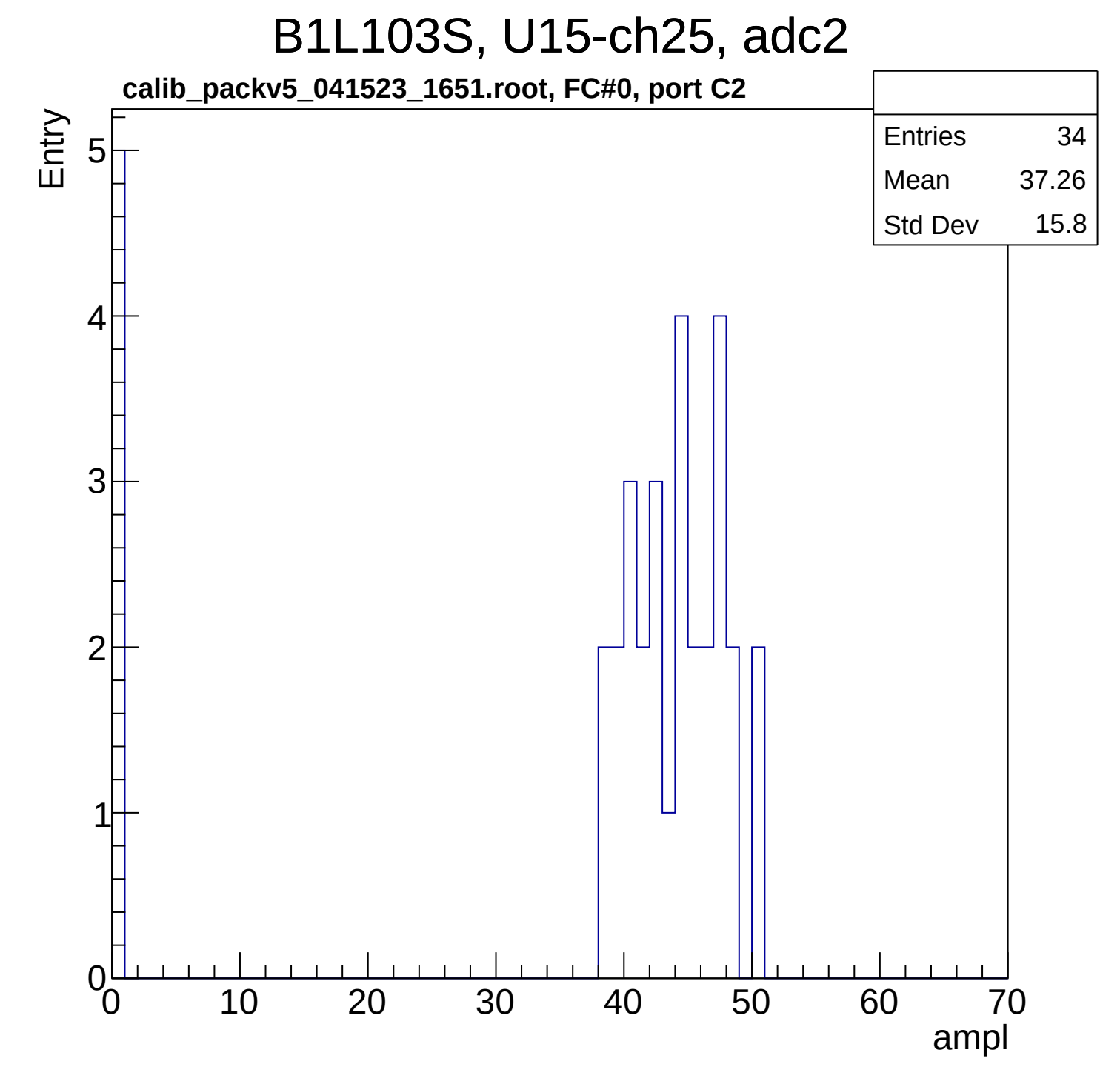

B1L103S, U15-ch24, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 57.65
Std Dev 3.162
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

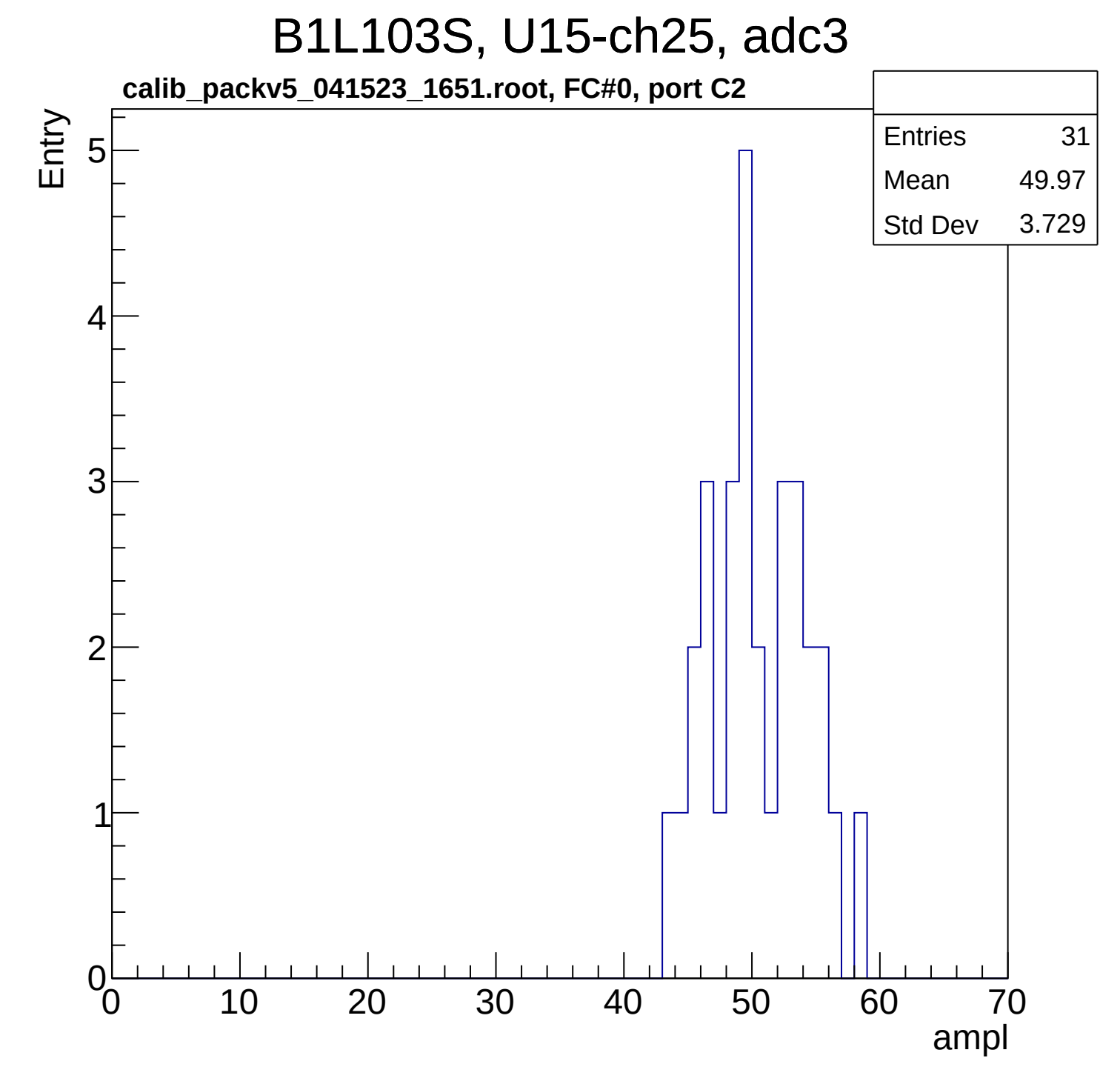

B1L103S, U15-ch24, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 56.8
Std Dev 15.26
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

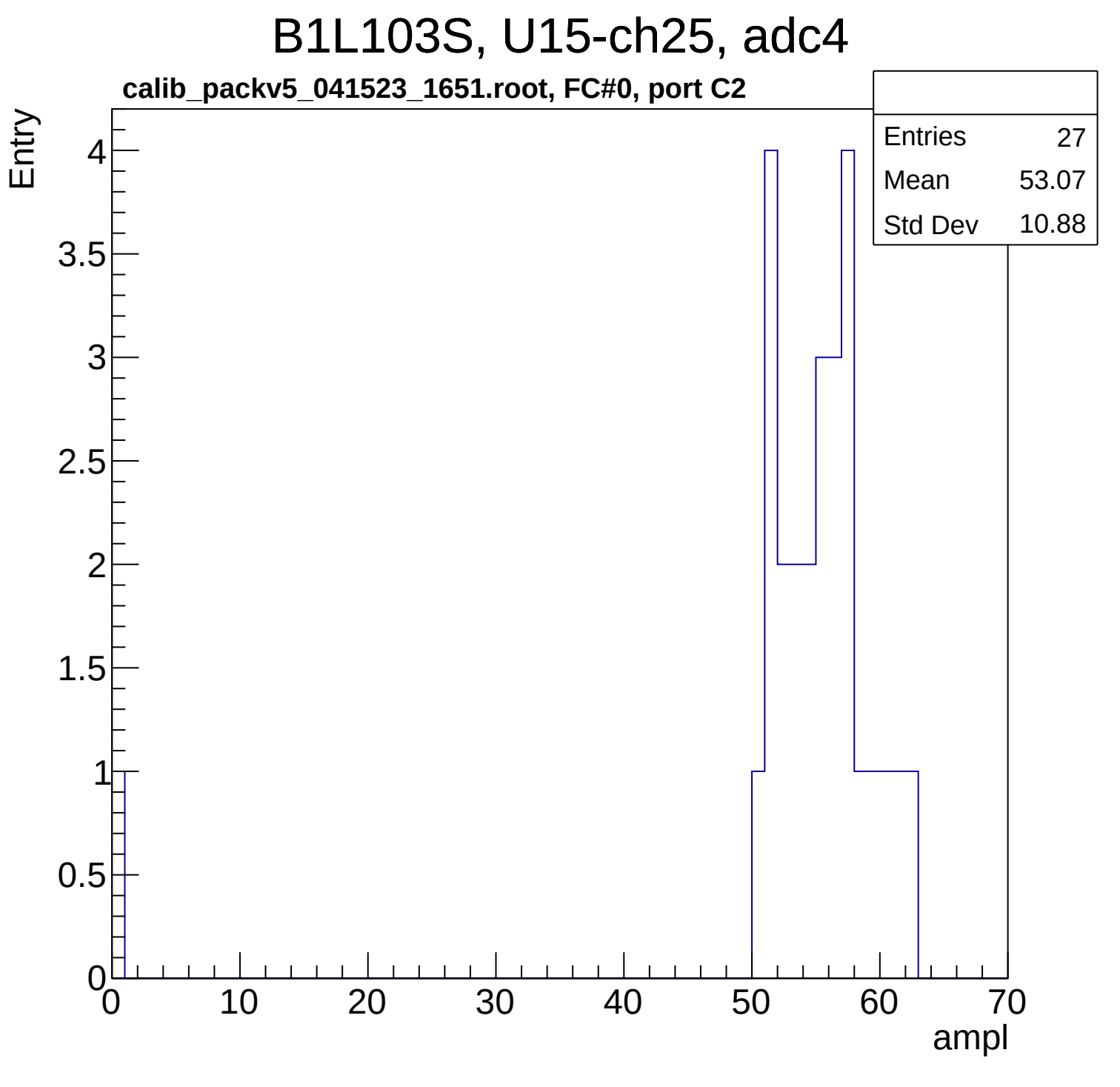

B1L103S, U15-ch24, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 10.17
Std Dev 22.75
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

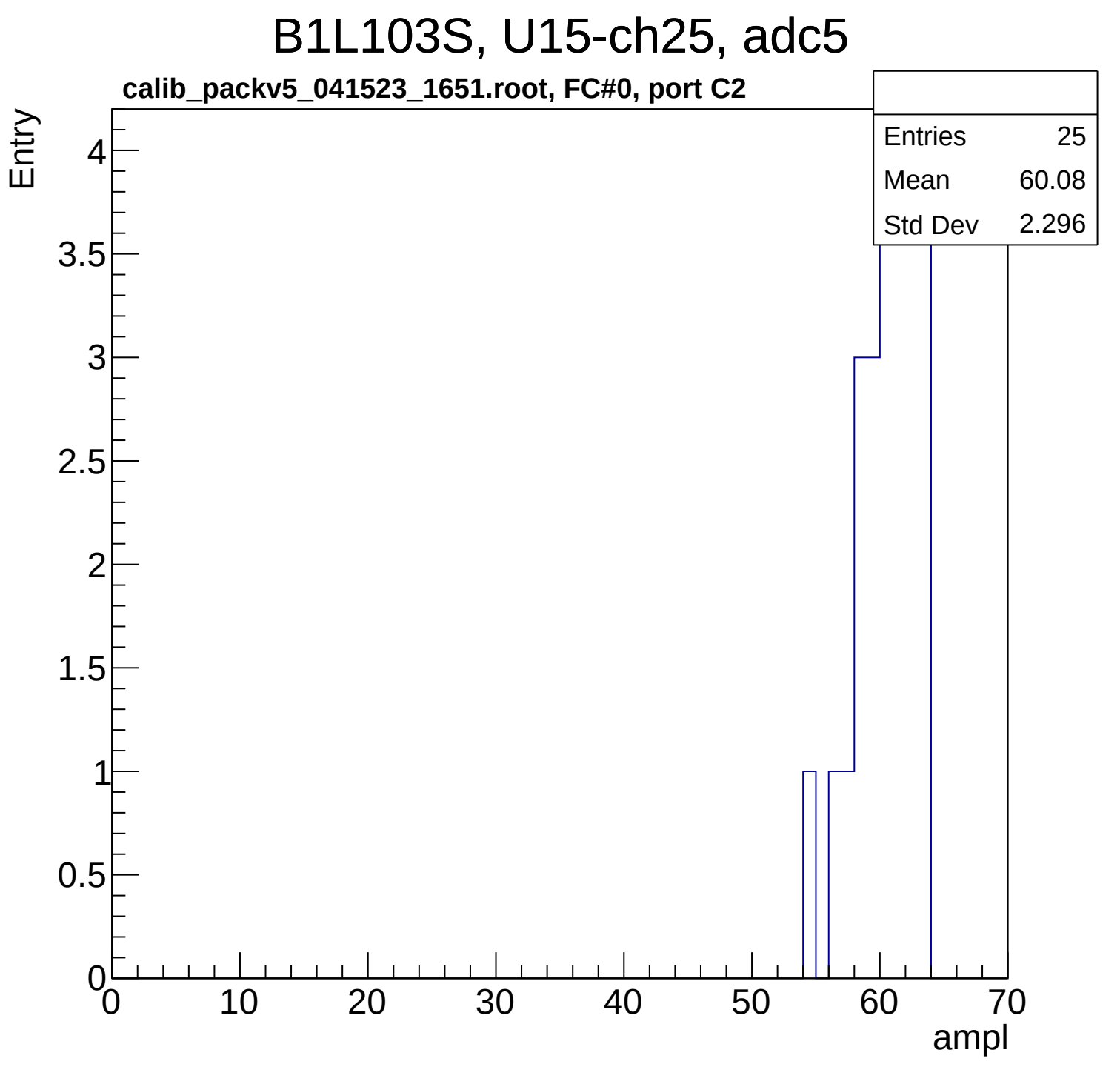

B1L103S, U15-ch25, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 25.73
Std Dev 12.33
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U15-ch25, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 35.43
Std Dev 9.409
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch25, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 37.26
Std Dev 15.8
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch25, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 49.97
Std Dev 3.729
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch25, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 53.07
Std Dev 10.88
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch25, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 60.08
Std Dev 2.296
Entry
ampl
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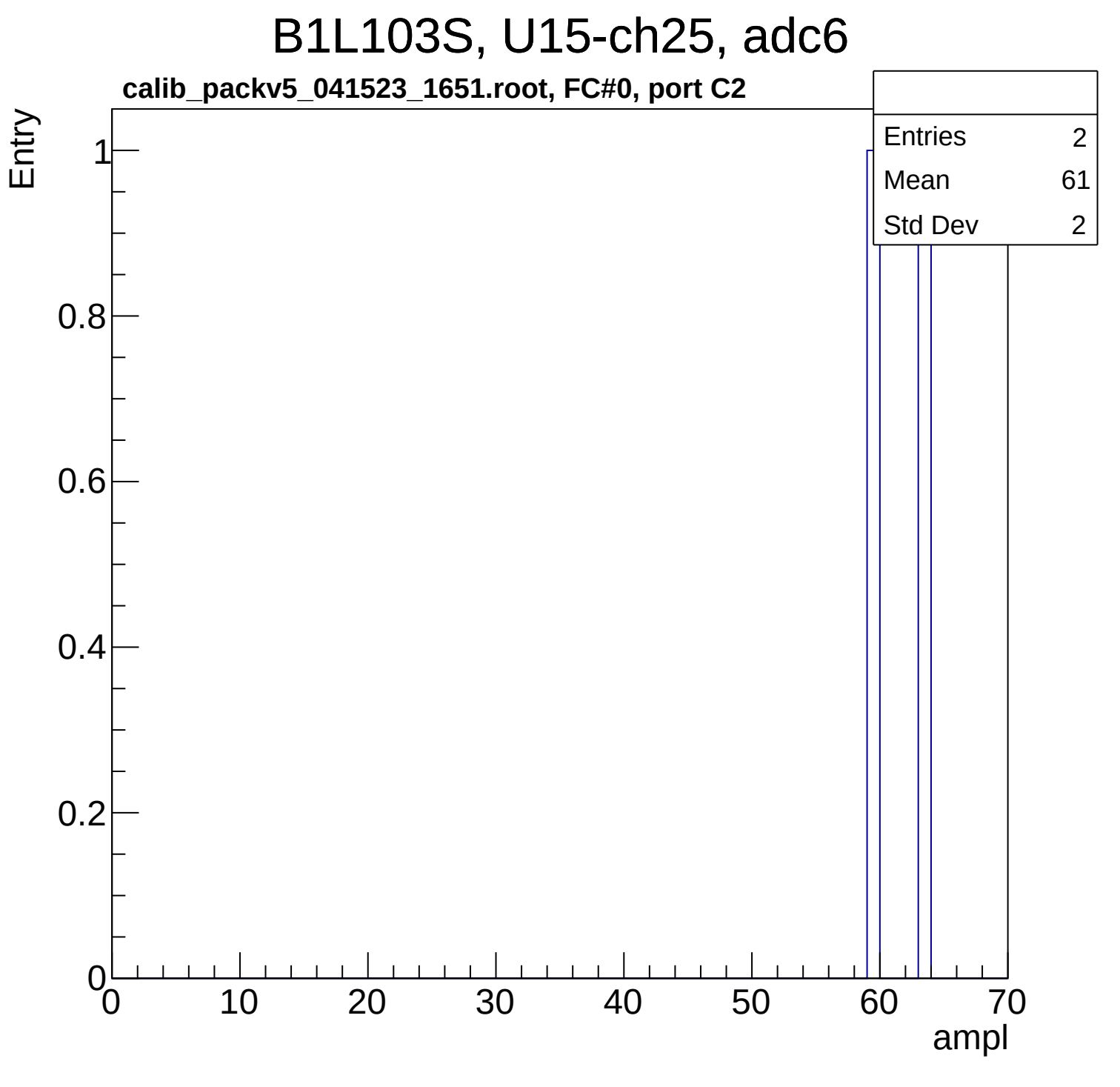
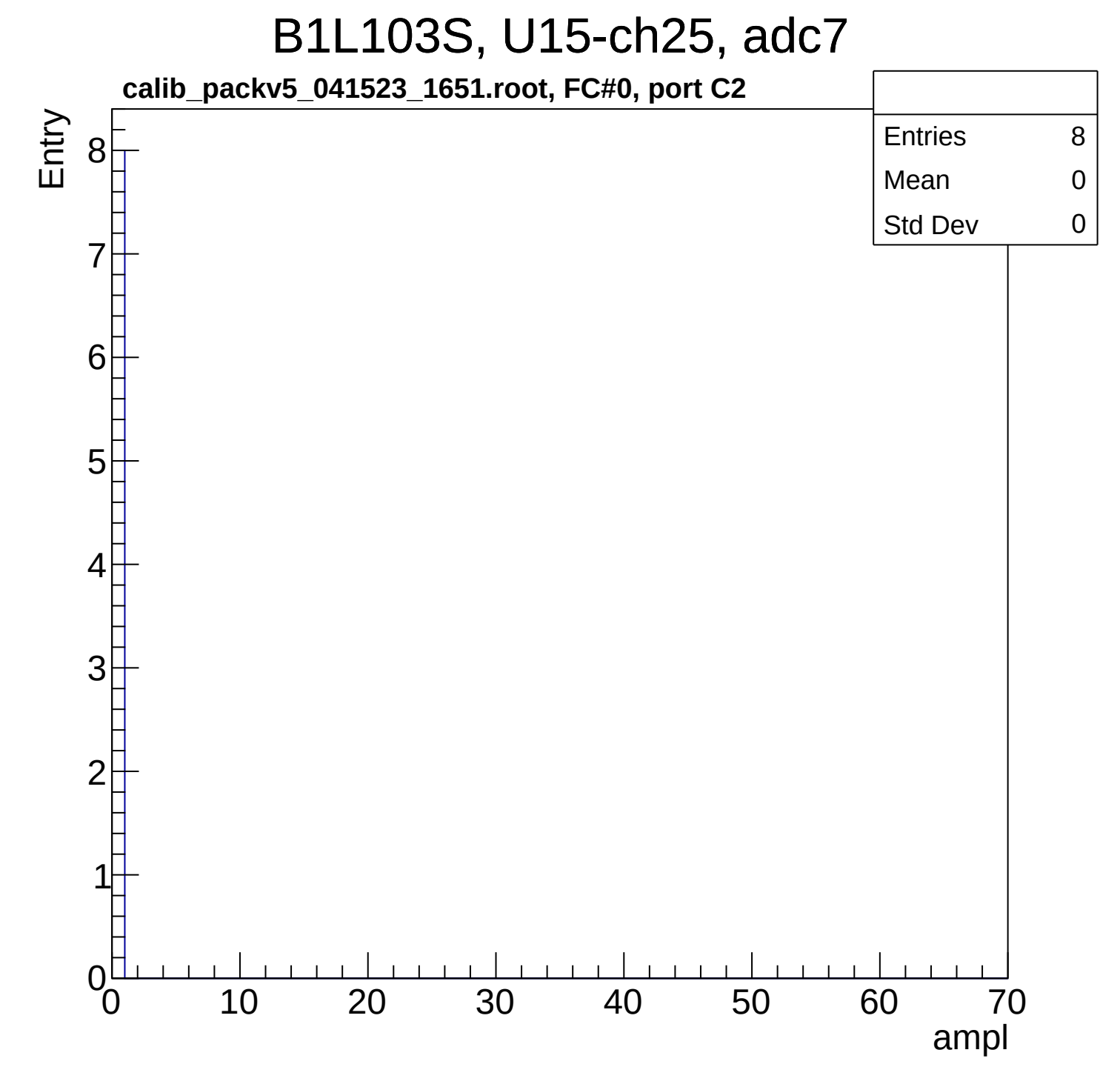
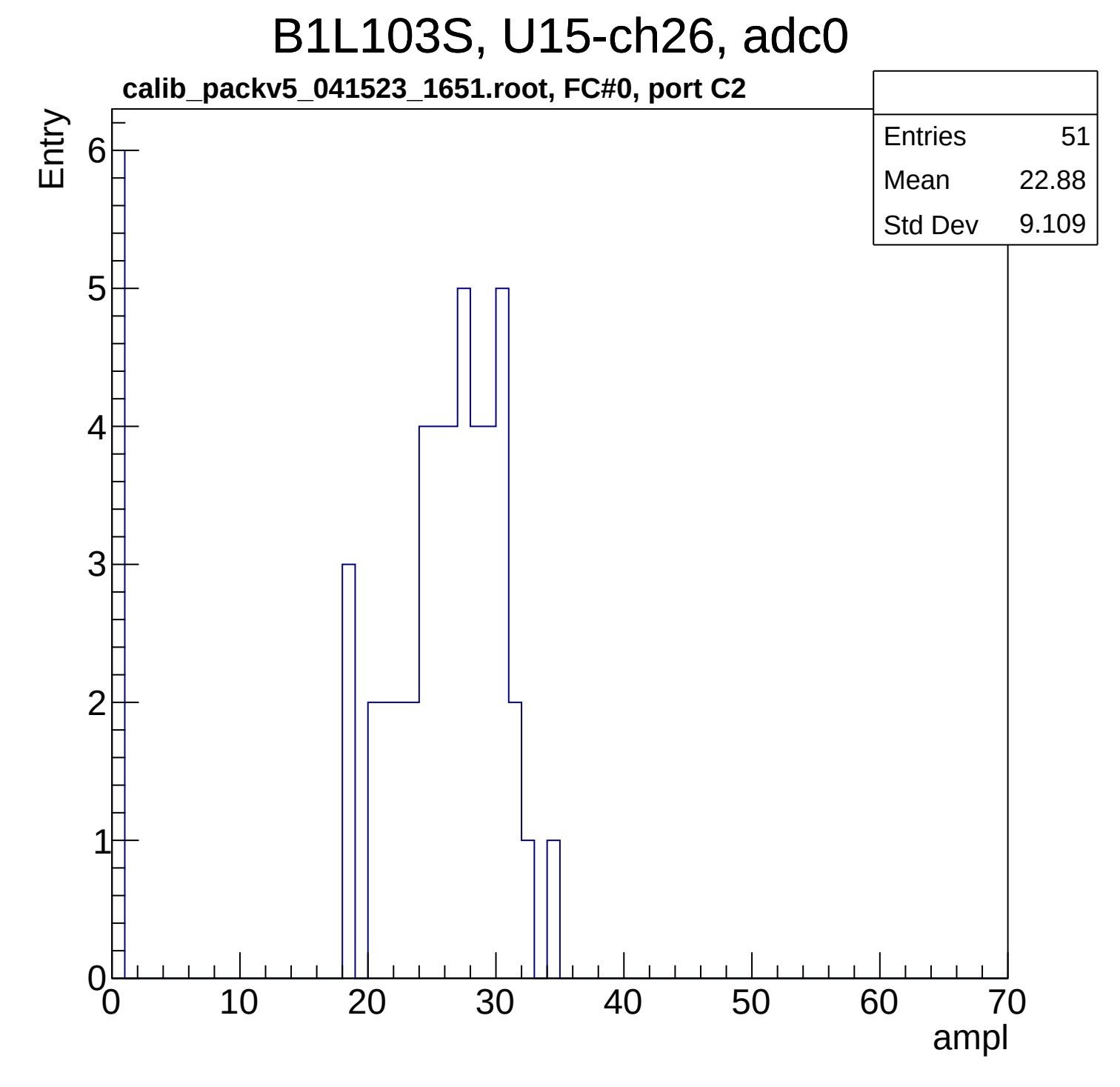
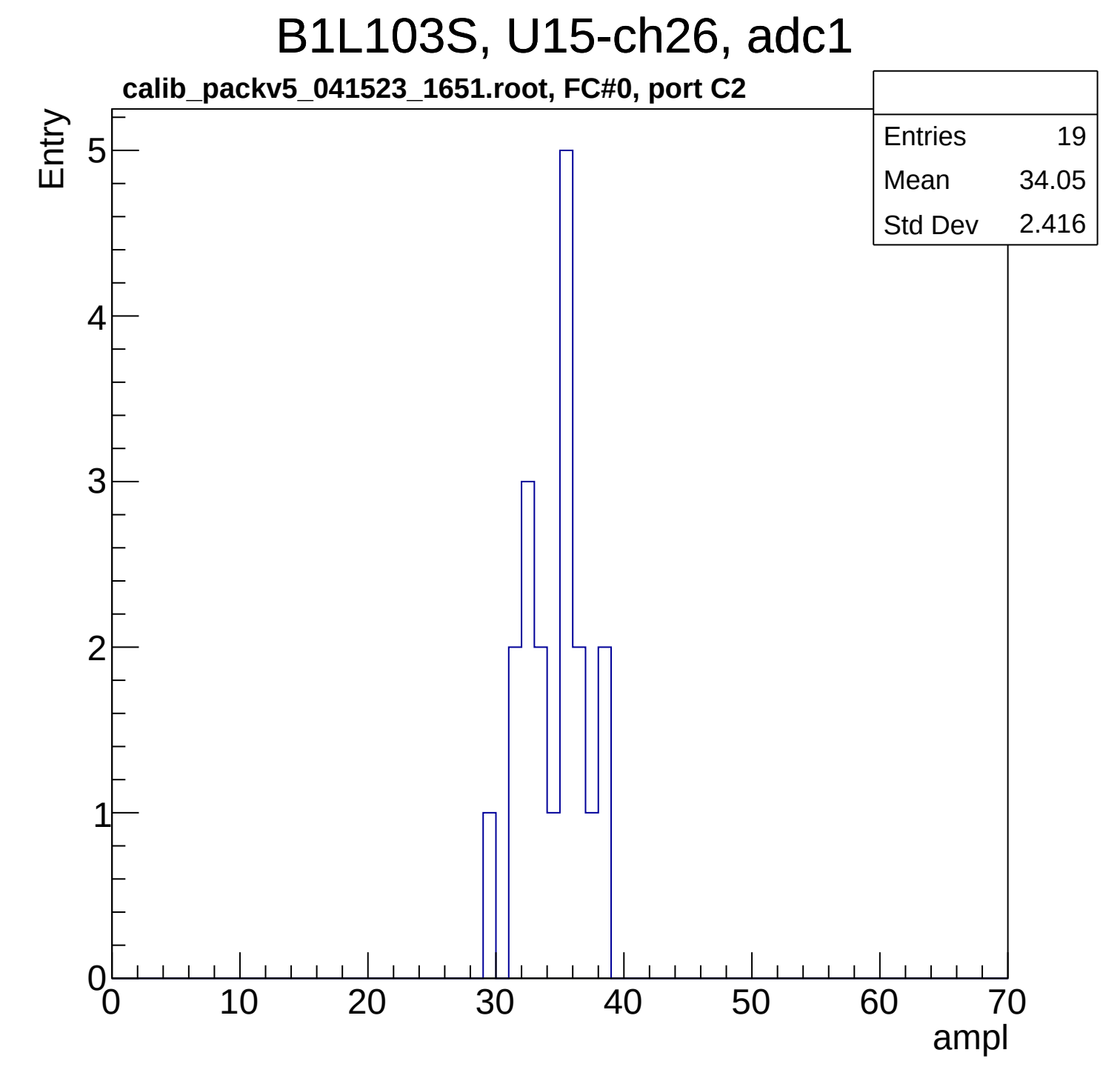
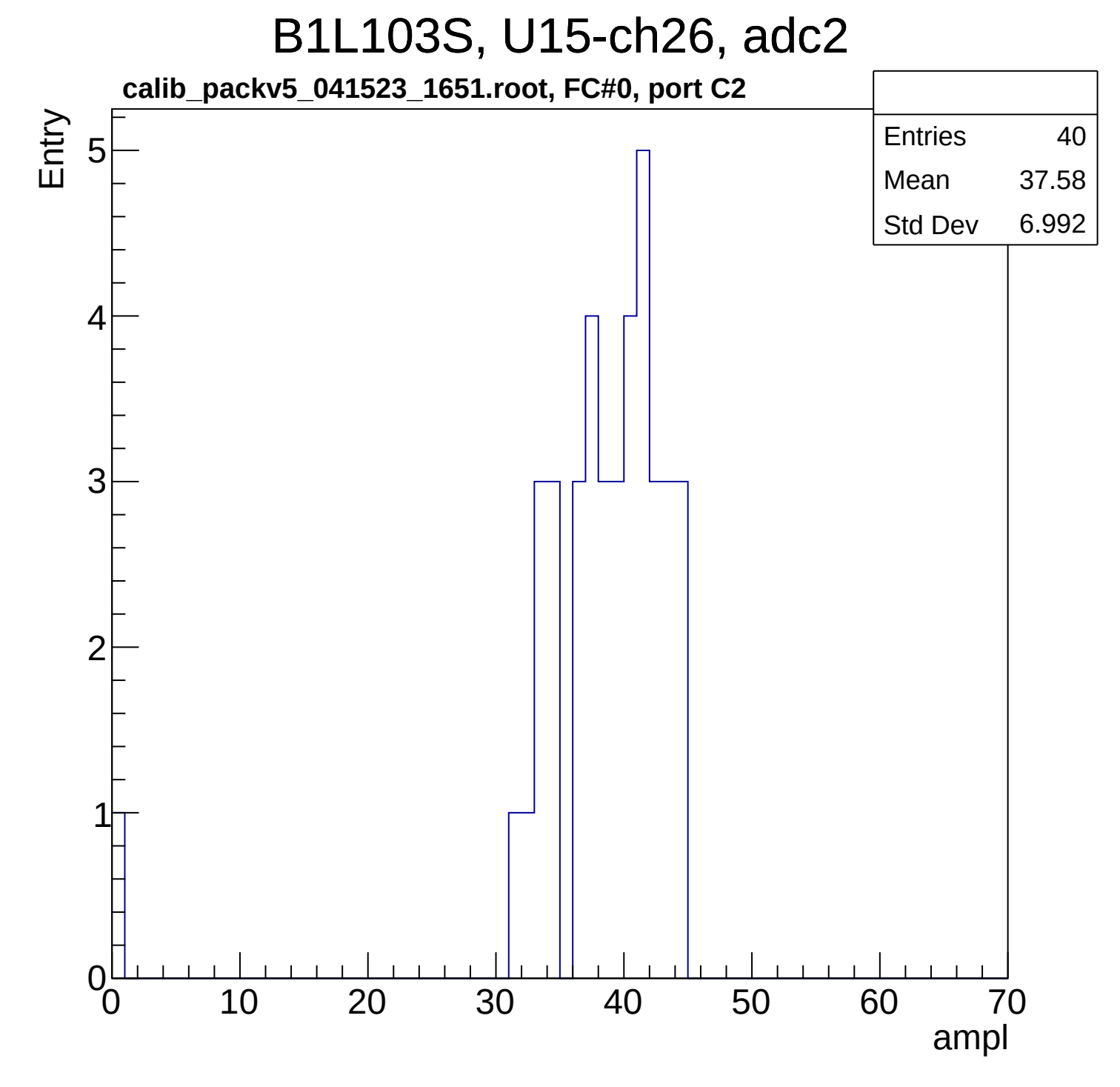
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

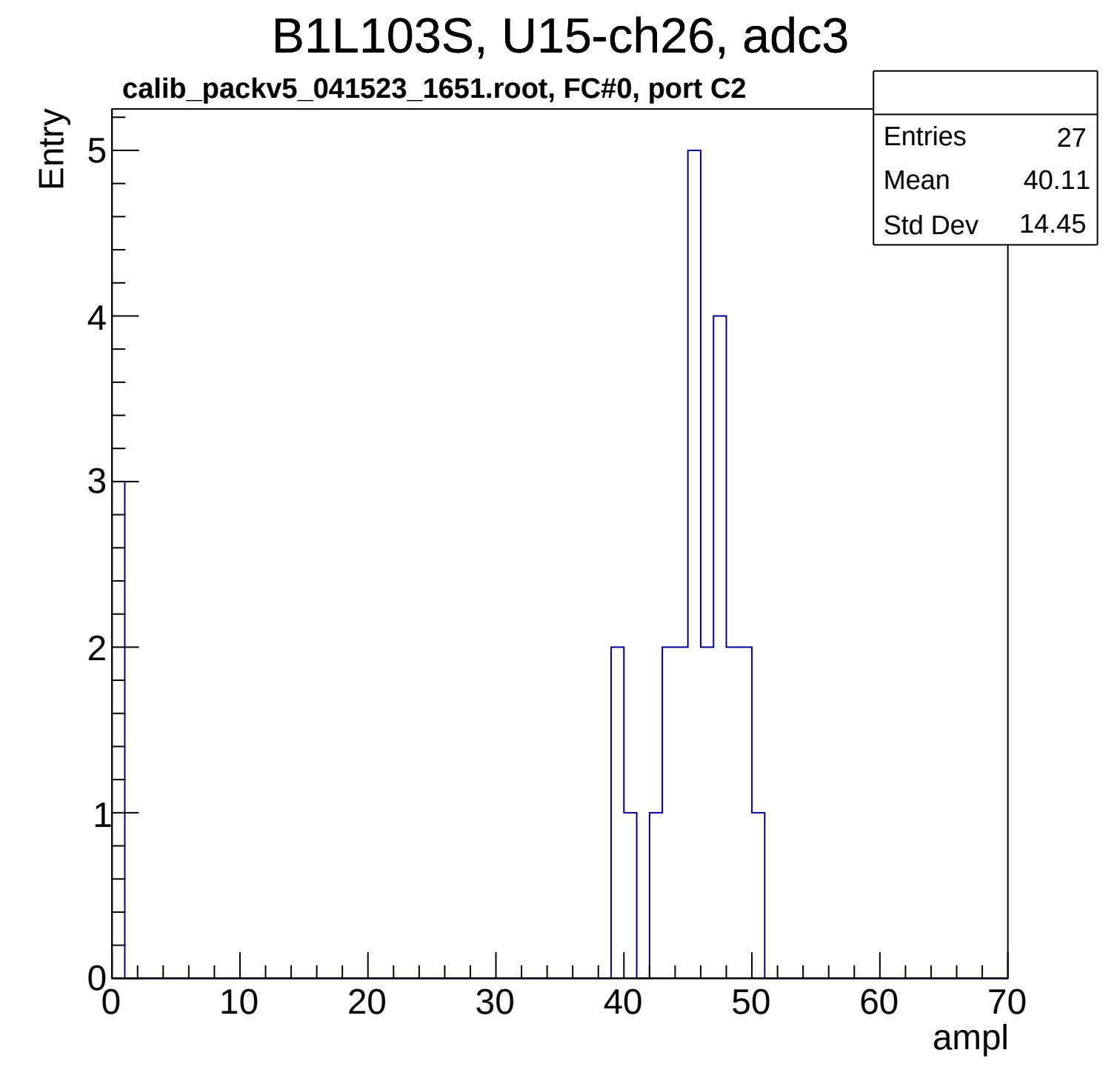

B1L103S, U15-ch25, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 61
Std Dev 2
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

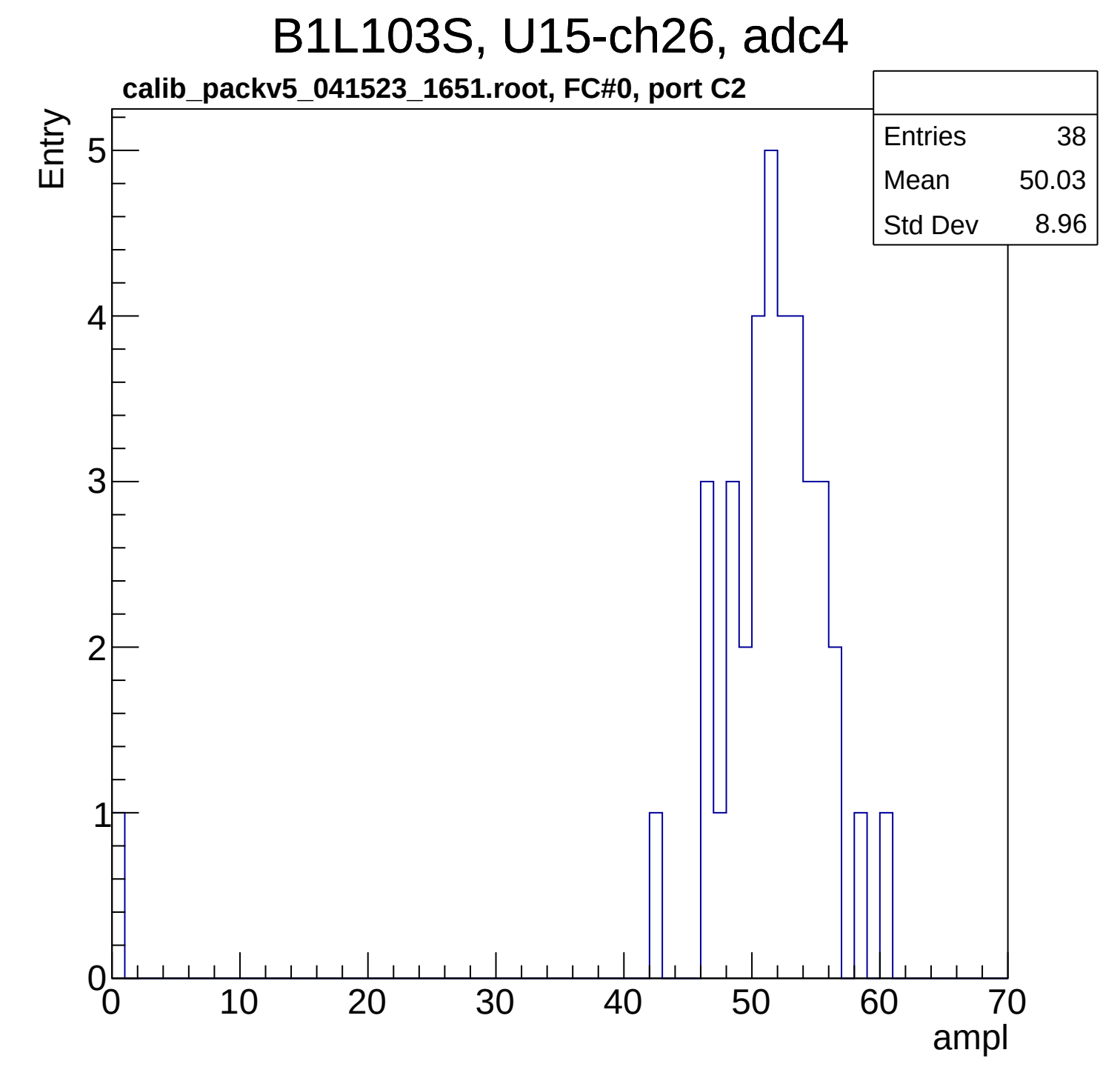

B1L103S, U15-ch25, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 0
Std Dev 0
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

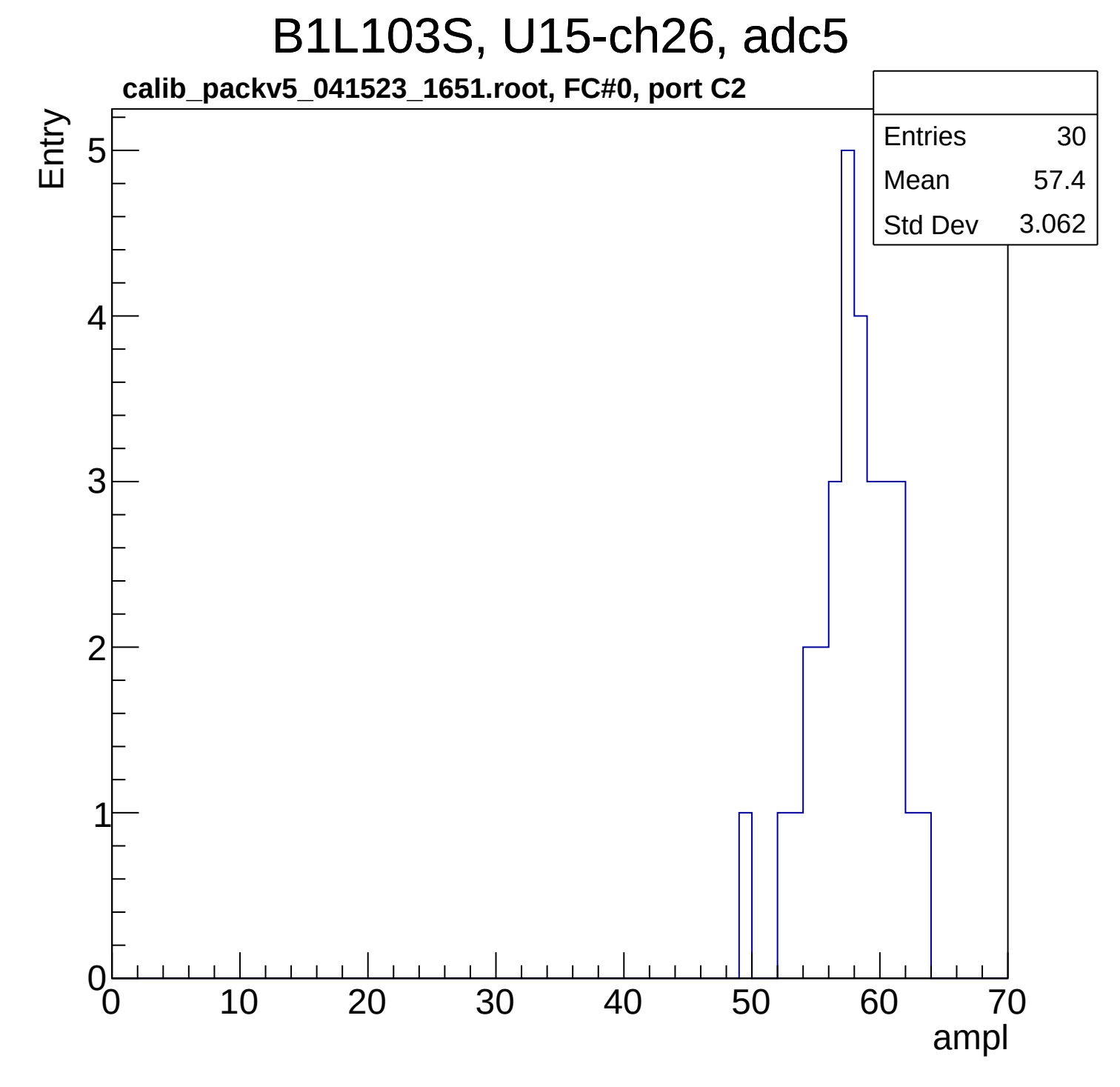

B1L103S, U15-ch26, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 22.88
Std Dev 9.109
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

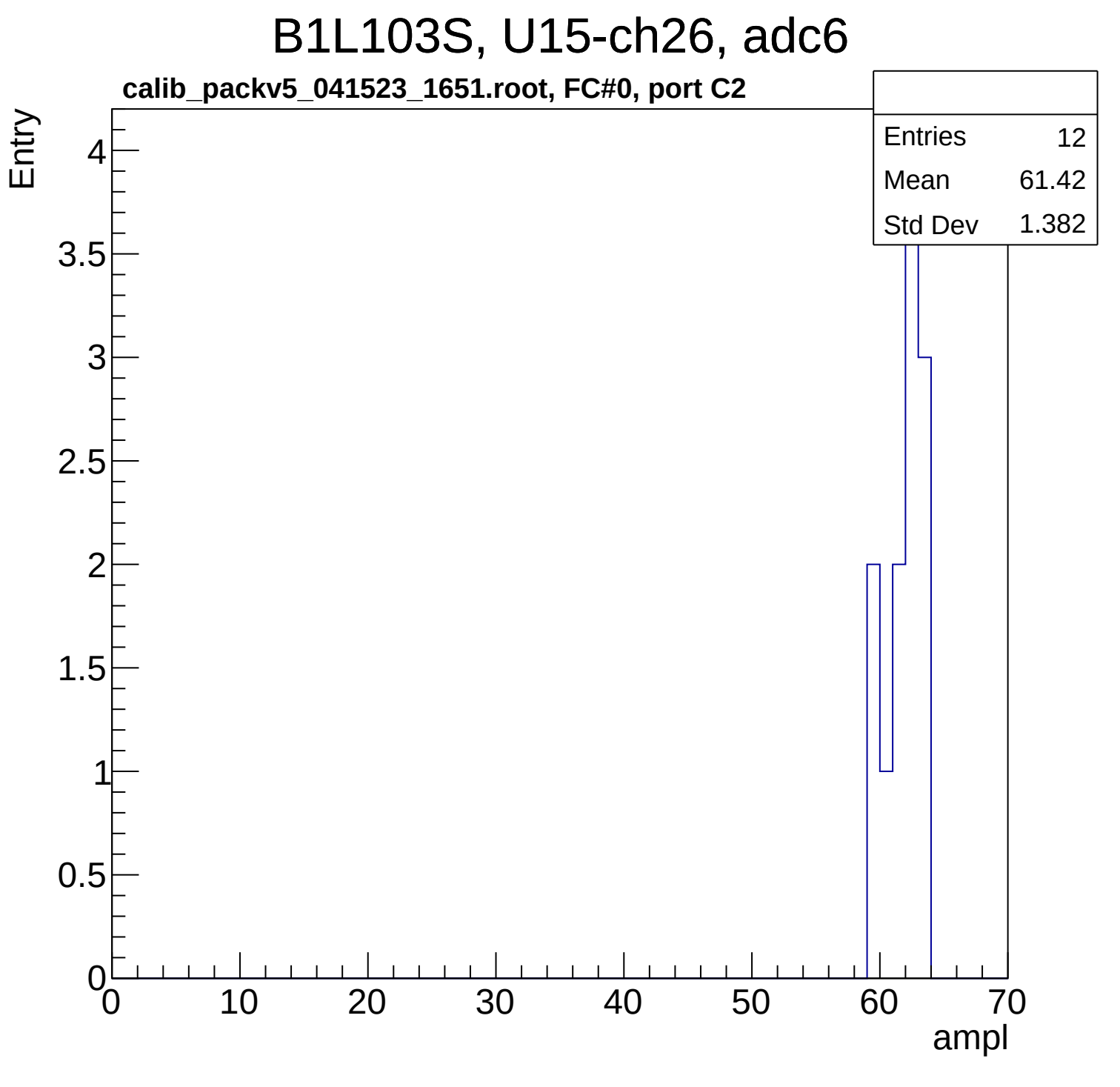

B1L103S, U15-ch26, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 34.05
Std Dev 2.416
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

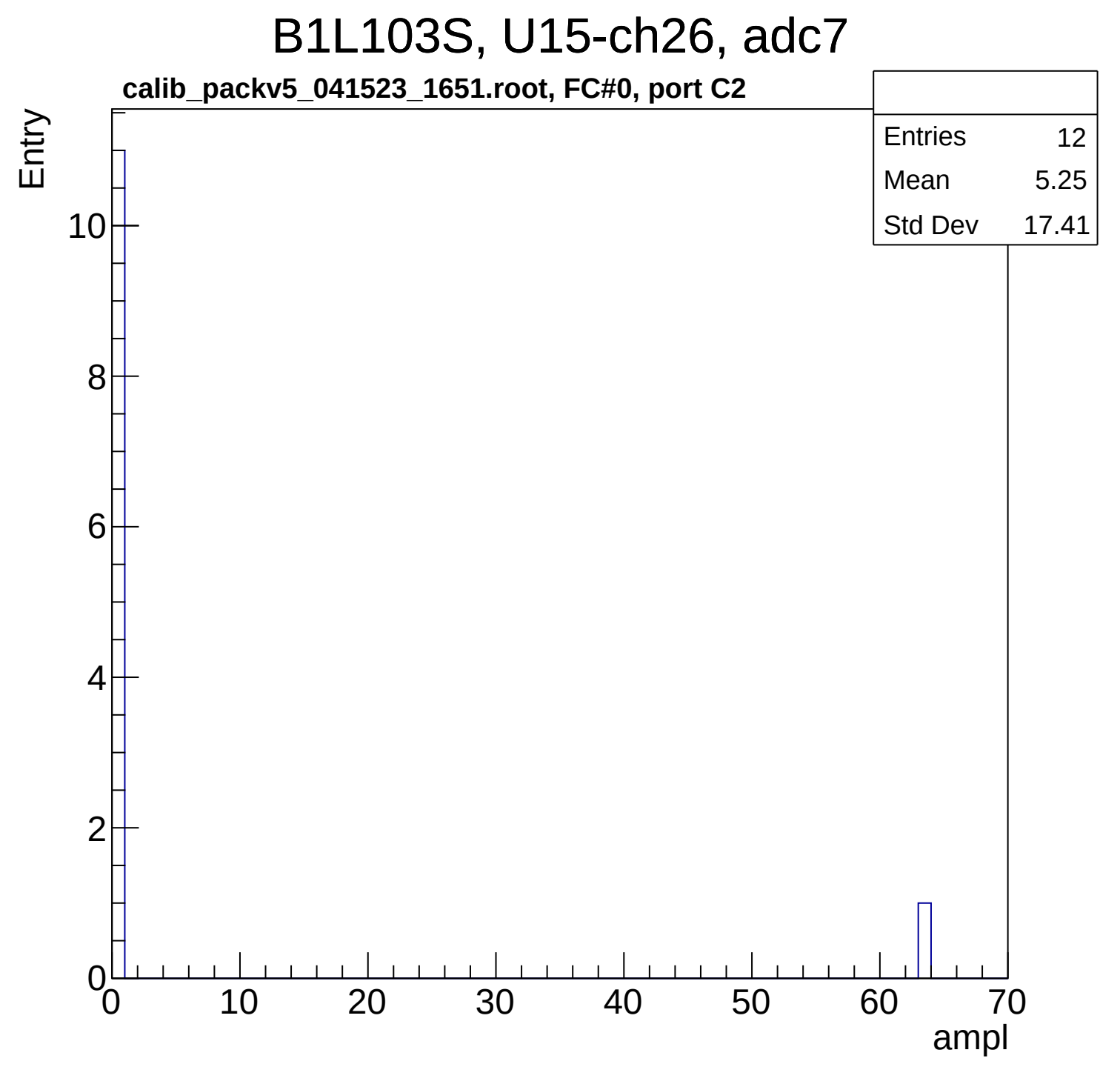

B1L103S, U15-ch26, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 37.58
Std Dev 6.992
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

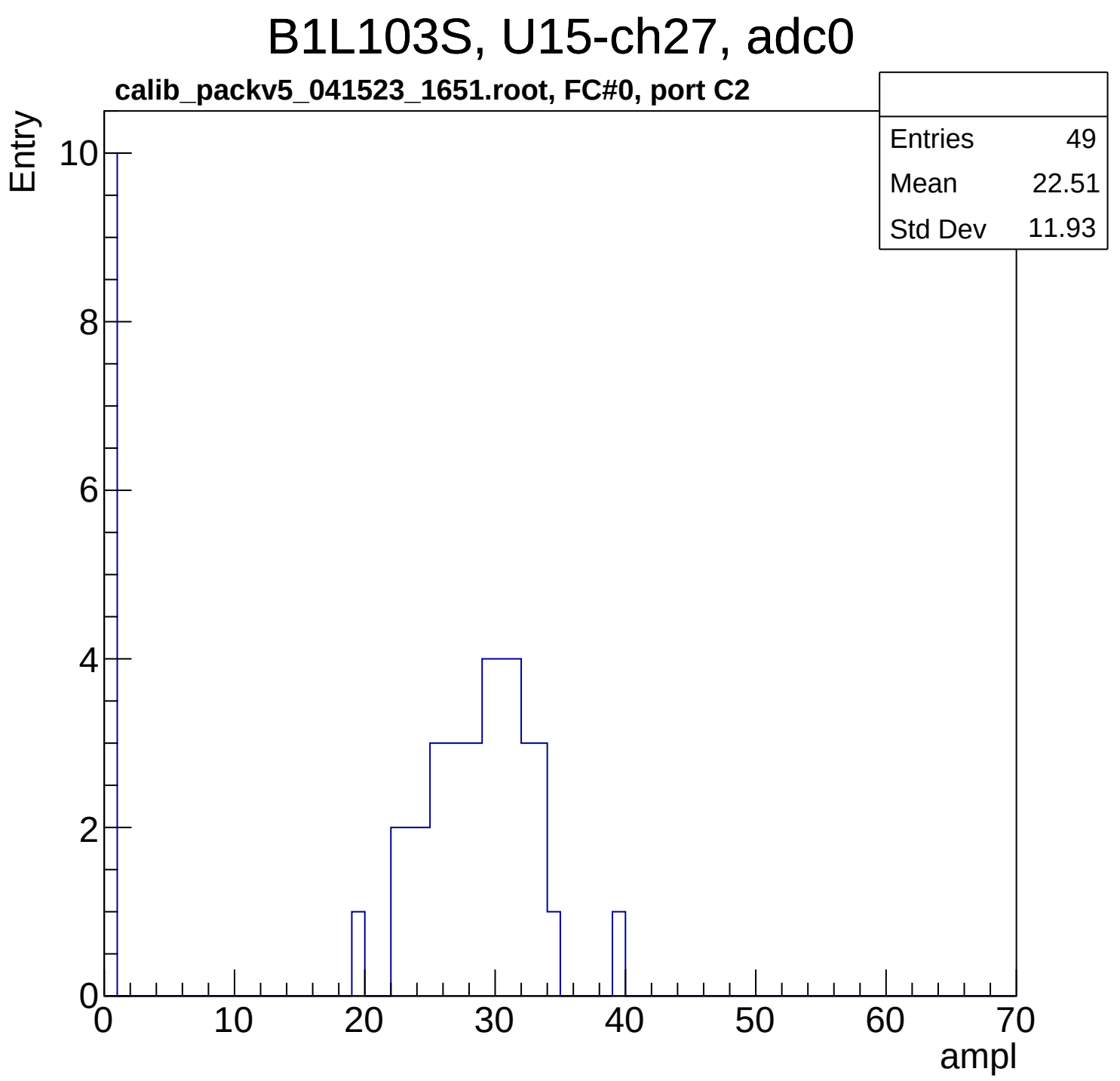

B1L103S, U15-ch26, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 40.11
Std Dev 14.45
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

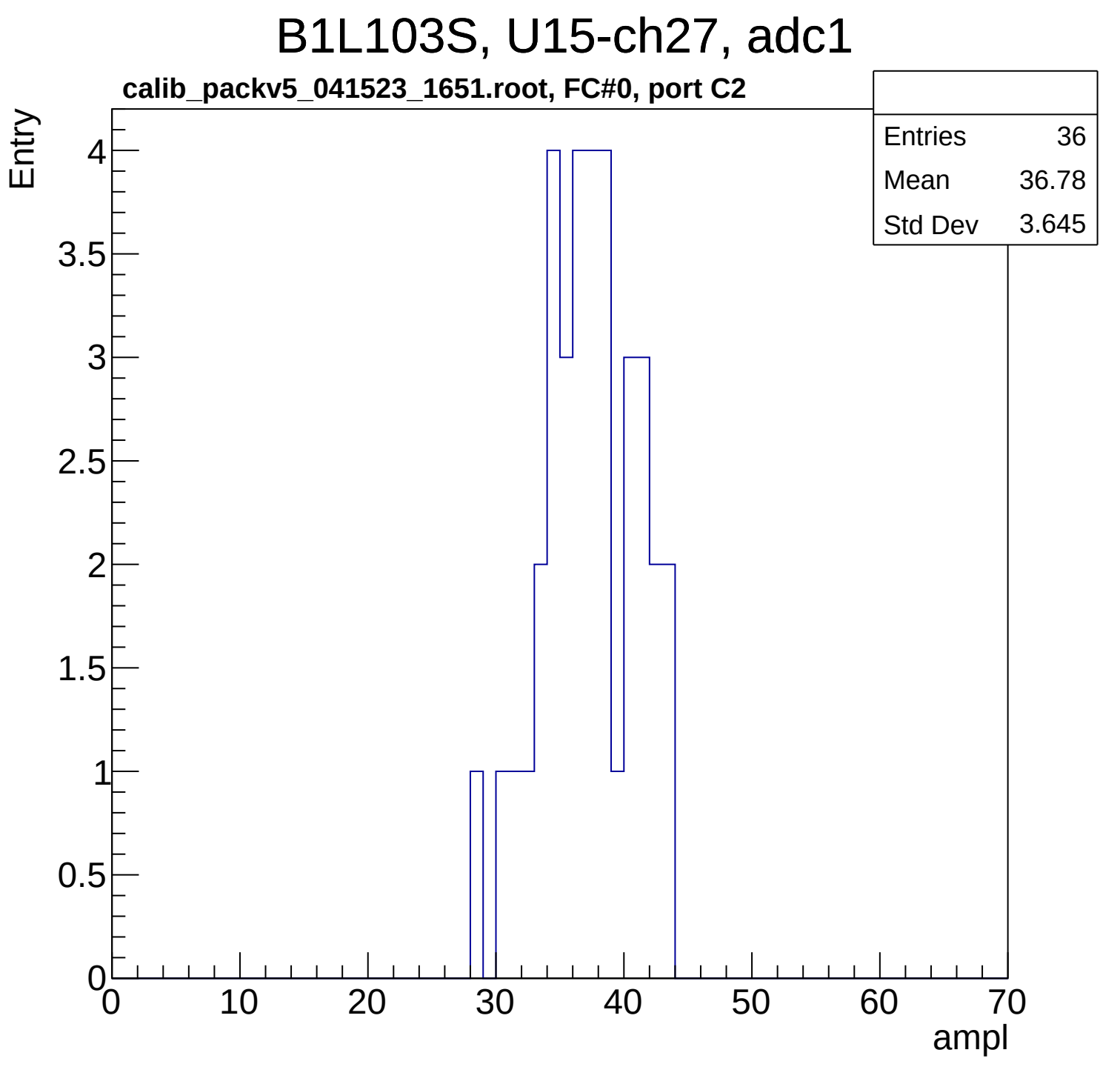

B1L103S, U15-ch26, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 50.03
Std Dev 8.96
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

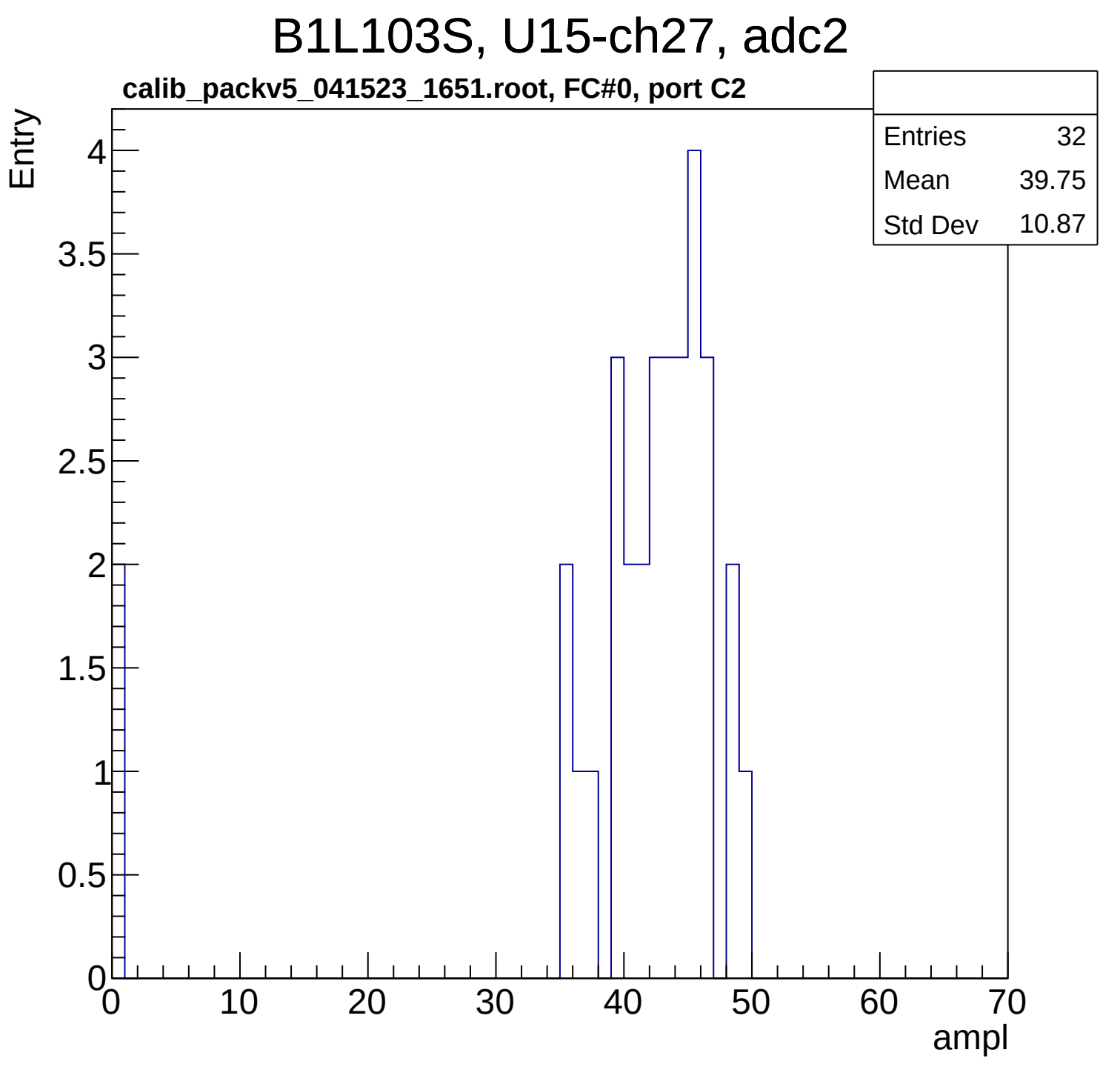

B1L103S, U15-ch26, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 57.4
Std Dev 3.062
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

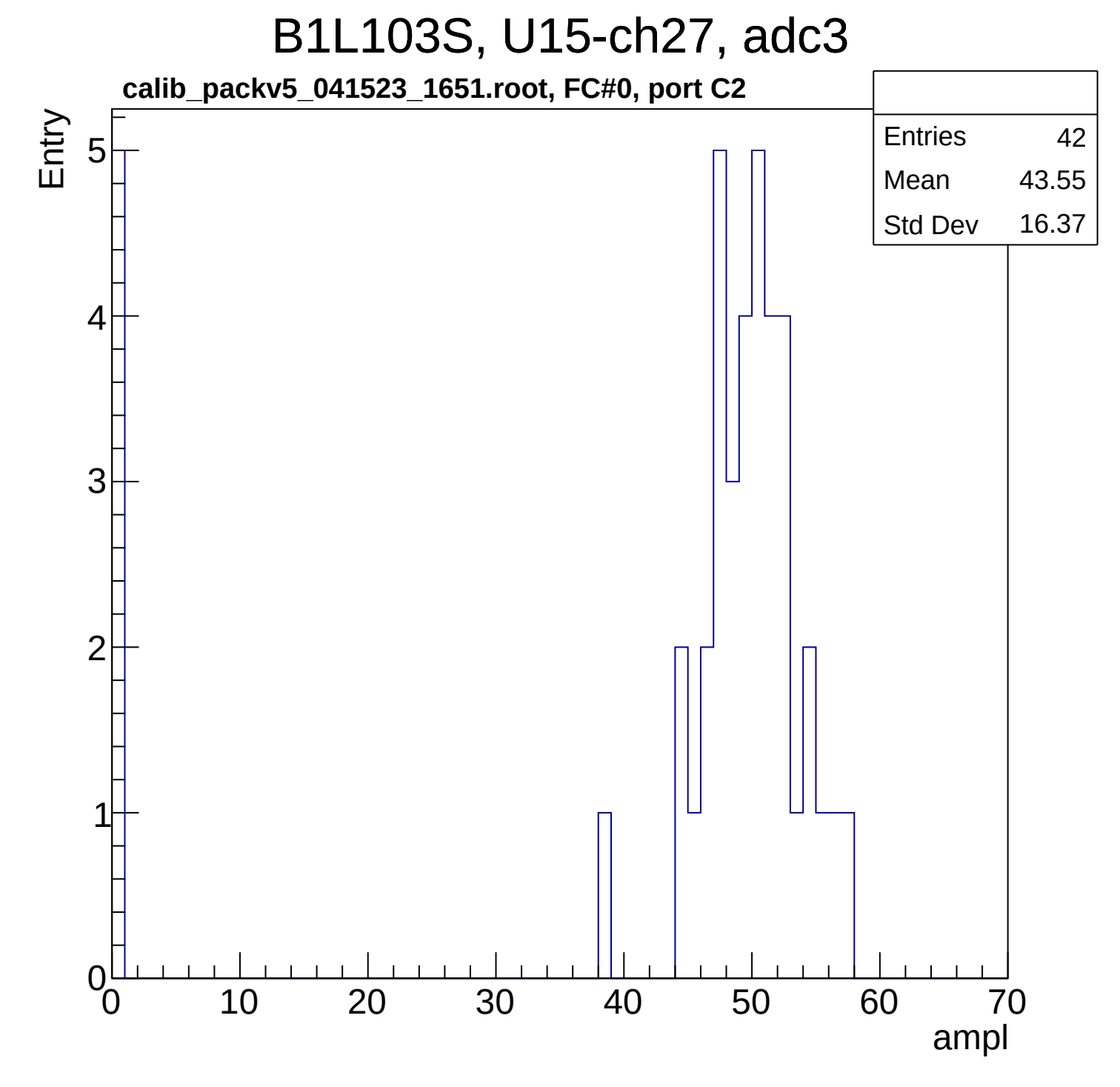

B1L103S, U15-ch26, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.42
Std Dev 1.382
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

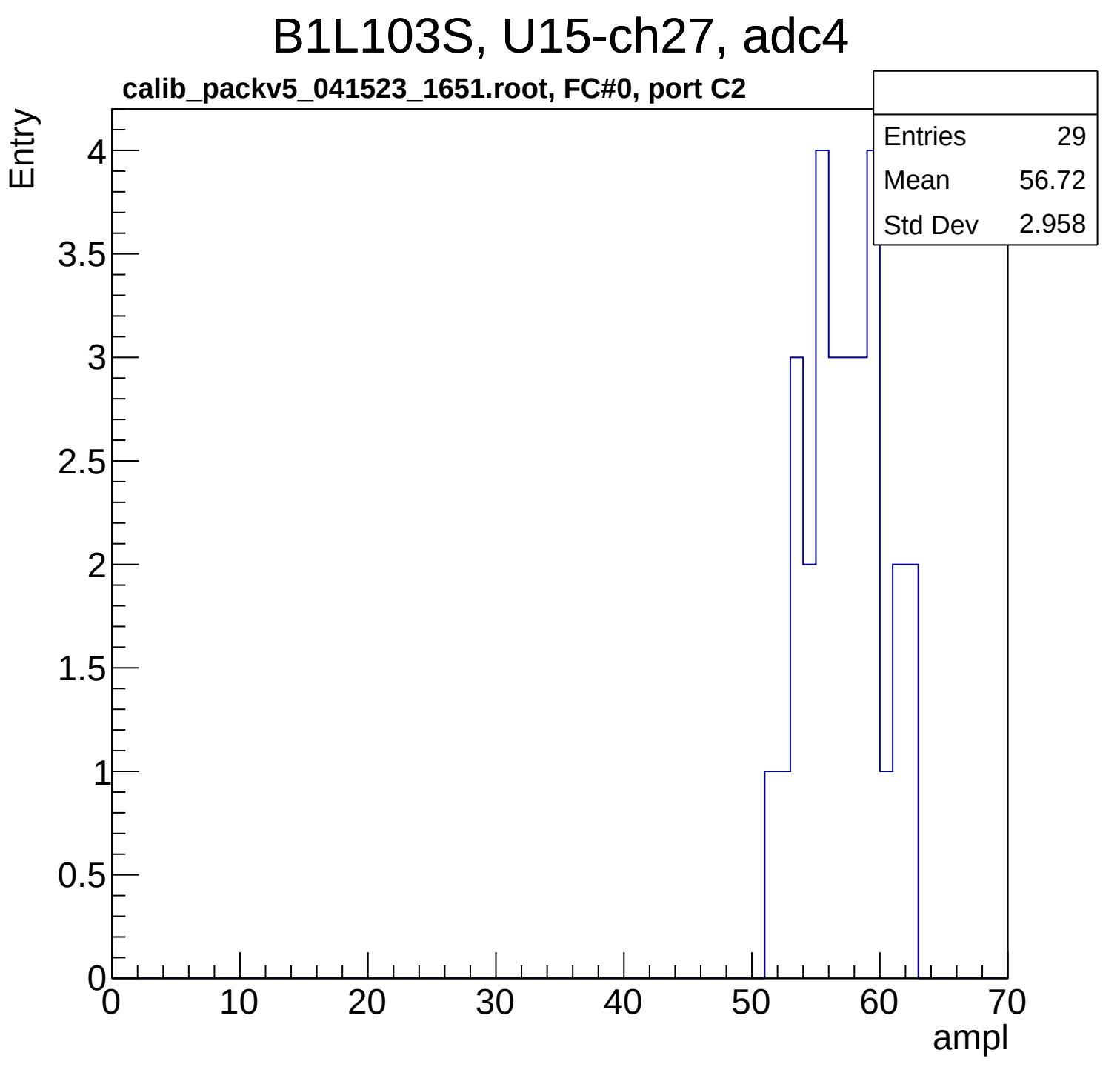

B1L103S, U15-ch26, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 5.25
Std Dev 17.41
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

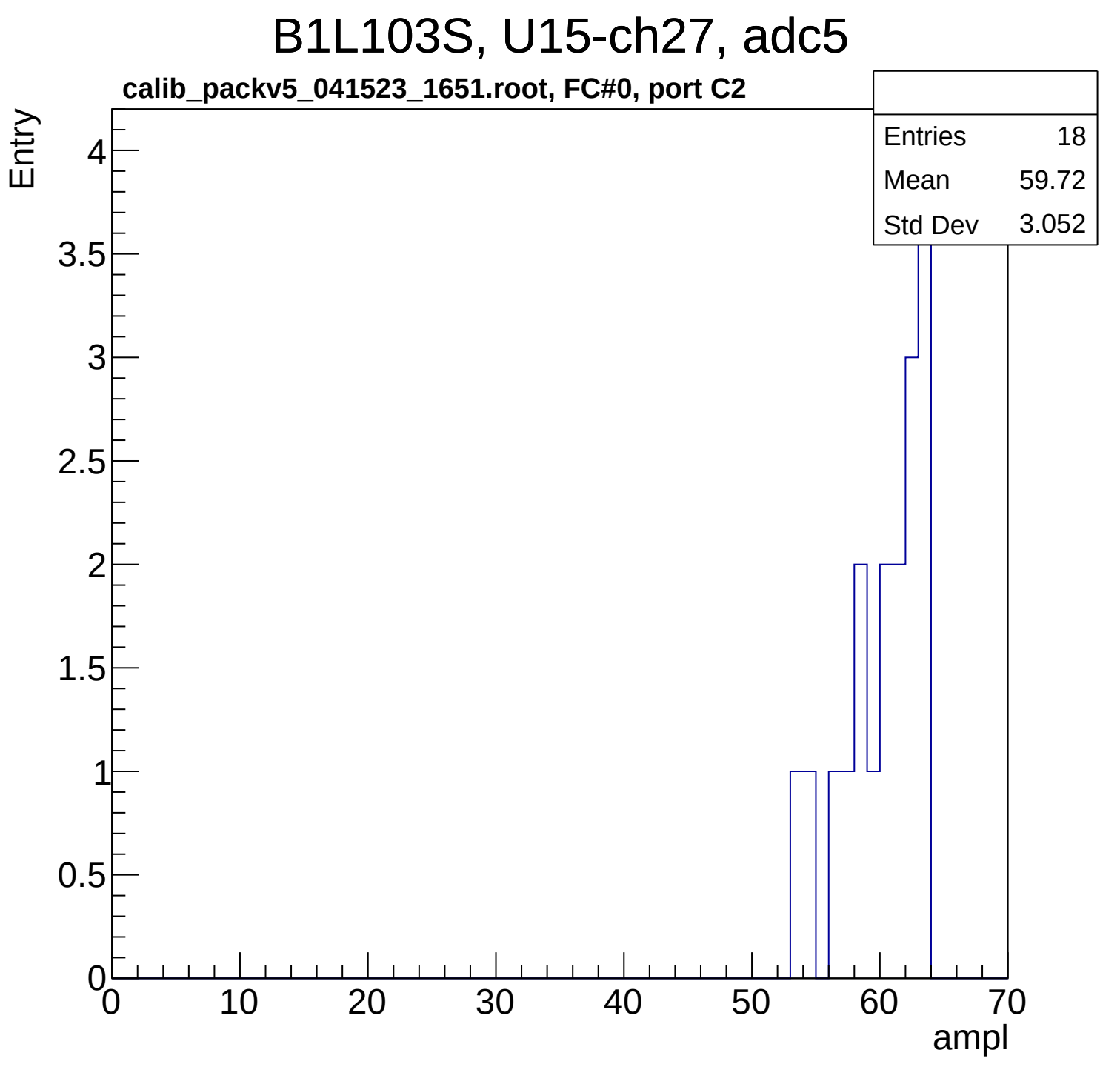

B1L103S, U15-ch27, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 22.51
Std Dev 11.93
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

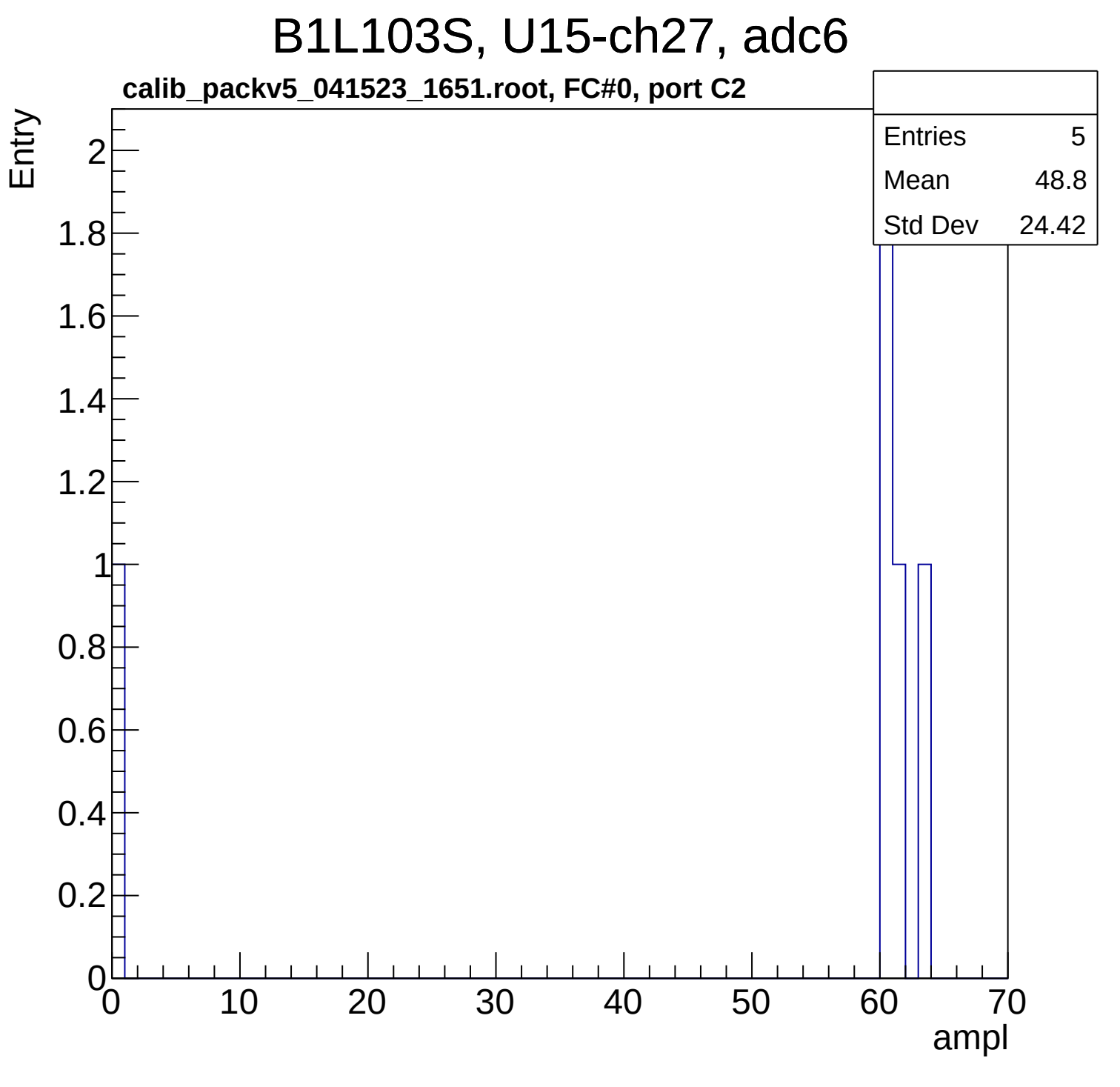

B1L103S, U15-ch27, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 36.78
Std Dev 3.645
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

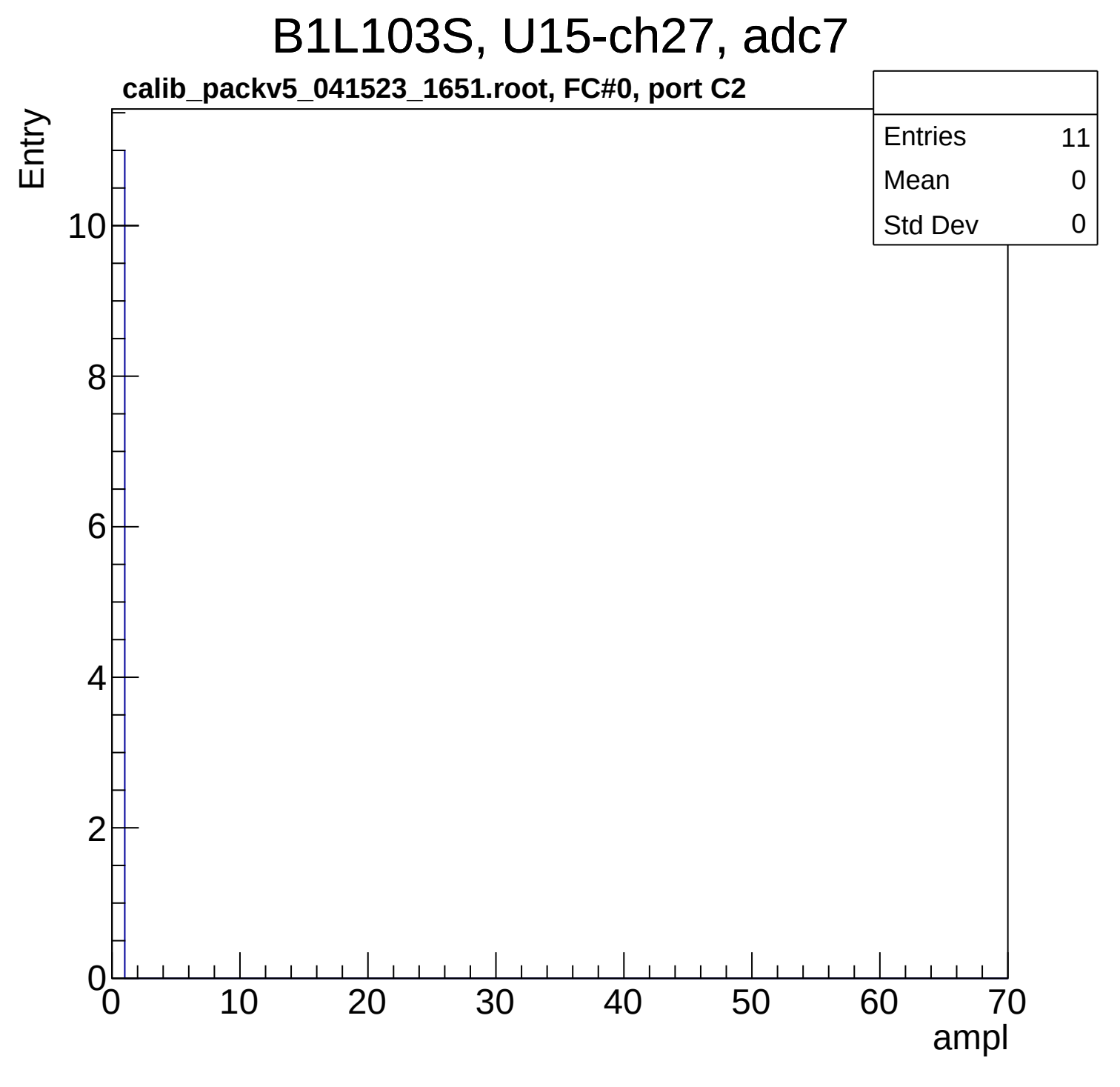

B1L103S, U15-ch27, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 39.75
Std Dev 10.87
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

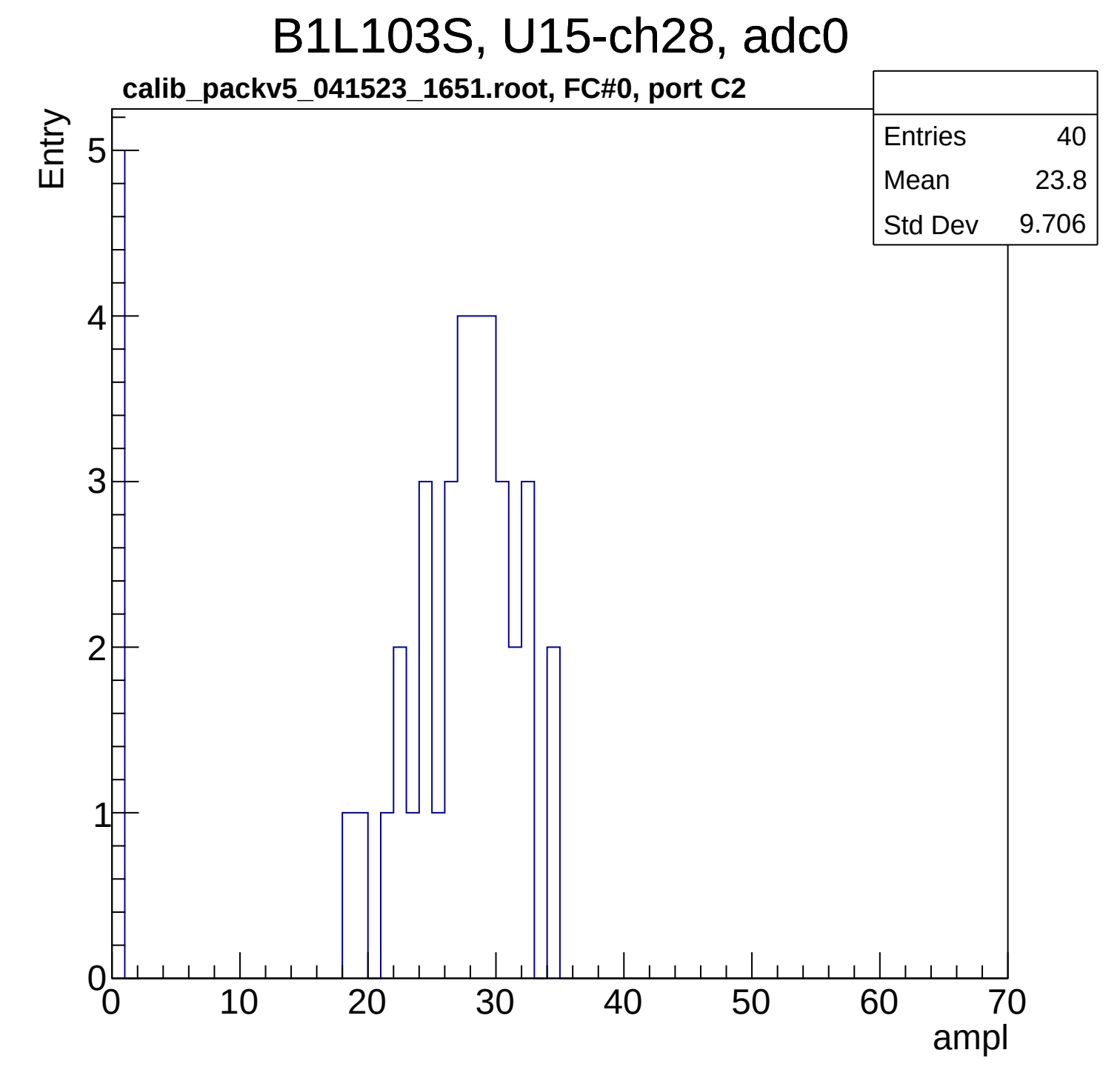

B1L103S, U15-ch27, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 43.55
Std Dev 16.37
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

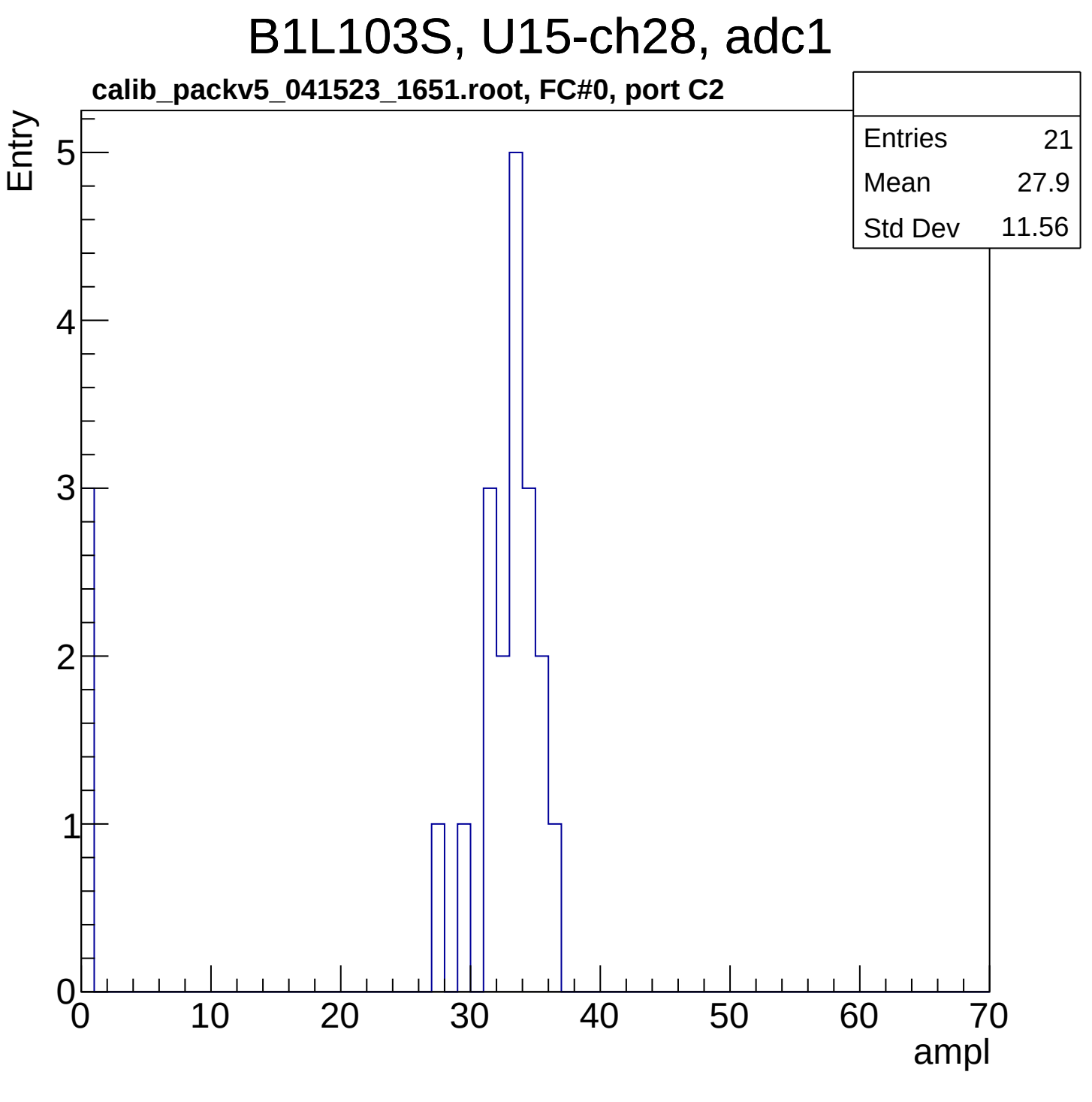

B1L103S, U15-ch27, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 56.72
Std Dev 2.958
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

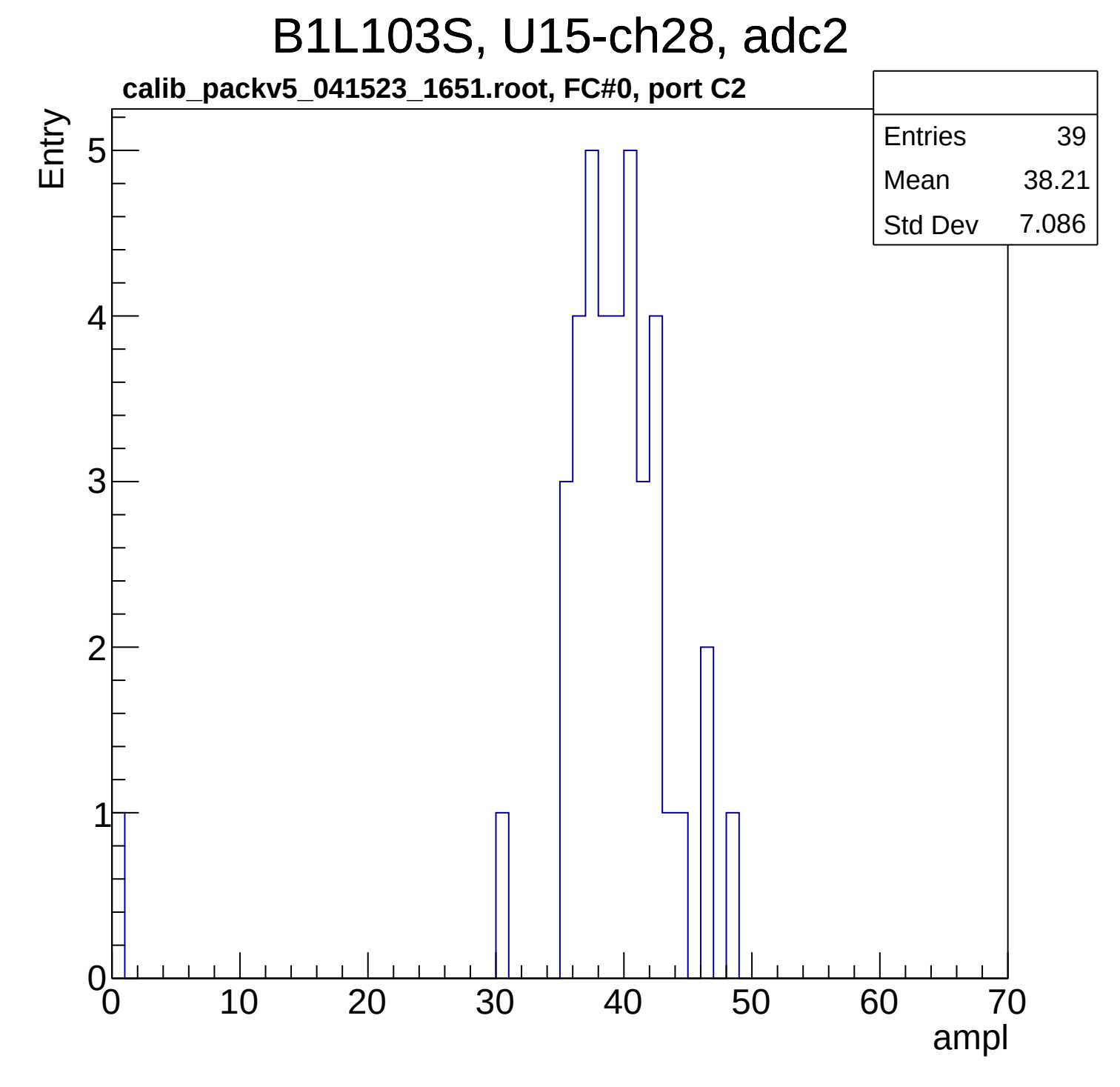

B1L103S, U15-ch27, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 59.72
Std Dev 3.052
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

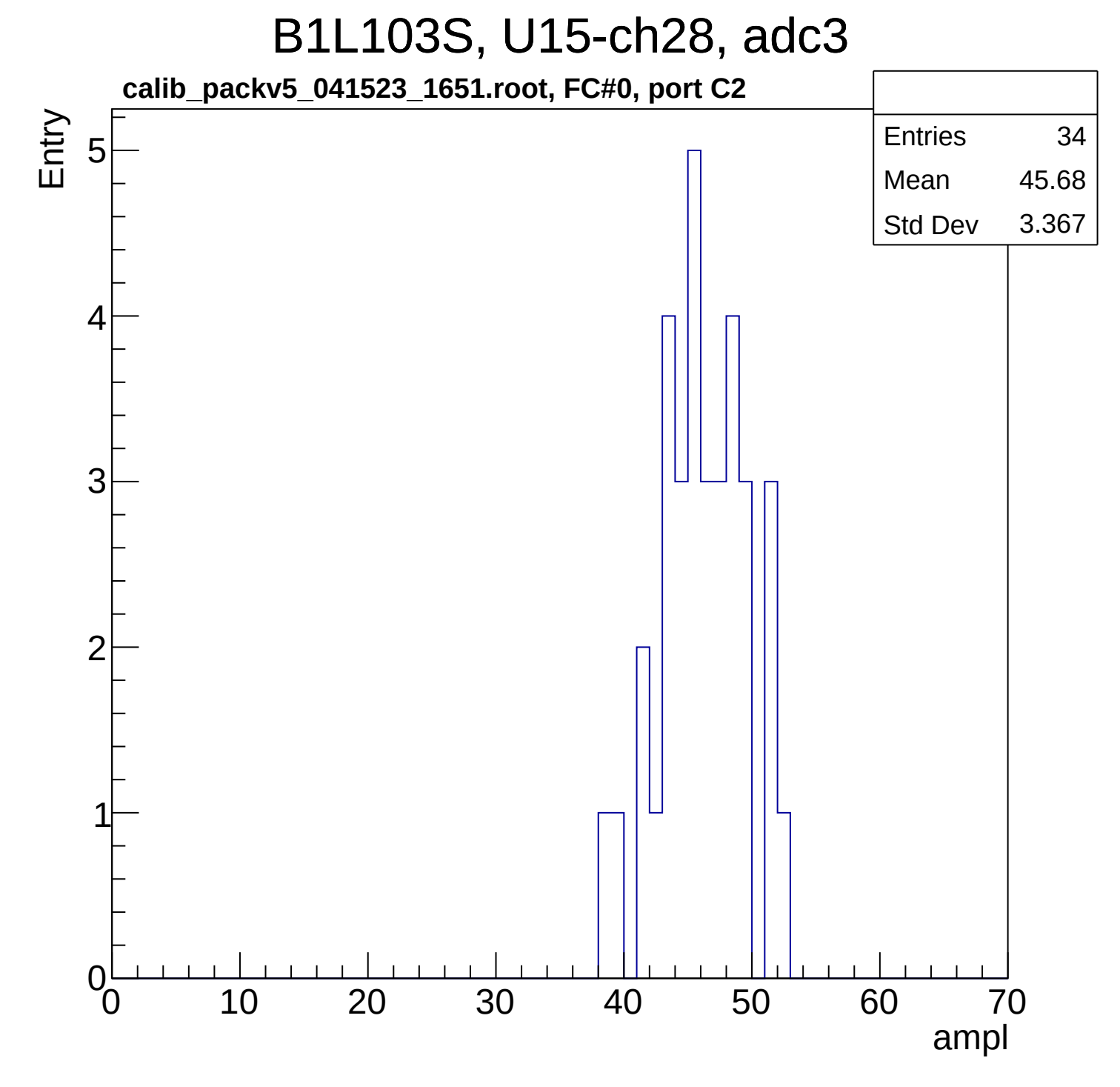

B1L103S, U15-ch27, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 48.8
Std Dev 24.42
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

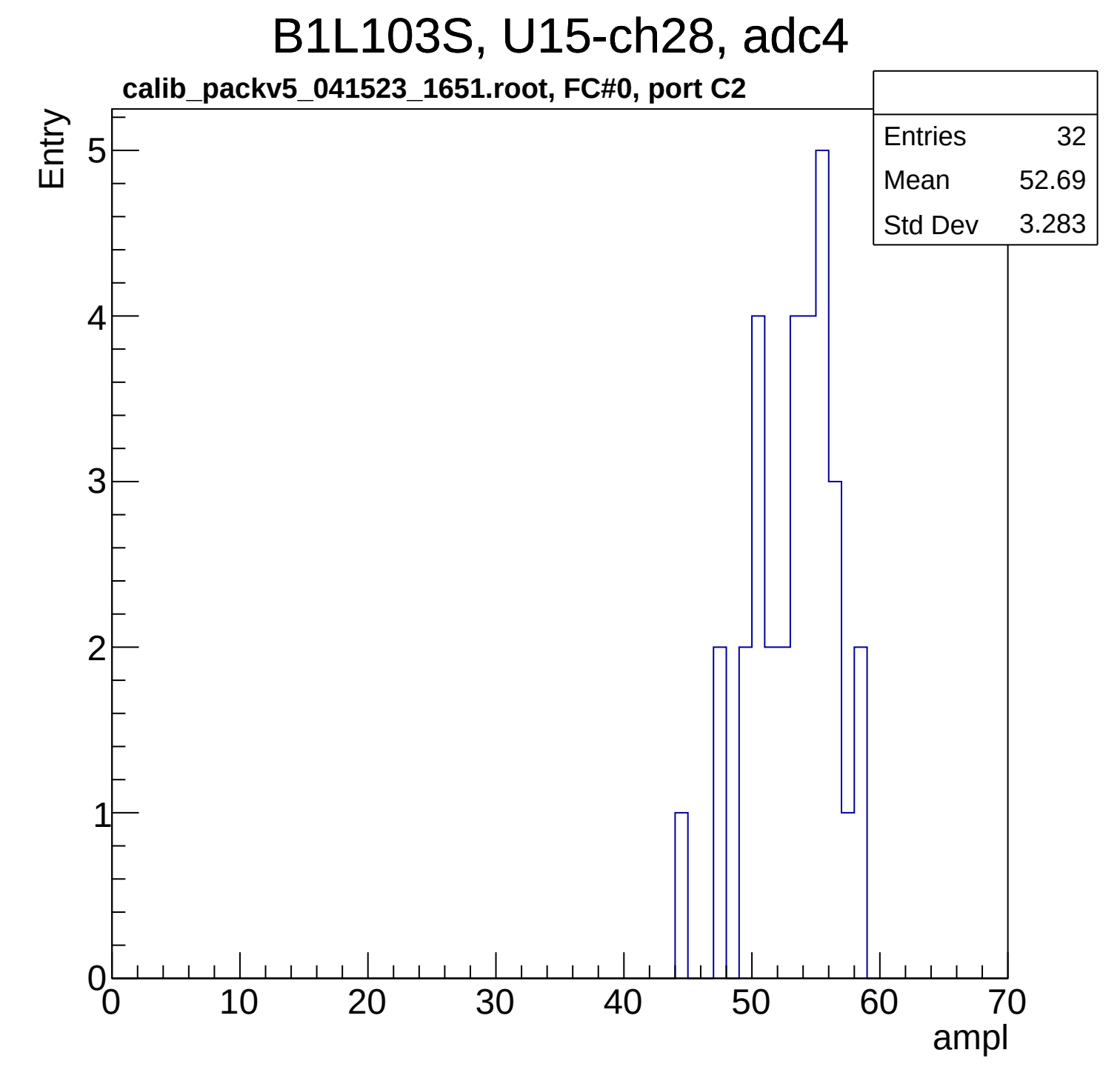

B1L103S, U15-ch27, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

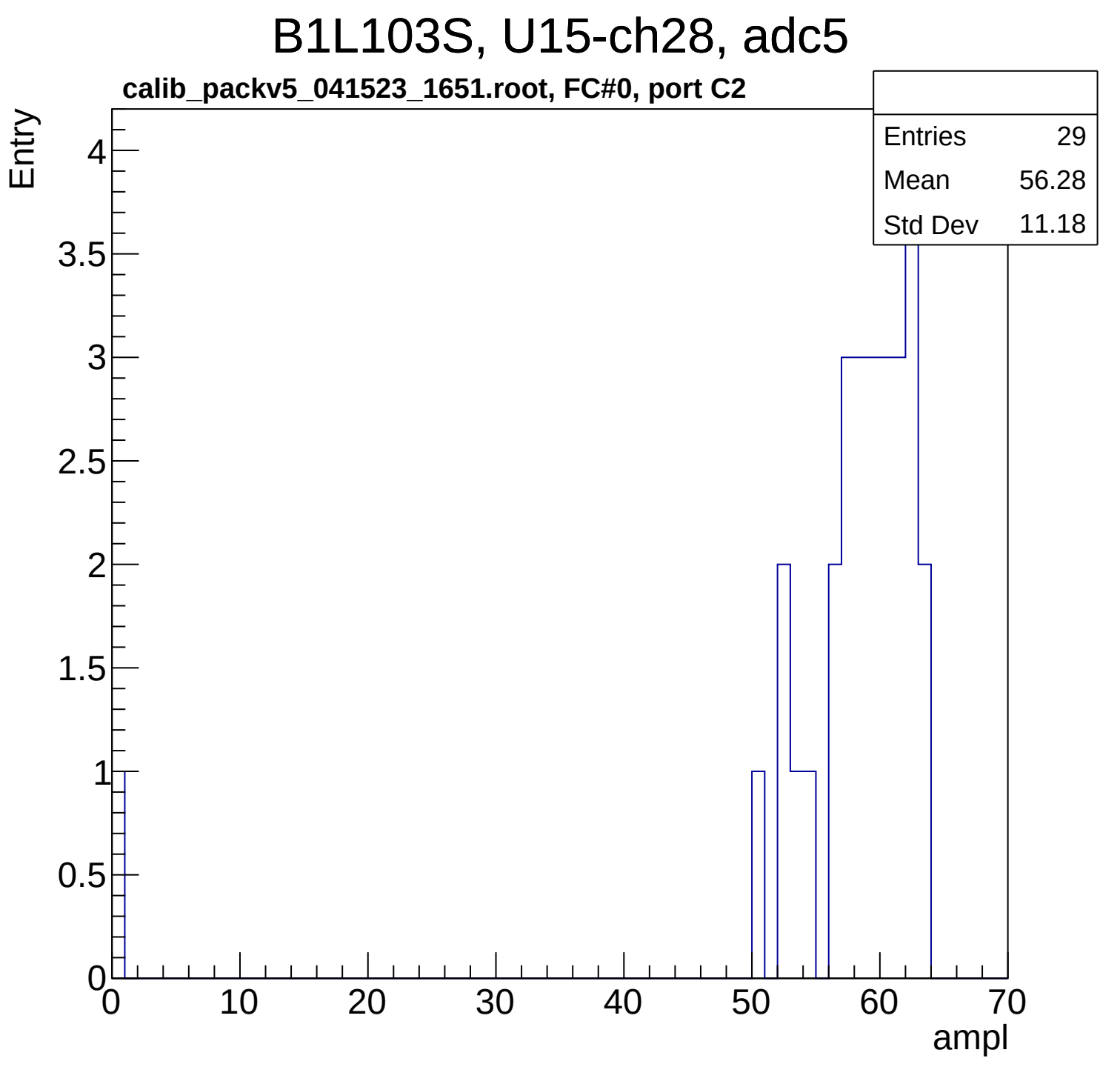

B1L103S, U15-ch28, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 23.8
Std Dev 9.706
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

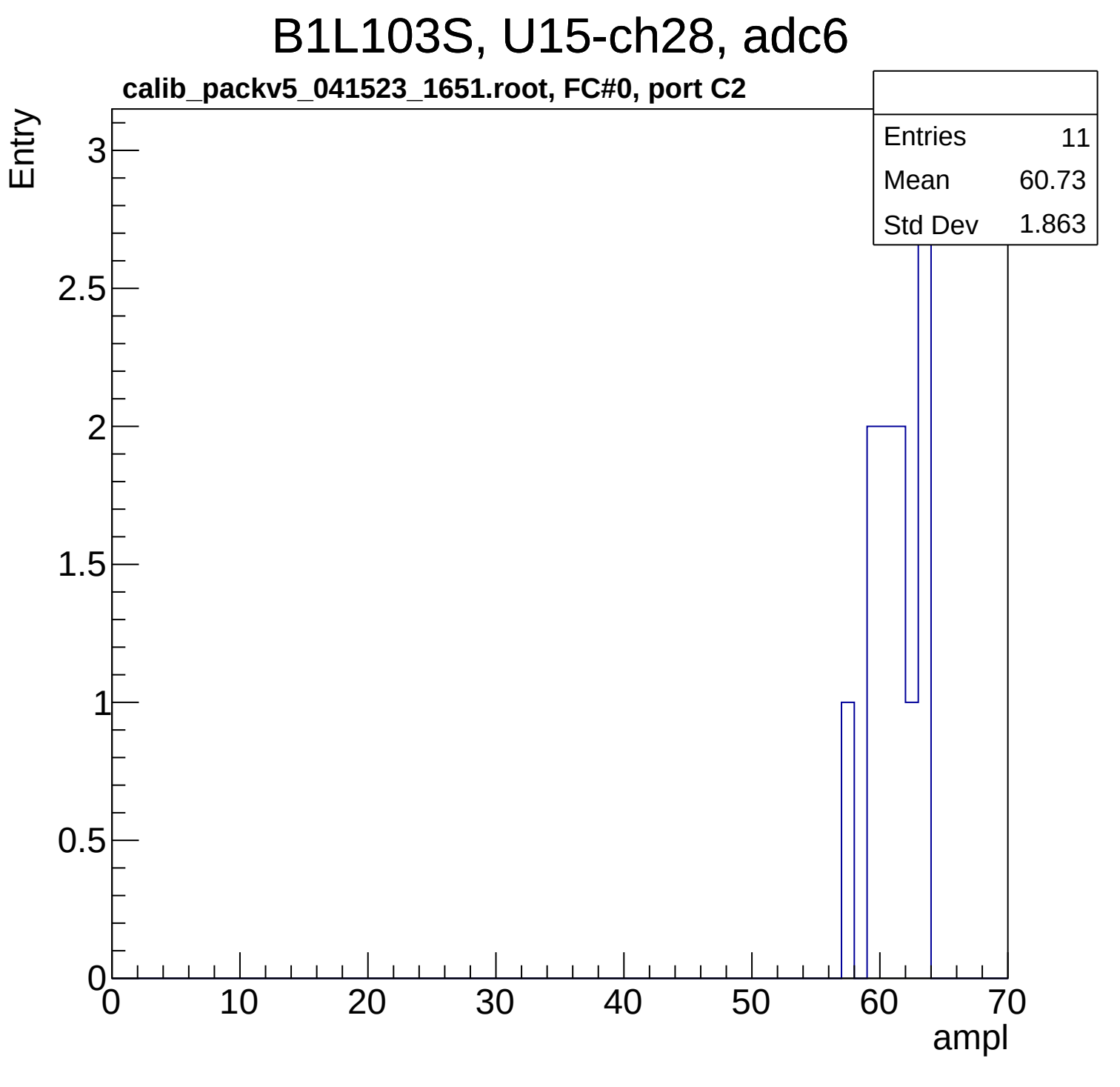

B1L103S, U15-ch28, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 27.9
Std Dev 11.56
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

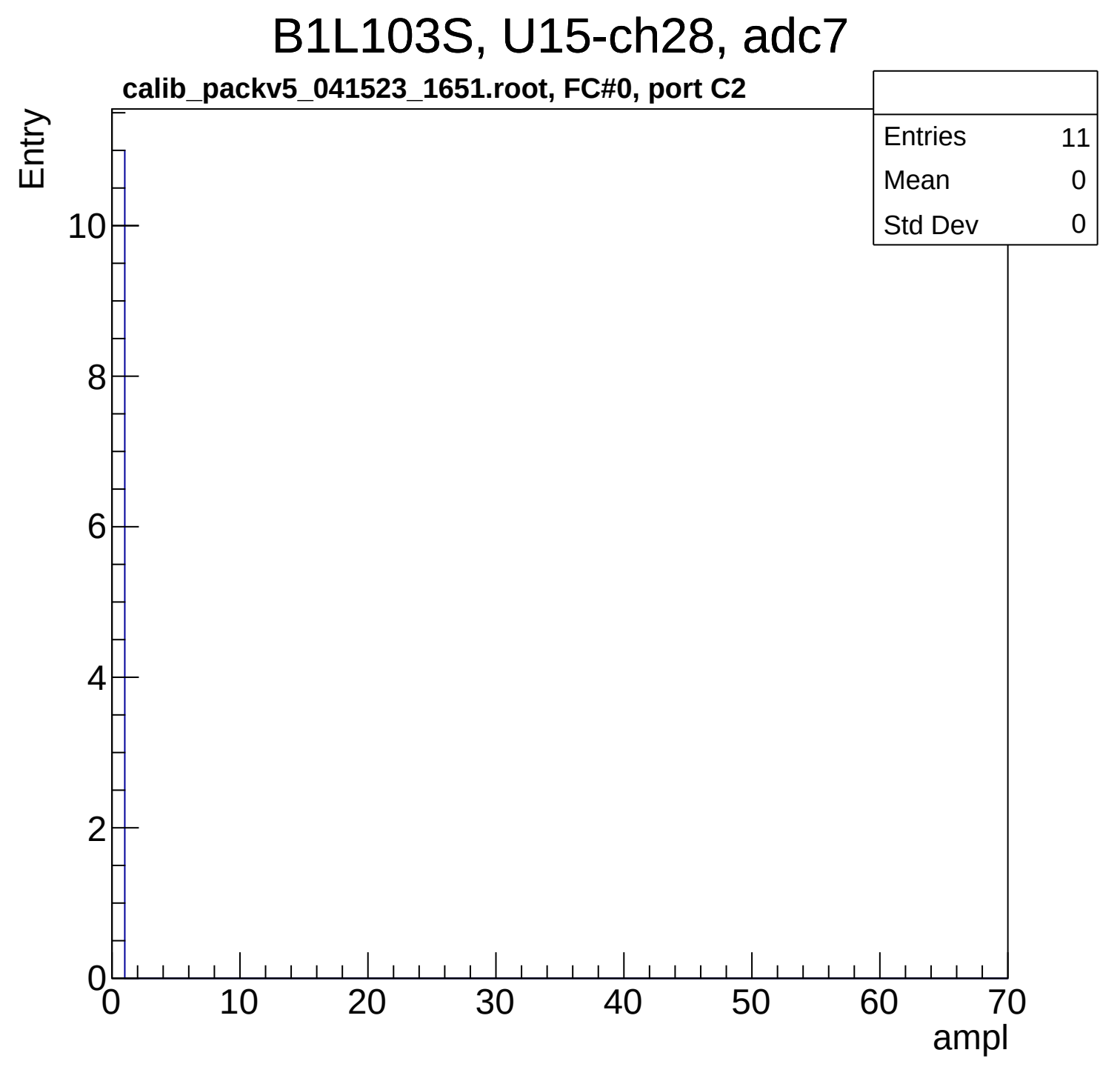

B1L103S, U15-ch28, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 38.21
Std Dev 7.086
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

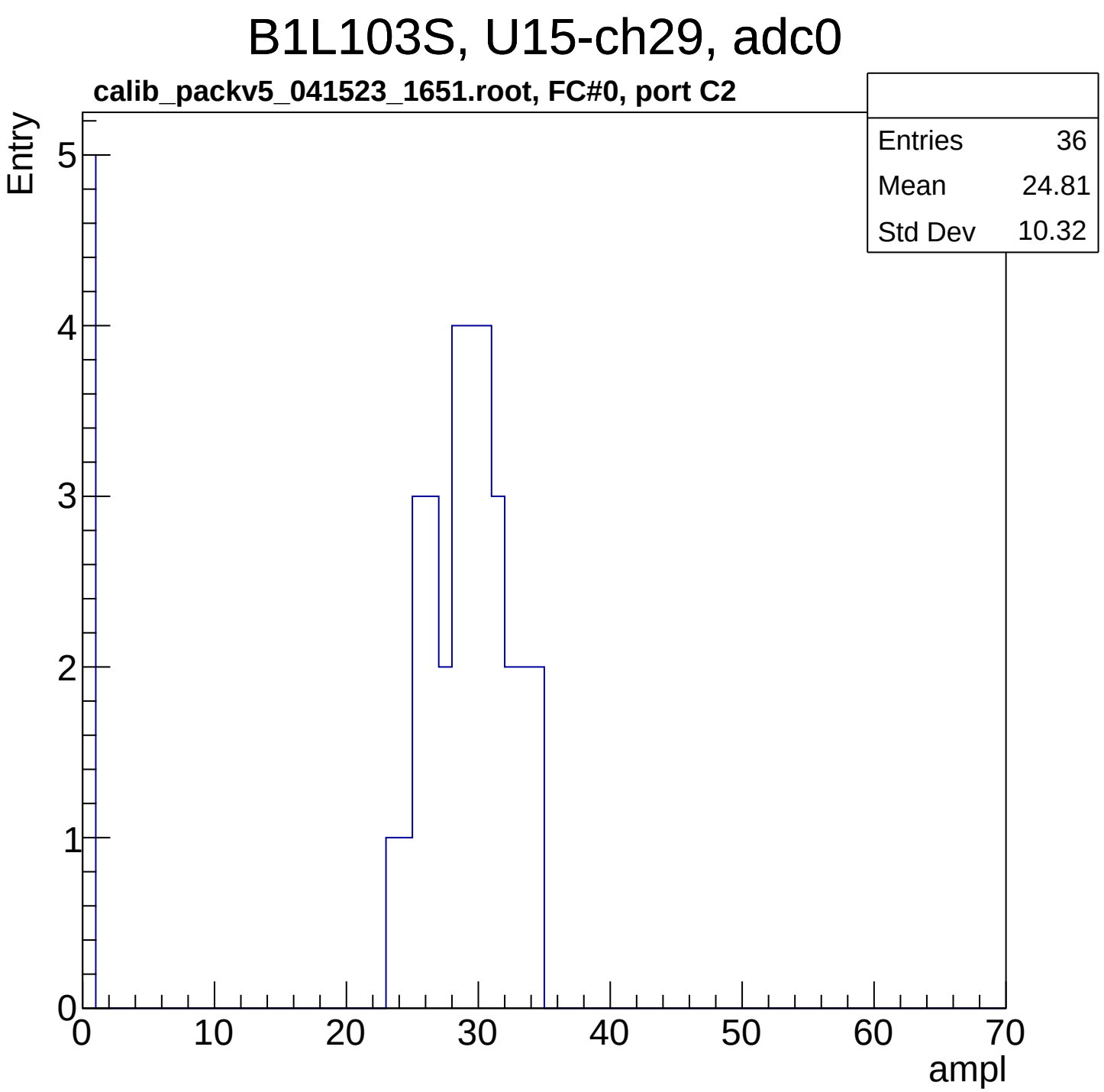

B1L103S, U15-ch28, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 45.68
Std Dev 3.367
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

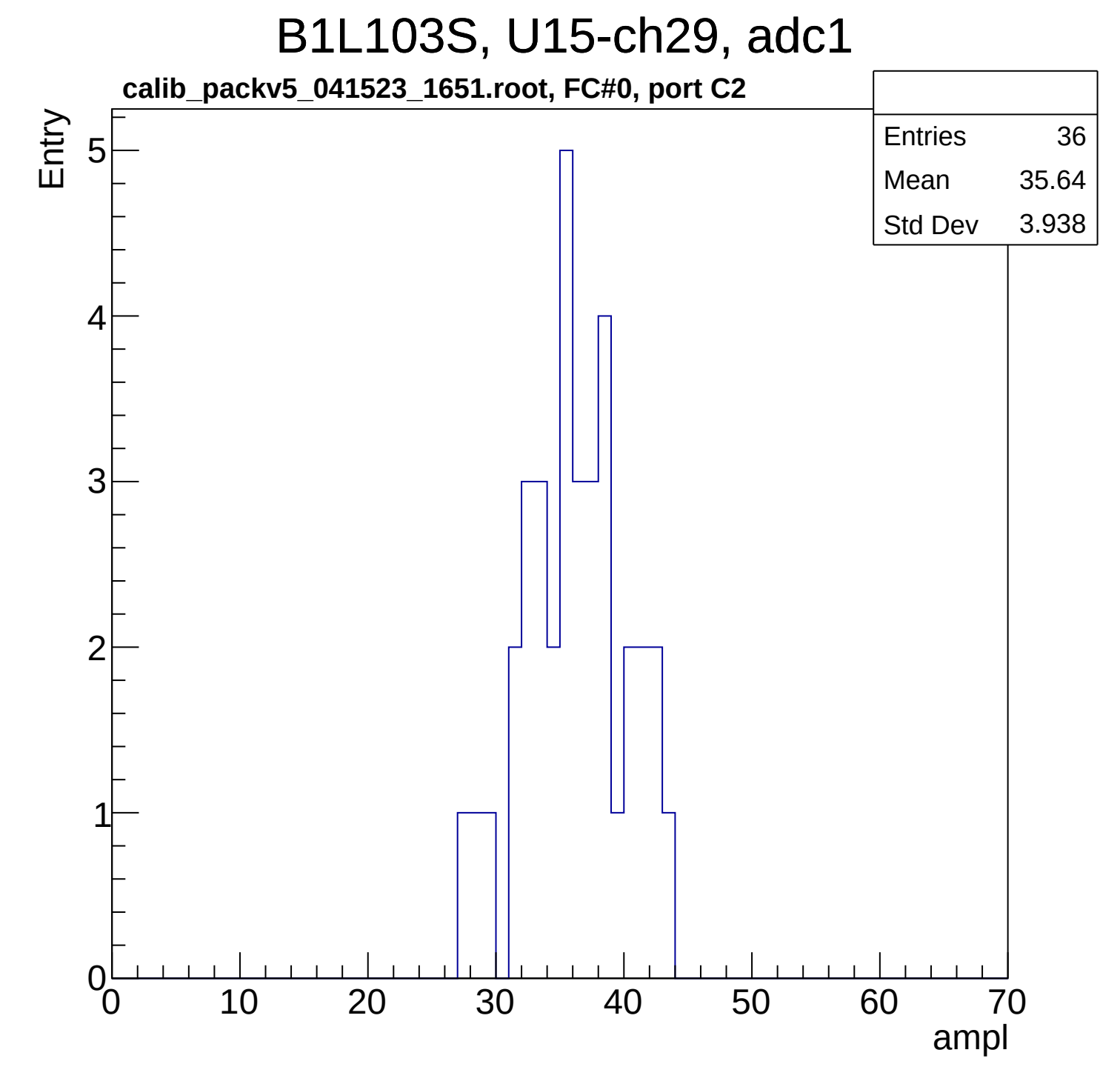

B1L103S, U15-ch28, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 52.69
Std Dev 3.283
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

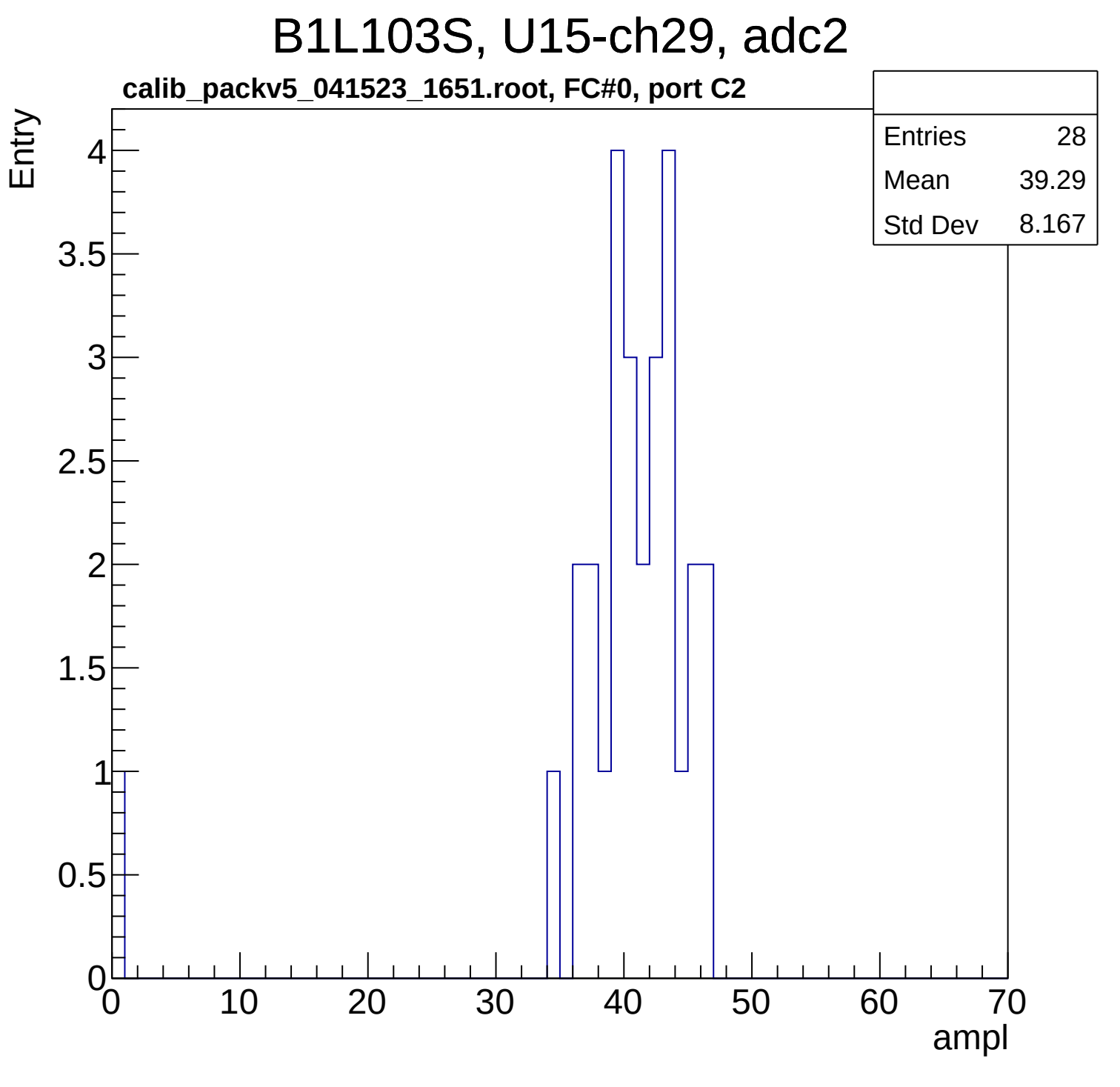

B1L103S, U15-ch28, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 56.28
Std Dev 11.18
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

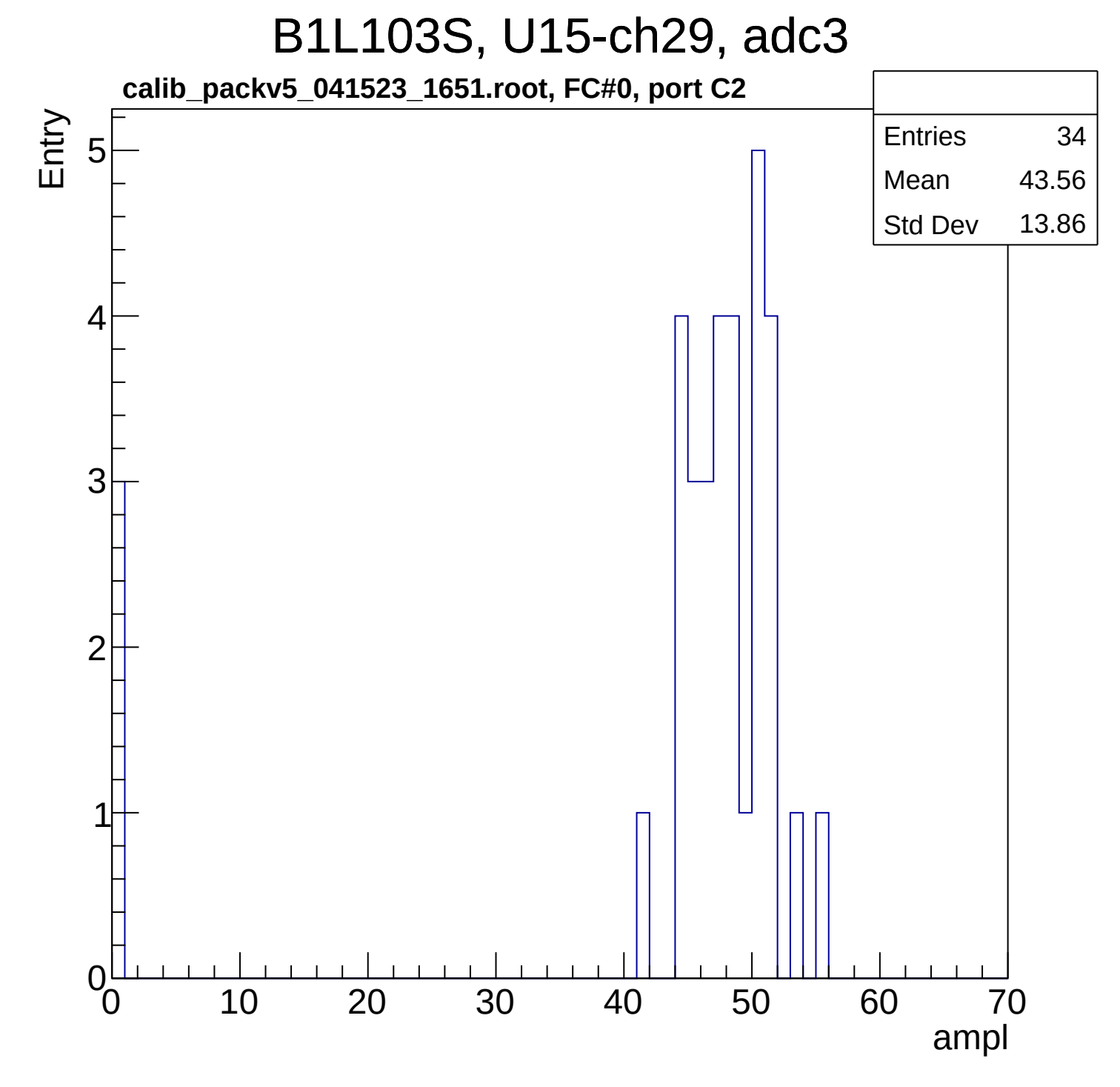

B1L103S, U15-ch28, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 60.73
Std Dev 1.863
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

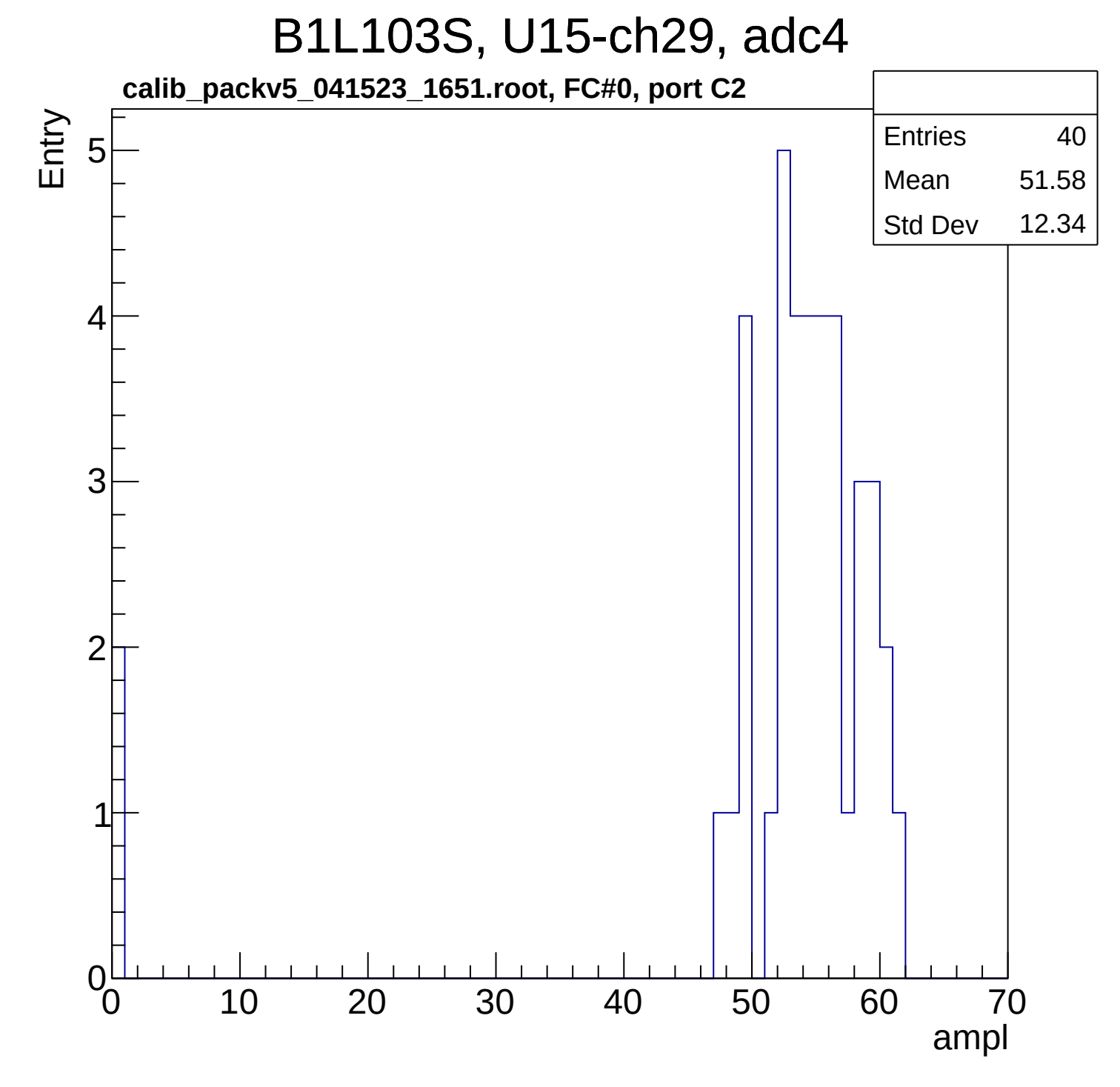

B1L103S, U15-ch28, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

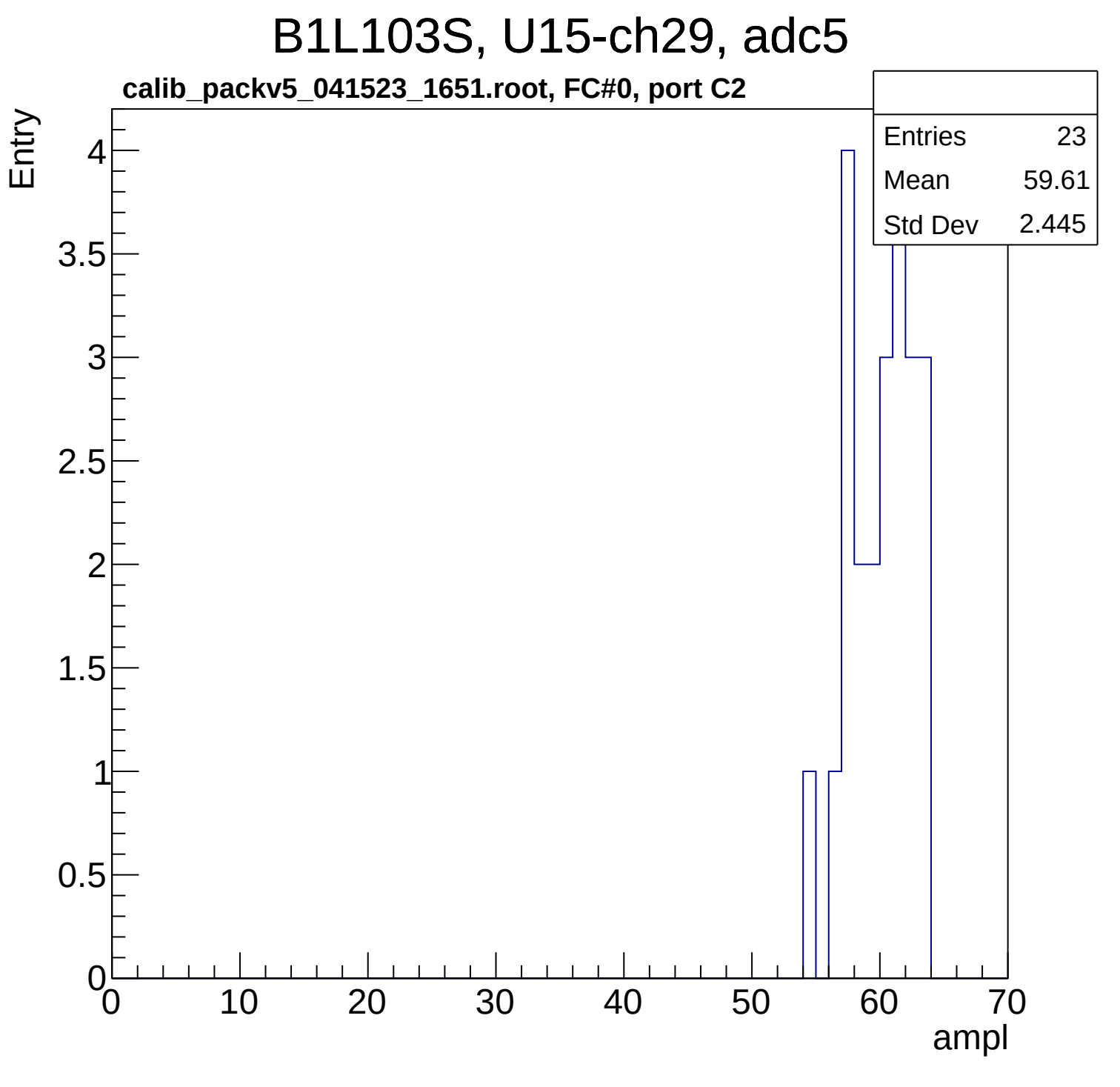

B1L103S, U15-ch29, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 24.81
Std Dev 10.32
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

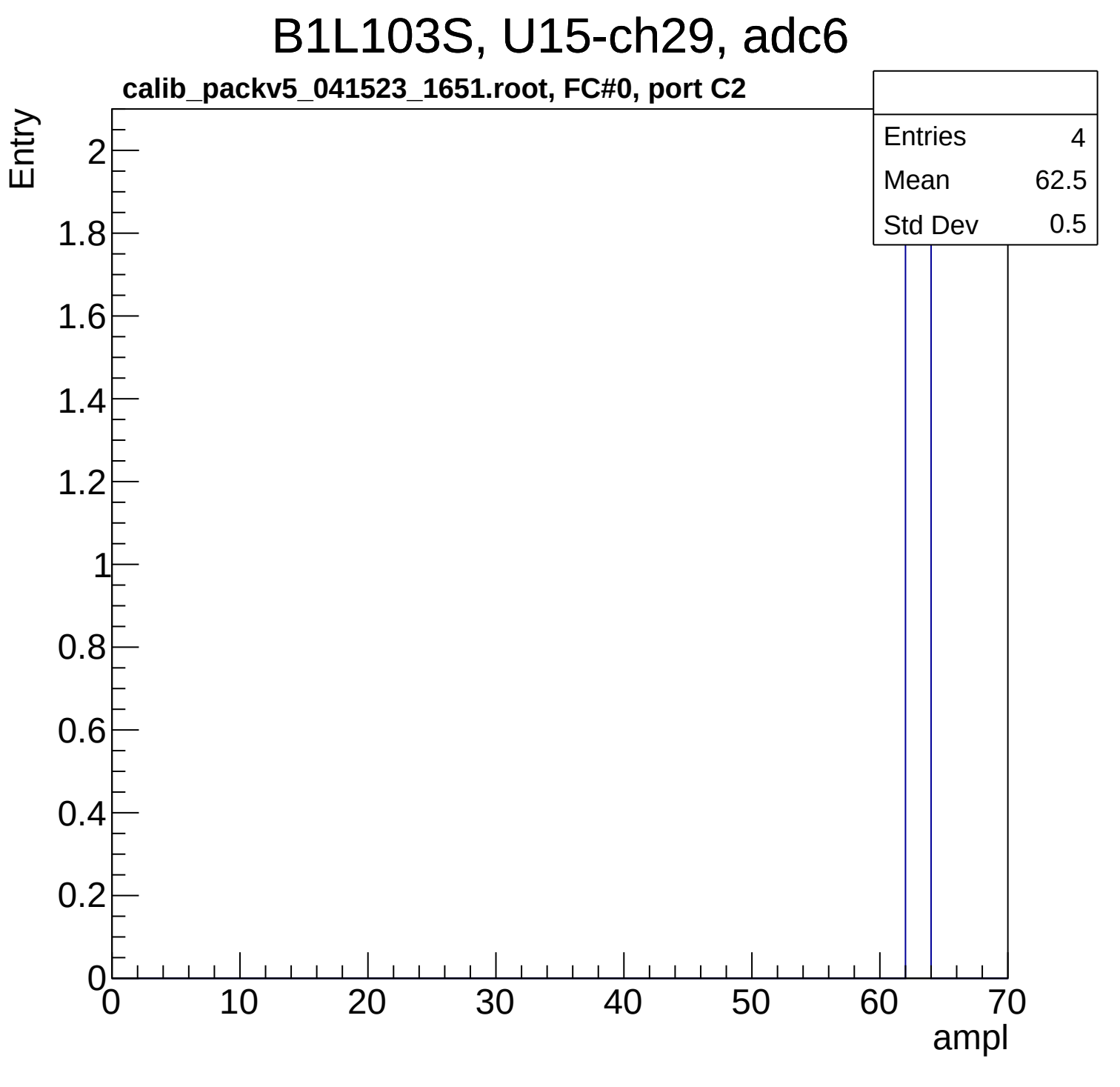

B1L103S, U15-ch29, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 35.64
Std Dev 3.938
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

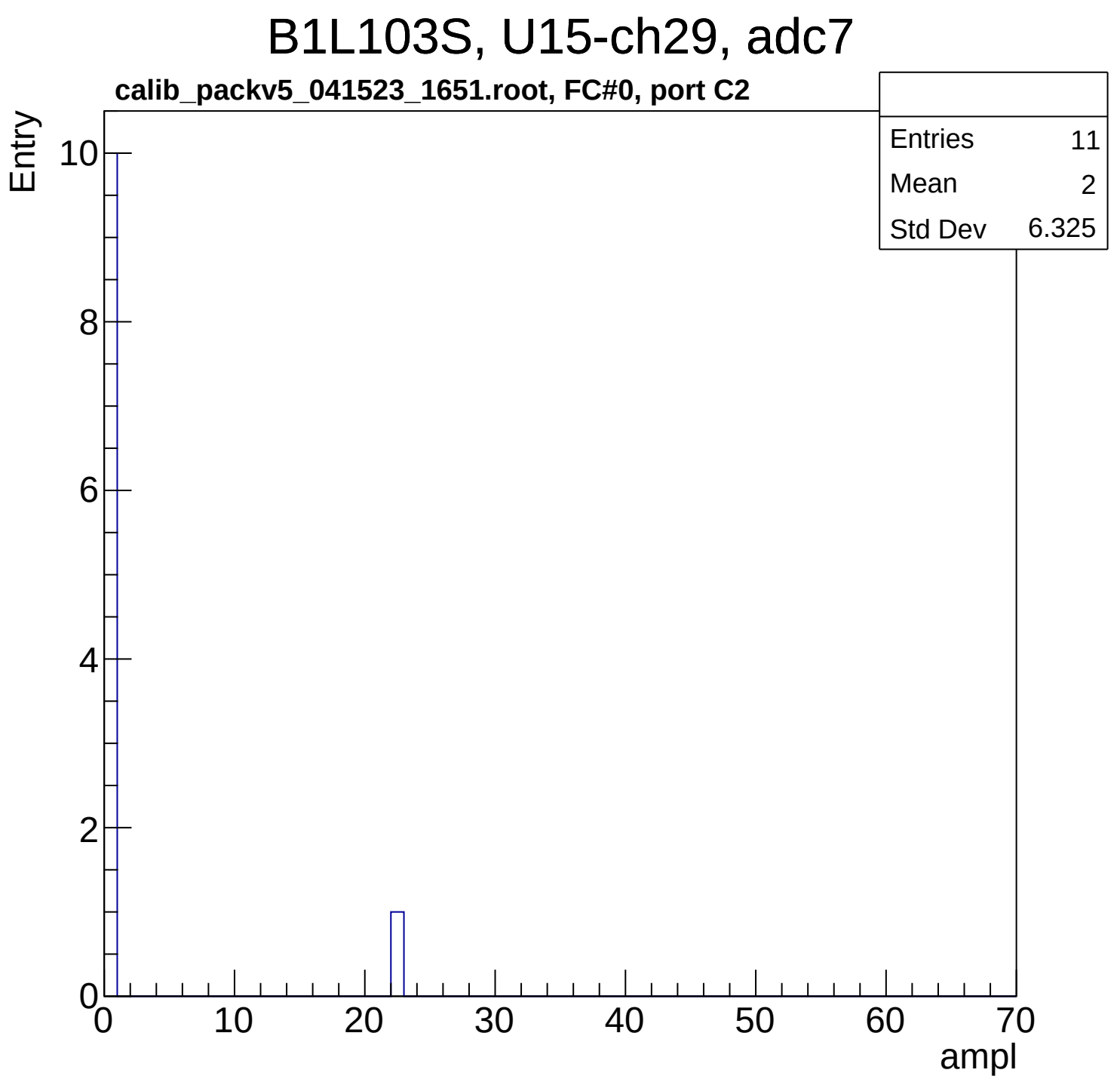

B1L103S, U15-ch29, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 39.29
Std Dev 8.167
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

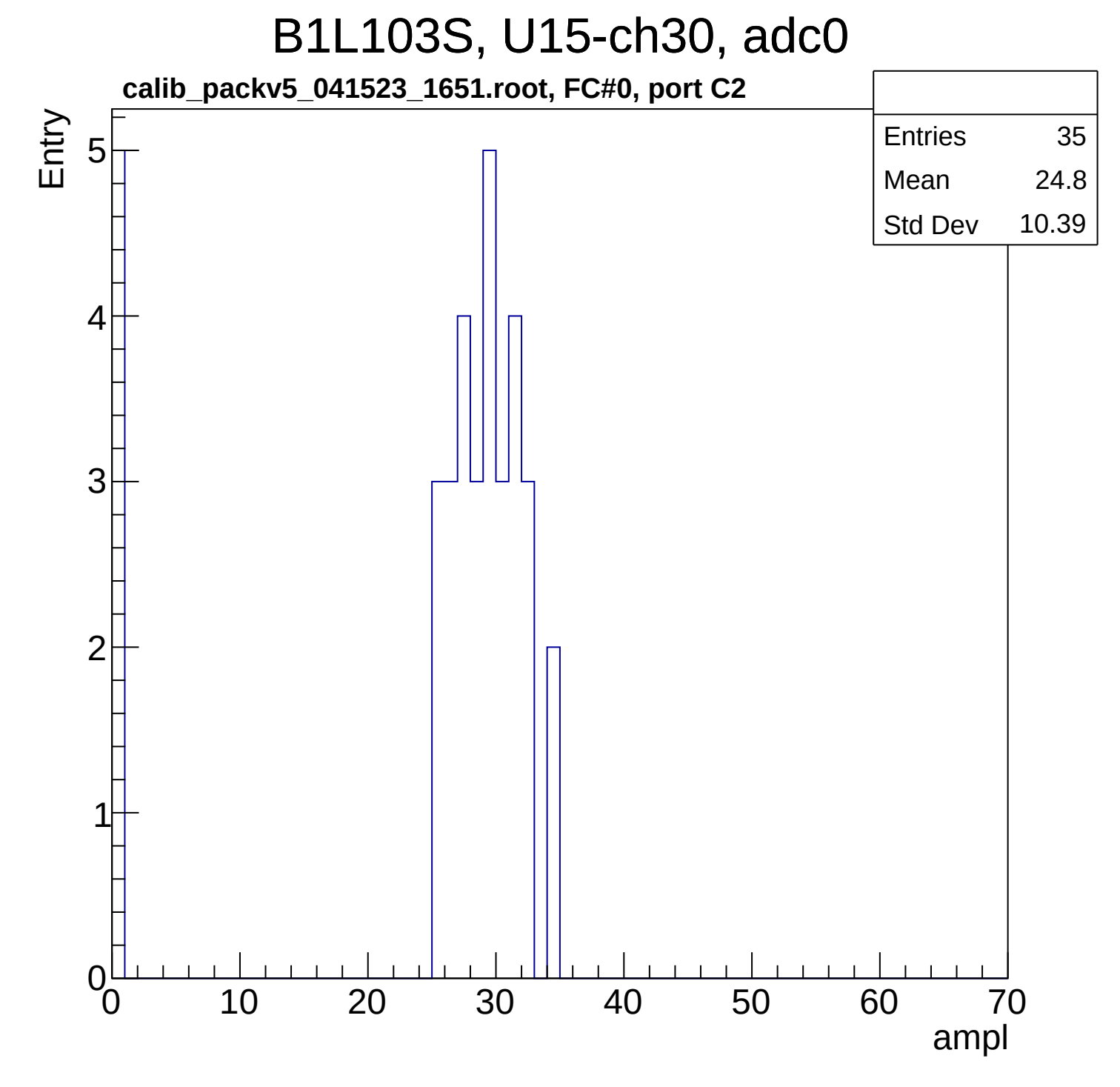

B1L103S, U15-ch29, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 43.56
Std Dev 13.86
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

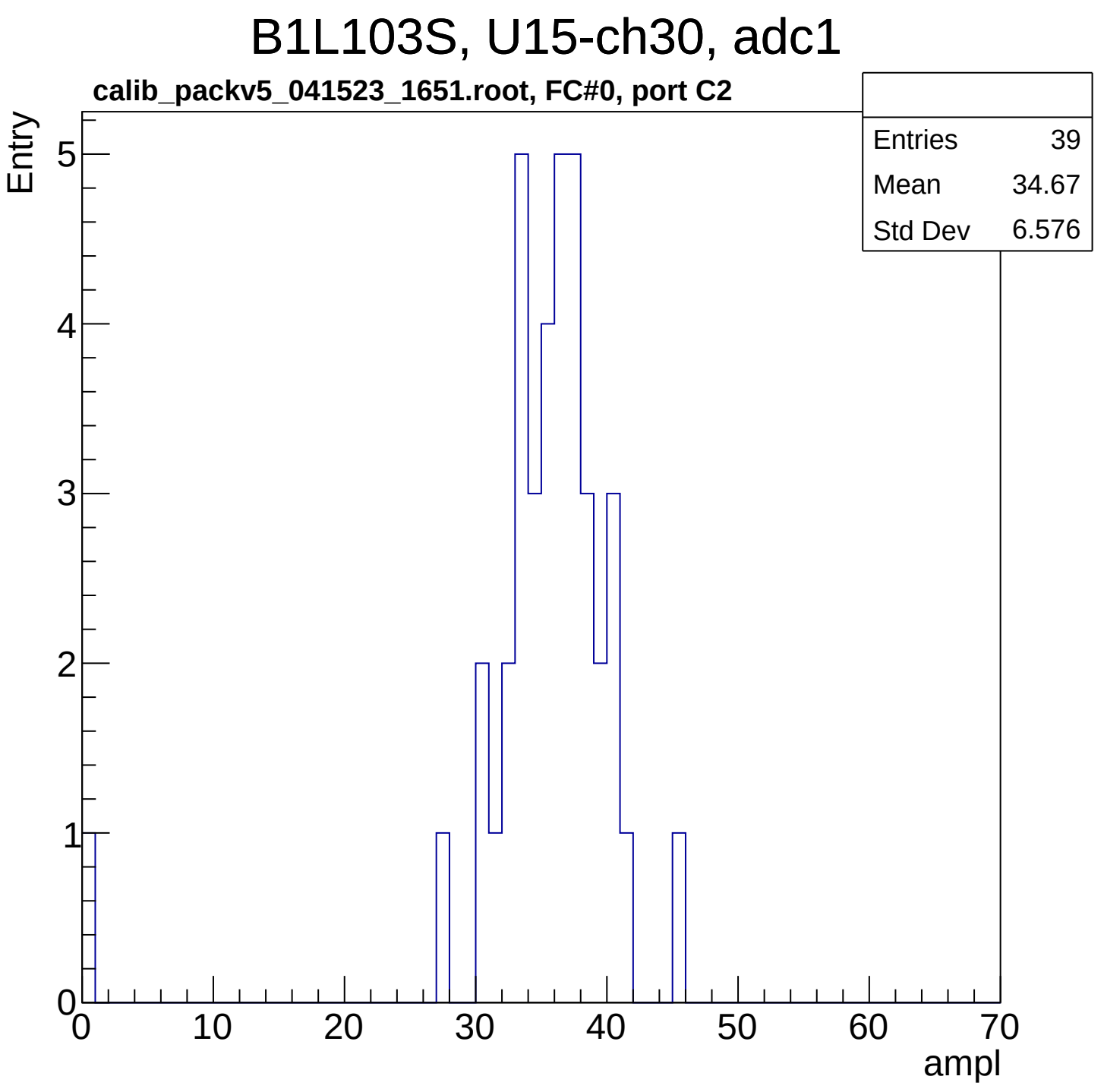

B1L103S, U15-ch29, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 51.58
Std Dev 12.34
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

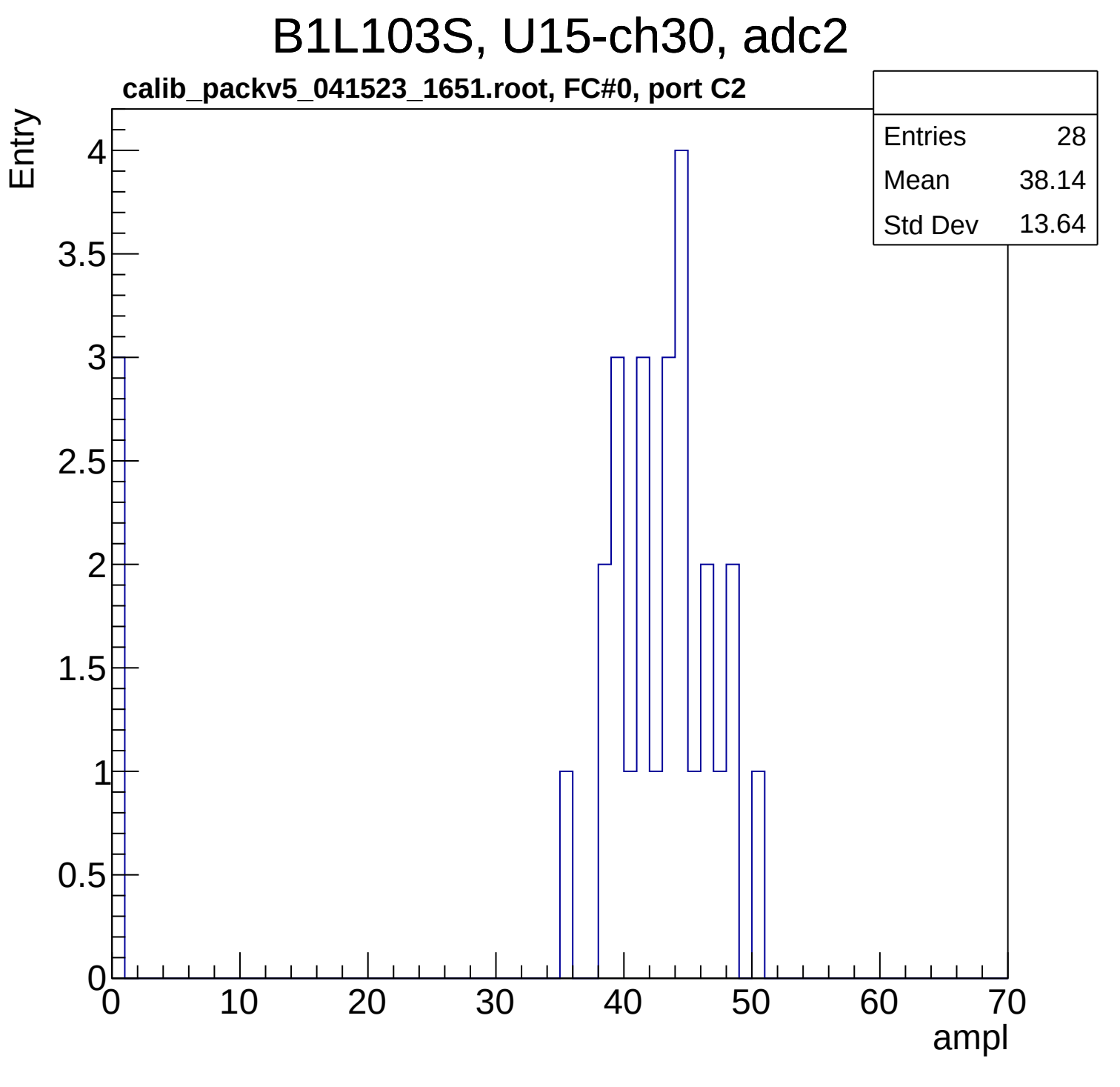

B1L103S, U15-ch29, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 59.61
Std Dev 2.445
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch29, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.5
Std Dev 0.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U15-ch29, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 2
Std Dev 6.325
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch30, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 24.8
Std Dev 10.39
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch30, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 34.67
Std Dev 6.576
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch30, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 38.14
Std Dev 13.64
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
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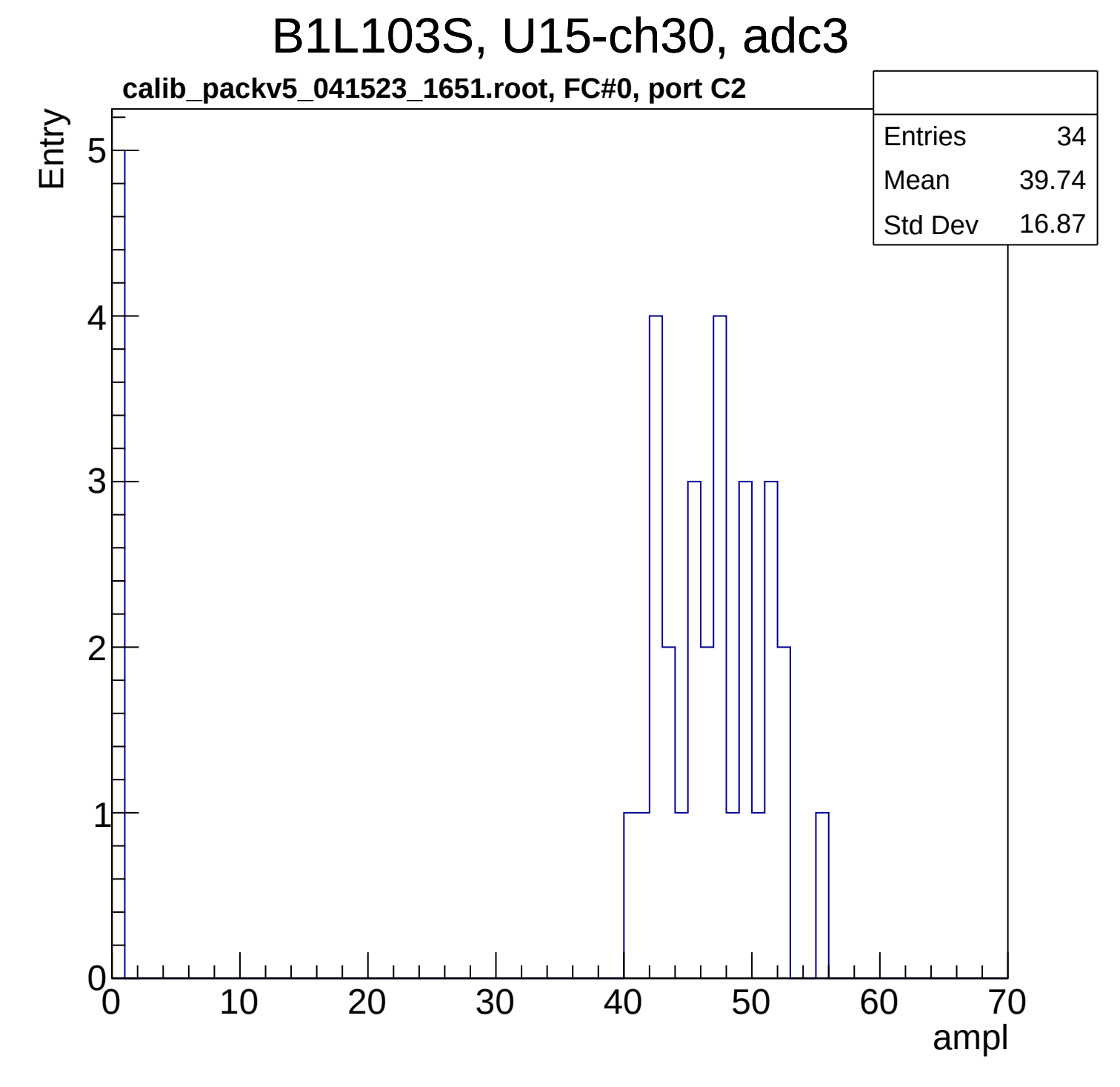
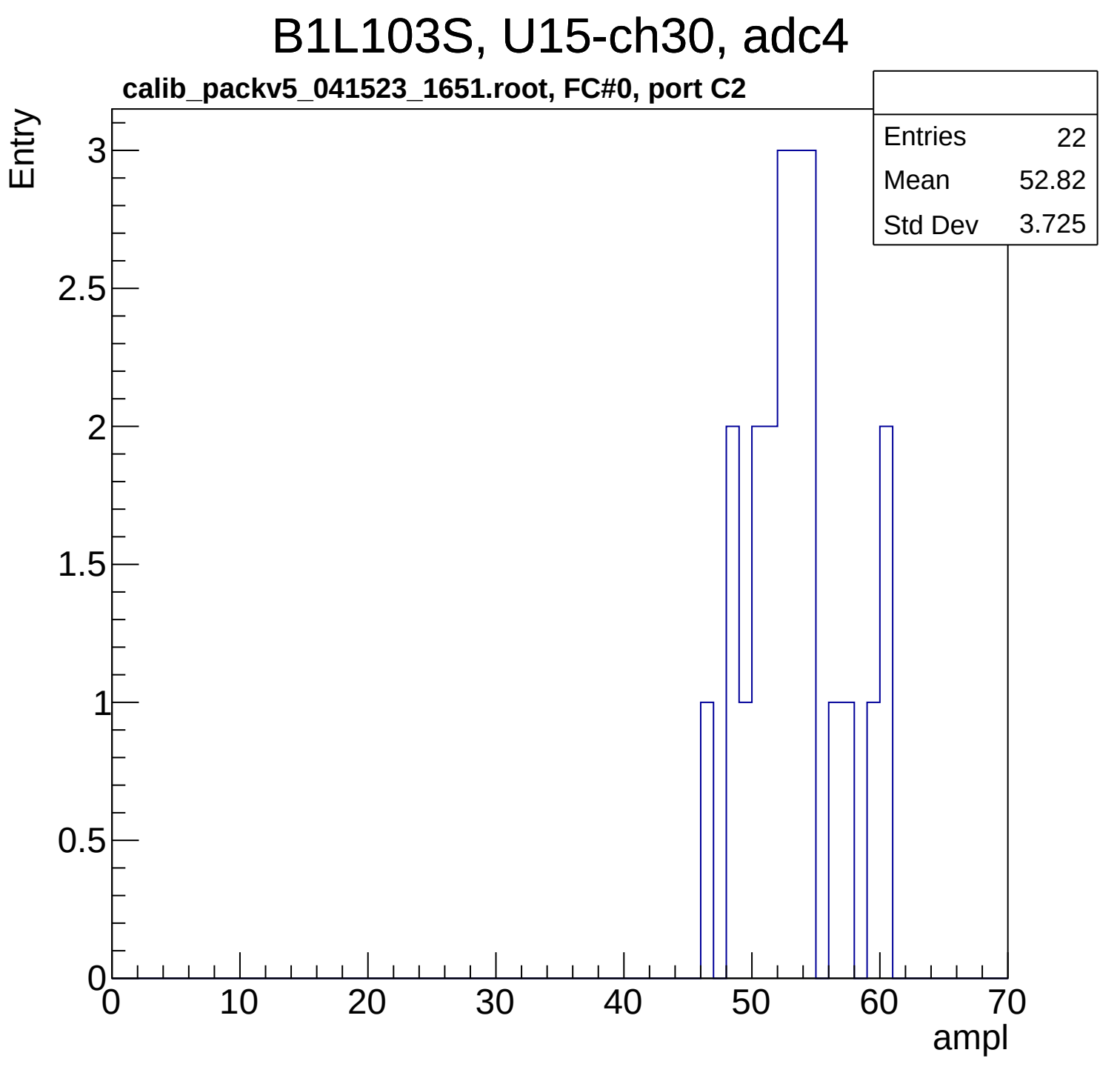
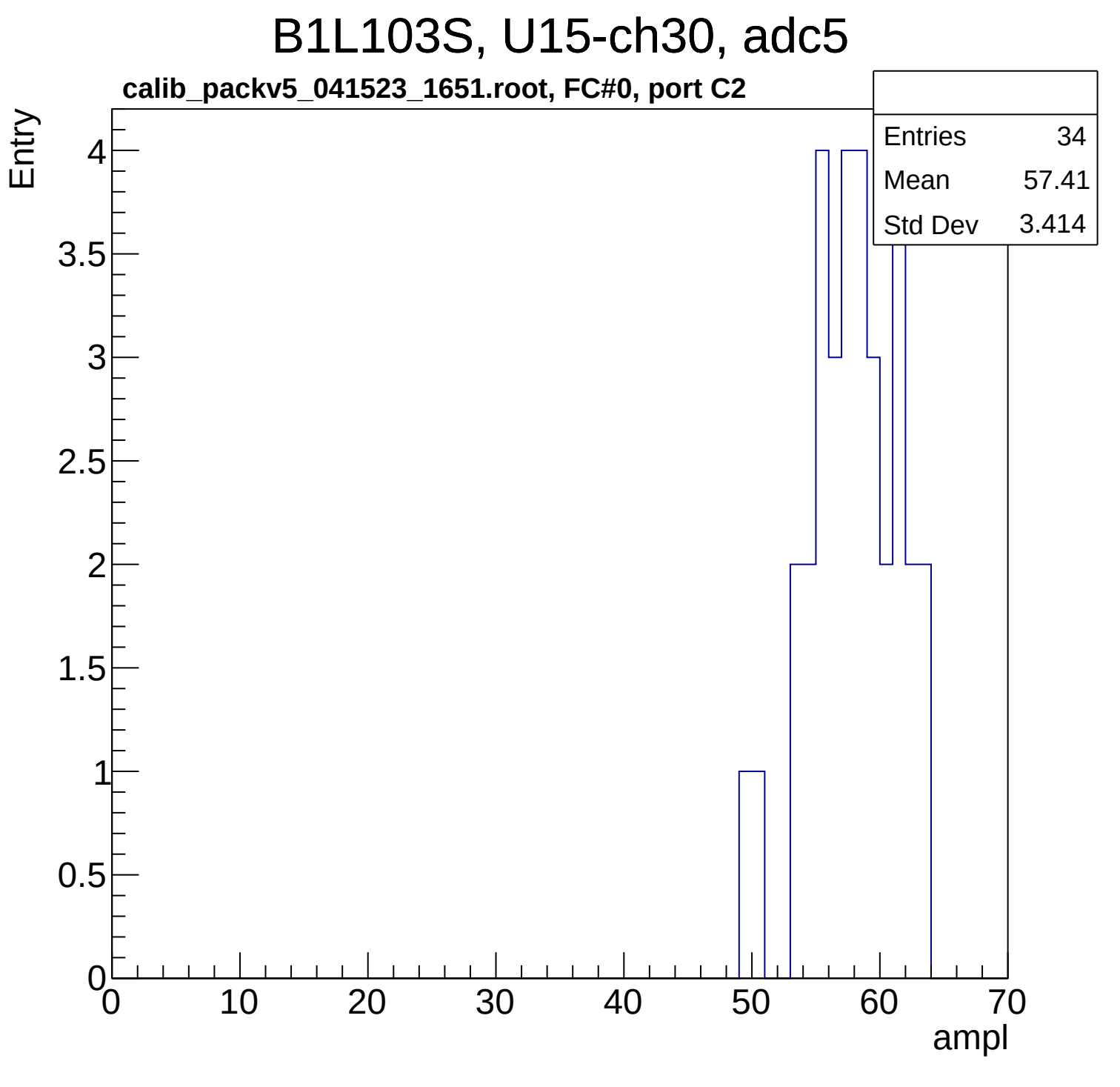
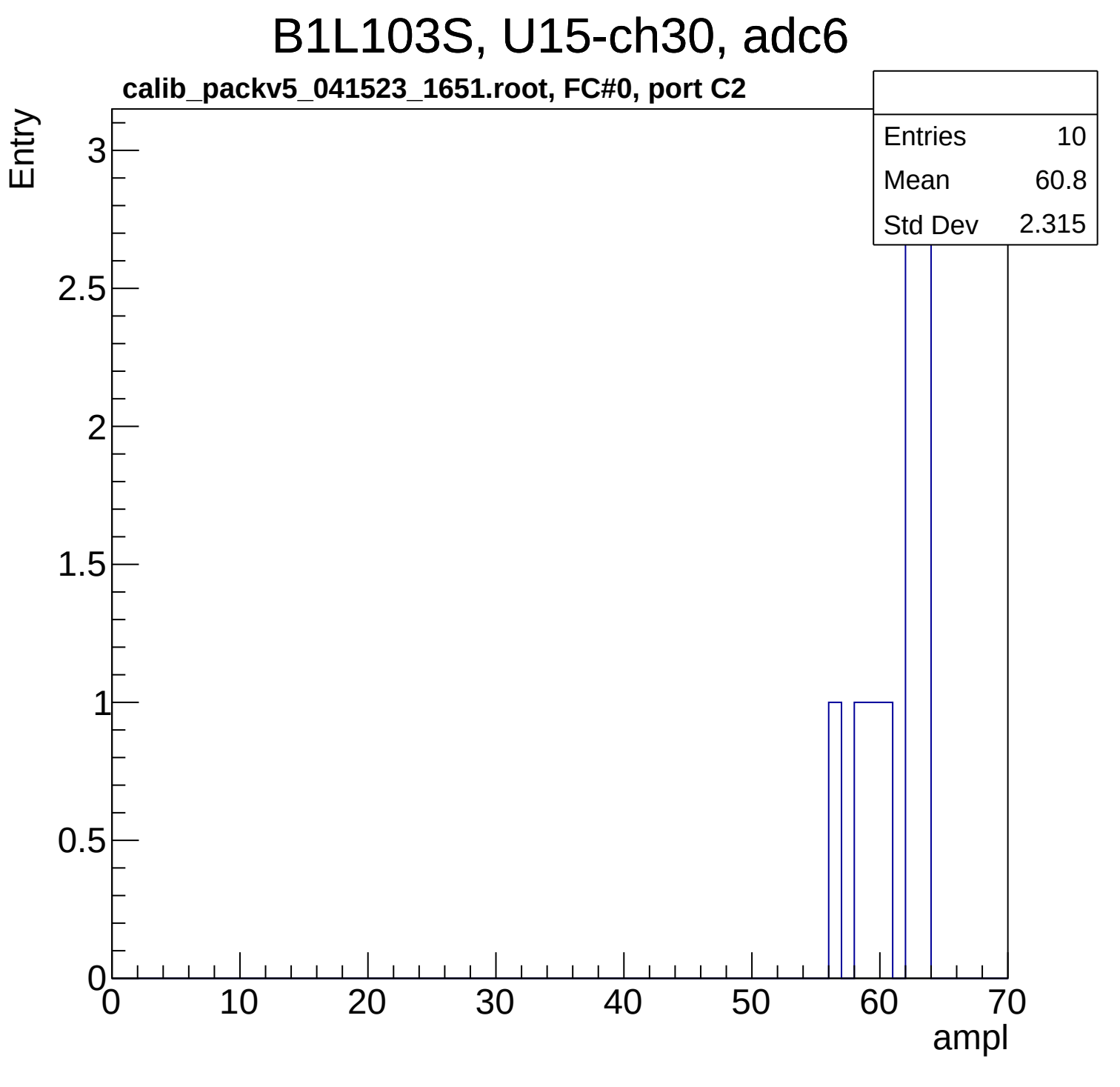
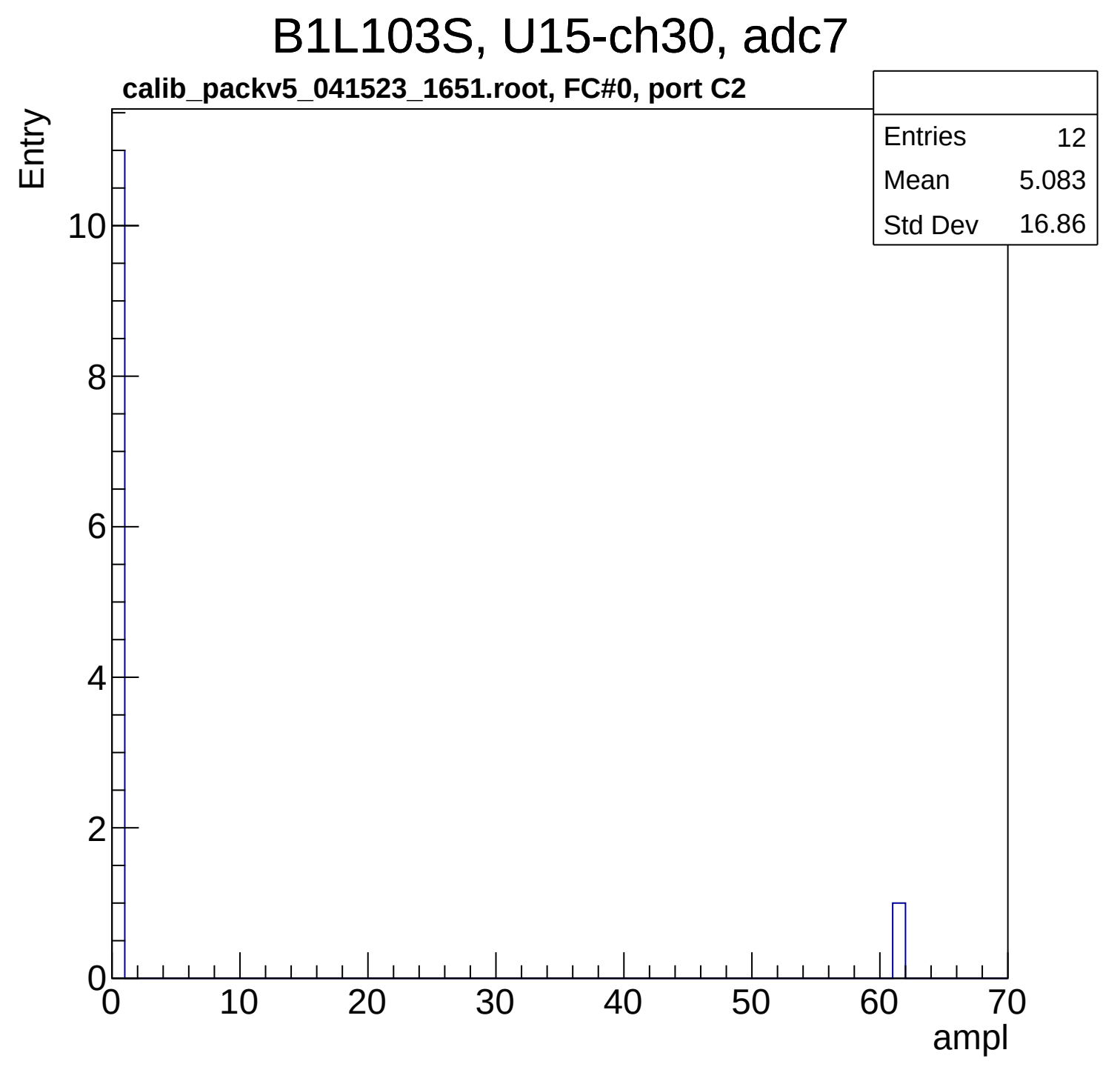
20
30
40
50
60
70

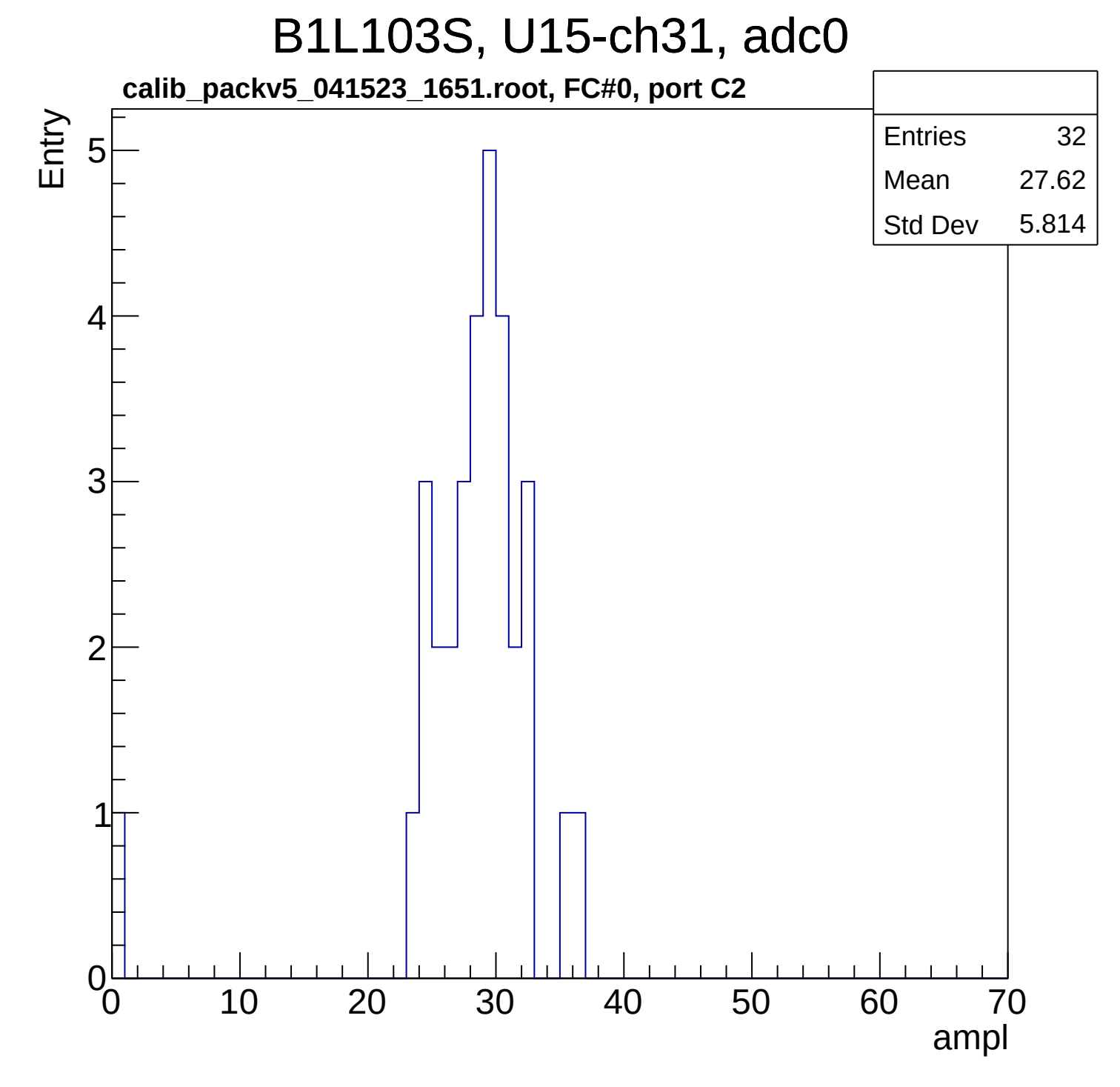

B1L103S, U15-ch30, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 39.74
Std Dev 16.87
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

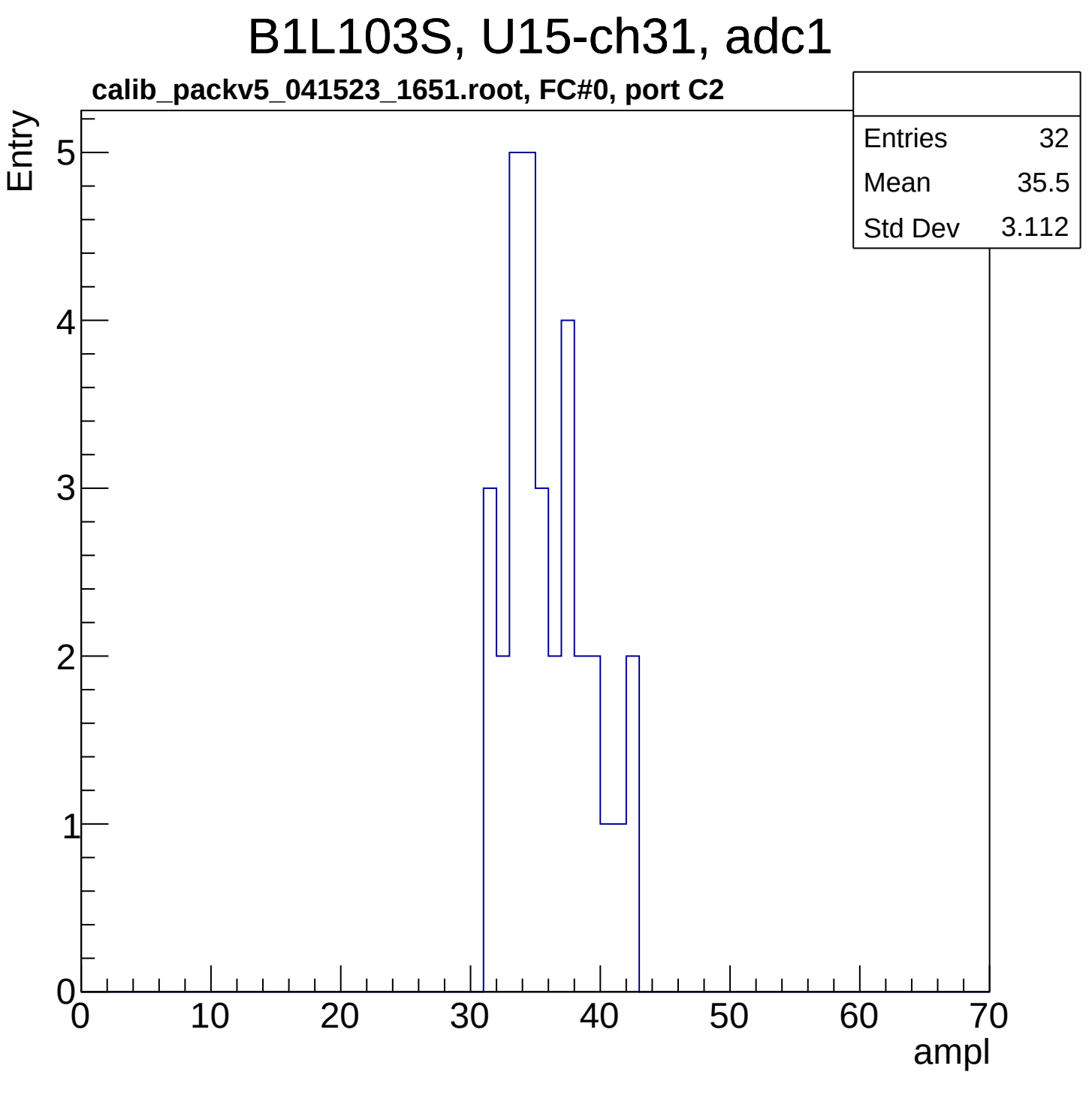

B1L103S, U15-ch30, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 52.82
Std Dev 3.725
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

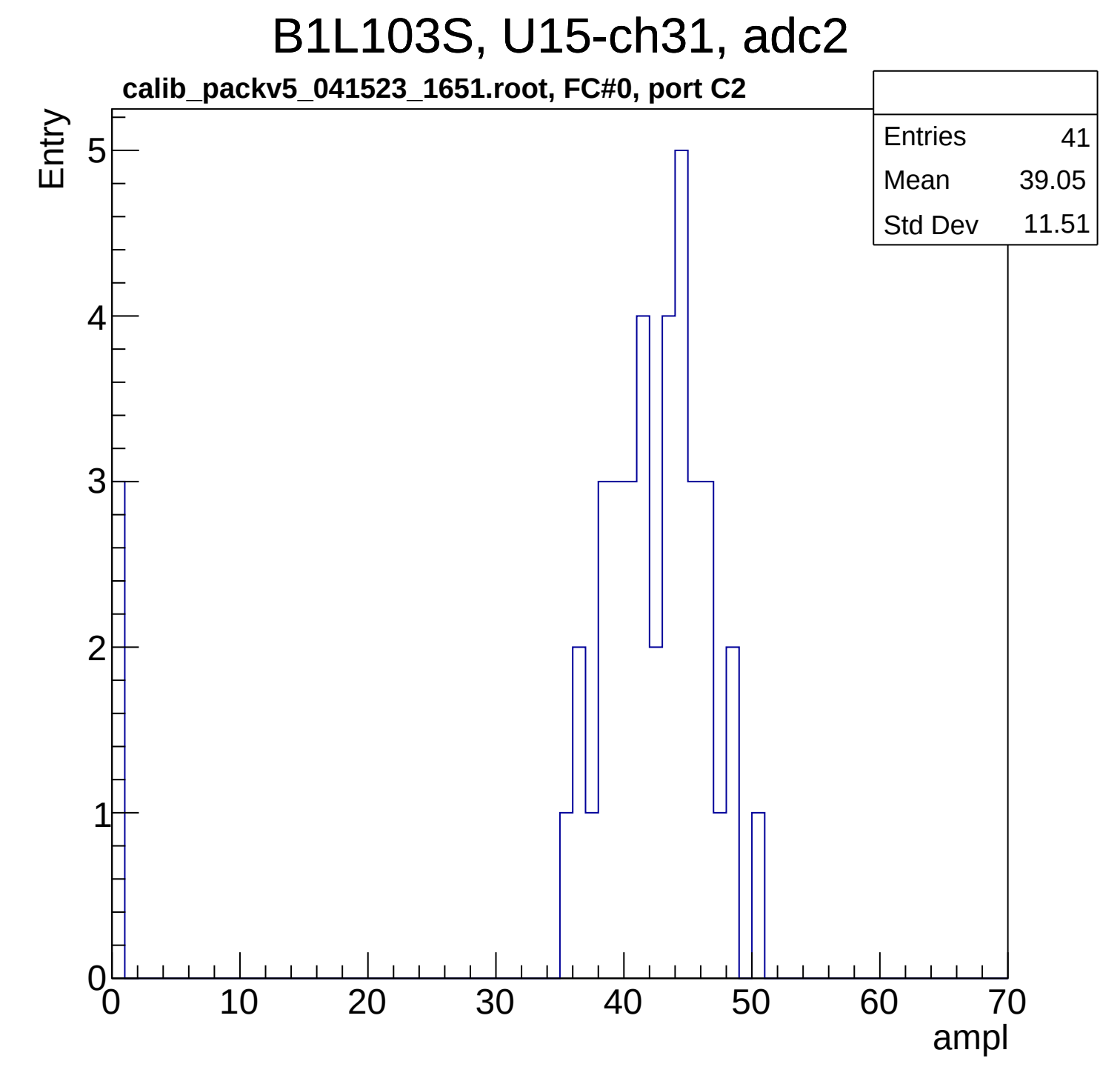

B1L103S, U15-ch30, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 57.41
Std Dev 3.414
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

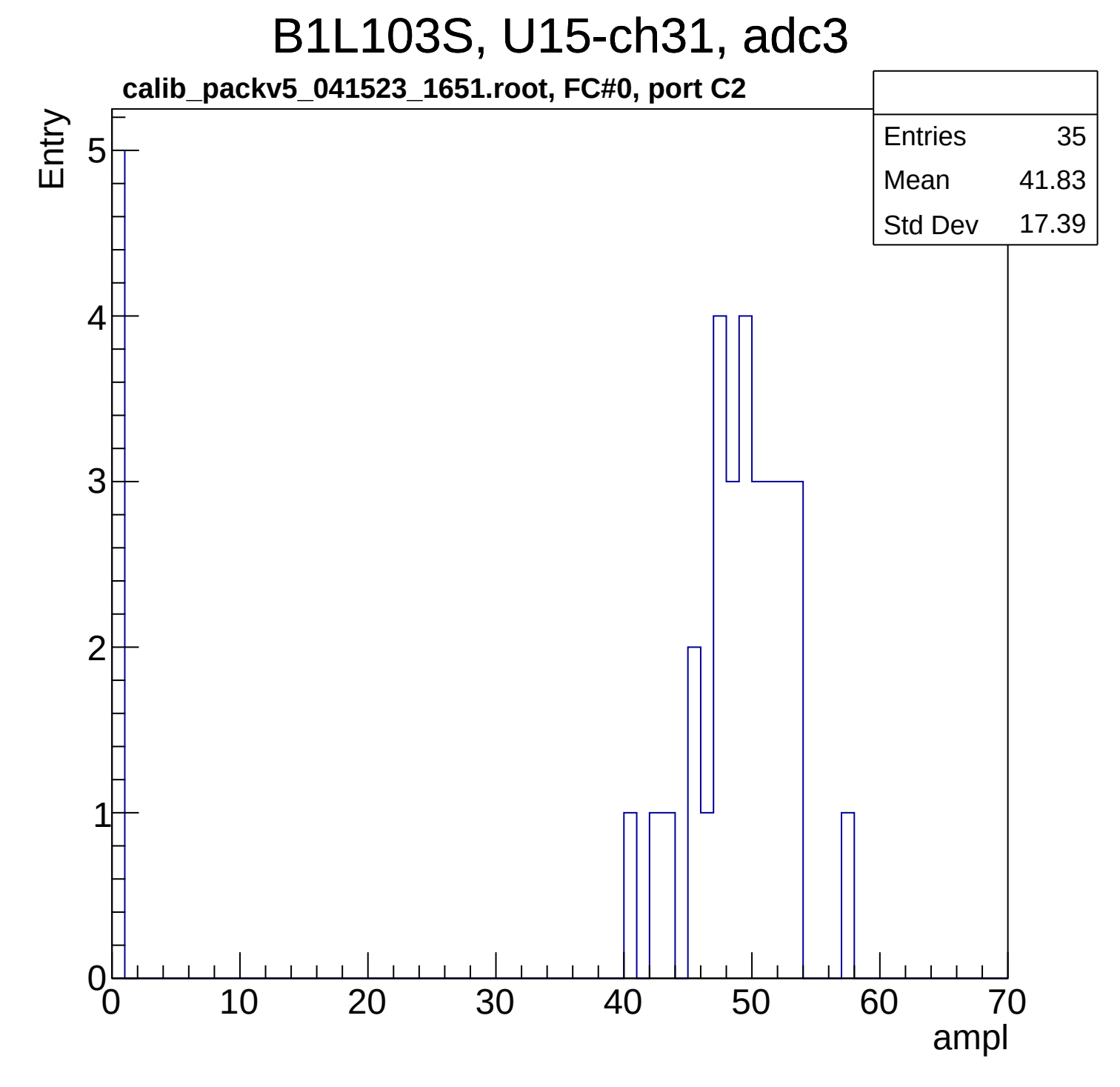

B1L103S, U15-ch30, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 60.8
Std Dev 2.315
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

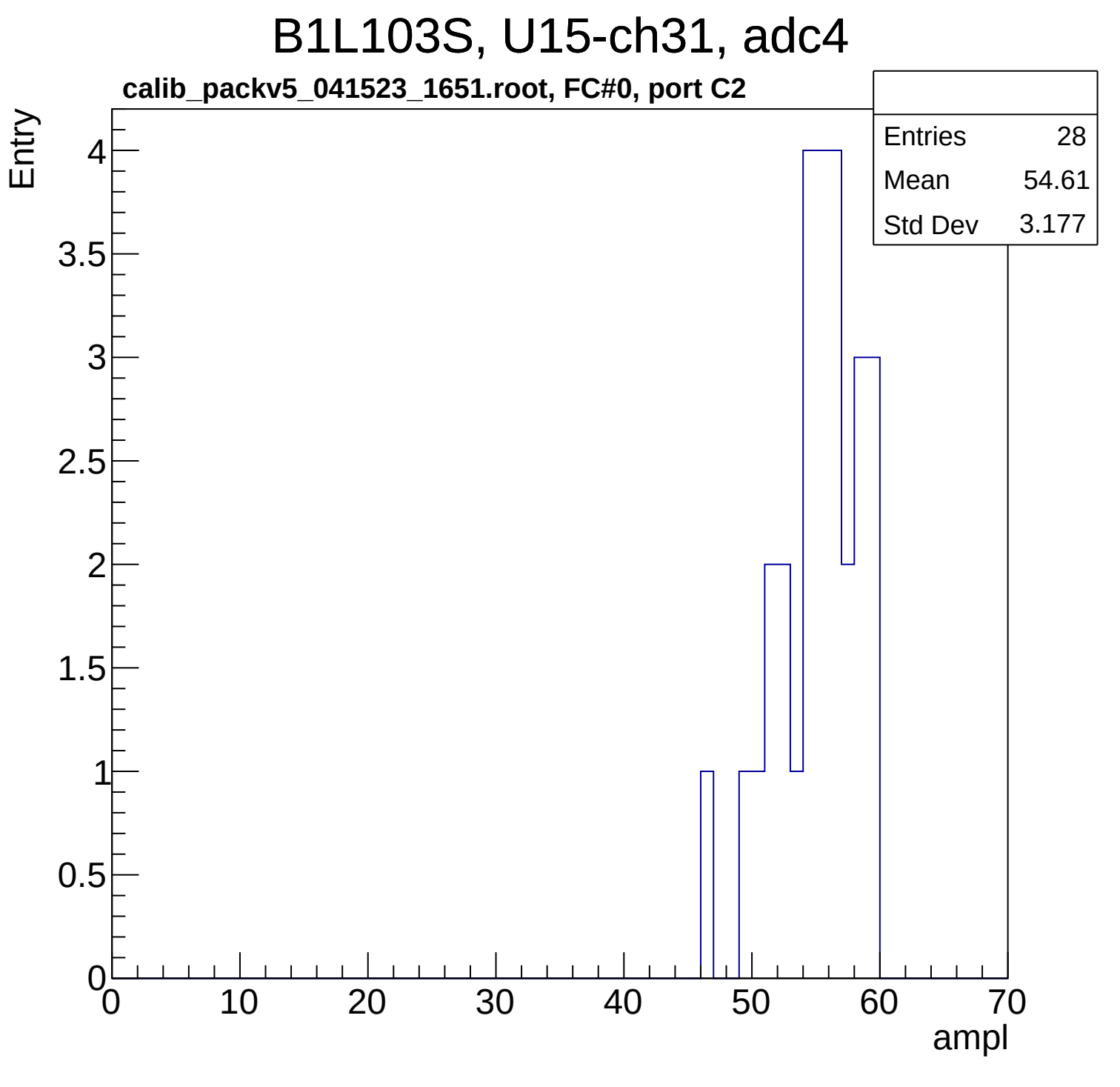

B1L103S, U15-ch30, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 5.083
Std Dev 16.86
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

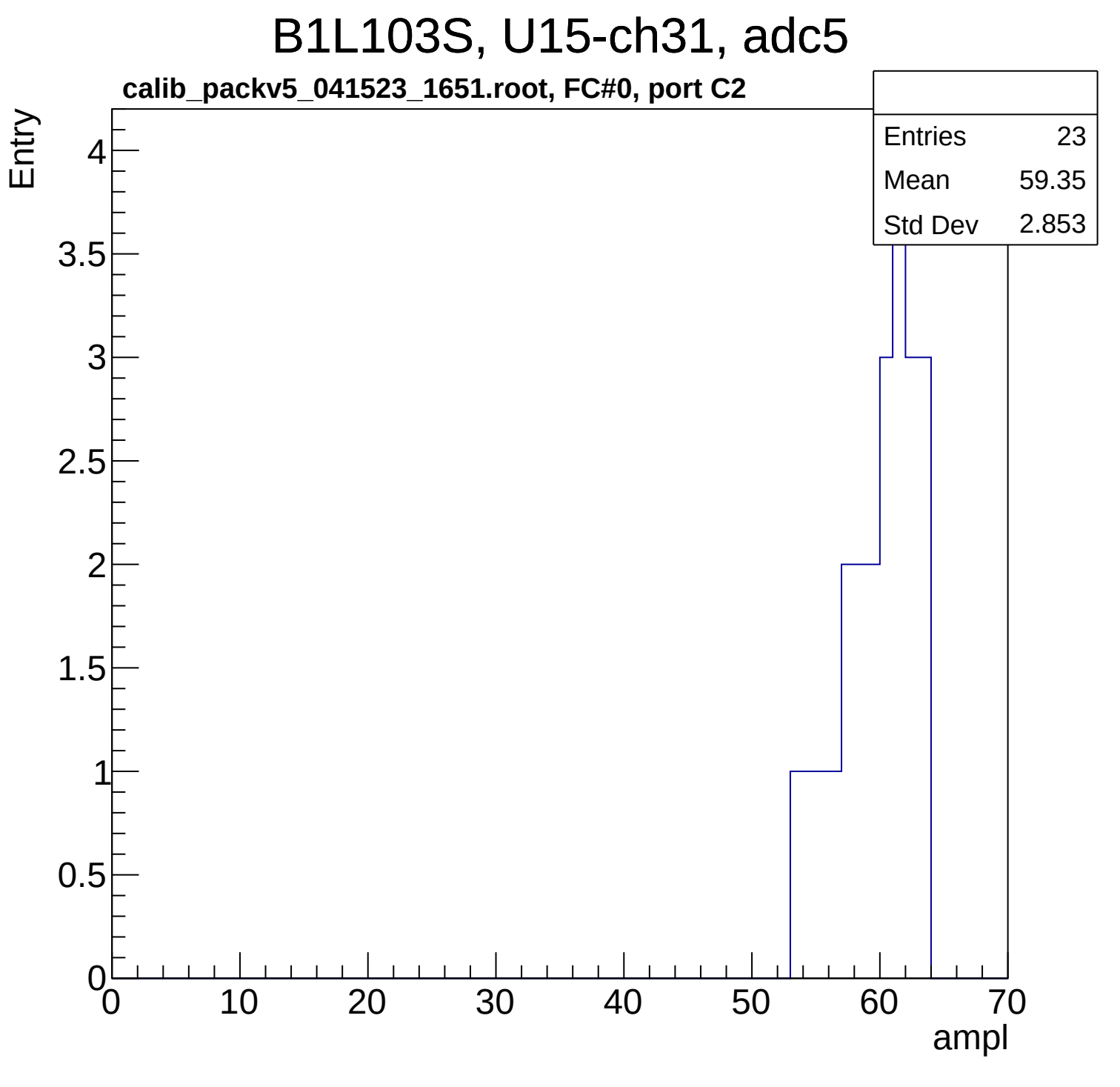

B1L103S, U15-ch31, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 27.62
Std Dev 5.814
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

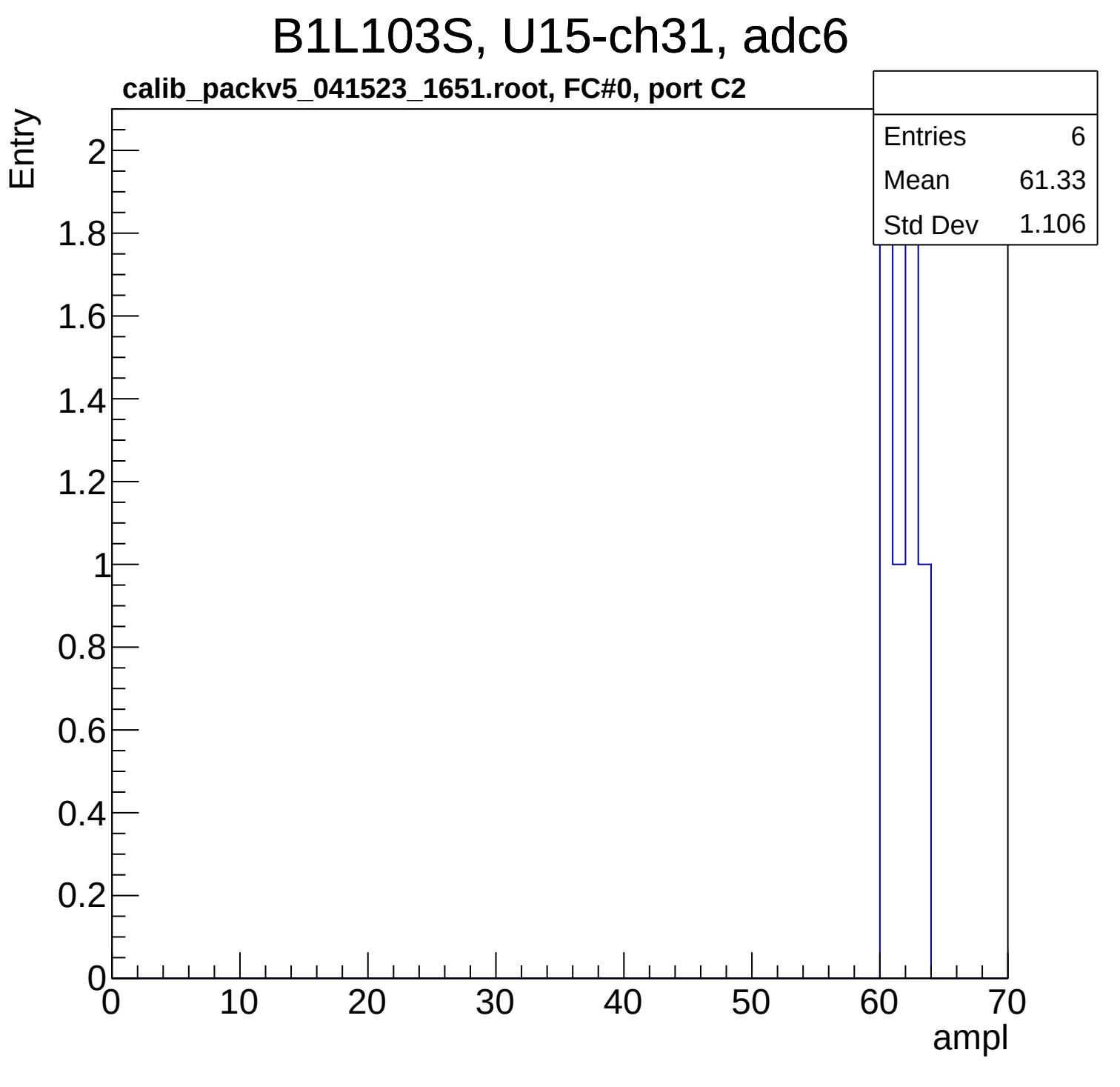

B1L103S, U15-ch31, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 35.5
Std Dev 3.112
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

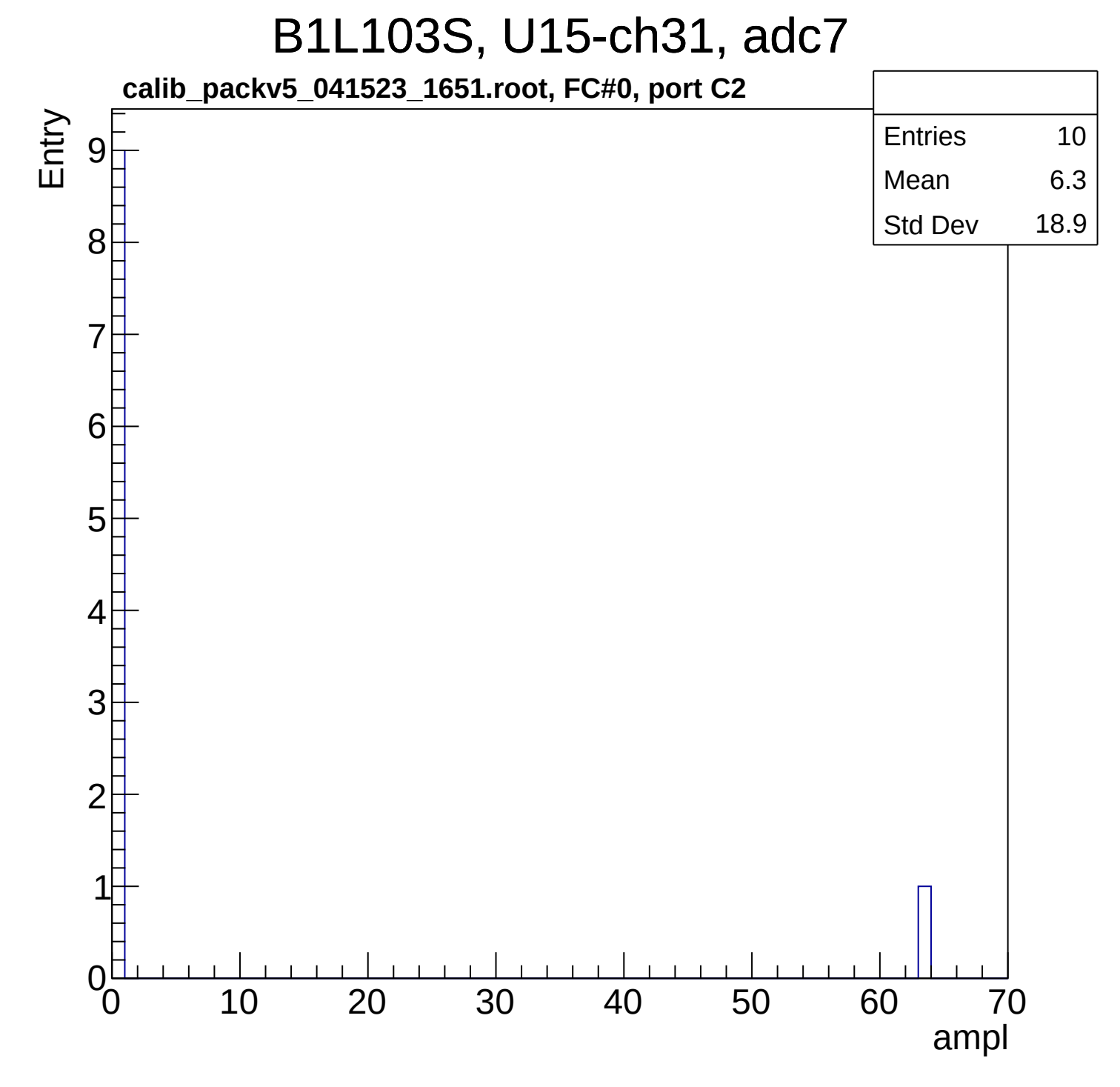

B1L103S, U15-ch31, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 39.05
Std Dev 11.51
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

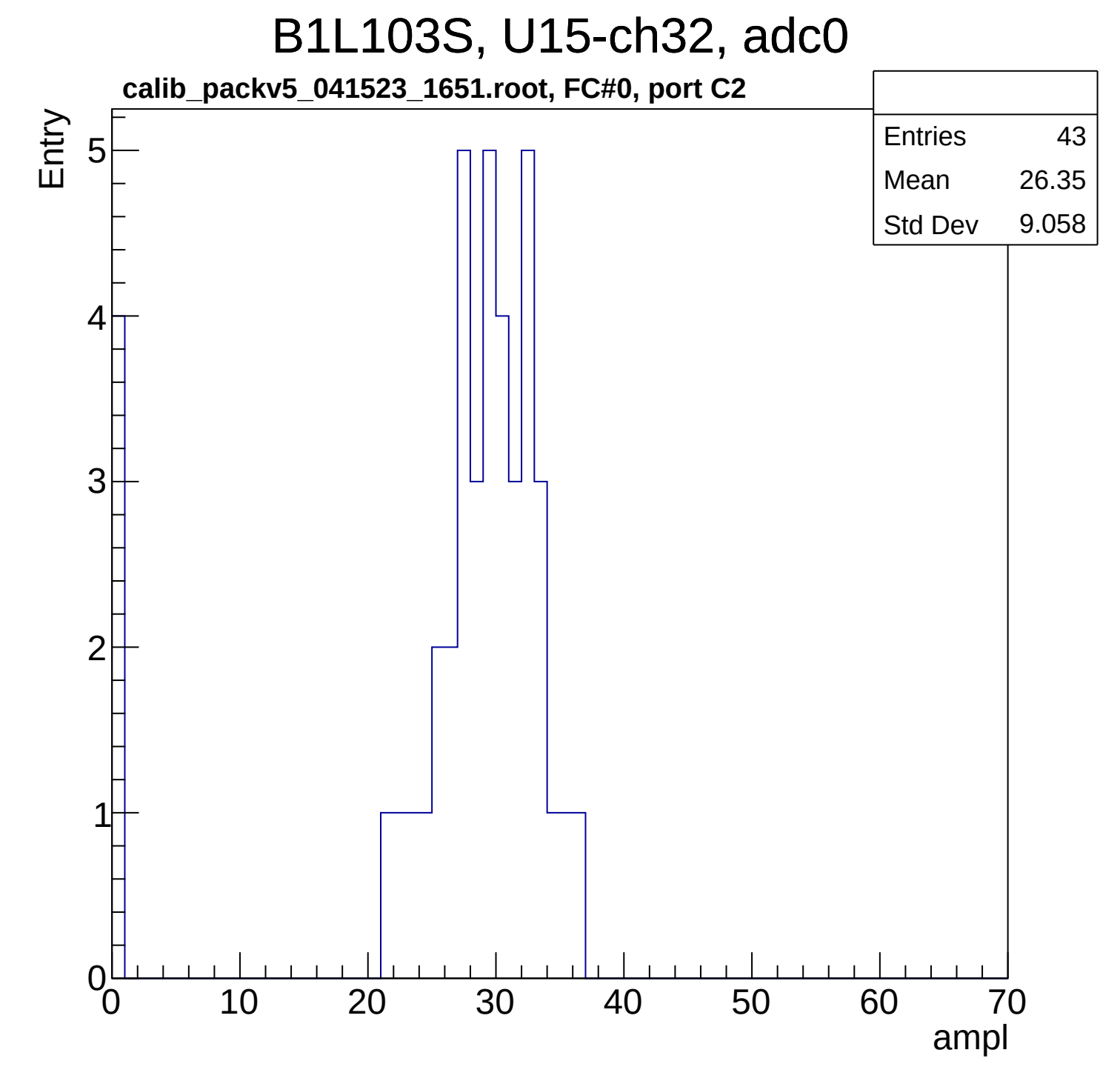

B1L103S, U15-ch31, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 41.83
Std Dev 17.39
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

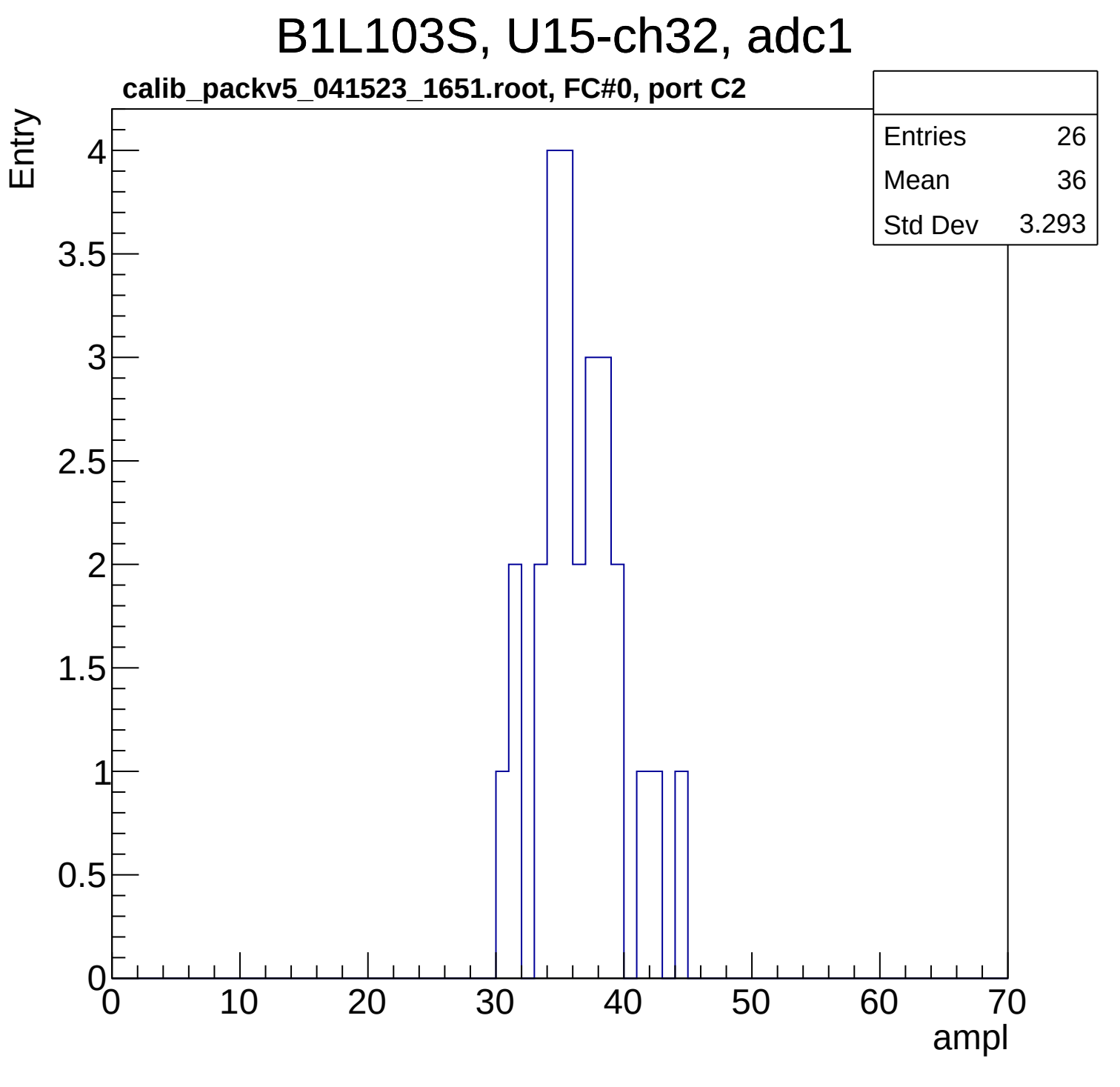

B1L103S, U15-ch31, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 54.61
Std Dev 3.177
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

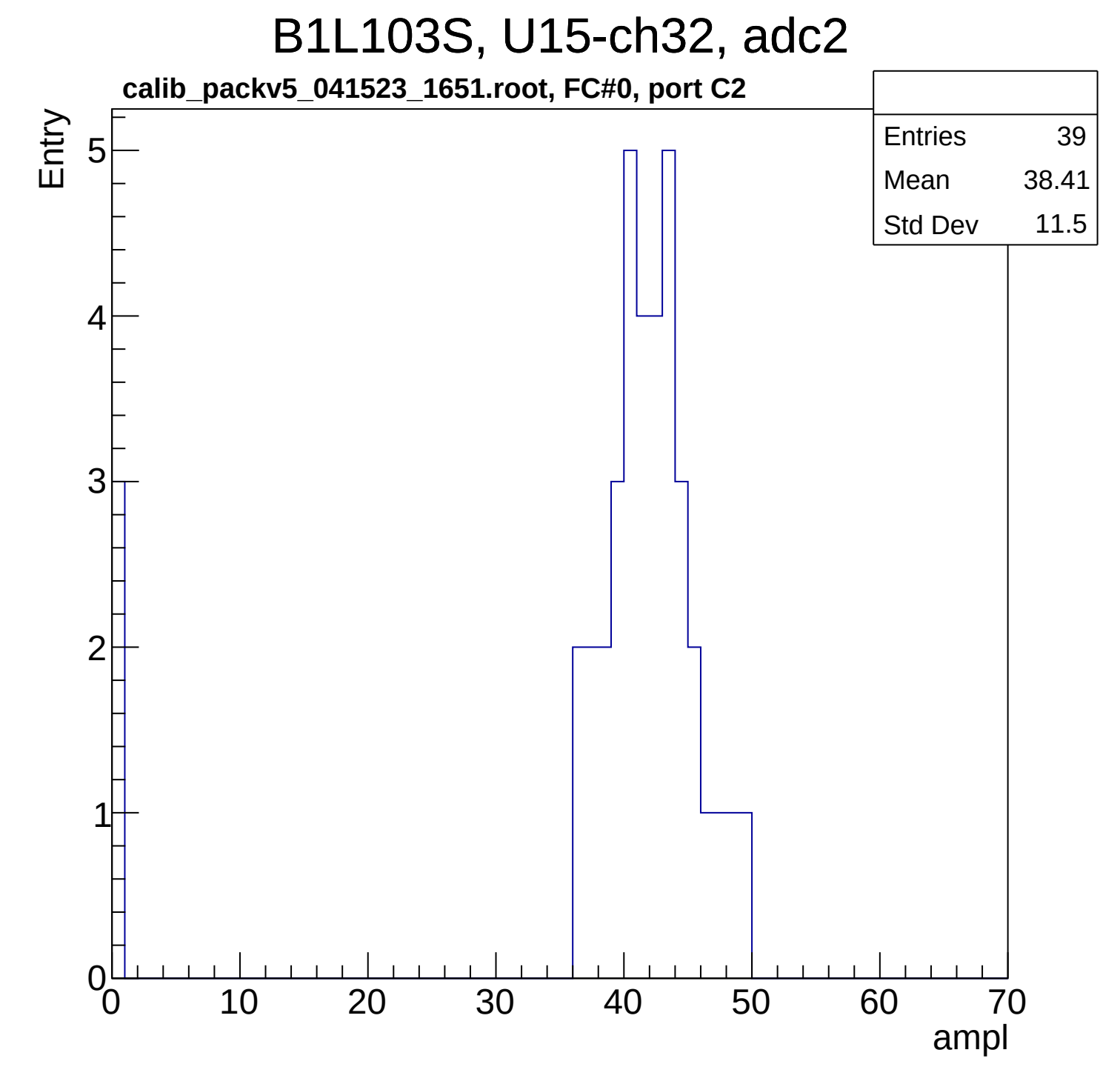

B1L103S, U15-ch31, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 59.35
Std Dev 2.853
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

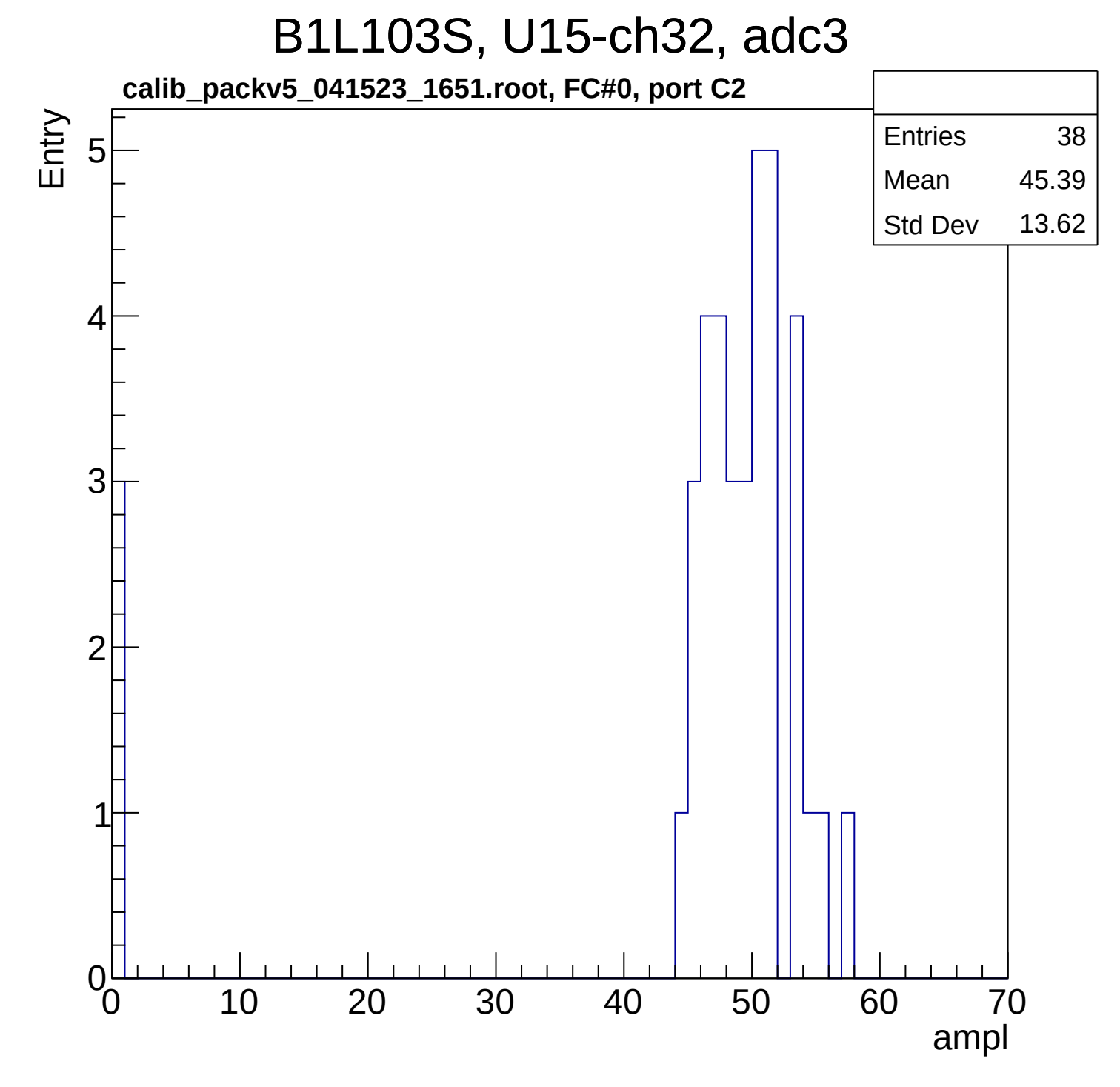

B1L103S, U15-ch31, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.33
Std Dev 1.106
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

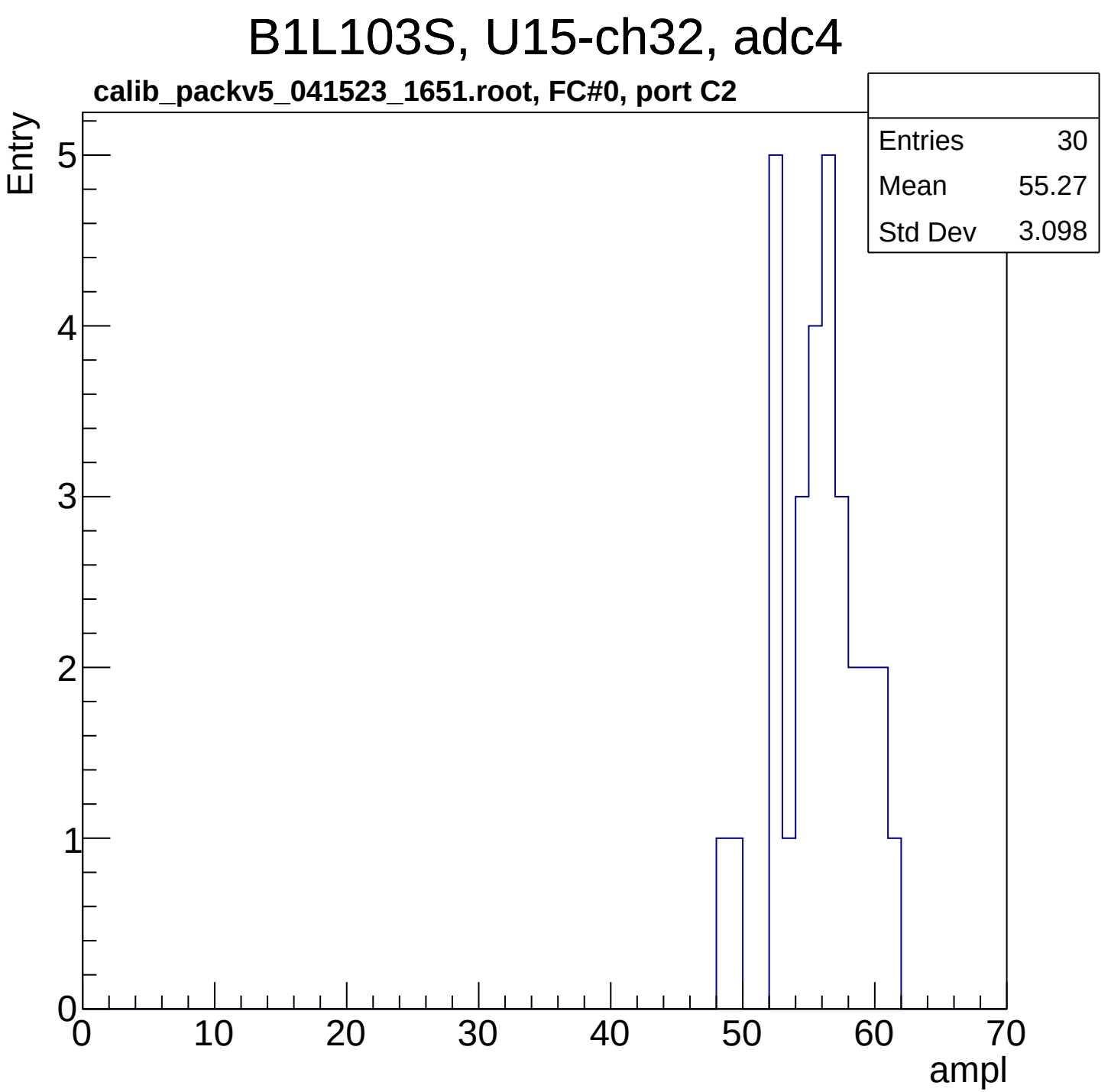

B1L103S, U15-ch31, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 6.3
Std Dev 18.9
Entry
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70
ampl

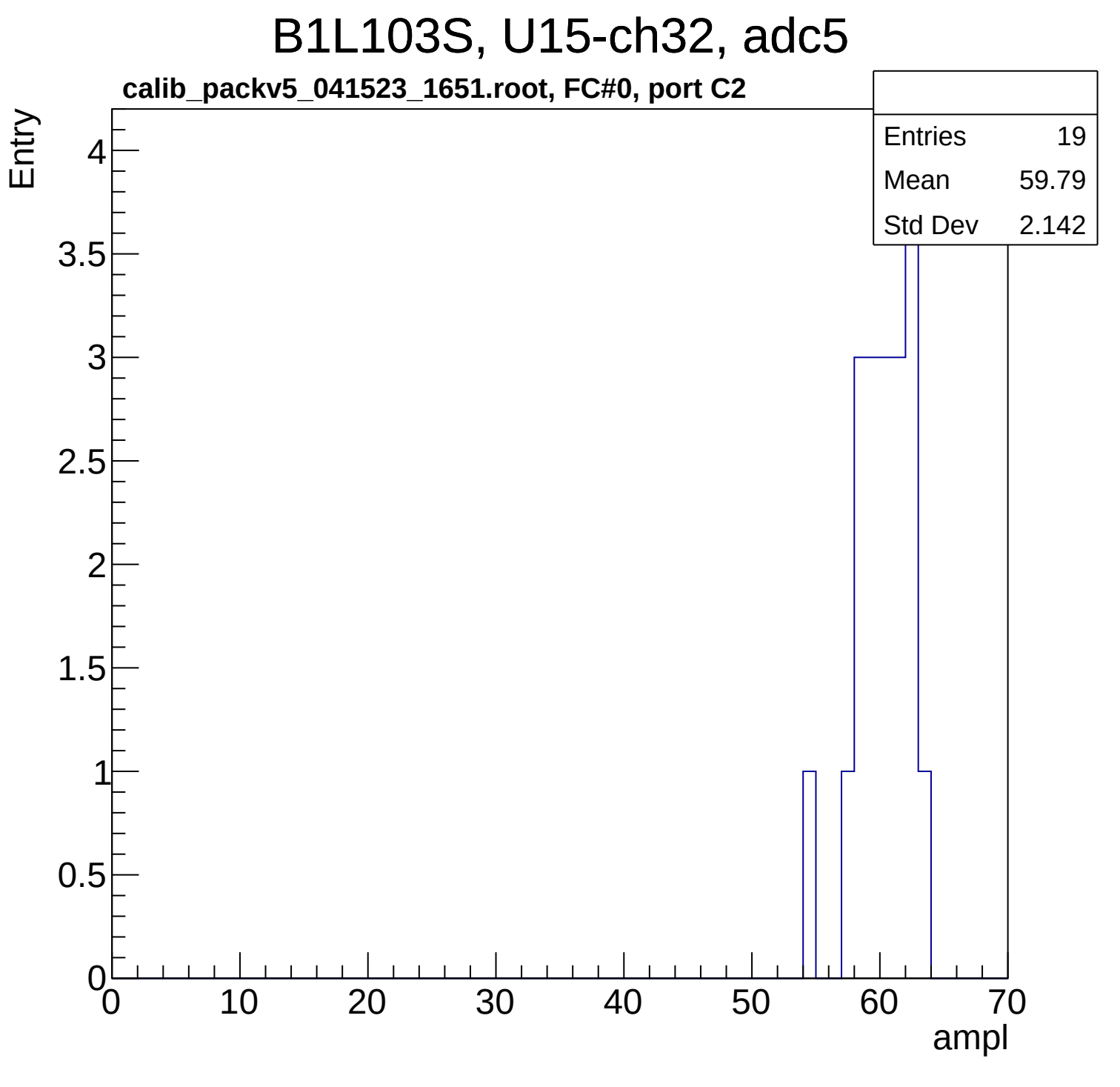

B1L103S, U15-ch32, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 26.35
Std Dev 9.058
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch32, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 36
Std Dev 3.293
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch32, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 38.41
Std Dev 11.5
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch32, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 45.39
Std Dev 13.62
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch32, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 55.27
Std Dev 3.098
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch32, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 59.79
Std Dev 2.142
Entry
ampl
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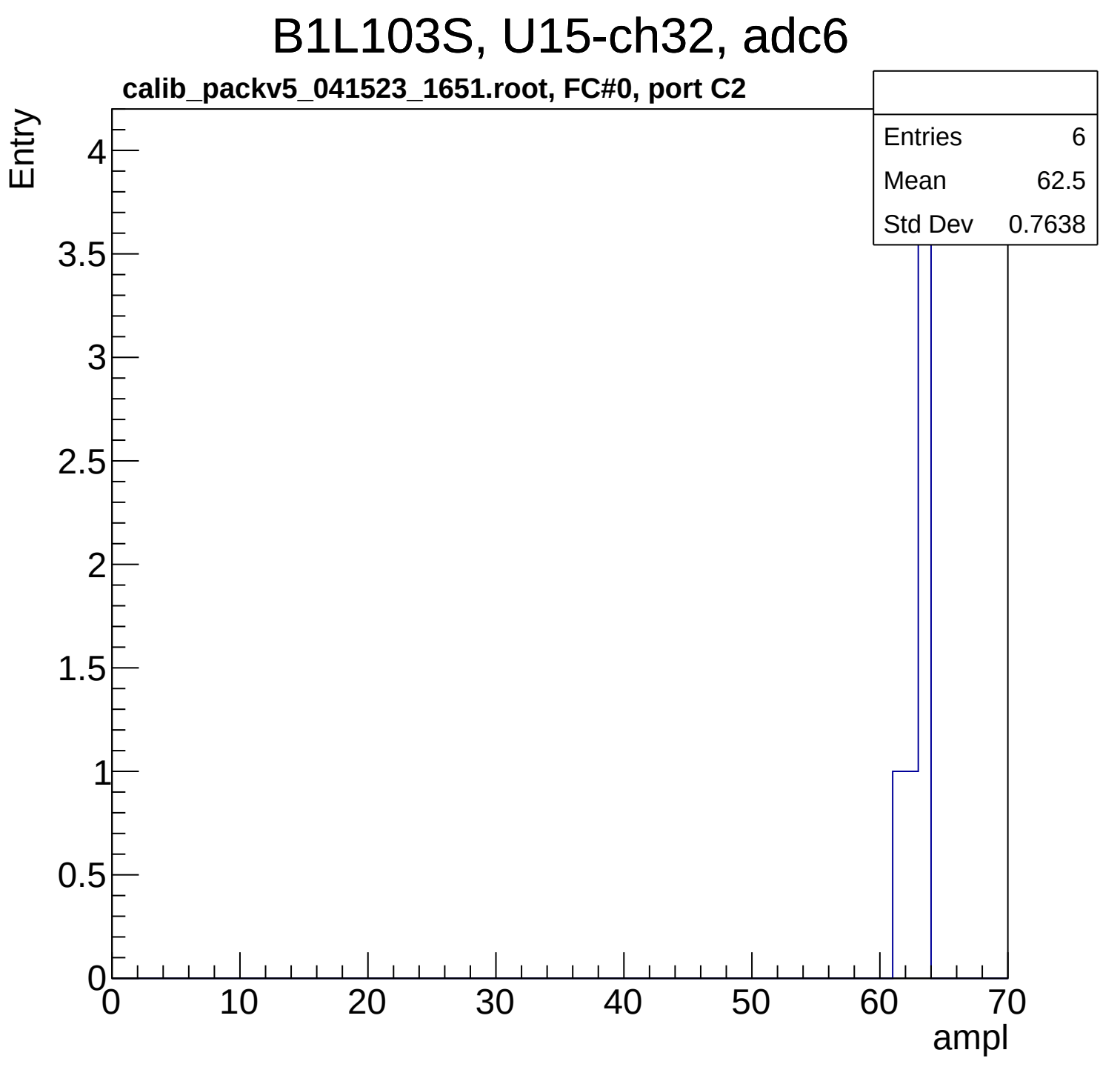
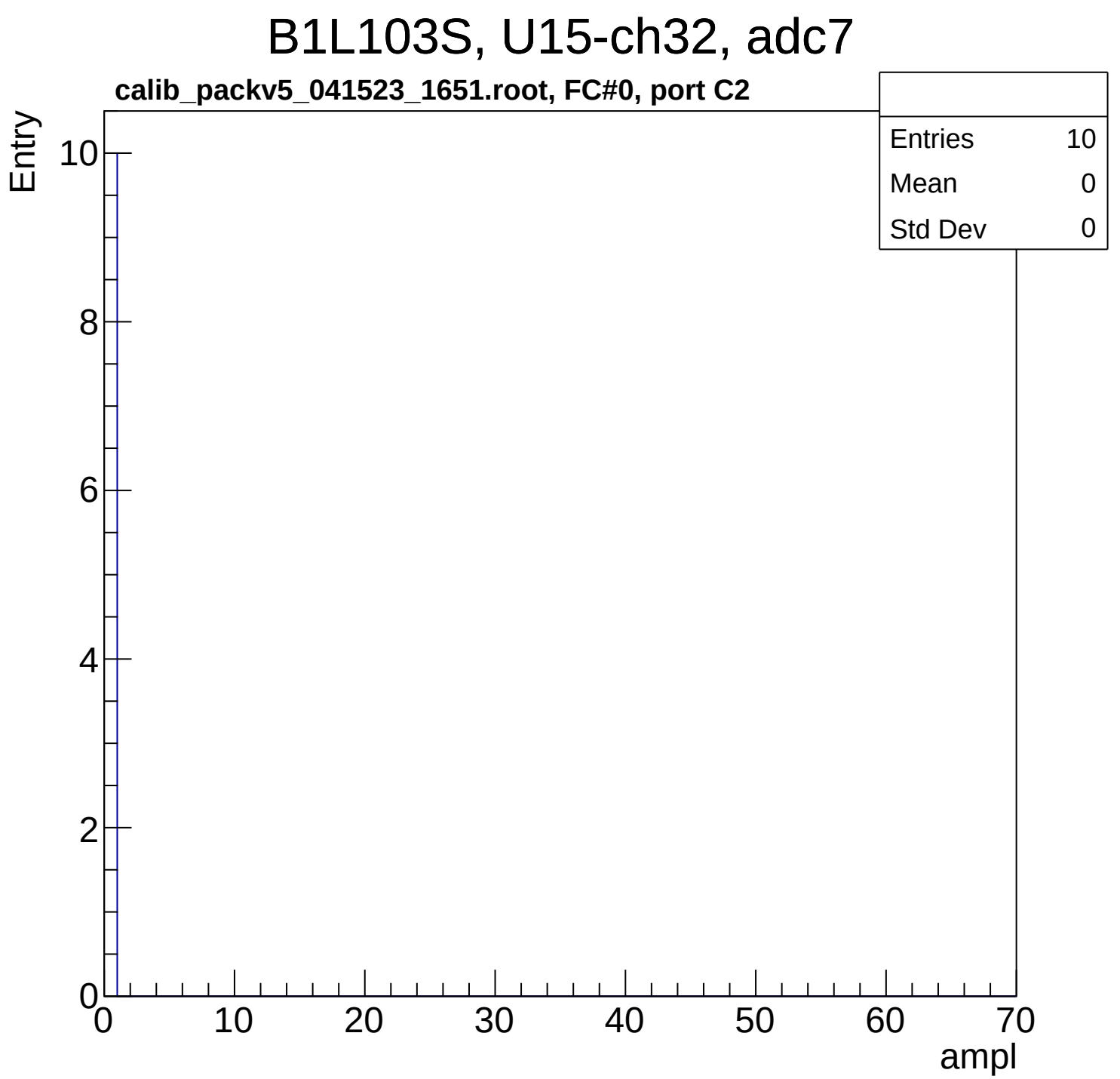
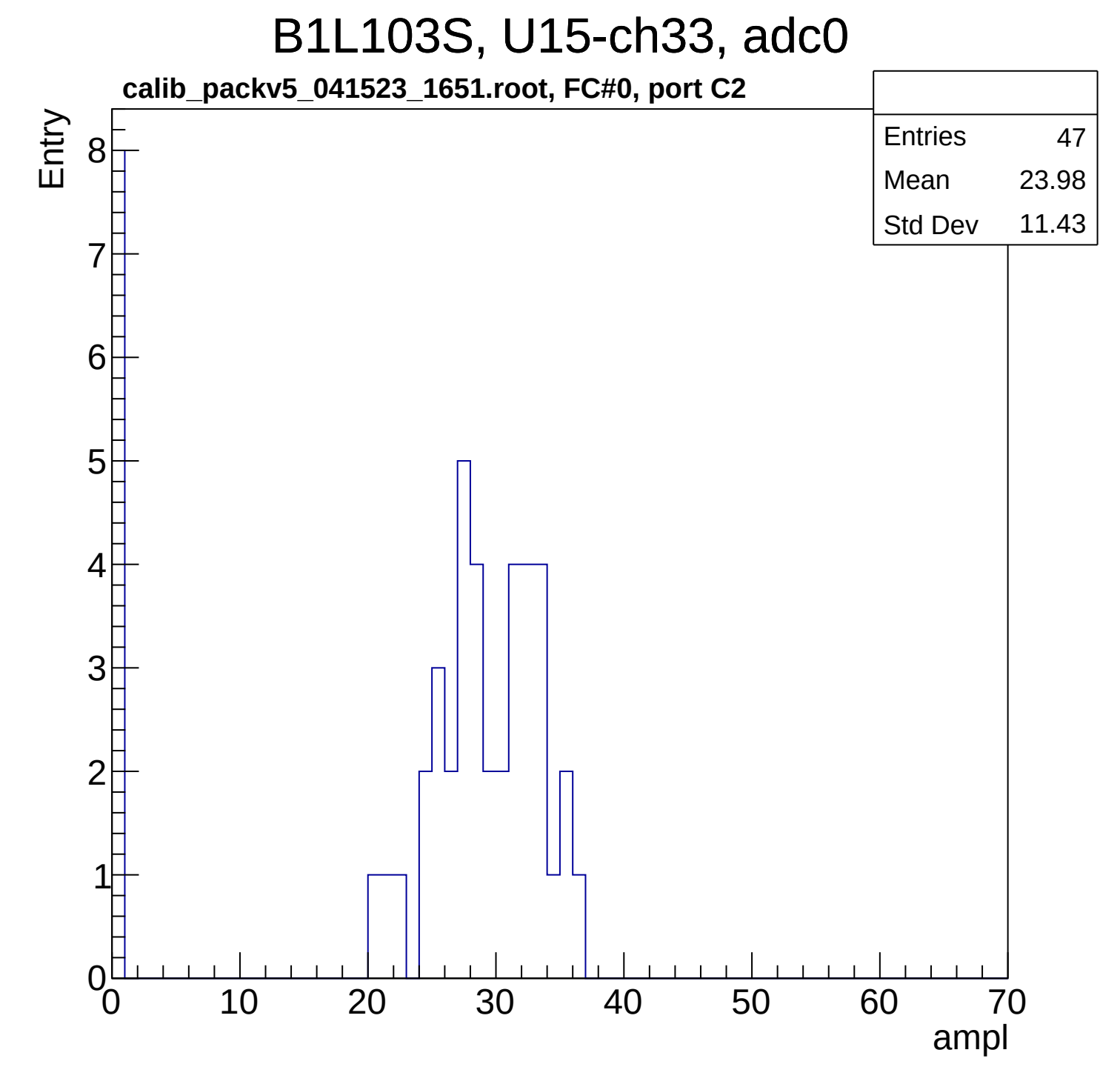
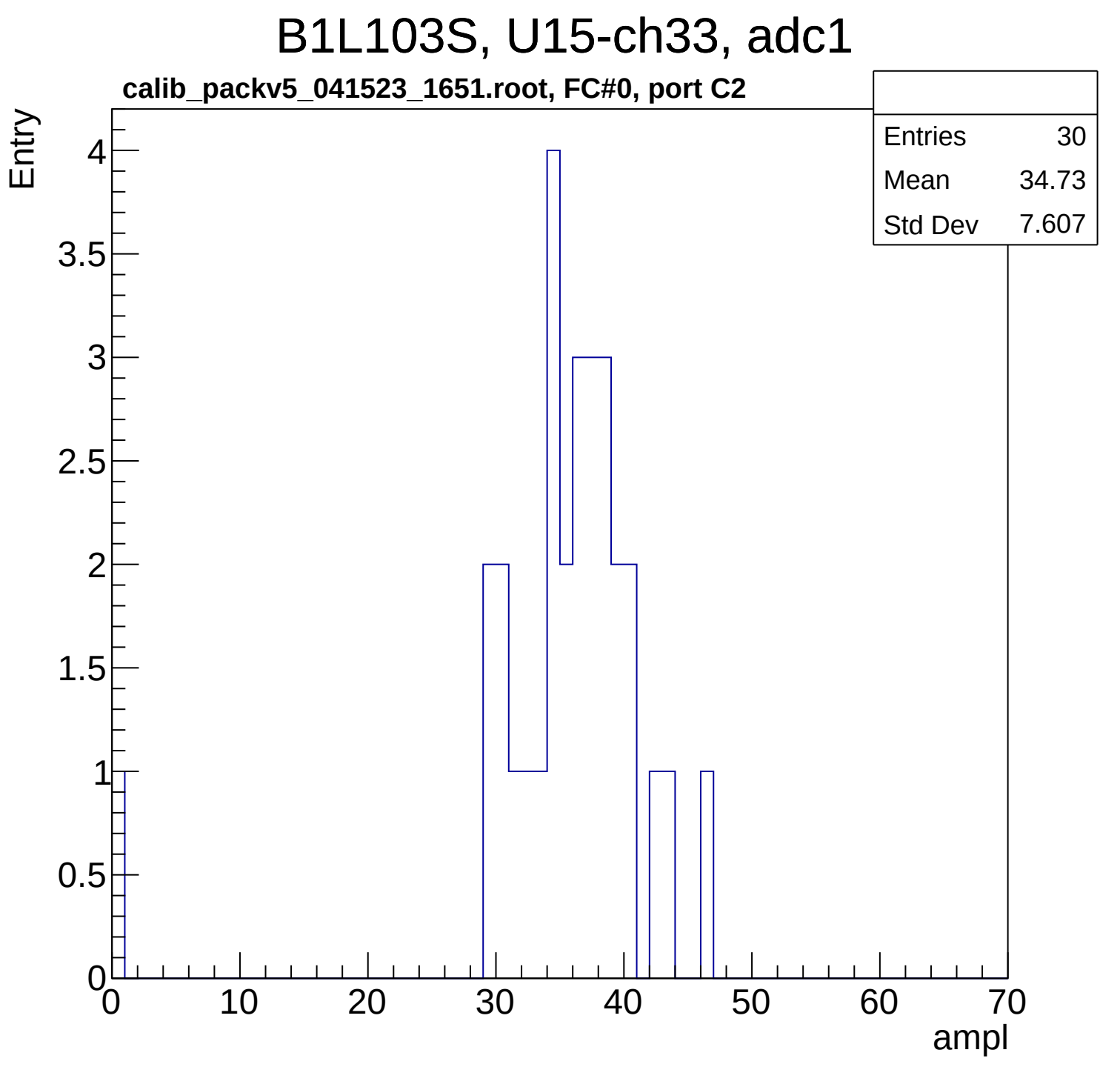
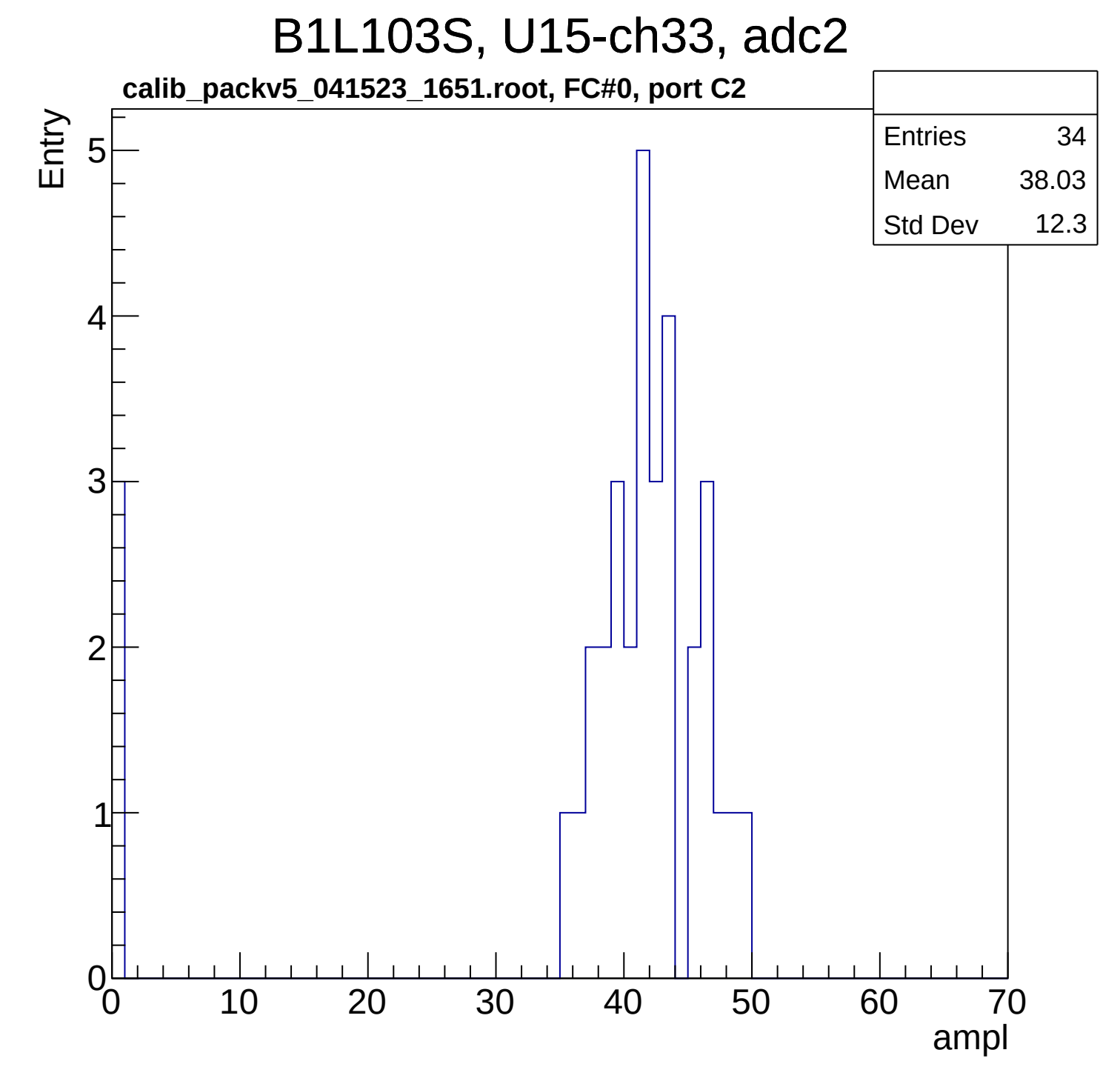
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

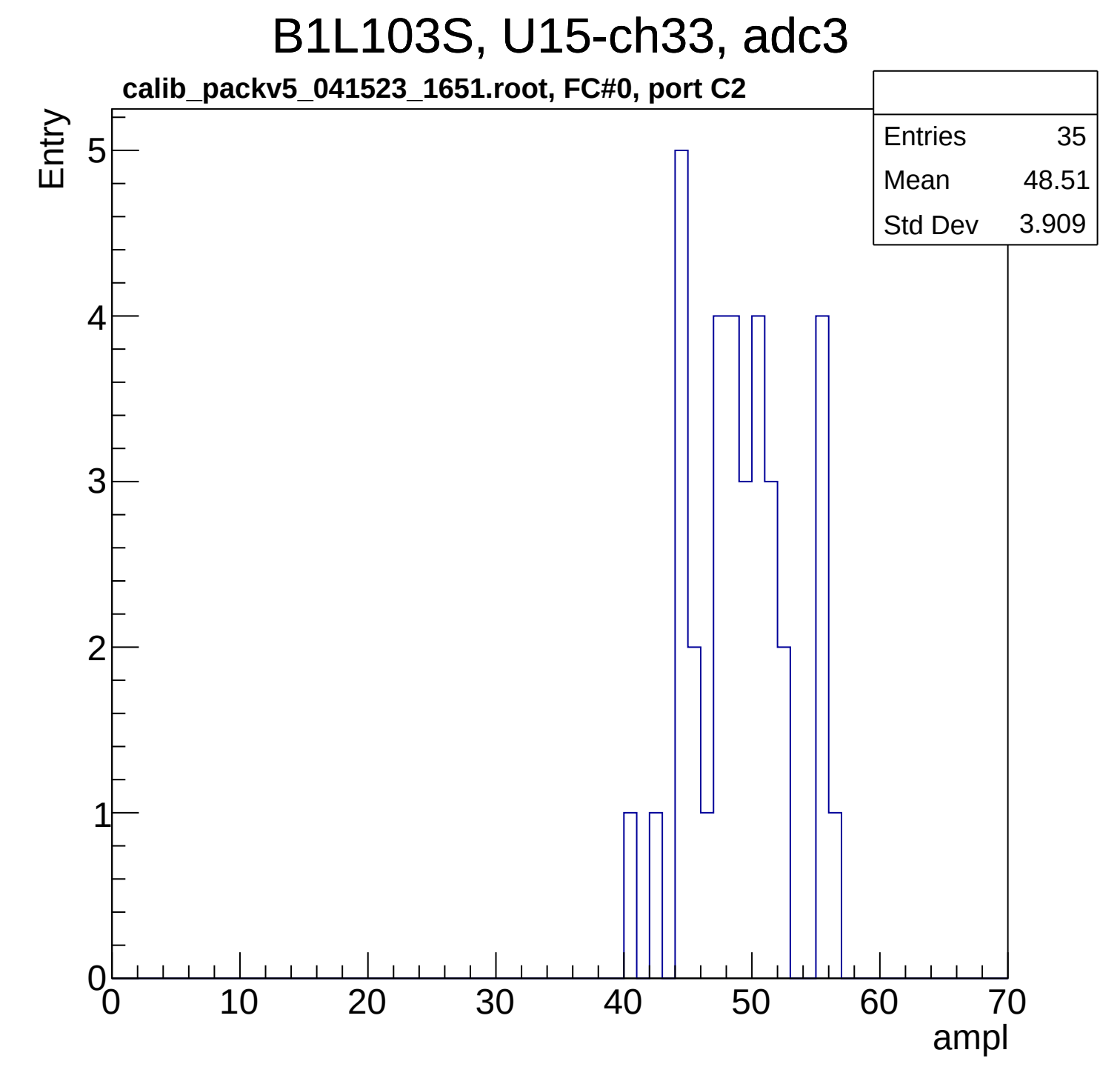

B1L103S, U15-ch32, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.5
Std Dev 0.7638
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

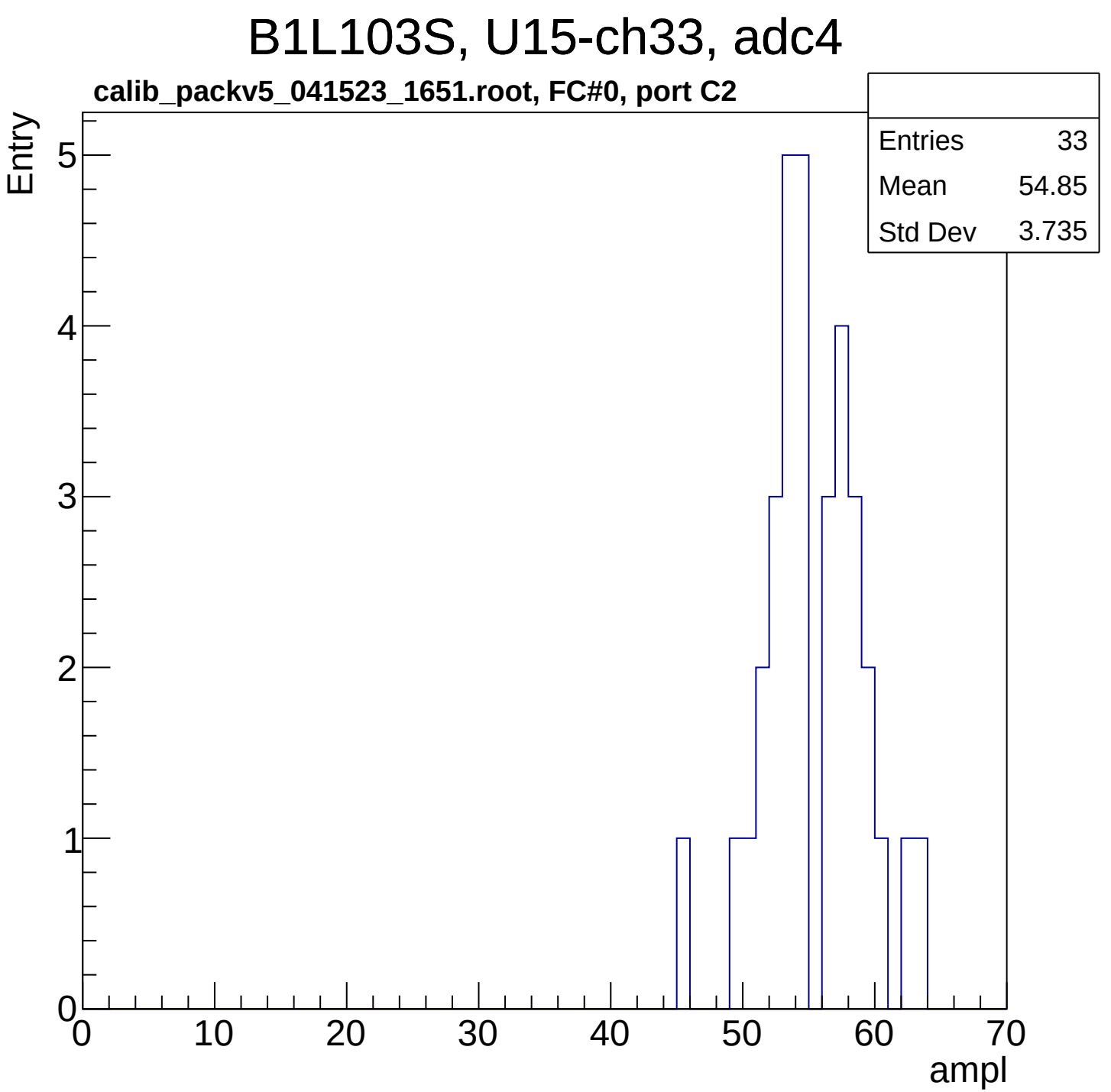

B1L103S, U15-ch32, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

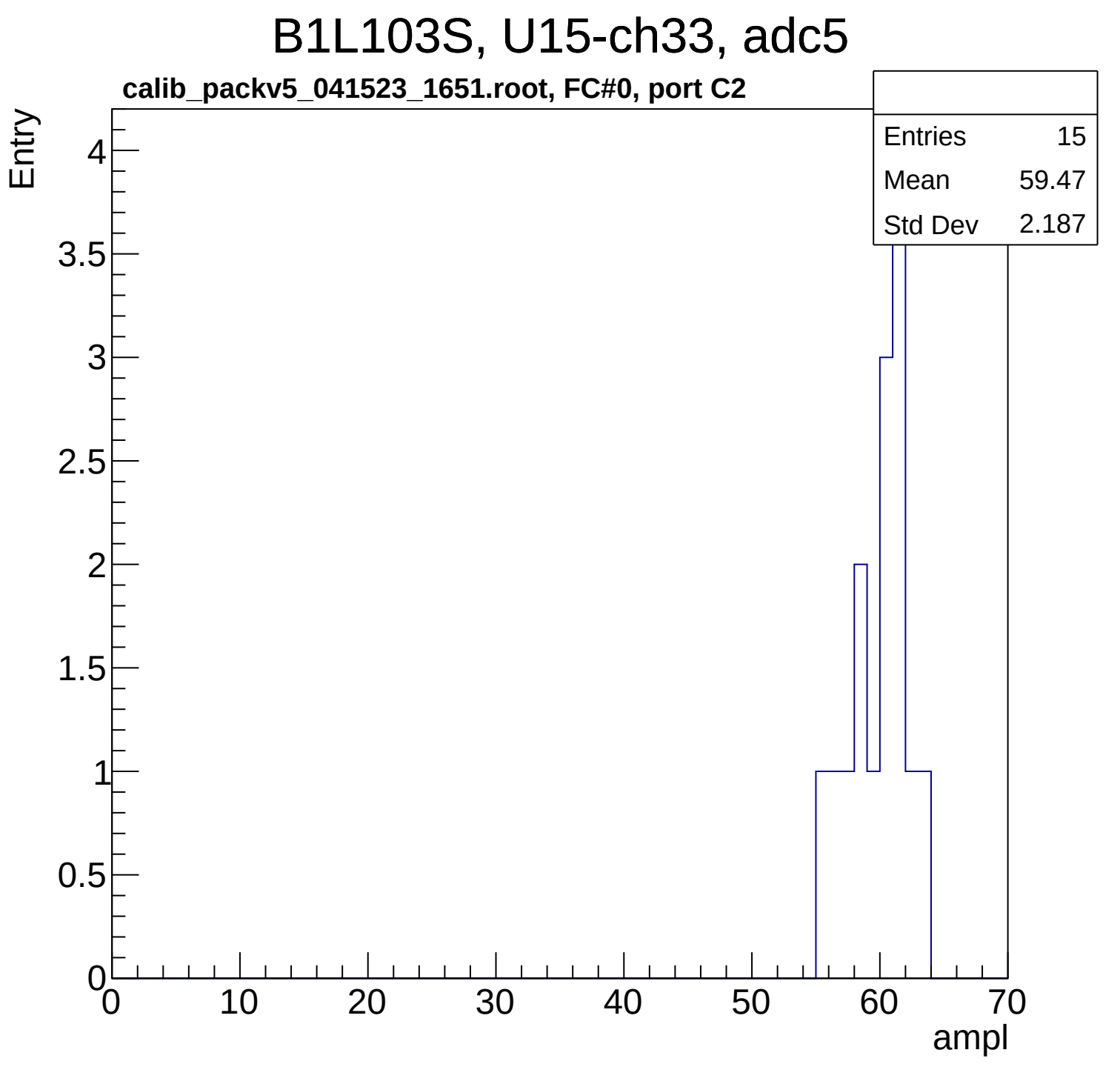

B1L103S, U15-ch33, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 23.98
Std Dev 11.43
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

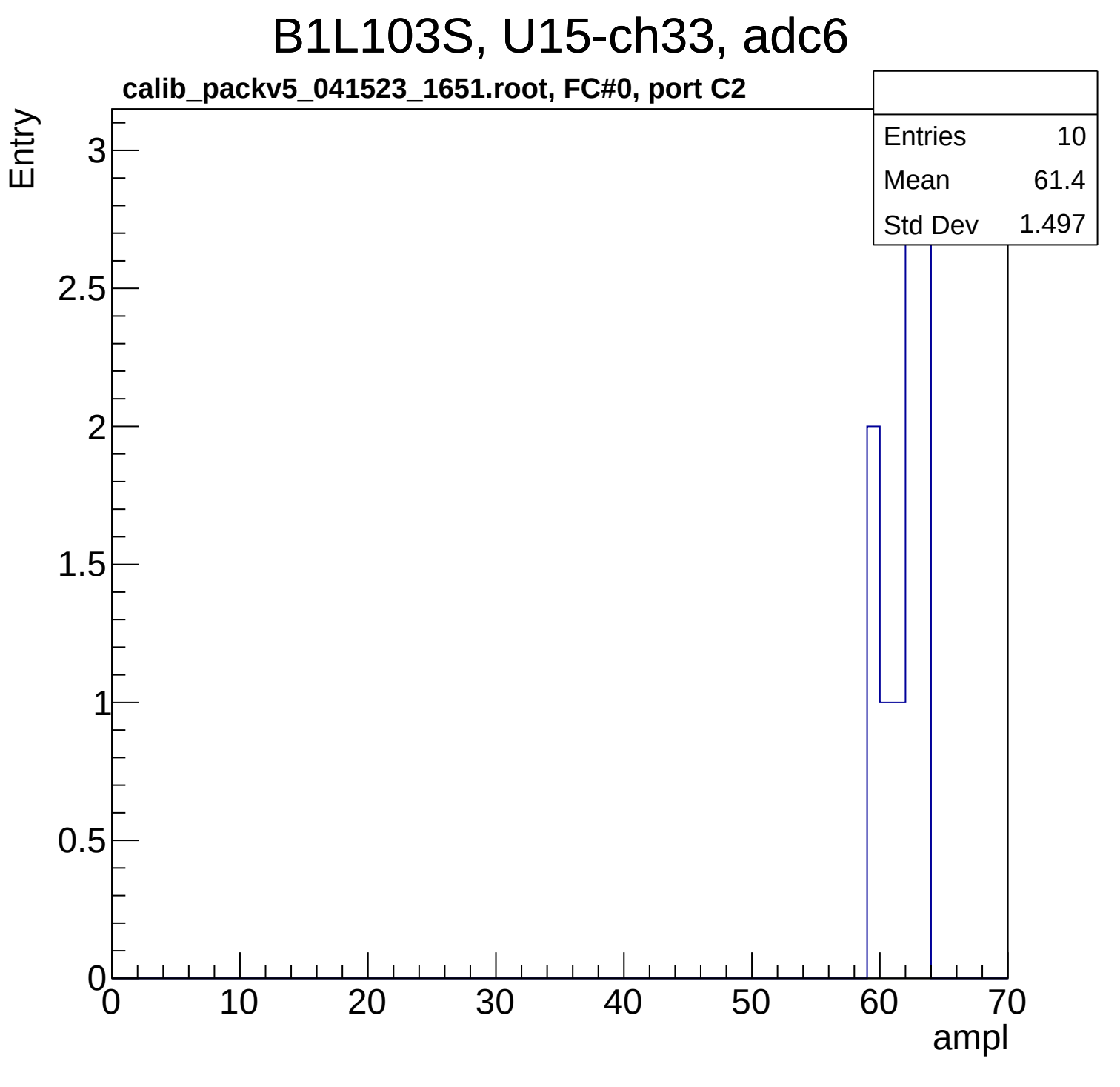

B1L103S, U15-ch33, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 34.73
Std Dev 7.607
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch33, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 38.03
Std Dev 12.3
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch33, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 48.51
Std Dev 3.909
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch33, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 54.85
Std Dev 3.735
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch33, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 59.47
Std Dev 2.187
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch33, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.4
Std Dev 1.497
Entry
ampl
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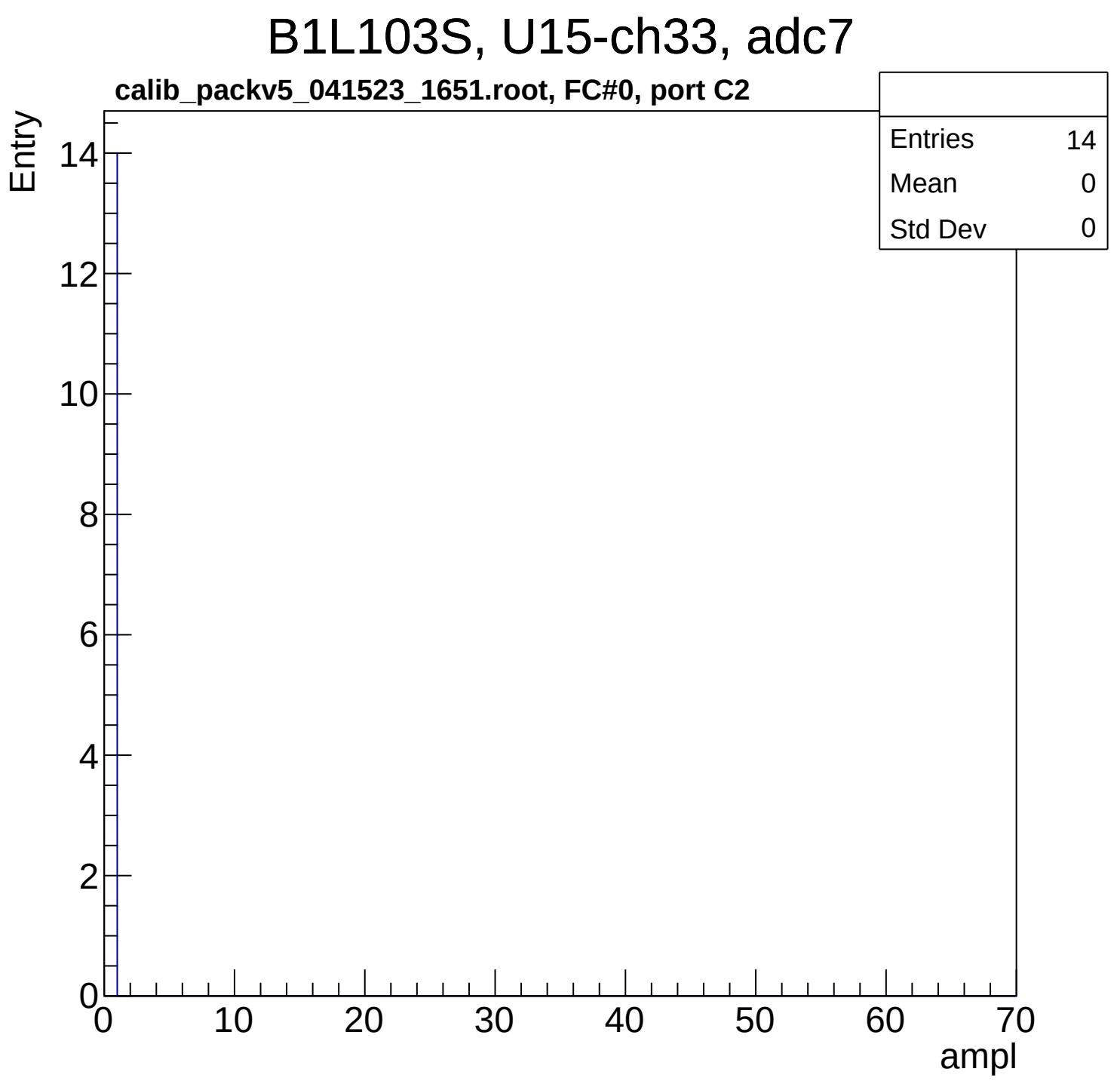
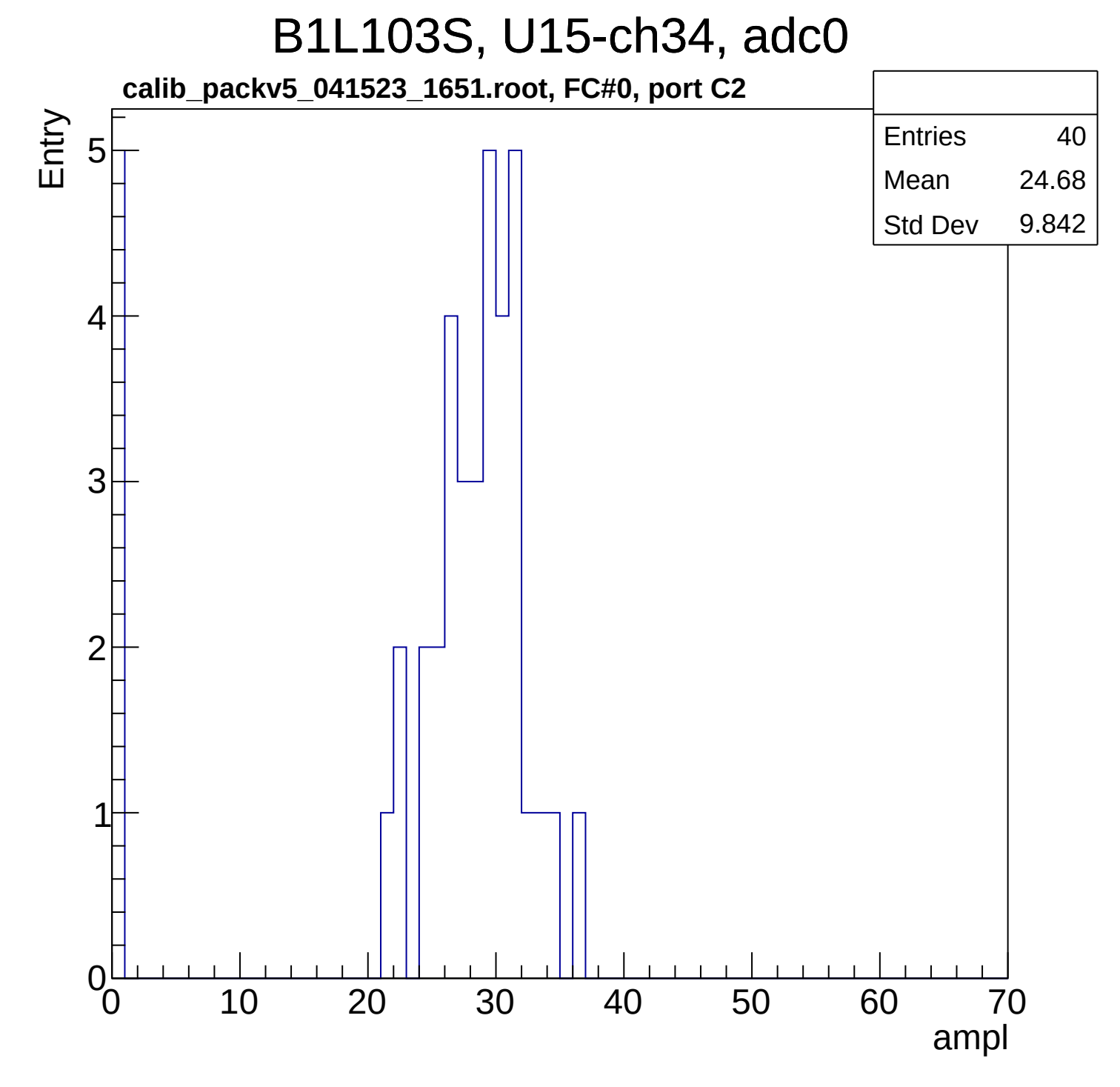
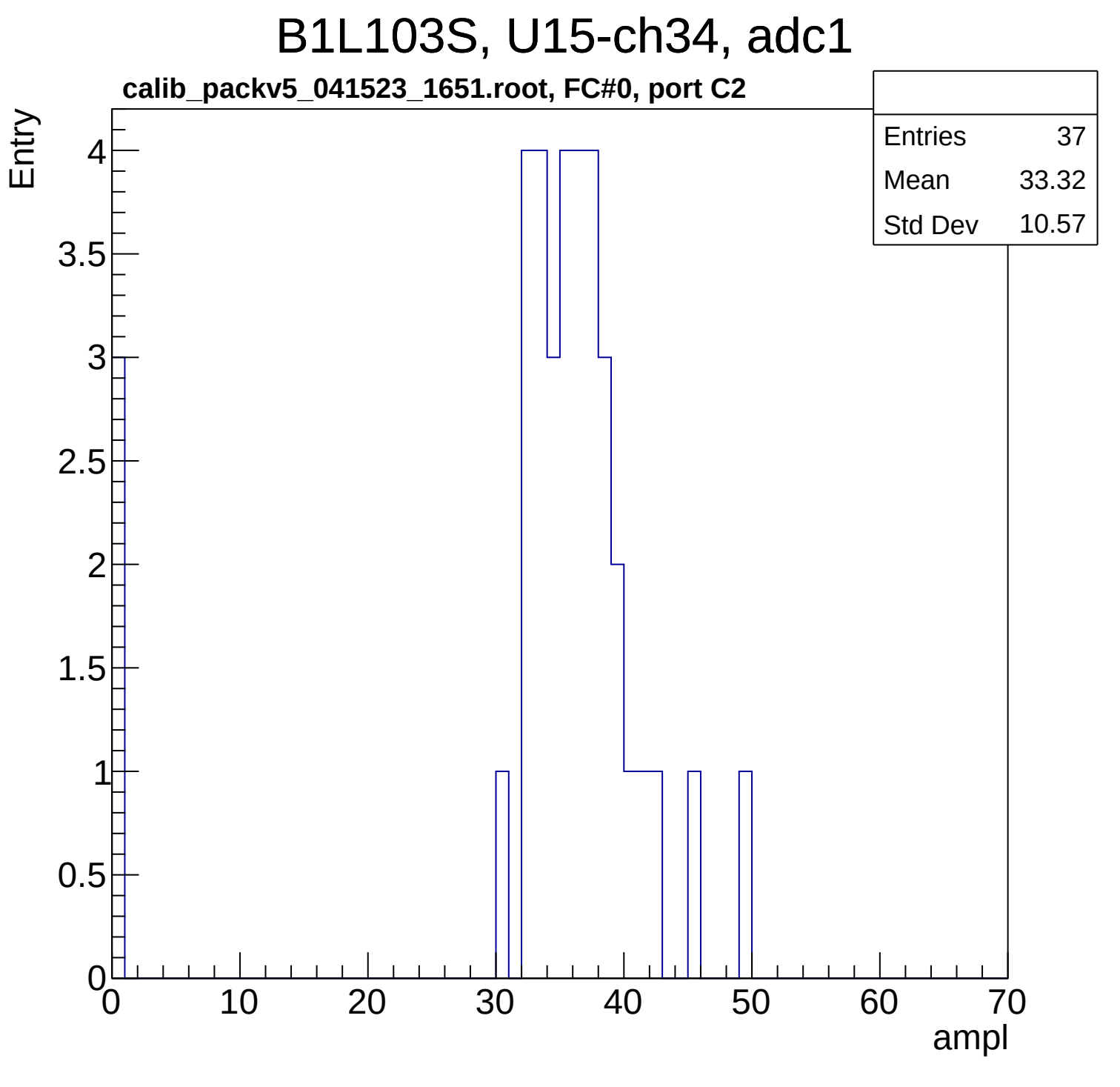
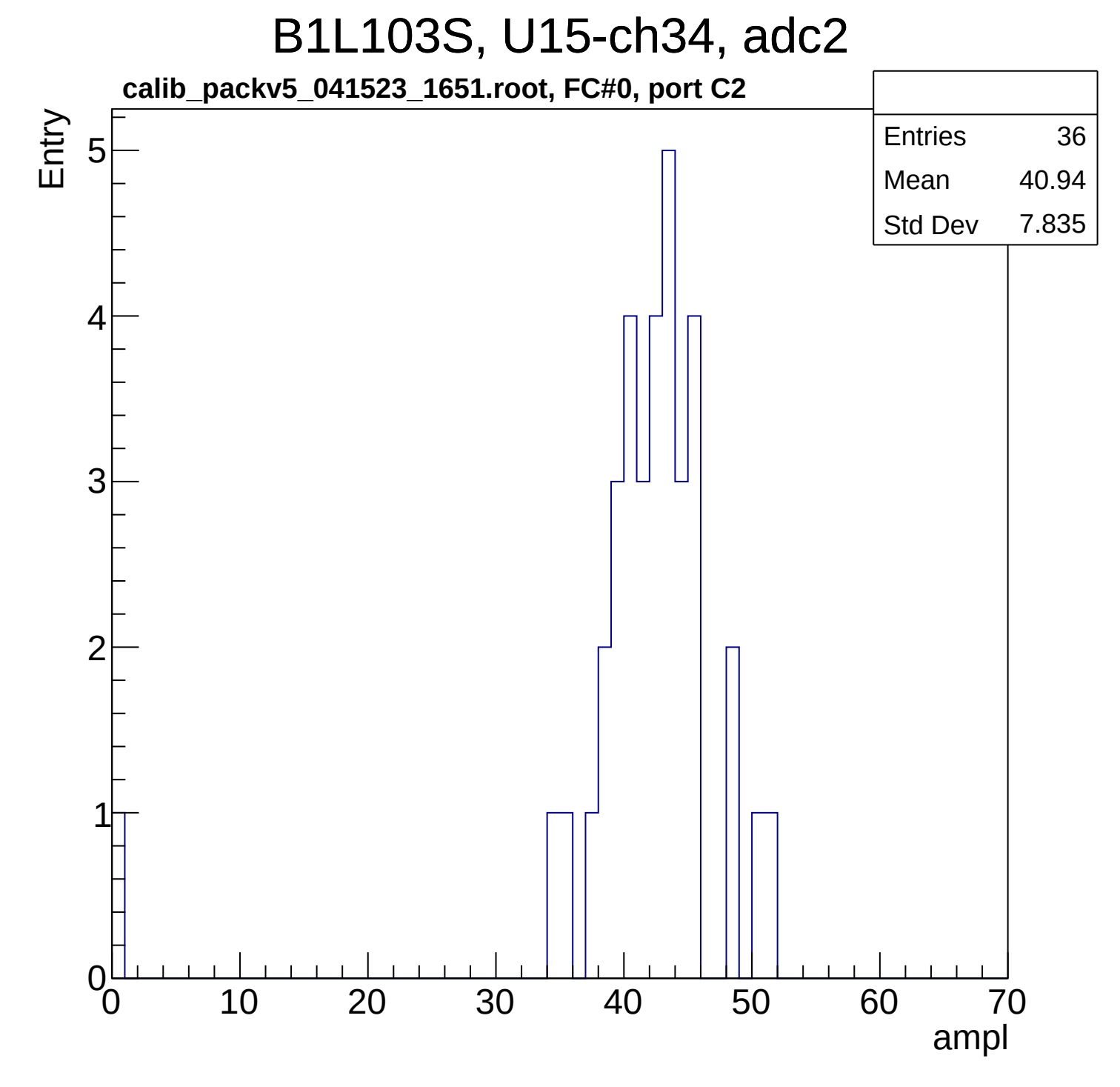
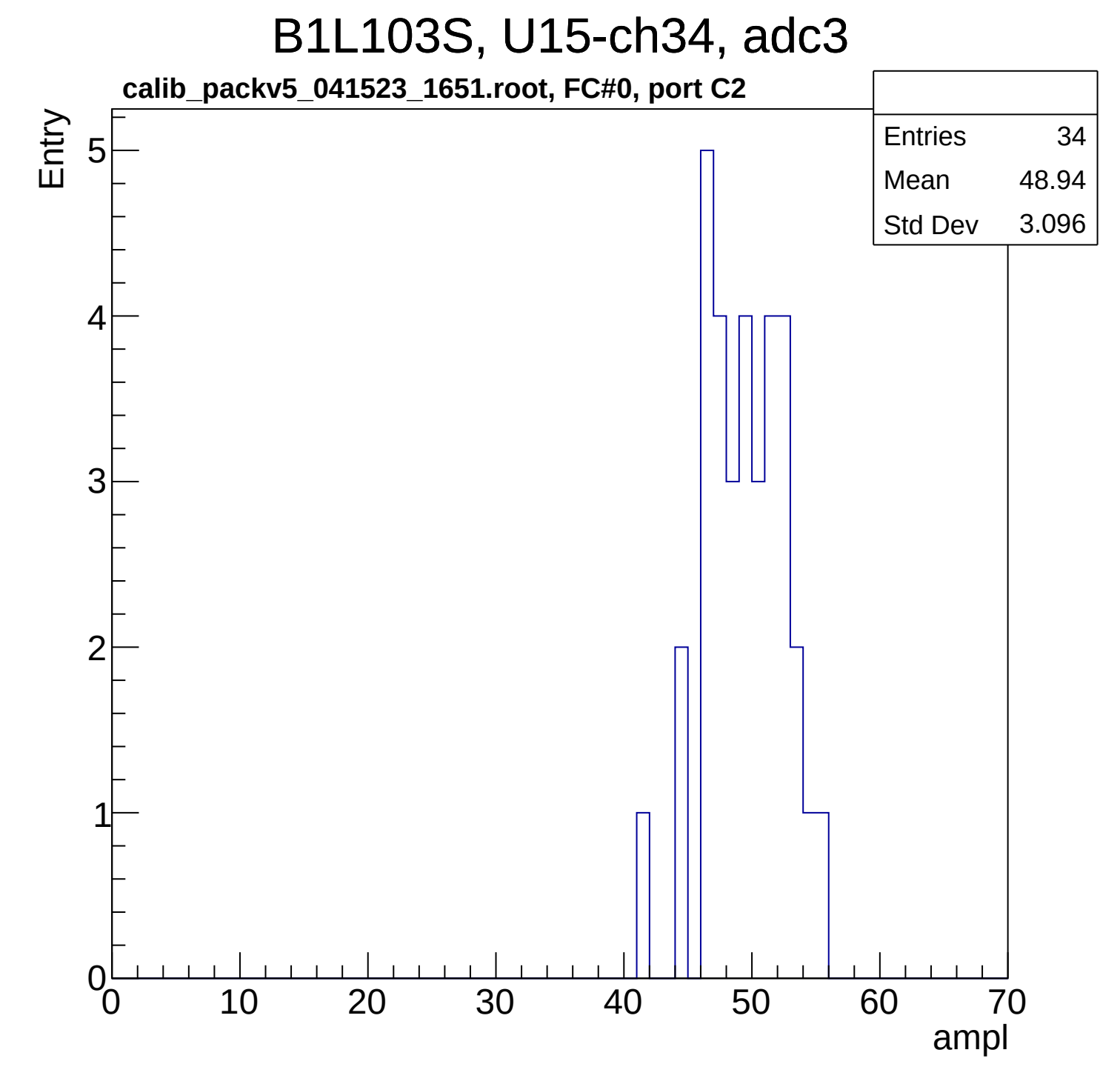
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

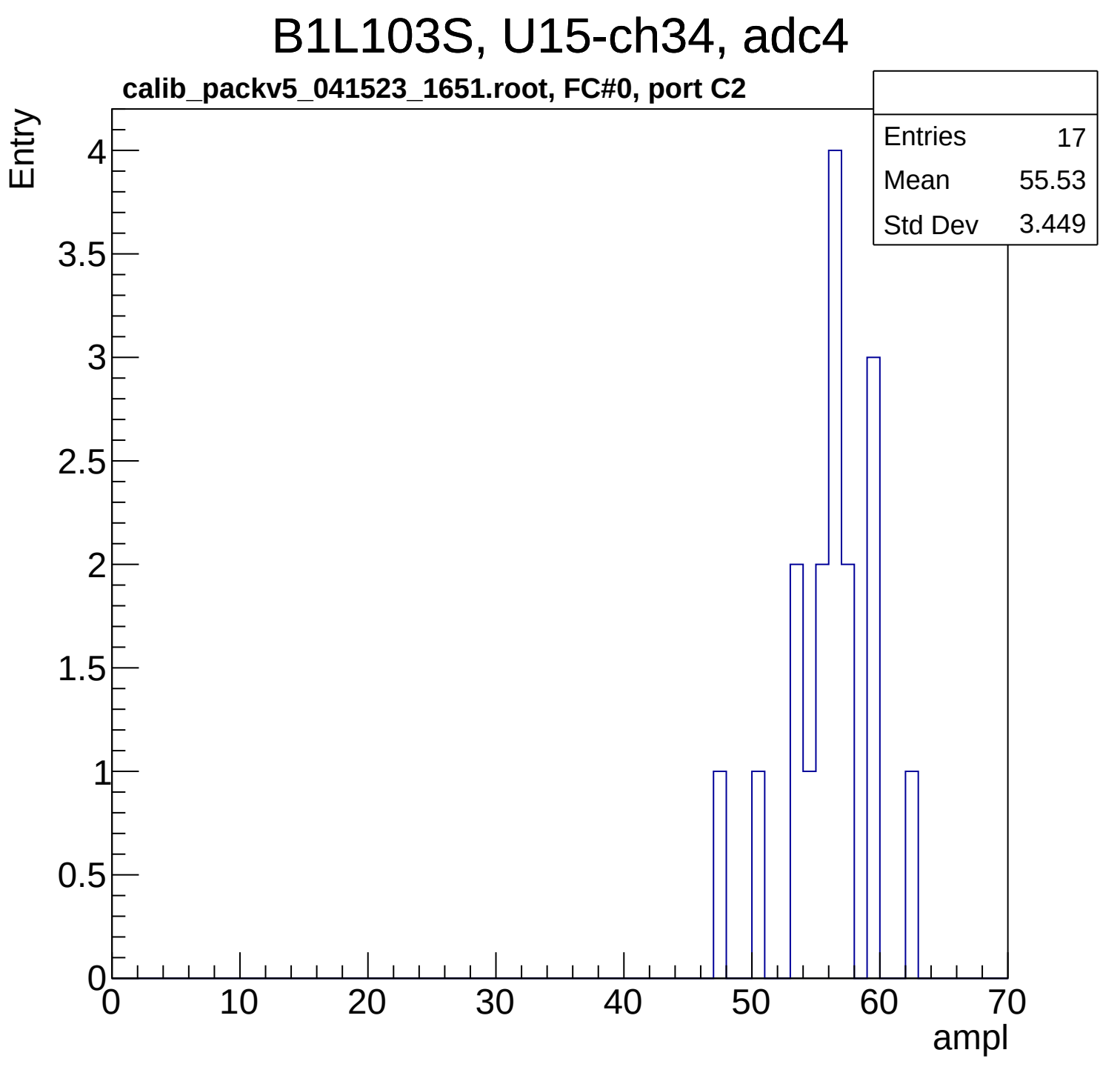

B1L103S, U15-ch33, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

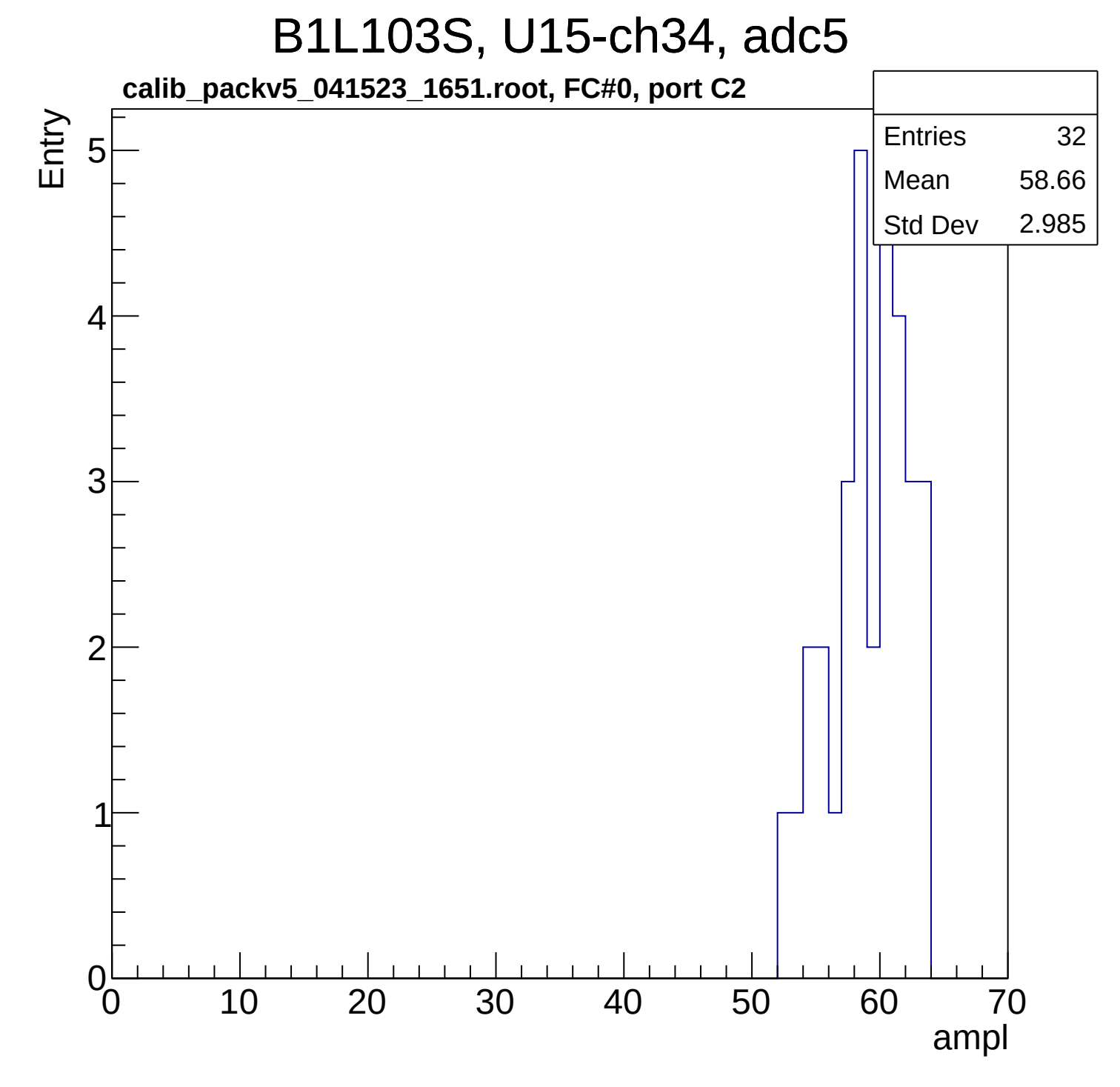

B1L103S, U15-ch34, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 24.68
Std Dev 9.842
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

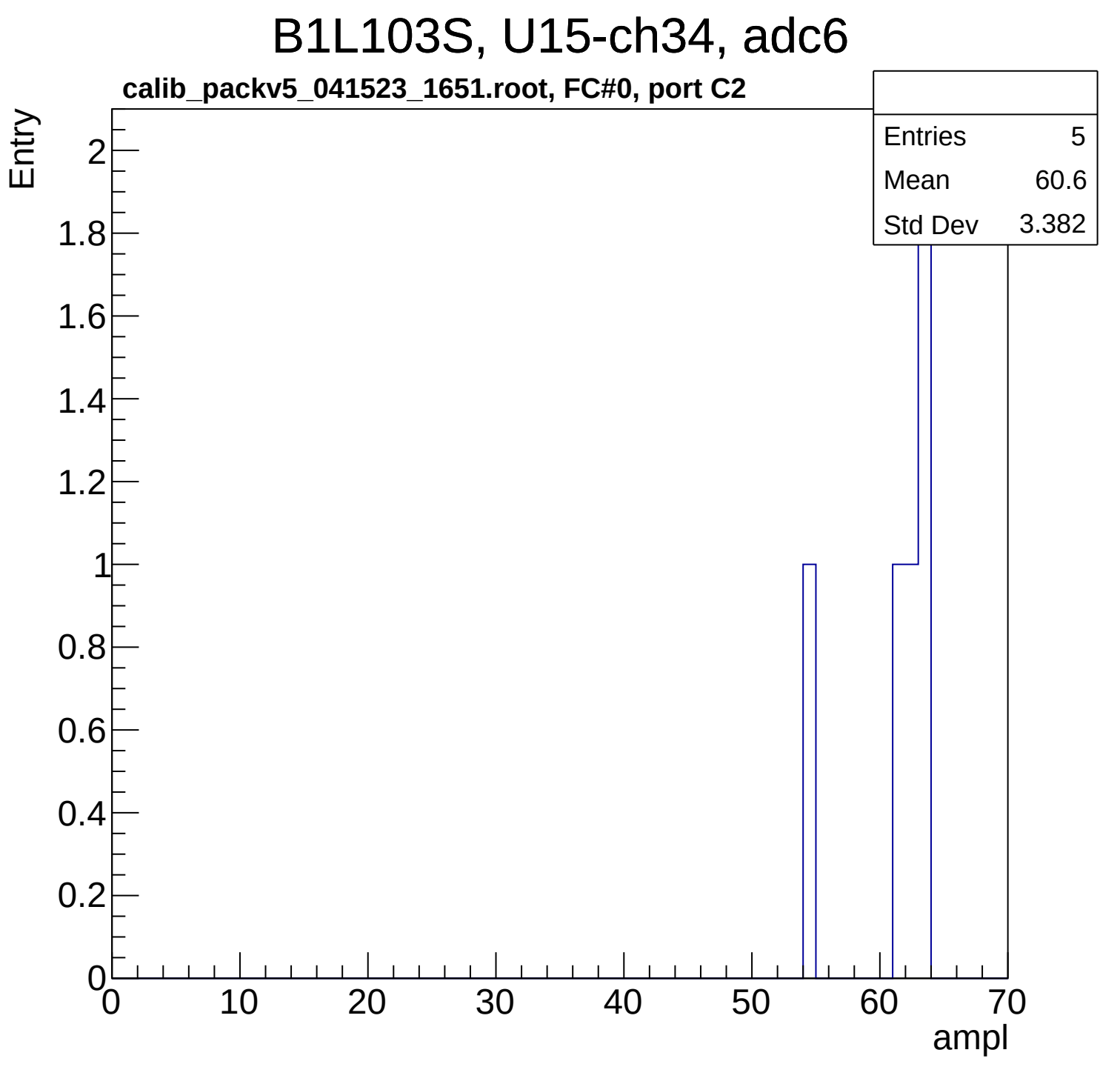

B1L103S, U15-ch34, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 33.32
Std Dev 10.57
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

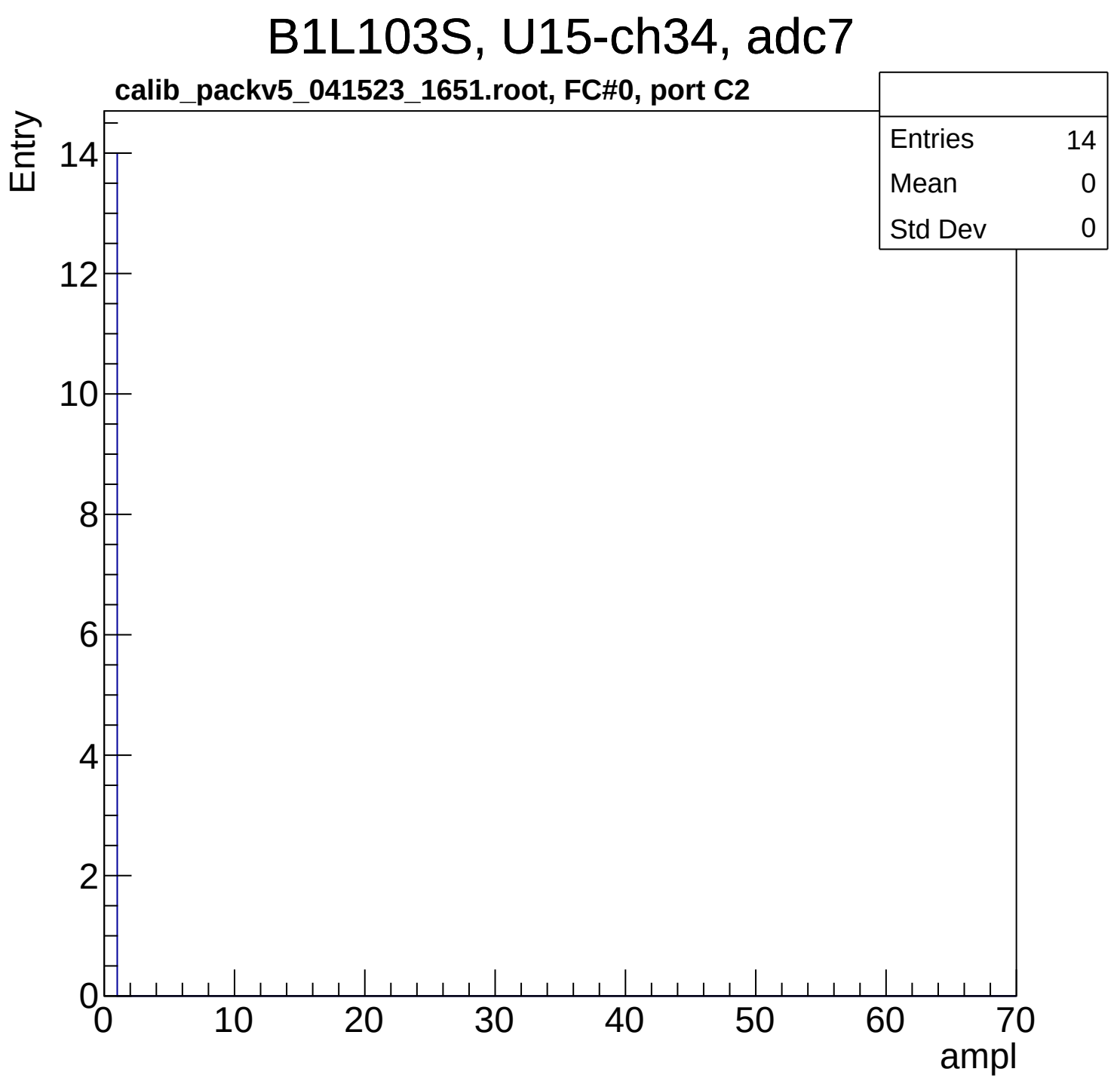

B1L103S, U15-ch34, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 40.94
Std Dev 7.835
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

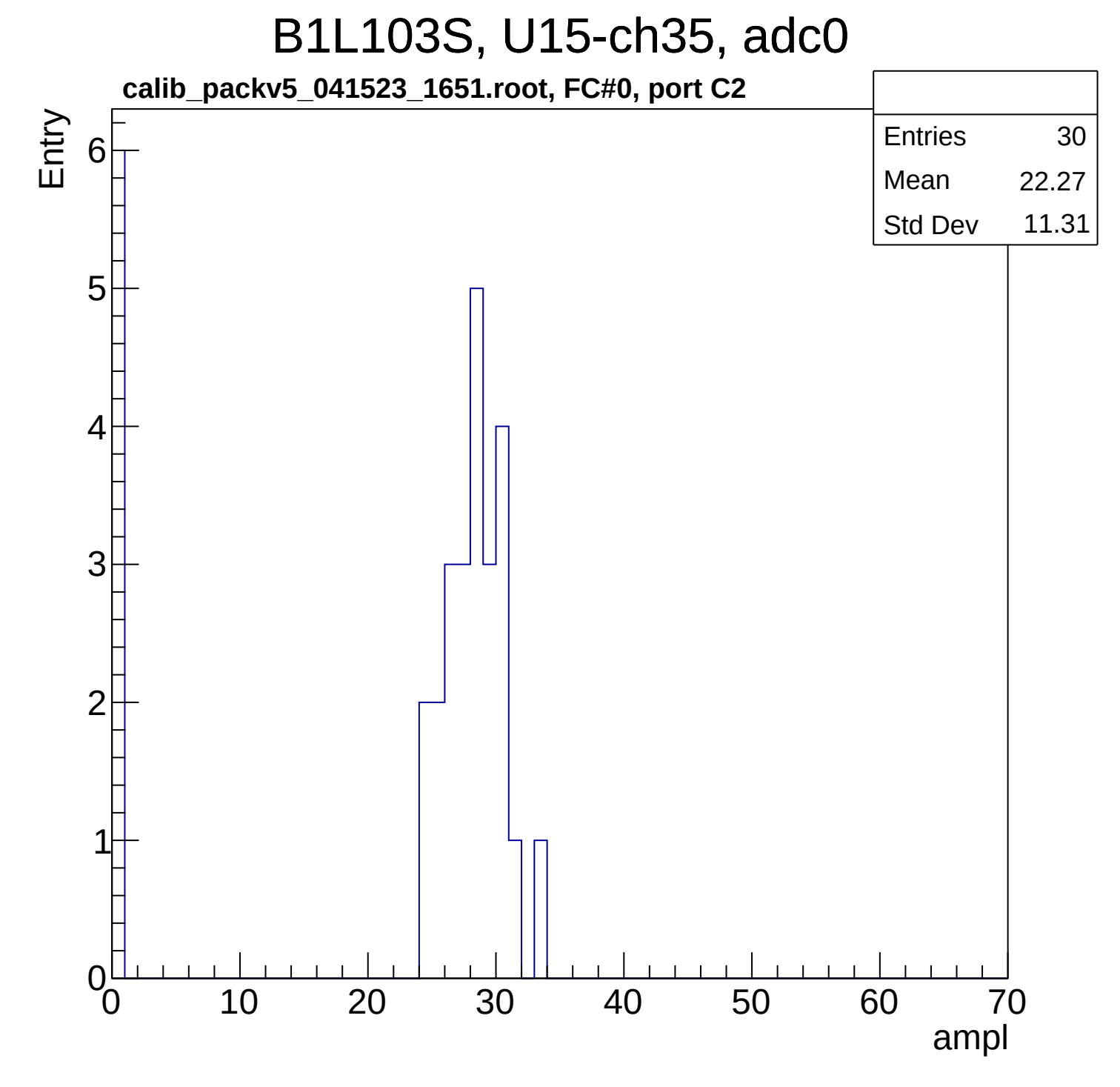

B1L103S, U15-ch34, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 48.94
Std Dev 3.096
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

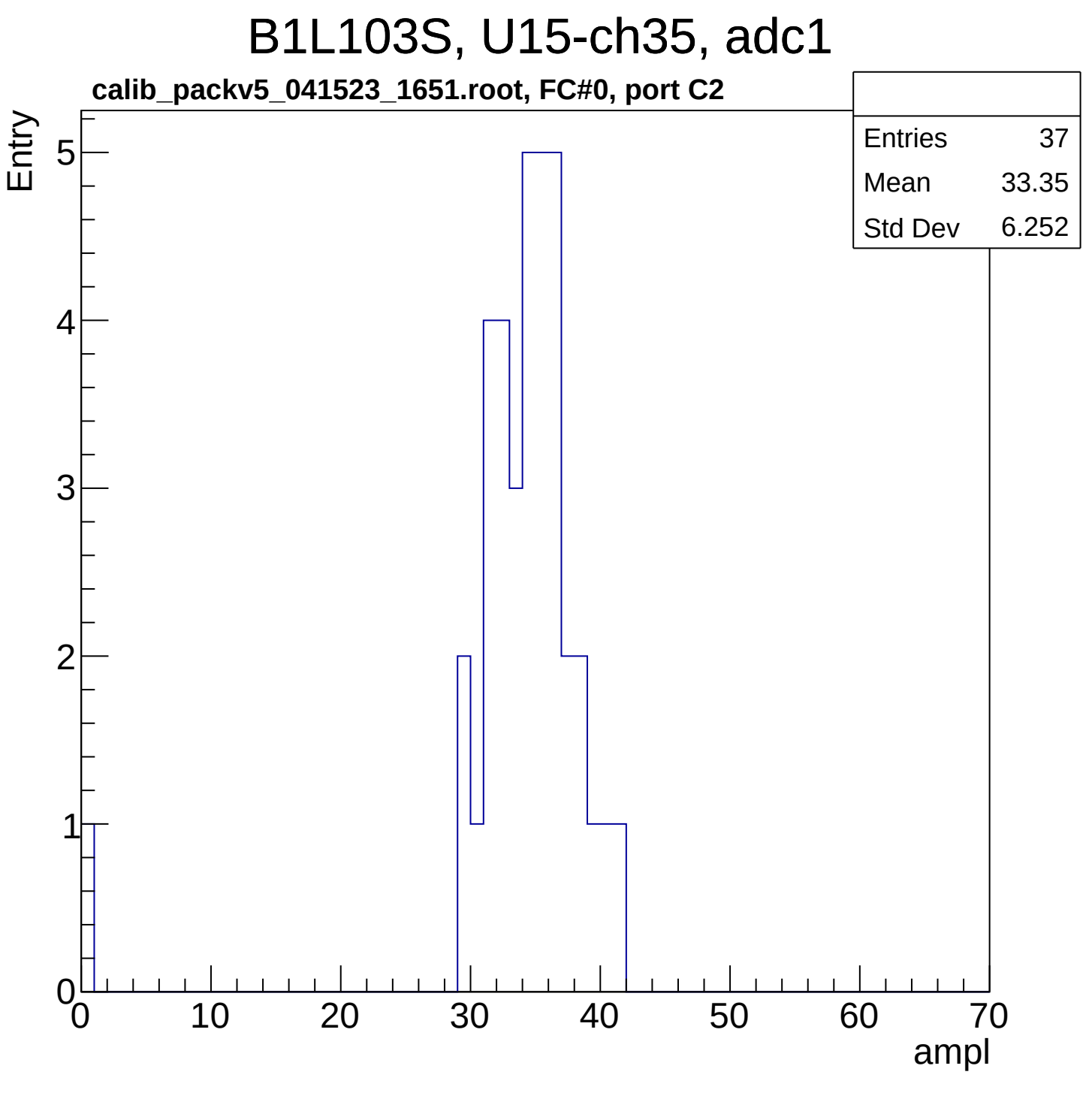

B1L103S, U15-ch34, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 55.53
Std Dev 3.449
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

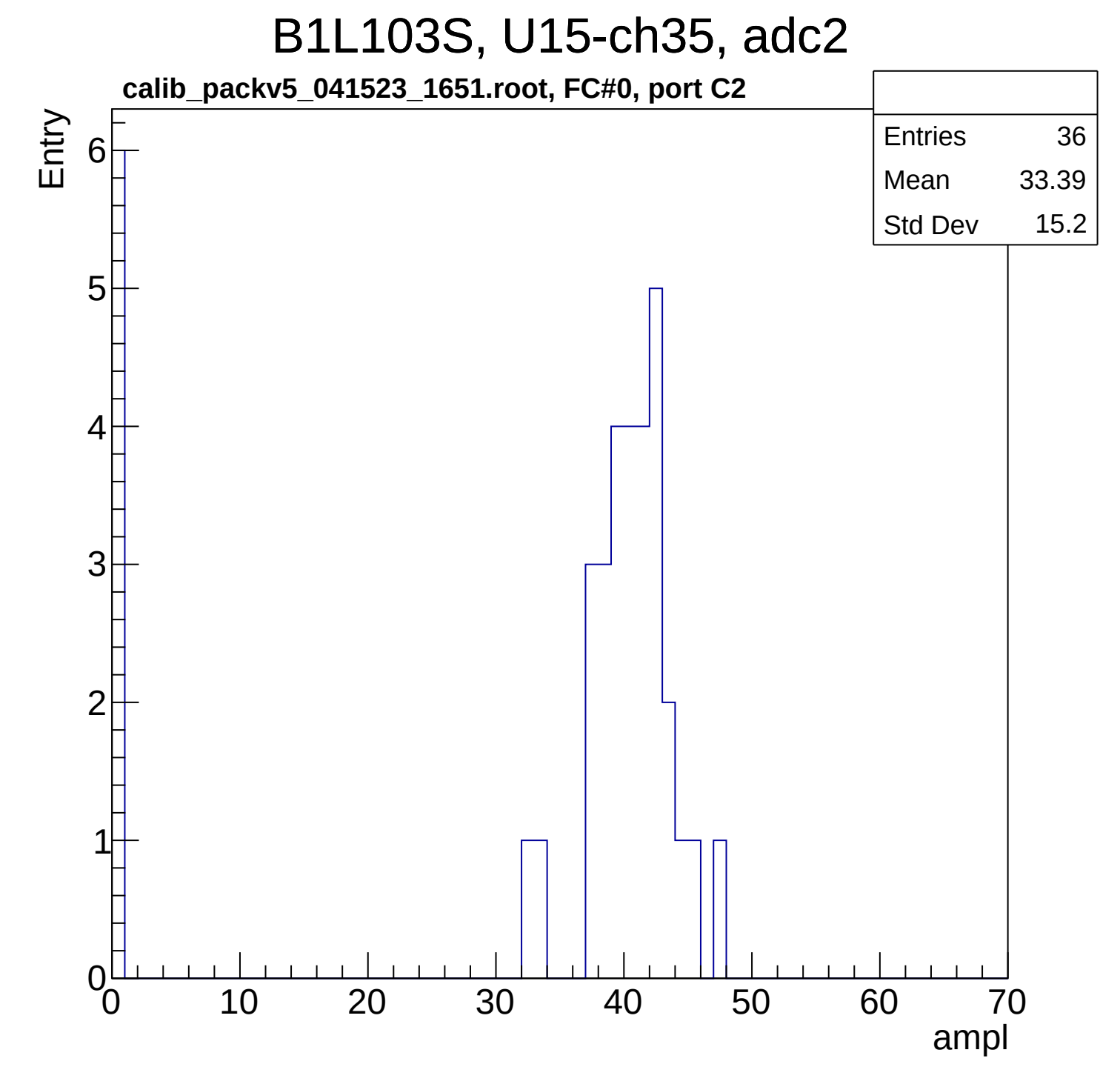

B1L103S, U15-ch34, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 58.66
Std Dev 2.985
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

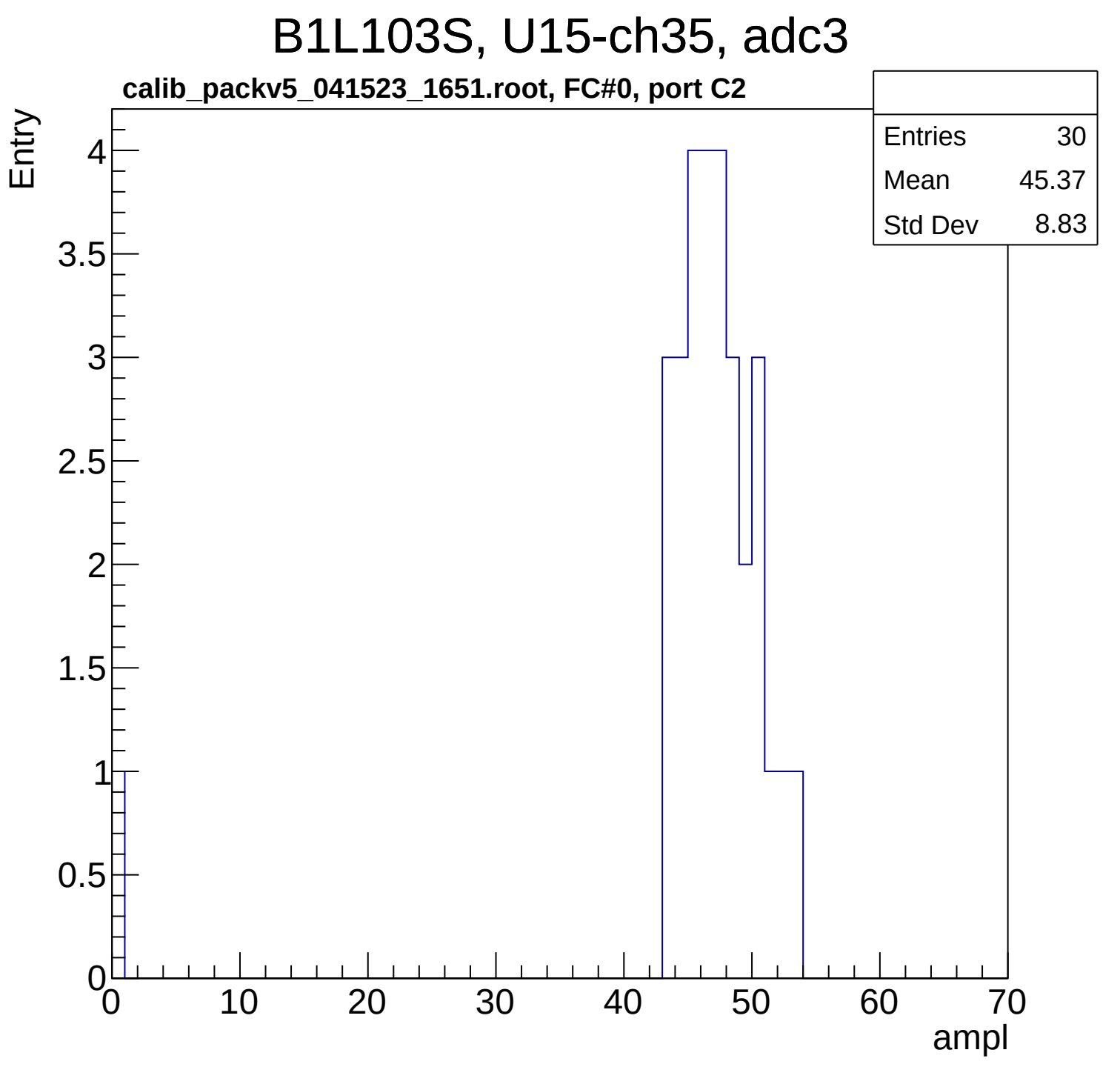

B1L103S, U15-ch34, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 60.6
Std Dev 3.382
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

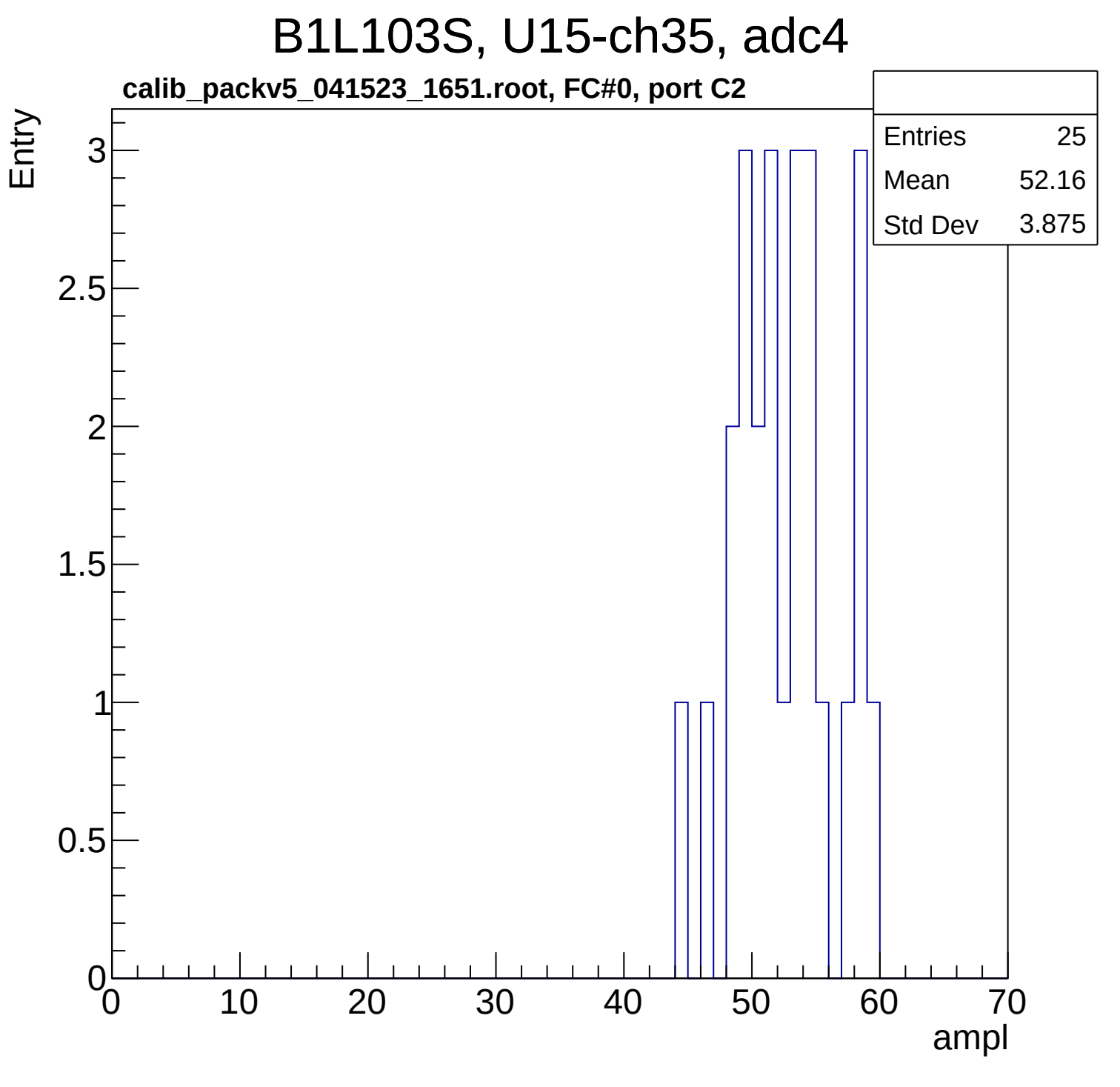

B1L103S, U15-ch34, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

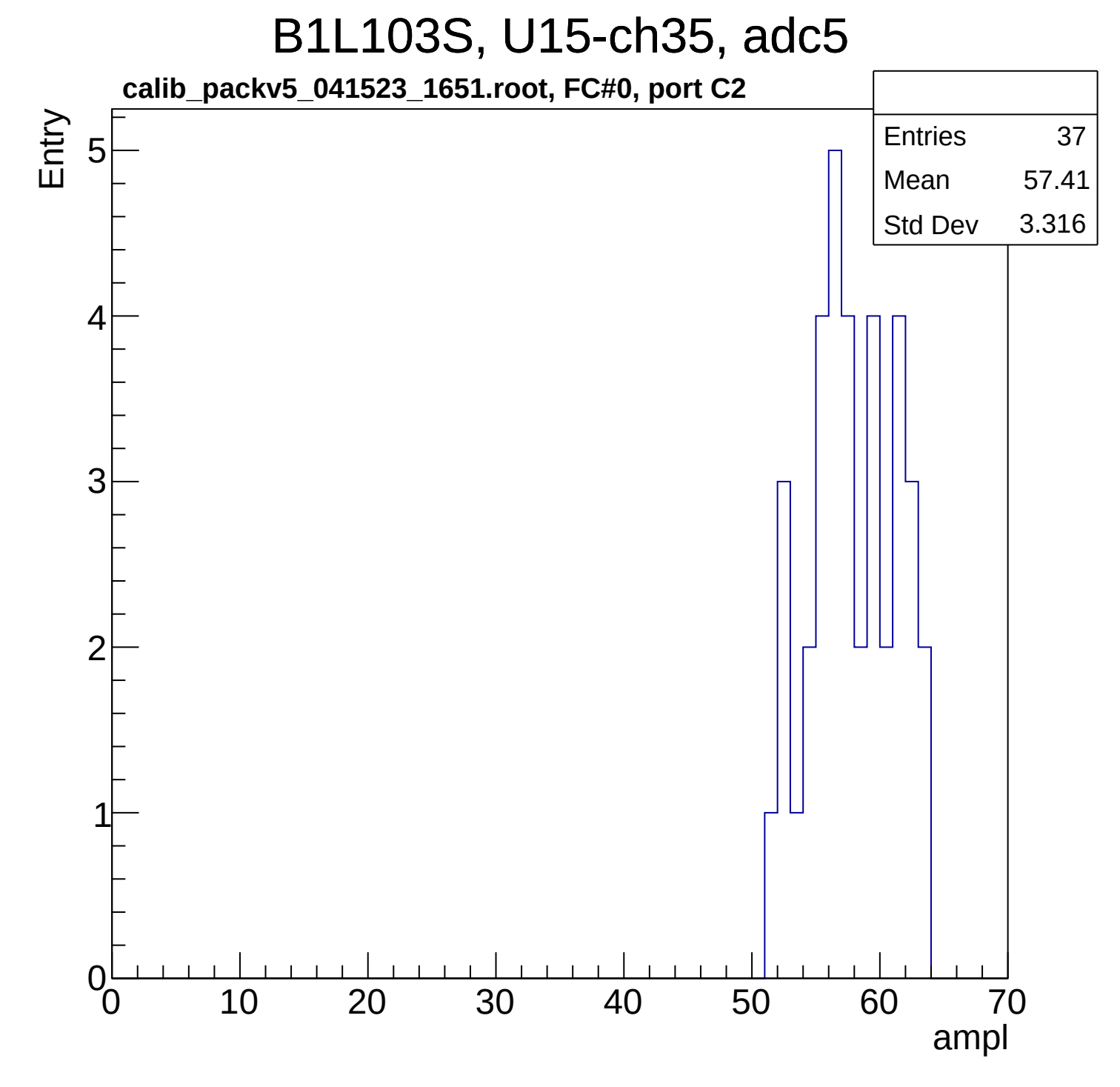

B1L103S, U15-ch35, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 22.27
Std Dev 11.31
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

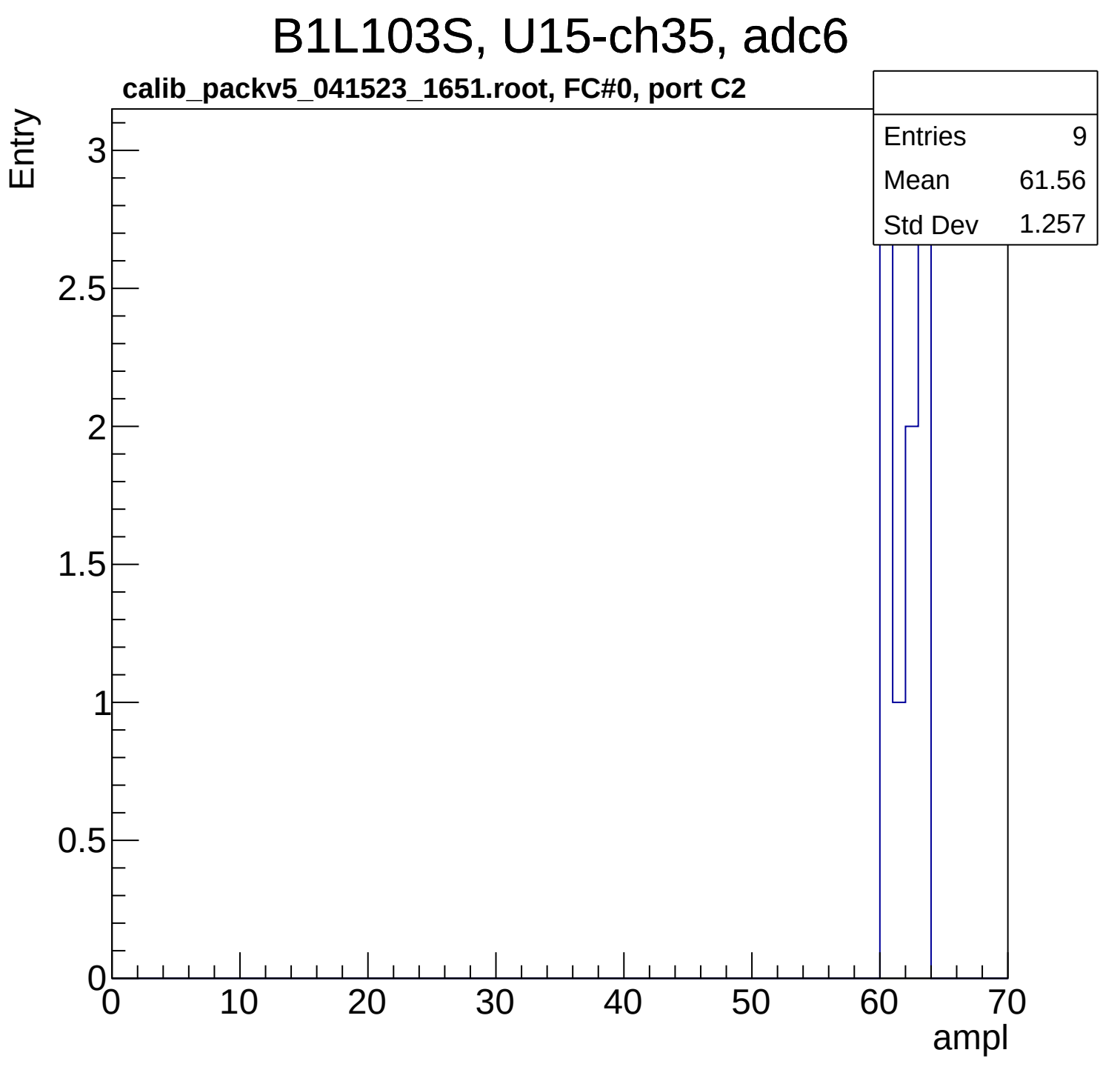

B1L103S, U15-ch35, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 33.35
Std Dev 6.252
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch35, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 33.39
Std Dev 15.2
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch35, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 45.37
Std Dev 8.83
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch35, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 52.16
Std Dev 3.875
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch35, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 57.41
Std Dev 3.316
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch35, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.56
Std Dev 1.257
Entry
ampl
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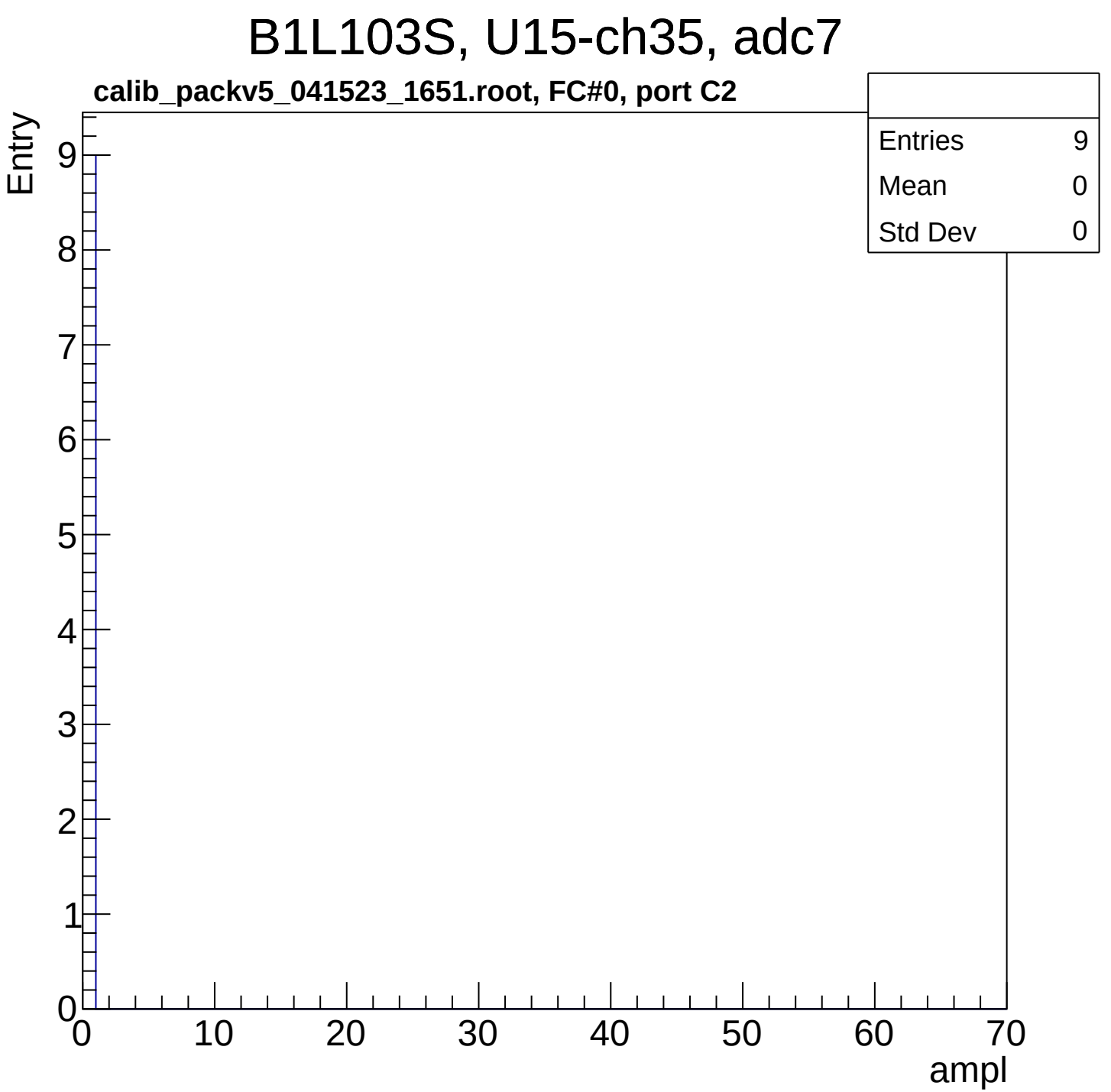
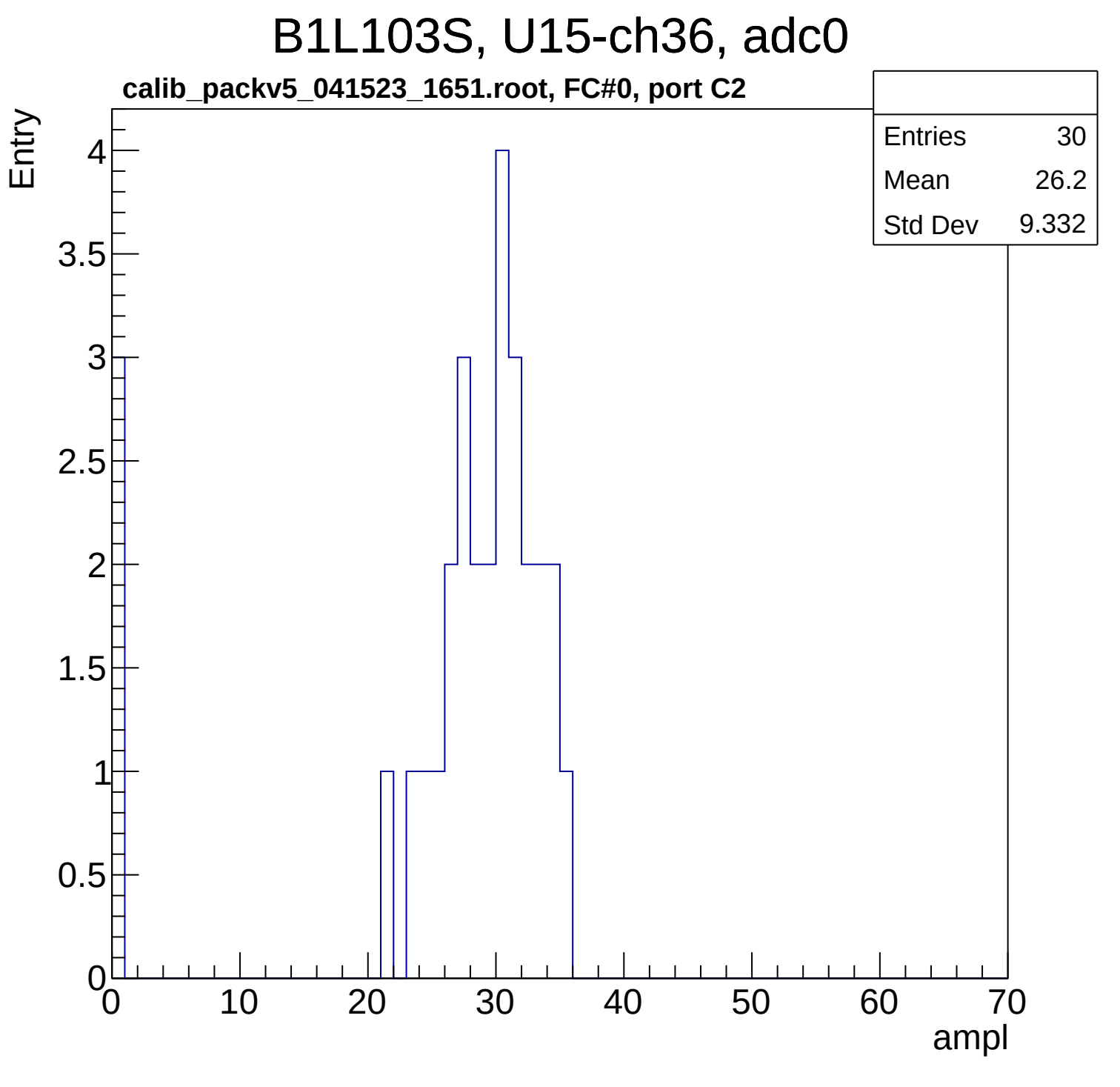
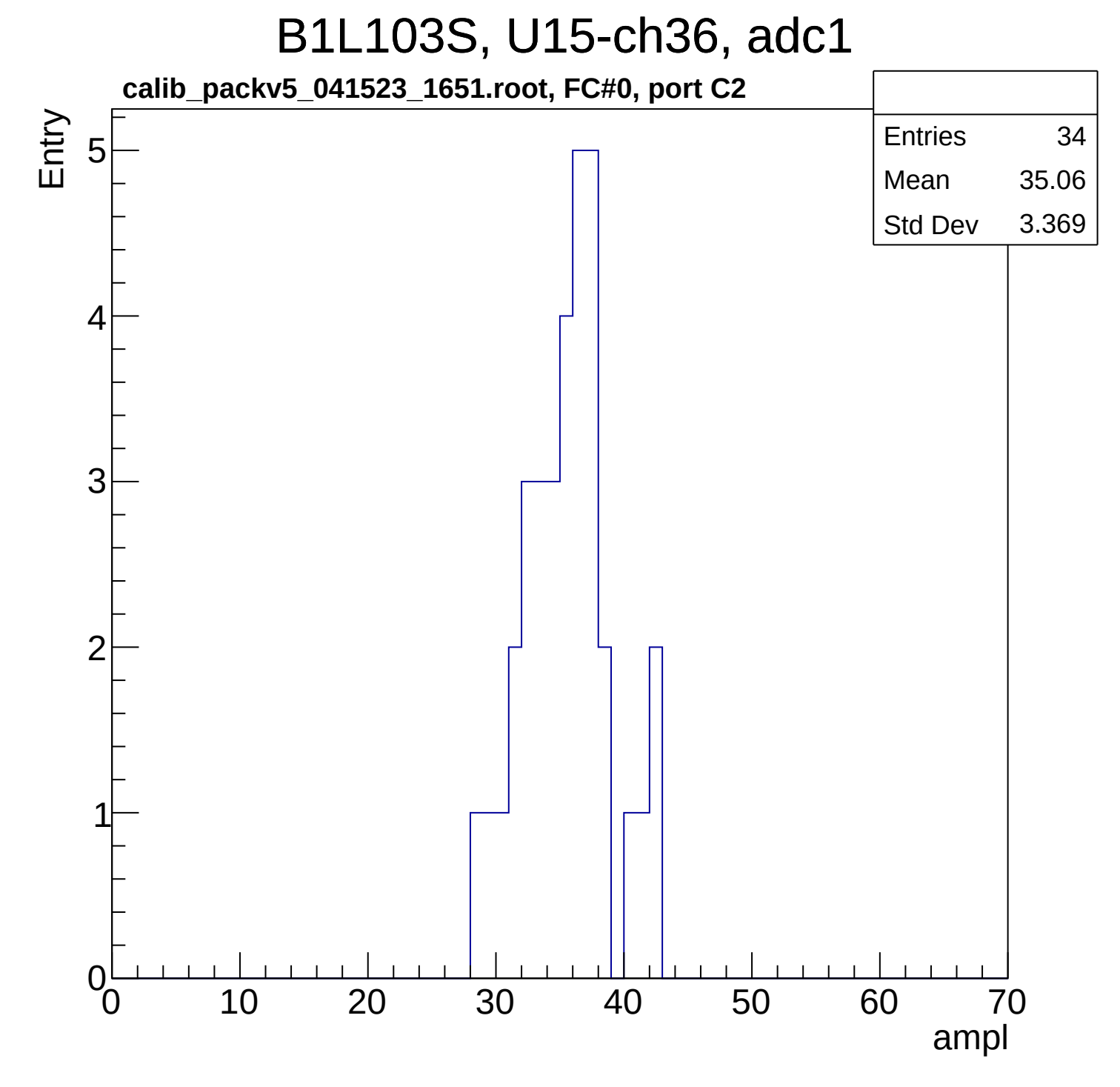
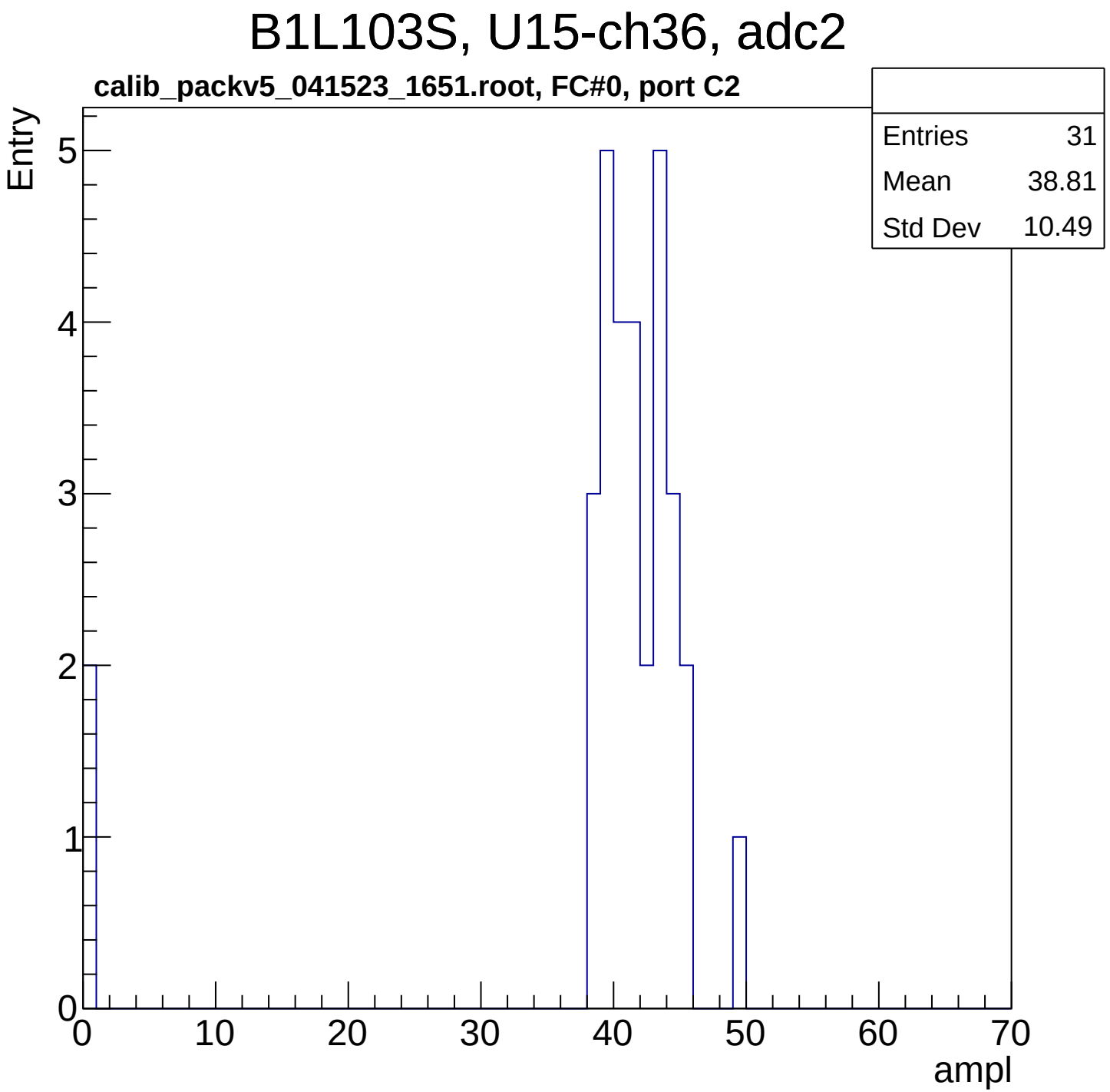
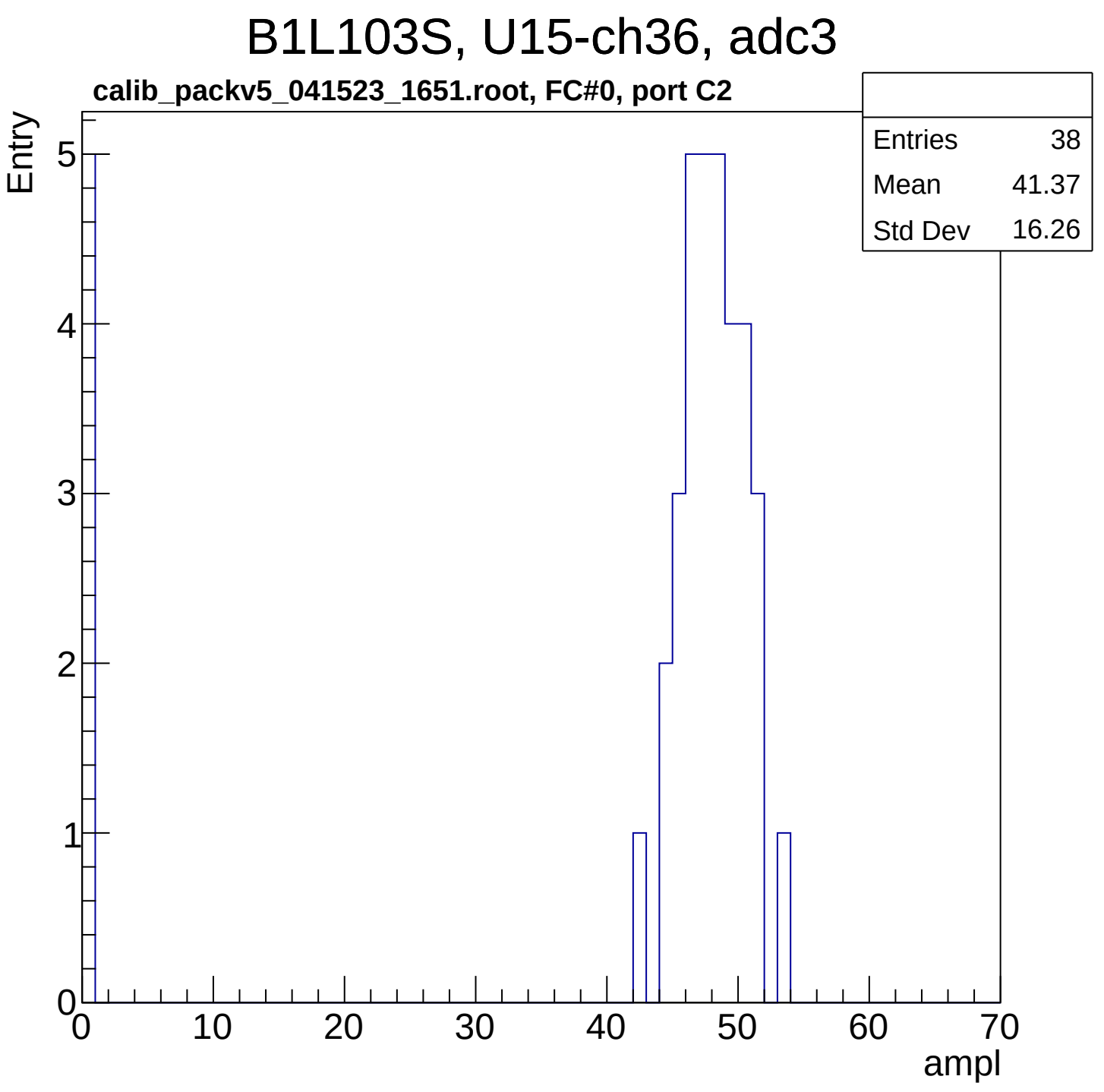
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

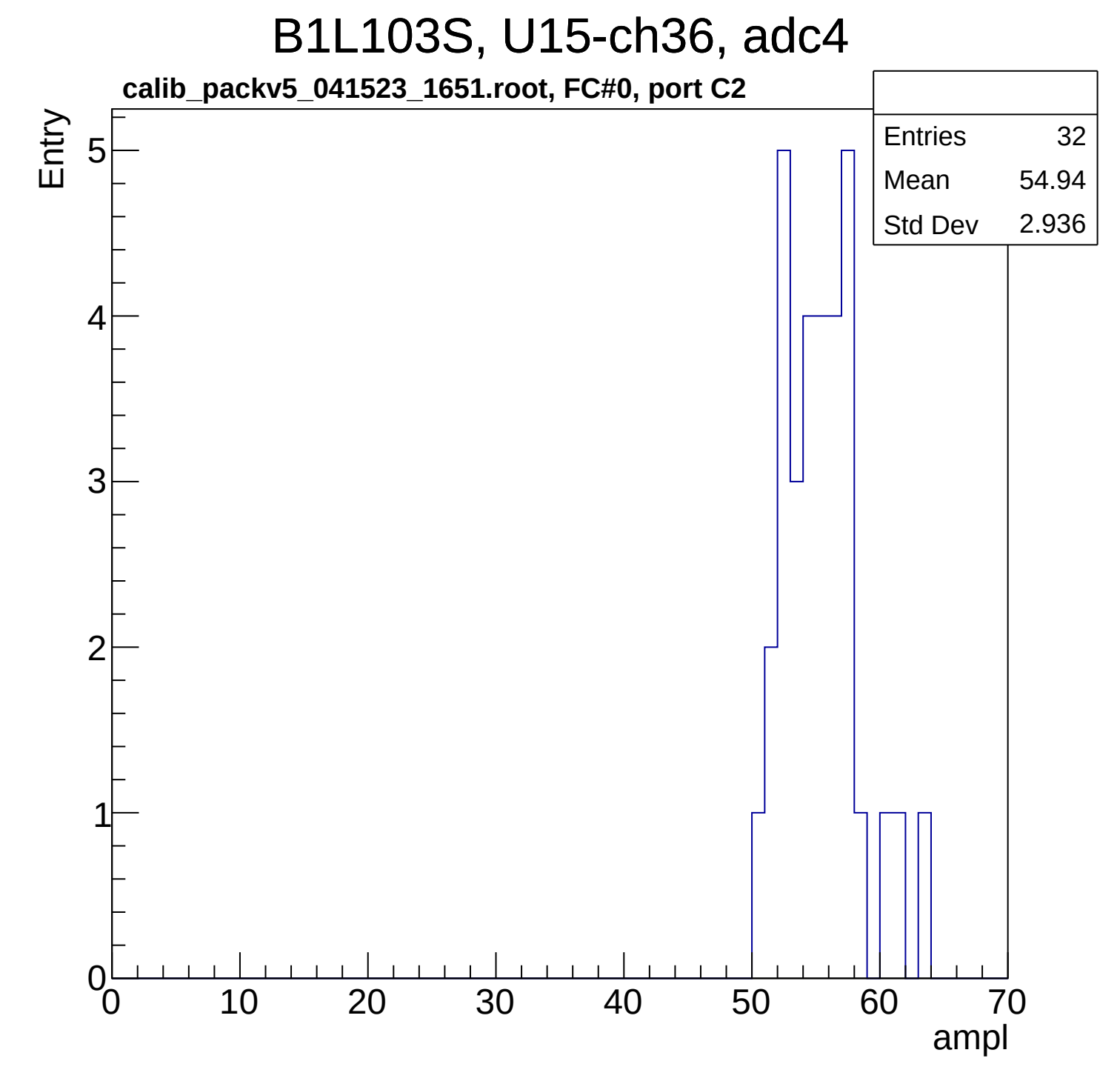

B1L103S, U15-ch35, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 0
Std Dev 0
Entry
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70
ampl

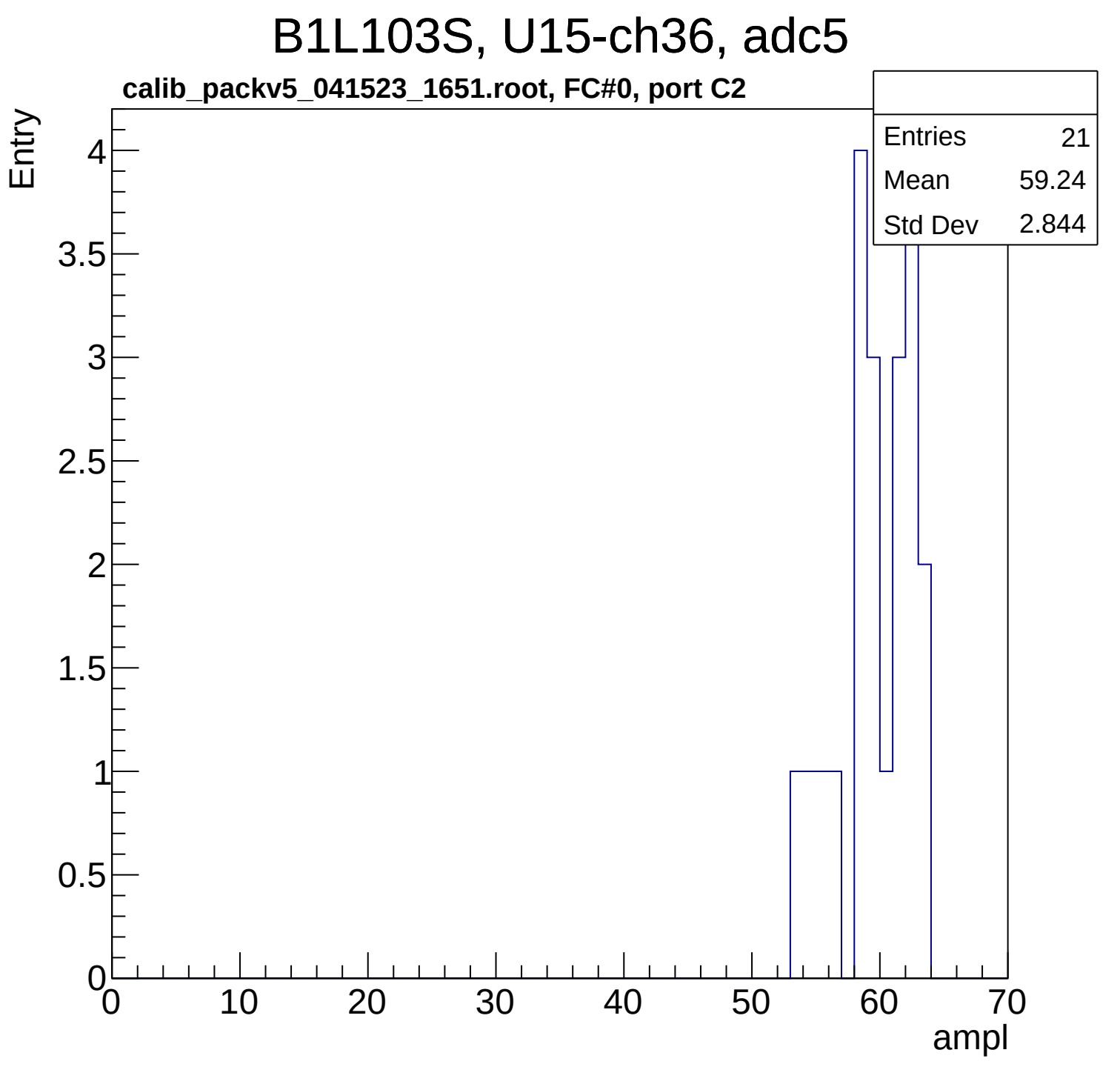

B1L103S, U15-ch36, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 26.2
Std Dev 9.332
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch36, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 35.06
Std Dev 3.369
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch36, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 38.81
Std Dev 10.49
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch36, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 41.37
Std Dev 16.26
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch36, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 54.94
Std Dev 2.936
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch36, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 59.24
Std Dev 2.844
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
50
60
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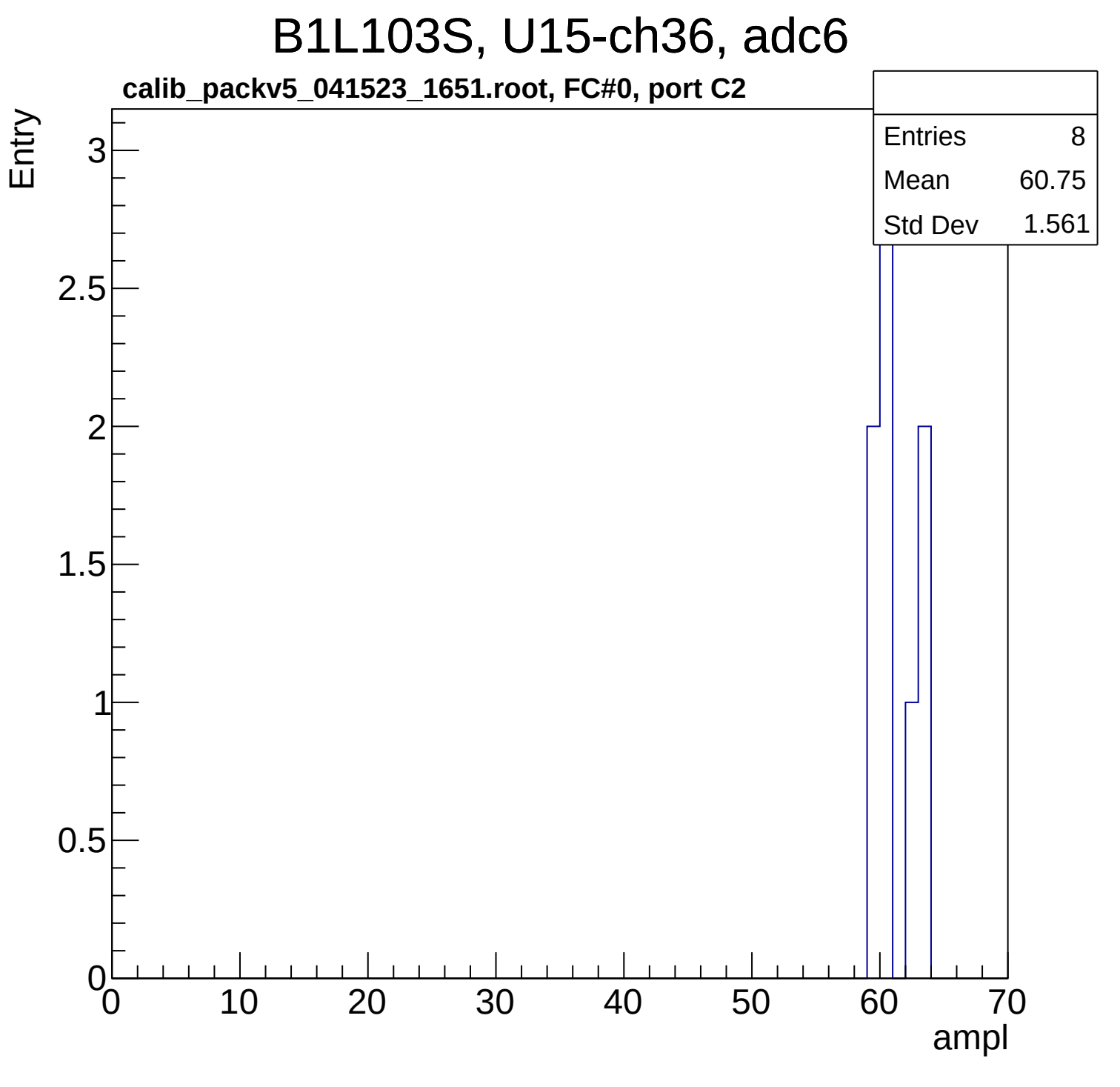
B1L103S, U15-ch36, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 60.75
Std Dev 1.561
Entry
ampl
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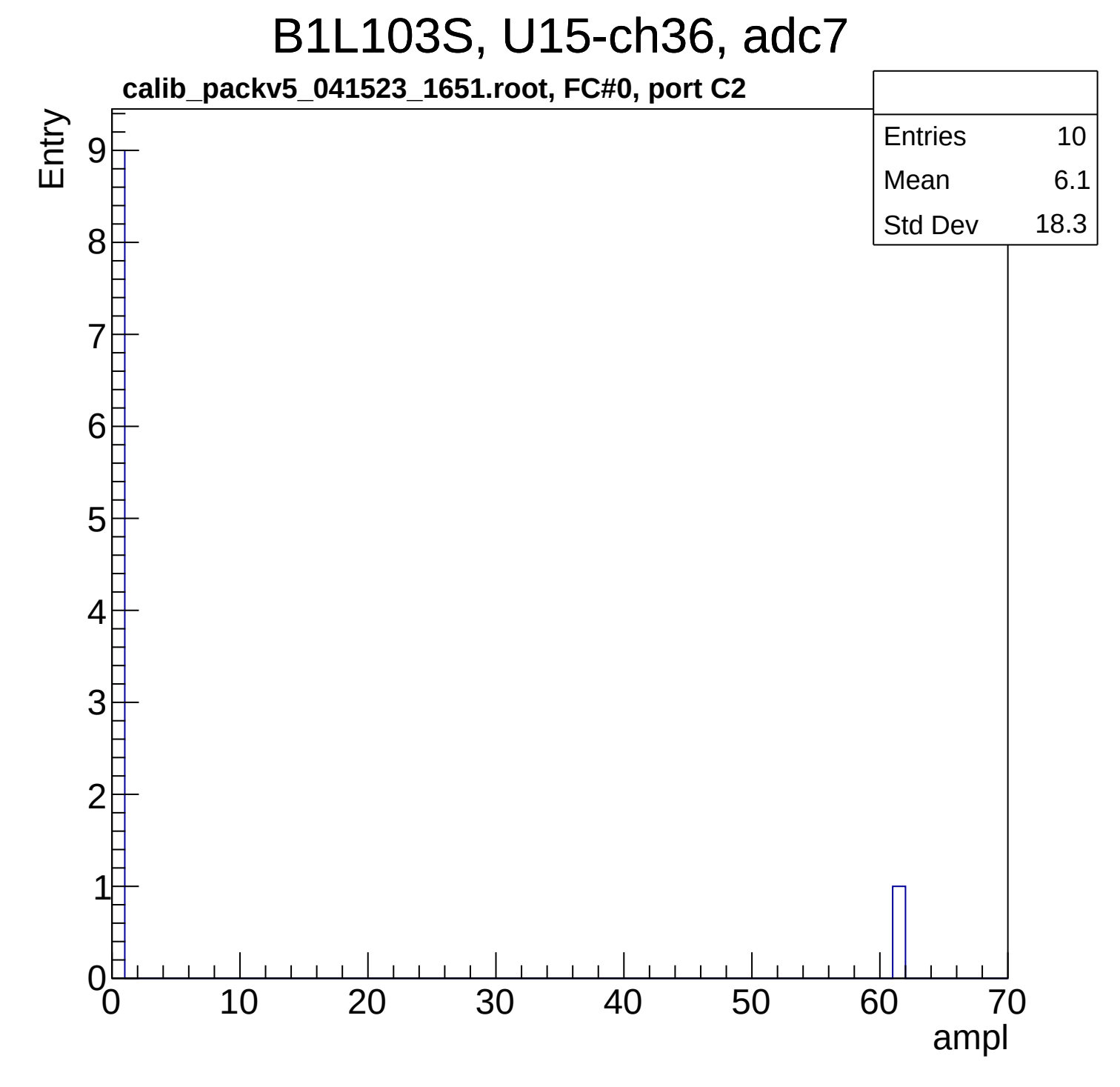
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch36, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 6.1
Std Dev 18.3
Entry
ampl
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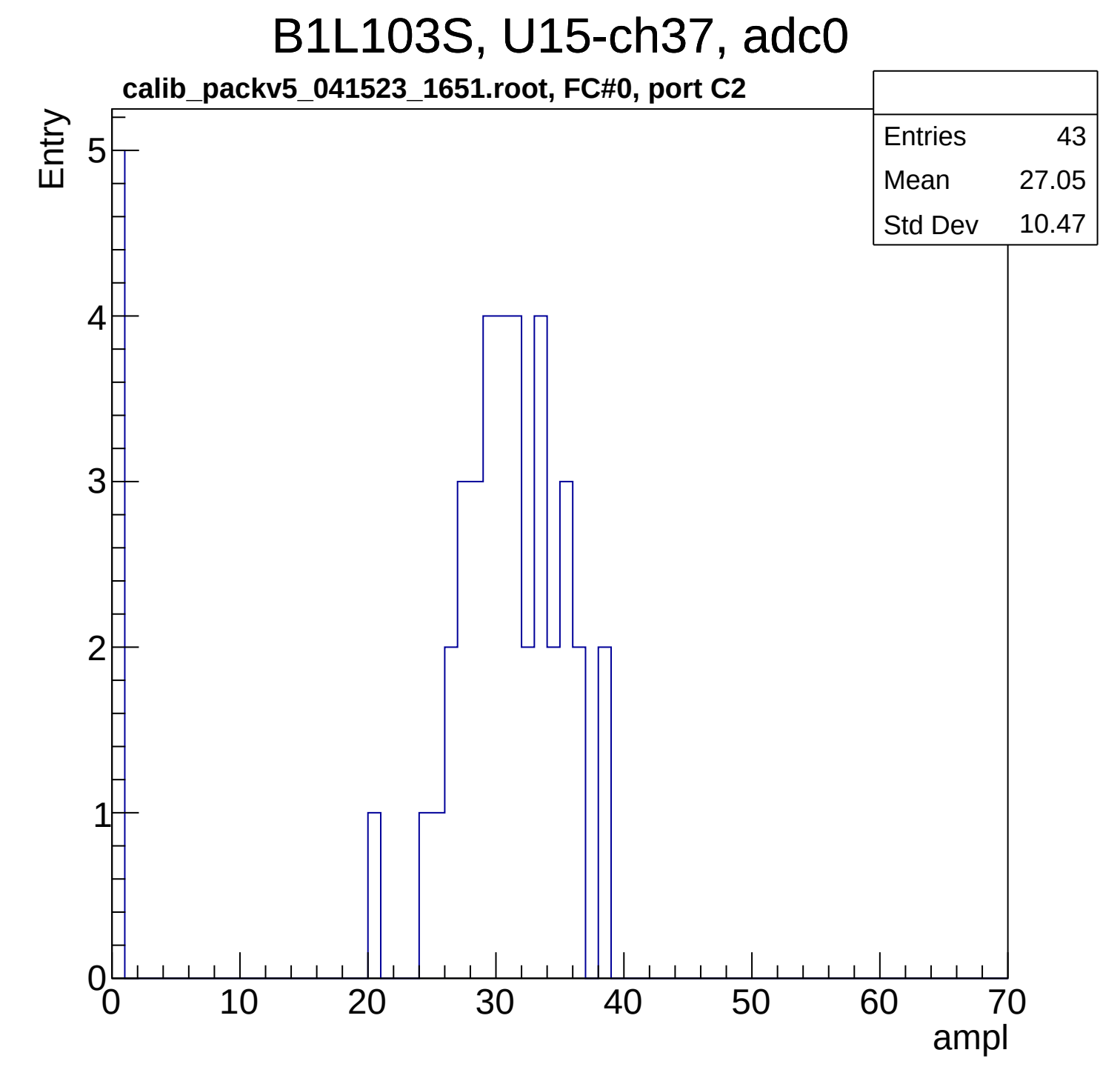
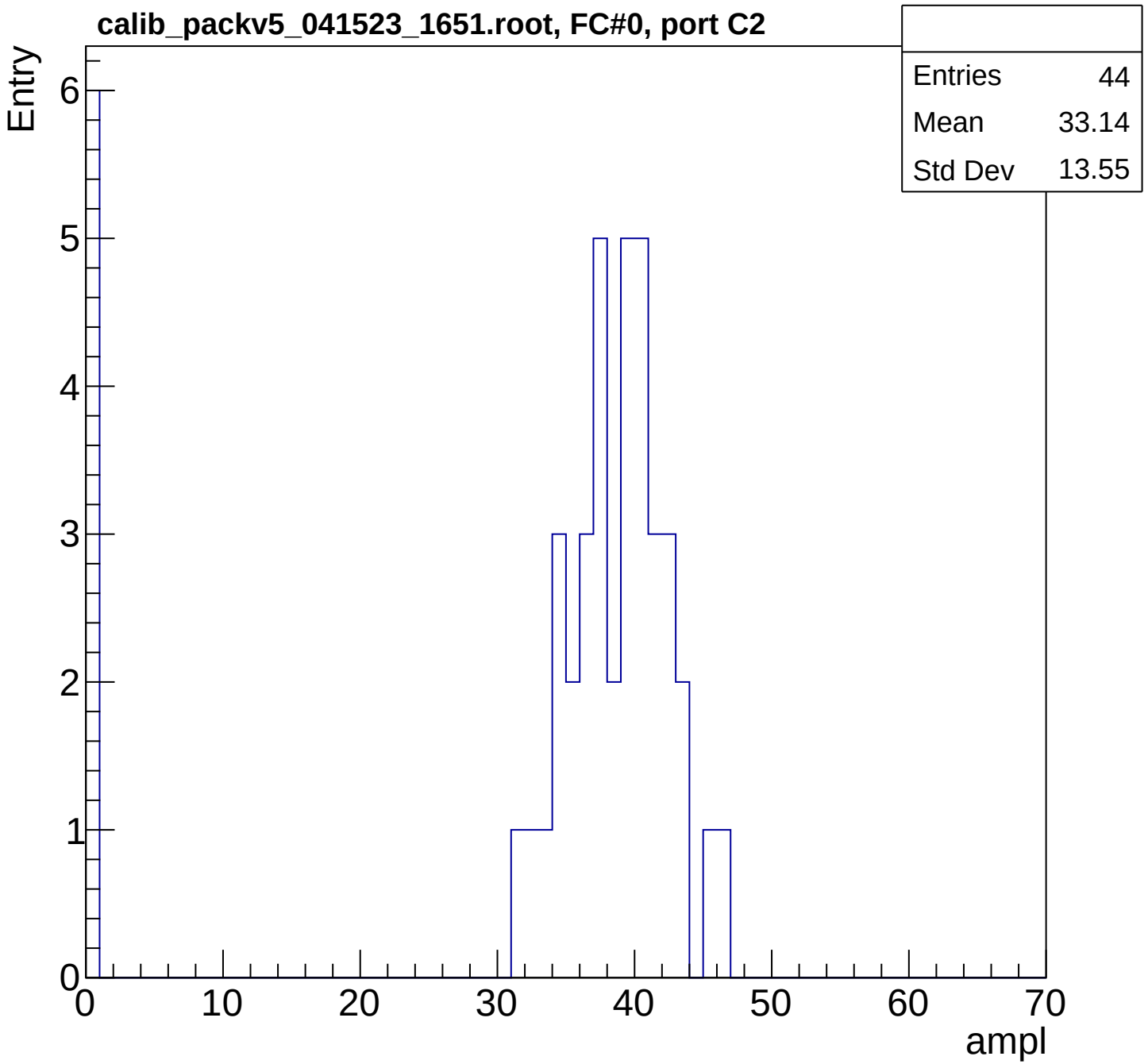
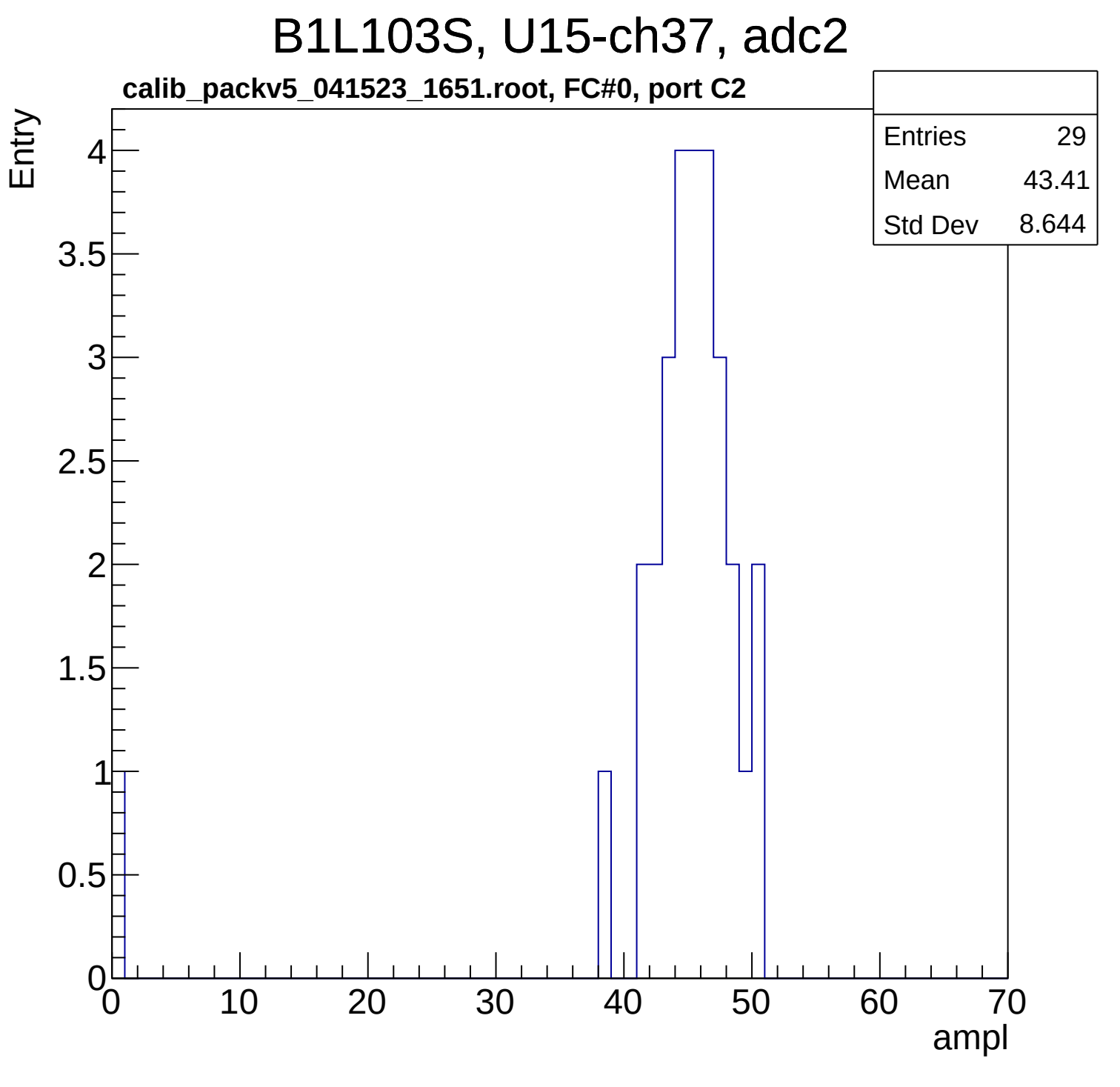
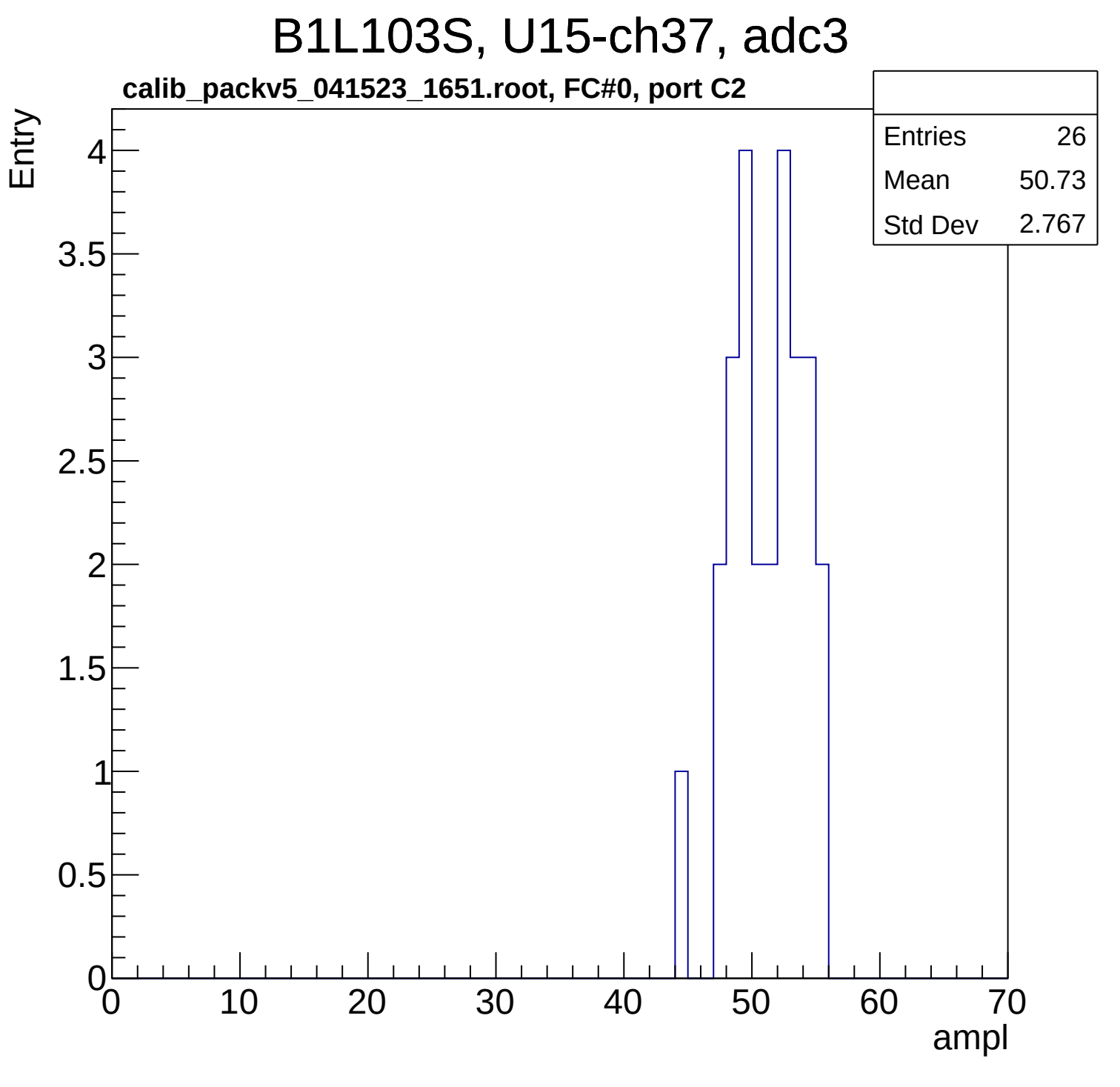
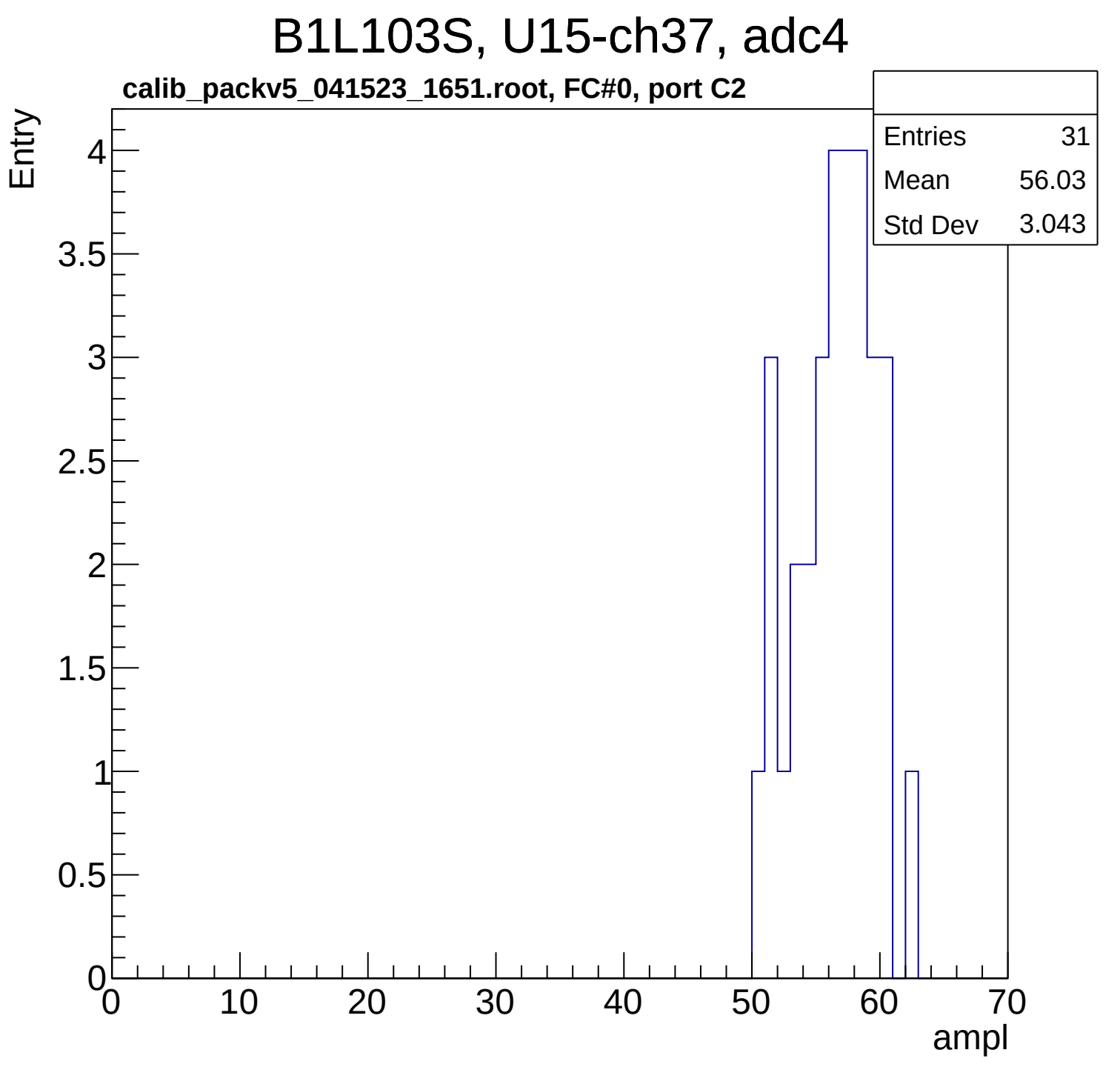
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

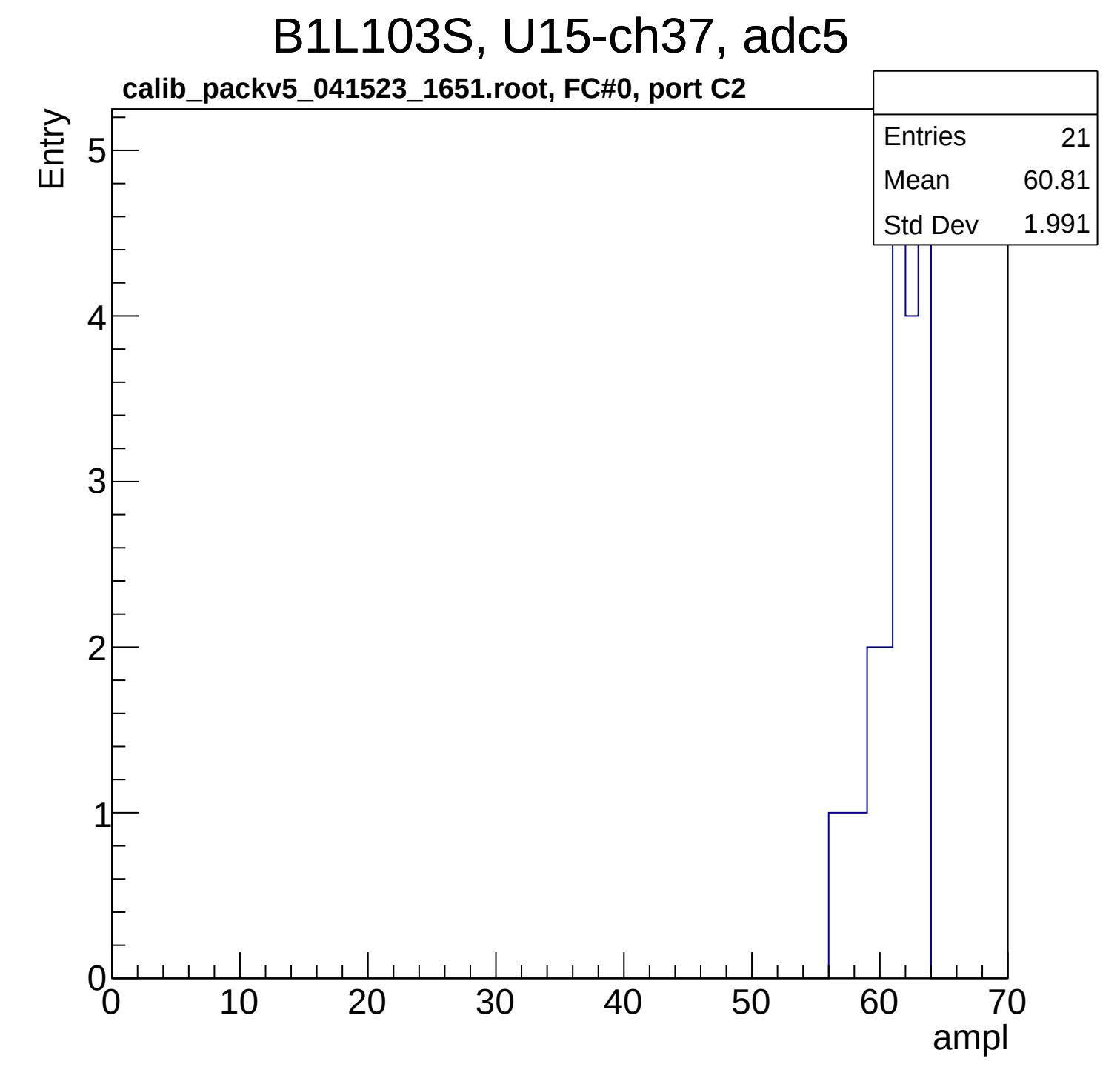

B1L103S, U15-ch37, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 27.05
Std Dev 10.47
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

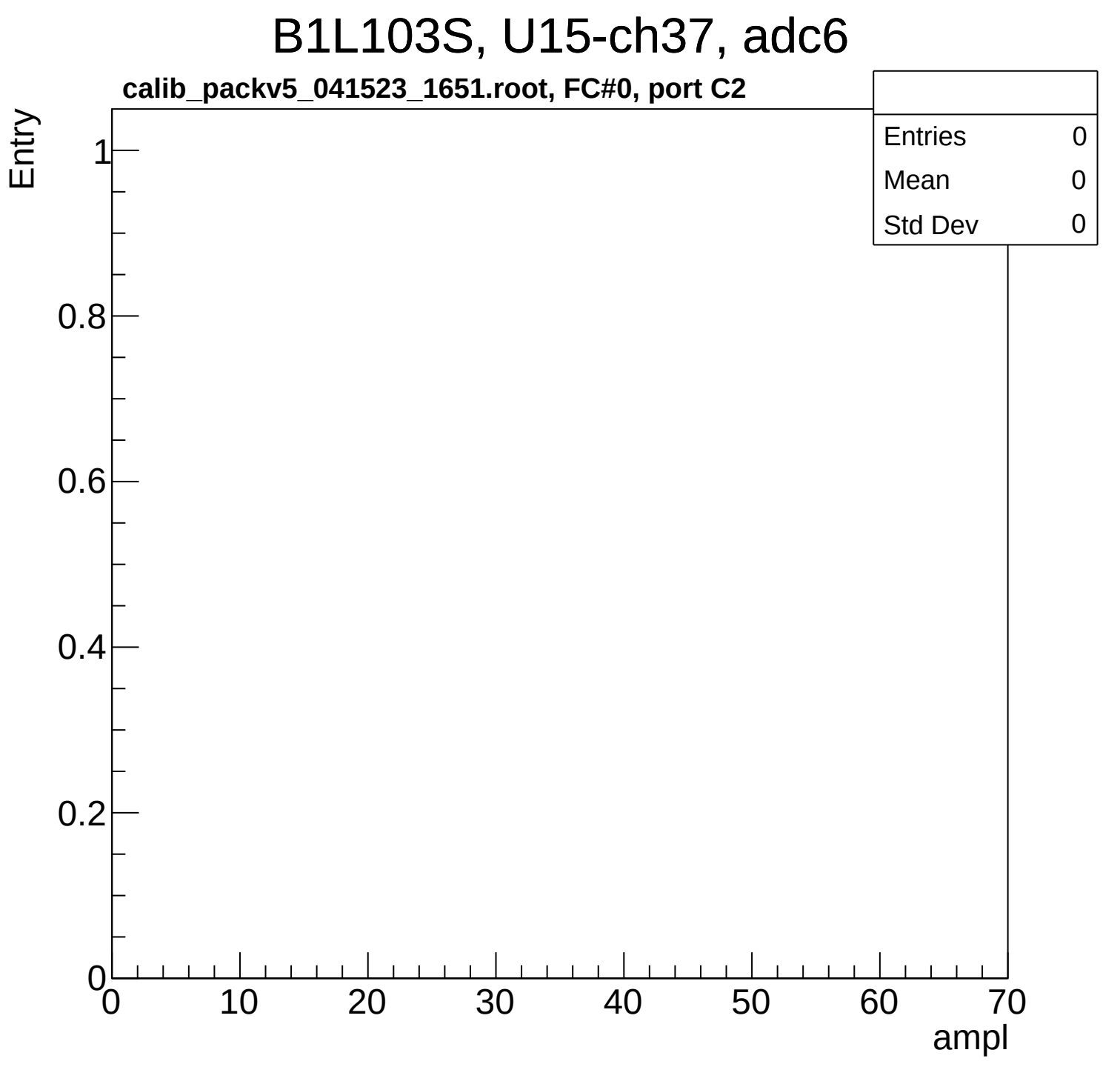

B1L103S, U15-ch37, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 33.14
Std Dev 13.55
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

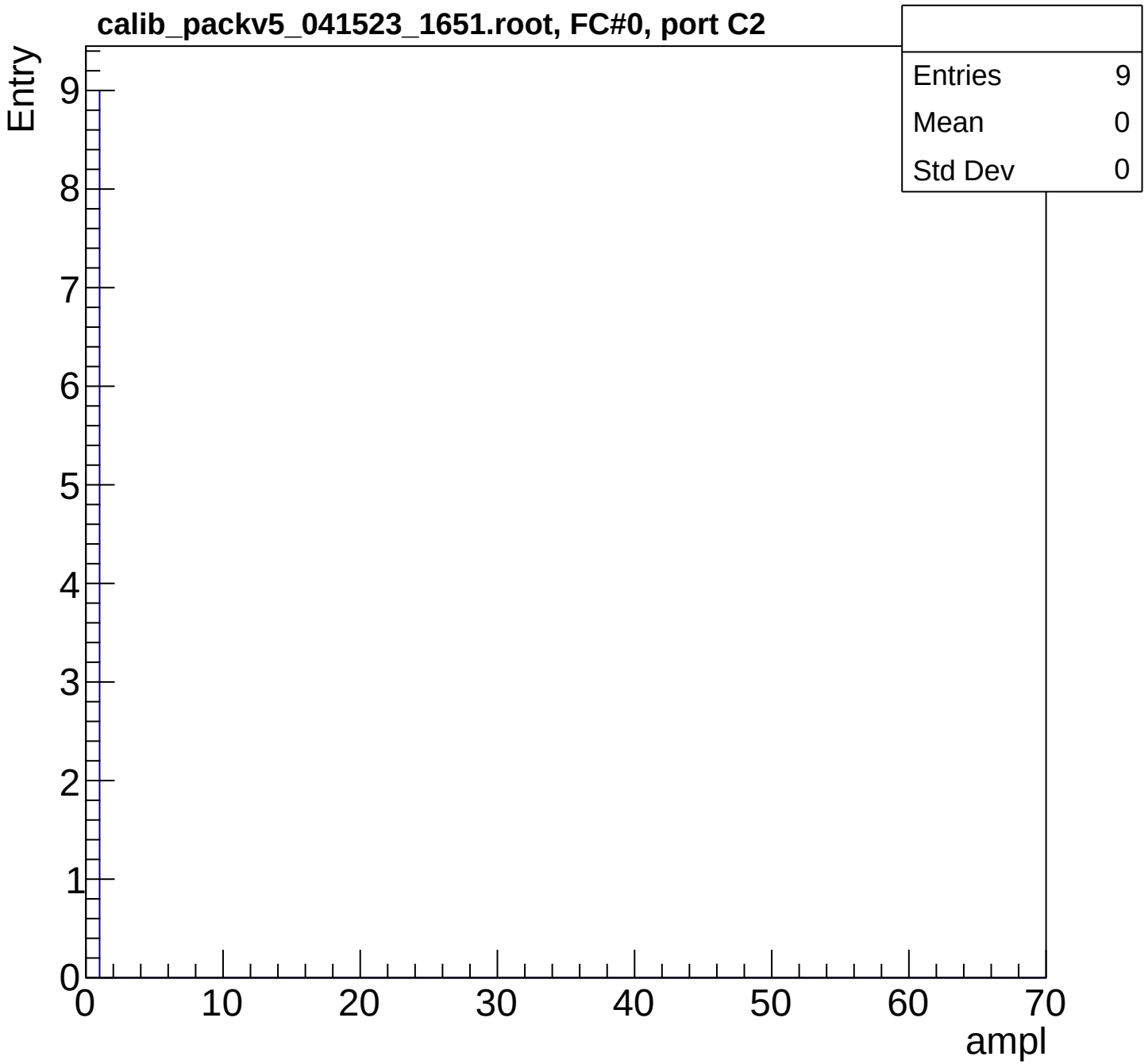

B1L103S, U15-ch37, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 43.41
Std Dev 8.644
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

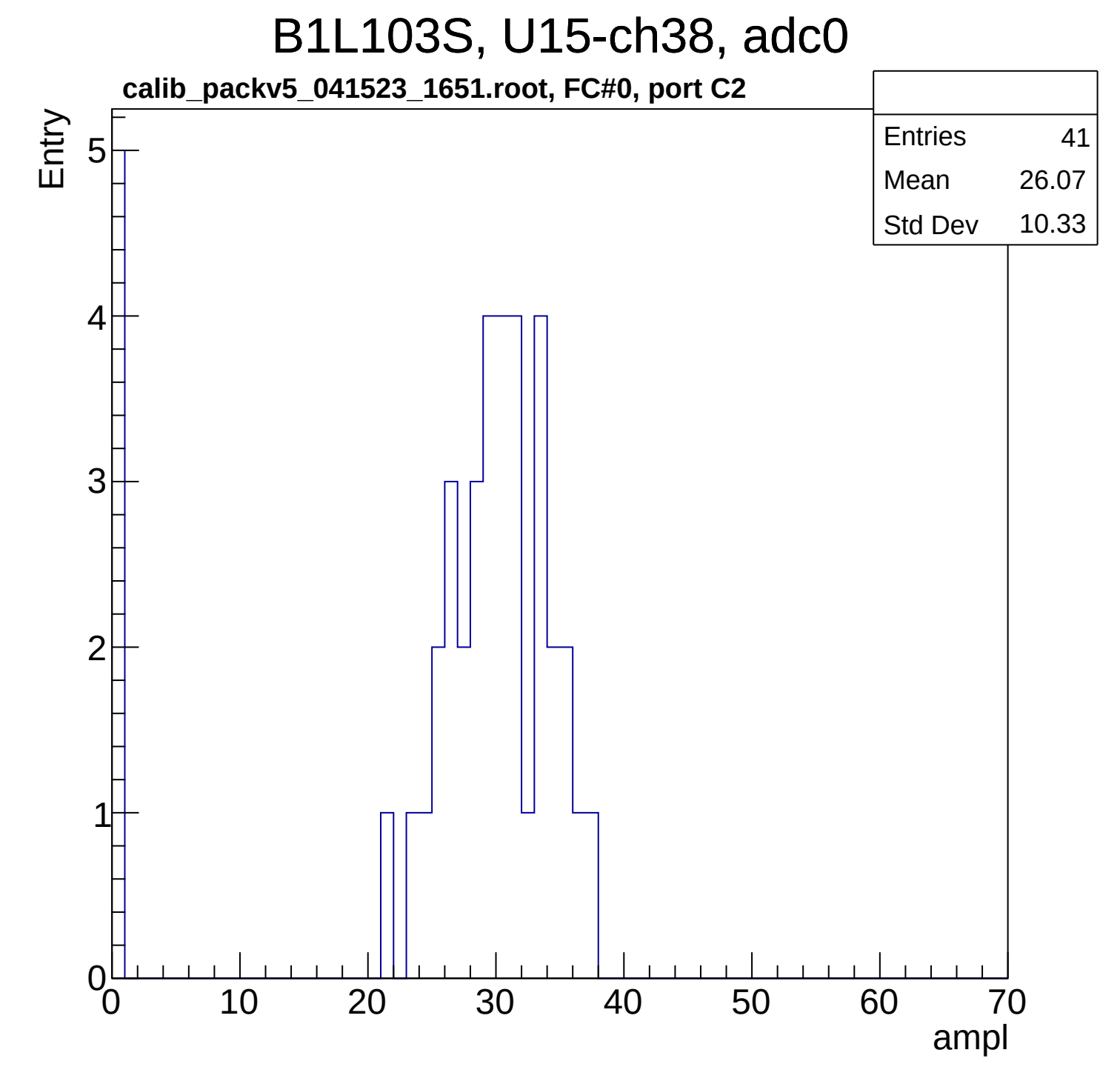

B1L103S, U15-ch37, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 50.73
Std Dev 2.767
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

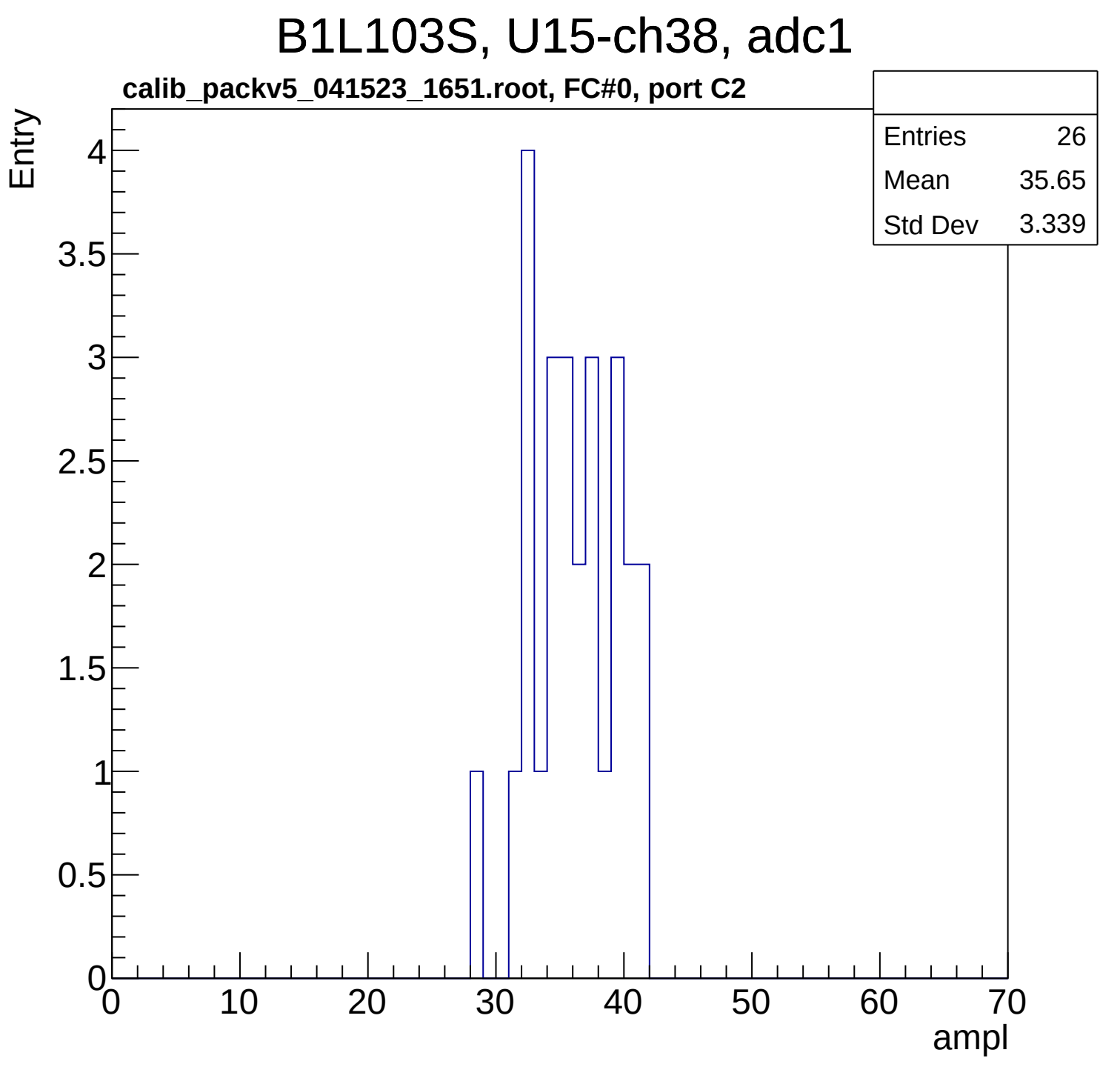

B1L103S, U15-ch37, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 56.03
Std Dev 3.043
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

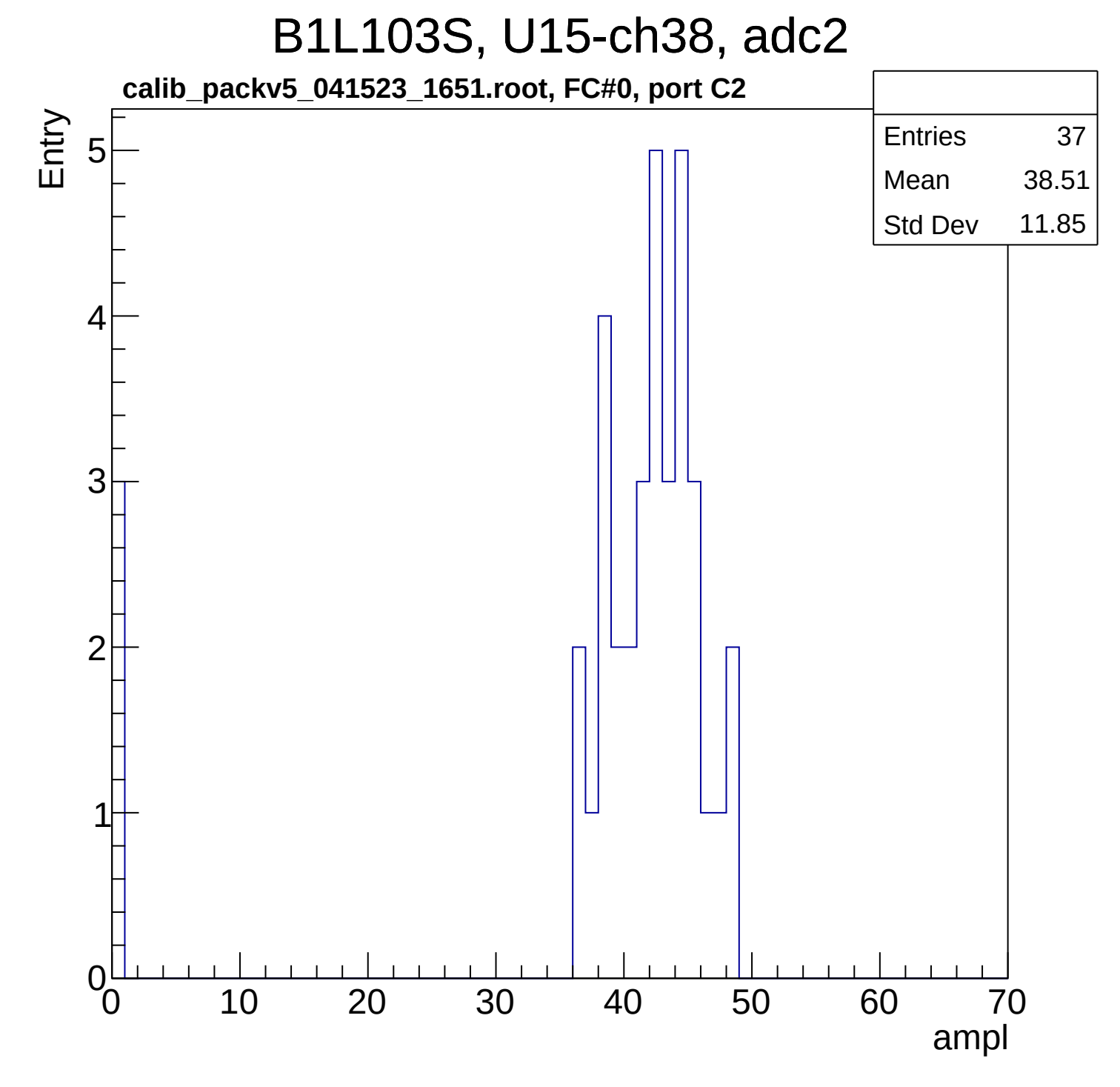

B1L103S, U15-ch37, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 60.81
Std Dev 1.991
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

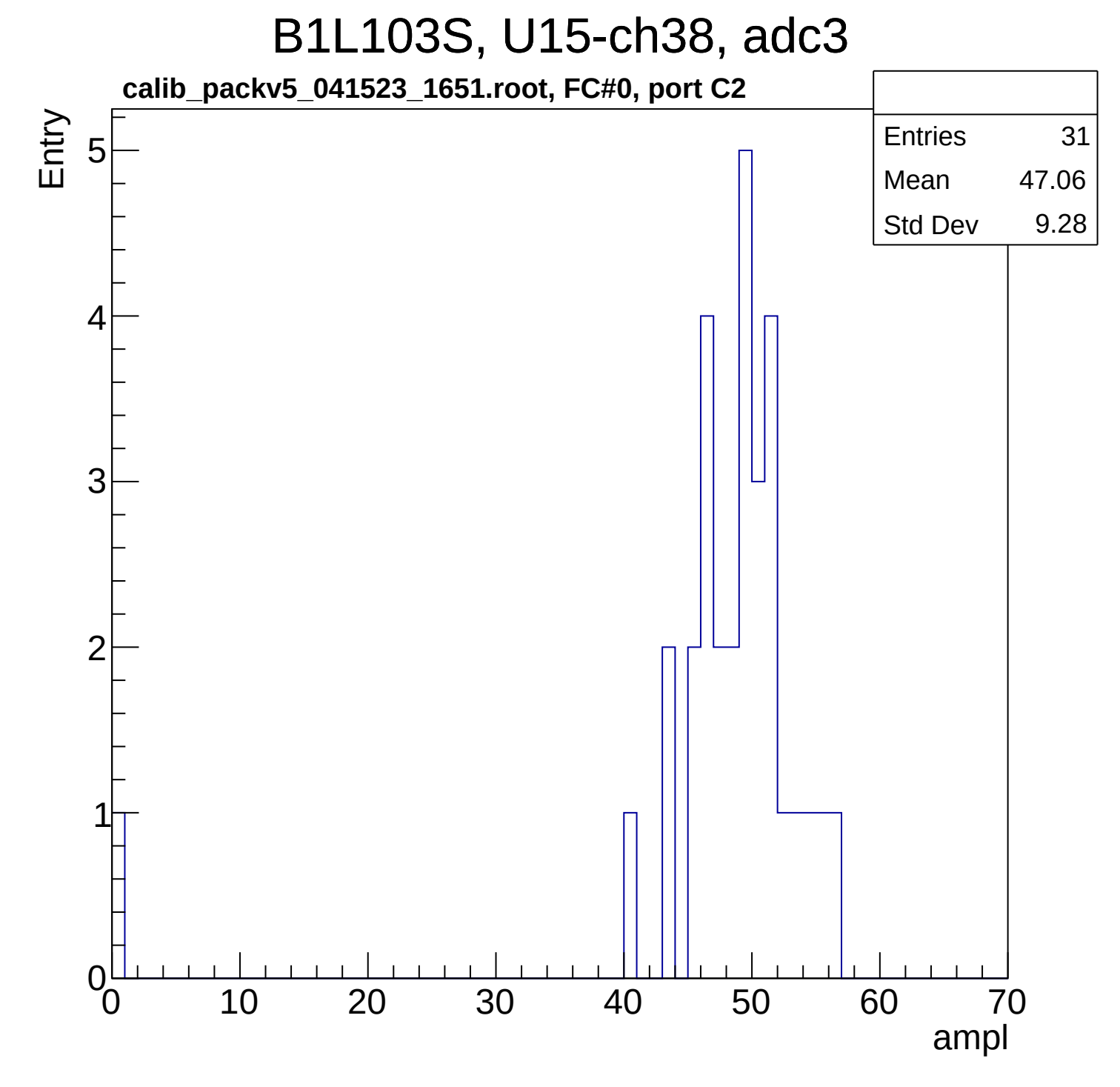

B1L103S, U15-ch37, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

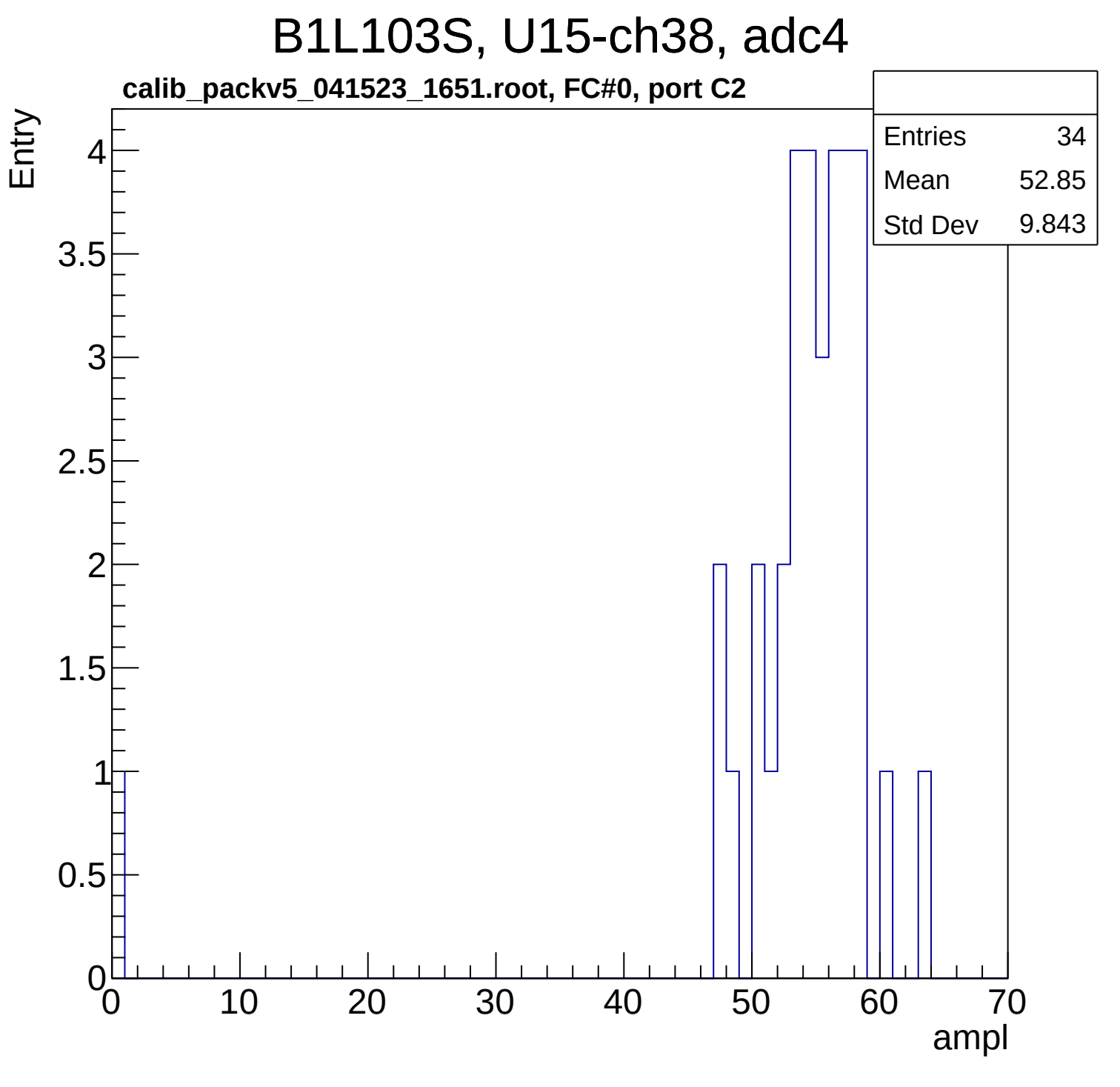

B1L103S, U15-ch37, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 0
Std Dev 0
Entry
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70
ampl

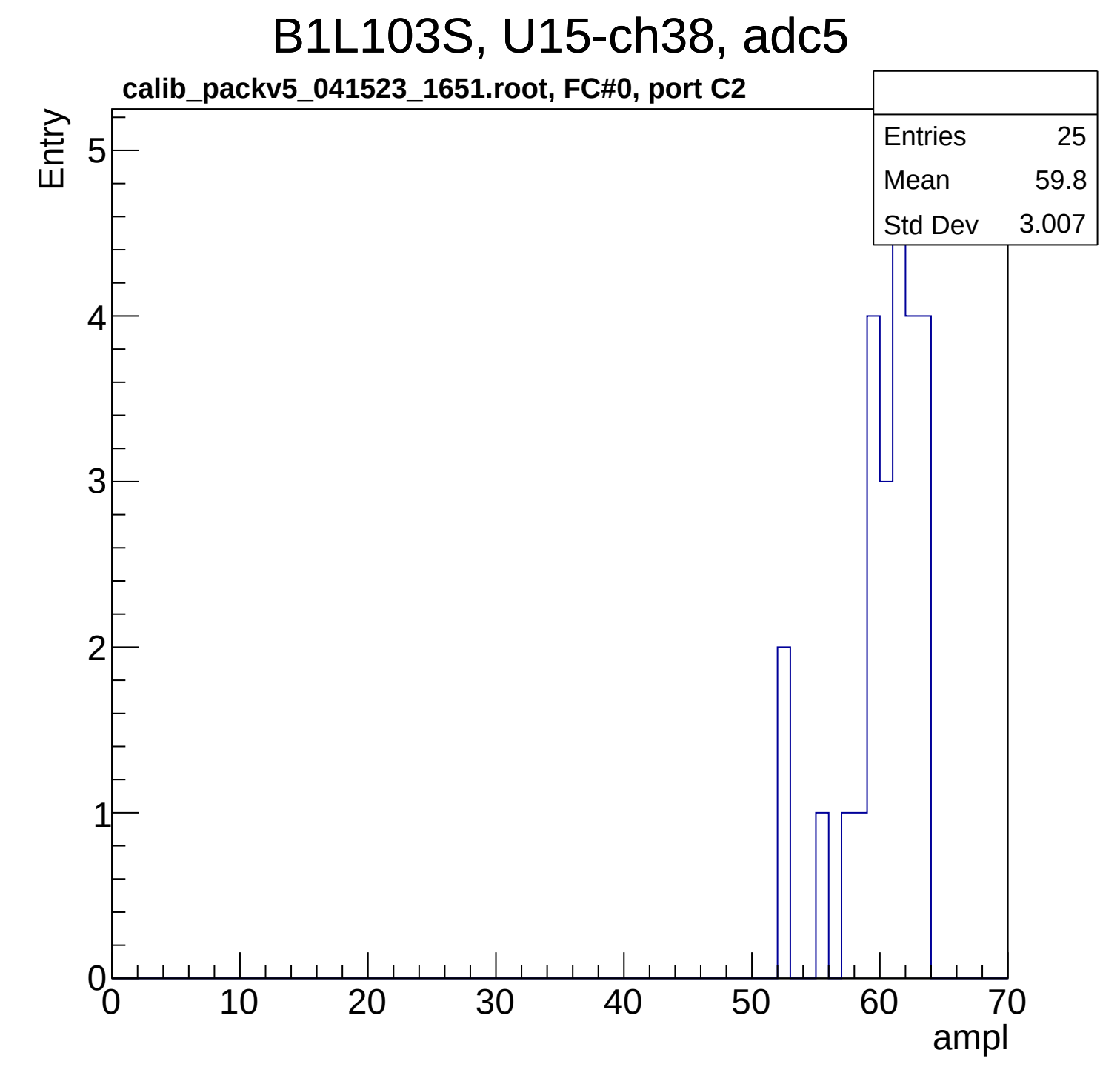

B1L103S, U15-ch38, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 26.07
Std Dev 10.33
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

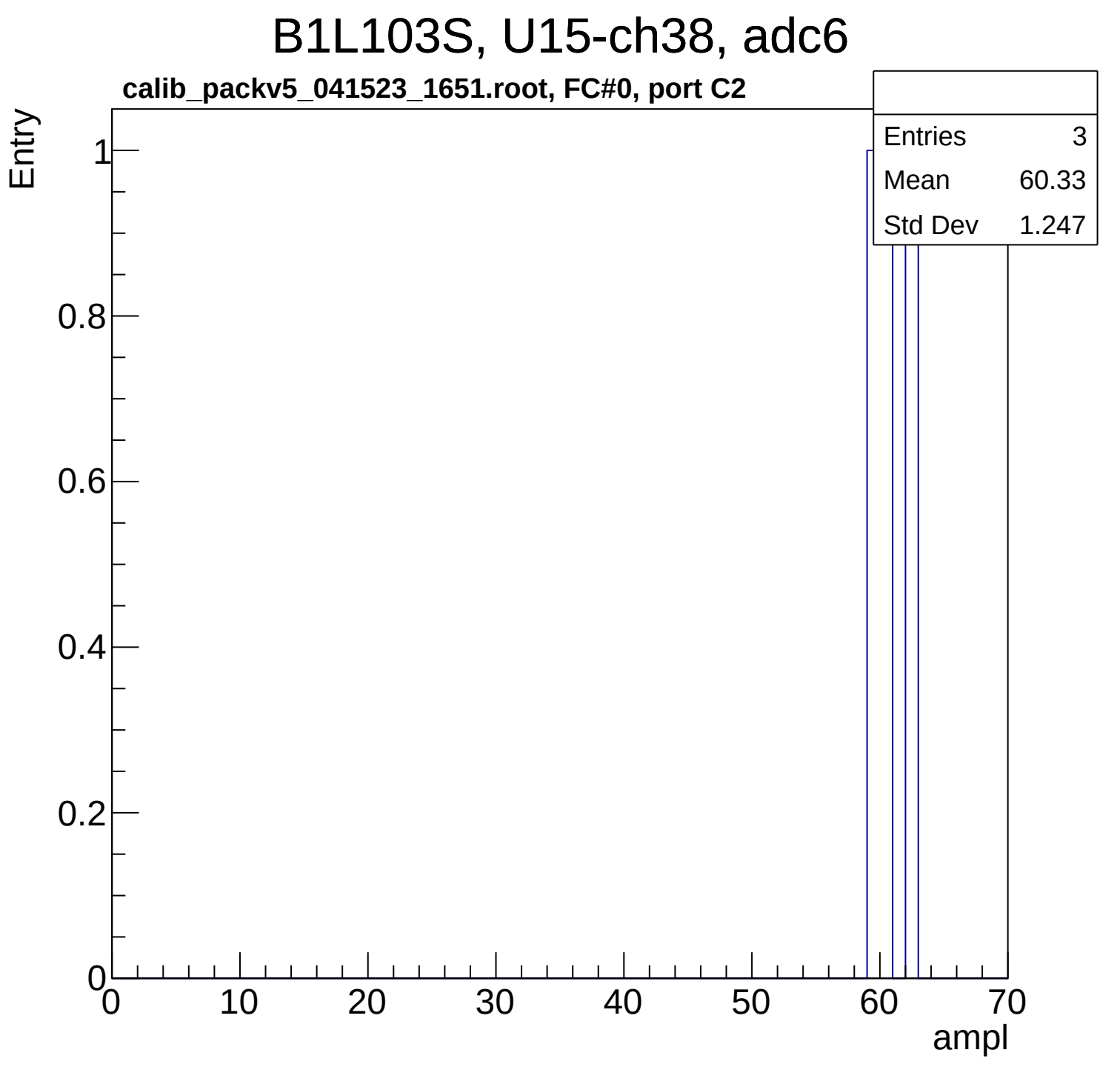

B1L103S, U15-ch38, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 35.65
Std Dev 3.339
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

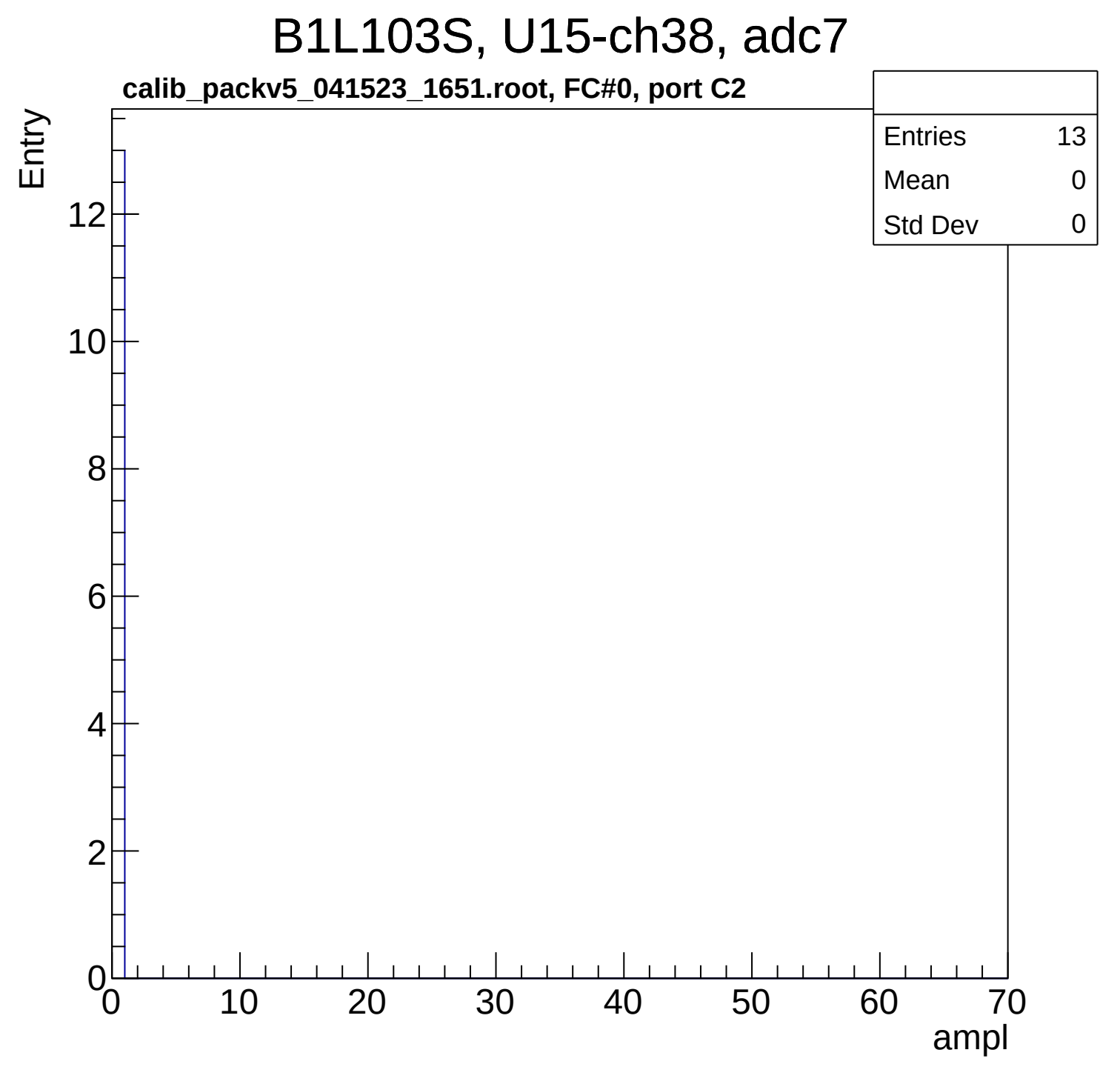

B1L103S, U15-ch38, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 38.51
Std Dev 11.85
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

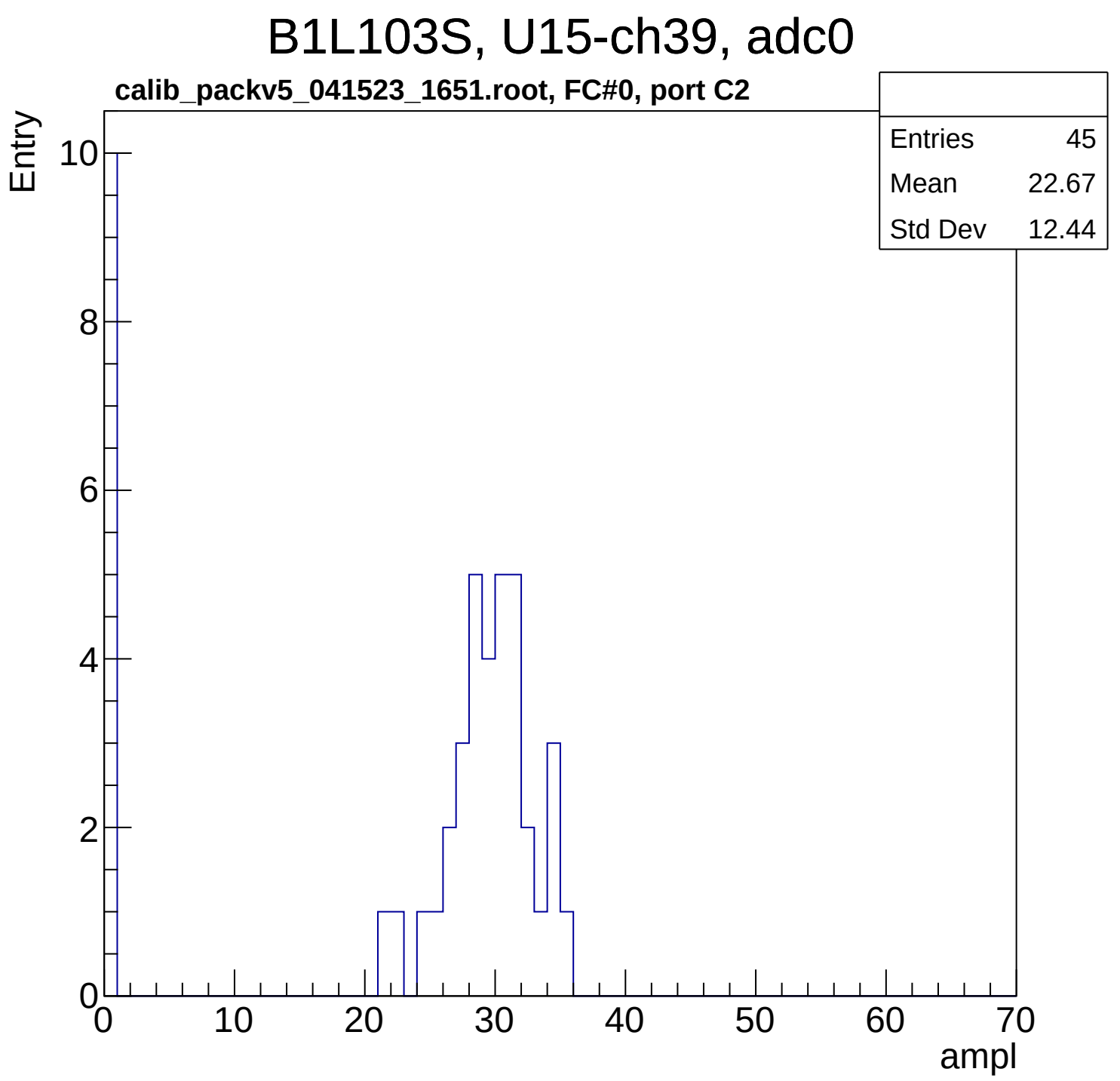

B1L103S, U15-ch38, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 47.06
Std Dev 9.28
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

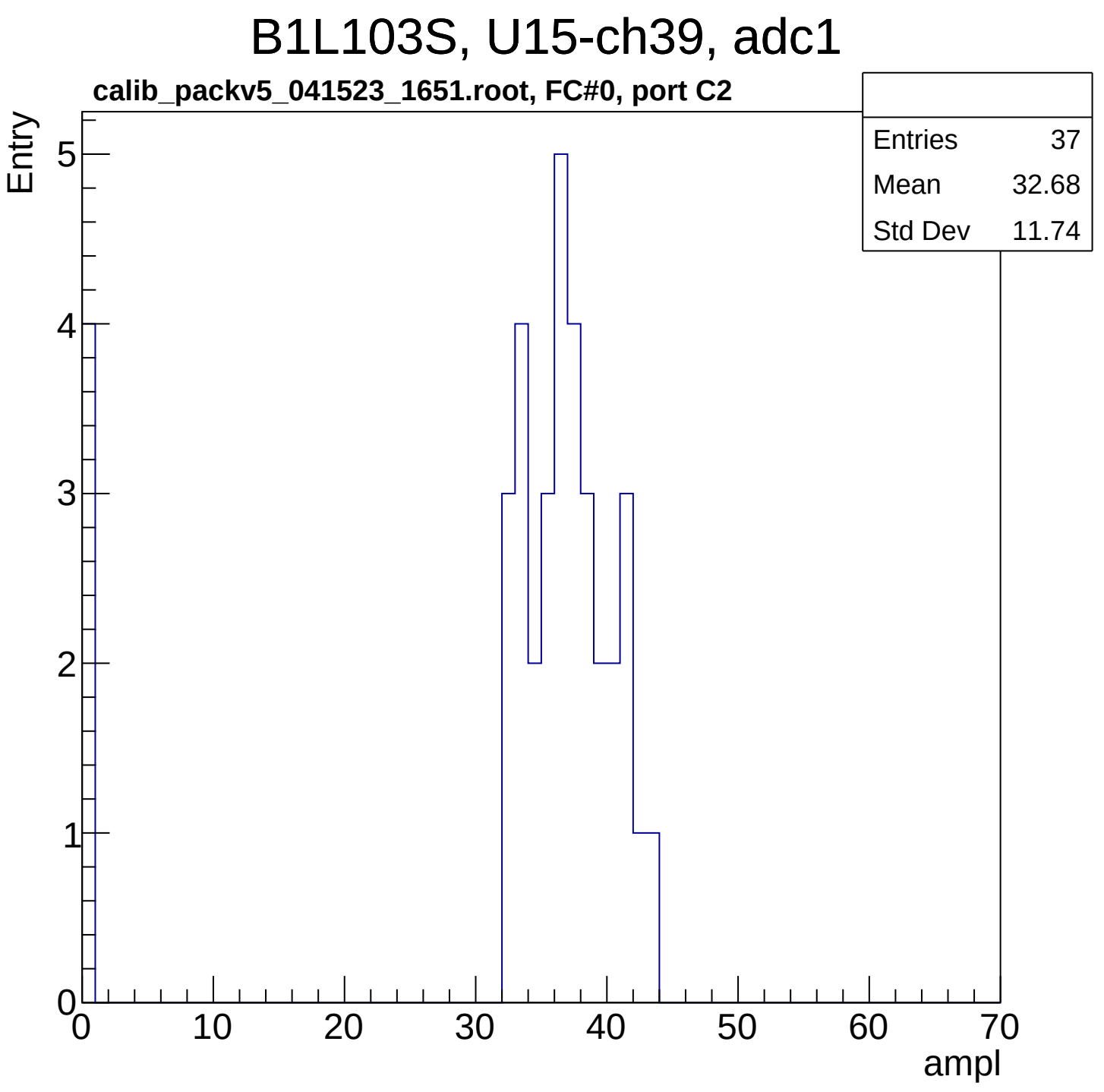

B1L103S, U15-ch38, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 52.85
Std Dev 9.843
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

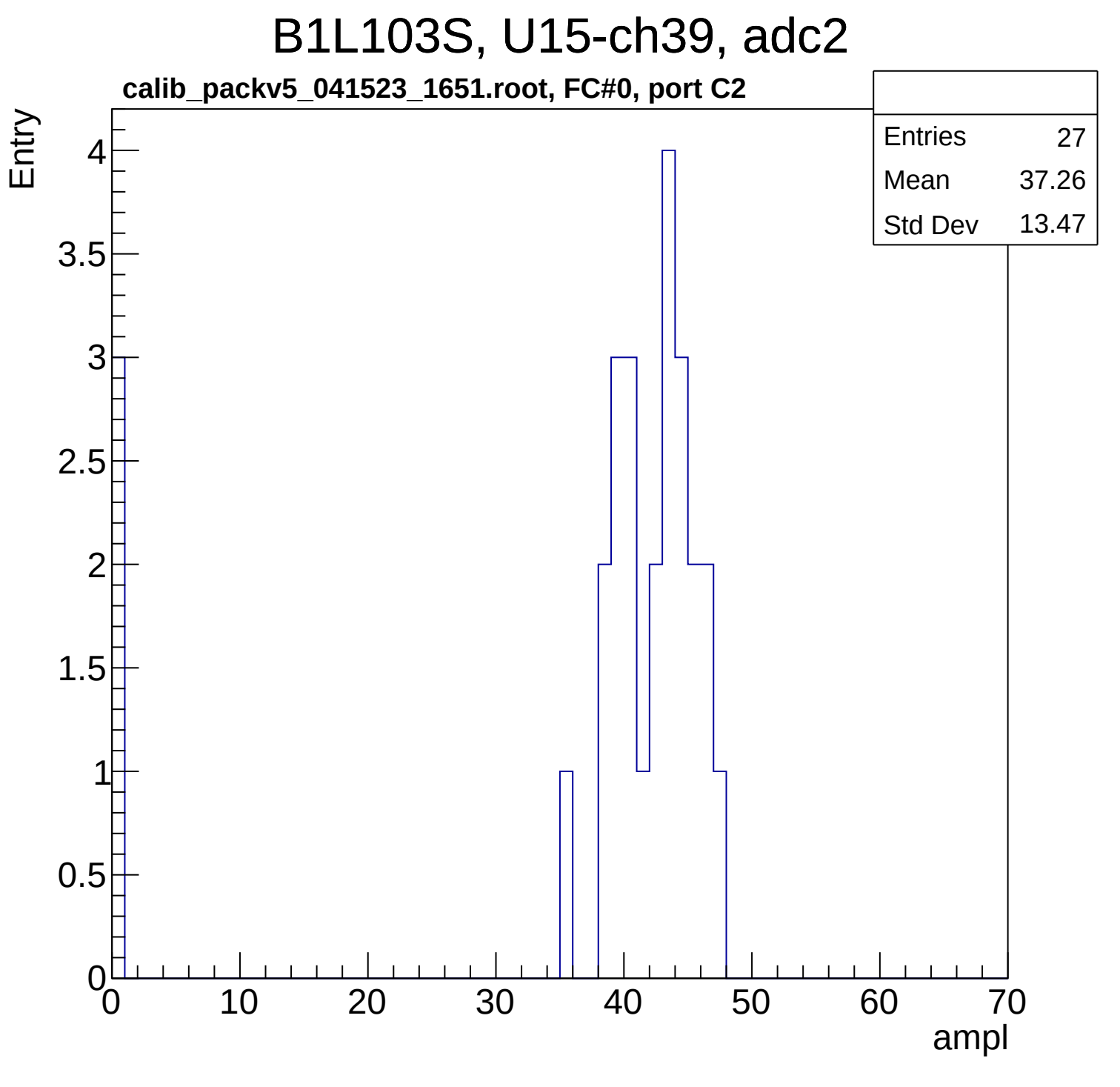

B1L103S, U15-ch38, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 59.8
Std Dev 3.007
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

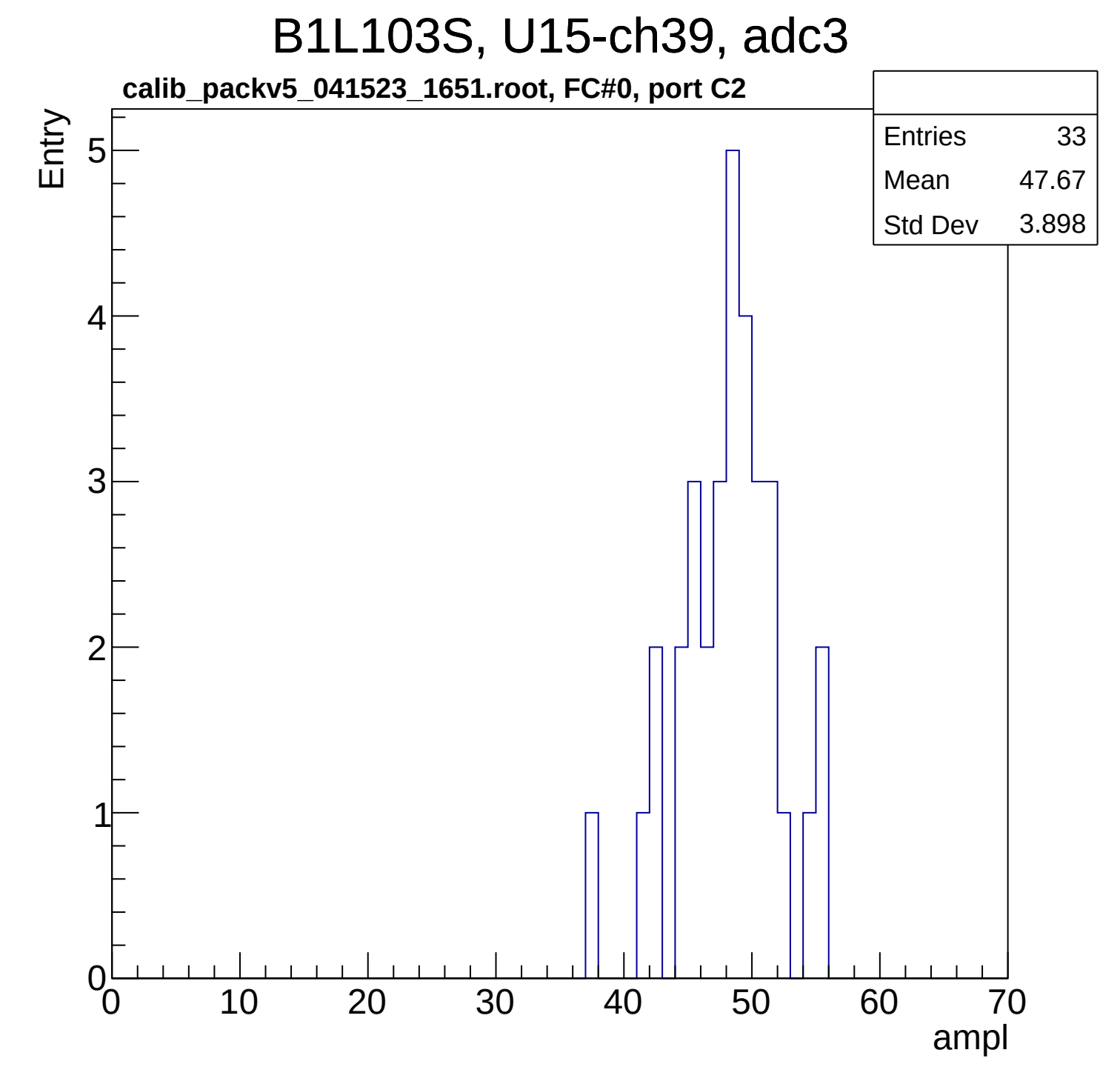

B1L103S, U15-ch38, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 60.33
Std Dev 1.247
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

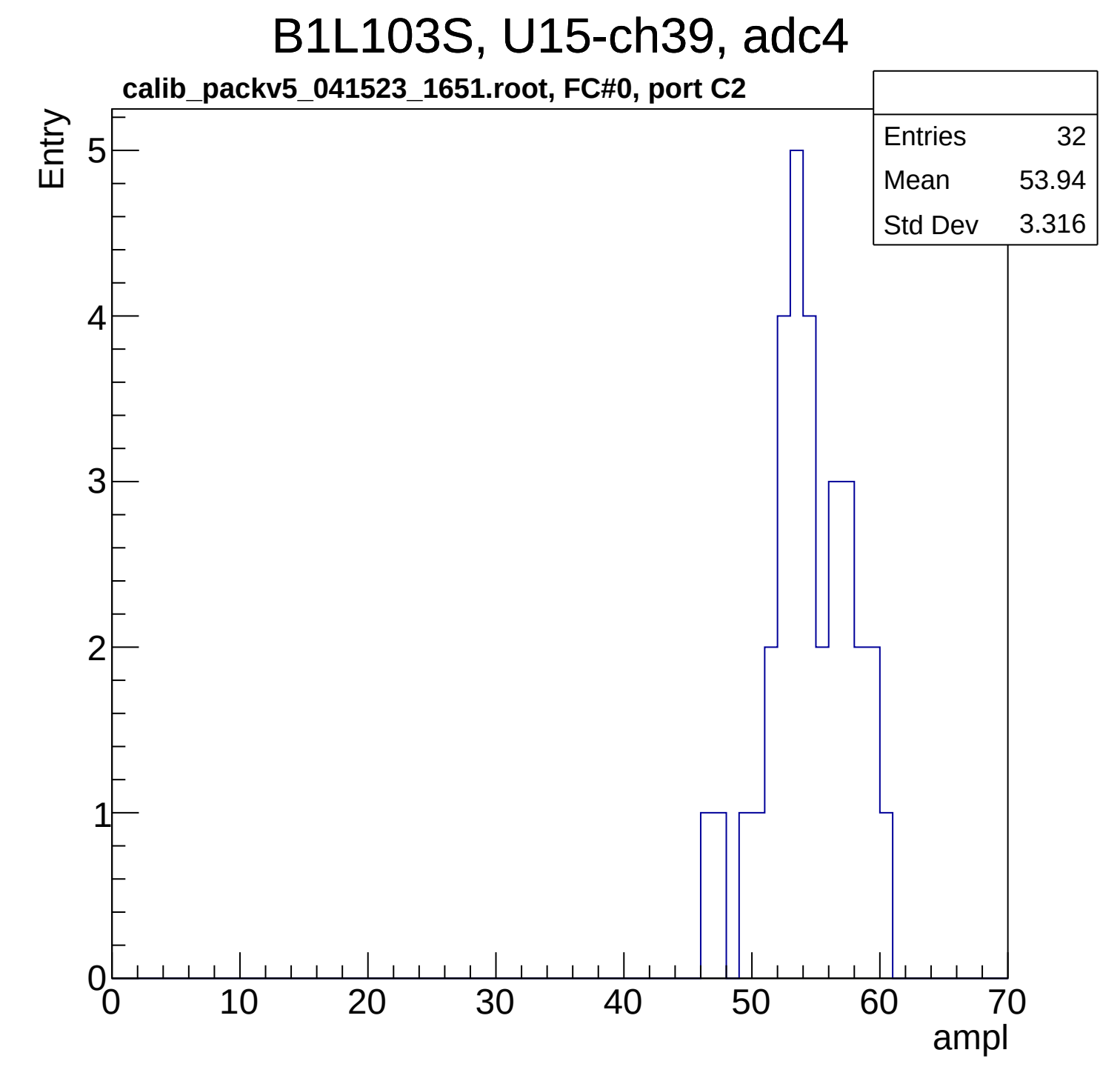

B1L103S, U15-ch38, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

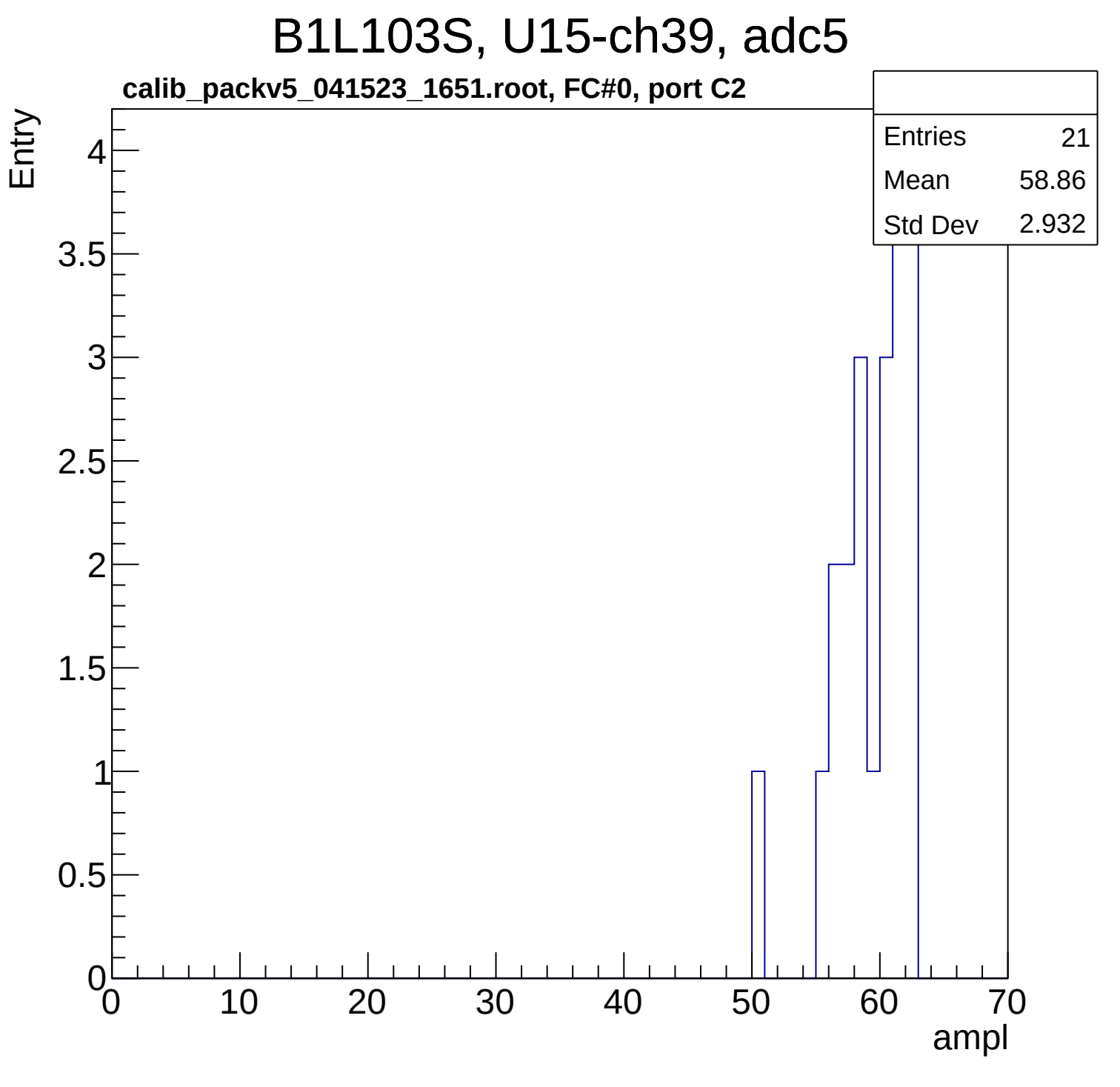

B1L103S, U15-ch39, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 22.67
Std Dev 12.44
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U15-ch39, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 32.68
Std Dev 11.74
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch39, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 37.26
Std Dev 13.47
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch39, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 47.67
Std Dev 3.898
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch39, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 53.94
Std Dev 3.316
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch39, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 58.86
Std Dev 2.932
Entry
ampl
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1
1.5
2
2.5
3
3.5
4
0
10
20
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40
50
60
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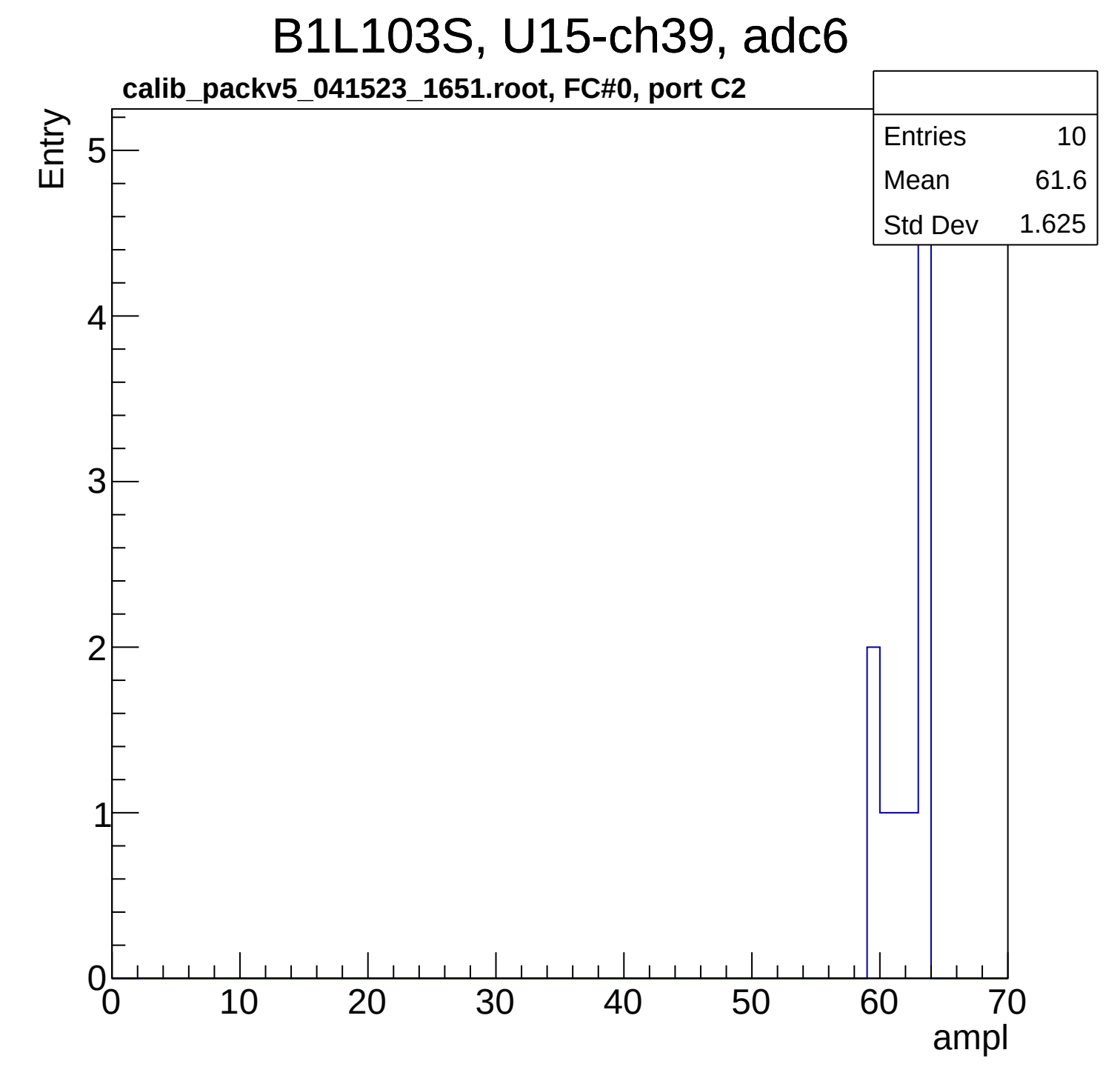
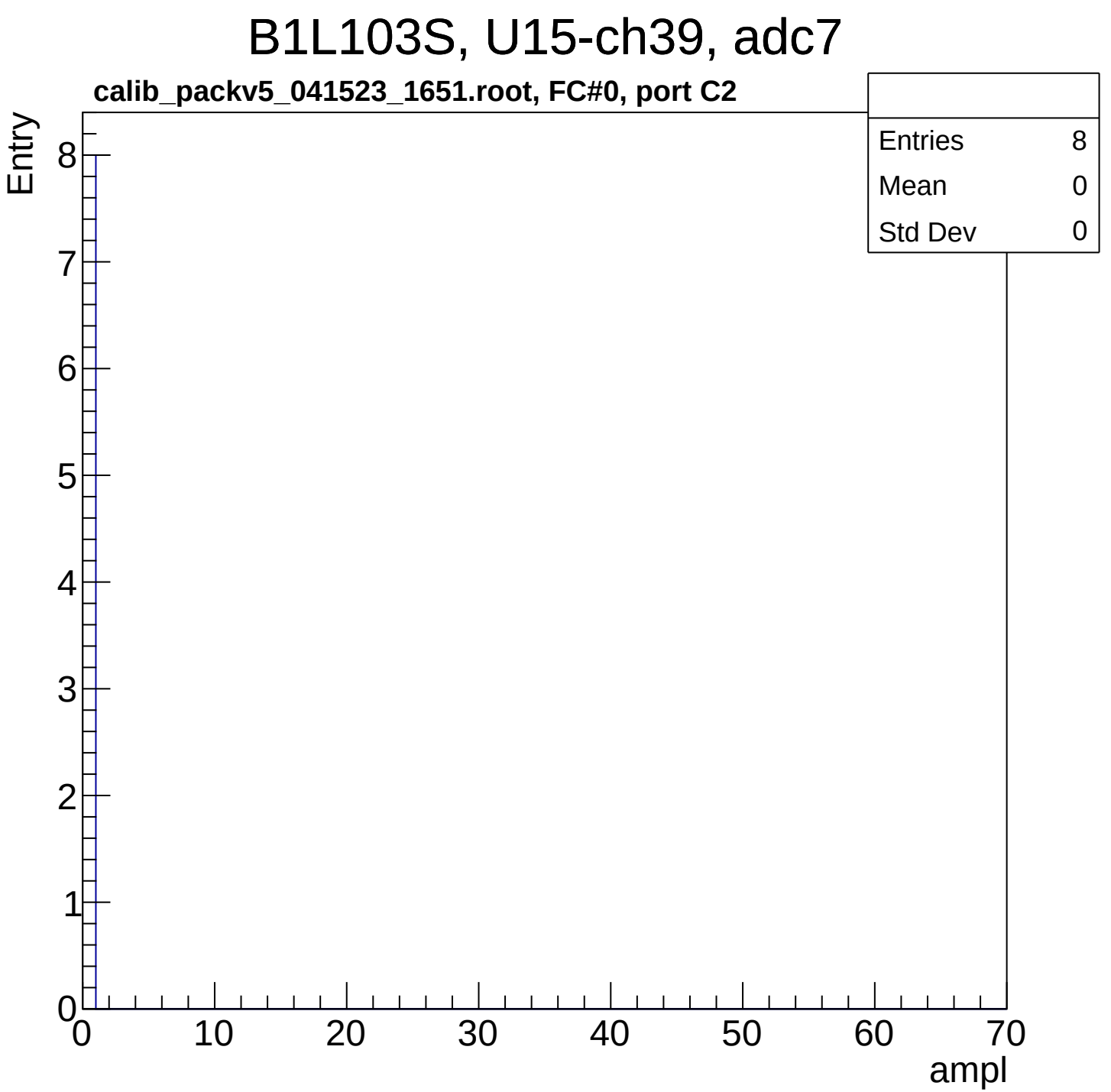
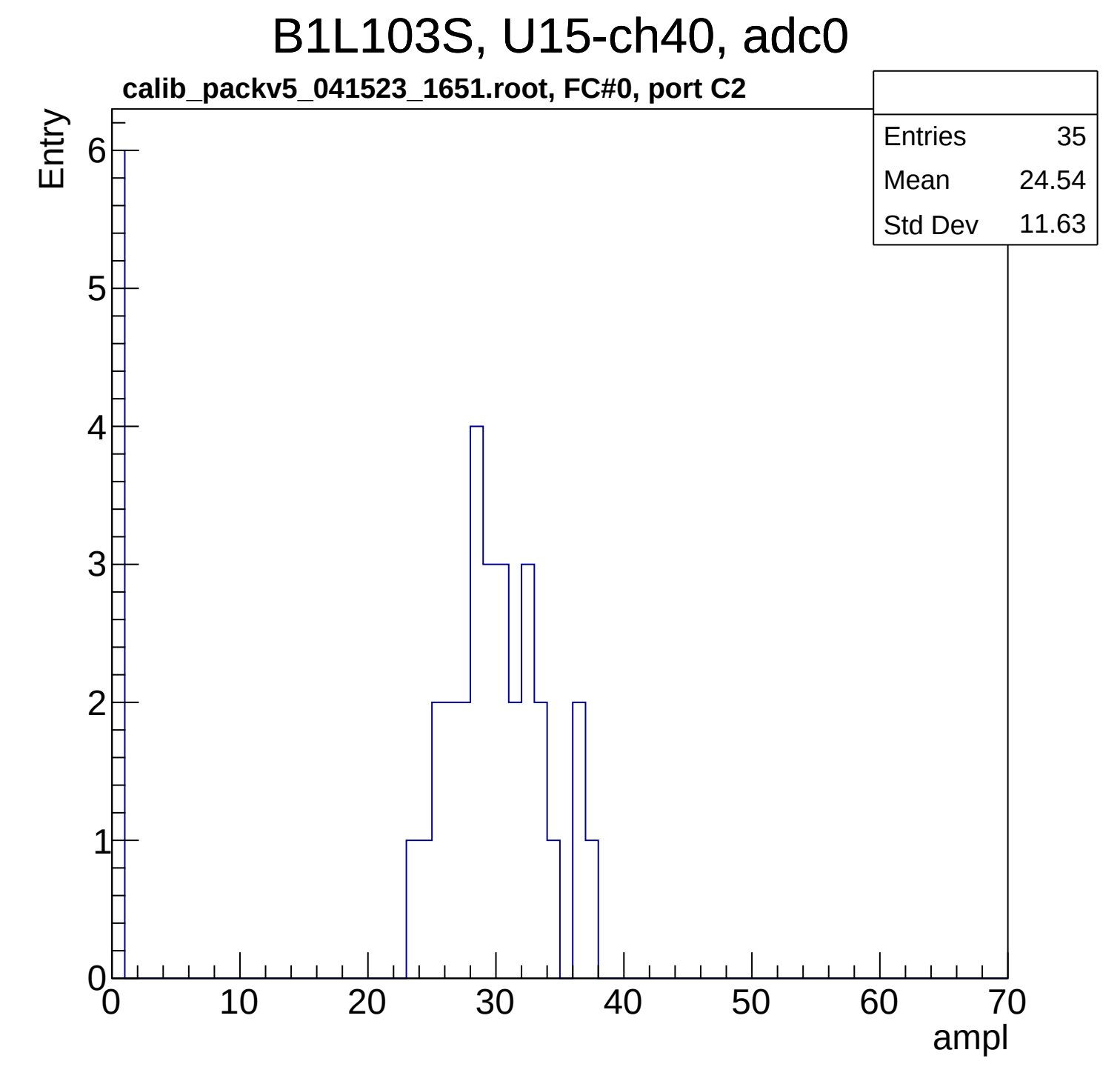
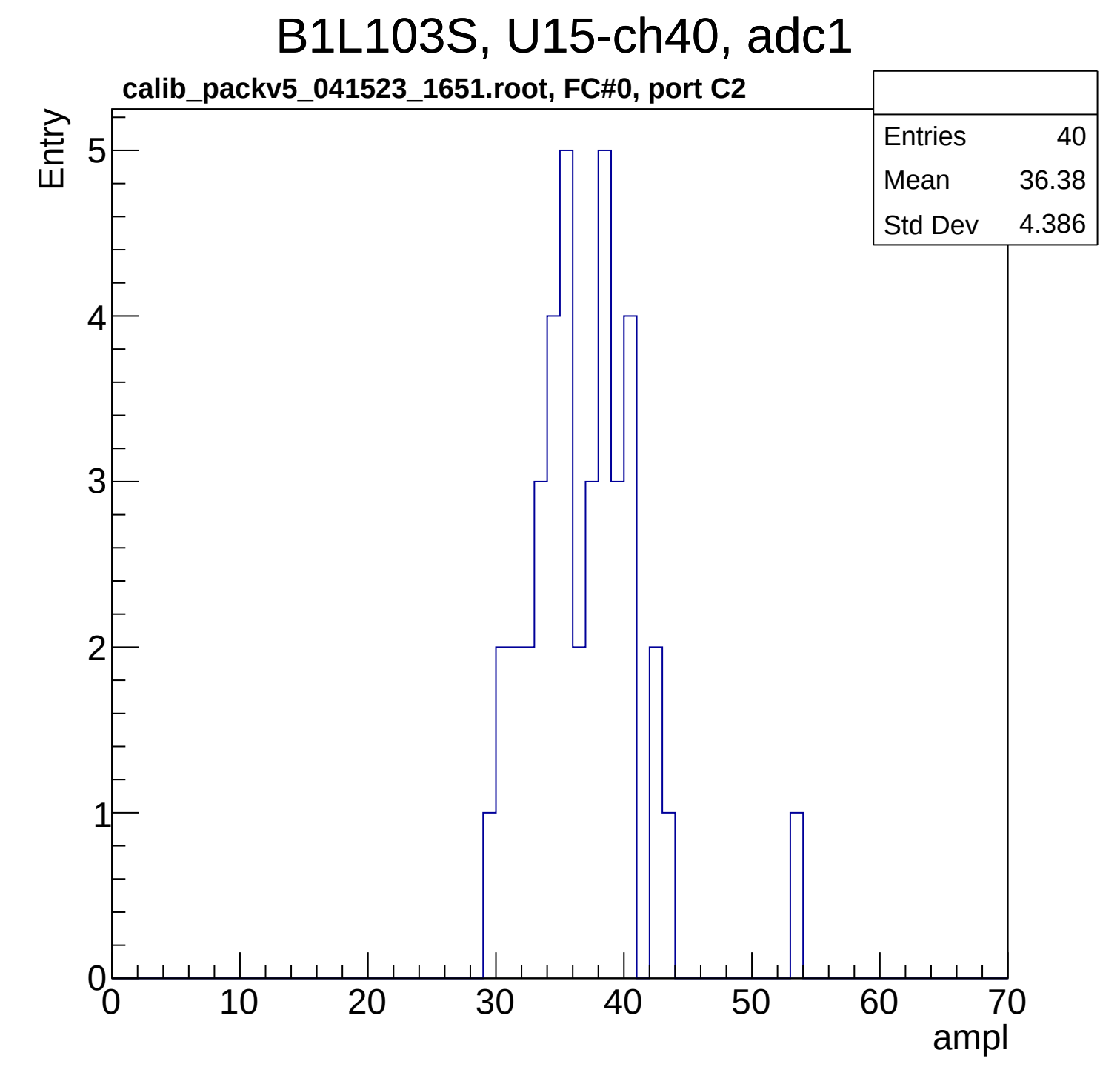
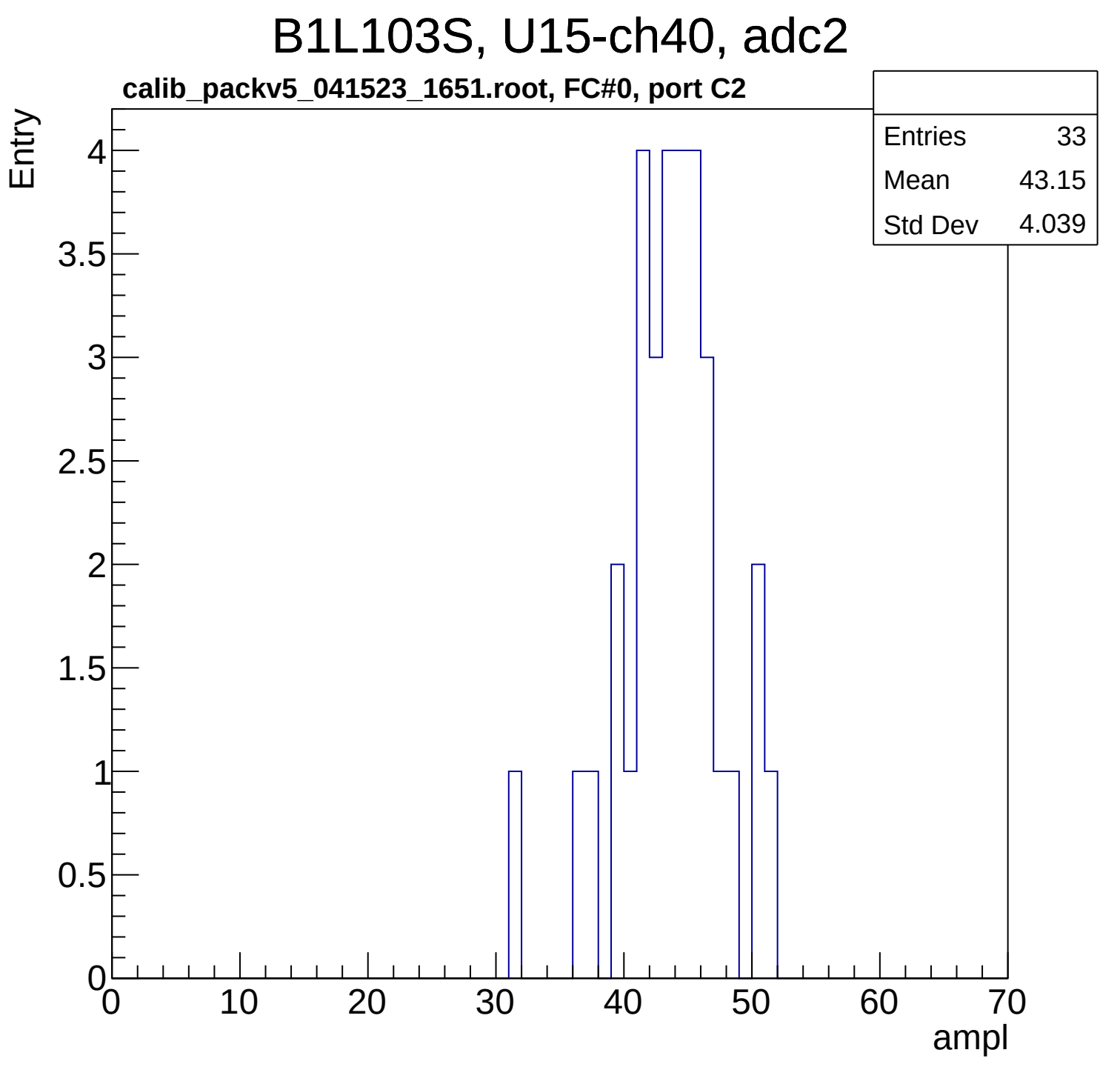

B1L103S, U15-ch39, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.6
Std Dev 1.625
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch39, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 0
Std Dev 0
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch40, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 24.54
Std Dev 11.63
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U15-ch40, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 36.38
Std Dev 4.386
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch40, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 43.15
Std Dev 4.039
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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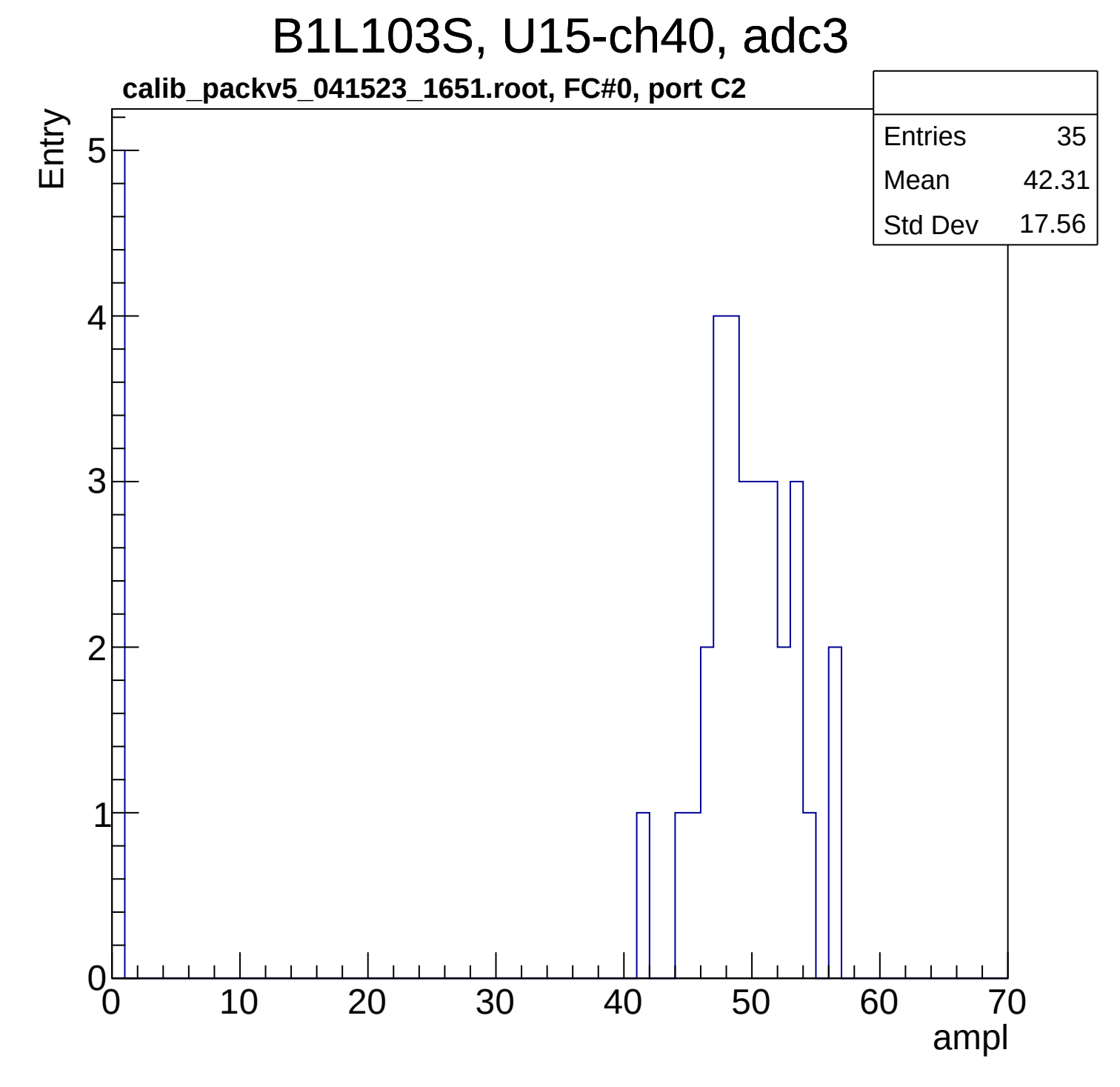
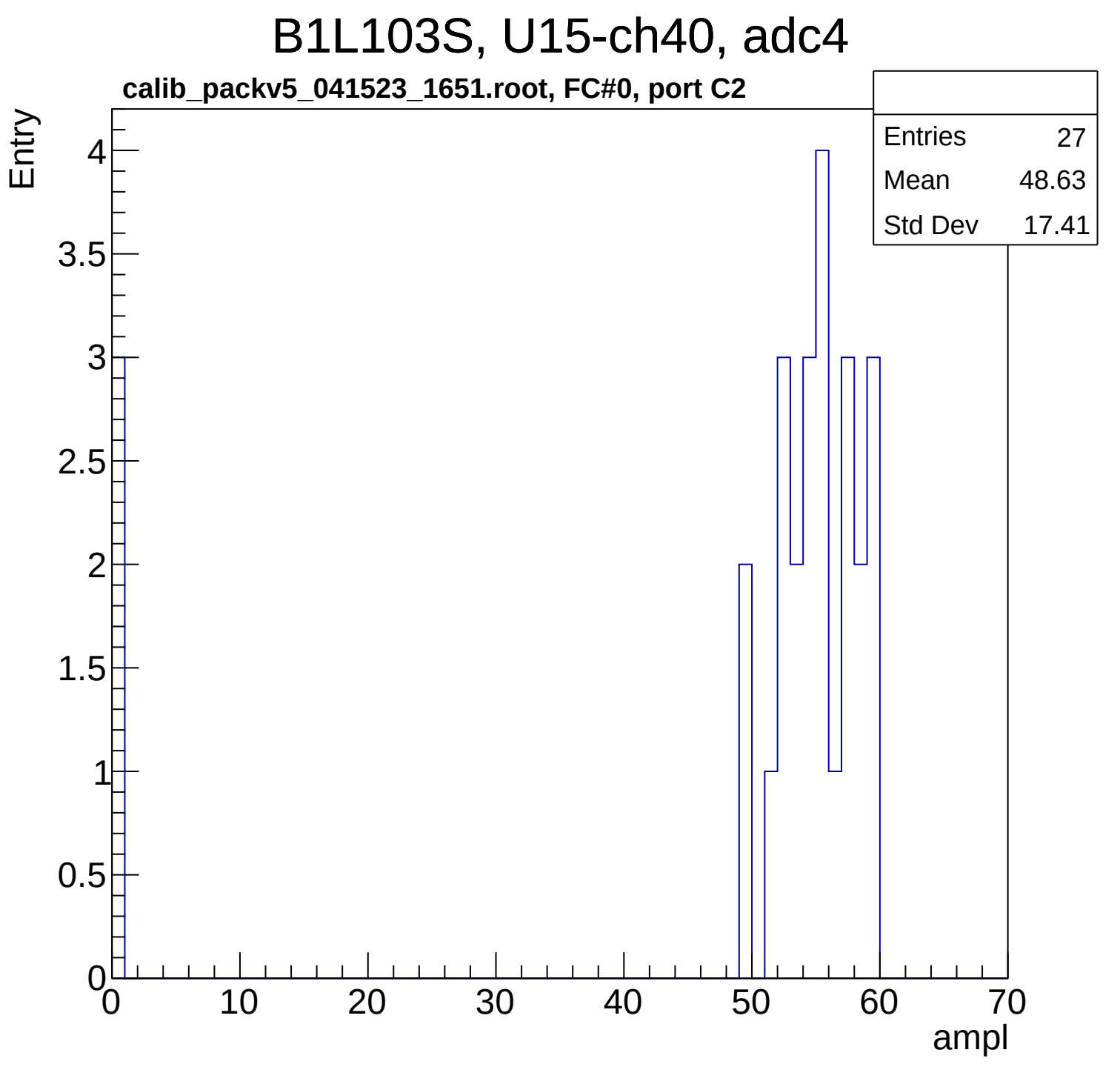

B1L103S, U15-ch40, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 42.31
Std Dev 17.56
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch40, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 48.63
Std Dev 17.41
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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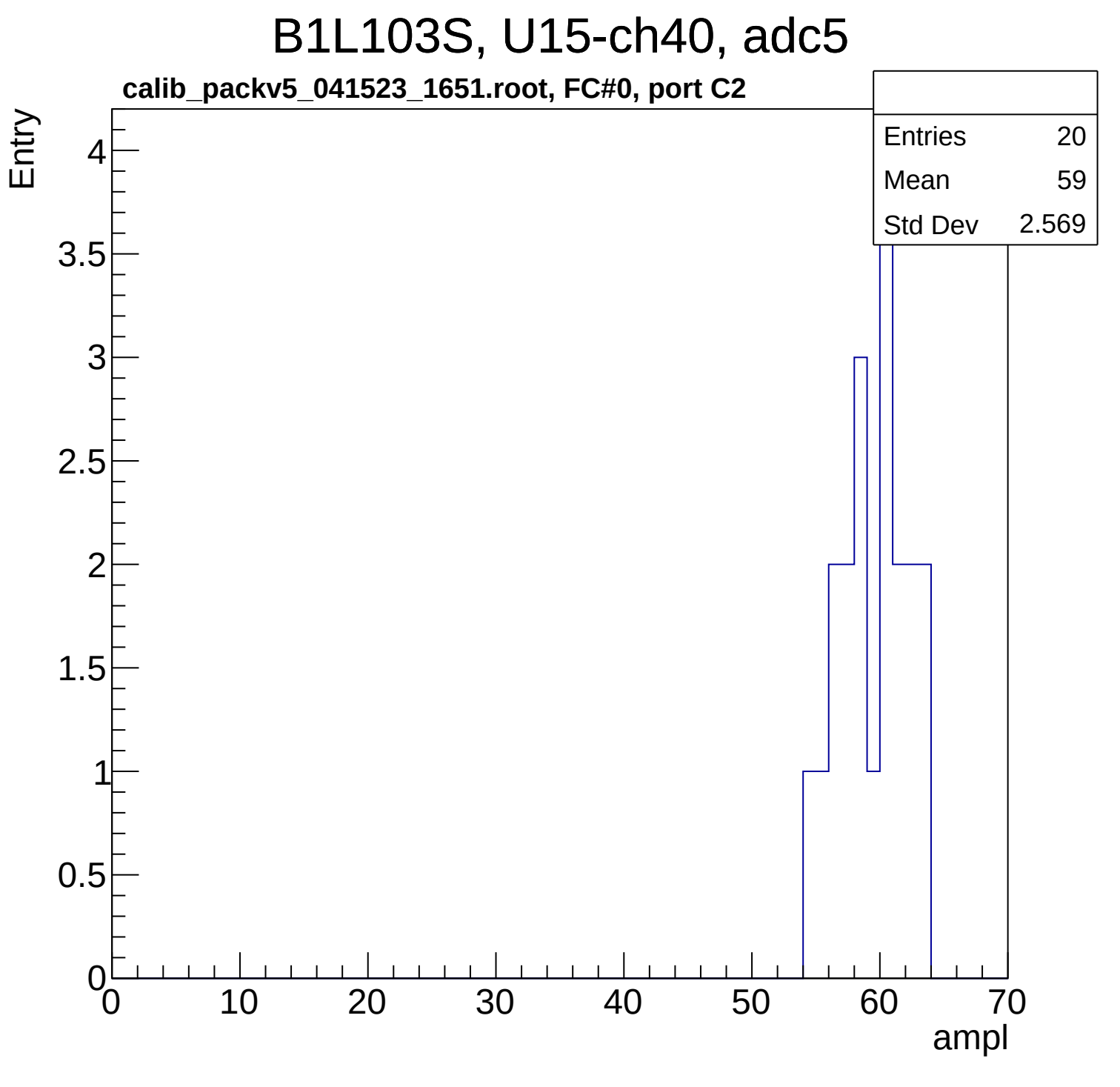
B1L103S, U15-ch40, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 59
Std Dev 2.569
Entry
ampl
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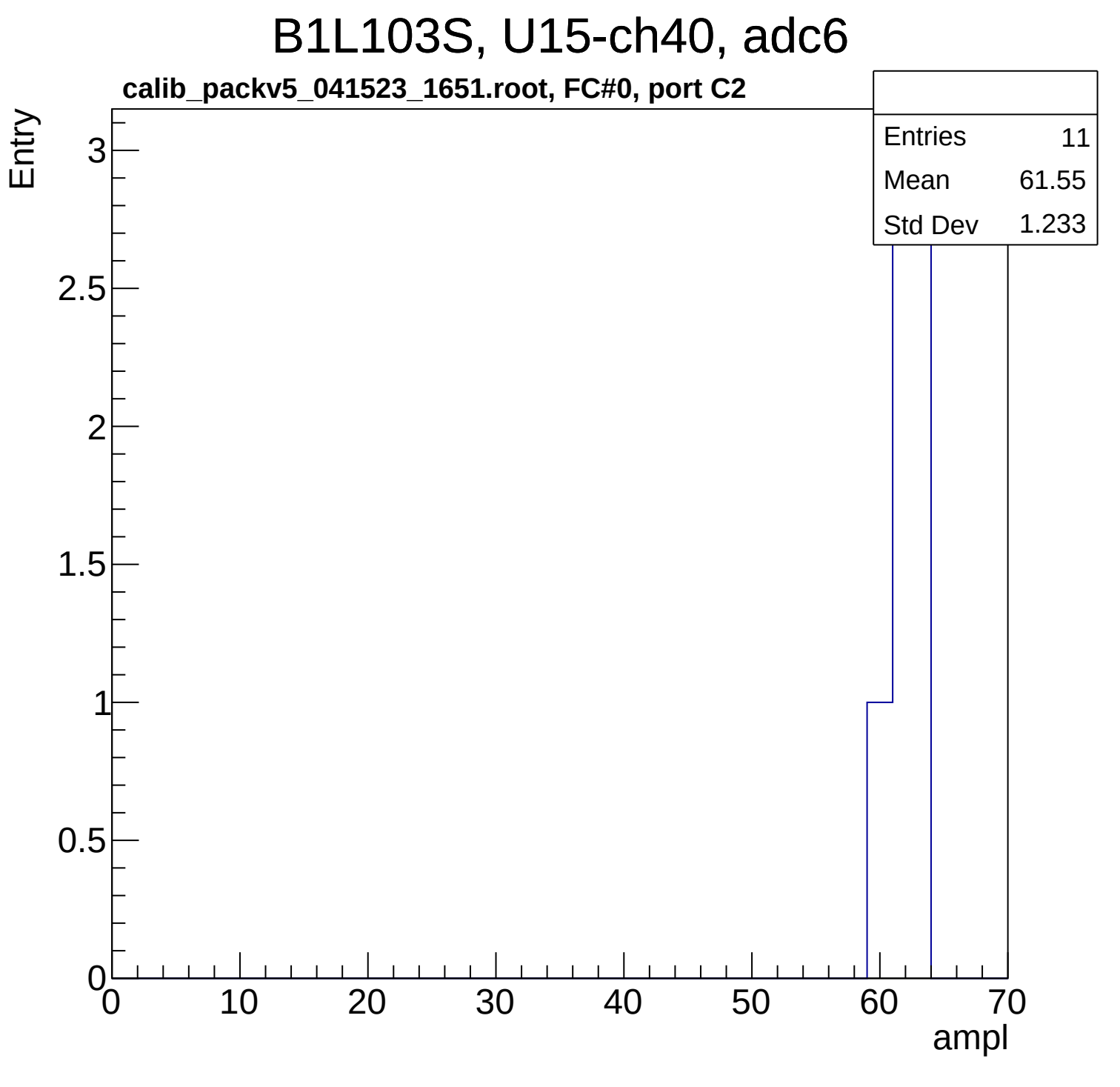
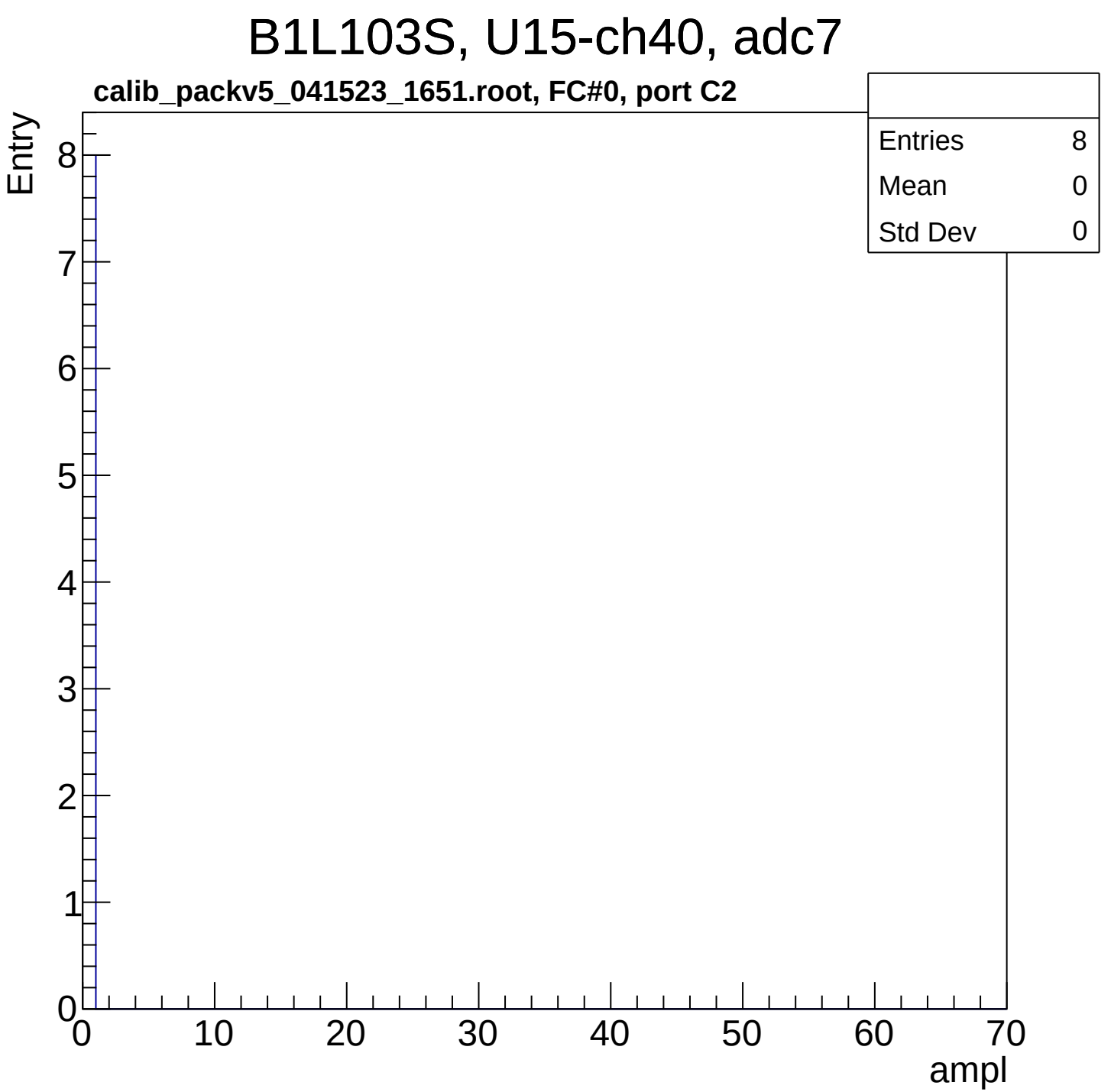
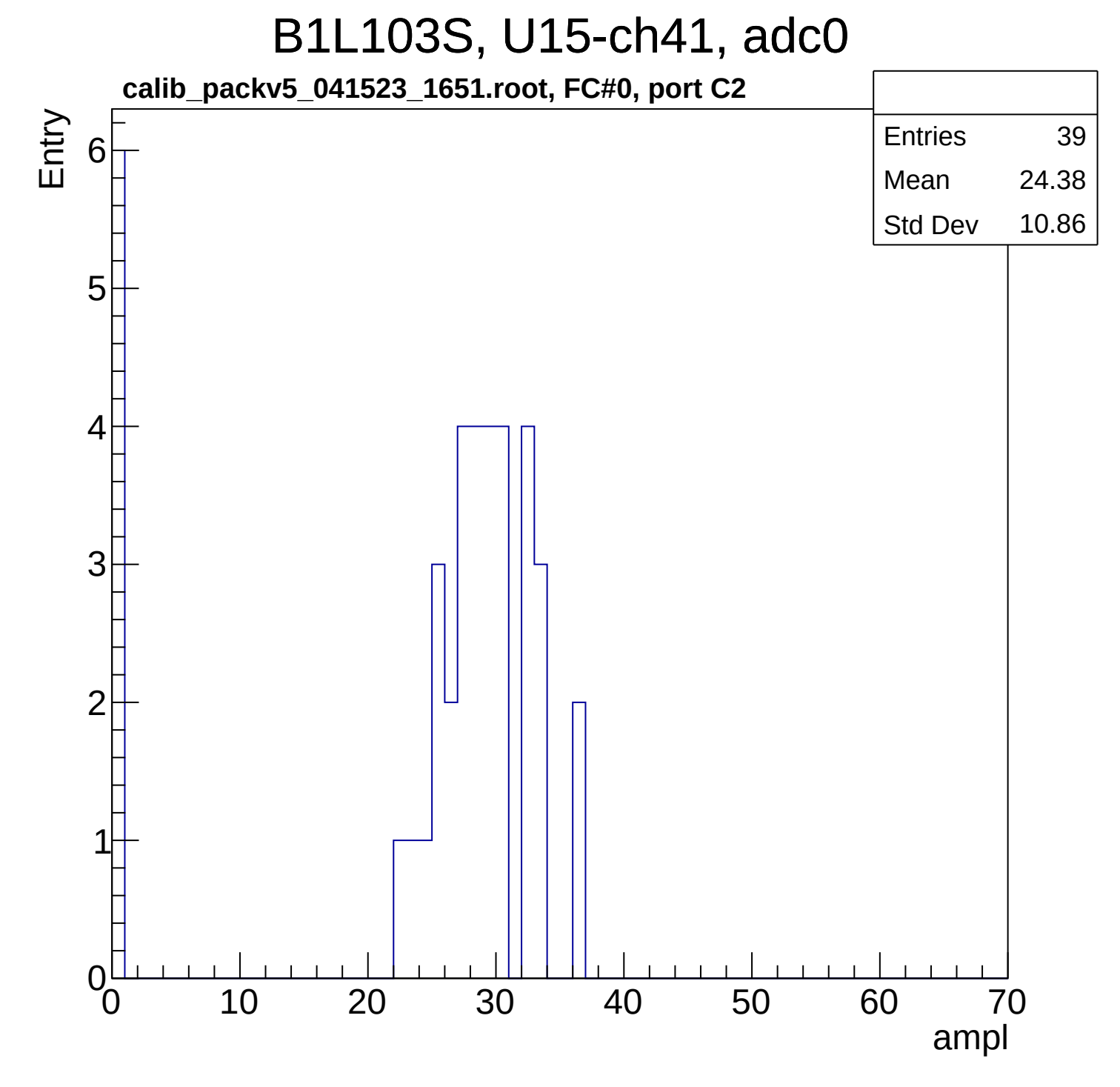
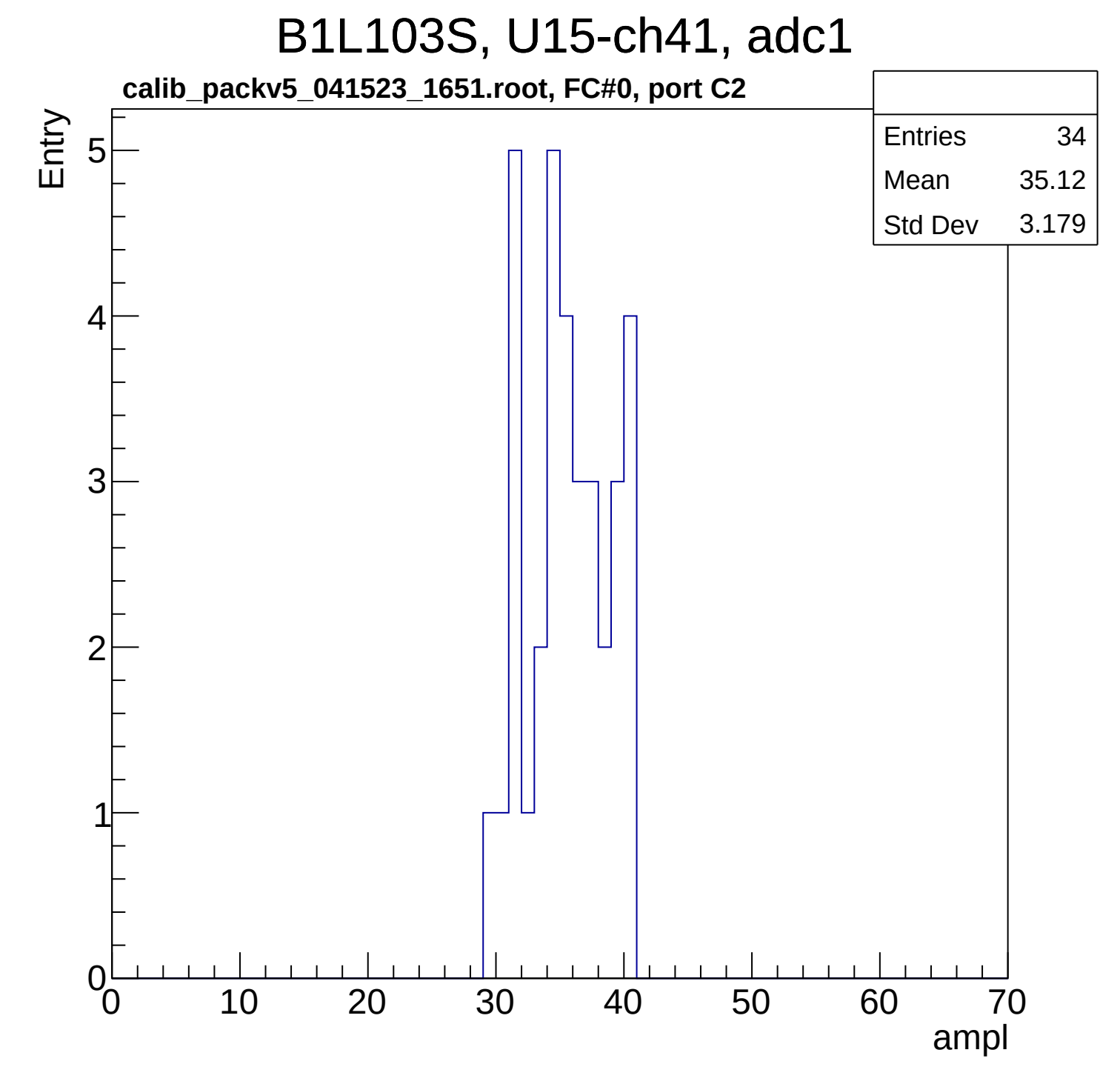
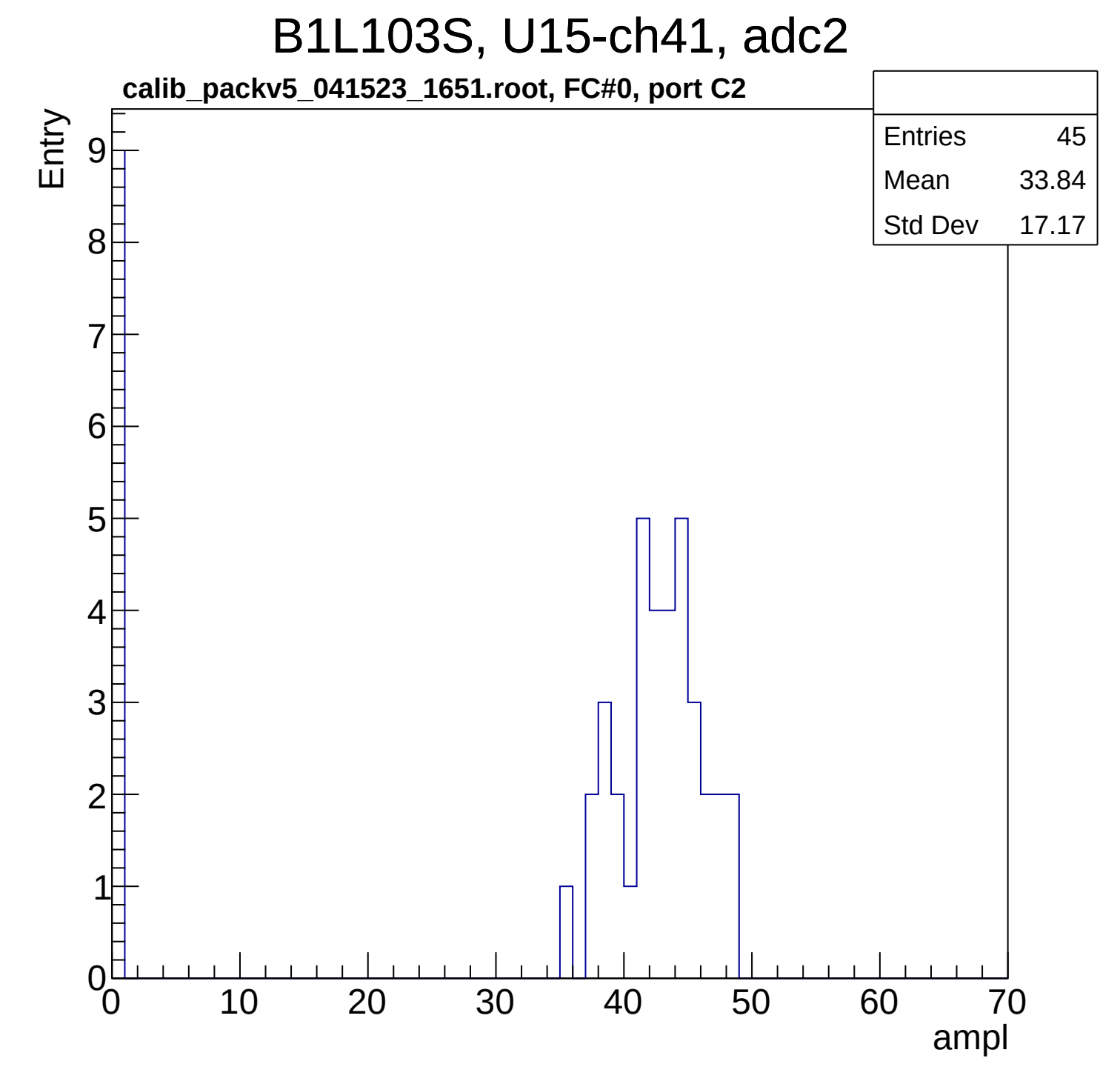
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

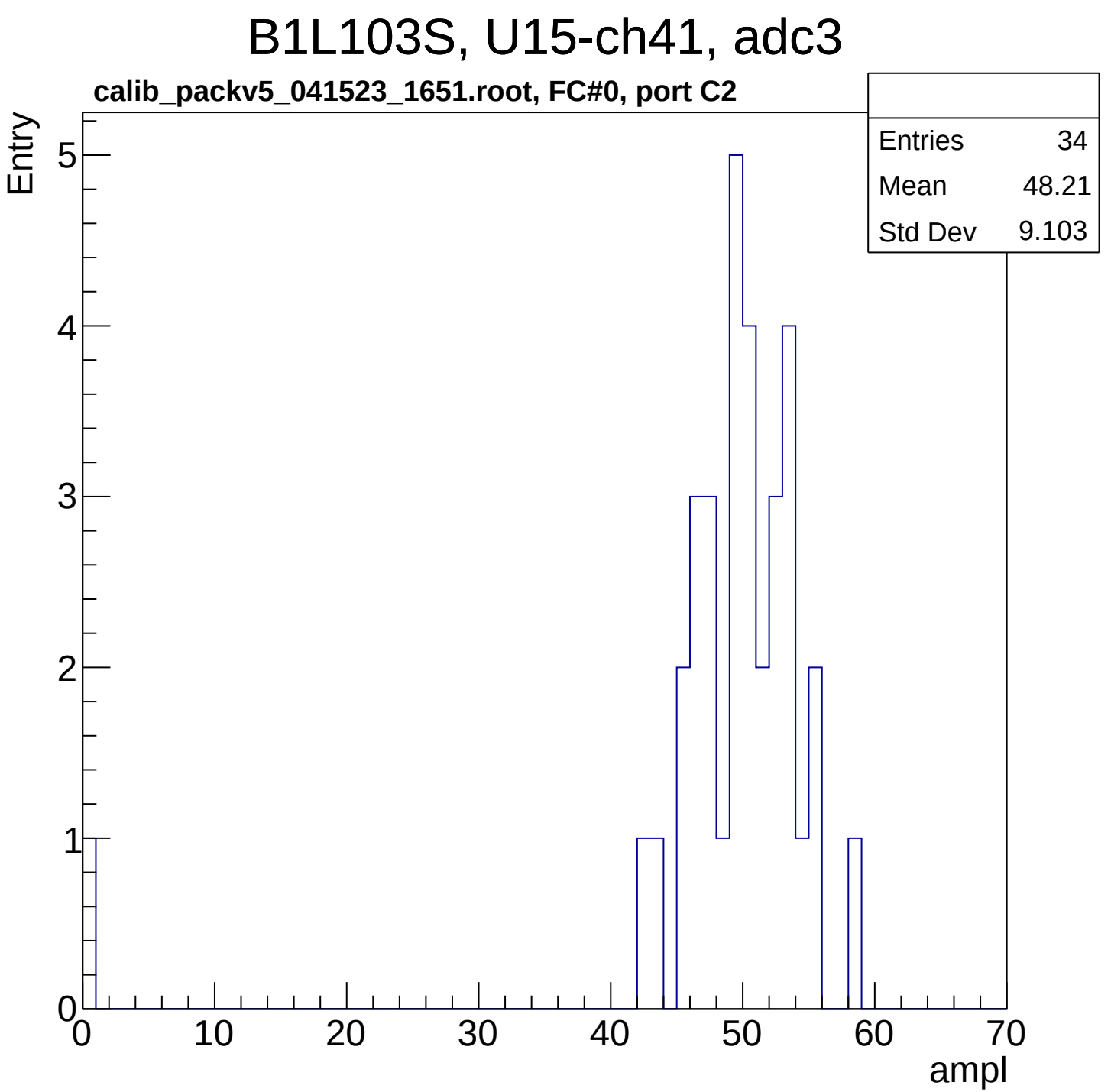

B1L103S, U15-ch40, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.55
Std Dev 1.233
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

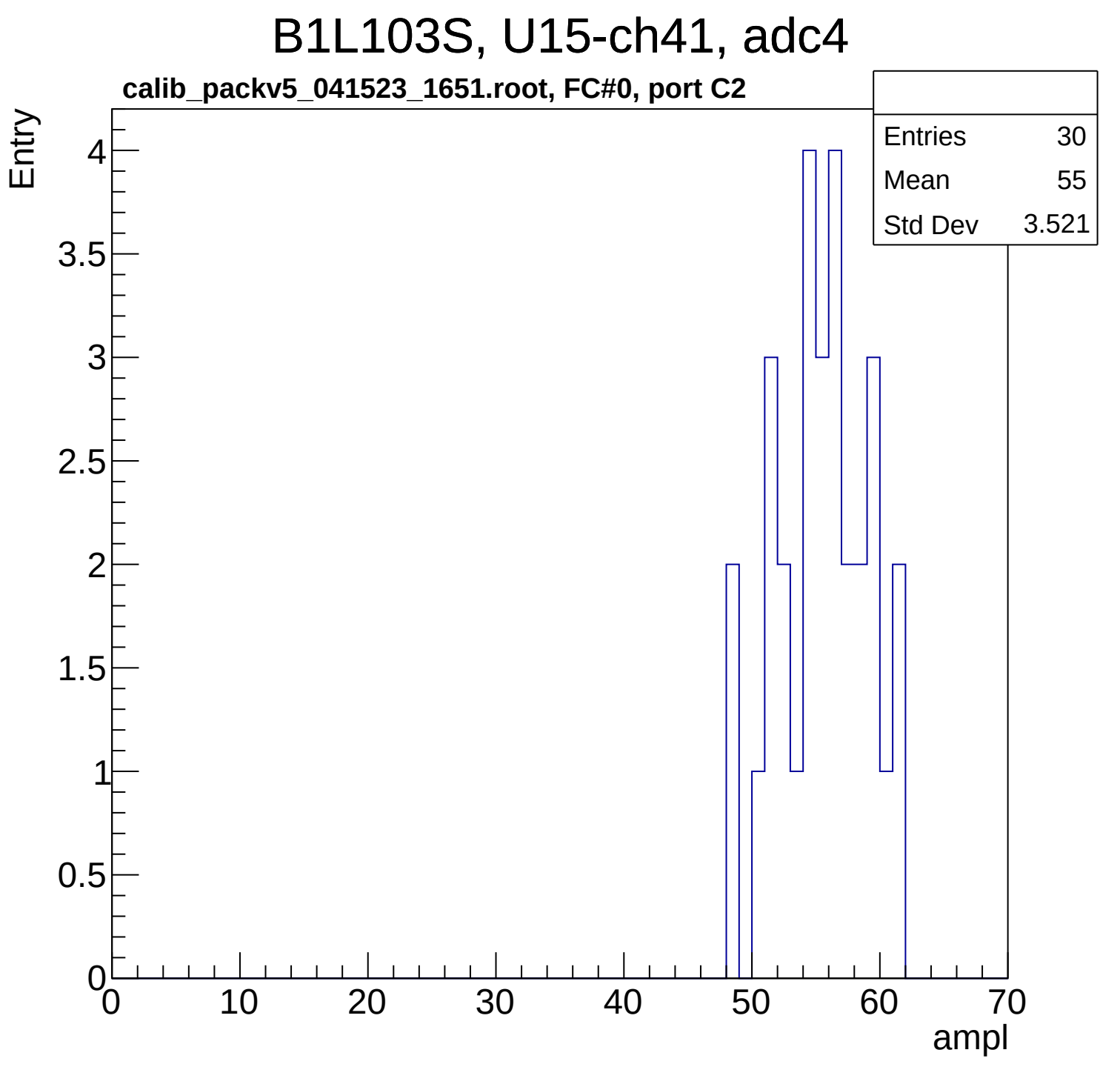

B1L103S, U15-ch40, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 0
Std Dev 0
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch41, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 24.38
Std Dev 10.86
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U15-ch41, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 35.12
Std Dev 3.179
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch41, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 33.84
Std Dev 17.17
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U15-ch41, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 48.21
Std Dev 9.103
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch41, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 55
Std Dev 3.521
Entry
ampl
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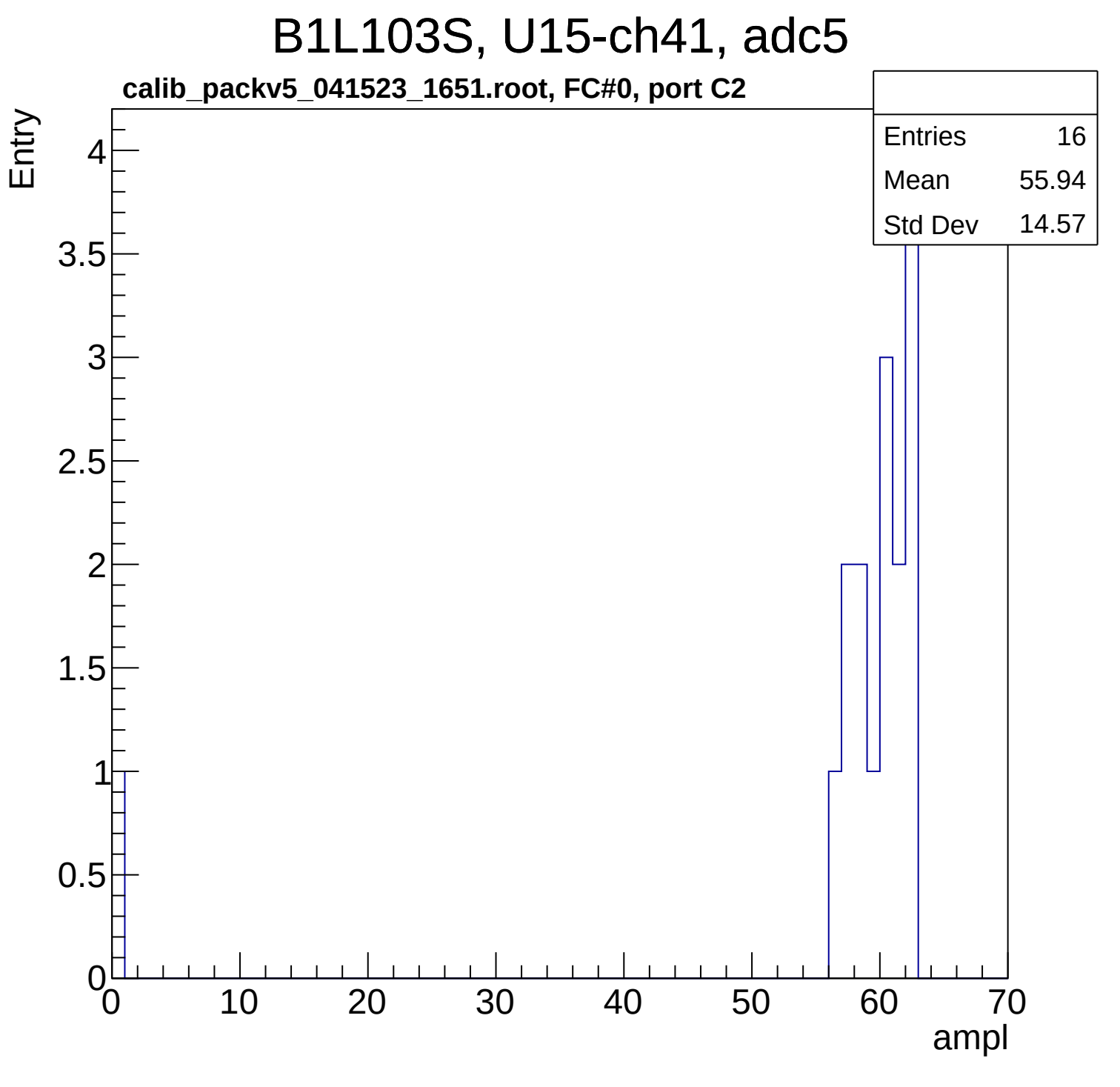
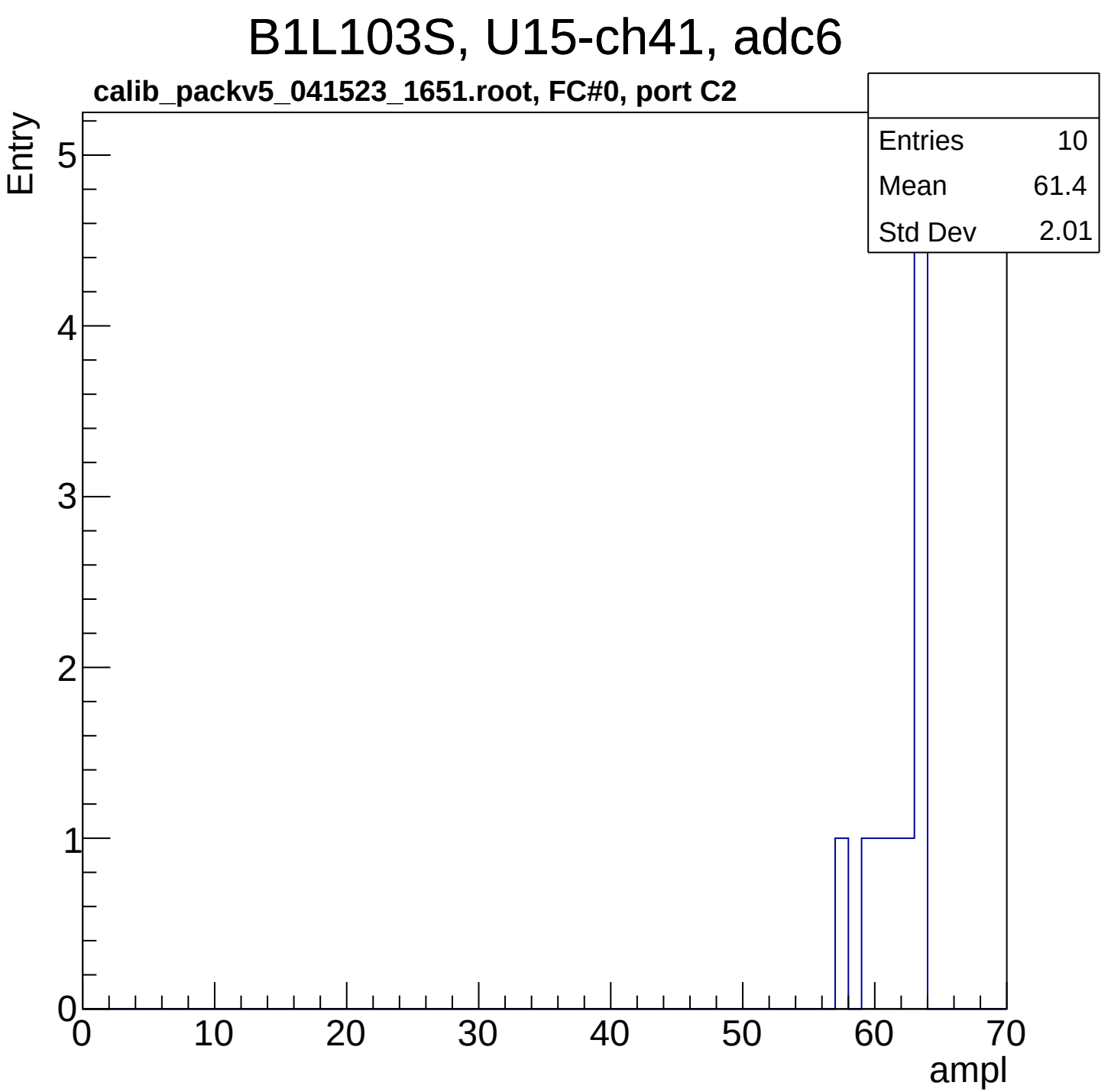
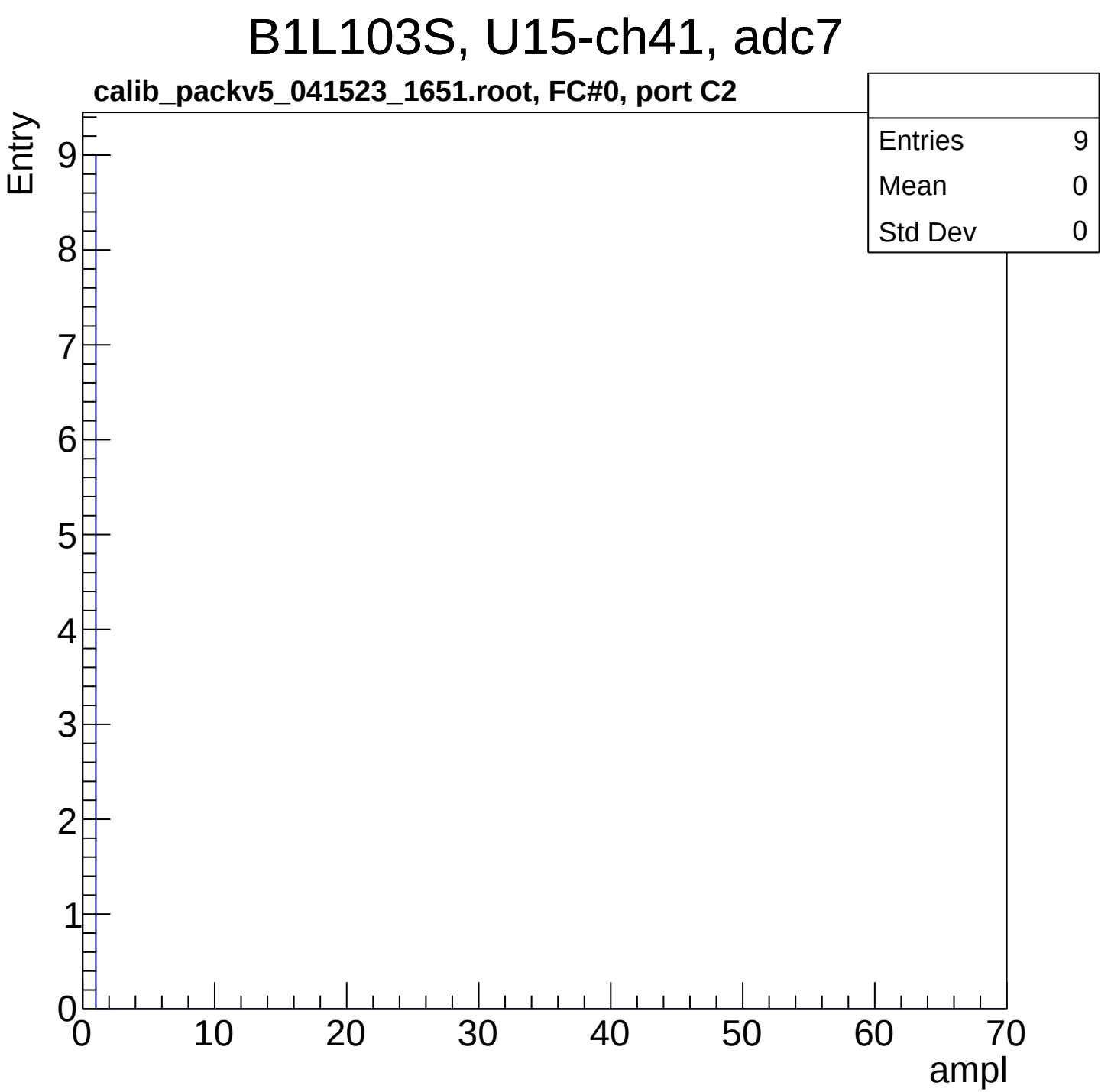
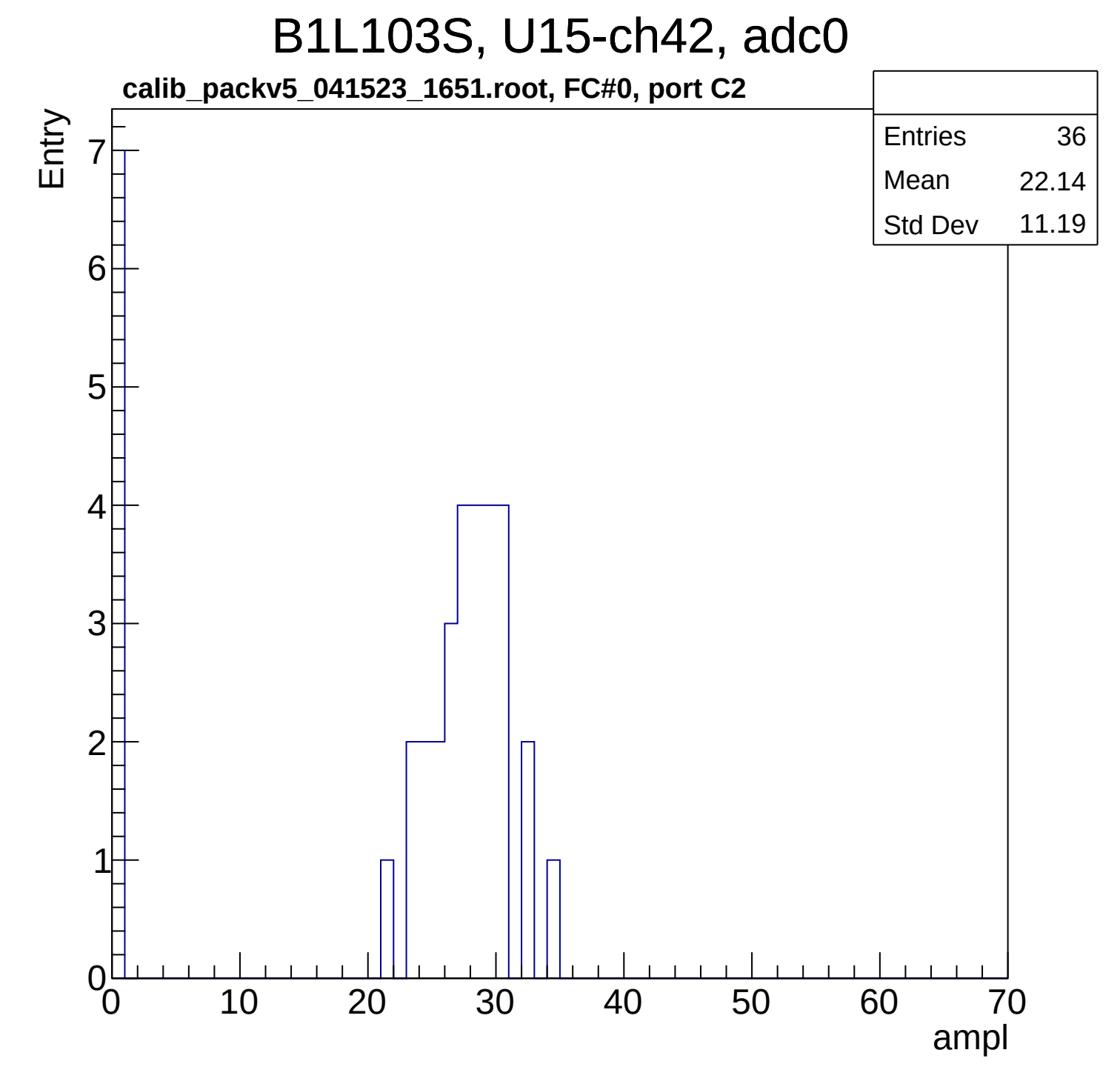
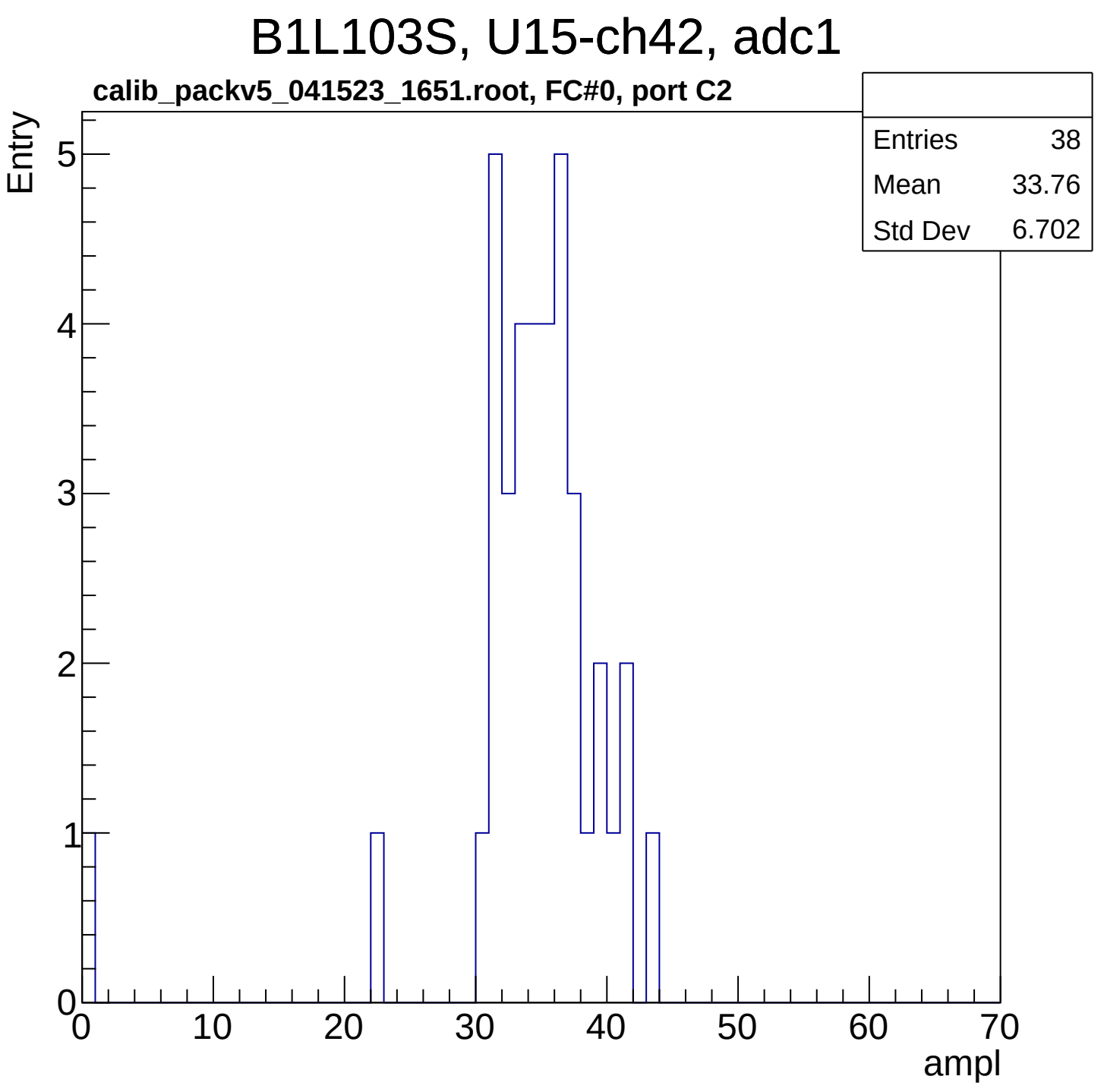
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

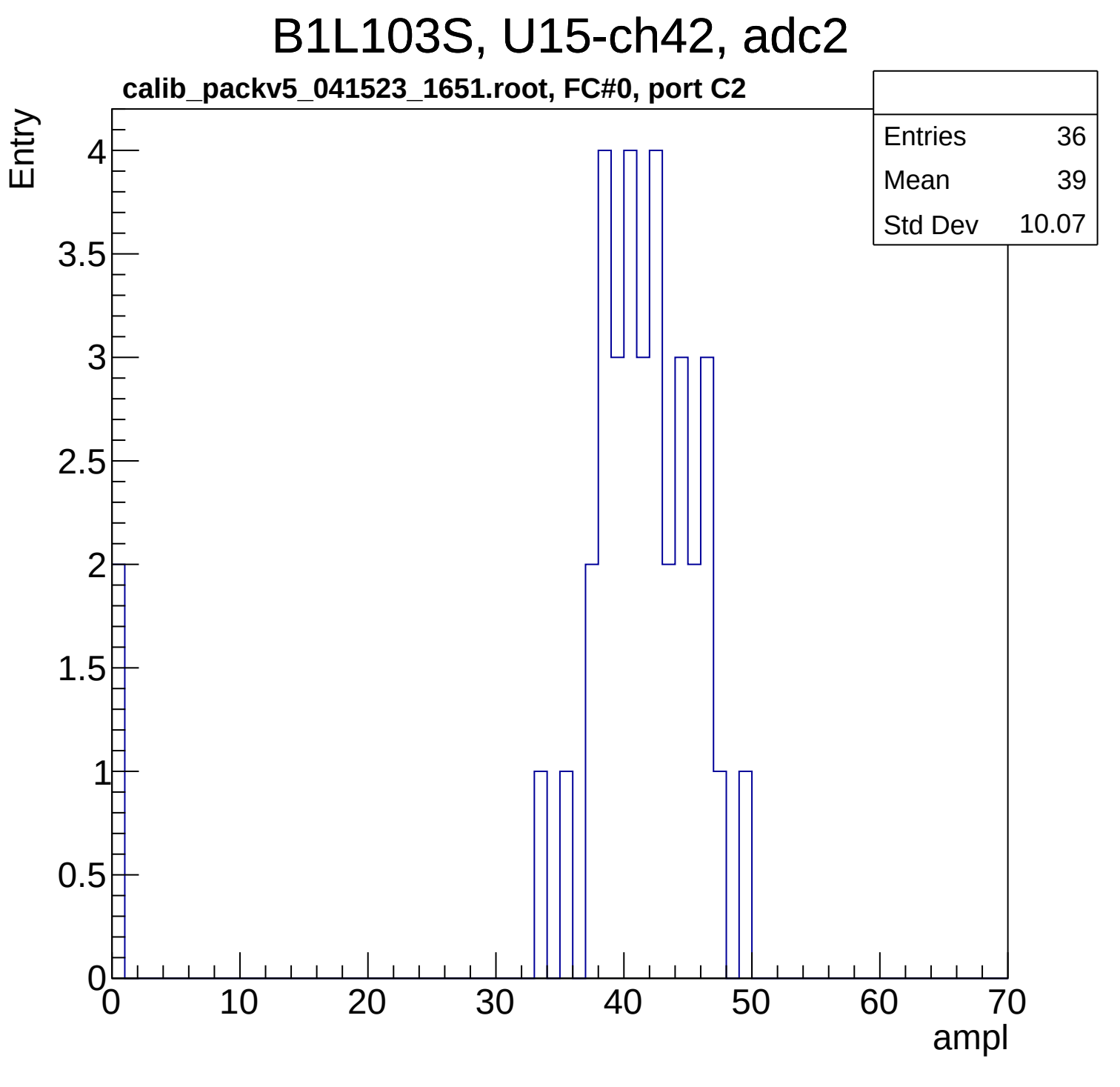

B1L103S, U15-ch41, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 55.94
Std Dev 14.57
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

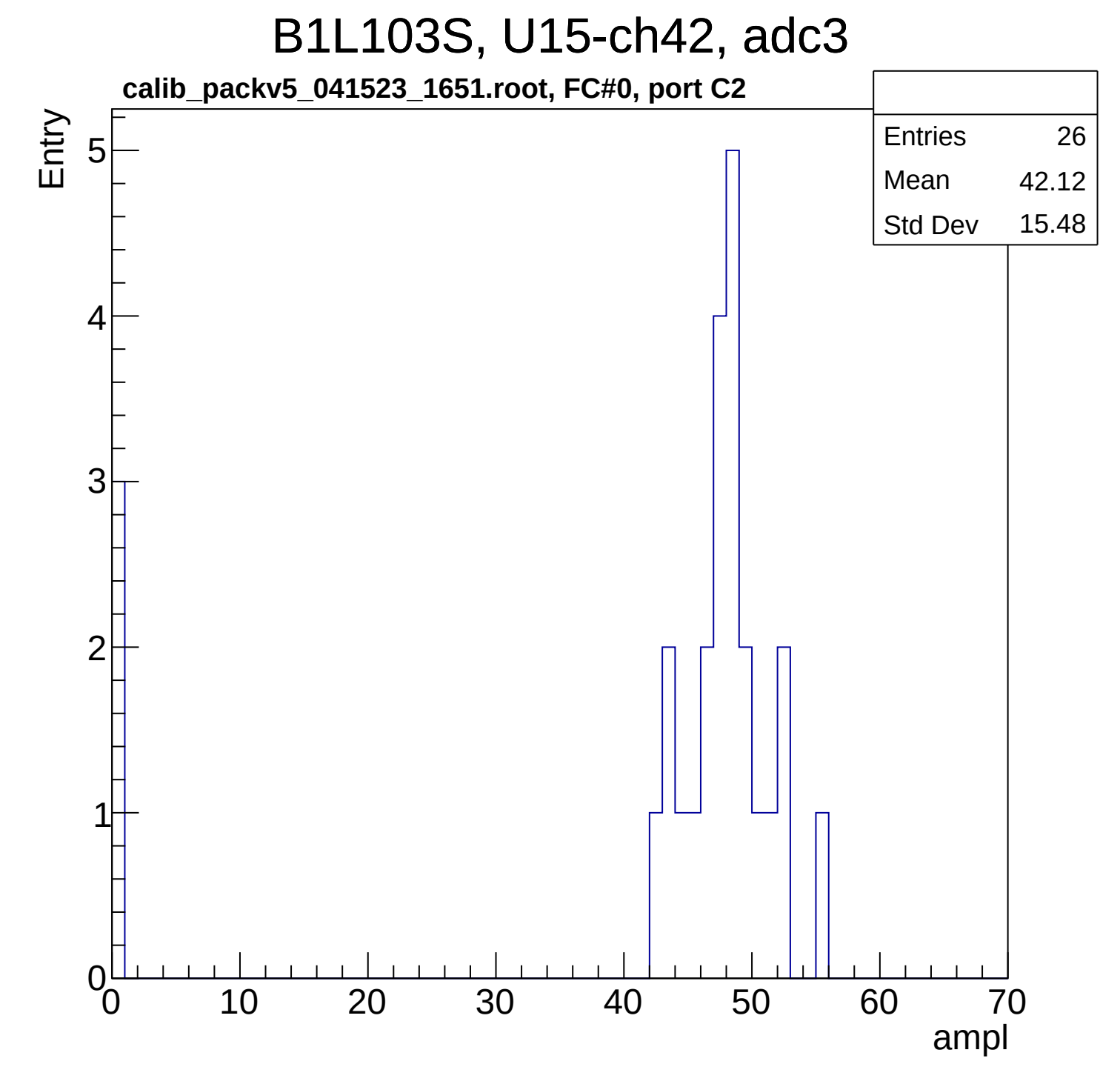

B1L103S, U15-ch41, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.4
Std Dev 2.01
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

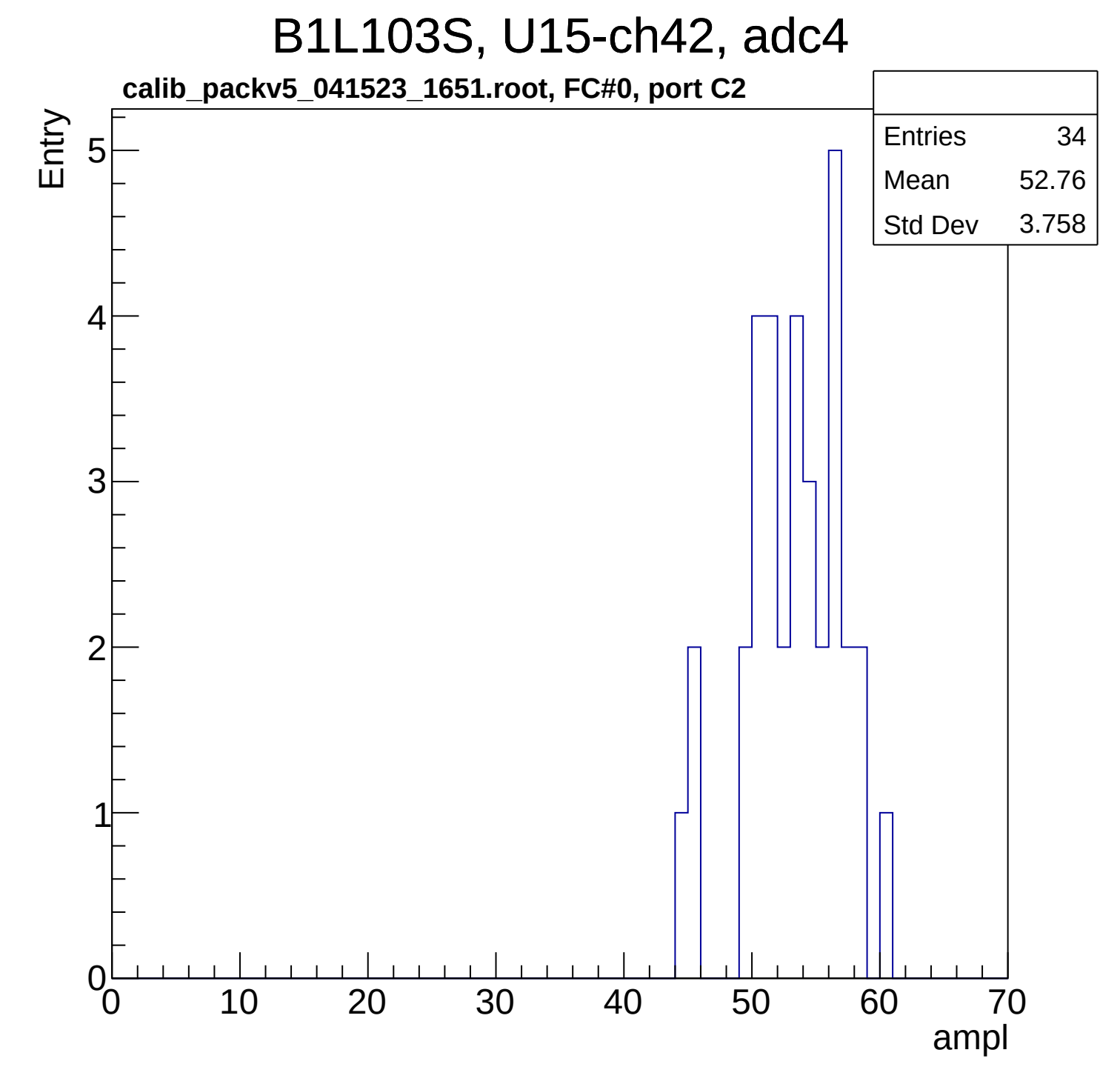

B1L103S, U15-ch41, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 0
Std Dev 0
Entry
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70
ampl

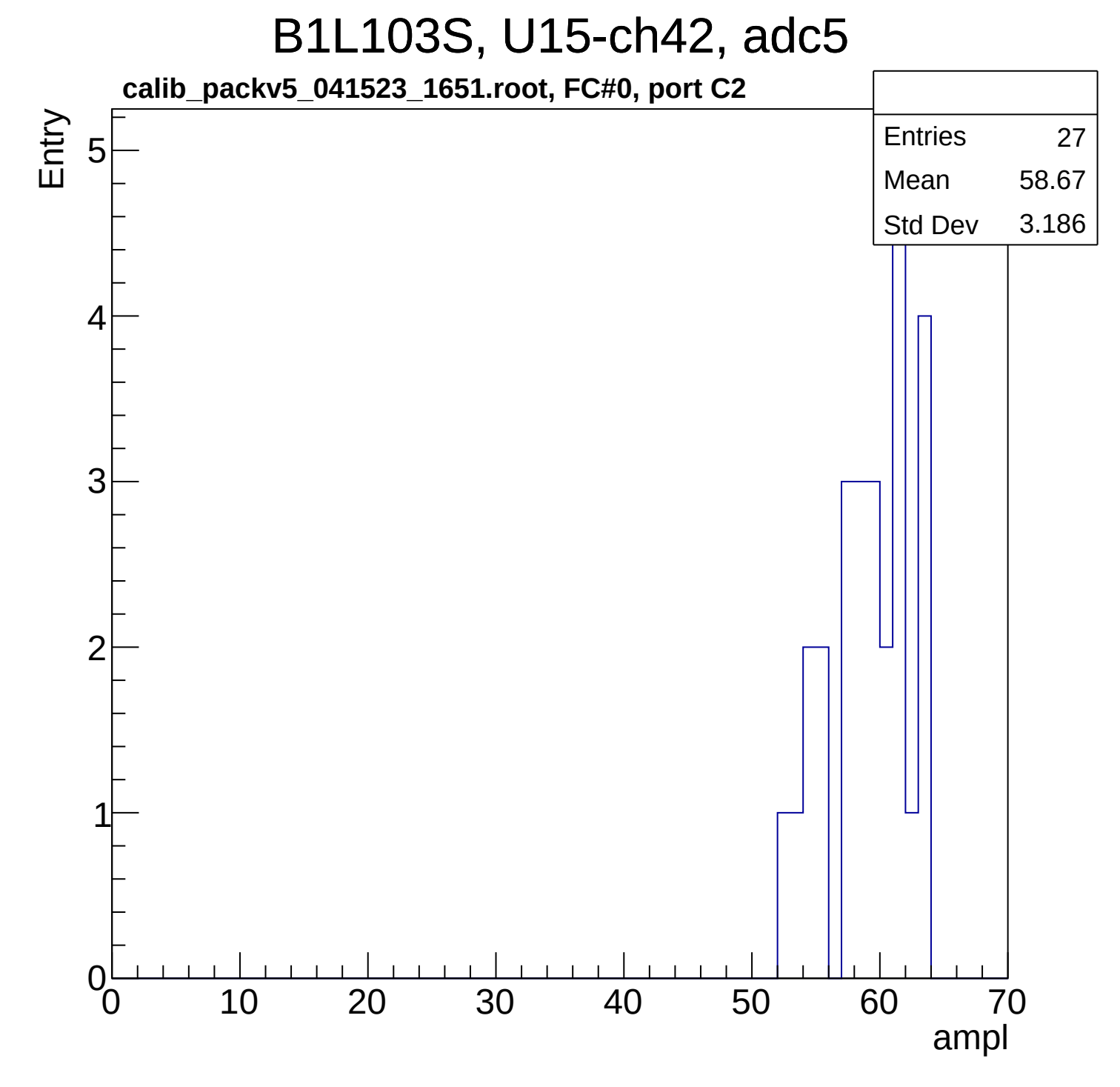

B1L103S, U15-ch42, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 22.14
Std Dev 11.19
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

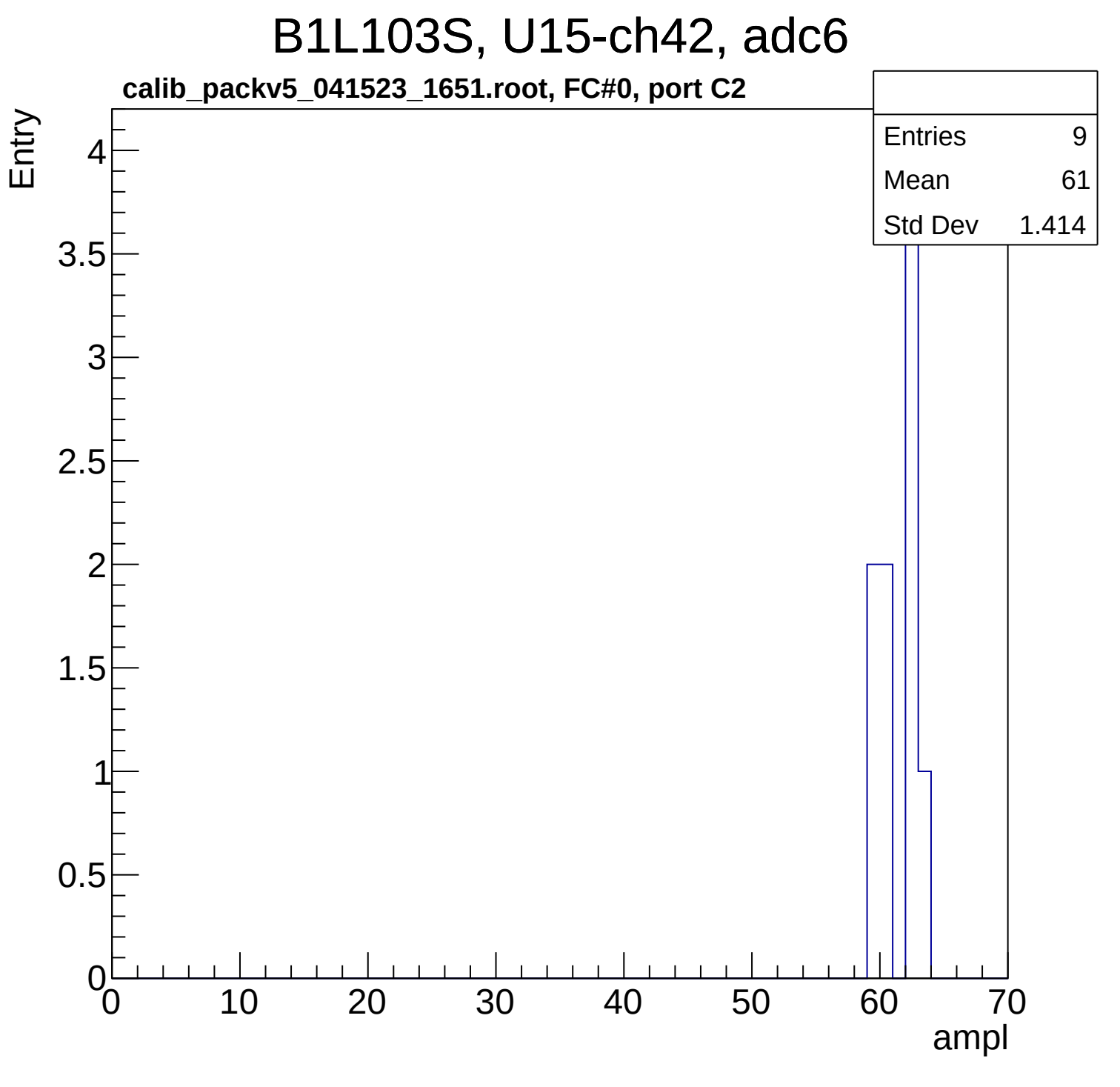

B1L103S, U15-ch42, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 33.76
Std Dev 6.702
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch42, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 39
Std Dev 10.07
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch42, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 42.12
Std Dev 15.48
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch42, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 52.76
Std Dev 3.758
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch42, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 58.67
Std Dev 3.186
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch42, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61
Std Dev 1.414
Entry
ampl
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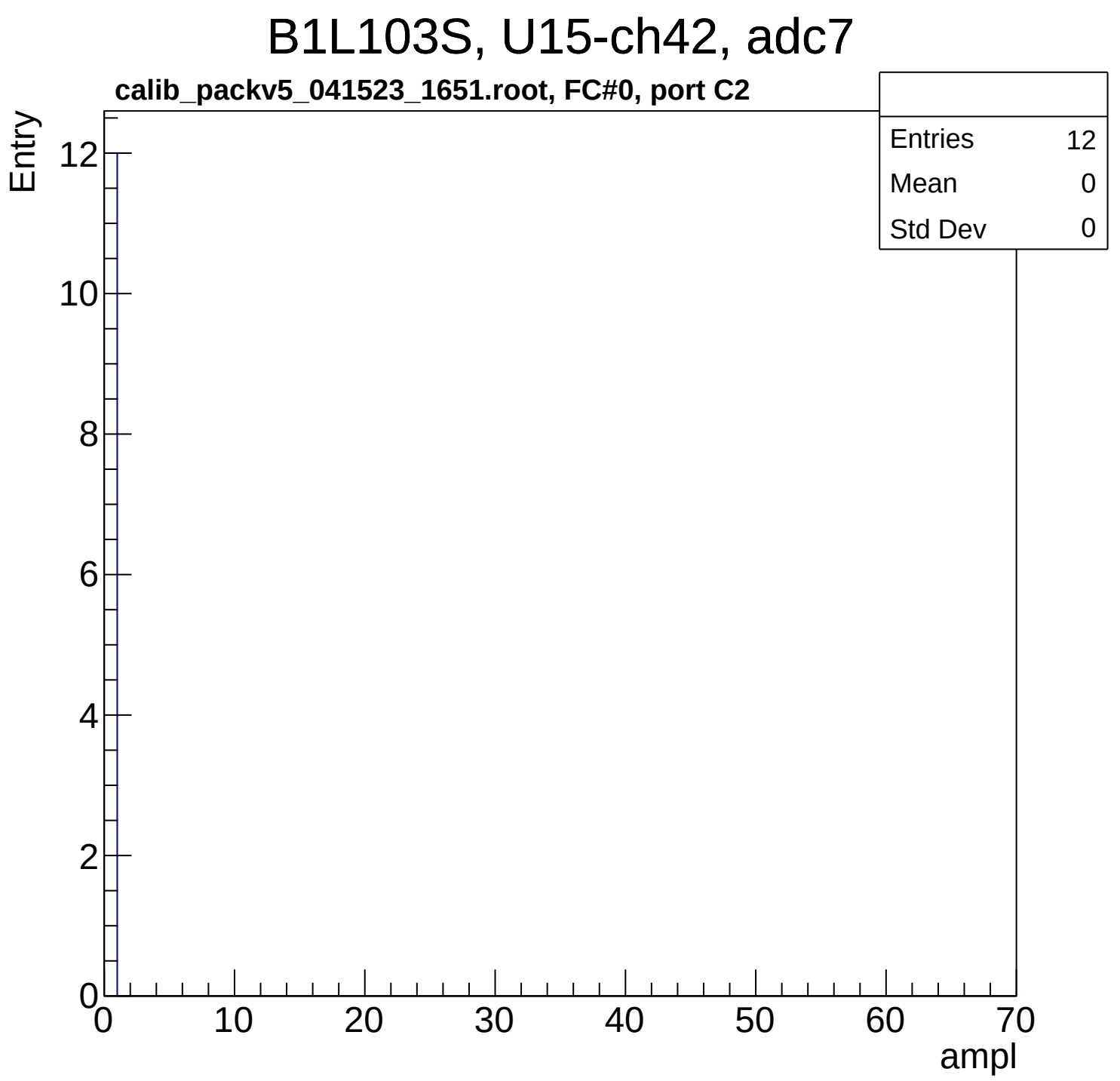
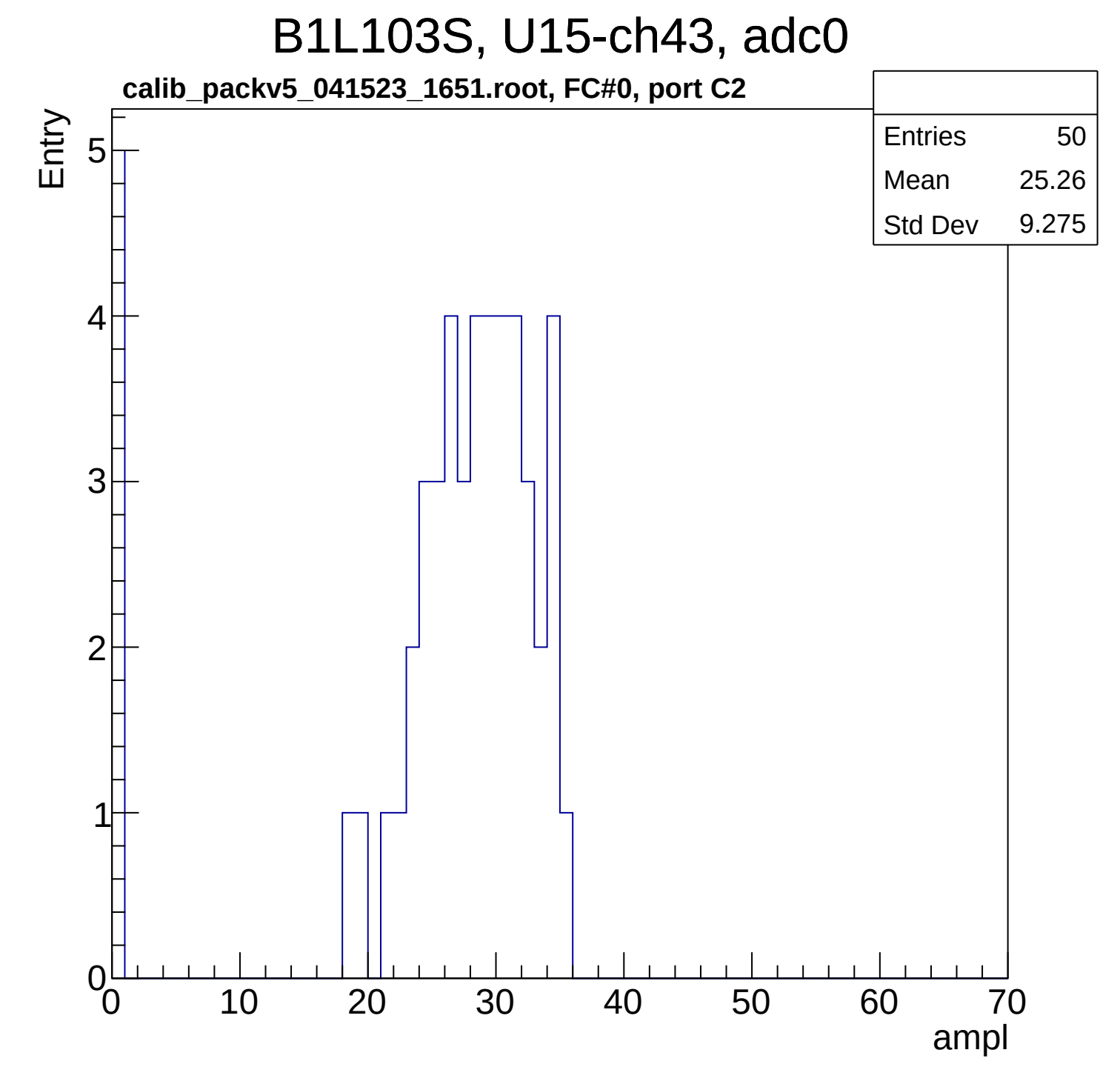
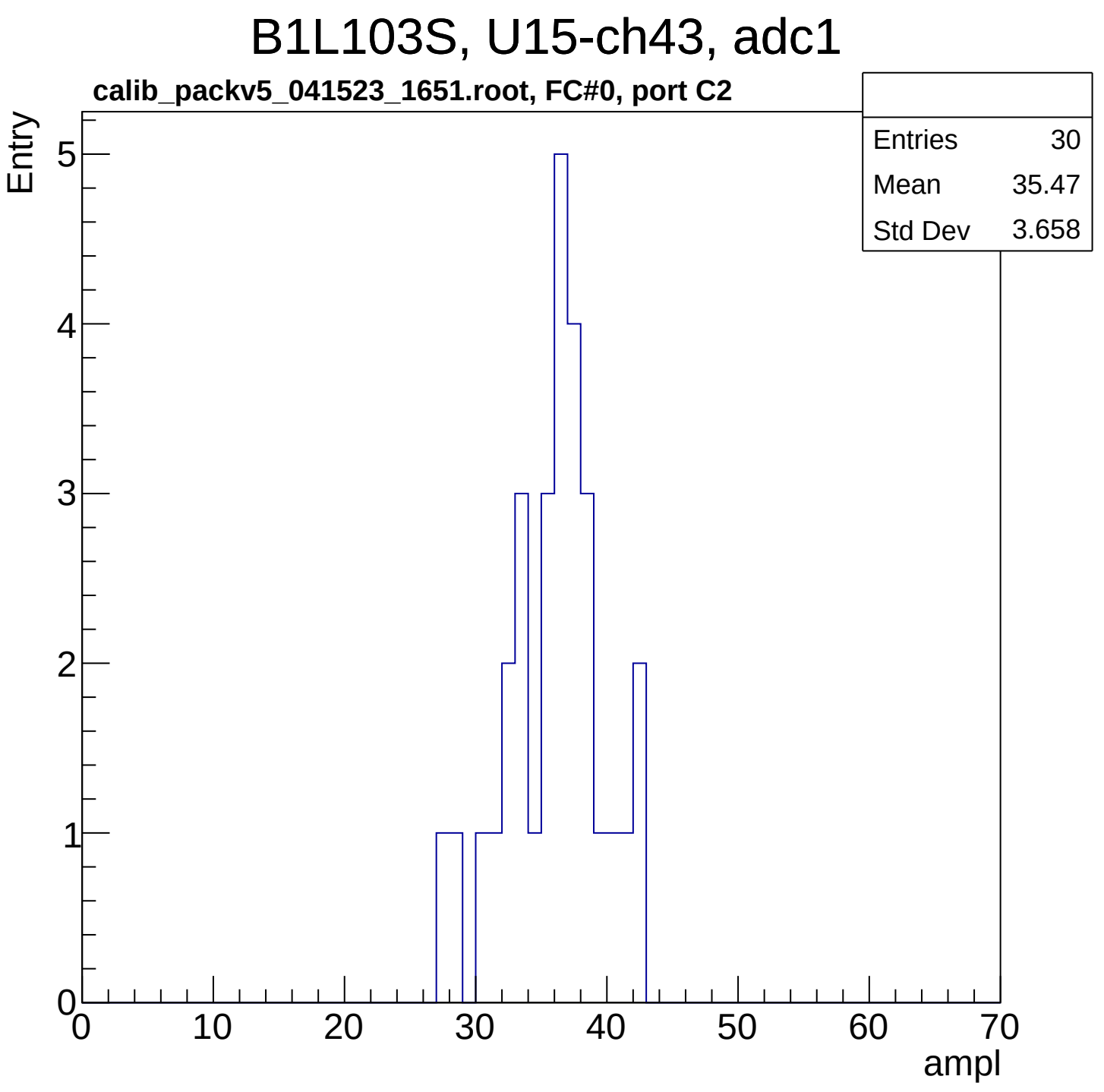
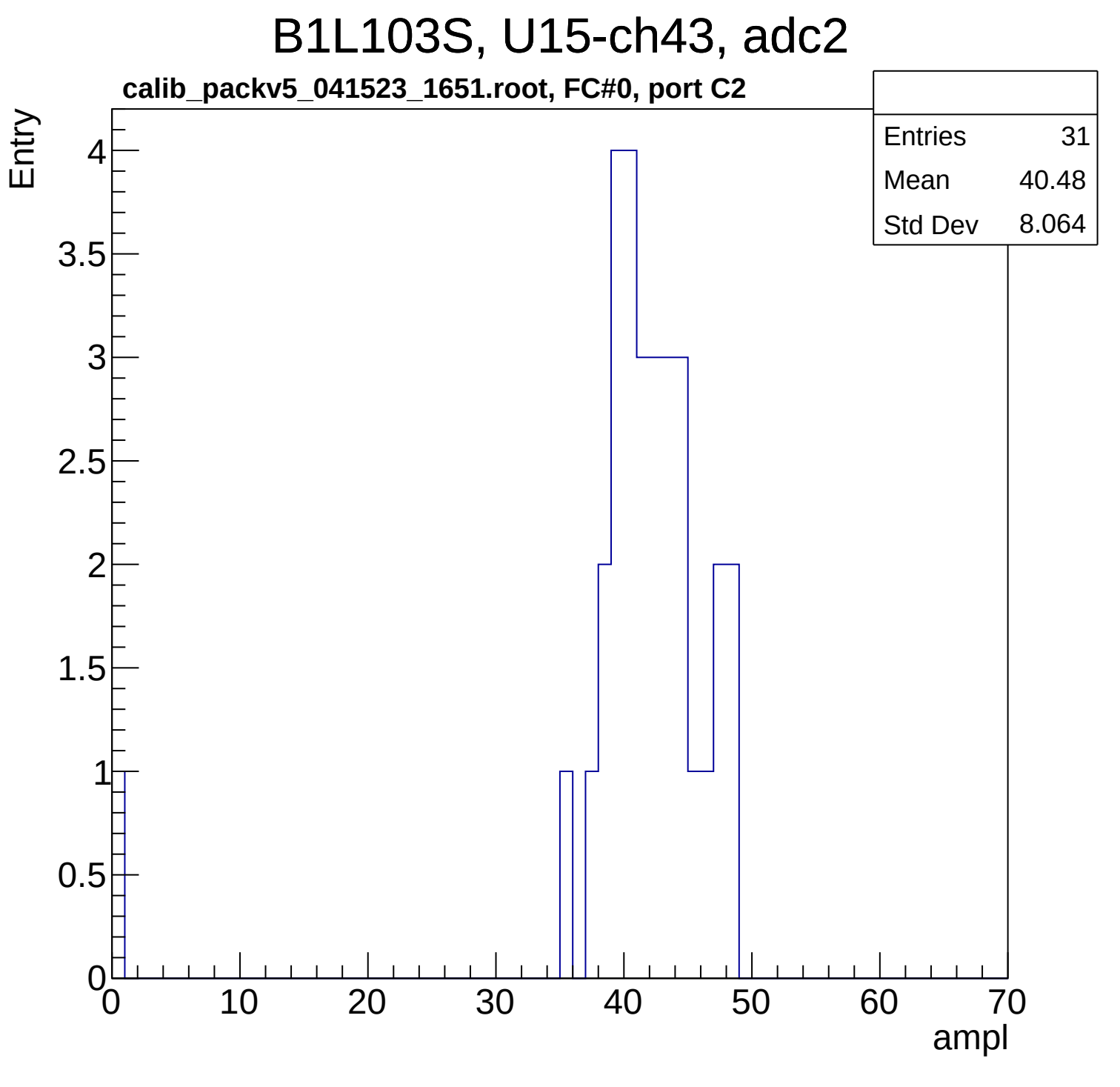
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch42, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch43, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 25.26
Std Dev 9.275
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch43, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 35.47
Std Dev 3.658
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch43, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 40.48
Std Dev 8.064
Entry
ampl
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0.5
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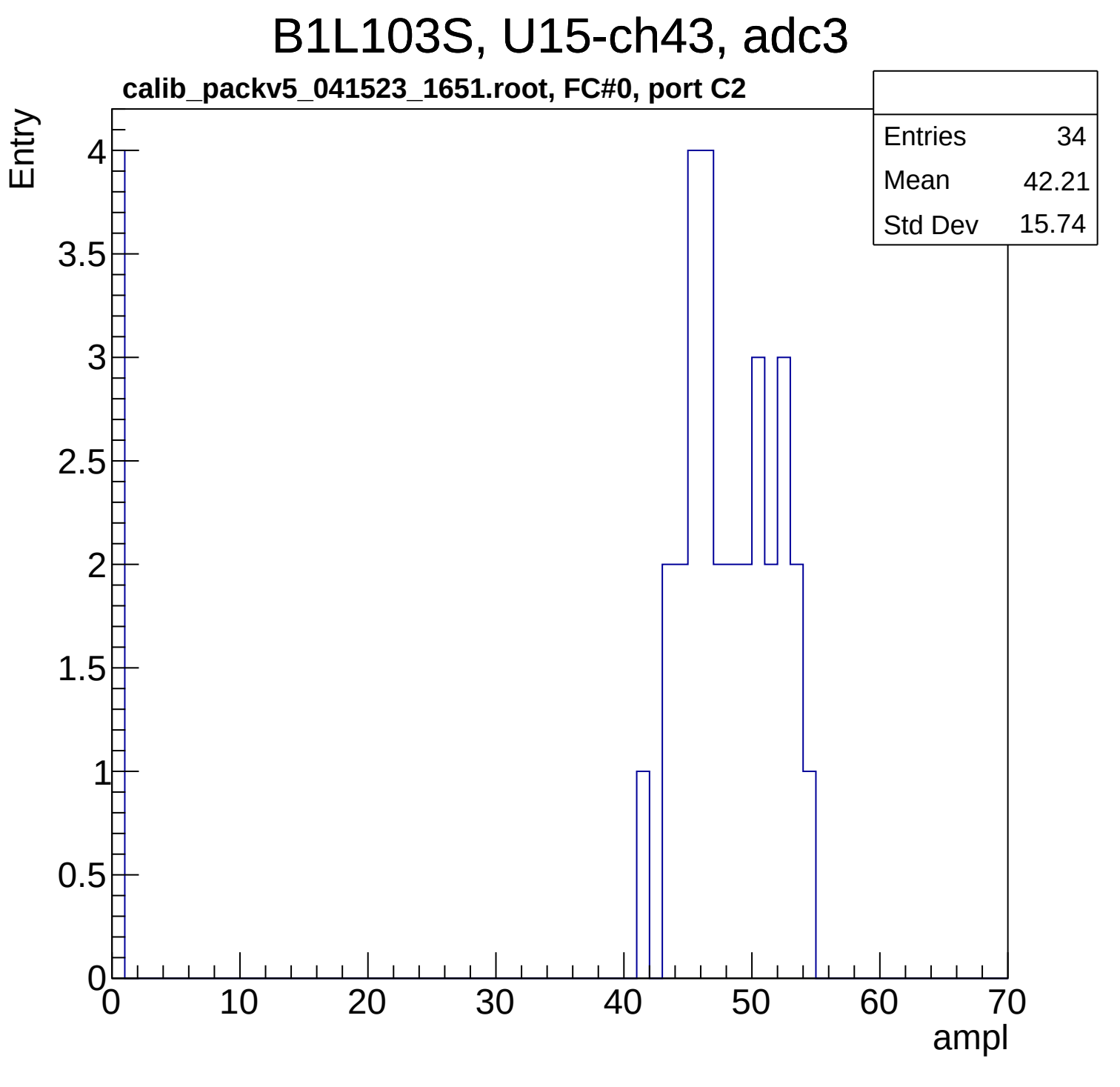
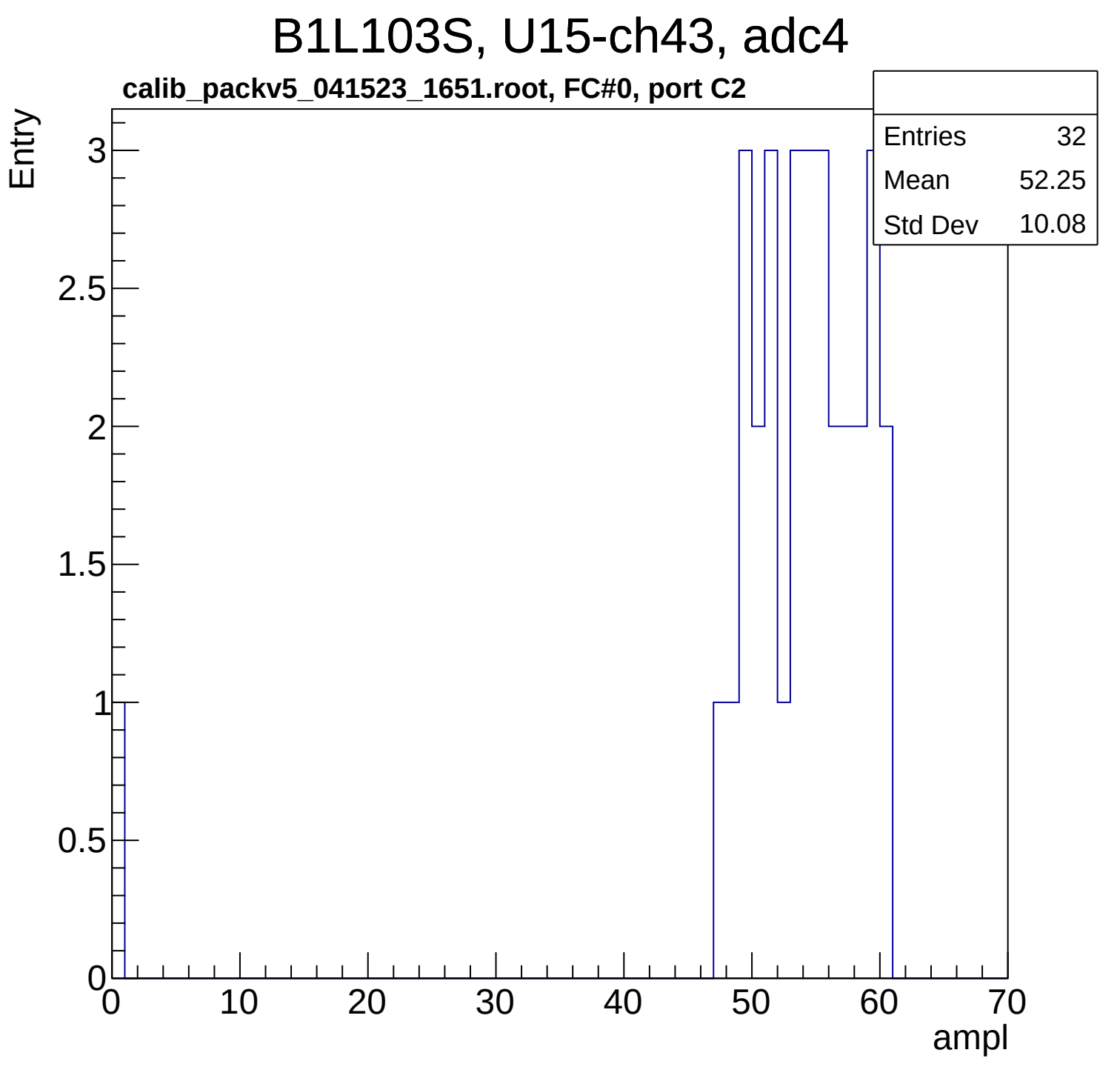
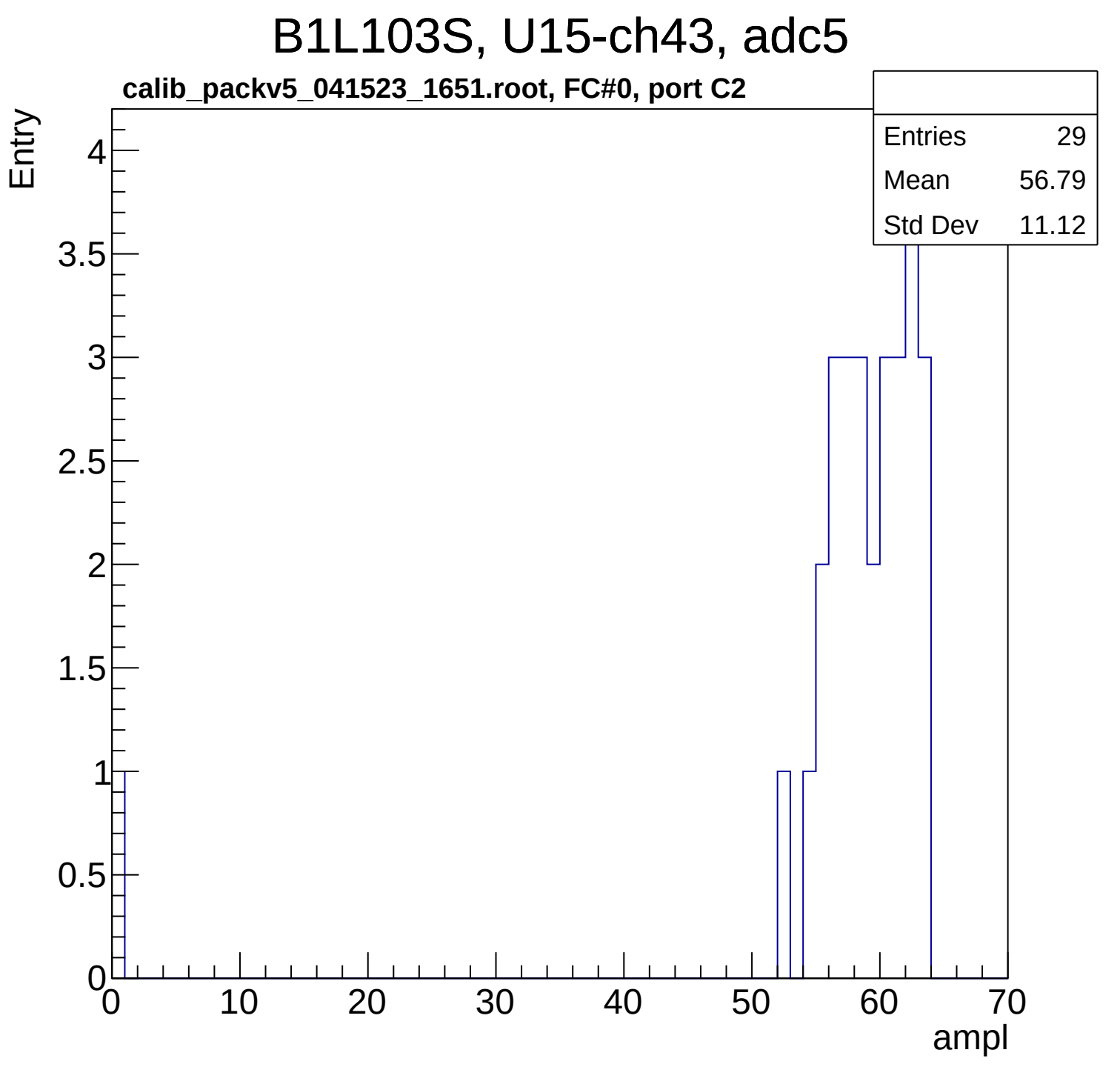
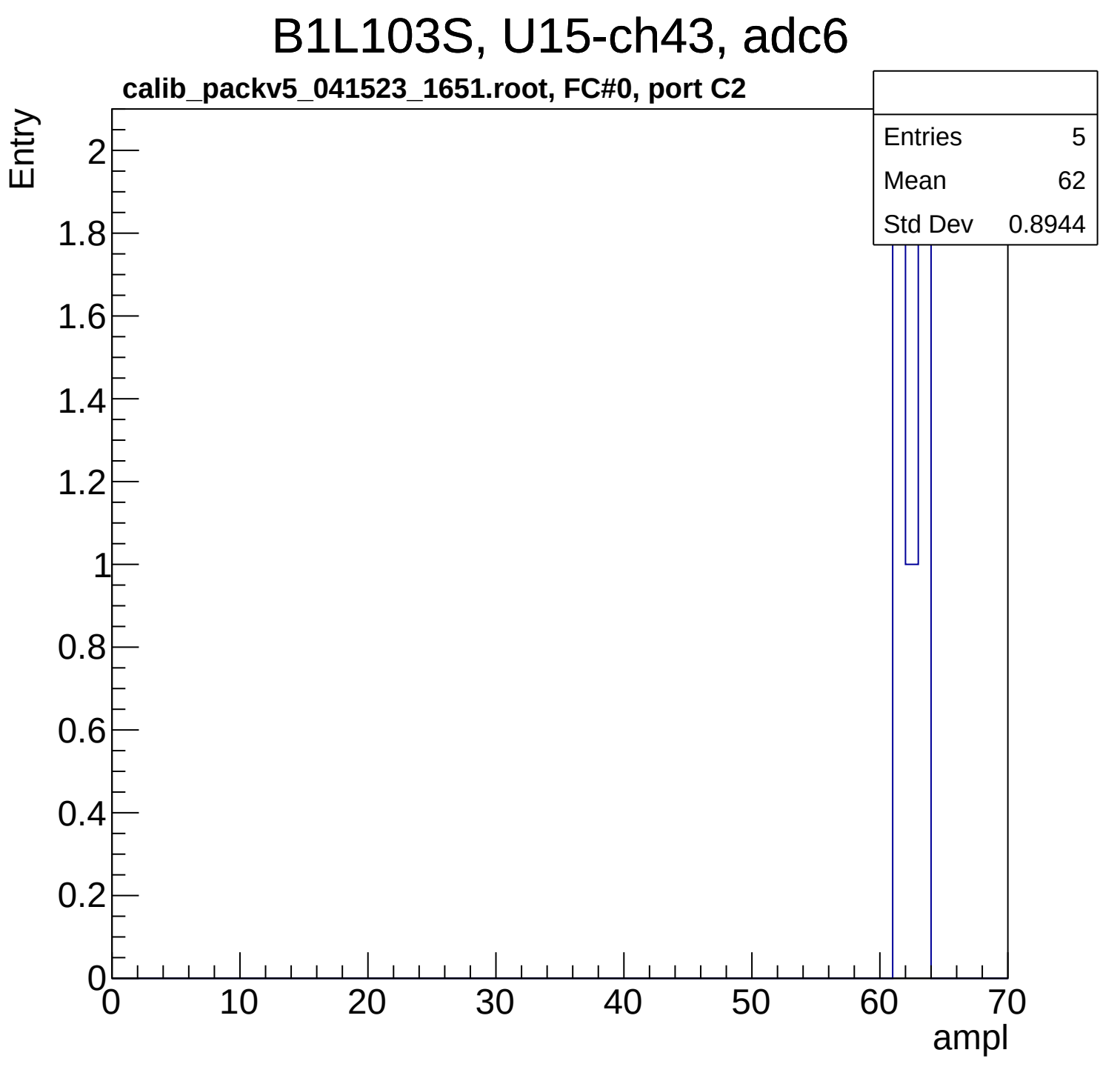
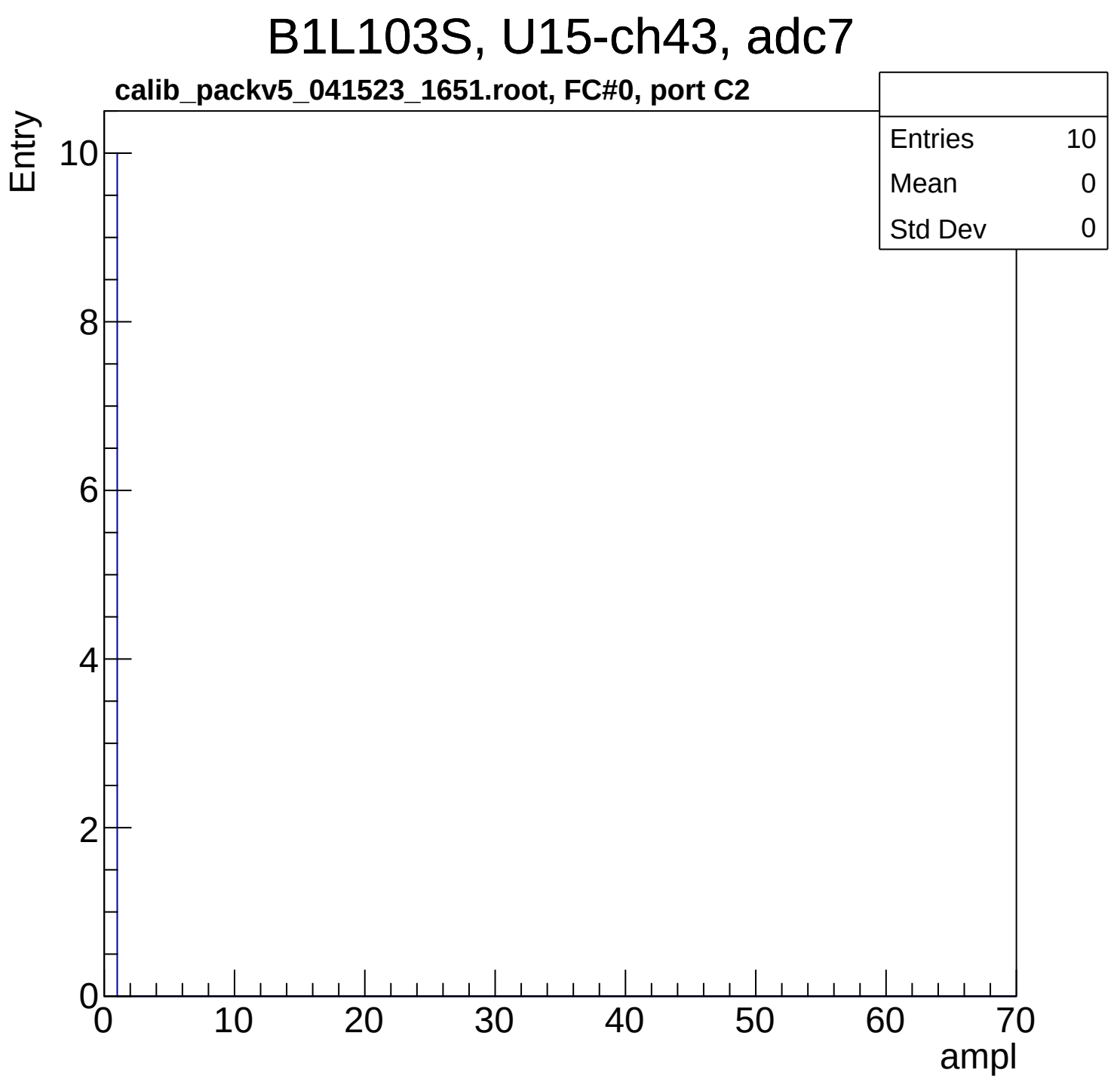
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

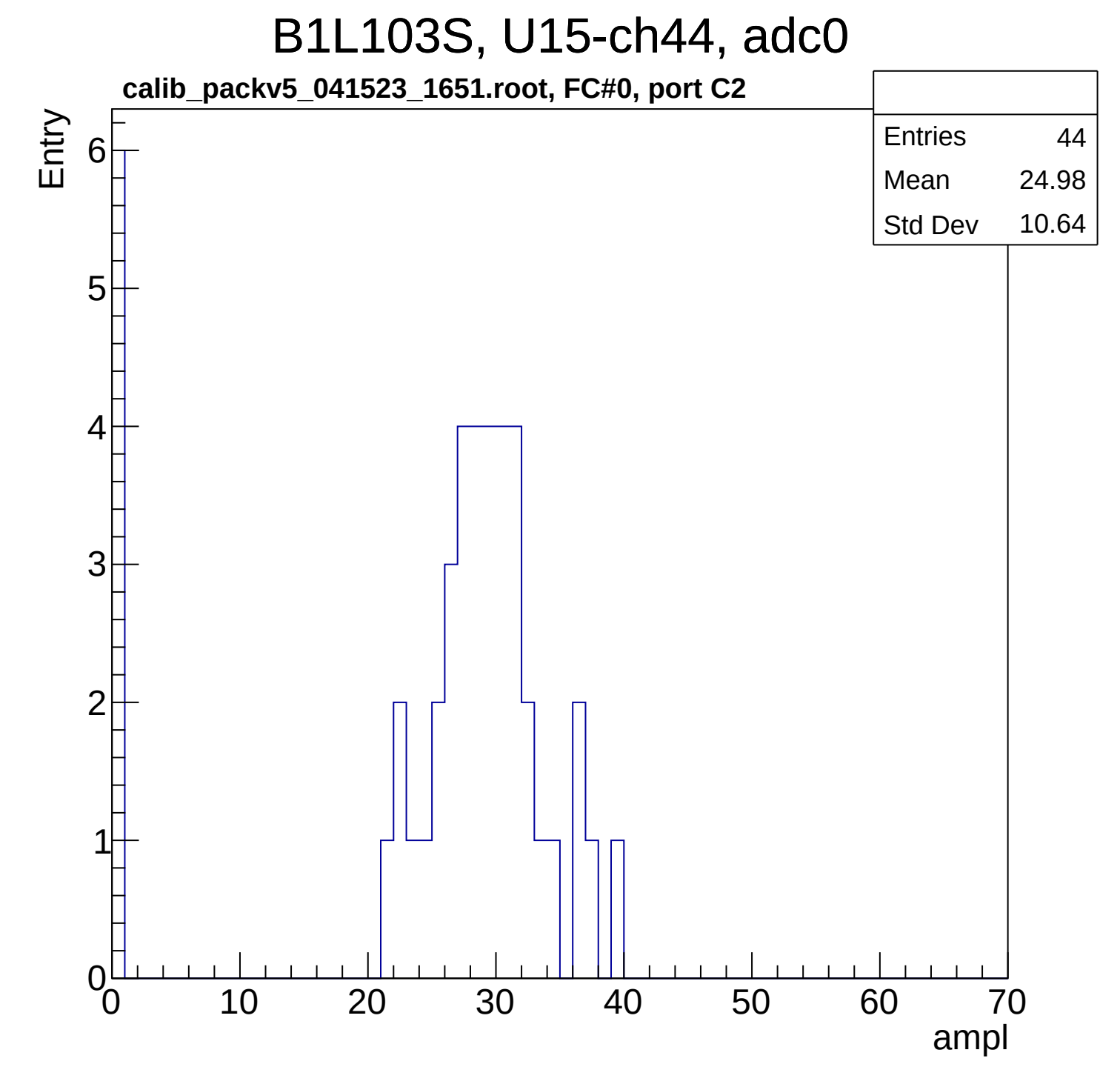

B1L103S, U15-ch43, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 42.21
Std Dev 15.74
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

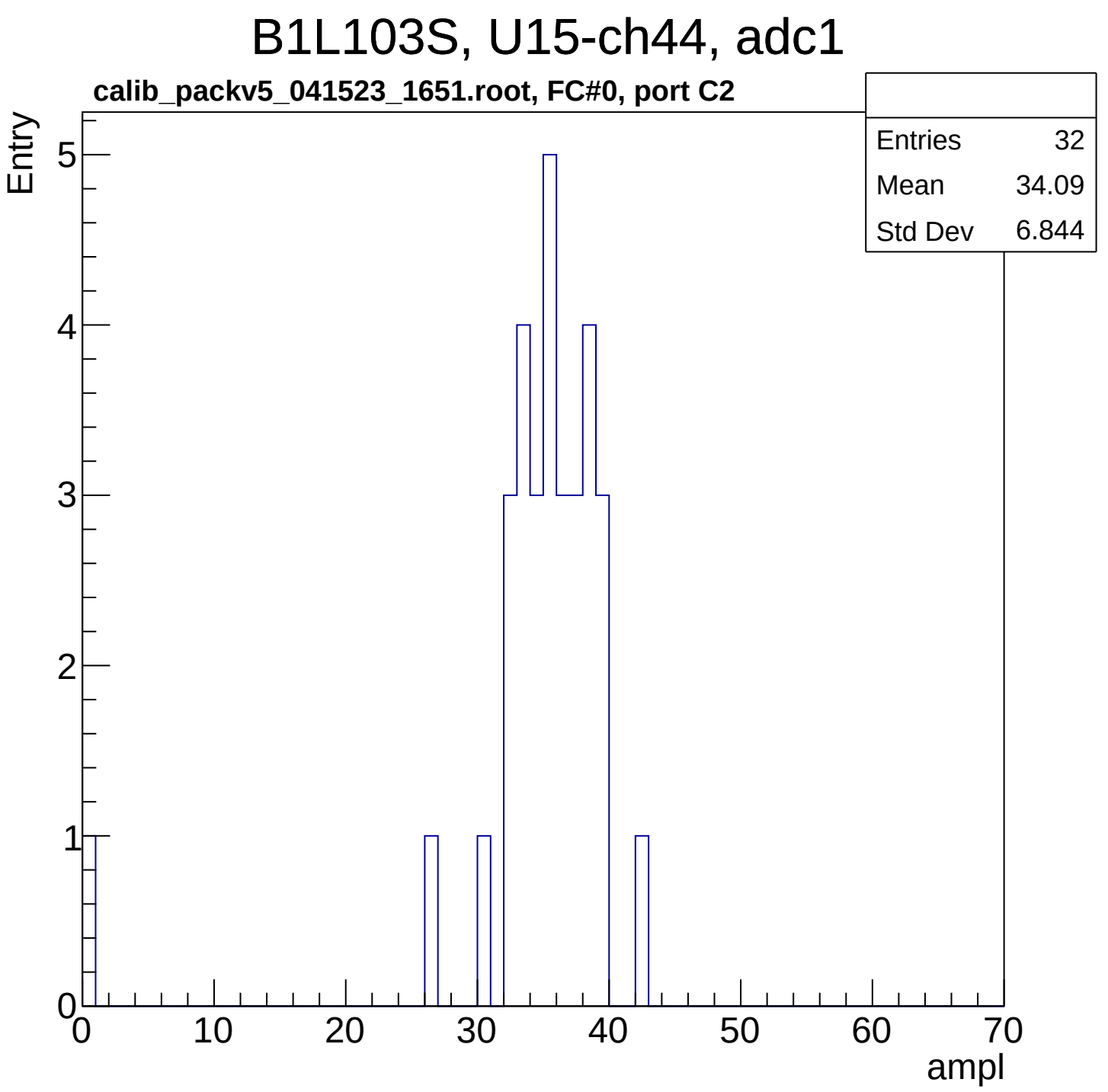

B1L103S, U15-ch43, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 52.25
Std Dev 10.08
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

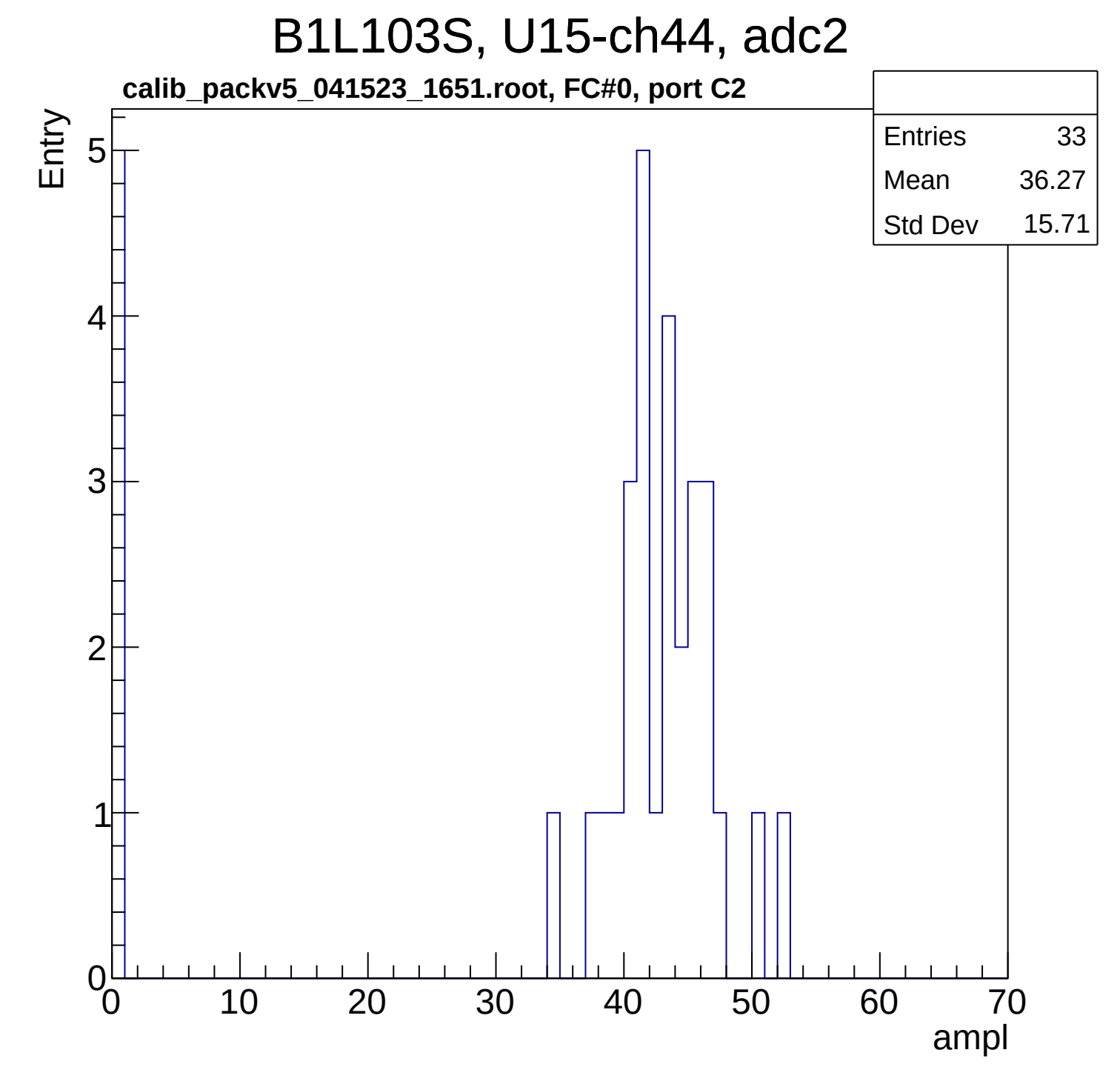

B1L103S, U15-ch43, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 56.79
Std Dev 11.12
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

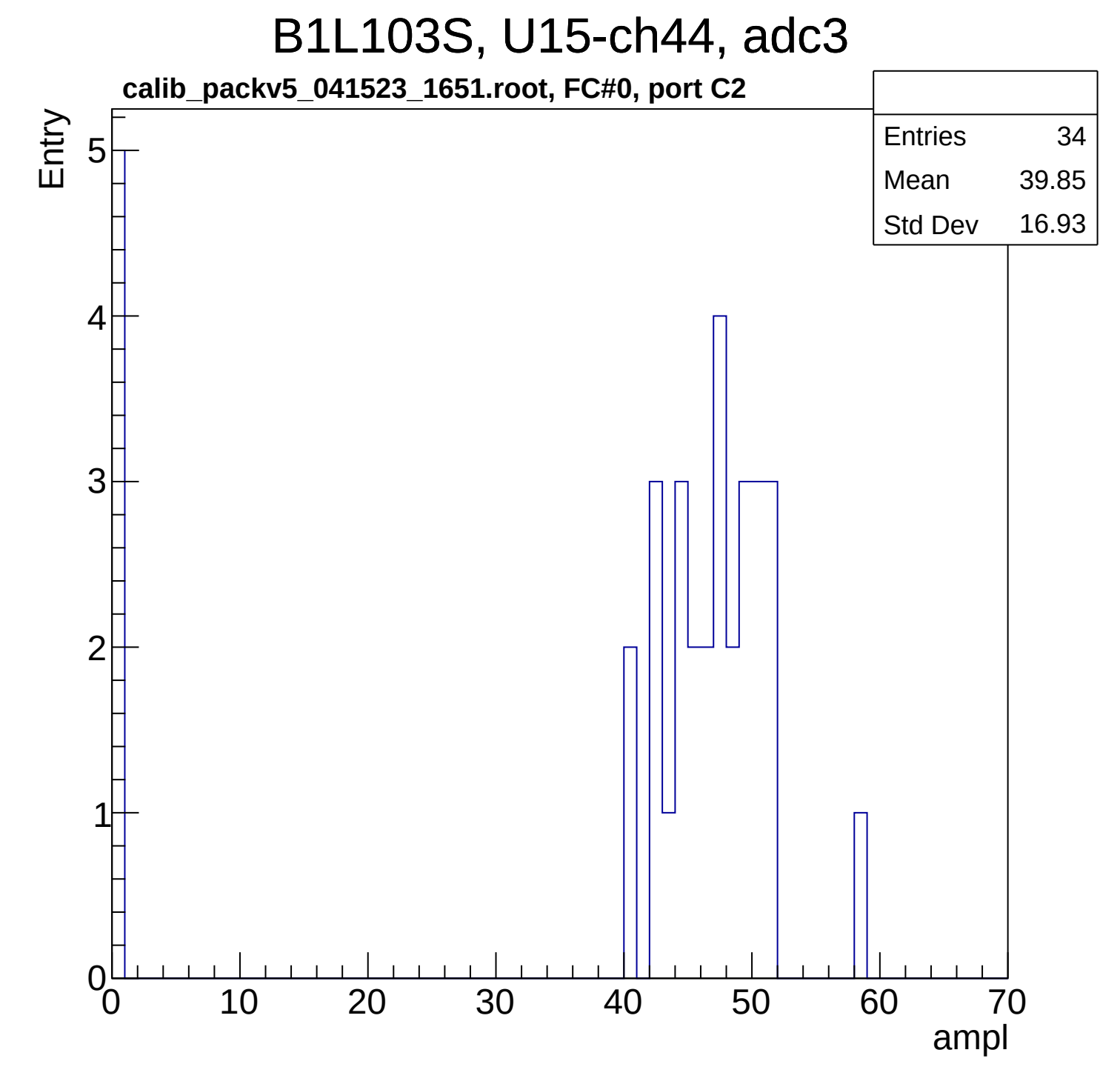

B1L103S, U15-ch43, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62
Std Dev 0.8944
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

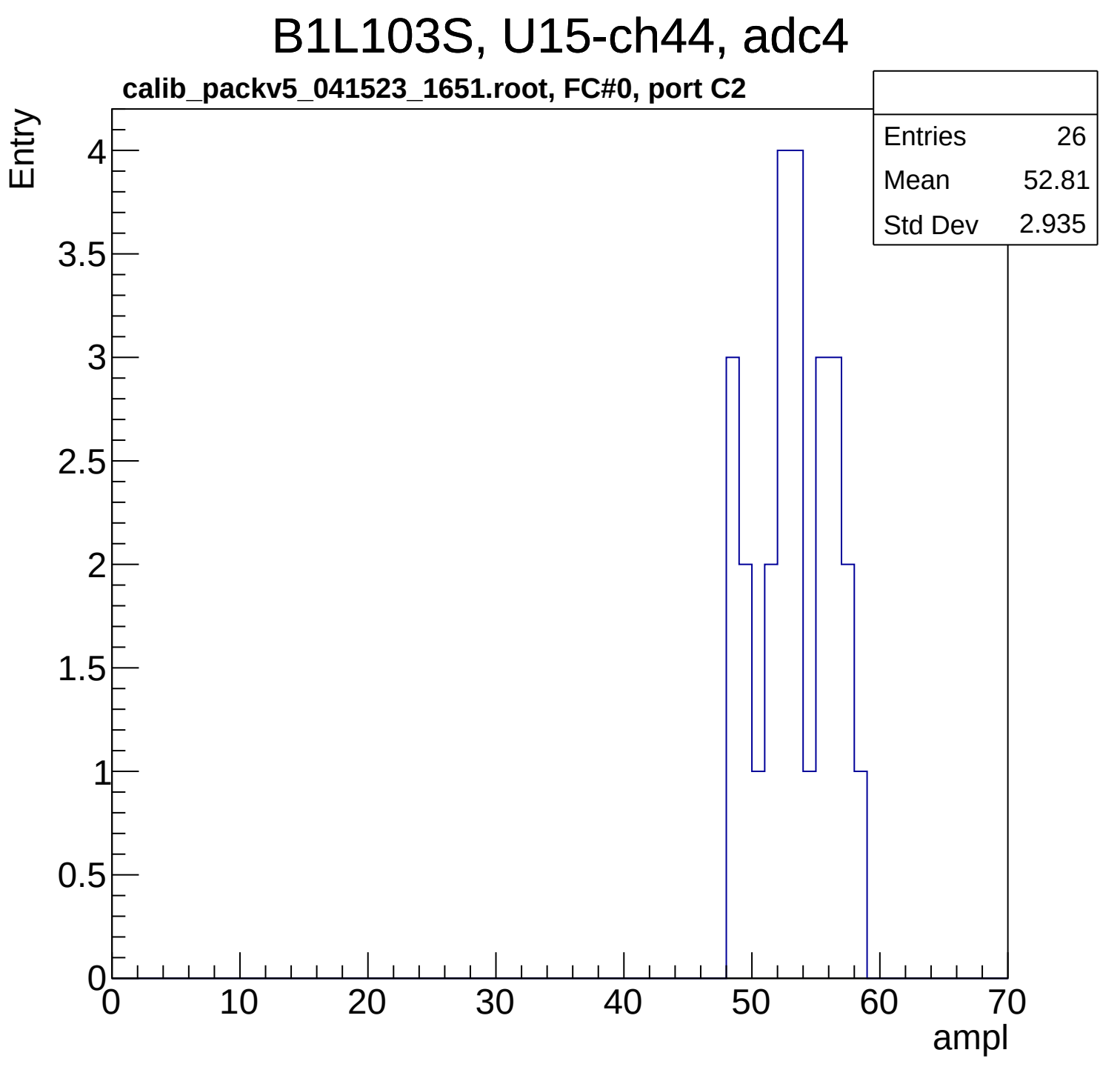

B1L103S, U15-ch43, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

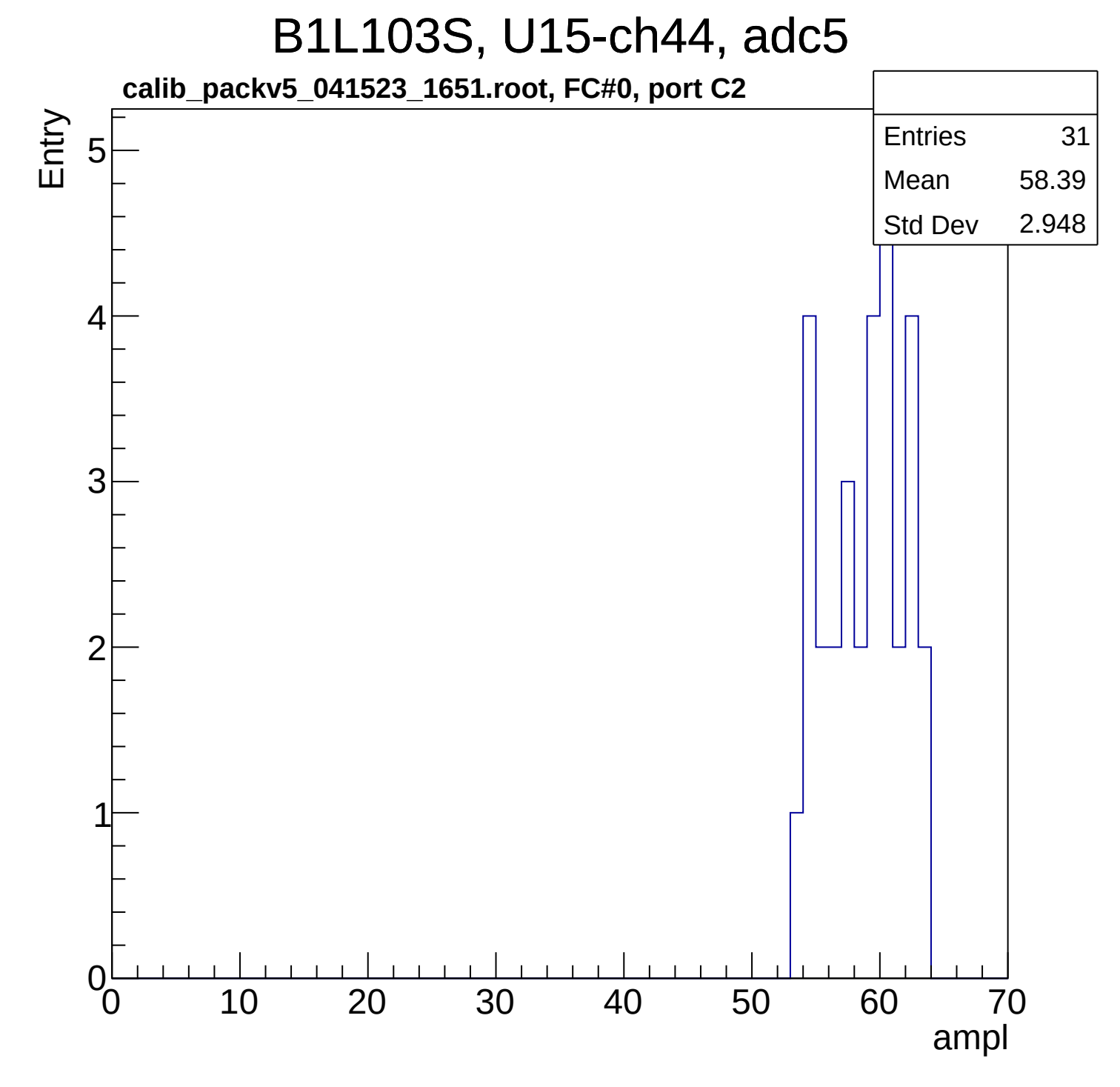

B1L103S, U15-ch44, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 24.98
Std Dev 10.64
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

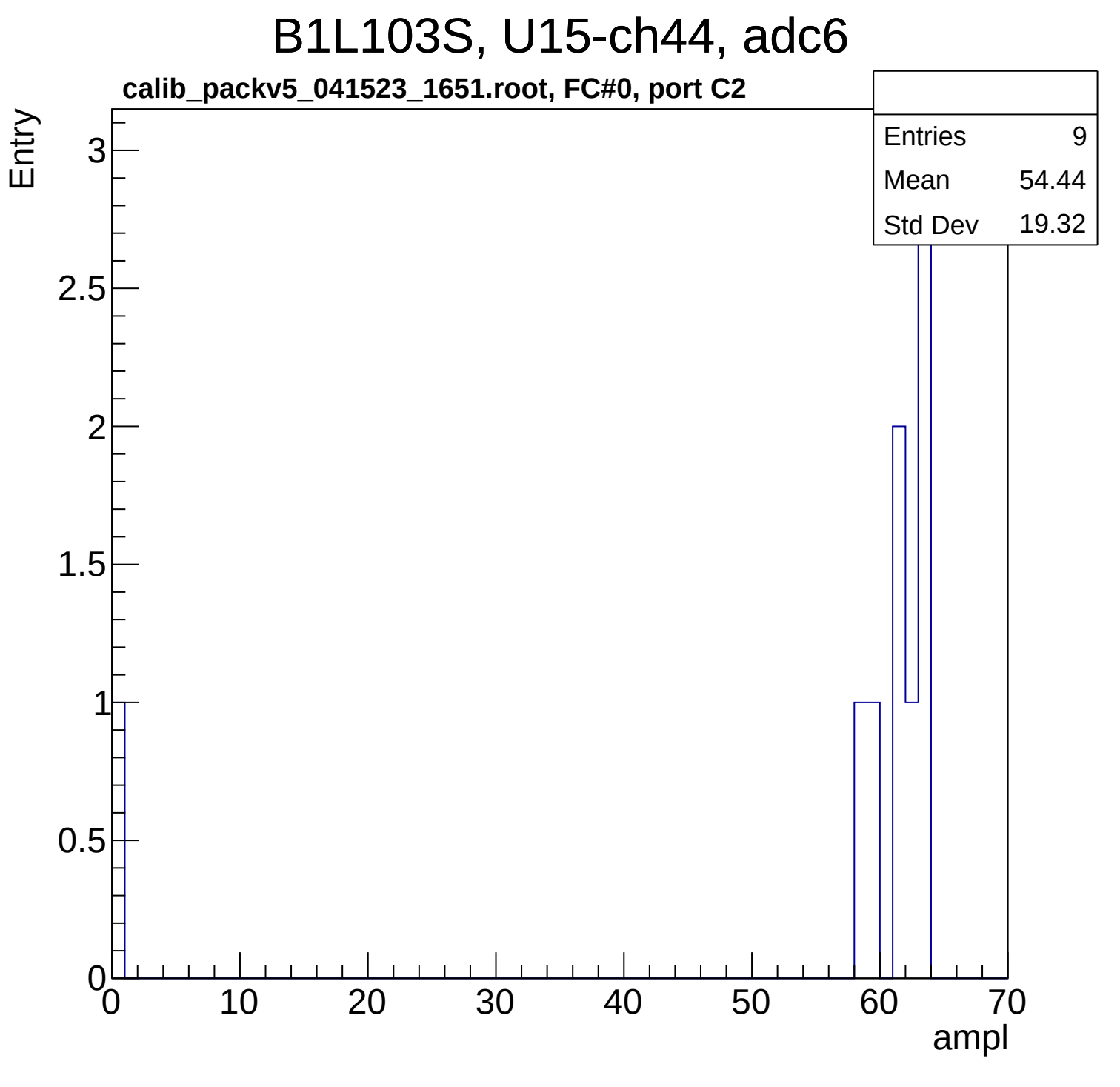

B1L103S, U15-ch44, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 34.09
Std Dev 6.844
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

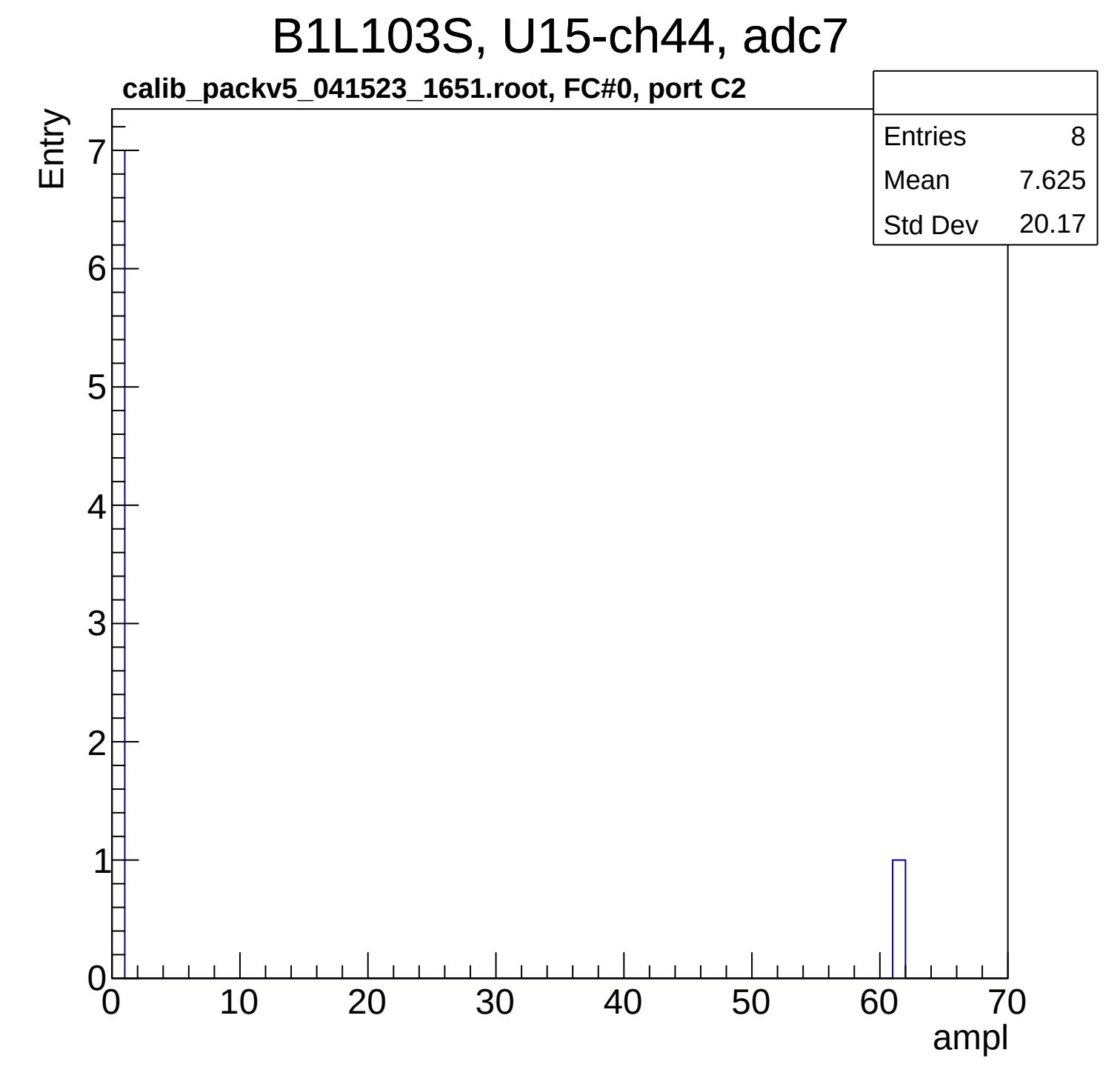

B1L103S, U15-ch44, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 36.27
Std Dev 15.71
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

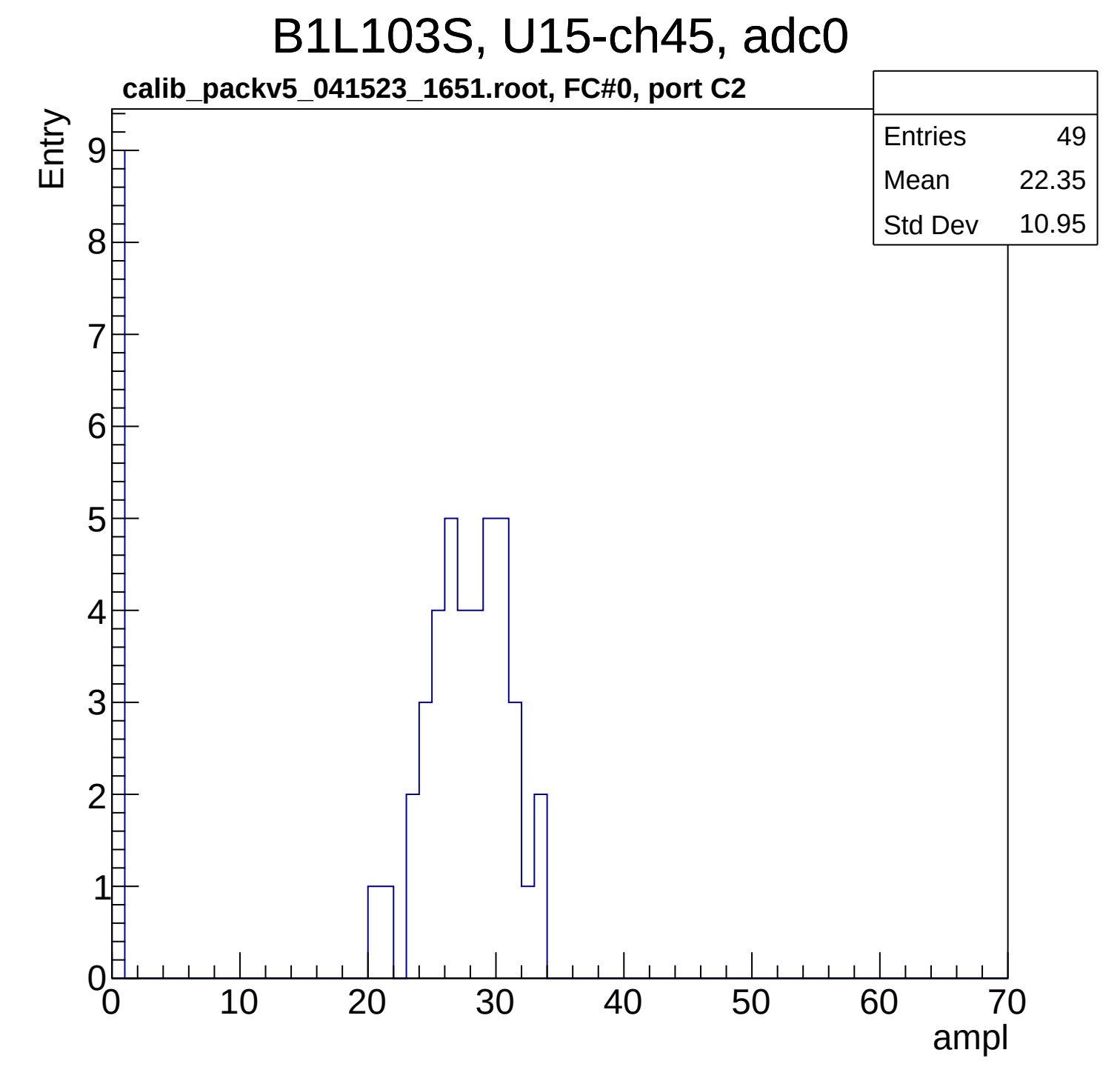

B1L103S, U15-ch44, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 39.85
Std Dev 16.93
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

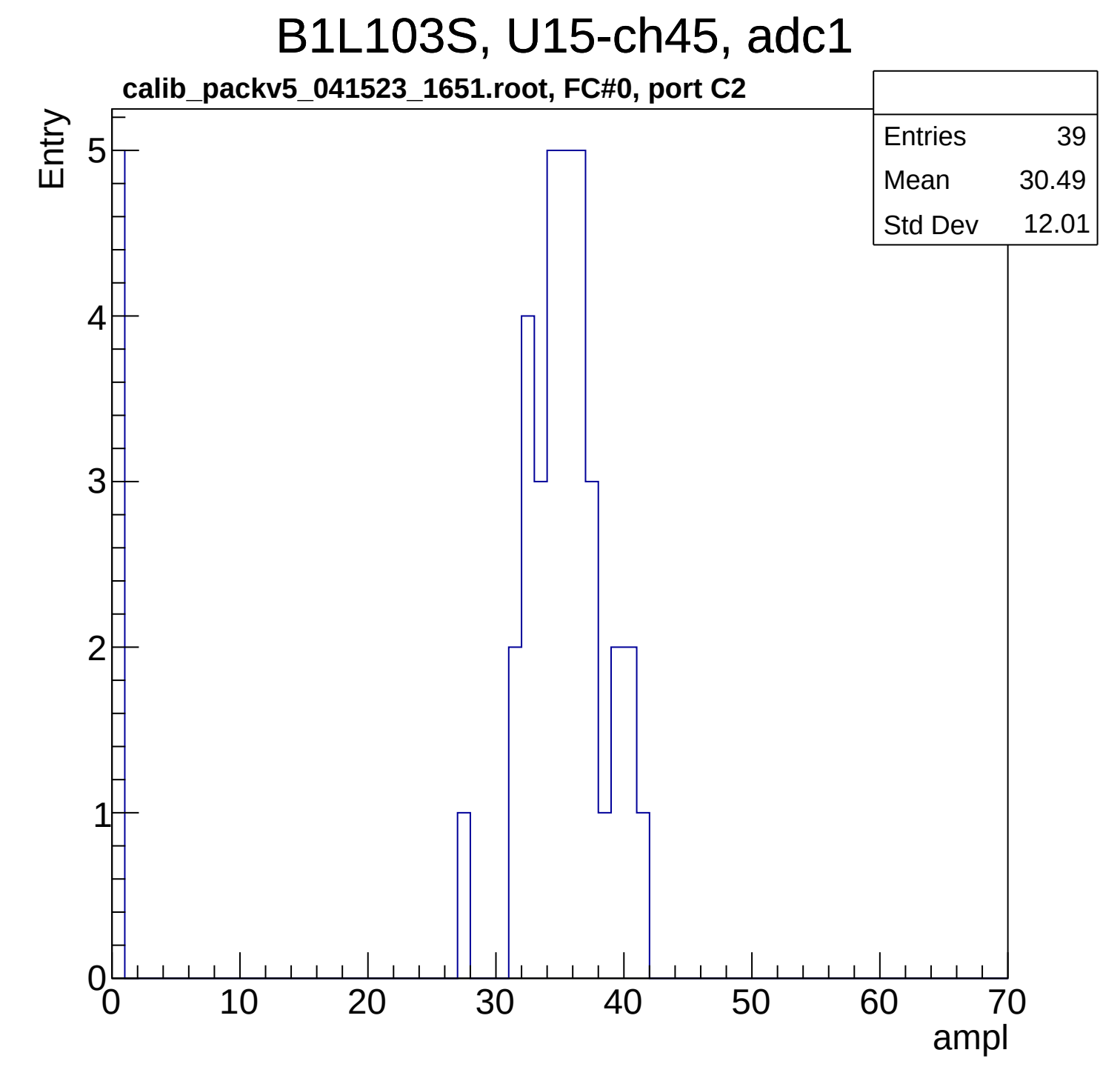

B1L103S, U15-ch44, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 52.81
Std Dev 2.935
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

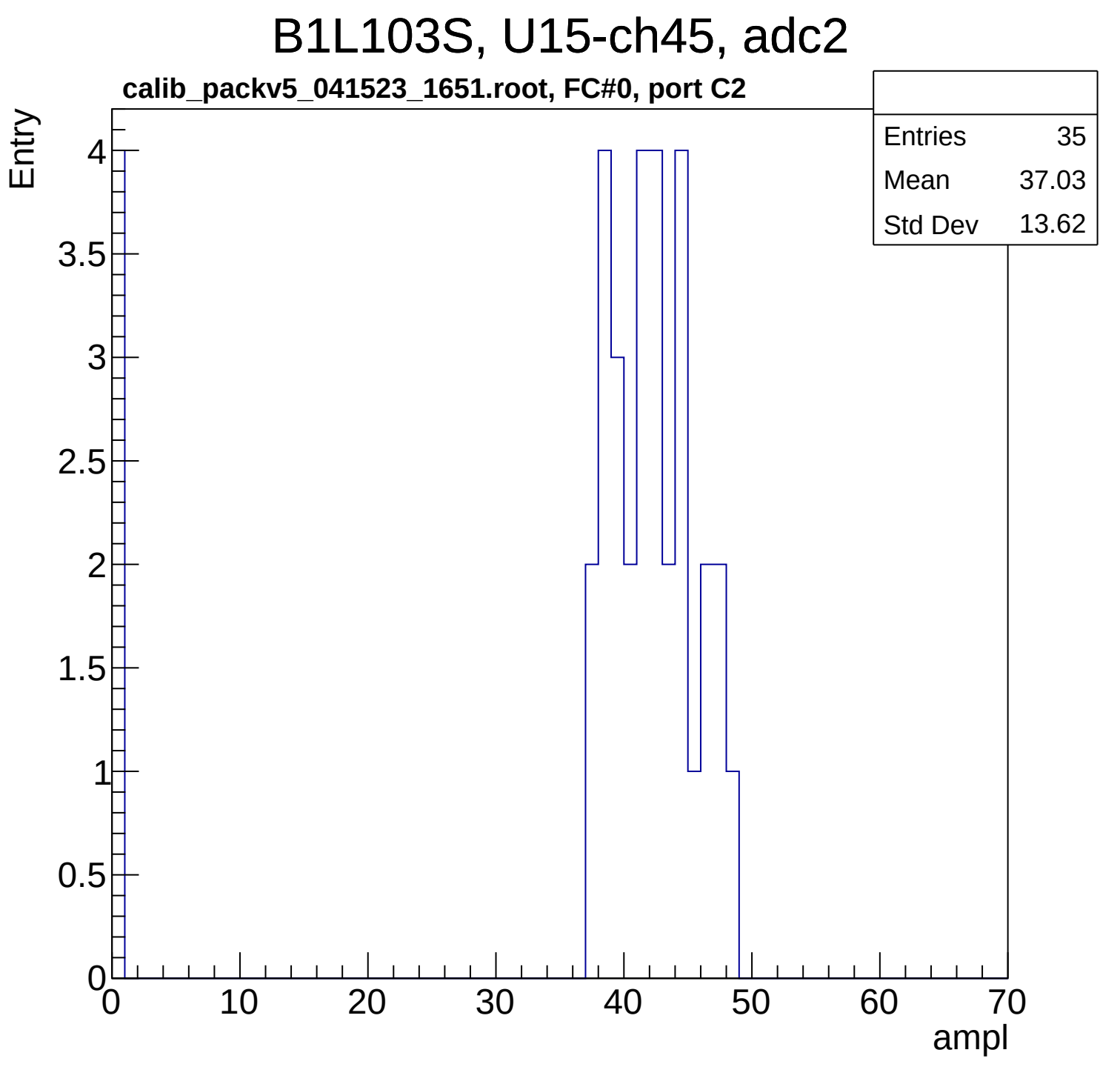

B1L103S, U15-ch44, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 58.39
Std Dev 2.948
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

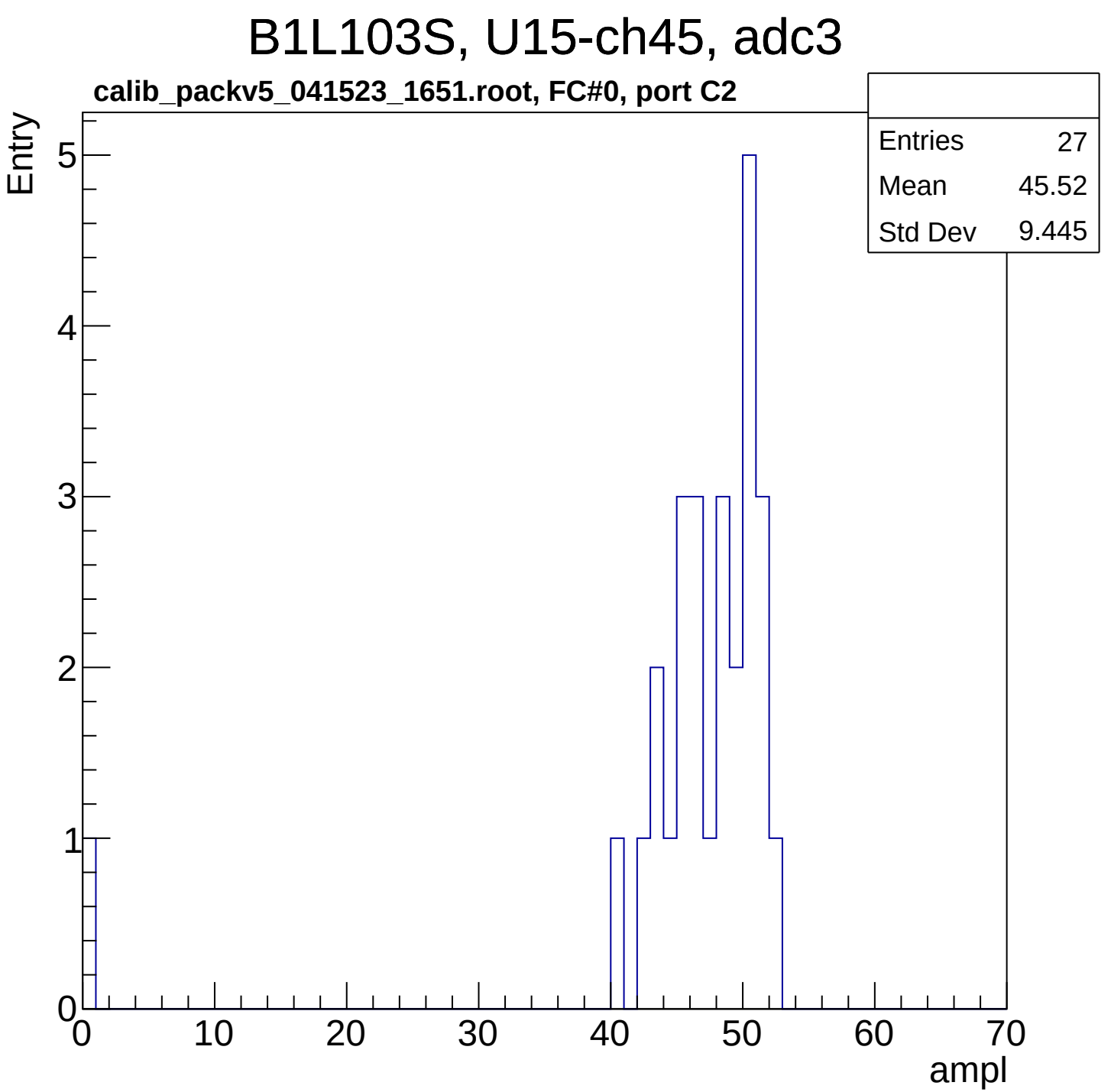

B1L103S, U15-ch44, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 54.44
Std Dev 19.32
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

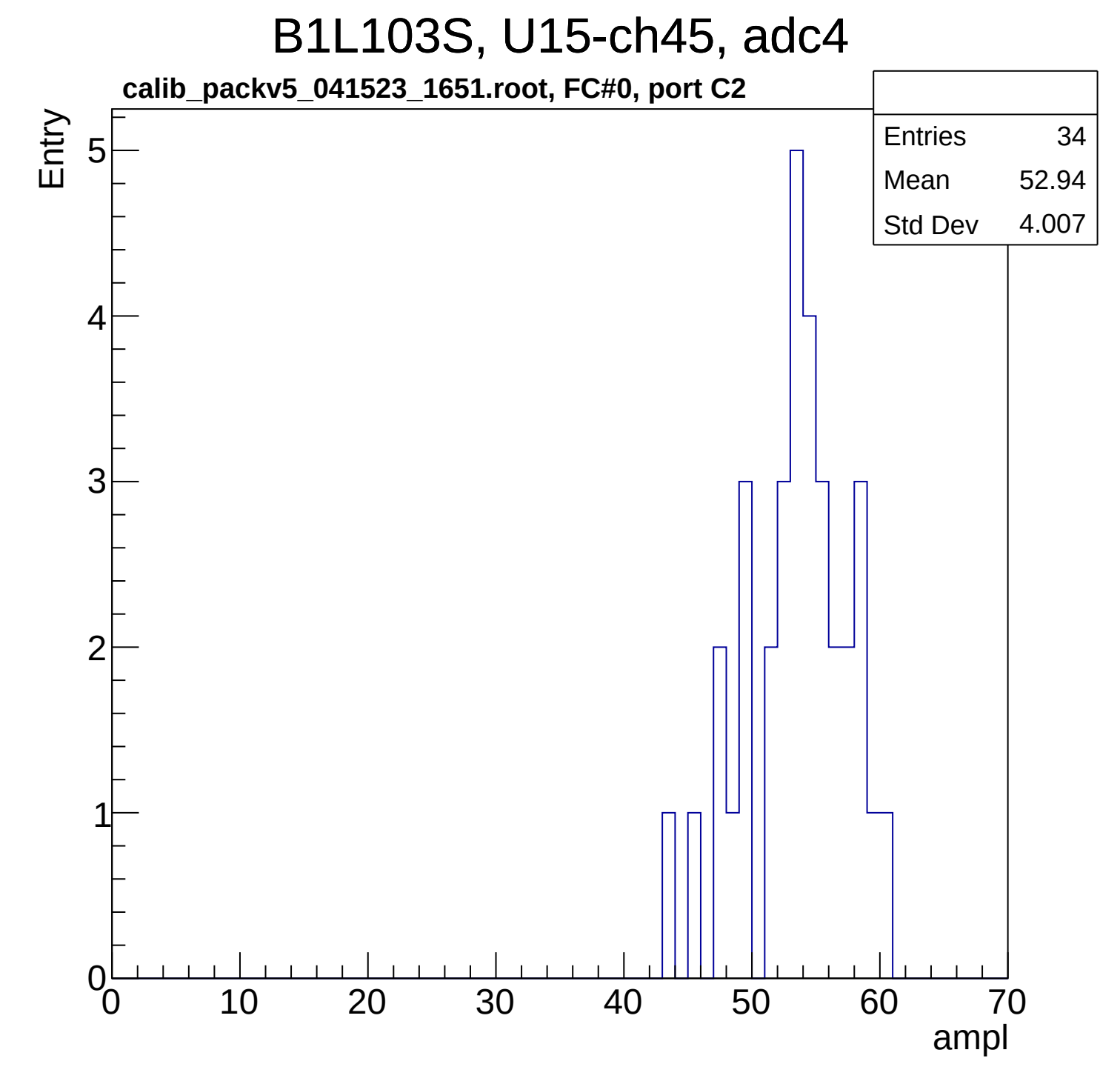

B1L103S, U15-ch44, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 7.625
Std Dev 20.17
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

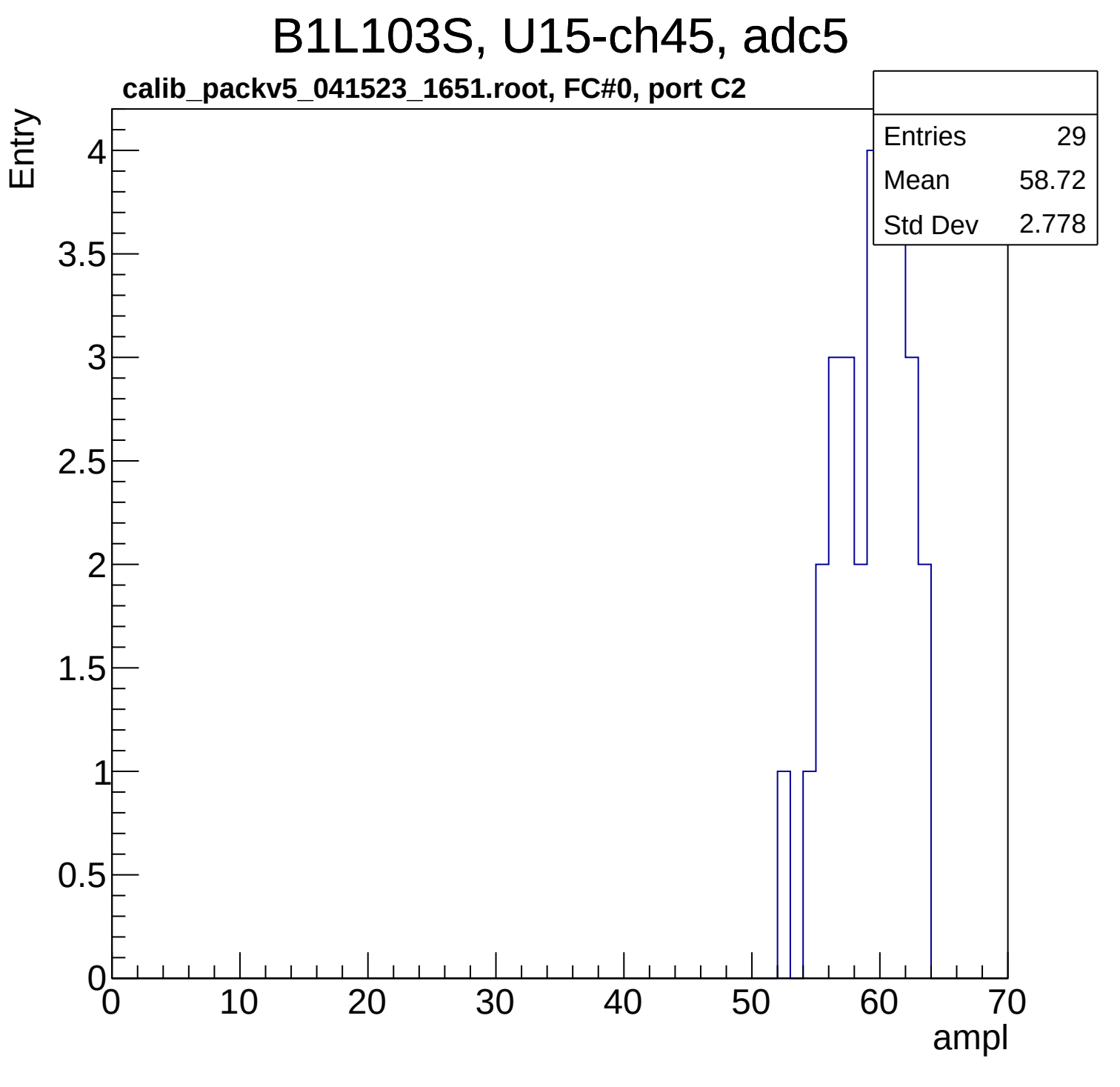

B1L103S, U15-ch45, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 22.35
Std Dev 10.95
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

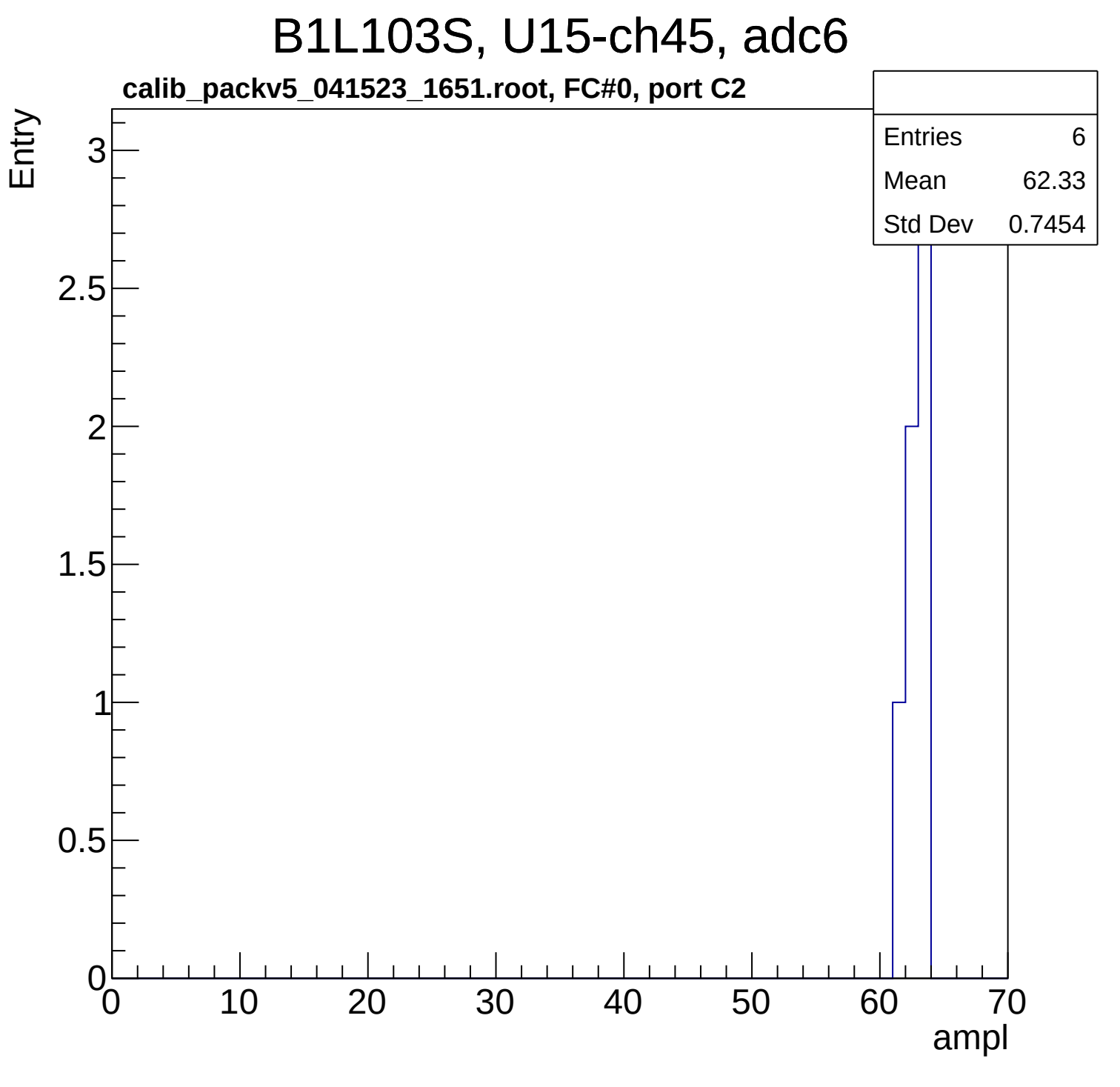

B1L103S, U15-ch45, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 30.49
Std Dev 12.01
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

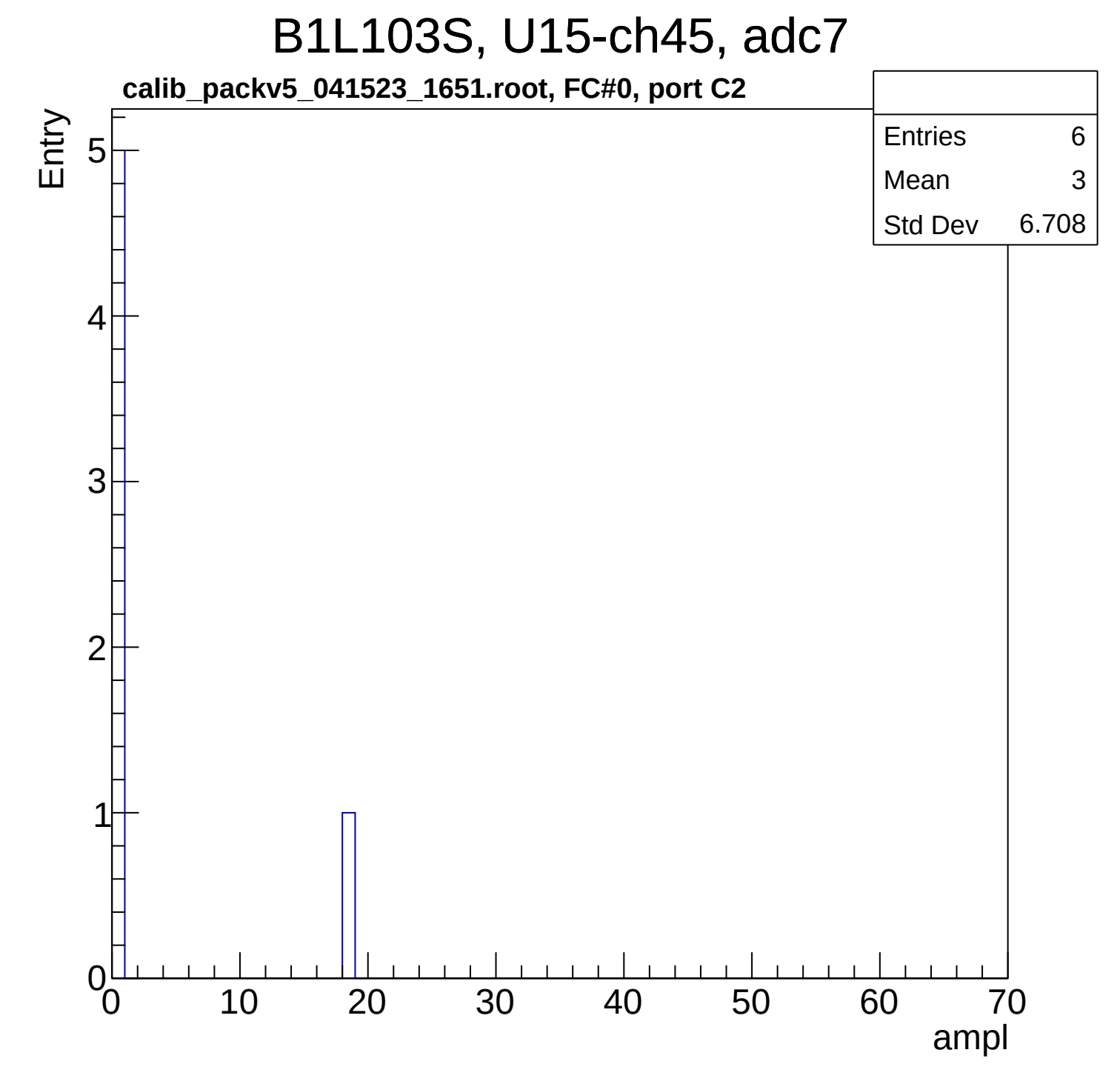

B1L103S, U15-ch45, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 37.03
Std Dev 13.62
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

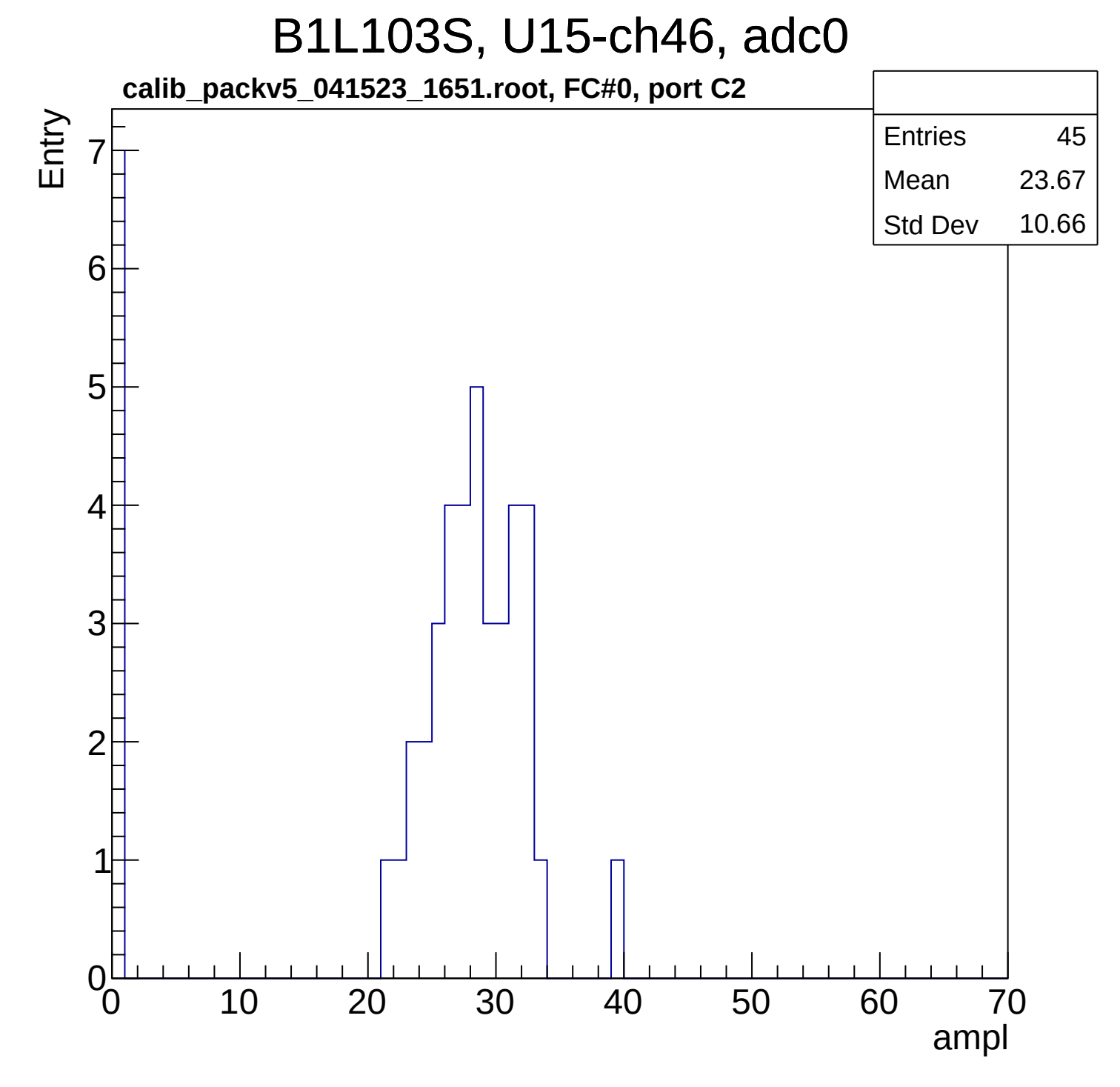

B1L103S, U15-ch45, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 45.52
Std Dev 9.445
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

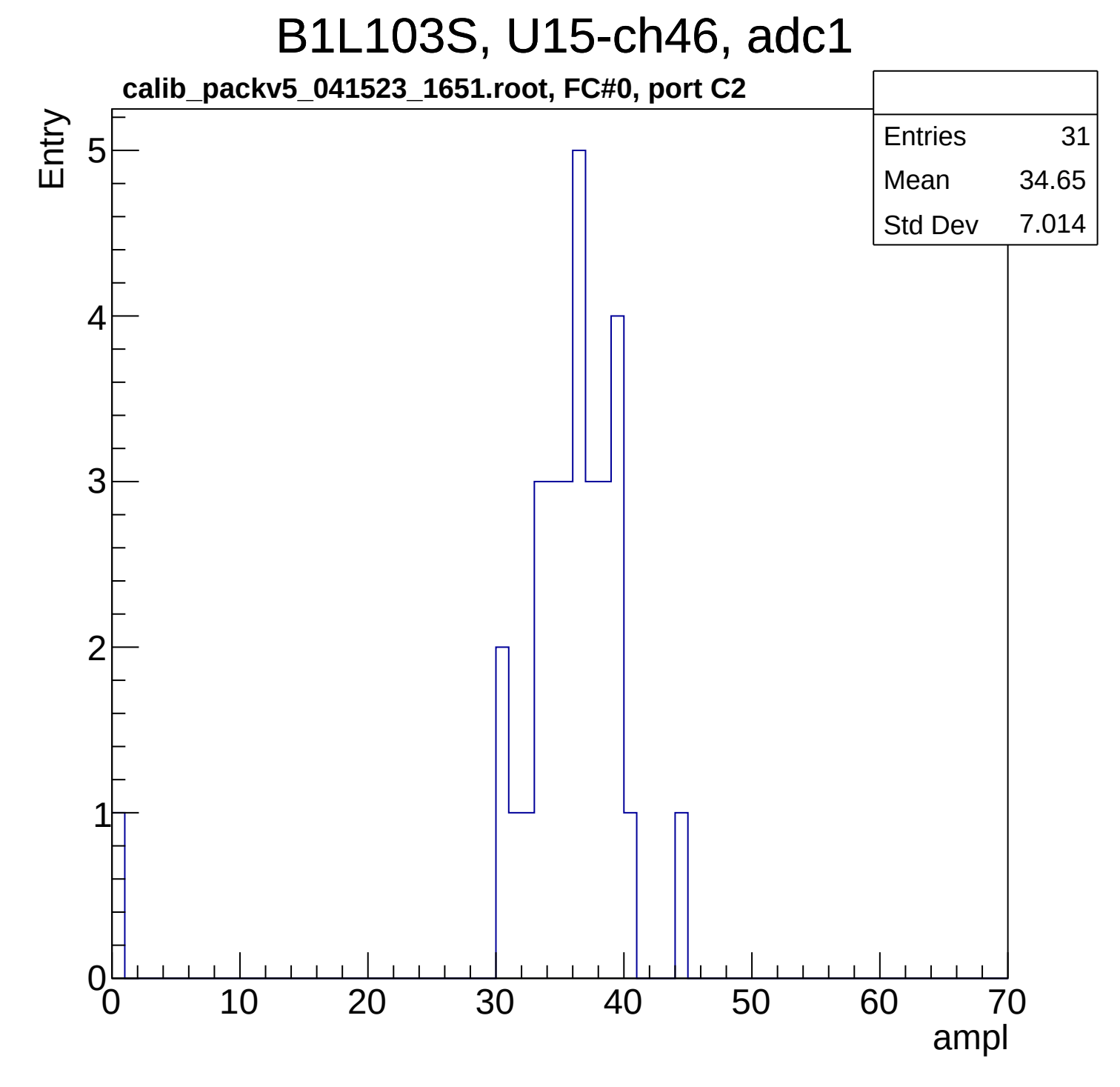

B1L103S, U15-ch45, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 52.94
Std Dev 4.007
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

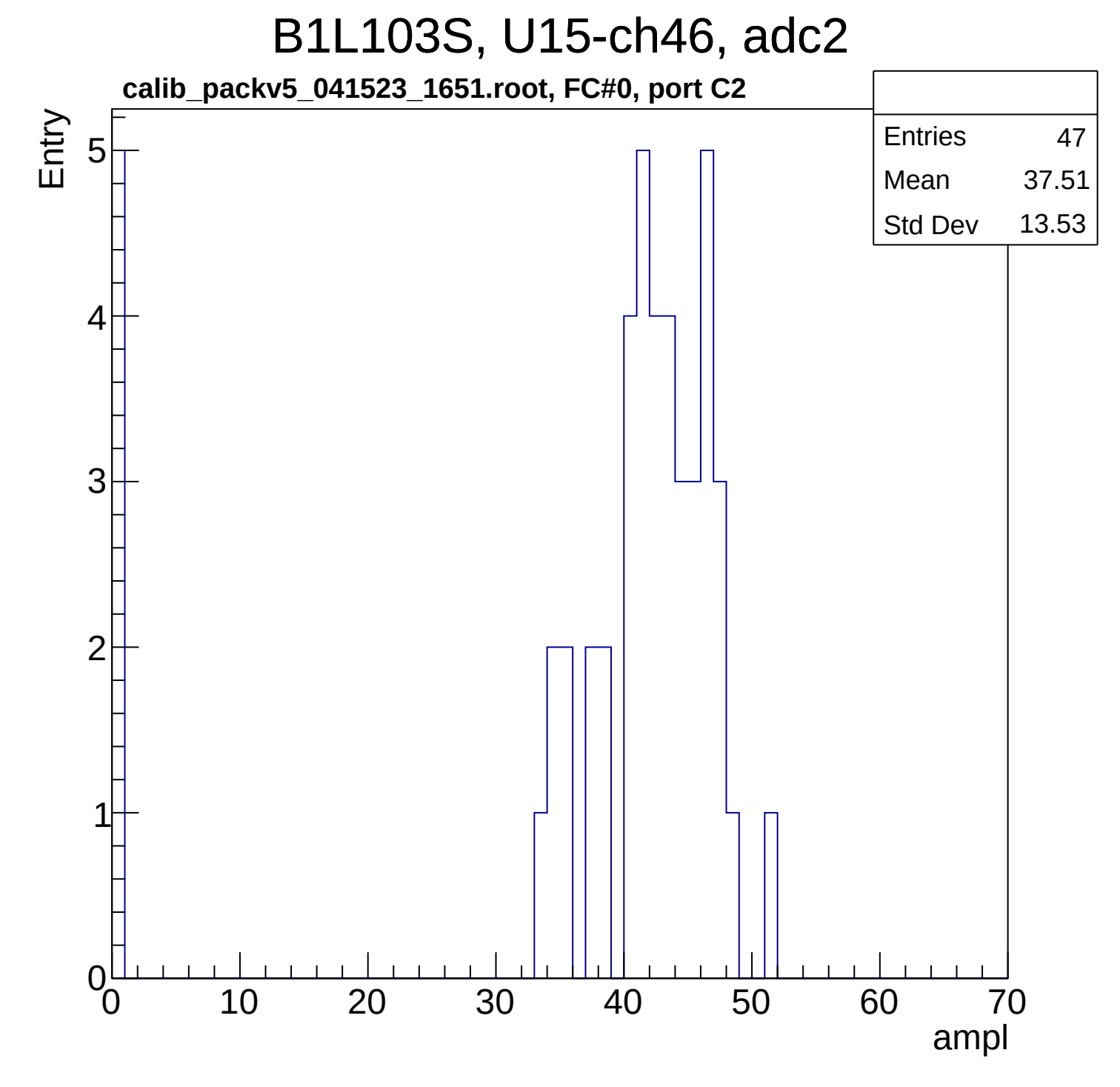

B1L103S, U15-ch45, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 58.72
Std Dev 2.778
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

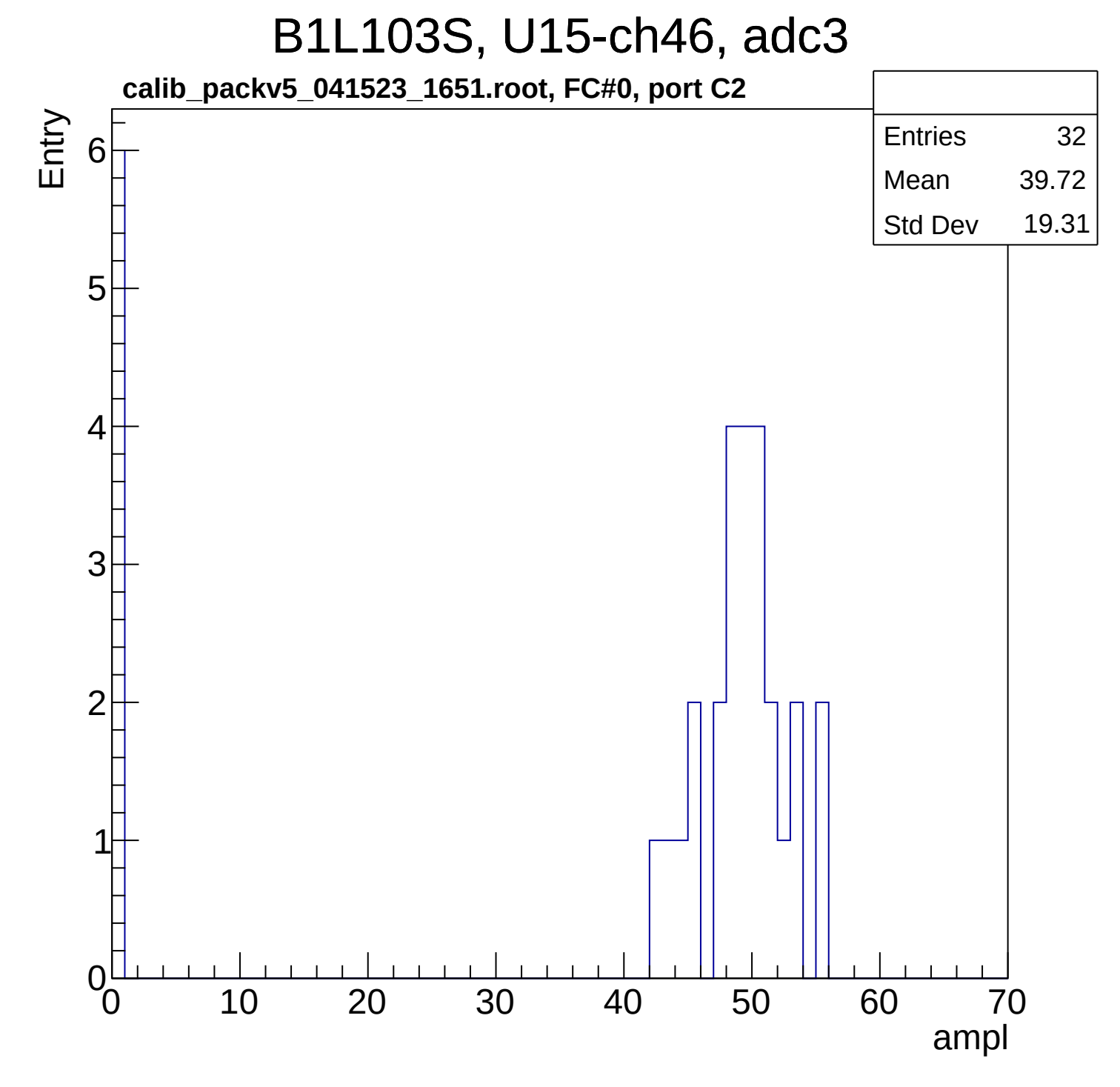

B1L103S, U15-ch45, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.33
Std Dev 0.7454
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

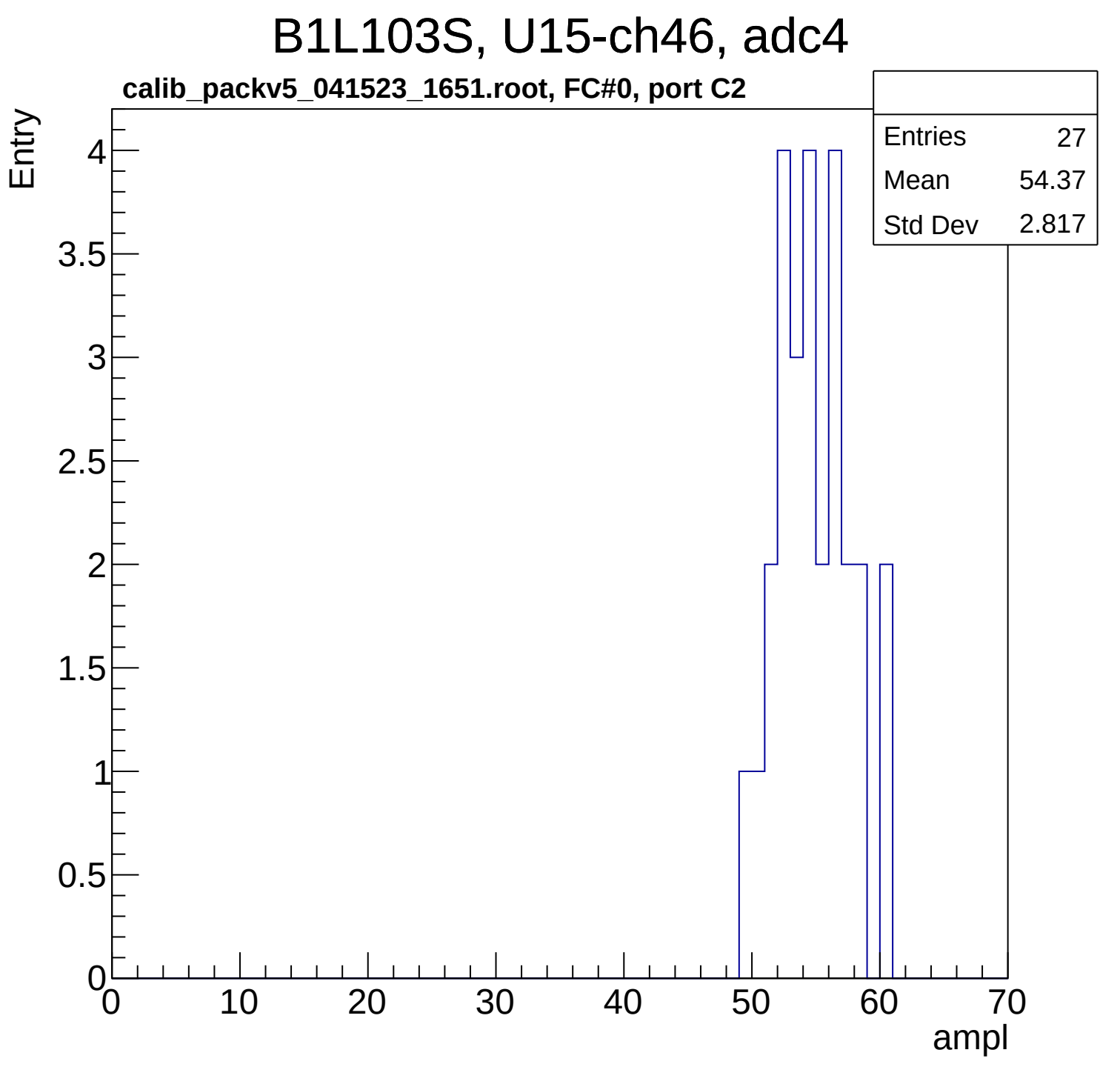

B1L103S, U15-ch45, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 3
Std Dev 6.708
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

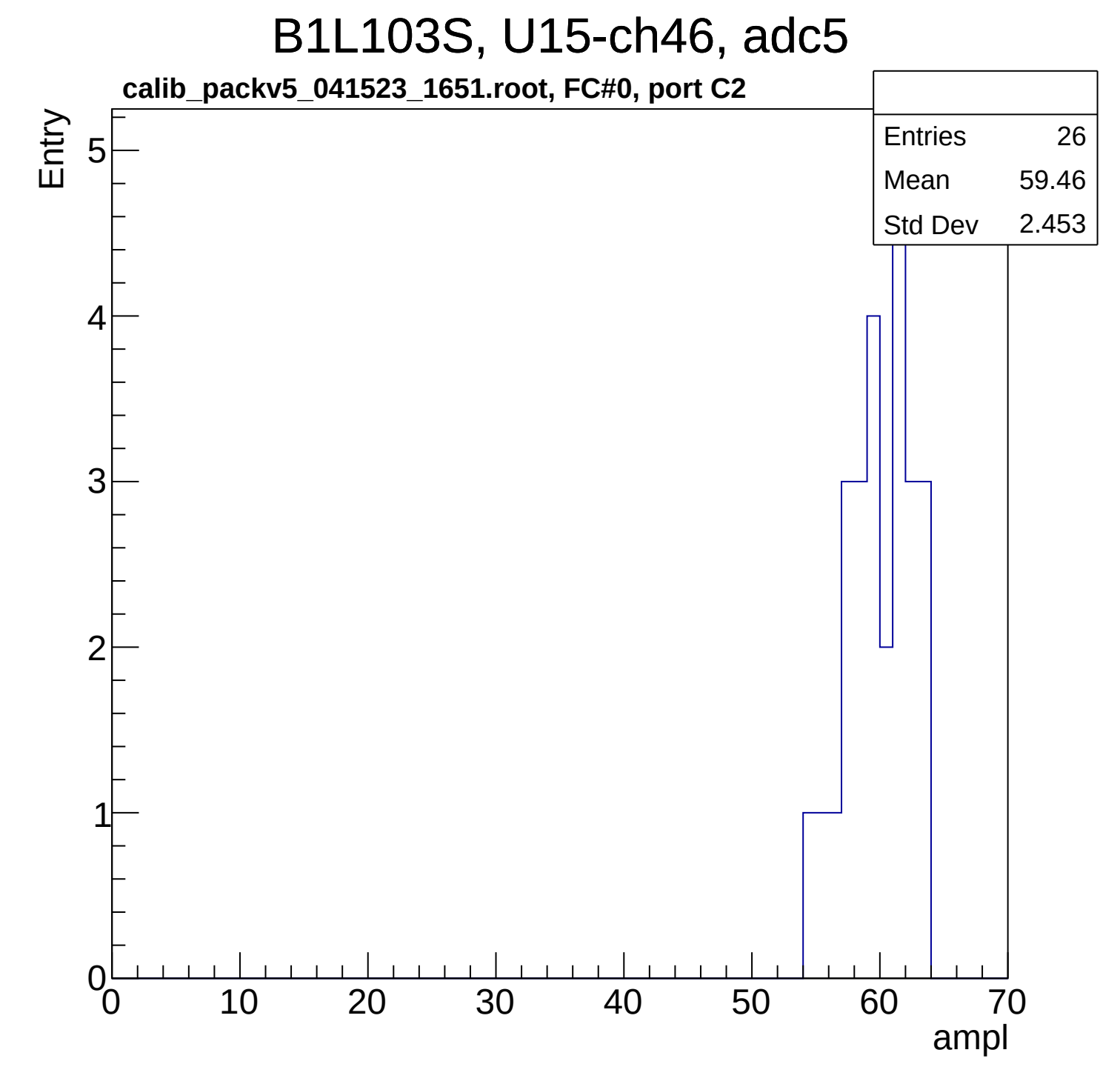

B1L103S, U15-ch46, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 23.67
Std Dev 10.66
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

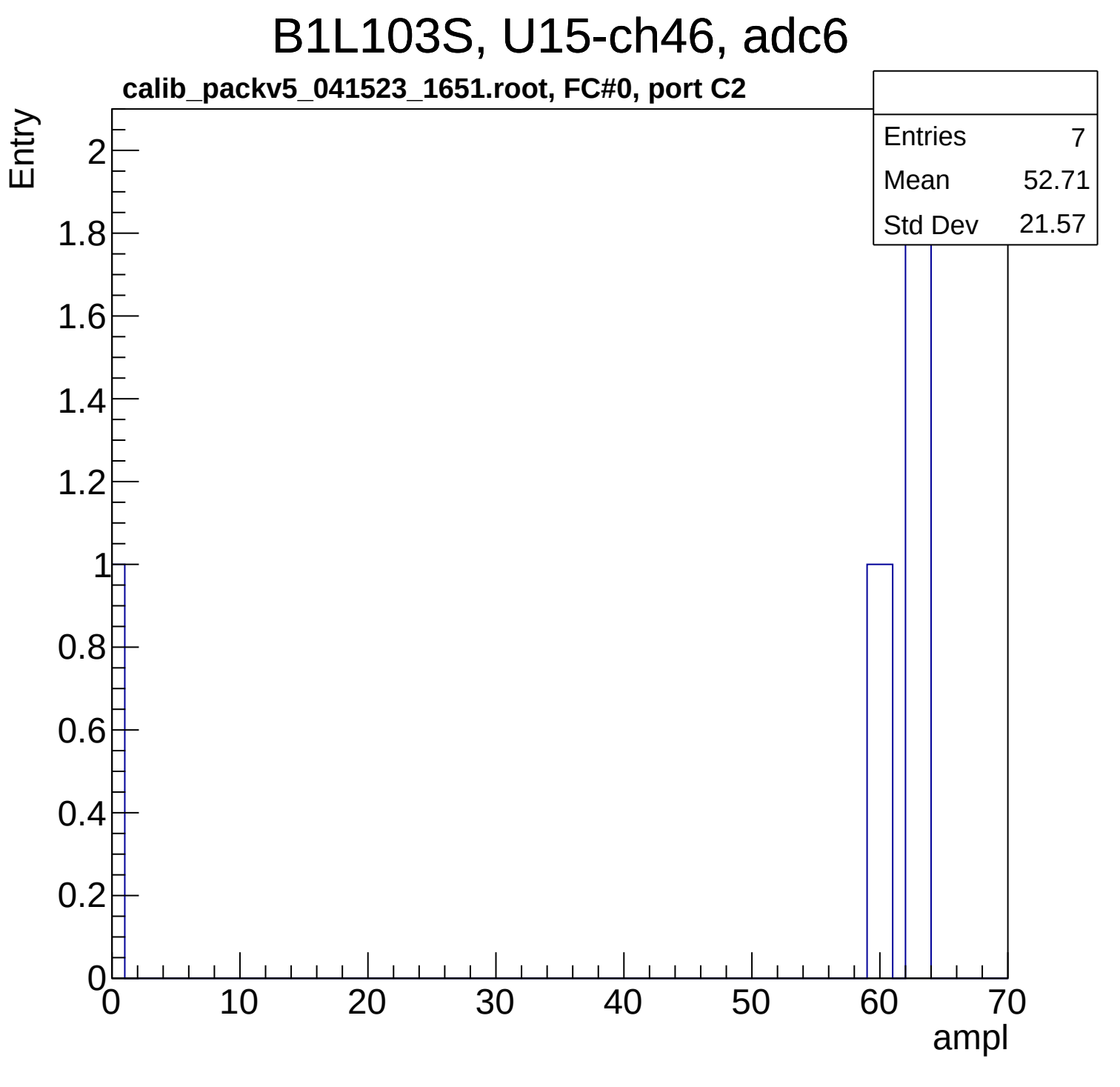

B1L103S, U15-ch46, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 34.65
Std Dev 7.014
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

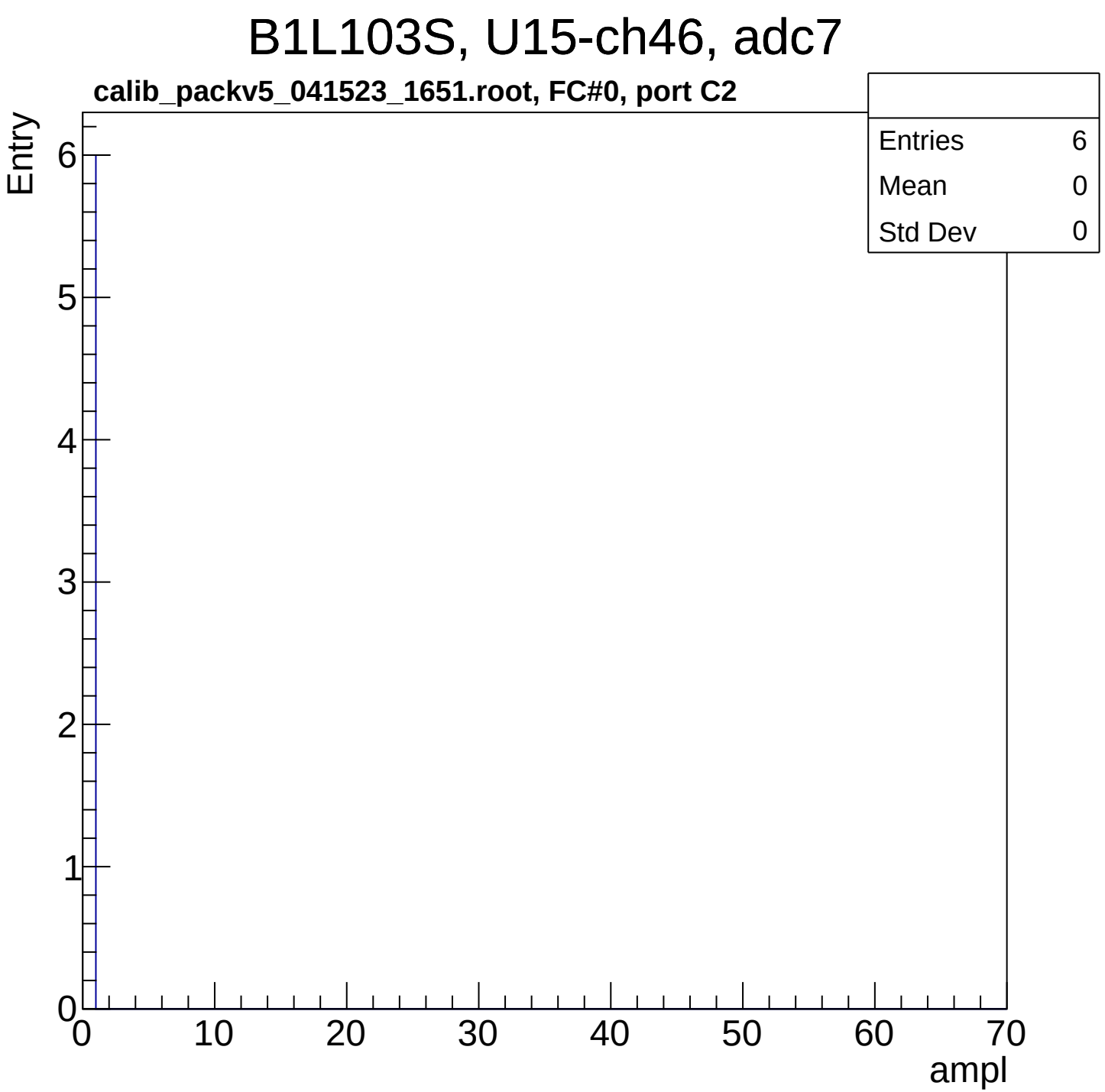

B1L103S, U15-ch46, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 37.51
Std Dev 13.53
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

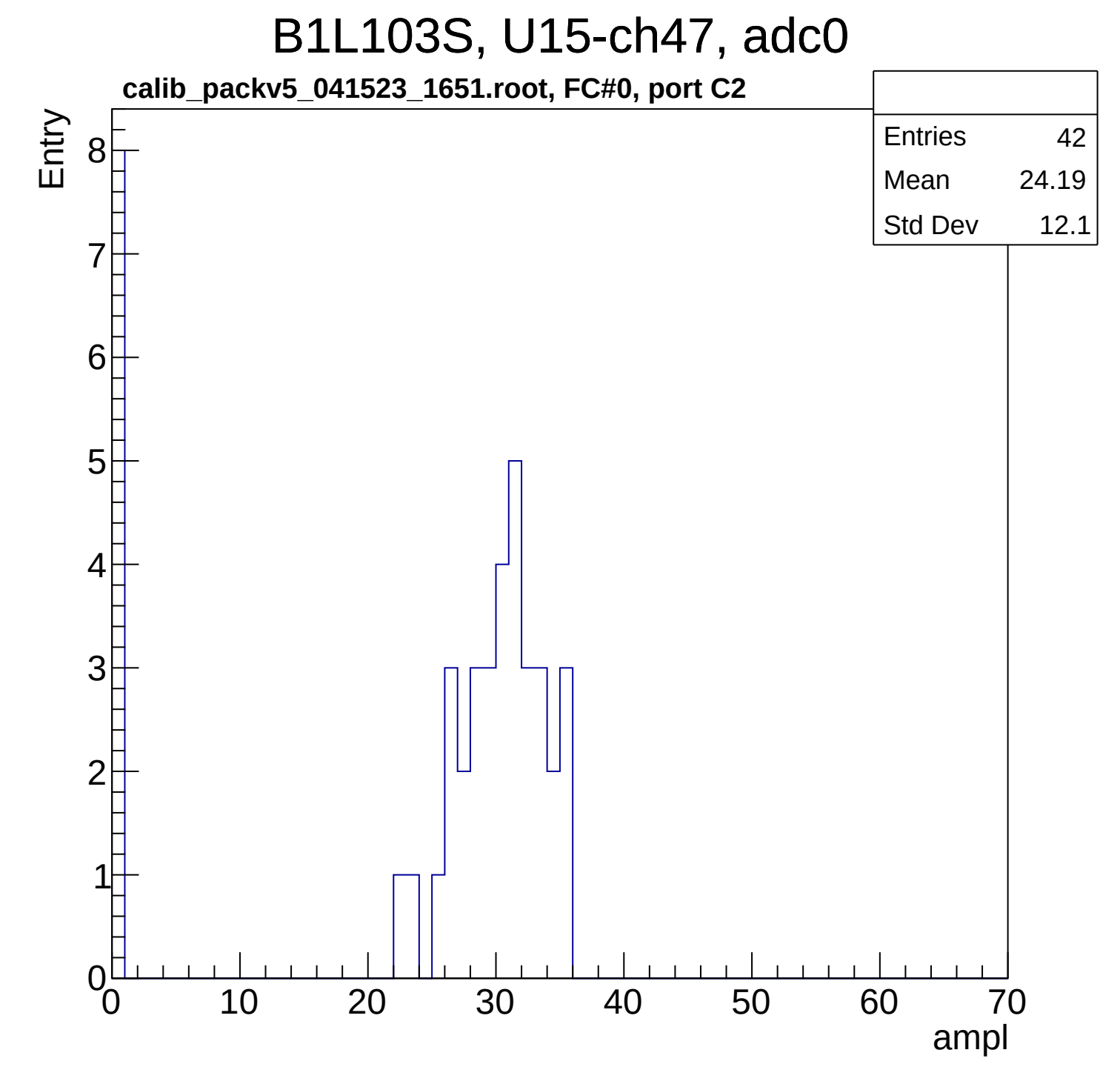

B1L103S, U15-ch46, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 39.72
Std Dev 19.31
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U15-ch46, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 54.37
Std Dev 2.817
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch46, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 59.46
Std Dev 2.453
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch46, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 52.71
Std Dev 21.57
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U15-ch46, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 0
Std Dev 0
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch47, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 24.19
Std Dev 12.1
Entry
ampl
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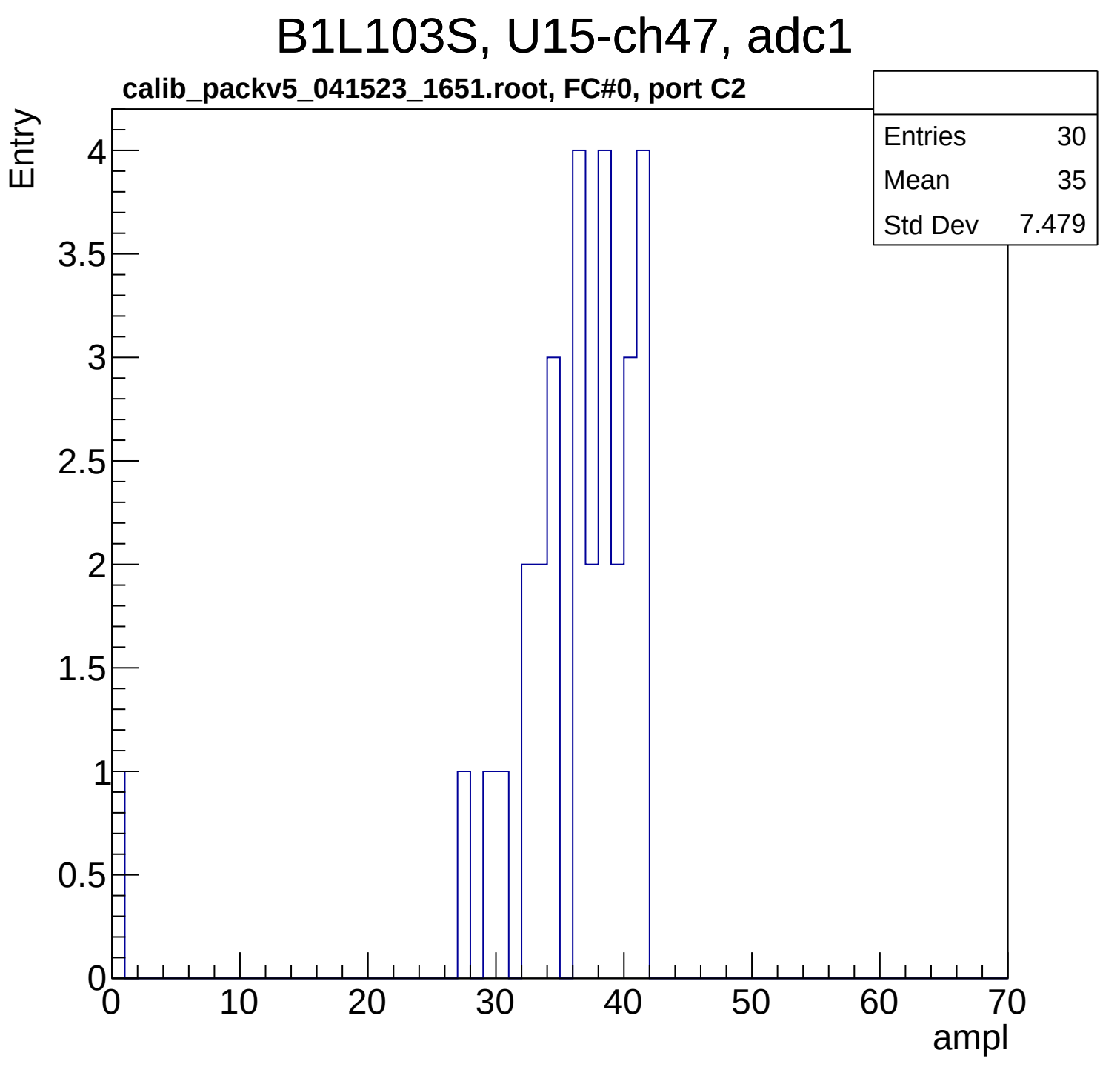
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U15-ch47, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 35
Std Dev 7.479
Entry
ampl
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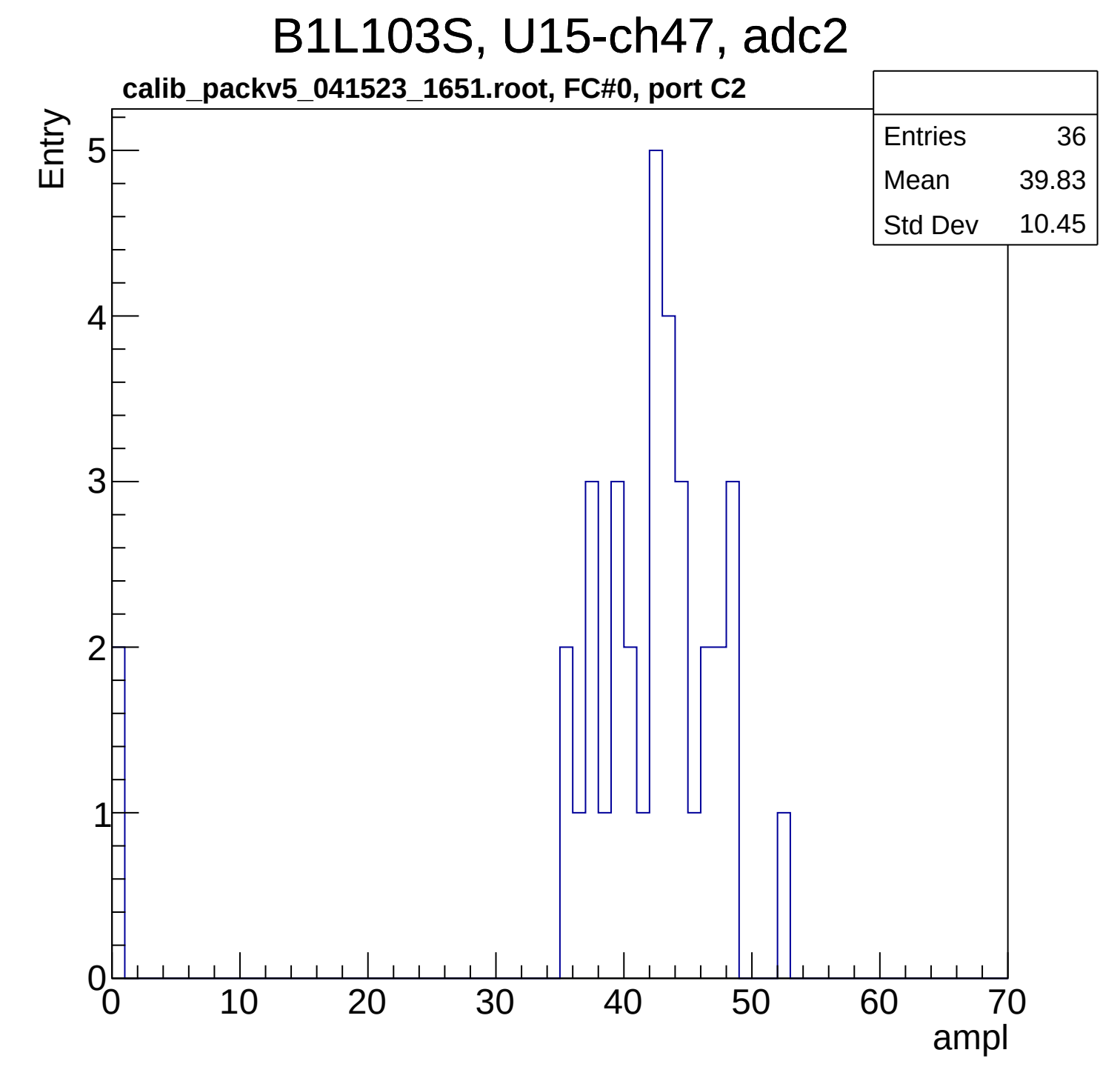
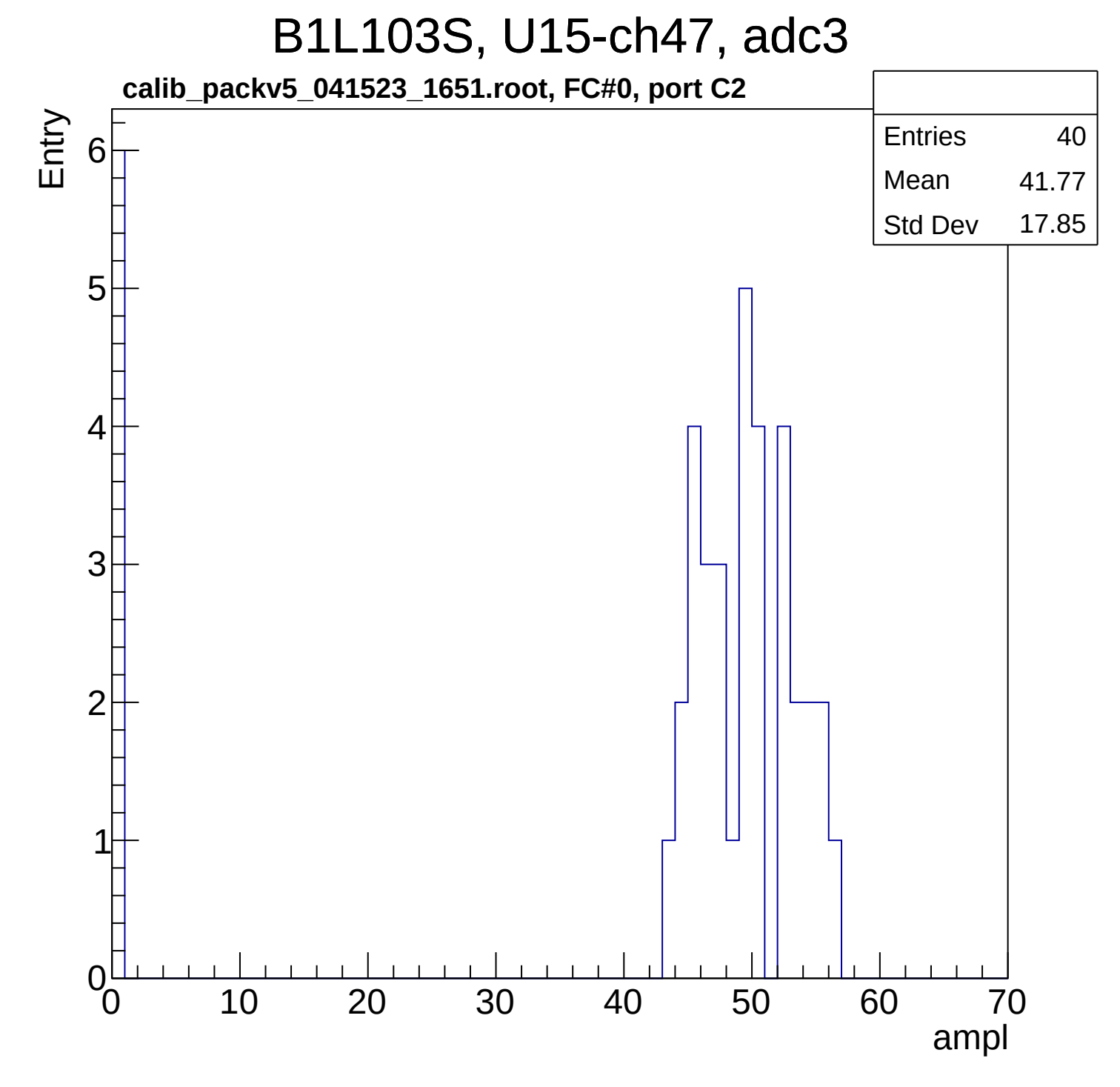
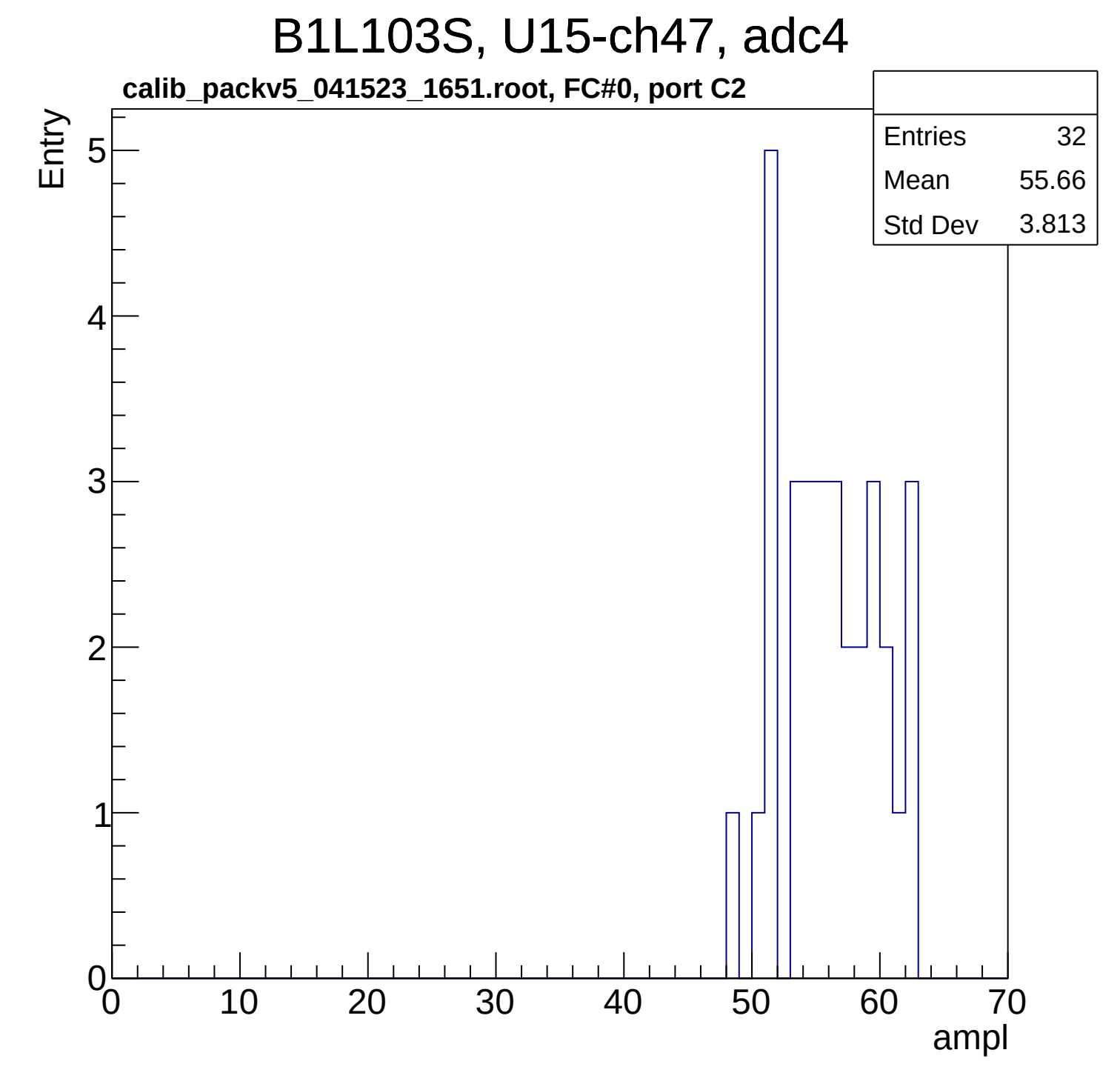
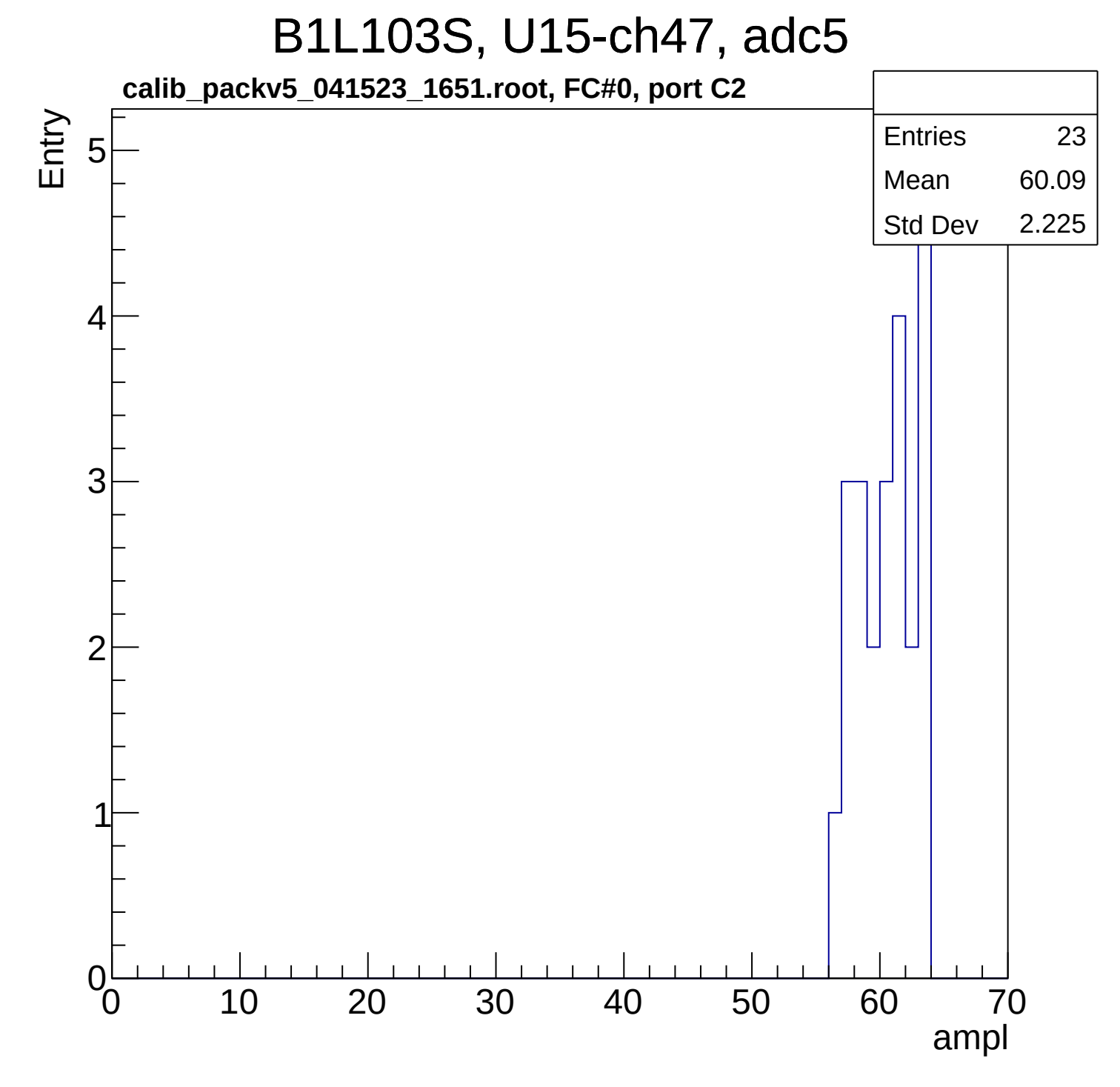
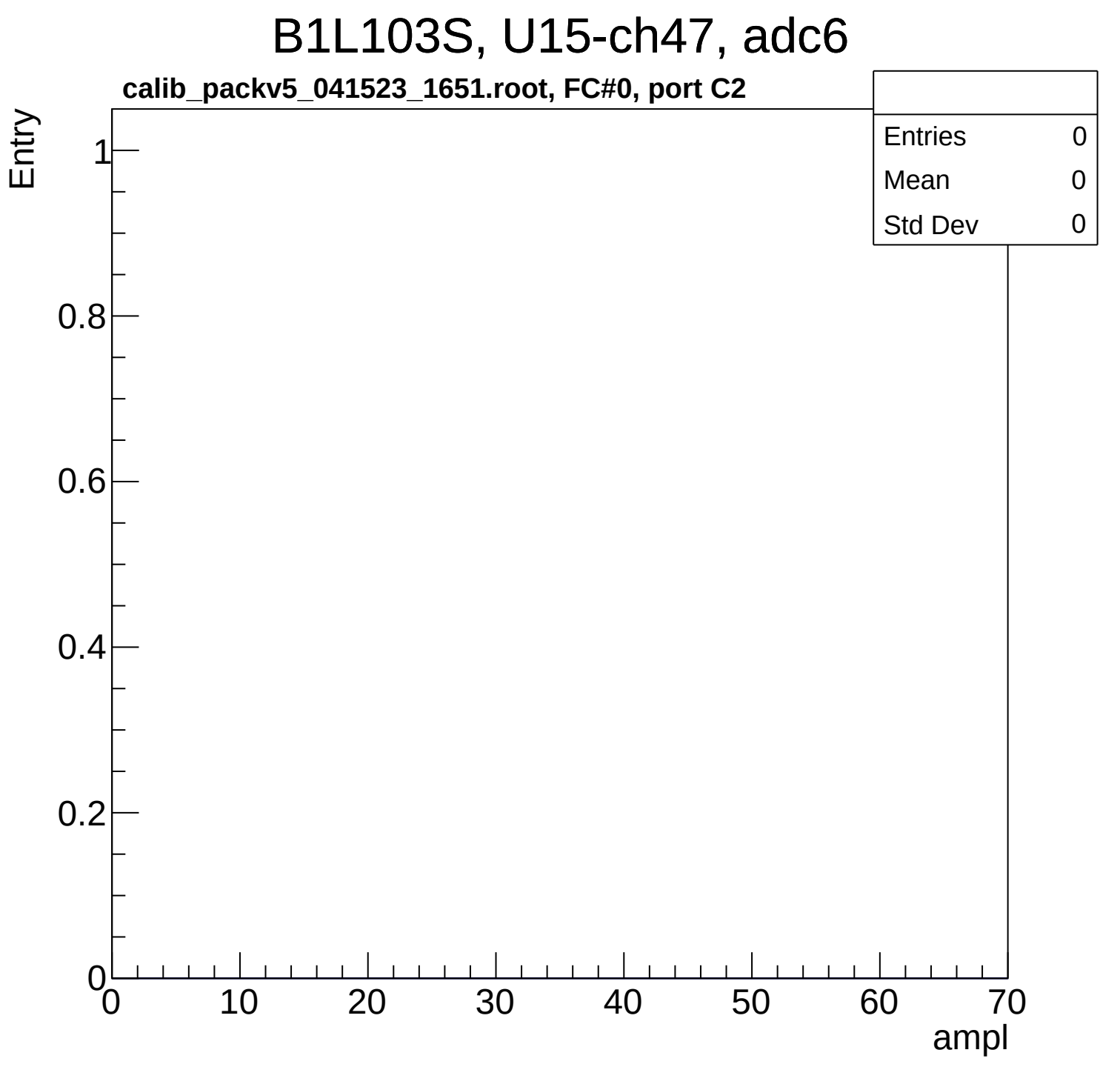
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch47, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 39.83
Std Dev 10.45
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch47, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 41.77
Std Dev 17.85
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch47, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 55.66
Std Dev 3.813
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch47, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 60.09
Std Dev 2.225
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch47, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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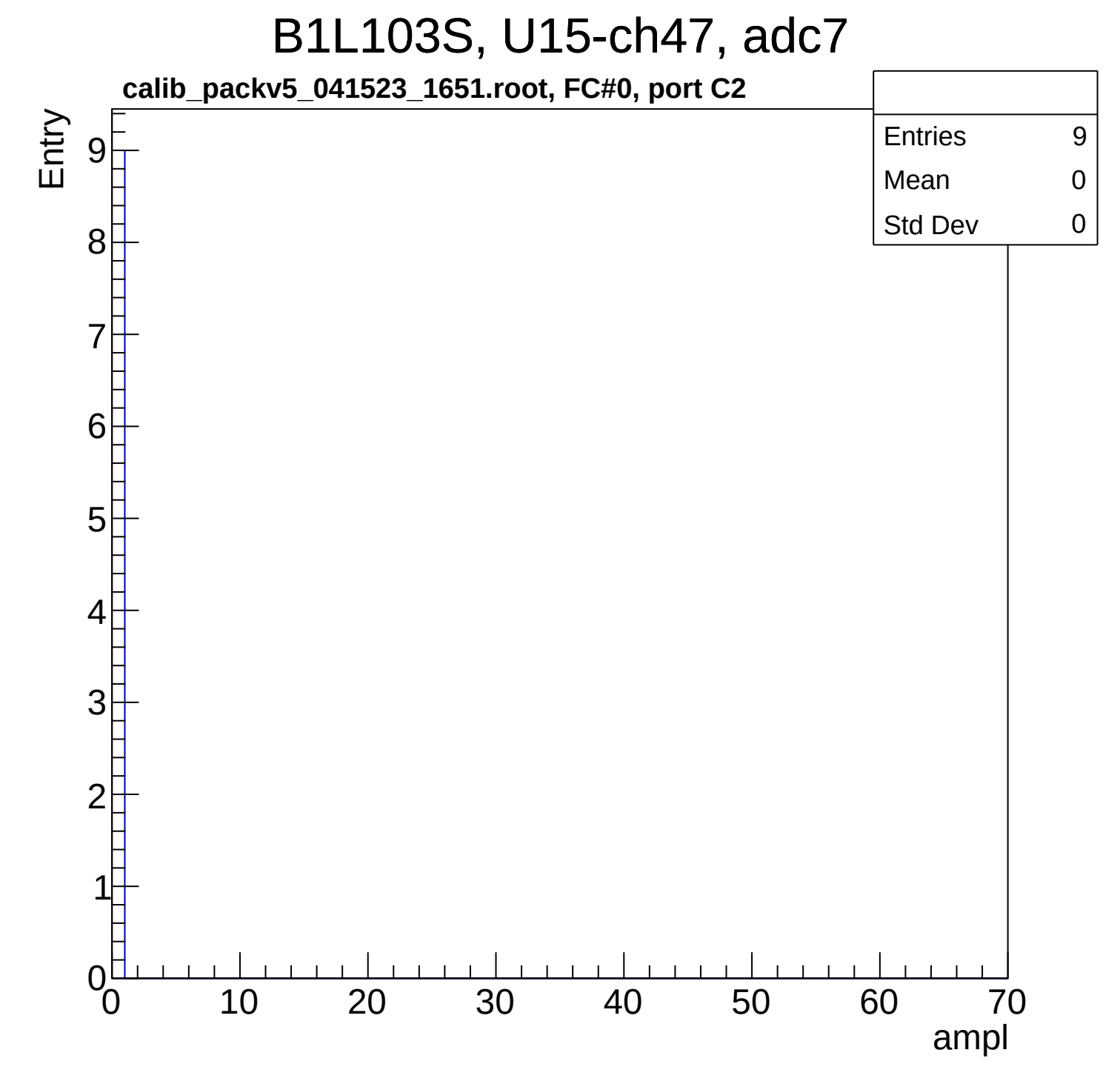
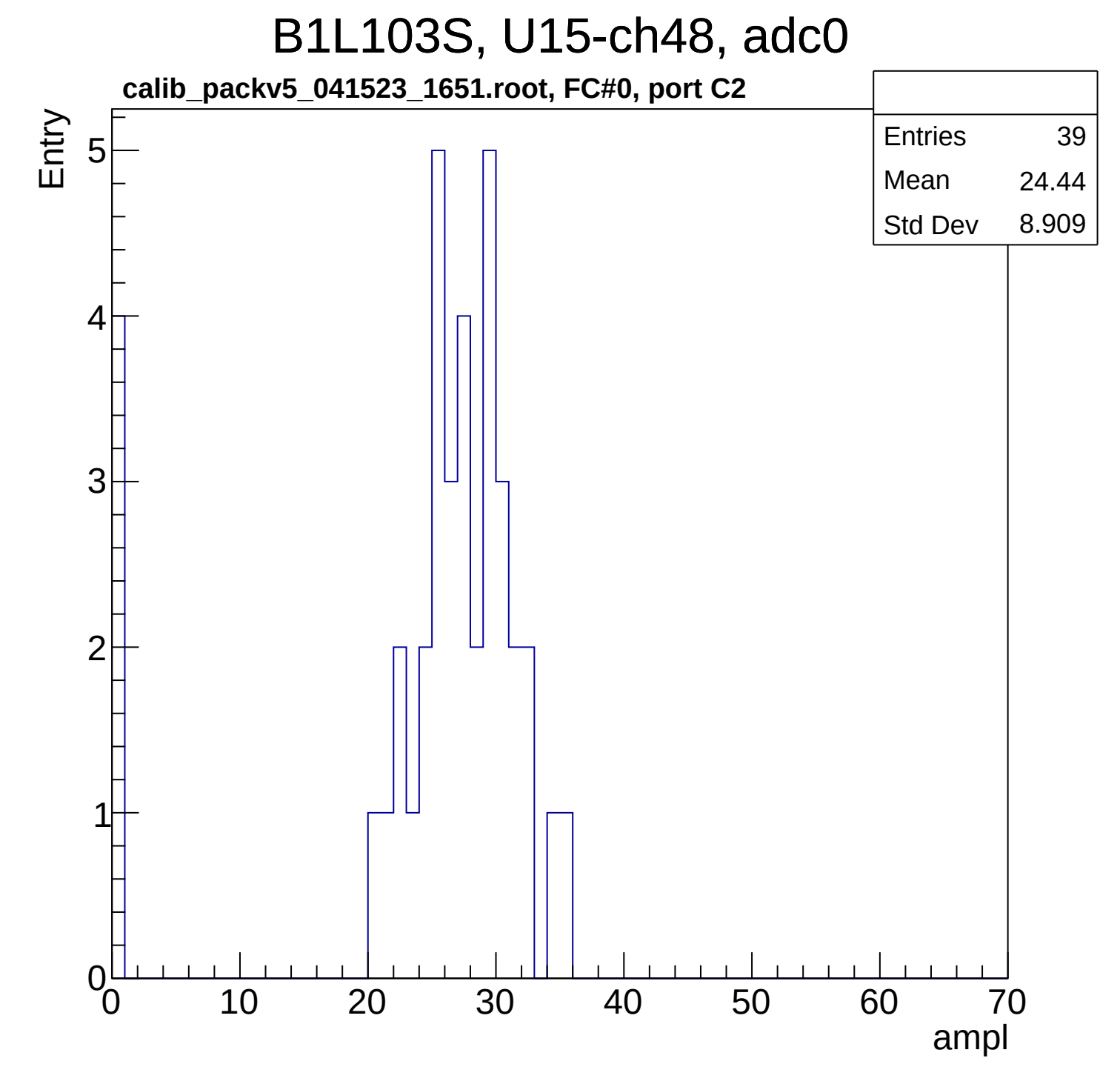
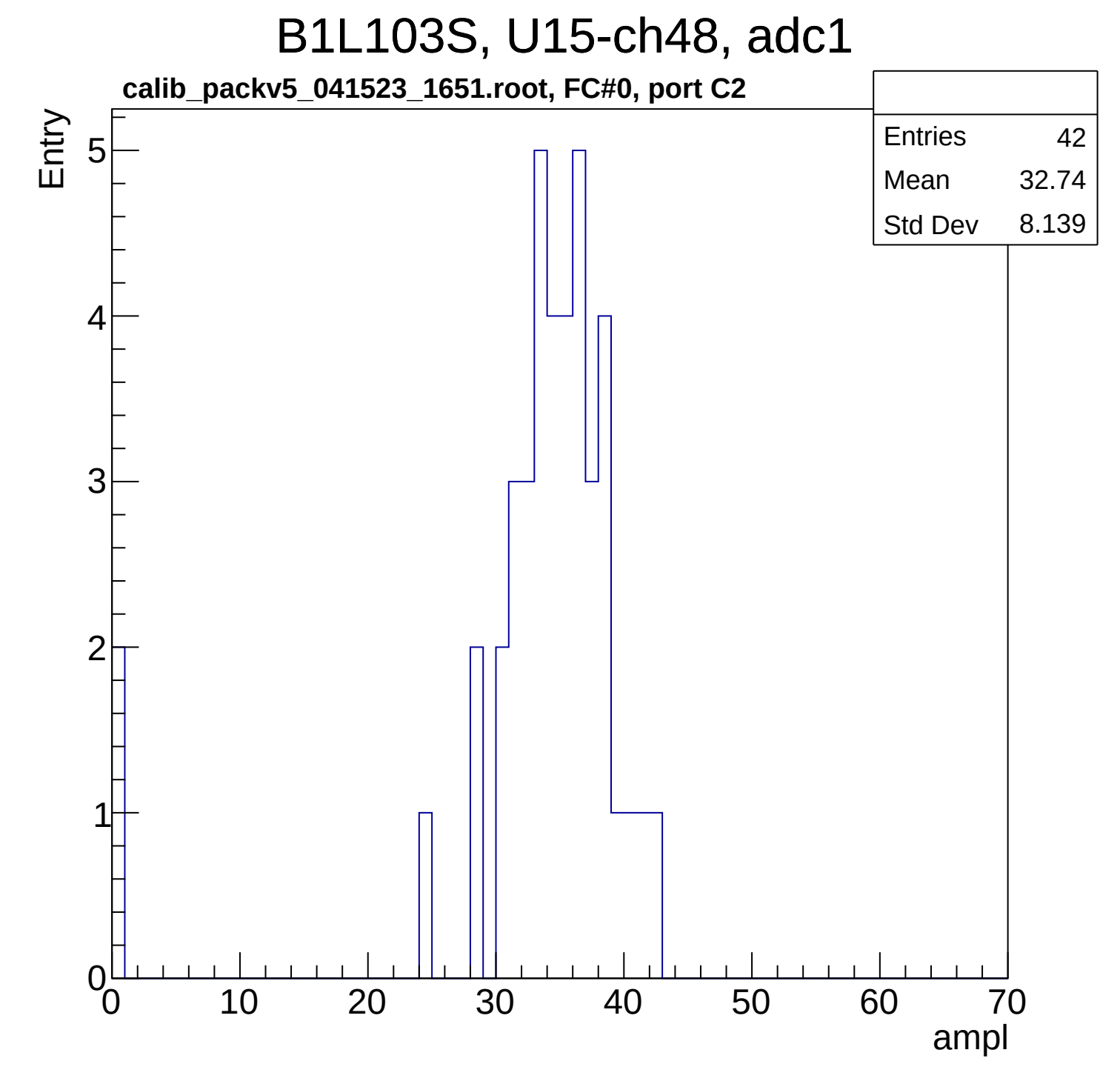
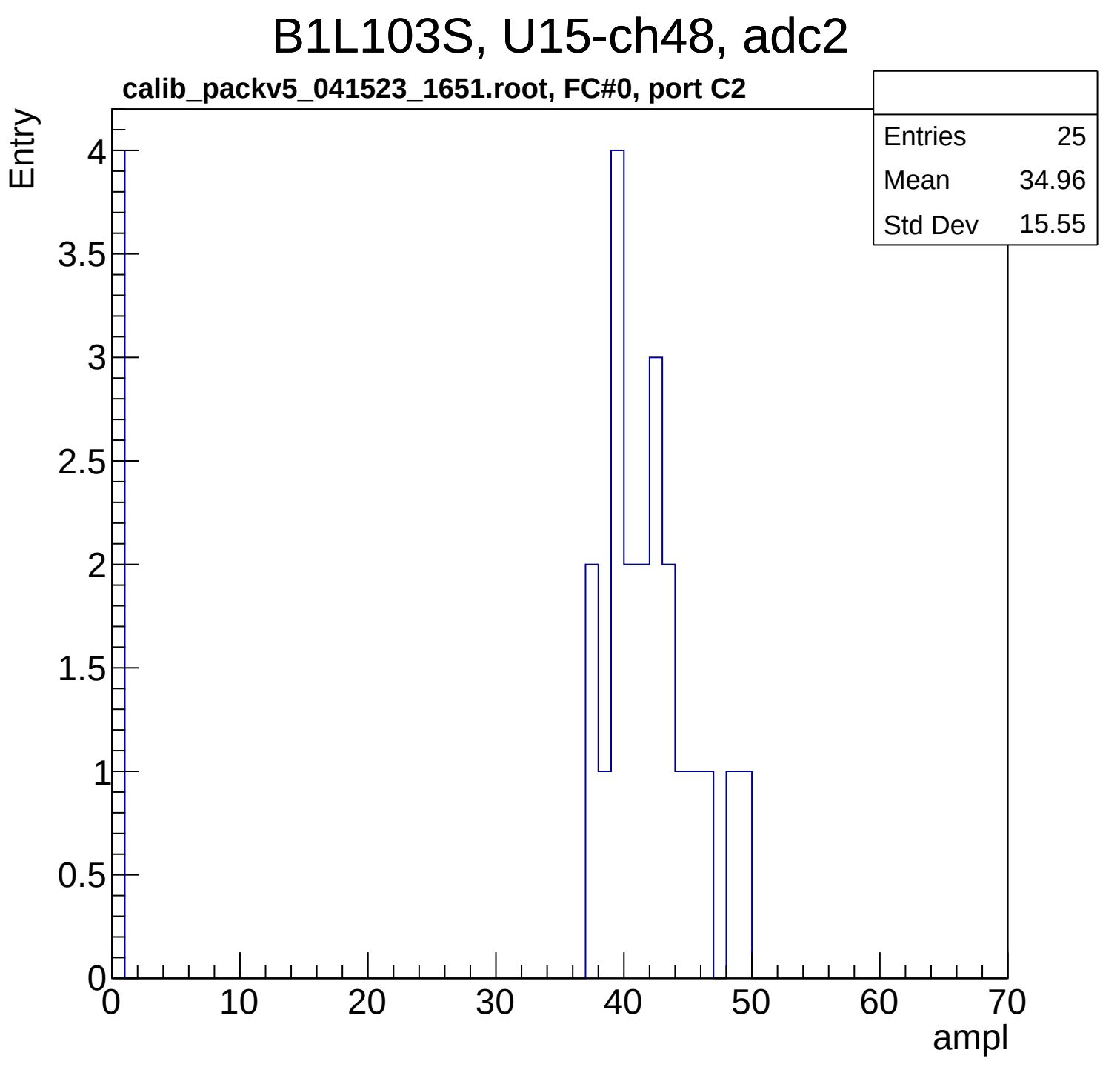
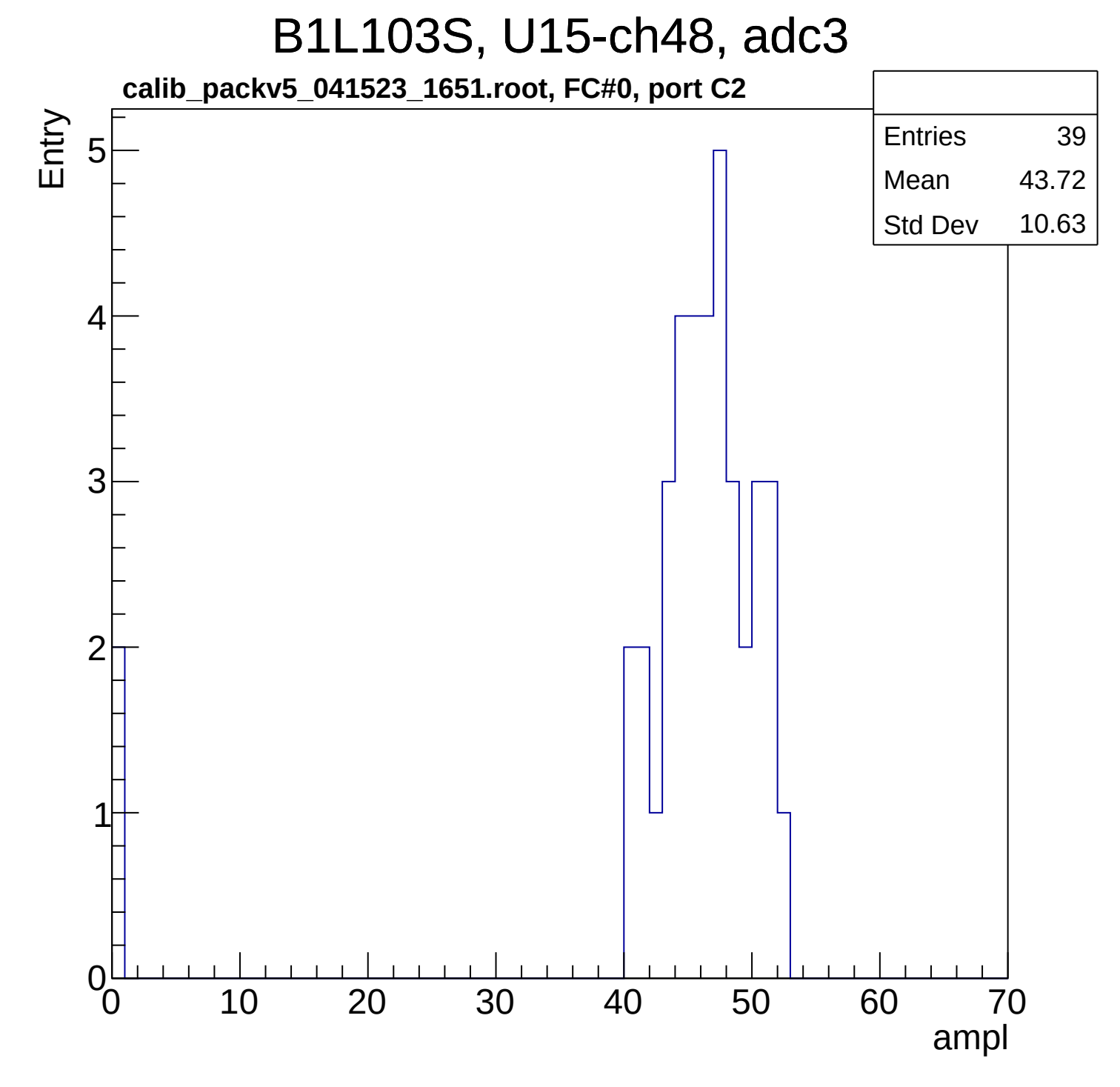
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

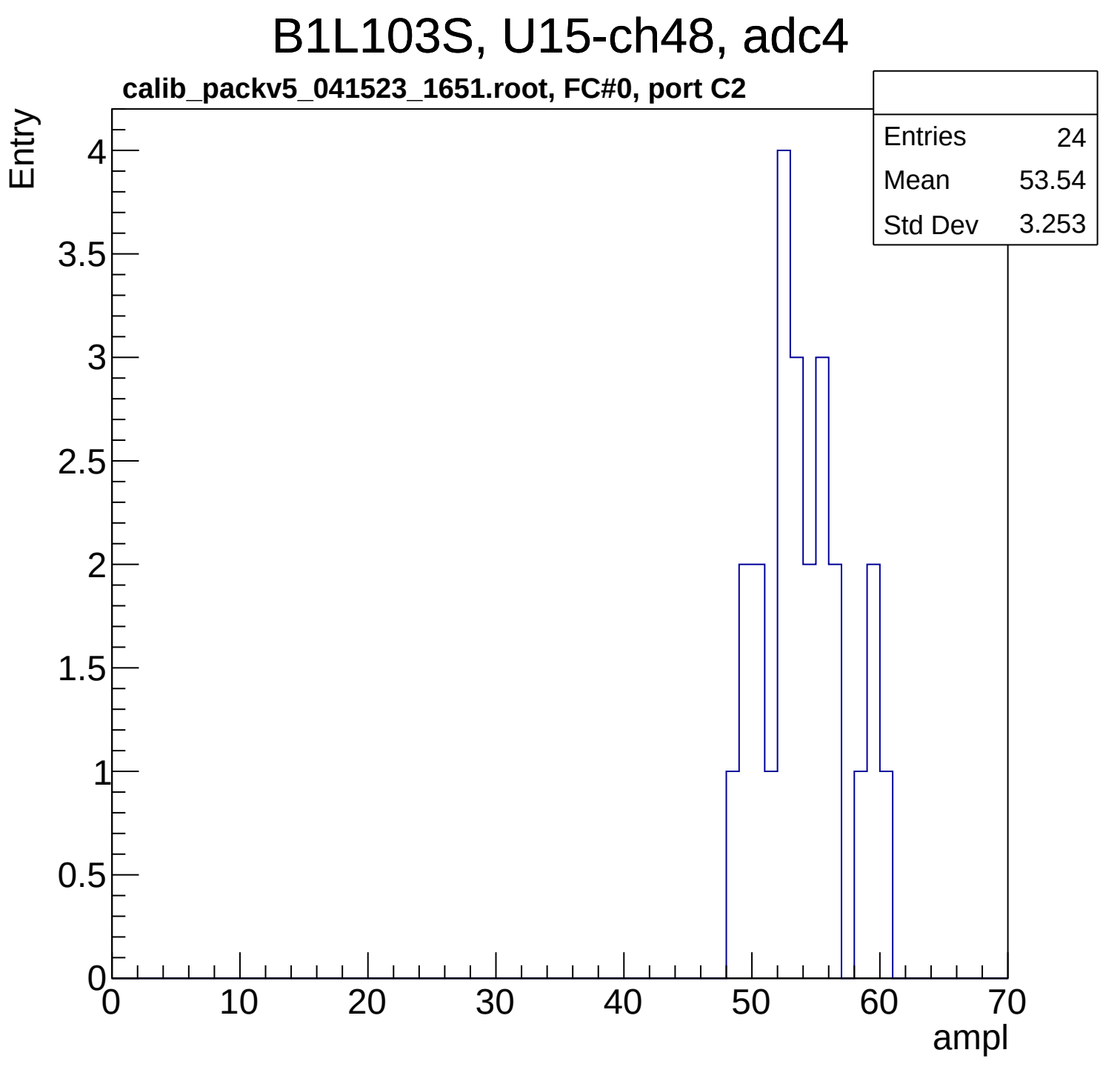

B1L103S, U15-ch47, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 0
Std Dev 0
Entry
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch48, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 24.44
Std Dev 8.909
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch48, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 32.74
Std Dev 8.139
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch48, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 34.96
Std Dev 15.55
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch48, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 43.72
Std Dev 10.63
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch48, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 53.54
Std Dev 3.253
Entry
ampl
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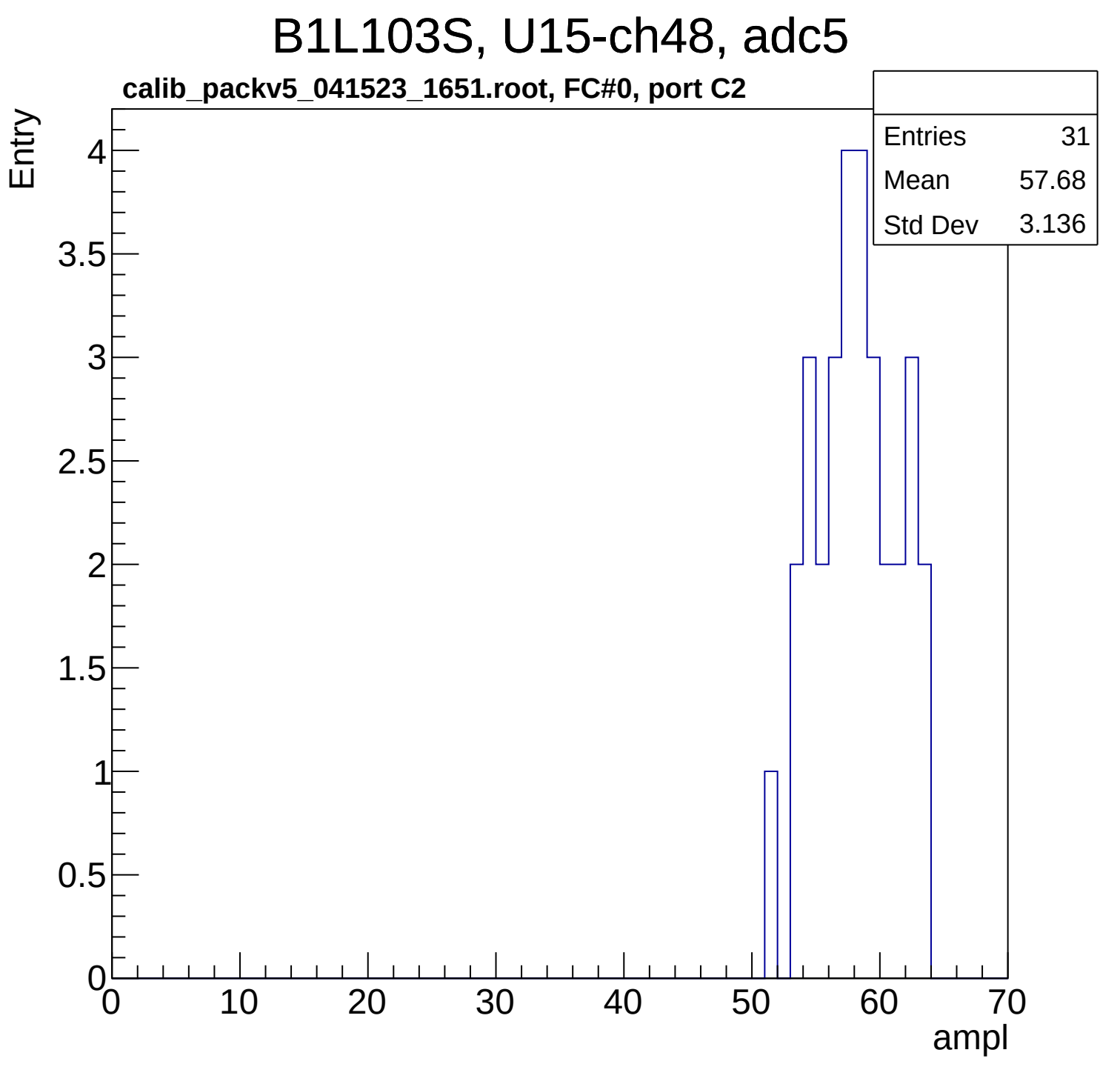
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch48, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 57.68
Std Dev 3.136
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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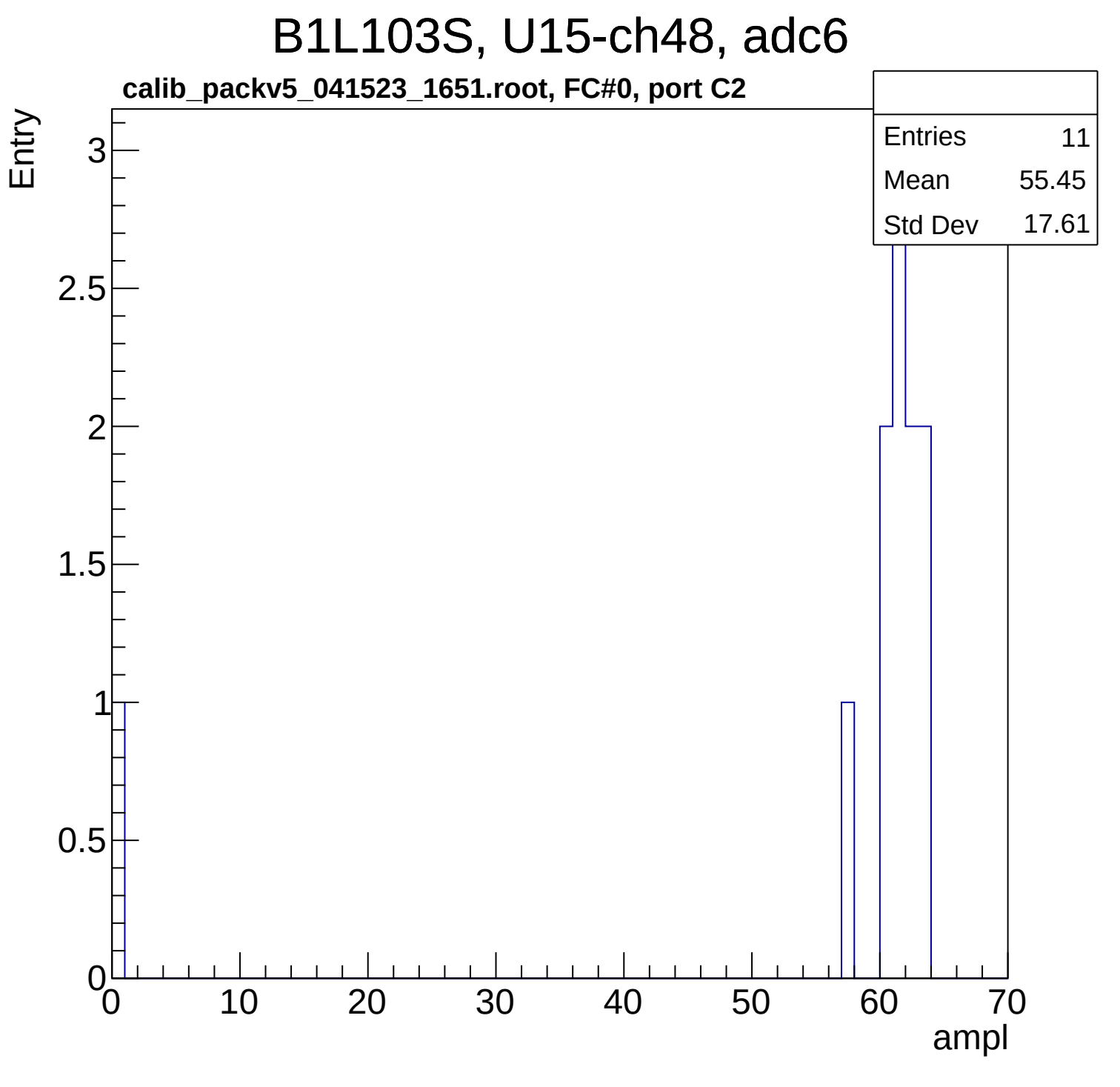
B1L103S, U15-ch48, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 55.45
Std Dev 17.61
Entry
ampl
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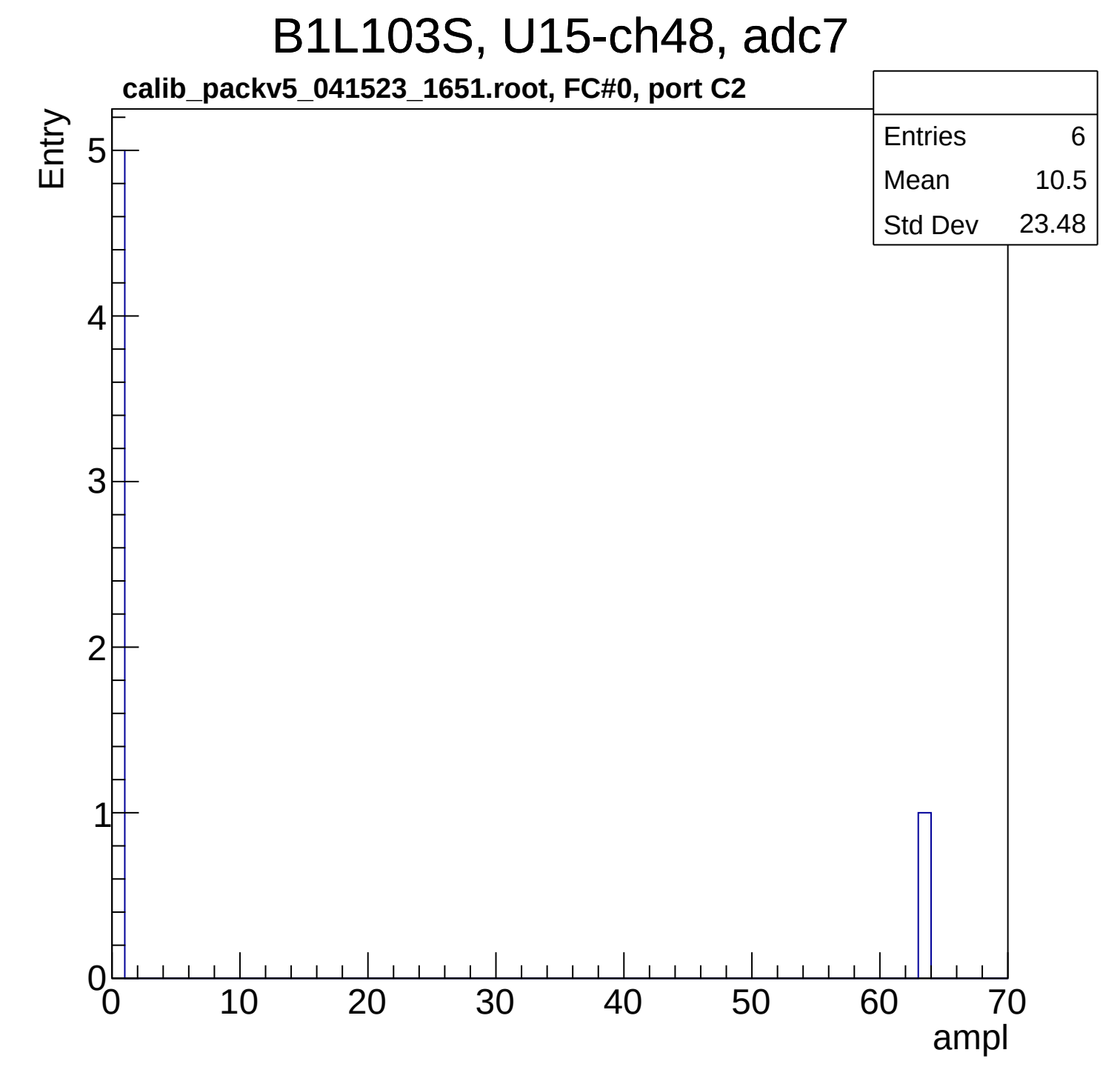
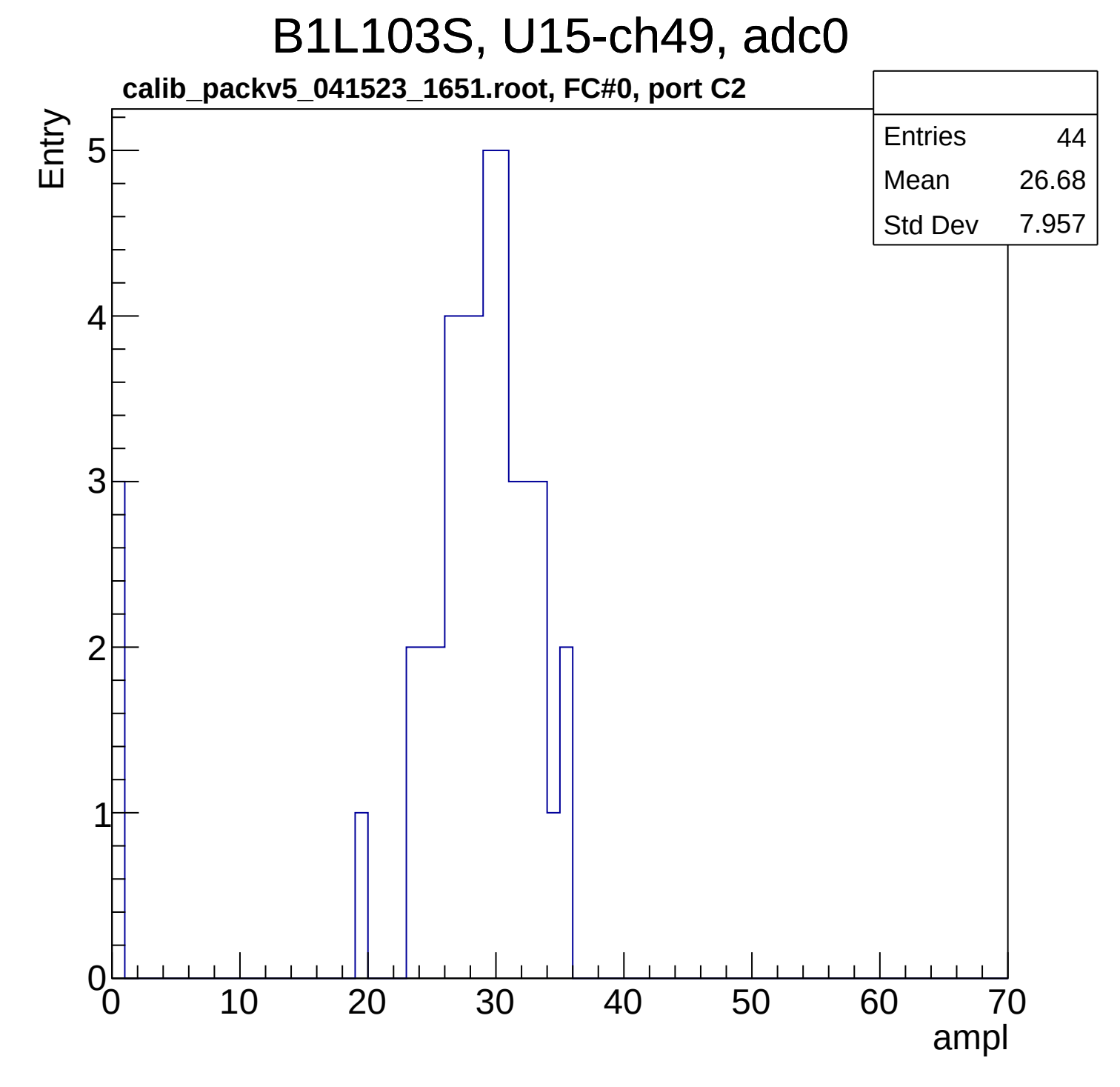
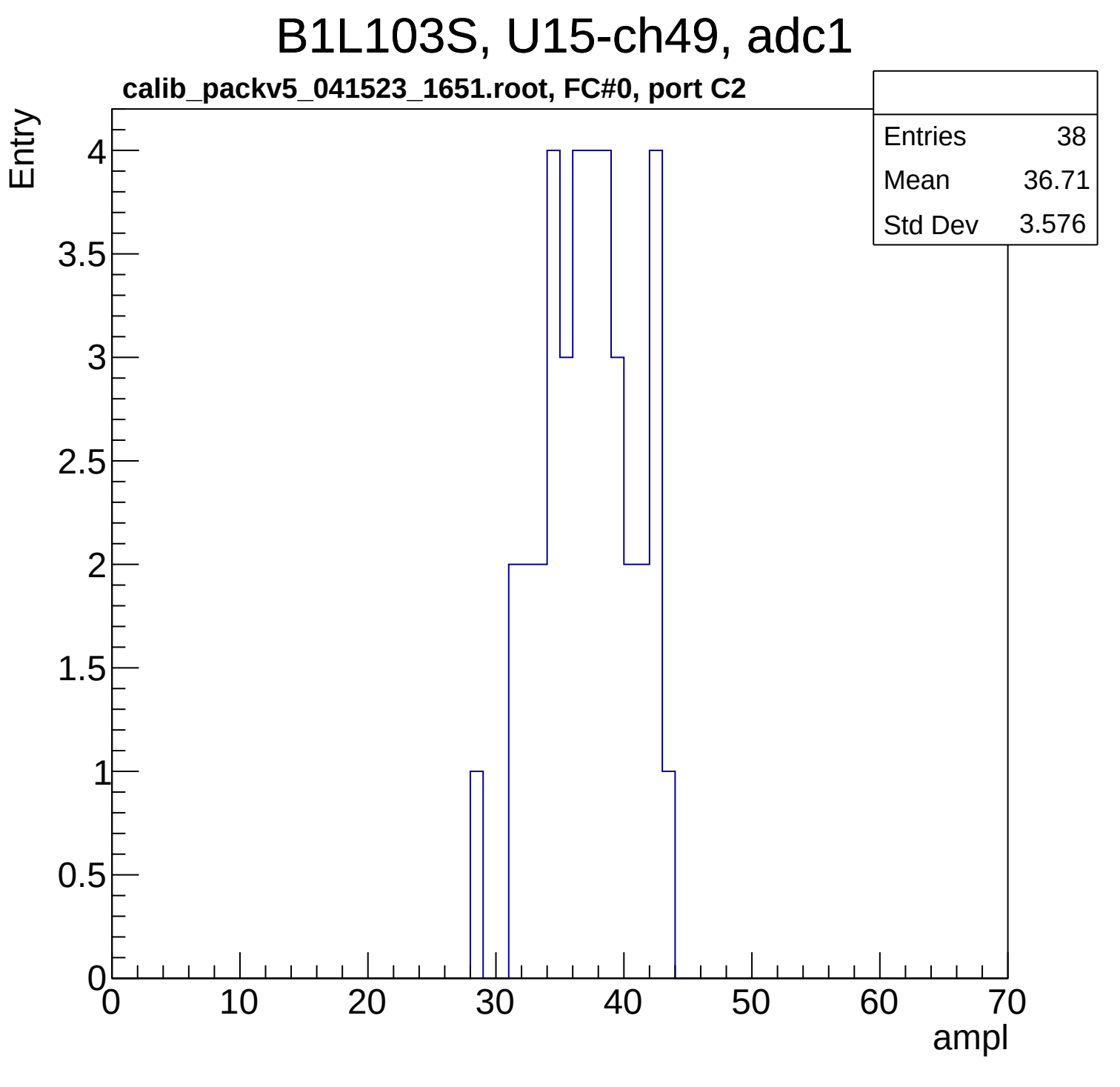
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch48, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 10.5
Std Dev 23.48
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch49, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 26.68
Std Dev 7.957
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch49, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 36.71
Std Dev 3.576
Entry
ampl
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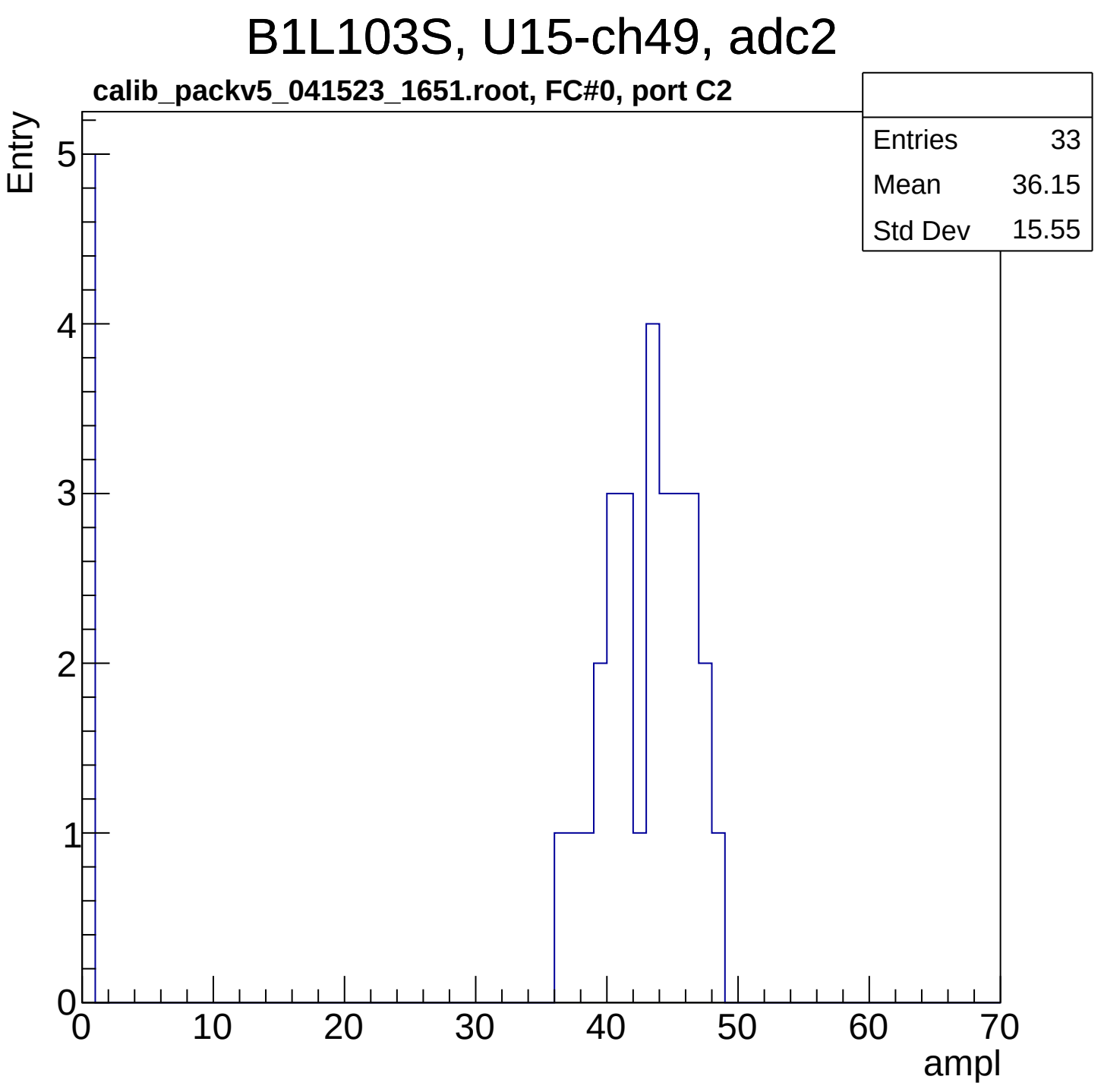
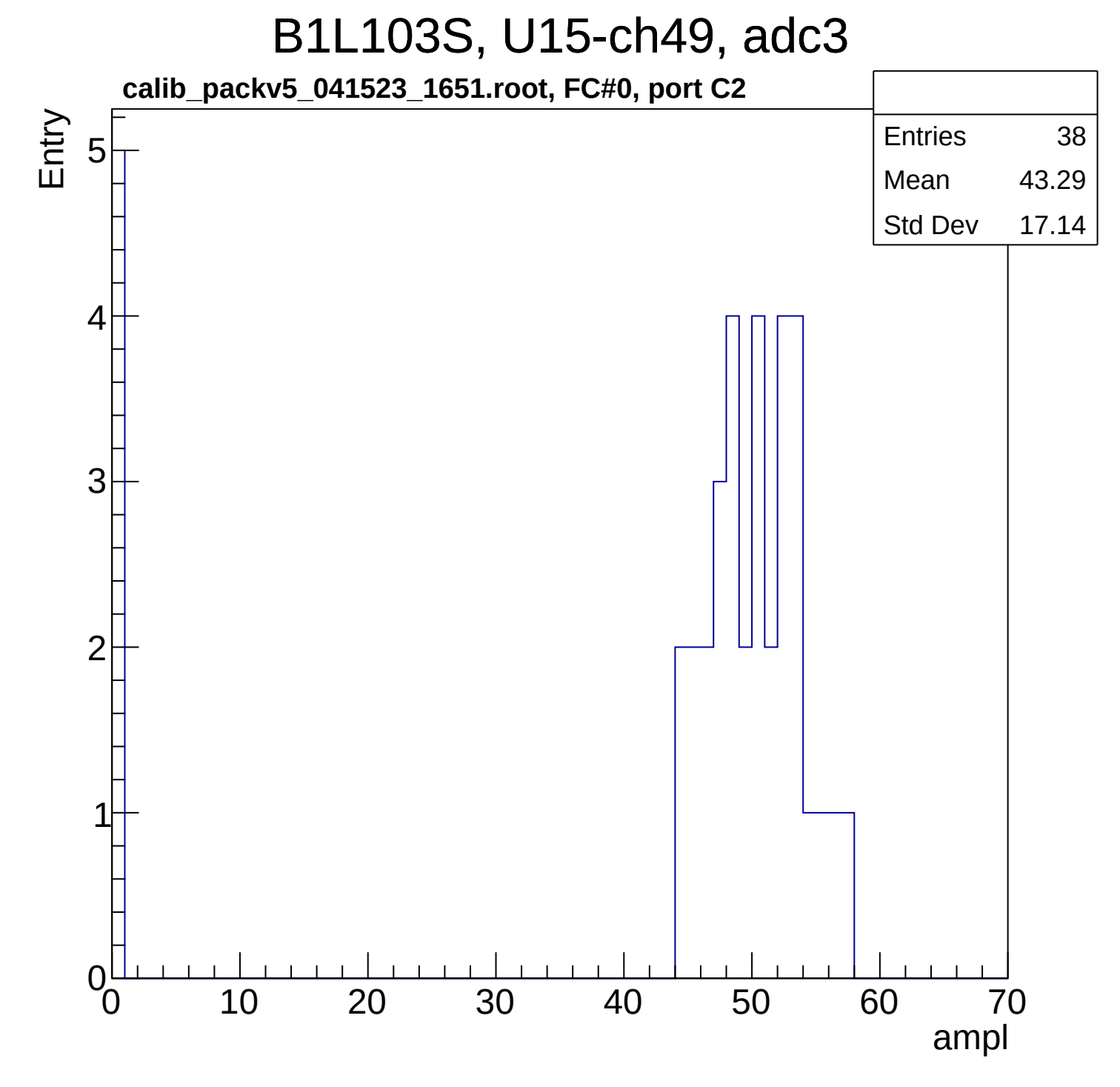
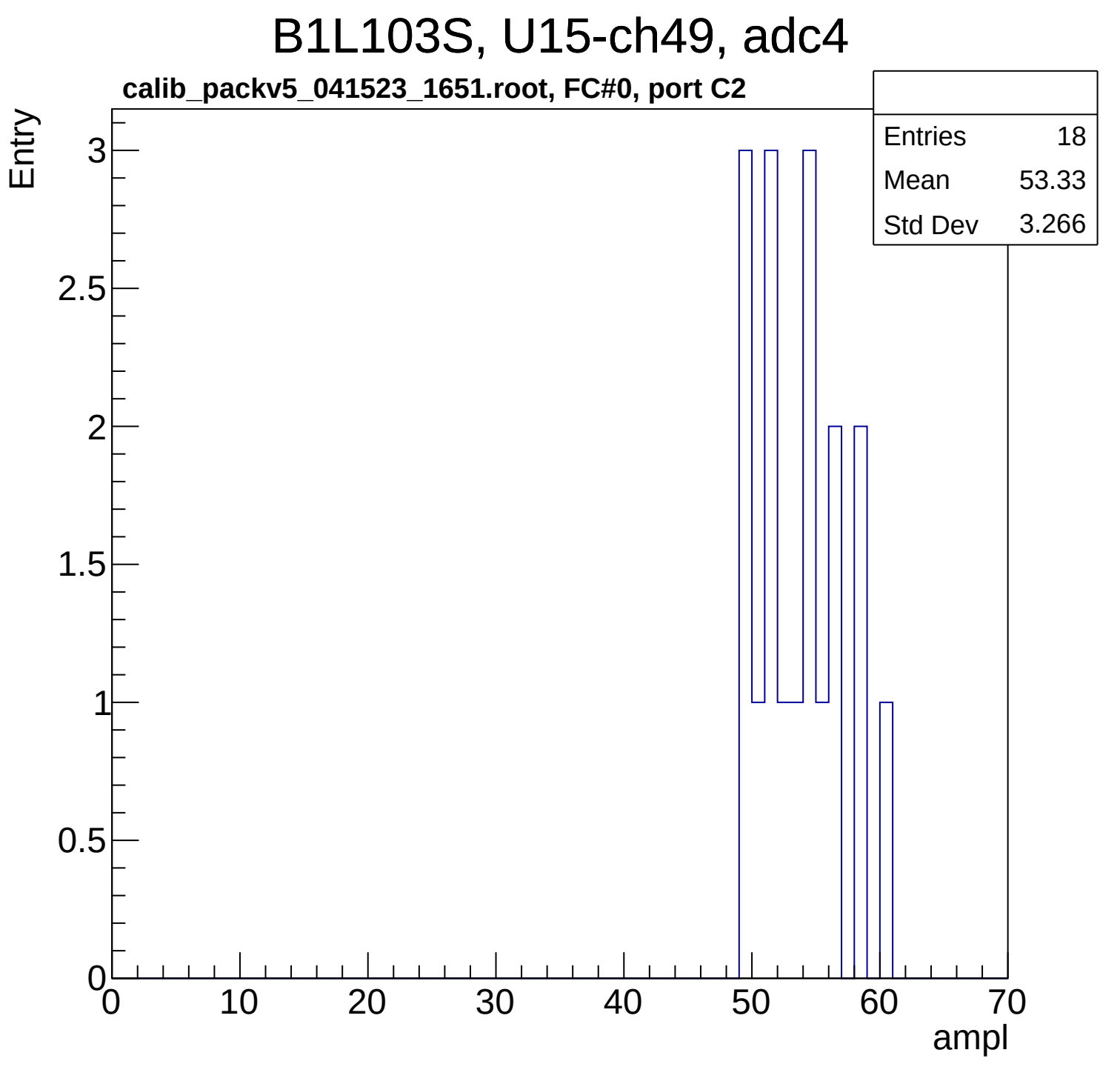
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch49, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 36.15
Std Dev 15.55
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch49, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 43.29
Std Dev 17.14
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch49, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 53.33
Std Dev 3.266
Entry
ampl
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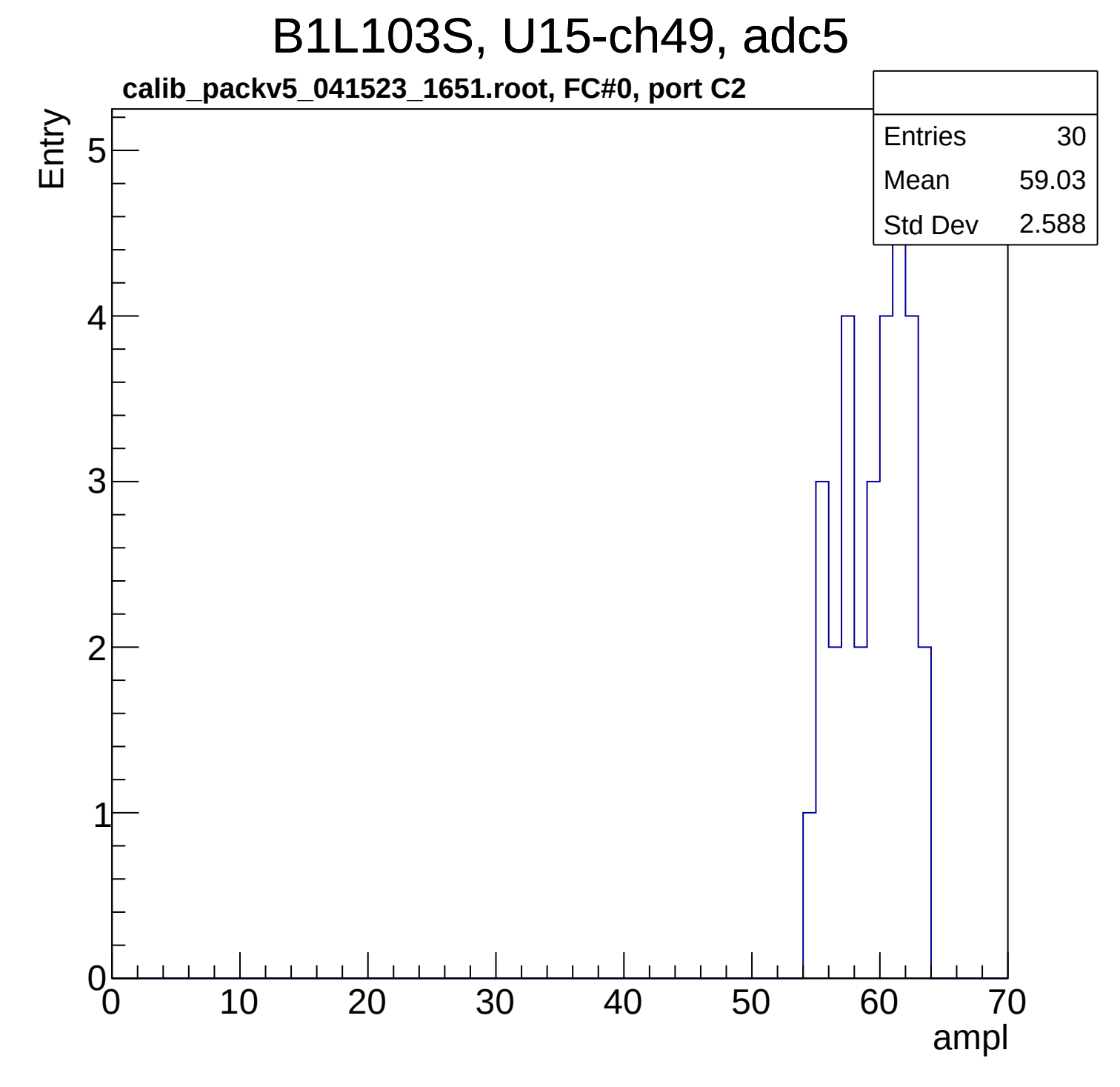
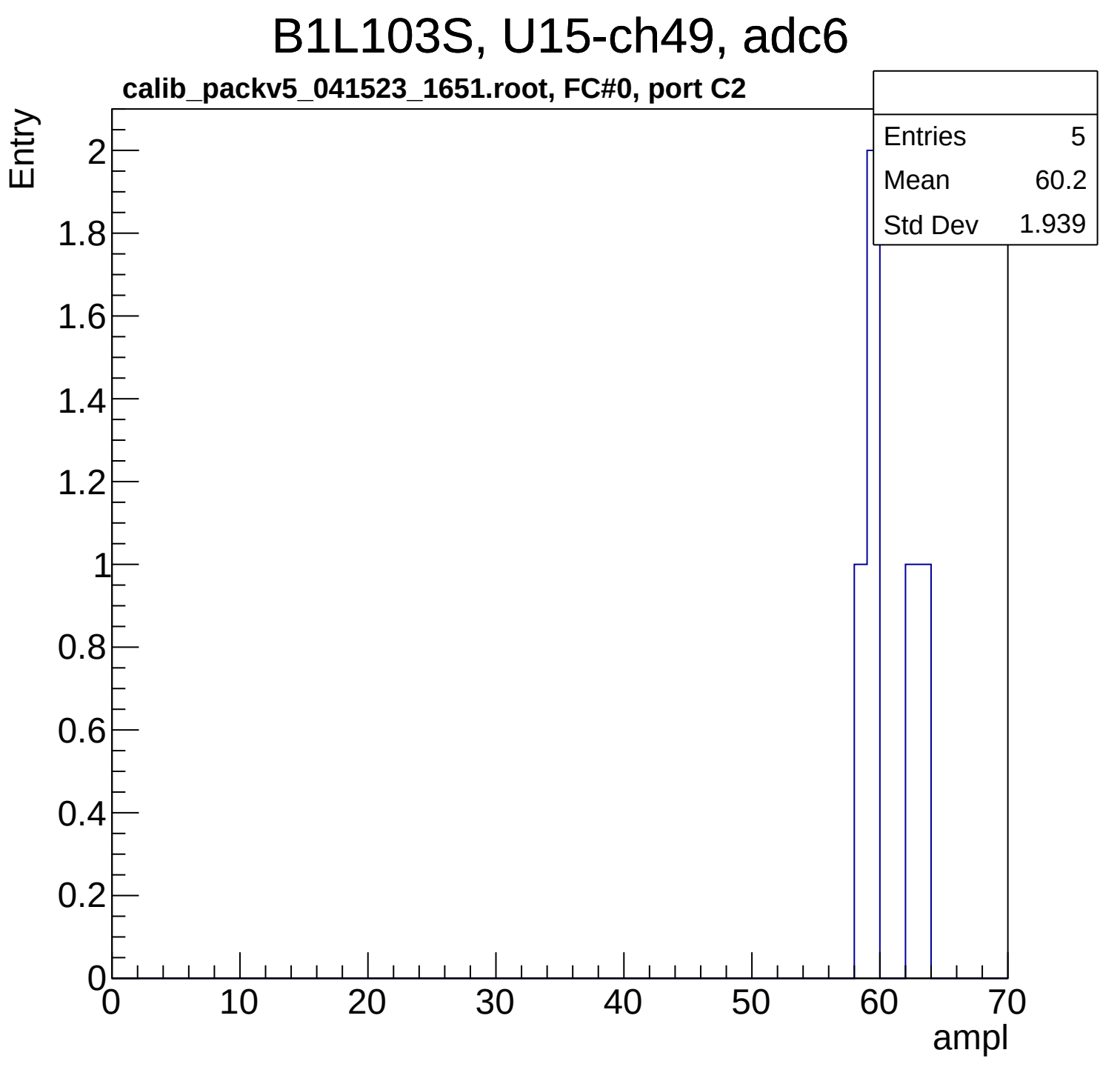
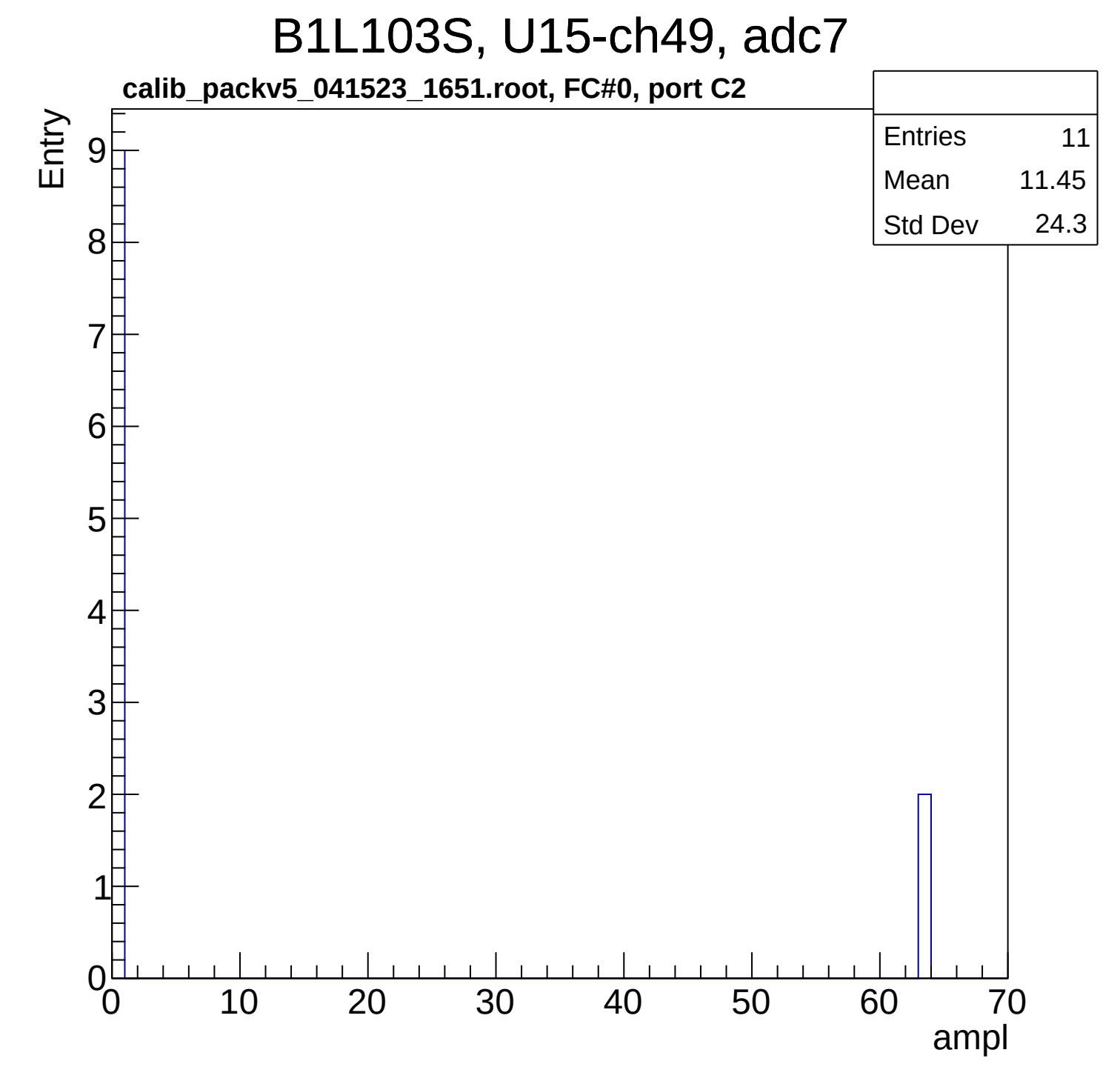
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch49, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 59.03
Std Dev 2.588
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch49, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 60.2
Std Dev 1.939
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U15-ch49, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 11.45
Std Dev 24.3
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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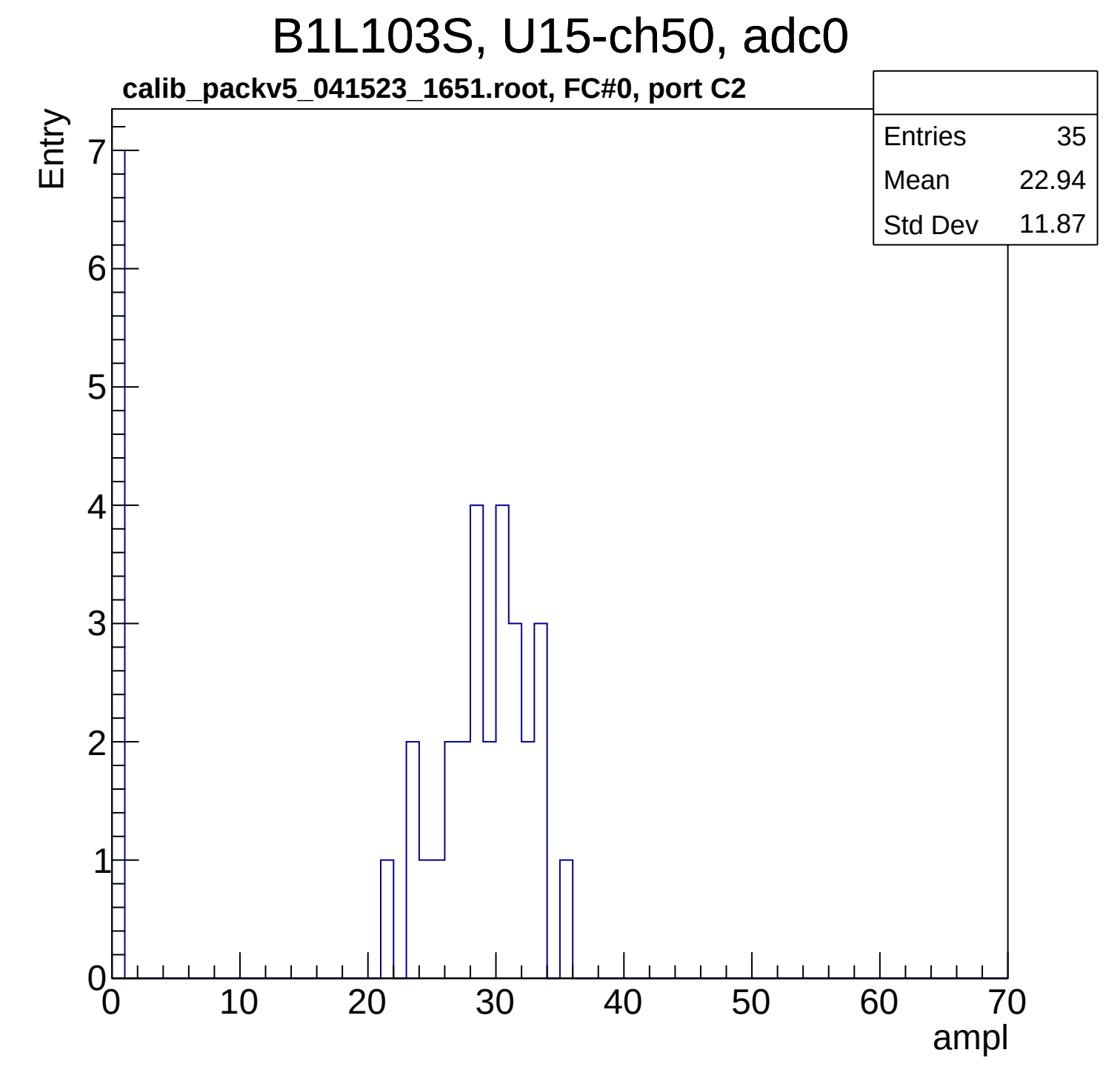
B1L103S, U15-ch50, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 22.94
Std Dev 11.87
Entry
ampl
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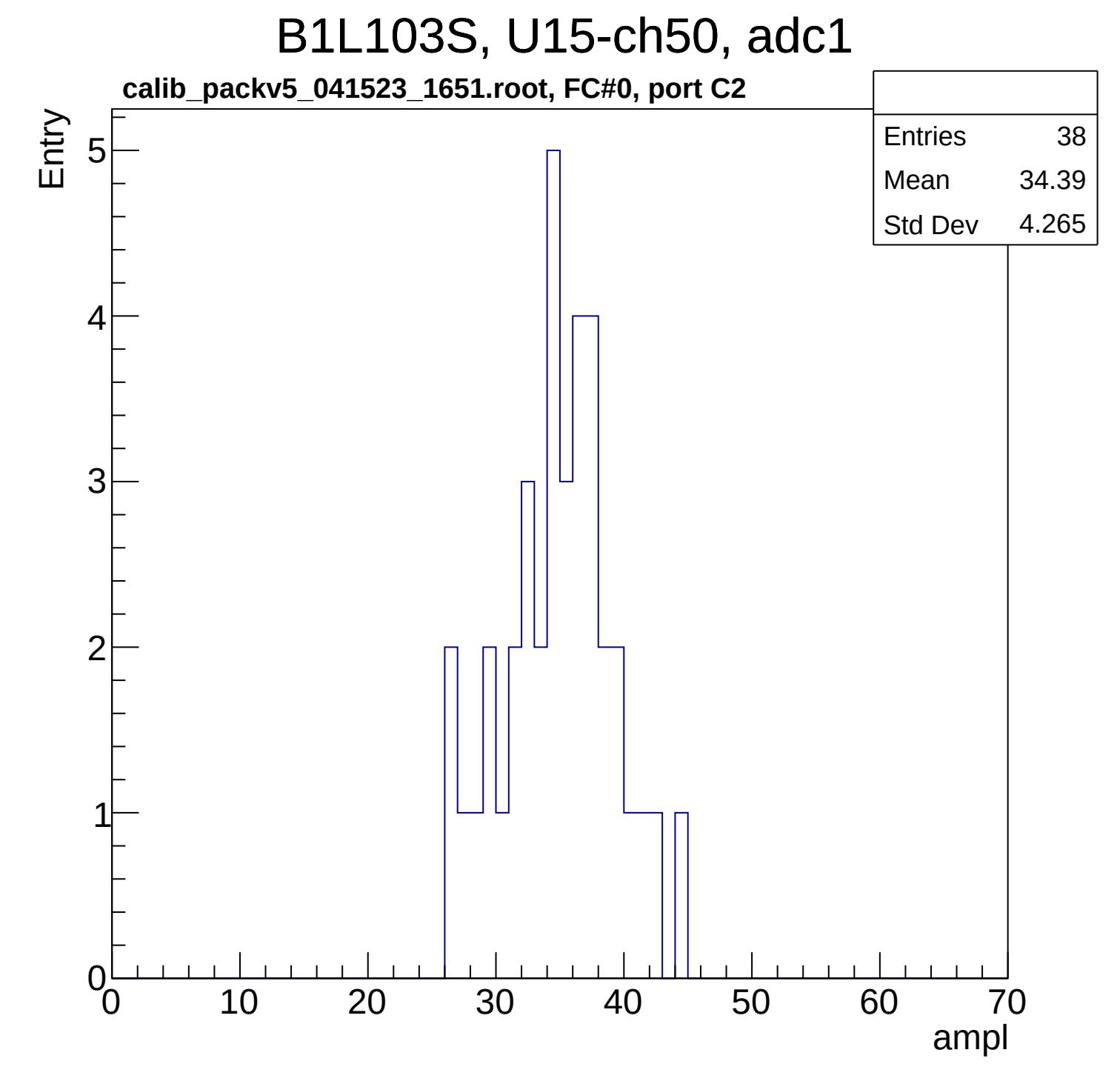
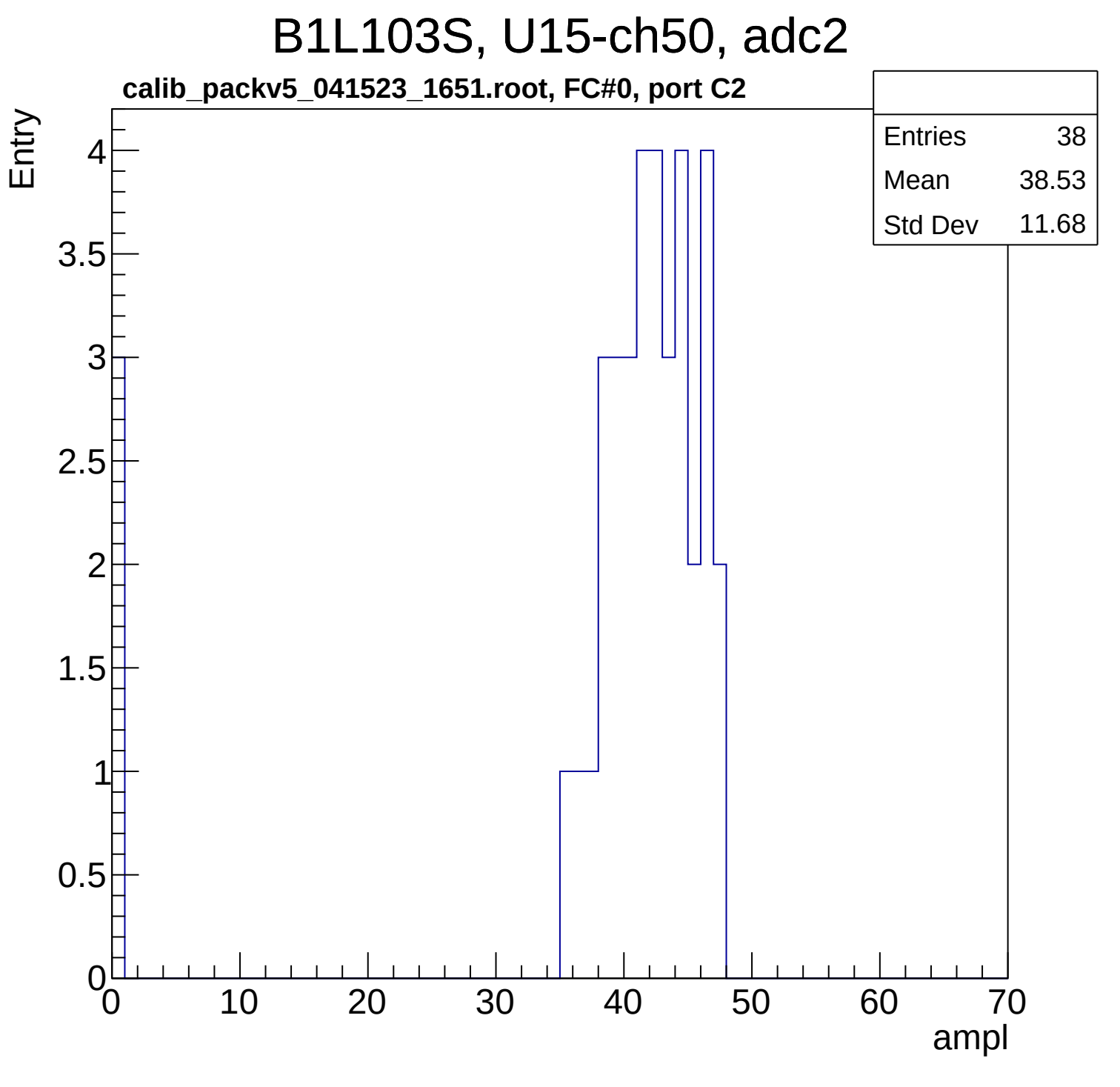
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U15-ch50, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 34.39
Std Dev 4.265
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch50, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 38.53
Std Dev 11.68
Entry
ampl
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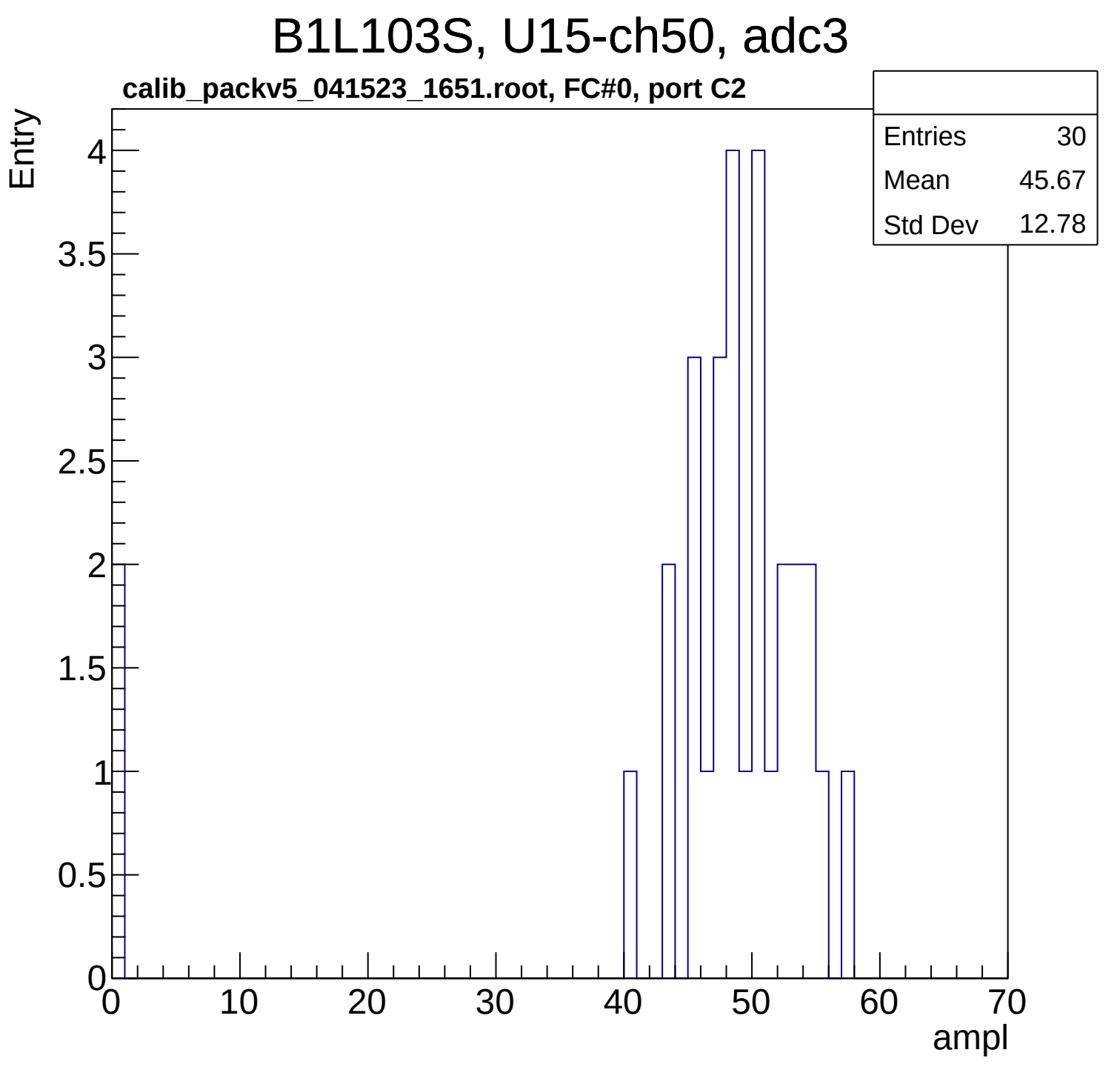
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch50, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 45.67
Std Dev 12.78
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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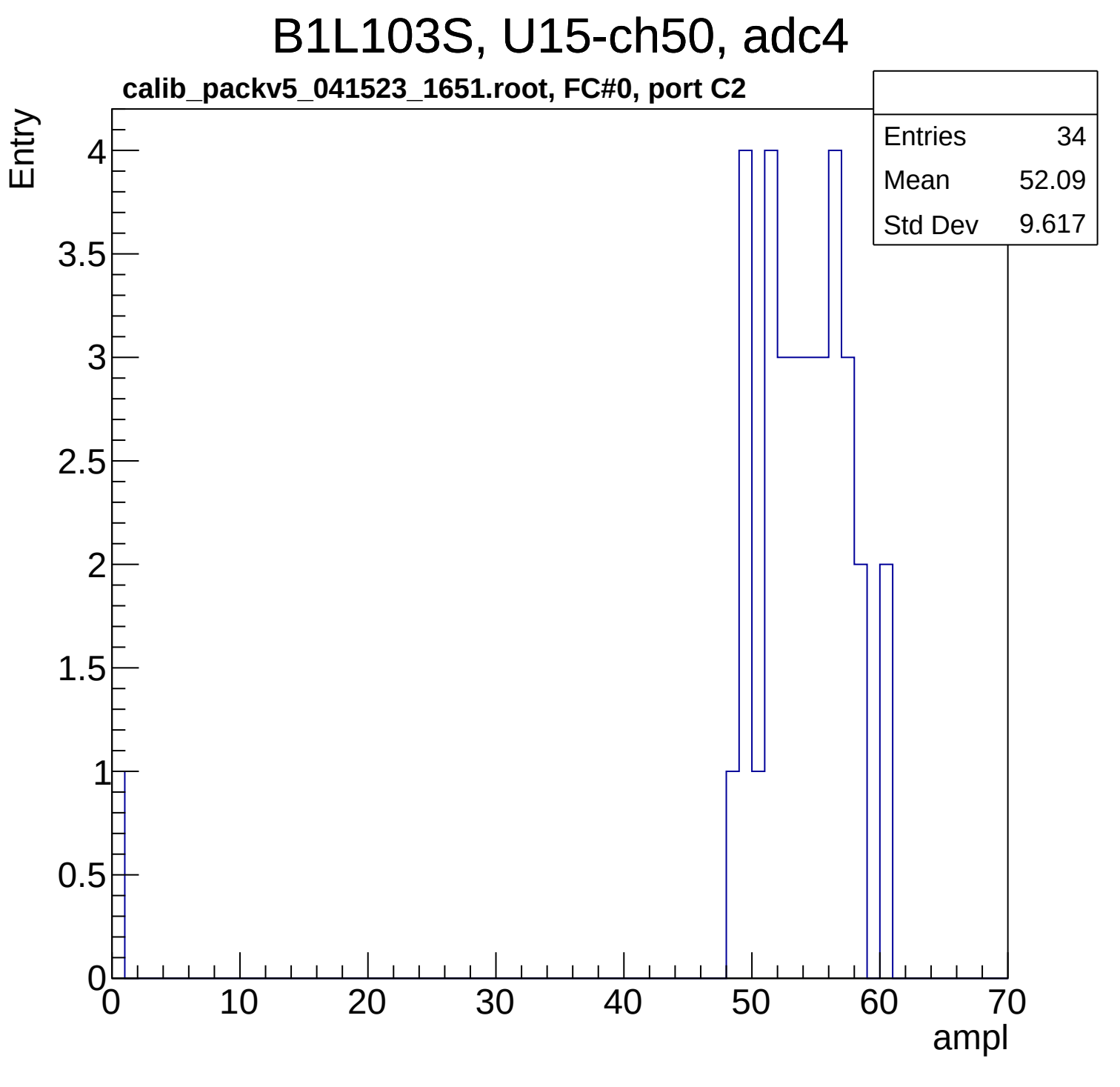
B1L103S, U15-ch50, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 52.09
Std Dev 9.617
Entry
ampl
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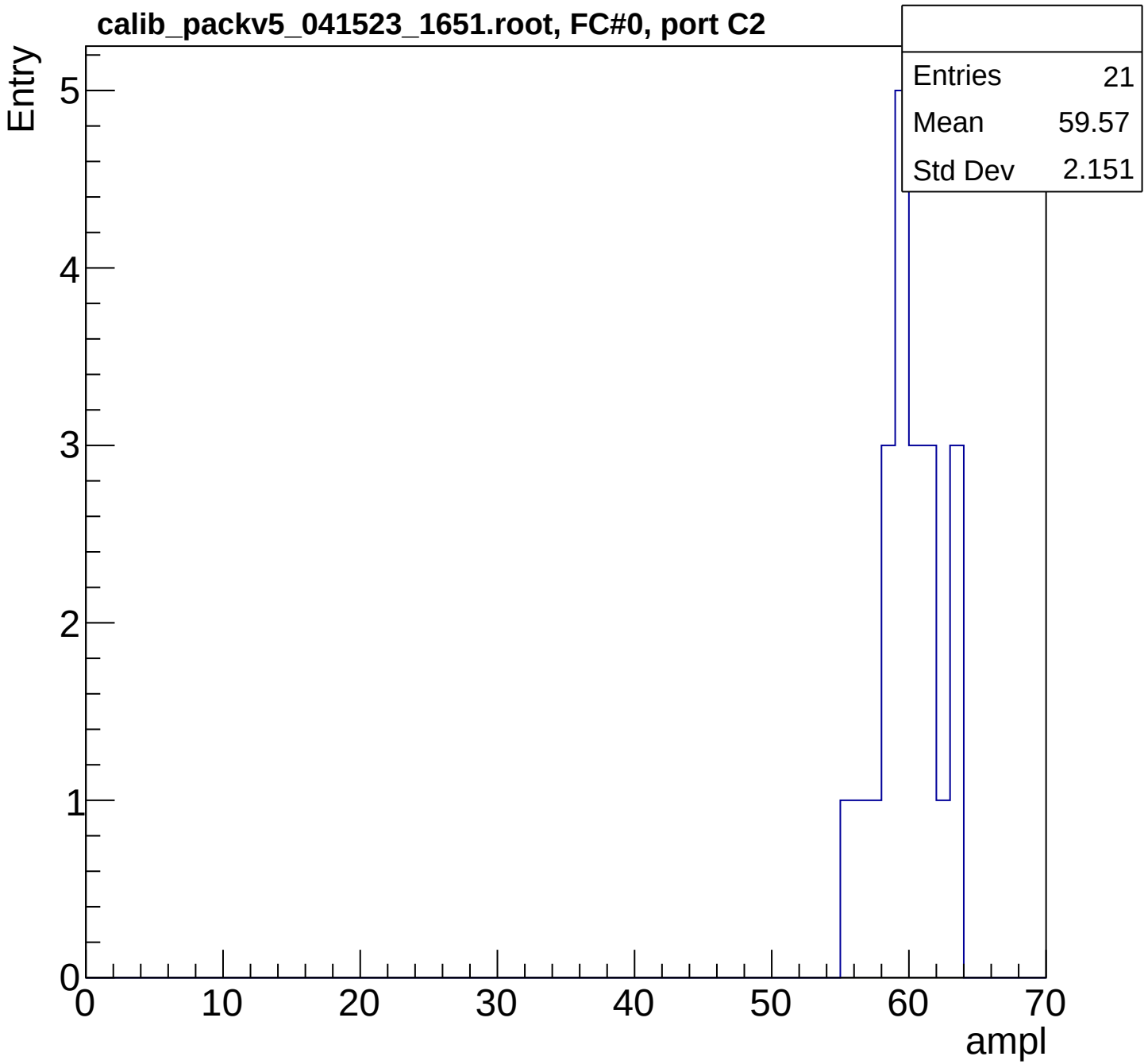
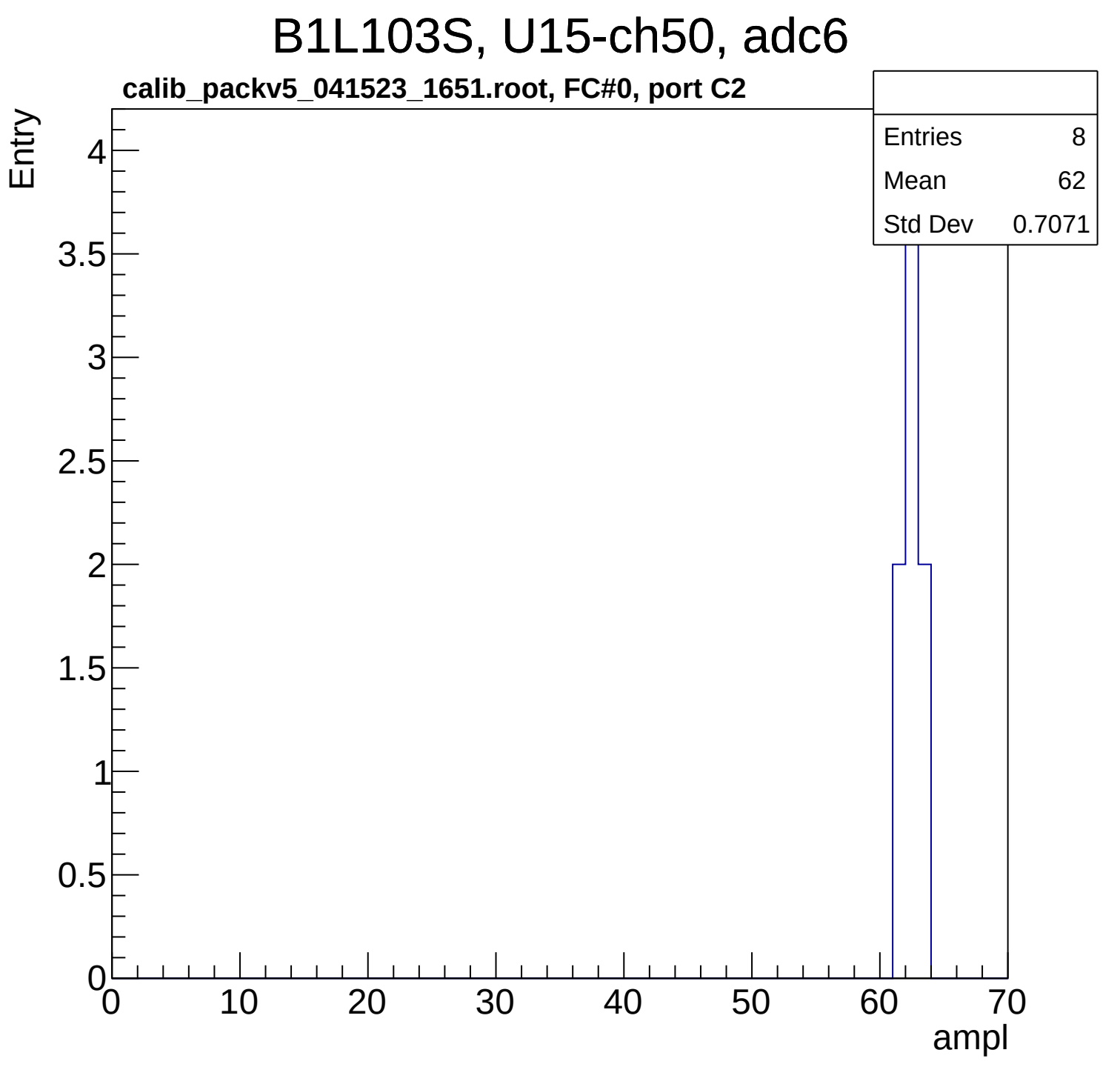
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch50, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 59.57
Std Dev 2.151
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch50, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62
Std Dev 0.7071
Entry
ampl
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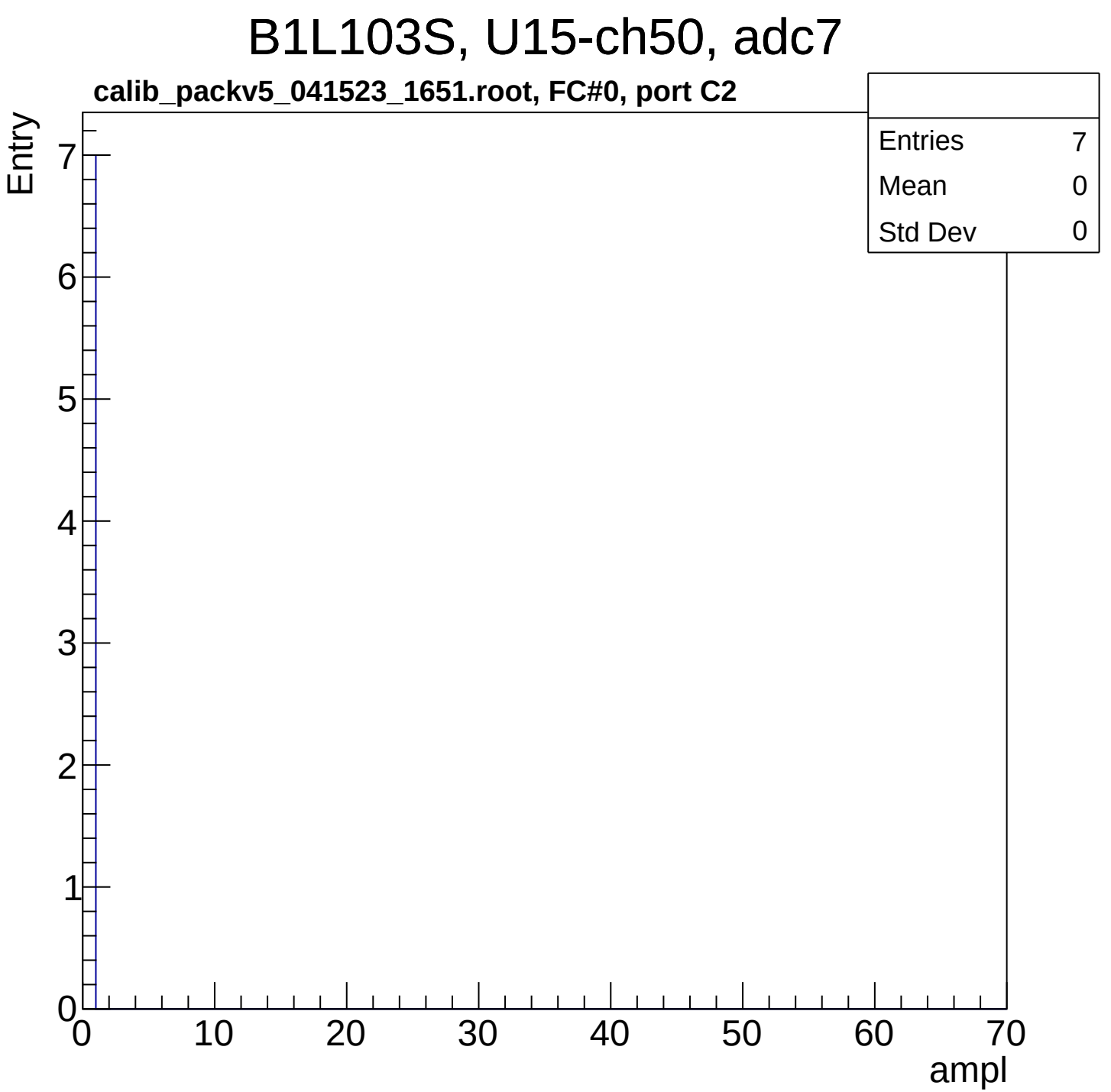
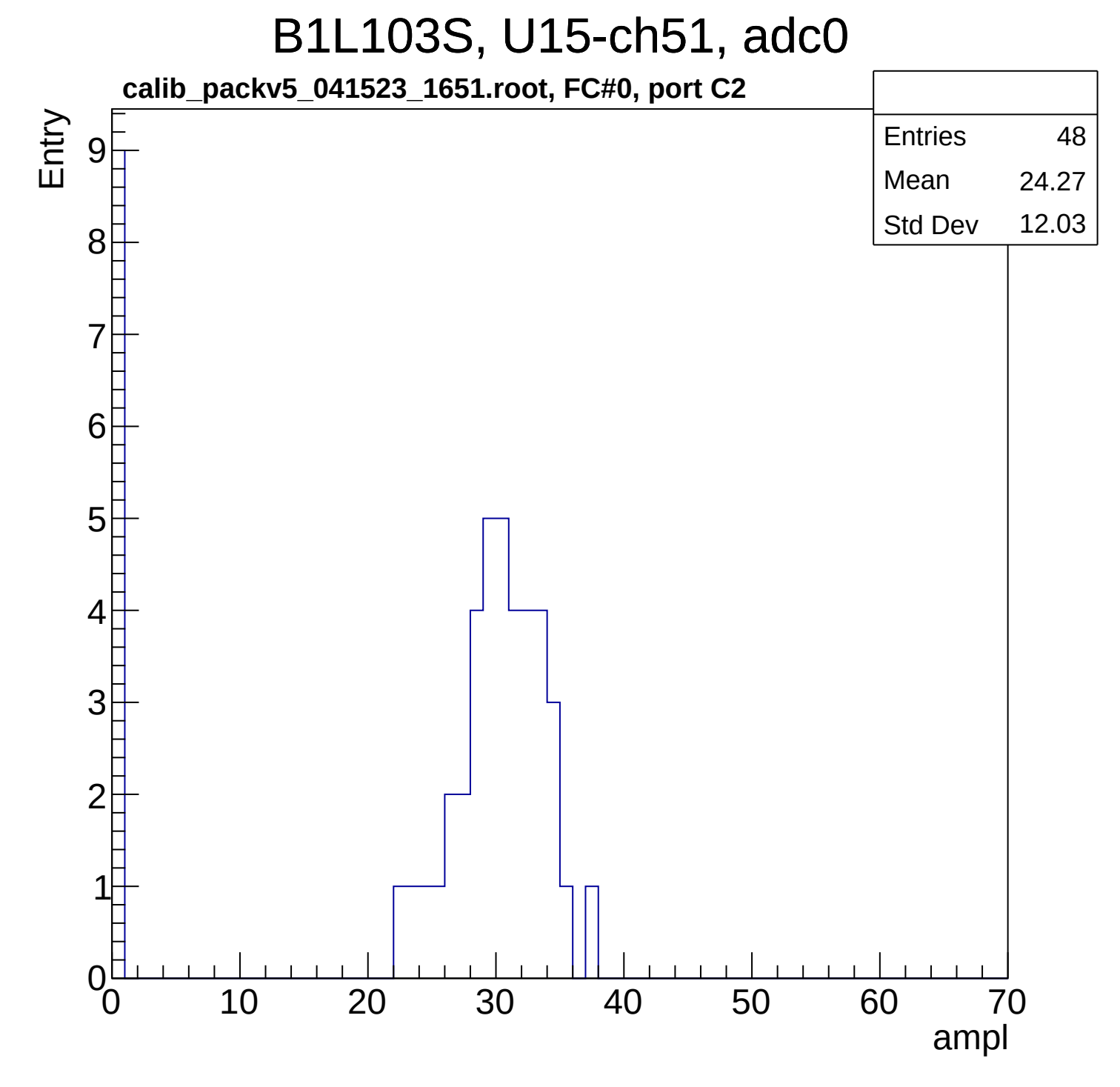
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch50, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 0
Std Dev 0
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch51, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 24.27
Std Dev 12.03
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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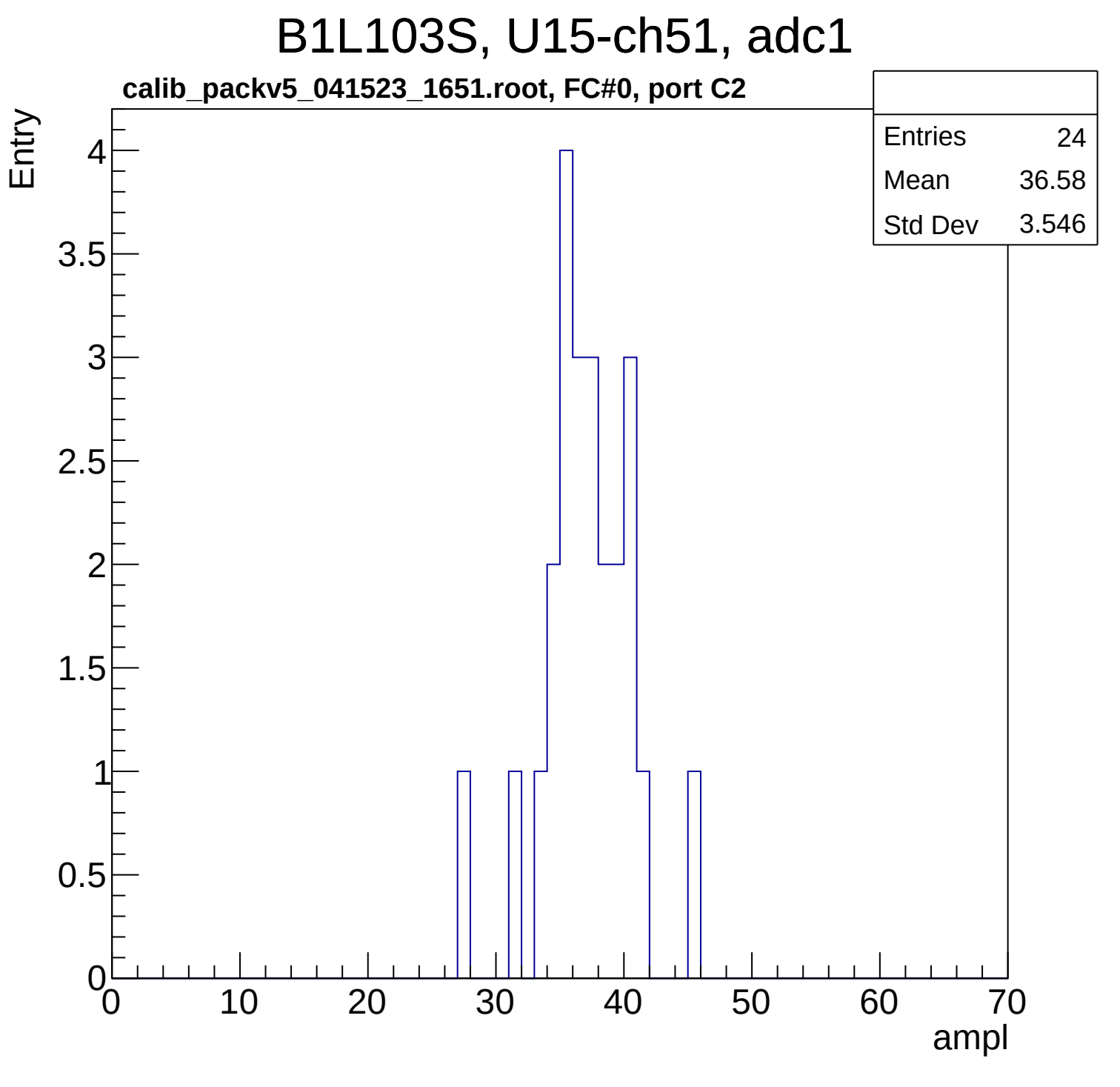
B1L103S, U15-ch51, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 36.58
Std Dev 3.546
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
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20
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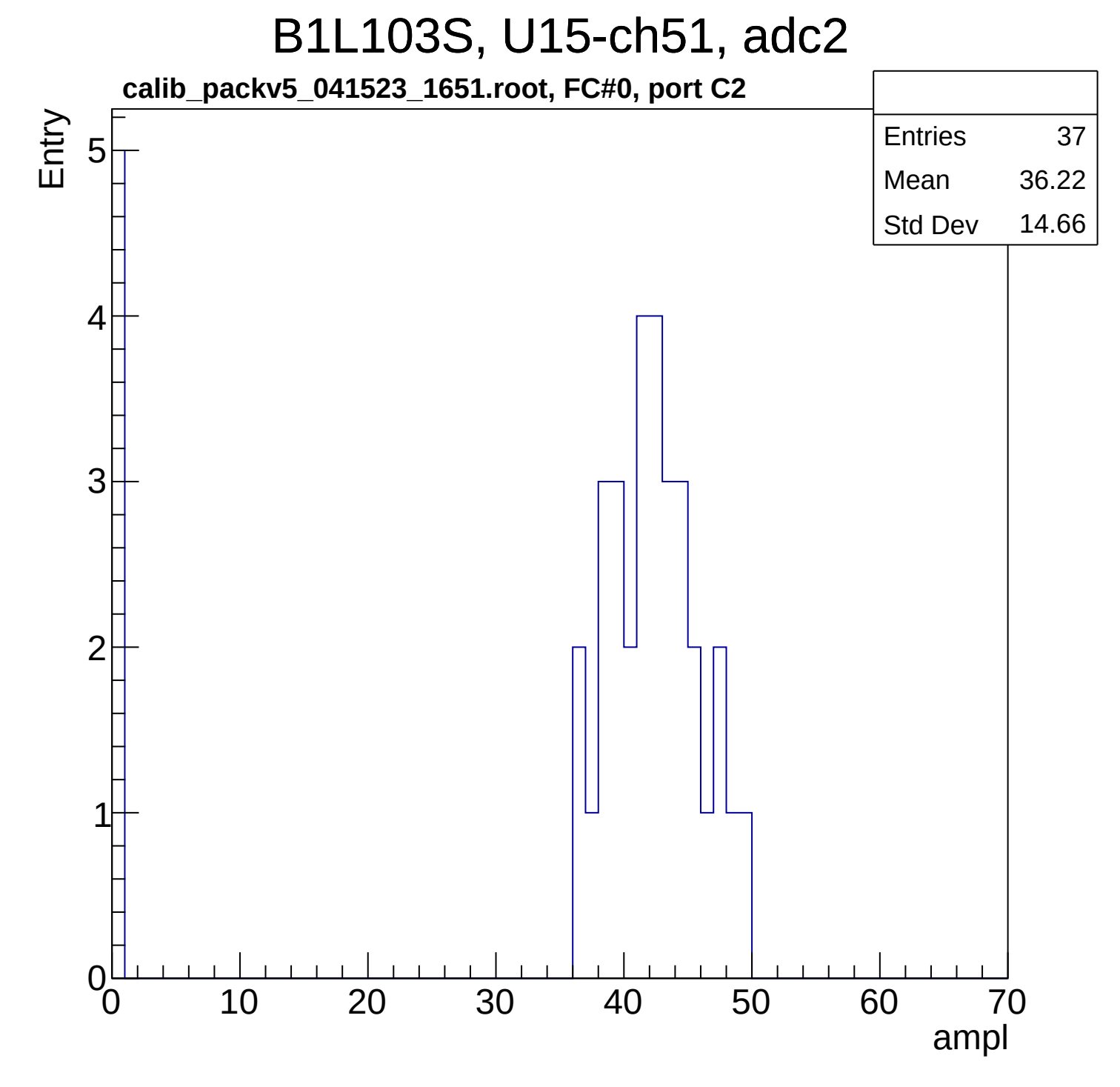
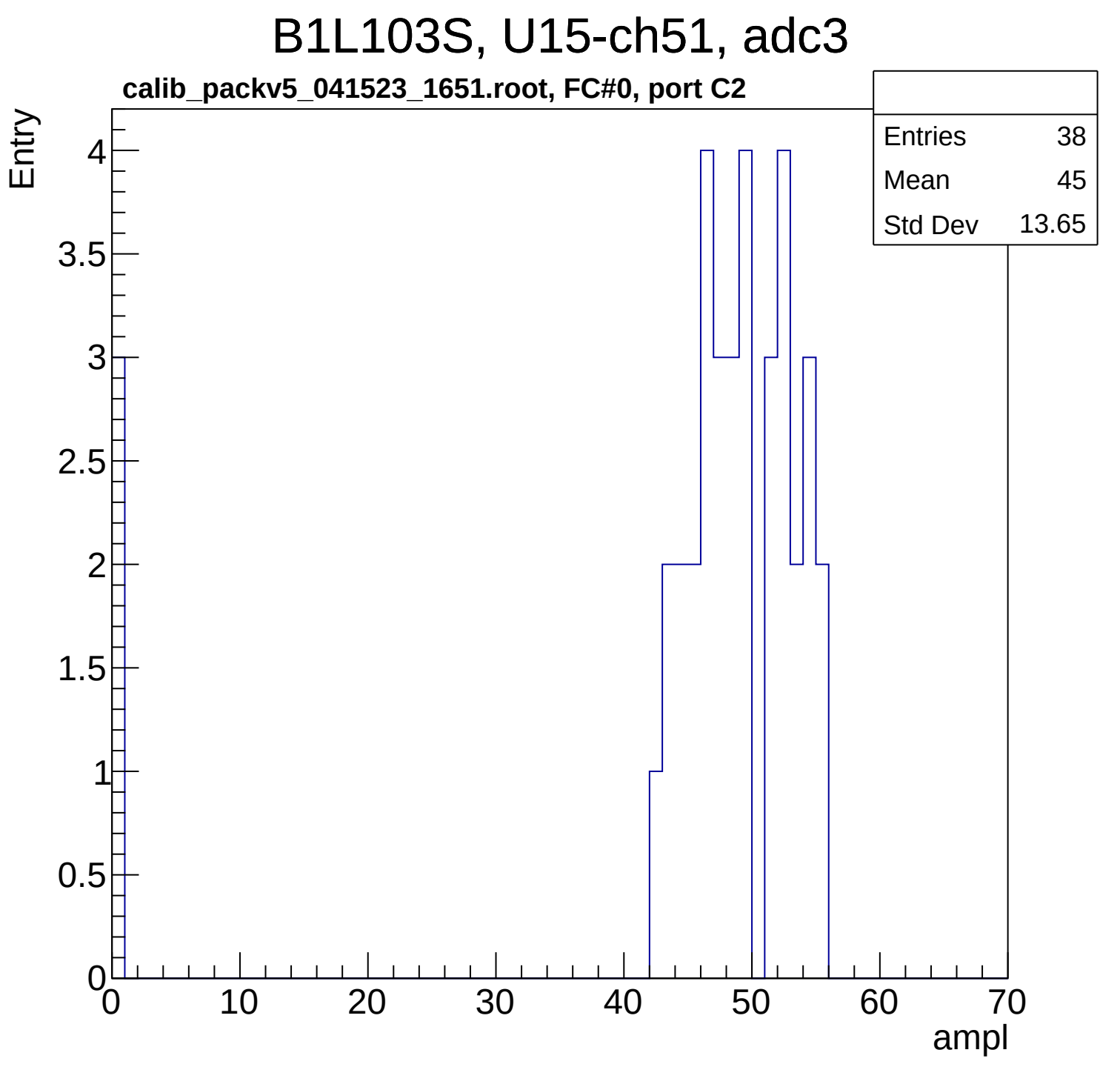
50
60
70


B1L103S, U15-ch51, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 36.22
Std Dev 14.66
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch51, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 45
Std Dev 13.65
Entry
ampl
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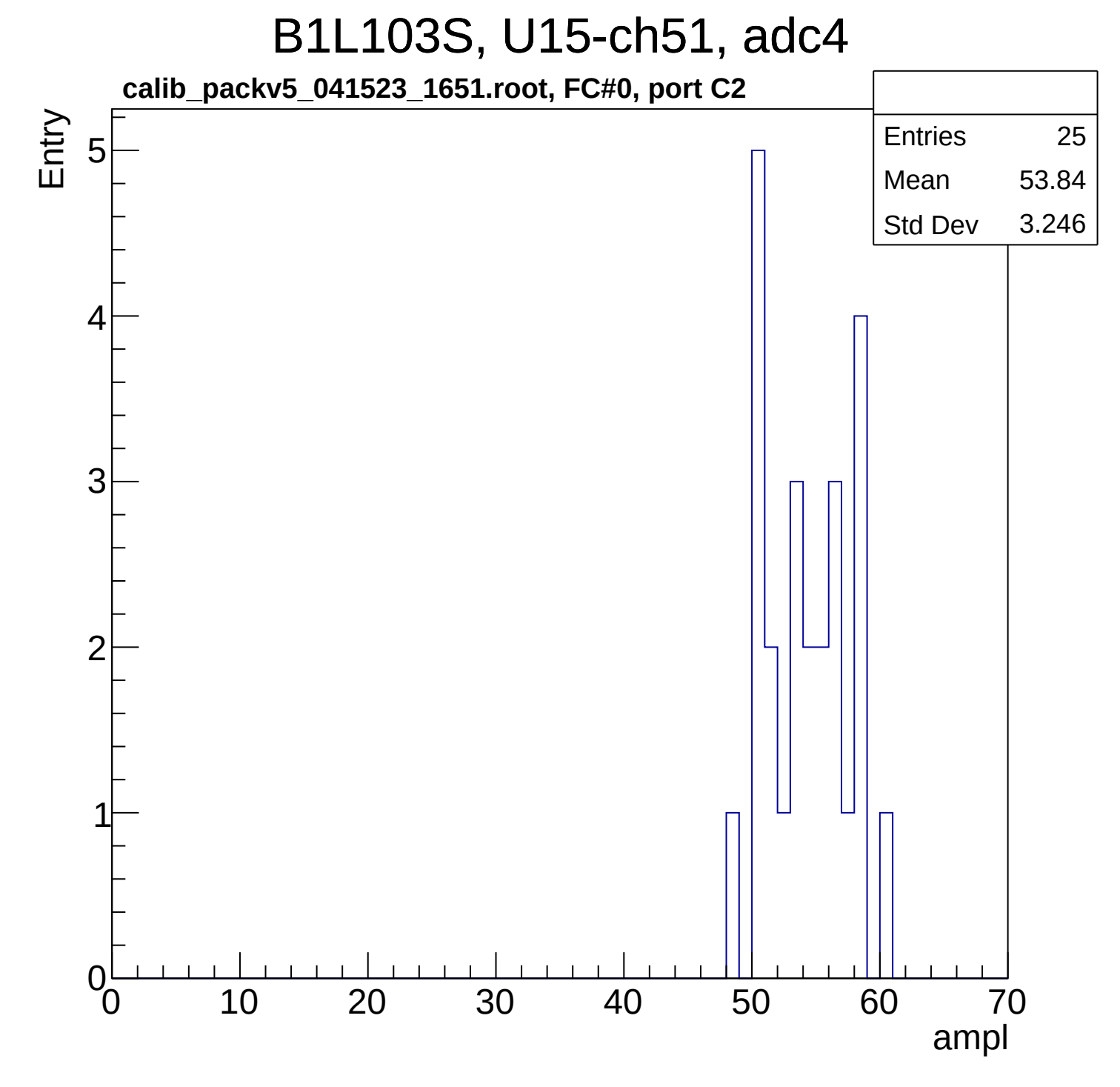
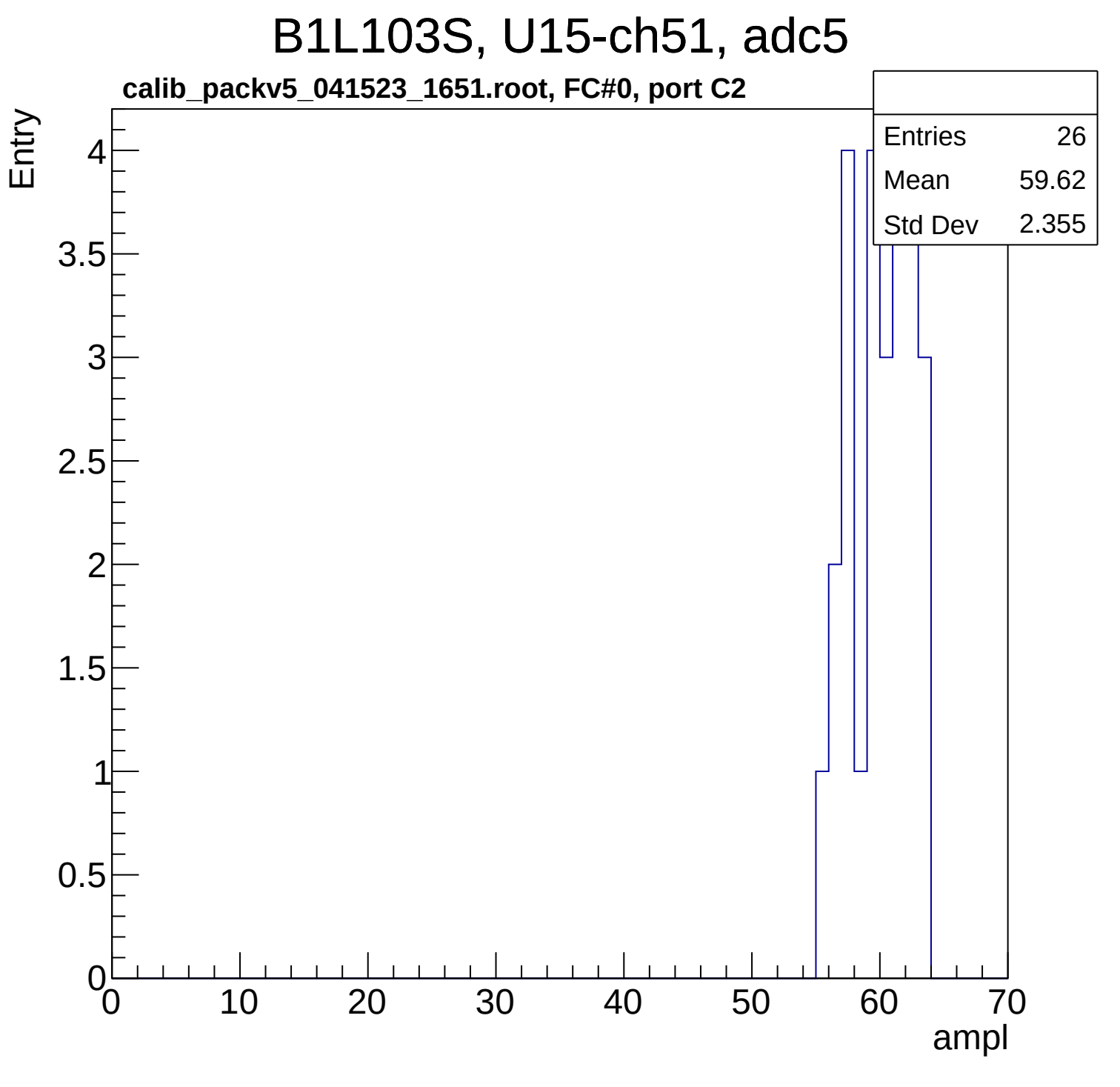
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch51, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 53.84
Std Dev 3.246
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch51, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 59.62
Std Dev 2.355
Entry
ampl
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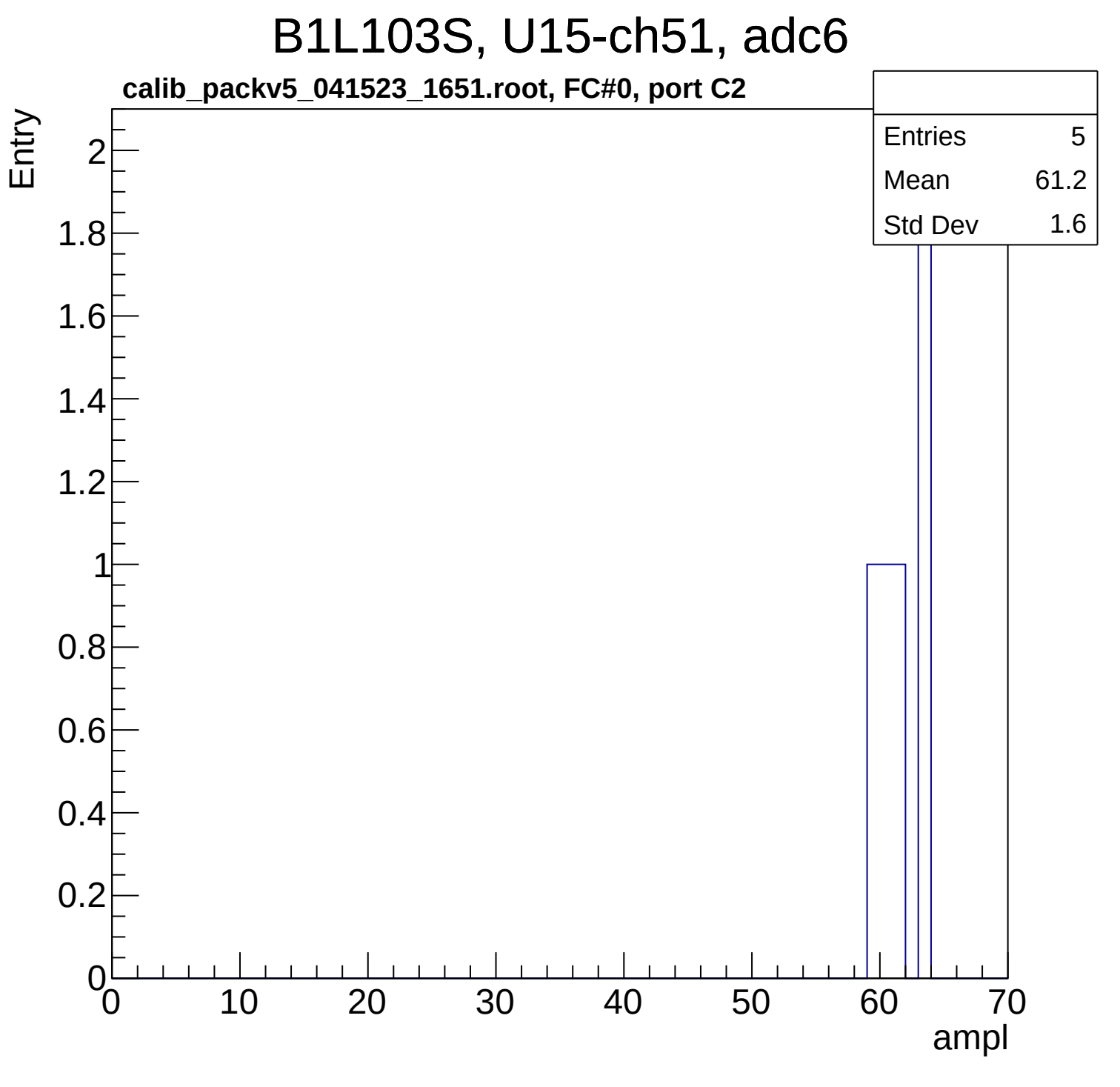
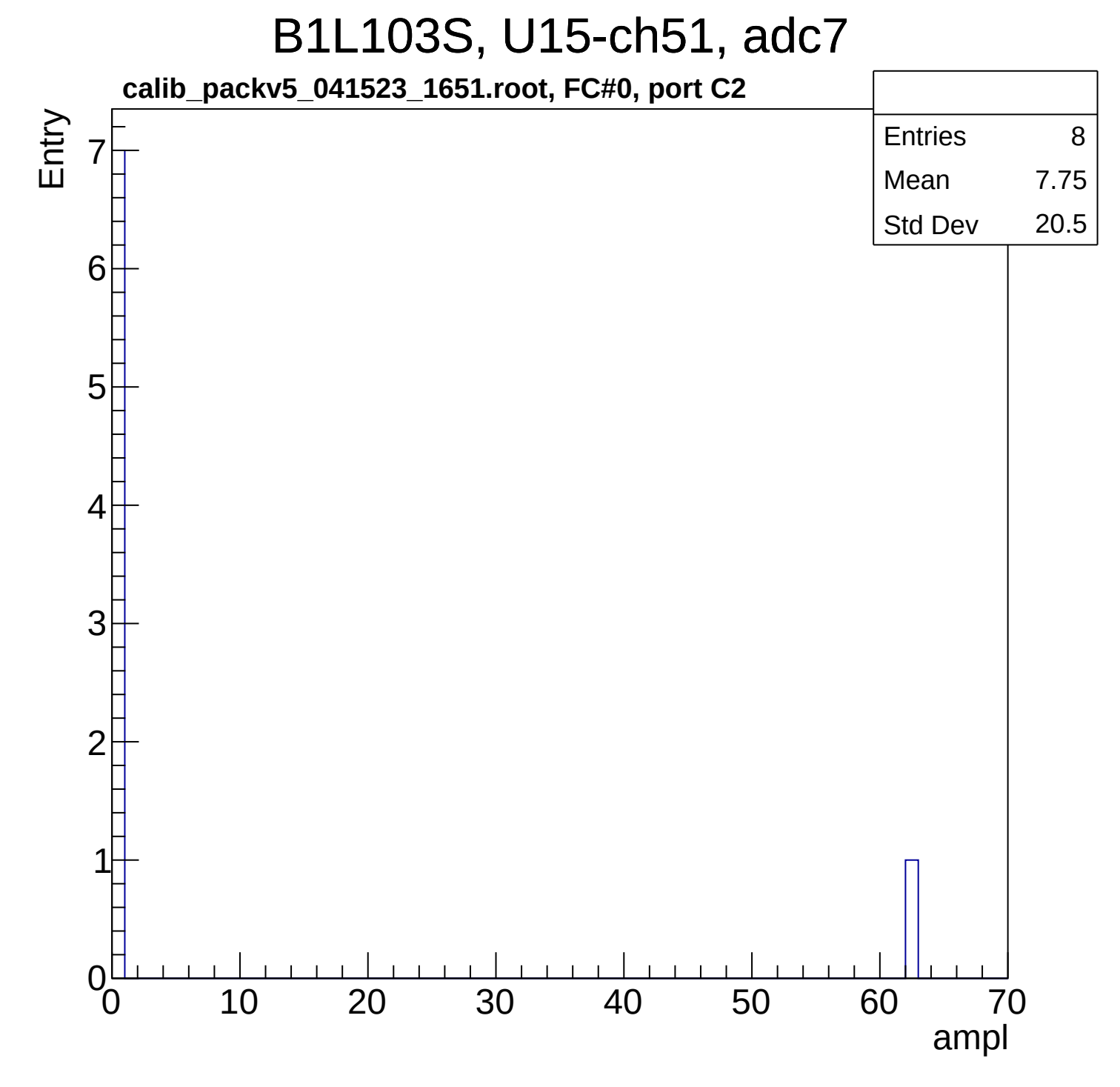
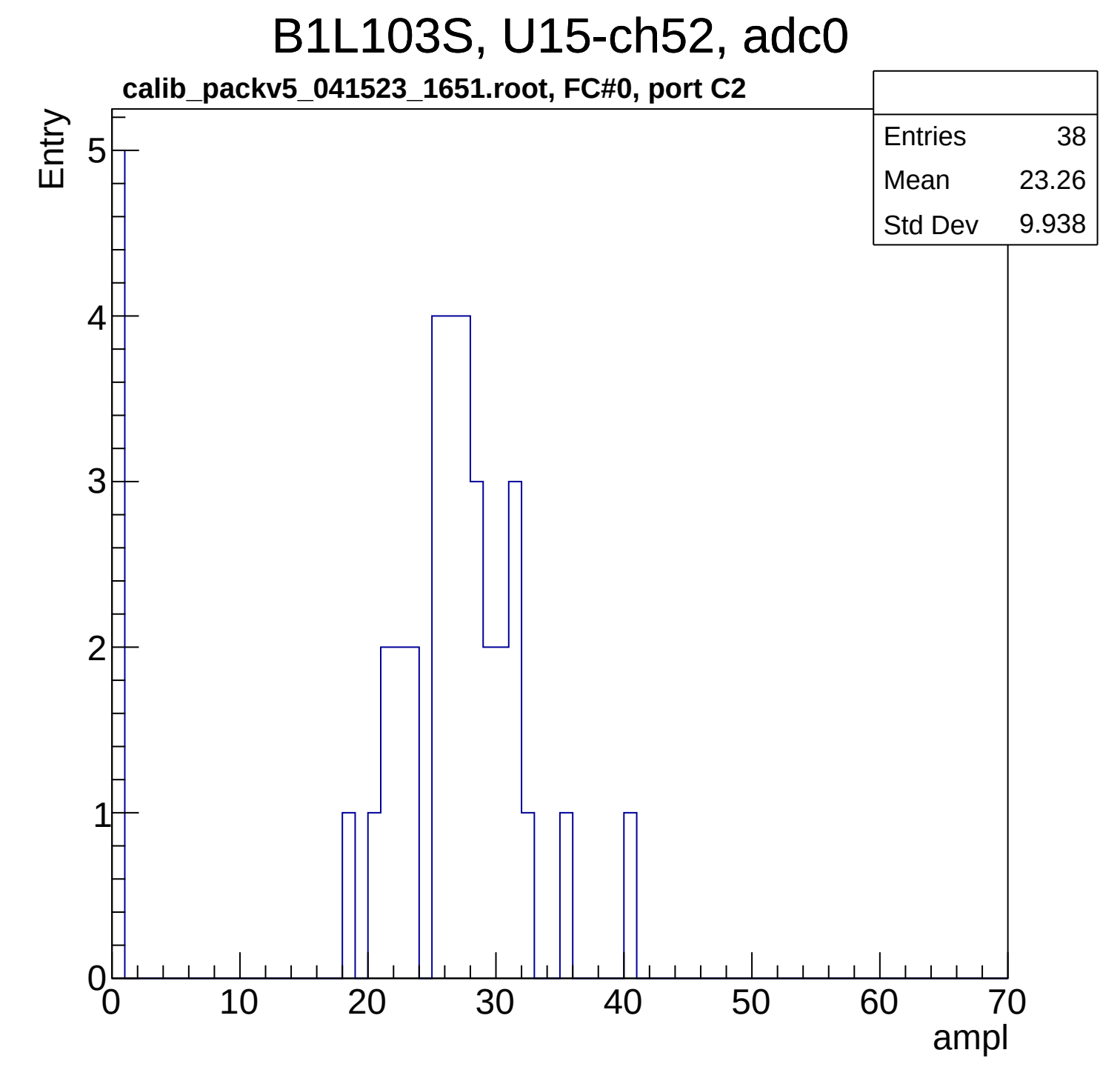
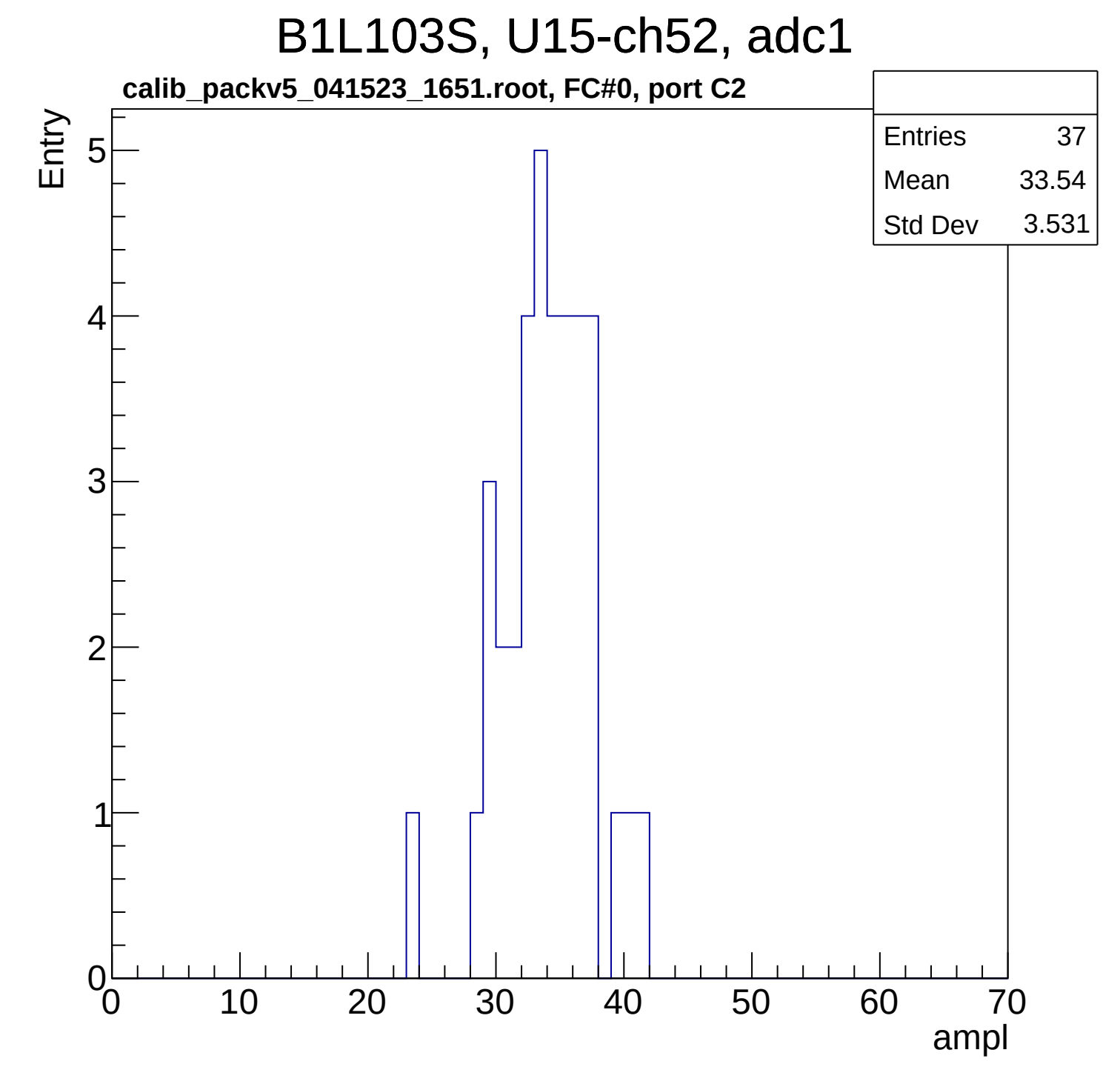
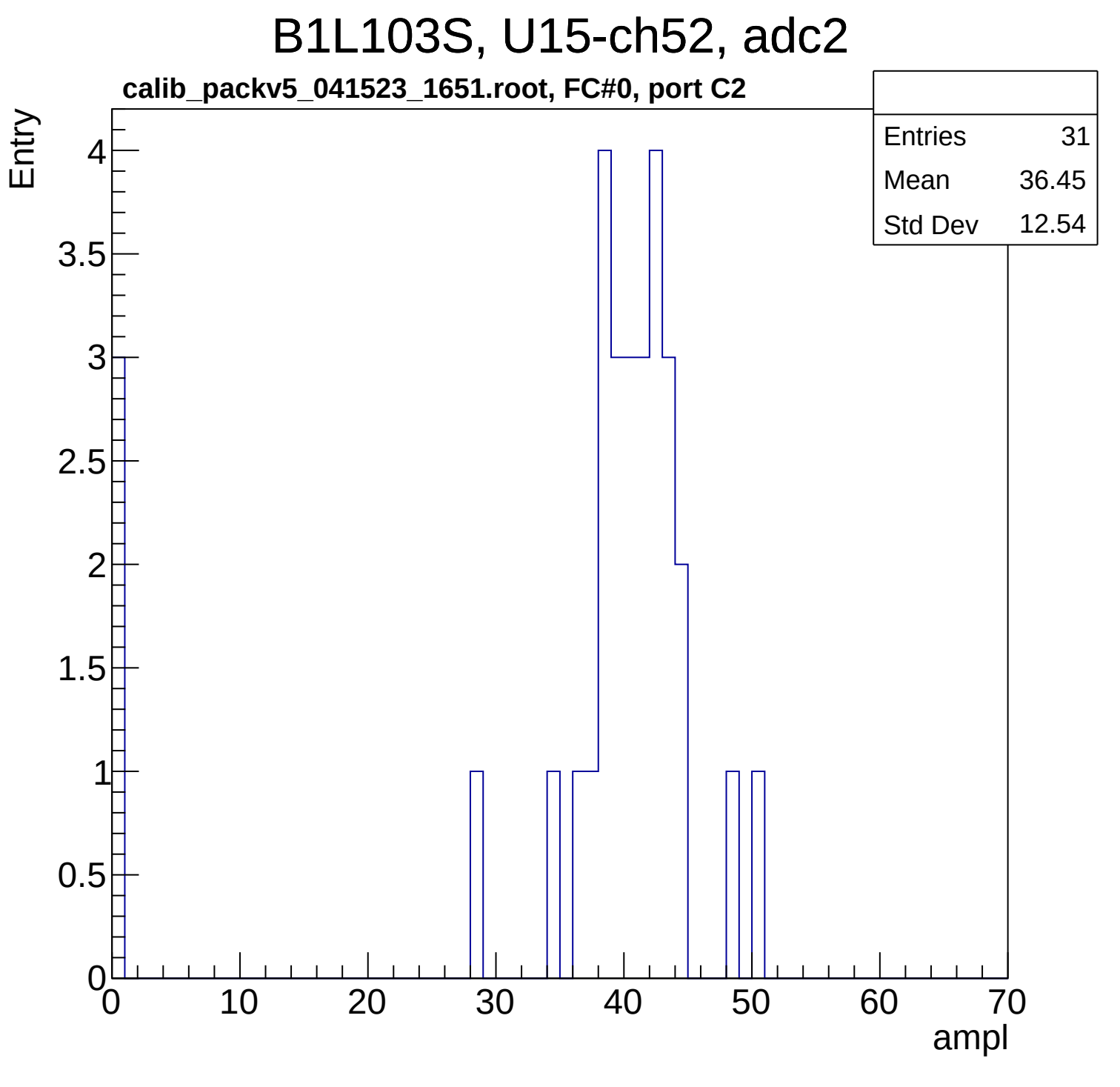
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

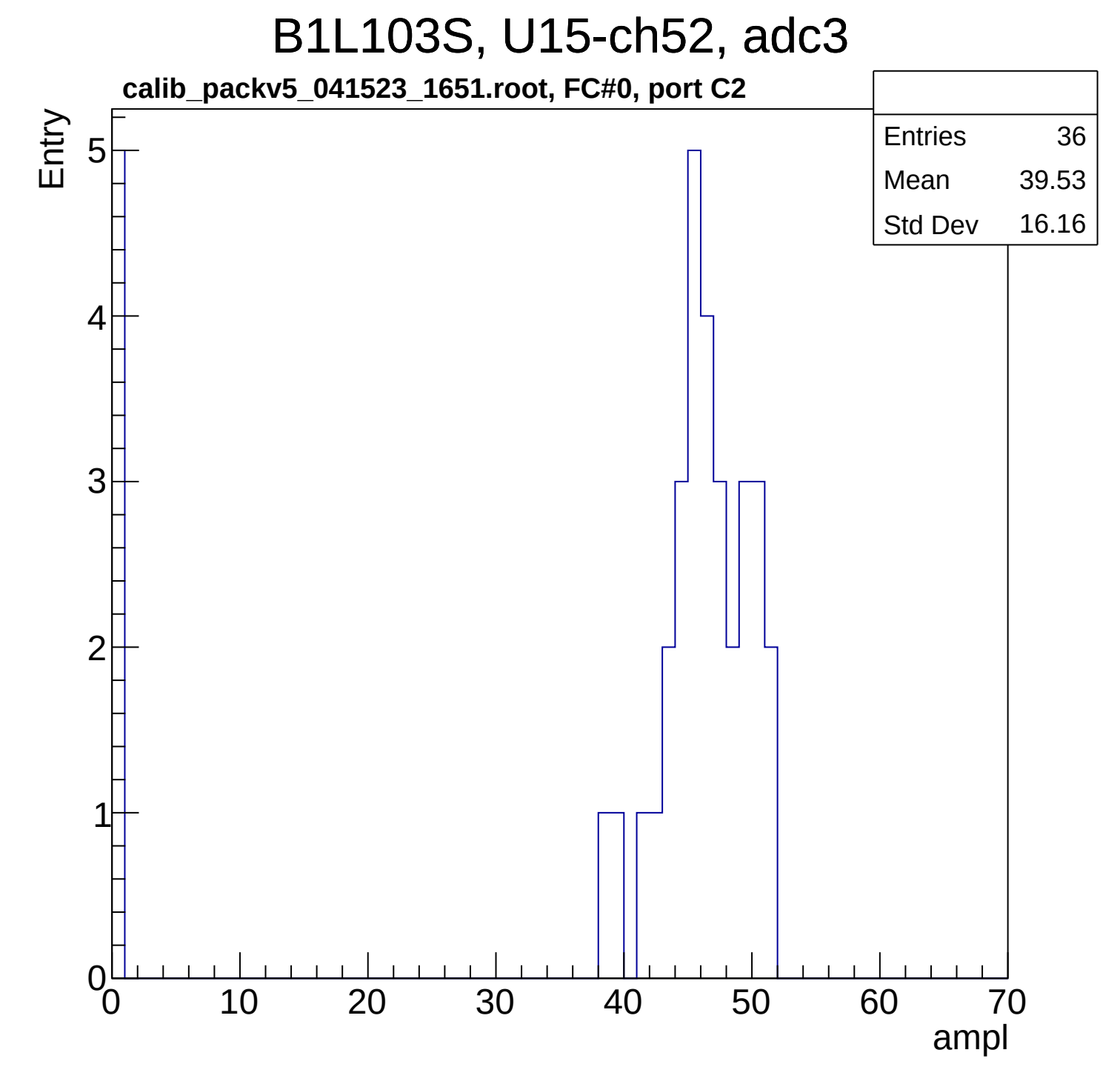

B1L103S, U15-ch51, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.2
Std Dev 1.6
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

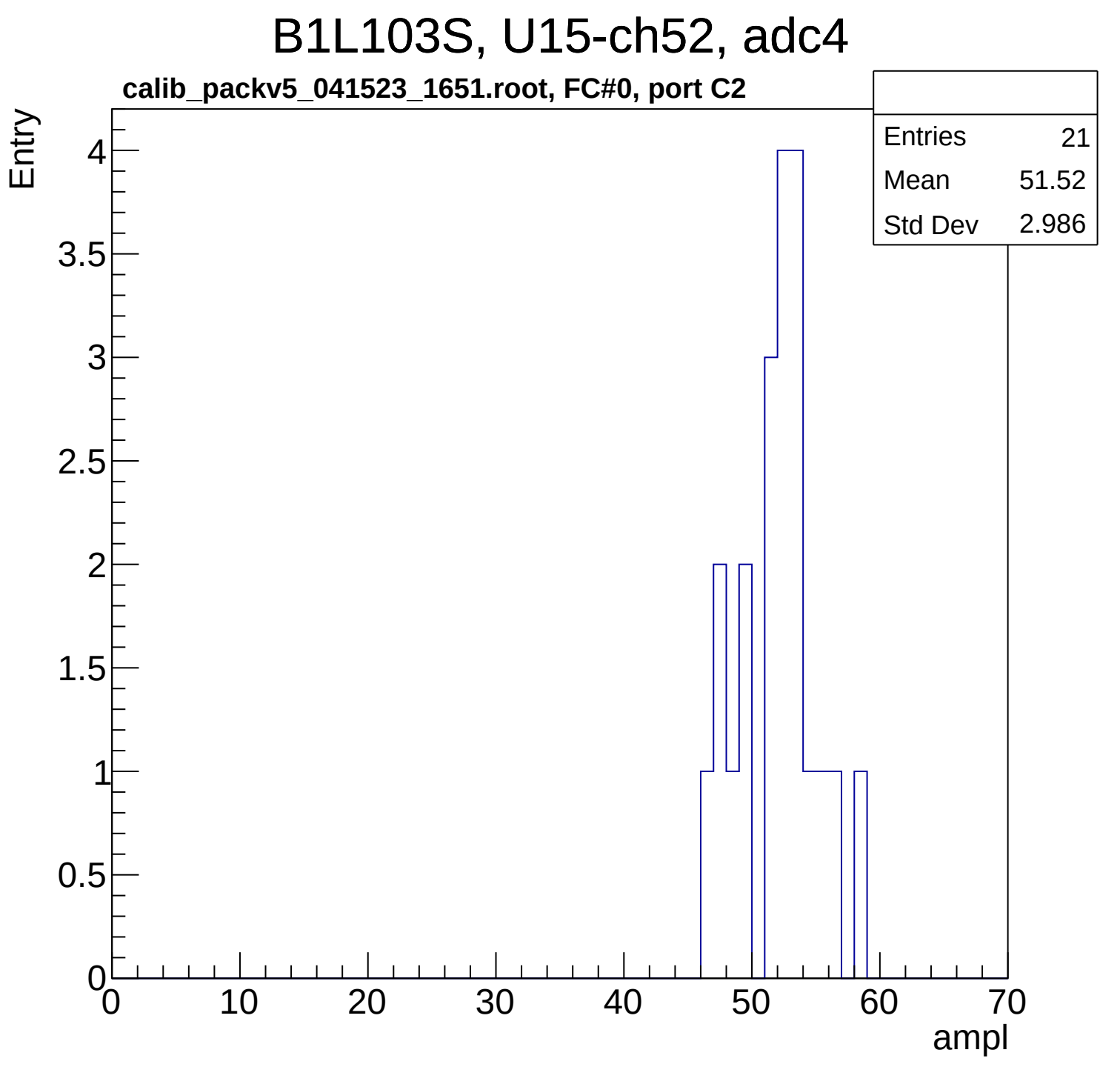

B1L103S, U15-ch51, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 7.75
Std Dev 20.5
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

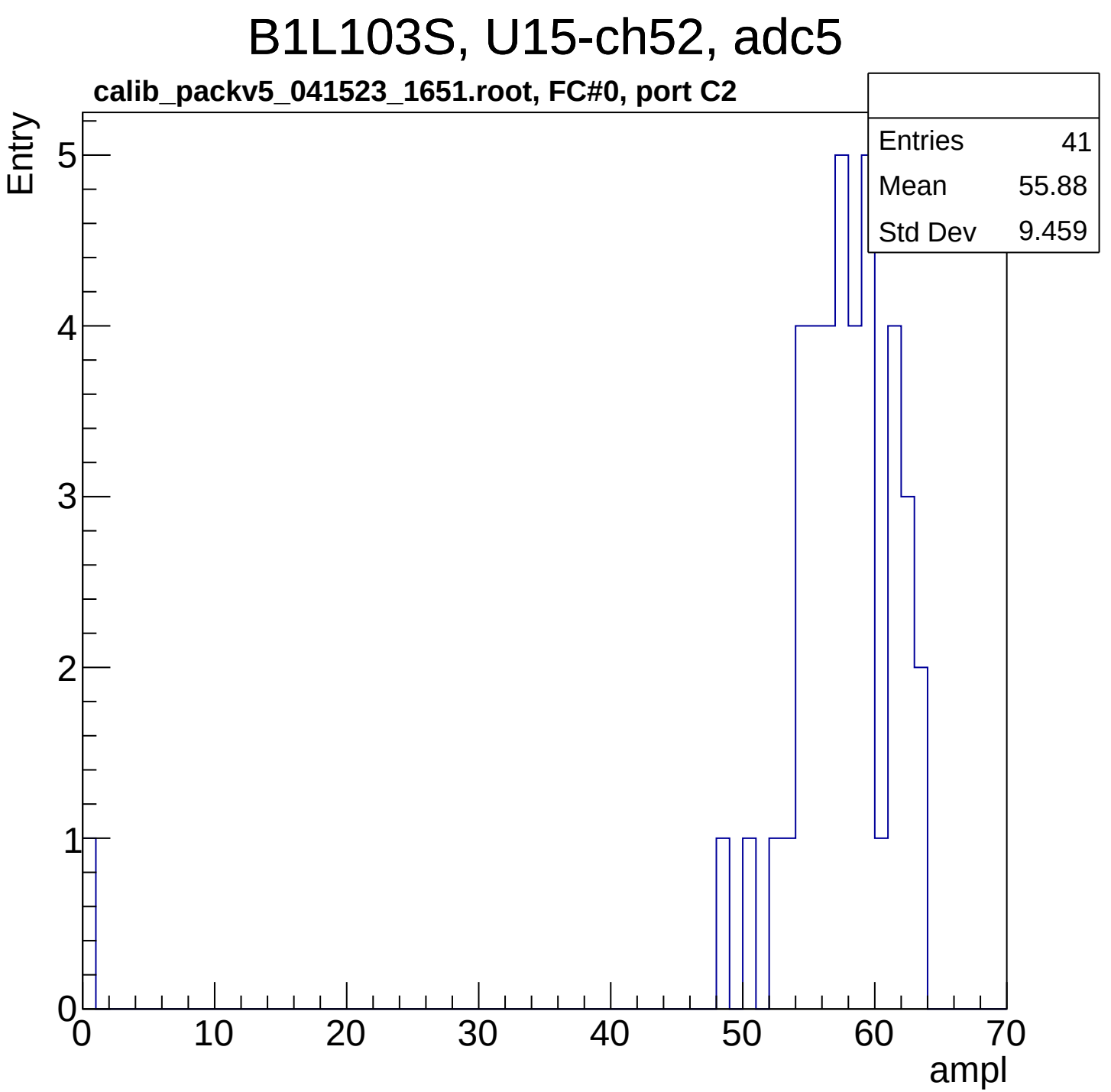

B1L103S, U15-ch52, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 23.26
Std Dev 9.938
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

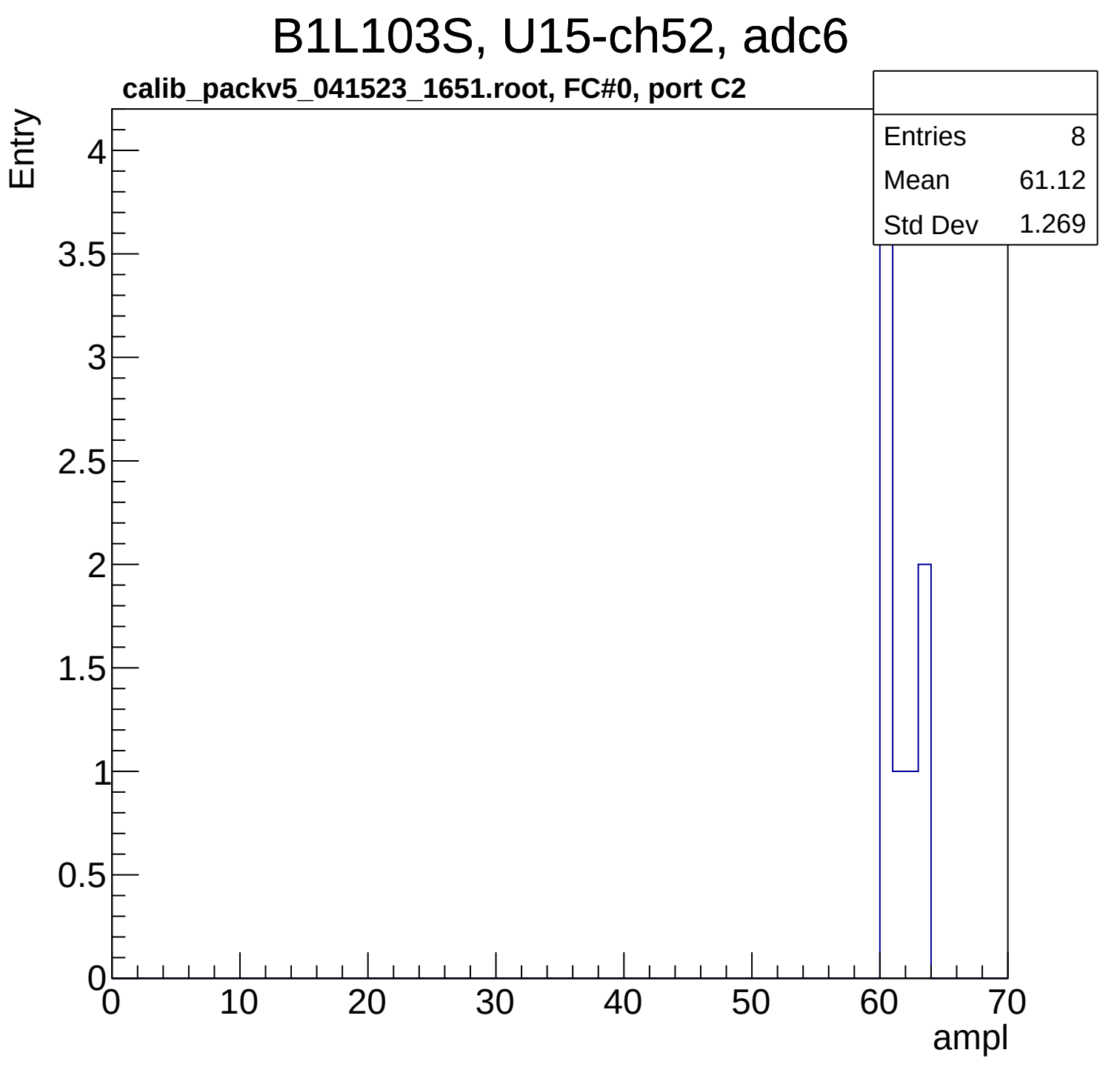

B1L103S, U15-ch52, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 33.54
Std Dev 3.531
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch52, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 36.45
Std Dev 12.54
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch52, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 39.53
Std Dev 16.16
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch52, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 51.52
Std Dev 2.986
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch52, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 55.88
Std Dev 9.459
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch52, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.12
Std Dev 1.269
Entry
ampl
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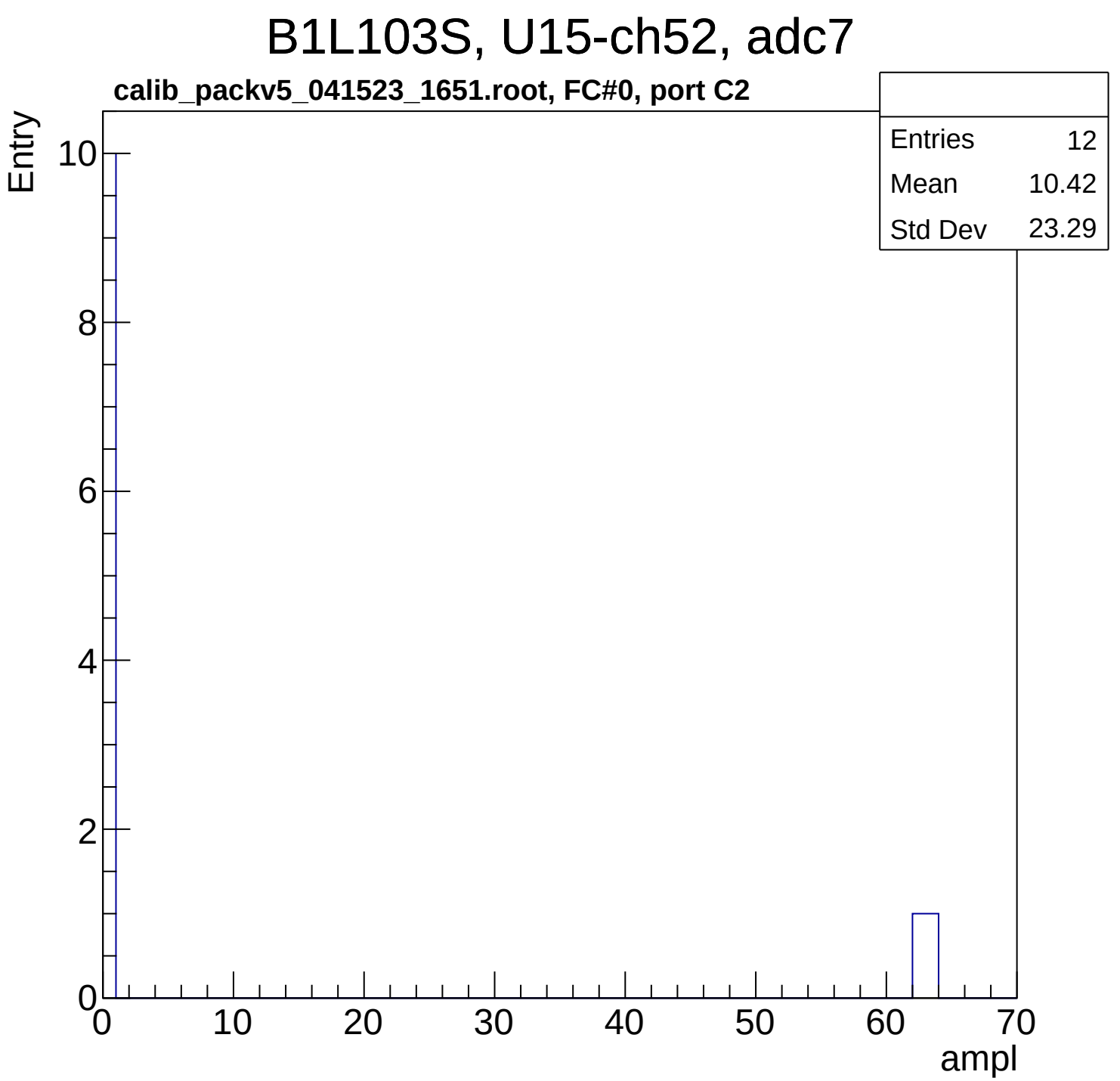
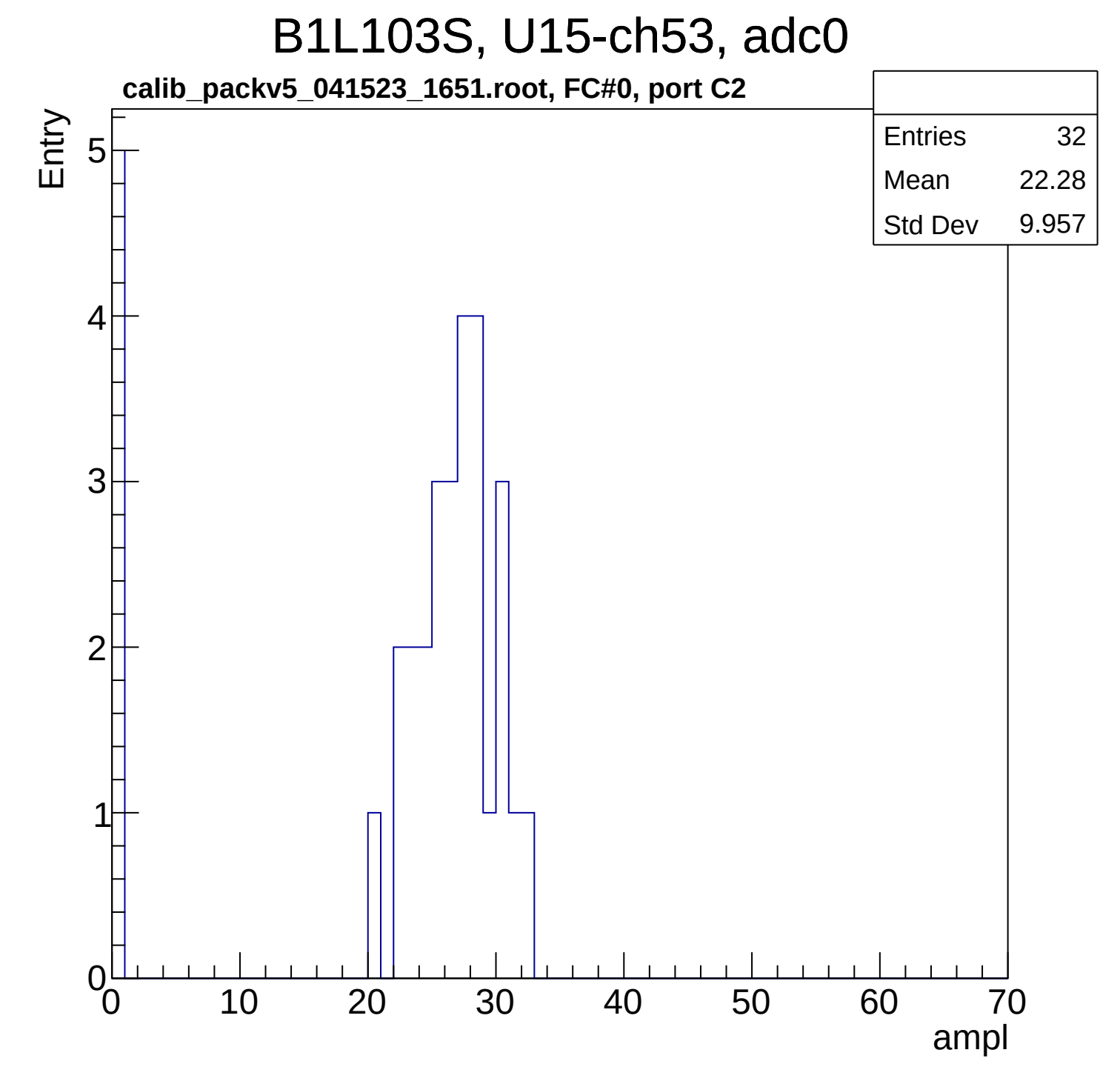
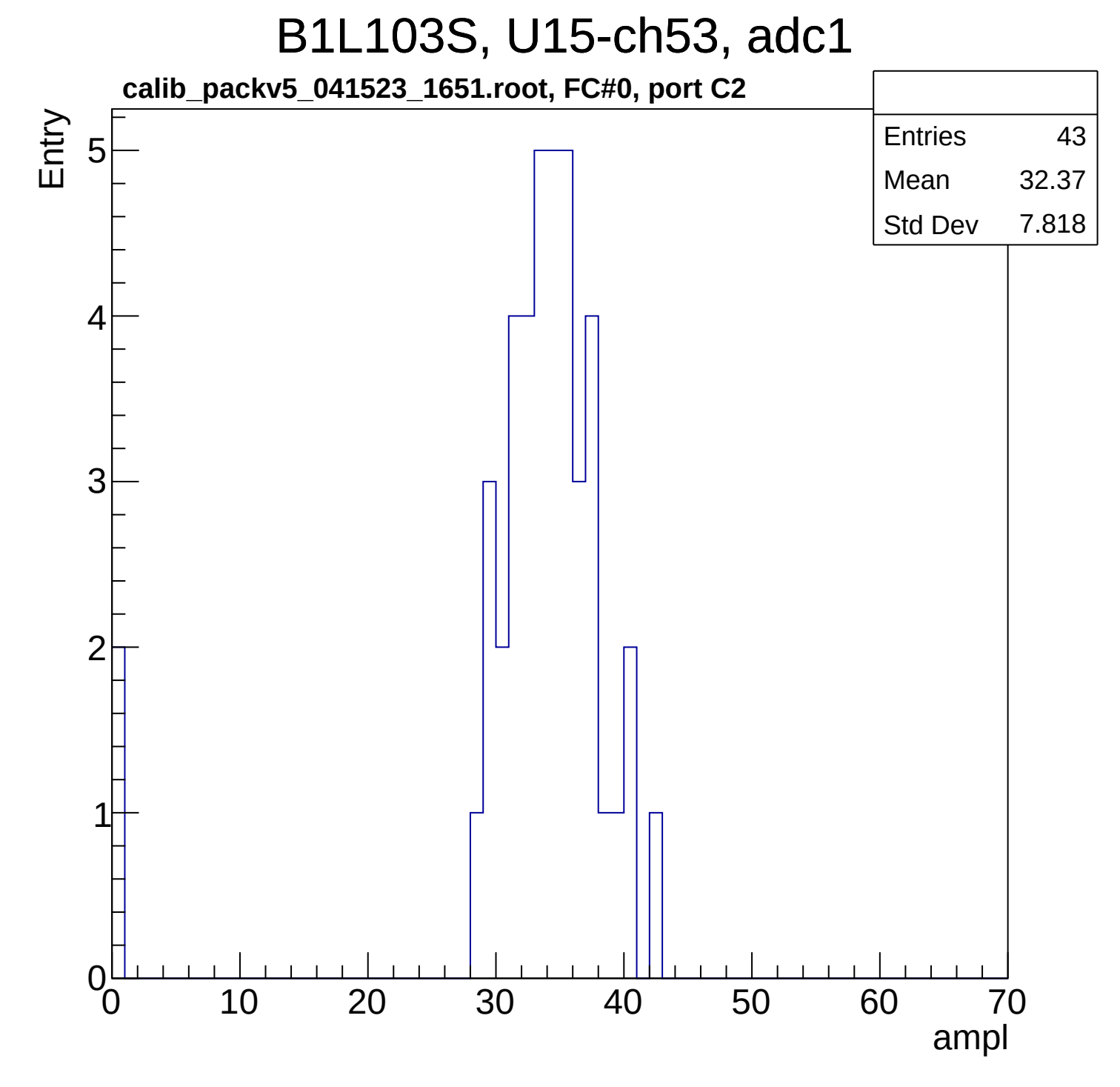
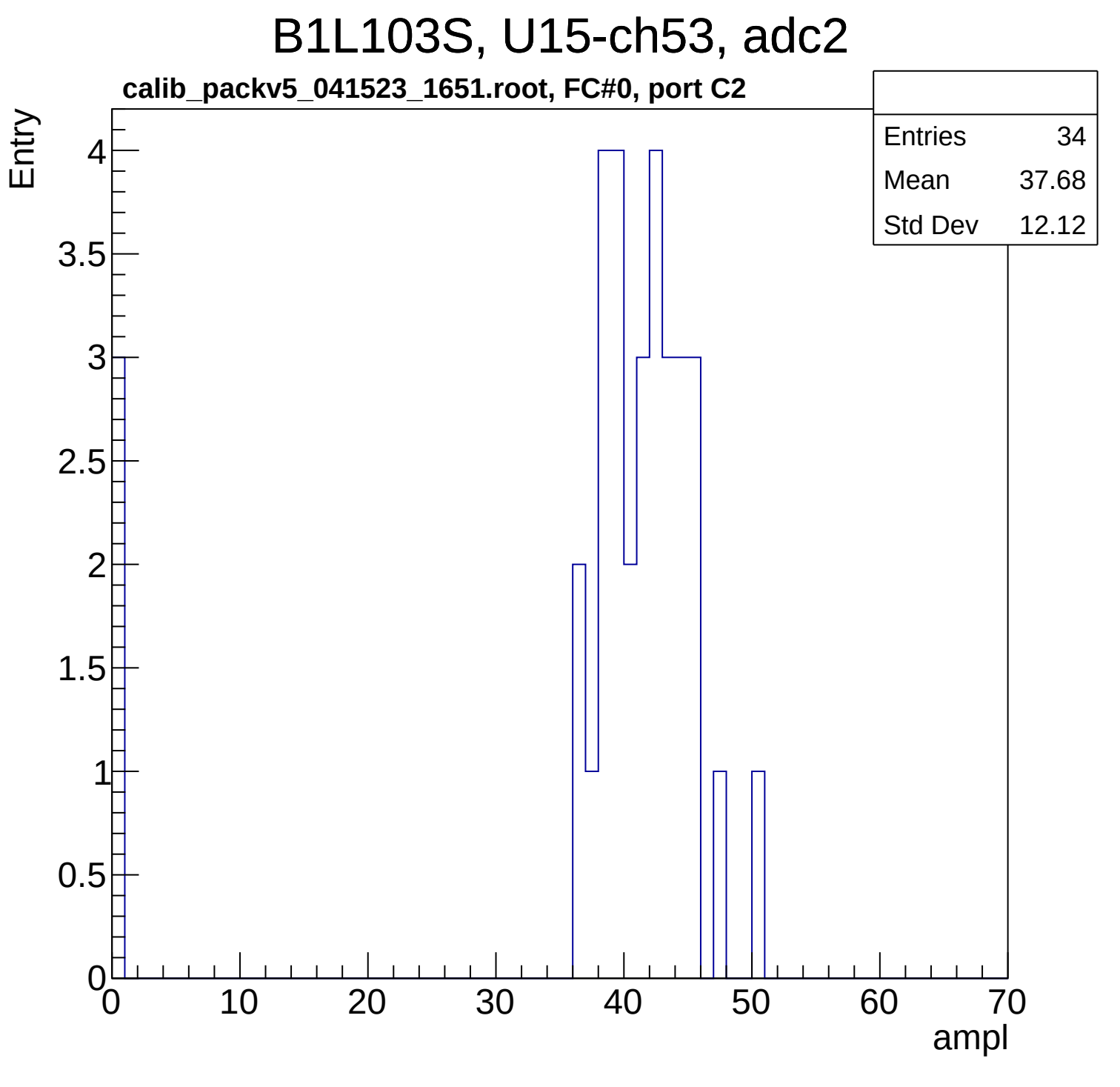
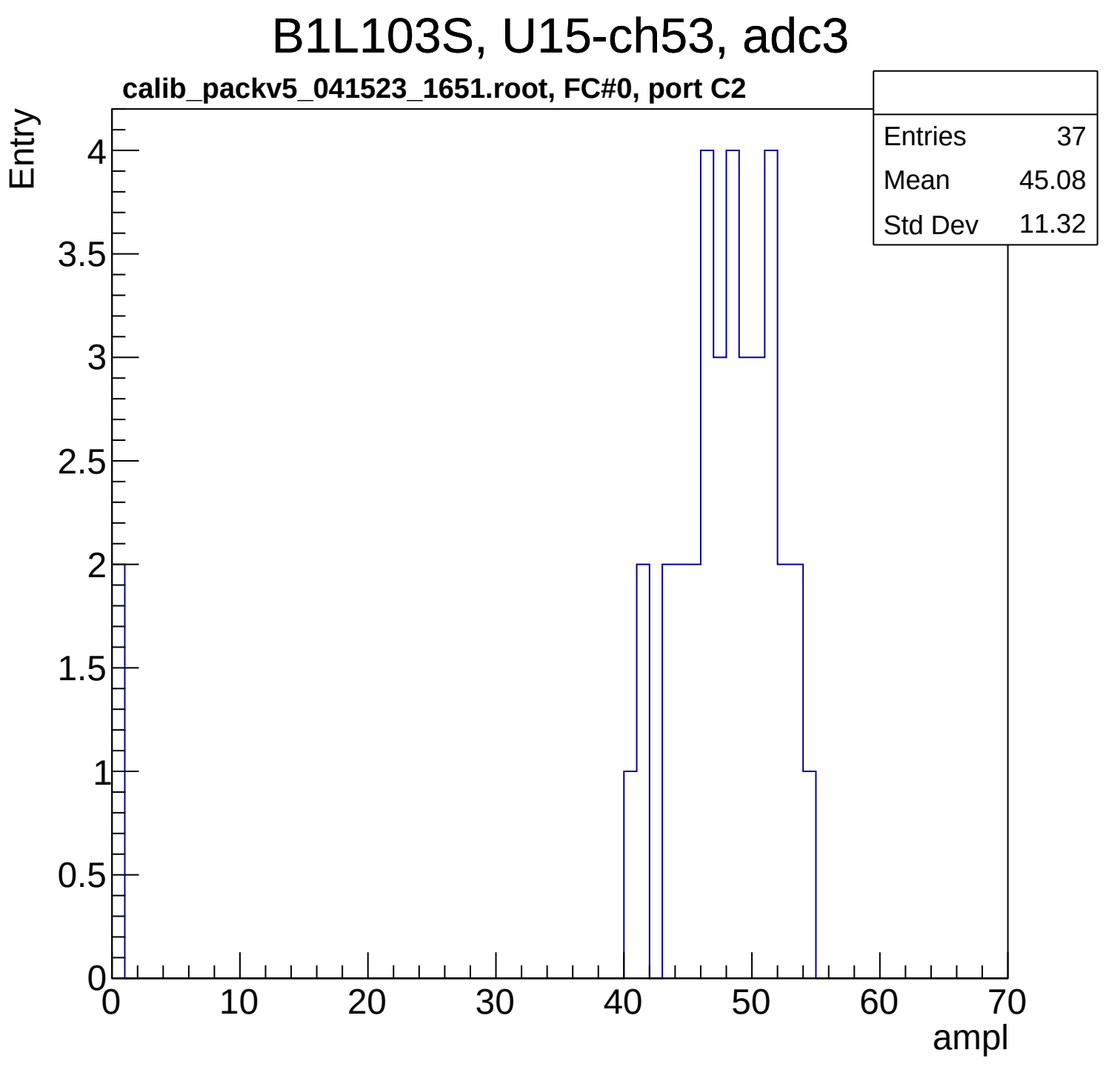
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch52, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 10.42
Std Dev 23.29
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch53, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 22.28
Std Dev 9.957
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch53, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 32.37
Std Dev 7.818
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch53, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 37.68
Std Dev 12.12
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch53, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 45.08
Std Dev 11.32
Entry
ampl
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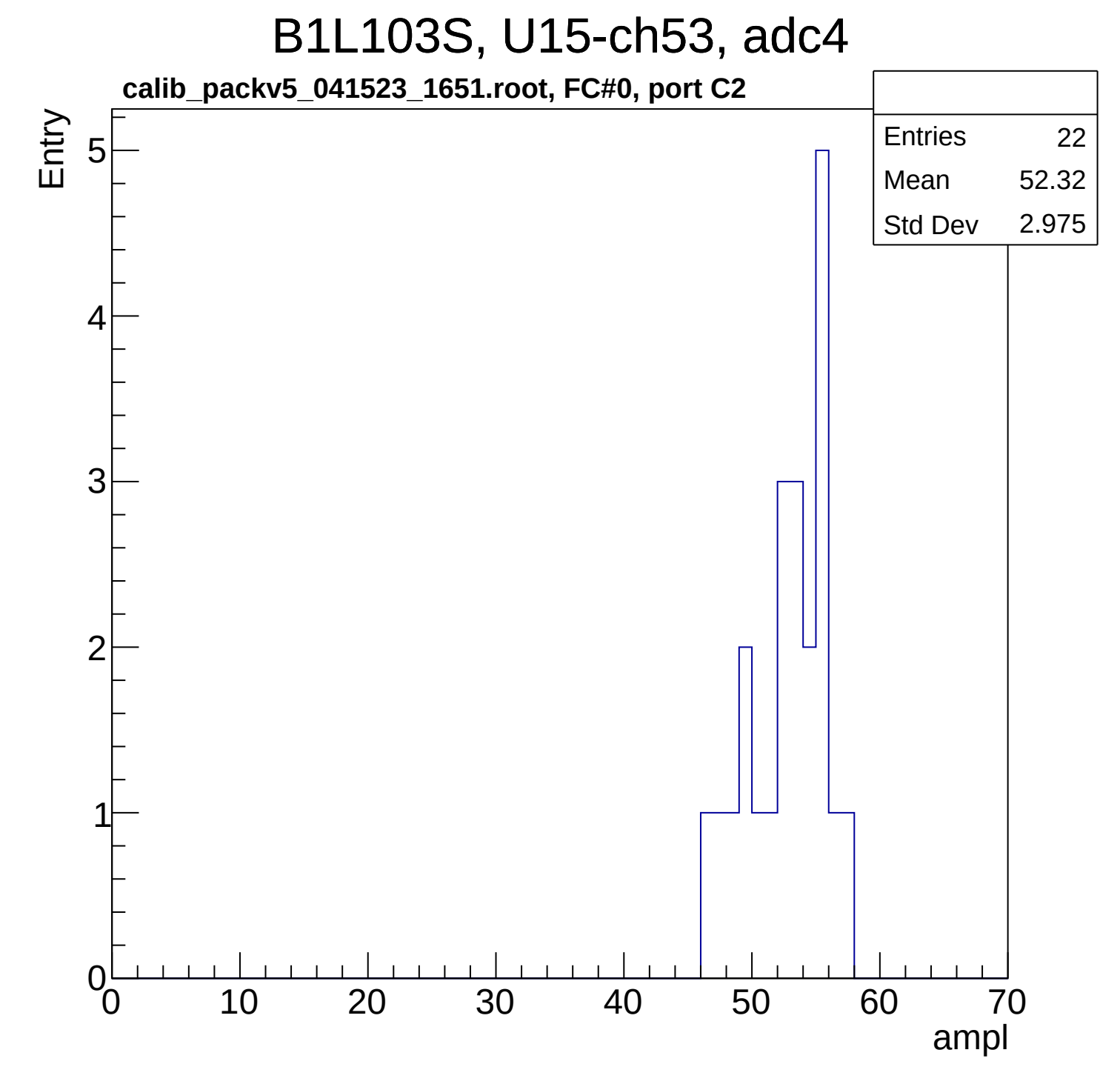
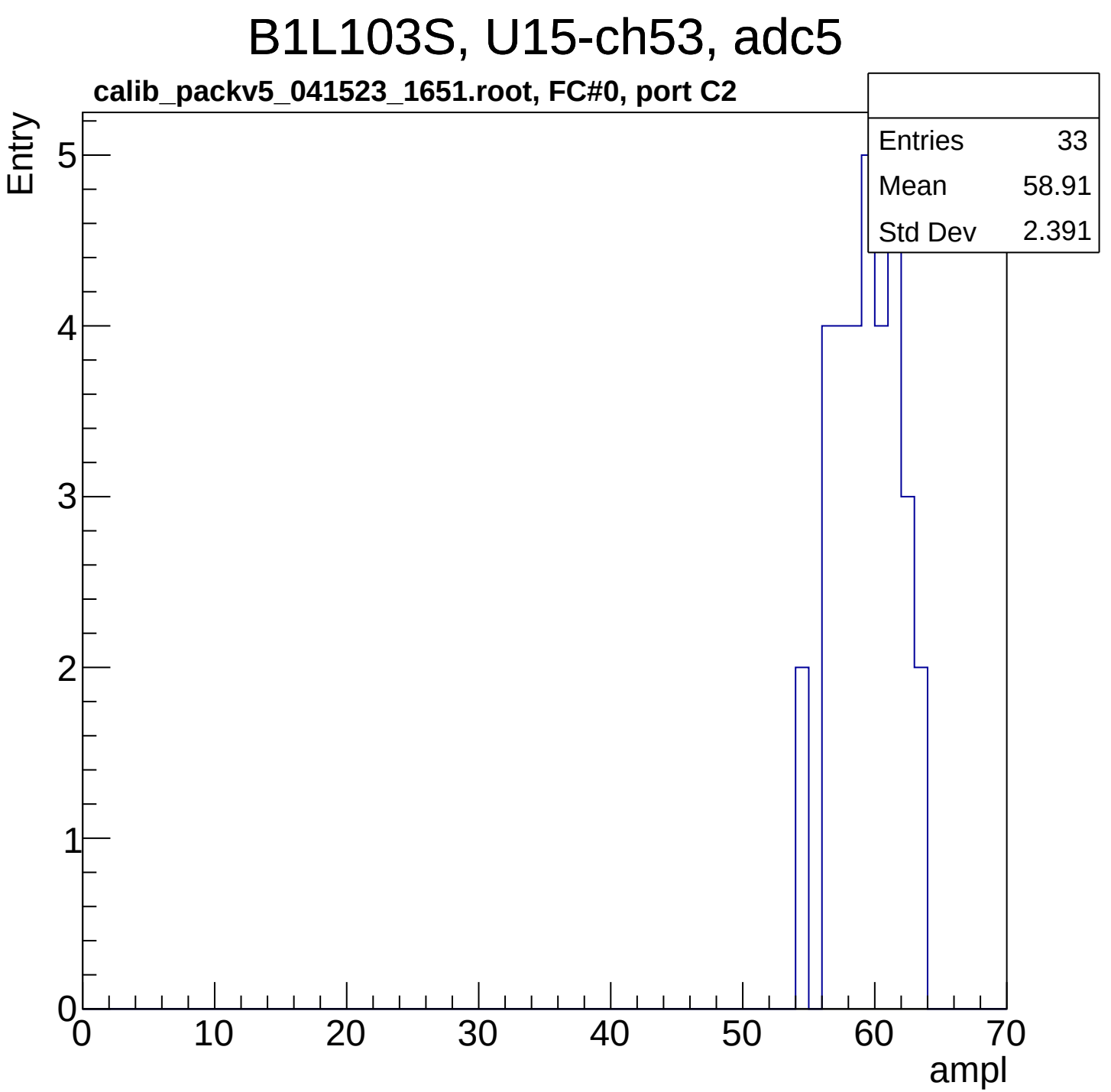
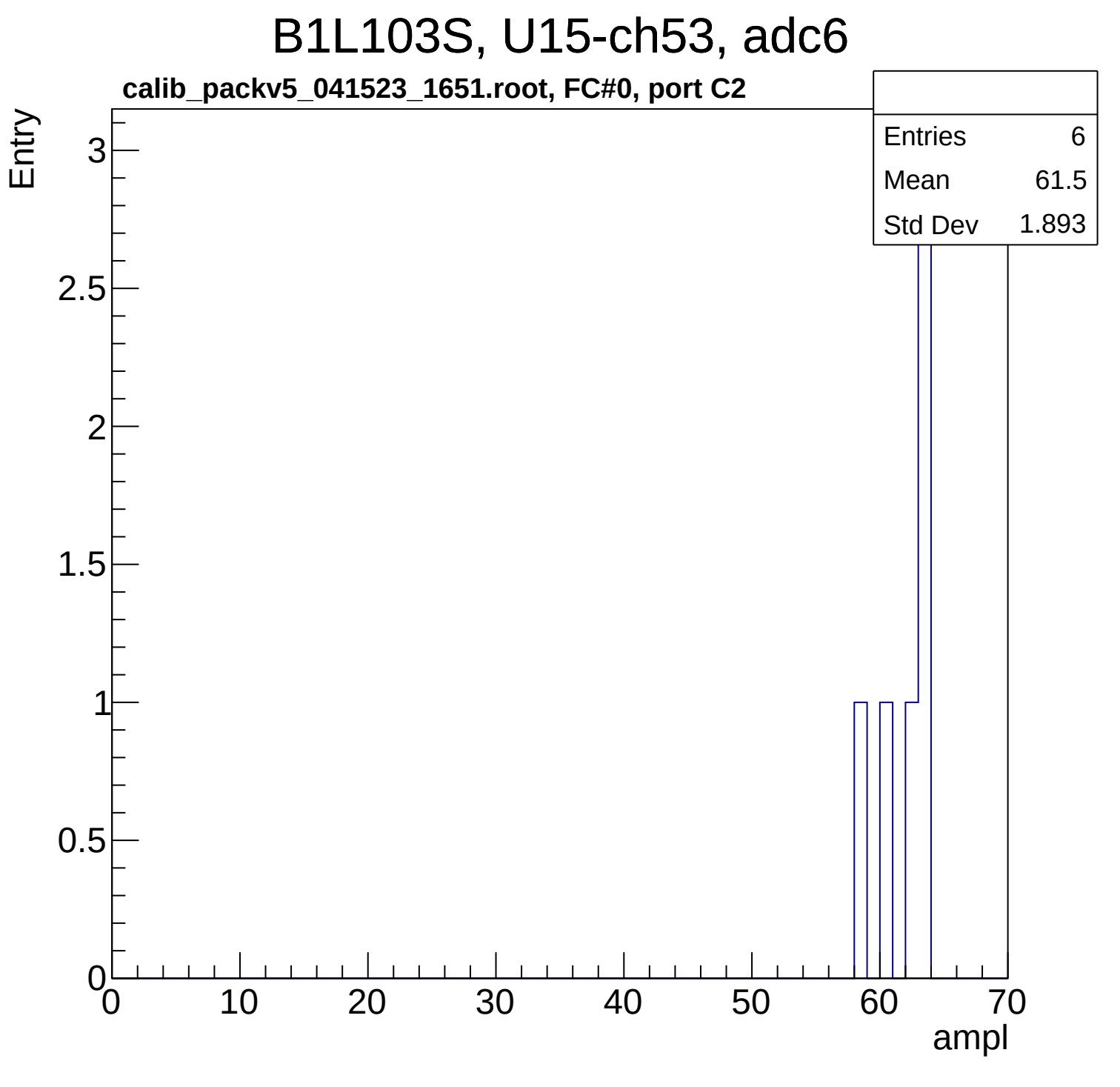
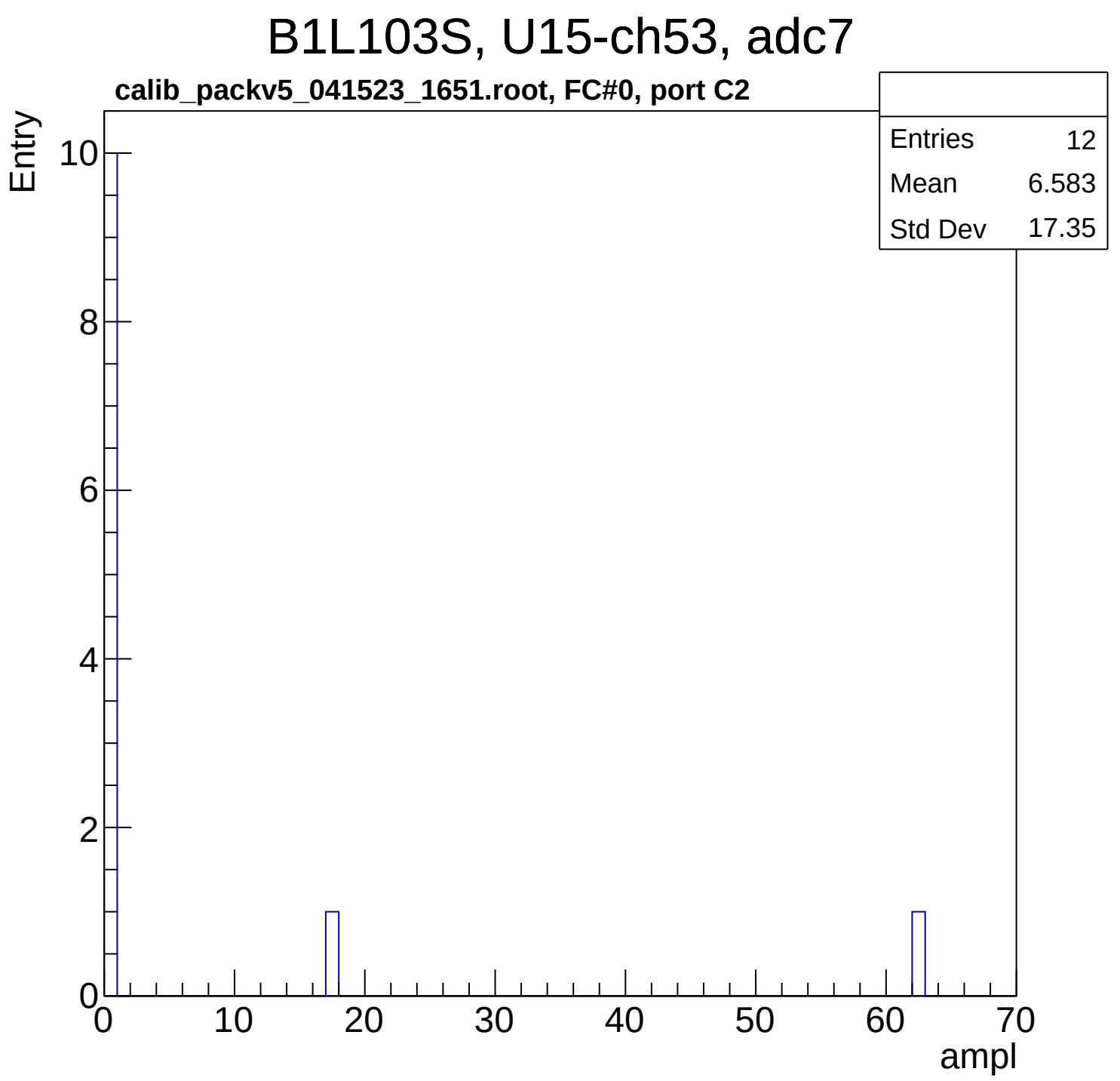
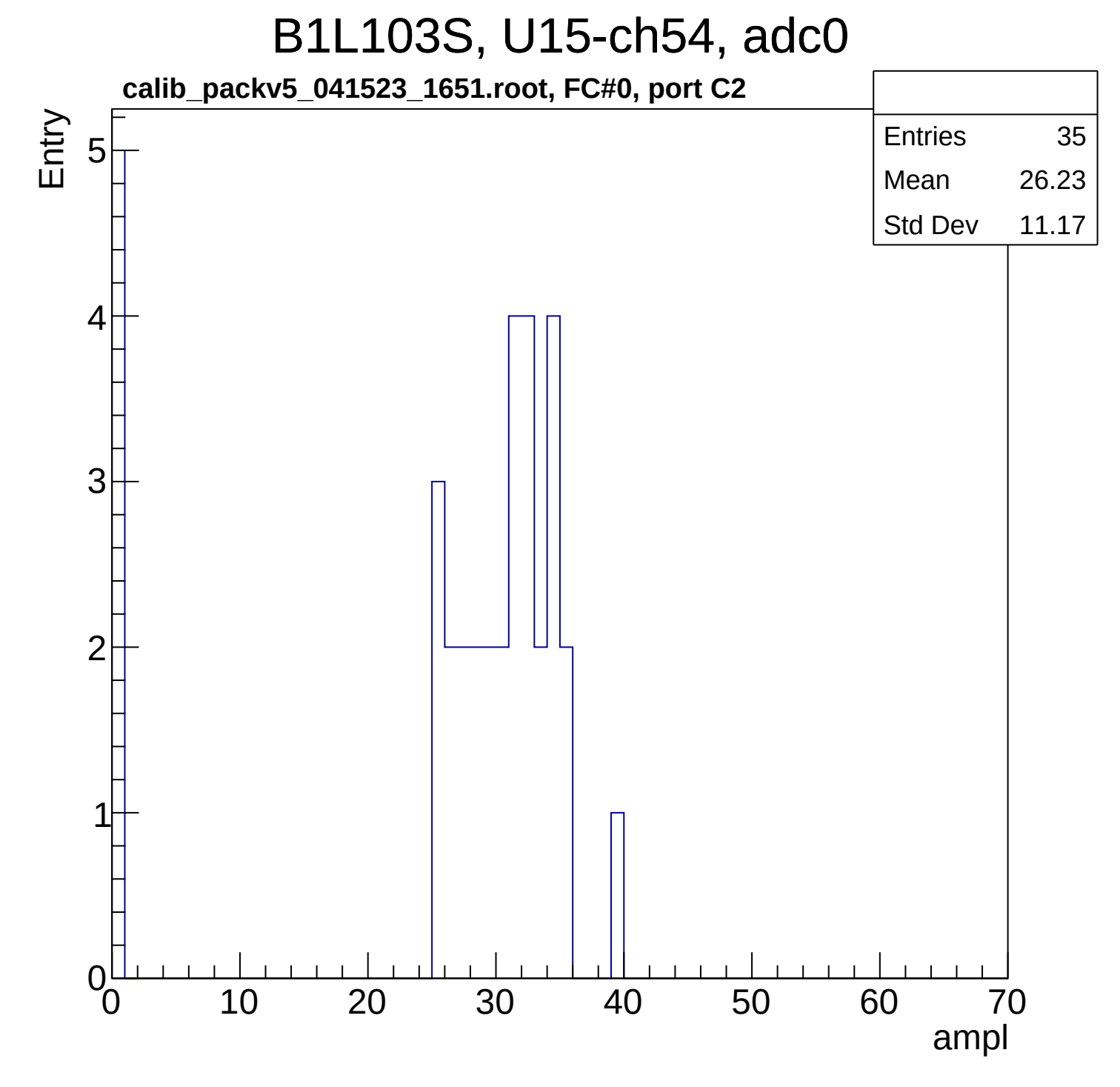
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

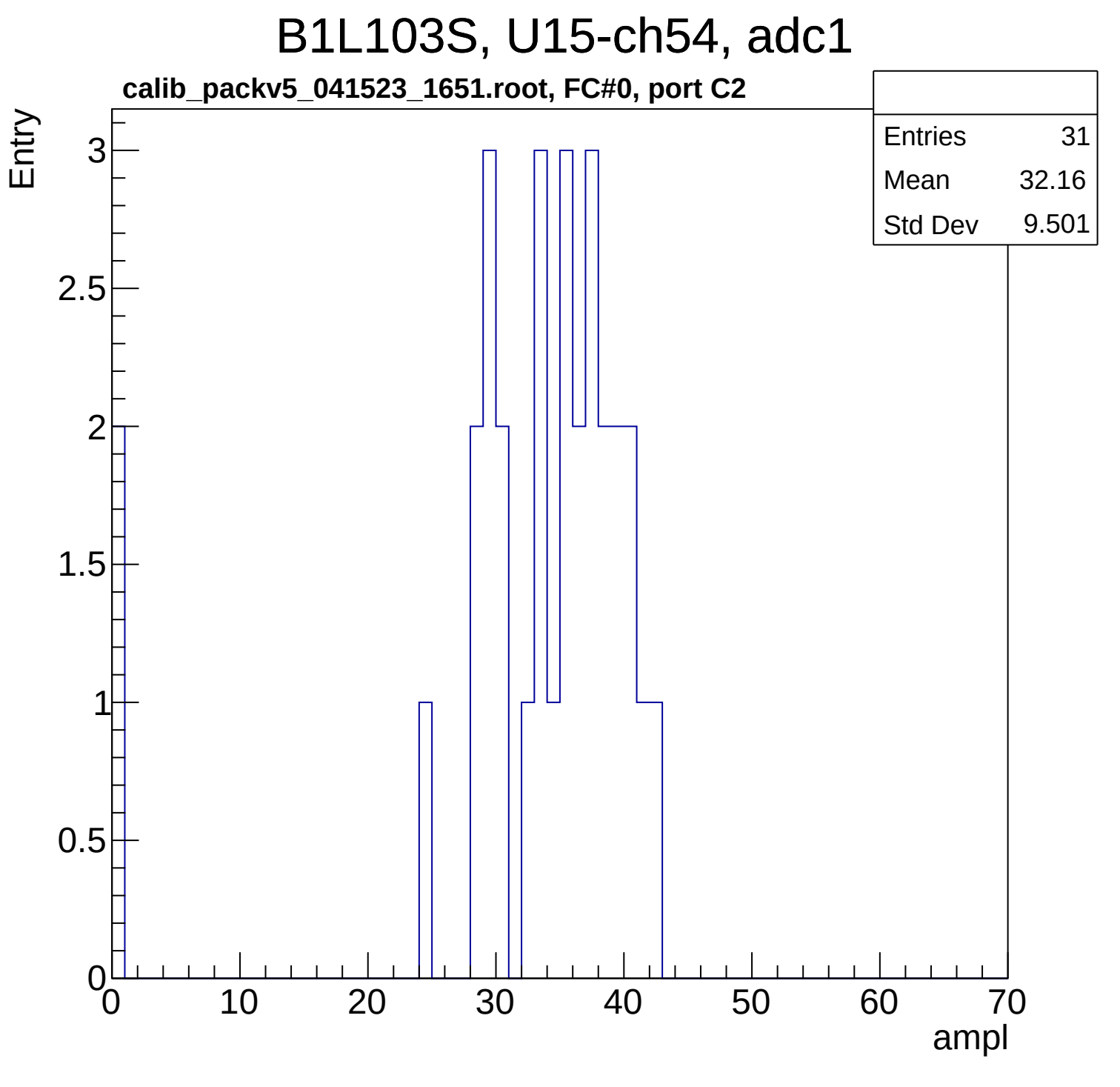

B1L103S, U15-ch53, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 52.32
Std Dev 2.975
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

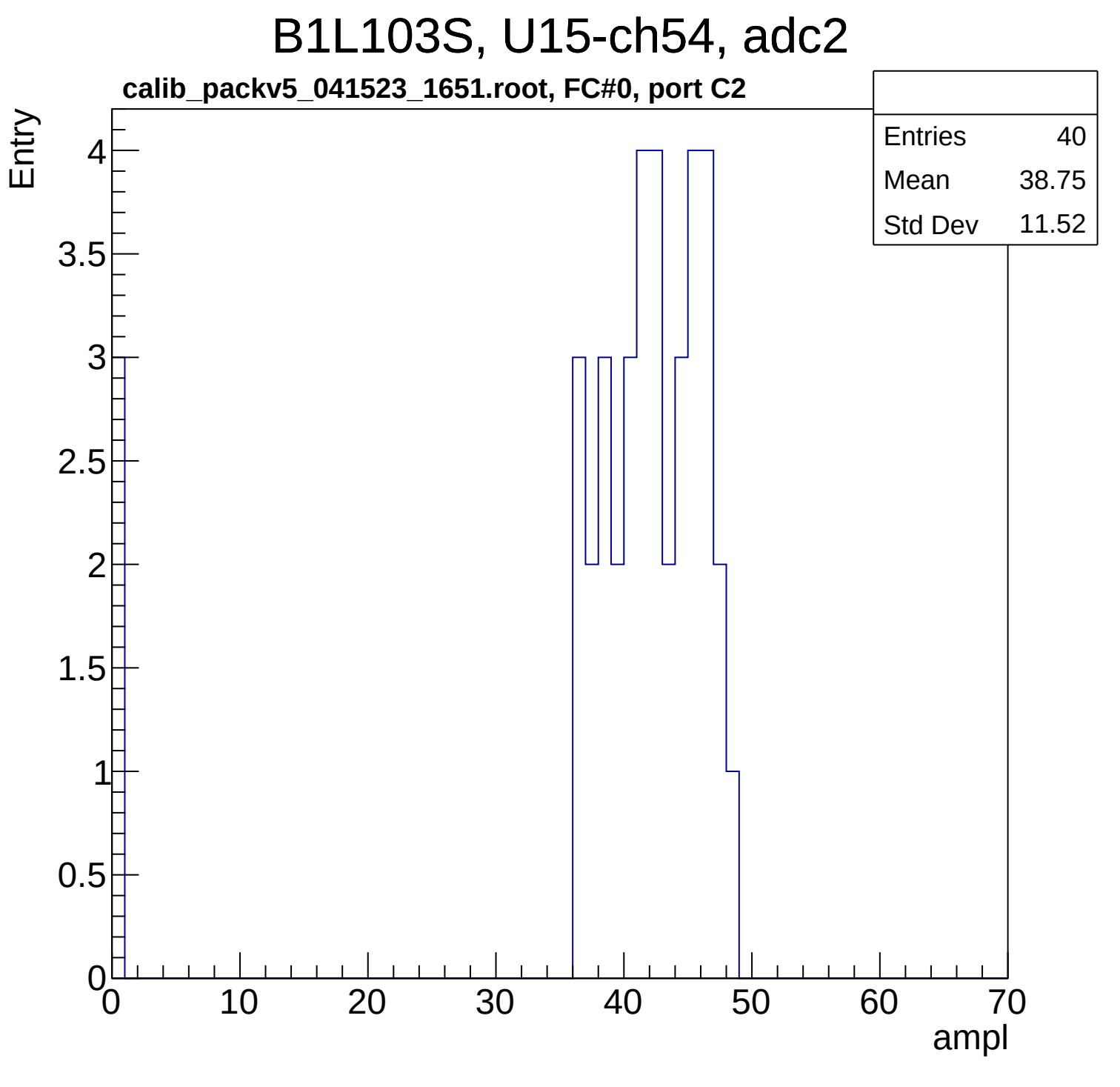

B1L103S, U15-ch53, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 58.91
Std Dev 2.391
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

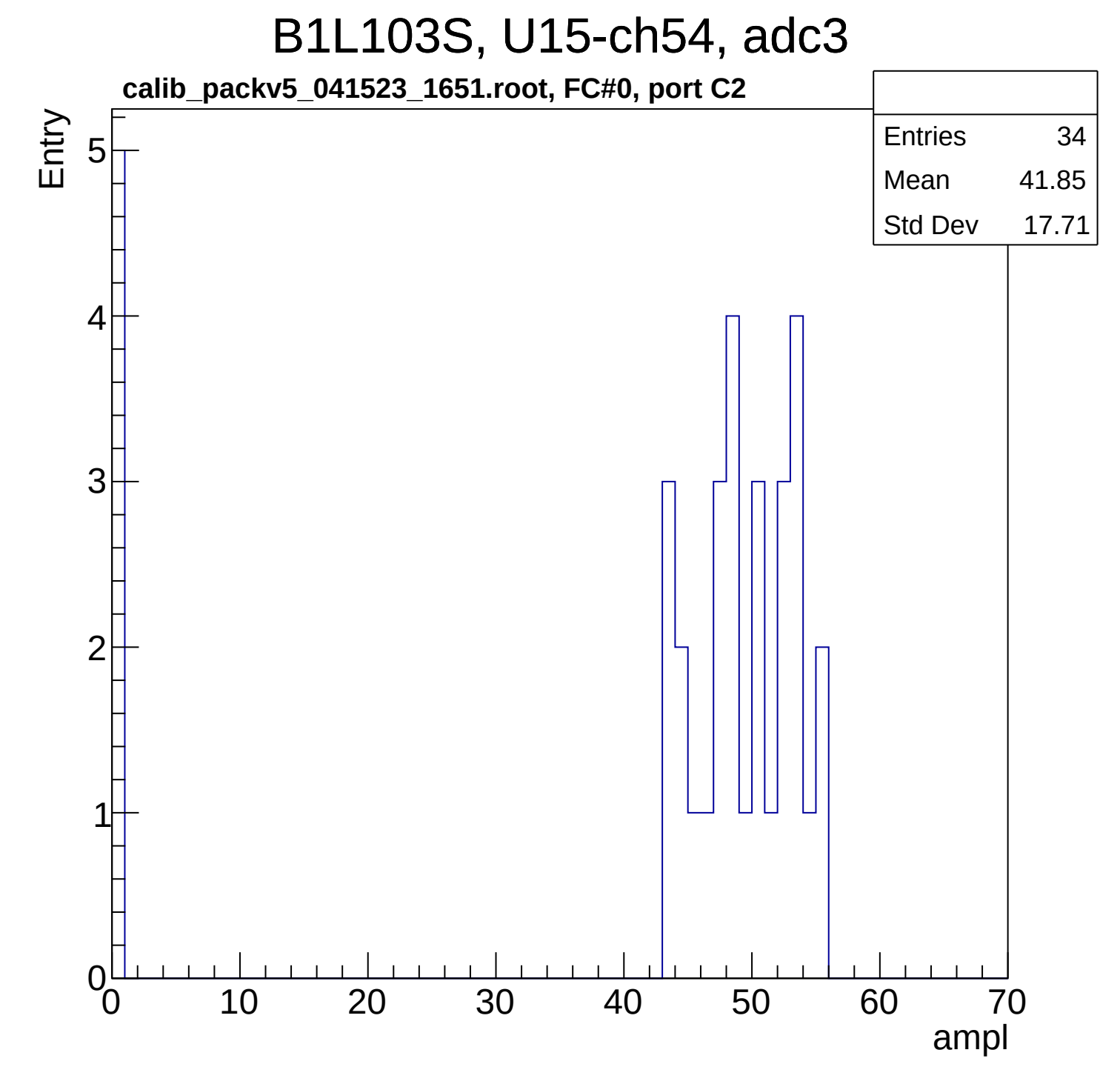

B1L103S, U15-ch53, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.5
Std Dev 1.893
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

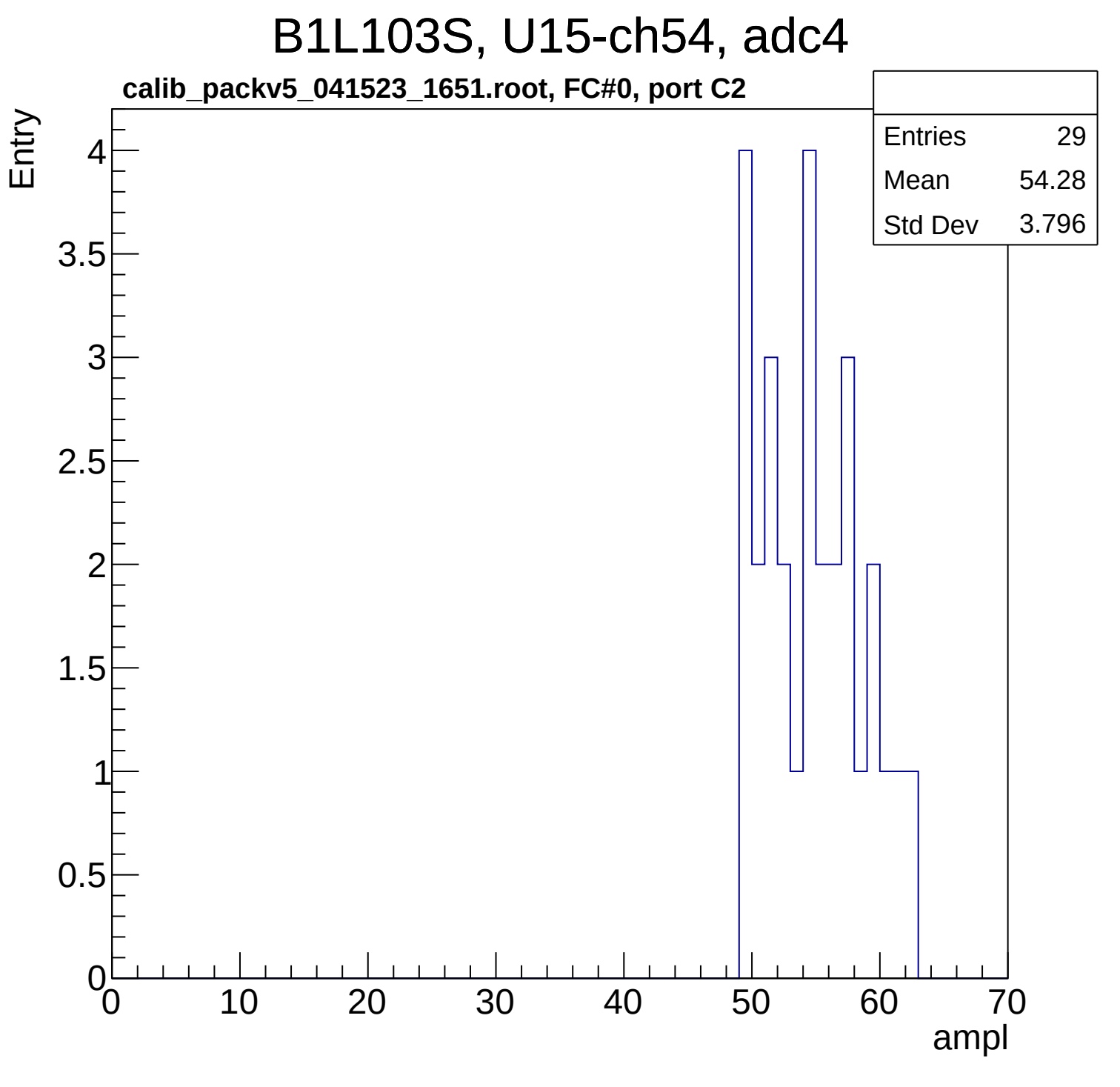

B1L103S, U15-ch53, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 6.583
Std Dev 17.35
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U15-ch54, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 26.23
Std Dev 11.17
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch54, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 32.16
Std Dev 9.501
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch54, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 38.75
Std Dev 11.52
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch54, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 41.85
Std Dev 17.71
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch54, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 54.28
Std Dev 3.796
Entry
ampl
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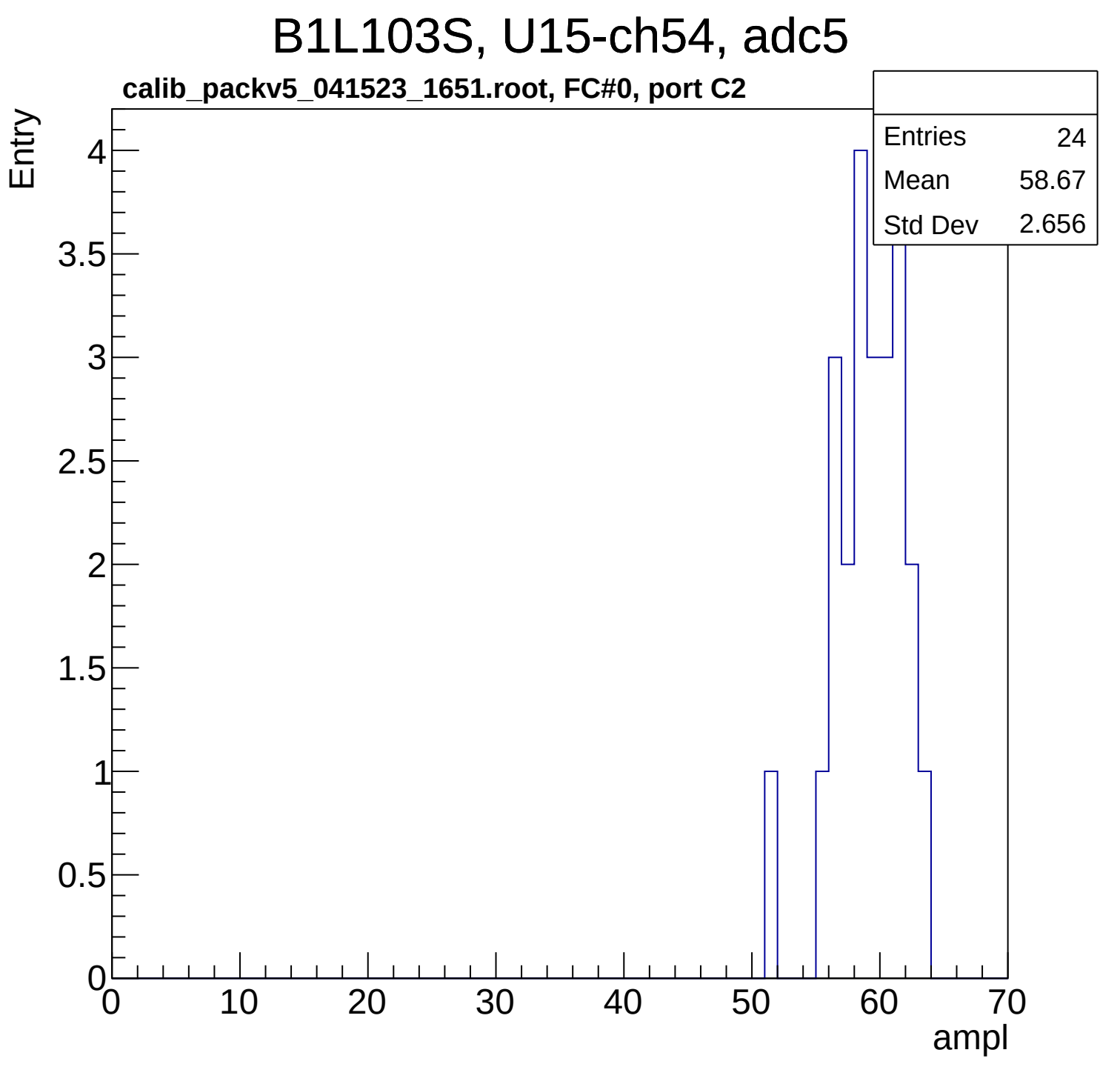
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch54, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 58.67
Std Dev 2.656
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
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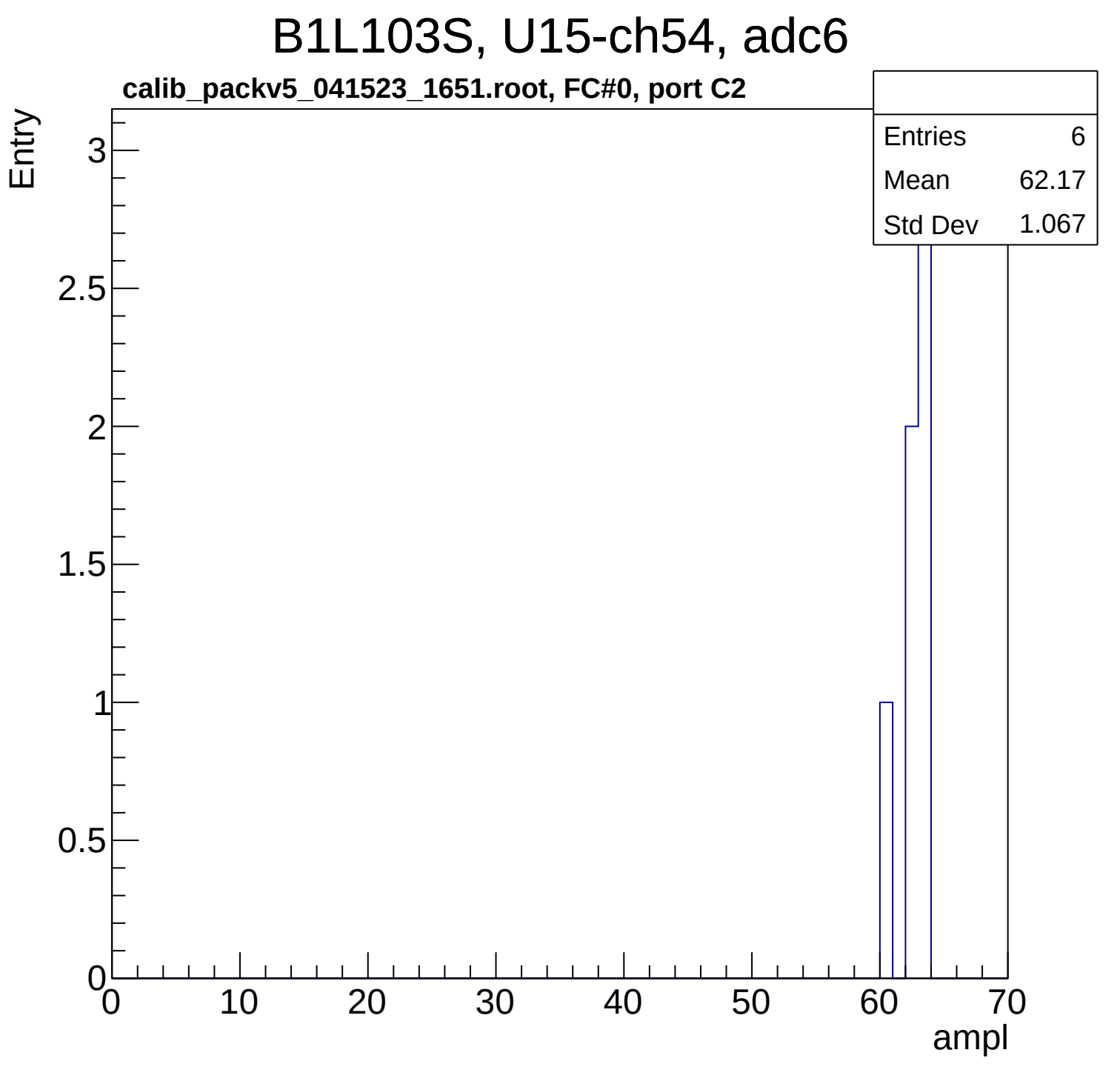
20
30
40
50
60
70


B1L103S, U15-ch54, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.17
Std Dev 1.067
Entry
ampl
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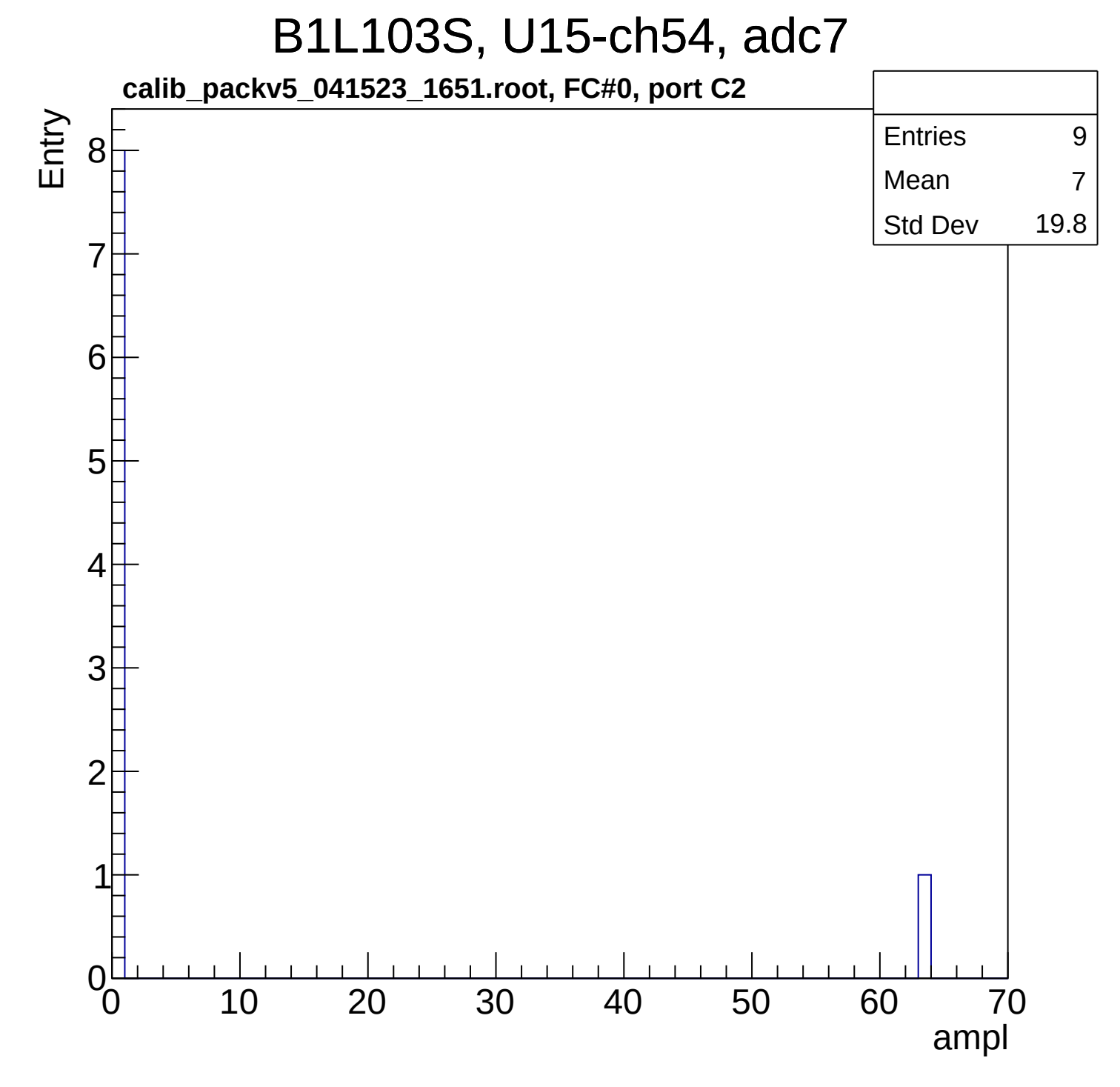
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch54, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 7
Std Dev 19.8
Entry
ampl
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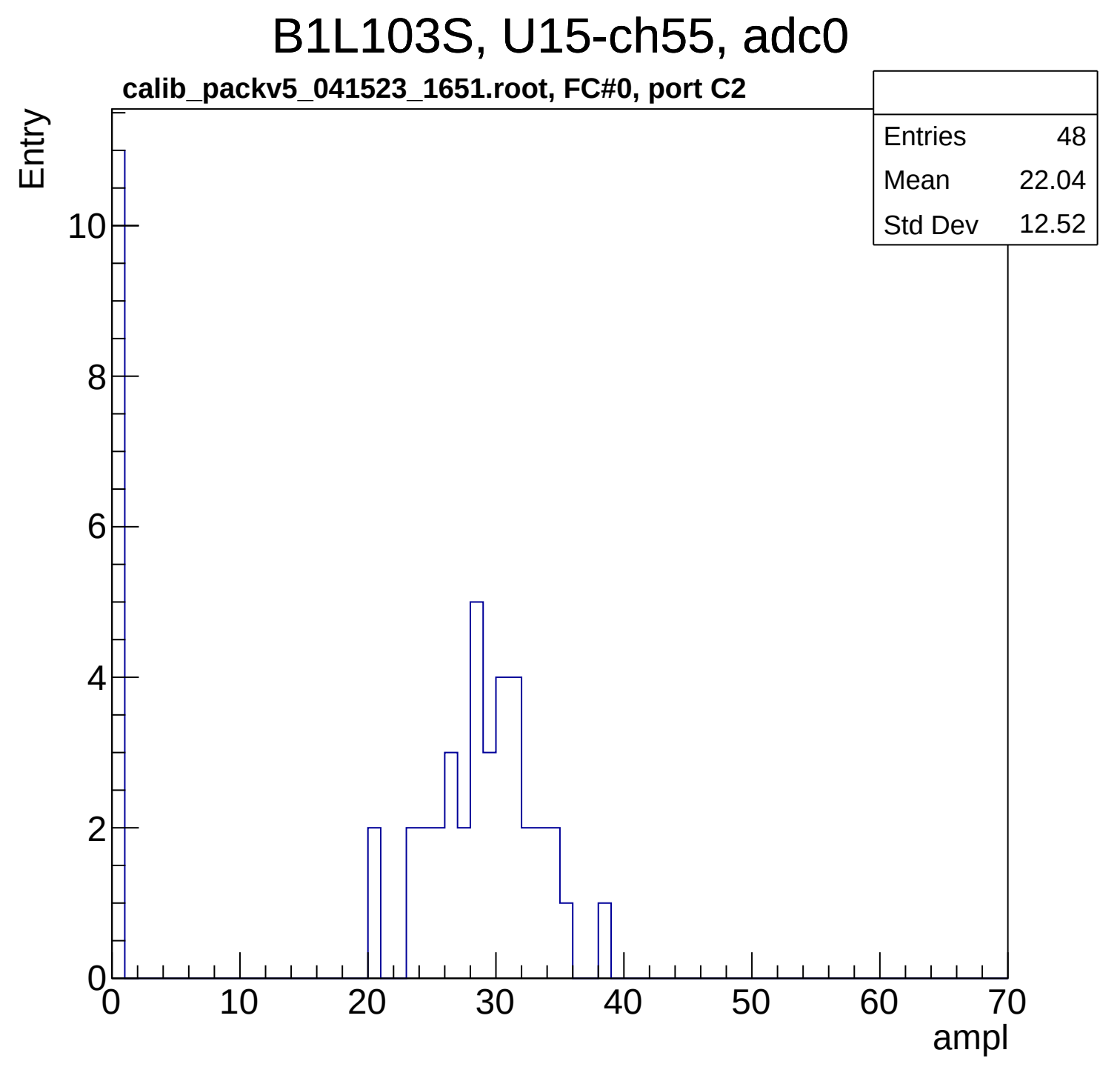
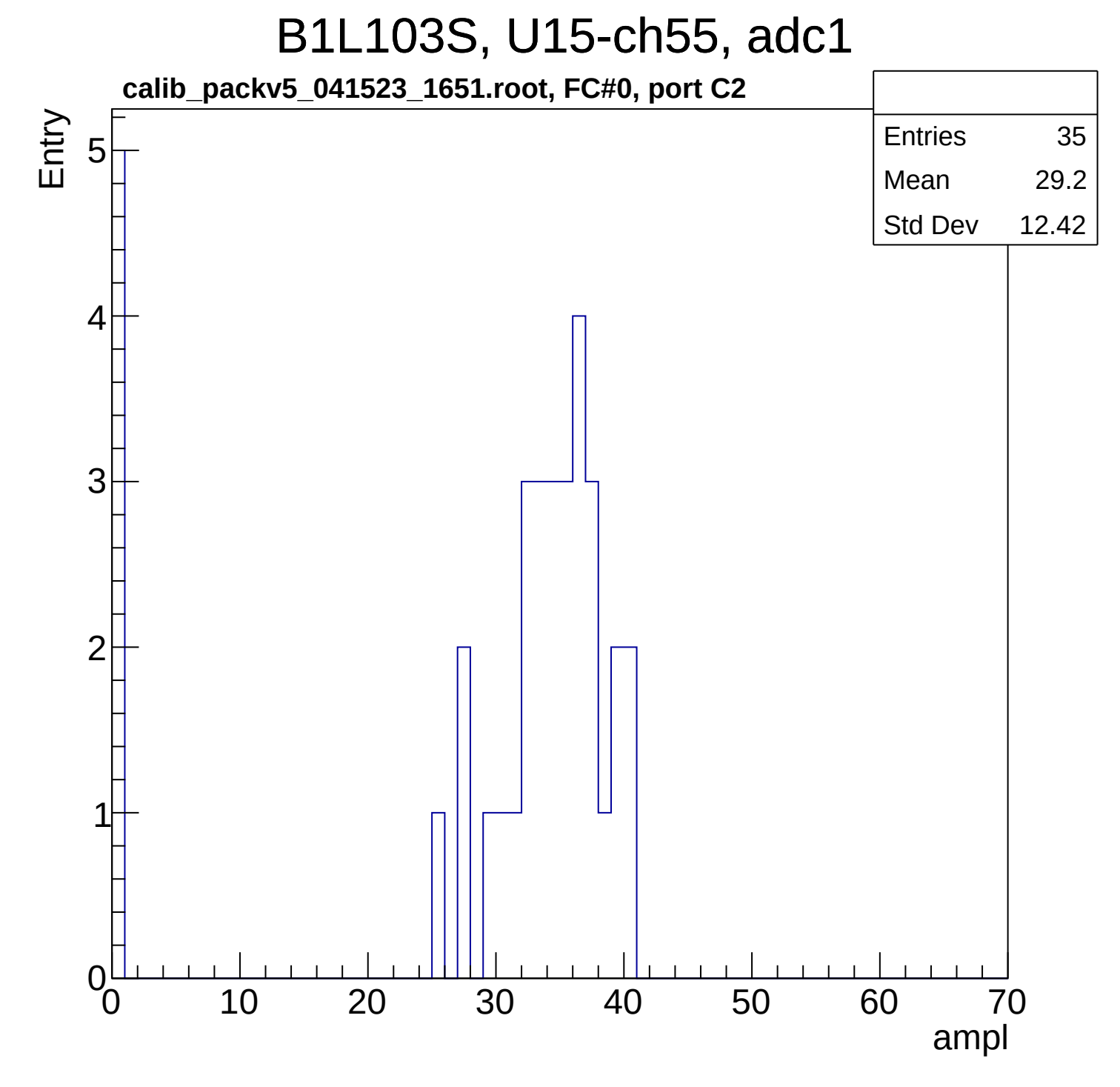
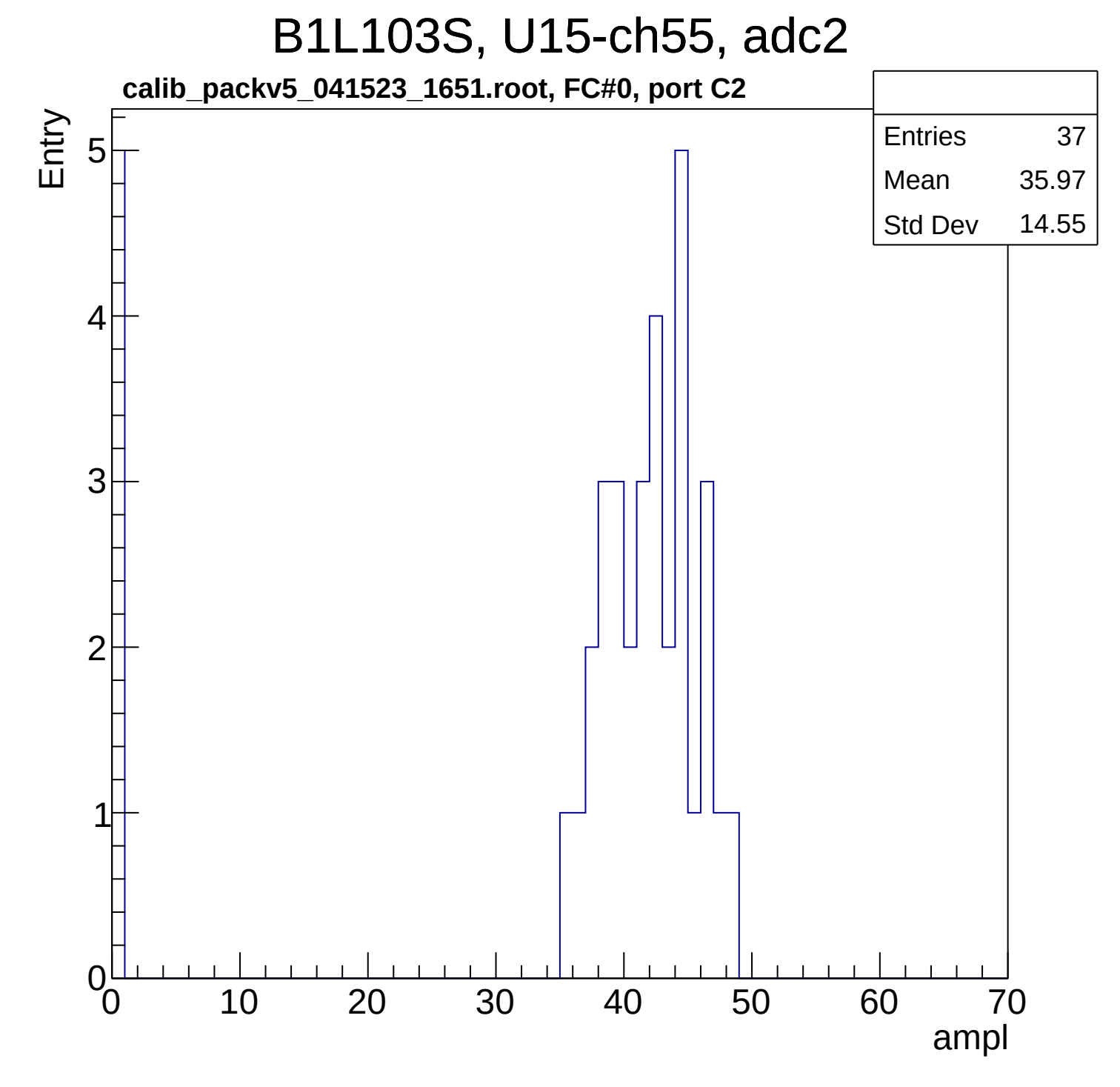
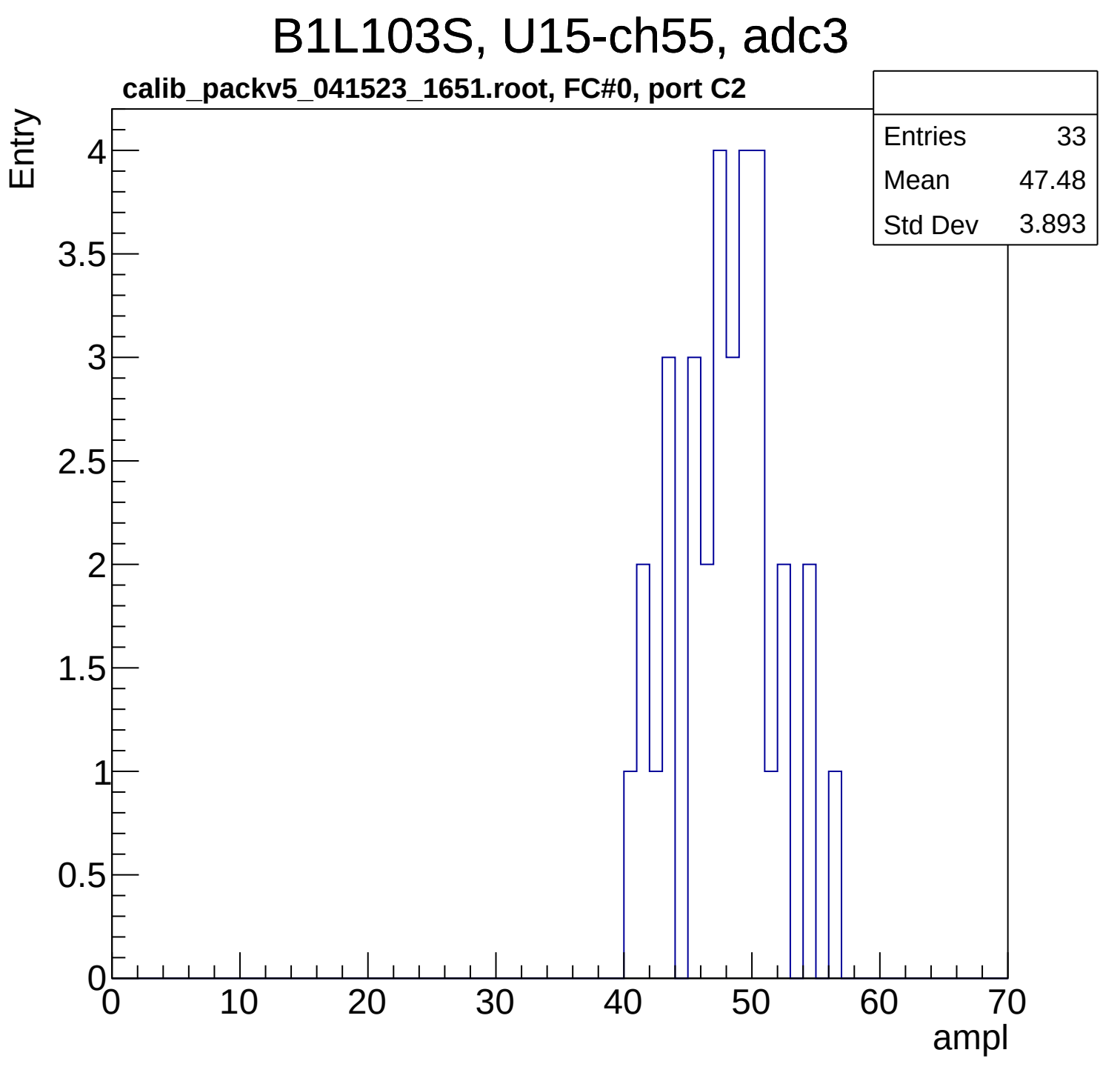
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U15-ch55, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 22.04
Std Dev 12.52
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch55, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 29.2
Std Dev 12.42
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch55, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 35.97
Std Dev 14.55
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch55, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 47.48
Std Dev 3.893
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
10
20
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40
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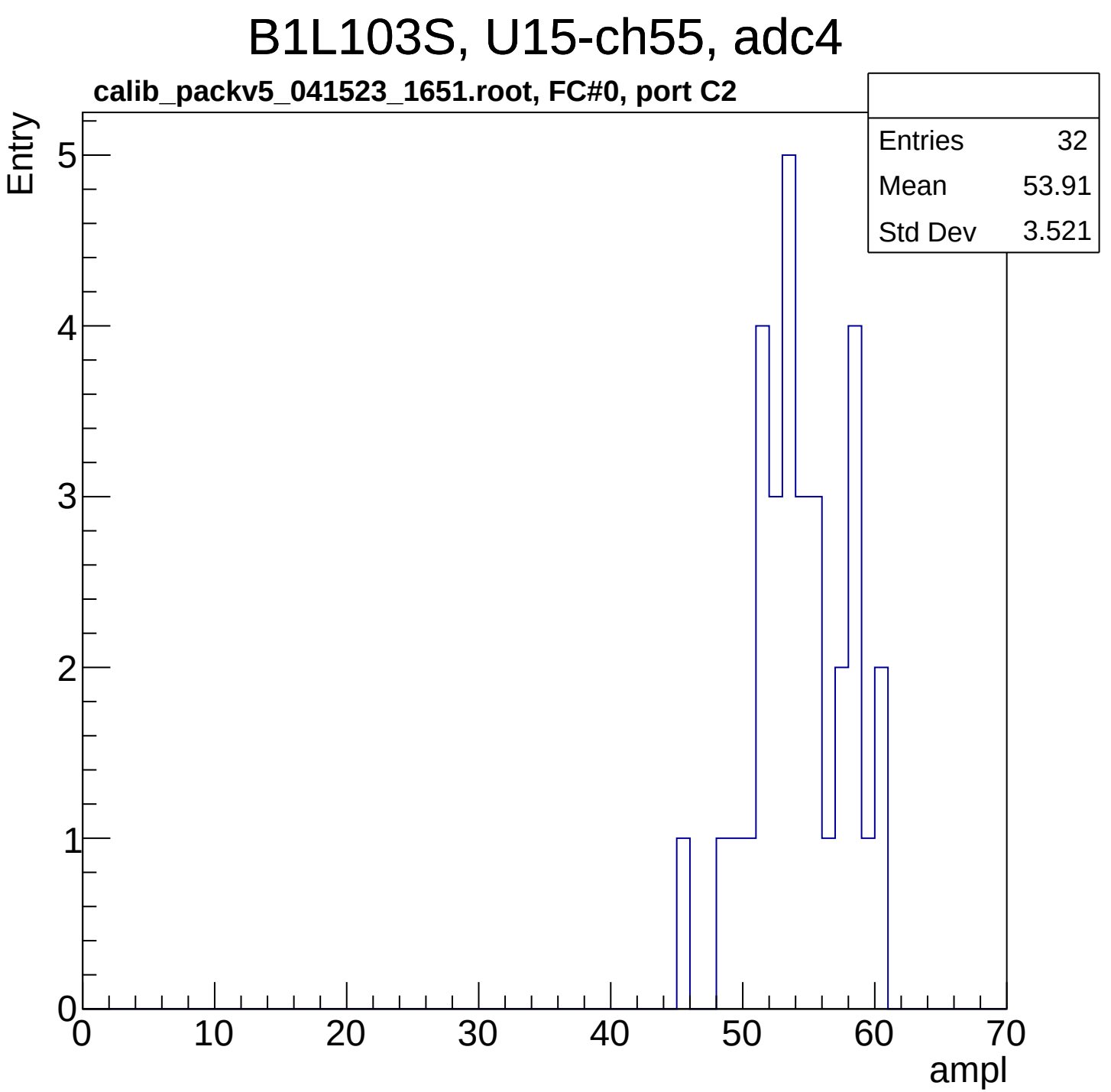
60
70


B1L103S, U15-ch55, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 53.91
Std Dev 3.521
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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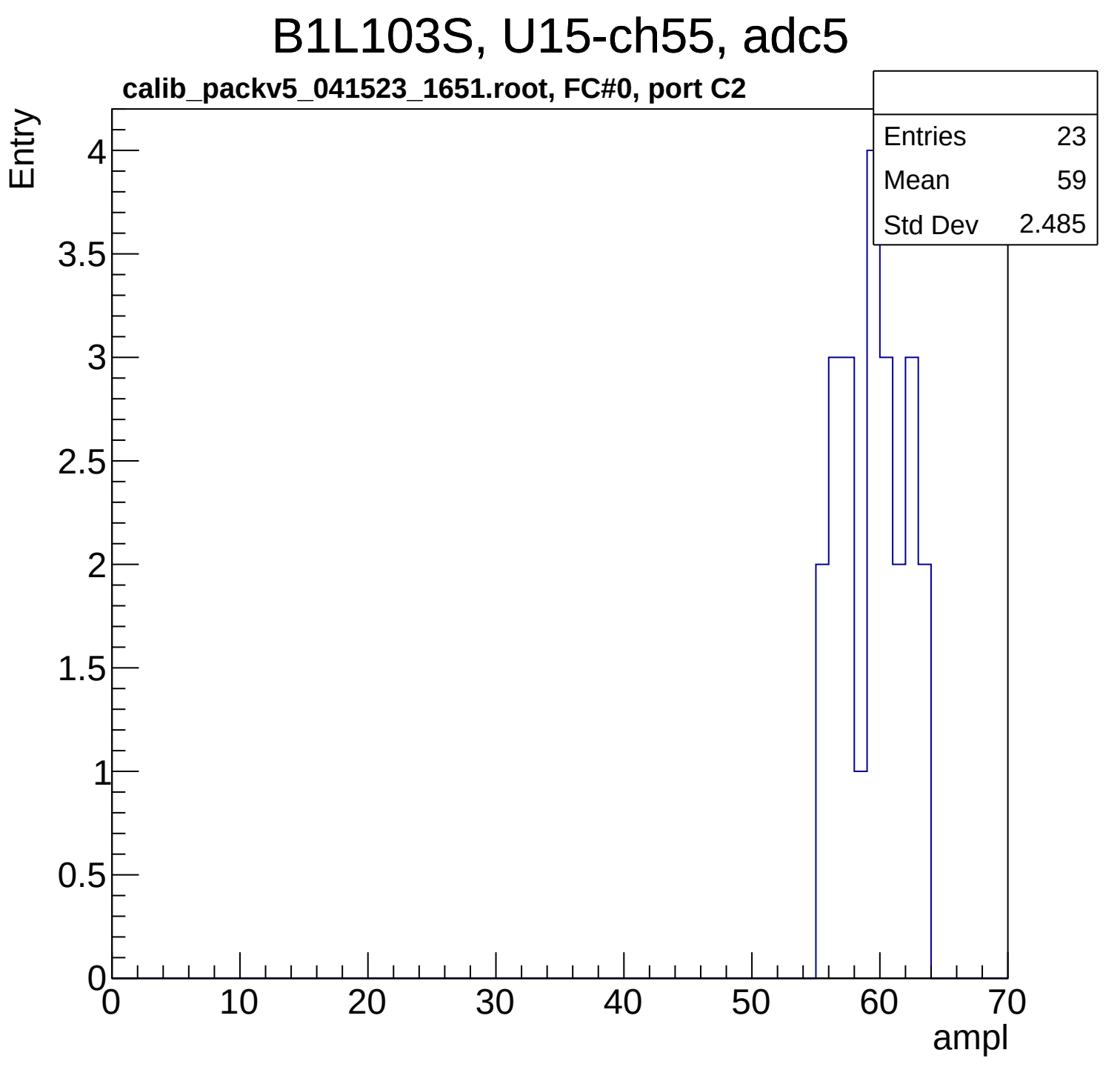
B1L103S, U15-ch55, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 59
Std Dev 2.485
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
10
20
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40
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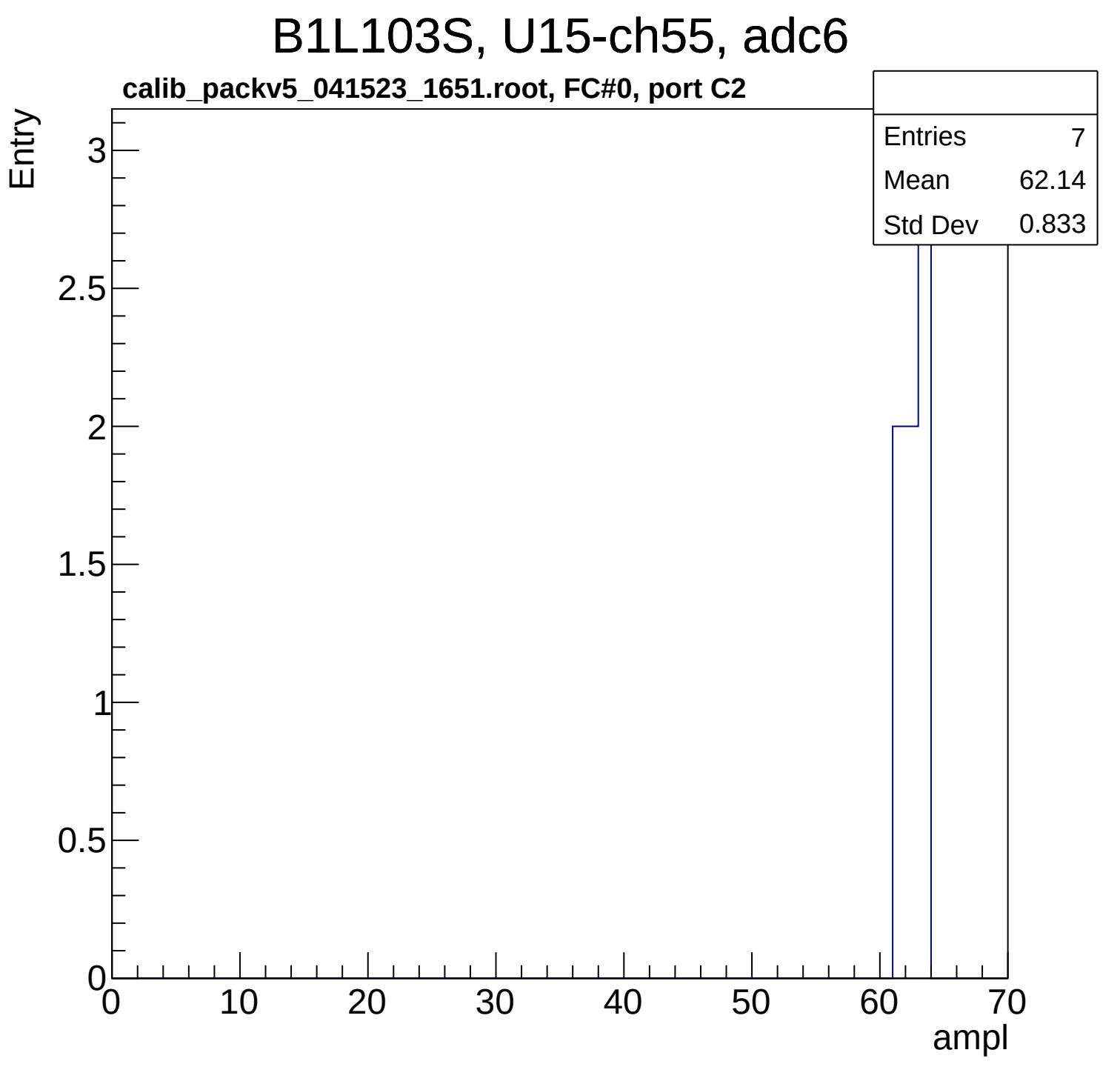
B1L103S, U15-ch55, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62.14
Std Dev 0.833
Entry
ampl
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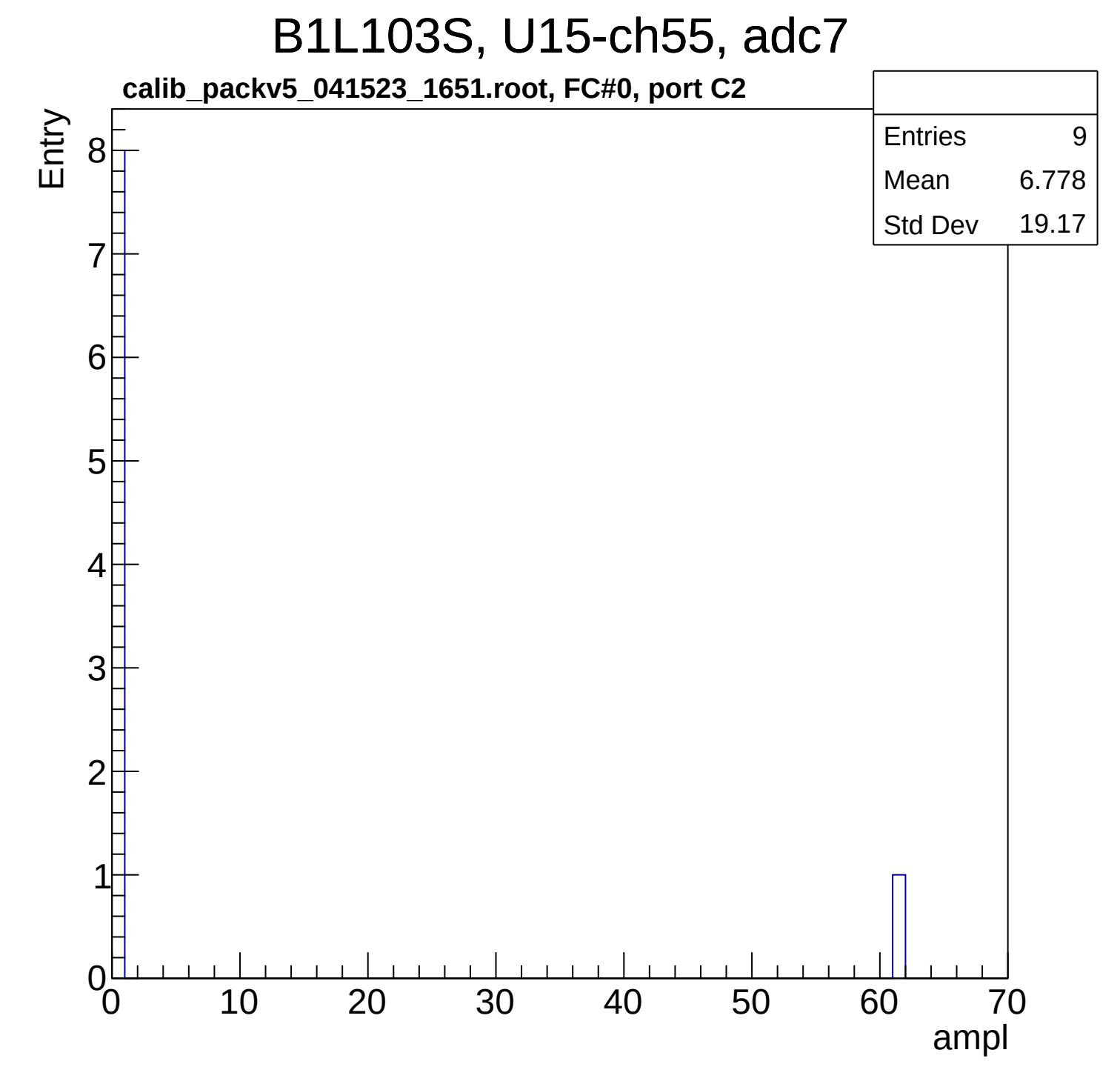
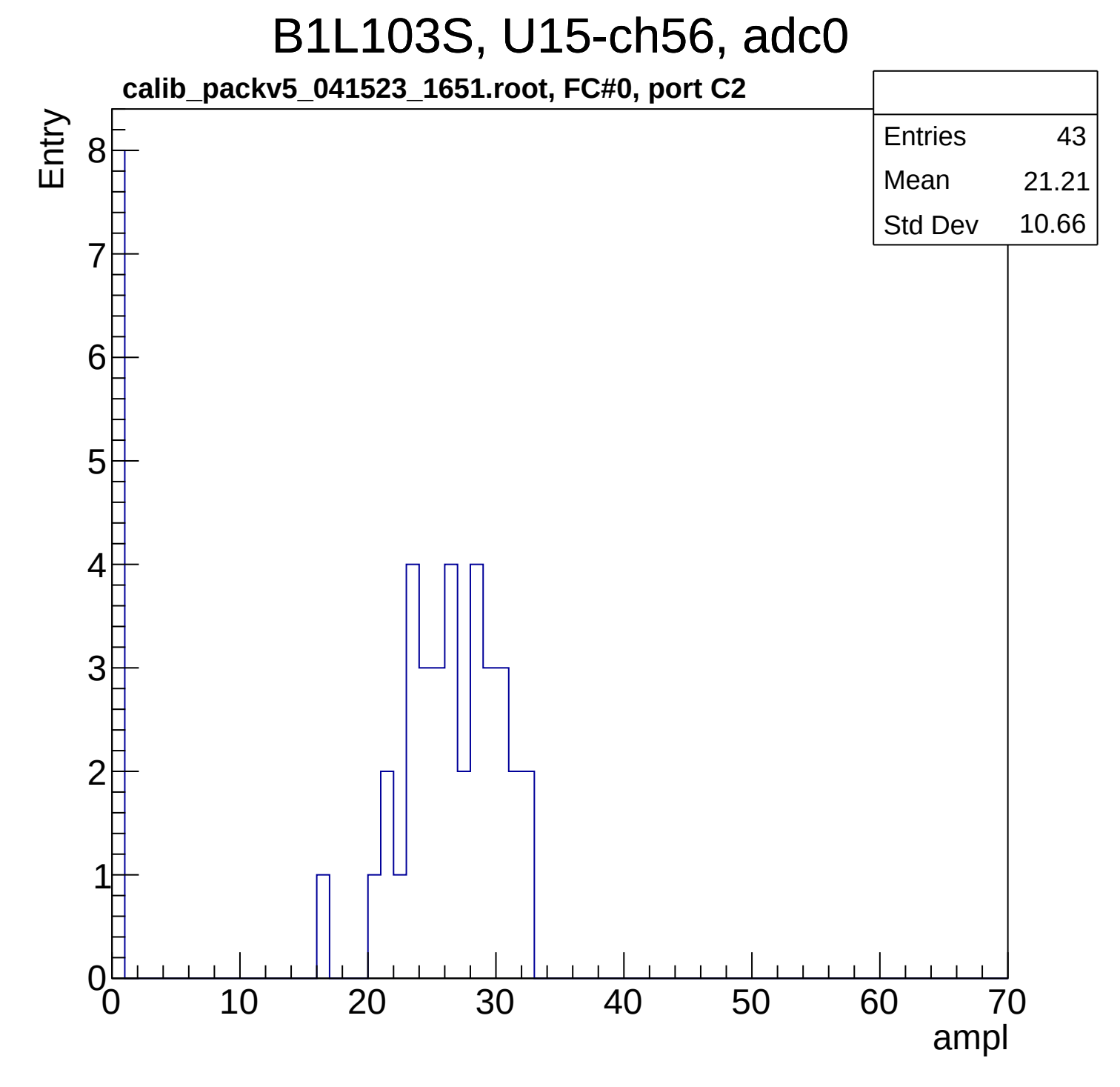
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch55, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 6.778
Std Dev 19.17
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch56, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 21.21
Std Dev 10.66
Entry
ampl
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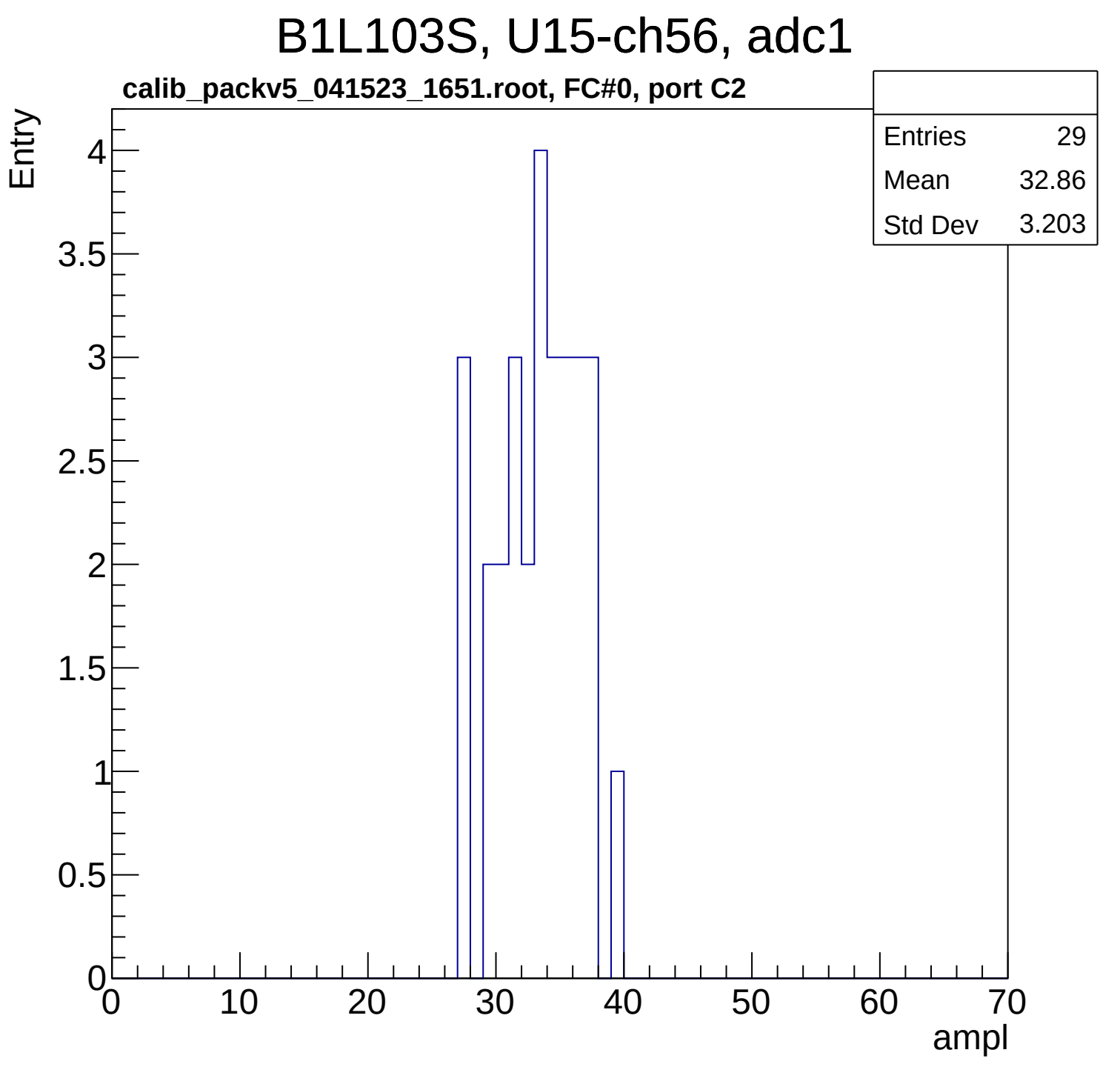
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U15-ch56, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 32.86
Std Dev 3.203
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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60
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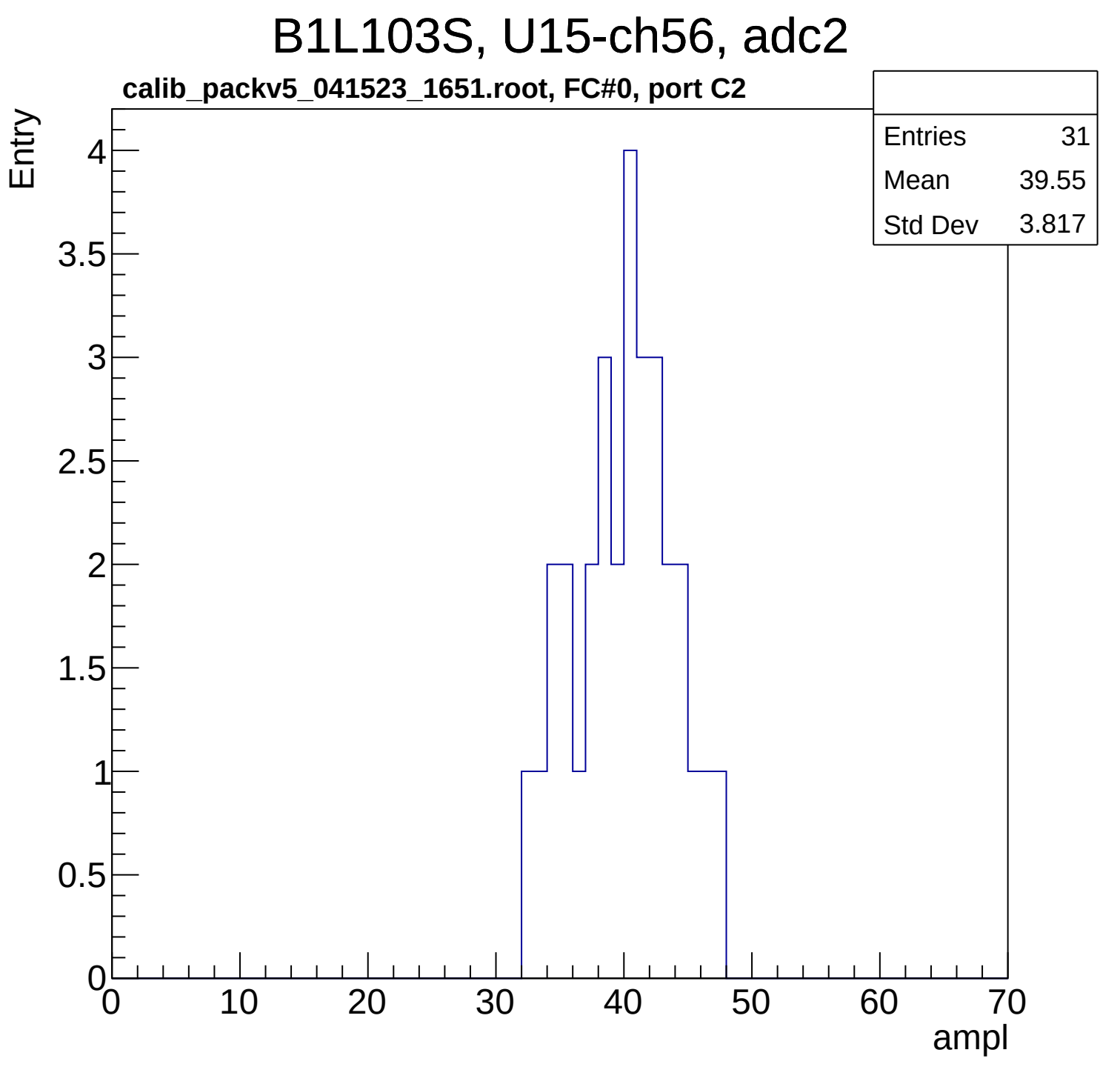
B1L103S, U15-ch56, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 39.55
Std Dev 3.817
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
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20
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40
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60
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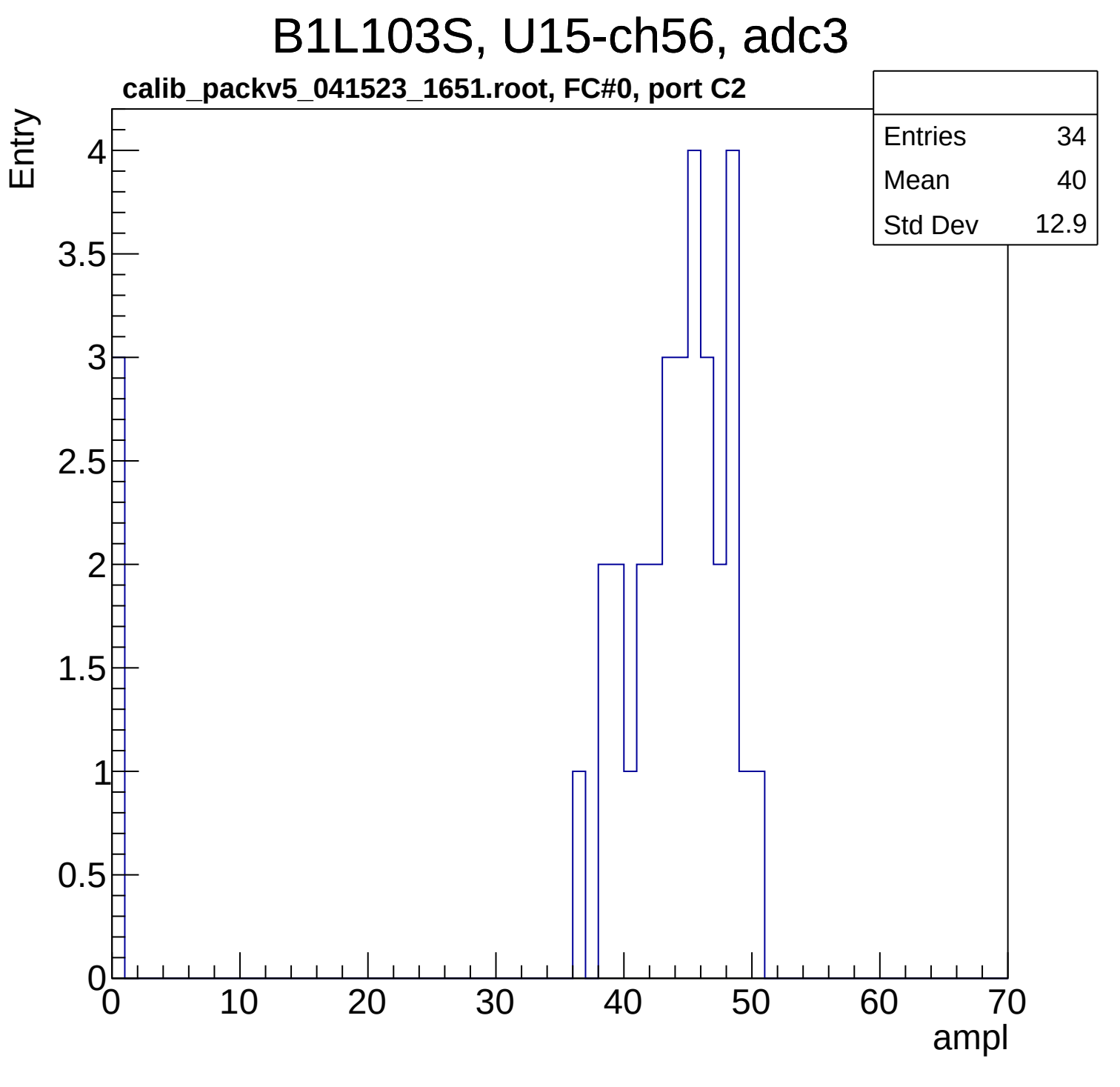
B1L103S, U15-ch56, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 40
Std Dev 12.9
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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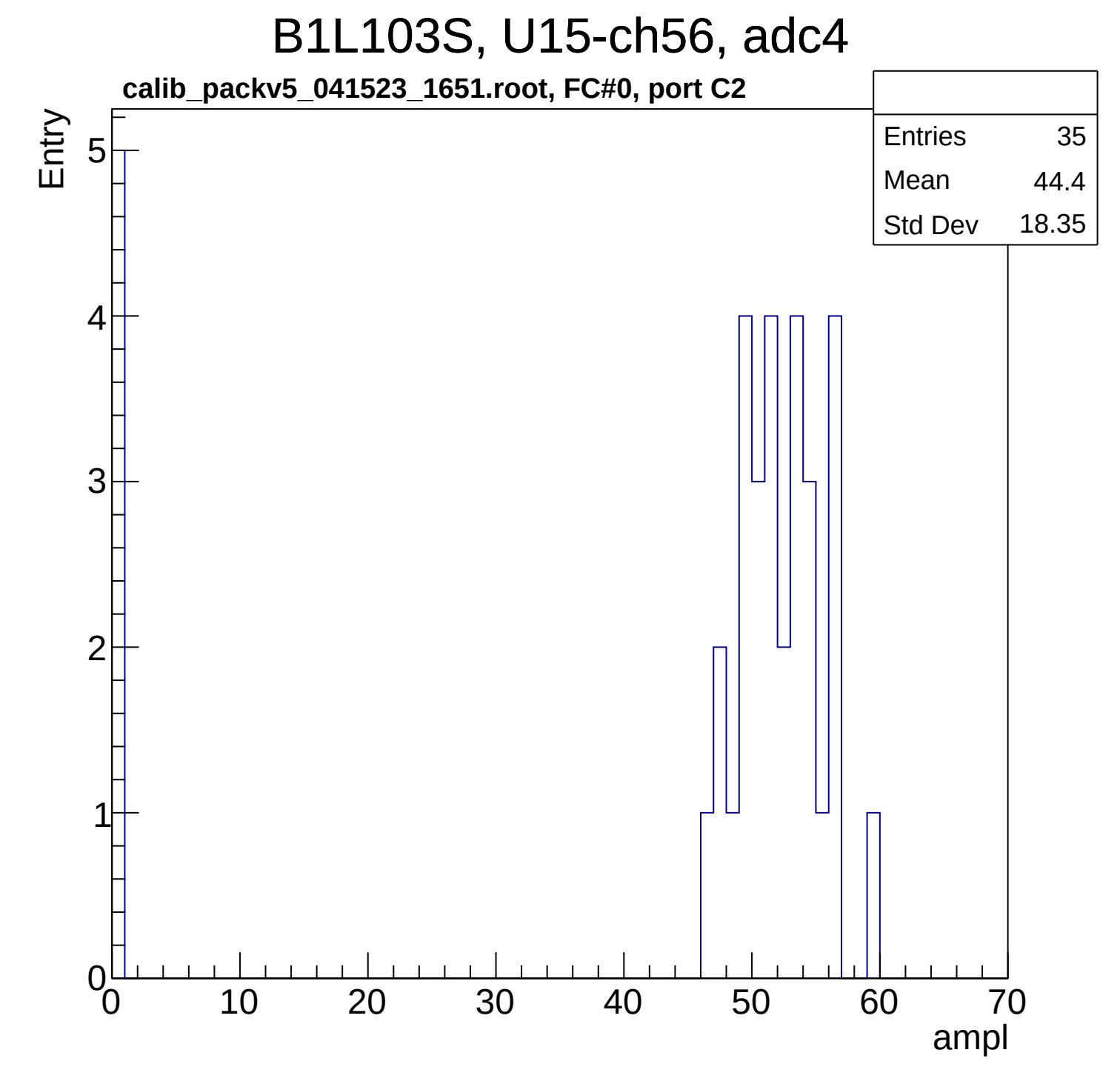
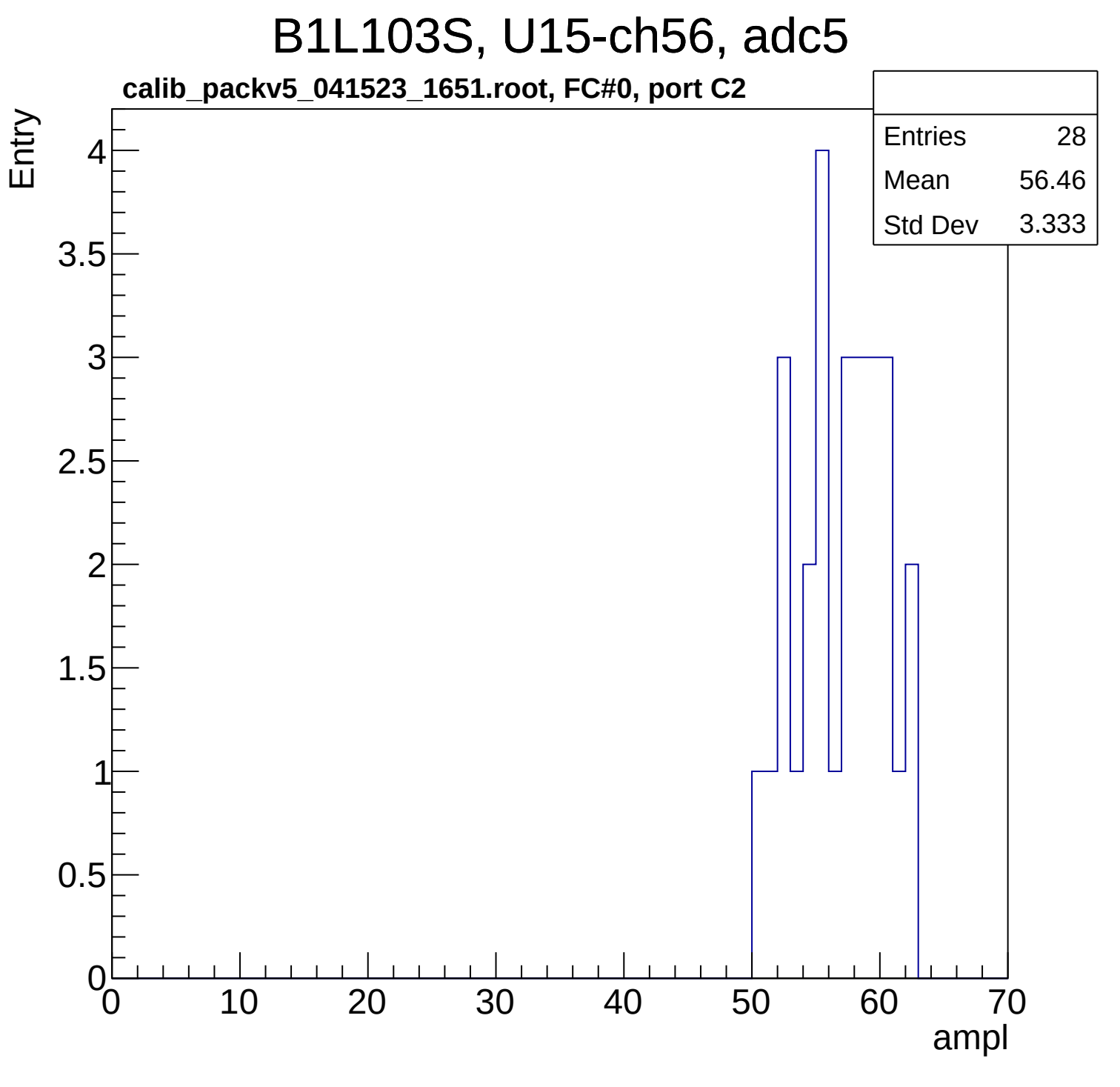

B1L103S, U15-ch56, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 44.4
Std Dev 18.35
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch56, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 56.46
Std Dev 3.333
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
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40
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60
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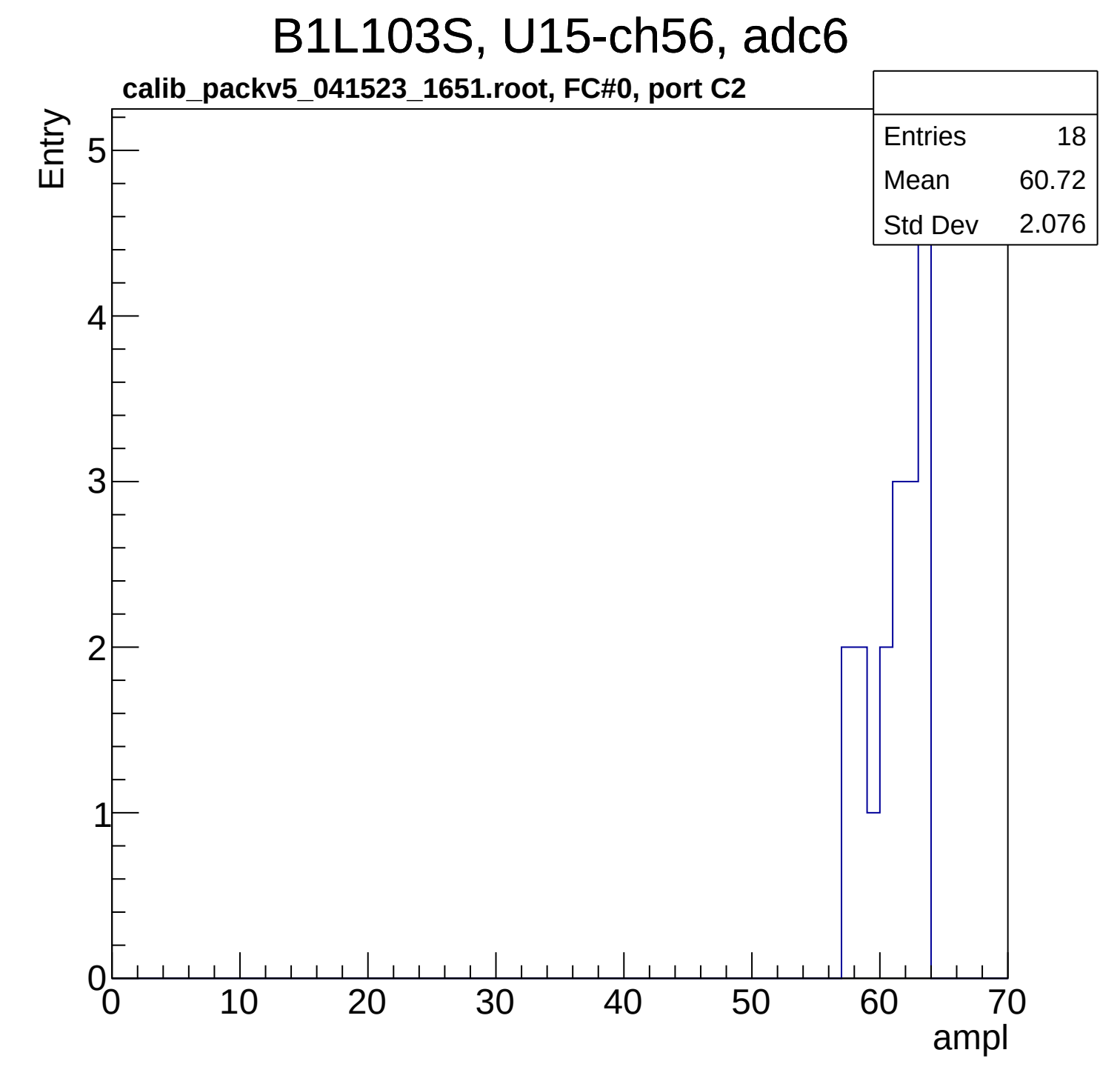
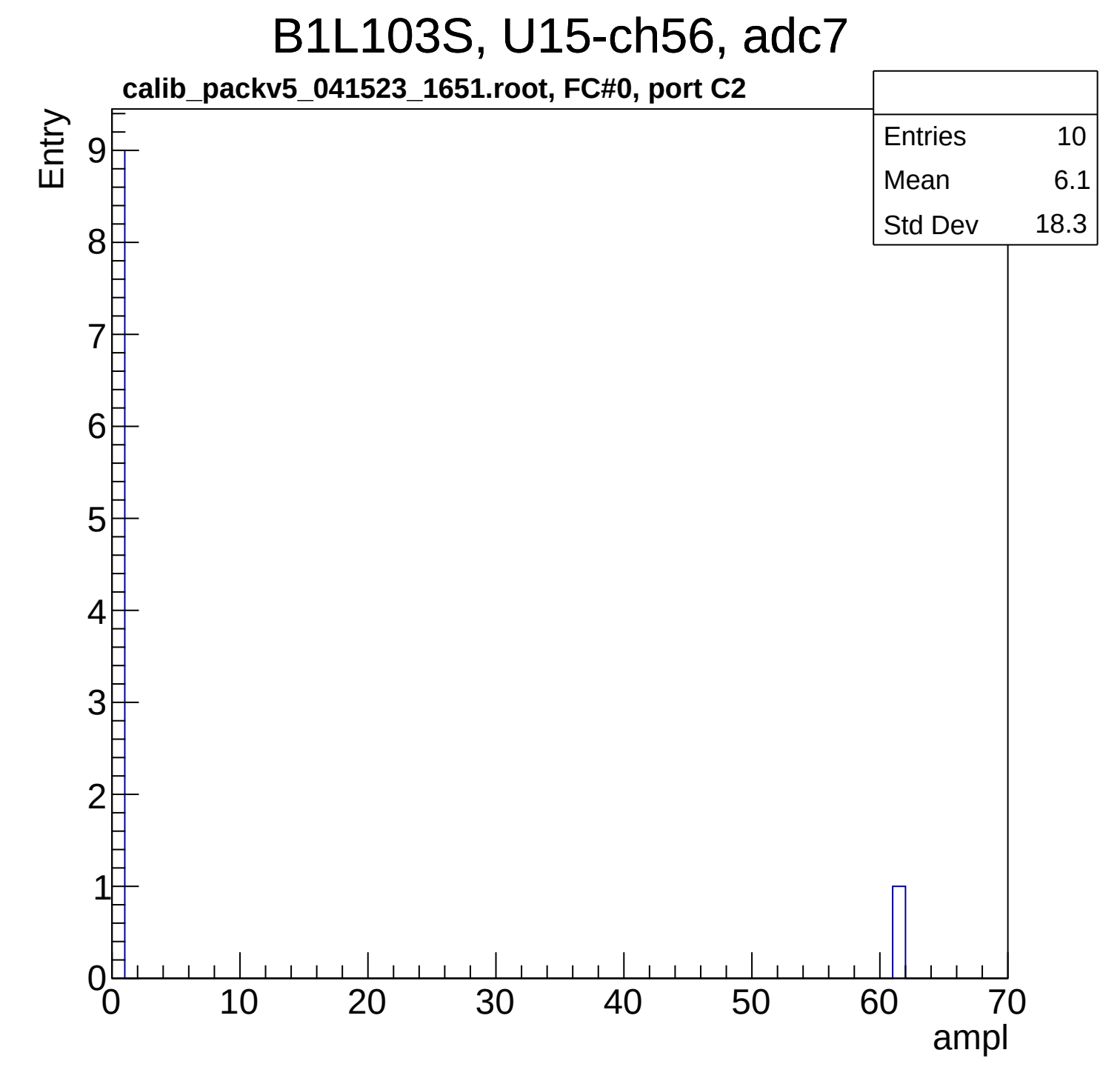

B1L103S, U15-ch56, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 60.72
Std Dev 2.076
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch56, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 6.1
Std Dev 18.3
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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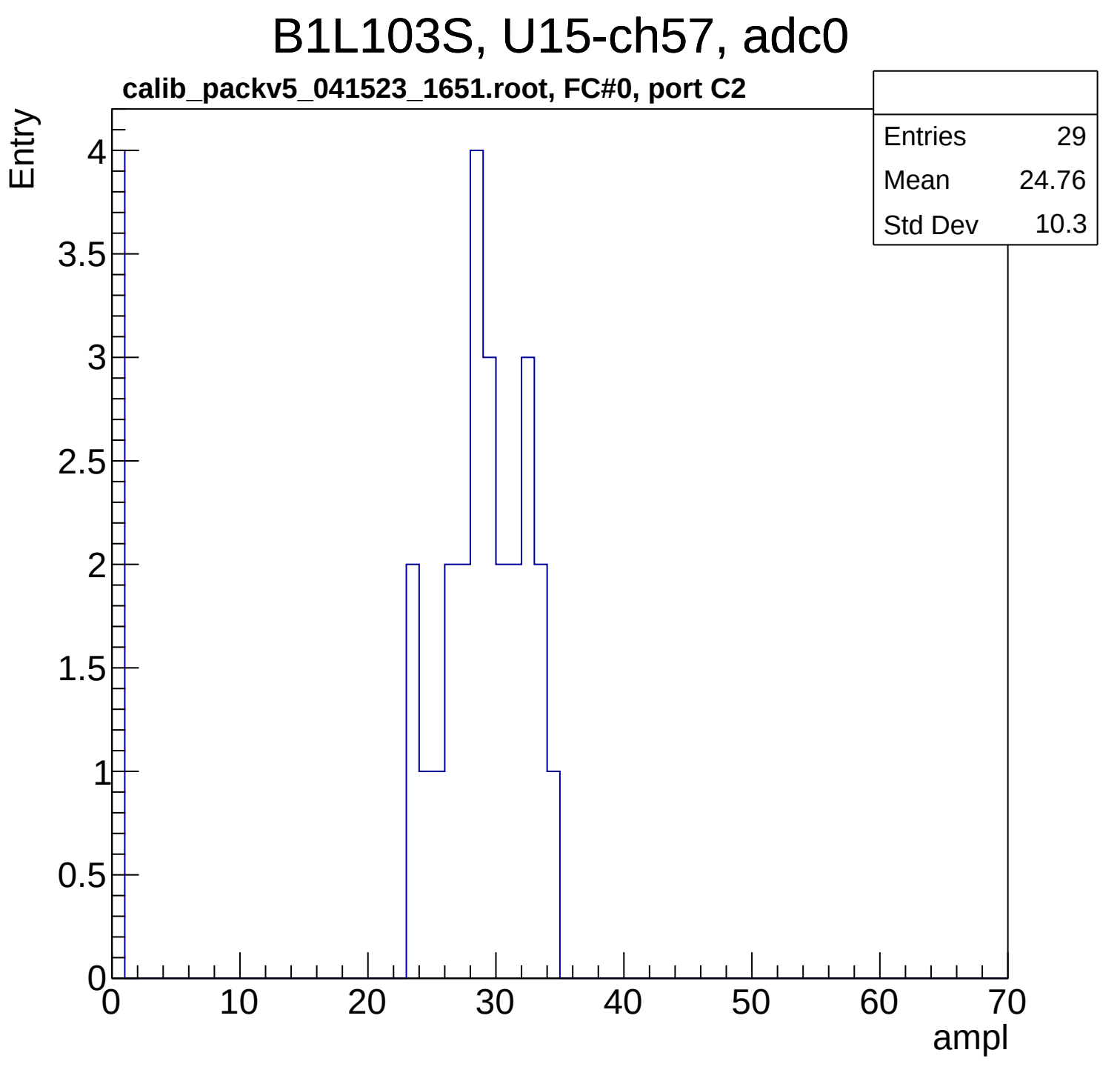
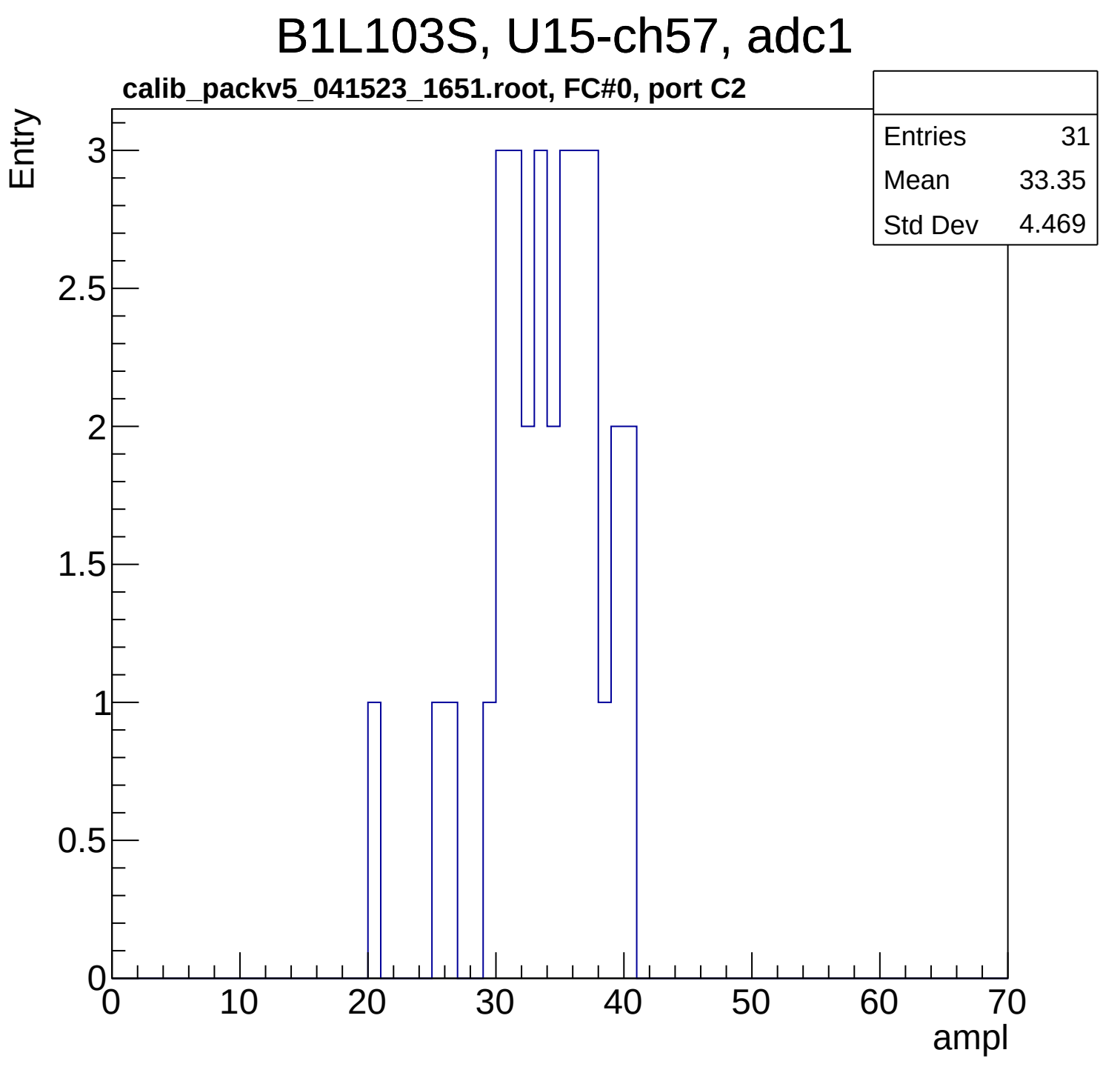
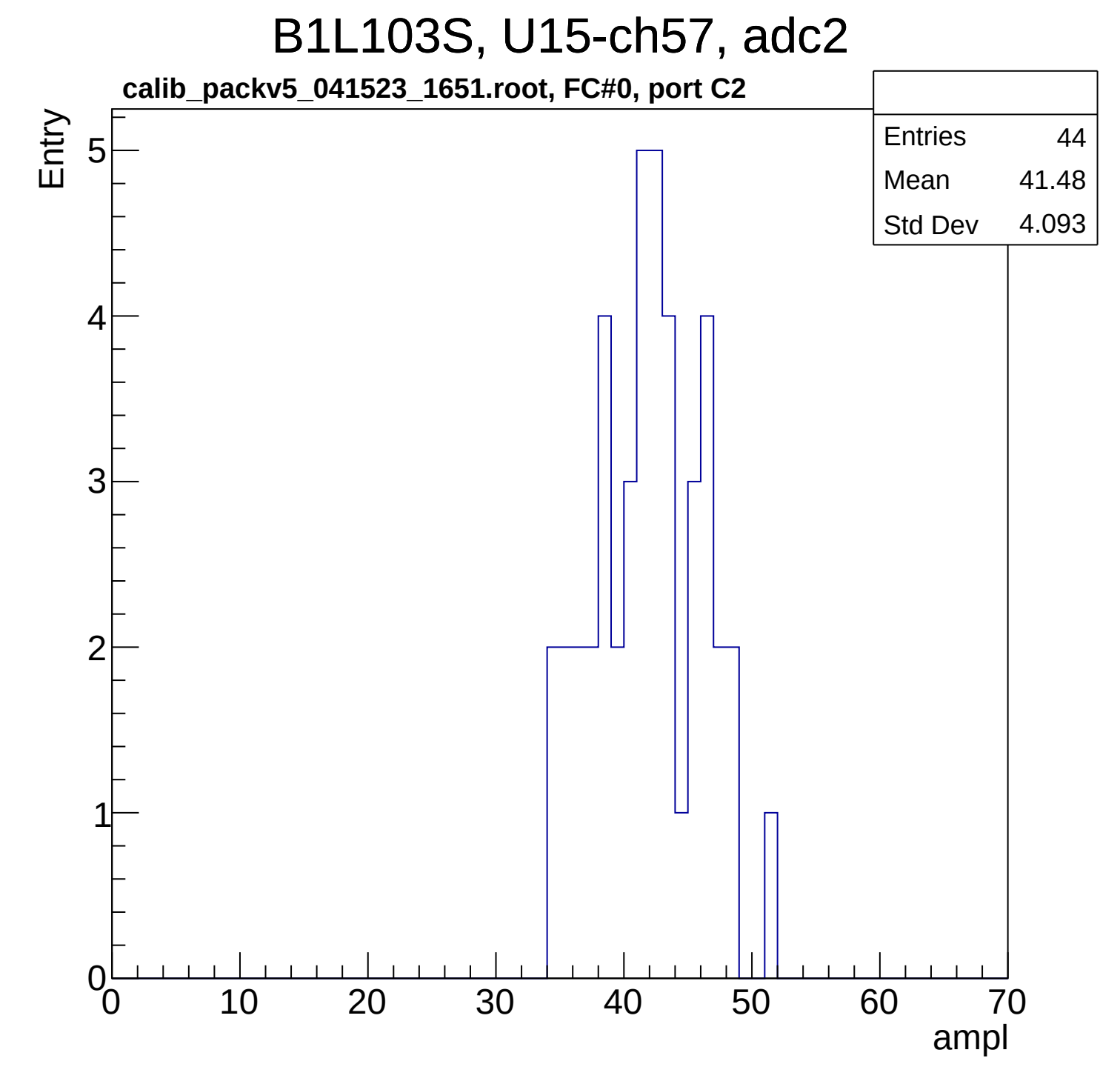
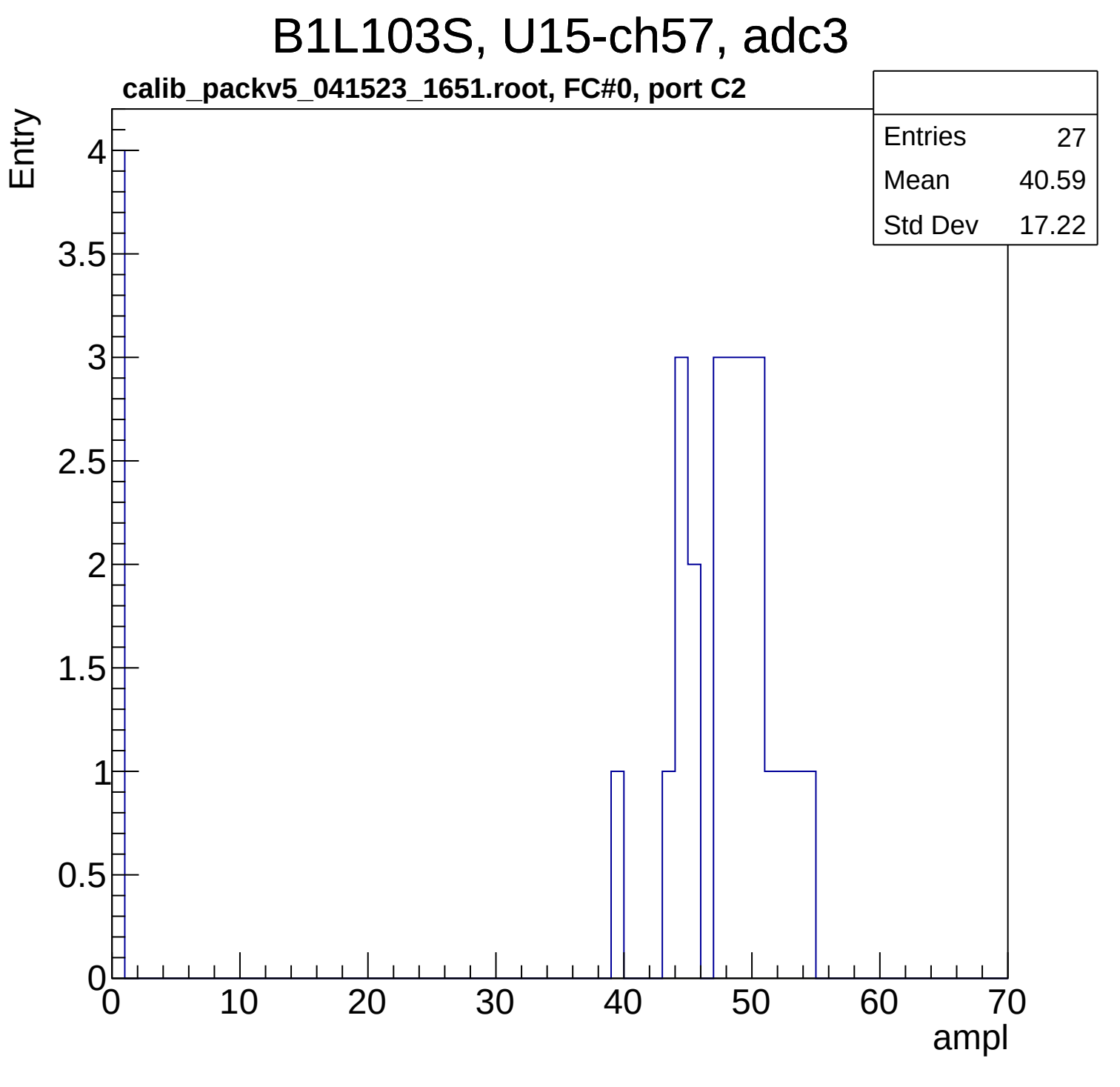
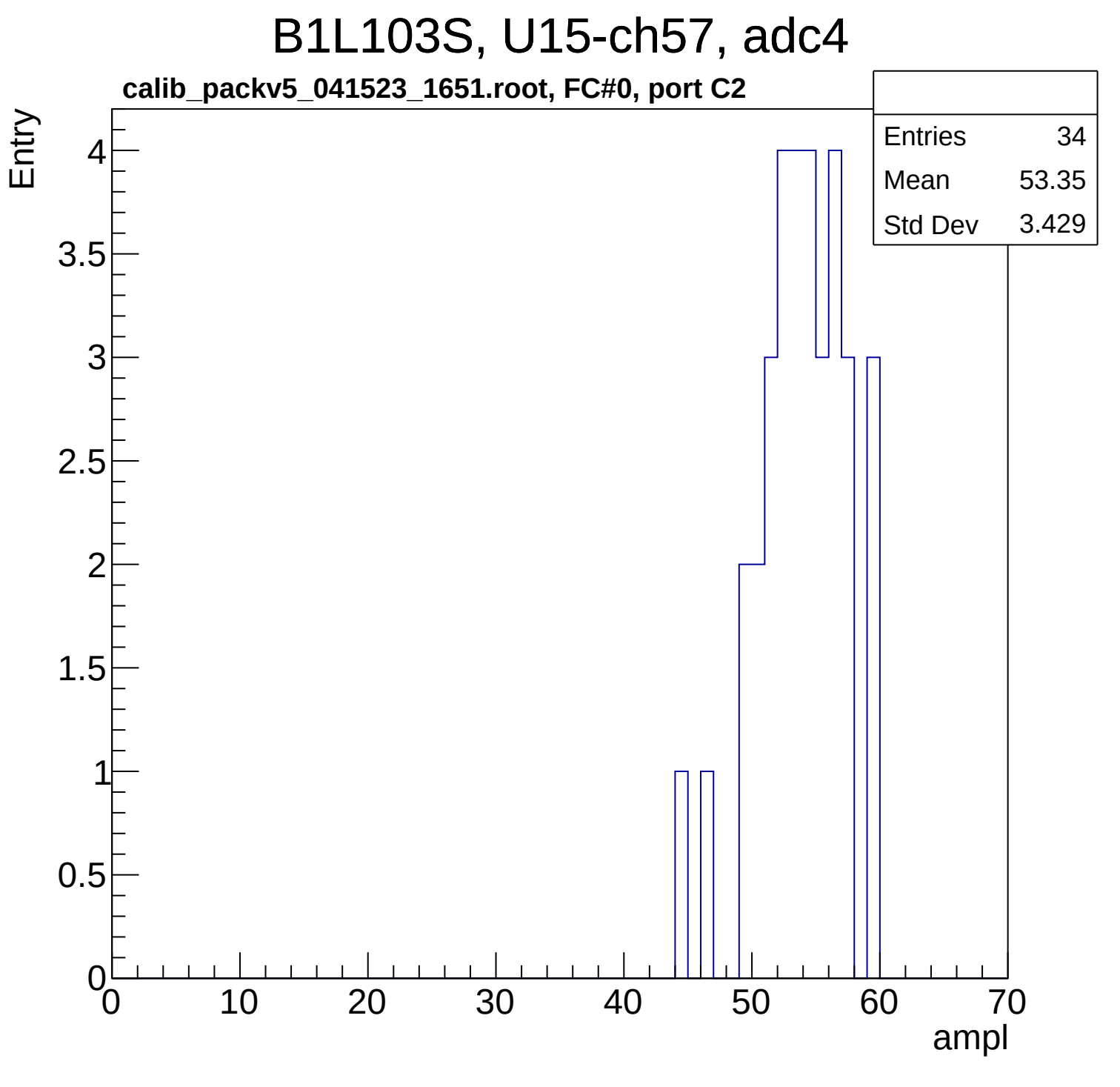
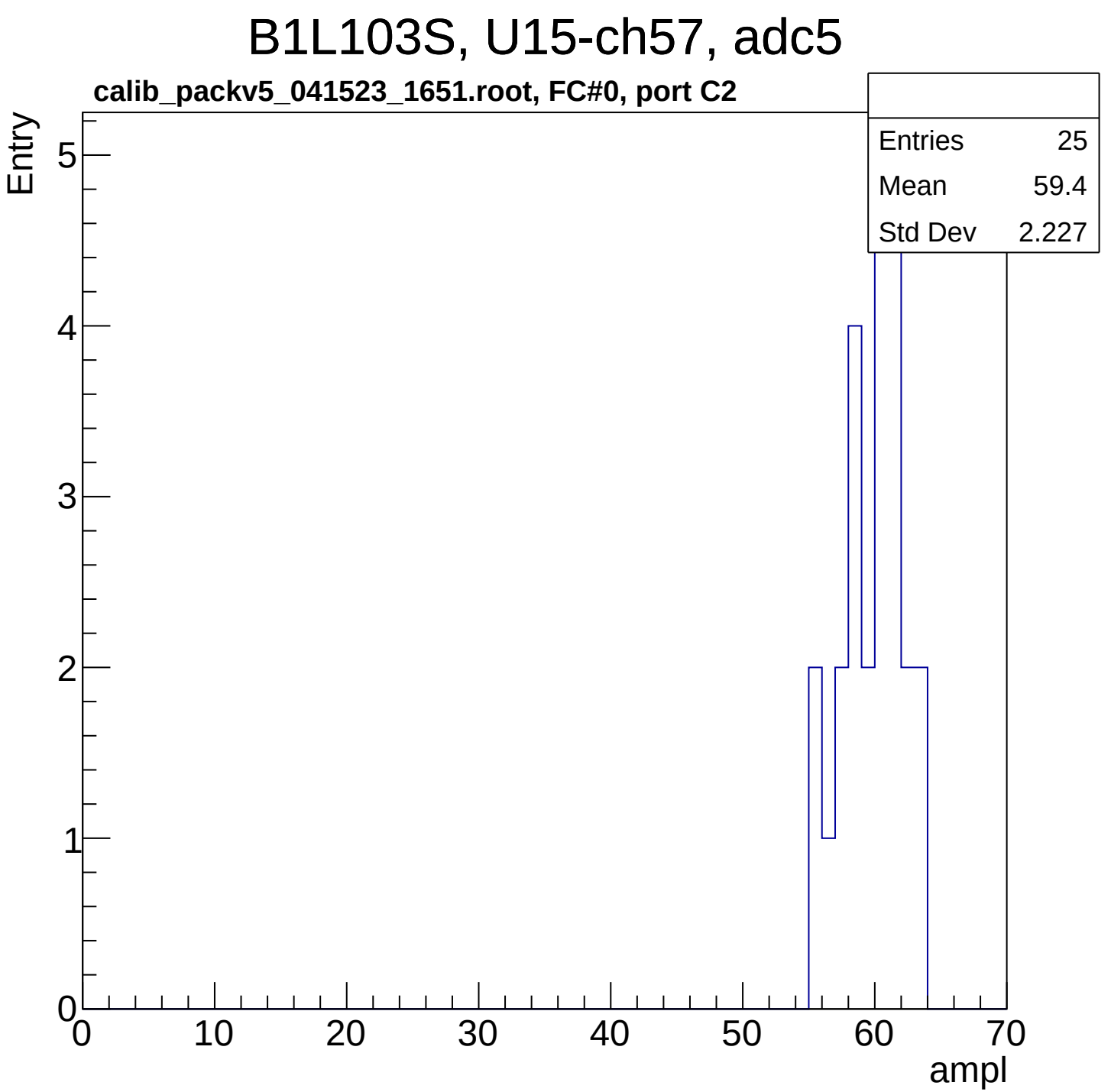

B1L103S, U15-ch57, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 24.76
Std Dev 10.3
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

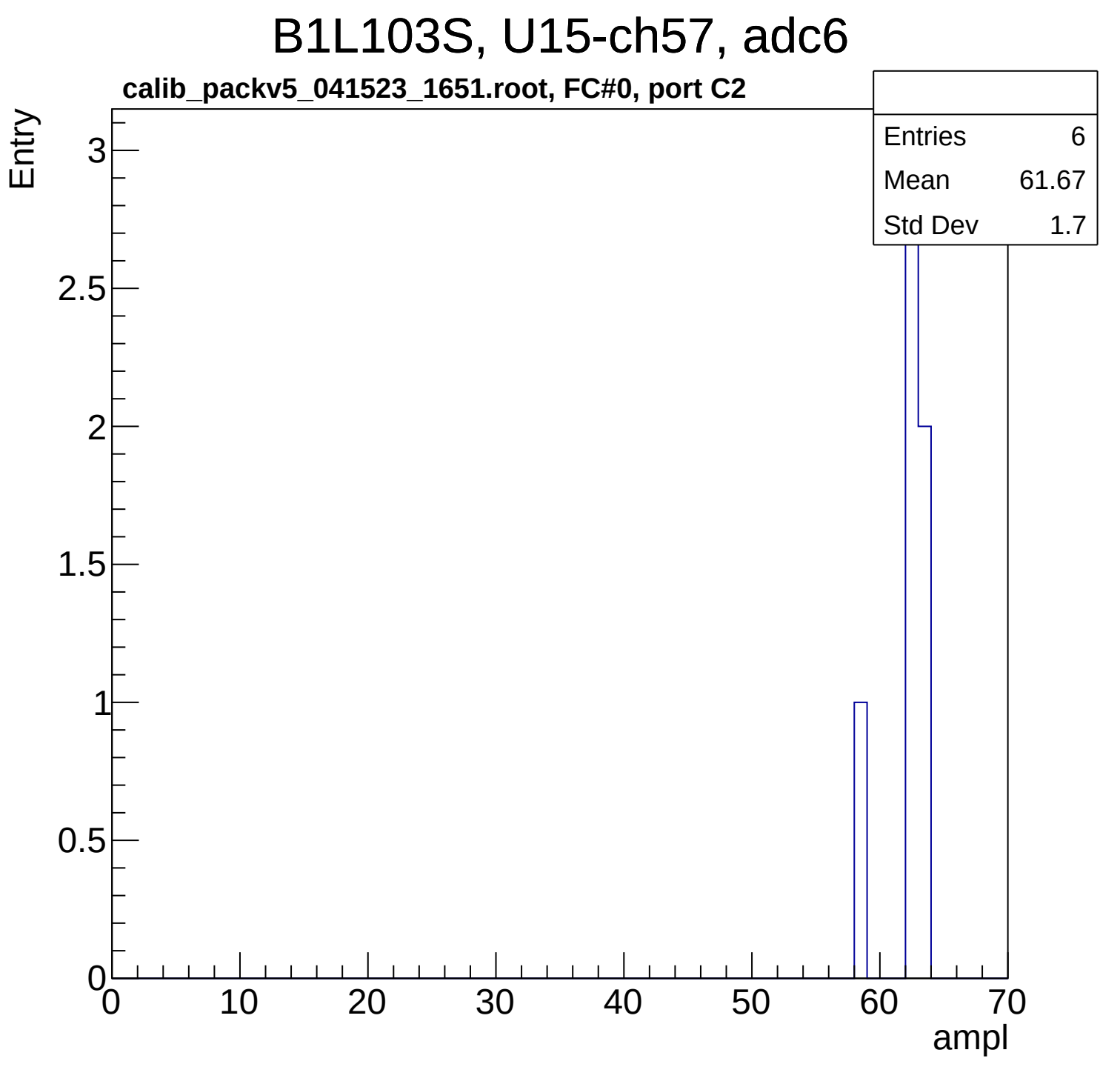

B1L103S, U15-ch57, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 33.35
Std Dev 4.469
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch57, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 41.48
Std Dev 4.093
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch57, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 40.59
Std Dev 17.22
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch57, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 53.35
Std Dev 3.429
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch57, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 59.4
Std Dev 2.227
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch57, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.67
Std Dev 1.7
Entry
ampl
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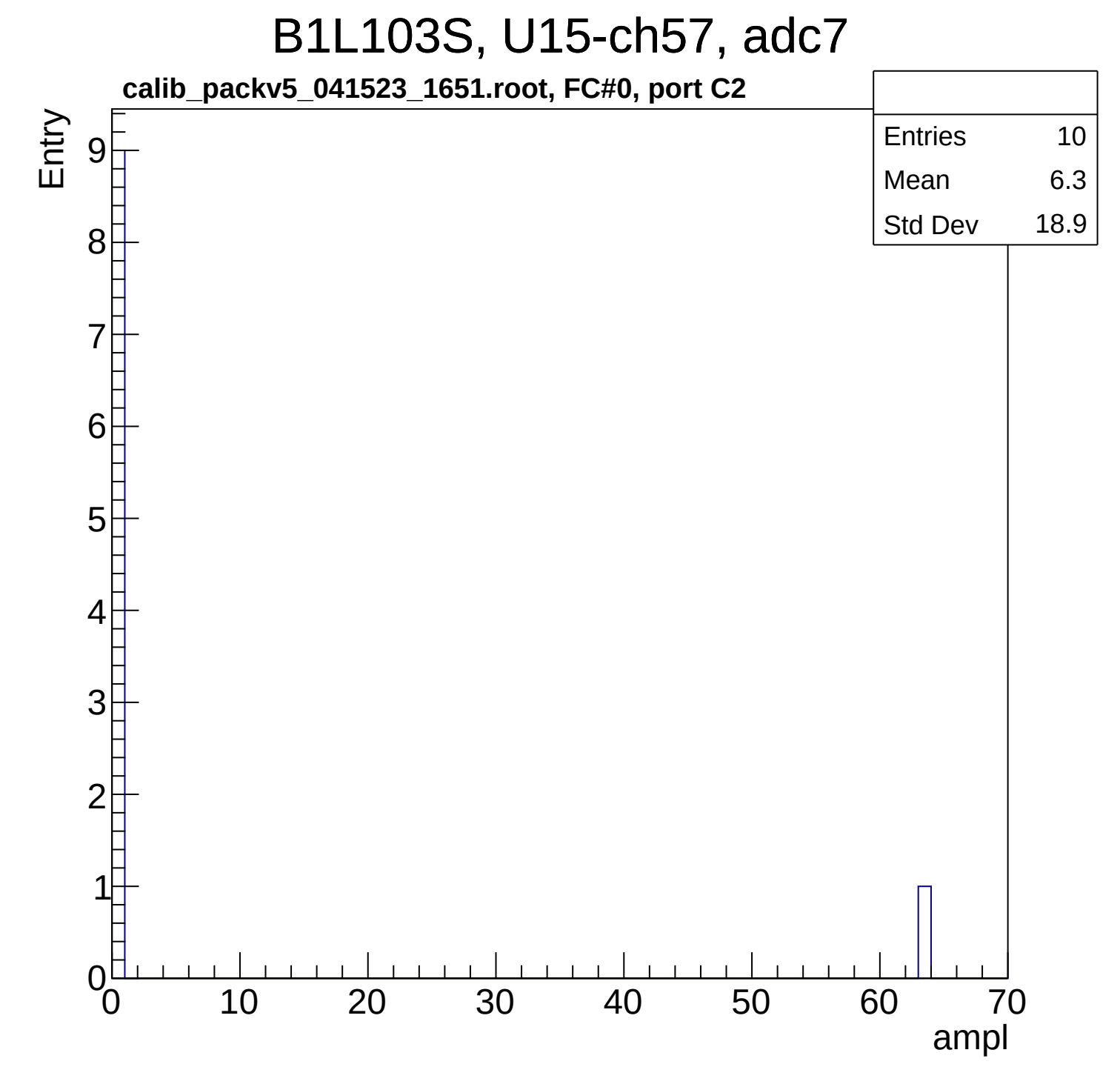
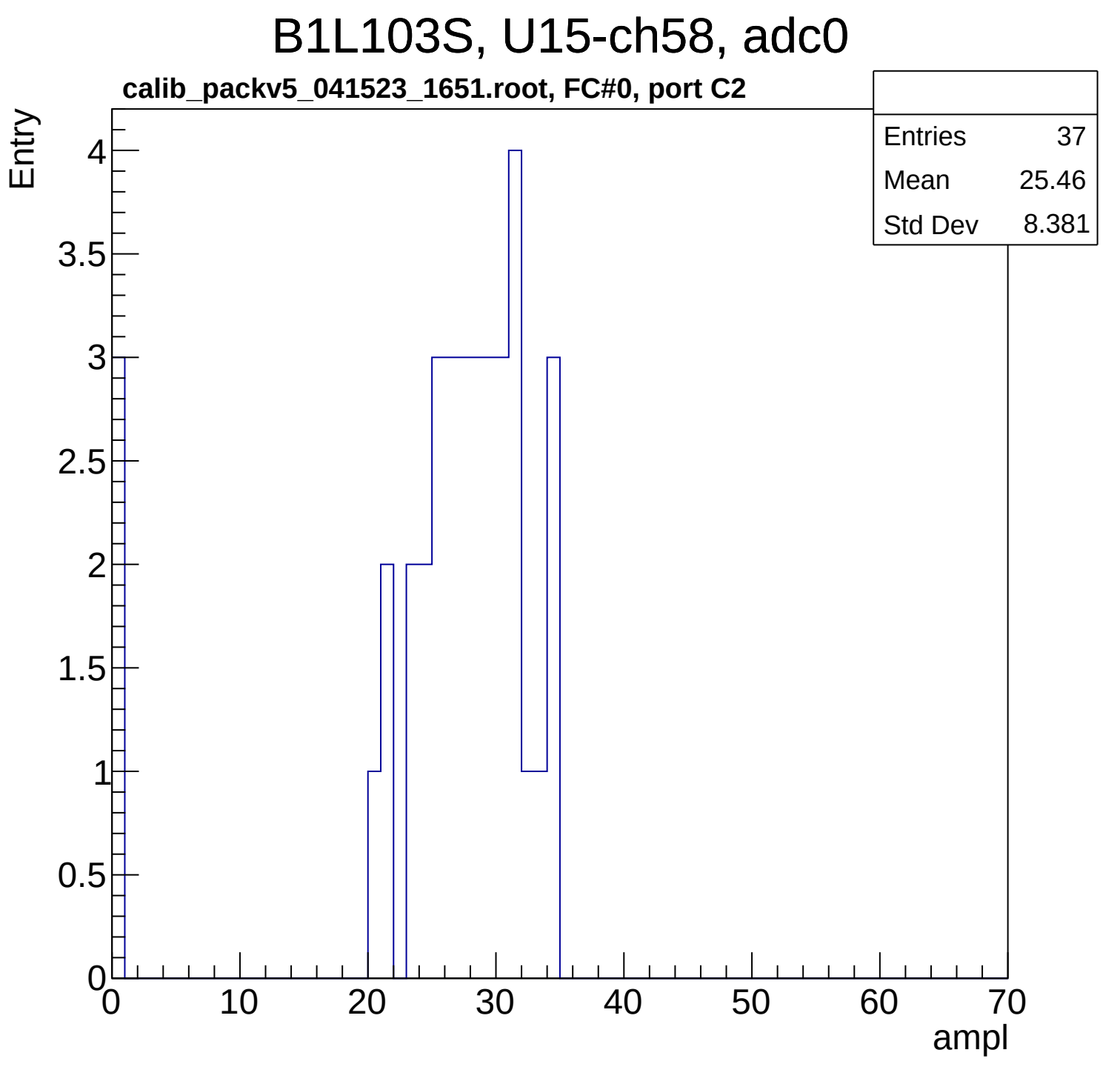
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch57, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 6.3
Std Dev 18.9
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U15-ch58, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 25.46
Std Dev 8.381
Entry
ampl
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0.5
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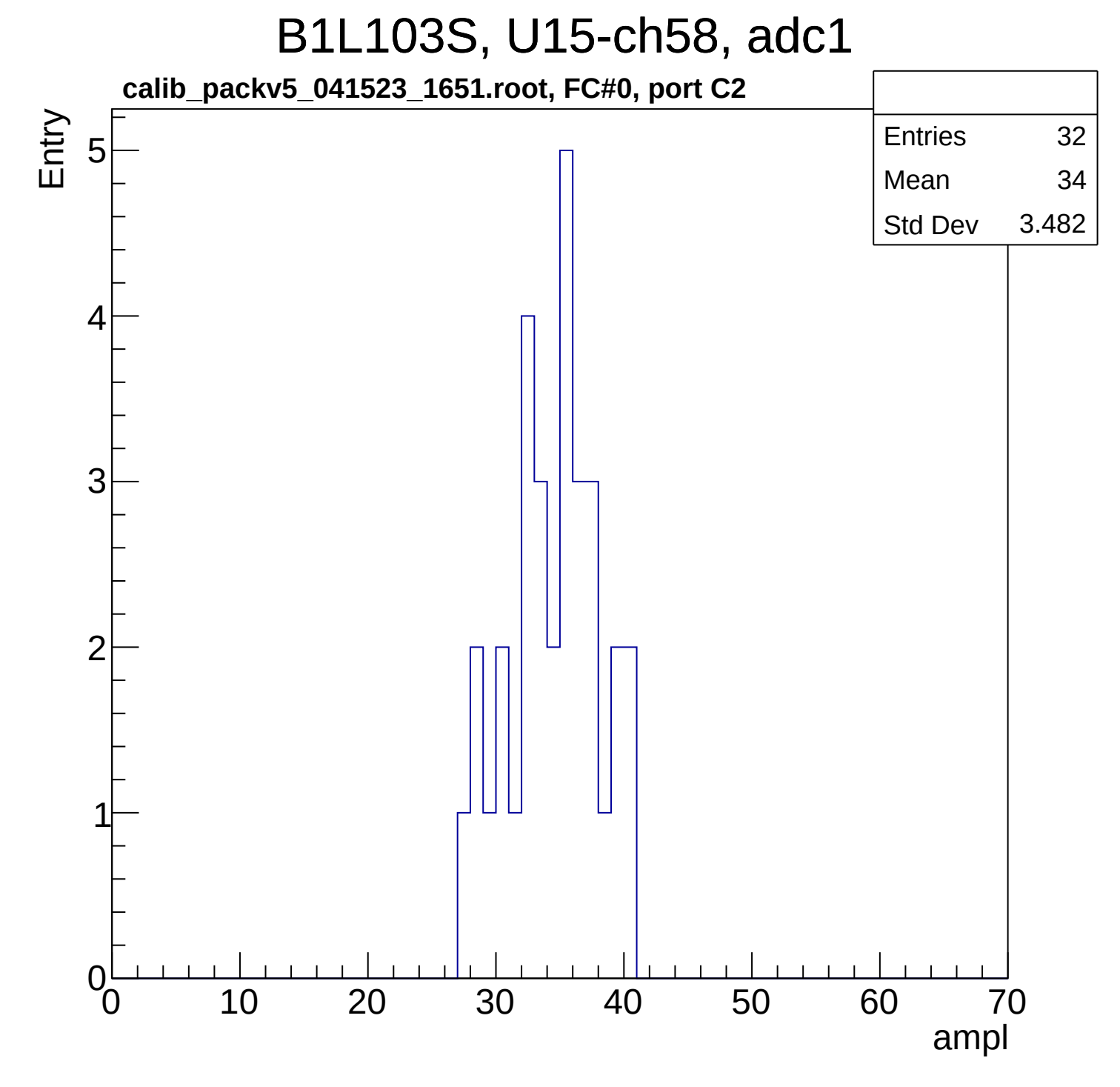
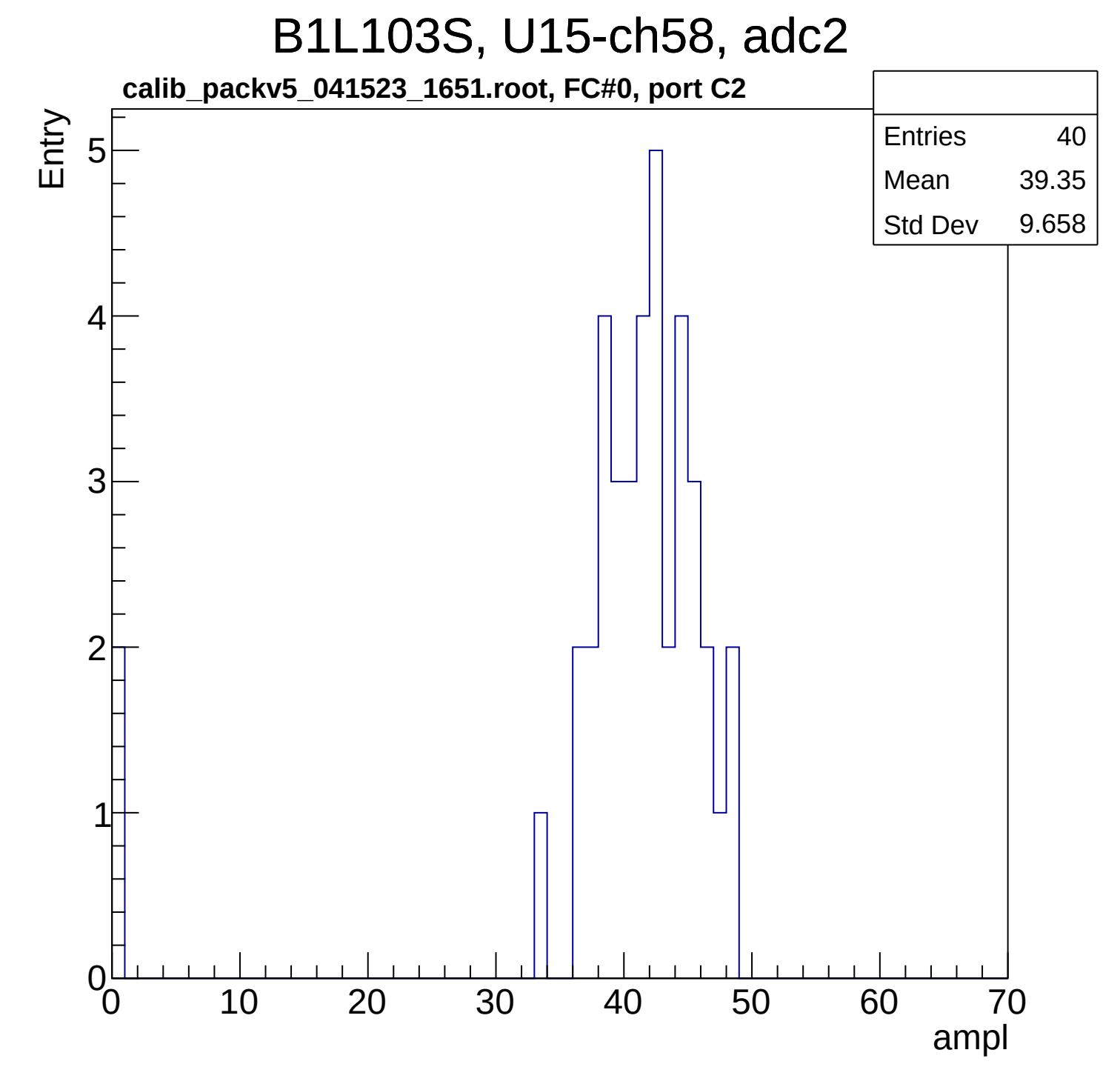
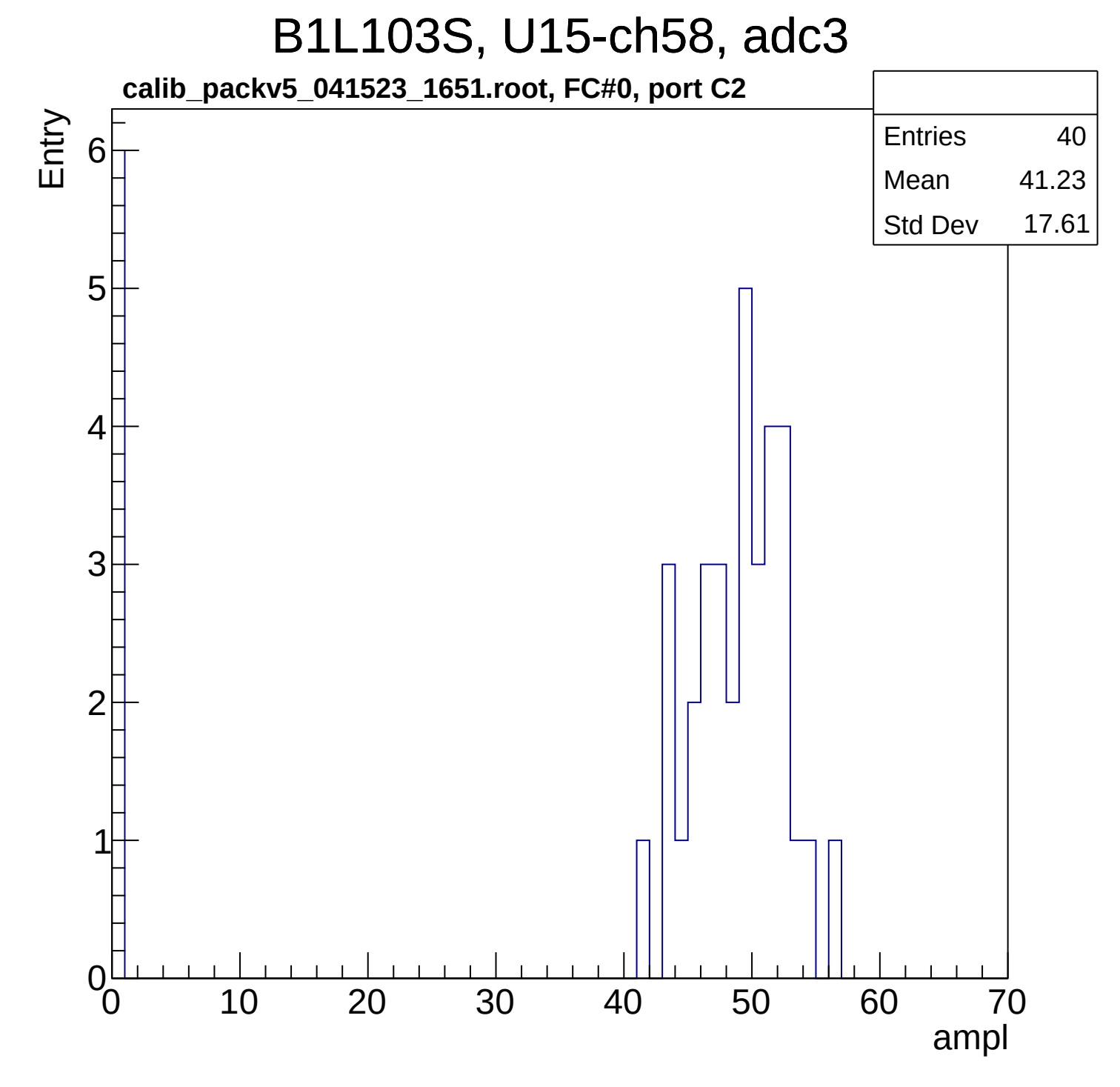
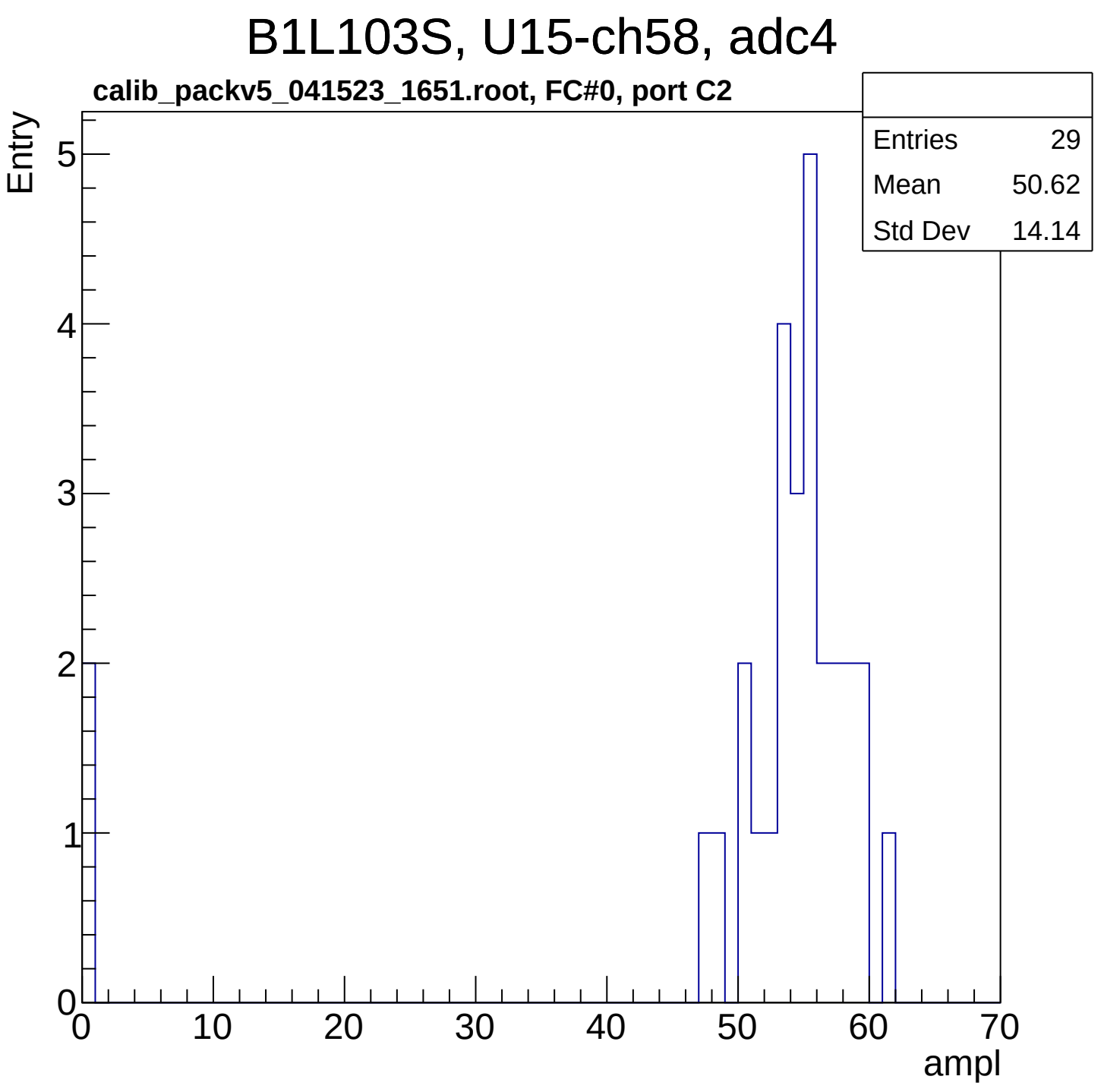
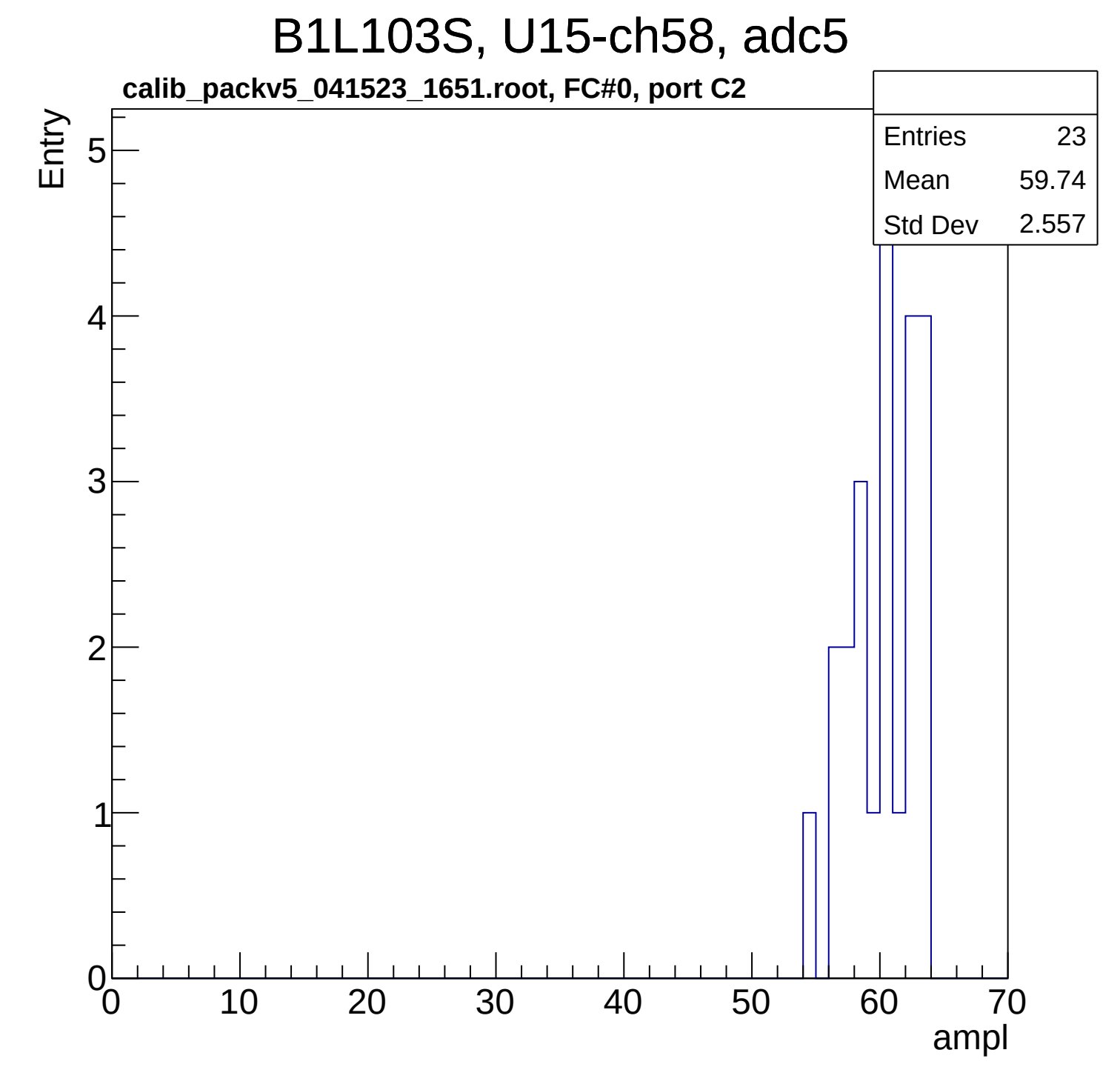
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch58, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 34
Std Dev 3.482
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch58, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 39.35
Std Dev 9.658
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch58, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 41.23
Std Dev 17.61
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U15-ch58, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 50.62
Std Dev 14.14
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch58, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 59.74
Std Dev 2.557
Entry
ampl
0
1
2
3
4
5
0
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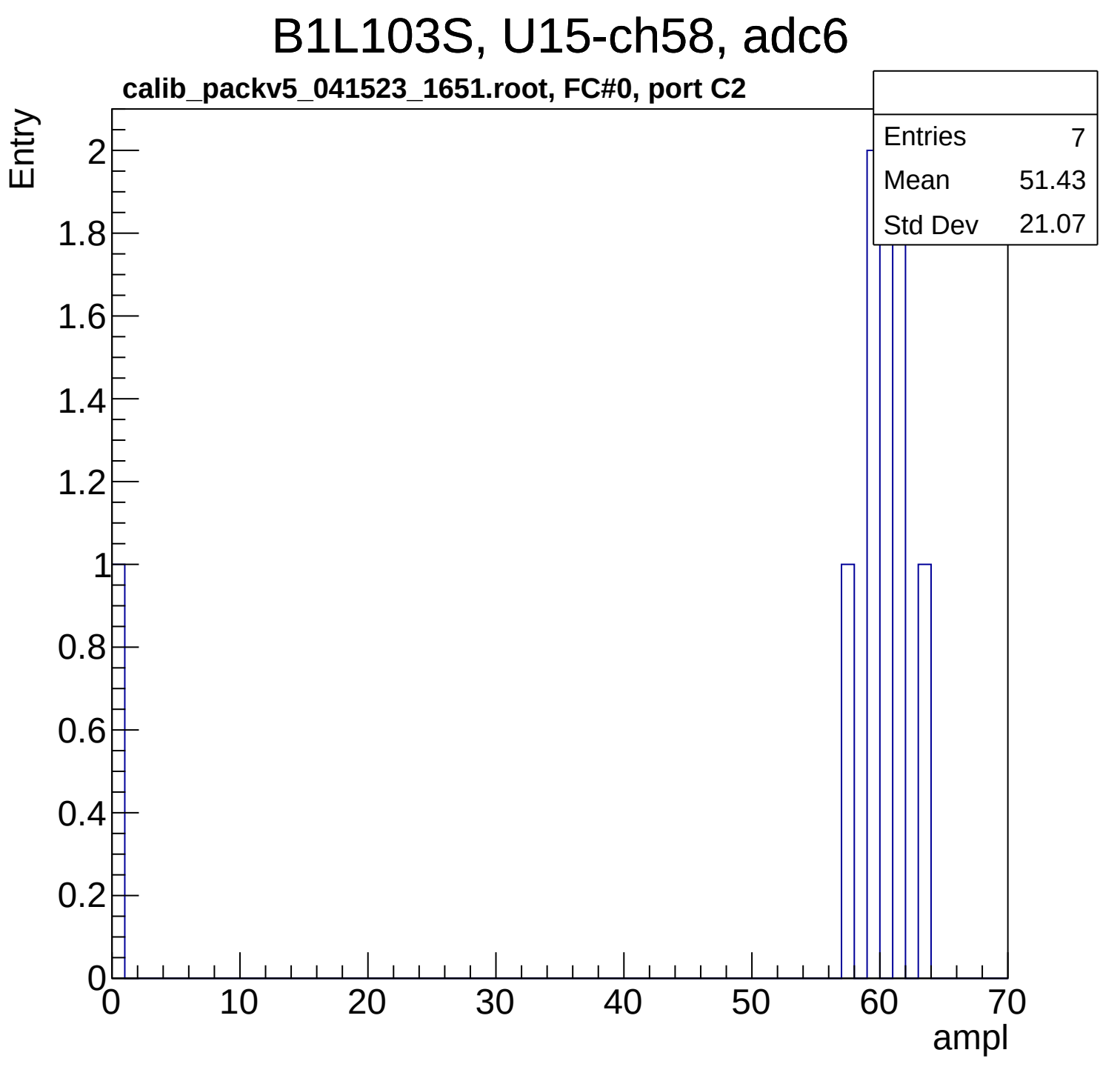
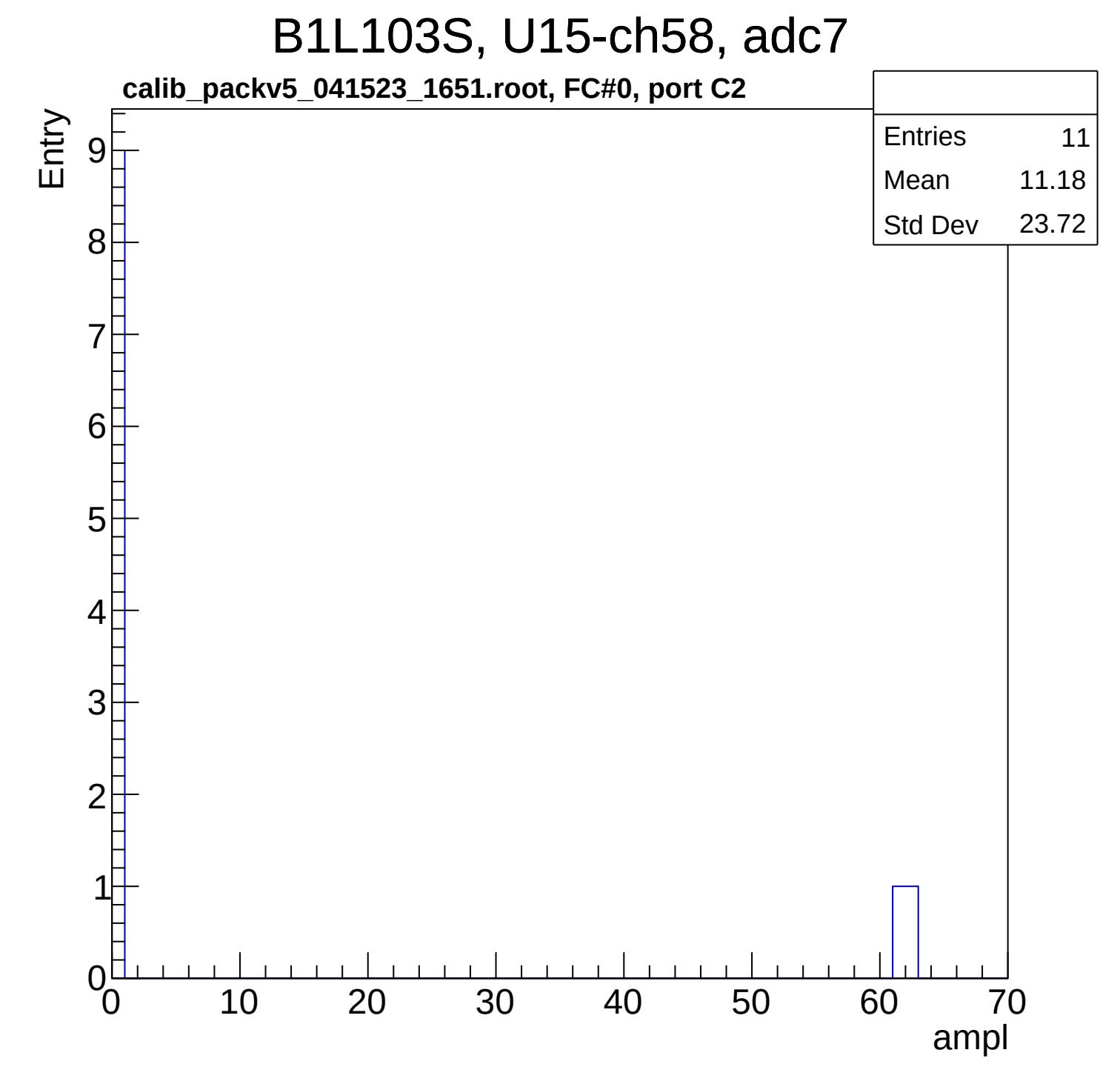
20
30
40
50
60
70


B1L103S, U15-ch58, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 51.43
Std Dev 21.07
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U15-ch58, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 11.18
Std Dev 23.72
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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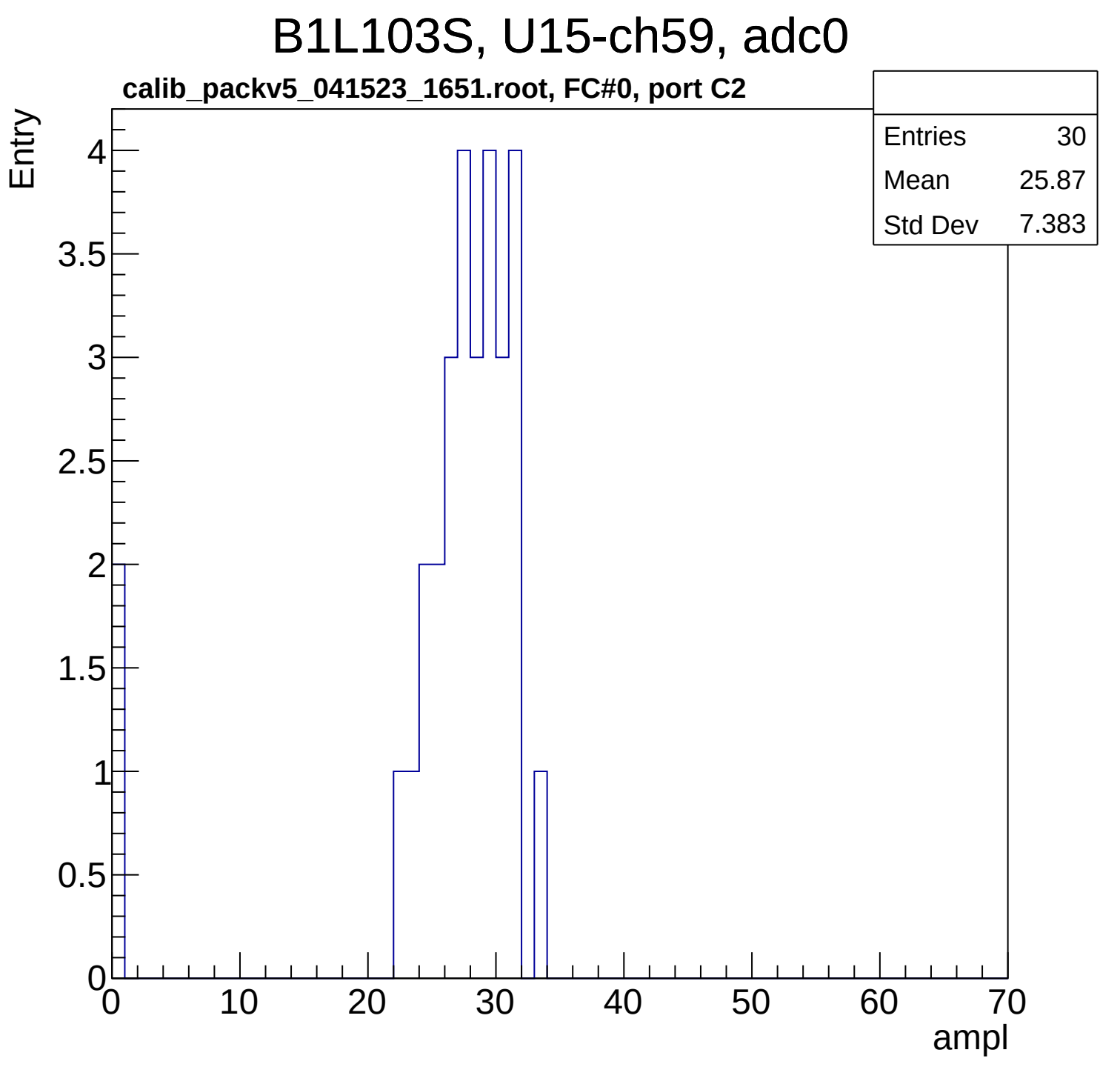
60
70


B1L103S, U15-ch59, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 25.87
Std Dev 7.383
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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20
30
40
50
60
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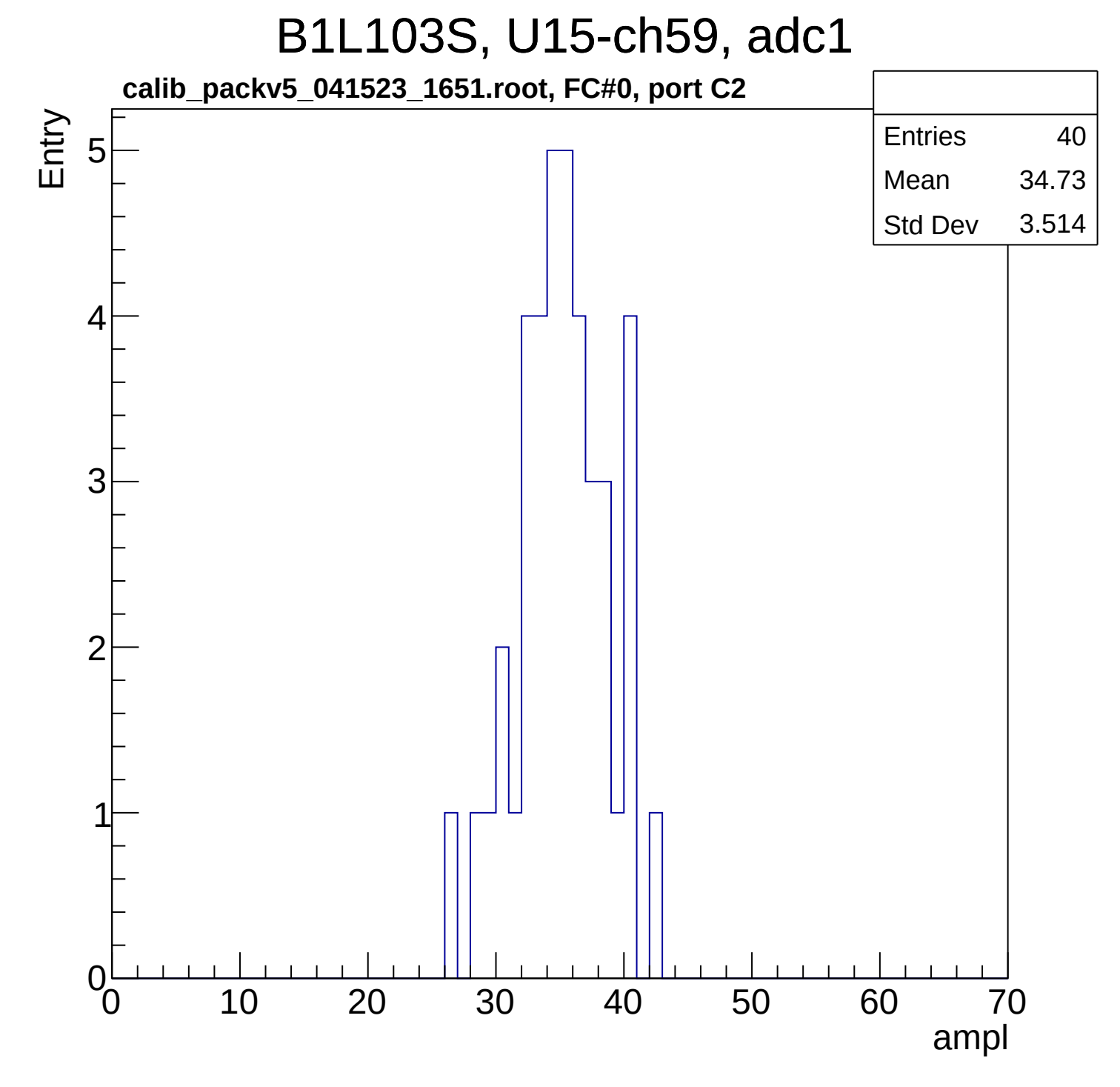
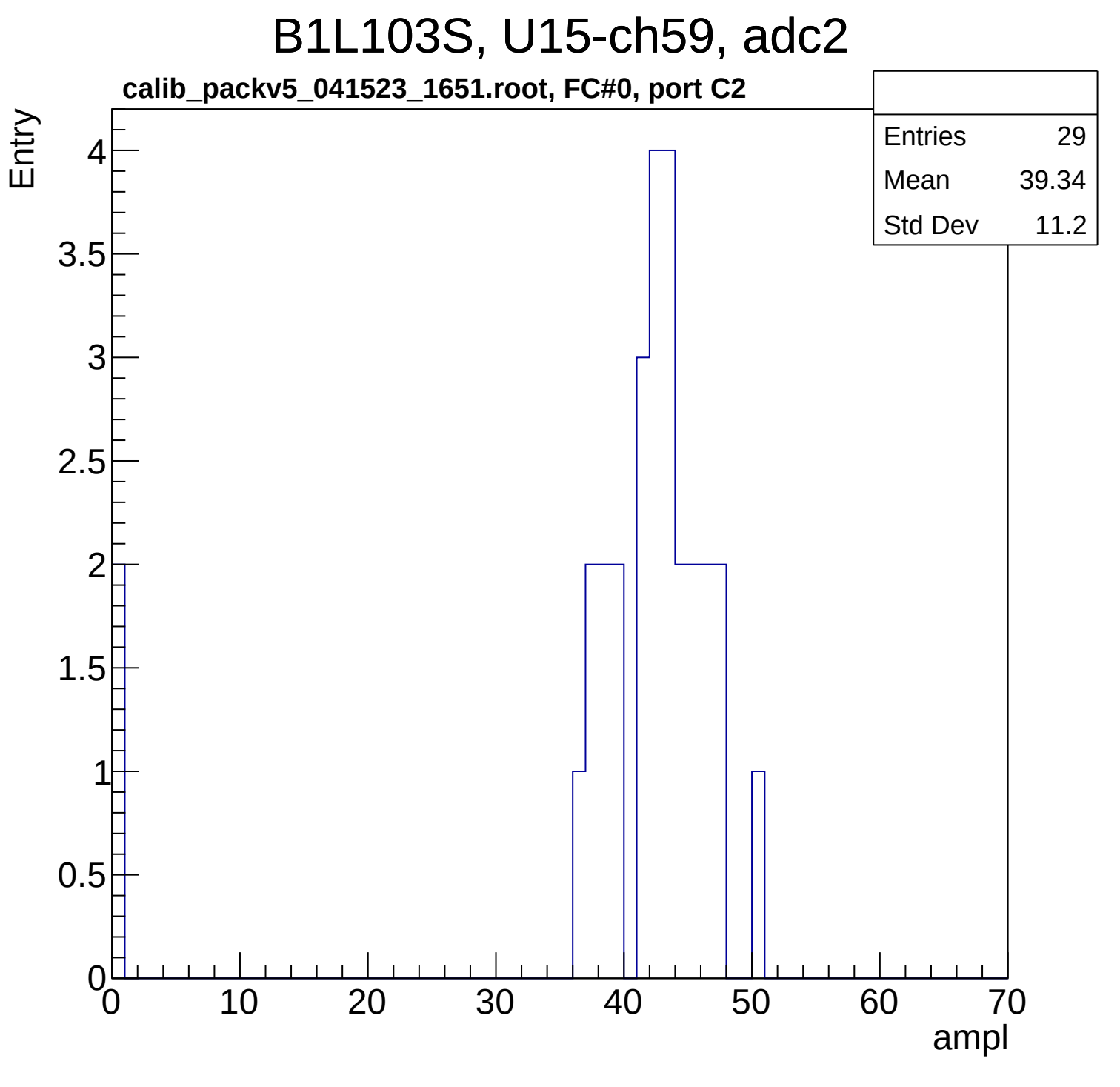

B1L103S, U15-ch59, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 34.73
Std Dev 3.514
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch59, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 39.34
Std Dev 11.2
Entry
ampl
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0.5
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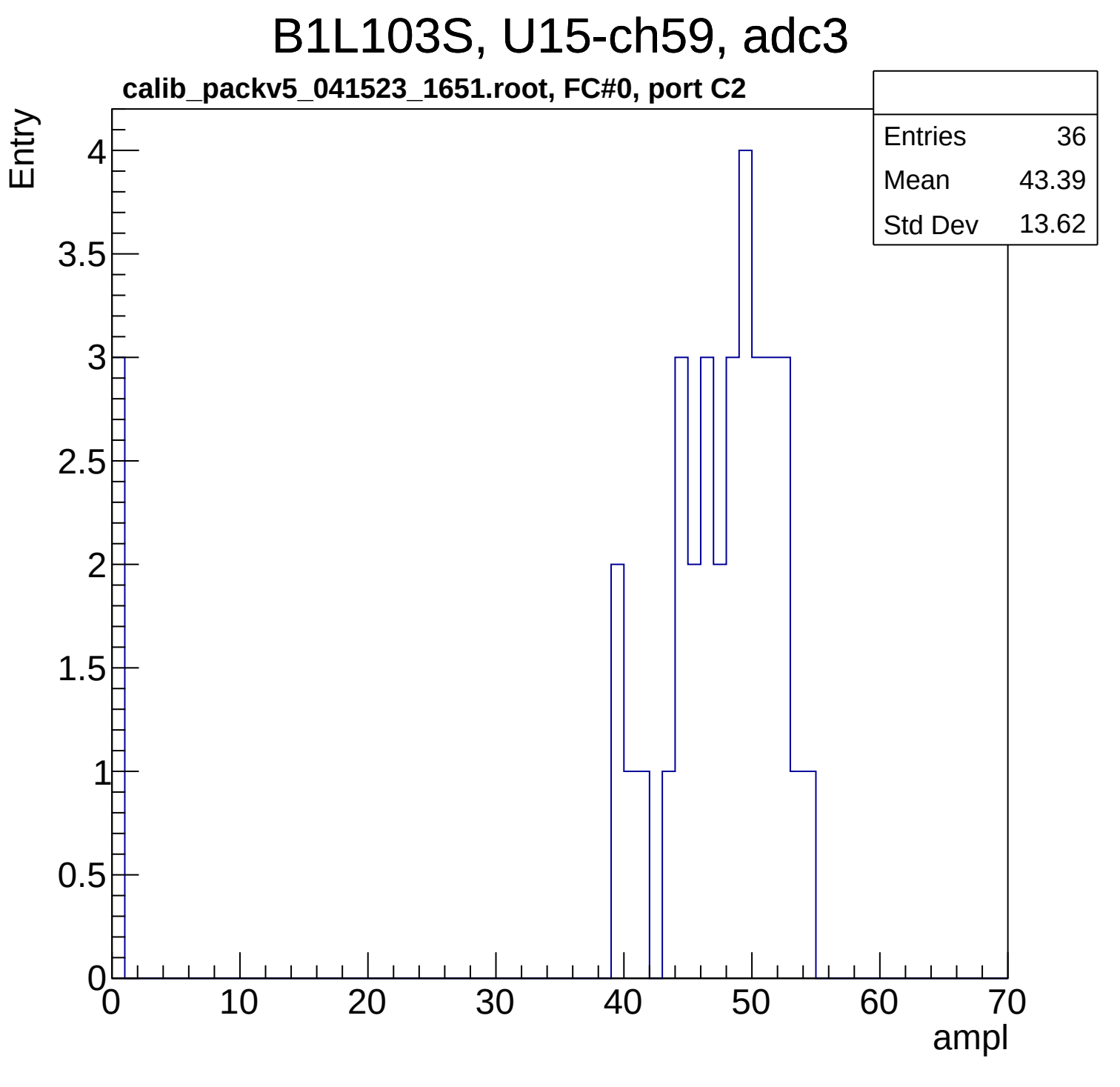
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch59, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 43.39
Std Dev 13.62
Entry
ampl
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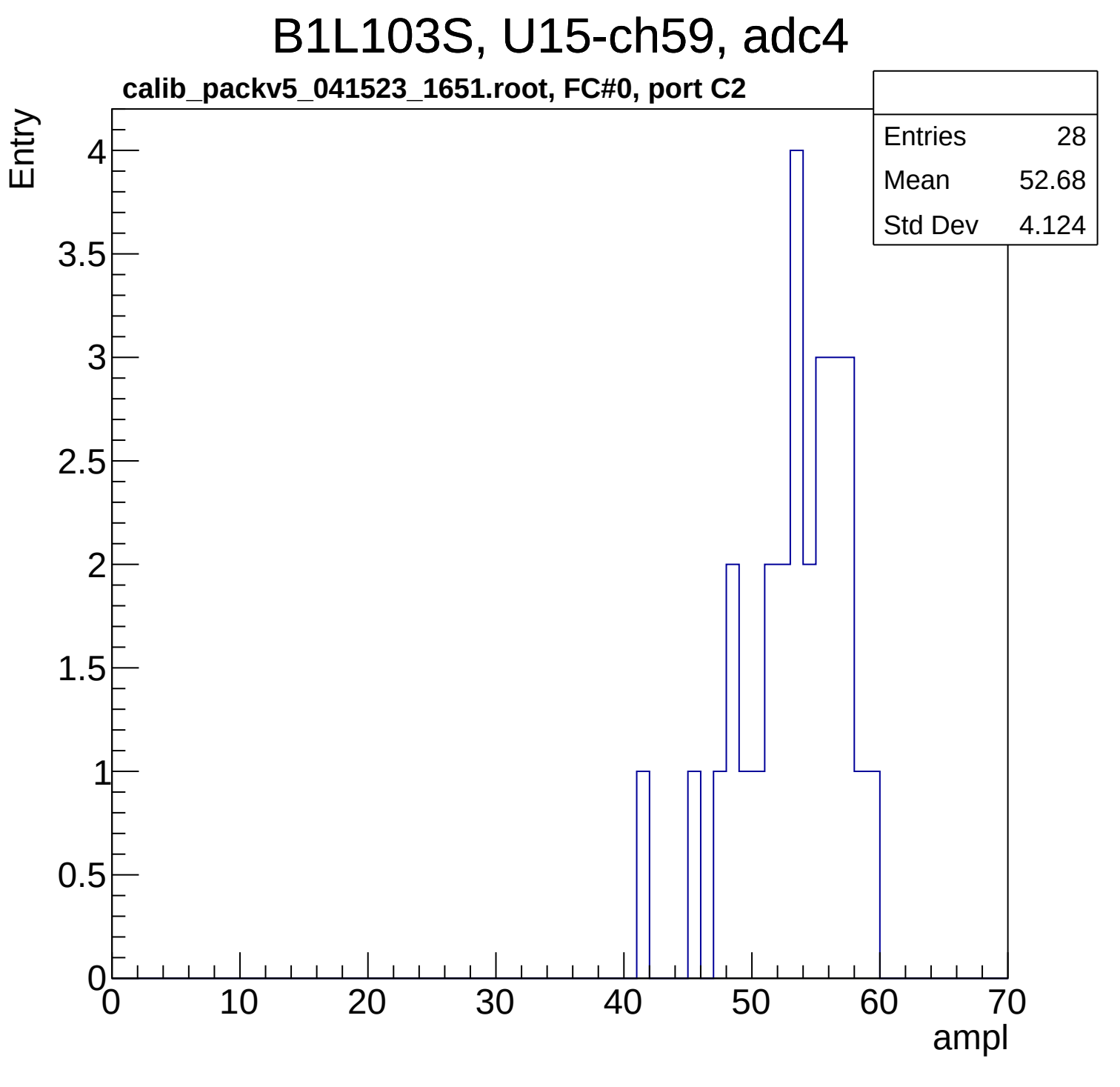
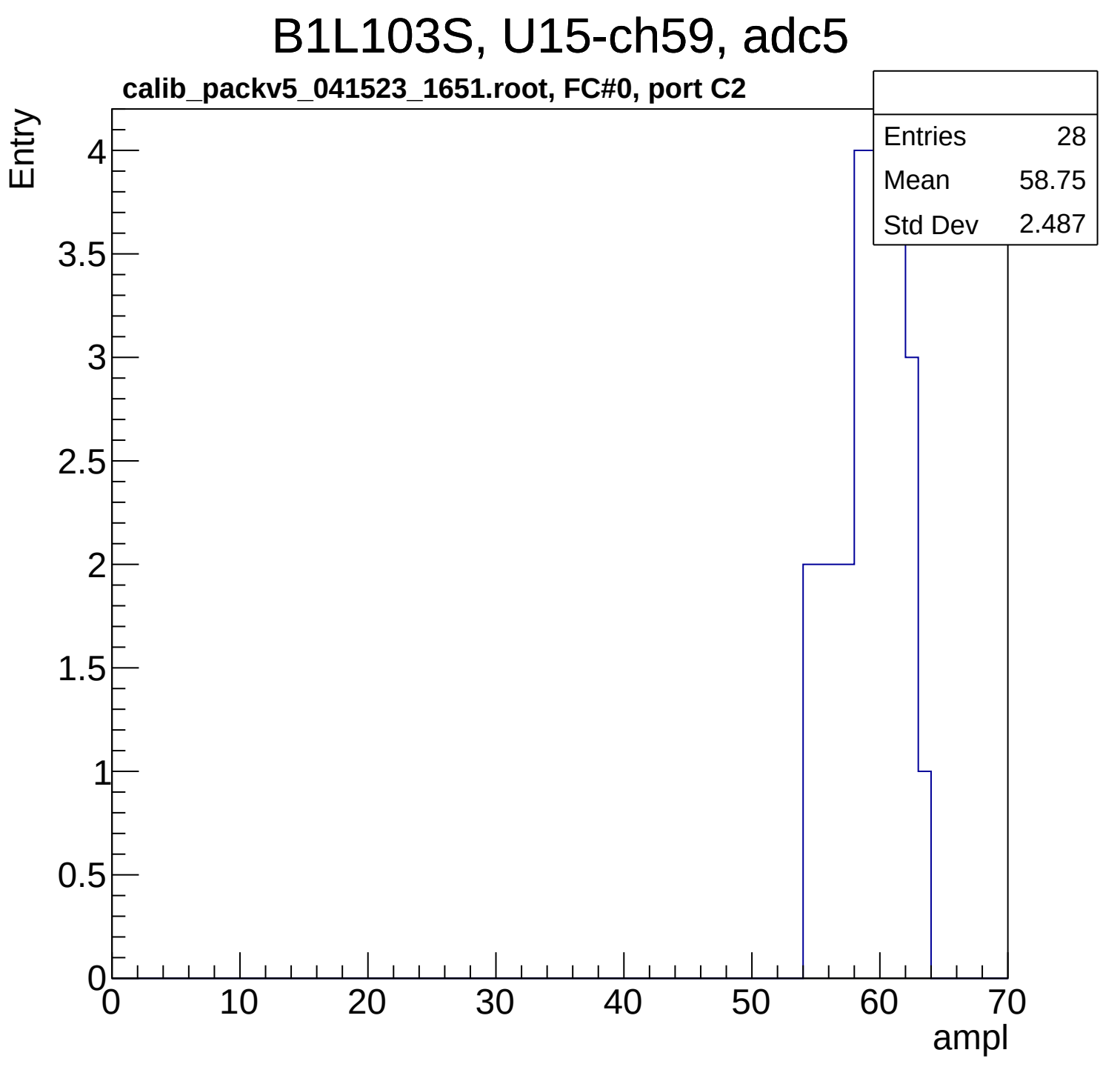
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch59, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 52.68
Std Dev 4.124
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch59, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 58.75
Std Dev 2.487
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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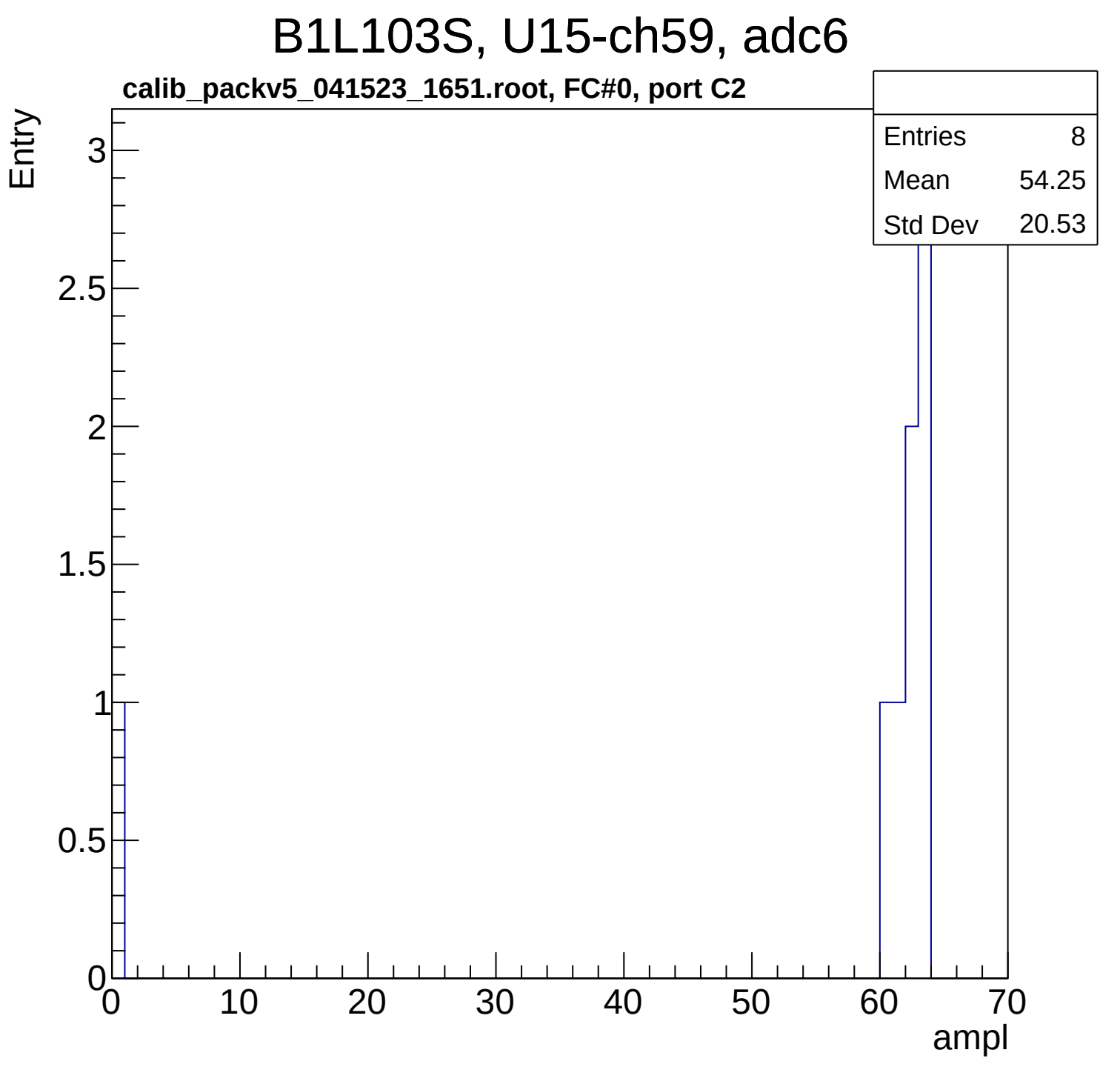
40
50
60
70


B1L103S, U15-ch59, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 54.25
Std Dev 20.53
Entry
ampl
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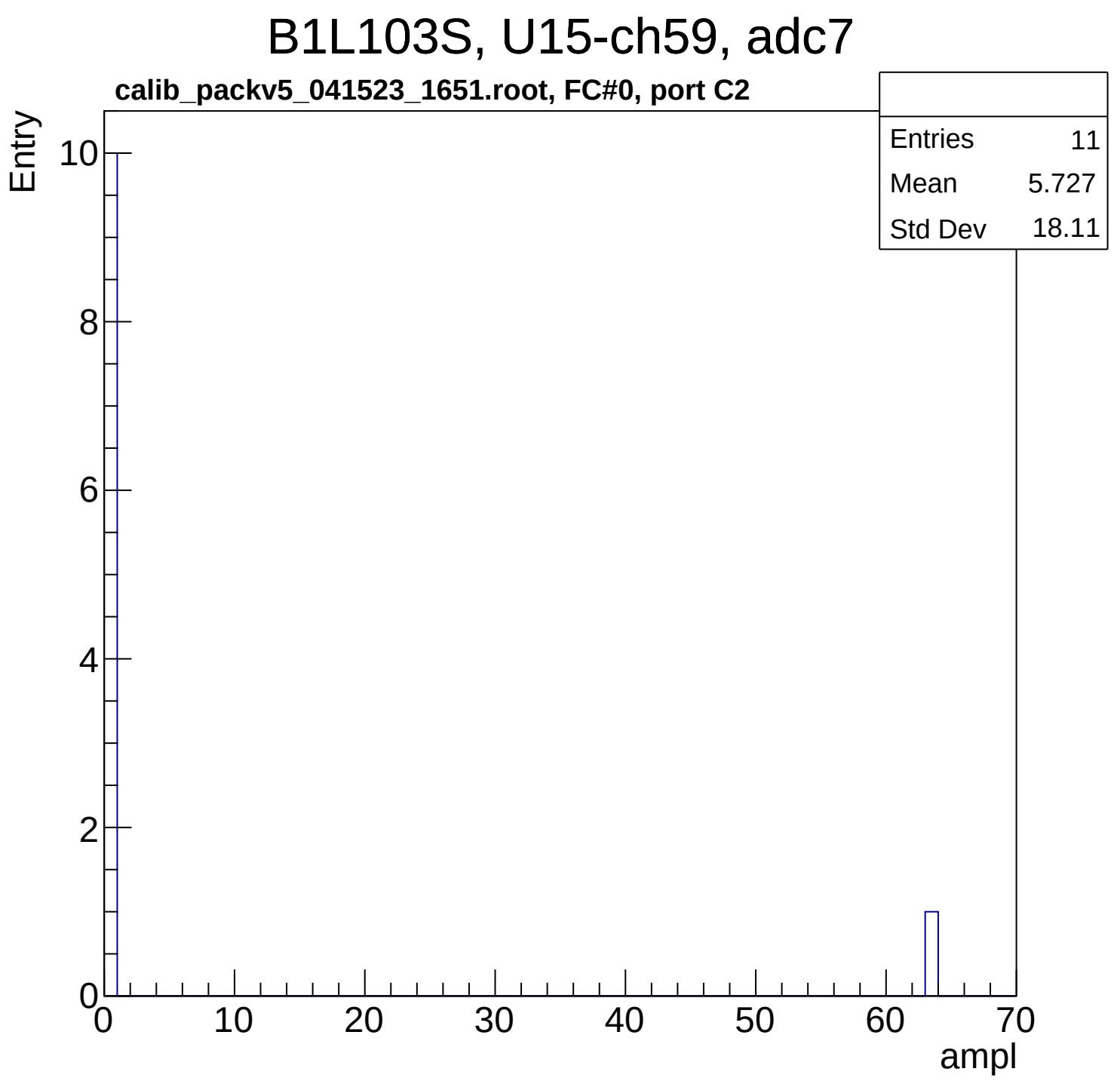
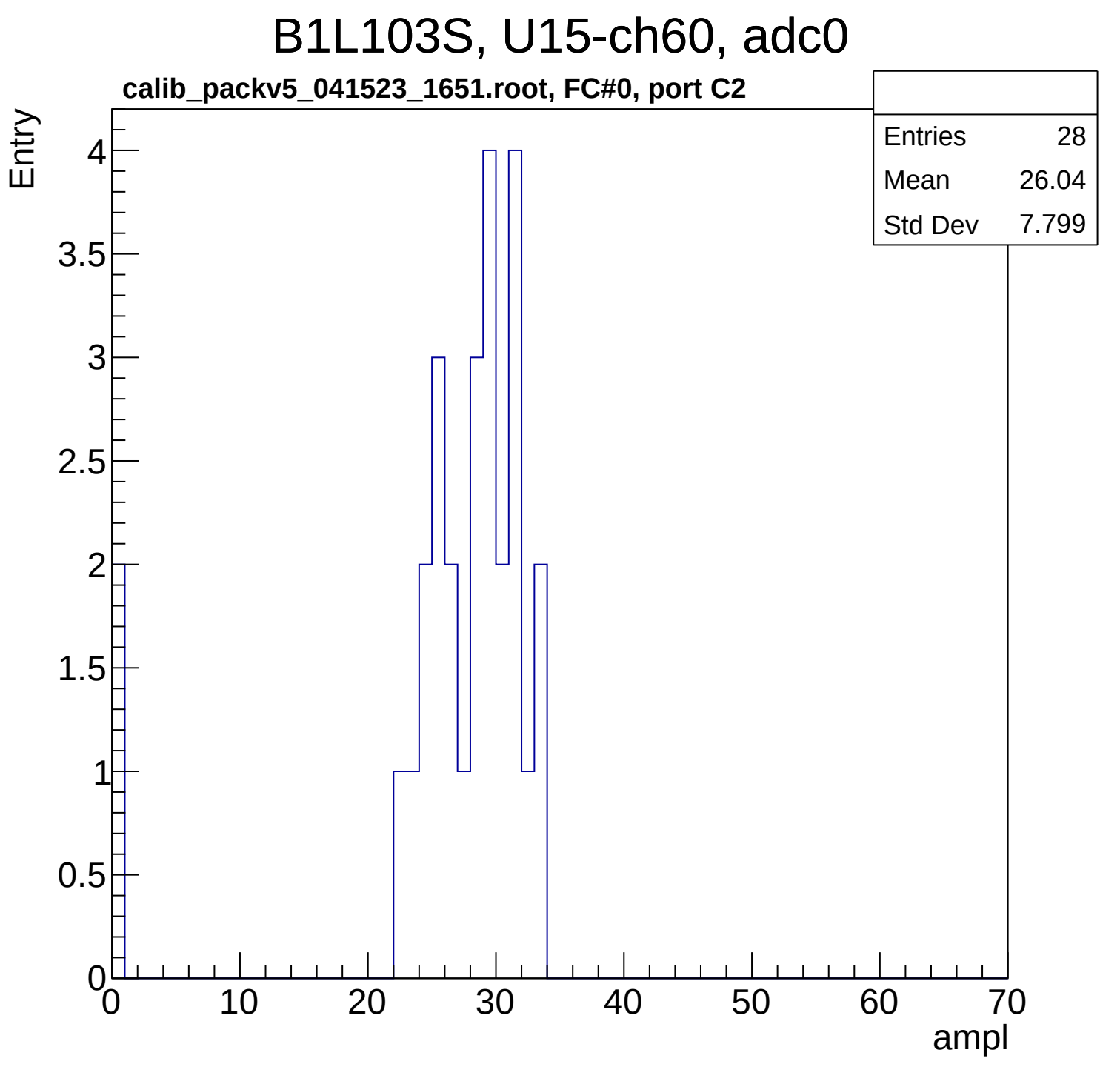
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch59, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 5.727
Std Dev 18.11
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch60, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 26.04
Std Dev 7.799
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
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20
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40
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60
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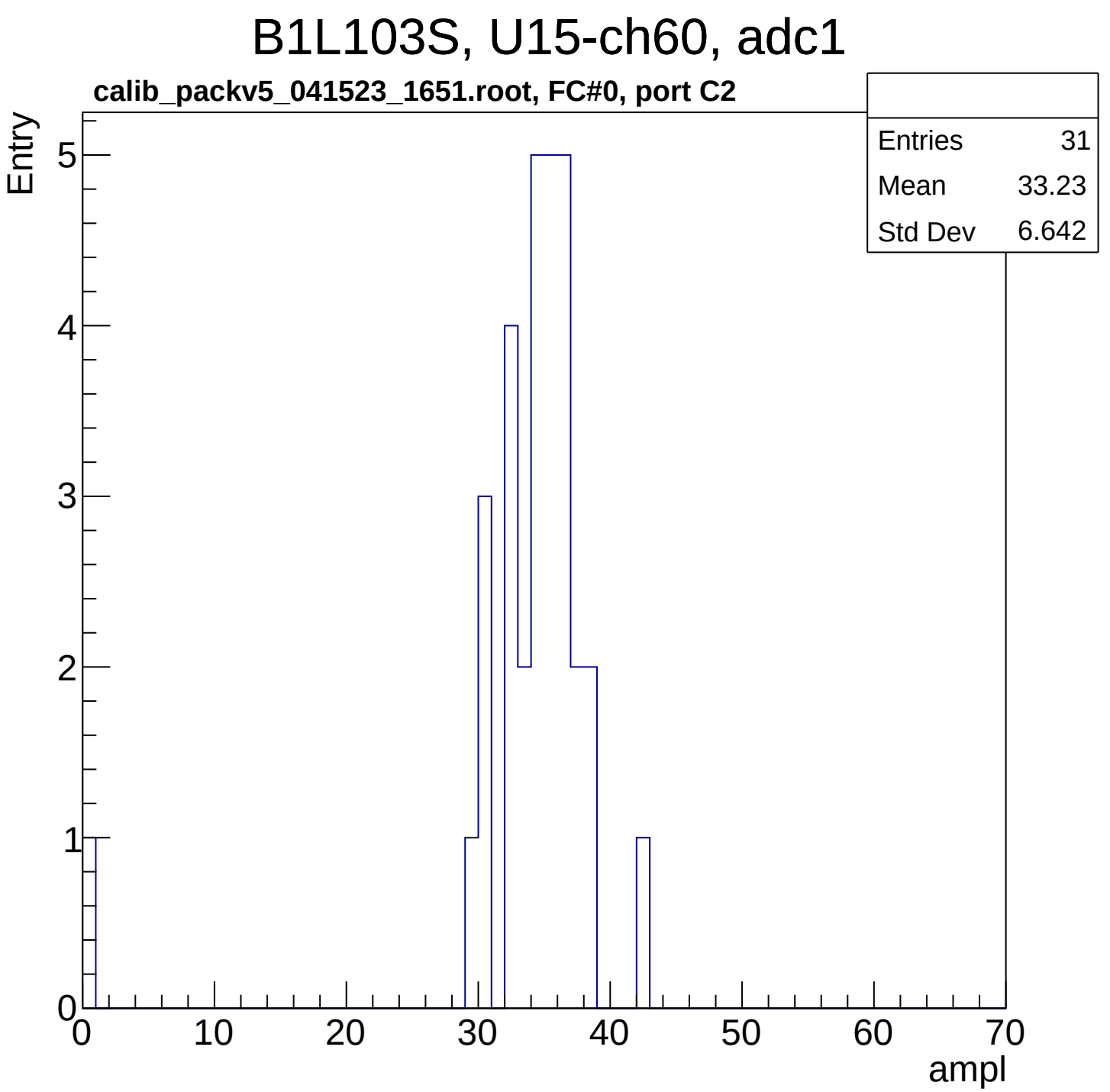
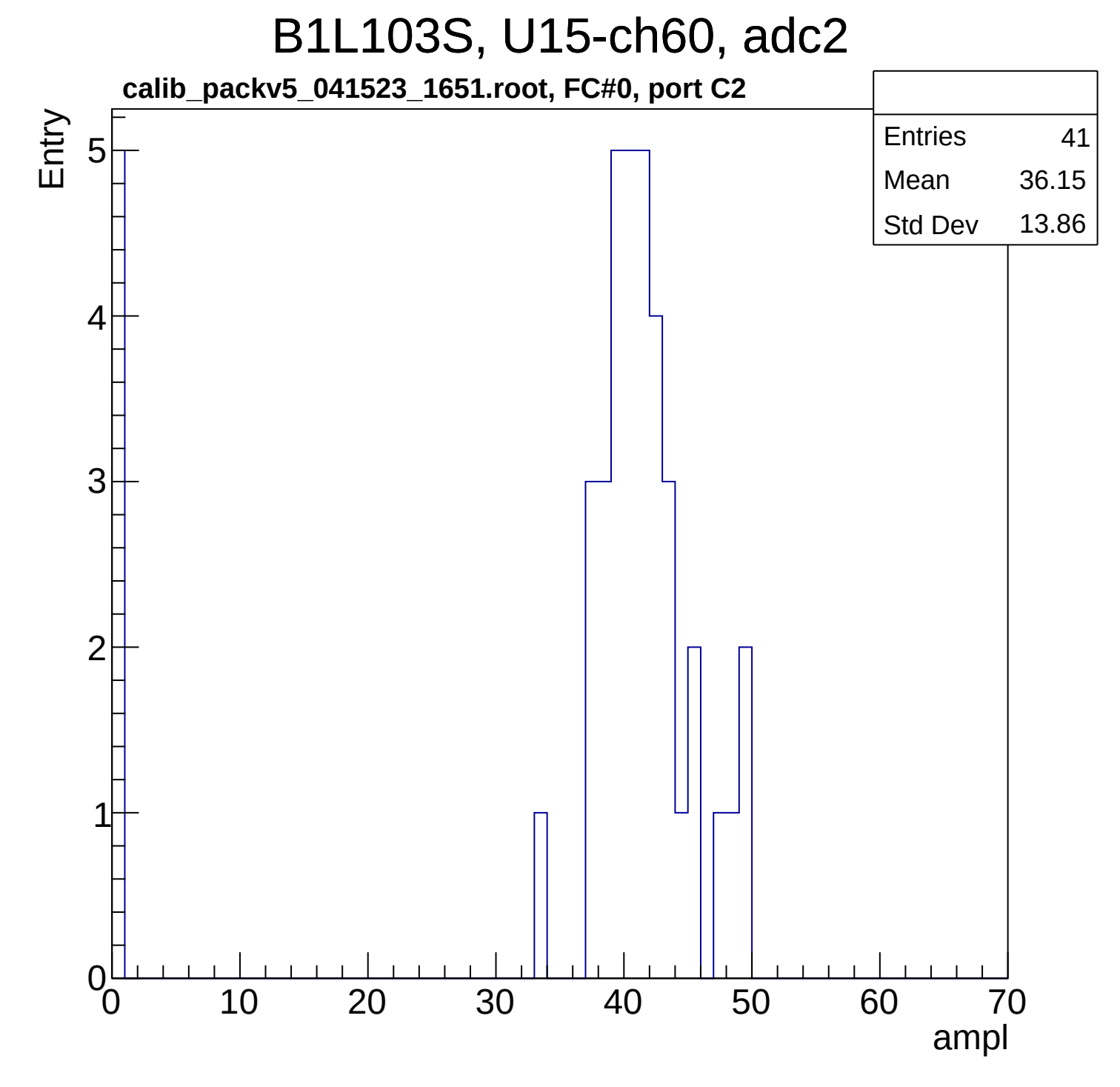
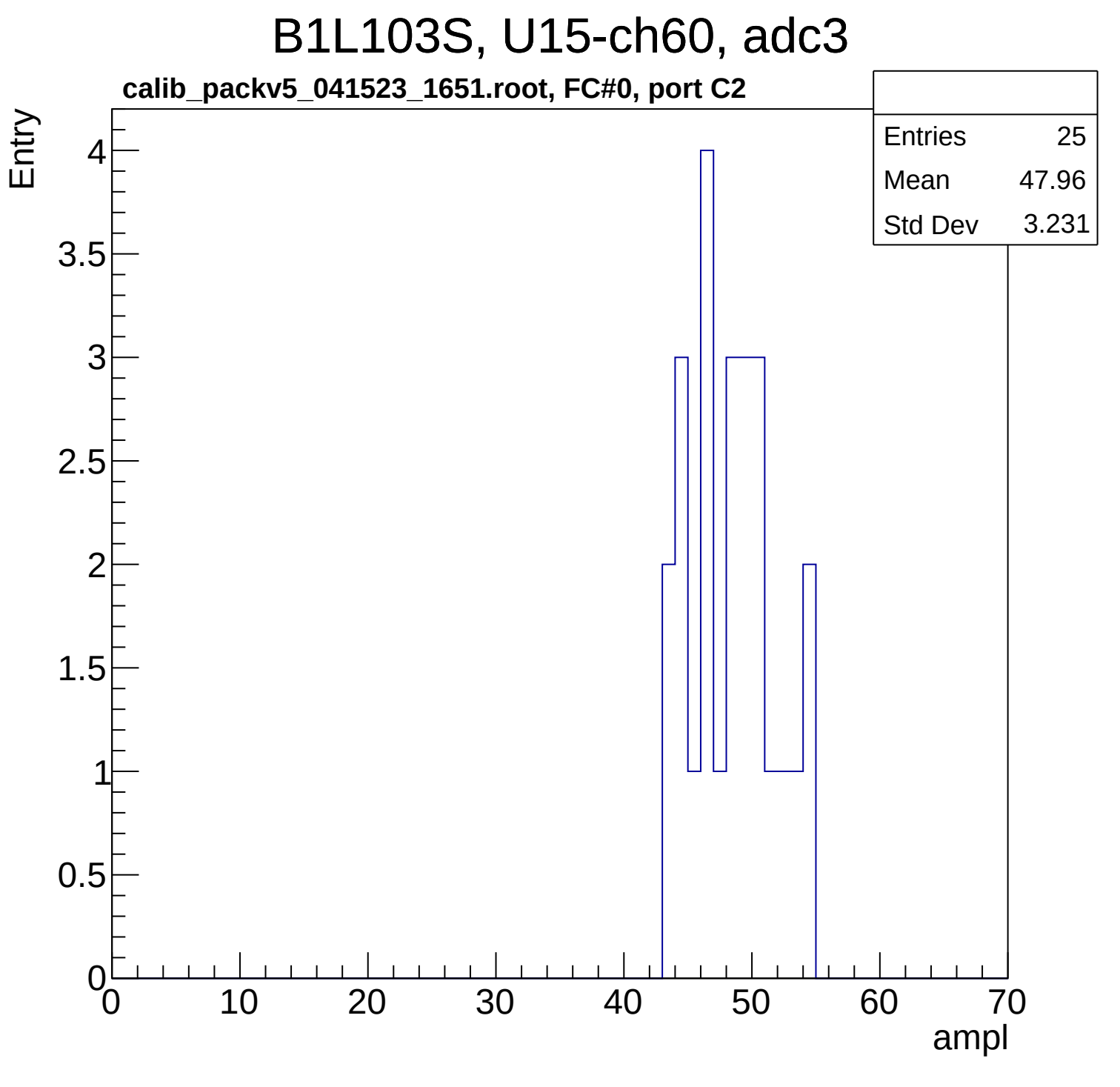

B1L103S, U15-ch60, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 33.23
Std Dev 6.642
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch60, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 36.15
Std Dev 13.86
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch60, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 47.96
Std Dev 3.231
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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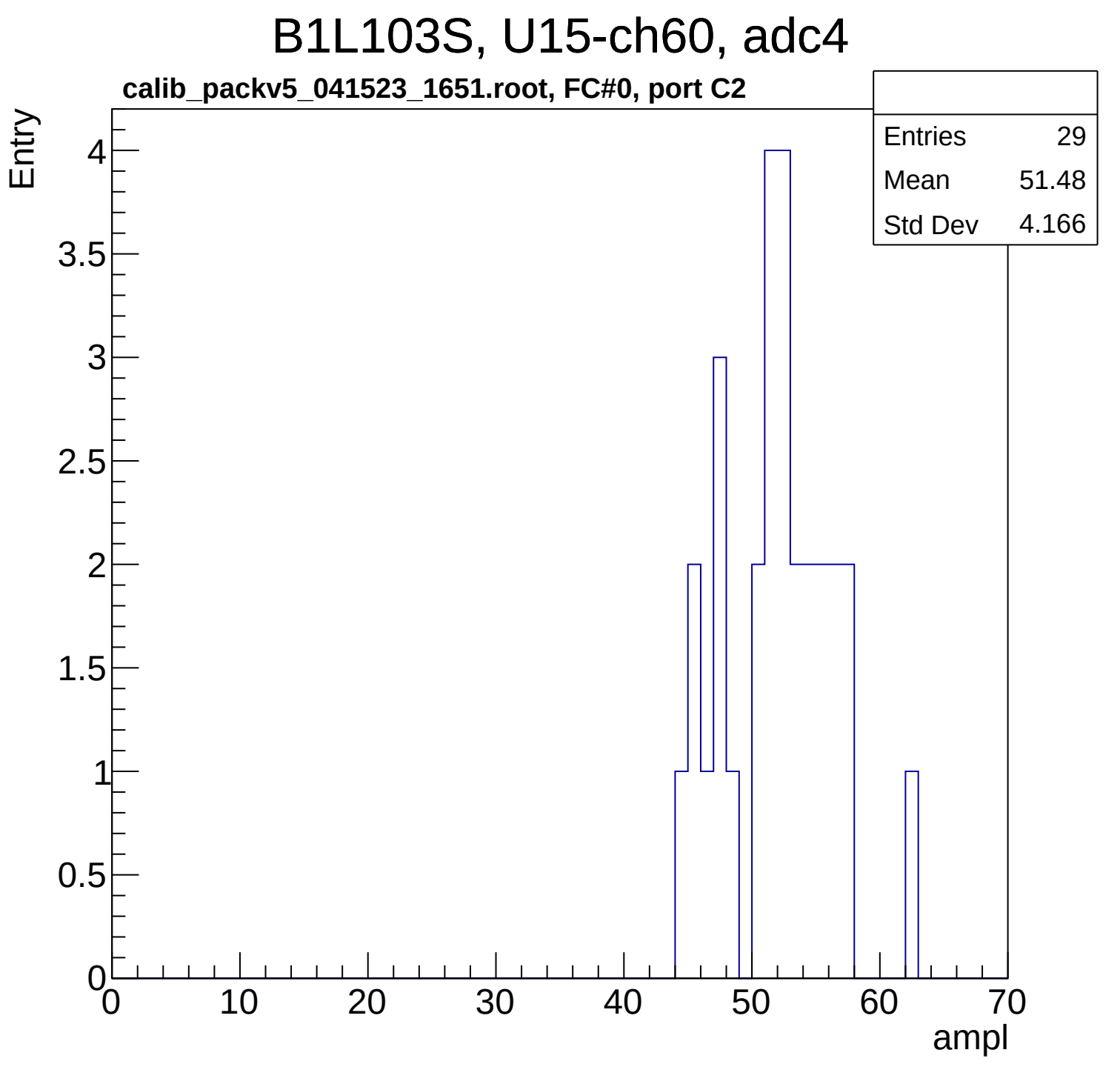
B1L103S, U15-ch60, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 51.48
Std Dev 4.166
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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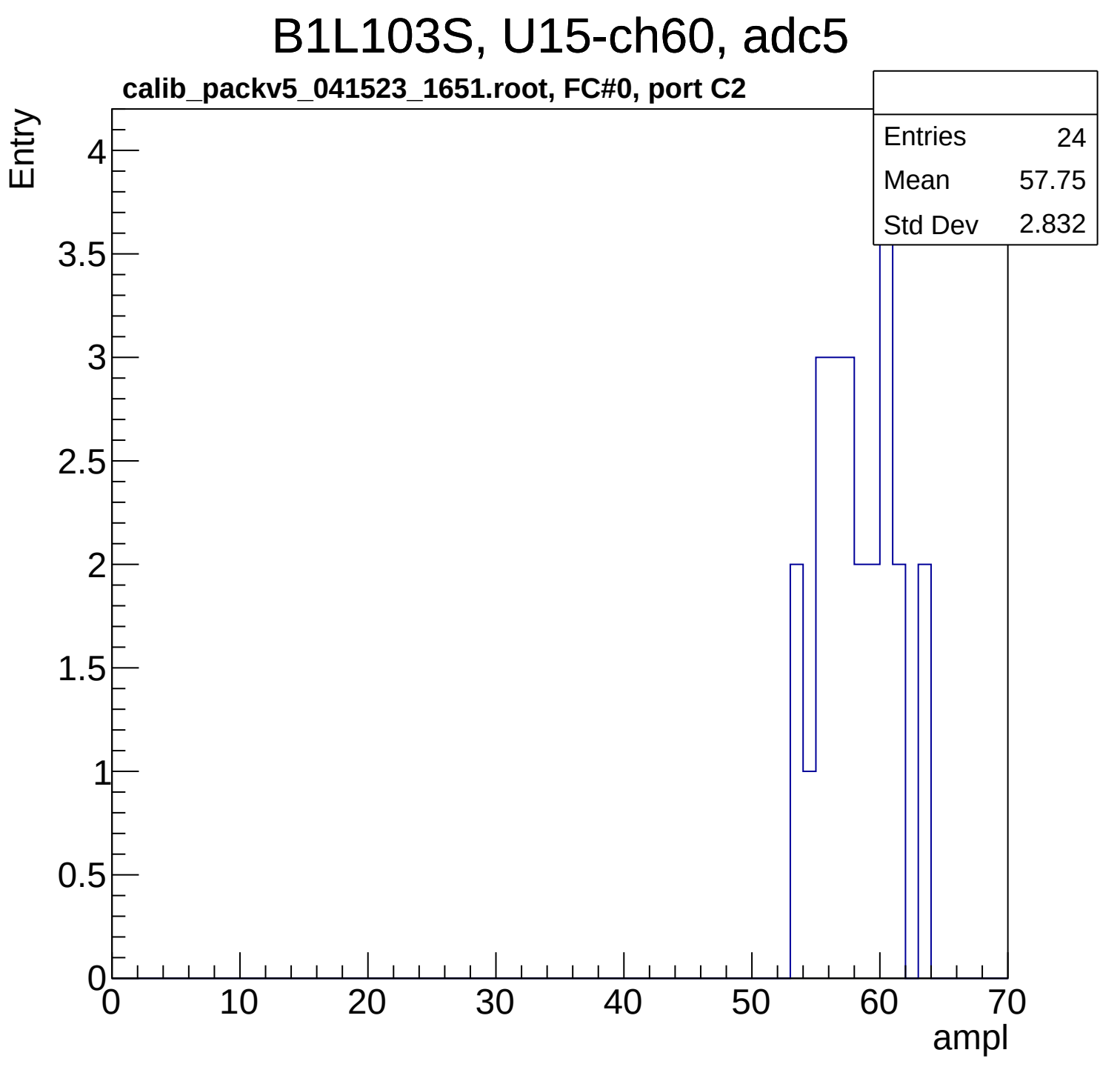
B1L103S, U15-ch60, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 57.75
Std Dev 2.832
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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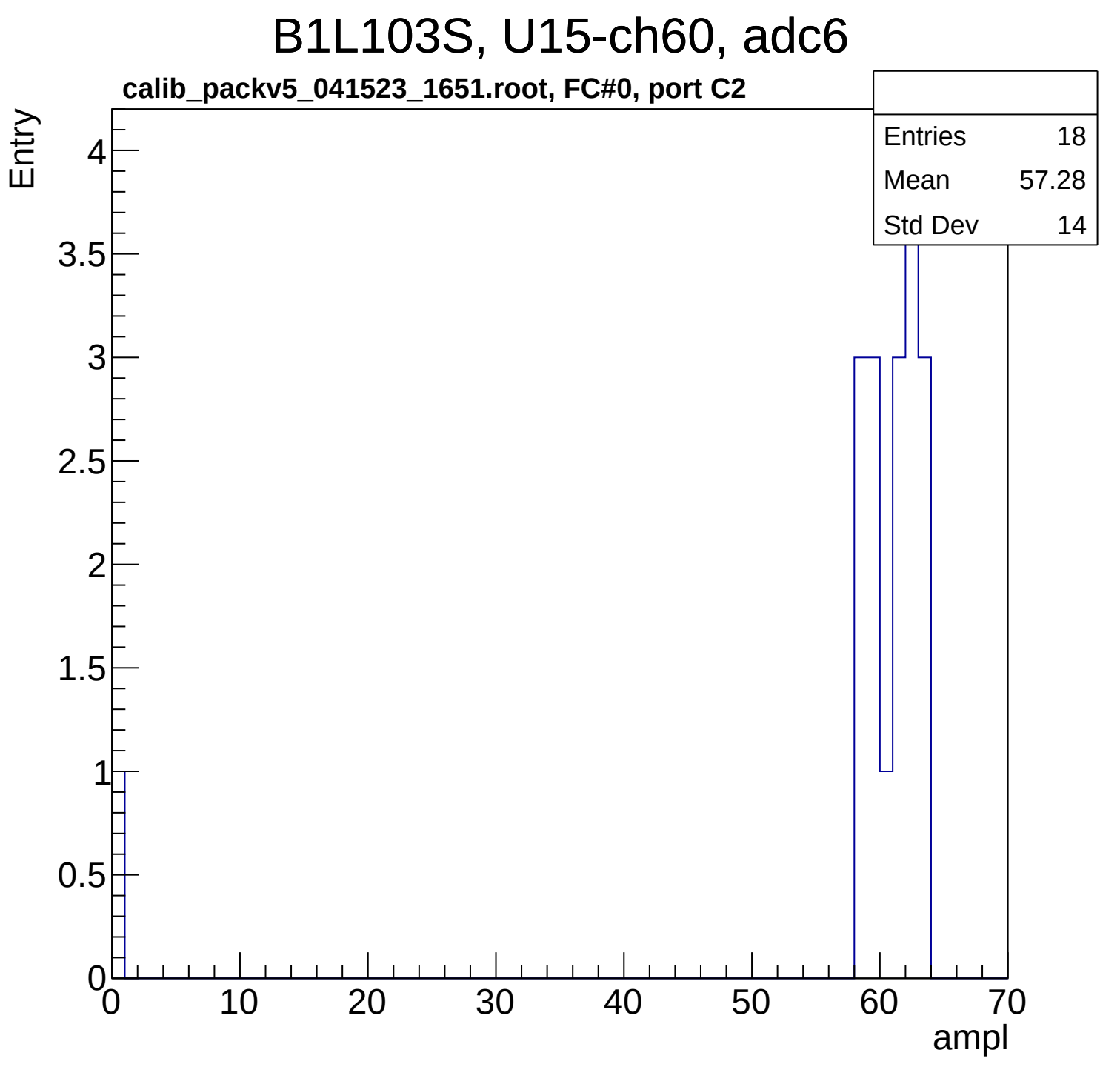
B1L103S, U15-ch60, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 57.28
Std Dev 14
Entry
ampl
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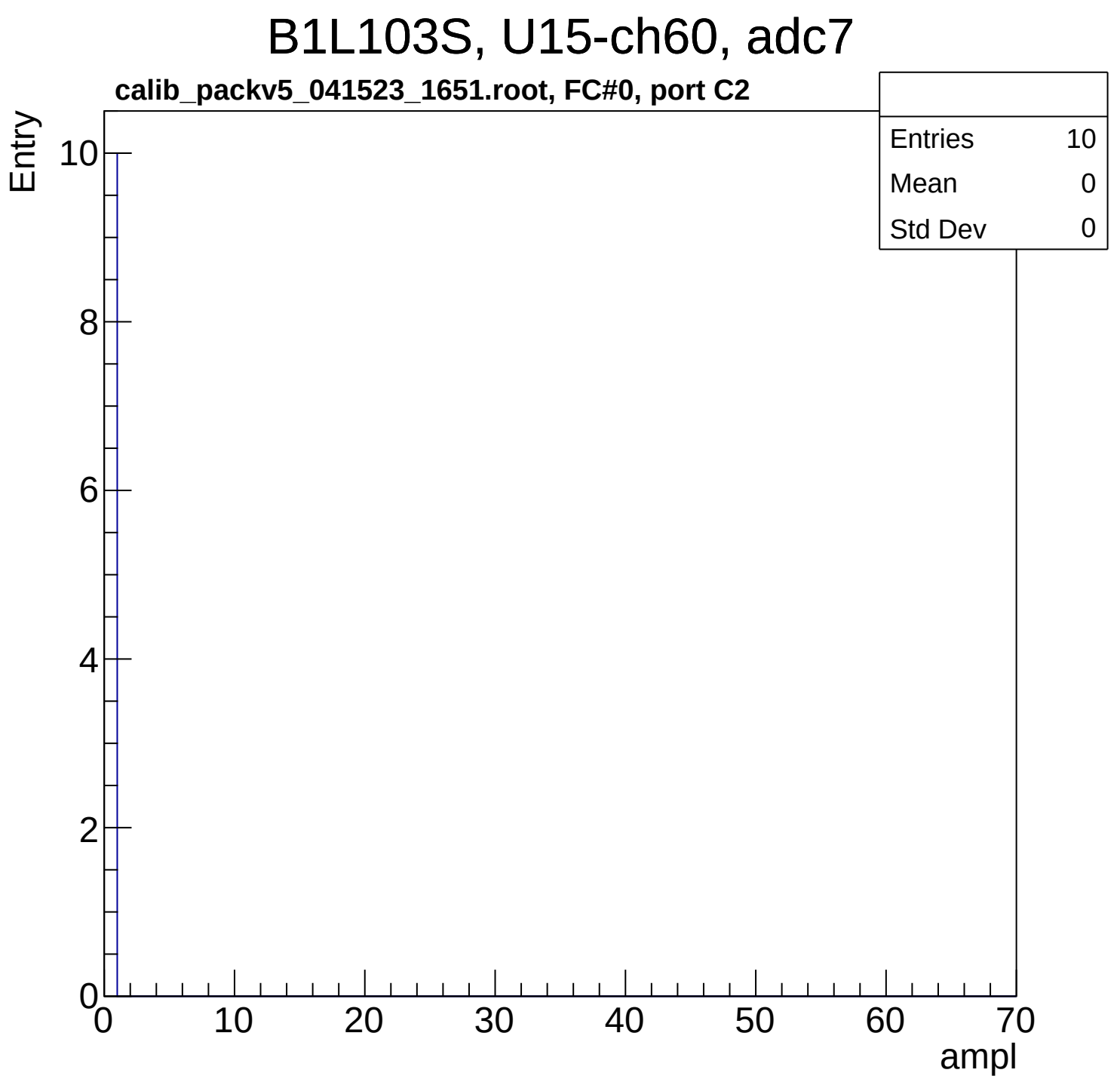
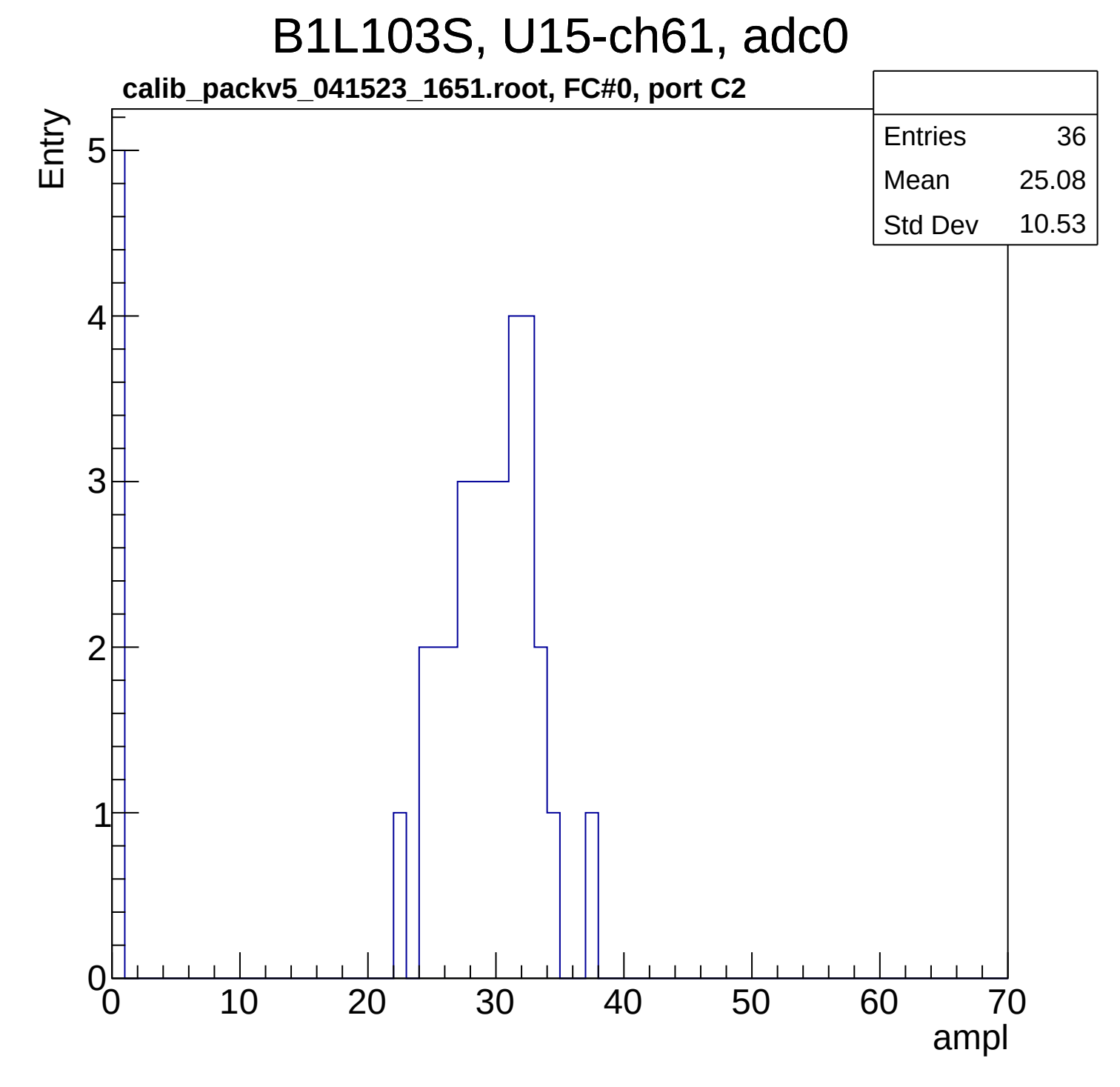
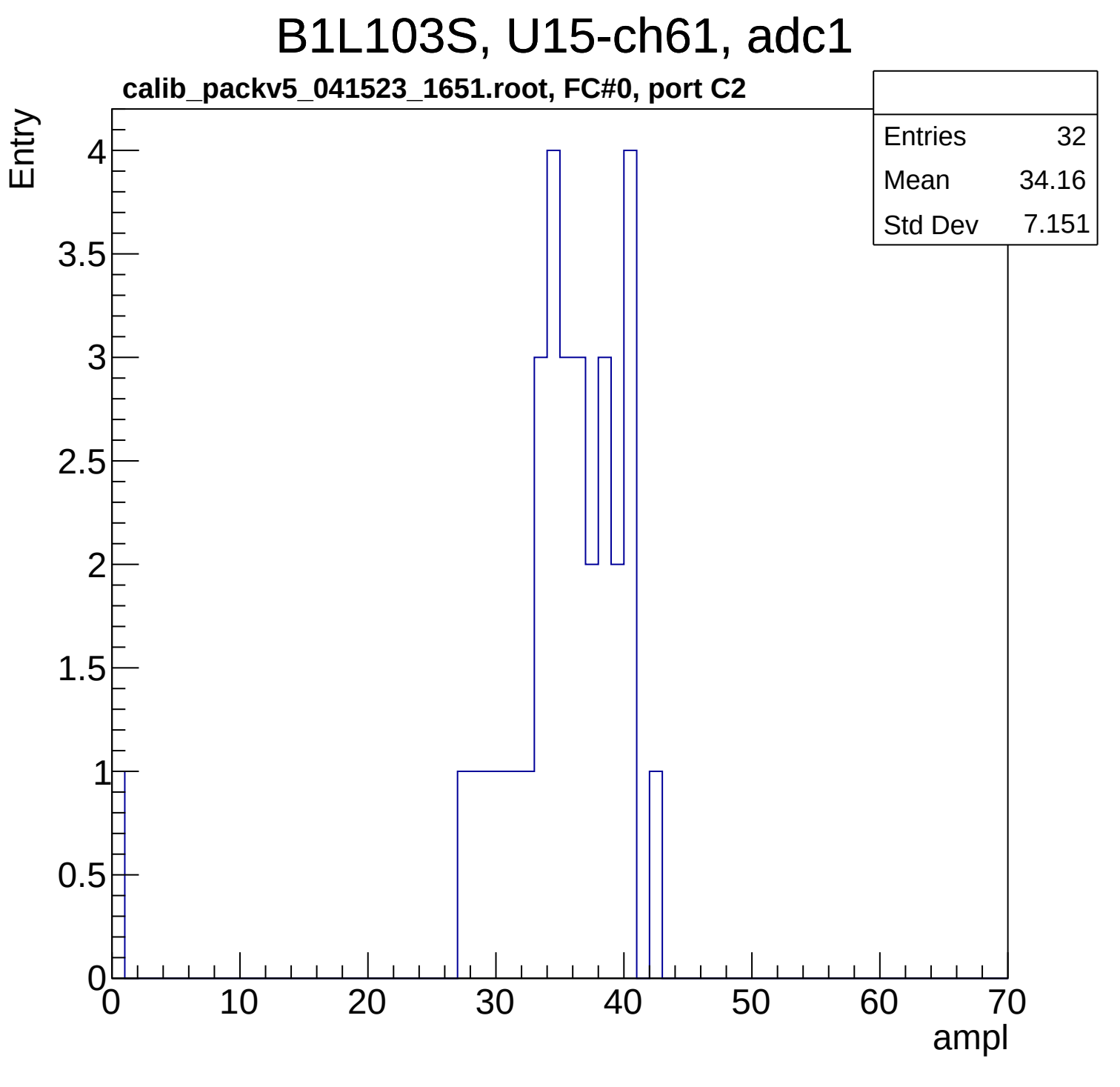
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch60, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch61, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 25.08
Std Dev 10.53
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch61, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 34.16
Std Dev 7.151
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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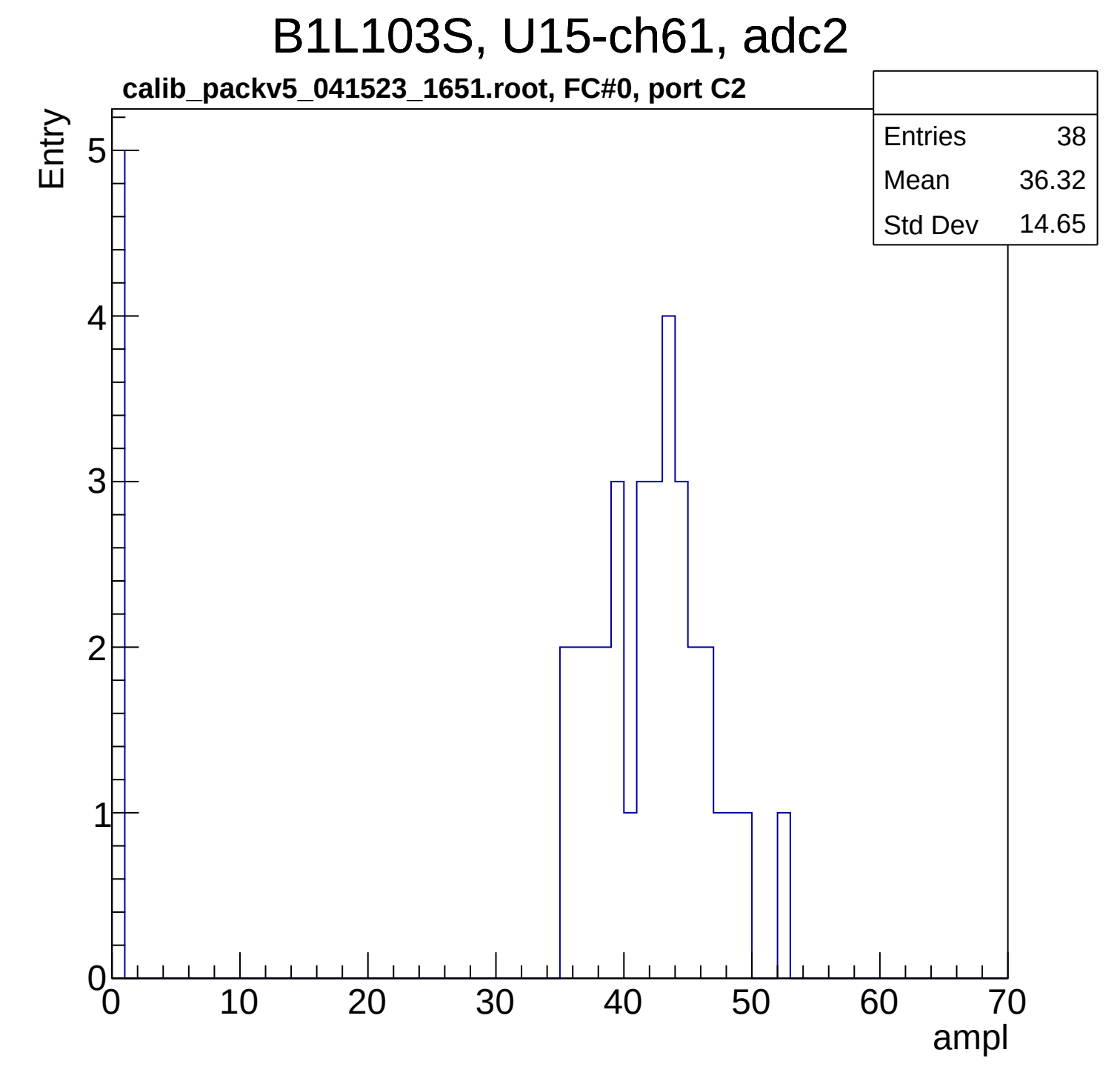
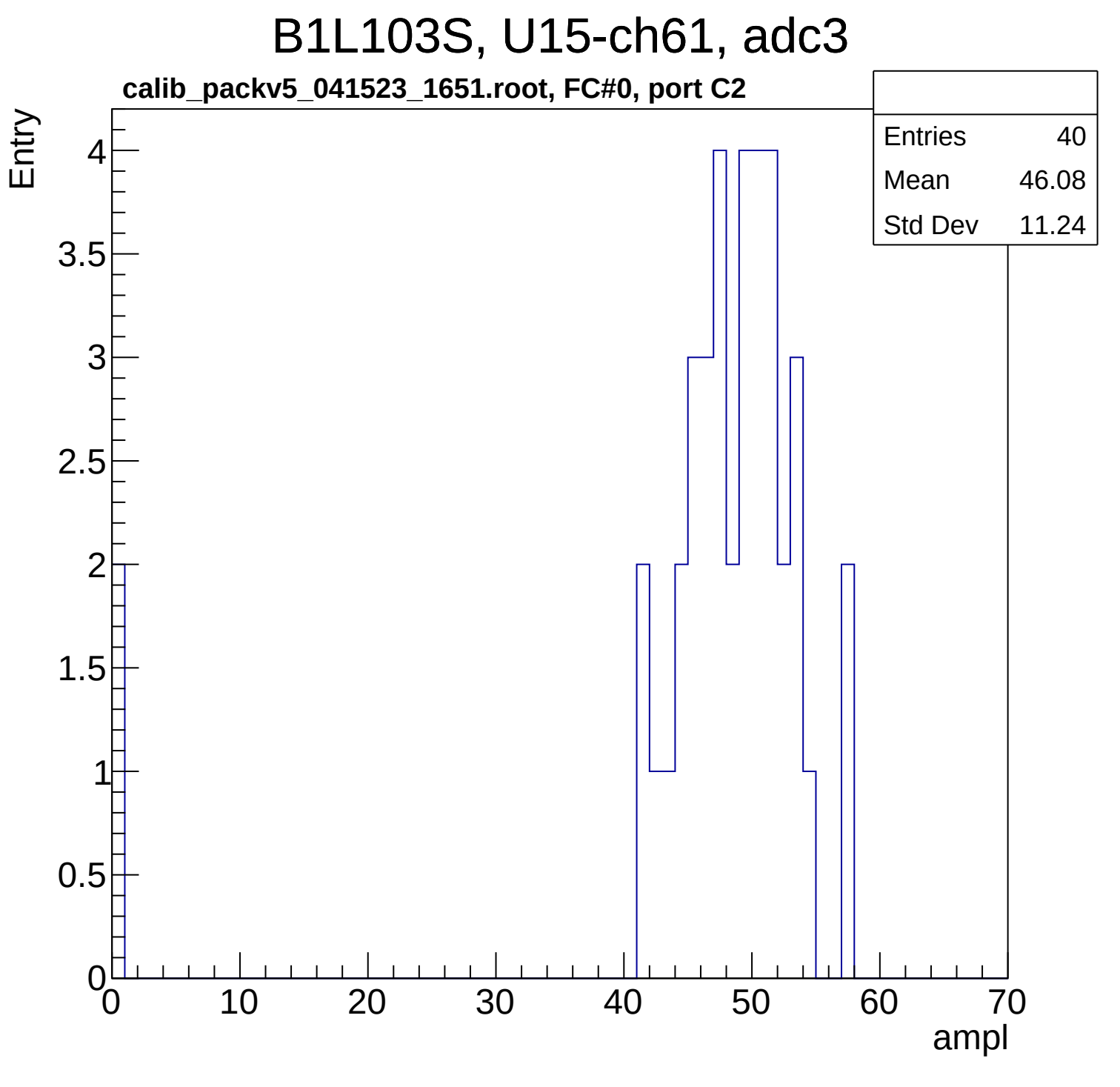
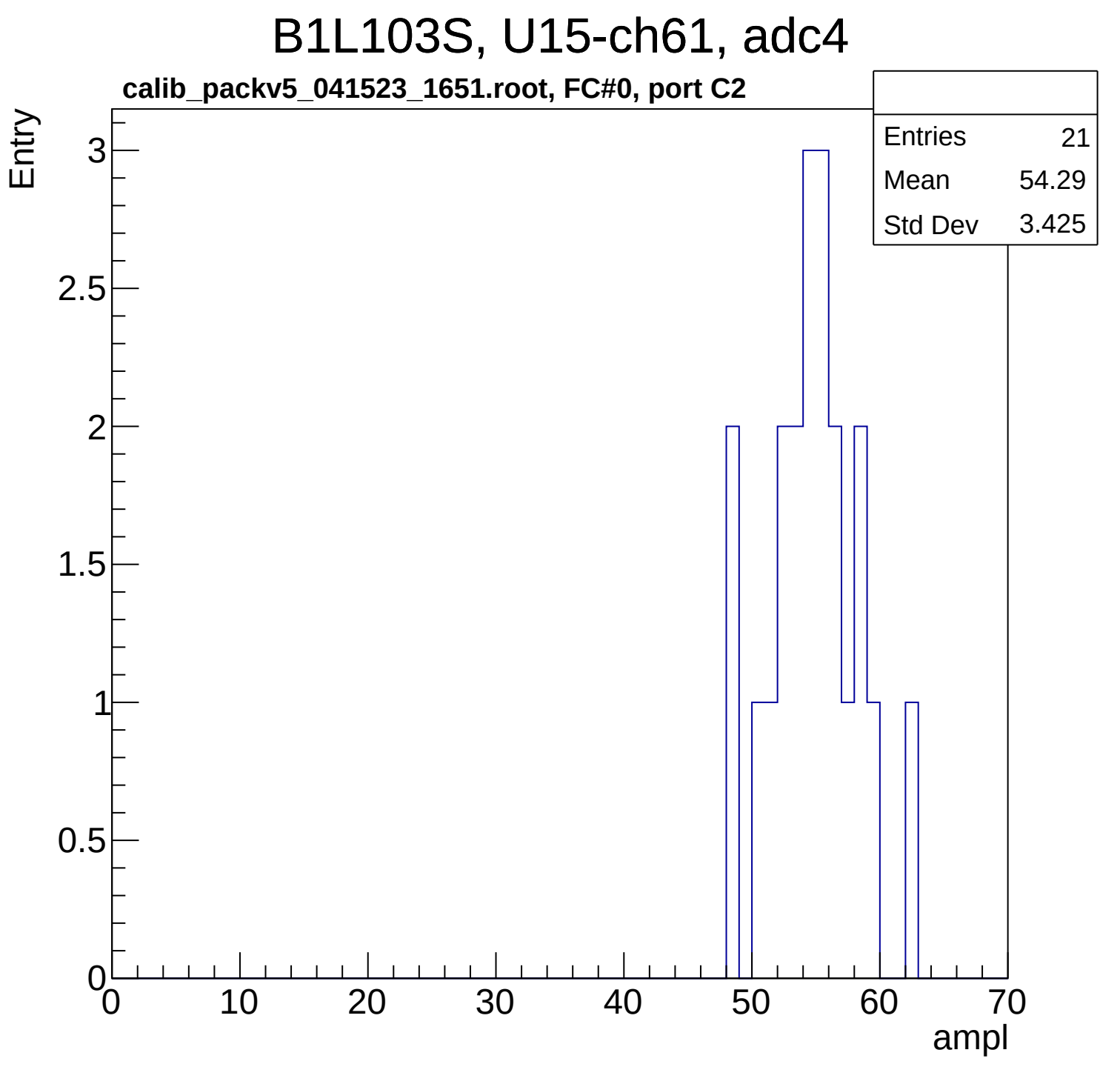

B1L103S, U15-ch61, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 36.32
Std Dev 14.65
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch61, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 46.08
Std Dev 11.24
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch61, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 54.29
Std Dev 3.425
Entry
ampl
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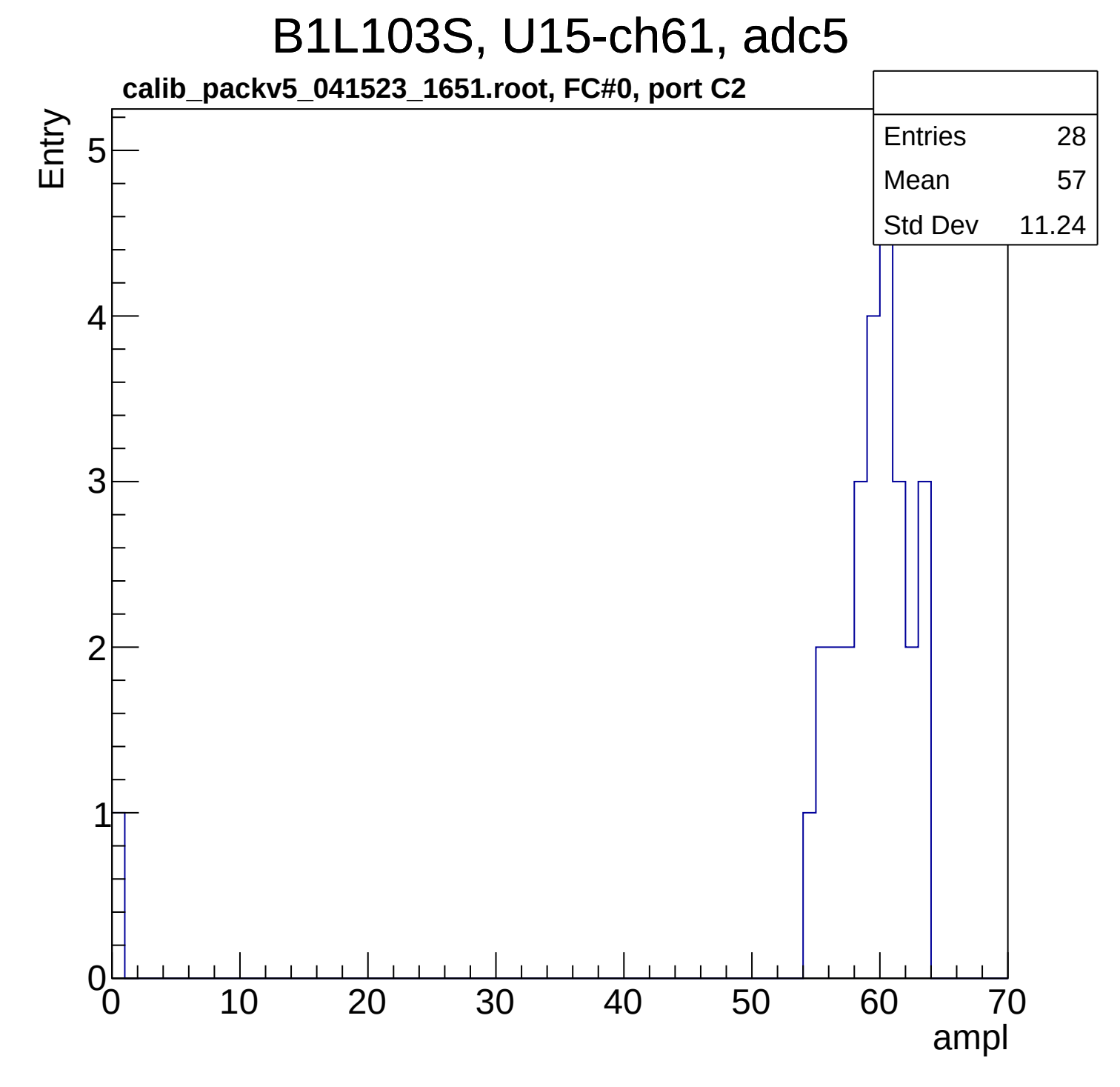
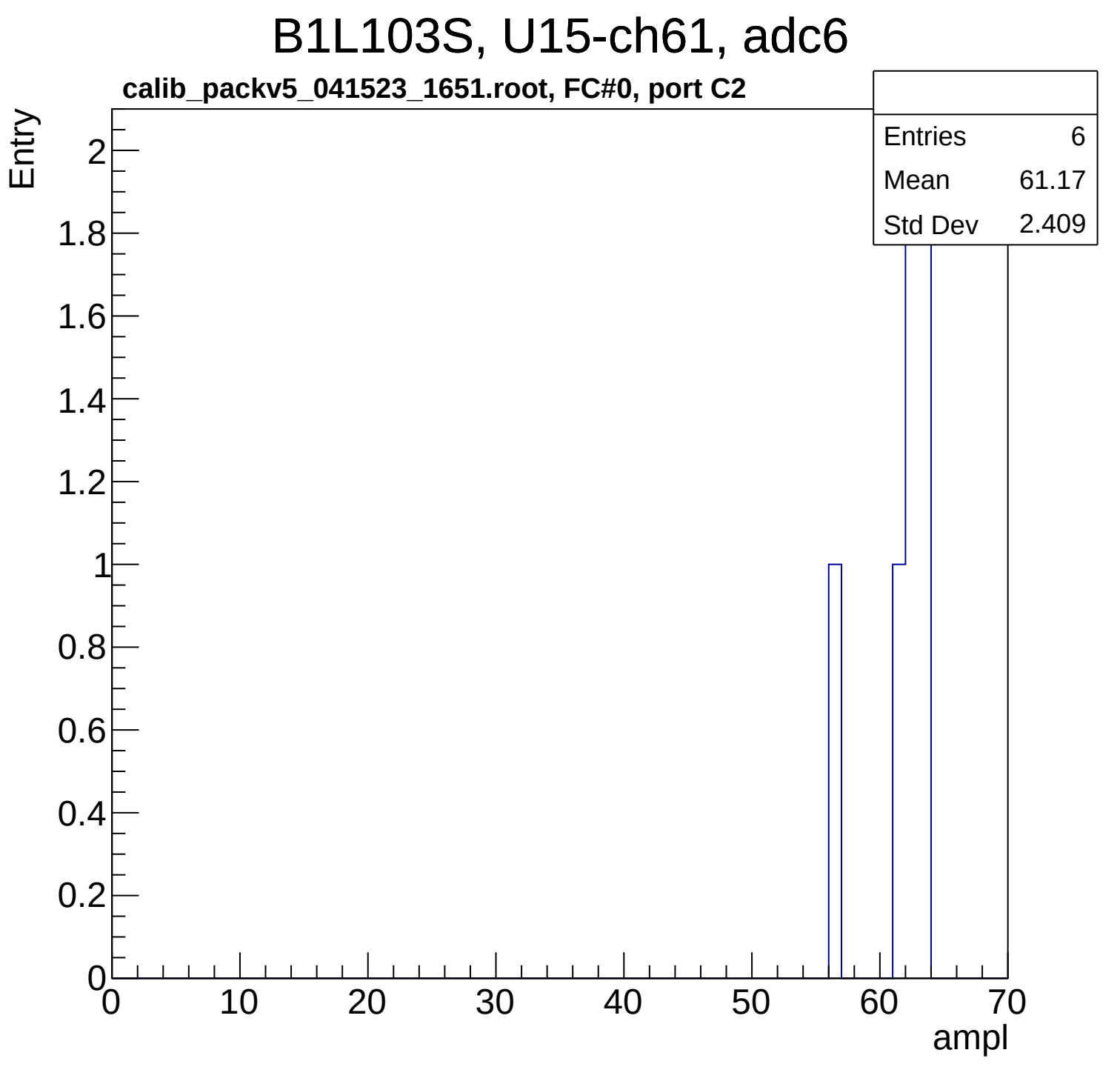
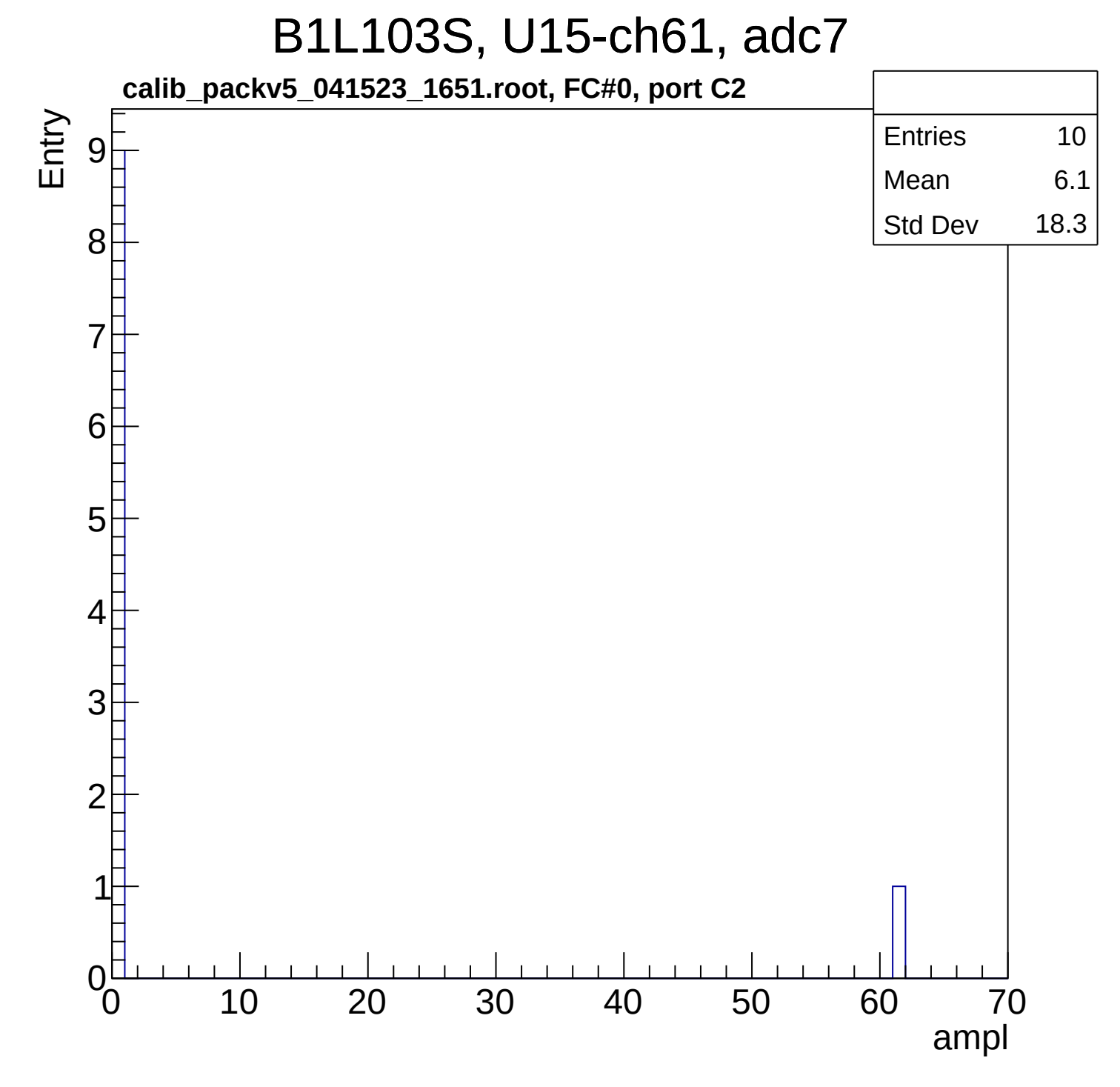
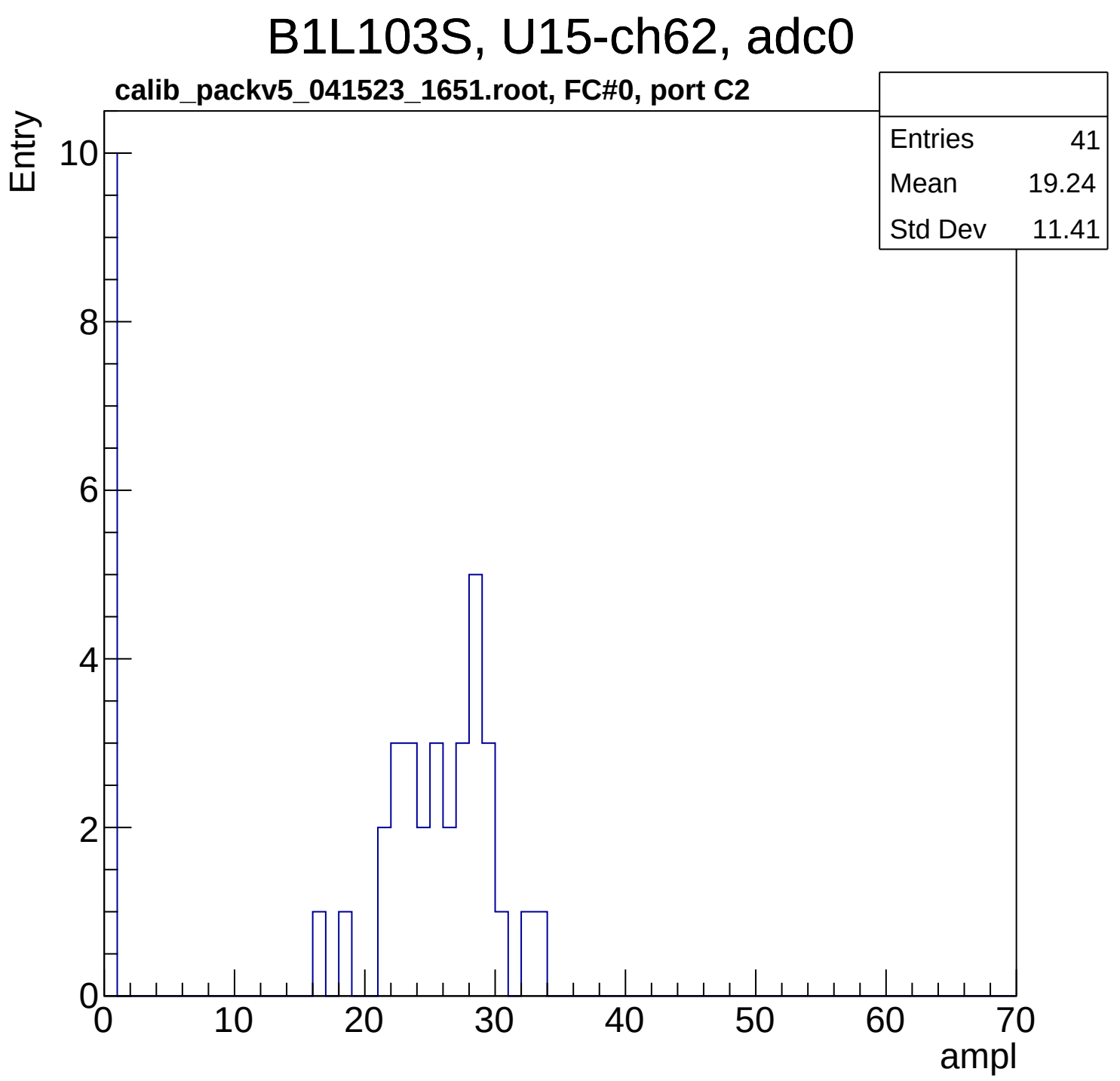
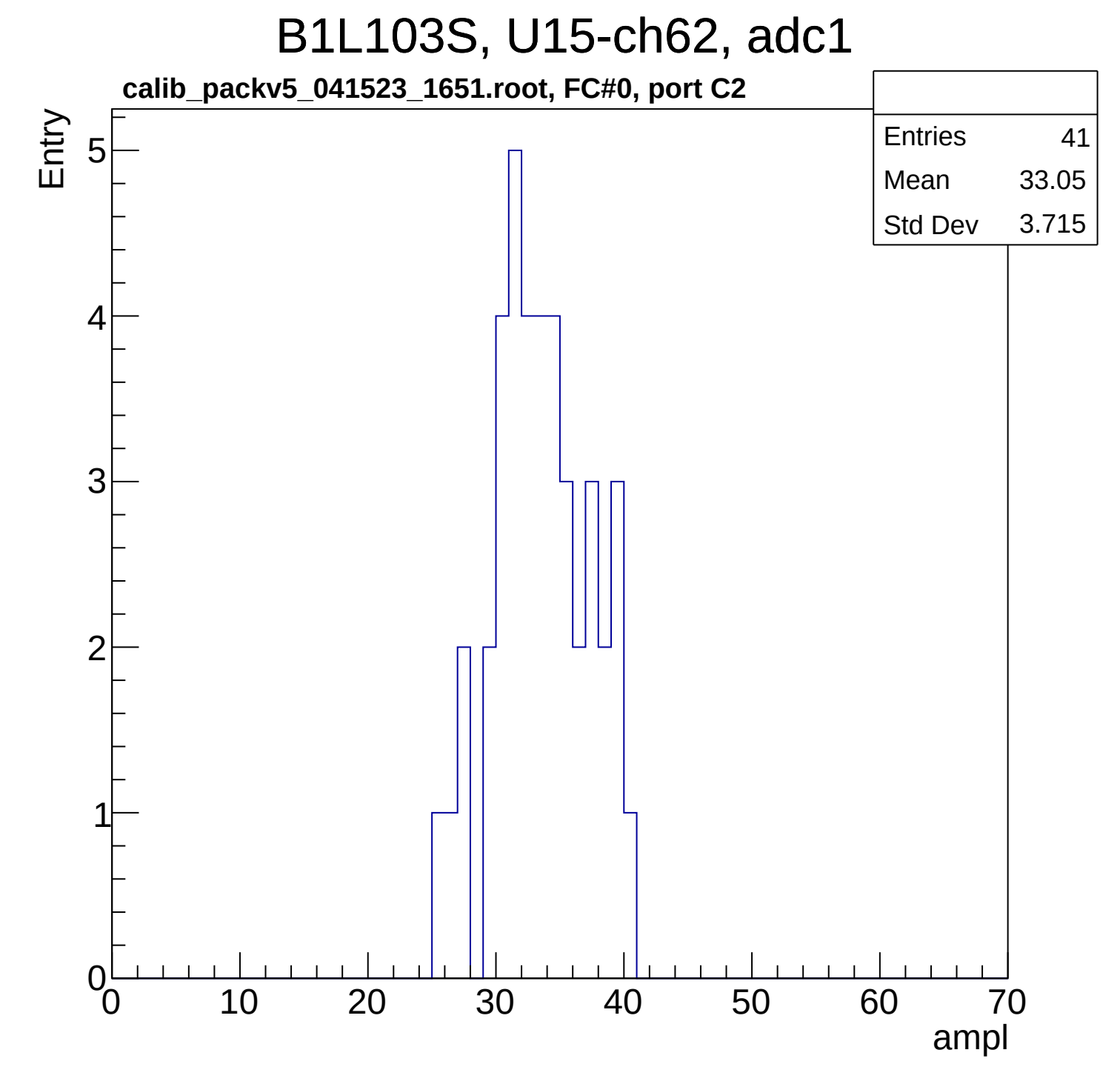
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

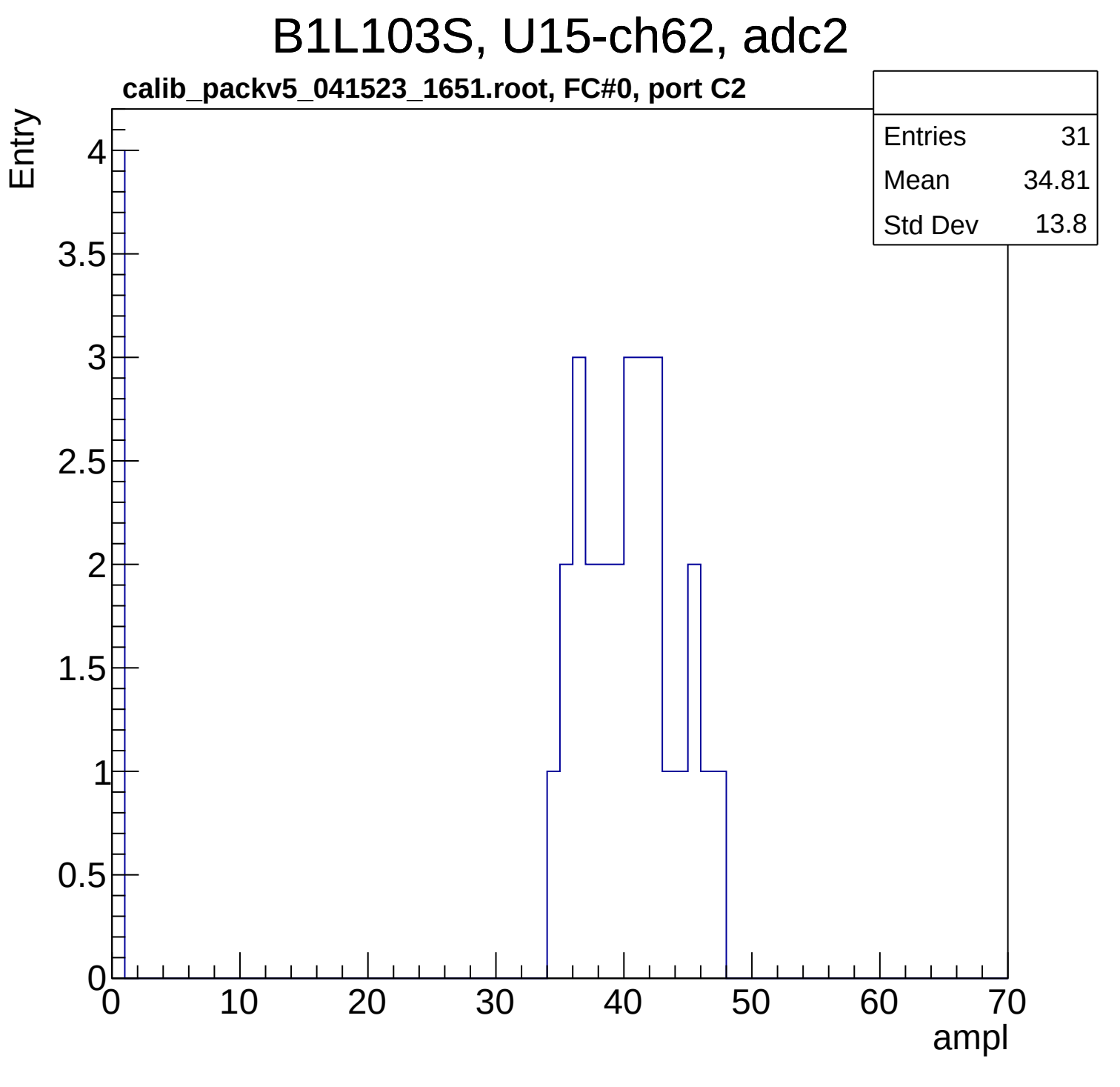

B1L103S, U15-ch61, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 57
Std Dev 11.24
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch61, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.17
Std Dev 2.409
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U15-ch61, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 6.1
Std Dev 18.3
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U15-ch62, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 19.24
Std Dev 11.41
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch62, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 33.05
Std Dev 3.715
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch62, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 34.81
Std Dev 13.8
Entry
ampl
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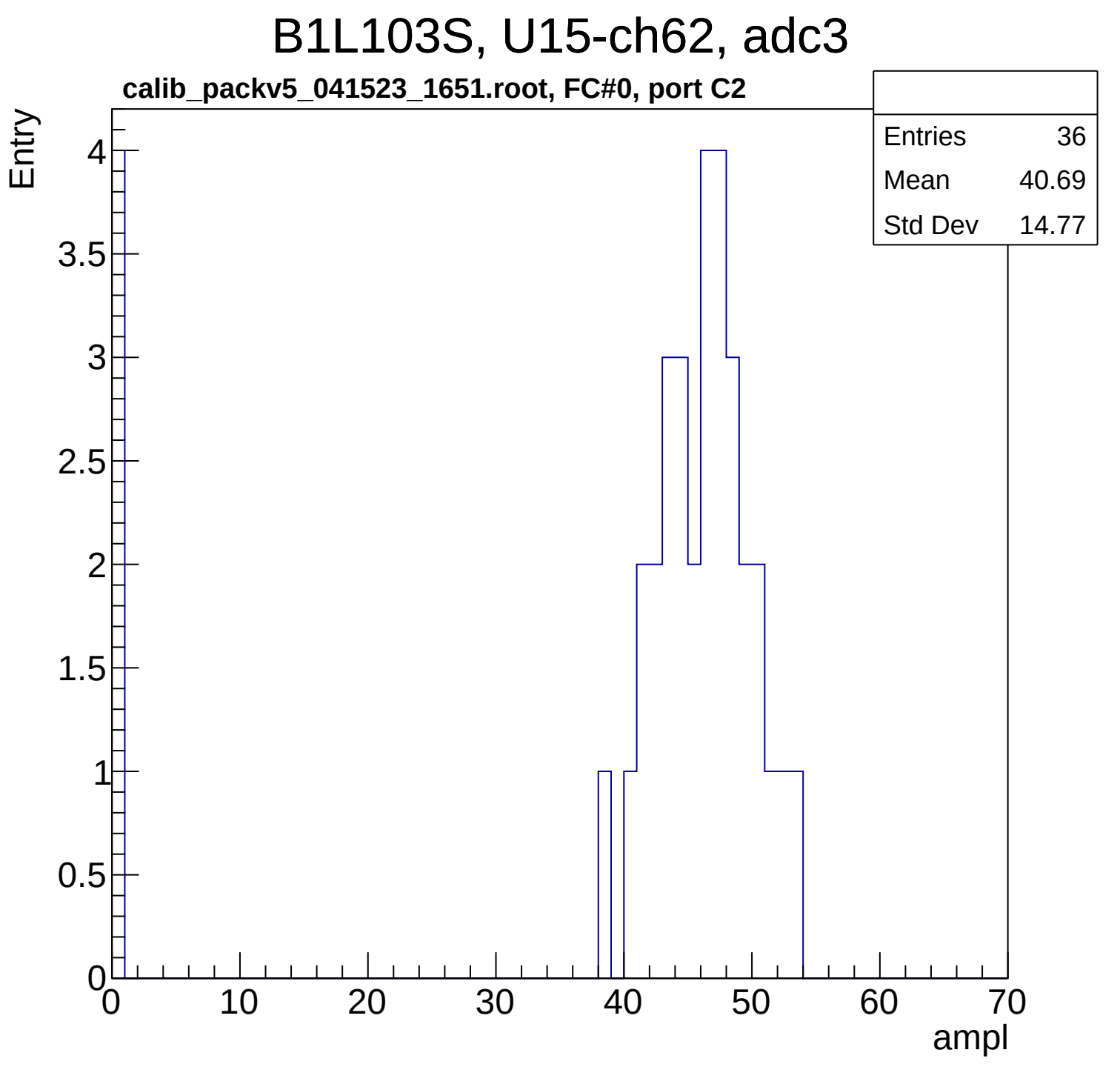
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch62, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 40.69
Std Dev 14.77
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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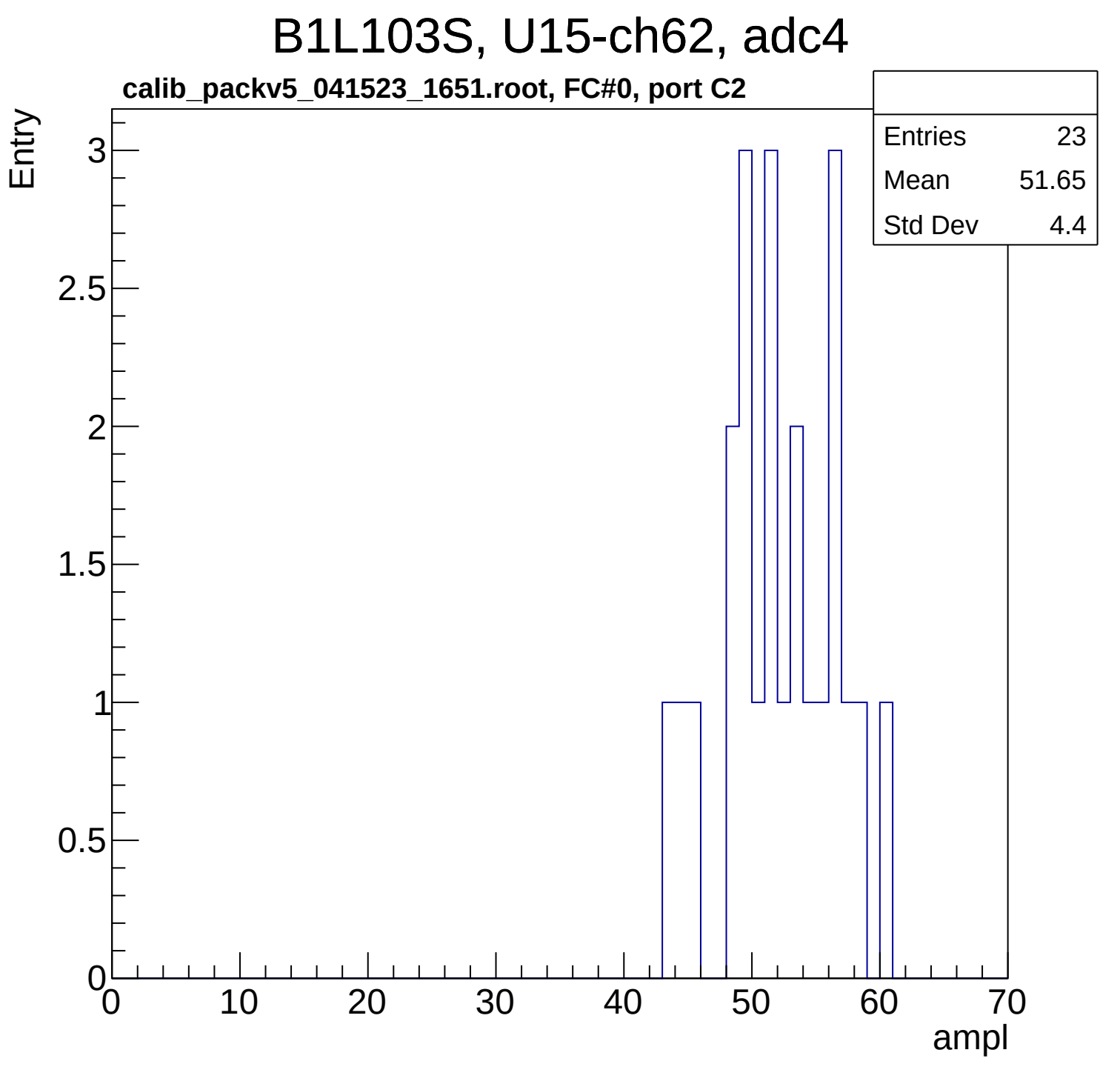
60
70


B1L103S, U15-ch62, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 51.65
Std Dev 4.4
Entry
ampl
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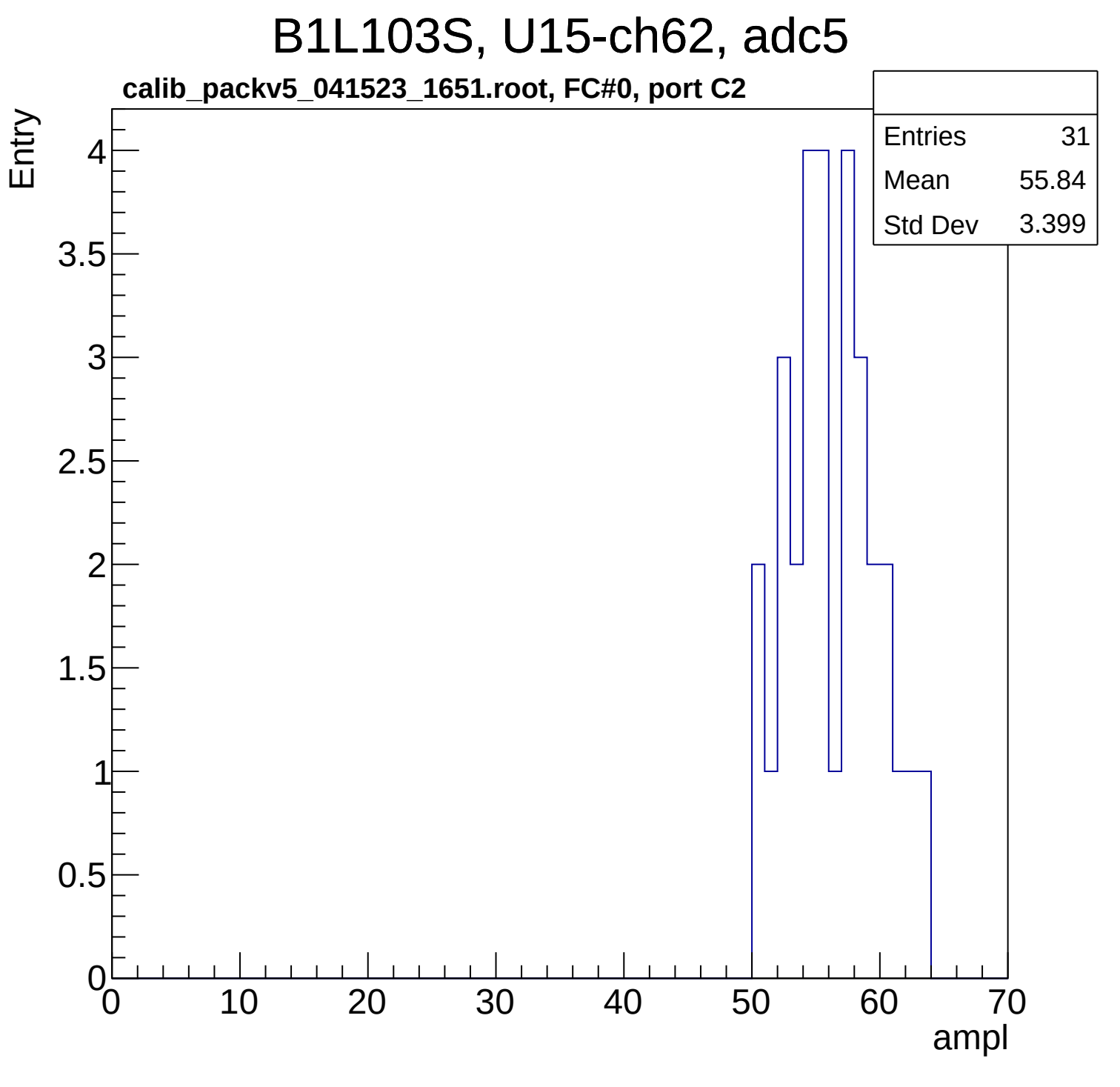
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch62, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 55.84
Std Dev 3.399
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
10
20
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60
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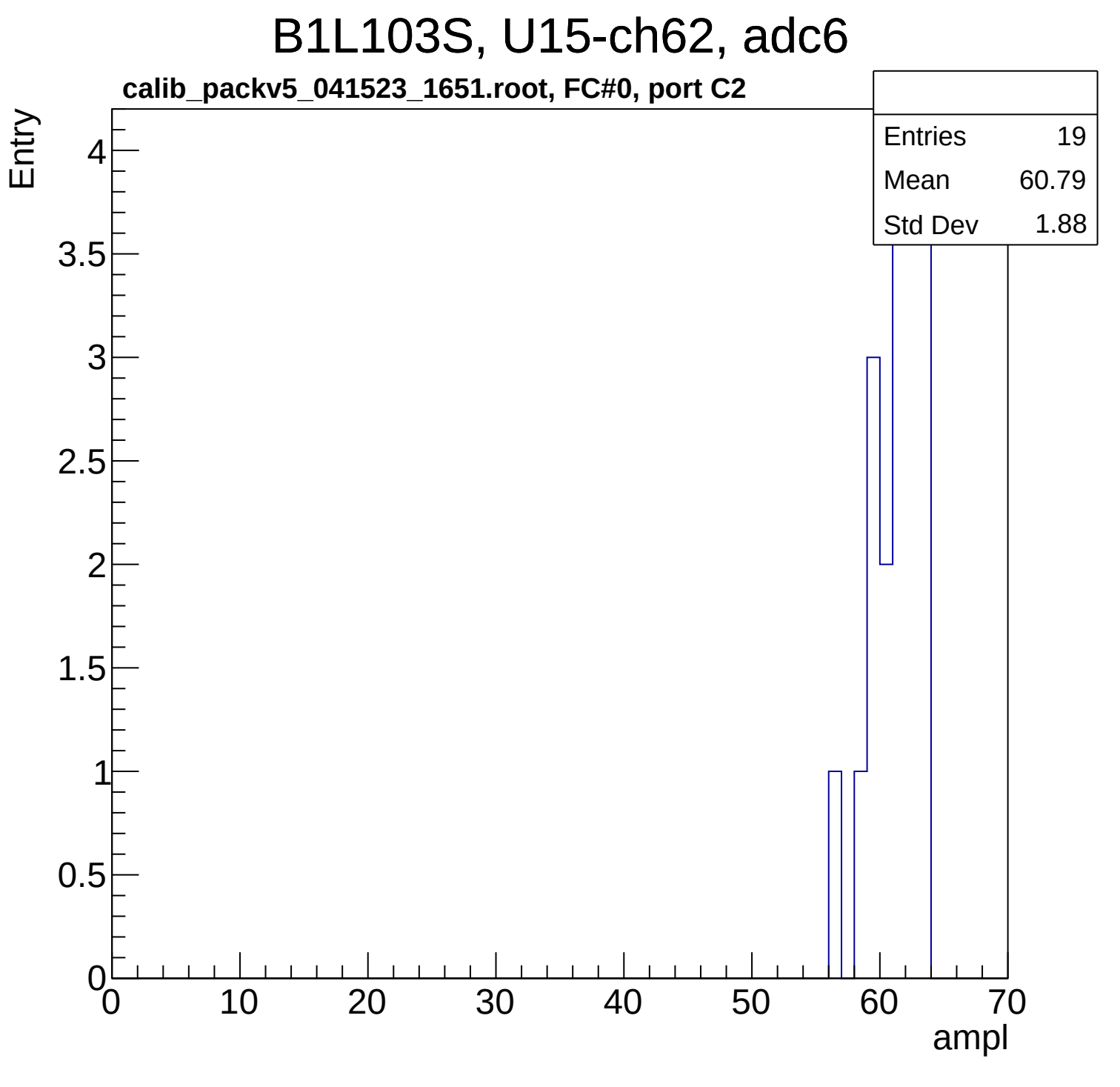
B1L103S, U15-ch62, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 60.79
Std Dev 1.88
Entry
ampl
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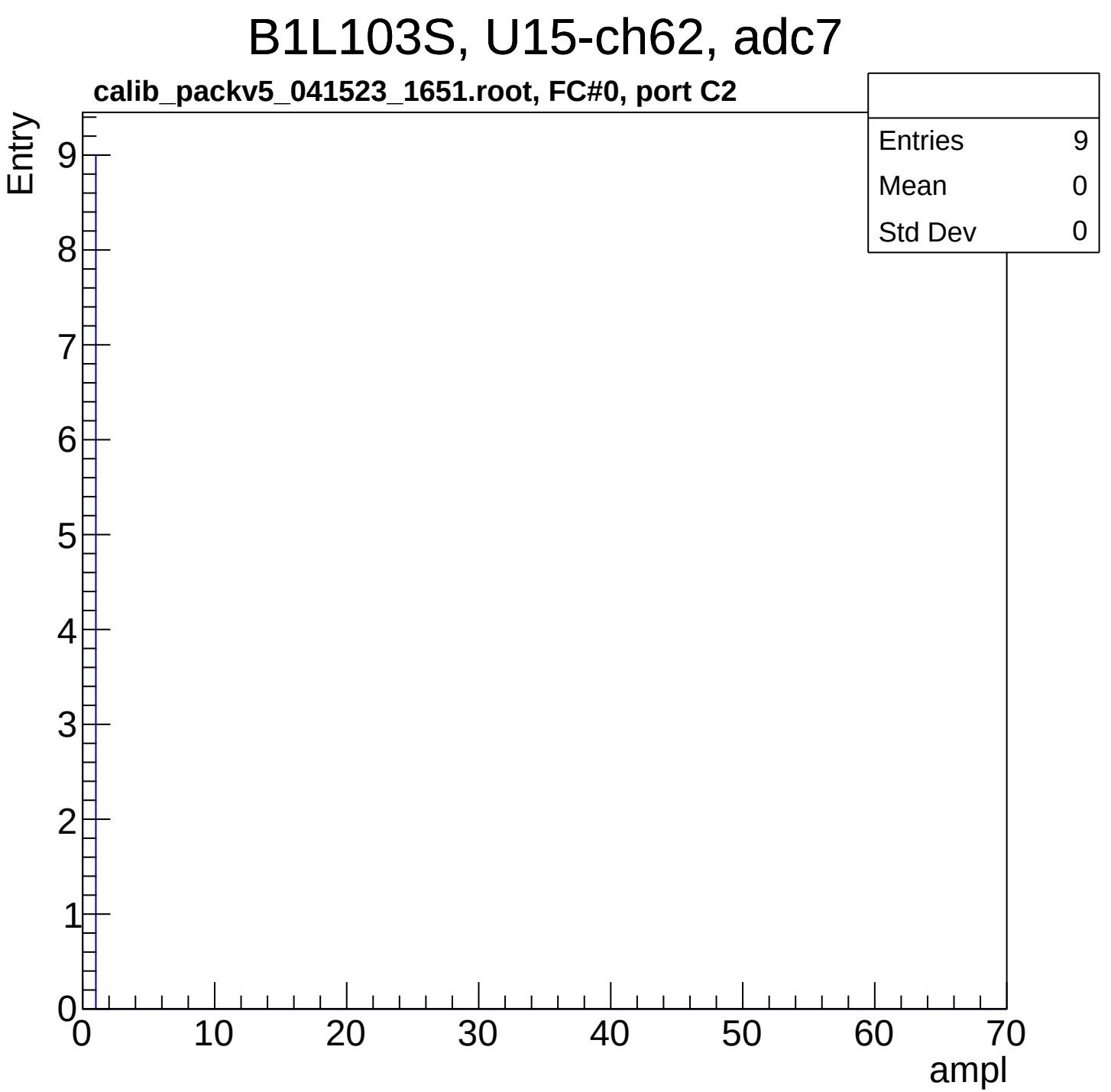
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch62, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 0
Std Dev 0
Entry
0
1
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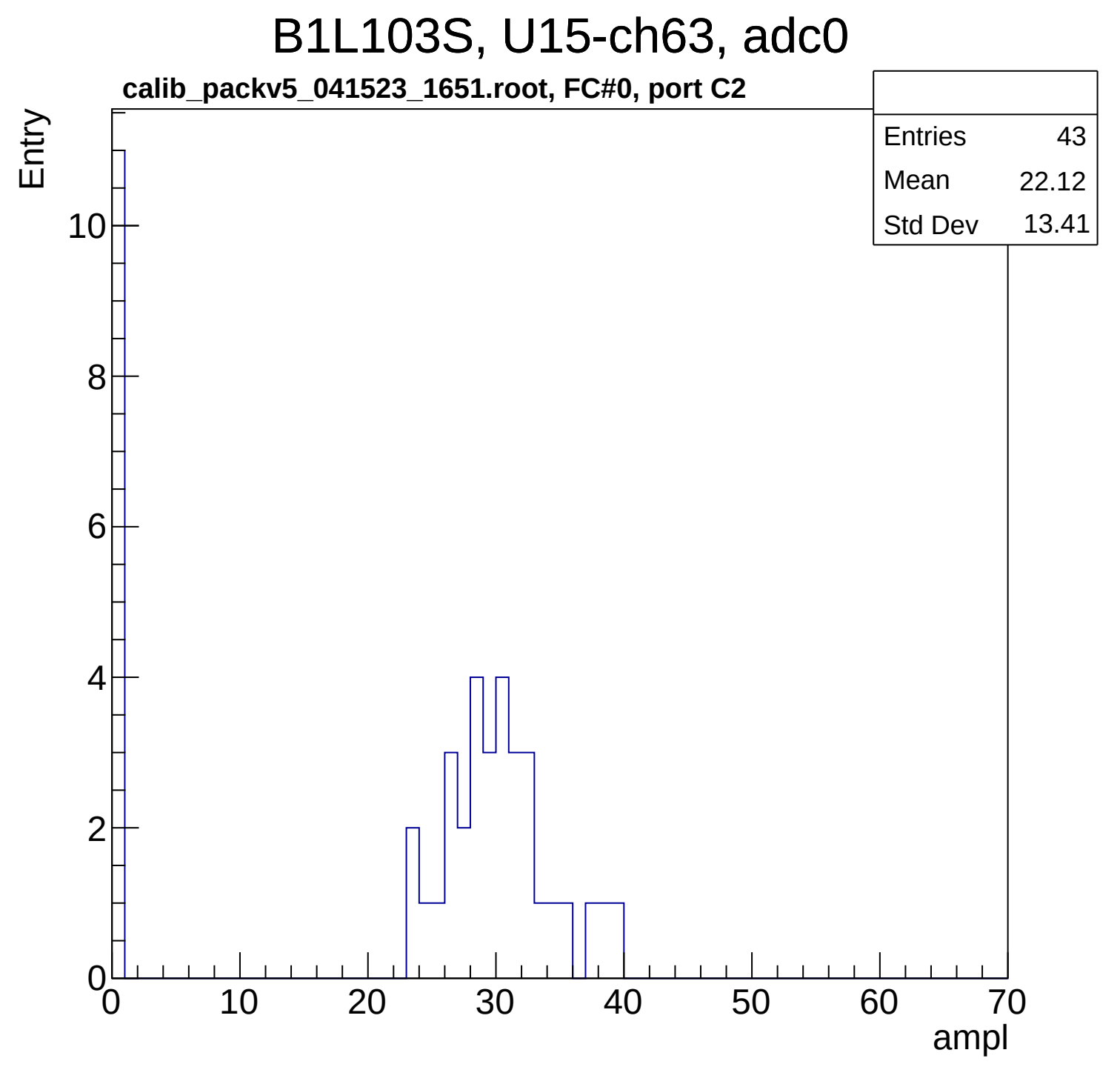
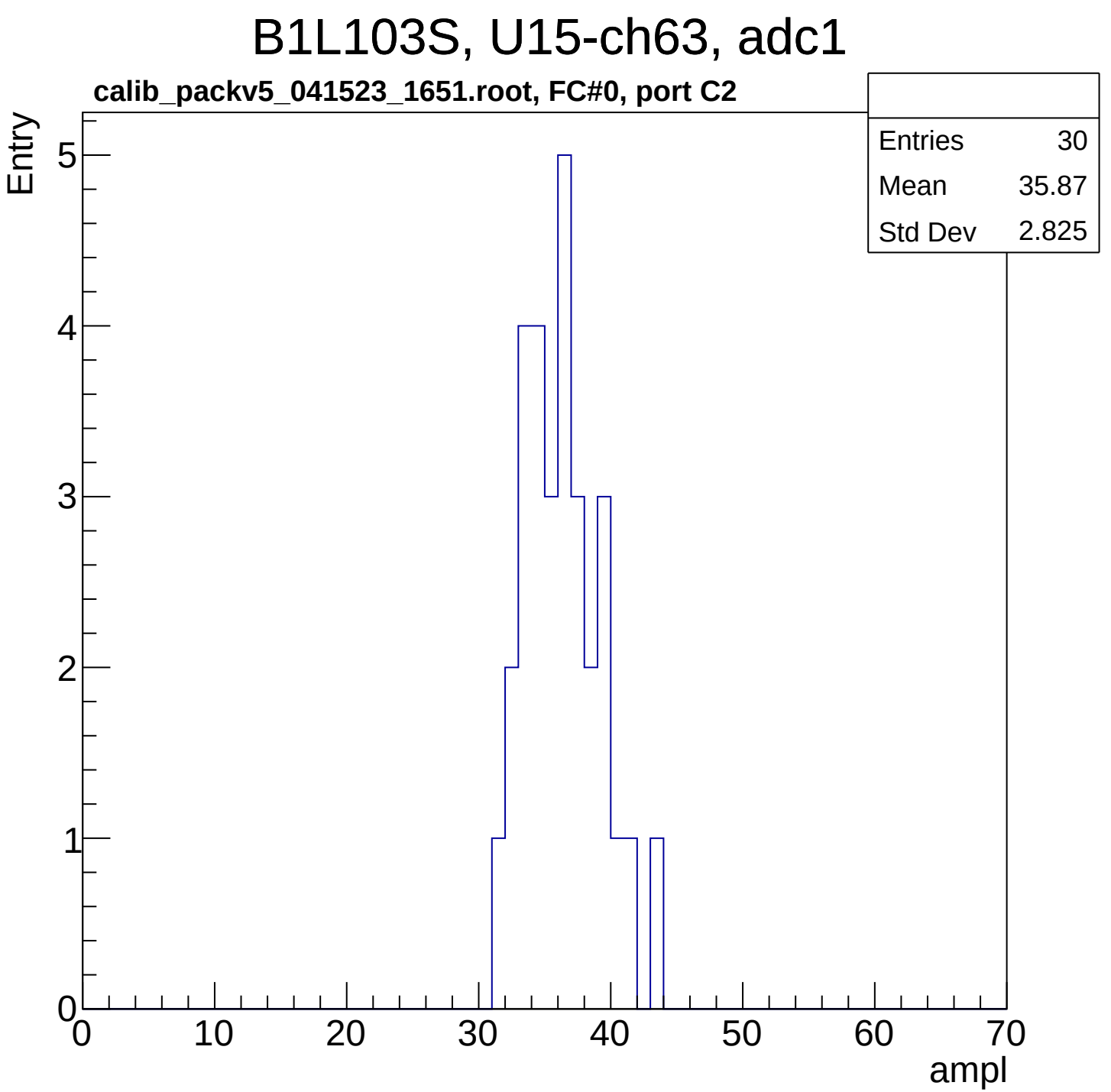
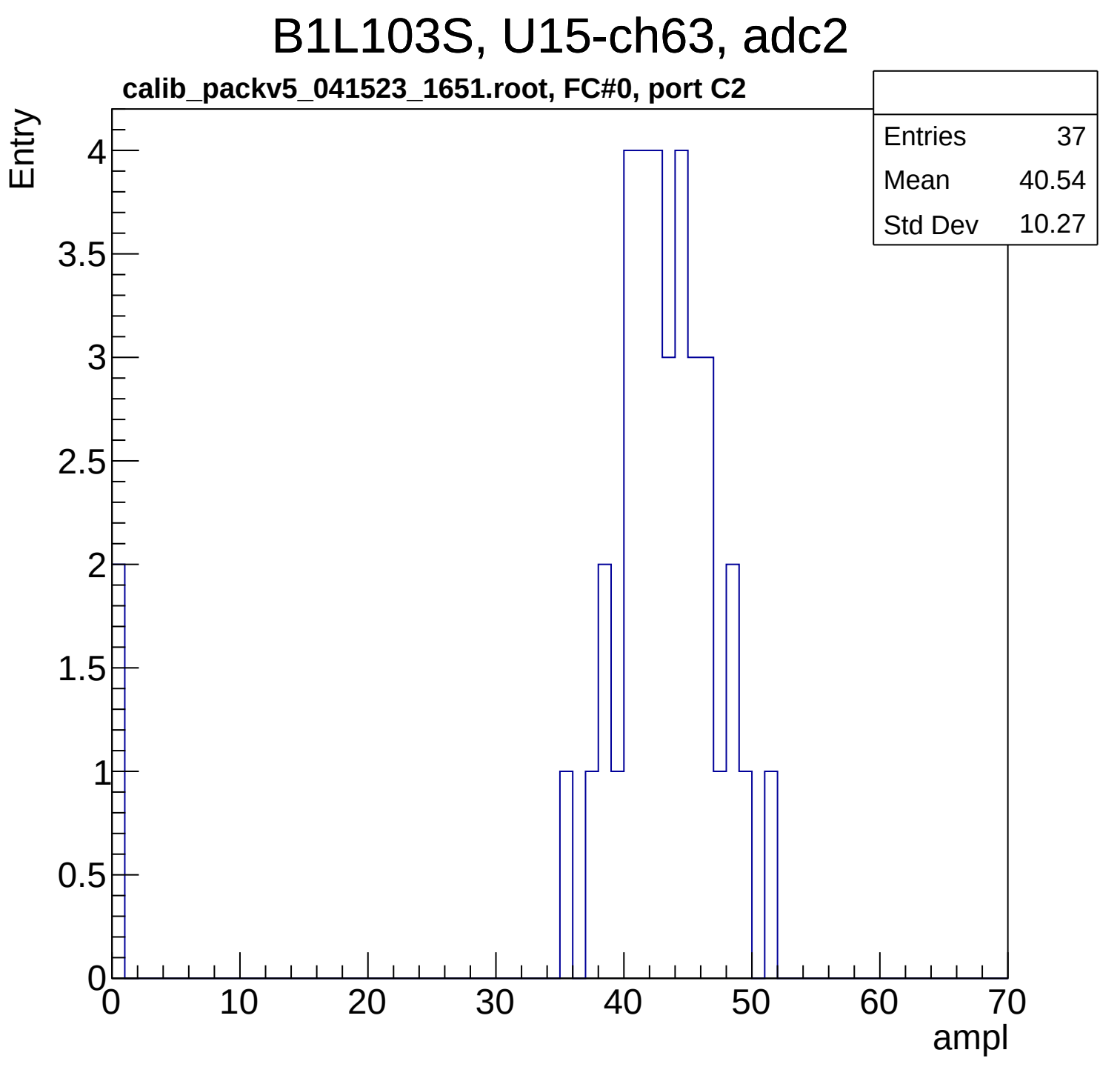
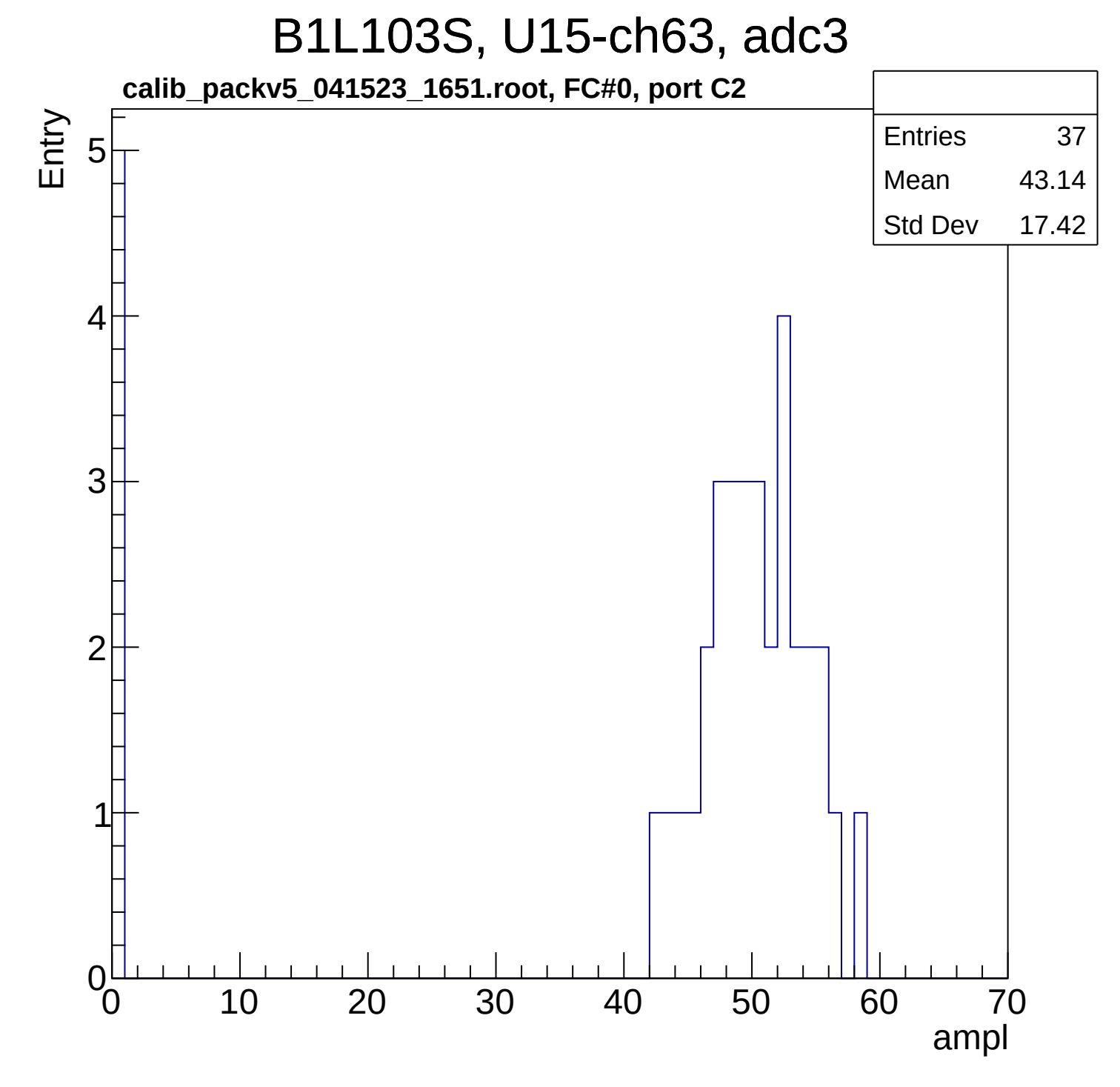
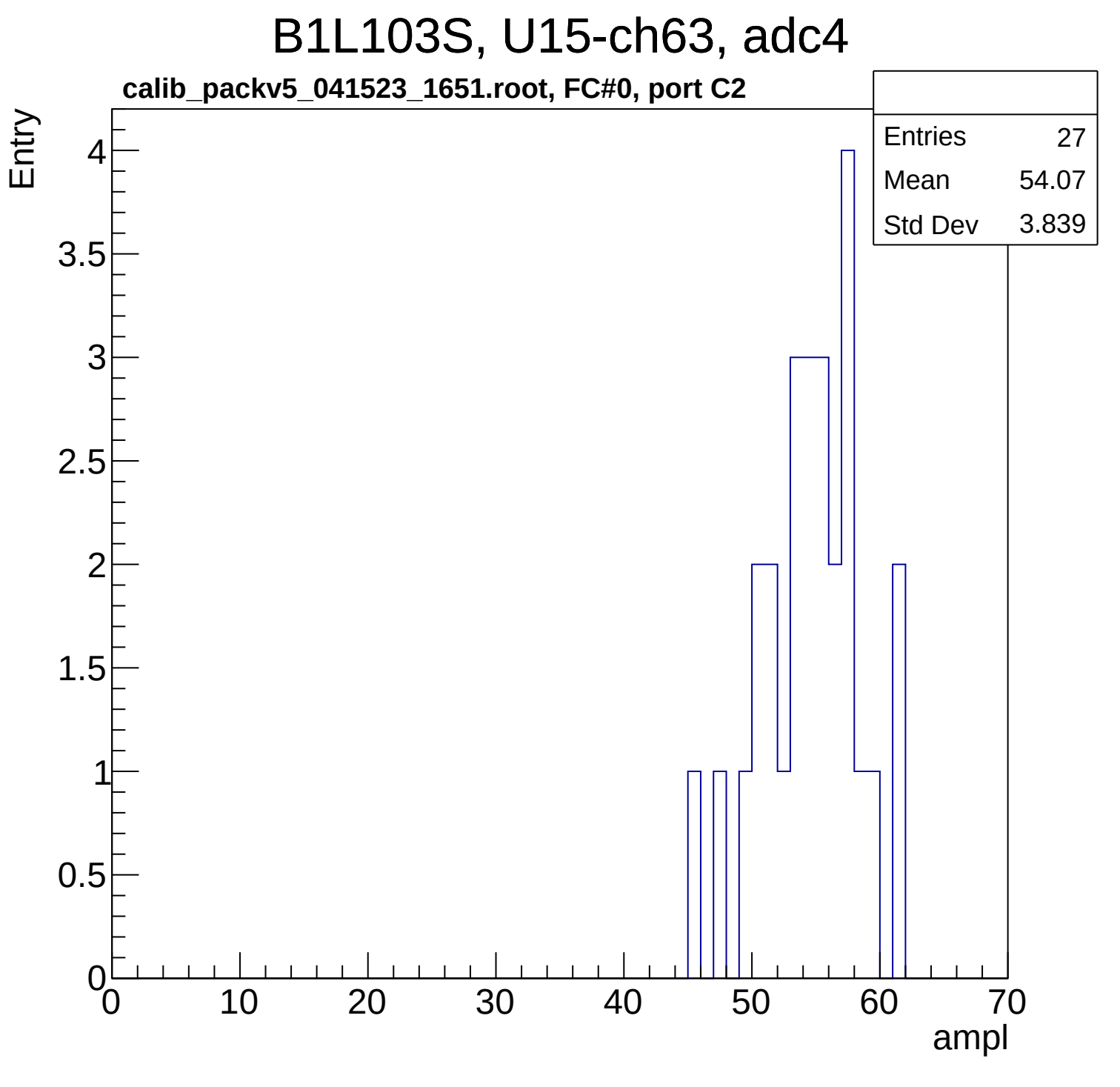
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch63, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 22.12
Std Dev 13.41
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch63, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 35.87
Std Dev 2.825
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch63, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 40.54
Std Dev 10.27
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch63, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 43.14
Std Dev 17.42
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch63, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 54.07
Std Dev 3.839
Entry
ampl
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0.5
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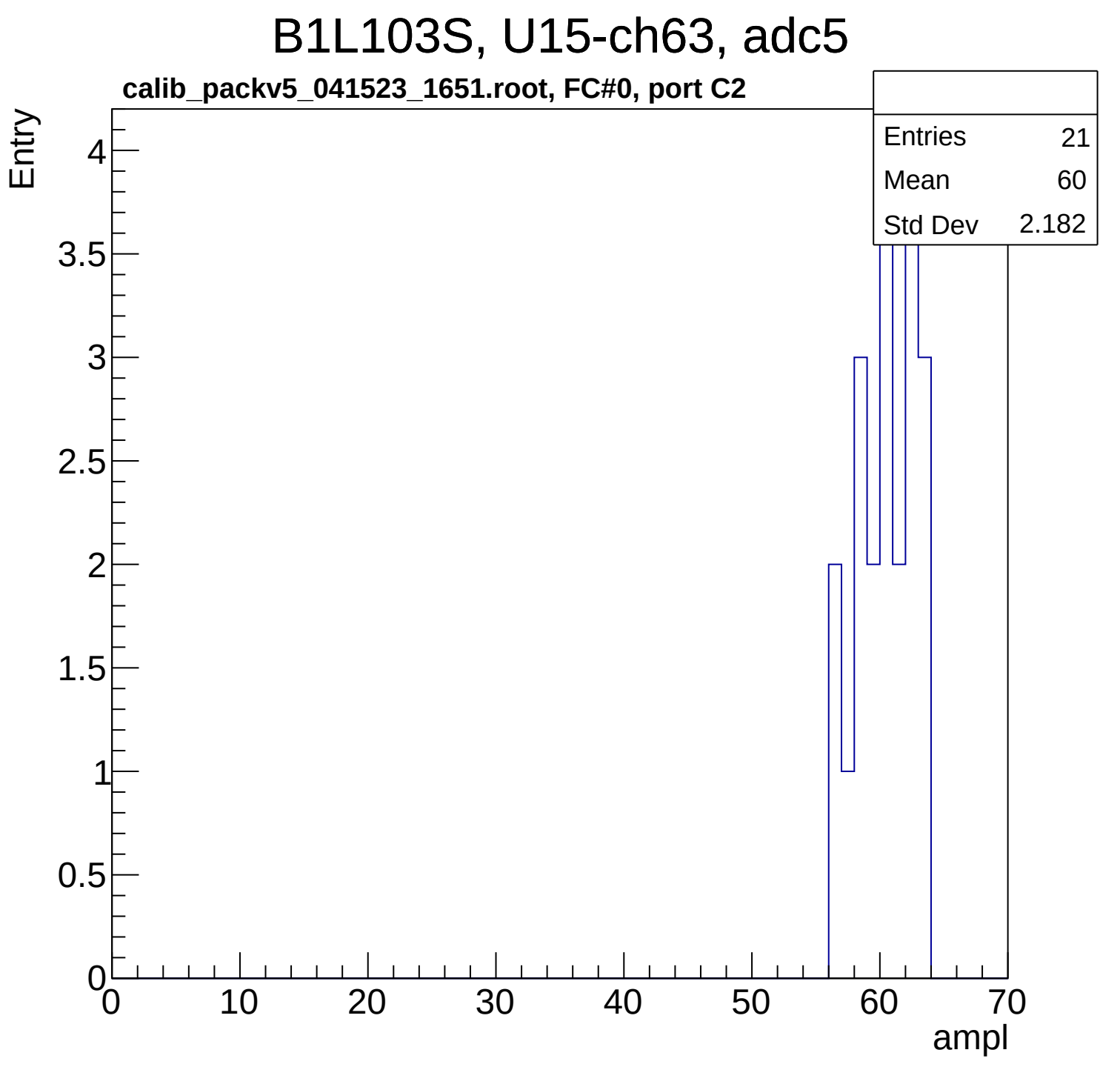
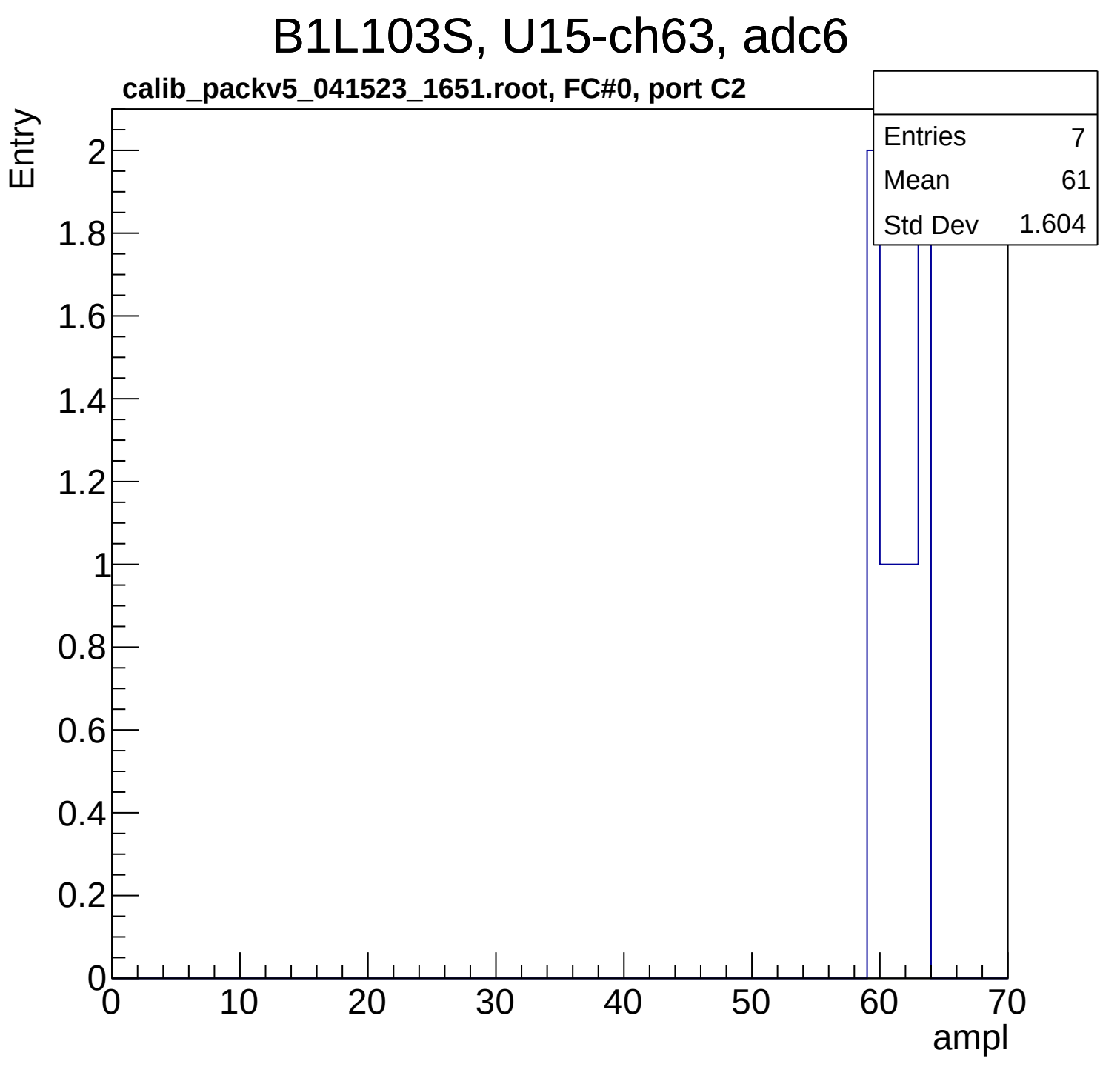
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch63, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 60
Std Dev 2.182
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch63, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61
Std Dev 1.604
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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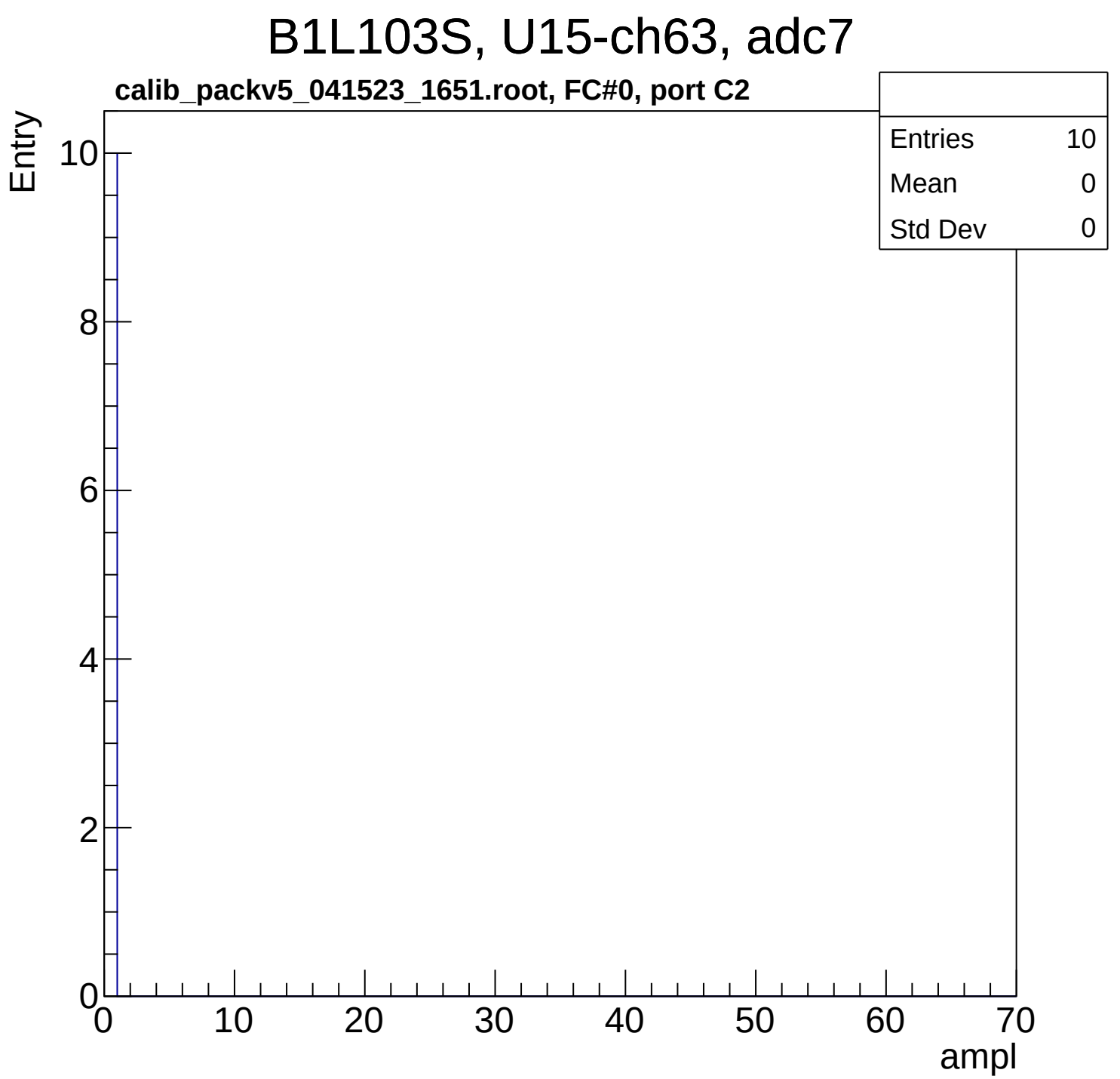
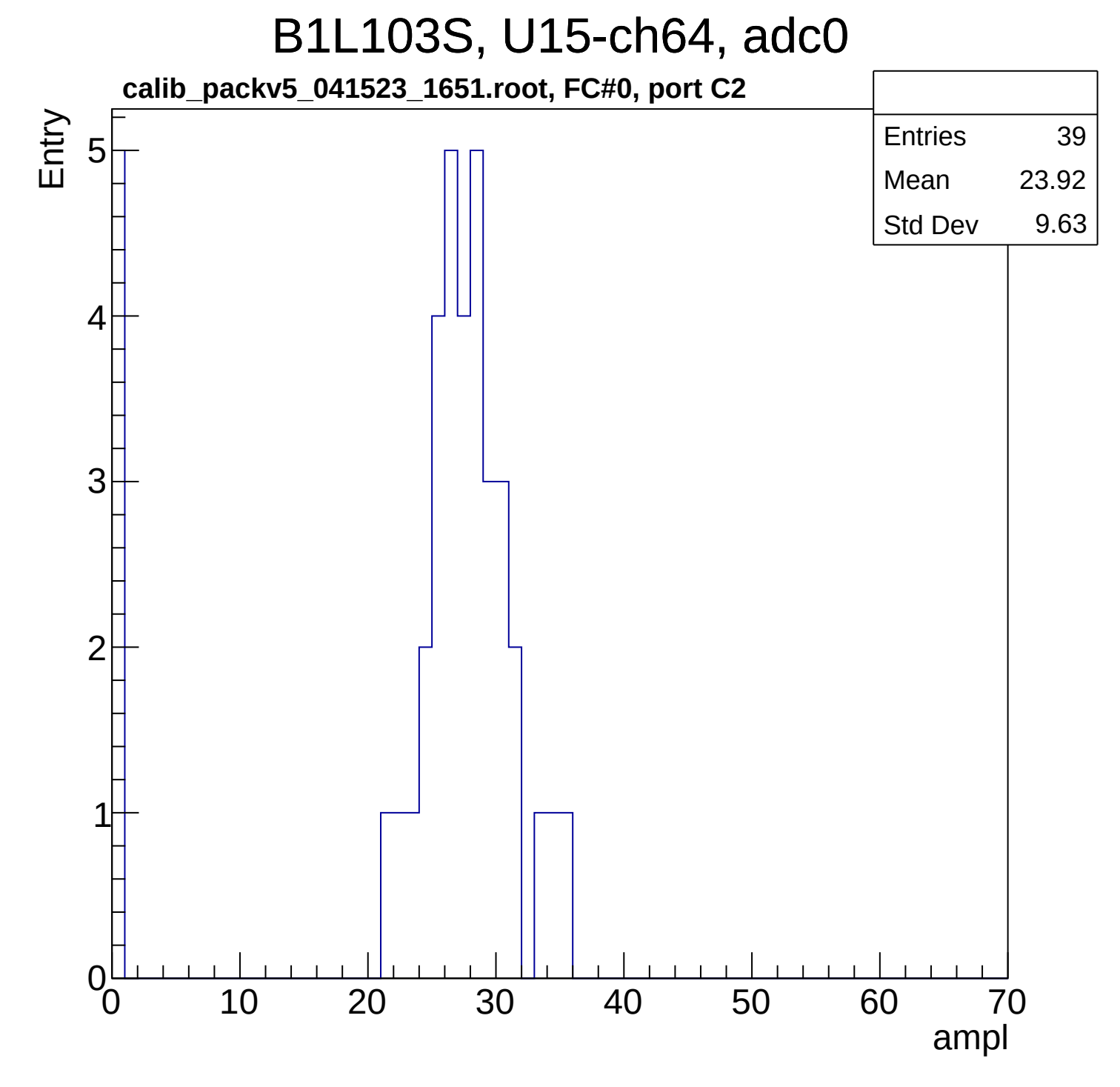
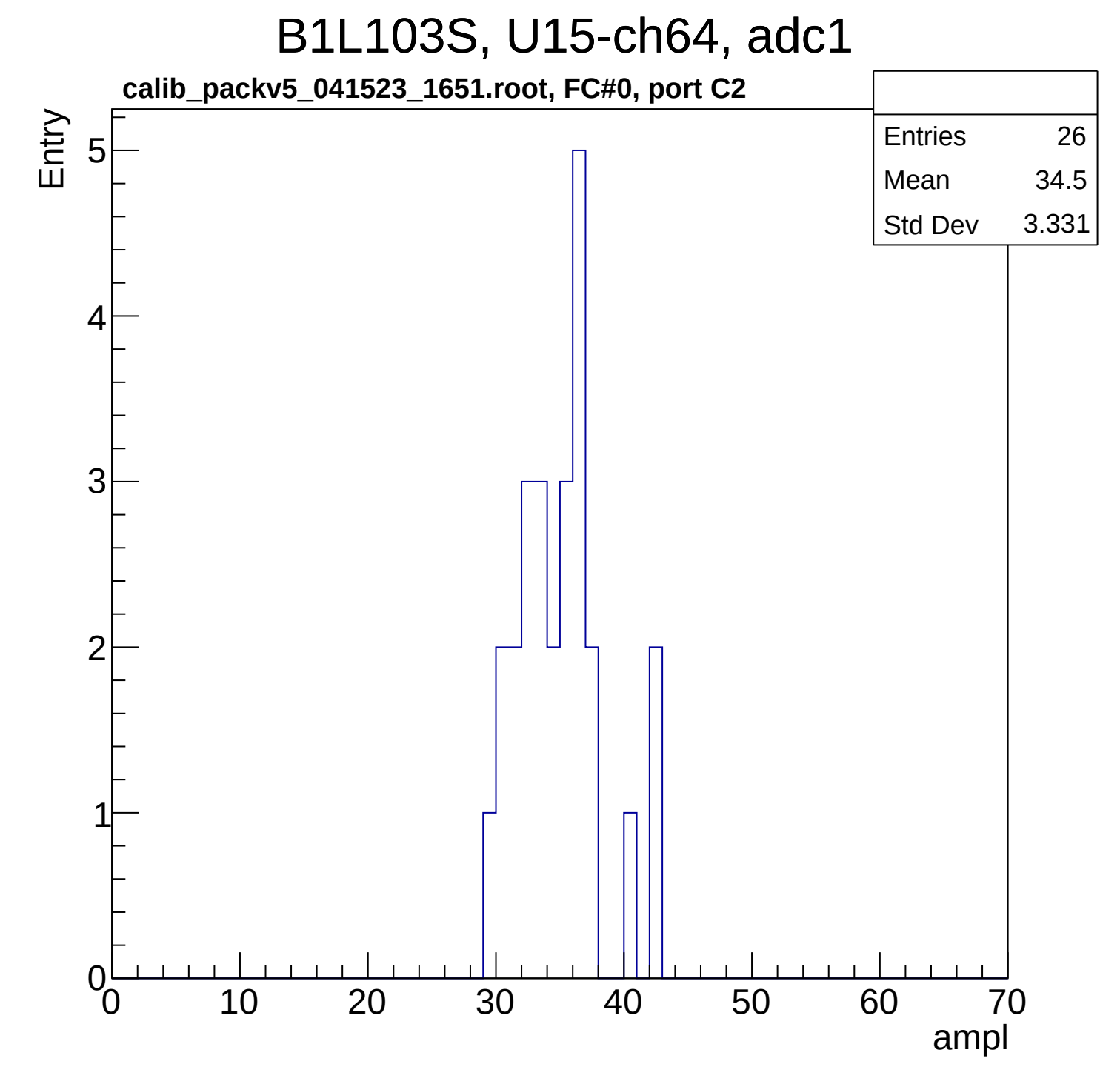
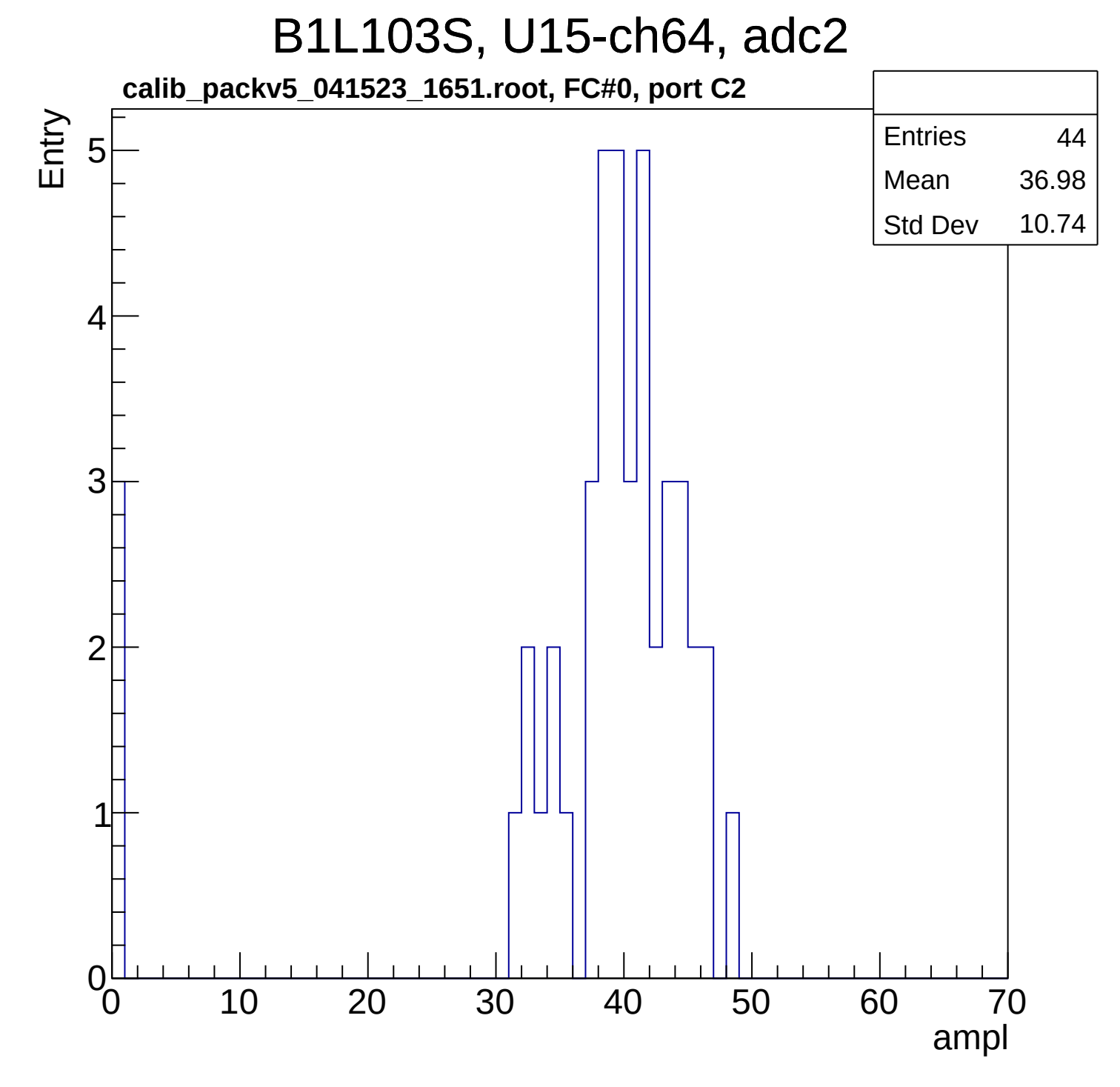
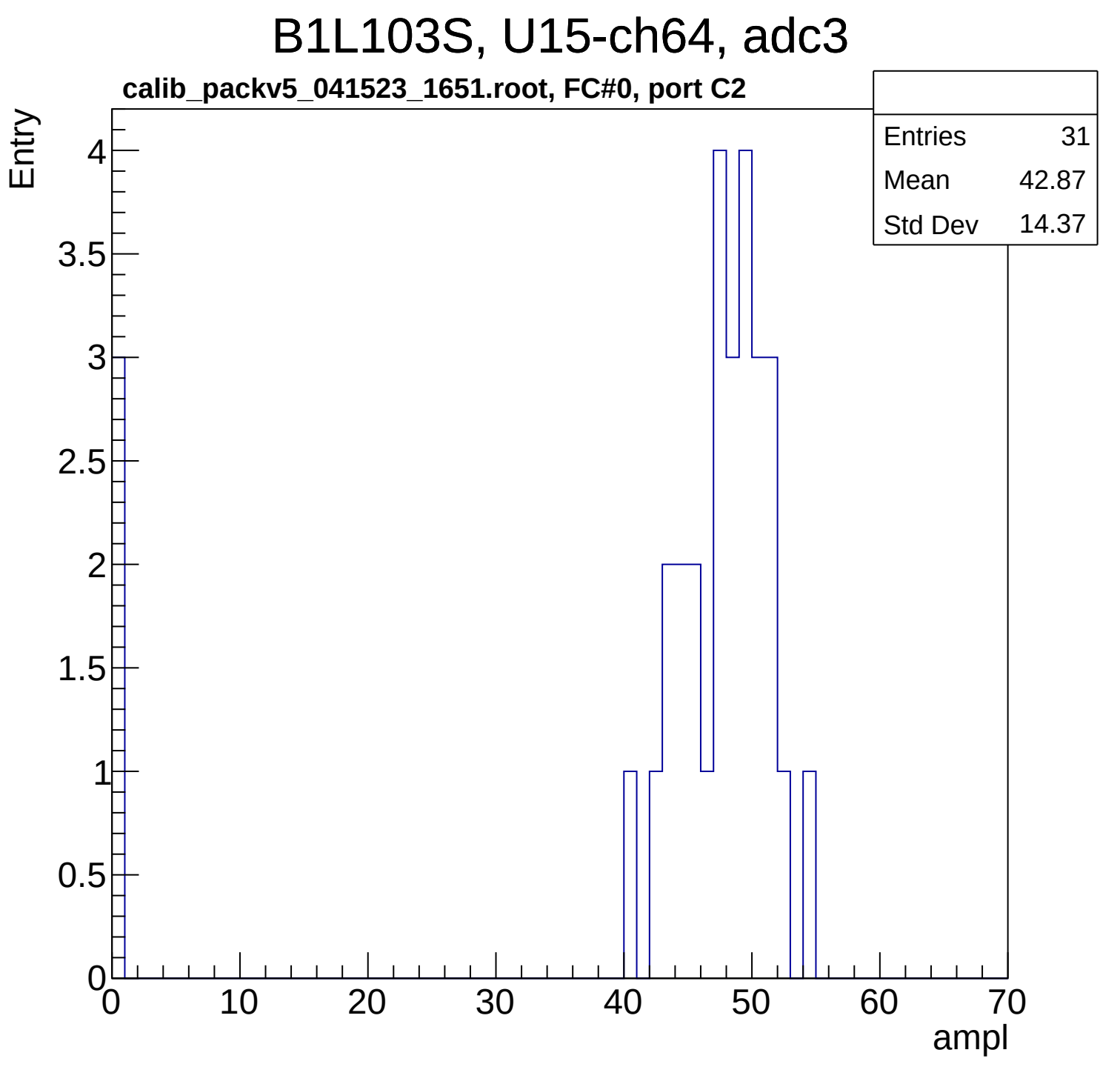
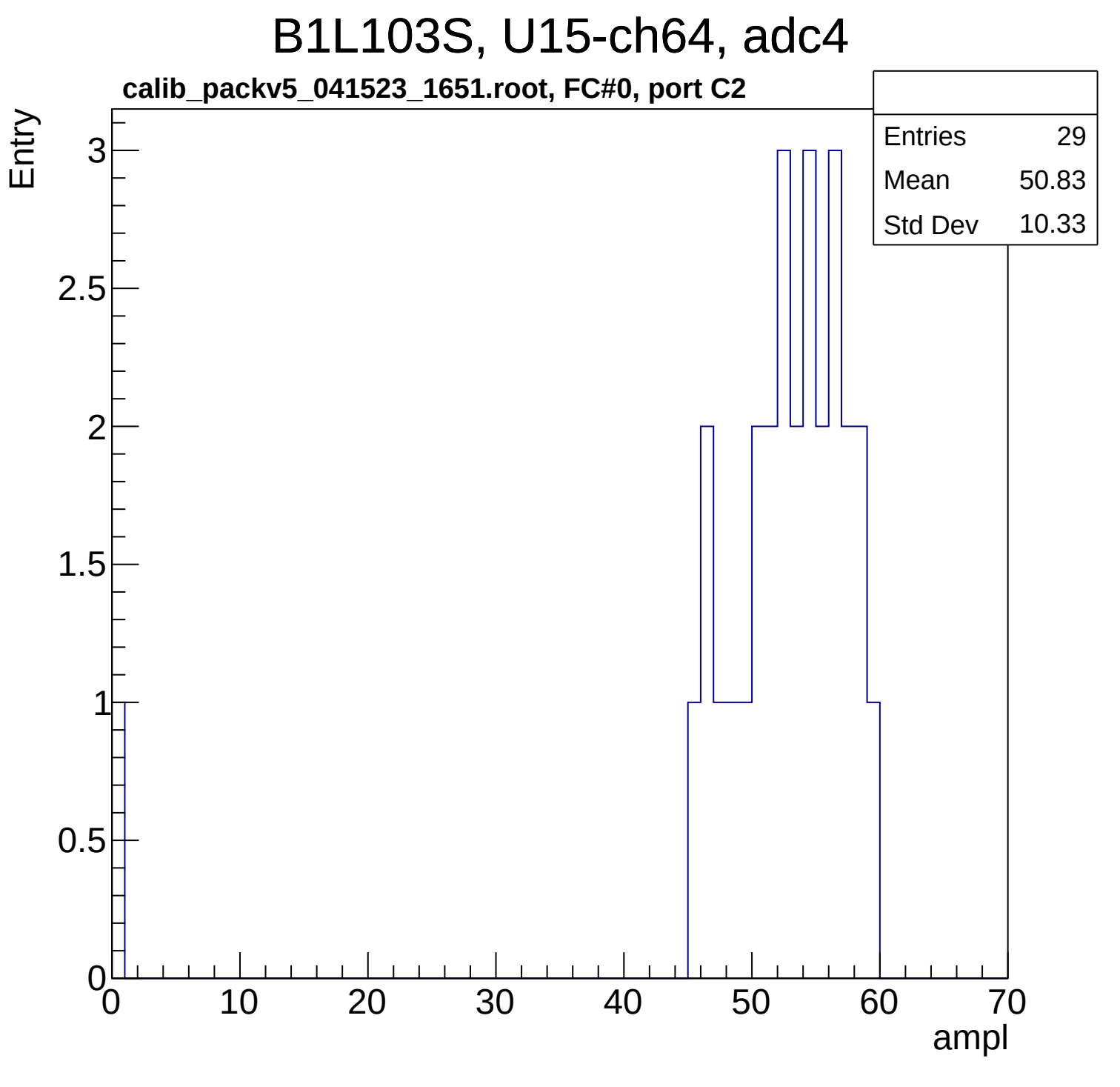

B1L103S, U15-ch63, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

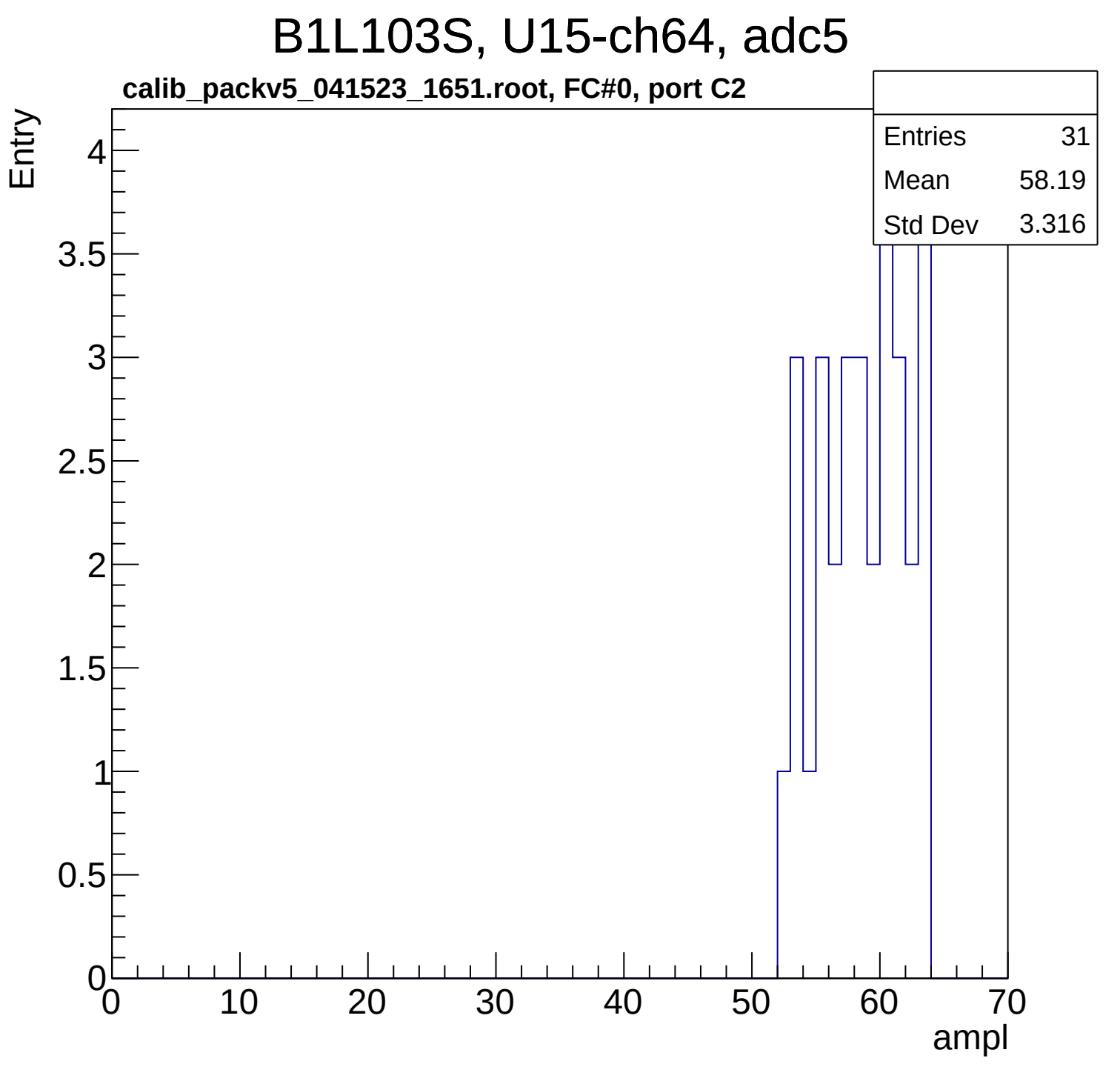

B1L103S, U15-ch64, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 23.92
Std Dev 9.63
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

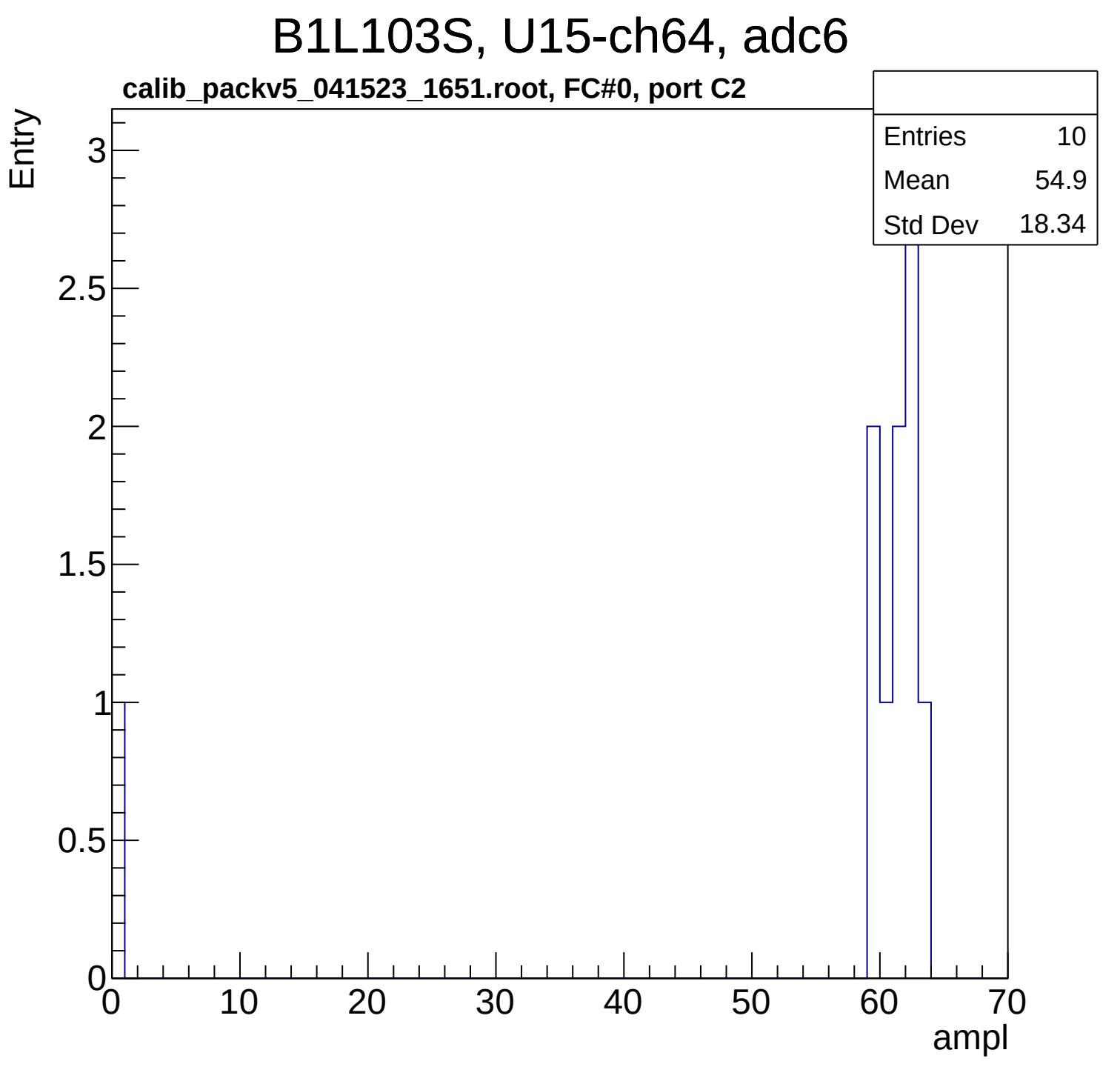

B1L103S, U15-ch64, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 34.5
Std Dev 3.331
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

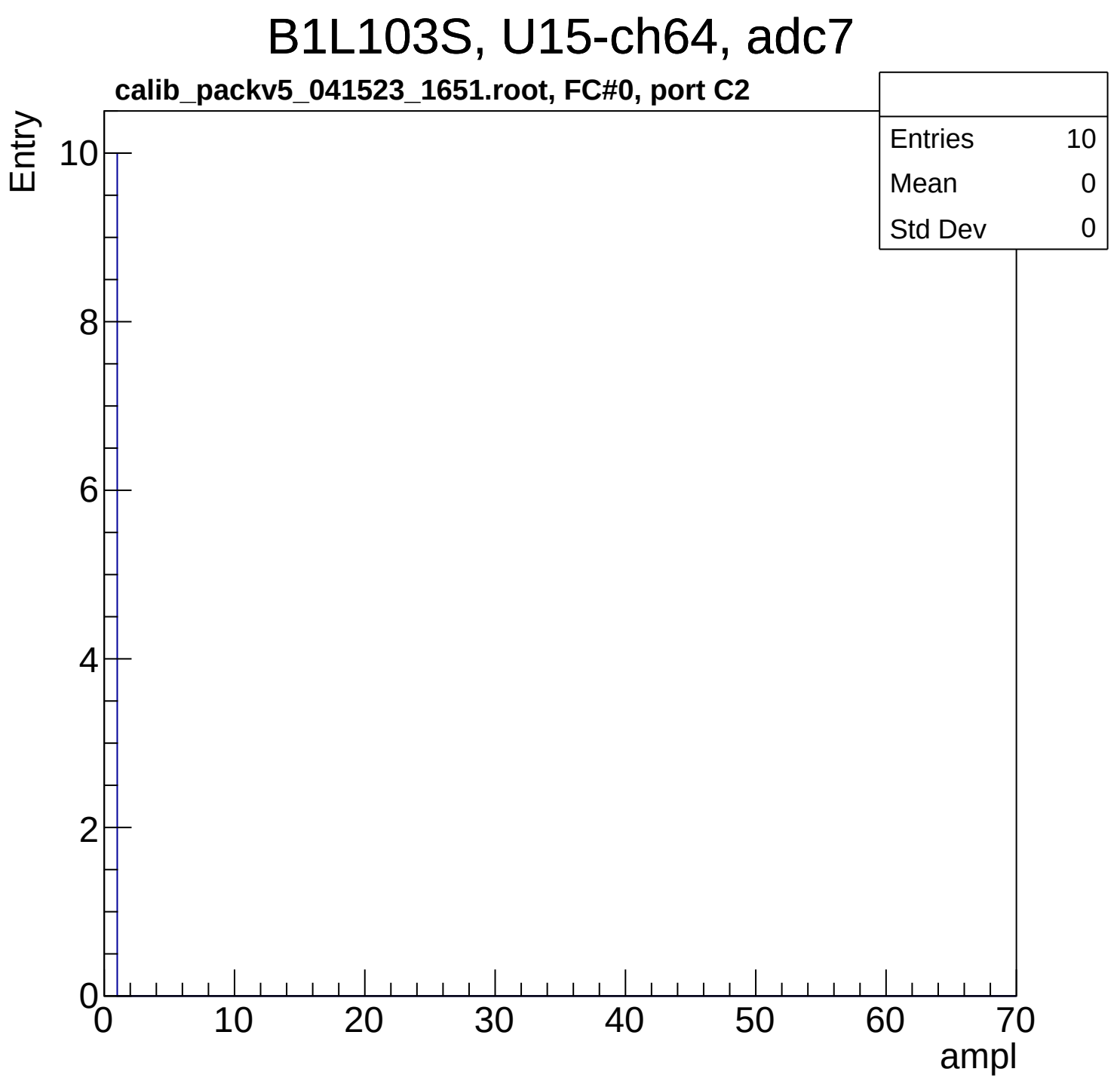

B1L103S, U15-ch64, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 36.98
Std Dev 10.74
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

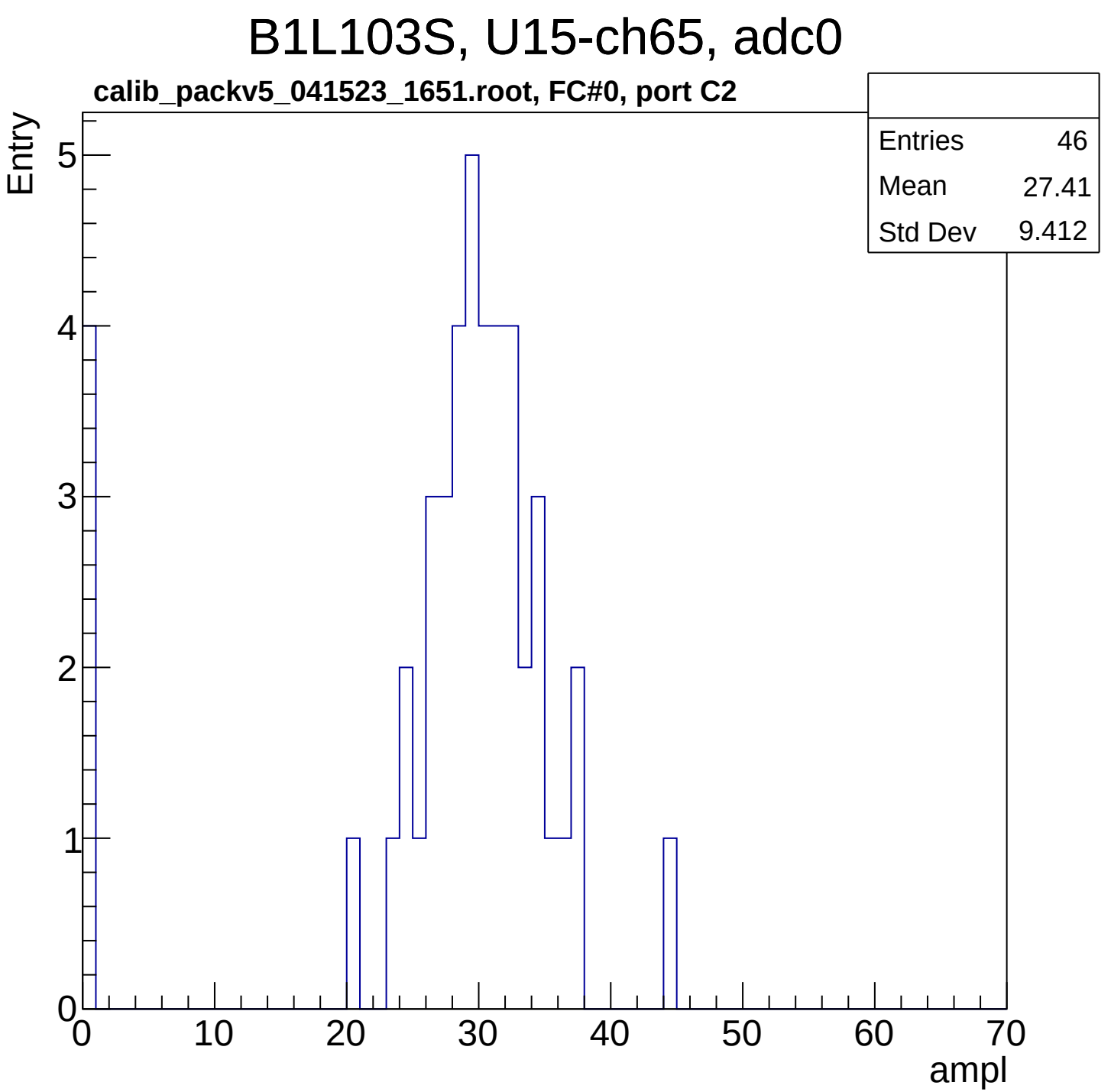

B1L103S, U15-ch64, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 42.87
Std Dev 14.37
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

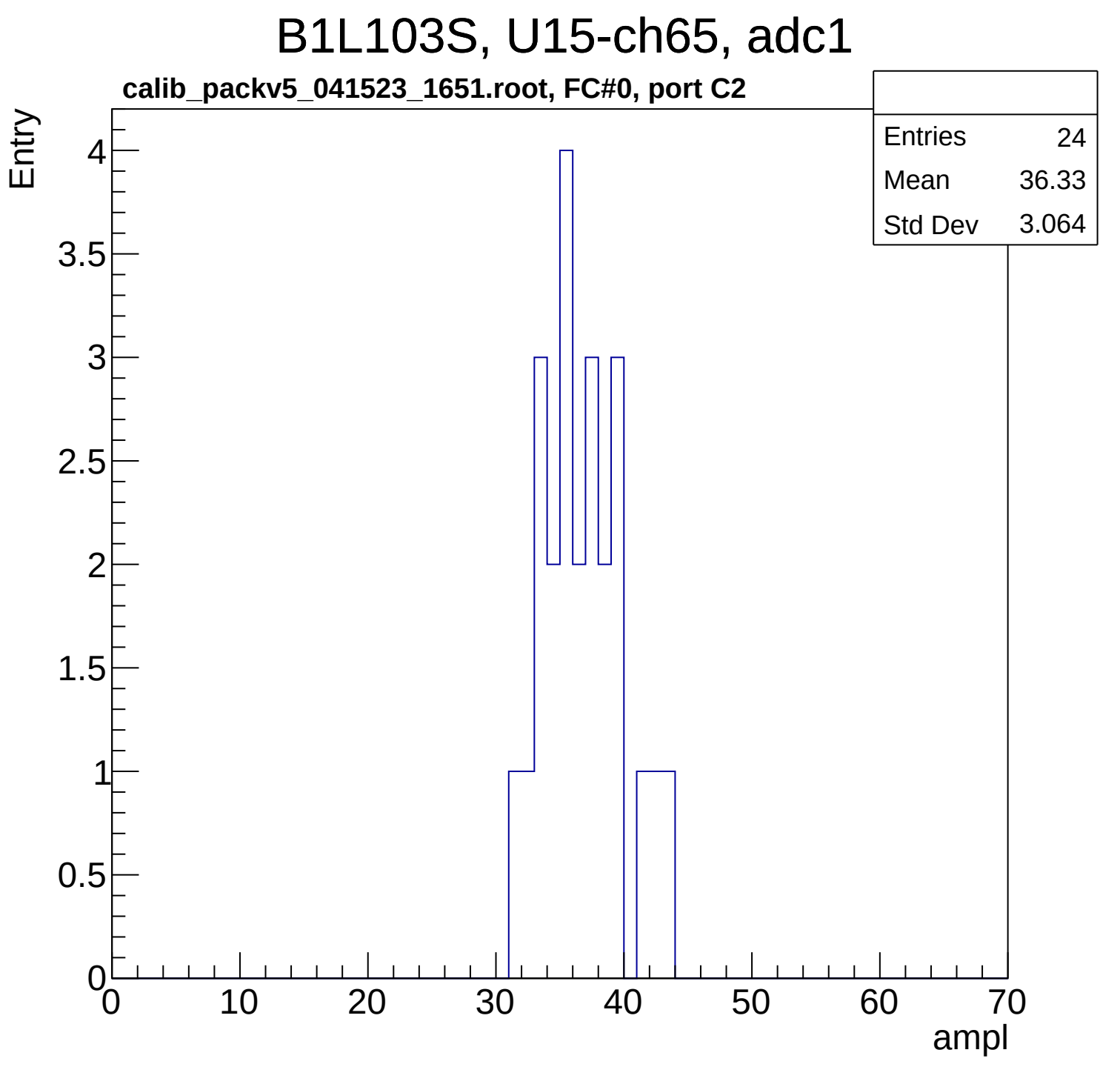

B1L103S, U15-ch64, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 50.83
Std Dev 10.33
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

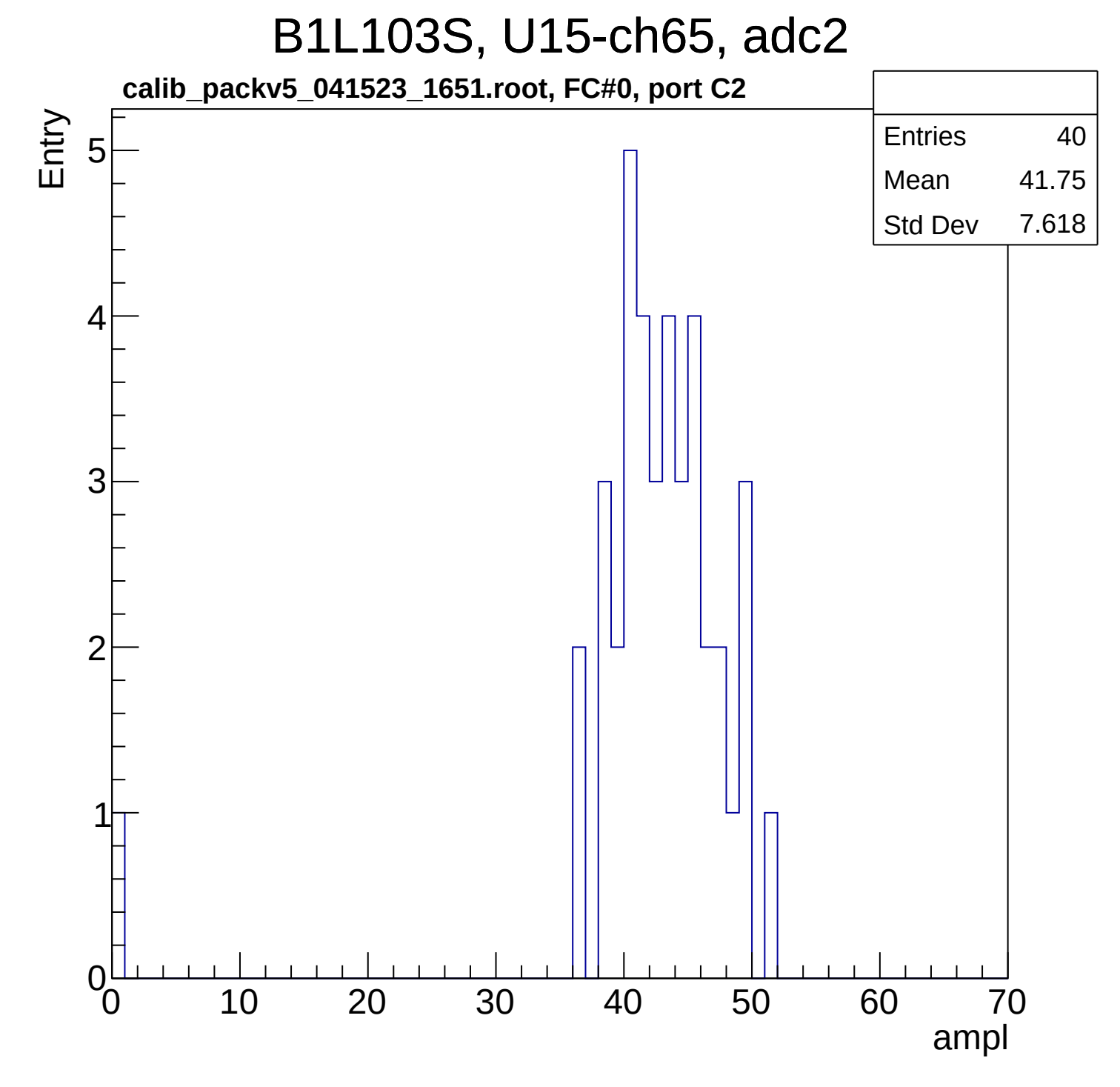

B1L103S, U15-ch64, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 58.19
Std Dev 3.316
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

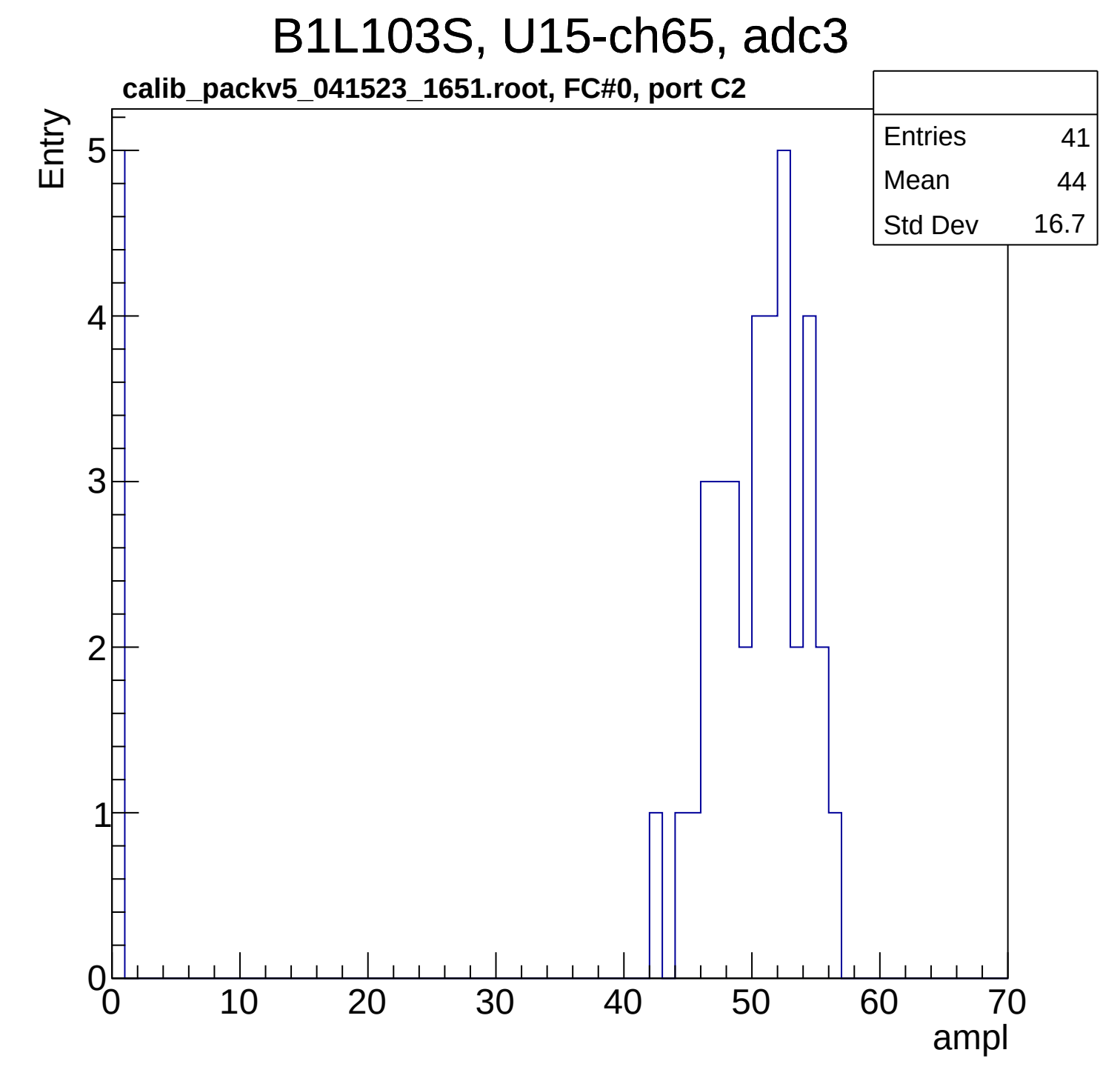

B1L103S, U15-ch64, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 54.9
Std Dev 18.34
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

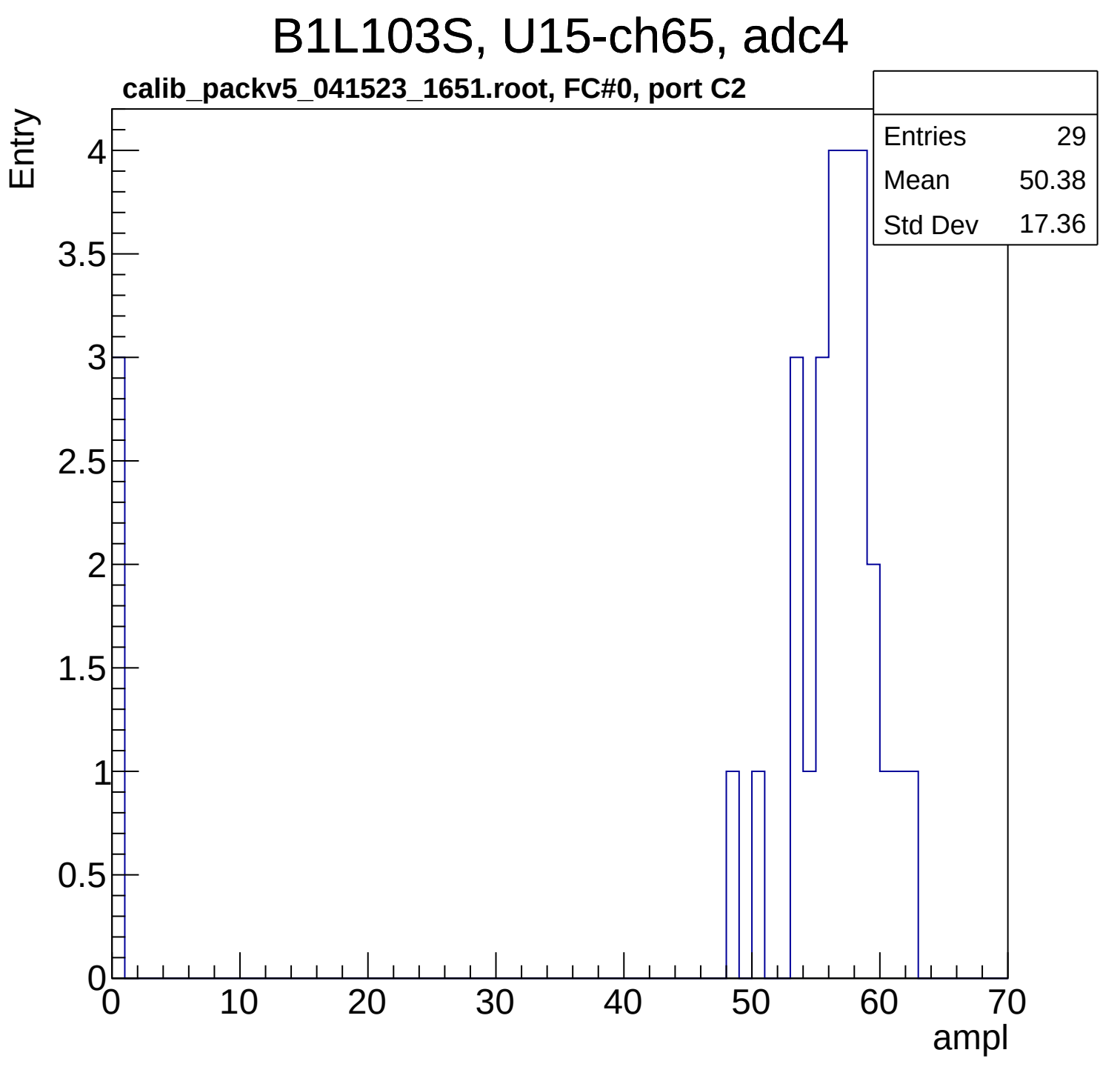

B1L103S, U15-ch64, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

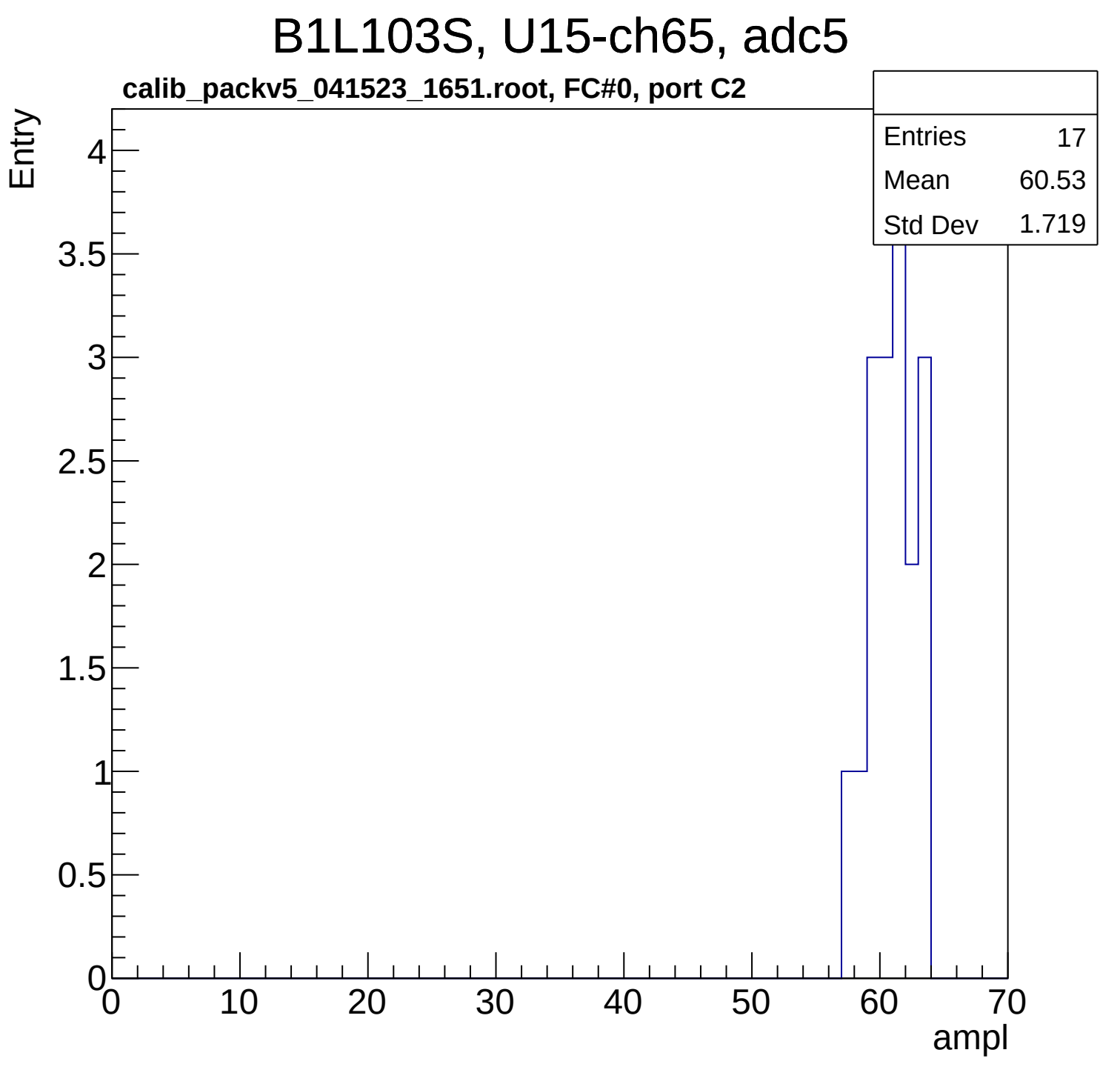

B1L103S, U15-ch65, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 27.41
Std Dev 9.412
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

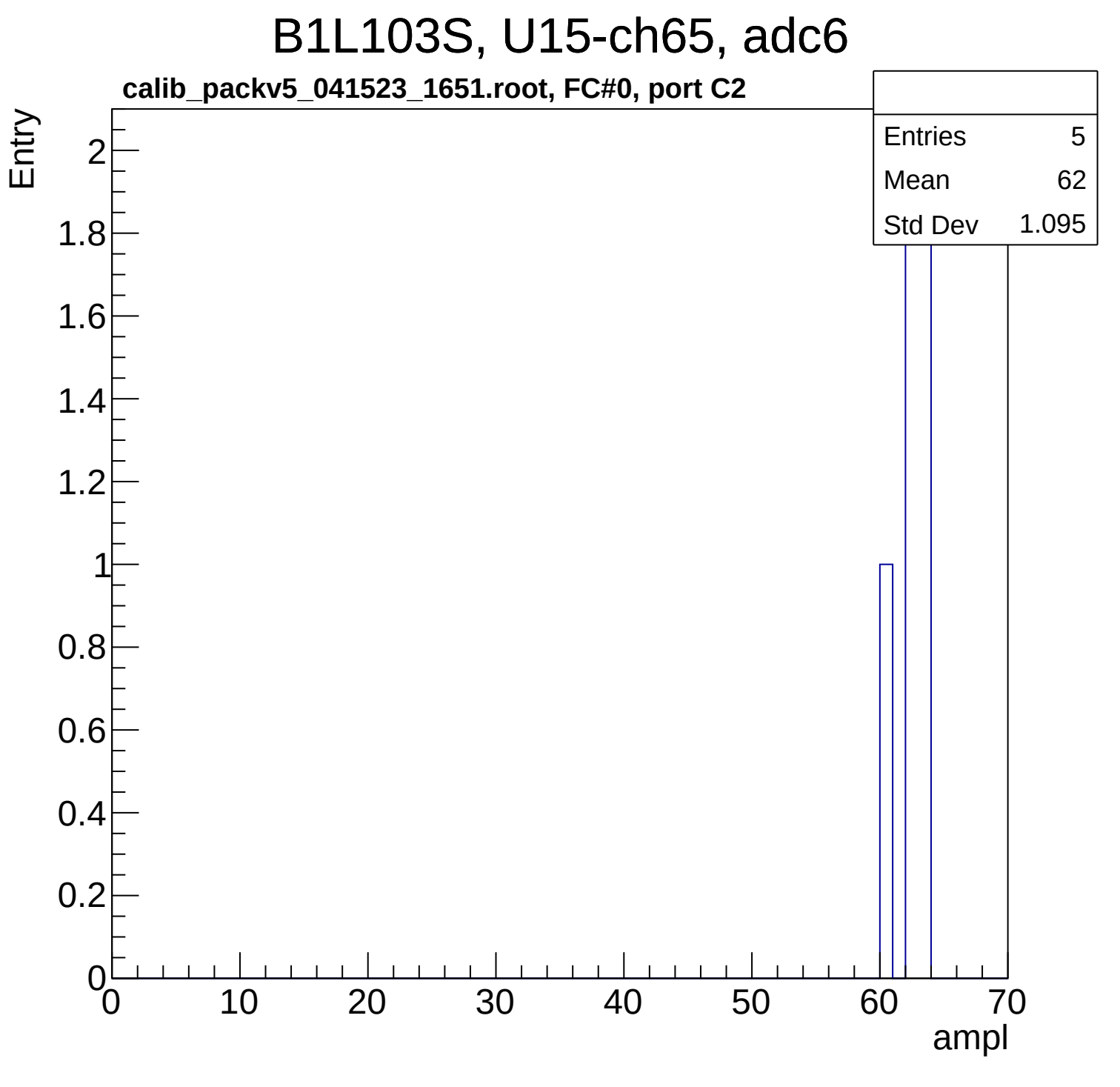

B1L103S, U15-ch65, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 36.33
Std Dev 3.064
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

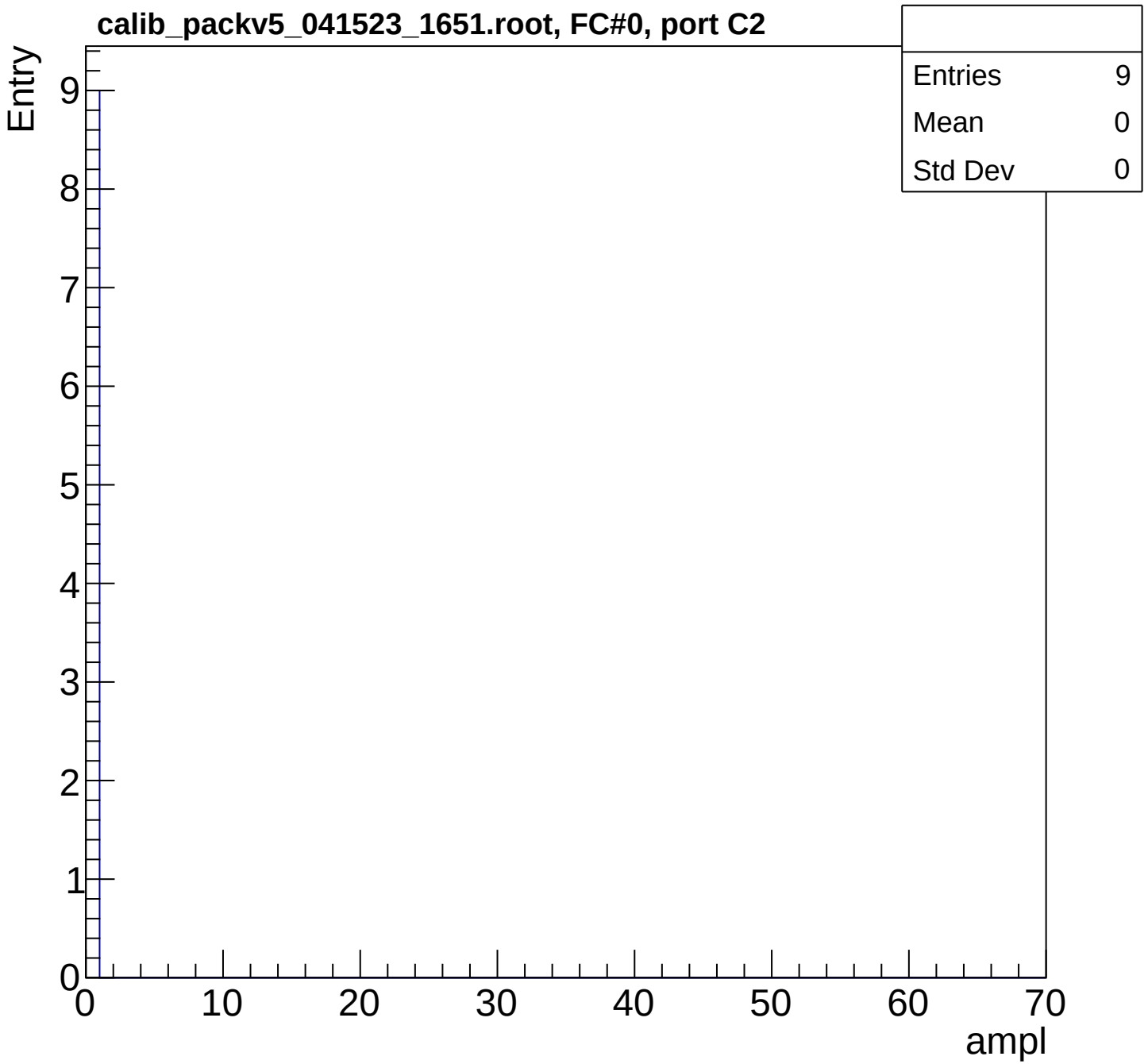

B1L103S, U15-ch65, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 41.75
Std Dev 7.618
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

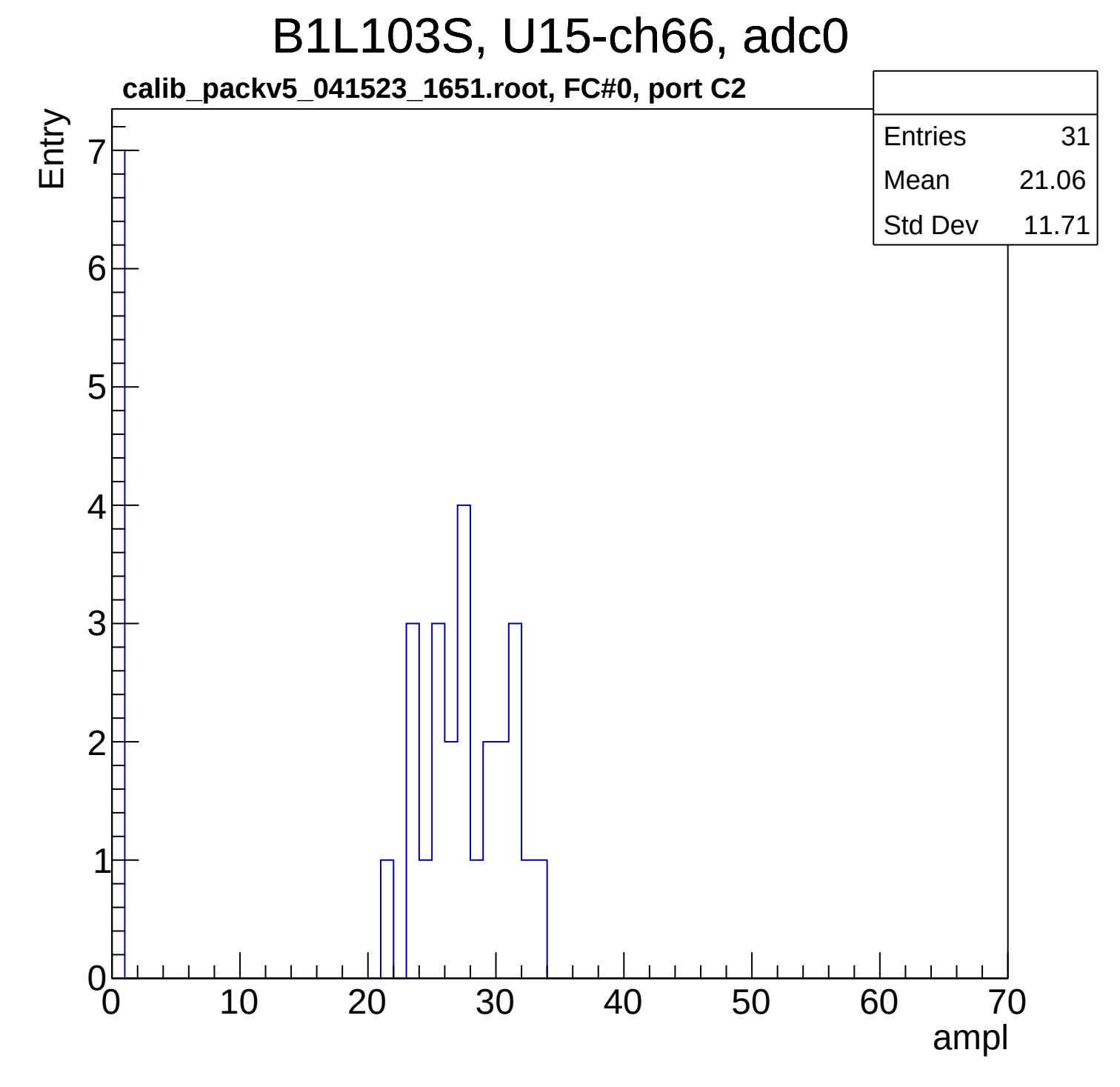

B1L103S, U15-ch65, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 44
Std Dev 16.7
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

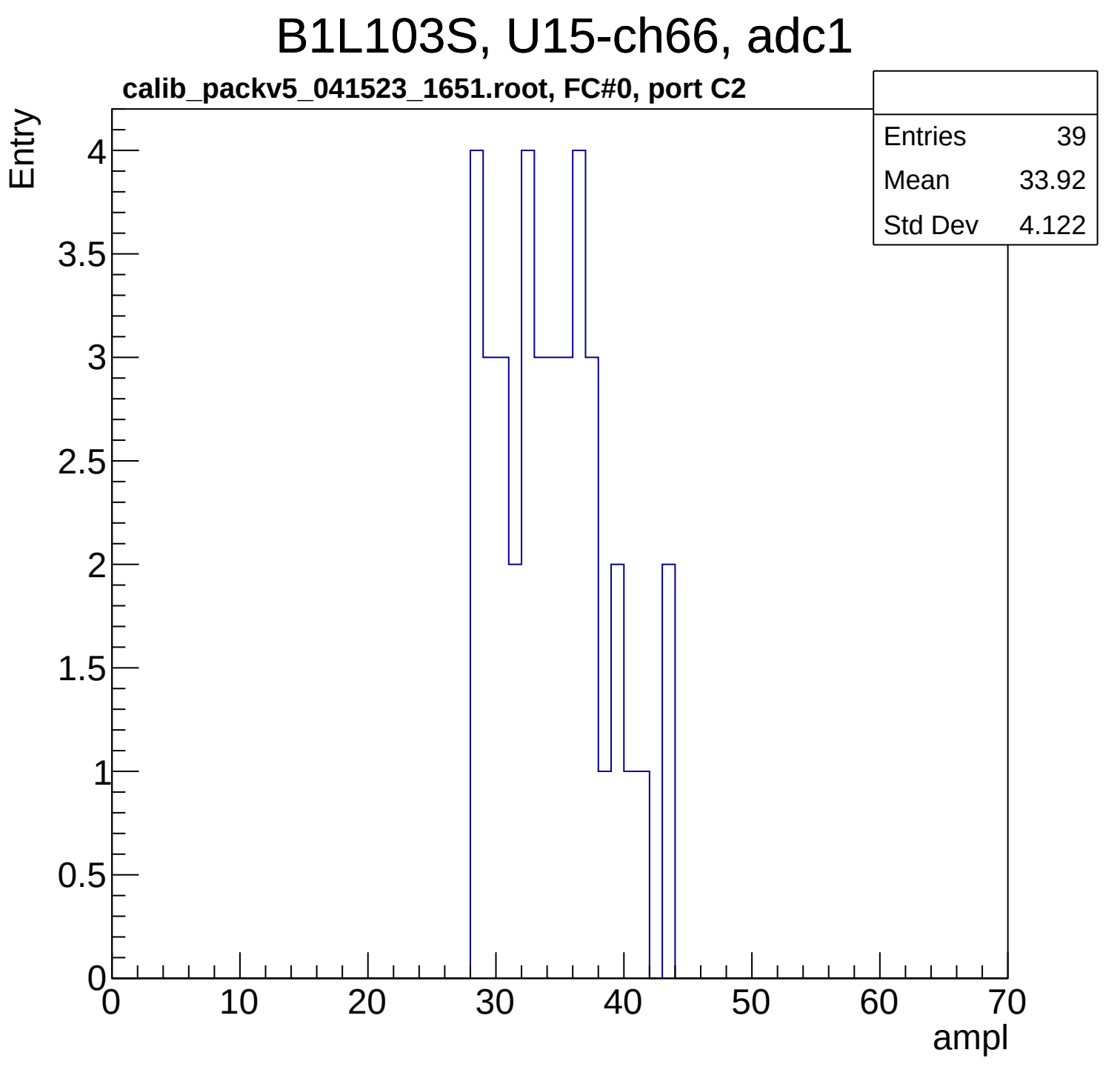

B1L103S, U15-ch65, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 50.38
Std Dev 17.36
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

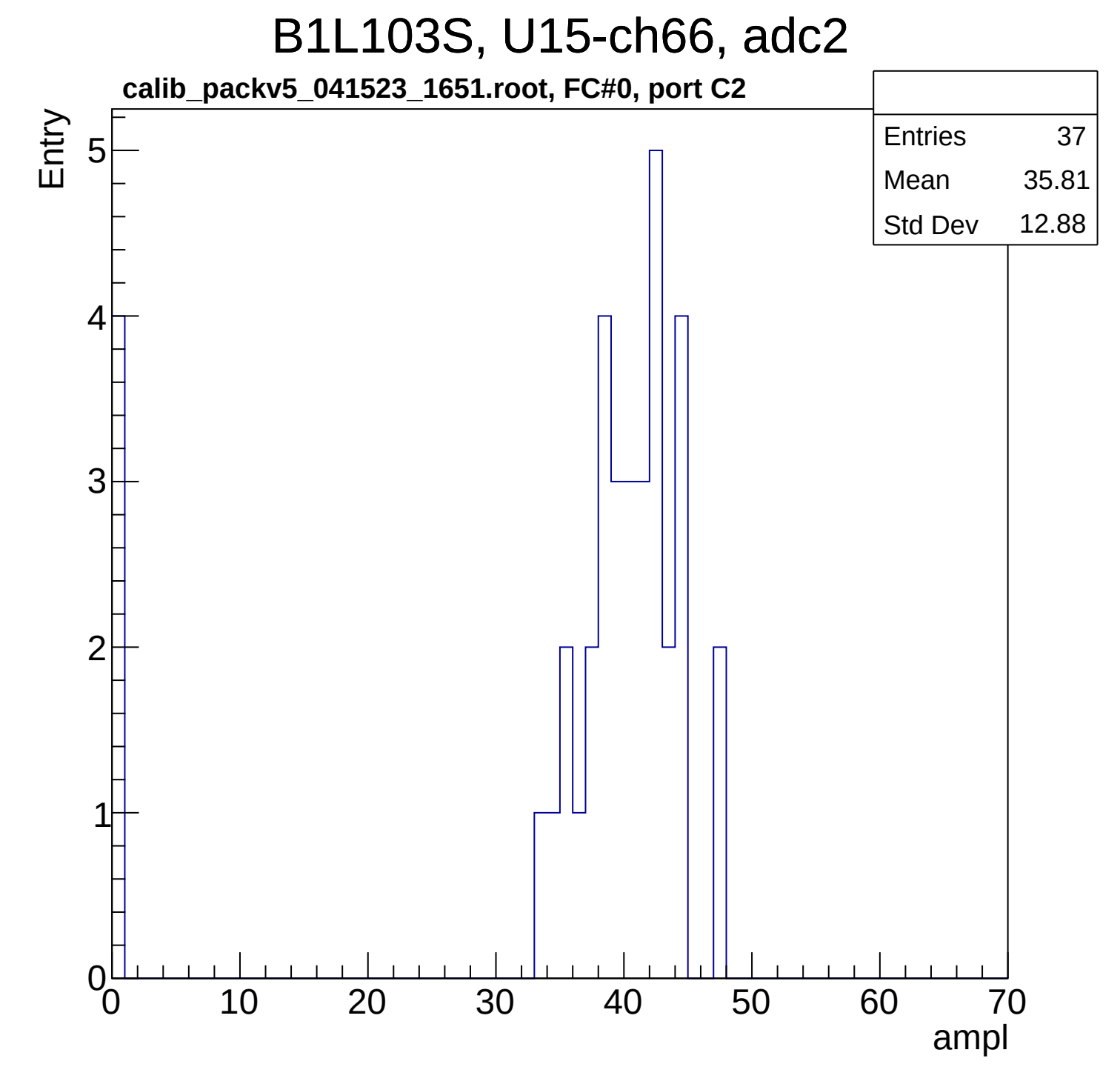

B1L103S, U15-ch65, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 60.53
Std Dev 1.719
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

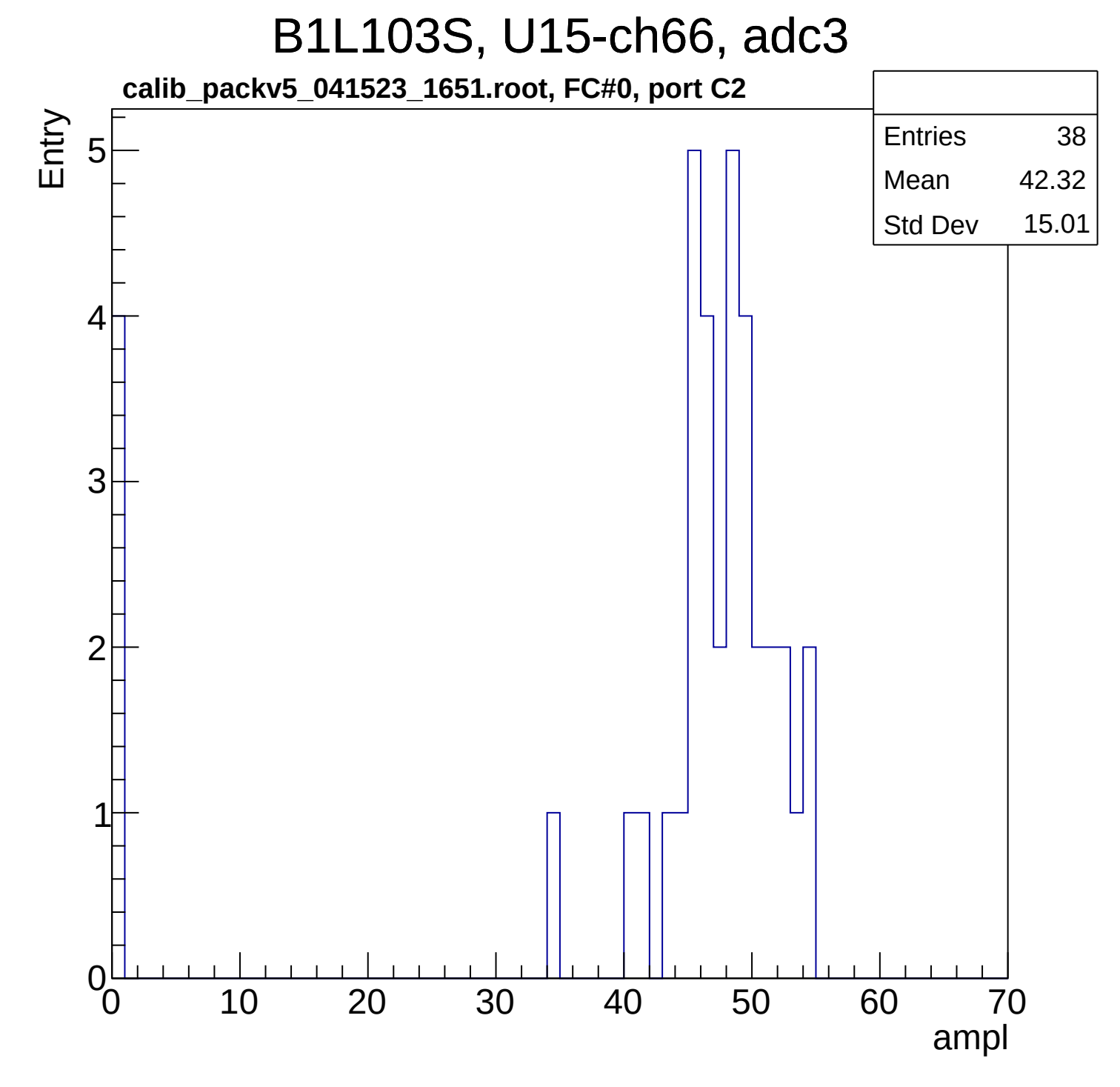

B1L103S, U15-ch65, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62
Std Dev 1.095
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

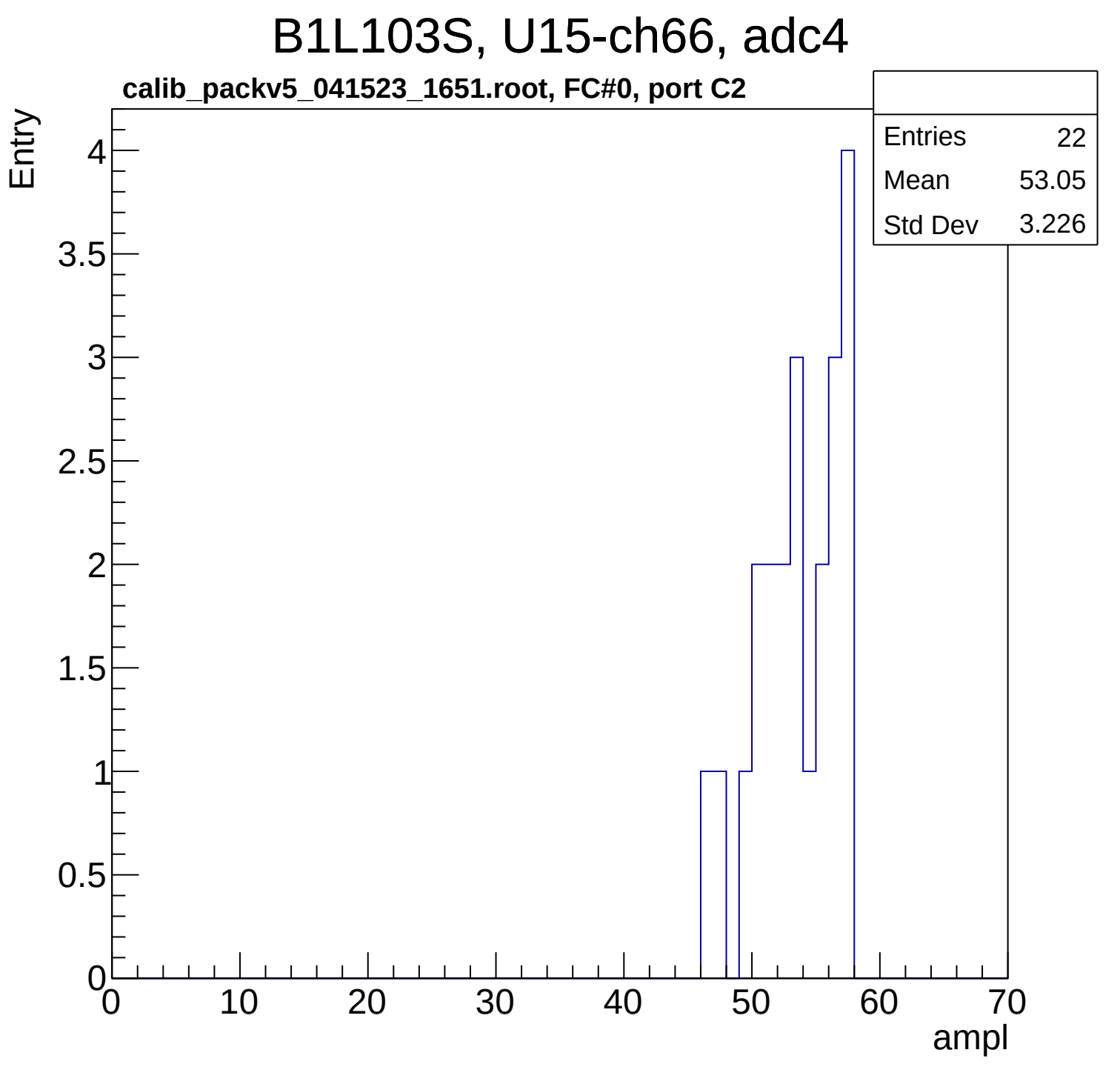

B1L103S, U15-ch65, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 0
Std Dev 0
Entry
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70
ampl

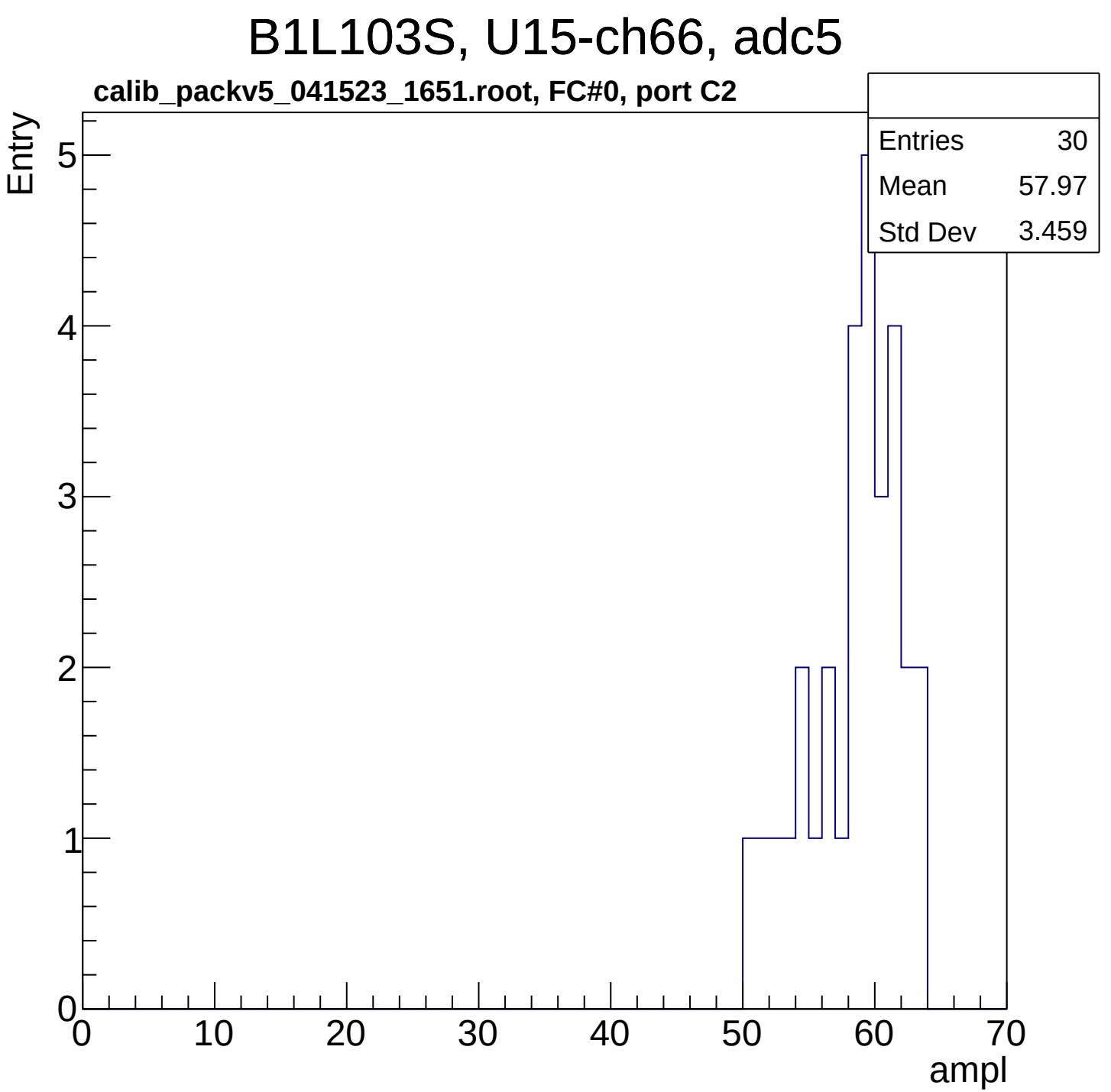

B1L103S, U15-ch66, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 21.06
Std Dev 11.71
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

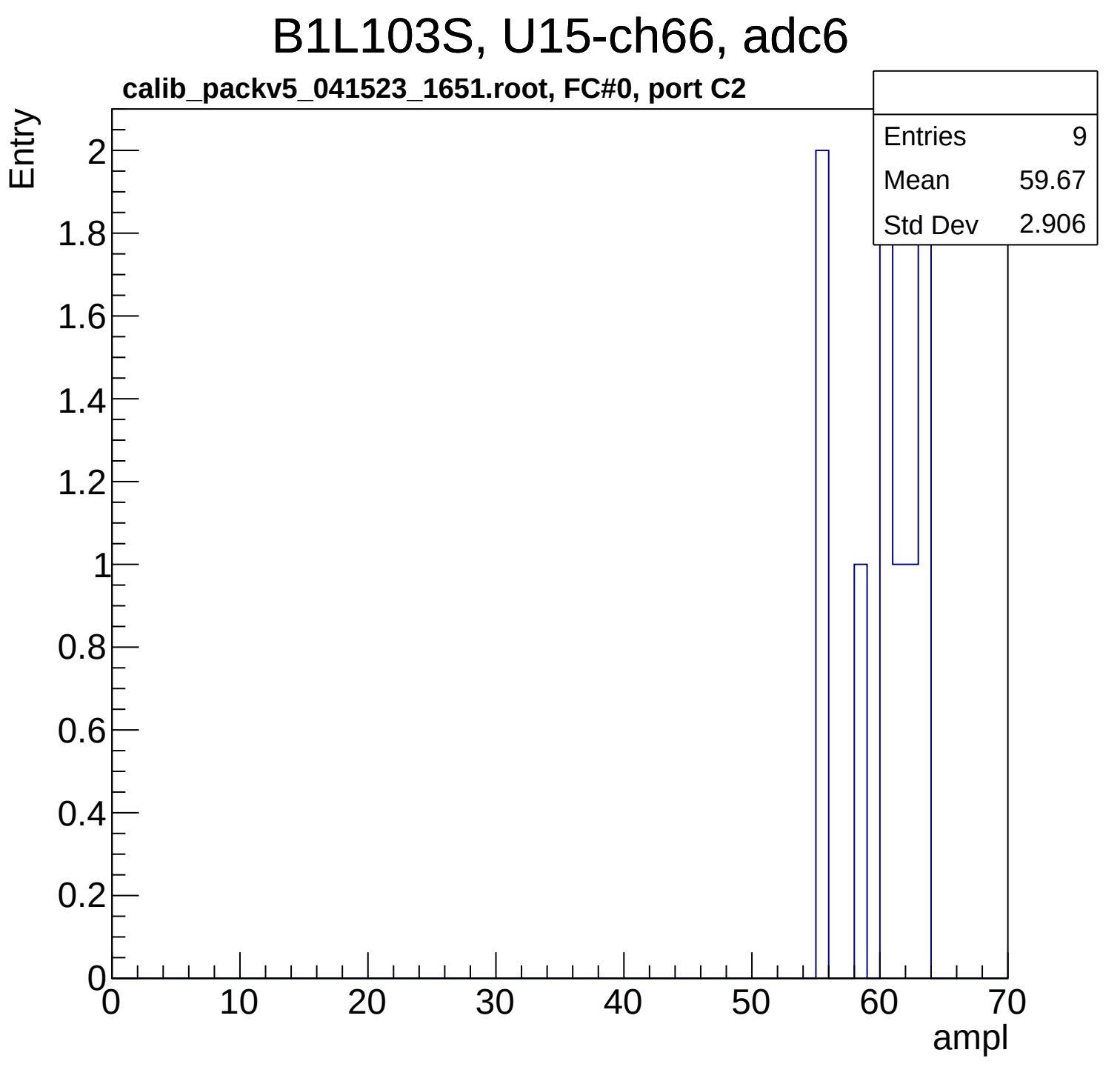

B1L103S, U15-ch66, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 33.92
Std Dev 4.122
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

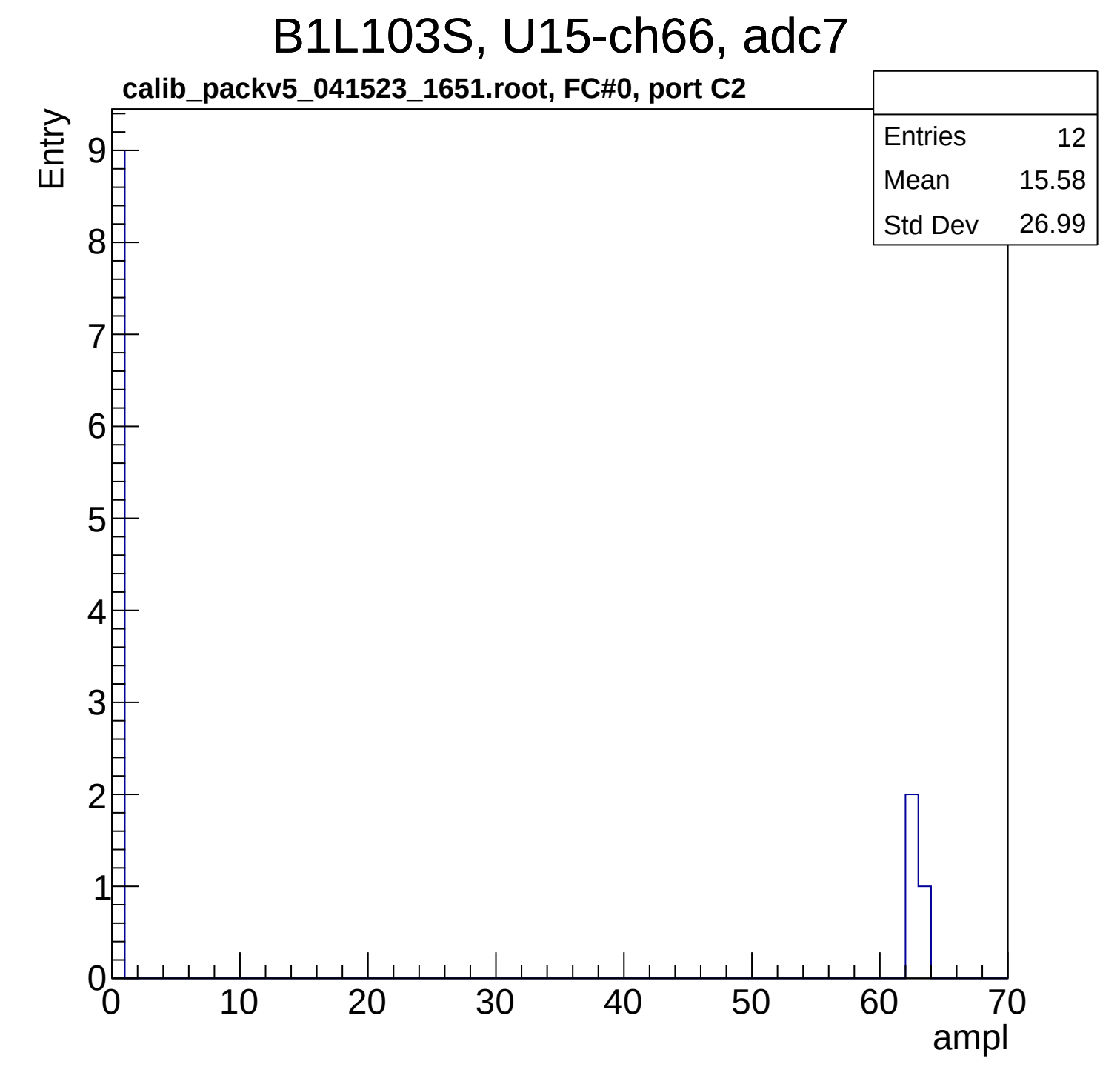

B1L103S, U15-ch66, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 35.81
Std Dev 12.88
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

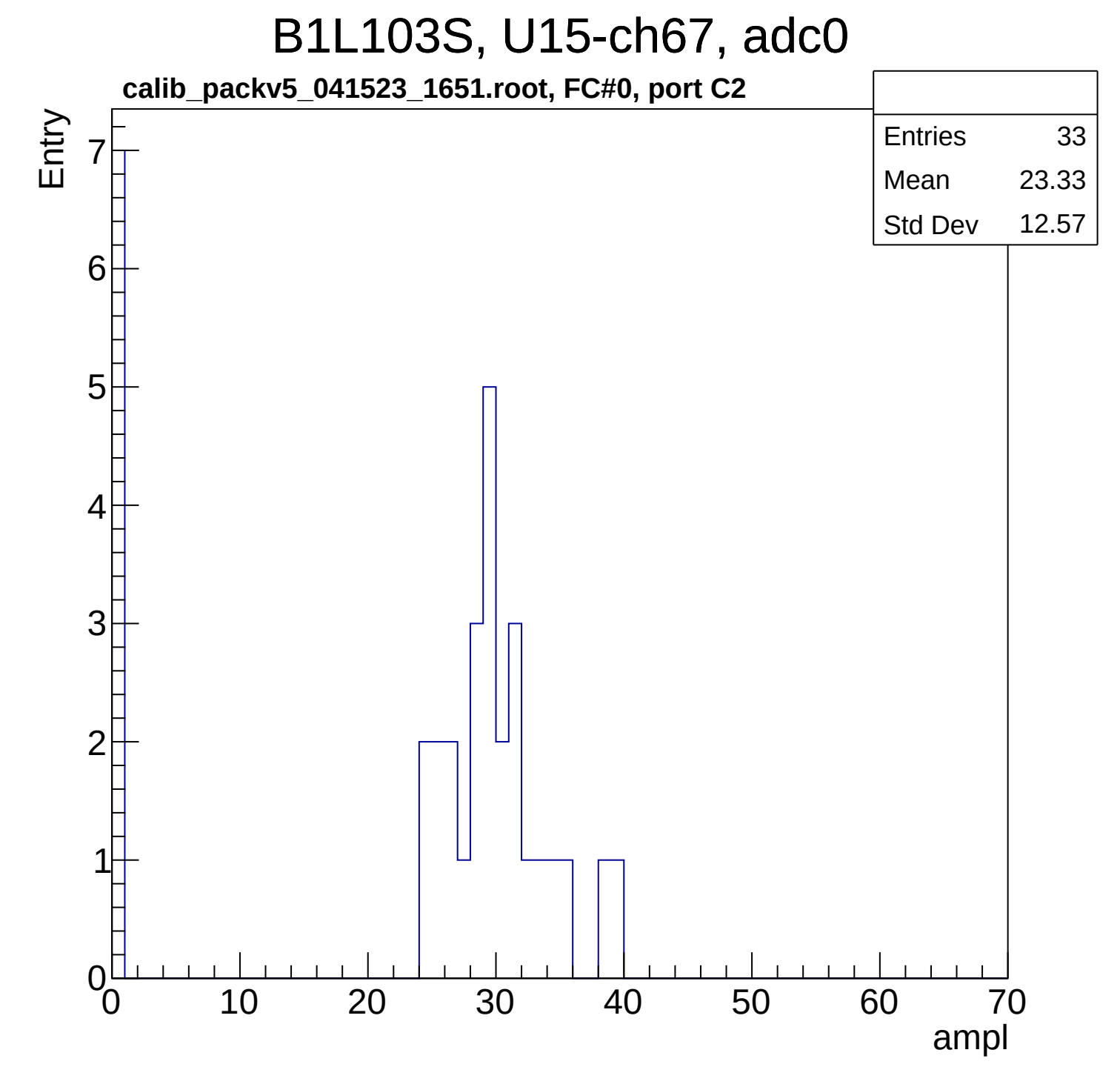

B1L103S, U15-ch66, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 42.32
Std Dev 15.01
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

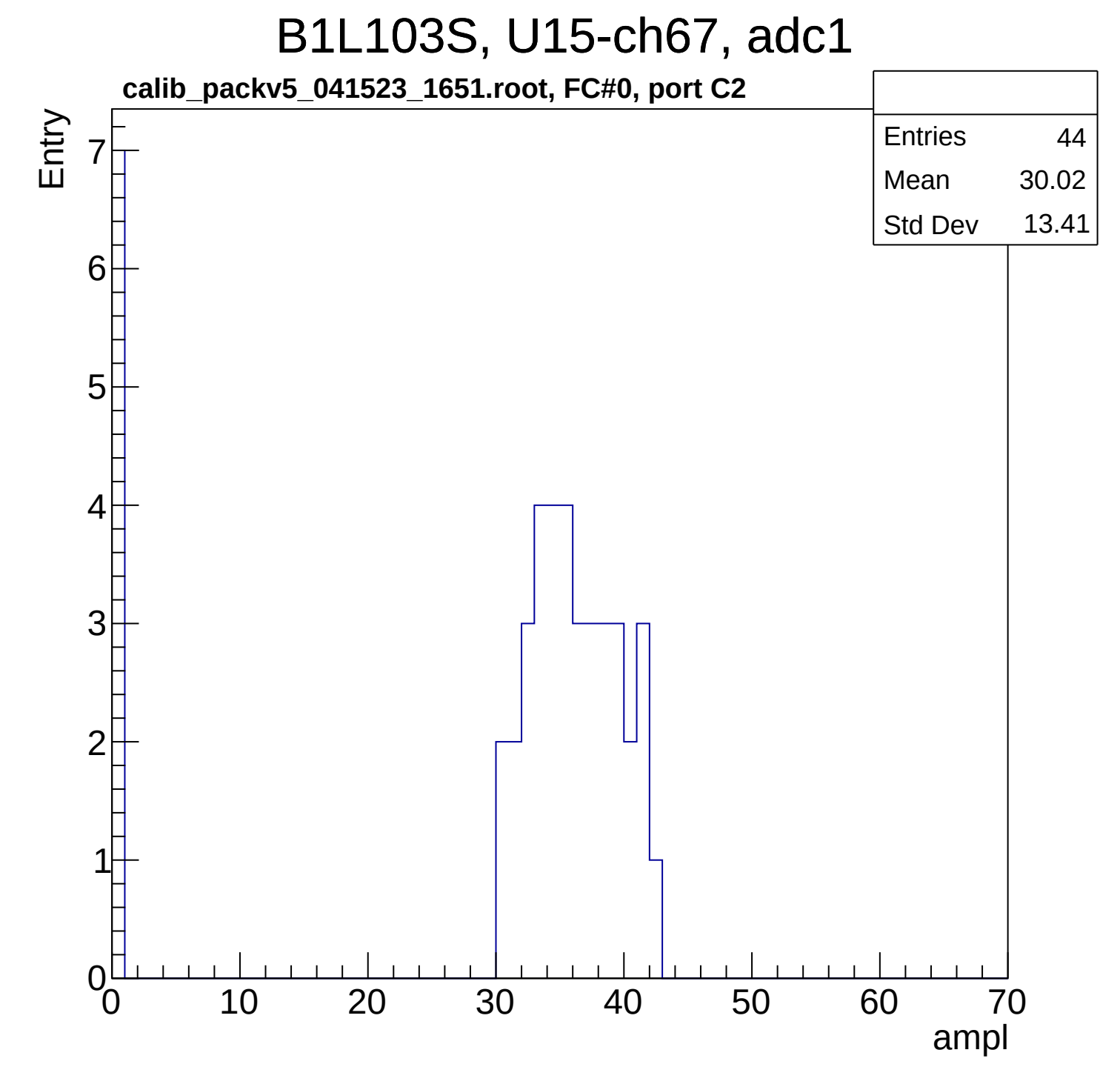

B1L103S, U15-ch66, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 53.05
Std Dev 3.226
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

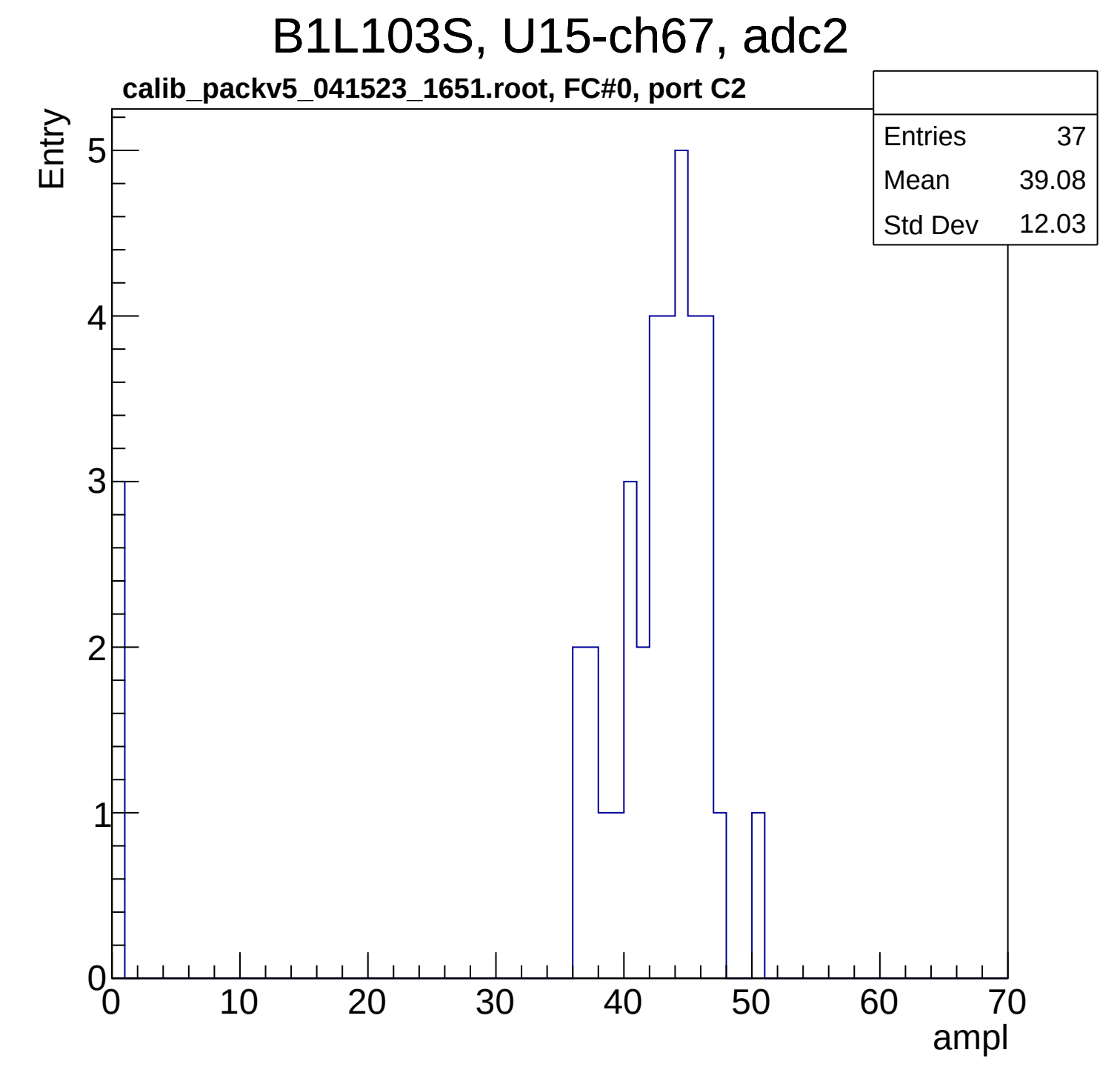

B1L103S, U15-ch66, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 57.97
Std Dev 3.459
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

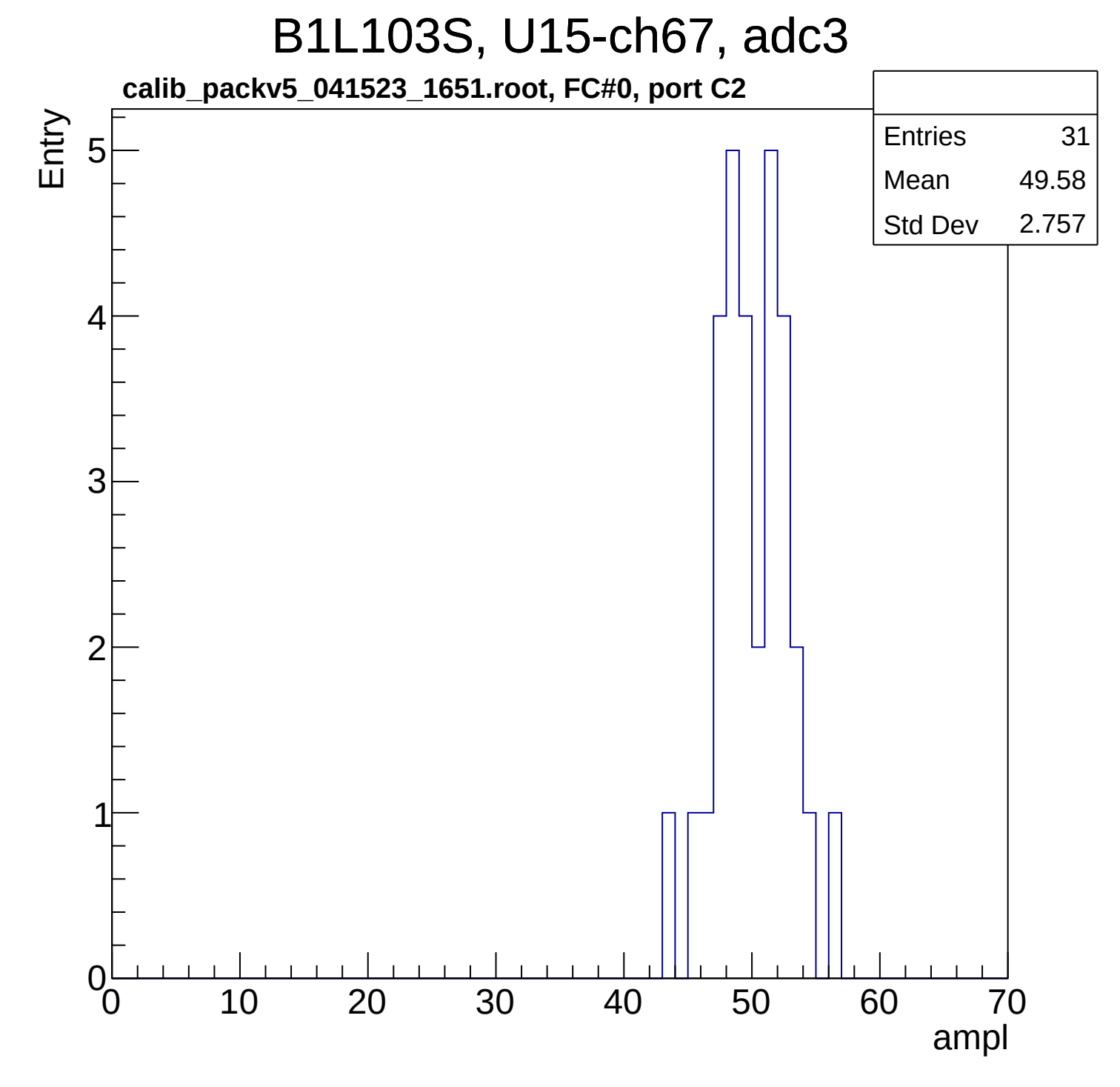

B1L103S, U15-ch66, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 59.67
Std Dev 2.906
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

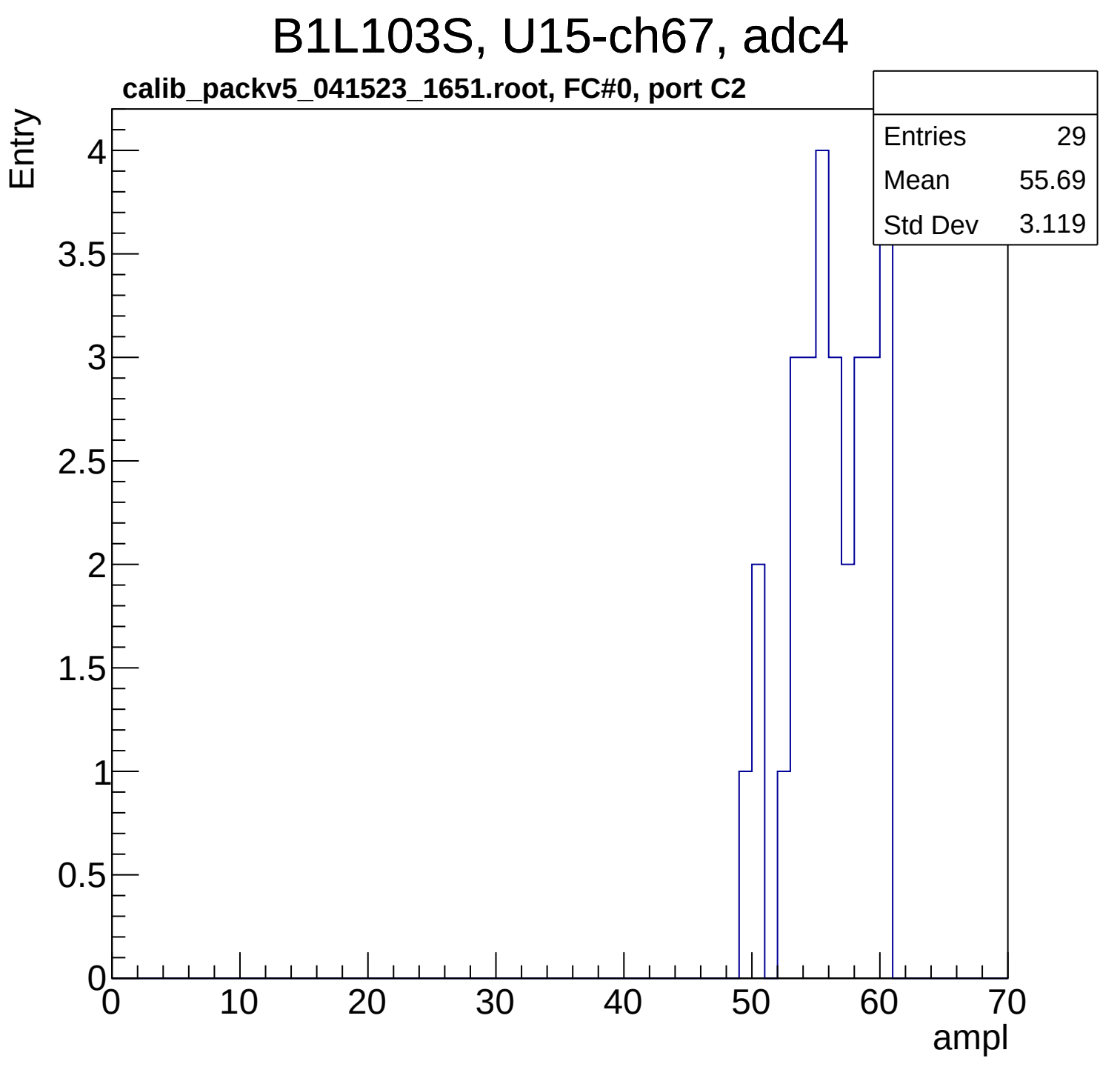

B1L103S, U15-ch66, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 15.58
Std Dev 26.99
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

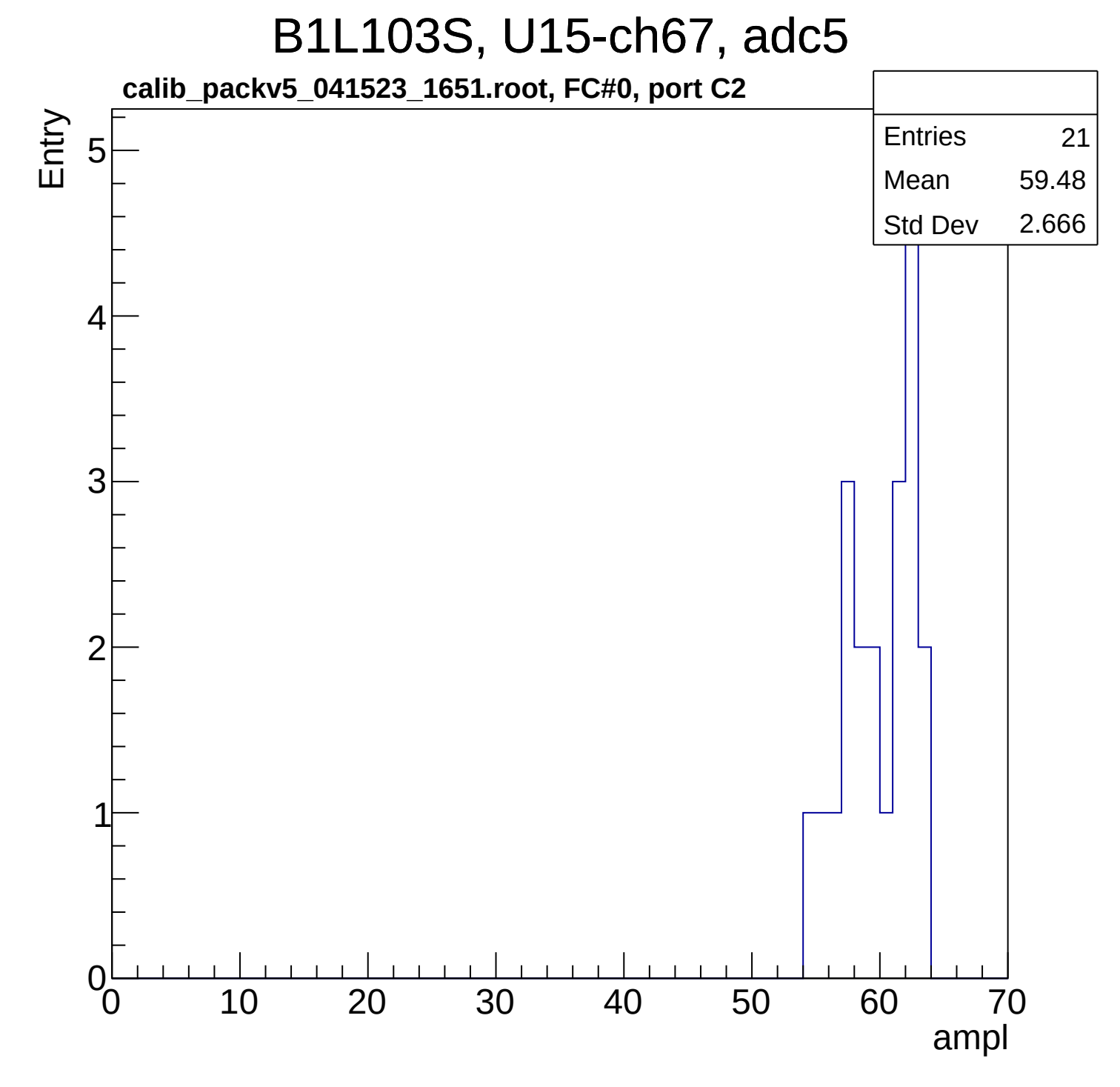

B1L103S, U15-ch67, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 23.33
Std Dev 12.57
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U15-ch67, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 30.02
Std Dev 13.41
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U15-ch67, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 39.08
Std Dev 12.03
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch67, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 49.58
Std Dev 2.757
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch67, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 55.69
Std Dev 3.119
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch67, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 59.48
Std Dev 2.666
Entry
ampl
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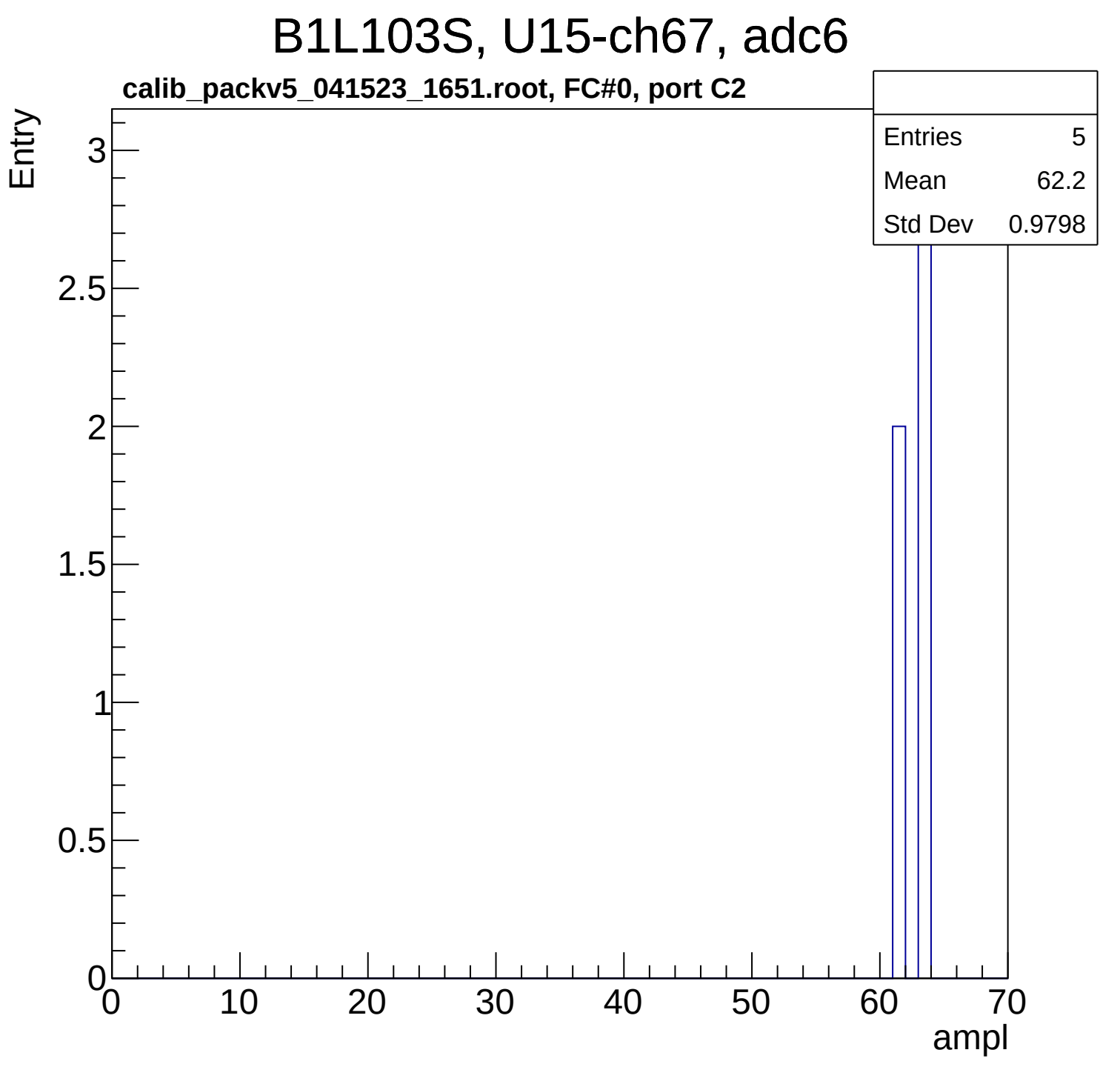
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch67, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.2
Std Dev 0.9798
Entry
ampl
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0.5
1
1.5
2
2.5
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0
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40
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60
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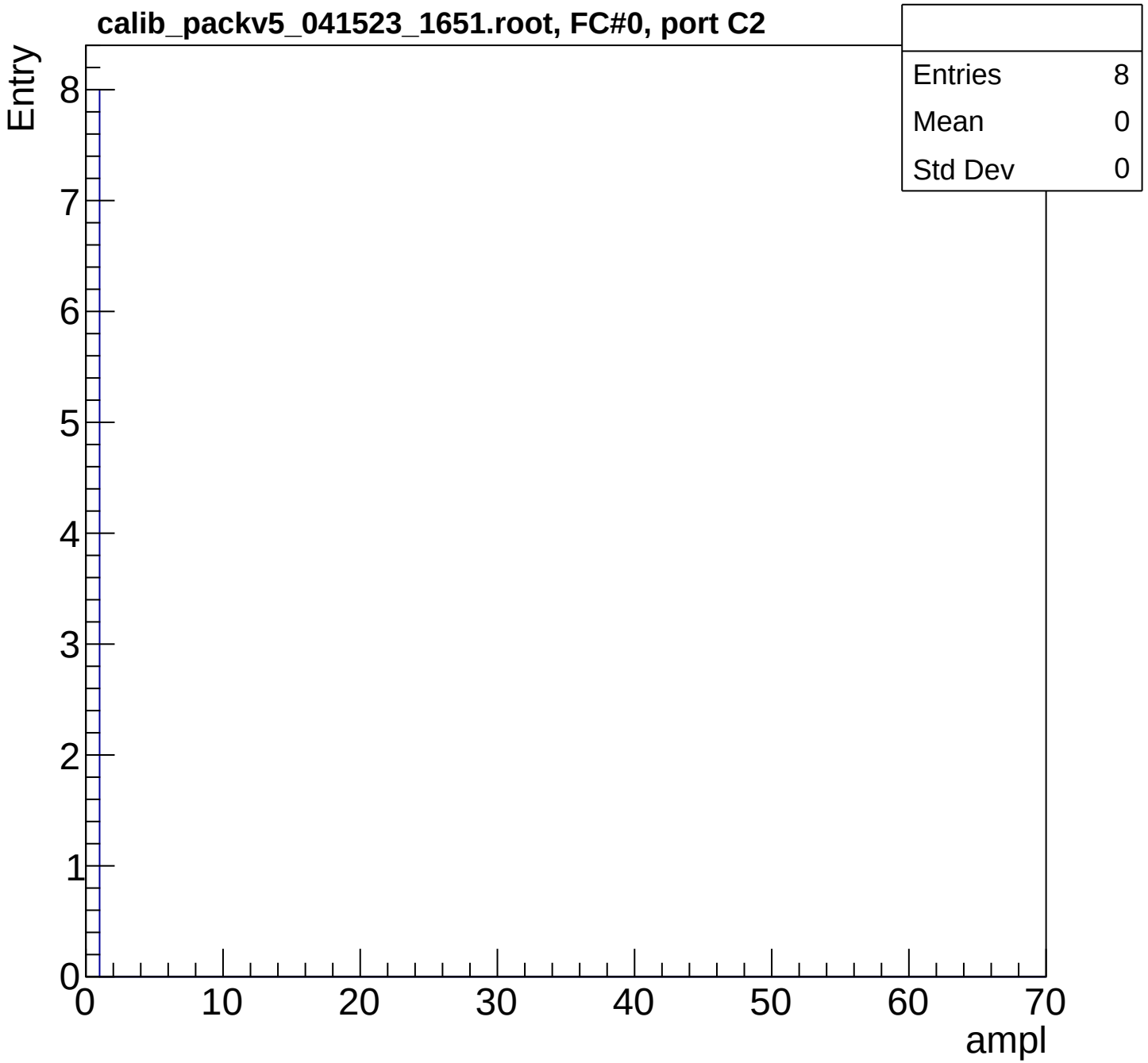
B1L103S, U15-ch67, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 0
Std Dev 0
Entry
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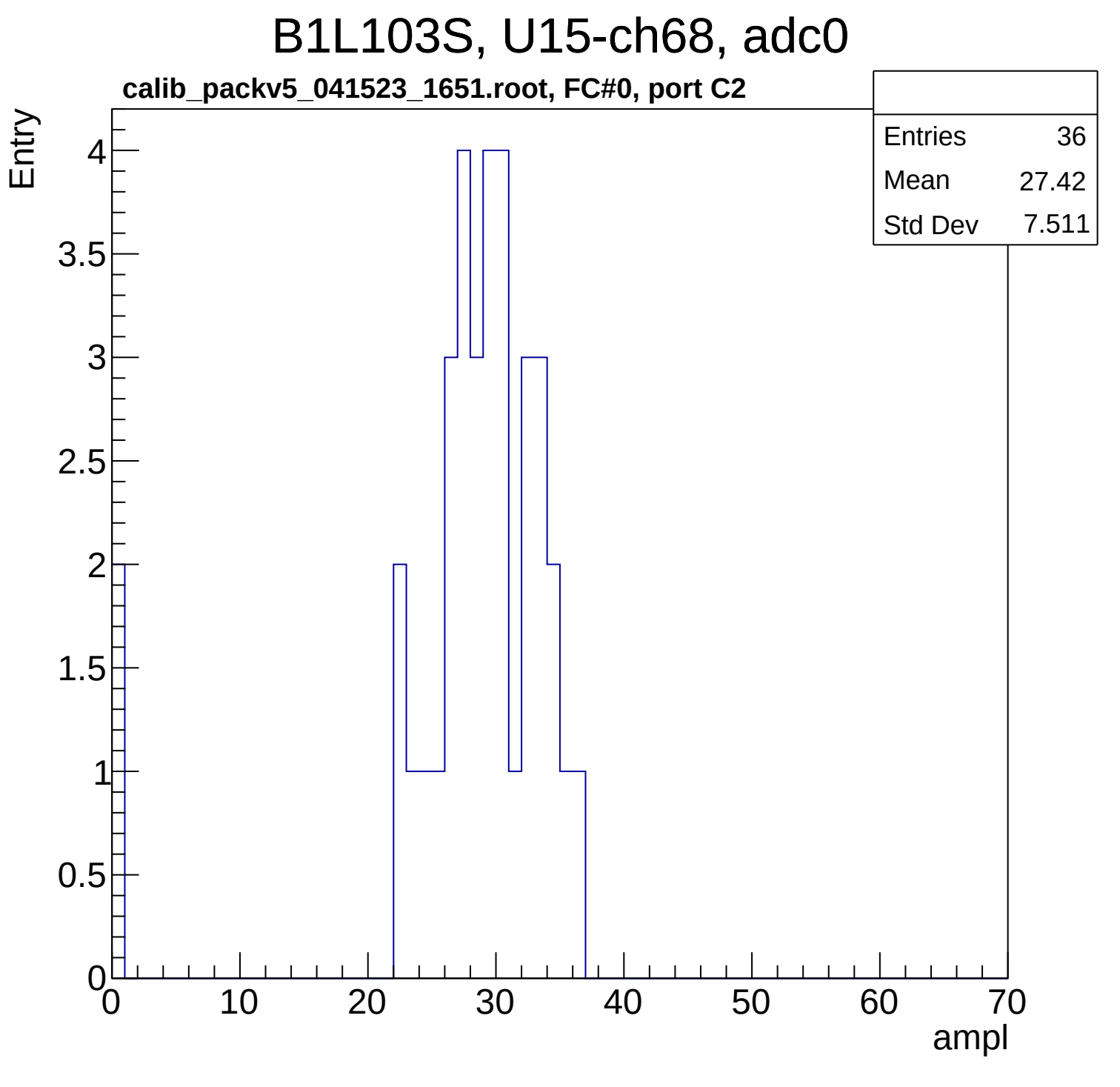
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch68, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 27.42
Std Dev 7.511
Entry
ampl
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1.5
2
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3.5
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0
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60
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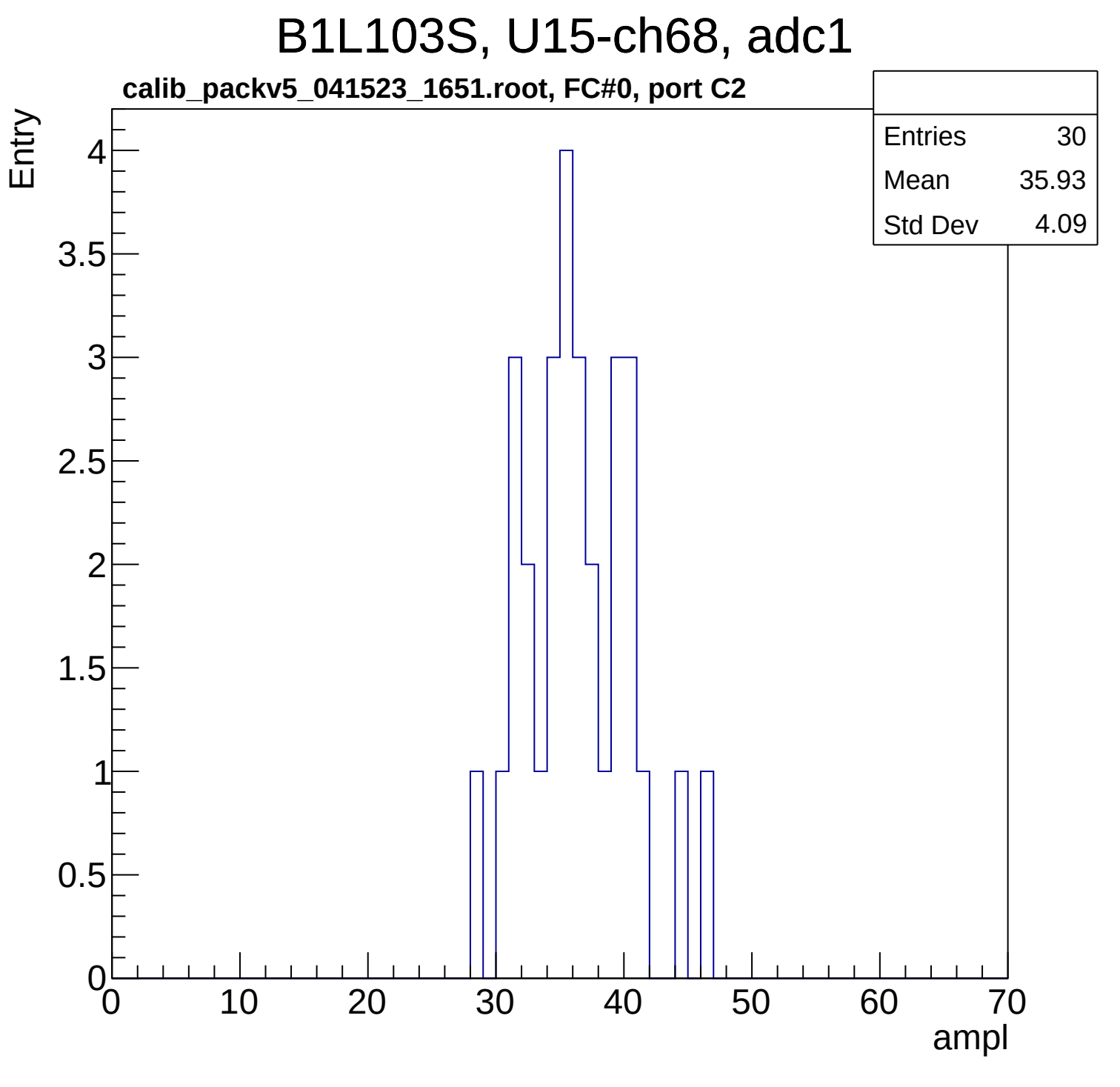
B1L103S, U15-ch68, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 35.93
Std Dev 4.09
Entry
ampl
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1.5
2
2.5
3
3.5
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0
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40
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60
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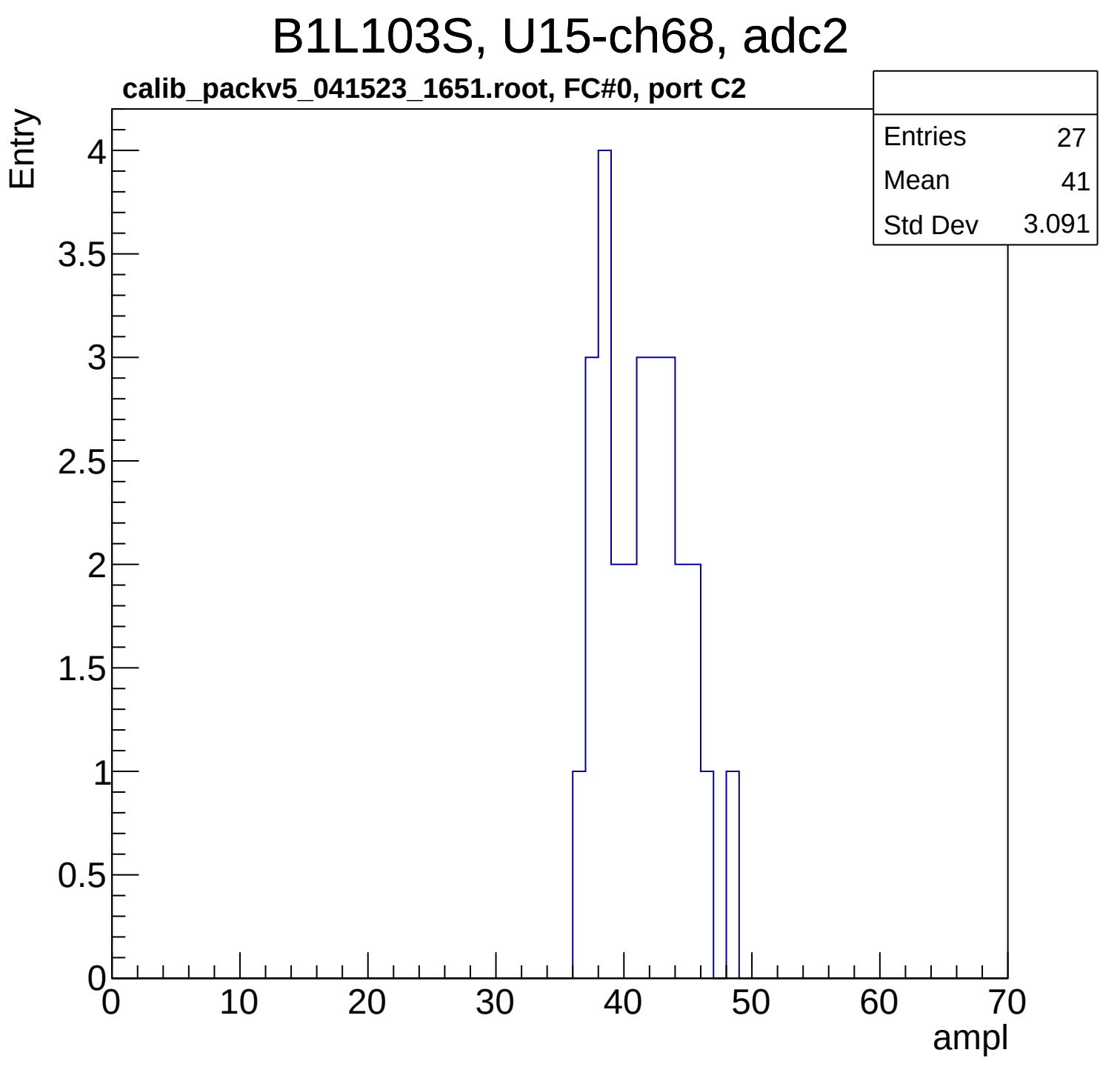
B1L103S, U15-ch68, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 41
Std Dev 3.091
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
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0
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40
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60
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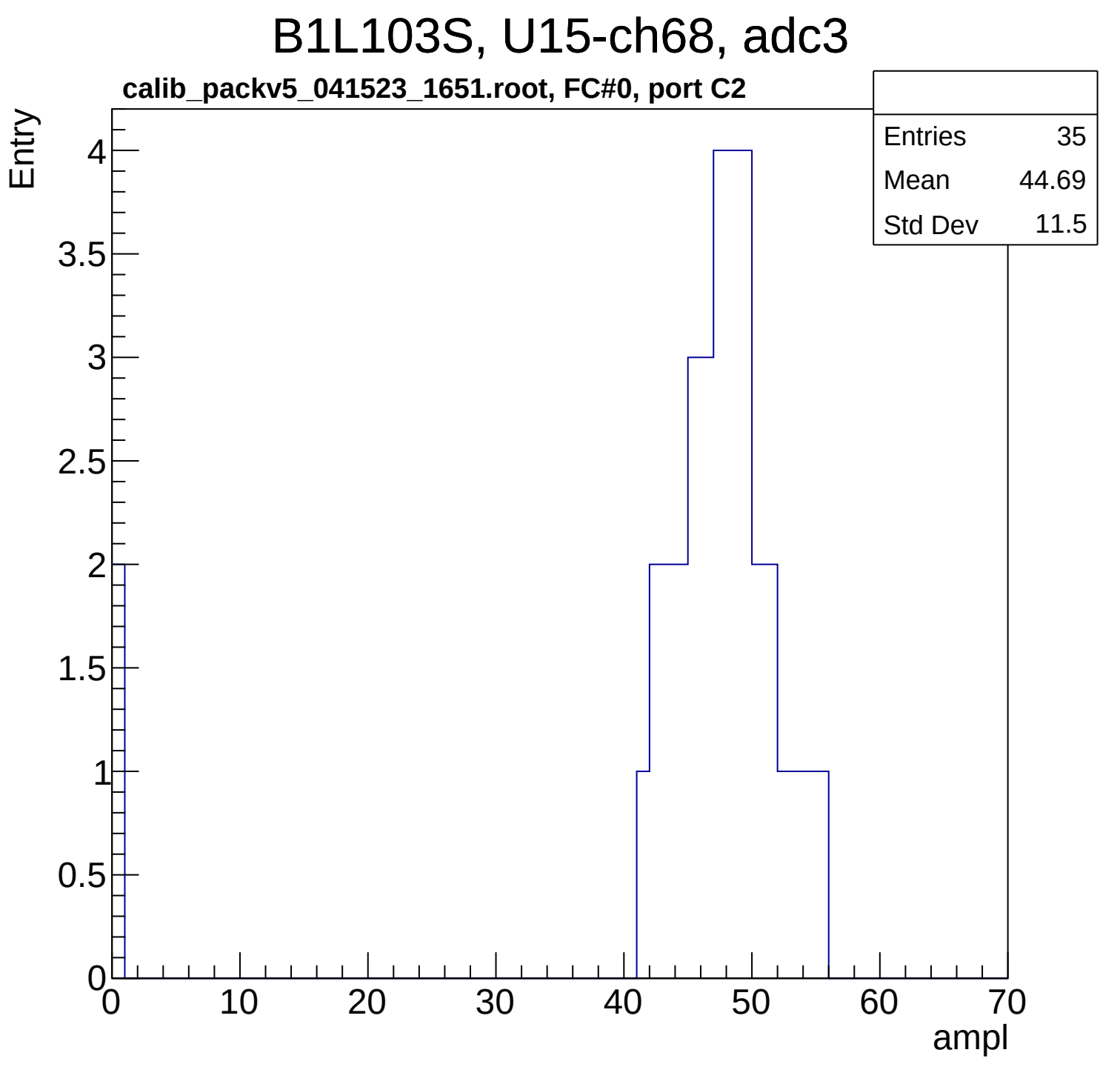
B1L103S, U15-ch68, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 44.69
Std Dev 11.5
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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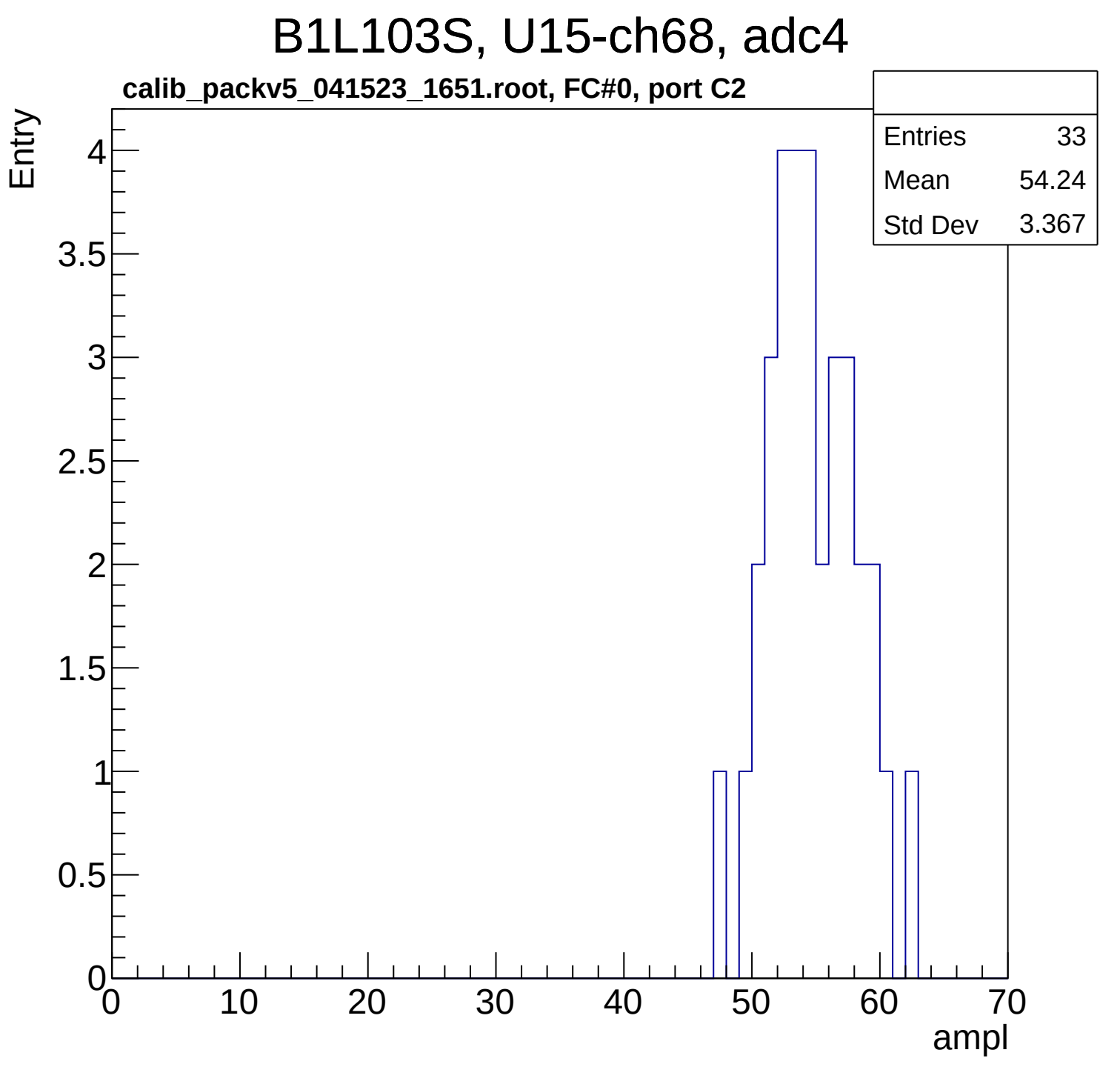
B1L103S, U15-ch68, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 54.24
Std Dev 3.367
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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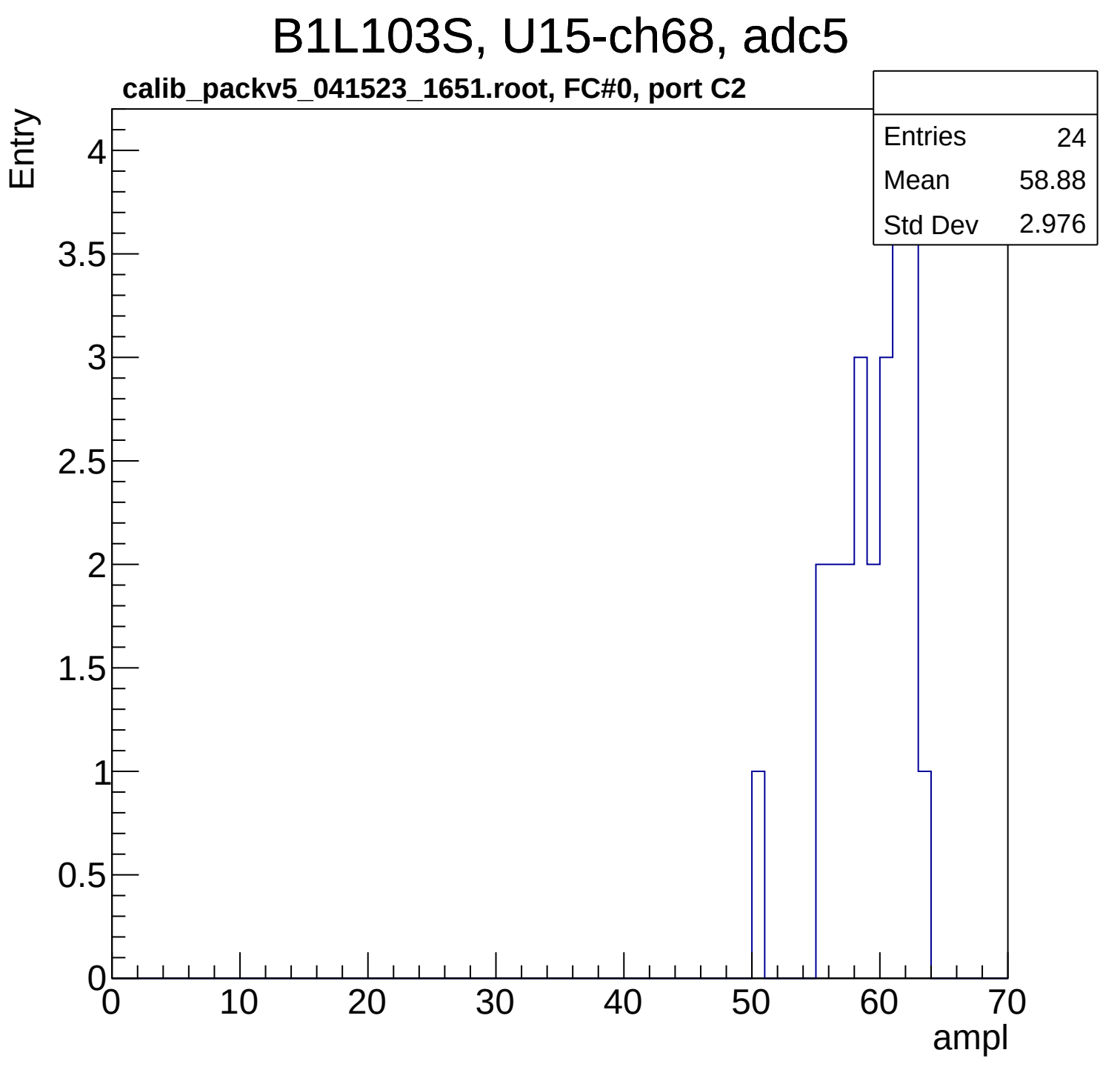
B1L103S, U15-ch68, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 58.88
Std Dev 2.976
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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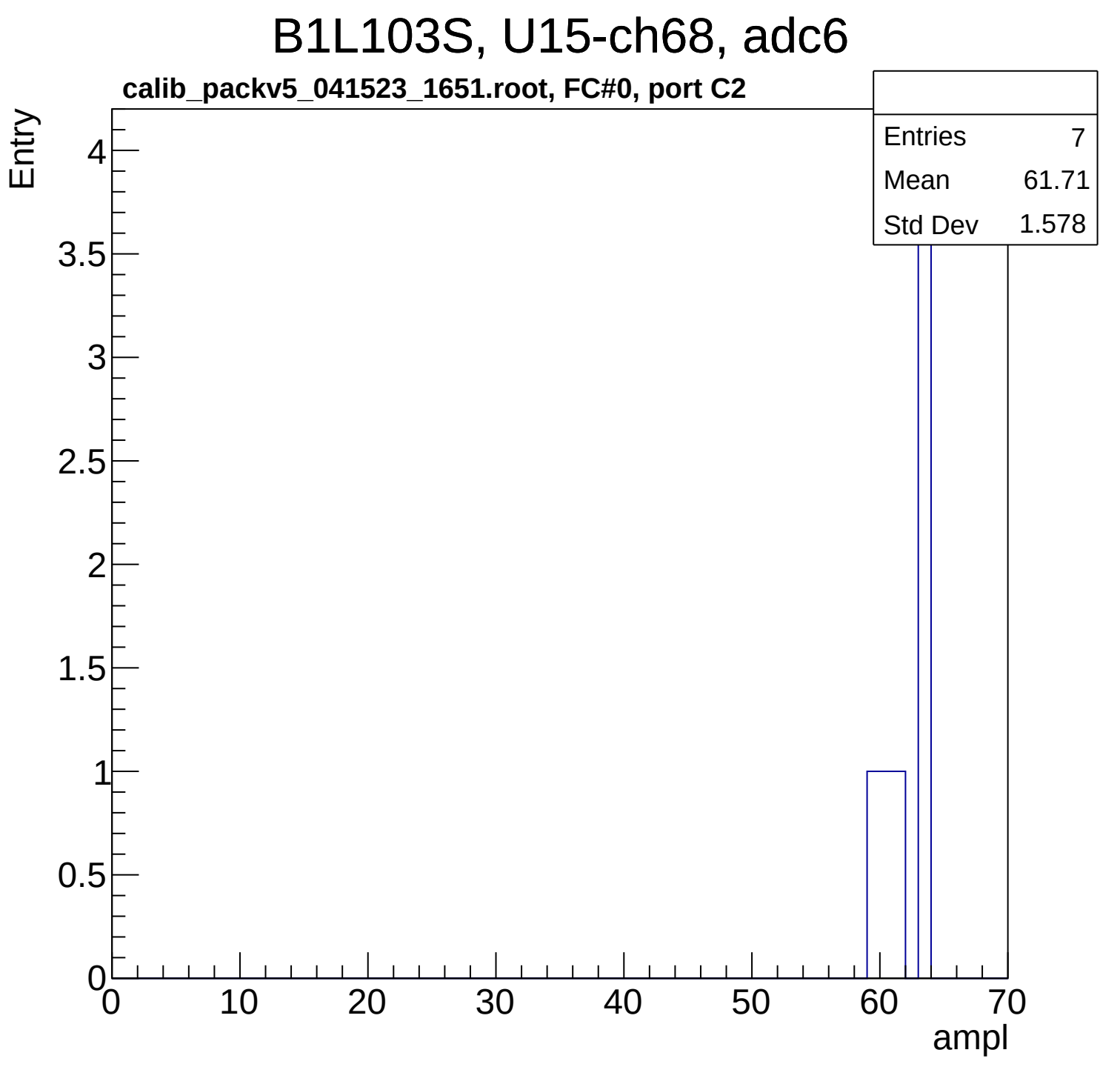
B1L103S, U15-ch68, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.71
Std Dev 1.578
Entry
ampl
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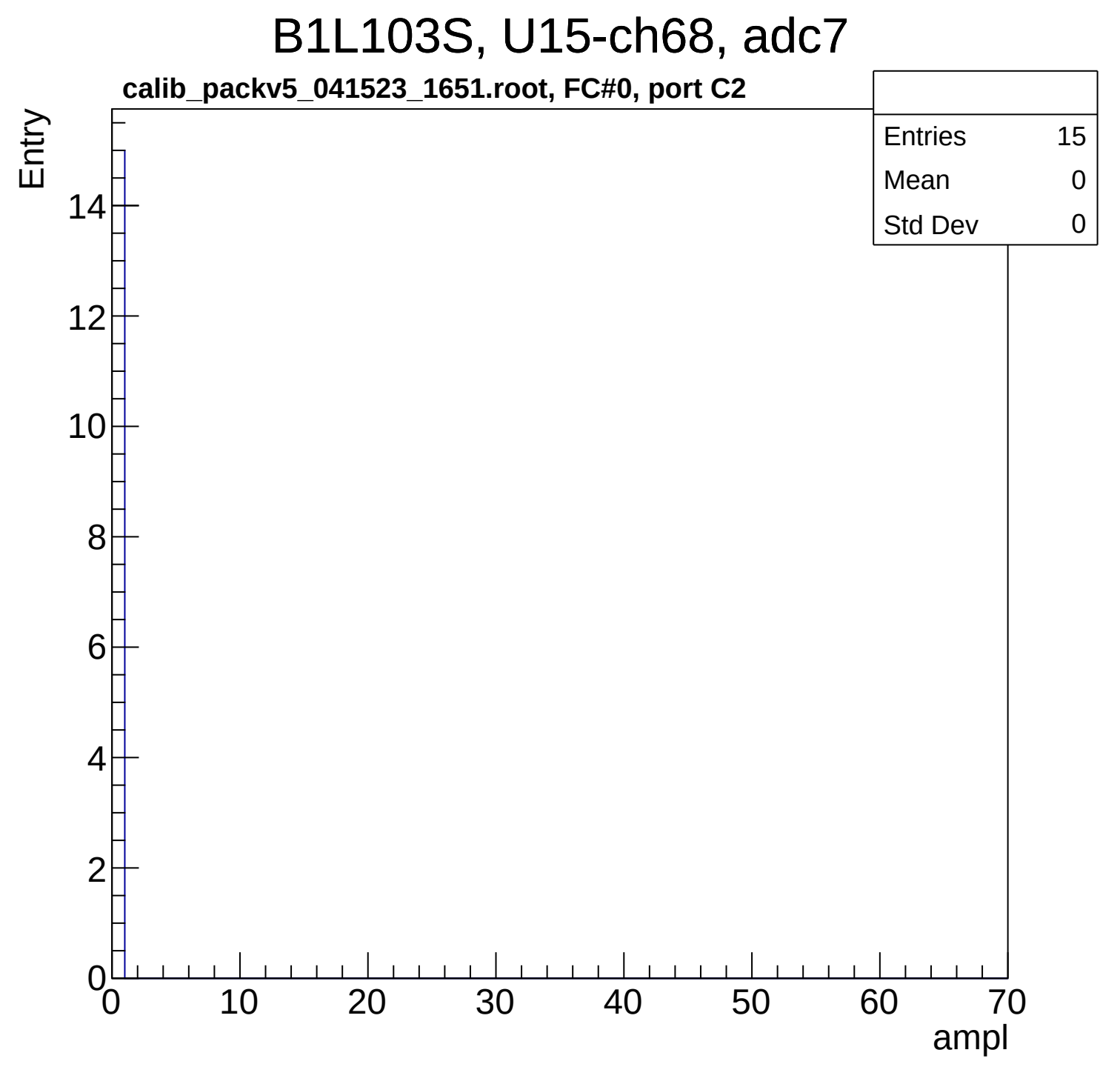
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch68, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 0
Std Dev 0
Entry
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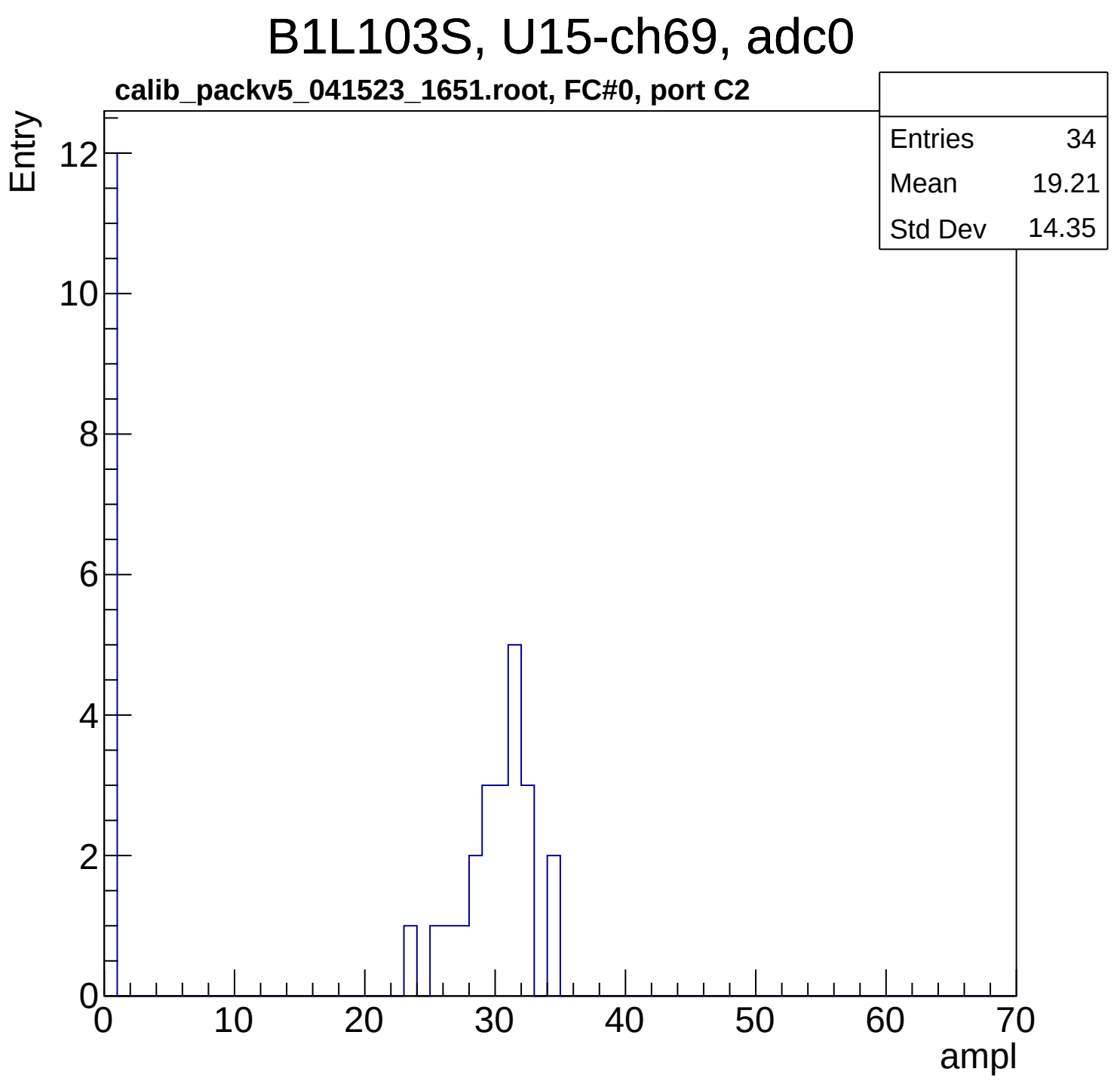
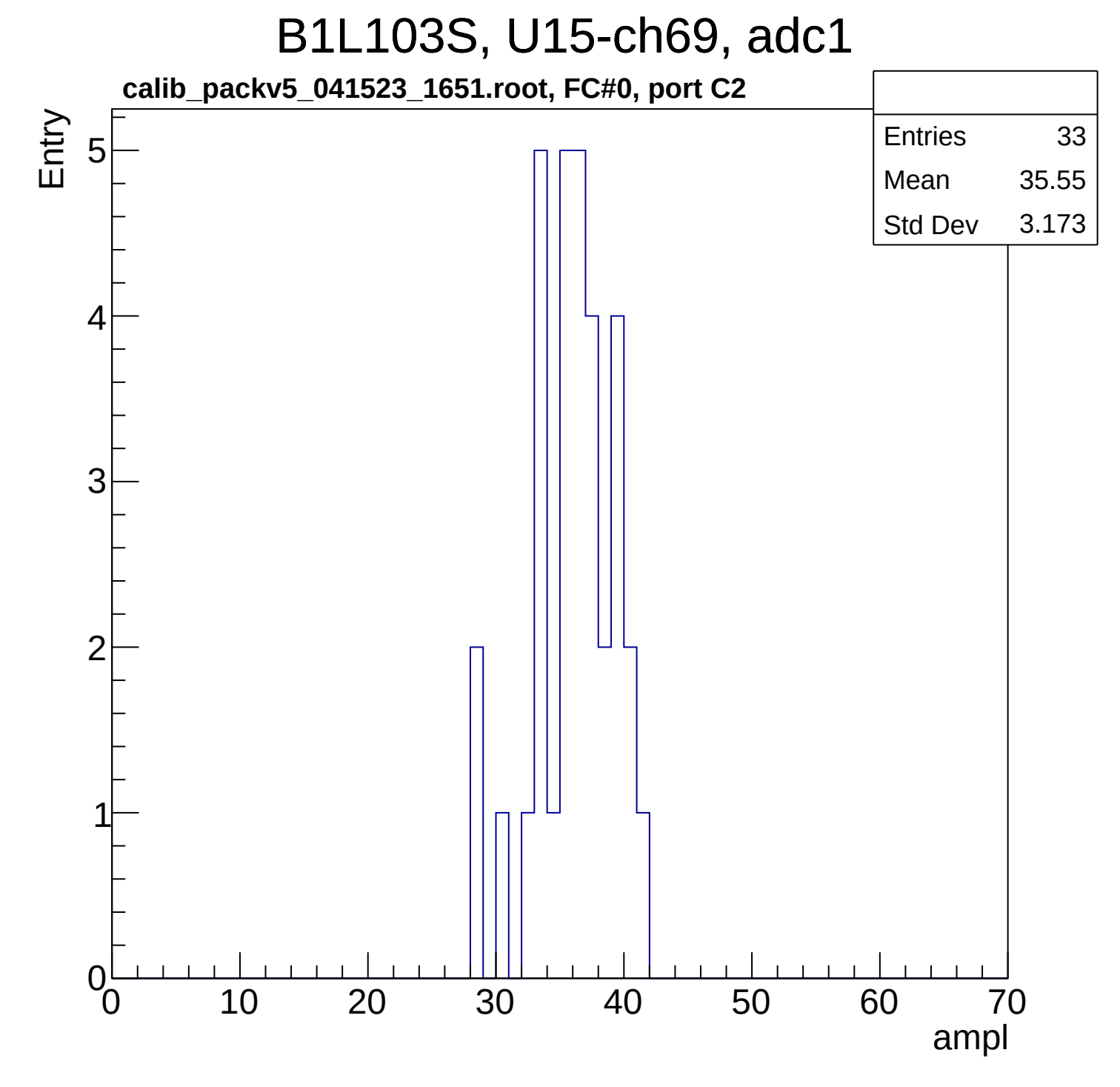
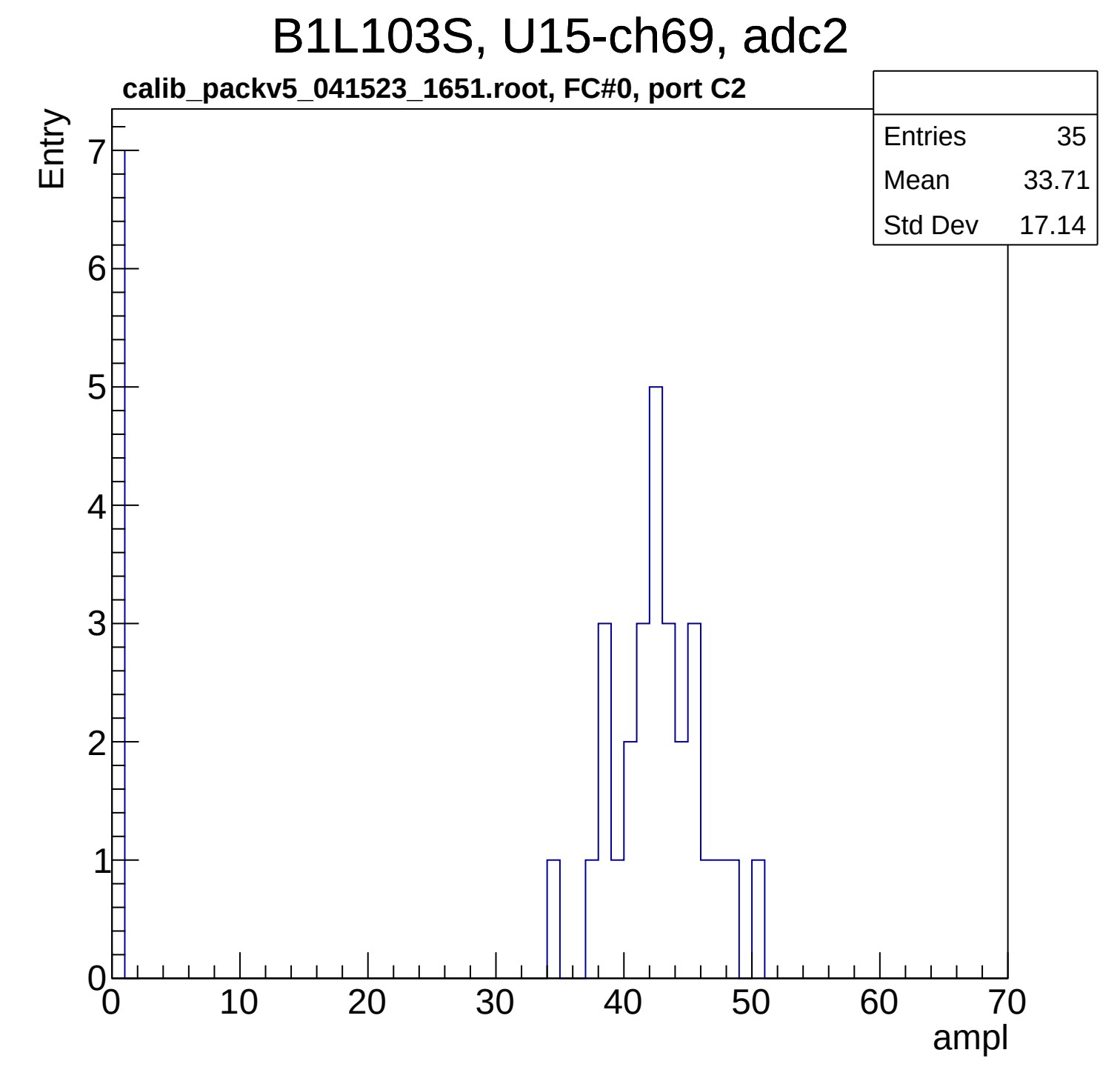
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch69, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 19.21
Std Dev 14.35
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch69, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 35.55
Std Dev 3.173
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch69, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 33.71
Std Dev 17.14
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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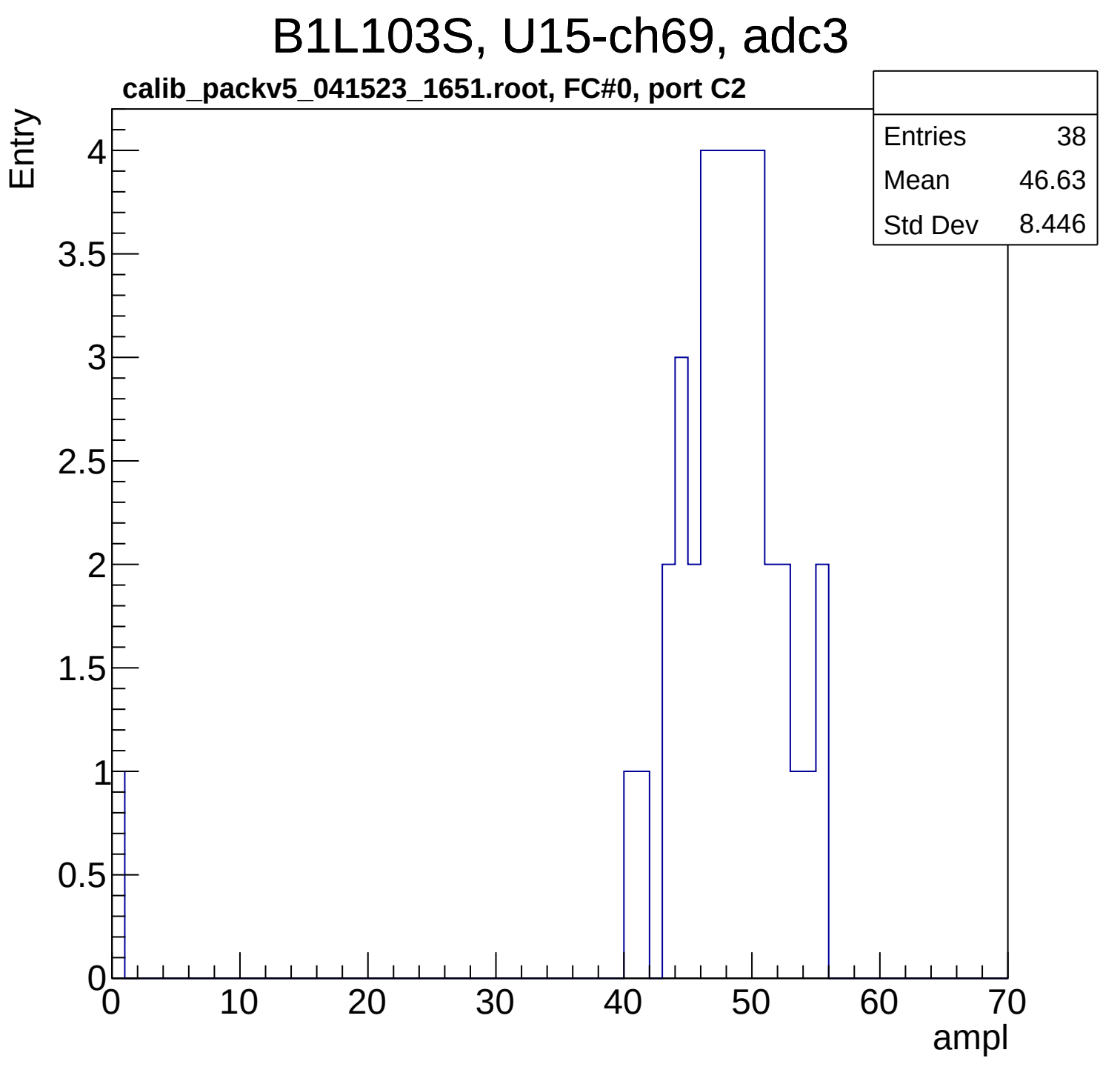
B1L103S, U15-ch69, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 46.63
Std Dev 8.446
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
10
20
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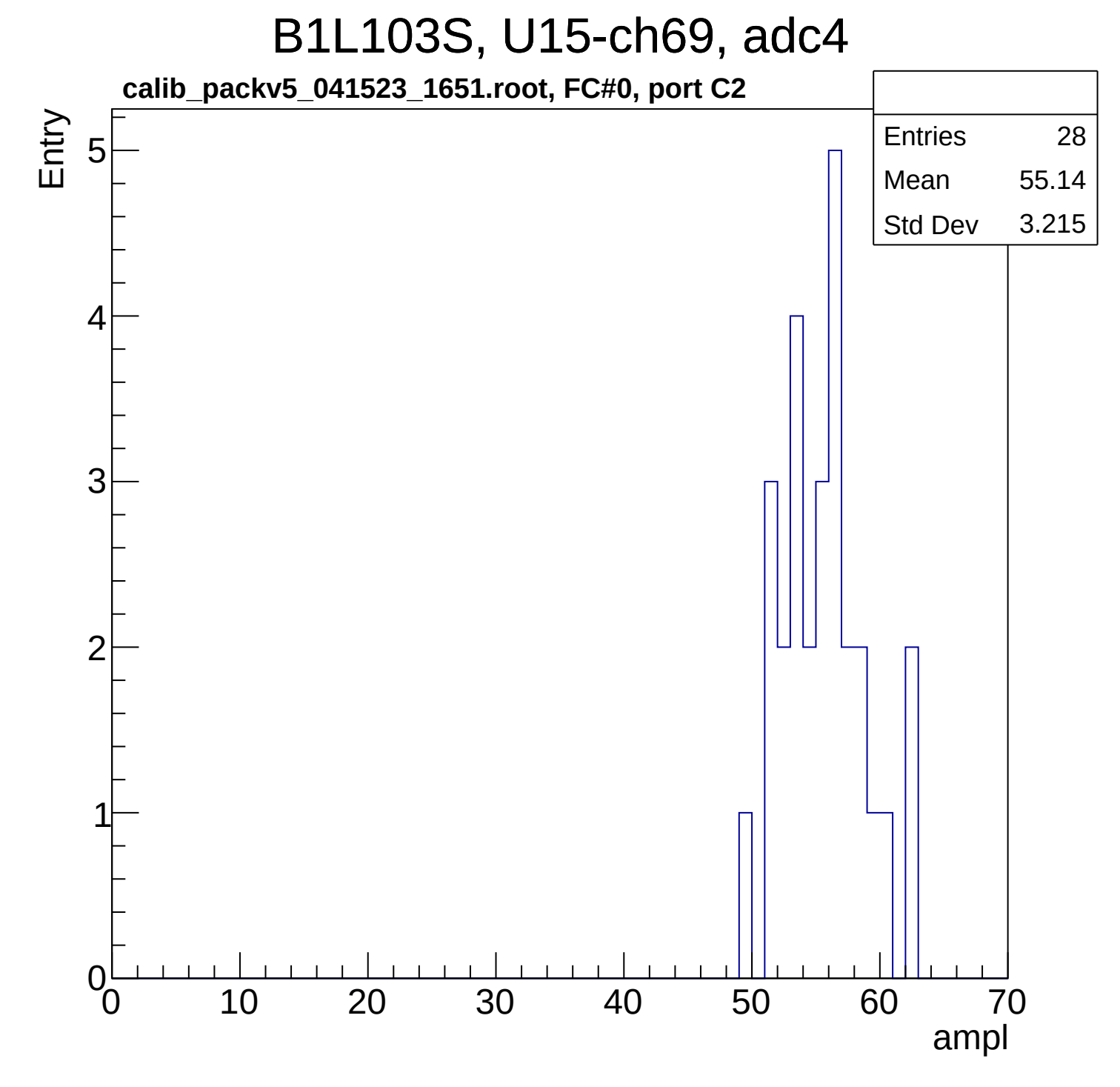
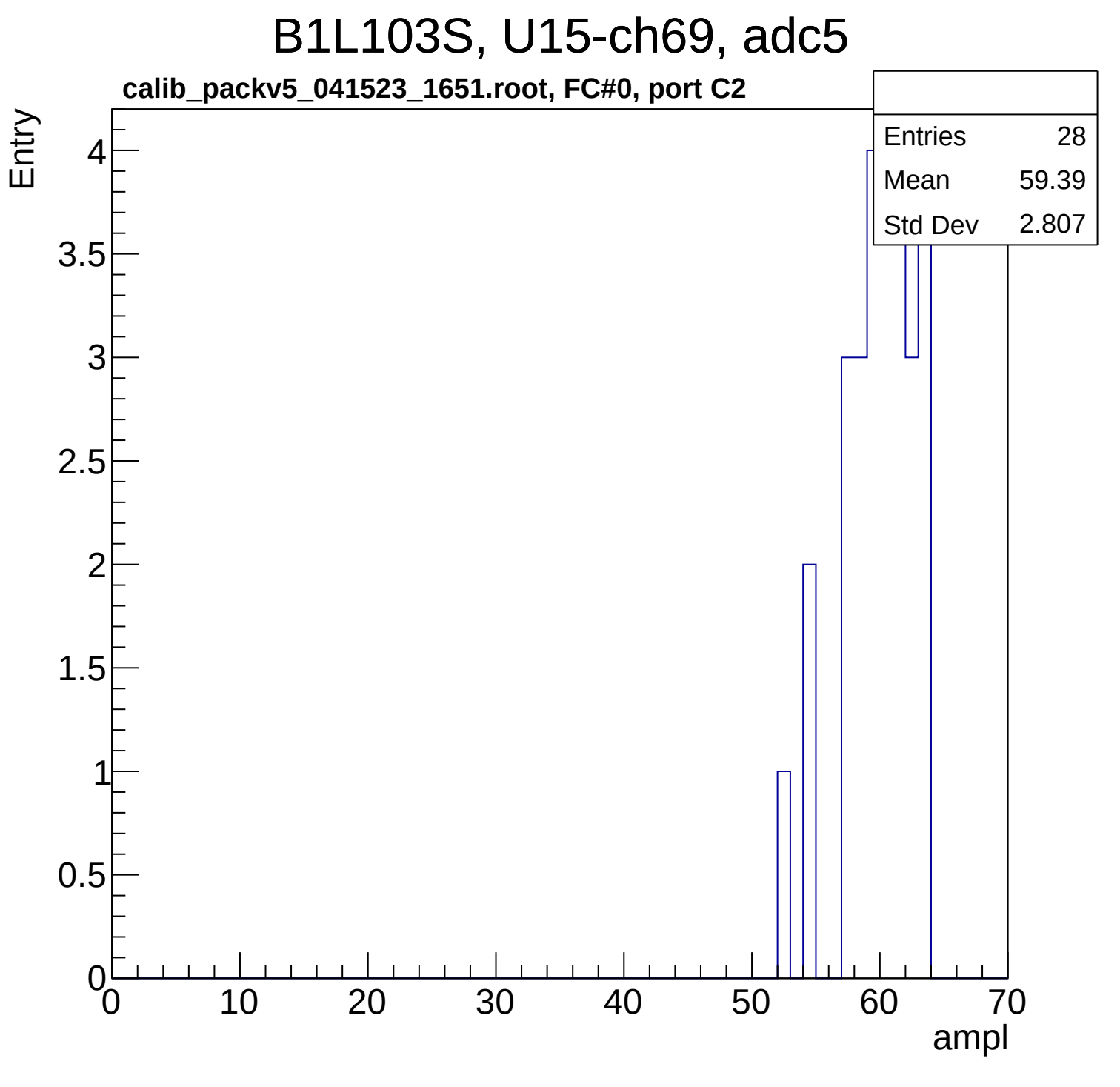
40
50
60
70


B1L103S, U15-ch69, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 55.14
Std Dev 3.215
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch69, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 59.39
Std Dev 2.807
Entry
ampl
0
0.5
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1.5
2
2.5
3
3.5
4
0
10
20
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40
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60
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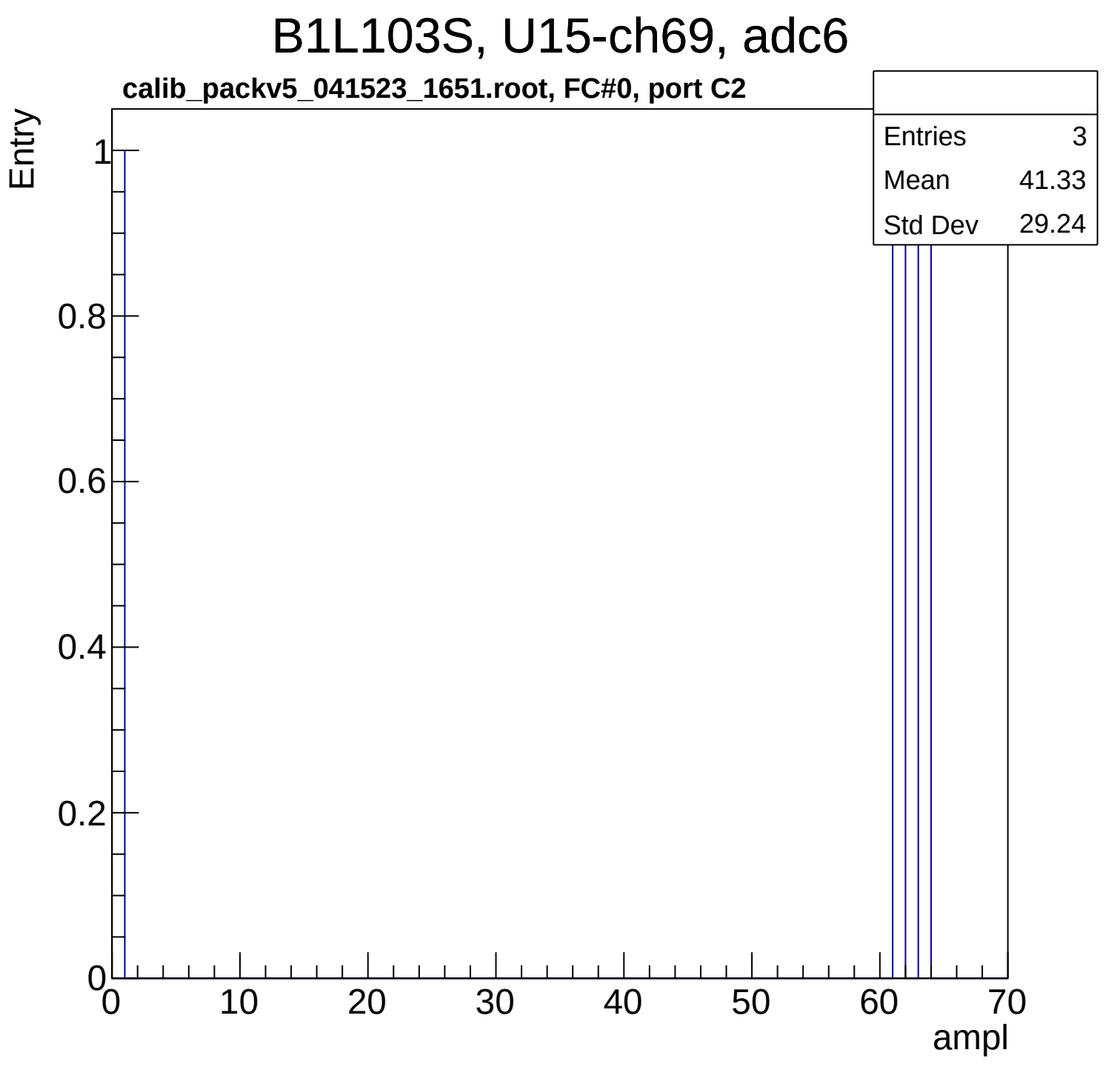
B1L103S, U15-ch69, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 41.33
Std Dev 29.24
Entry
ampl
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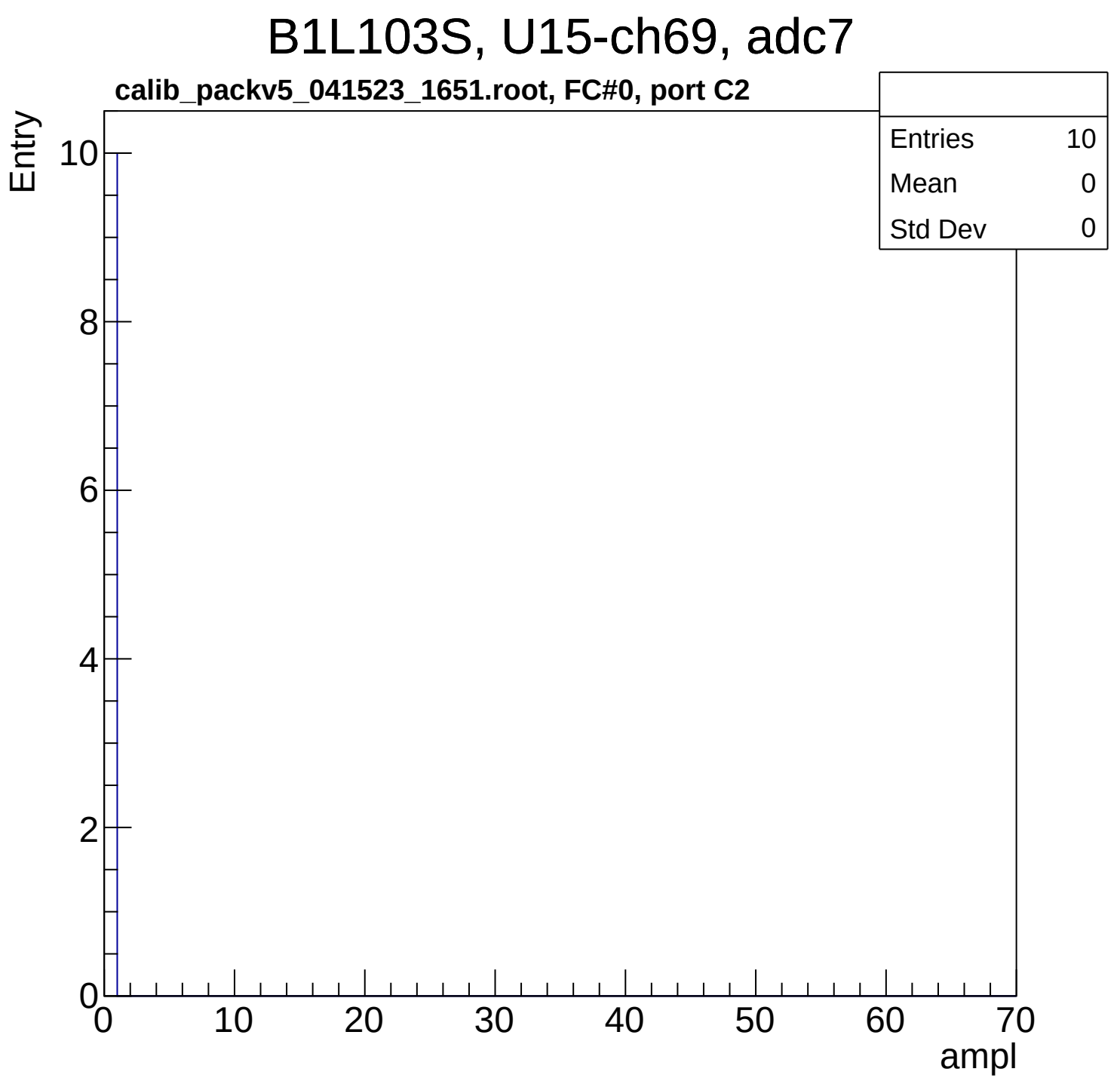
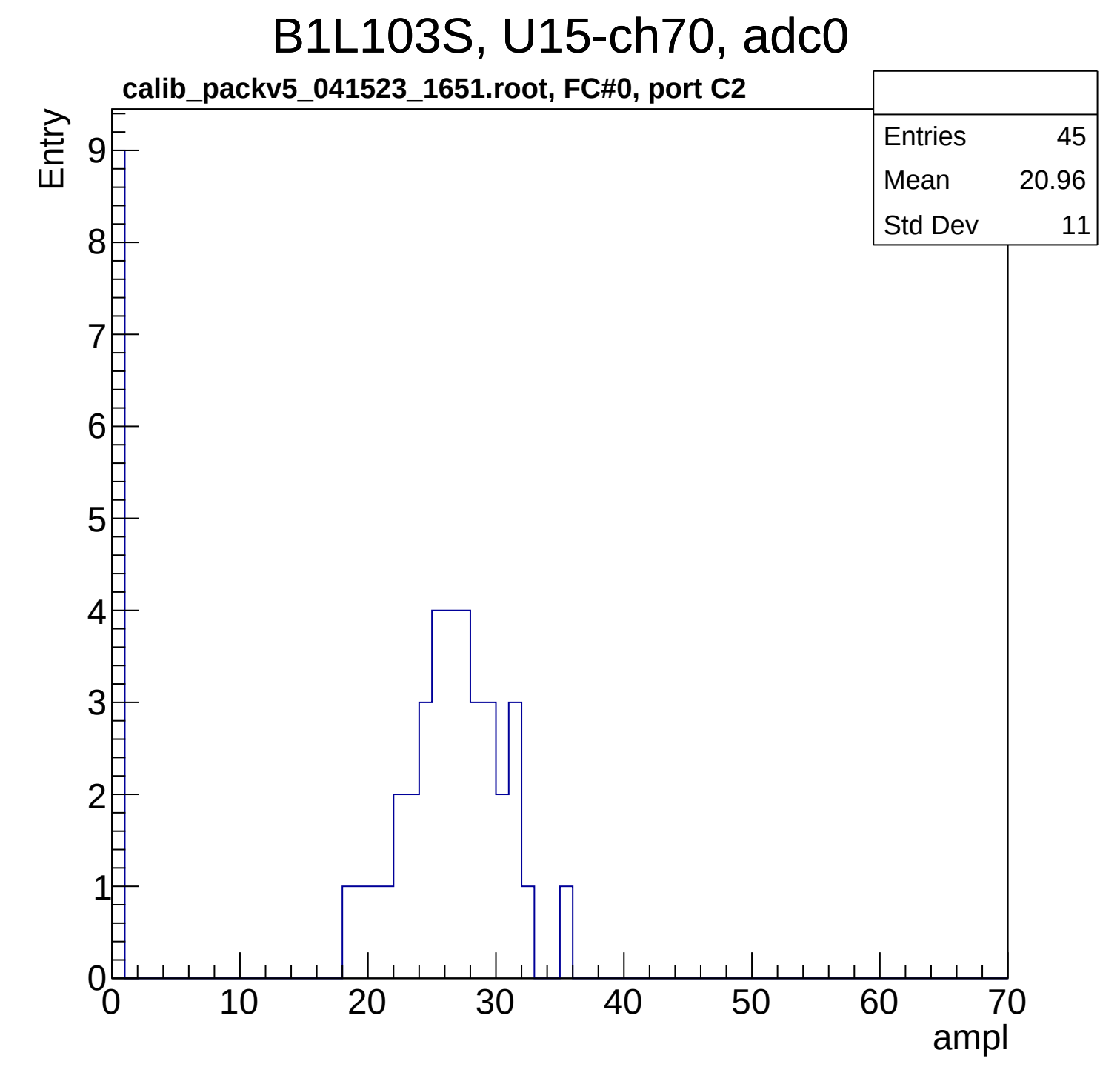
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L103S, U15-ch69, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch70, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 20.96
Std Dev 11
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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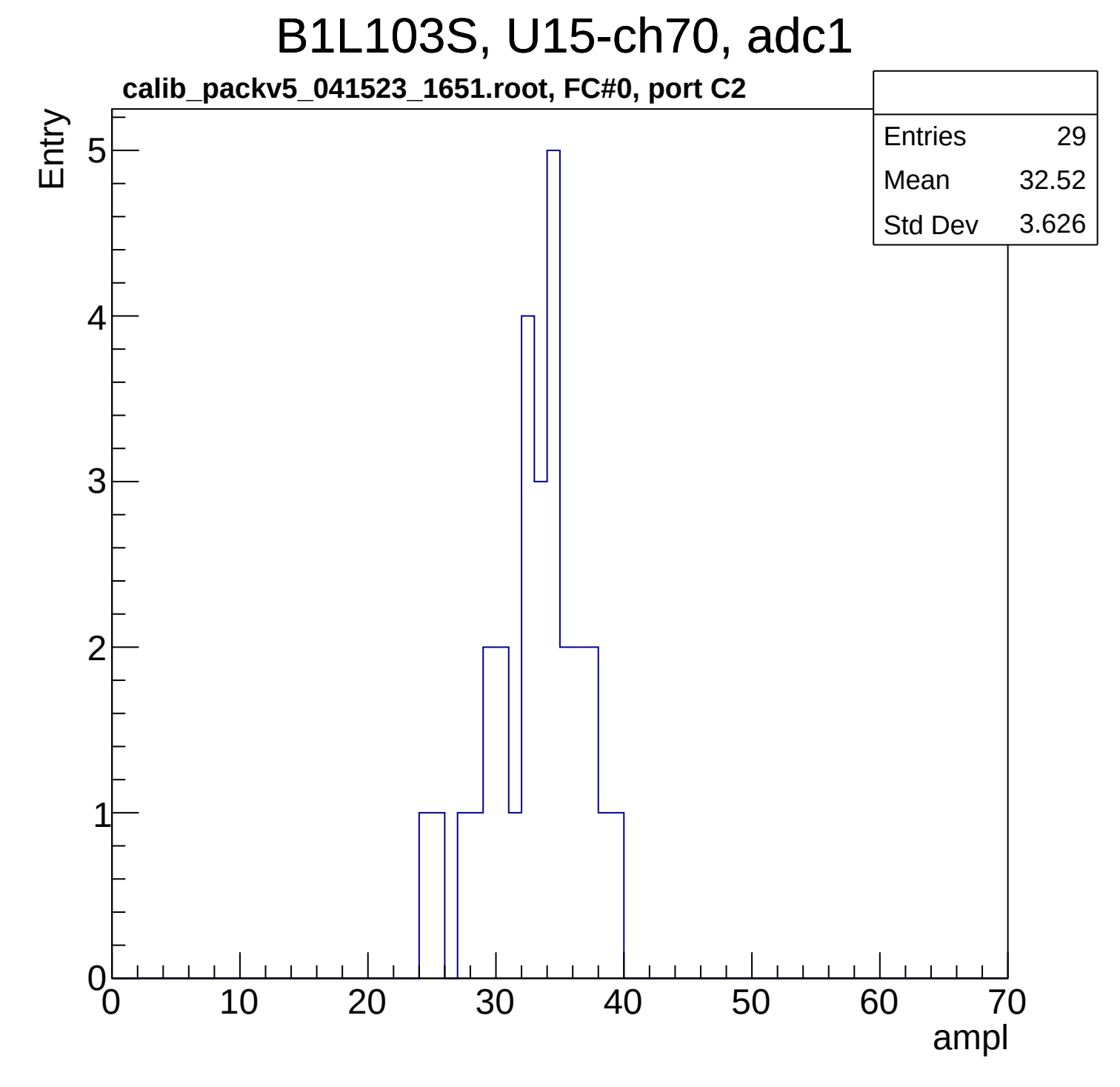
B1L103S, U15-ch70, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 32.52
Std Dev 3.626
Entry
ampl
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2
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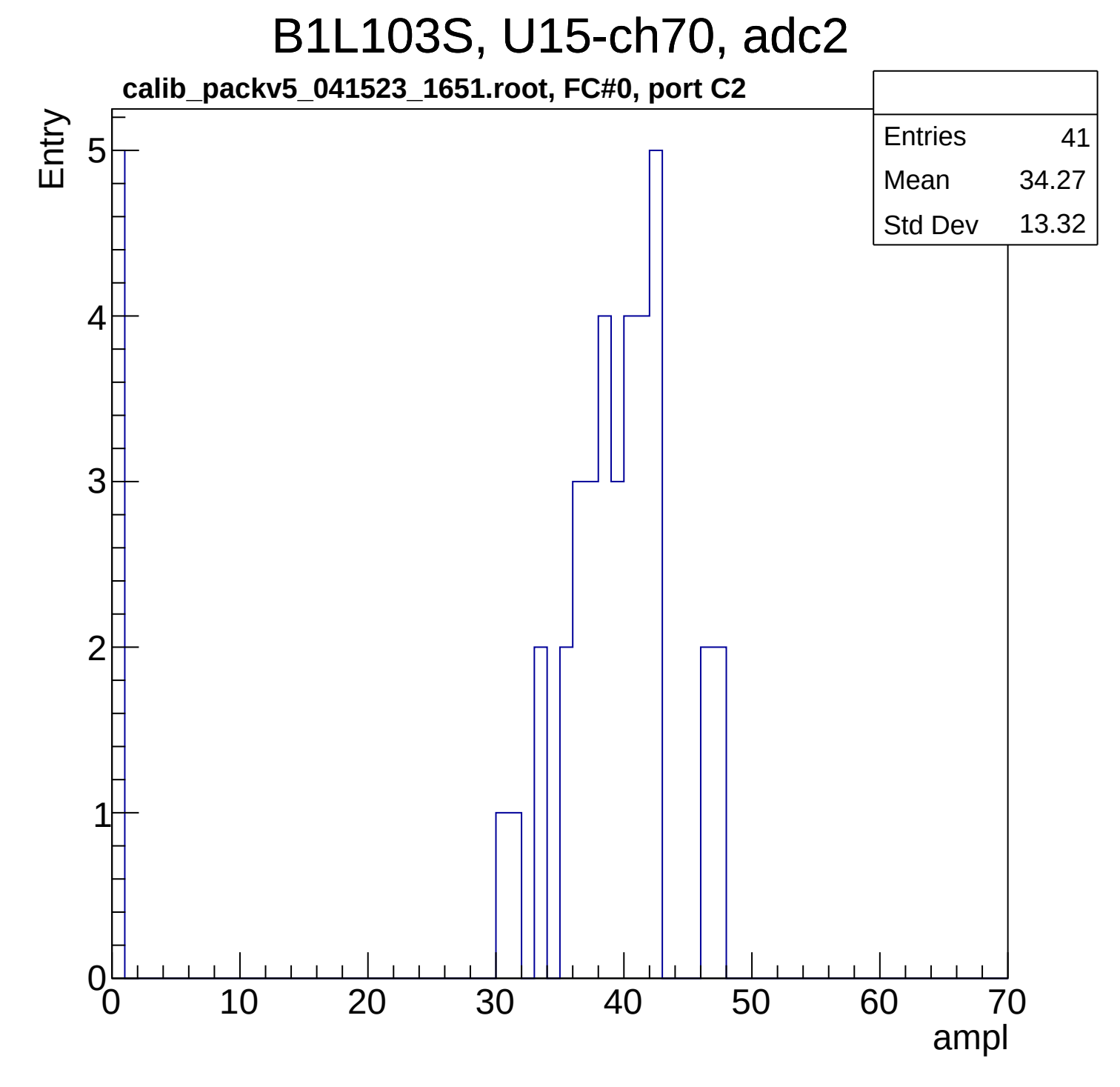
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch70, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 34.27
Std Dev 13.32
Entry
0
1
2
3
4
5
0
10
20
30
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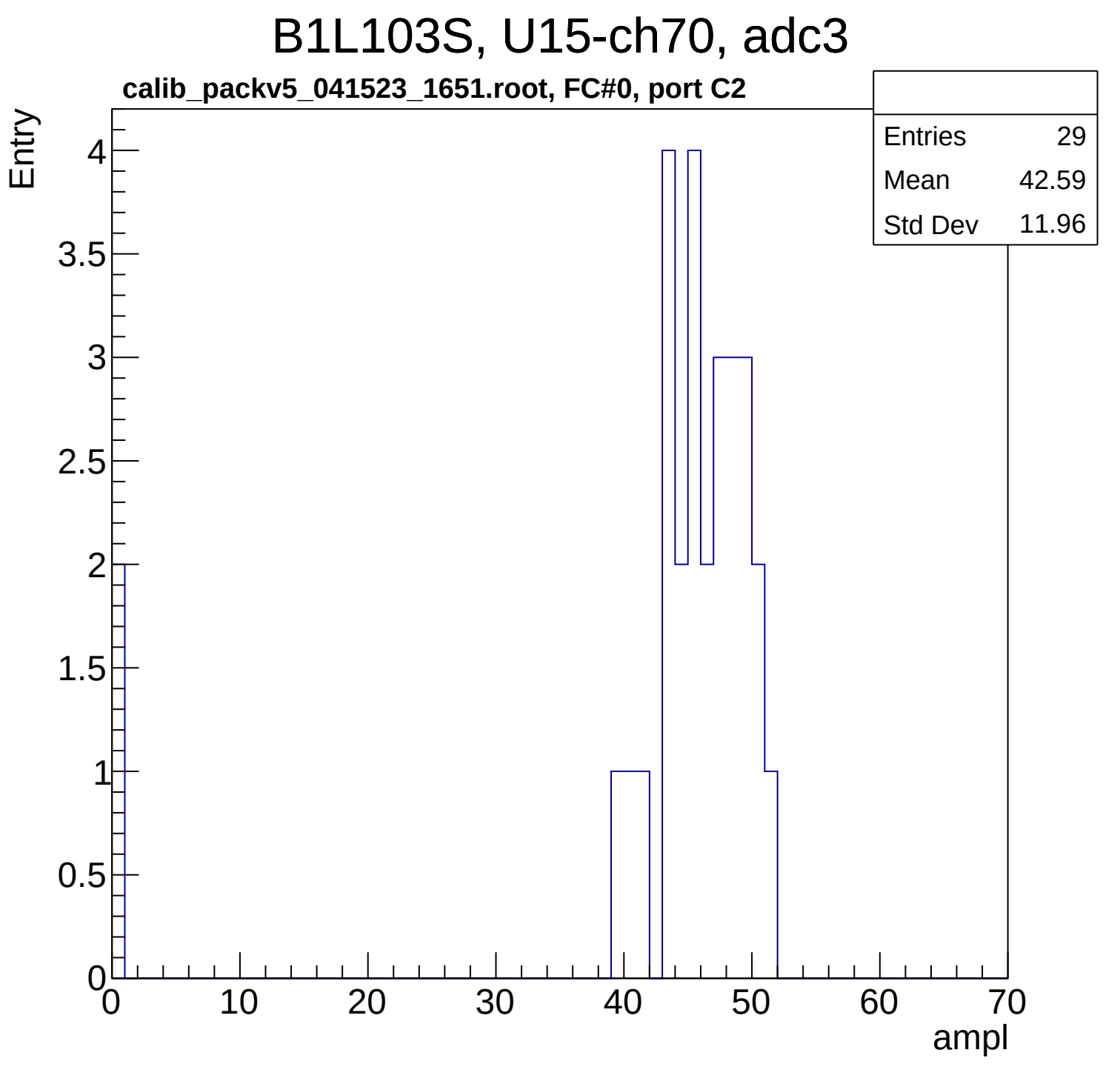
50
60
70
ampl


B1L103S, U15-ch70, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 42.59
Std Dev 11.96
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
10
20
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40
50
60
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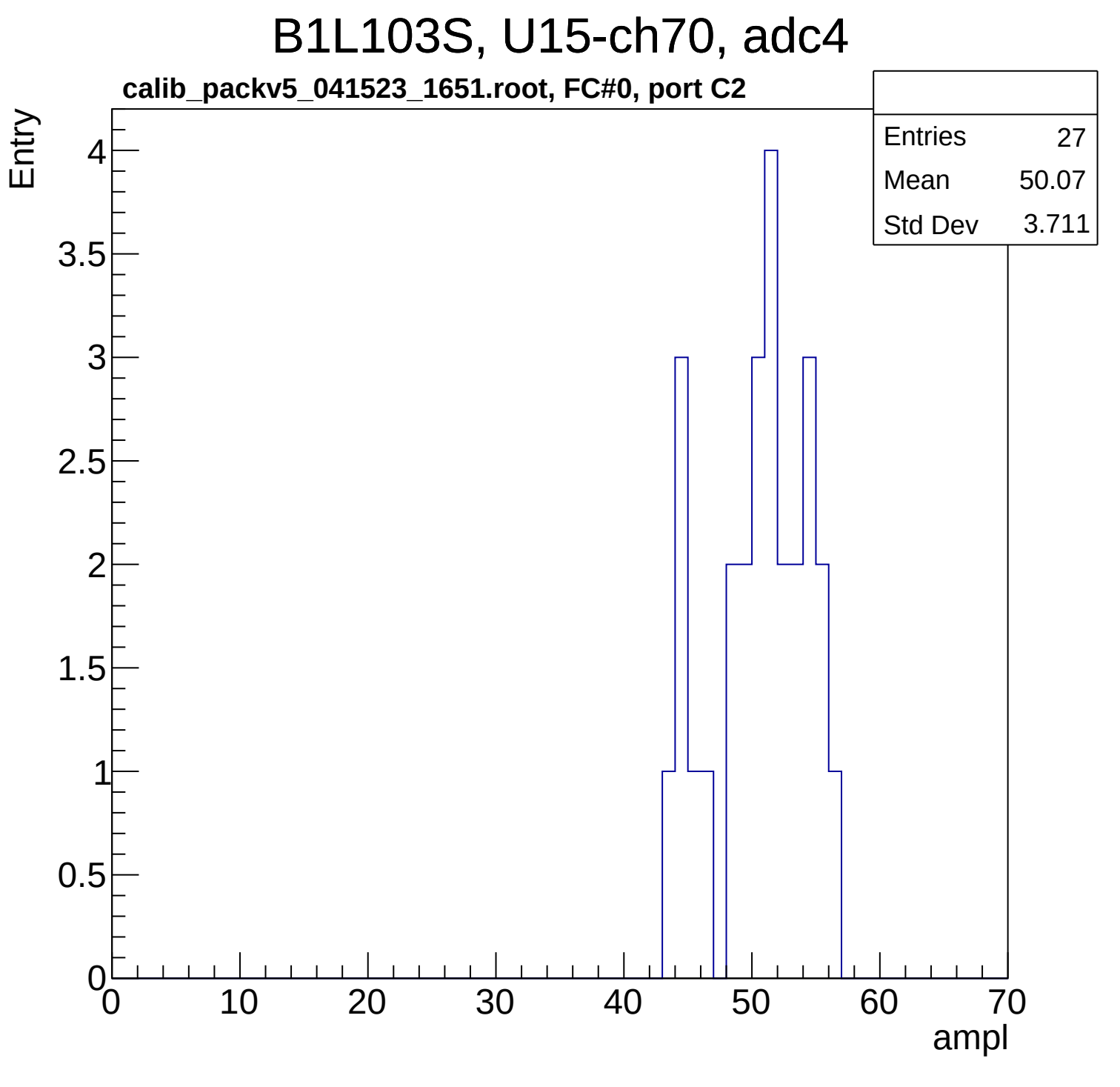
B1L103S, U15-ch70, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 50.07
Std Dev 3.711
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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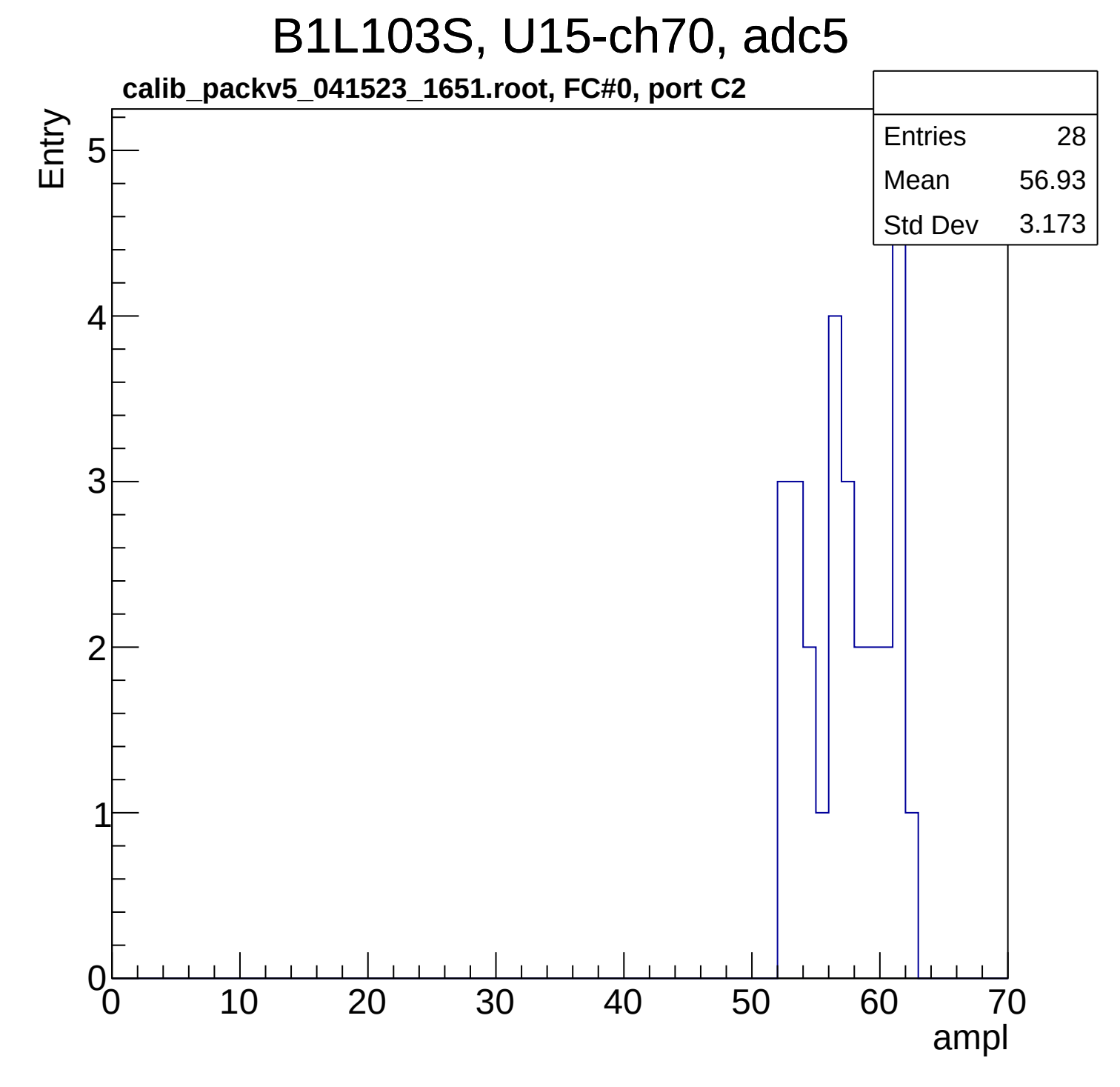
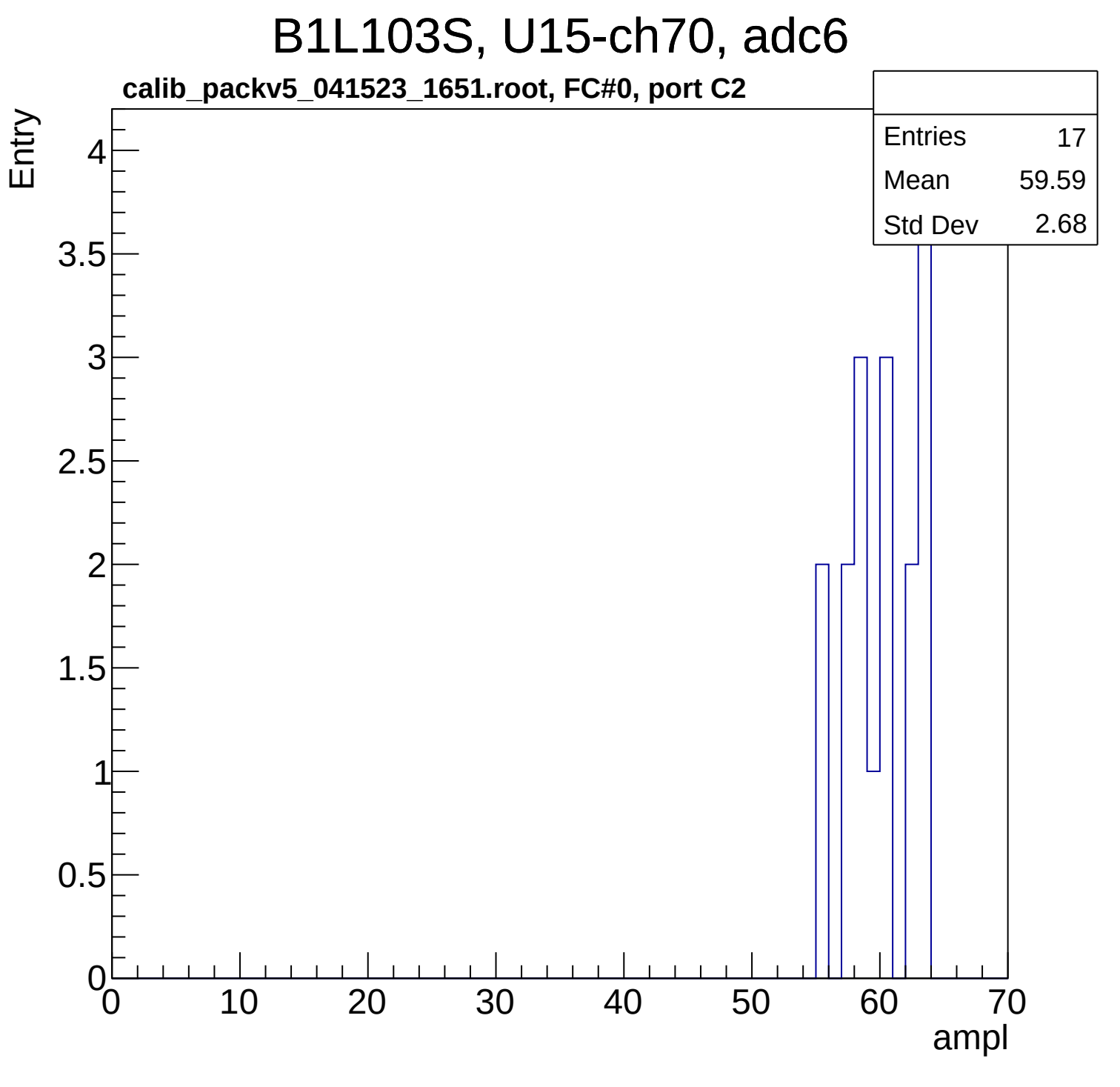

B1L103S, U15-ch70, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 56.93
Std Dev 3.173
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch70, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 59.59
Std Dev 2.68
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
10
20
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60
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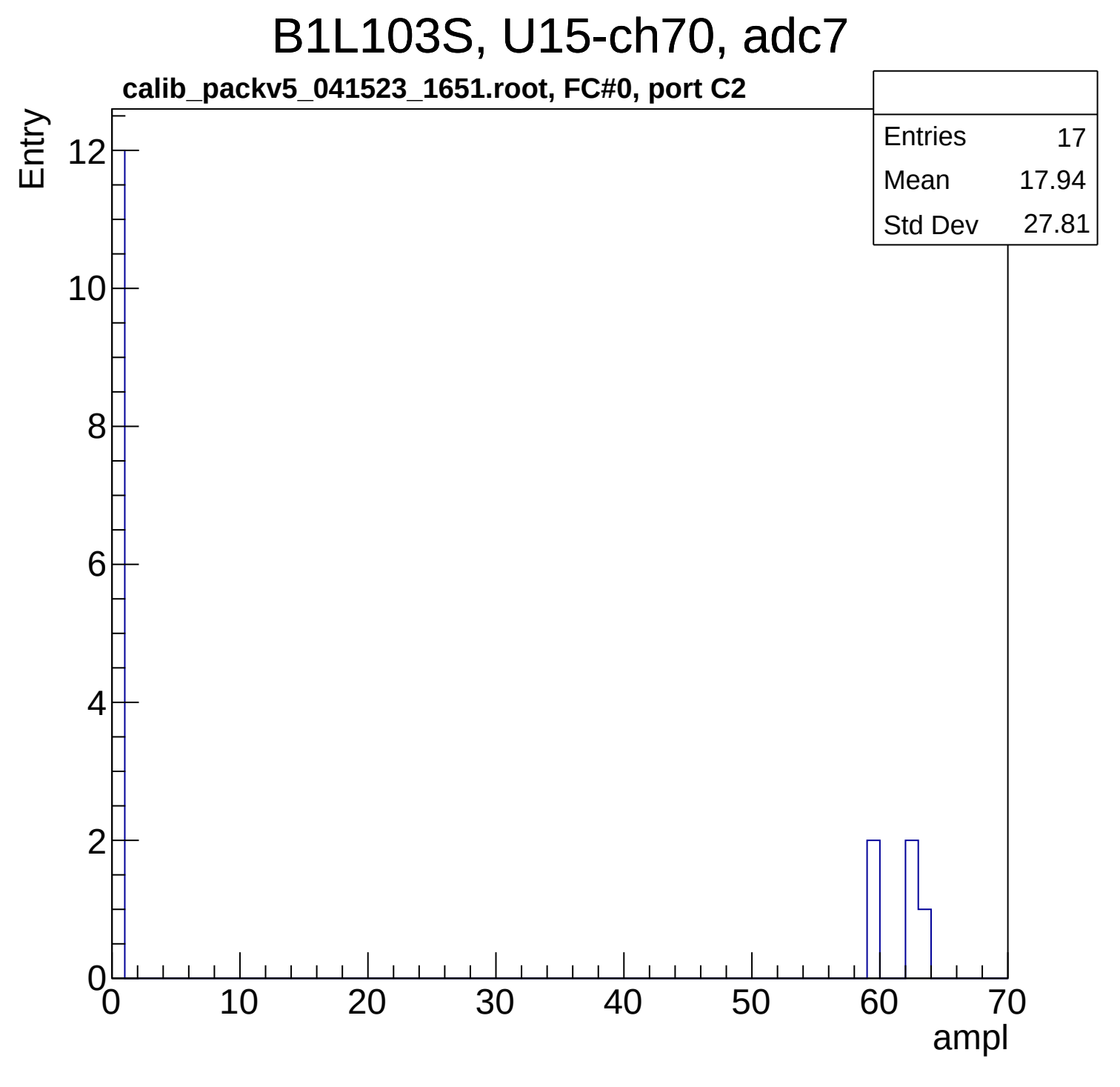
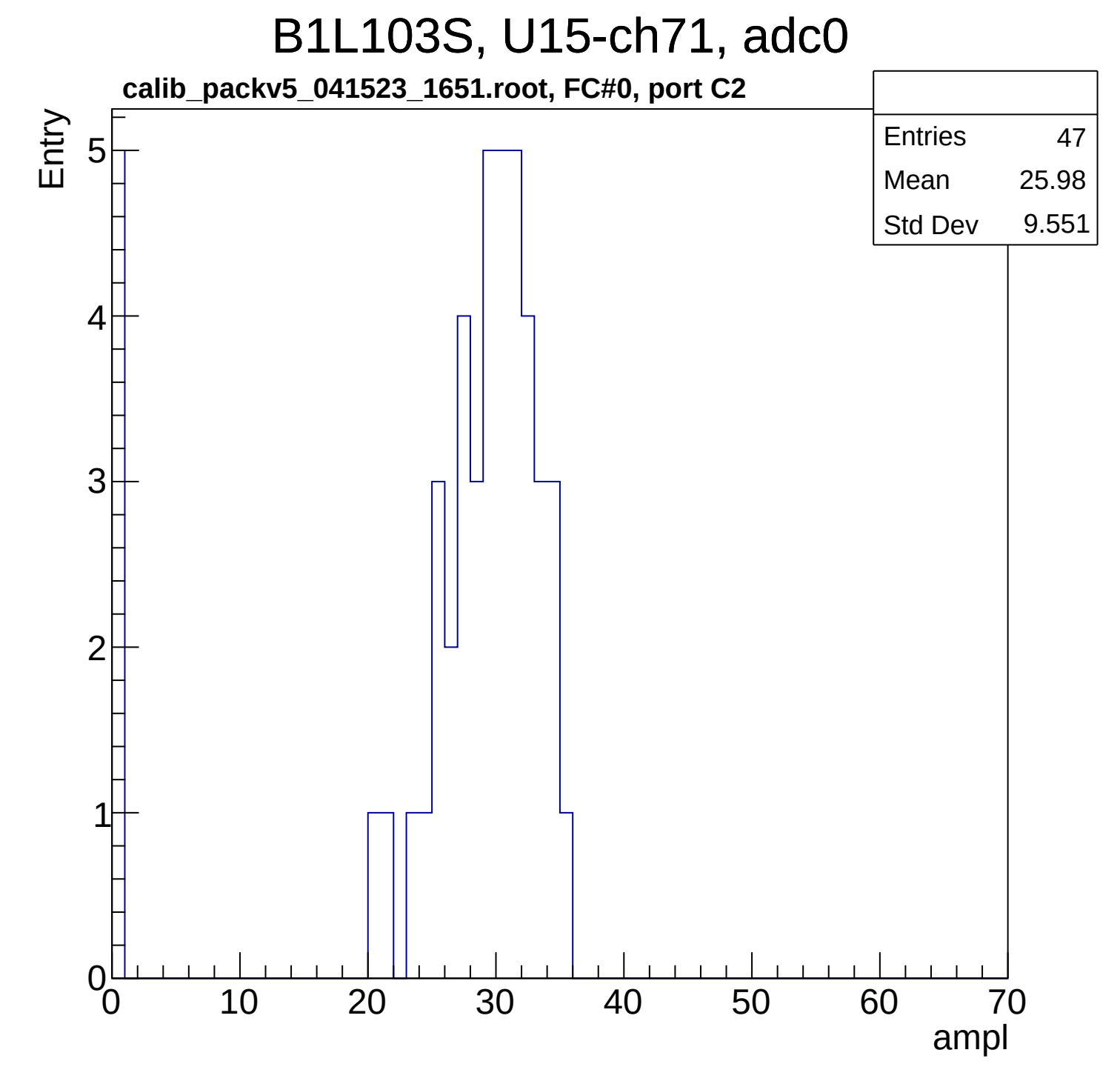
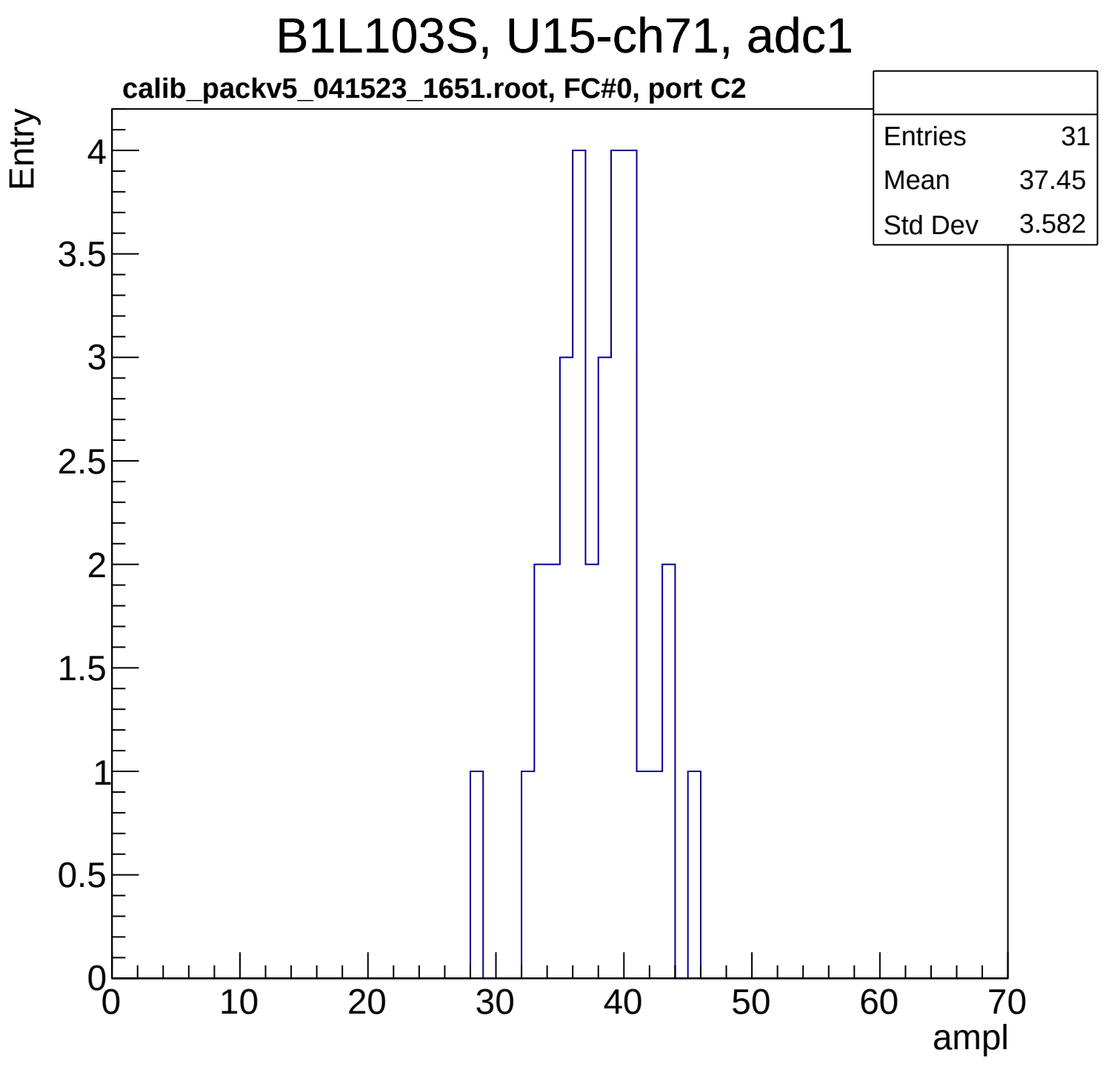

B1L103S, U15-ch70, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 17.94
Std Dev 27.81
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch71, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 25.98
Std Dev 9.551
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch71, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 37.45
Std Dev 3.582
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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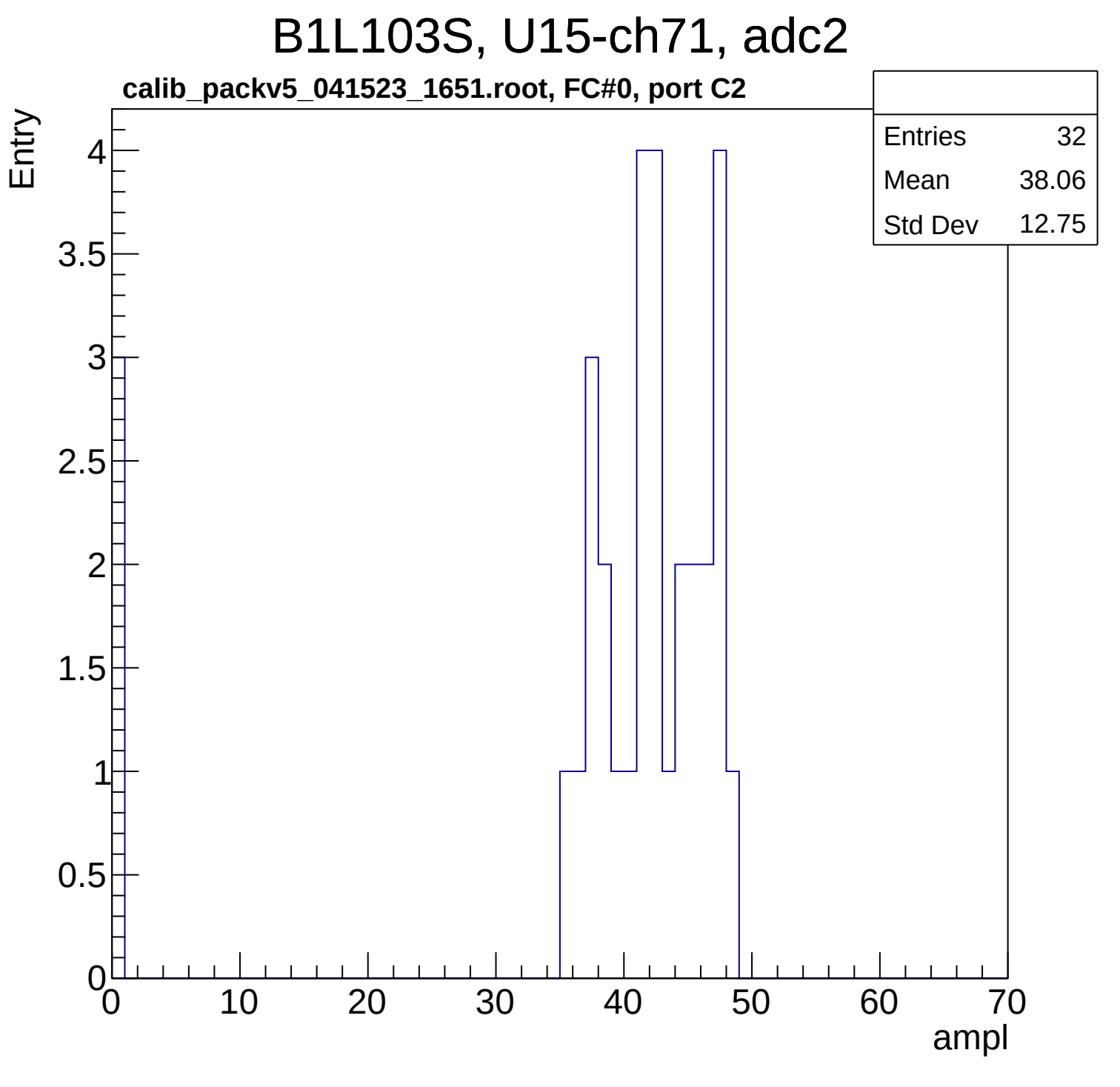
B1L103S, U15-ch71, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 38.06
Std Dev 12.75
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
10
20
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40
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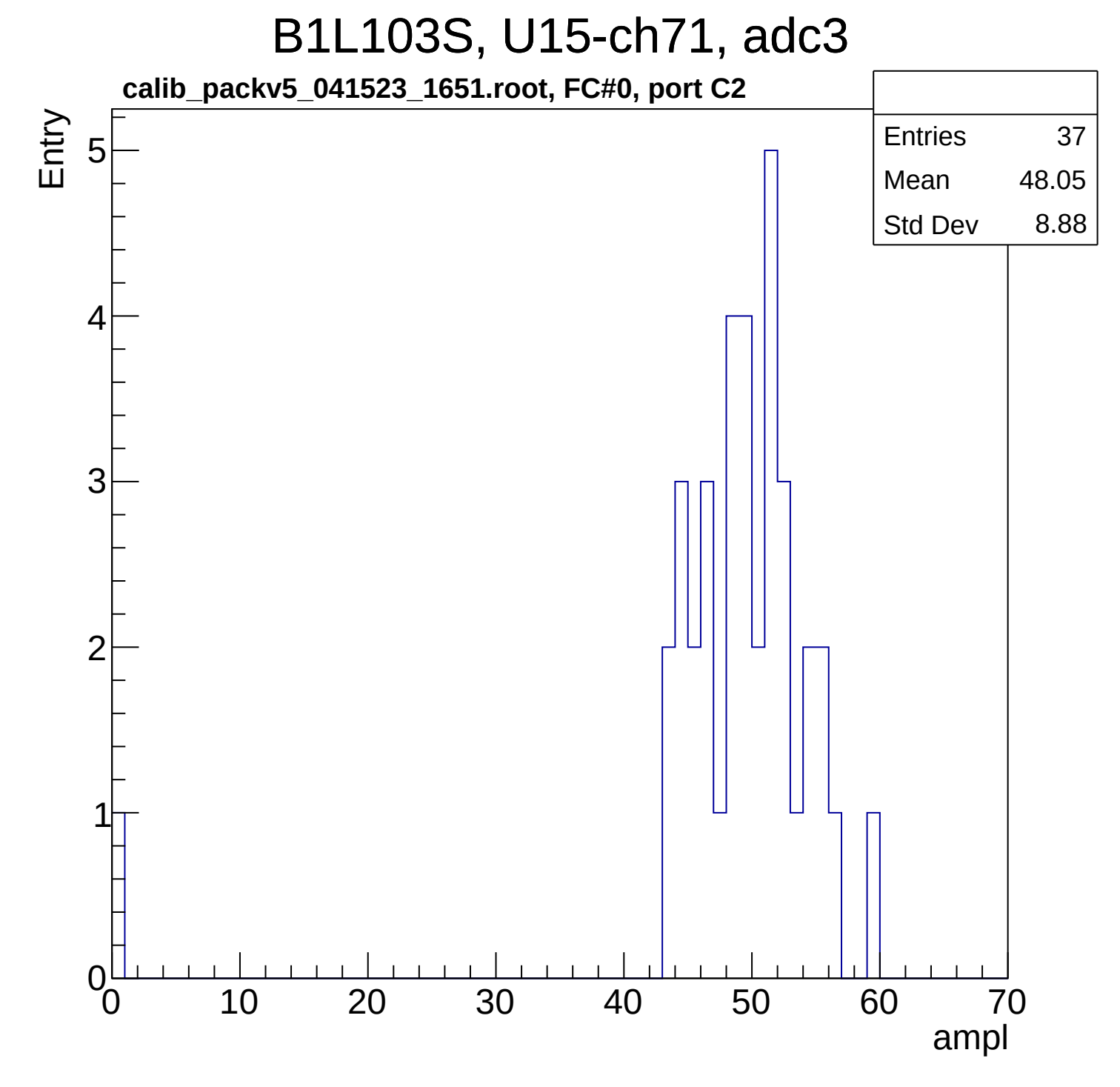
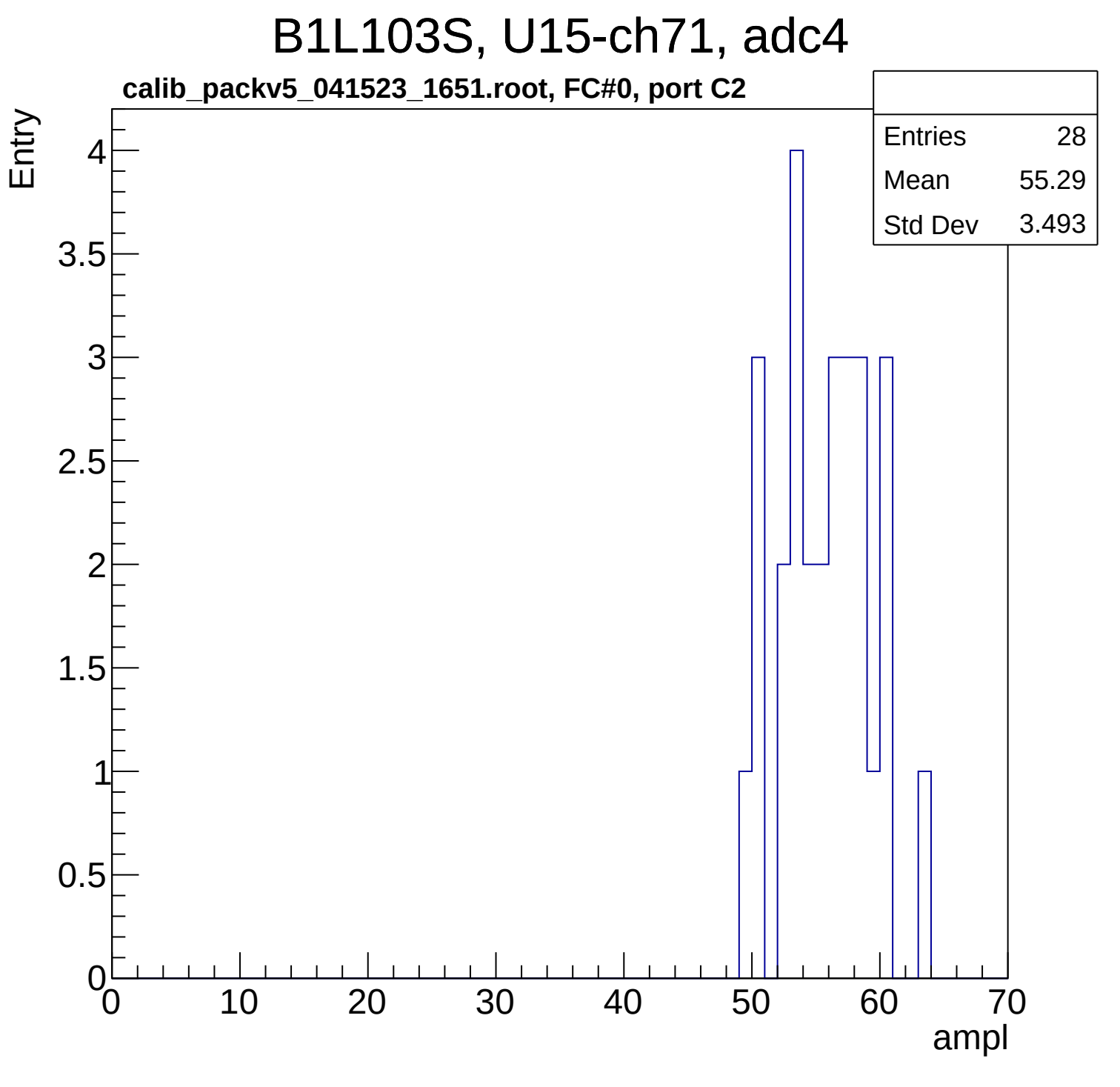
60
70


B1L103S, U15-ch71, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 48.05
Std Dev 8.88
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch71, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 55.29
Std Dev 3.493
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
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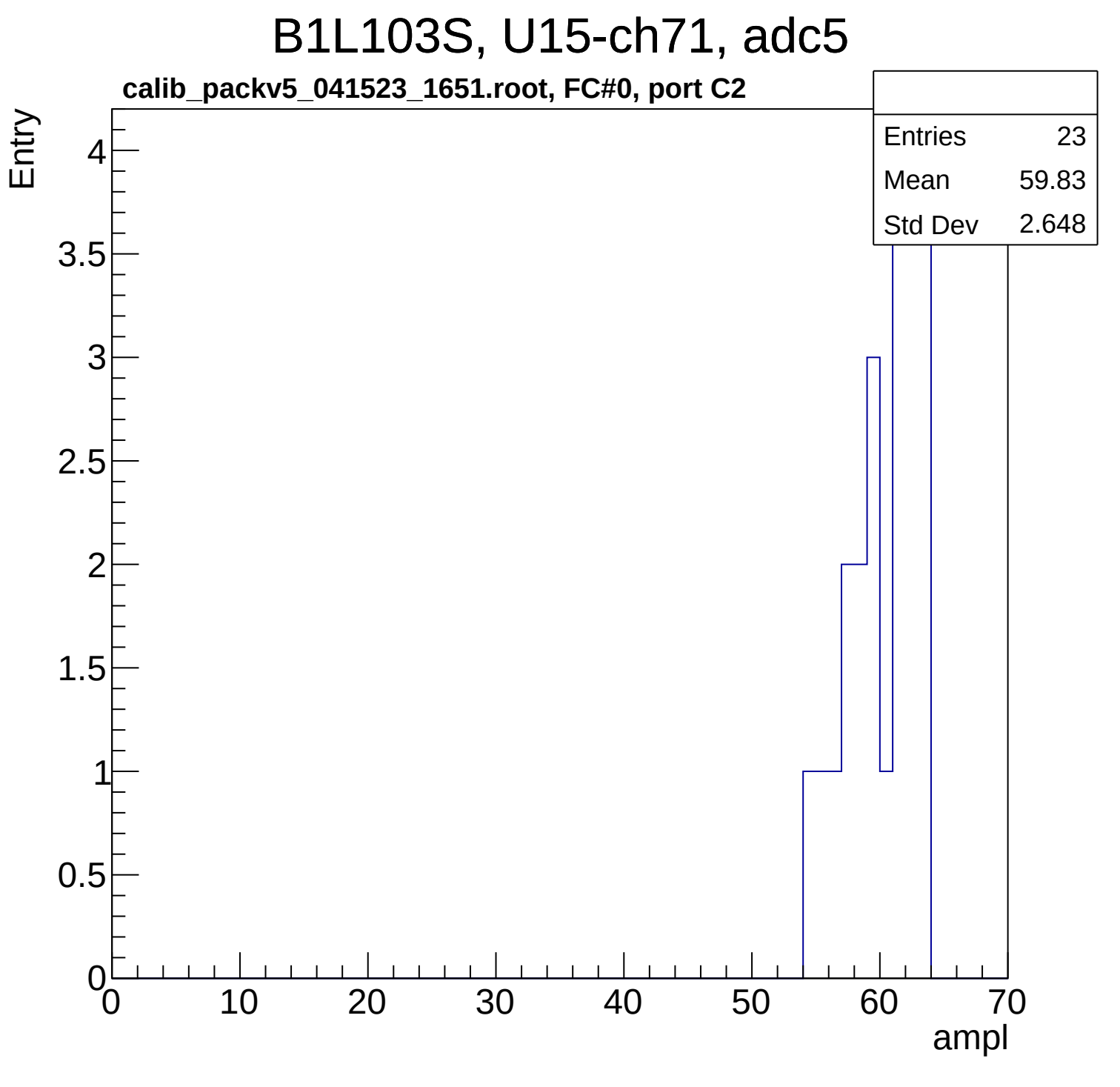
40
50
60
70


B1L103S, U15-ch71, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 59.83
Std Dev 2.648
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
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40
50
60
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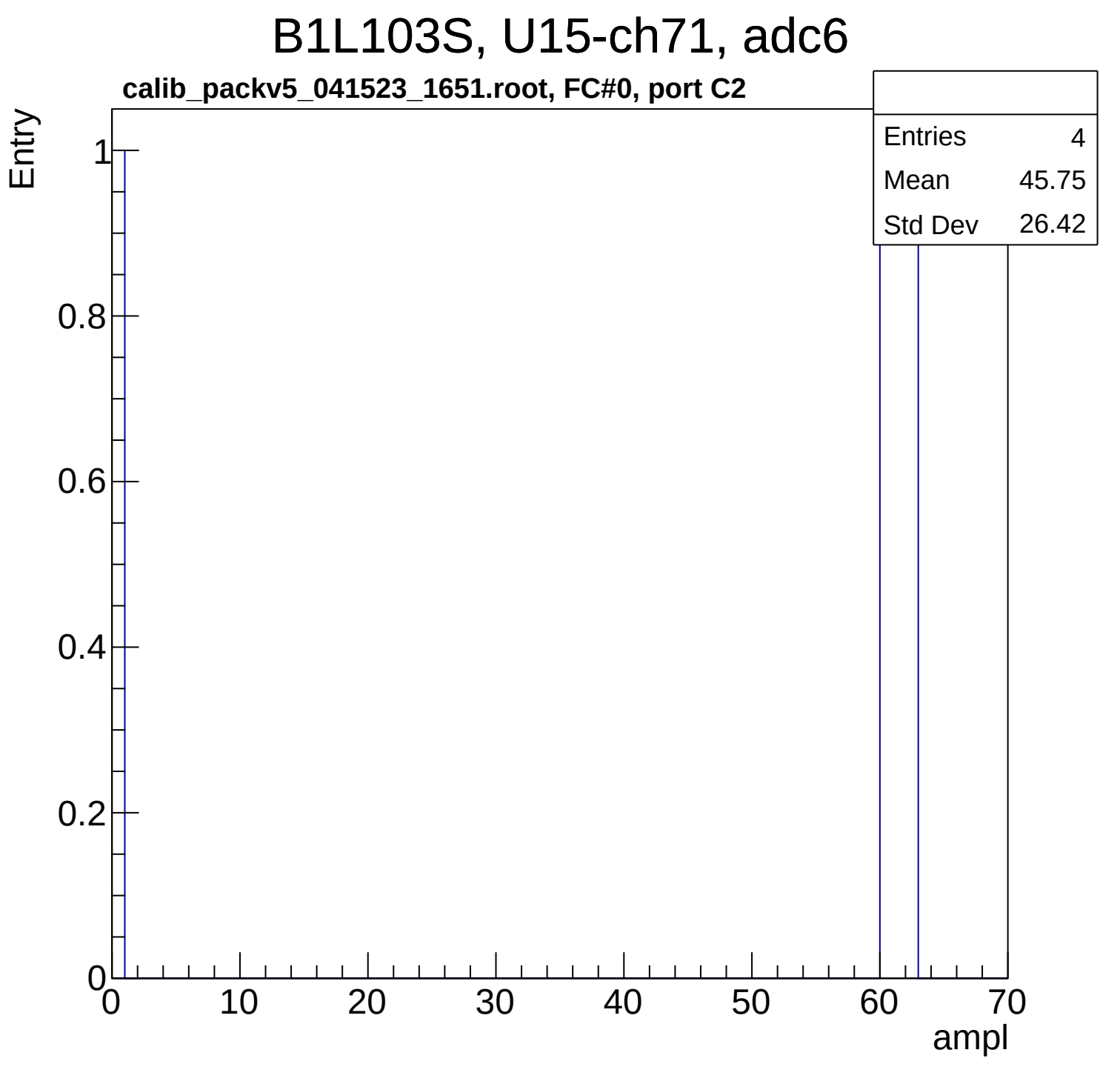
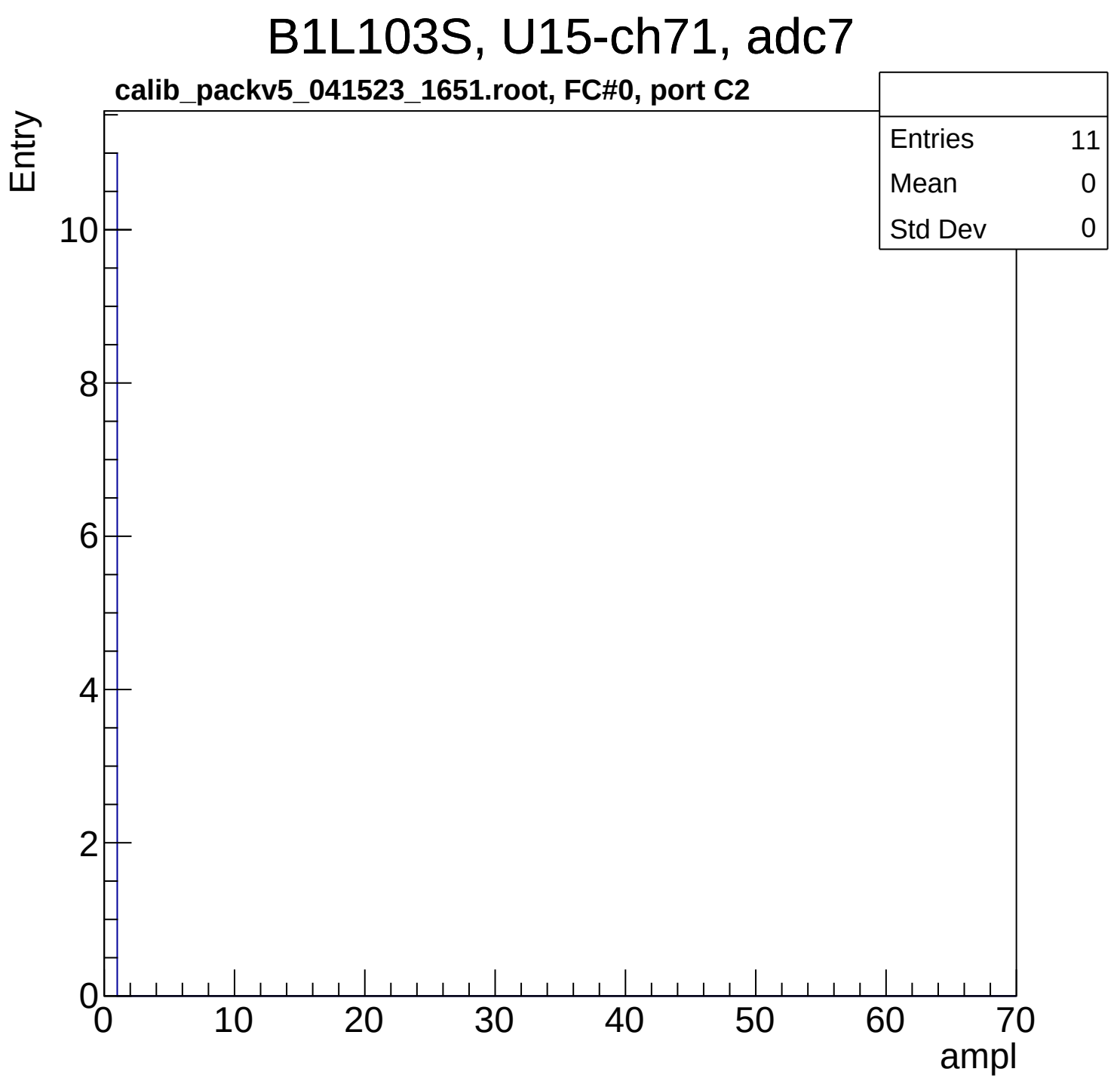
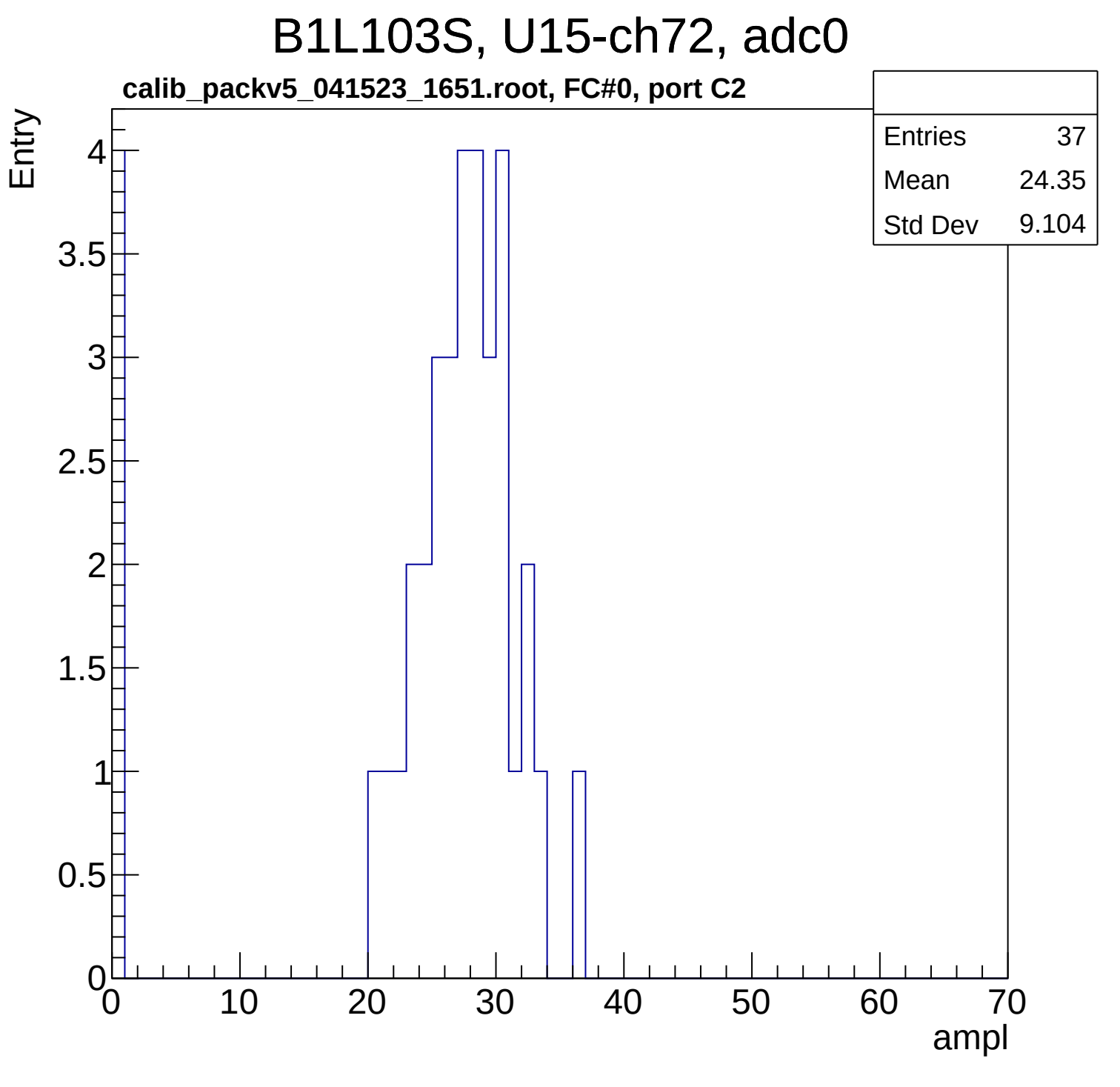
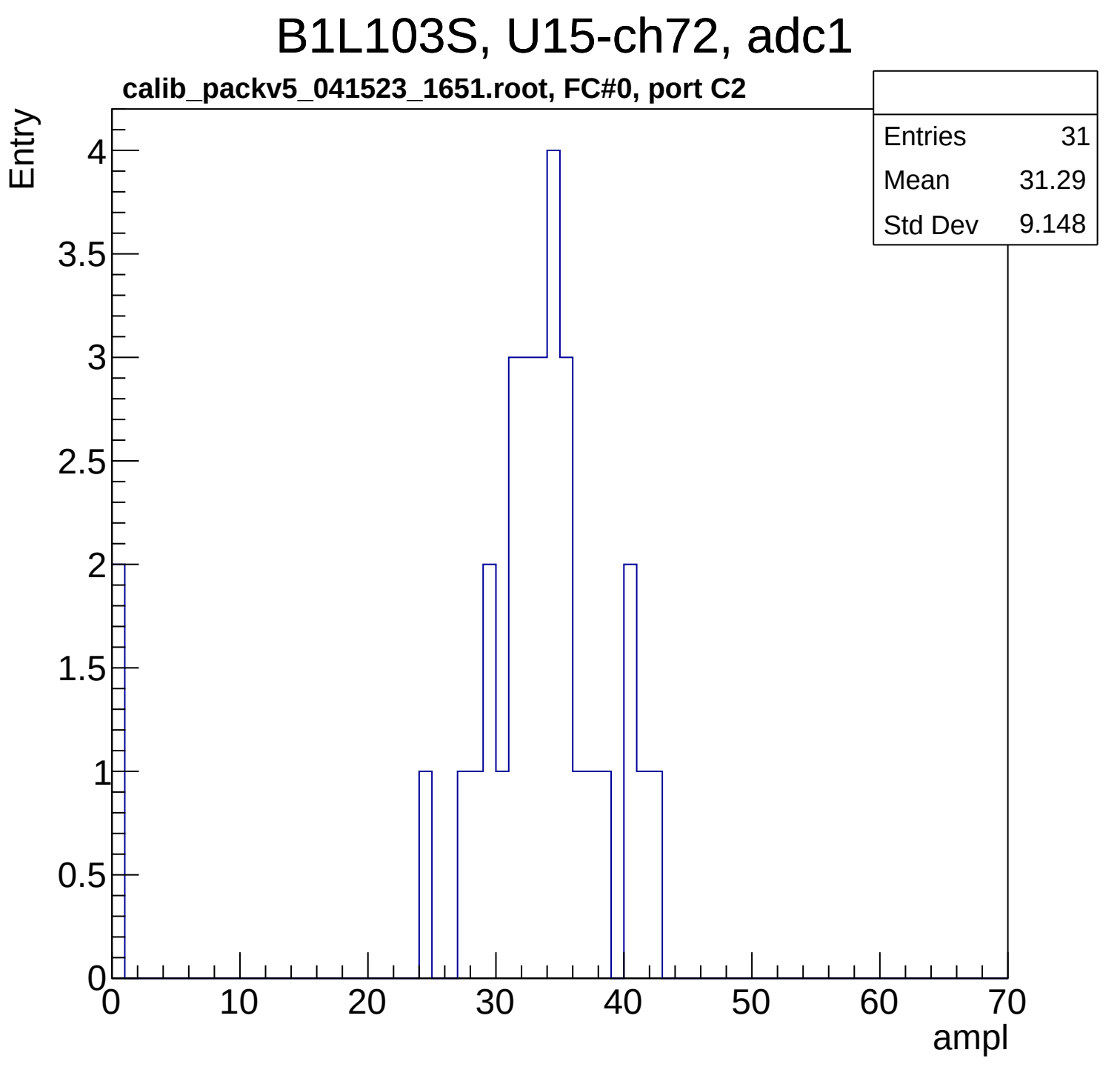
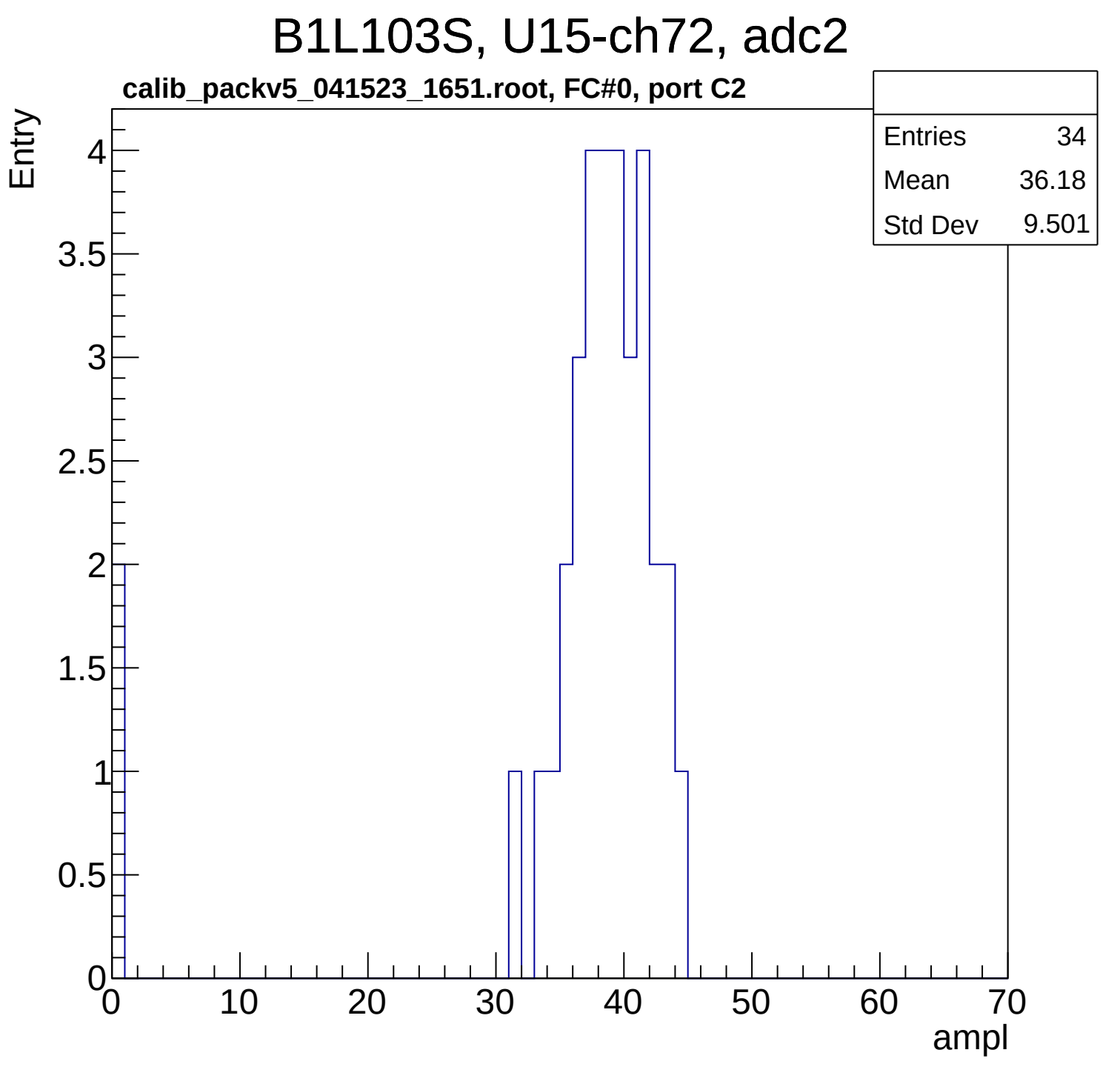
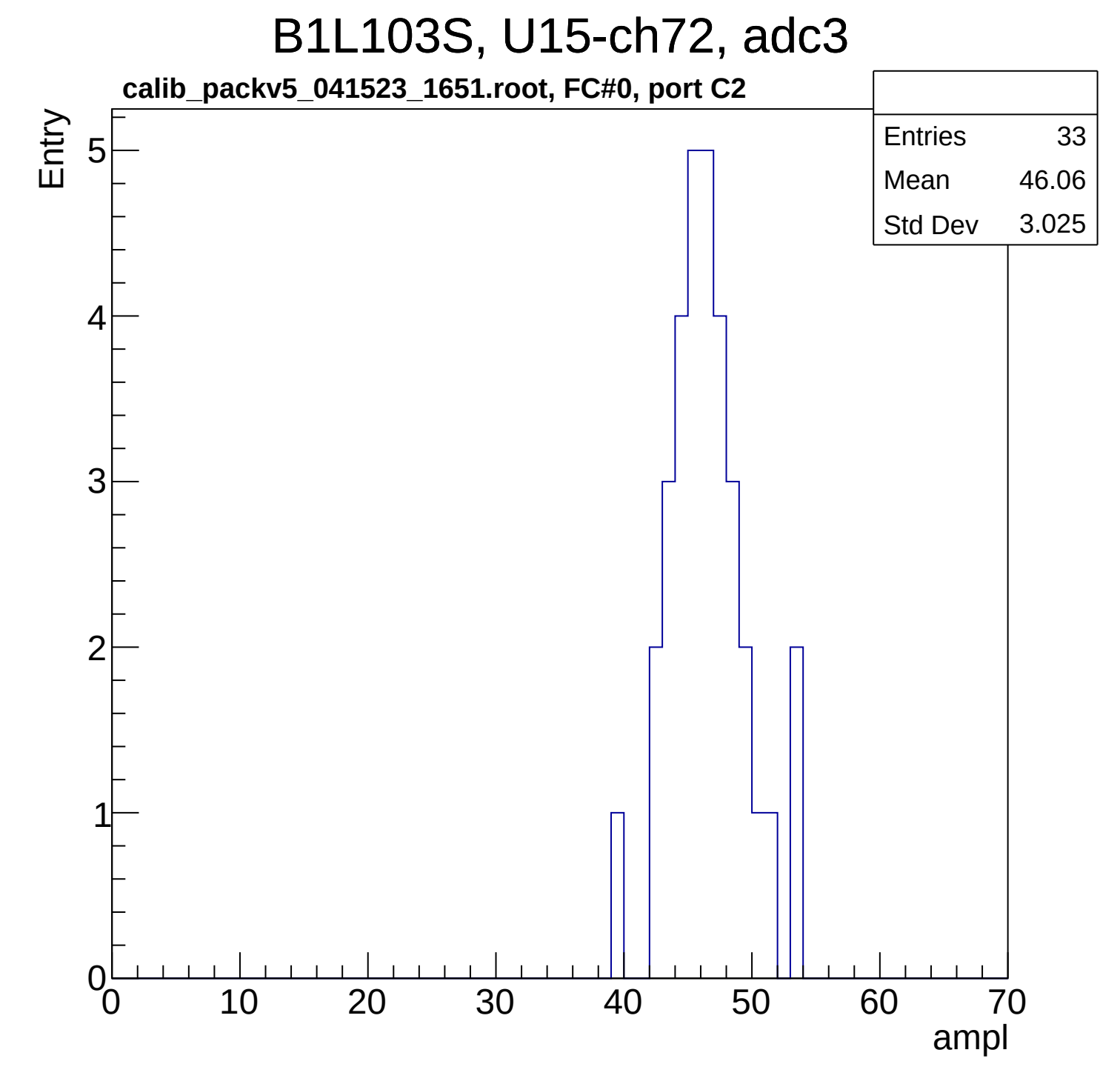

B1L103S, U15-ch71, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 45.75
Std Dev 26.42
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

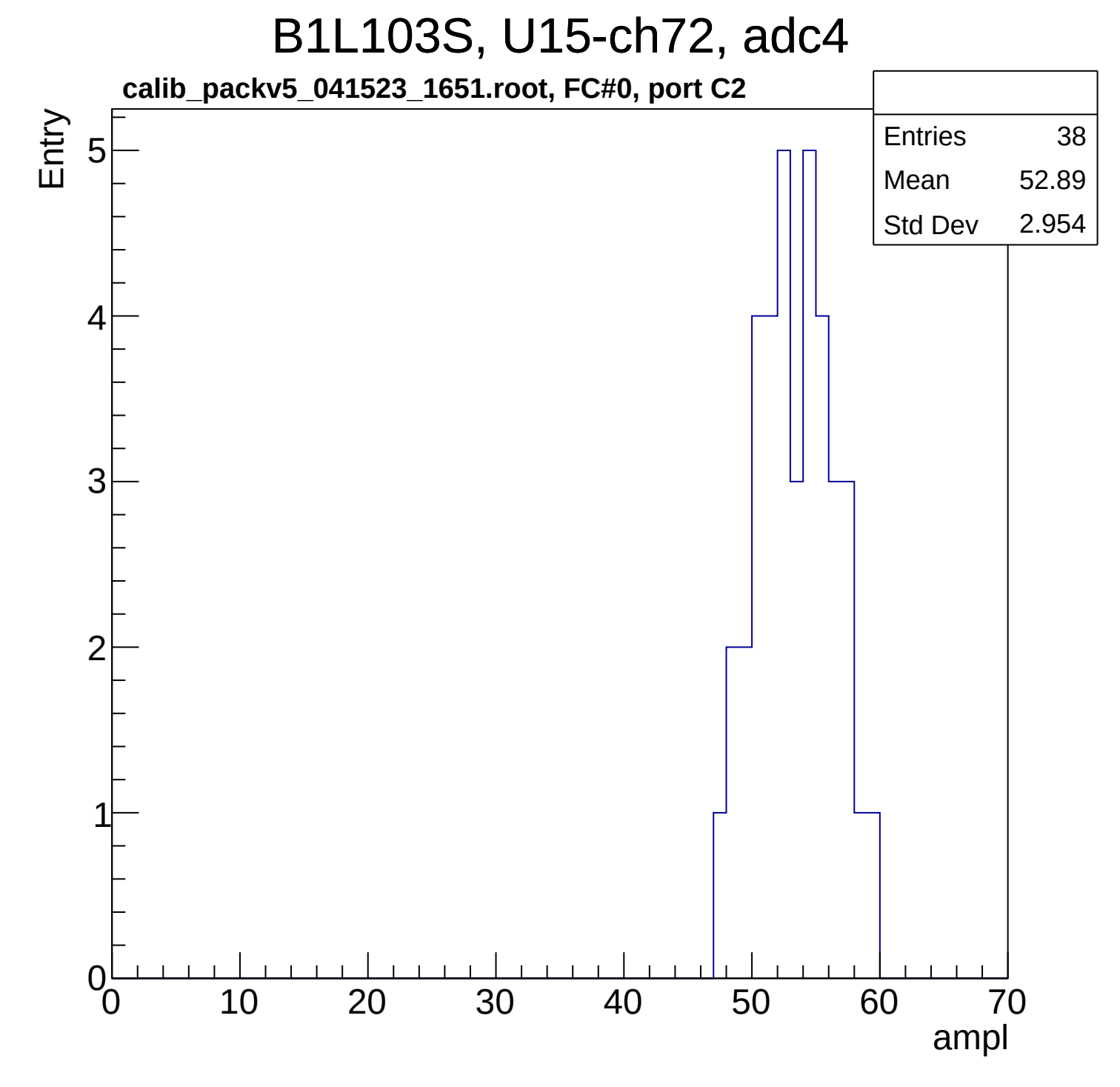

B1L103S, U15-ch71, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

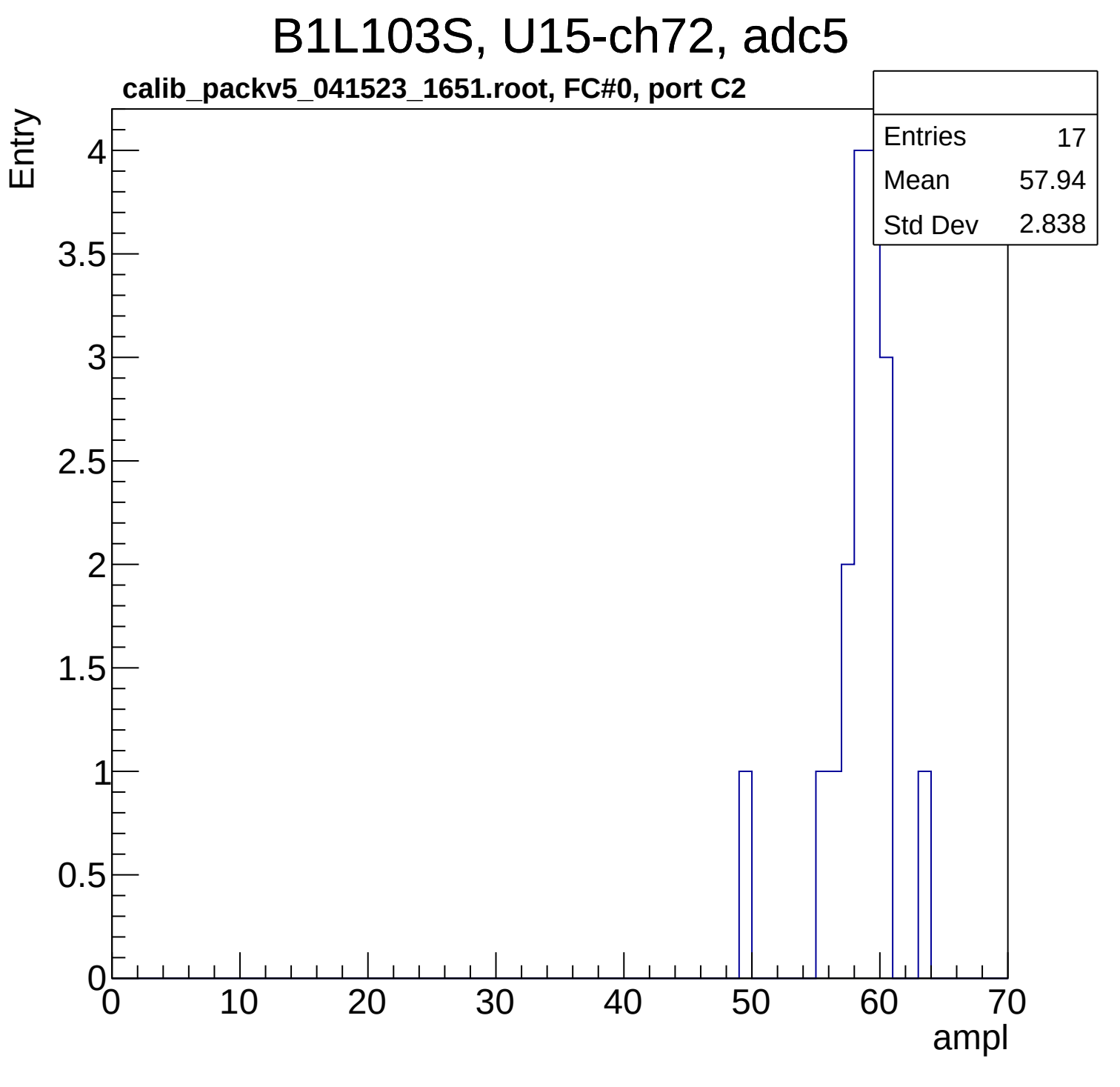

B1L103S, U15-ch72, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 24.35
Std Dev 9.104
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch72, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 31.29
Std Dev 9.148
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch72, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 36.18
Std Dev 9.501
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch72, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 46.06
Std Dev 3.025
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch72, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 52.89
Std Dev 2.954
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch72, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 57.94
Std Dev 2.838
Entry
ampl
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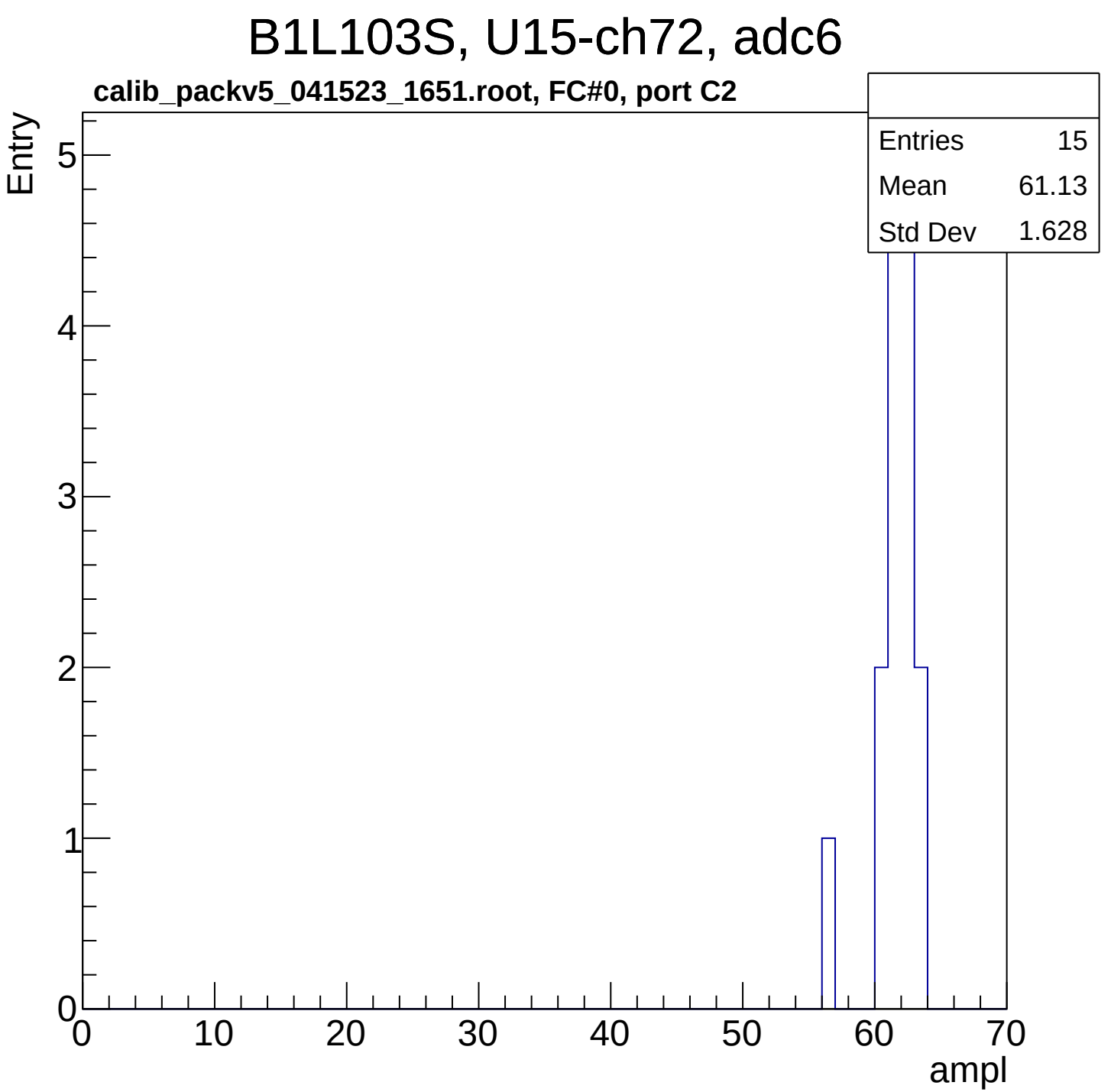
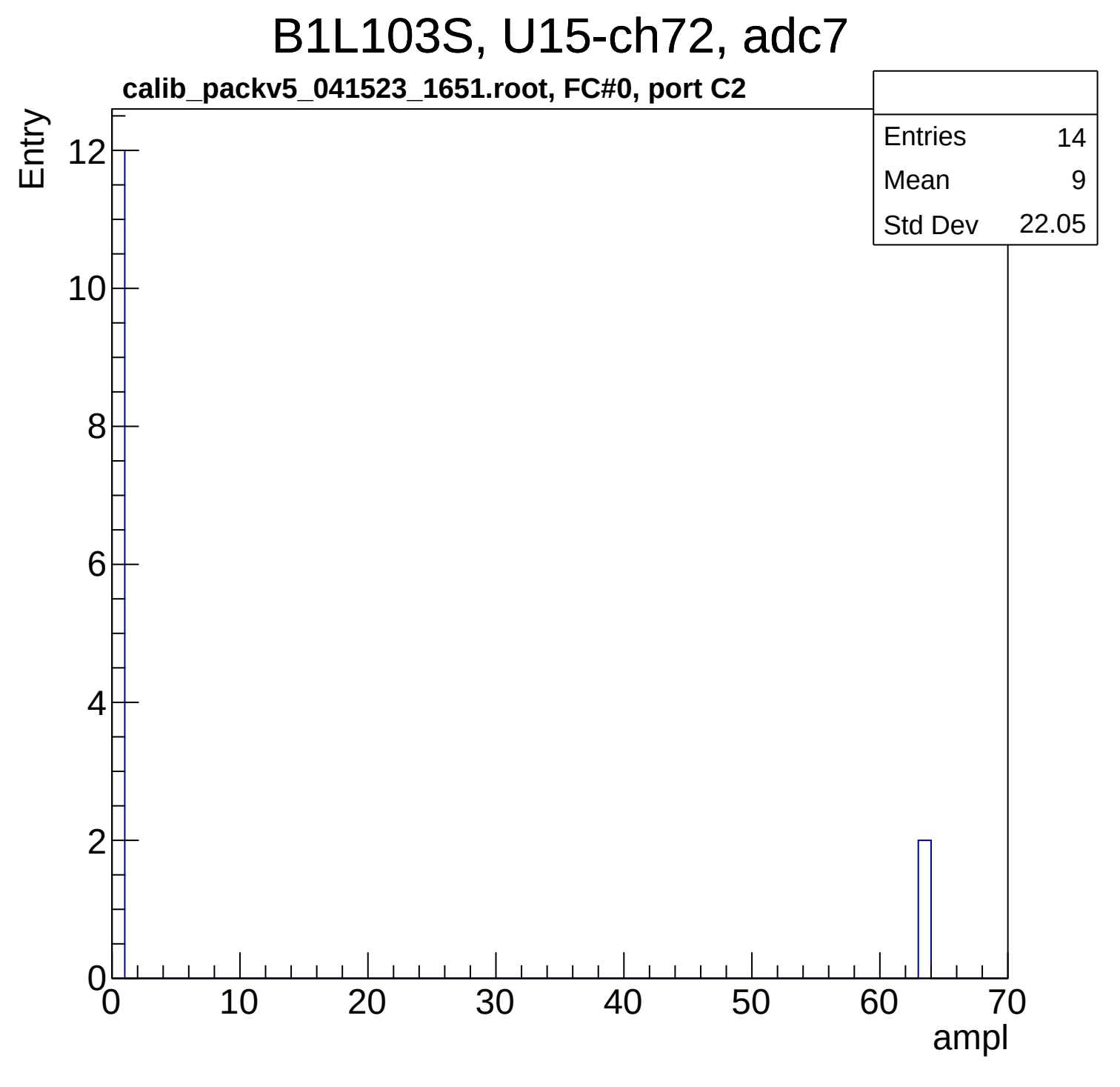
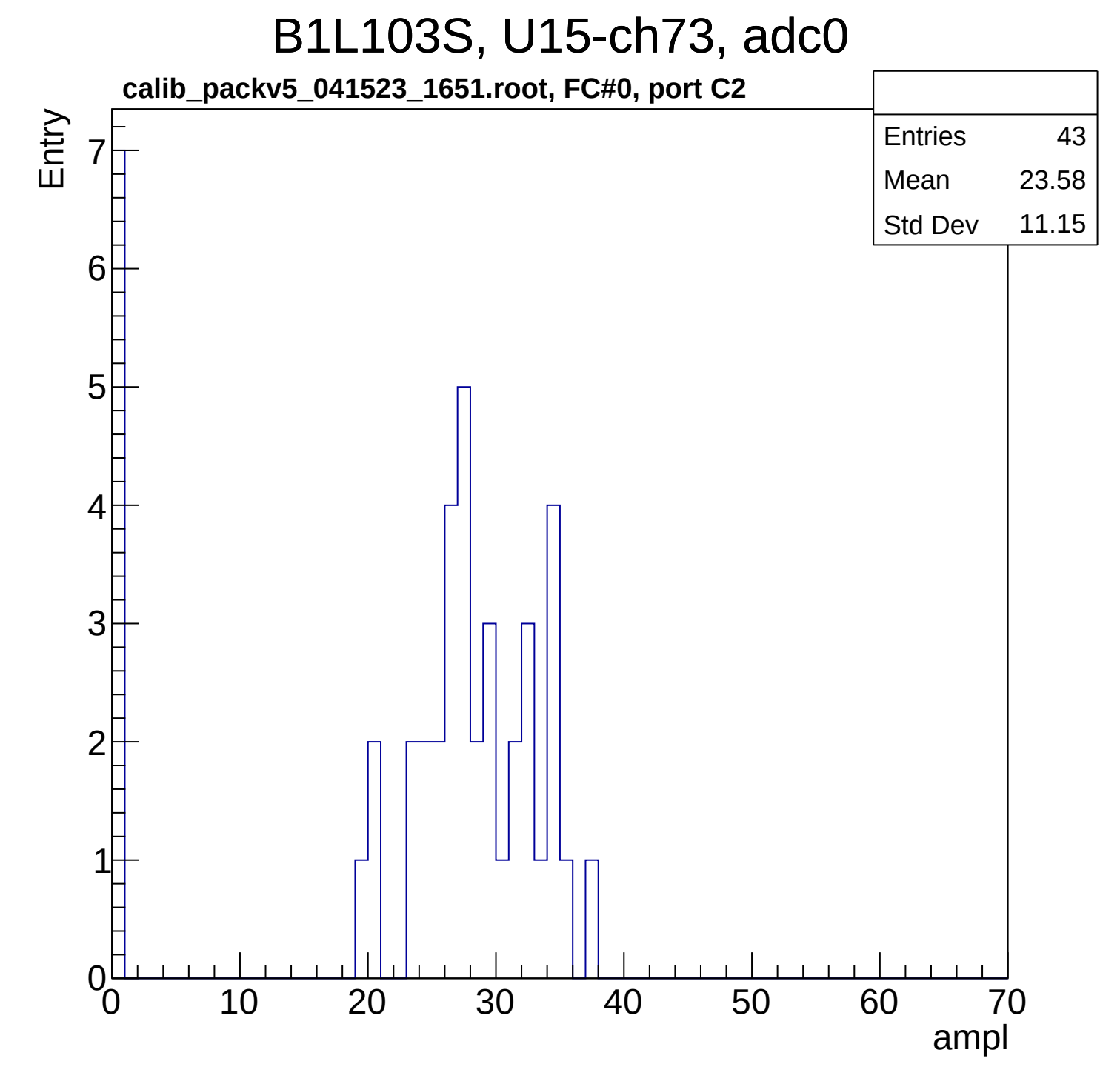
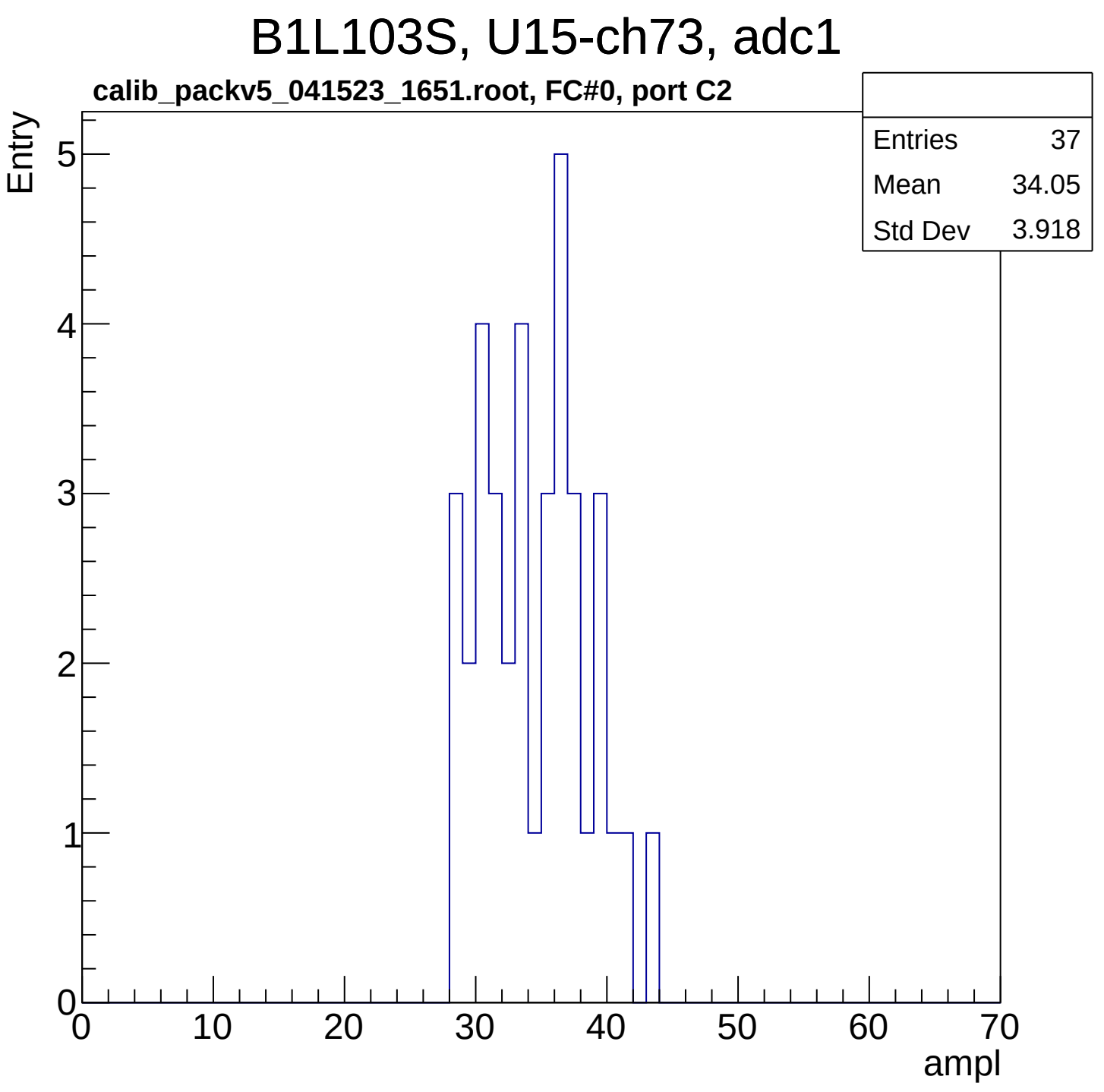
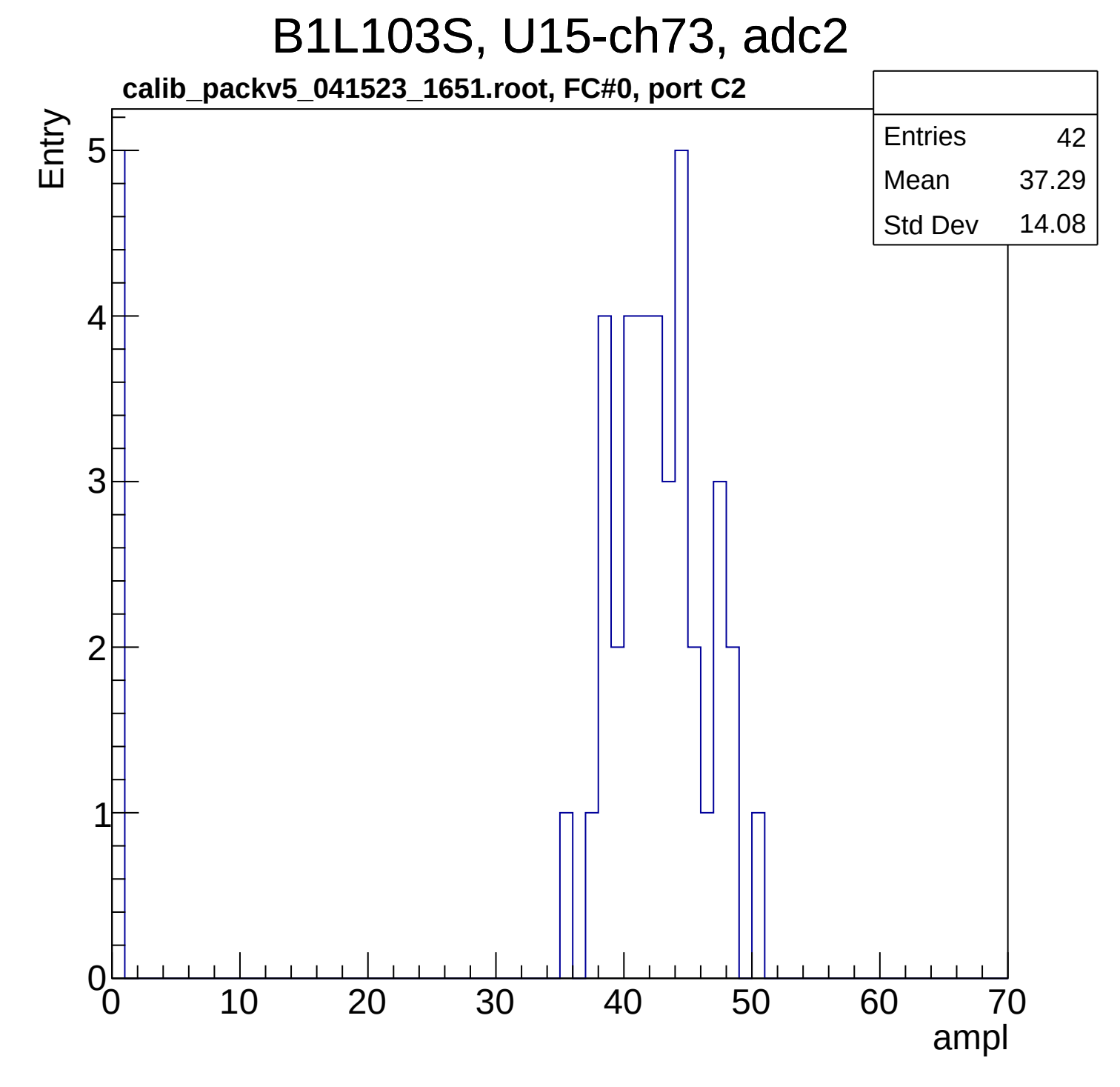
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

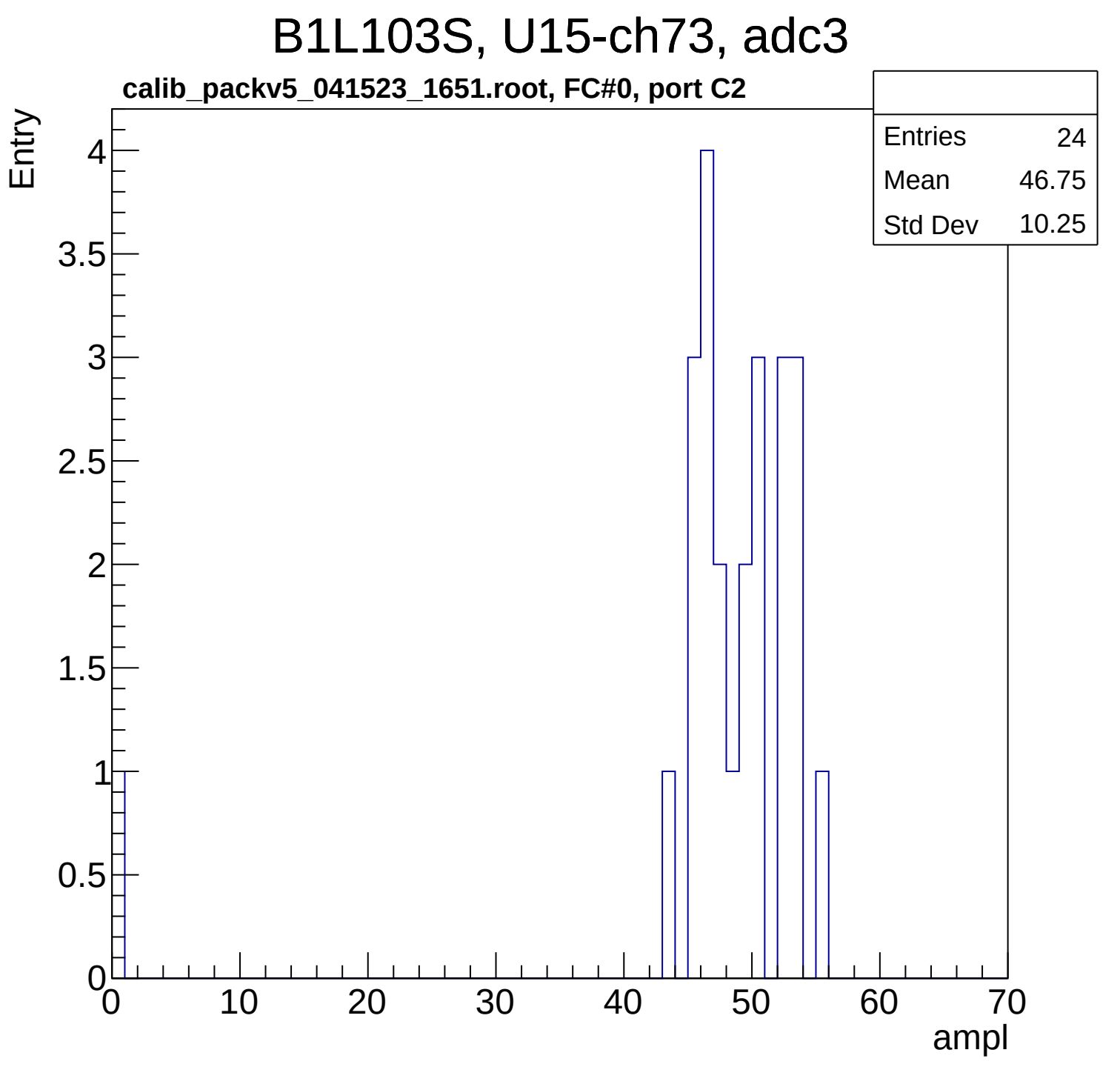

B1L103S, U15-ch72, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.13
Std Dev 1.628
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

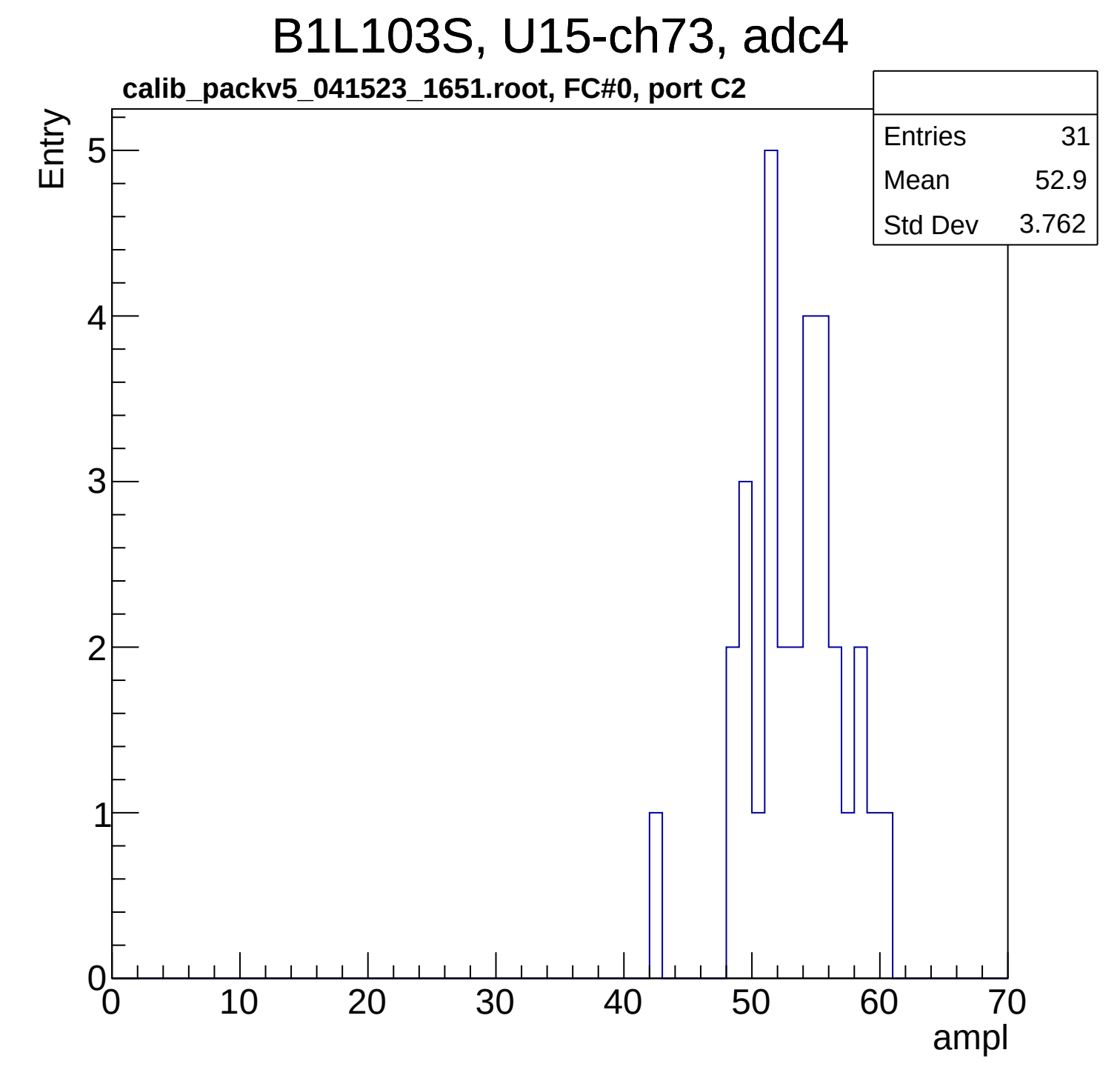

B1L103S, U15-ch72, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 9
Std Dev 22.05
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

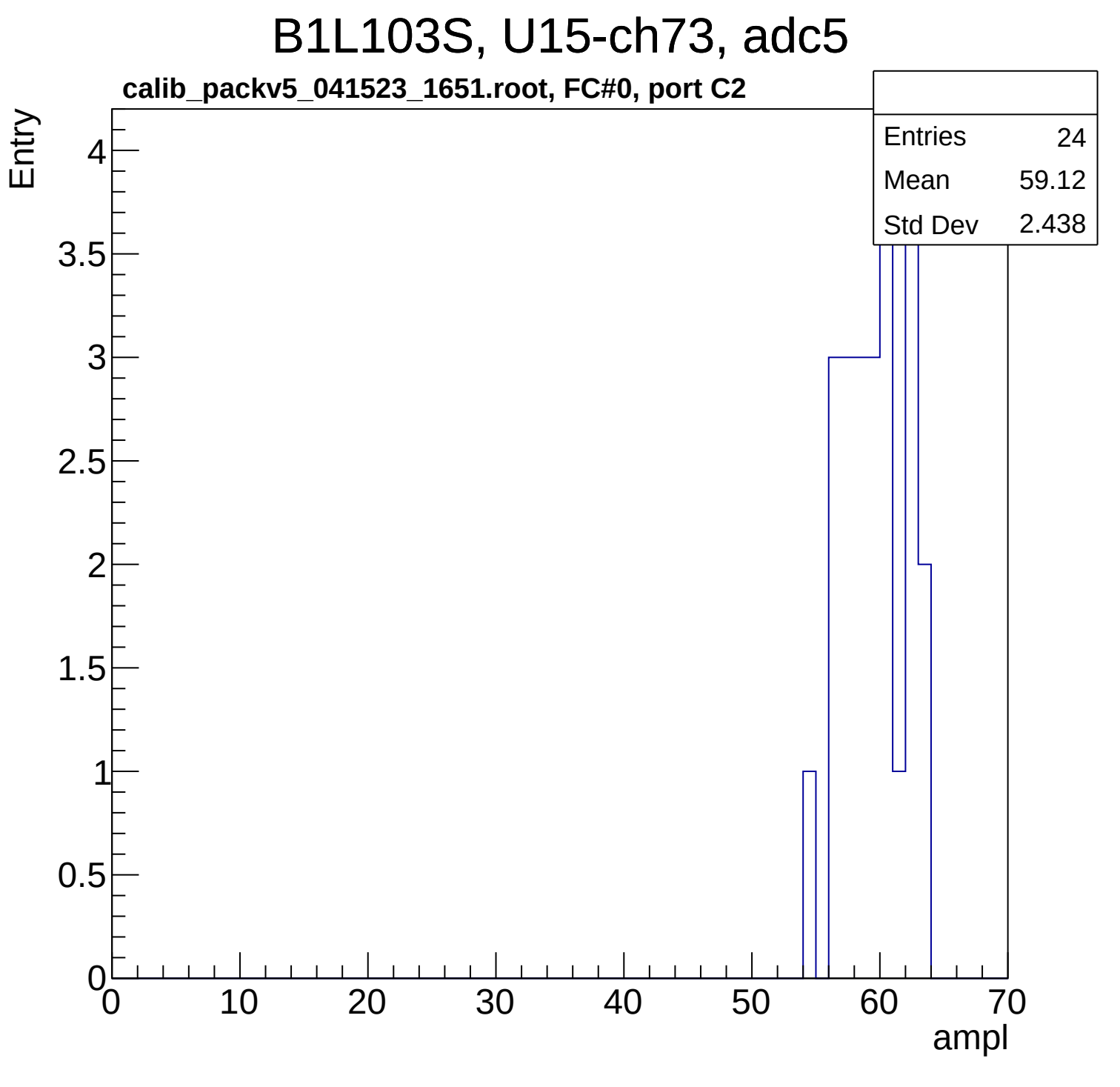

B1L103S, U15-ch73, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 23.58
Std Dev 11.15
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U15-ch73, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 34.05
Std Dev 3.918
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch73, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 37.29
Std Dev 14.08
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch73, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 46.75
Std Dev 10.25
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch73, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 52.9
Std Dev 3.762
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch73, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 59.12
Std Dev 2.438
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
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20
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40
50
60
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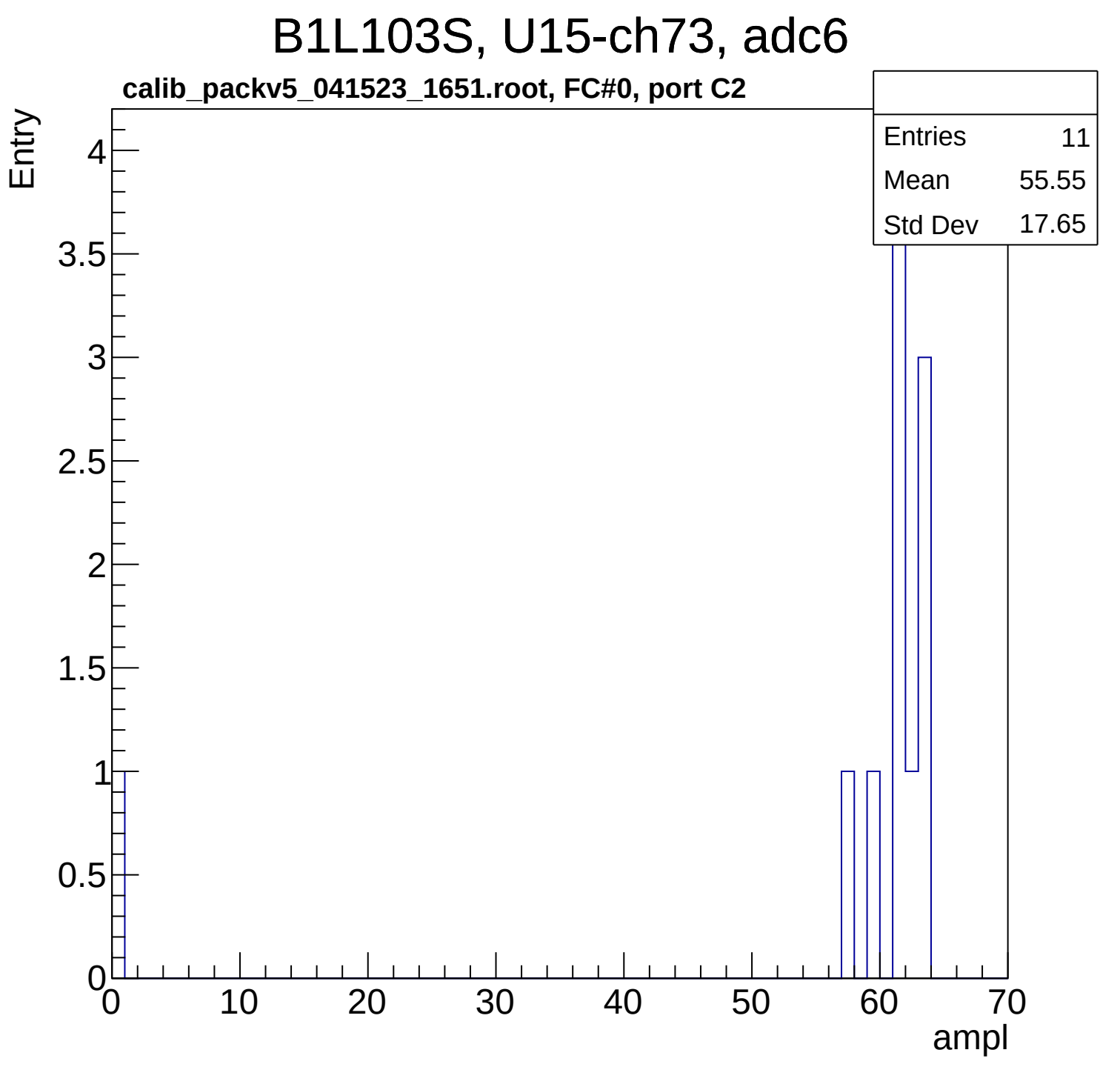
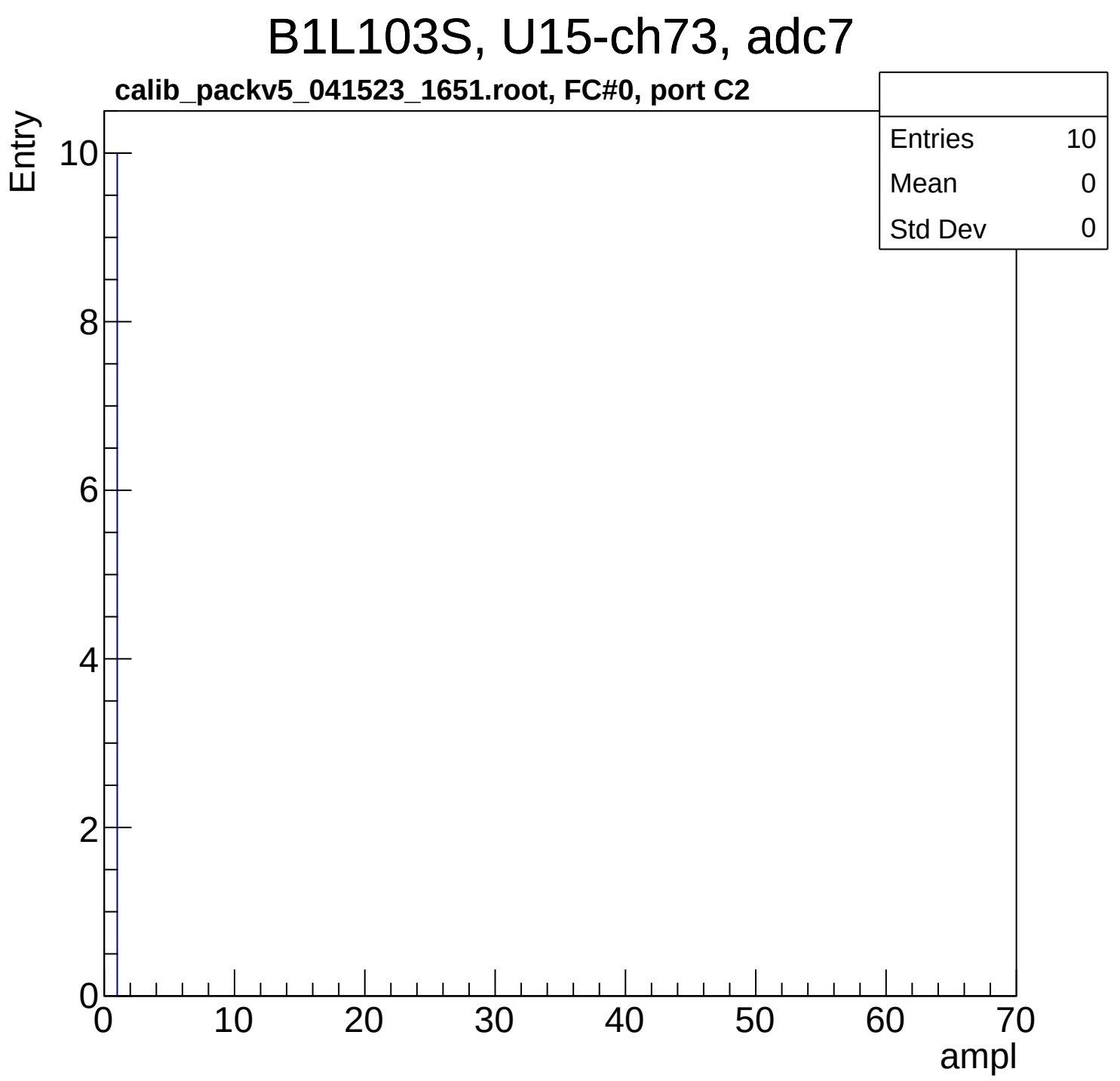
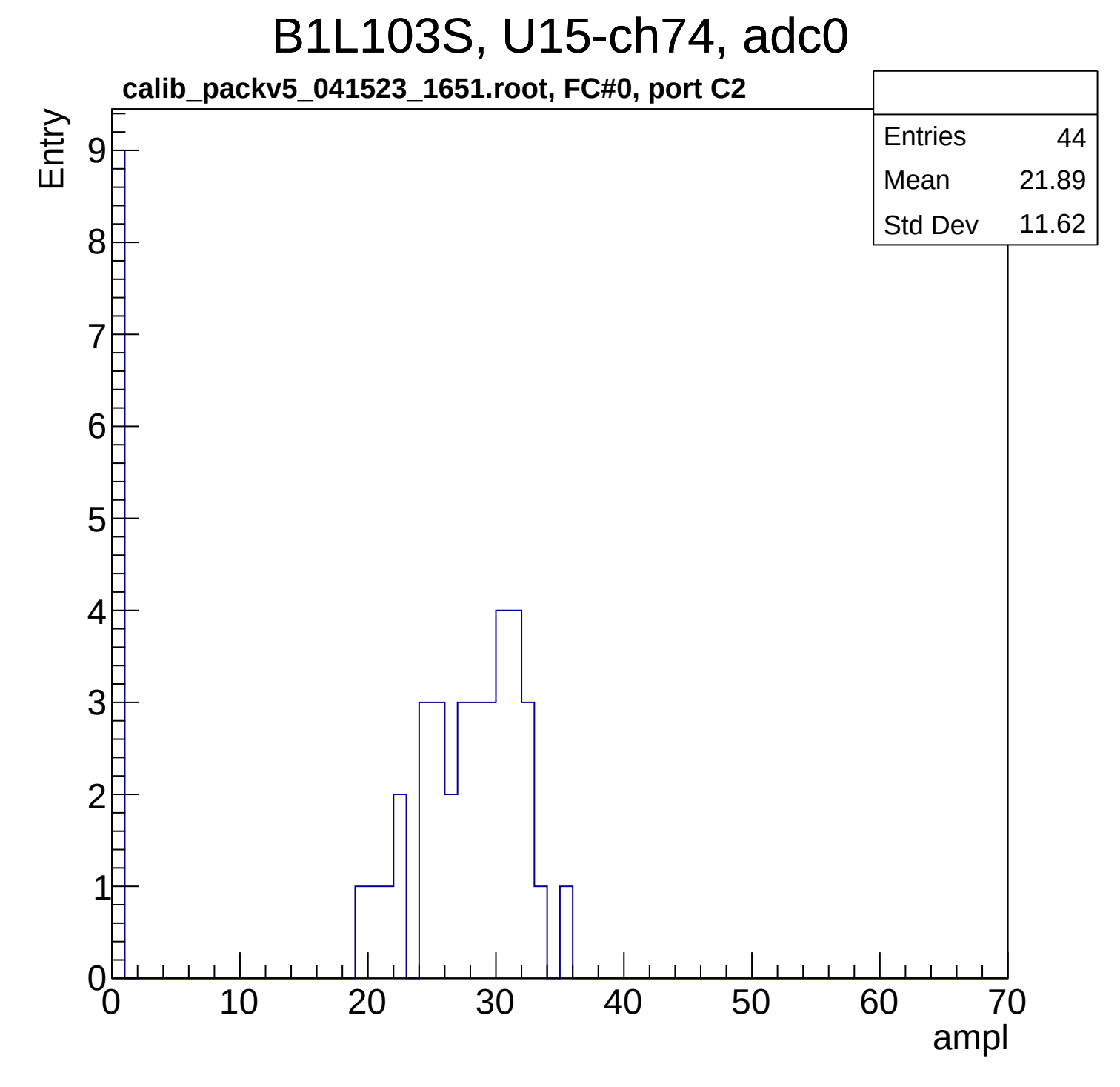

B1L103S, U15-ch73, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 55.55
Std Dev 17.65
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch73, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch74, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 21.89
Std Dev 11.62
Entry
ampl
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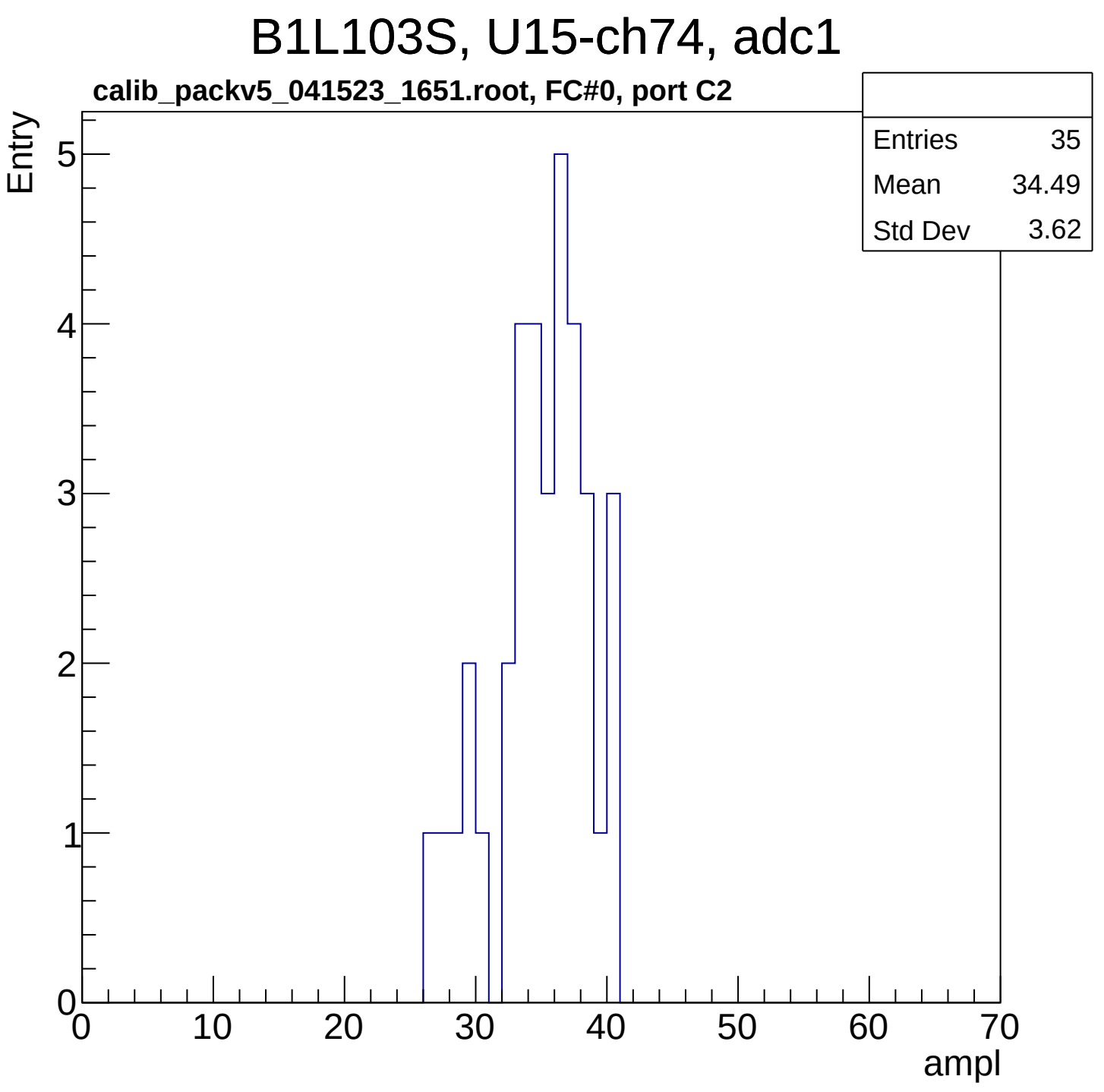
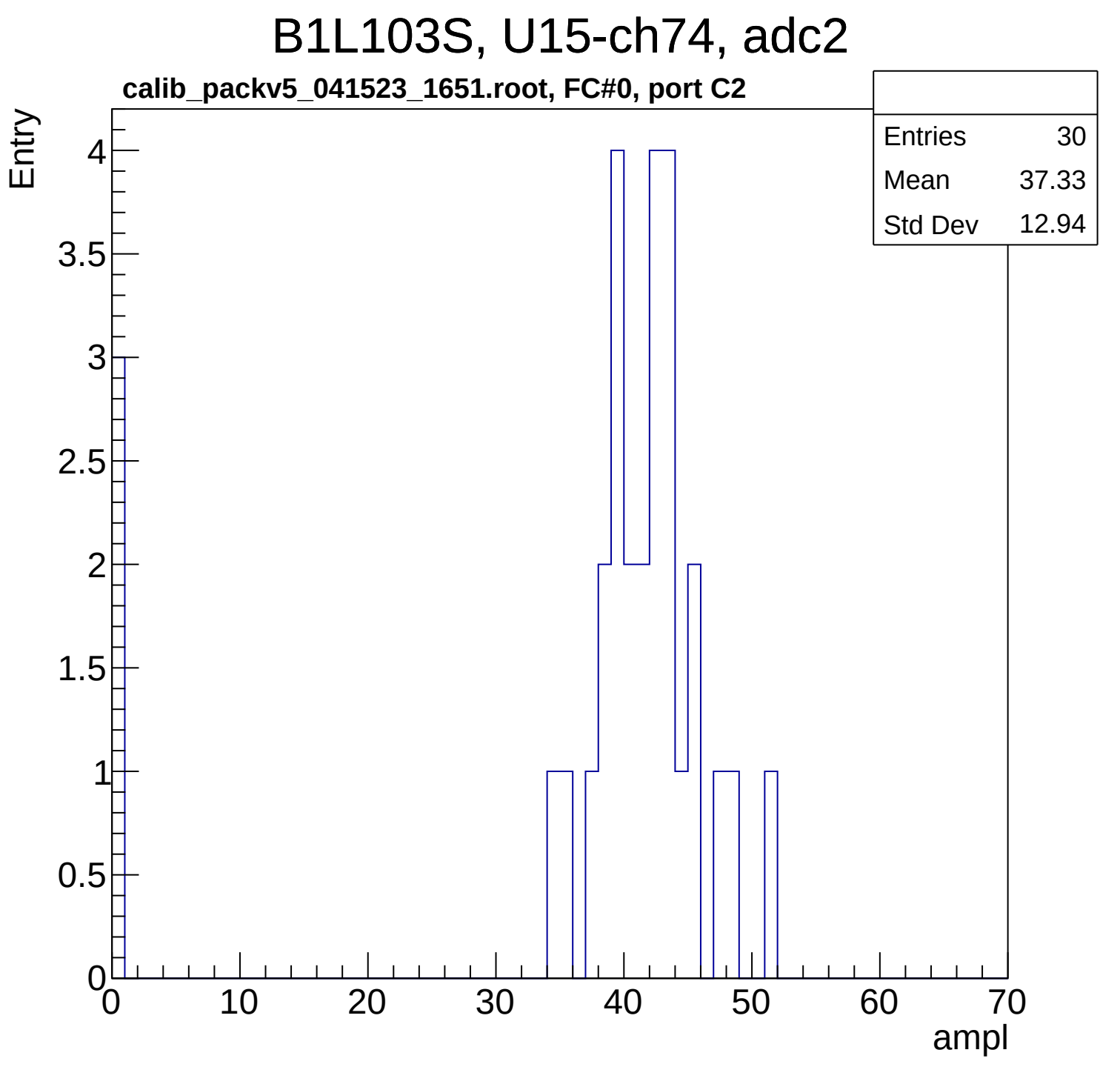
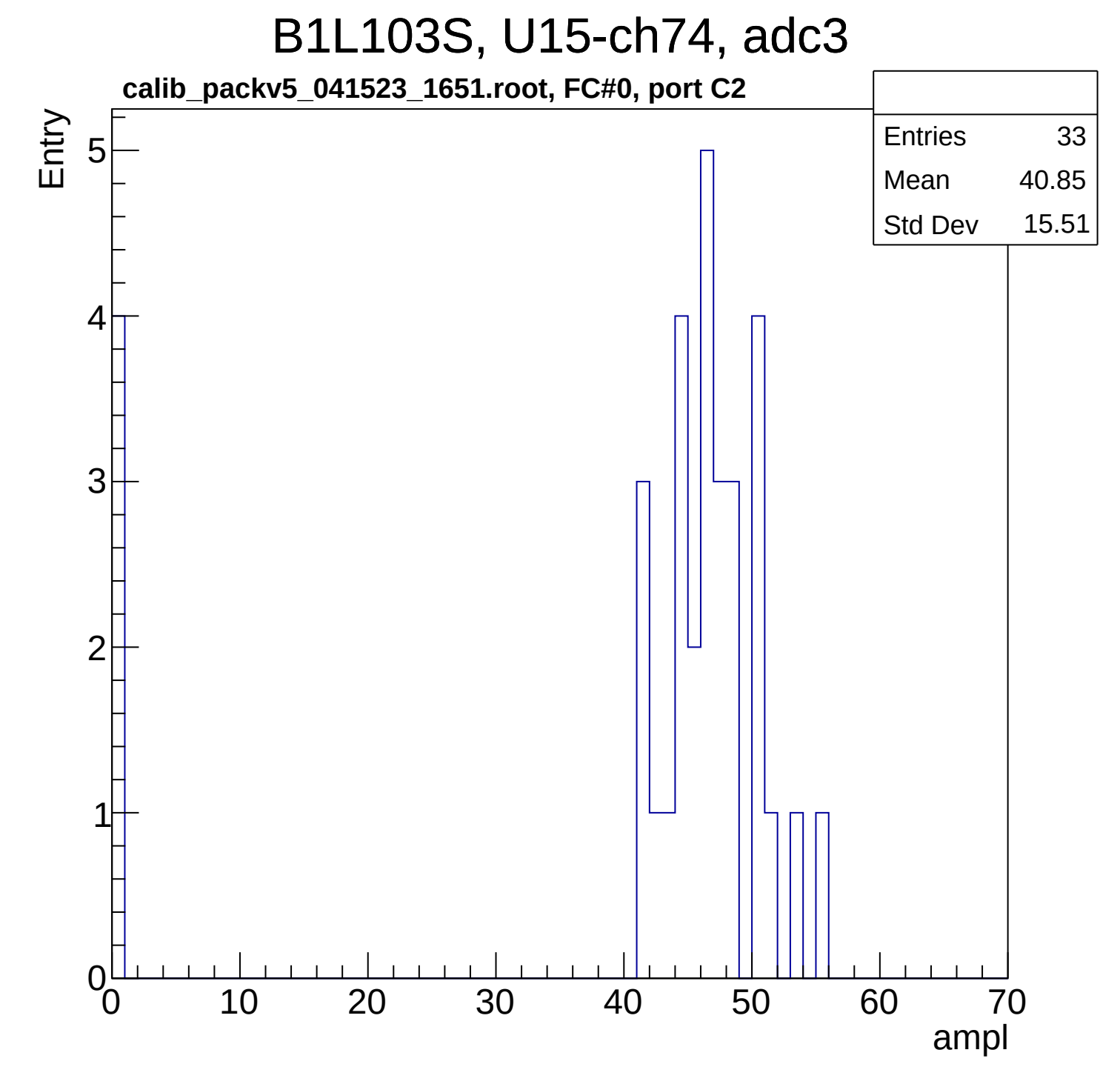
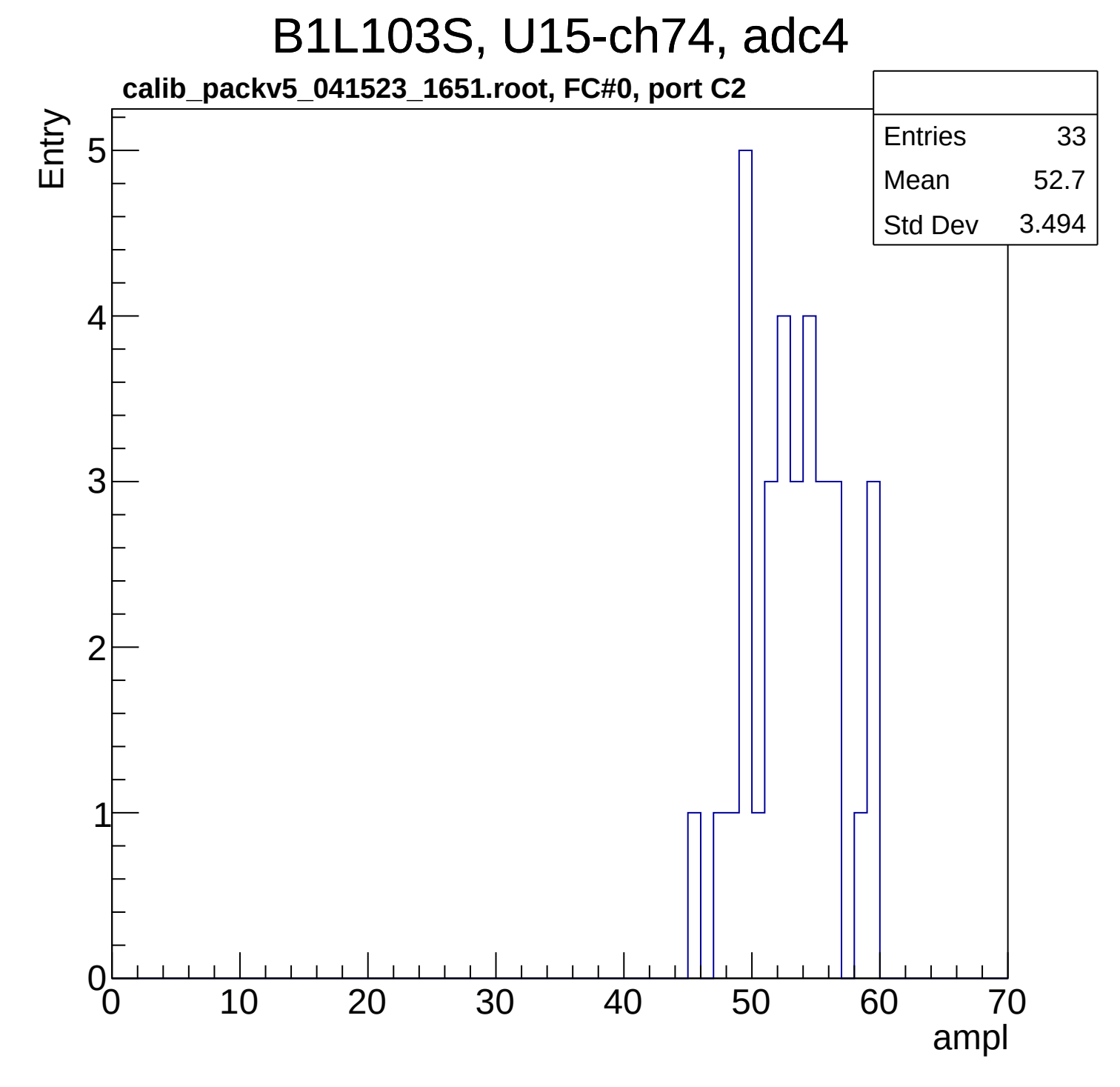
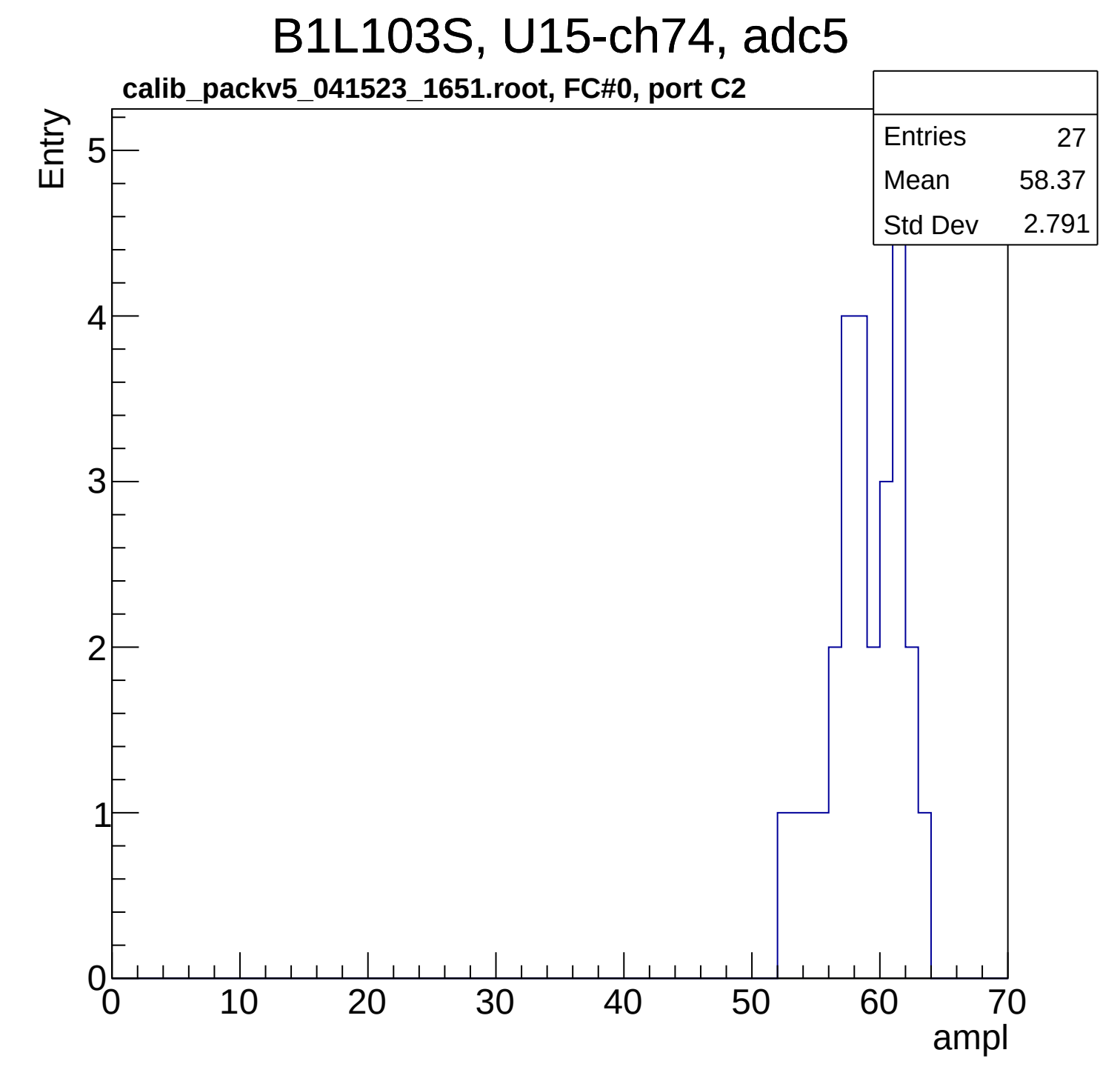
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

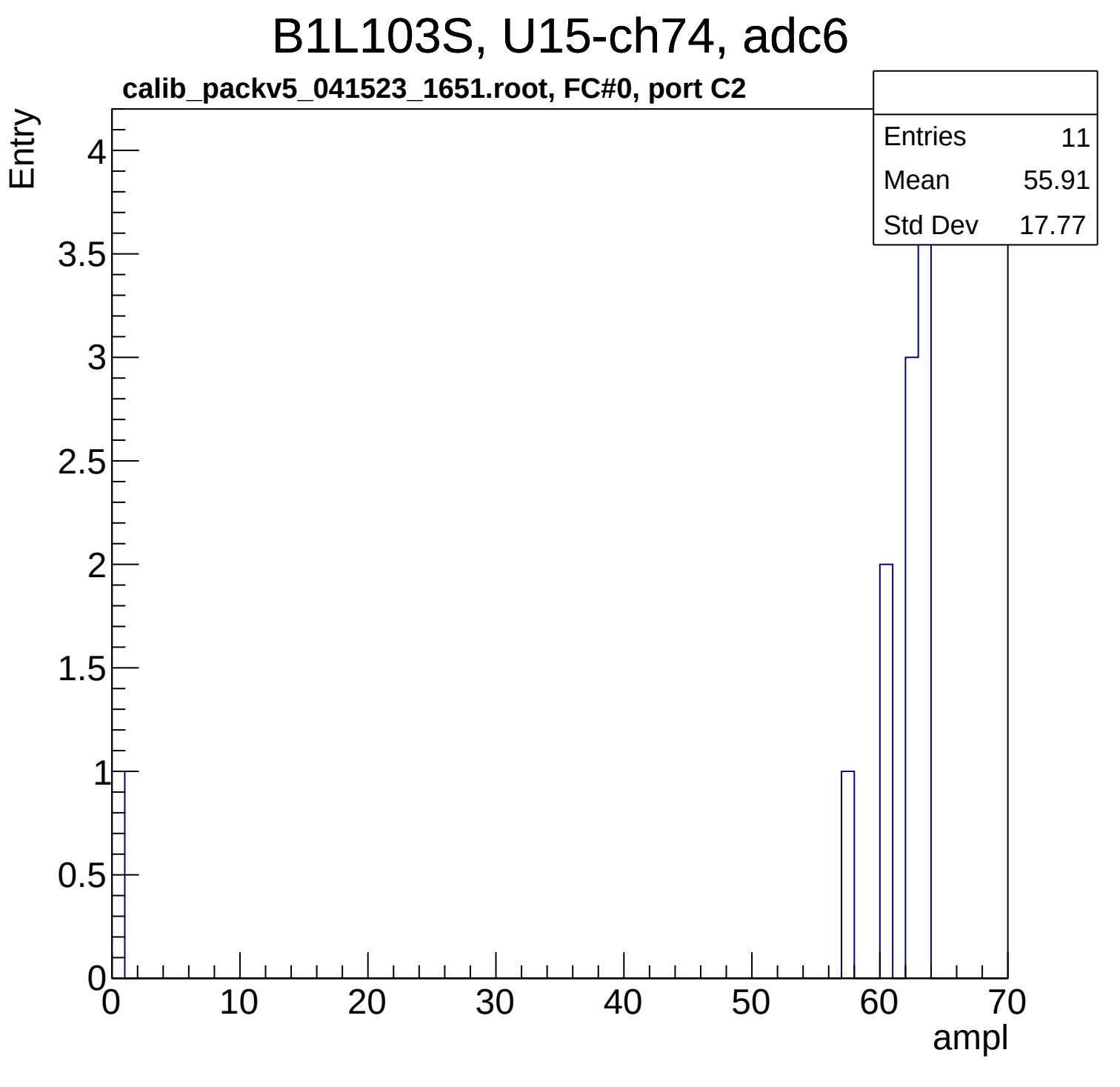

B1L103S, U15-ch74, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 34.49
Std Dev 3.62
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch74, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 37.33
Std Dev 12.94
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch74, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 40.85
Std Dev 15.51
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch74, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 52.7
Std Dev 3.494
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch74, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 58.37
Std Dev 2.791
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch74, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 55.91
Std Dev 17.77
Entry
ampl
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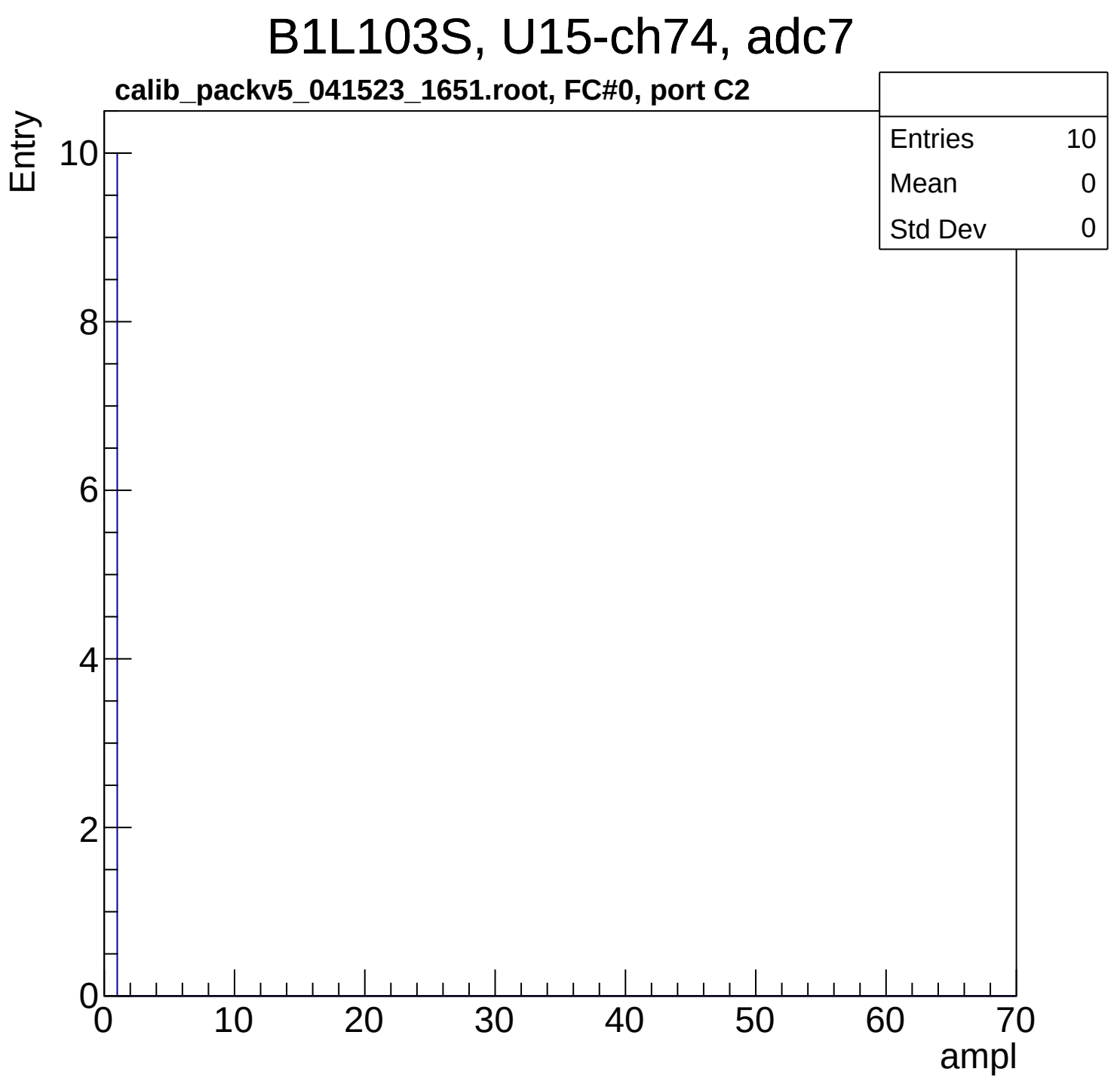
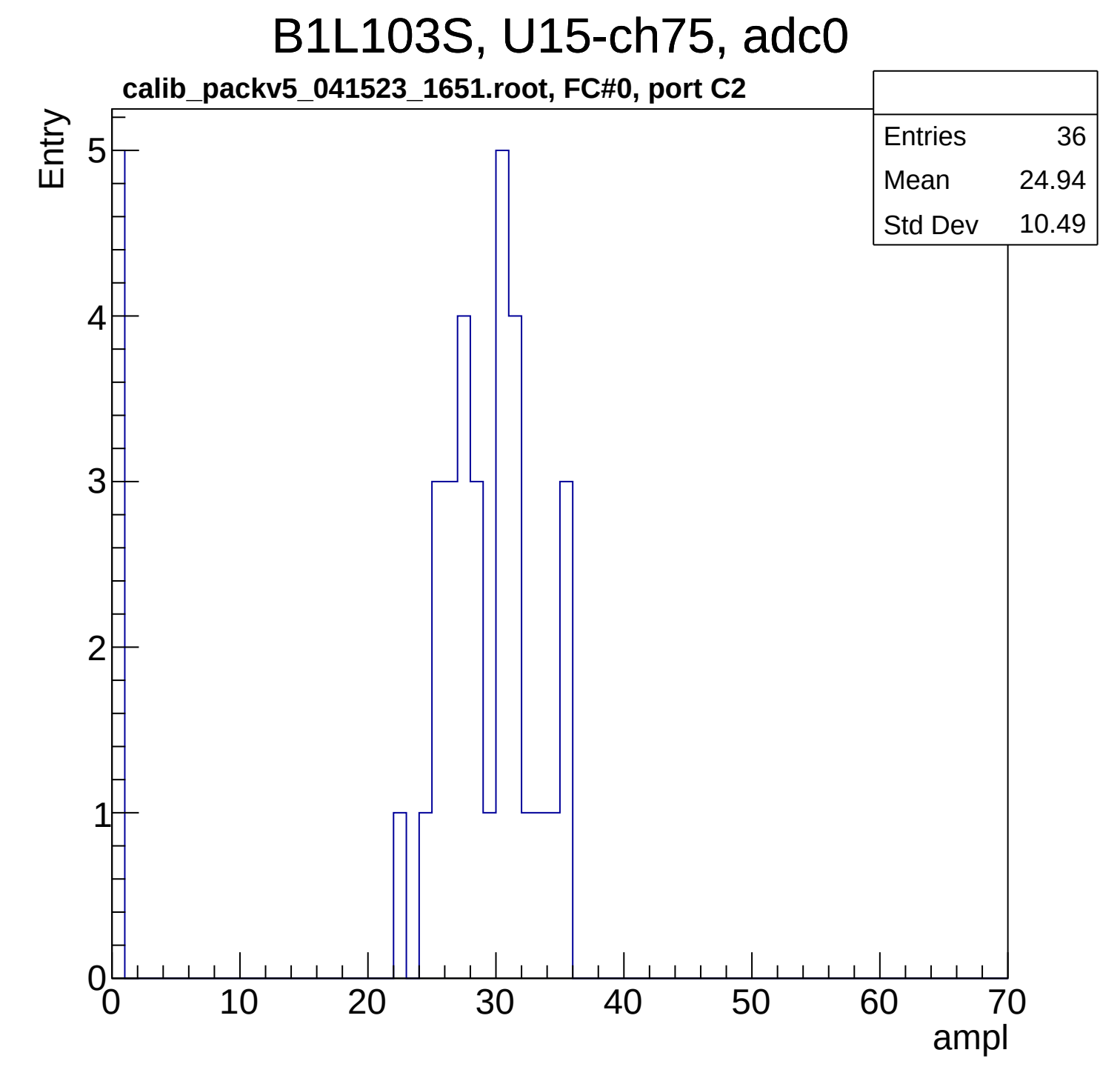
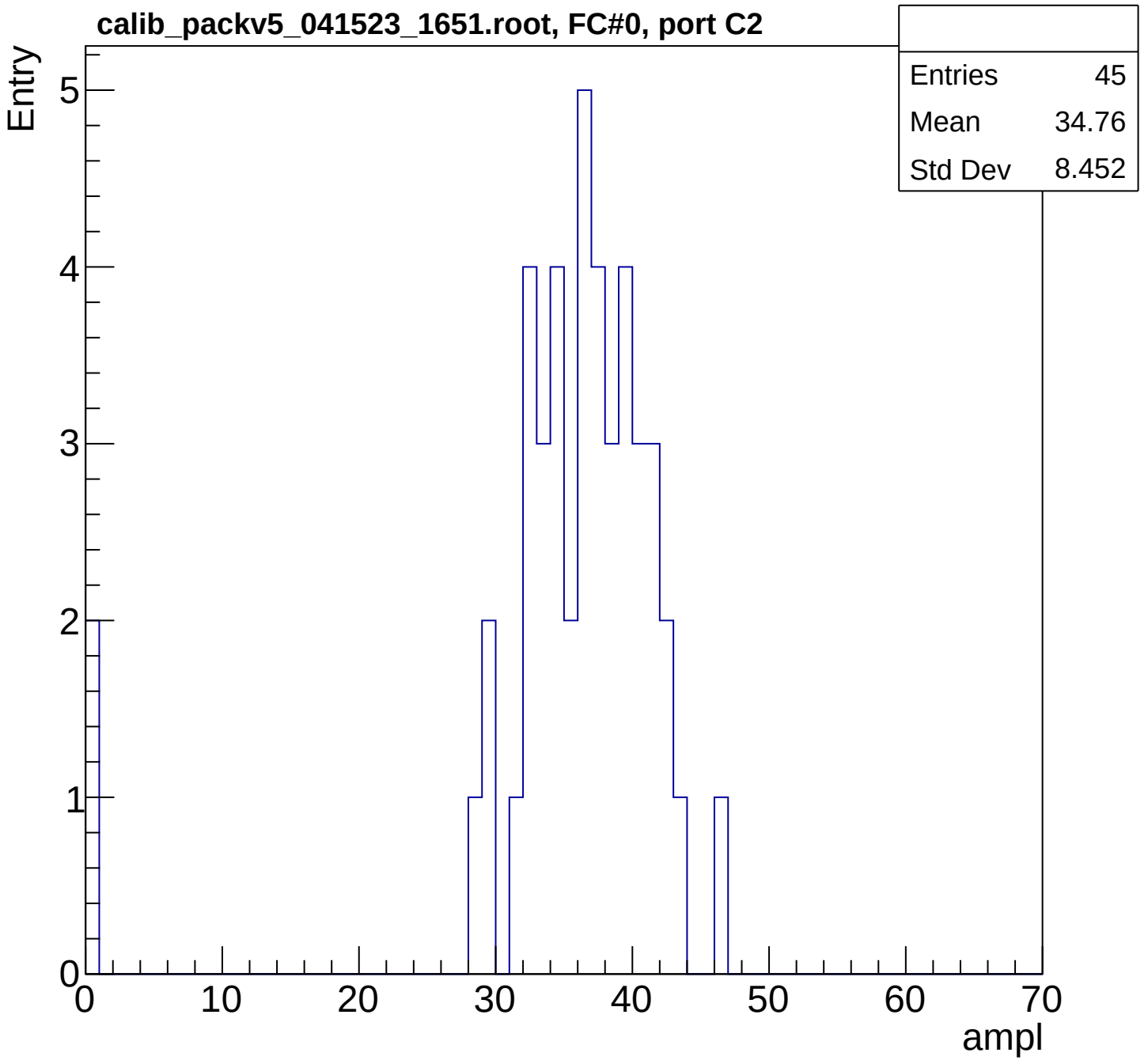
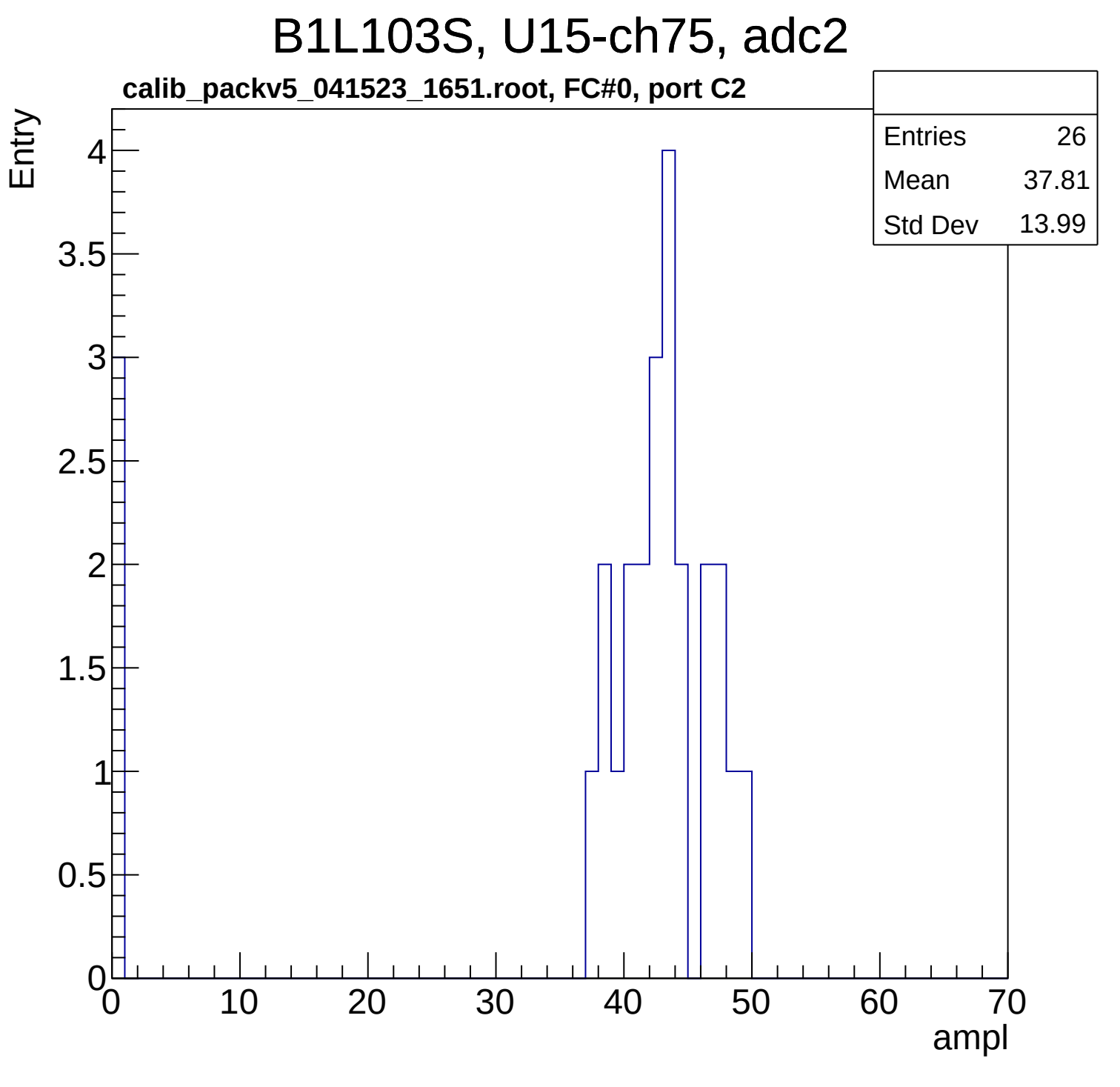
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch74, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch75, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 24.94
Std Dev 10.49
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch75, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 34.76
Std Dev 8.452
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch75, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 37.81
Std Dev 13.99
Entry
ampl
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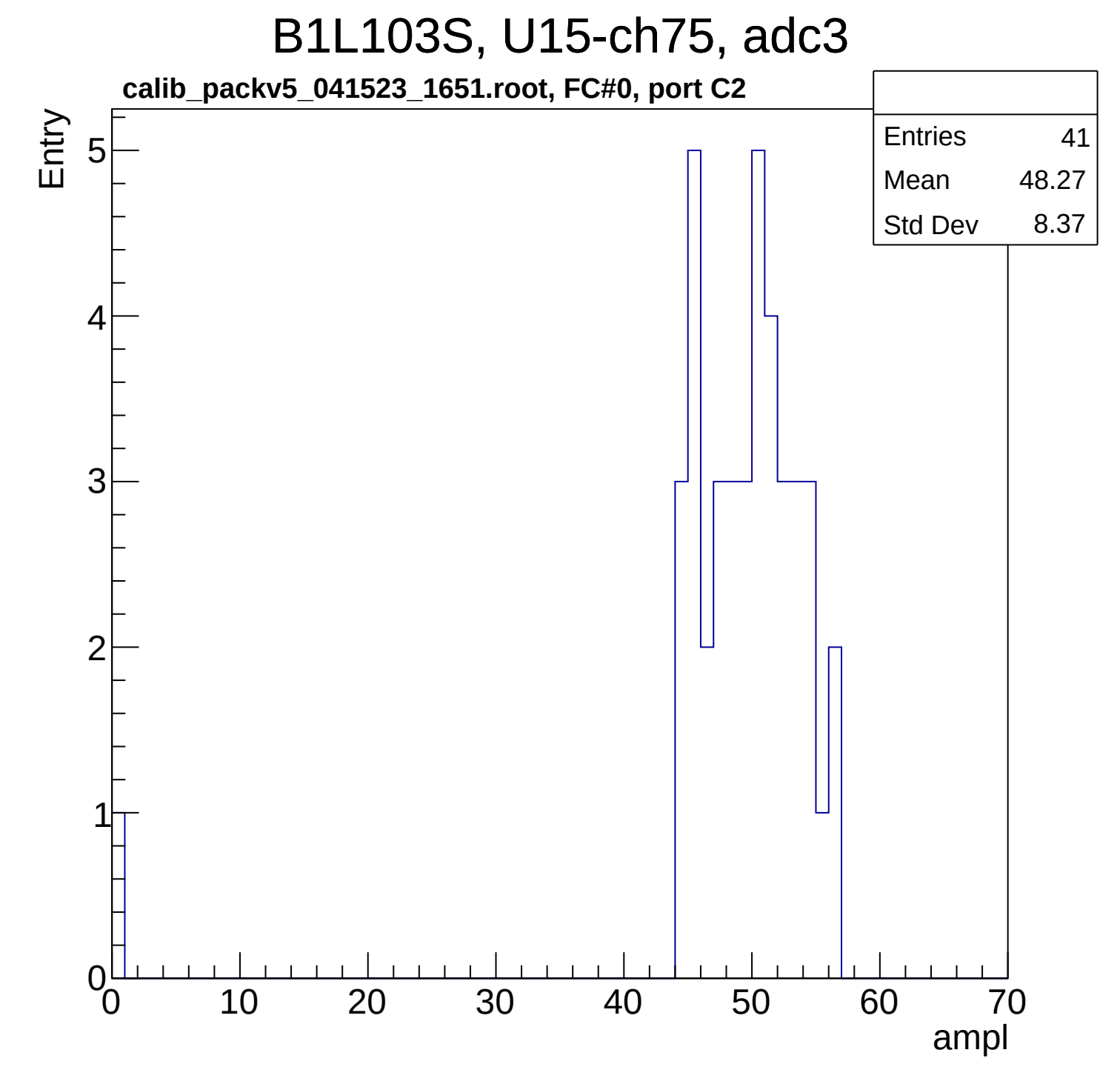
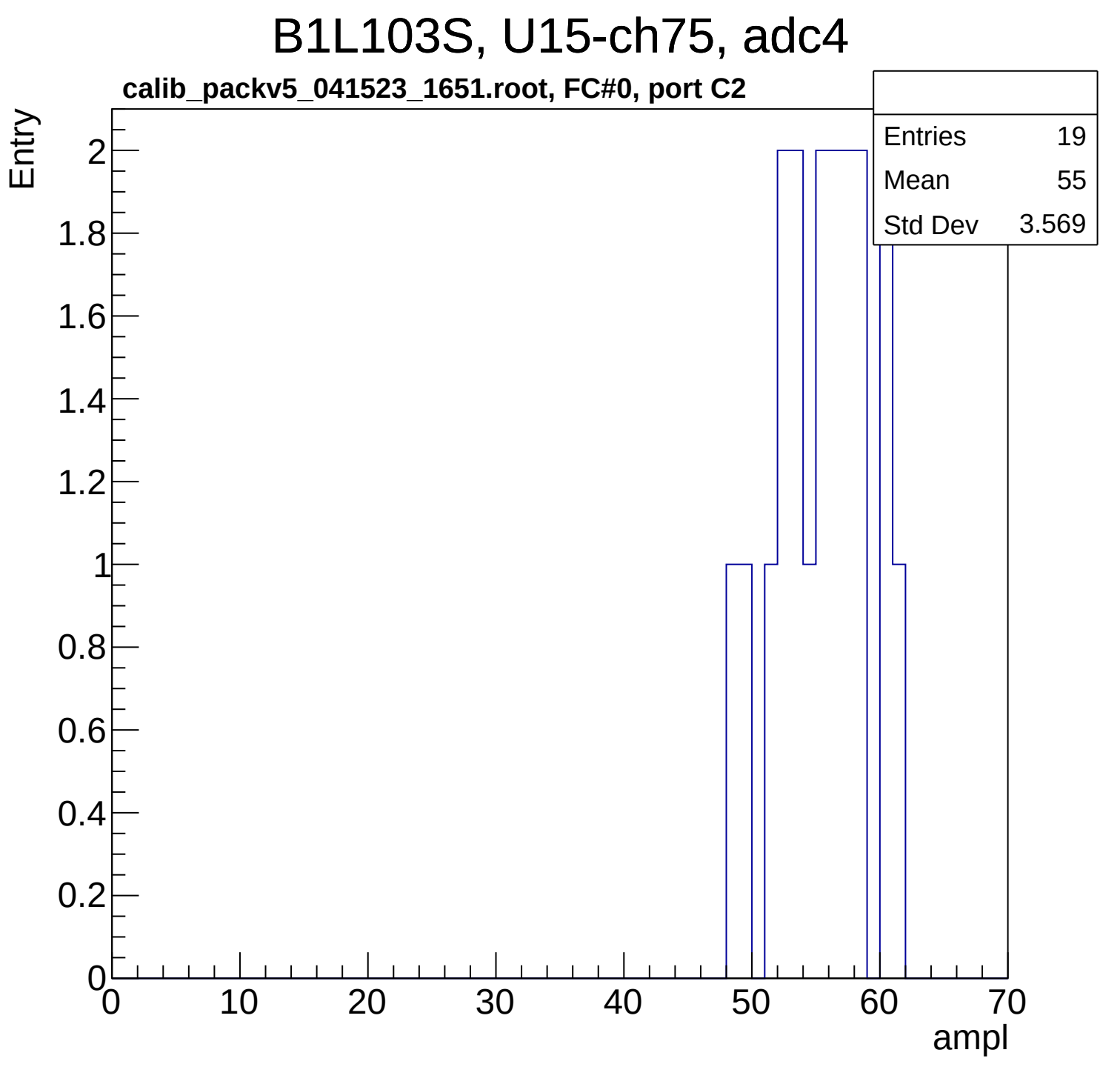
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch75, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 48.27
Std Dev 8.37
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch75, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 55
Std Dev 3.569
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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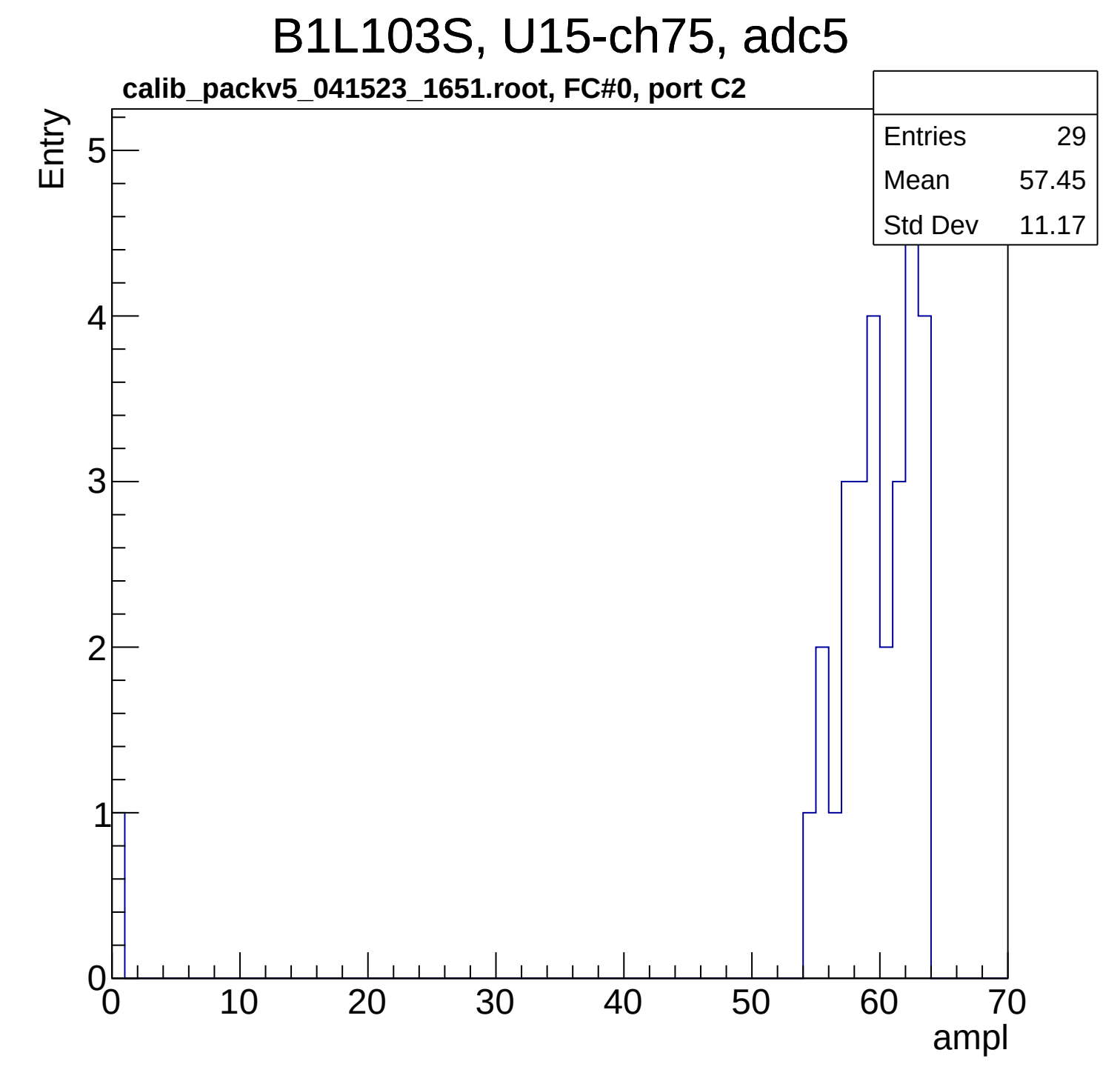
40
50
60
70


B1L103S, U15-ch75, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 57.45
Std Dev 11.17
Entry
ampl
0
1
2
3
4
5
0
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20
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40
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60
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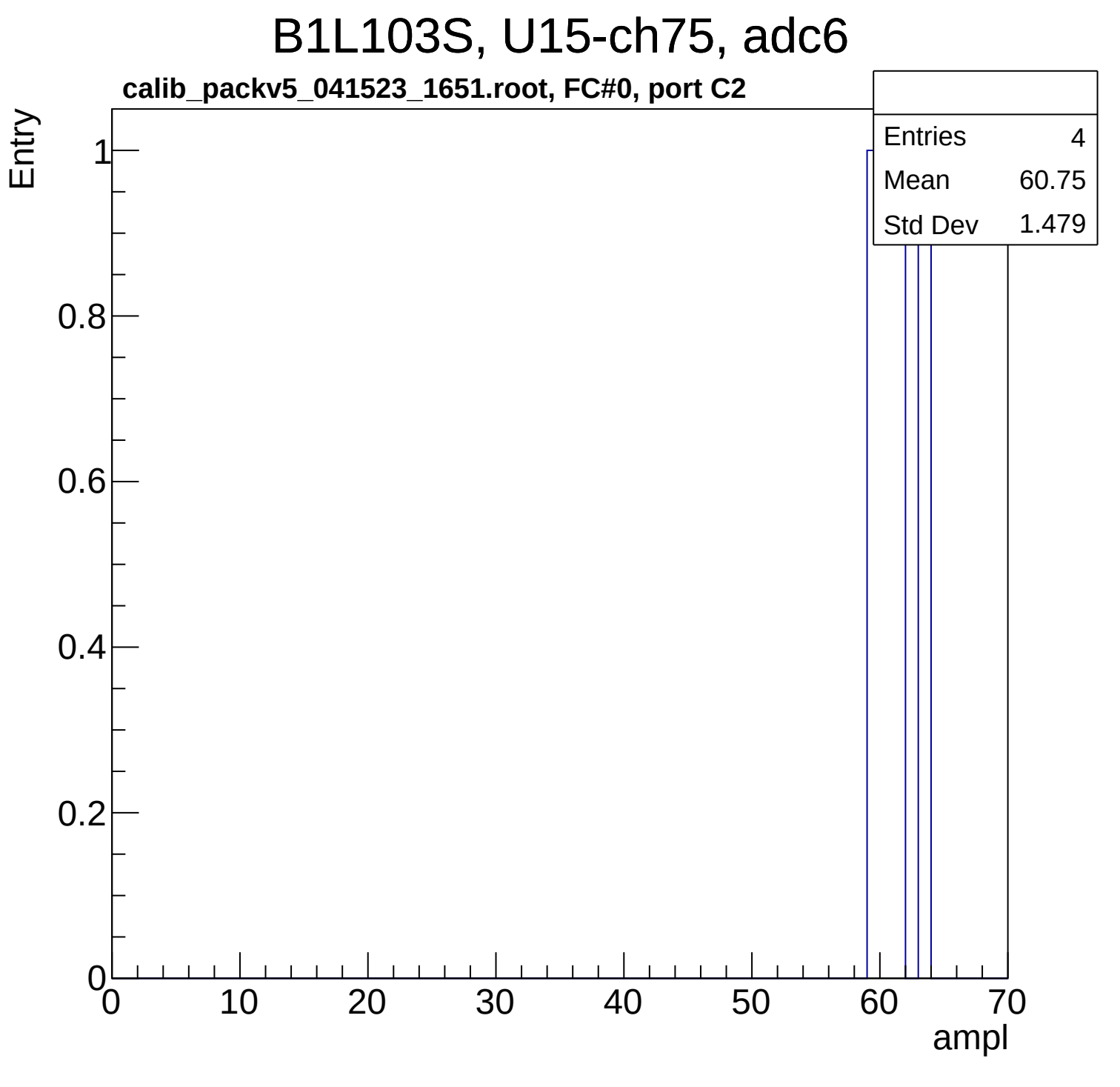
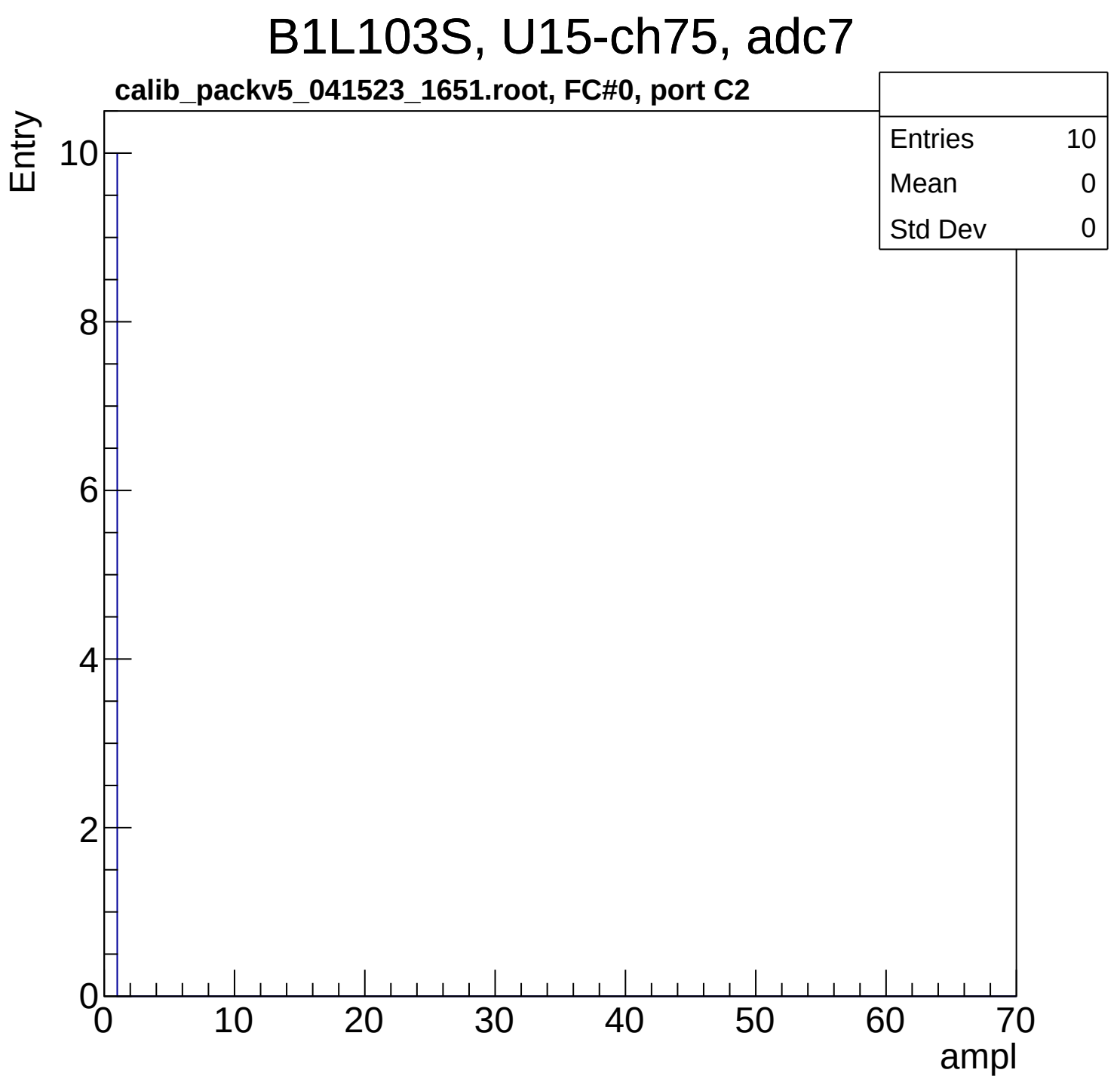
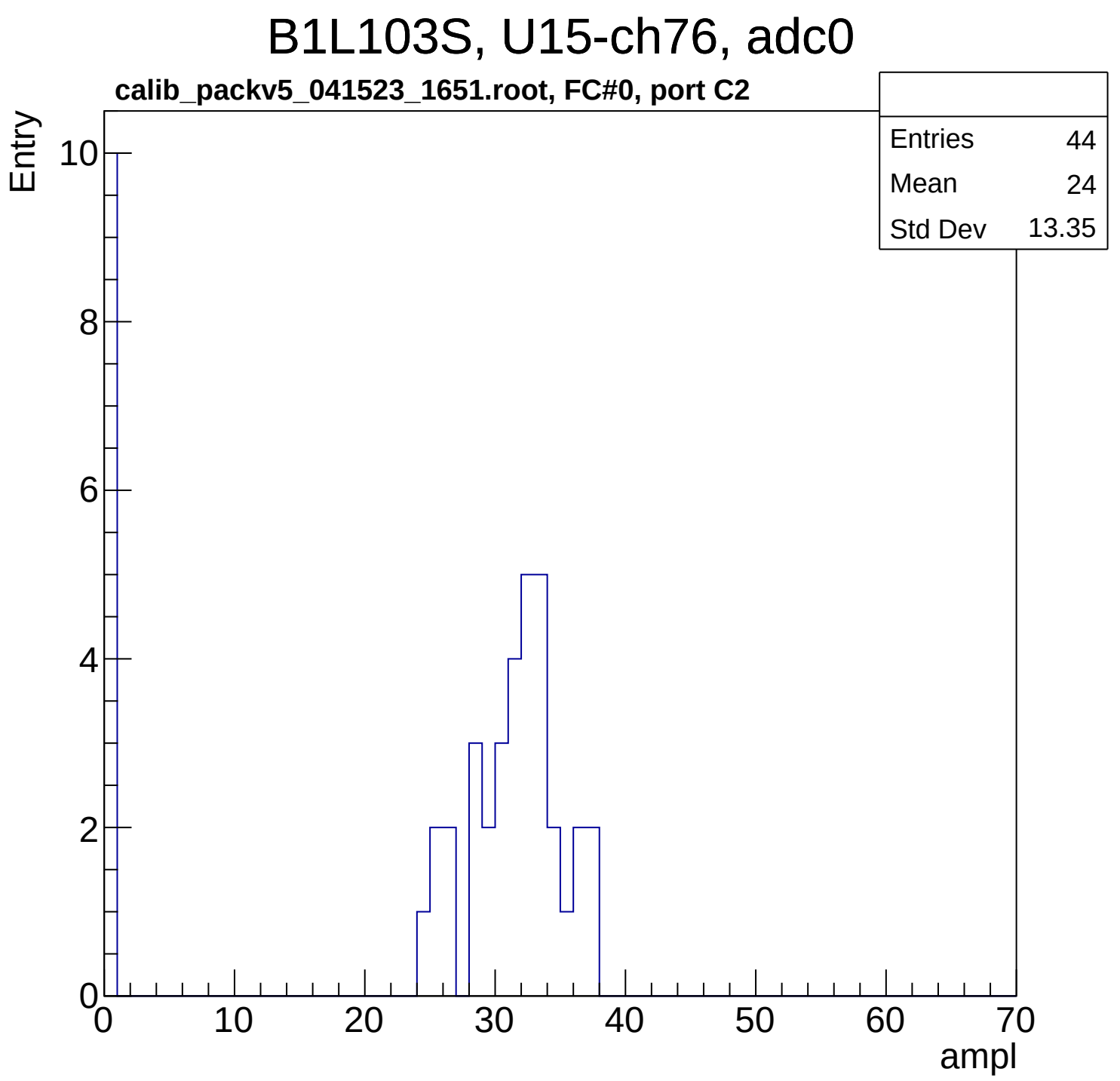
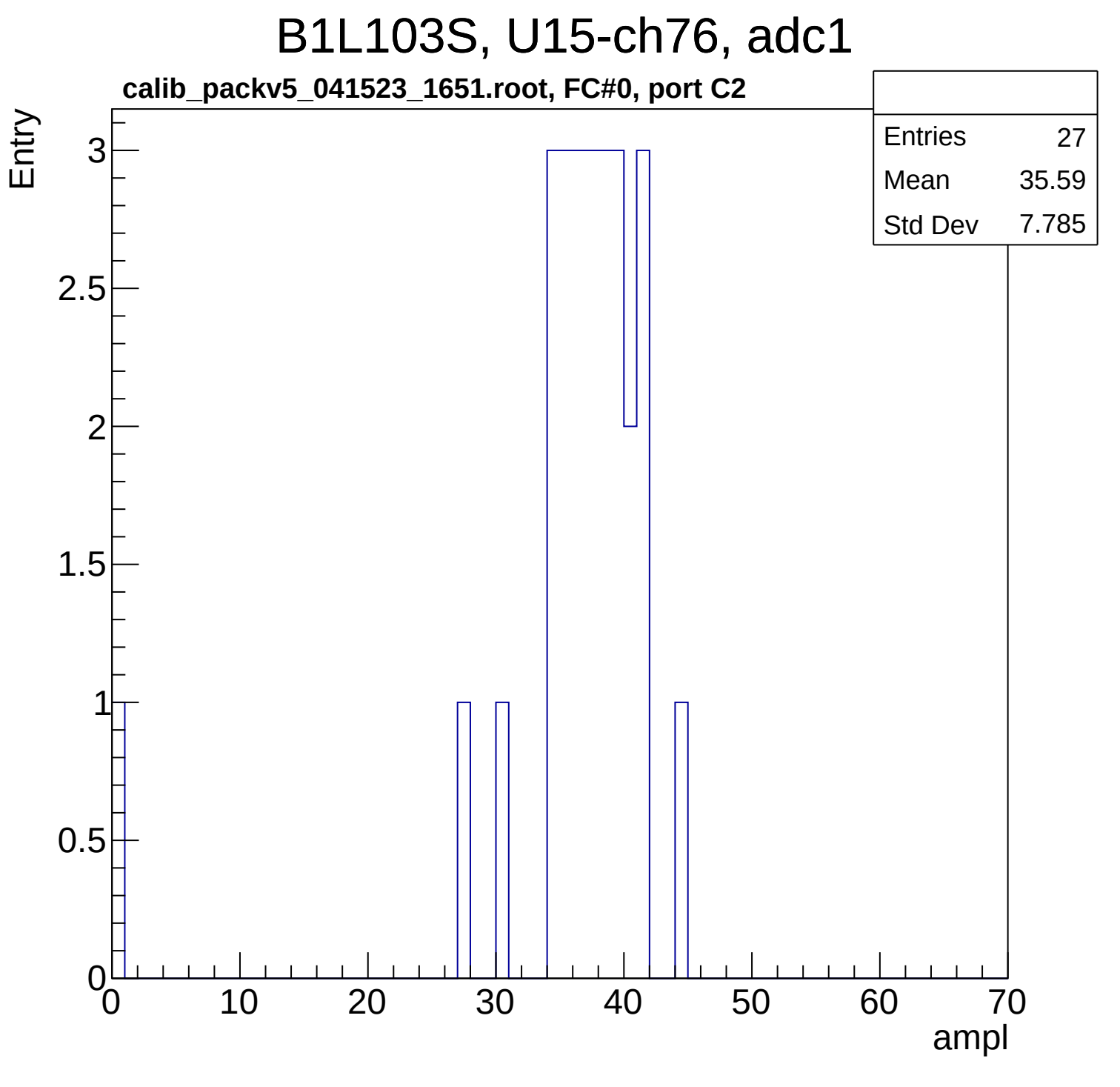

B1L103S, U15-ch75, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 60.75
Std Dev 1.479
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L103S, U15-ch75, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch76, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 24
Std Dev 13.35
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U15-ch76, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 35.59
Std Dev 7.785
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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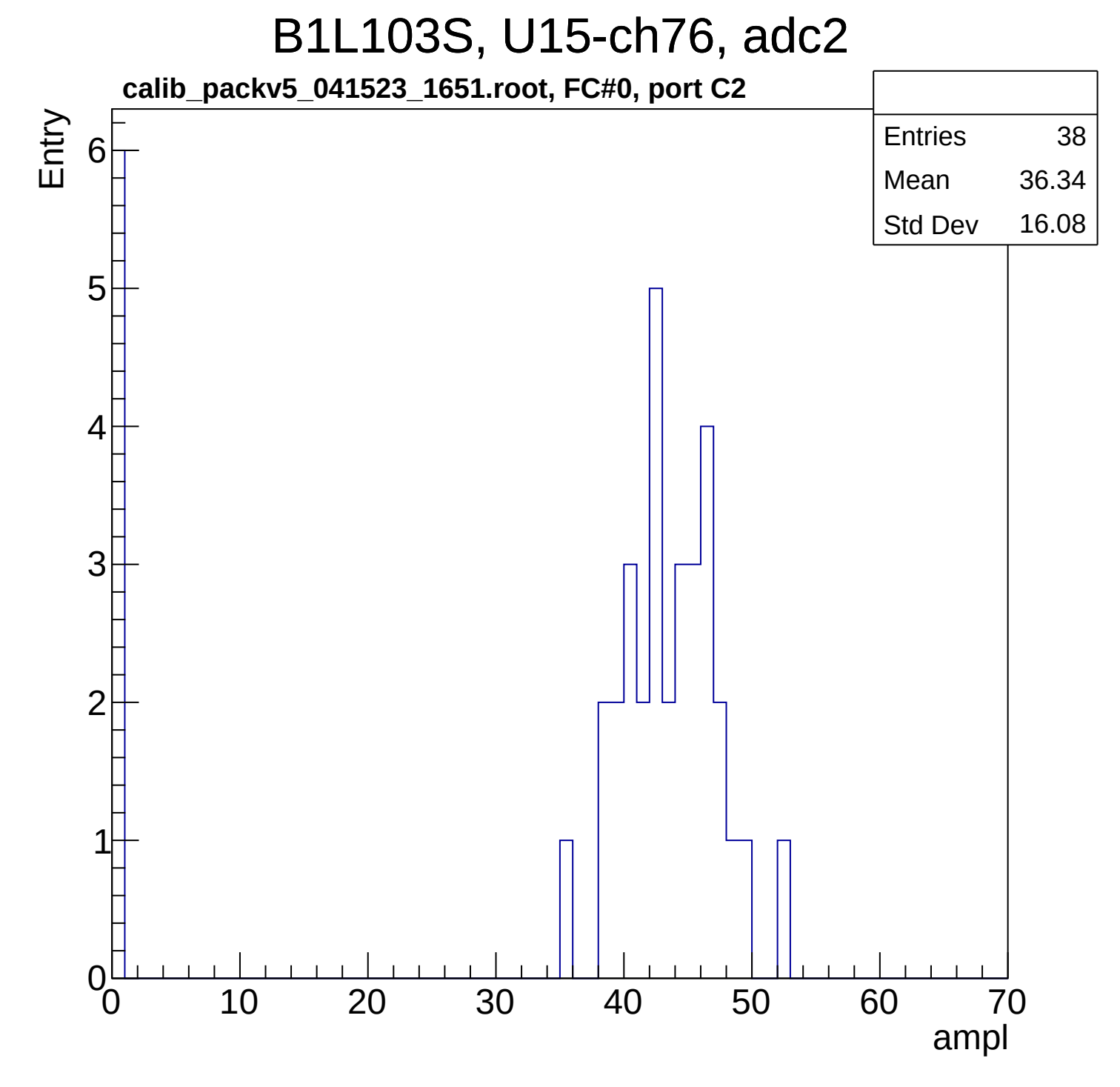
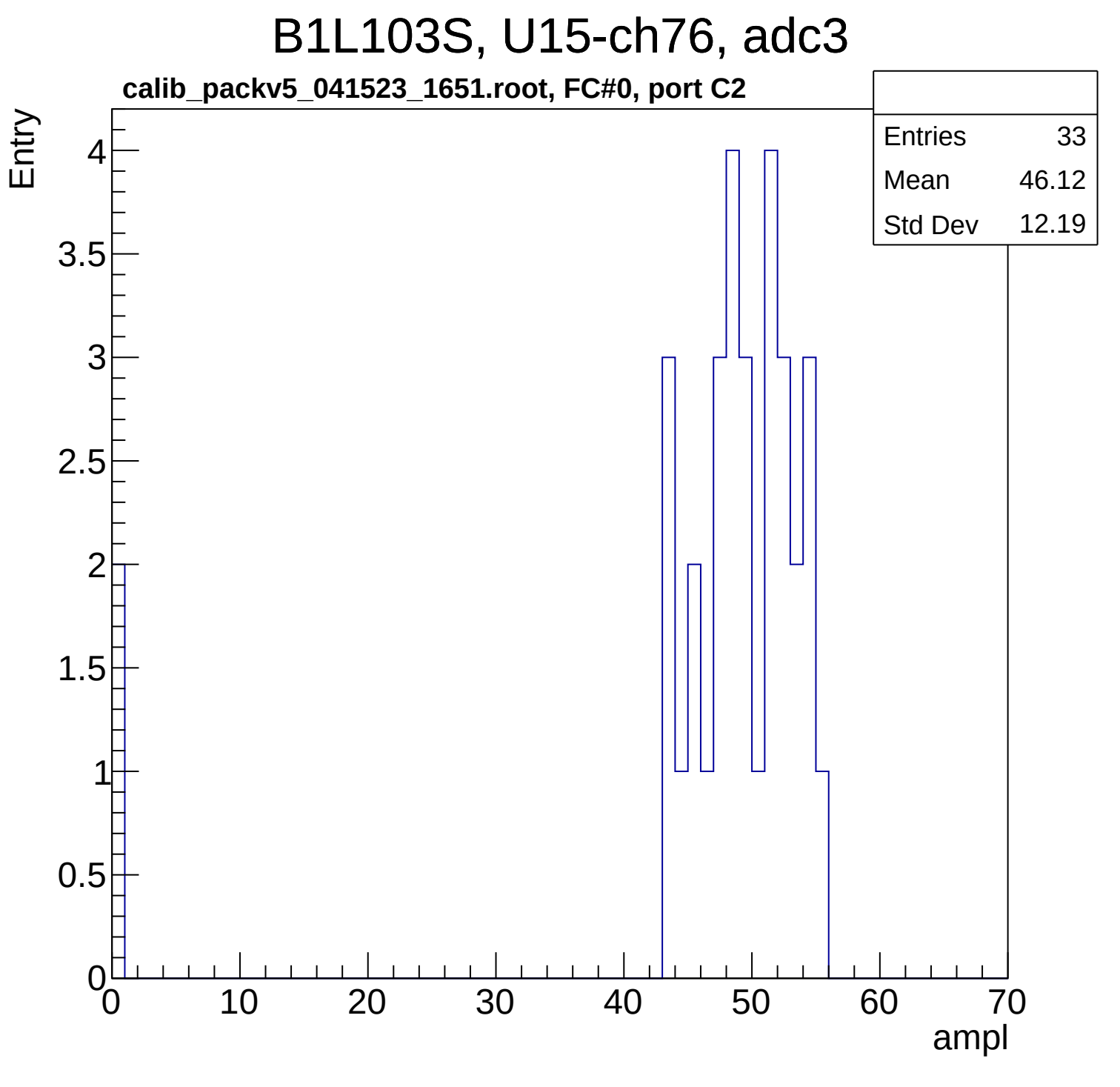

B1L103S, U15-ch76, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 36.34
Std Dev 16.08
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U15-ch76, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 46.12
Std Dev 12.19
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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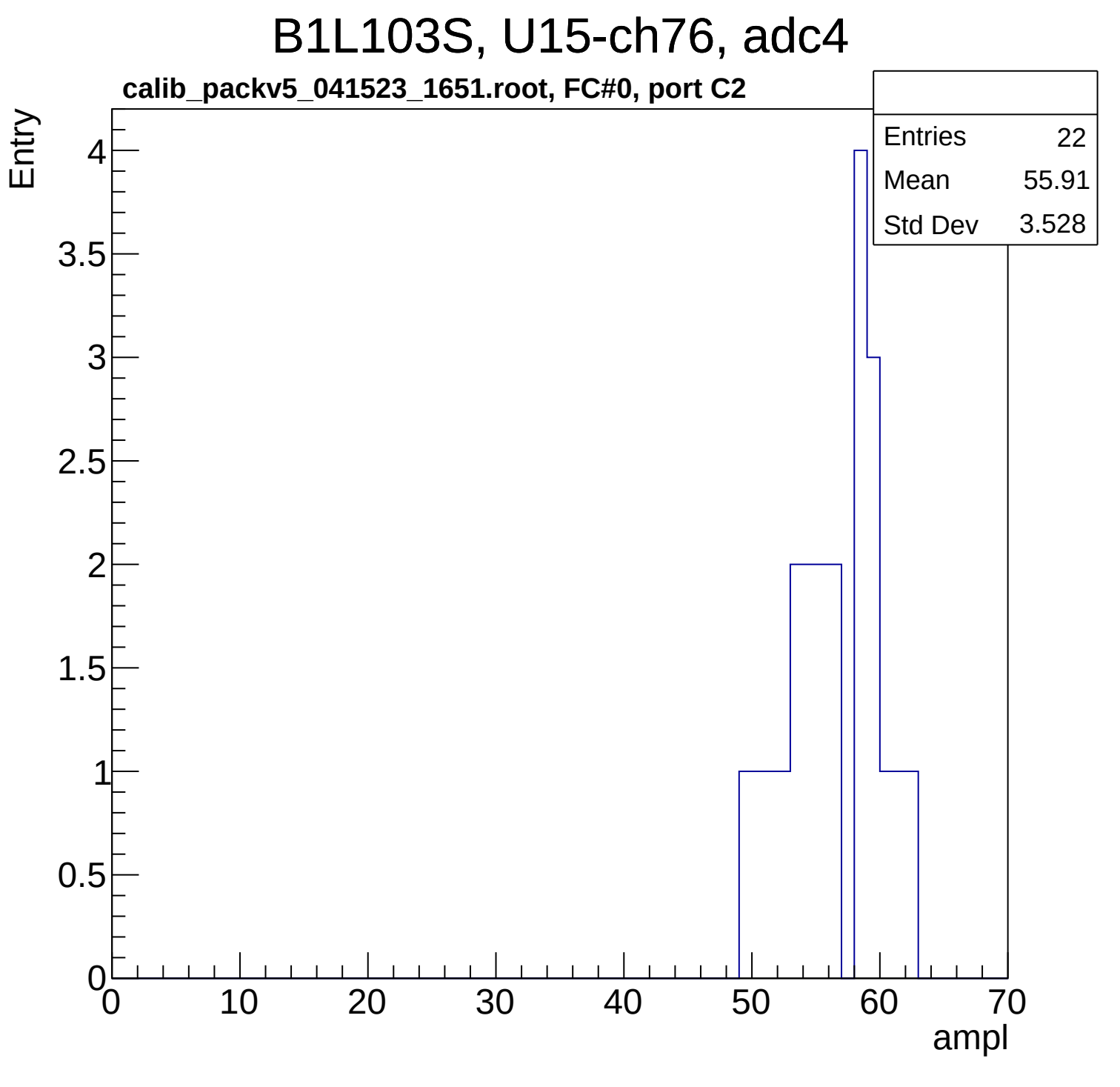
B1L103S, U15-ch76, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 55.91
Std Dev 3.528
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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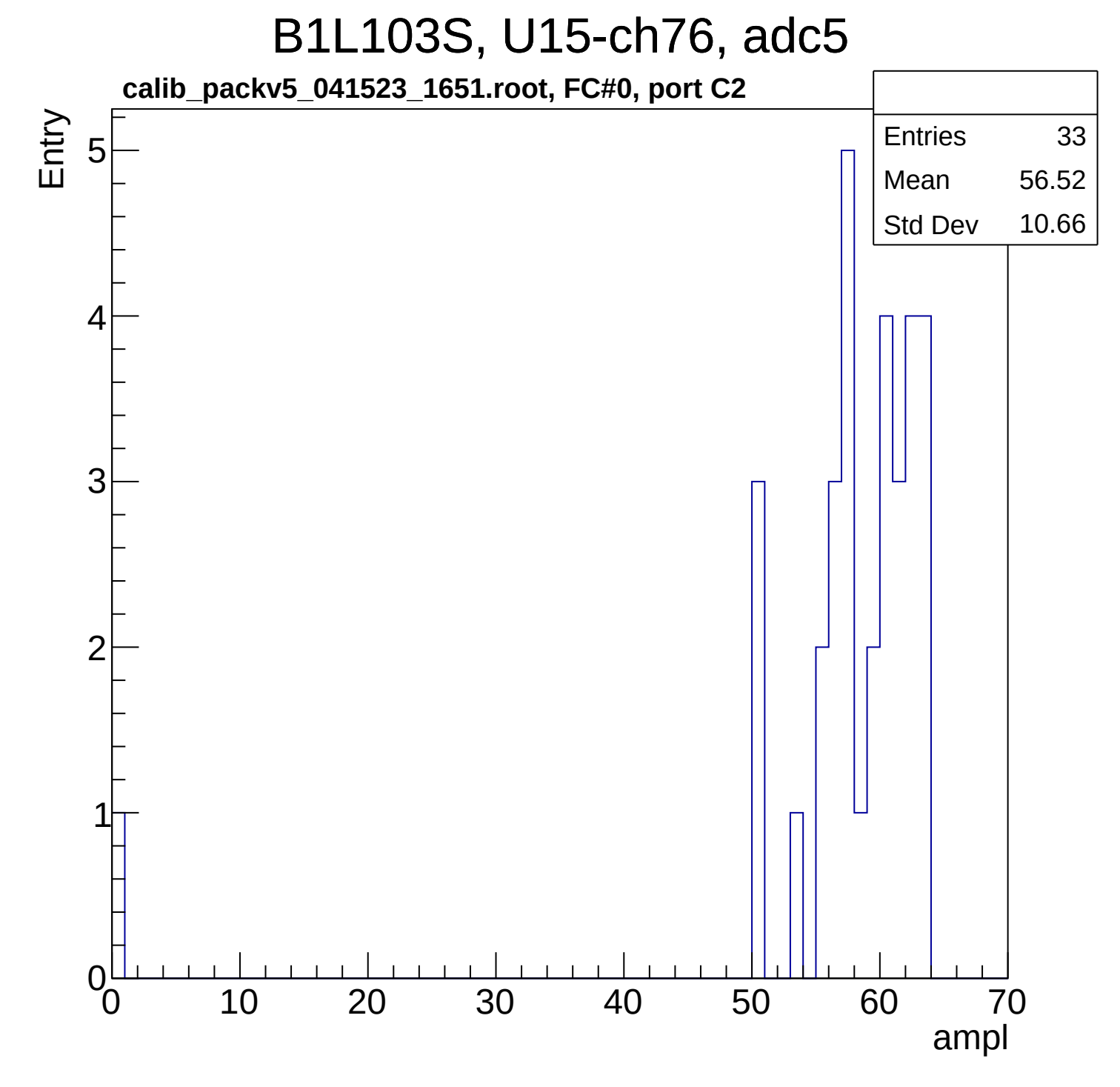
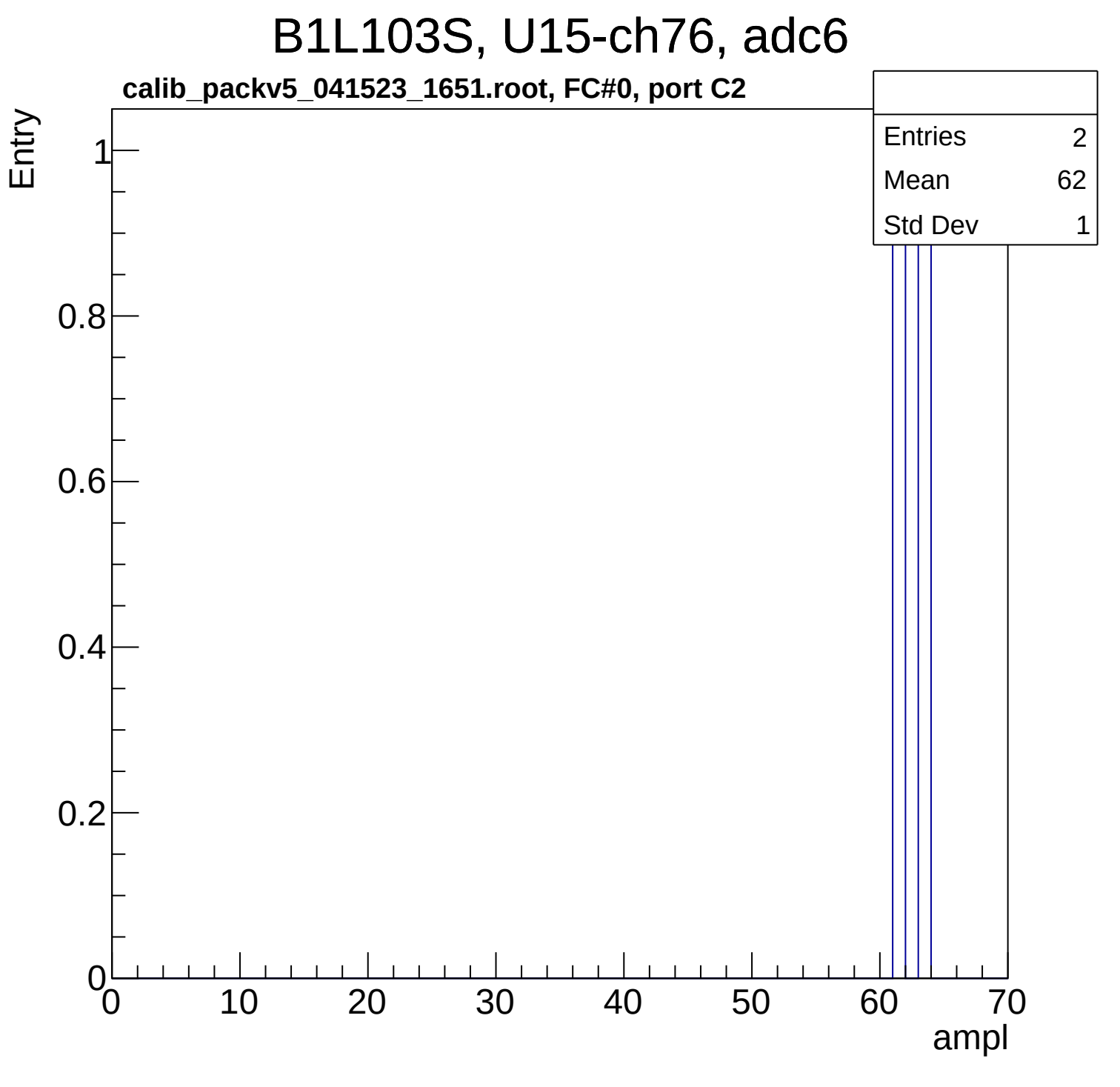

B1L103S, U15-ch76, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 56.52
Std Dev 10.66
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch76, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62
Std Dev 1
Entry
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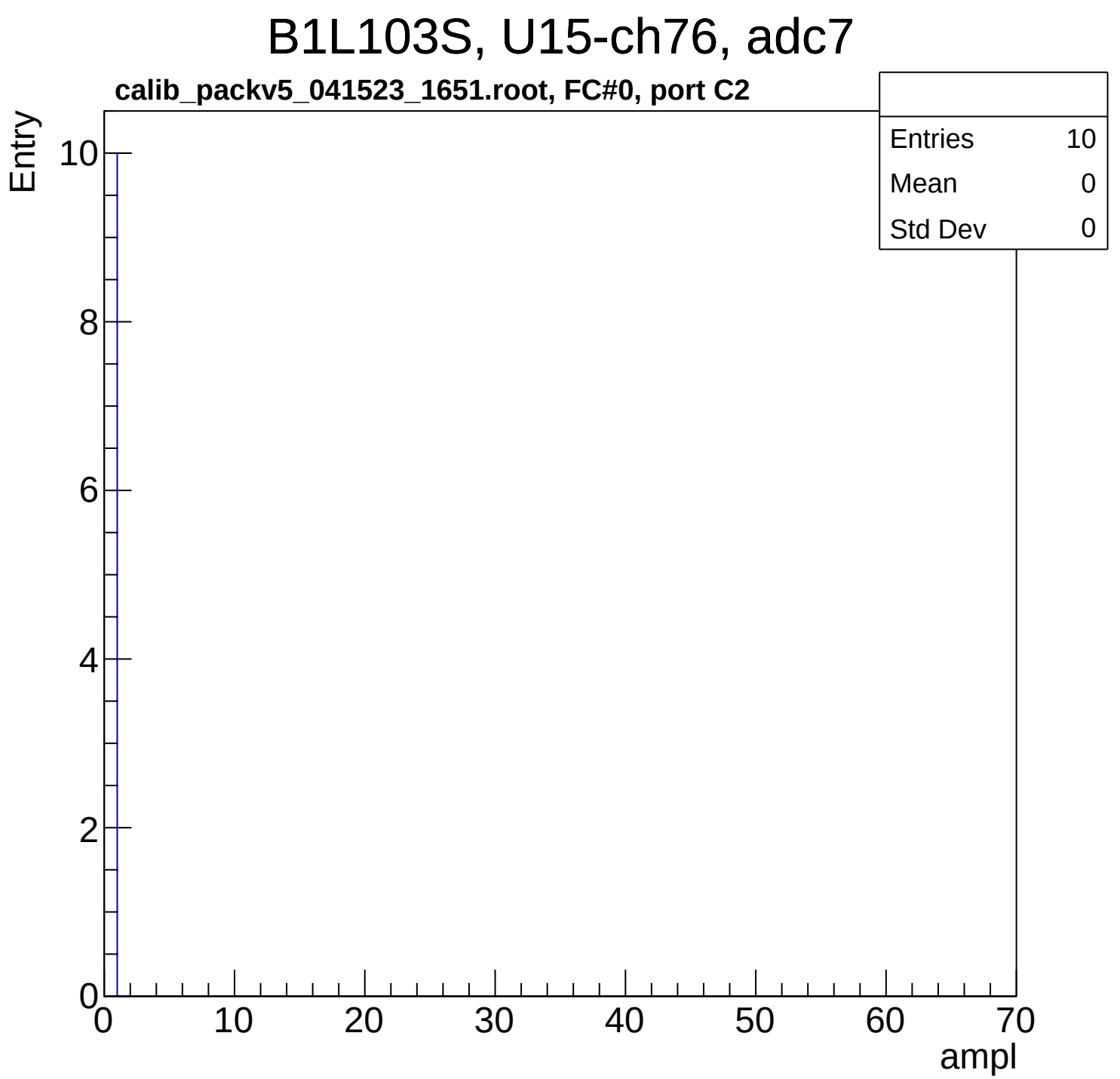
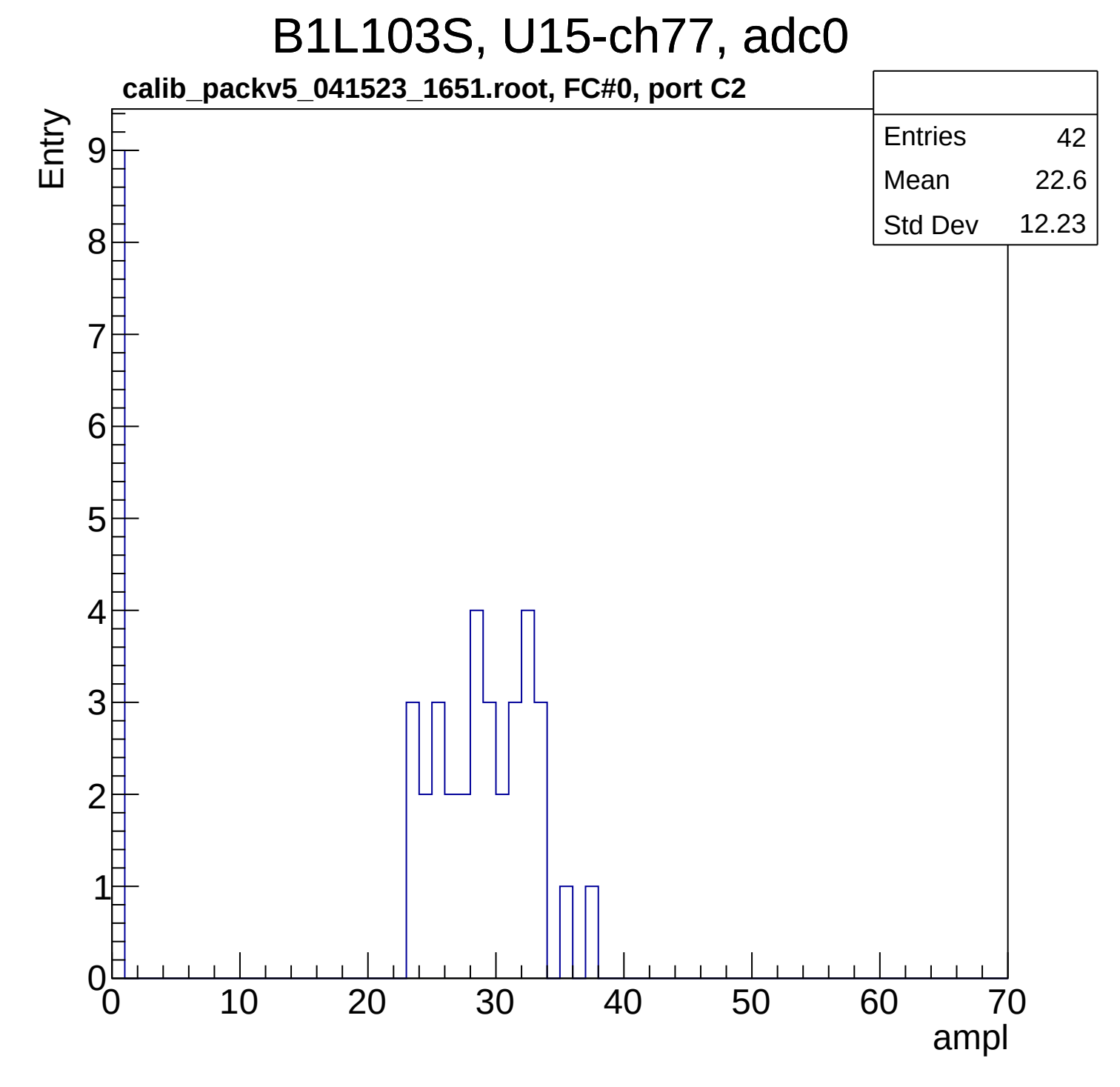
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch76, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch77, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 22.6
Std Dev 12.23
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
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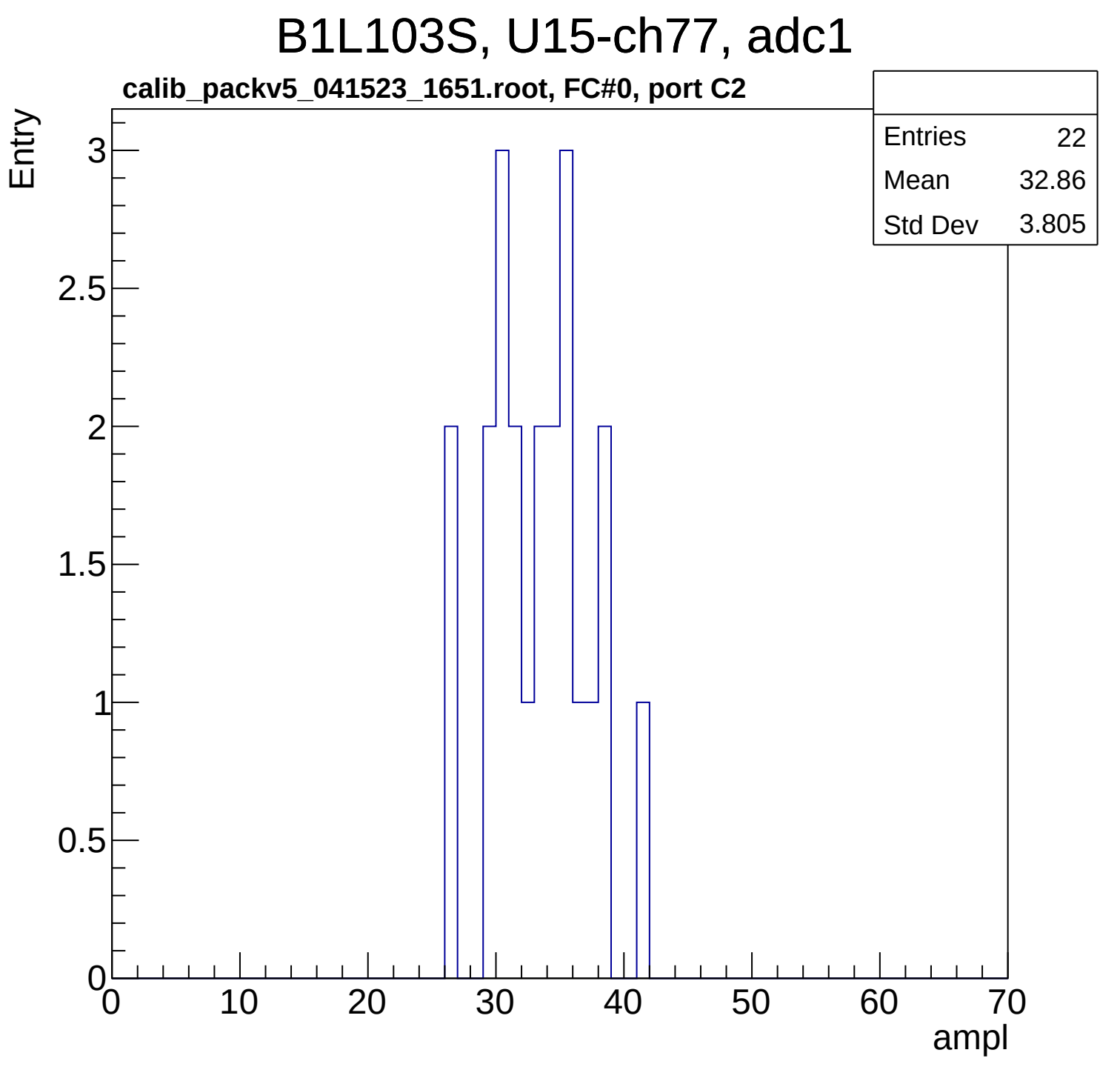
40
50
60
70


B1L103S, U15-ch77, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 32.86
Std Dev 3.805
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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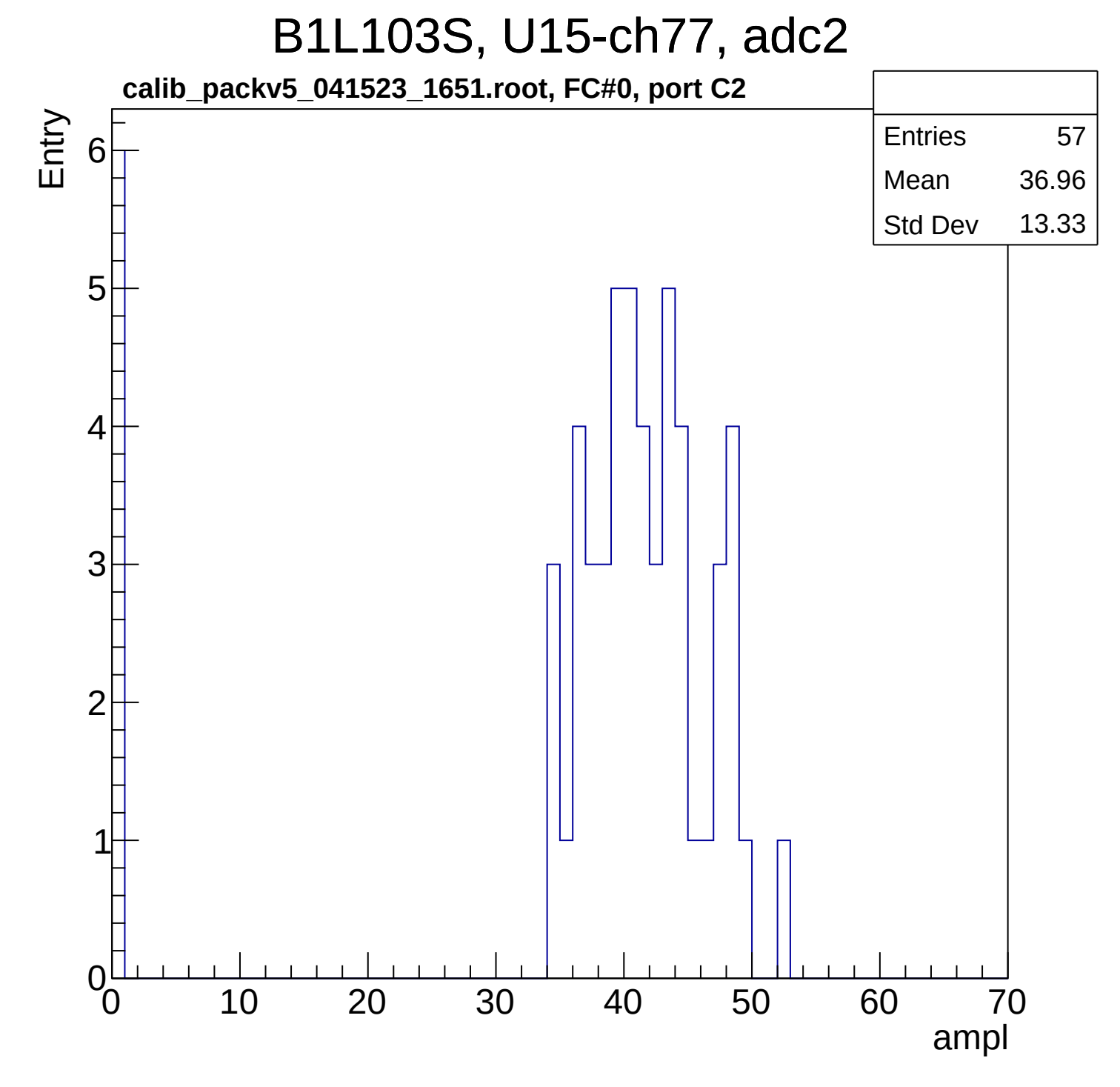
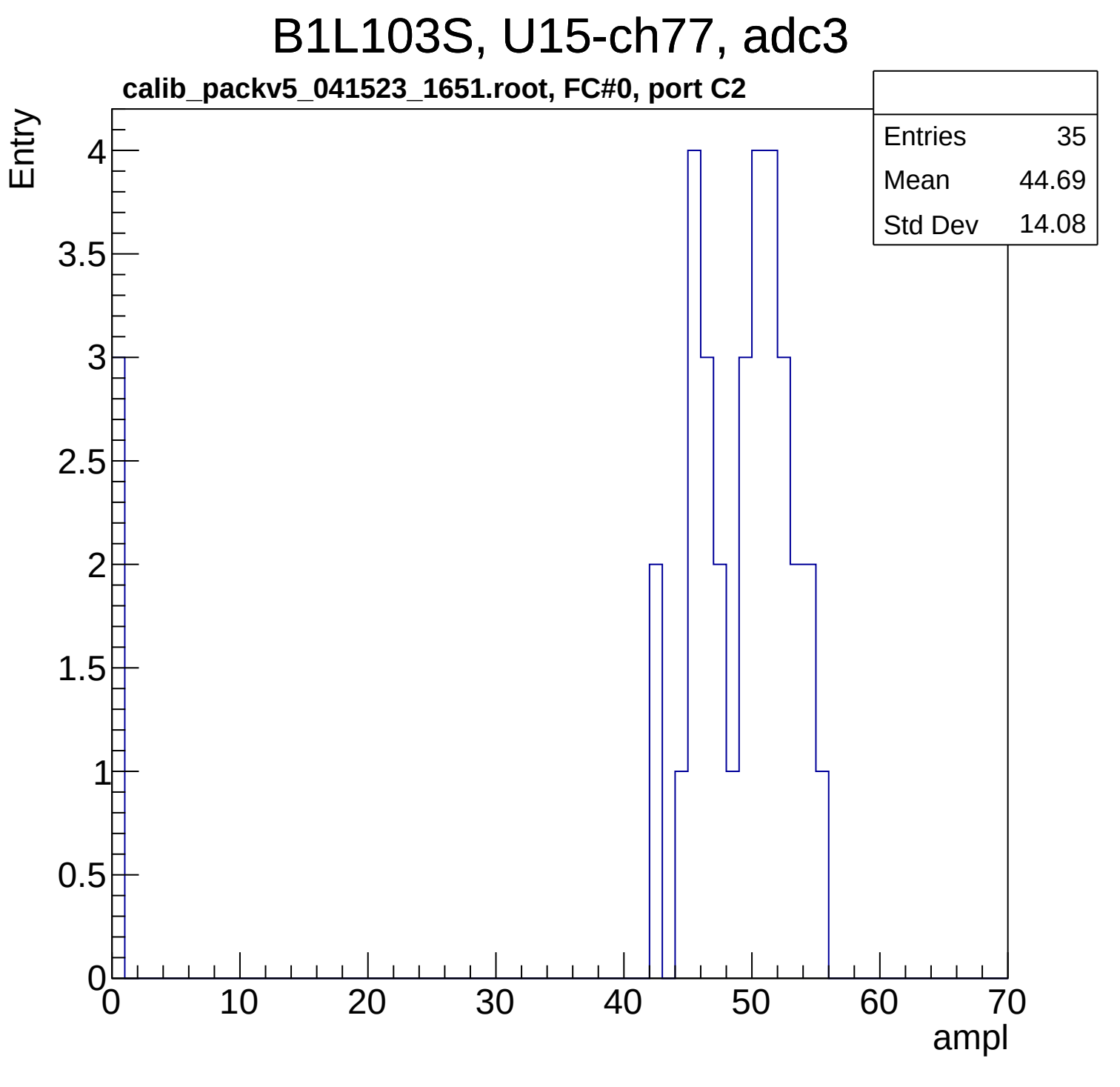
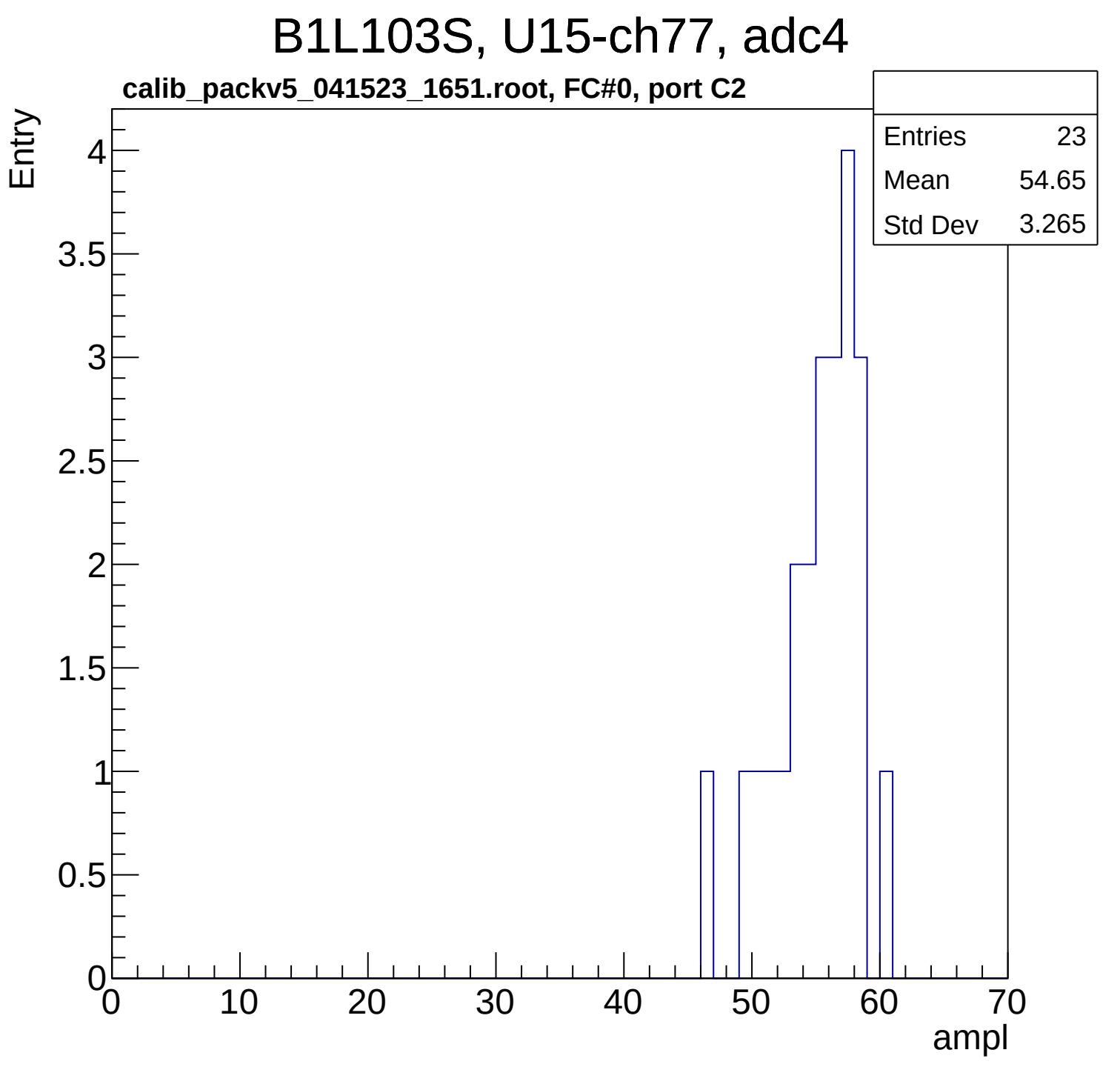

B1L103S, U15-ch77, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 36.96
Std Dev 13.33
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch77, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 44.69
Std Dev 14.08
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch77, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 54.65
Std Dev 3.265
Entry
ampl
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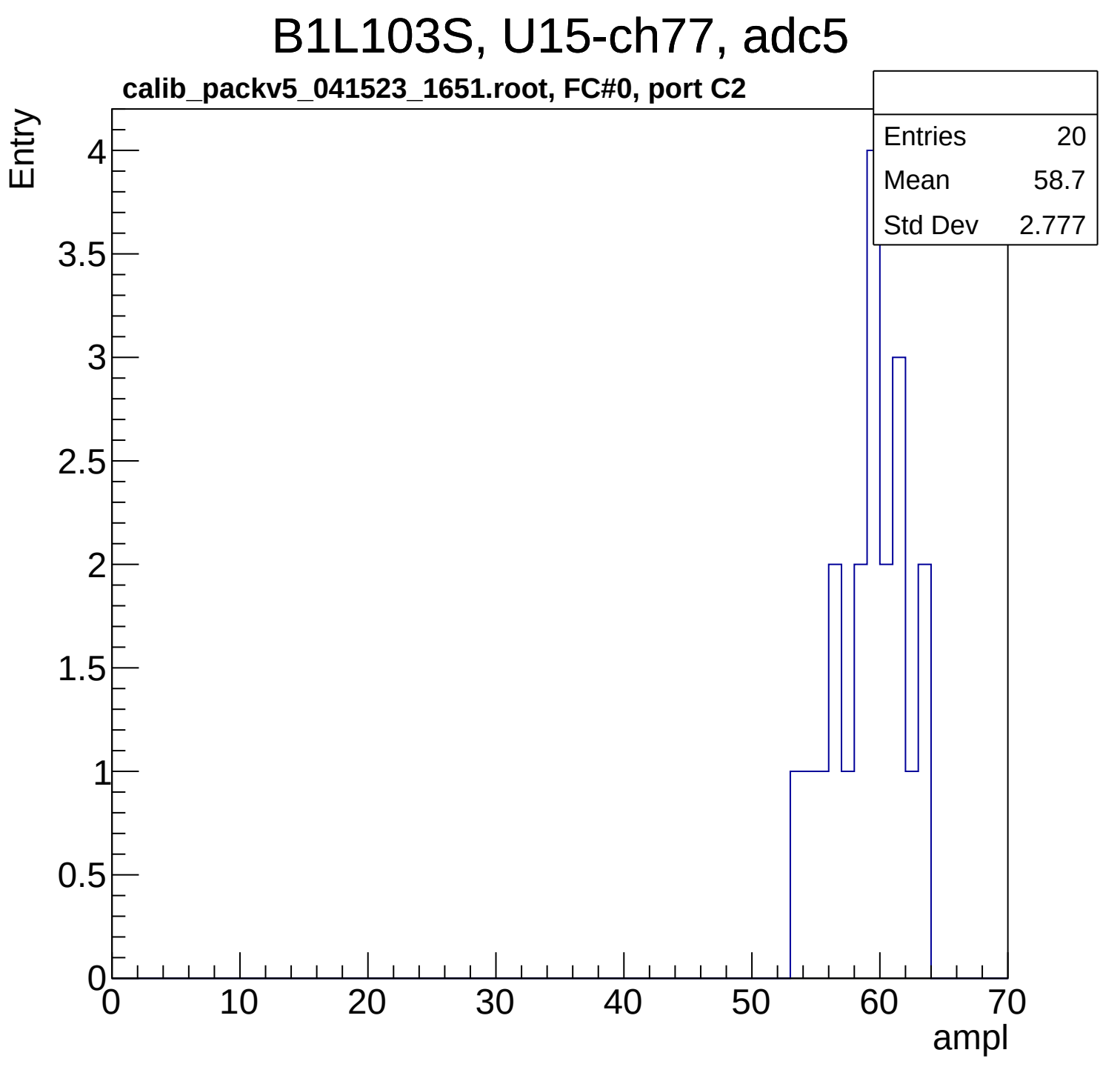
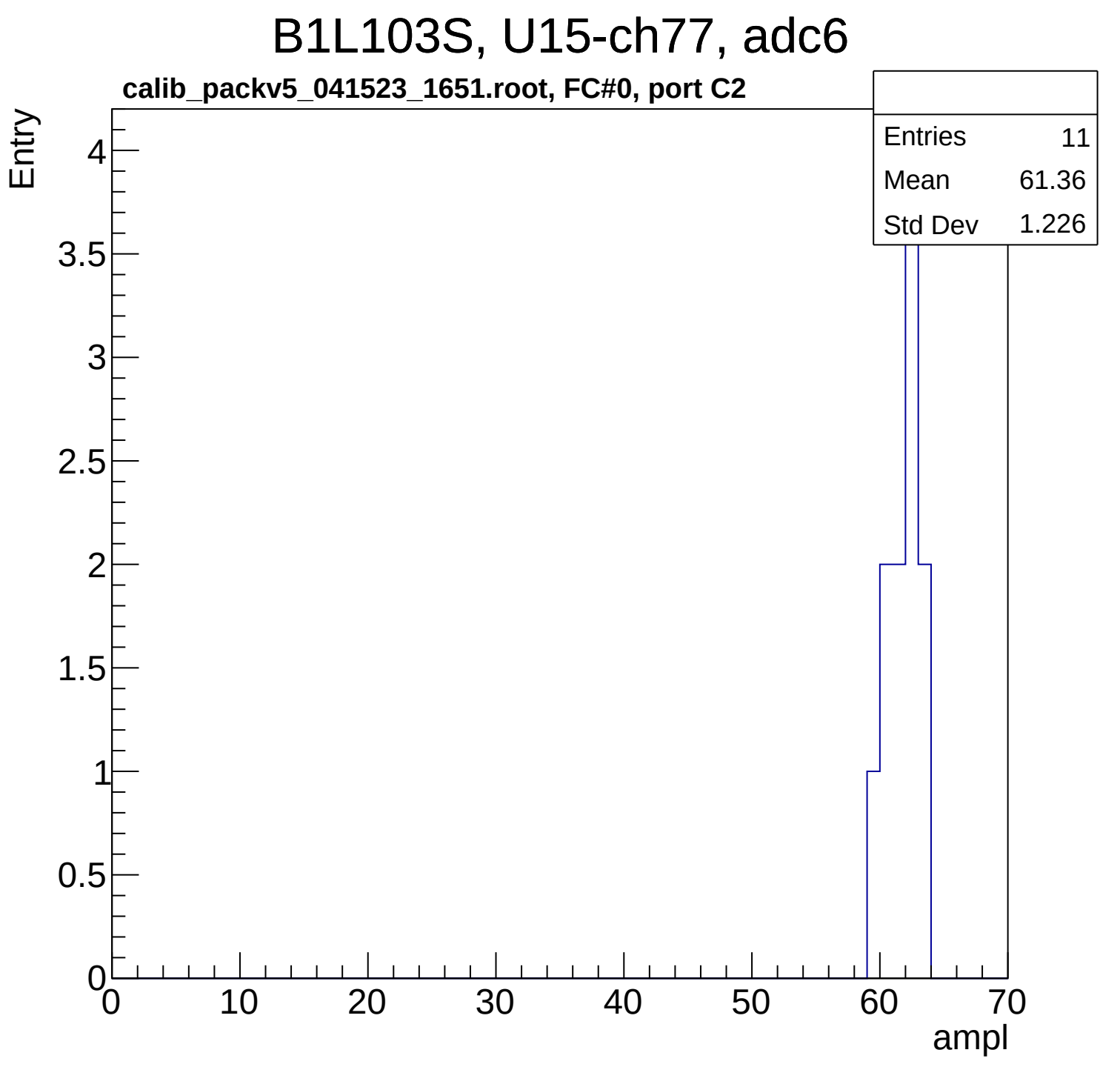
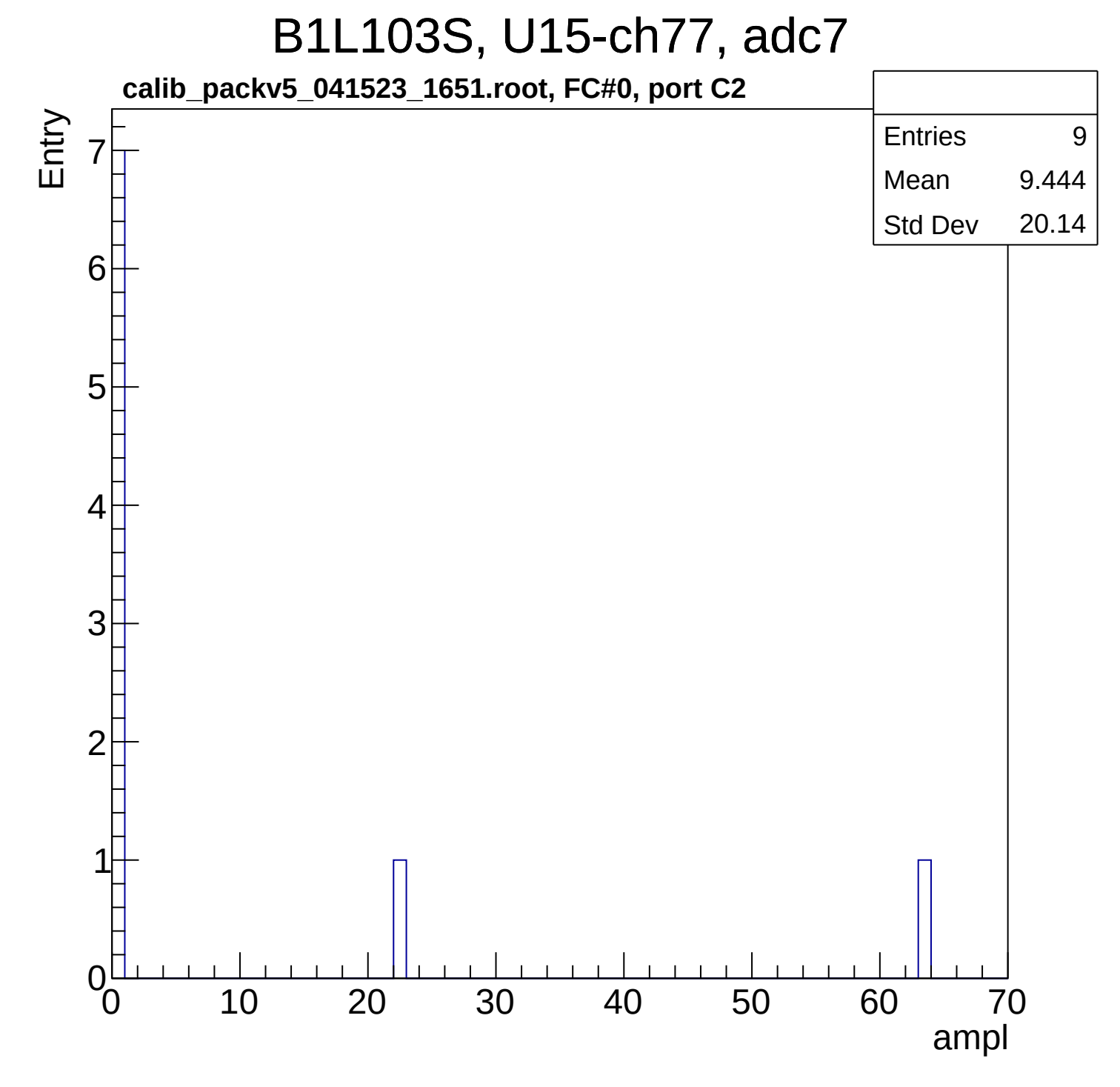
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch77, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 58.7
Std Dev 2.777
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch77, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.36
Std Dev 1.226
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch77, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 9.444
Std Dev 20.14
Entry
ampl
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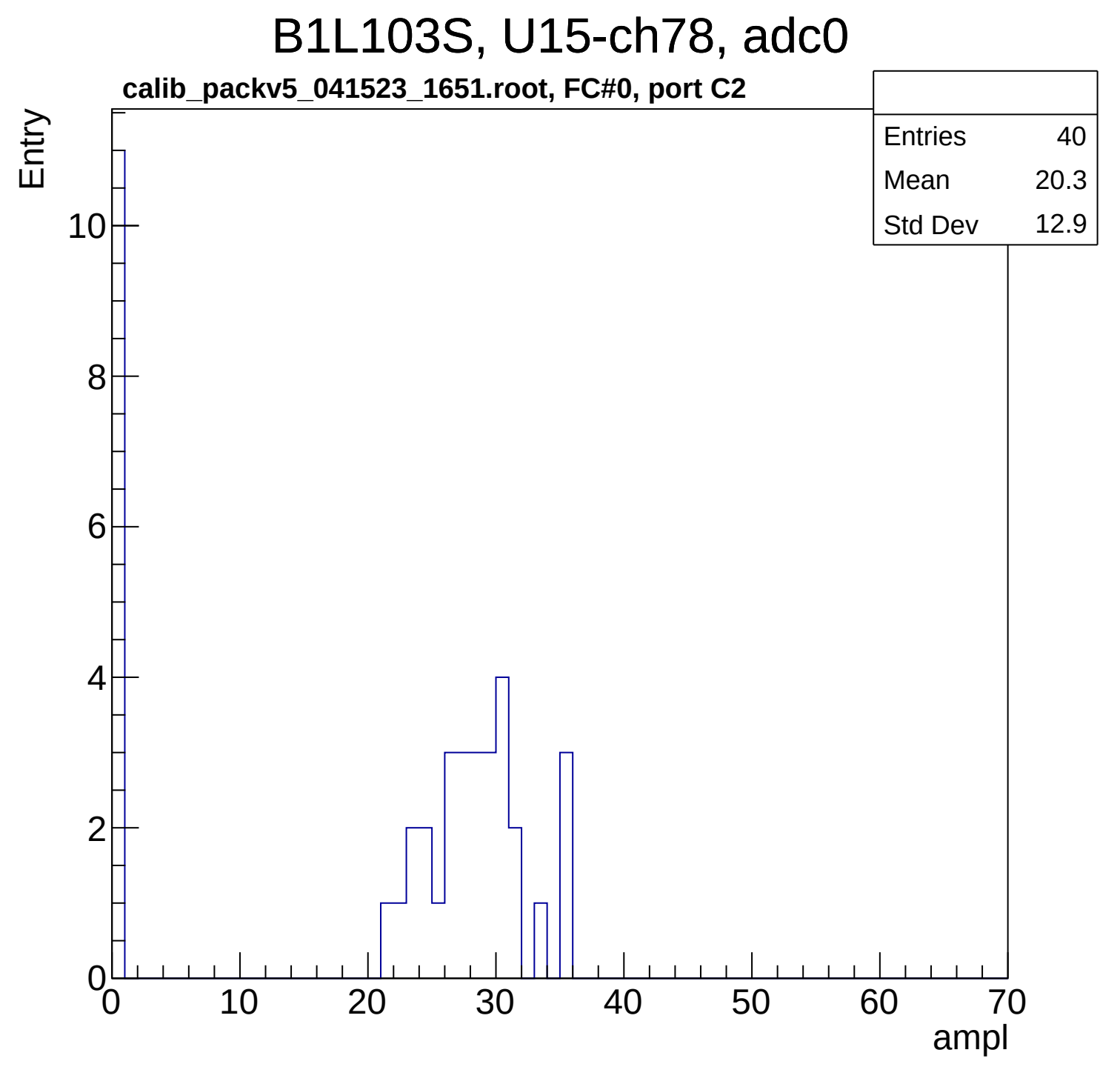
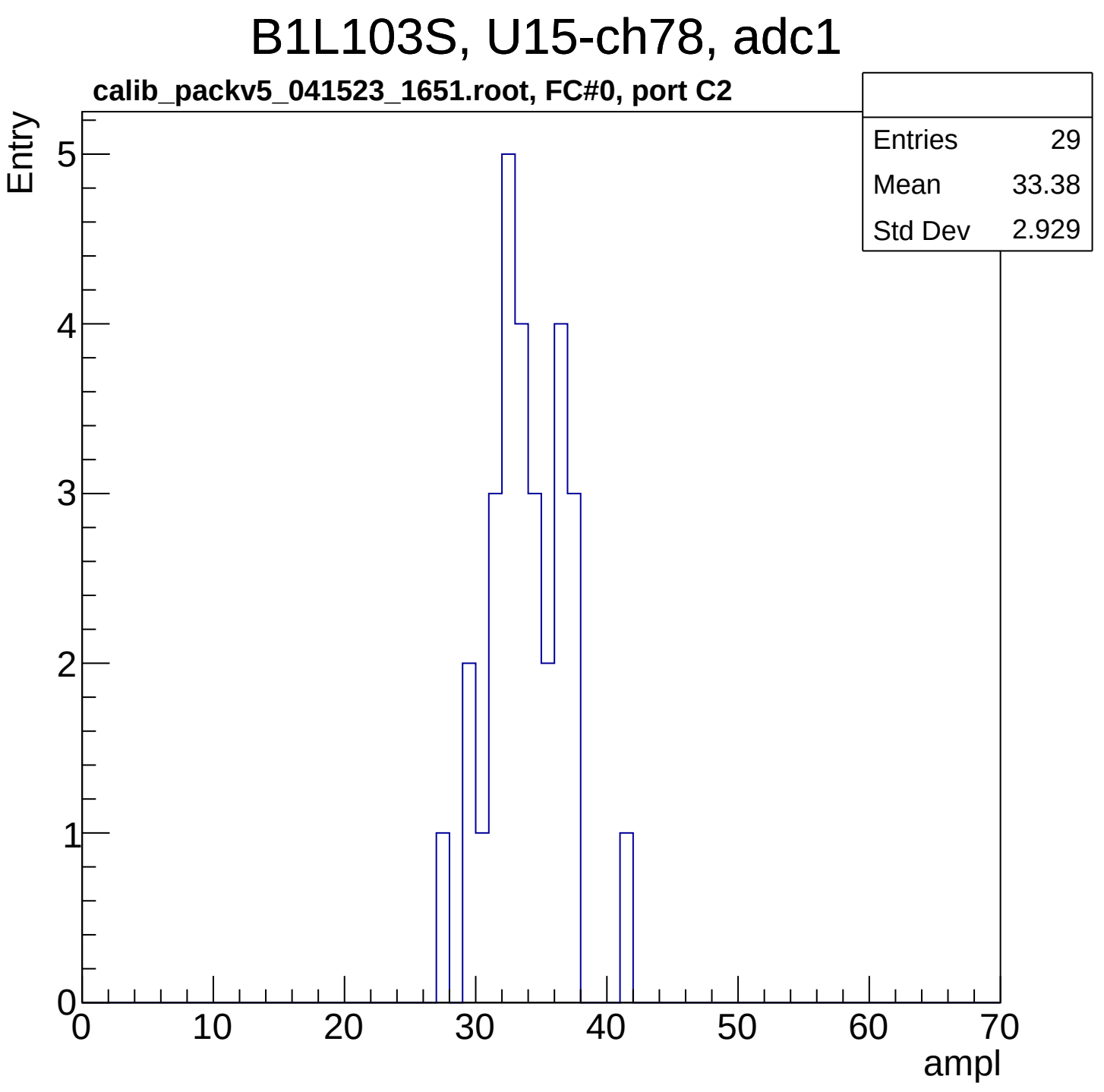
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U15-ch78, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 20.3
Std Dev 12.9
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch78, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 33.38
Std Dev 2.929
Entry
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1
2
3
4
5
0
10
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30
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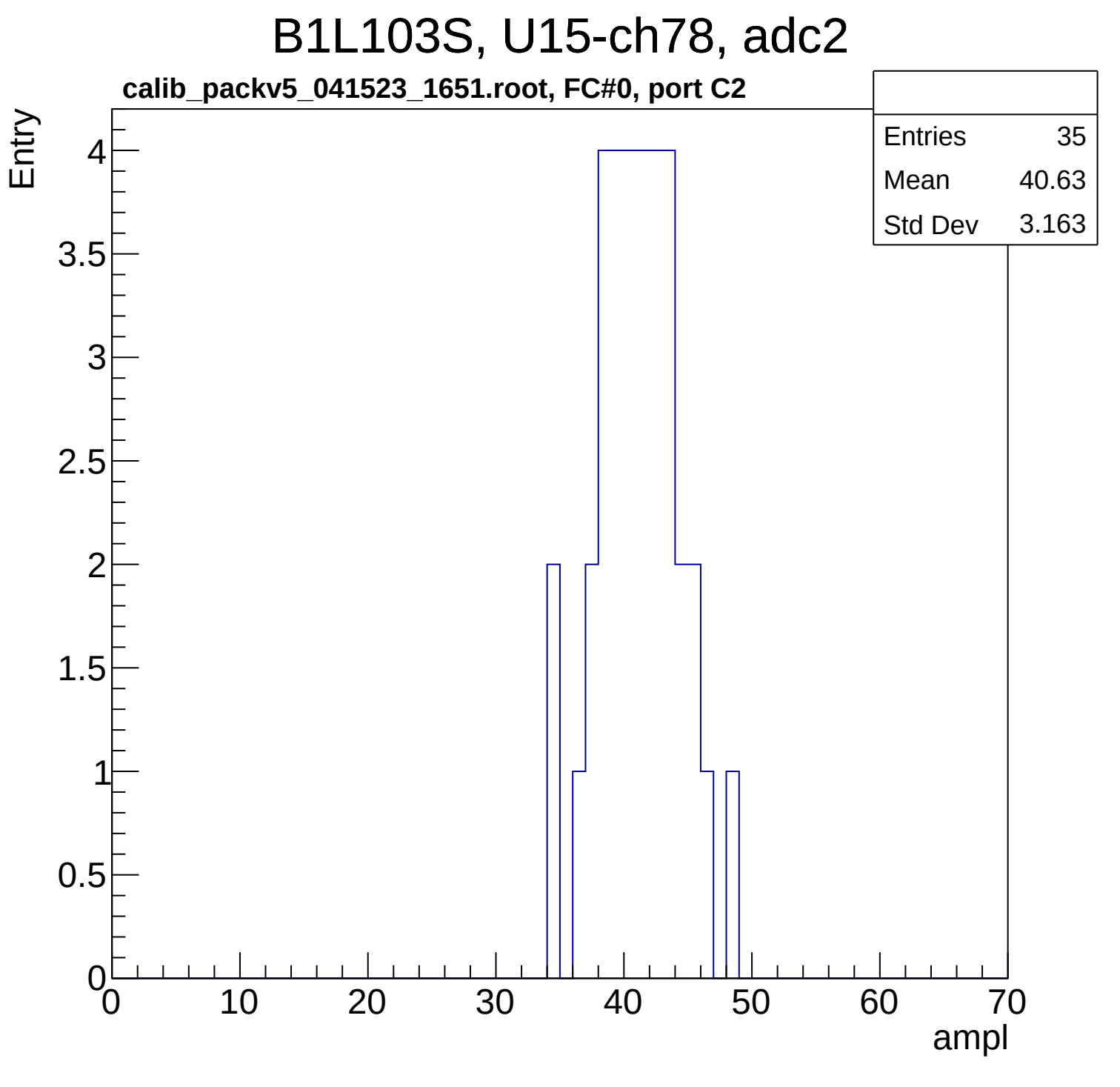
50
60
70
ampl


B1L103S, U15-ch78, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 40.63
Std Dev 3.163
Entry
ampl
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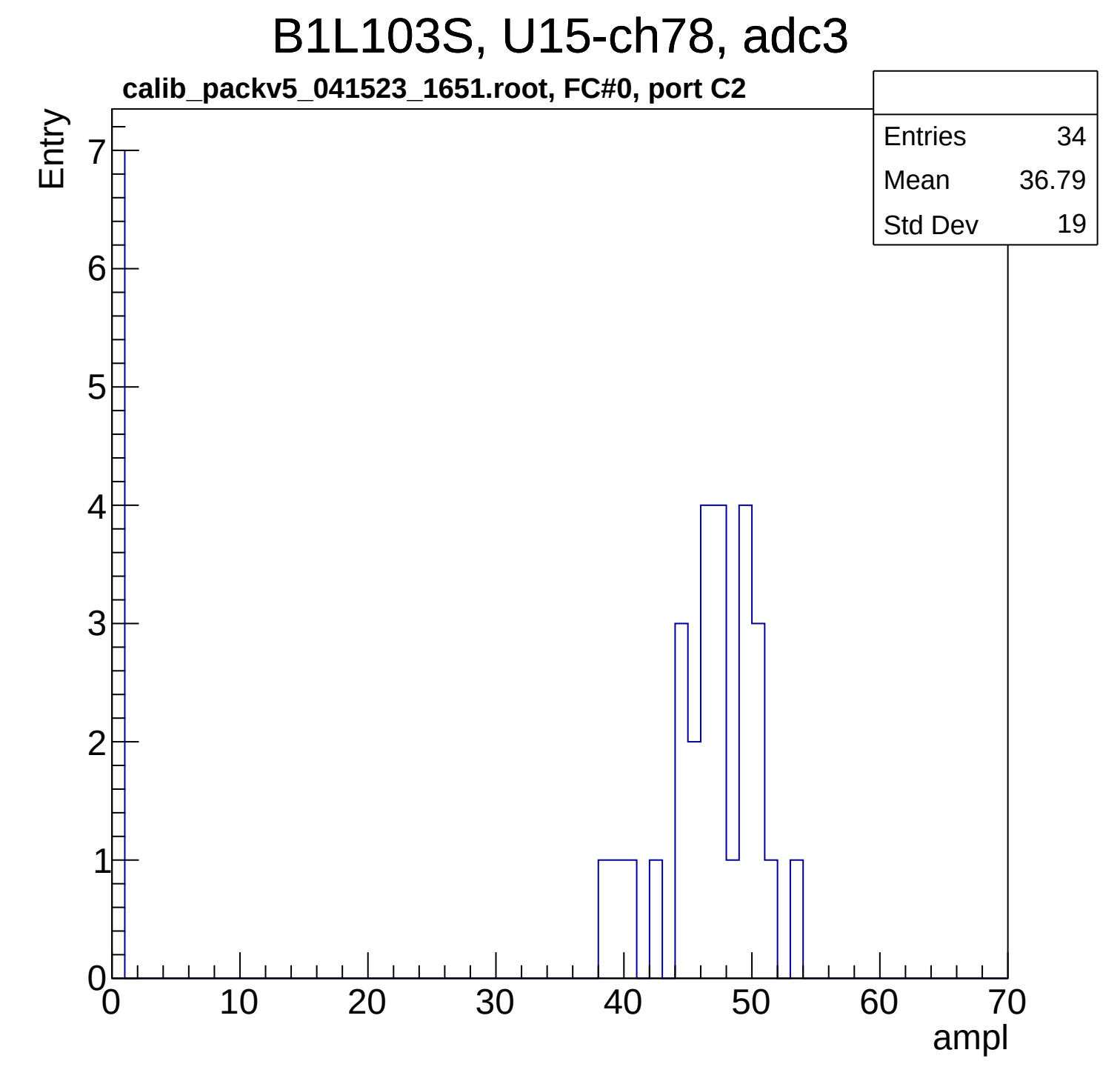
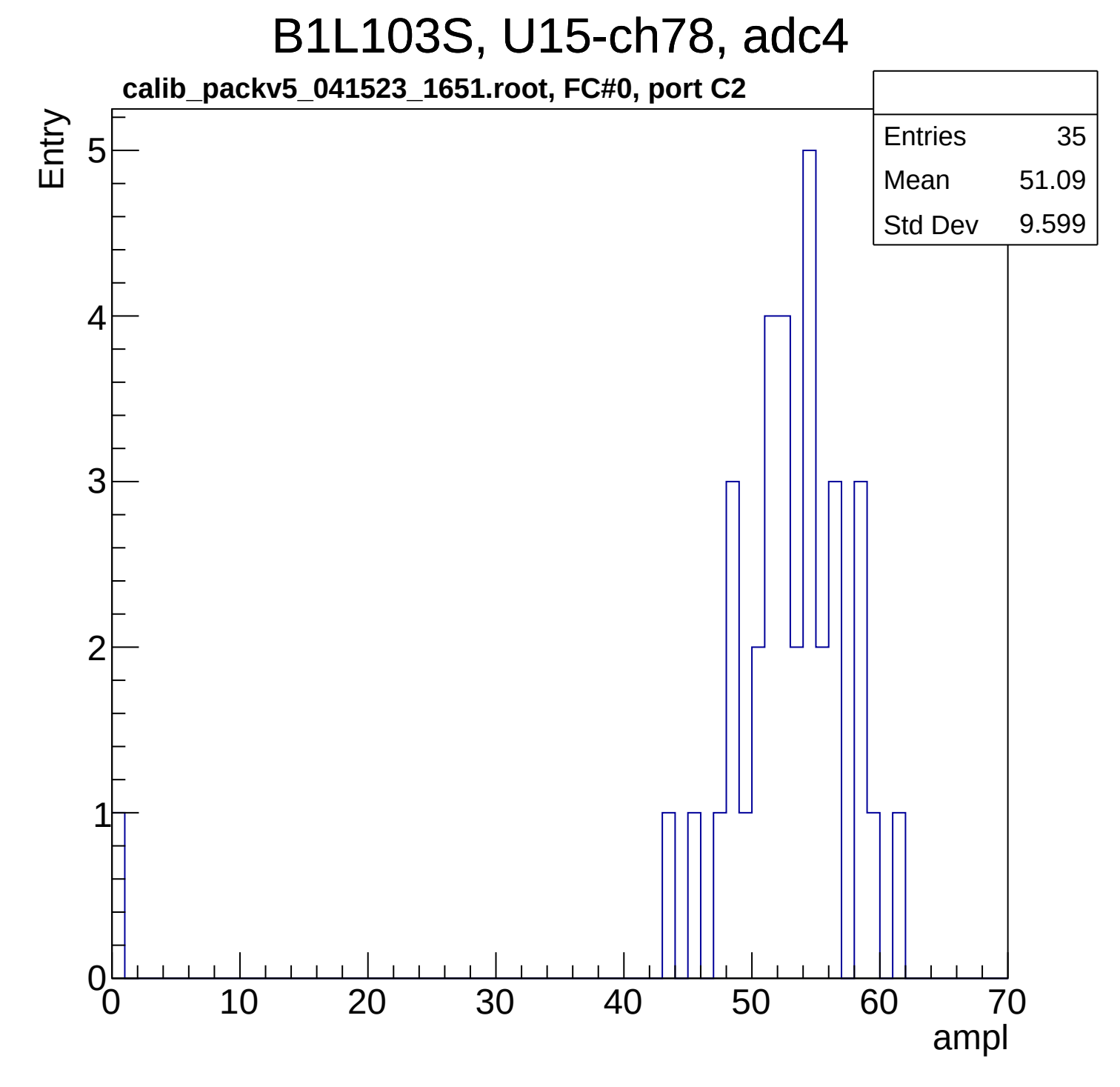
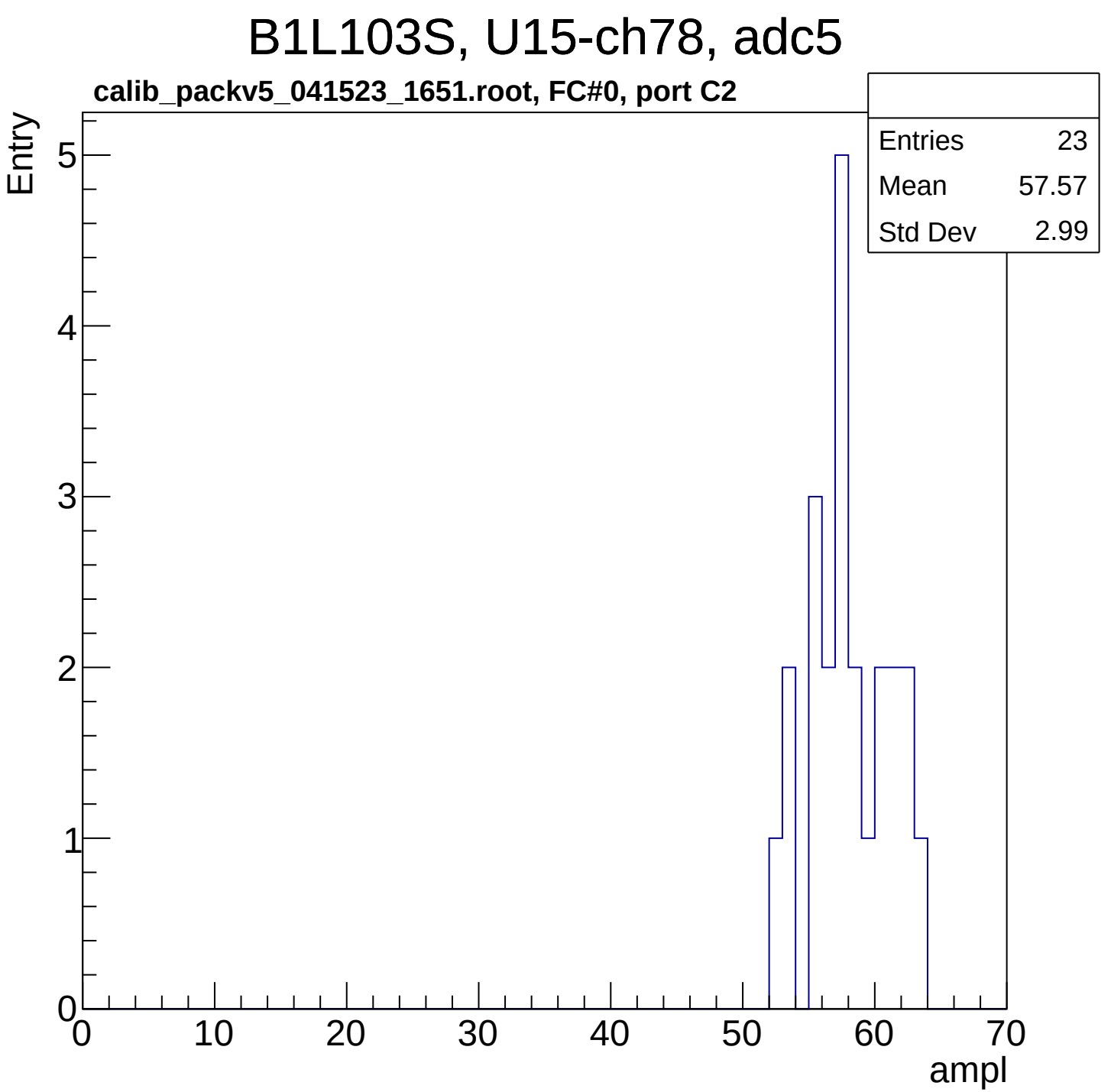
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch78, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 36.79
Std Dev 19
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U15-ch78, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 51.09
Std Dev 9.599
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch78, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 57.57
Std Dev 2.99
Entry
0
1
2
3
4
5
0
10
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30
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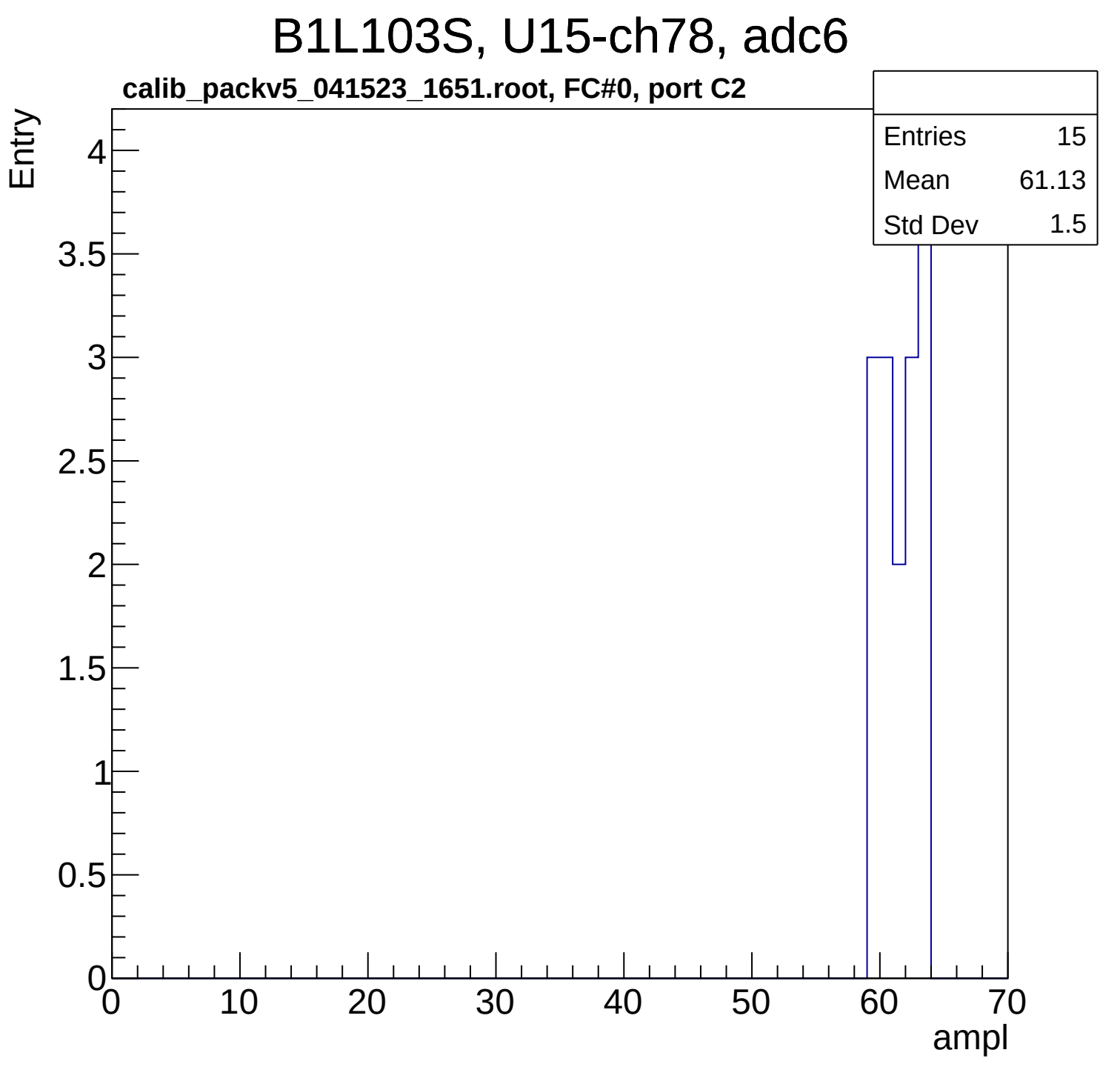
50
60
70
ampl


B1L103S, U15-ch78, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.13
Std Dev 1.5
Entry
ampl
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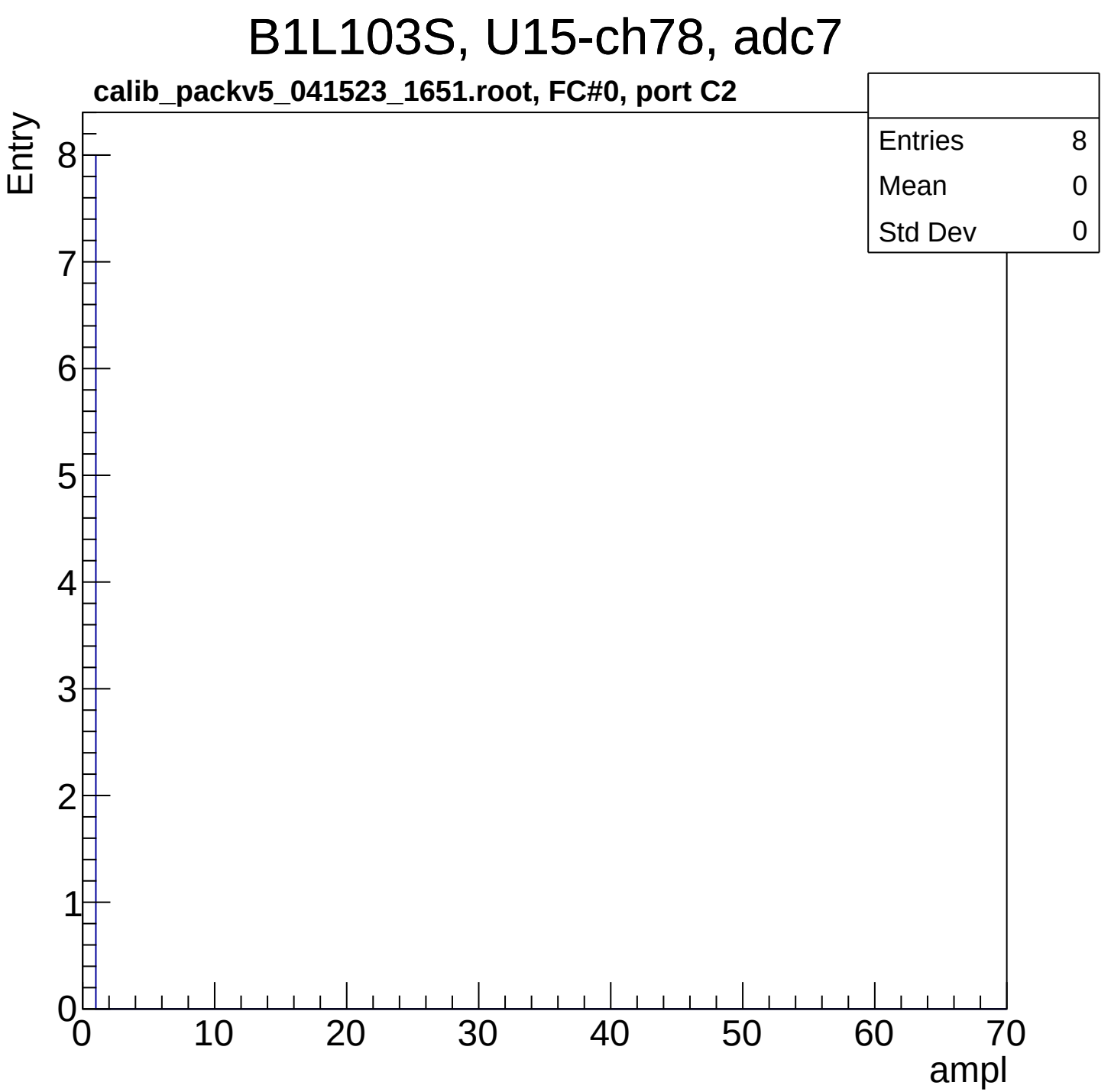
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch78, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 0
Std Dev 0
Entry
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1
2
3
4
5
6
7
8
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10
20
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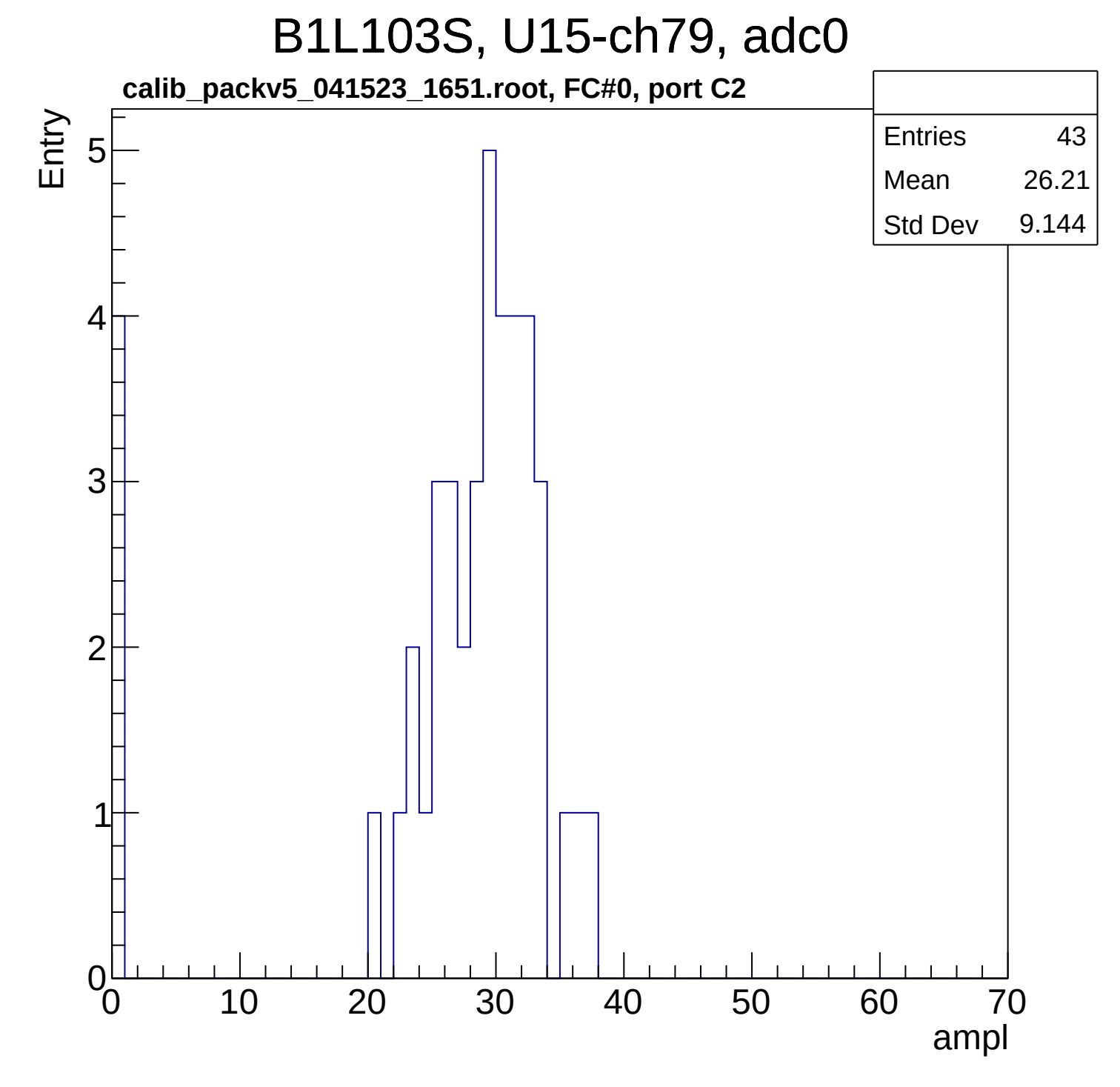
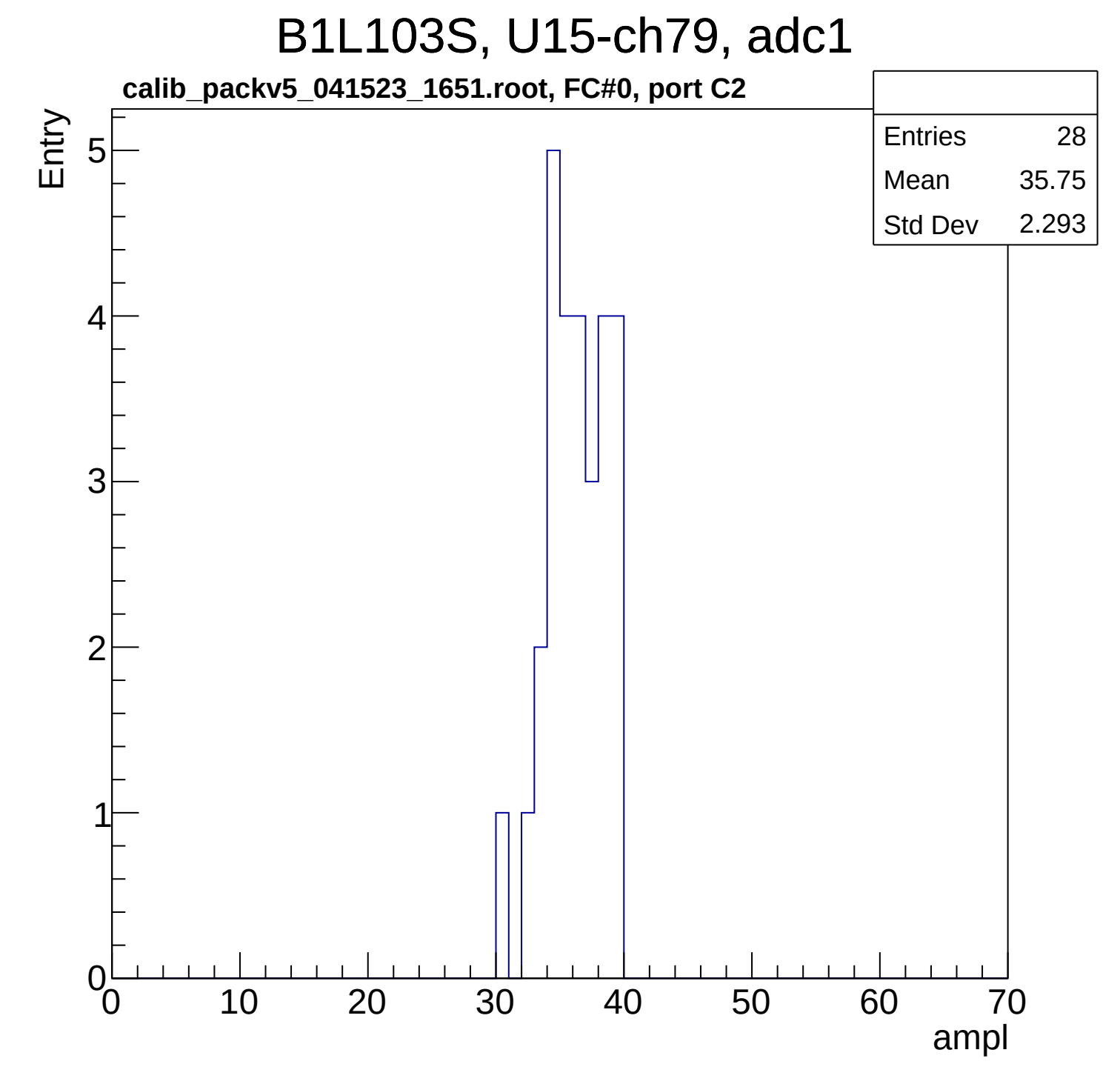
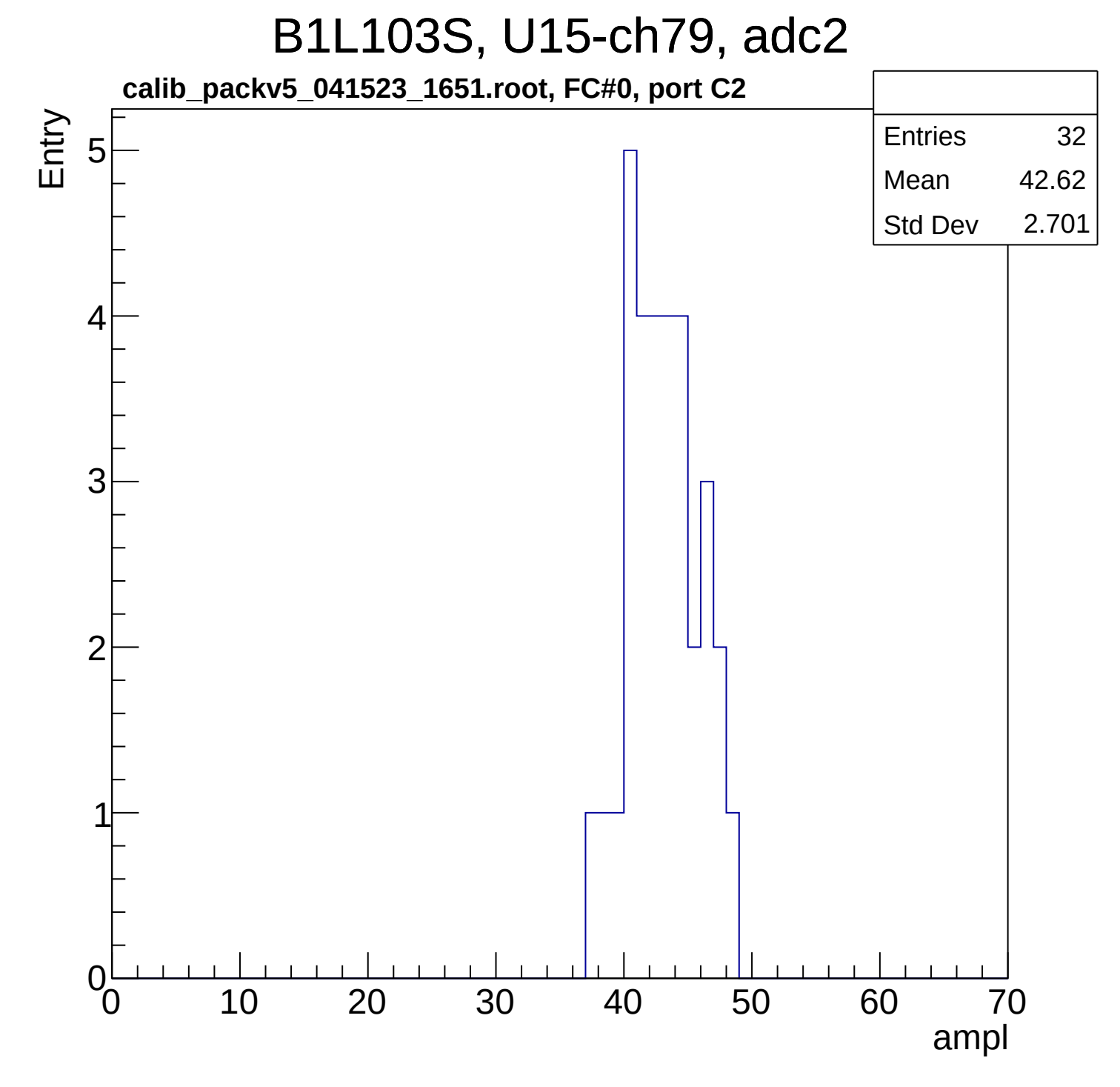
50
60
70
ampl


B1L103S, U15-ch79, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 26.21
Std Dev 9.144
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch79, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 35.75
Std Dev 2.293
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch79, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 42.62
Std Dev 2.701
Entry
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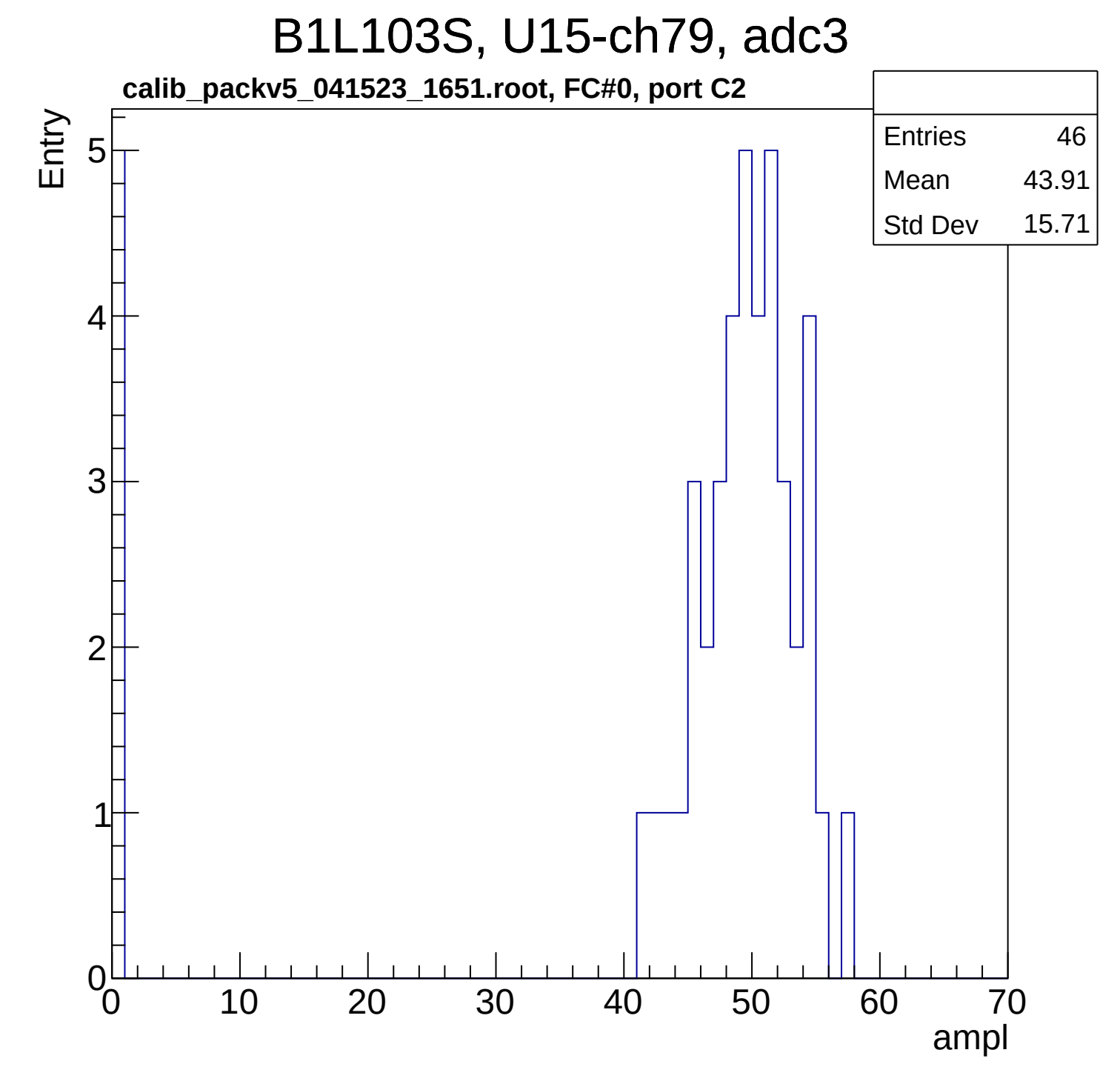
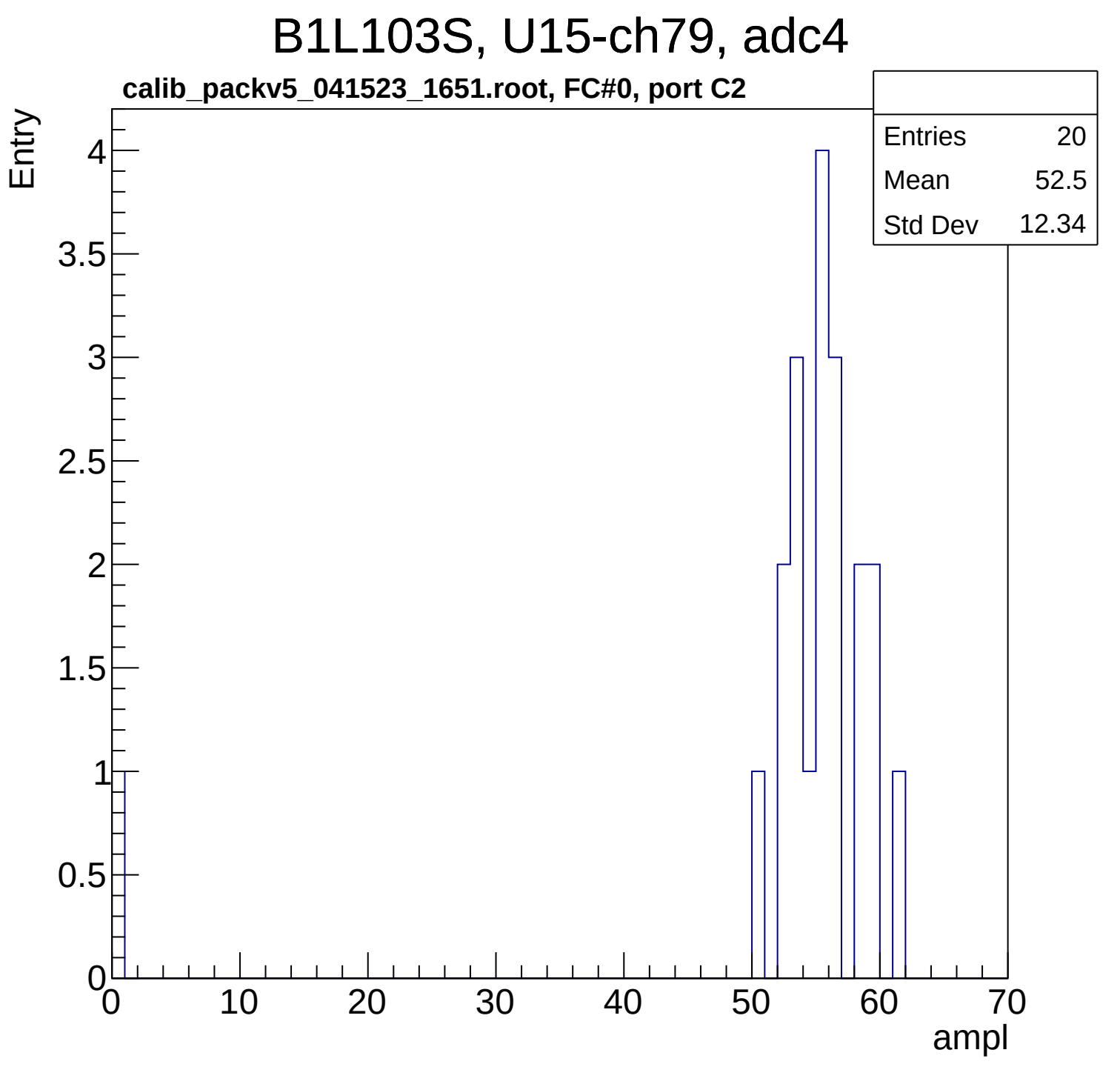
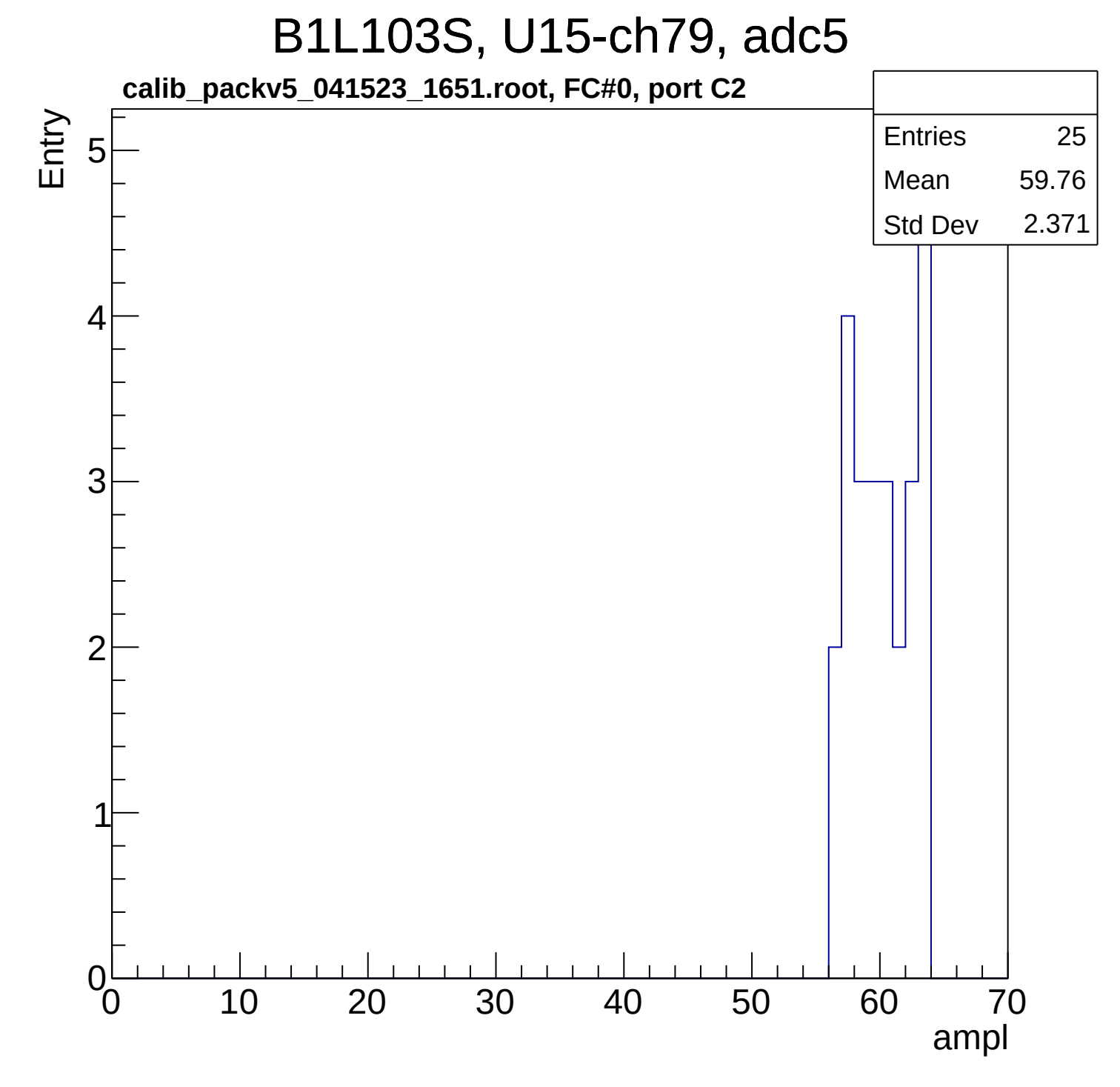
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch79, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 43.91
Std Dev 15.71
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch79, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 52.5
Std Dev 12.34
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch79, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 59.76
Std Dev 2.371
Entry
ampl
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1
2
3
4
5
0
10
20
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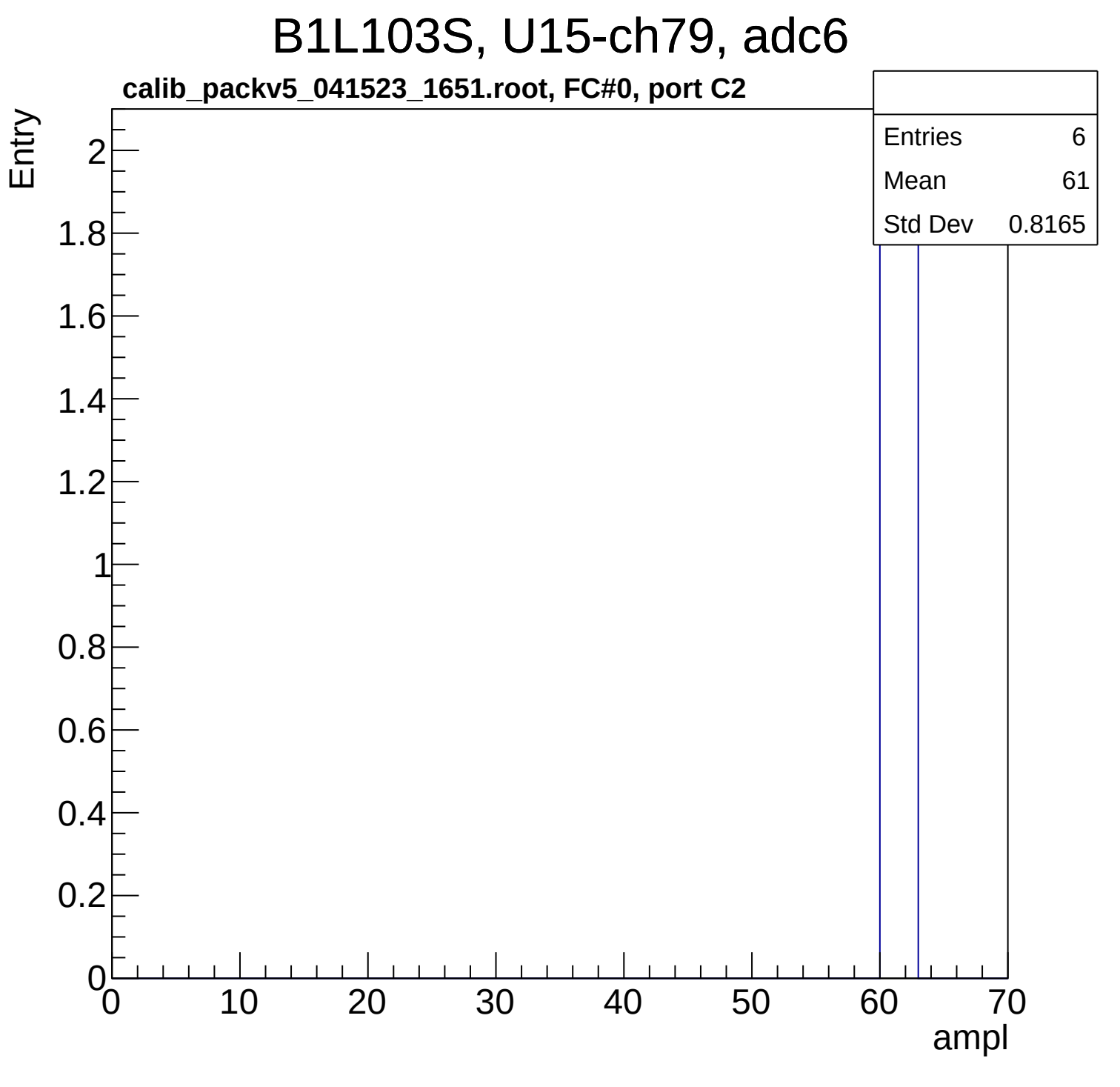
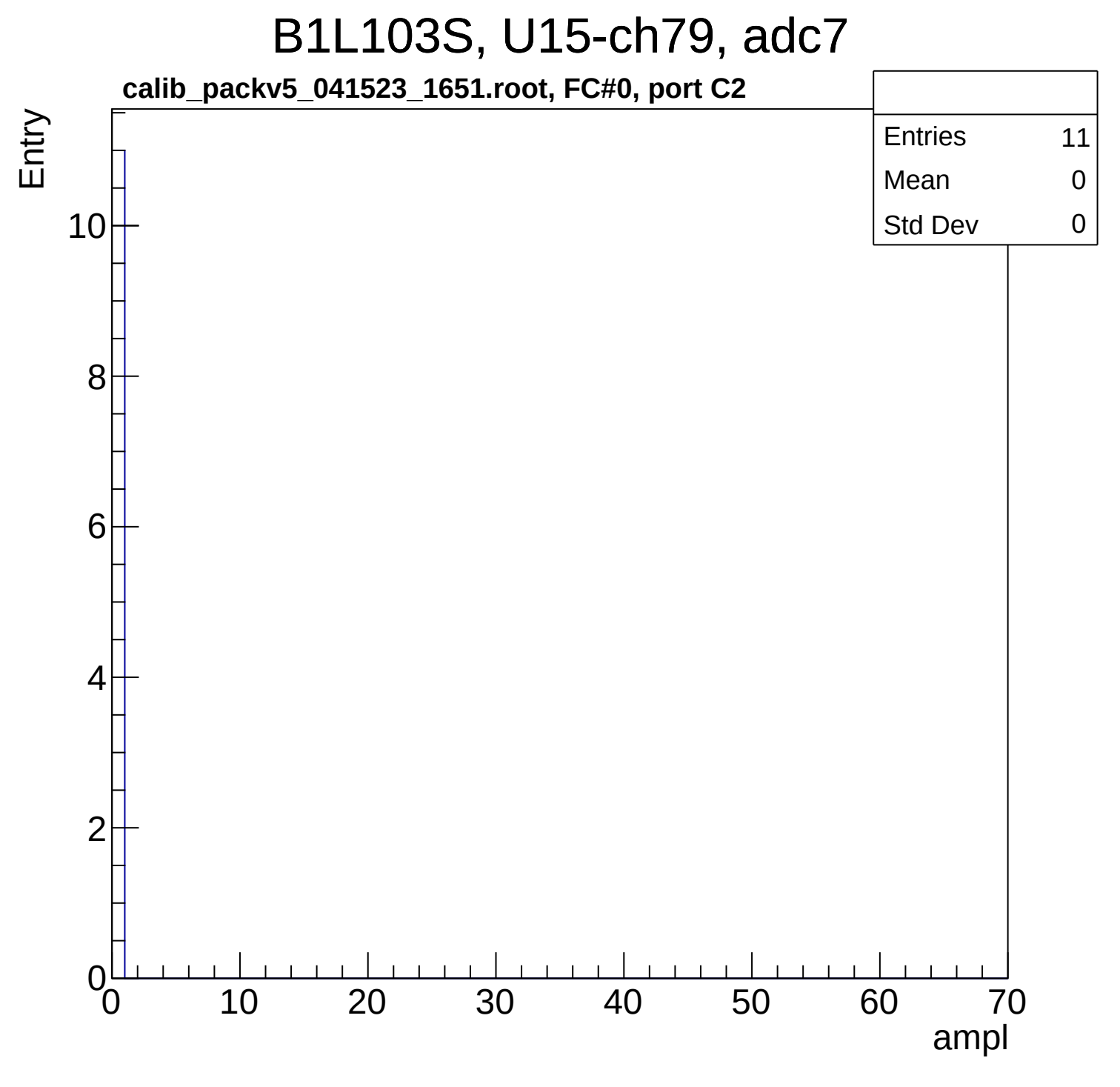
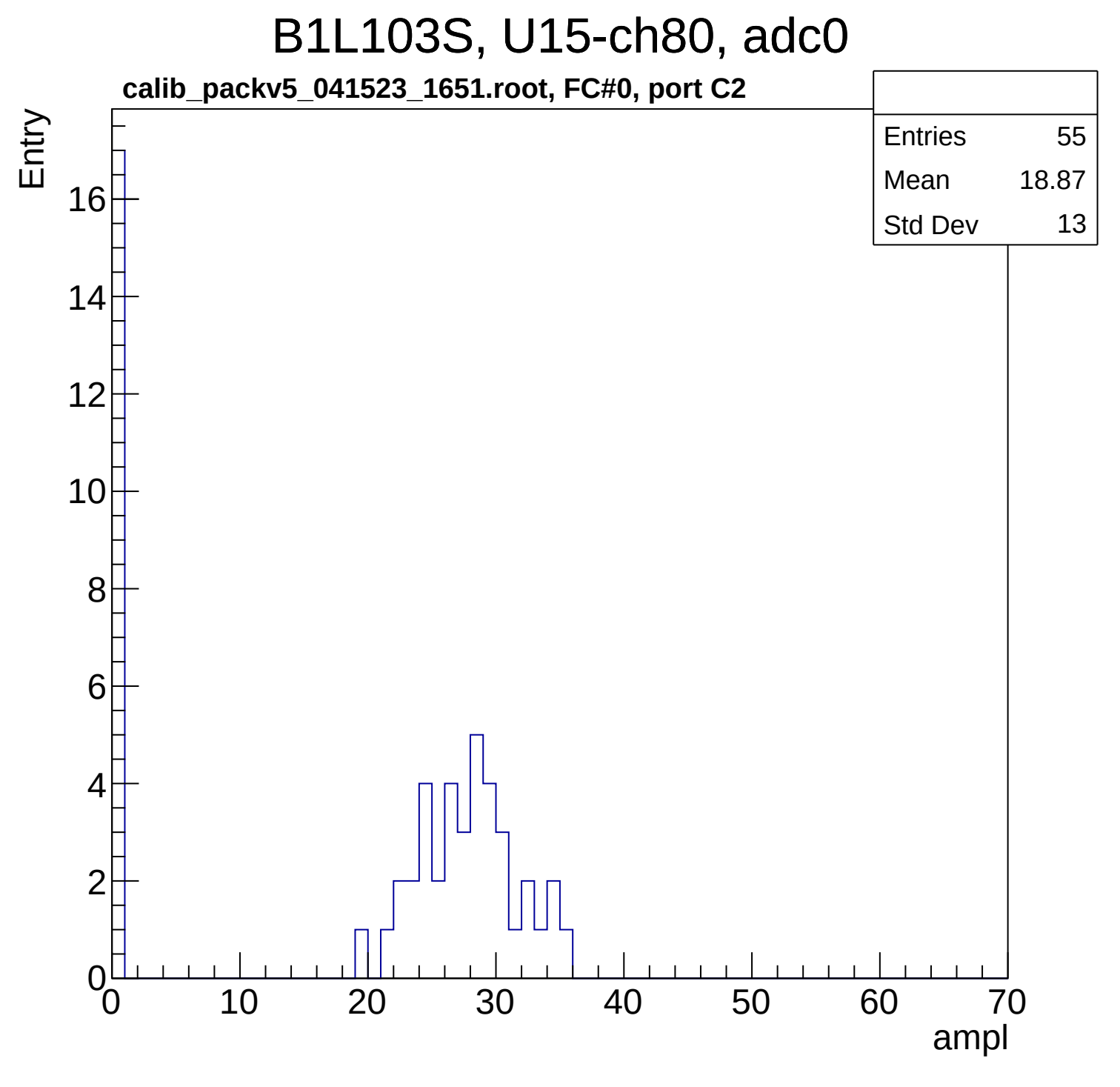
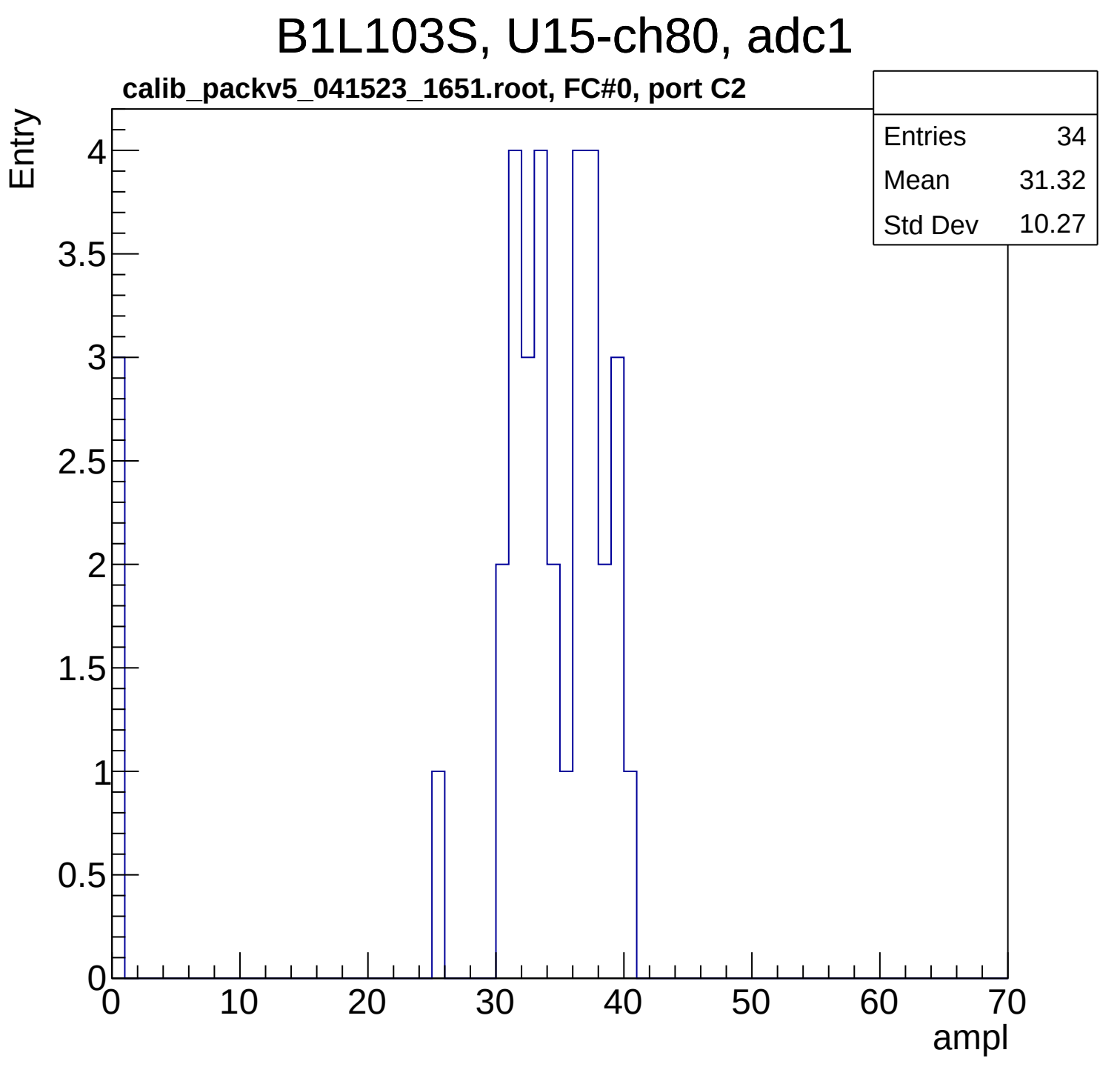
40
50
60
70


B1L103S, U15-ch79, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61
Std Dev 0.8165
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U15-ch79, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch80, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 18.87
Std Dev 13
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch80, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 31.32
Std Dev 10.27
Entry
ampl
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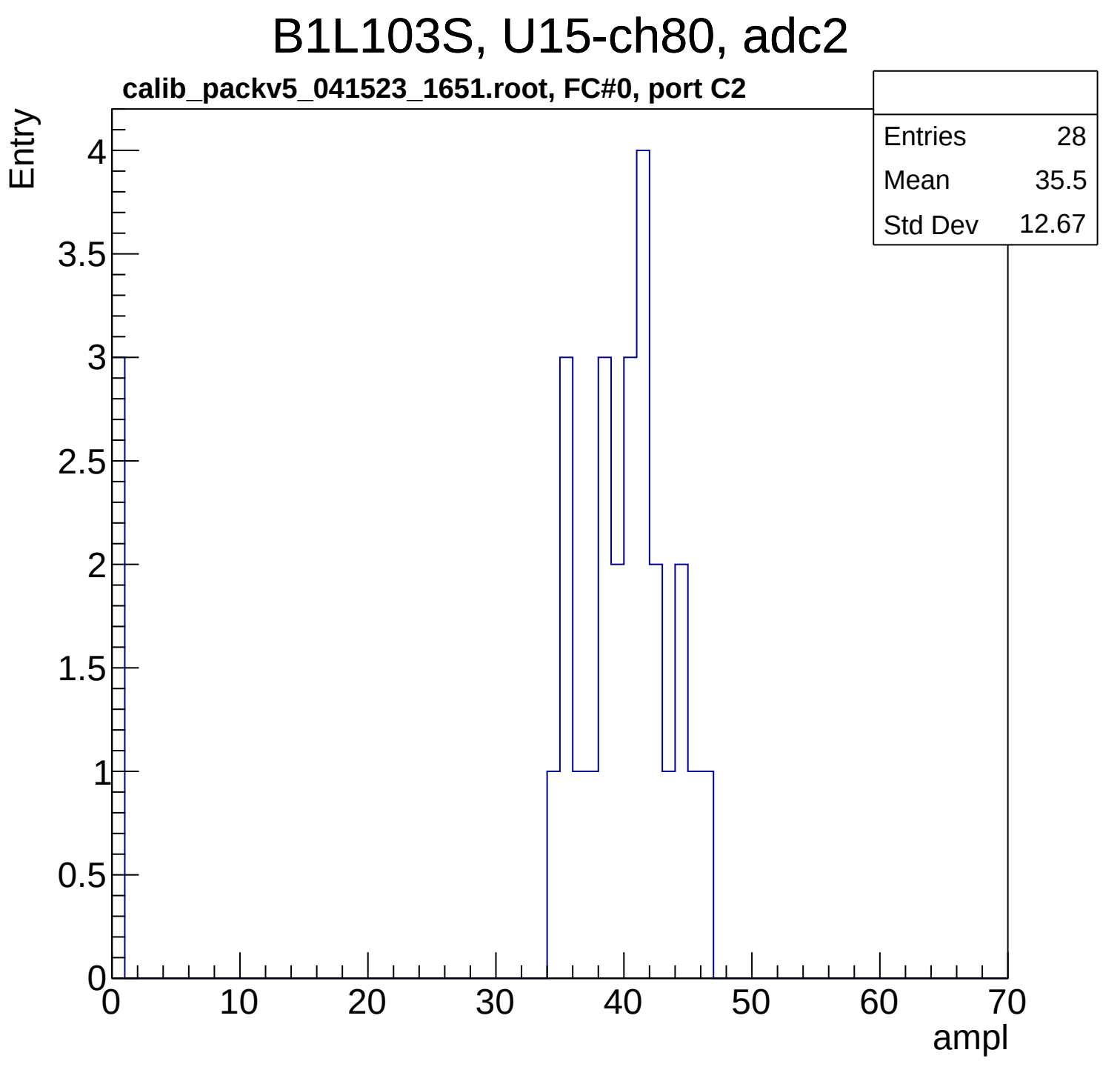
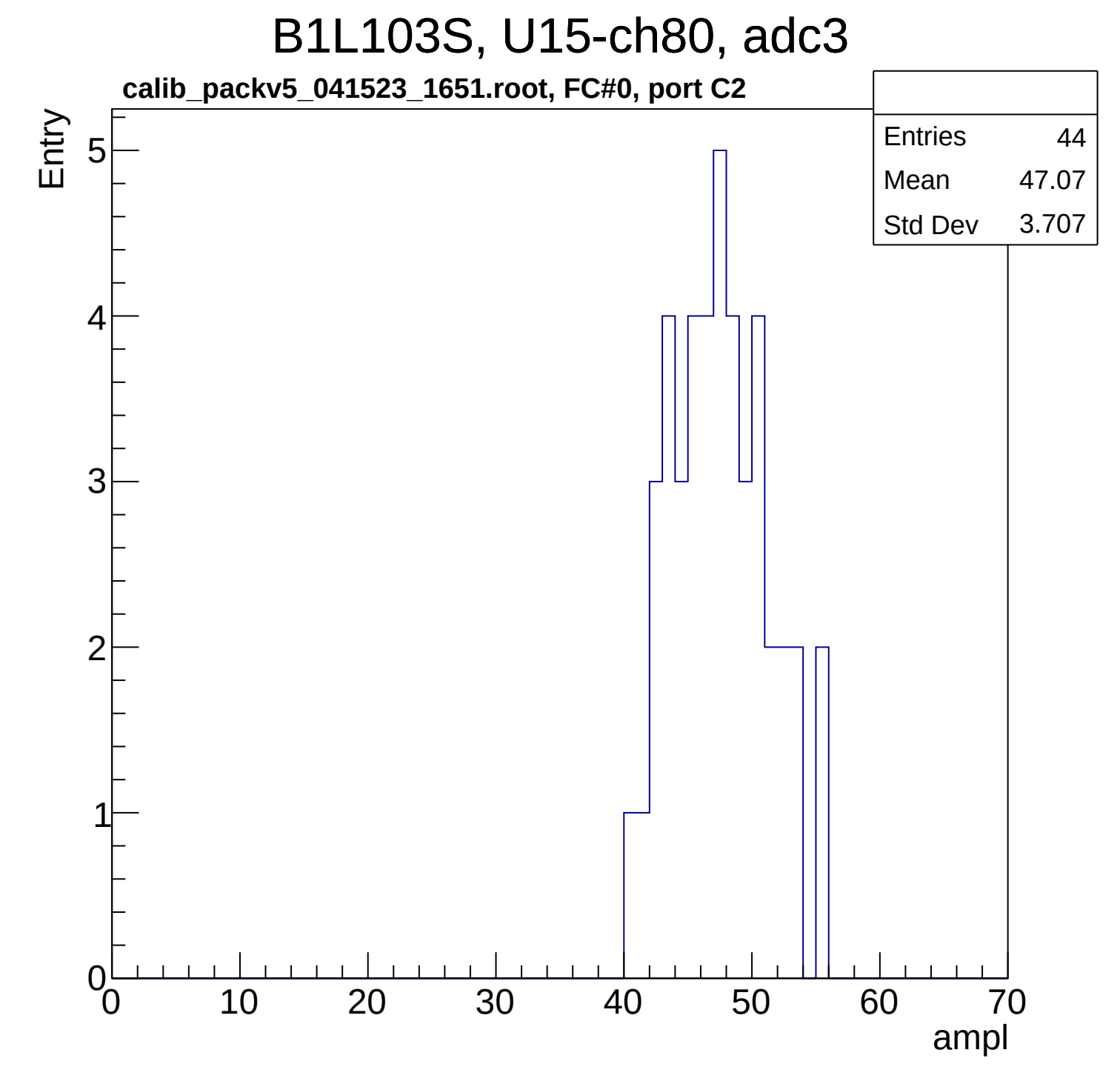
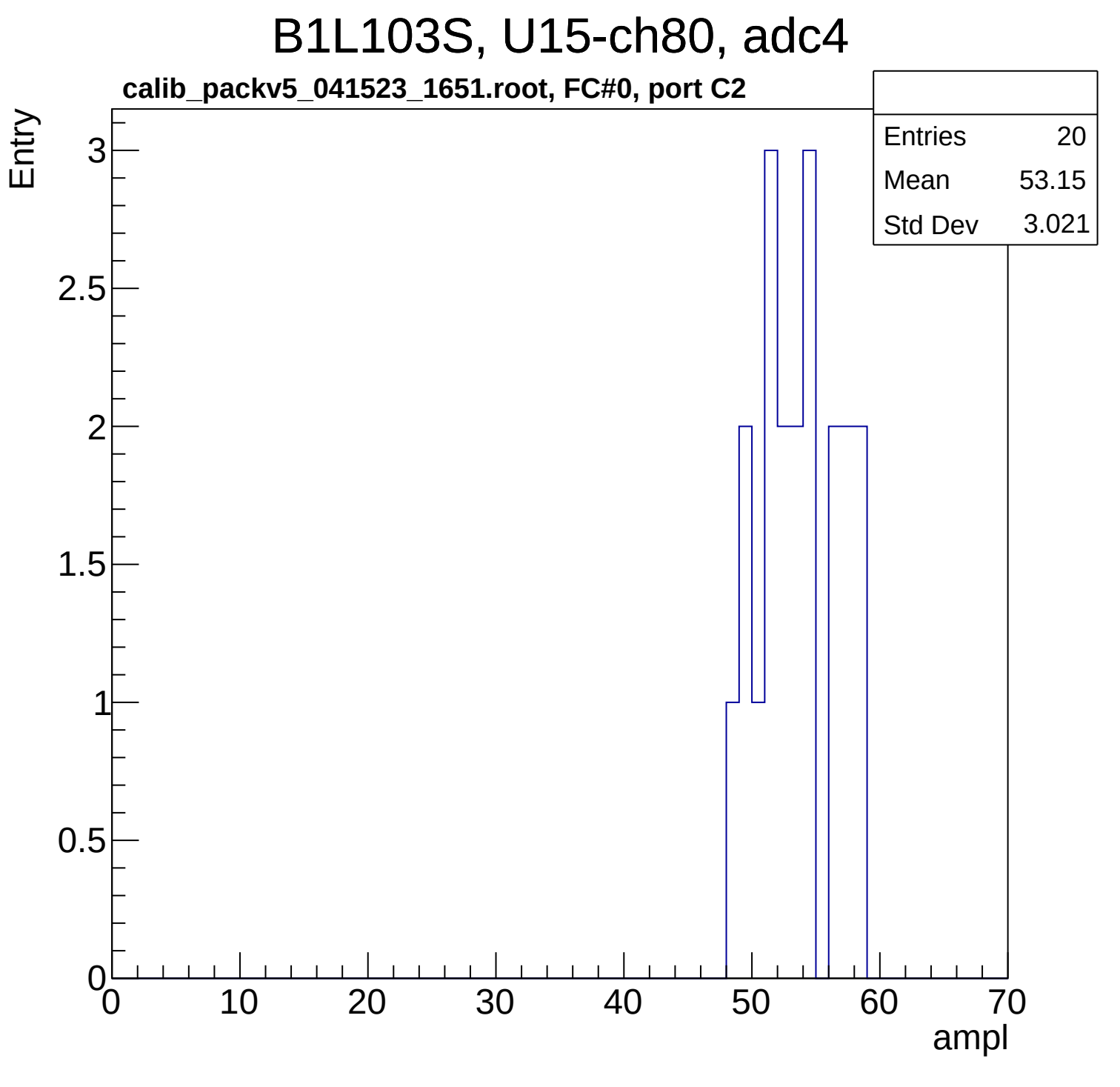
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch80, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 35.5
Std Dev 12.67
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch80, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 47.07
Std Dev 3.707
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch80, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 53.15
Std Dev 3.021
Entry
ampl
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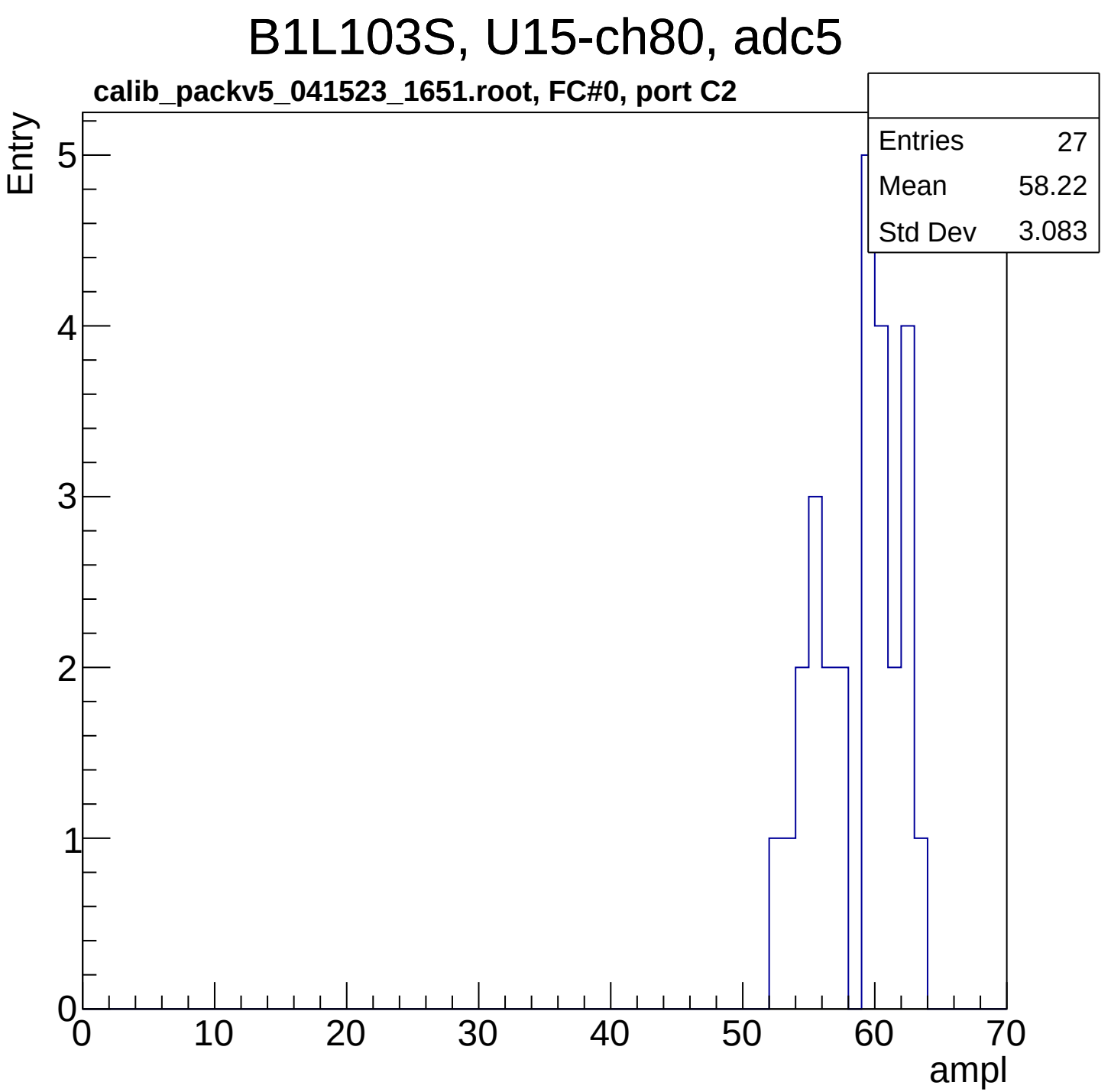
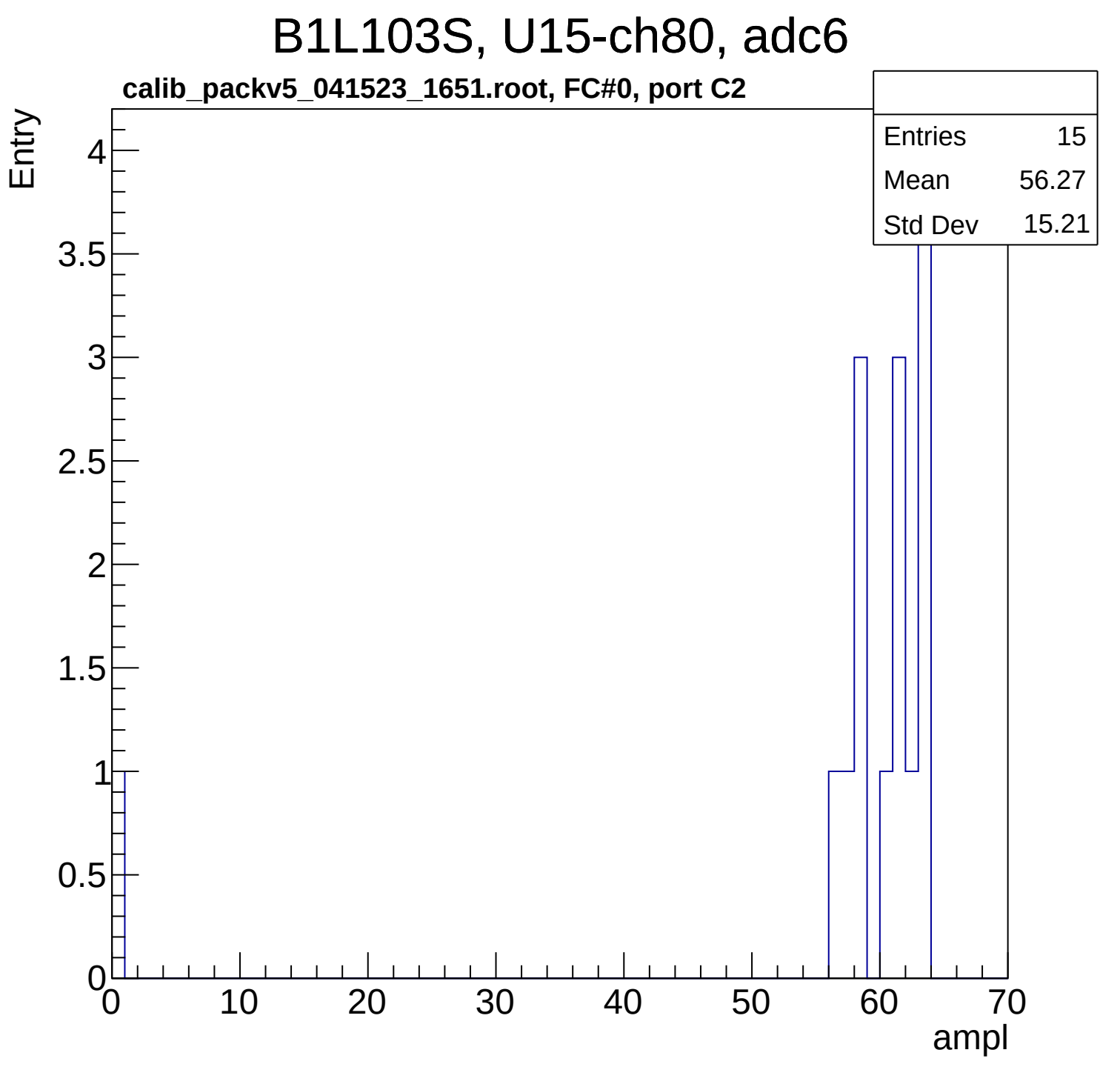
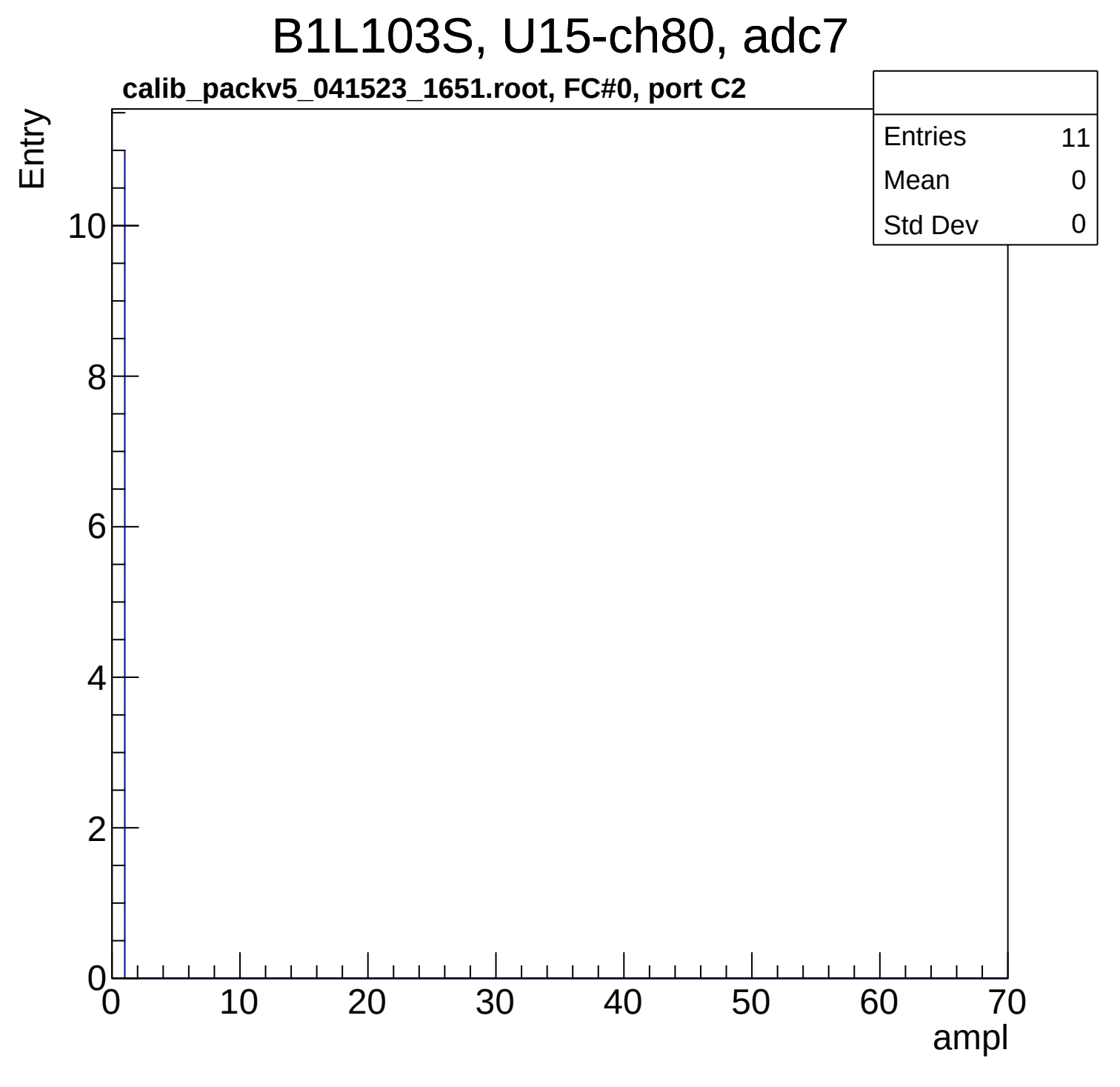
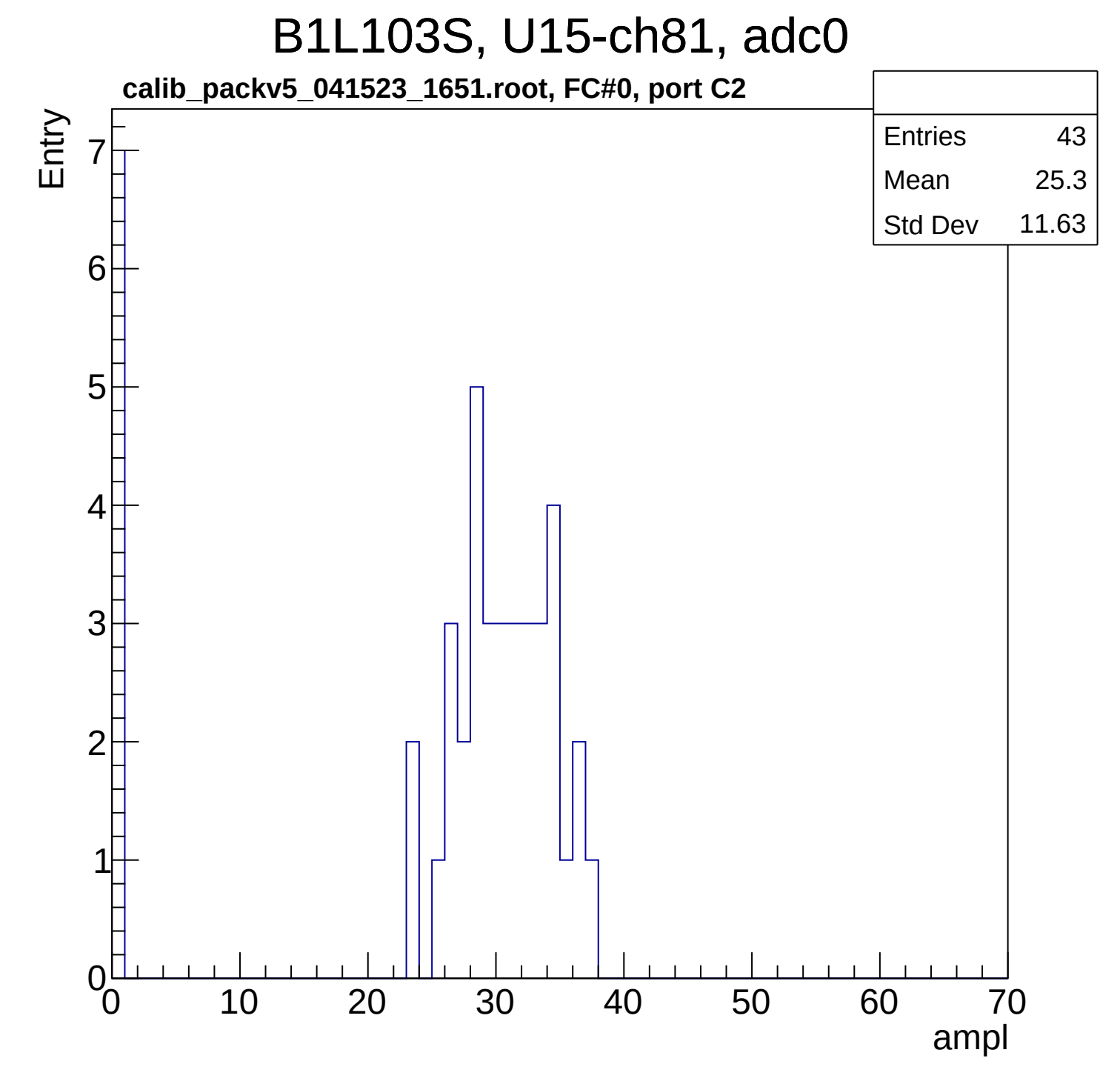
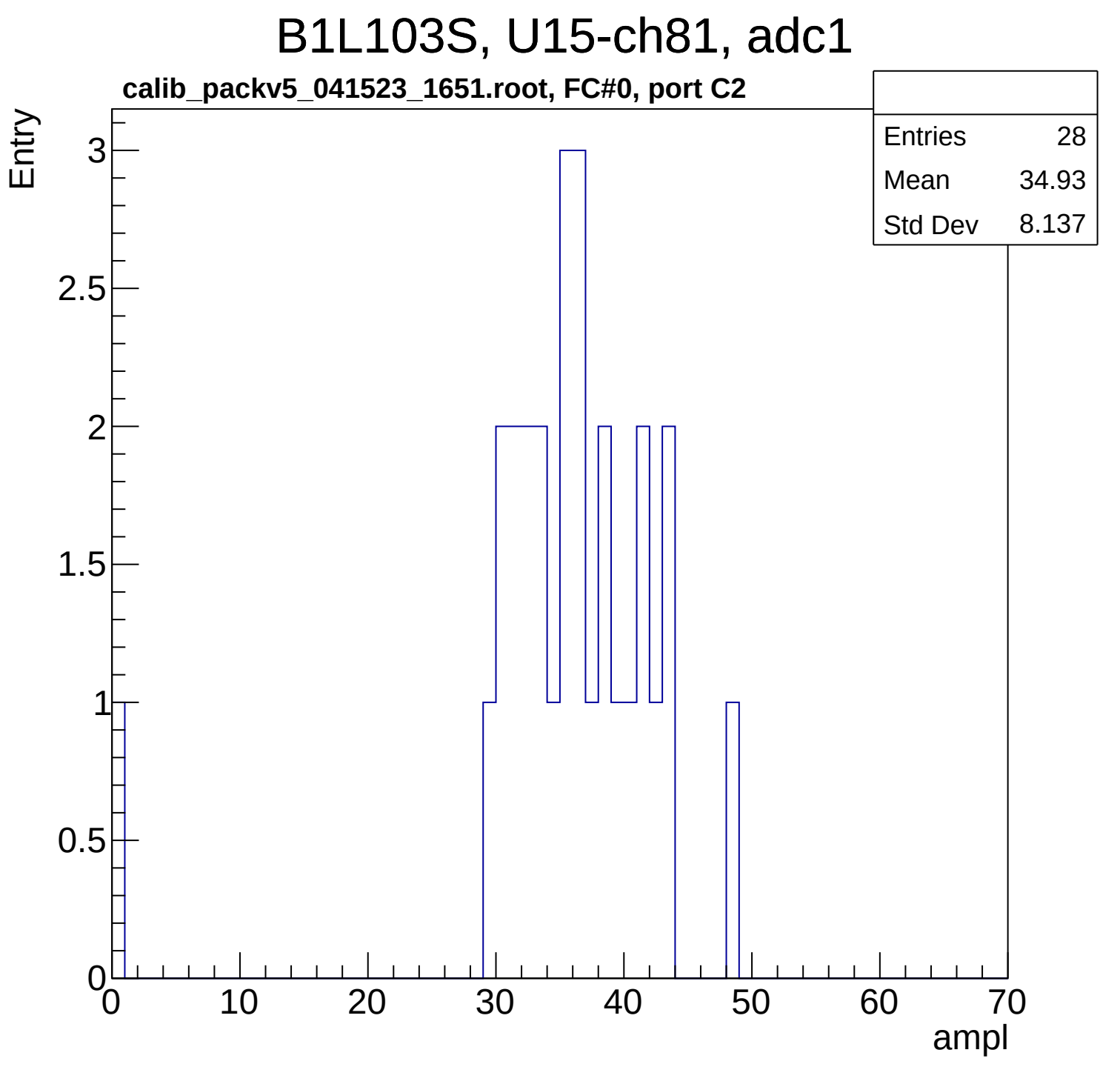
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

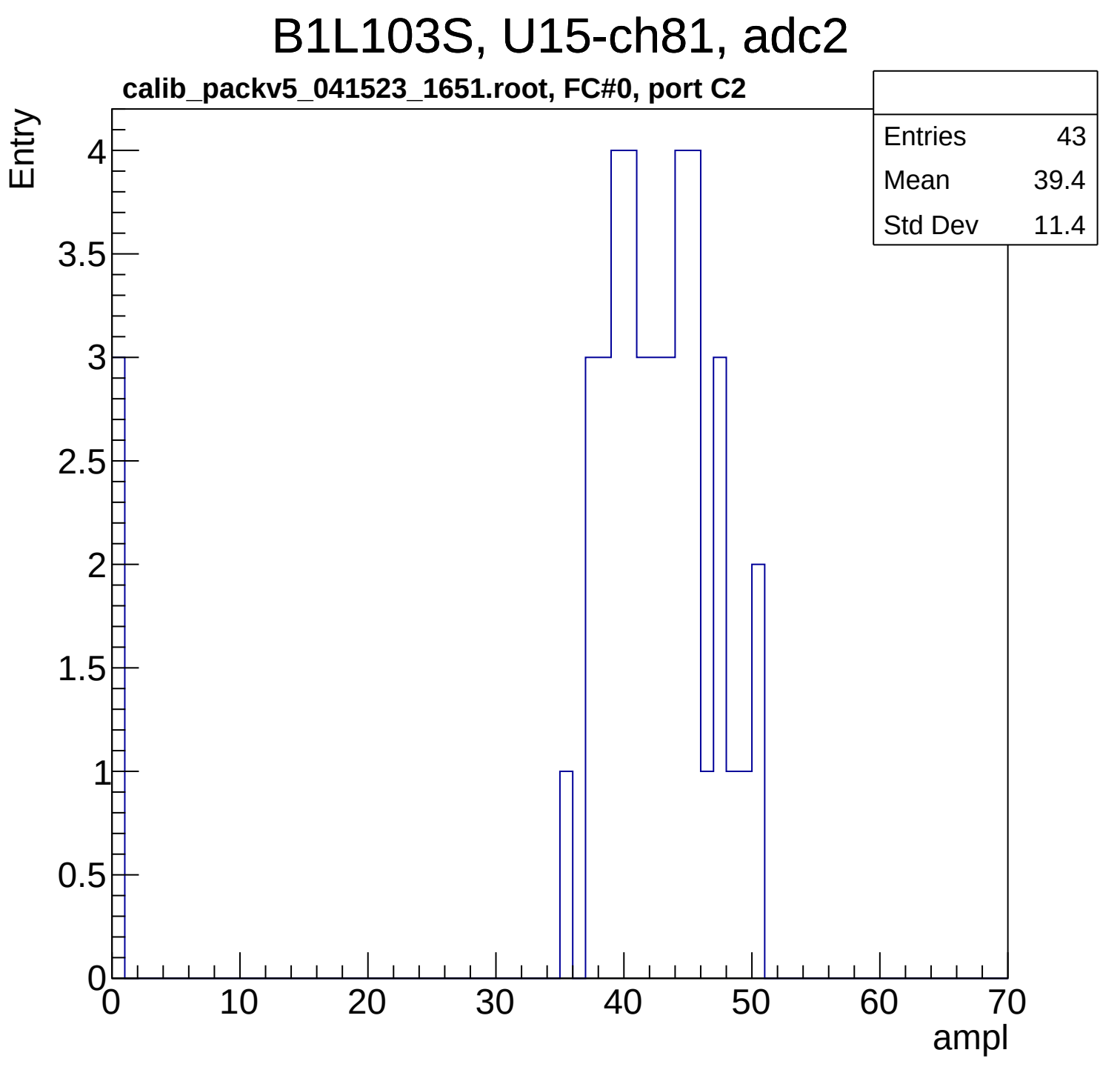

B1L103S, U15-ch80, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 58.22
Std Dev 3.083
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch80, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 56.27
Std Dev 15.21
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch80, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch81, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 25.3
Std Dev 11.63
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U15-ch81, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 34.93
Std Dev 8.137
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch81, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 39.4
Std Dev 11.4
Entry
ampl
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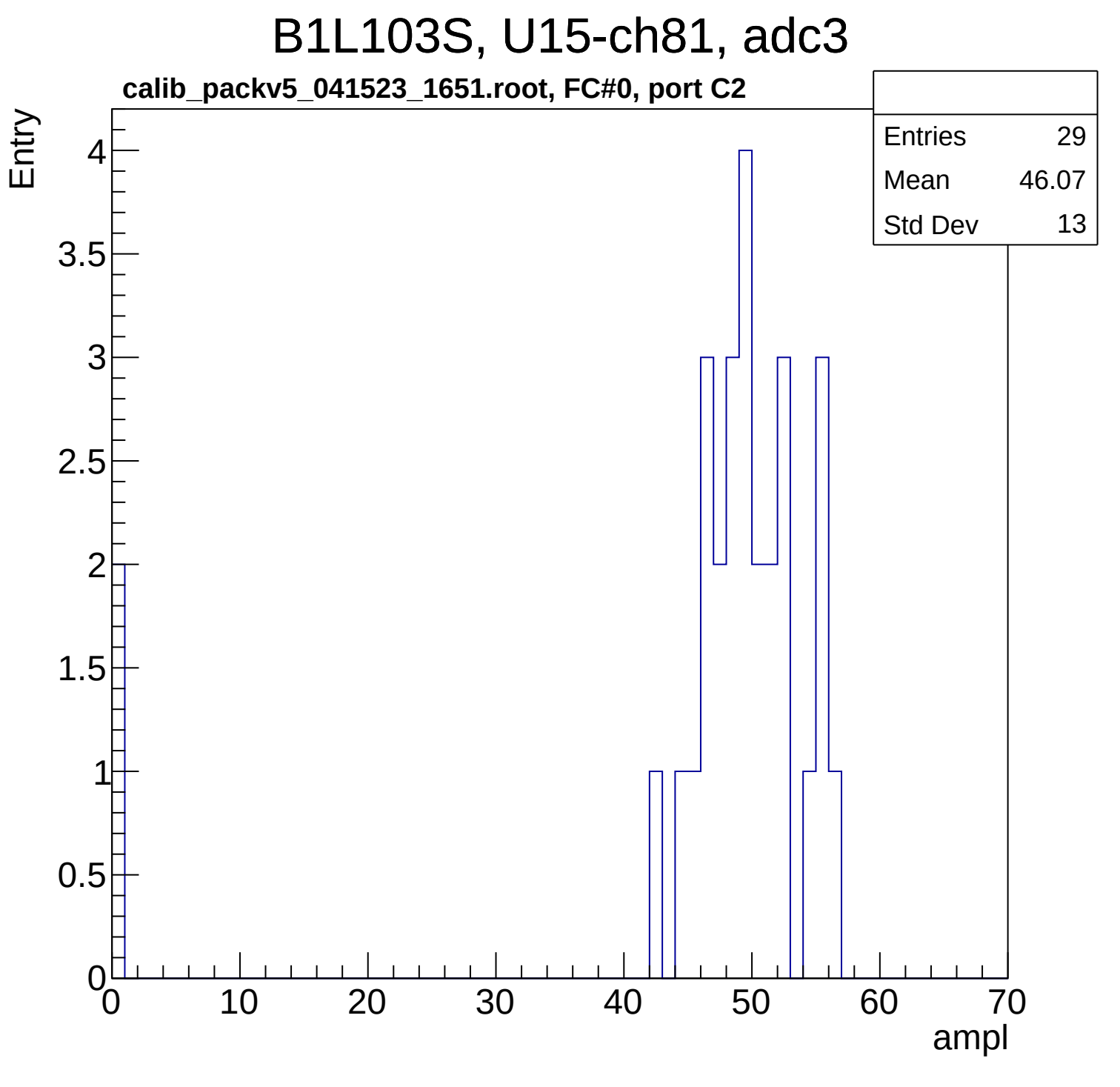
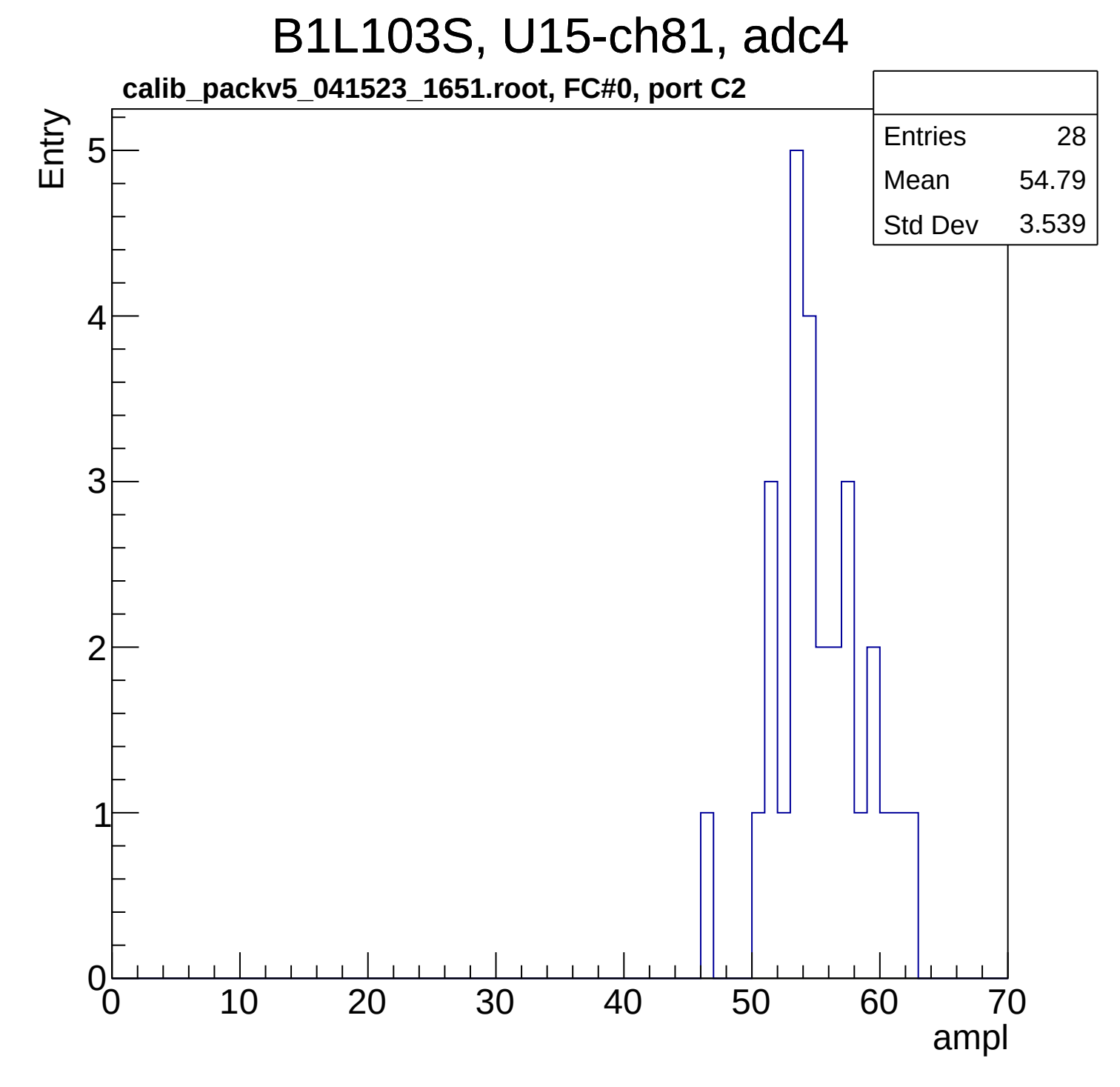
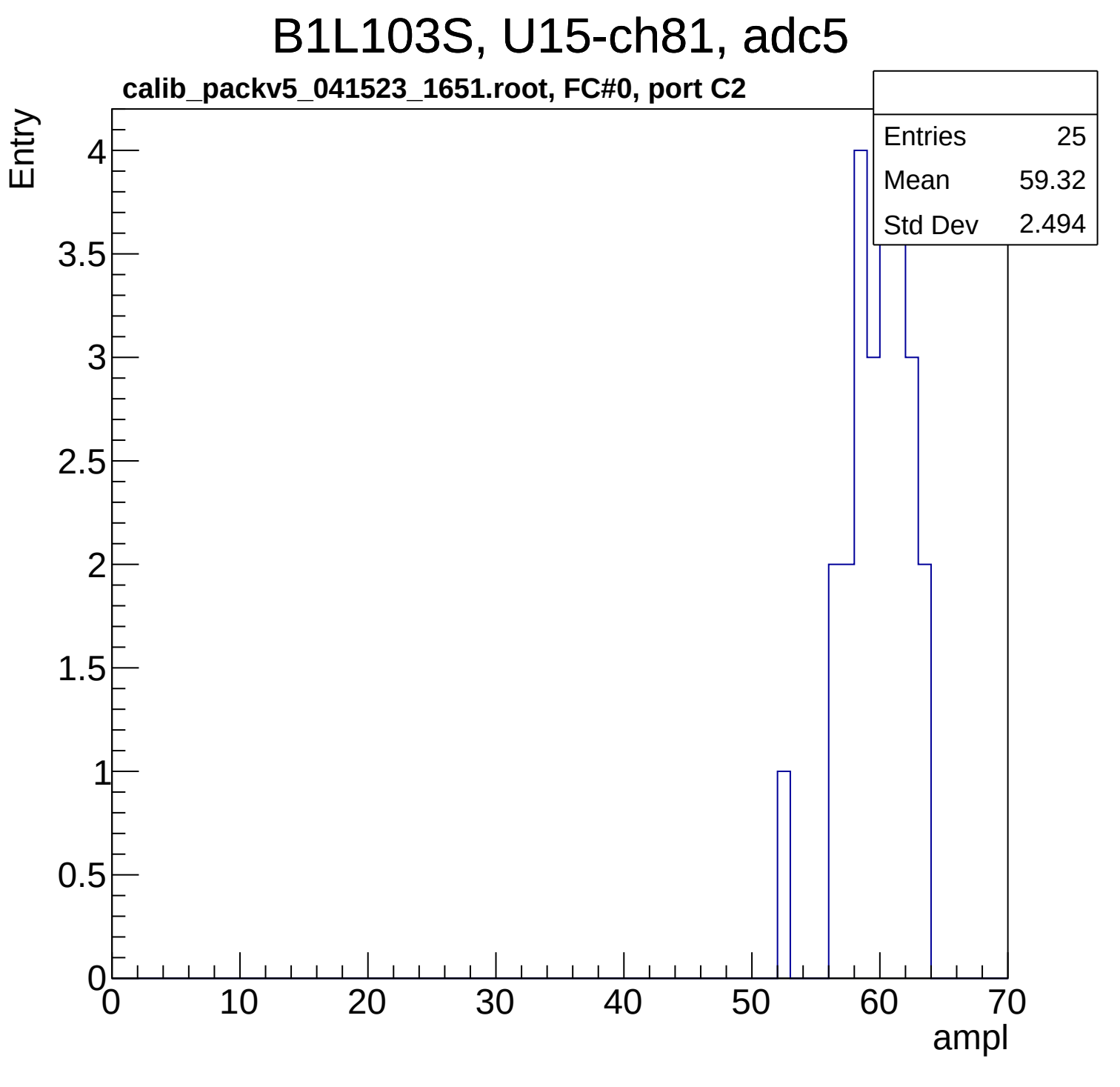
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch81, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 46.07
Std Dev 13
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch81, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 54.79
Std Dev 3.539
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch81, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 59.32
Std Dev 2.494
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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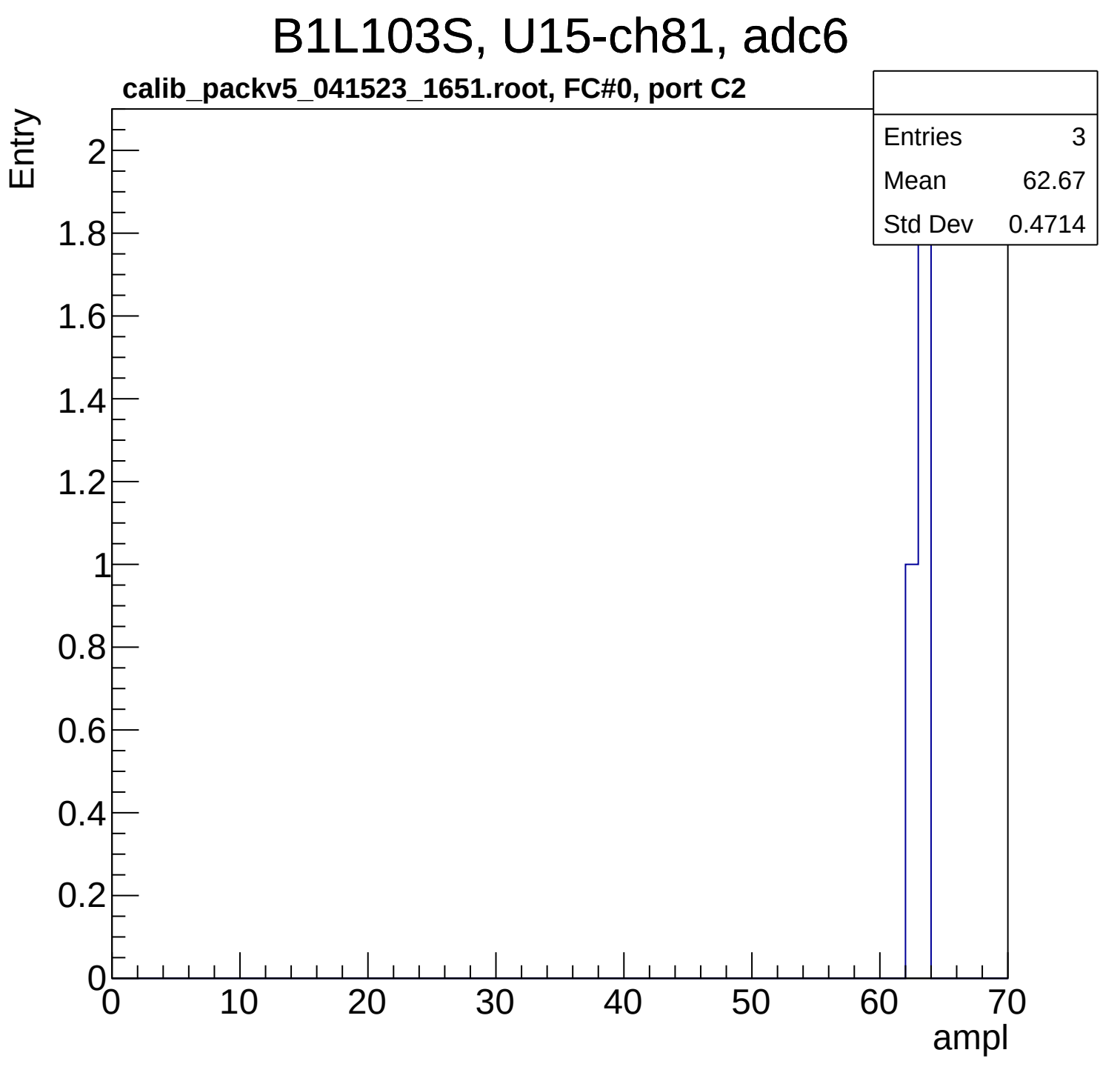
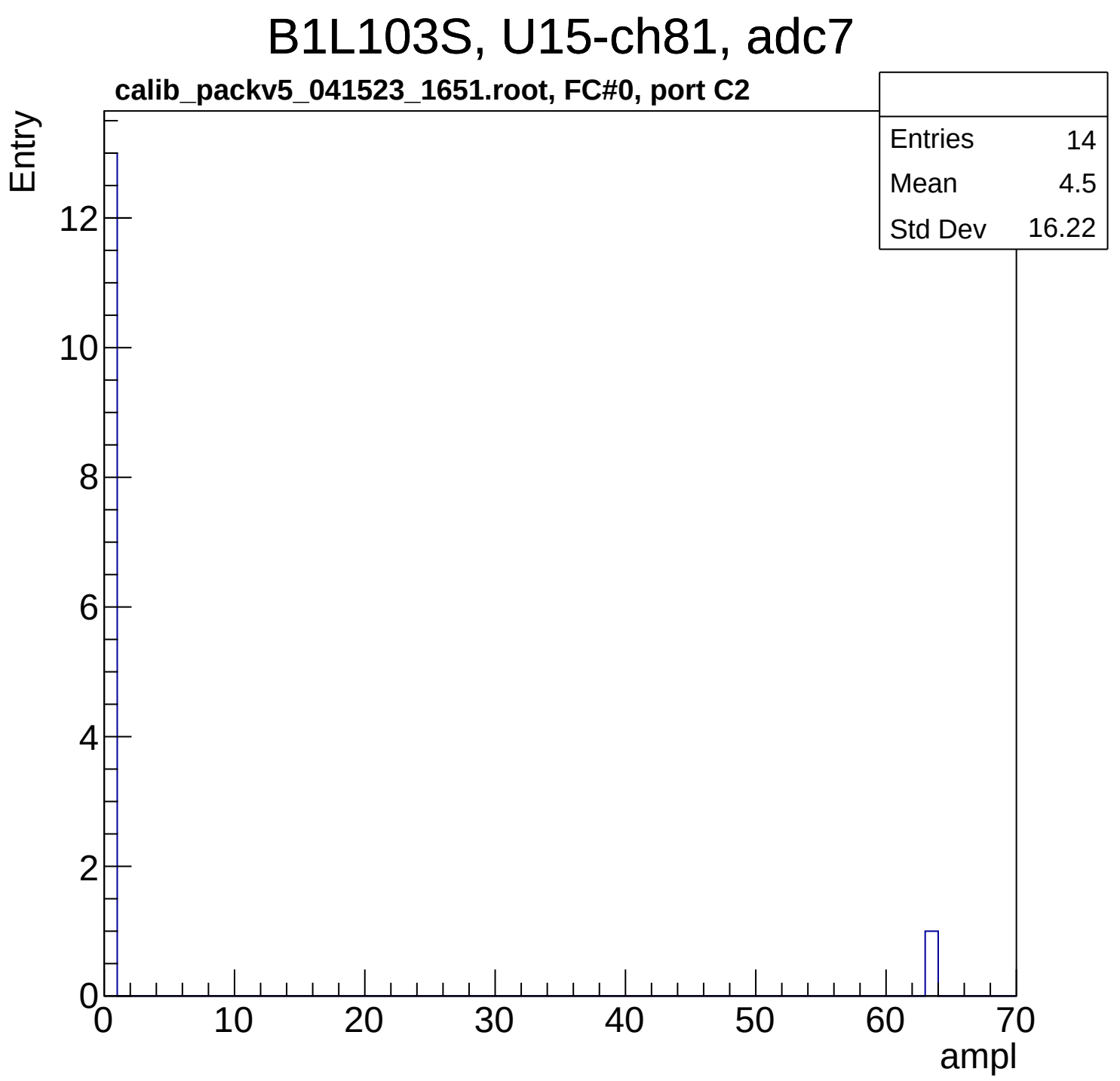
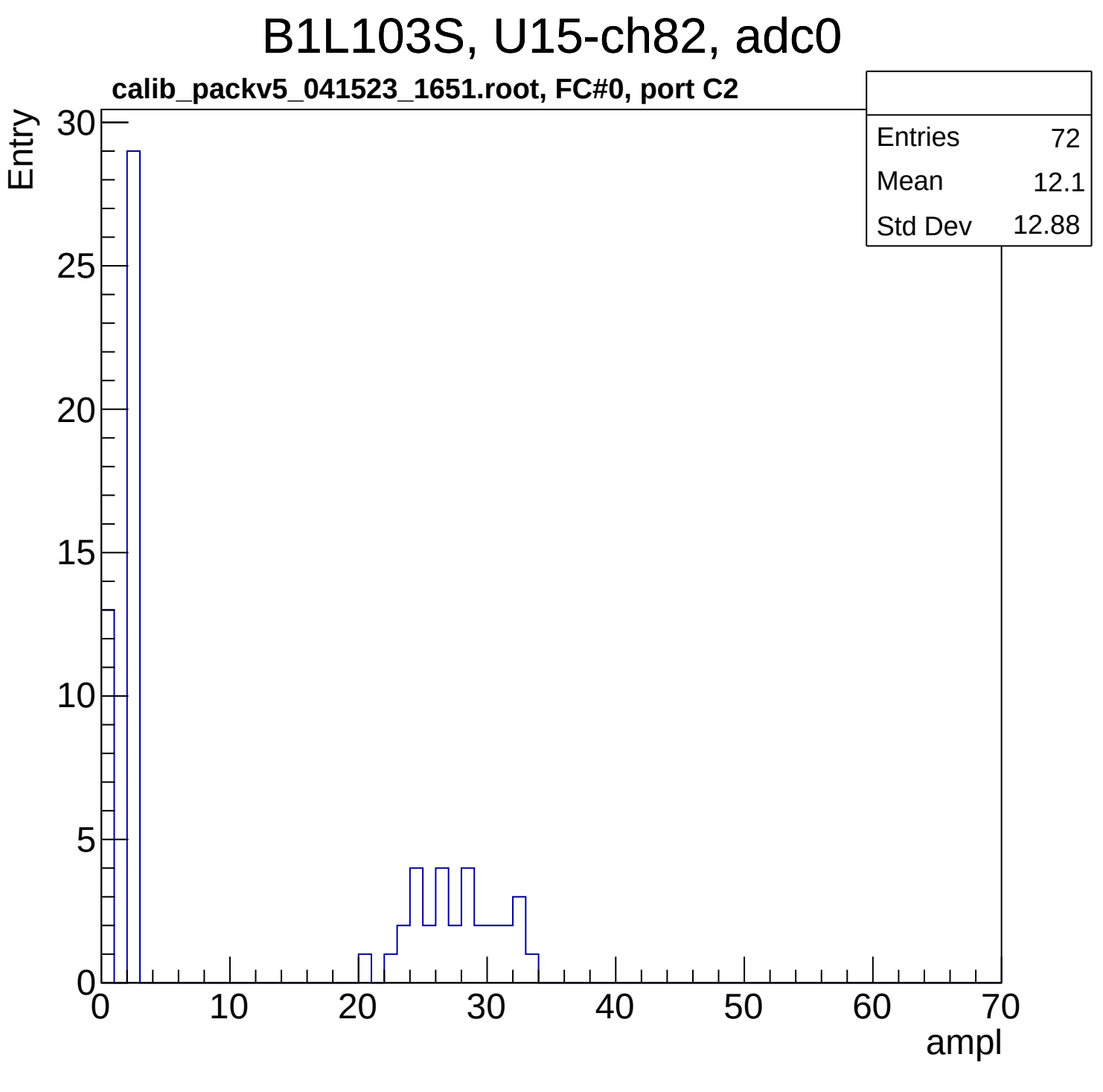
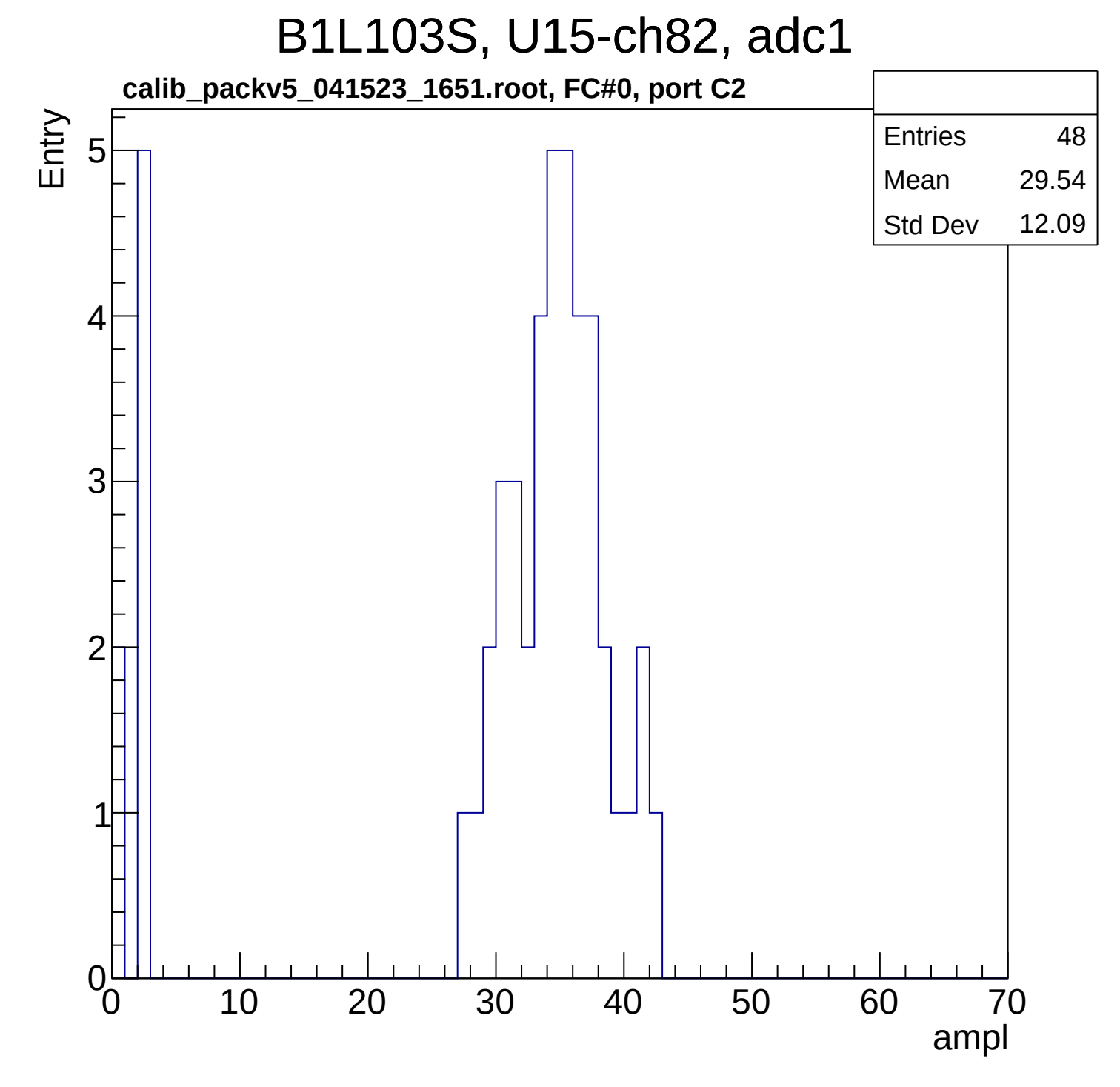
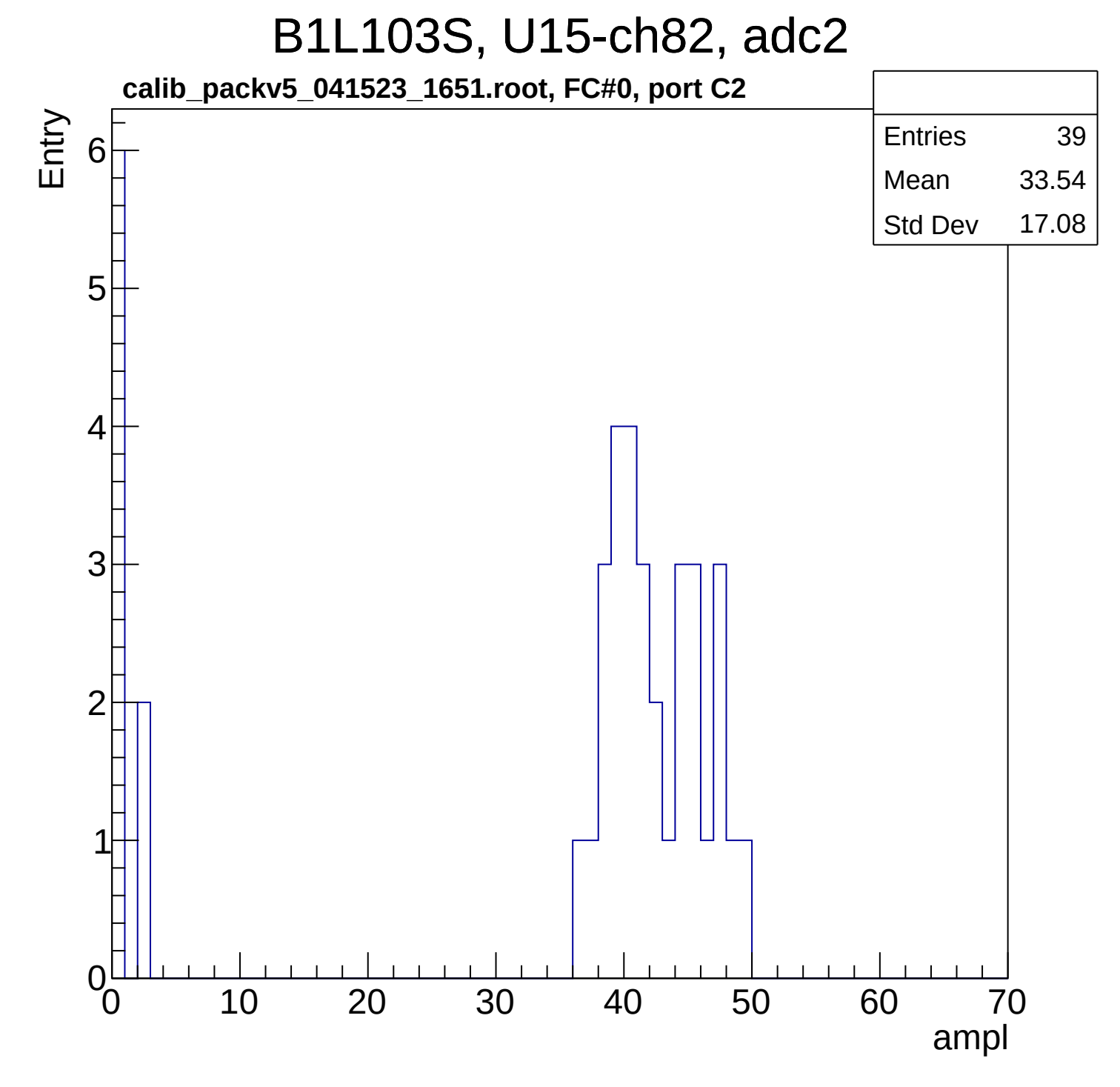
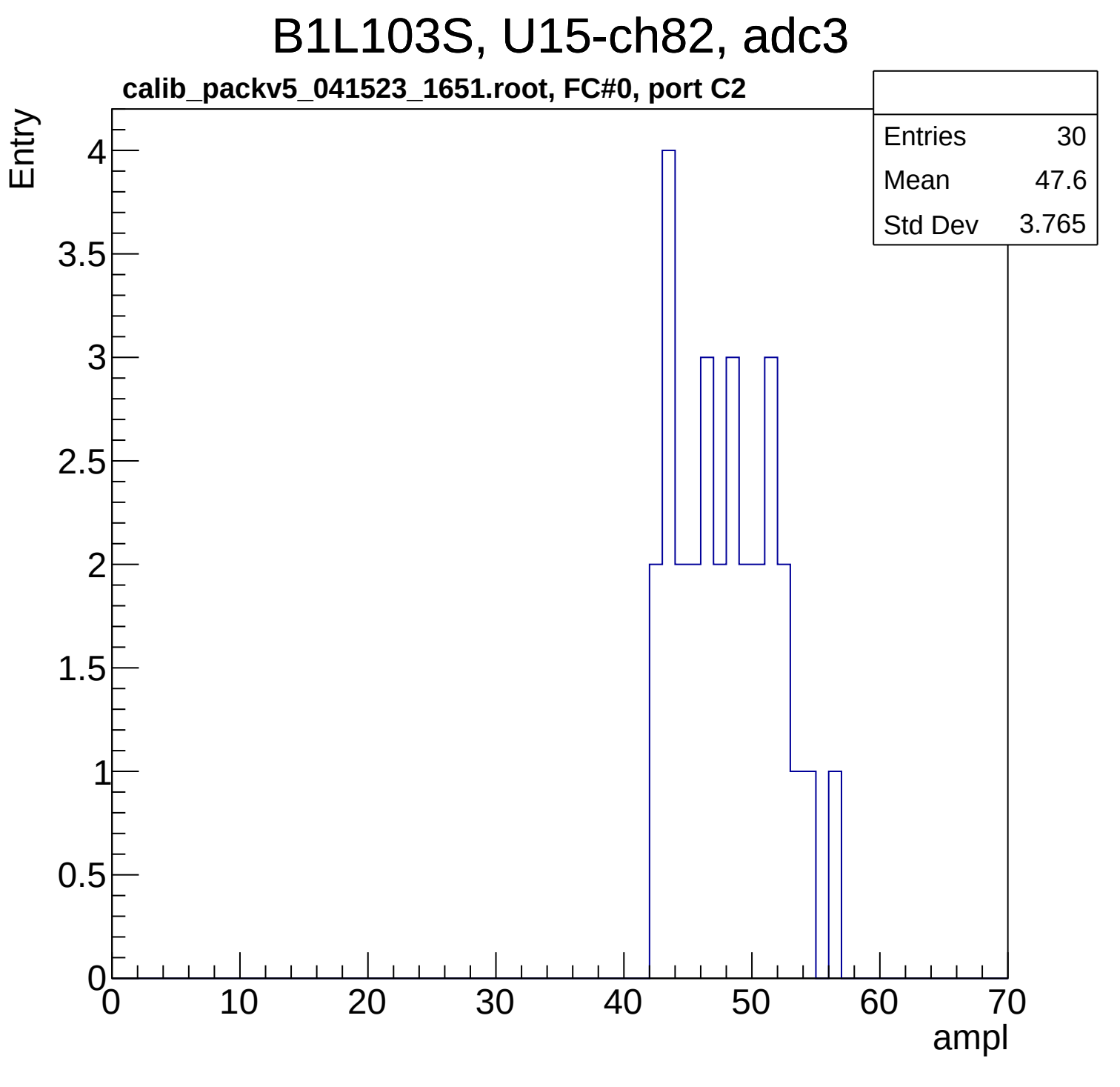

B1L103S, U15-ch81, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U15-ch81, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 4.5
Std Dev 16.22
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch82, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 12.1
Std Dev 12.88
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch82, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 29.54
Std Dev 12.09
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch82, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 33.54
Std Dev 17.08
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch82, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 47.6
Std Dev 3.765
Entry
ampl
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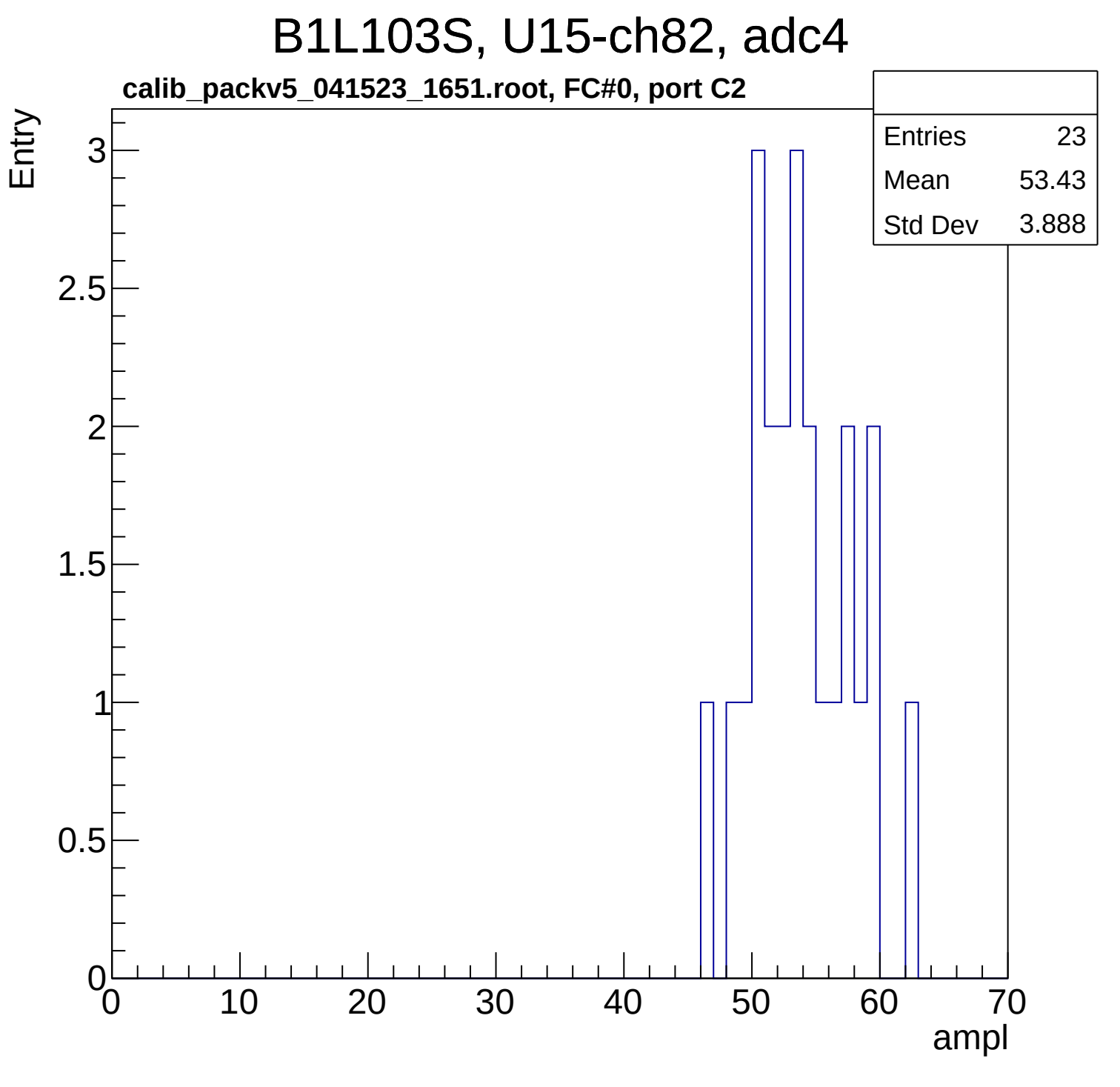
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch82, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 53.43
Std Dev 3.888
Entry
ampl
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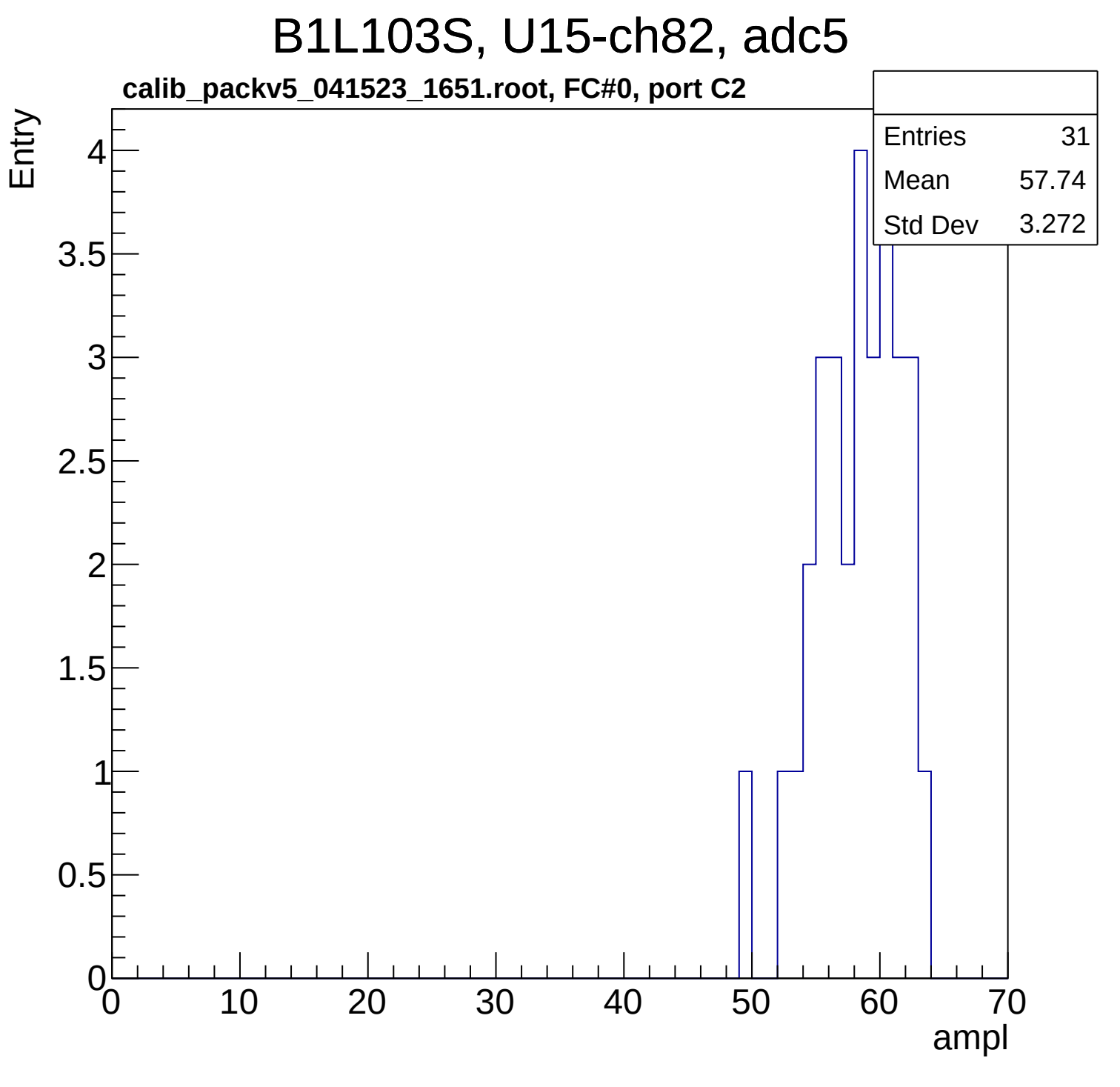
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch82, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 57.74
Std Dev 3.272
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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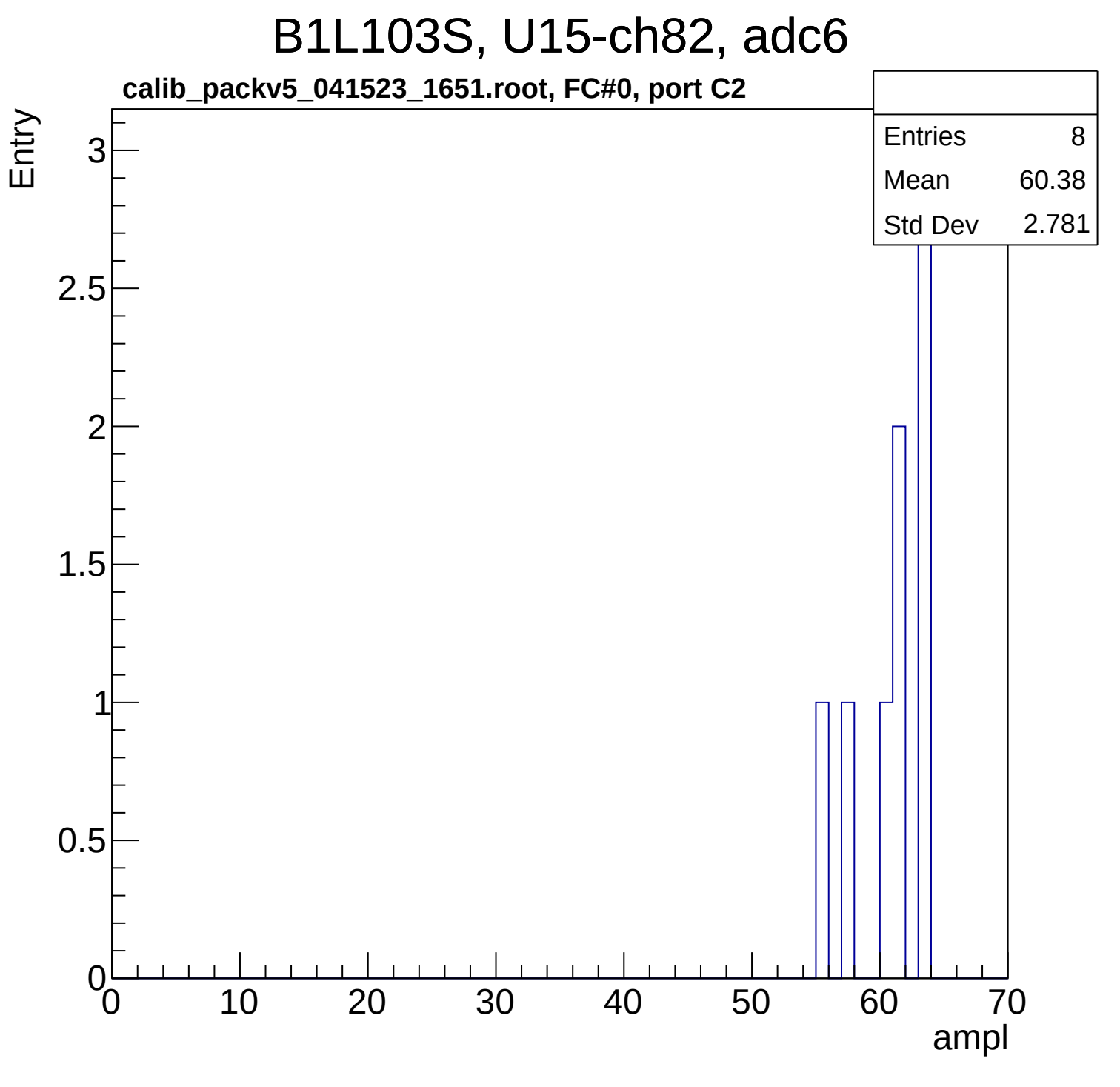
40
50
60
70


B1L103S, U15-ch82, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 60.38
Std Dev 2.781
Entry
ampl
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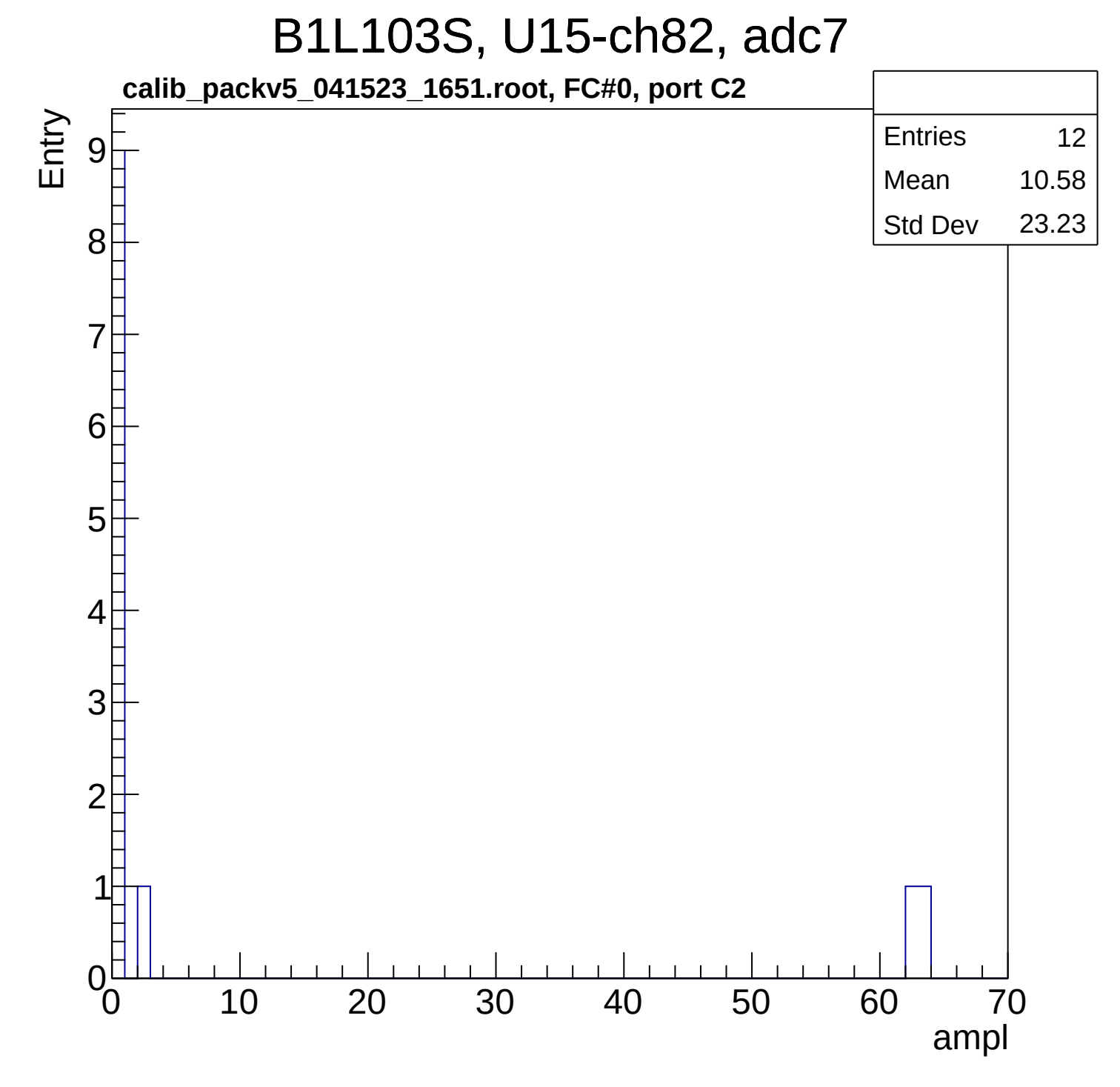
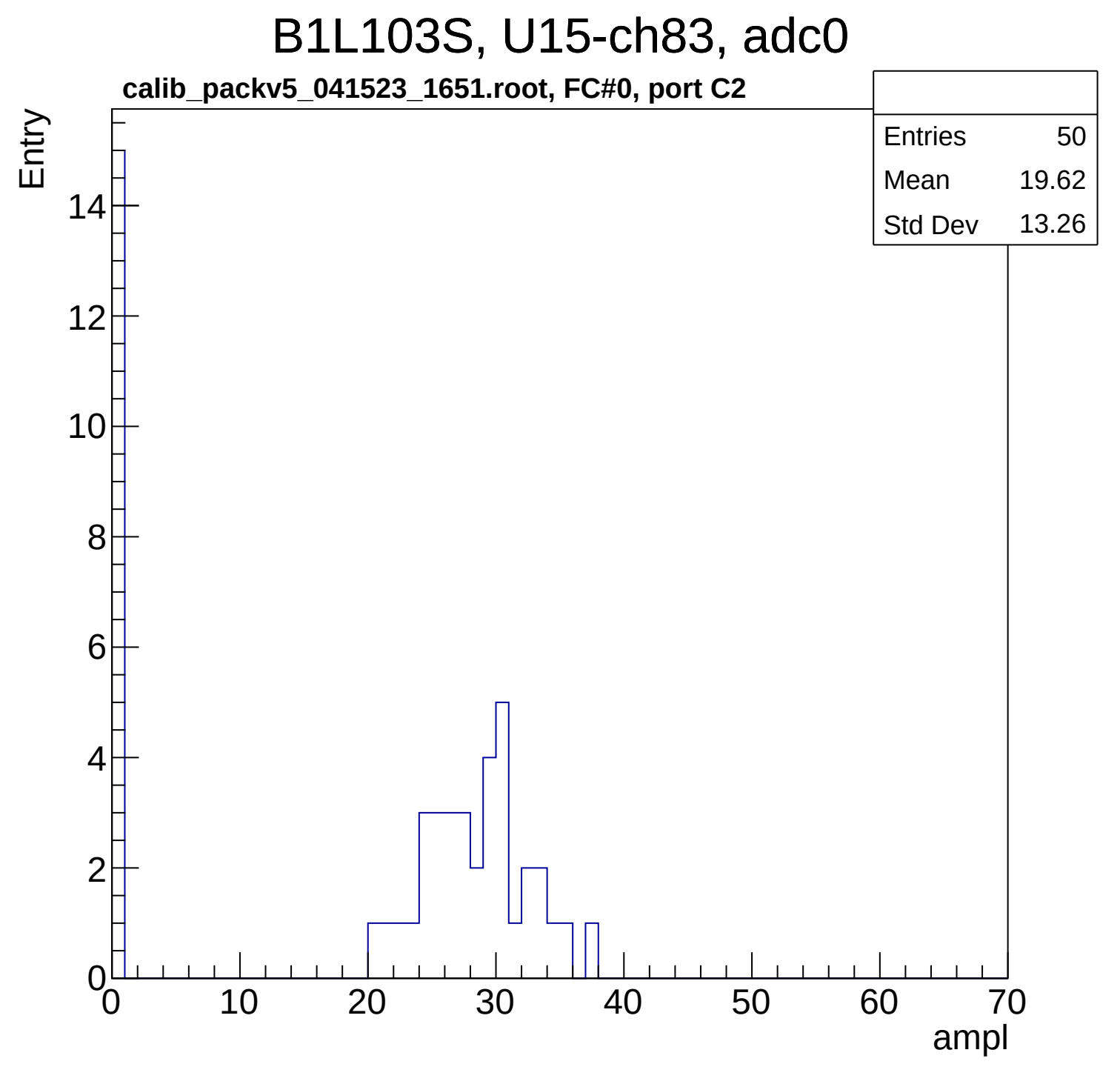
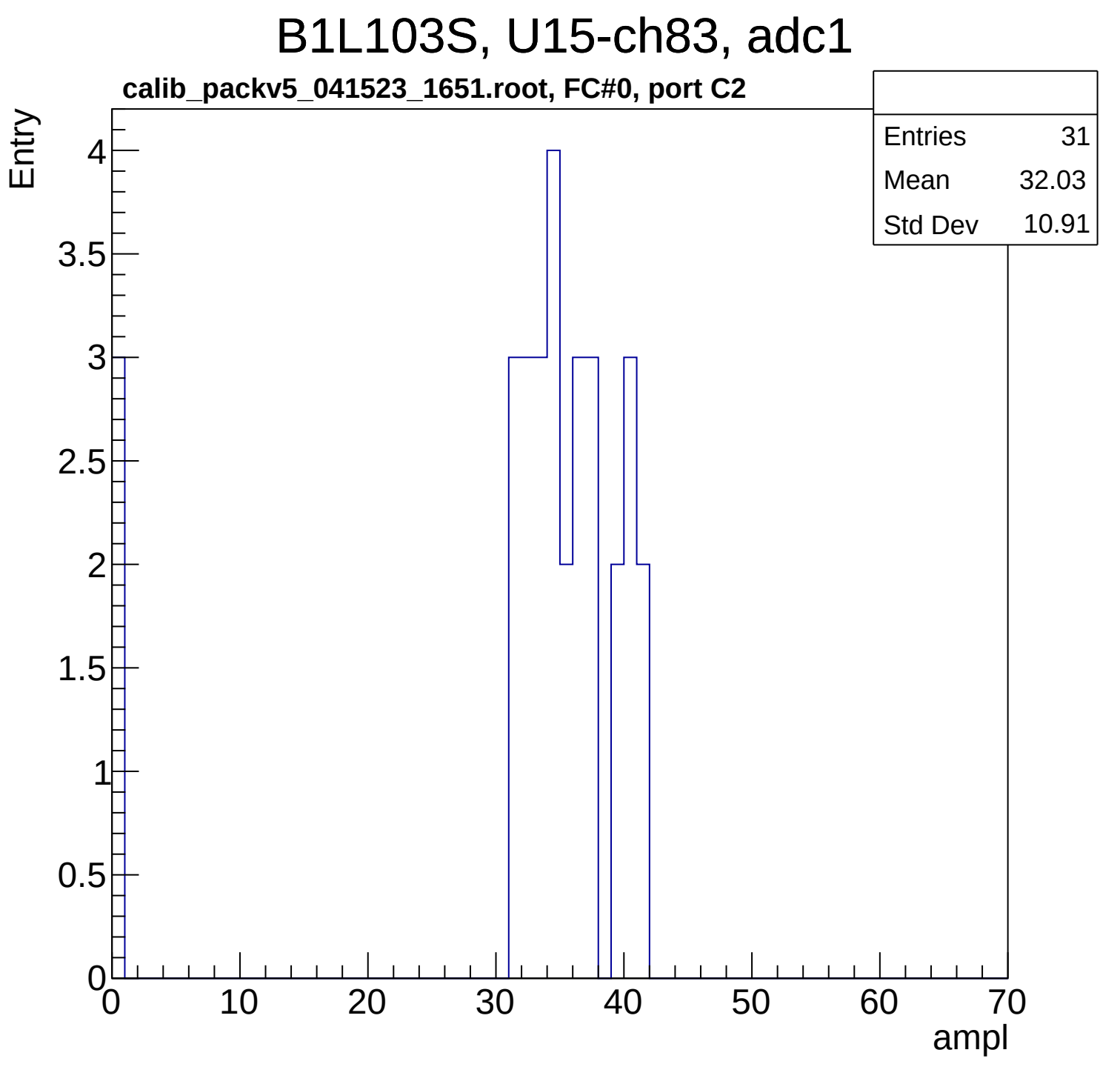
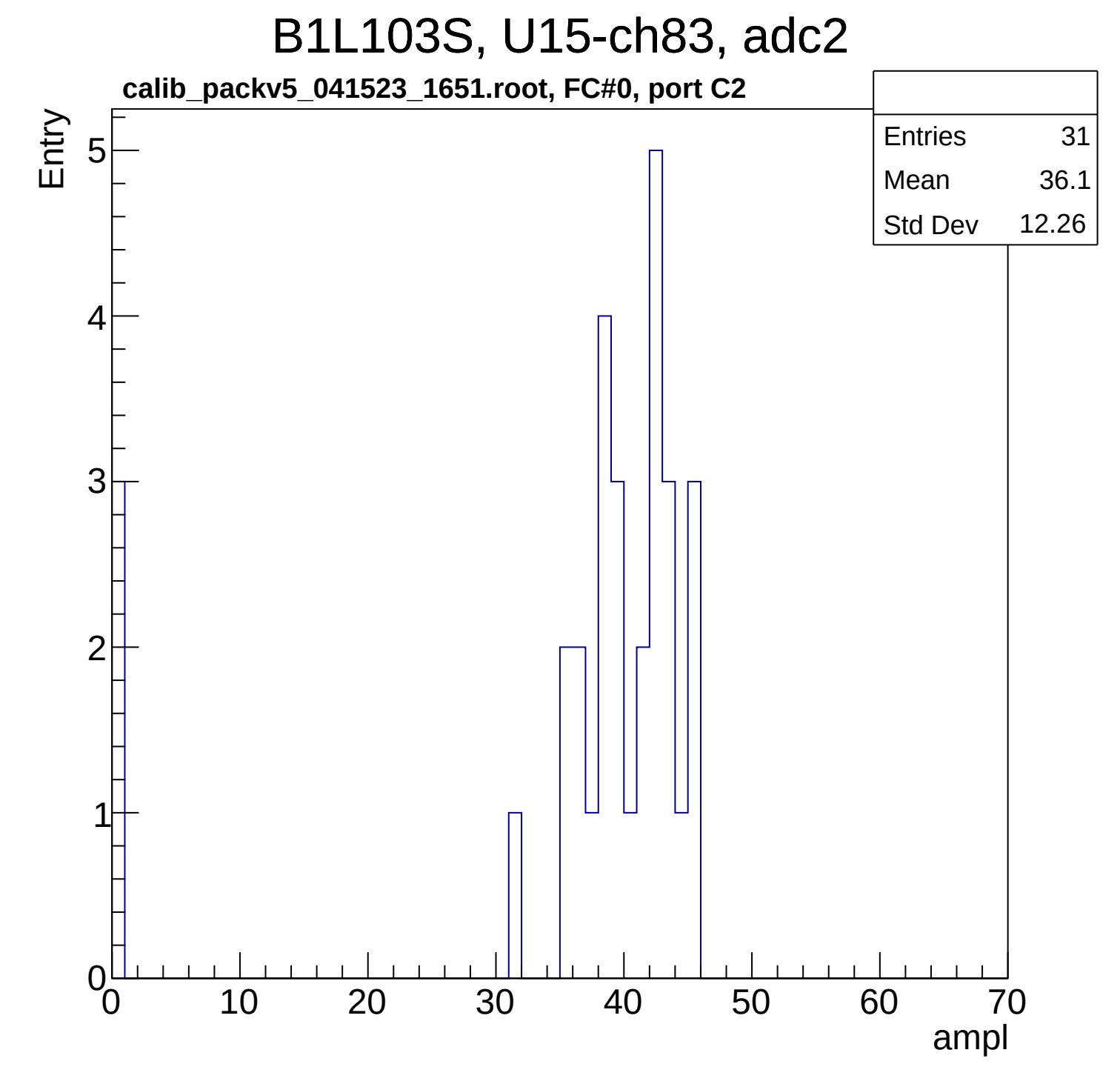
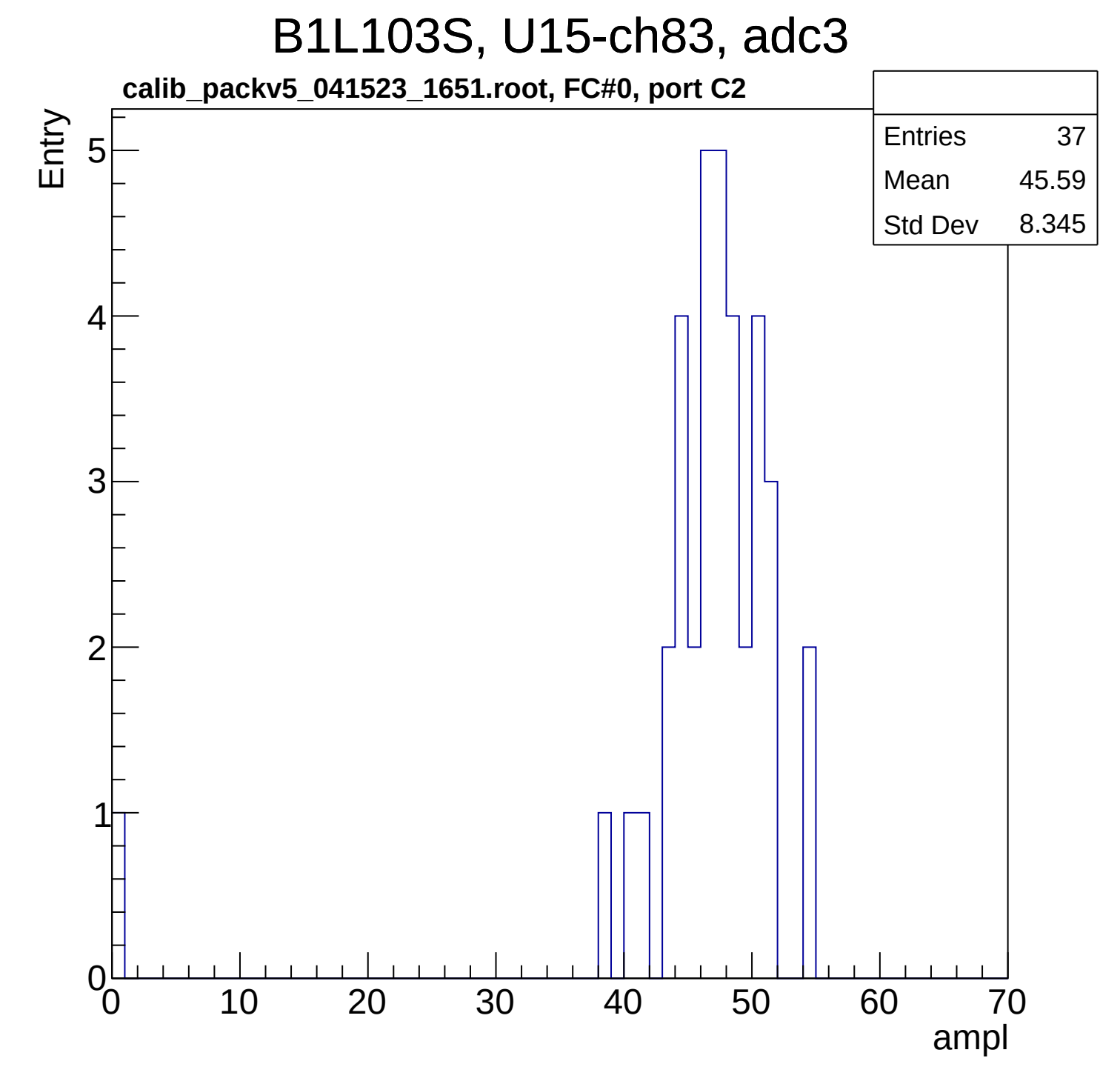
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

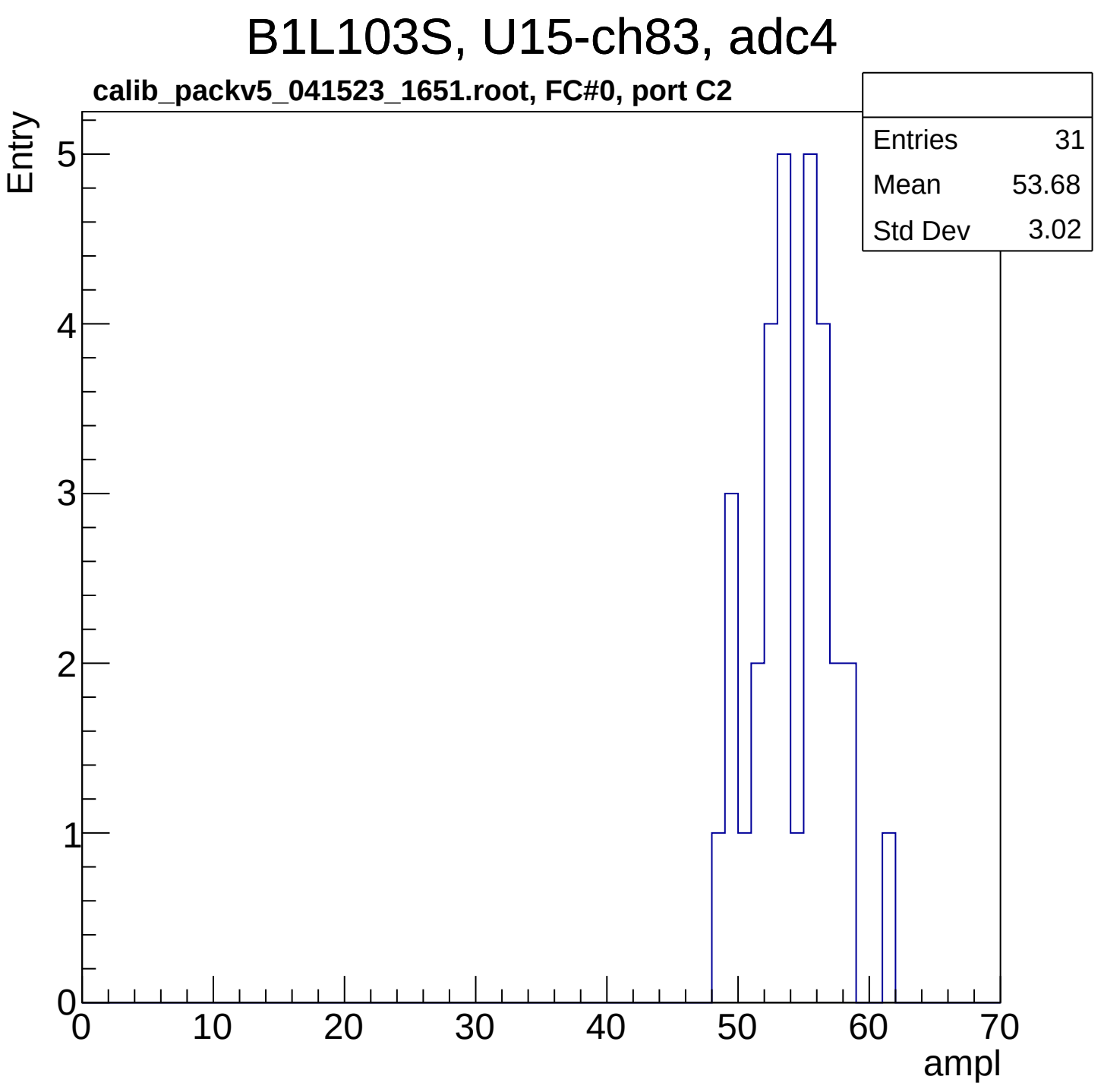

B1L103S, U15-ch82, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 10.58
Std Dev 23.23
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

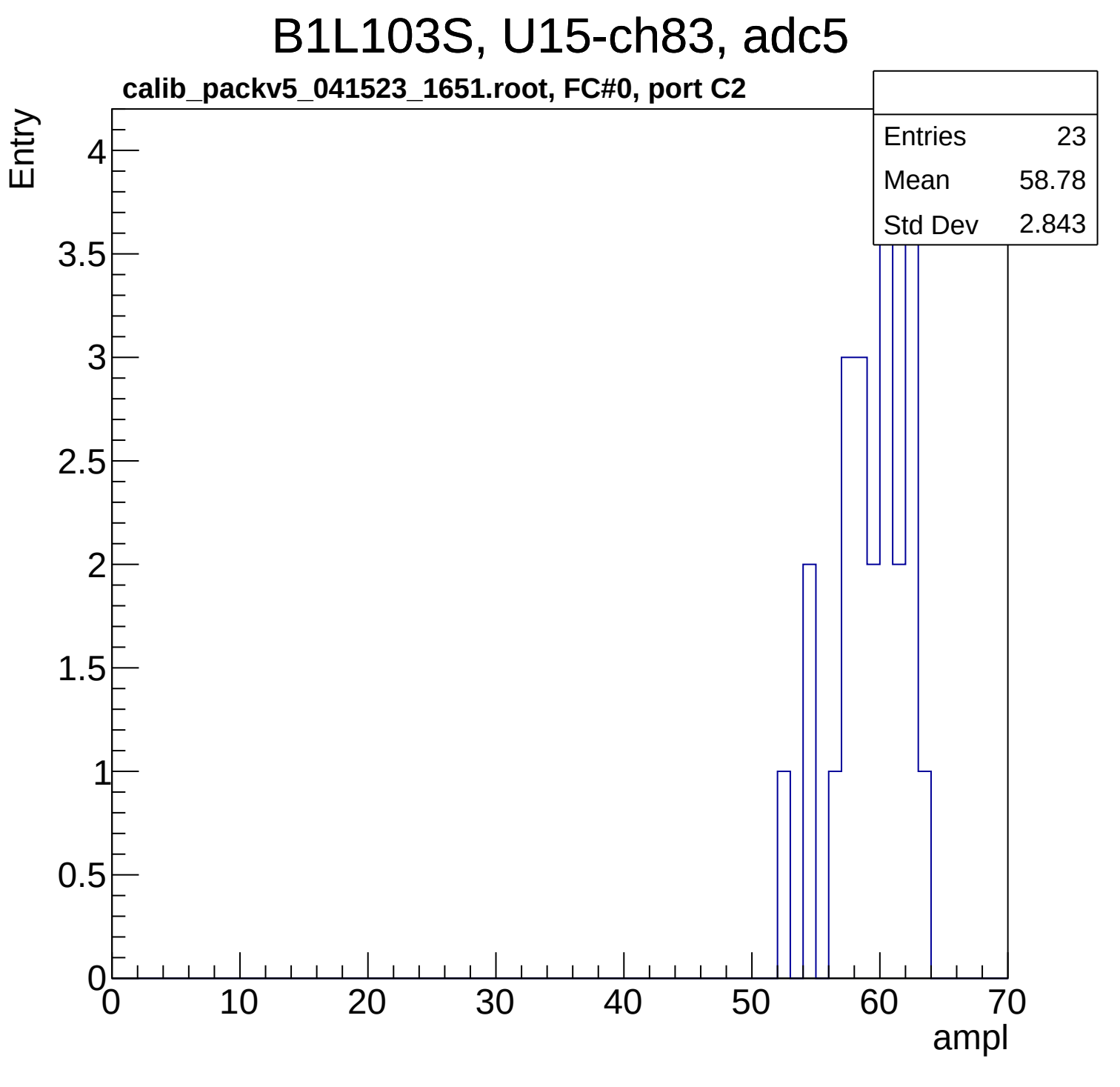

B1L103S, U15-ch83, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 19.62
Std Dev 13.26
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

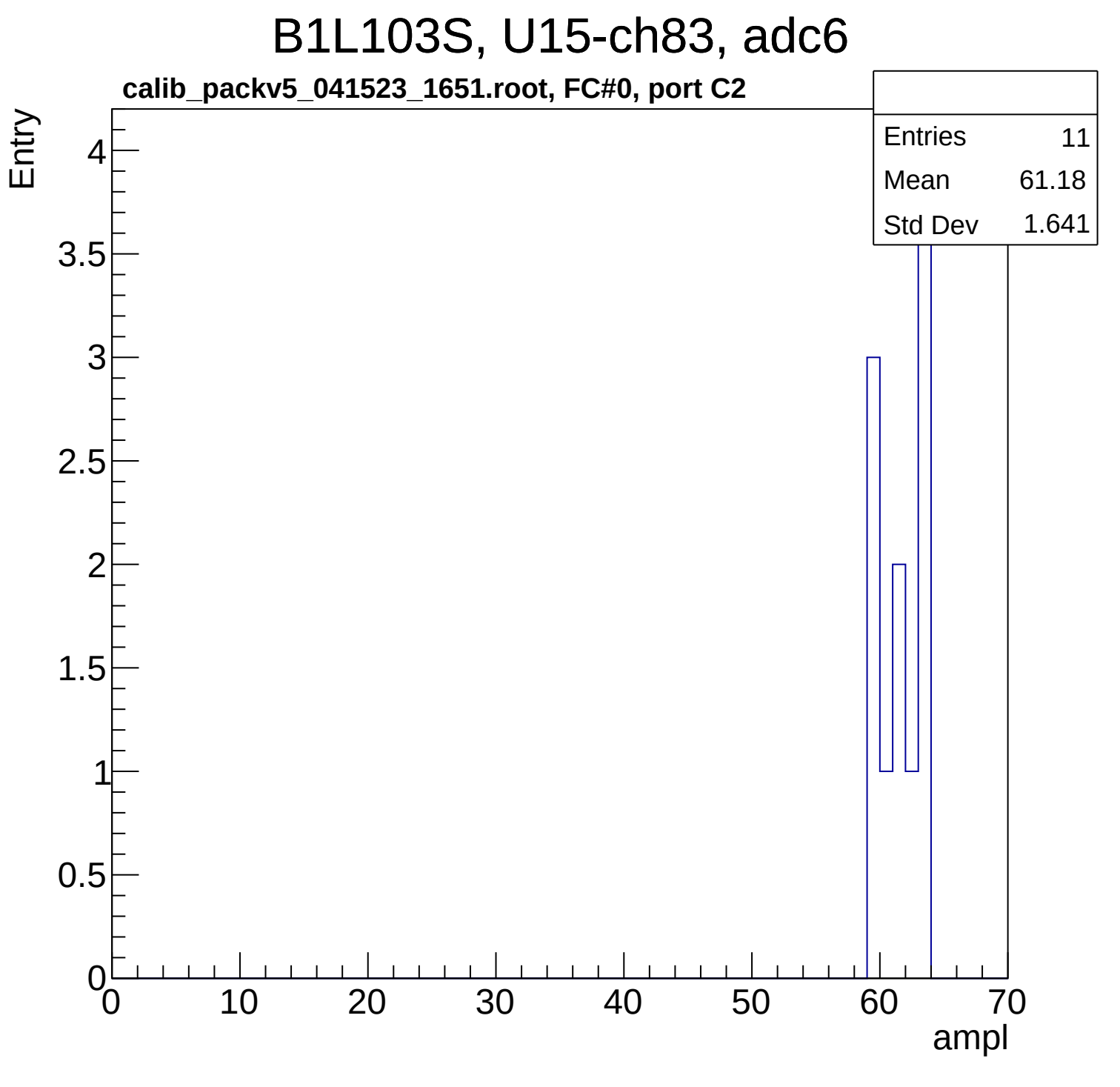

B1L103S, U15-ch83, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 32.03
Std Dev 10.91
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

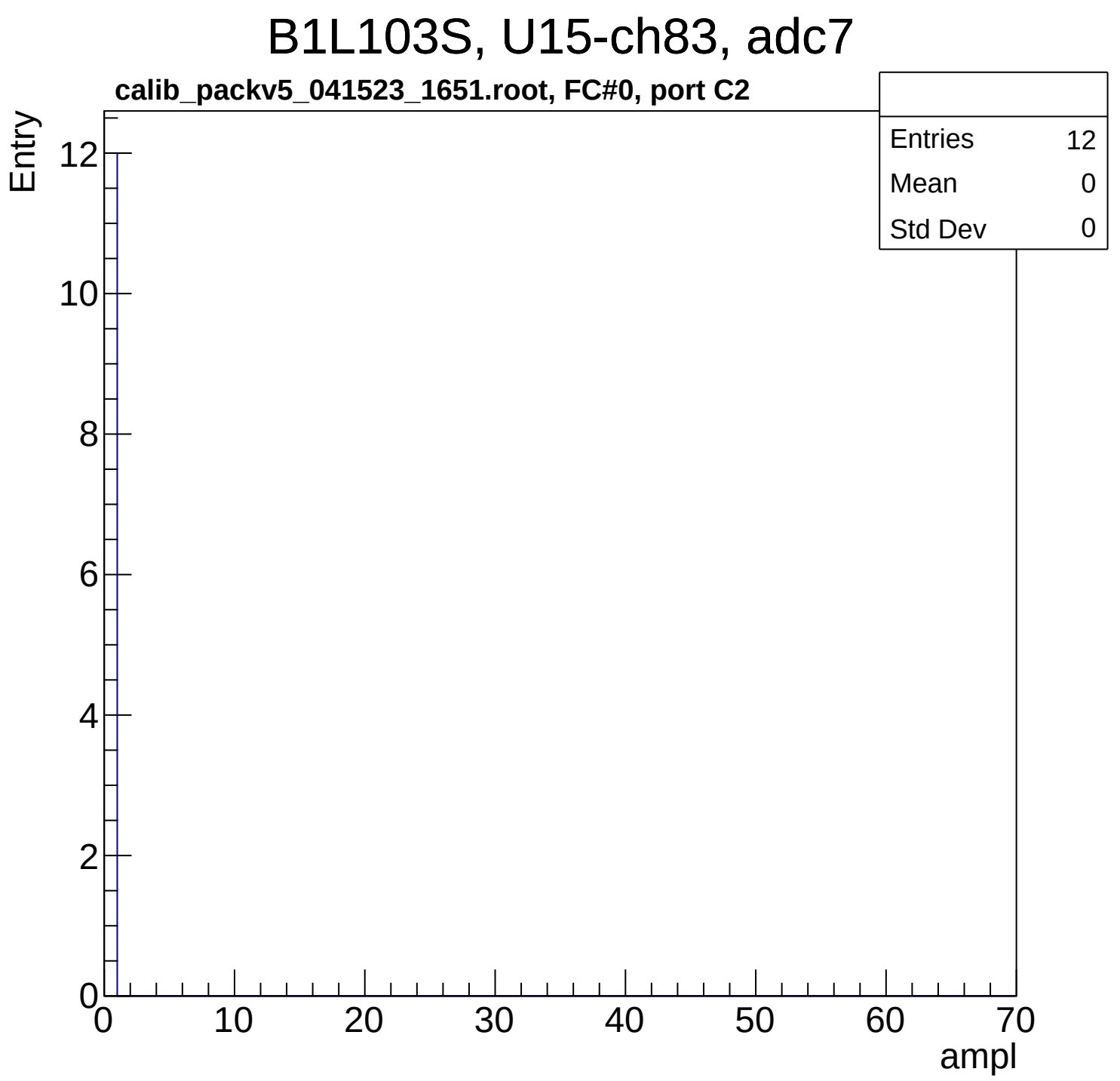

B1L103S, U15-ch83, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 36.1
Std Dev 12.26
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

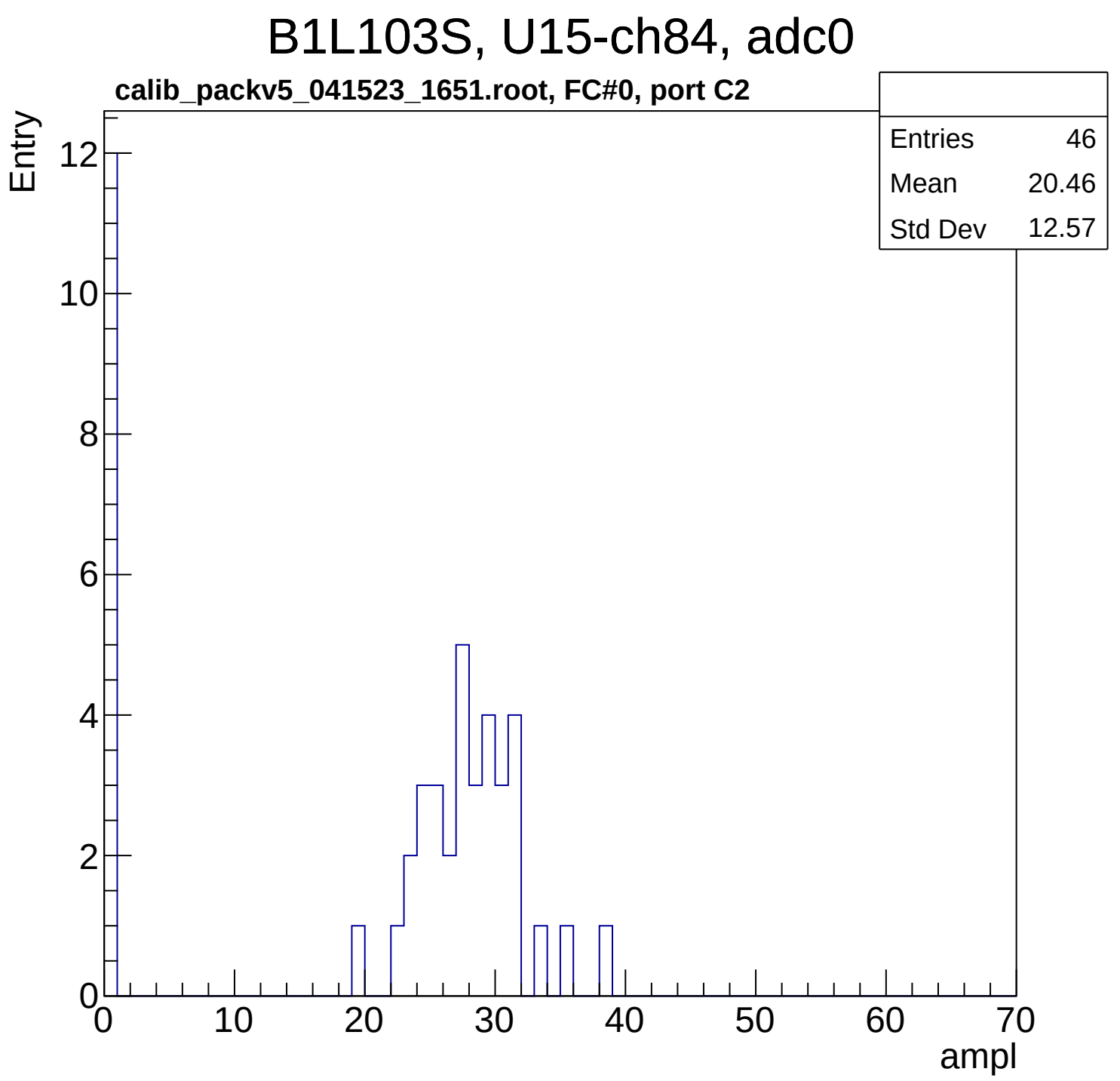

B1L103S, U15-ch83, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 45.59
Std Dev 8.345
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

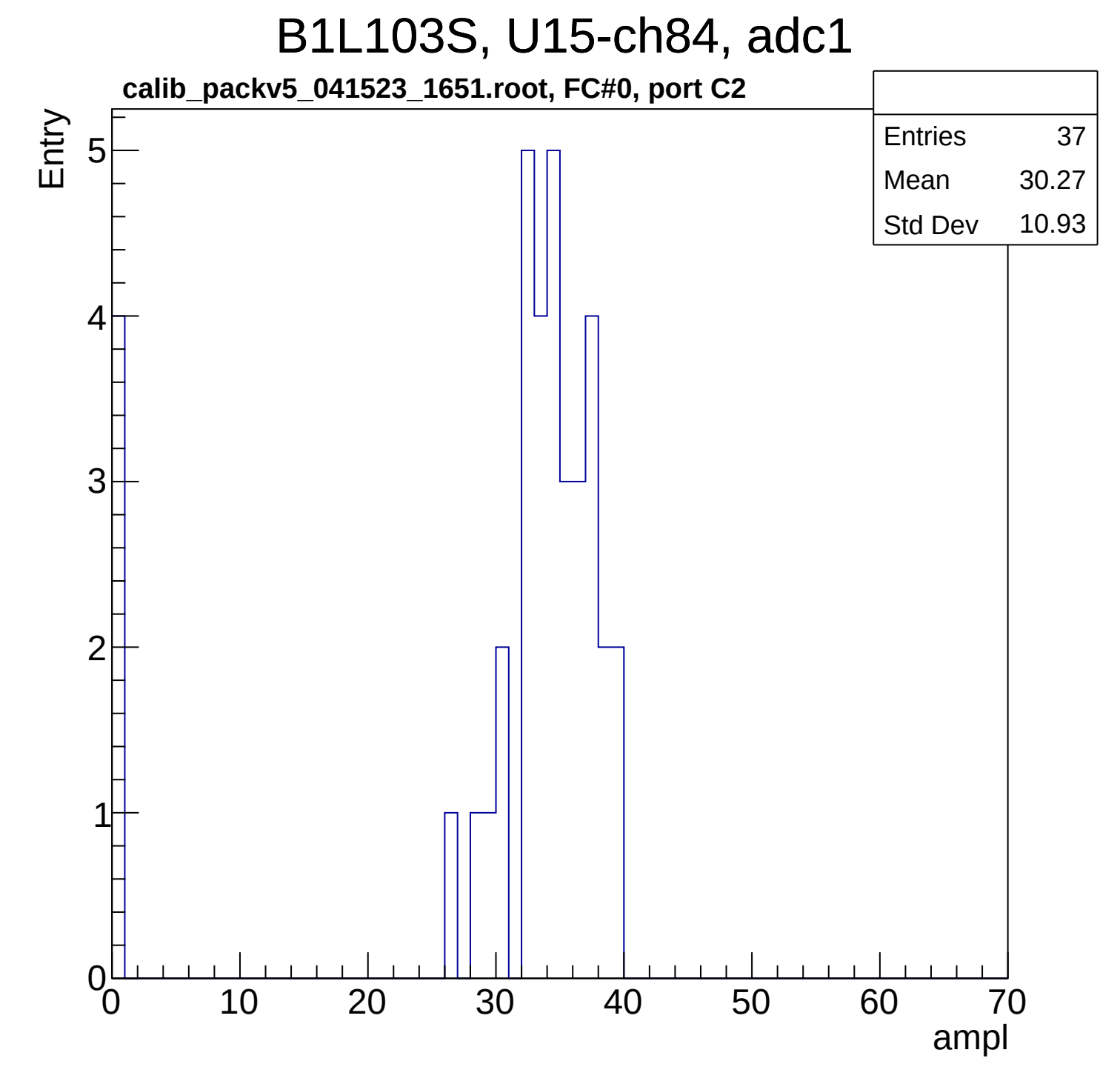

B1L103S, U15-ch83, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 53.68
Std Dev 3.02
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

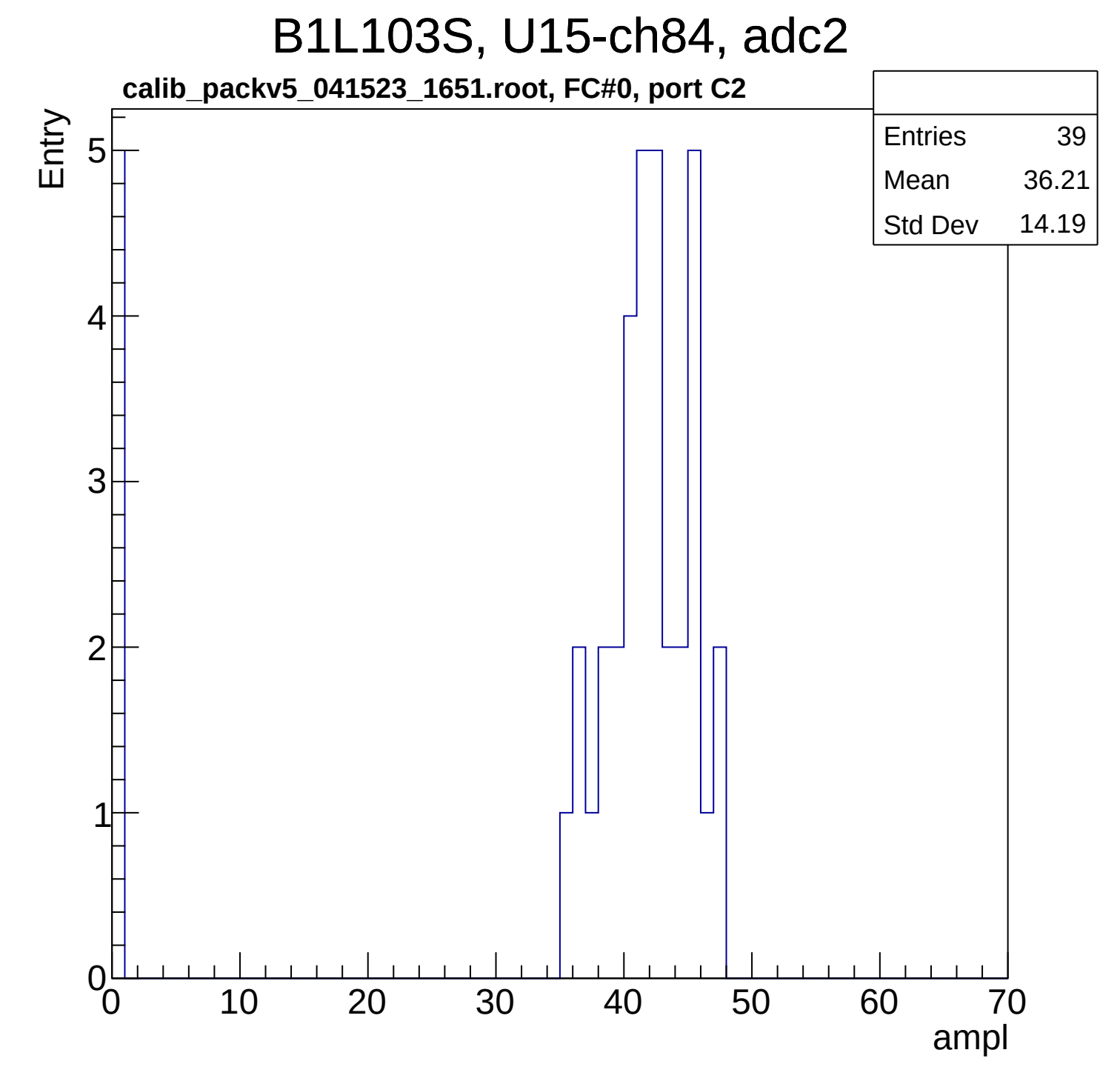

B1L103S, U15-ch83, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 58.78
Std Dev 2.843
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

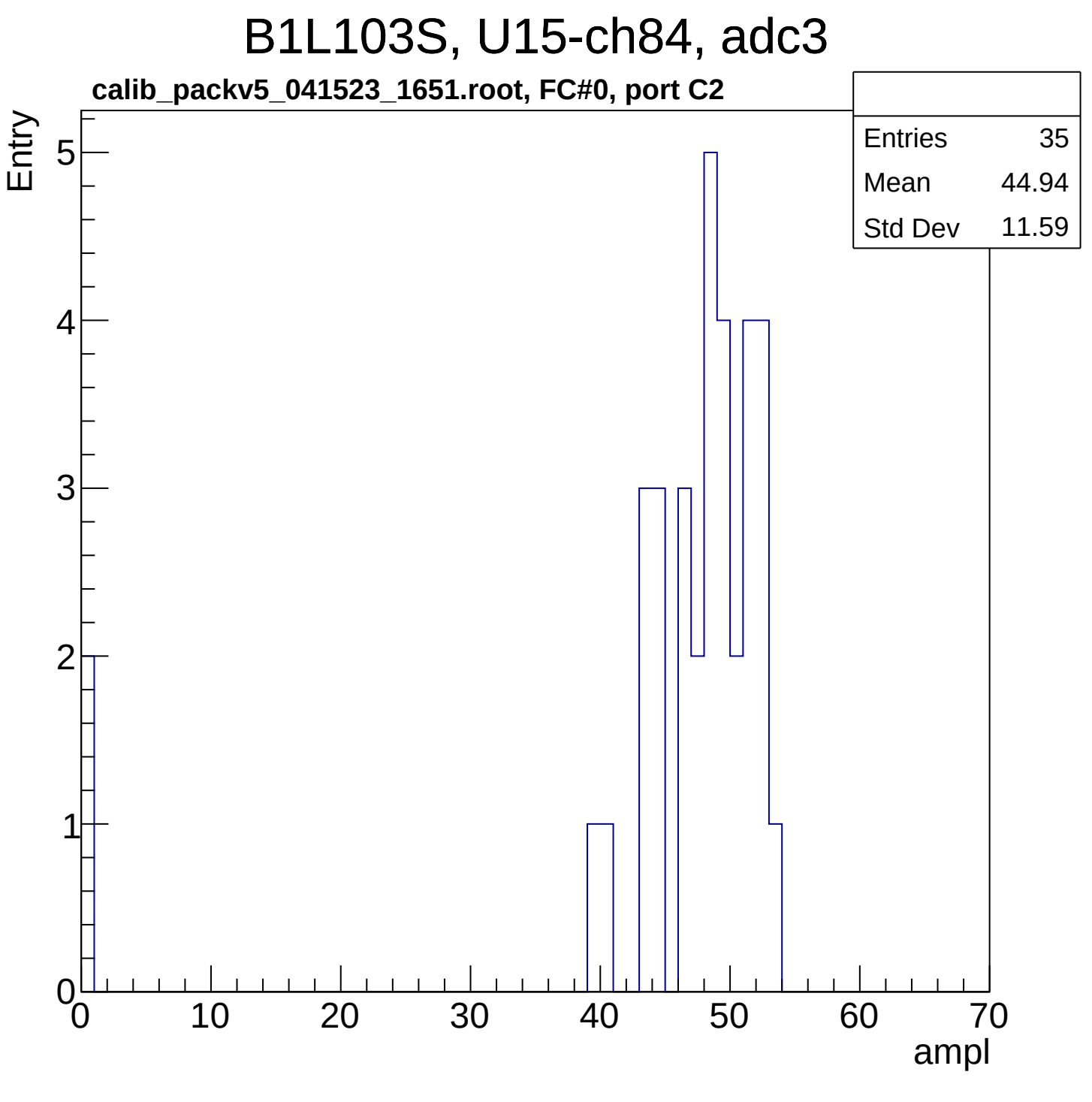

B1L103S, U15-ch83, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.18
Std Dev 1.641
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

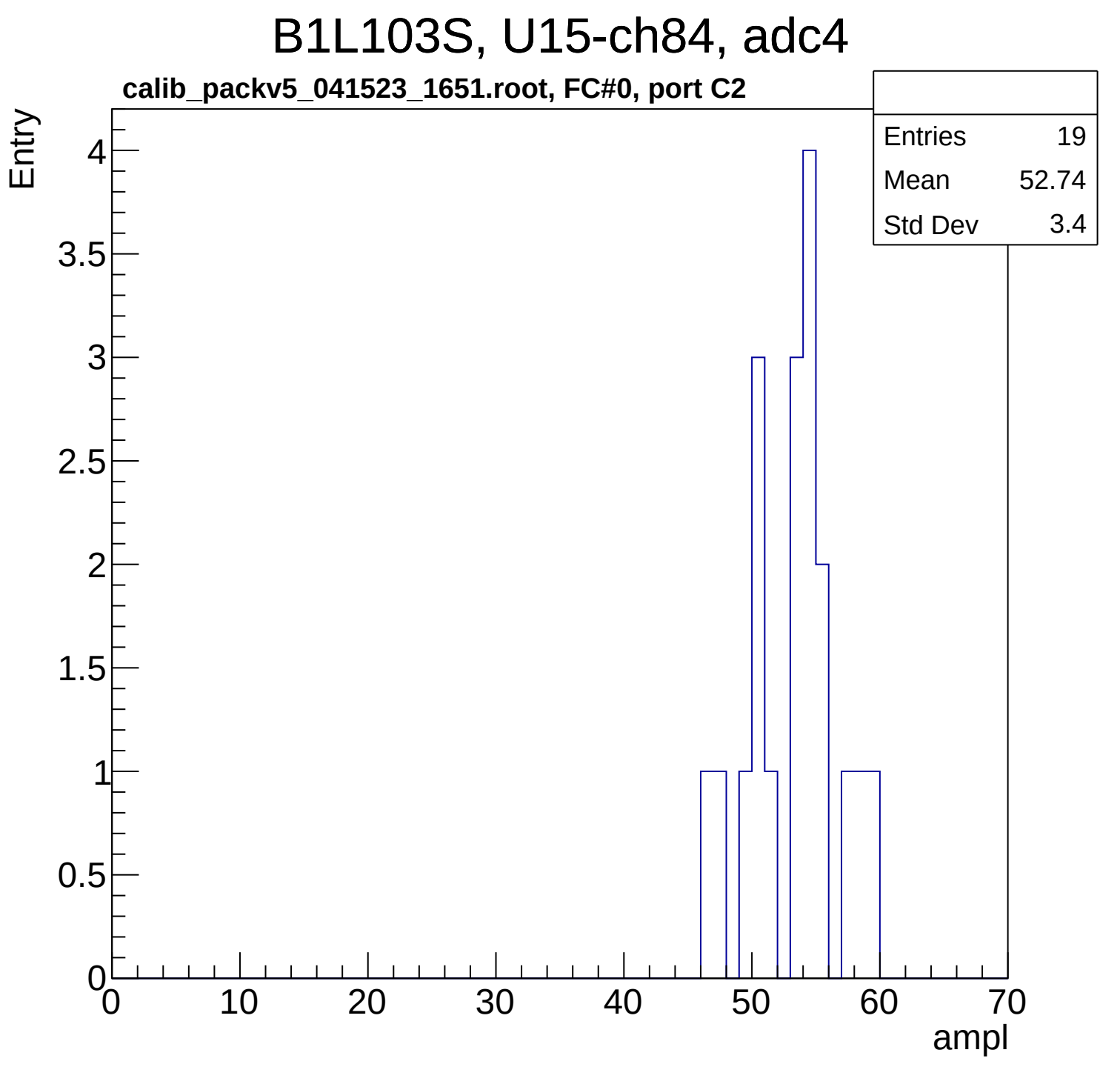

B1L103S, U15-ch83, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

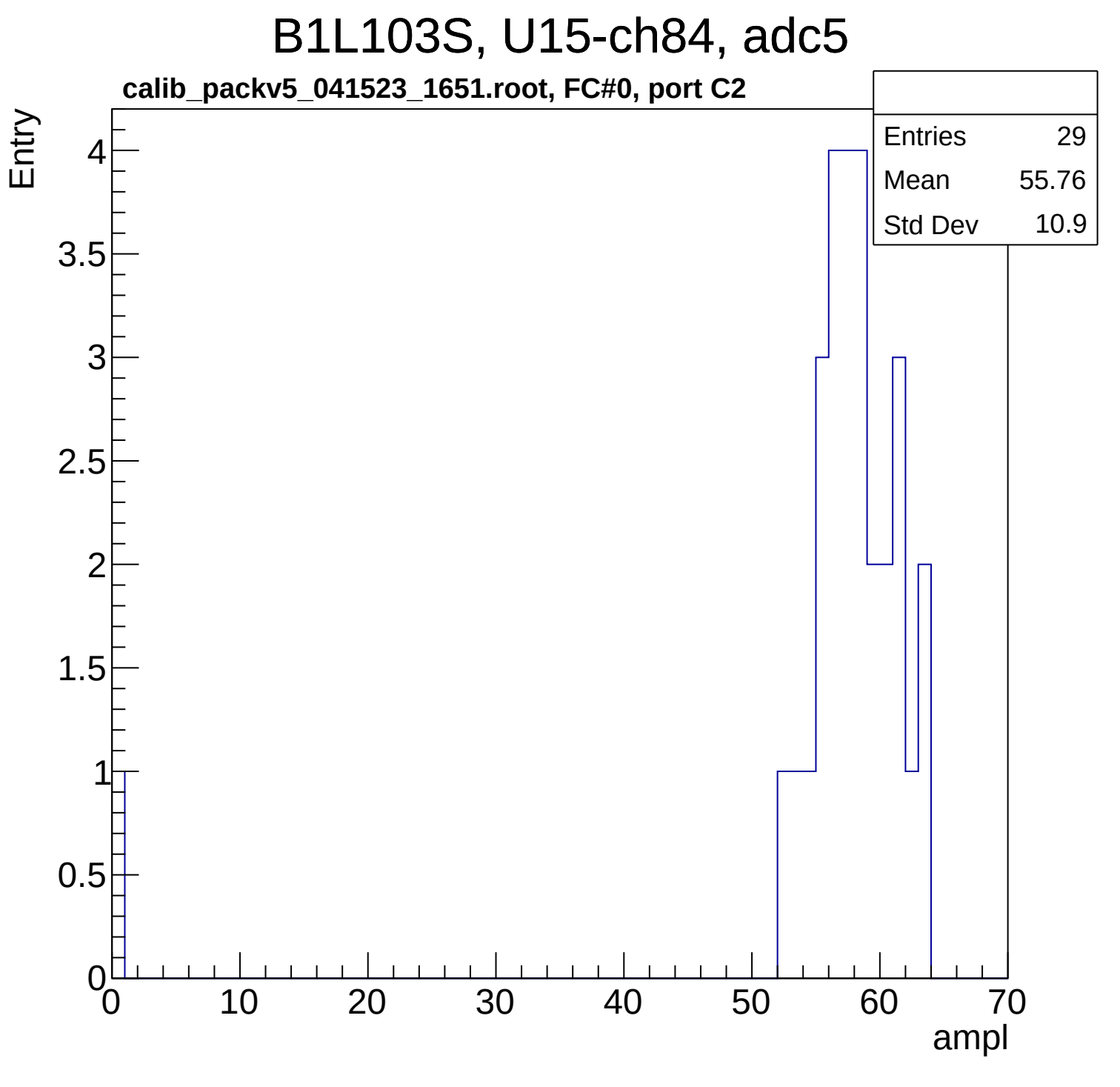

B1L103S, U15-ch84, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 20.46
Std Dev 12.57
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

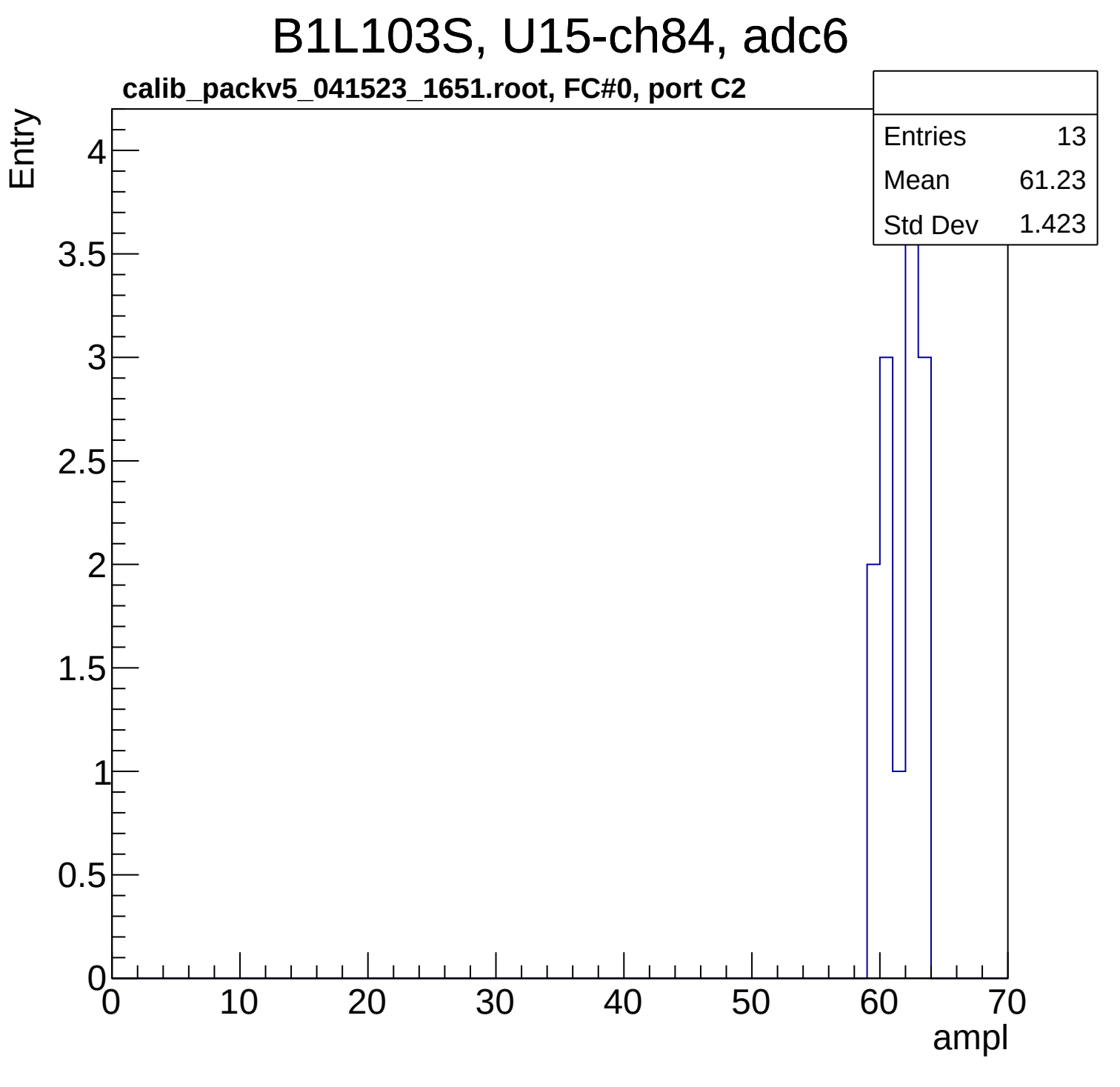

B1L103S, U15-ch84, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 30.27
Std Dev 10.93
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

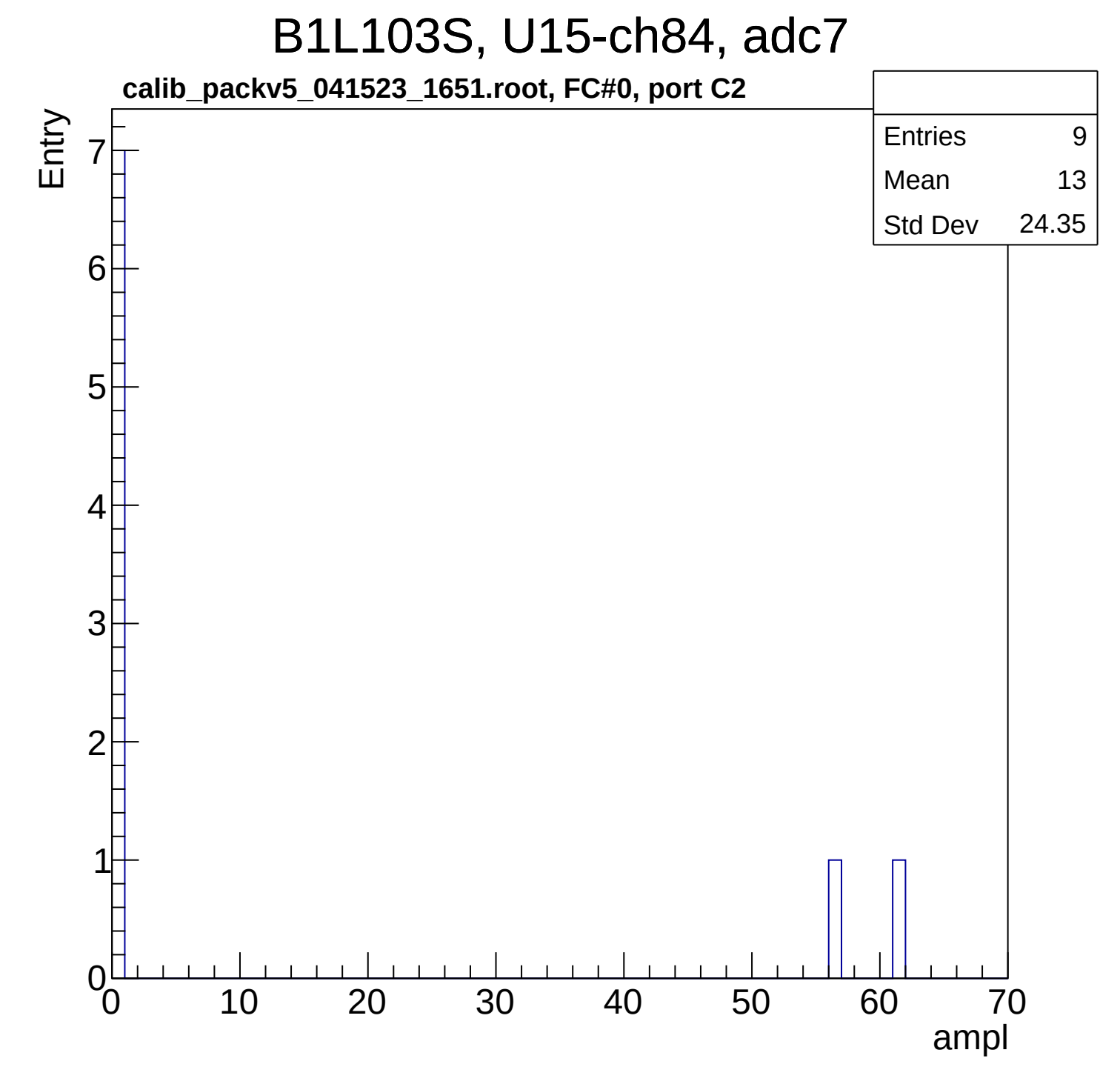

B1L103S, U15-ch84, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 36.21
Std Dev 14.19
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

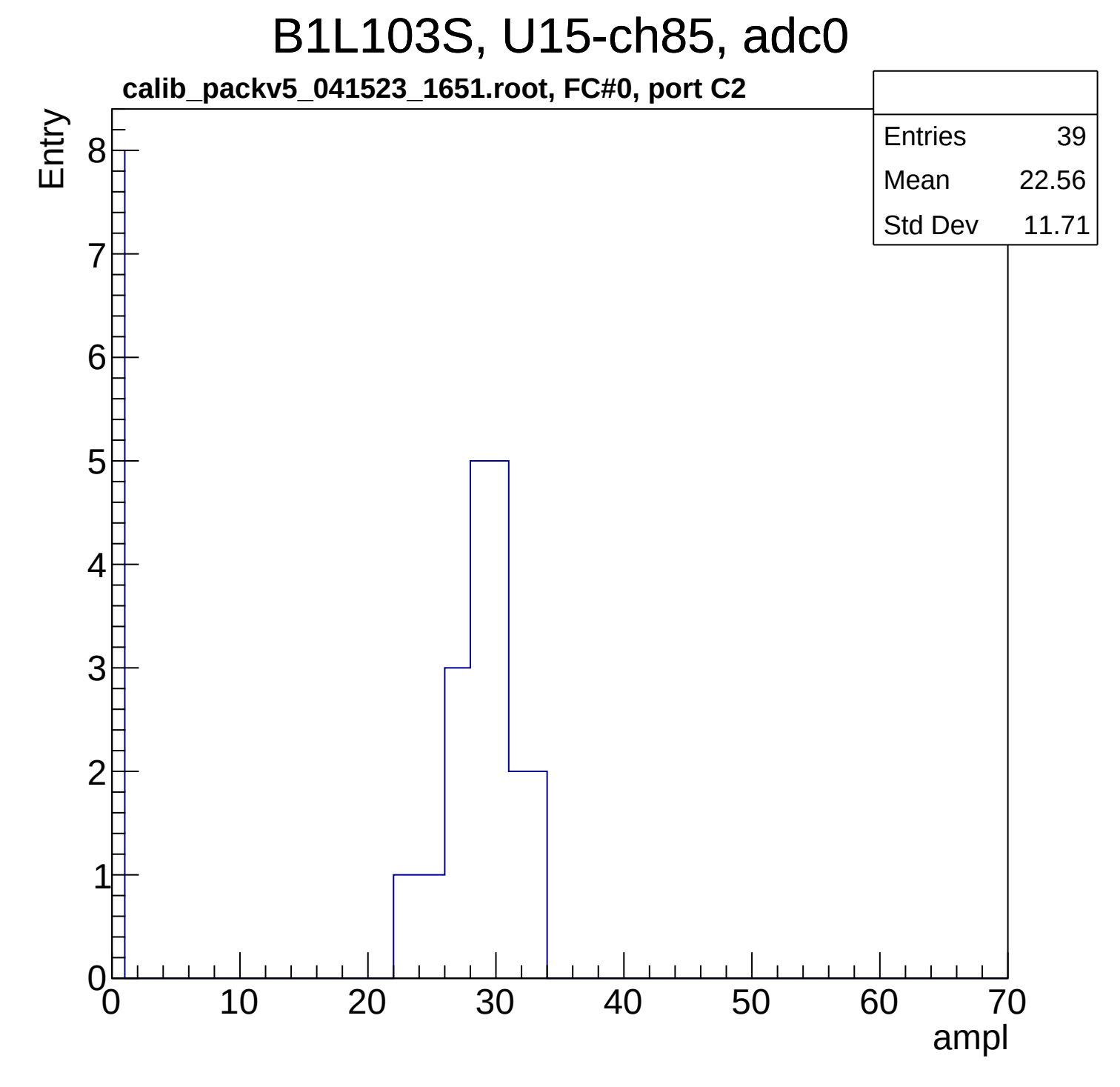

B1L103S, U15-ch84, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 44.94
Std Dev 11.59
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

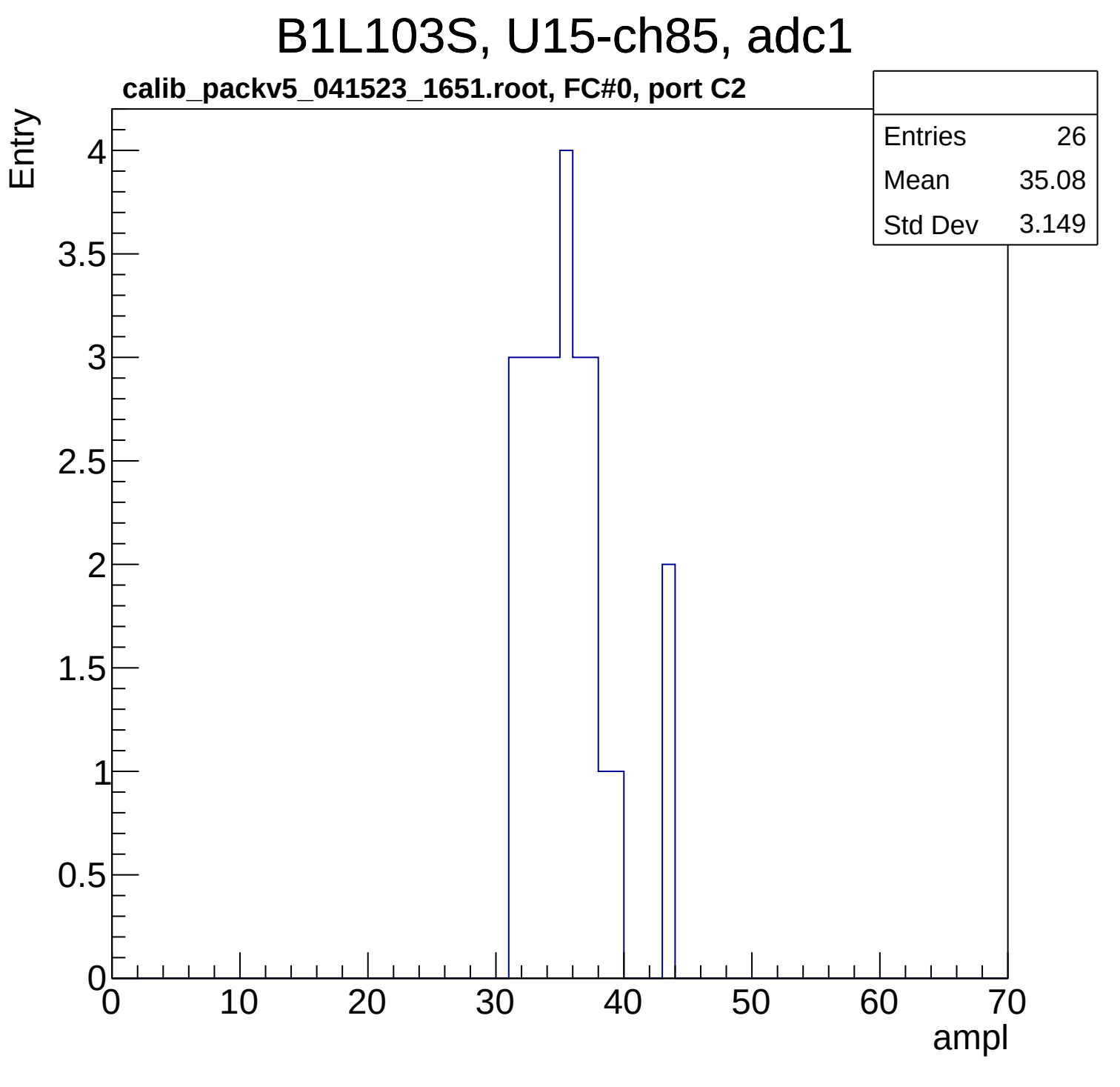

B1L103S, U15-ch84, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 52.74
Std Dev 3.4
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

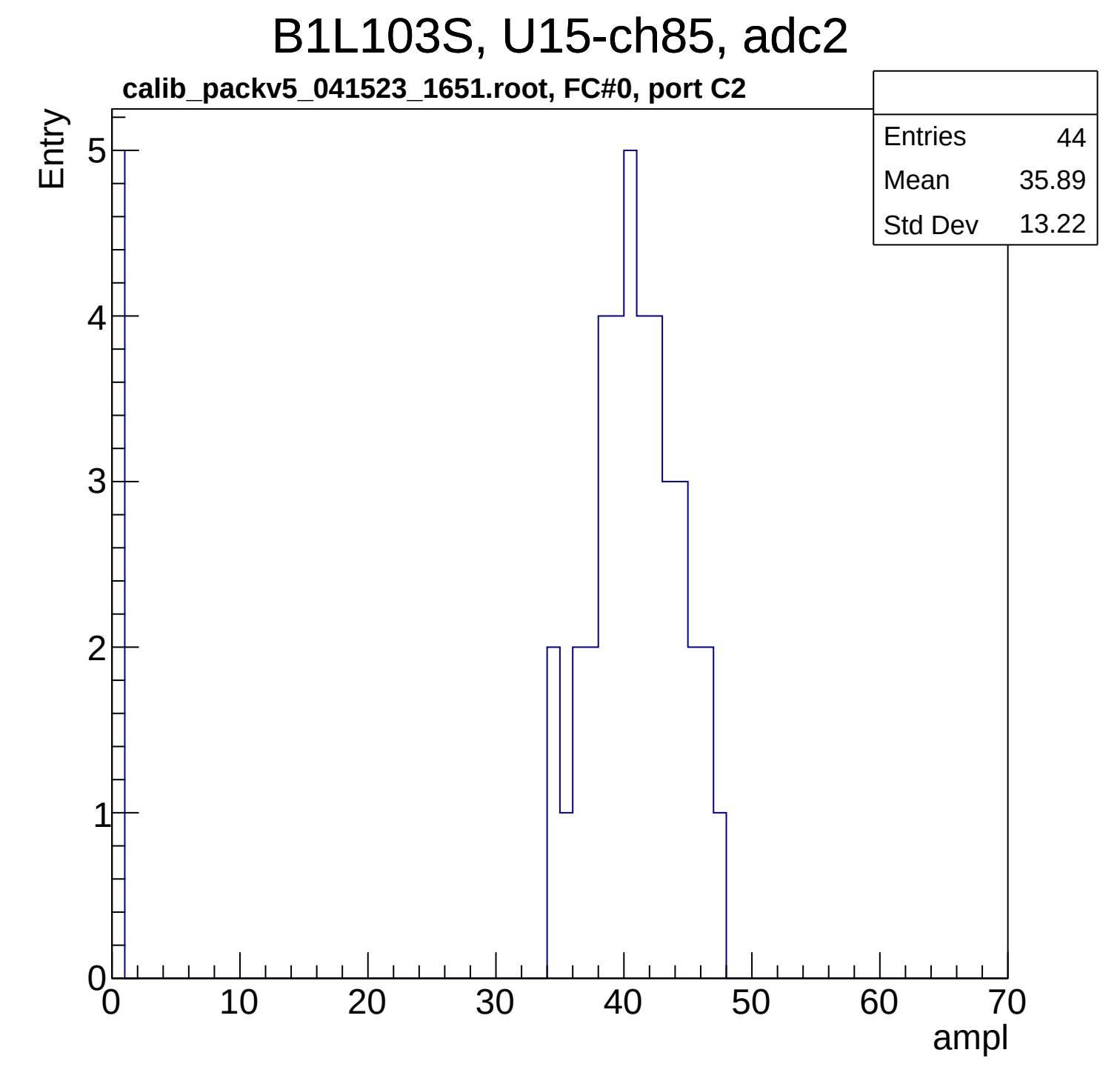

B1L103S, U15-ch84, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 55.76
Std Dev 10.9
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

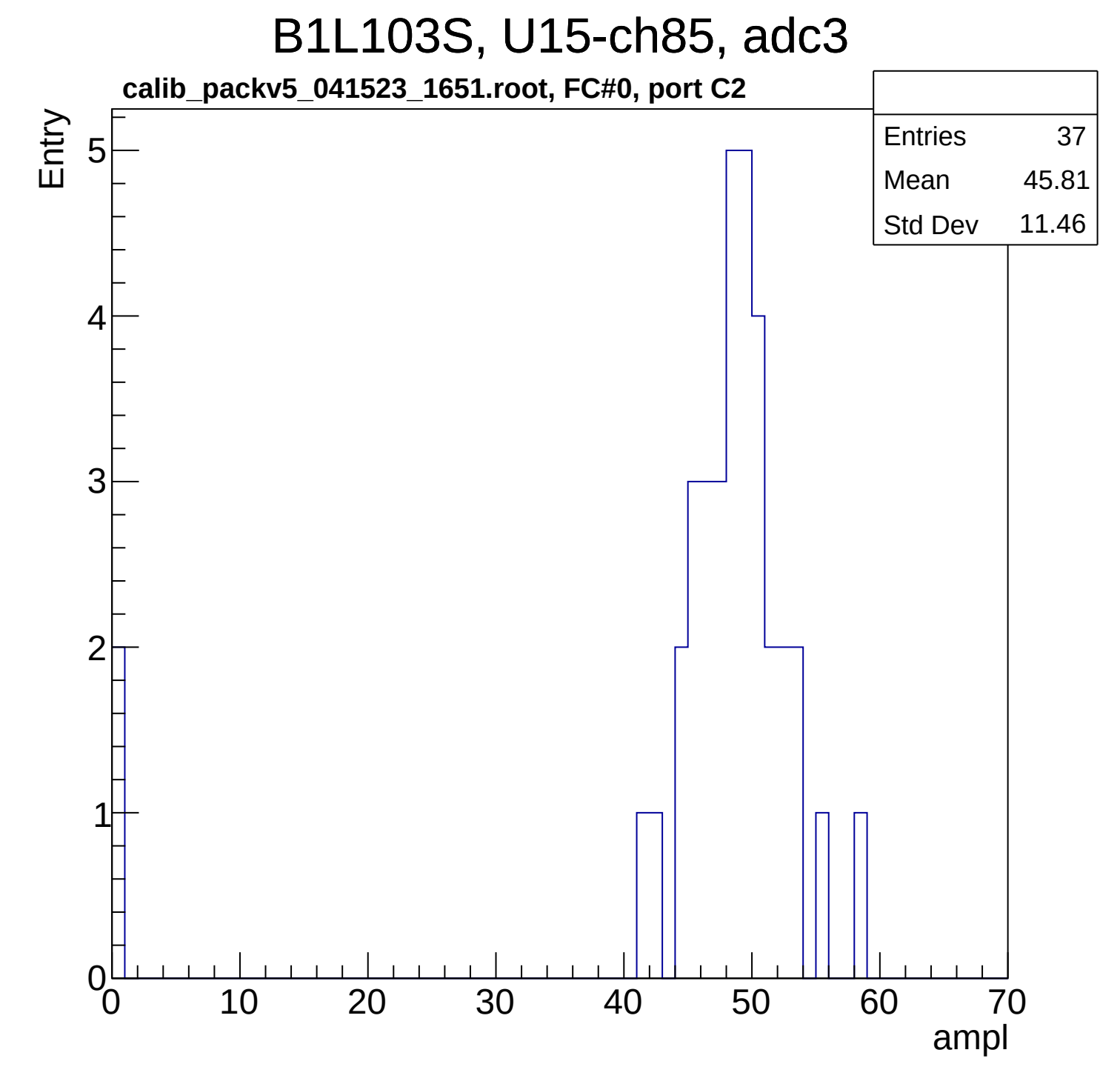

B1L103S, U15-ch84, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.23
Std Dev 1.423
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

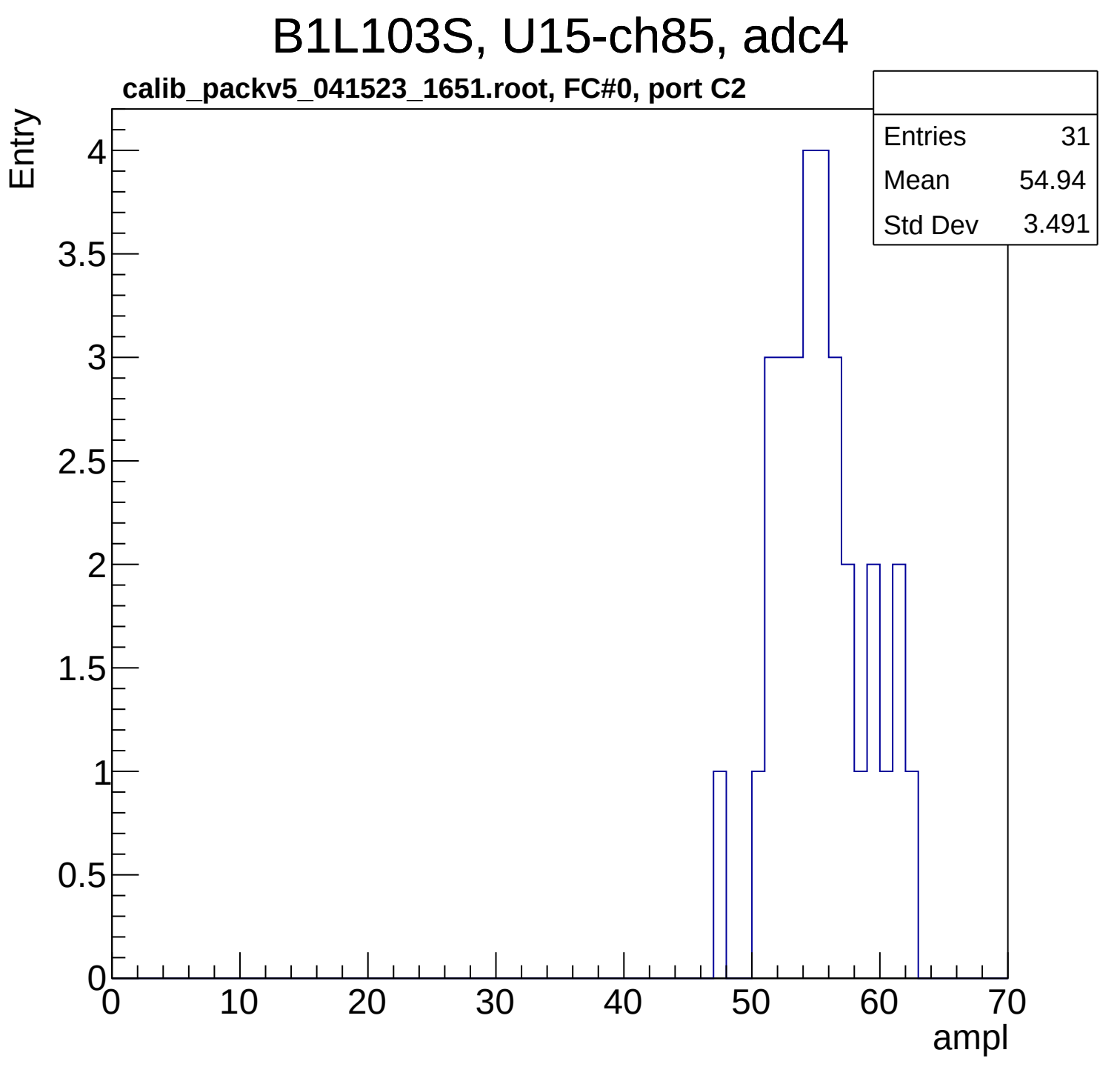

B1L103S, U15-ch84, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 13
Std Dev 24.35
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

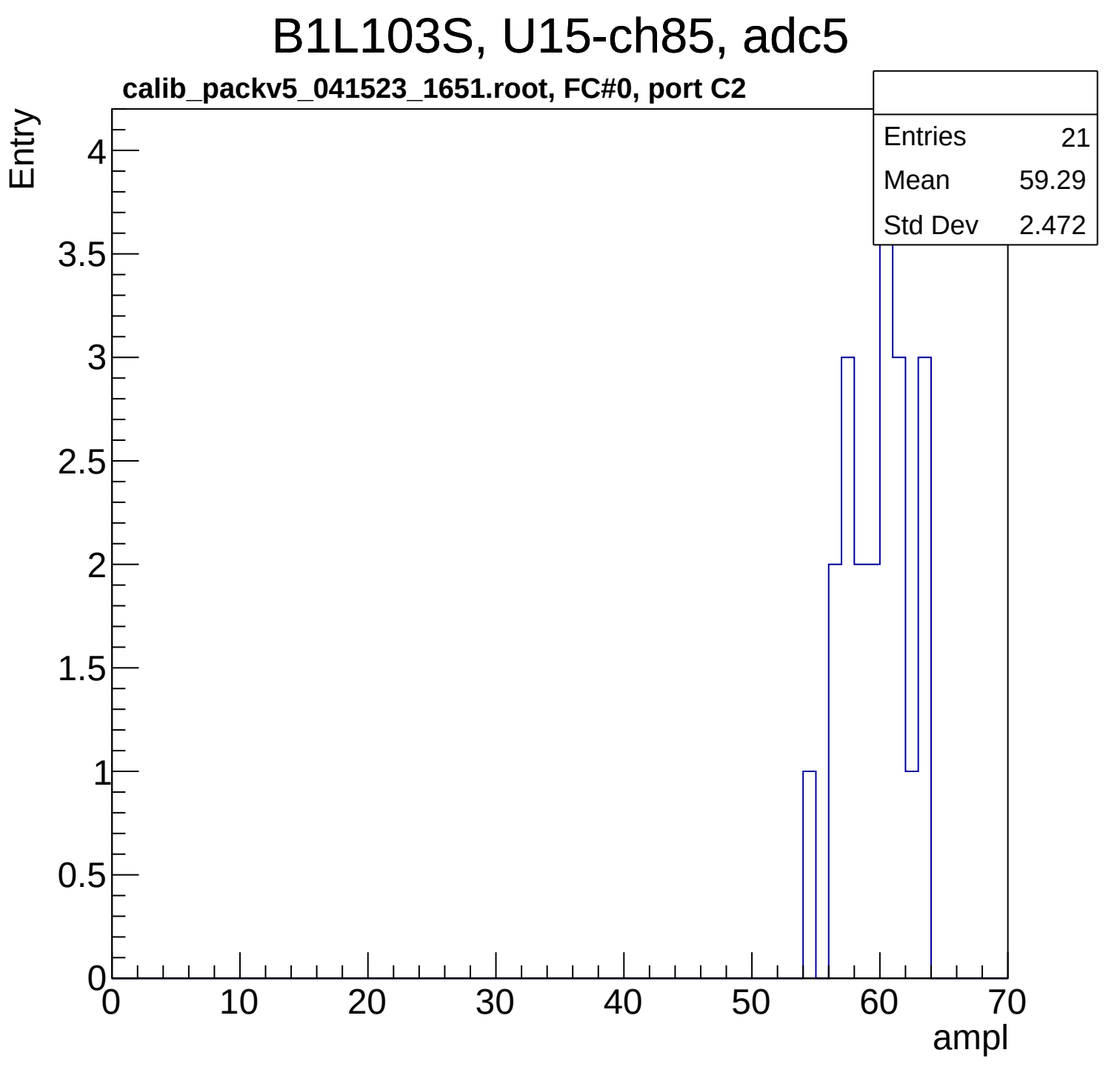

B1L103S, U15-ch85, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 22.56
Std Dev 11.71
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U15-ch85, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 35.08
Std Dev 3.149
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch85, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 35.89
Std Dev 13.22
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch85, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 45.81
Std Dev 11.46
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch85, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 54.94
Std Dev 3.491
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch85, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 59.29
Std Dev 2.472
Entry
ampl
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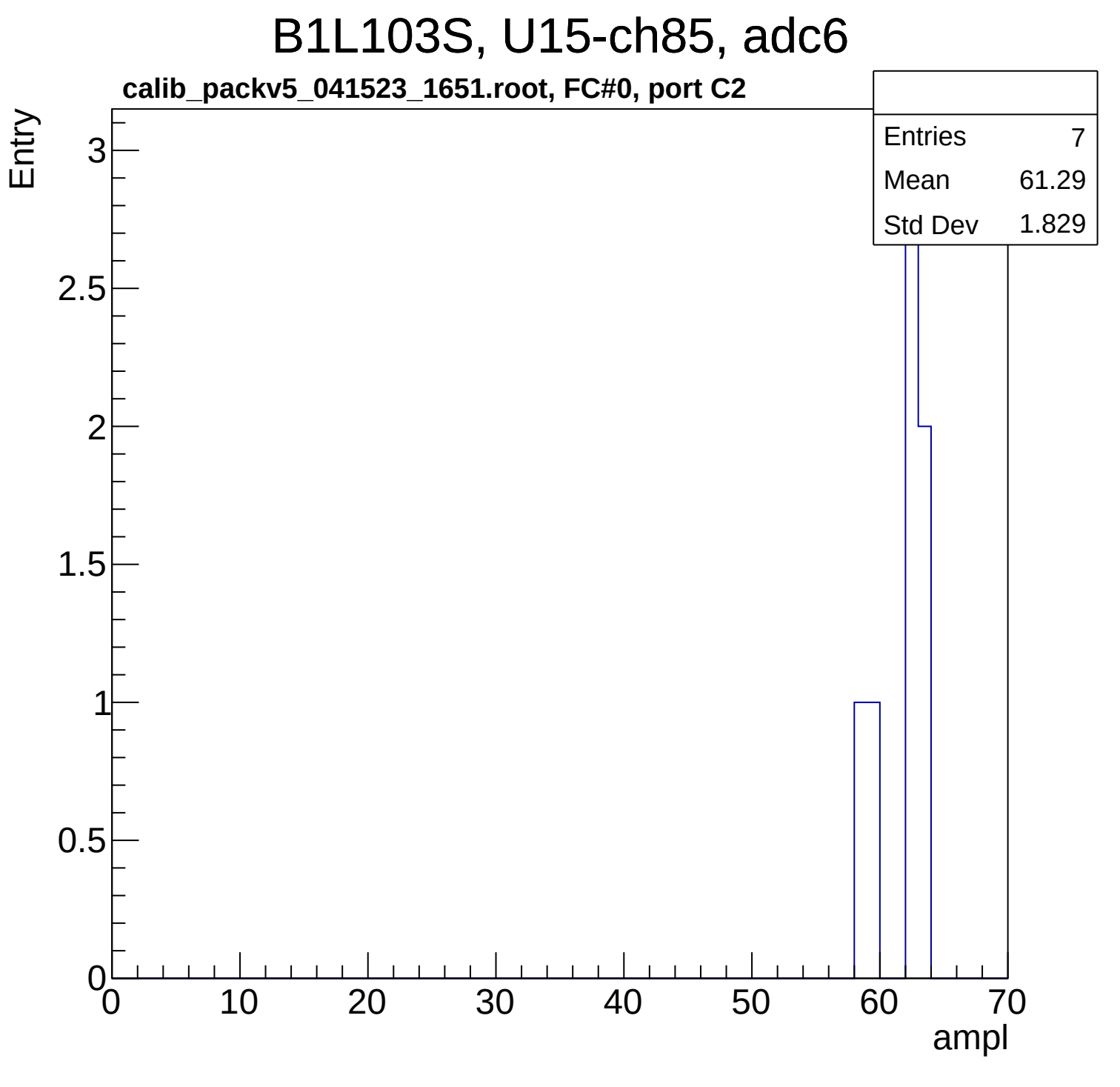
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch85, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.29
Std Dev 1.829
Entry
ampl
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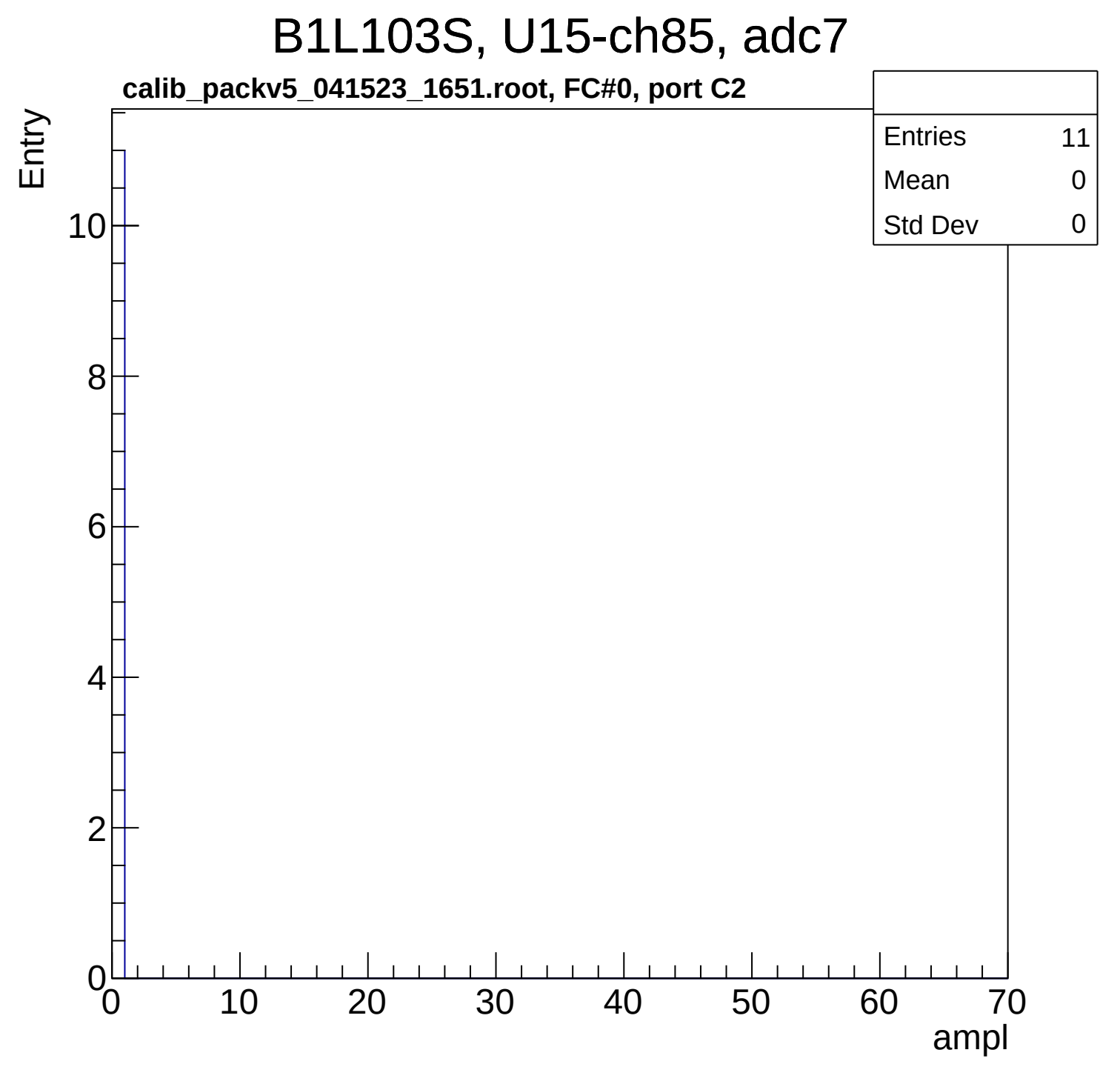
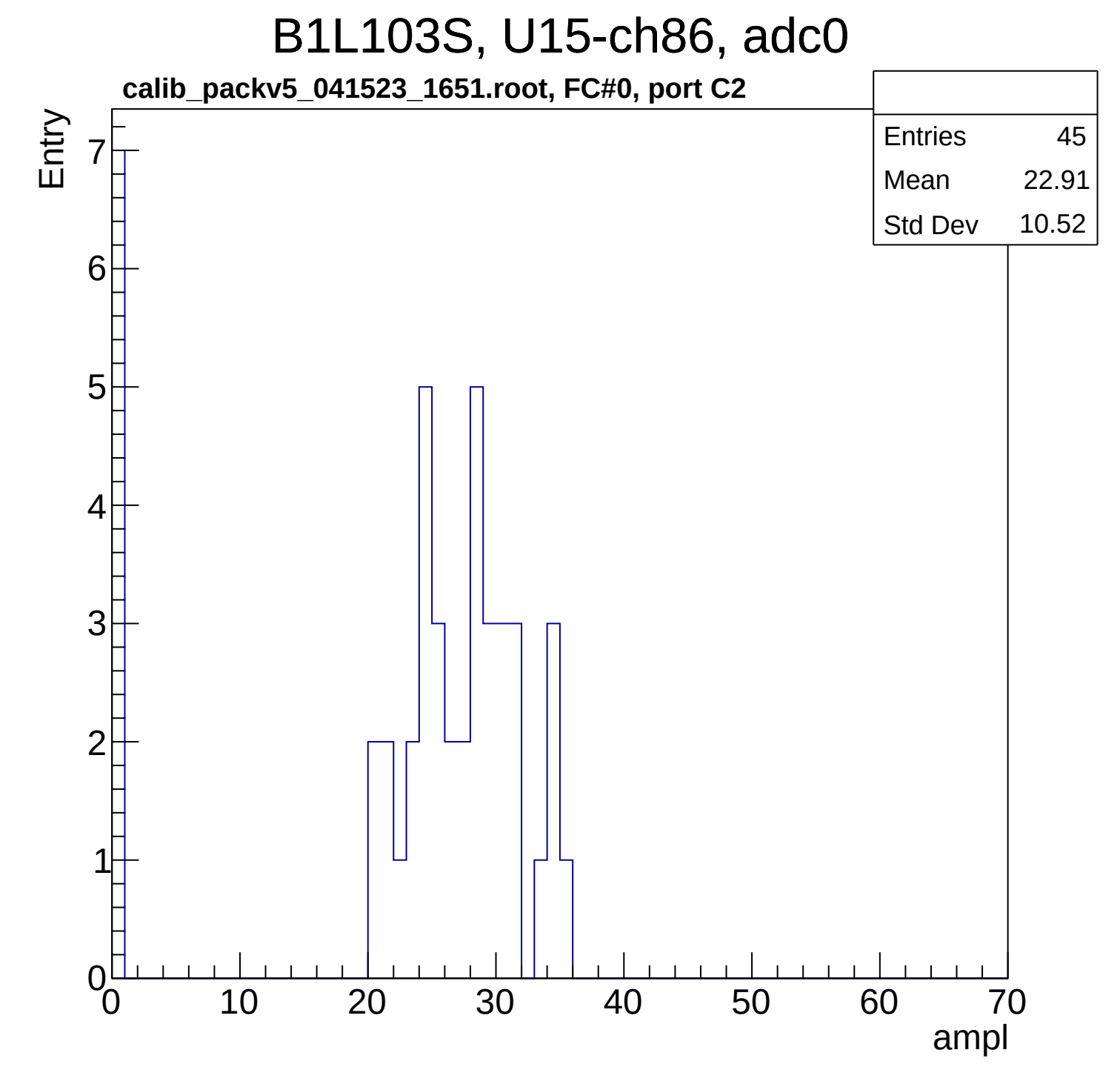
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch85, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch86, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 22.91
Std Dev 10.52
Entry
ampl
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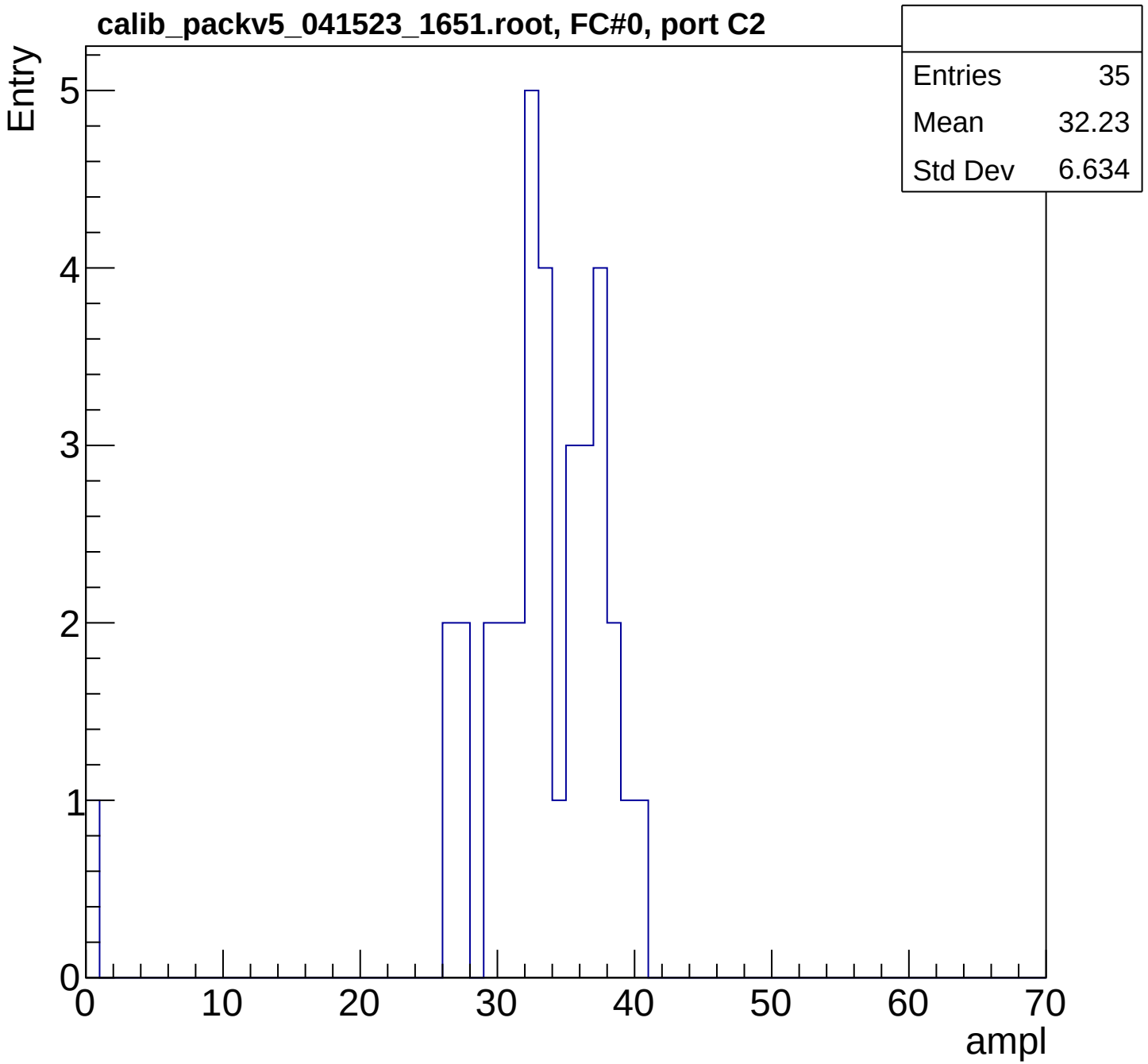
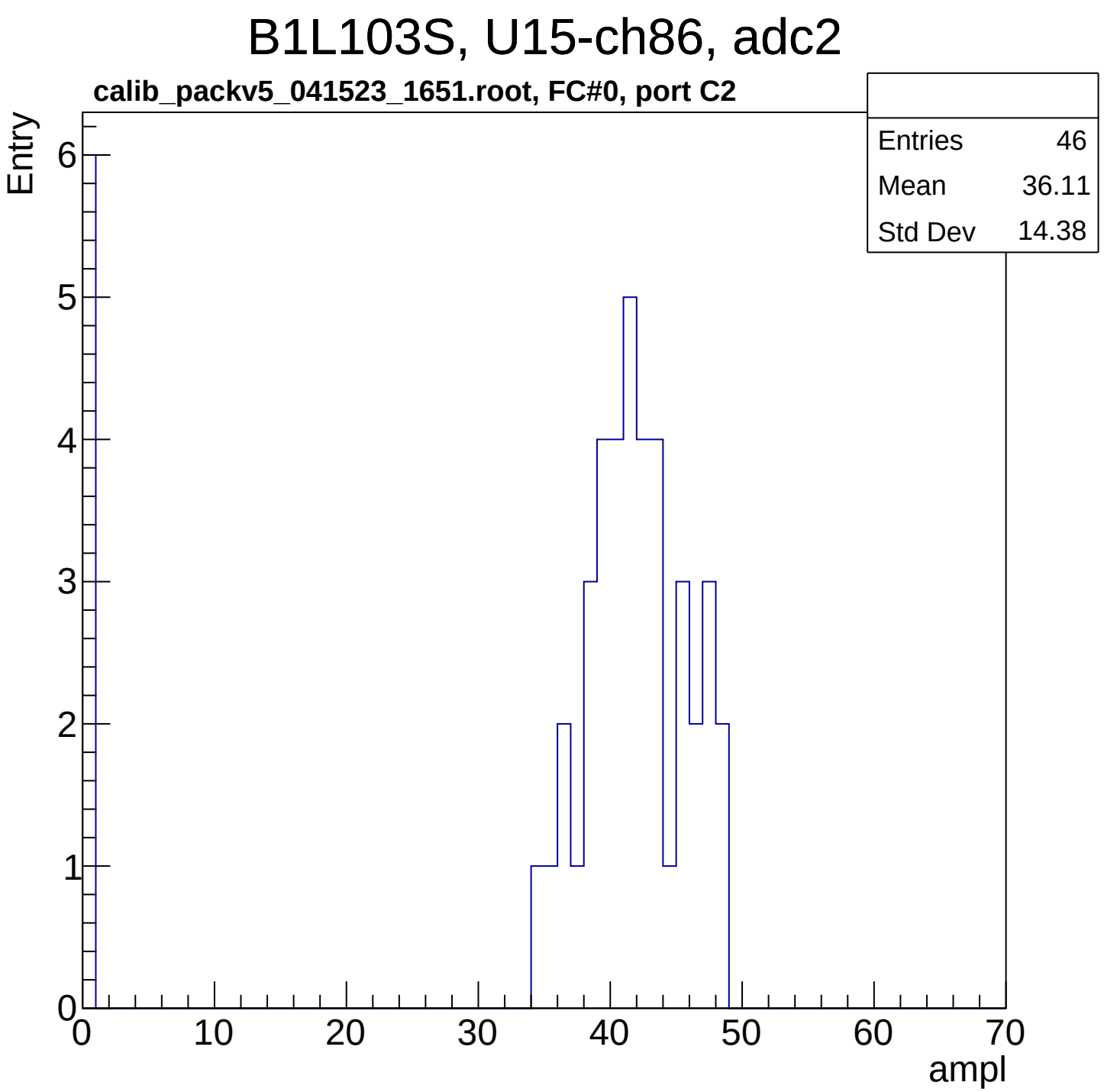
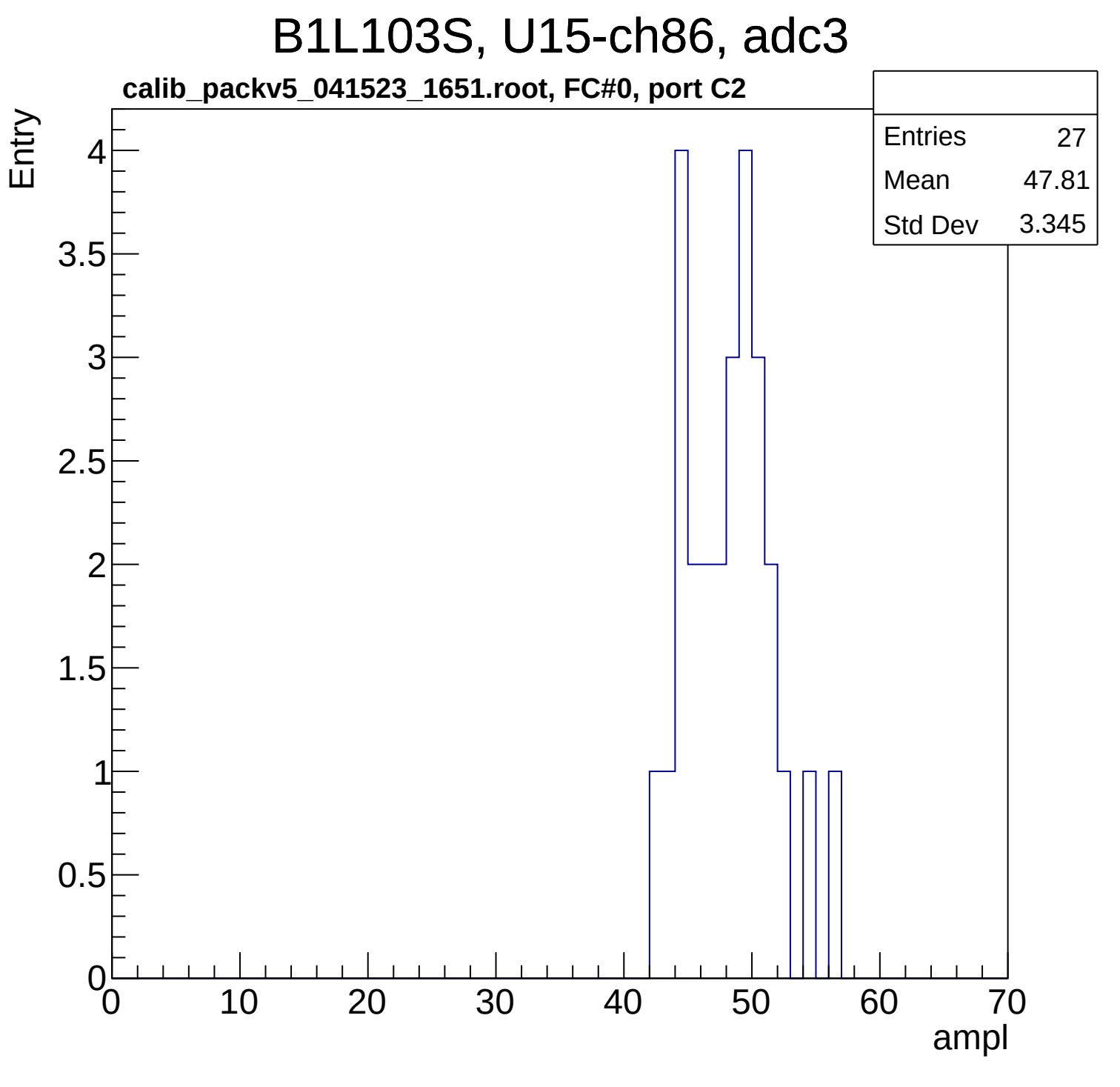
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U15-ch86, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 32.23
Std Dev 6.634
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch86, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 36.11
Std Dev 14.38
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U15-ch86, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 47.81
Std Dev 3.345
Entry
ampl
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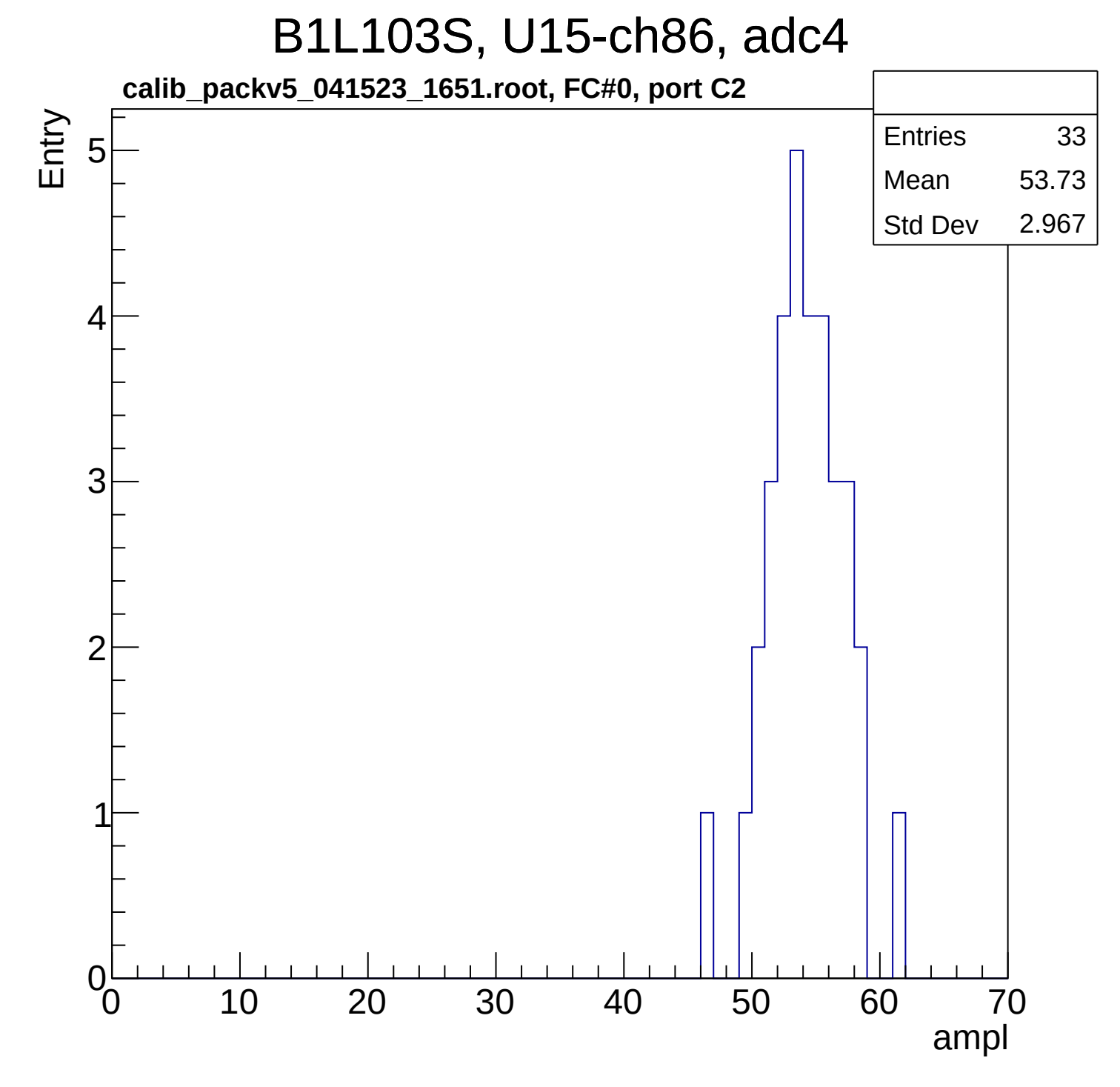
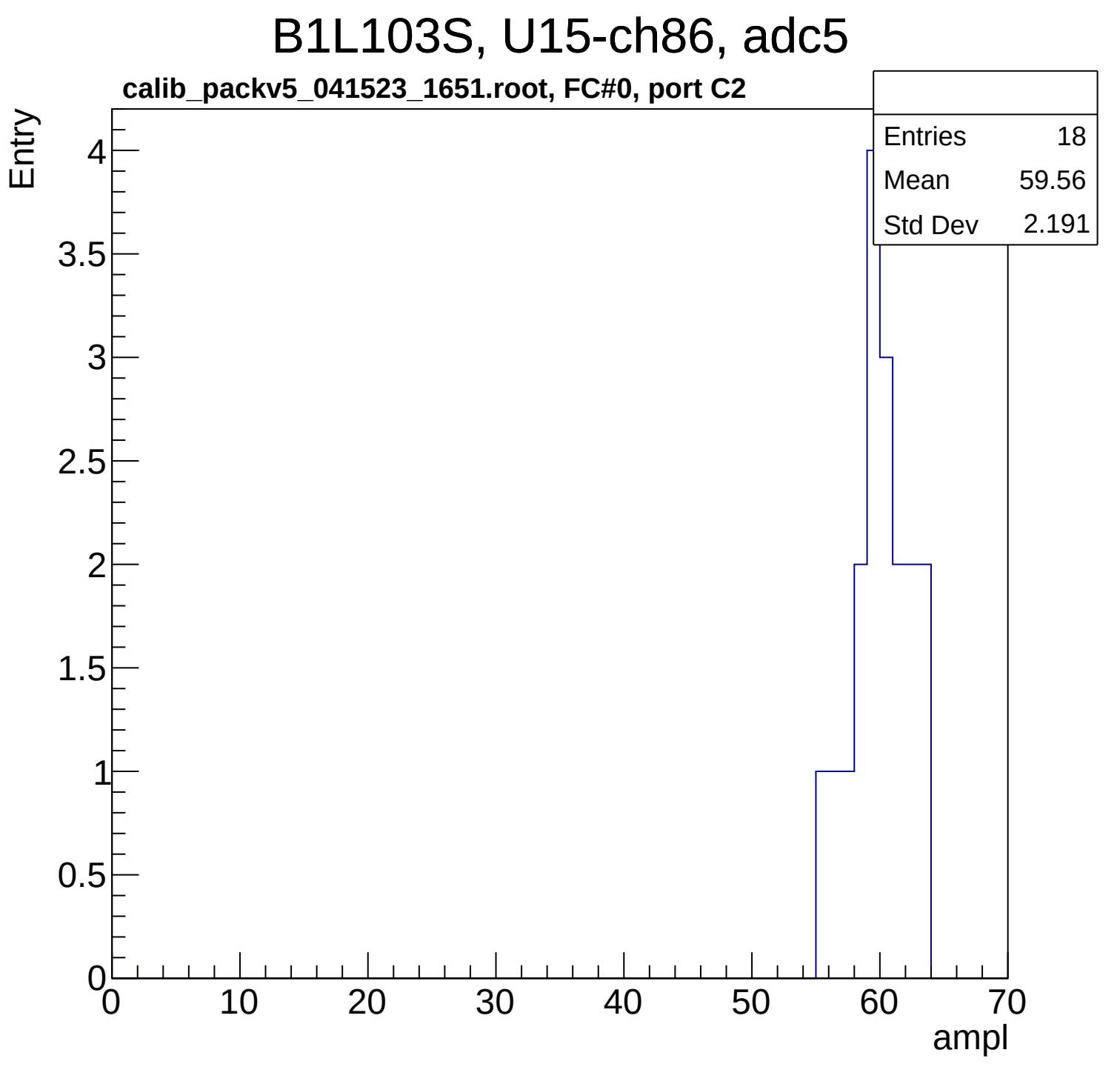
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch86, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 53.73
Std Dev 2.967
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch86, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 59.56
Std Dev 2.191
Entry
ampl
0
0.5
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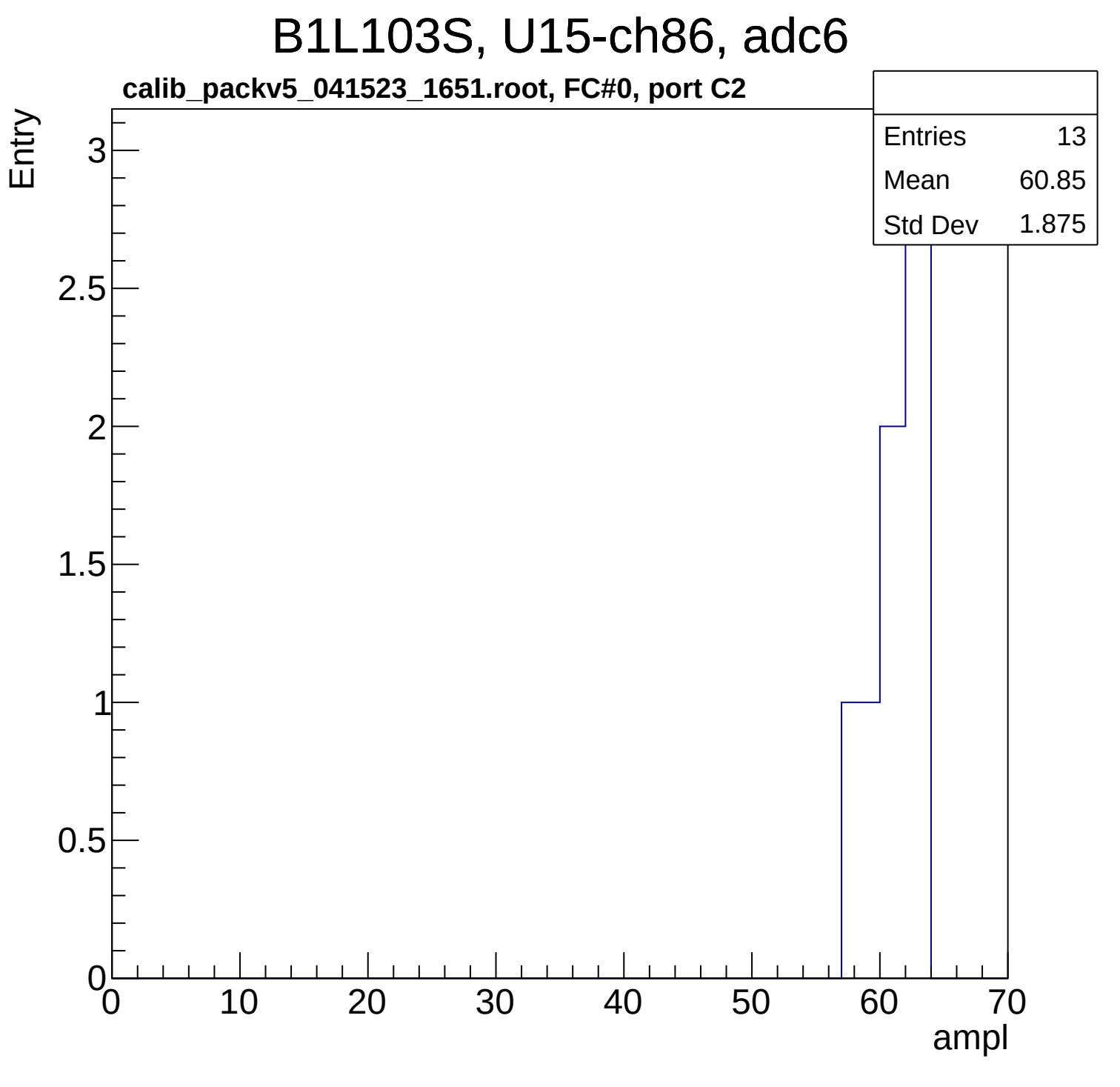
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch86, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 60.85
Std Dev 1.875
Entry
ampl
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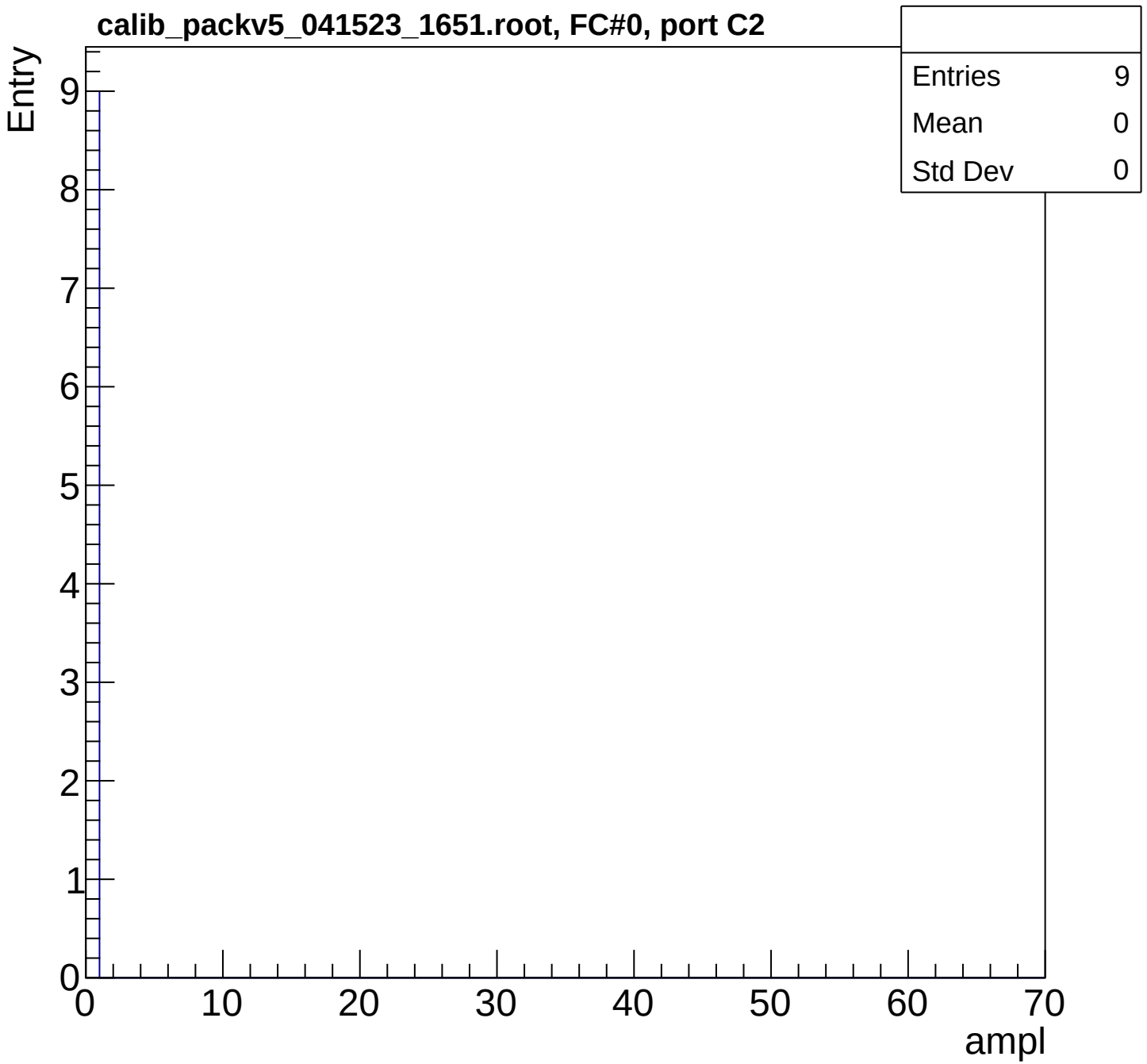
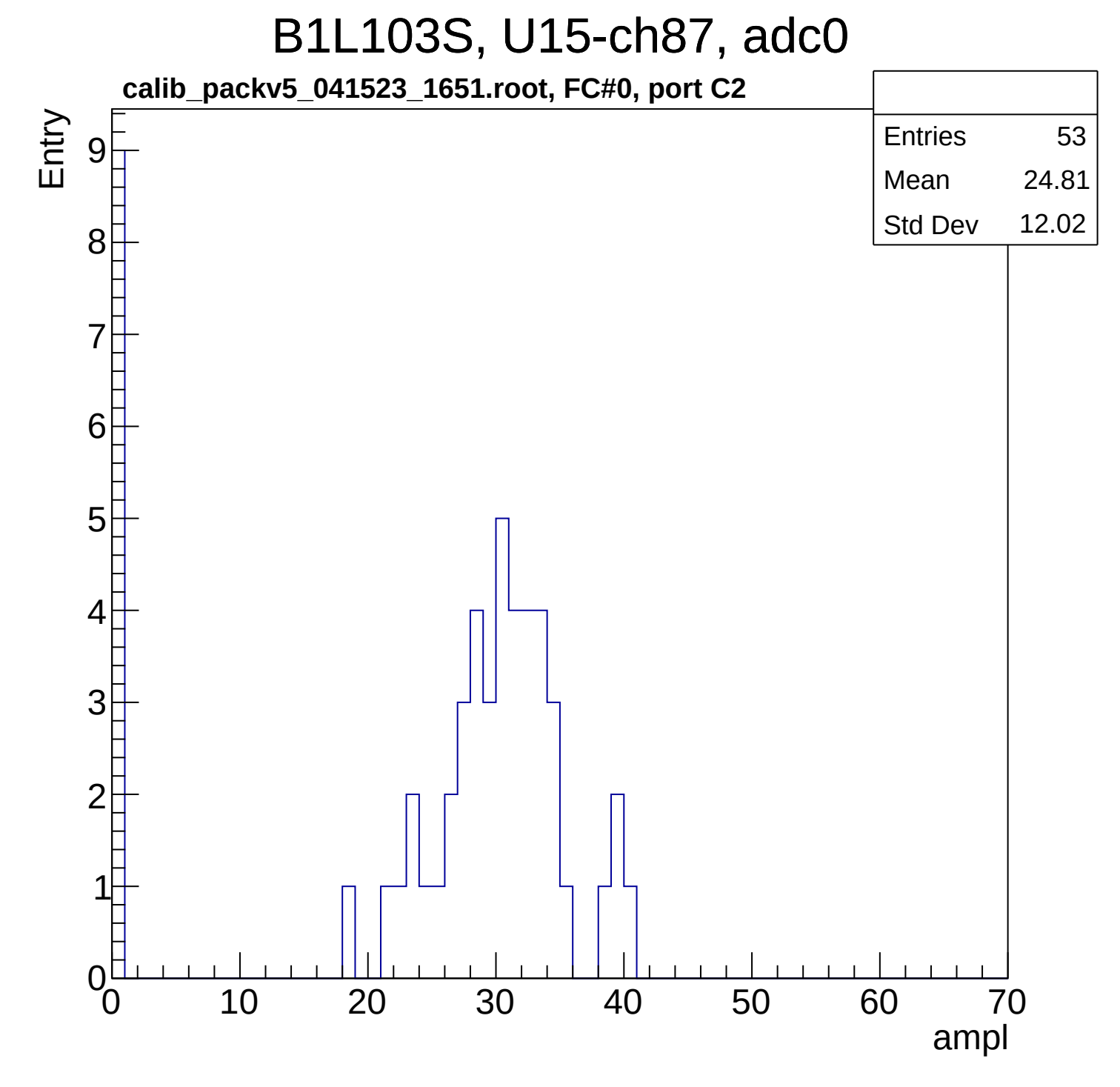
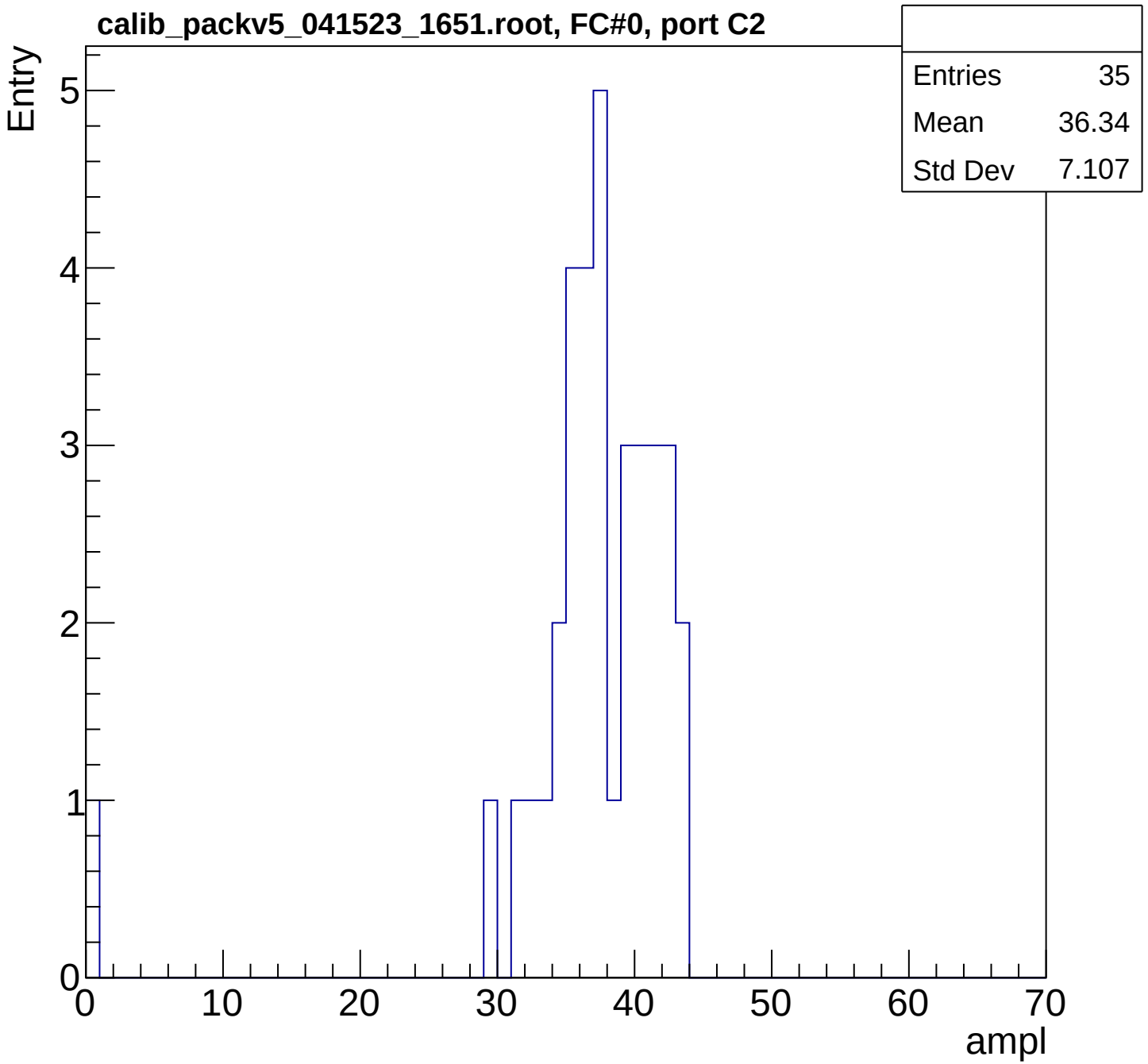
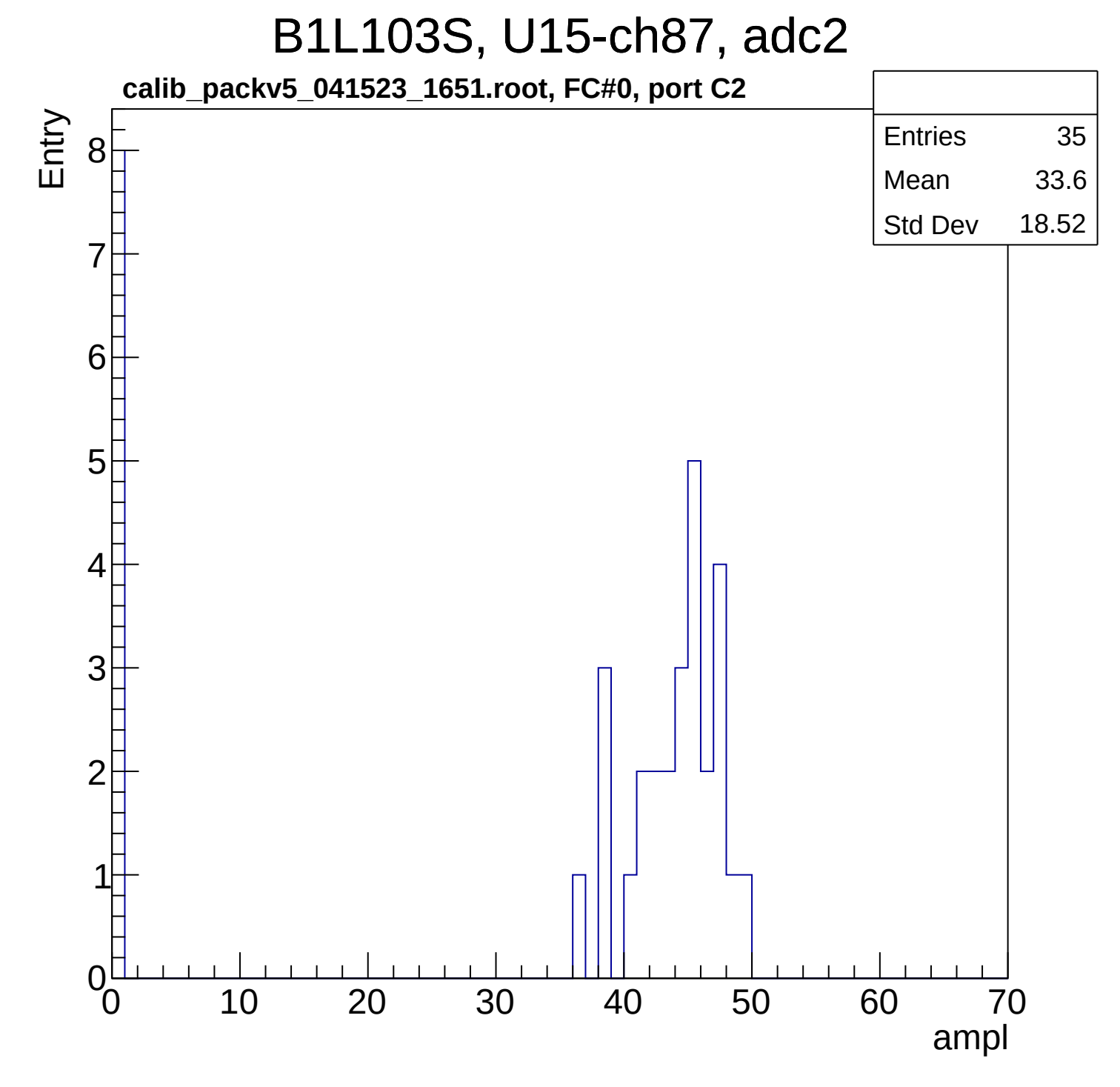
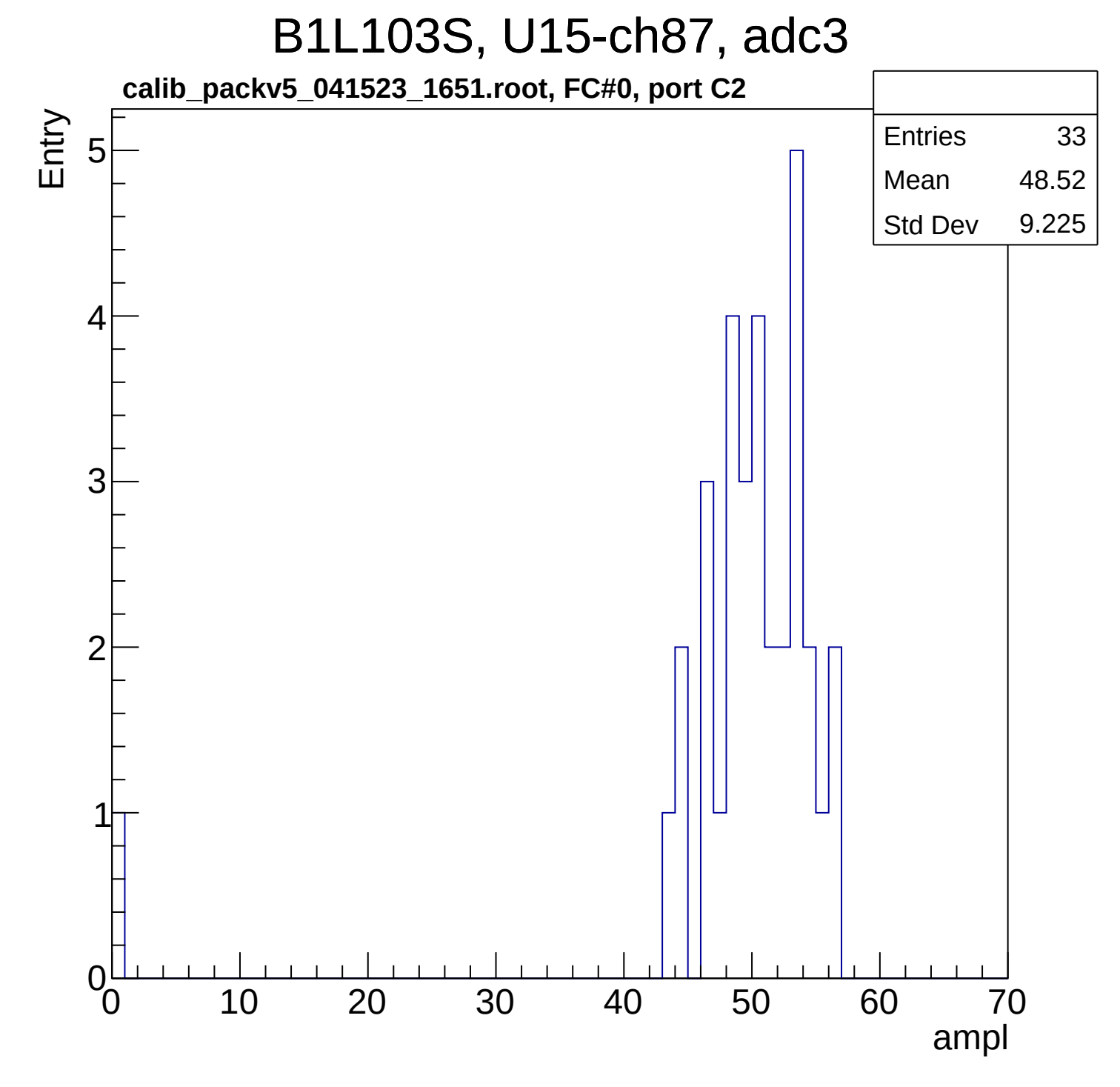
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

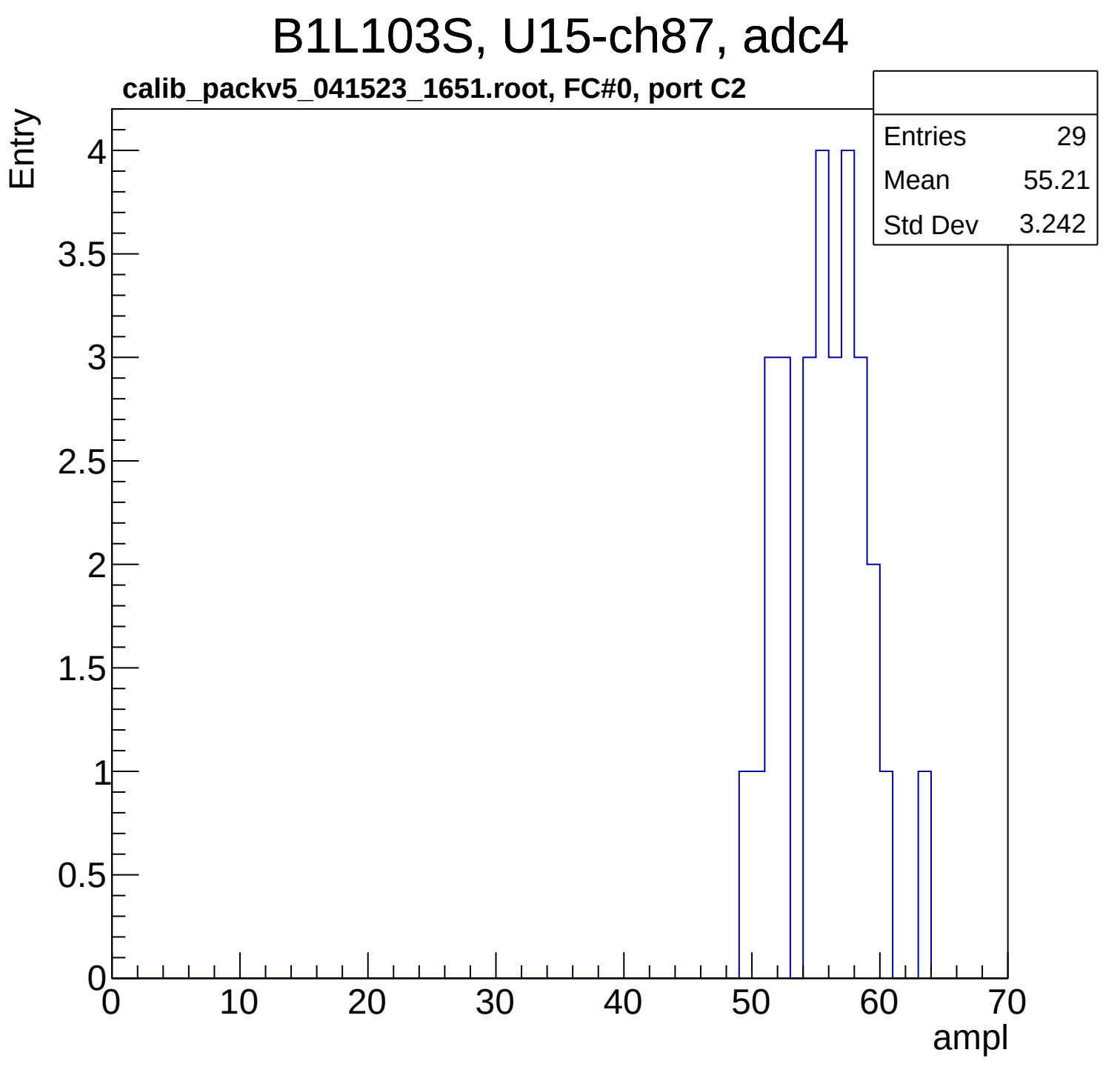

B1L103S, U15-ch86, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 0
Std Dev 0
Entry
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70
ampl

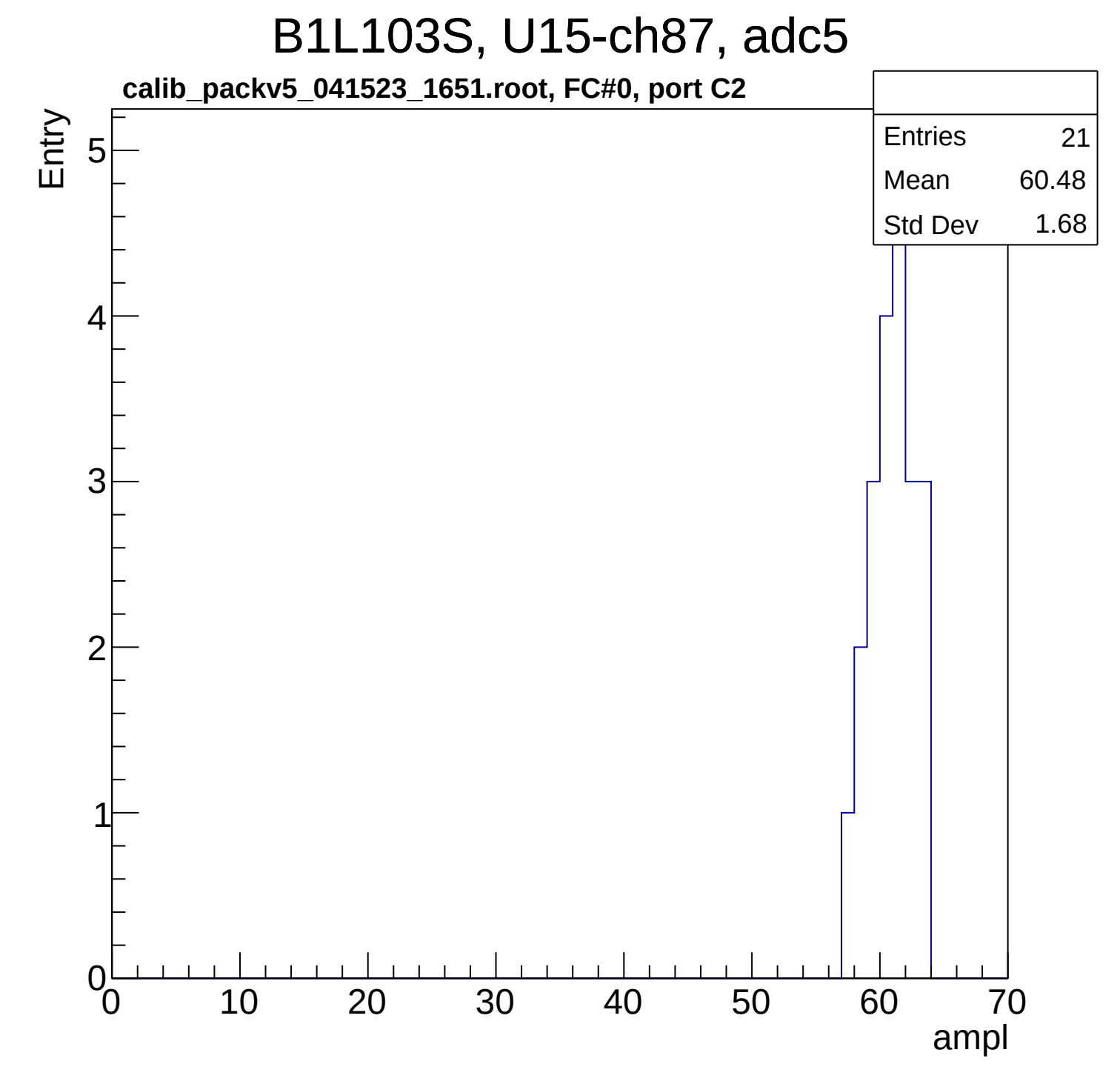

B1L103S, U15-ch87, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 24.81
Std Dev 12.02
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

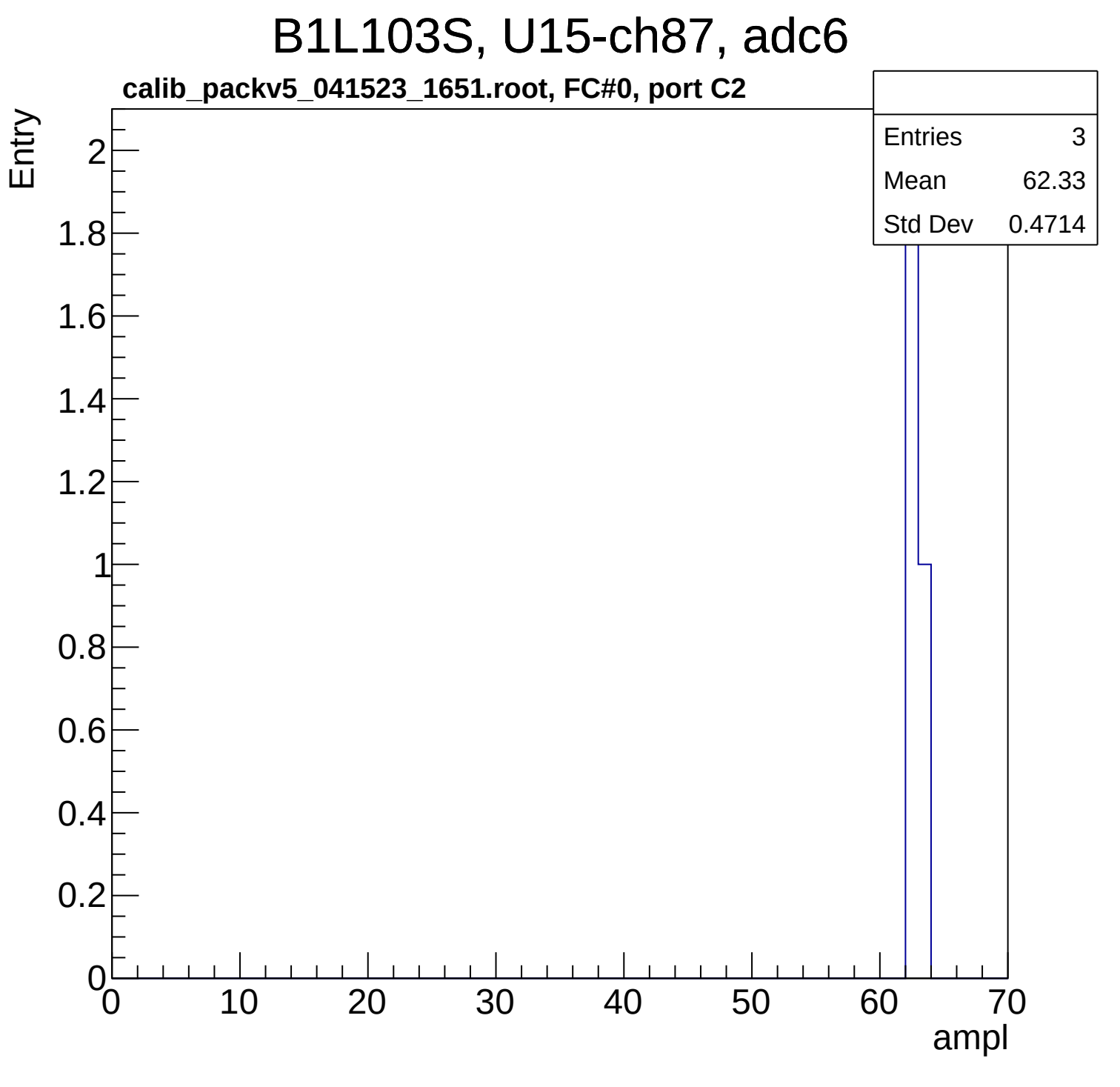

B1L103S, U15-ch87, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 36.34
Std Dev 7.107
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

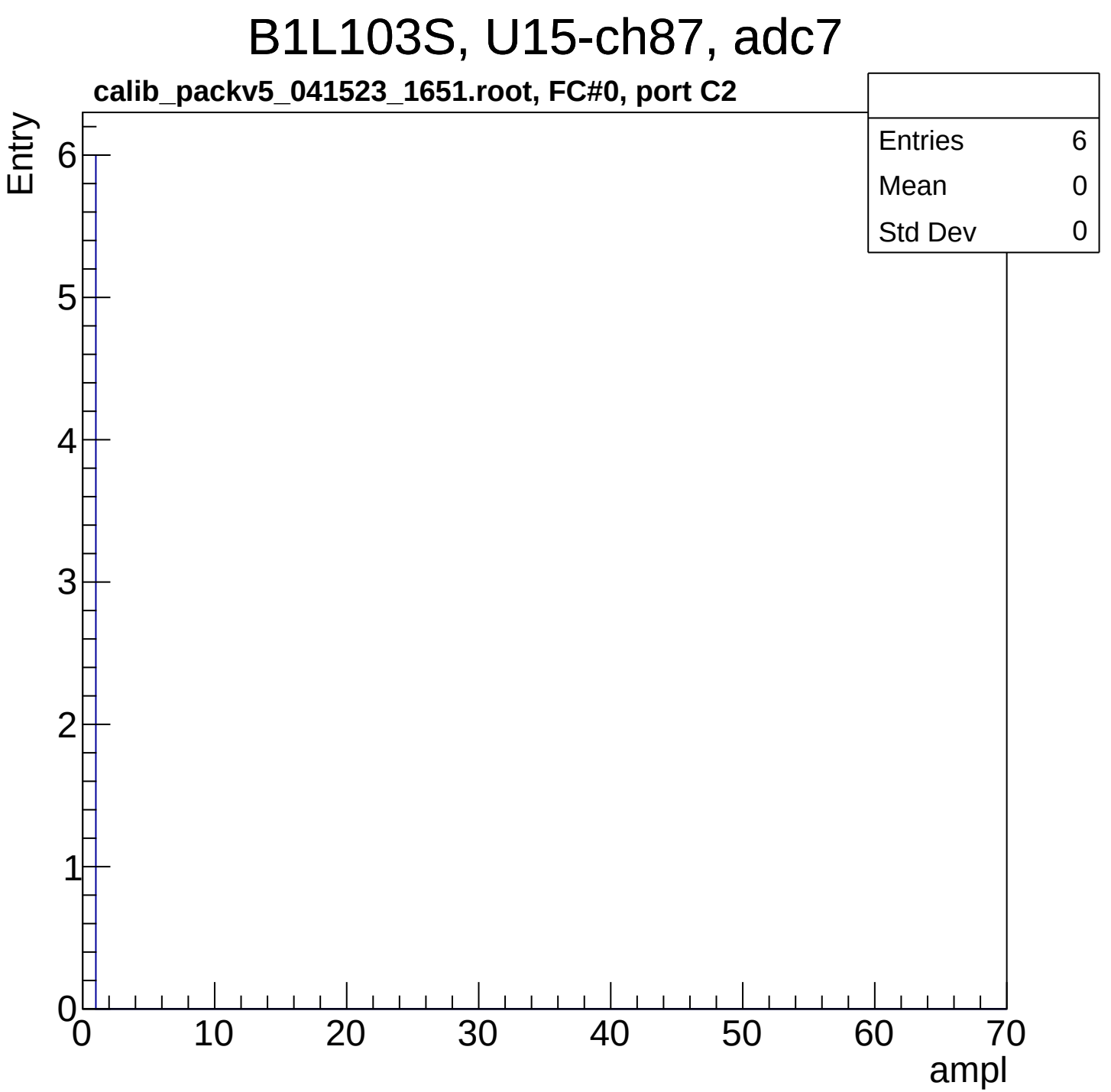

B1L103S, U15-ch87, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 33.6
Std Dev 18.52
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

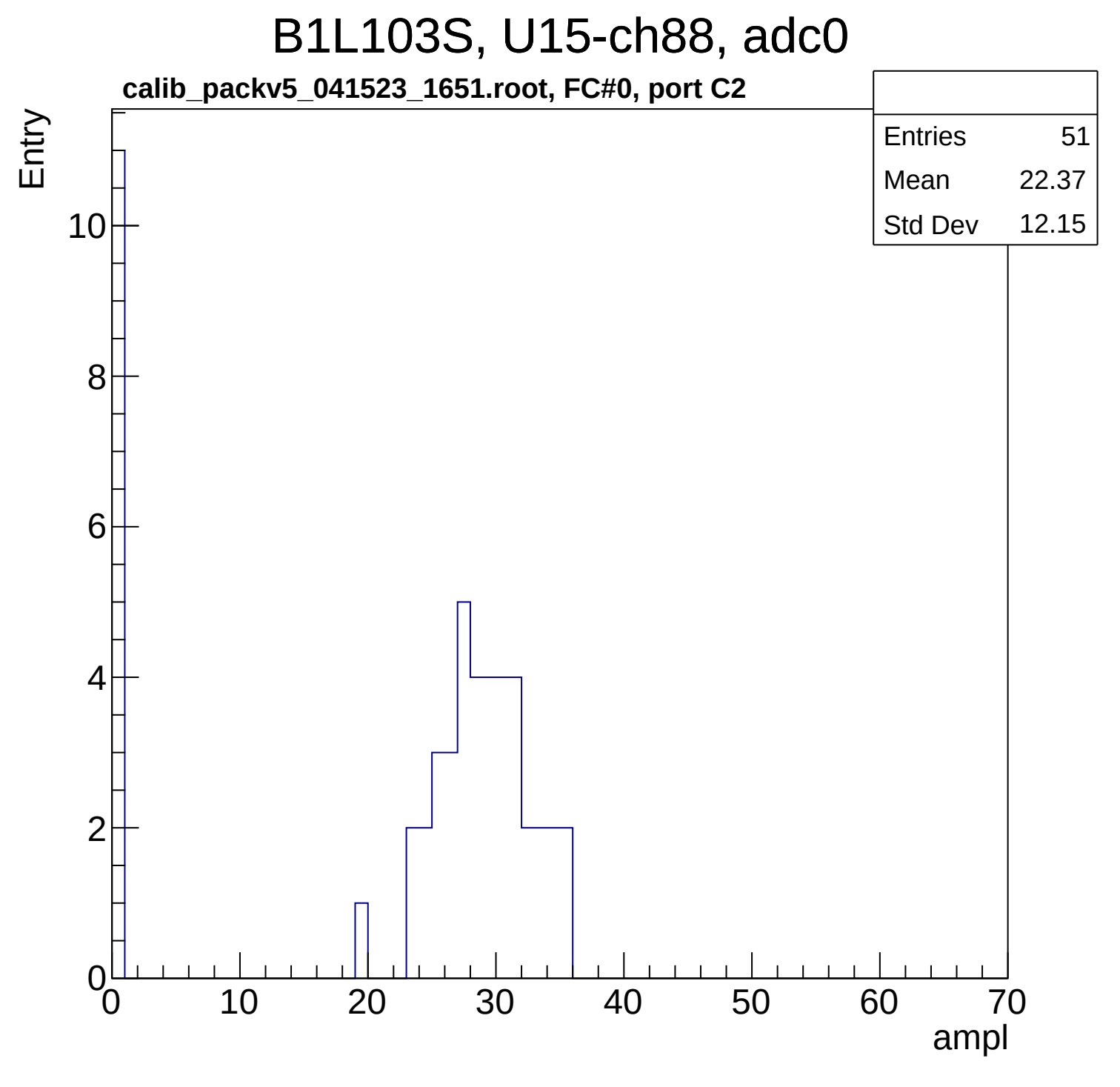

B1L103S, U15-ch87, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 48.52
Std Dev 9.225
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

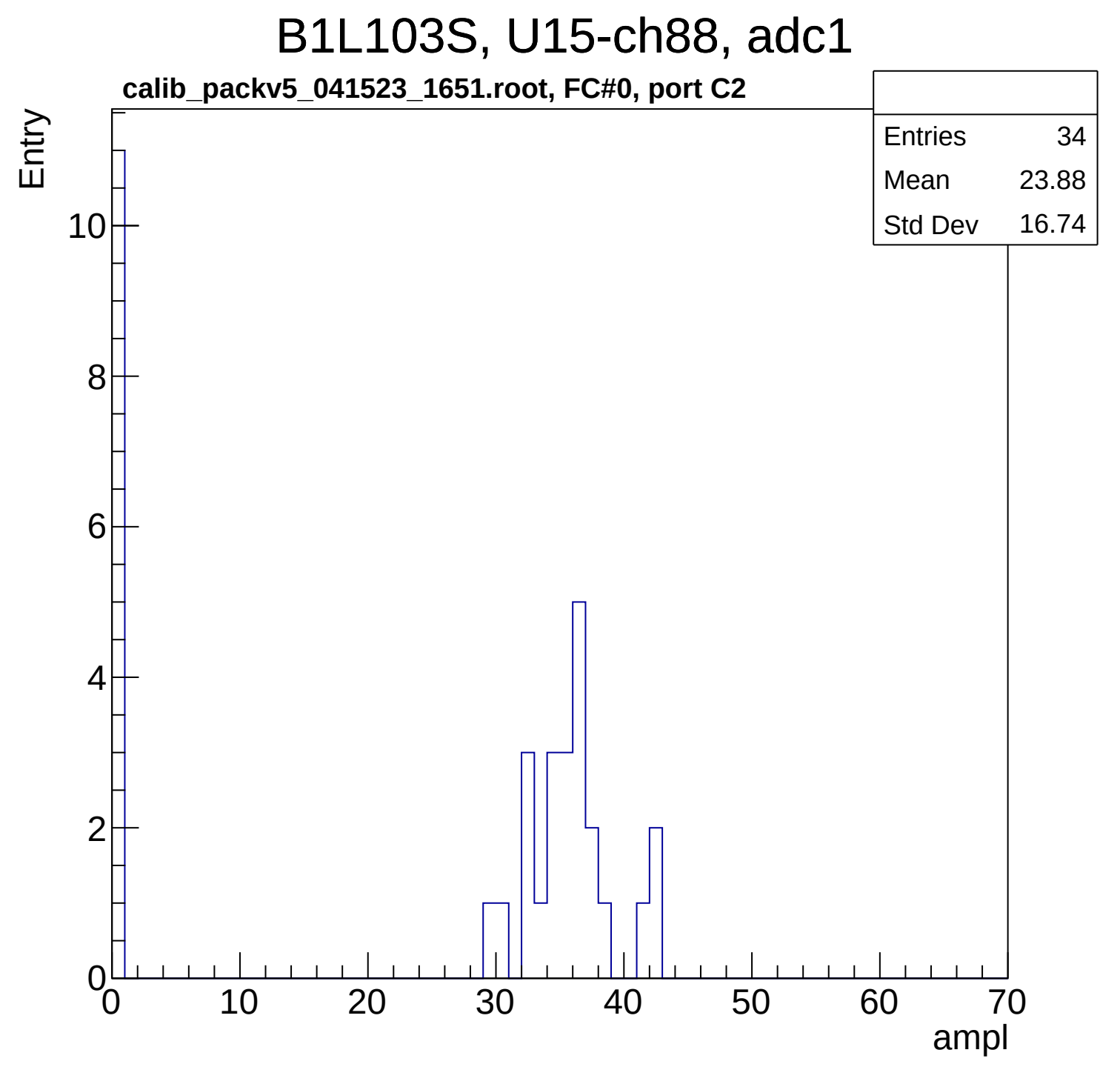

B1L103S, U15-ch87, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 55.21
Std Dev 3.242
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

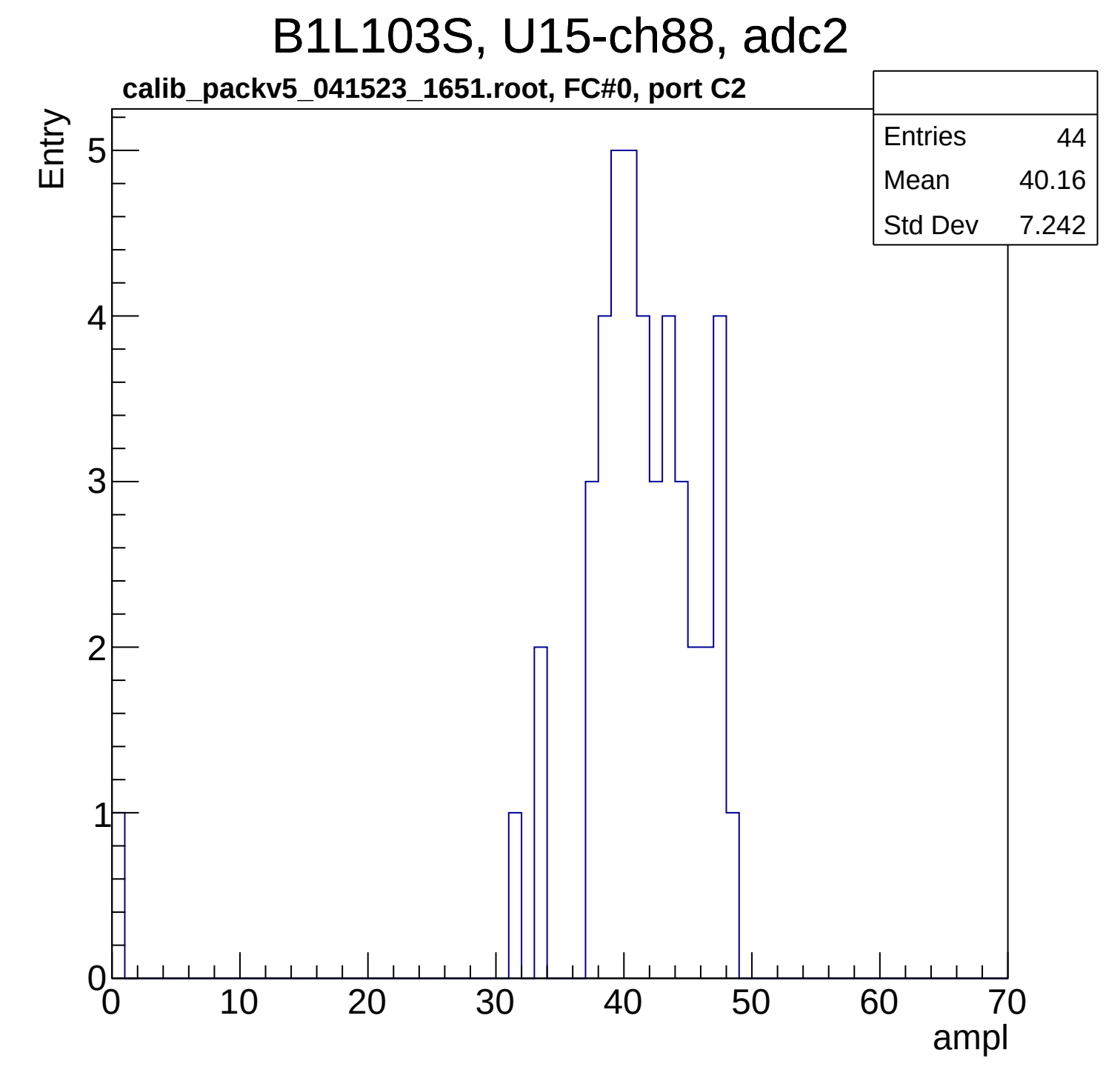

B1L103S, U15-ch87, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 60.48
Std Dev 1.68
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

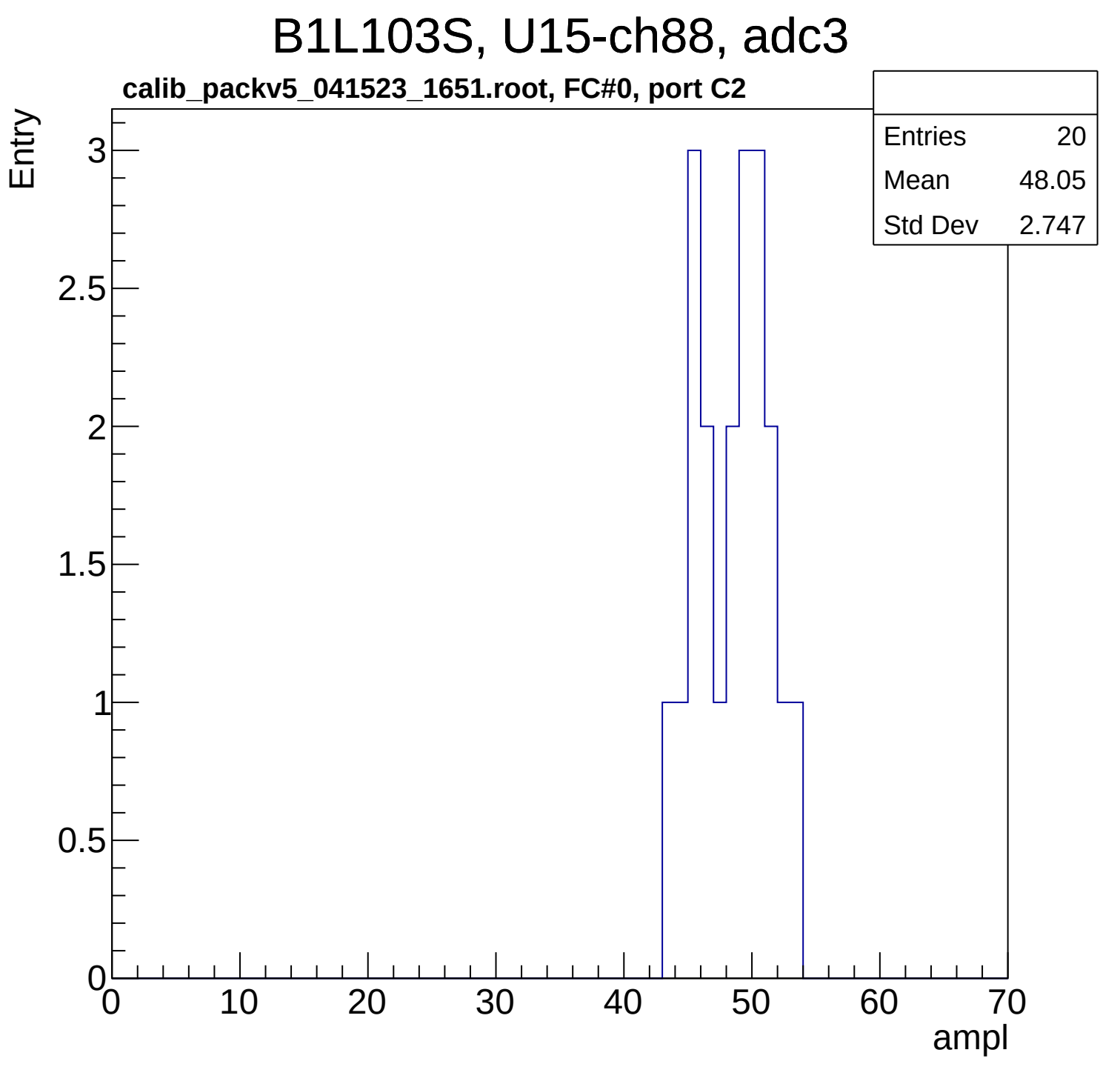

B1L103S, U15-ch87, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U15-ch87, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 0
Std Dev 0
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch88, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 22.37
Std Dev 12.15
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch88, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 23.88
Std Dev 16.74
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch88, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 40.16
Std Dev 7.242
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch88, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 48.05
Std Dev 2.747
Entry
ampl
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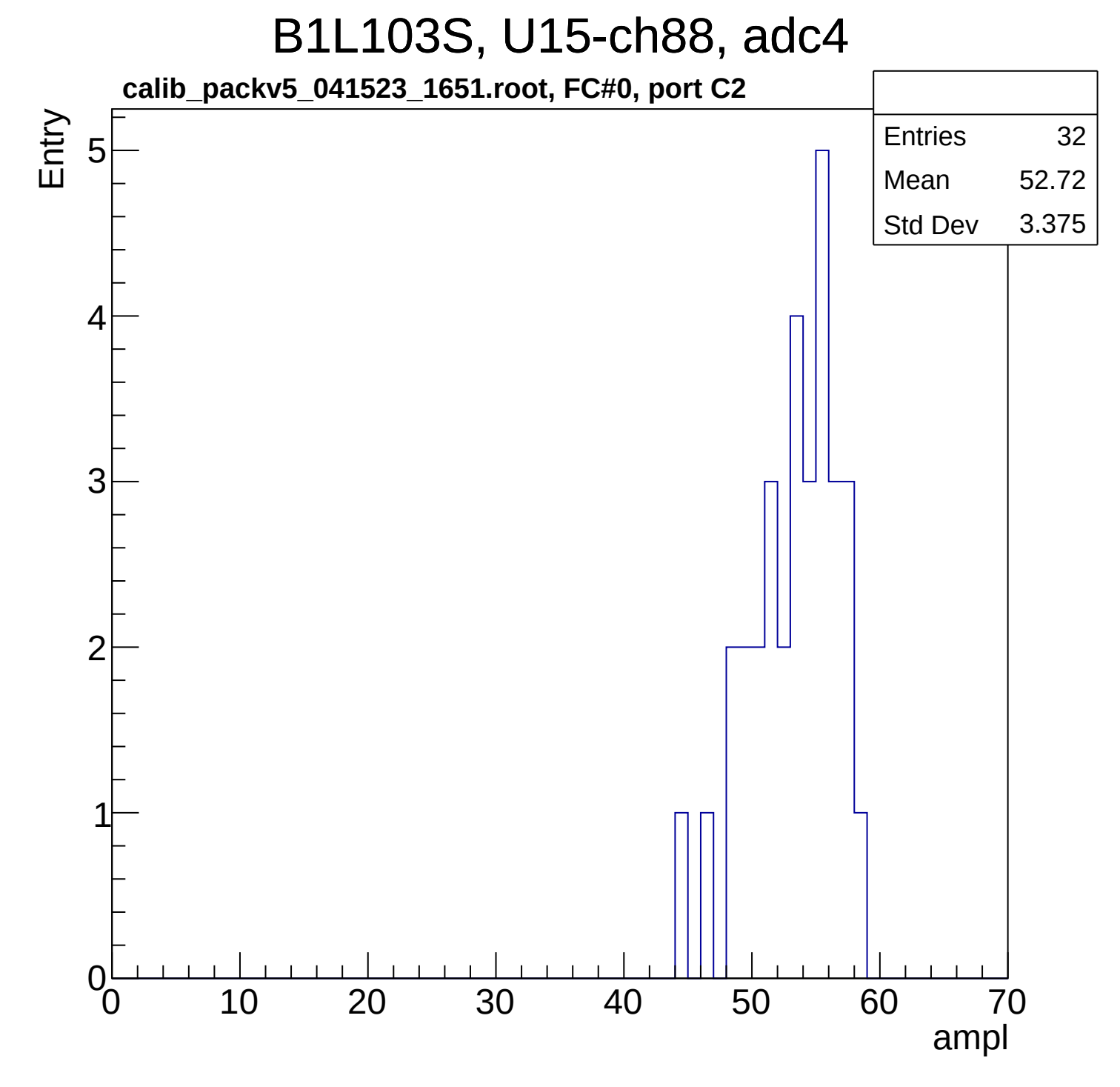
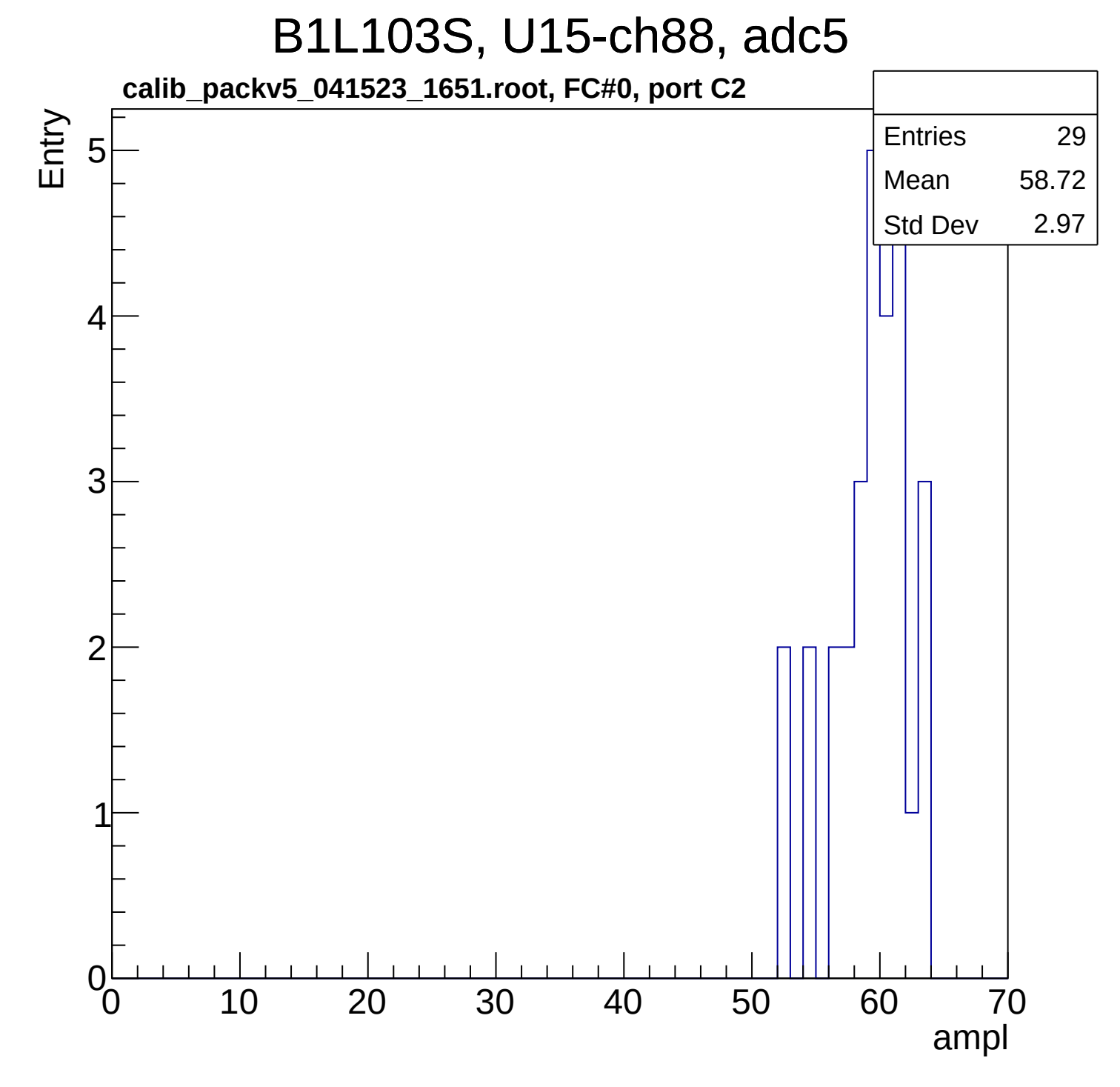
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch88, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 52.72
Std Dev 3.375
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch88, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 58.72
Std Dev 2.97
Entry
ampl
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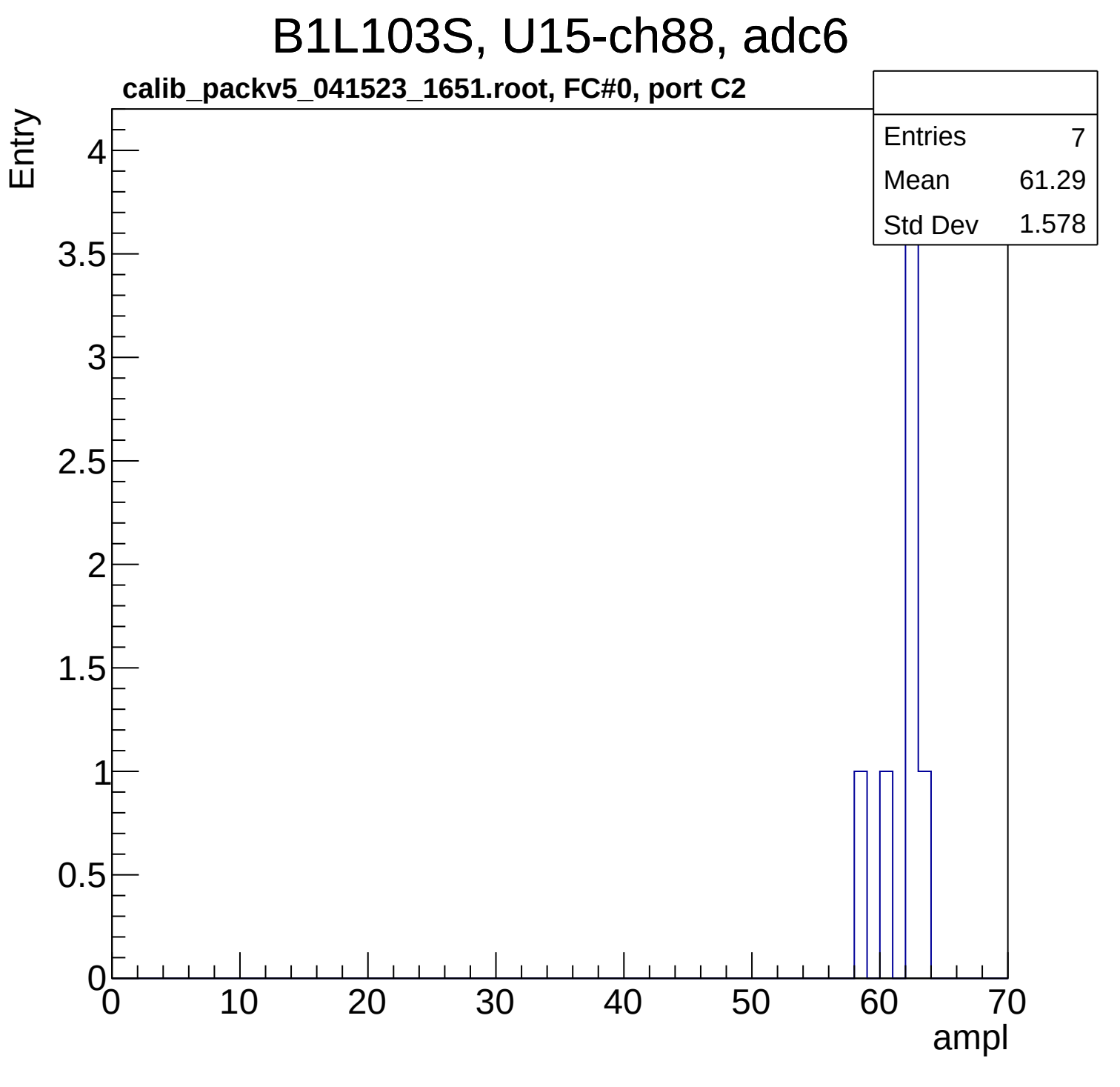
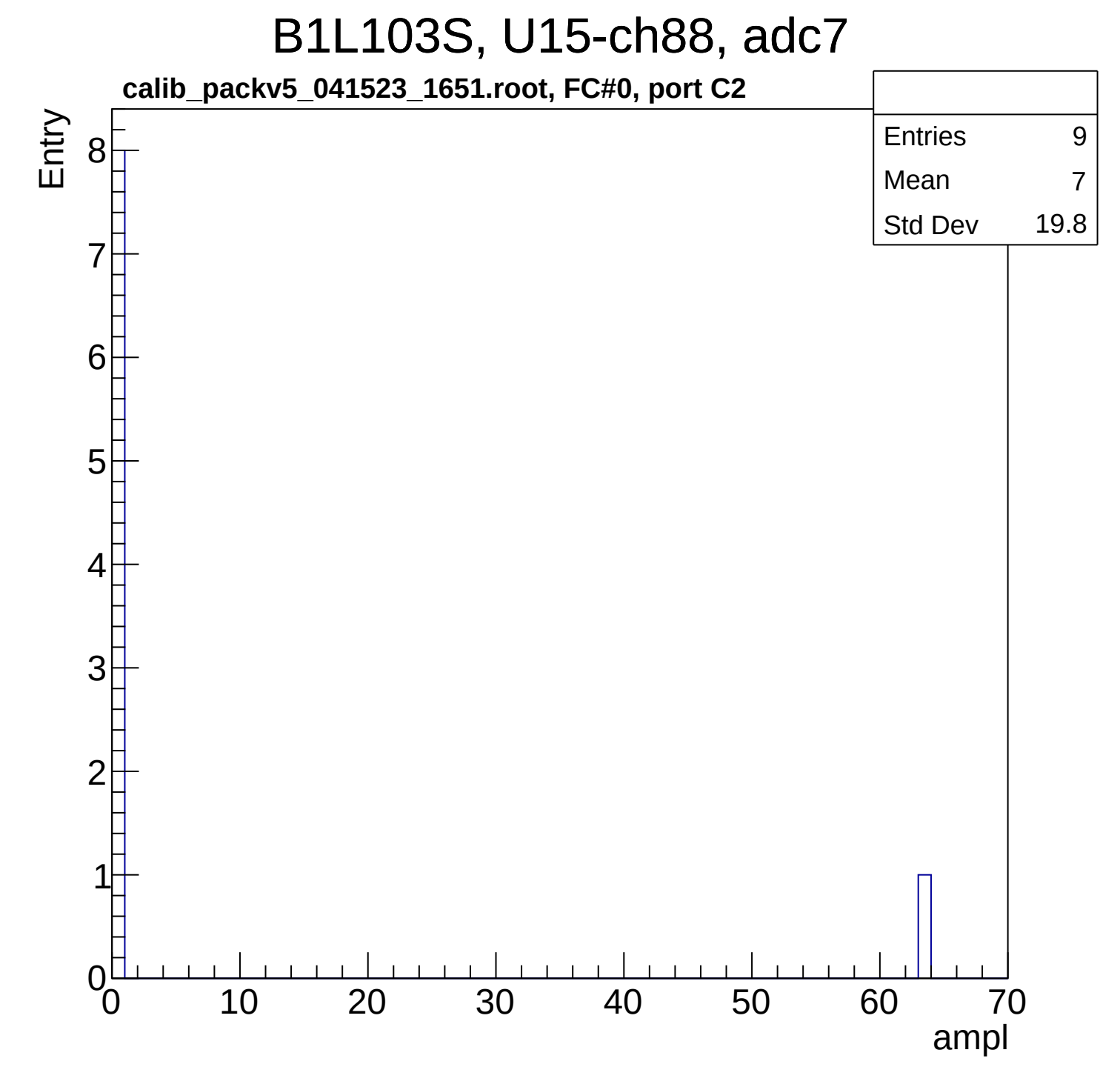
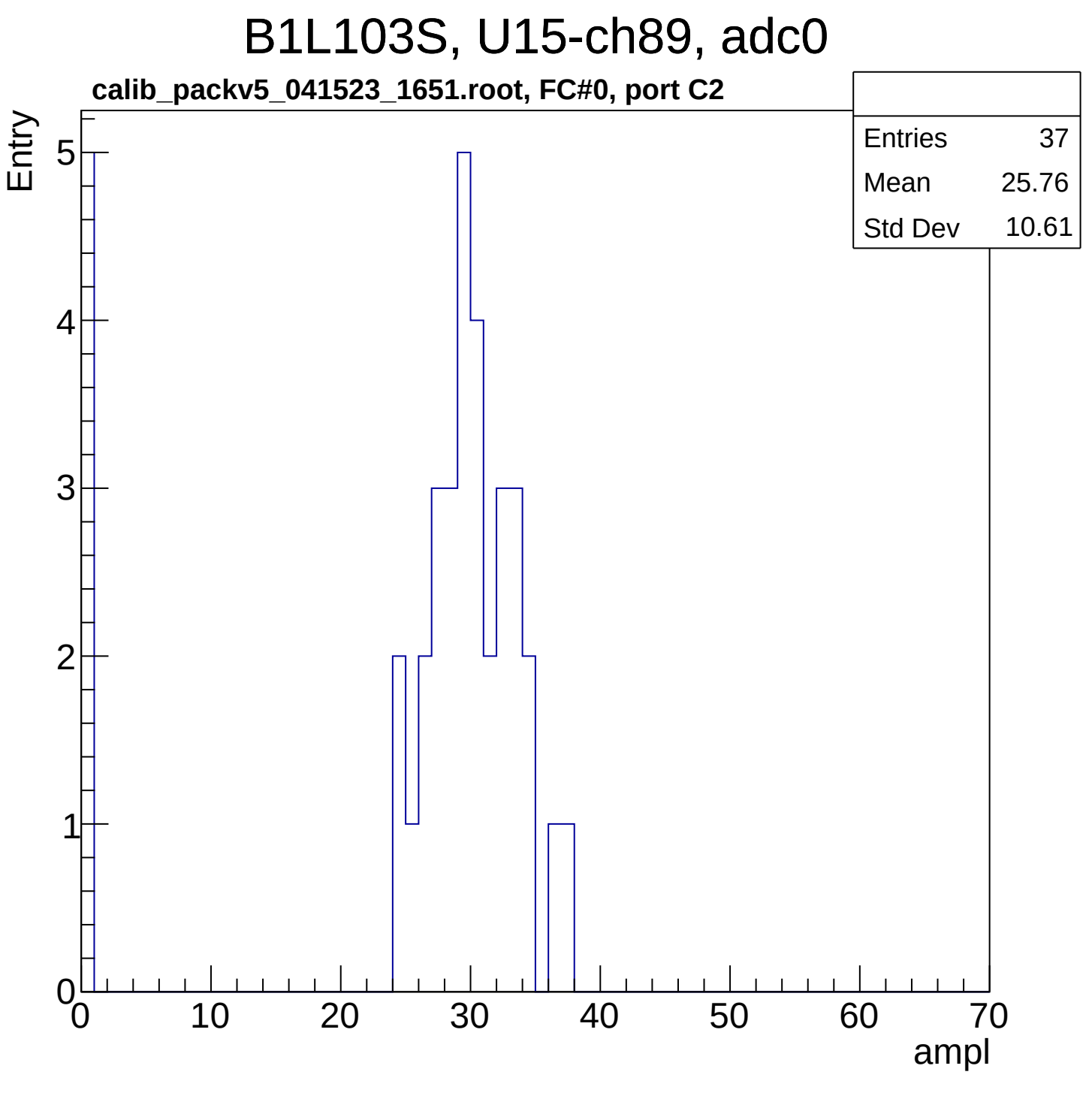
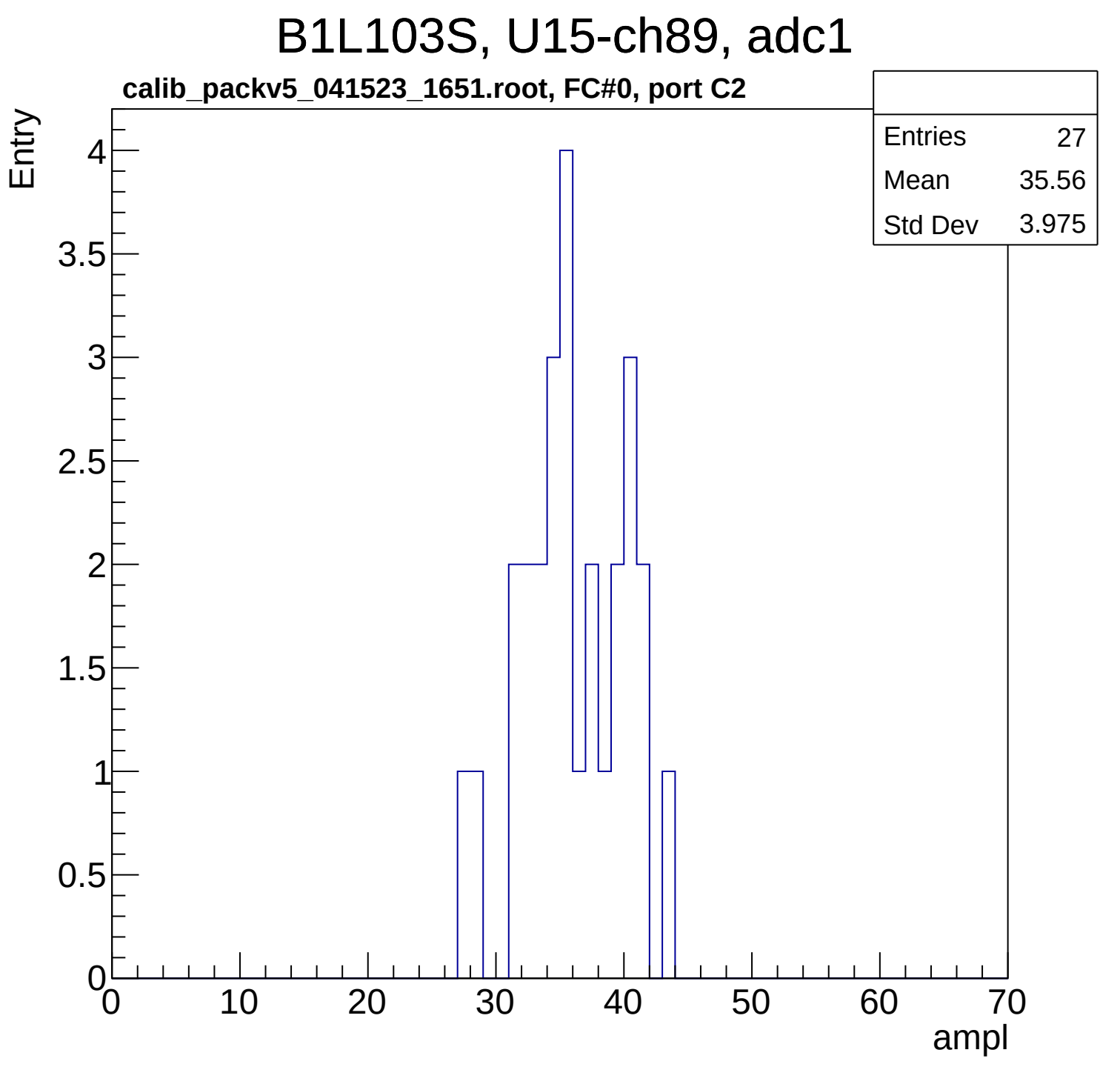
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch88, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.29
Std Dev 1.578
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch88, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 7
Std Dev 19.8
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch89, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 25.76
Std Dev 10.61
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch89, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 35.56
Std Dev 3.975
Entry
ampl
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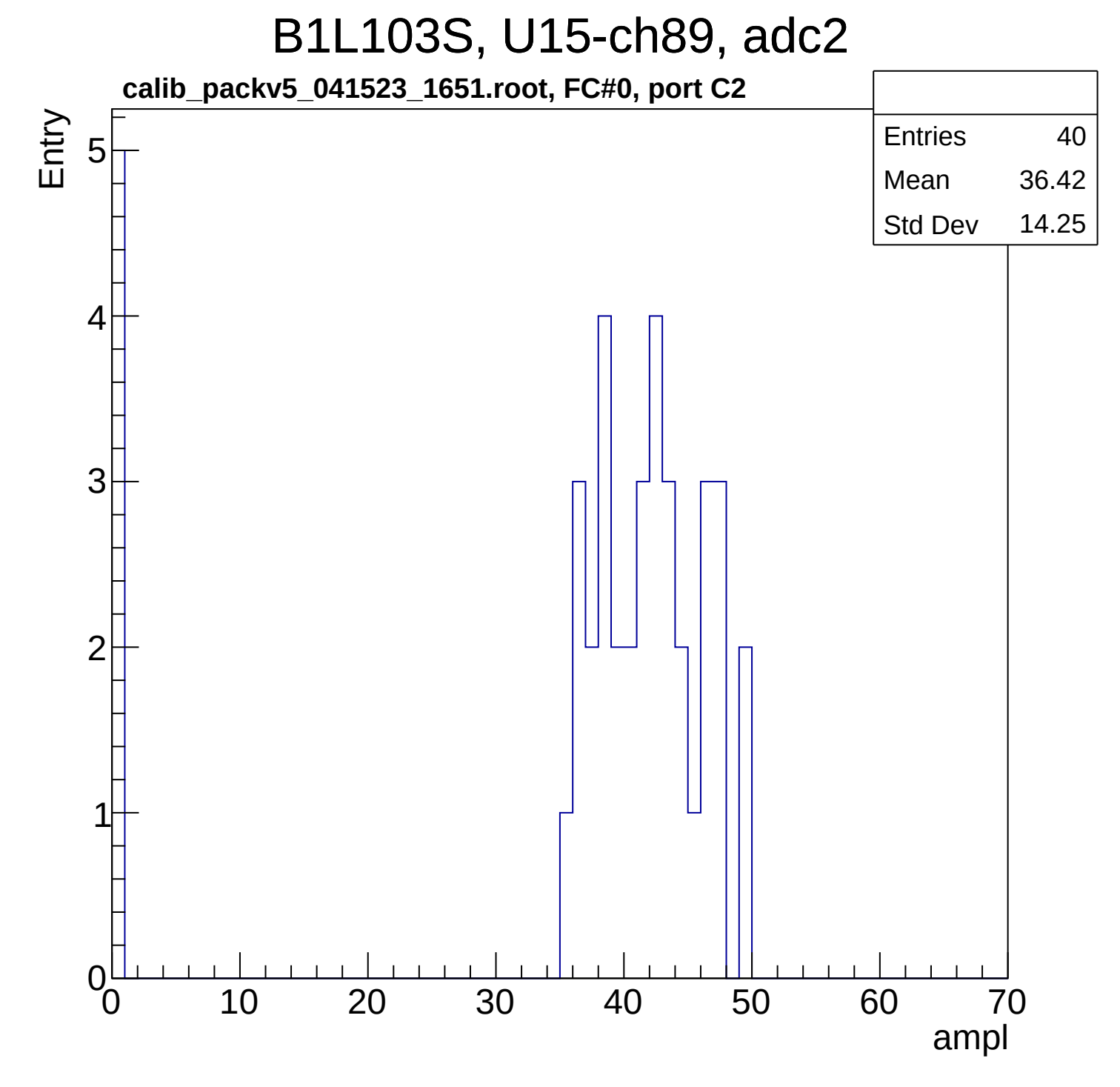
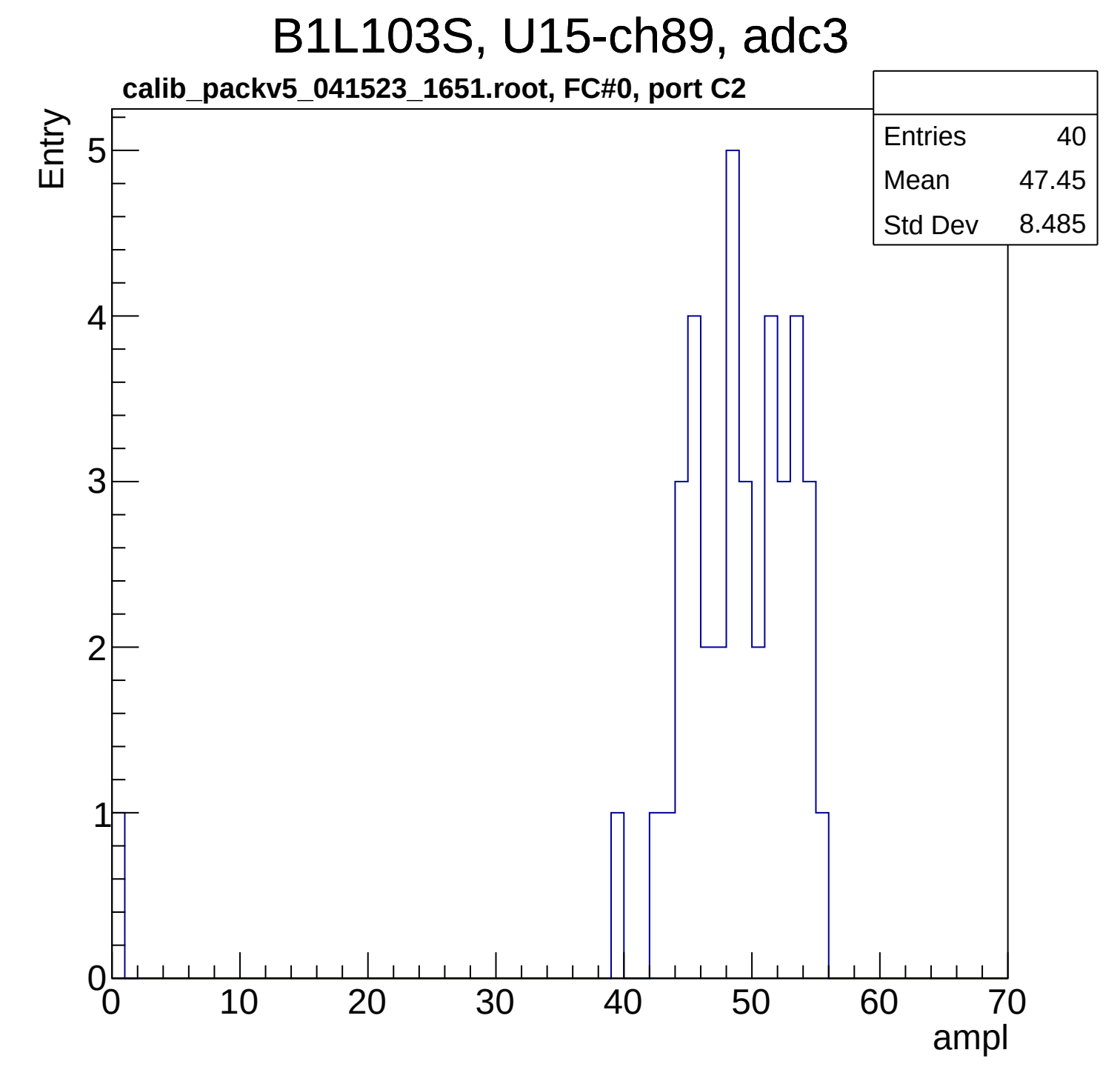
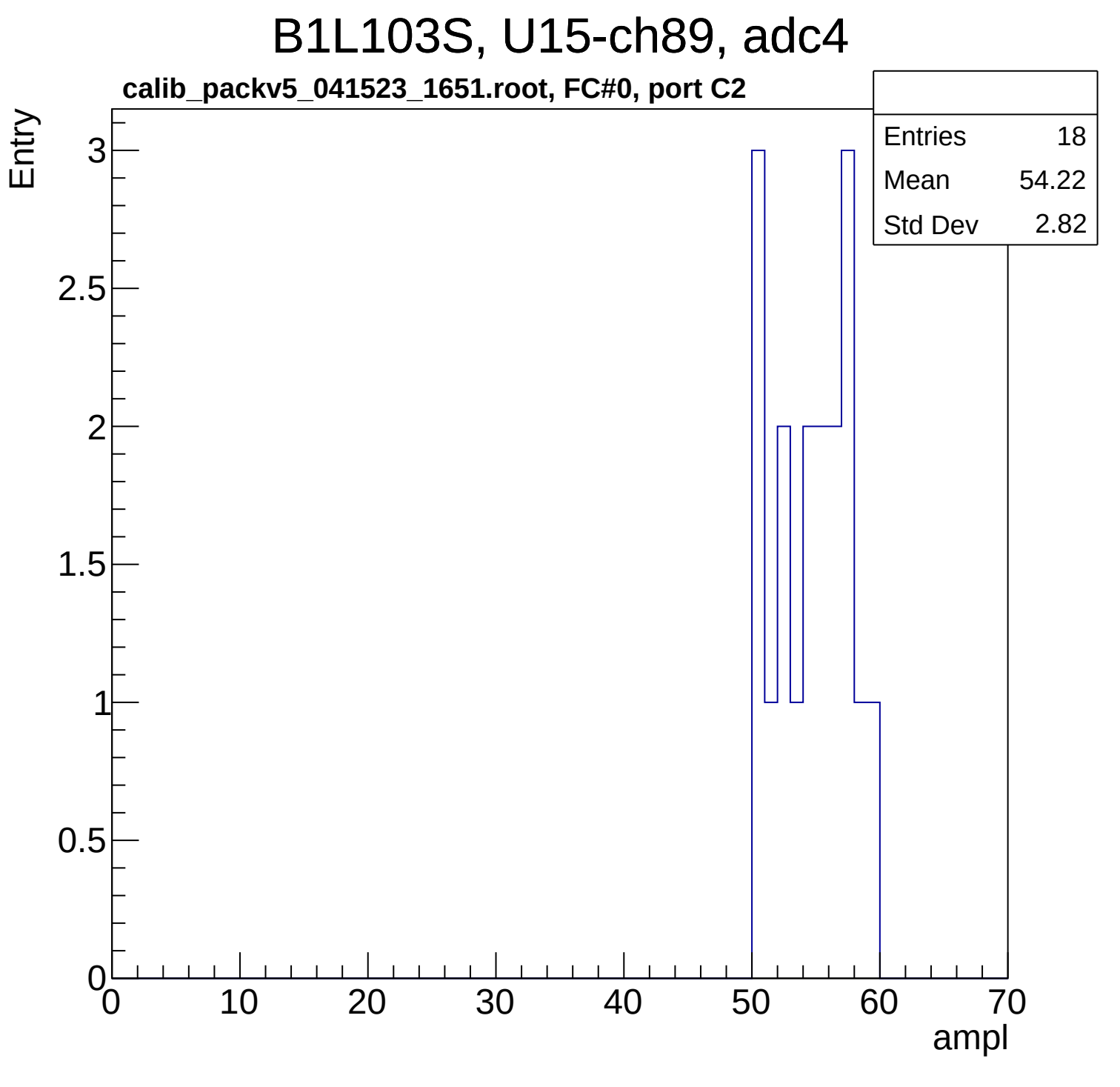
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch89, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 36.42
Std Dev 14.25
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch89, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 47.45
Std Dev 8.485
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch89, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 54.22
Std Dev 2.82
Entry
ampl
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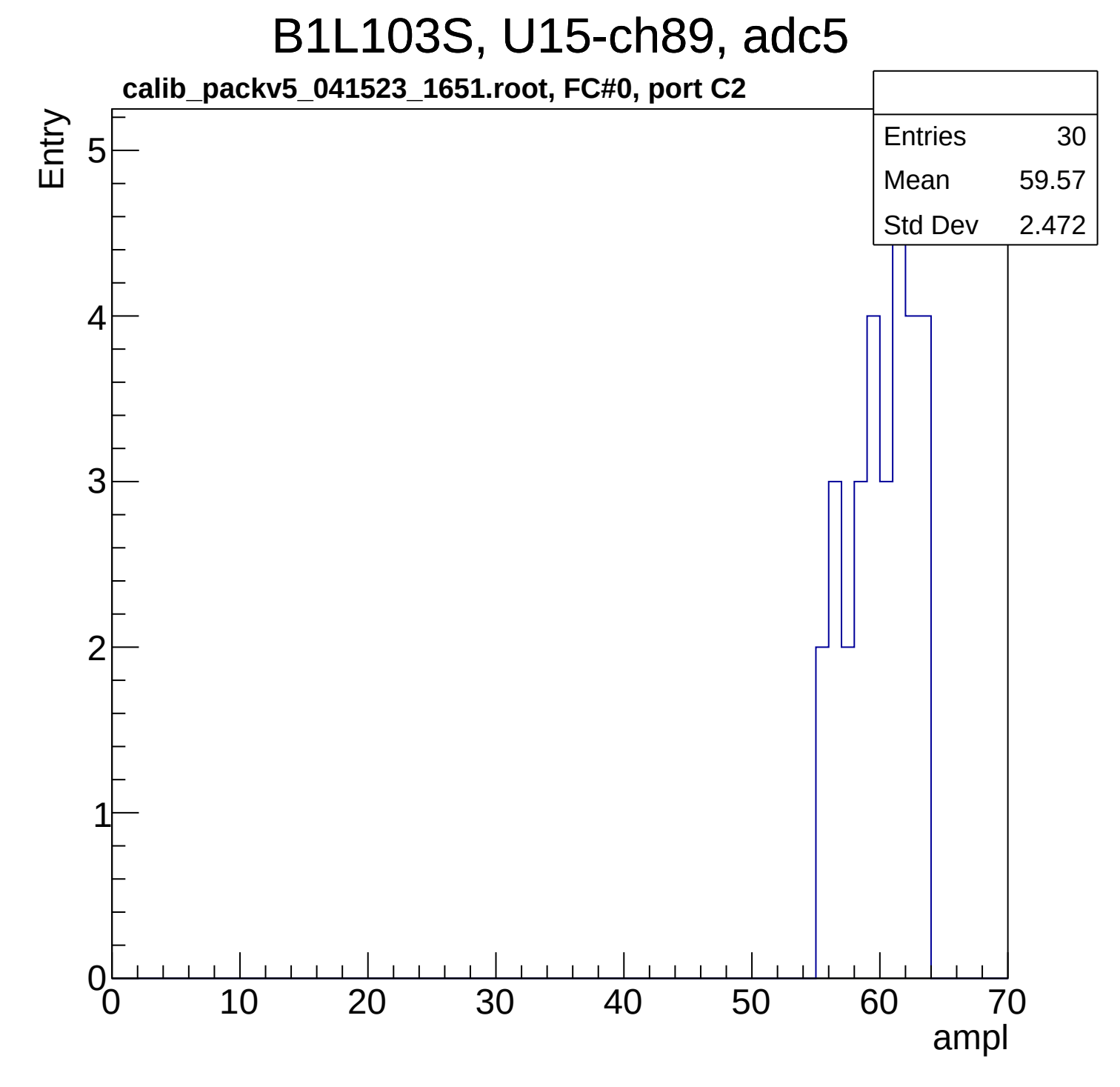
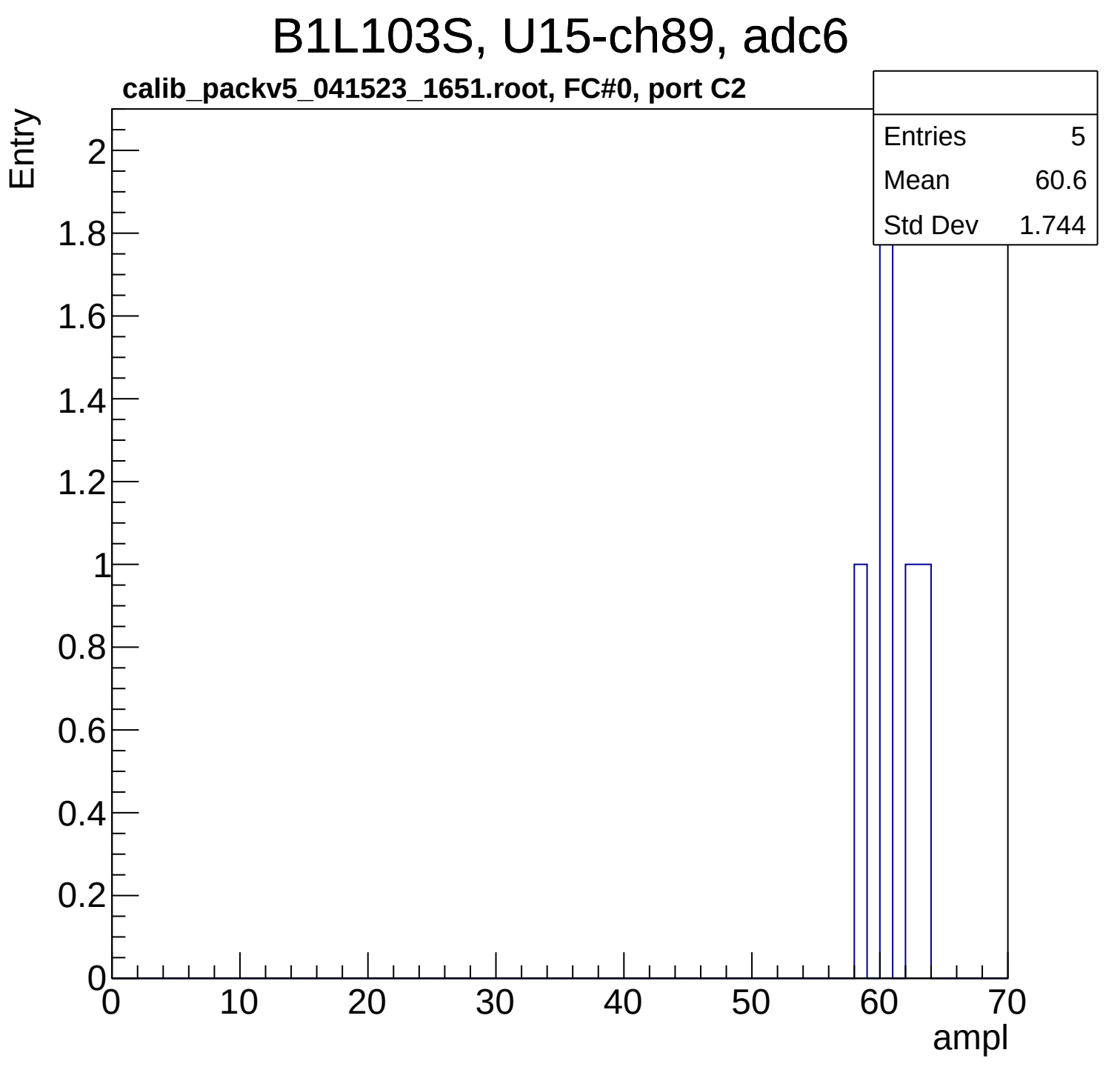
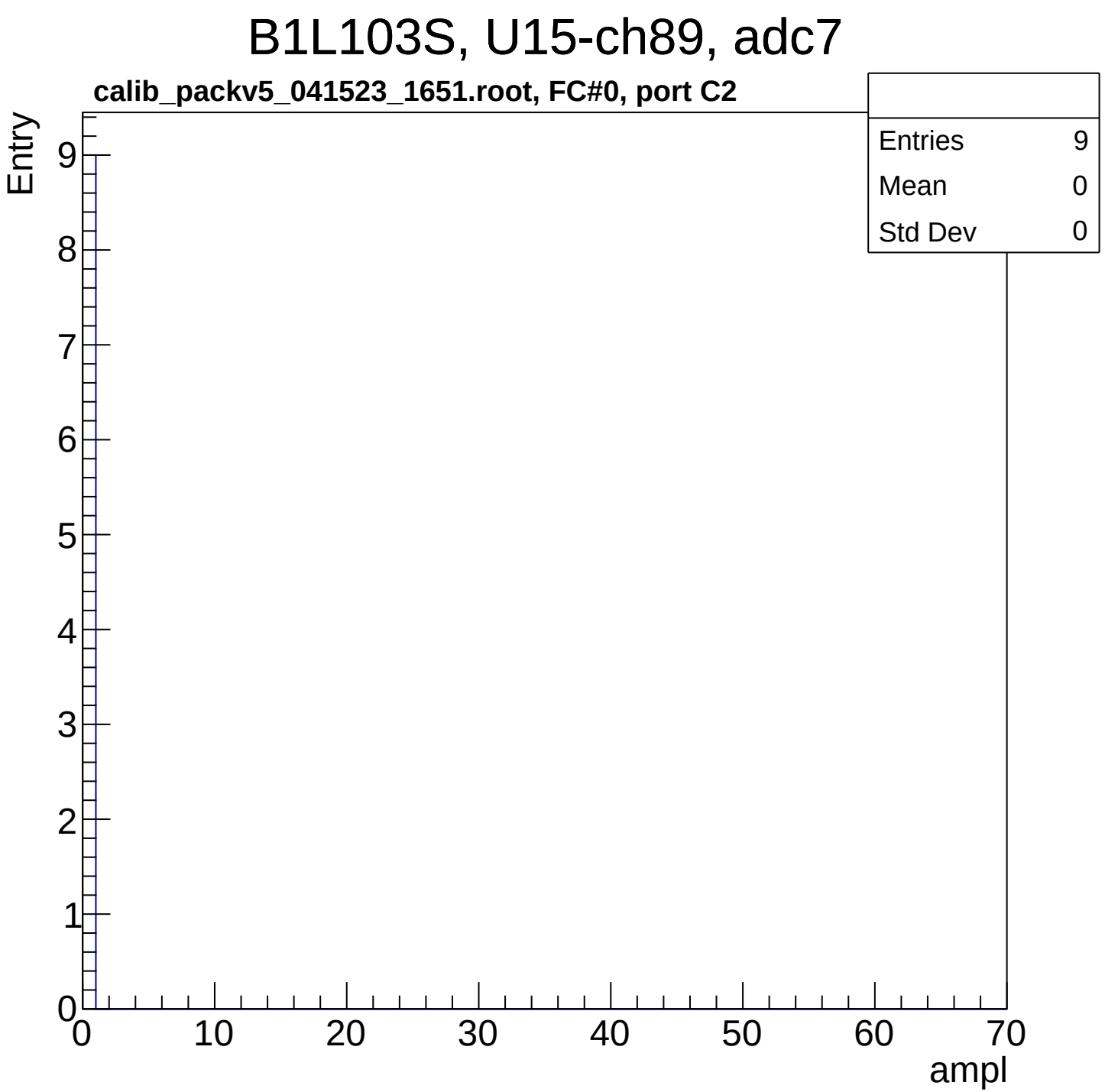
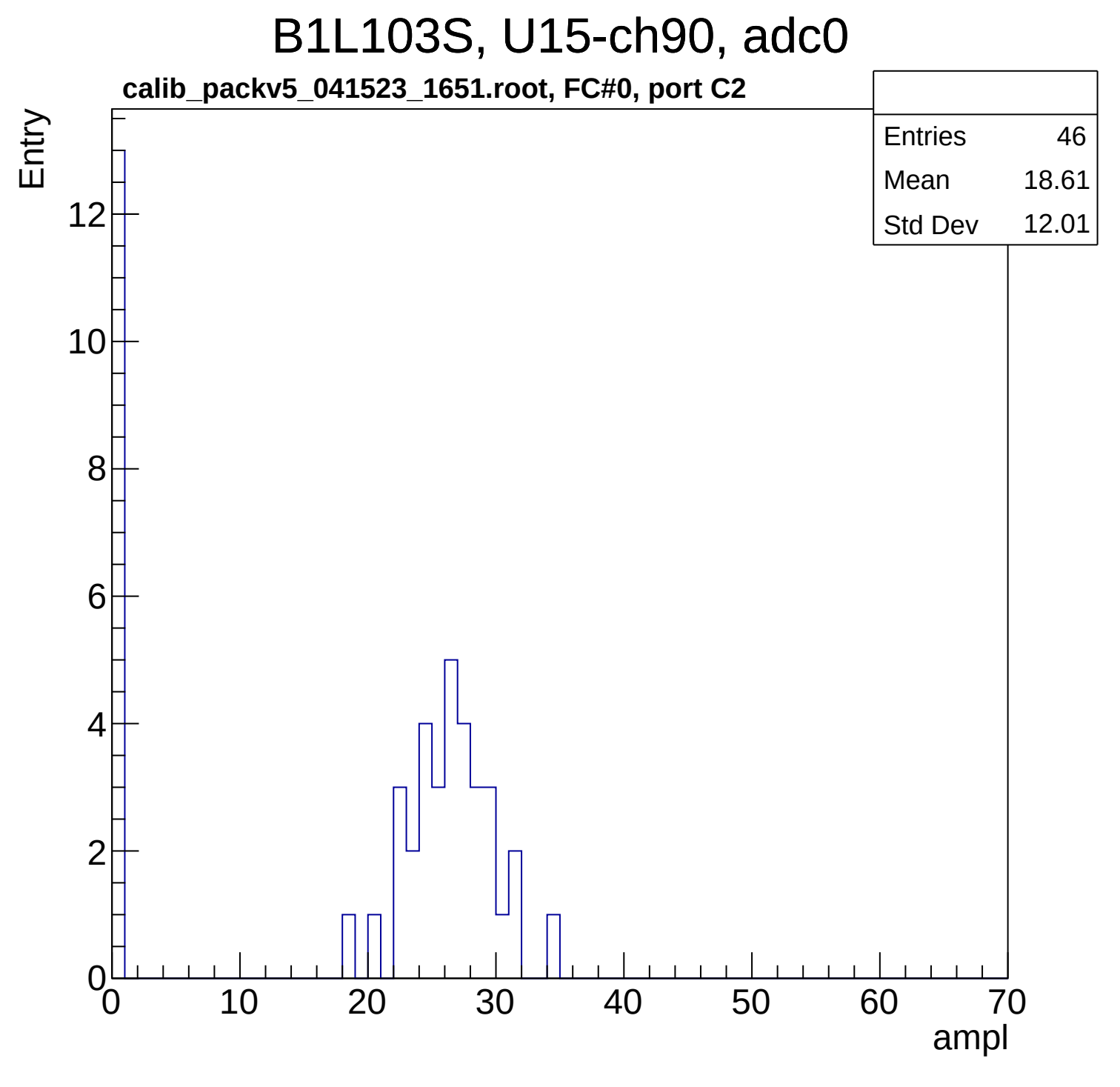
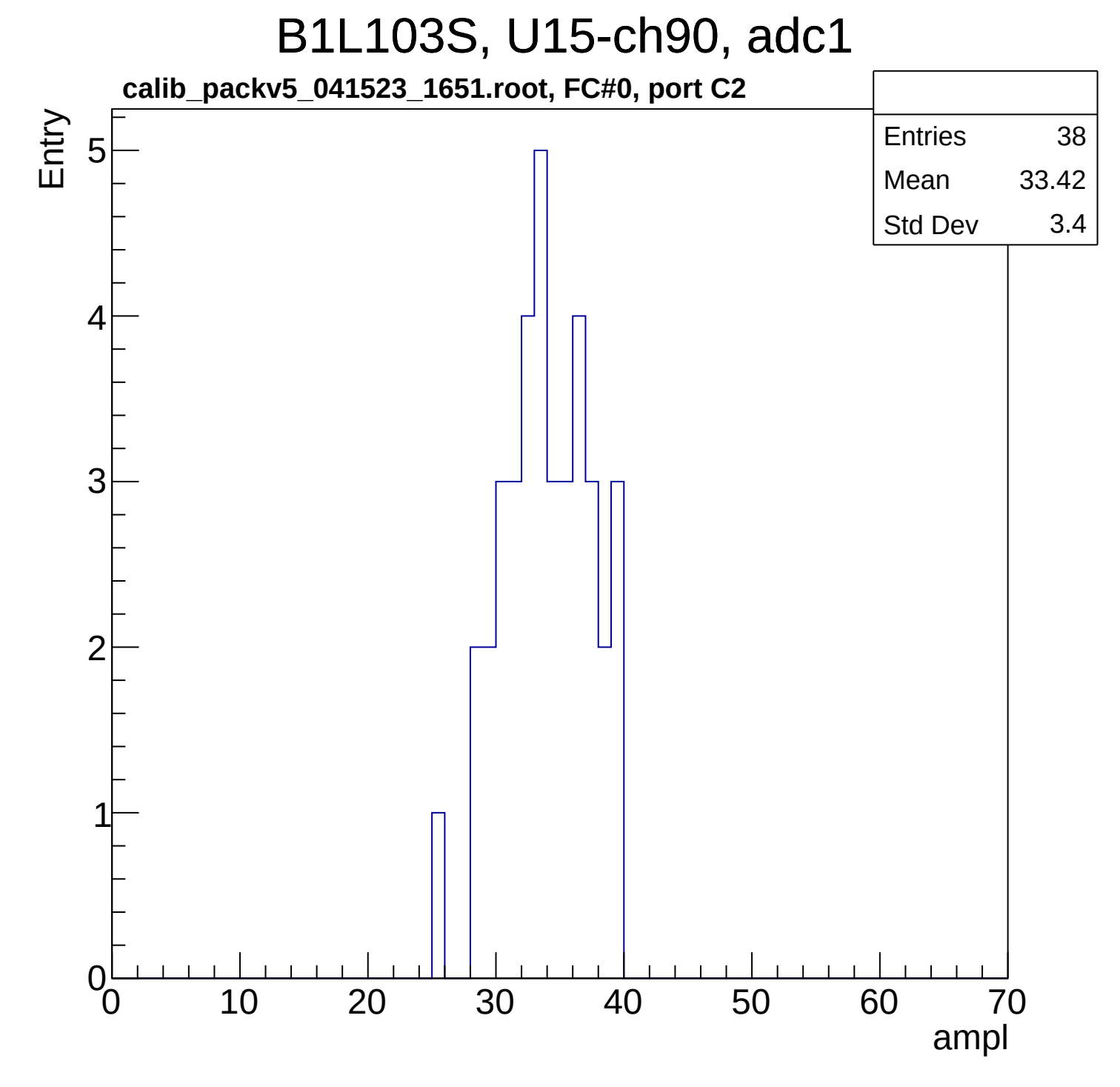
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

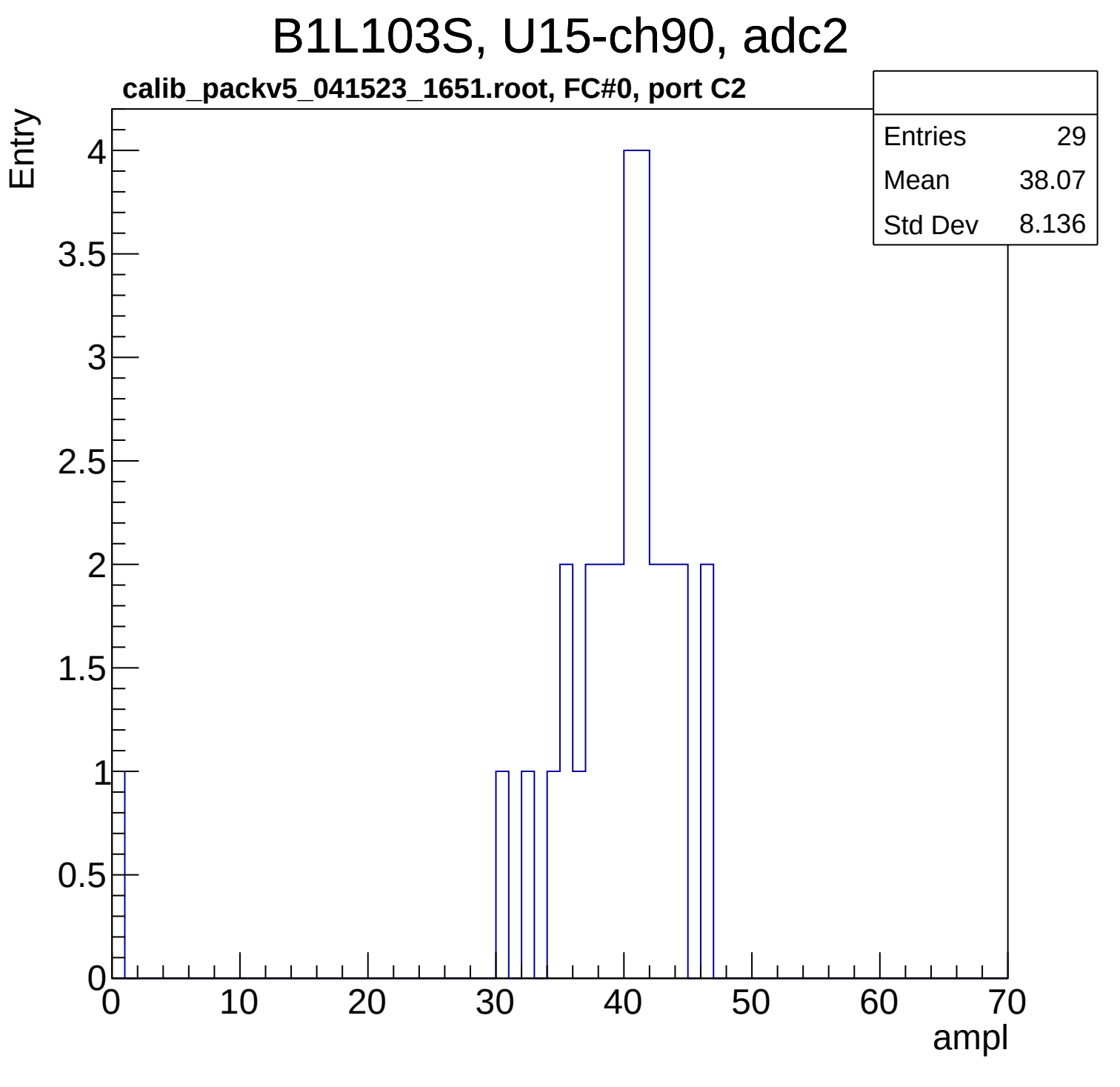

B1L103S, U15-ch89, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 59.57
Std Dev 2.472
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch89, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 60.6
Std Dev 1.744
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U15-ch89, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 0
Std Dev 0
Entry
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch90, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 18.61
Std Dev 12.01
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch90, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 33.42
Std Dev 3.4
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch90, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 38.07
Std Dev 8.136
Entry
ampl
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1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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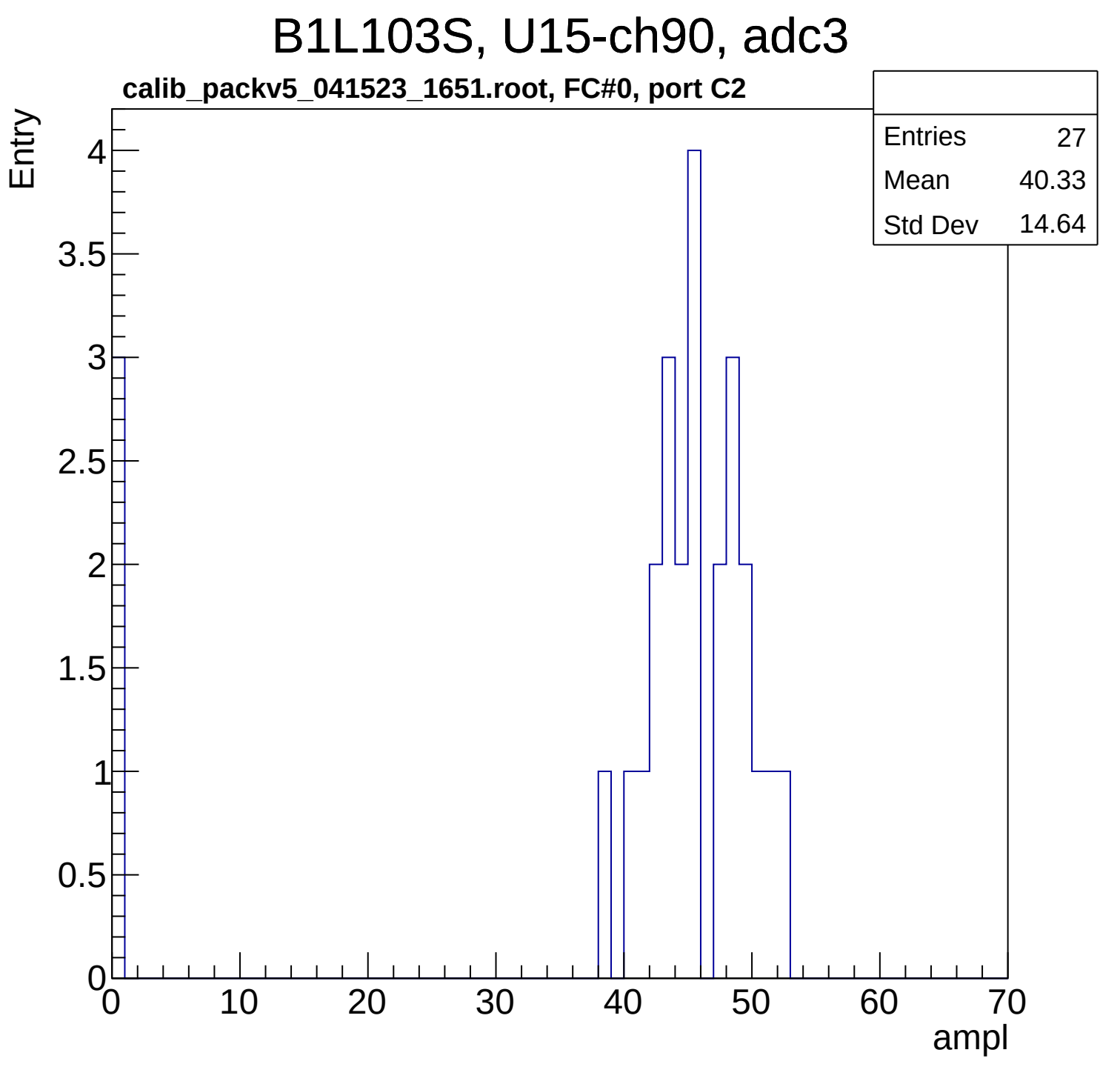
B1L103S, U15-ch90, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 40.33
Std Dev 14.64
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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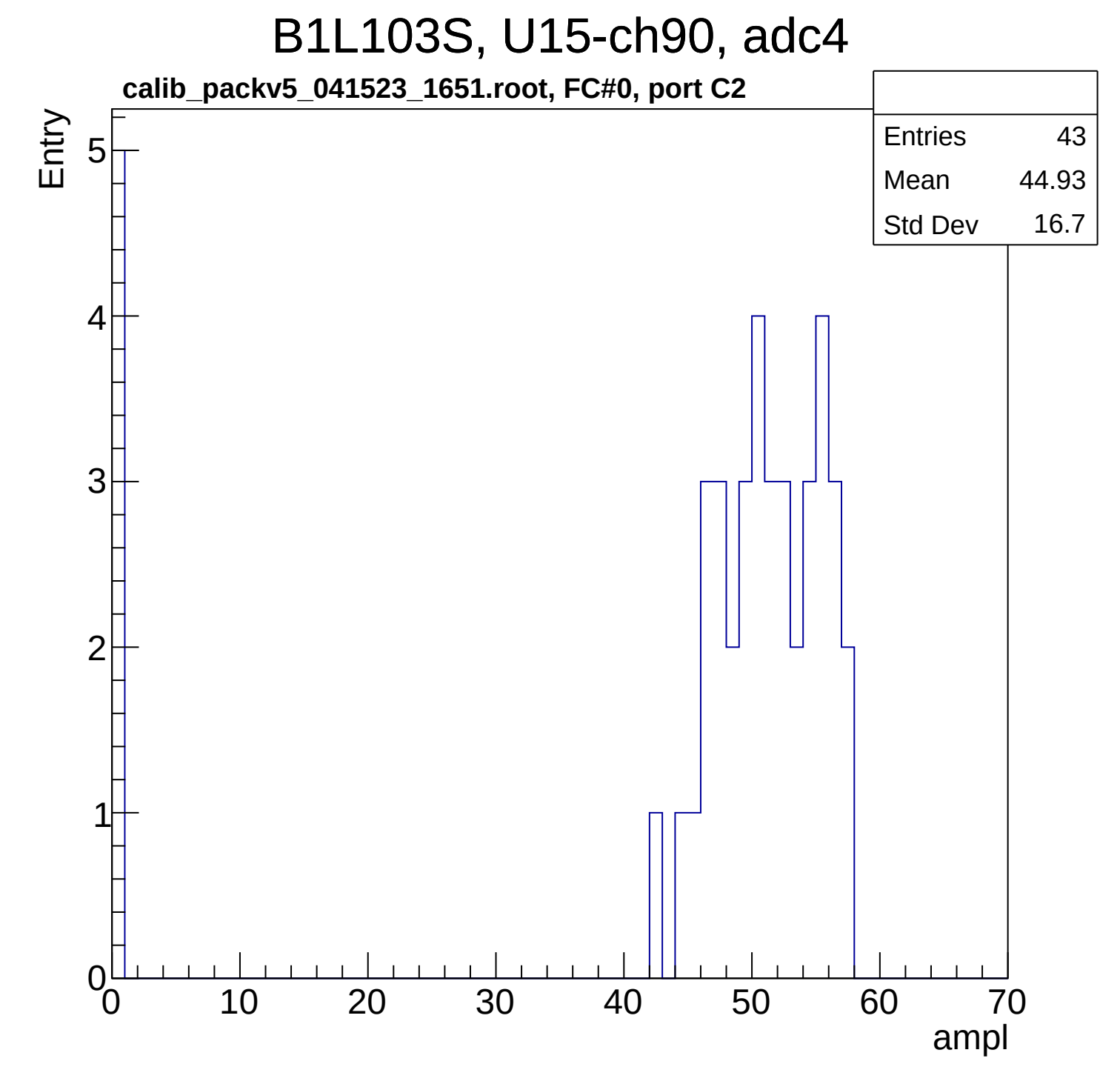
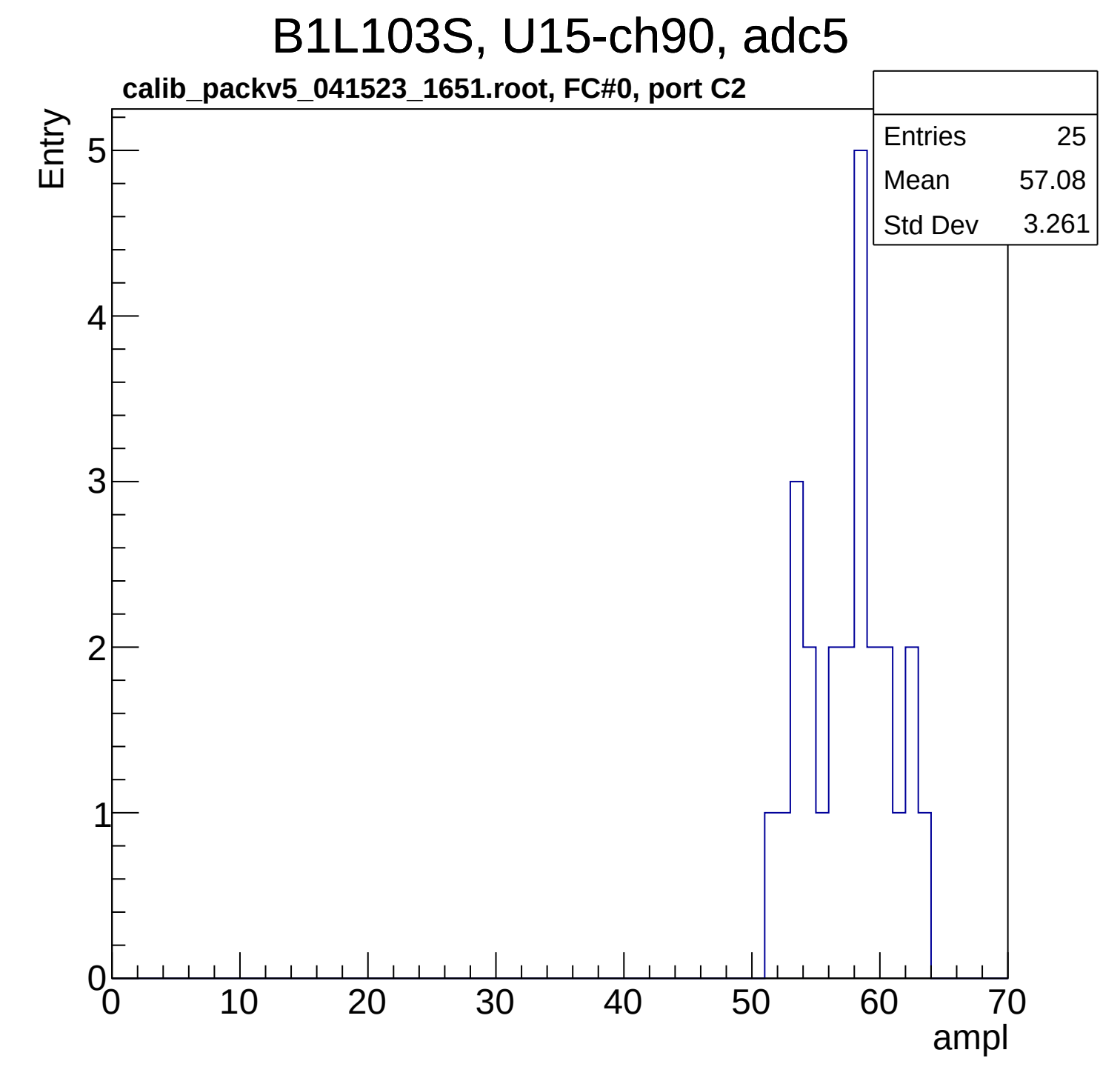
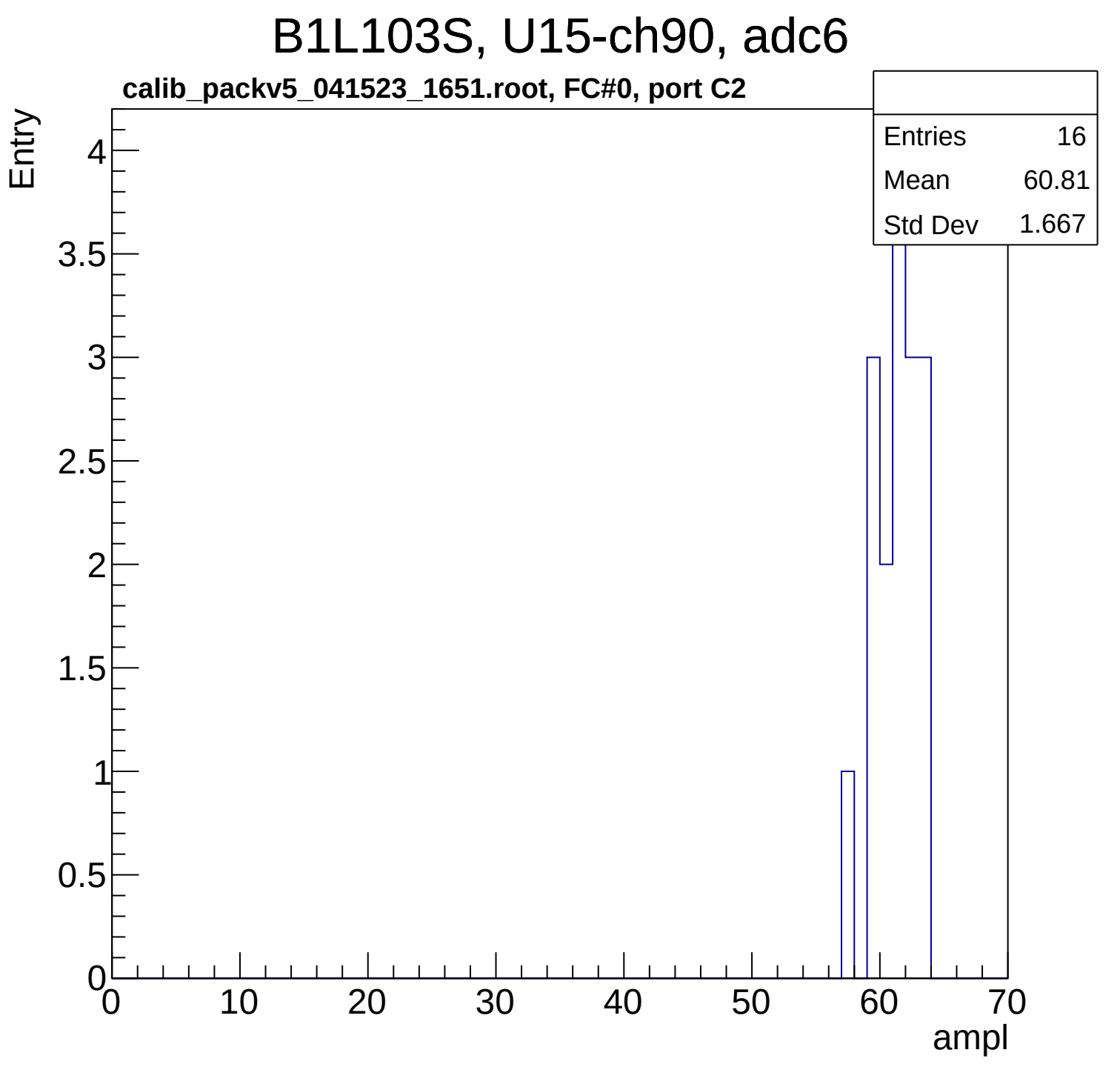
40
50
60
70


B1L103S, U15-ch90, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 44.93
Std Dev 16.7
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch90, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 57.08
Std Dev 3.261
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch90, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 60.81
Std Dev 1.667
Entry
ampl
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0.5
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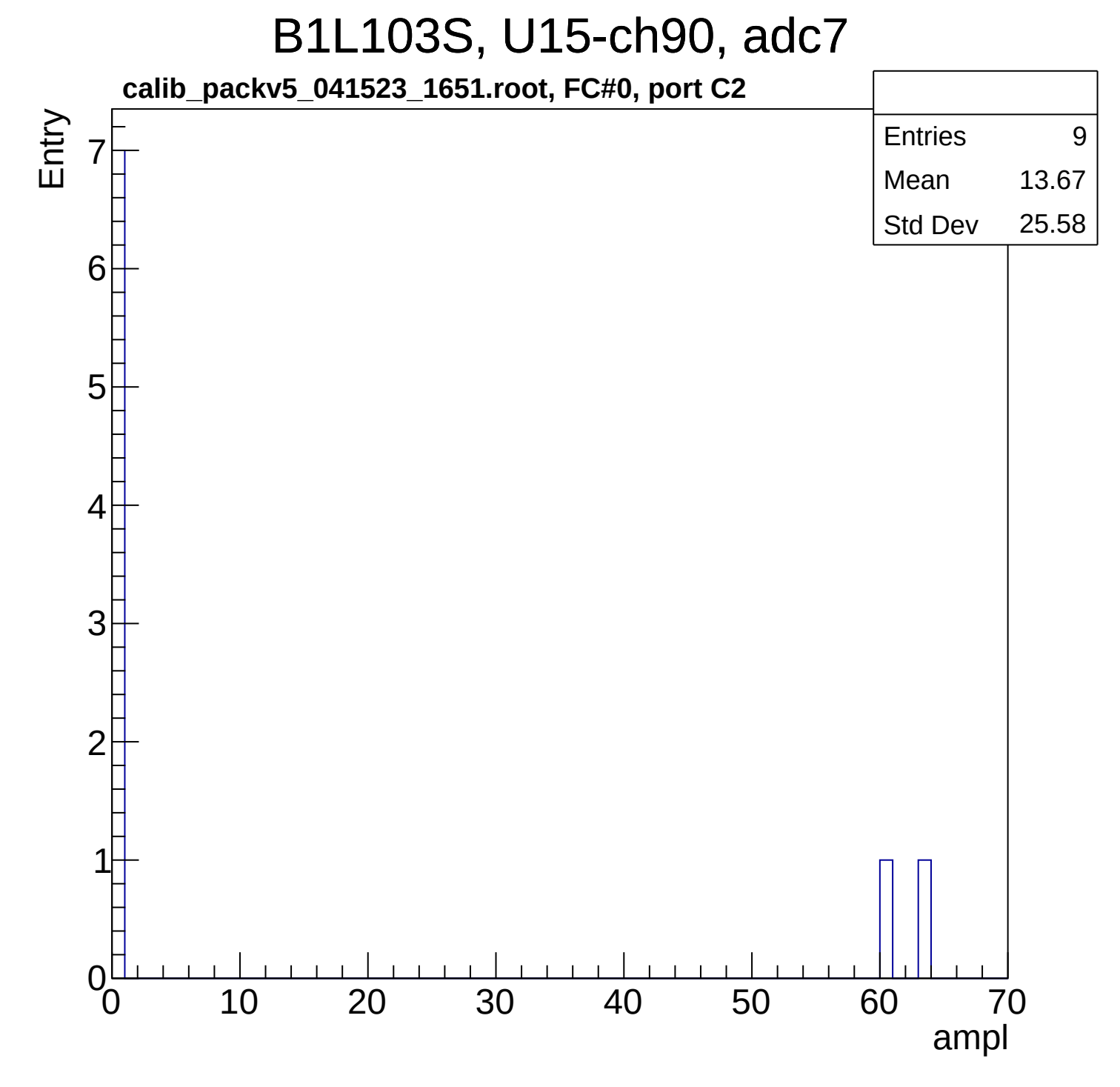
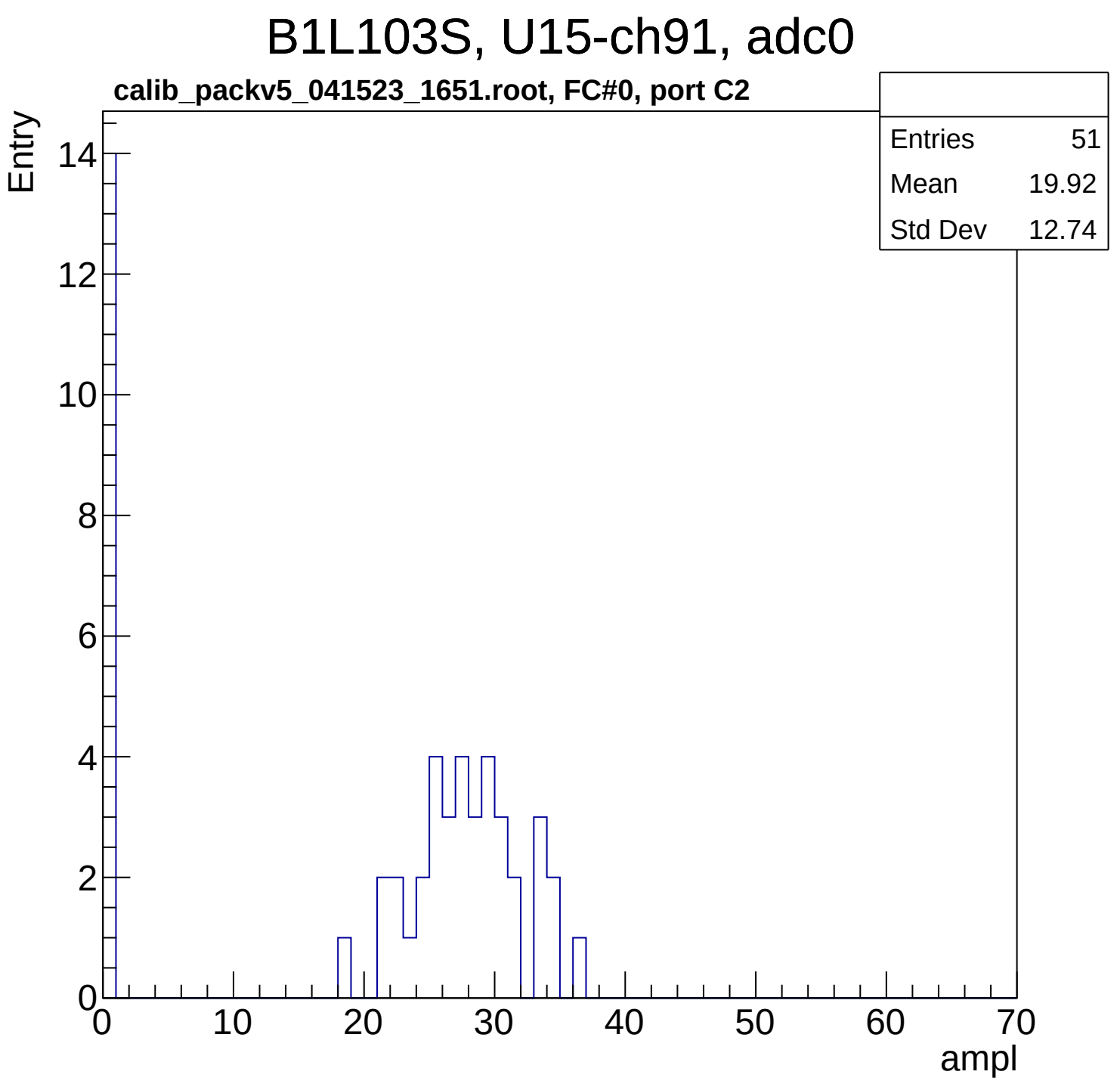
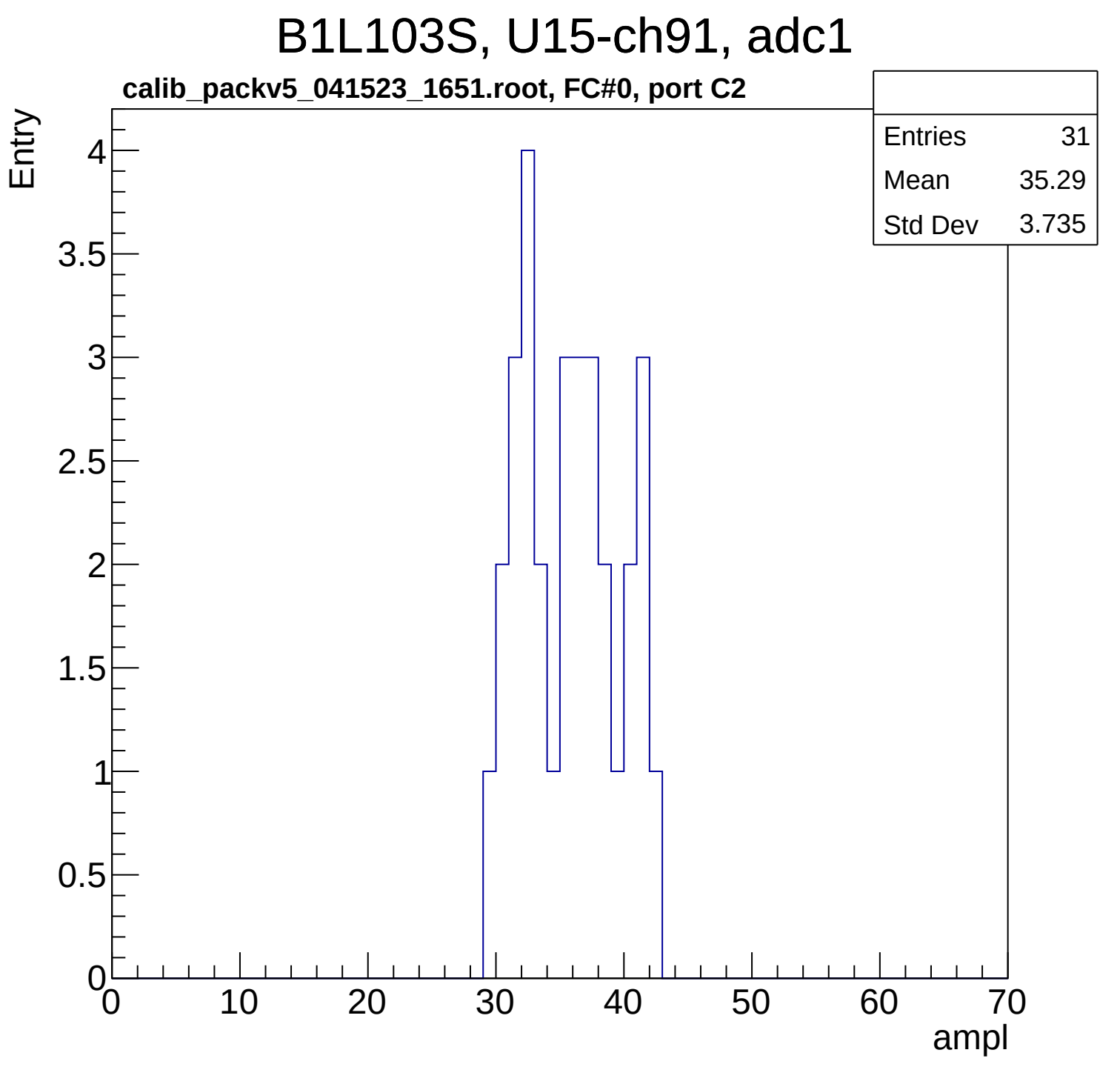
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch90, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 13.67
Std Dev 25.58
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U15-ch91, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 19.92
Std Dev 12.74
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch91, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 35.29
Std Dev 3.735
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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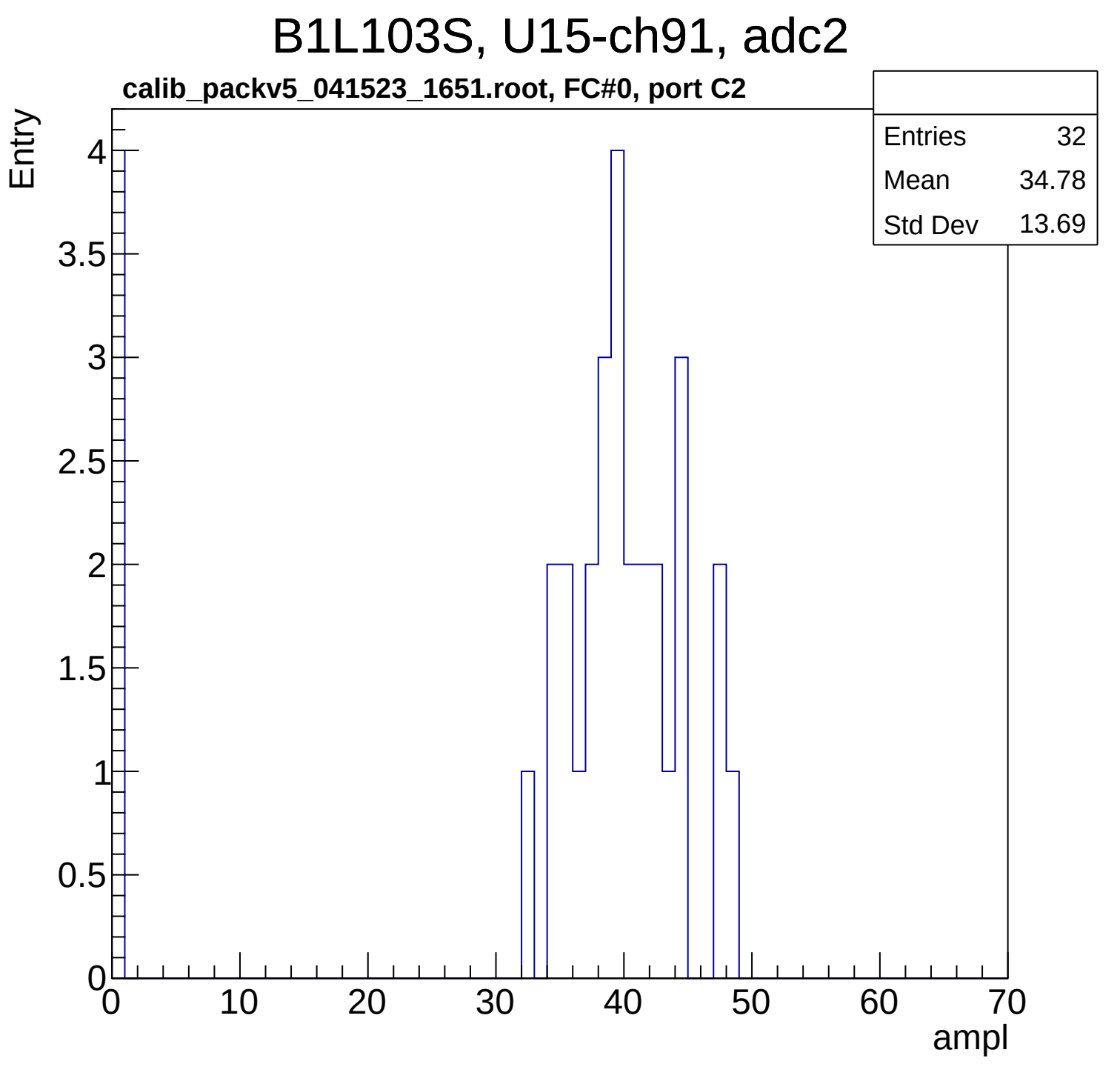
B1L103S, U15-ch91, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 34.78
Std Dev 13.69
Entry
ampl
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0.5
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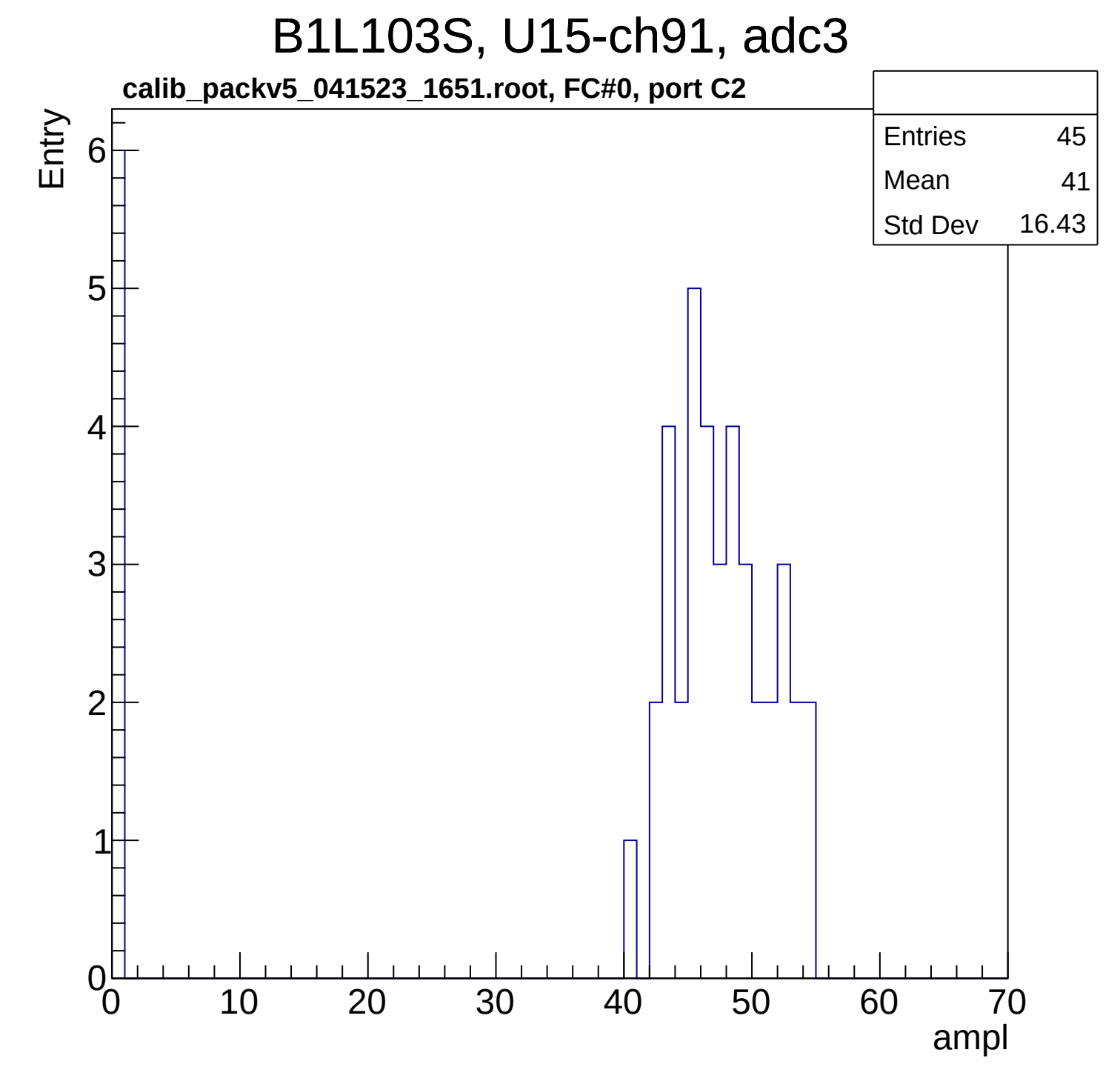
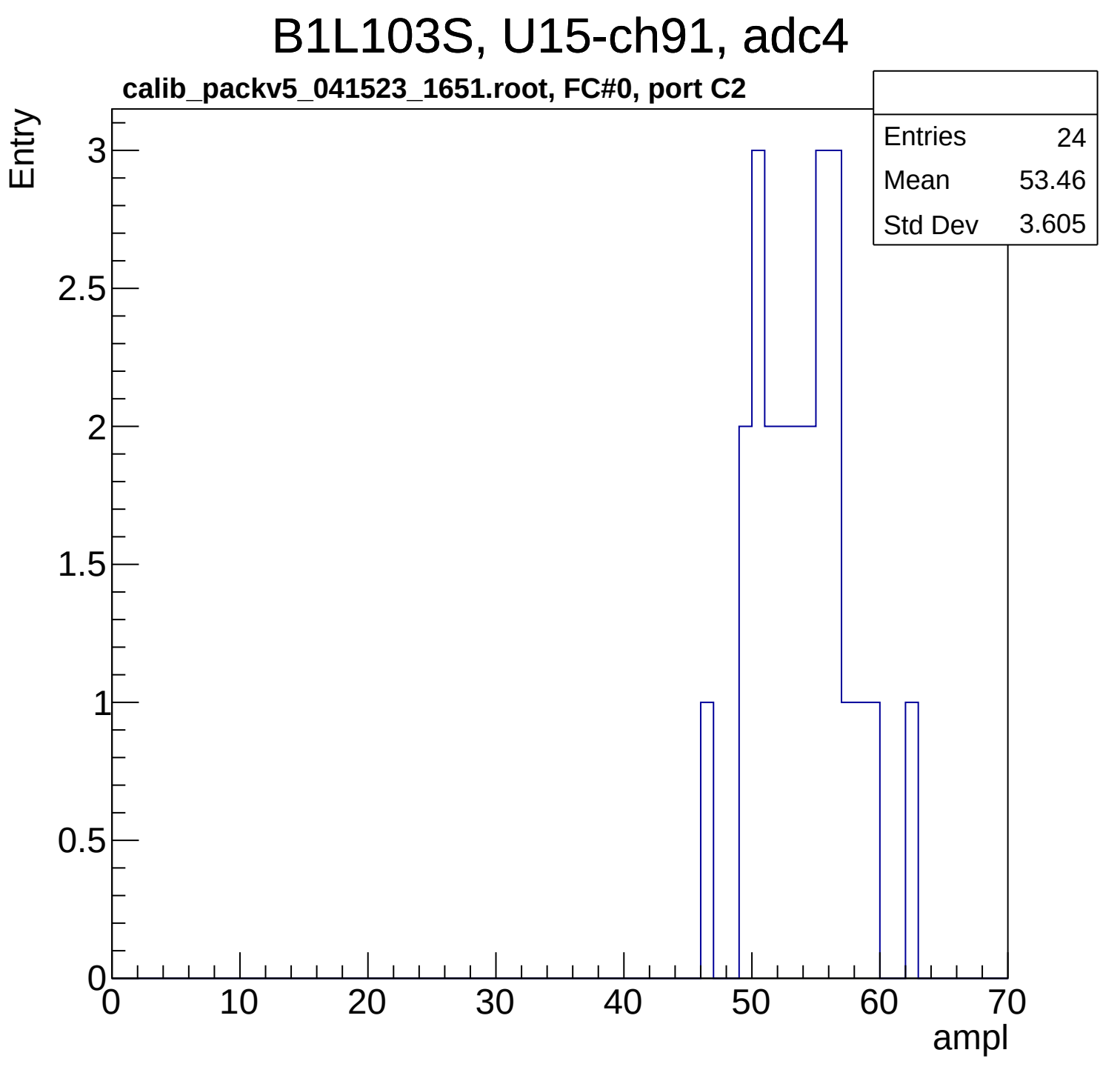
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch91, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 41
Std Dev 16.43
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U15-ch91, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 53.46
Std Dev 3.605
Entry
ampl
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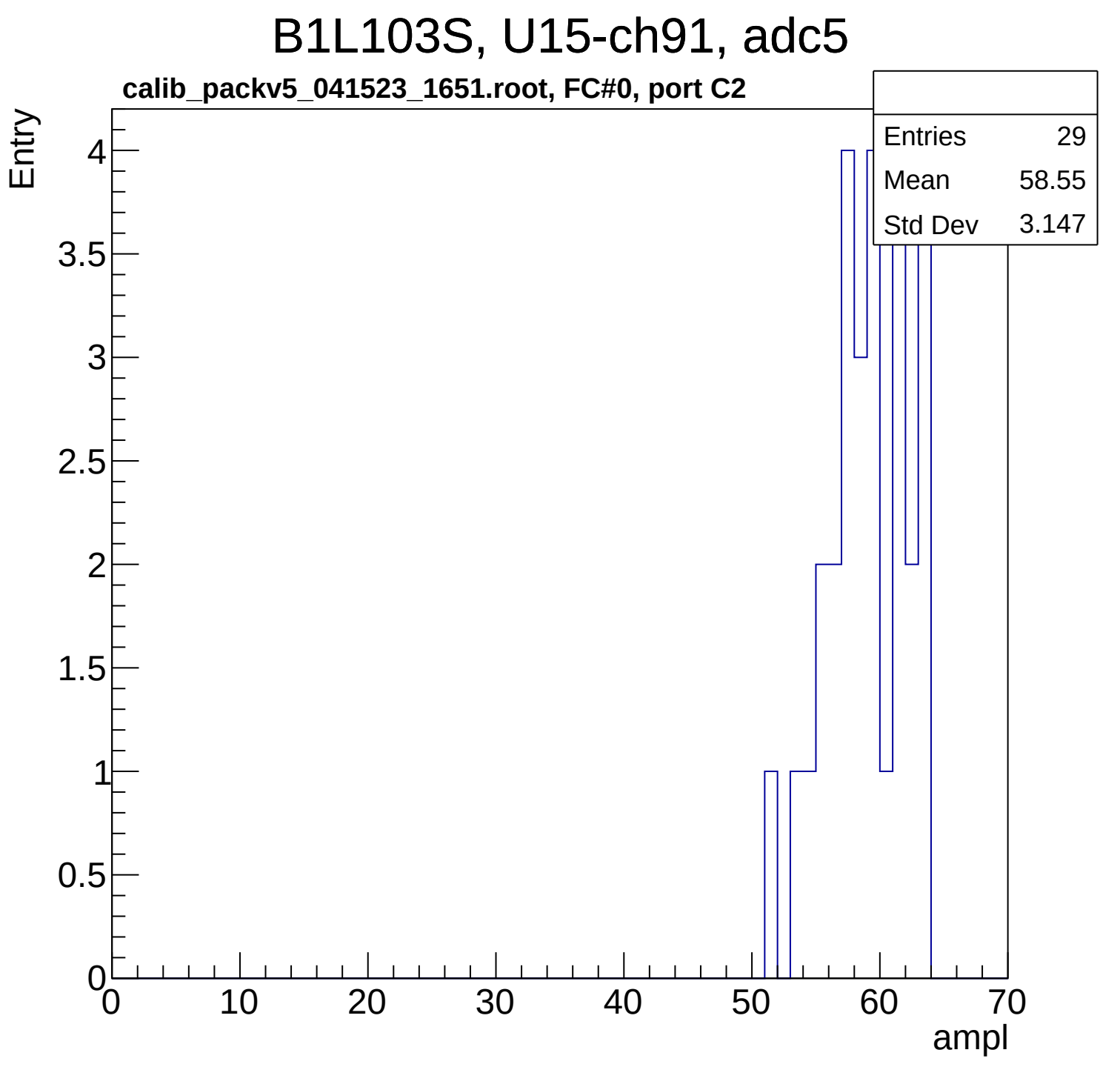
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch91, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 58.55
Std Dev 3.147
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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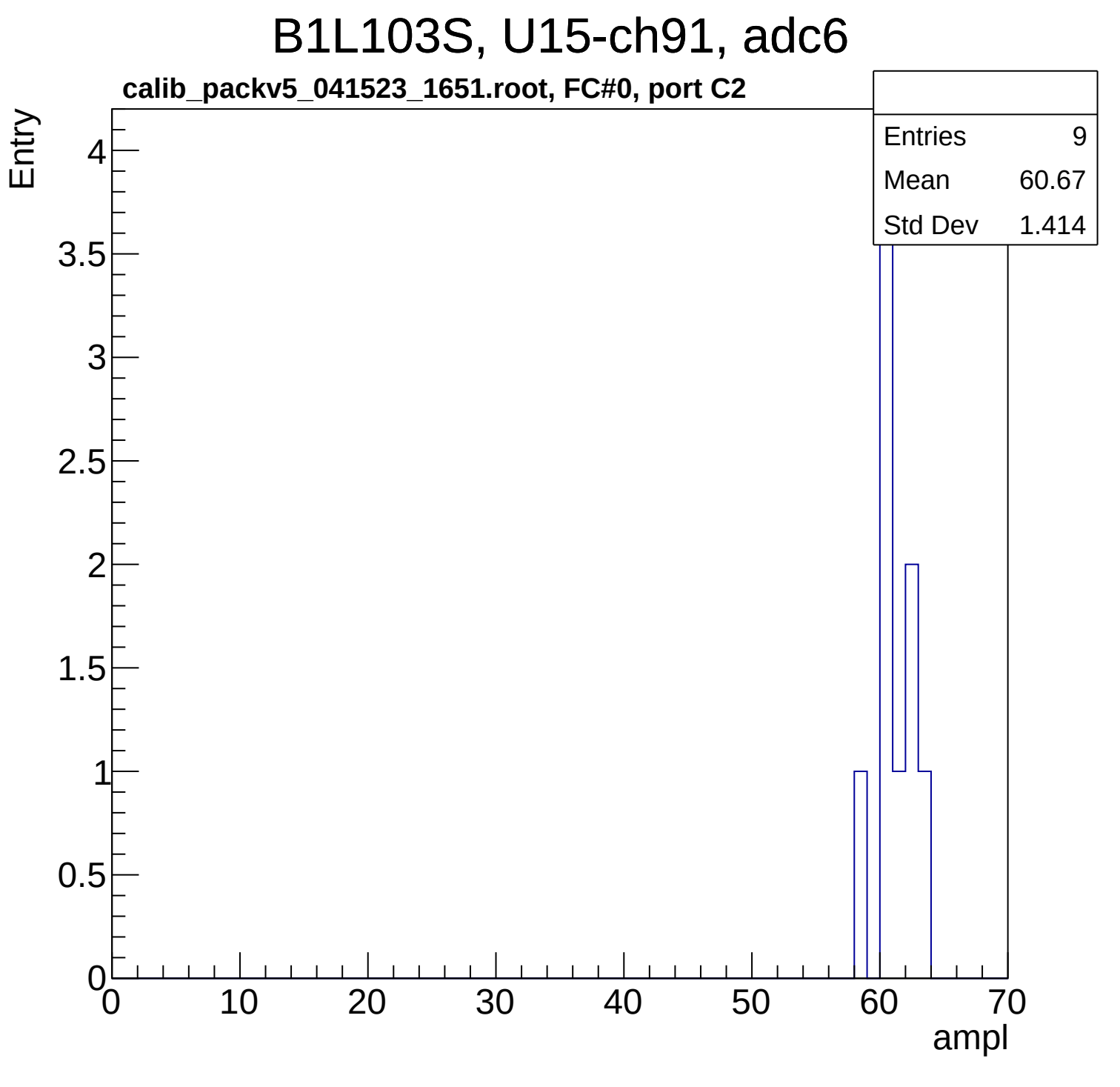
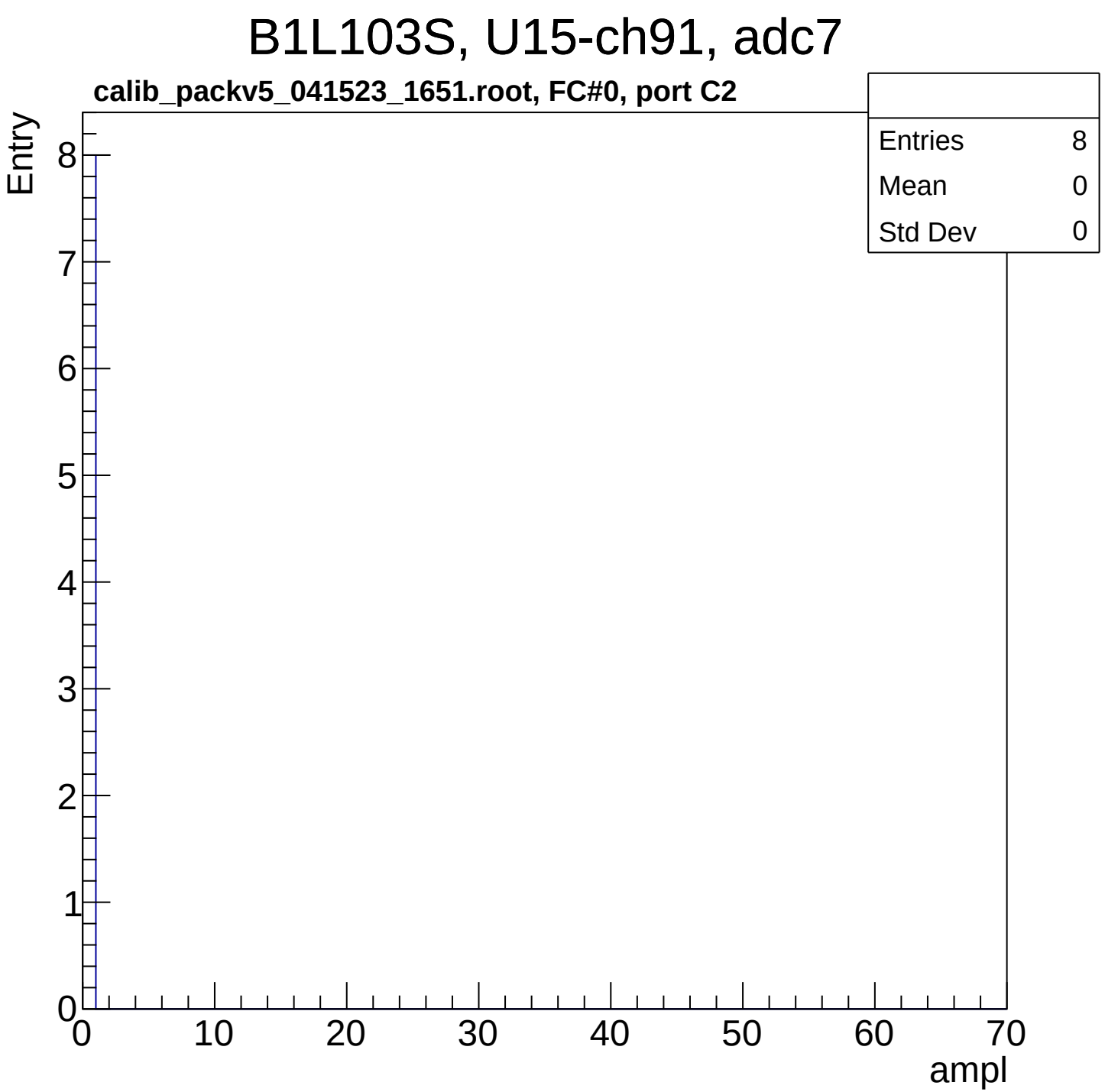
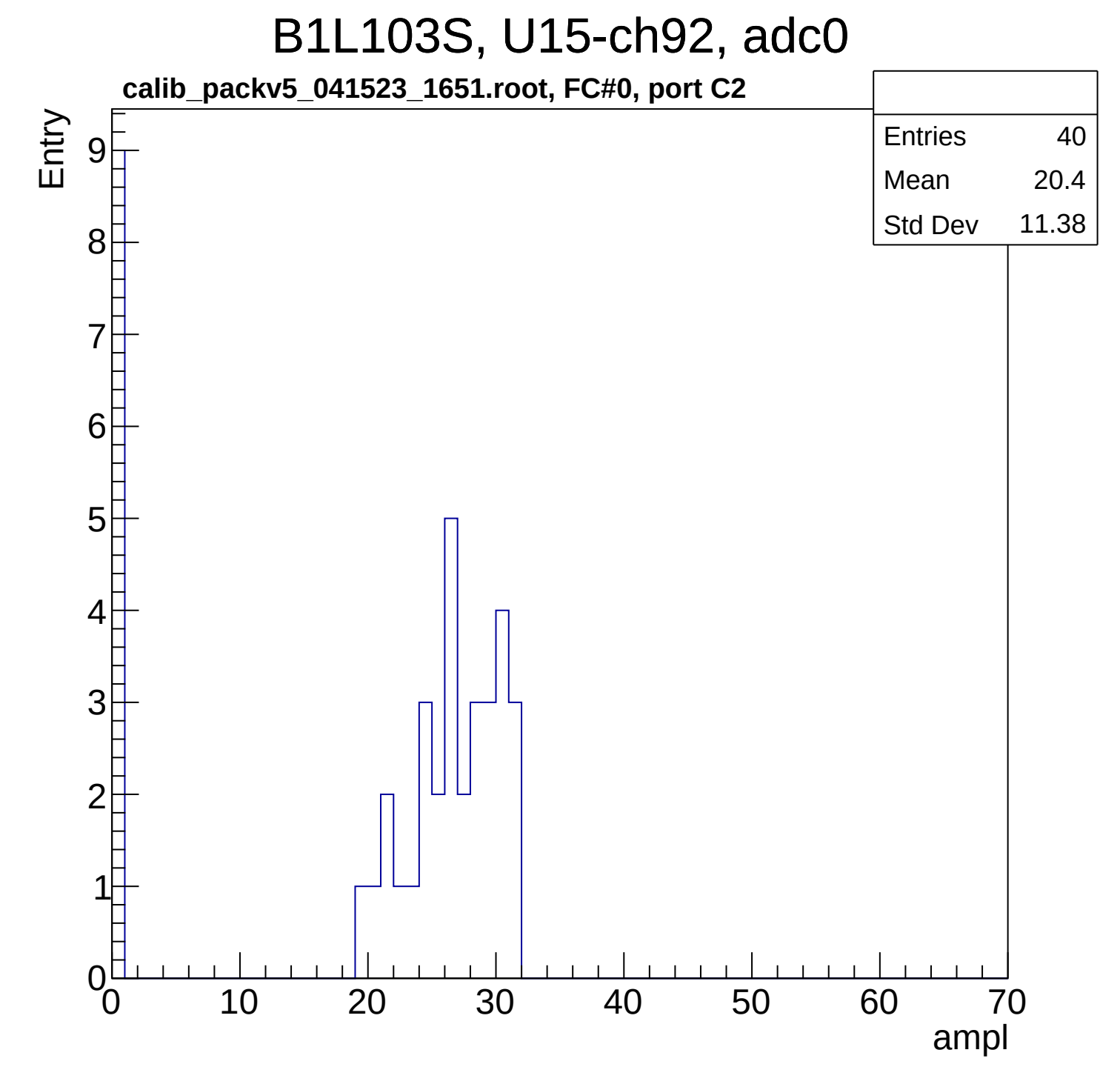
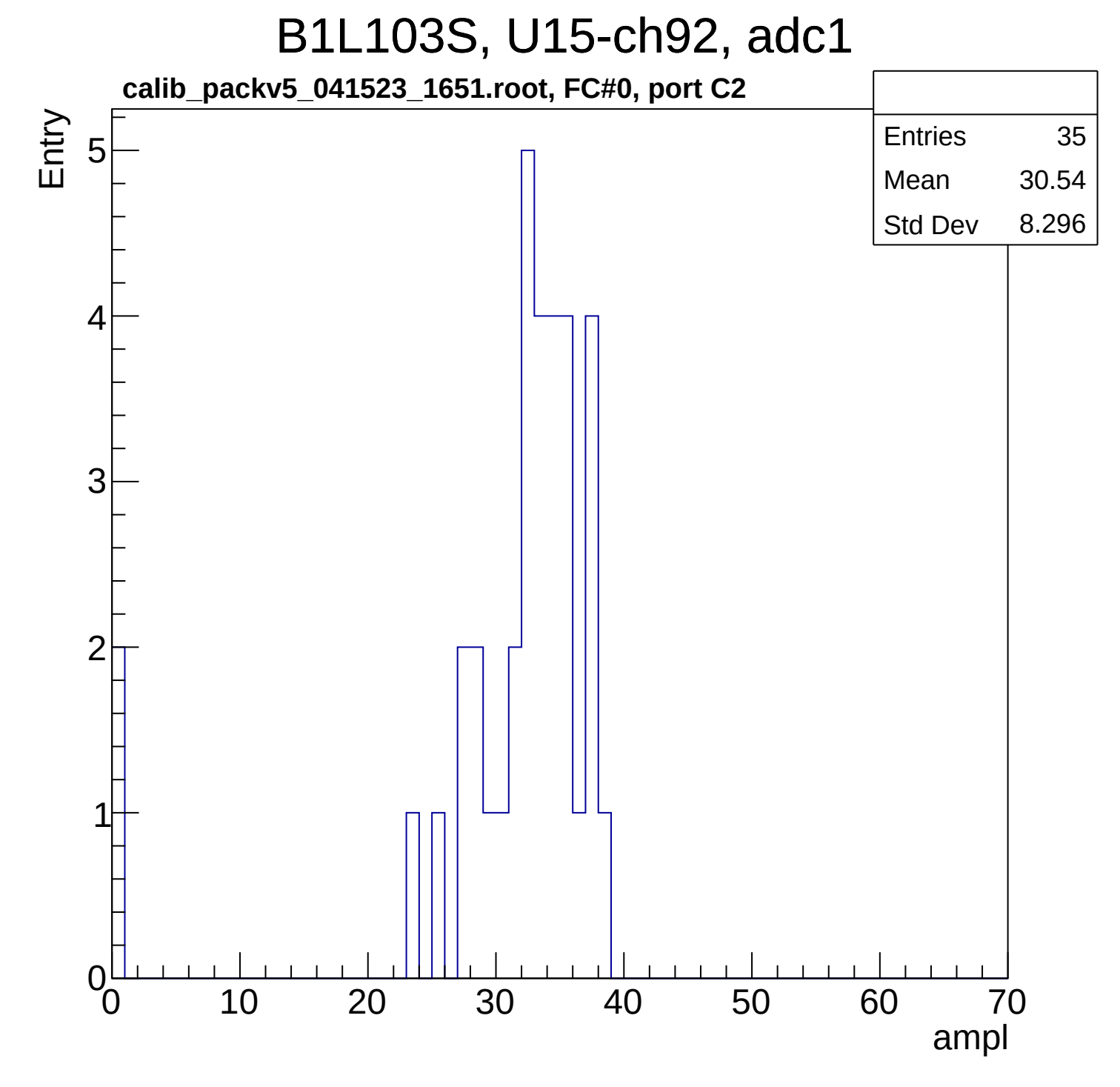
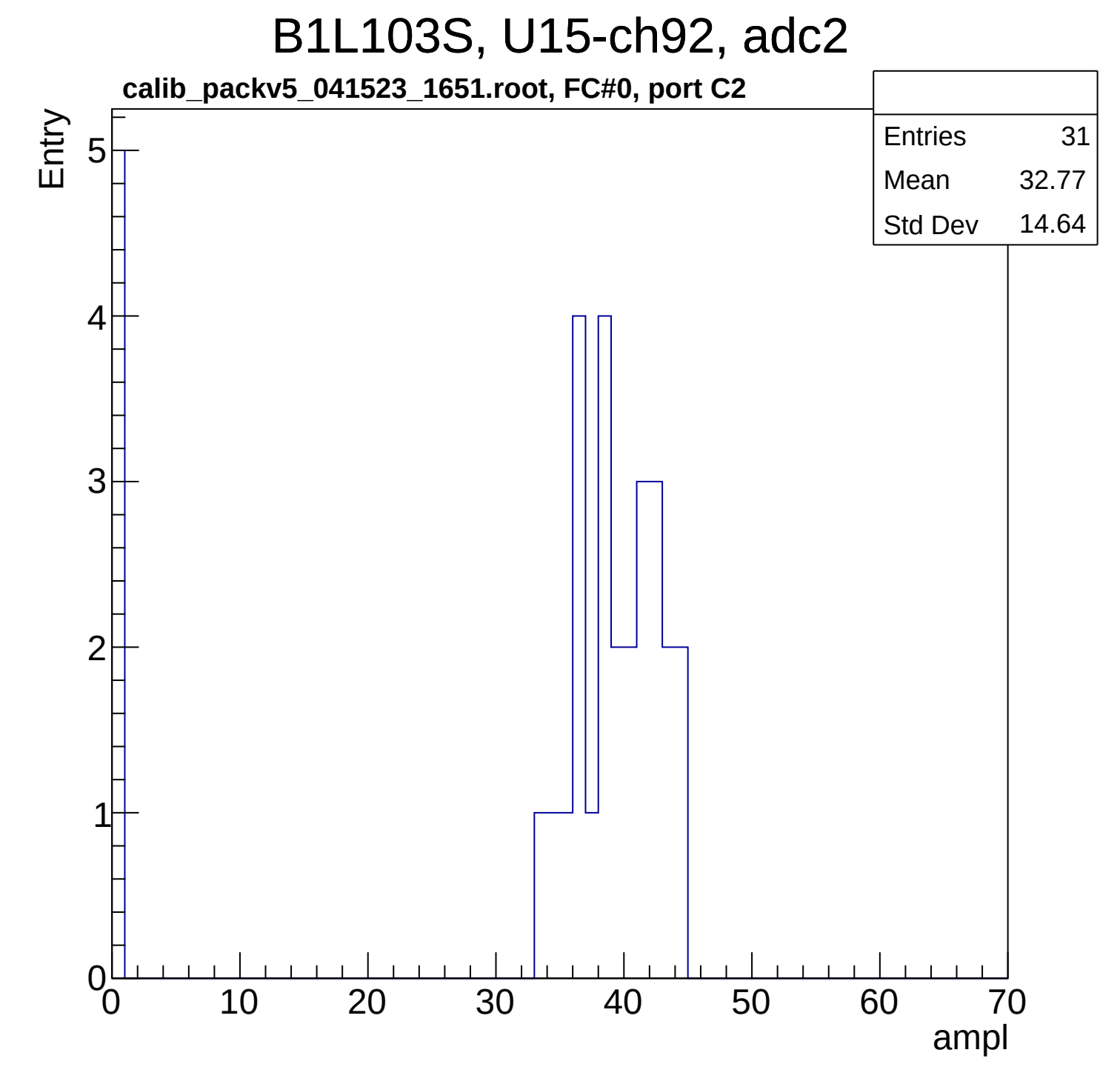
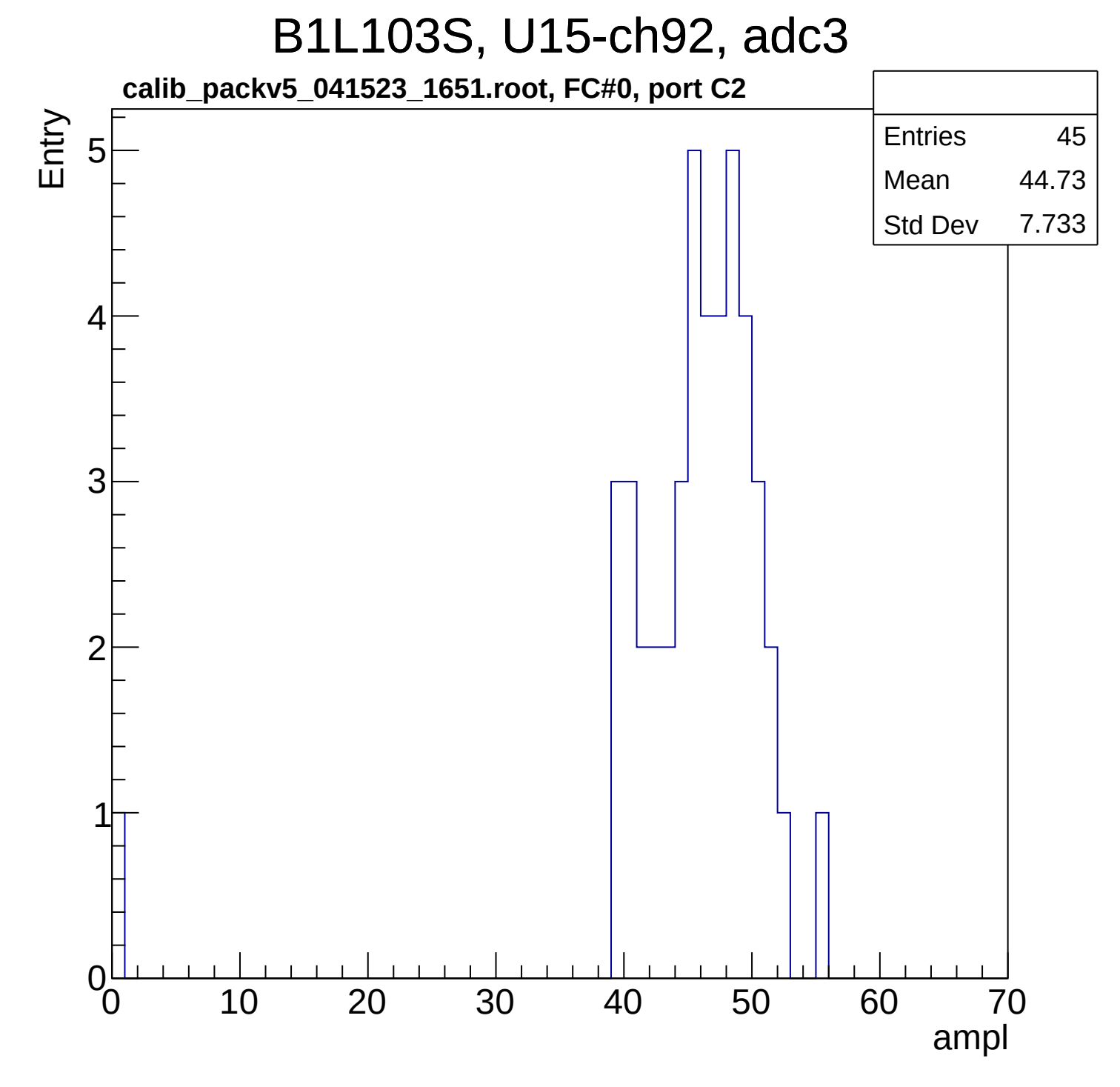

B1L103S, U15-ch91, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 60.67
Std Dev 1.414
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

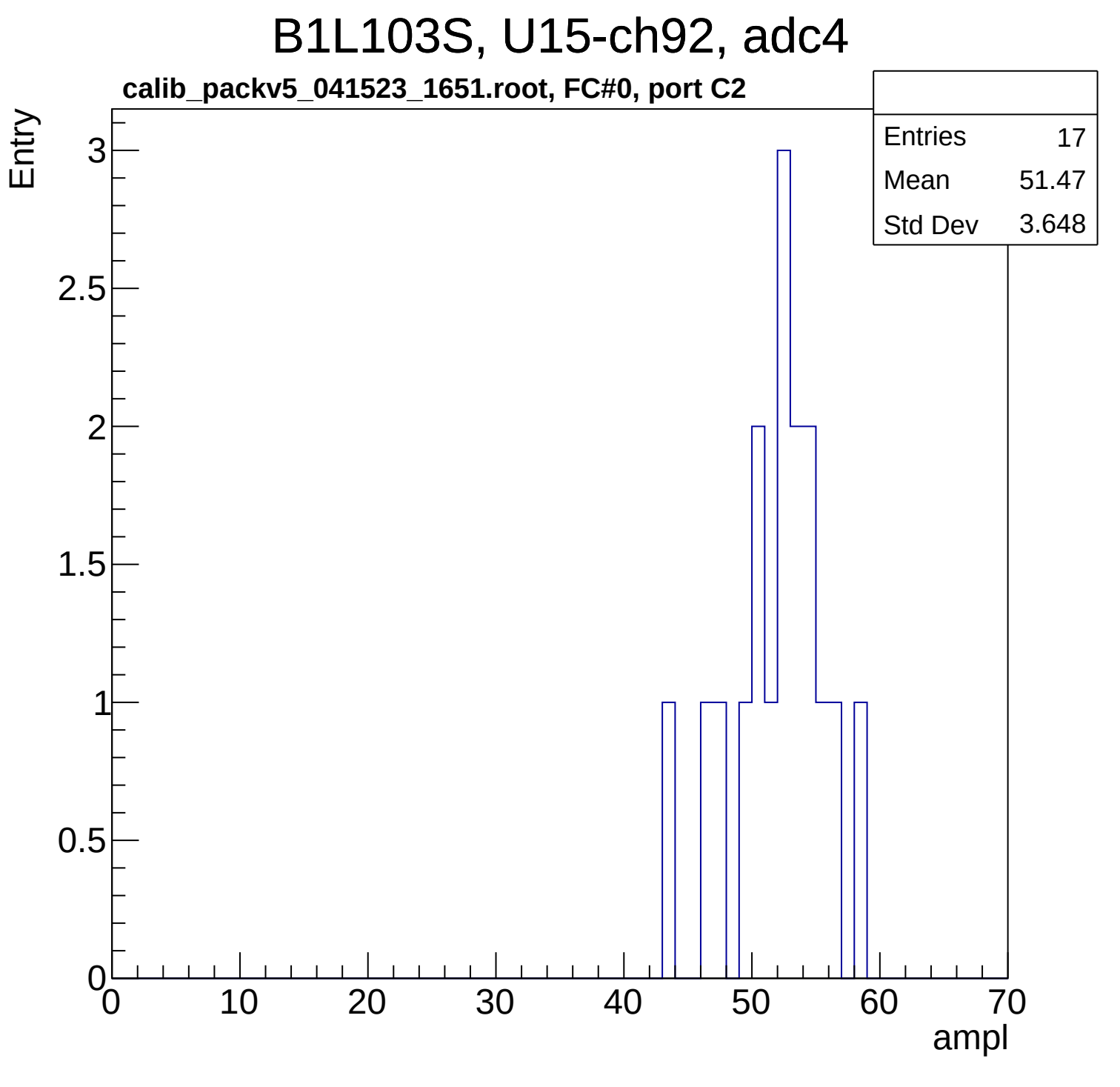

B1L103S, U15-ch91, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 0
Std Dev 0
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch92, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 20.4
Std Dev 11.38
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U15-ch92, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 30.54
Std Dev 8.296
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch92, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 32.77
Std Dev 14.64
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch92, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 44.73
Std Dev 7.733
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch92, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 51.47
Std Dev 3.648
Entry
ampl
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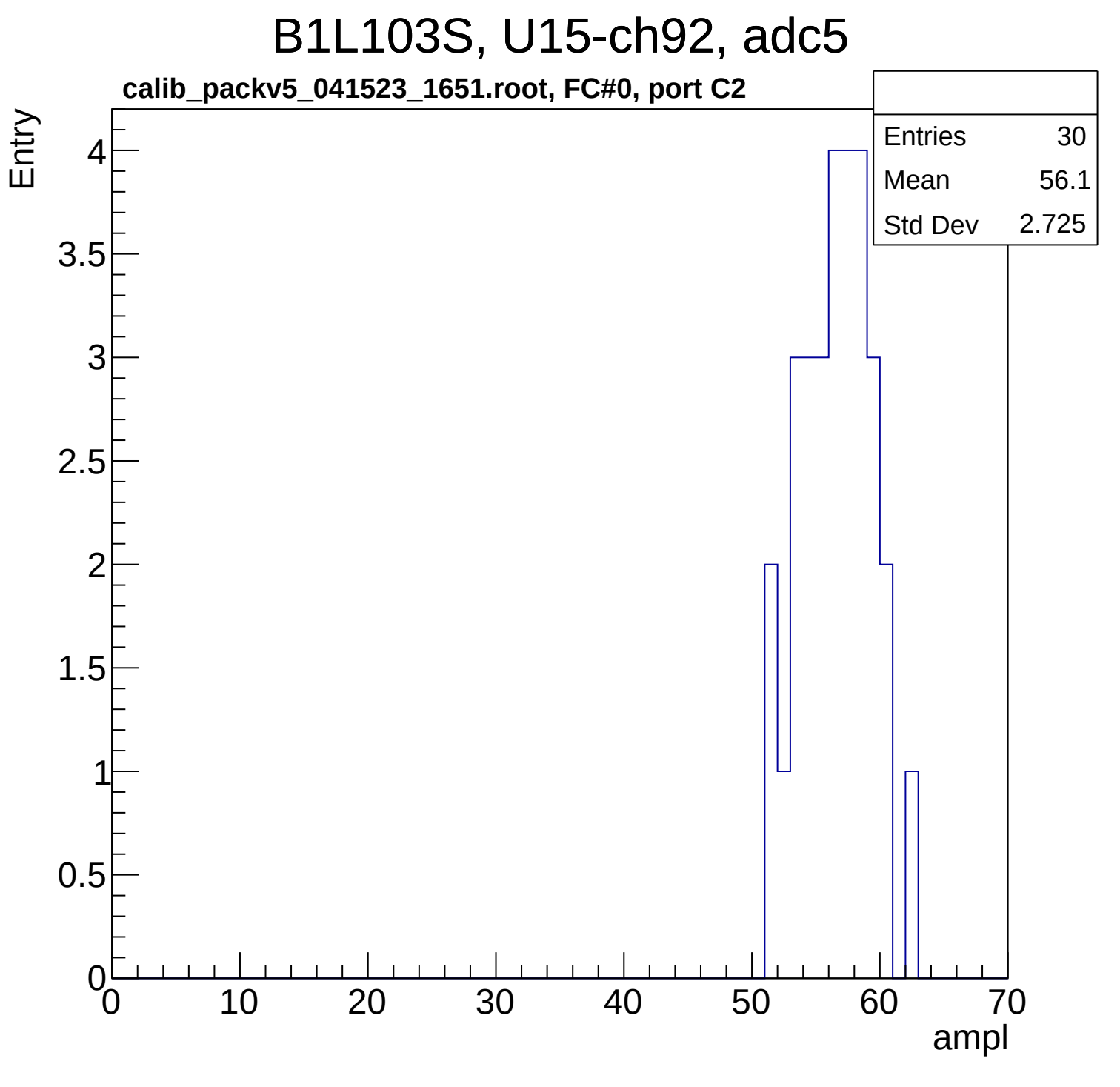
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch92, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 56.1
Std Dev 2.725
Entry
ampl
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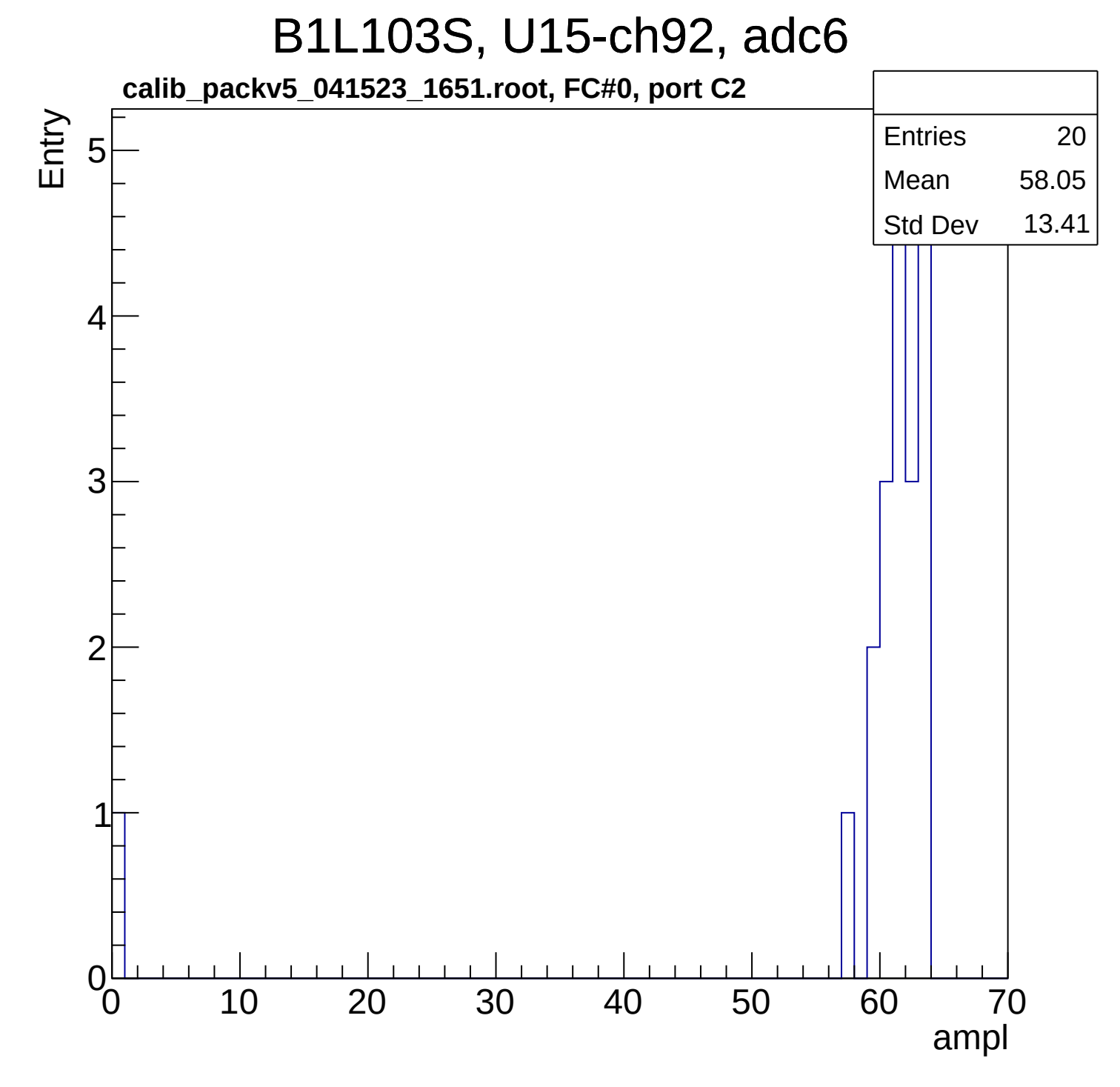
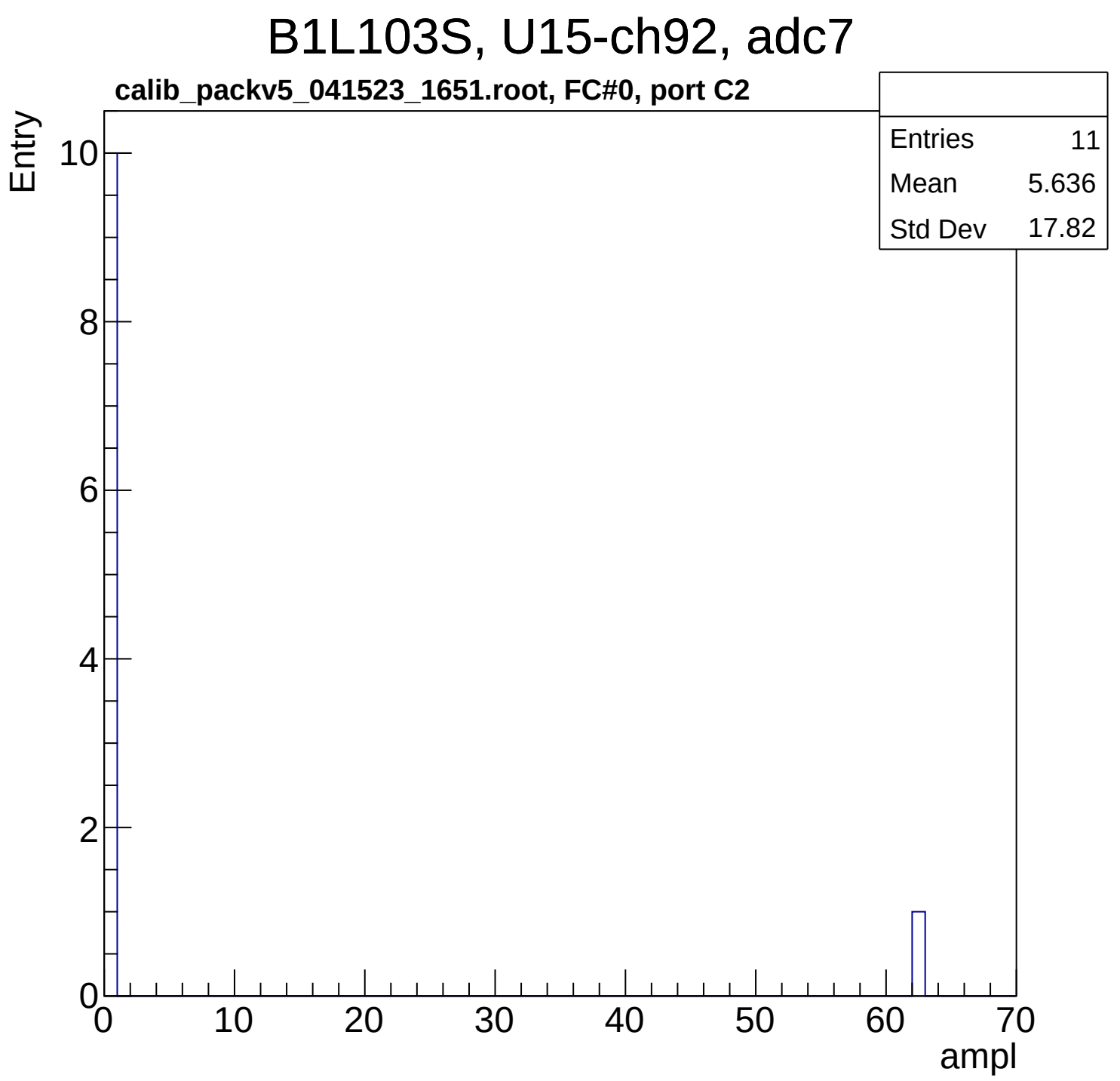
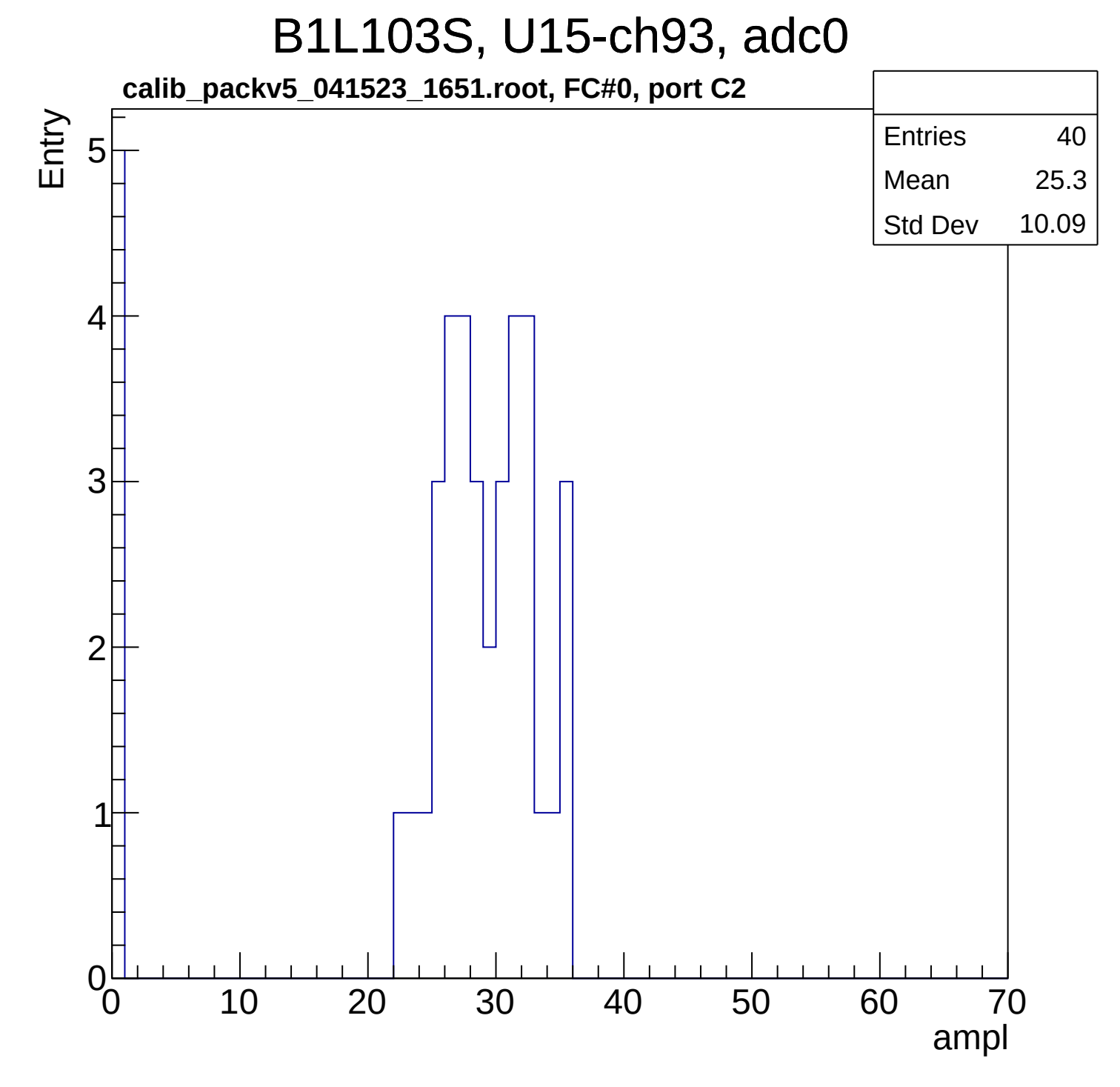
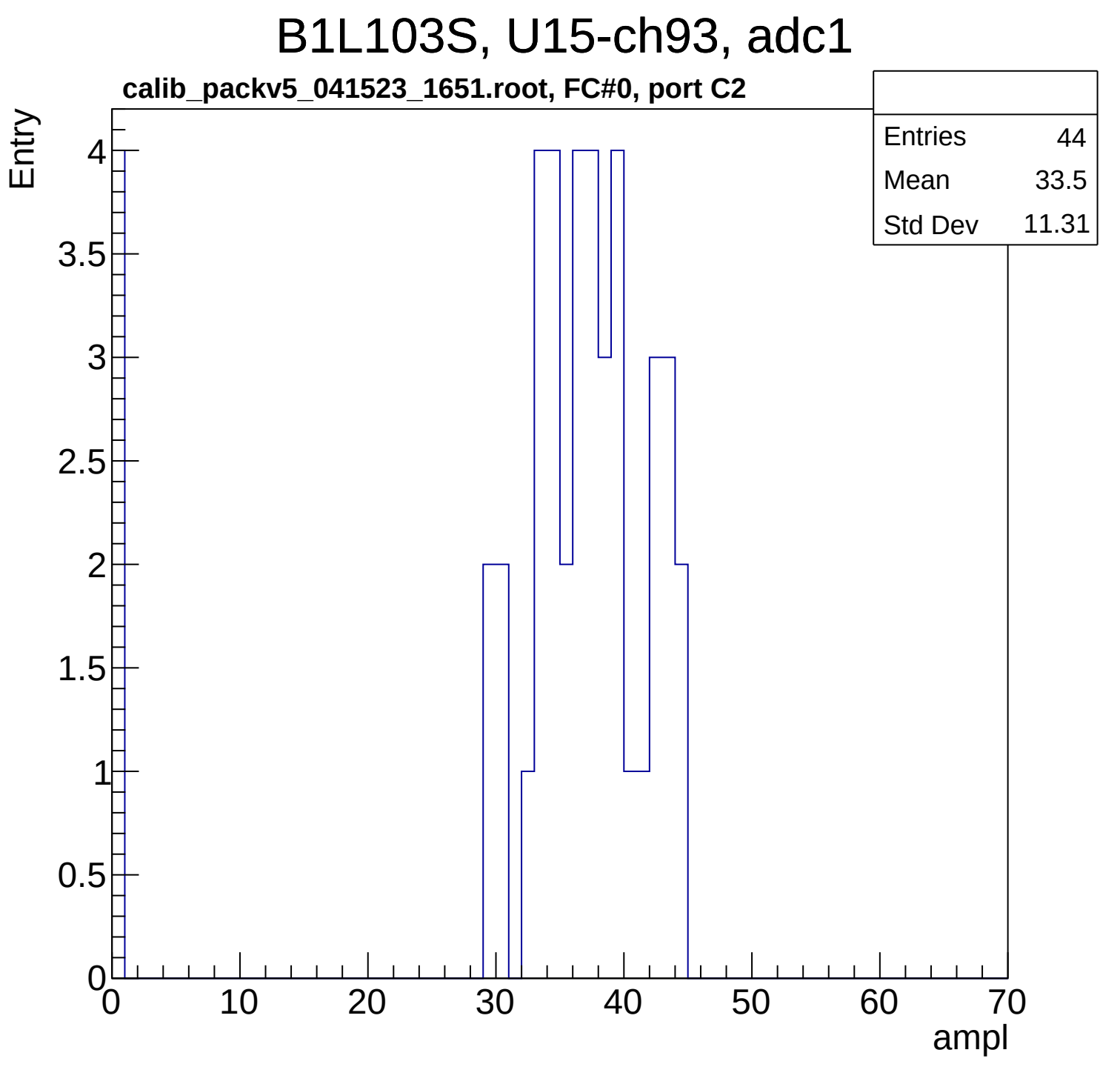
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch92, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 58.05
Std Dev 13.41
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch92, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 5.636
Std Dev 17.82
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch93, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 25.3
Std Dev 10.09
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch93, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 33.5
Std Dev 11.31
Entry
ampl
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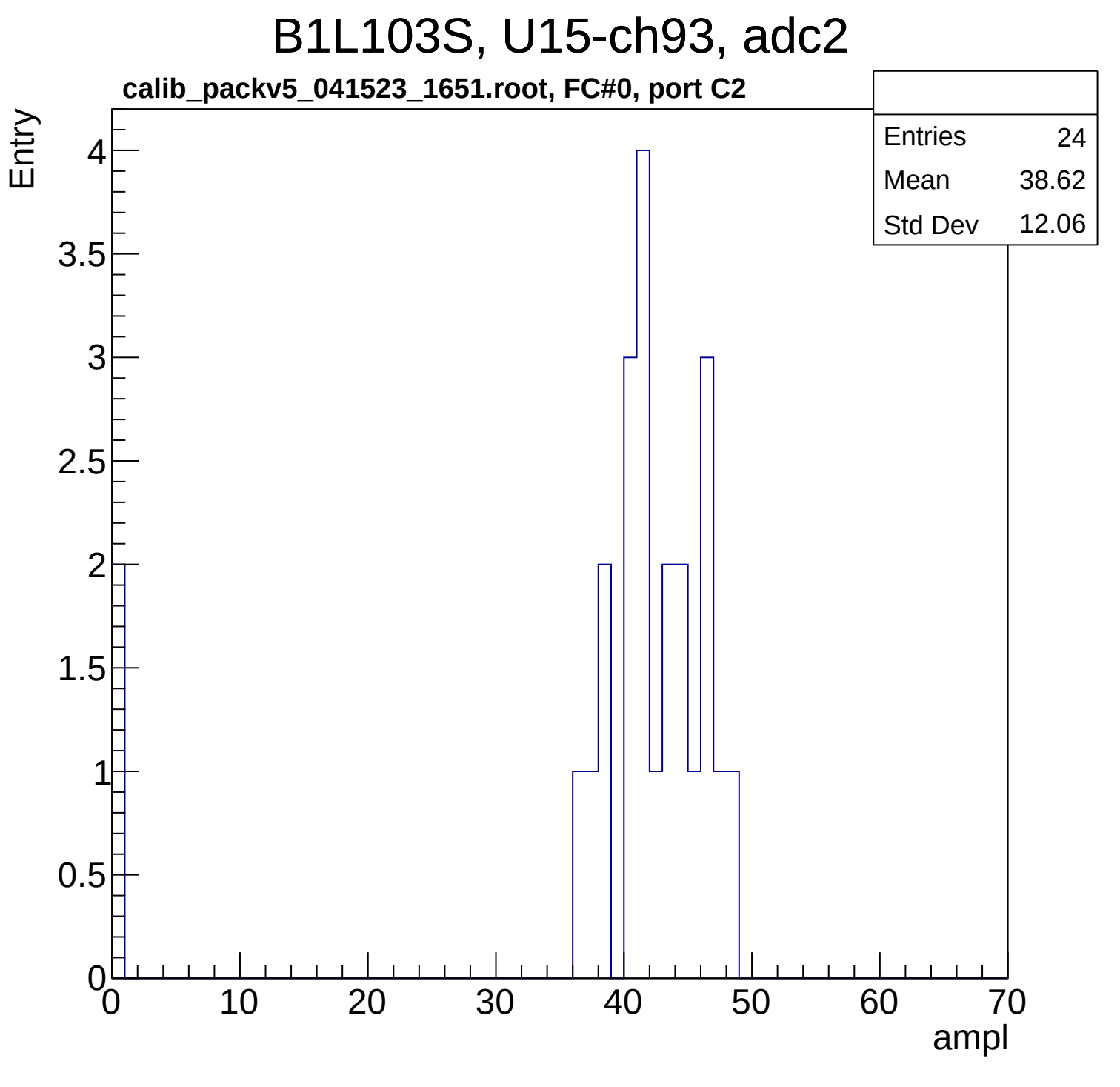
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch93, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 38.62
Std Dev 12.06
Entry
ampl
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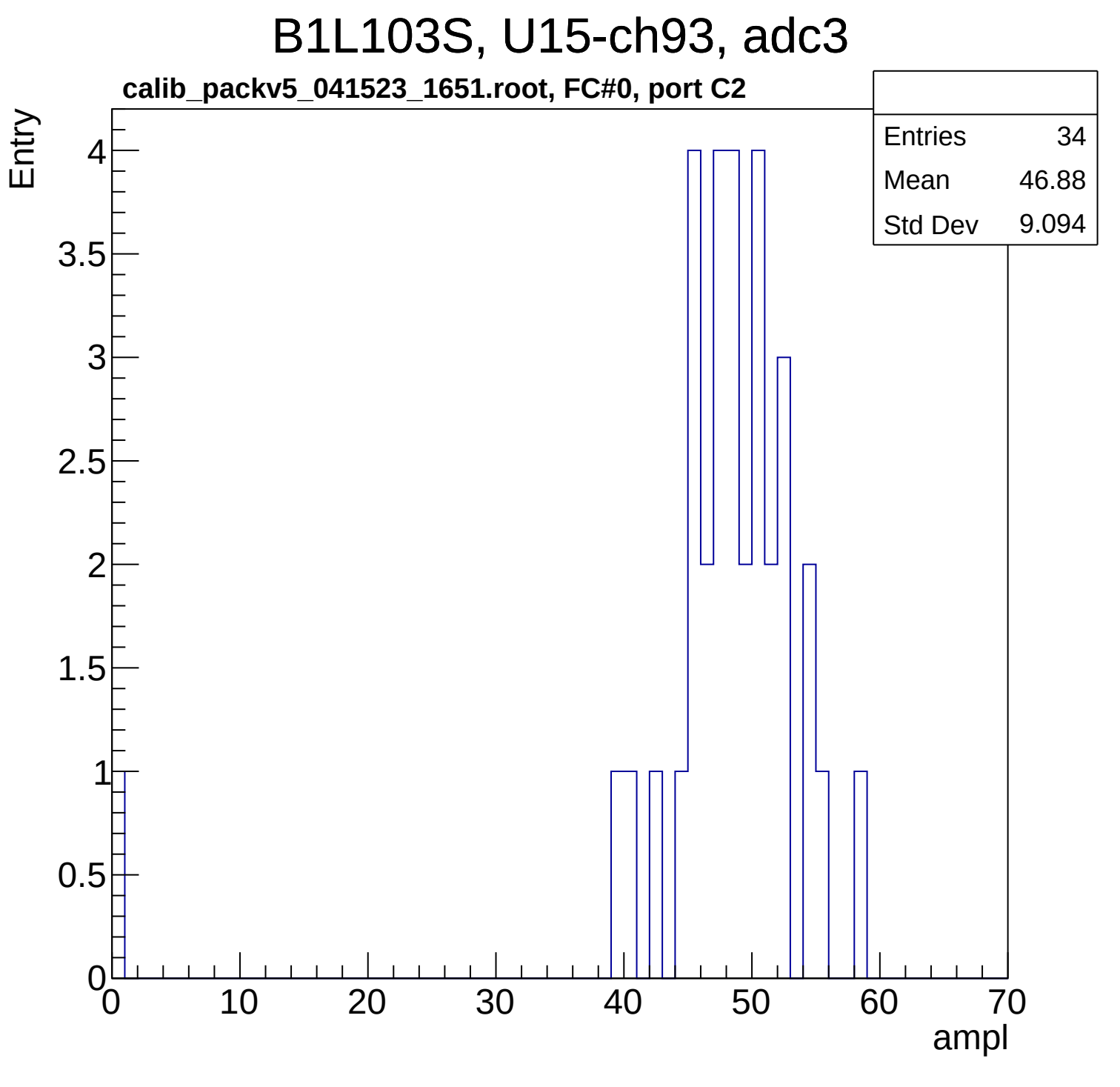
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch93, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 46.88
Std Dev 9.094
Entry
ampl
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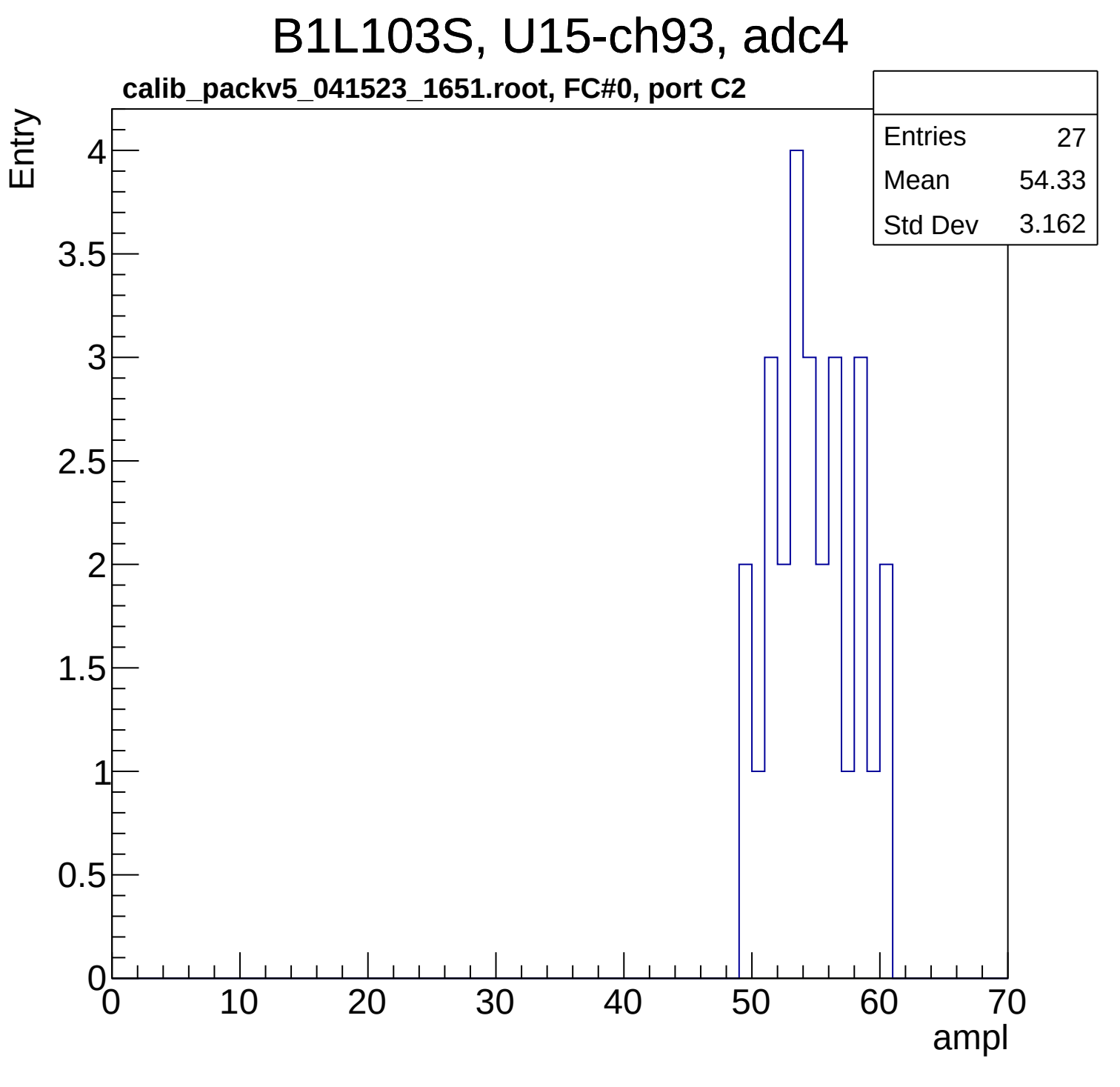
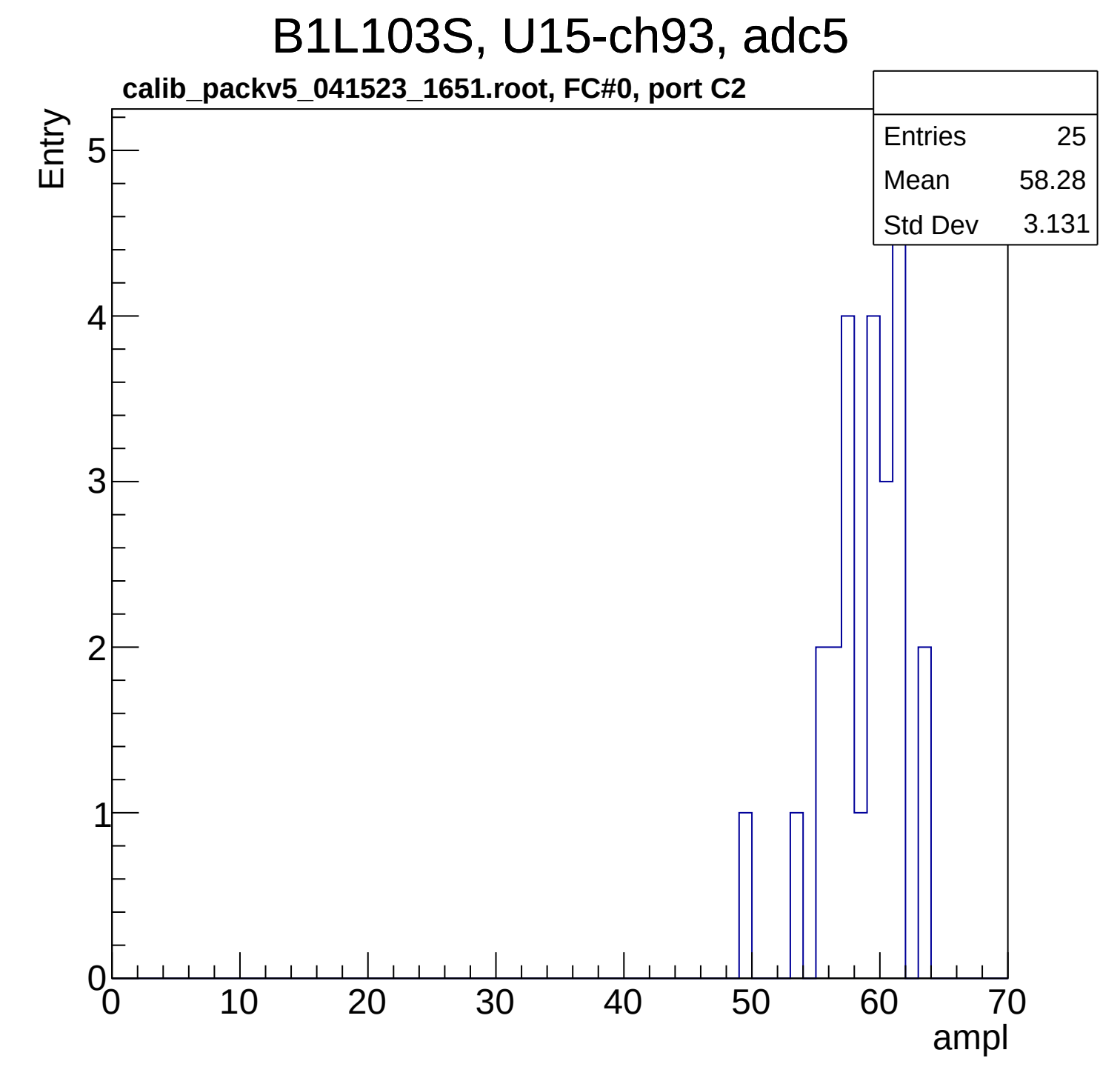
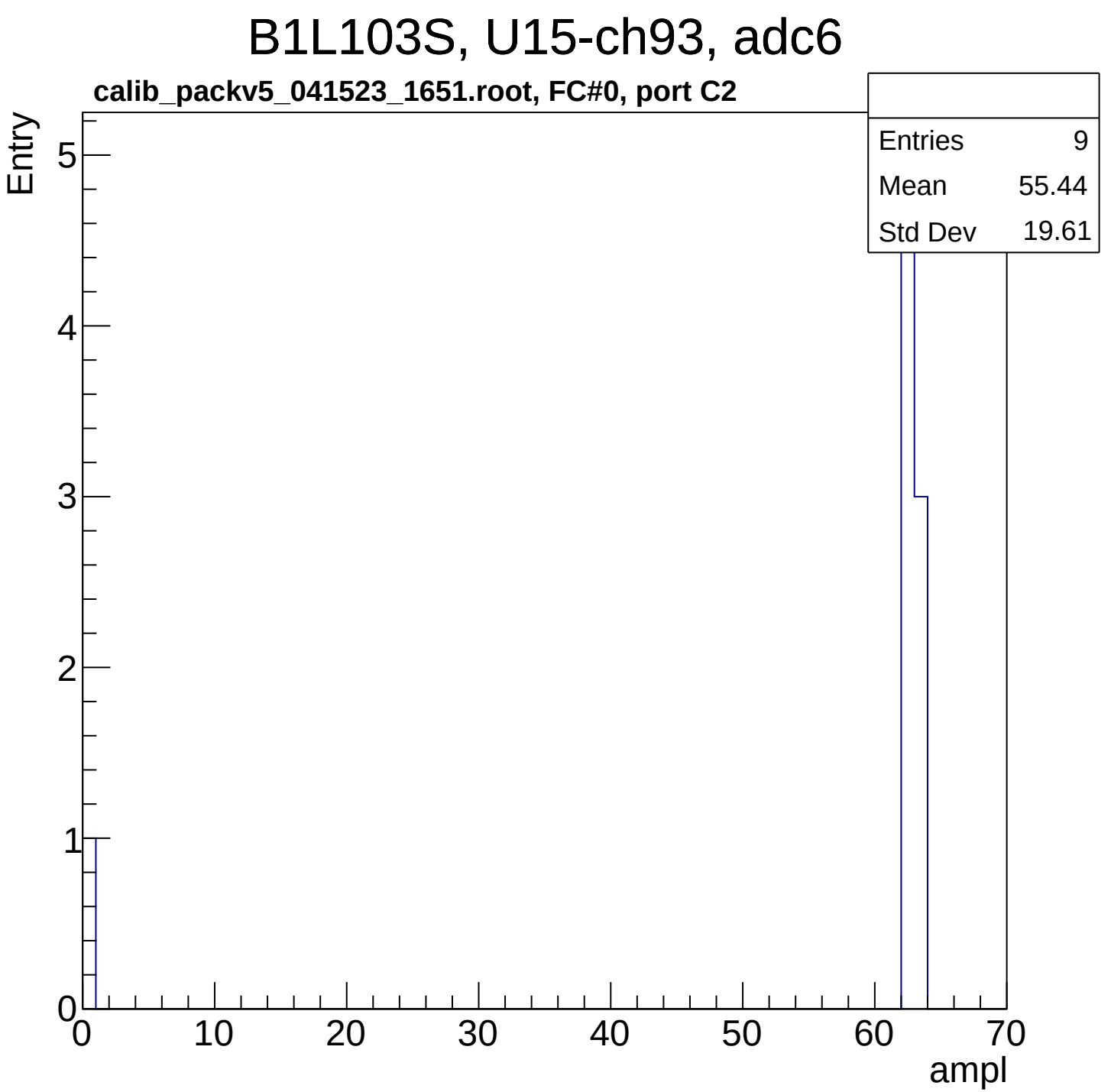
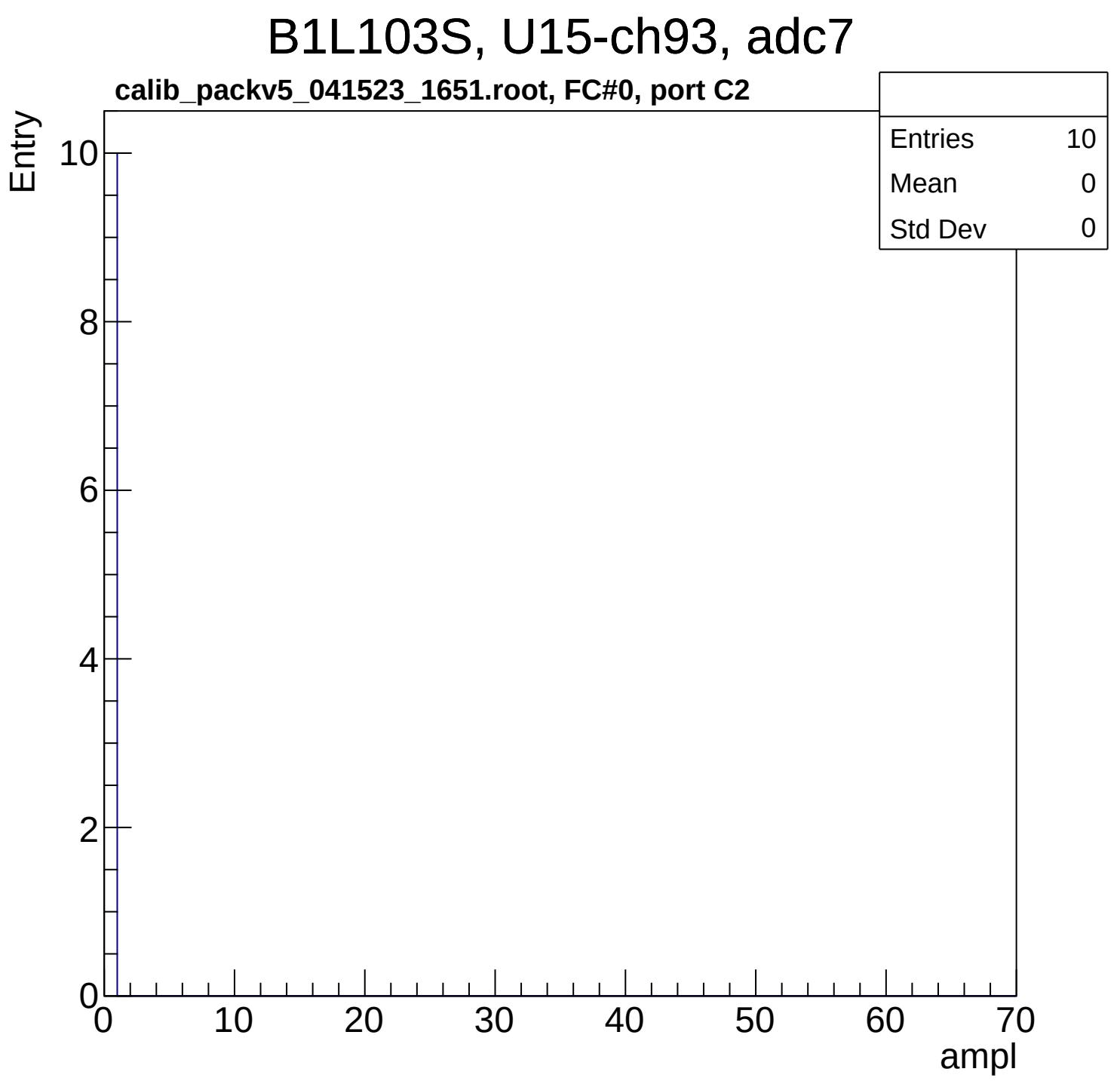
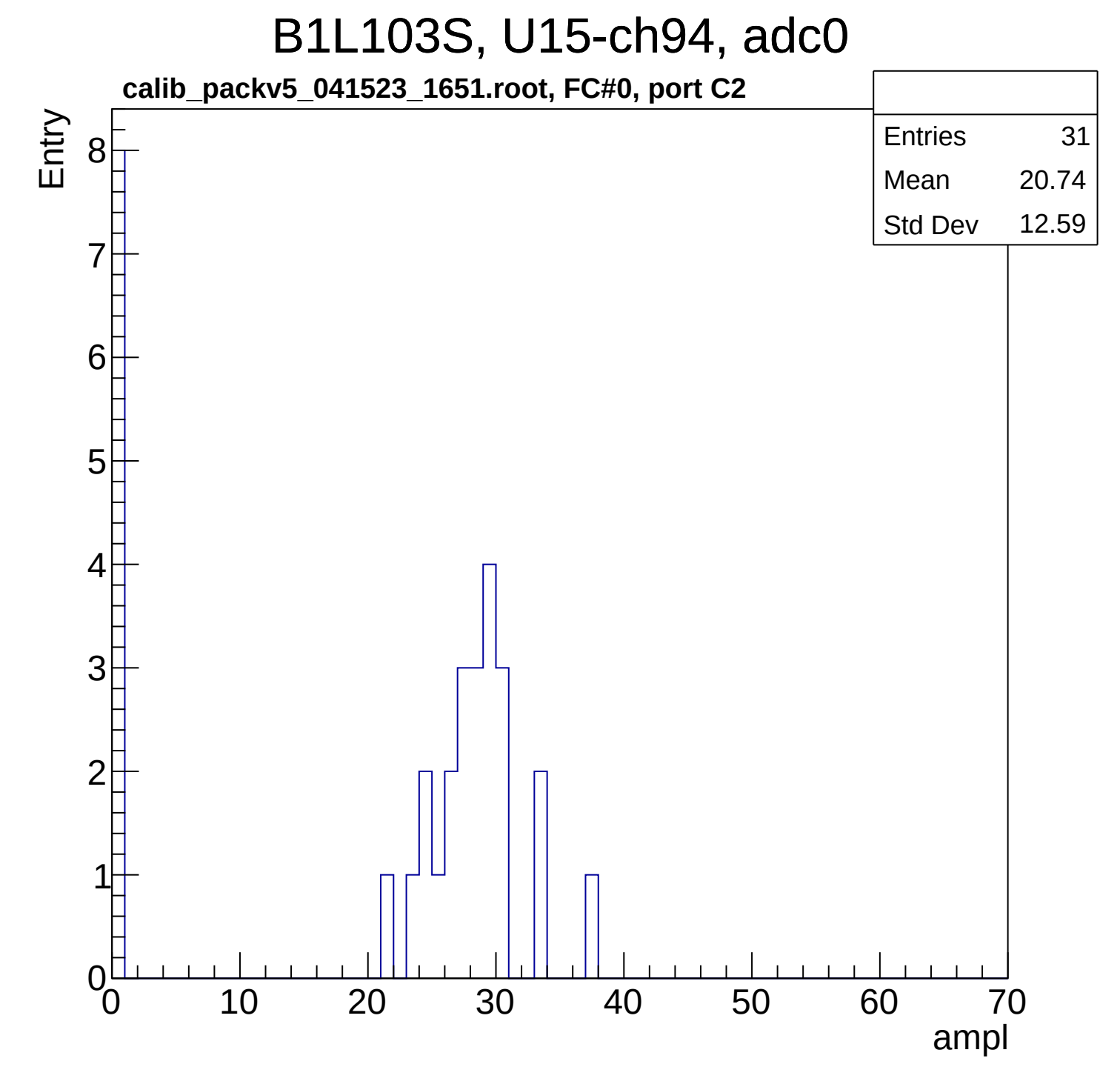
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch93, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 54.33
Std Dev 3.162
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch93, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 58.28
Std Dev 3.131
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch93, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 55.44
Std Dev 19.61
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch93, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch94, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 20.74
Std Dev 12.59
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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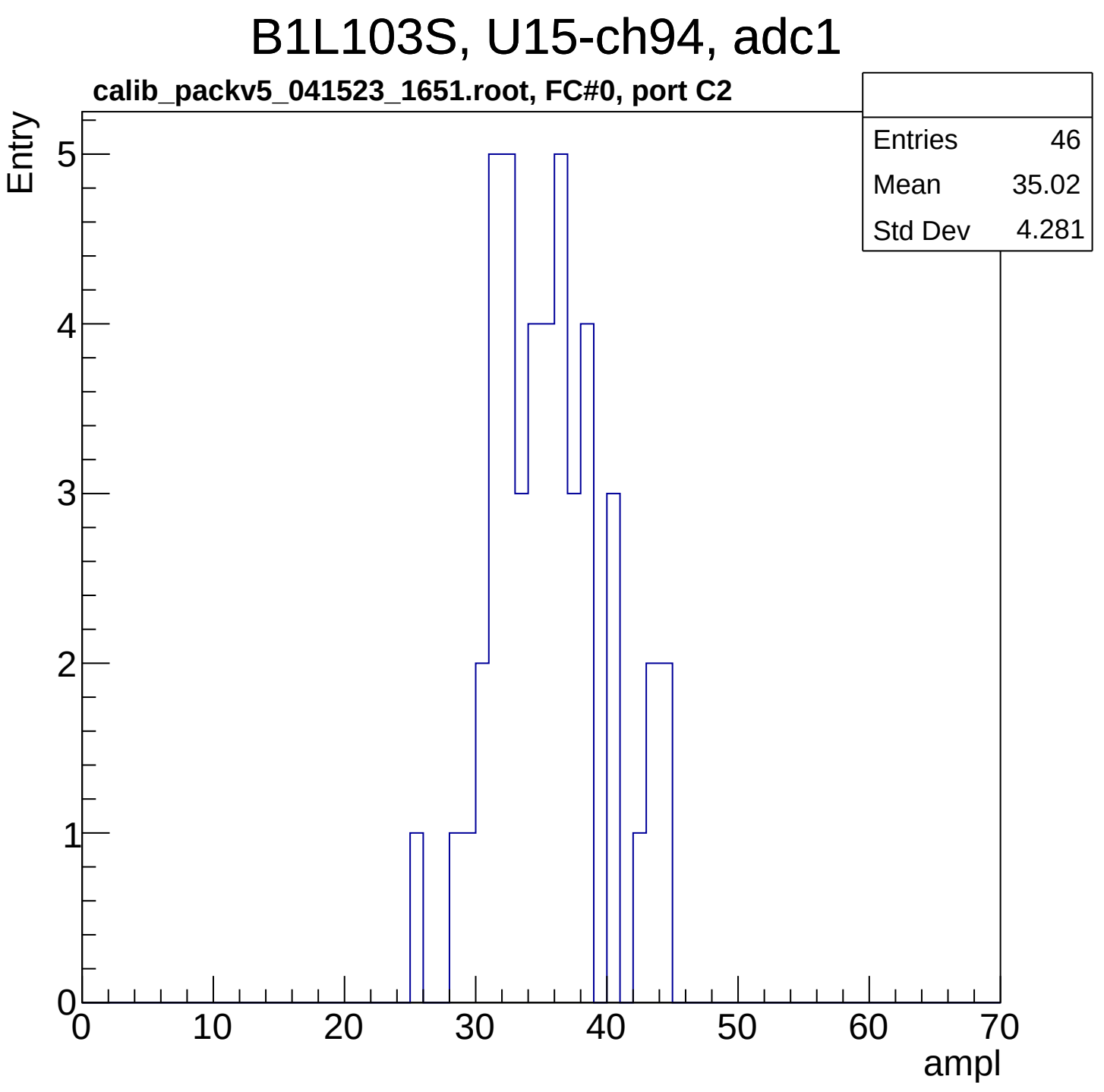
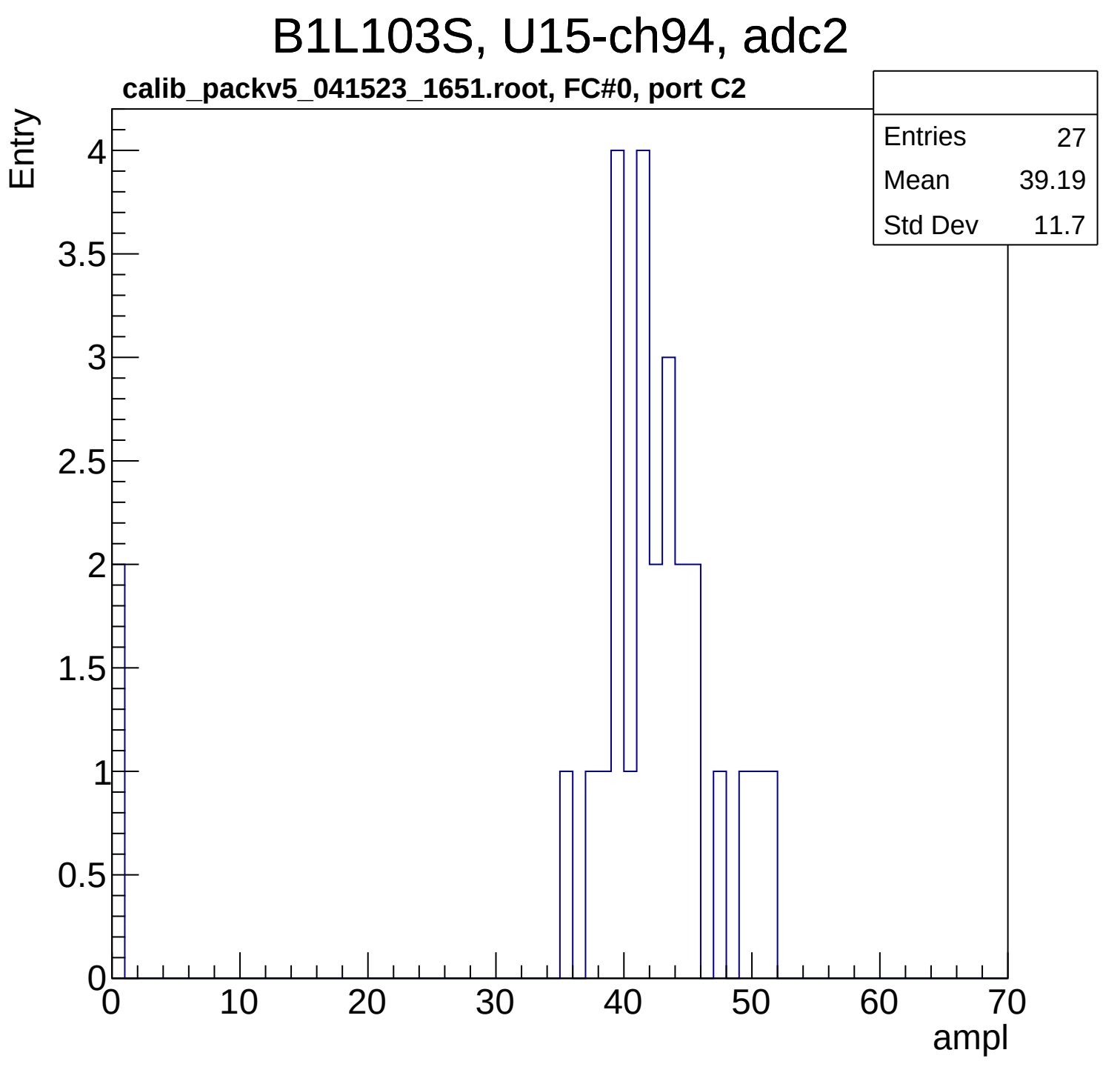
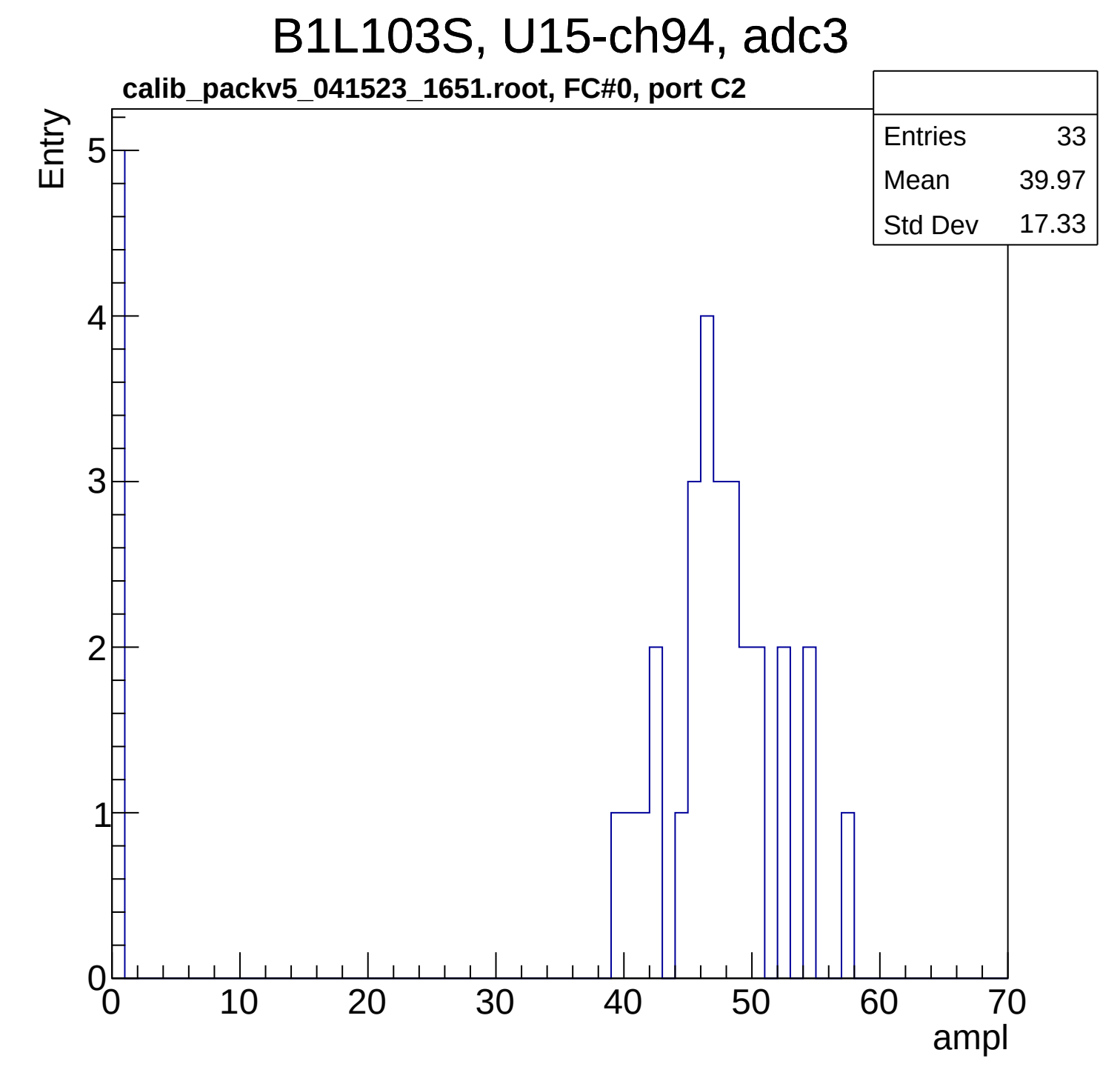
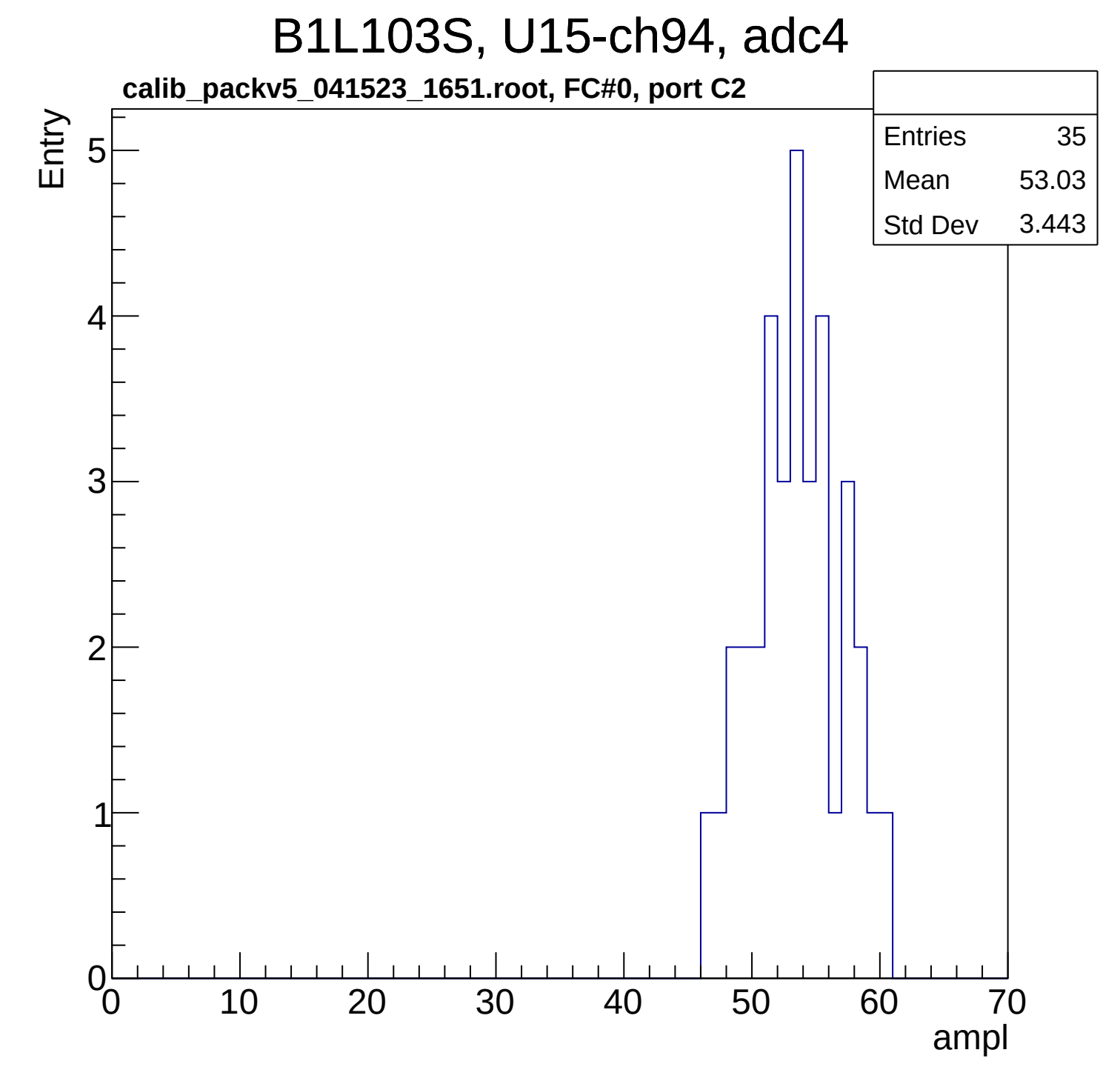
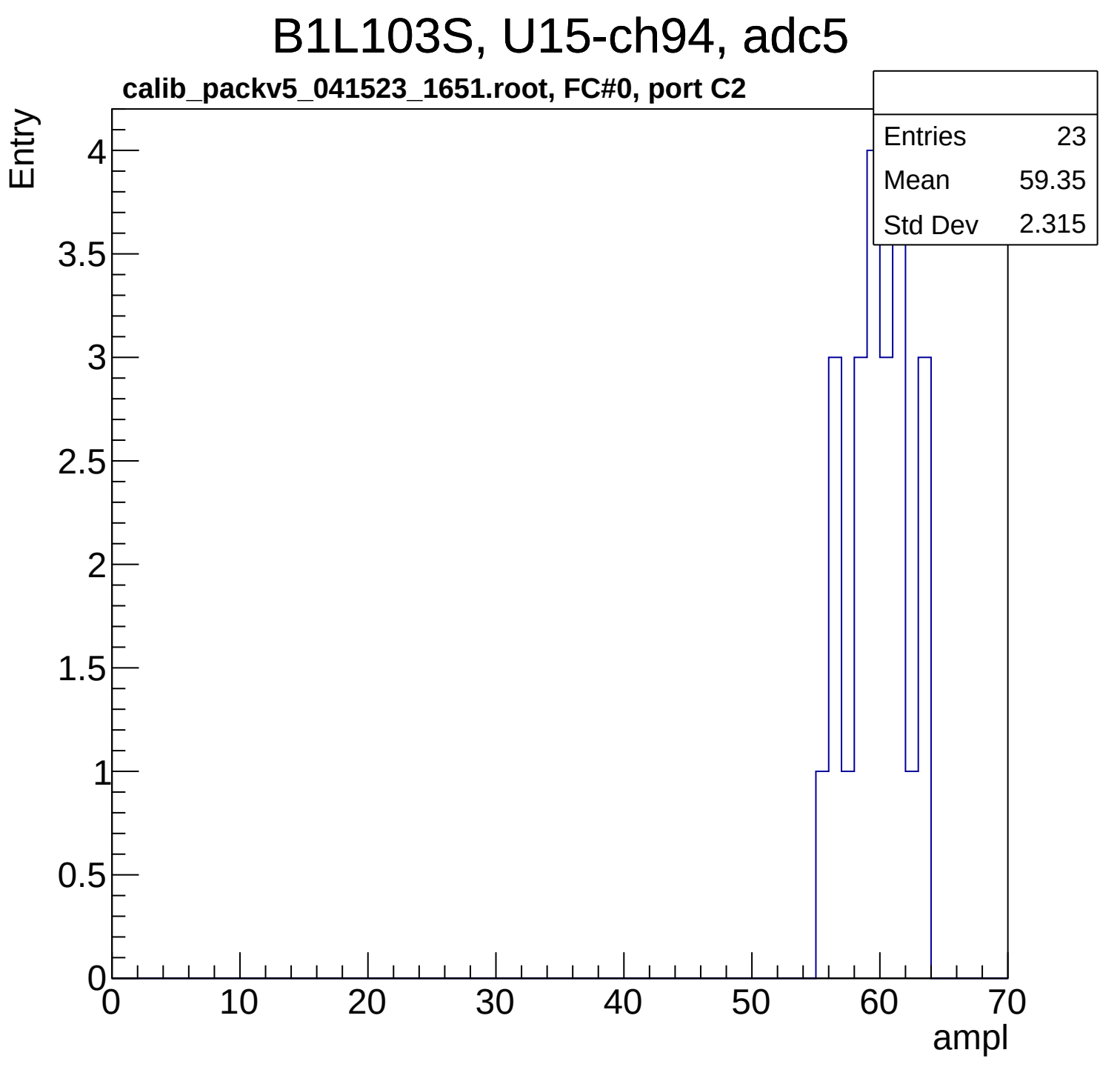
40
50
60
70


B1L103S, U15-ch94, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 35.02
Std Dev 4.281
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch94, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 39.19
Std Dev 11.7
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch94, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 39.97
Std Dev 17.33
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch94, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 53.03
Std Dev 3.443
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch94, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 59.35
Std Dev 2.315
Entry
ampl
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0.5
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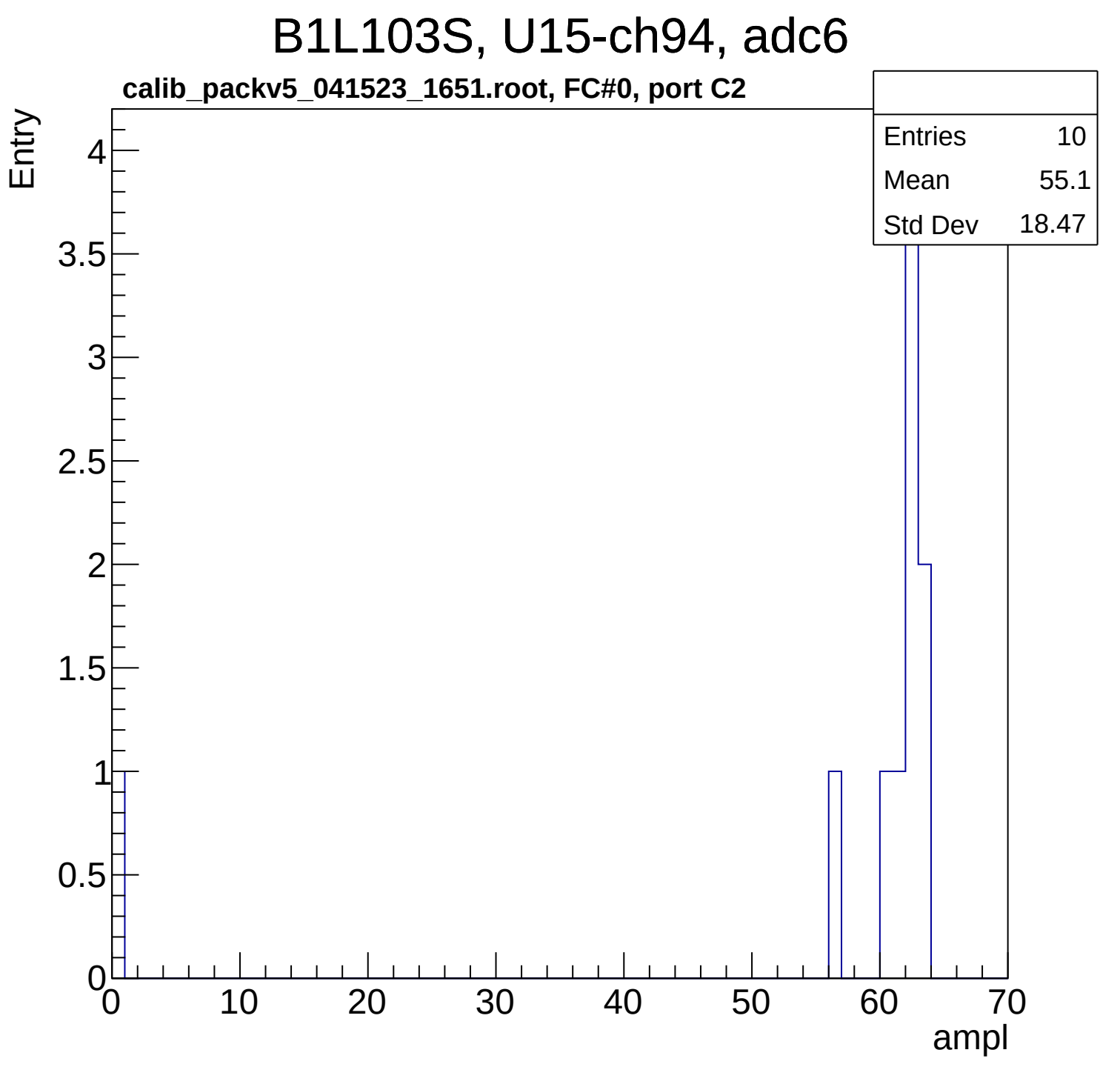
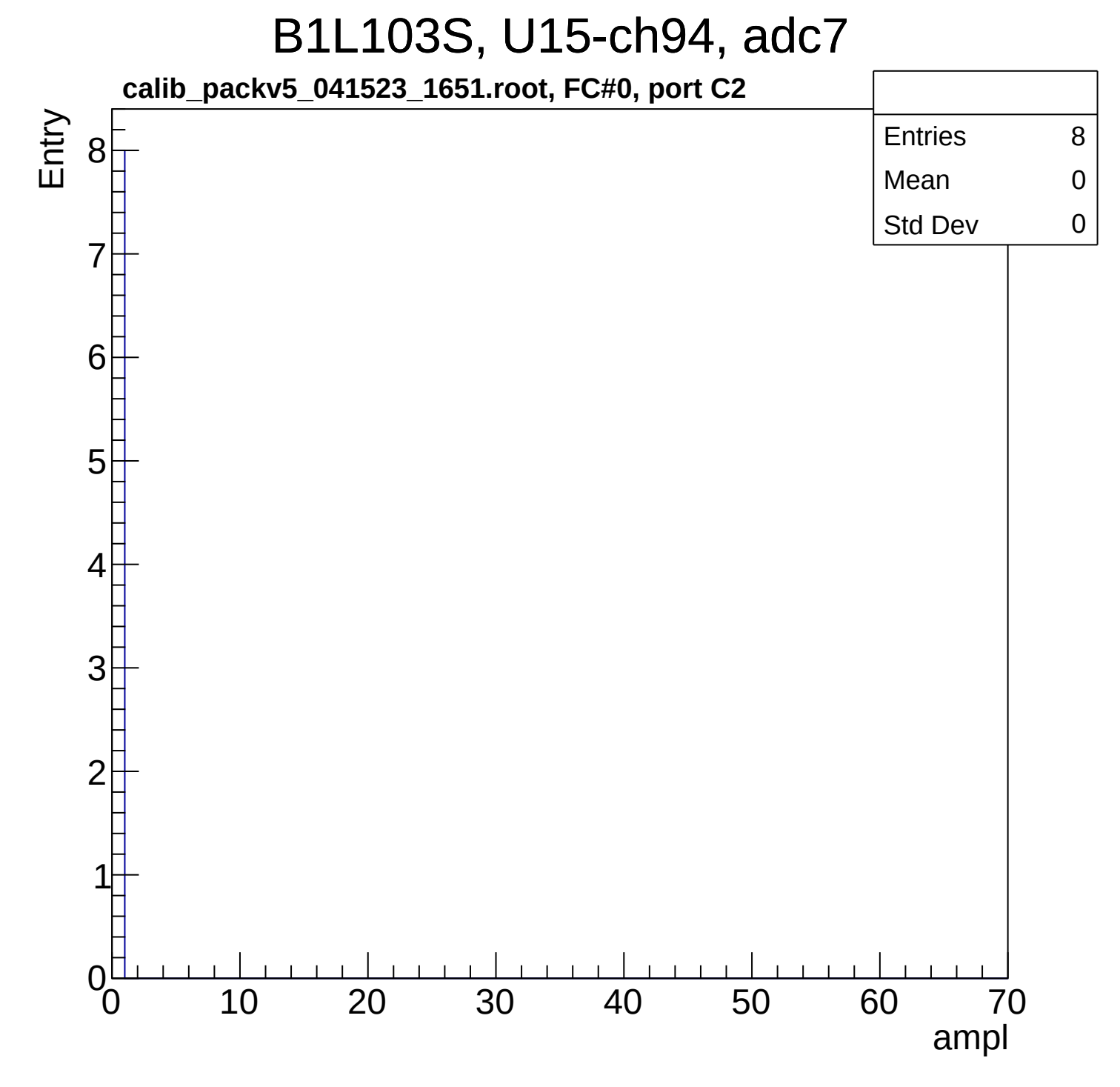
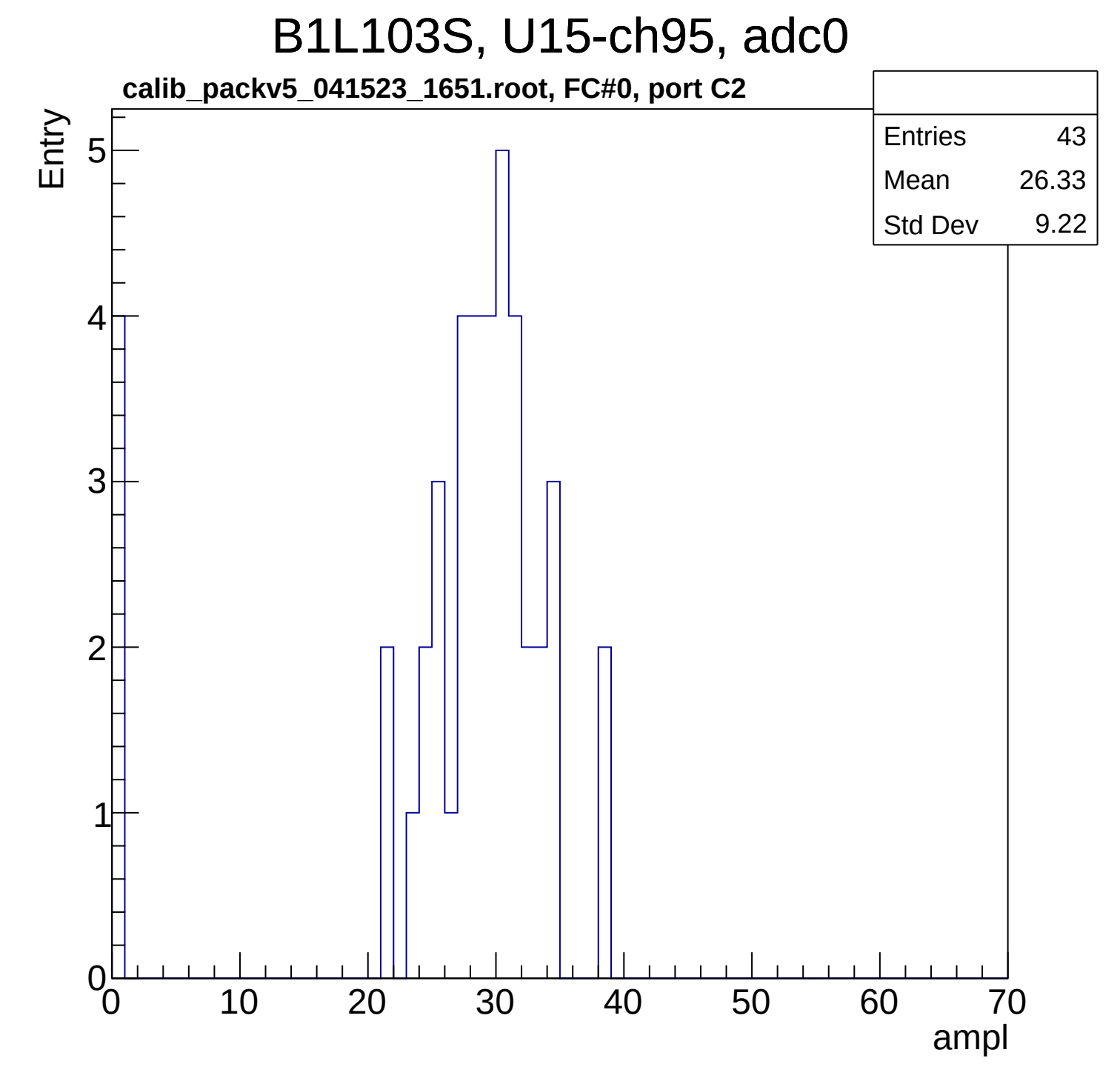
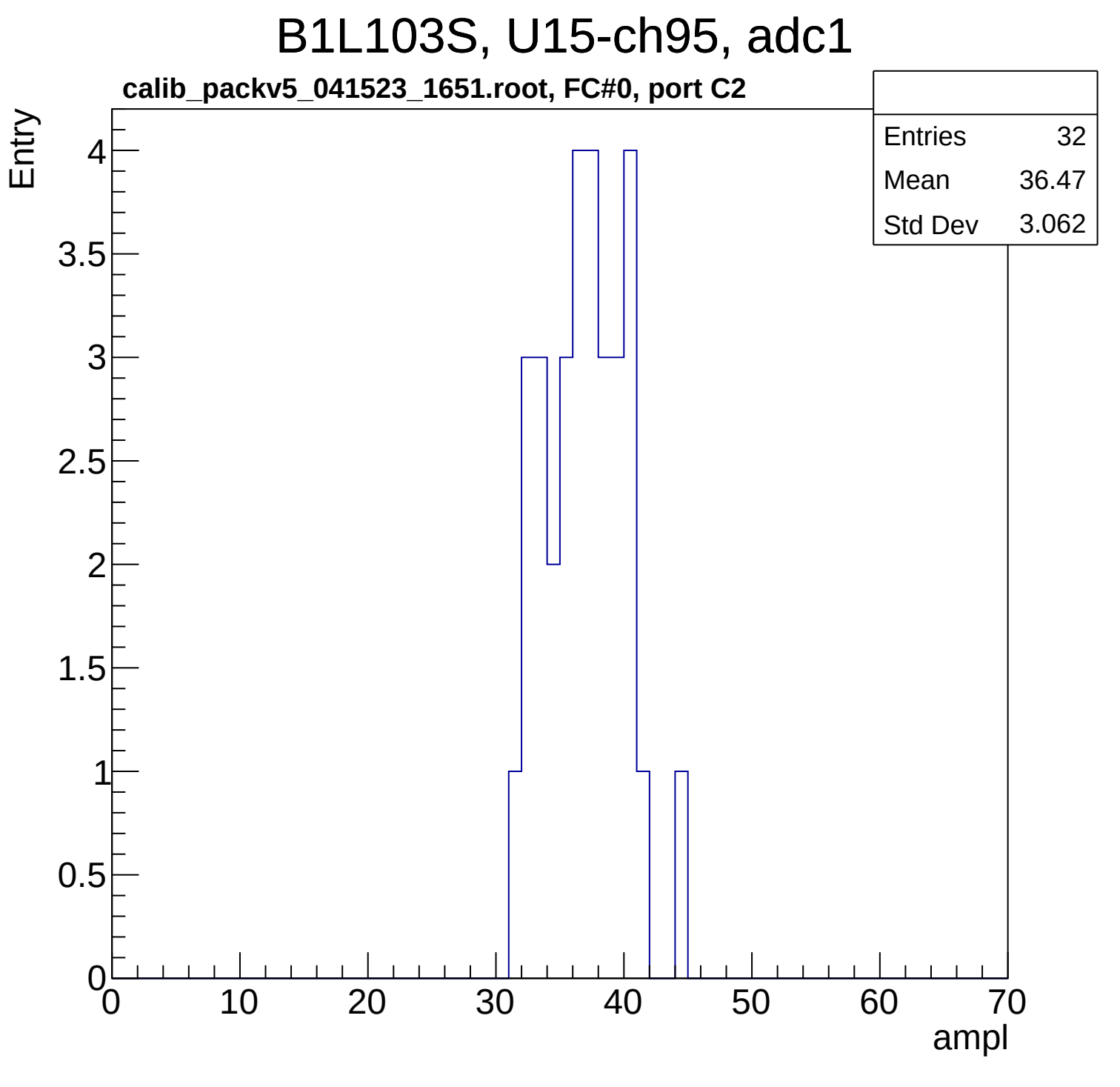
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch94, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.1
Std Dev 18.47
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch94, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 0
Std Dev 0
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch95, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 26.33
Std Dev 9.22
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch95, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 36.47
Std Dev 3.062
Entry
ampl
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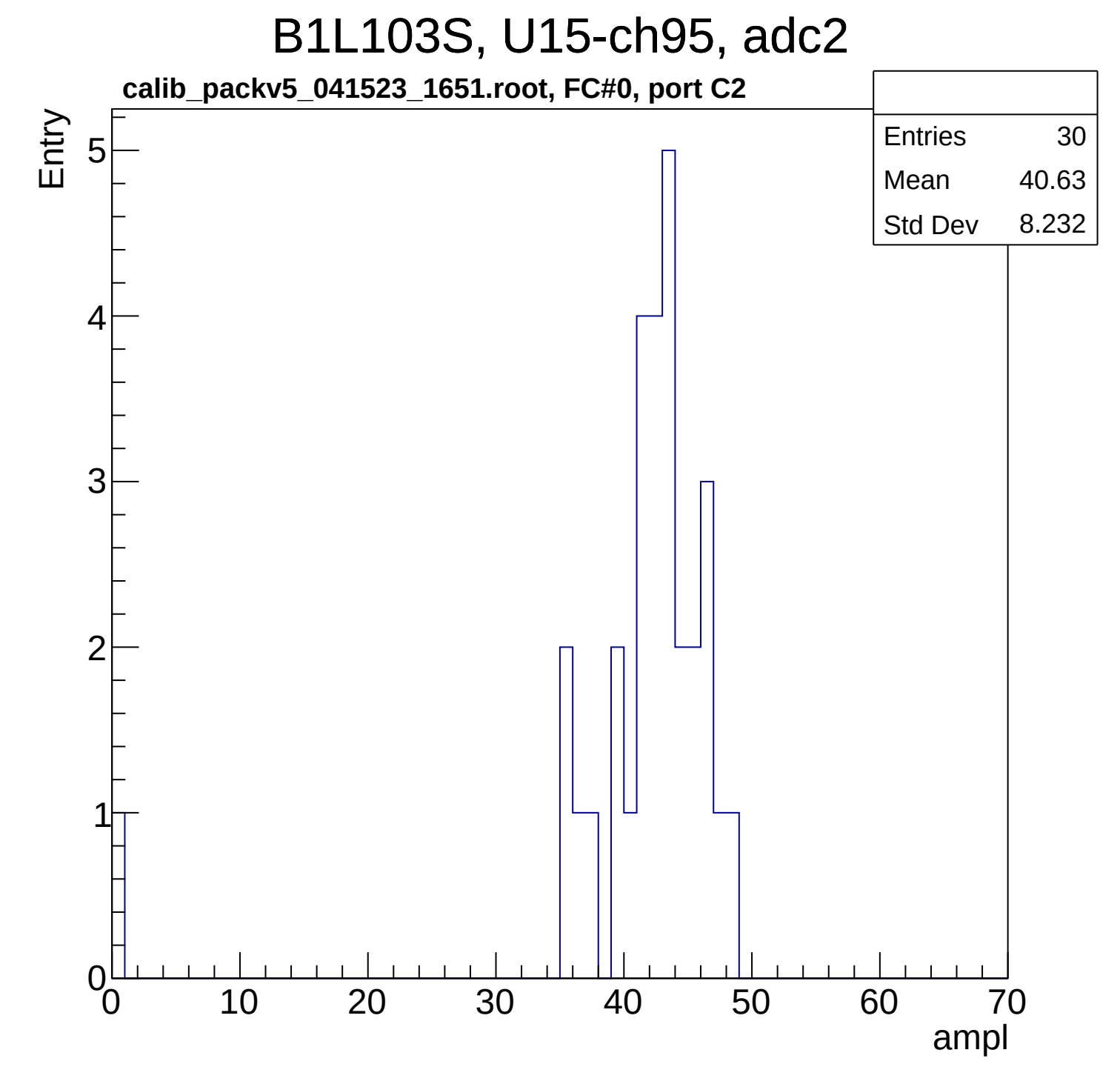
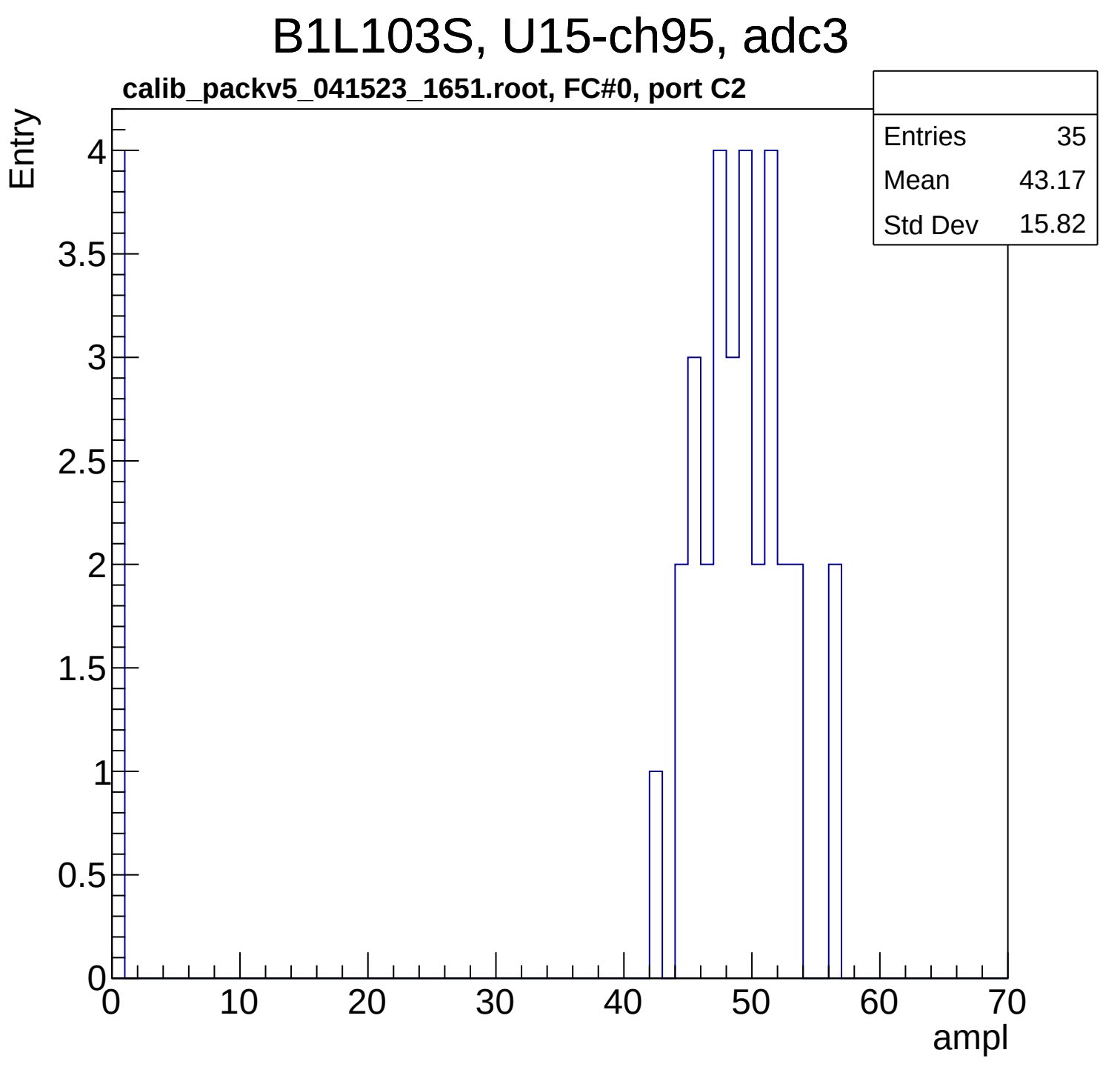
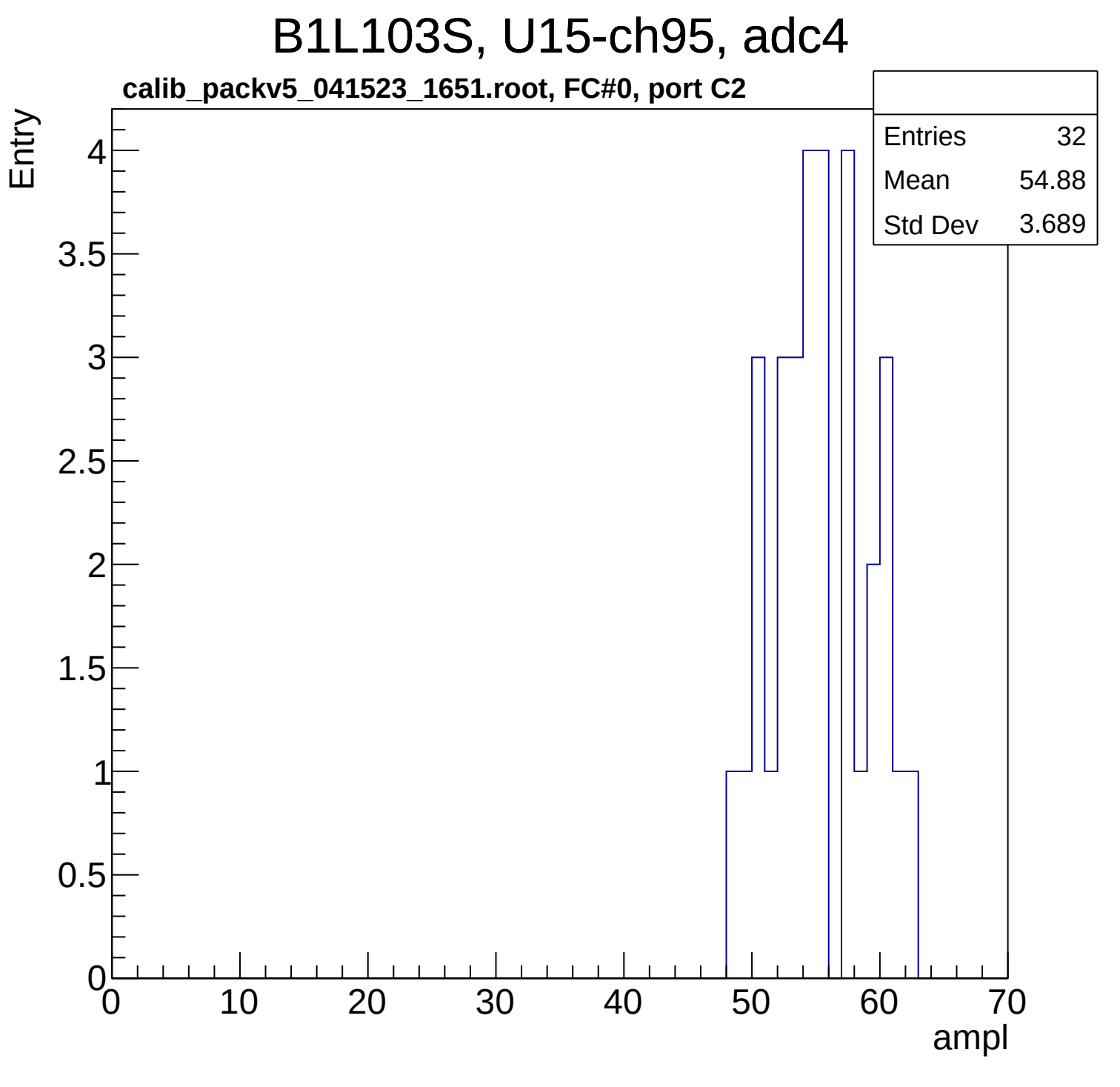
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch95, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 40.63
Std Dev 8.232
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch95, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 43.17
Std Dev 15.82
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch95, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 54.88
Std Dev 3.689
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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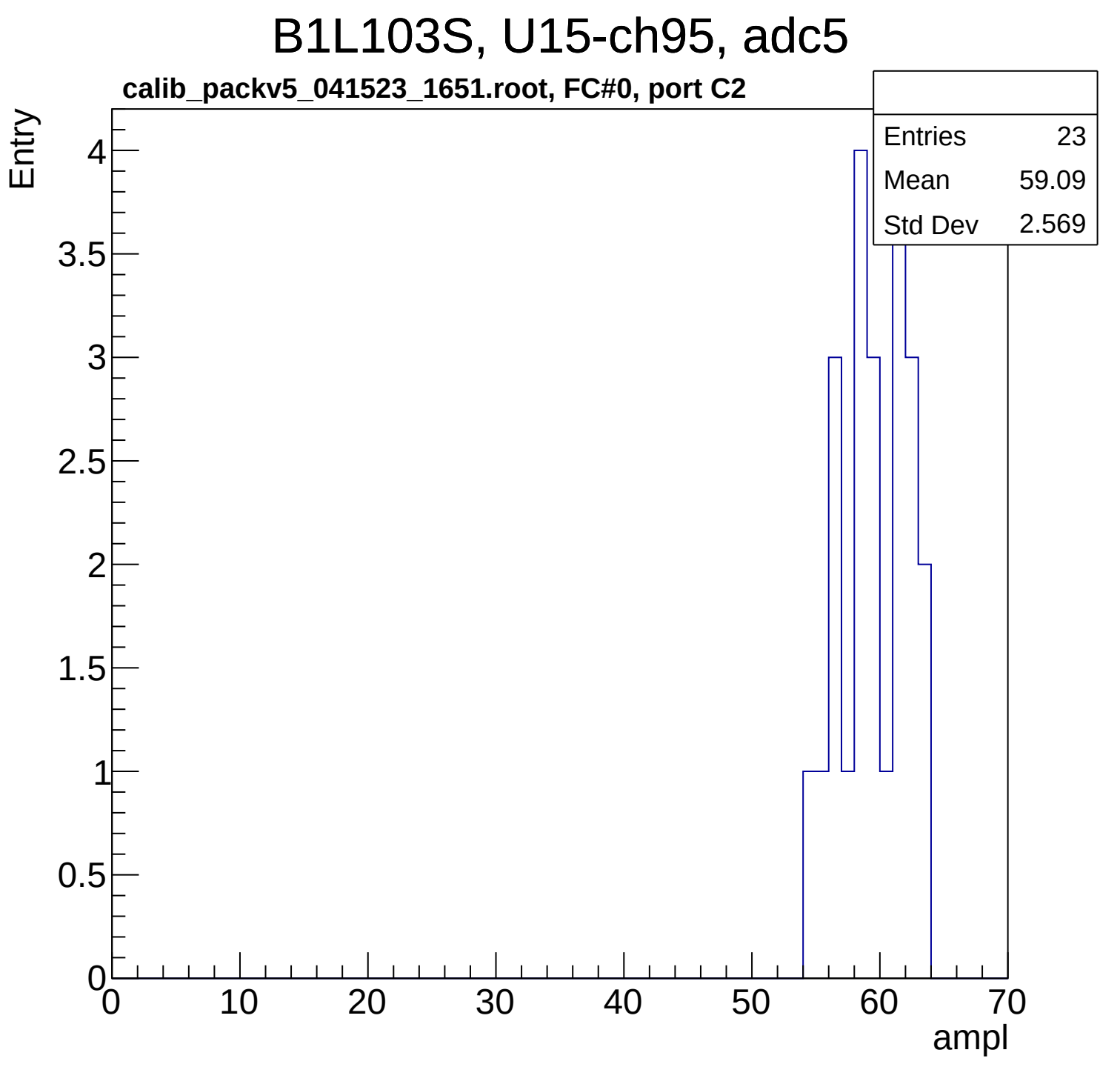
40
50
60
70


B1L103S, U15-ch95, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 59.09
Std Dev 2.569
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
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40
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60
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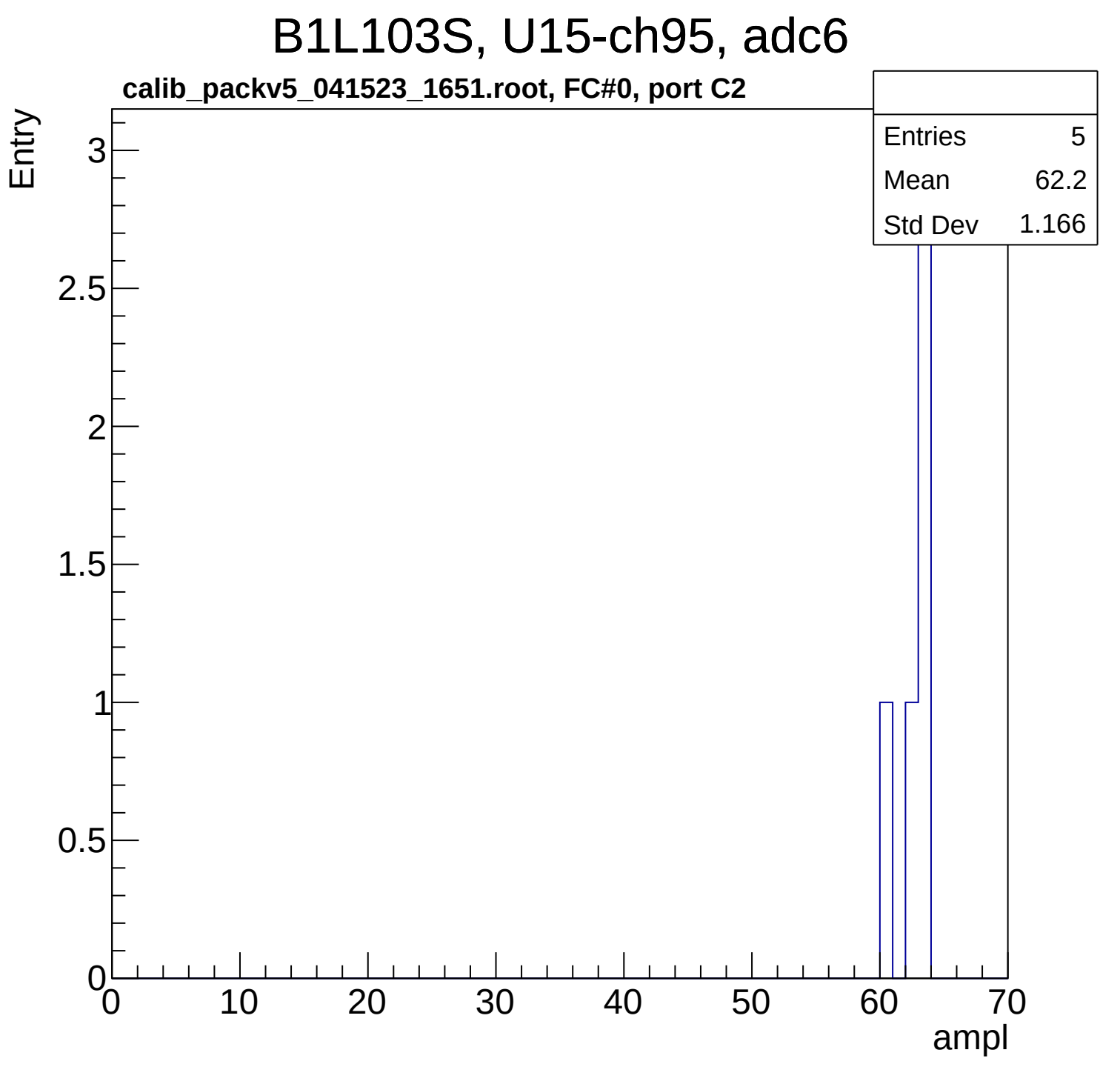
B1L103S, U15-ch95, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.2
Std Dev 1.166
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
50
60
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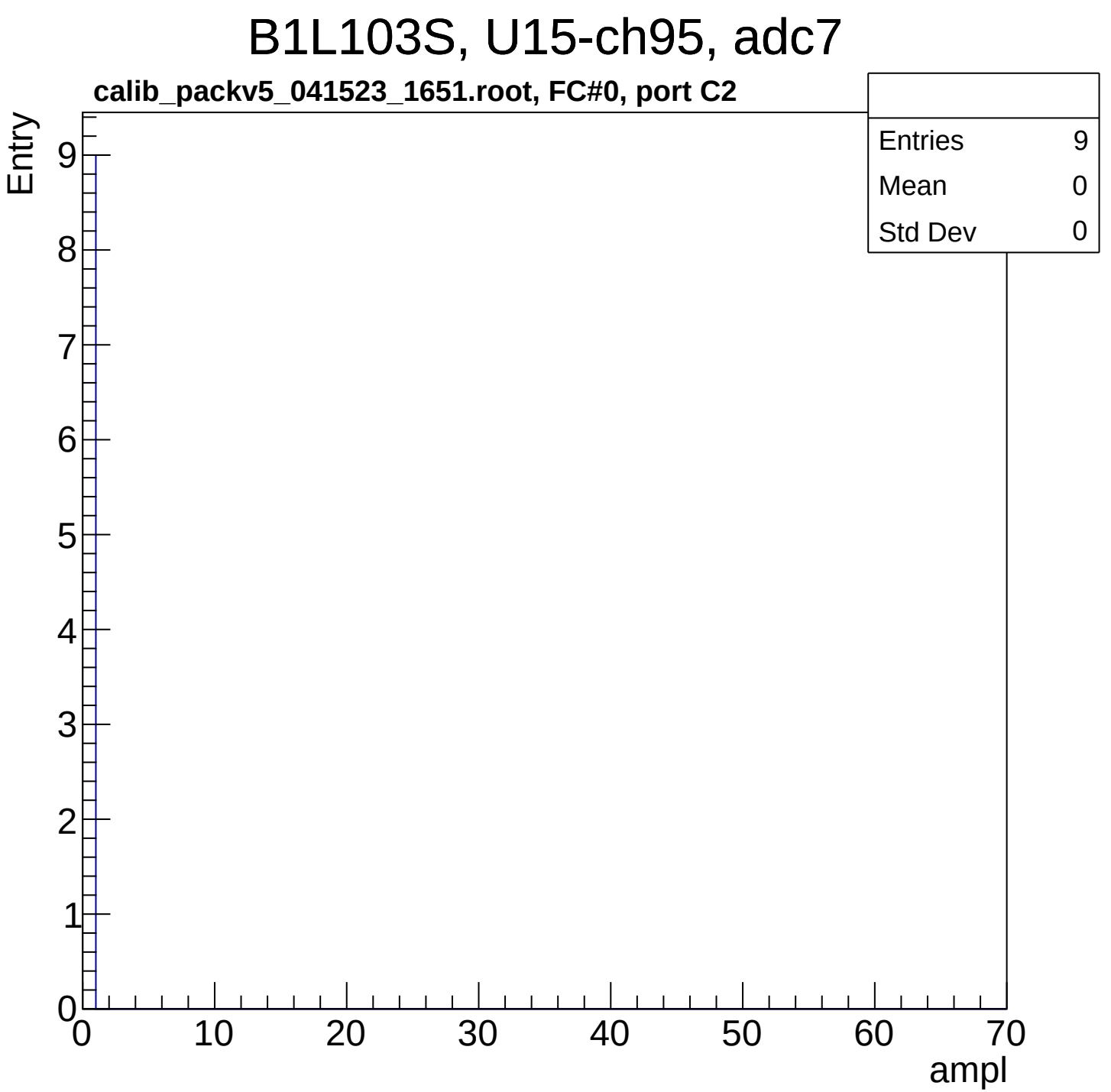
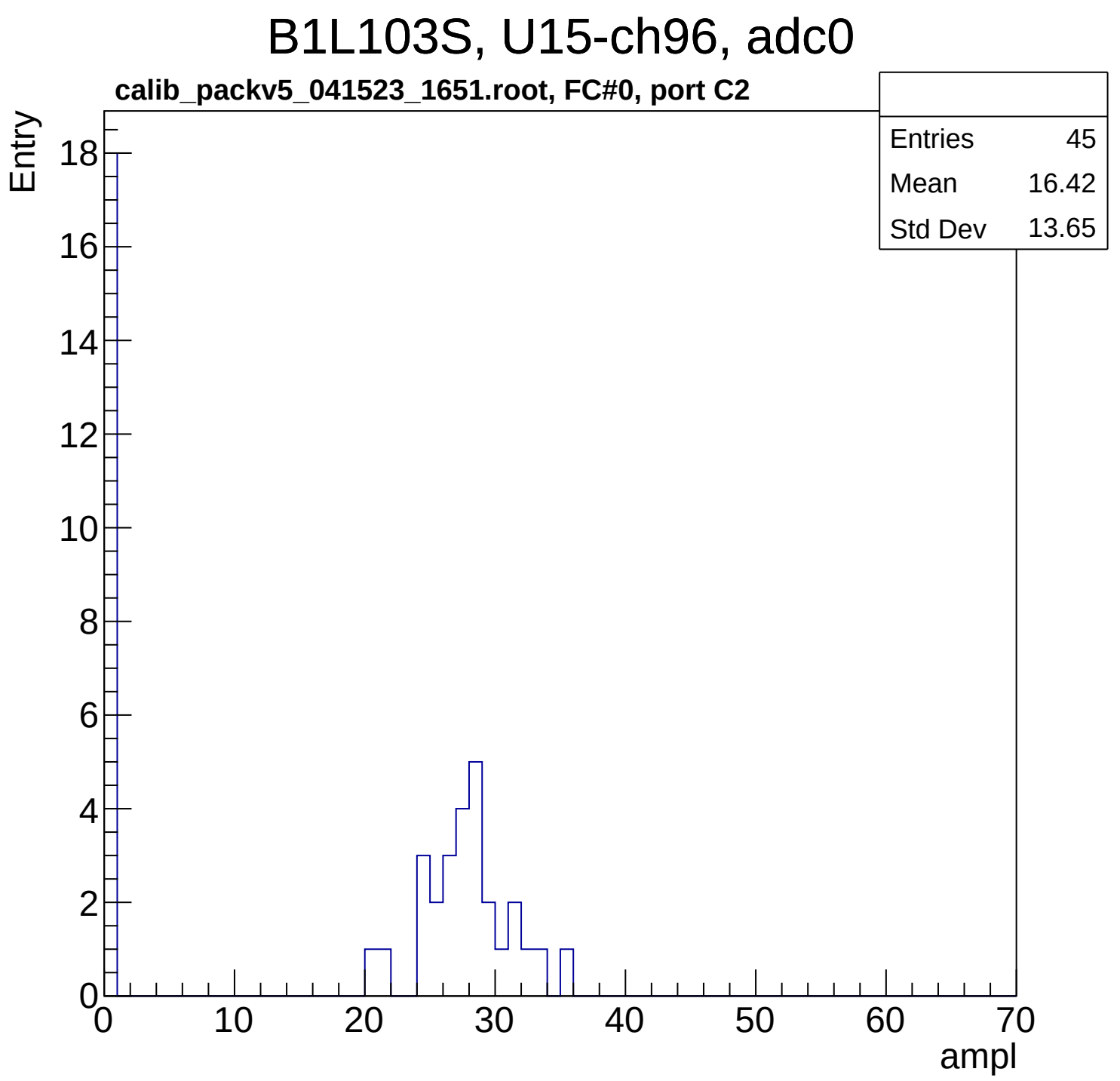
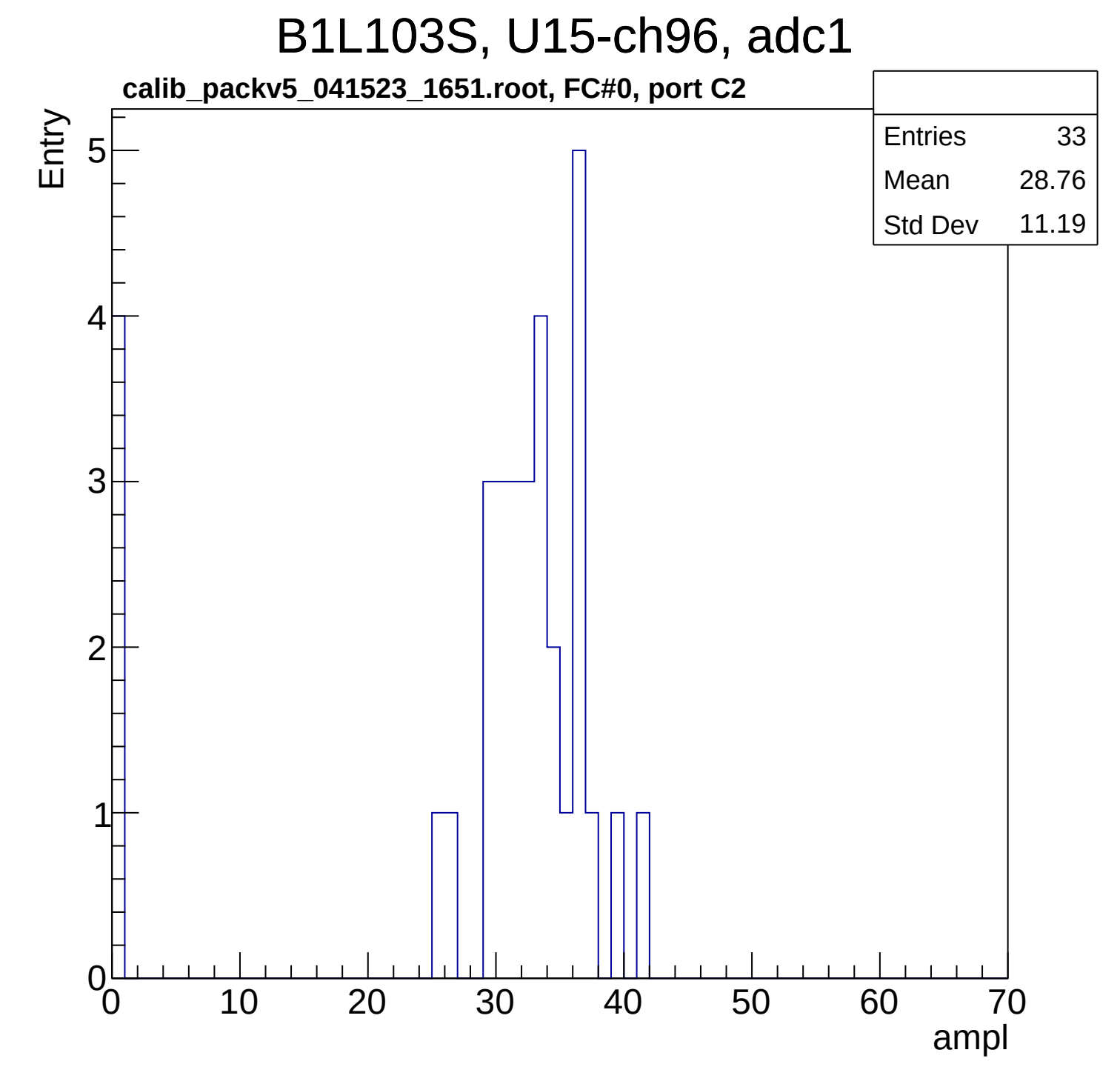
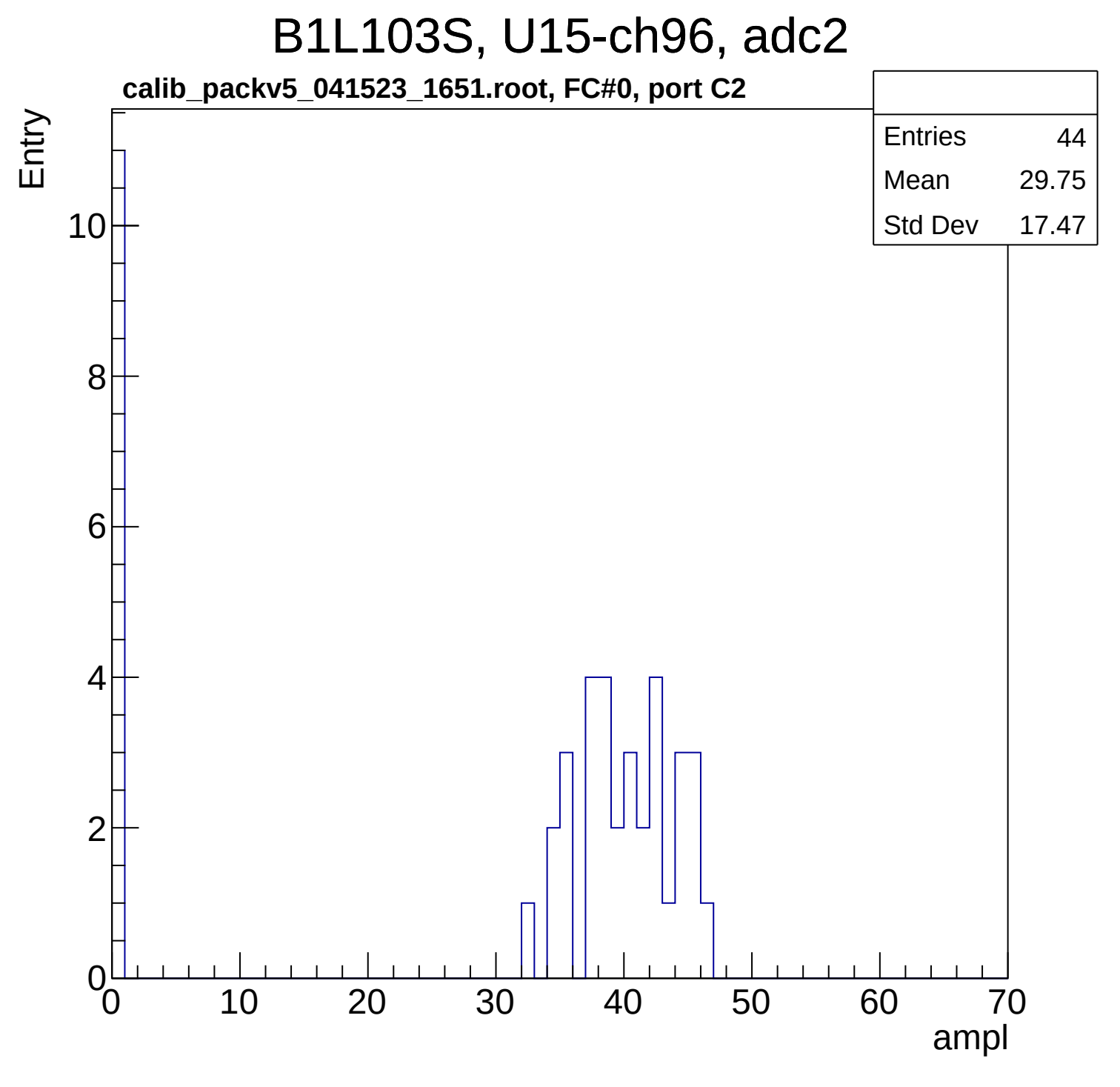
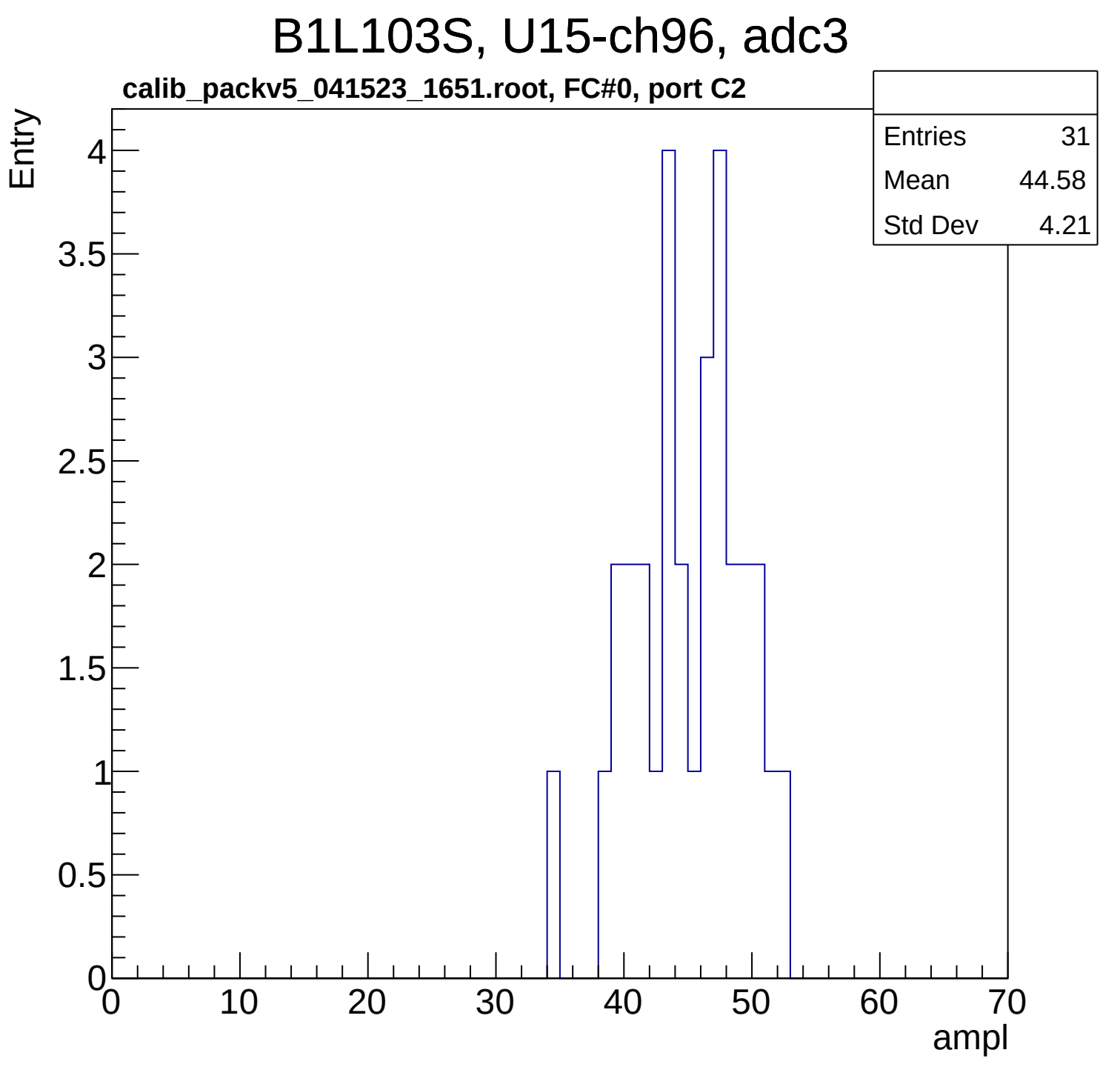

B1L103S, U15-ch95, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 0
Std Dev 0
Entry
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch96, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 16.42
Std Dev 13.65
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch96, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 28.76
Std Dev 11.19
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch96, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 29.75
Std Dev 17.47
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch96, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 44.58
Std Dev 4.21
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
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40
50
60
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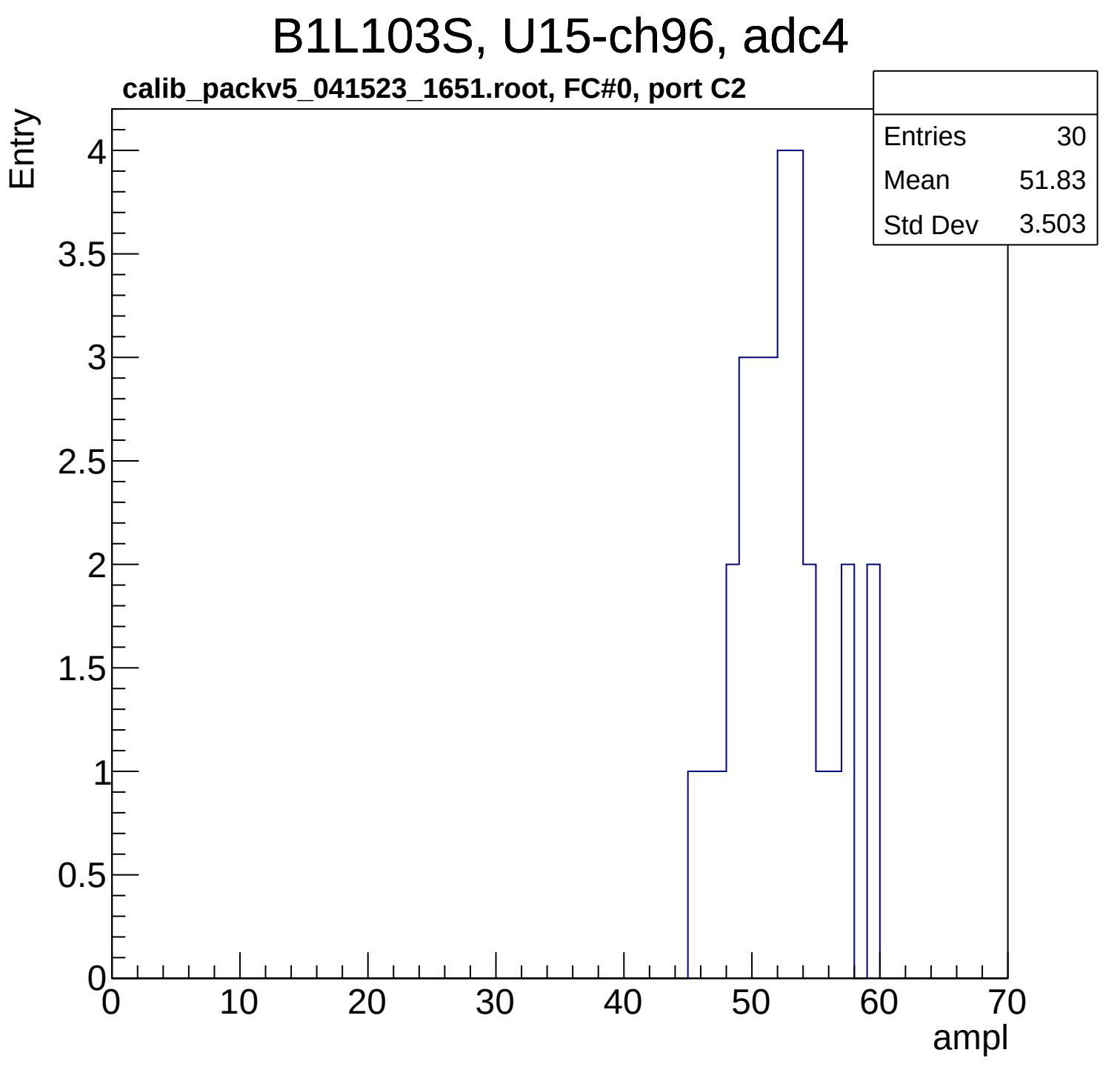
B1L103S, U15-ch96, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 51.83
Std Dev 3.503
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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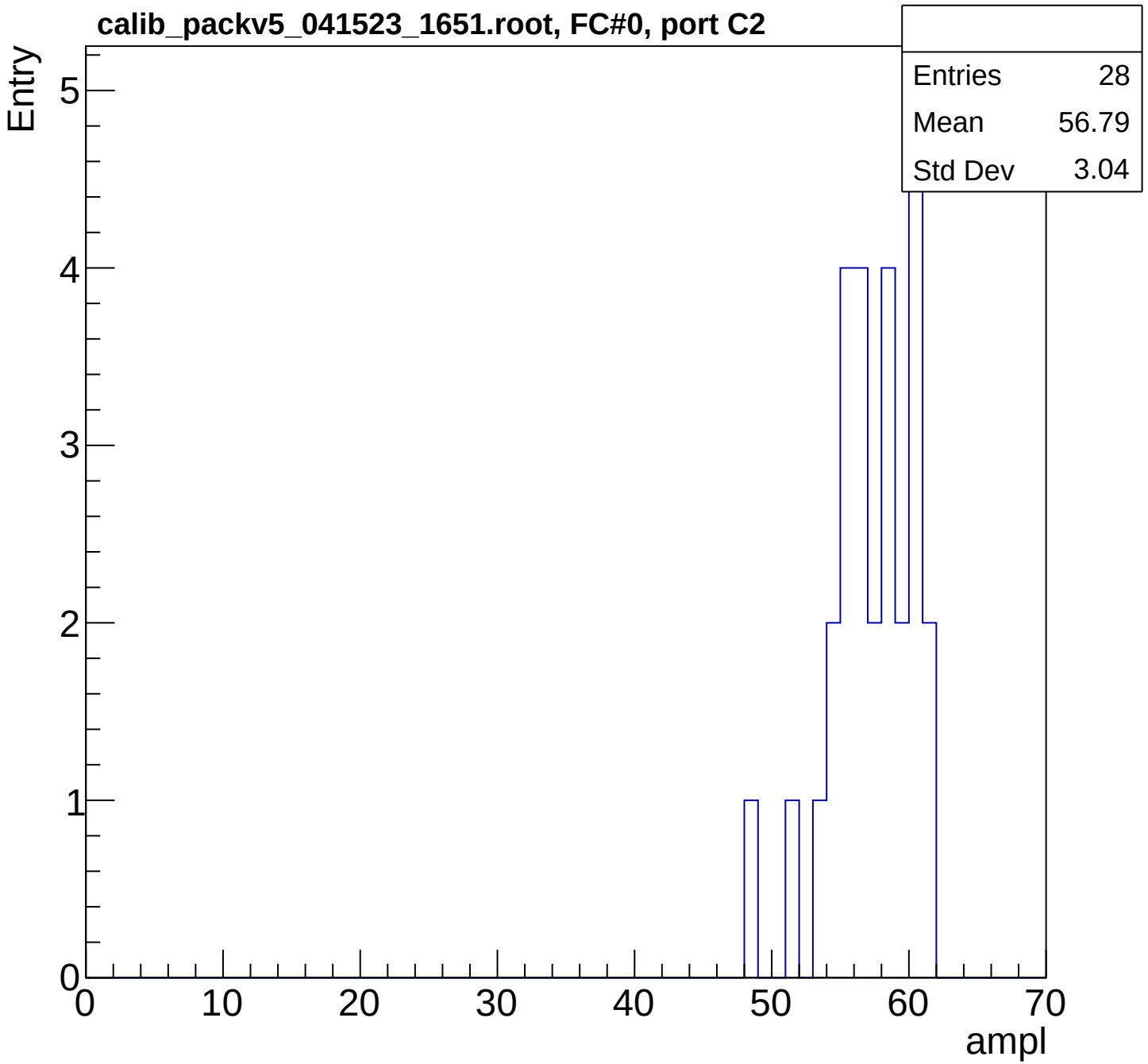
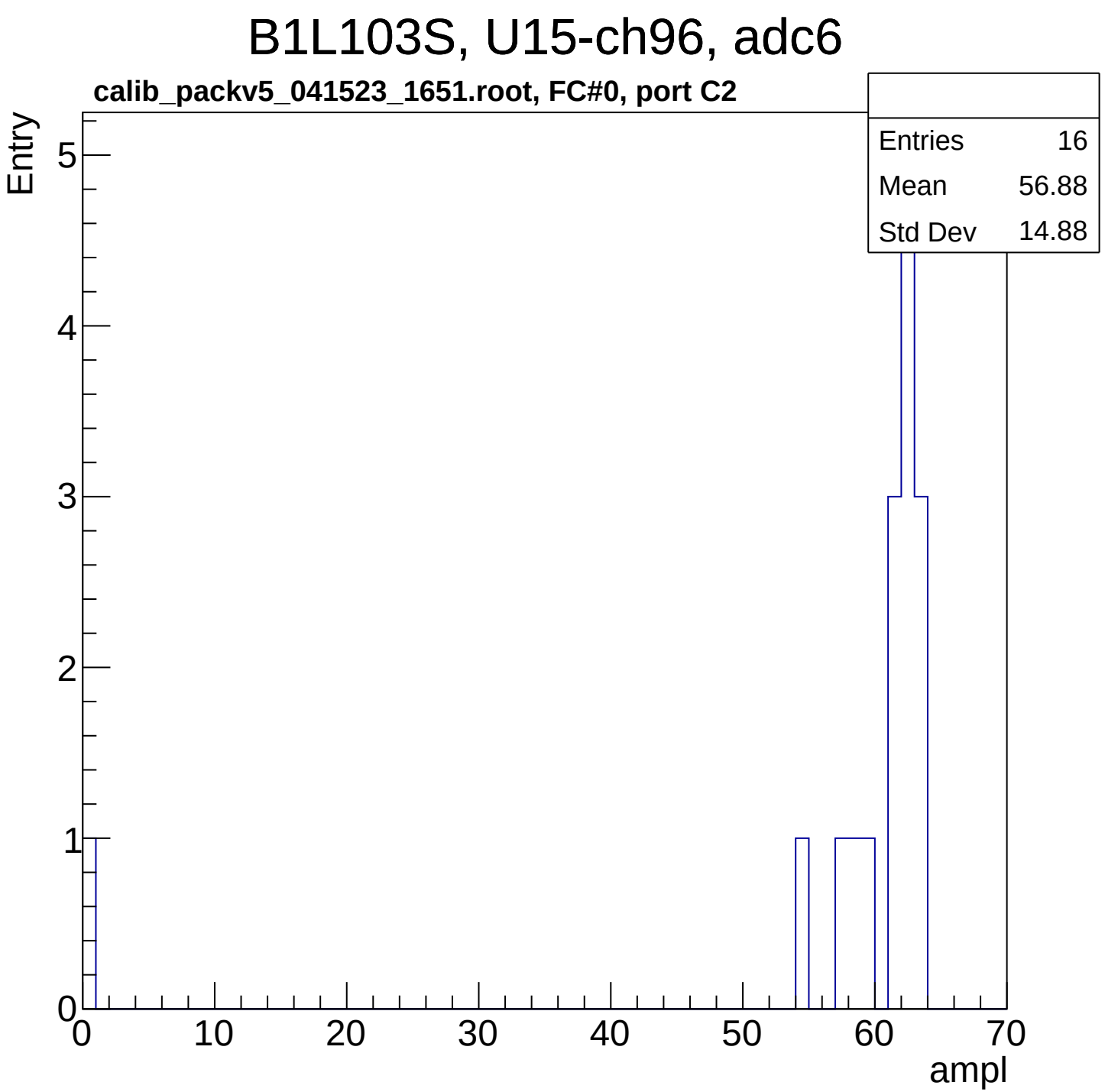
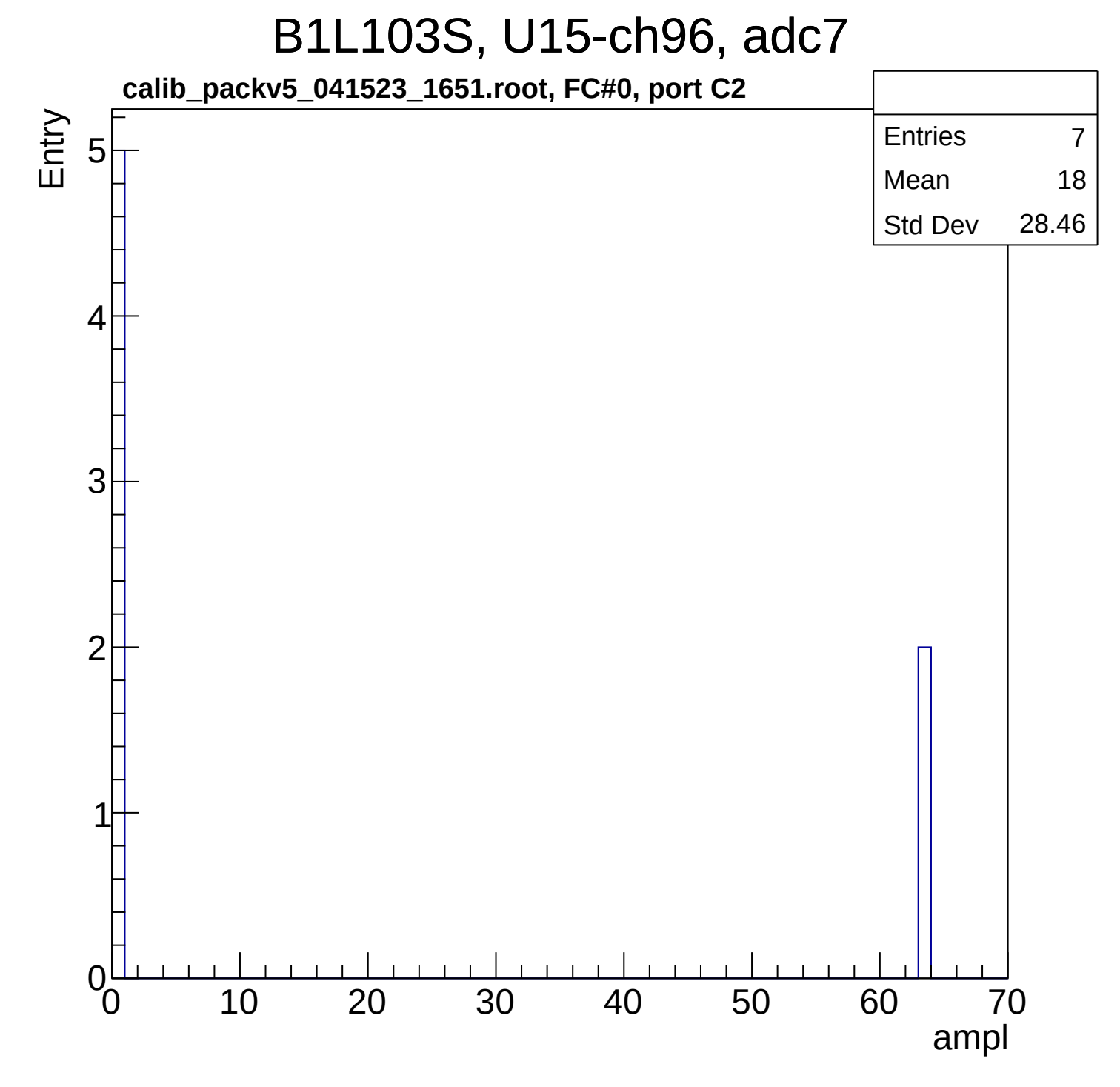
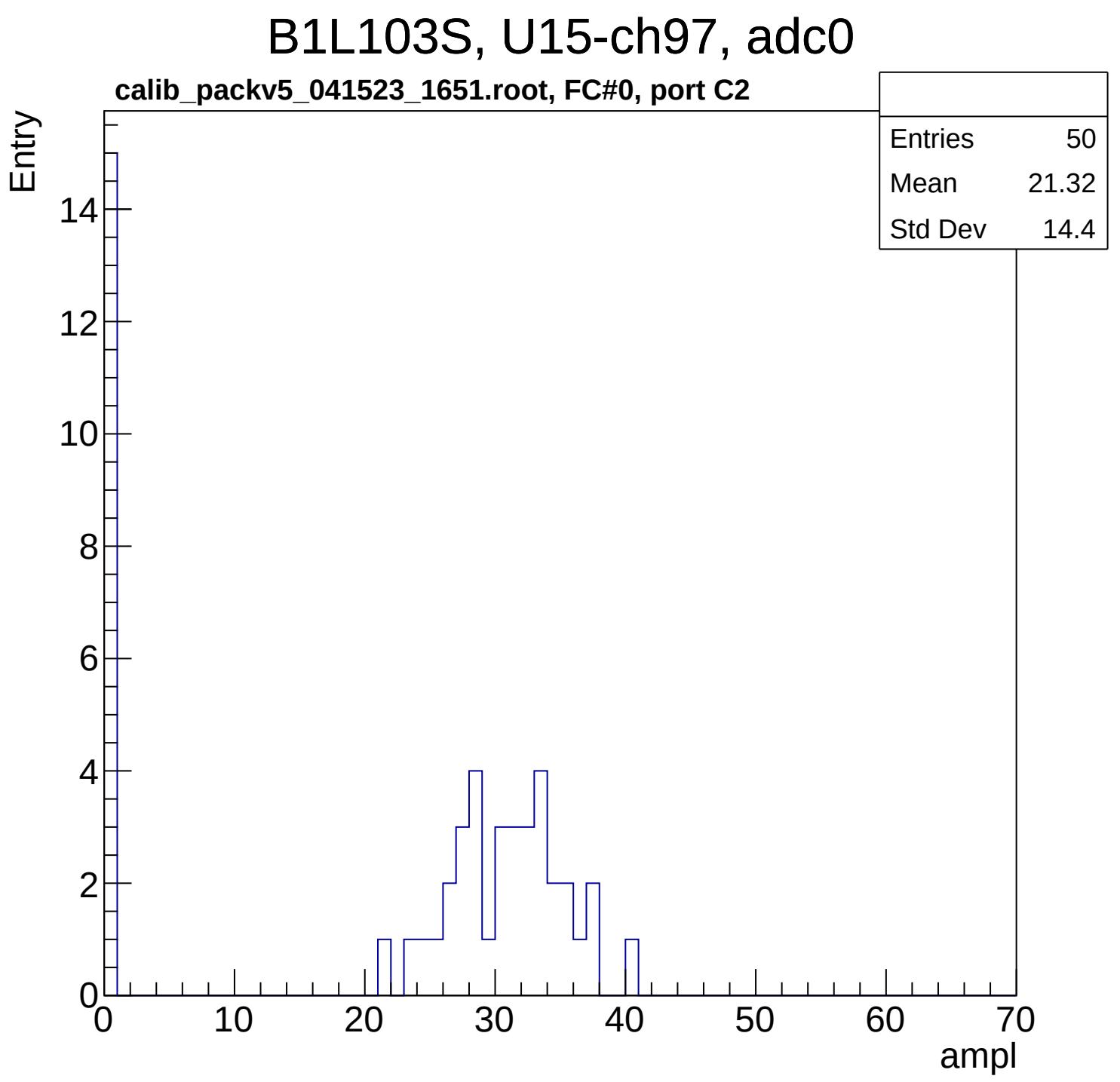

B1L103S, U15-ch96, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 56.79
Std Dev 3.04
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch96, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 56.88
Std Dev 14.88
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch96, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 18
Std Dev 28.46
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch97, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 21.32
Std Dev 14.4
Entry
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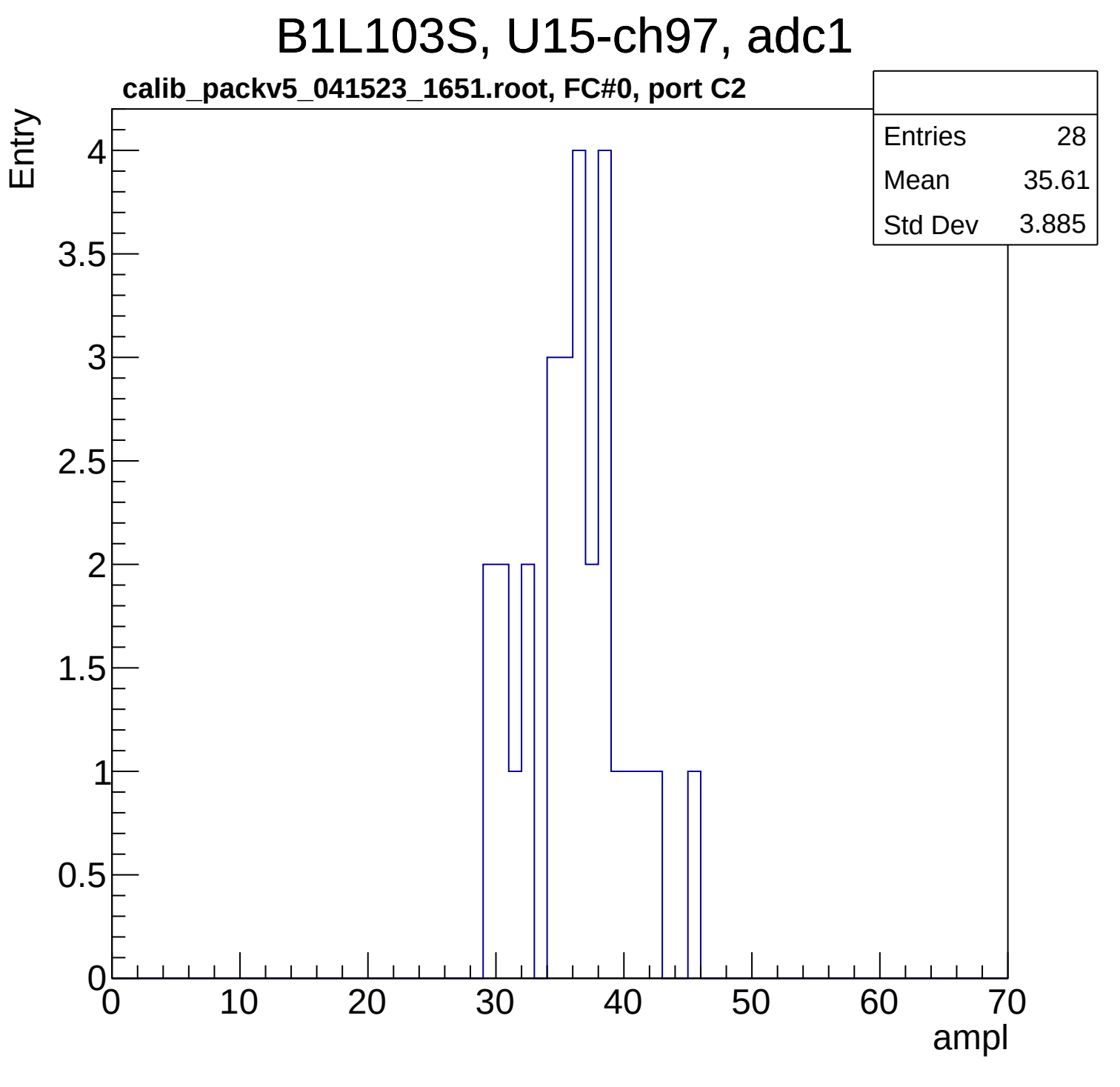
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch97, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 35.61
Std Dev 3.885
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
10
20
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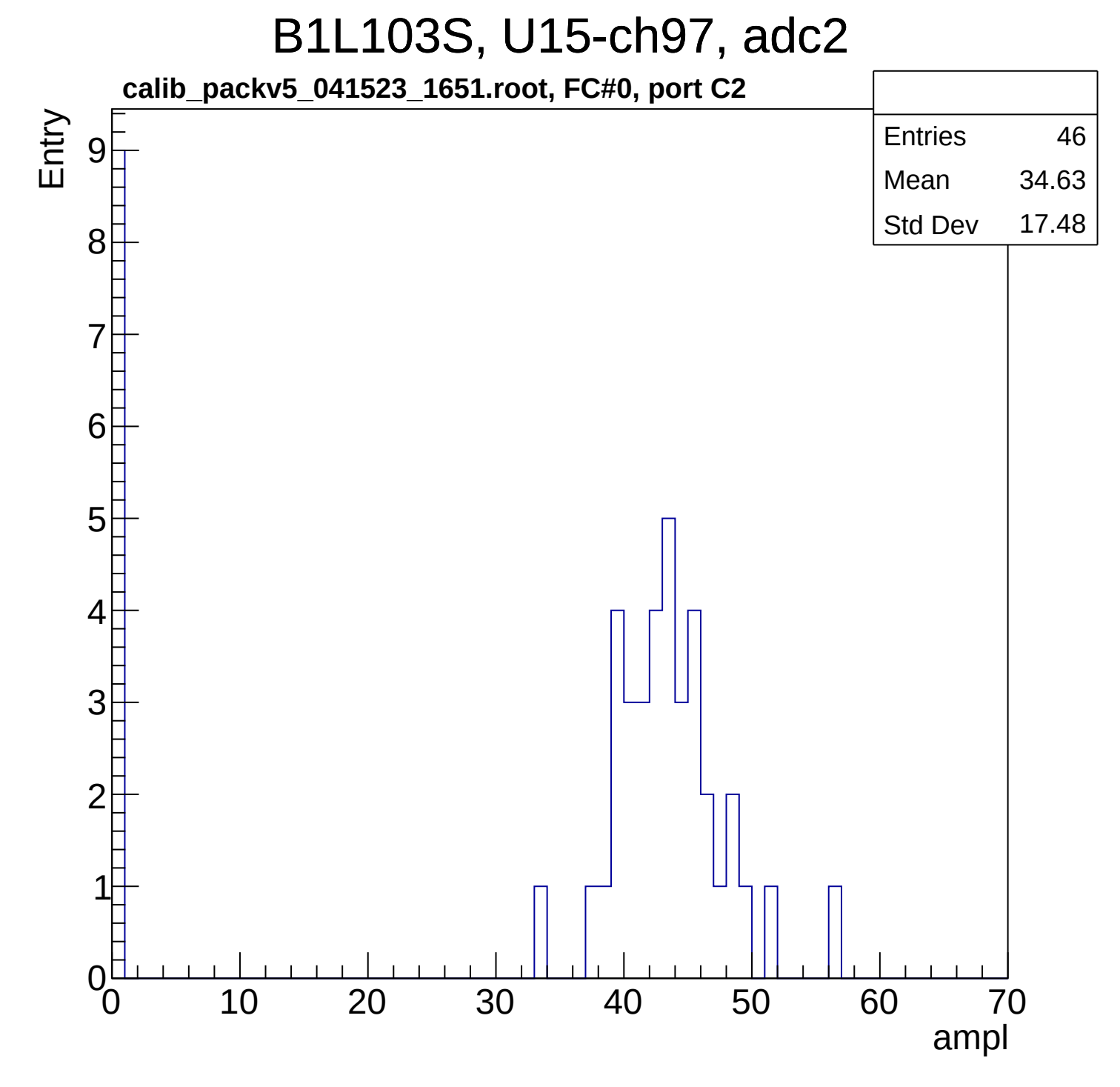
40
50
60
70


B1L103S, U15-ch97, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 34.63
Std Dev 17.48
Entry
ampl
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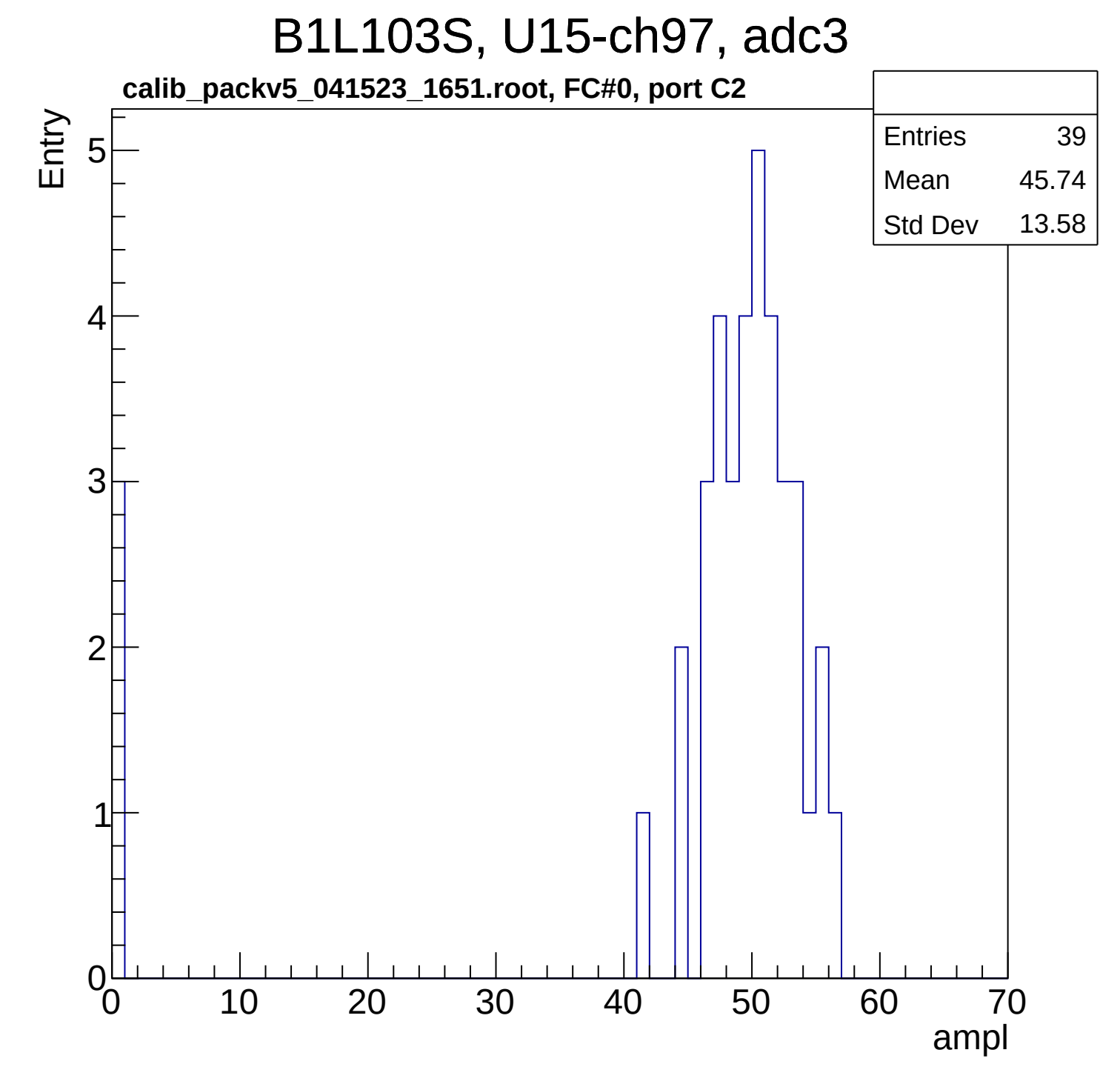
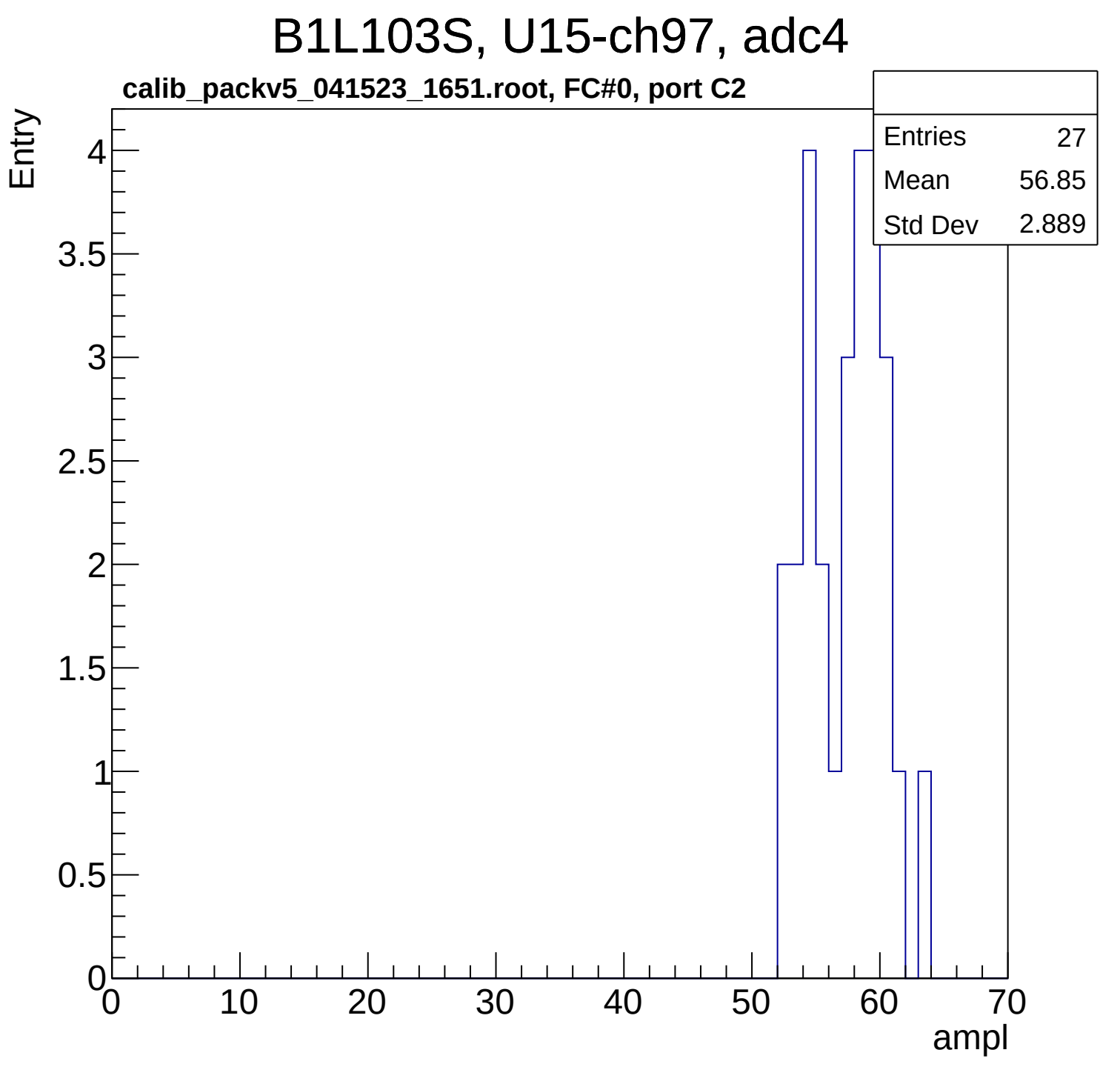
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U15-ch97, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 45.74
Std Dev 13.58
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch97, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 56.85
Std Dev 2.889
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
50
60
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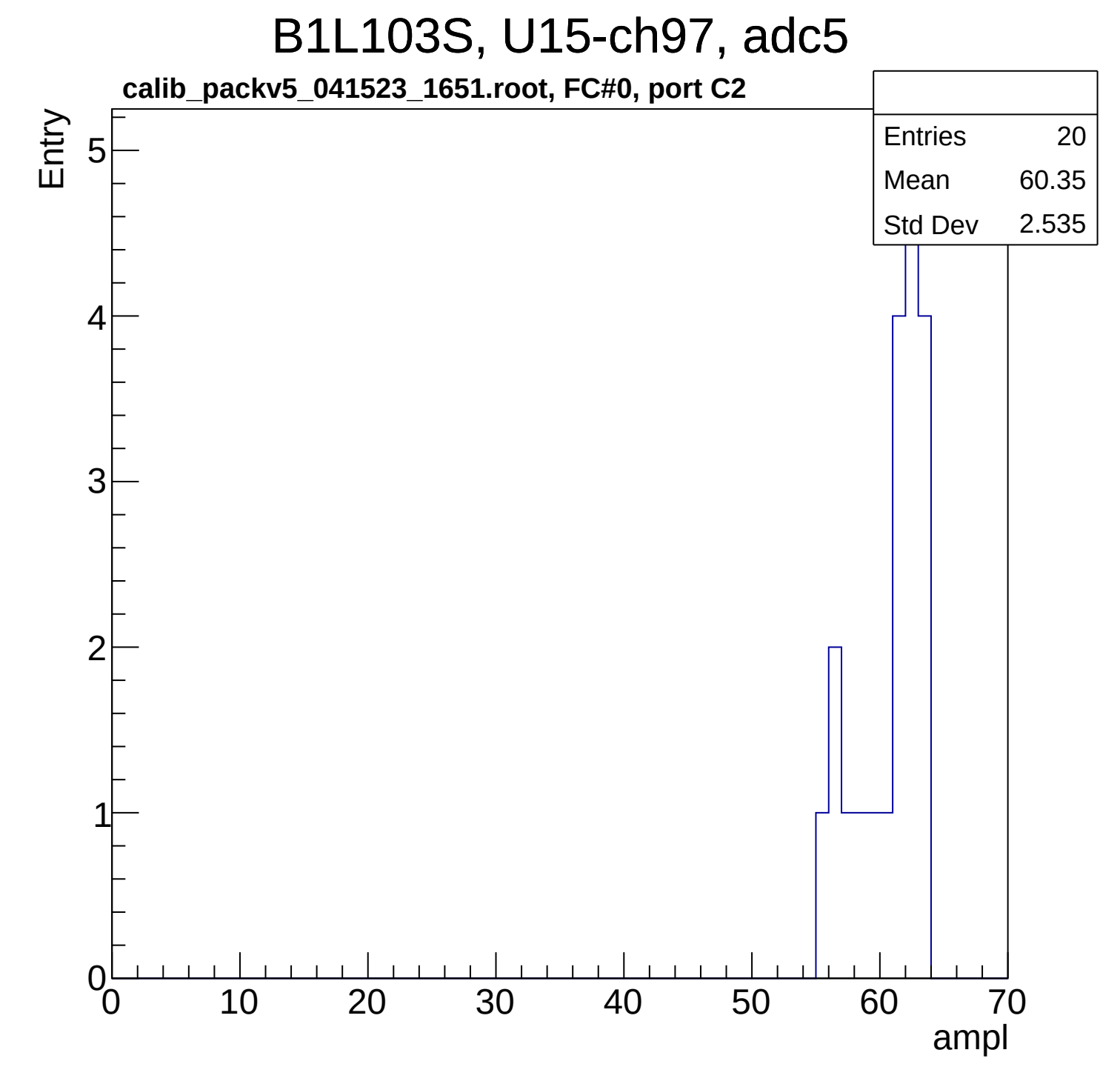
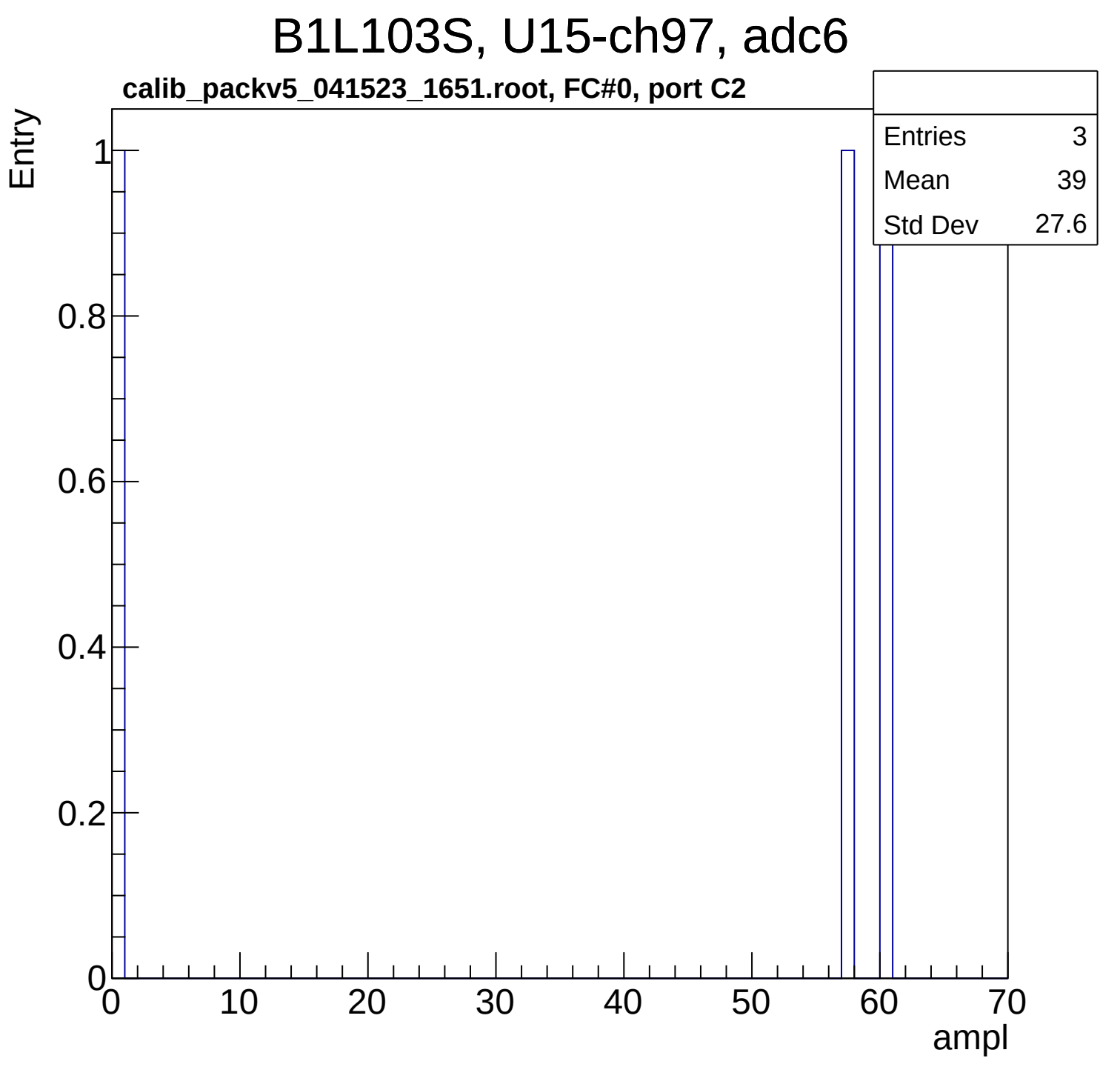

B1L103S, U15-ch97, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 60.35
Std Dev 2.535
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch97, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 39
Std Dev 27.6
Entry
ampl
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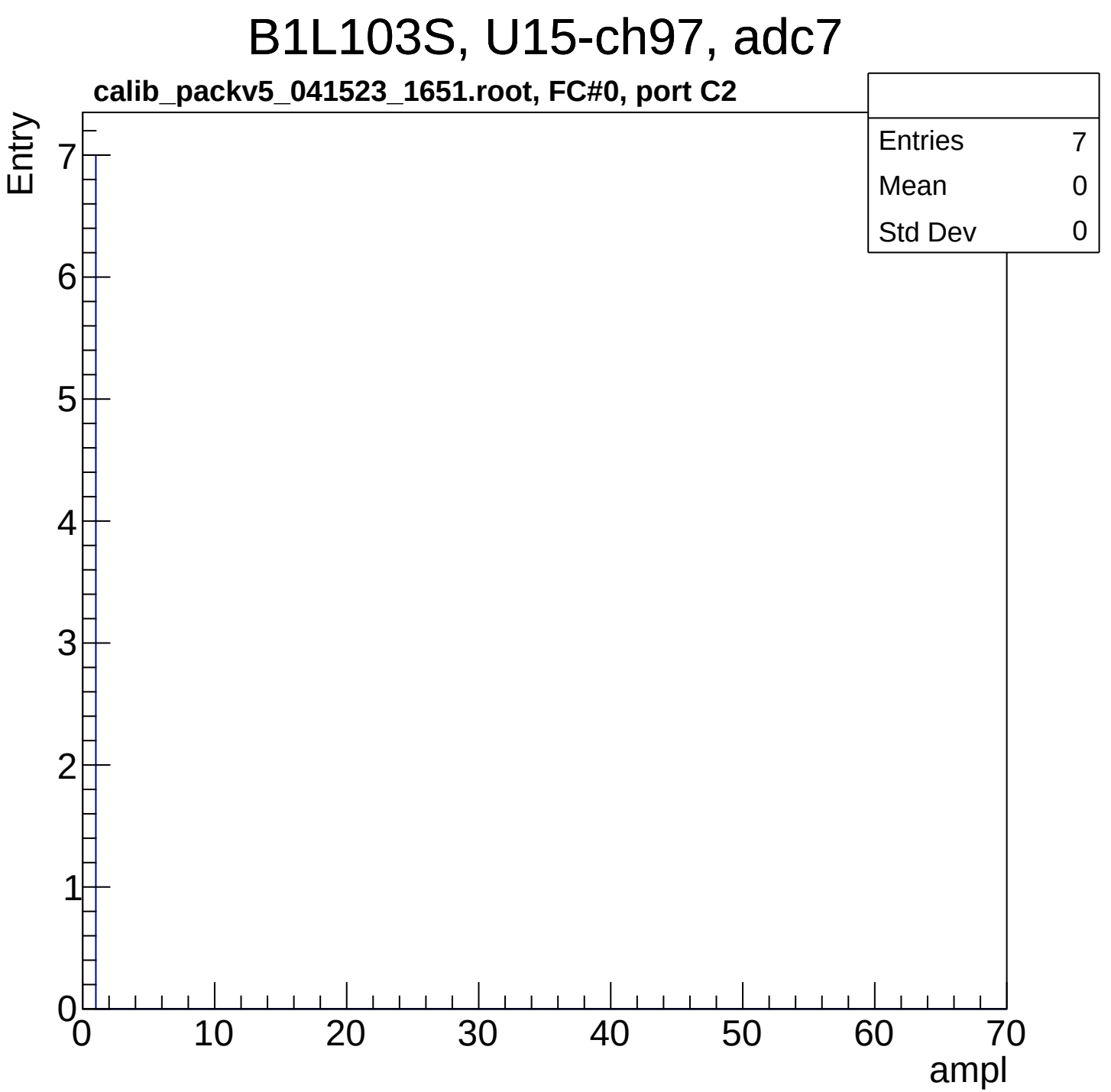
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L103S, U15-ch97, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 0
Std Dev 0
Entry
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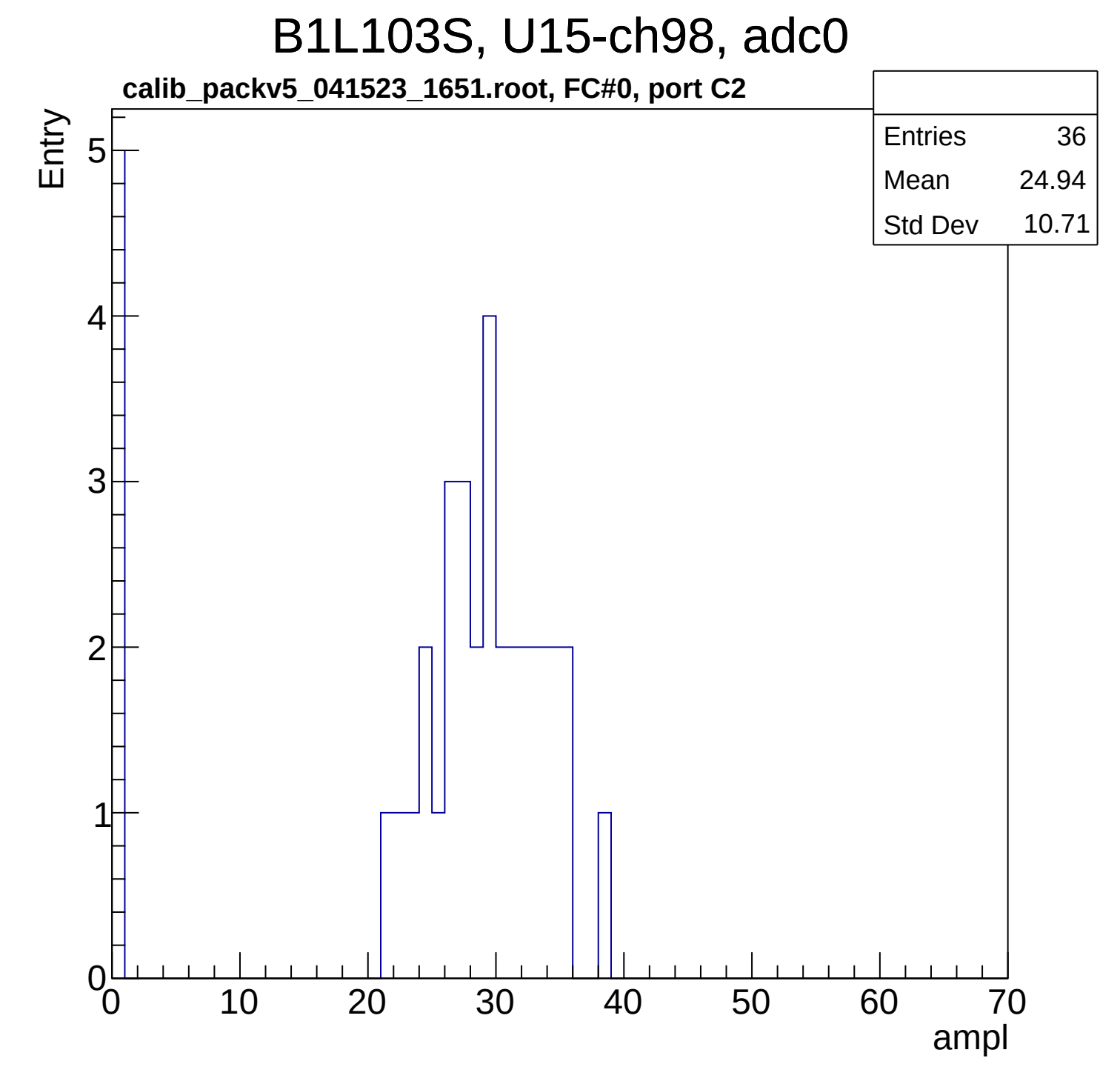
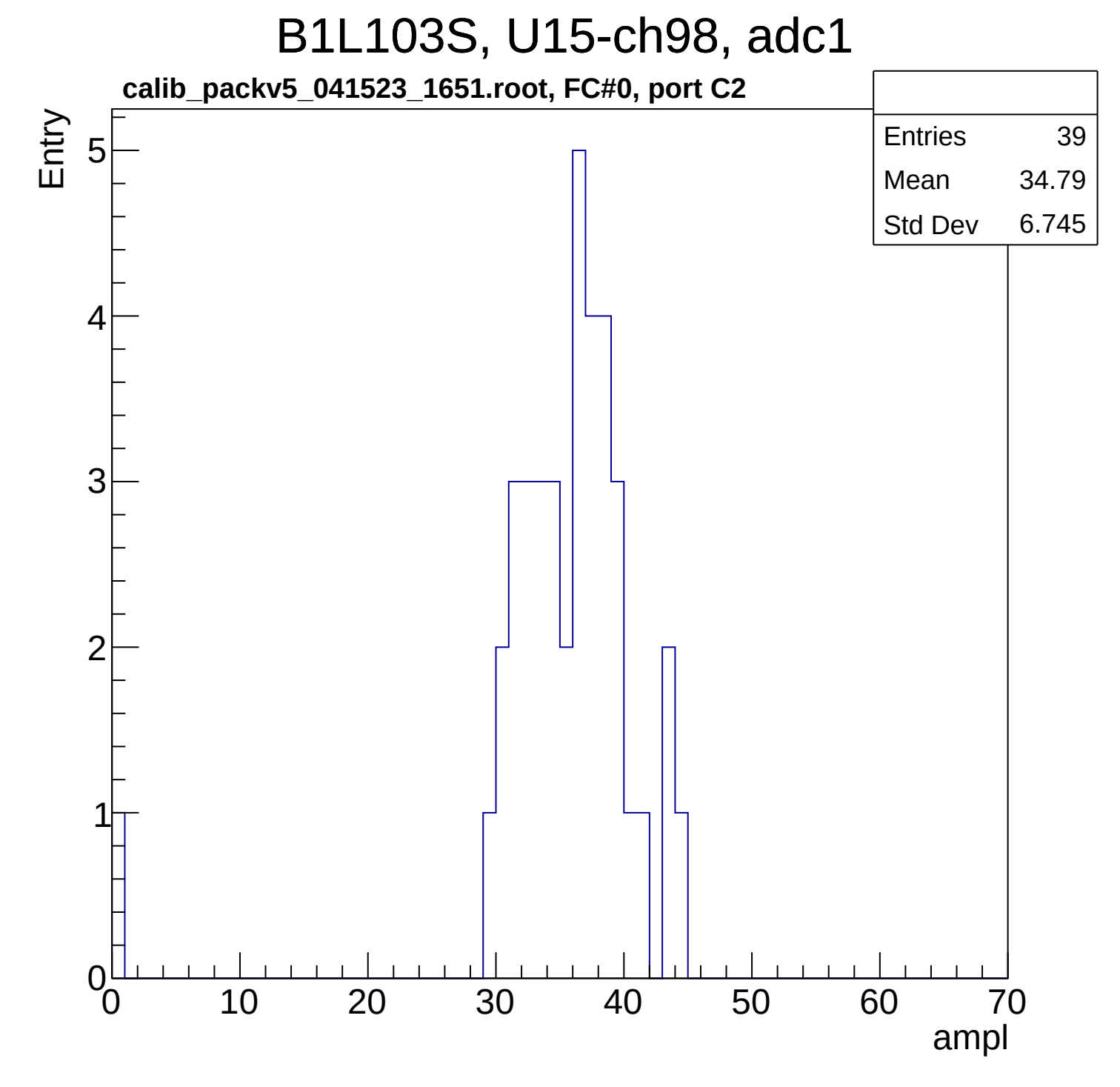
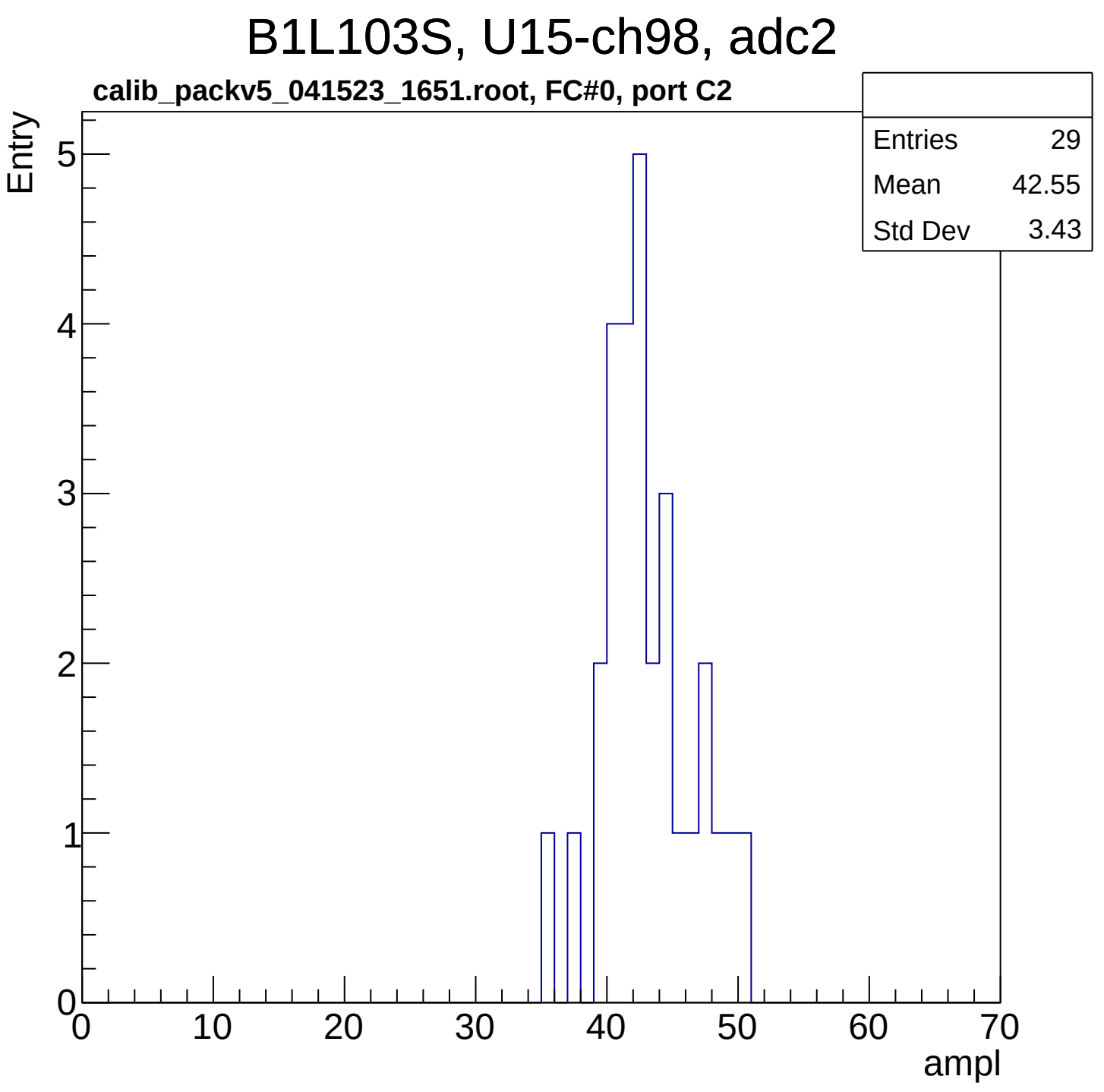
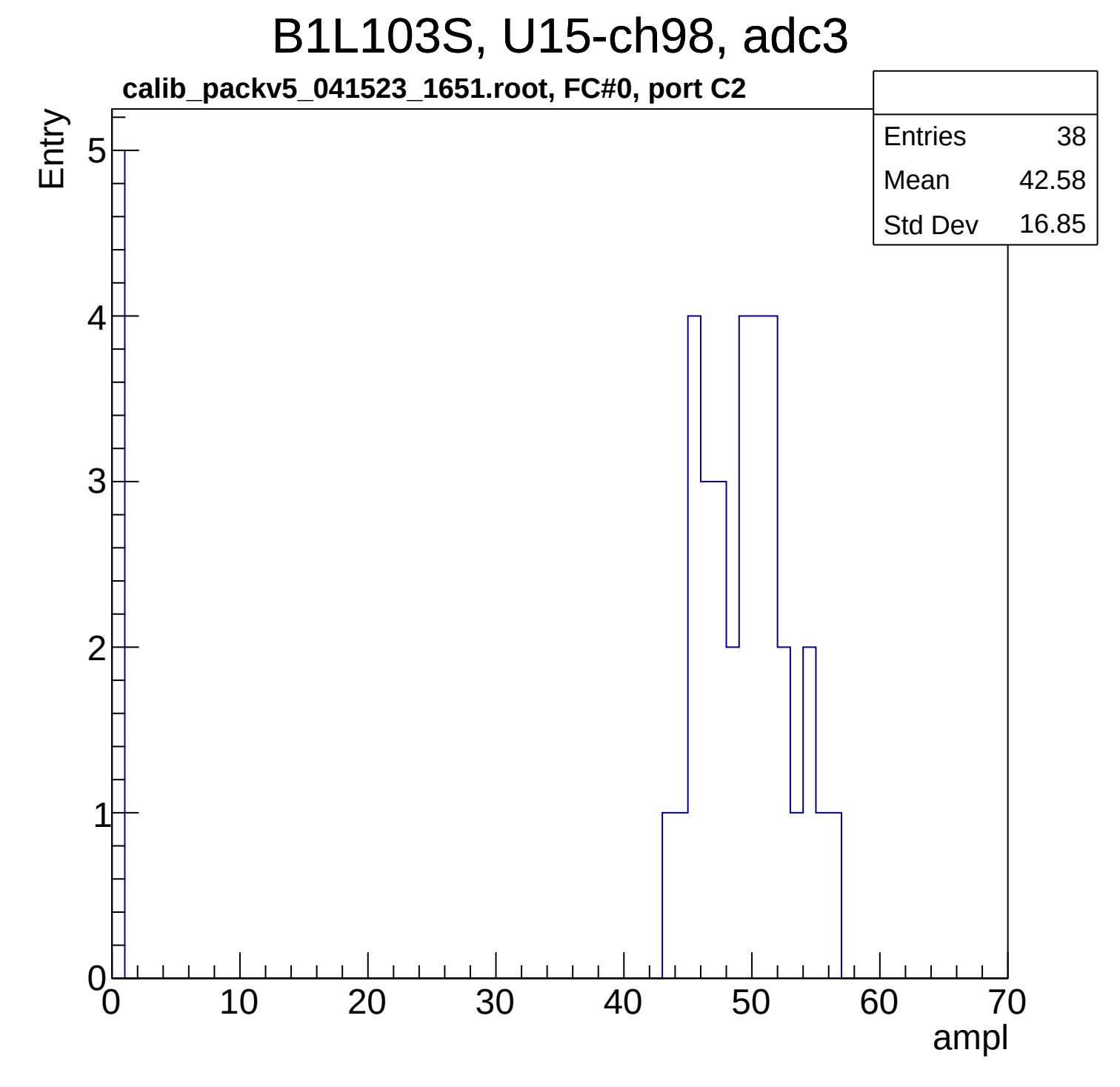
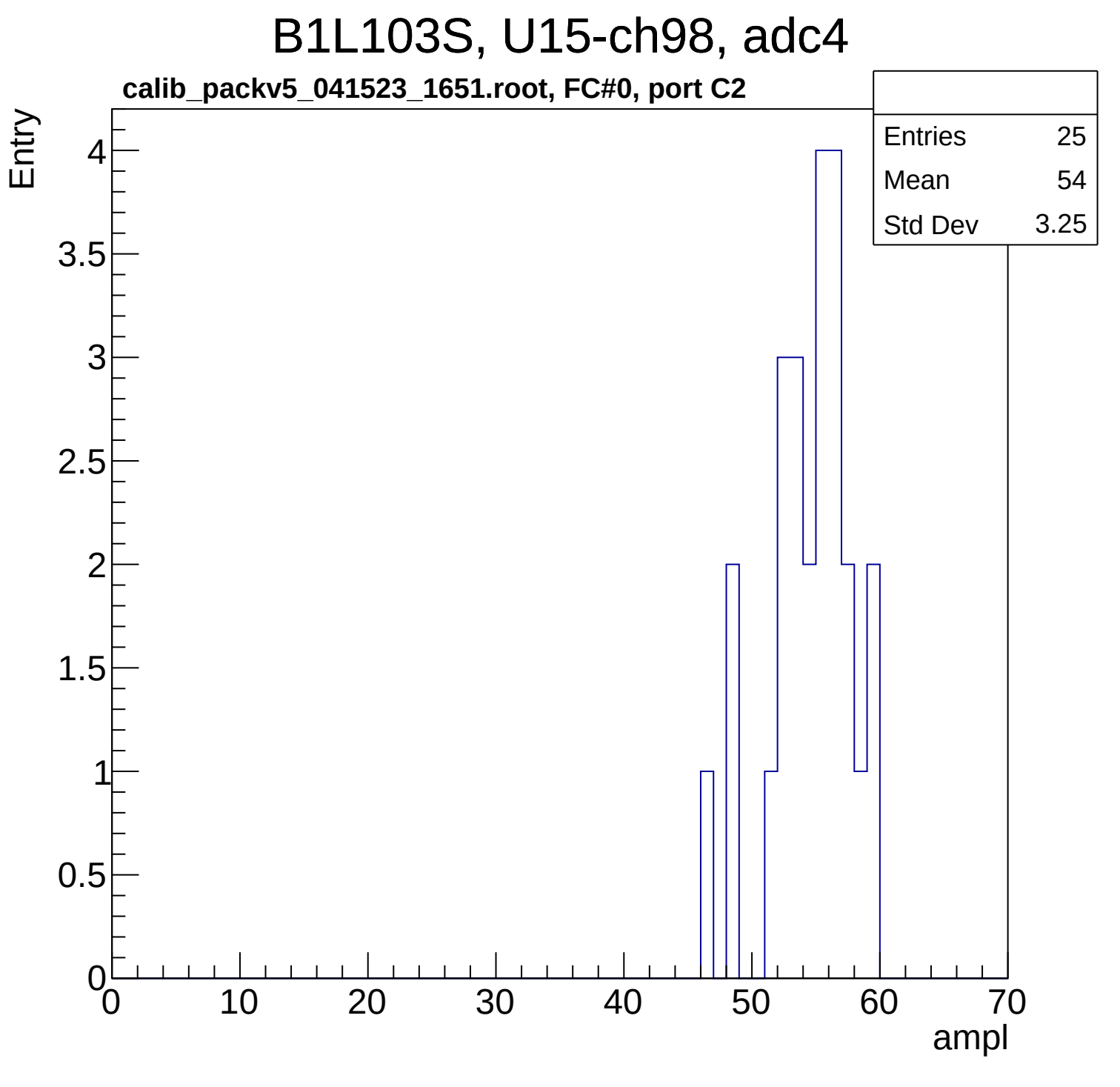
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch98, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 24.94
Std Dev 10.71
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch98, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 34.79
Std Dev 6.745
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch98, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 42.55
Std Dev 3.43
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch98, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 42.58
Std Dev 16.85
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch98, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 54
Std Dev 3.25
Entry
ampl
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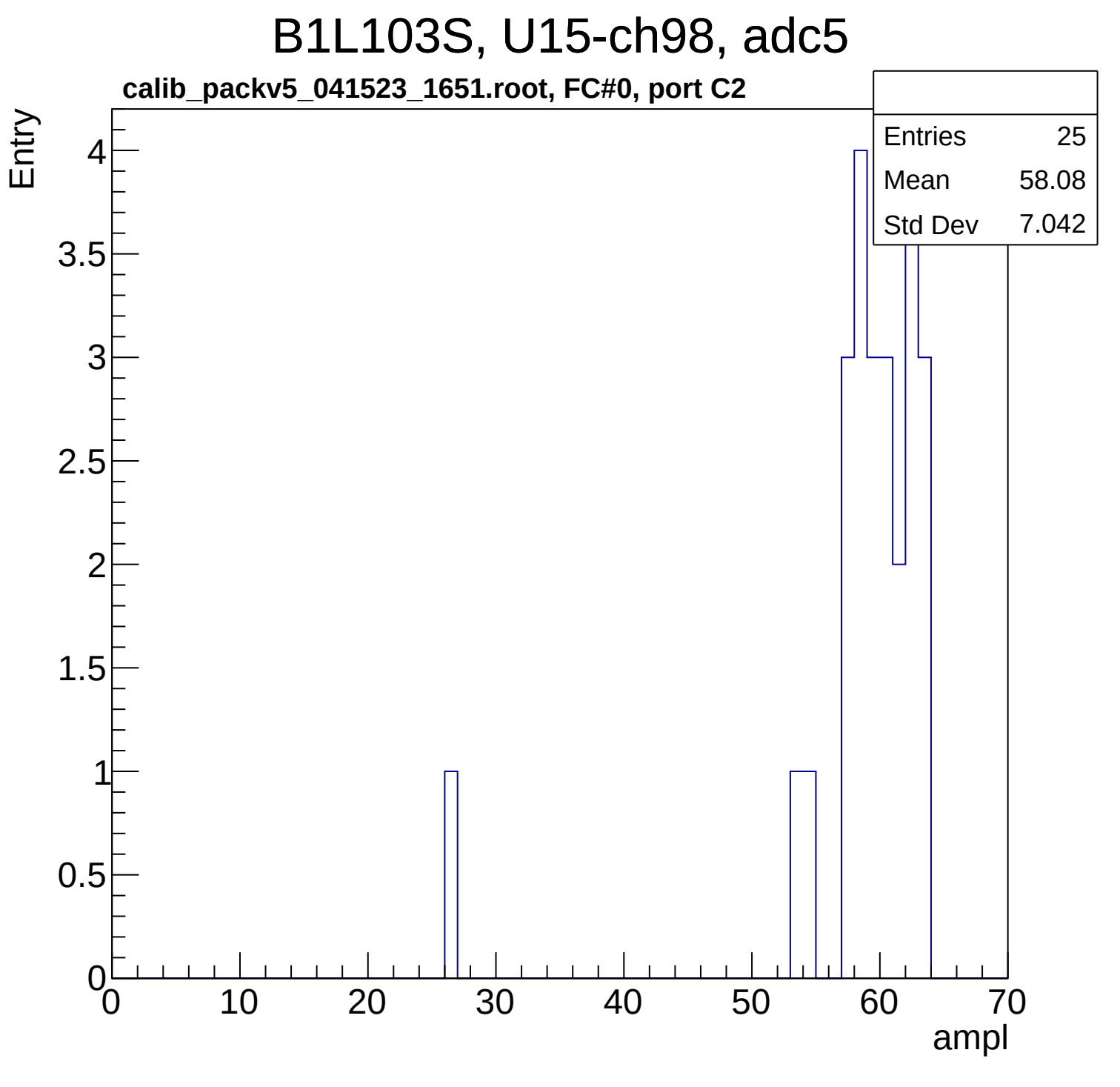
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch98, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 58.08
Std Dev 7.042
Entry
ampl
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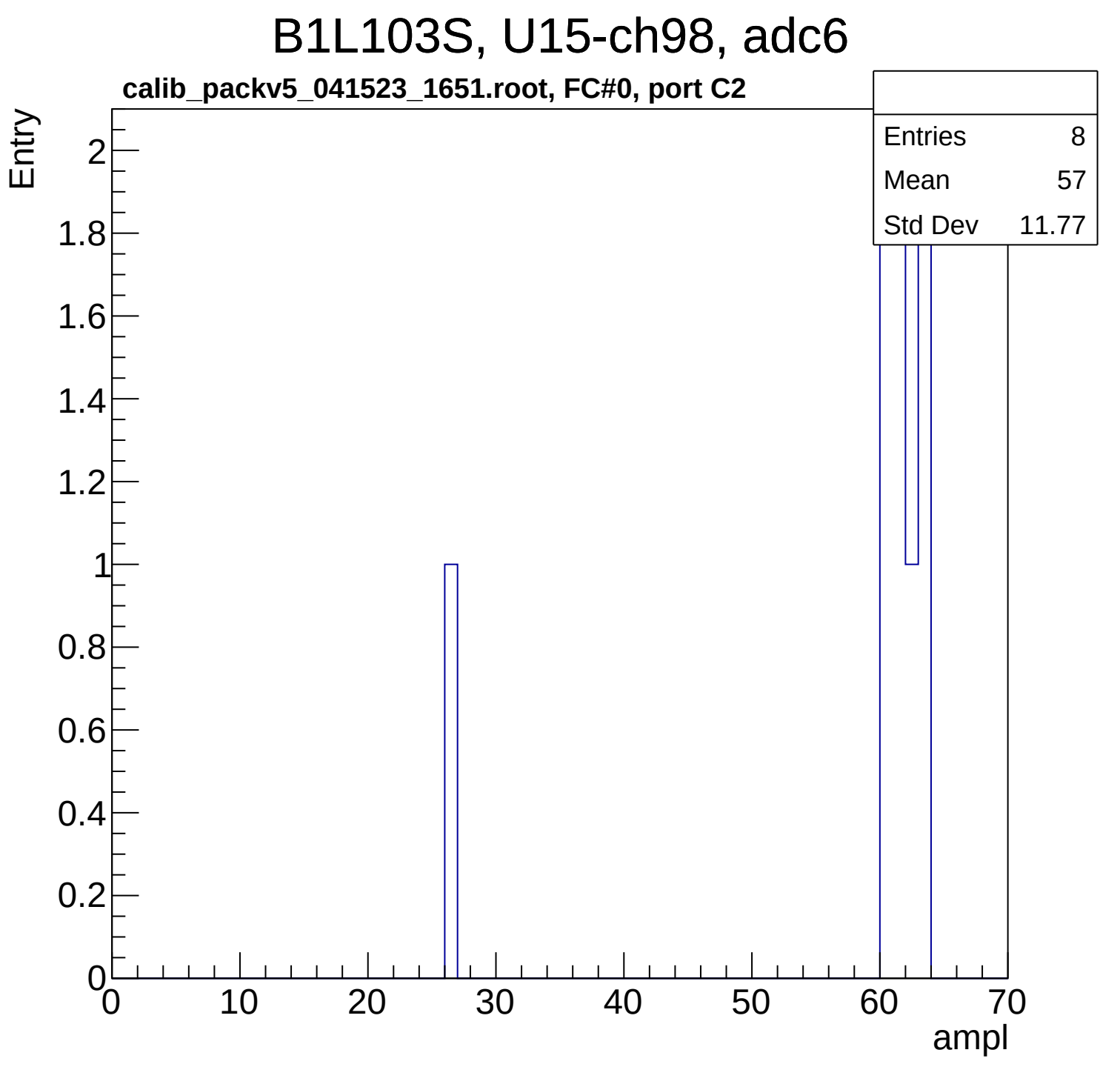
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch98, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 57
Std Dev 11.77
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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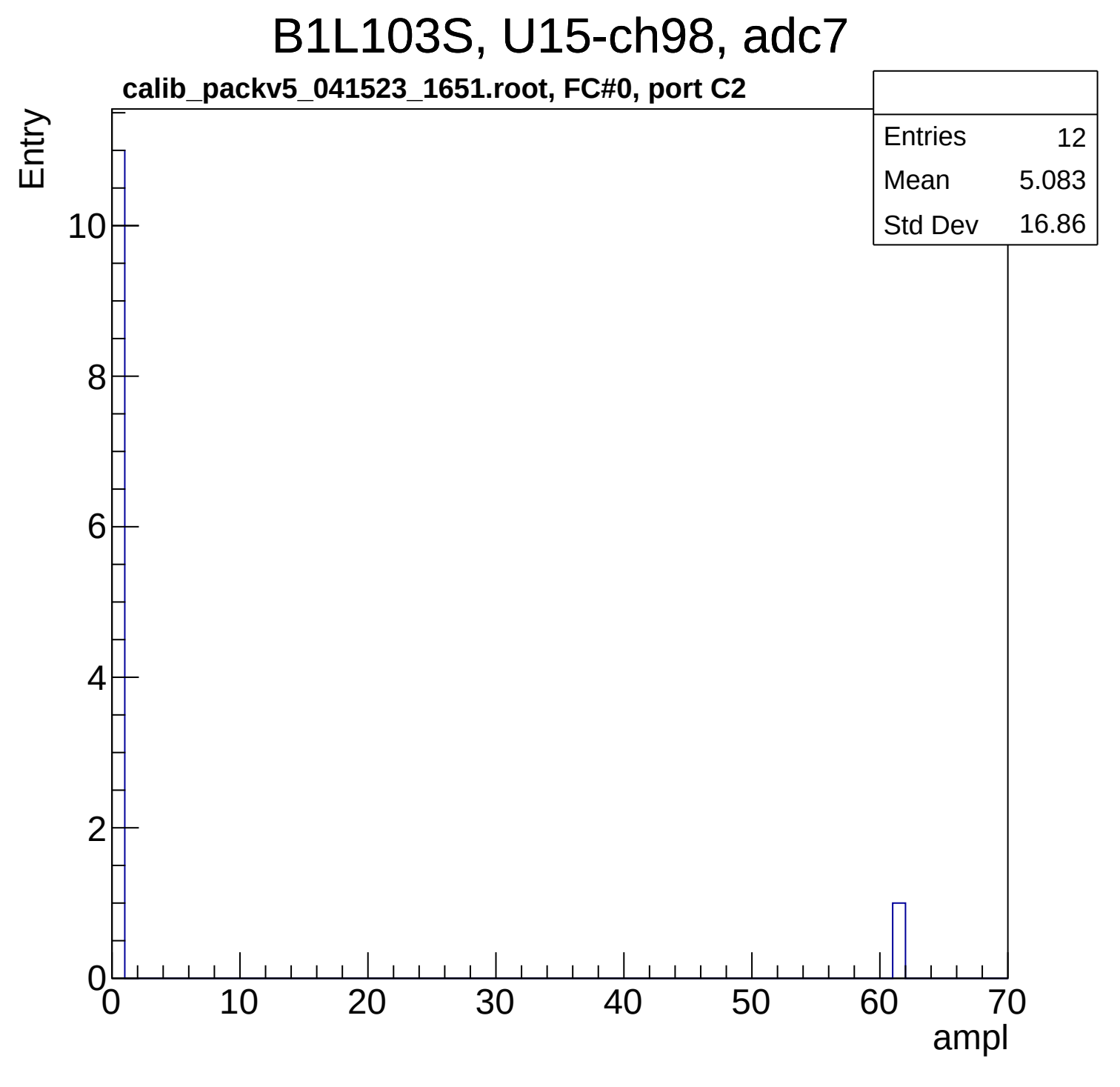
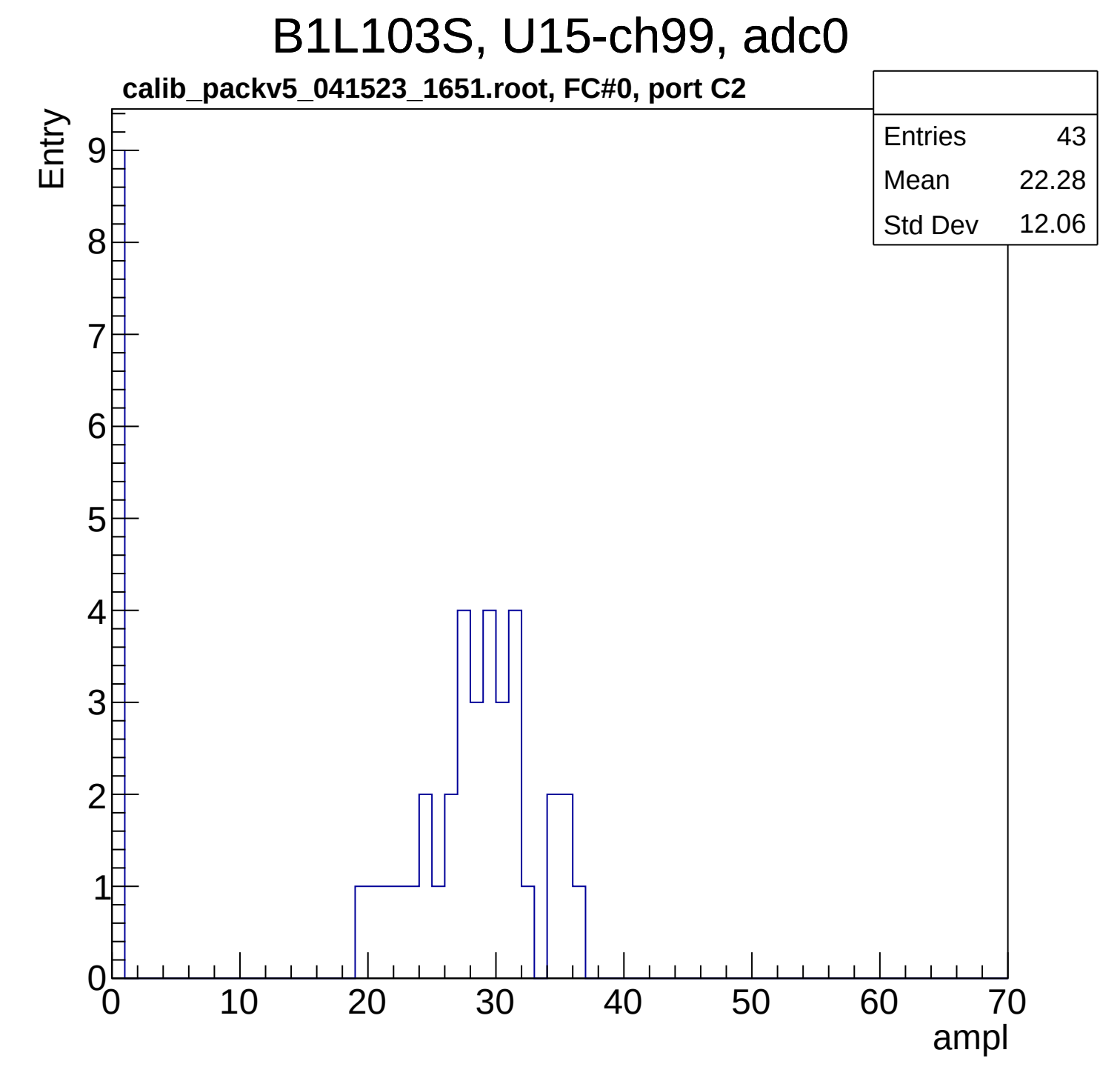
40
50
60
70


B1L103S, U15-ch98, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 5.083
Std Dev 16.86
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch99, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 22.28
Std Dev 12.06
Entry
ampl
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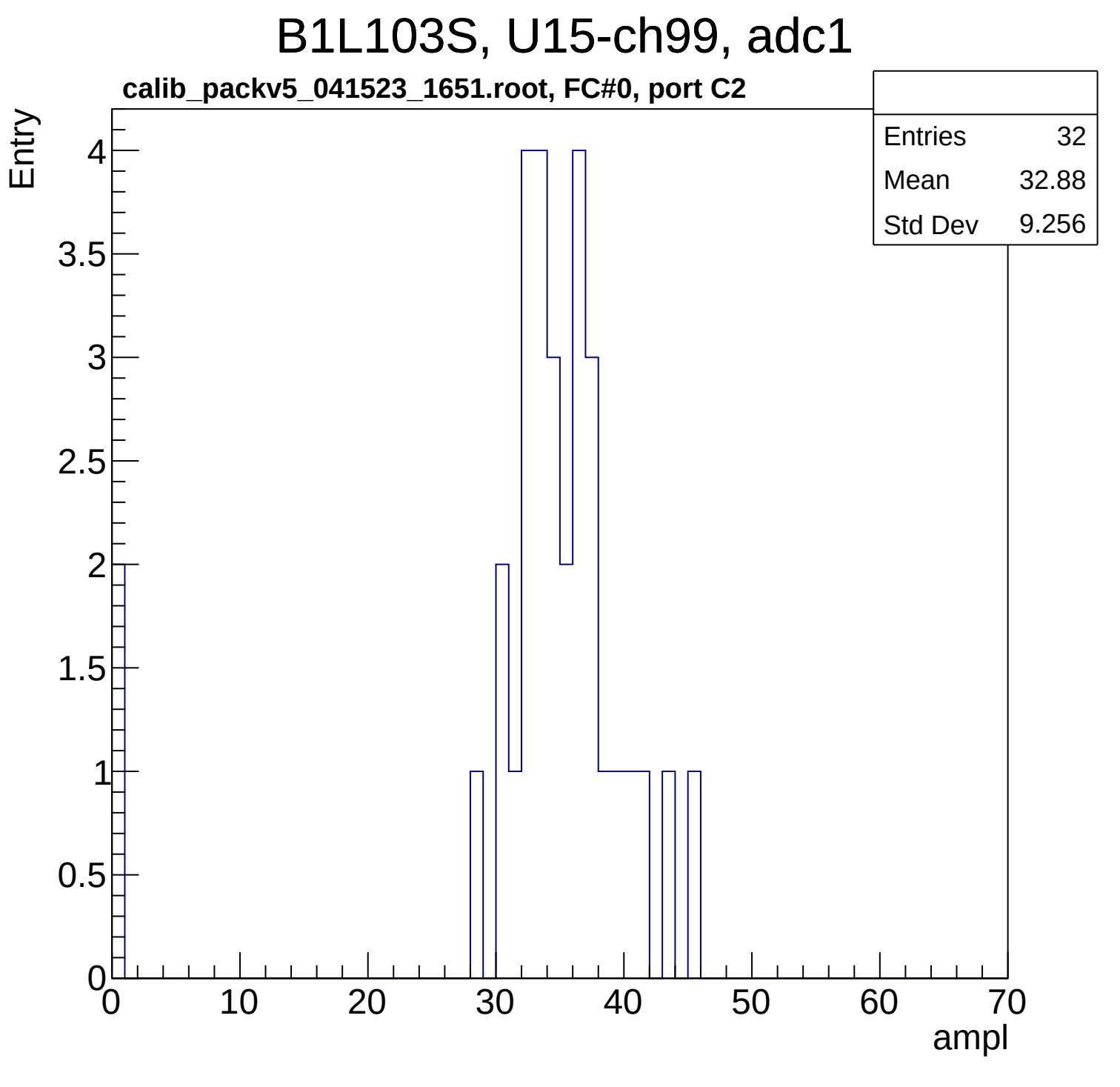
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U15-ch99, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 32.88
Std Dev 9.256
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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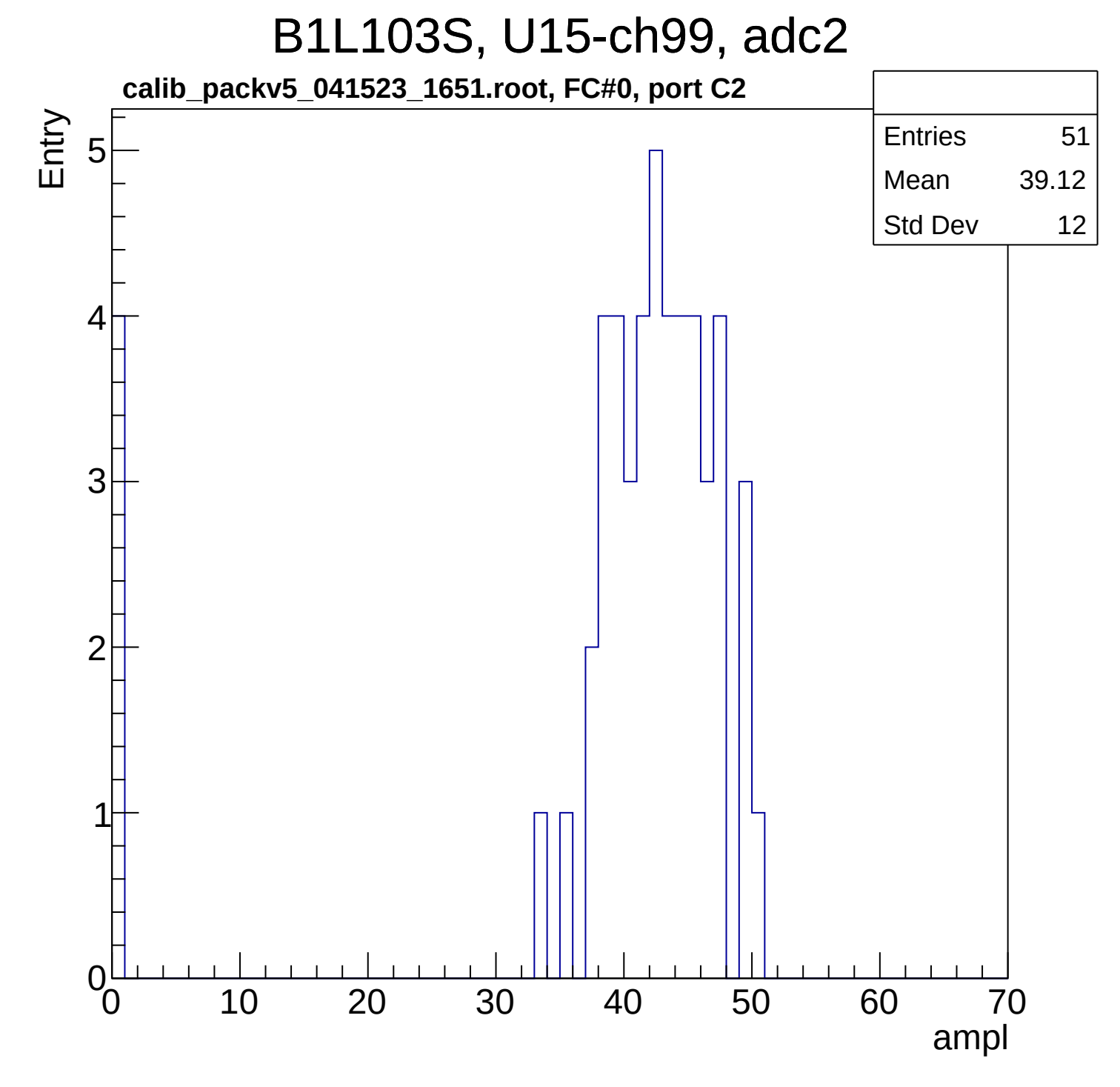
B1L103S, U15-ch99, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 39.12
Std Dev 12
Entry
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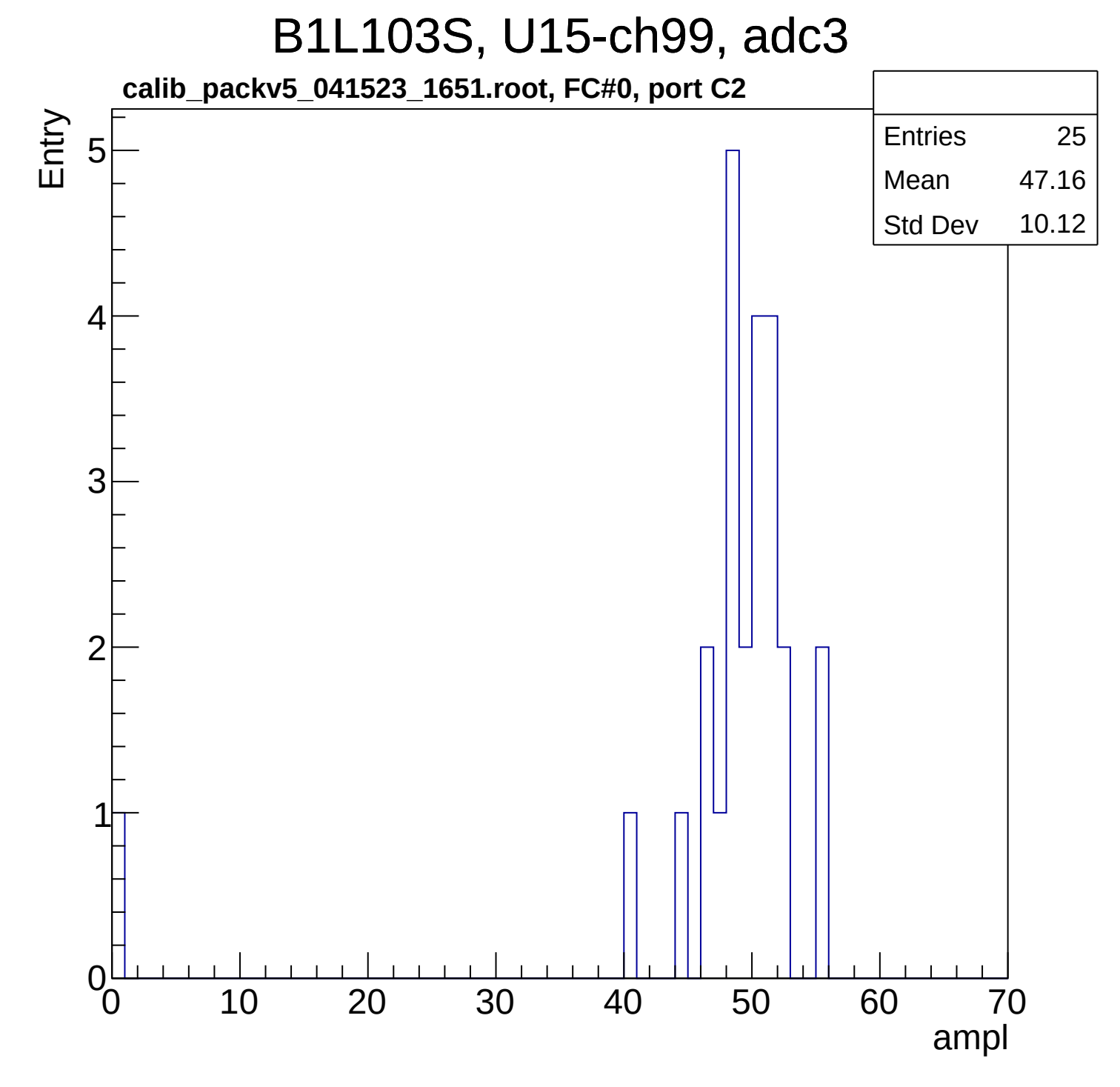
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch99, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 47.16
Std Dev 10.12
Entry
ampl
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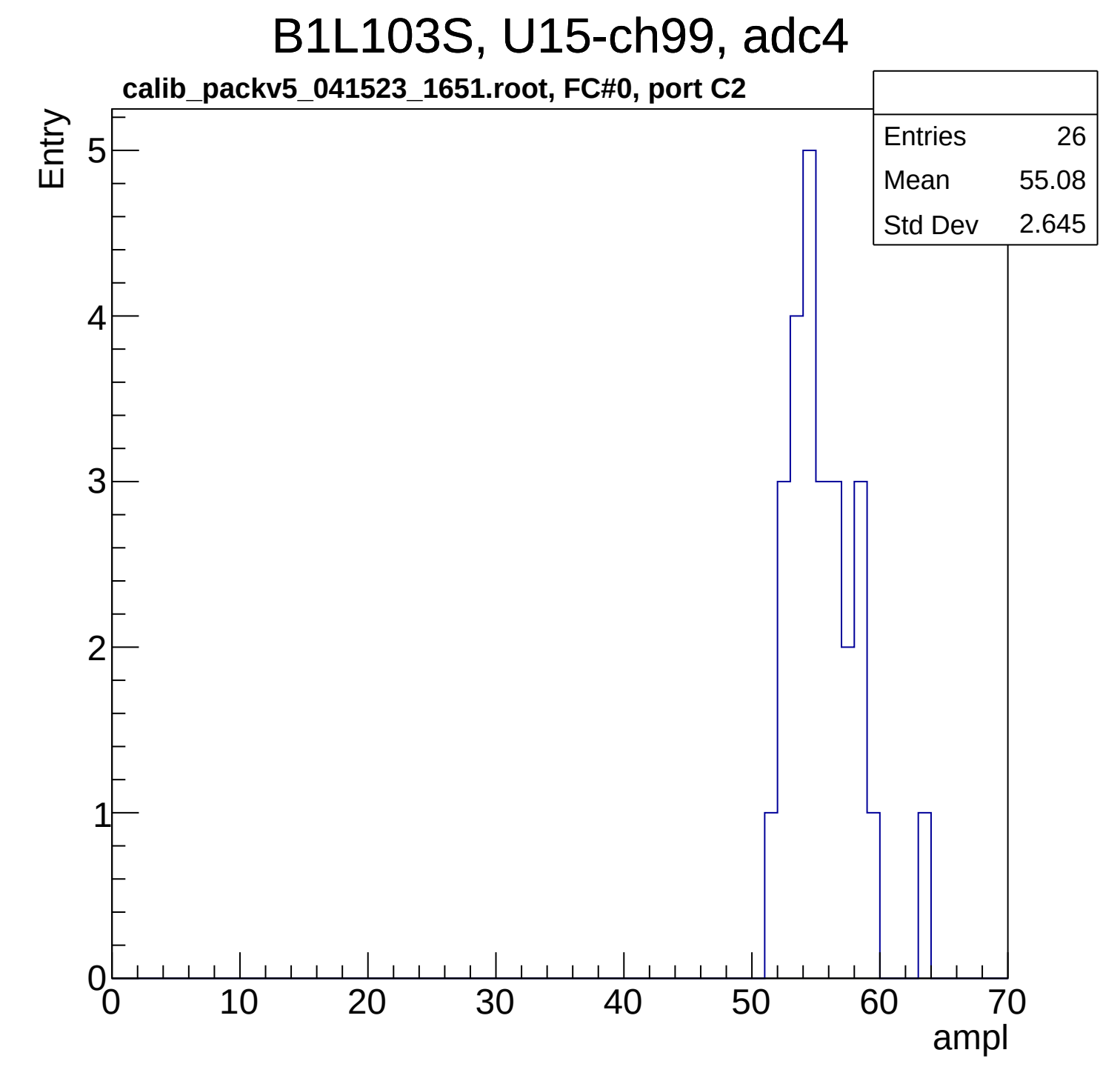
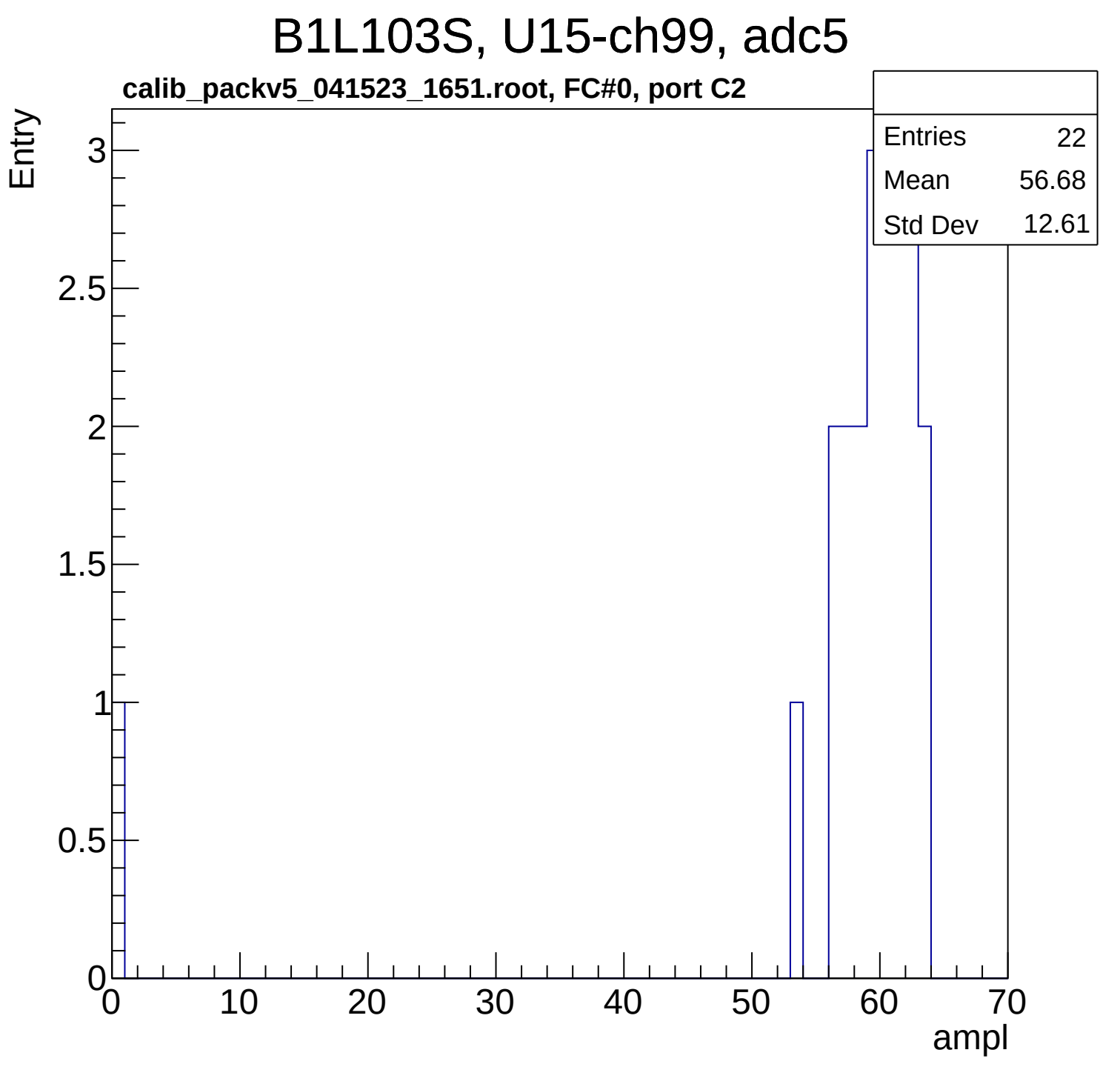
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch99, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 55.08
Std Dev 2.645
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch99, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 56.68
Std Dev 12.61
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
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20
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40
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60
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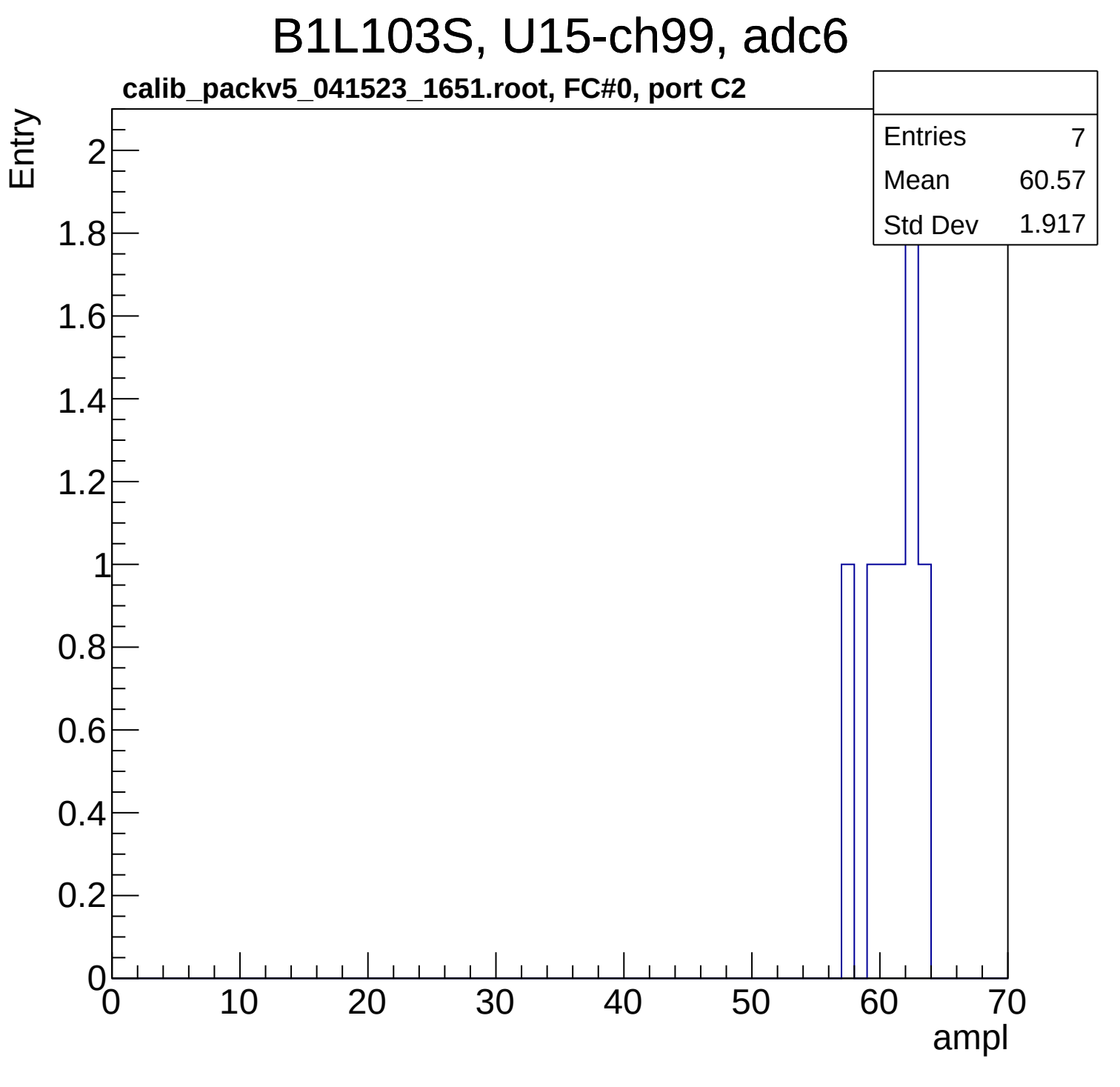
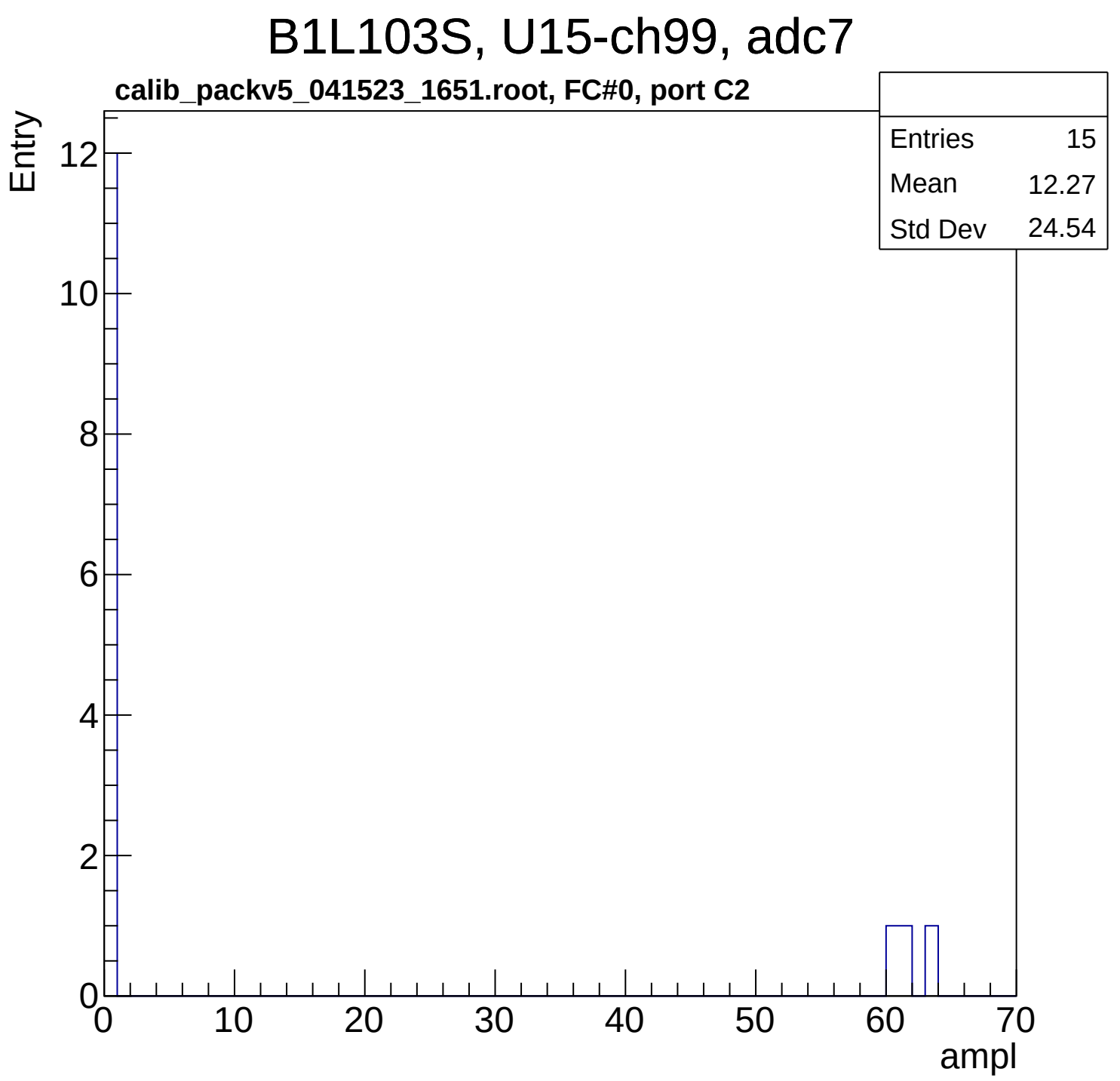
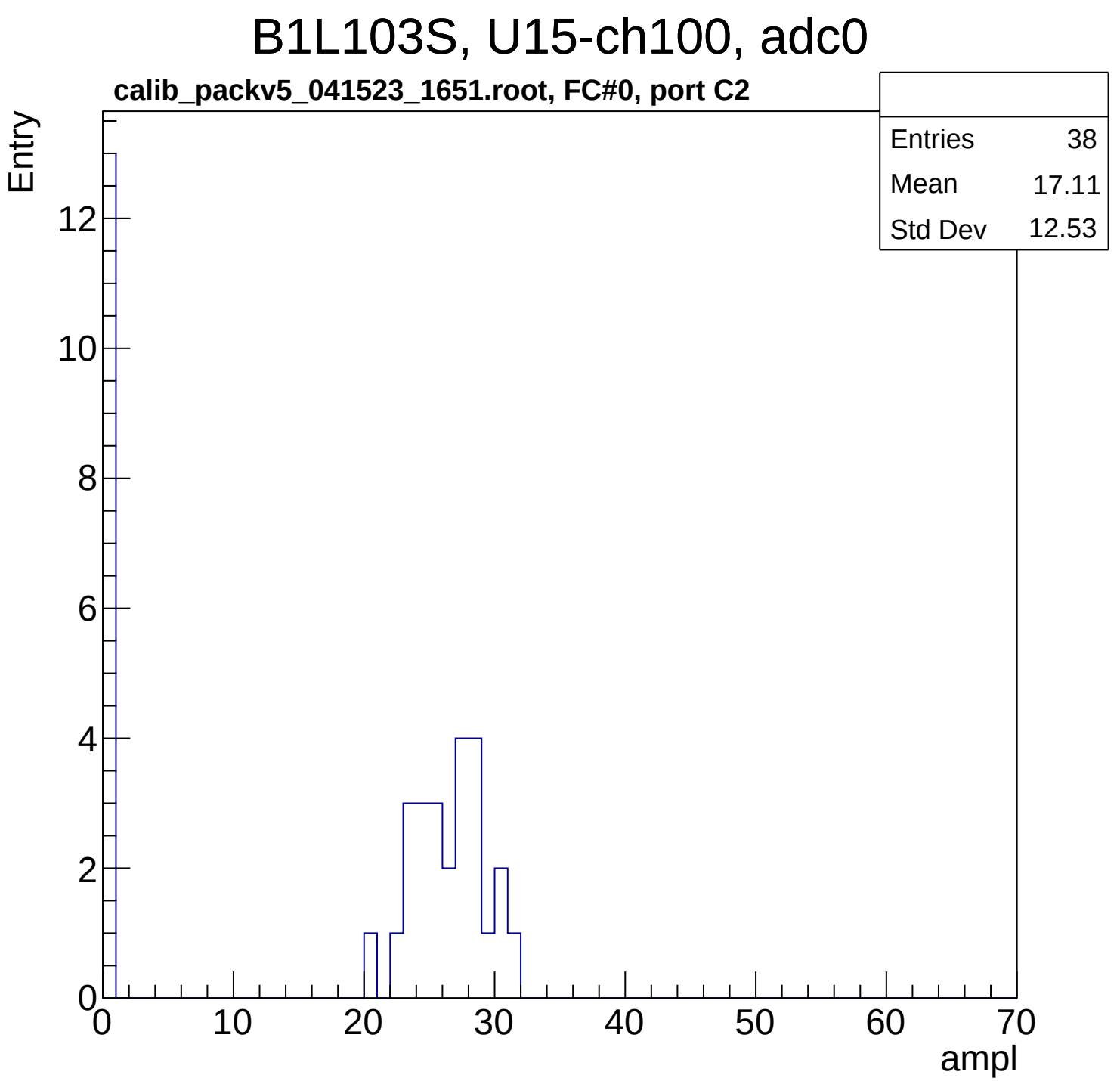
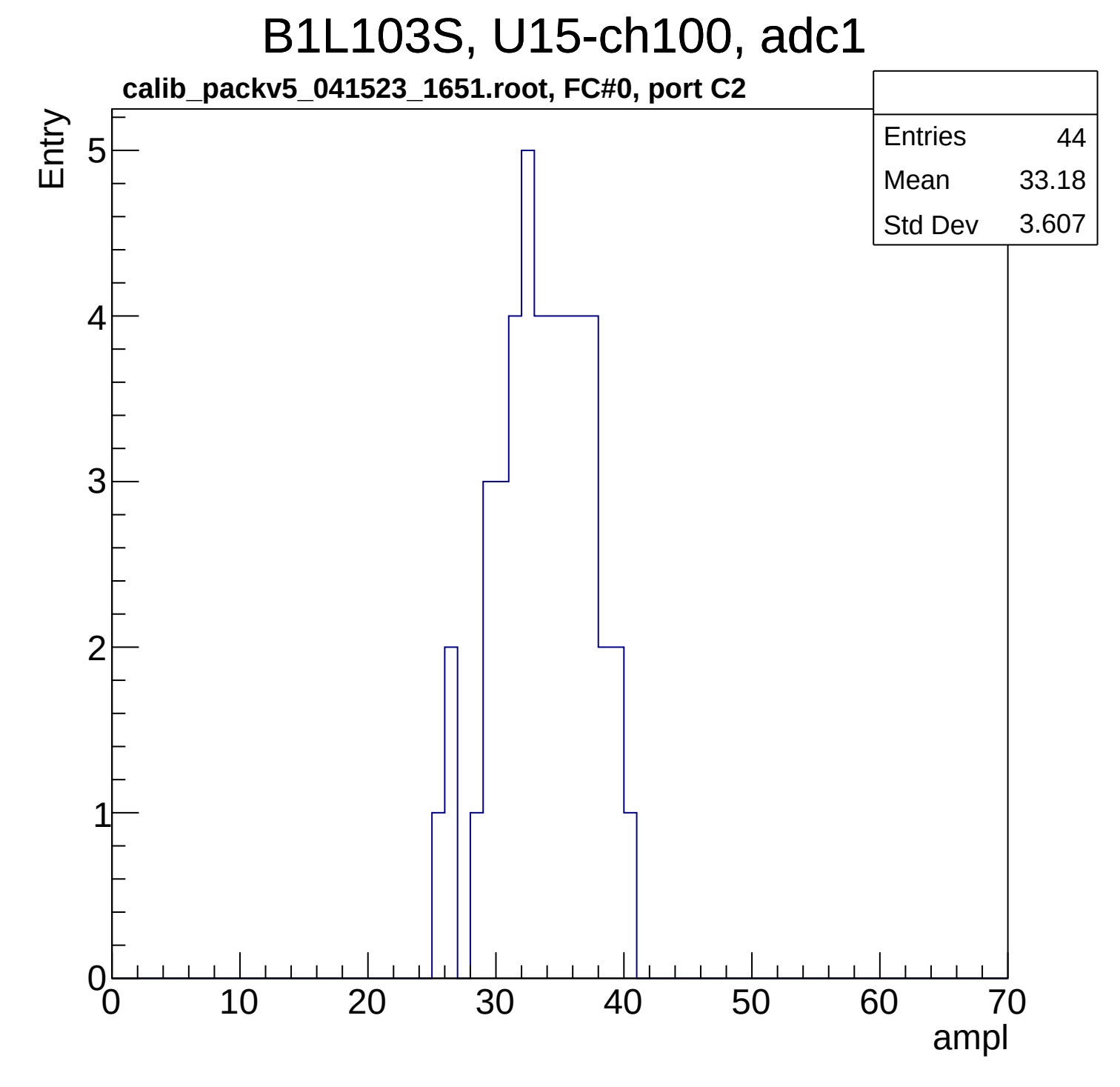
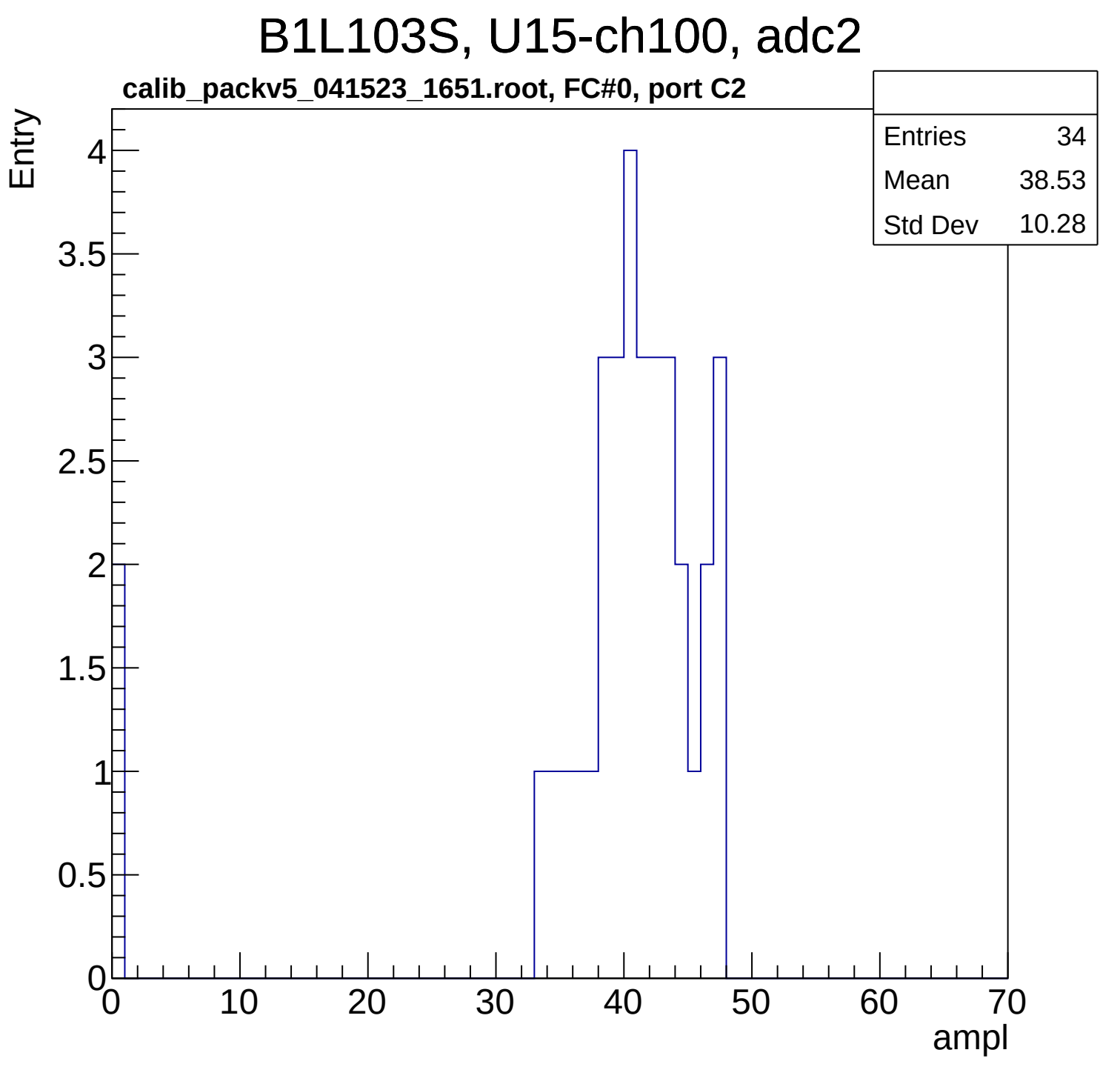

B1L103S, U15-ch99, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 60.57
Std Dev 1.917
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U15-ch99, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 12.27
Std Dev 24.54
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch100, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 17.11
Std Dev 12.53
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch100, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 33.18
Std Dev 3.607
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch100, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 38.53
Std Dev 10.28
Entry
ampl
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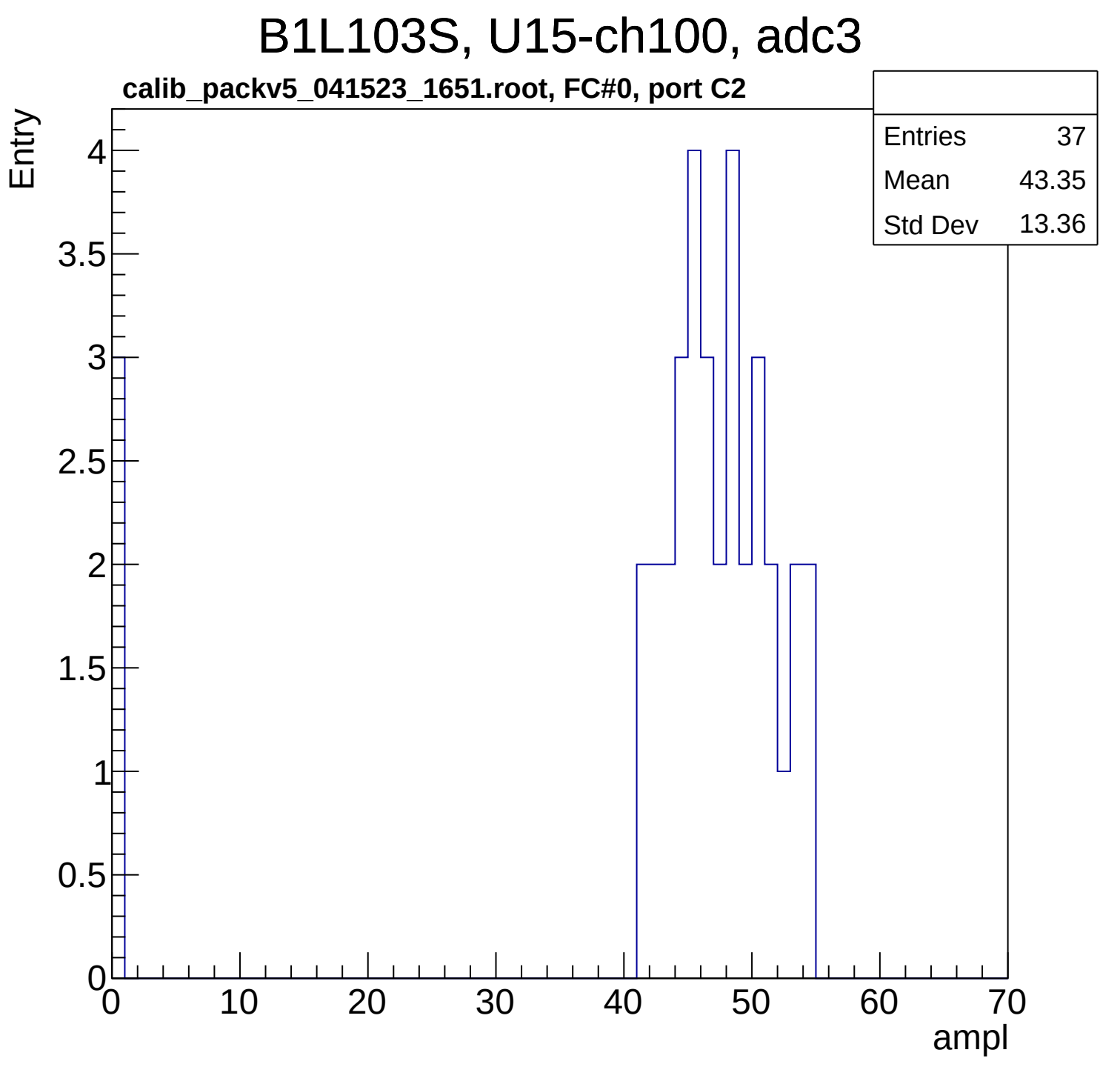
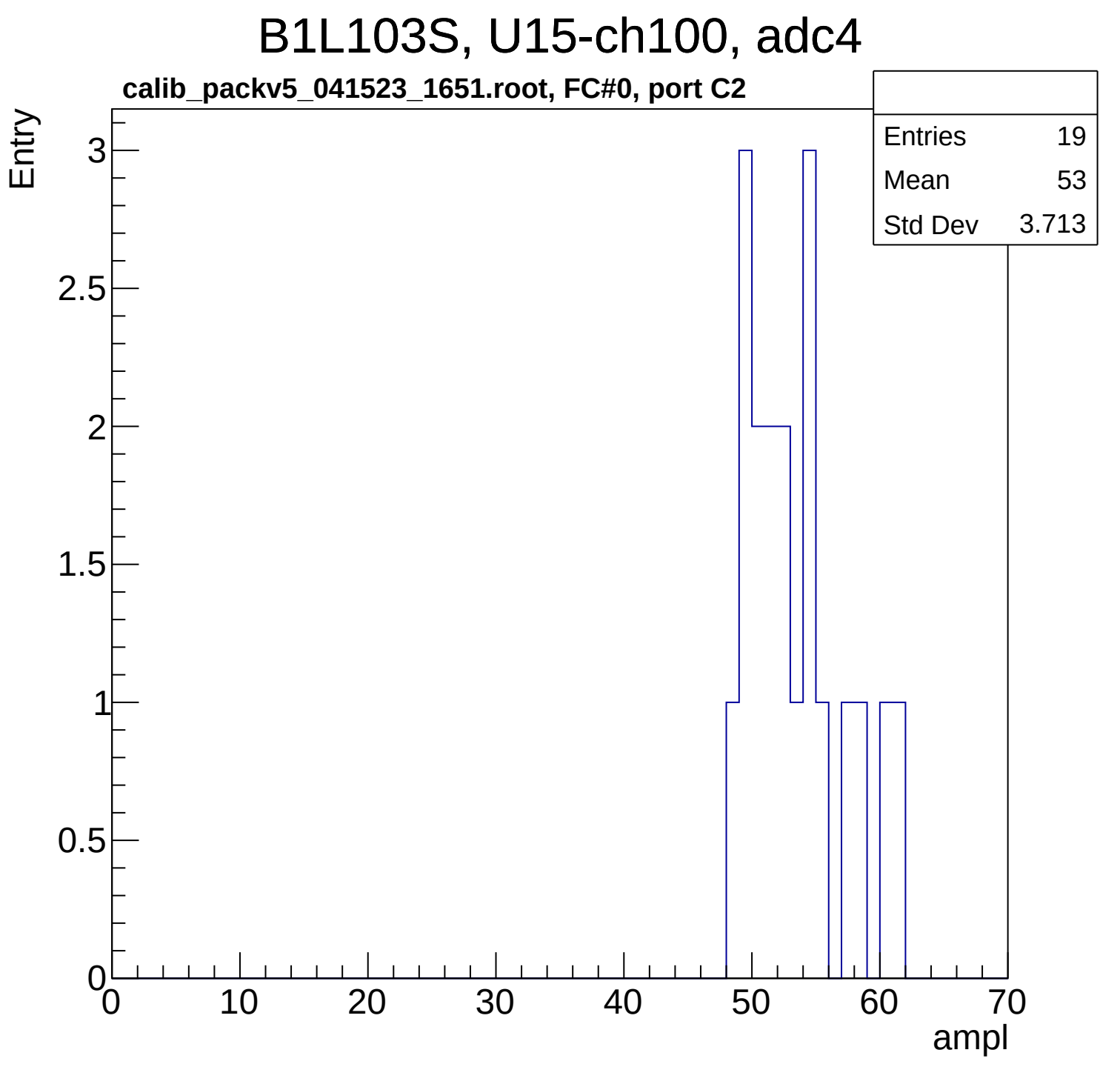
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch100, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 43.35
Std Dev 13.36
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch100, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 53
Std Dev 3.713
Entry
ampl
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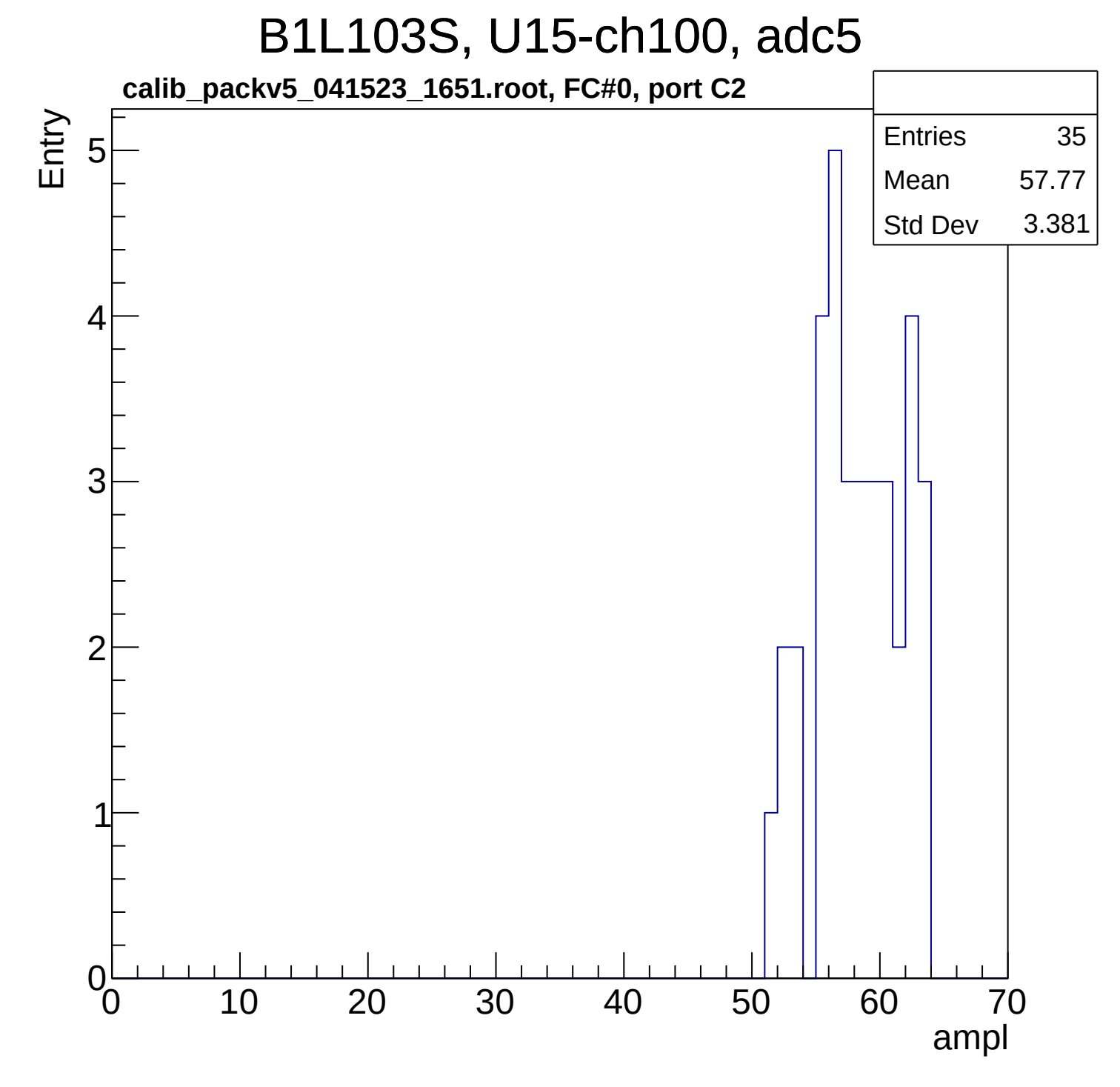
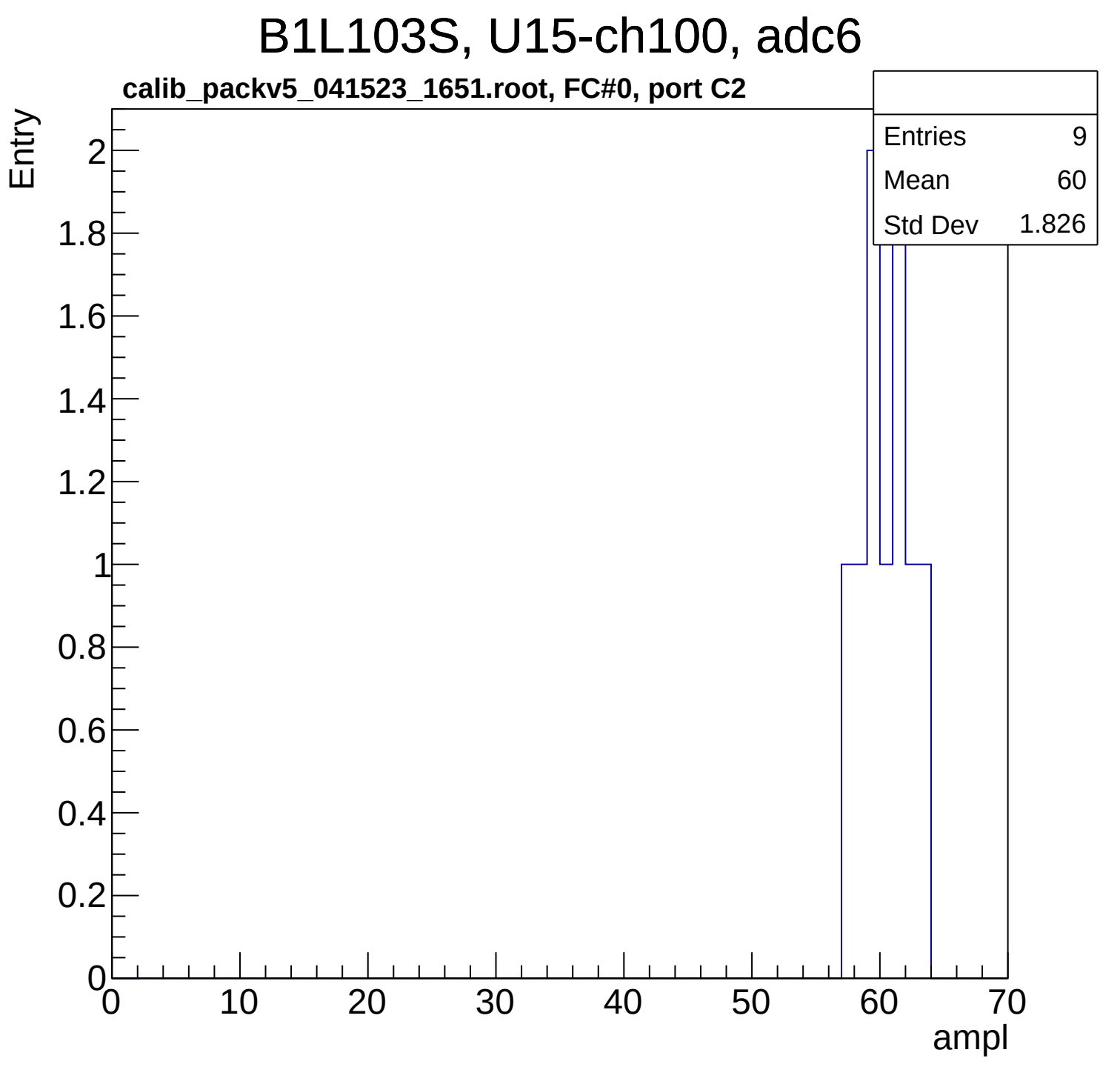
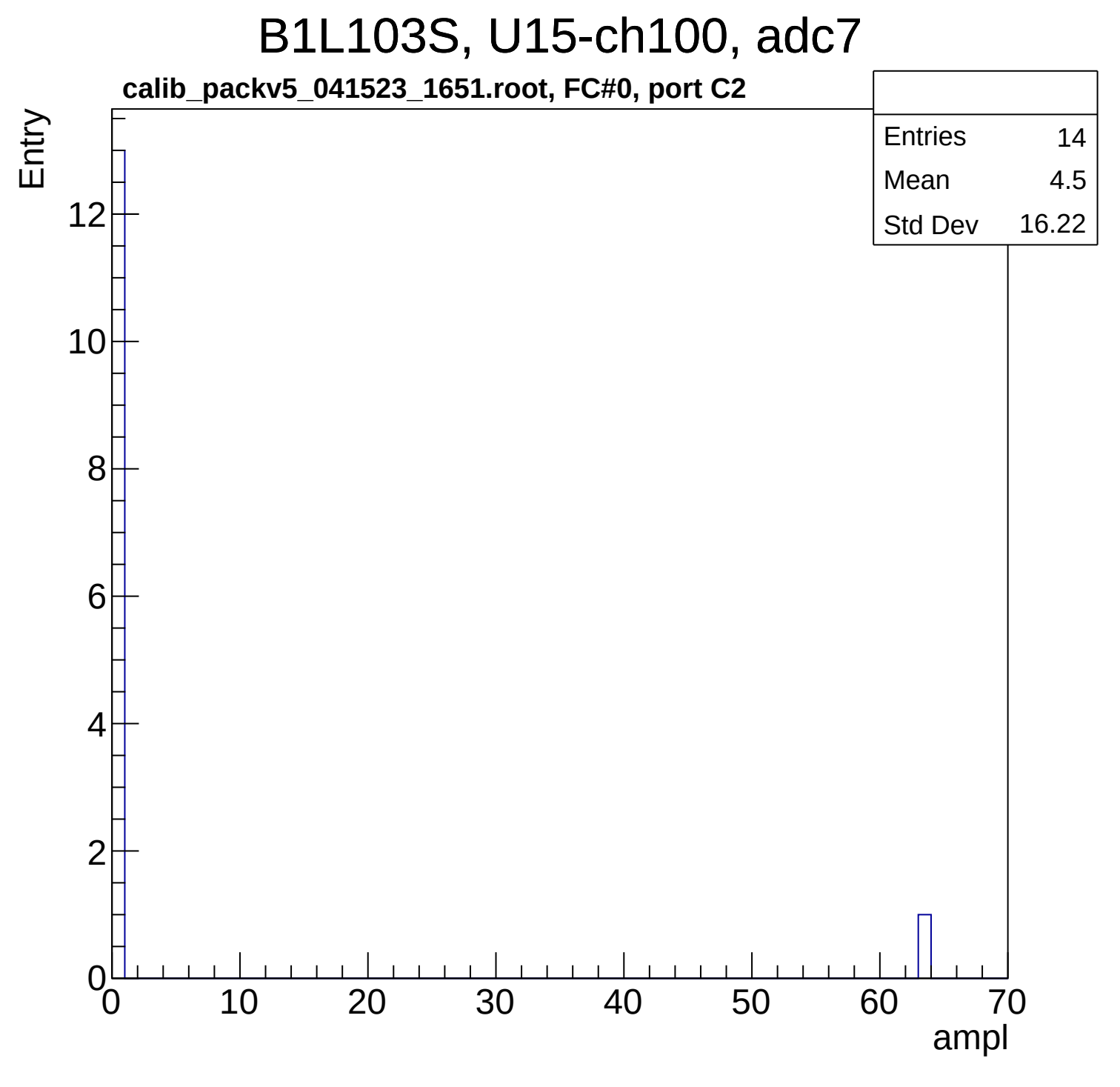
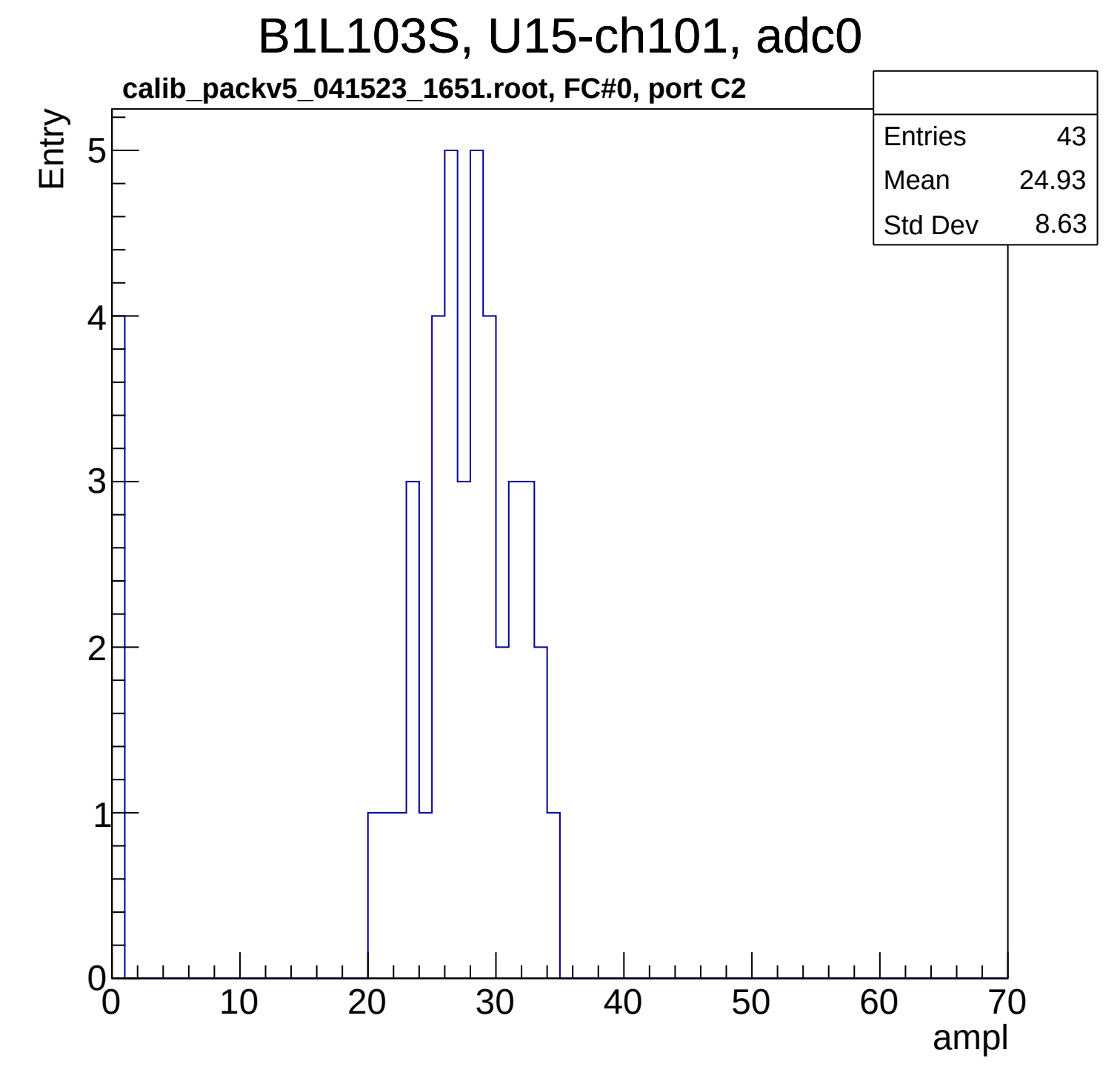
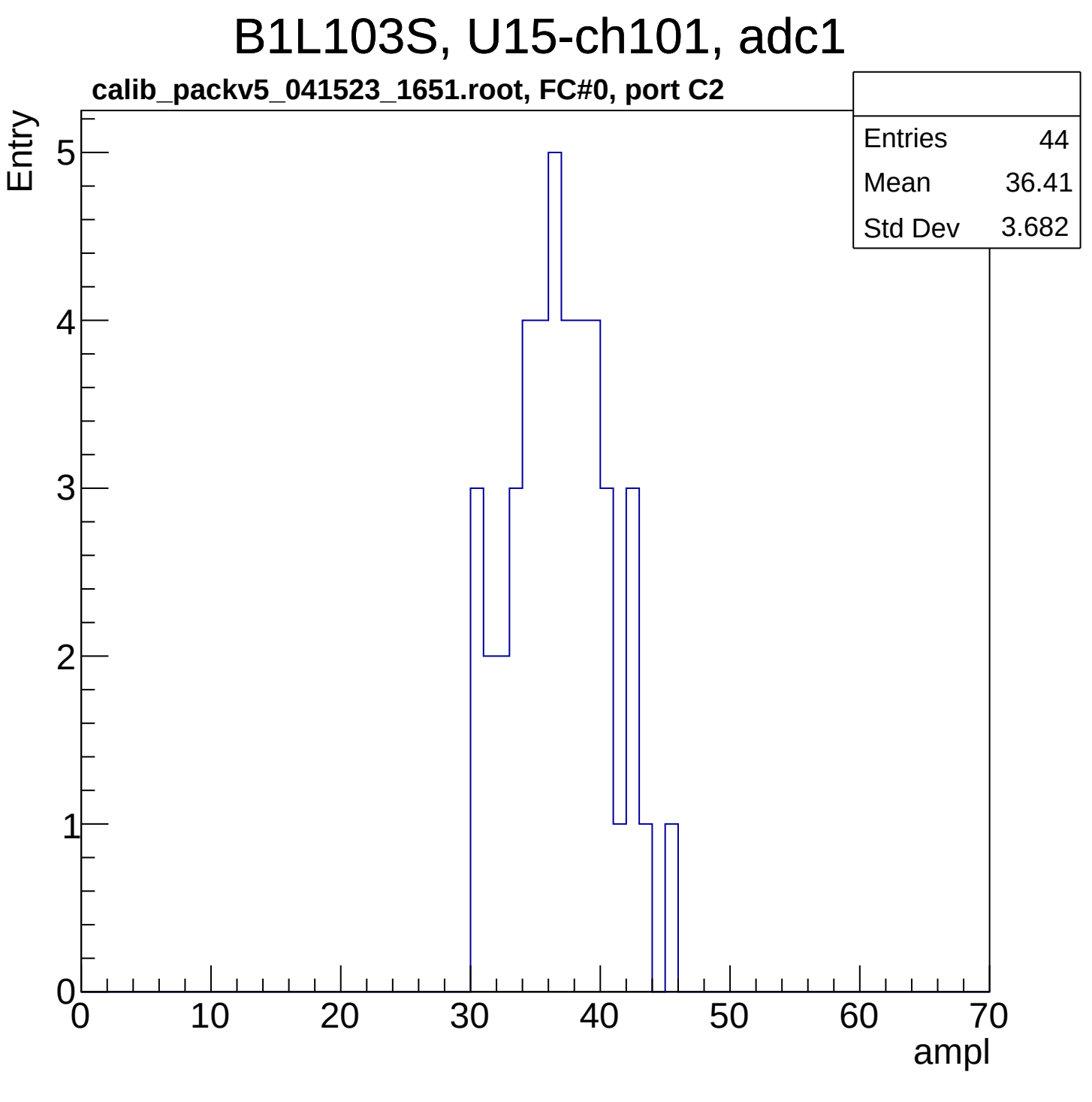
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

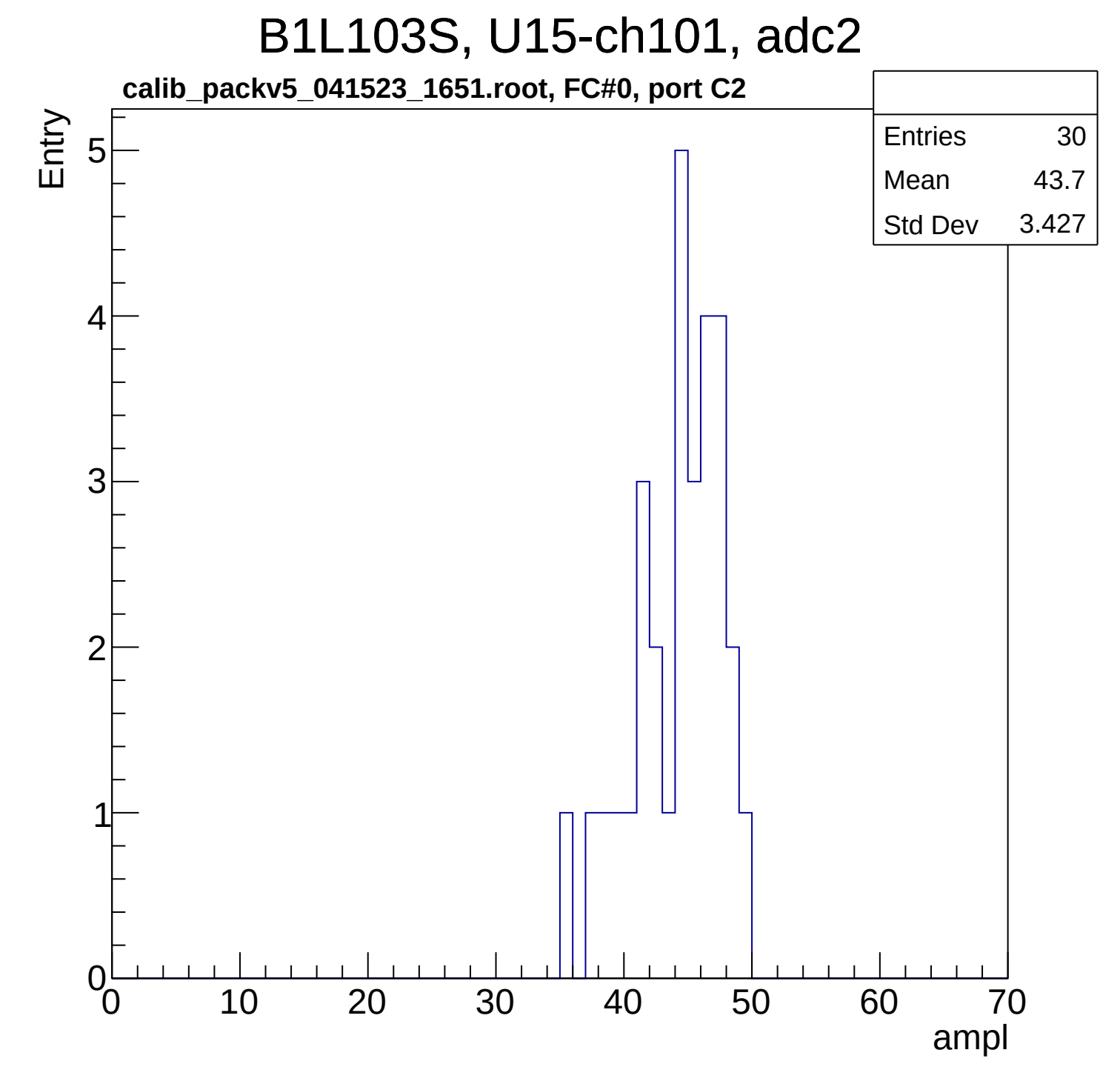

B1L103S, U15-ch100, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 57.77
Std Dev 3.381
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

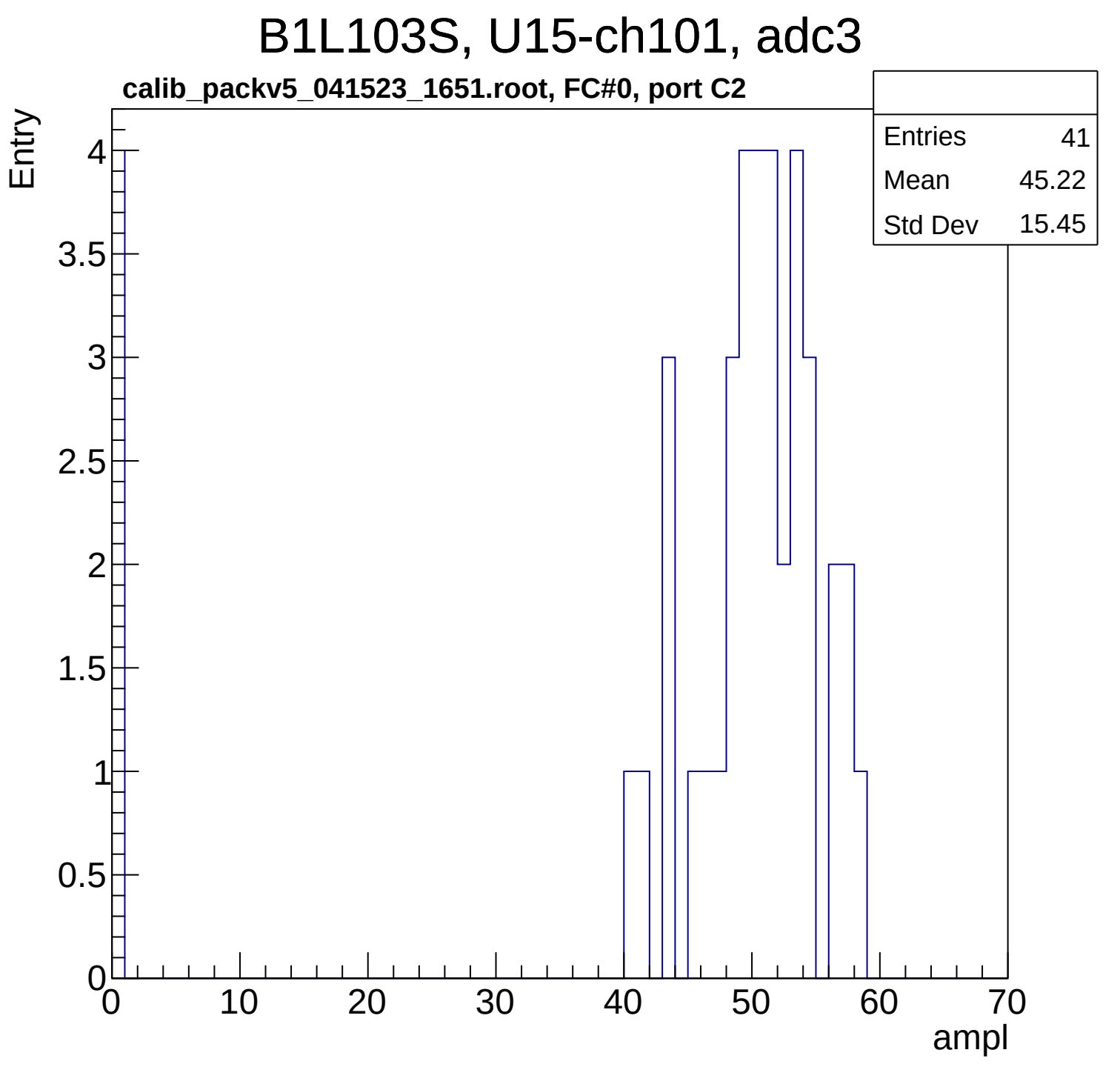

B1L103S, U15-ch100, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 60
Std Dev 1.826
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U15-ch100, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 4.5
Std Dev 16.22
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch101, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 24.93
Std Dev 8.63
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch101, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 36.41
Std Dev 3.682
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch101, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 43.7
Std Dev 3.427
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch101, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 45.22
Std Dev 15.45
Entry
ampl
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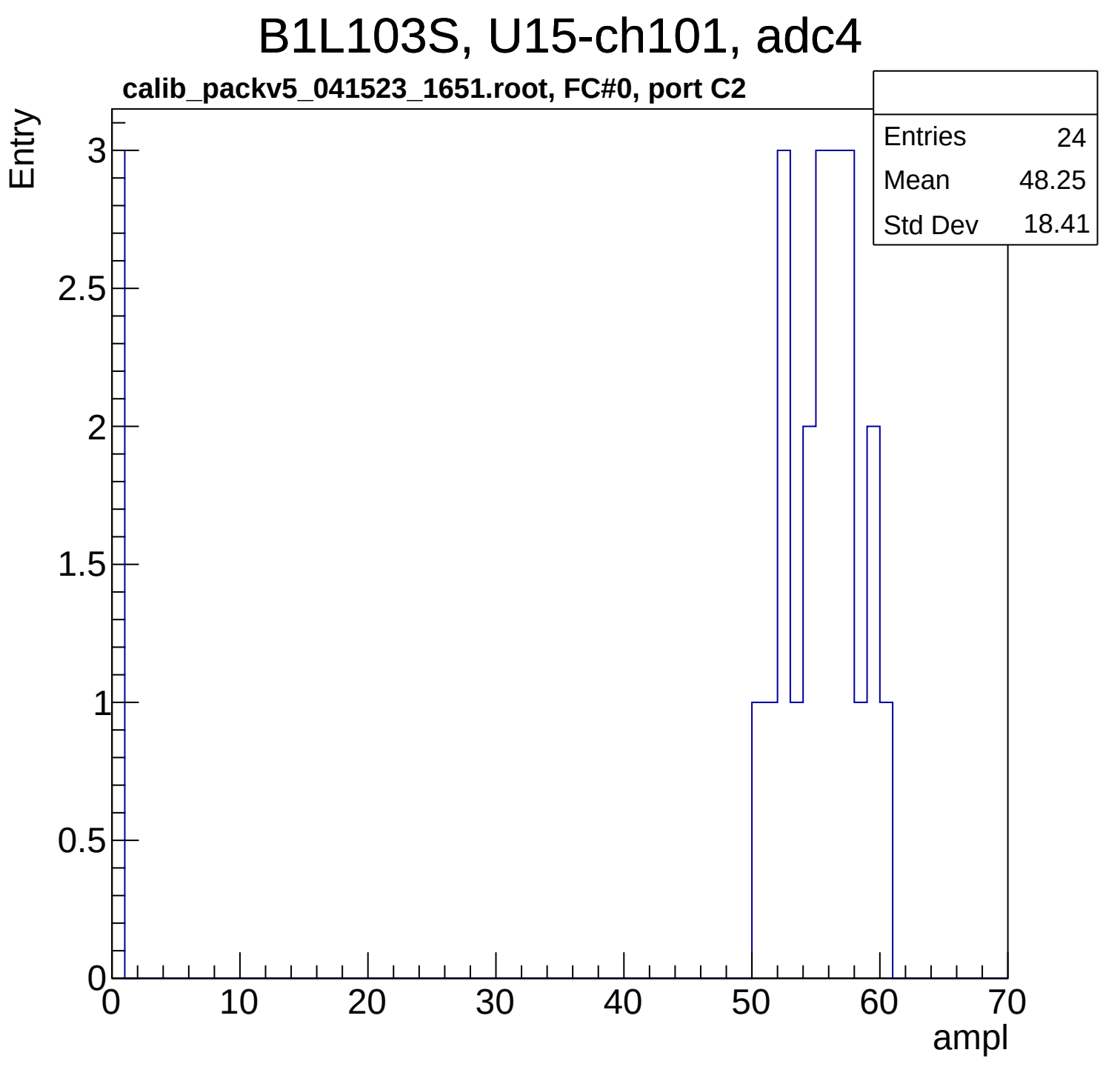
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch101, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 48.25
Std Dev 18.41
Entry
ampl
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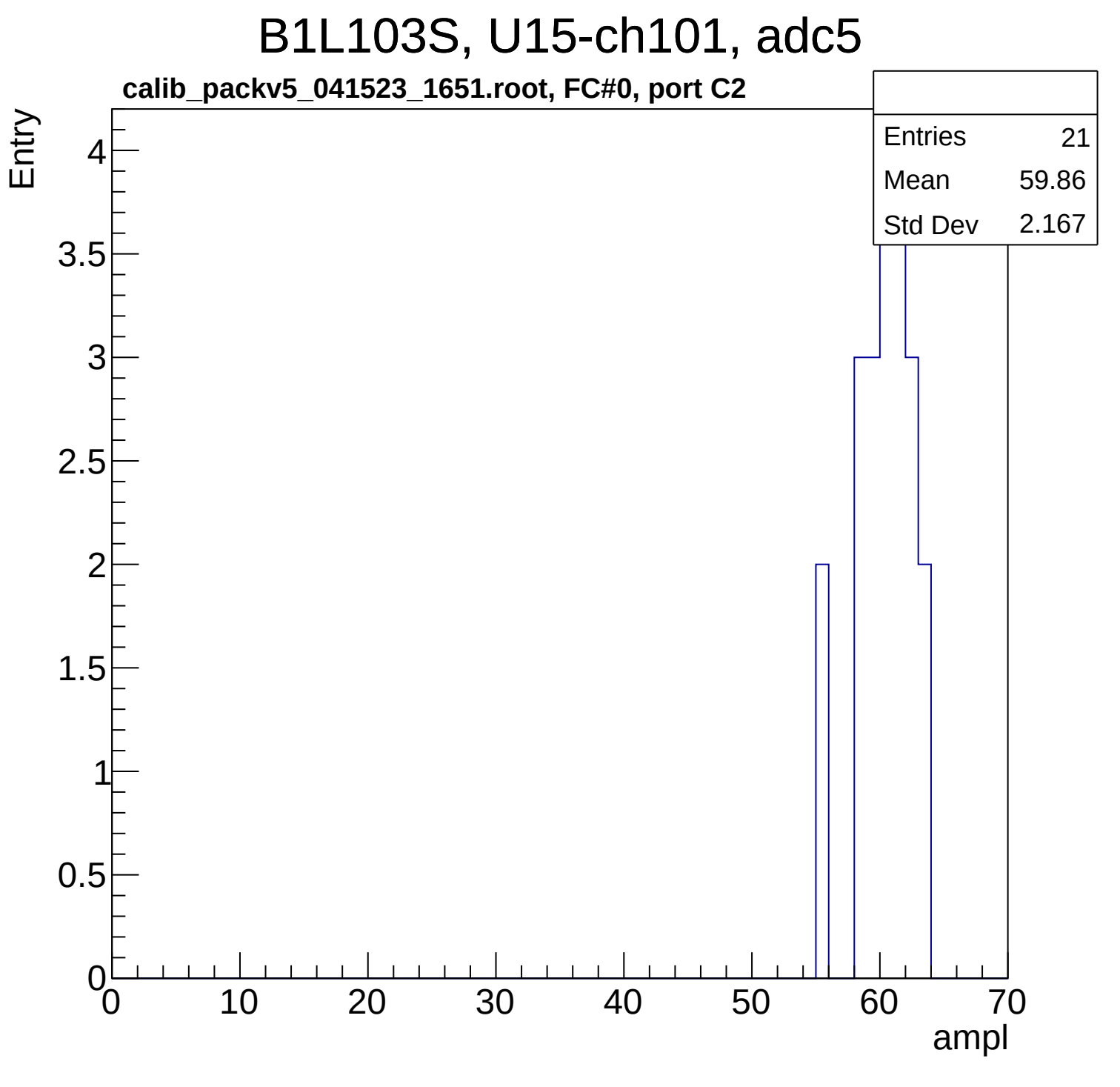
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch101, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 59.86
Std Dev 2.167
Entry
ampl
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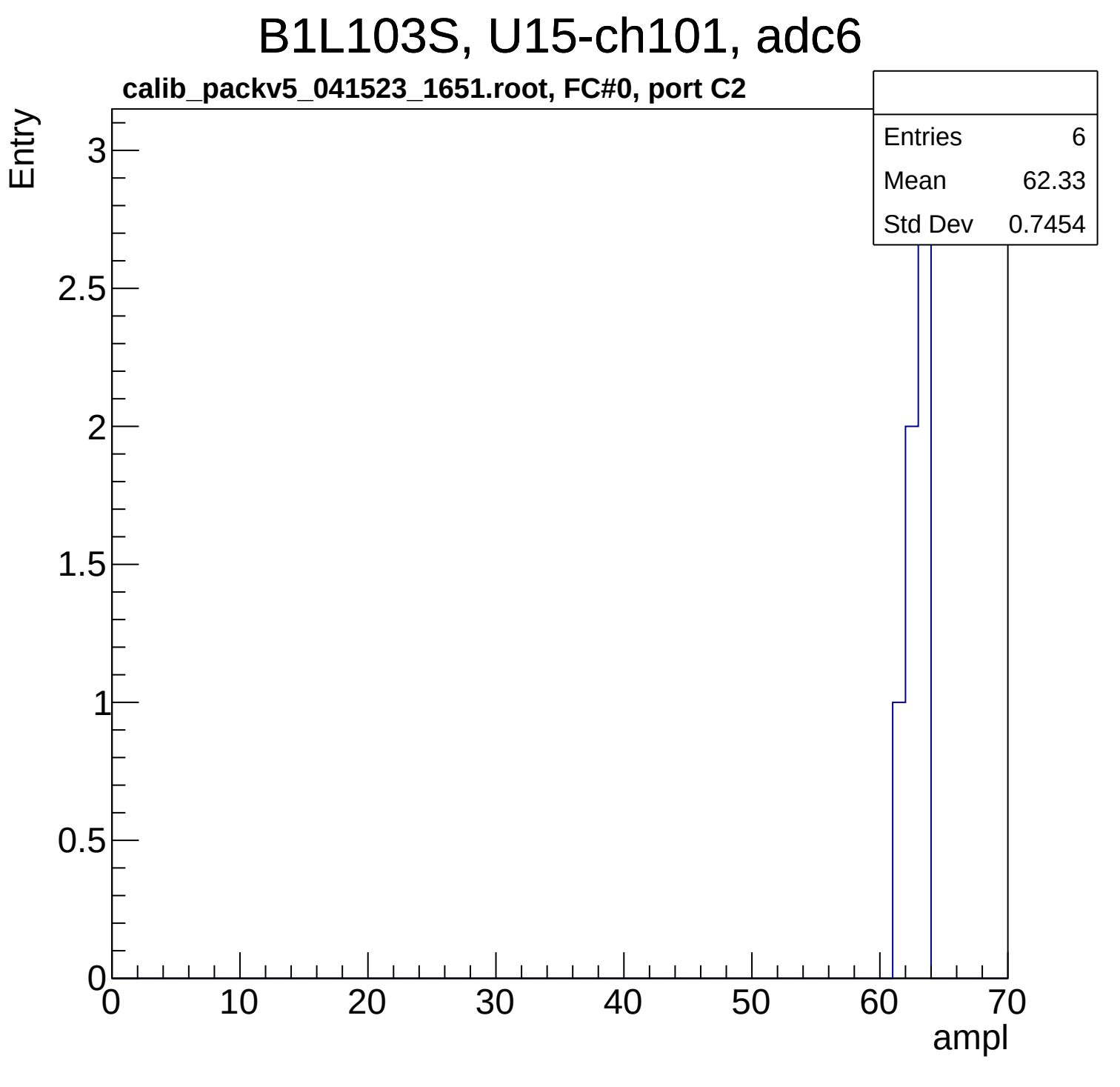
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch101, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.33
Std Dev 0.7454
Entry
ampl
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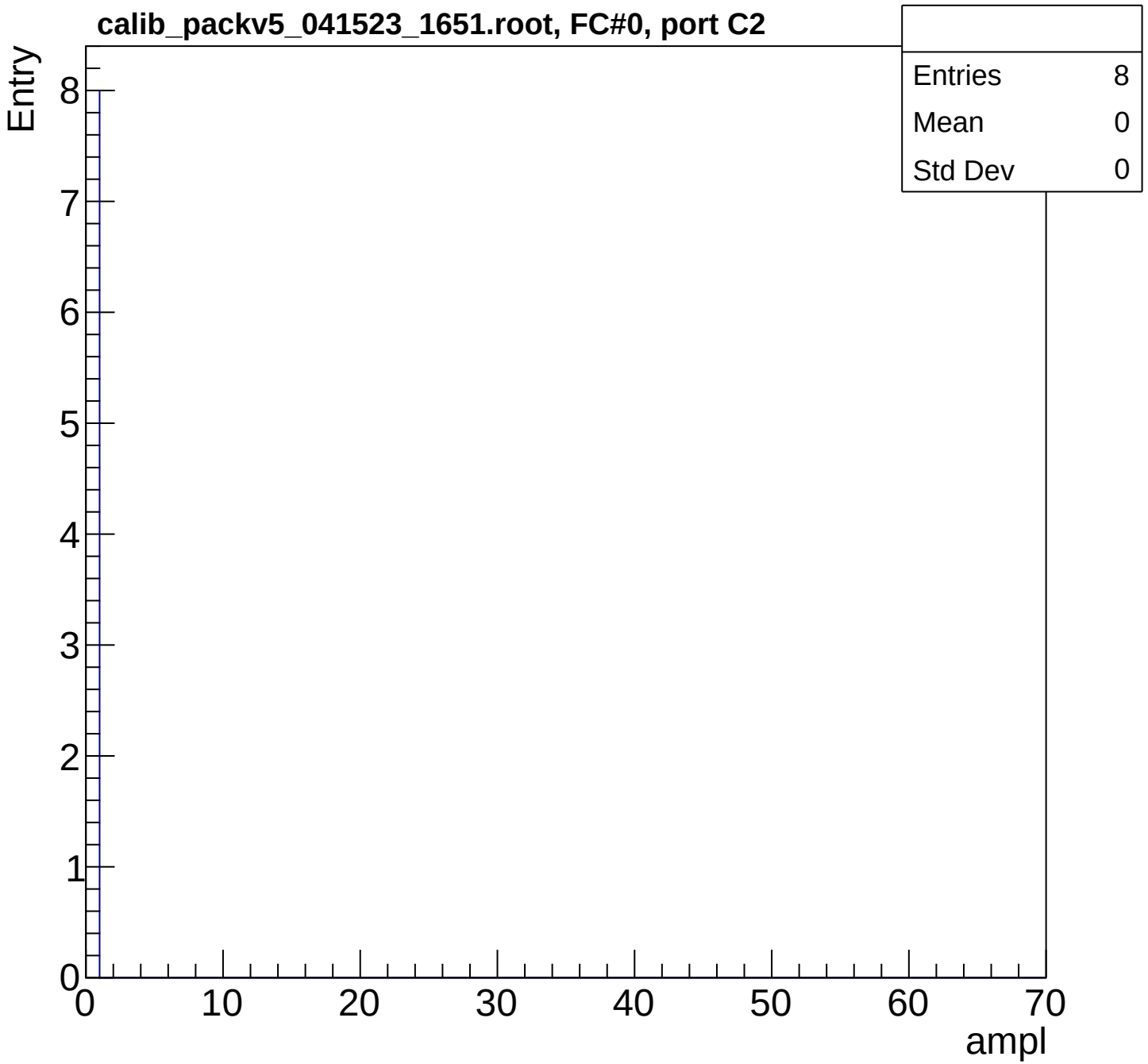
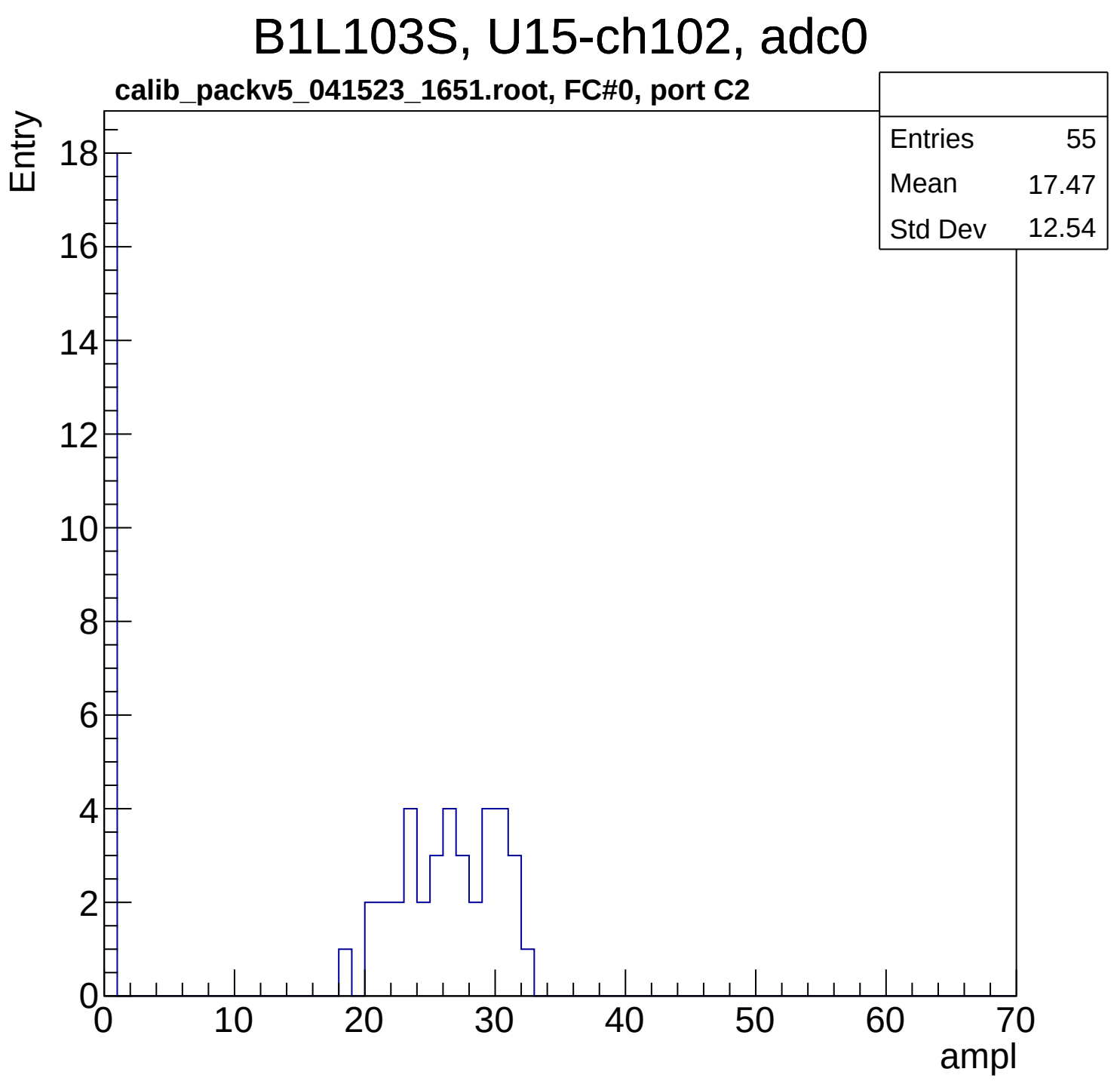
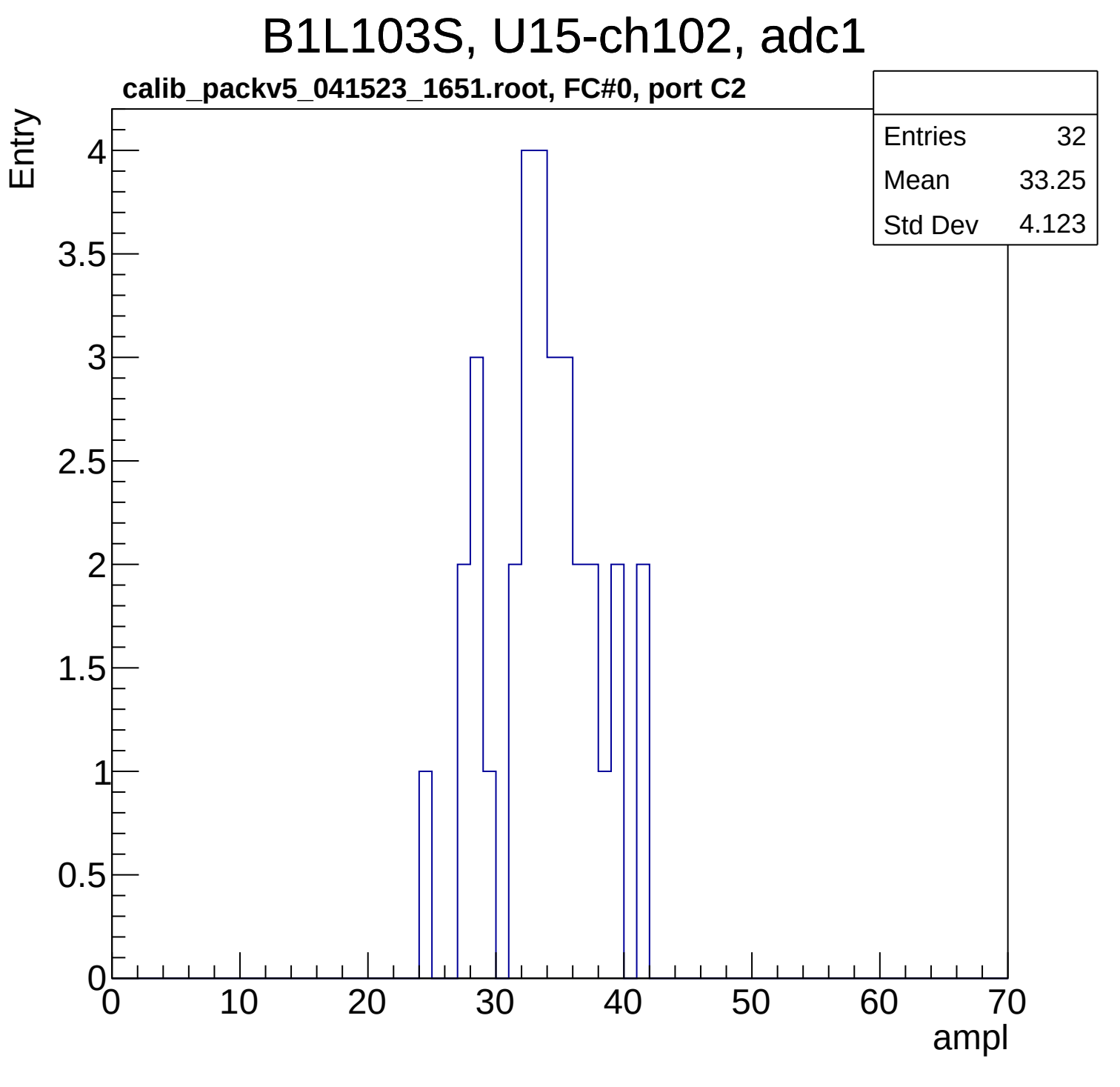
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch101, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 0
Std Dev 0
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch102, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 17.47
Std Dev 12.54
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch102, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 33.25
Std Dev 4.123
Entry
ampl
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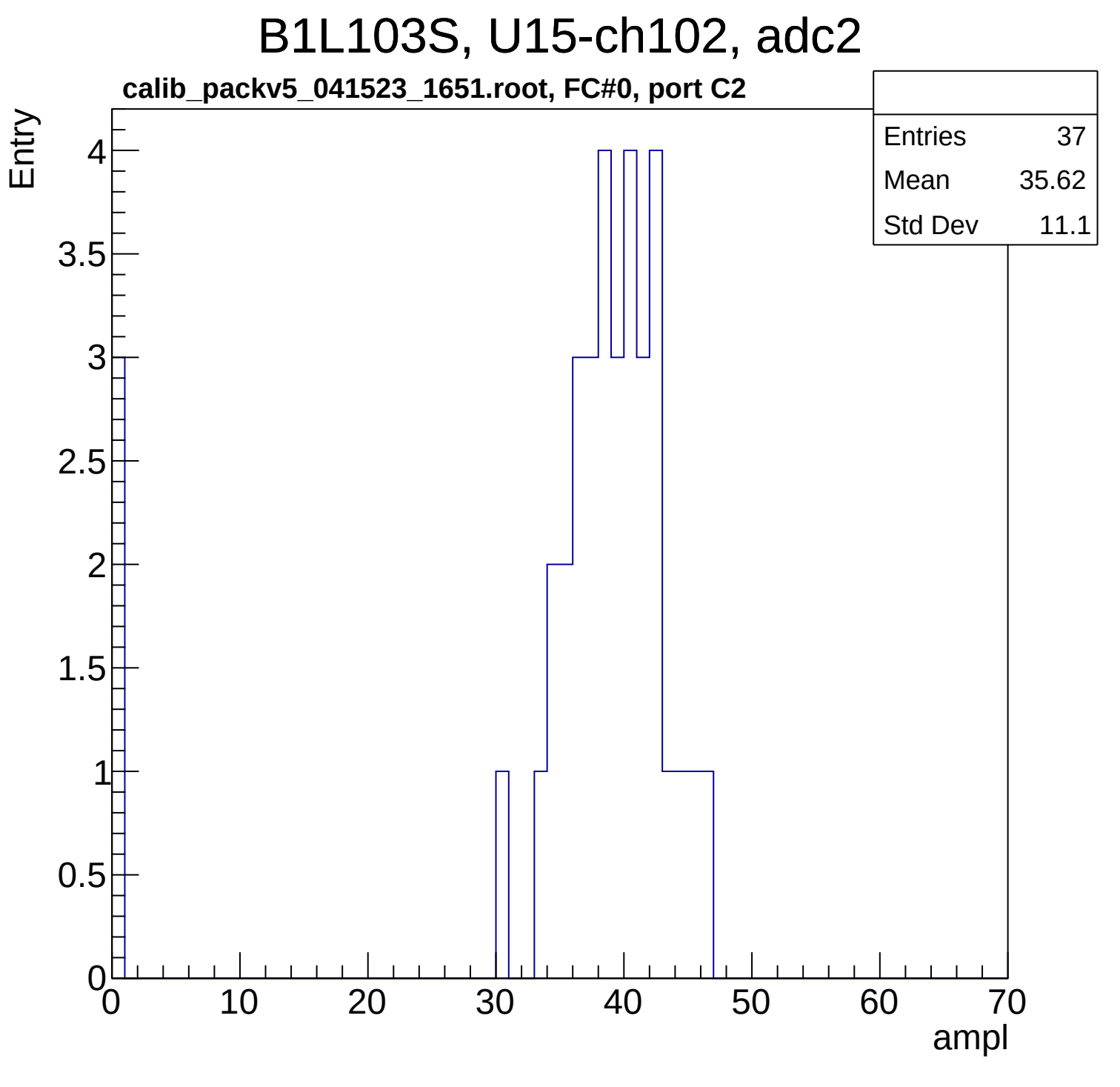
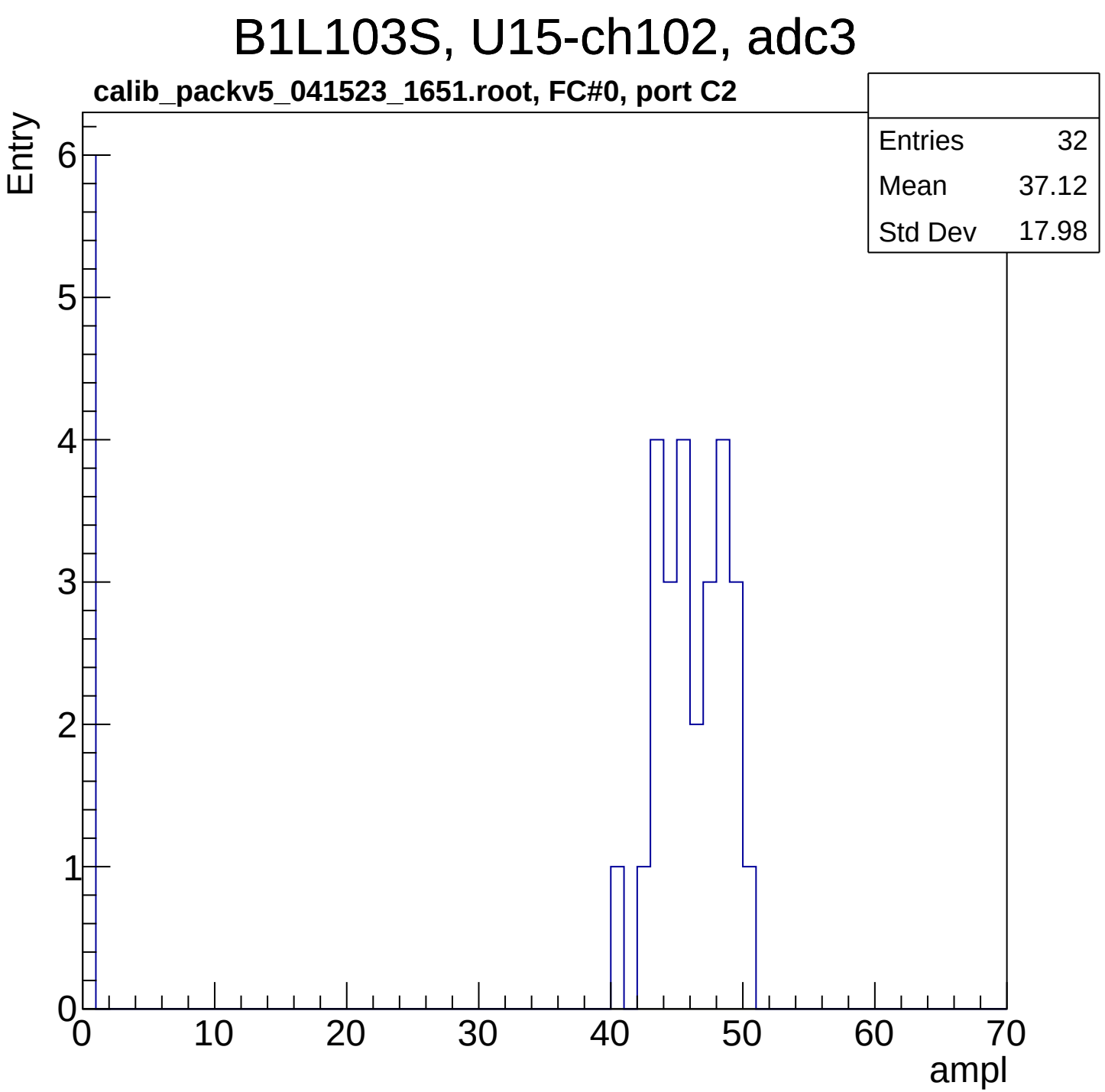
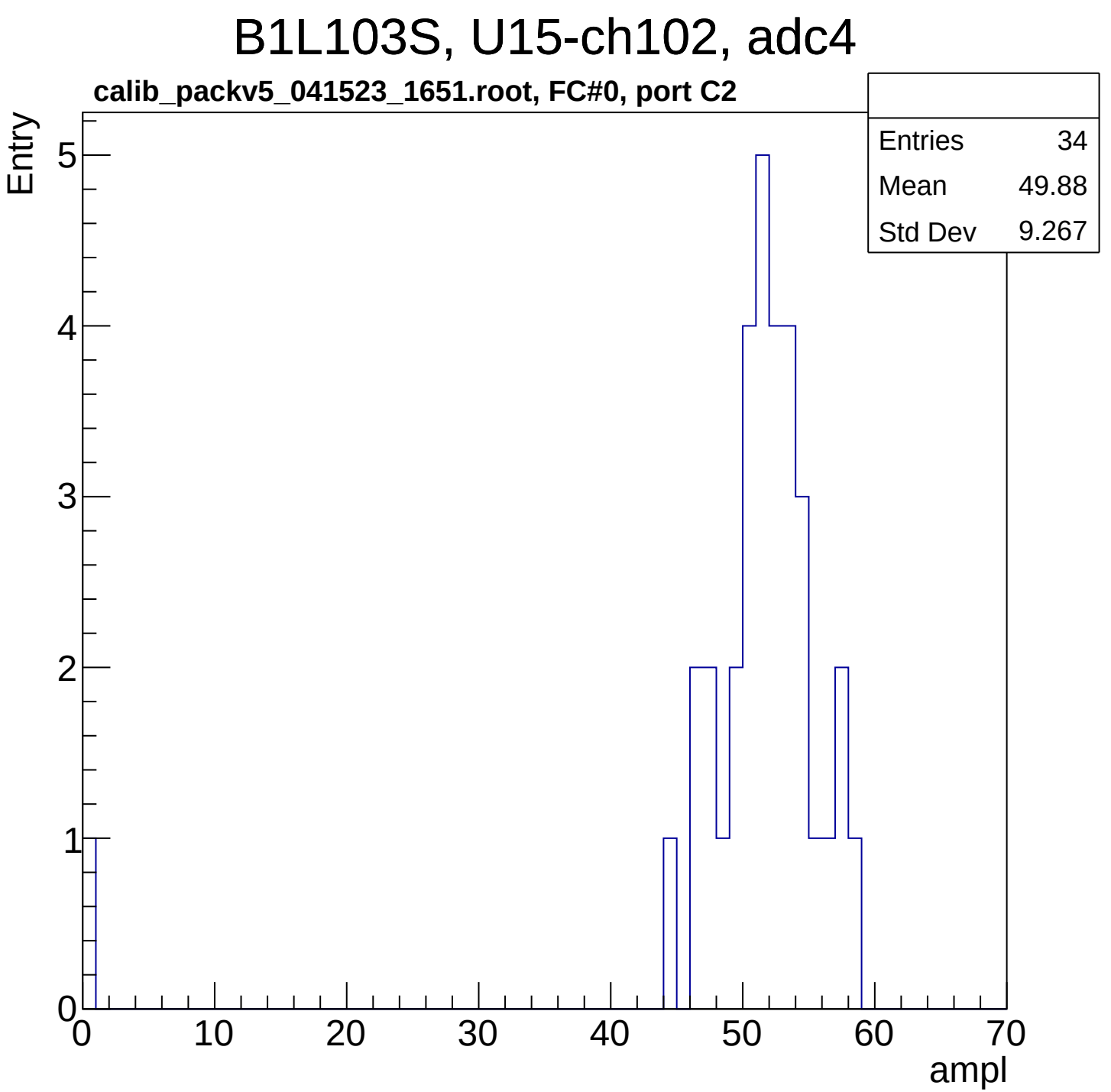
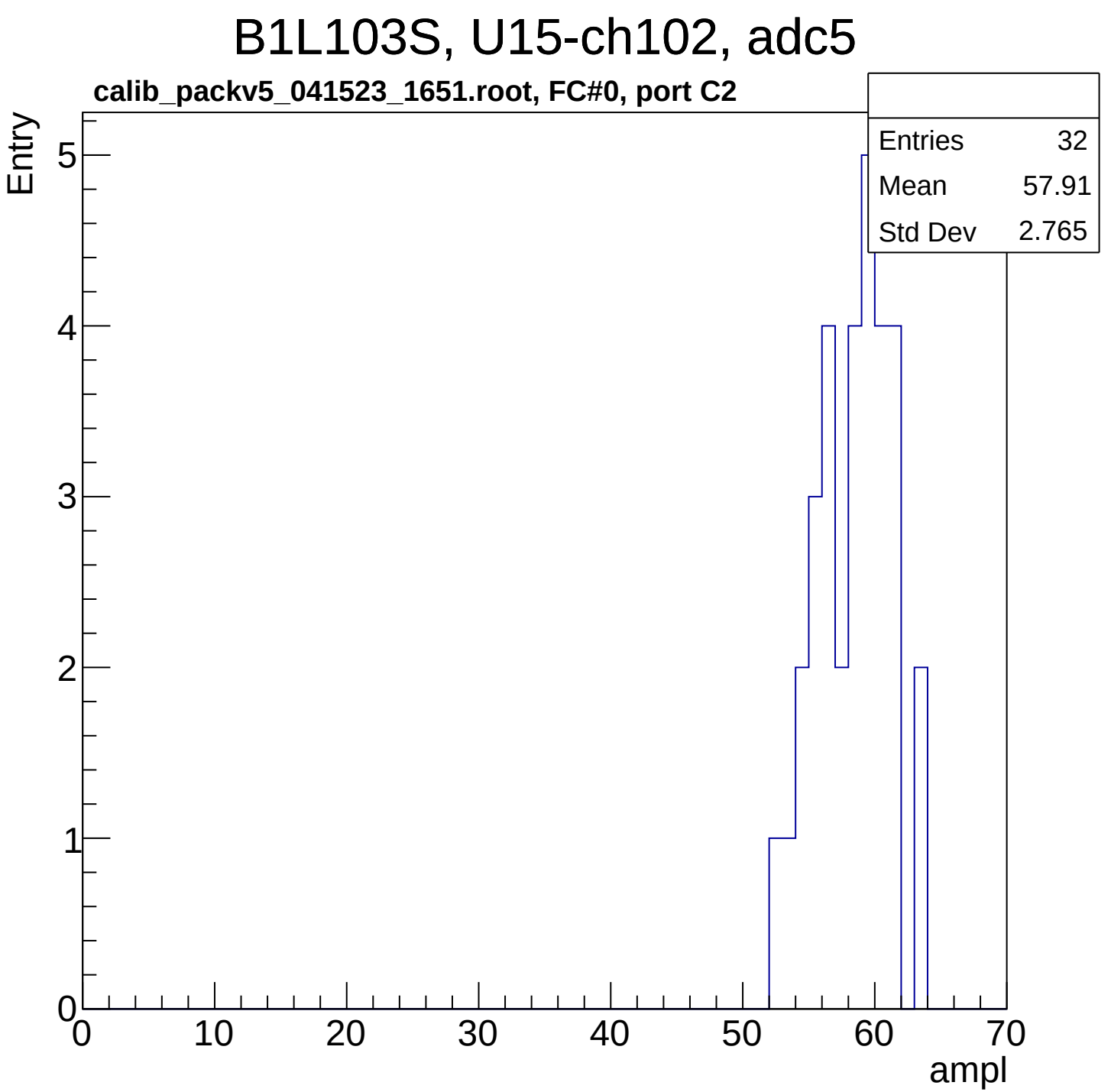
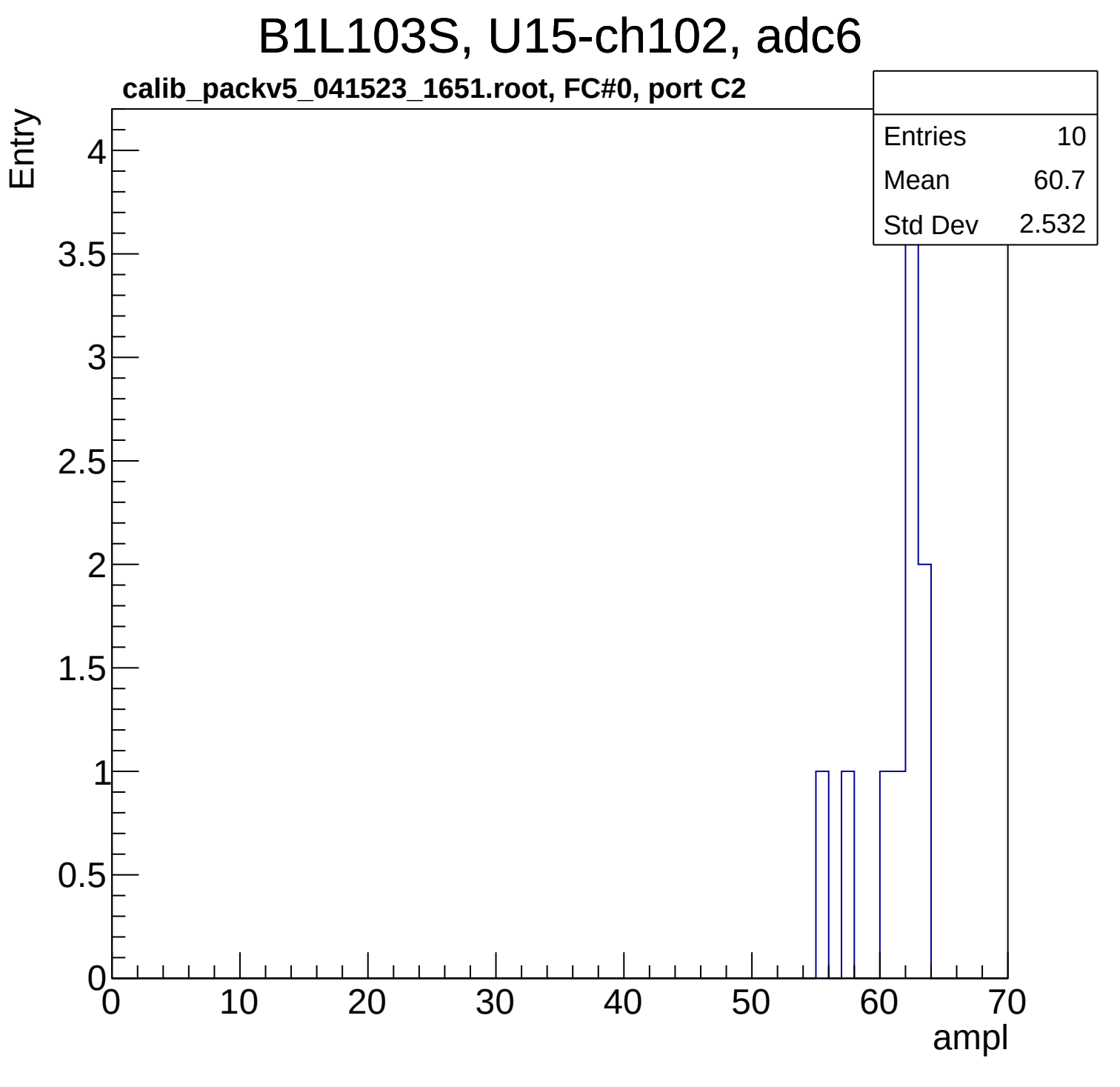
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch102, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 35.62
Std Dev 11.1
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch102, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 37.12
Std Dev 17.98
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch102, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 49.88
Std Dev 9.267
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch102, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 57.91
Std Dev 2.765
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch102, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 60.7
Std Dev 2.532
Entry
ampl
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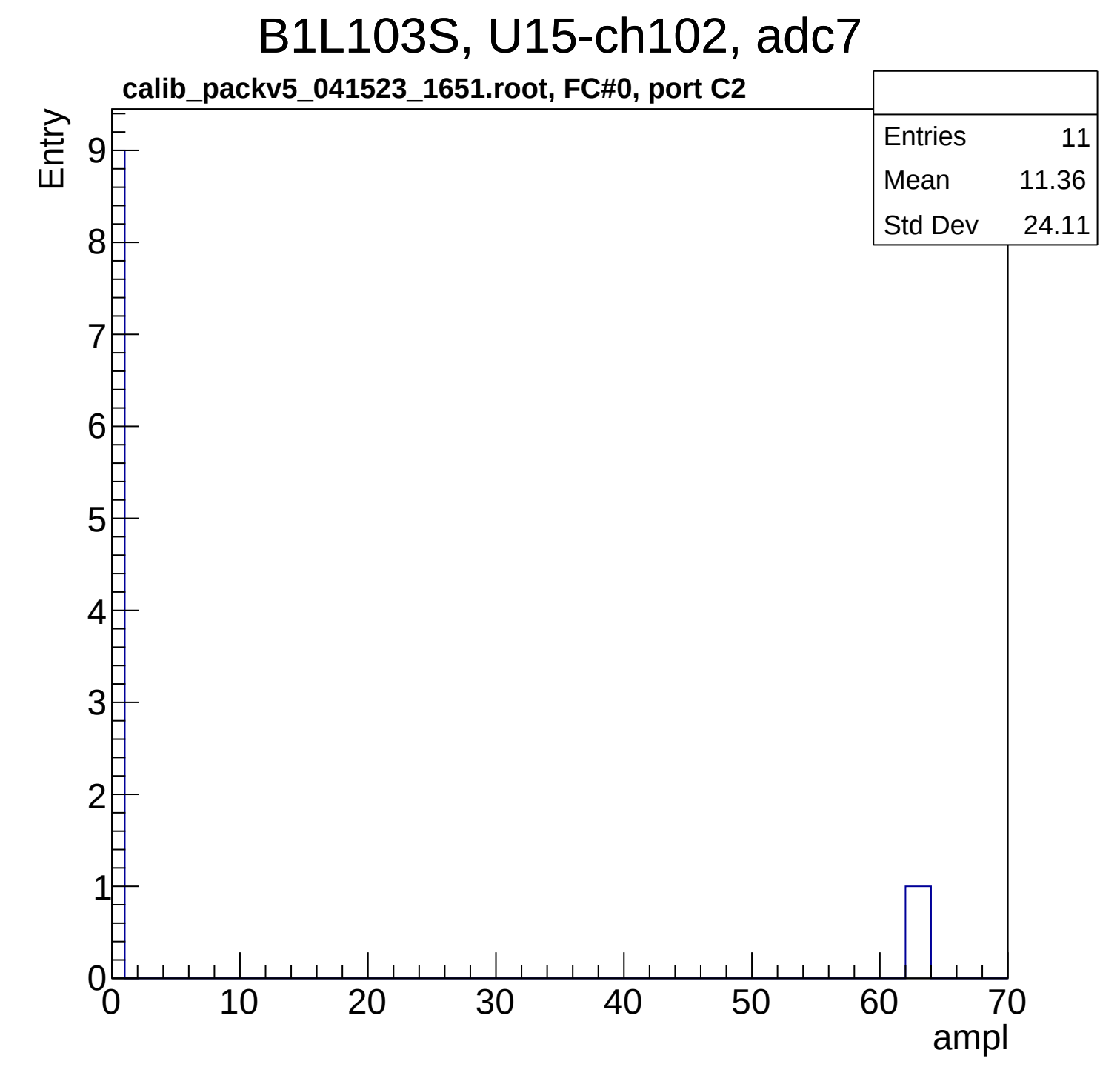
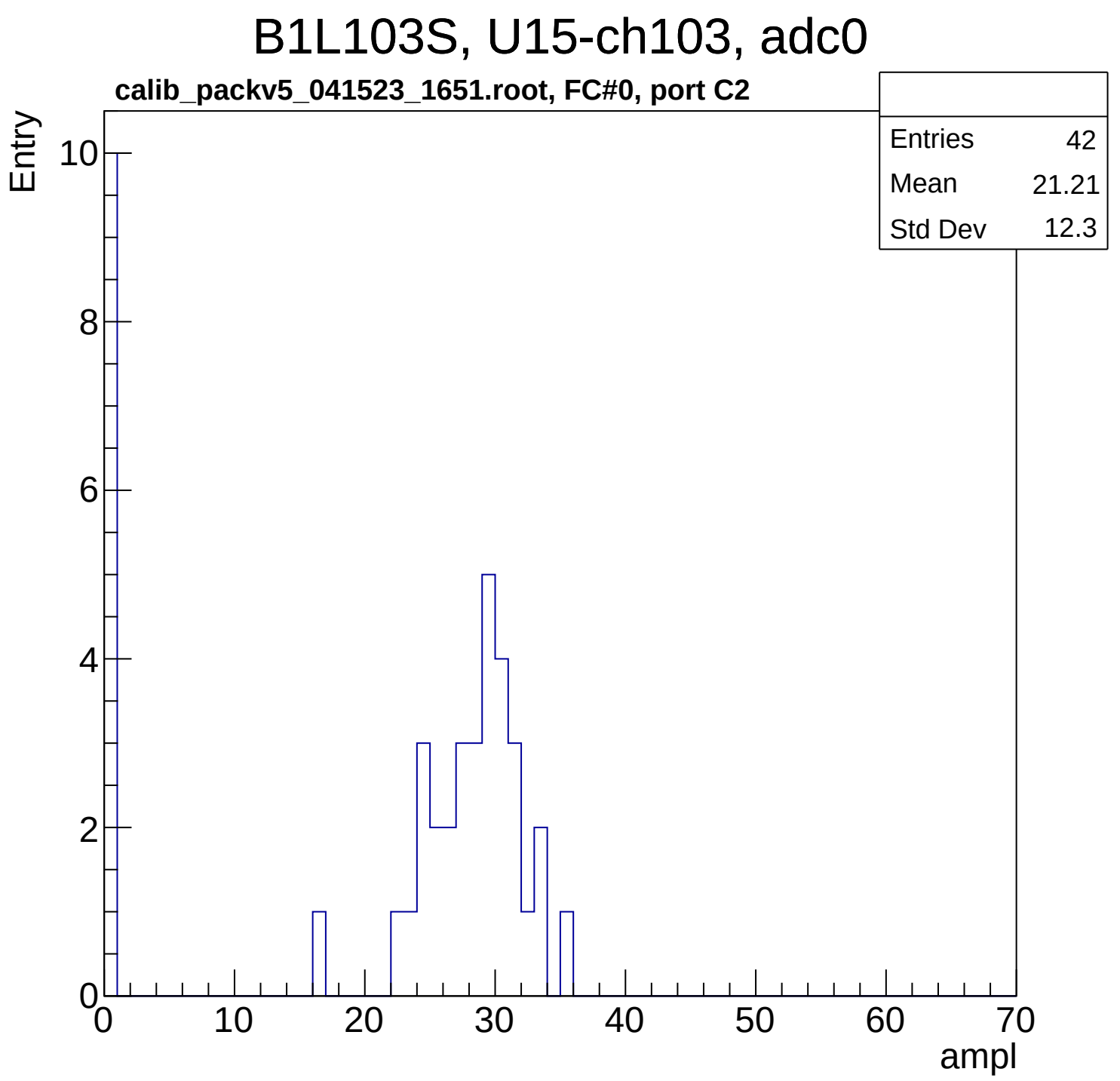
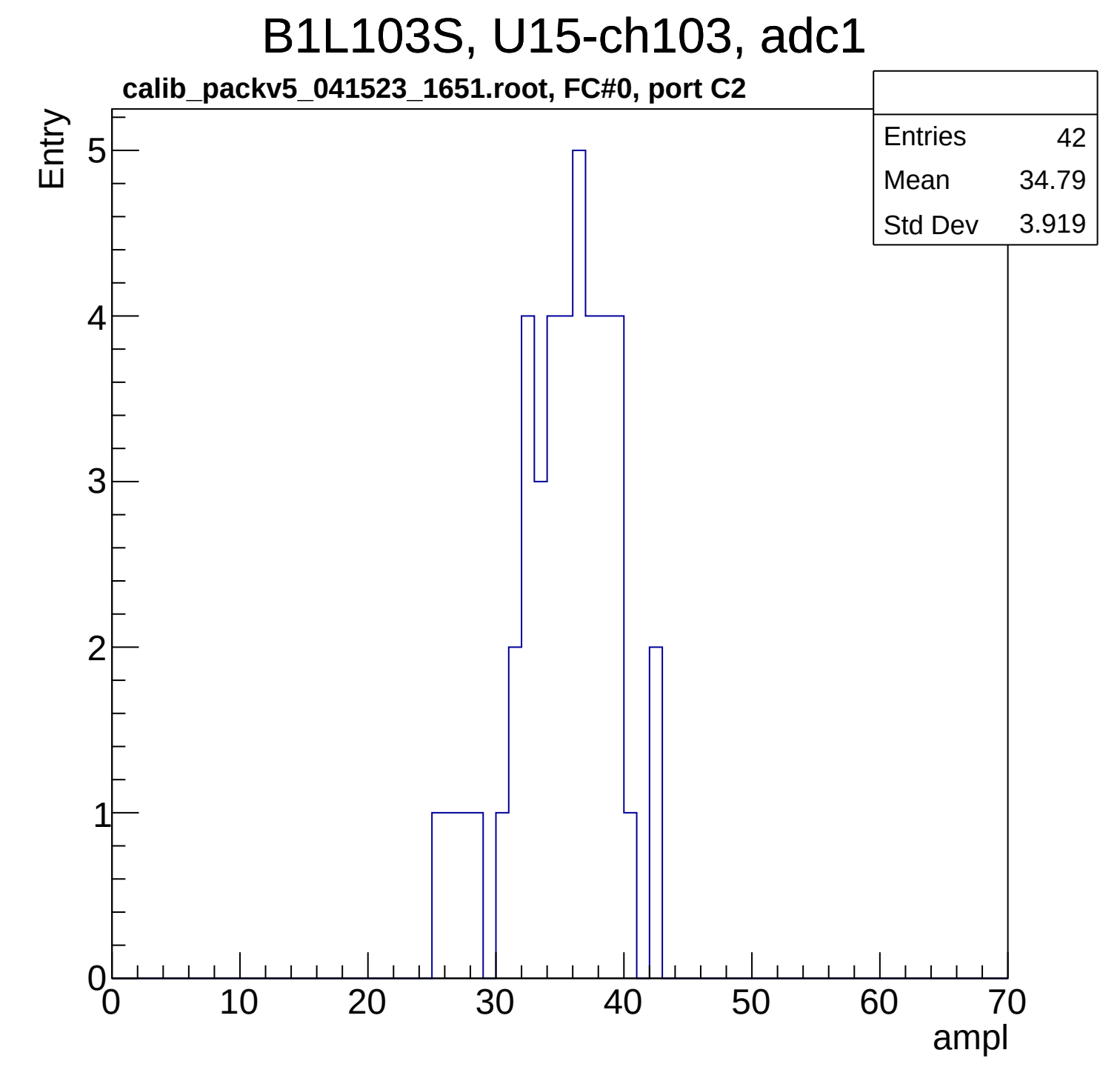
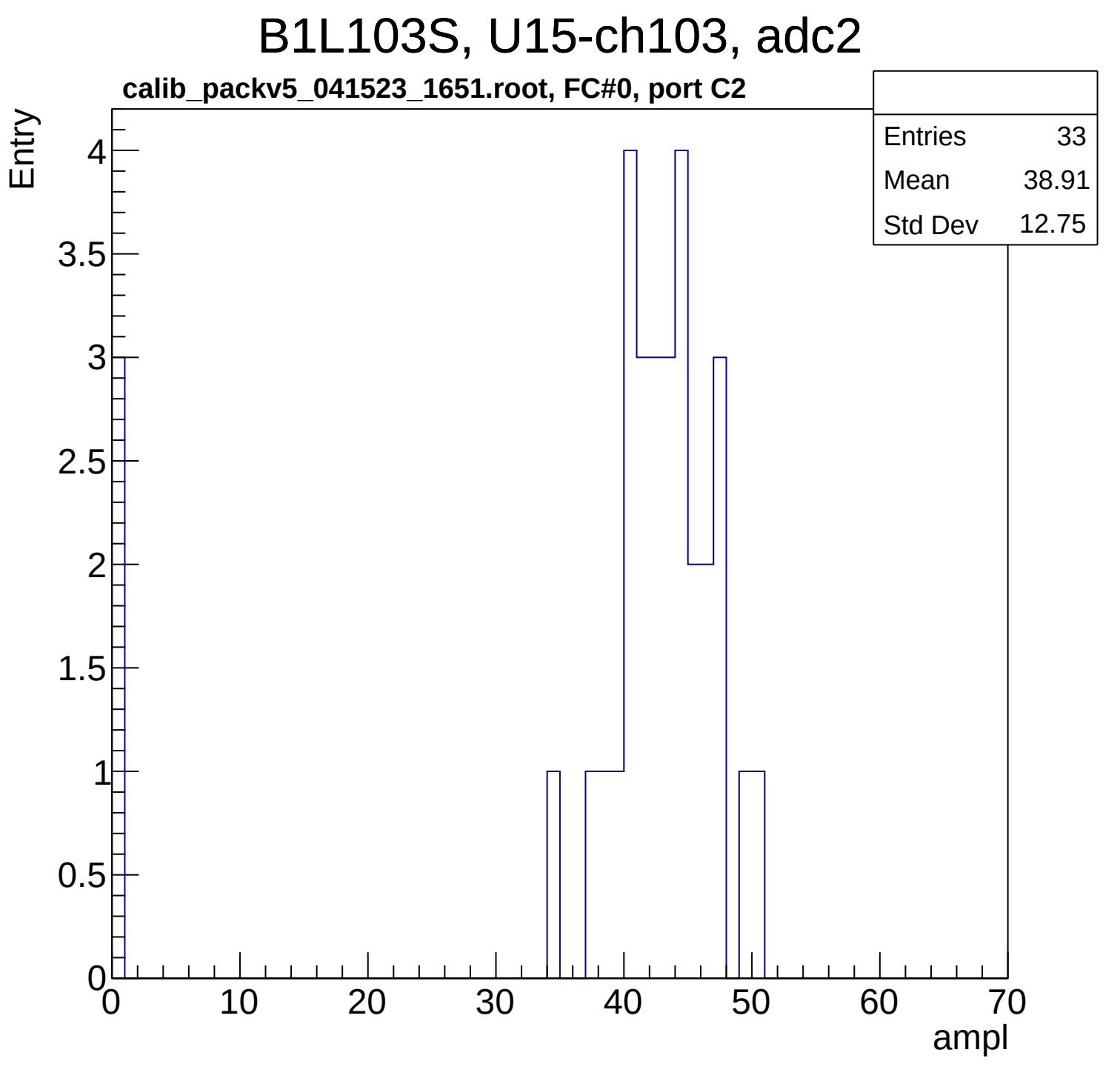
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch102, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 11.36
Std Dev 24.11
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U15-ch103, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 21.21
Std Dev 12.3
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U15-ch103, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 34.79
Std Dev 3.919
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch103, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 38.91
Std Dev 12.75
Entry
ampl
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0.5
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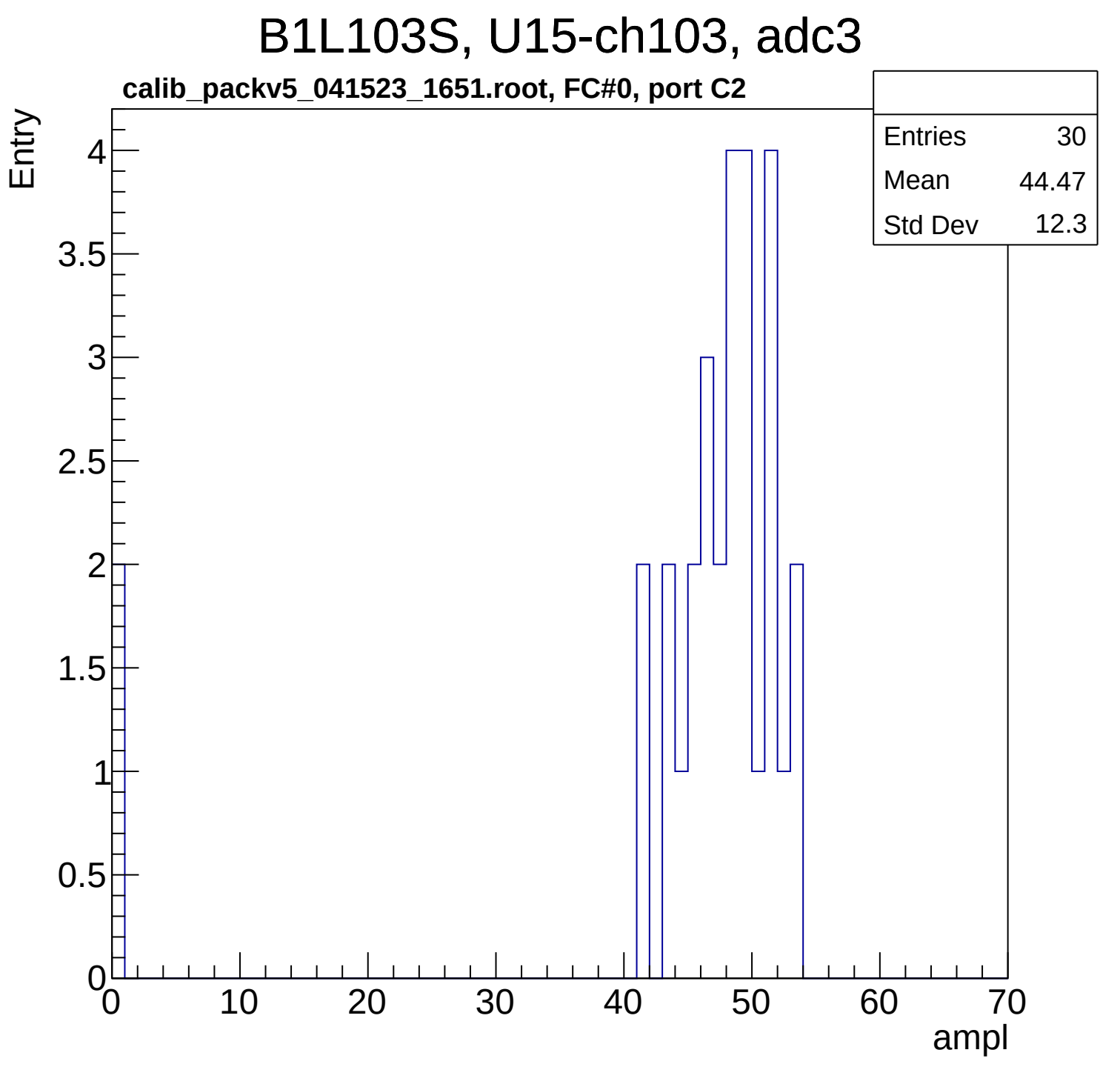
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch103, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 44.47
Std Dev 12.3
Entry
ampl
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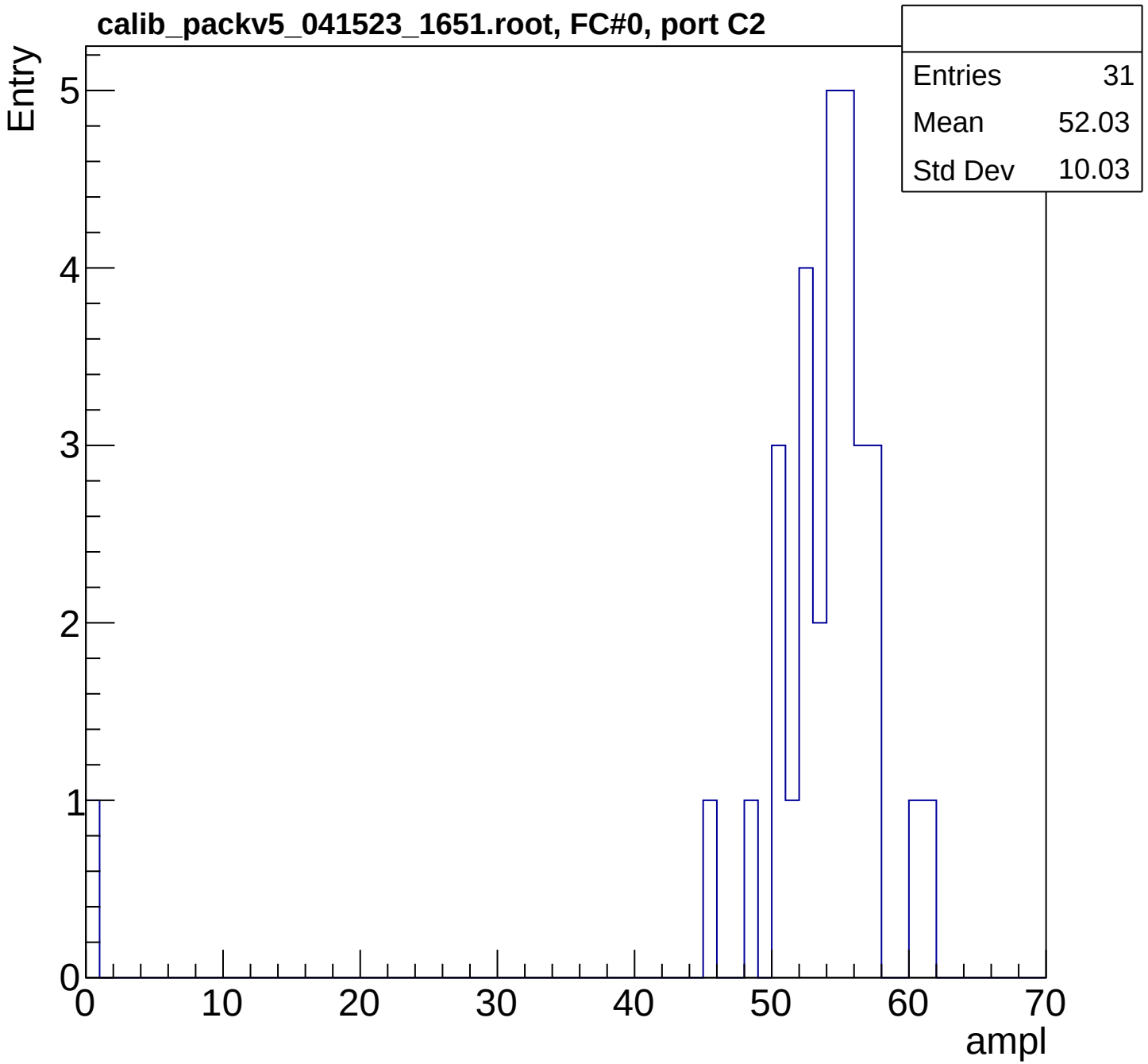
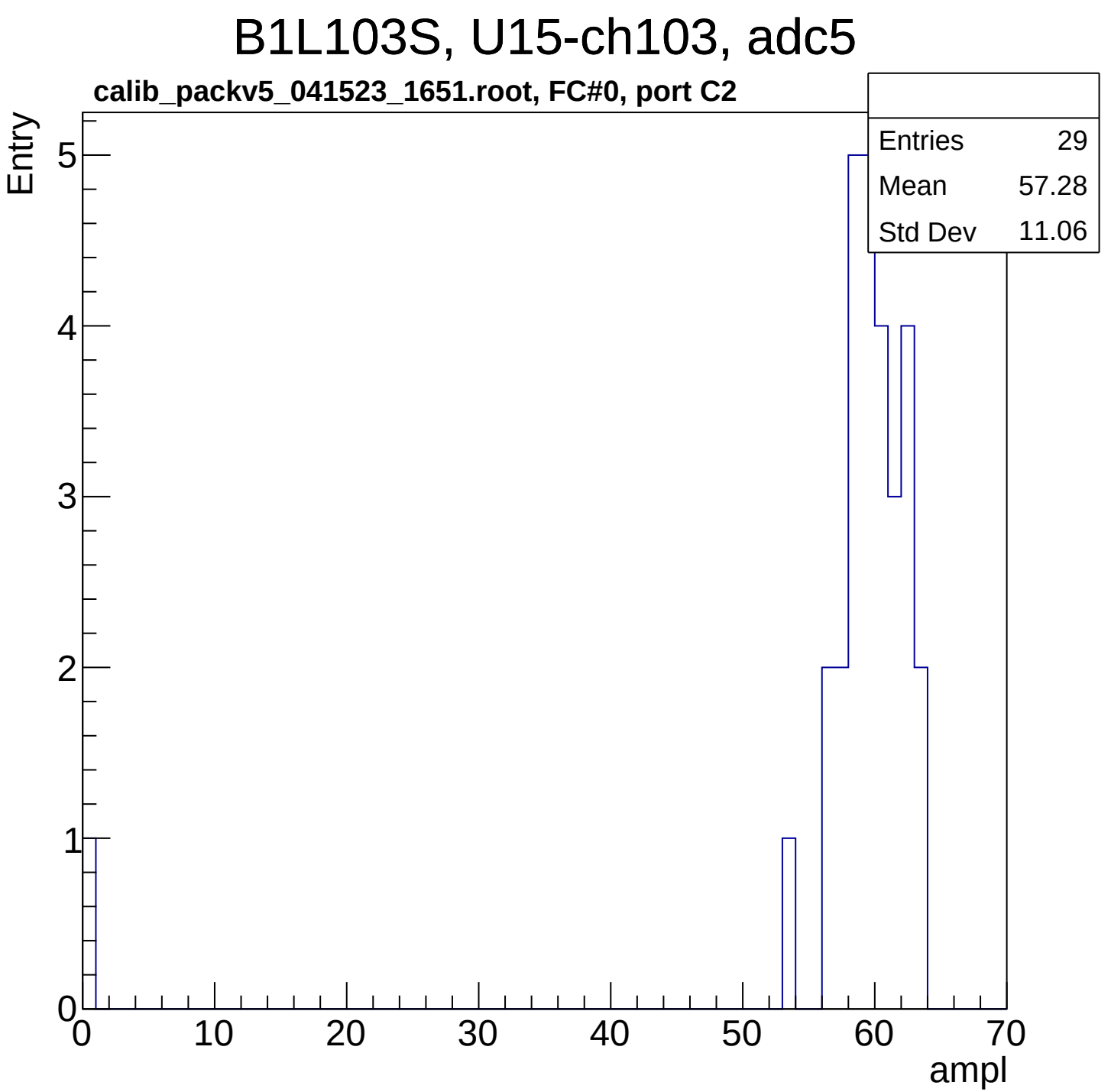
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch103, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 52.03
Std Dev 10.03
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch103, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 57.28
Std Dev 11.06
Entry
0
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2
3
4
5
0
10
20
30
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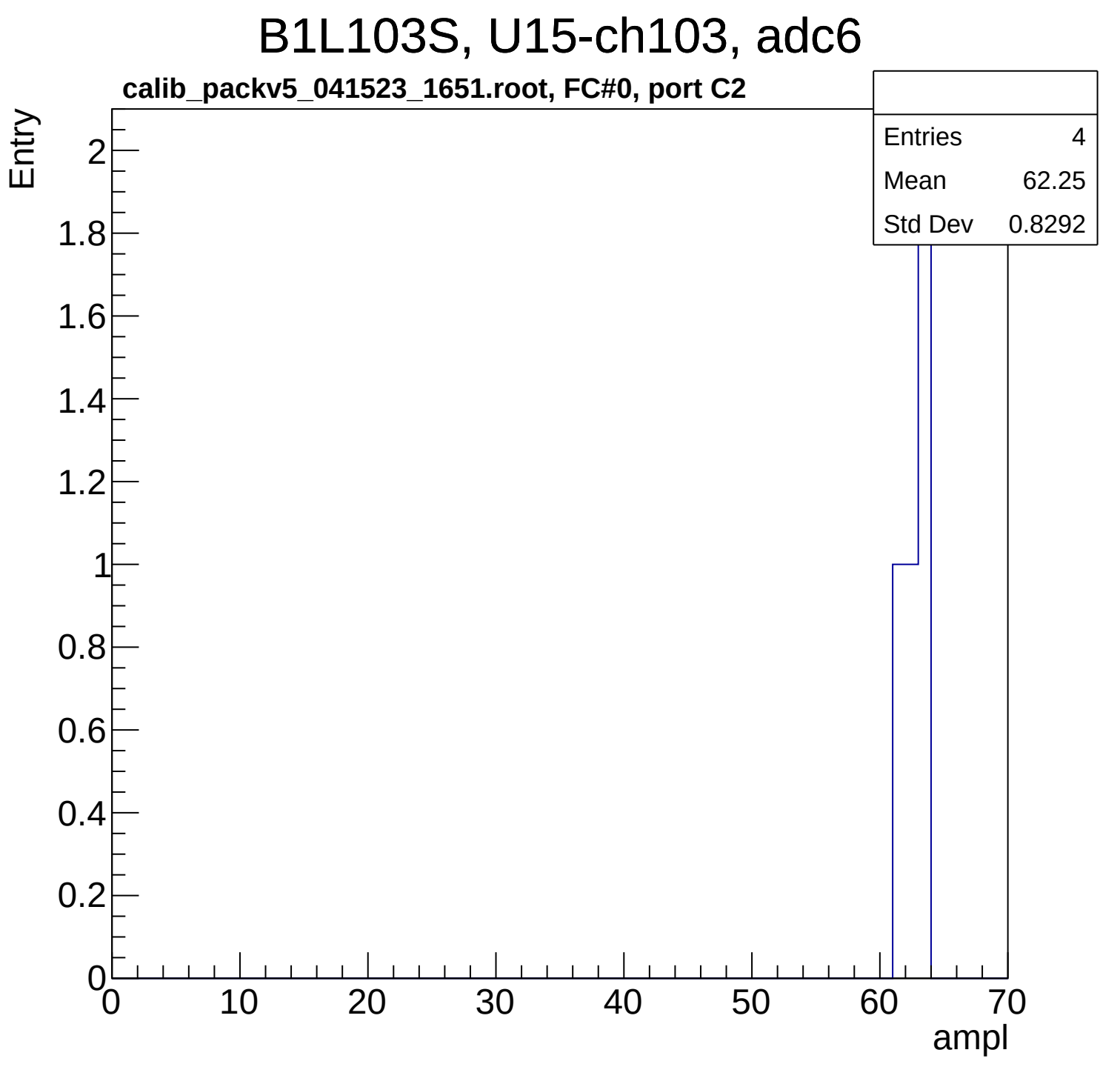
50
60
70
ampl


B1L103S, U15-ch103, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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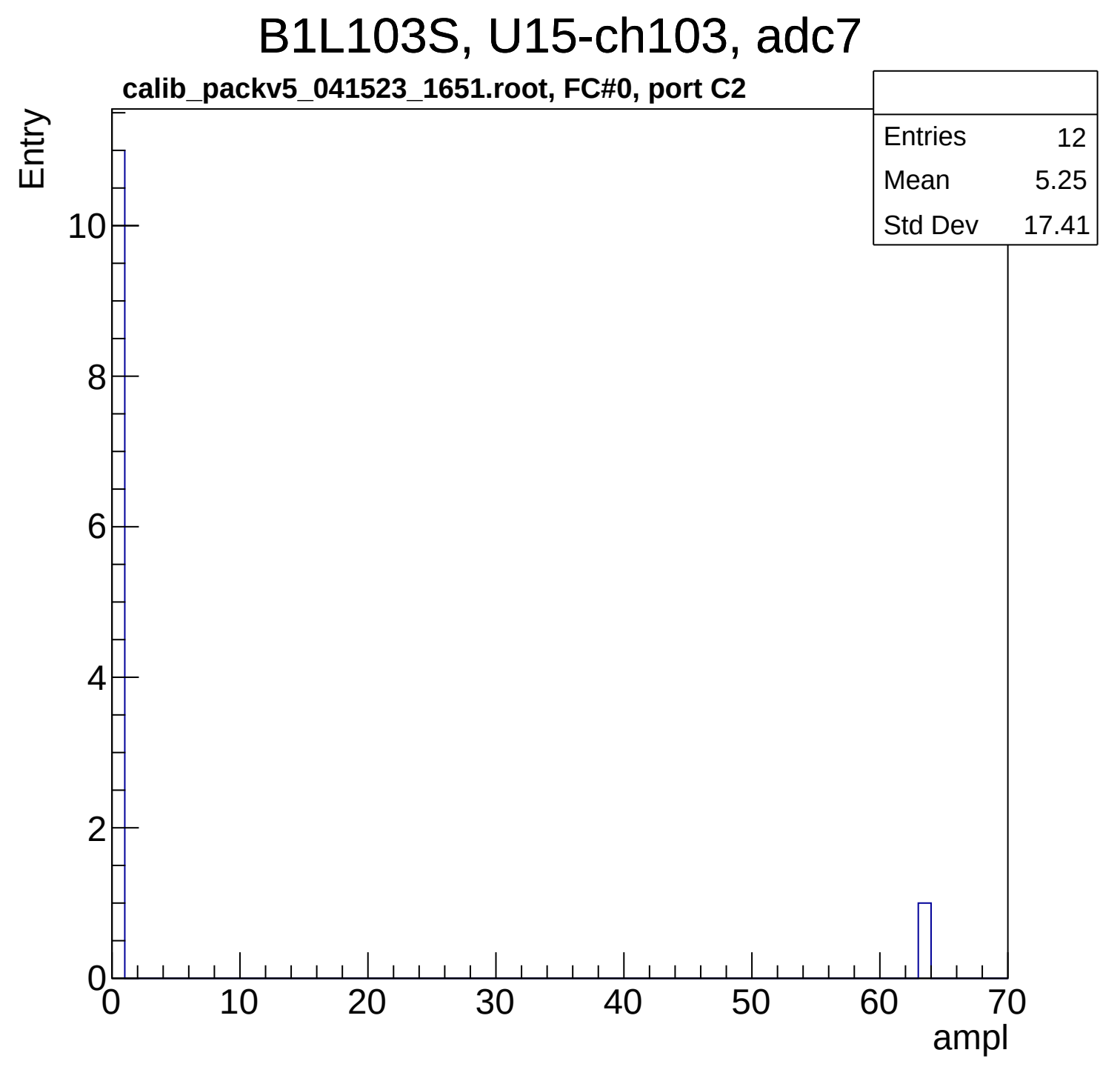
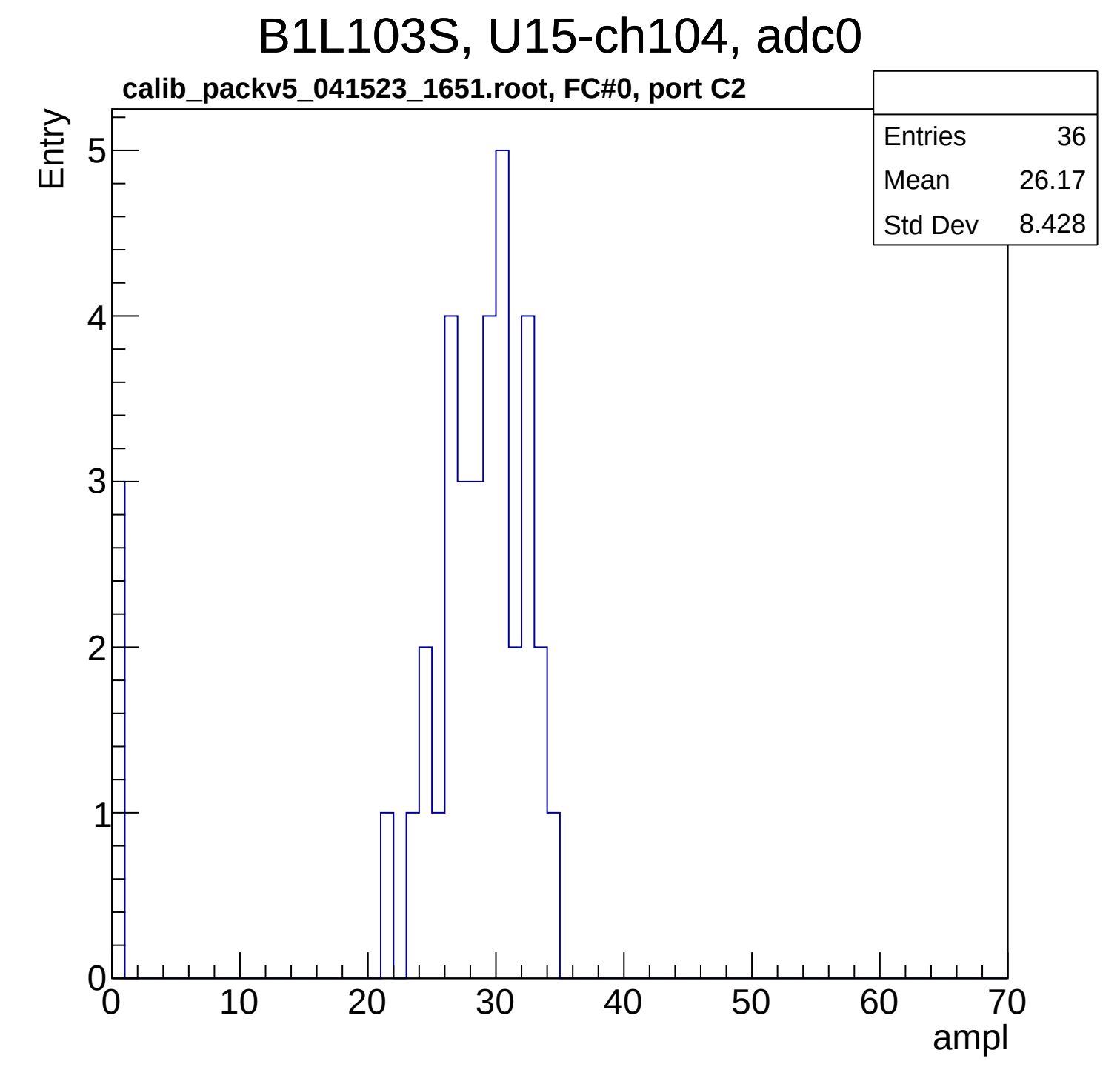
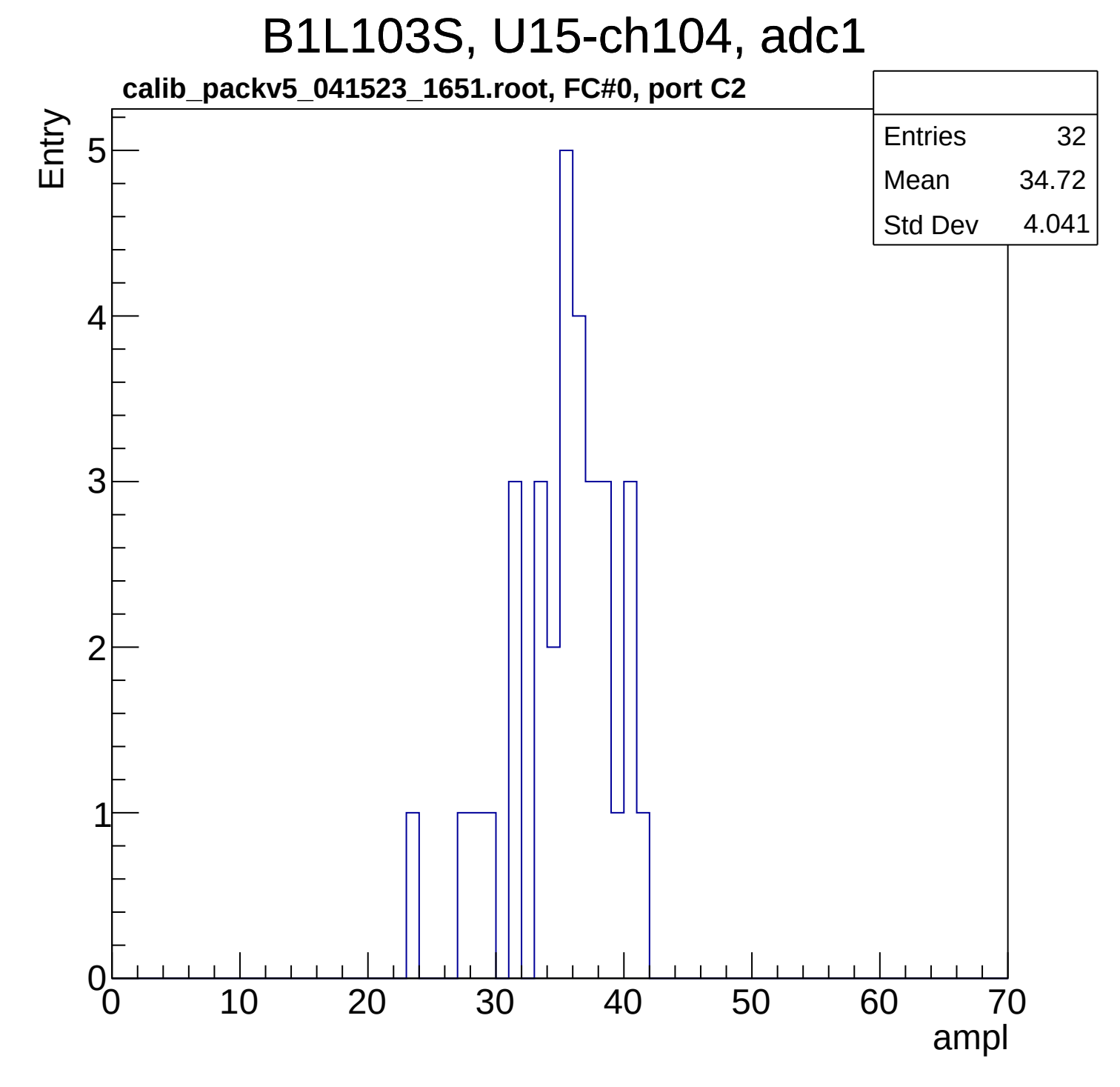
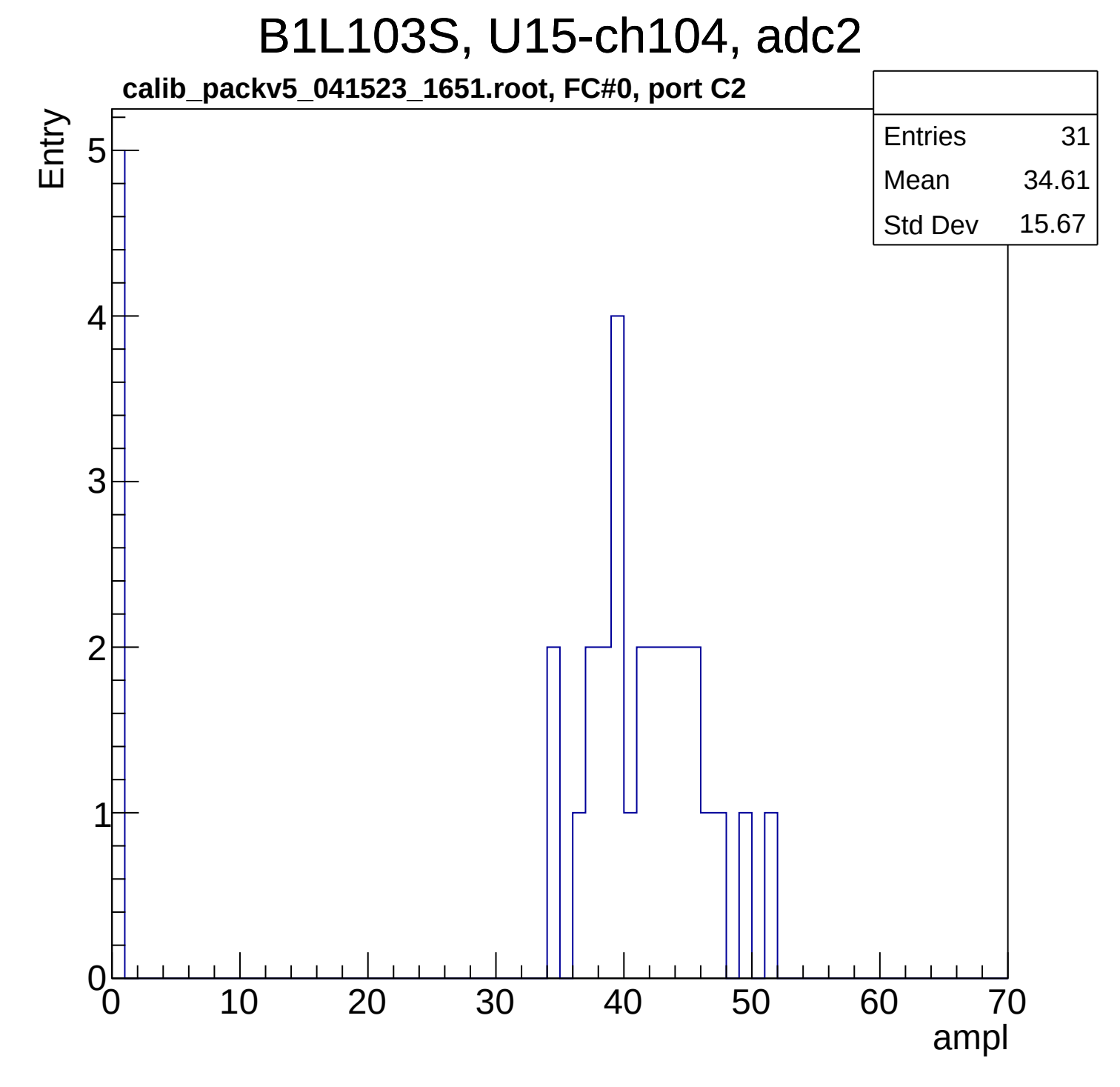
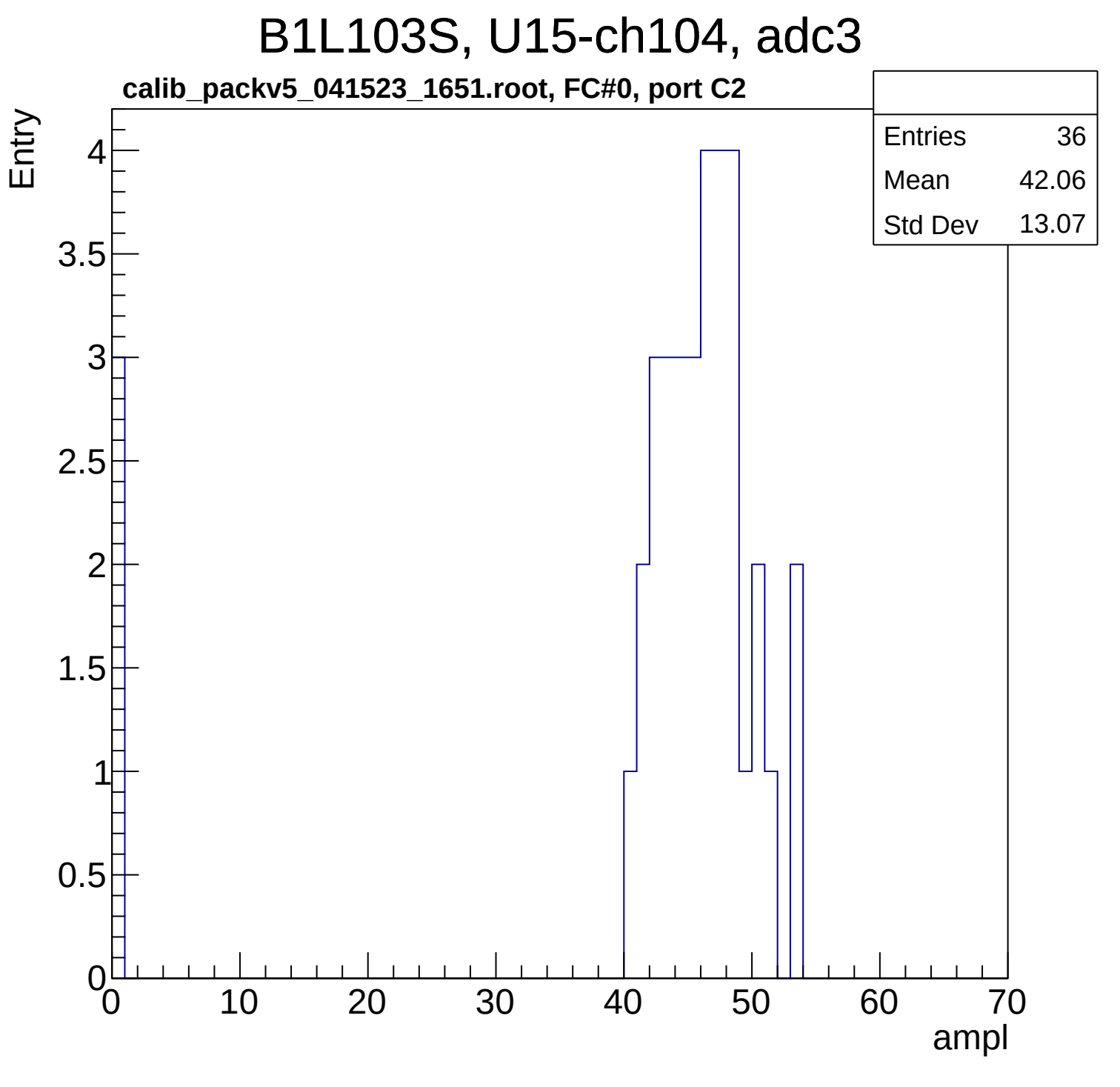

B1L103S, U15-ch103, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 5.25
Std Dev 17.41
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch104, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 26.17
Std Dev 8.428
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch104, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 34.72
Std Dev 4.041
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch104, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 34.61
Std Dev 15.67
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch104, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 42.06
Std Dev 13.07
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
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40
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60
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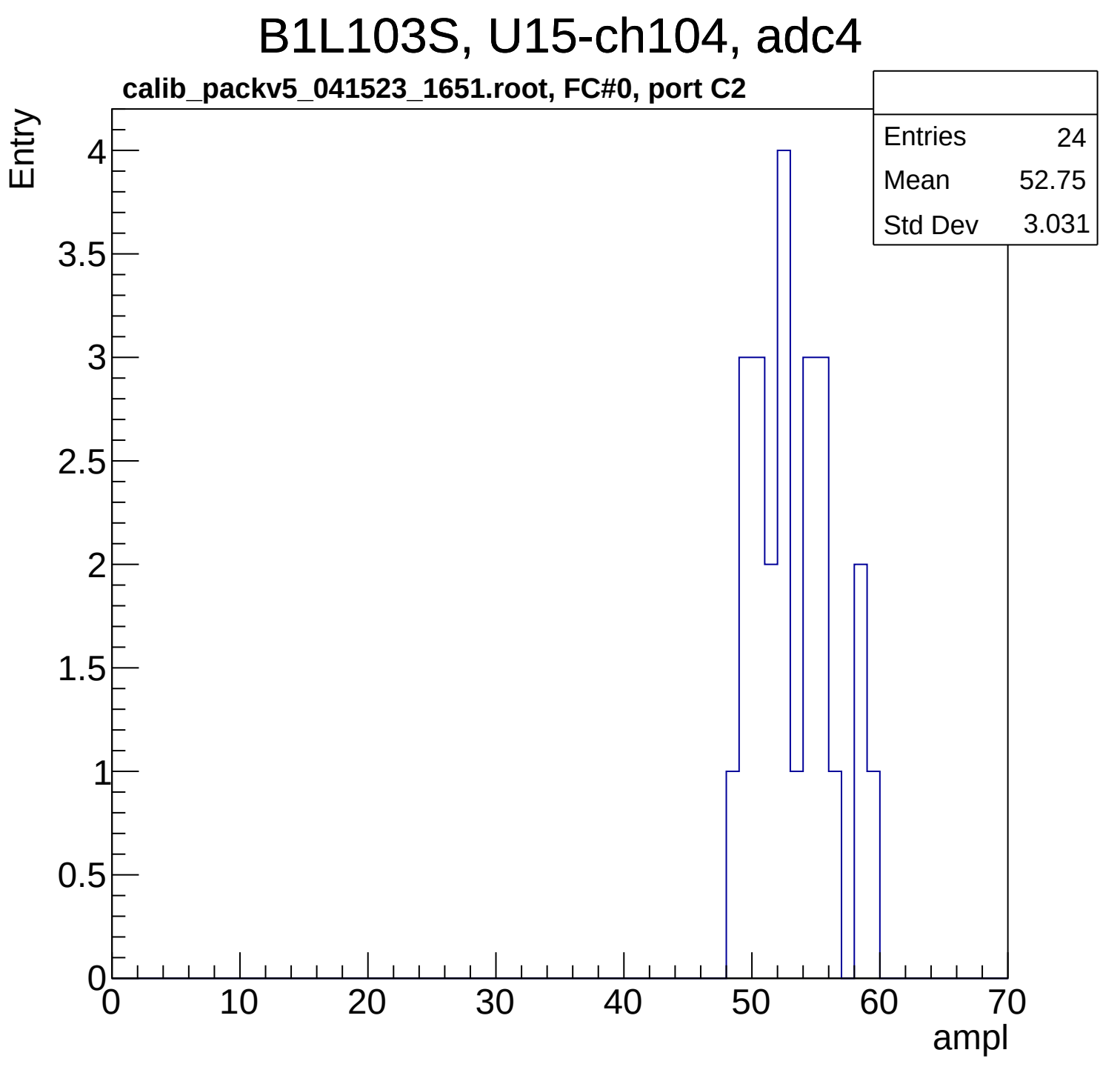
B1L103S, U15-ch104, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 52.75
Std Dev 3.031
Entry
ampl
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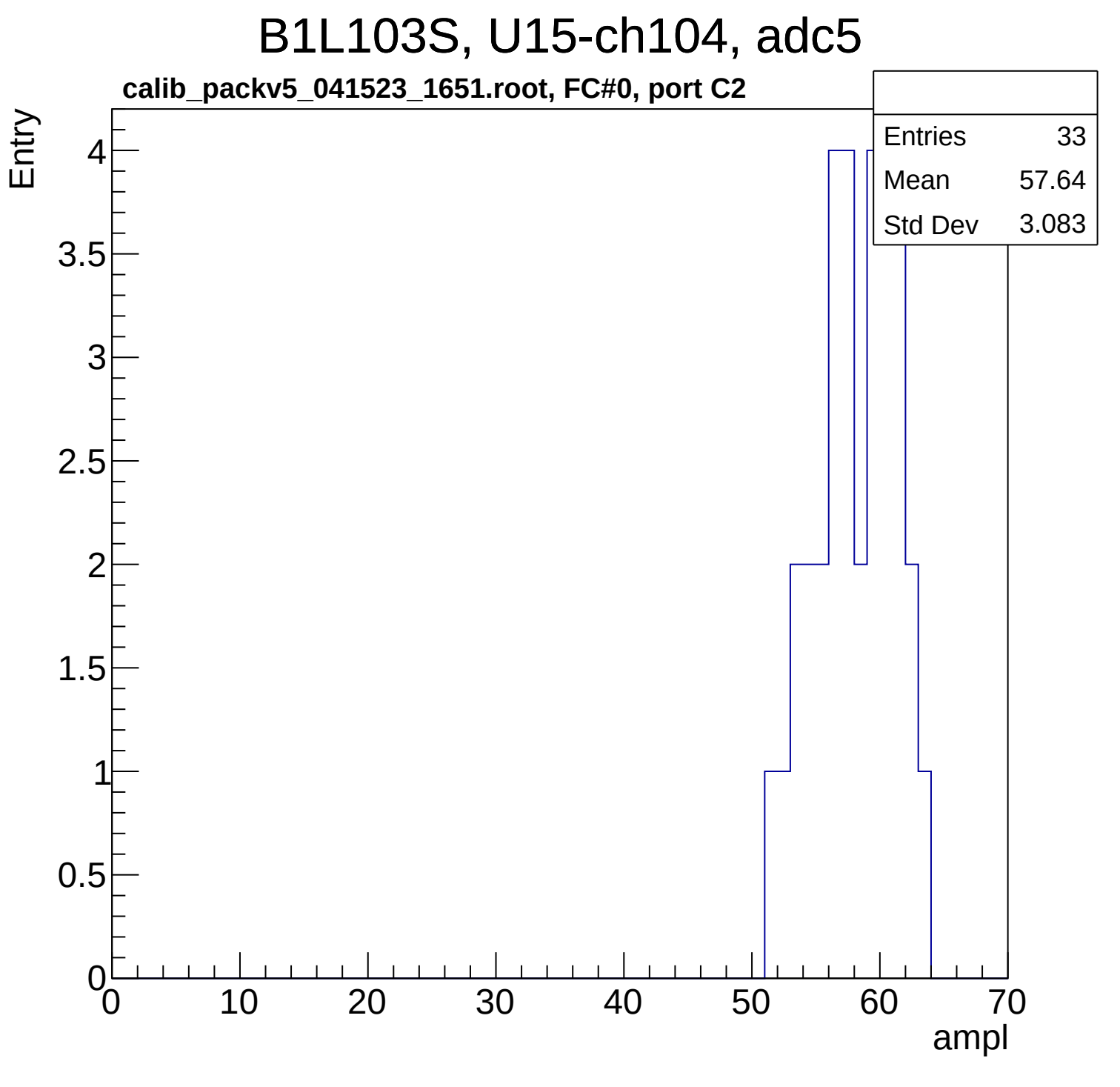
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch104, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 57.64
Std Dev 3.083
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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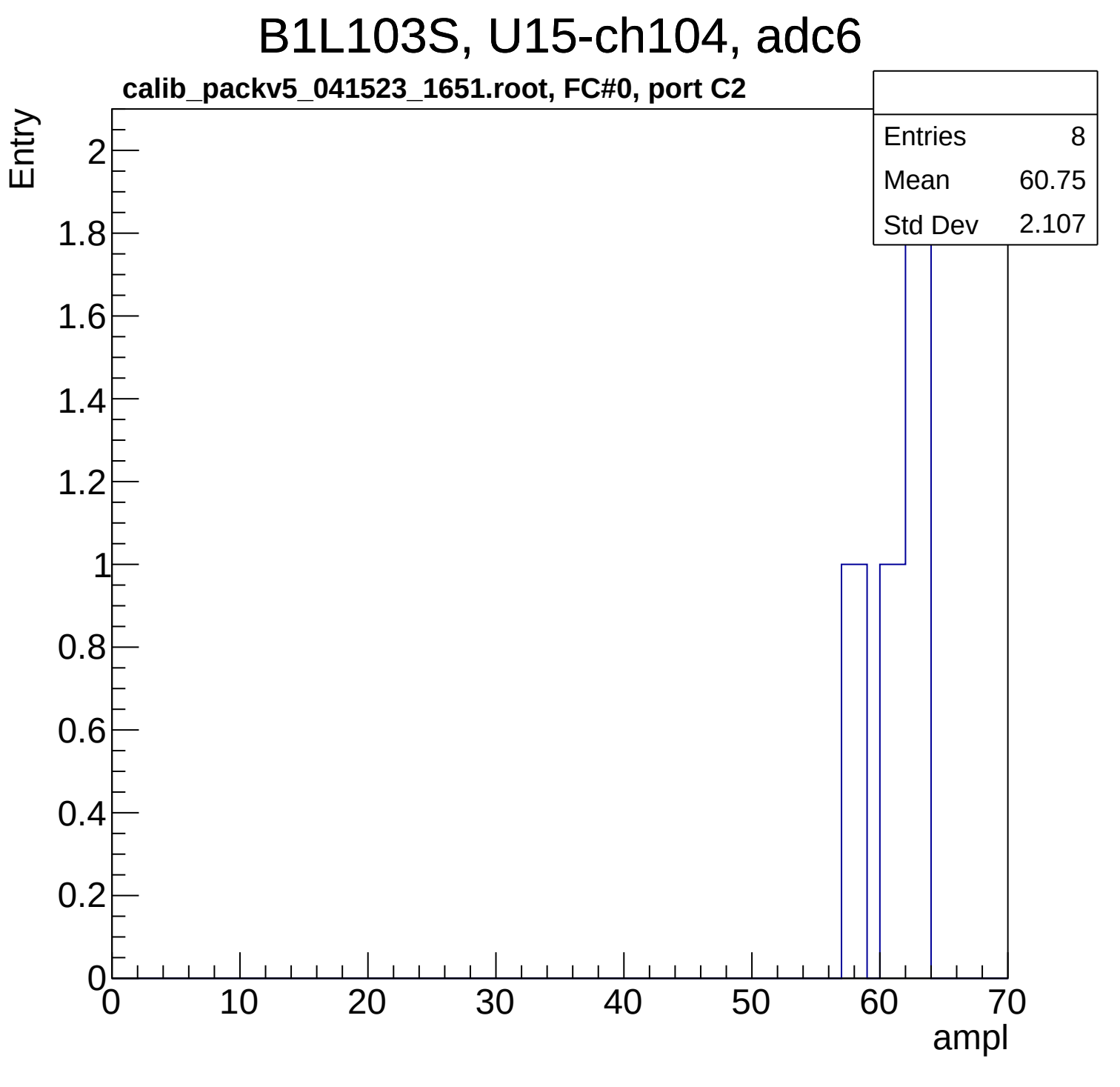
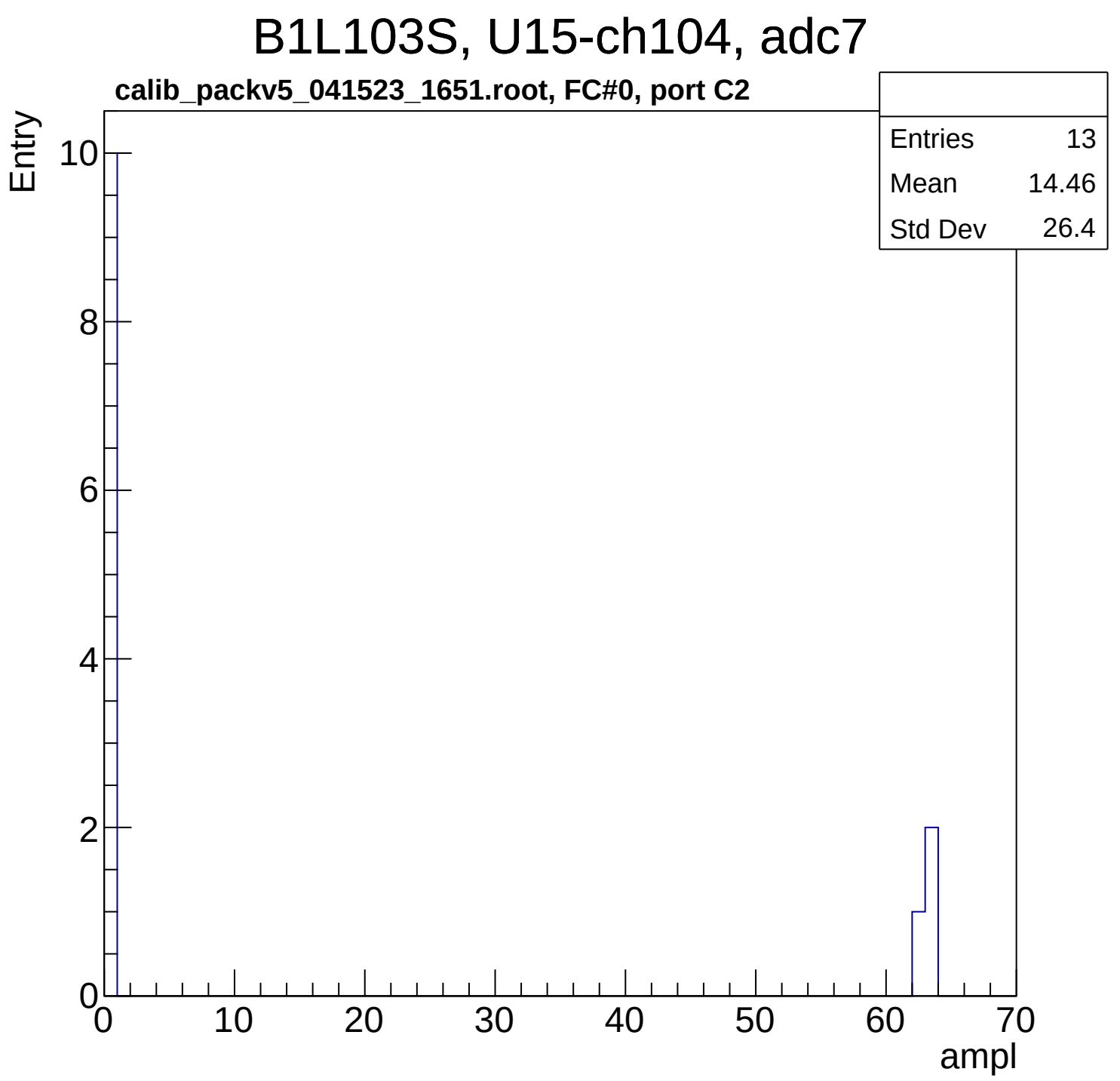
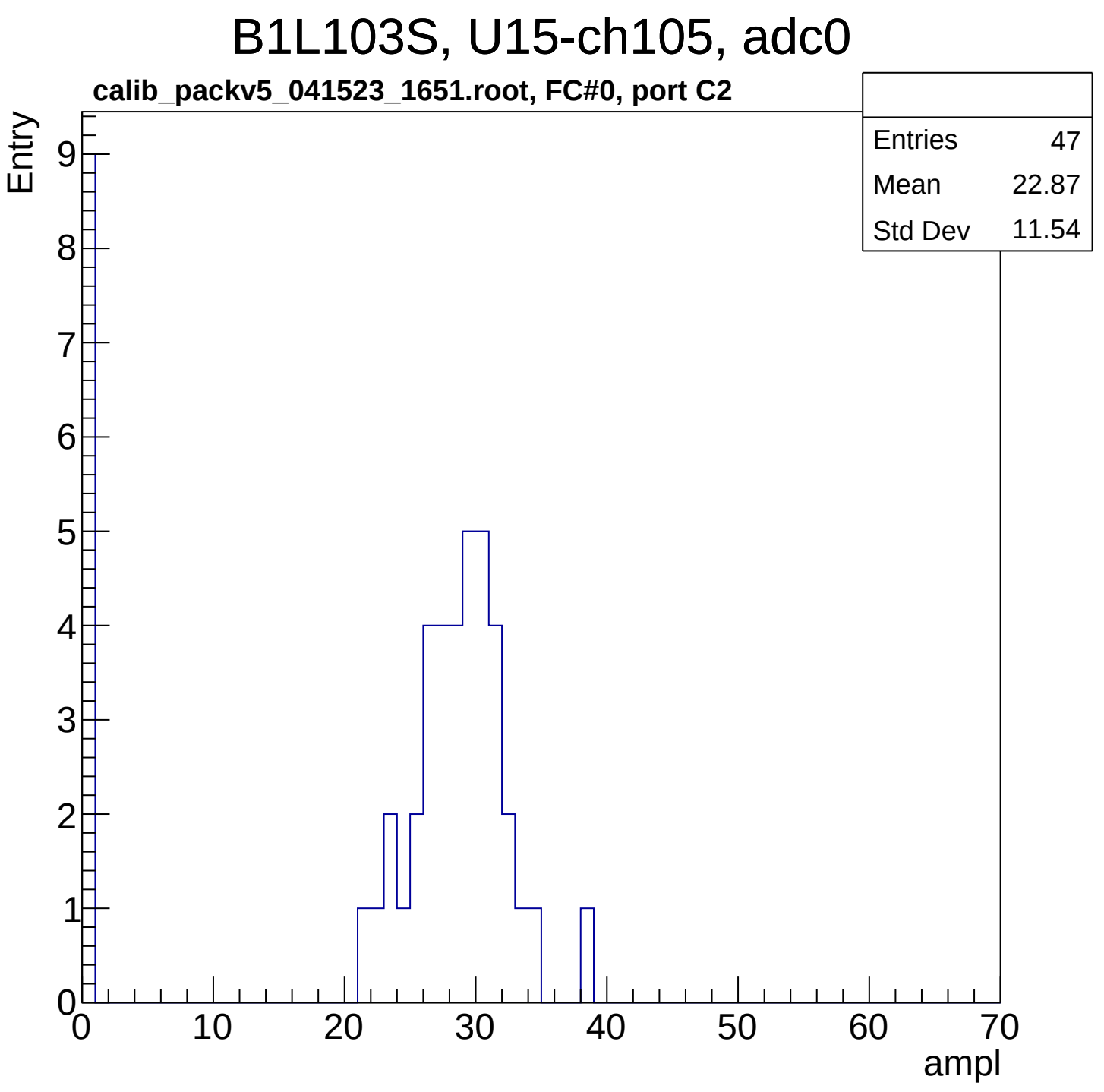

B1L103S, U15-ch104, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 60.75
Std Dev 2.107
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U15-ch104, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 14.46
Std Dev 26.4
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch105, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 22.87
Std Dev 11.54
Entry
ampl
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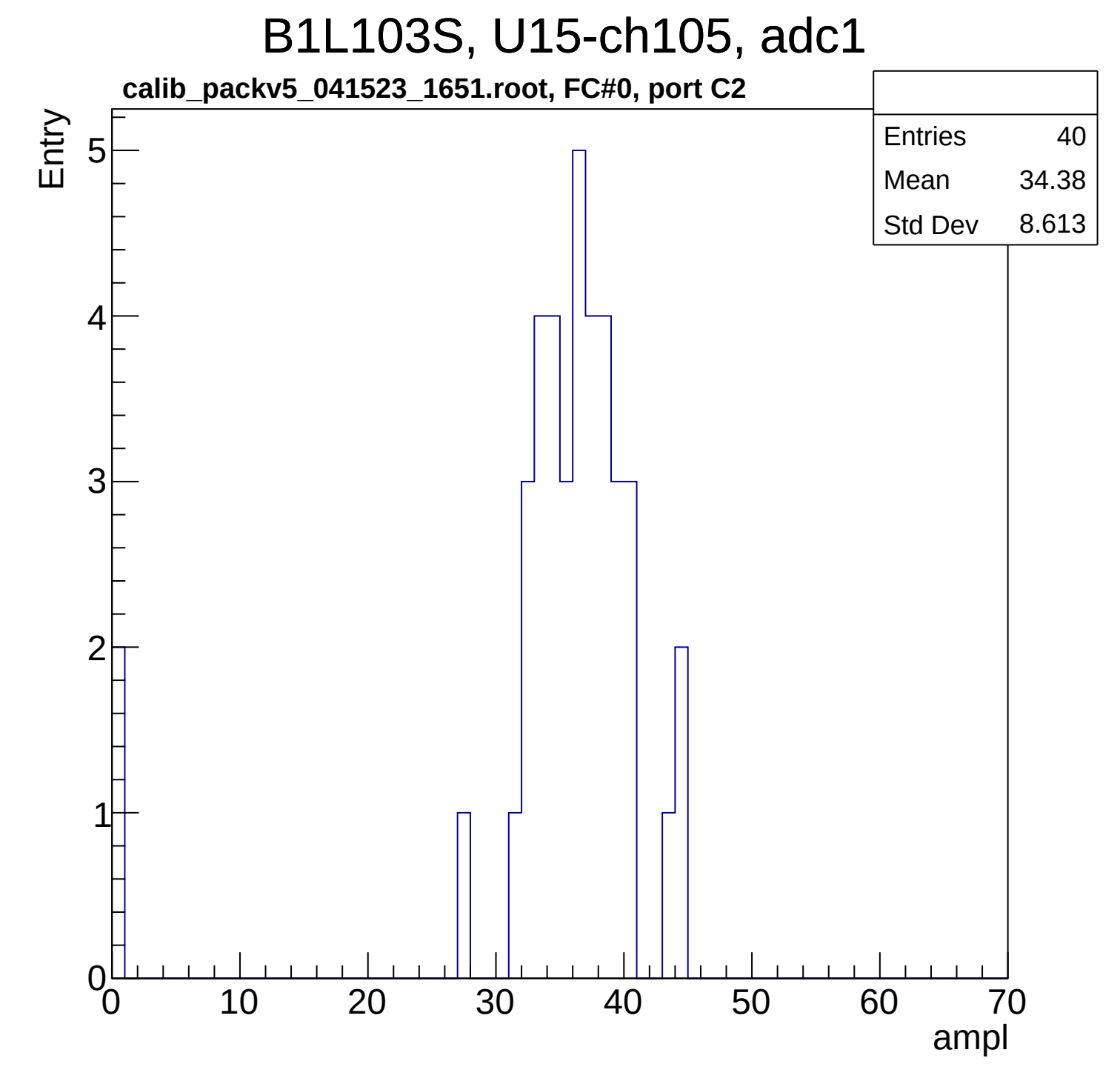
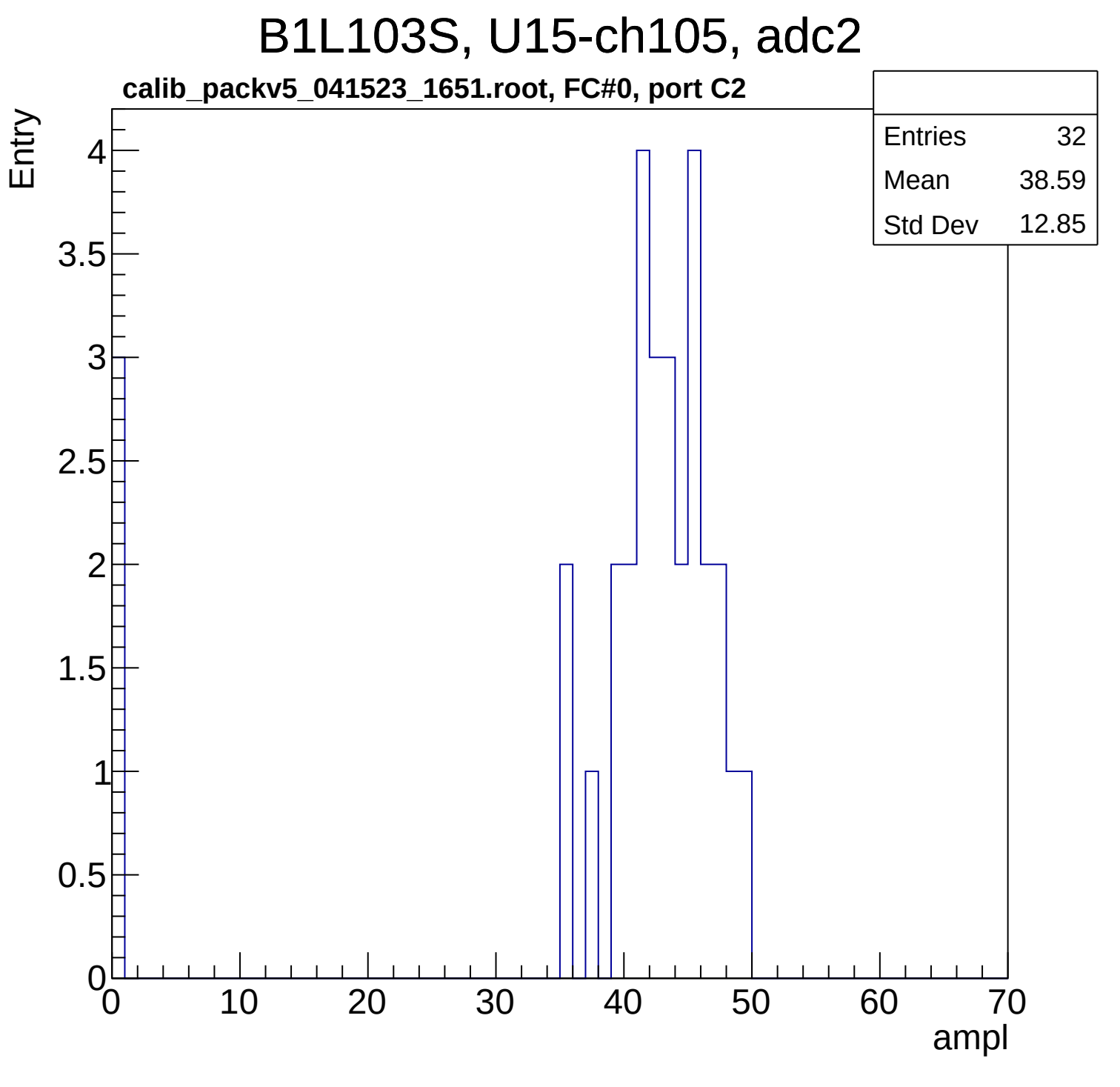
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U15-ch105, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 34.38
Std Dev 8.613
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch105, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 38.59
Std Dev 12.85
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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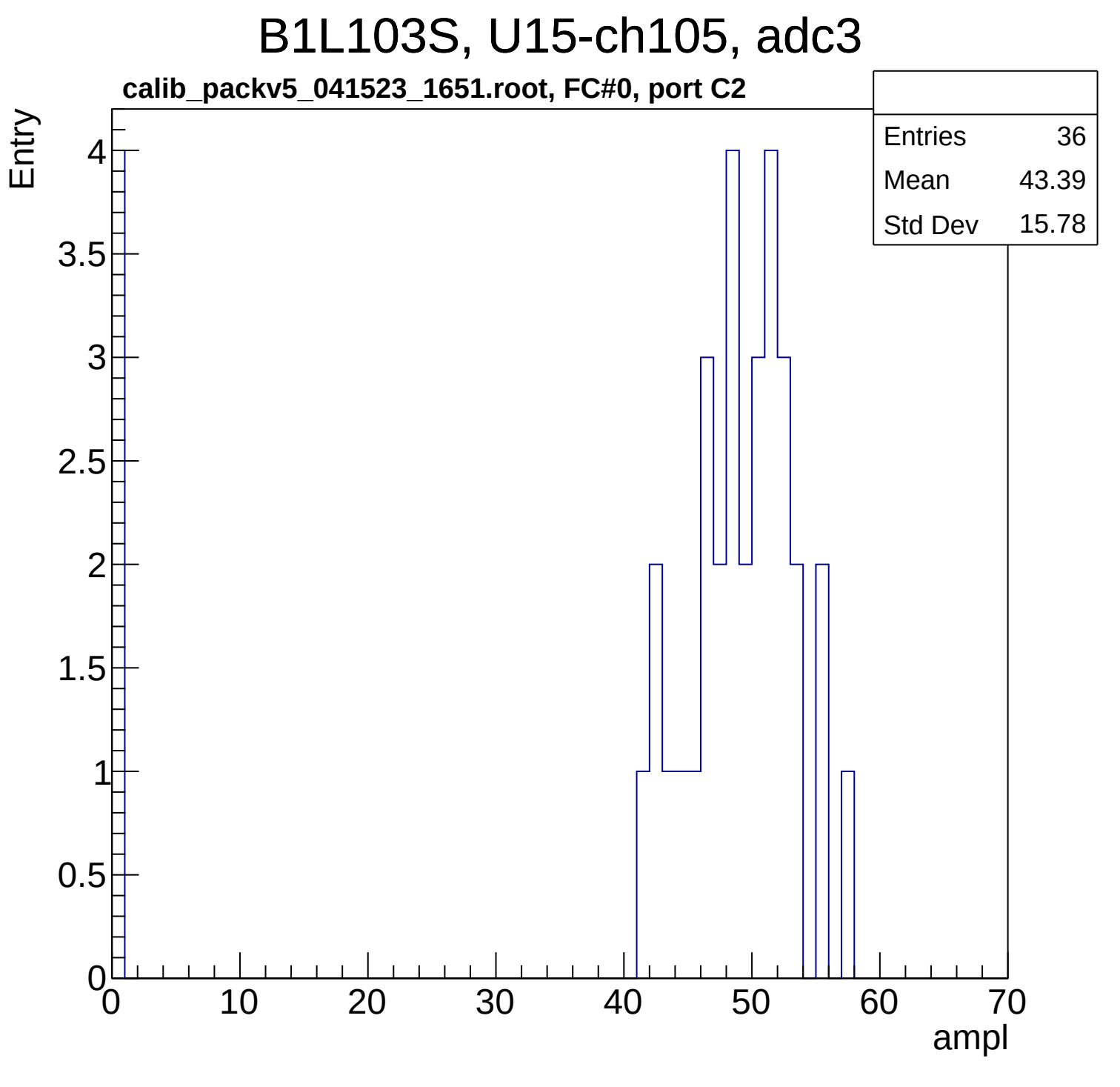
40
50
60
70


B1L103S, U15-ch105, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 43.39
Std Dev 15.78
Entry
ampl
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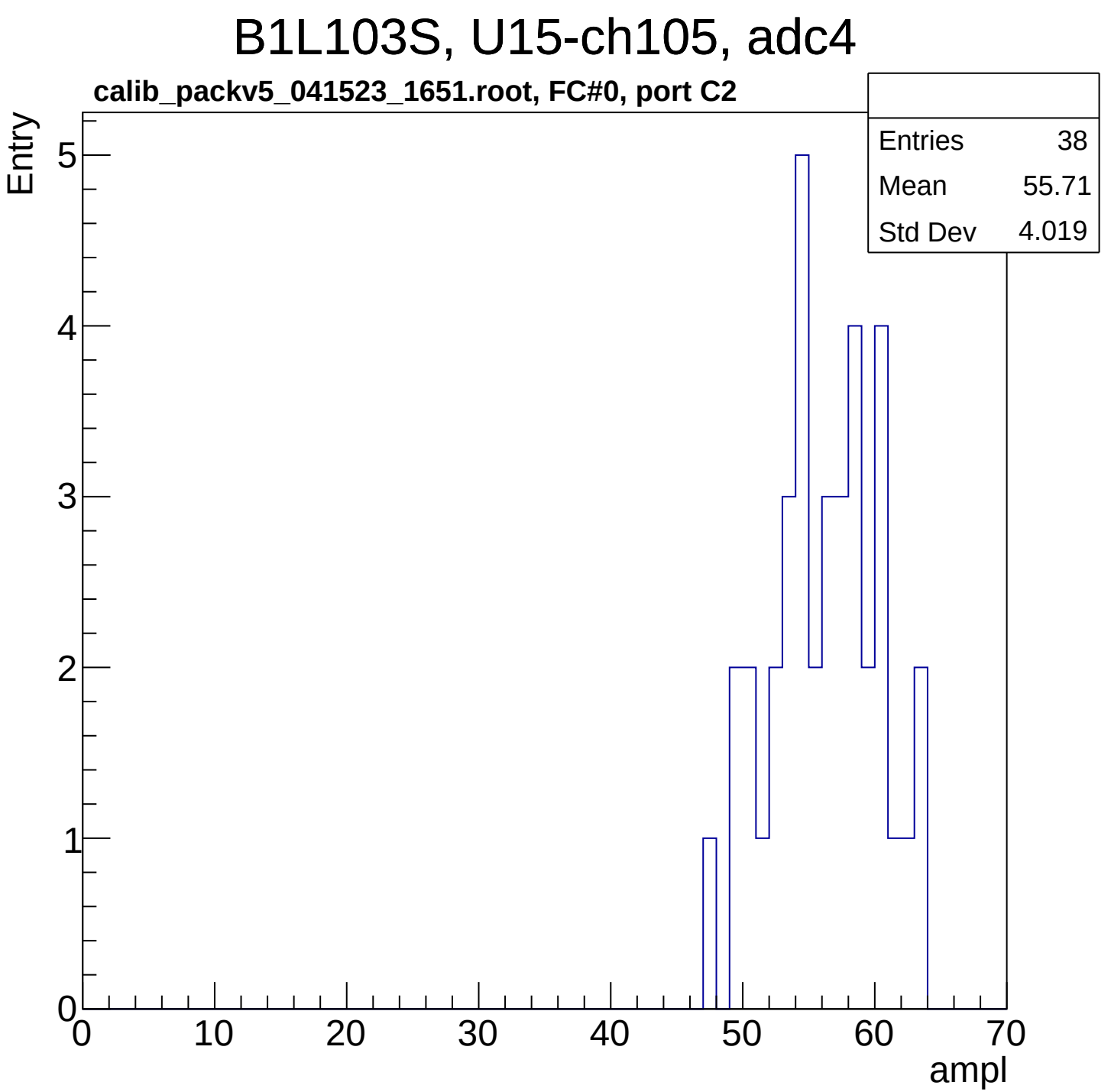
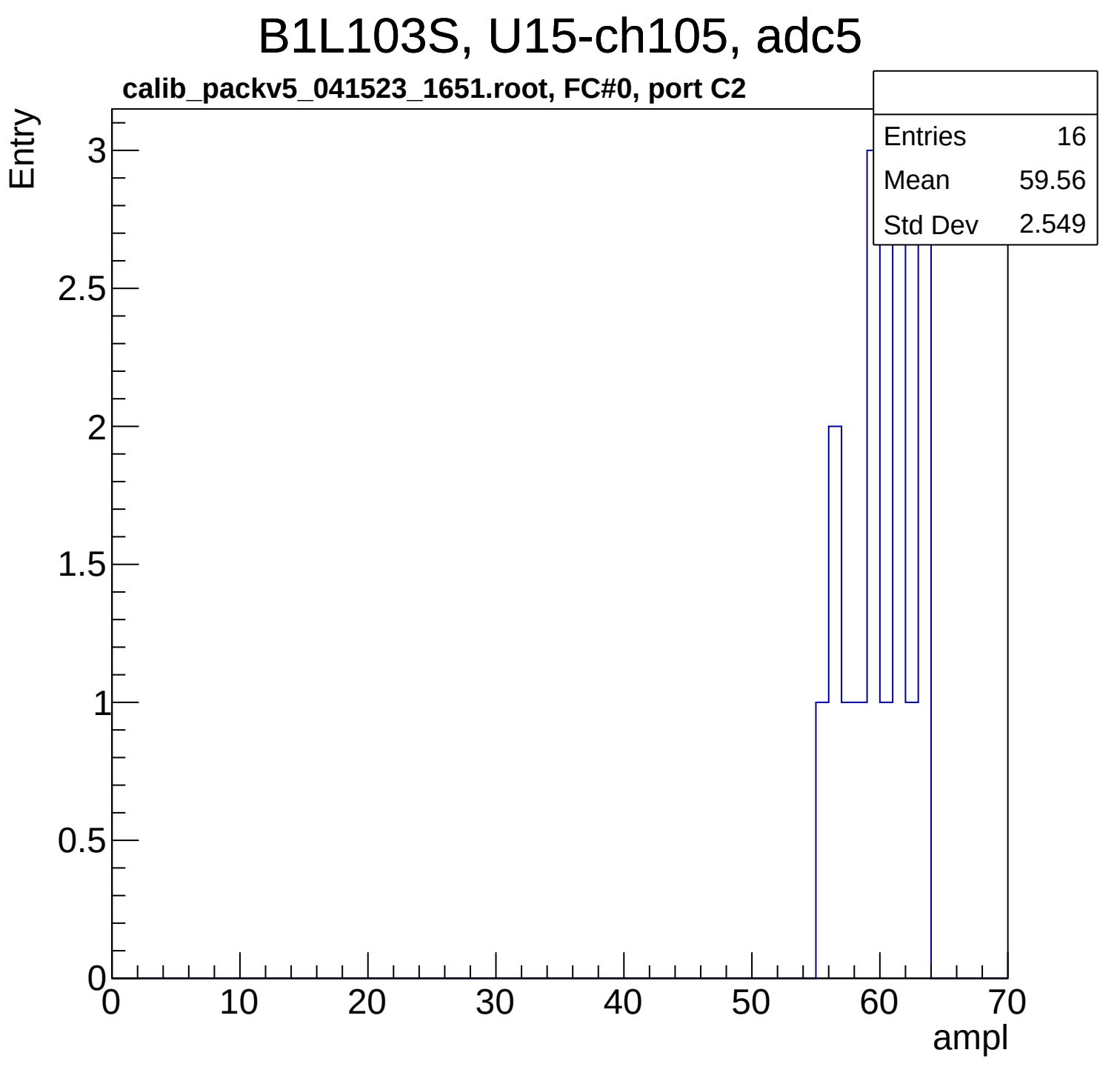
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch105, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 55.71
Std Dev 4.019
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch105, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 59.56
Std Dev 2.549
Entry
ampl
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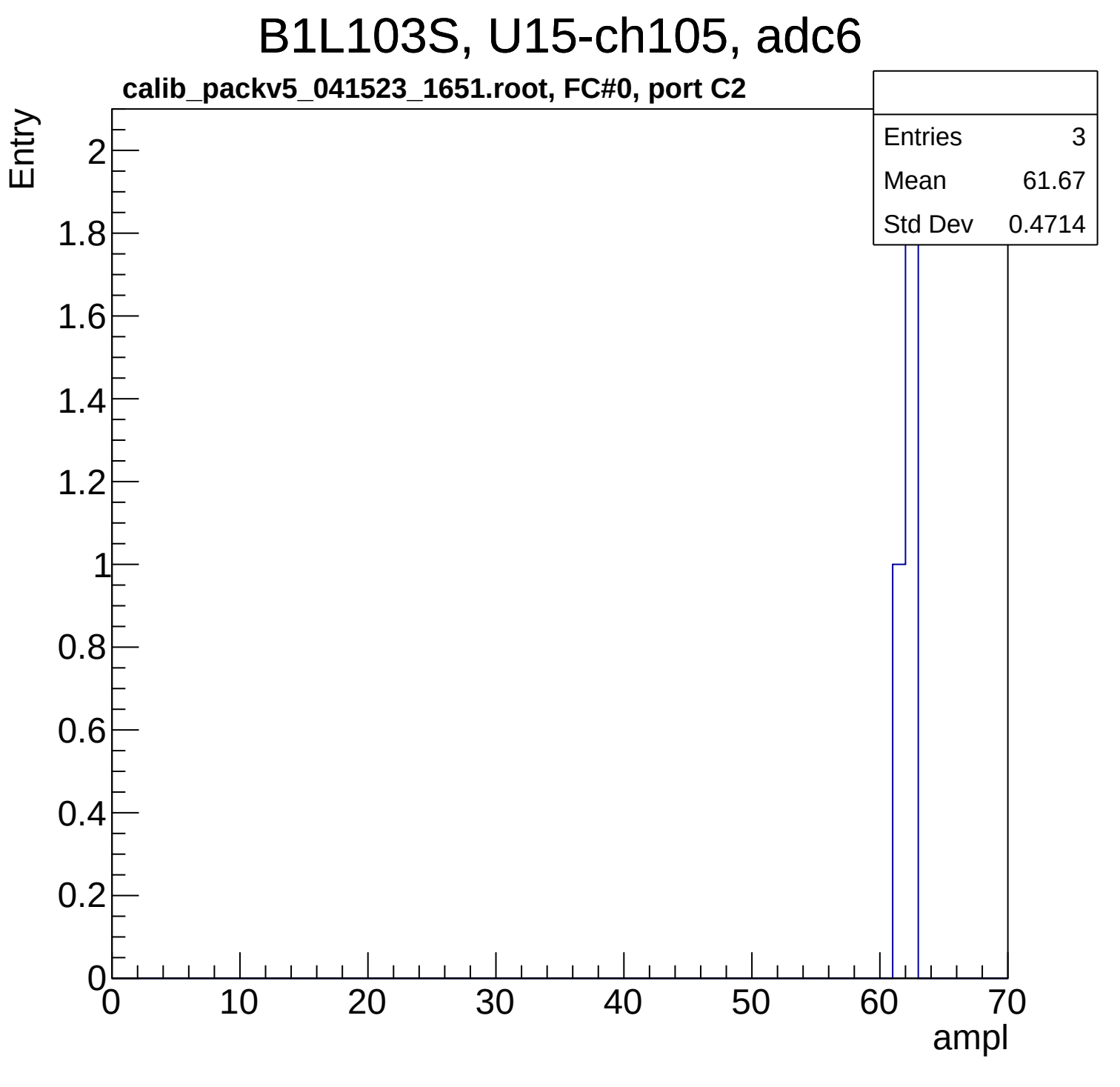
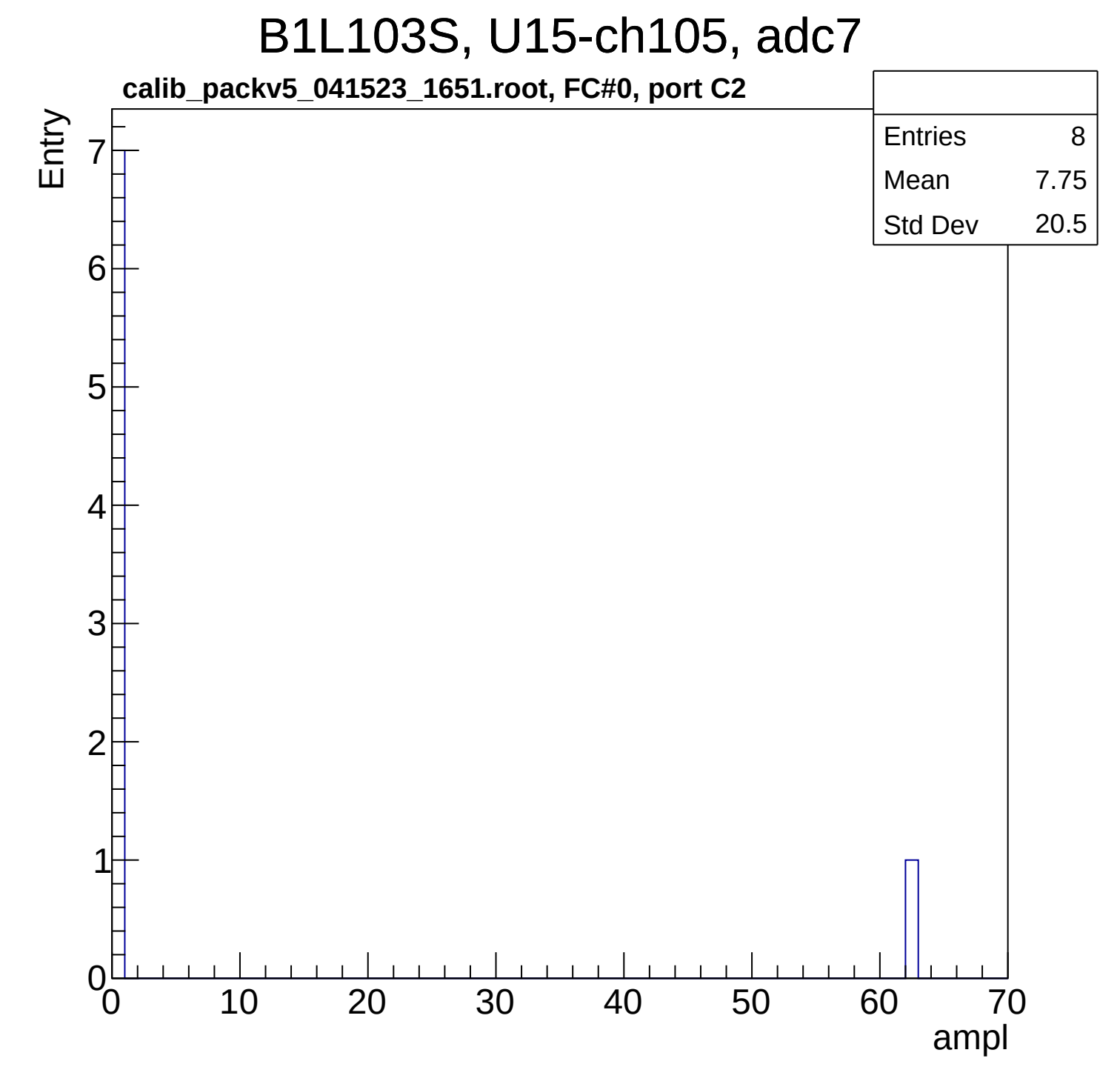
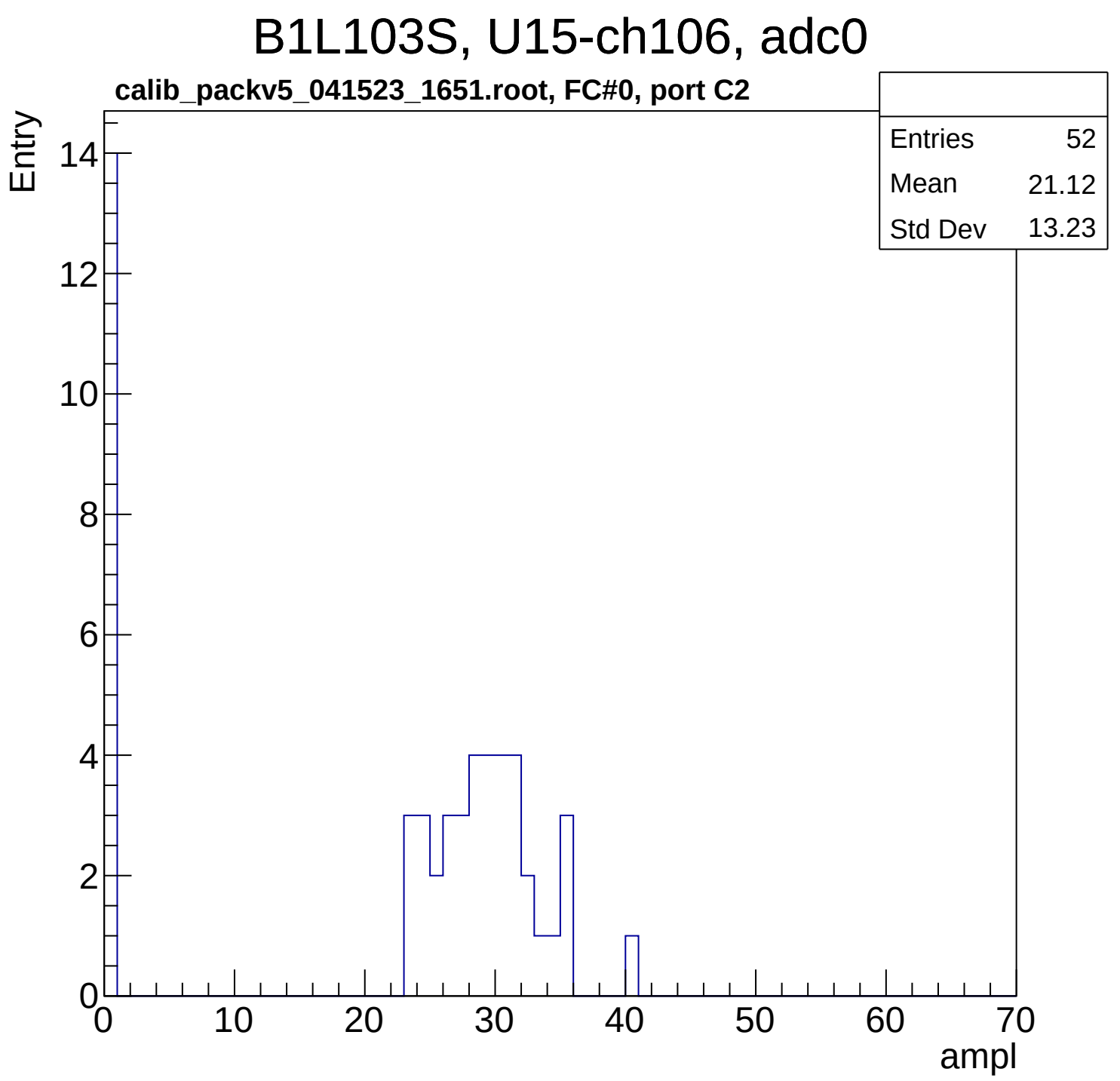
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch105, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 61.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U15-ch105, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 7.75
Std Dev 20.5
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch106, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 21.12
Std Dev 13.23
Entry
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4
6
8
10
12
14
0
10
20
30
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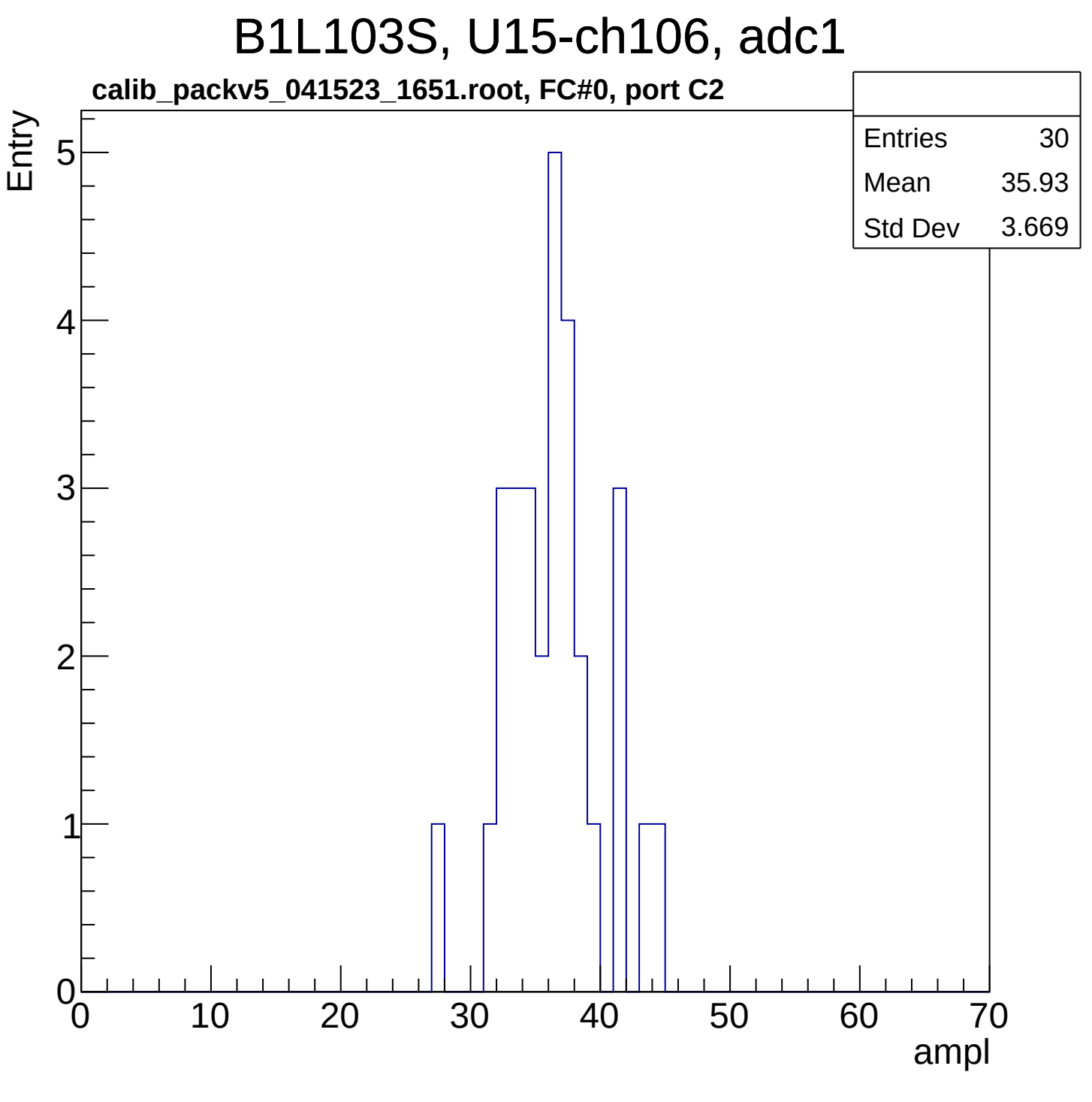
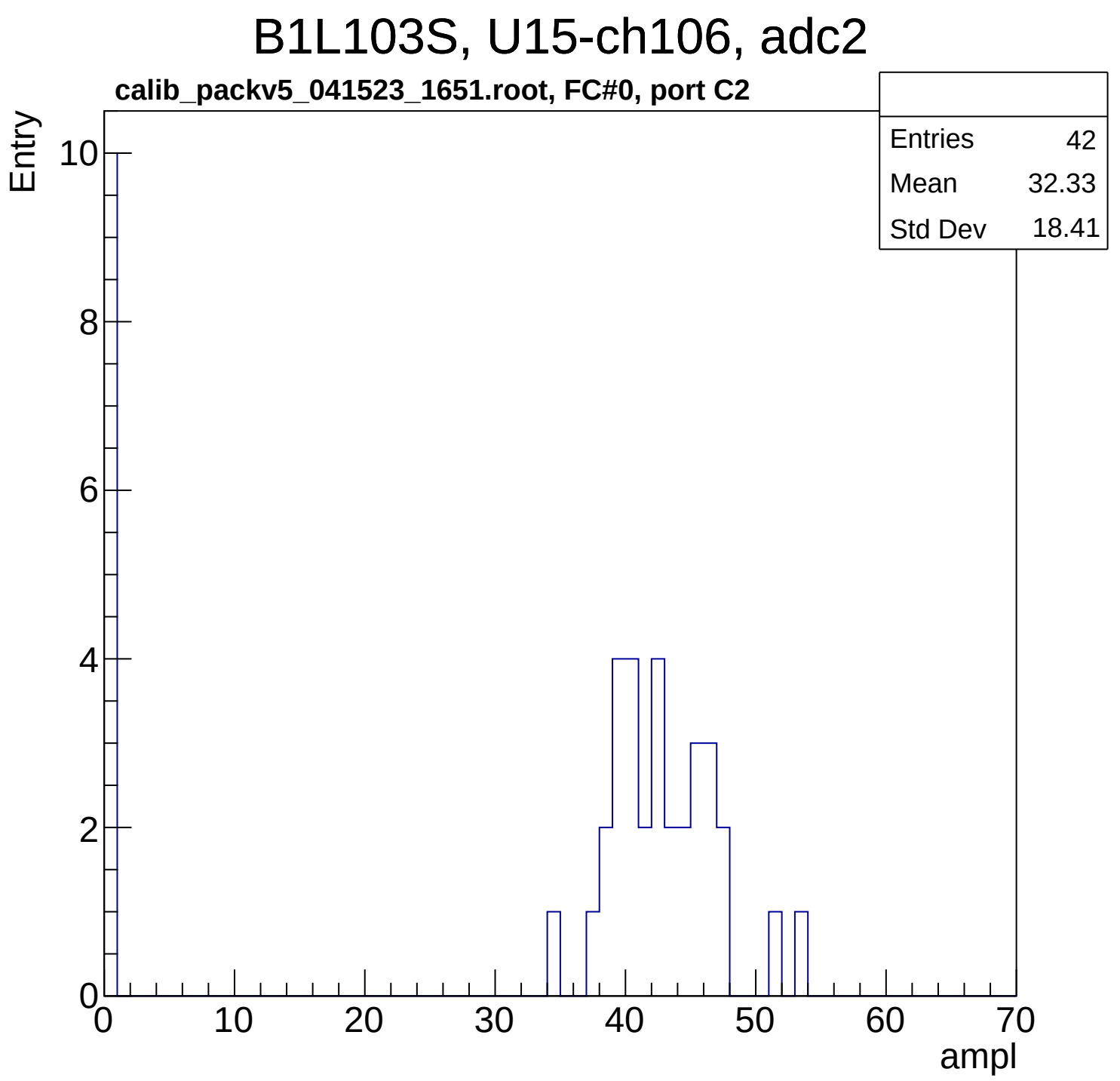
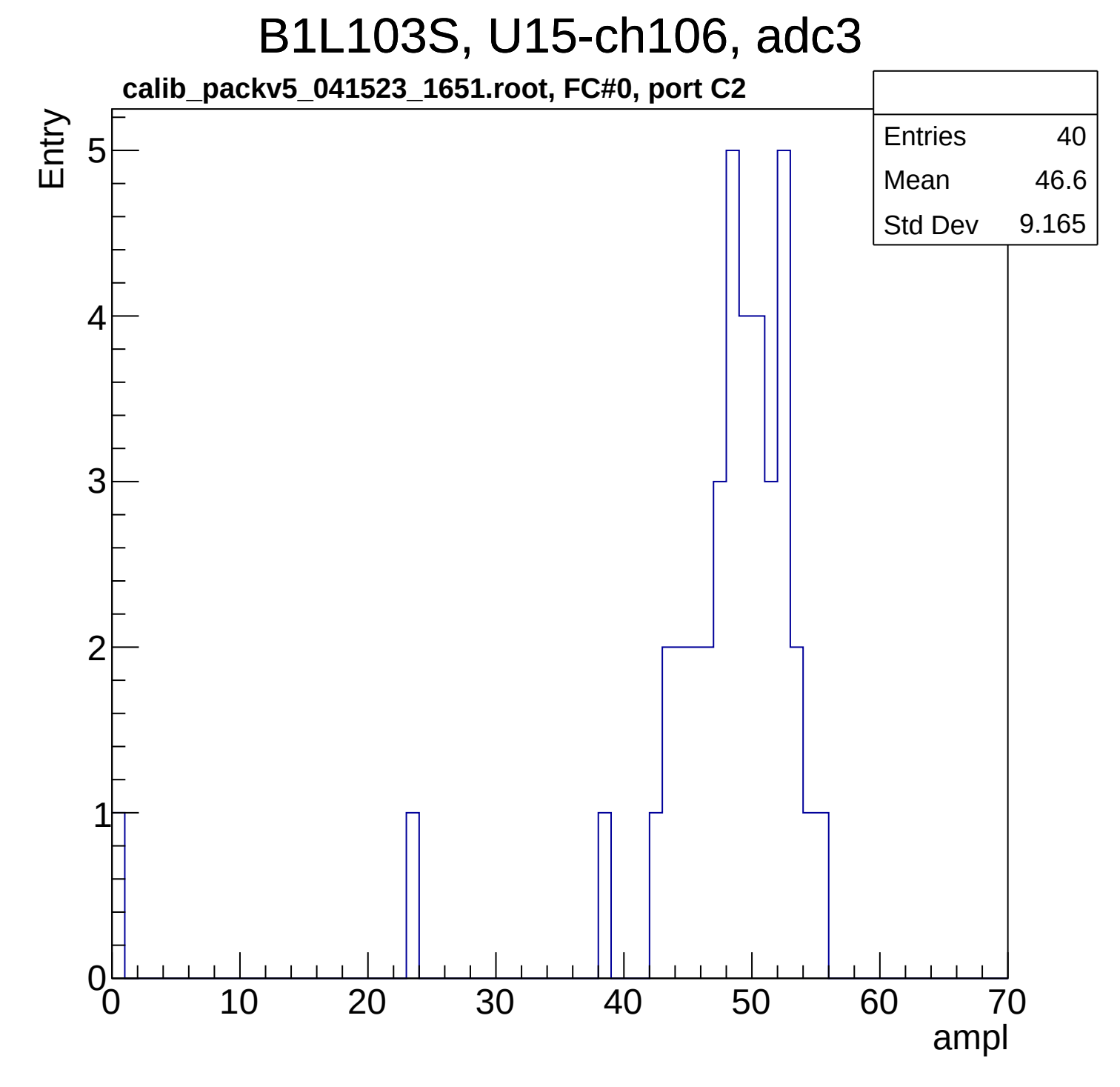
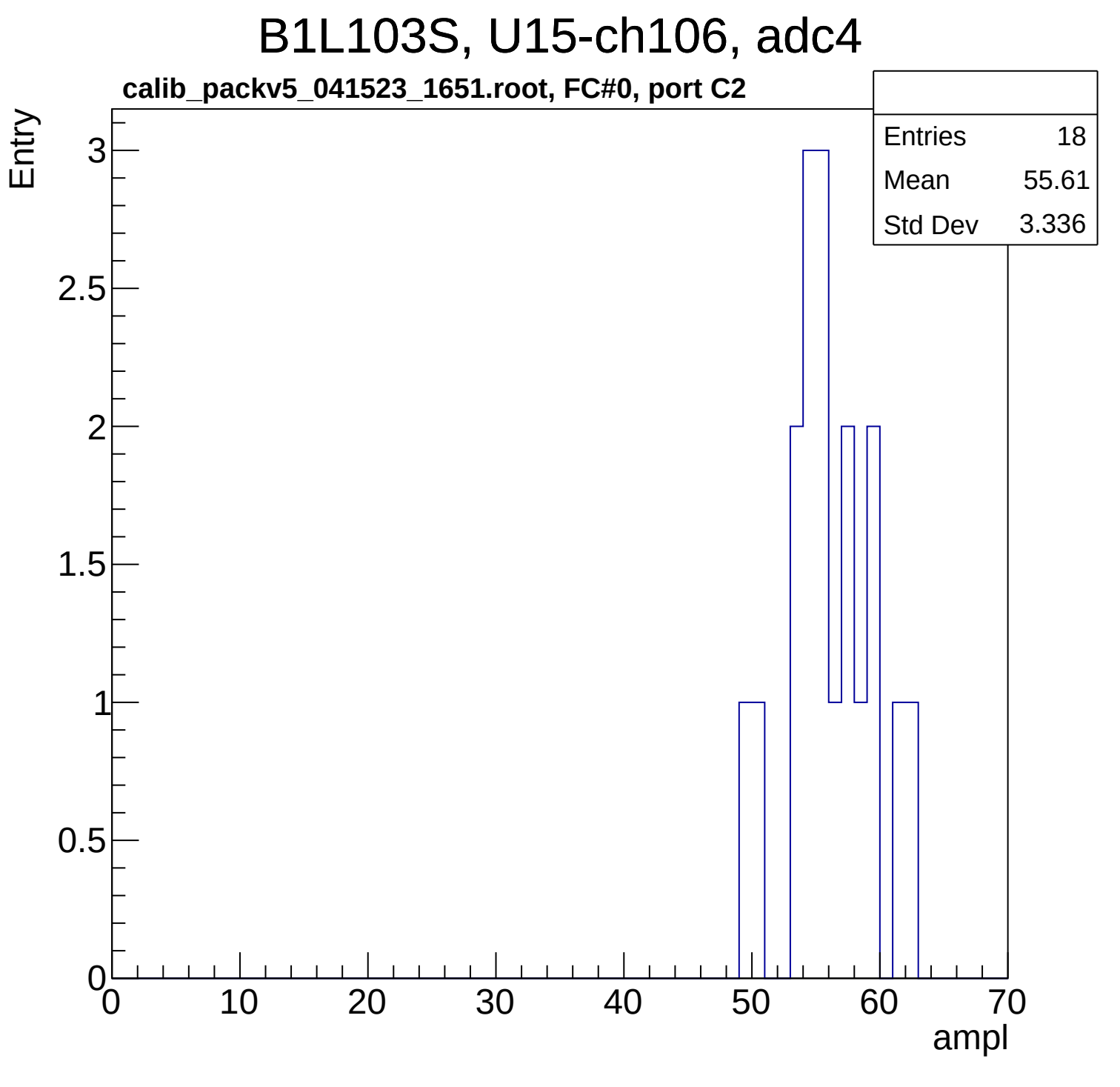
50
60
70
ampl


B1L103S, U15-ch106, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 35.93
Std Dev 3.669
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch106, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 32.33
Std Dev 18.41
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch106, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 46.6
Std Dev 9.165
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch106, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 55.61
Std Dev 3.336
Entry
ampl
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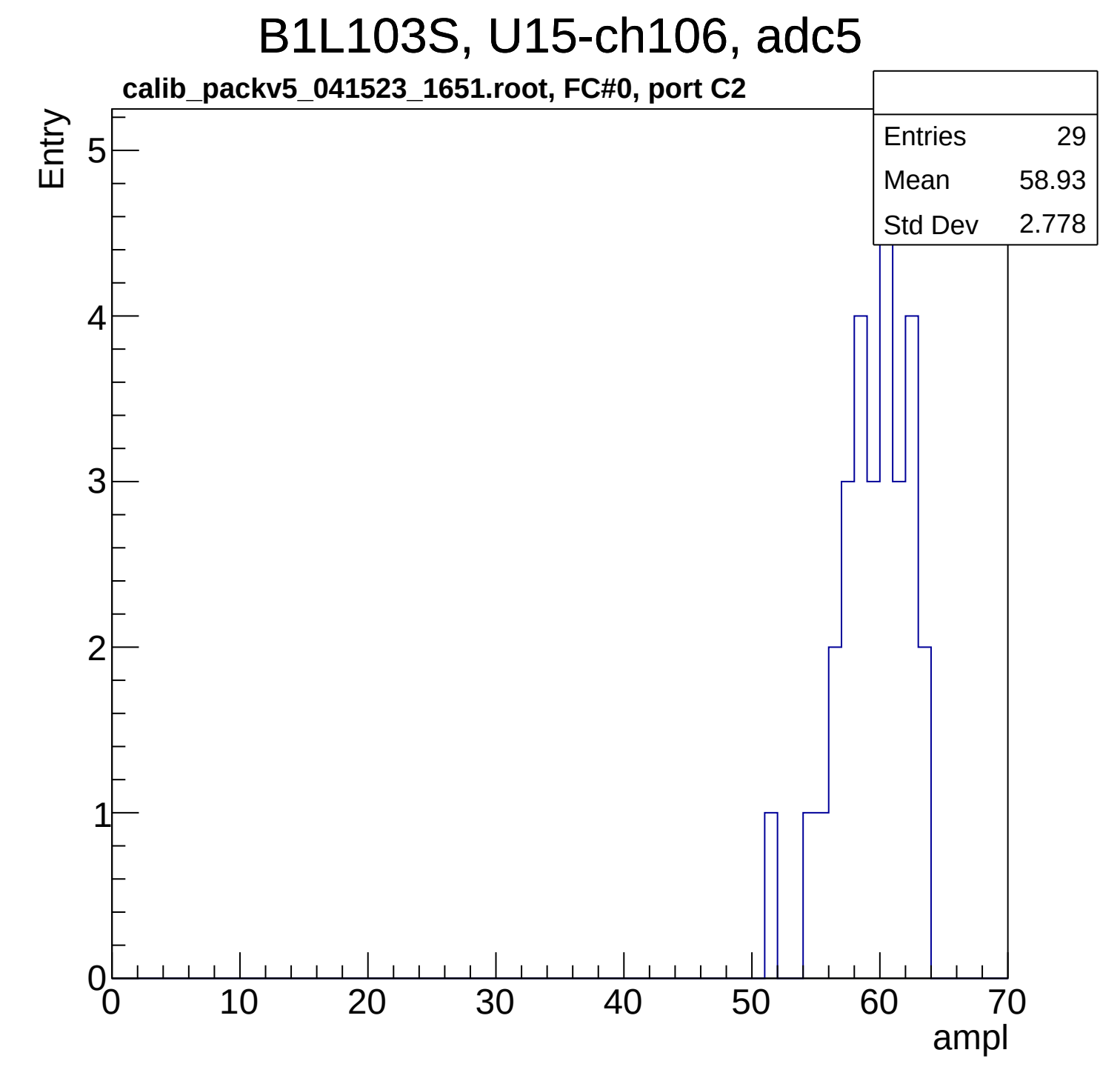
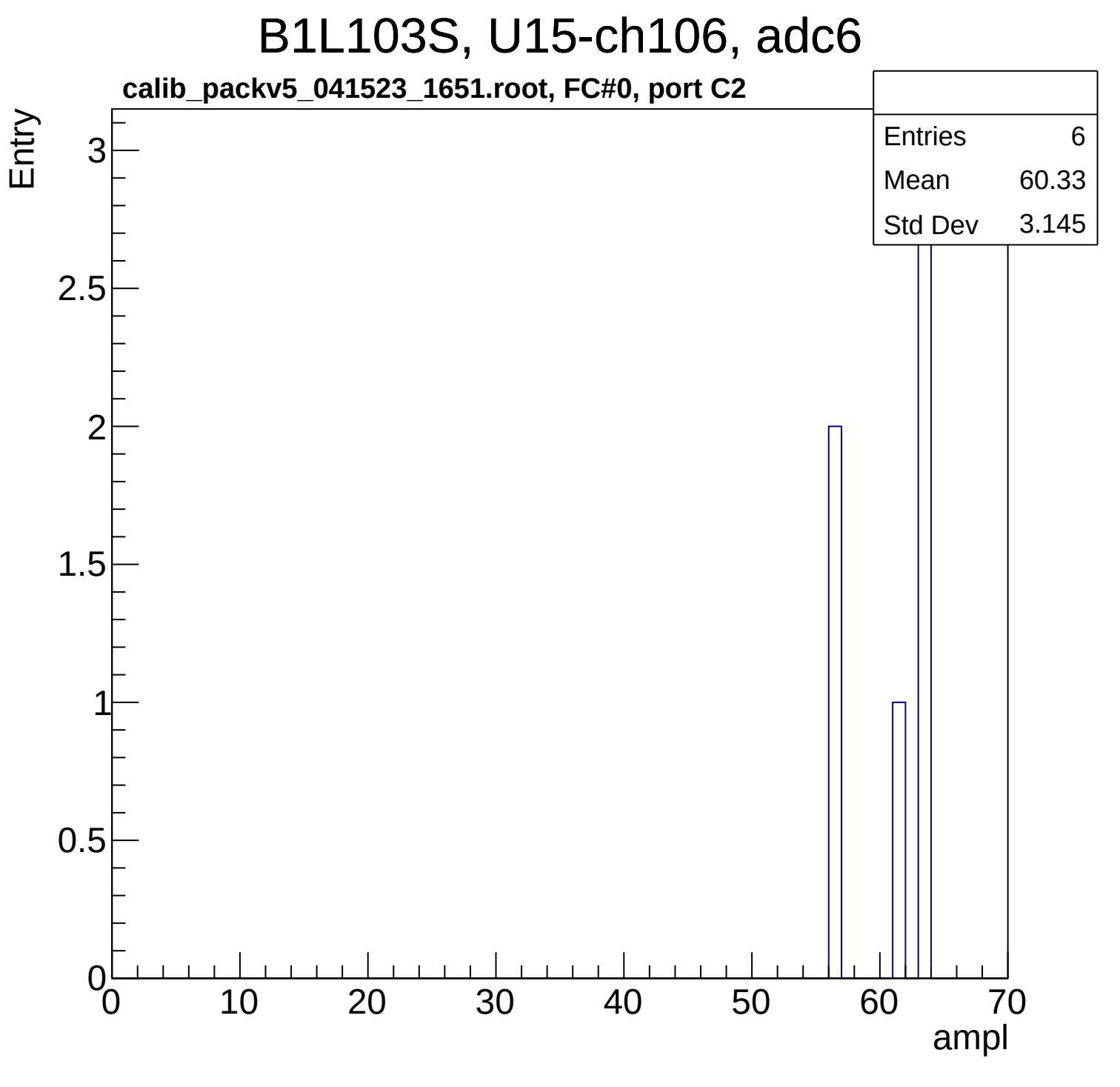
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch106, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 58.93
Std Dev 2.778
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch106, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 60.33
Std Dev 3.145
Entry
ampl
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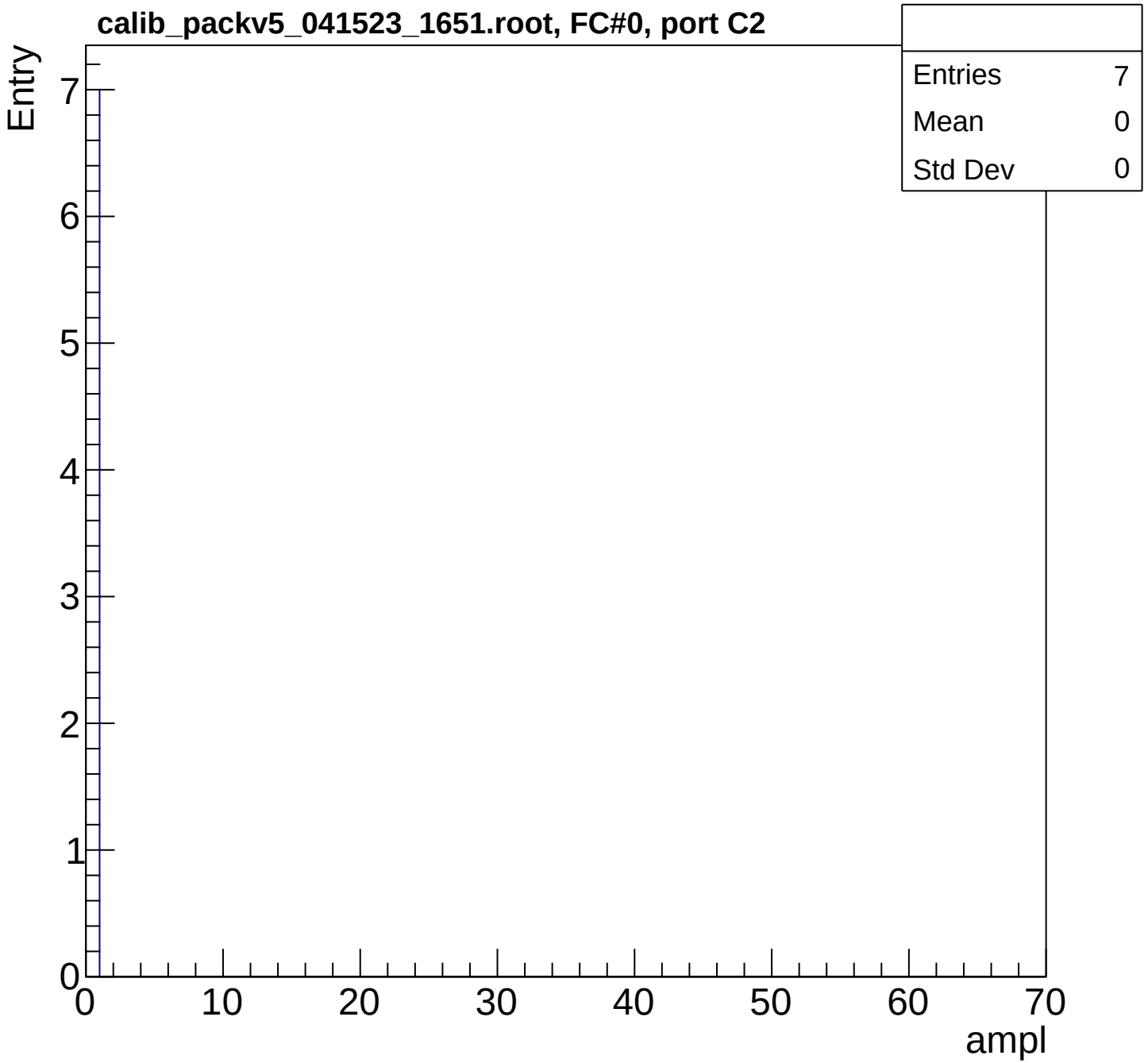
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch106, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 0
Std Dev 0
Entry
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1
2
3
4
5
6
7
0
10
20
30
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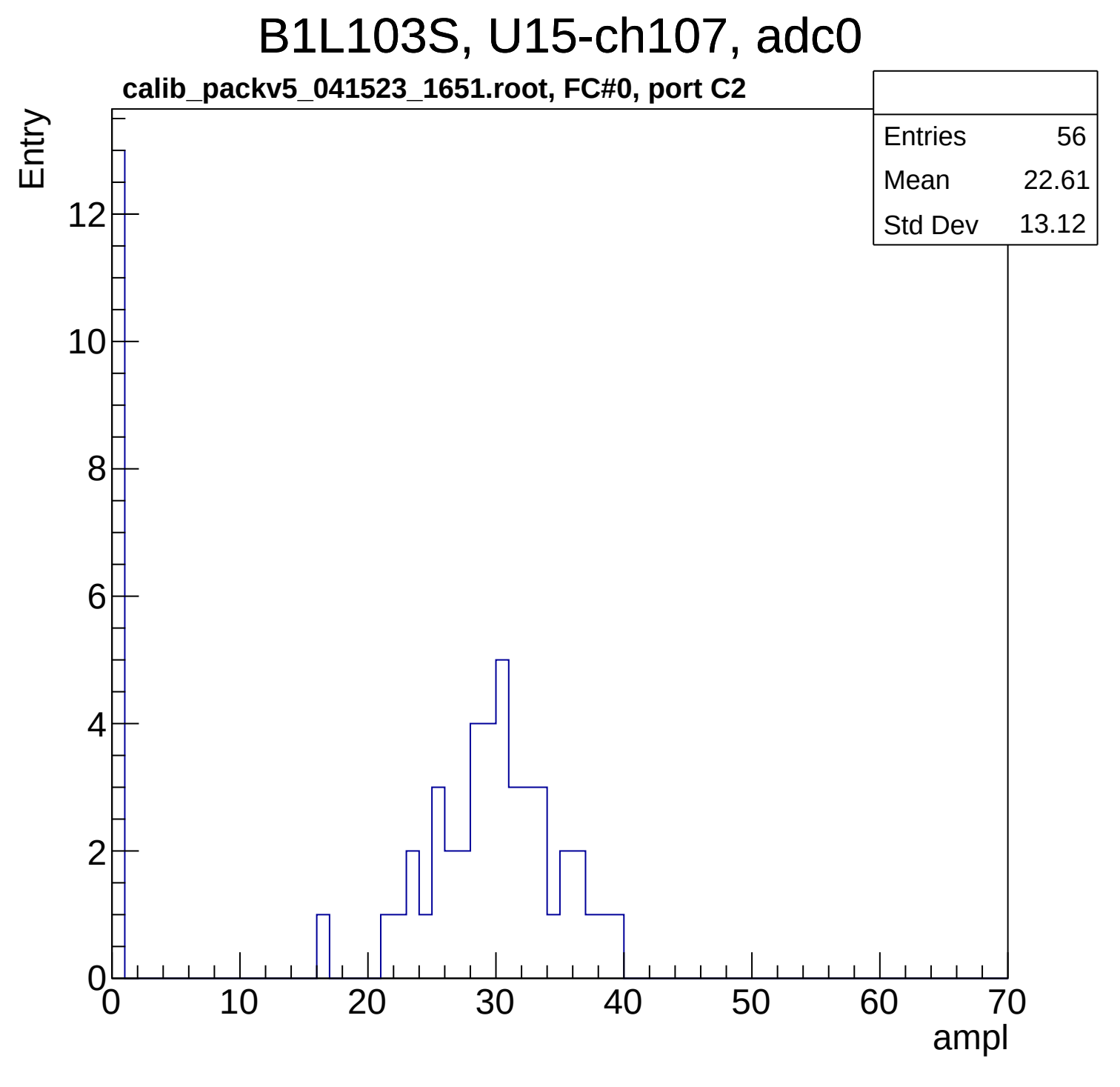
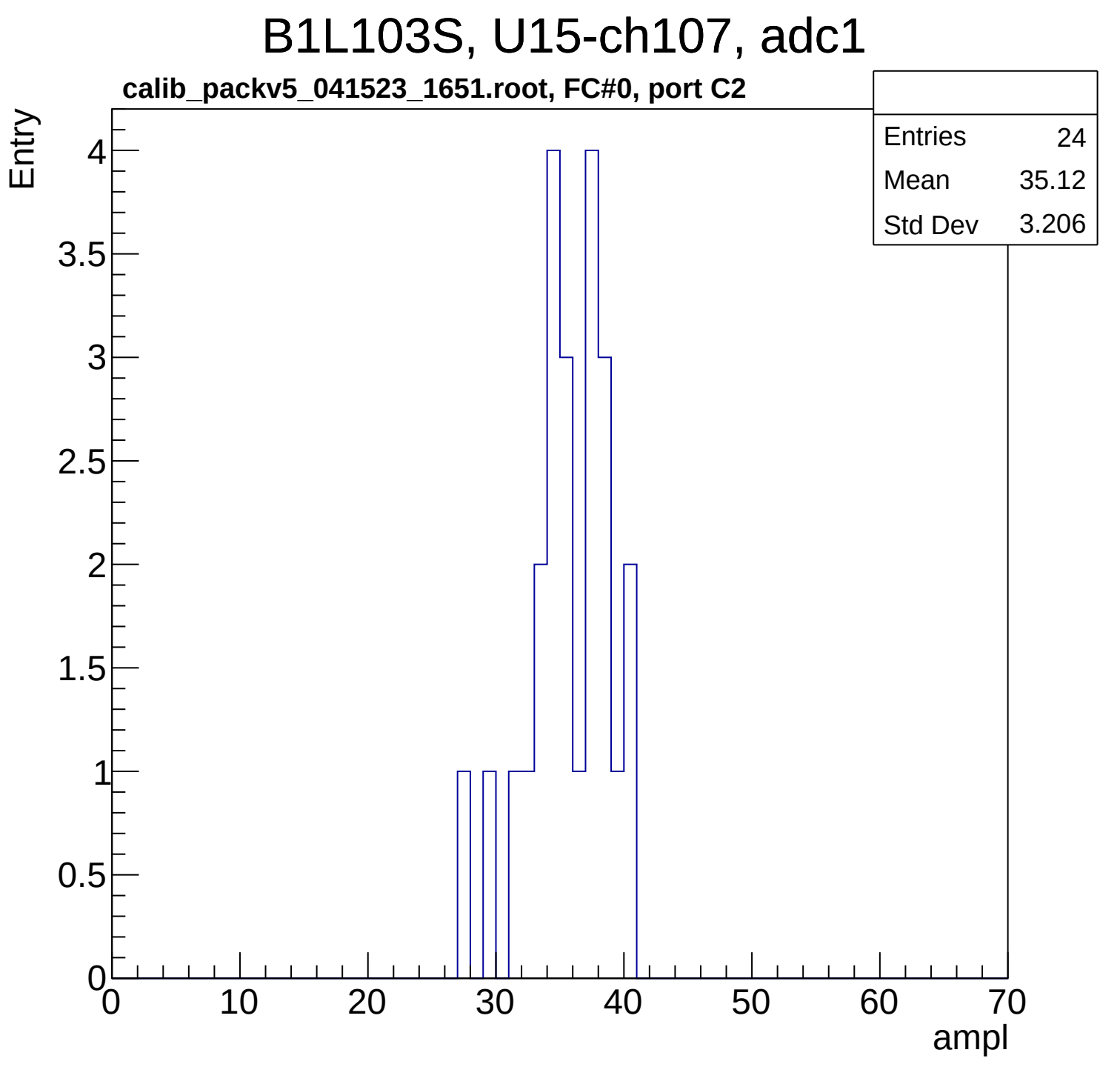
50
60
70
ampl


B1L103S, U15-ch107, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 22.61
Std Dev 13.12
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch107, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 35.12
Std Dev 3.206
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
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0
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20
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60
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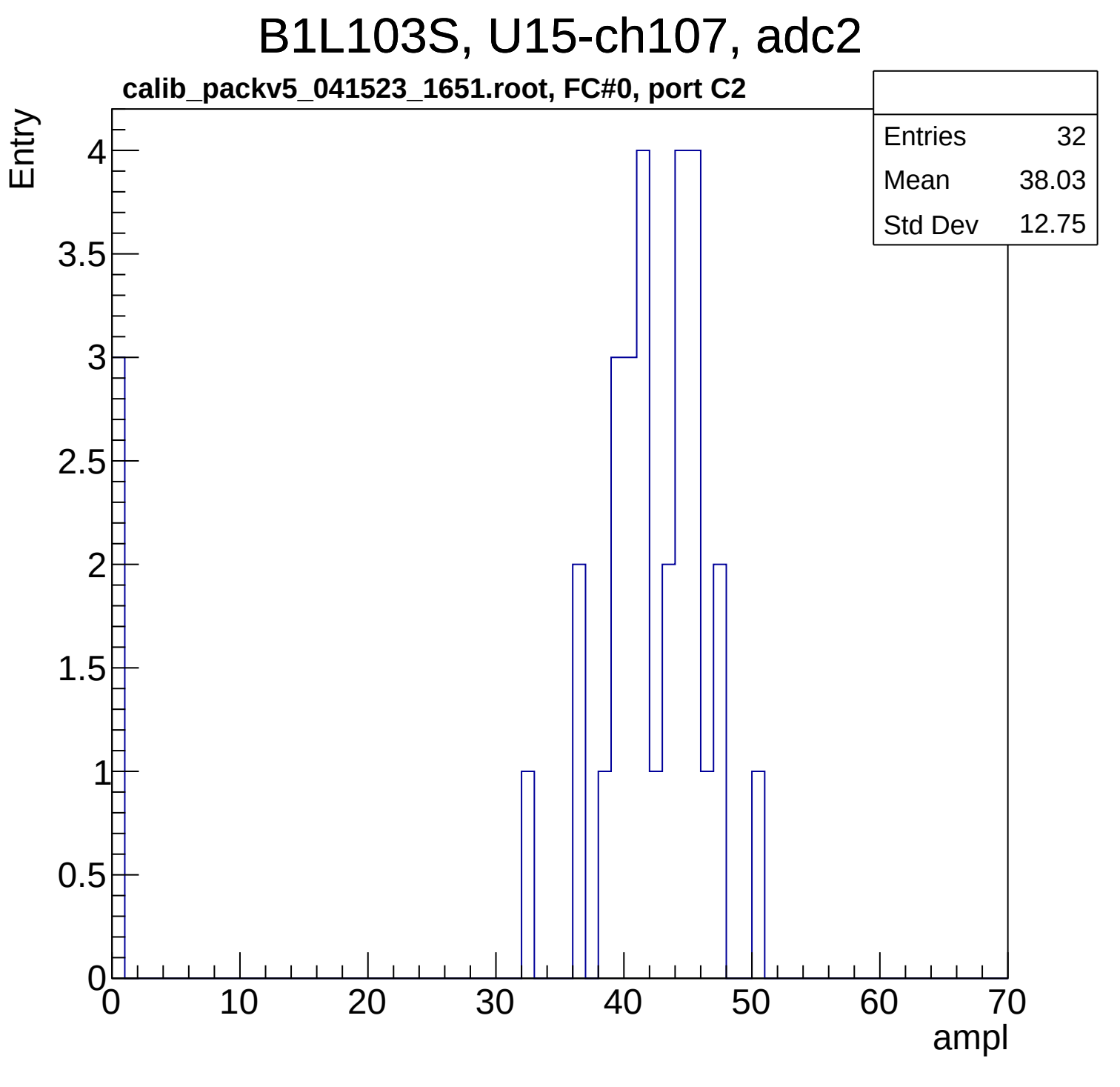
B1L103S, U15-ch107, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 38.03
Std Dev 12.75
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
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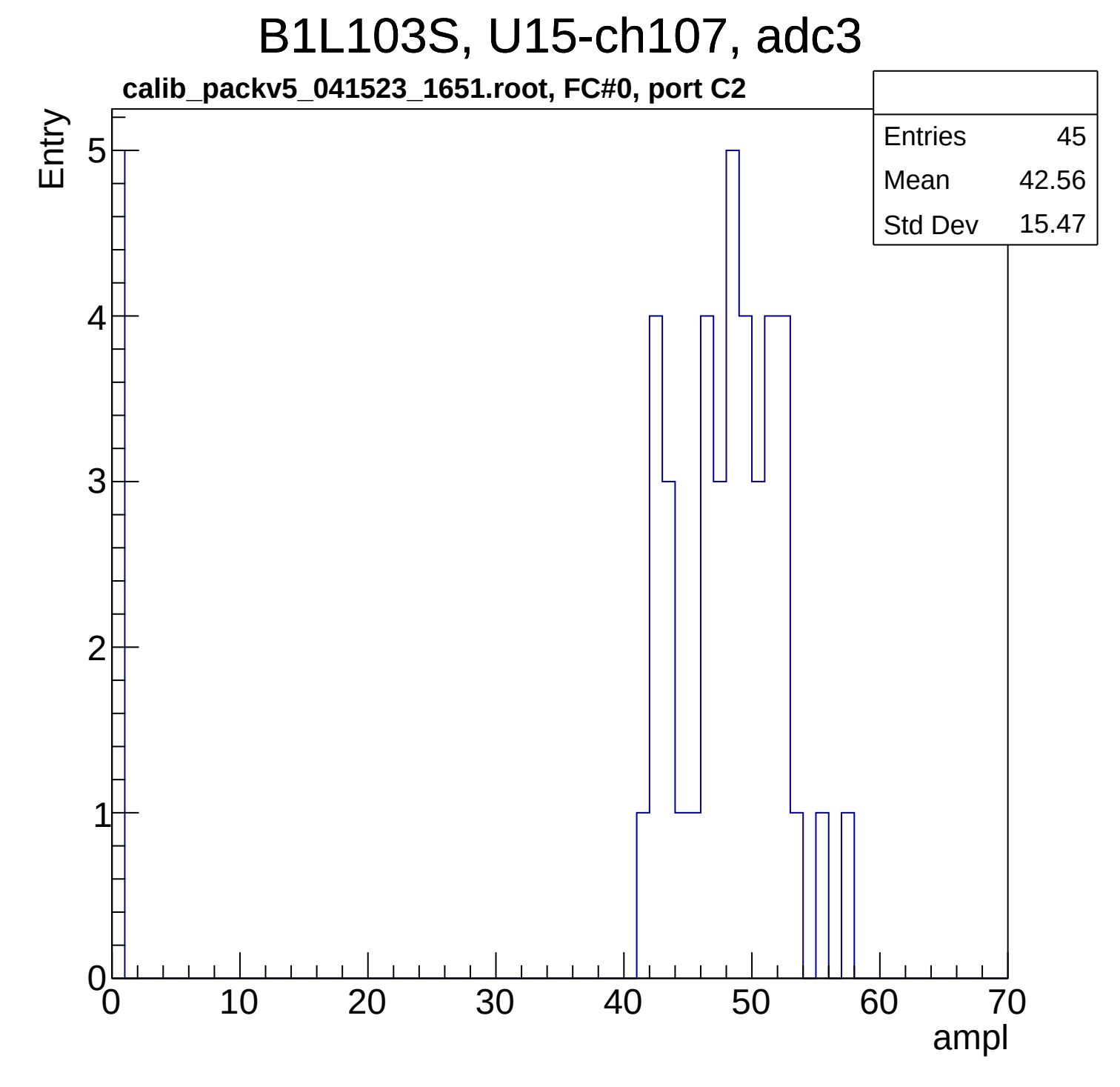
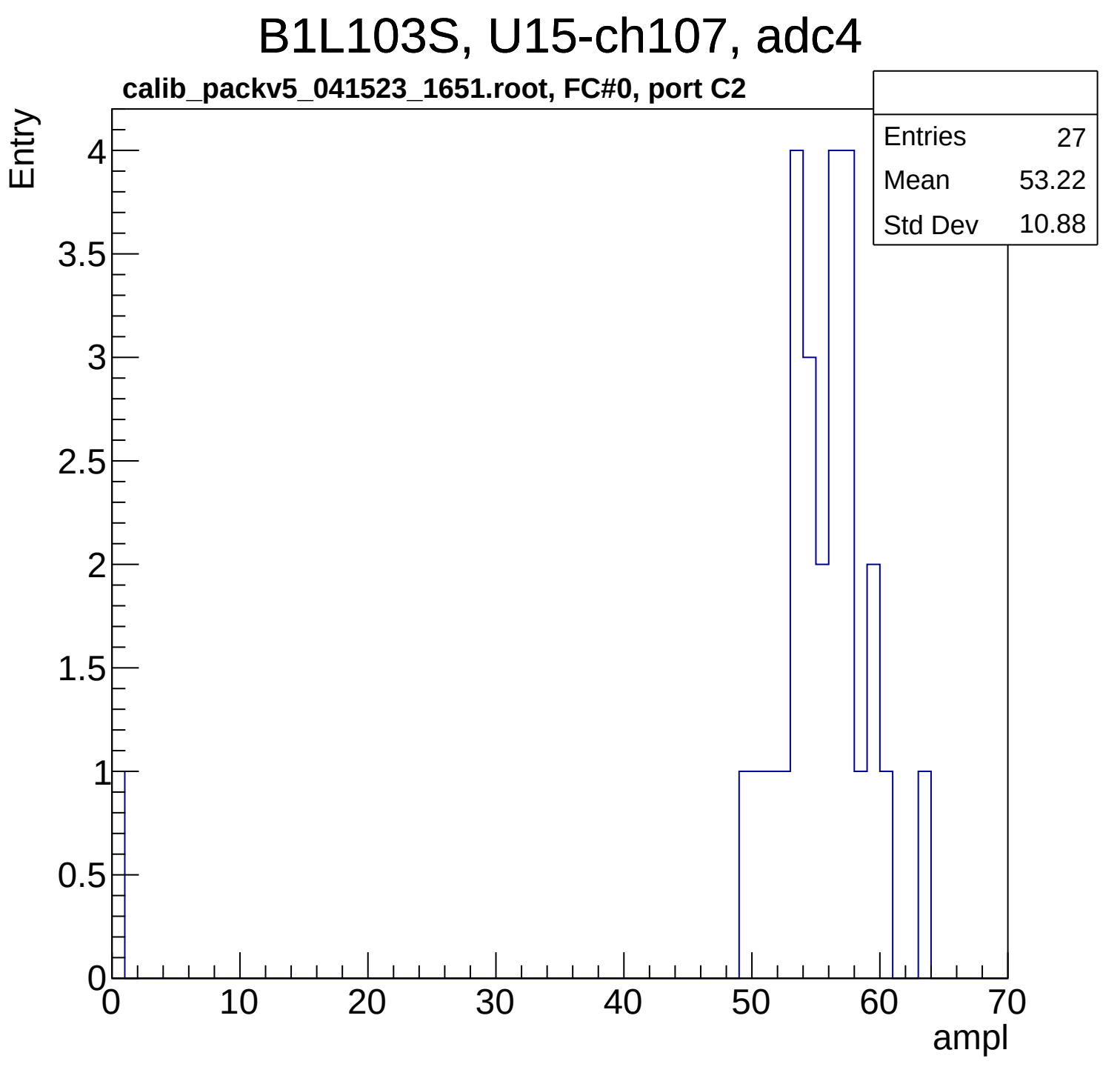
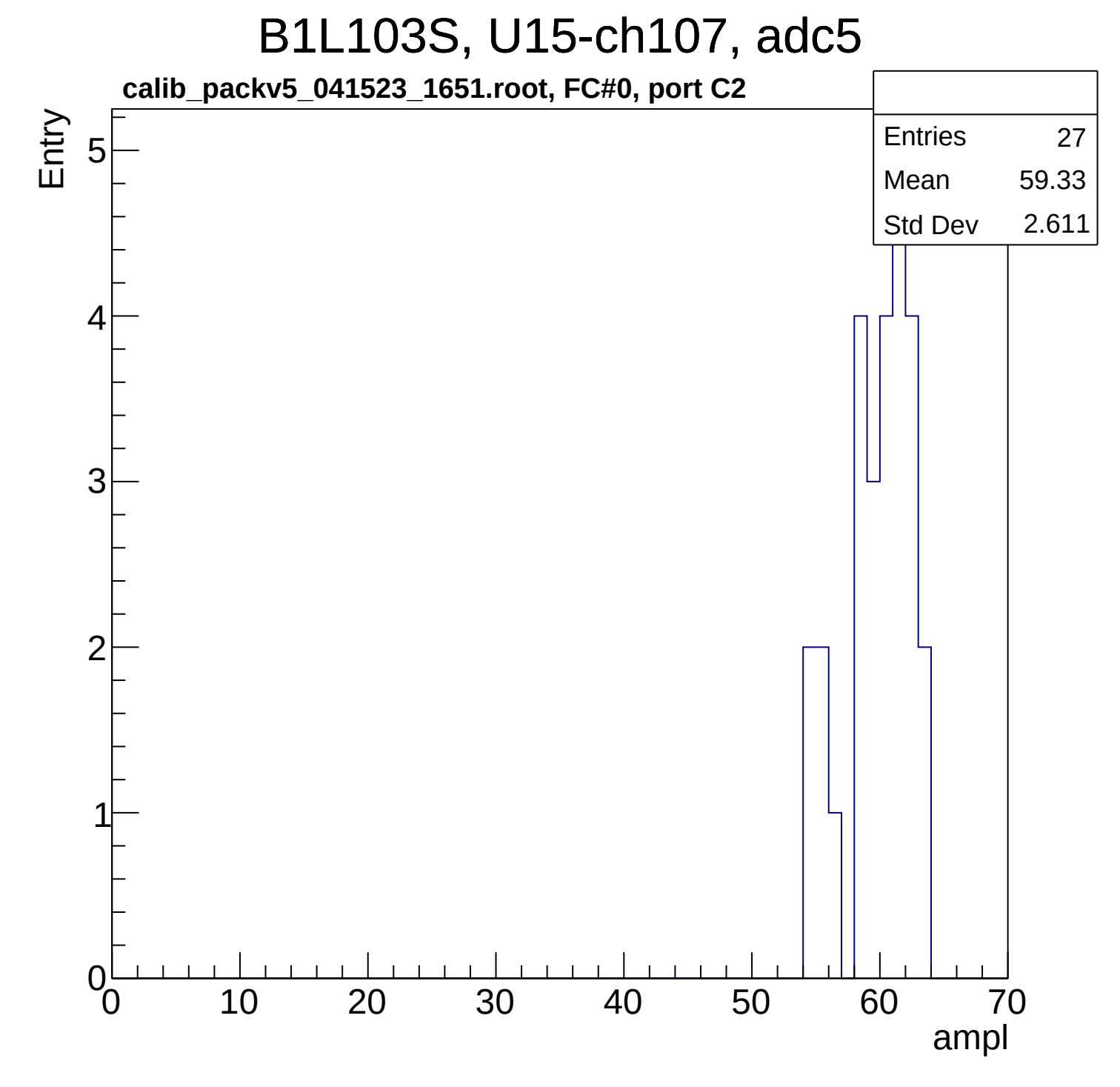
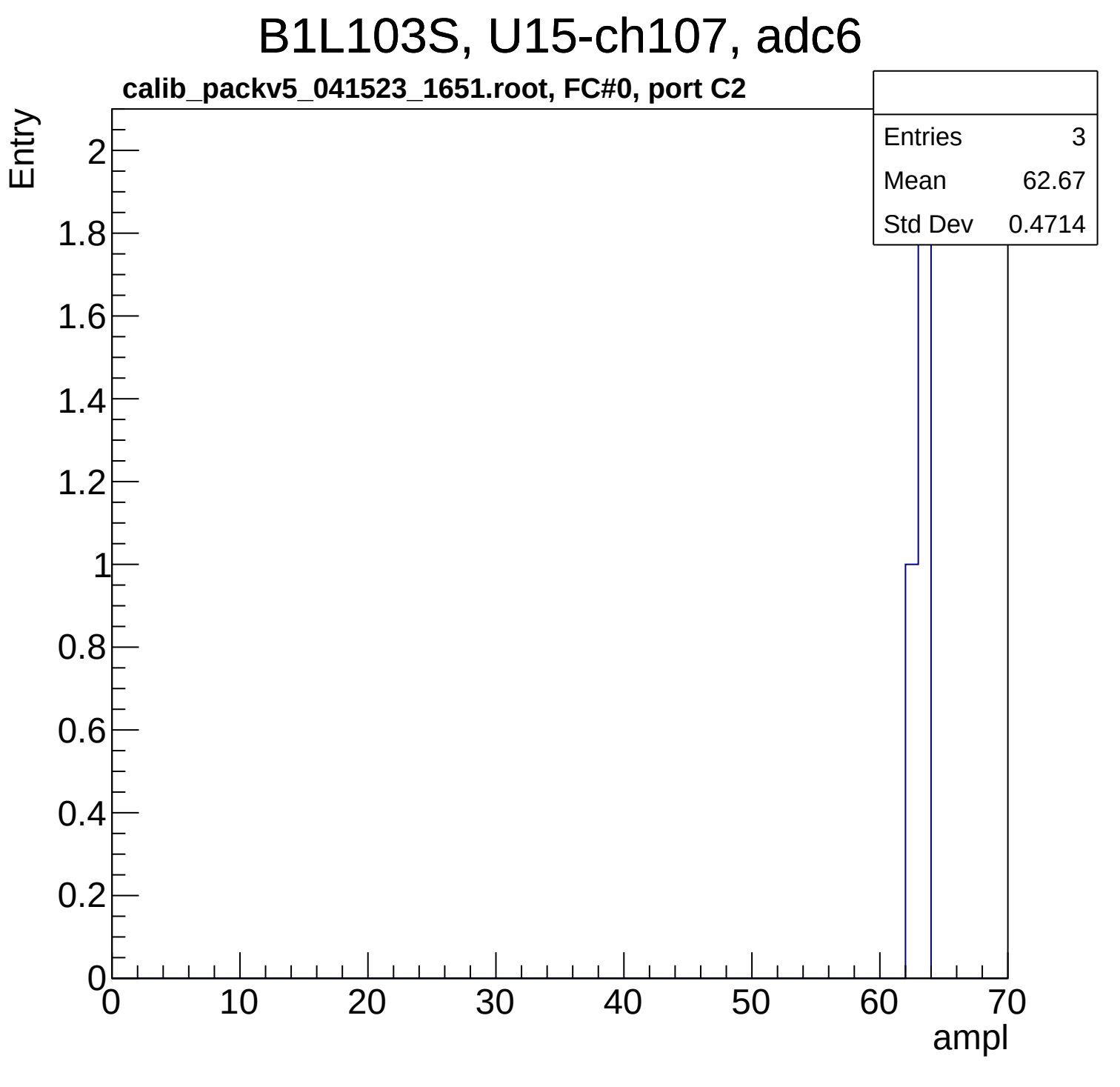
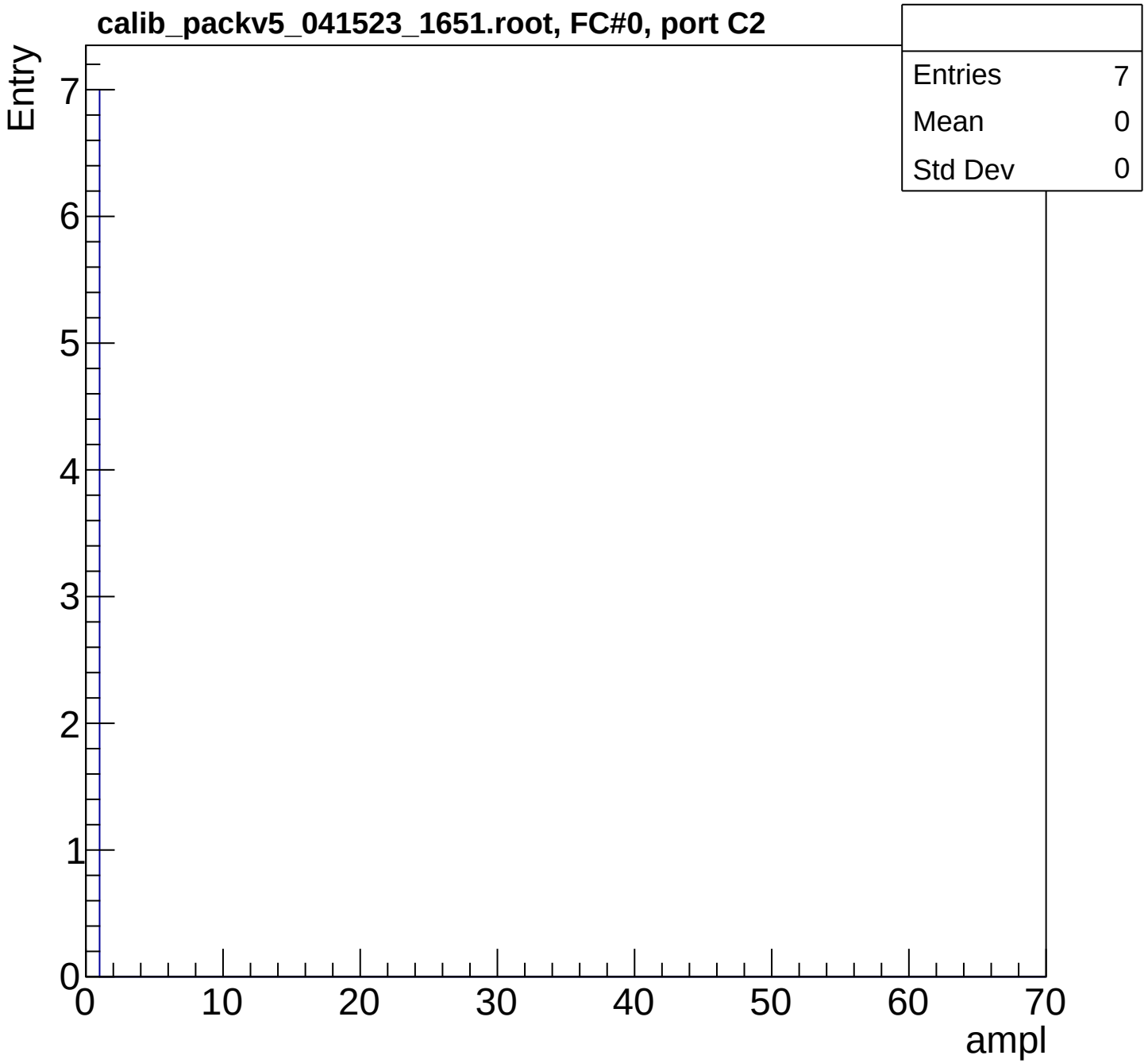
60
70

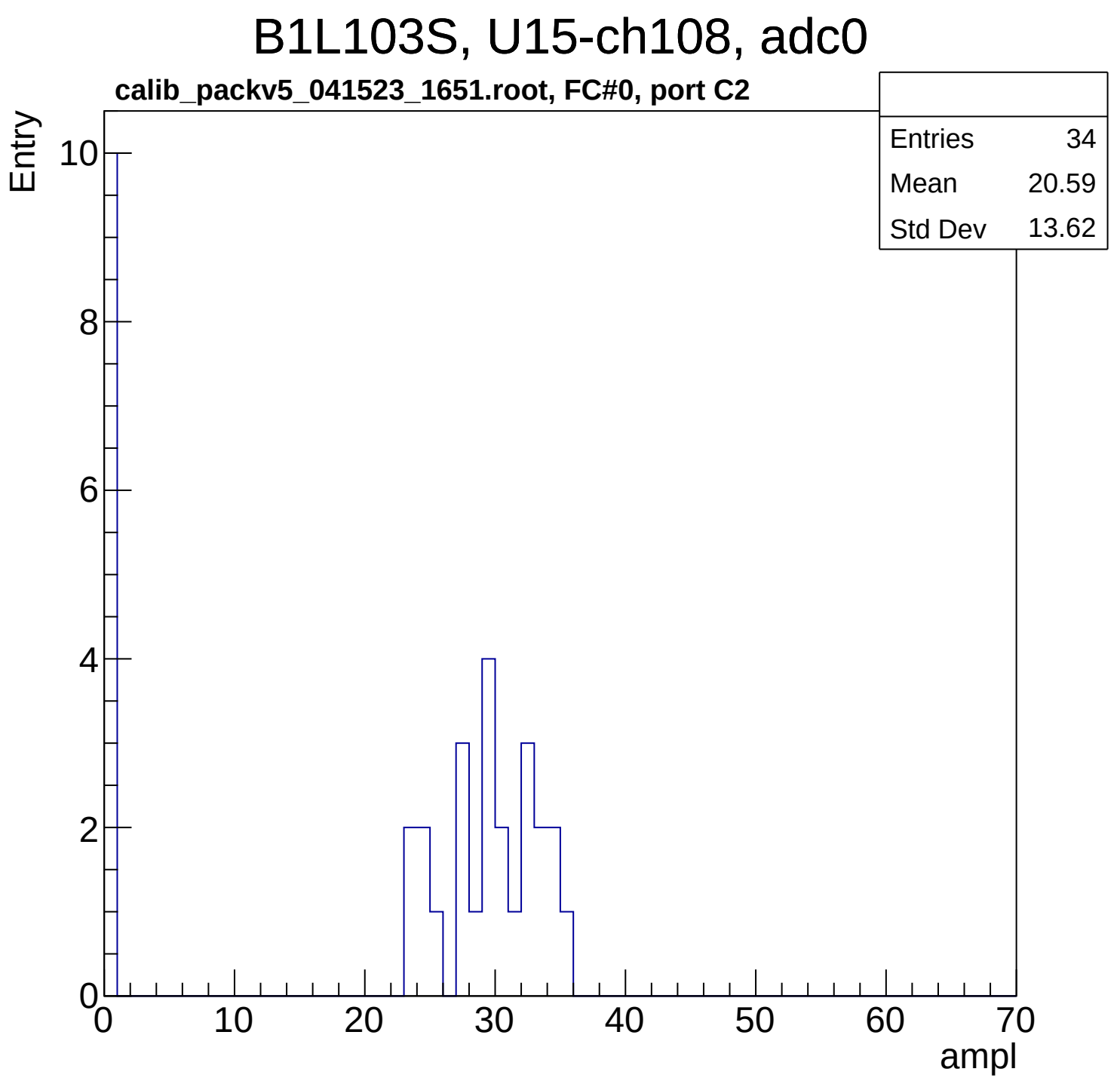

B1L103S, U15-ch107, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 42.56
Std Dev 15.47
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

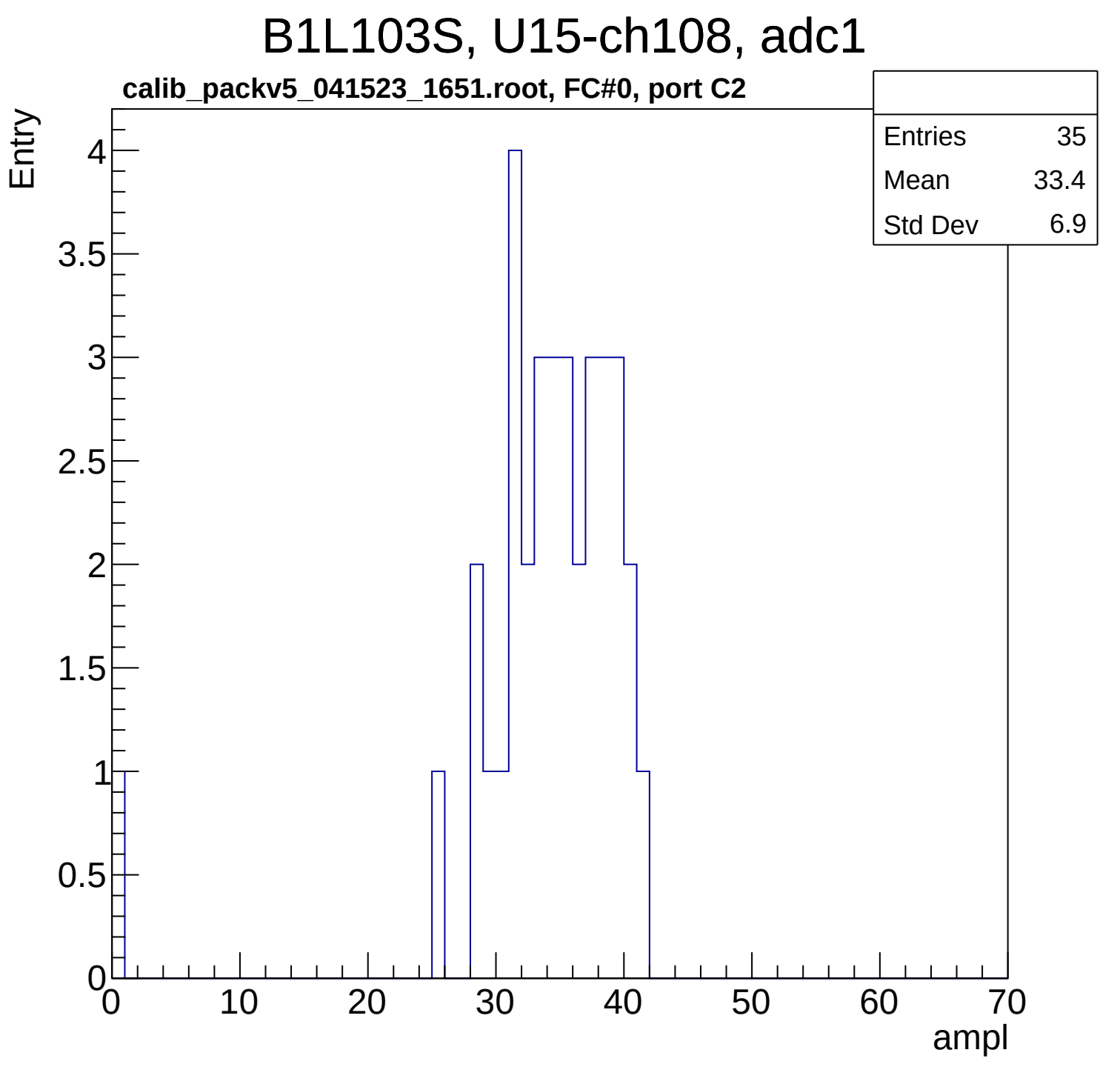

B1L103S, U15-ch107, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 53.22
Std Dev 10.88
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

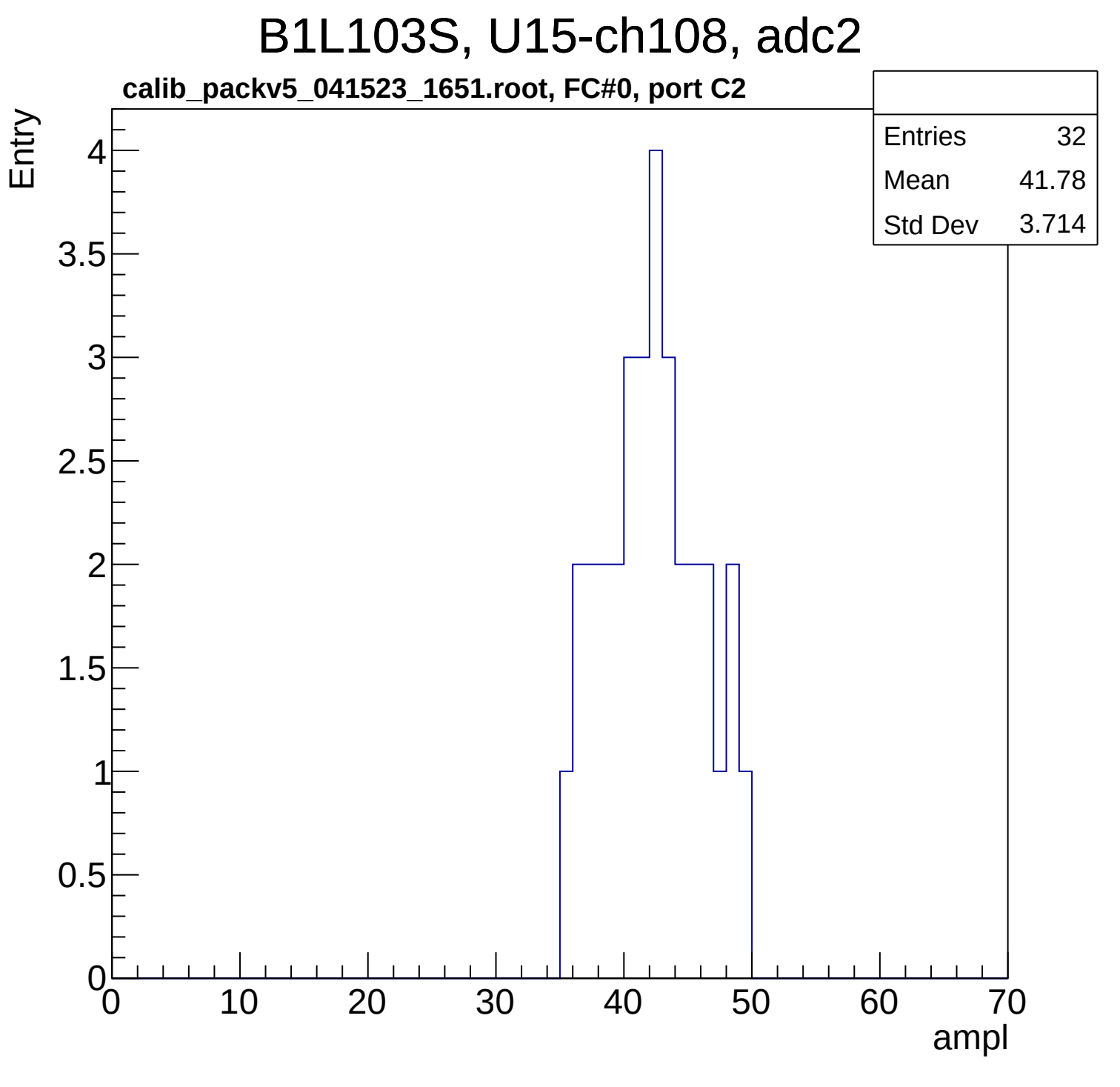

B1L103S, U15-ch107, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 59.33
Std Dev 2.611
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

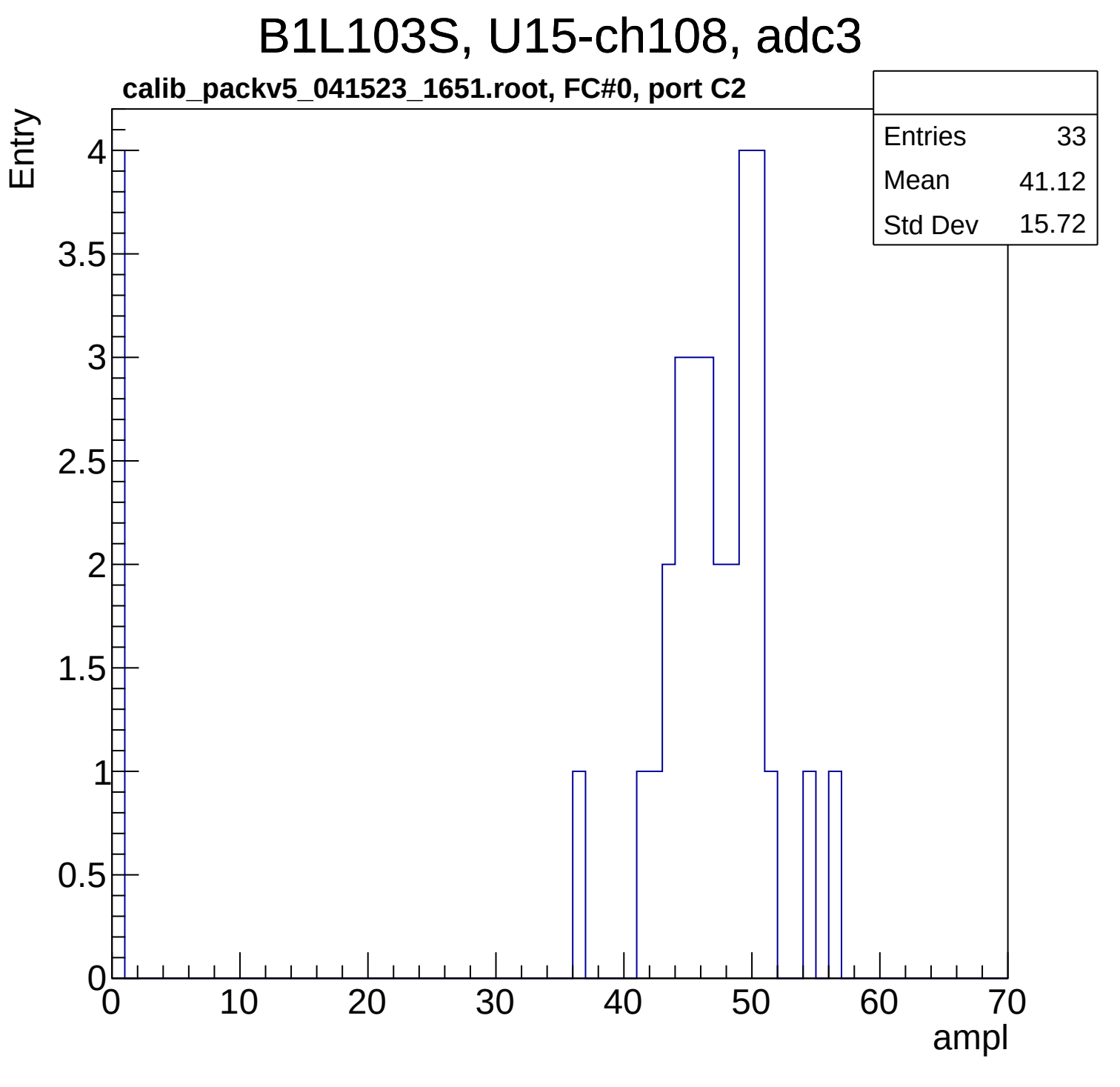

B1L103S, U15-ch107, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

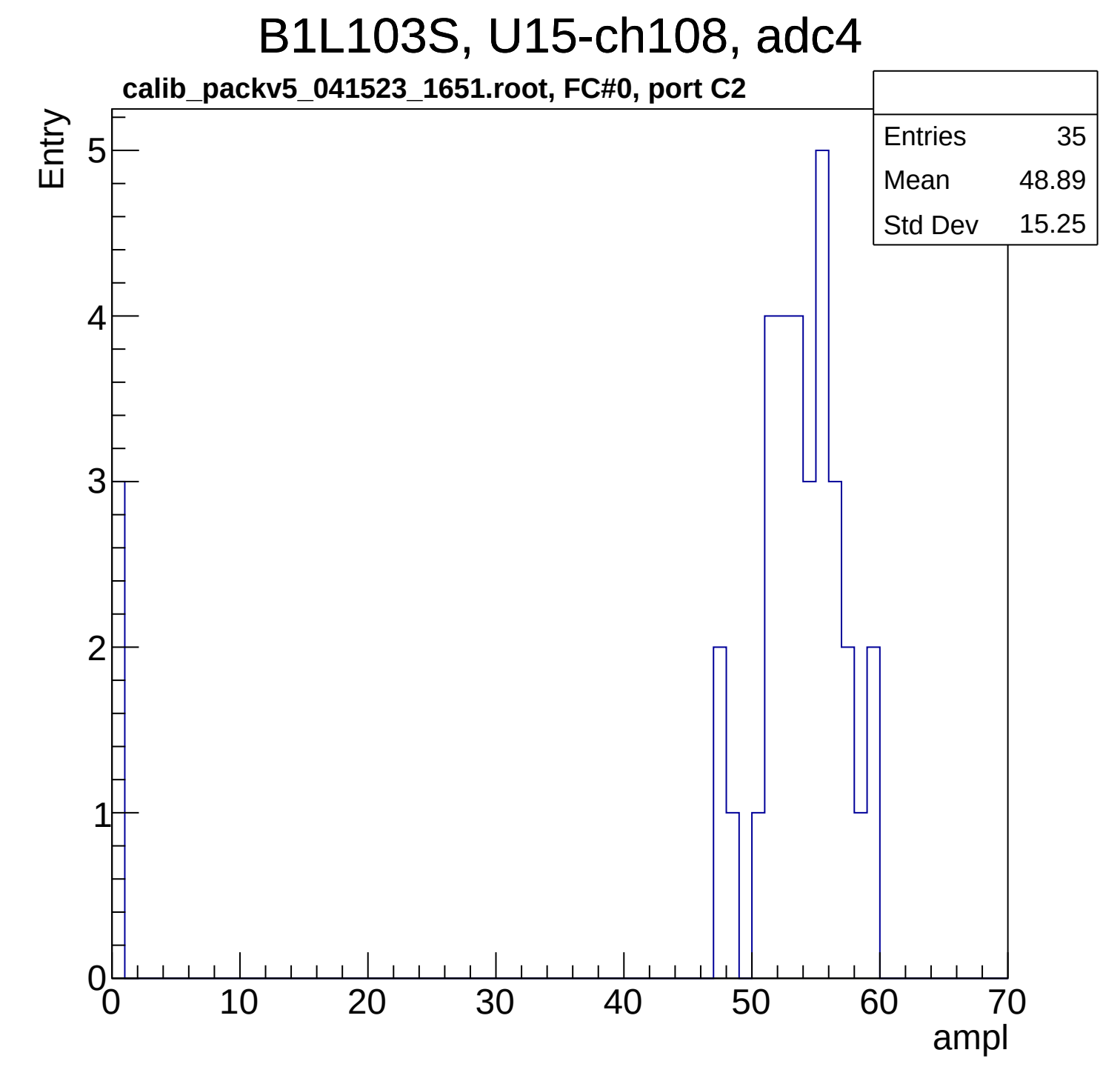

B1L103S, U15-ch107, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 0
Std Dev 0
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

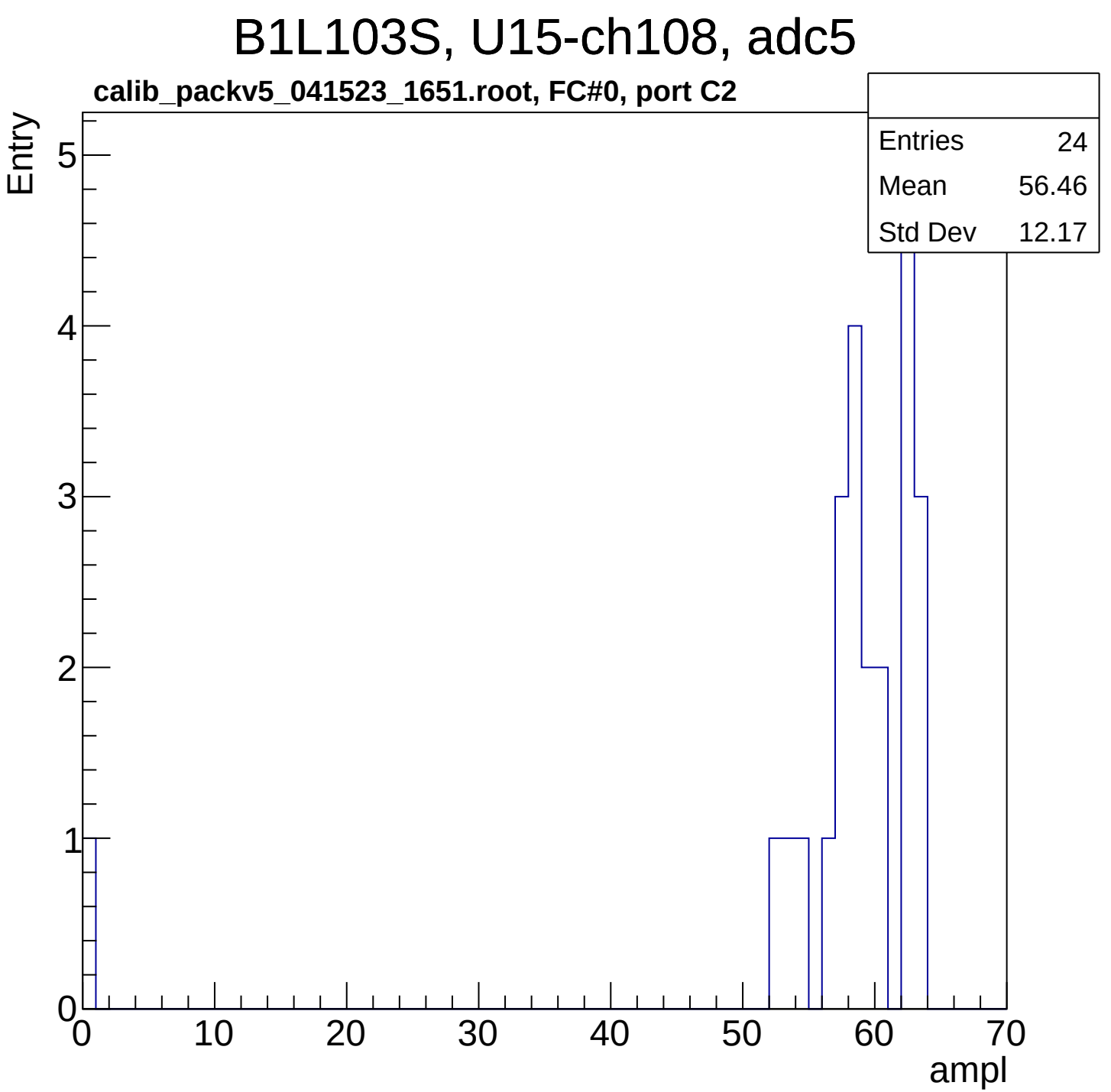

B1L103S, U15-ch108, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 20.59
Std Dev 13.62
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

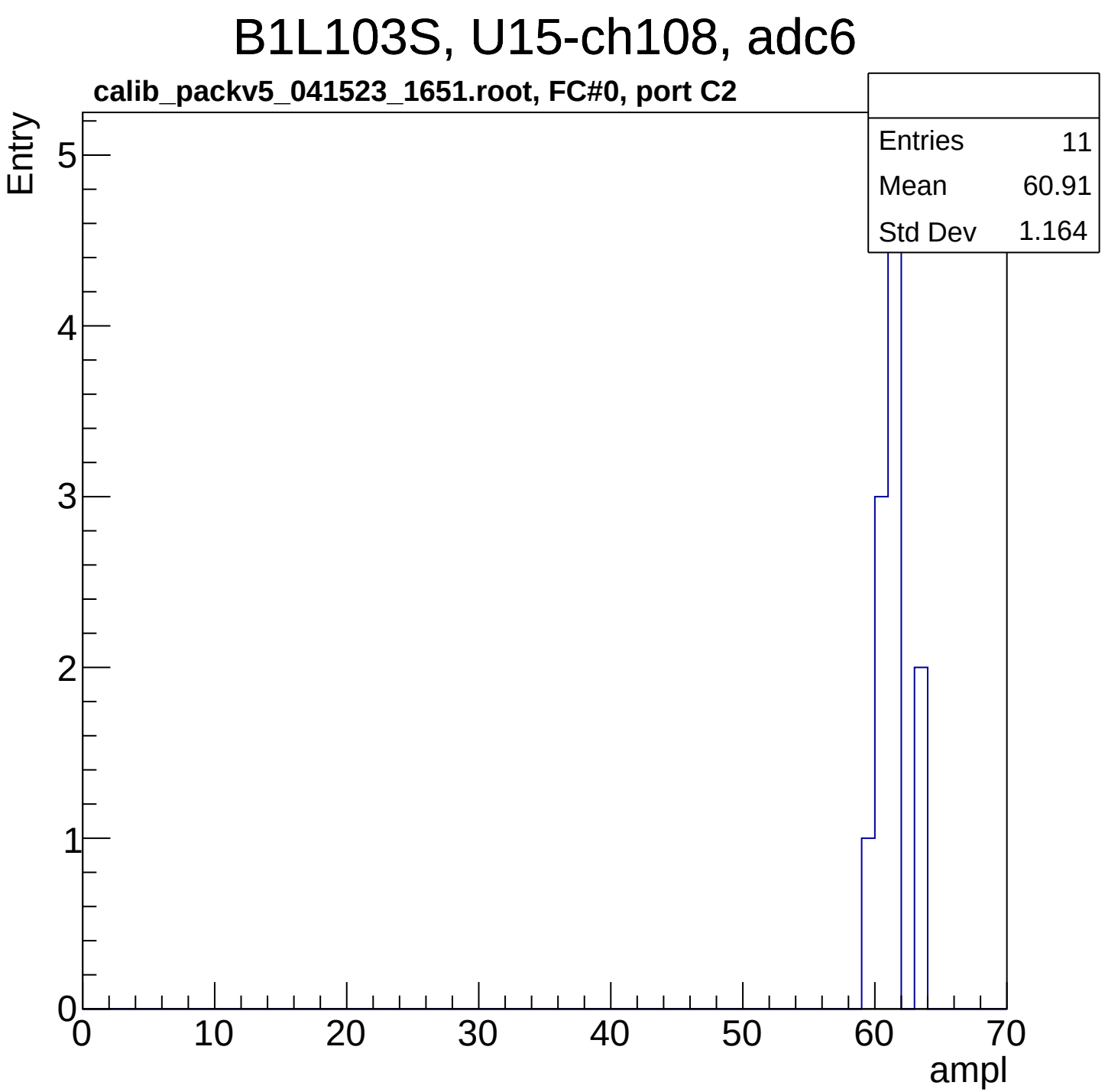

B1L103S, U15-ch108, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 33.4
Std Dev 6.9
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

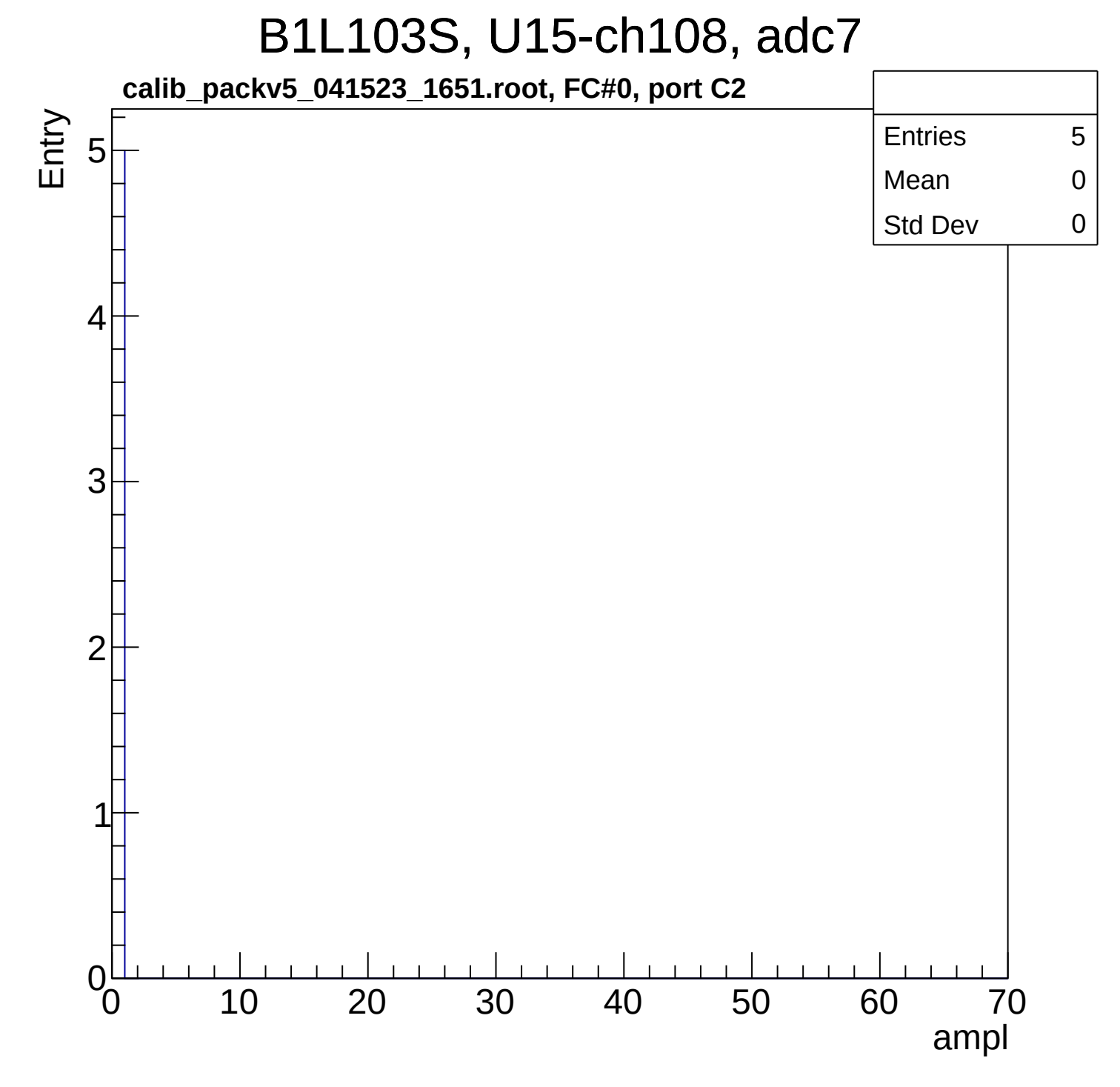

B1L103S, U15-ch108, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 41.78
Std Dev 3.714
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

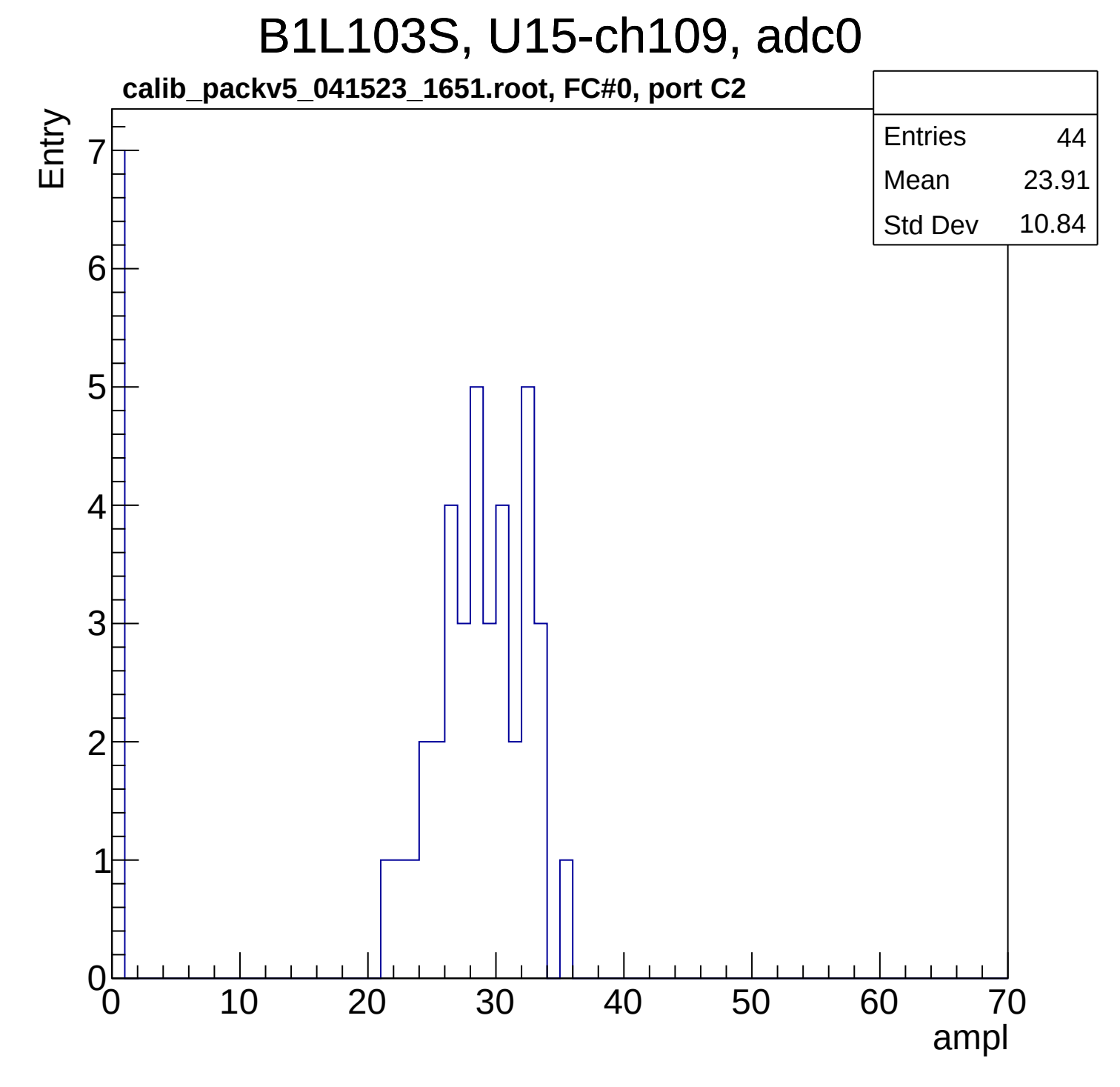

B1L103S, U15-ch108, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 41.12
Std Dev 15.72
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

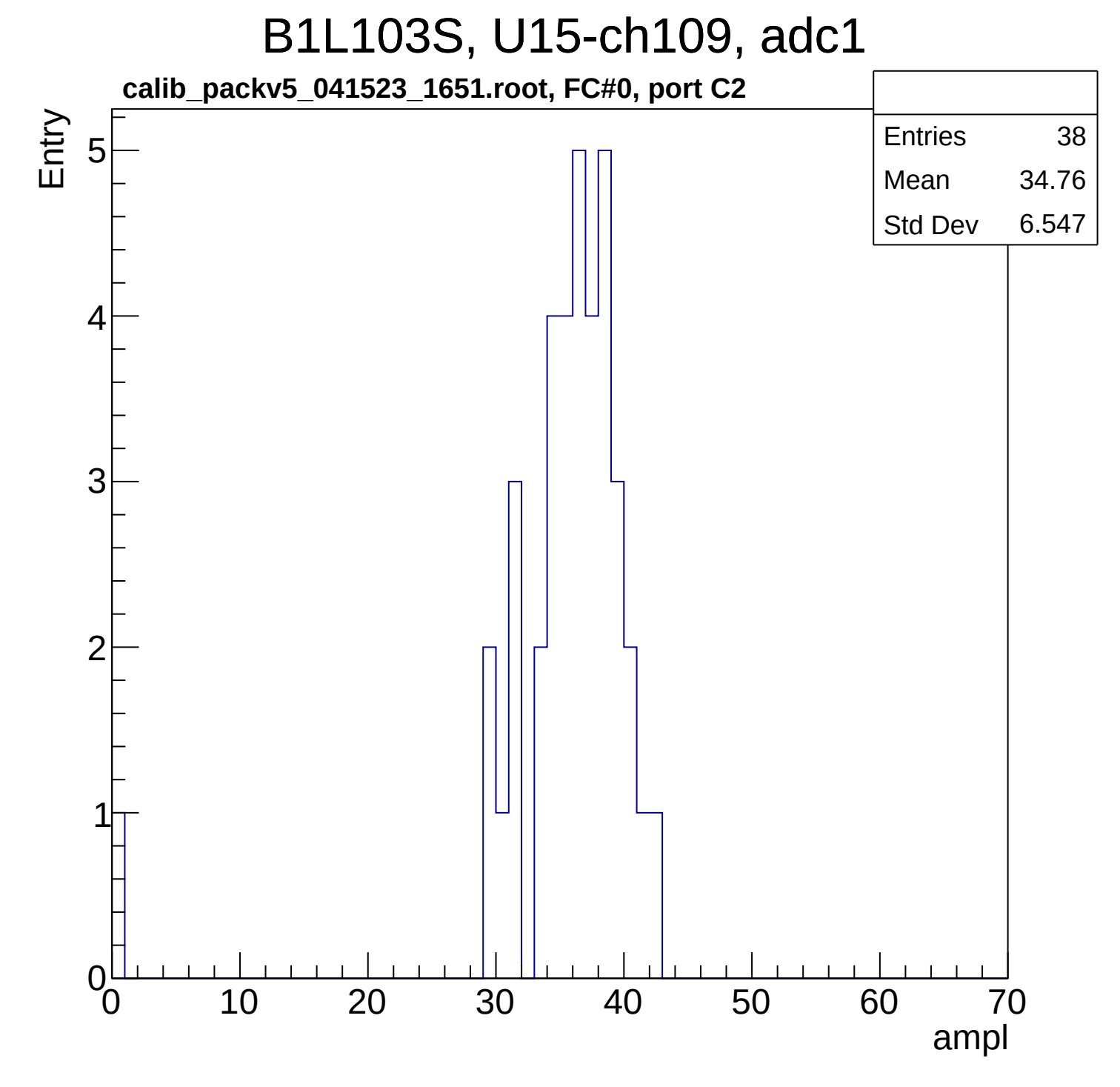

B1L103S, U15-ch108, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 48.89
Std Dev 15.25
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

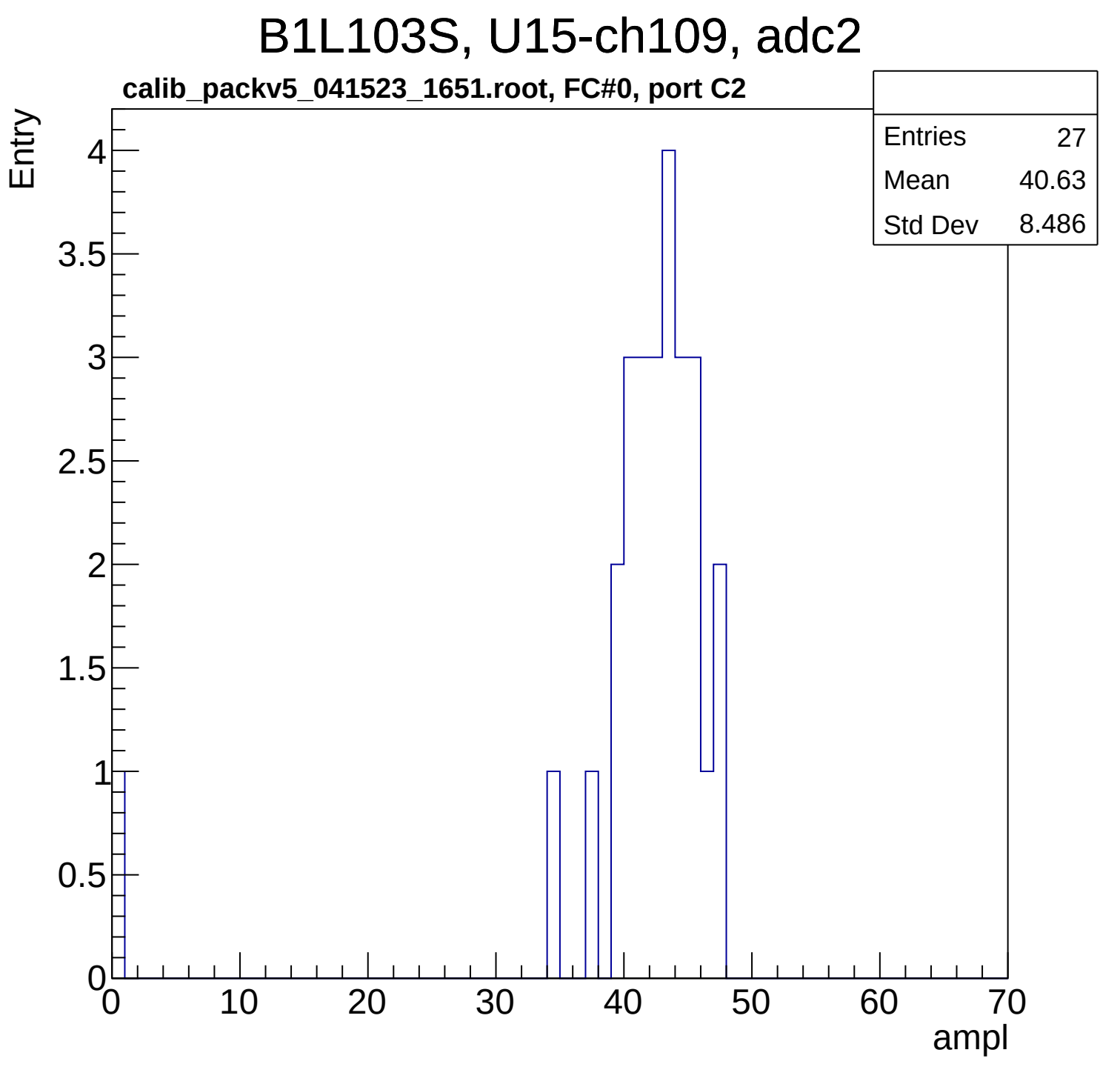

B1L103S, U15-ch108, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 56.46
Std Dev 12.17
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

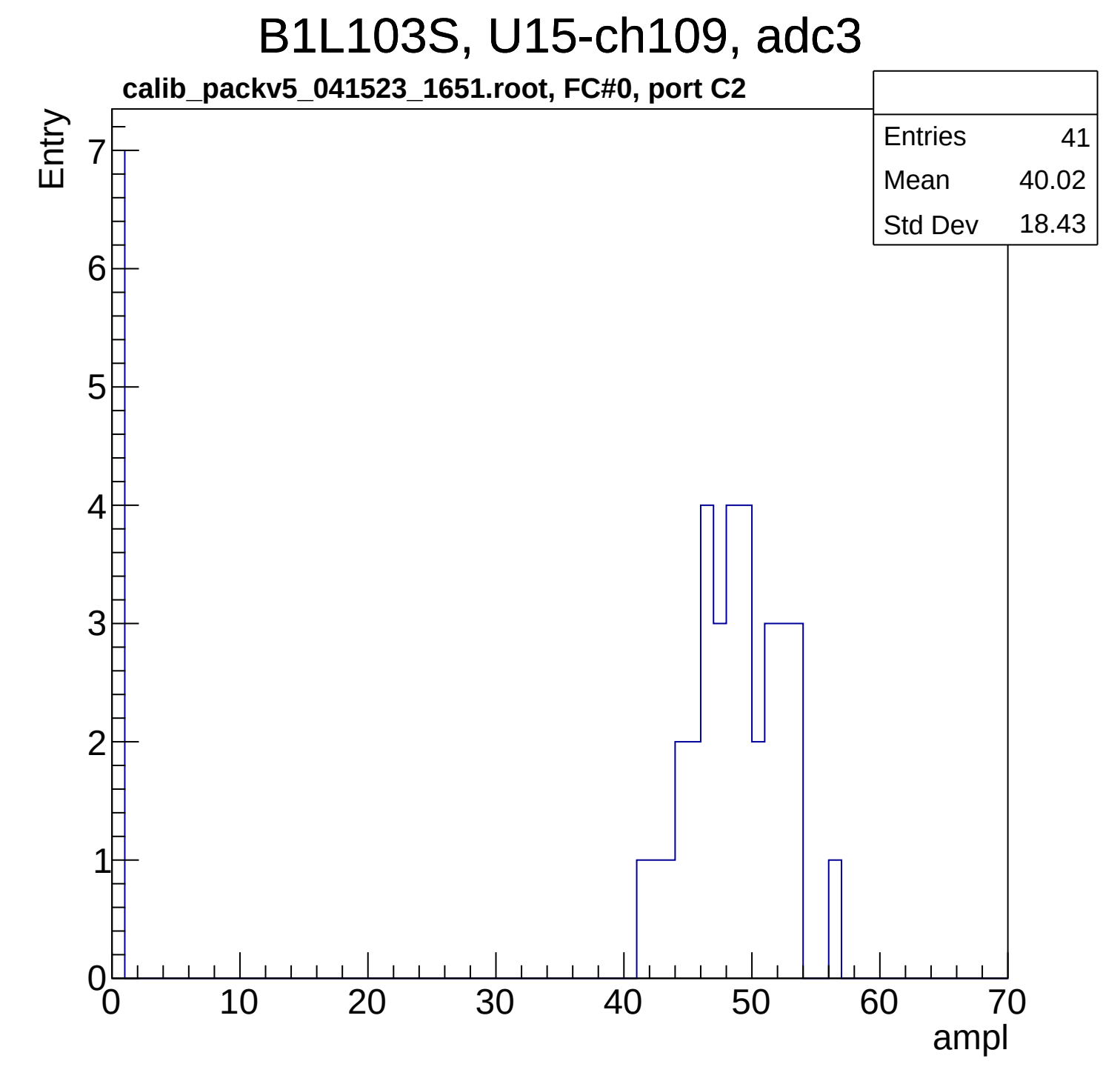

B1L103S, U15-ch108, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 60.91
Std Dev 1.164
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

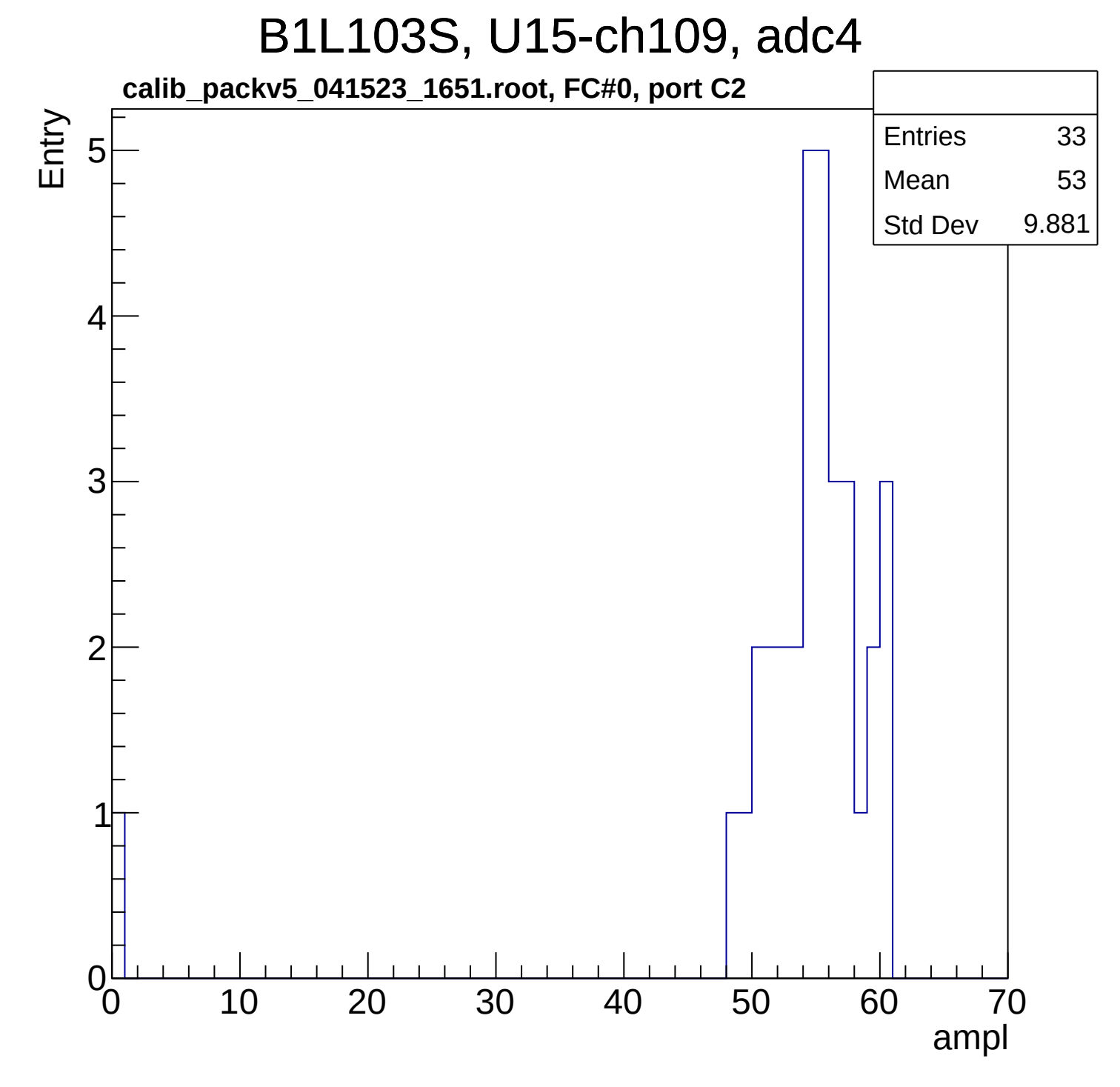

B1L103S, U15-ch108, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 0
Std Dev 0
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

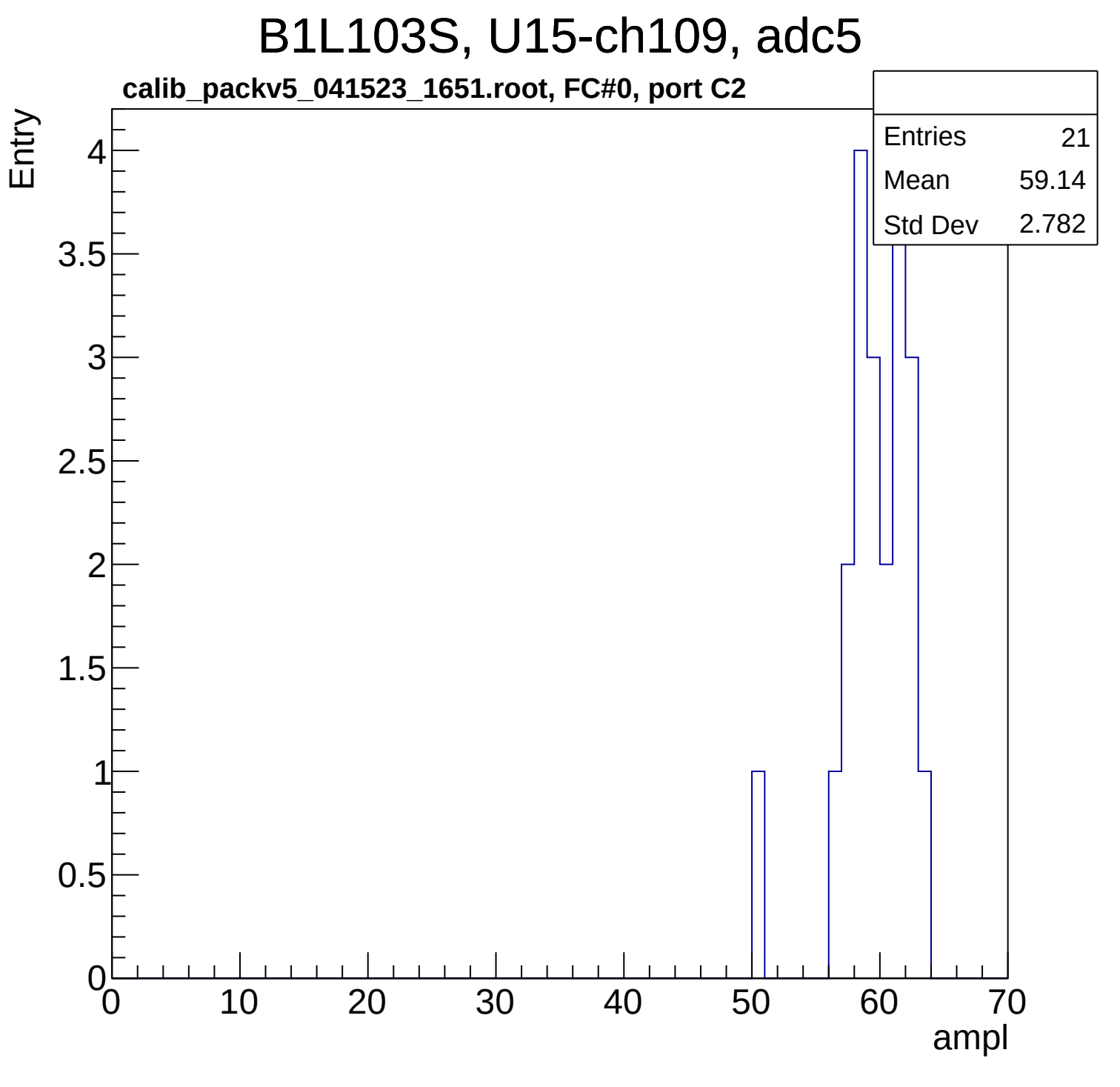

B1L103S, U15-ch109, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 23.91
Std Dev 10.84
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U15-ch109, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 34.76
Std Dev 6.547
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch109, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 40.63
Std Dev 8.486
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch109, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 40.02
Std Dev 18.43
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U15-ch109, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 53
Std Dev 9.881
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch109, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 59.14
Std Dev 2.782
Entry
ampl
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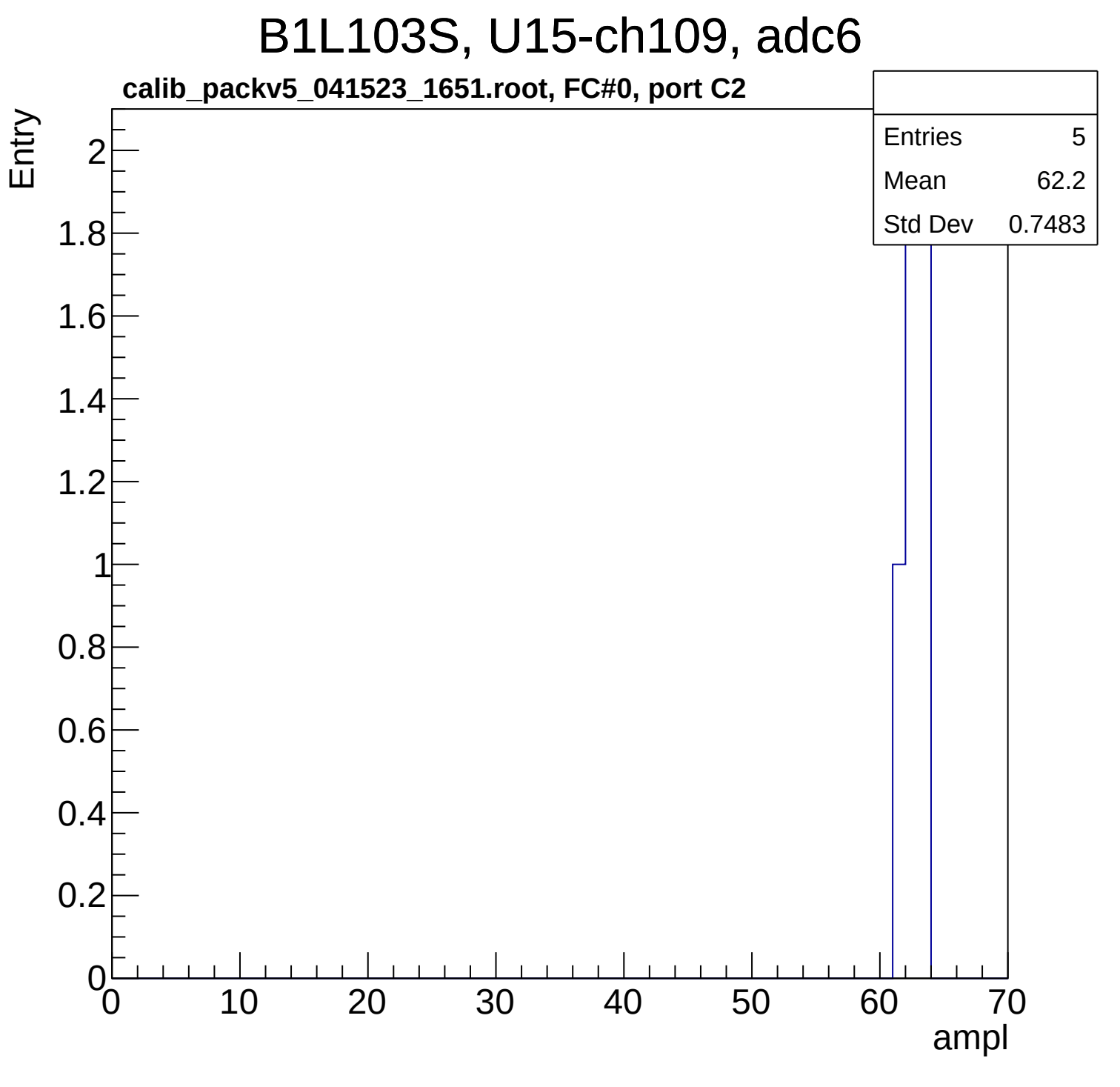
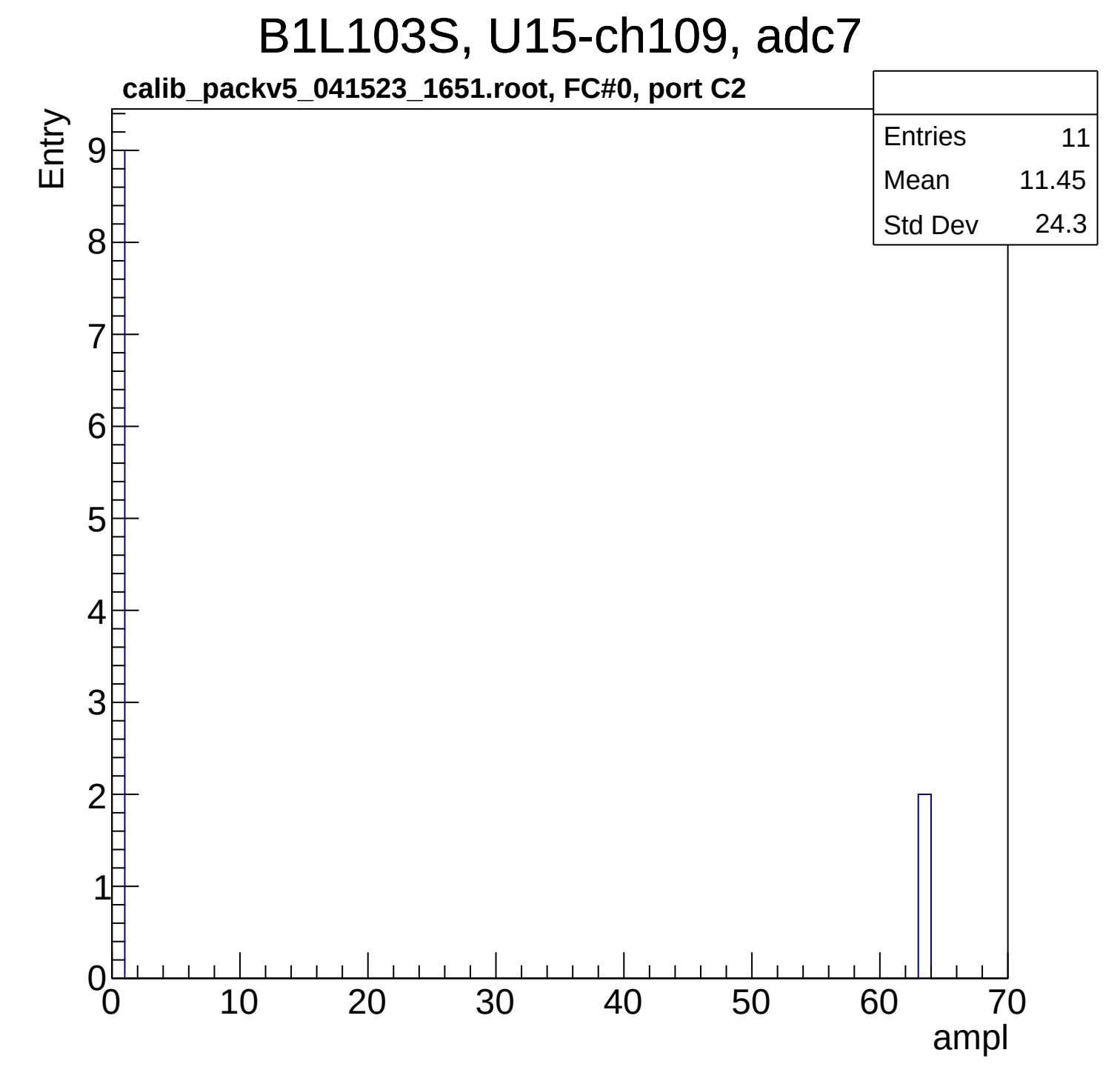
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch109, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.2
Std Dev 0.7483
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U15-ch109, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 11.45
Std Dev 24.3
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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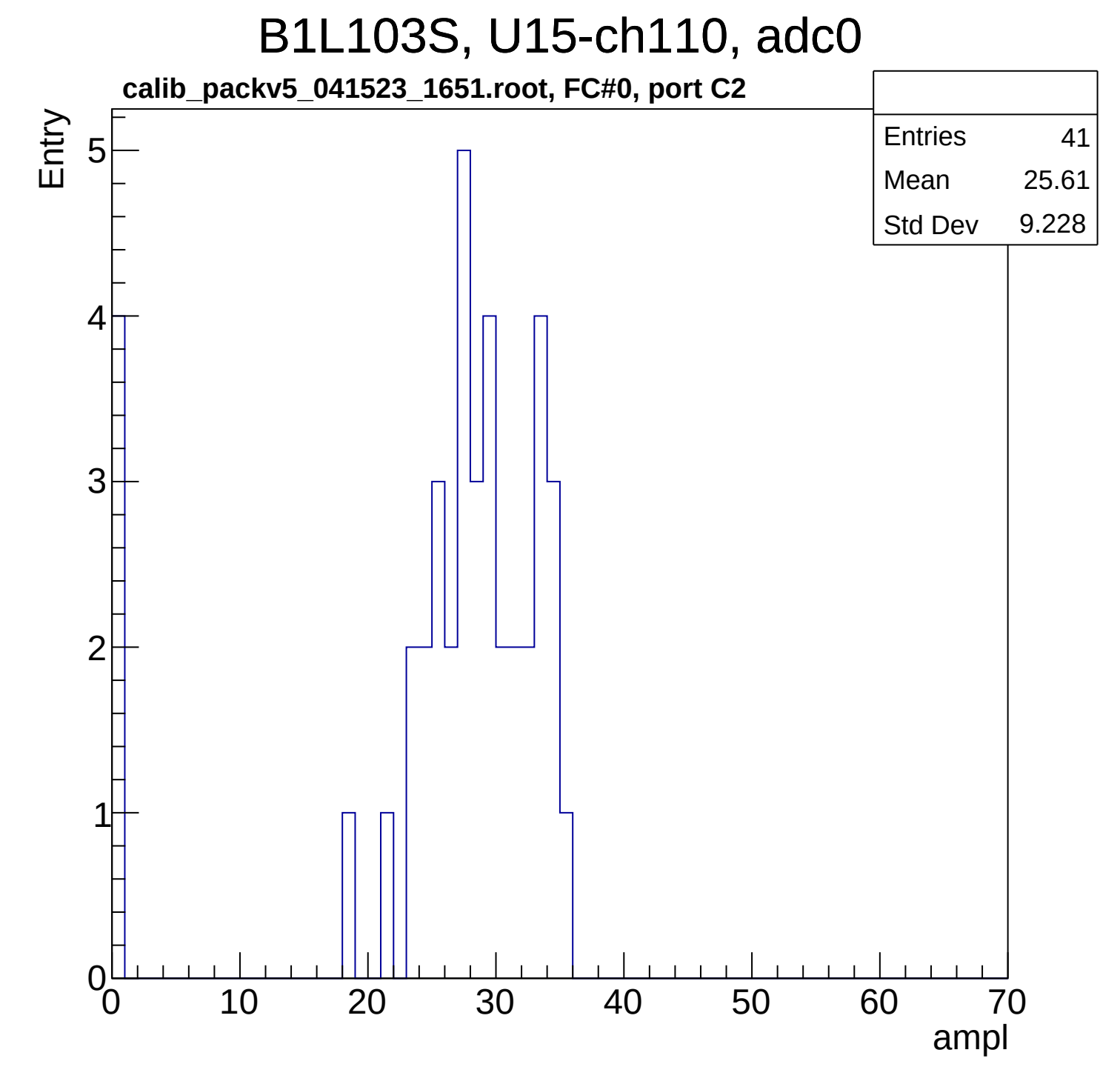
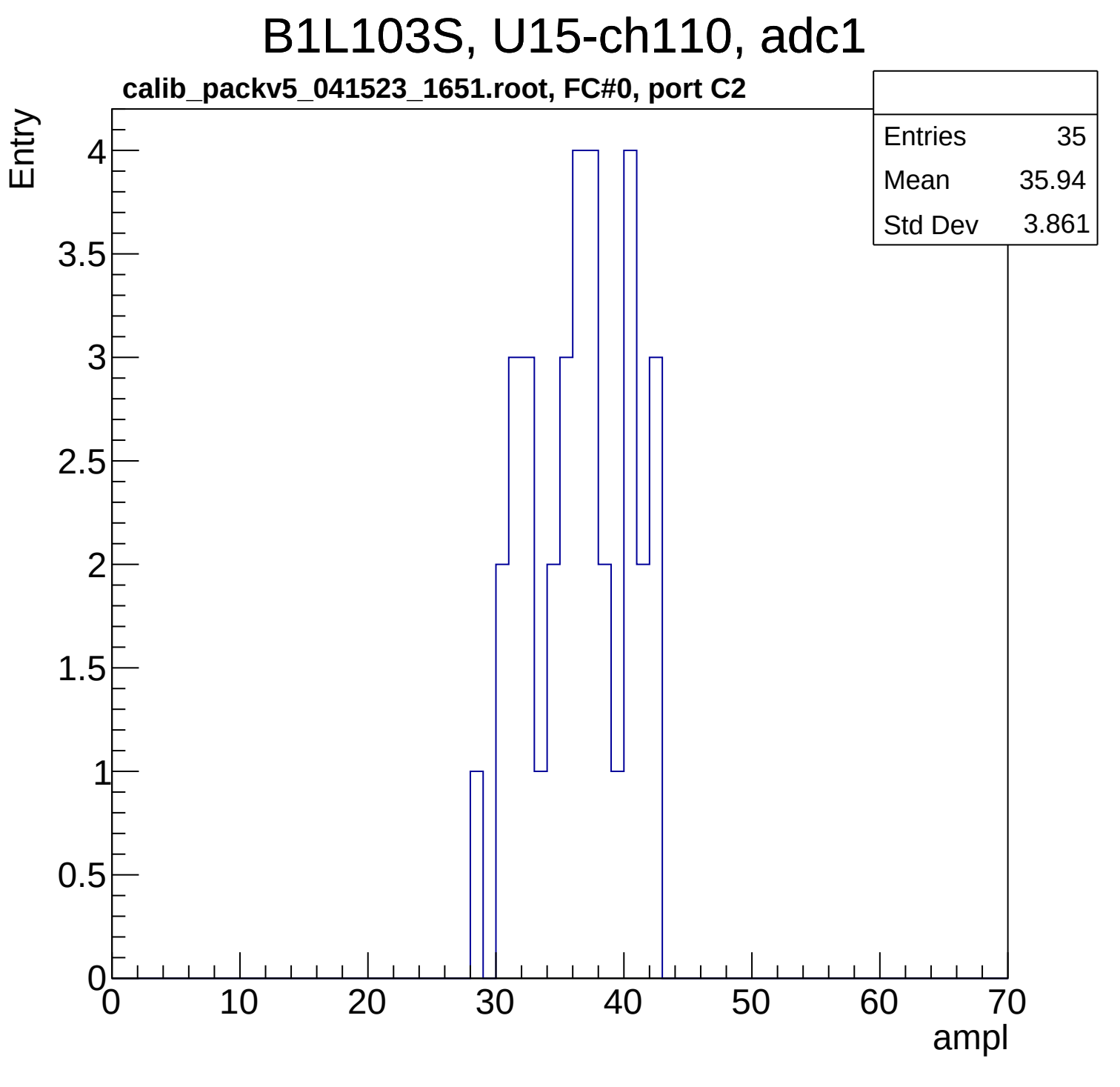
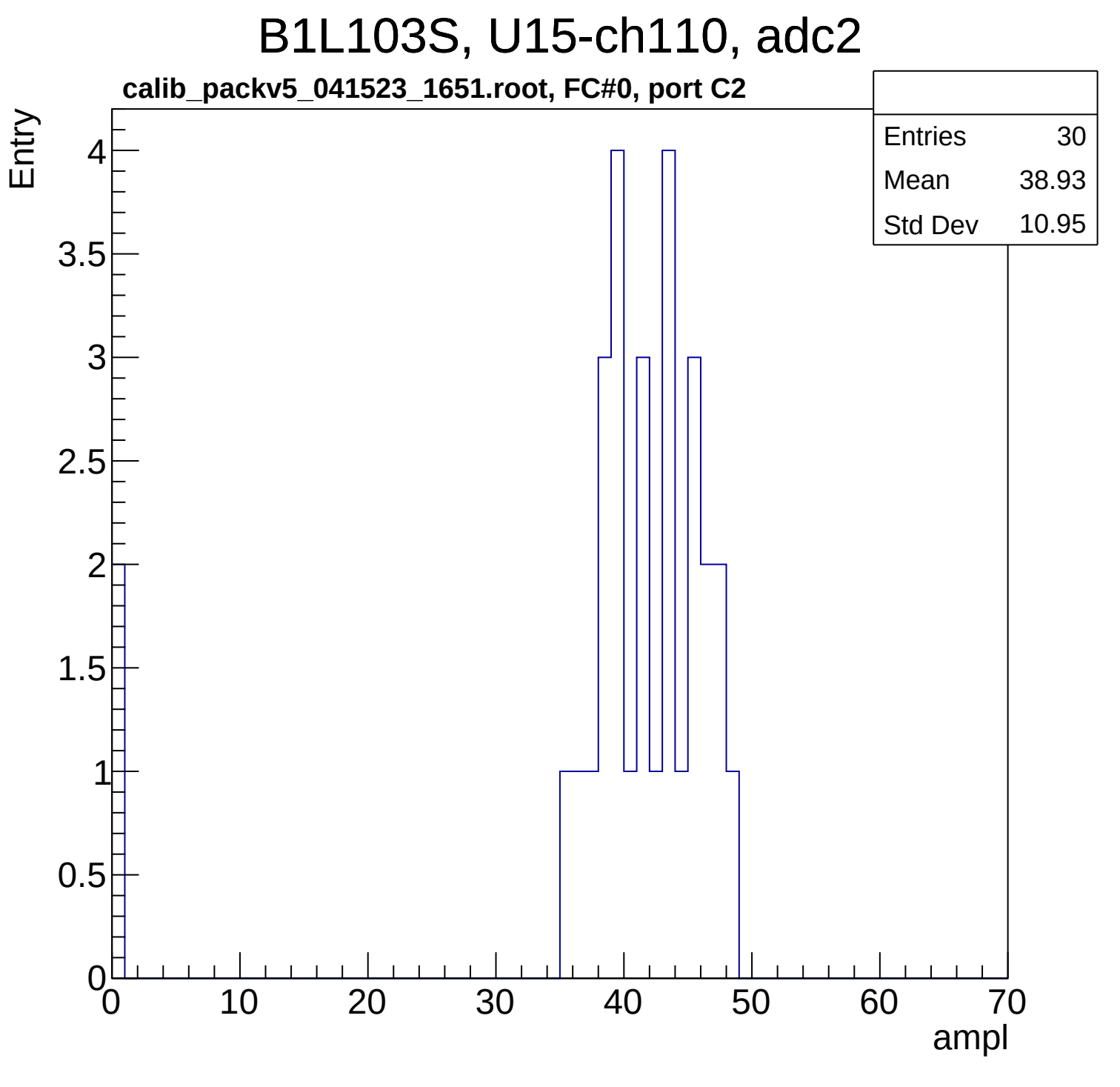
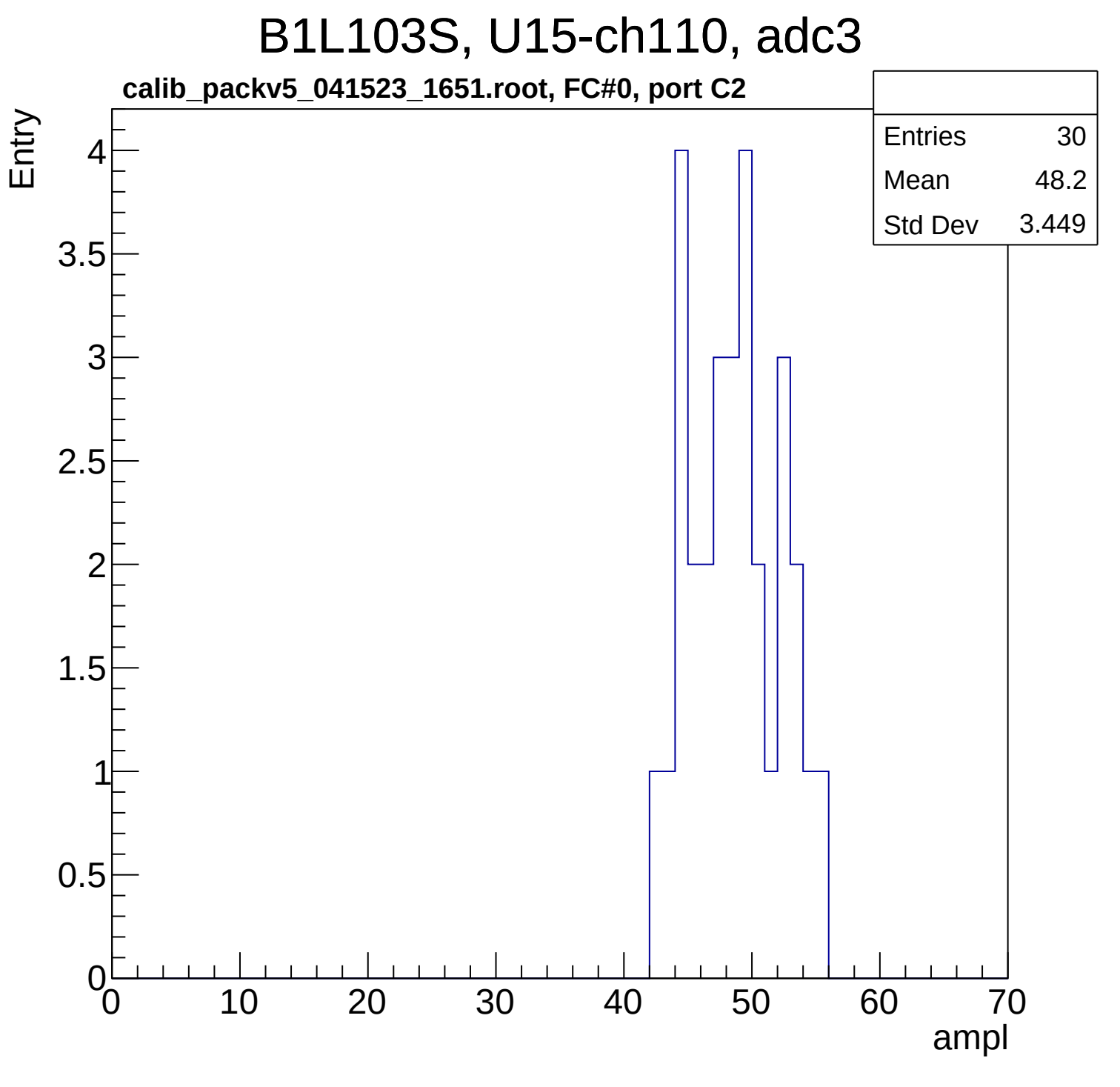
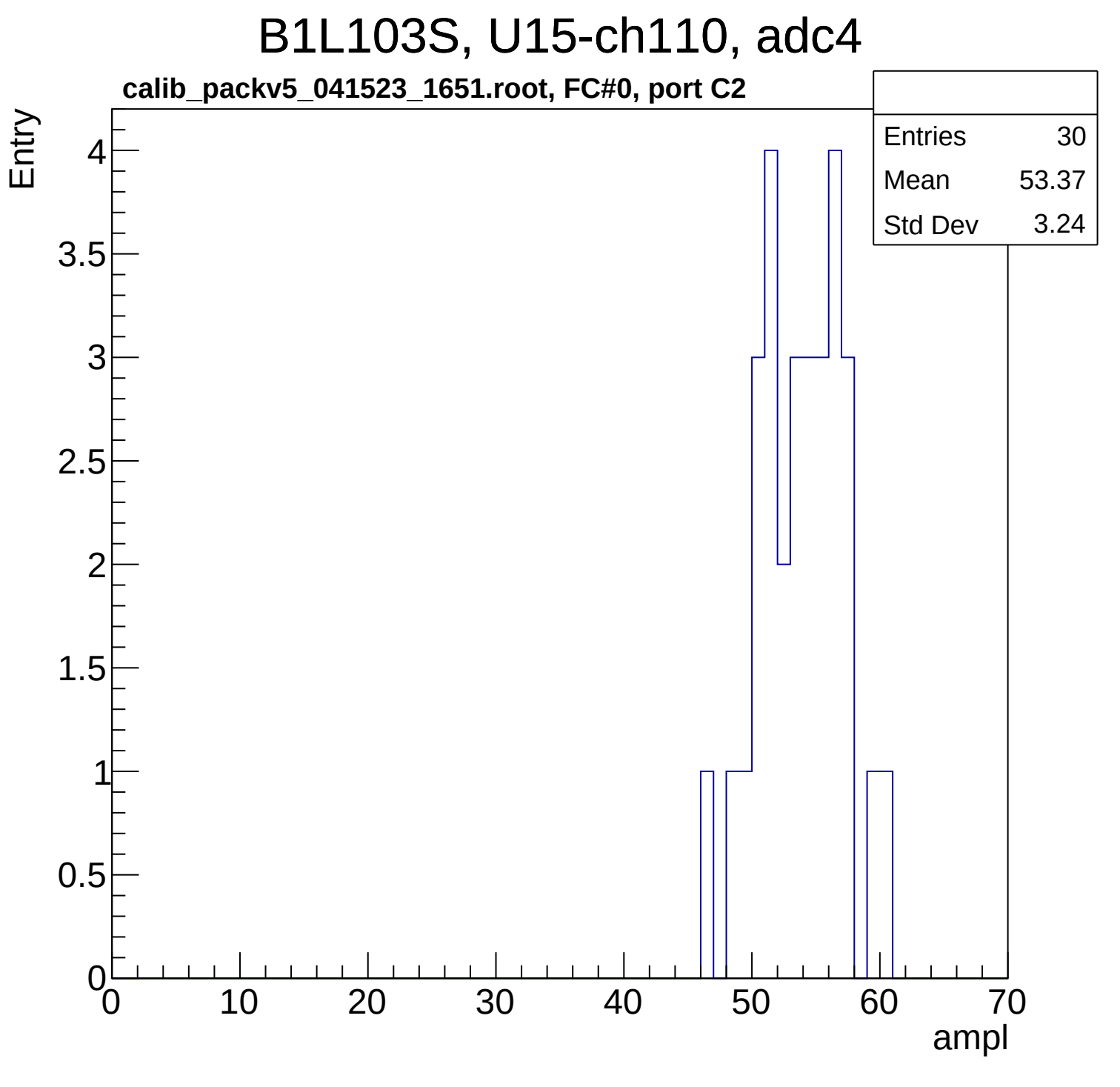
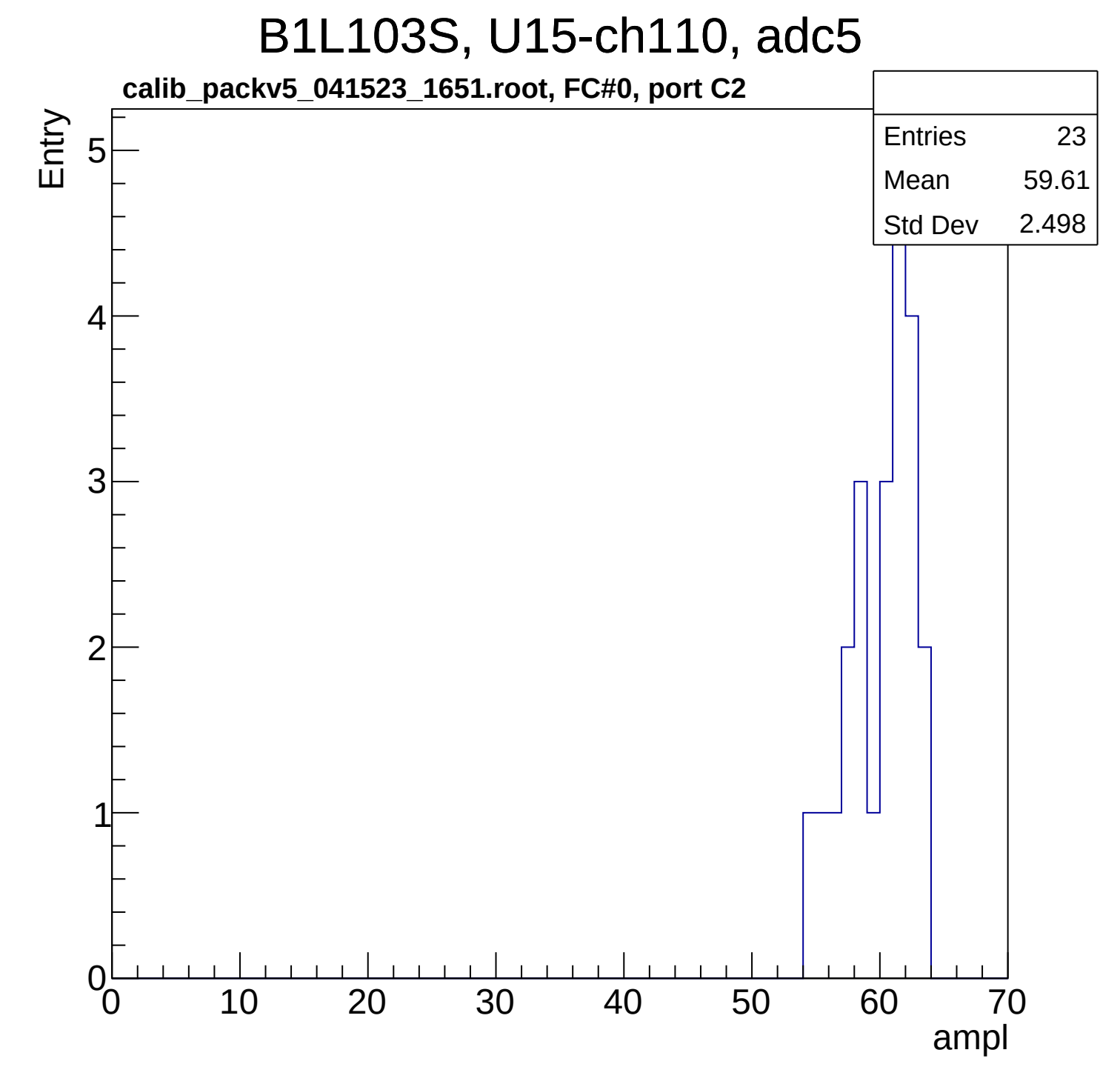

B1L103S, U15-ch110, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 25.61
Std Dev 9.228
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

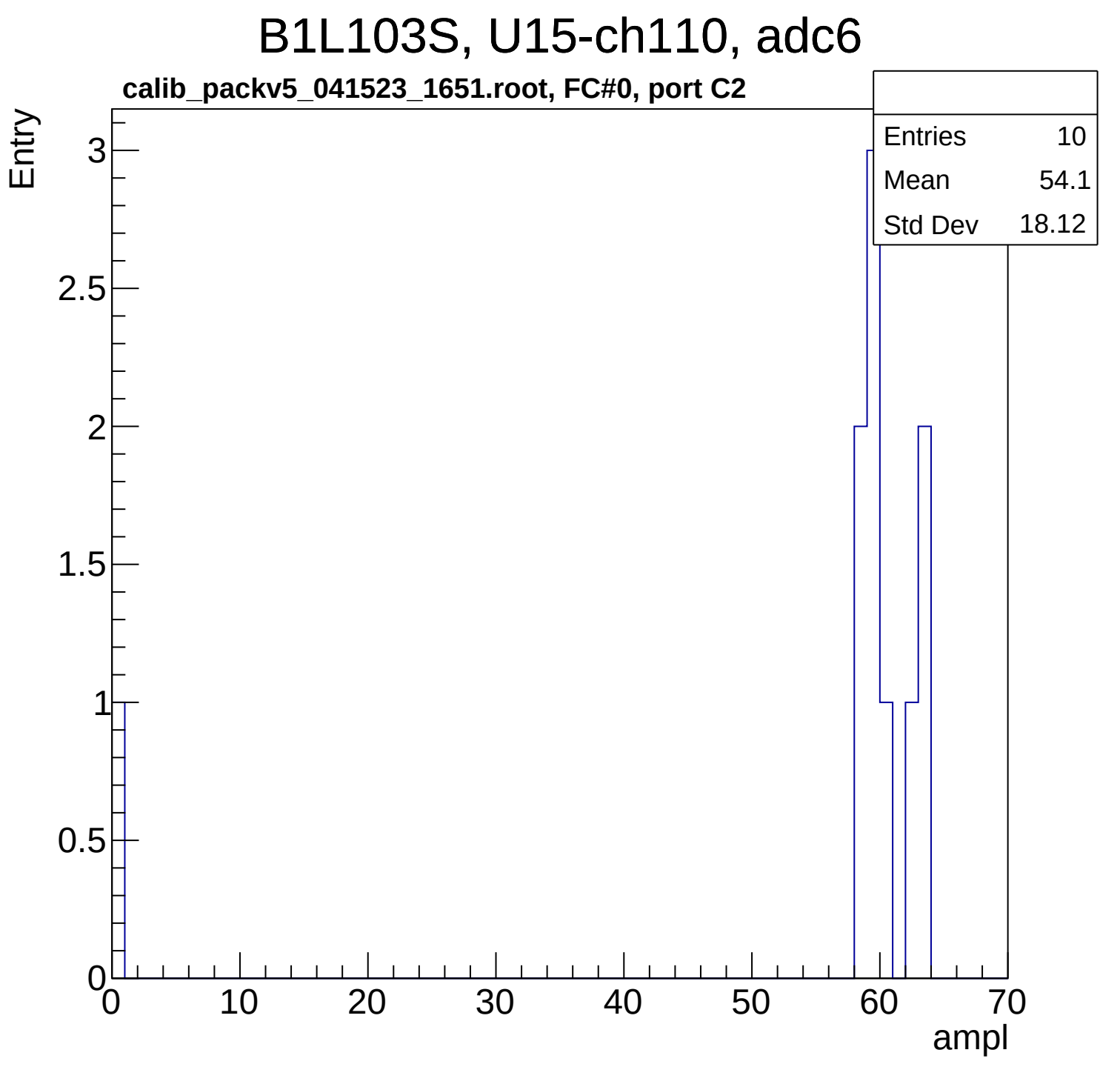

B1L103S, U15-ch110, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 35.94
Std Dev 3.861
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

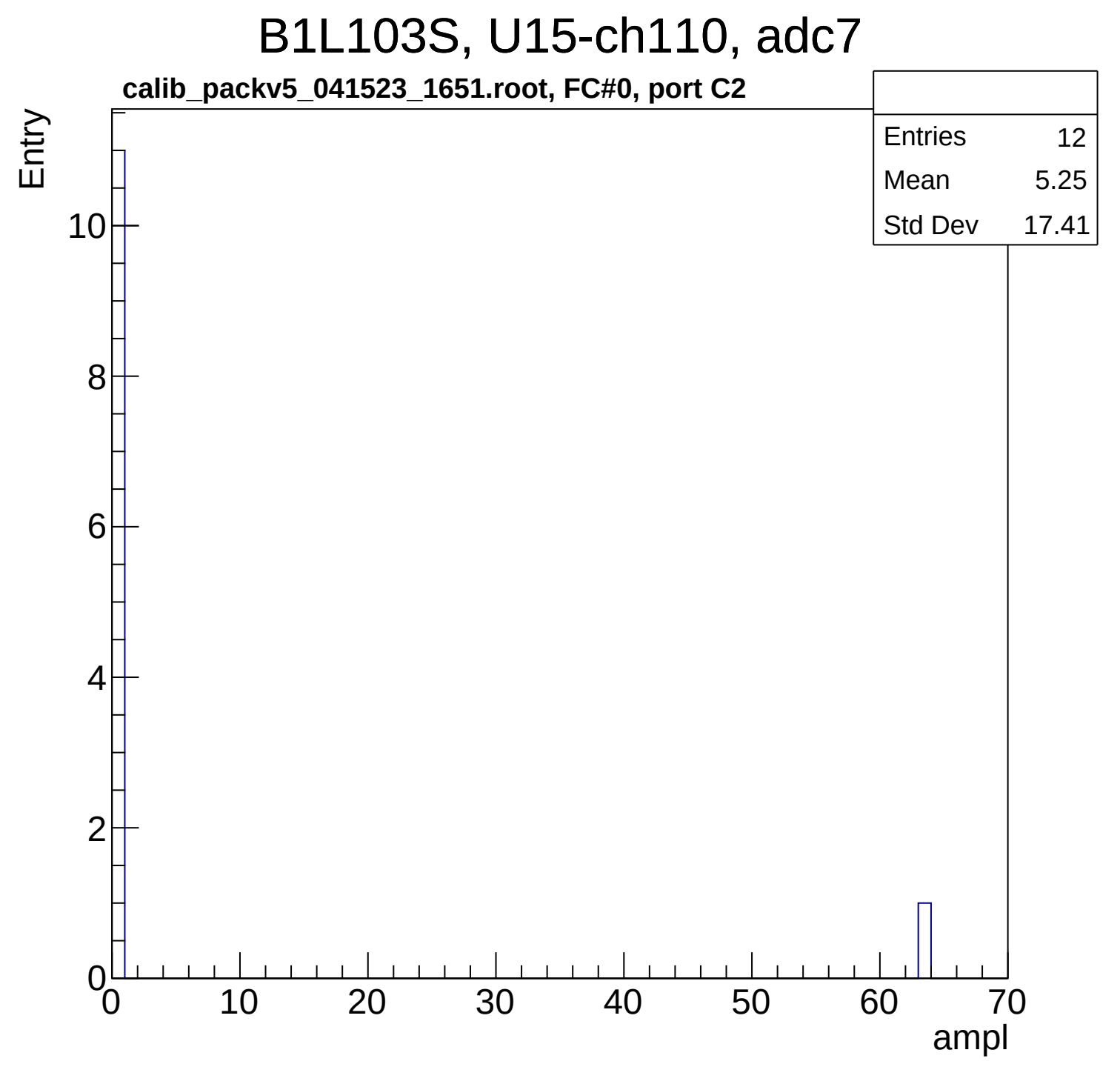

B1L103S, U15-ch110, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 38.93
Std Dev 10.95
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

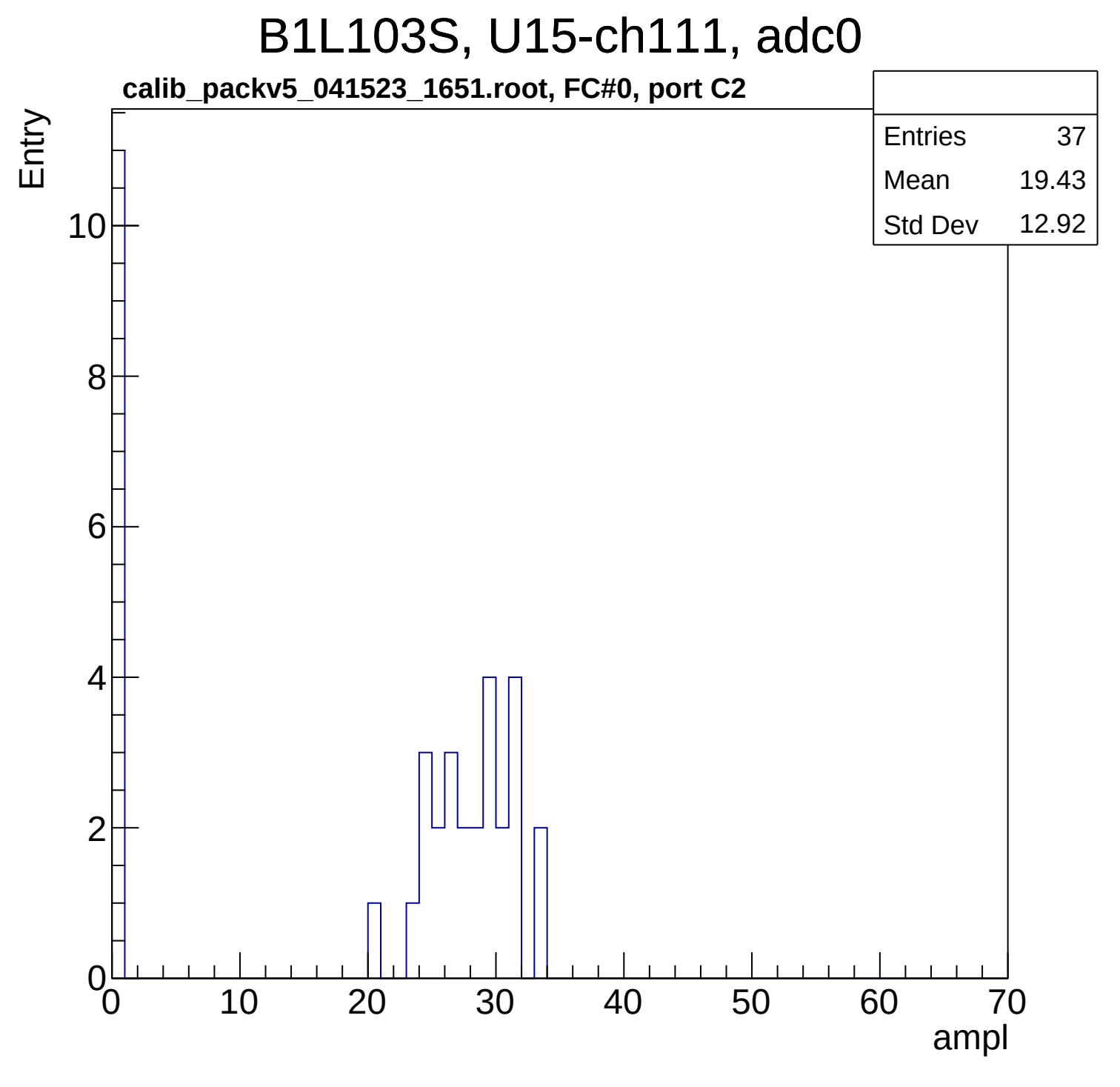

B1L103S, U15-ch110, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 48.2
Std Dev 3.449
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

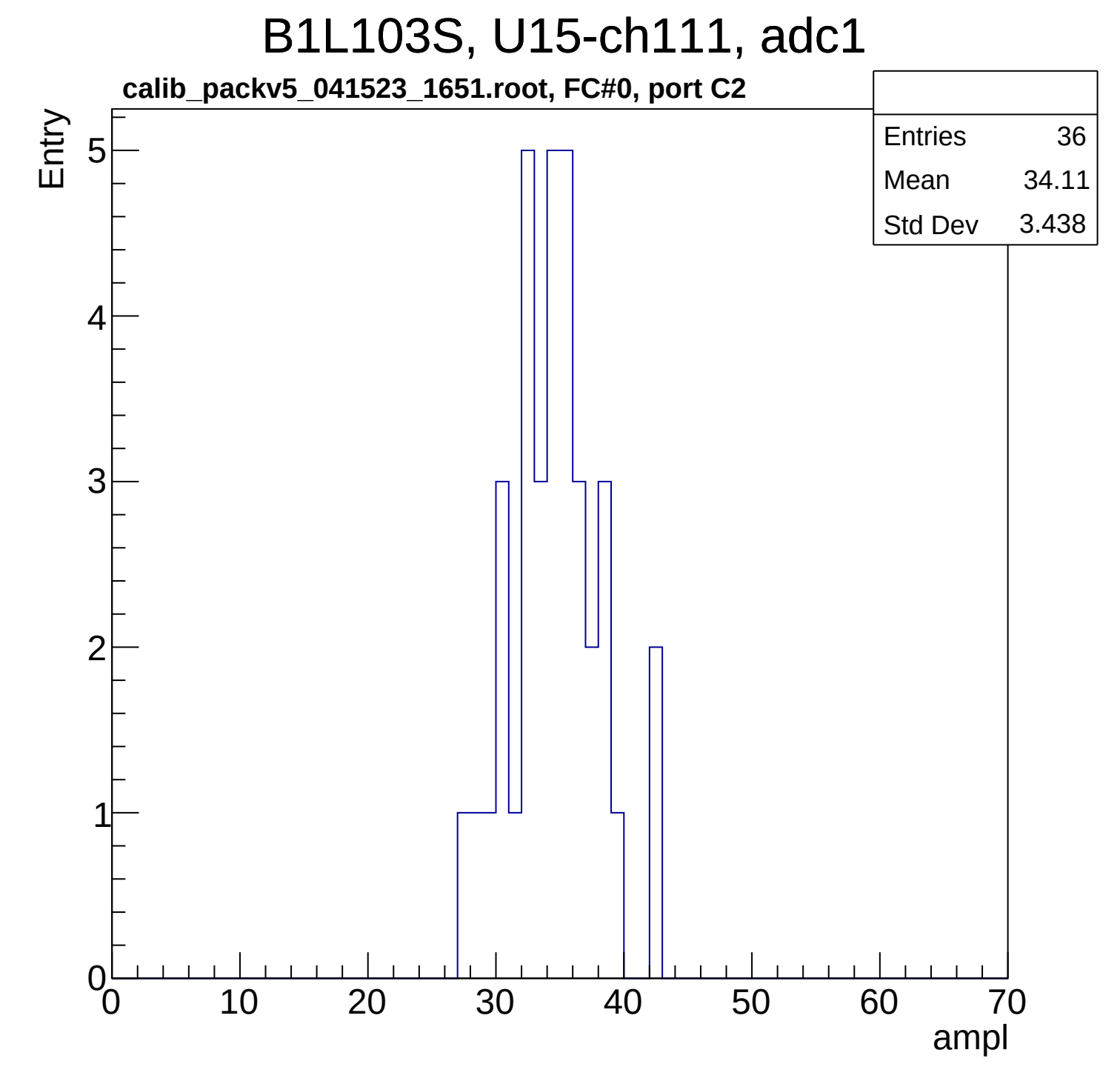

B1L103S, U15-ch110, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 53.37
Std Dev 3.24
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

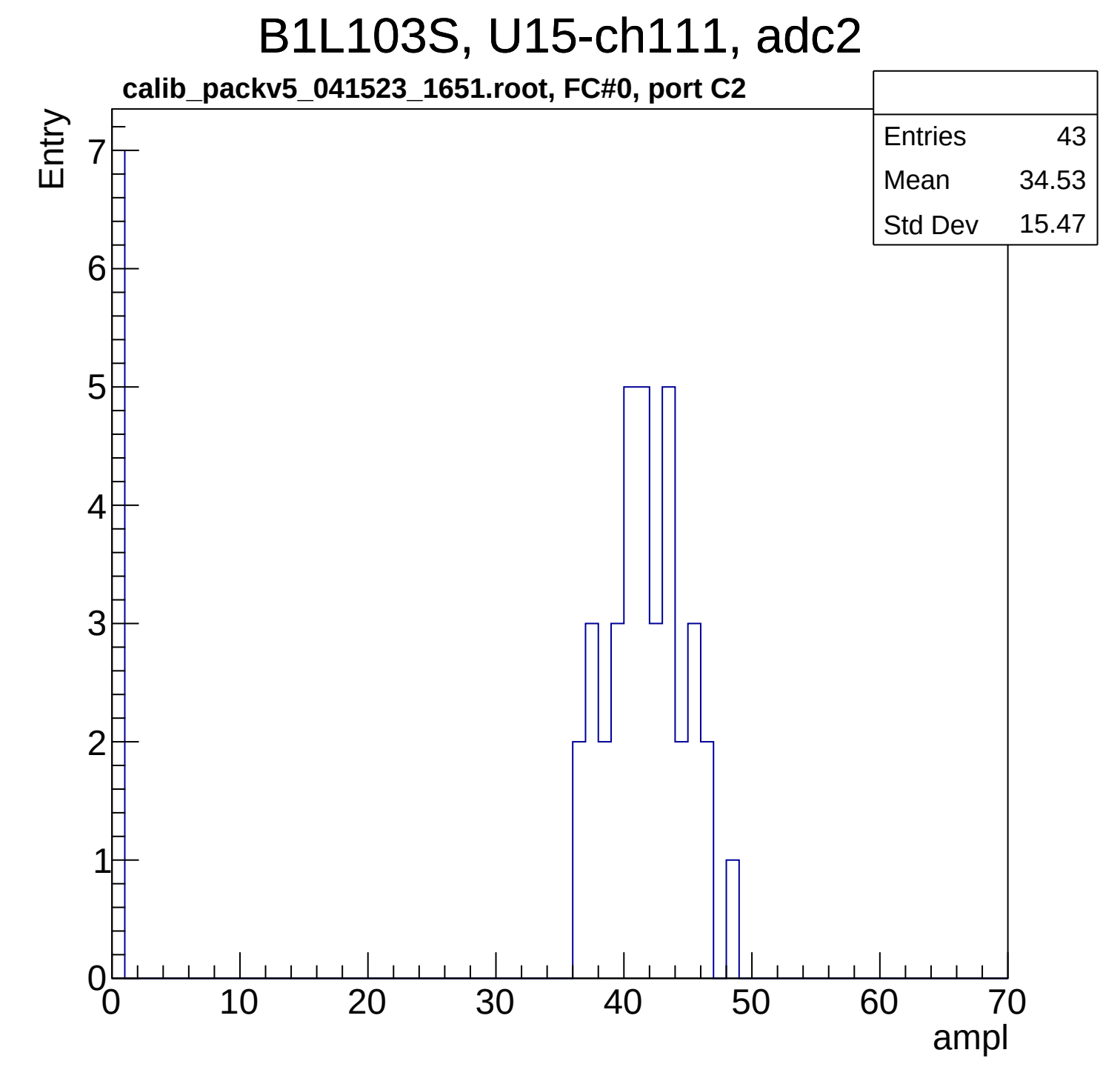

B1L103S, U15-ch110, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 59.61
Std Dev 2.498
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch110, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 54.1
Std Dev 18.12
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch110, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 5.25
Std Dev 17.41
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch111, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 19.43
Std Dev 12.92
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U15-ch111, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 34.11
Std Dev 3.438
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch111, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 34.53
Std Dev 15.47
Entry
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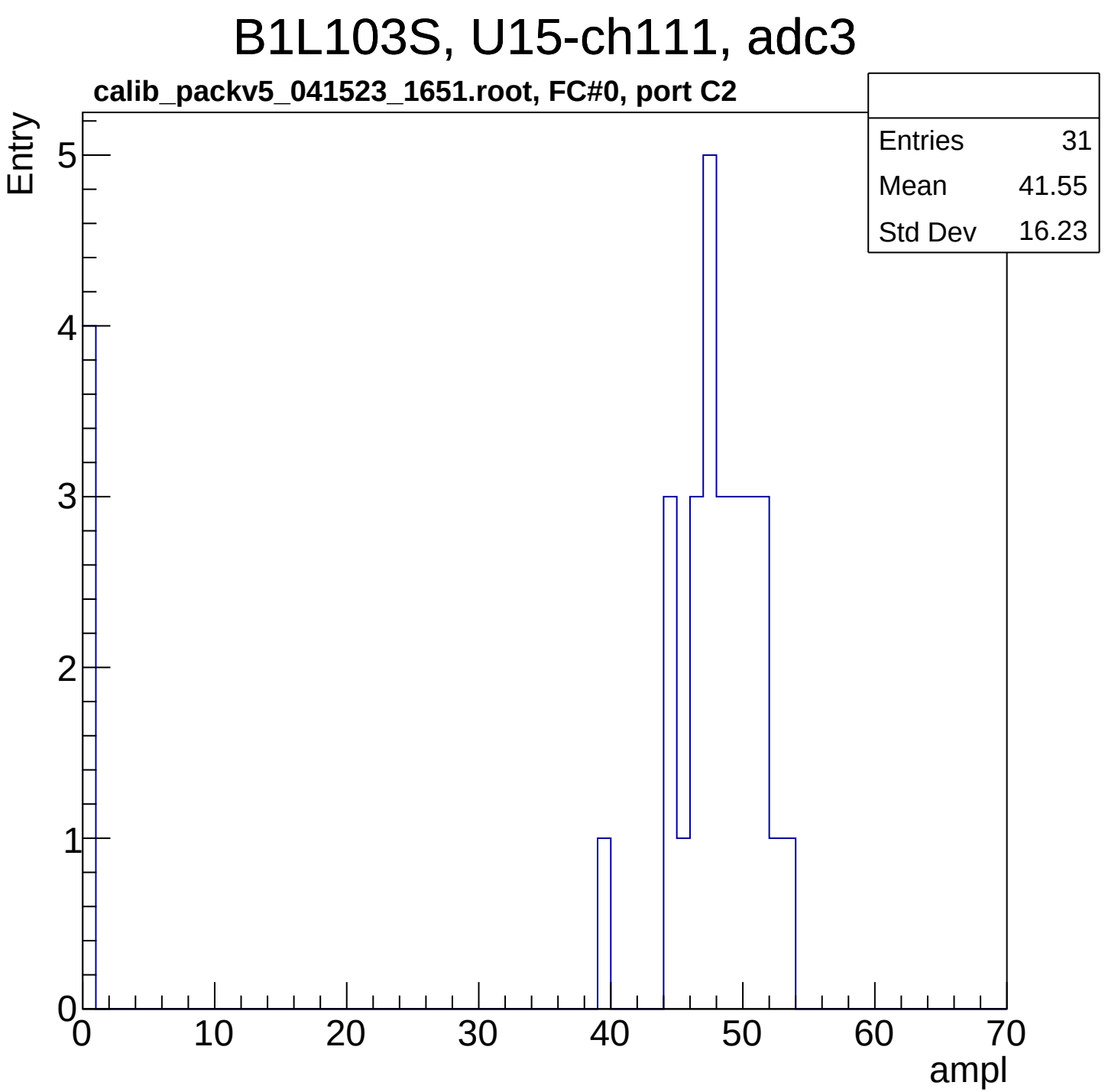
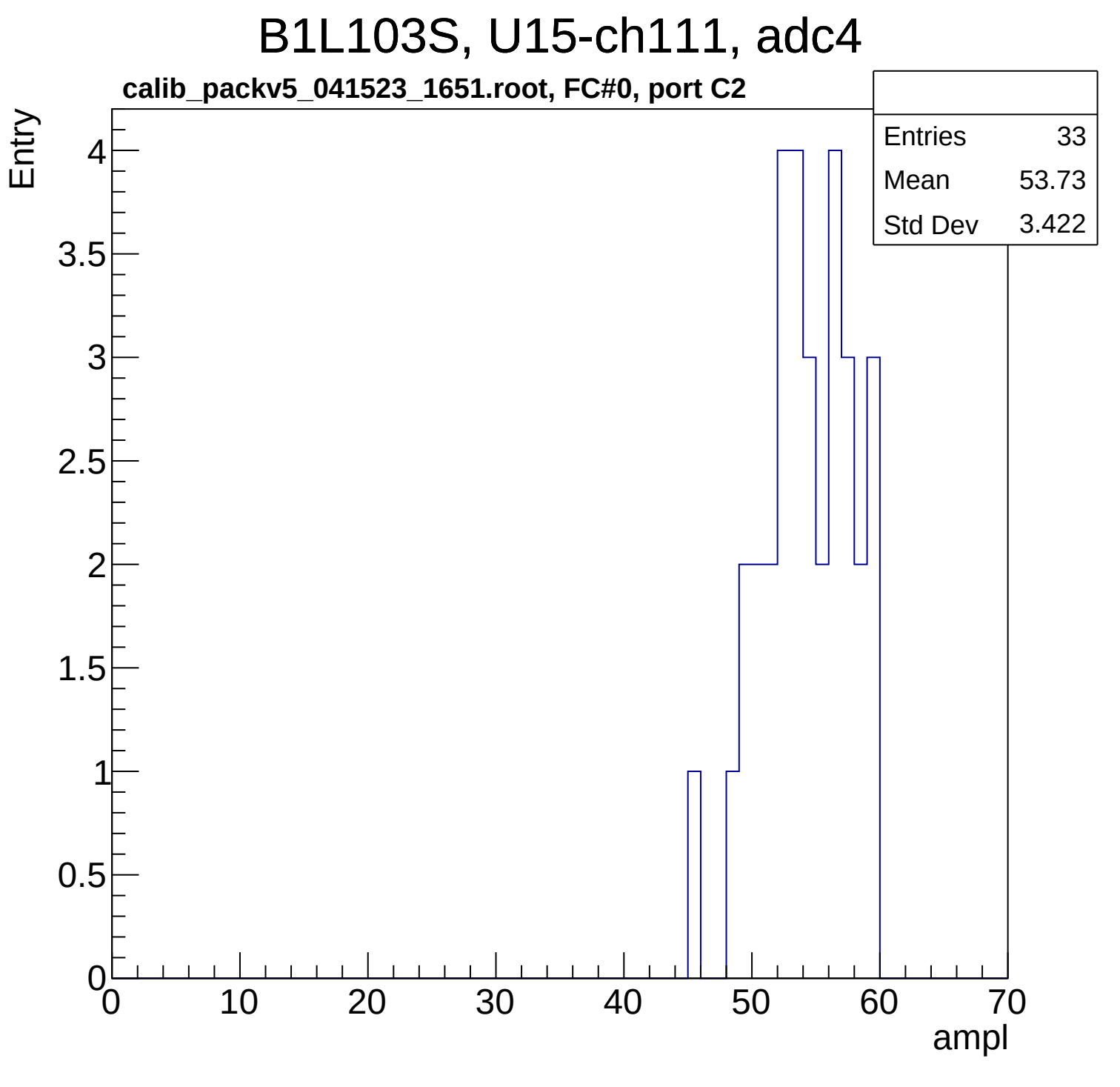
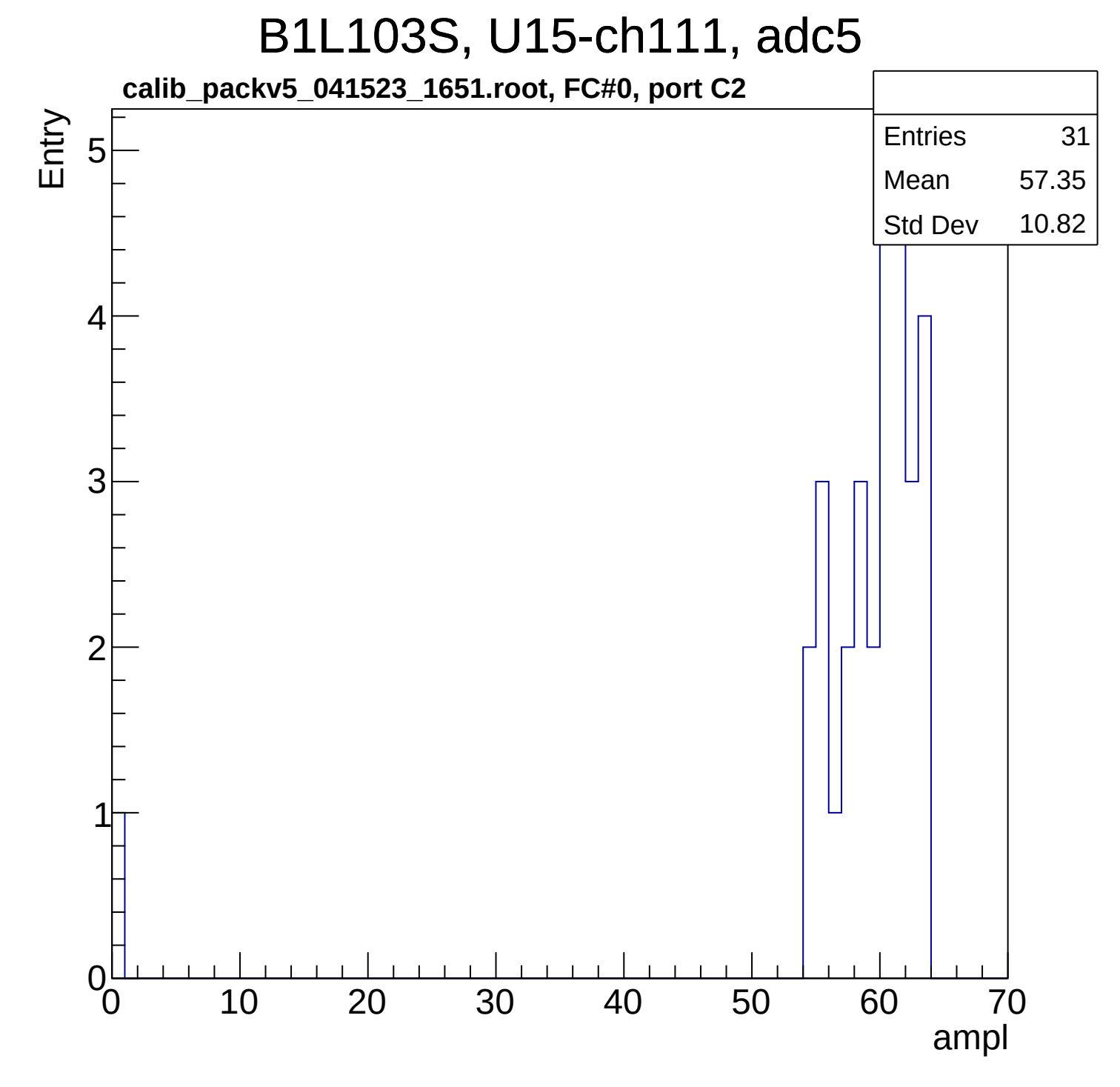
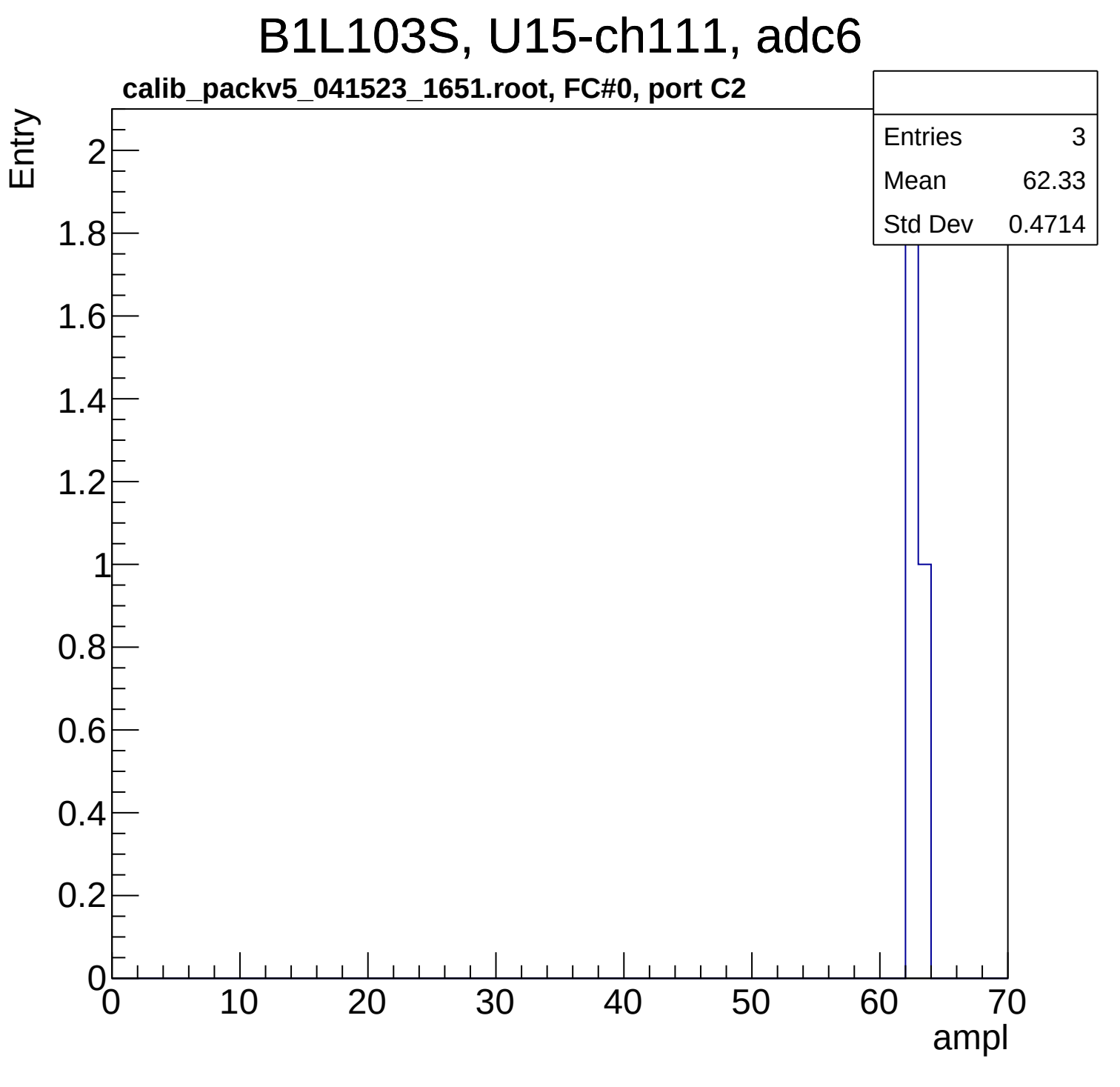
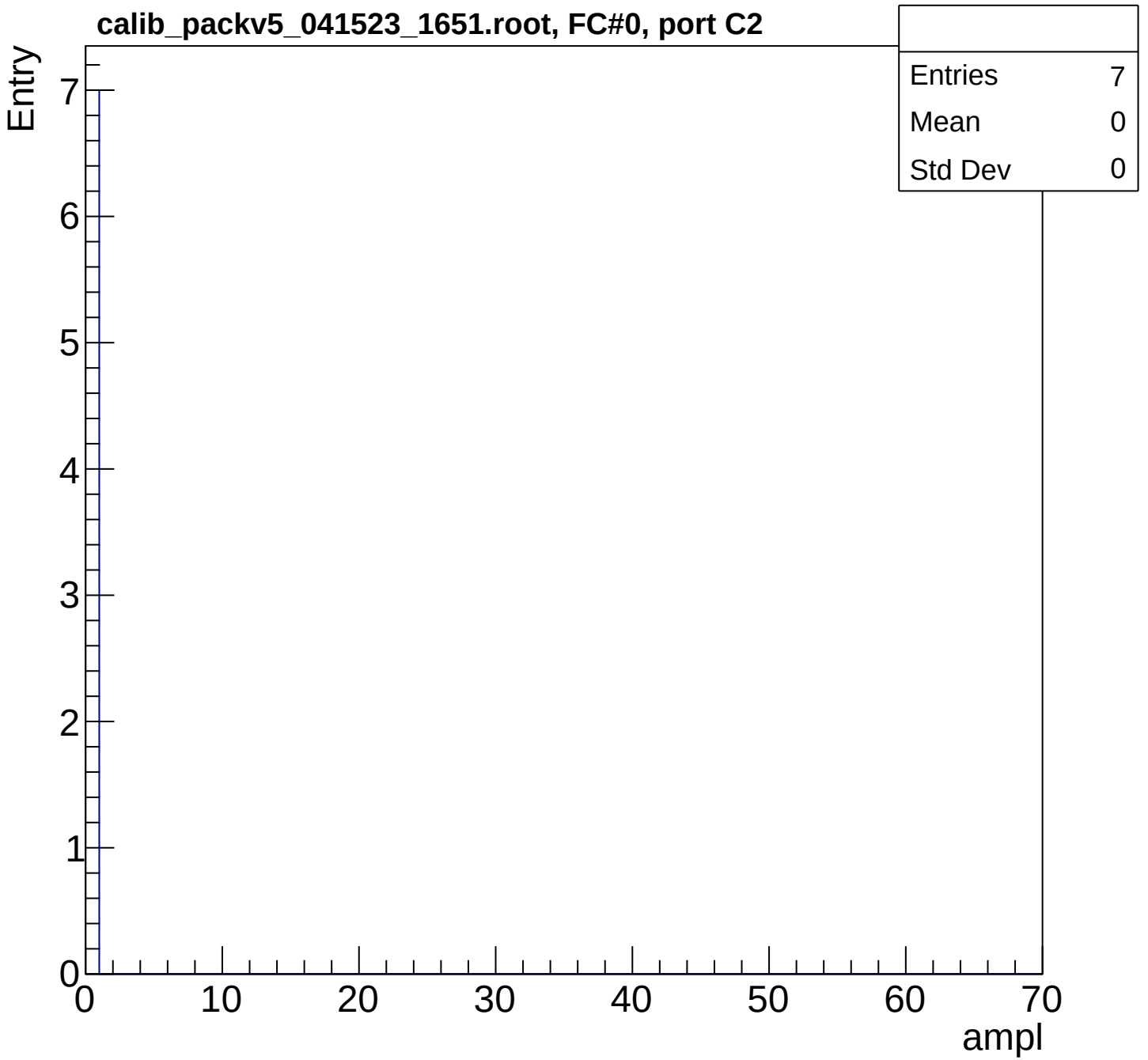
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

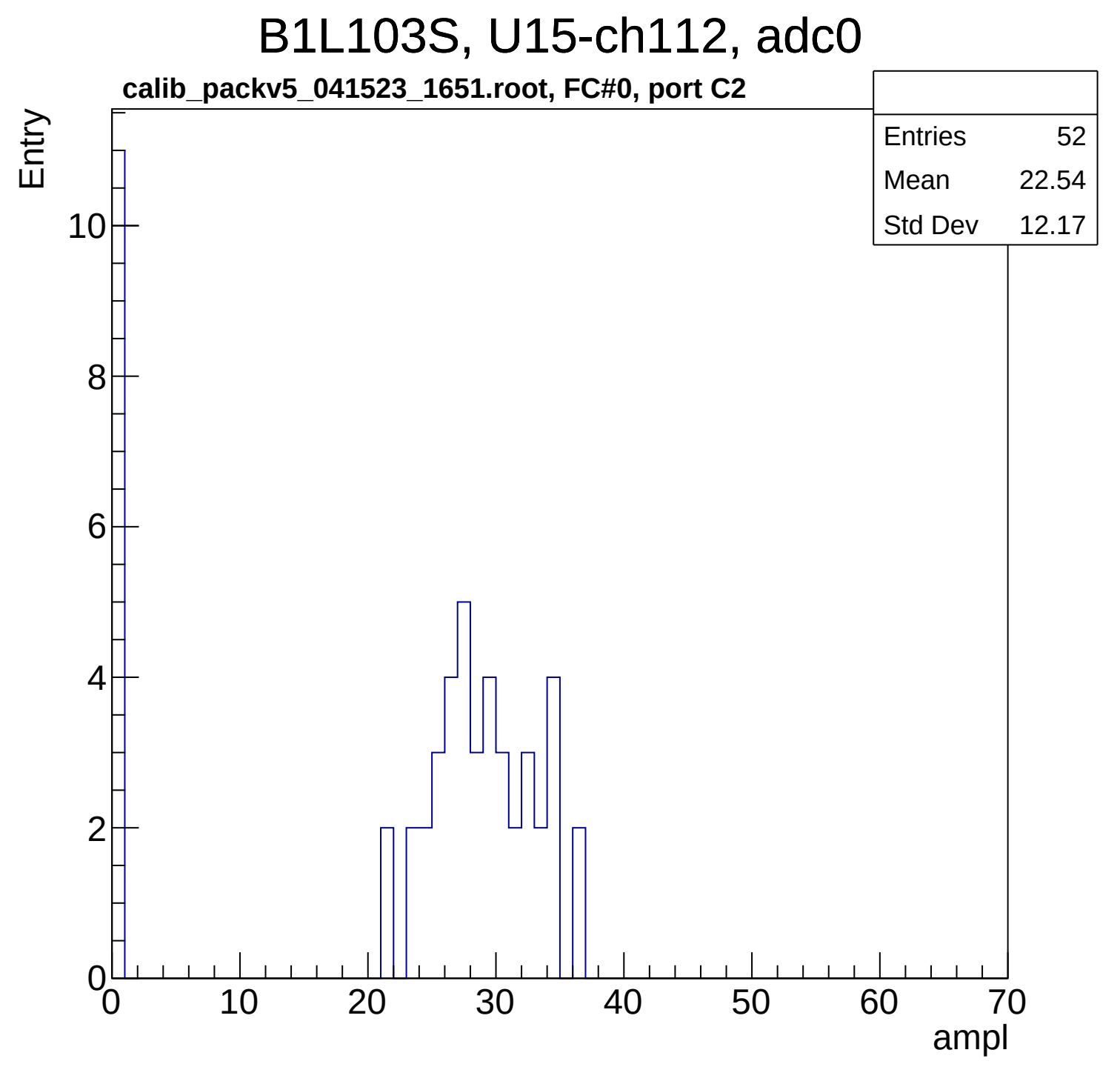

B1L103S, U15-ch111, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 41.55
Std Dev 16.23
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

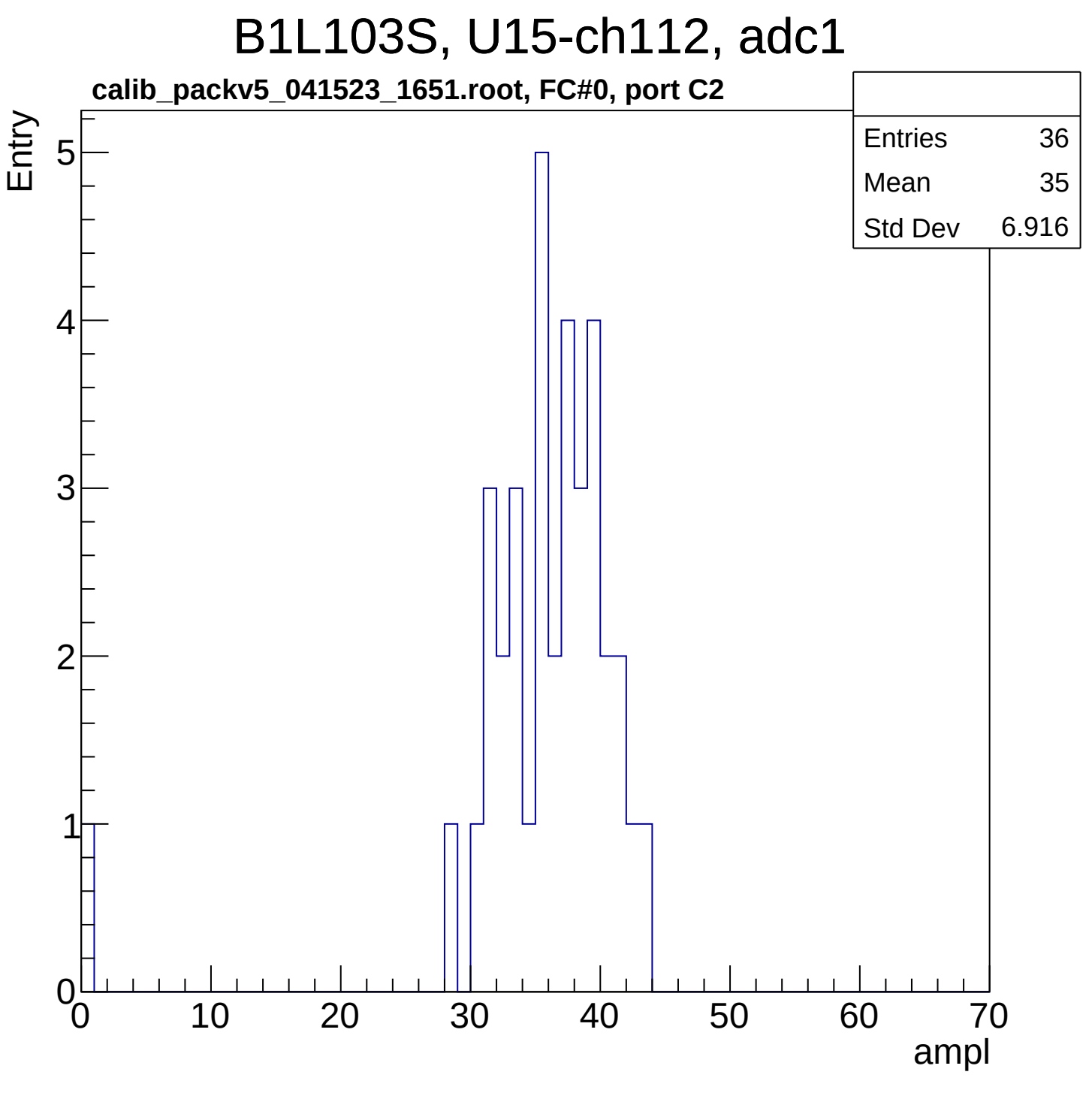

B1L103S, U15-ch111, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 53.73
Std Dev 3.422
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

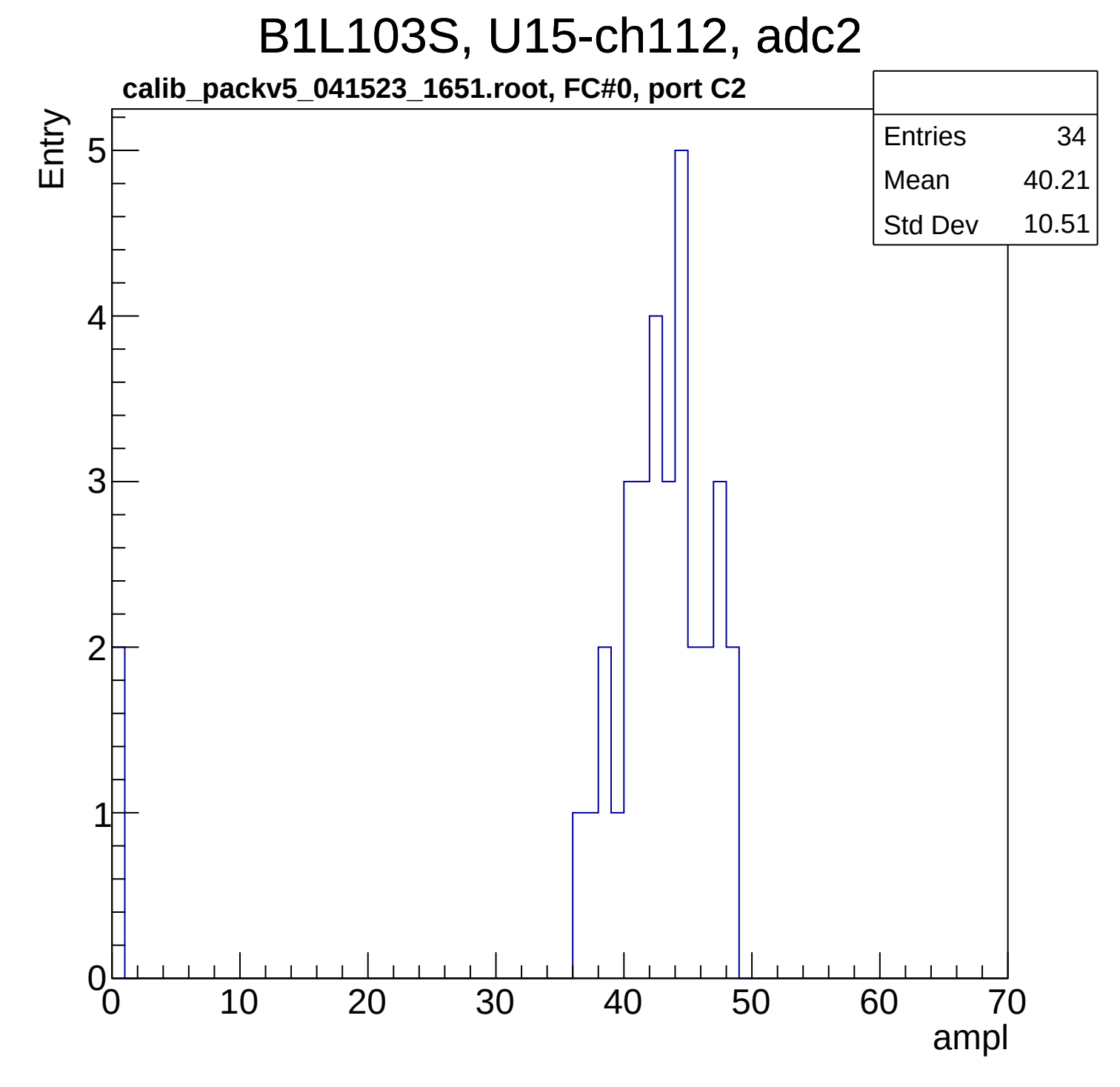

B1L103S, U15-ch111, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 57.35
Std Dev 10.82
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

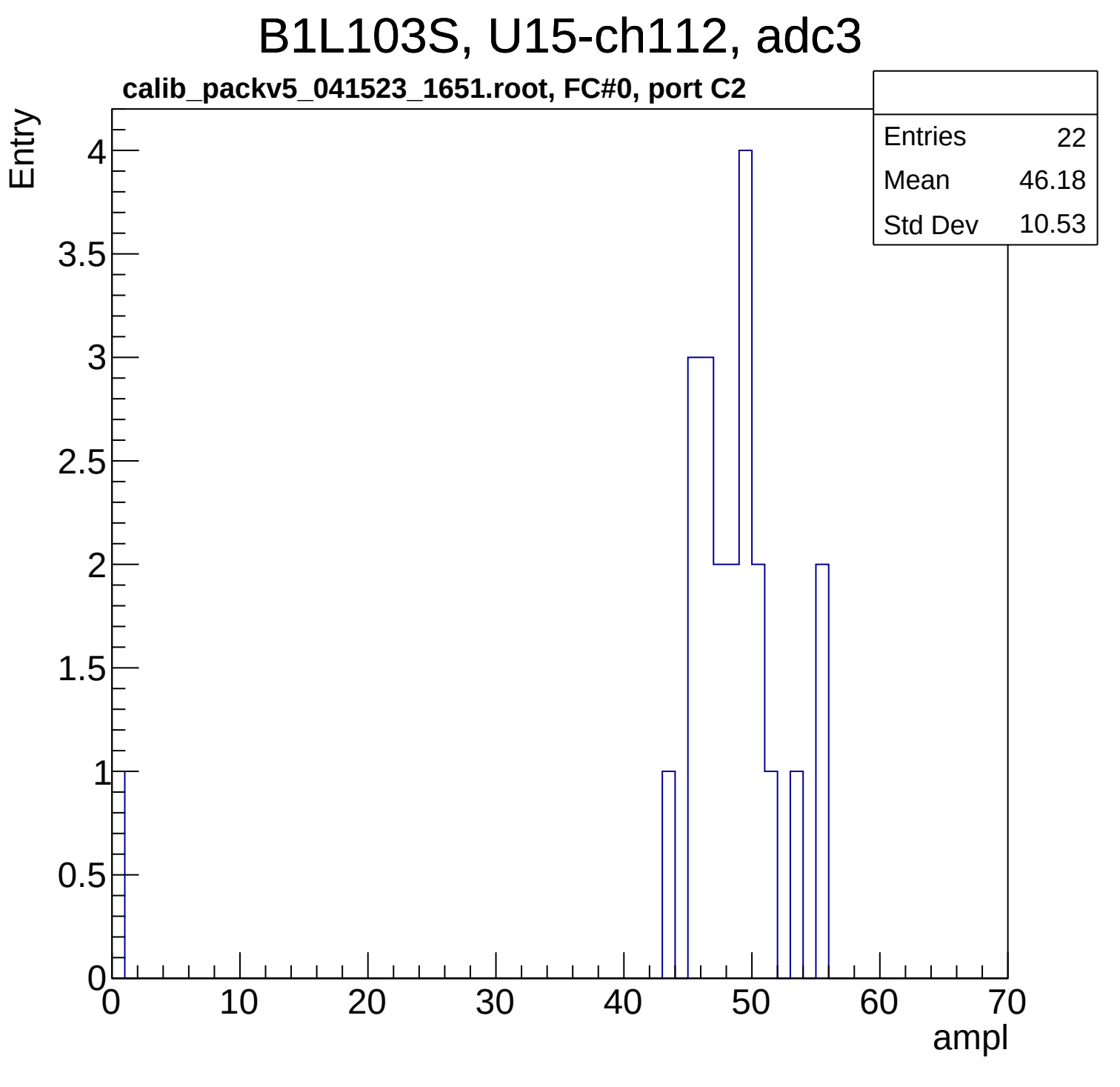

B1L103S, U15-ch111, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

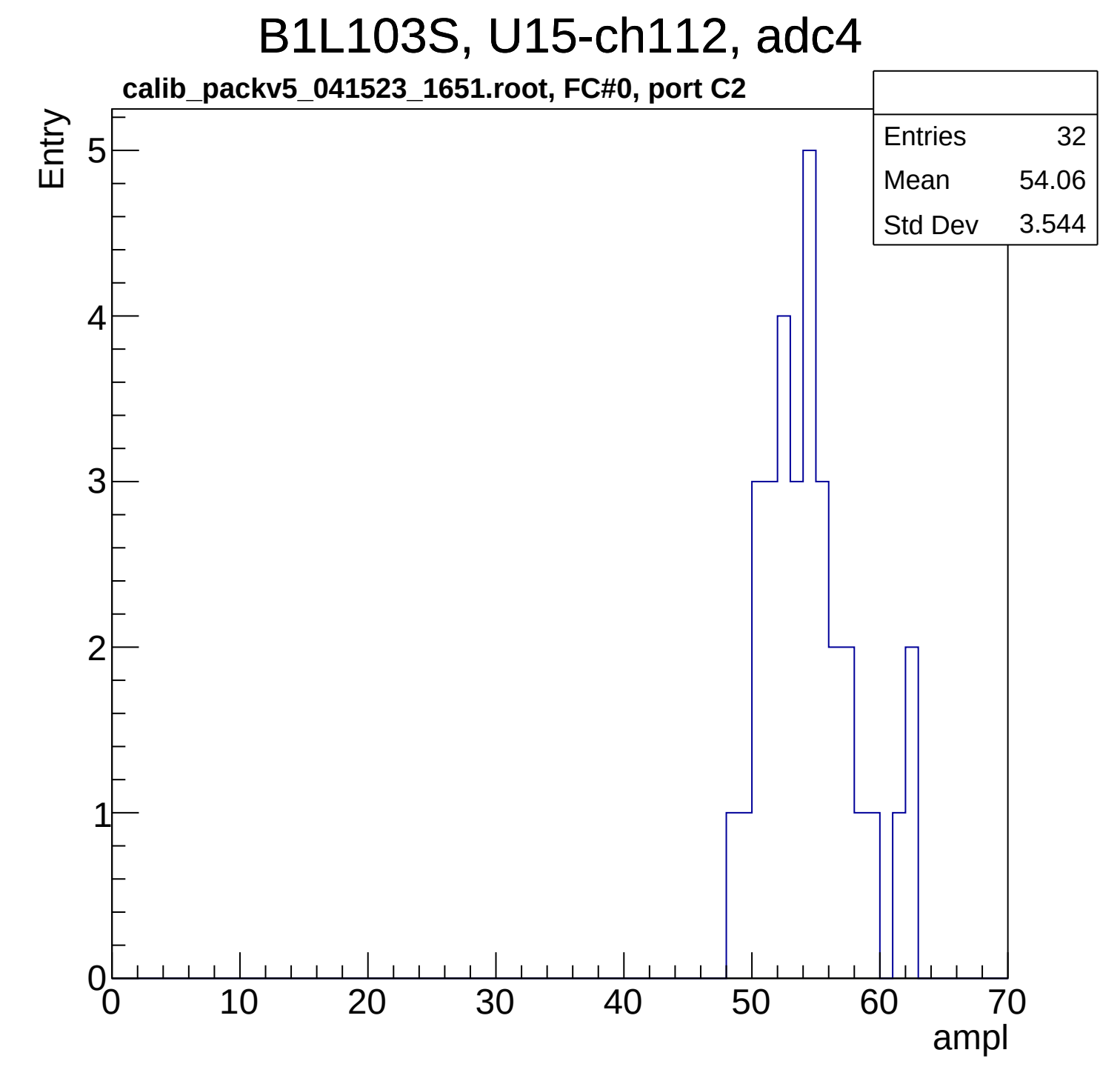

B1L103S, U15-ch111, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 0
Std Dev 0
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

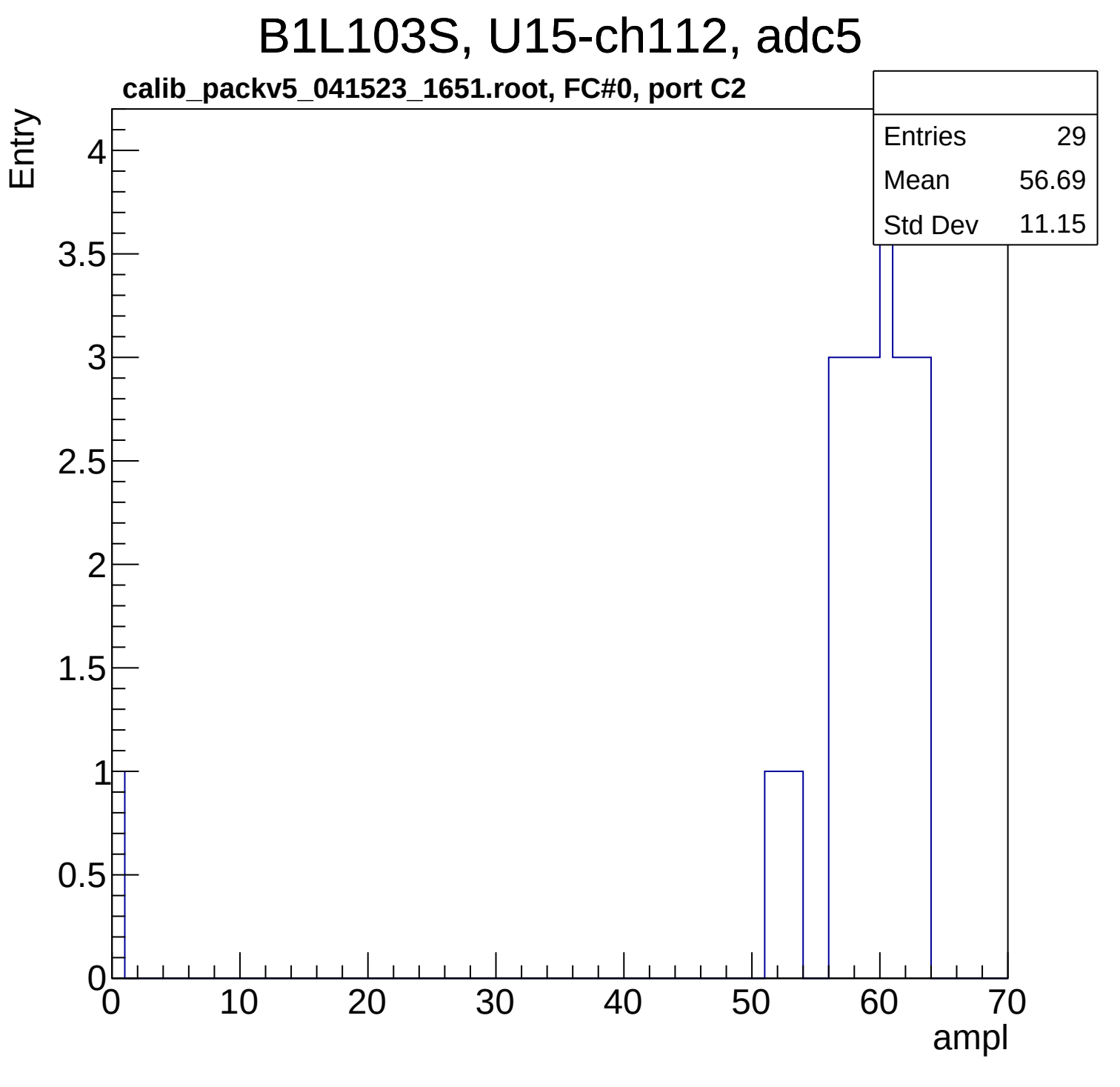

B1L103S, U15-ch112, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 22.54
Std Dev 12.17
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

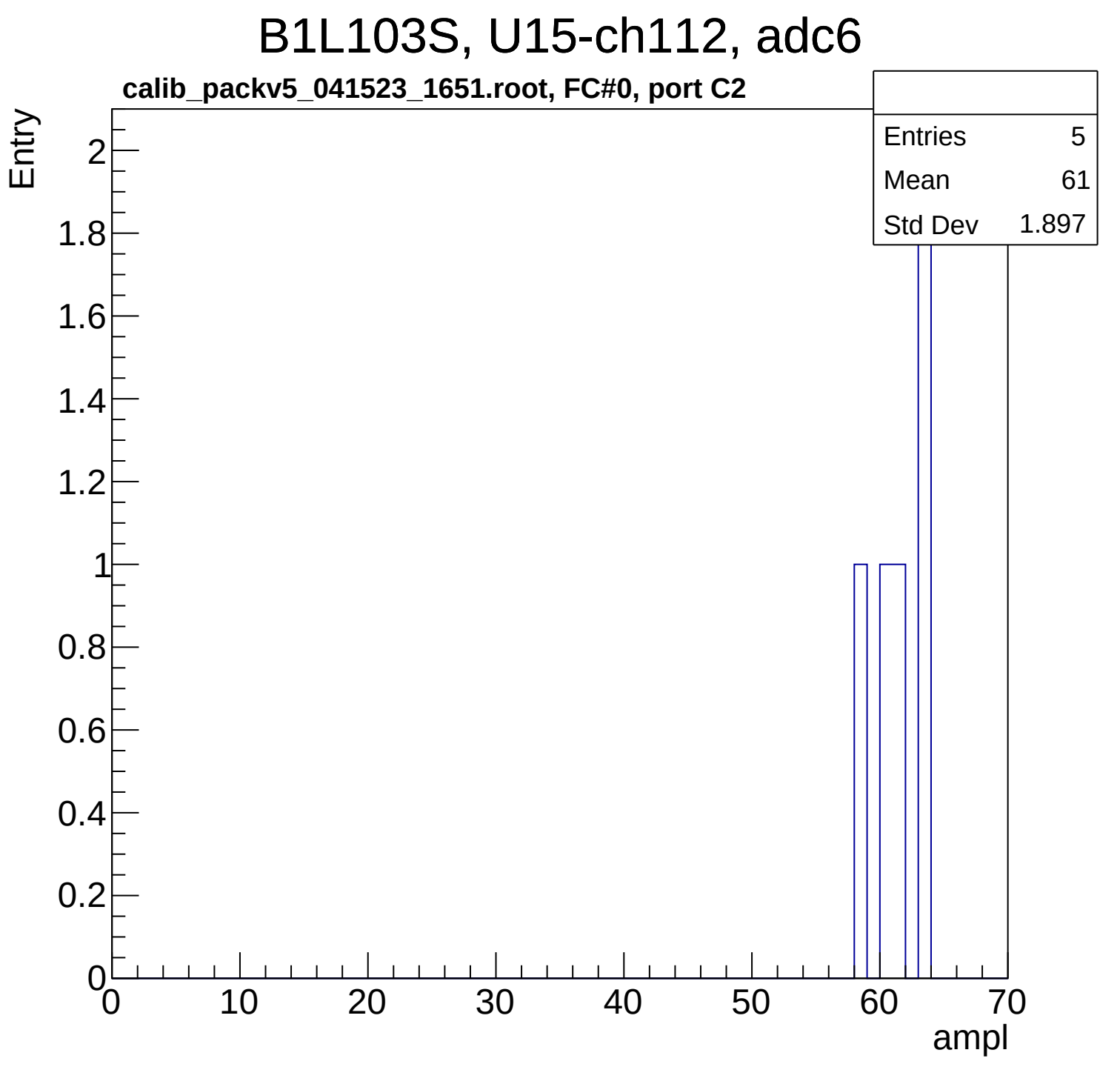

B1L103S, U15-ch112, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 35
Std Dev 6.916
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

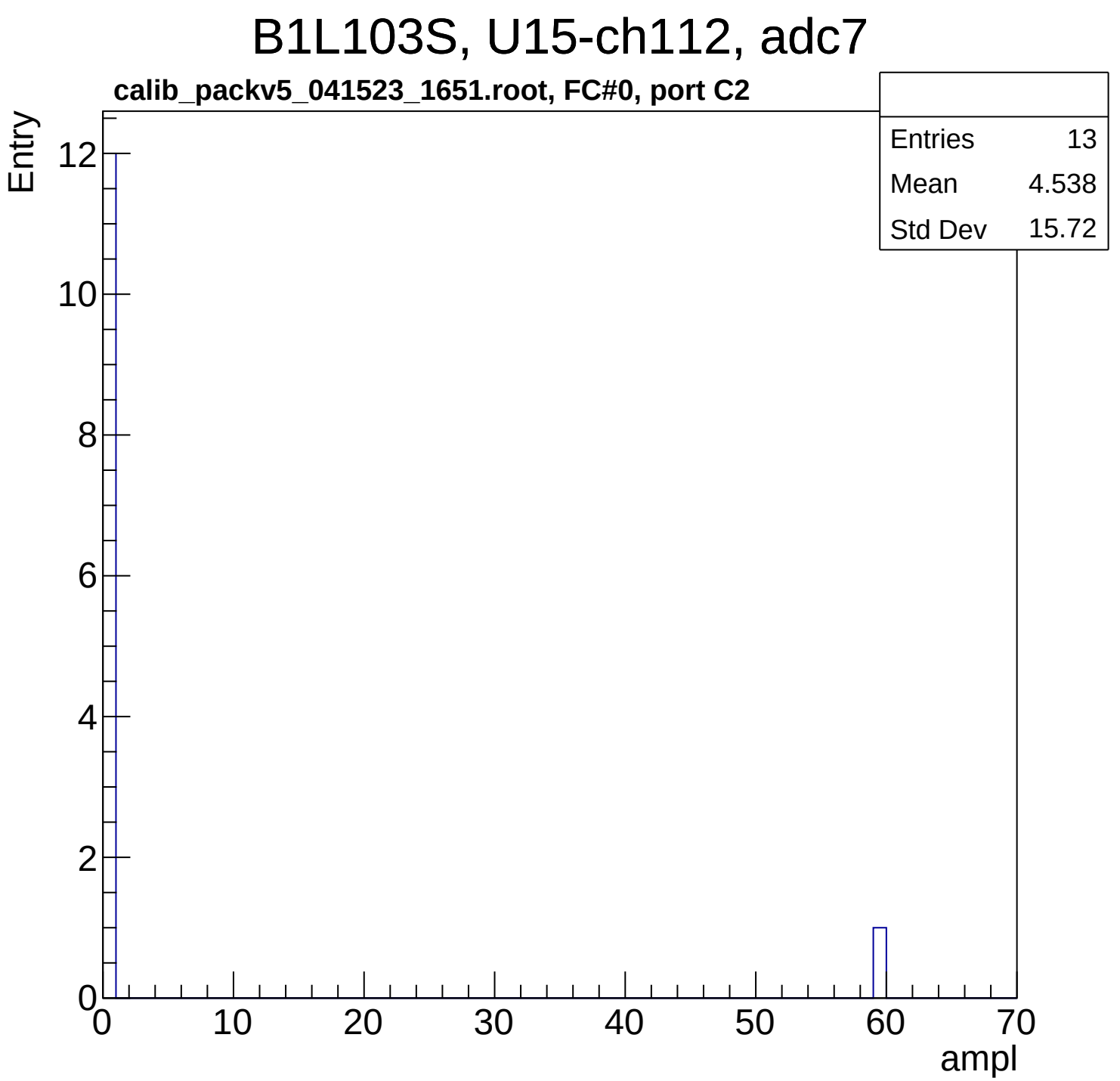

B1L103S, U15-ch112, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 40.21
Std Dev 10.51
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

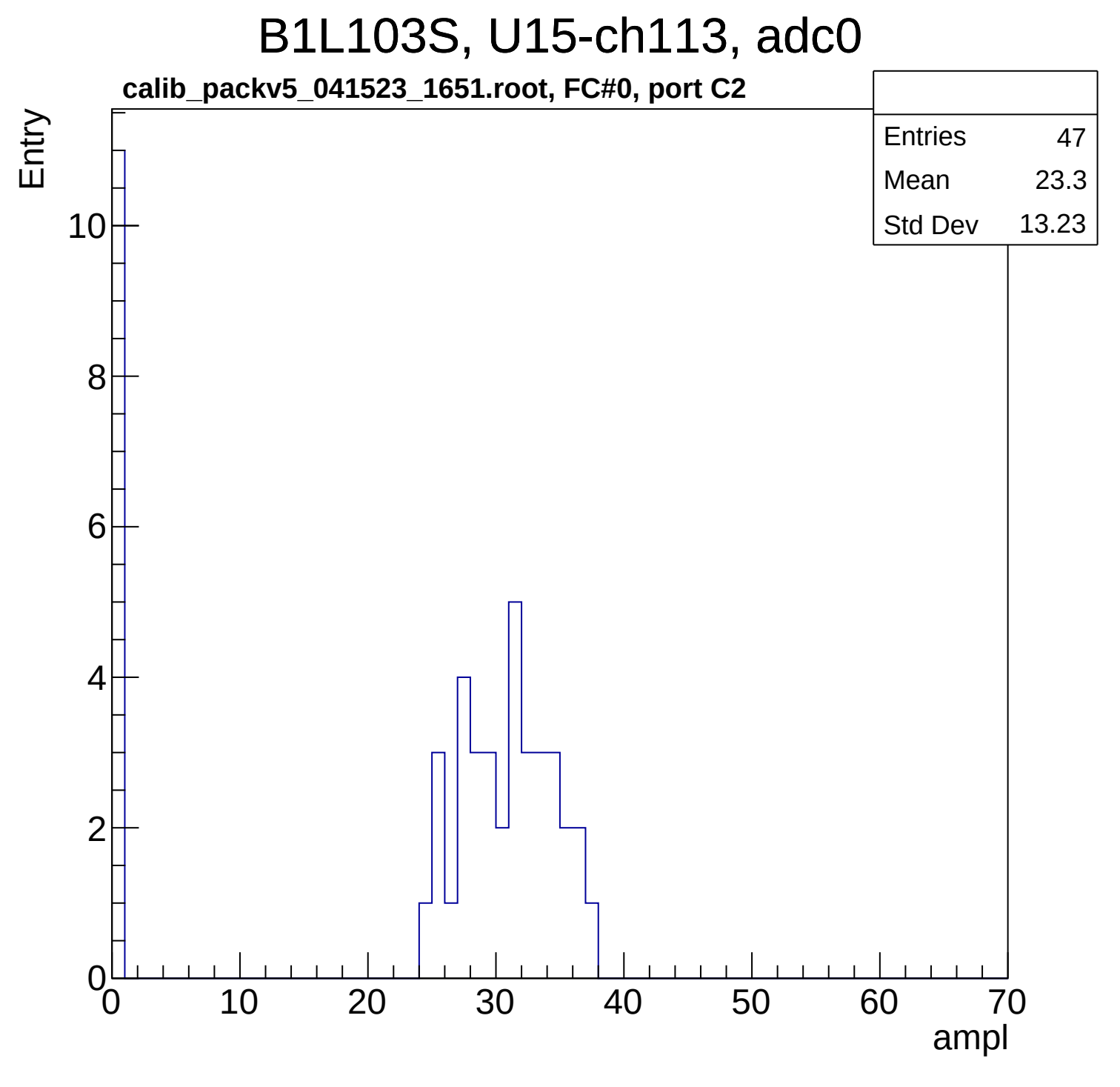

B1L103S, U15-ch112, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 46.18
Std Dev 10.53
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

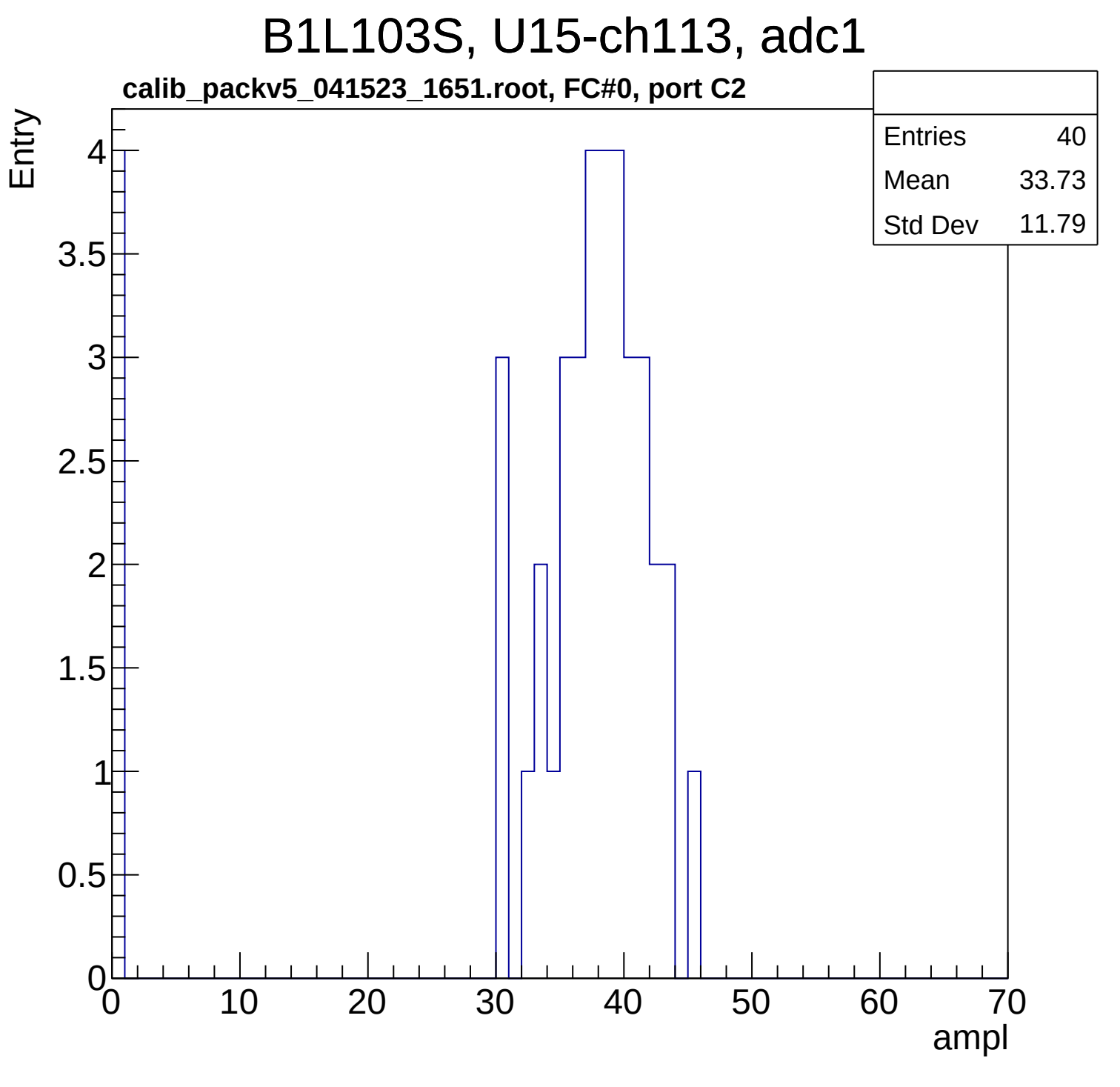

B1L103S, U15-ch112, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 54.06
Std Dev 3.544
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

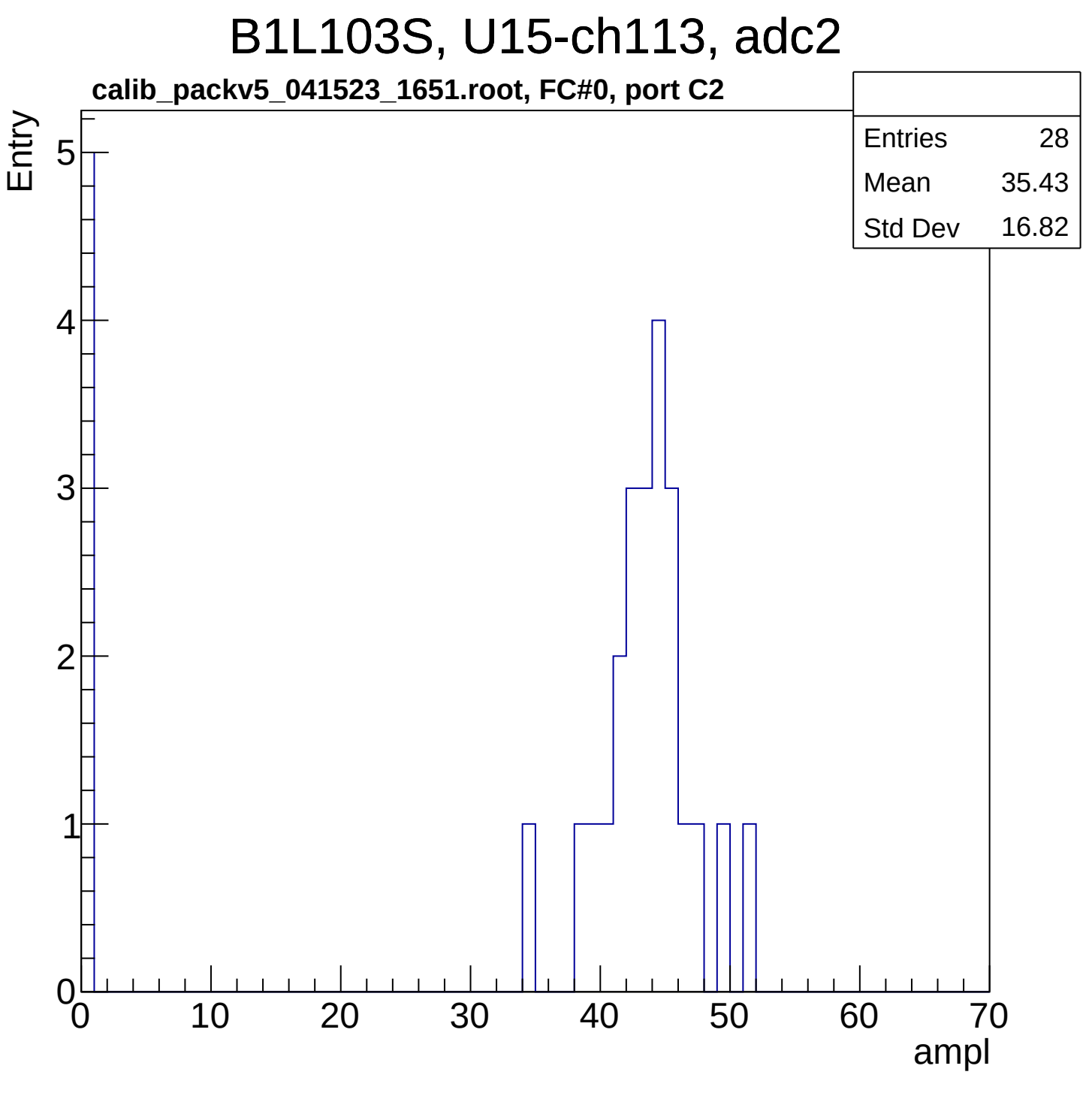

B1L103S, U15-ch112, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 56.69
Std Dev 11.15
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

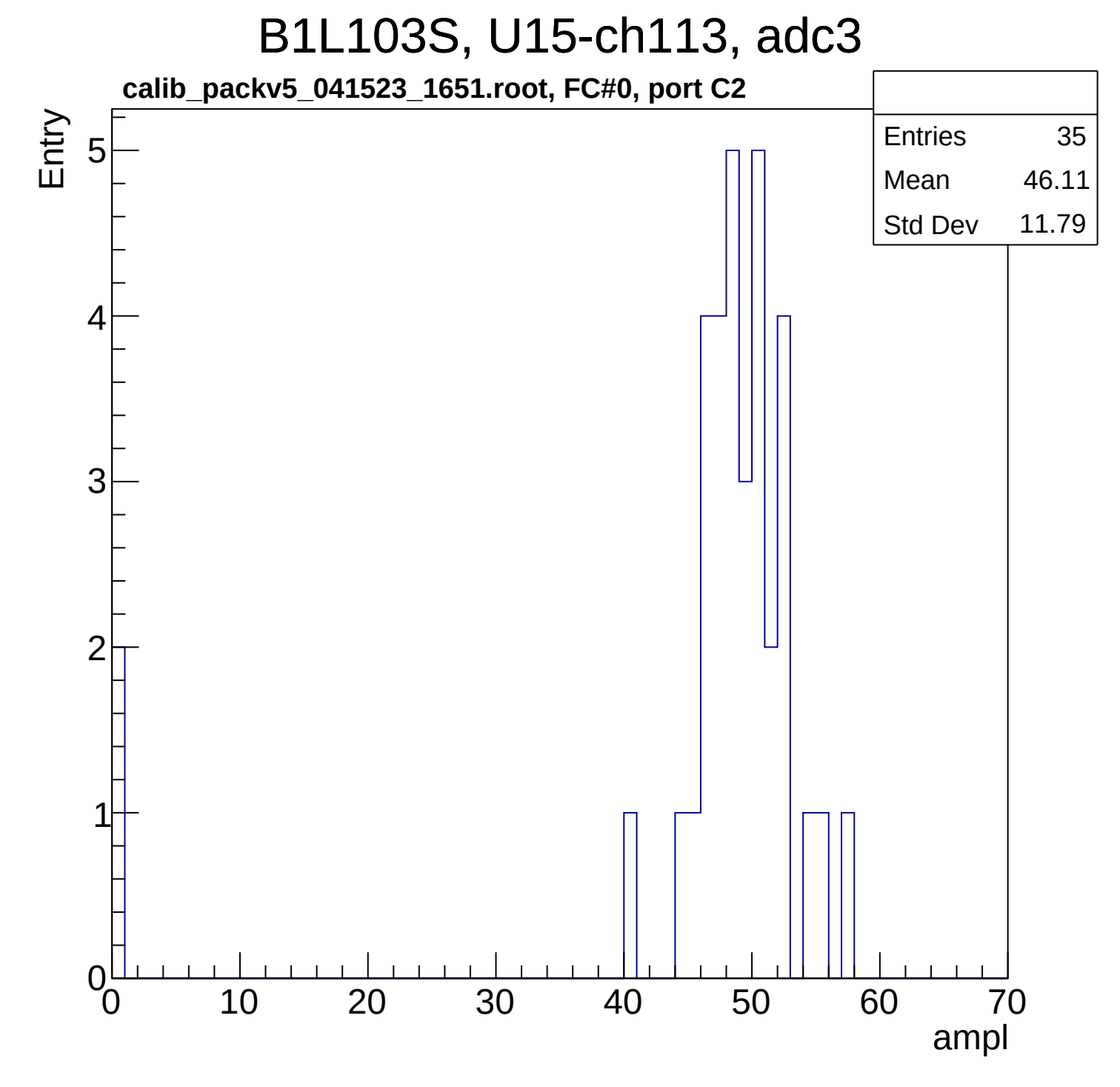

B1L103S, U15-ch112, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61
Std Dev 1.897
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

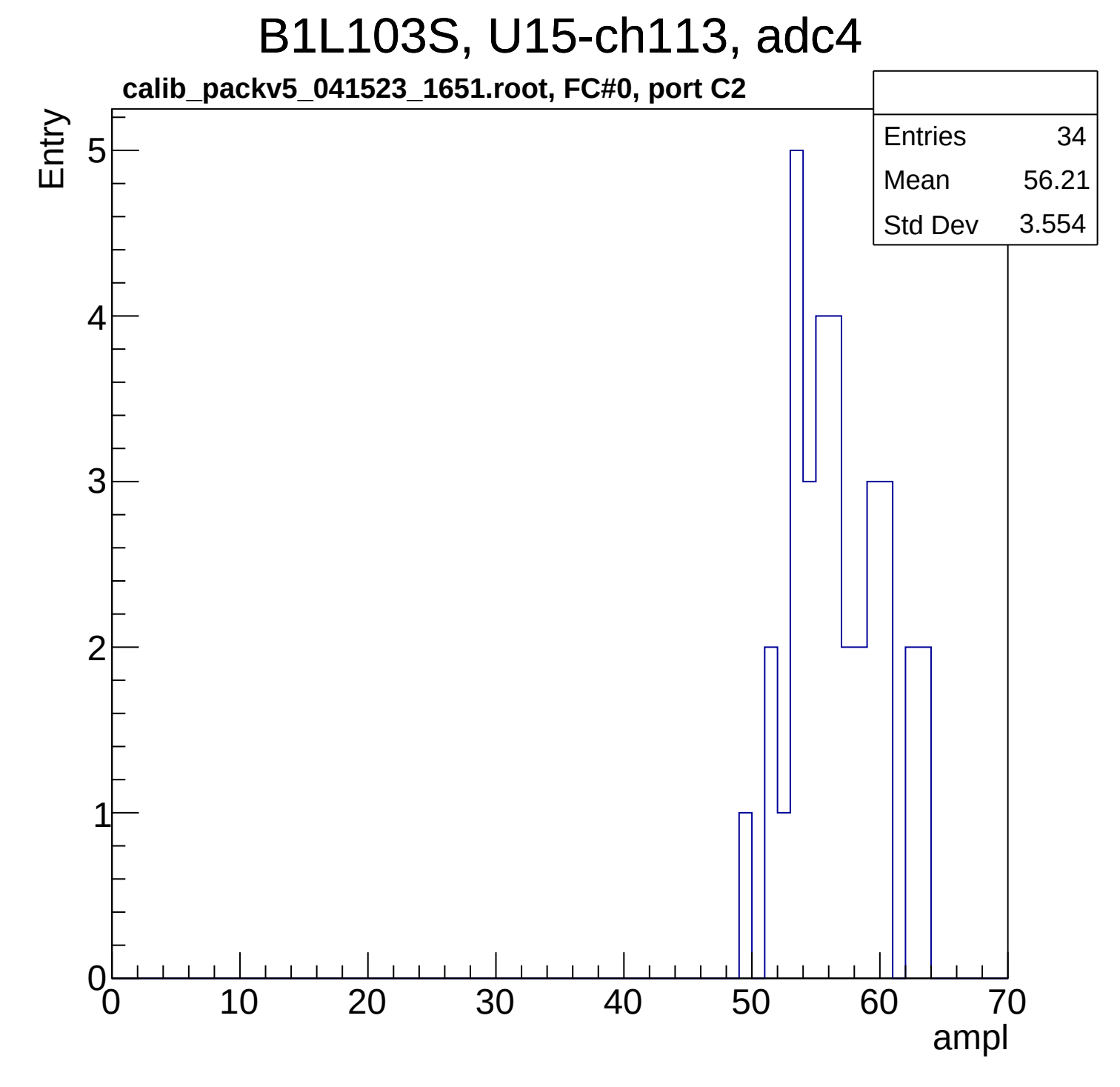

B1L103S, U15-ch112, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 4.538
Std Dev 15.72
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

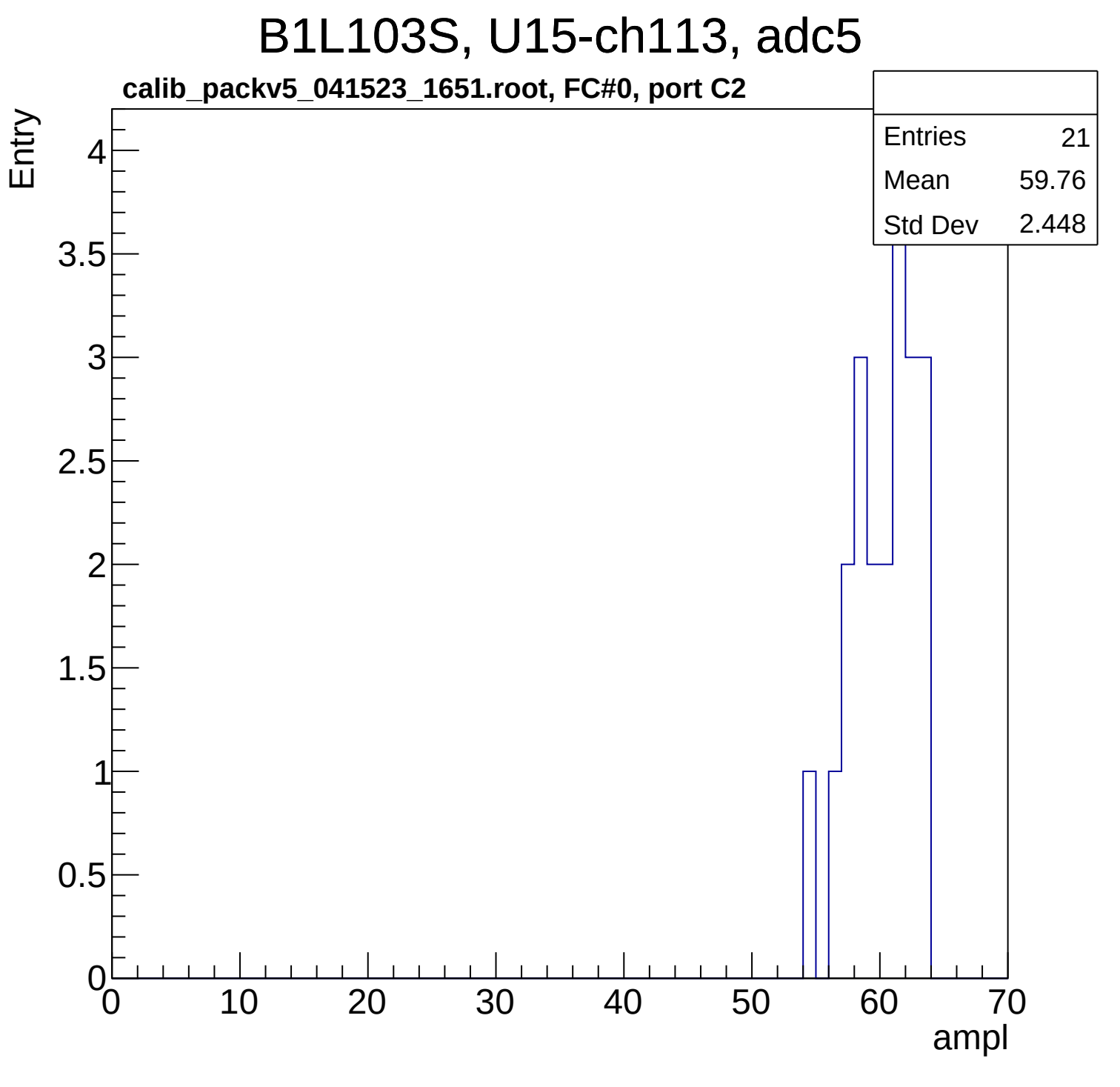

B1L103S, U15-ch113, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 23.3
Std Dev 13.23
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

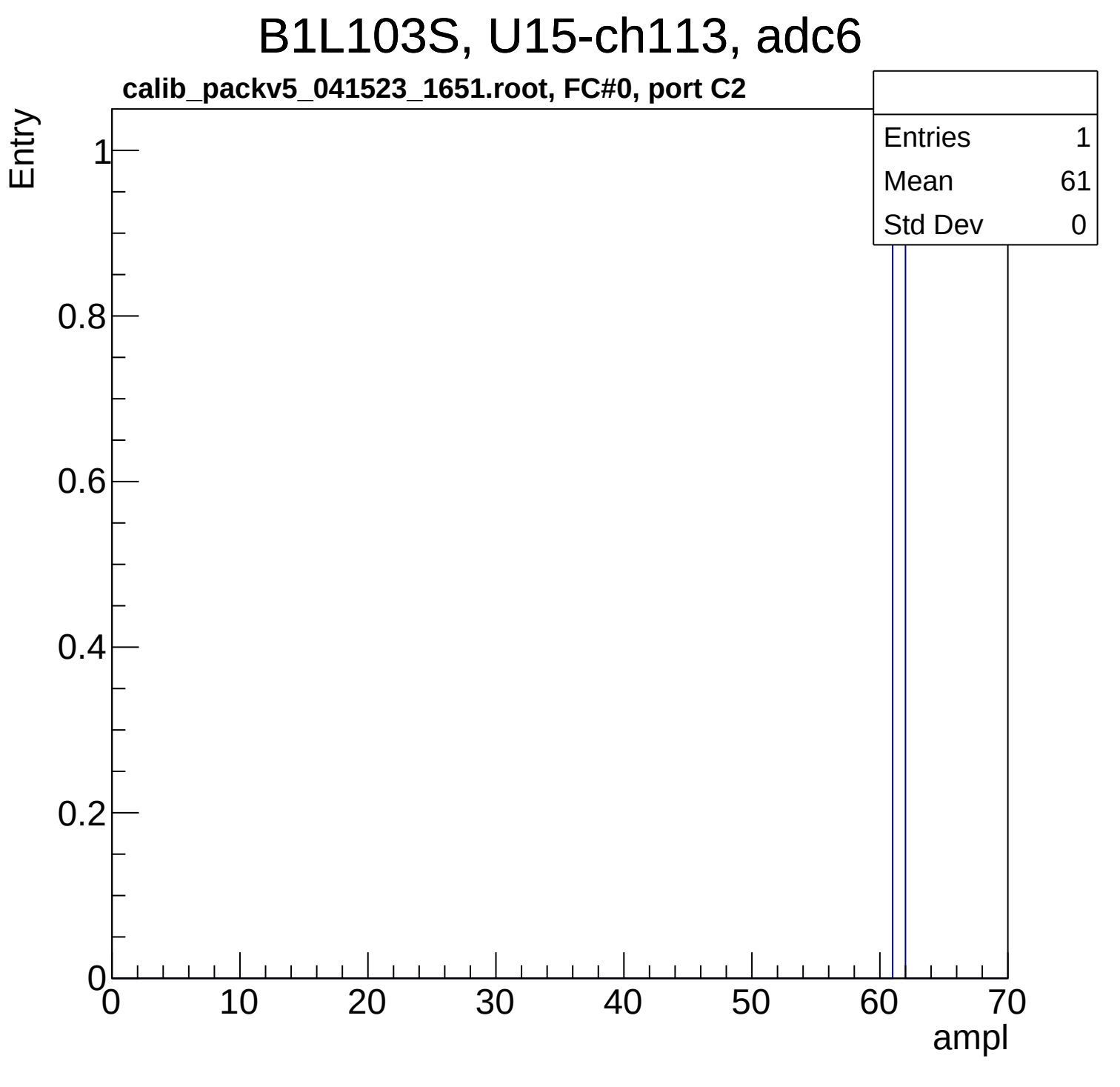

B1L103S, U15-ch113, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 33.73
Std Dev 11.79
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

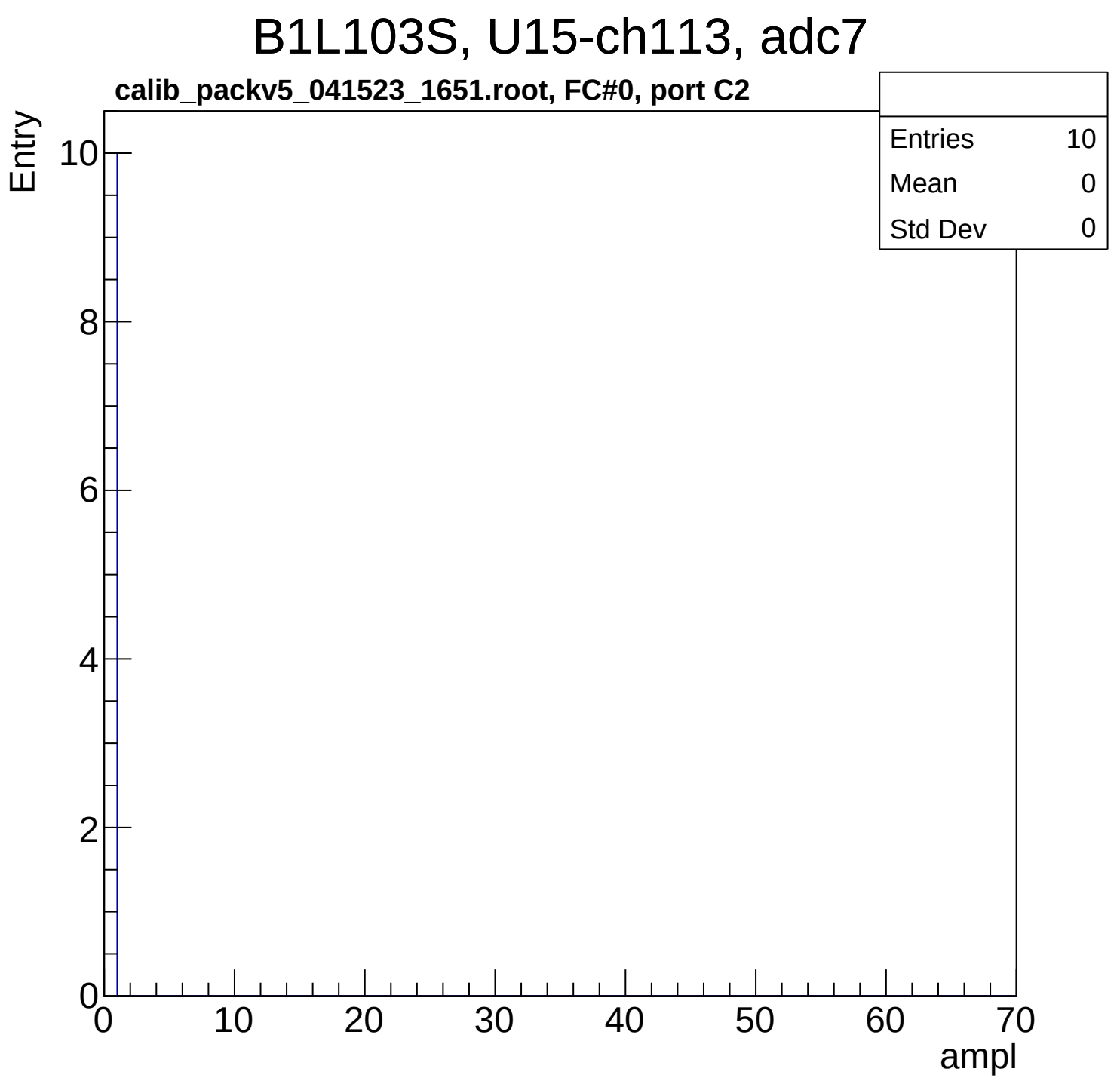

B1L103S, U15-ch113, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 35.43
Std Dev 16.82
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

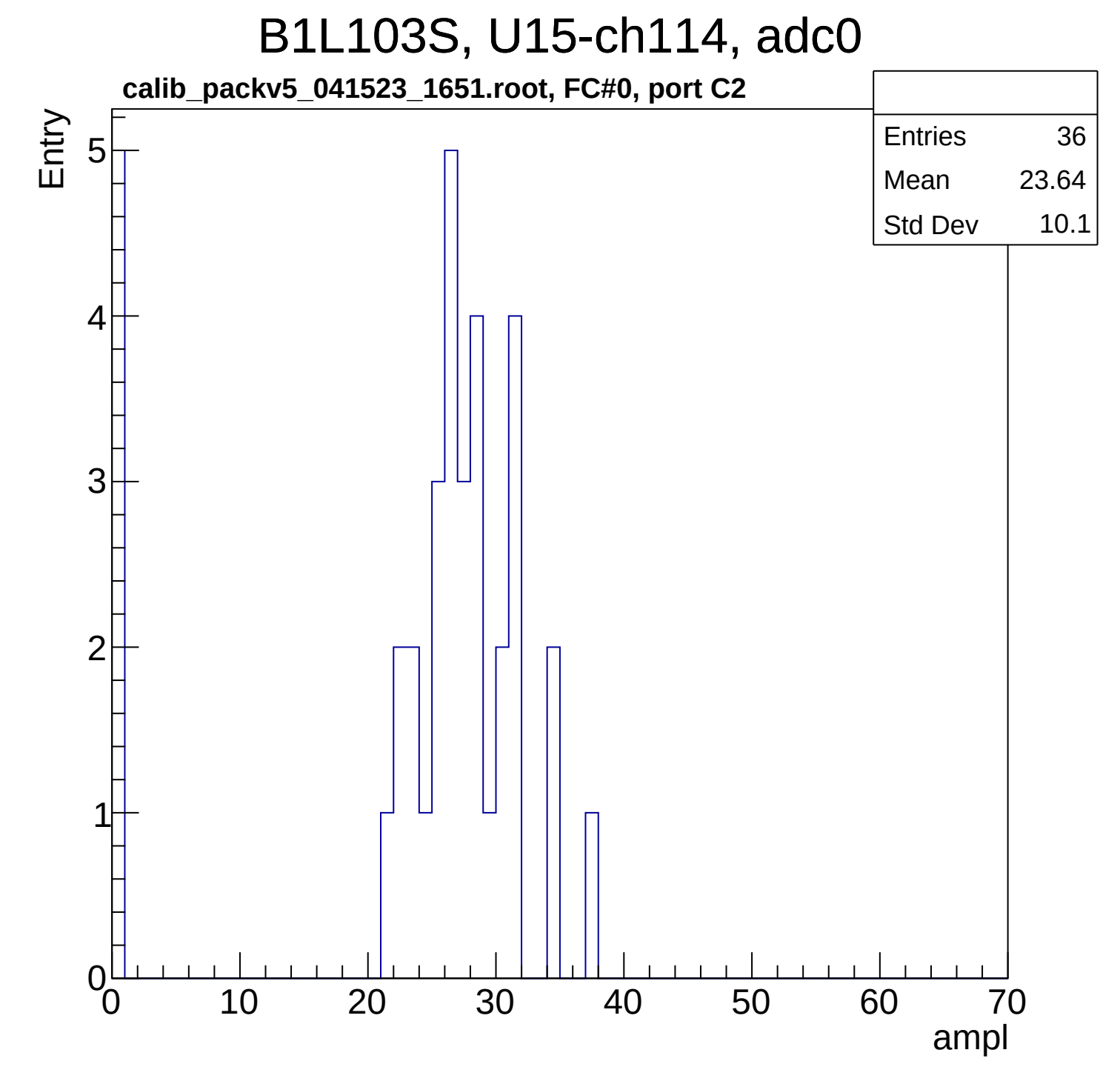

B1L103S, U15-ch113, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 46.11
Std Dev 11.79
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

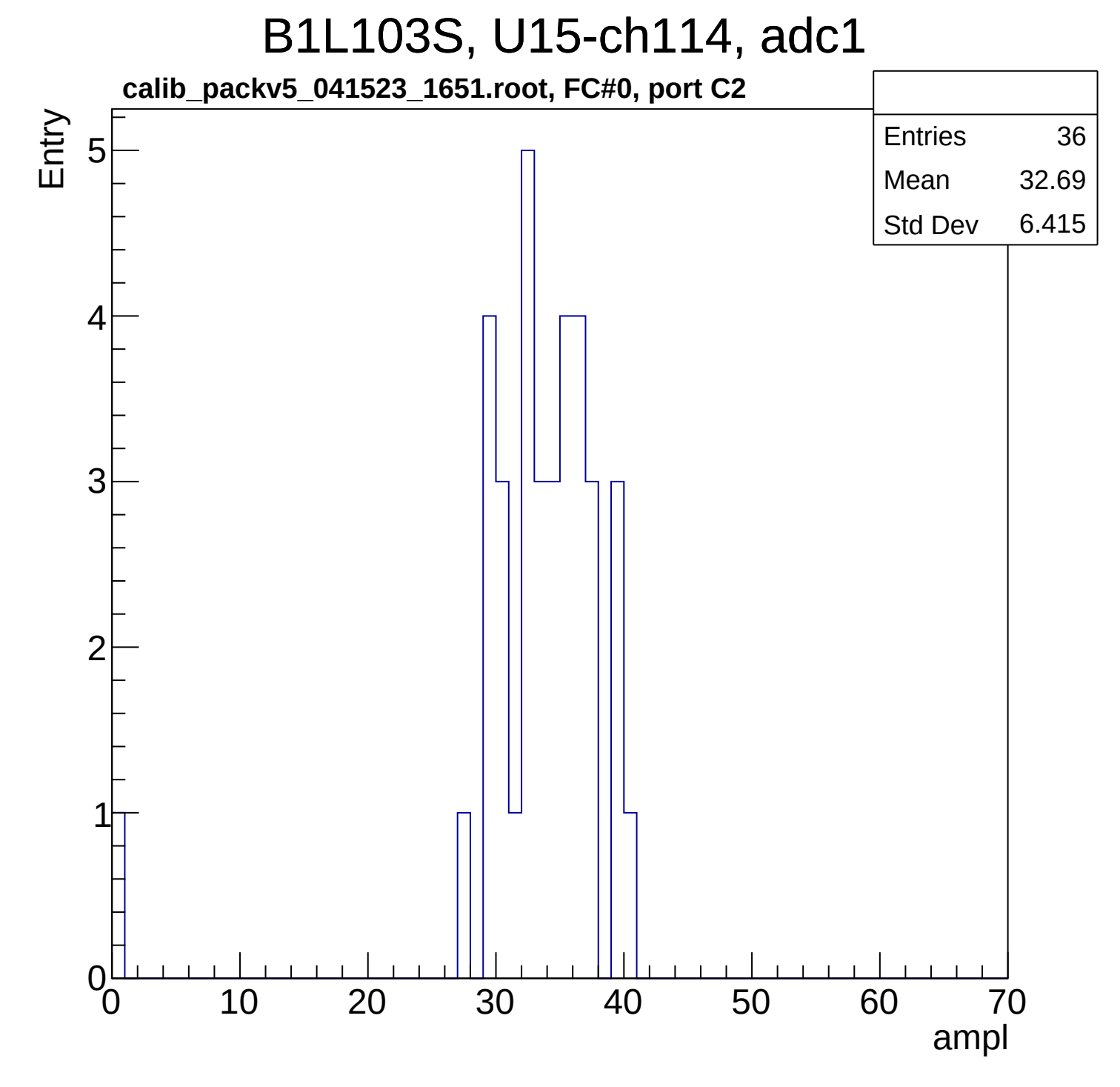

B1L103S, U15-ch113, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 56.21
Std Dev 3.554
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

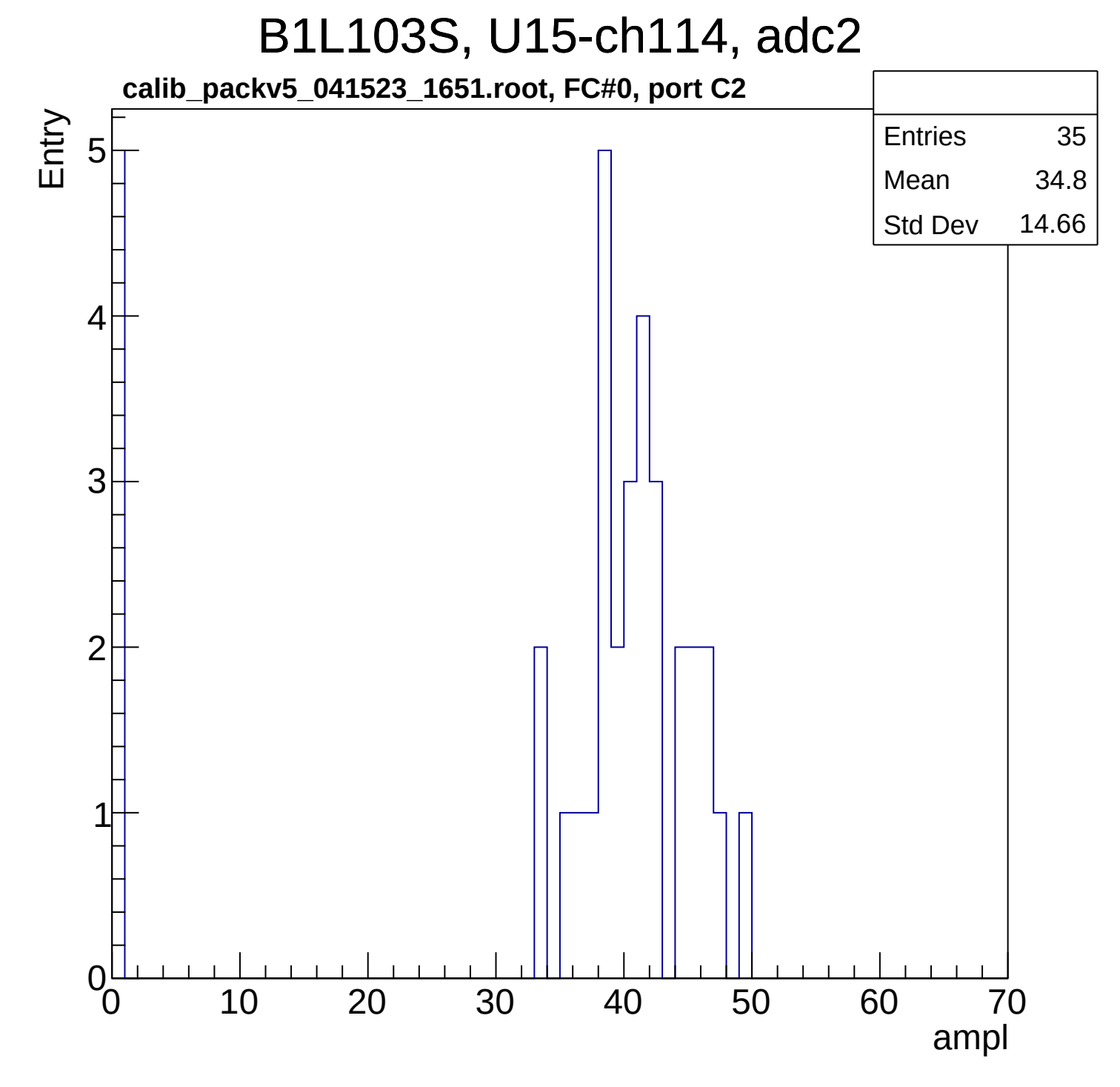

B1L103S, U15-ch113, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 59.76
Std Dev 2.448
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

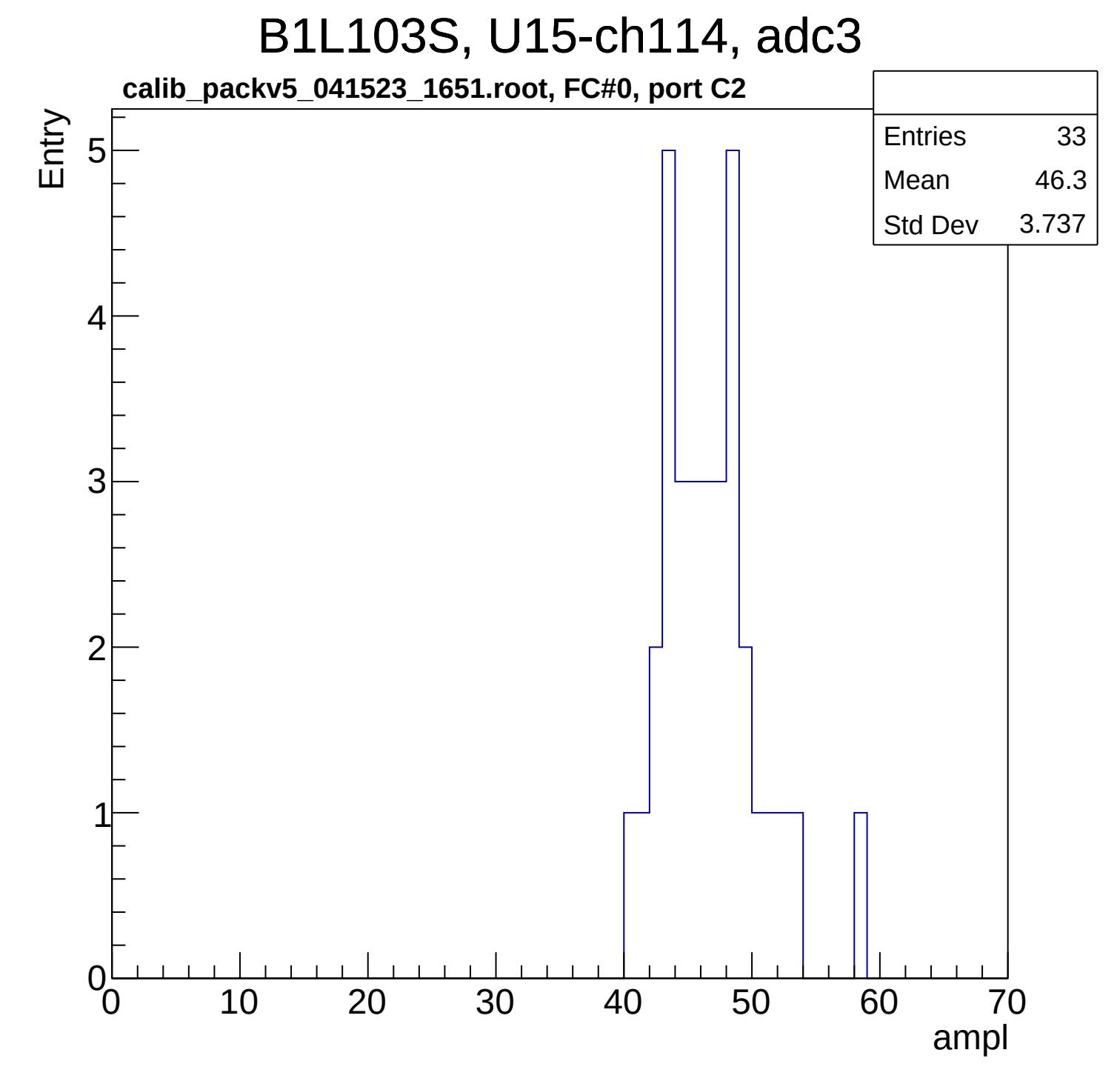

B1L103S, U15-ch113, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 61
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

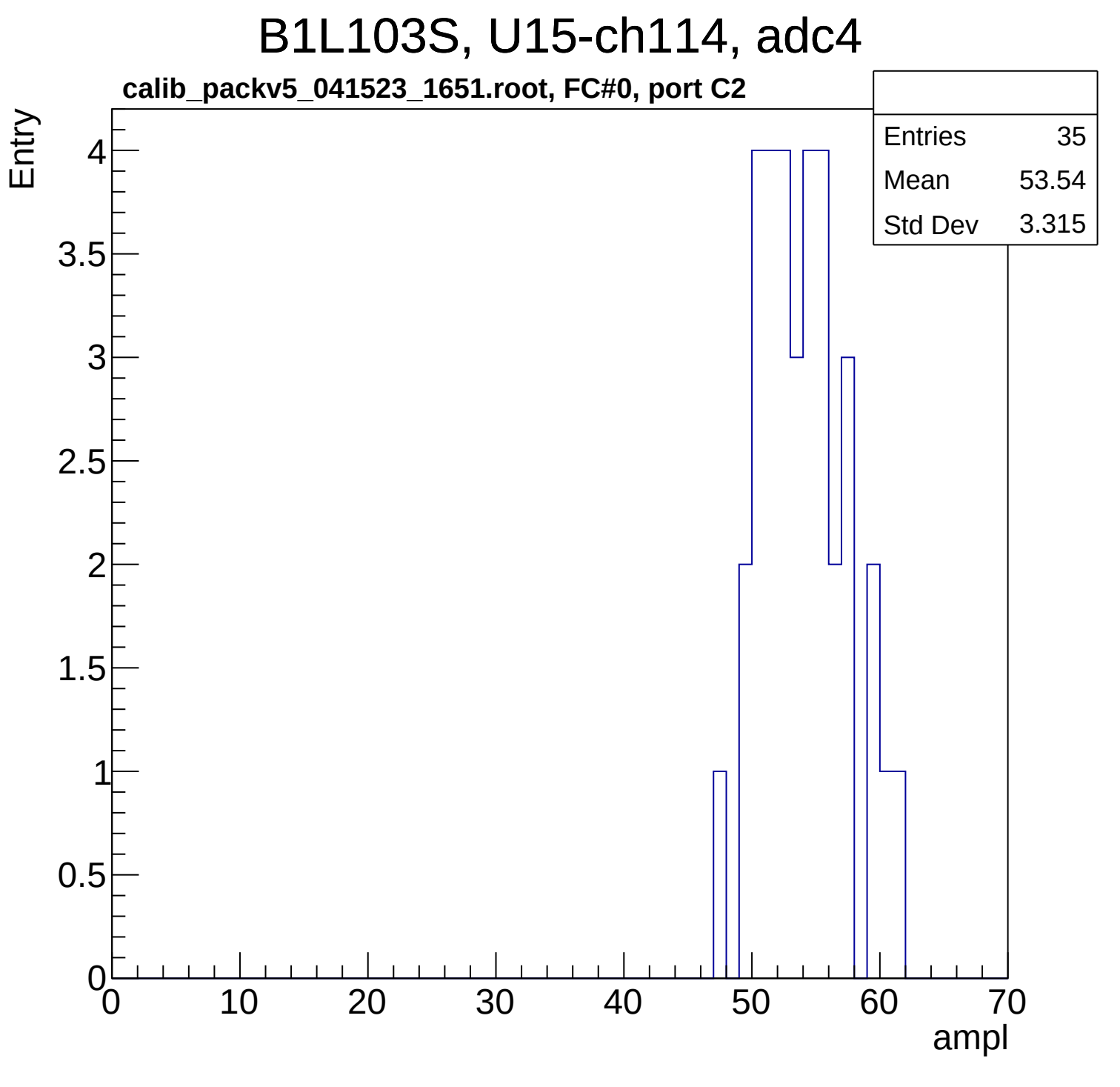

B1L103S, U15-ch113, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

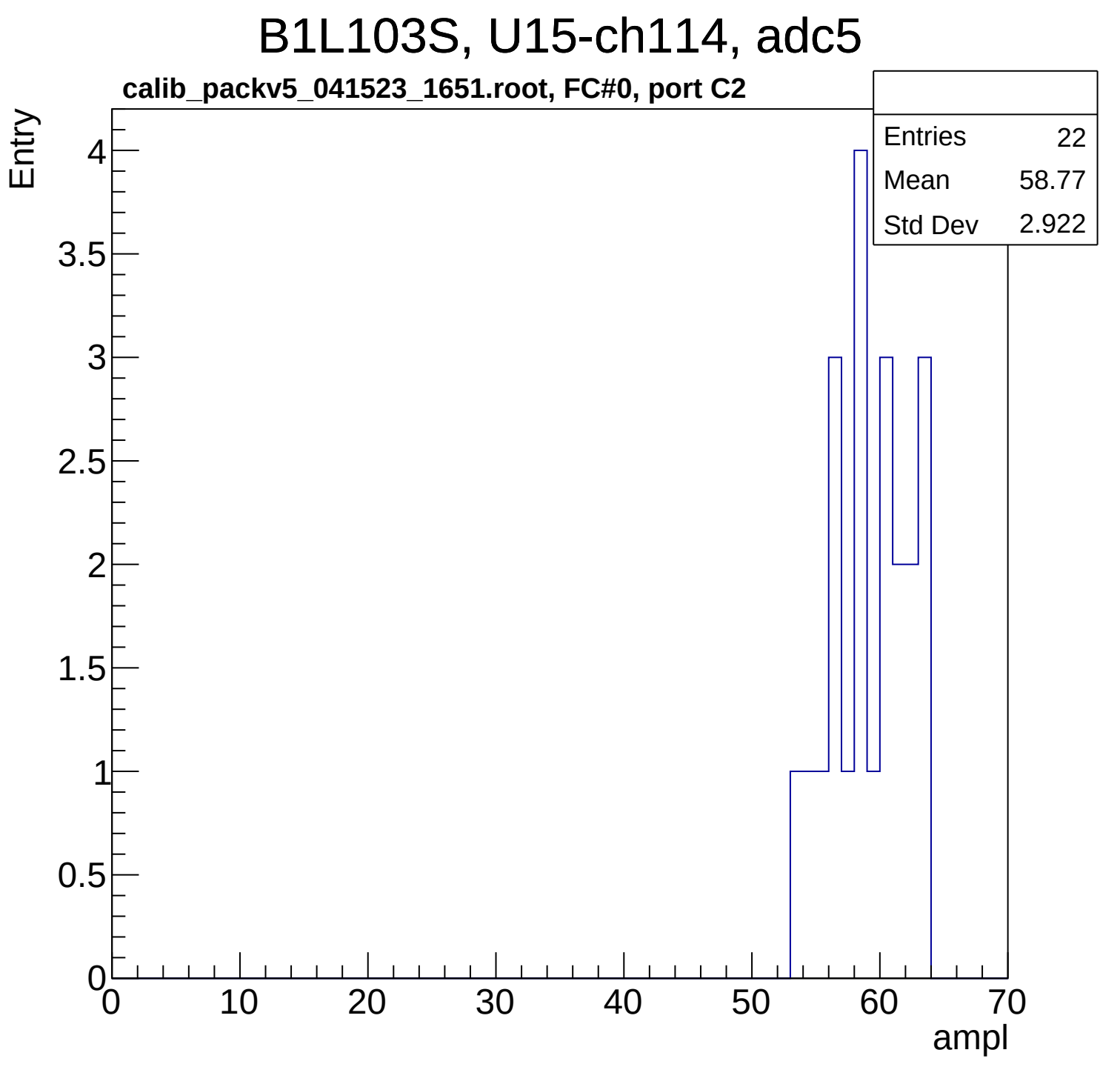

B1L103S, U15-ch114, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 23.64
Std Dev 10.1
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

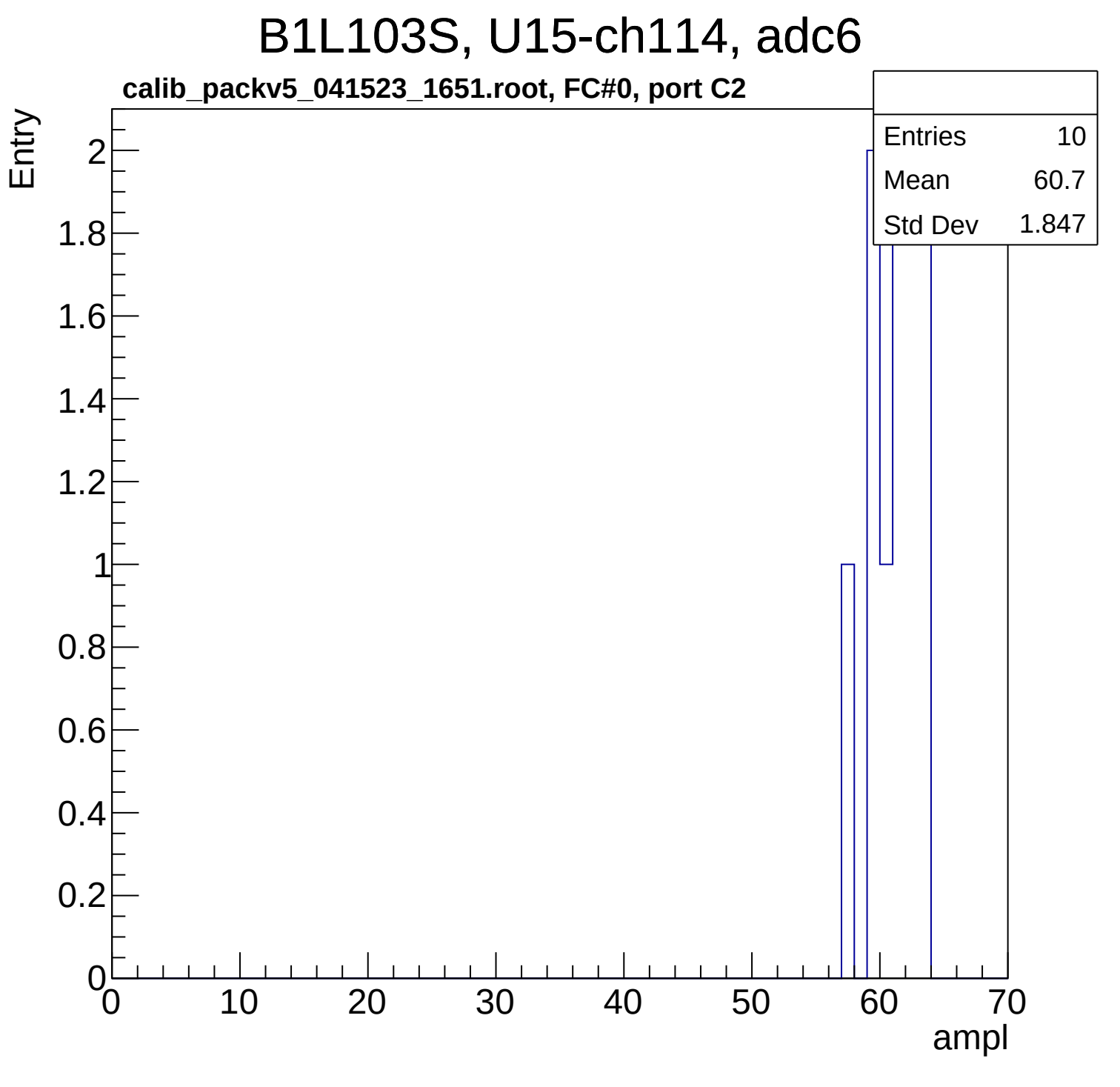

B1L103S, U15-ch114, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 32.69
Std Dev 6.415
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

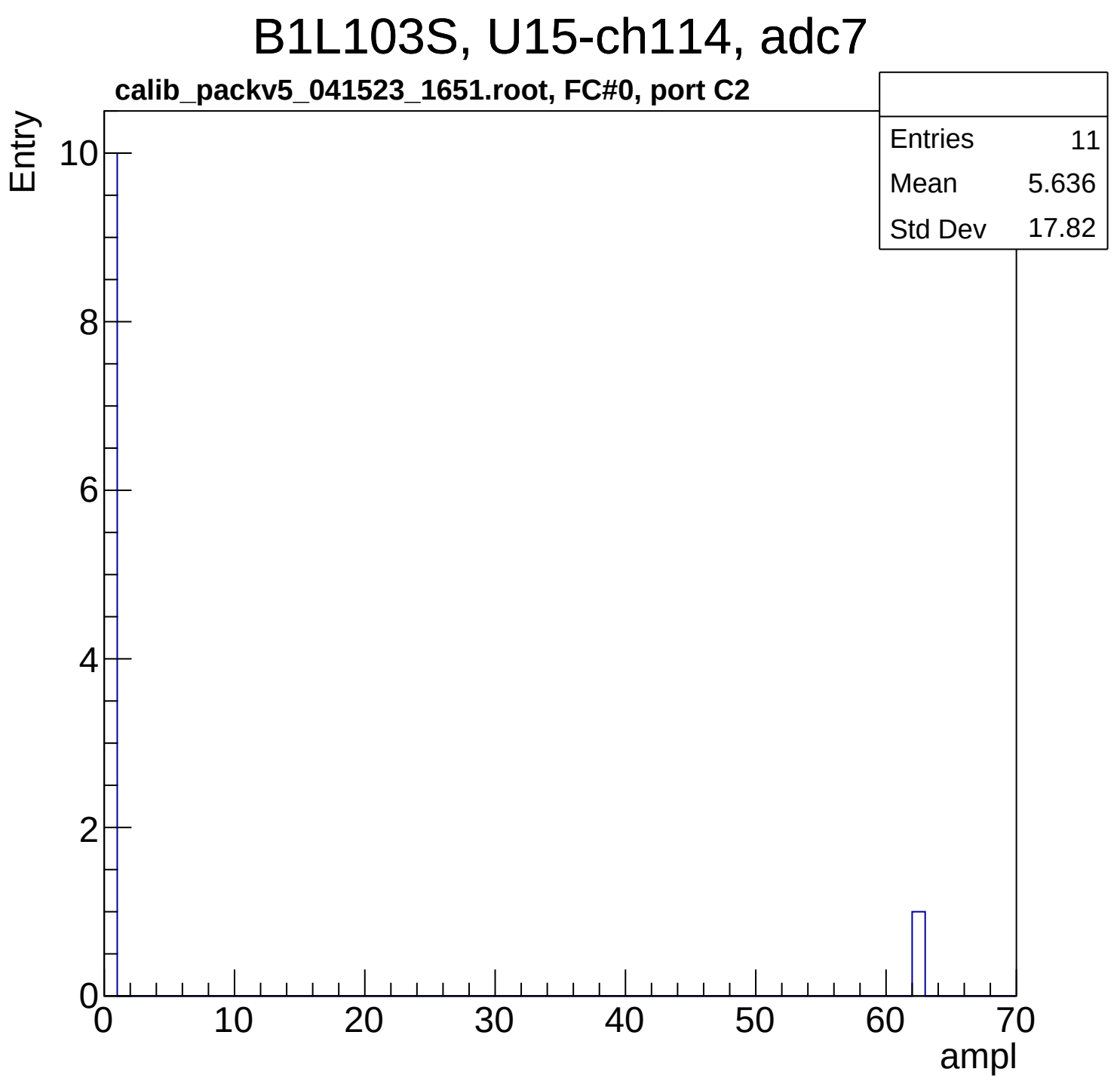

B1L103S, U15-ch114, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 34.8
Std Dev 14.66
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

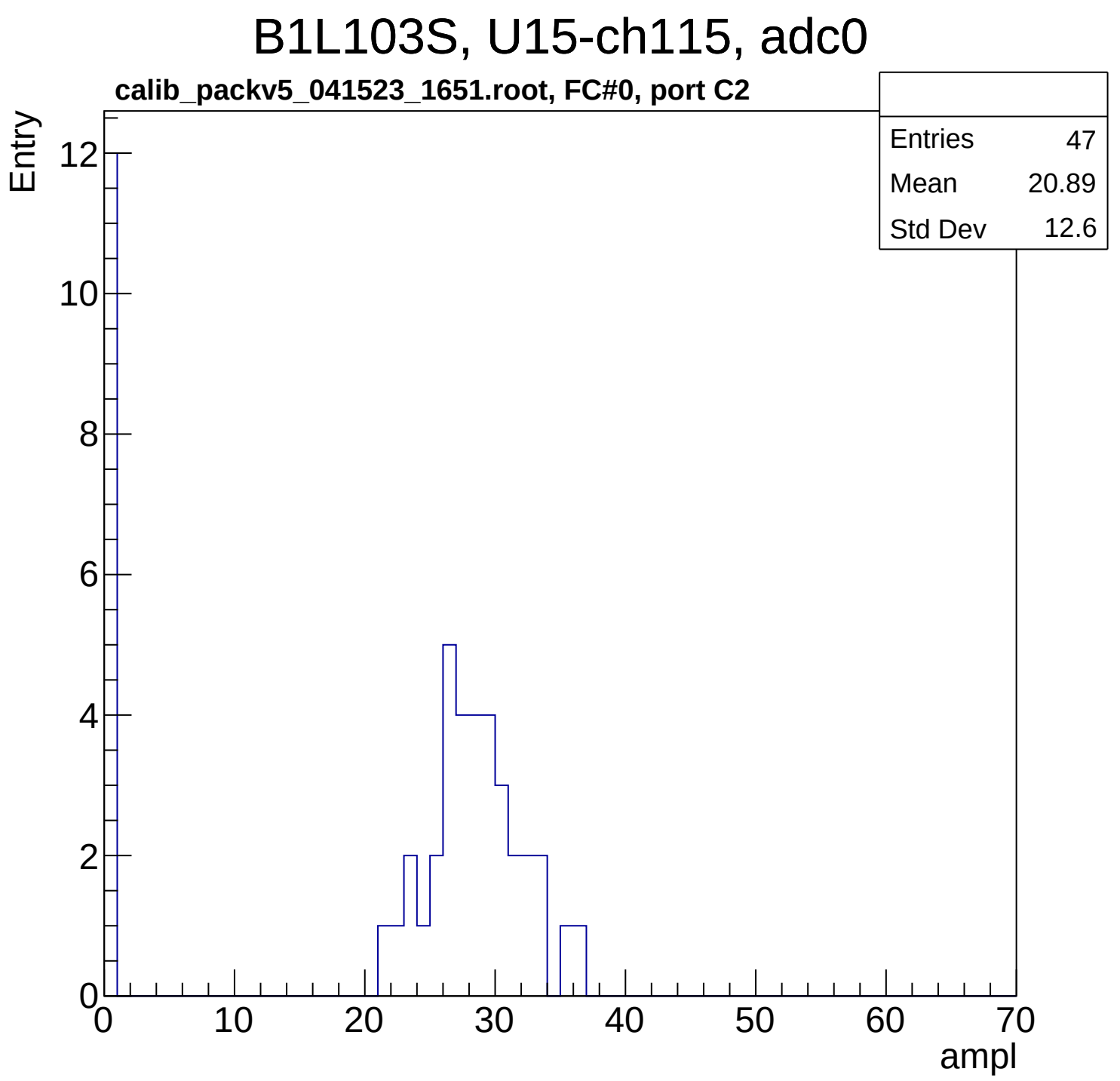

B1L103S, U15-ch114, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 46.3
Std Dev 3.737
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

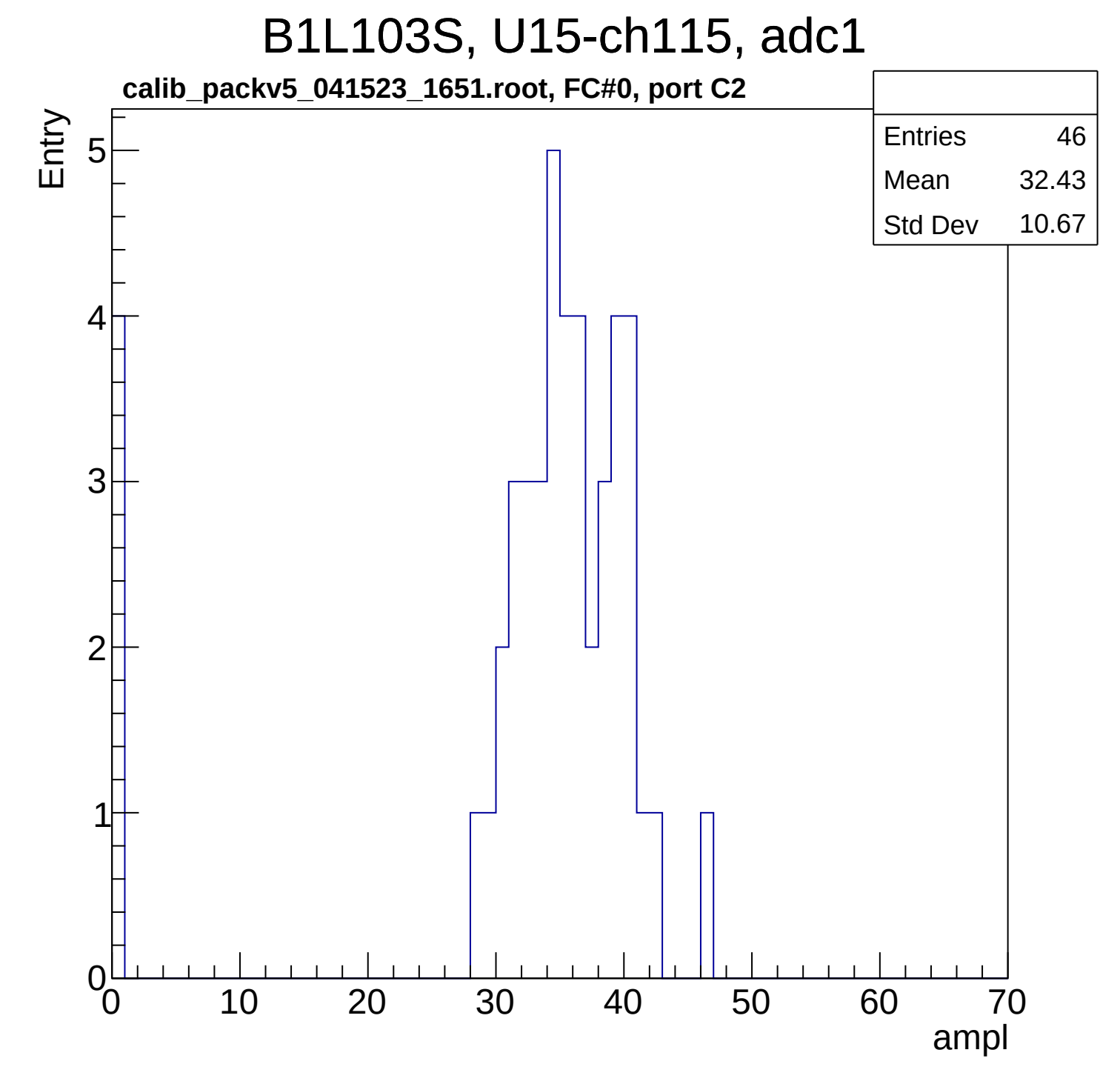

B1L103S, U15-ch114, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 53.54
Std Dev 3.315
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

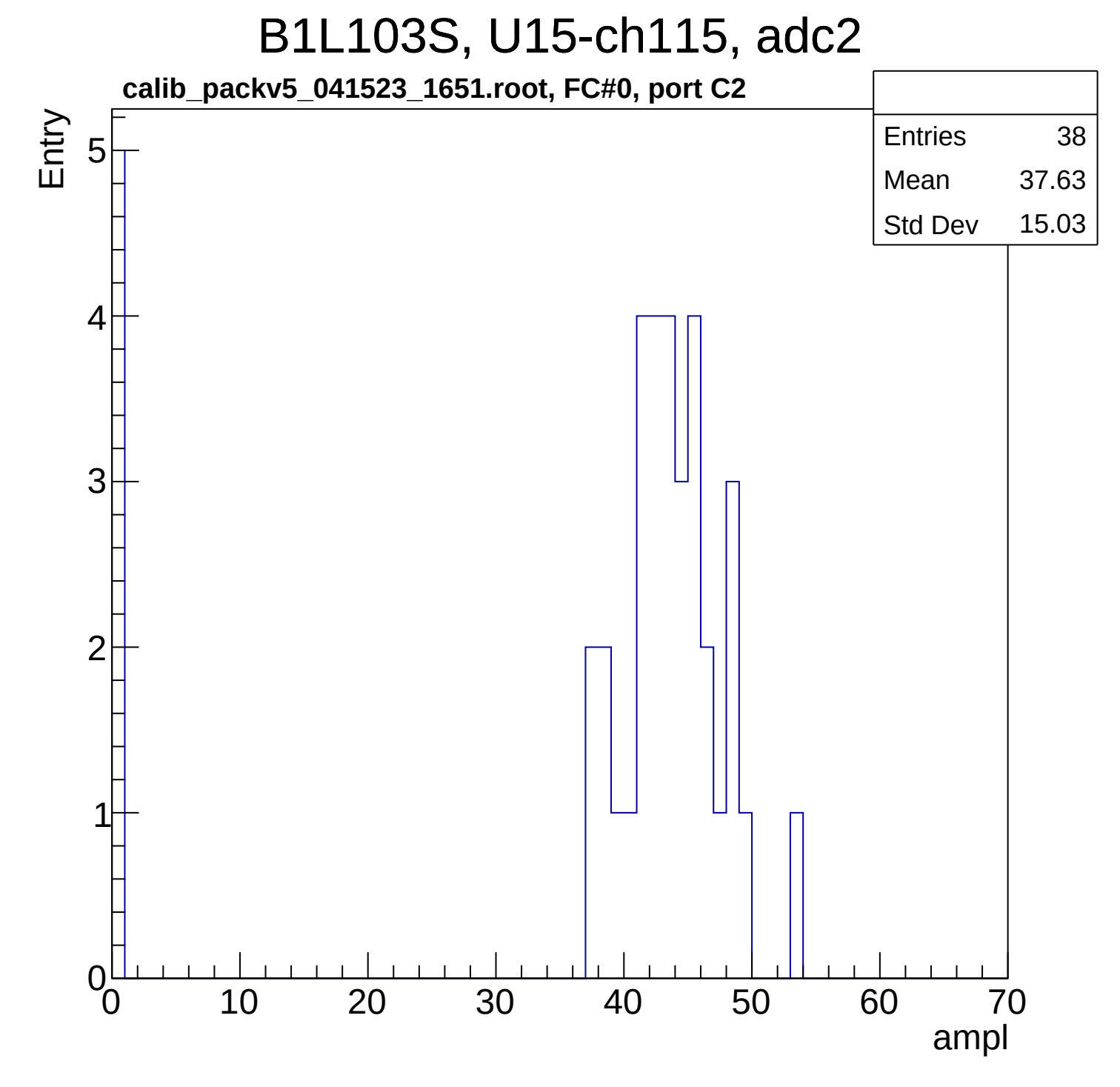

B1L103S, U15-ch114, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.77
Std Dev 2.922
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

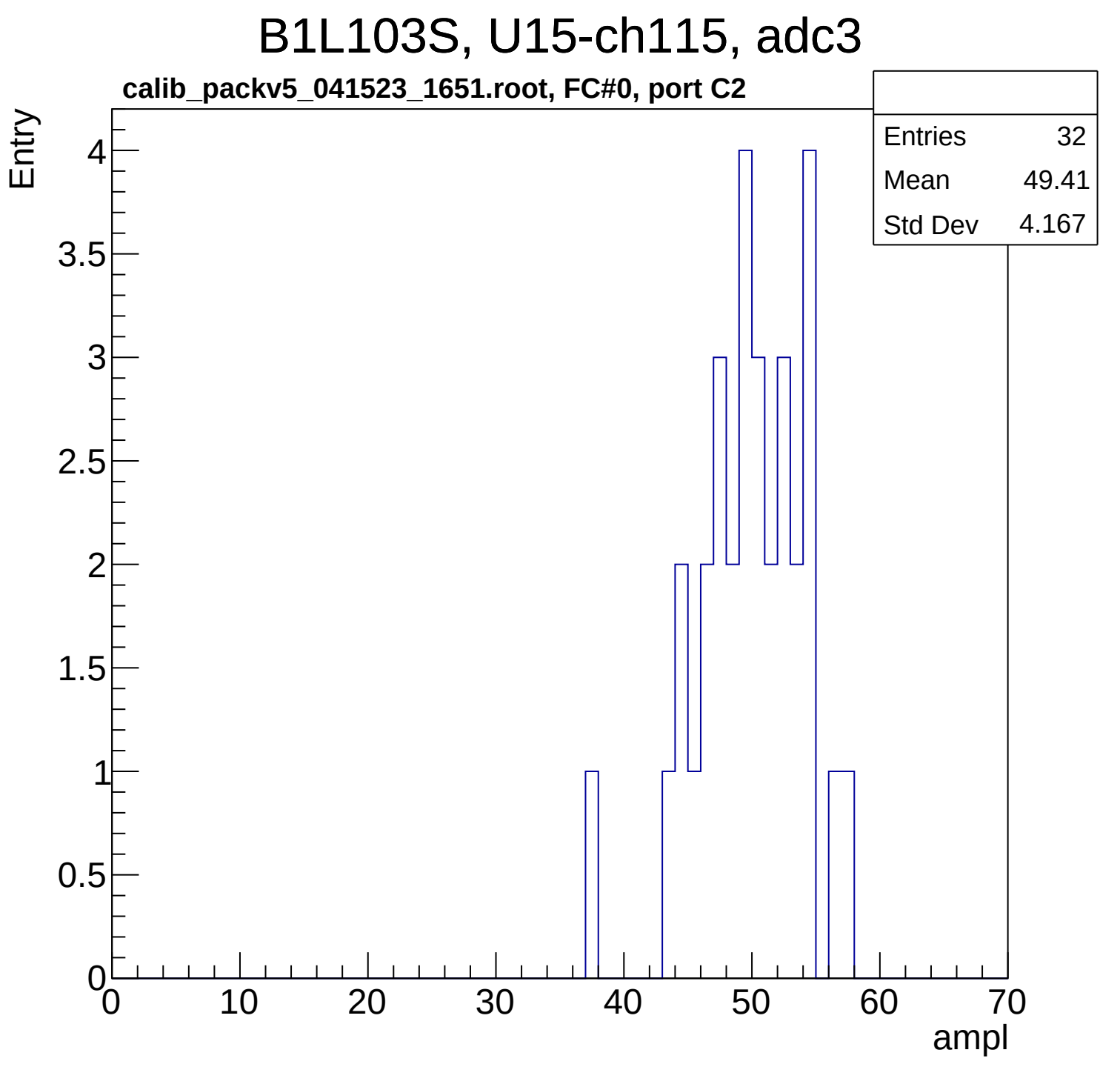

B1L103S, U15-ch114, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 60.7
Std Dev 1.847
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

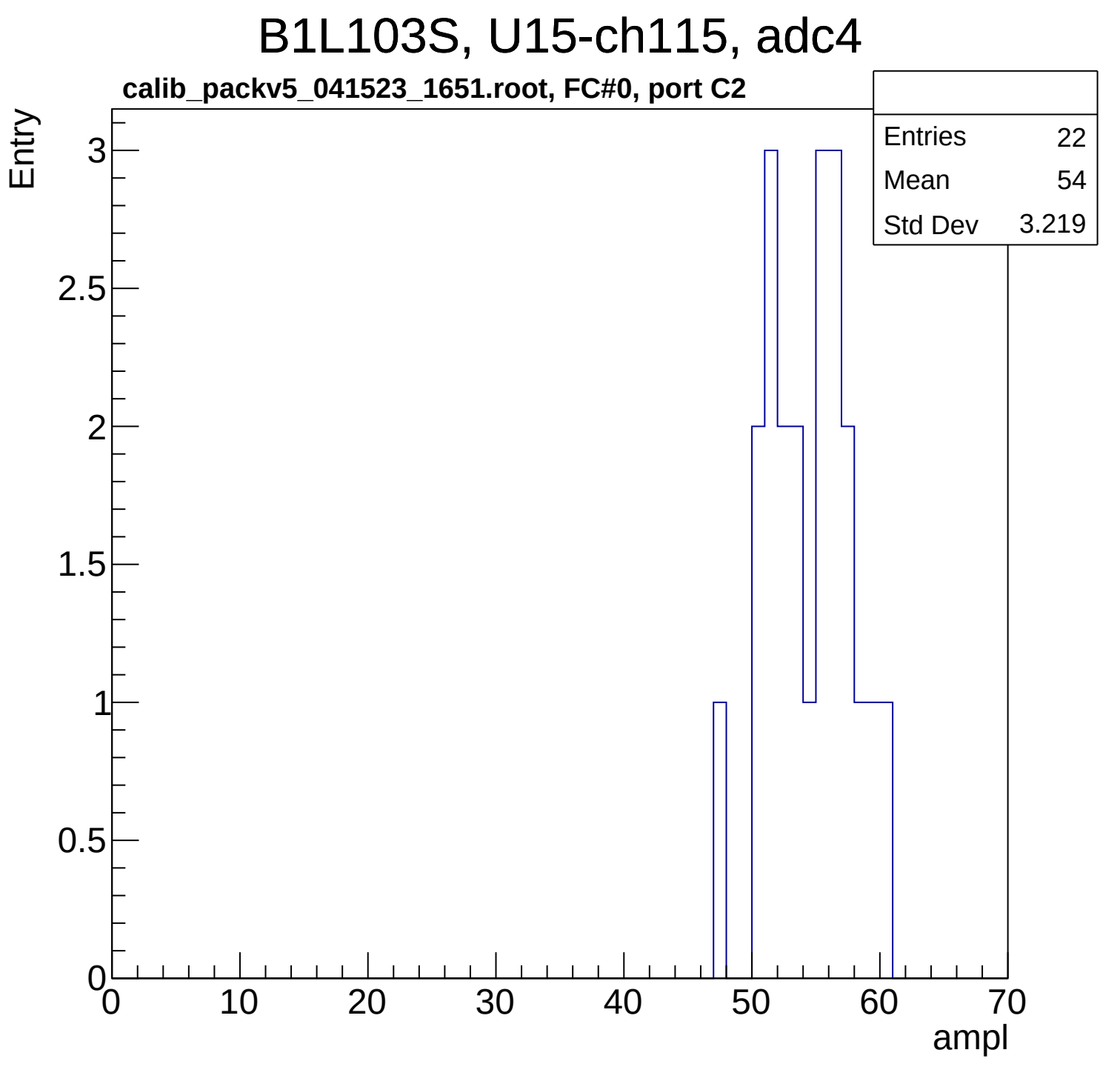

B1L103S, U15-ch114, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 5.636
Std Dev 17.82
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

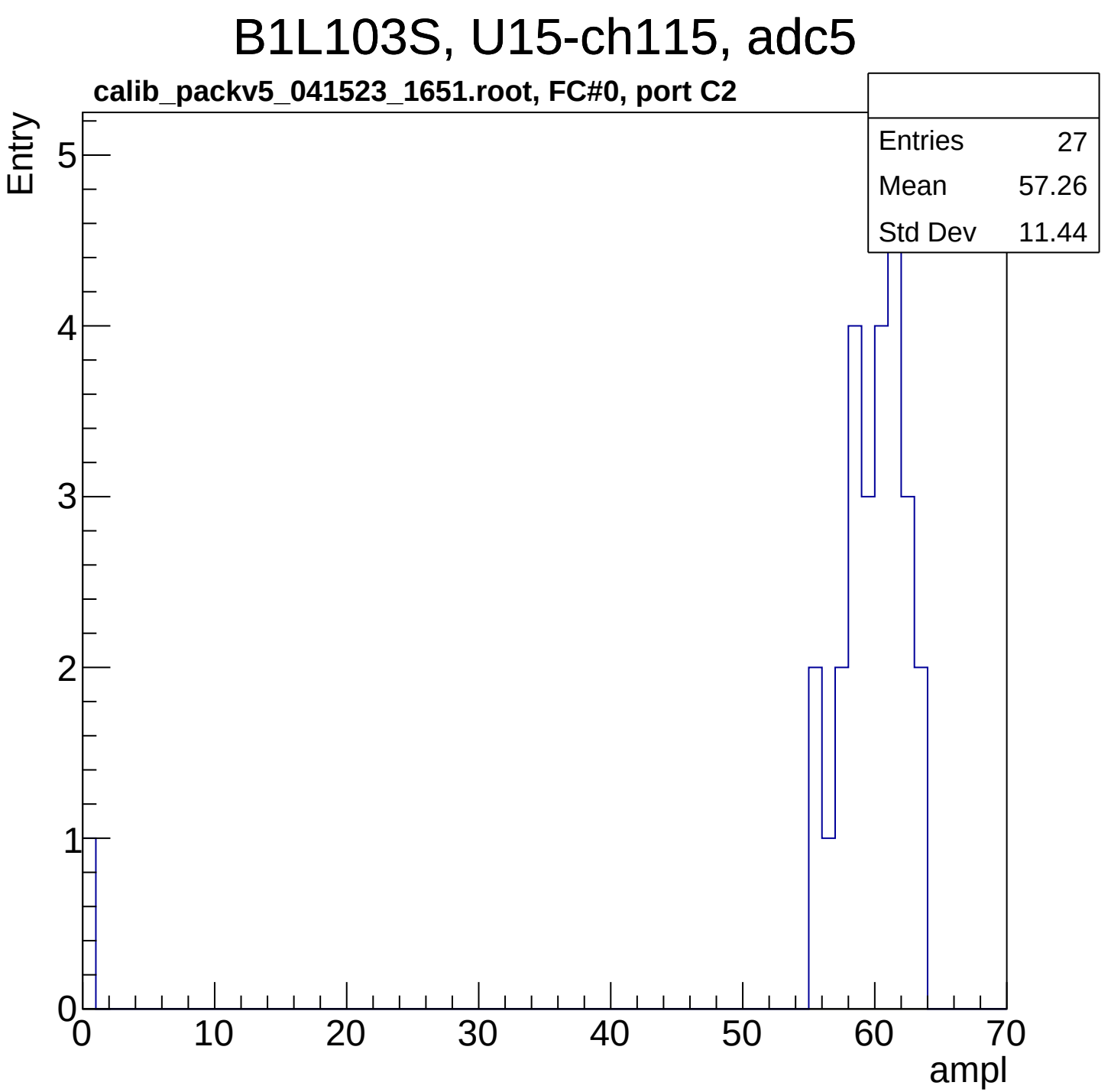

B1L103S, U15-ch115, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 20.89
Std Dev 12.6
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

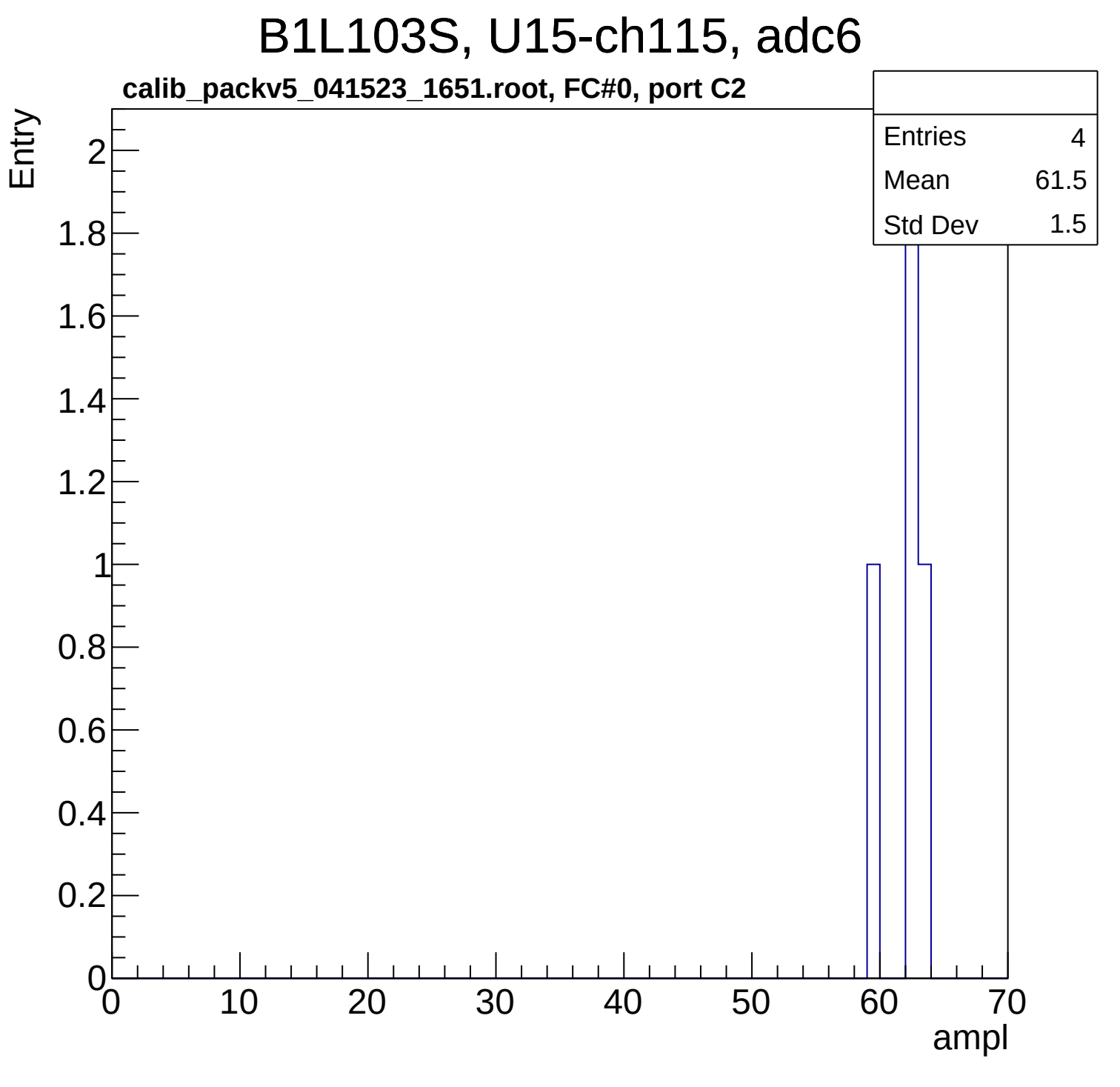

B1L103S, U15-ch115, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 32.43
Std Dev 10.67
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

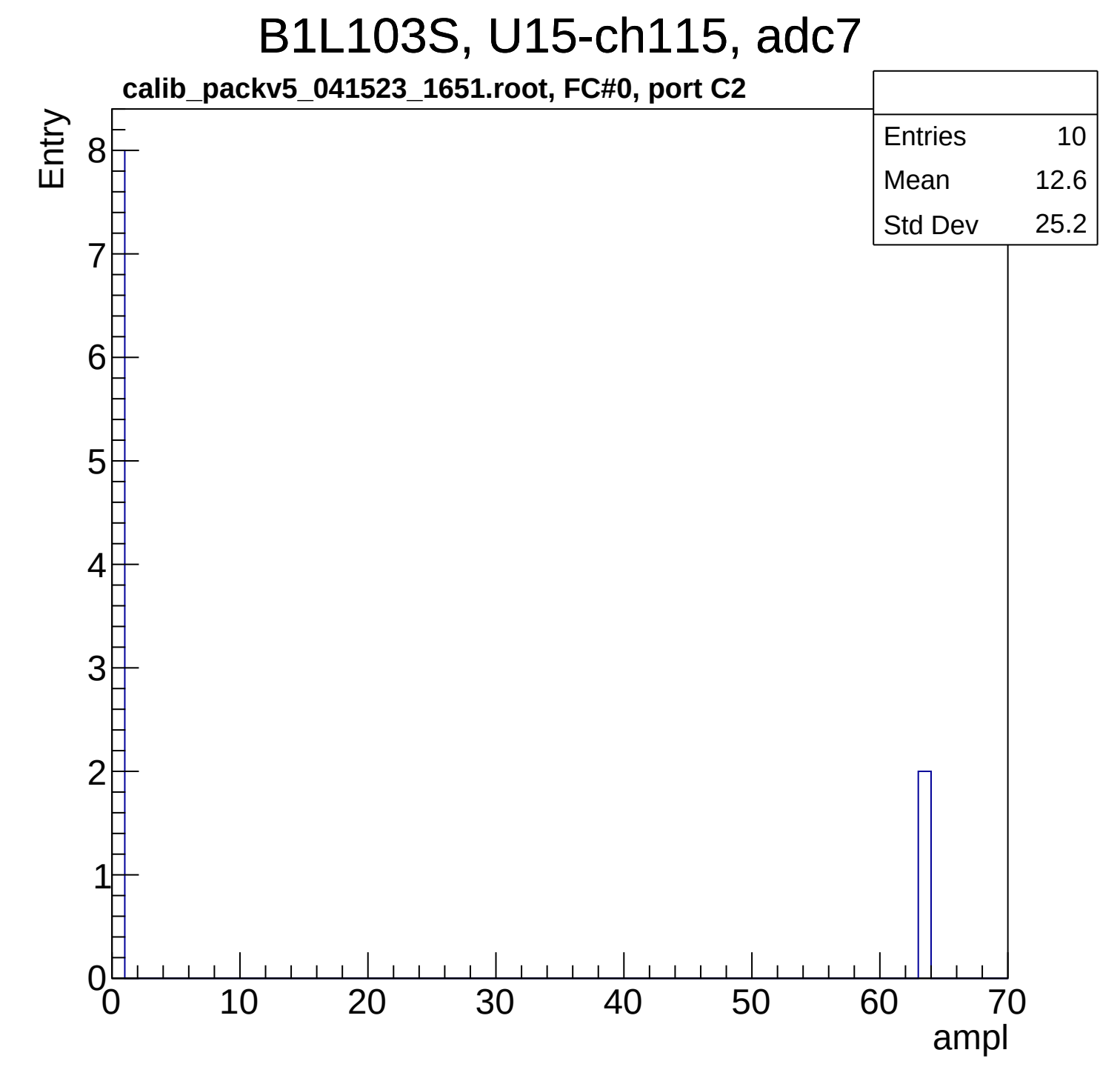

B1L103S, U15-ch115, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 37.63
Std Dev 15.03
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

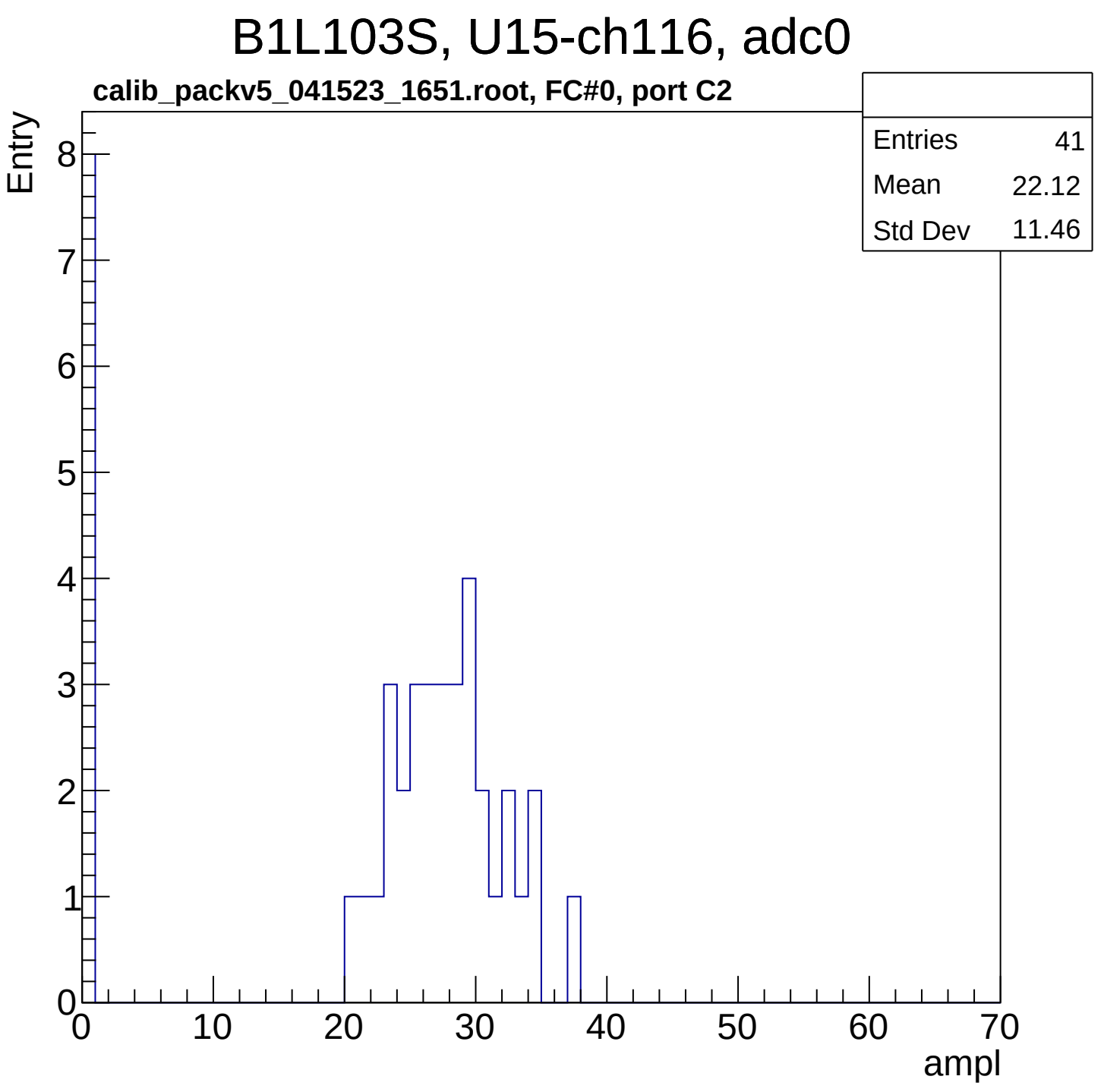

B1L103S, U15-ch115, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 49.41
Std Dev 4.167
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

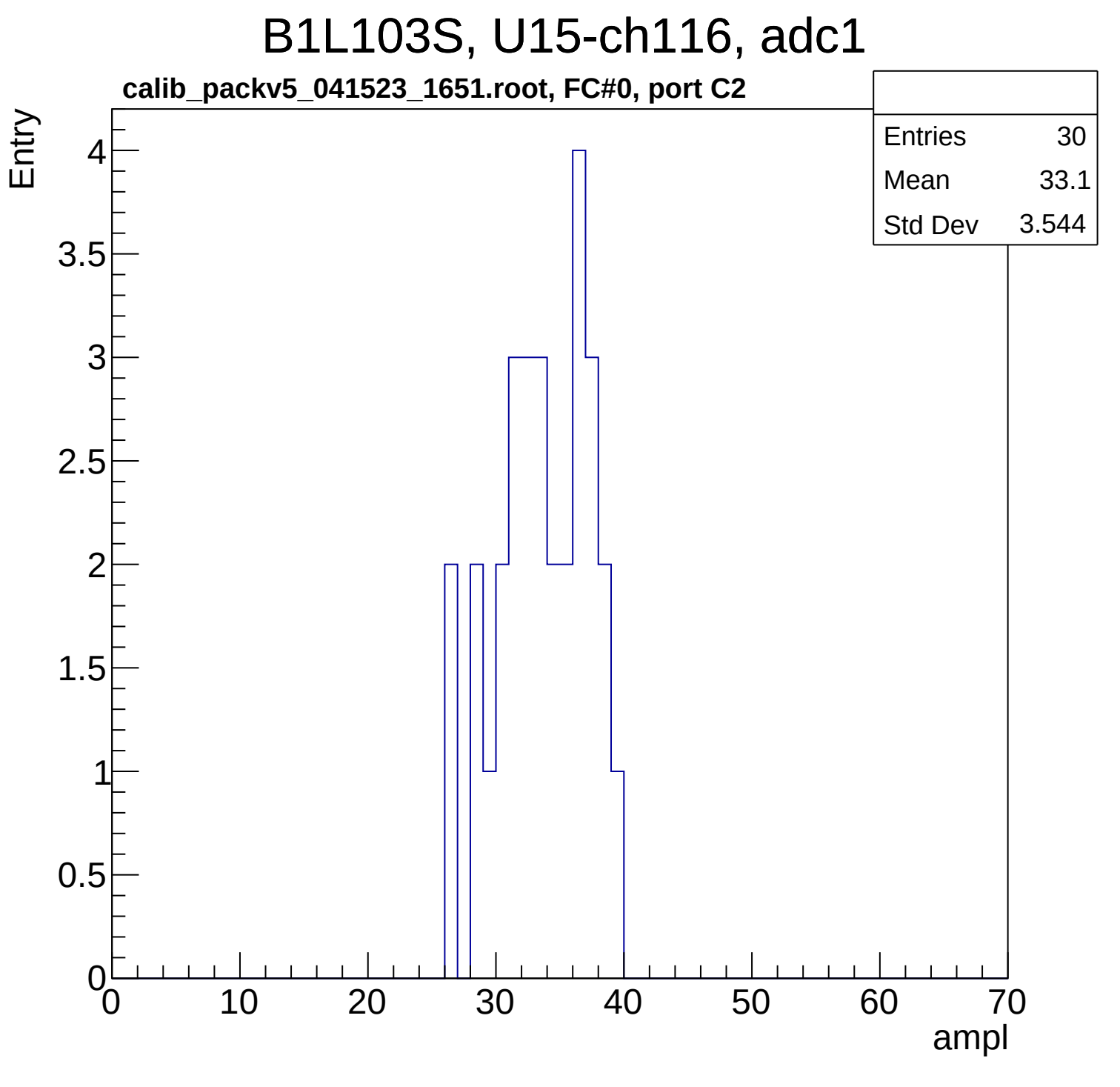

B1L103S, U15-ch115, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 54
Std Dev 3.219
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

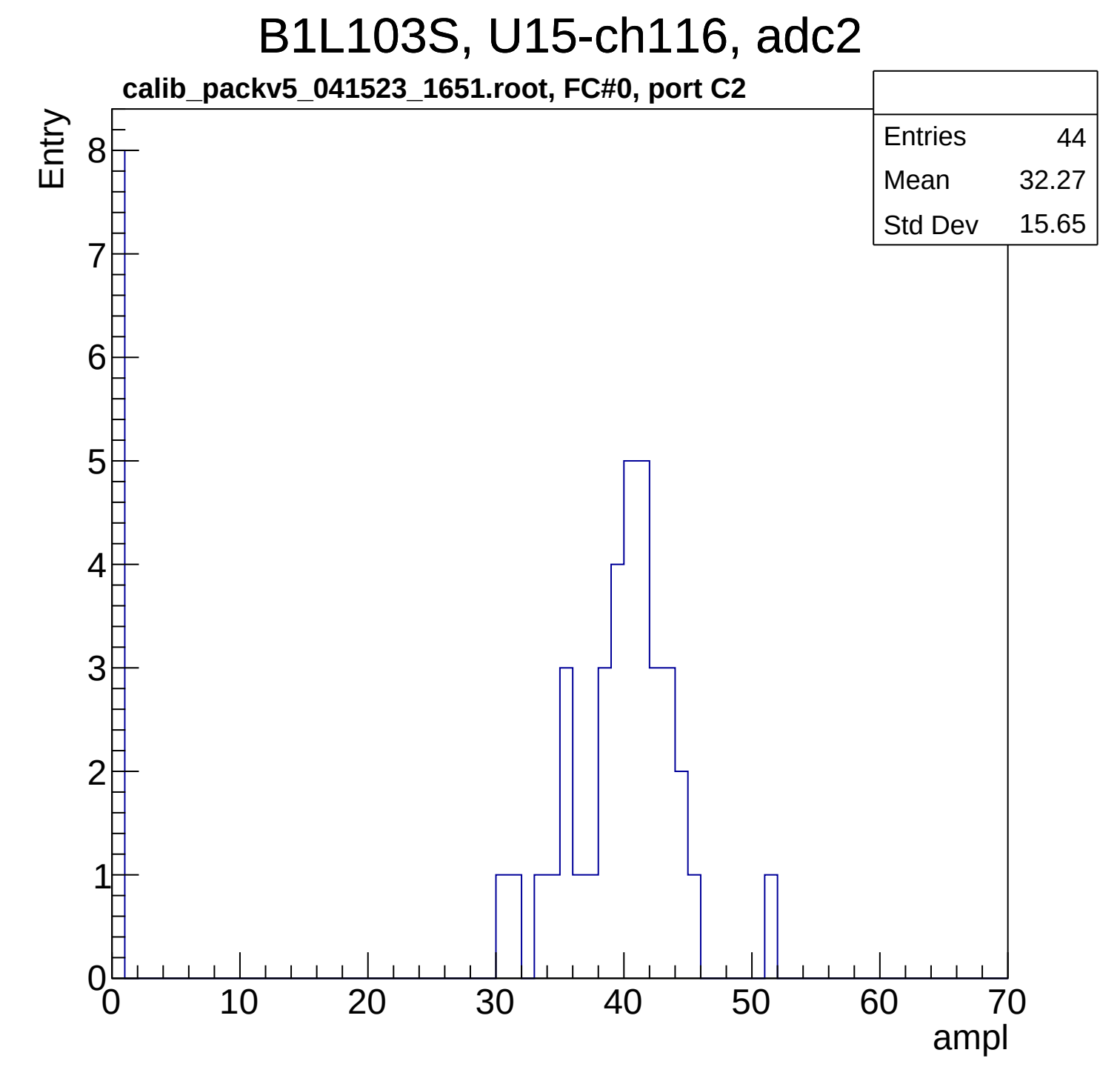

B1L103S, U15-ch115, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 57.26
Std Dev 11.44
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

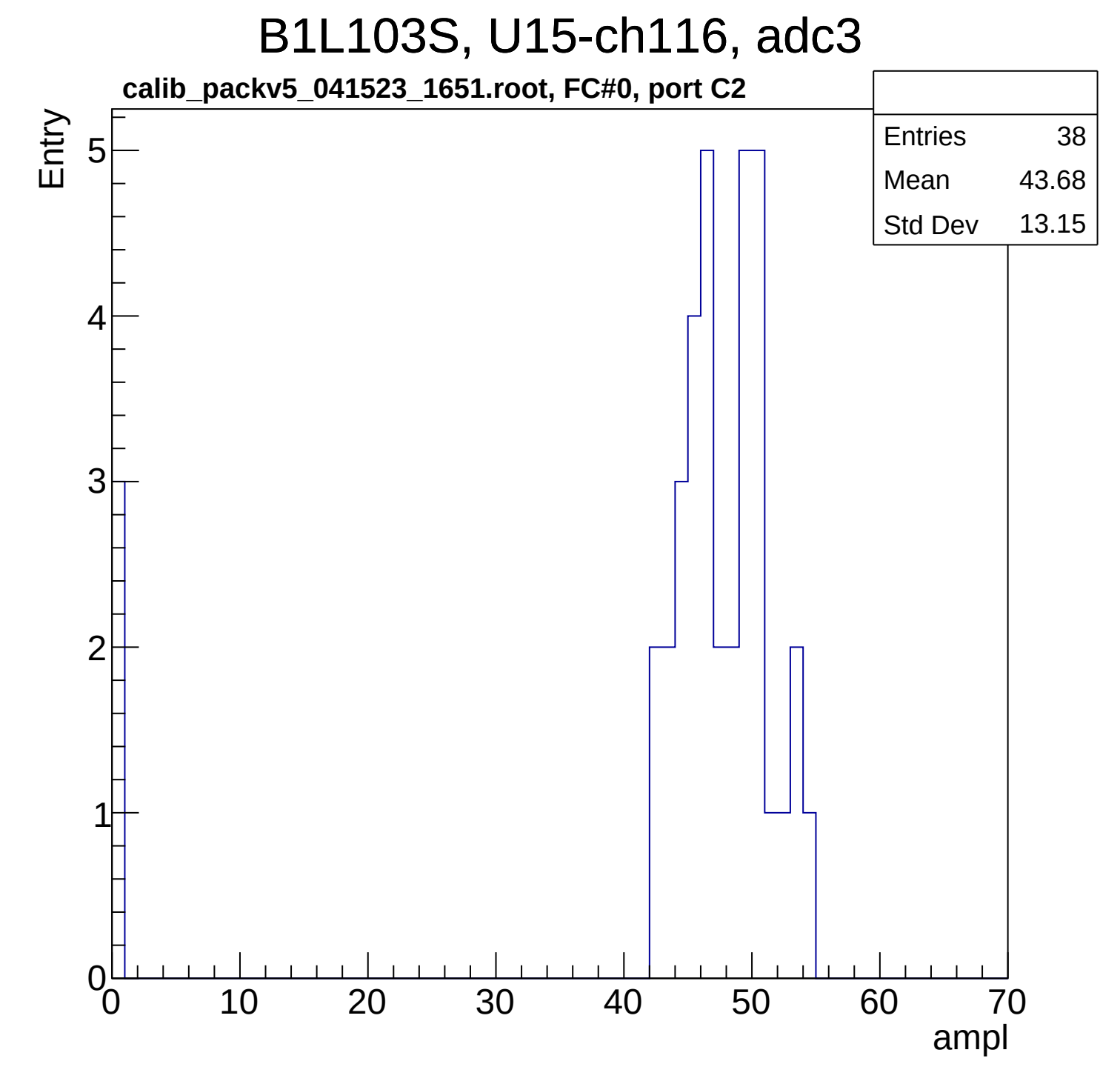

B1L103S, U15-ch115, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61.5
Std Dev 1.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

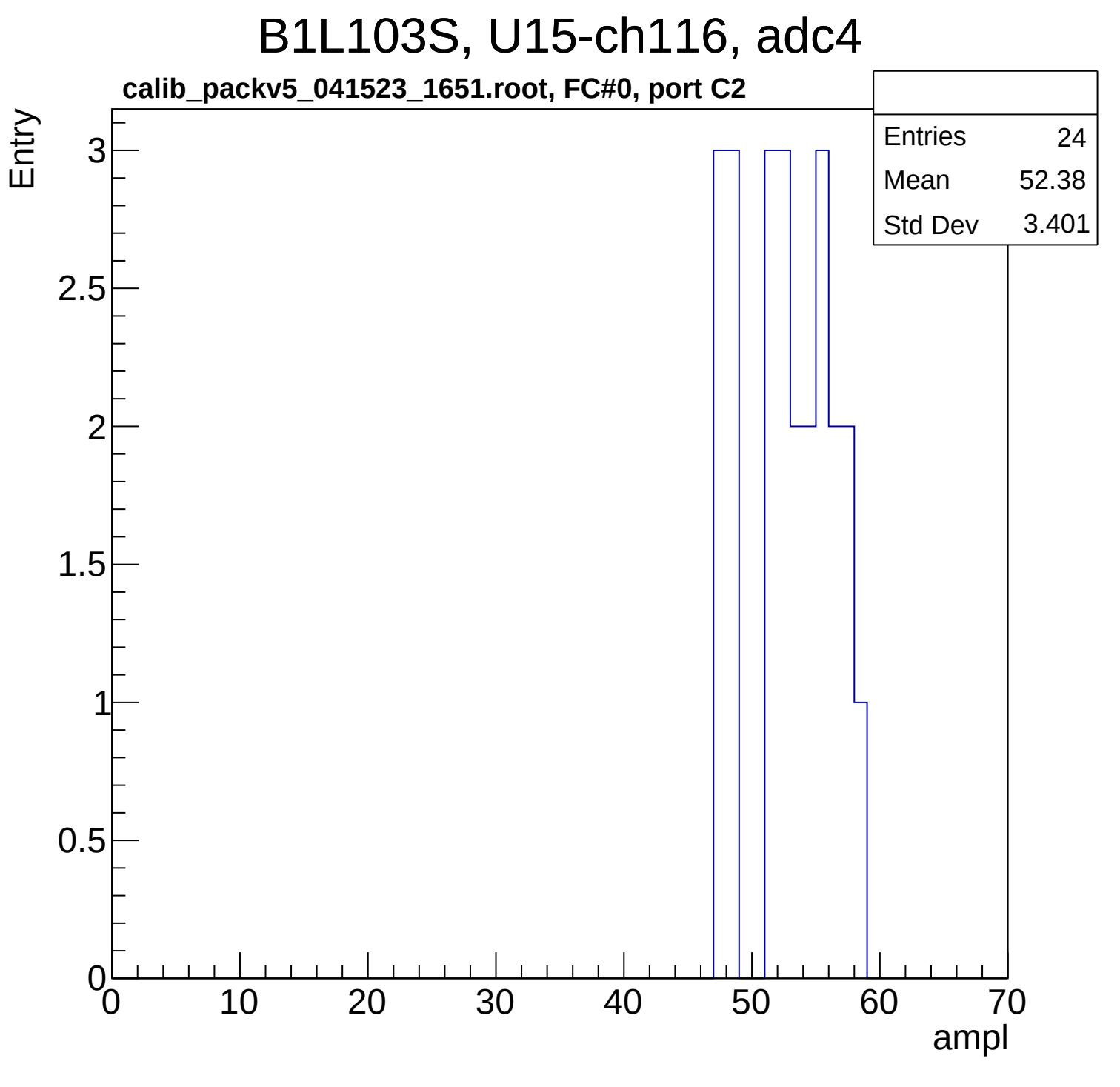

B1L103S, U15-ch115, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 12.6
Std Dev 25.2
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

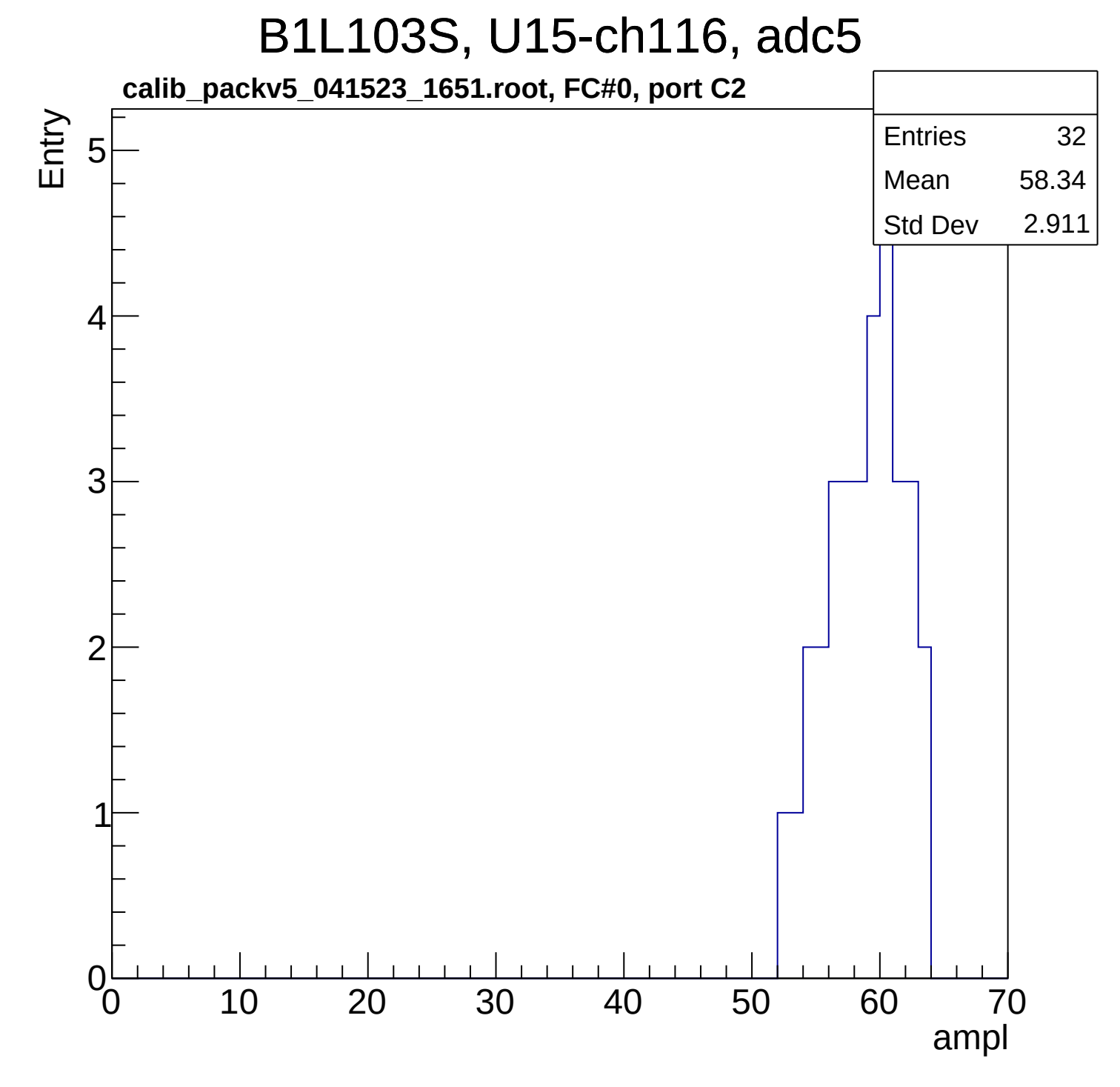

B1L103S, U15-ch116, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 22.12
Std Dev 11.46
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

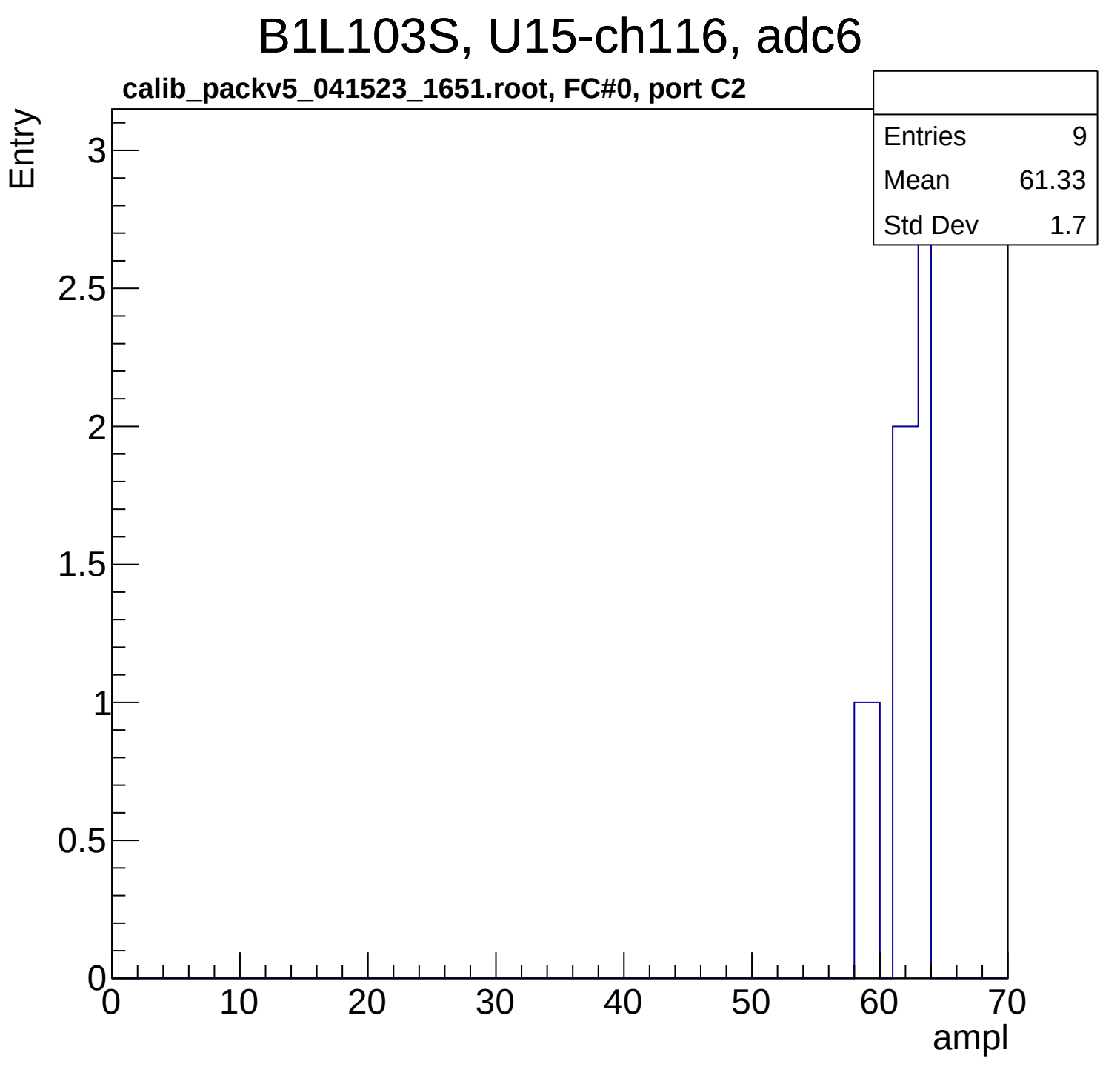

B1L103S, U15-ch116, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 33.1
Std Dev 3.544
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

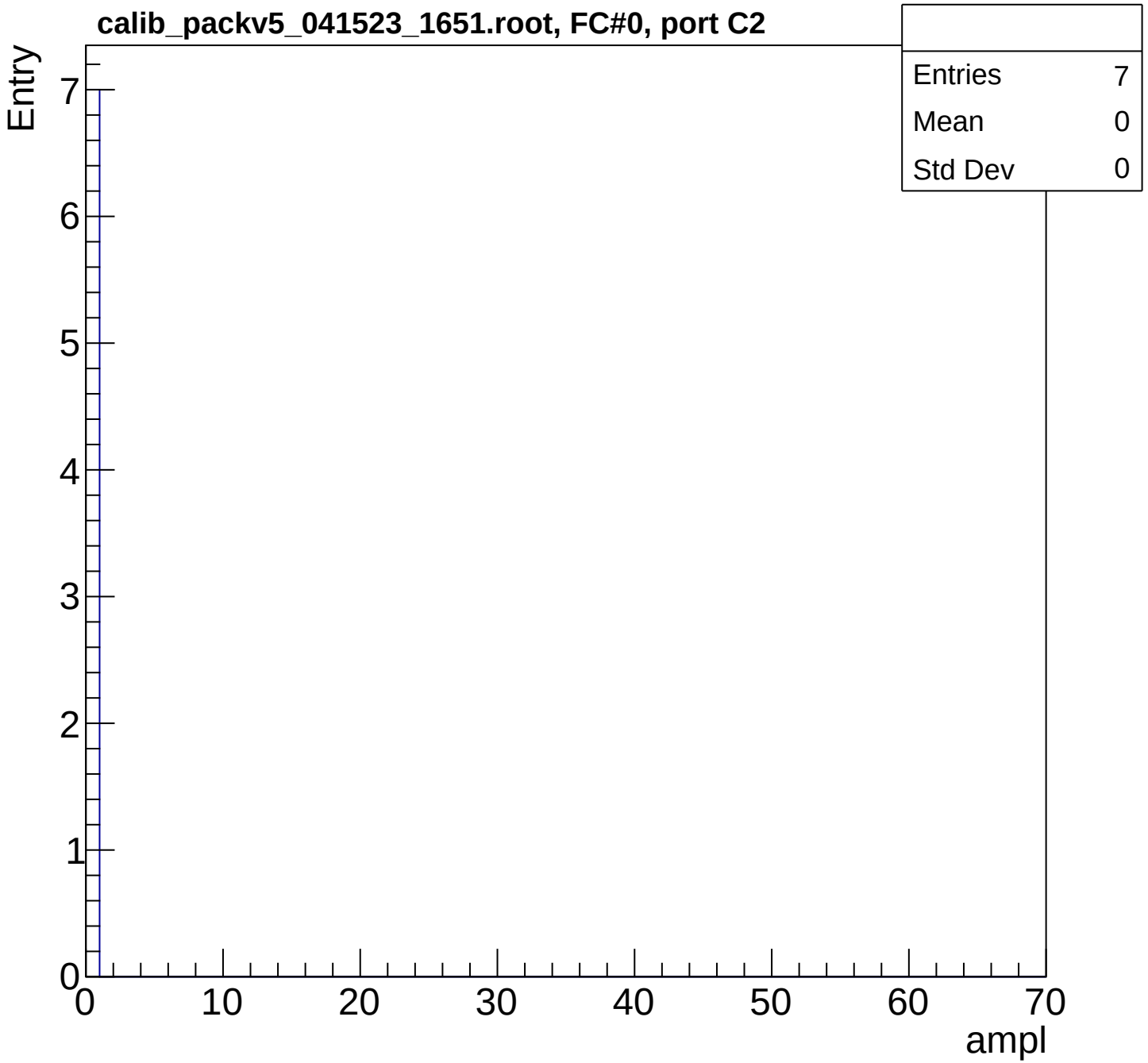

B1L103S, U15-ch116, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 32.27
Std Dev 15.65
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

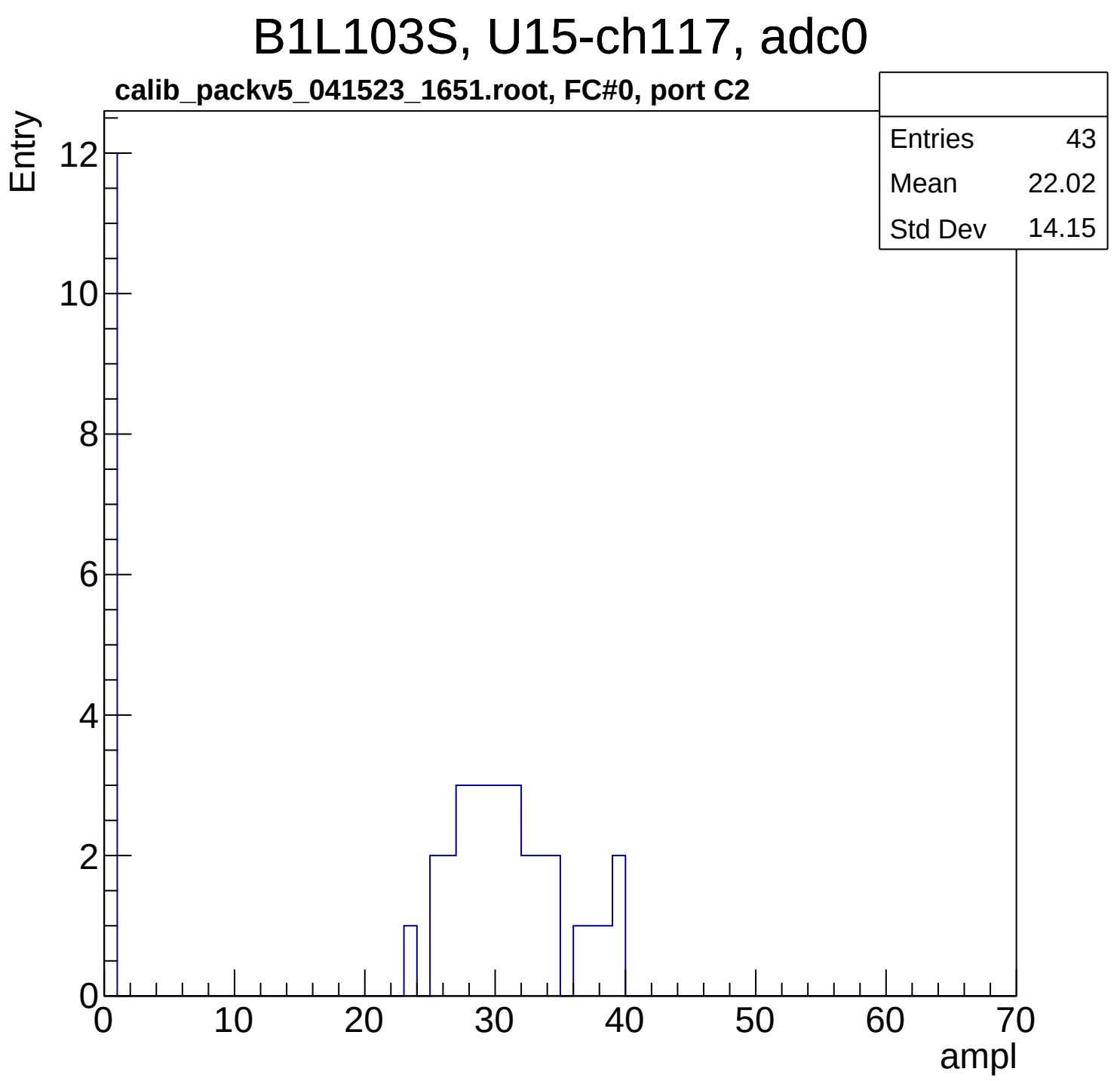

B1L103S, U15-ch116, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 43.68
Std Dev 13.15
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

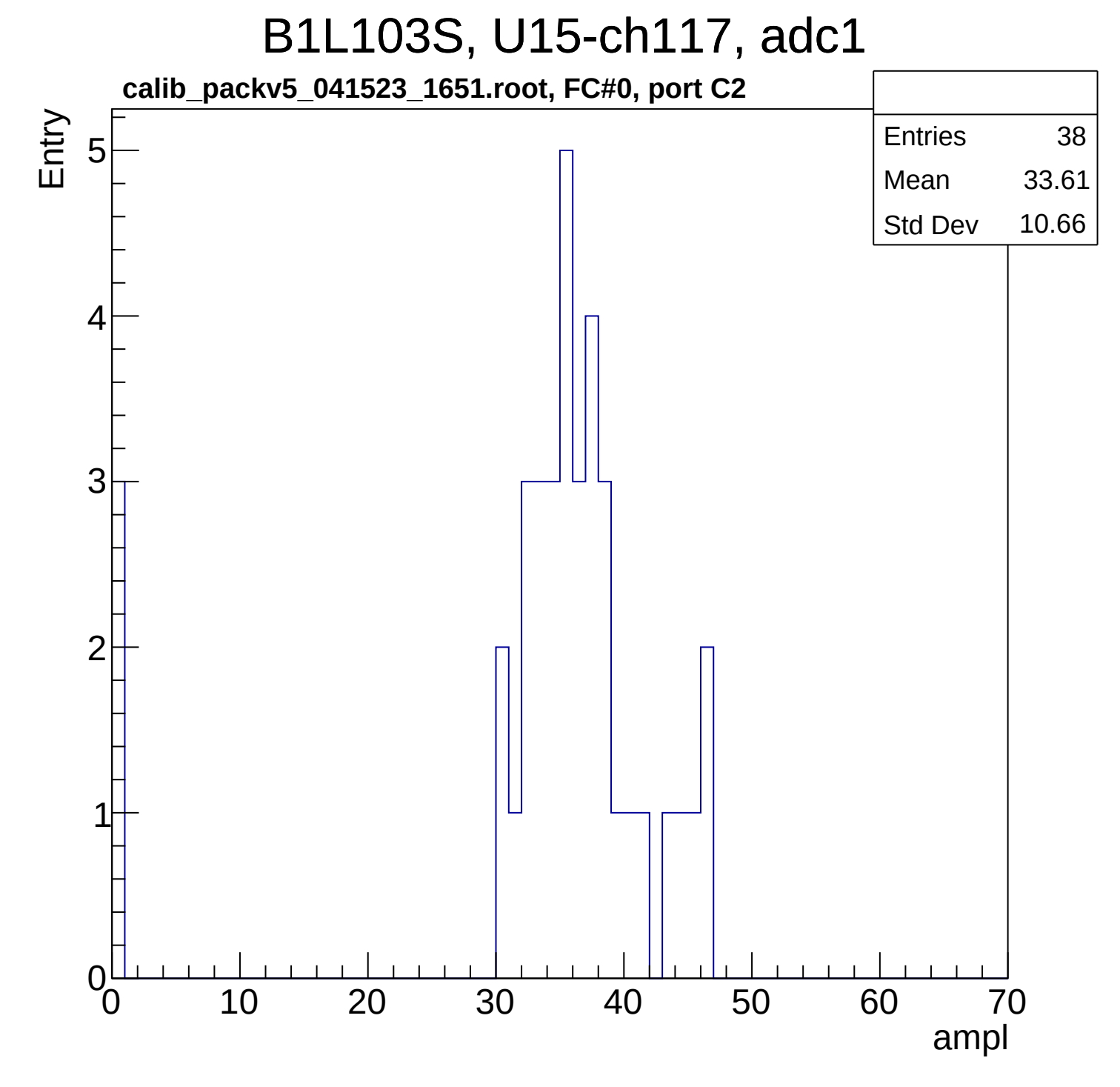

B1L103S, U15-ch116, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 52.38
Std Dev 3.401
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

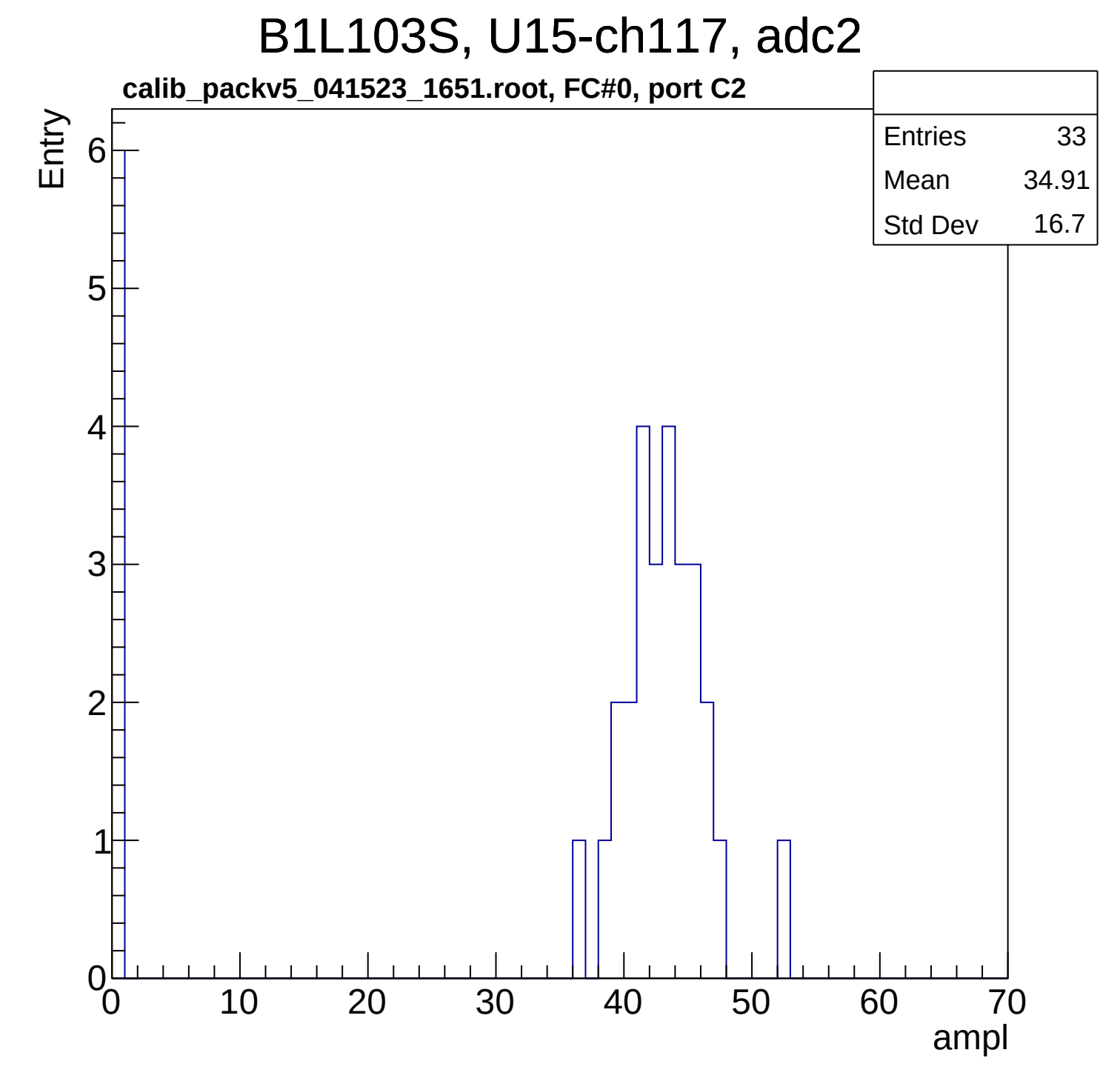

B1L103S, U15-ch116, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 58.34
Std Dev 2.911
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

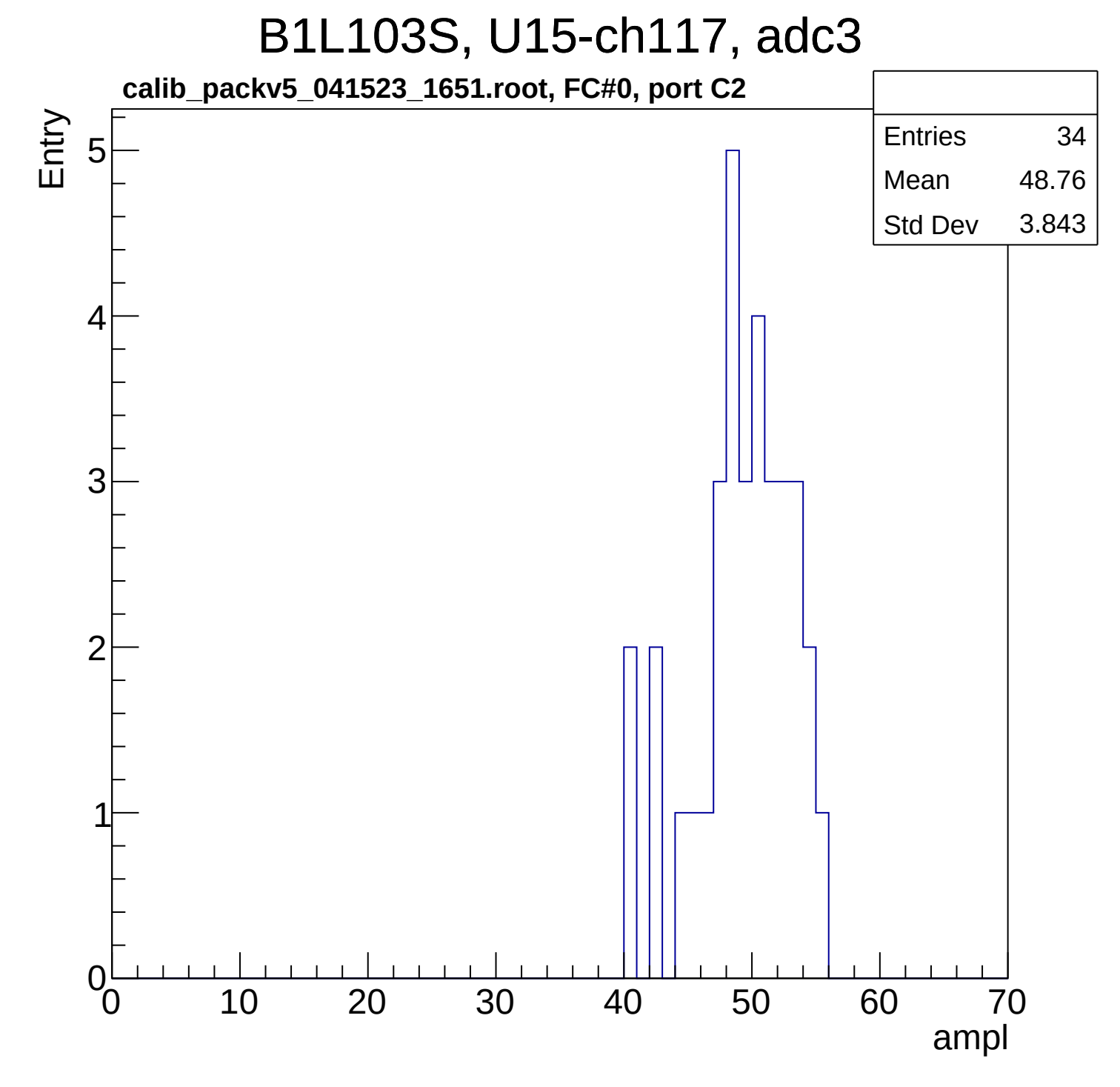

B1L103S, U15-ch116, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.33
Std Dev 1.7
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

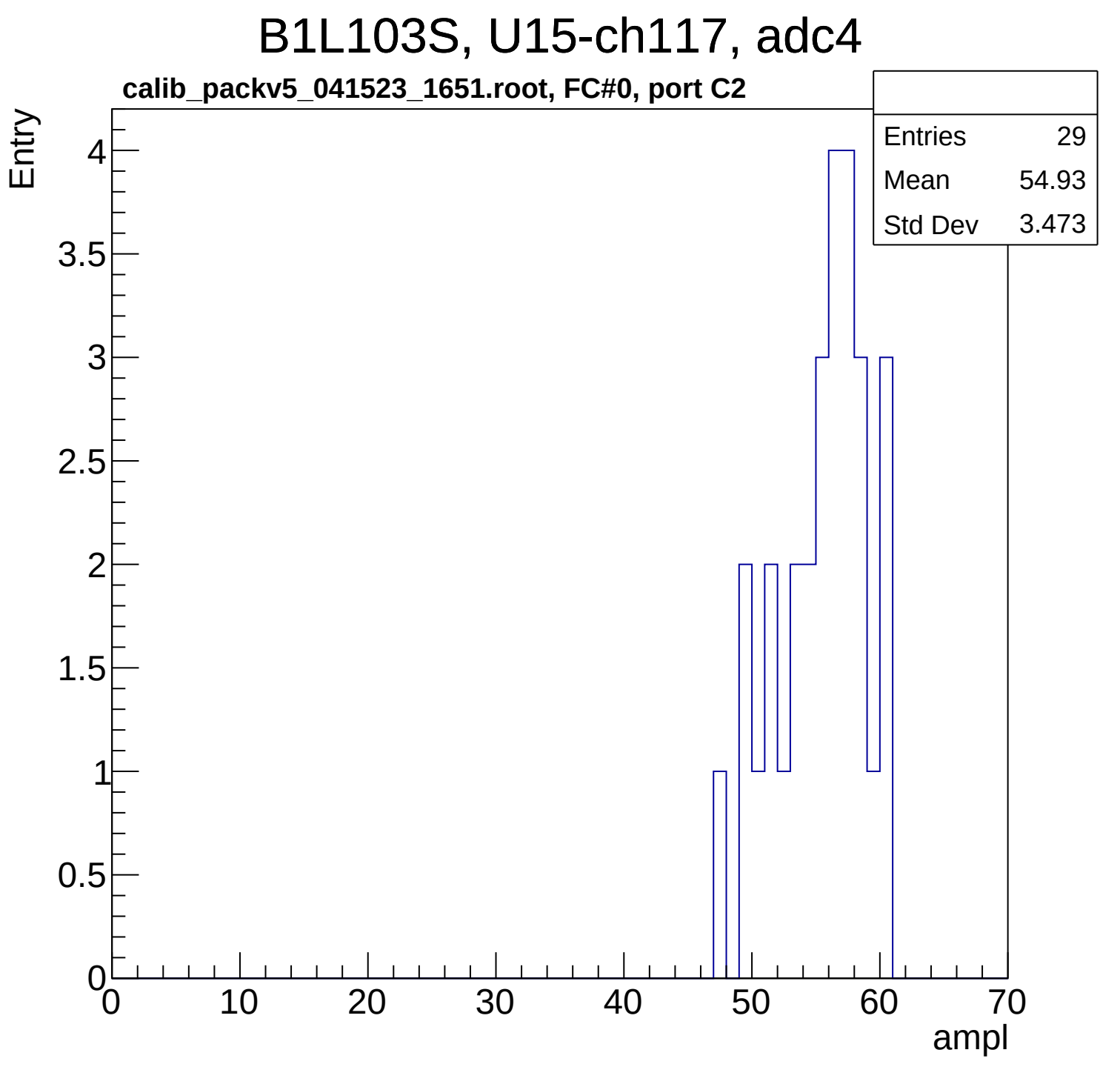

B1L103S, U15-ch116, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 0
Std Dev 0
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

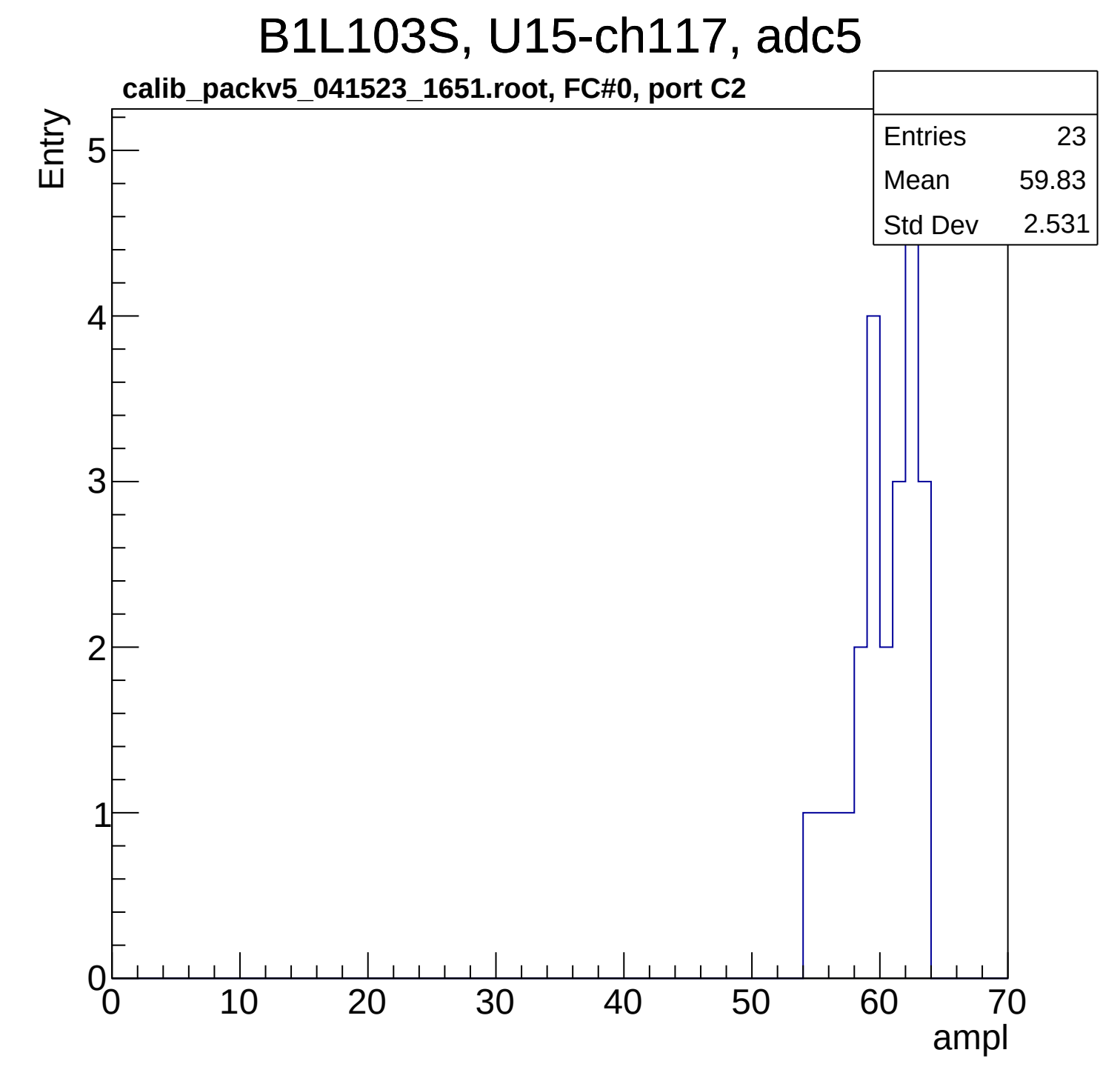

B1L103S, U15-ch117, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 22.02
Std Dev 14.15
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

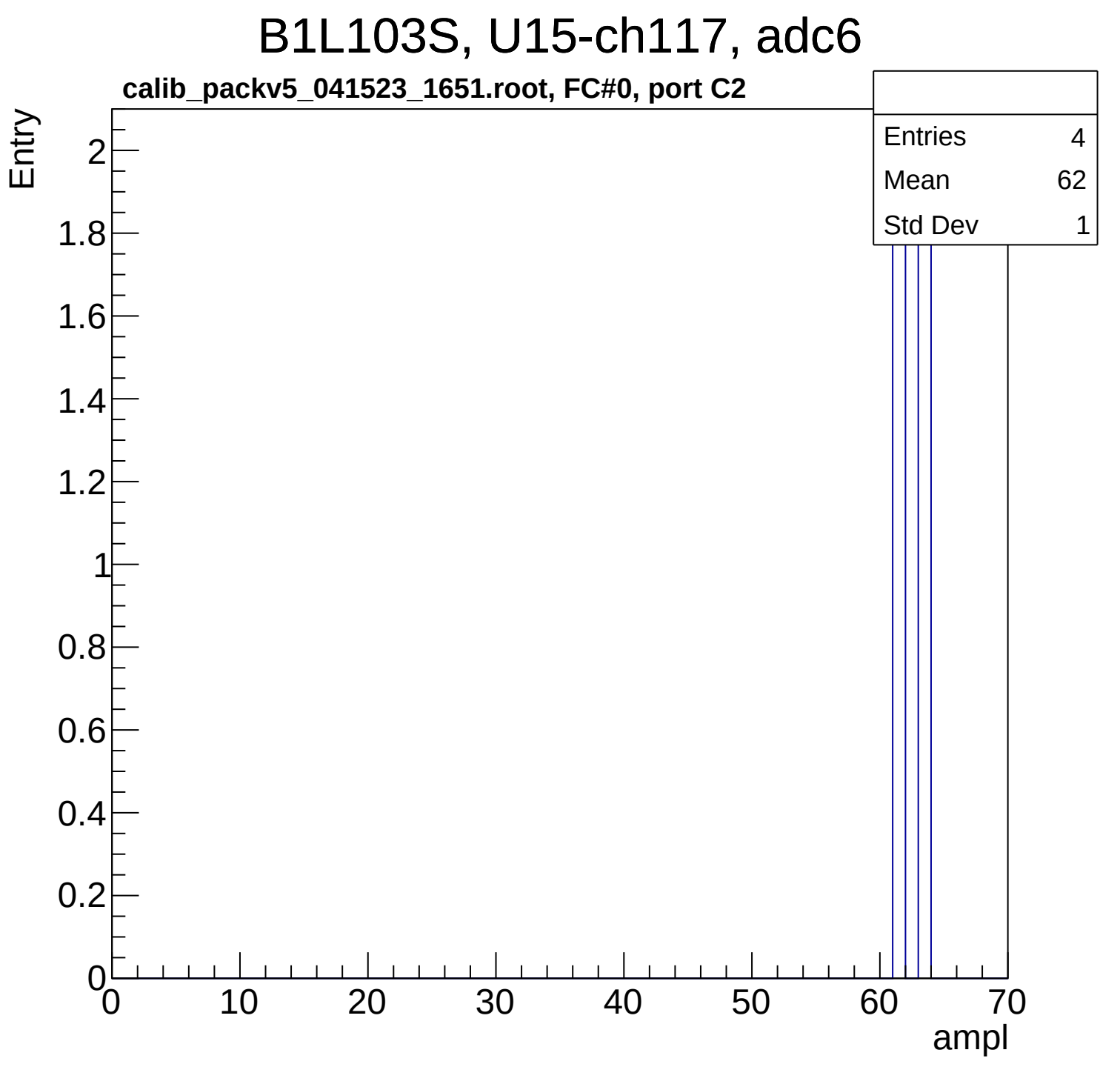

B1L103S, U15-ch117, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 33.61
Std Dev 10.66
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

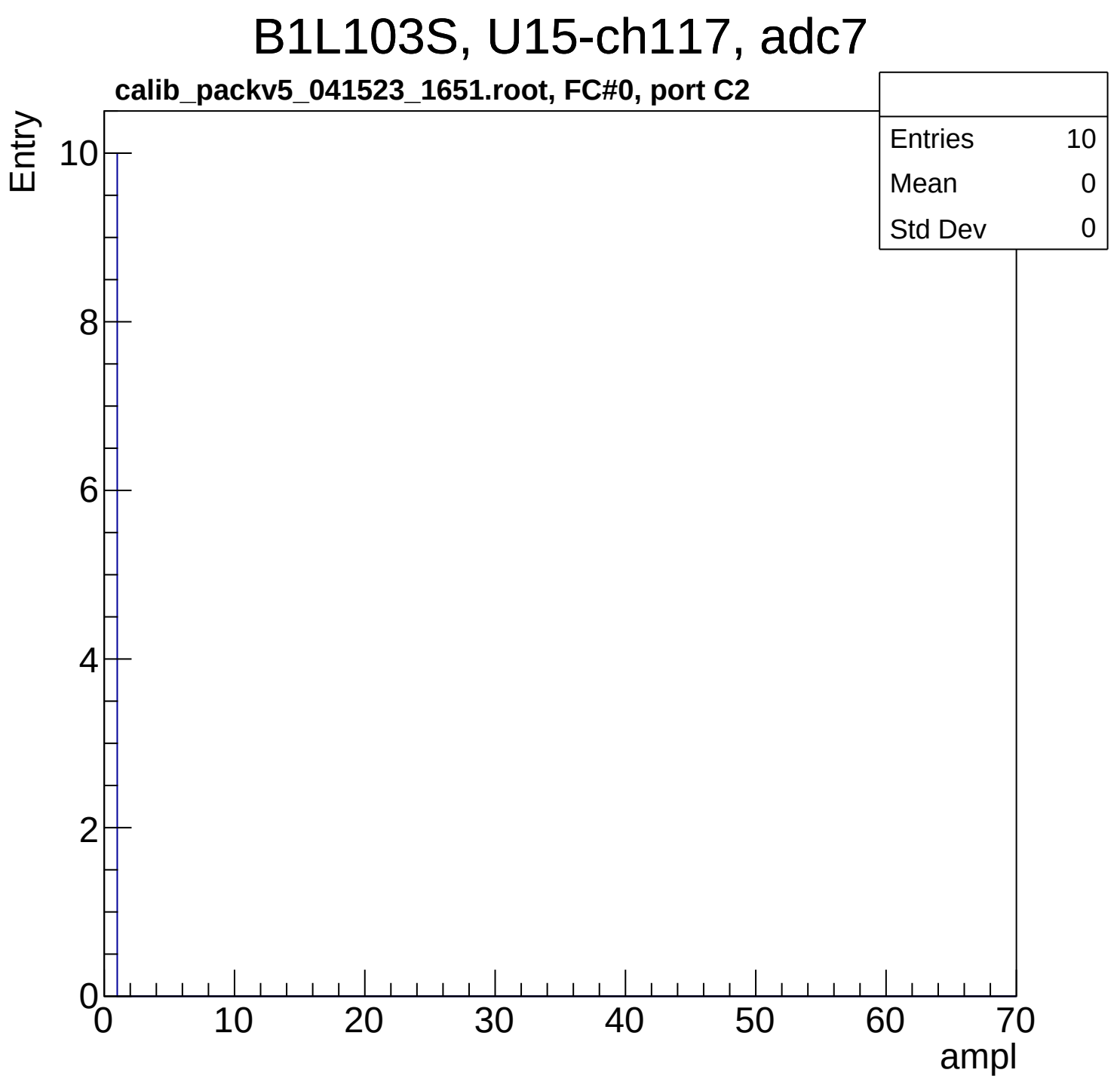

B1L103S, U15-ch117, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 34.91
Std Dev 16.7
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

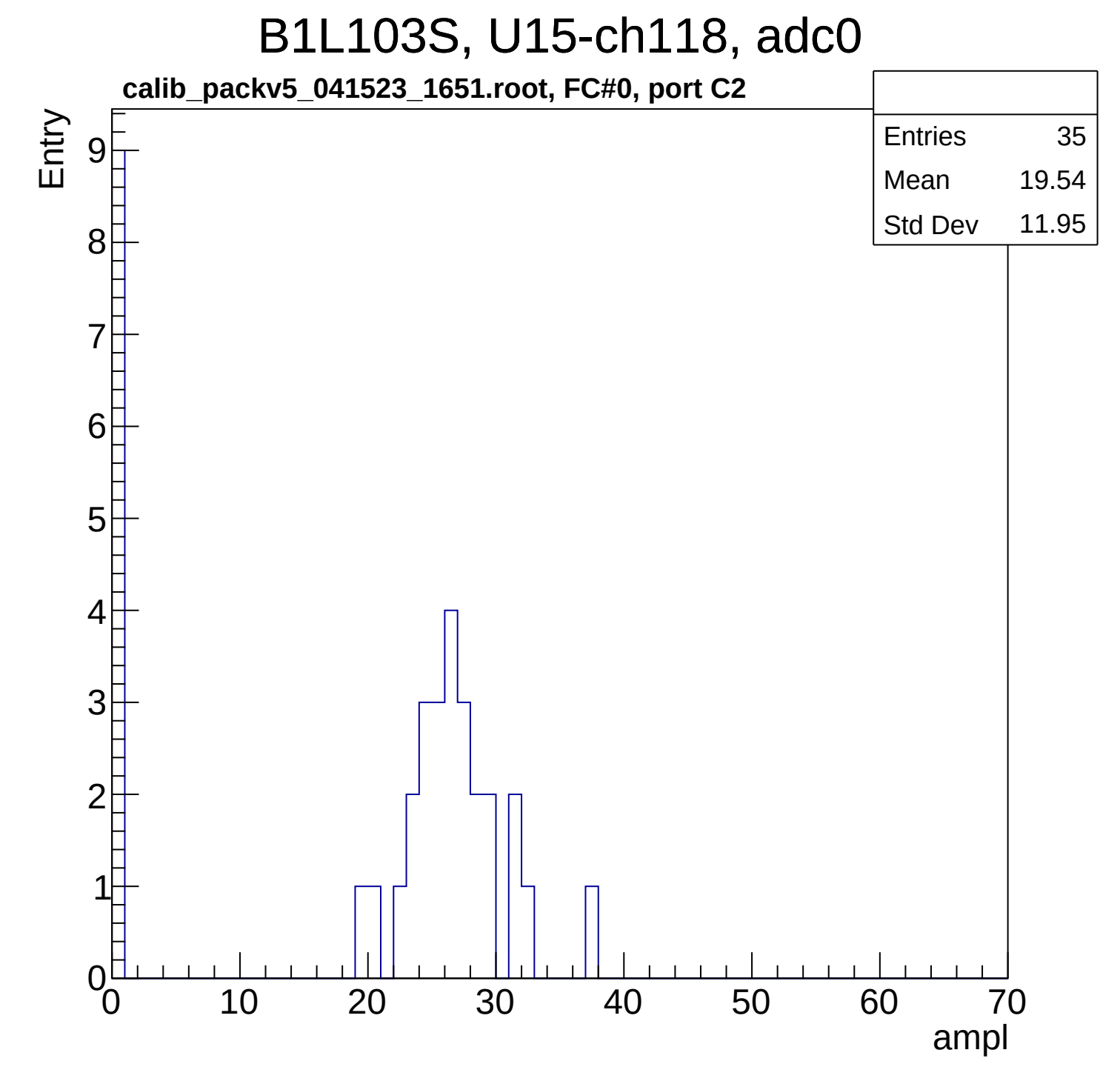

B1L103S, U15-ch117, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 48.76
Std Dev 3.843
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

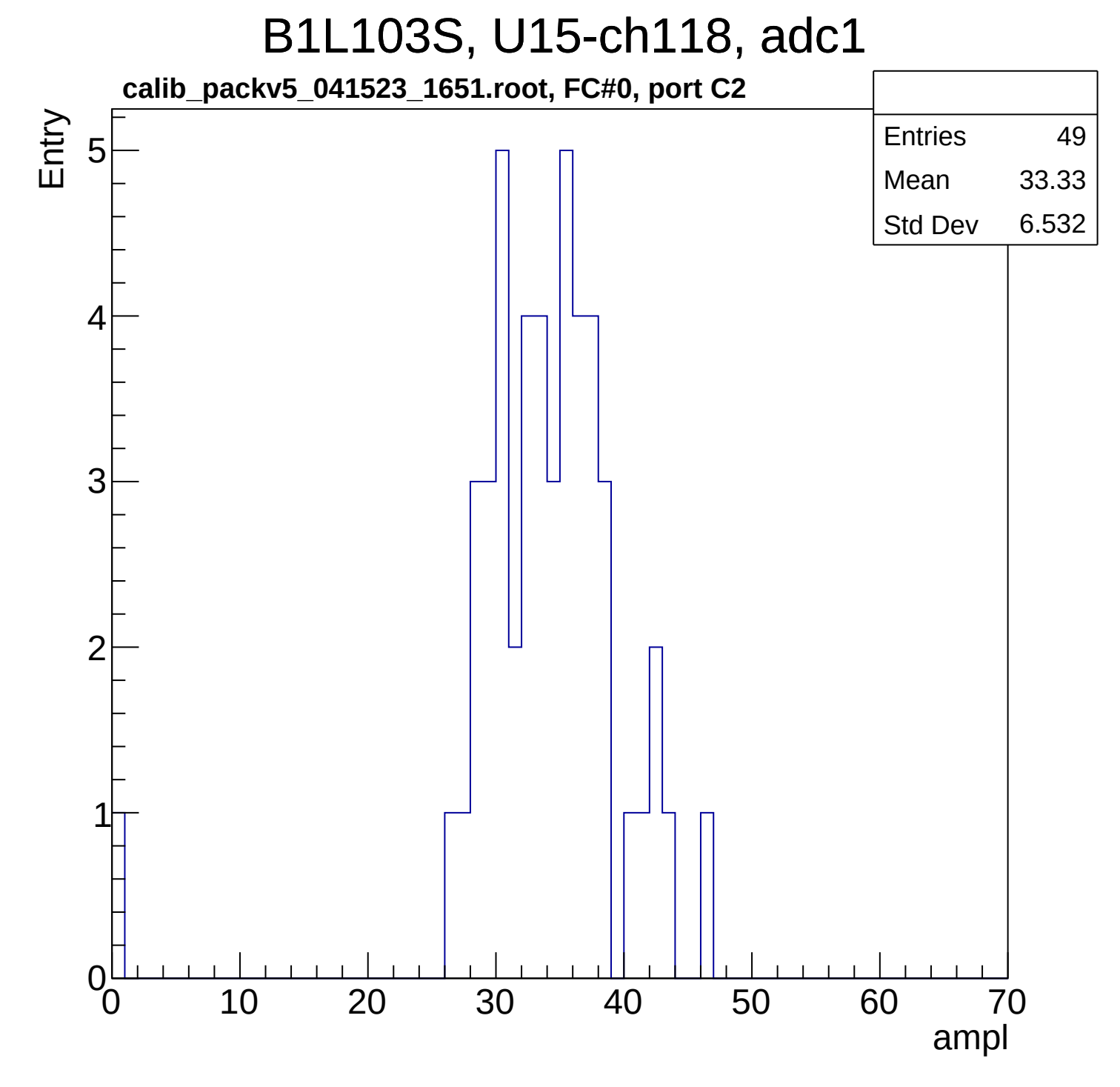

B1L103S, U15-ch117, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 54.93
Std Dev 3.473
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

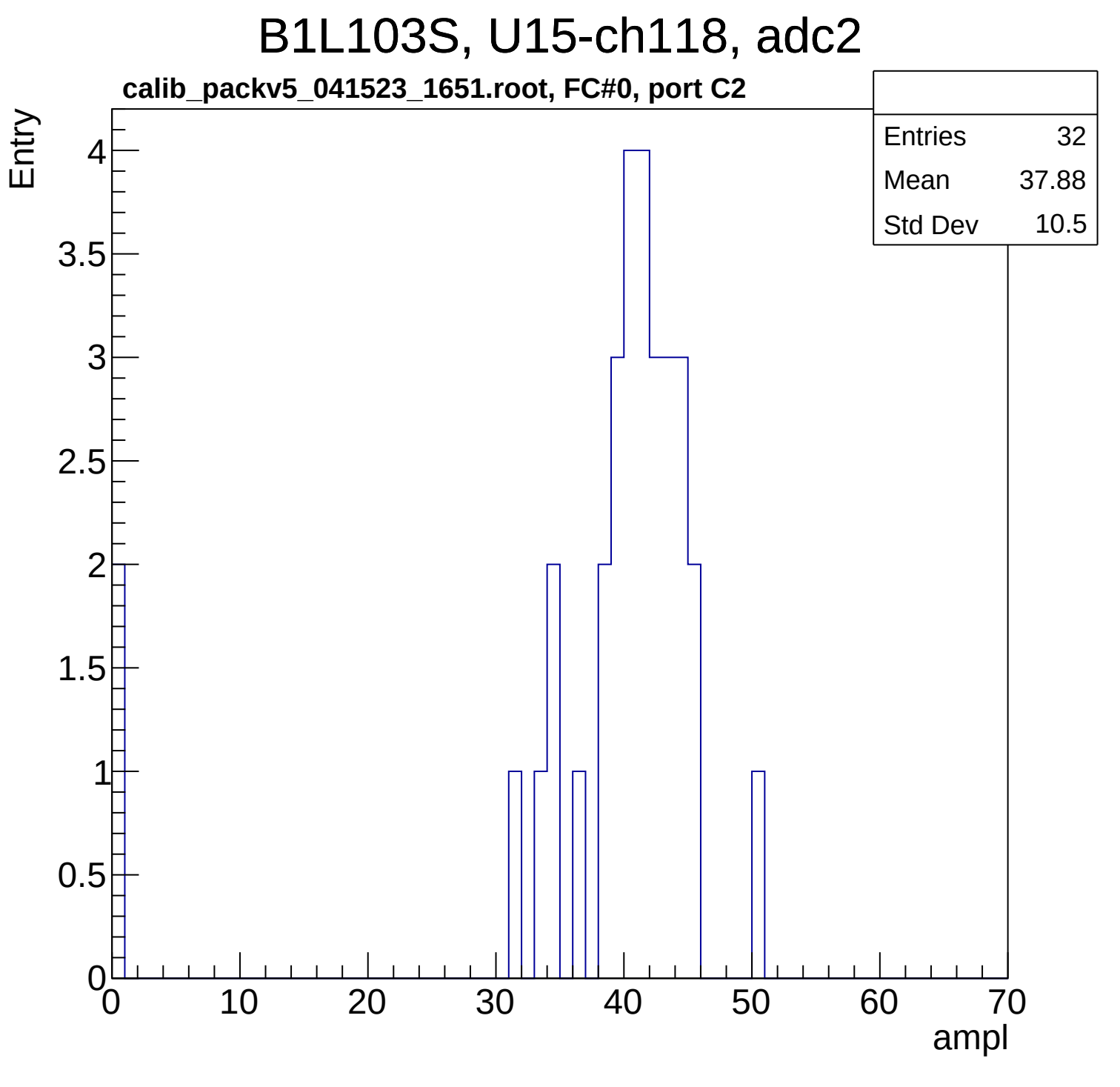

B1L103S, U15-ch117, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 59.83
Std Dev 2.531
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

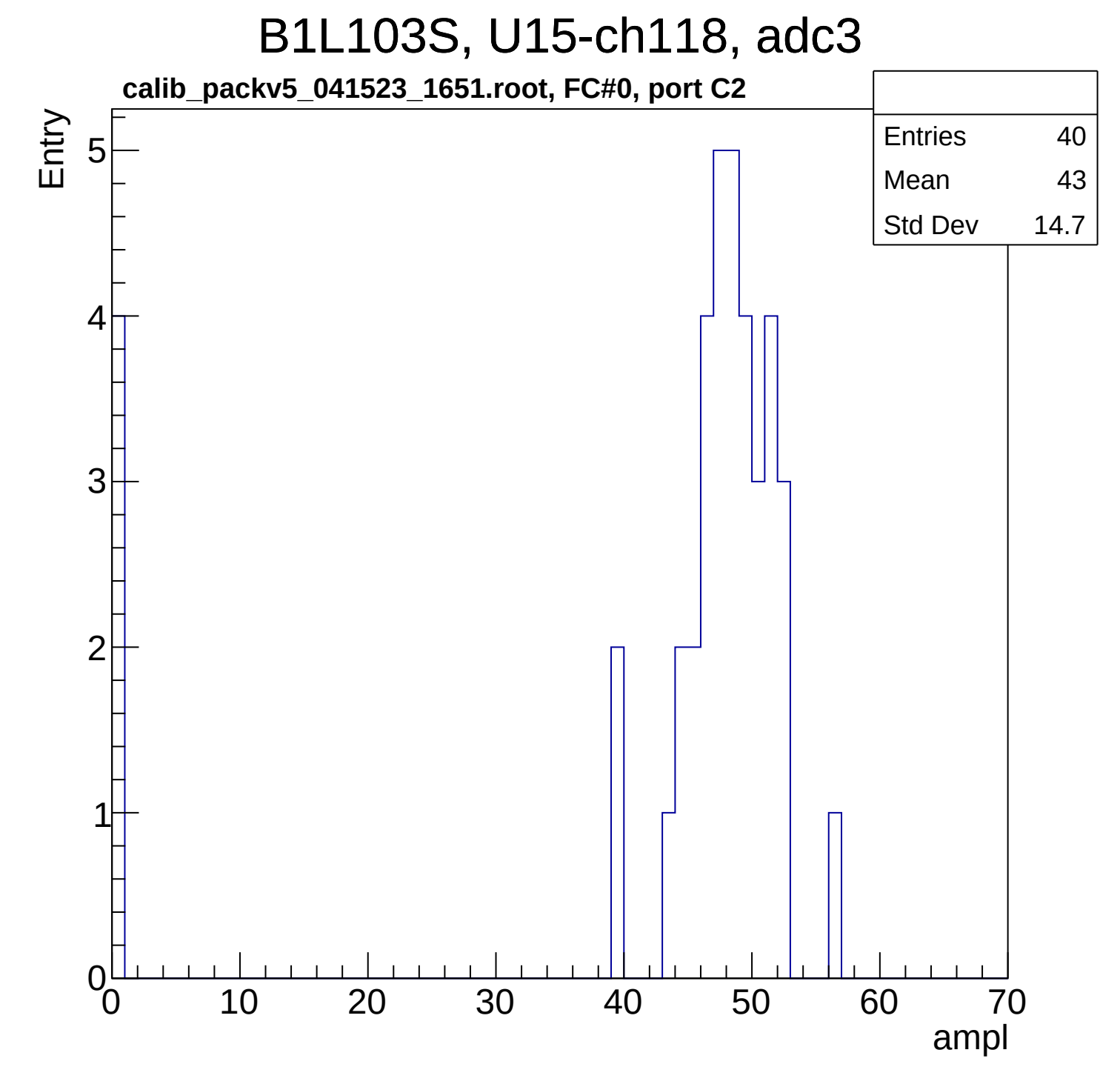

B1L103S, U15-ch117, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62
Std Dev 1
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

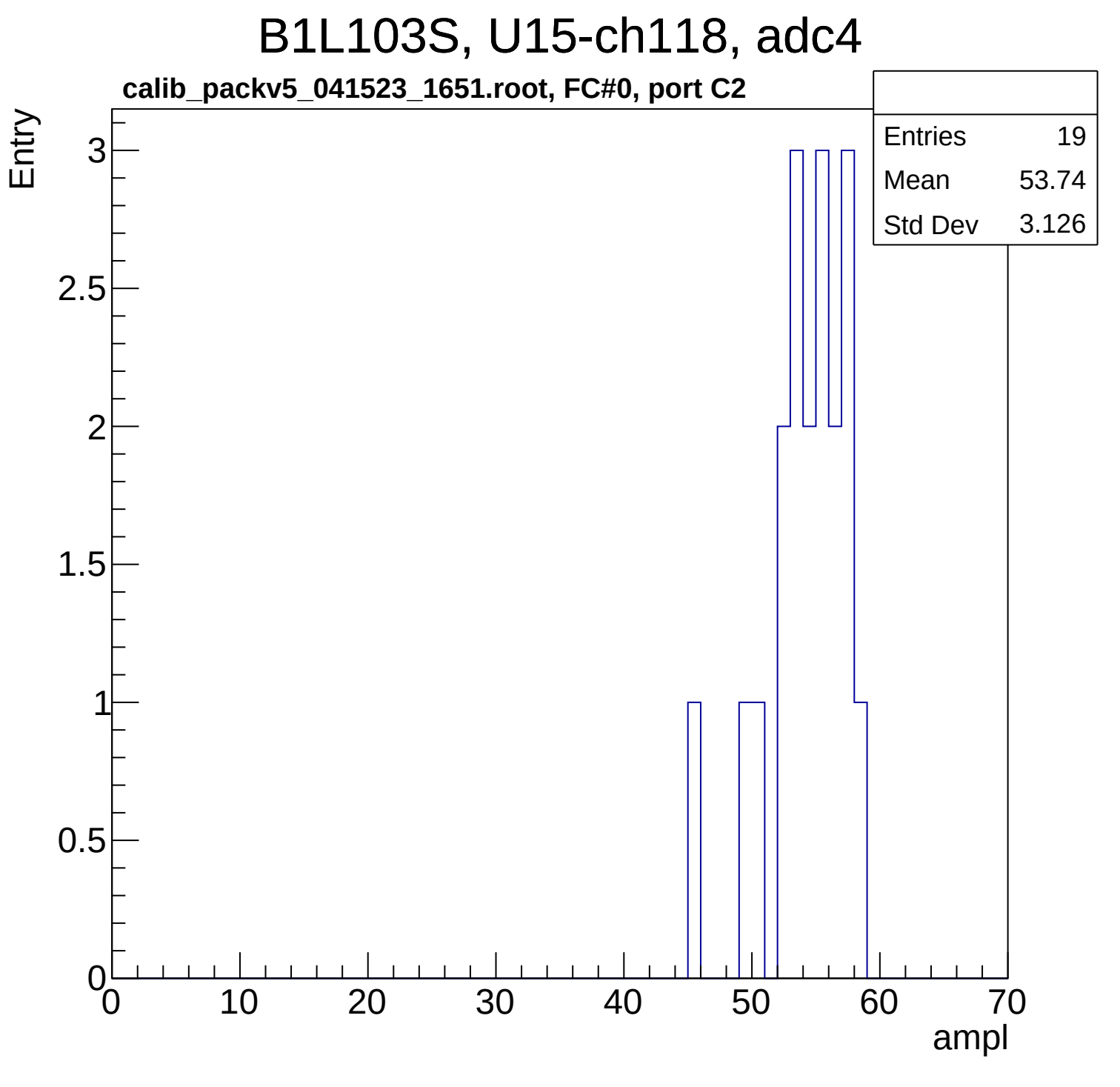

B1L103S, U15-ch117, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

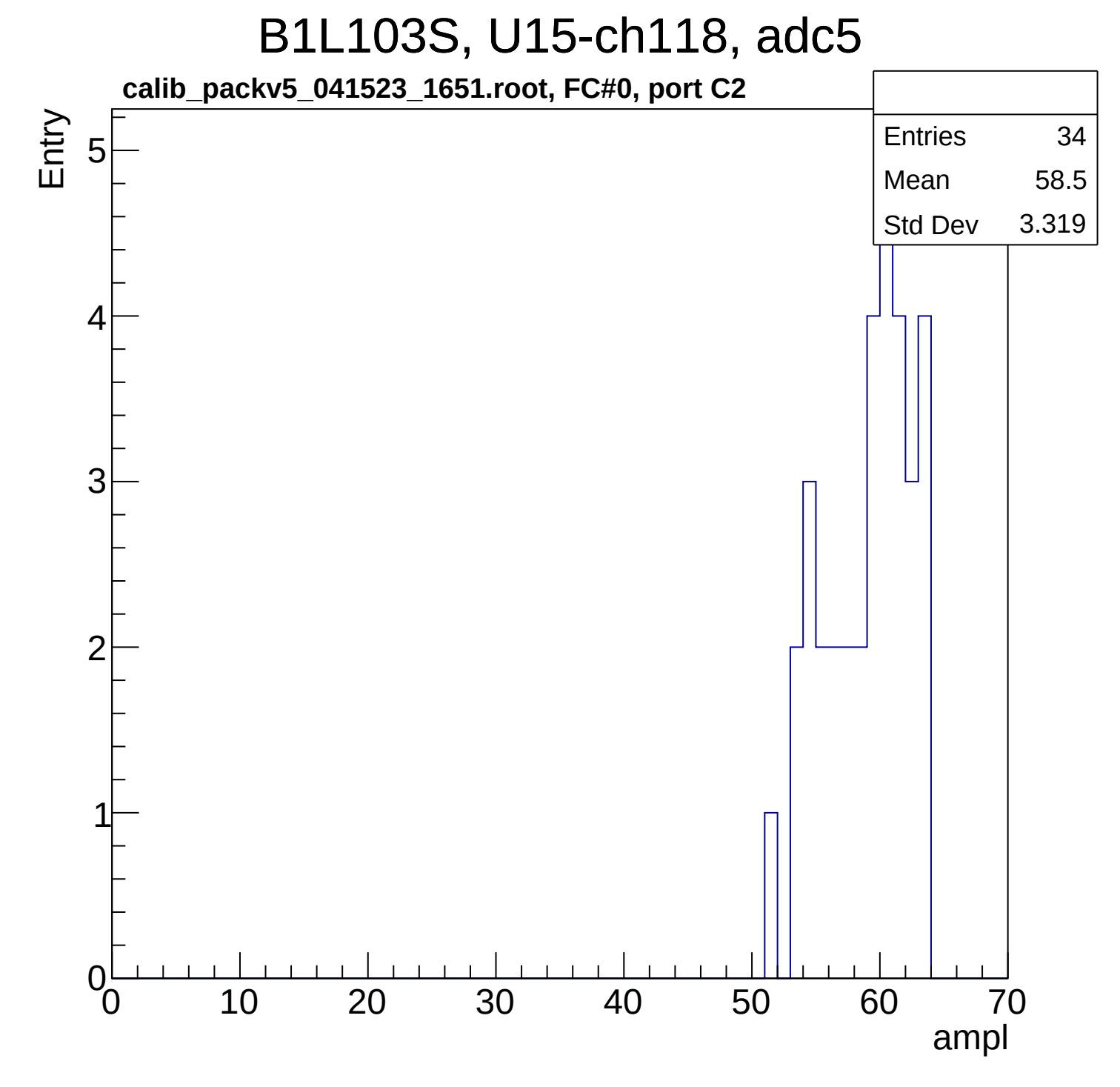

B1L103S, U15-ch118, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 19.54
Std Dev 11.95
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

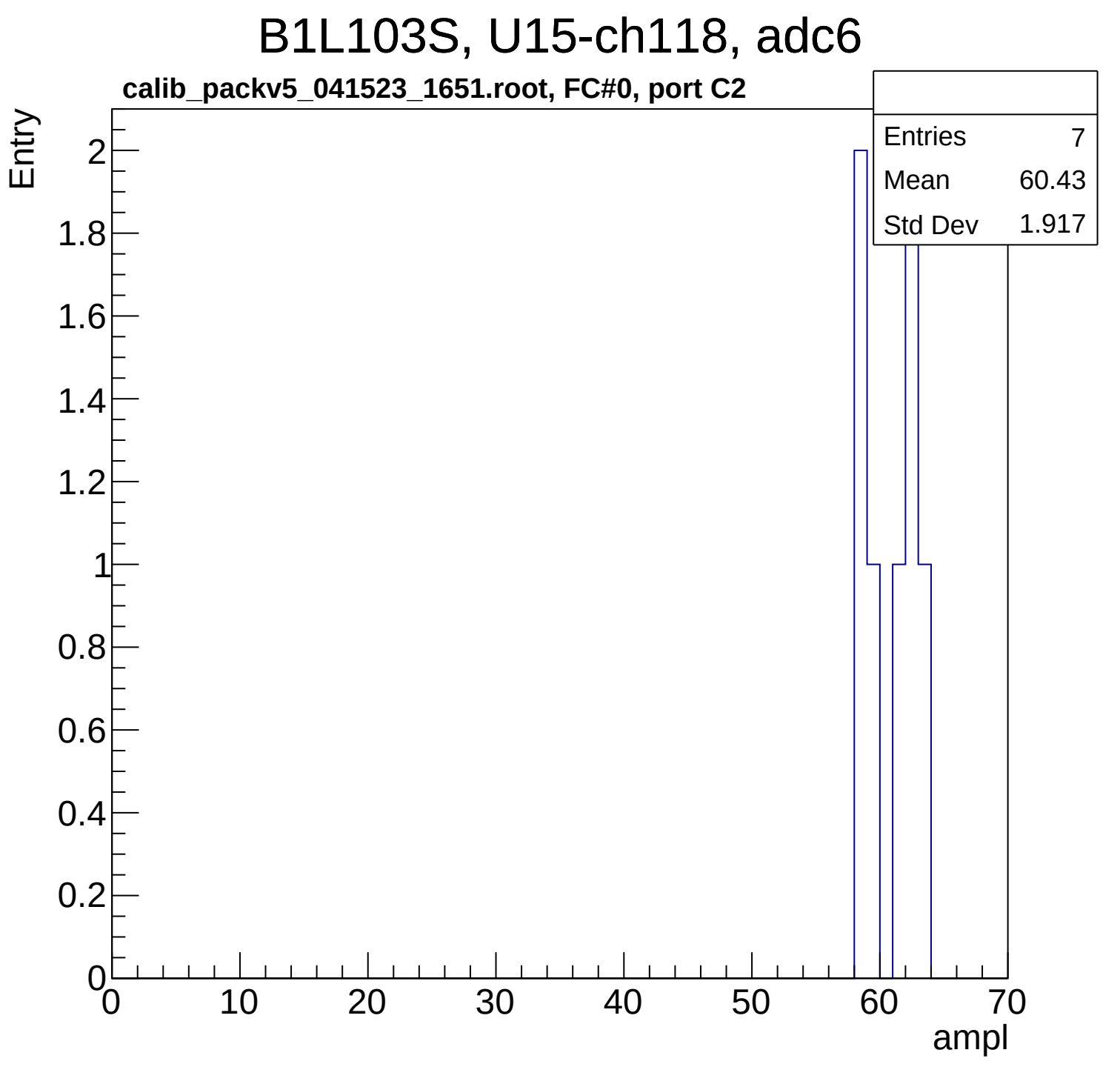

B1L103S, U15-ch118, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 33.33
Std Dev 6.532
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

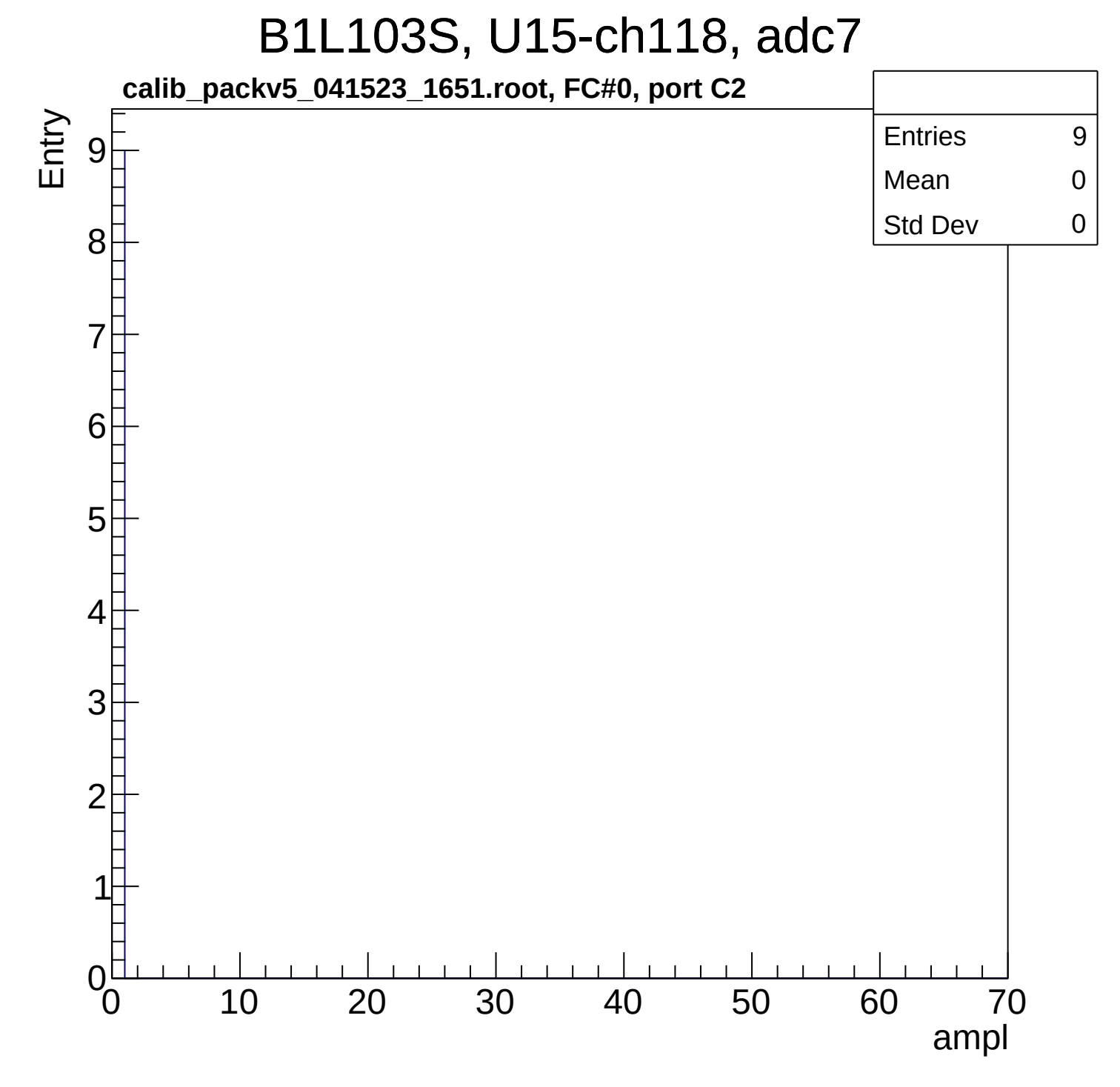

B1L103S, U15-ch118, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 37.88
Std Dev 10.5
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

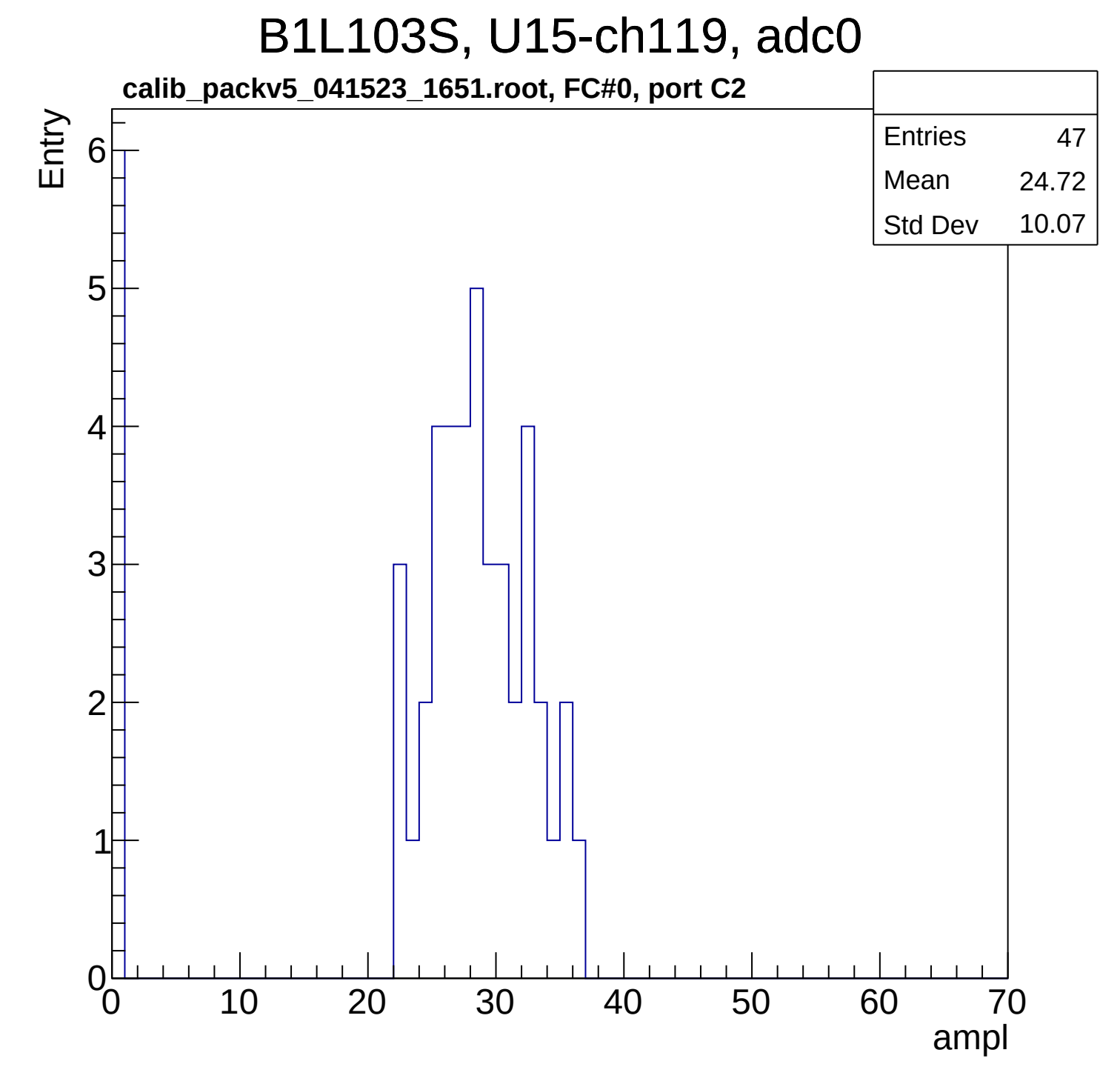

B1L103S, U15-ch118, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 43
Std Dev 14.7
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

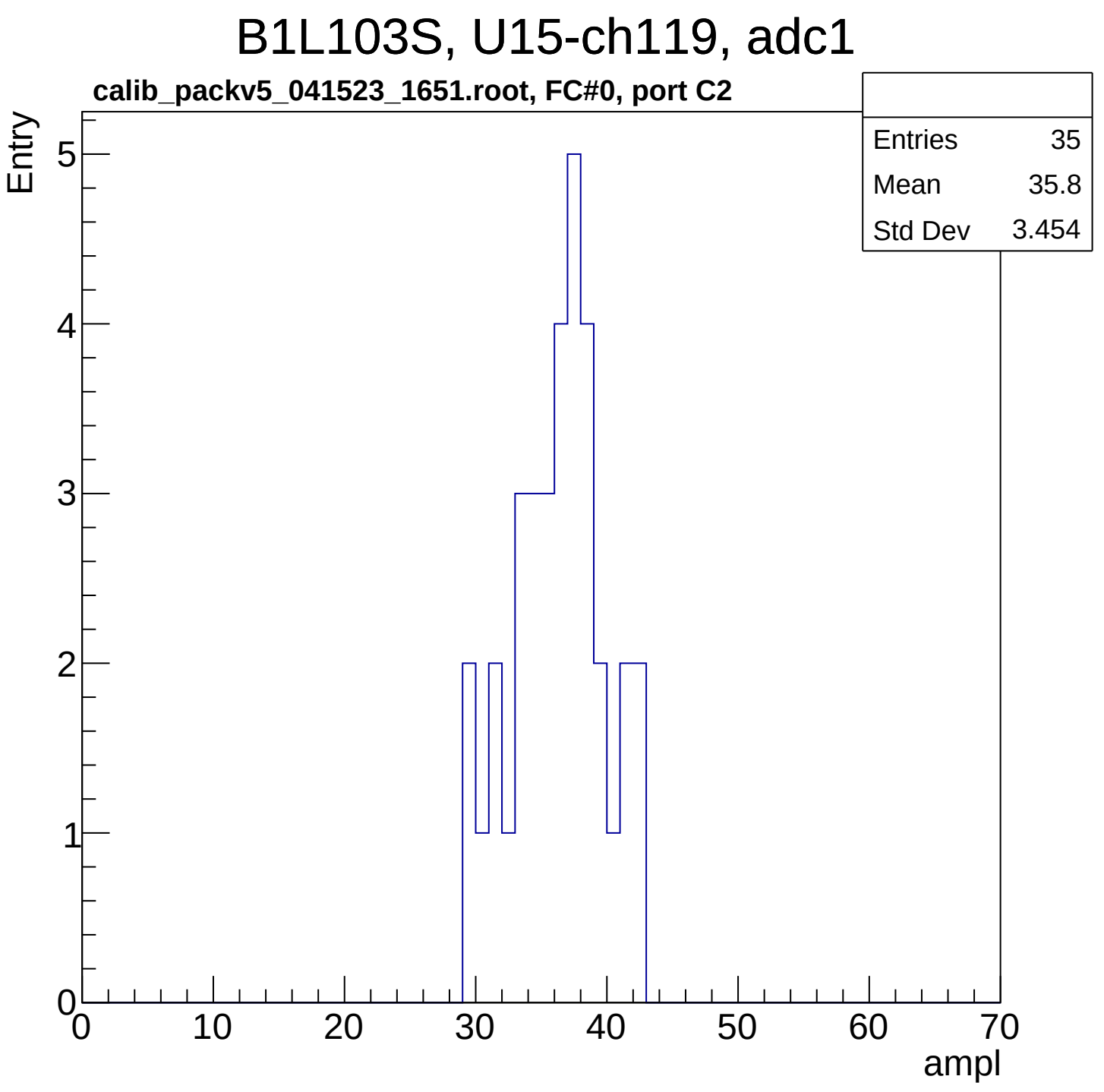

B1L103S, U15-ch118, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 53.74
Std Dev 3.126
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

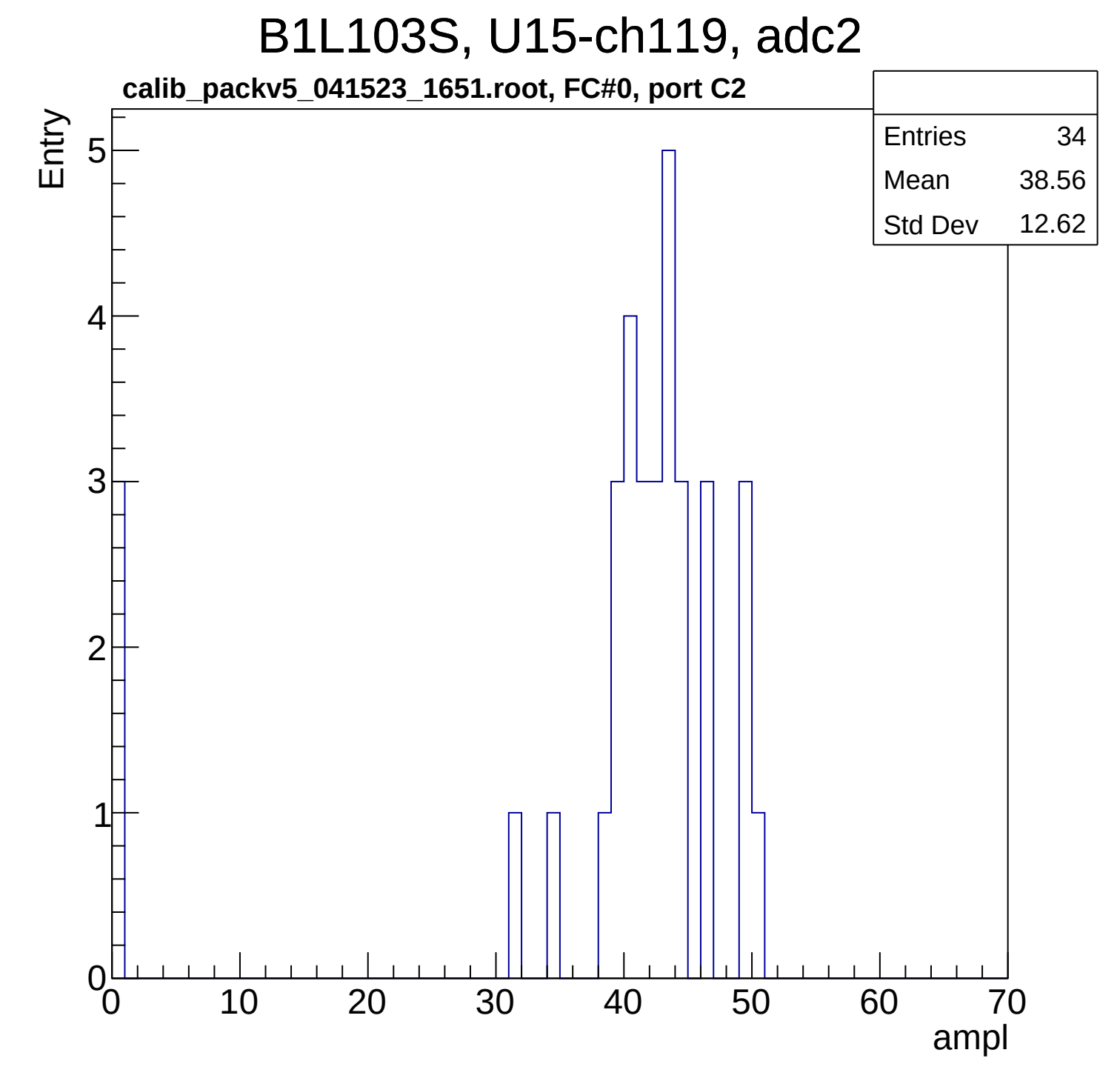

B1L103S, U15-ch118, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 58.5
Std Dev 3.319
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

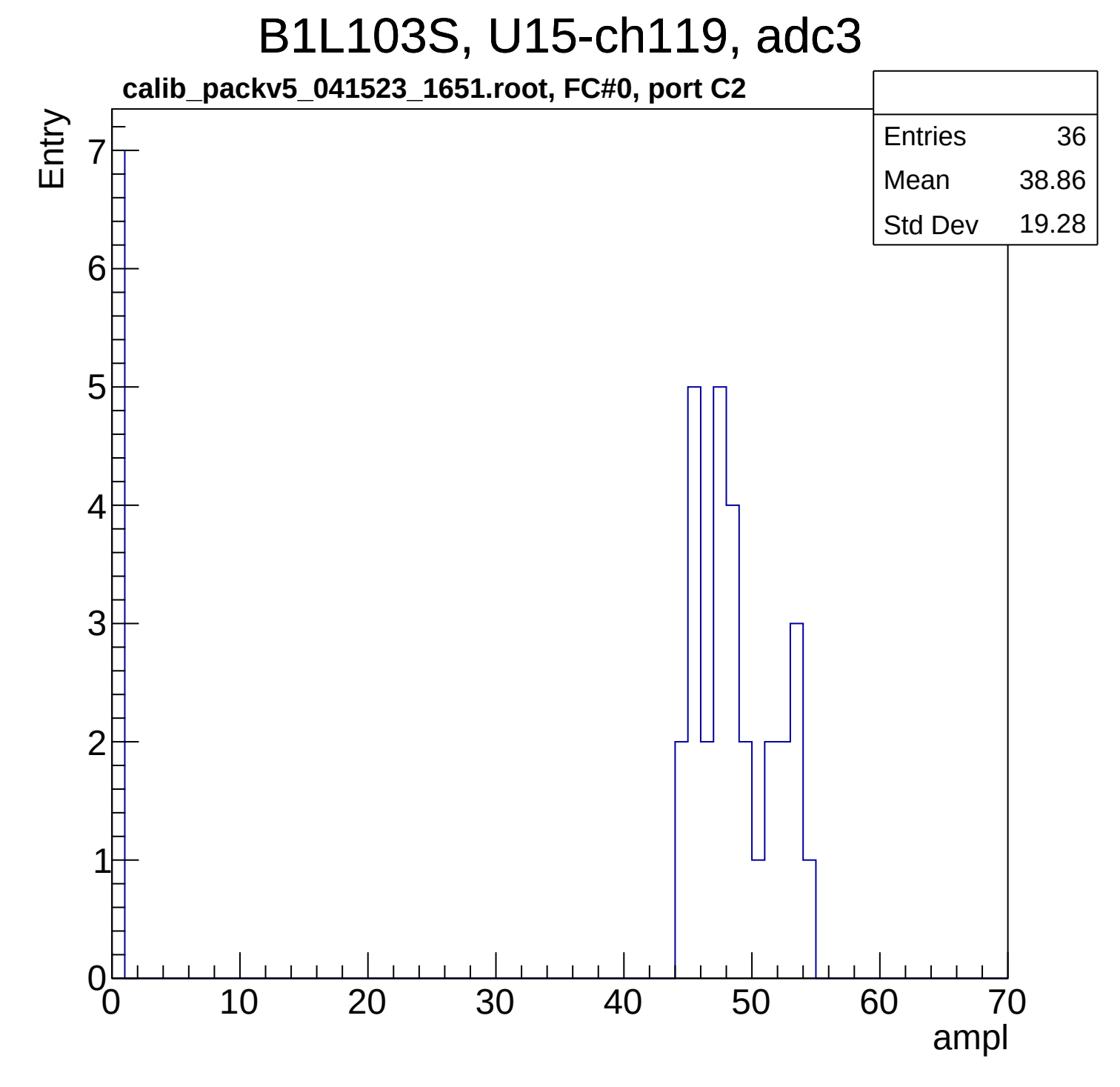

B1L103S, U15-ch118, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 60.43
Std Dev 1.917
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

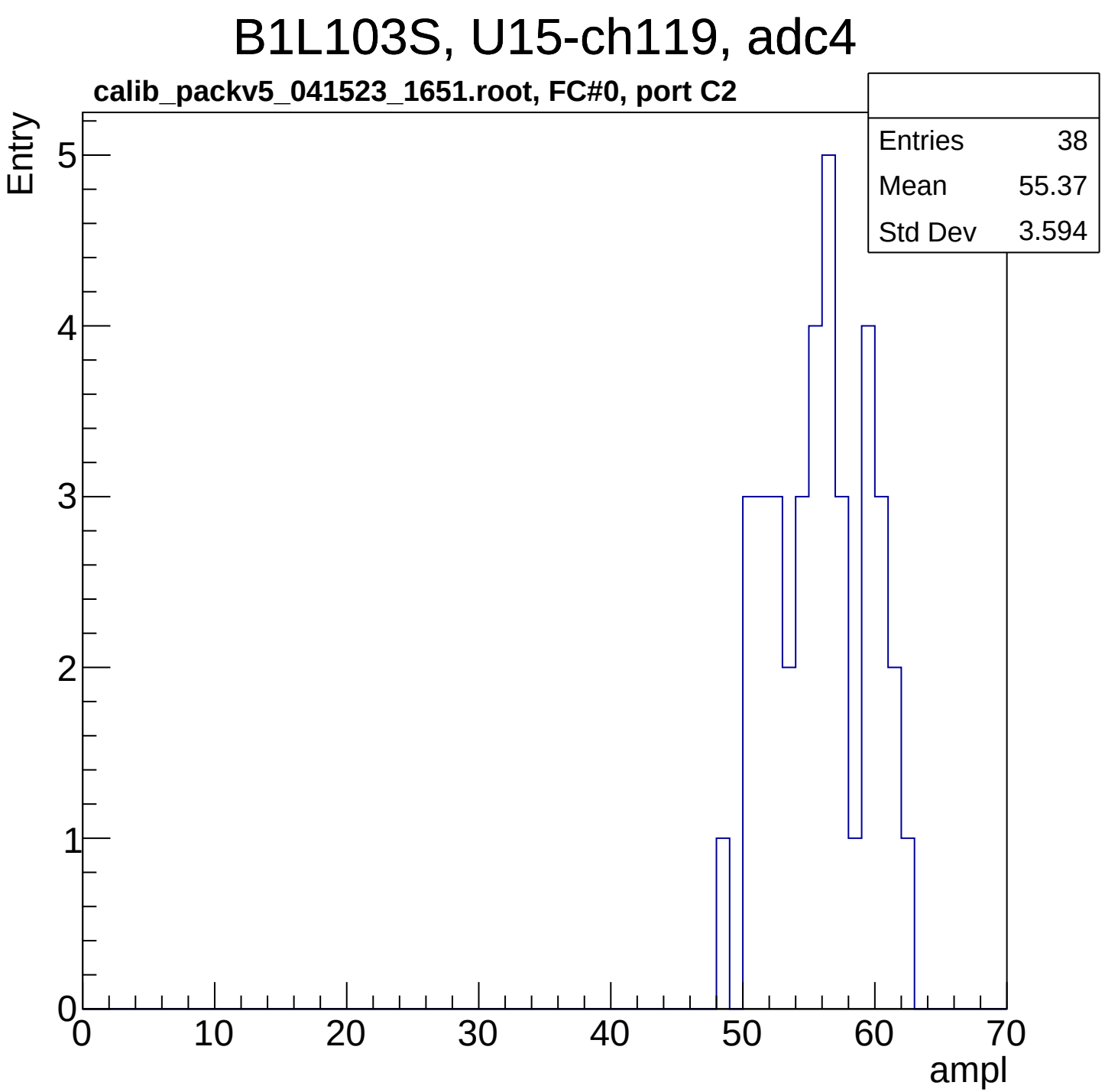

B1L103S, U15-ch118, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 0
Std Dev 0
Entry
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70
ampl

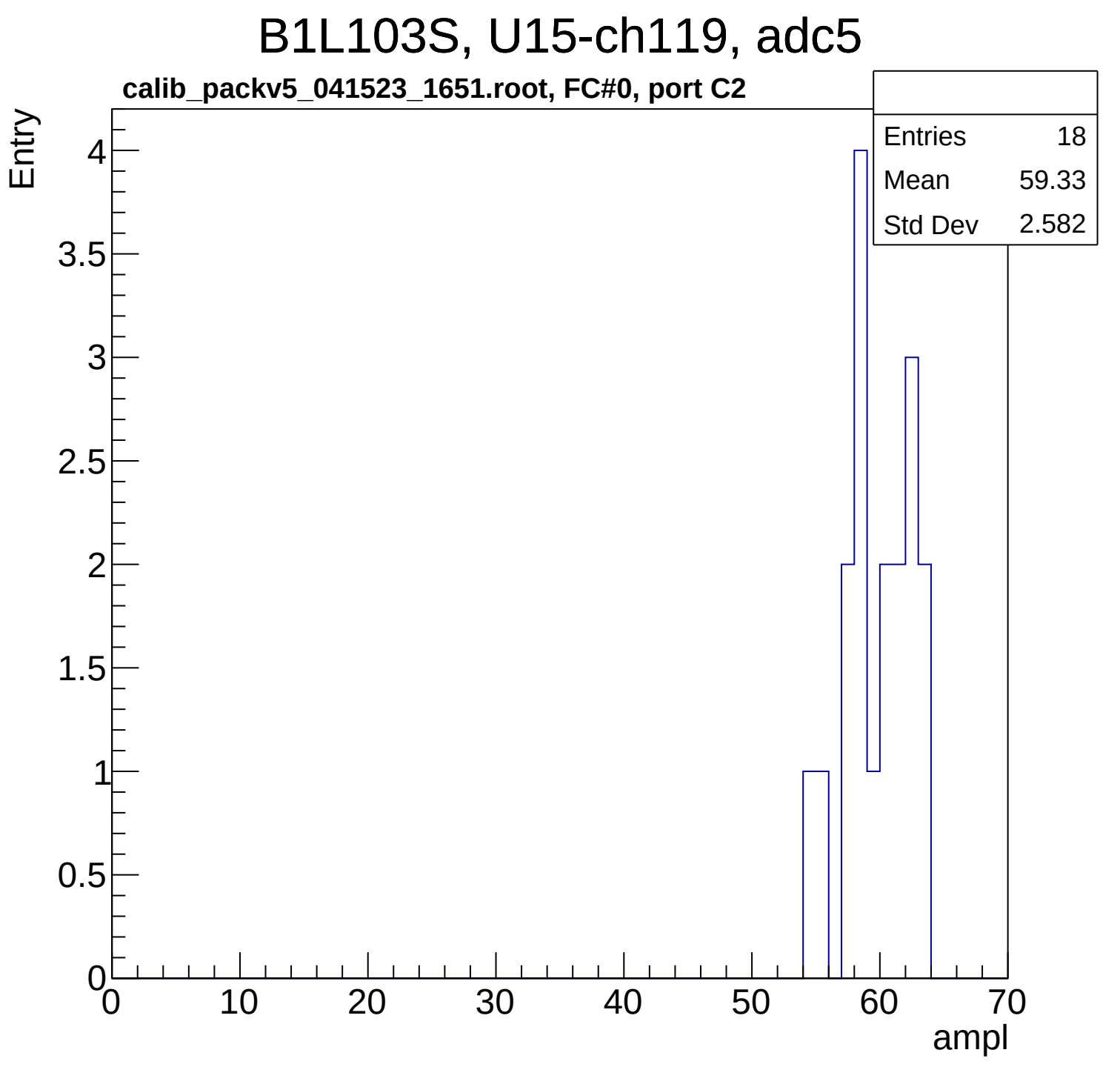

B1L103S, U15-ch119, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 24.72
Std Dev 10.07
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U15-ch119, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 35.8
Std Dev 3.454
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch119, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 38.56
Std Dev 12.62
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch119, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 38.86
Std Dev 19.28
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U15-ch119, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 55.37
Std Dev 3.594
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch119, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 59.33
Std Dev 2.582
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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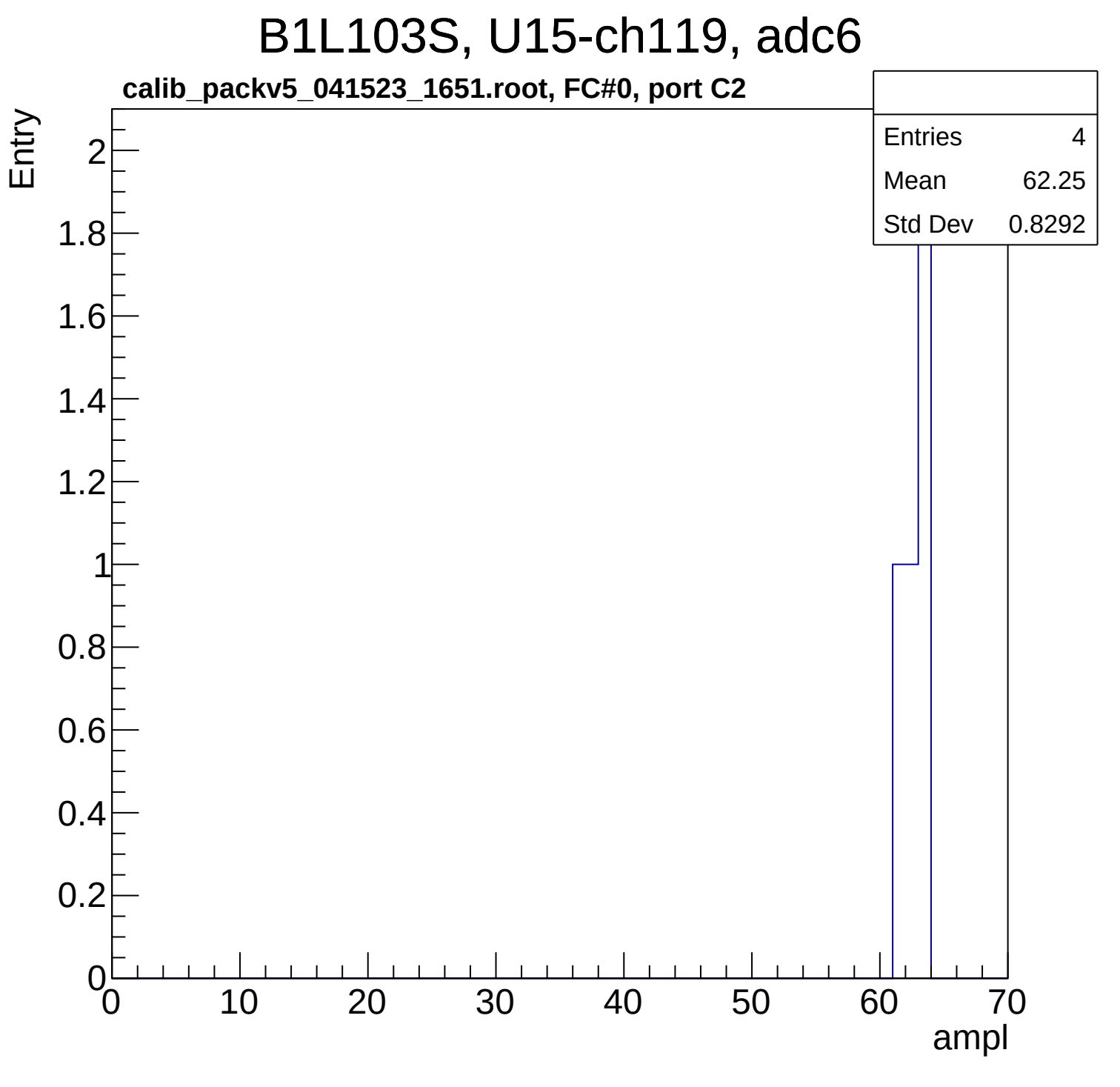
B1L103S, U15-ch119, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
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30
40
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60
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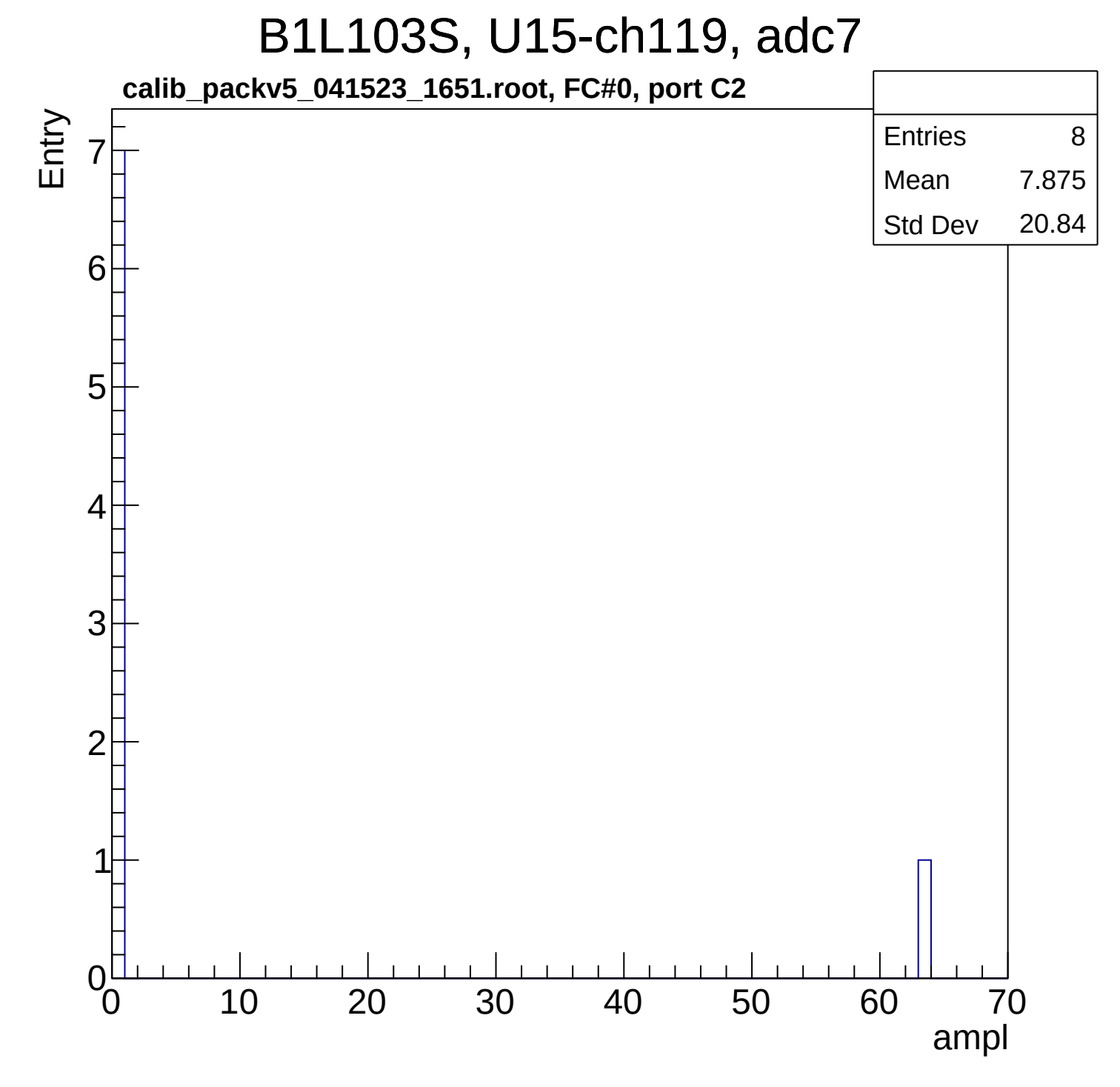
B1L103S, U15-ch119, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 7.875
Std Dev 20.84
Entry
ampl
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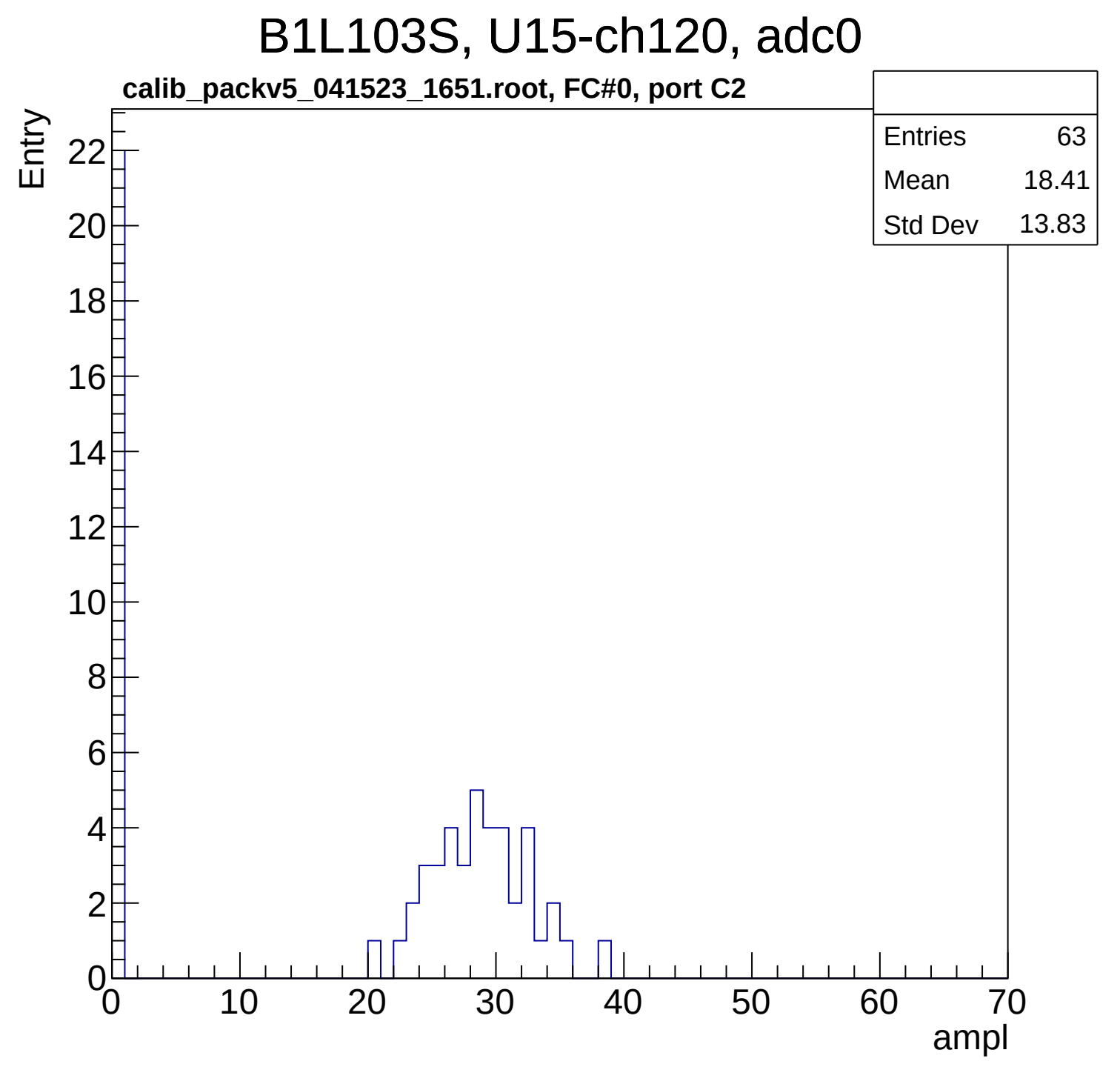
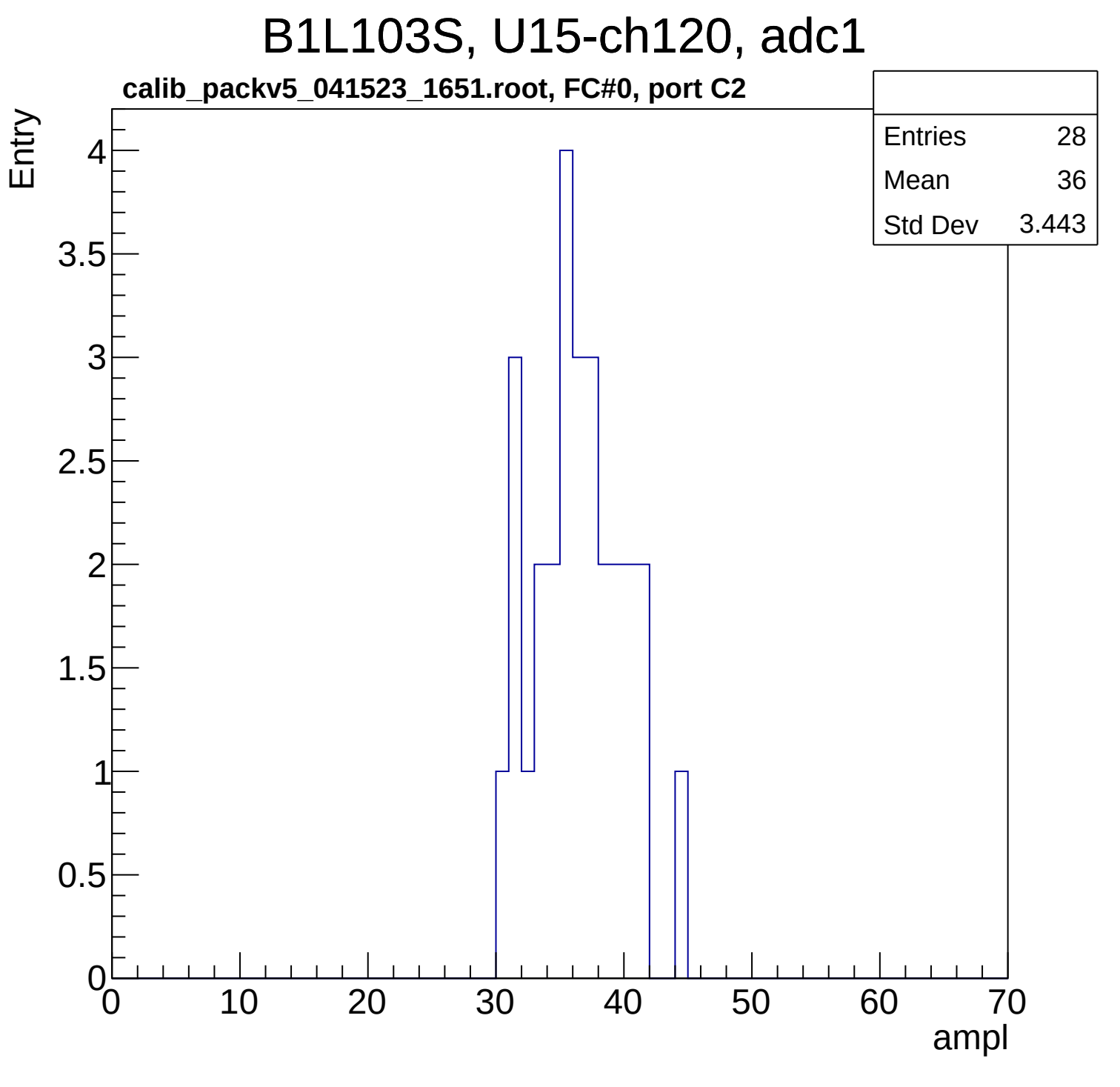
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U15-ch120, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 18.41
Std Dev 13.83
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U15-ch120, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 36
Std Dev 3.443
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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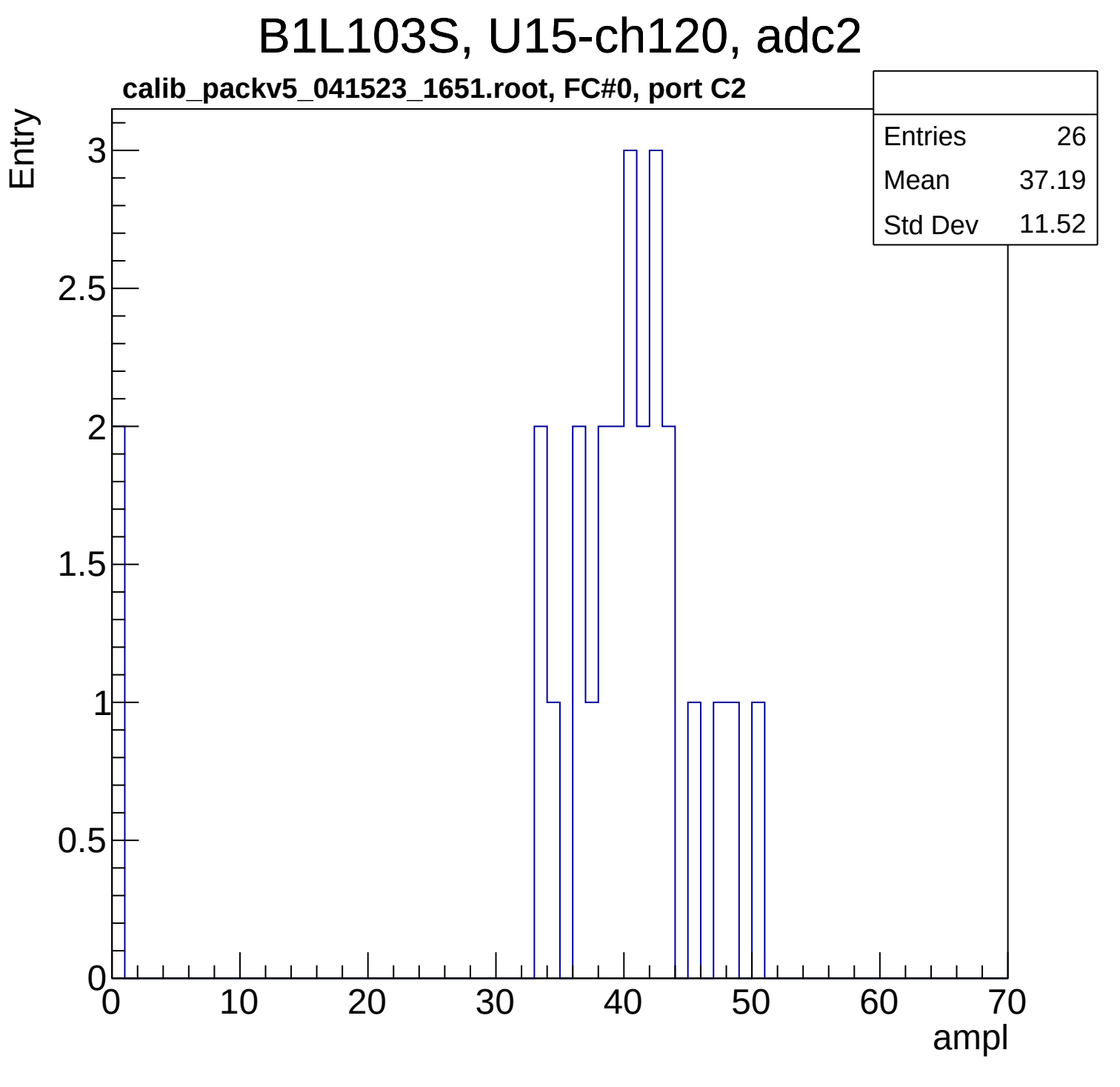
B1L103S, U15-ch120, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 37.19
Std Dev 11.52
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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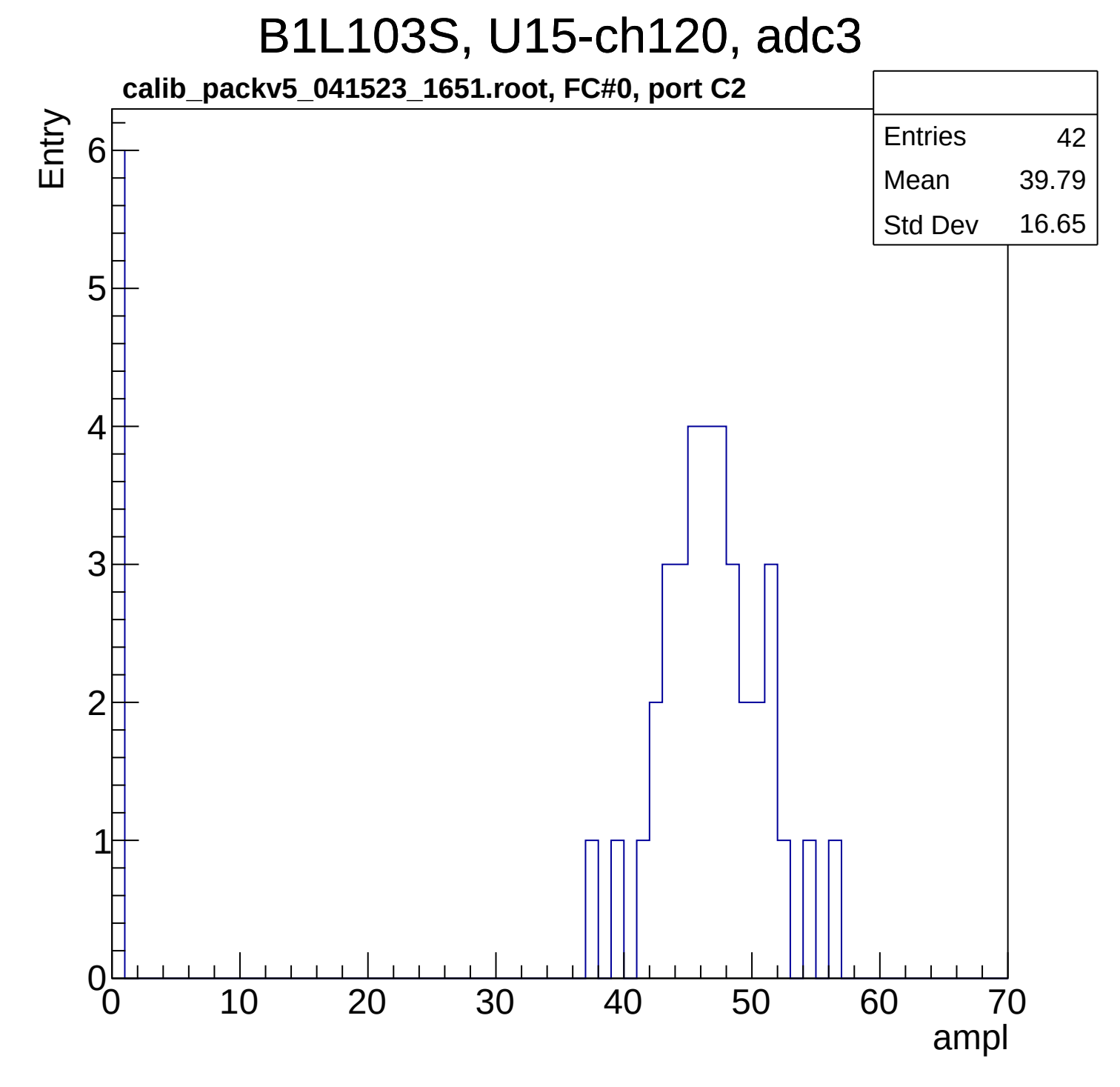
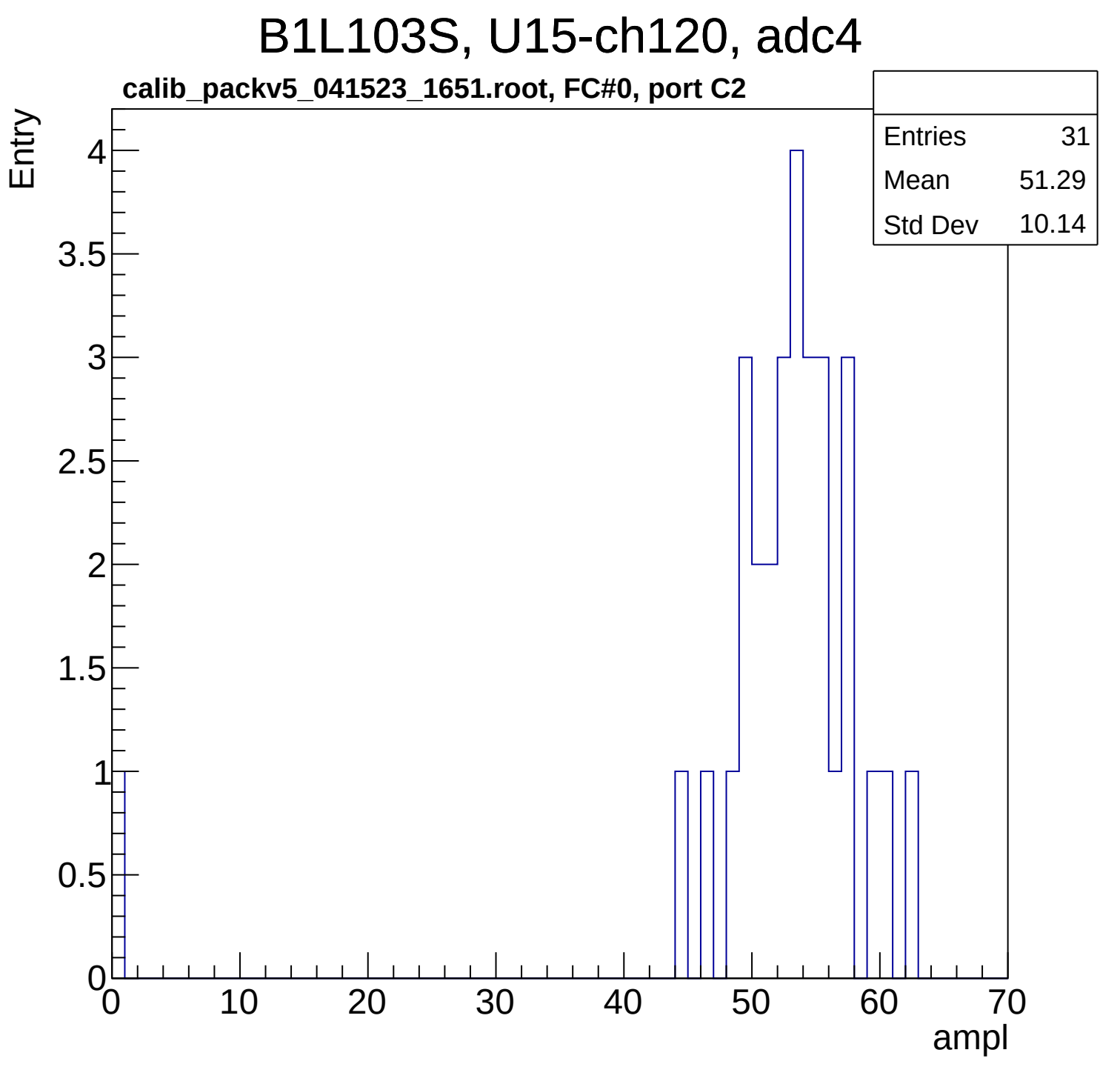

B1L103S, U15-ch120, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 39.79
Std Dev 16.65
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch120, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 51.29
Std Dev 10.14
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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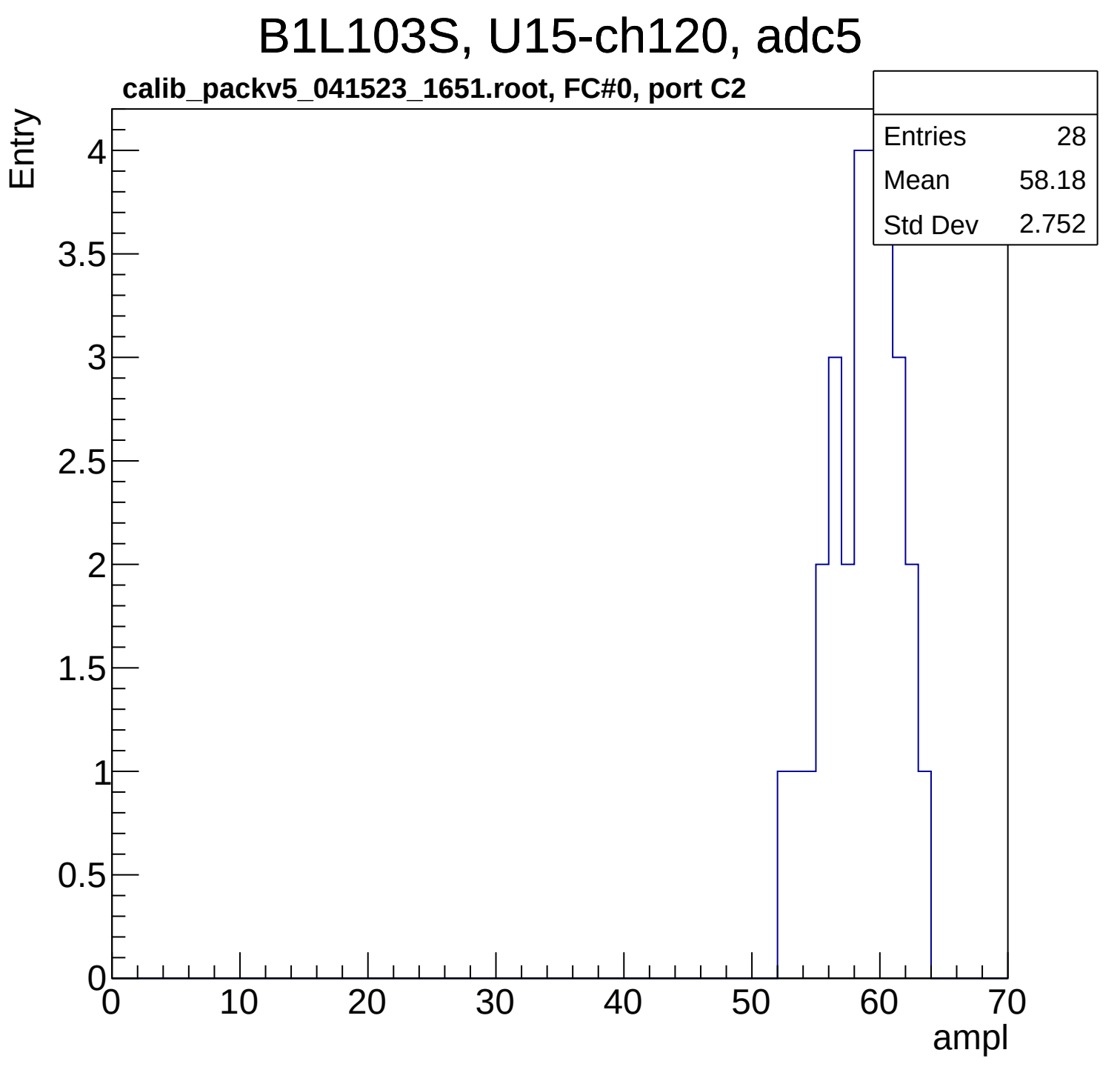
B1L103S, U15-ch120, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 58.18
Std Dev 2.752
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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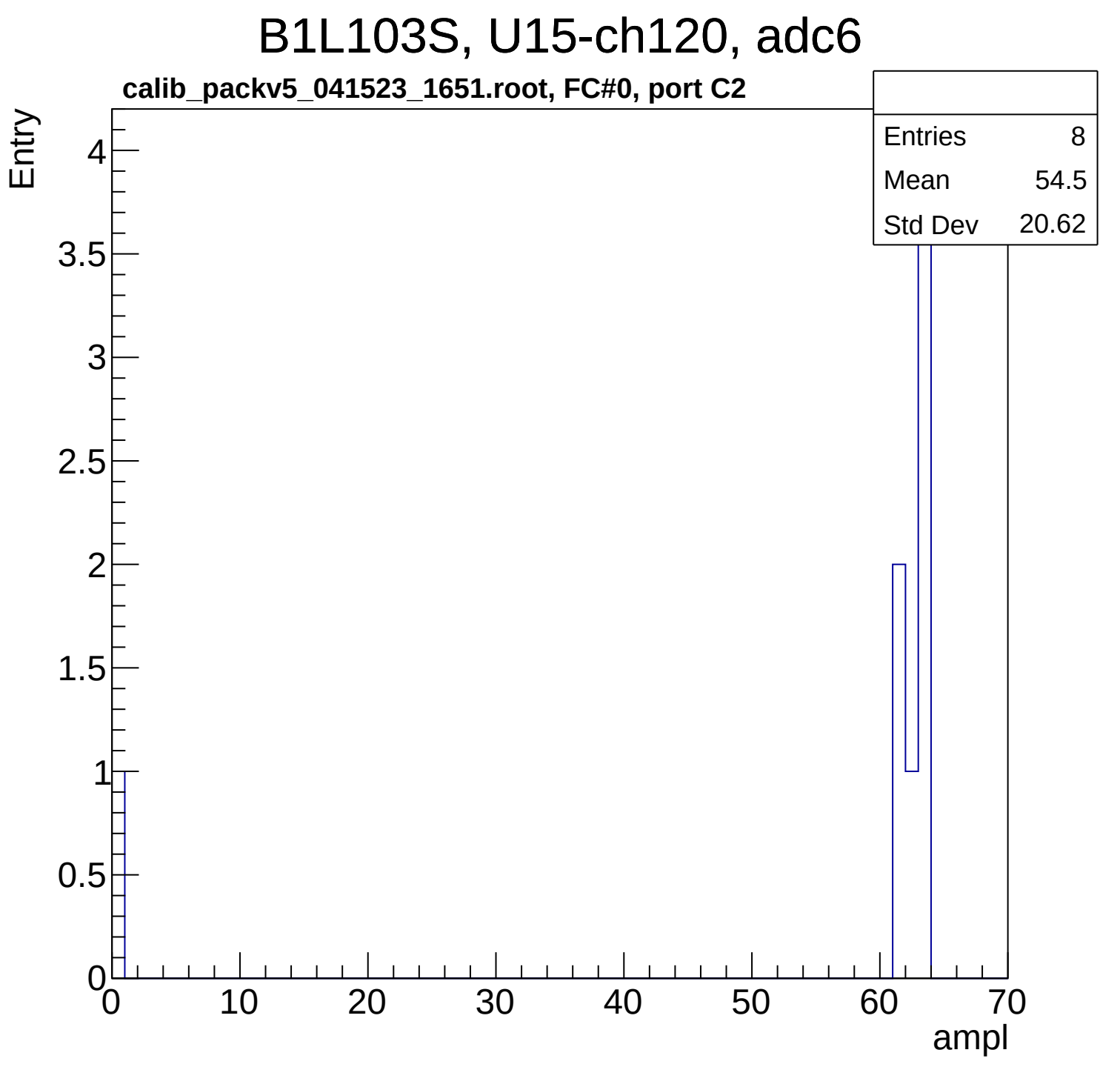
B1L103S, U15-ch120, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 54.5
Std Dev 20.62
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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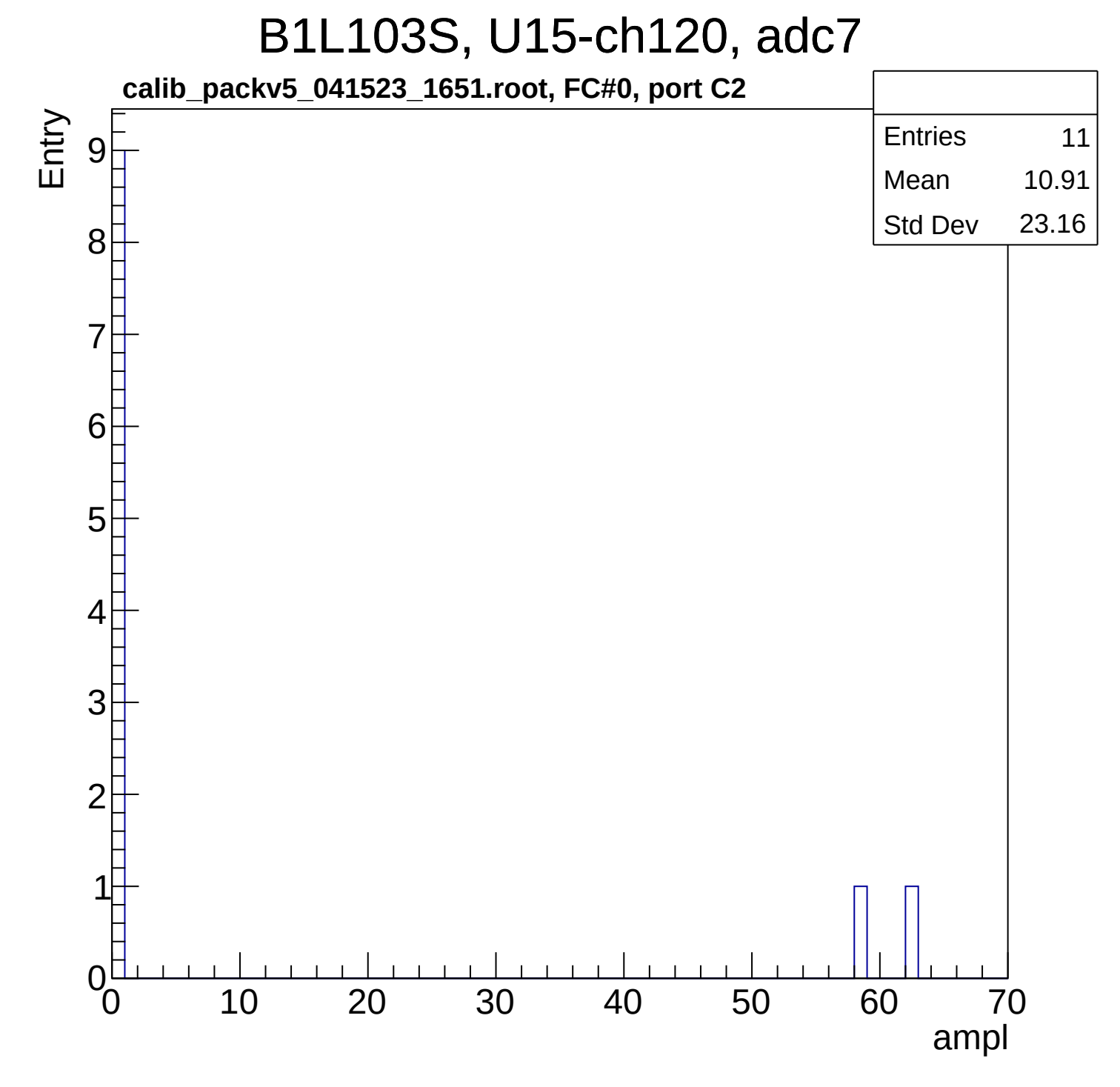
B1L103S, U15-ch120, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 10.91
Std Dev 23.16
Entry
ampl
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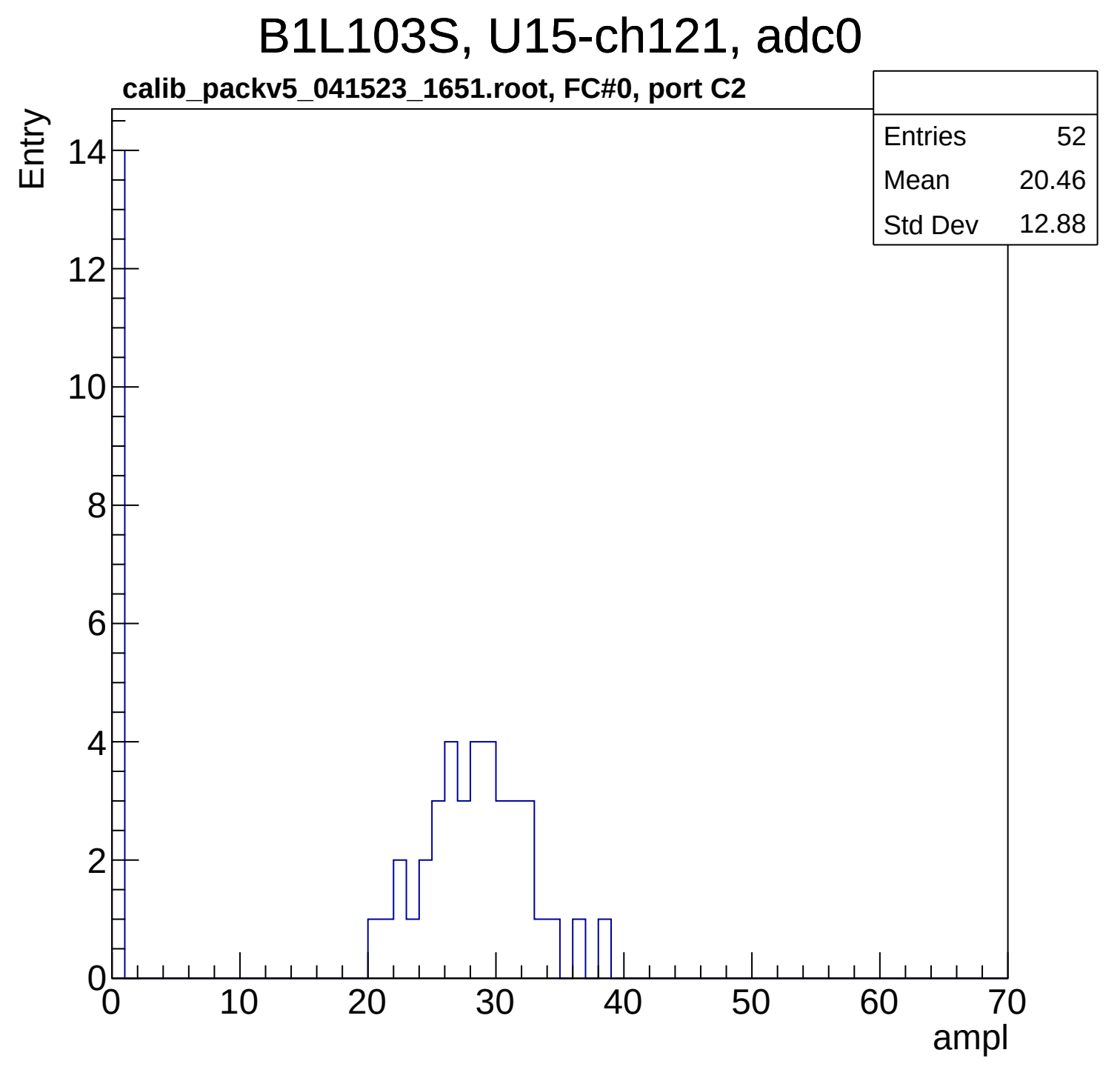
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U15-ch121, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 20.46
Std Dev 12.88
Entry
ampl
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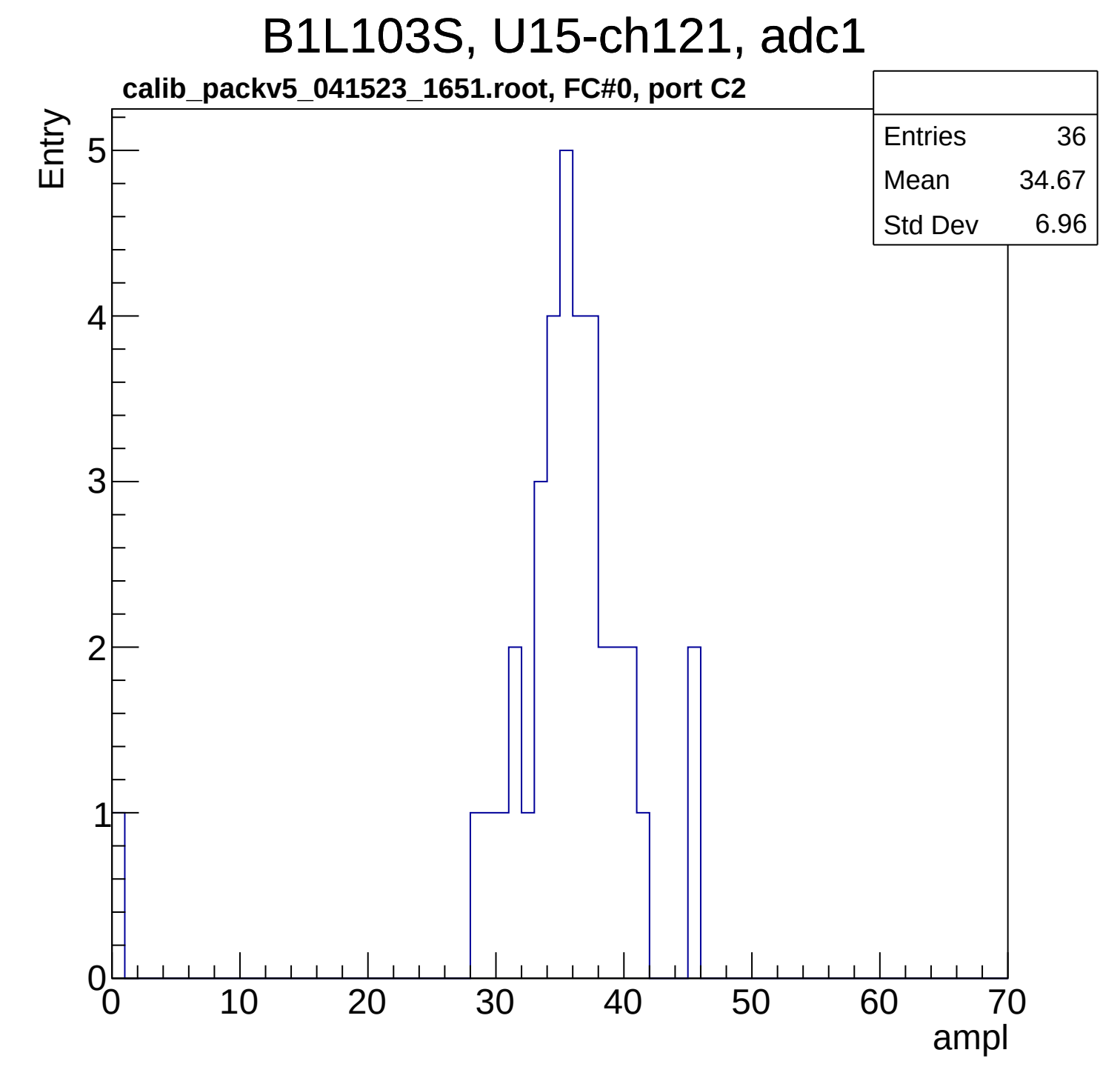
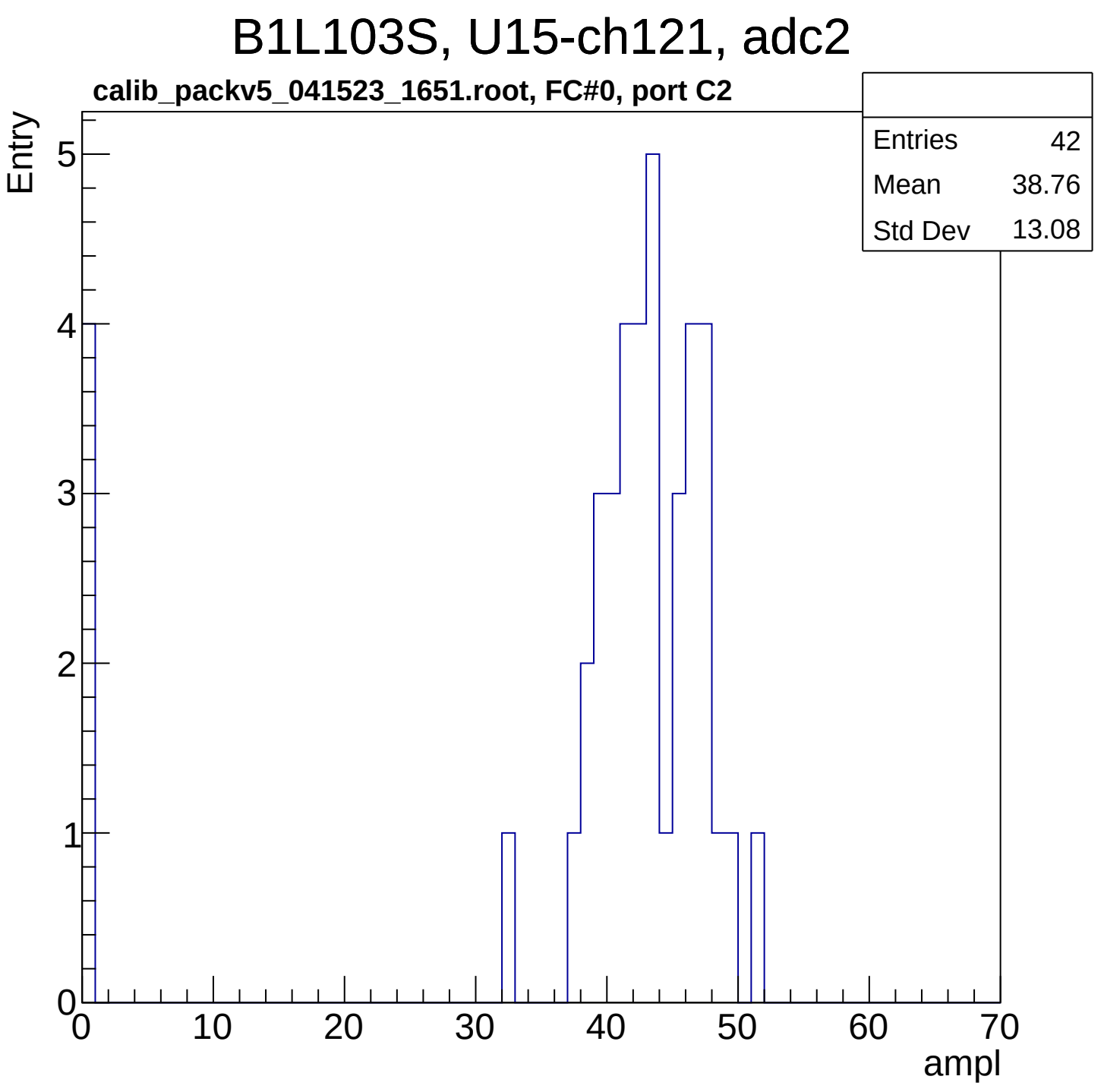
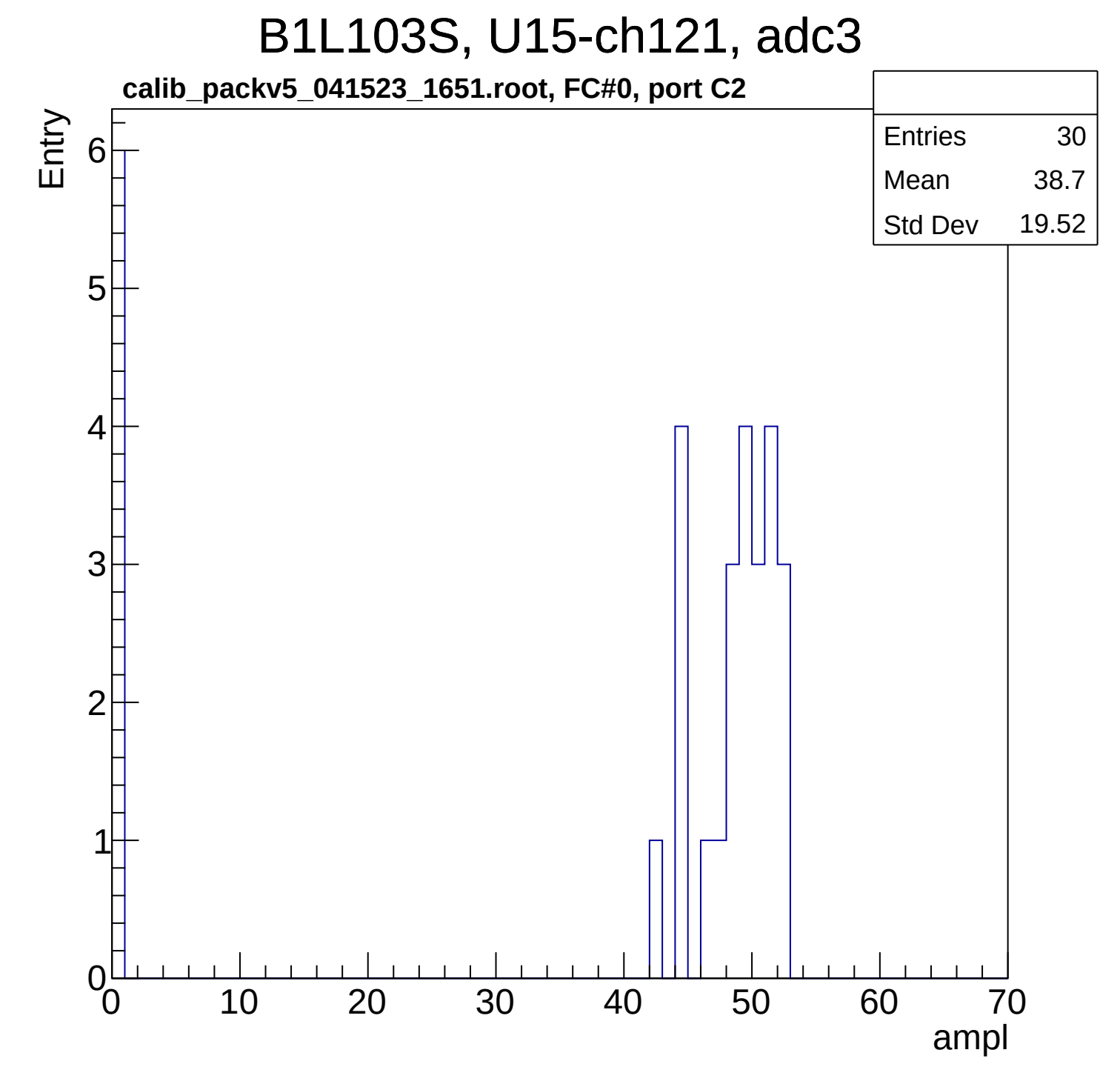
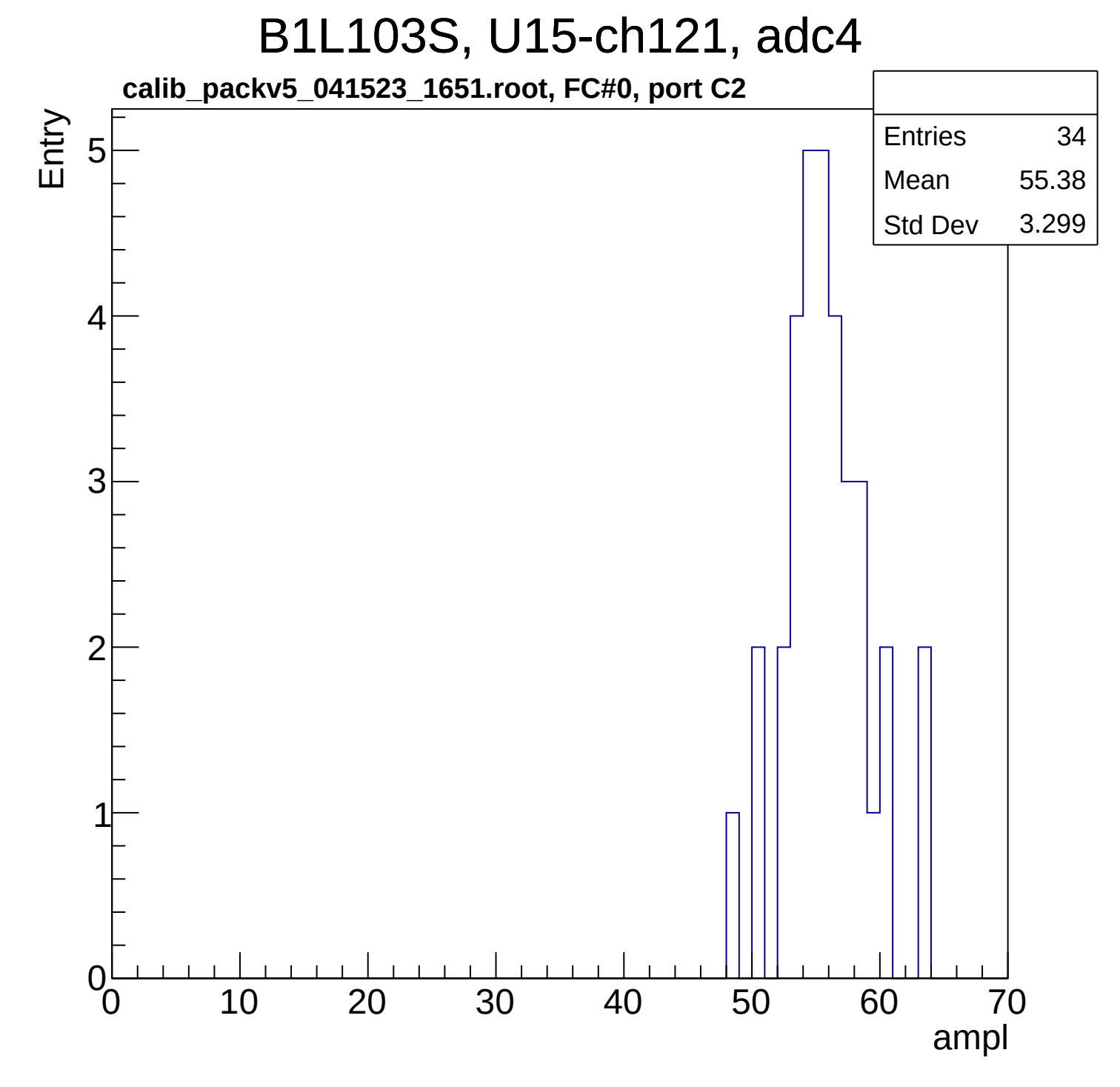
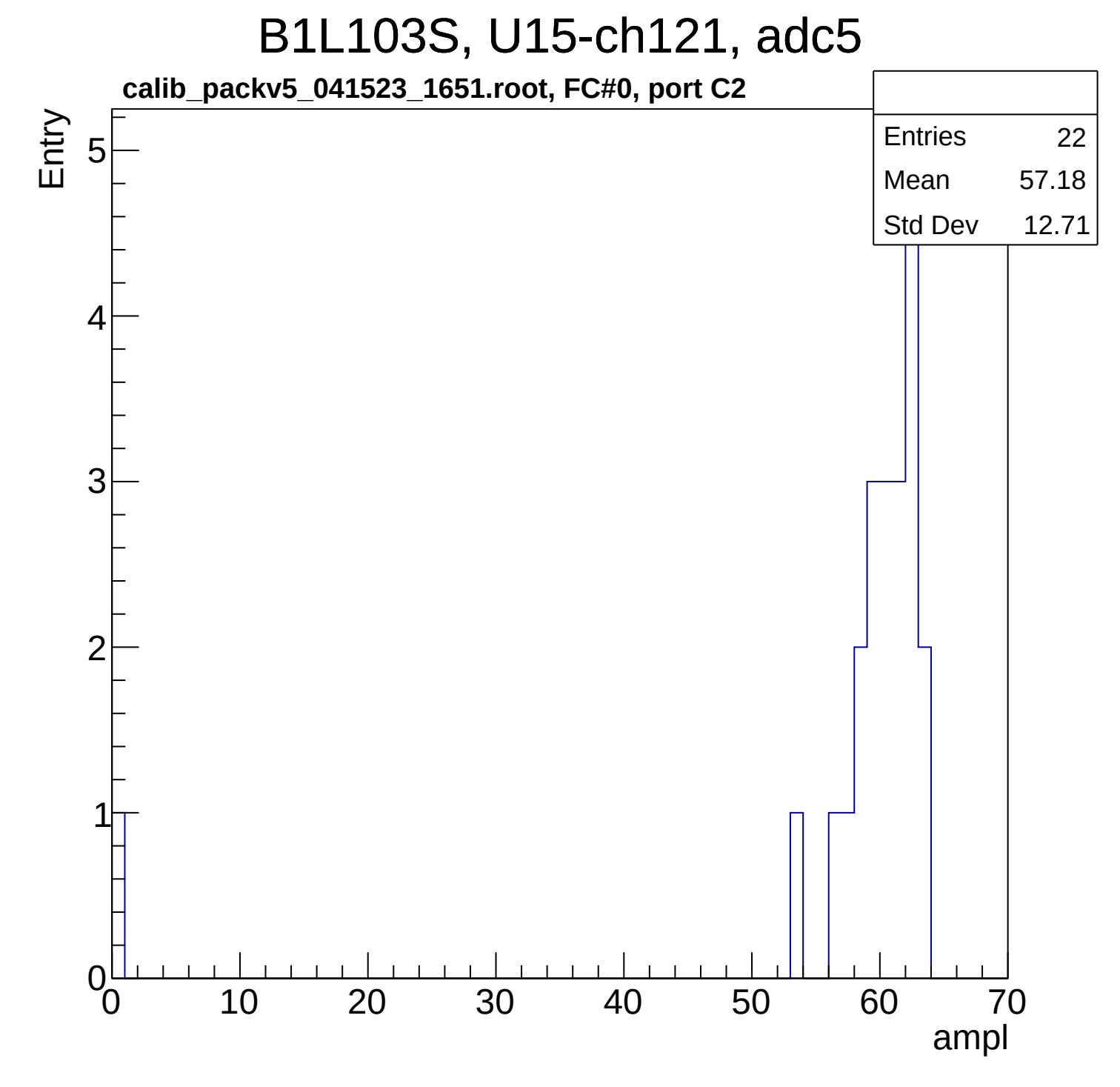
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

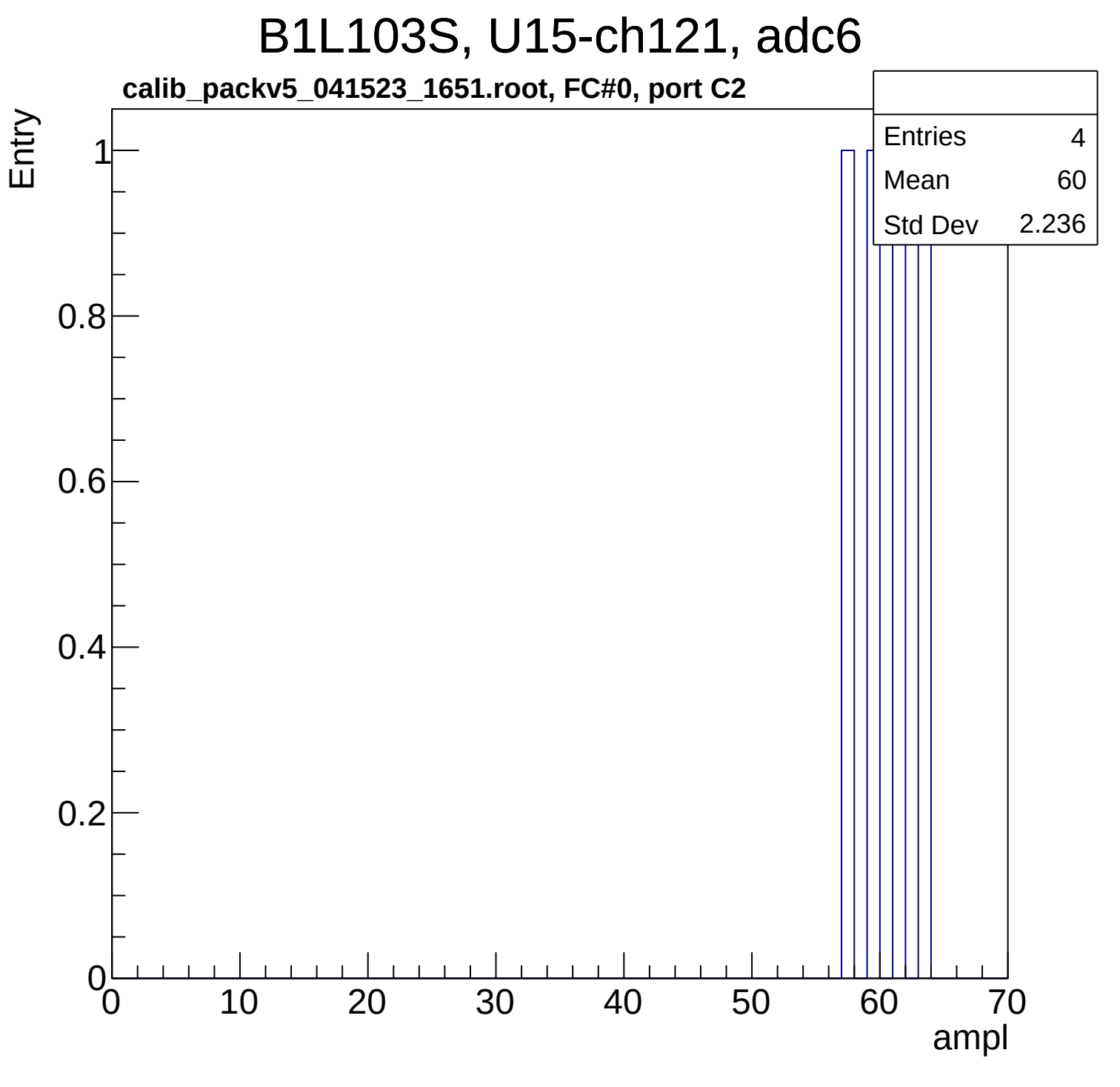

B1L103S, U15-ch121, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 34.67
Std Dev 6.96
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch121, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 38.76
Std Dev 13.08
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch121, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 38.7
Std Dev 19.52
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U15-ch121, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 55.38
Std Dev 3.299
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch121, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 57.18
Std Dev 12.71
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch121, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 60
Std Dev 2.236
Entry
ampl
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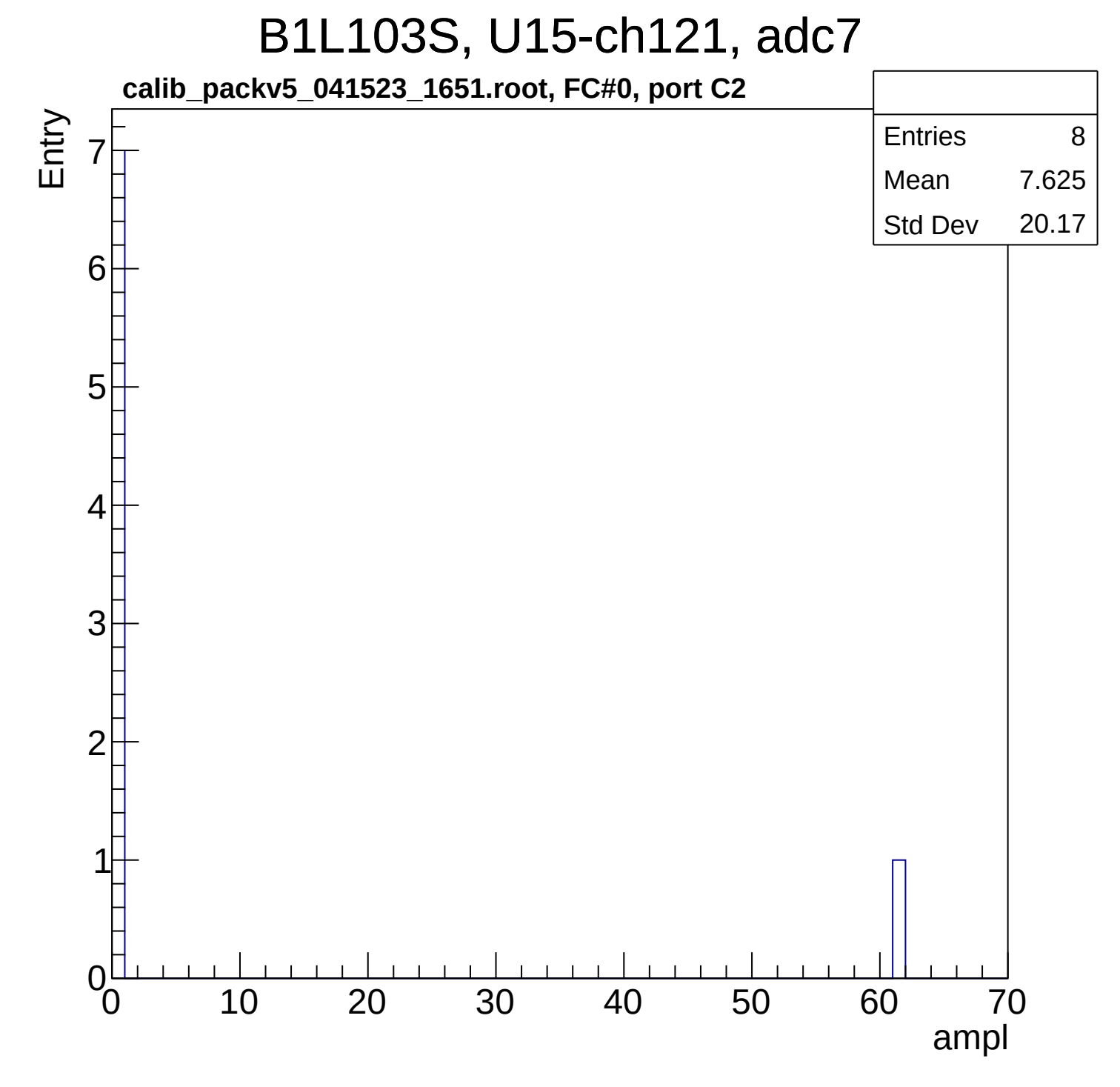
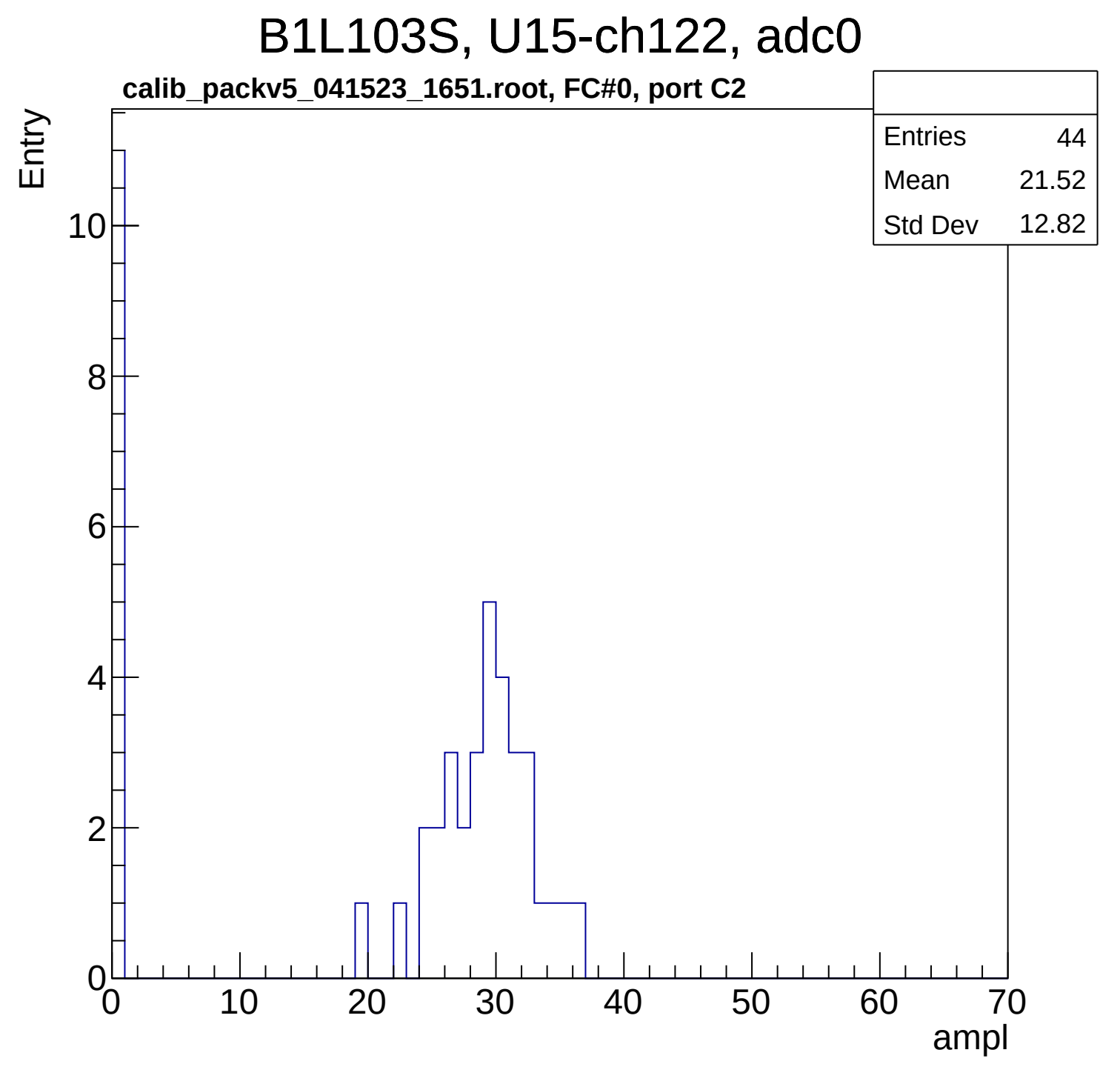
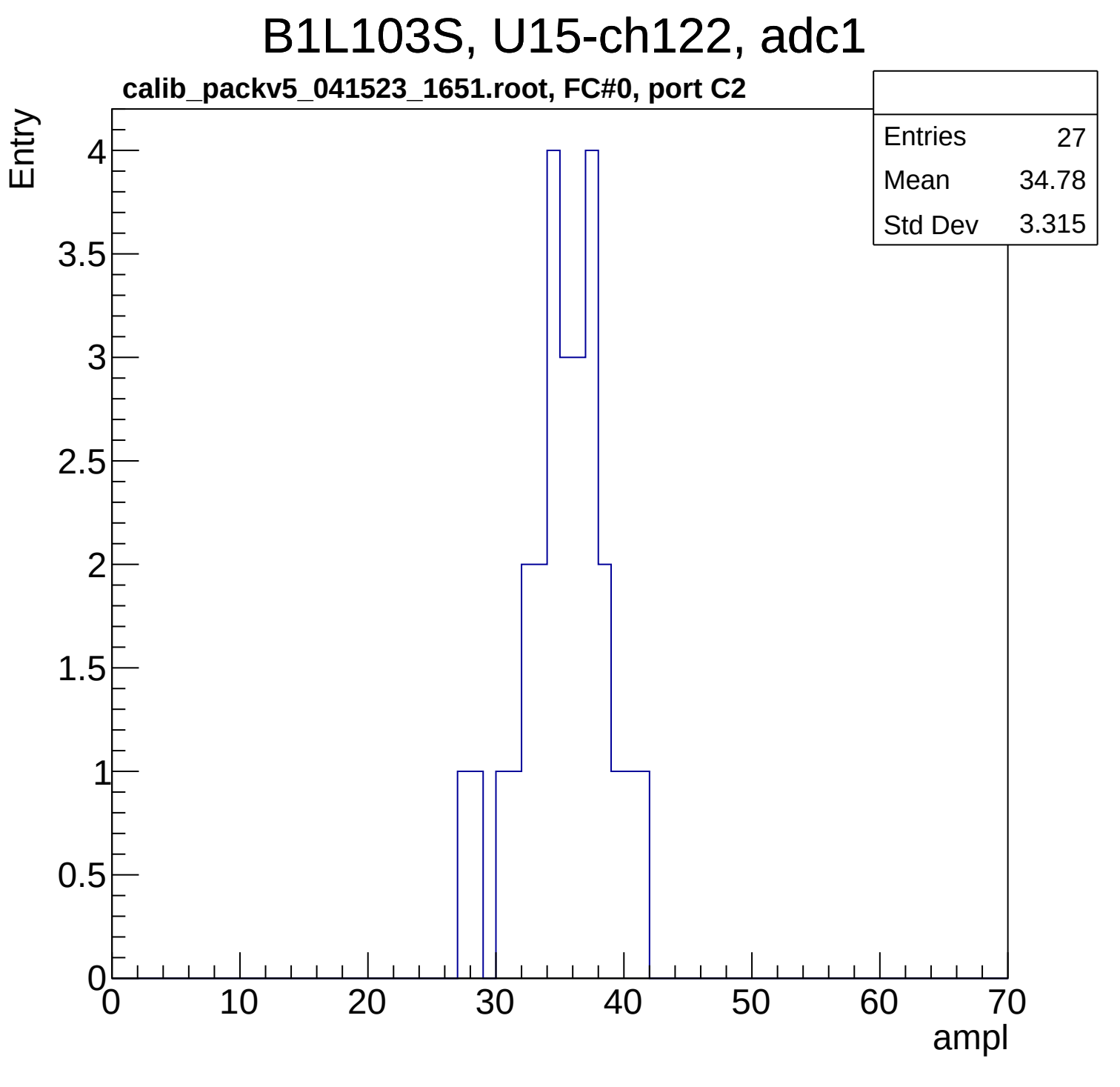
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L103S, U15-ch121, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 7.625
Std Dev 20.17
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U15-ch122, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 21.52
Std Dev 12.82
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch122, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 34.78
Std Dev 3.315
Entry
ampl
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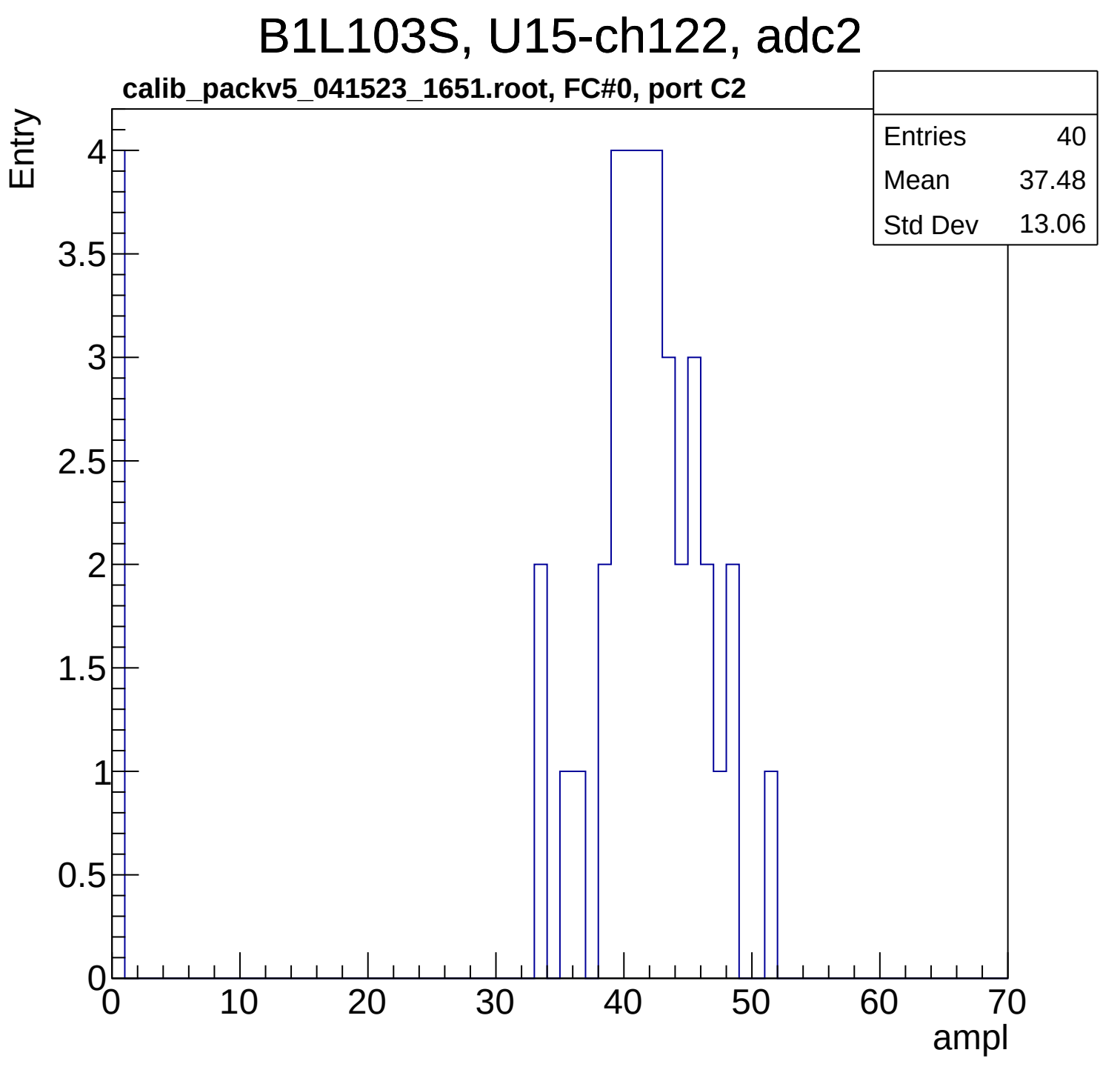
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch122, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 37.48
Std Dev 13.06
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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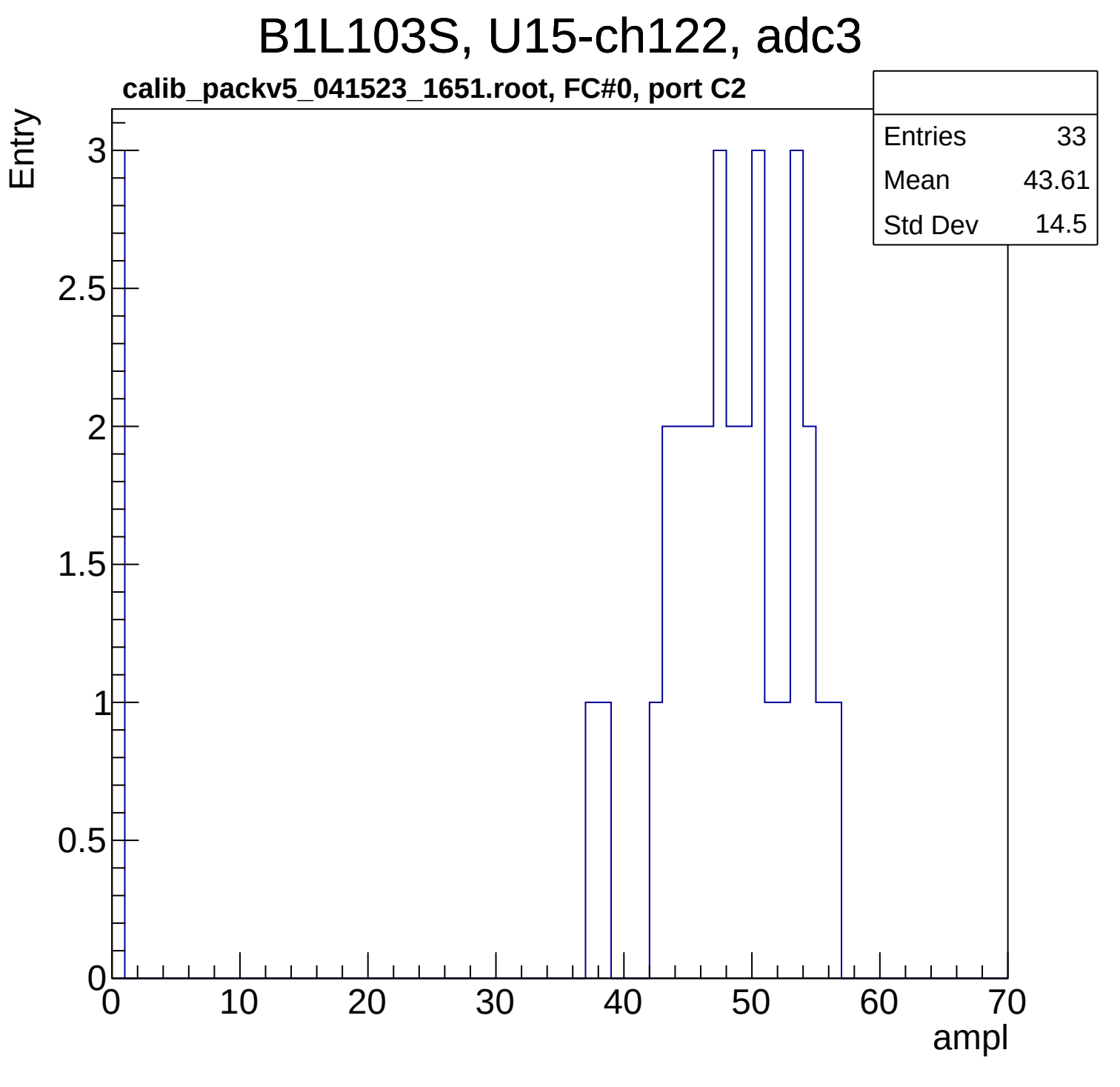
B1L103S, U15-ch122, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 43.61
Std Dev 14.5
Entry
ampl
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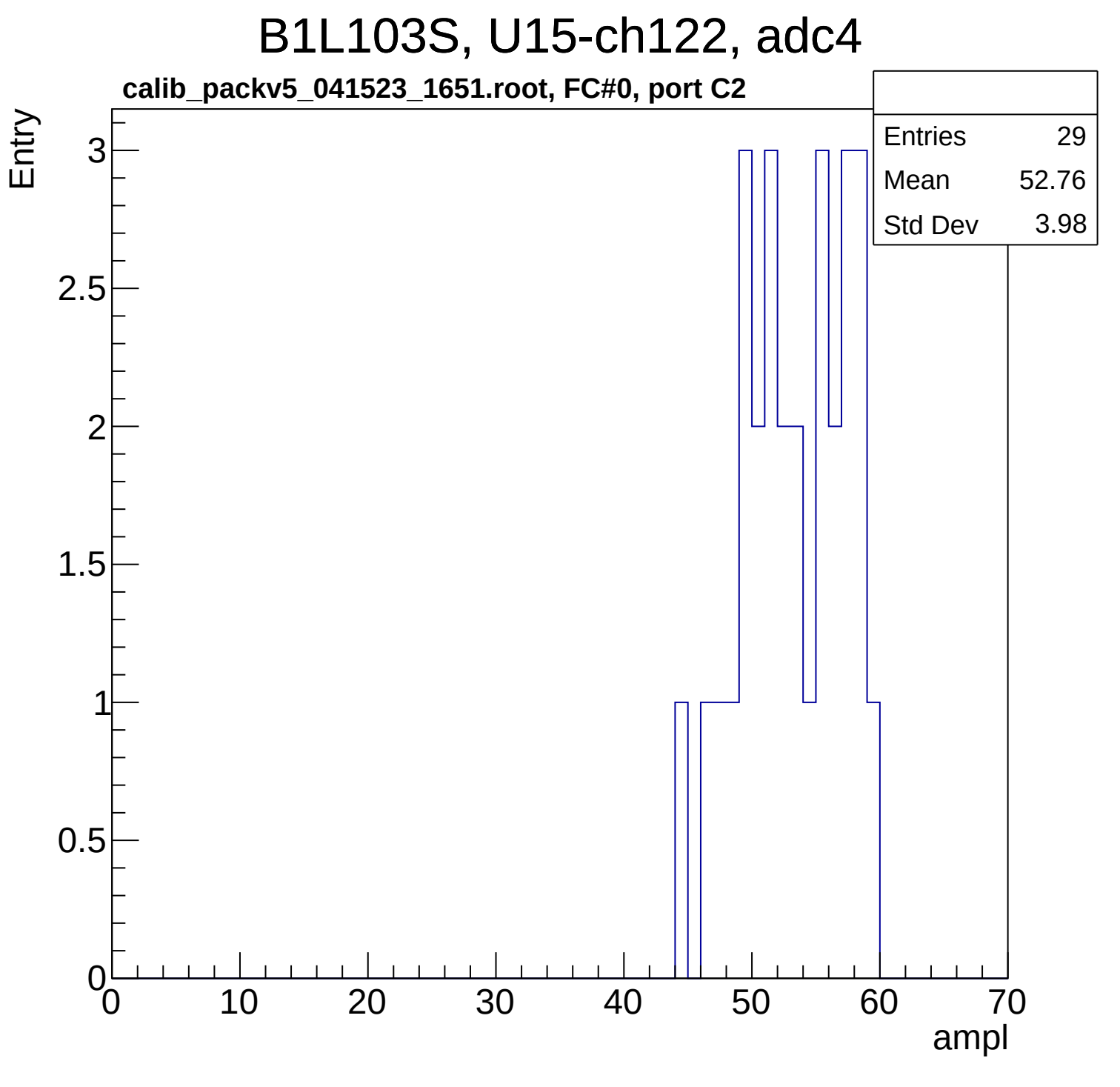
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch122, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 52.76
Std Dev 3.98
Entry
ampl
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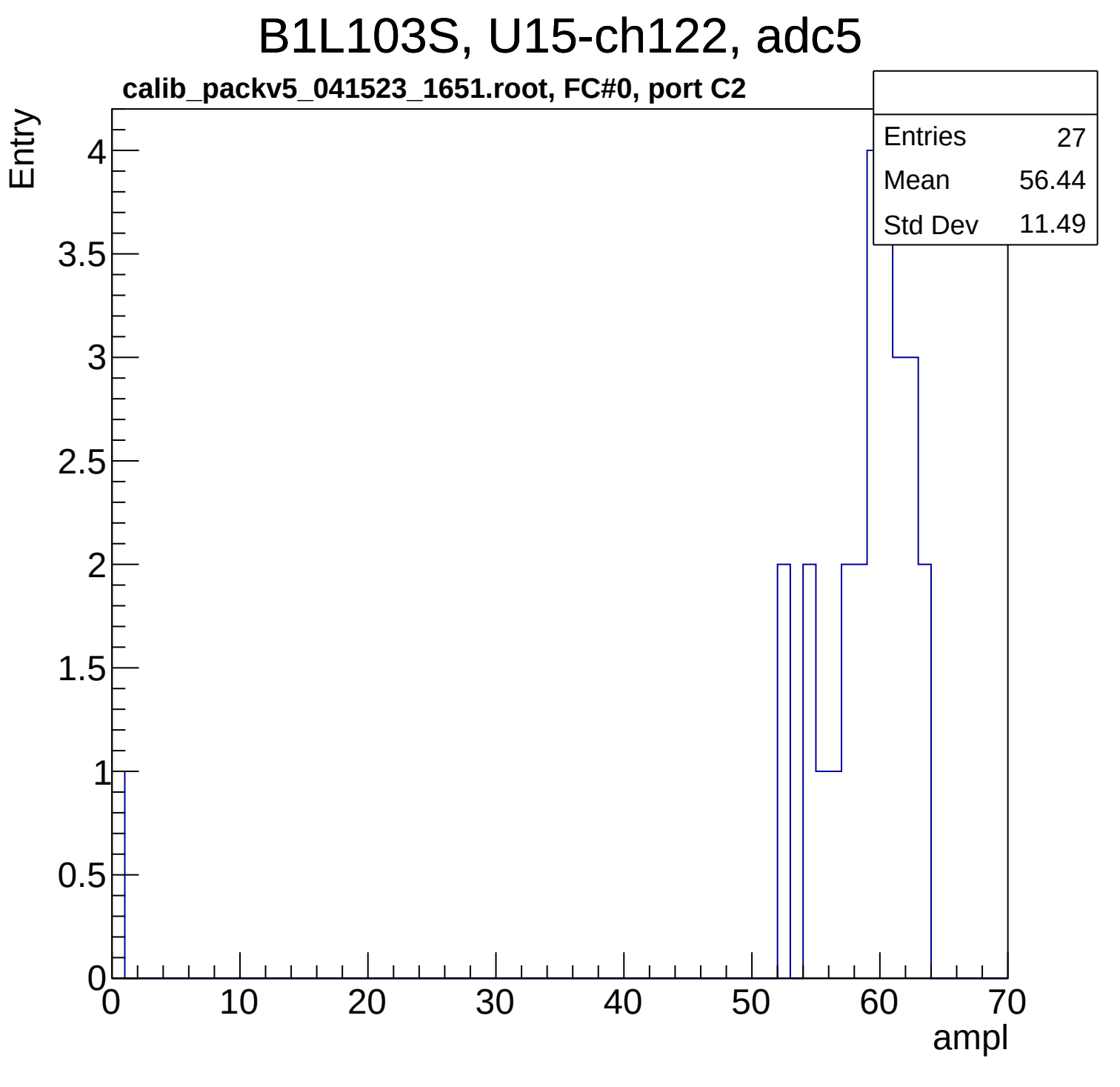
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch122, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 56.44
Std Dev 11.49
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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20
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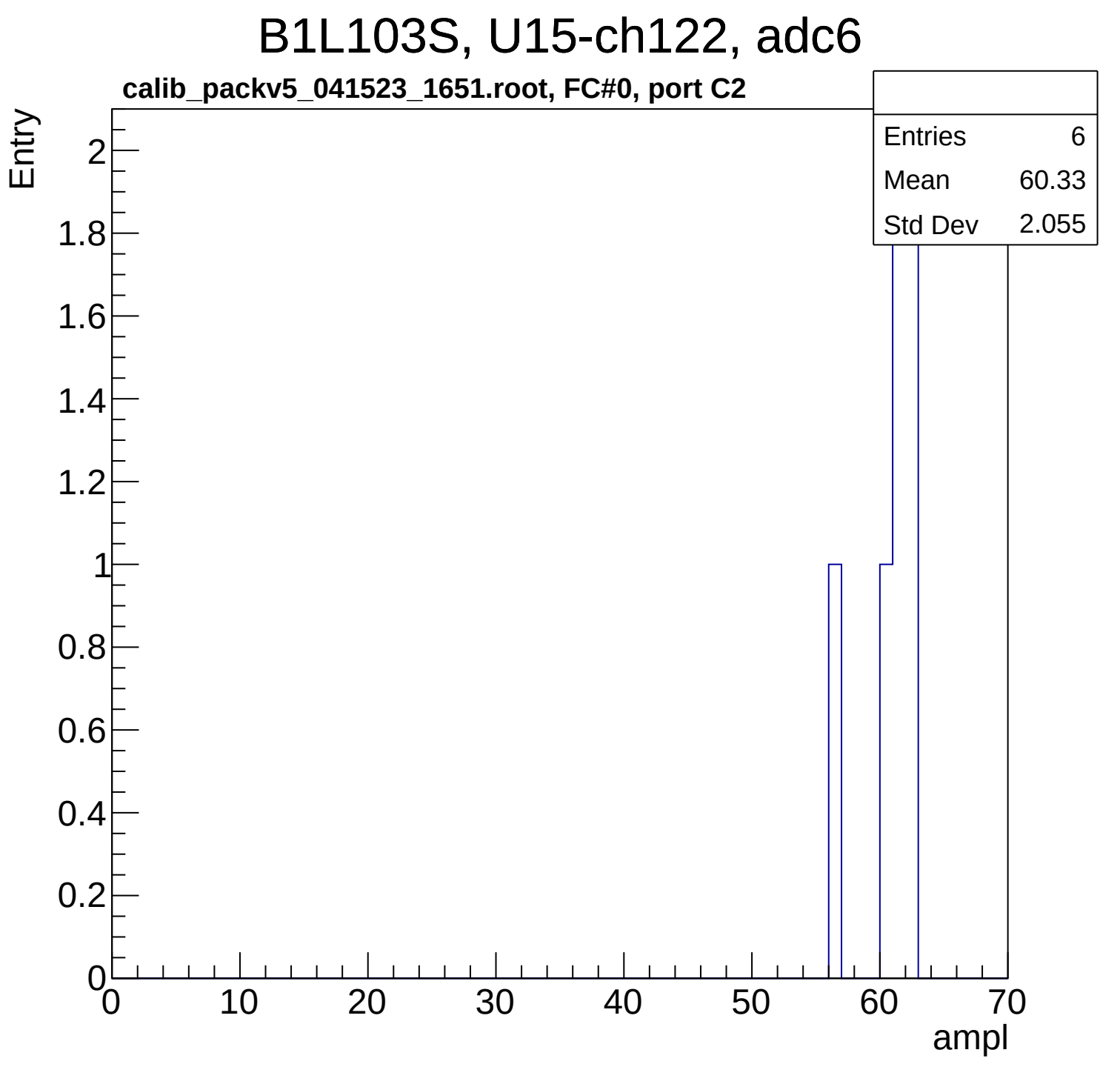
40
50
60
70


B1L103S, U15-ch122, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 60.33
Std Dev 2.055
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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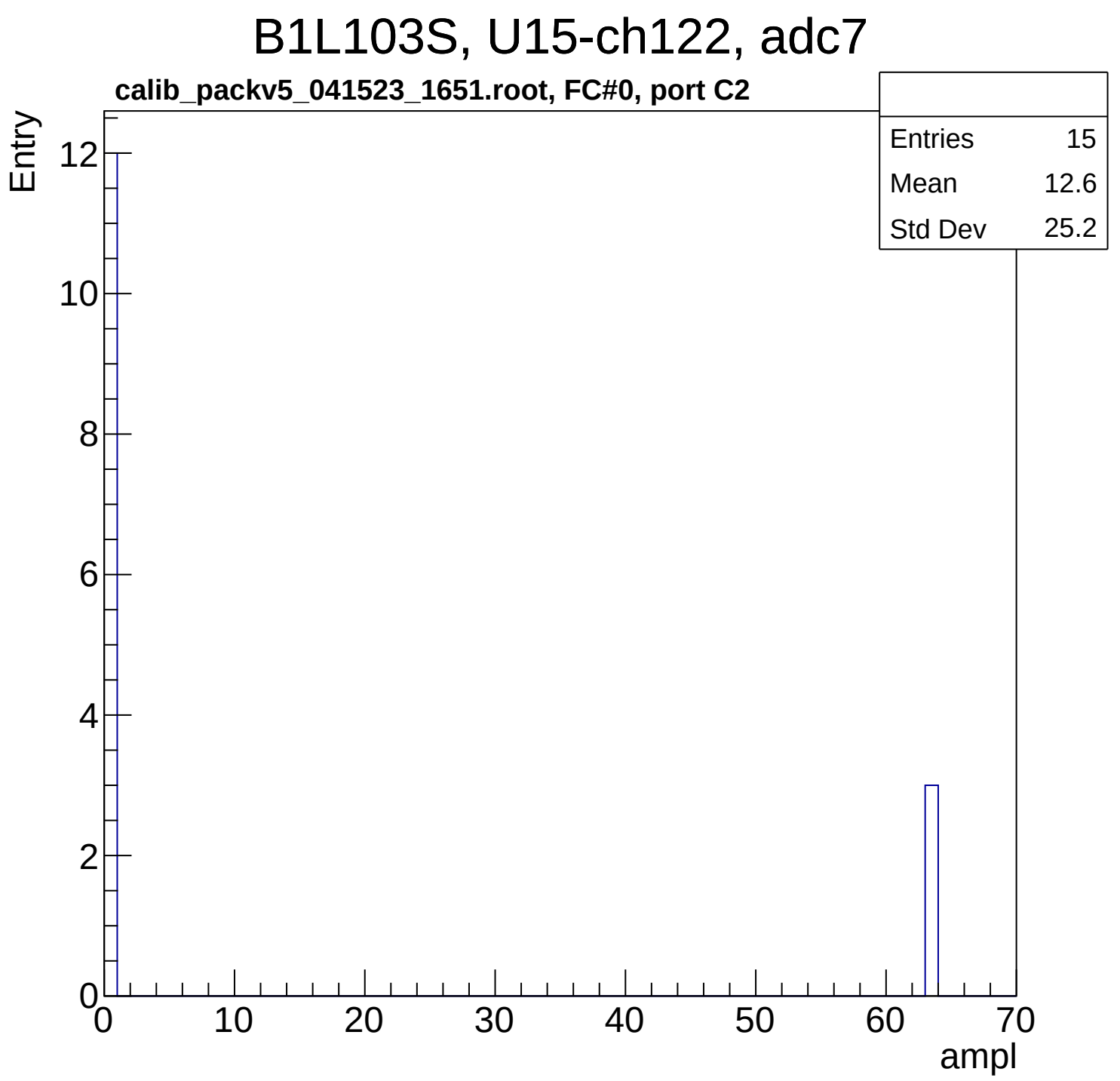
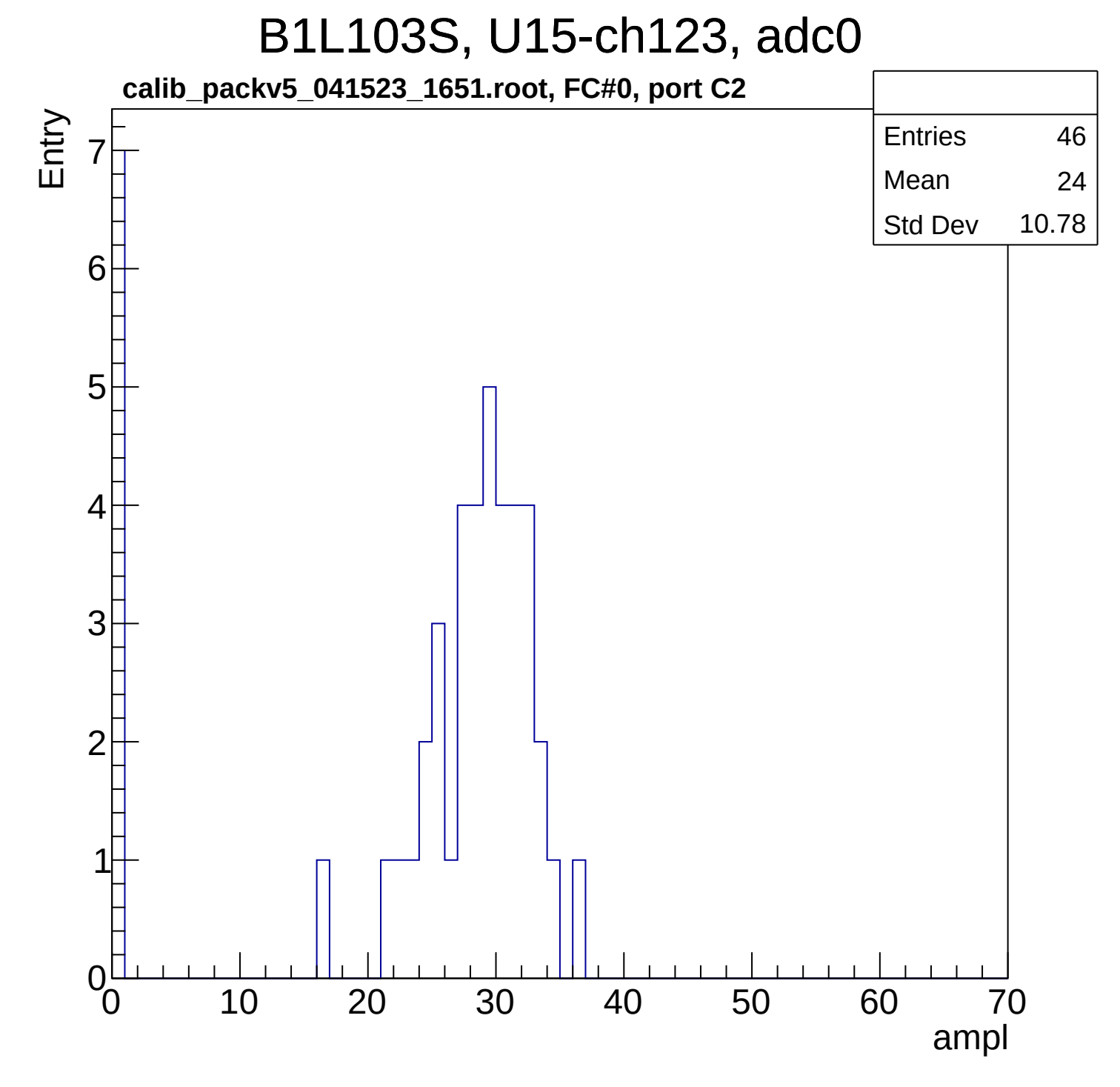
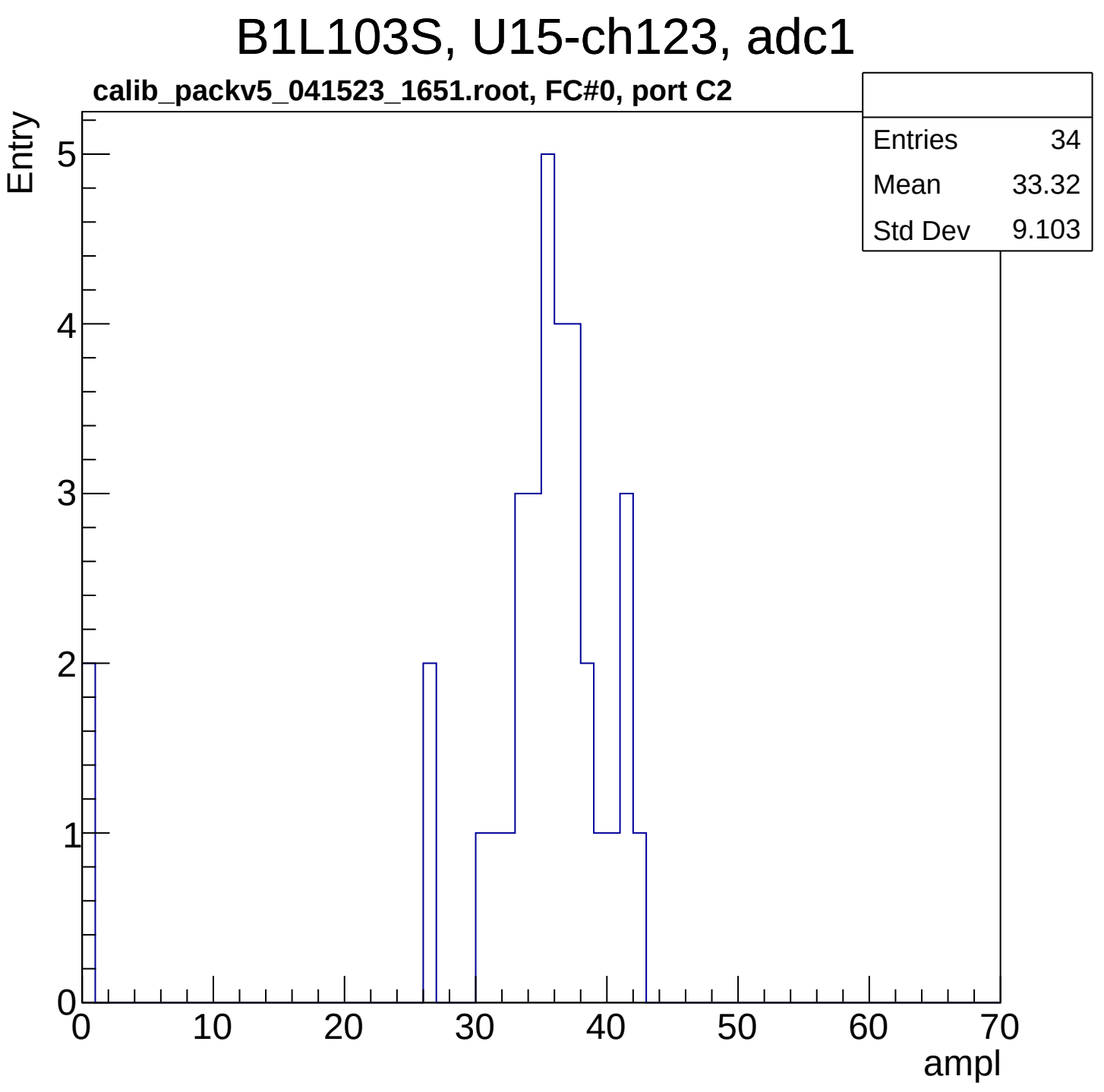
40
50
60
70


B1L103S, U15-ch122, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 12.6
Std Dev 25.2
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch123, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 24
Std Dev 10.78
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U15-ch123, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 33.32
Std Dev 9.103
Entry
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3
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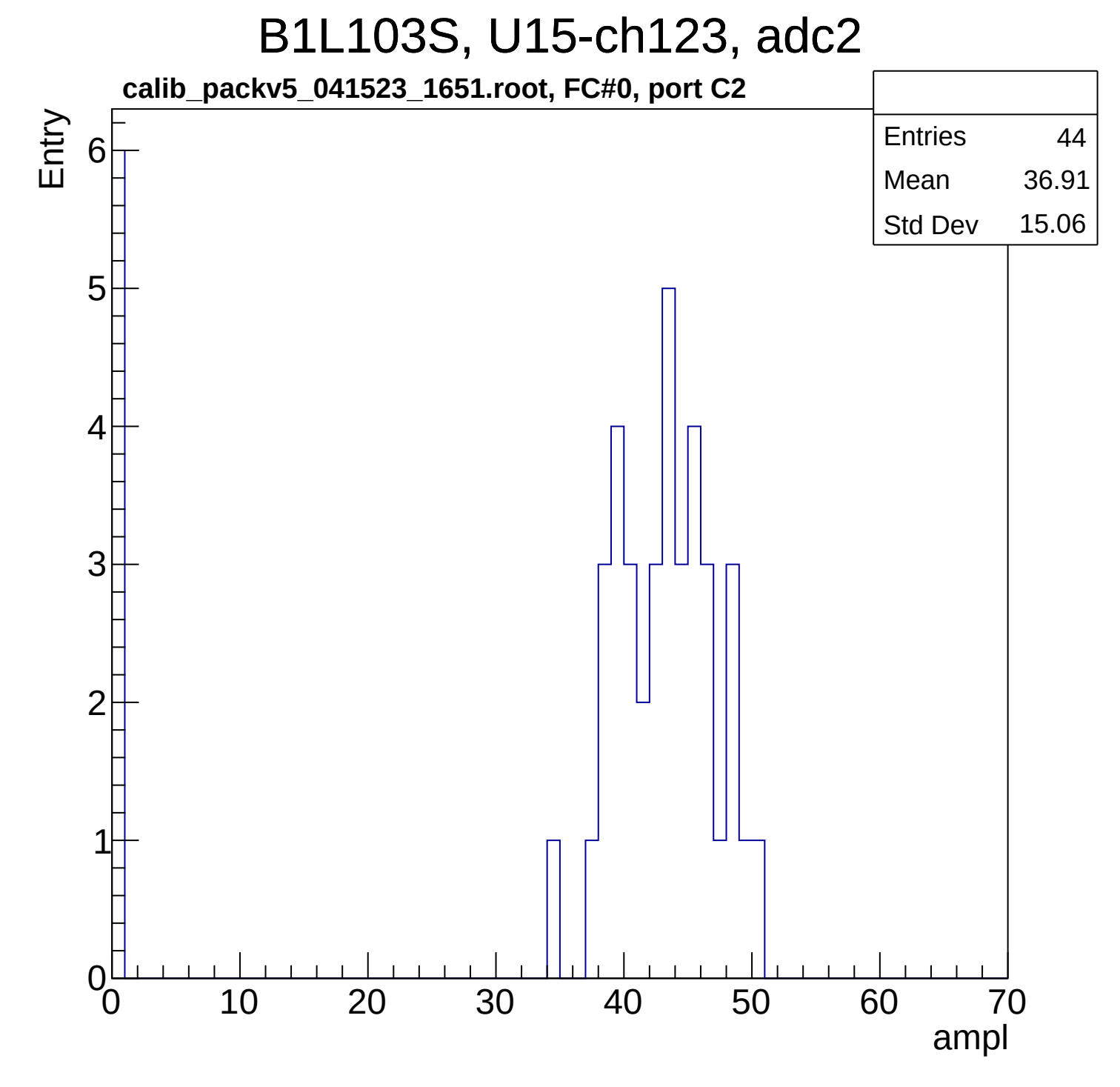
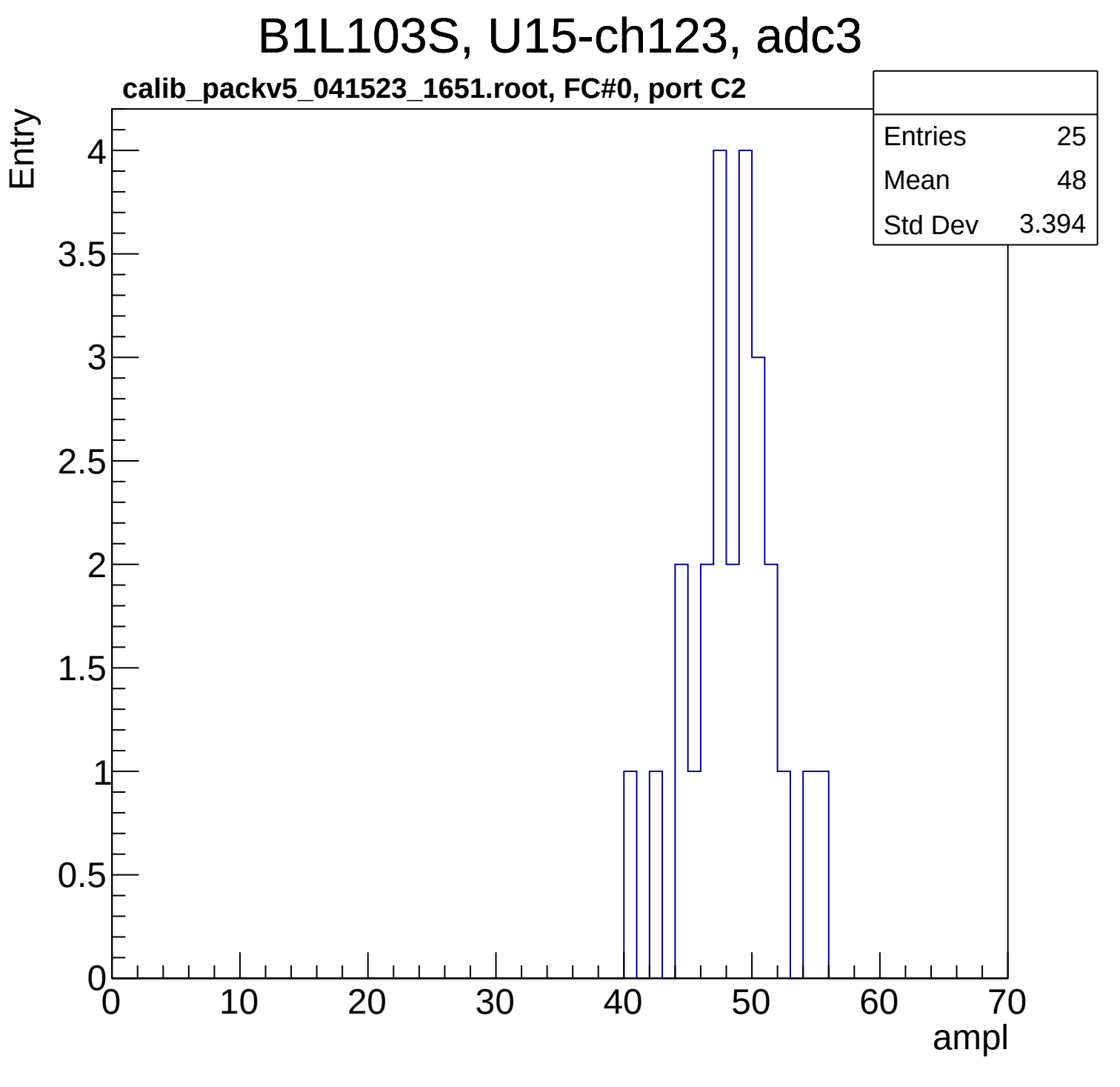
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch123, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 36.91
Std Dev 15.06
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch123, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 48
Std Dev 3.394
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
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40
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60
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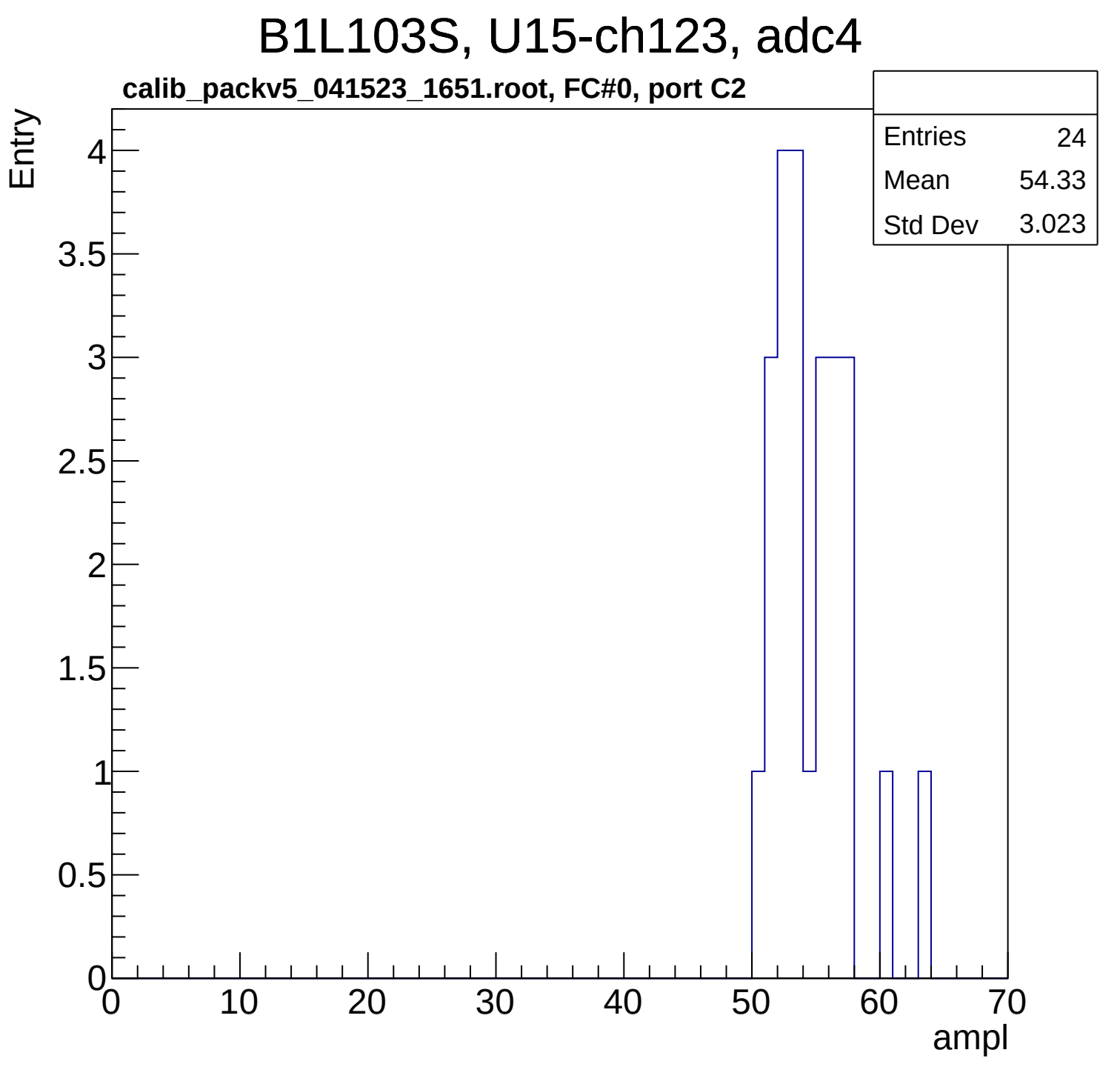
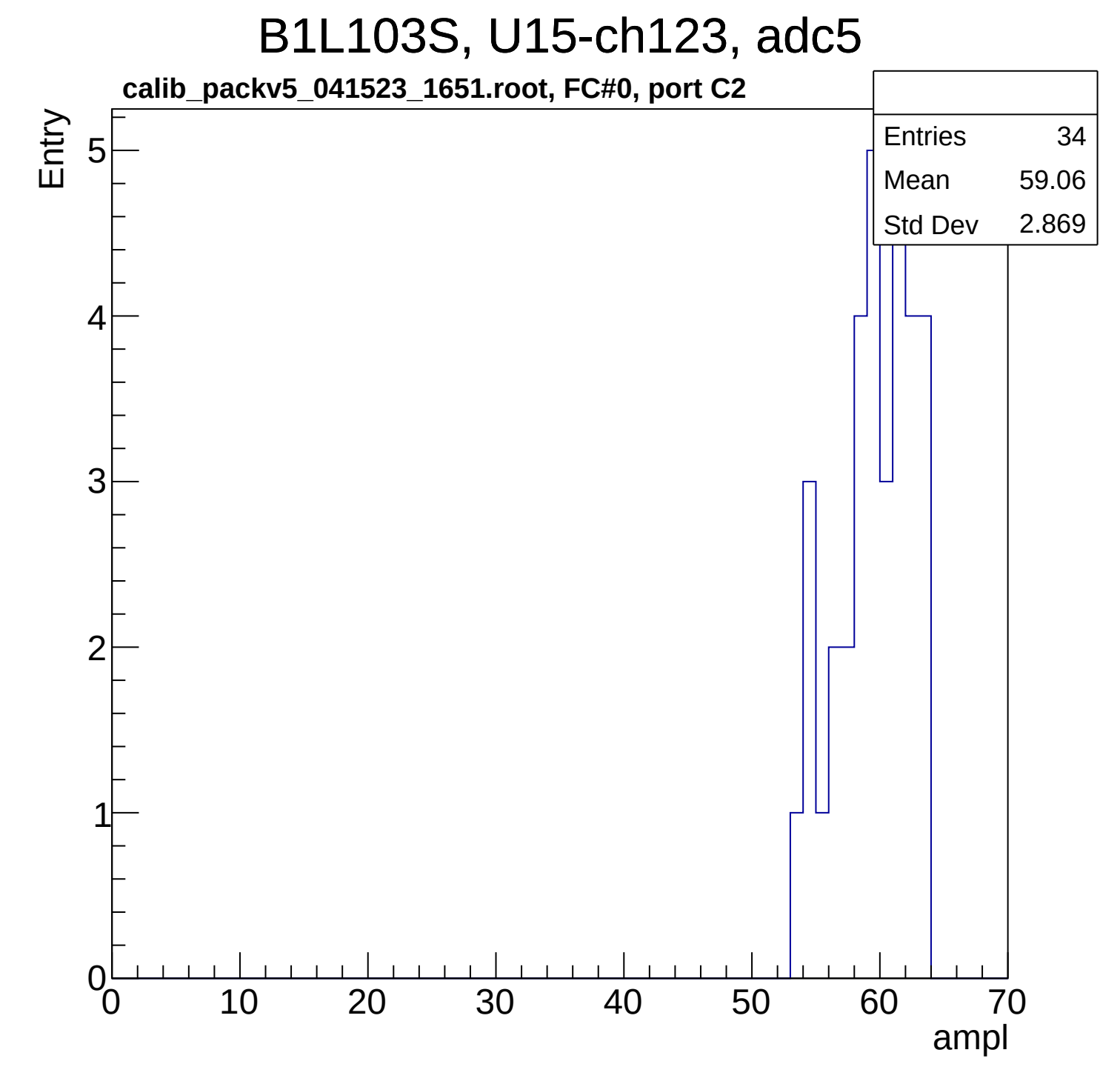
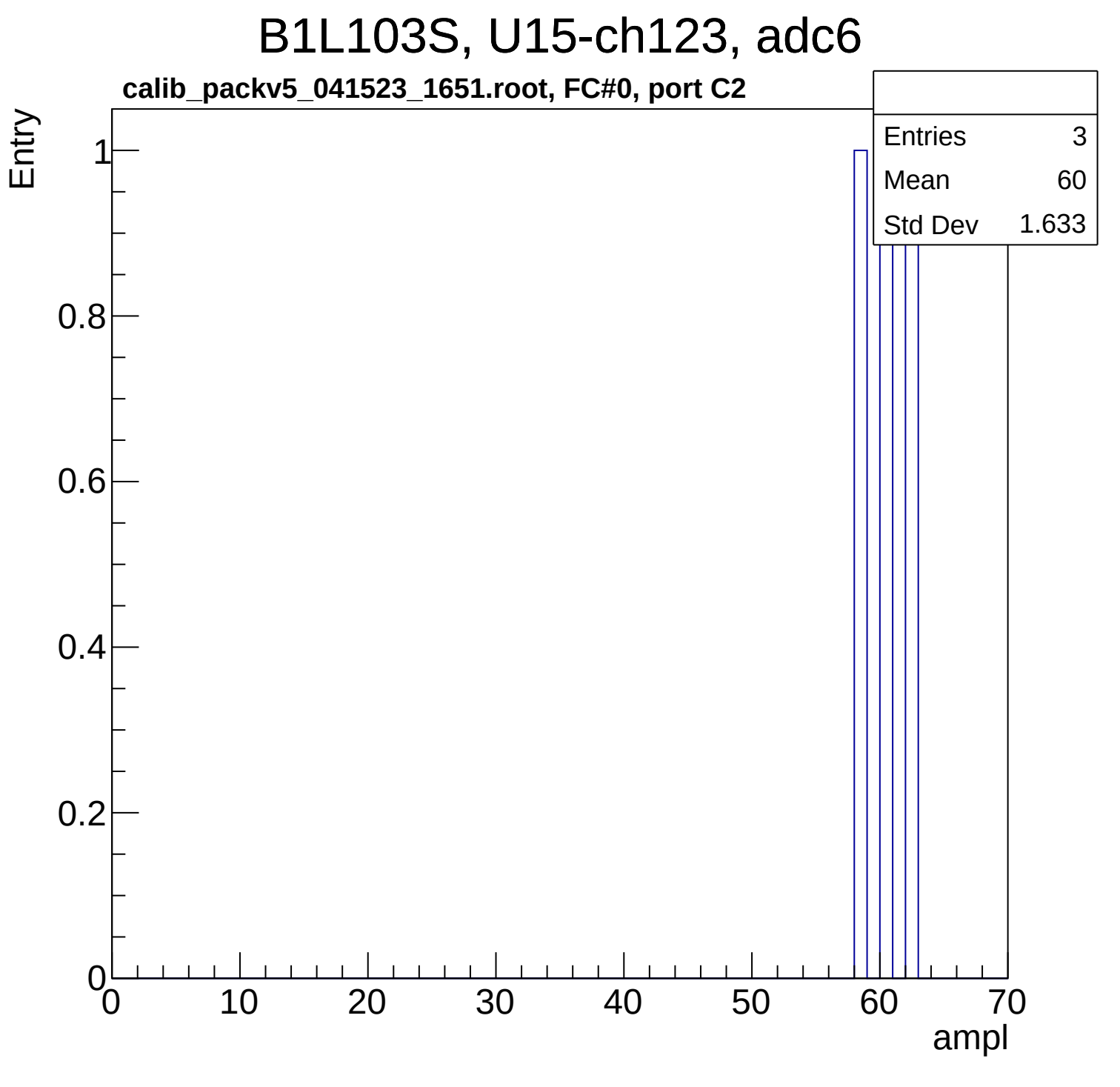
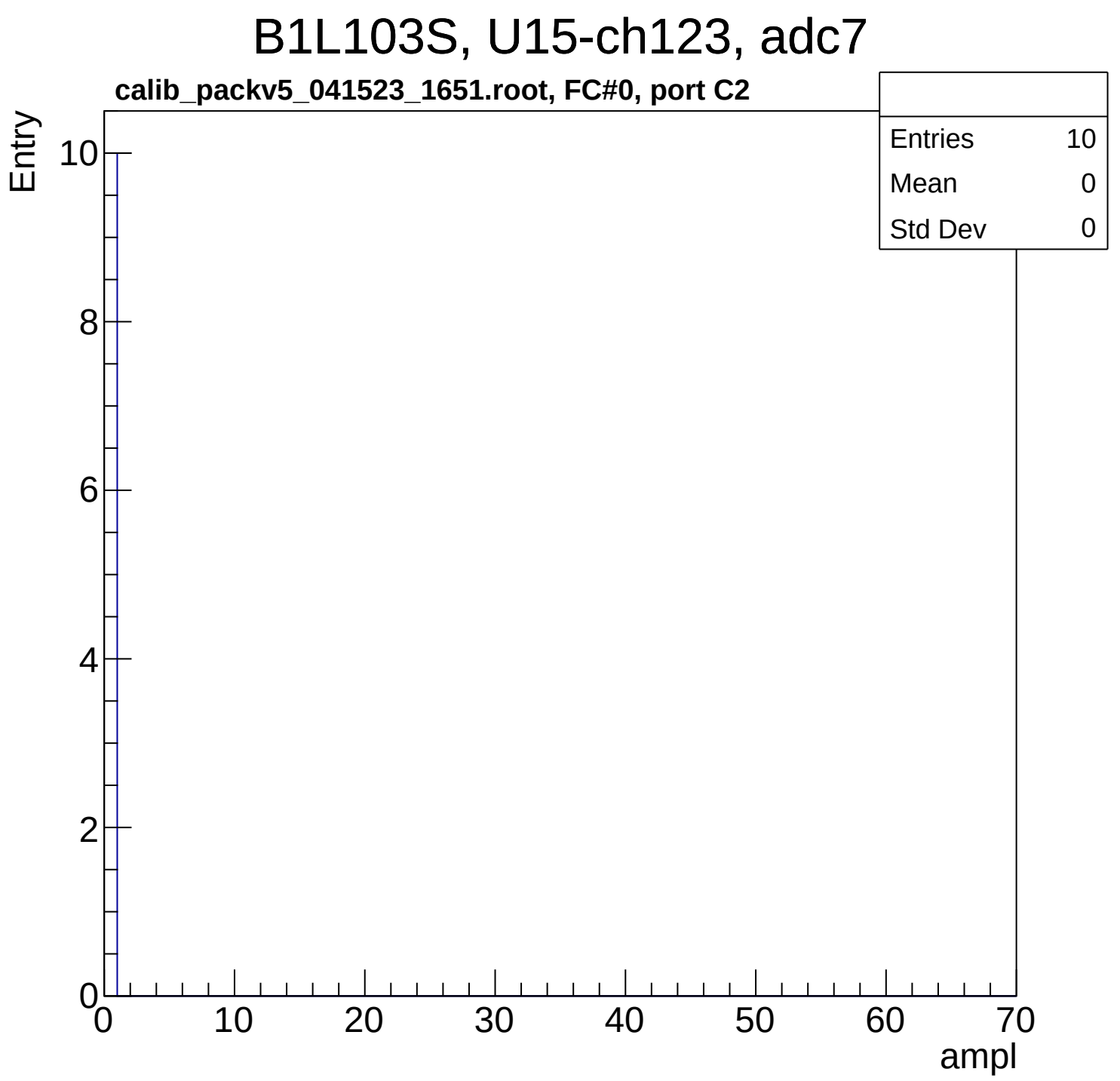
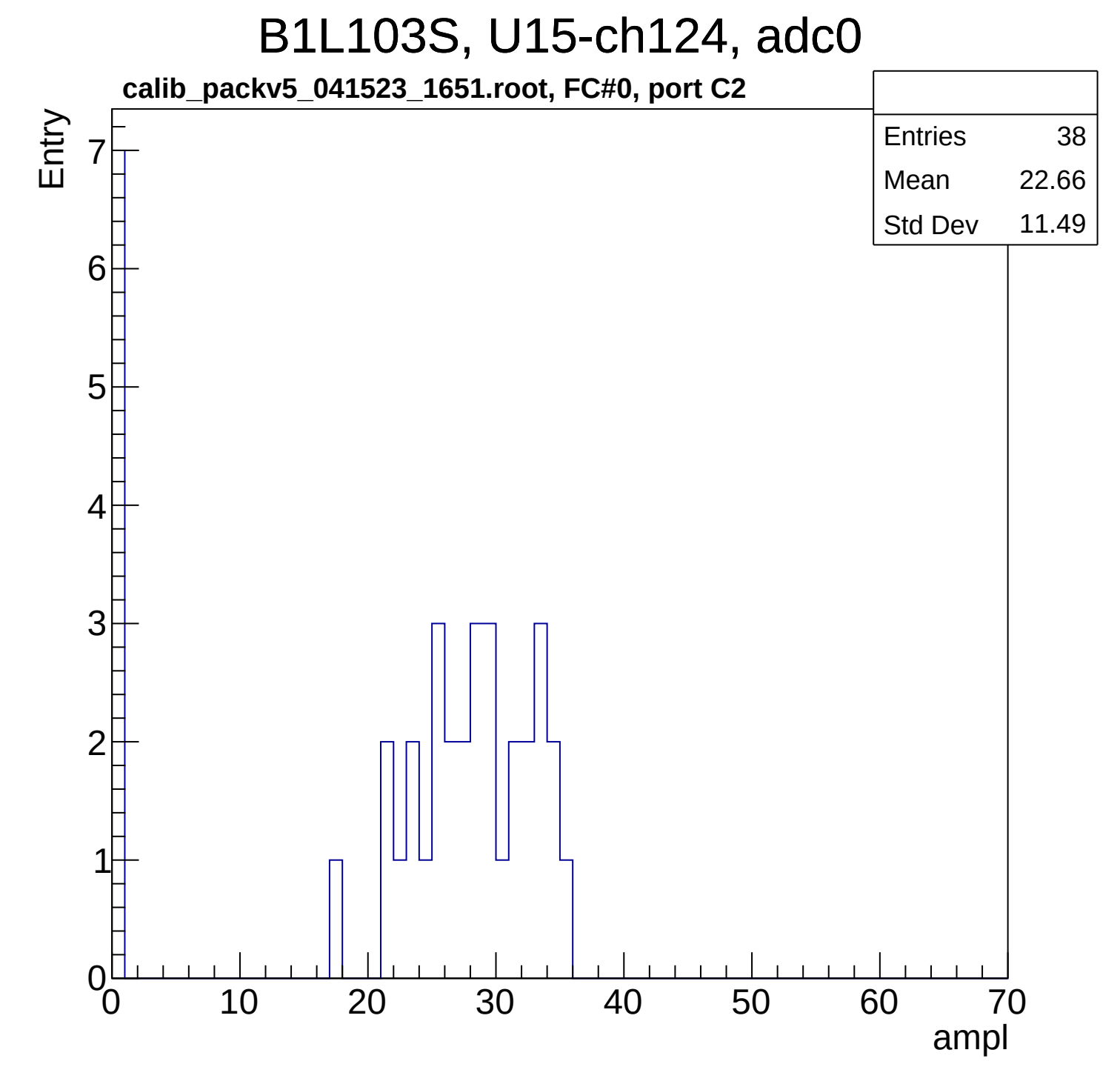
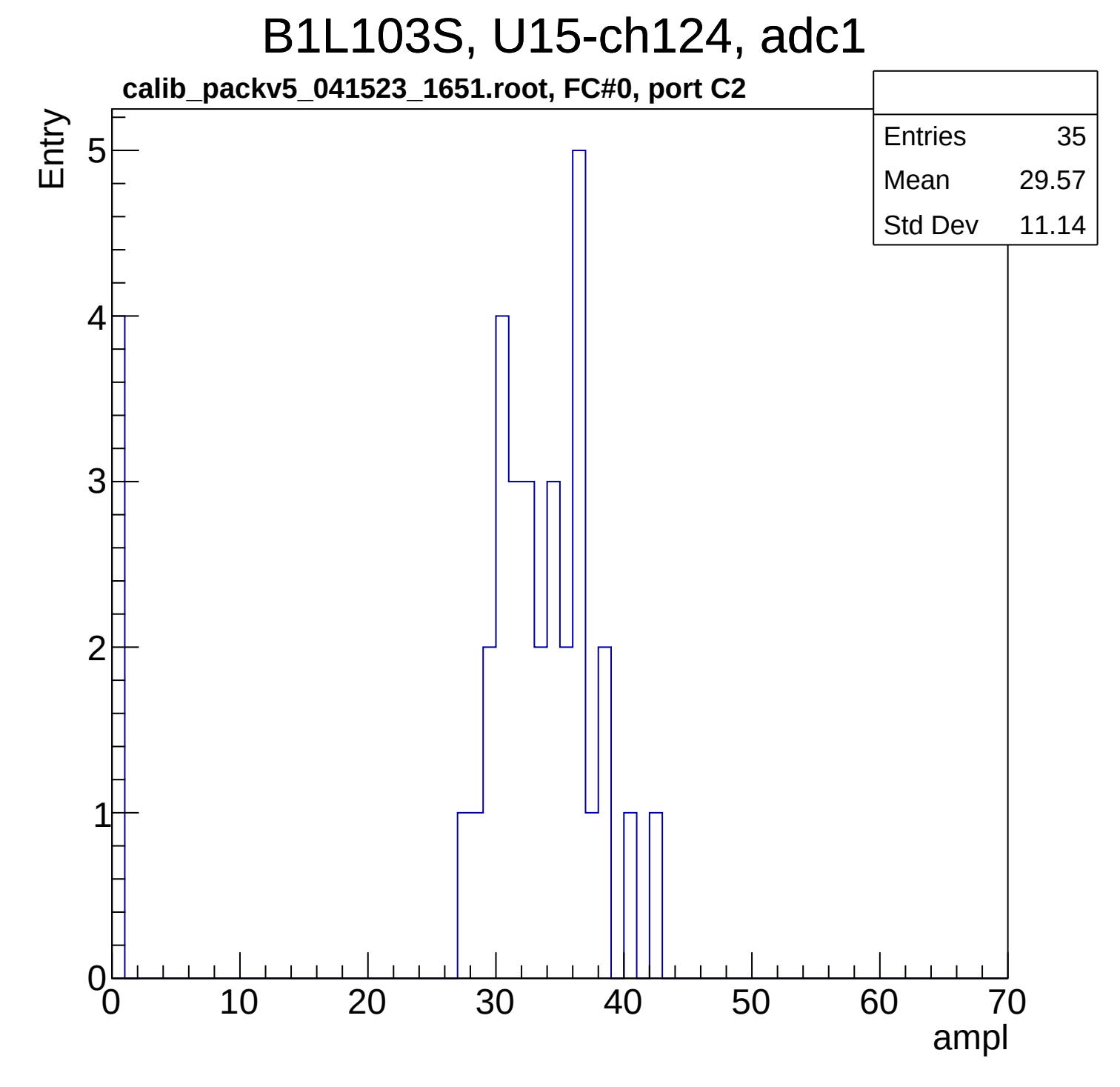

B1L103S, U15-ch123, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 54.33
Std Dev 3.023
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

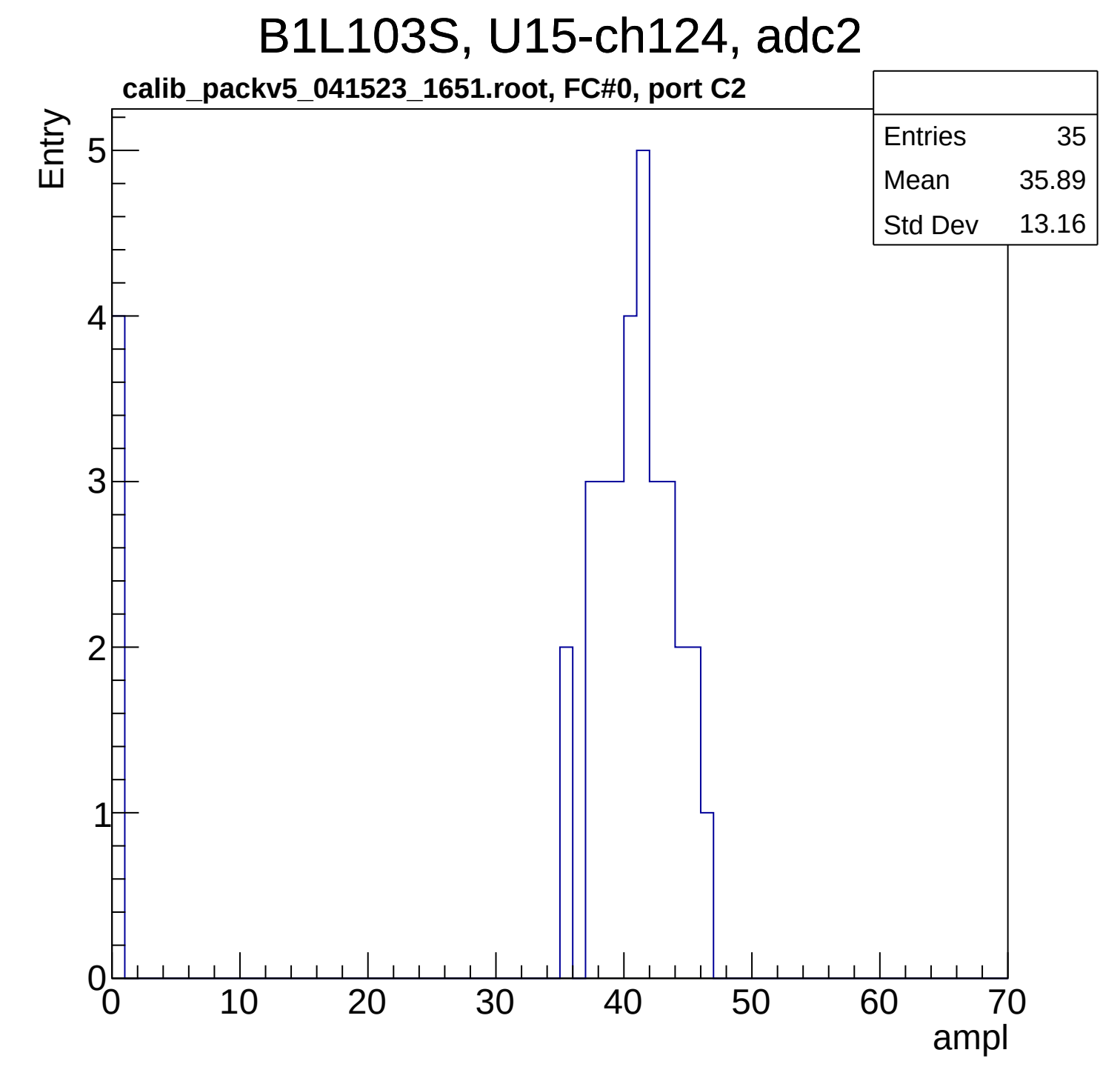

B1L103S, U15-ch123, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 59.06
Std Dev 2.869
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

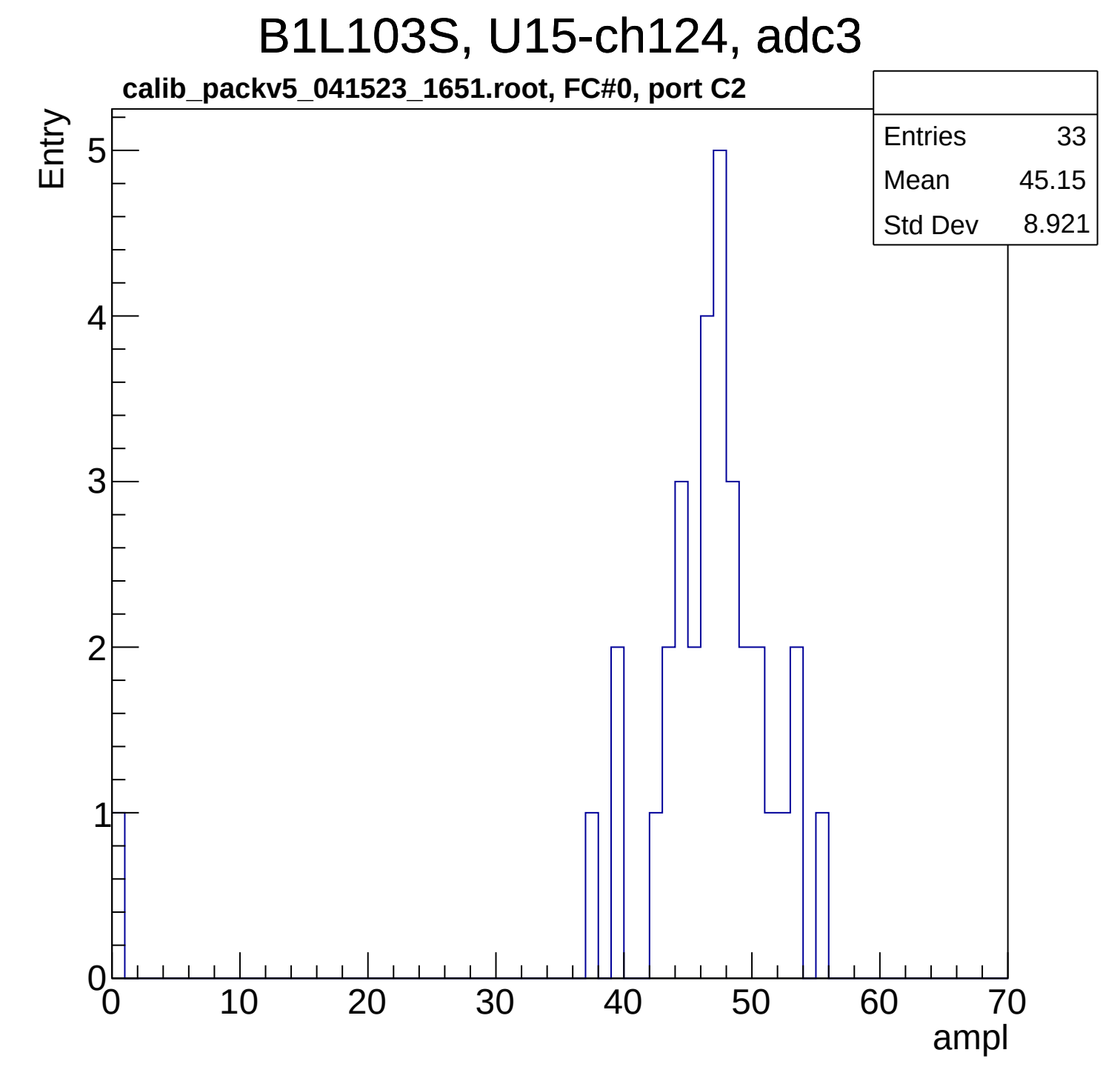

B1L103S, U15-ch123, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 60
Std Dev 1.633
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

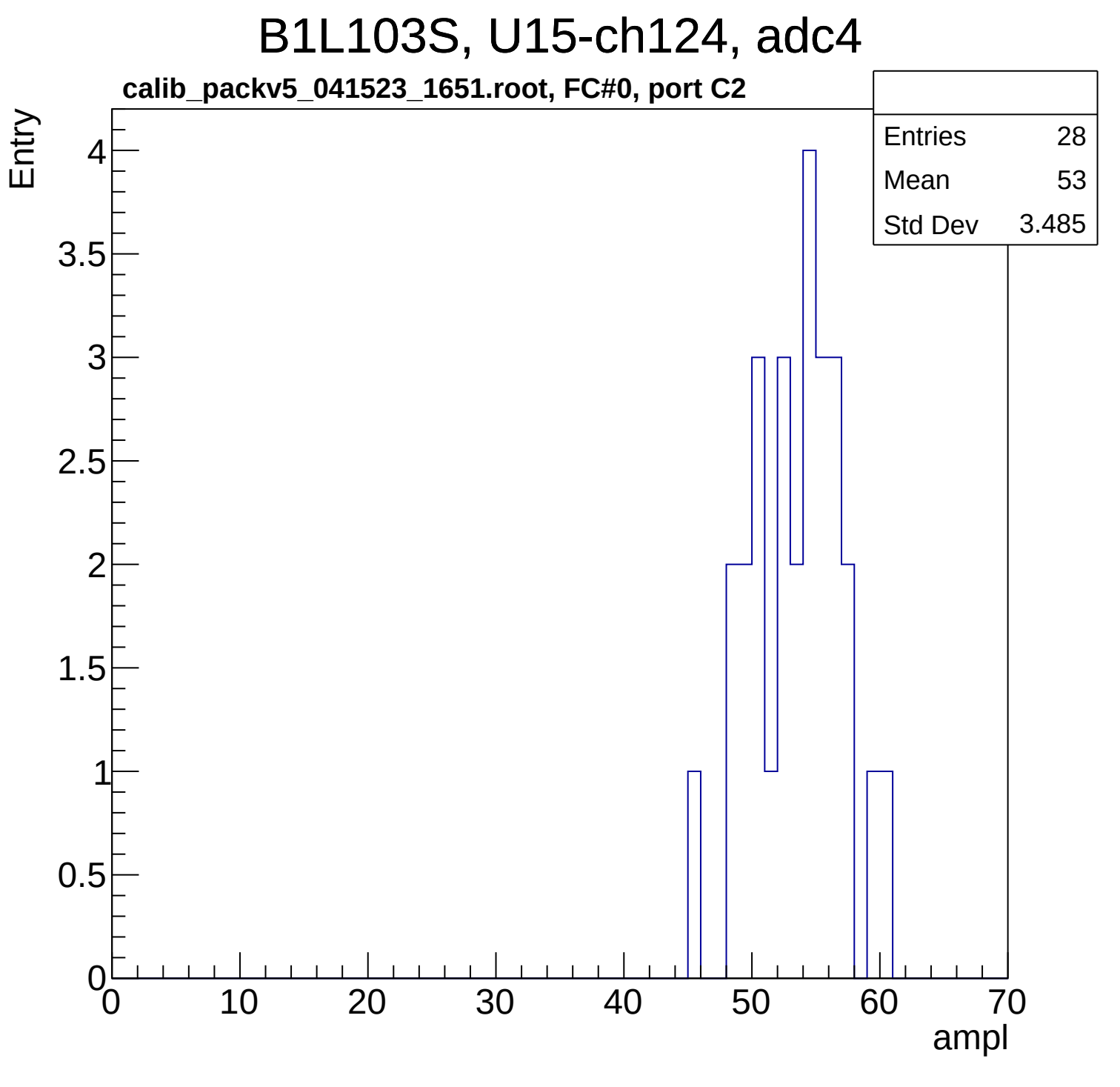

B1L103S, U15-ch123, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

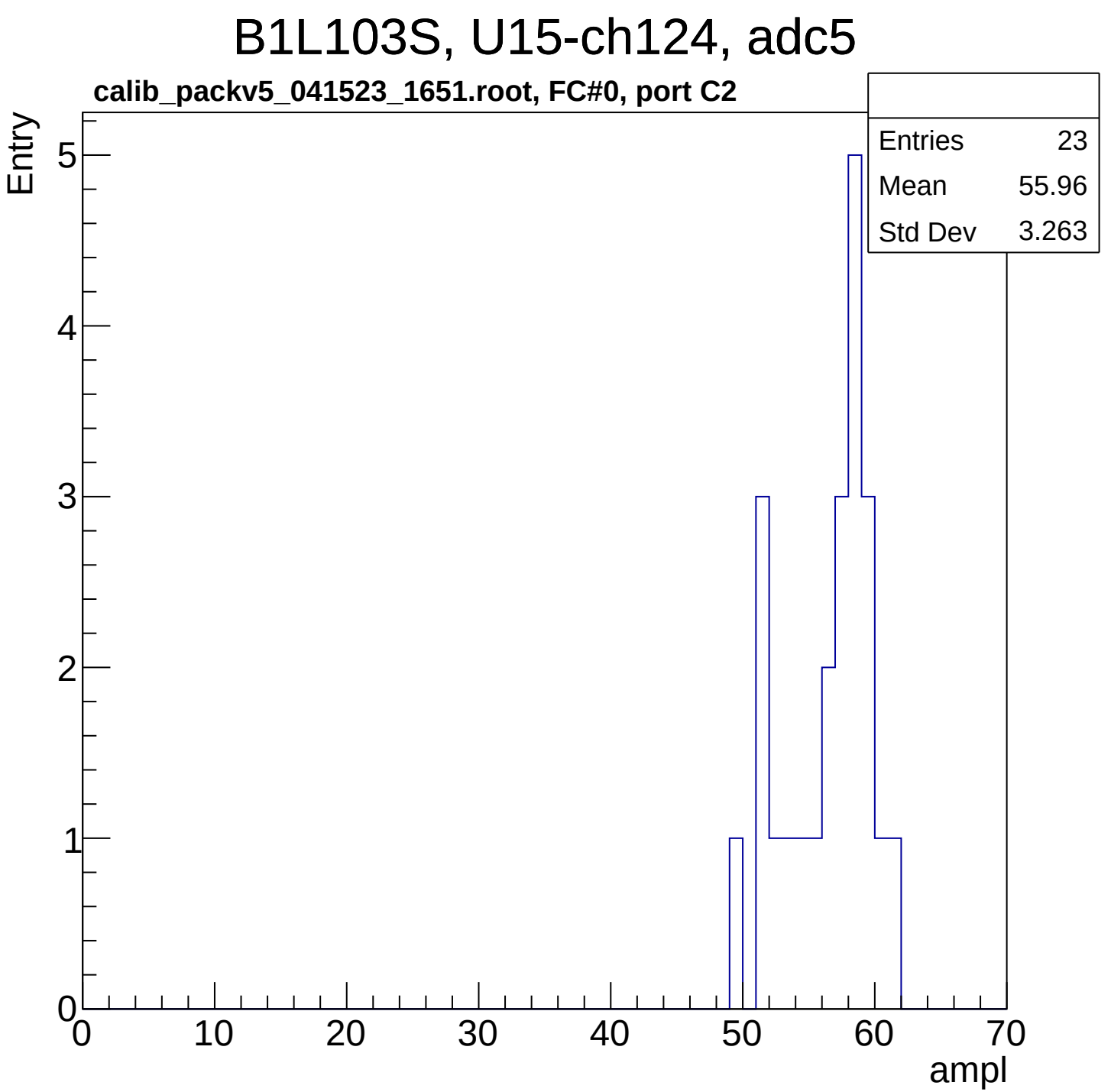

B1L103S, U15-ch124, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 22.66
Std Dev 11.49
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

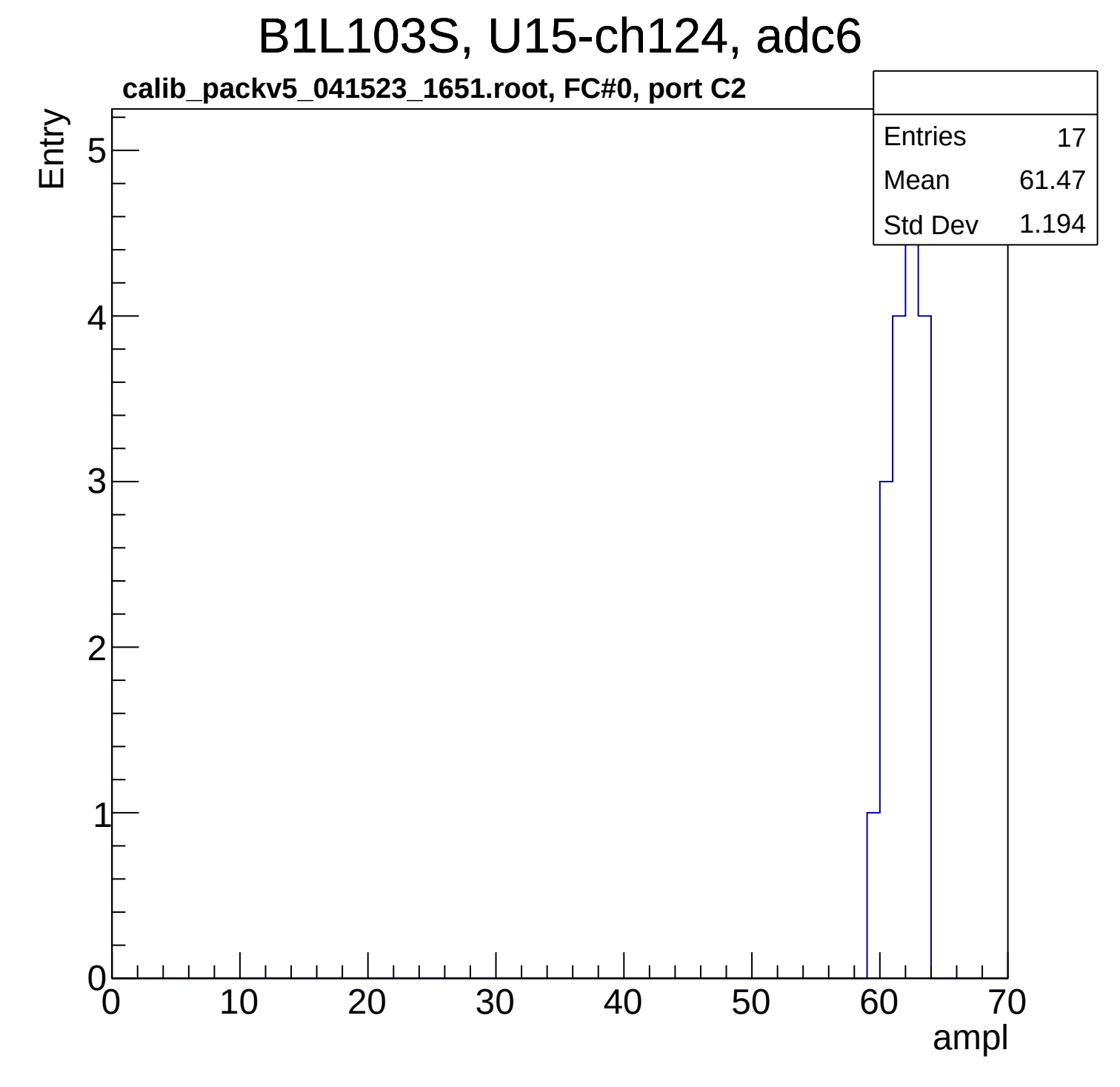

B1L103S, U15-ch124, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 29.57
Std Dev 11.14
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

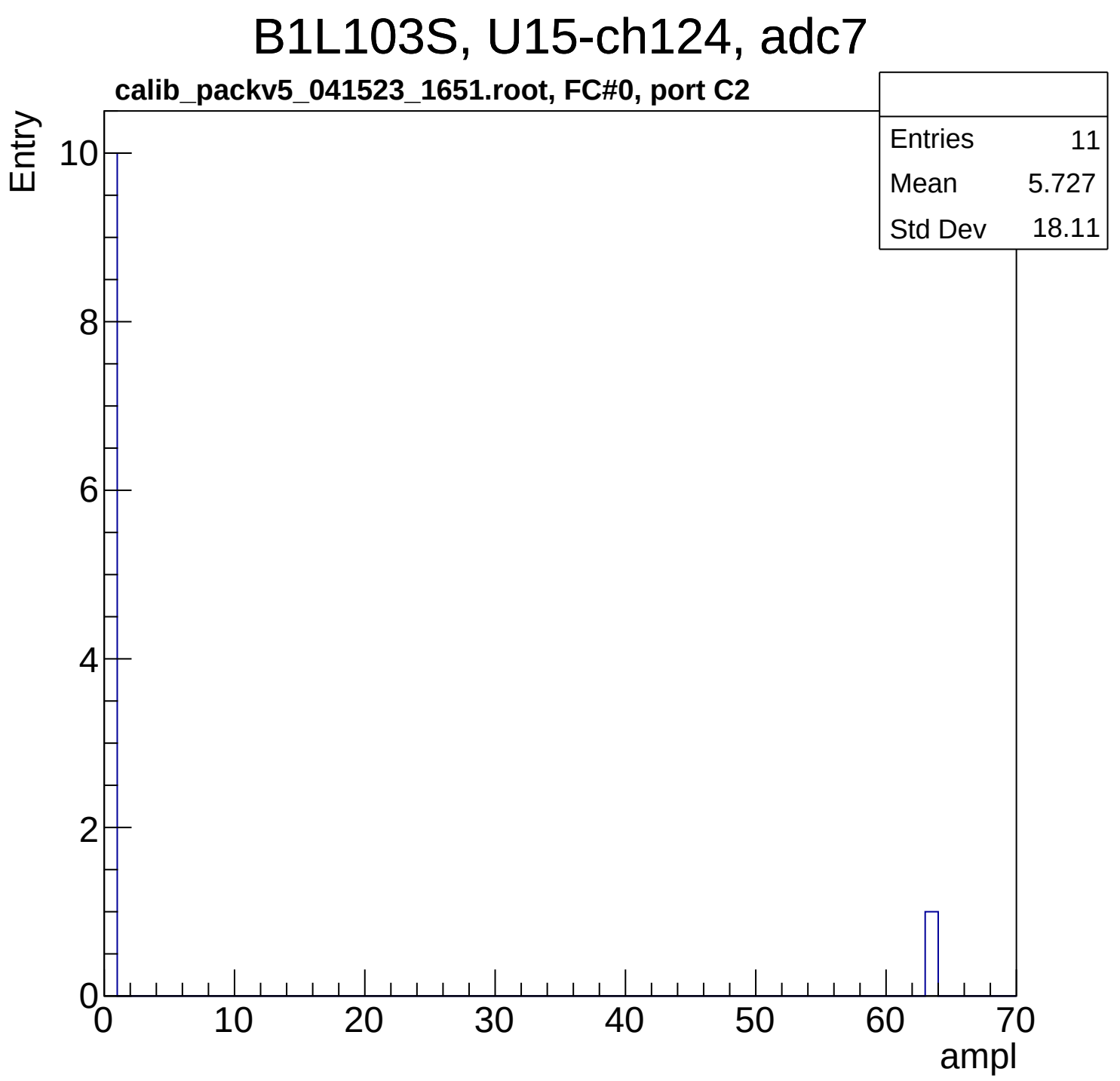

B1L103S, U15-ch124, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 35.89
Std Dev 13.16
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

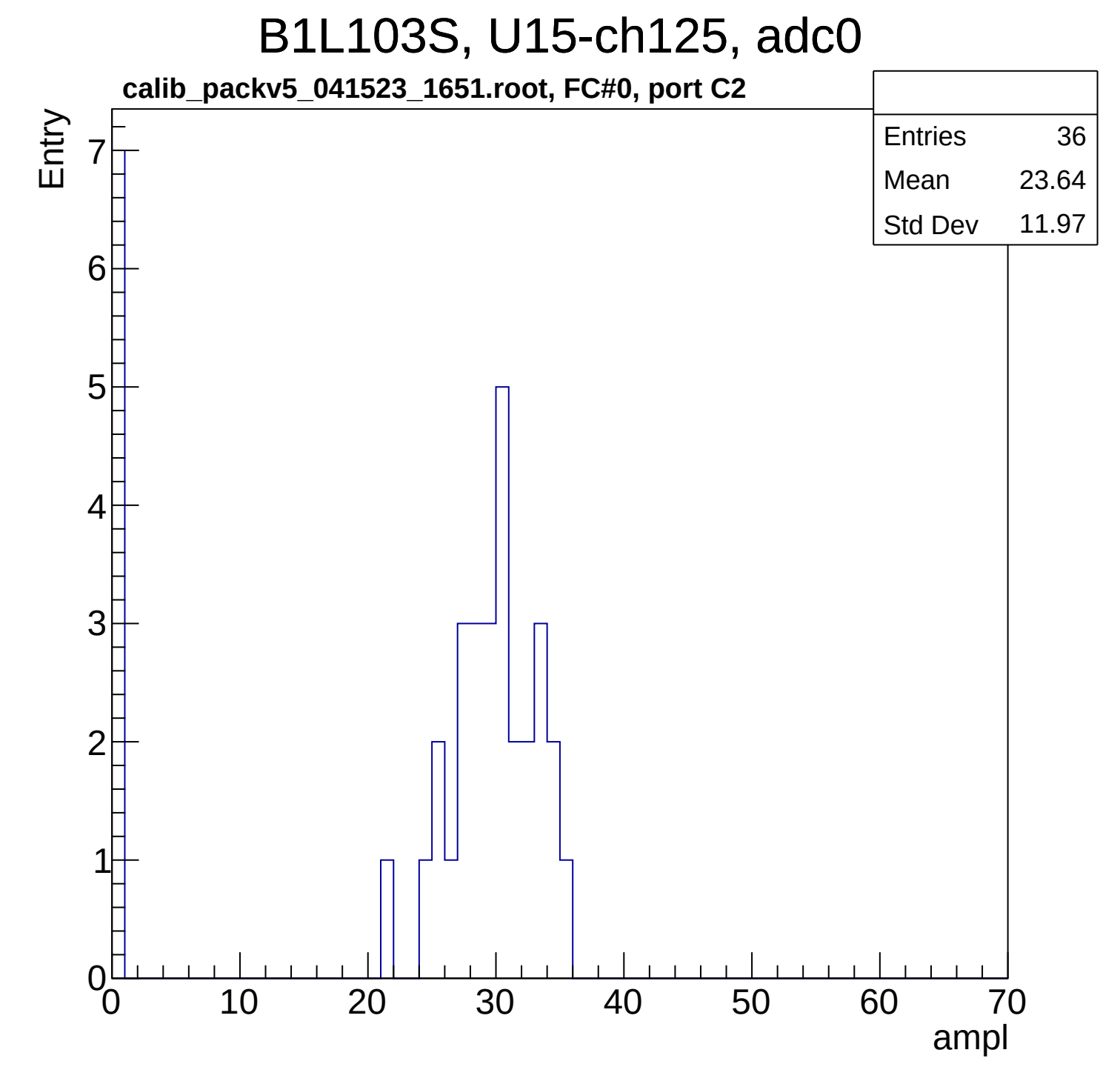

B1L103S, U15-ch124, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 45.15
Std Dev 8.921
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

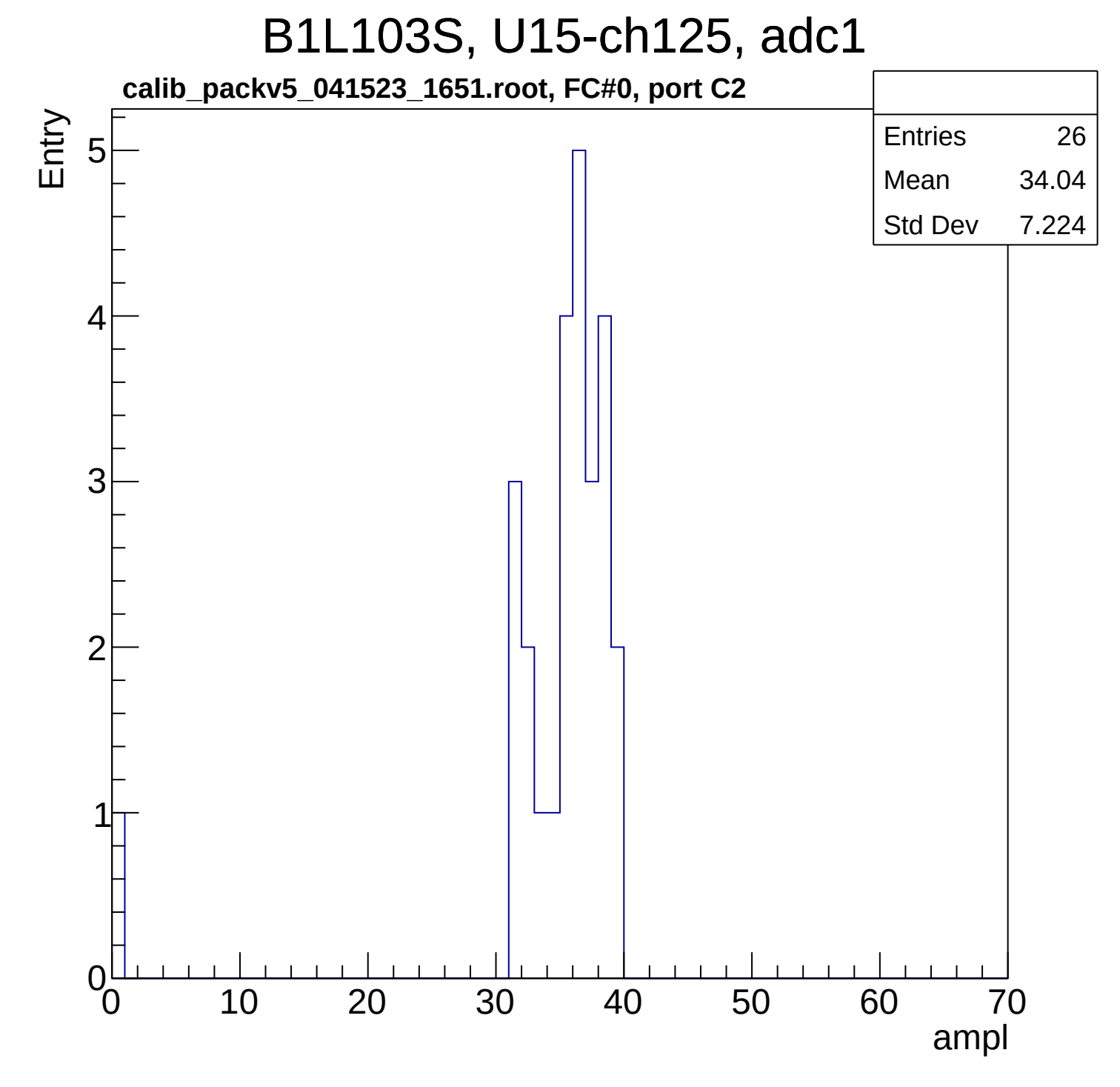

B1L103S, U15-ch124, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 53
Std Dev 3.485
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

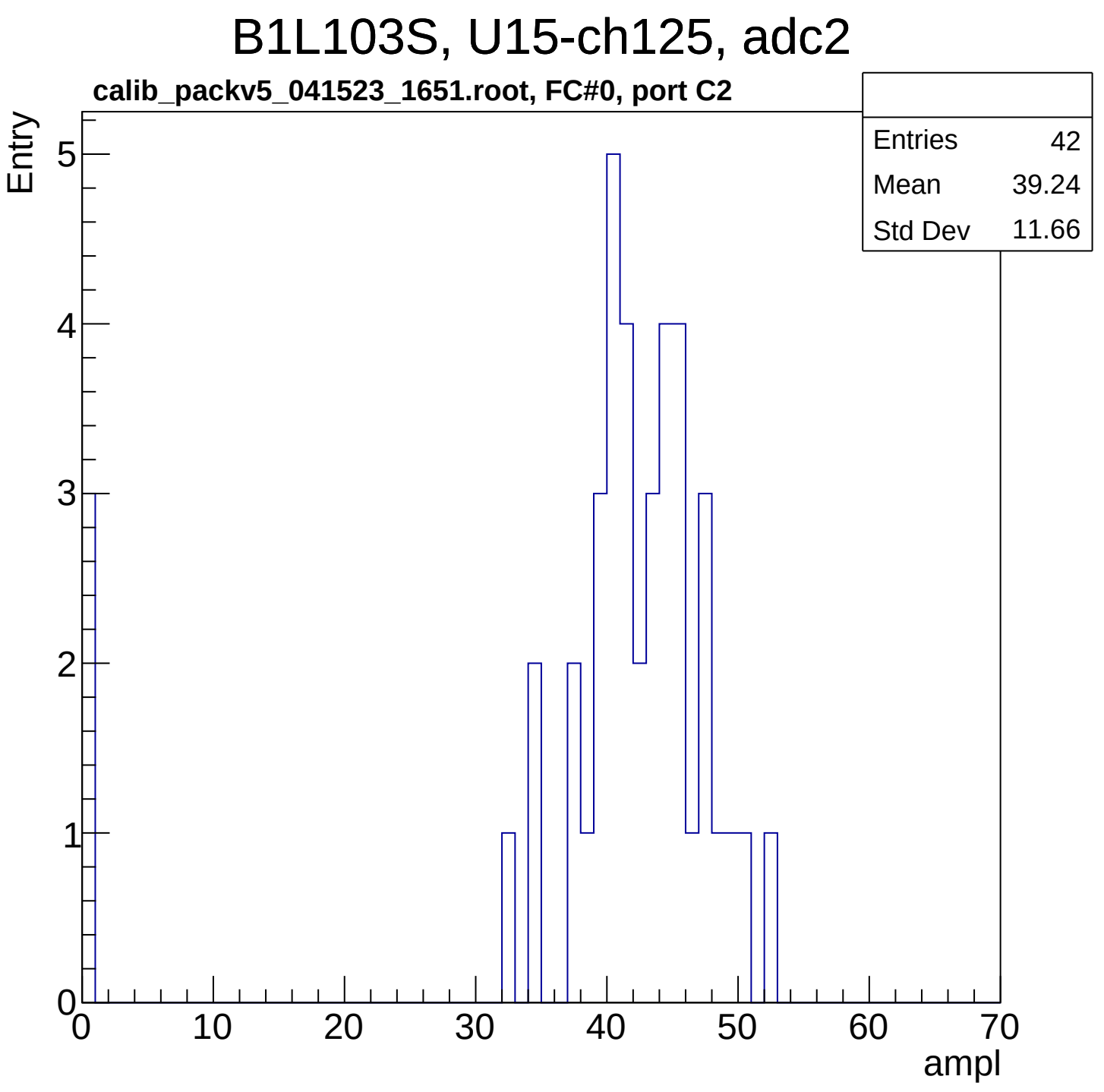

B1L103S, U15-ch124, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 55.96
Std Dev 3.263
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

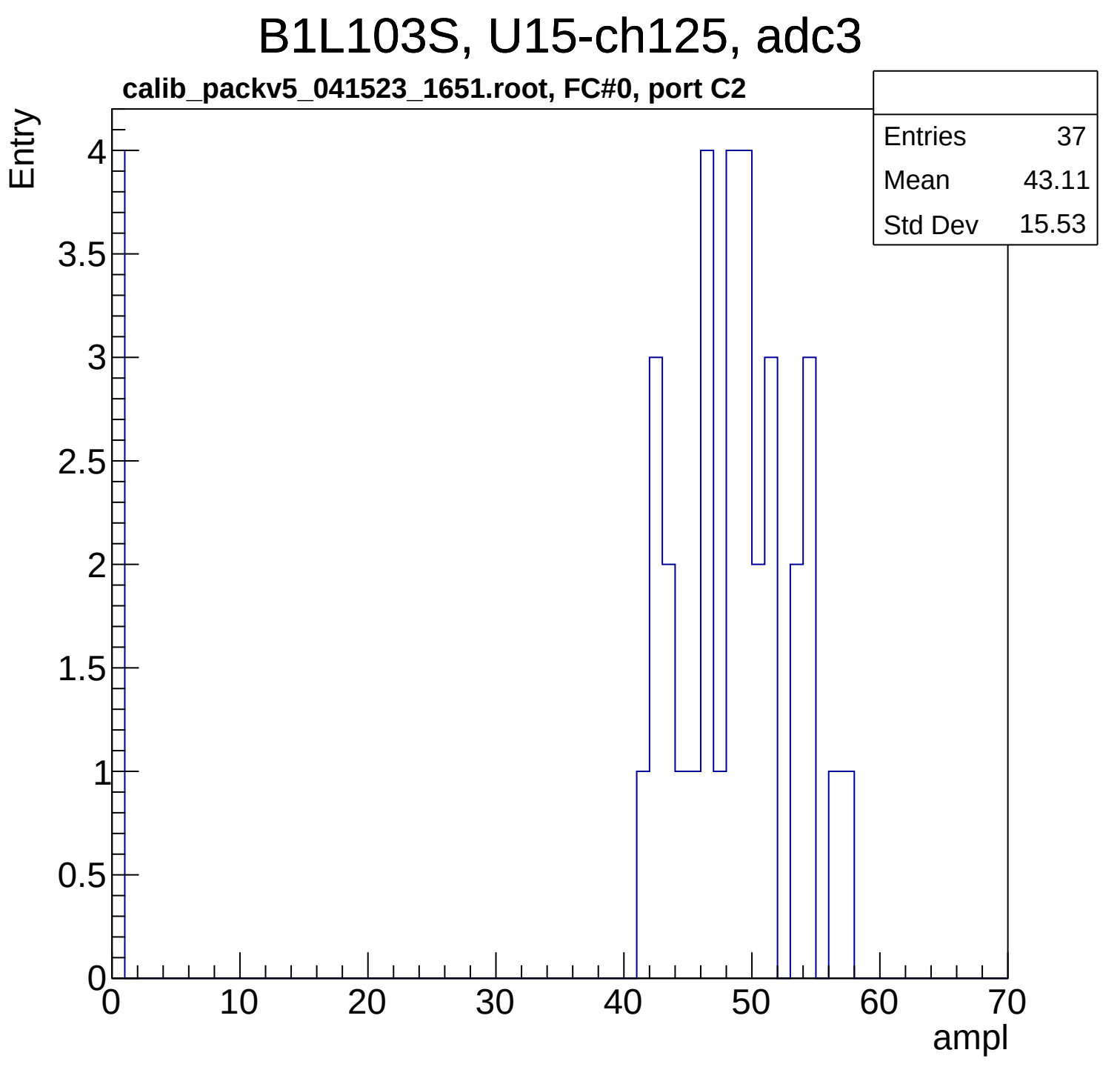

B1L103S, U15-ch124, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.47
Std Dev 1.194
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

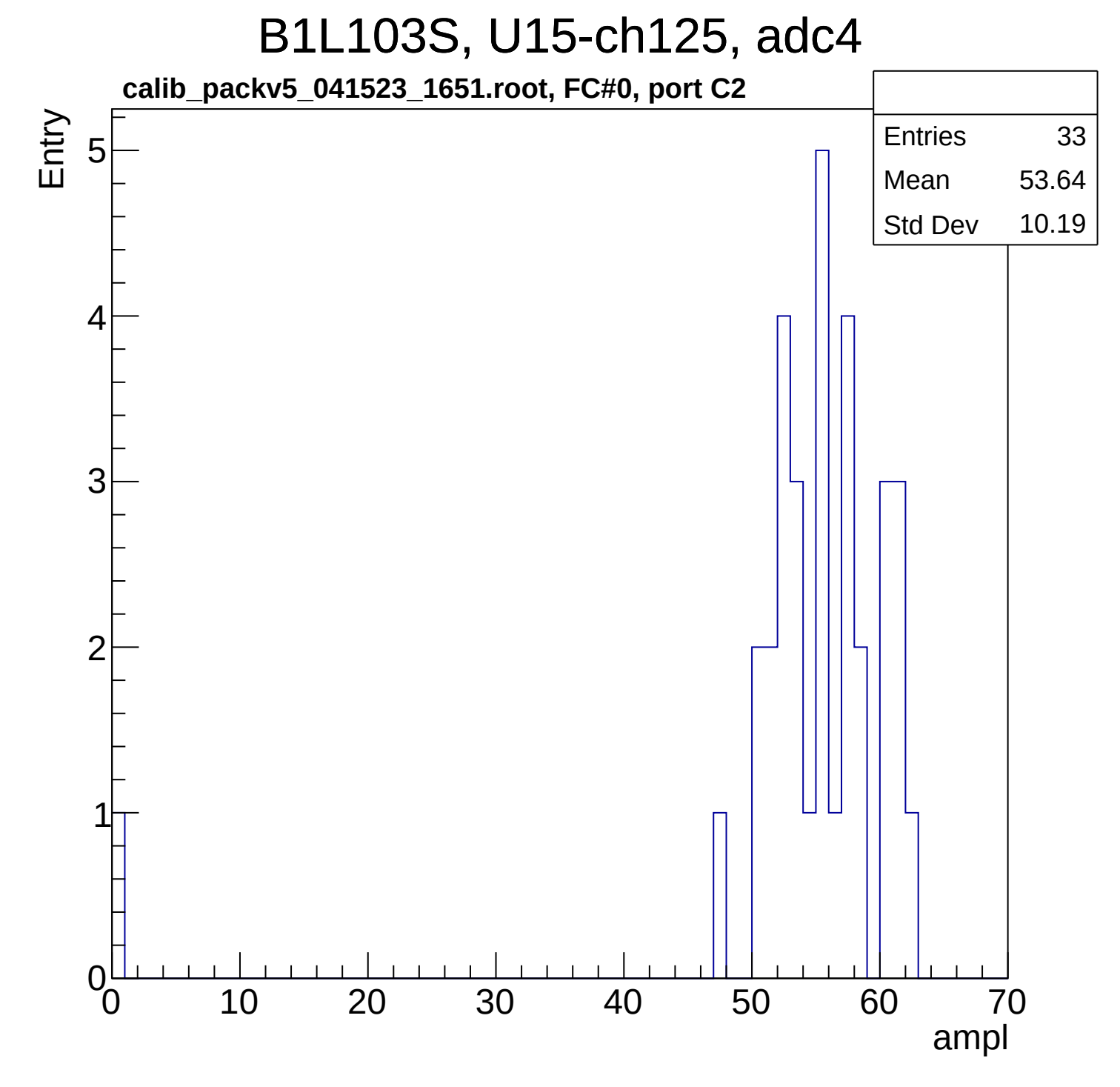

B1L103S, U15-ch124, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 5.727
Std Dev 18.11
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

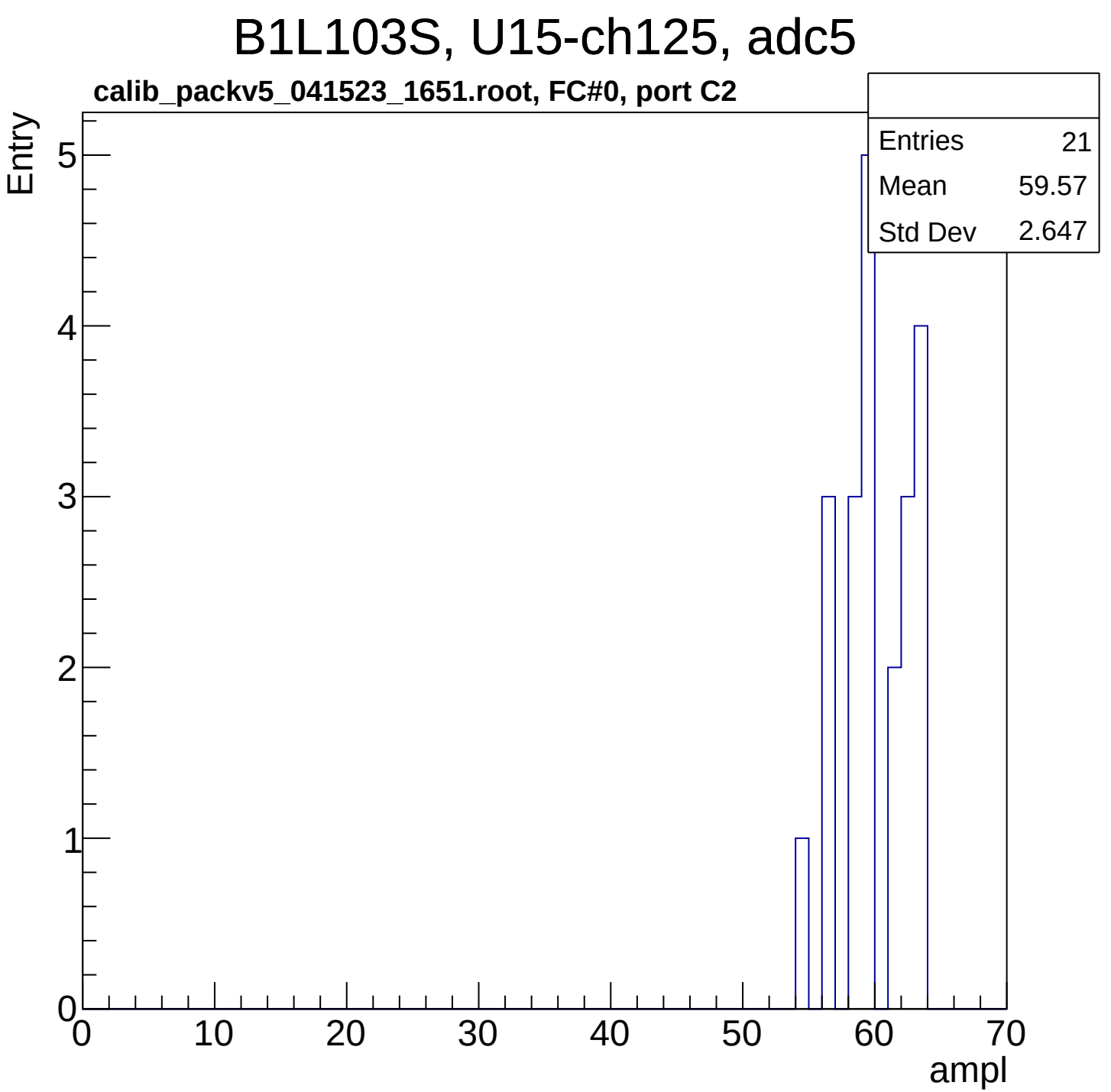

B1L103S, U15-ch125, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 23.64
Std Dev 11.97
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

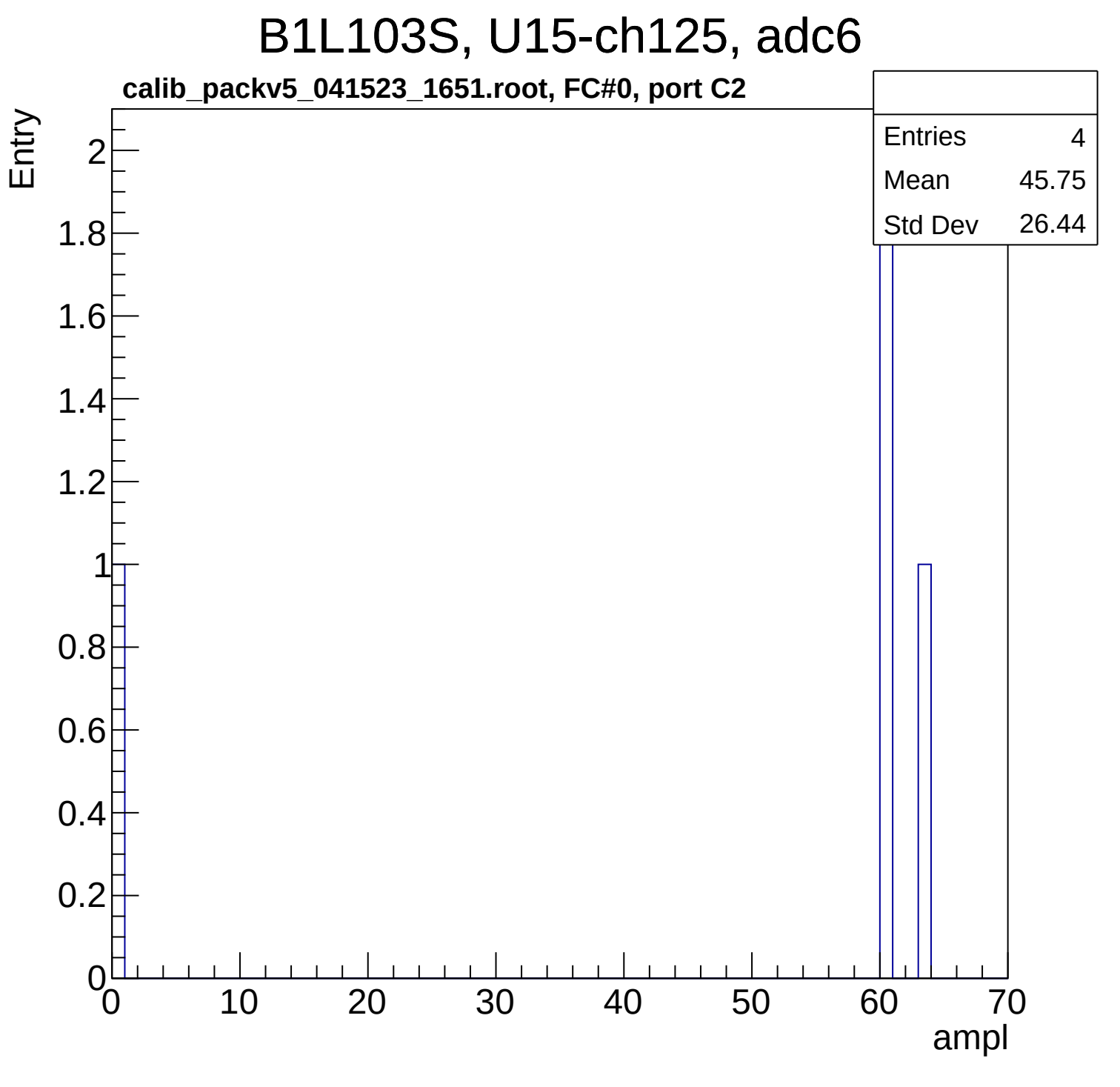

B1L103S, U15-ch125, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 34.04
Std Dev 7.224
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

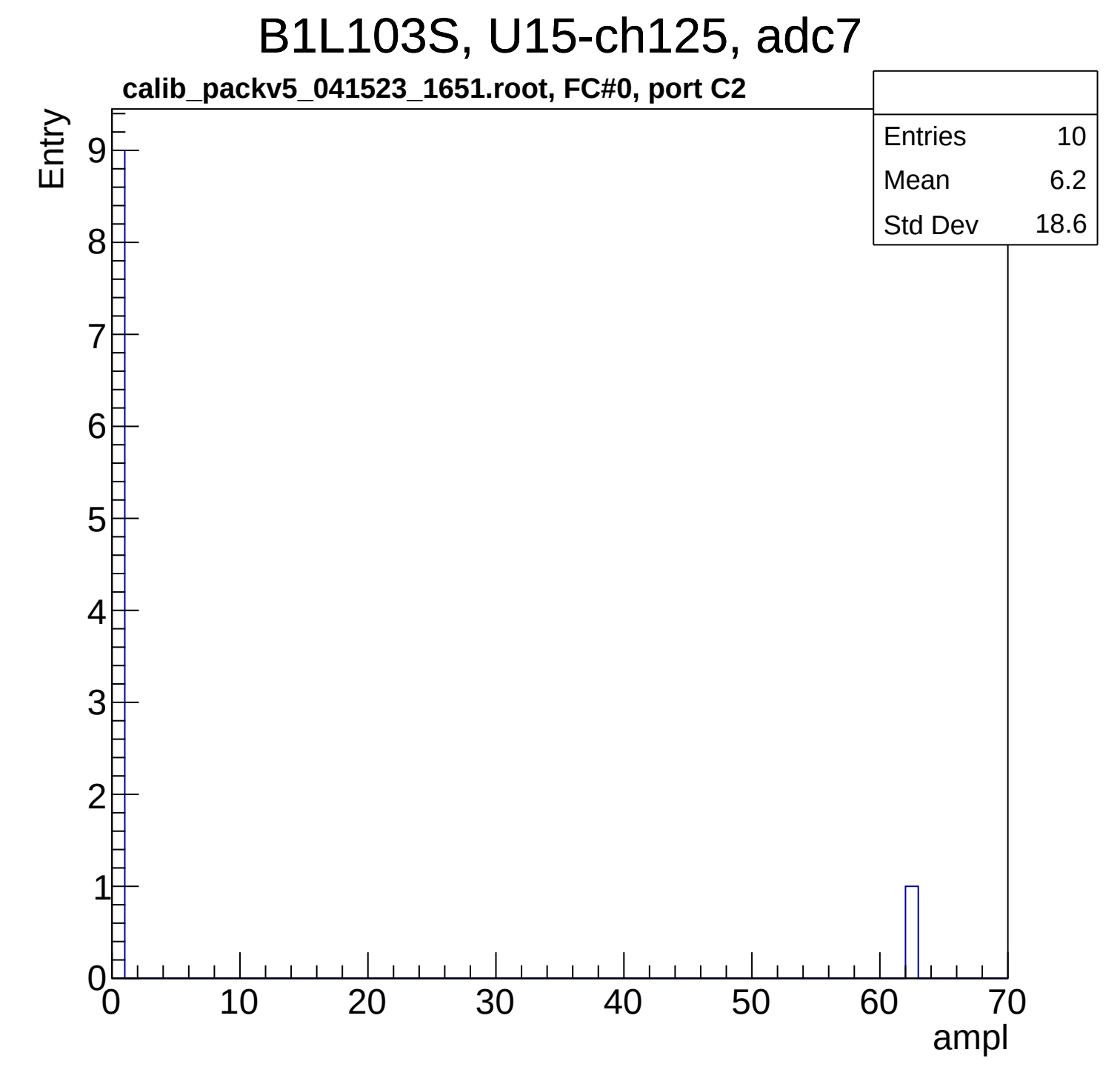

B1L103S, U15-ch125, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 39.24
Std Dev 11.66
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

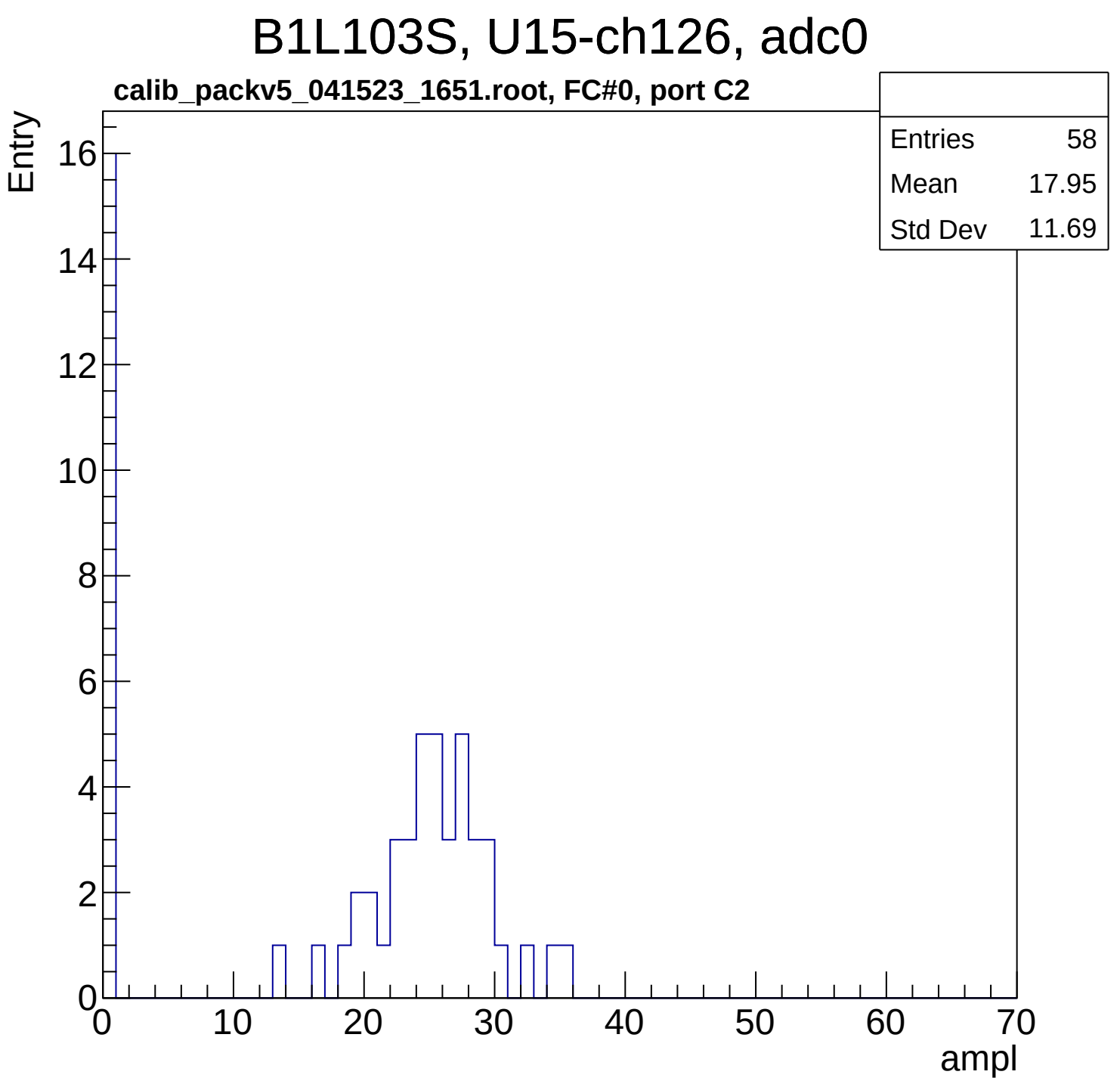

B1L103S, U15-ch125, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 43.11
Std Dev 15.53
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

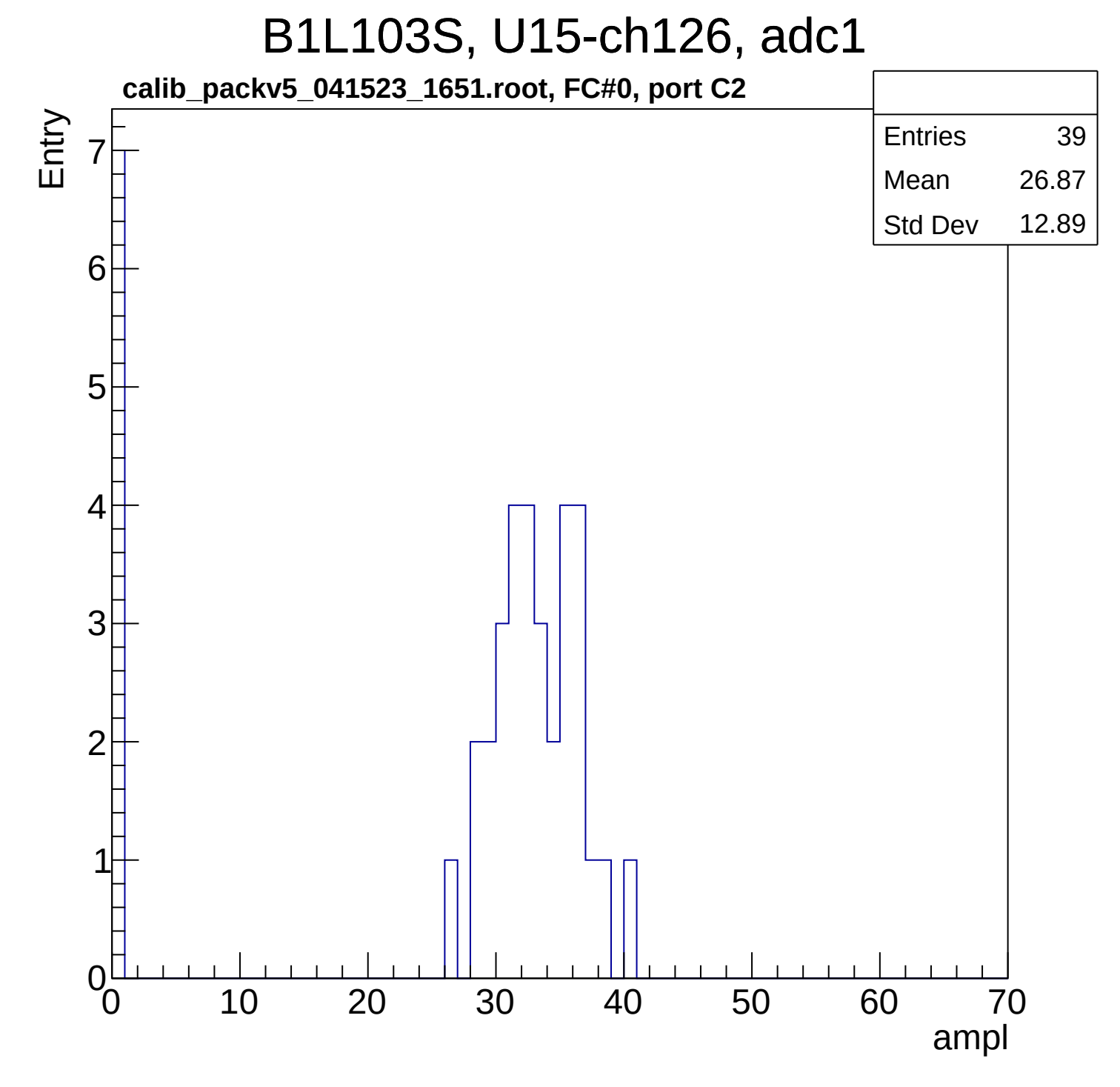

B1L103S, U15-ch125, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 53.64
Std Dev 10.19
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

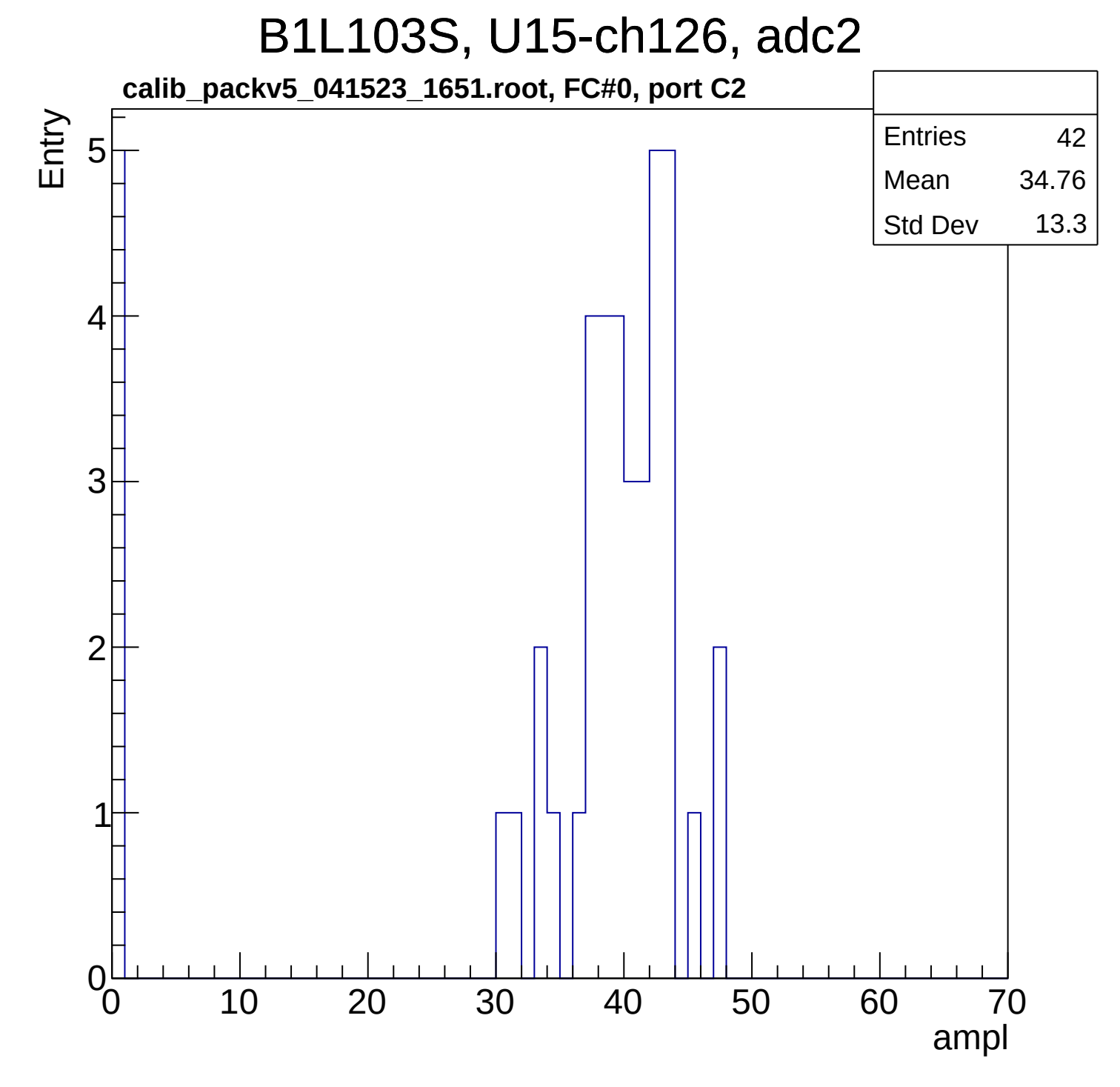

B1L103S, U15-ch125, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 59.57
Std Dev 2.647
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

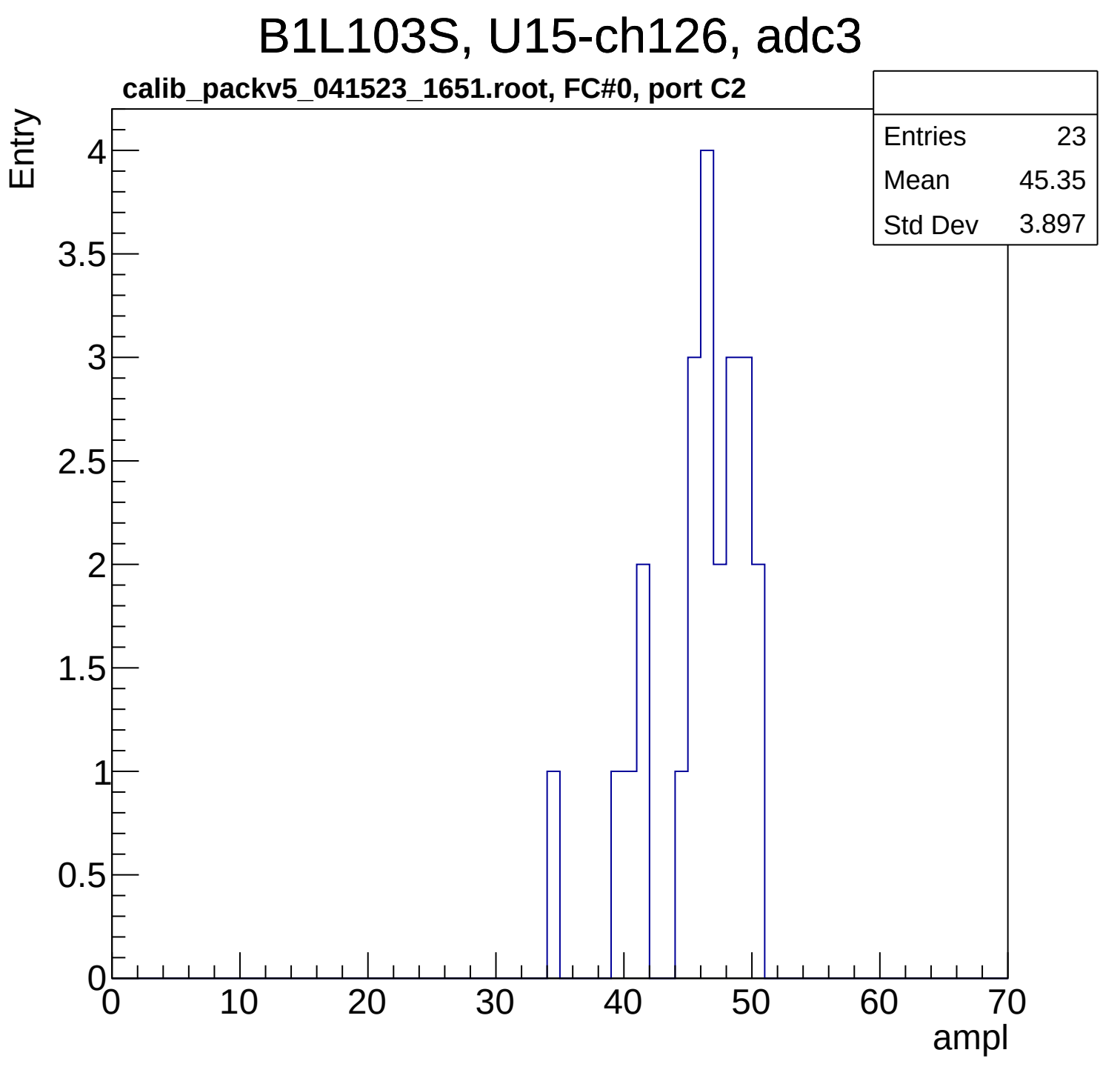

B1L103S, U15-ch125, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 45.75
Std Dev 26.44
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U15-ch125, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 6.2
Std Dev 18.6
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U15-ch126, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 17.95
Std Dev 11.69
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch126, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 26.87
Std Dev 12.89
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U15-ch126, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 34.76
Std Dev 13.3
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch126, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 45.35
Std Dev 3.897
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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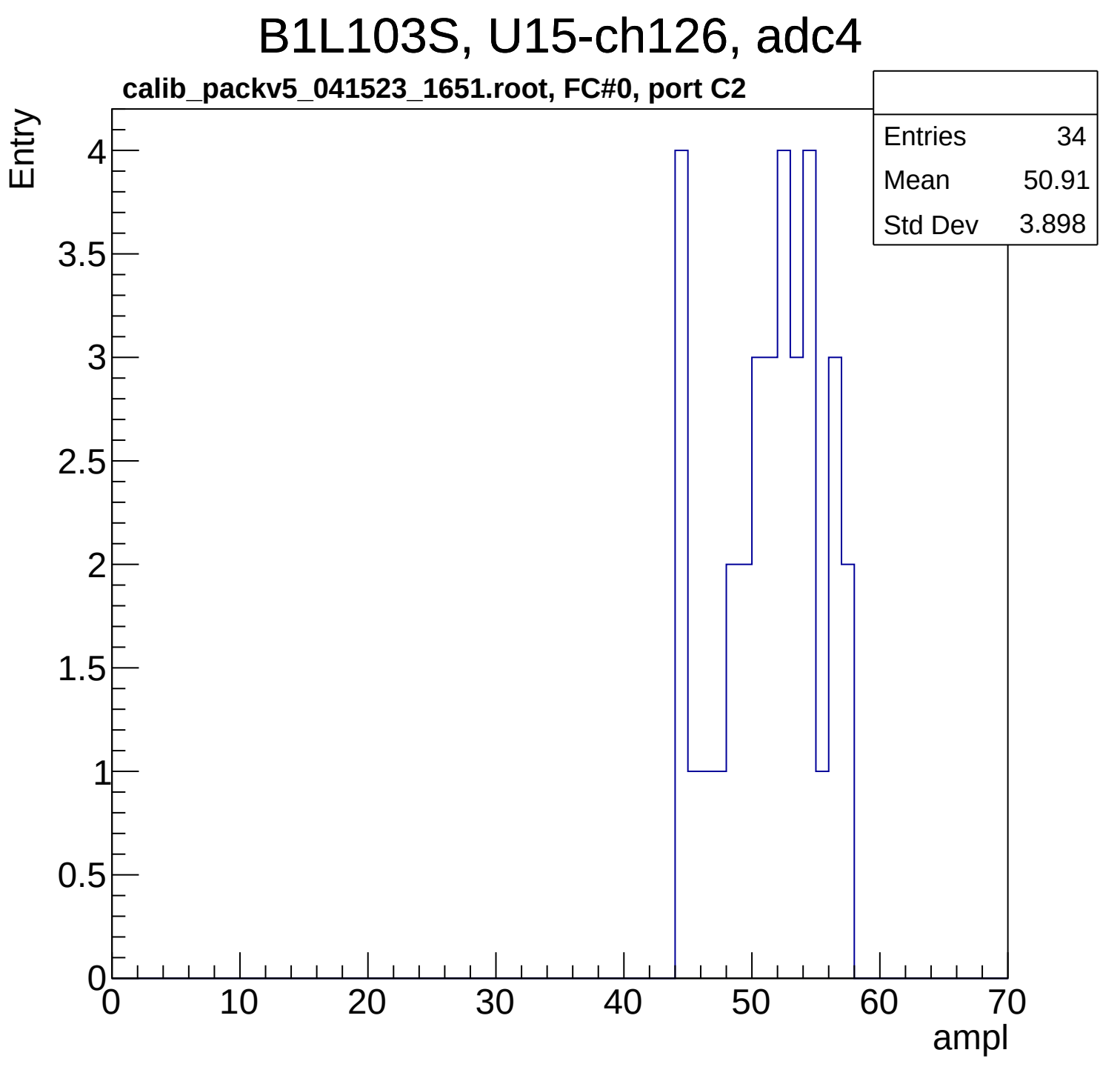
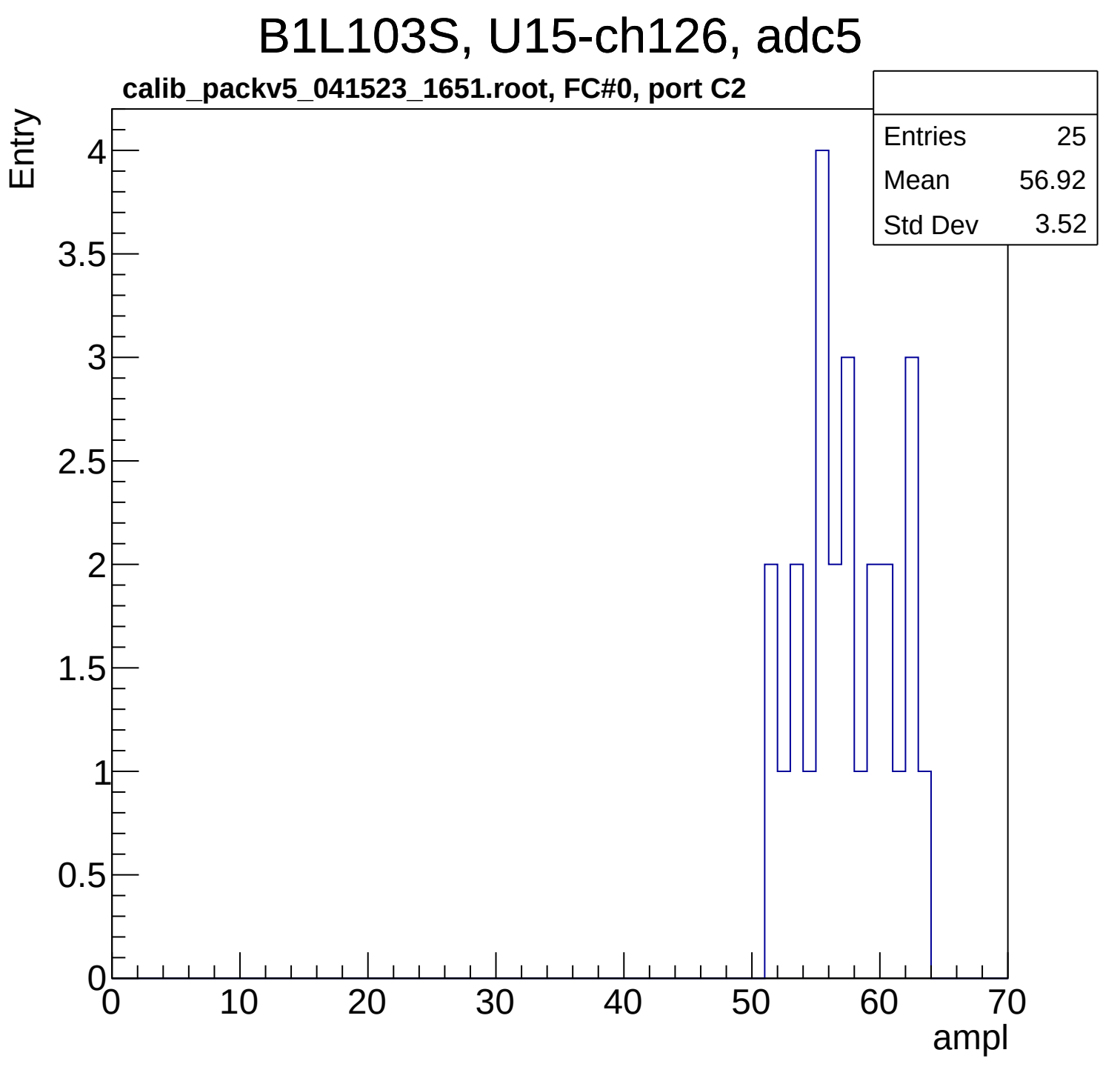
40
50
60
70


B1L103S, U15-ch126, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 50.91
Std Dev 3.898
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch126, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 56.92
Std Dev 3.52
Entry
ampl
0
0.5
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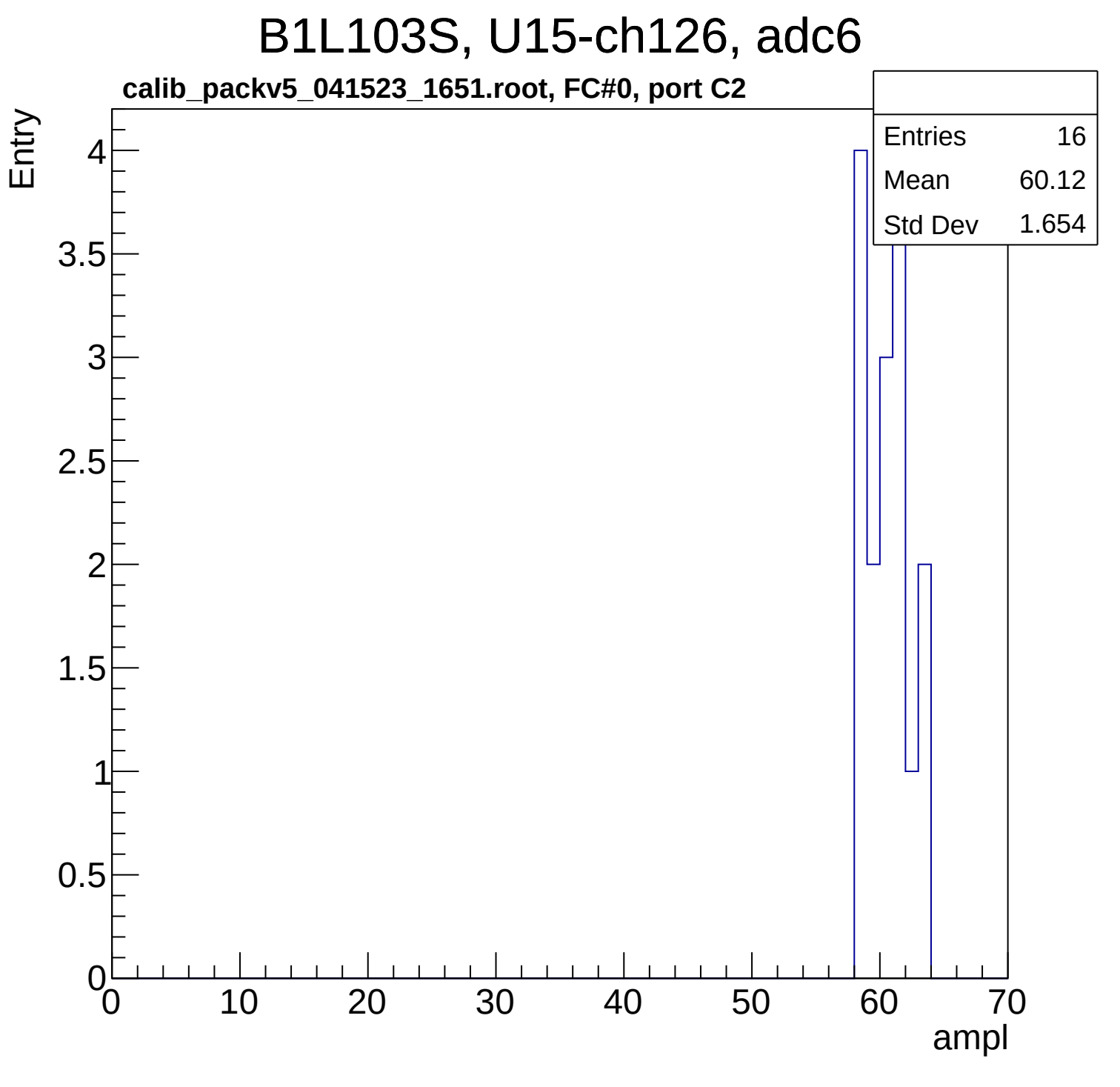
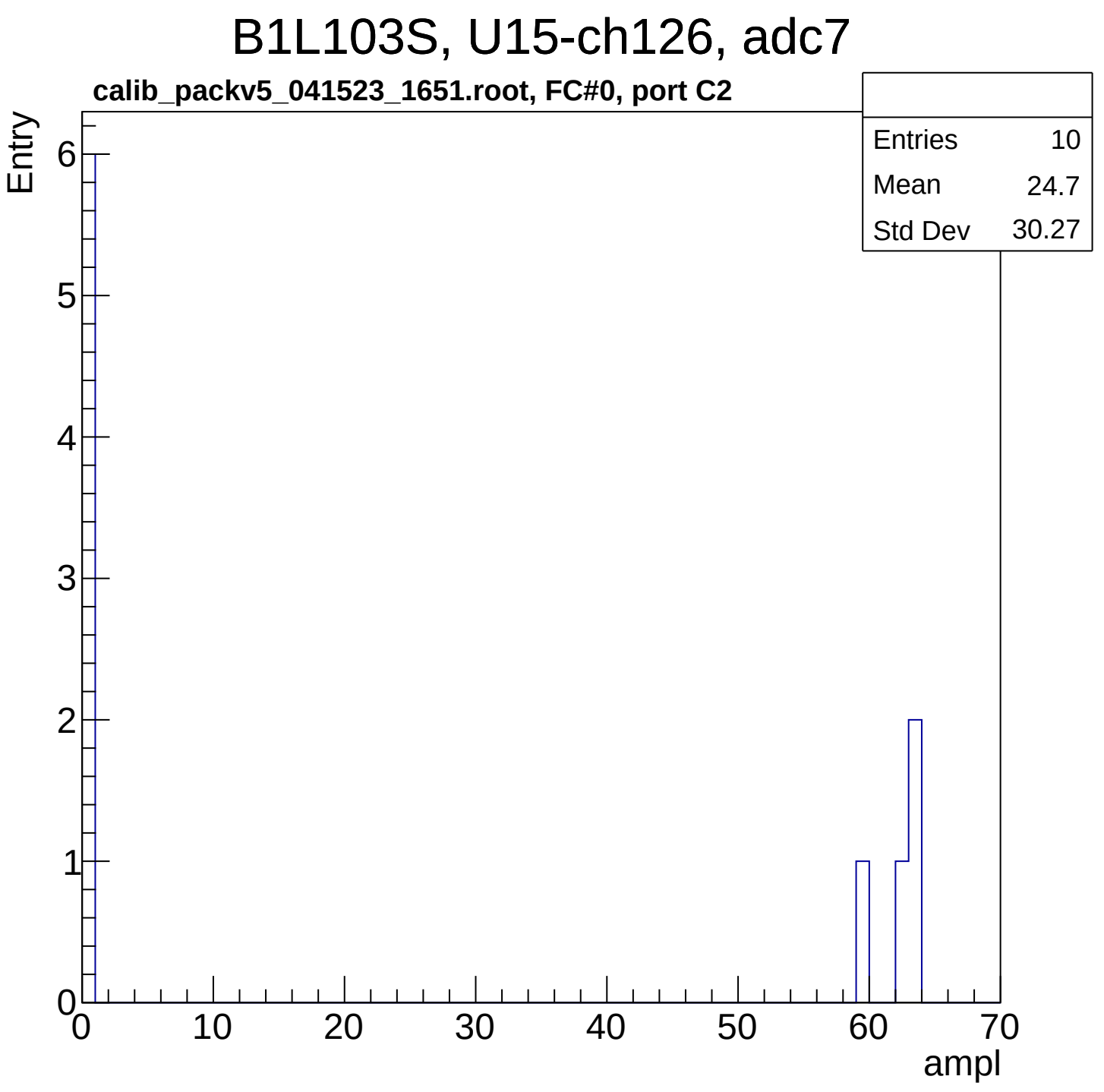
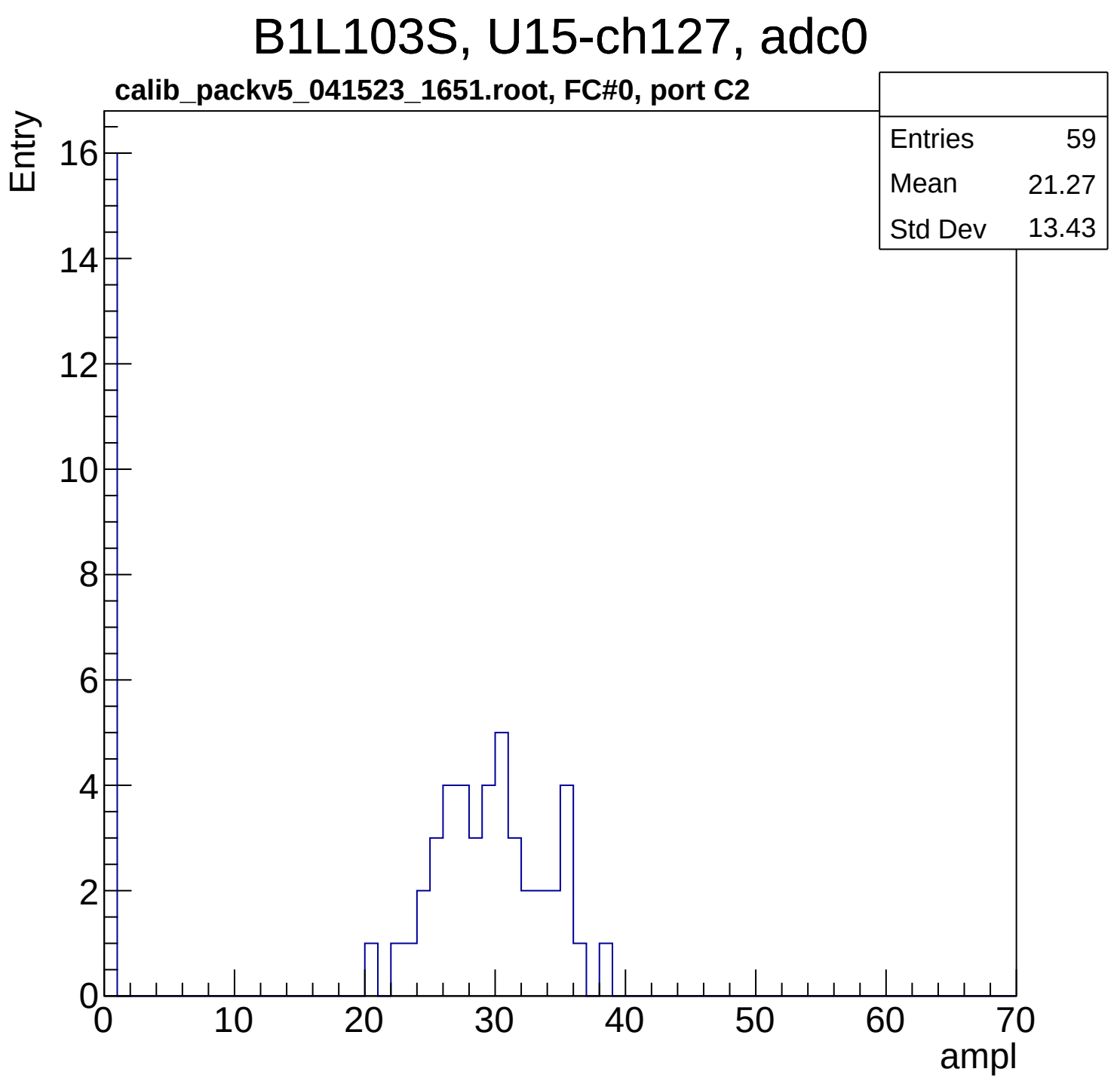
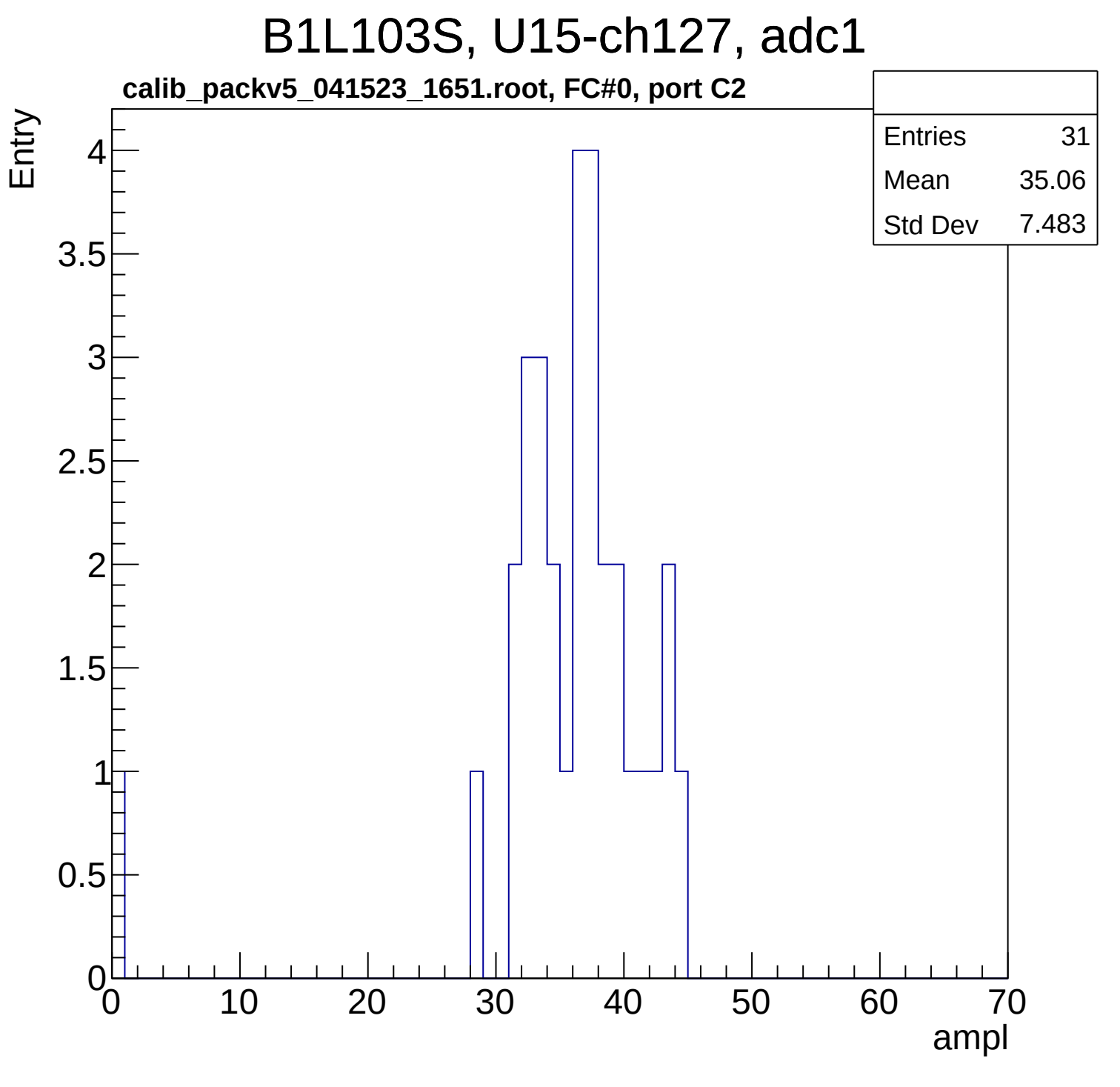
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch126, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 60.12
Std Dev 1.654
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U15-ch126, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 24.7
Std Dev 30.27
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch127, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 21.27
Std Dev 13.43
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U15-ch127, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 35.06
Std Dev 7.483
Entry
ampl
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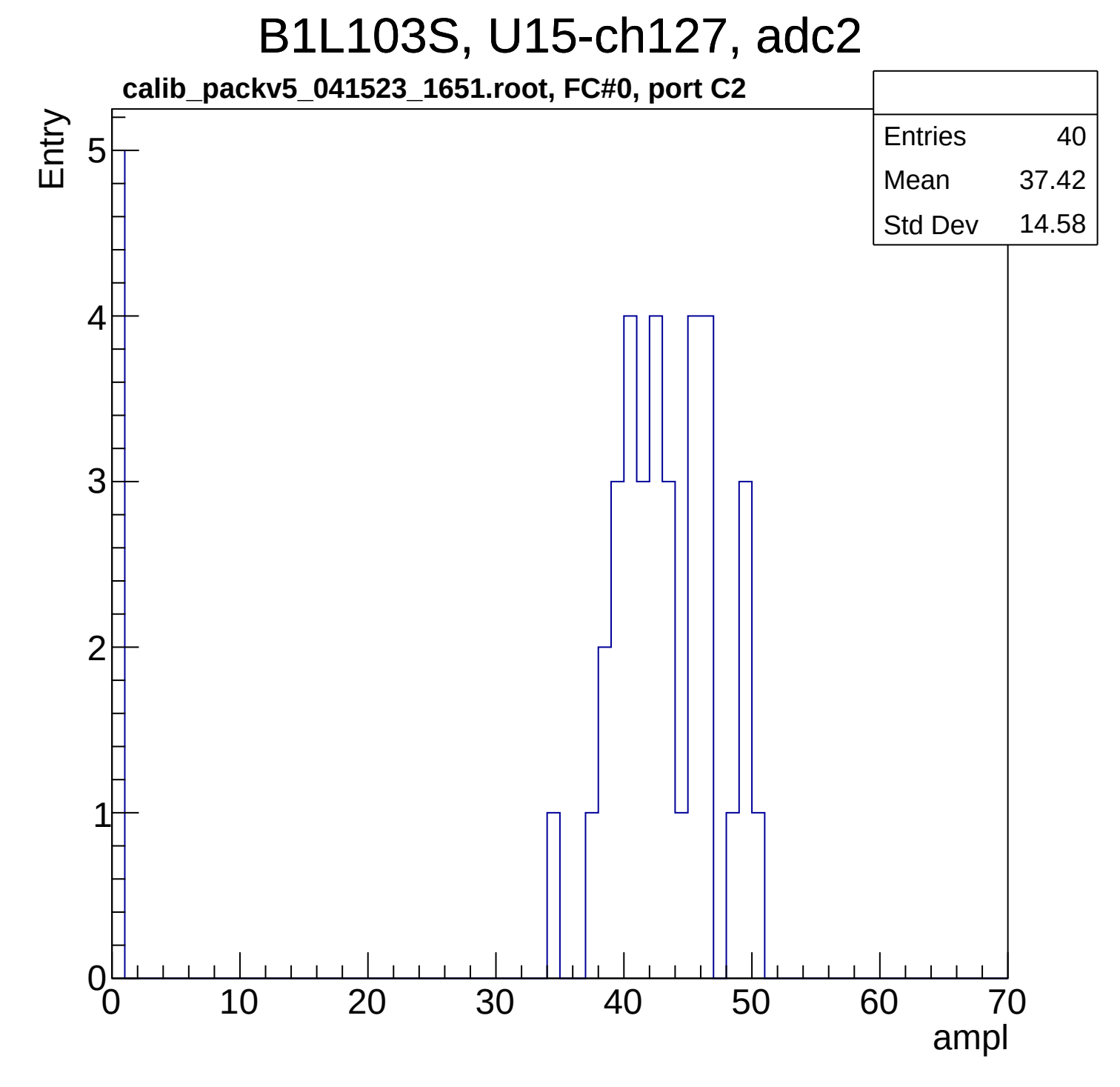
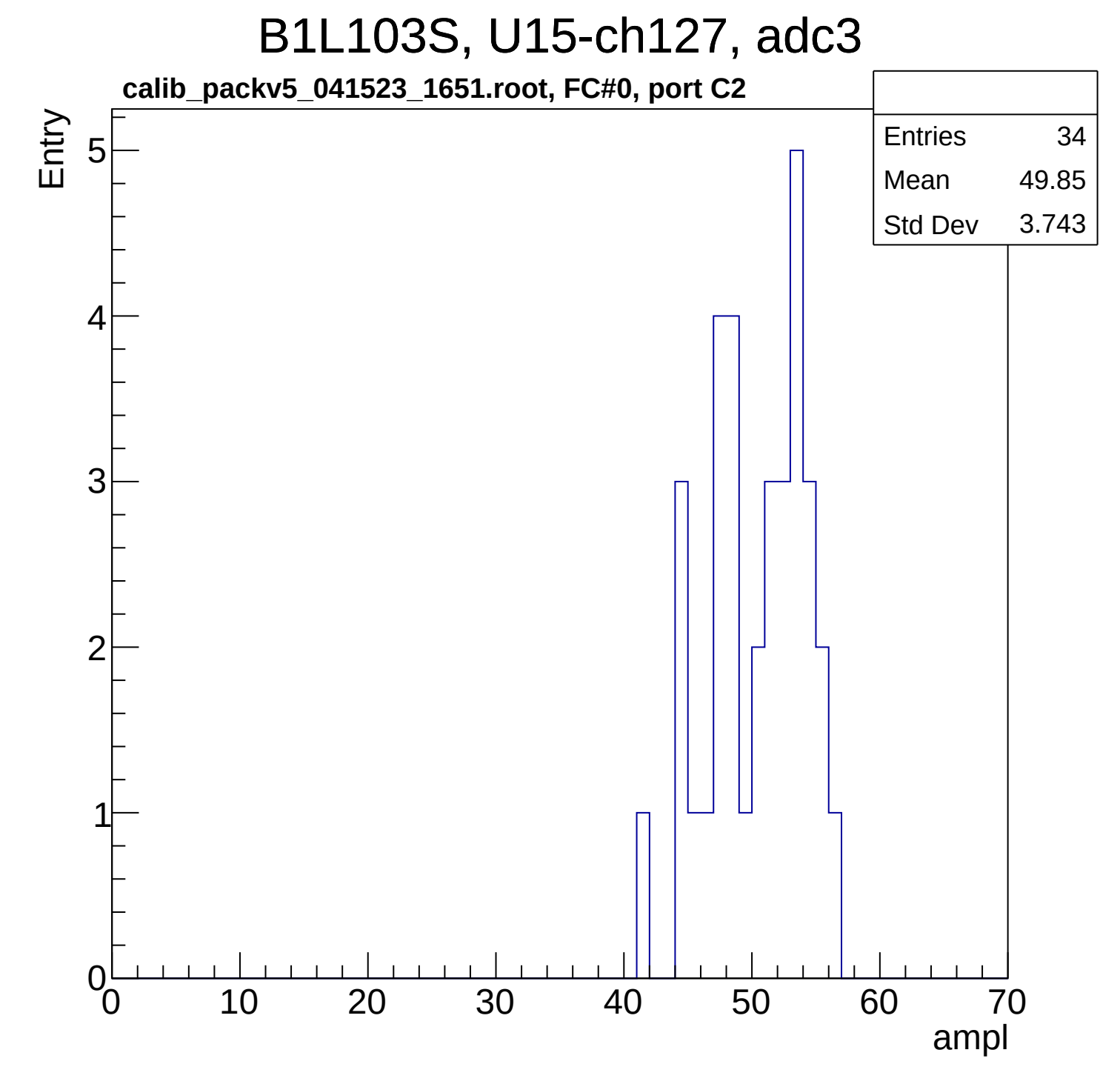
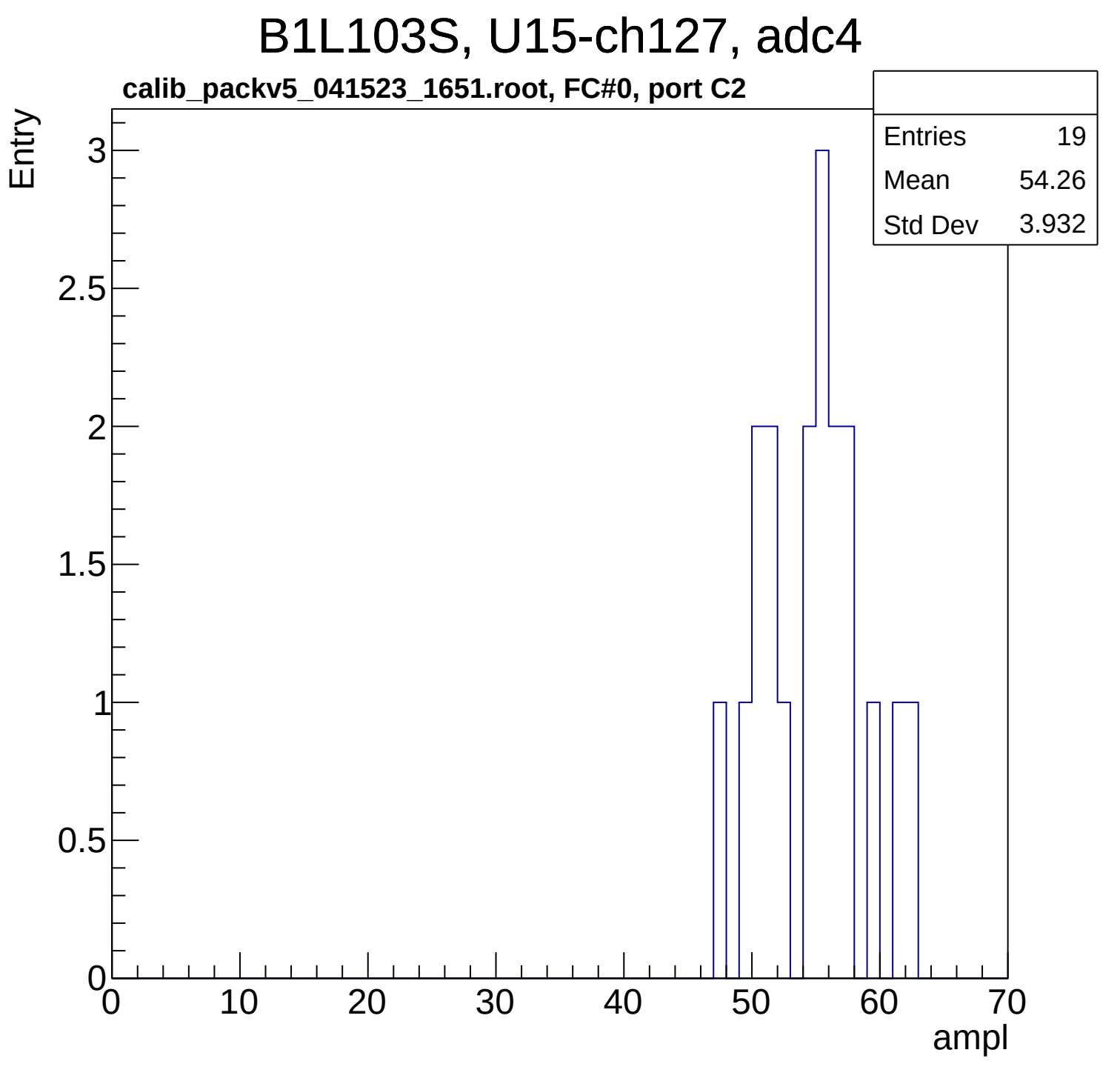
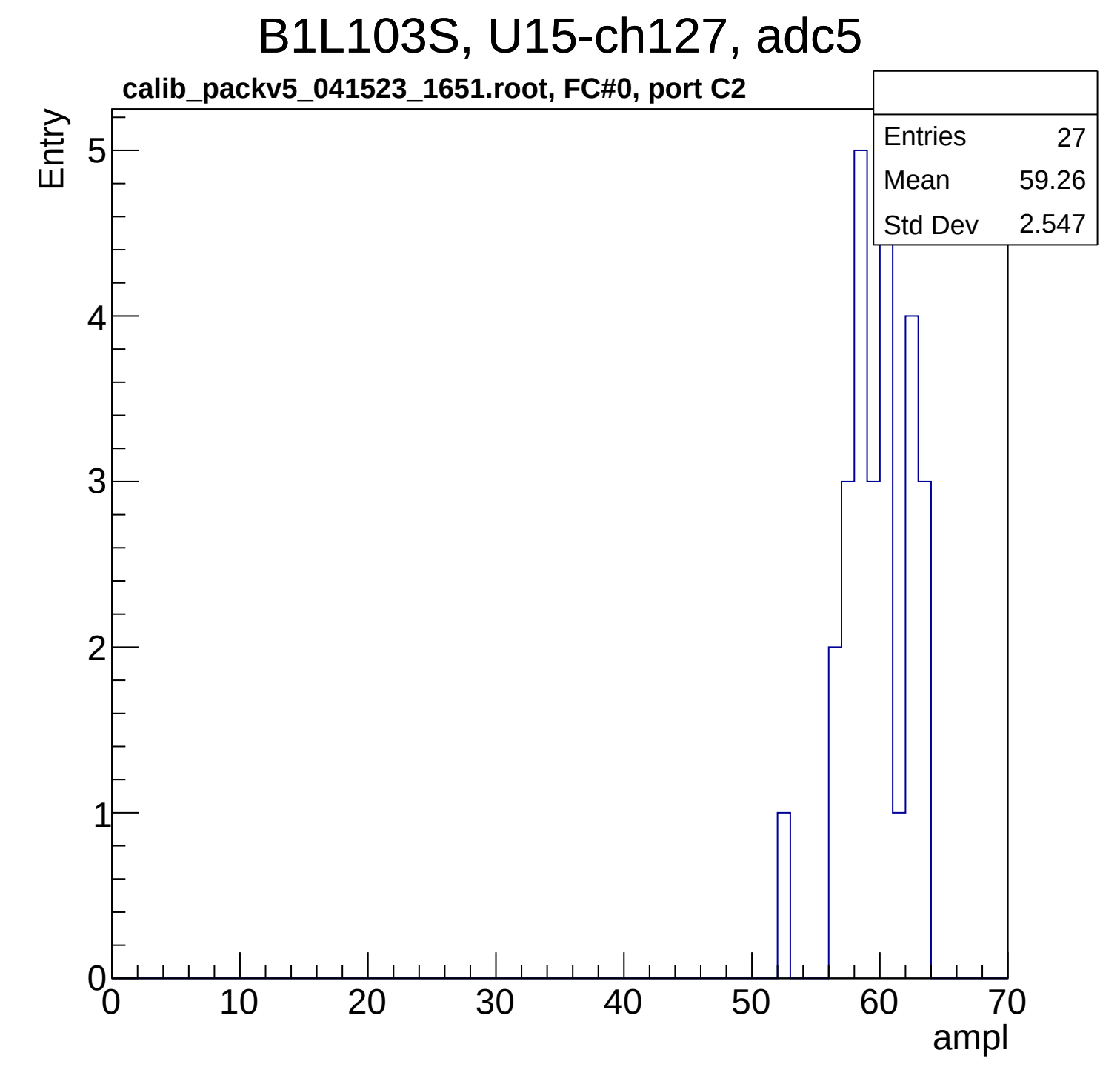
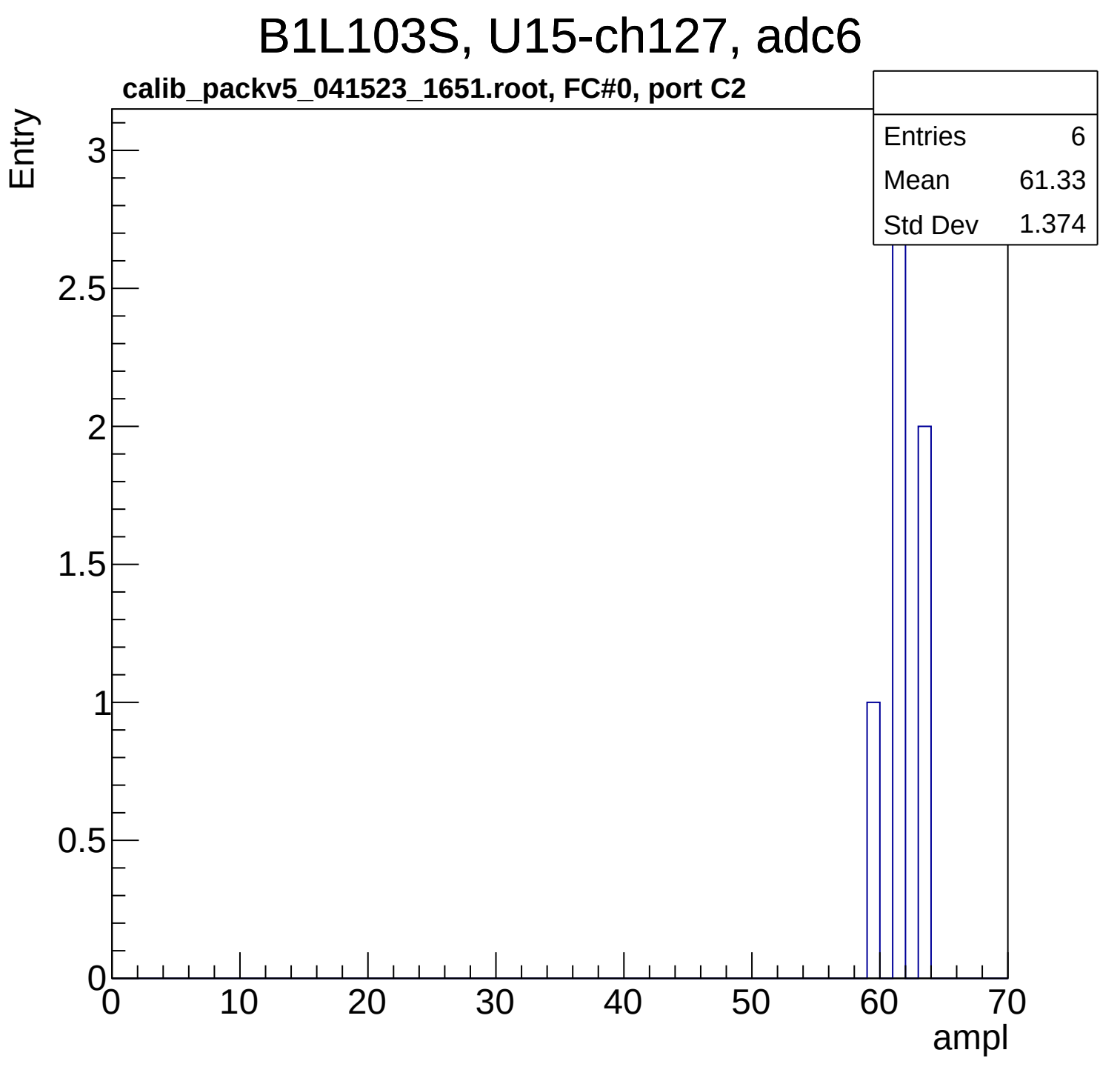
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

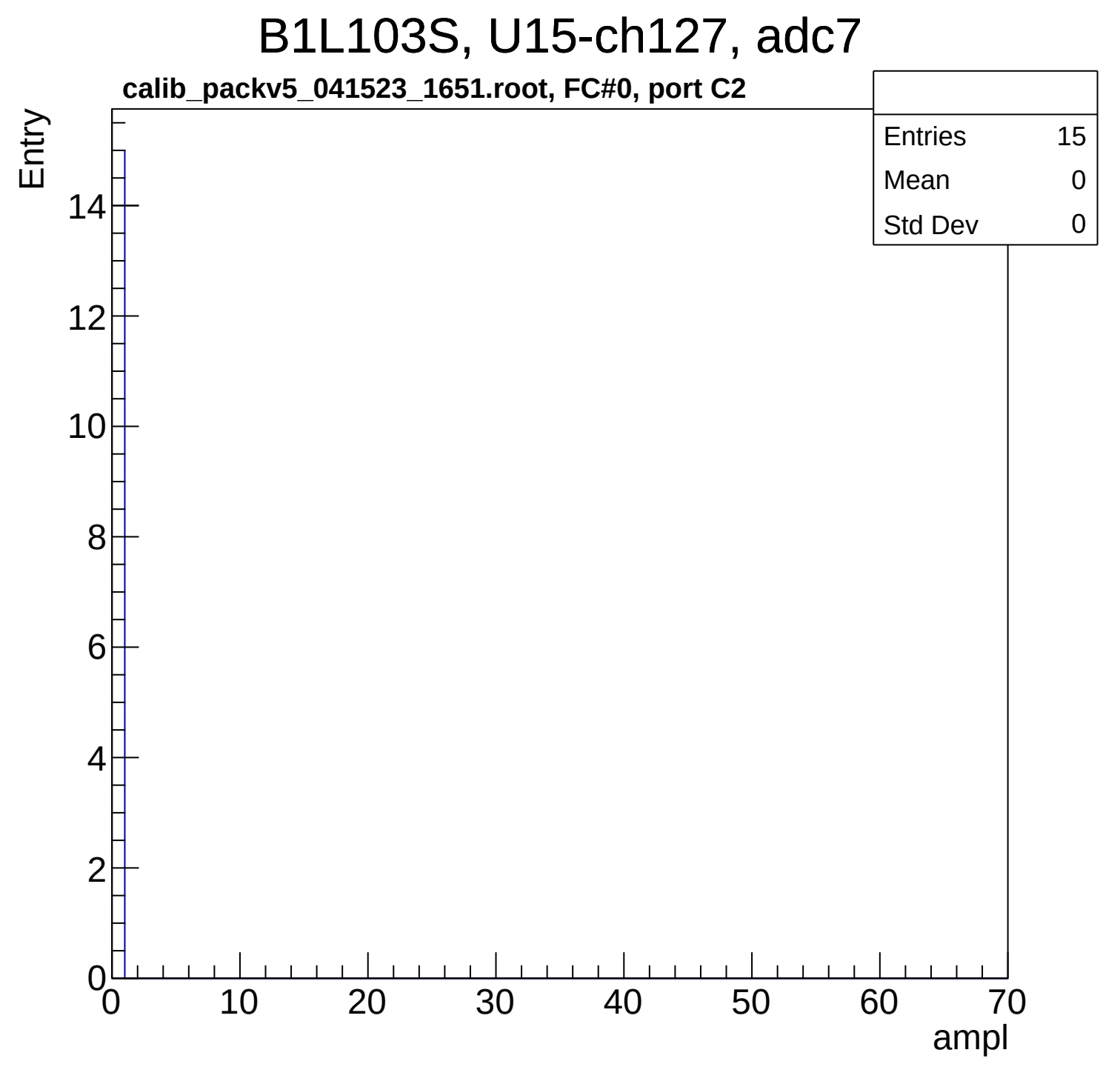

B1L103S, U15-ch127, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 37.42
Std Dev 14.58
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

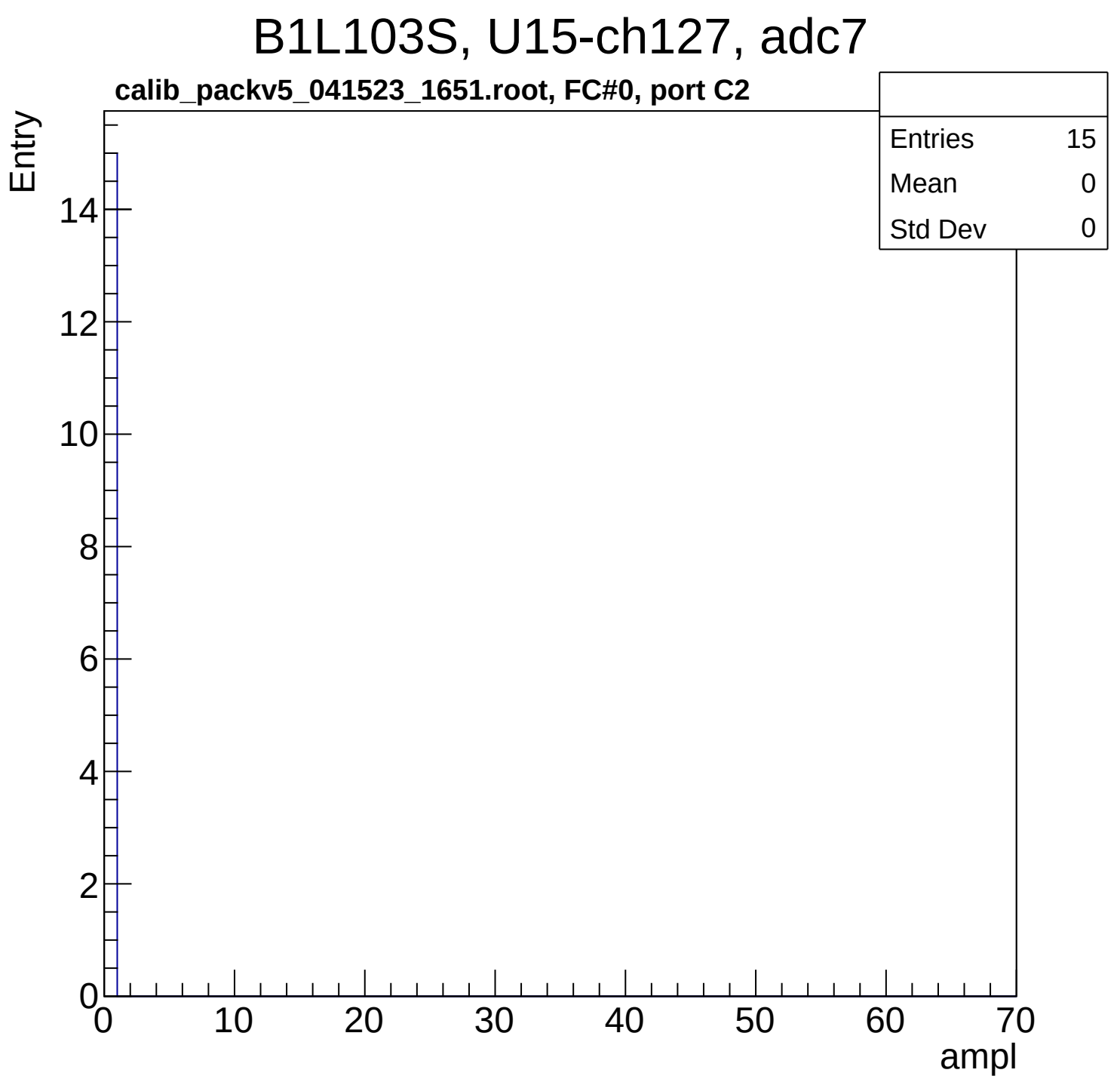

B1L103S, U15-ch127, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 49.85
Std Dev 3.743
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch127, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 54.26
Std Dev 3.932
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch127, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 59.26
Std Dev 2.547
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U15-ch127, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.33
Std Dev 1.374
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U15-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl