

B1L101S, U11-ch0

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.28
Std Dev	11.72

Turn on : 27.5389

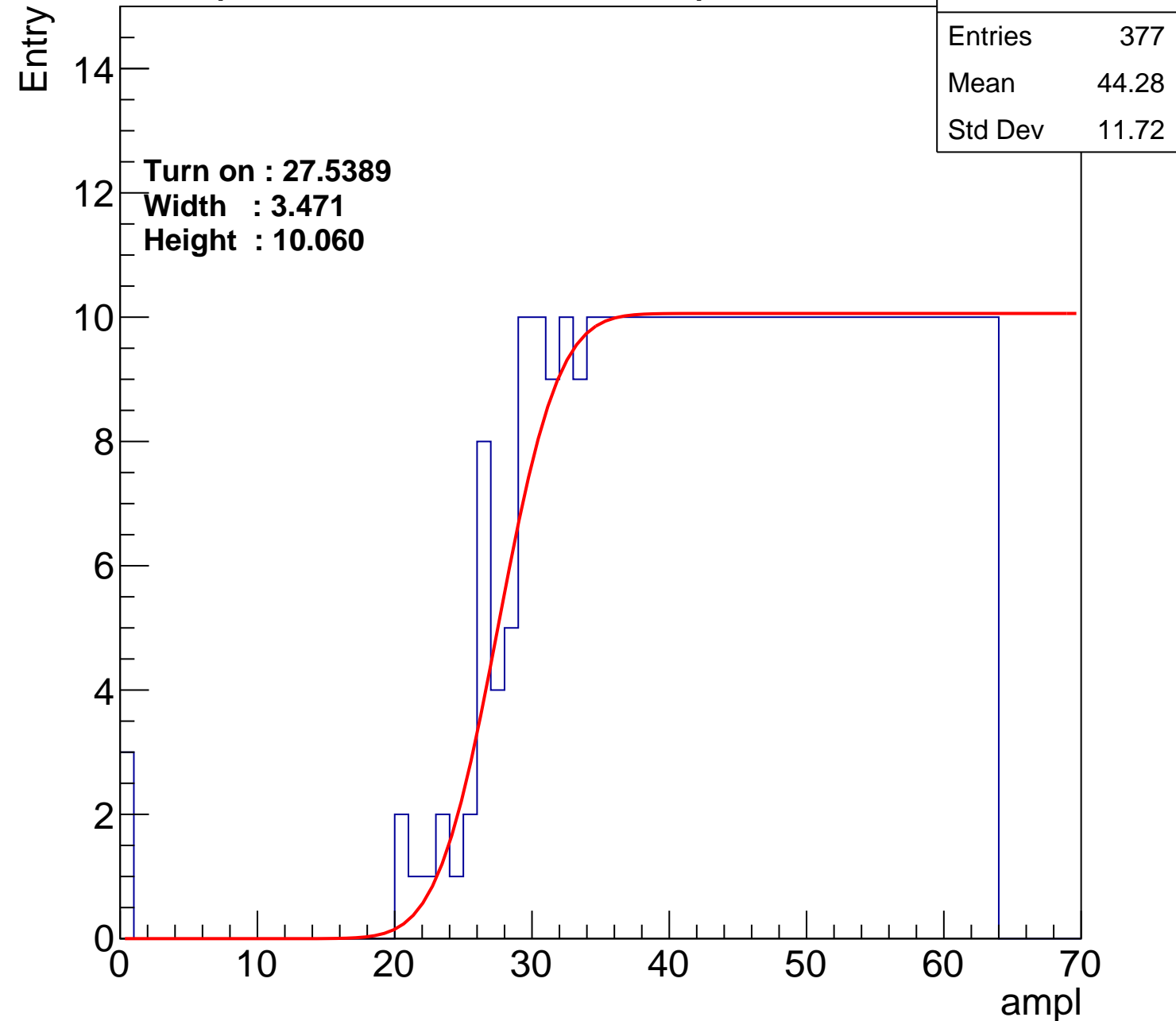
Width : 3.471

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch1

calib_packv5_042523_0143.root, FC#0, port D2

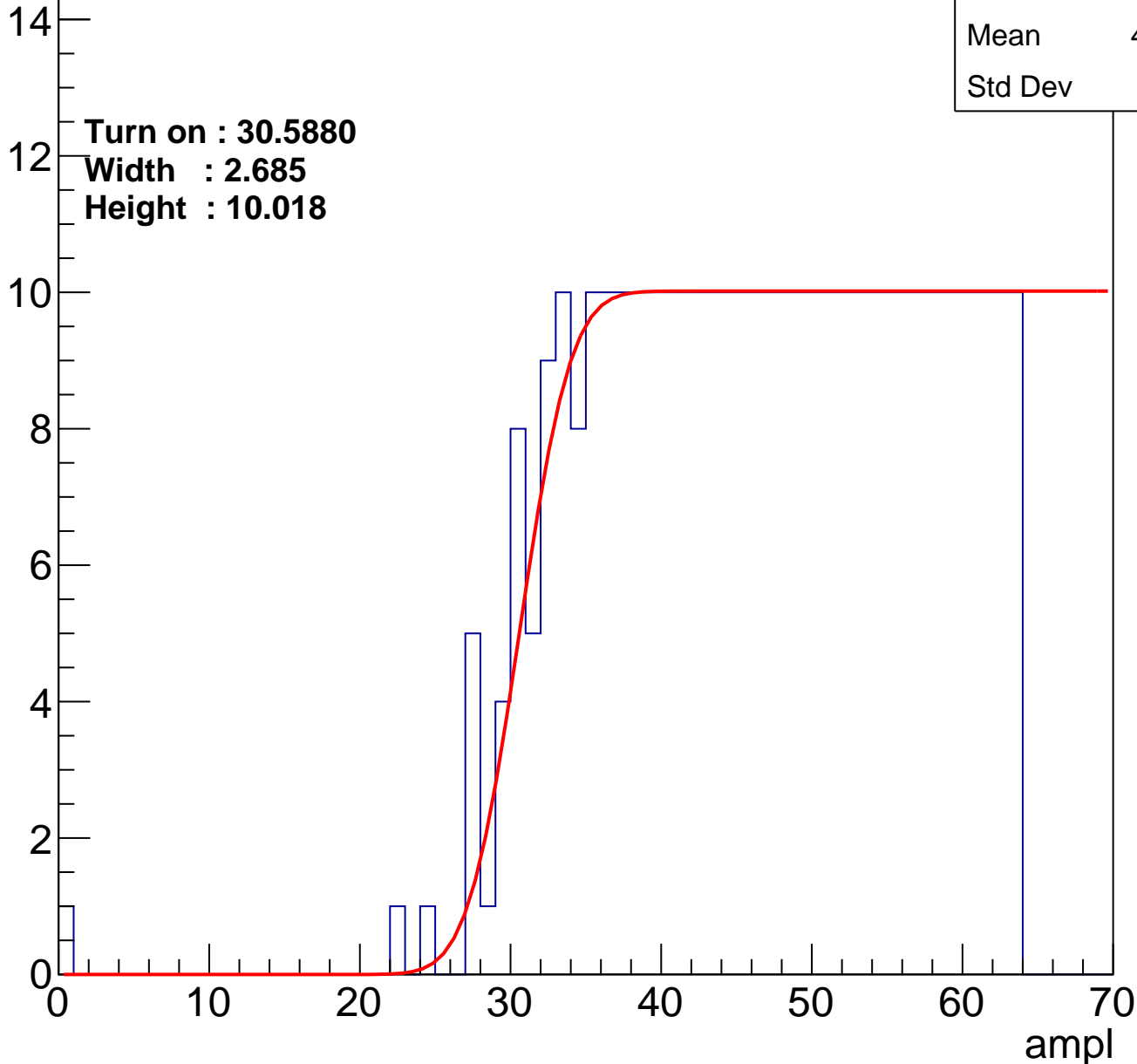
Entries	343
Mean	46.12
Std Dev	10.41

Turn on : 30.5880

Width : 2.685

Height : 10.018

Entry



B1L101S, U11-ch2

calib_packv5_042523_0143.root, FC#0, port D2

Entries	380
Mean	44.31
Std Dev	11.37

Turn on : 26.3336

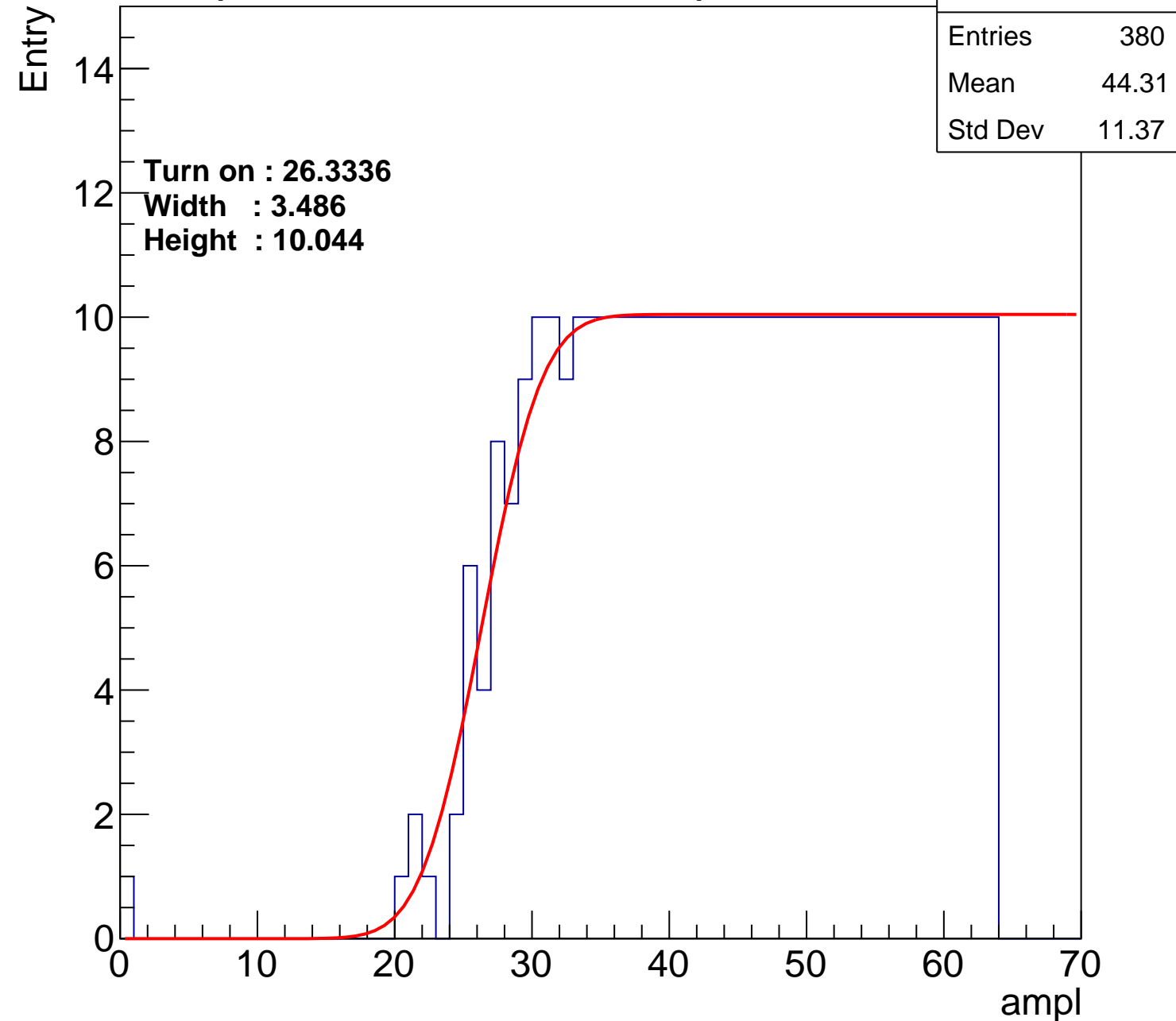
Width : 3.486

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch3

calib_packv5_042523_0143.root, FC#0, port D2

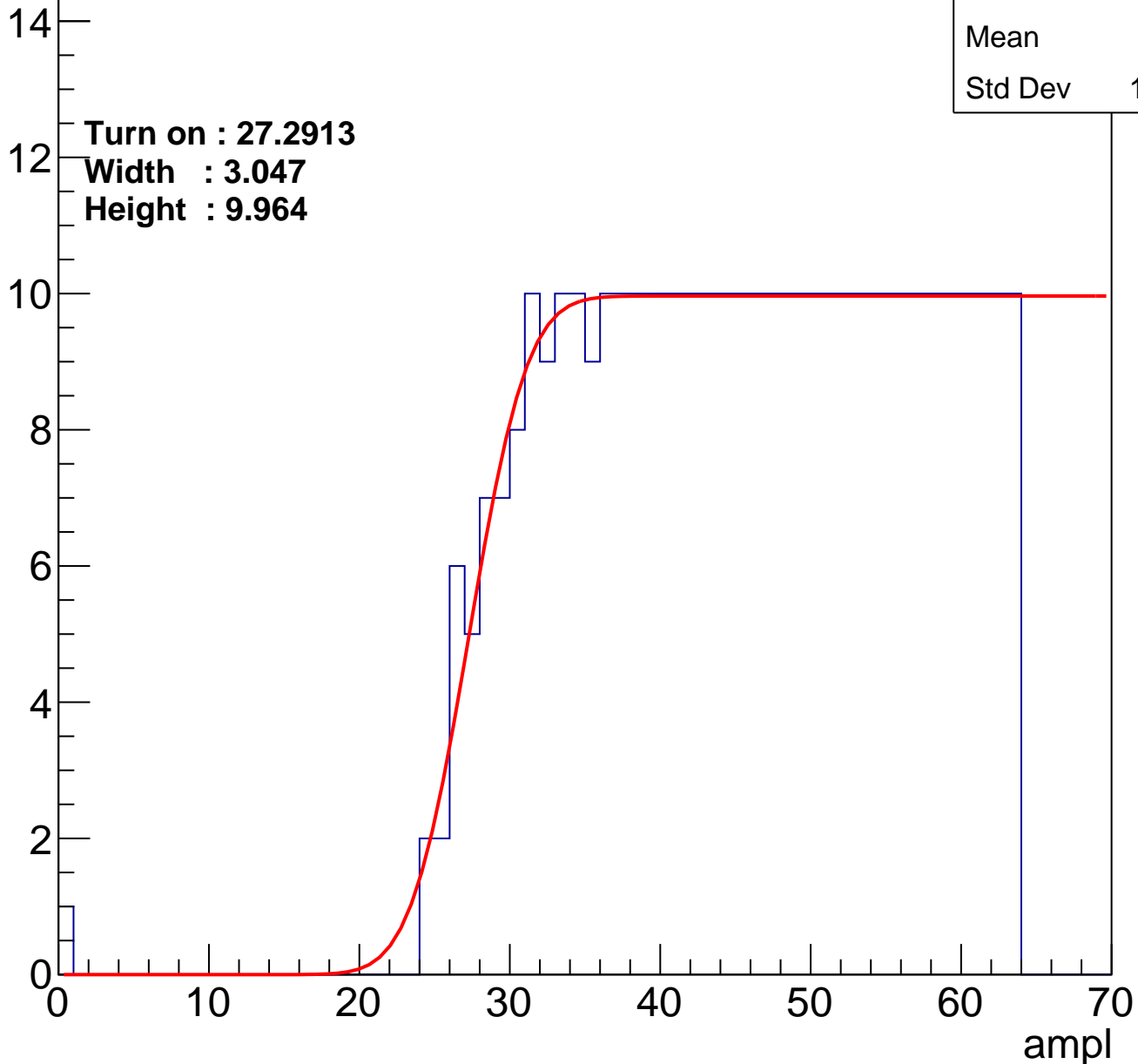
Entries	366
Mean	45
Std Dev	10.97

Turn on : 27.2913

Width : 3.047

Height : 9.964

Entry



B1L101S, U11-ch4

calib_packv5_042523_0143.root, FC#0, port D2

Entries	373
Mean	44.29
Std Dev	12.14

Turn on : 27.7586

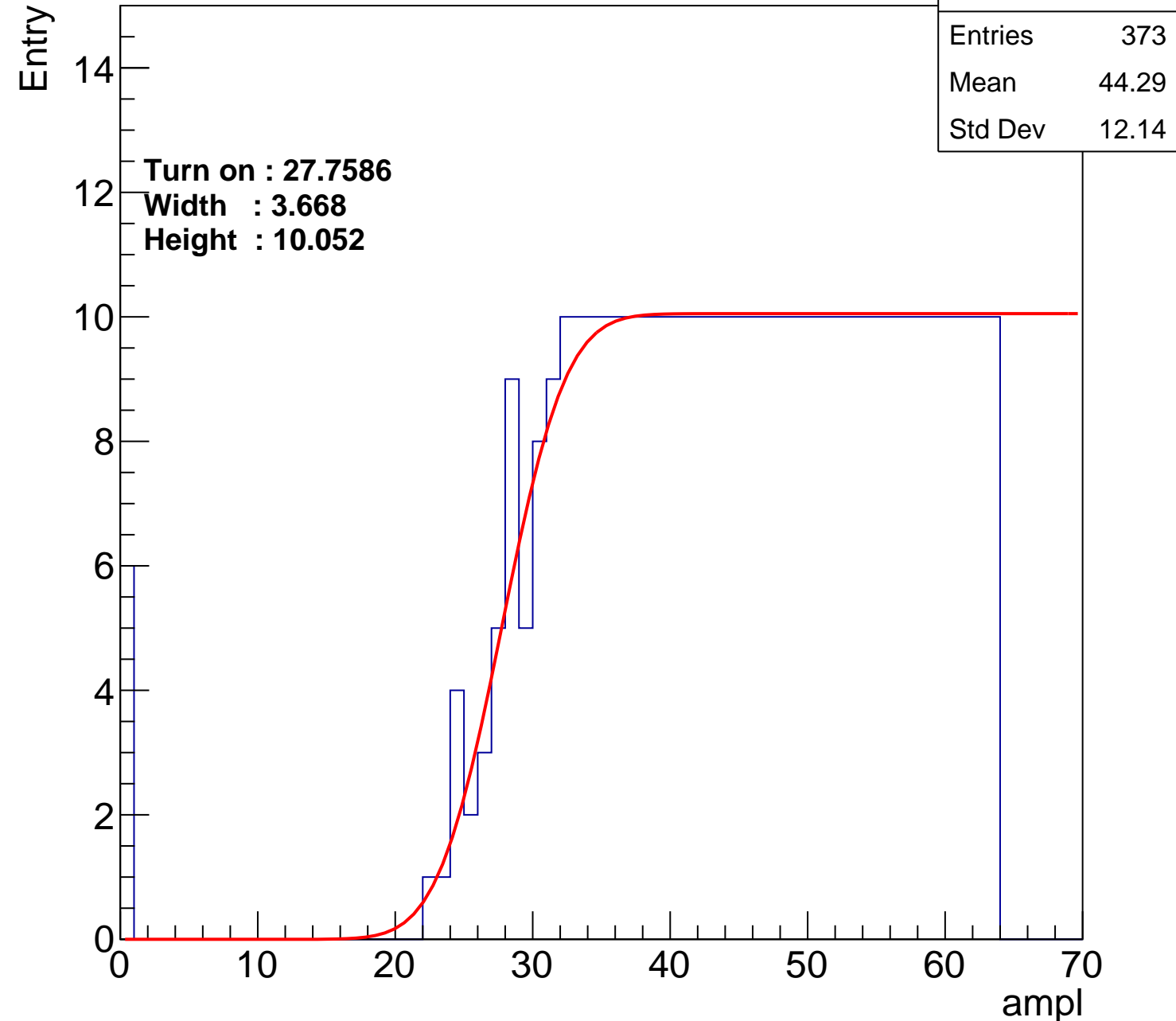
Width : 3.668

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch5

calib_packv5_042523_0143.root, FC#0, port D2

Entries	367
Mean	44.65
Std Dev	11.83

Turn on : 27.7943

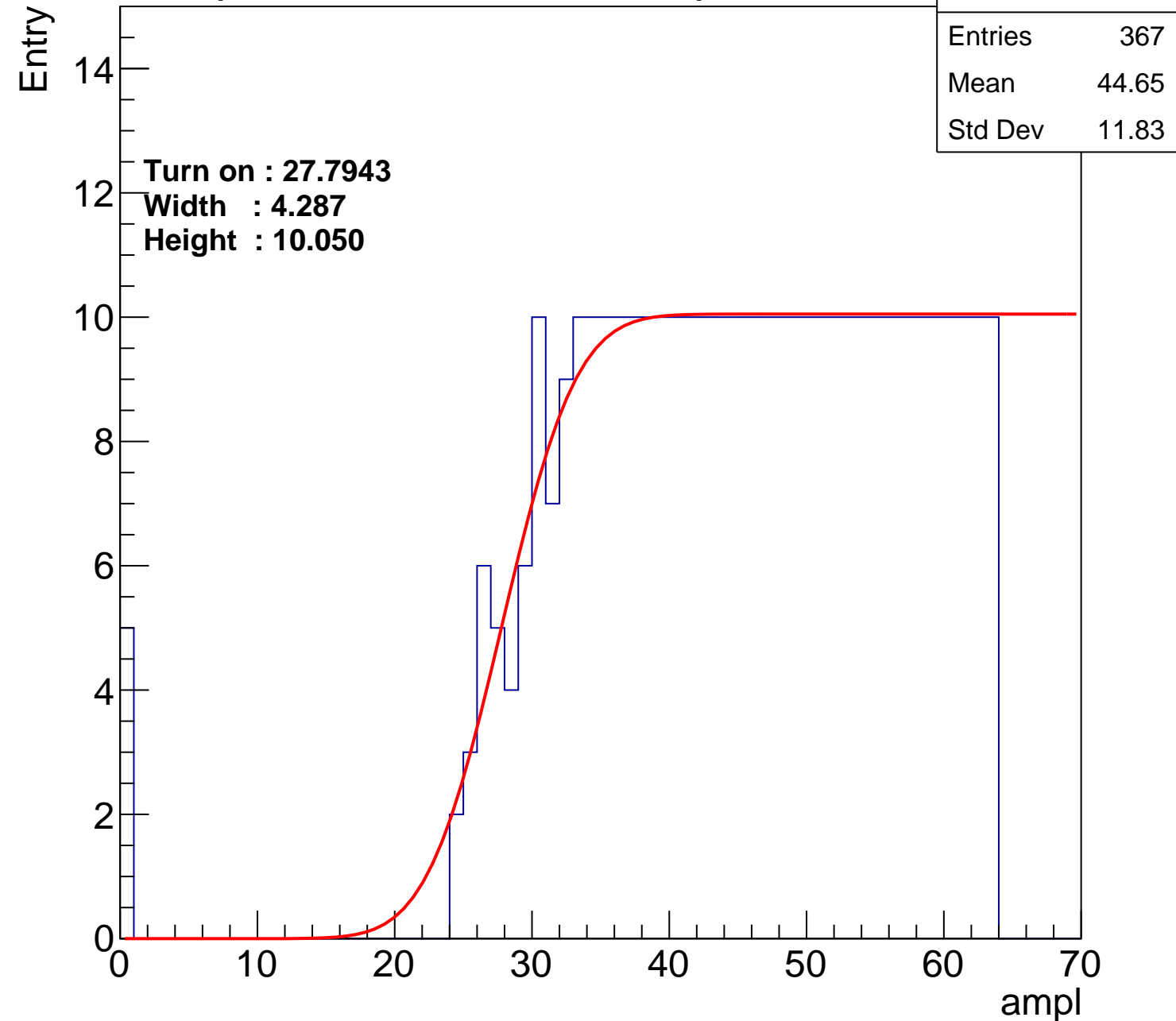
Width : 4.287

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch6

calib_packv5_042523_0143.root, FC#0, port D2

Entries	397
Mean	43.34
Std Dev	12.21

Turn on : 24.5345

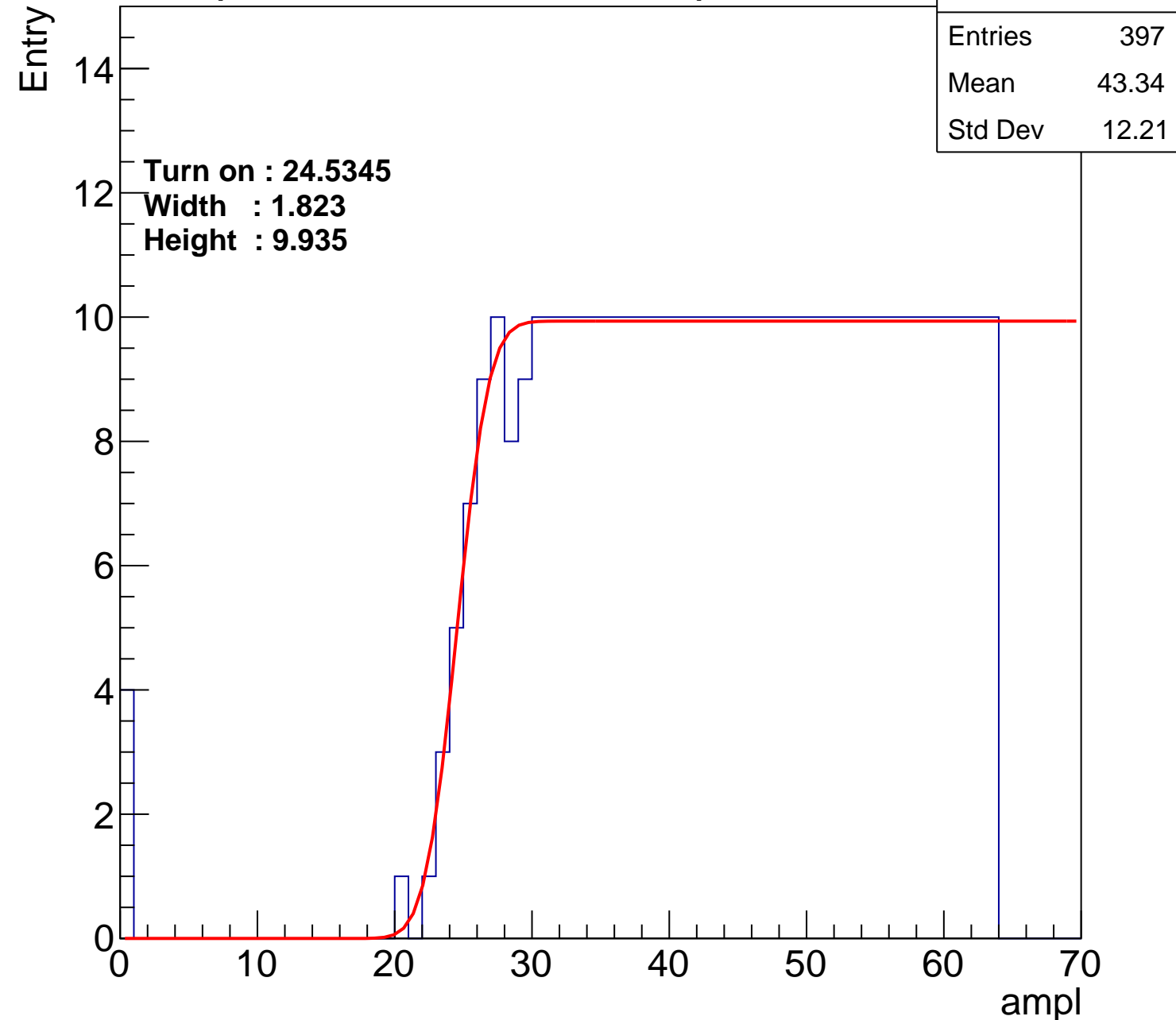
Width : 1.823

Height : 9.935

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch7

calib_packv5_042523_0143.root, FC#0, port D2

Entries	371
Mean	44.65
Std Dev	11.45

Turn on : 27.0659

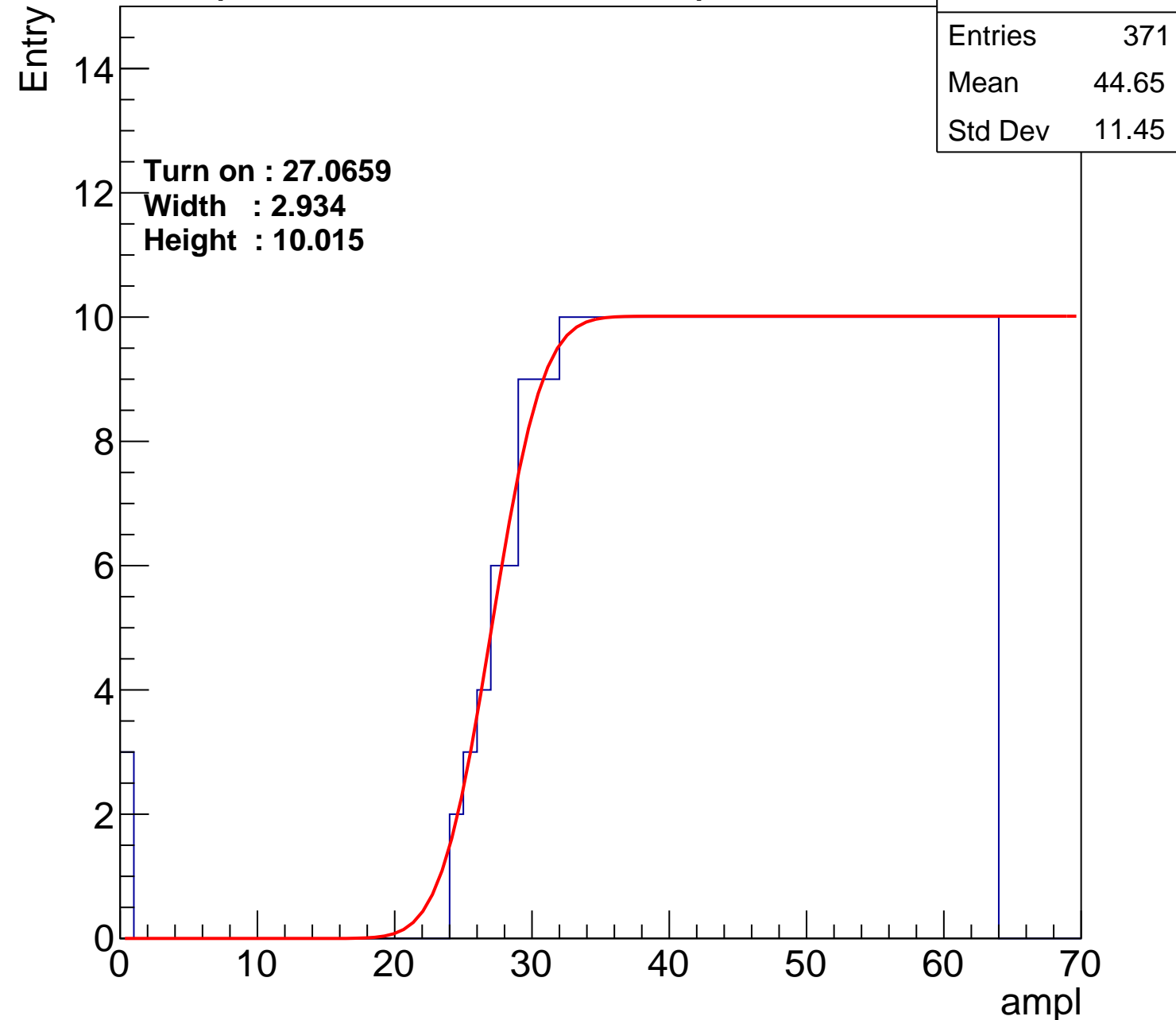
Width : 2.934

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch8

calib_packv5_042523_0143.root, FC#0, port D2

Entries	379
Mean	44.26
Std Dev	11.65

Turn on : 26.5909

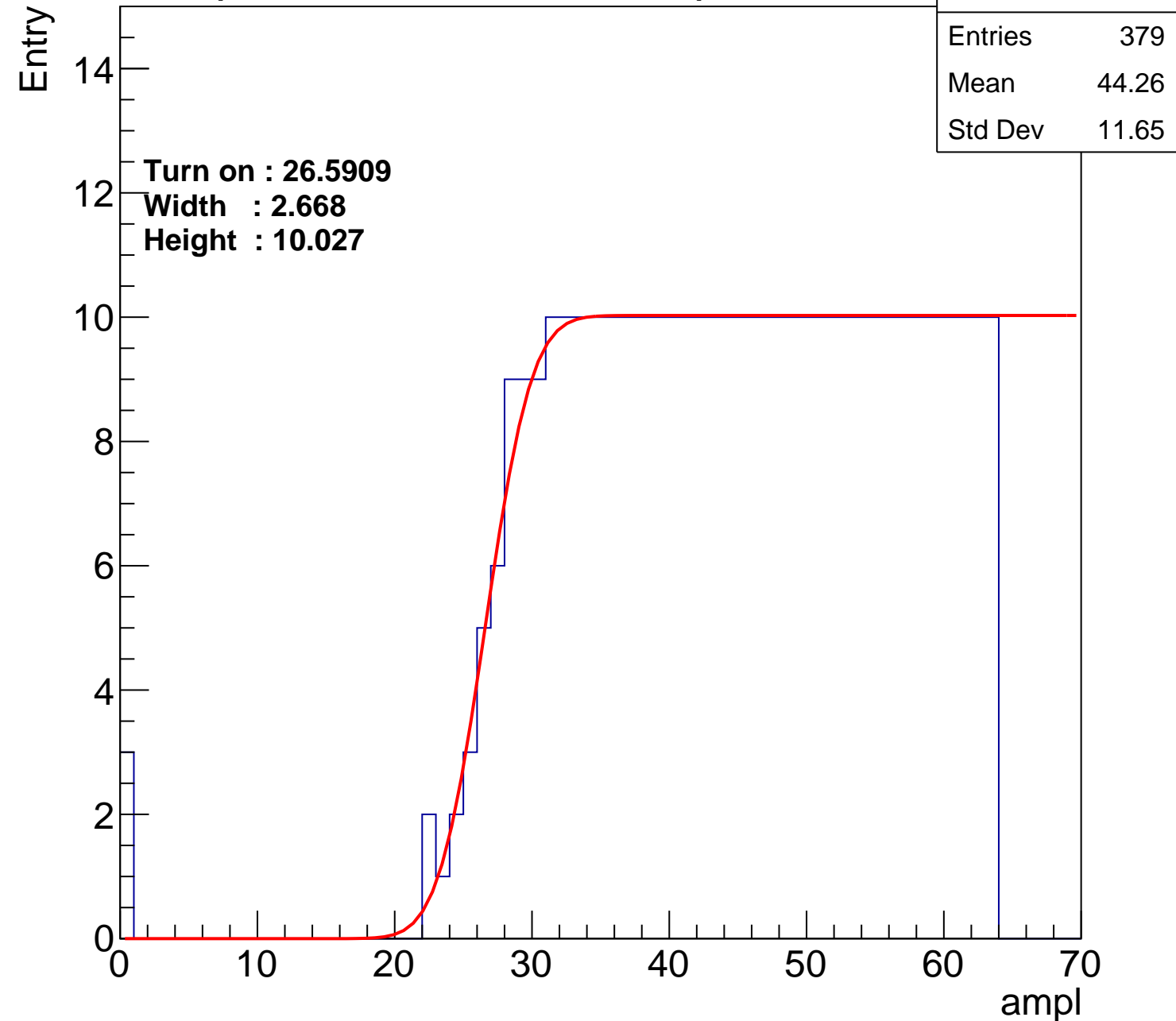
Width : 2.668

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch9

calib_packv5_042523_0143.root, FC#0, port D2

Entries	360
Mean	45.09
Std Dev	11.44

Turn on : 28.5892

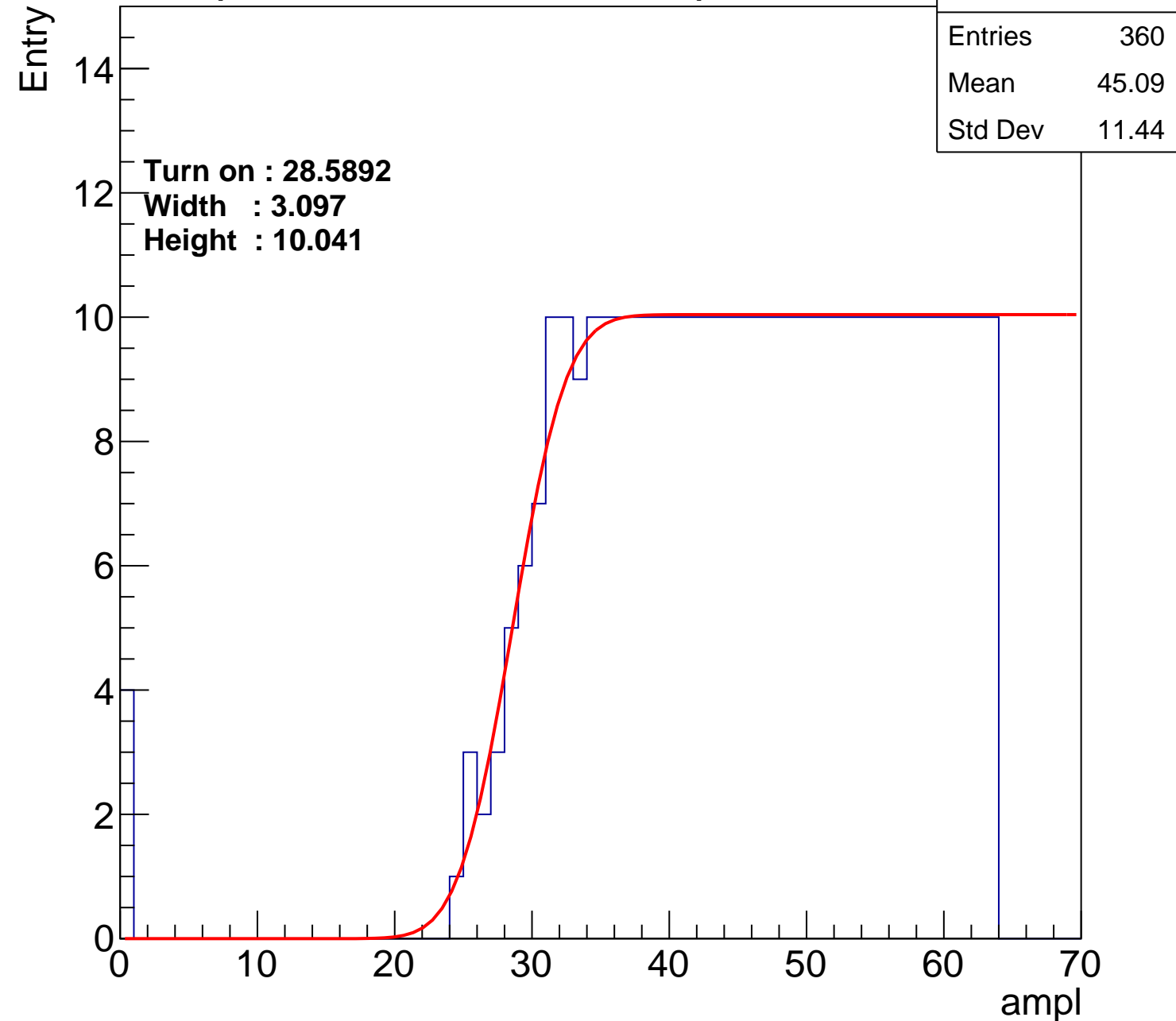
Width : 3.097

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch10

calib_packv5_042523_0143.root, FC#0, port D2

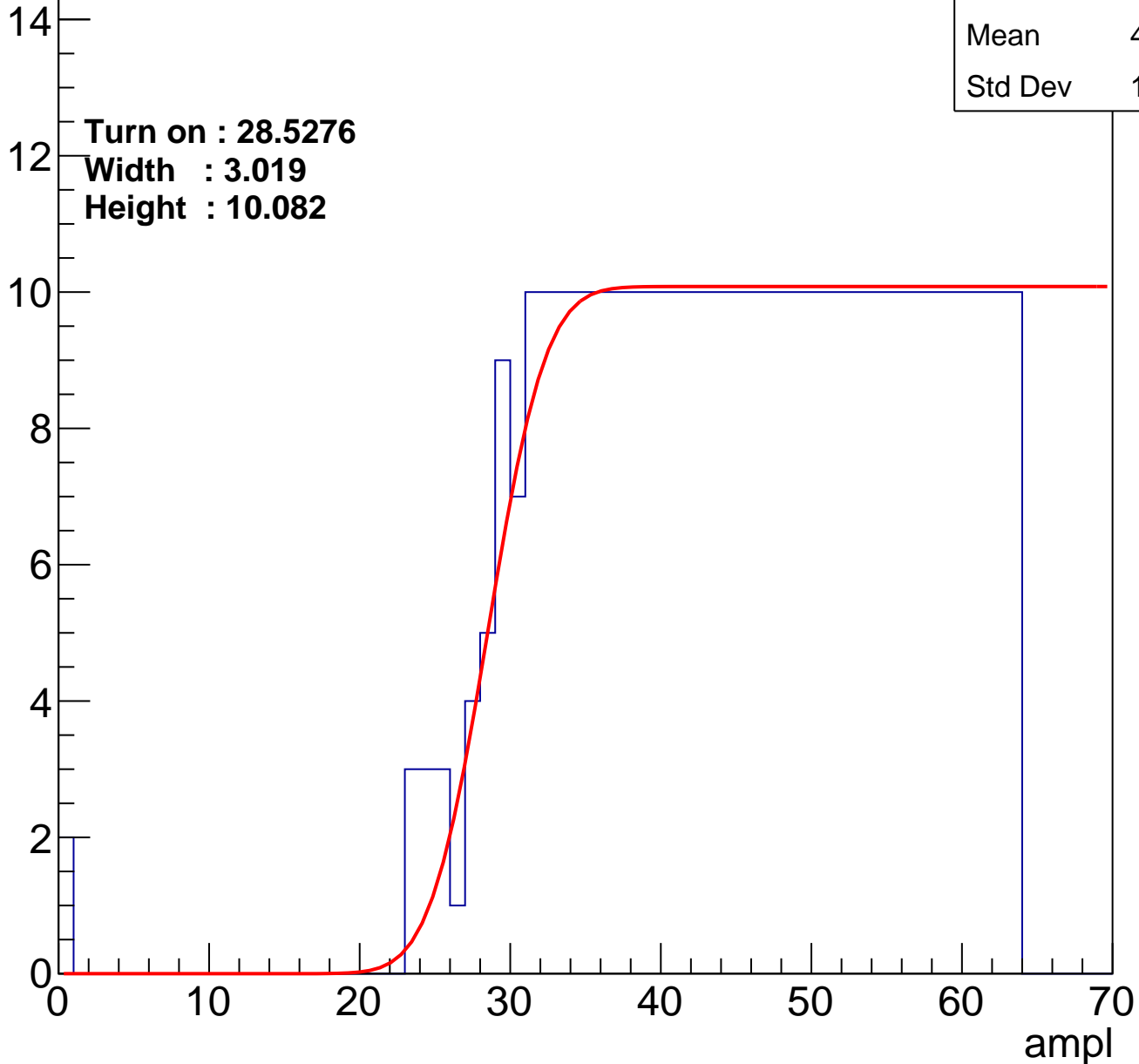
Entries	367
Mean	44.88
Std Dev	11.22

Turn on : 28.5276

Width : 3.019

Height : 10.082

Entry



B1L101S, U11-ch11

calib_packv5_042523_0143.root, FC#0, port D2

Entries	361
Mean	45.04
Std Dev	11.47

Turn on : 28.6238

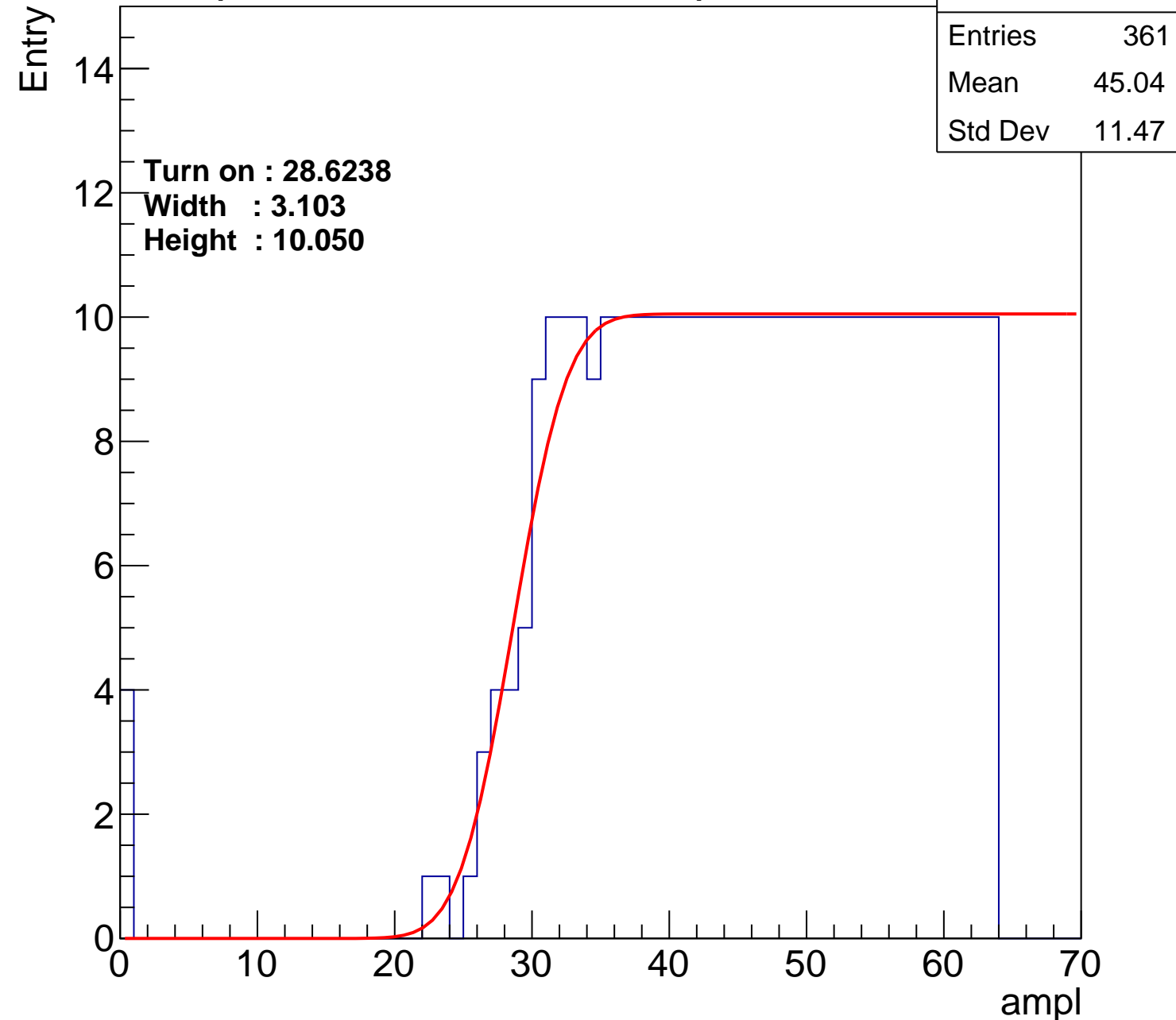
Width : 3.103

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch12

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.37
Std Dev	11.77

Turn on : 27.4731

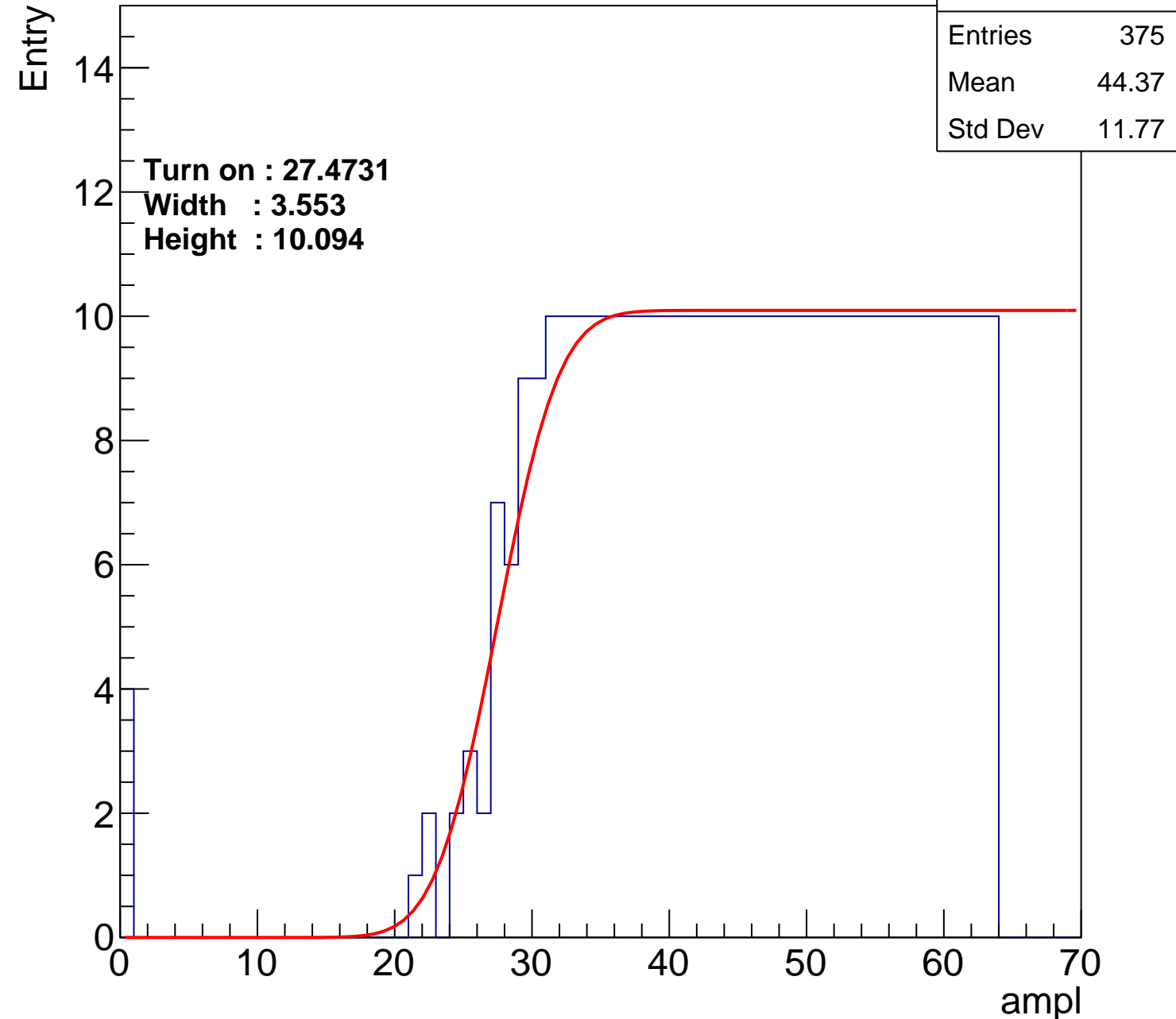
Width : 3.553

Height : 10.094

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch13

calib_packv5_042523_0143.root, FC#0, port D2

Entries	359
Mean	45.38
Std Dev	10.75

Turn on : 28.2046

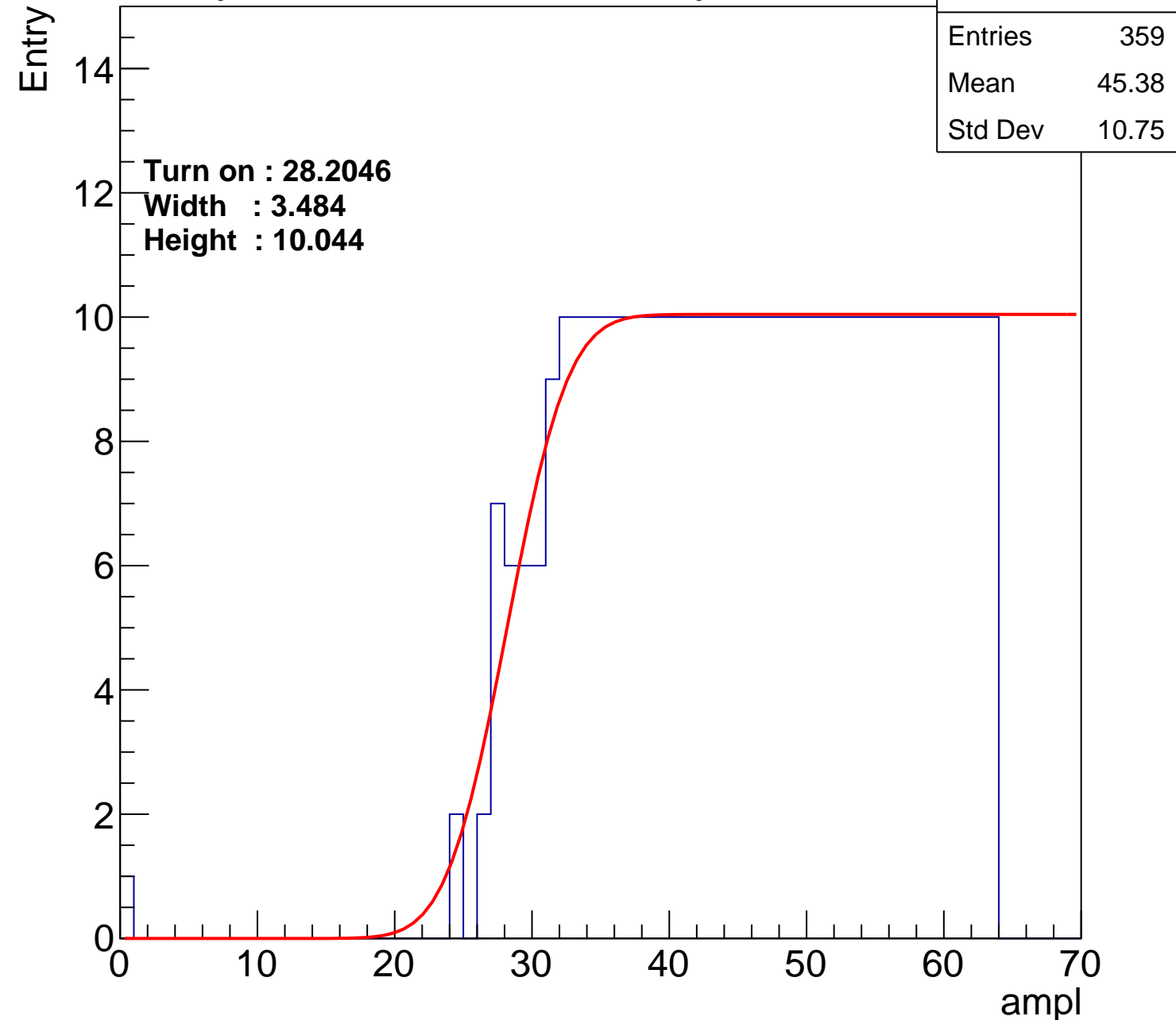
Width : 3.484

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch14

calib_packv5_042523_0143.root, FC#0, port D2

Entries	367
Mean	44.65
Std Dev	11.83

Turn on : 28.3200

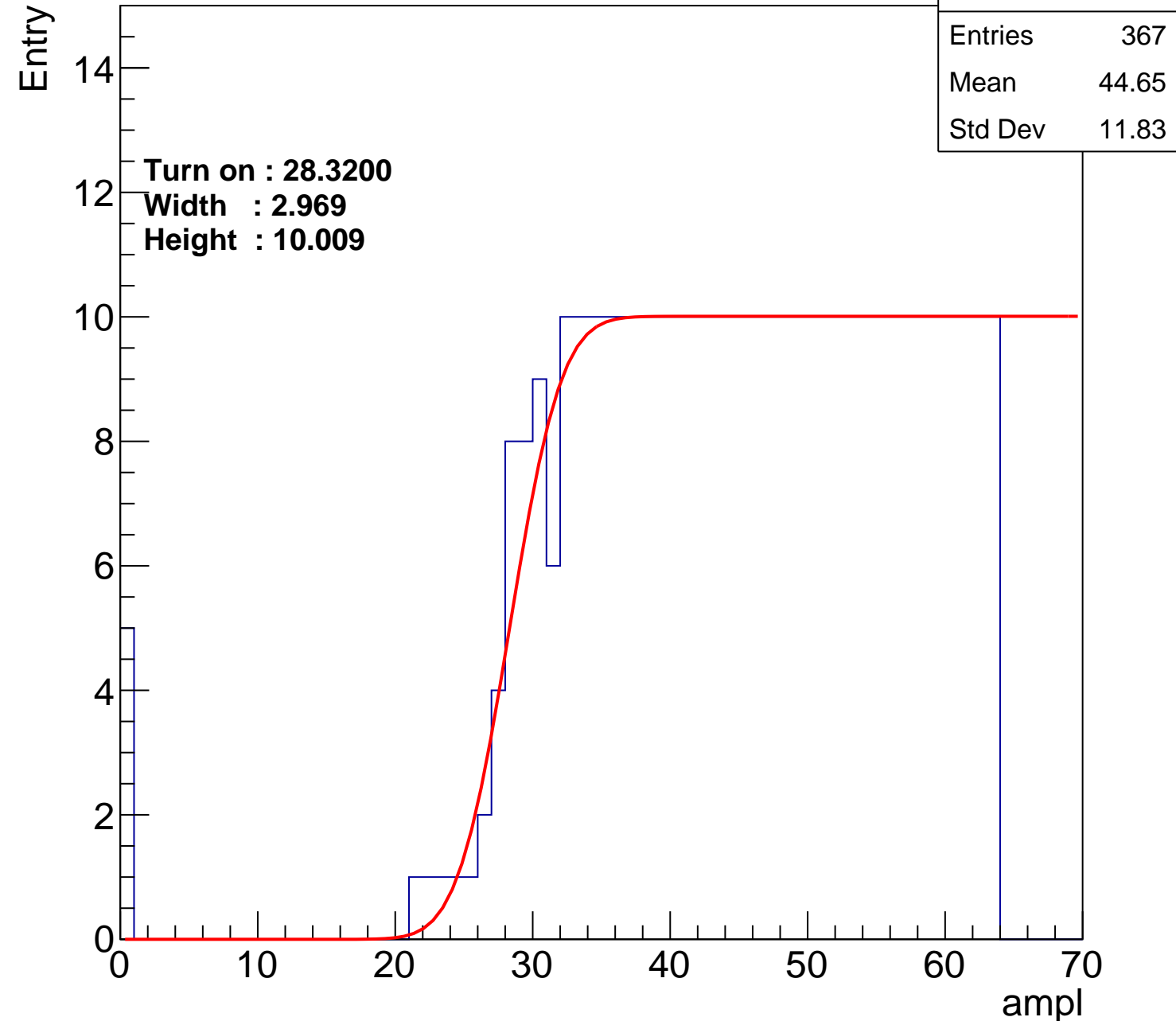
Width : 2.969

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch15

calib_packv5_042523_0143.root, FC#0, port D2

Entries	355
Mean	45.41
Std Dev	11.12

Turn on : 29.1330

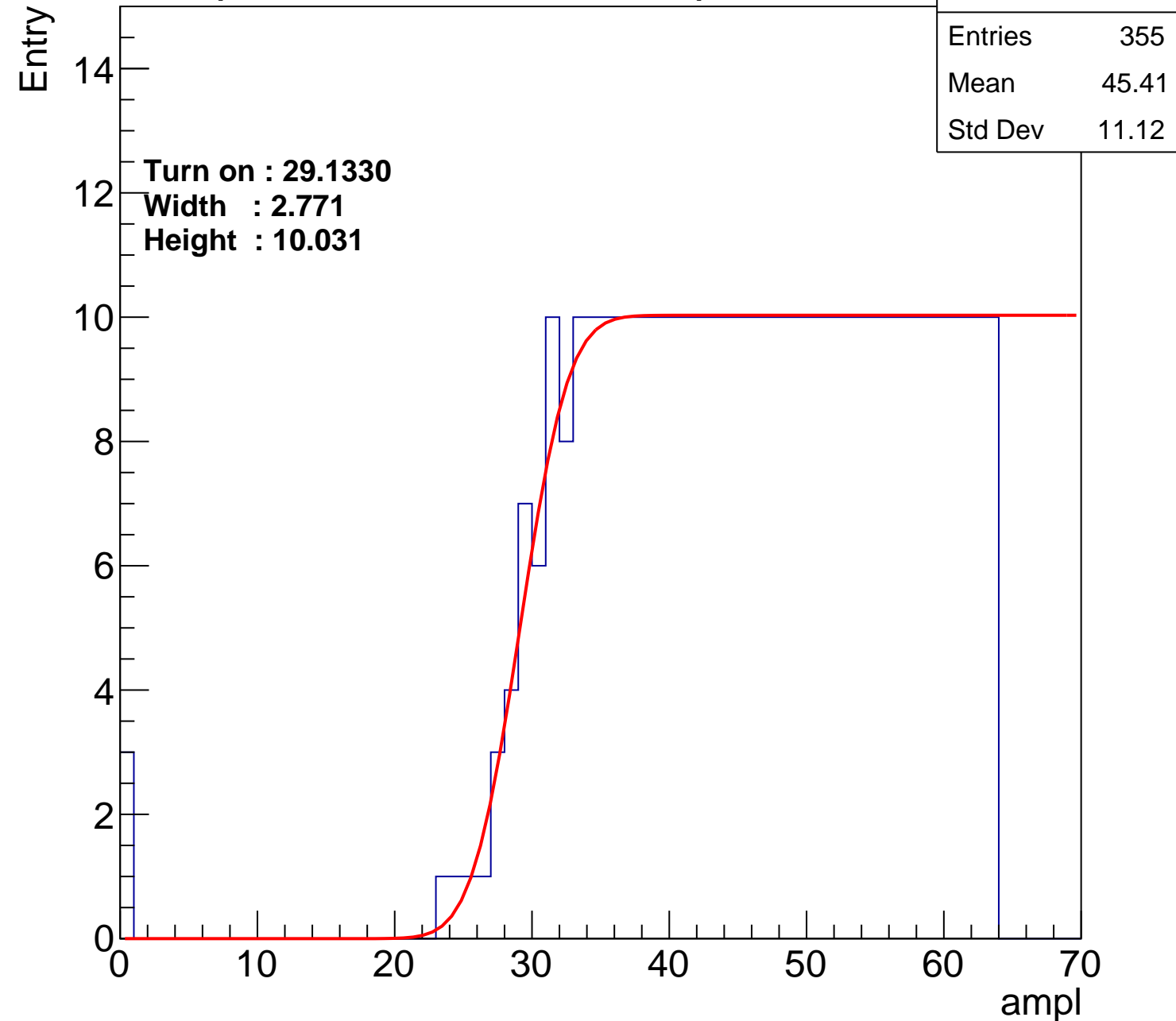
Width : 2.771

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch16

calib_packv5_042523_0143.root, FC#0, port D2

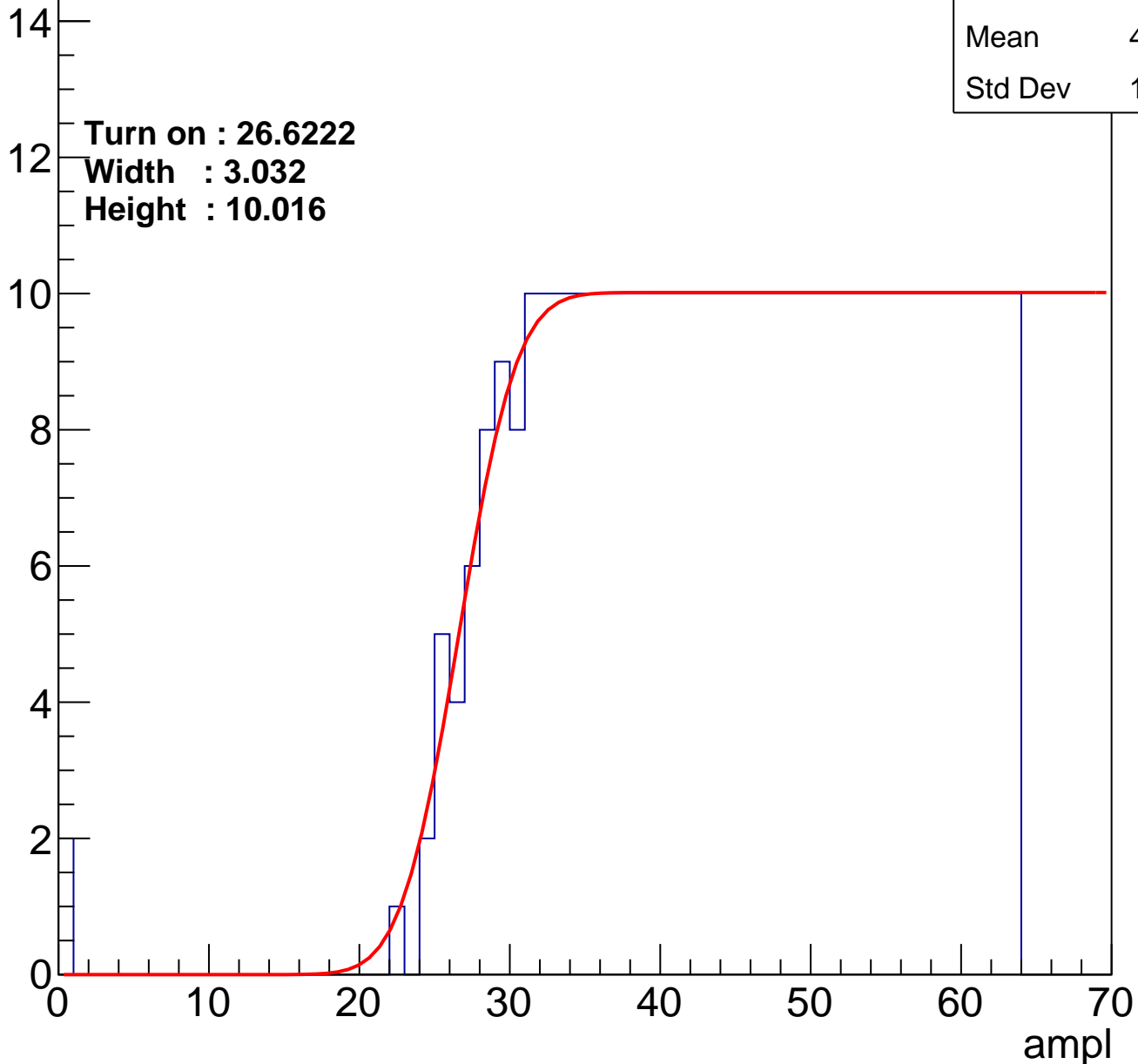
Entries	375
Mean	44.52
Std Dev	11.36

Turn on : 26.6222

Width : 3.032

Height : 10.016

Entry



B1L101S, U11-ch17

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.61
Std Dev	11.14

Turn on : 26.7064

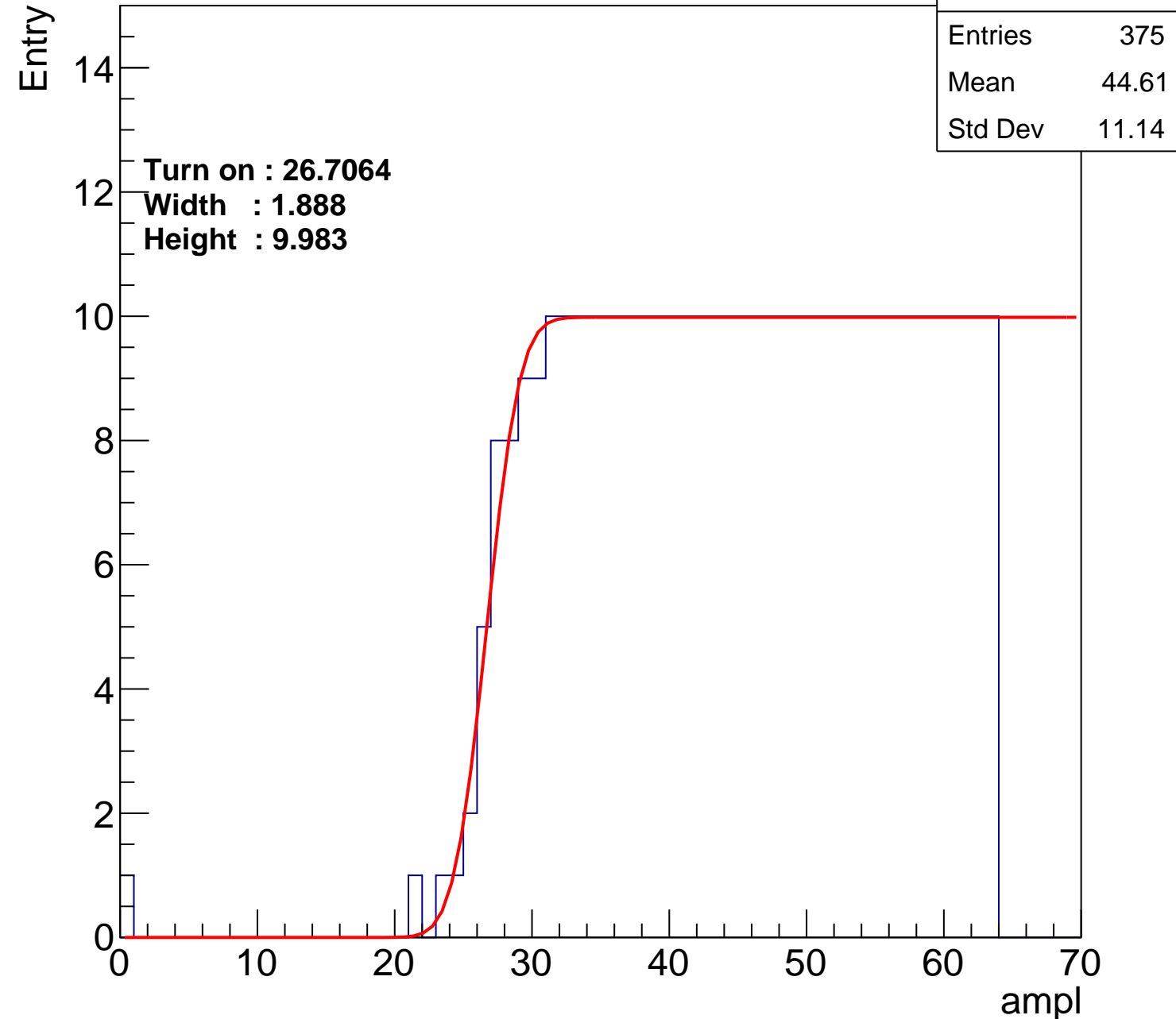
Width : 1.888

Height : 9.983

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch18

calib_packv5_042523_0143.root, FC#0, port D2

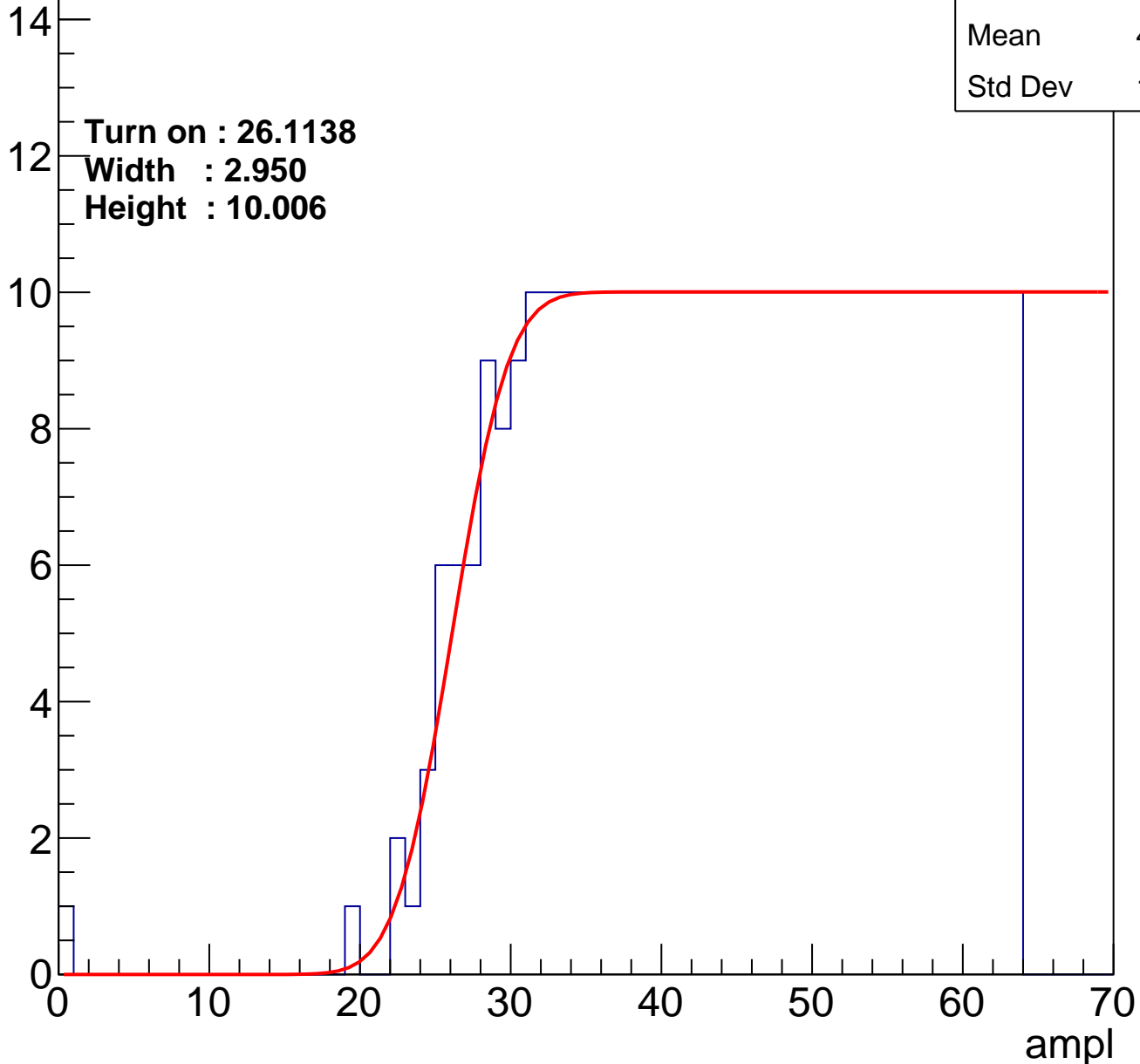
Entries	382
Mean	44.21
Std Dev	11.41

Turn on : 26.1138

Width : 2.950

Height : 10.006

Entry



B1L101S, U11-ch19

calib_packv5_042523_0143.root, FC#0, port D2

Entries	360
Mean	45.22
Std Dev	11.05

Turn on : 28.2841

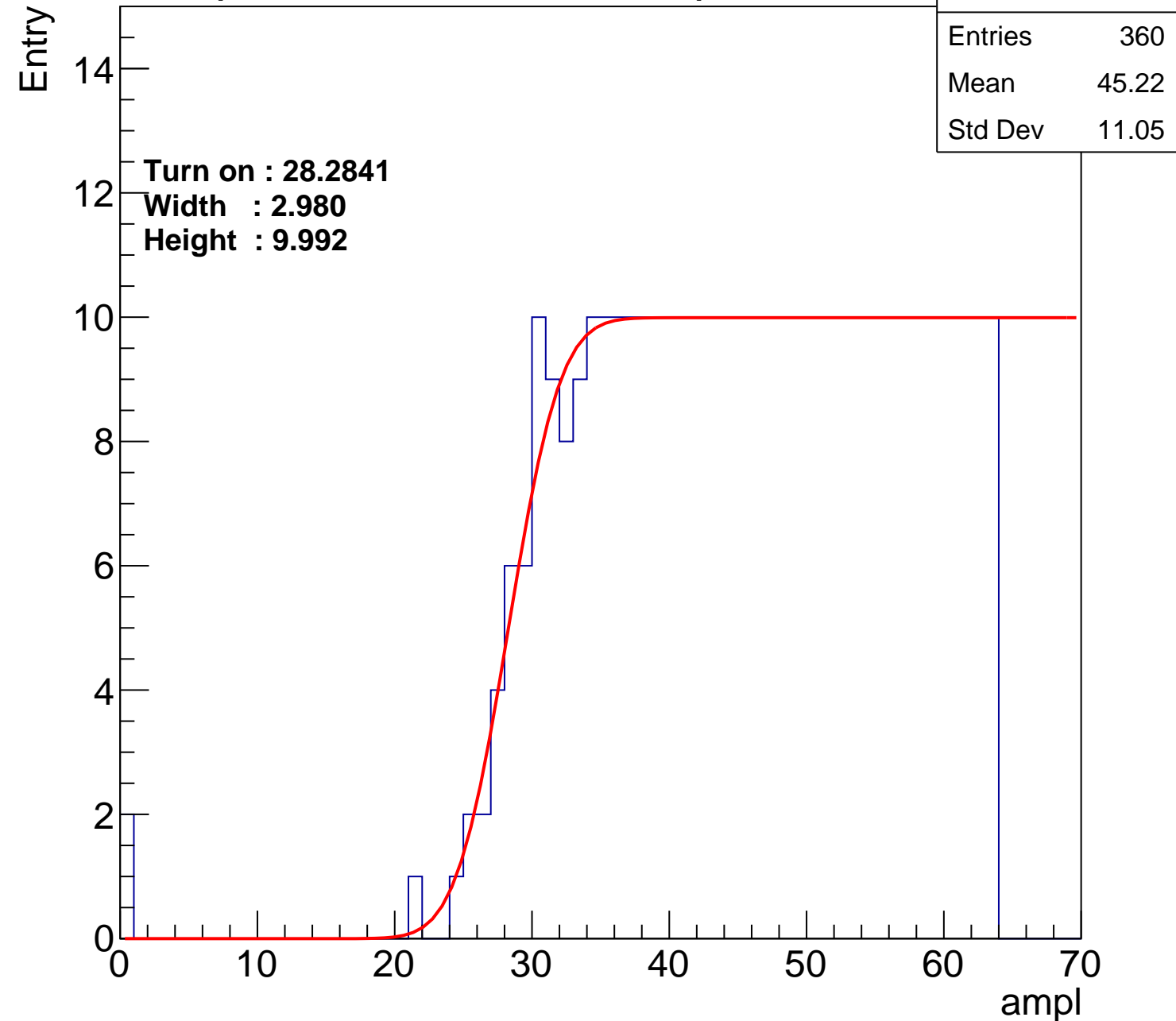
Width : 2.980

Height : 9.992

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch20

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.34
Std Dev	11.8

Turn on : 27.0833

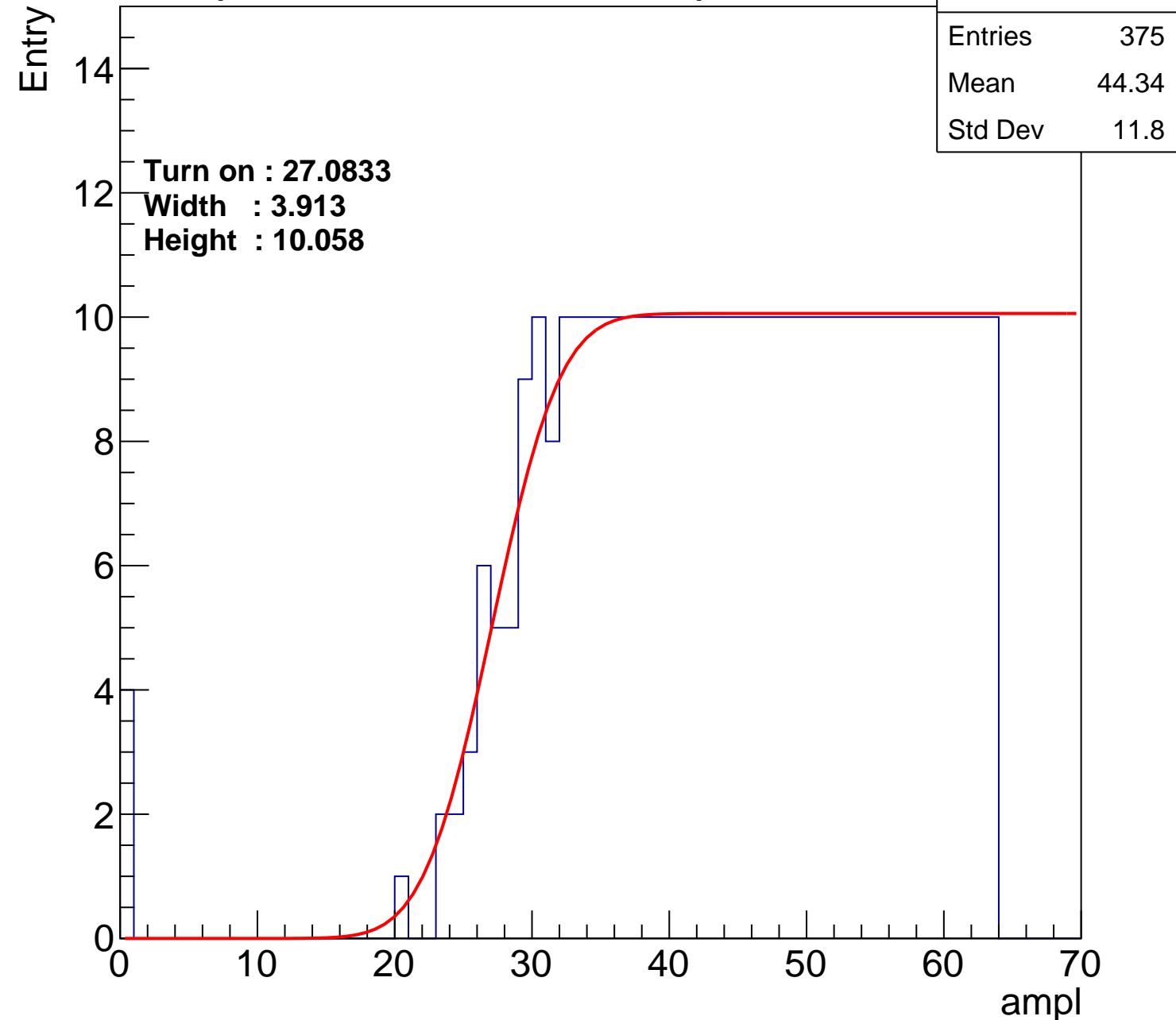
Width : 3.913

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch21

calib_packv5_042523_0143.root, FC#0, port D2

Entries	389
Mean	43.81
Std Dev	11.83

Turn on : 25.4954

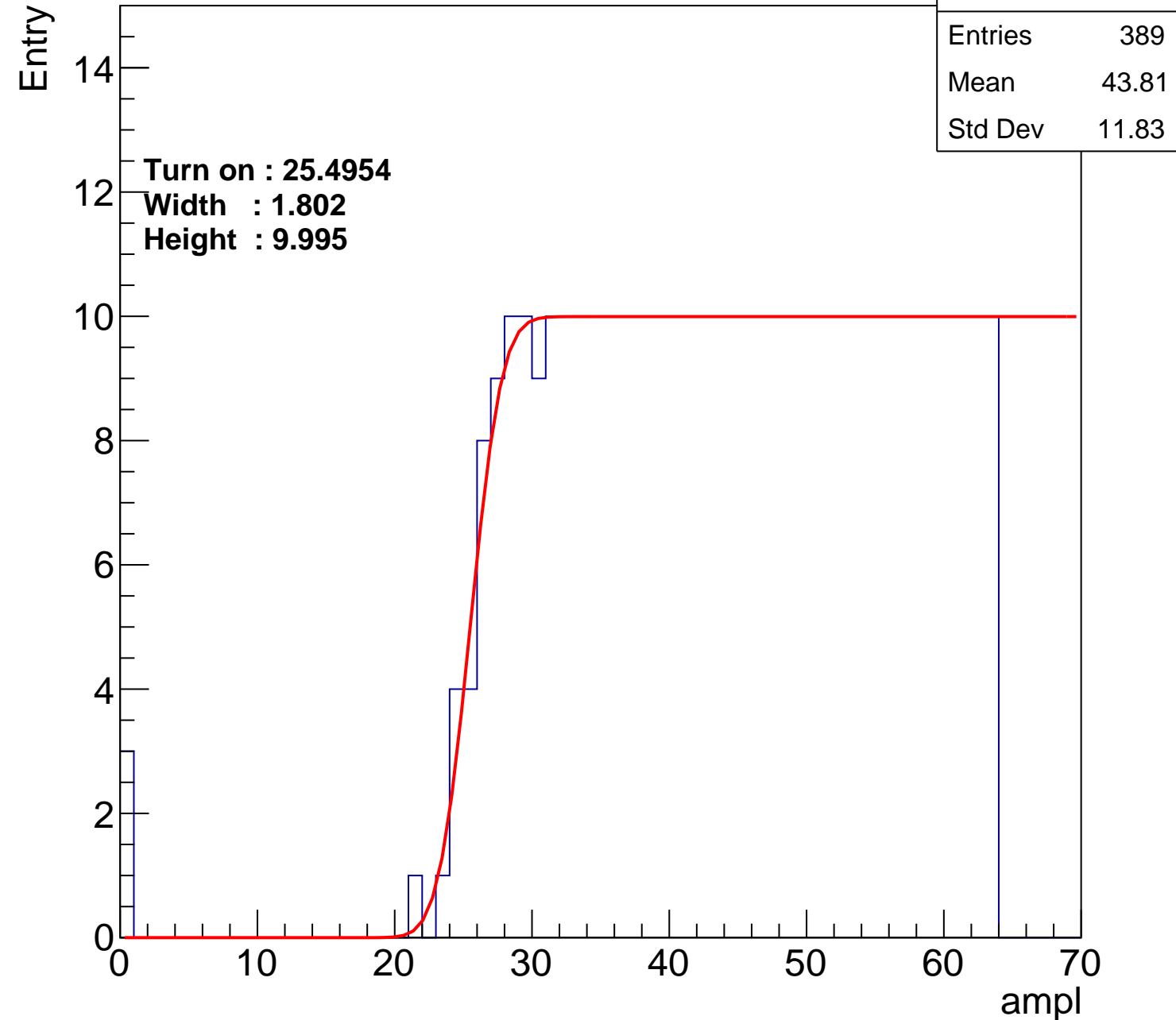
Width : 1.802

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch22

calib_packv5_042523_0143.root, FC#0, port D2

Entries	373
Mean	44.42
Std Dev	11.88

Turn on : 27.5021

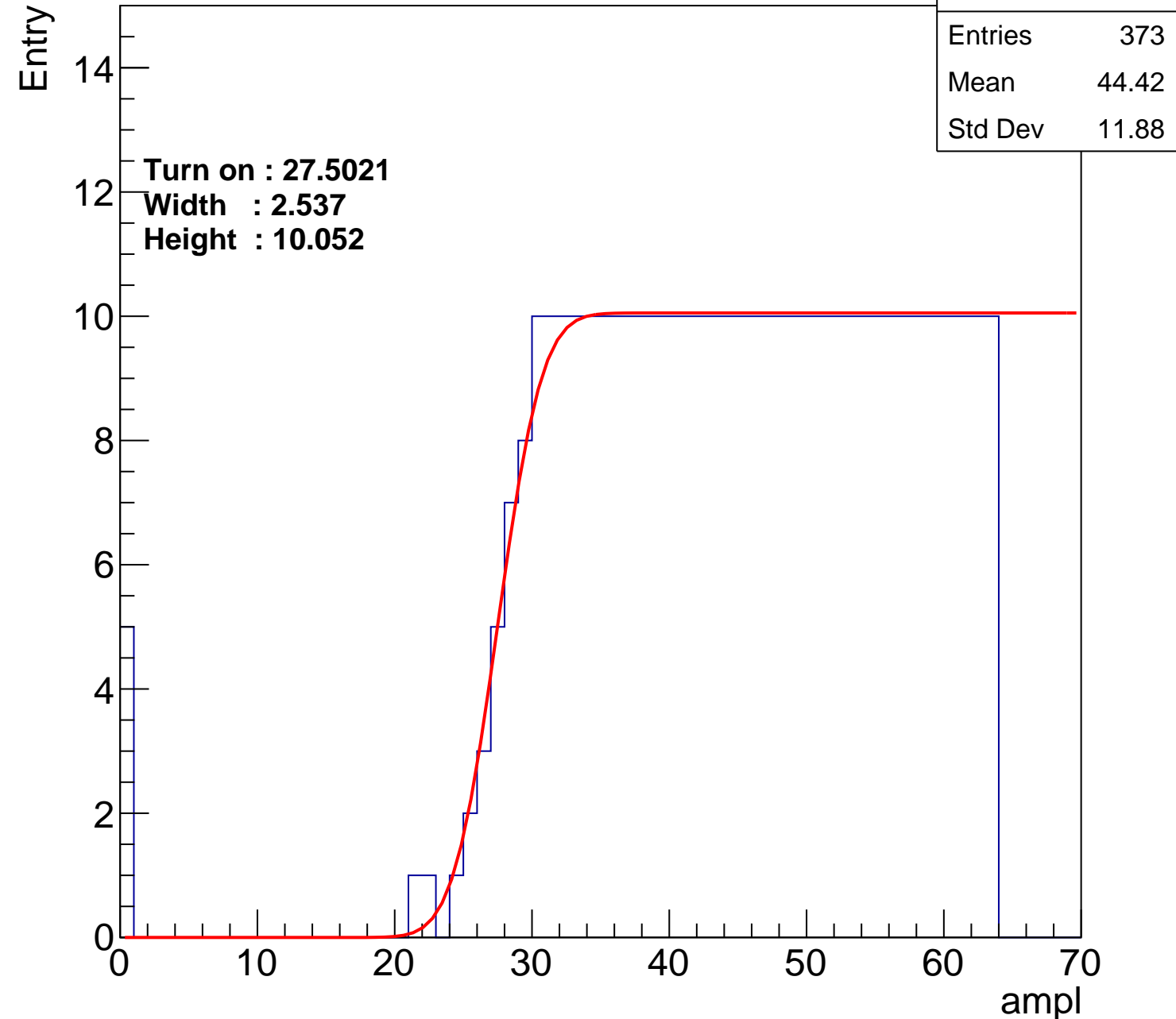
Width : 2.537

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch23

calib_packv5_042523_0143.root, FC#0, port D2

Entries	364
Mean	45.15
Std Dev	10.86

Turn on : 27.9147

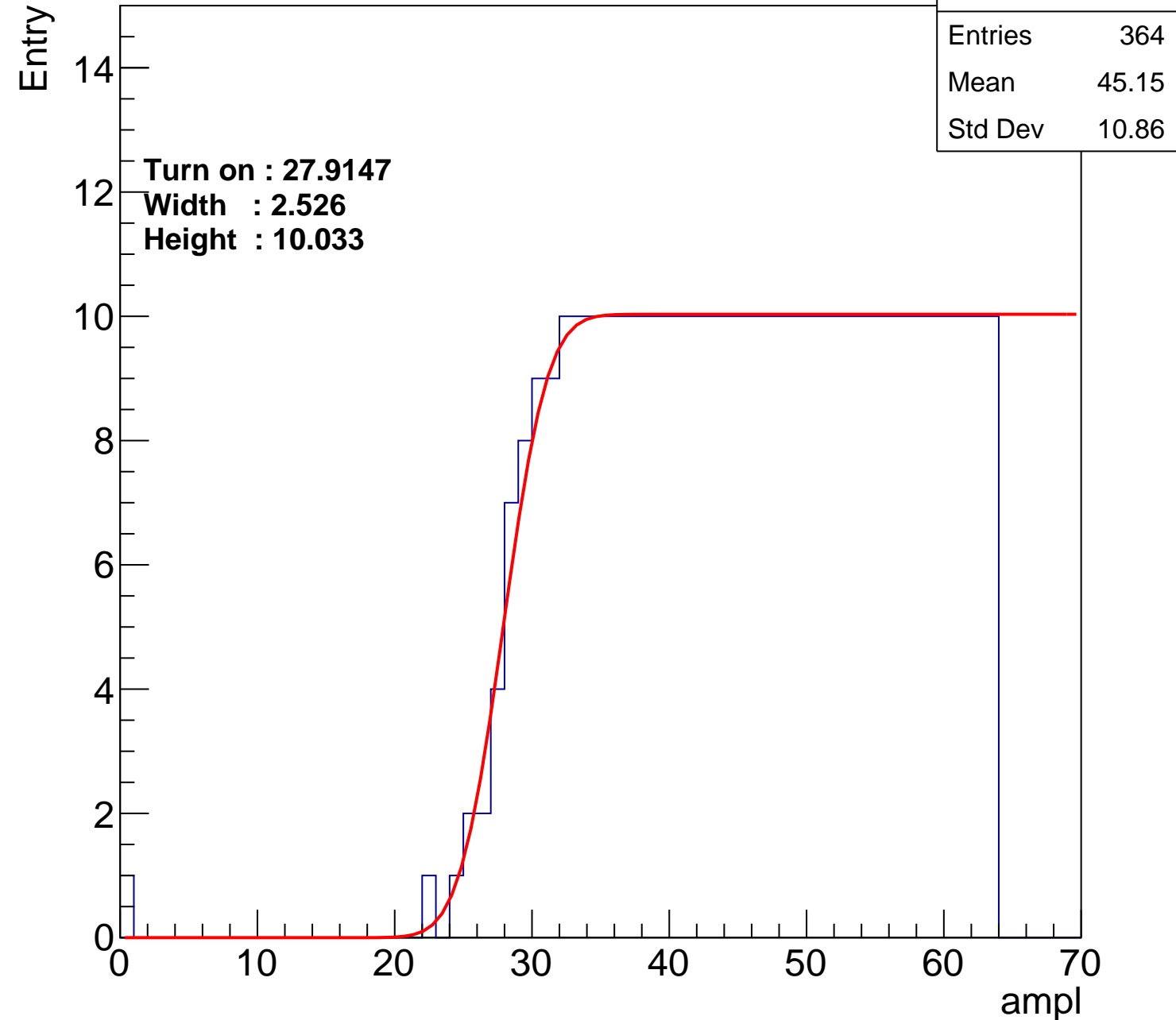
Width : 2.526

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch24

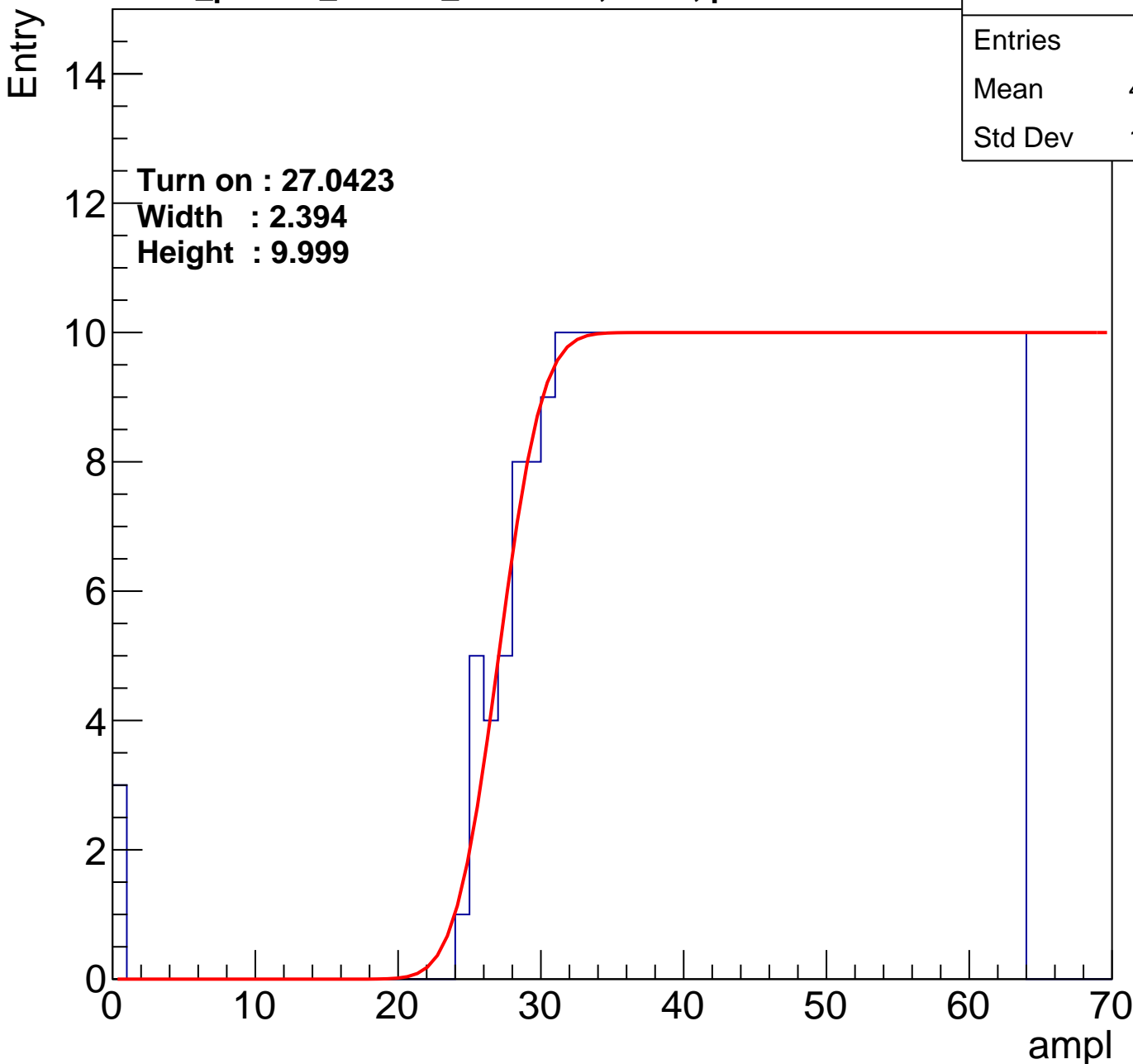
calib_packv5_042523_0143.root, FC#0, port D2

Entries	373
Mean	44.57
Std Dev	11.48

Turn on : 27.0423

Width : 2.394

Height : 9.999



B1L101S, U11-ch25

calib_packv5_042523_0143.root, FC#0, port D2

Entries	381
Mean	44.15
Std Dev	11.72

Turn on : 26.4434

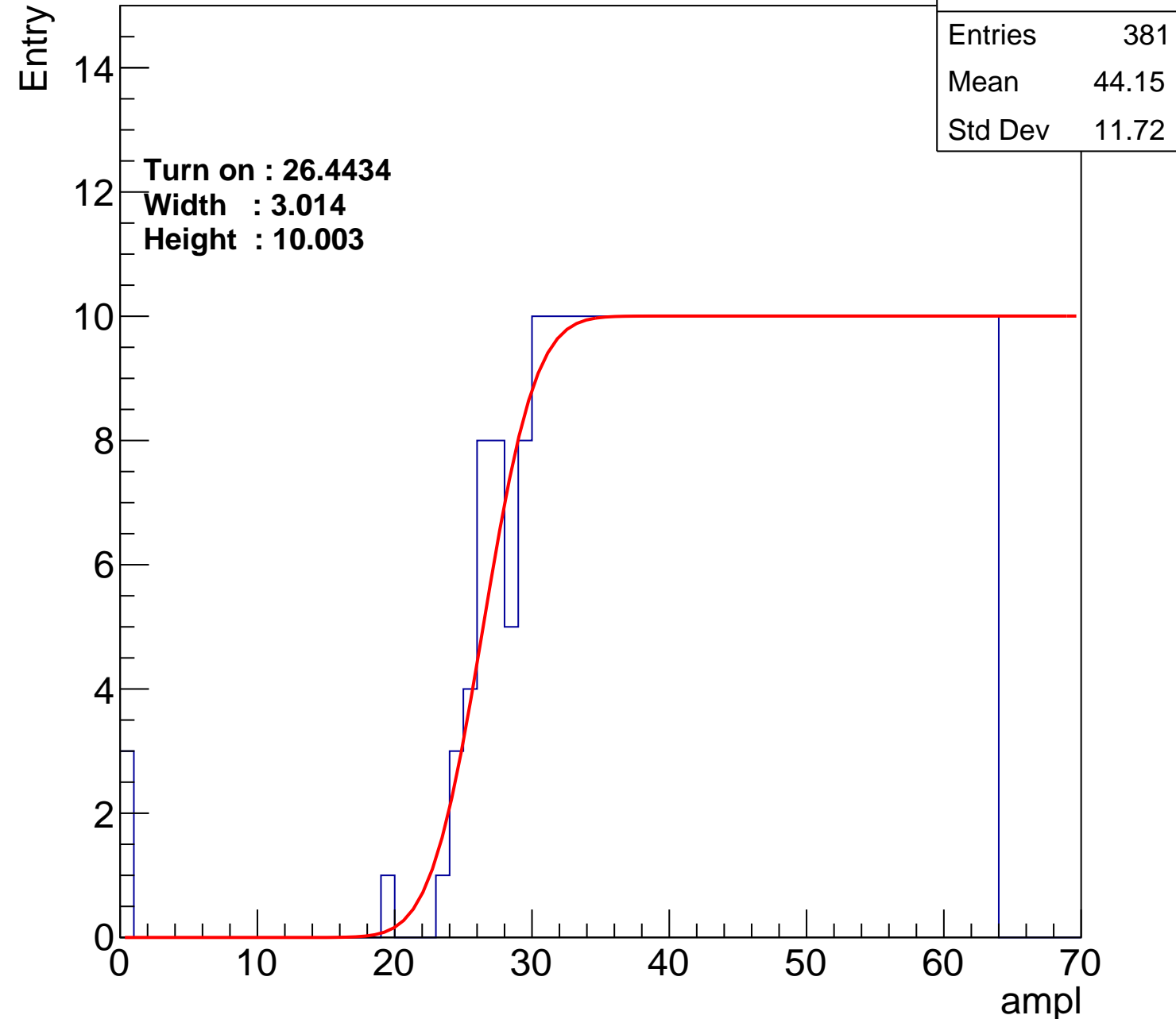
Width : 3.014

Height : 10.003

Entry

14
12
10
8
6
4
2
0

ampl



calib_packv5_042523_0143.root, FC#0, port D2

calib_packv5_042523_0143.root, FC#0, port D2

Turn on : 27.6999
Width : 3.831
Height : 10.033



B1L101S, U11-ch27

calib_packv5_042523_0143.root, FC#0, port D2

Entries	360
Mean	45.03
Std Dev	11.62

Turn on : 28.6824

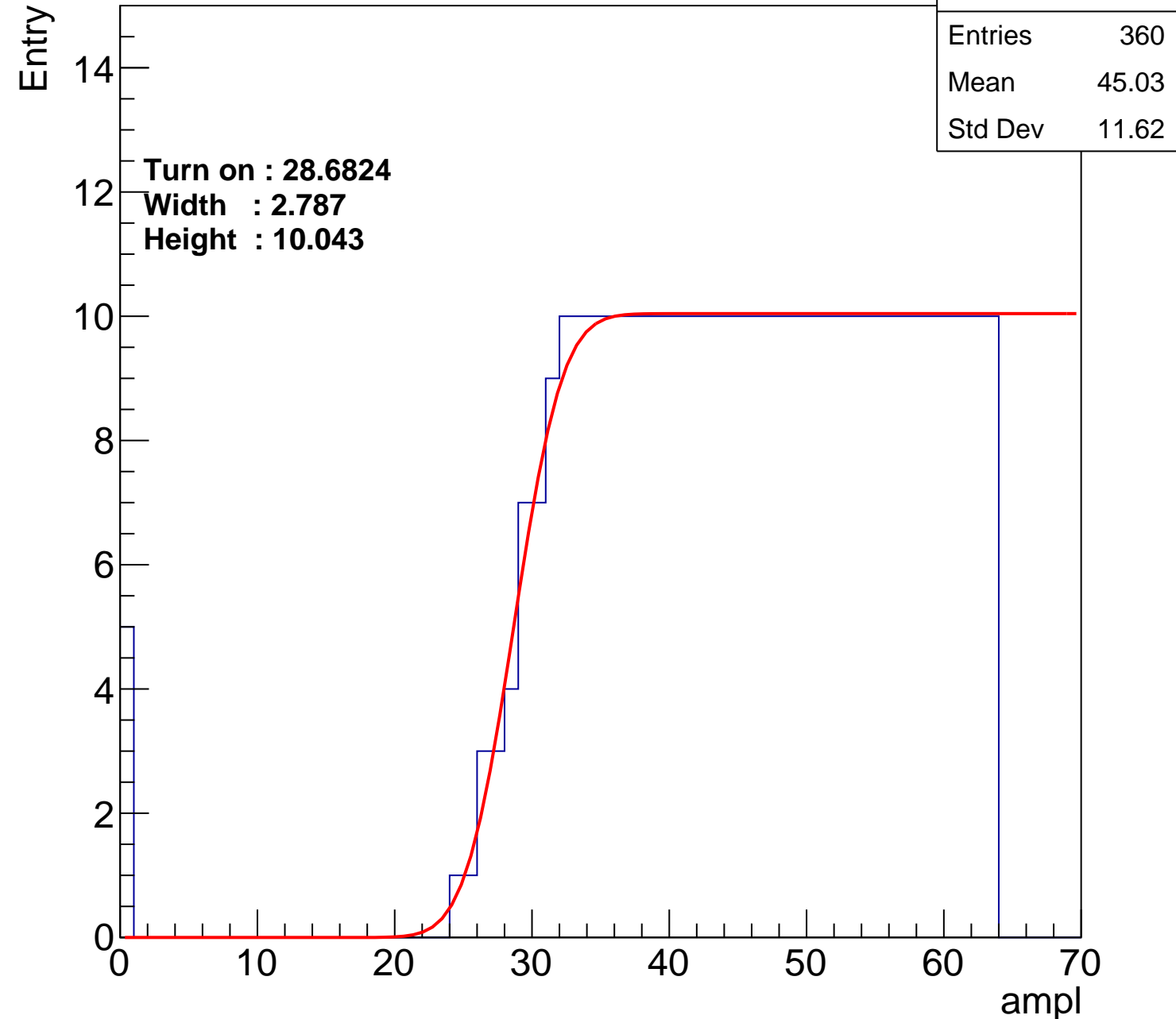
Width : 2.787

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



calib_packv5_042523_0143.root, FC#0, port D2

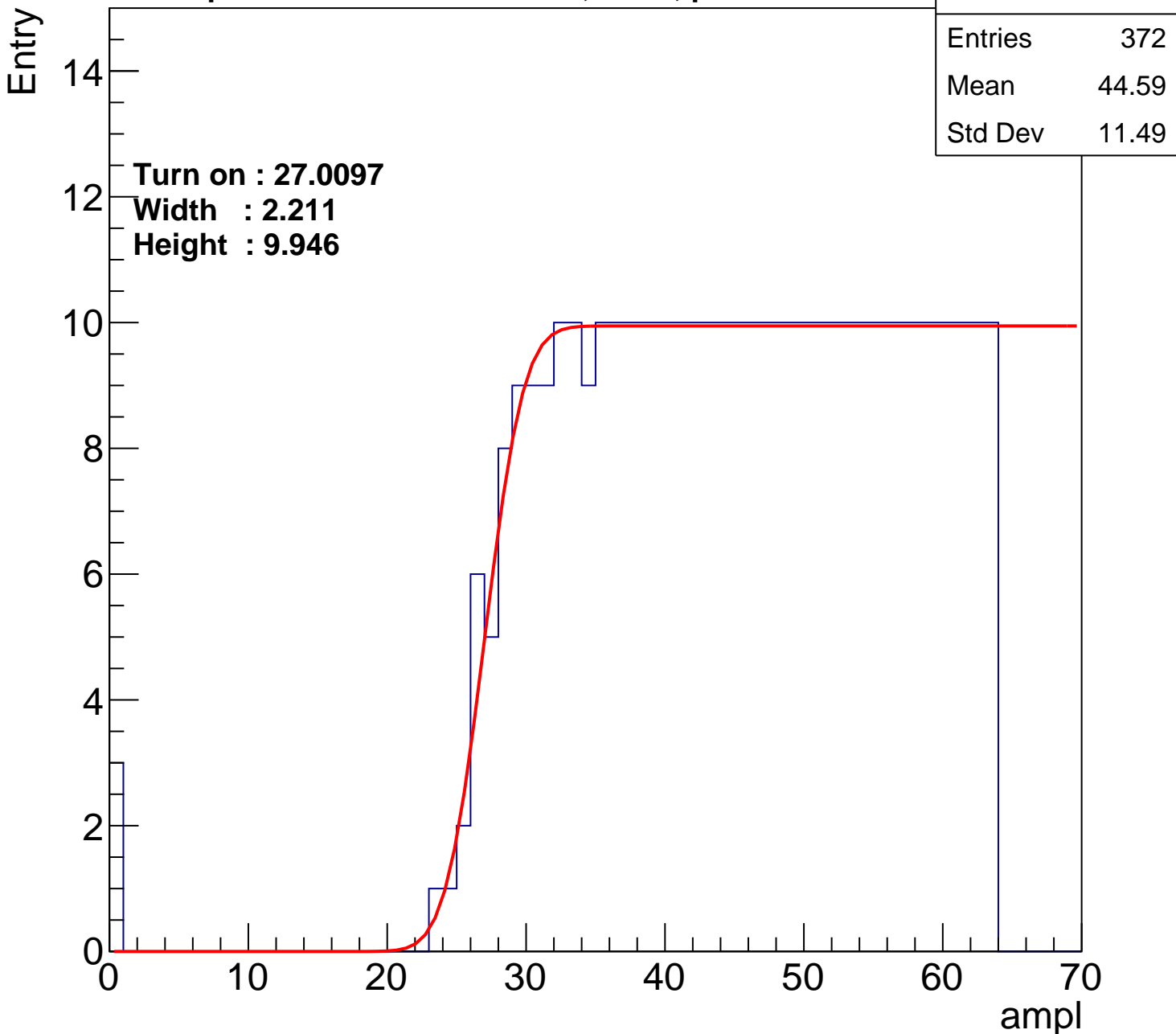
Entries	372
Mean	44.59
Std Dev	11.49

Mean	44.59
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Std Dev	11.49
---------	-------

Width : 2.211

Height : 9.946



B1L101S, U11-ch29

calib_packv5_042523_0143.root, FC#0, port D2

Entries	350
Mean	45.75
Std Dev	10.74

Turn on : 28.6474

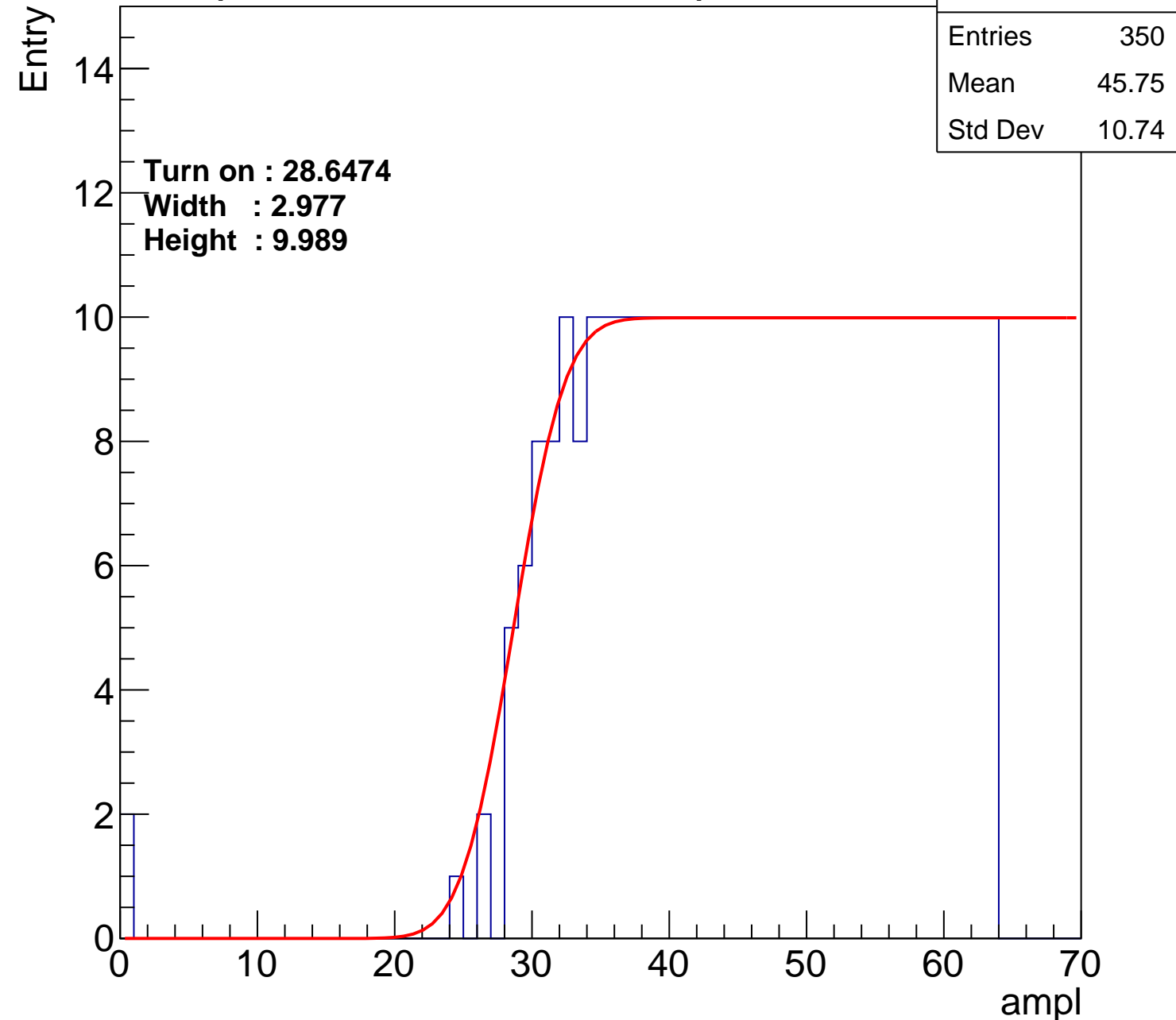
Width : 2.977

Height : 9.989

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch30

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.44
Std Dev	11.39

Turn on : 27.2053

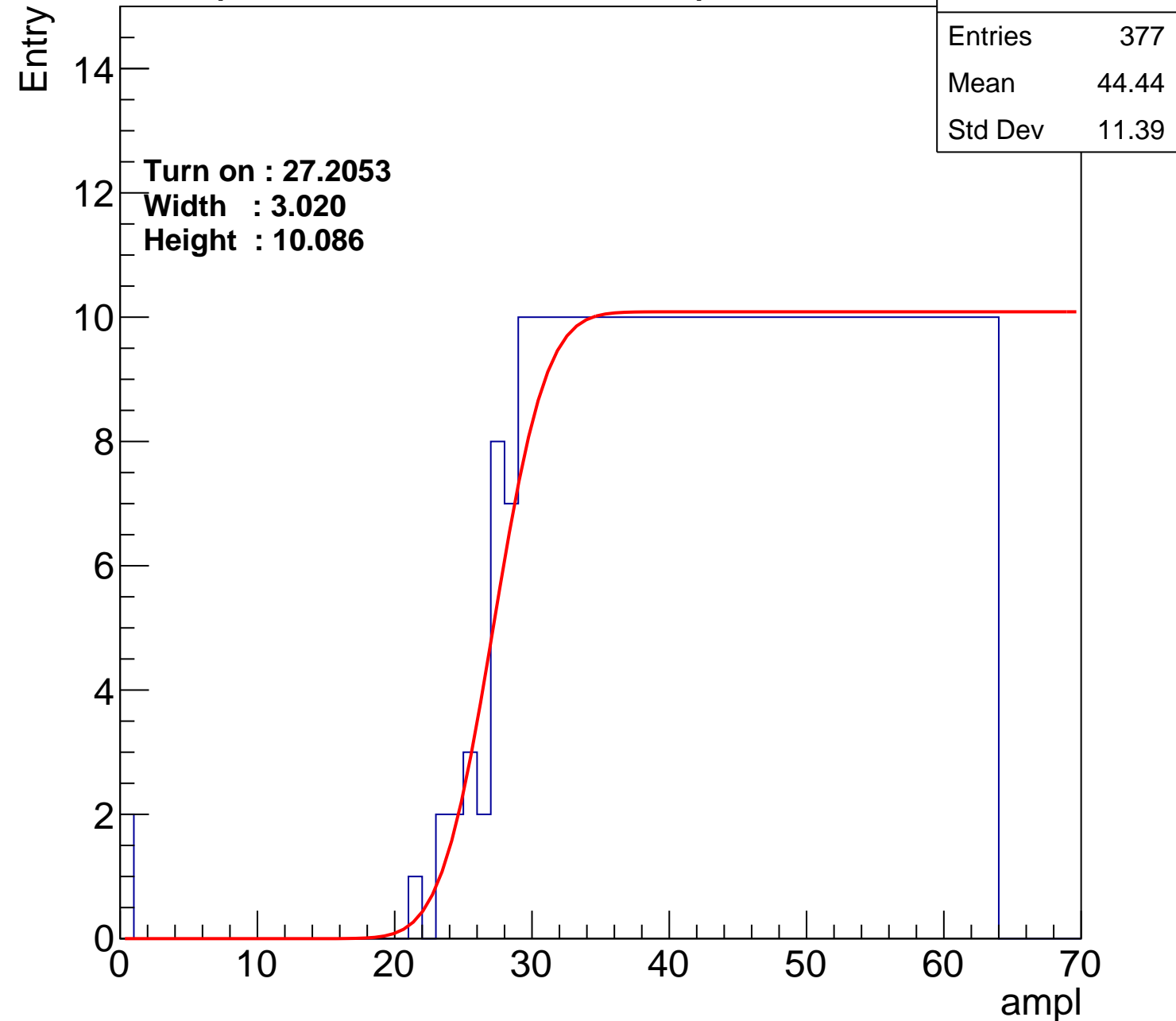
Width : 3.020

Height : 10.086

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch31

calib_packv5_042523_0143.root, FC#0, port D2

Entries	362
Mean	45.09
Std Dev	11.24

Turn on : 28.5867

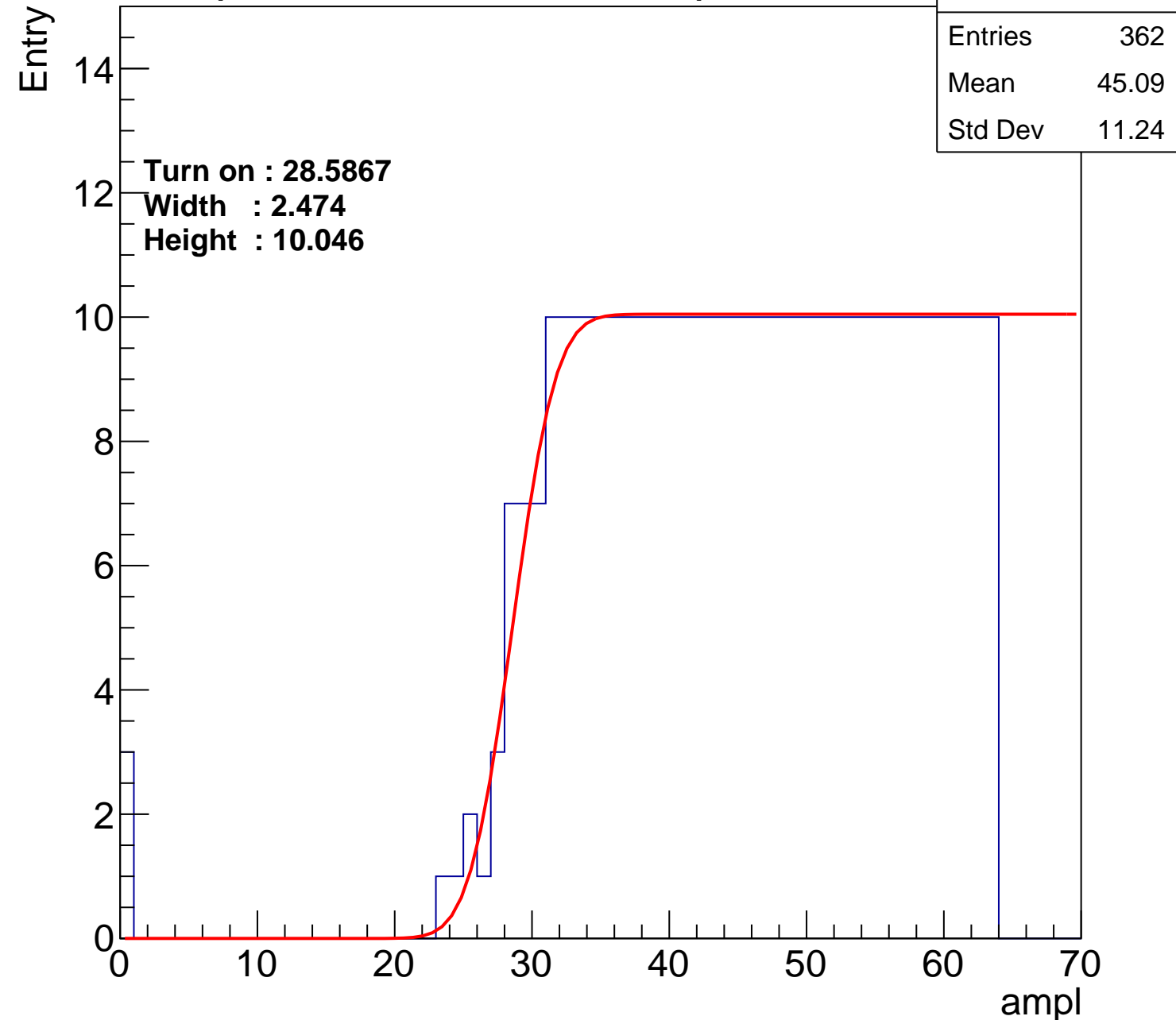
Width : 2.474

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch32

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.59
Std Dev	11.18

Turn on : 26.7890

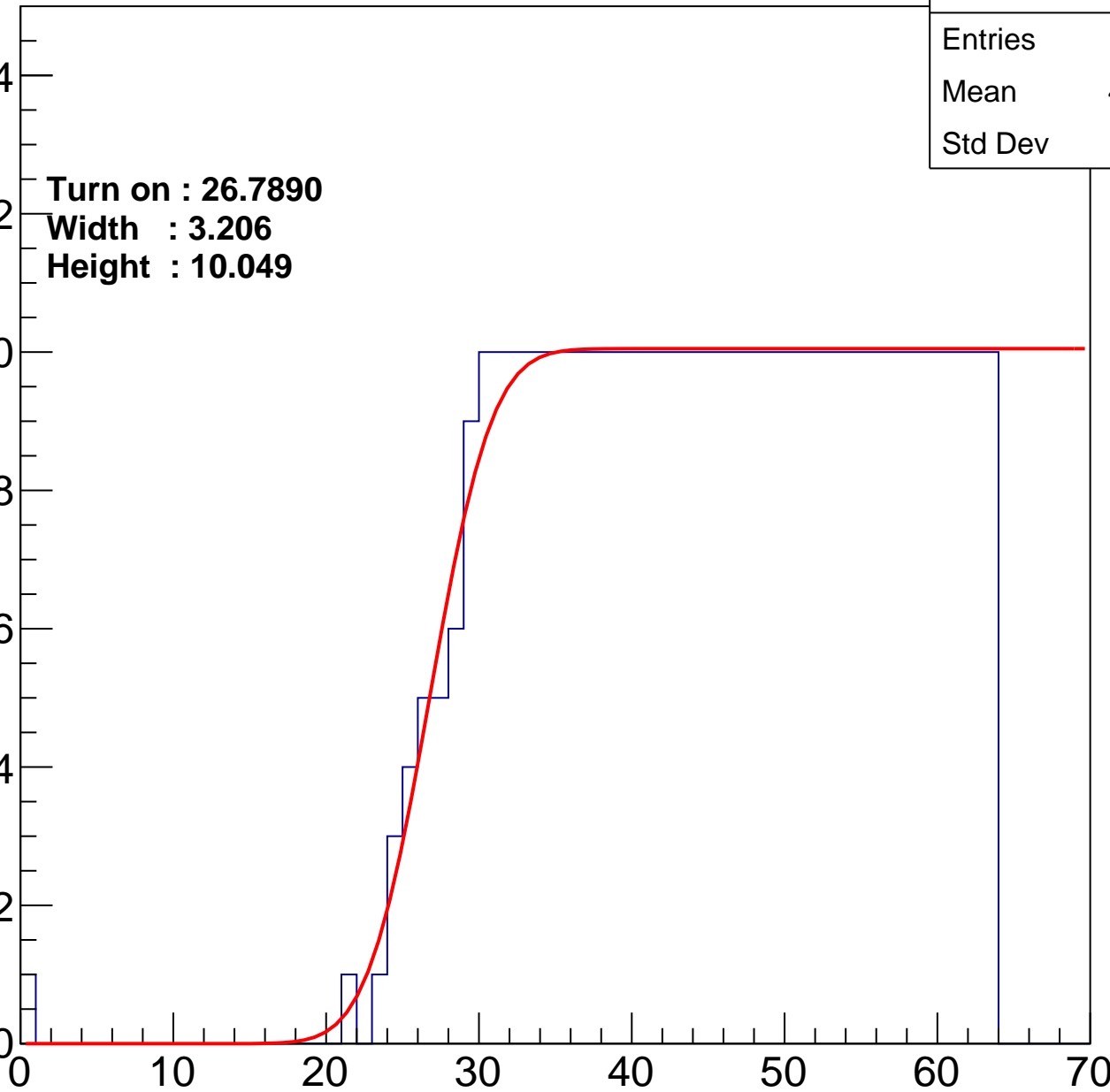
Width : 3.206

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch33

calib_packv5_042523_0143.root, FC#0, port D2

Entries	384
Mean	44.02
Std Dev	11.76

Turn on : 26.0887

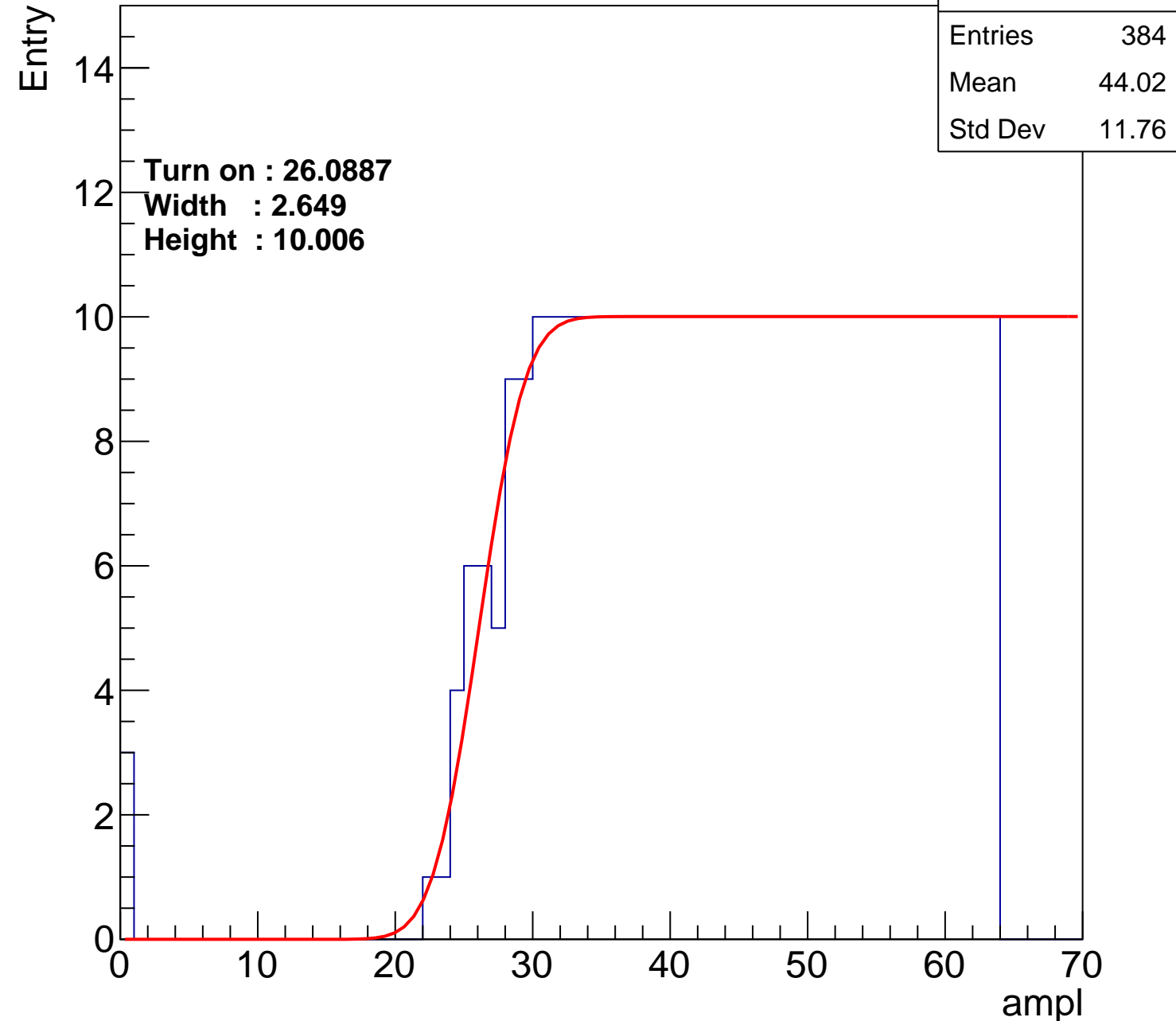
Width : 2.649

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch34

calib_packv5_042523_0143.root, FC#0, port D2

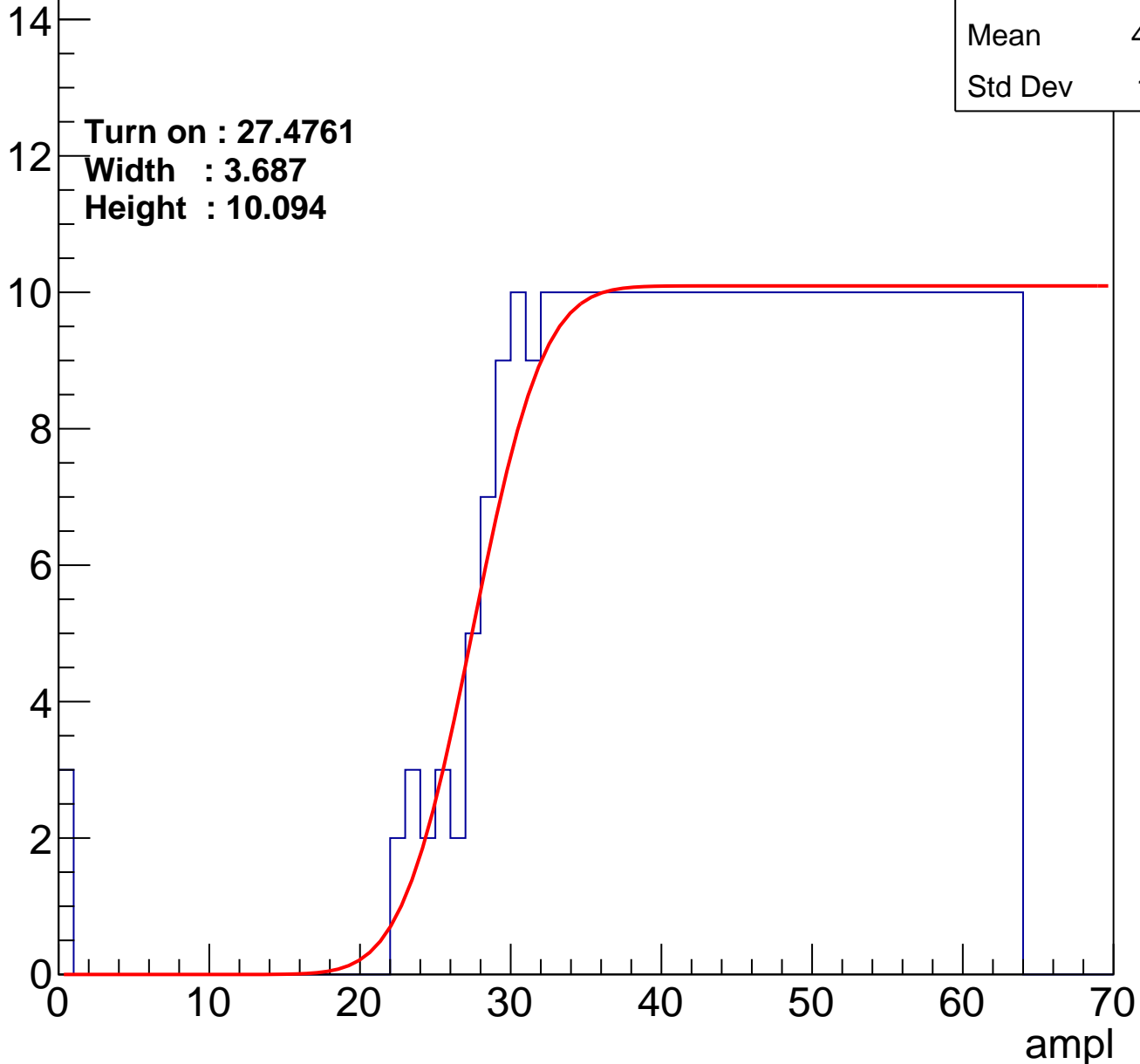
Entries	375
Mean	44.42
Std Dev	11.61

Turn on : 27.4761

Width : 3.687

Height : 10.094

Entry



B1L101S, U11-ch35

calib_packv5_042523_0143.root, FC#0, port D2

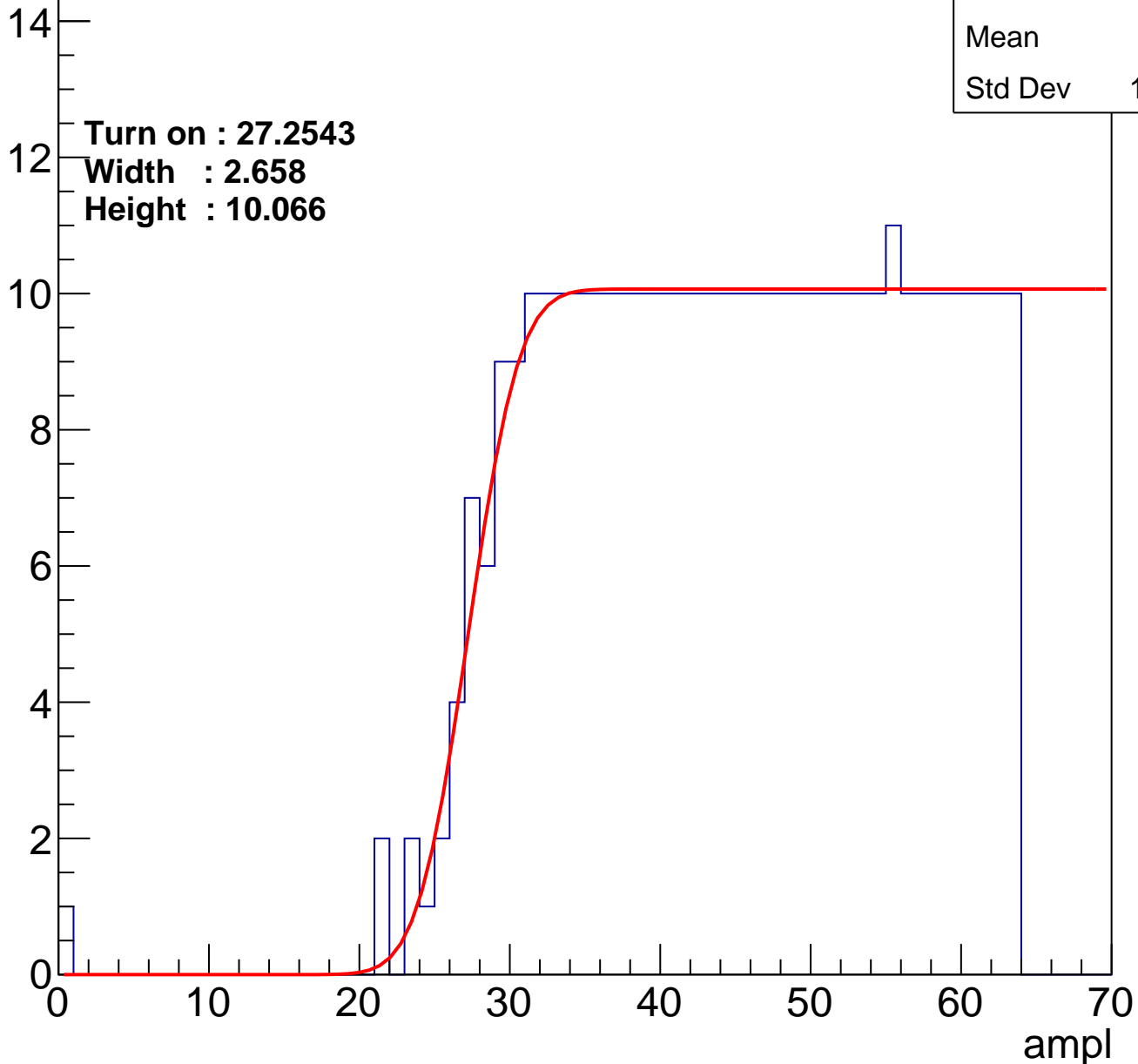
Entries	374
Mean	44.7
Std Dev	11.15

Turn on : 27.2543

Width : 2.658

Height : 10.066

Entry



B1L101S, U11-ch36

calib_packv5_042523_0143.root, FC#0, port D2

Entries	368
Mean	44.97
Std Dev	10.93

Turn on : 27.0967

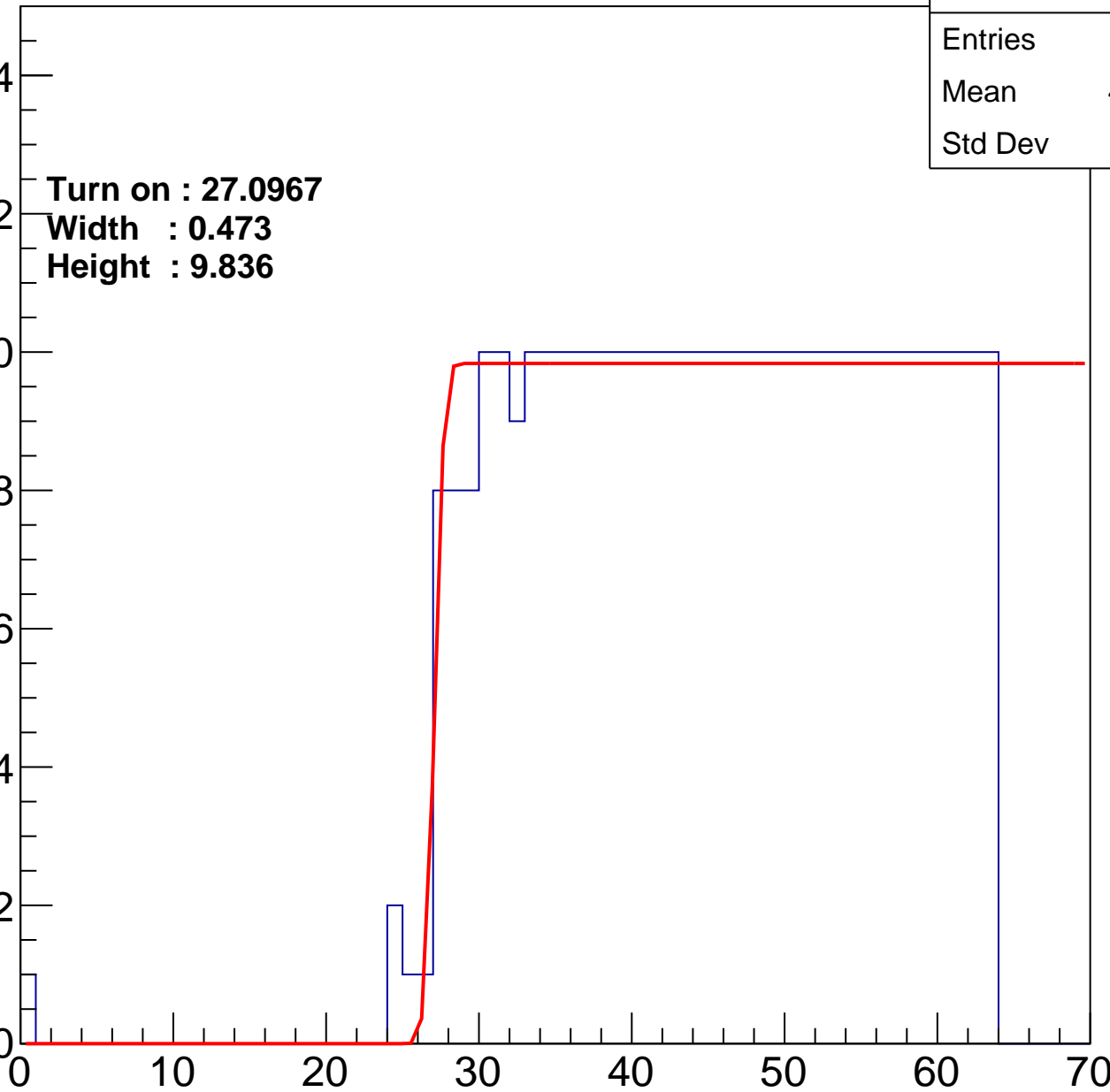
Width : 0.473

Height : 9.836

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch37

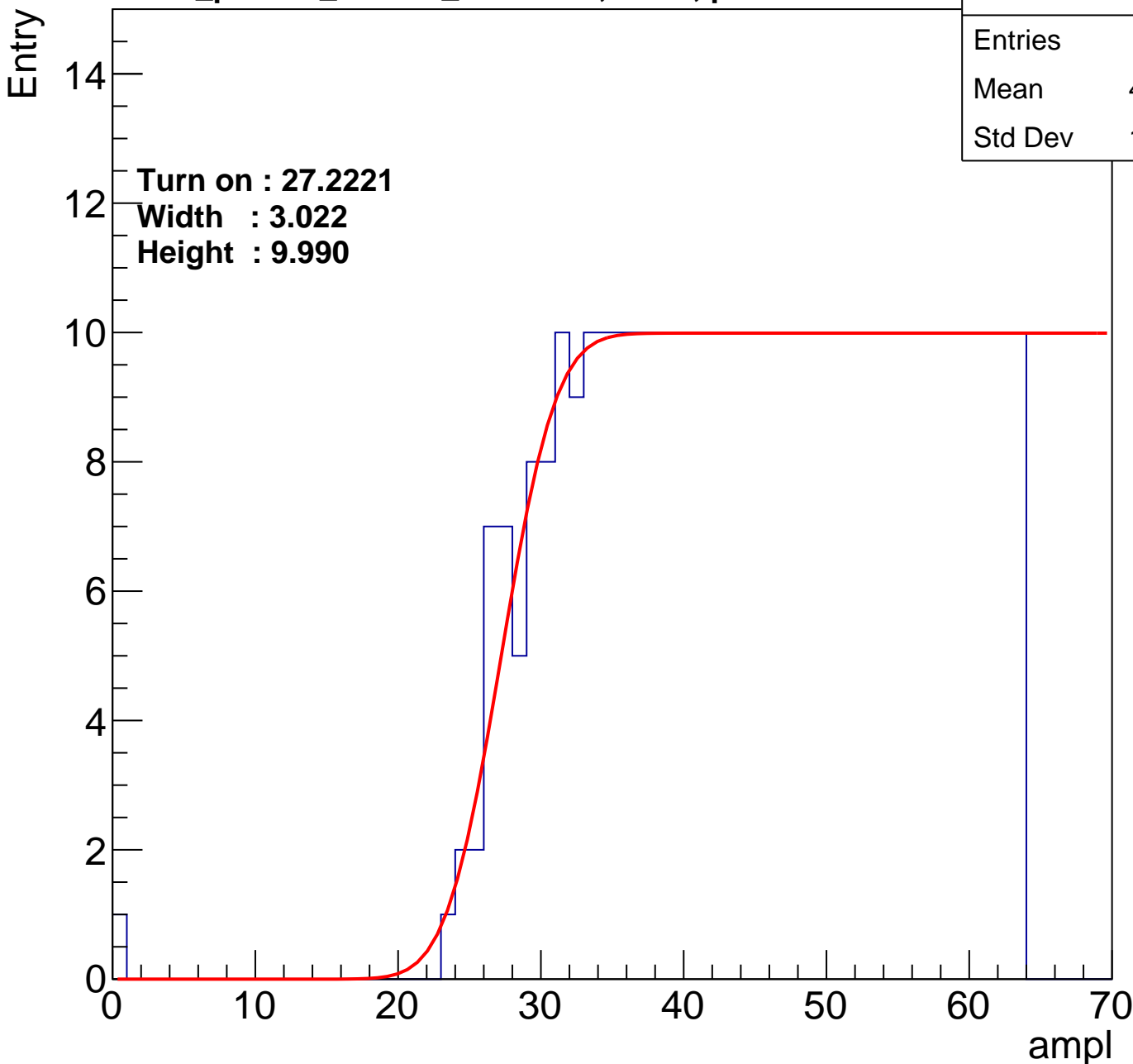
calib_packv5_042523_0143.root, FC#0, port D2

Entries	370
Mean	44.82
Std Dev	11.07

Turn on : 27.2221

Width : 3.022

Height : 9.990



B1L101S, U11-ch38

calib_packv5_042523_0143.root, FC#0, port D2

Entries	386
Mean	44.07
Std Dev	11.43

Turn on : 25.7152

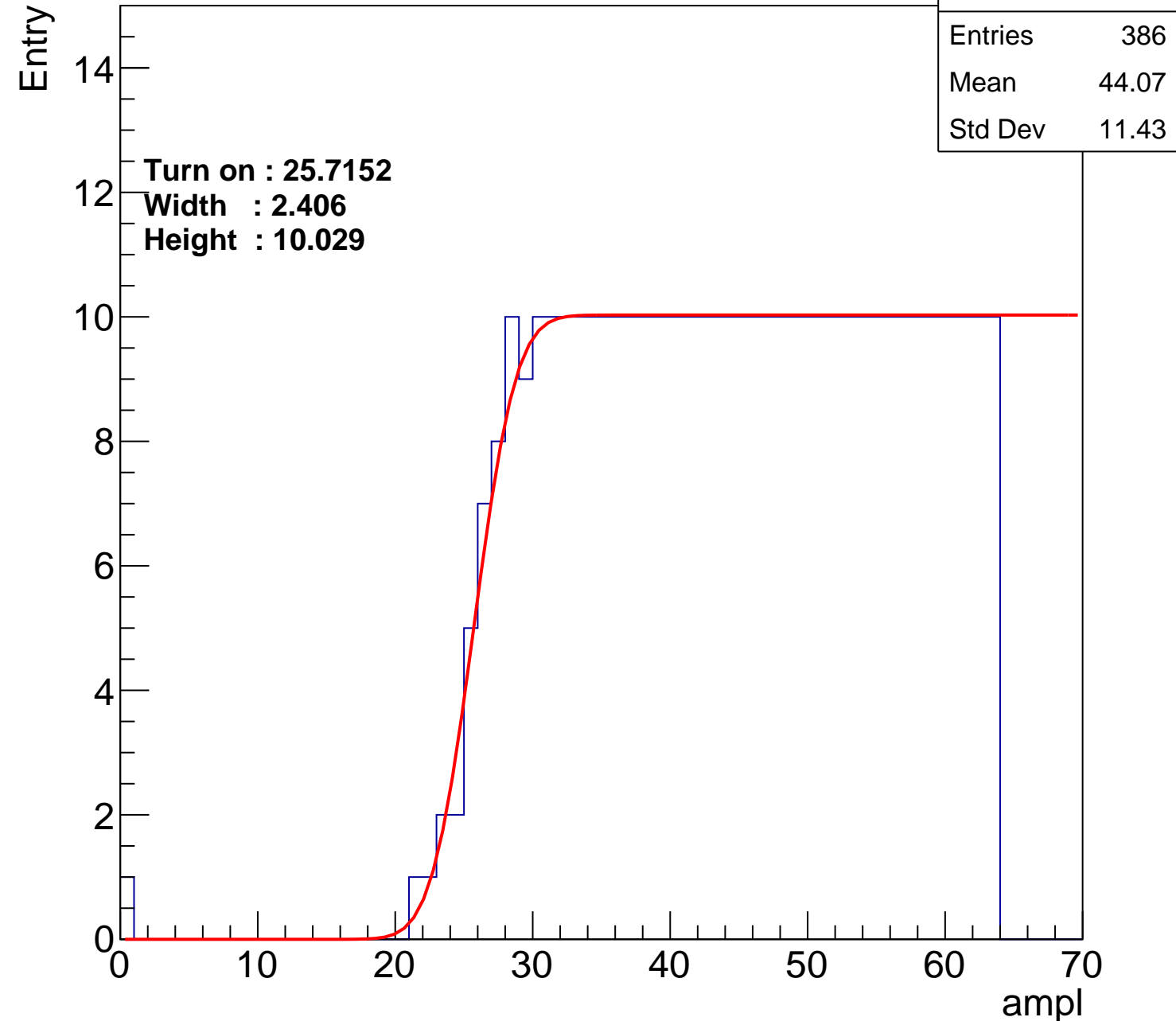
Width : 2.406

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch39

calib_packv5_042523_0143.root, FC#0, port D2

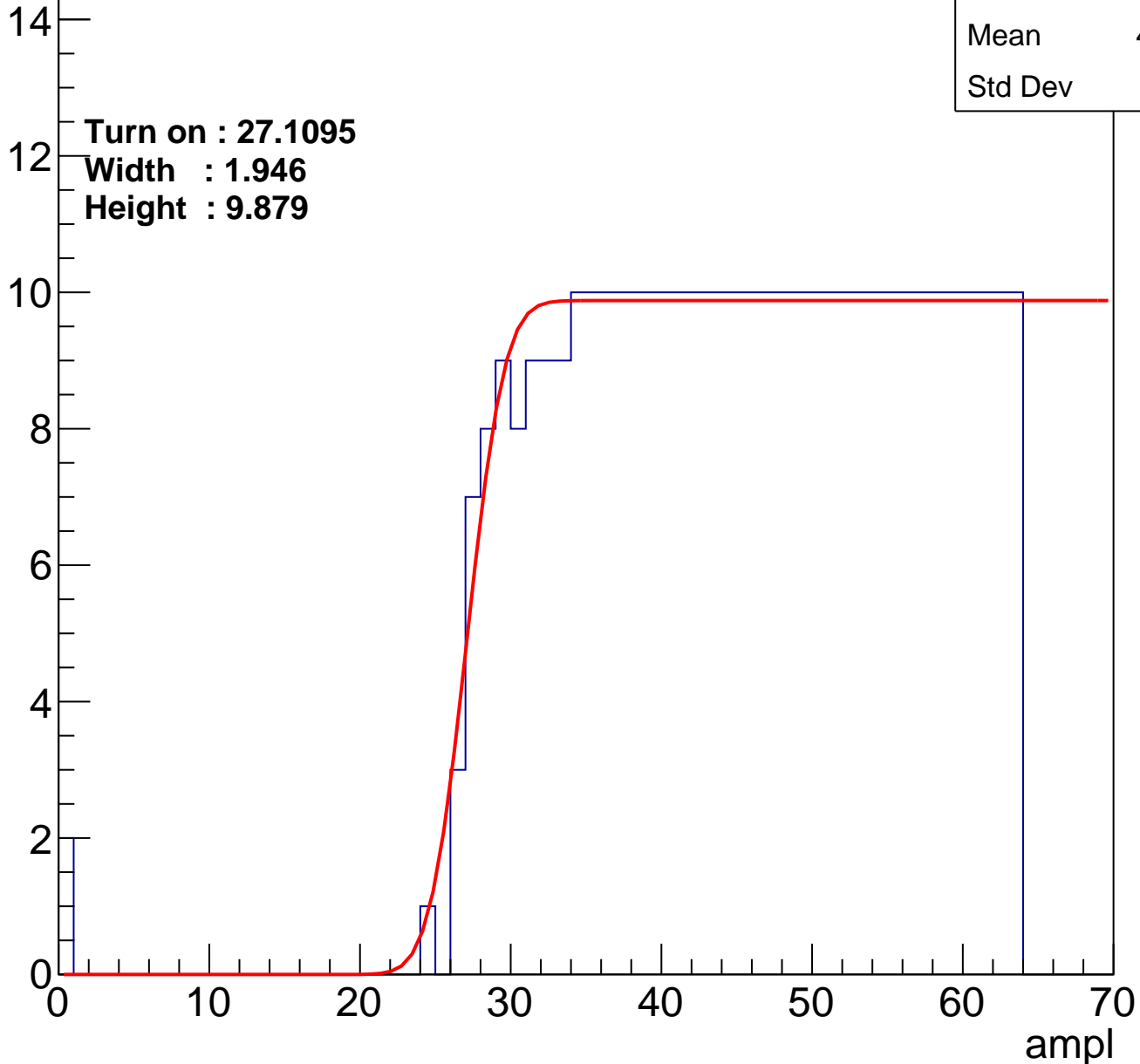
Entries	365
Mean	45.01
Std Dev	11.1

Turn on : 27.1095

Width : 1.946

Height : 9.879

Entry



B1L101S, U11-ch40

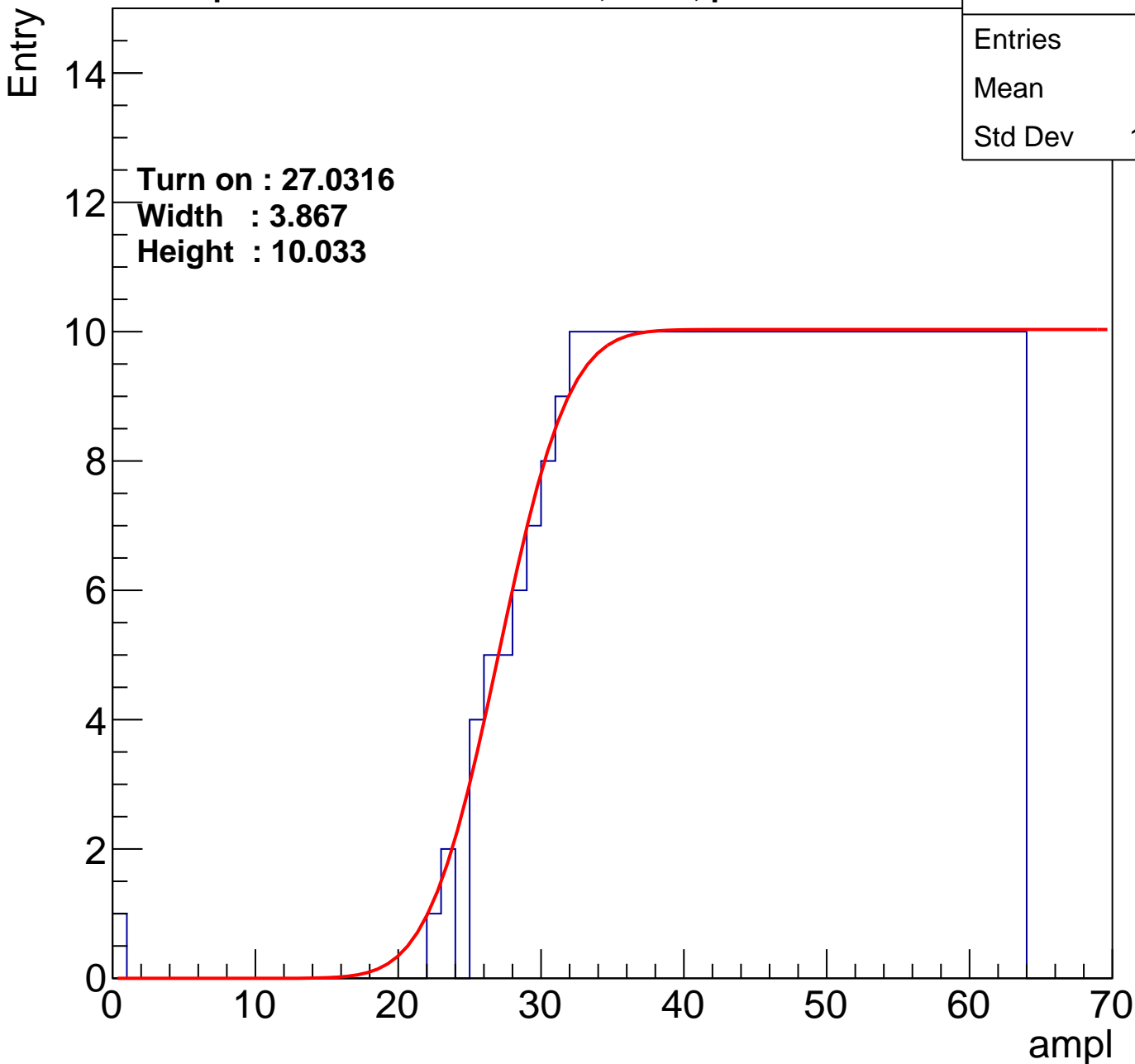
calib_packv5_042523_0143.root, FC#0, port D2

Entries	368
Mean	44.9
Std Dev	11.05

Turn on : 27.0316

Width : 3.867

Height : 10.033



B1L101S, U11-ch41

calib_packv5_042523_0143.root, FC#0, port D2

Entries	370
Mean	44.76
Std Dev	11.26

Turn on : 27.3926

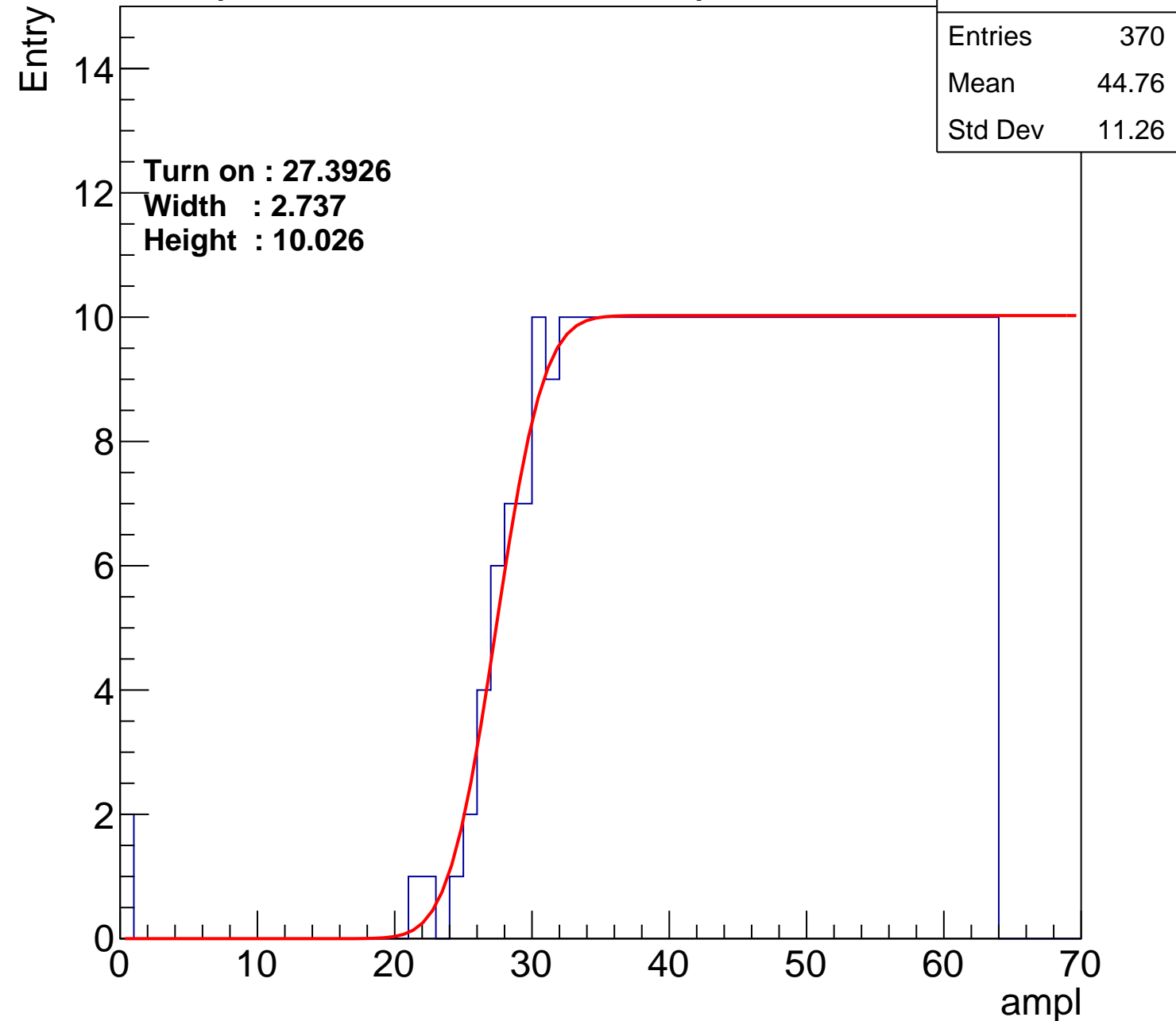
Width : 2.737

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch42

calib_packv5_042523_0143.root, FC#0, port D2

Entries	378
Mean	44.2
Std Dev	11.87

Turn on : 26.9053

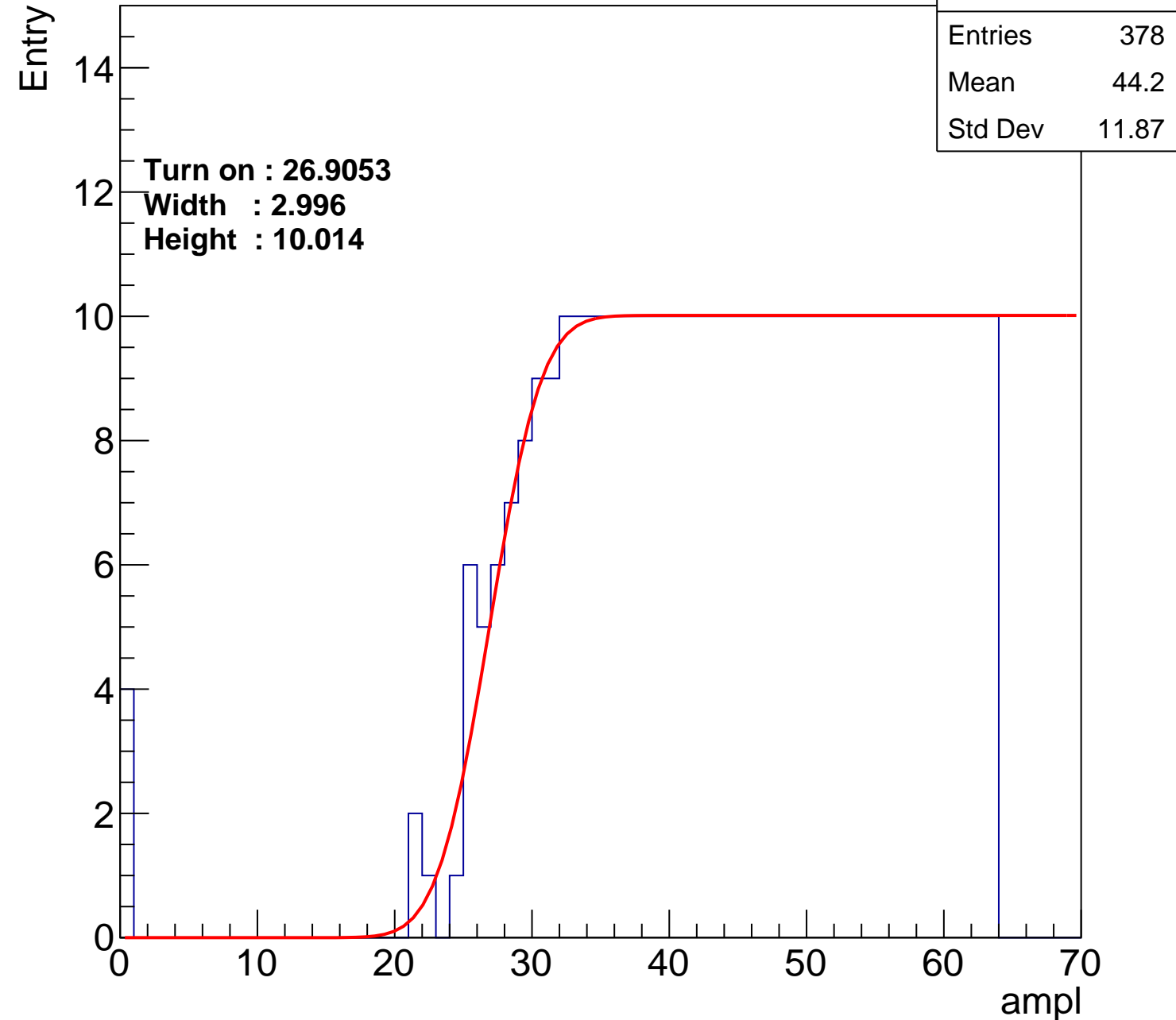
Width : 2.996

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch43

calib_packv5_042523_0143.root, FC#0, port D2

Entries	365
Mean	44.92
Std Dev	11.36

Turn on : 28.0323

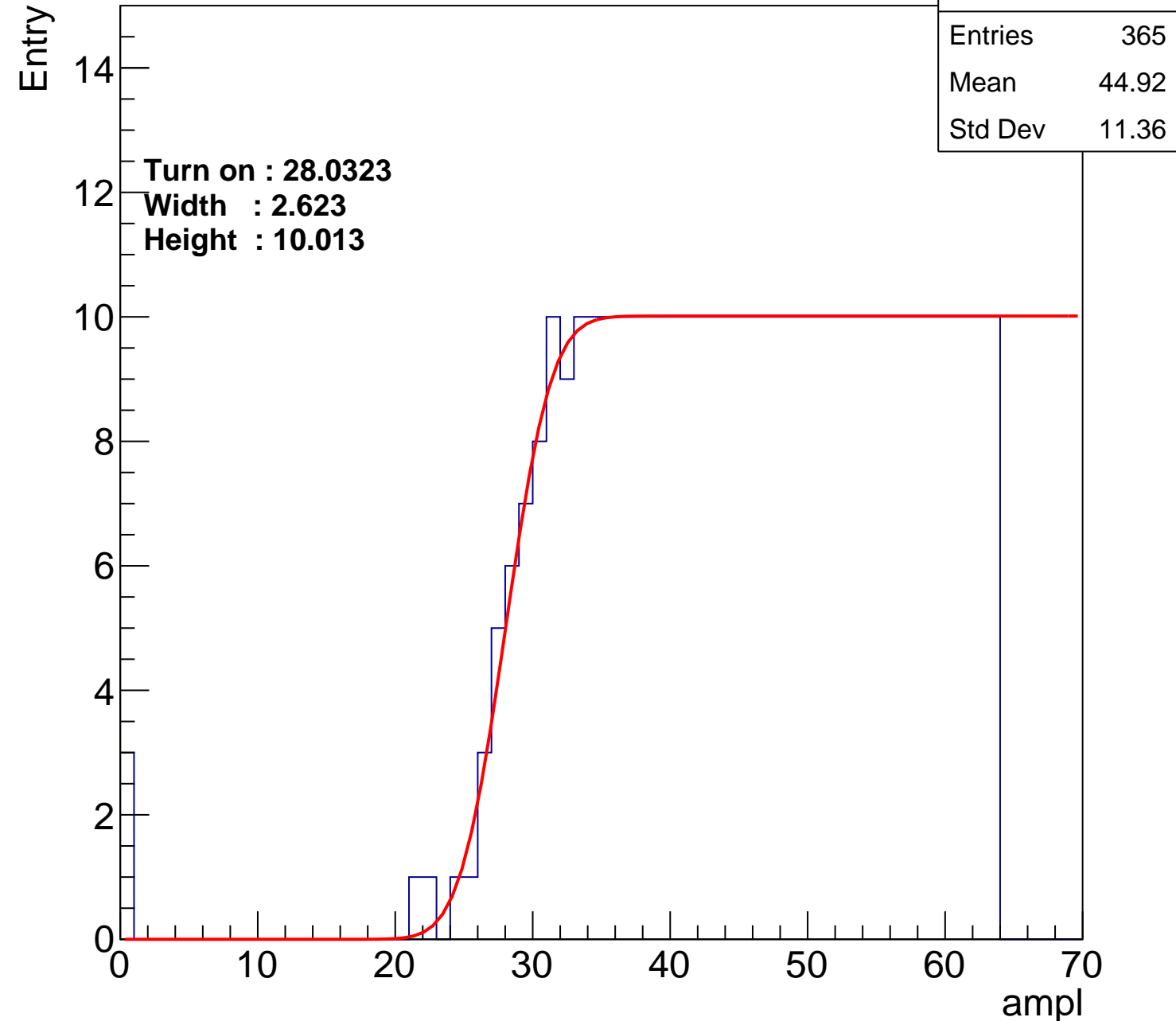
Width : 2.623

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch44

calib_packv5_042523_0143.root, FC#0, port D2

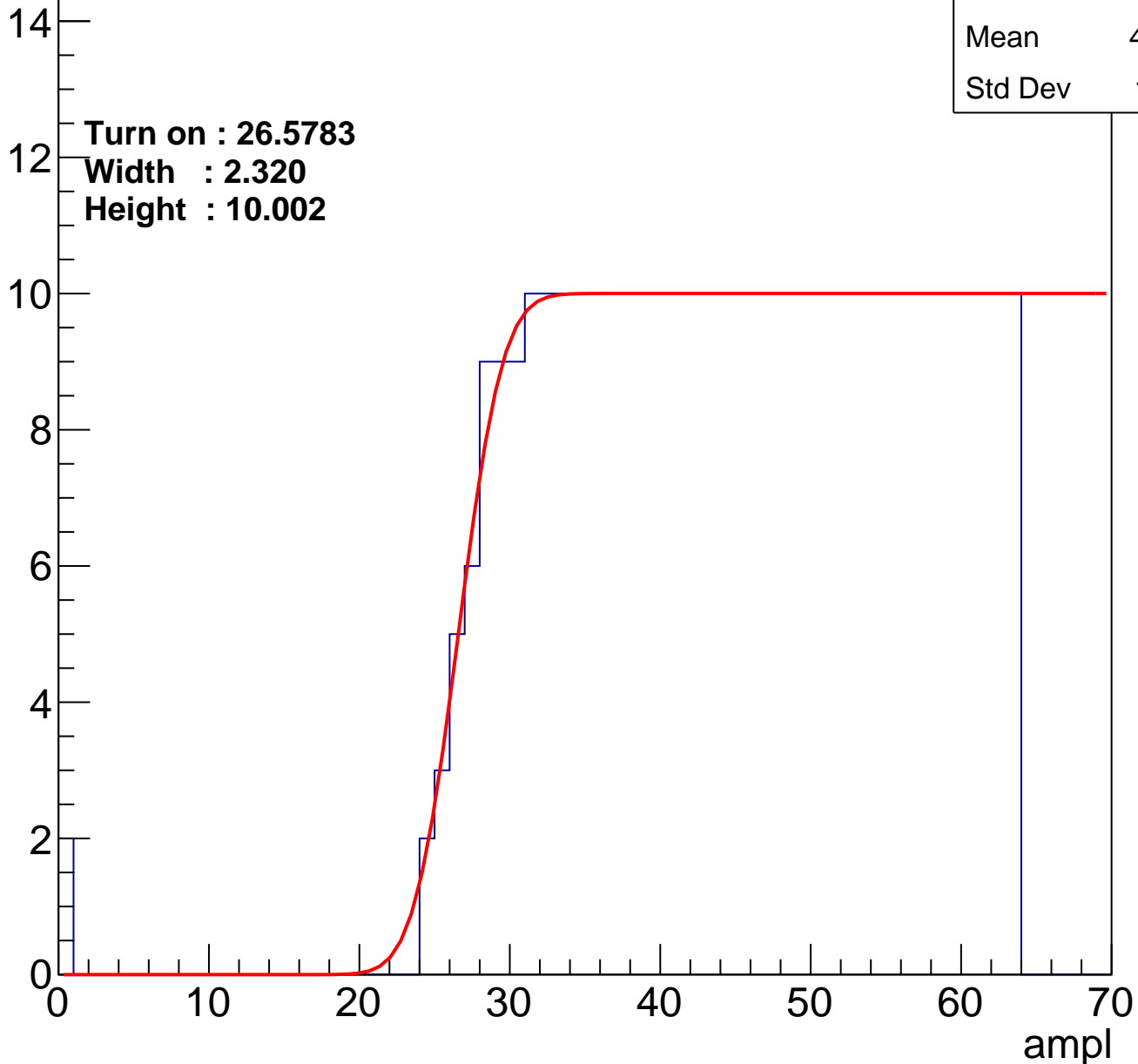
Entries	375
Mean	44.55
Std Dev	11.31

Turn on : 26.5783

Width : 2.320

Height : 10.002

Entry



B1L101S, U11-ch45

calib_packv5_042523_0143.root, FC#0, port D2

Entries	378
Mean	44.45
Std Dev	11.24

Turn on : 26.6254

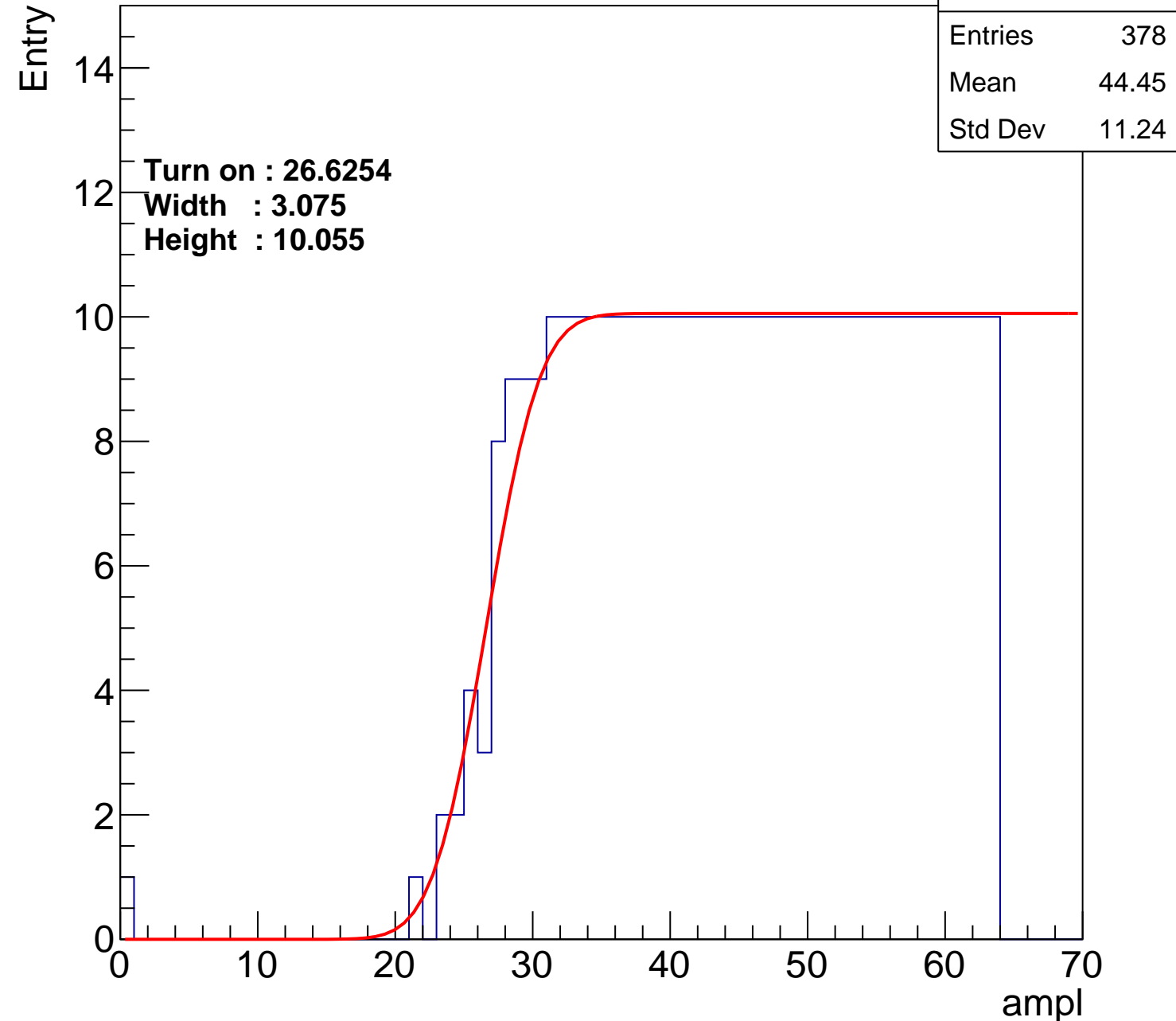
Width : 3.075

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch46

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.29
Std Dev	11.95

Turn on : 27.0103

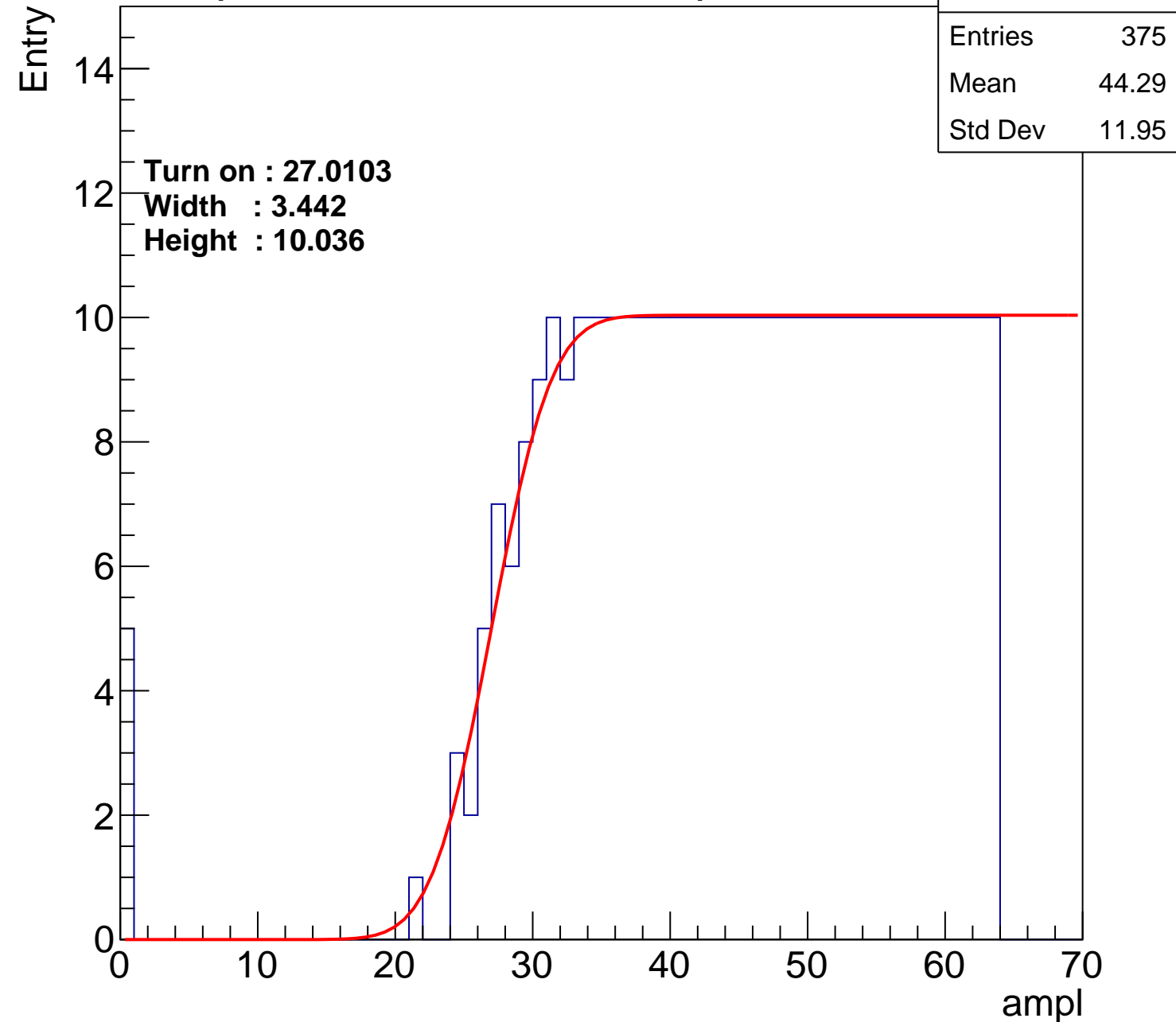
Width : 3.442

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch47

calib_packv5_042523_0143.root, FC#0, port D2

Entries	362
Mean	45.13
Std Dev	11.09

Turn on : 28.4385

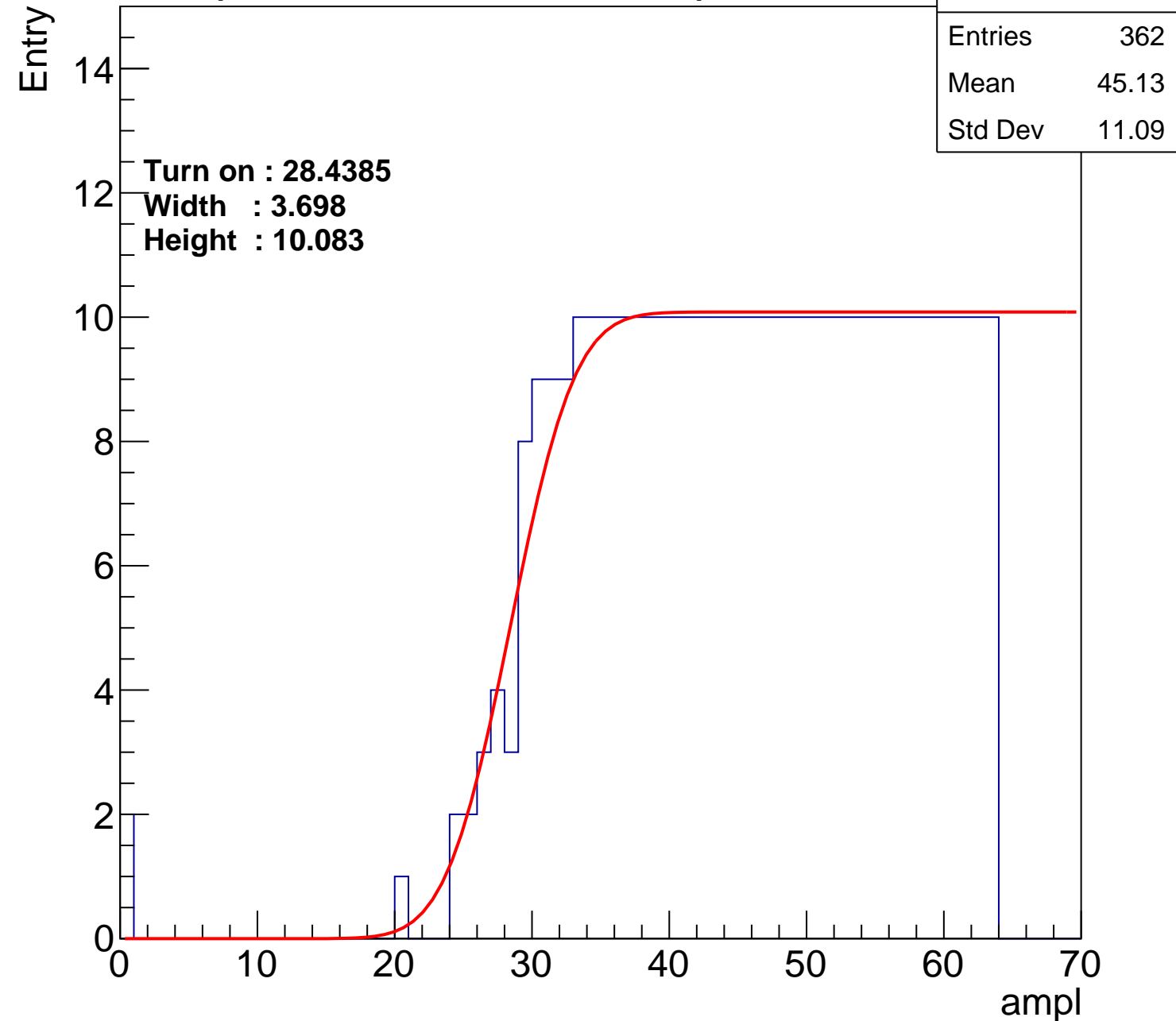
Width : 3.698

Height : 10.083

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch48

calib_packv5_042523_0143.root, FC#0, port D2

Entries	380
Mean	44.11
Std Dev	11.91

Turn on : 26.8939

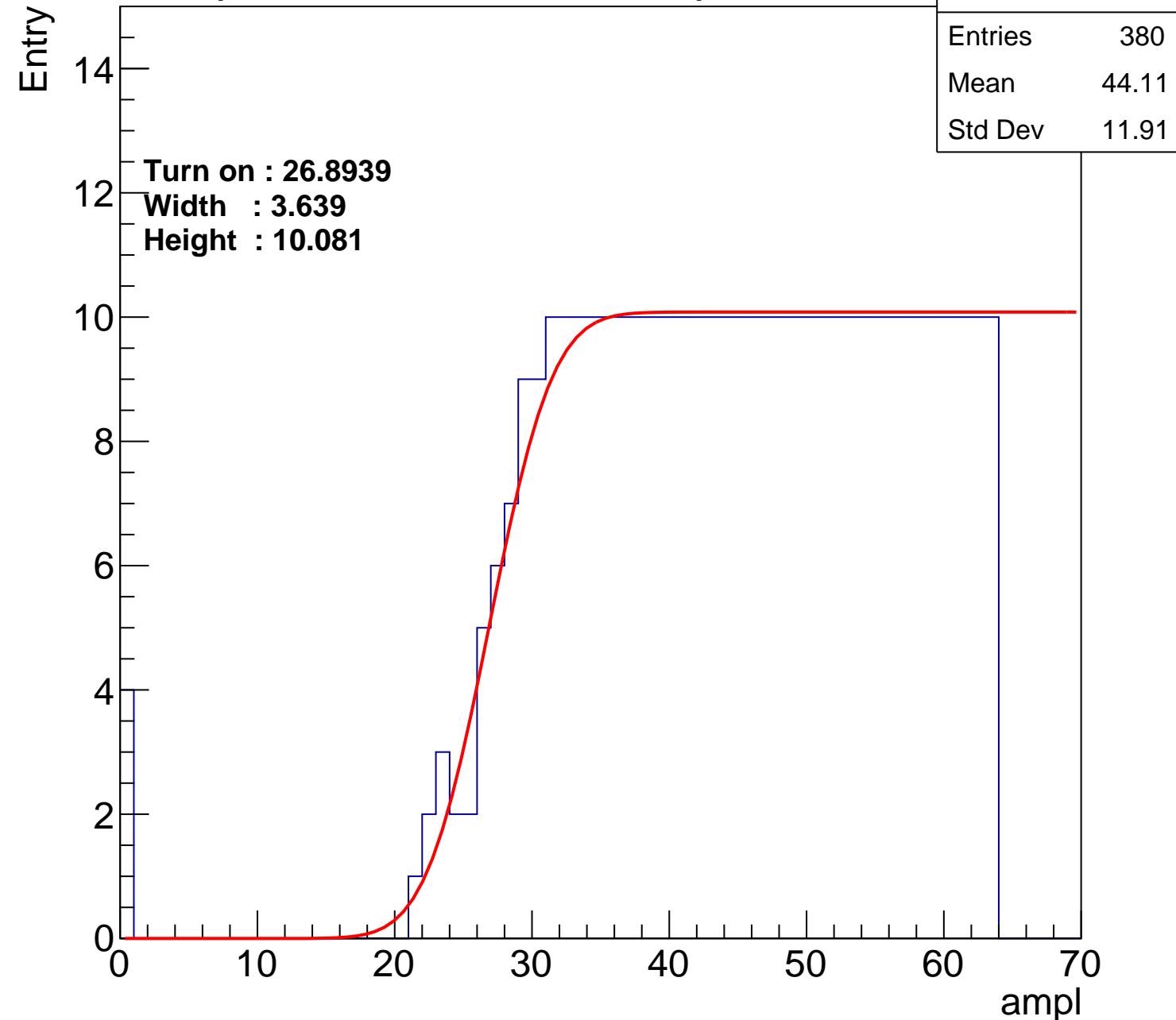
Width : 3.639

Height : 10.081

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch49

calib_packv5_042523_0143.root, FC#0, port D2

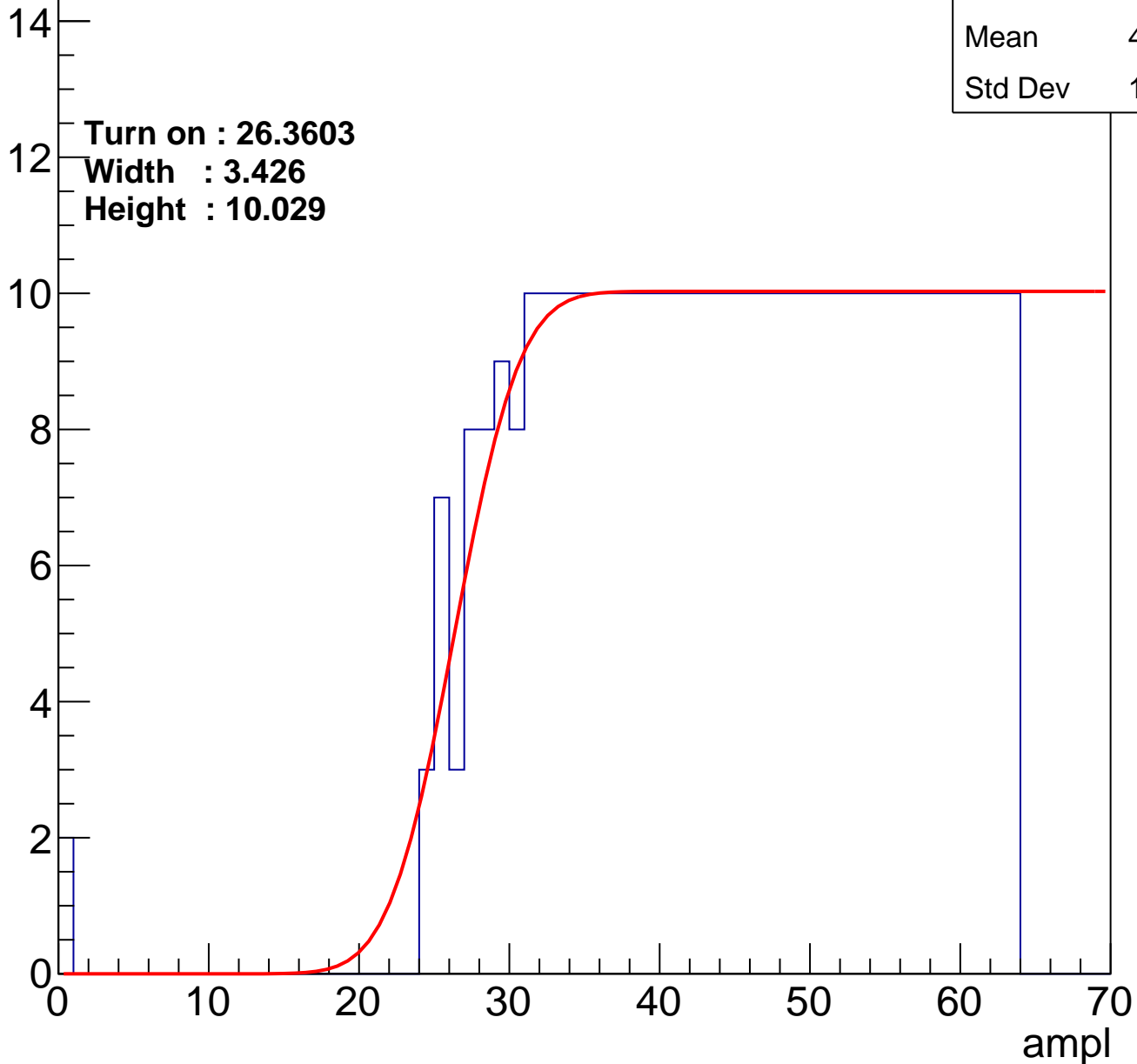
Entries	378
Mean	44.38
Std Dev	11.43

Turn on : 26.3603

Width : 3.426

Height : 10.029

Entry



calib_packv5_042523_0143.root, FC#0, port D2

calib_packv5_042523_0143.root, FC#0, port D2

Turn on : 25.0970
Width : 2.455
Height : 9.973



B1L101S, U11-ch51

calib_packv5_042523_0143.root, FC#0, port D2

Entries	388
Mean	43.81
Std Dev	11.89

Turn on : 25.8529

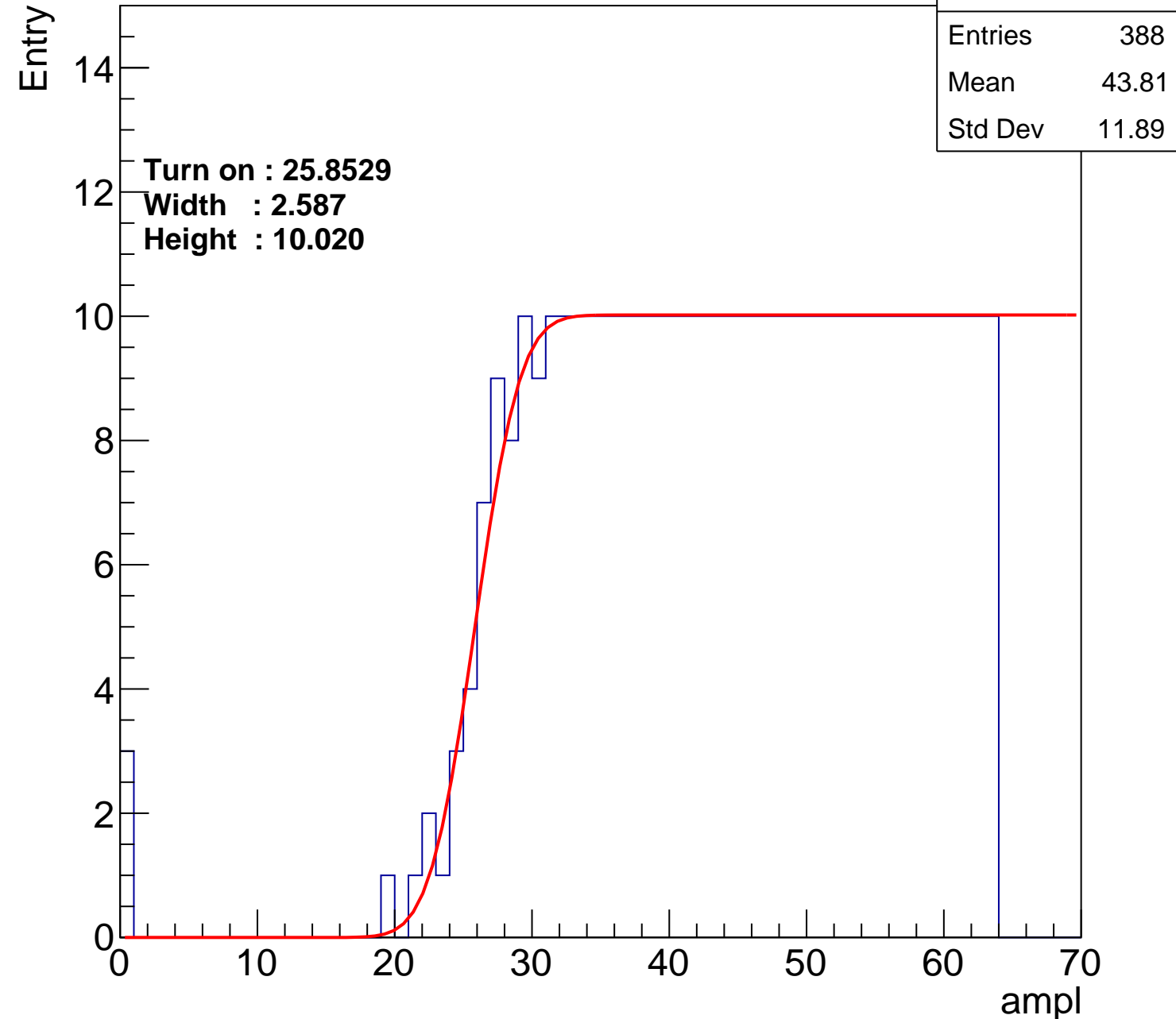
Width : 2.587

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch52

calib_packv5_042523_0143.root, FC#0, port D2

Entries	397
Mean	43.31
Std Dev	12.19

Turn on : 23.7874

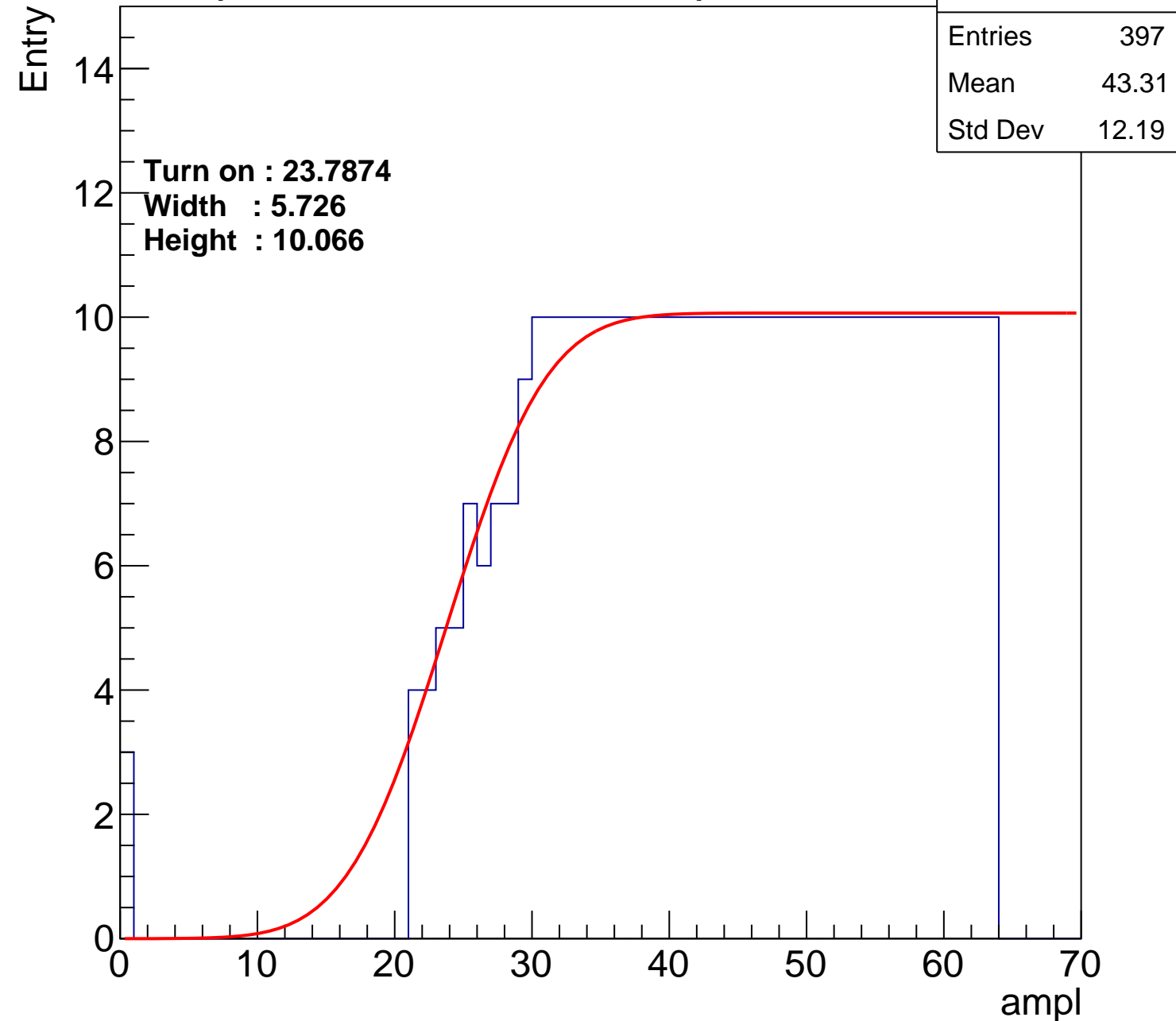
Width : 5.726

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch53

calib_packv5_042523_0143.root, FC#0, port D2

Entries	378
Mean	44.41
Std Dev	11.31

Turn on : 26.4629

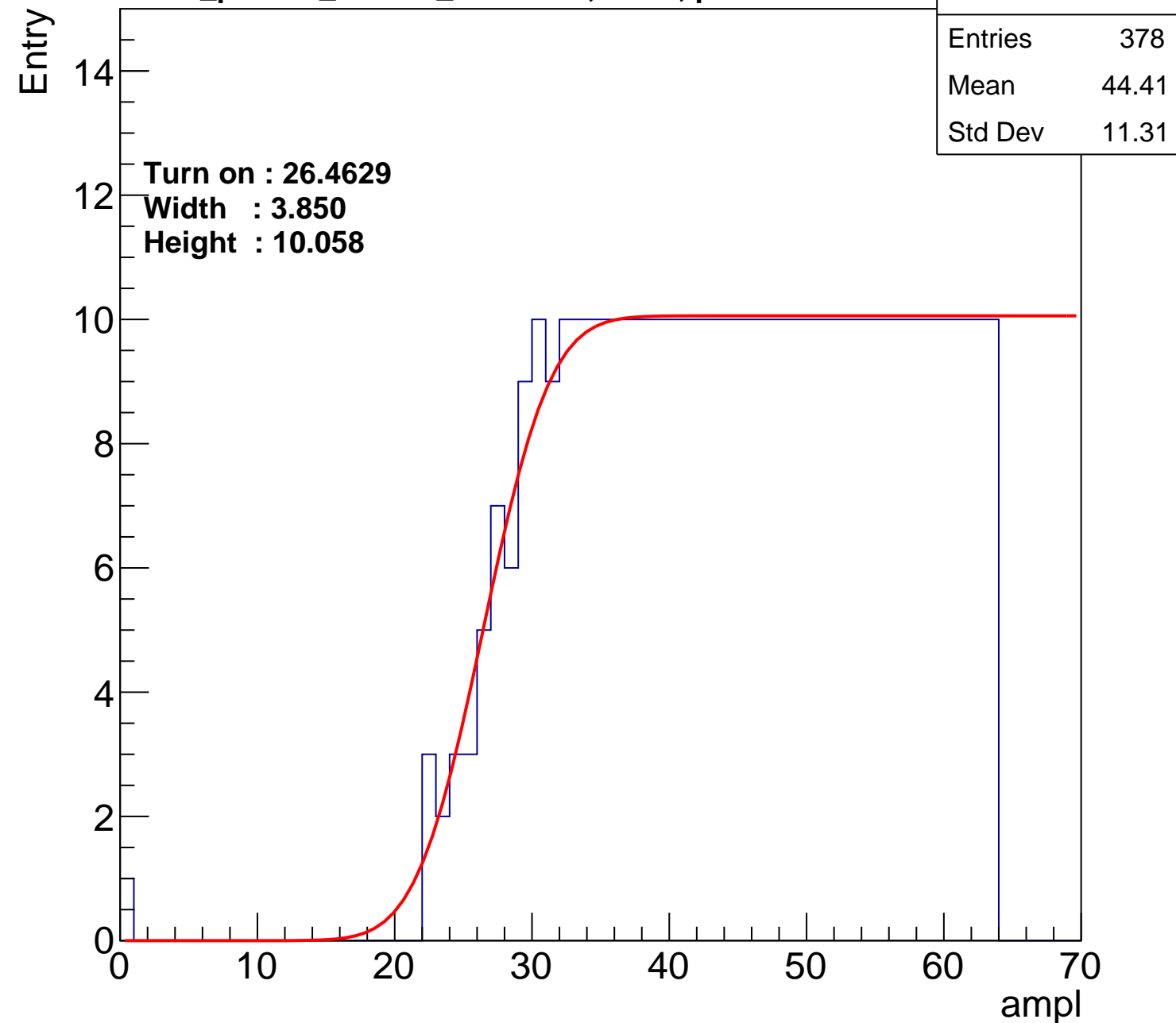
Width : 3.850

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch54

calib_packv5_042523_0143.root, FC#0, port D2

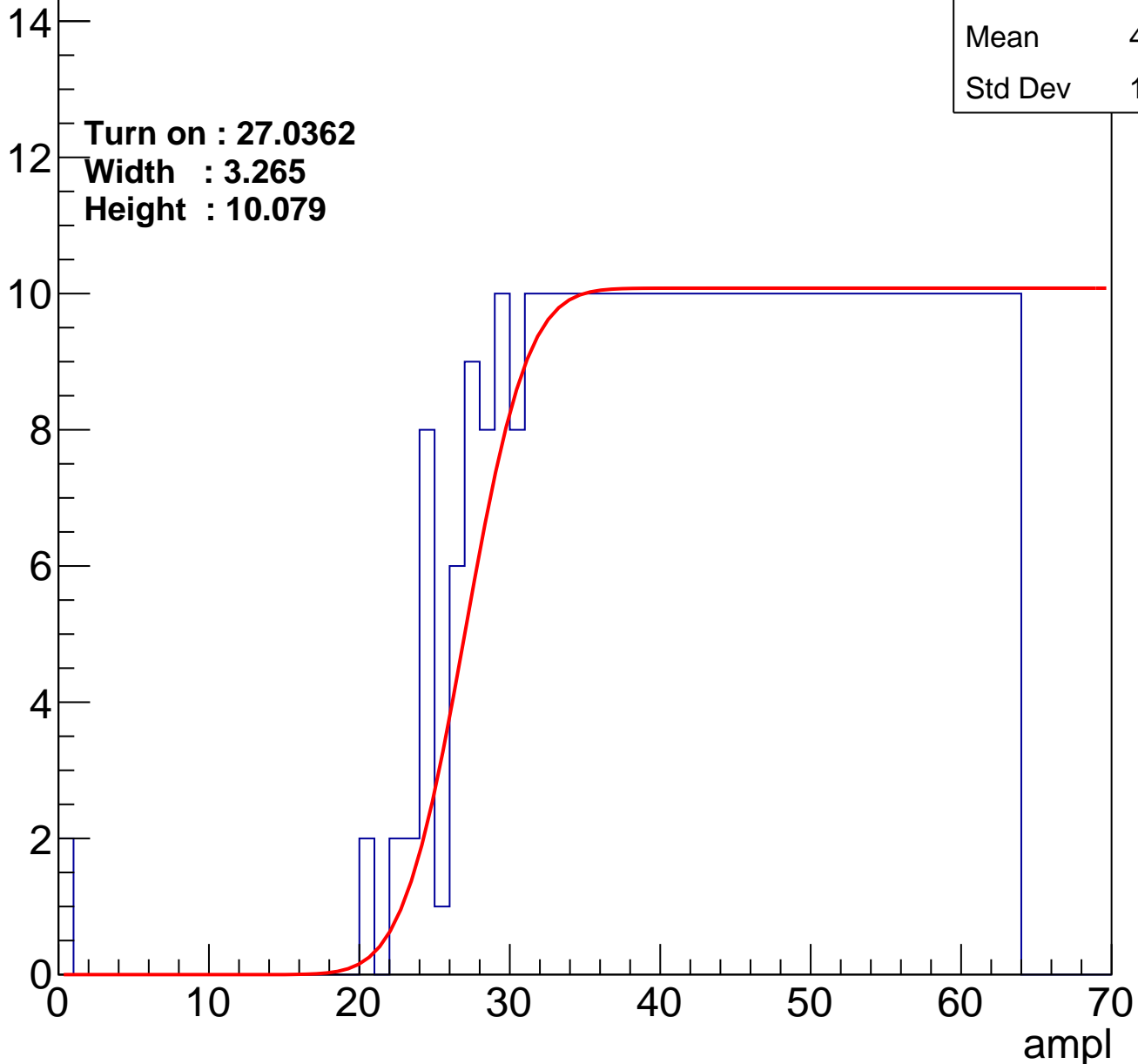
Entries	388
Mean	43.84
Std Dev	11.77

Turn on : 27.0362

Width : 3.265

Height : 10.079

Entry



B1L101S, U11-ch55

calib_packv5_042523_0143.root, FC#0, port D2

Entries	370
Mean	44.81
Std Dev	11.07

Turn on : 27.1291

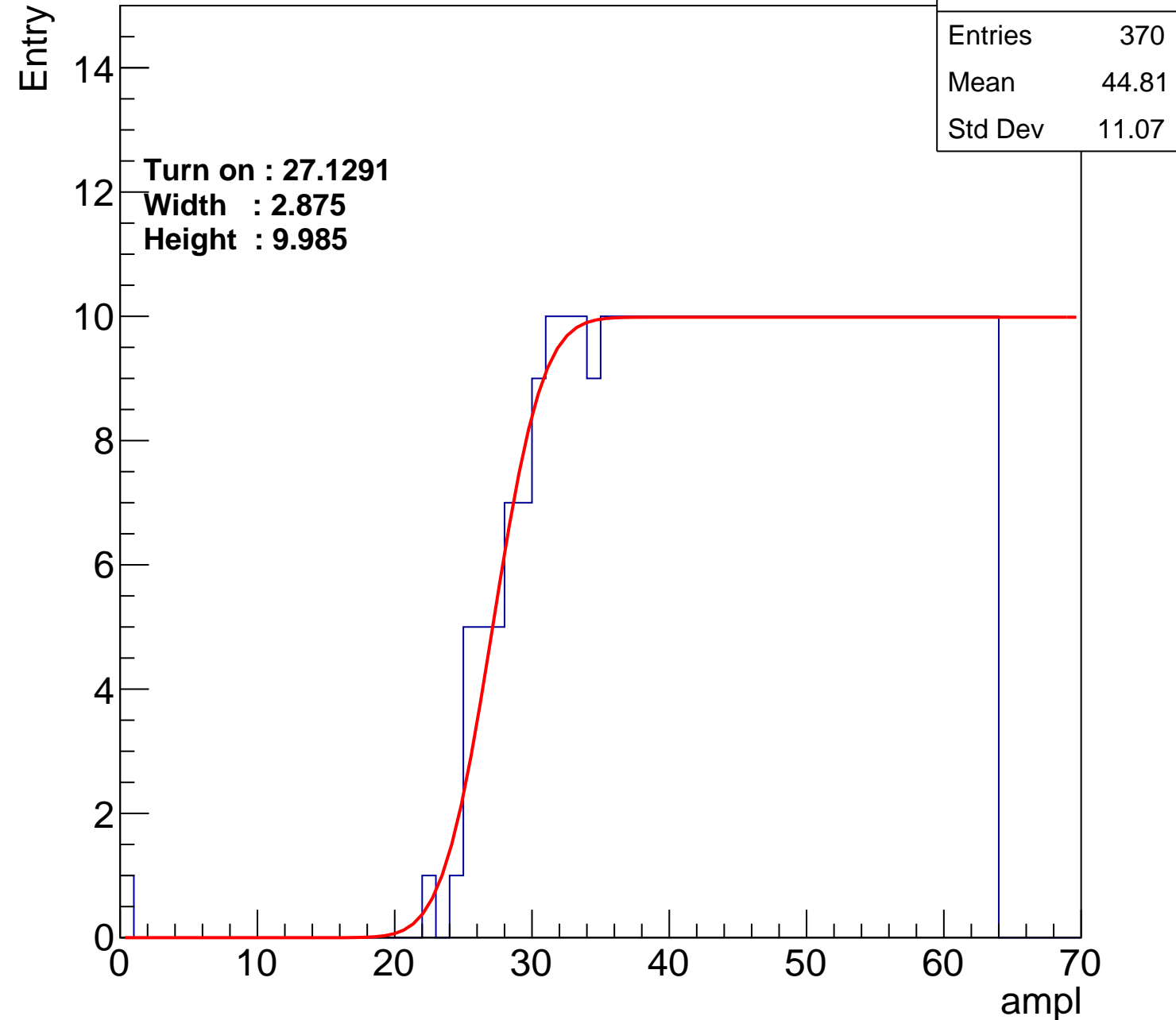
Width : 2.875

Height : 9.985

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch56

calib_packv5_042523_0143.root, FC#0, port D2

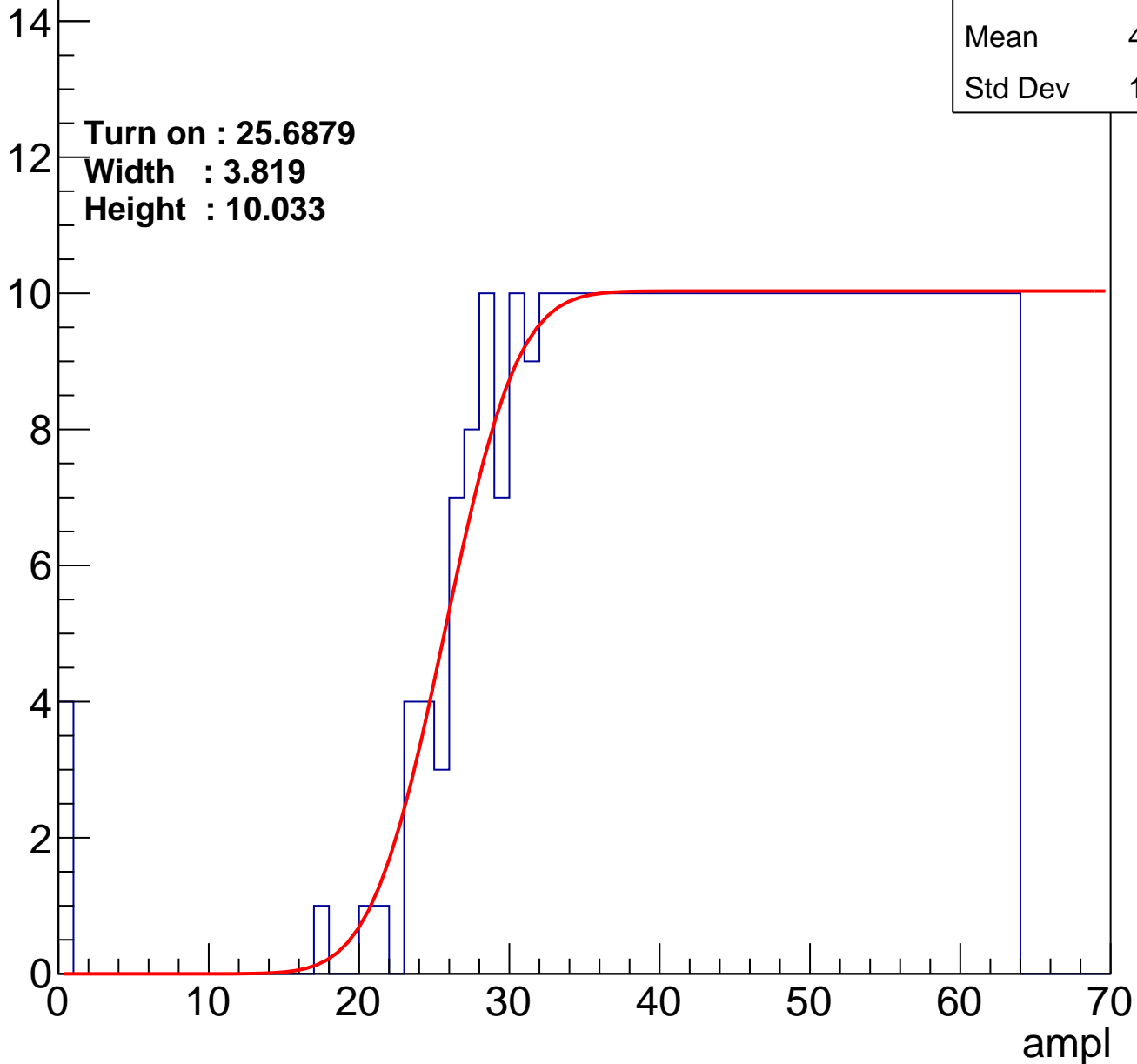
Entries	389
Mean	43.65
Std Dev	12.14

Turn on : 25.6879

Width : 3.819

Height : 10.033

Entry



B1L101S, U11-ch57

calib_packv5_042523_0143.root, FC#0, port D2

Entries	358
Mean	45.23
Std Dev	11.24

Turn on : 29.4758

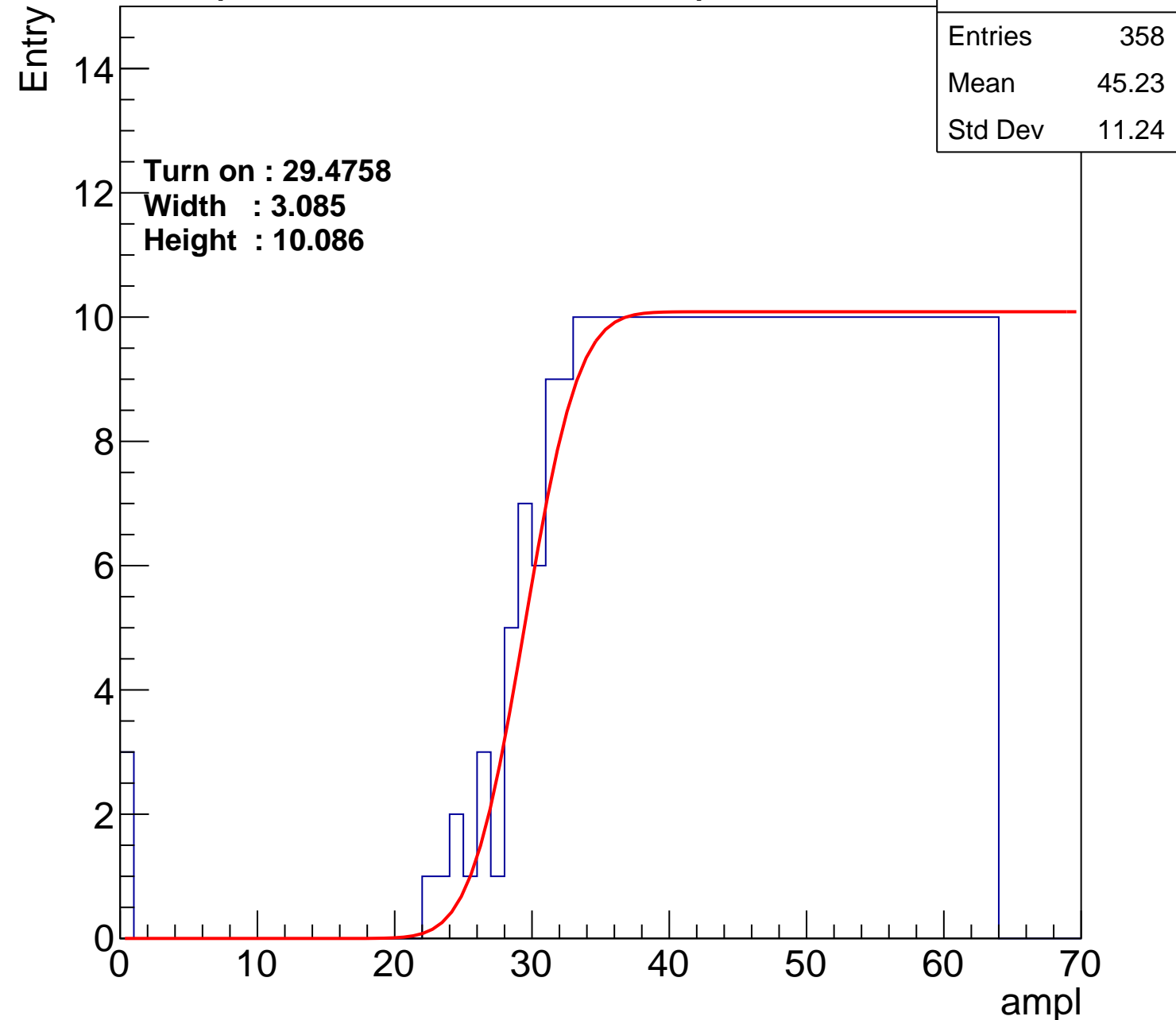
Width : 3.085

Height : 10.086

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch58

calib_packv5_042523_0143.root, FC#0, port D2

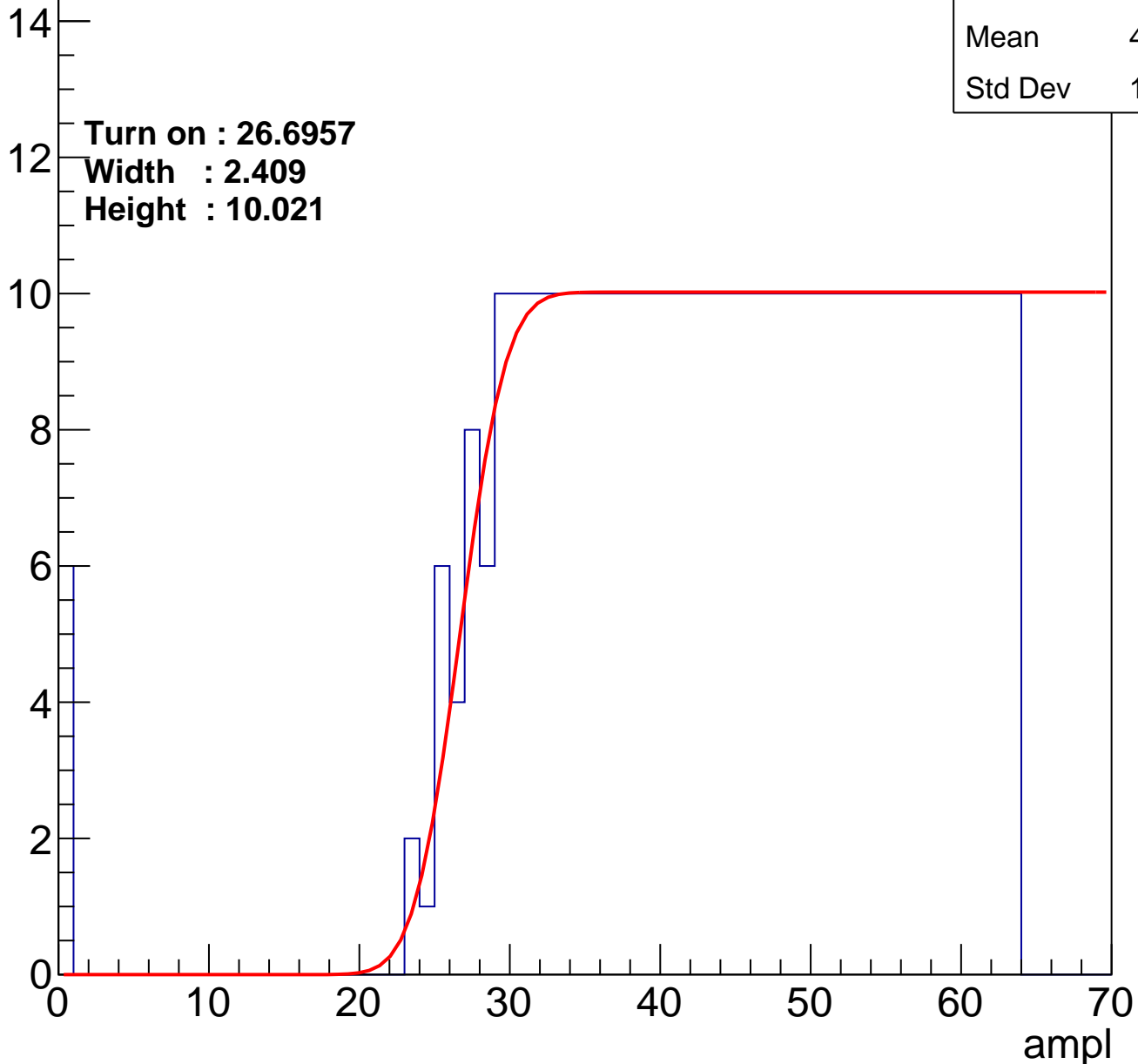
Entries	383
Mean	43.89
Std Dev	12.23

Turn on : 26.6957

Width : 2.409

Height : 10.021

Entry



B1L101S, U11-ch59

calib_packv5_042523_0143.root, FC#0, port D2

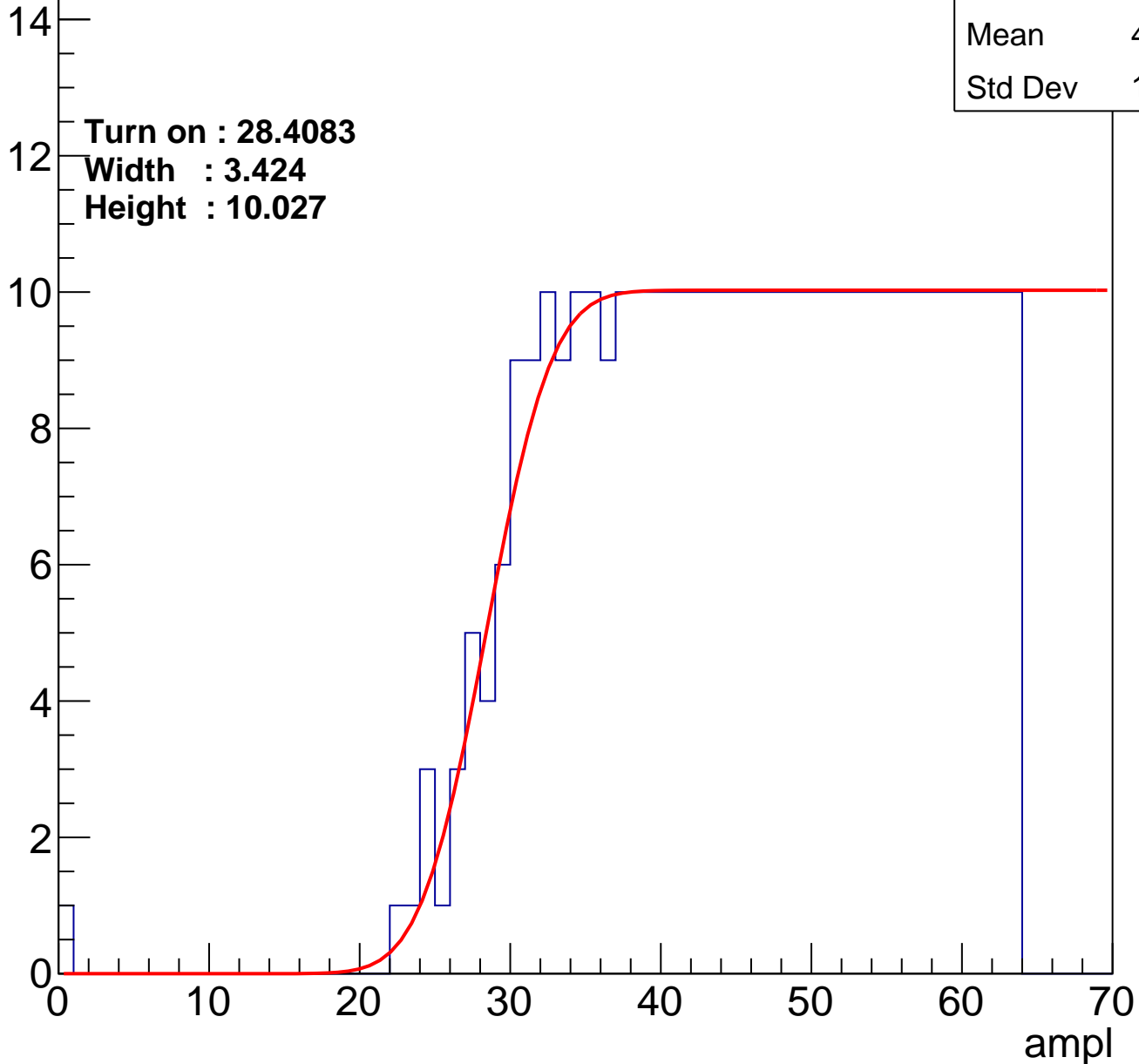
Entries	361
Mean	45.21
Std Dev	10.91

Turn on : 28.4083

Width : 3.424

Height : 10.027

Entry



B1L101S, U11-ch60

calib_packv5_042523_0143.root, FC#0, port D2

Entries	367
Mean	44.77
Std Dev	11.48

Turn on : 29.2375

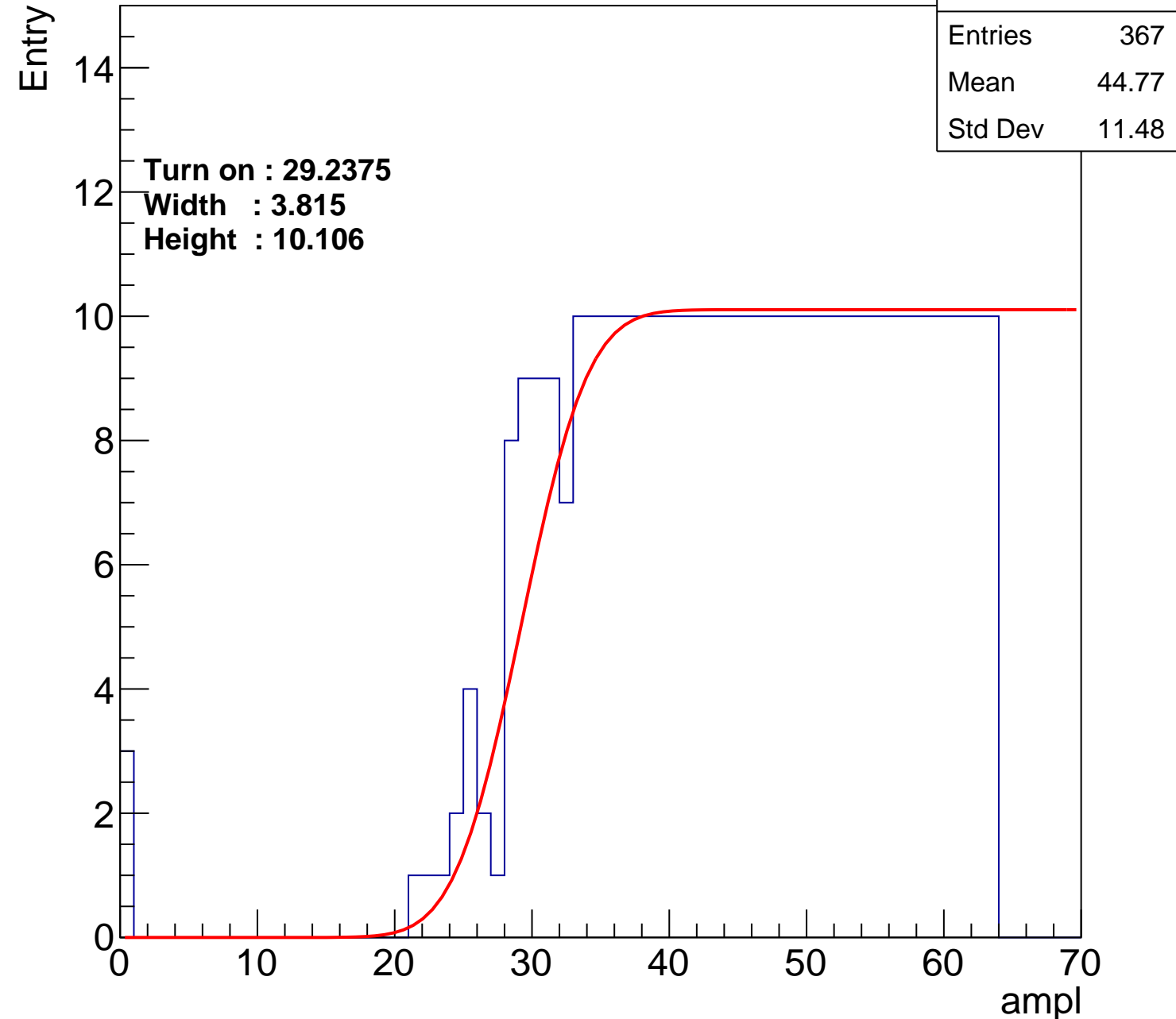
Width : 3.815

Height : 10.106

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch61

calib_packv5_042523_0143.root, FC#0, port D2

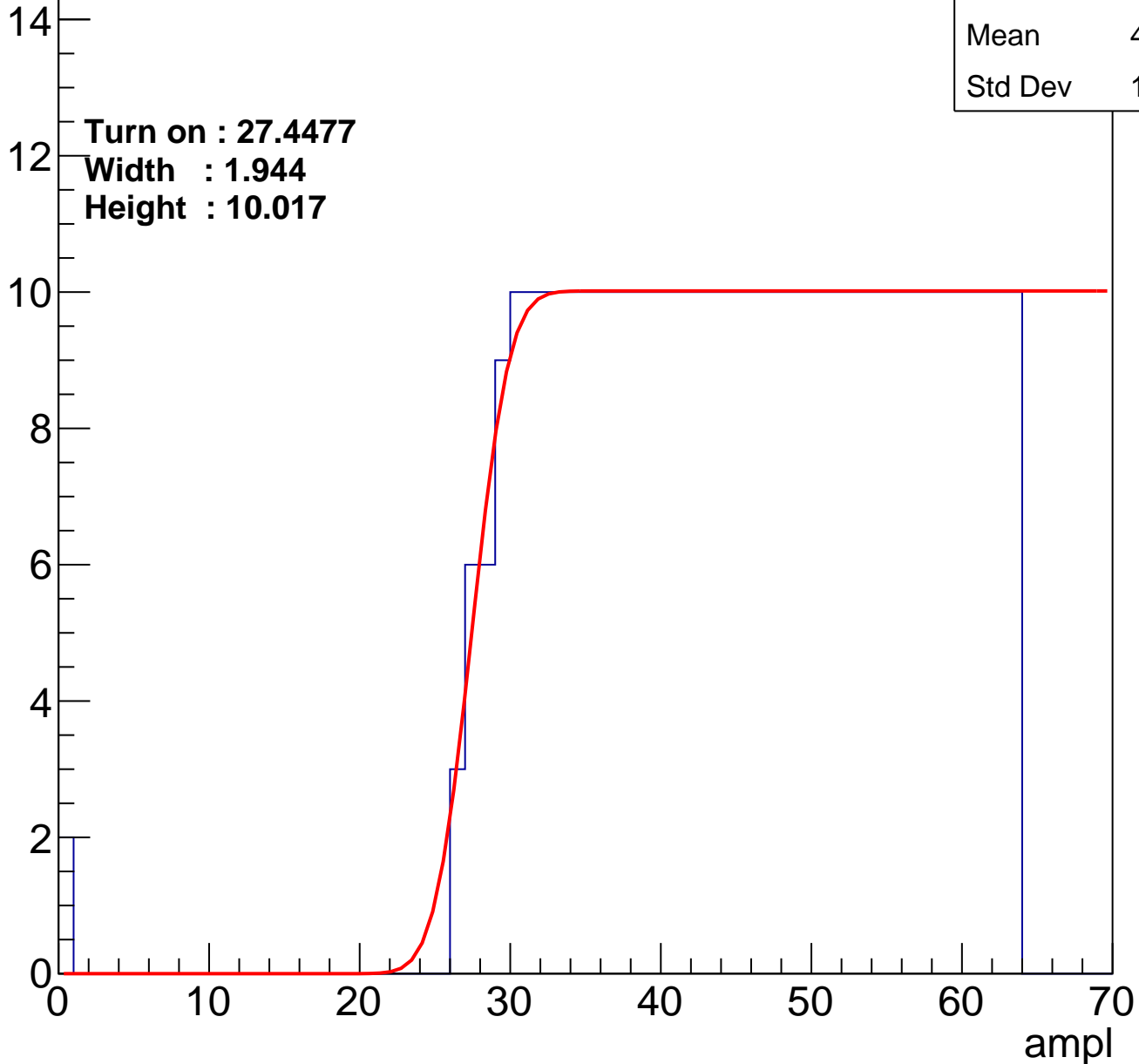
Entries	366
Mean	45.02
Std Dev	11.04

Turn on : 27.4477

Width : 1.944

Height : 10.017

Entry



B1L101S, U11-ch62

calib_packv5_042523_0143.root, FC#0, port D2

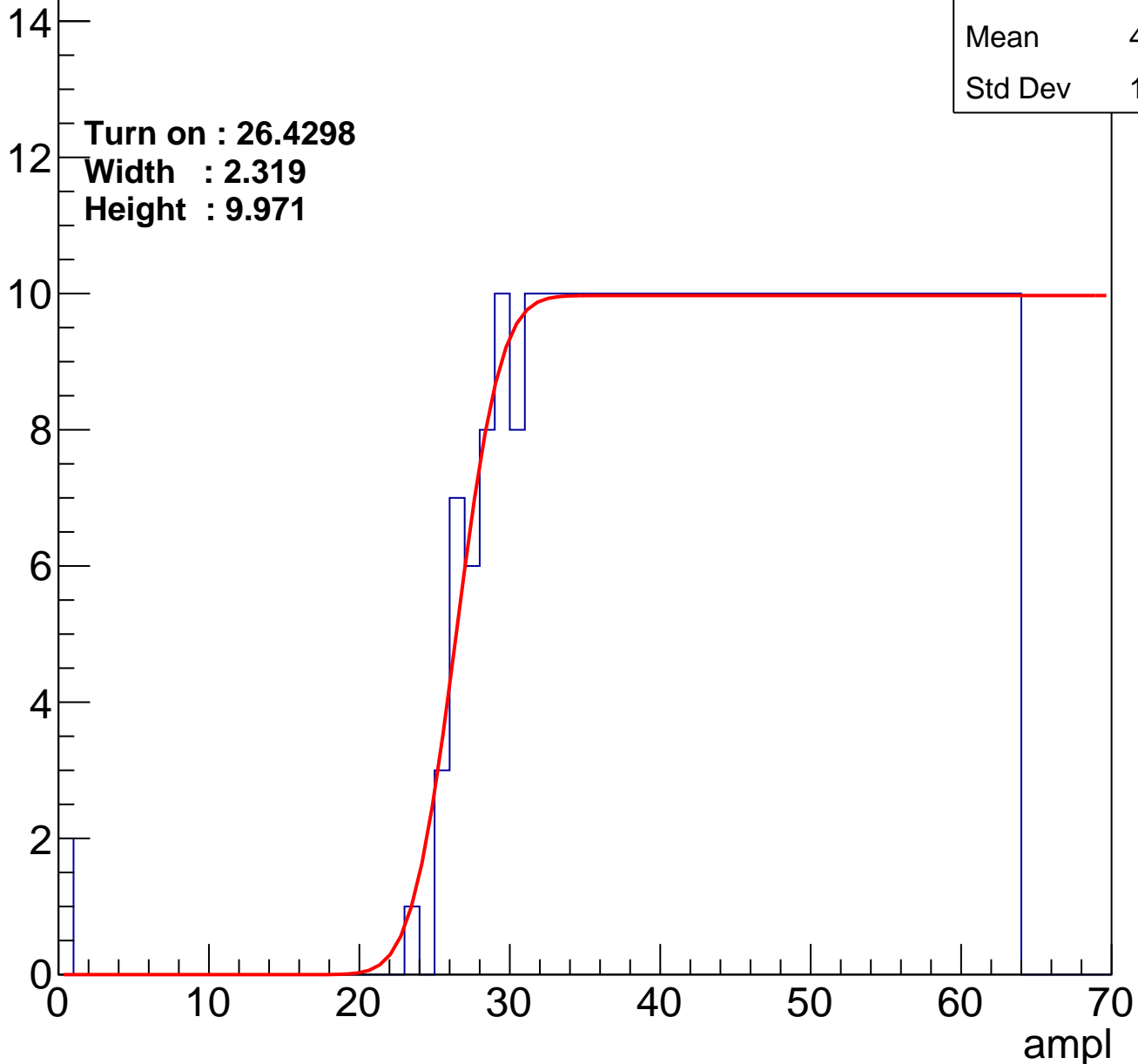
Entries	375
Mean	44.55
Std Dev	11.32

Turn on : 26.4298

Width : 2.319

Height : 9.971

Entry



B1L101S, U11-ch63

calib_packv5_042523_0143.root, FC#0, port D2

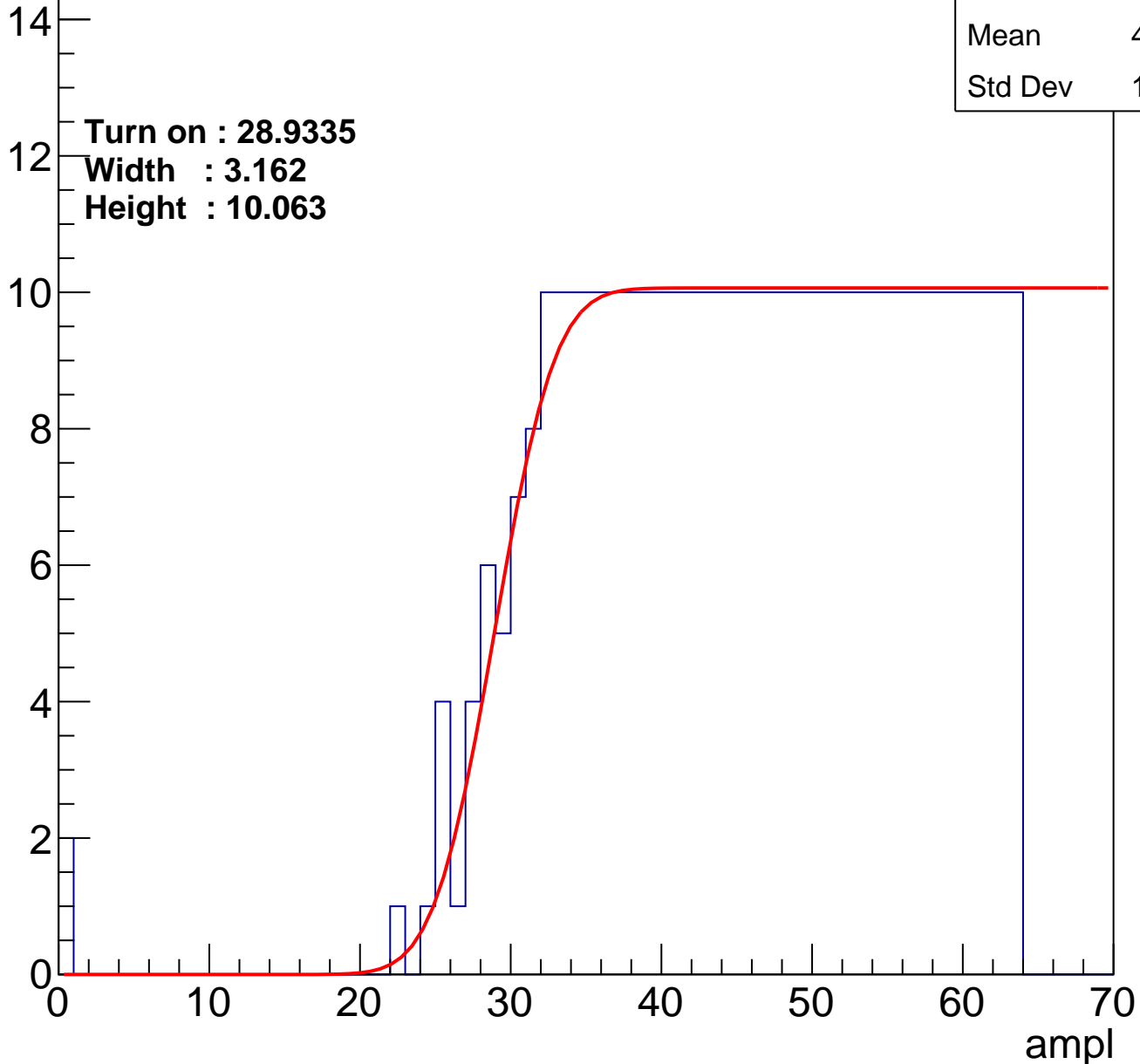
Entries	359
Mean	45.27
Std Dev	11.03

Turn on : 28.9335

Width : 3.162

Height : 10.063

Entry



B1L101S, U11-ch64

calib_packv5_042523_0143.root, FC#0, port D2

Entries	380
Mean	44.24
Std Dev	11.55

Turn on : 26.2121

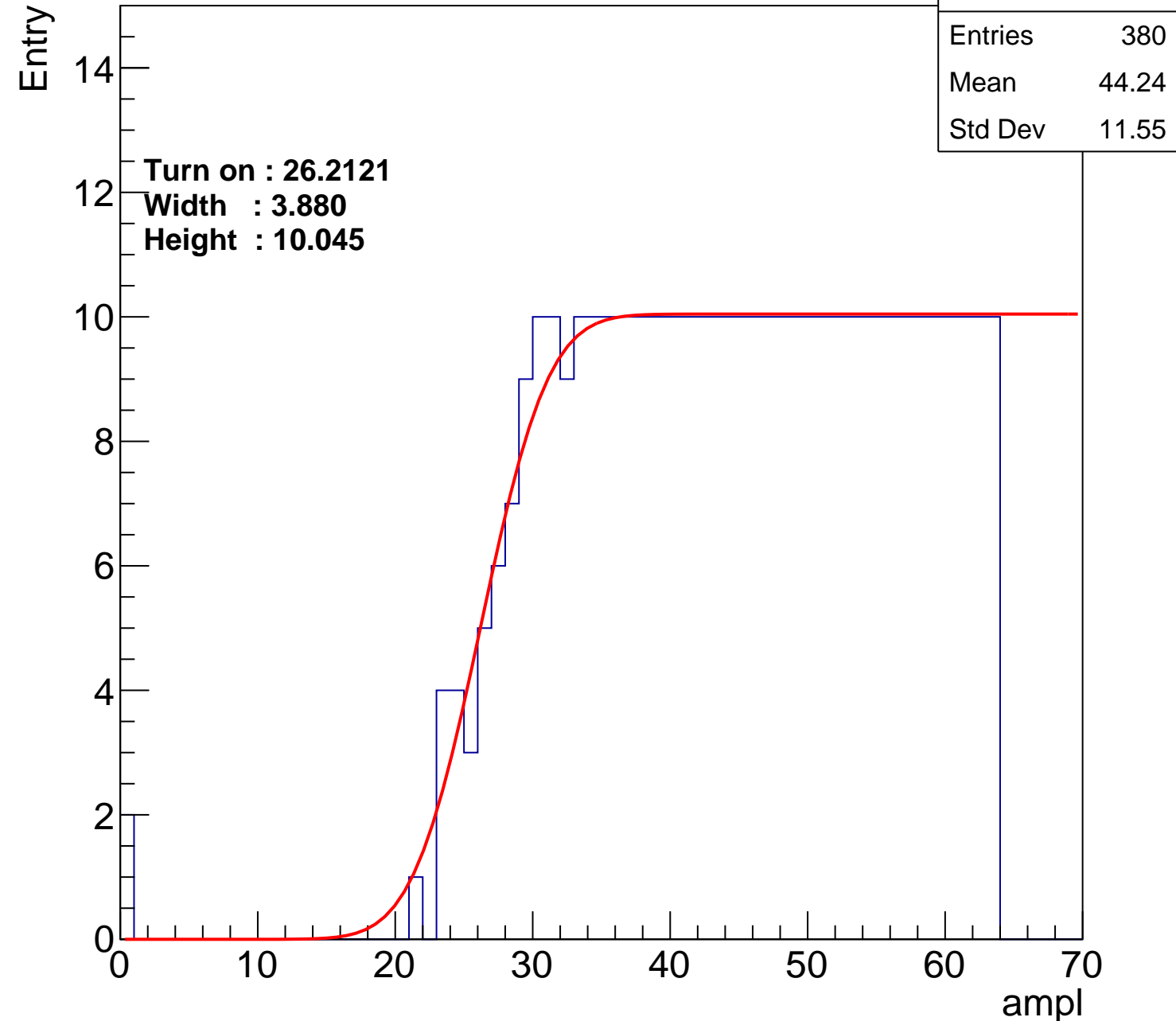
Width : 3.880

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch65

calib_packv5_042523_0143.root, FC#0, port D2

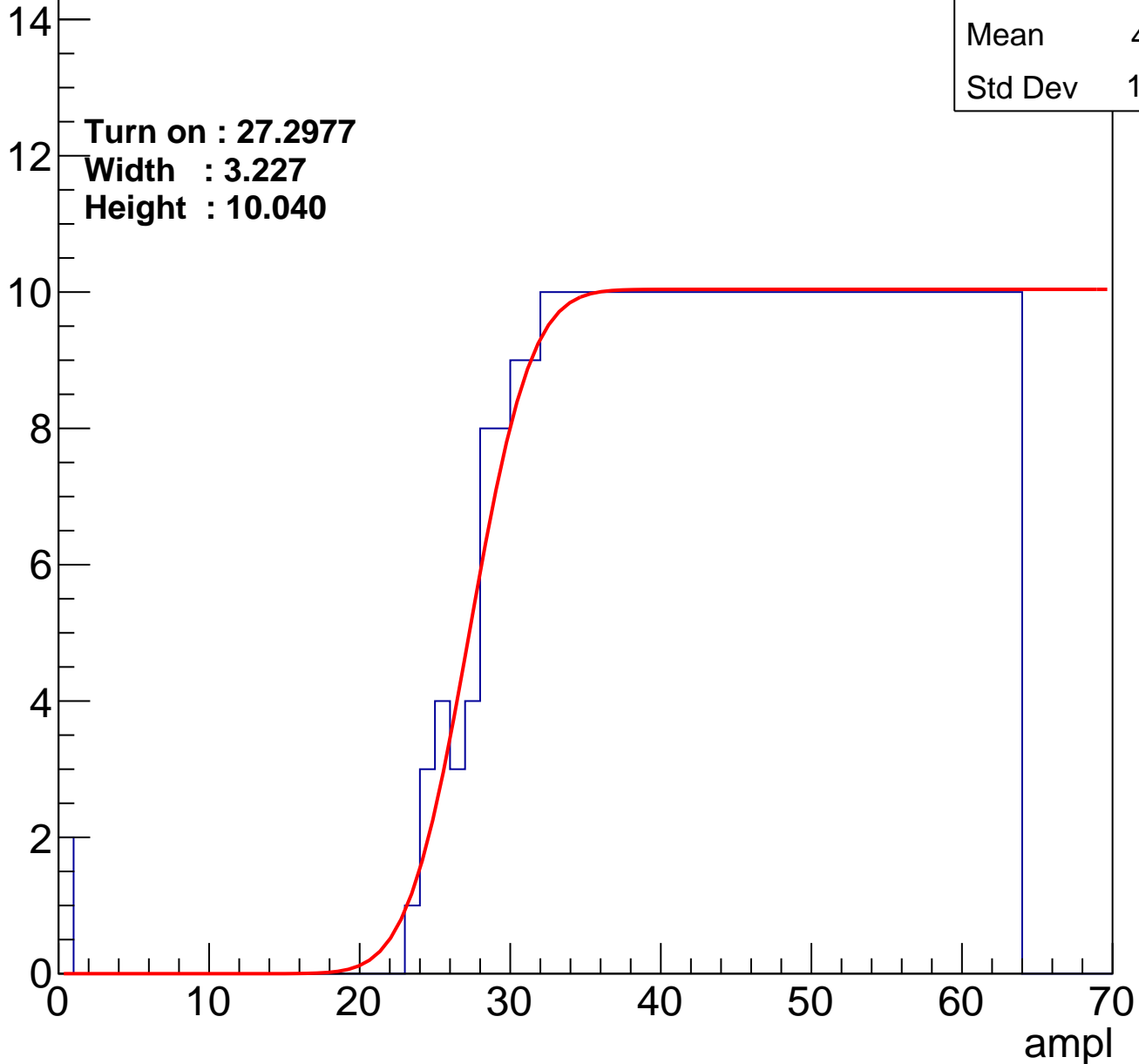
Entries	371
Mean	44.71
Std Dev	11.28

Turn on : 27.2977

Width : 3.227

Height : 10.040

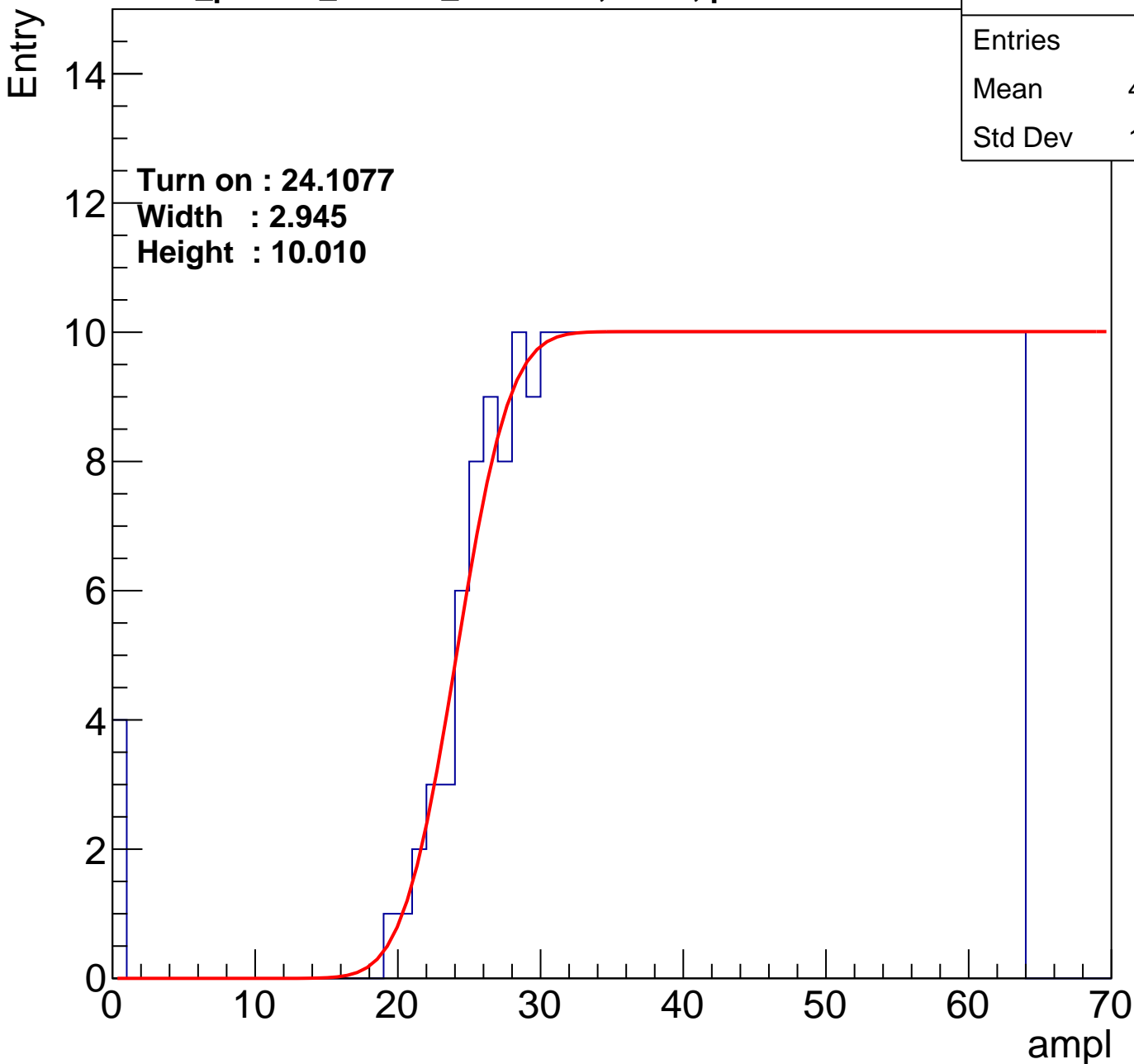
Entry



calib_packv5_042523_0143.root, FC#0, port D2

calib_packv5_042523_0143.root, FC#0, port D2

Turn on : 24.1077
Width : 2.945
Height : 10.010



B1L101S, U11-ch67

calib_packv5_042523_0143.root, FC#0, port D2

Entries	363
Mean	45.1
Std Dev	11.07

Turn on : 27.9101

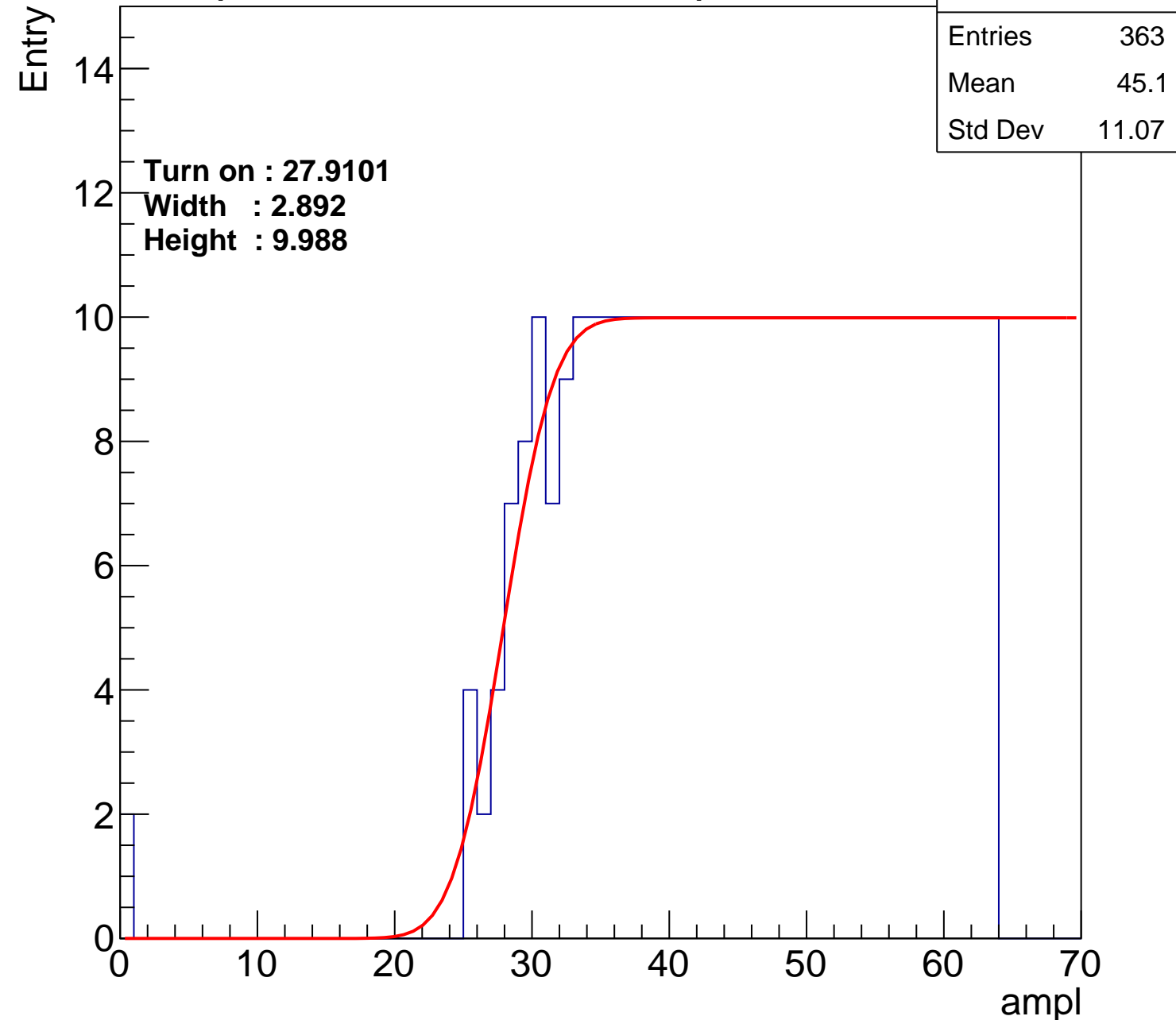
Width : 2.892

Height : 9.988

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch68

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.21
Std Dev	11.89

Turn on : 26.4865

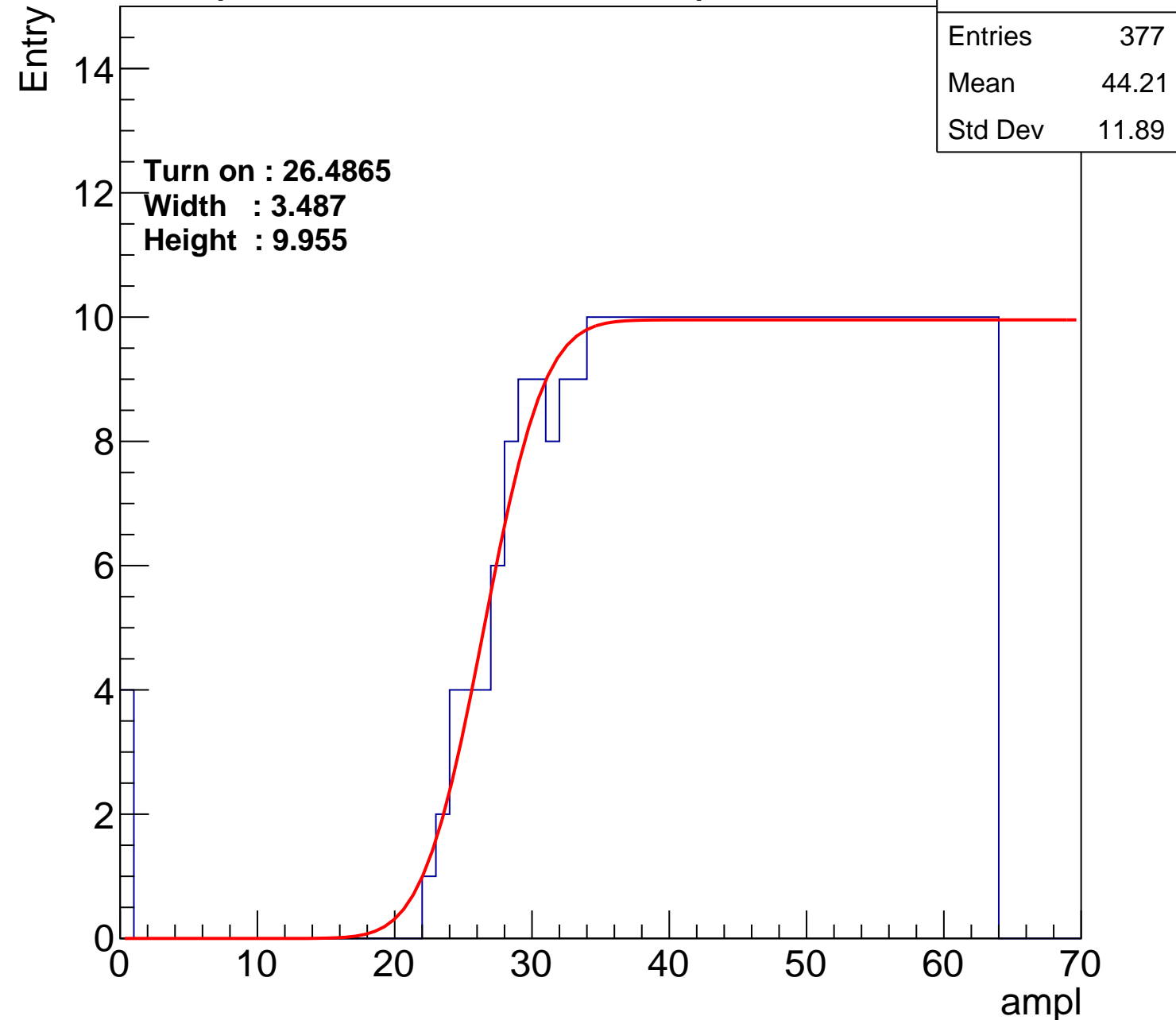
Width : 3.487

Height : 9.955

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch69

calib_packv5_042523_0143.root, FC#0, port D2

Entries	362
Mean	44.89
Std Dev	11.72

Turn on : 28.6406

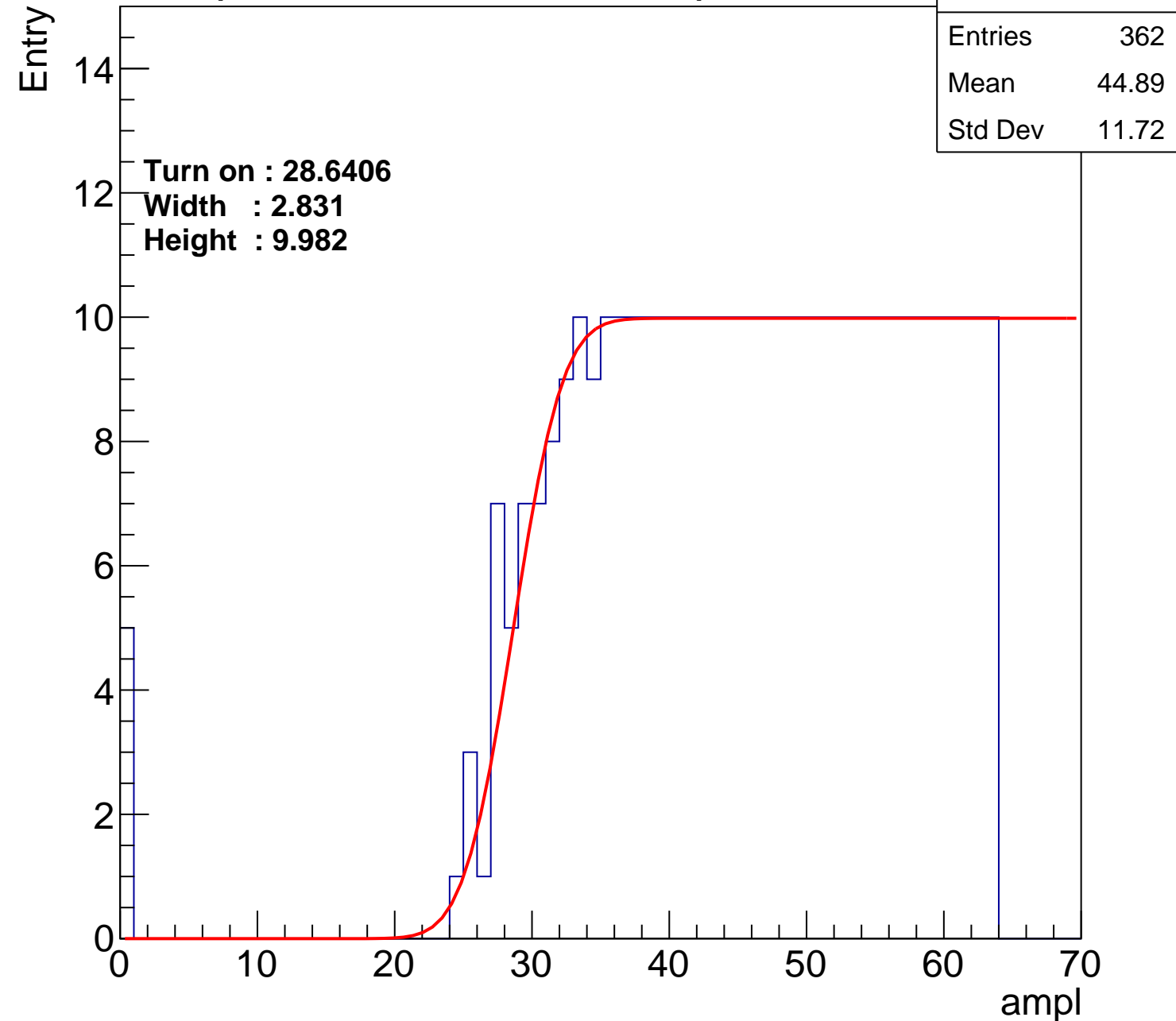
Width : 2.831

Height : 9.982

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch70

calib_packv5_042523_0143.root, FC#0, port D2

Entries	390
Mean	43.7
Std Dev	11.95

Turn on : 25.4000

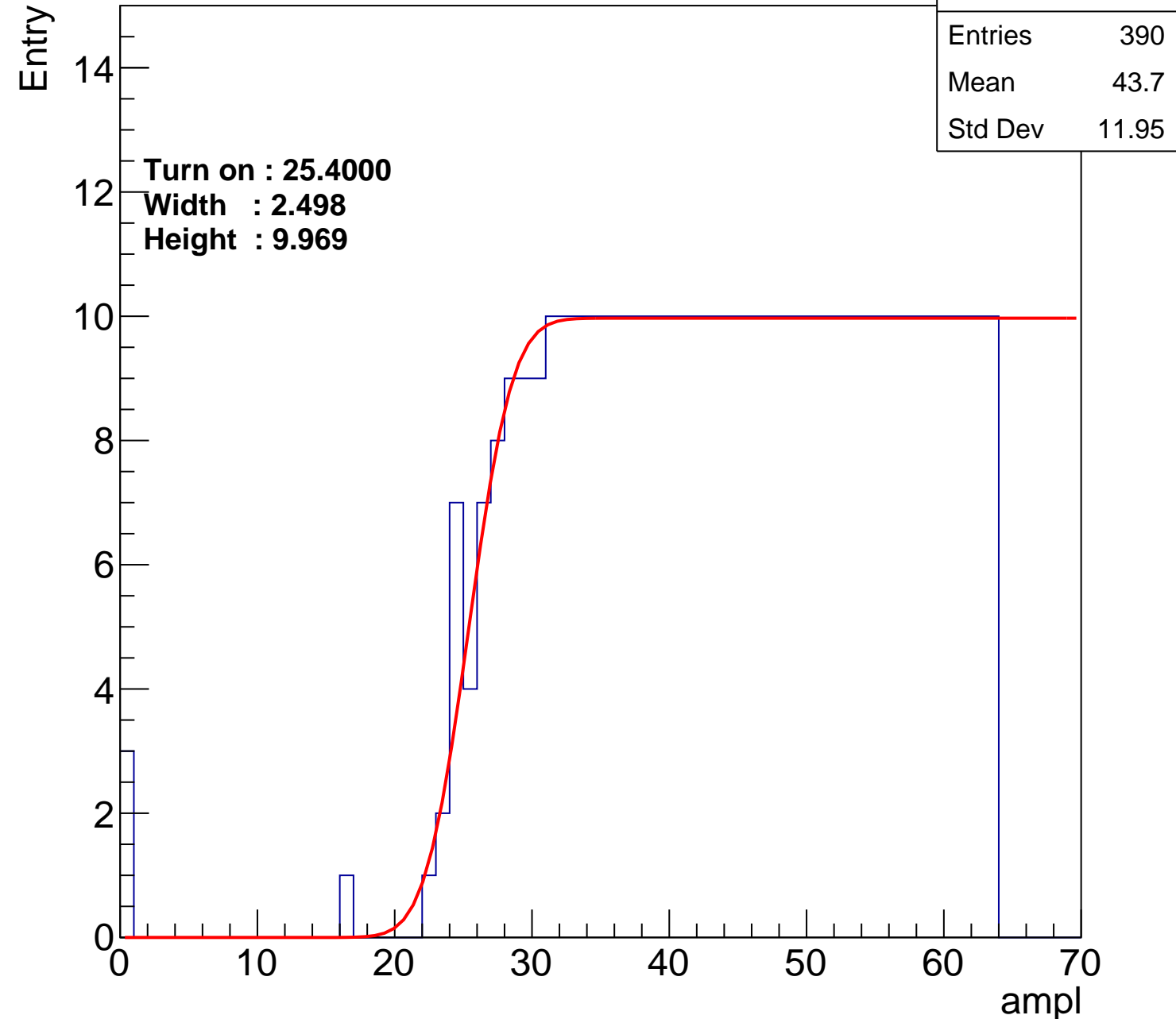
Width : 2.498

Height : 9.969

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch71

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.49
Std Dev	11.55

Turn on : 27.4369

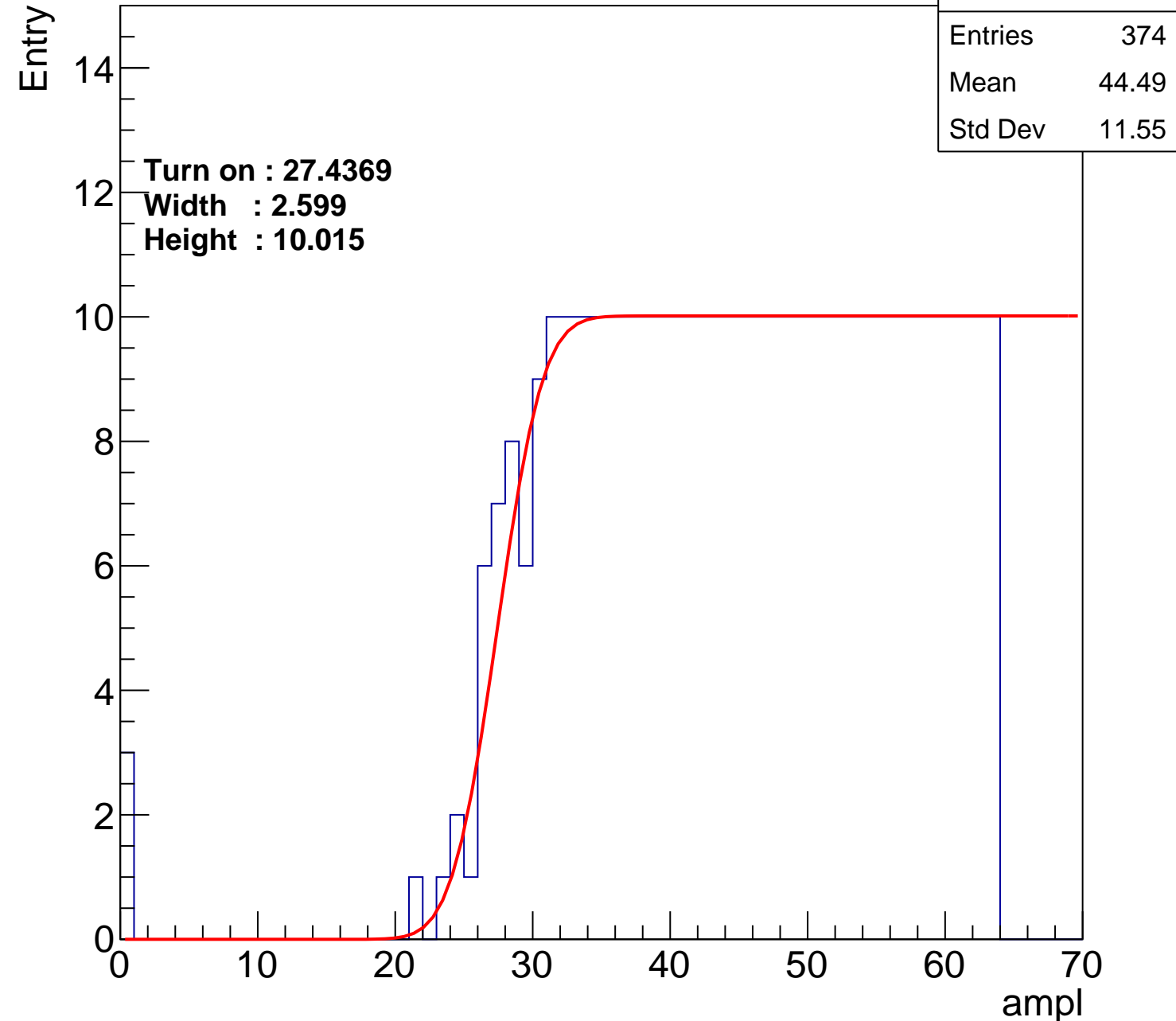
Width : 2.599

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch72

calib_packv5_042523_0143.root, FC#0, port D2

Entries	383
Mean	43.96
Std Dev	11.98

Turn on : 26.2654

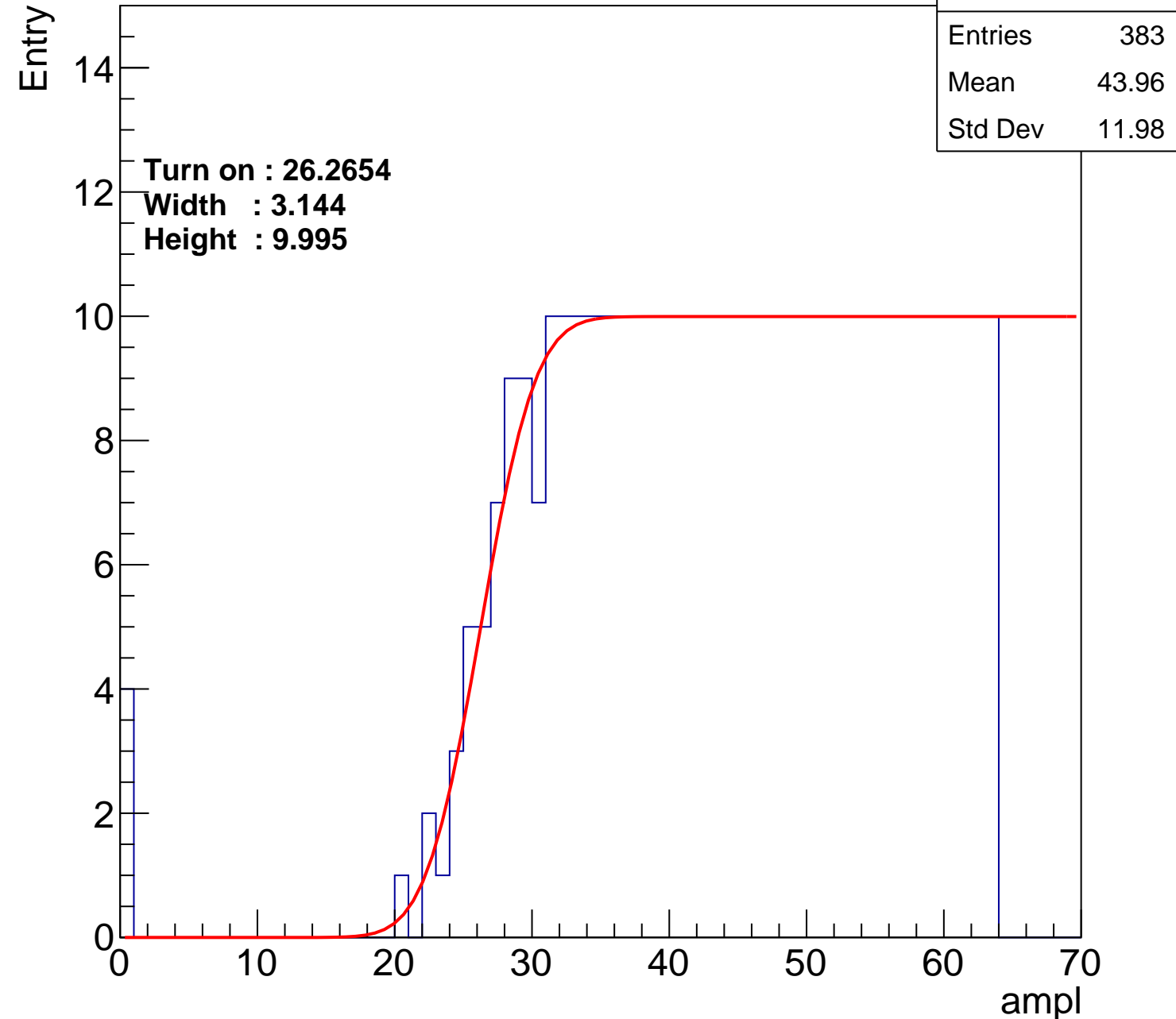
Width : 3.144

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch73

calib_packv5_042523_0143.root, FC#0, port D2

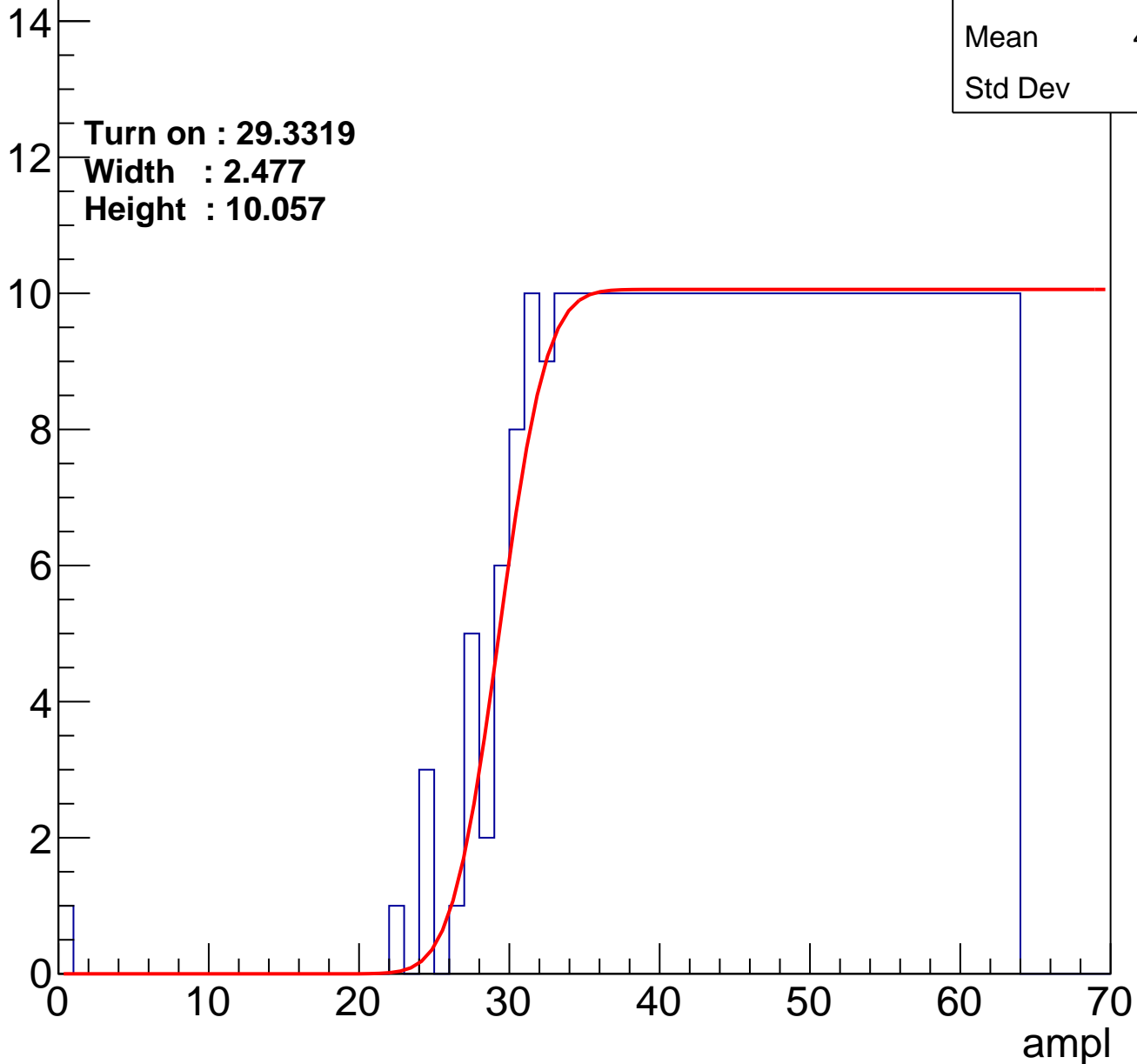
Entries	356
Mean	45.51
Std Dev	10.7

Turn on : 29.3319

Width : 2.477

Height : 10.057

Entry



B1L101S, U11-ch74

calib_packv5_042523_0143.root, FC#0, port D2

Entries	380
Mean	44.07
Std Dev	12.04

Turn on : 26.6527

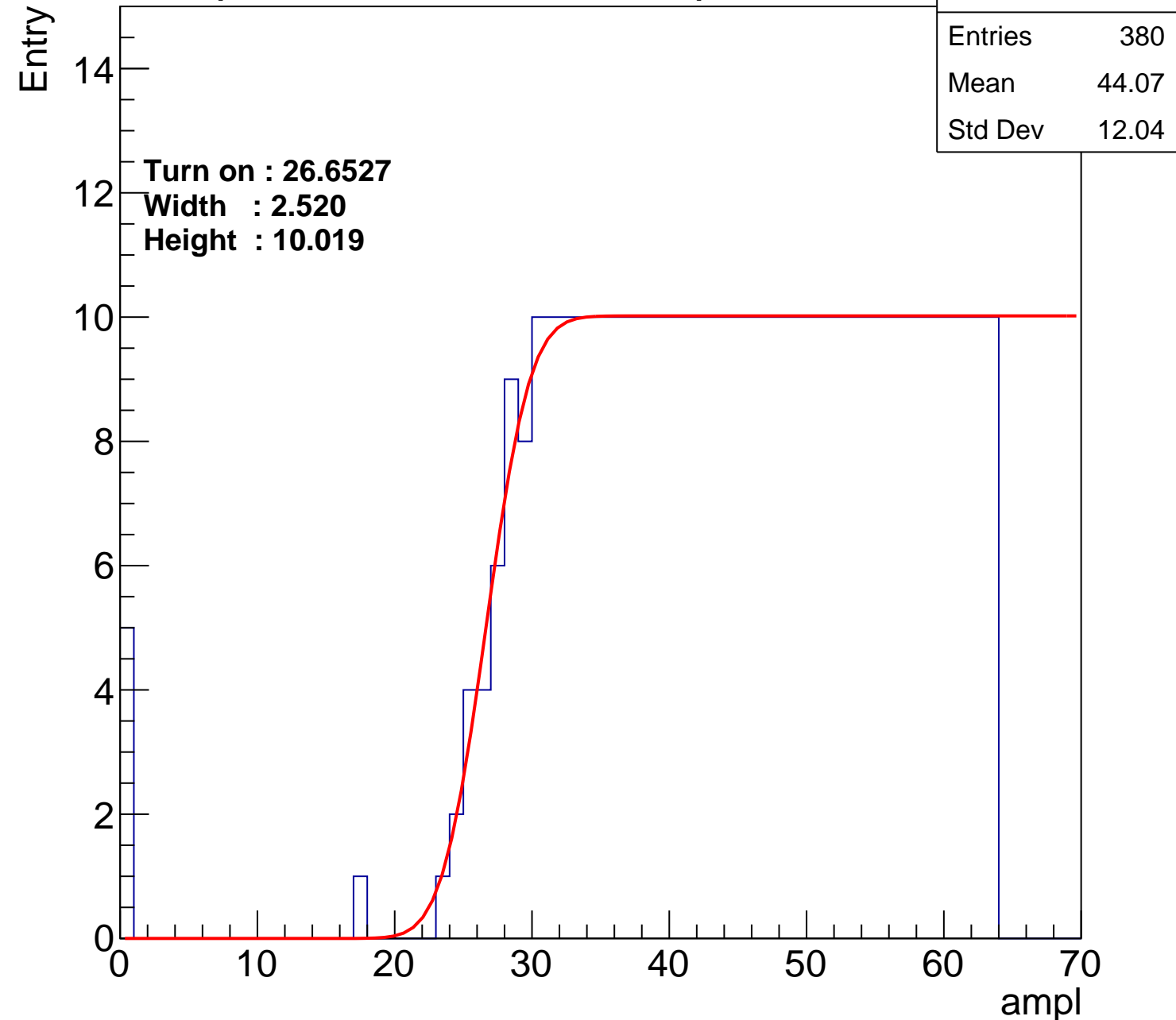
Width : 2.520

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch75

calib_packv5_042523_0143.root, FC#0, port D2

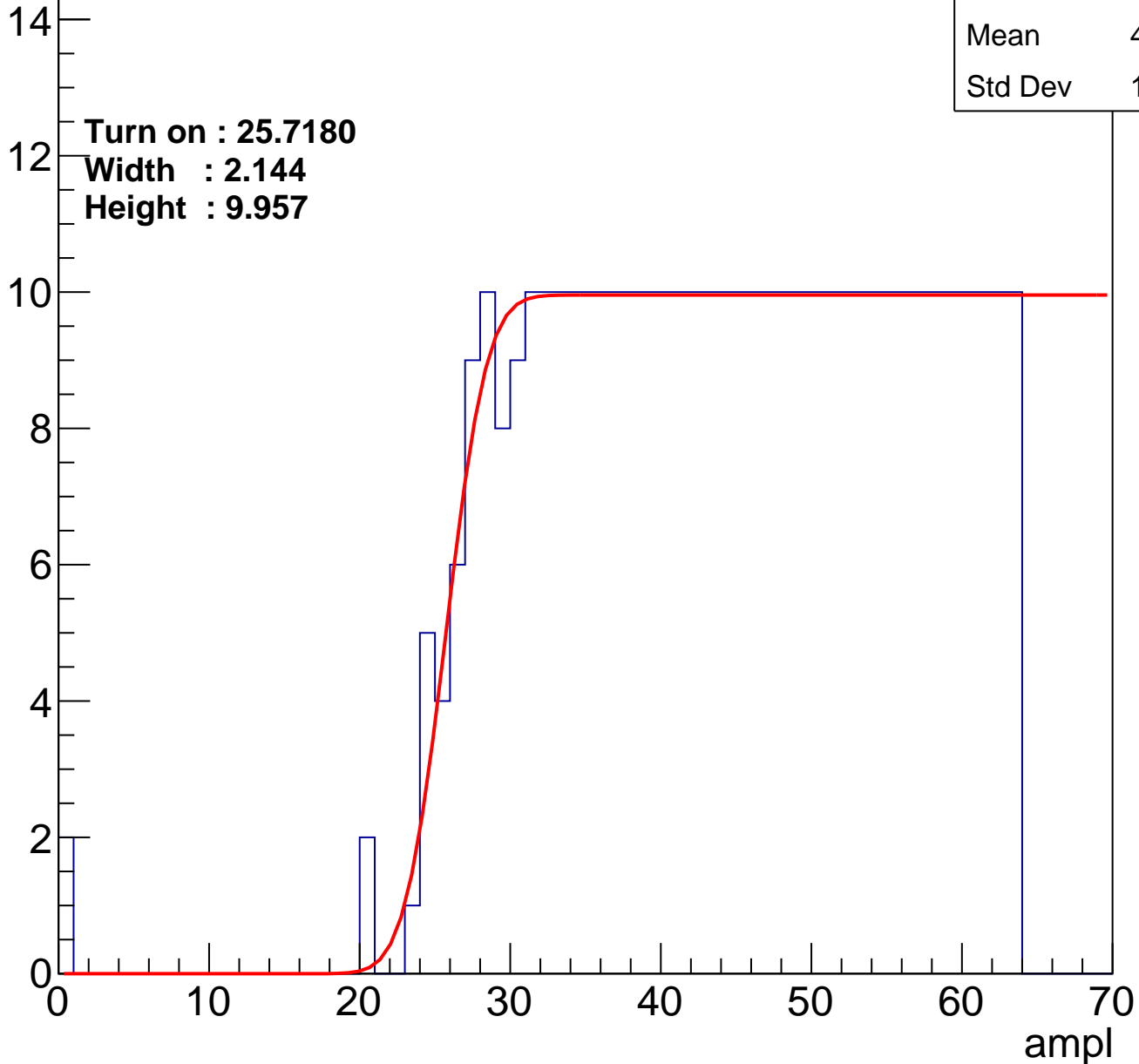
Entries	386
Mean	43.97
Std Dev	11.66

Turn on : 25.7180

Width : 2.144

Height : 9.957

Entry



B1L101S, U11-ch76

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.54
Std Dev	11.2

Turn on : 26.6286

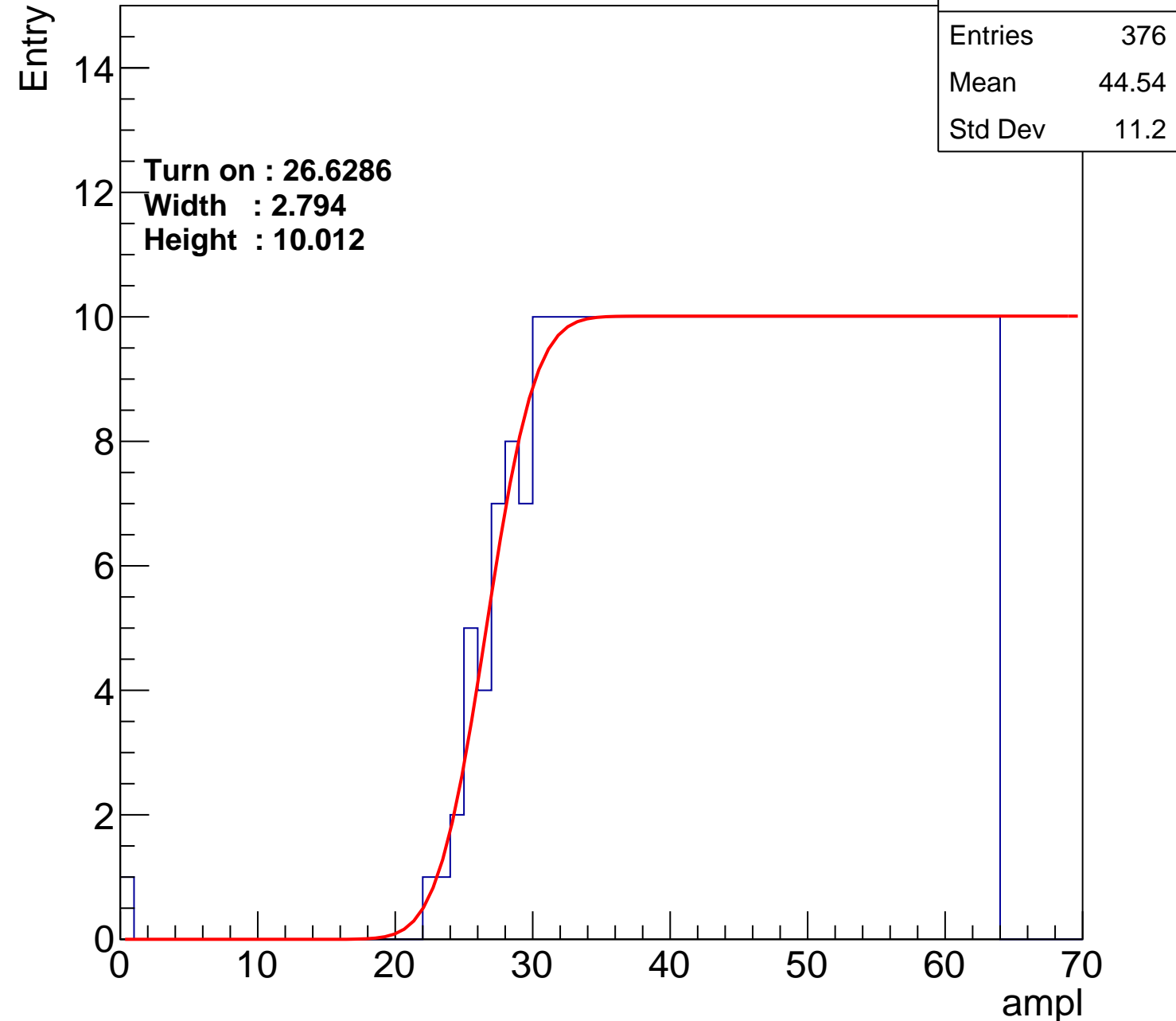
Width : 2.794

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch77

calib_packv5_042523_0143.root, FC#0, port D2

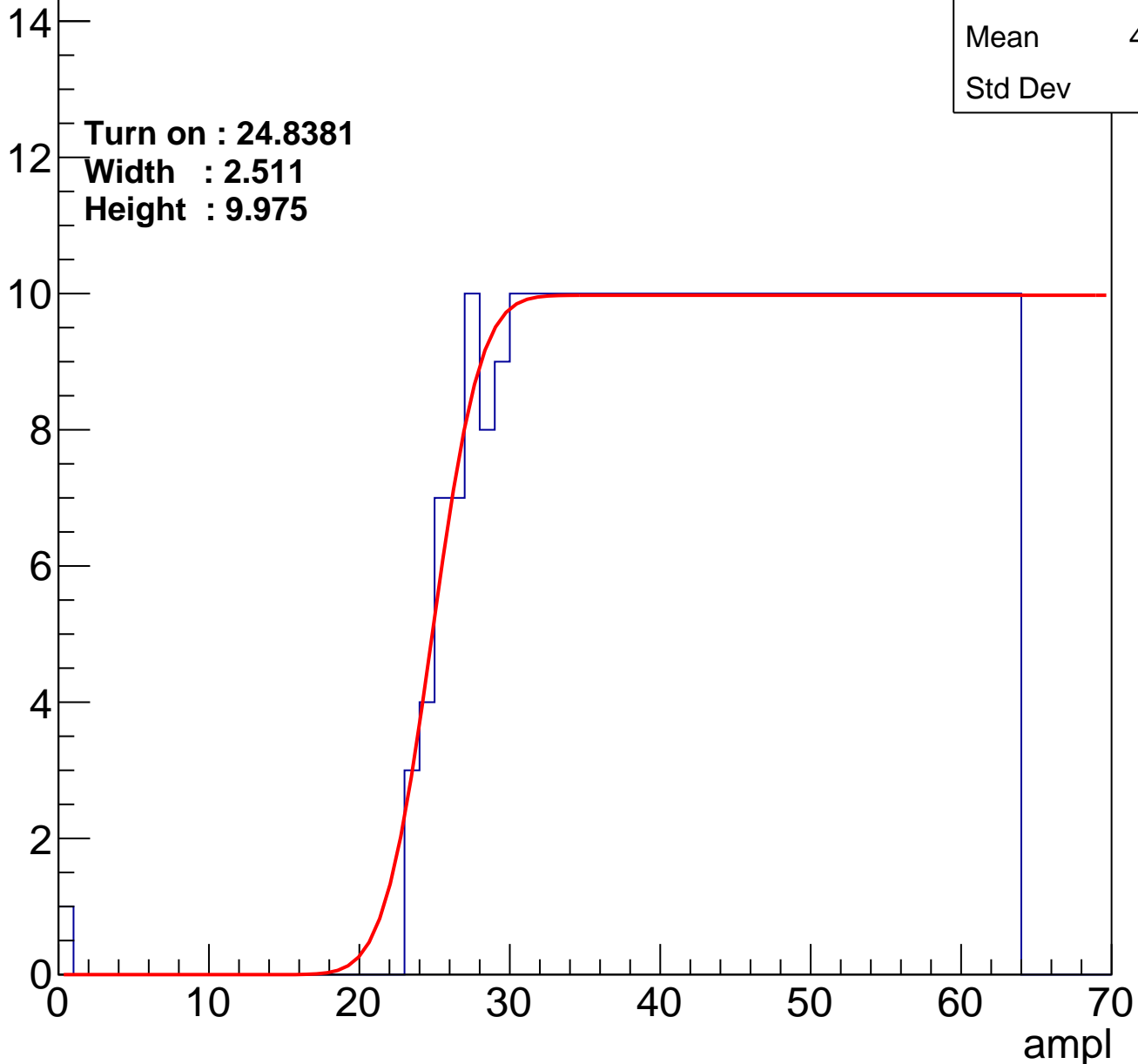
Entries	389
Mean	43.93
Std Dev	11.5

Turn on : 24.8381

Width : 2.511

Height : 9.975

Entry



B1L101S, U11-ch78

calib_packv5_042523_0143.root, FC#0, port D2

Entries	364
Mean	44.99
Std Dev	11.19

Turn on : 27.0954

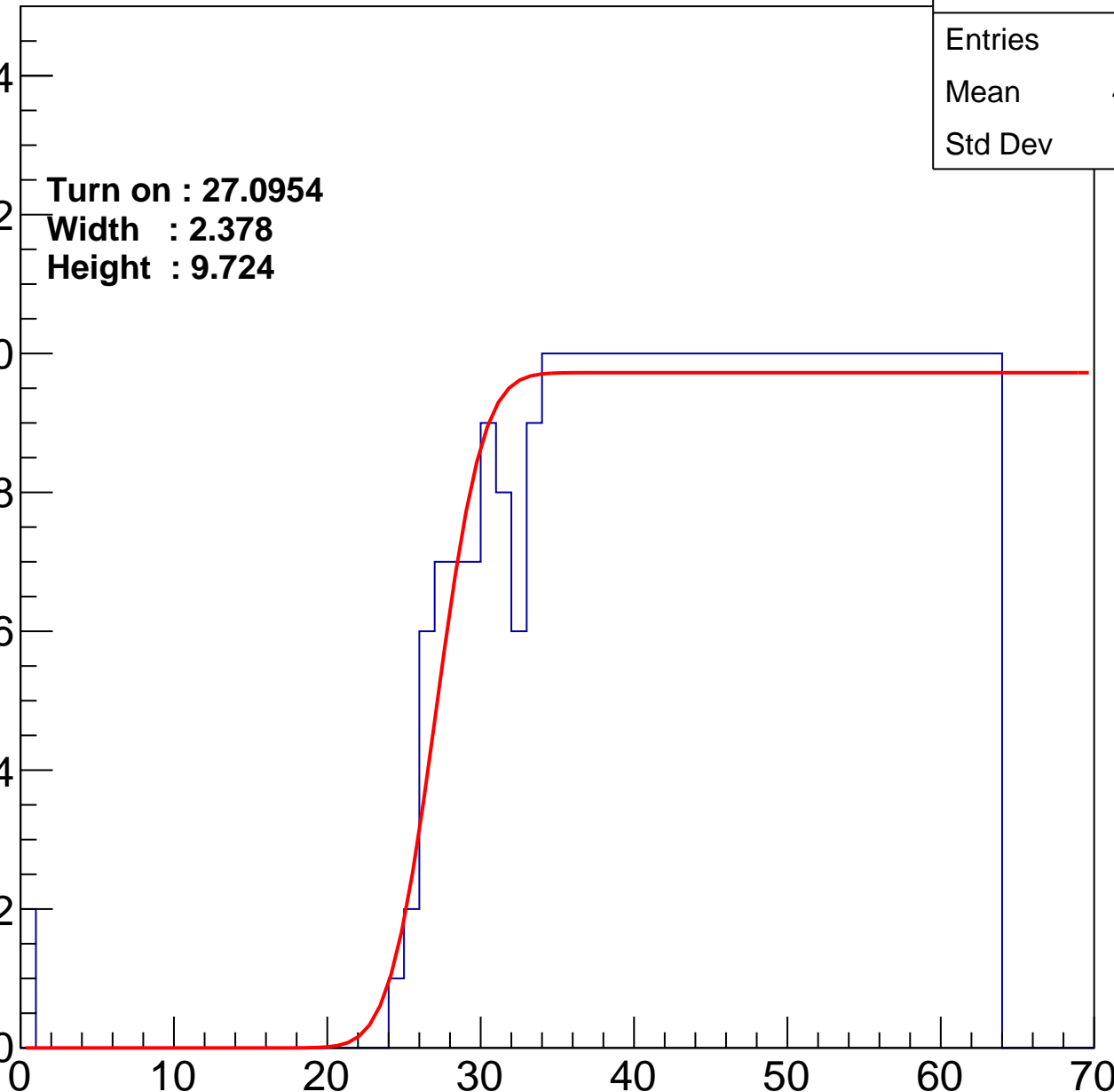
Width : 2.378

Height : 9.724

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch79

calib_packv5_042523_0143.root, FC#0, port D2

Entries	368
Mean	44.72
Std Dev	11.59

Turn on : 29.6712

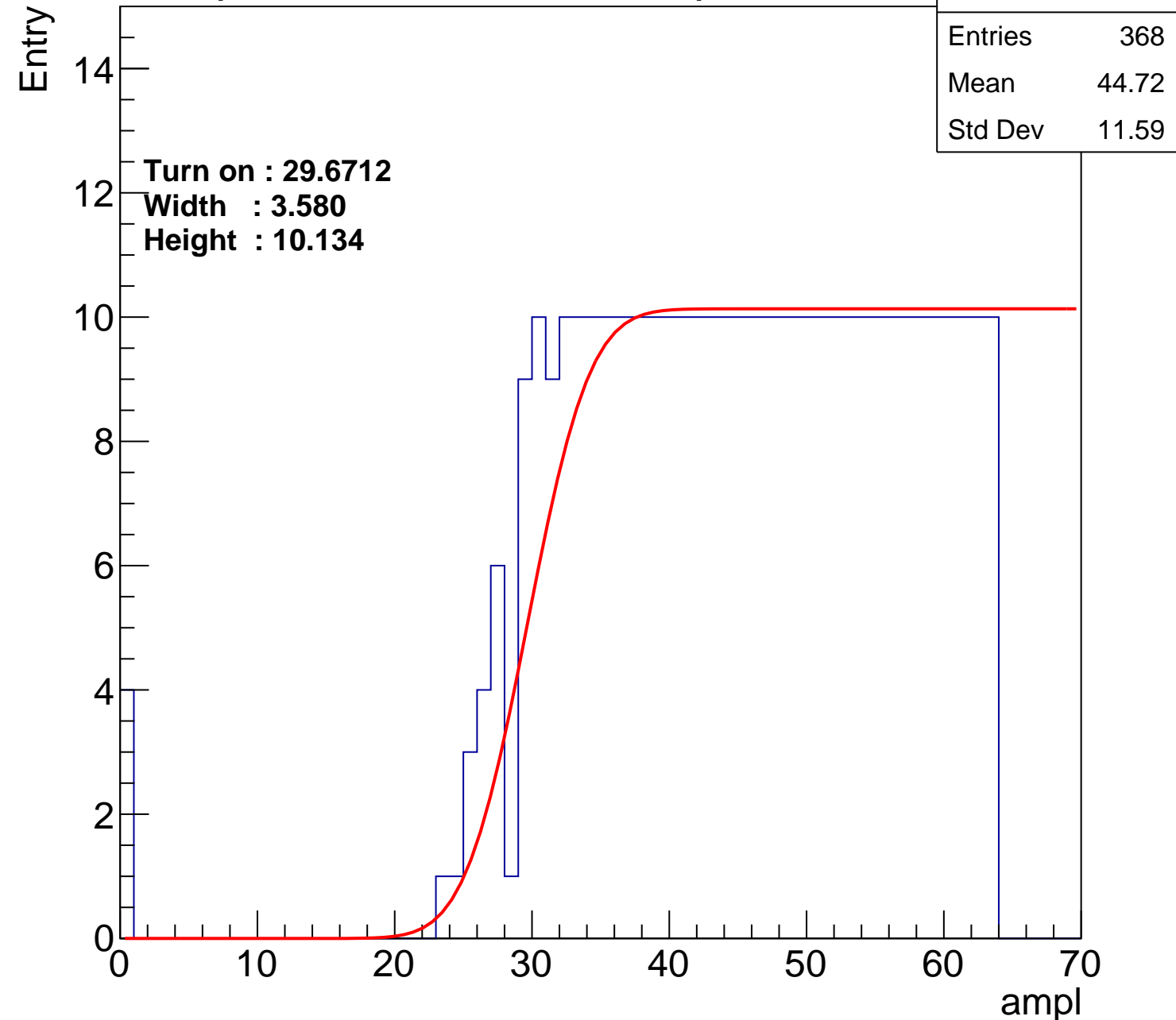
Width : 3.580

Height : 10.134

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch80

calib_packv5_042523_0143.root, FC#0, port D2

Entries	386
Mean	44.04
Std Dev	11.48

Turn on : 26.0144

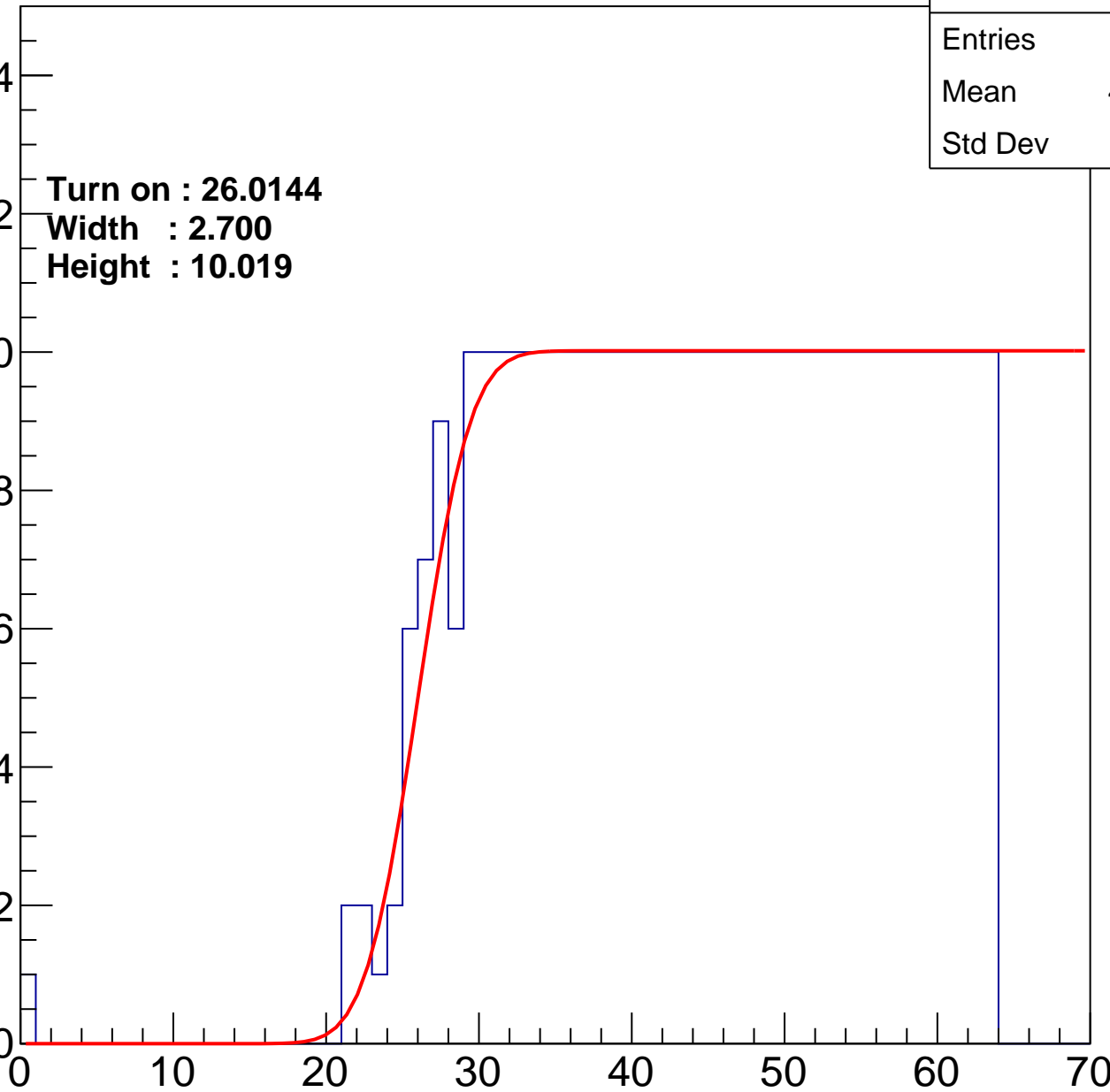
Width : 2.700

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch81

calib_packv5_042523_0143.root, FC#0, port D2

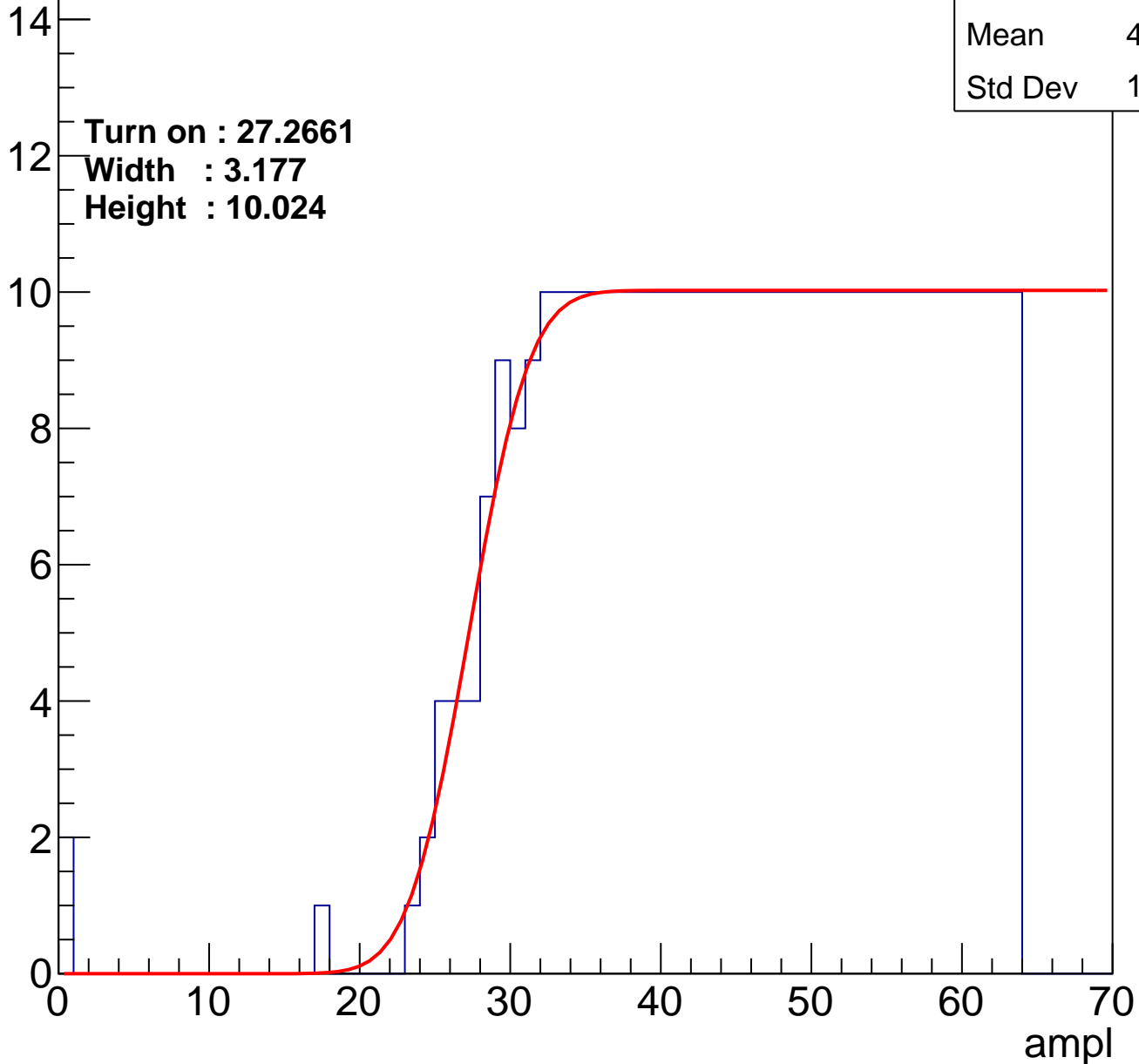
Entries	371
Mean	44.68
Std Dev	11.34

Turn on : 27.2661

Width : 3.177

Height : 10.024

Entry



B1L101S, U11-ch82

calib_packv5_042523_0143.root, FC#0, port D2

Entries	380
Mean	44.21
Std Dev	11.67

Turn on : 26.1138

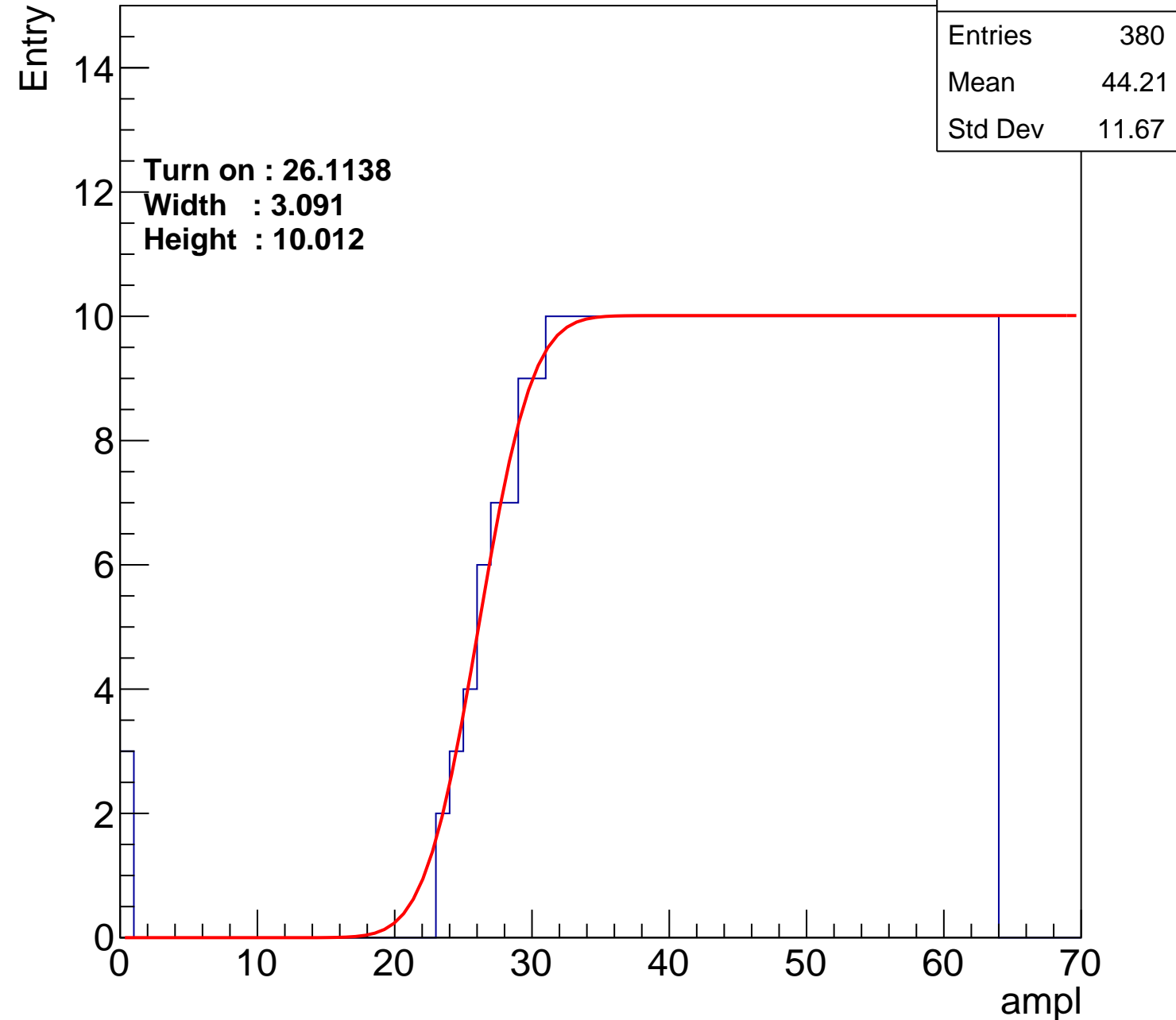
Width : 3.091

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch83

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.43
Std Dev	11.55

Turn on : 26.9872

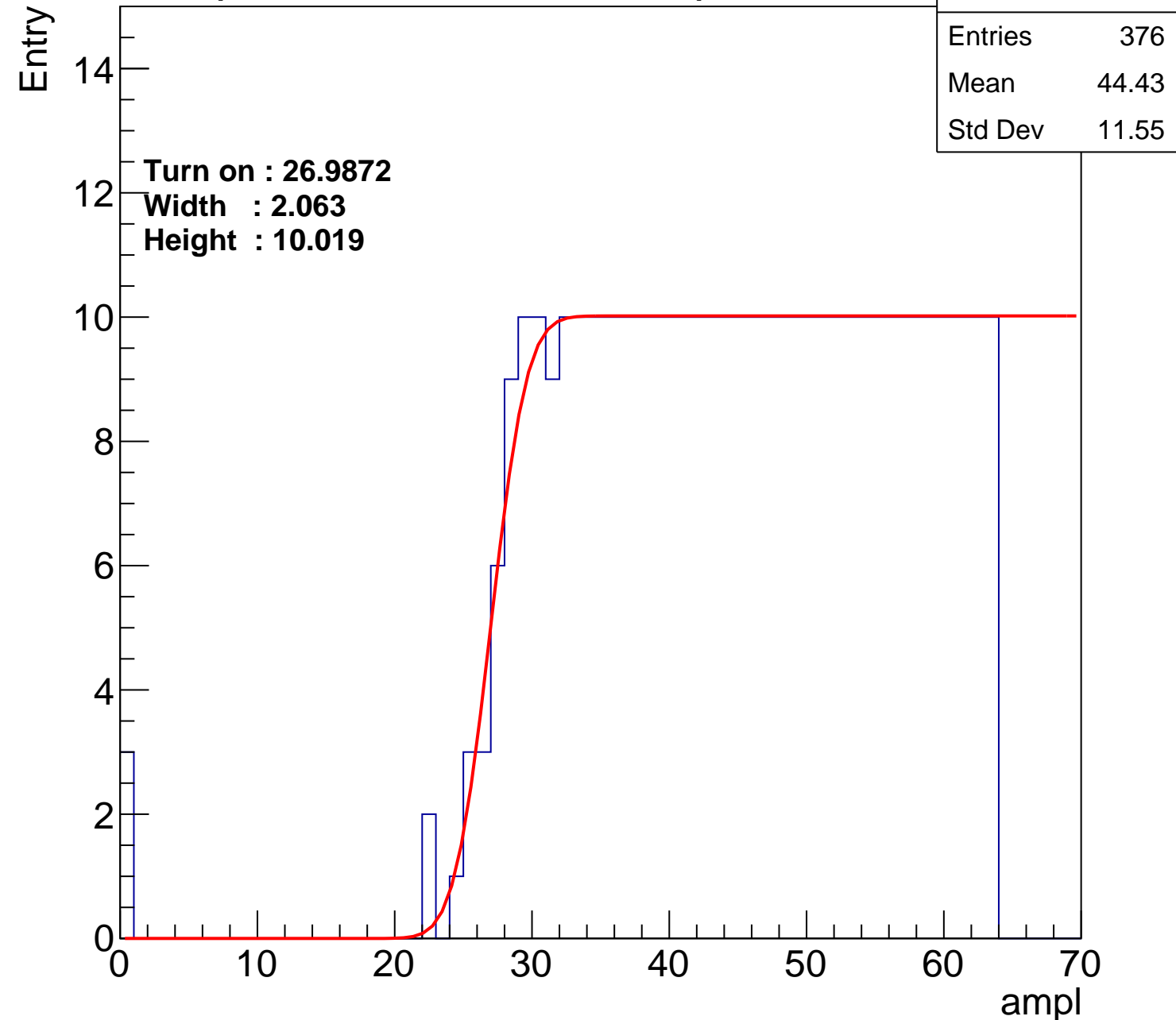
Width : 2.063

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch84

calib_packv5_042523_0143.root, FC#0, port D2

Entries	370
Mean	44.84
Std Dev	11.04

Turn on : 27.4610

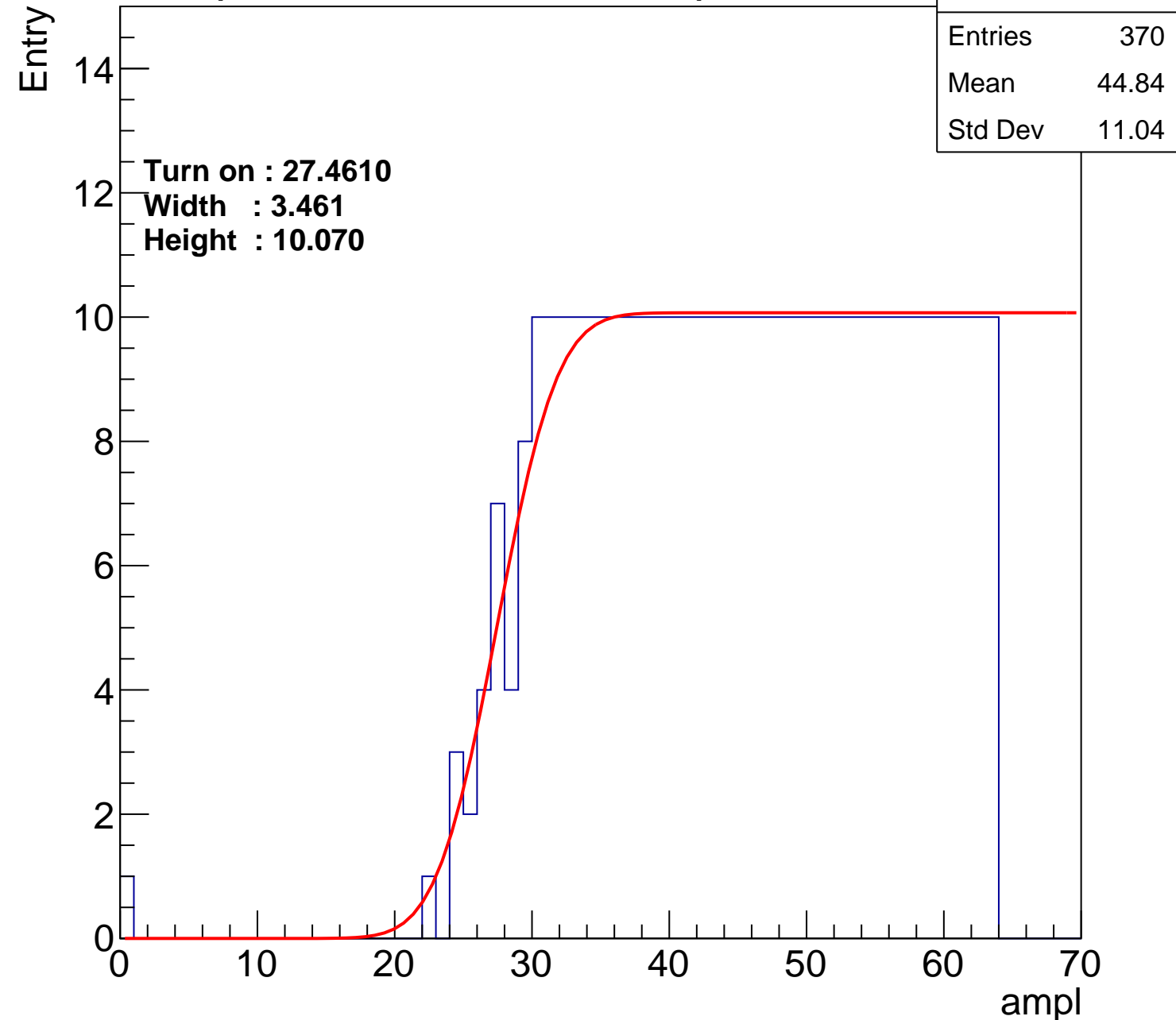
Width : 3.461

Height : 10.070

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch85

calib_packv5_042523_0143.root, FC#0, port D2

Entries	380
Mean	44.33
Std Dev	11.33

Turn on : 26.0374

Width : 3.698

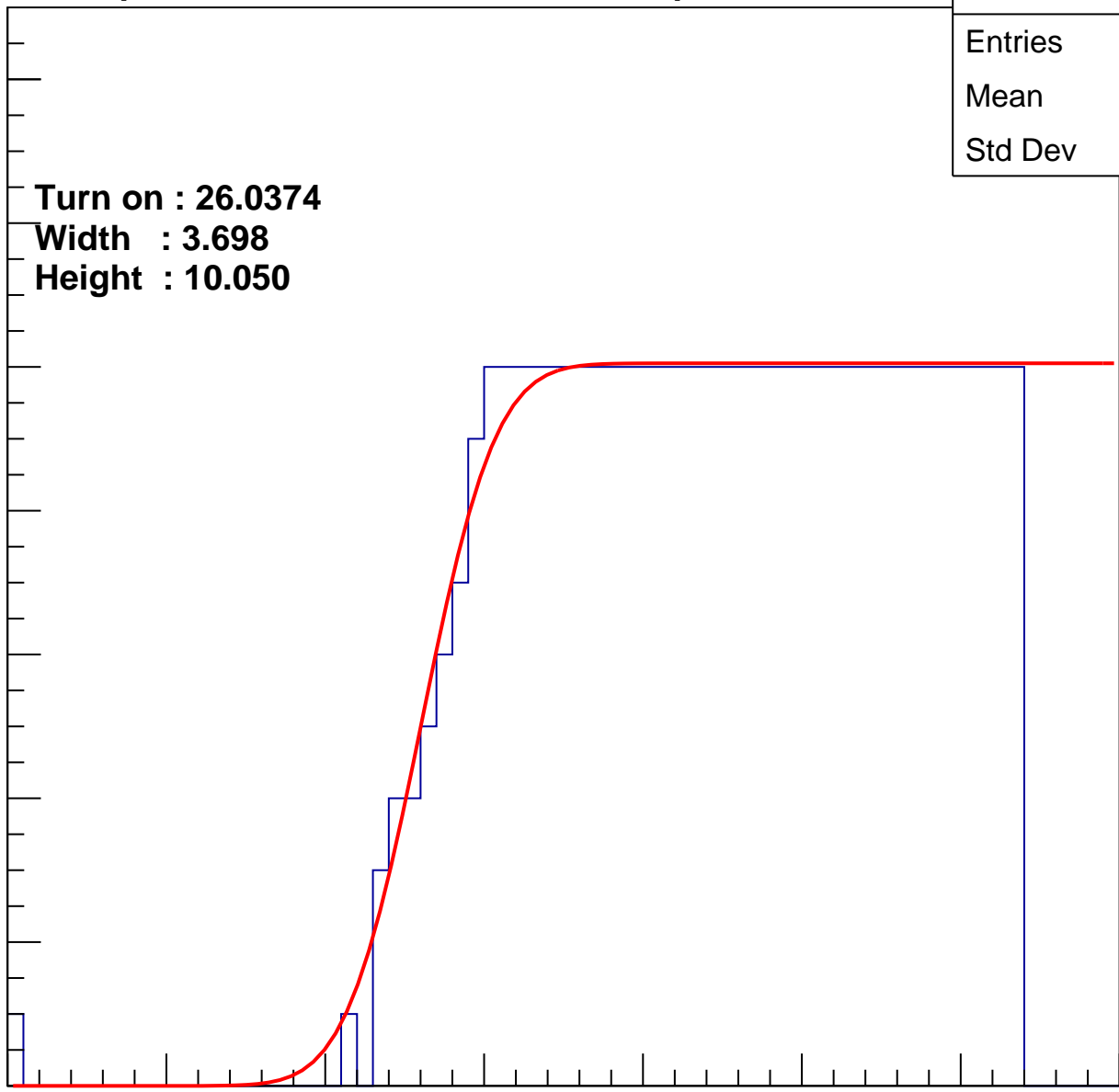
Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L101S, U11-ch86

calib_packv5_042523_0143.root, FC#0, port D2

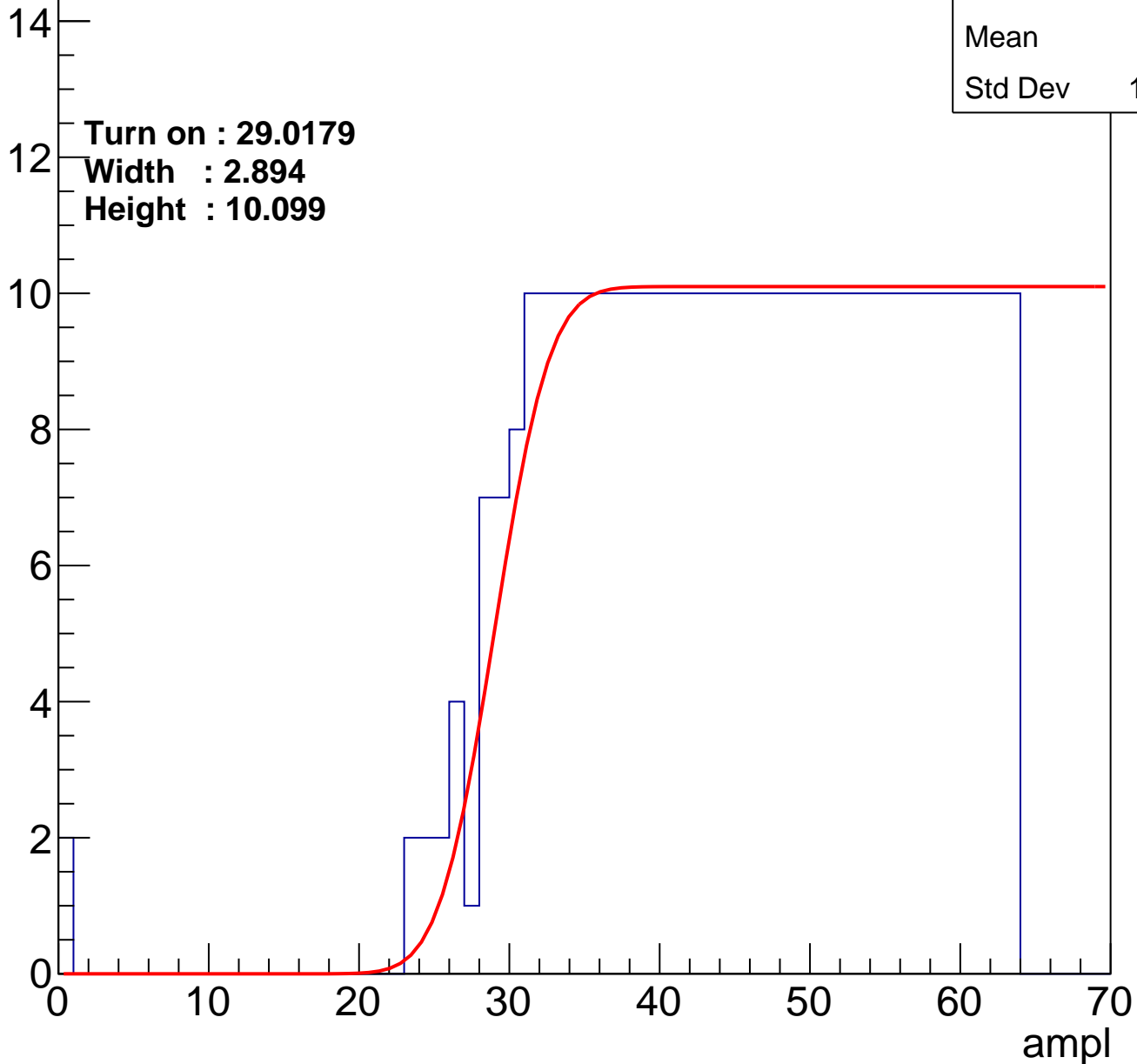
Entries	365
Mean	45
Std Dev	11.14

Turn on : 29.0179

Width : 2.894

Height : 10.099

Entry



B1L101S, U11-ch87

calib_packv5_042523_0143.root, FC#0, port D2

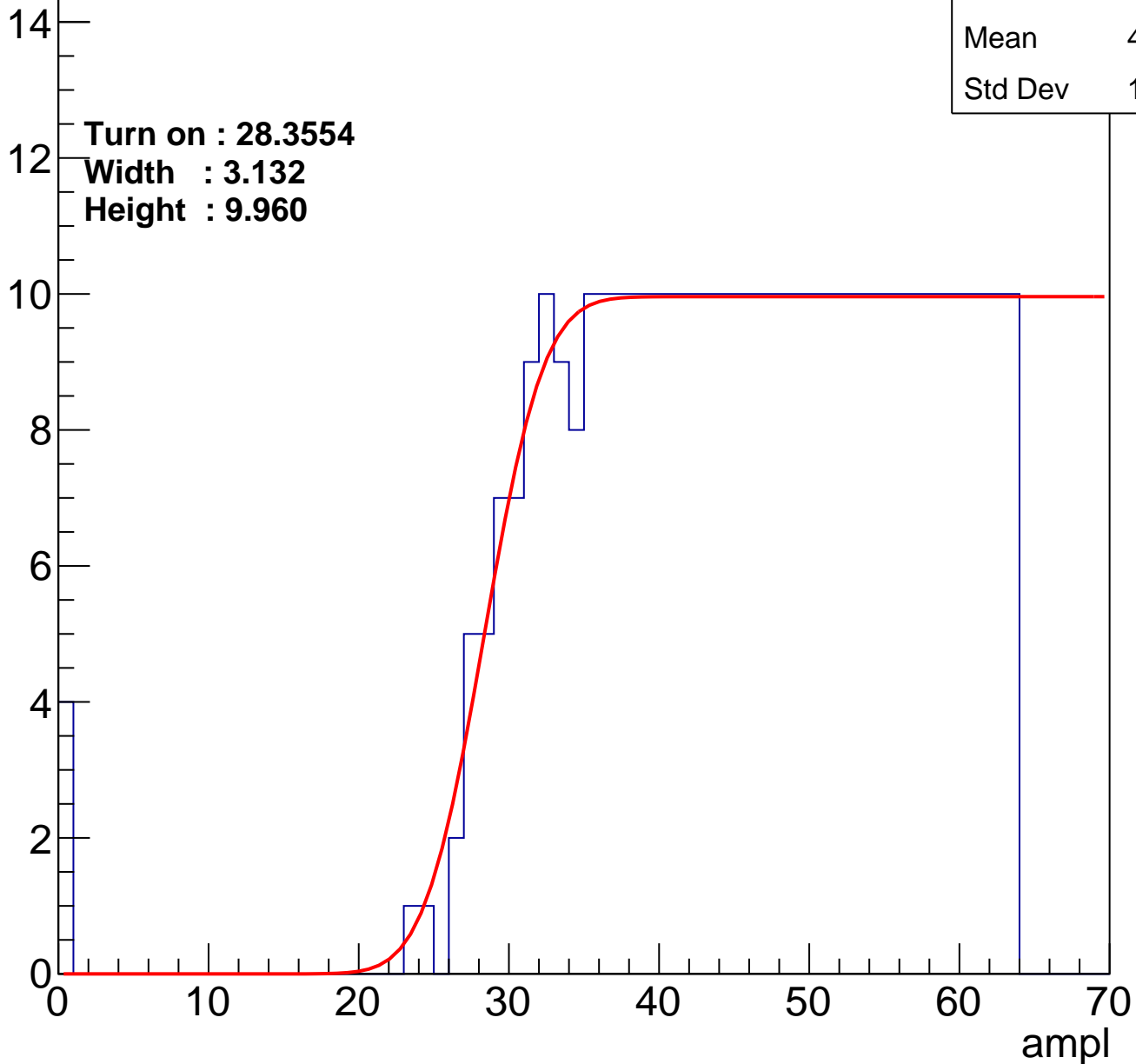
Entry

Entries	358
Mean	45.15
Std Dev	11.44

Turn on : 28.3554

Width : 3.132

Height : 9.960



B1L101S, U11-ch88

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.42
Std Dev	11.43

Turn on : 26.8047

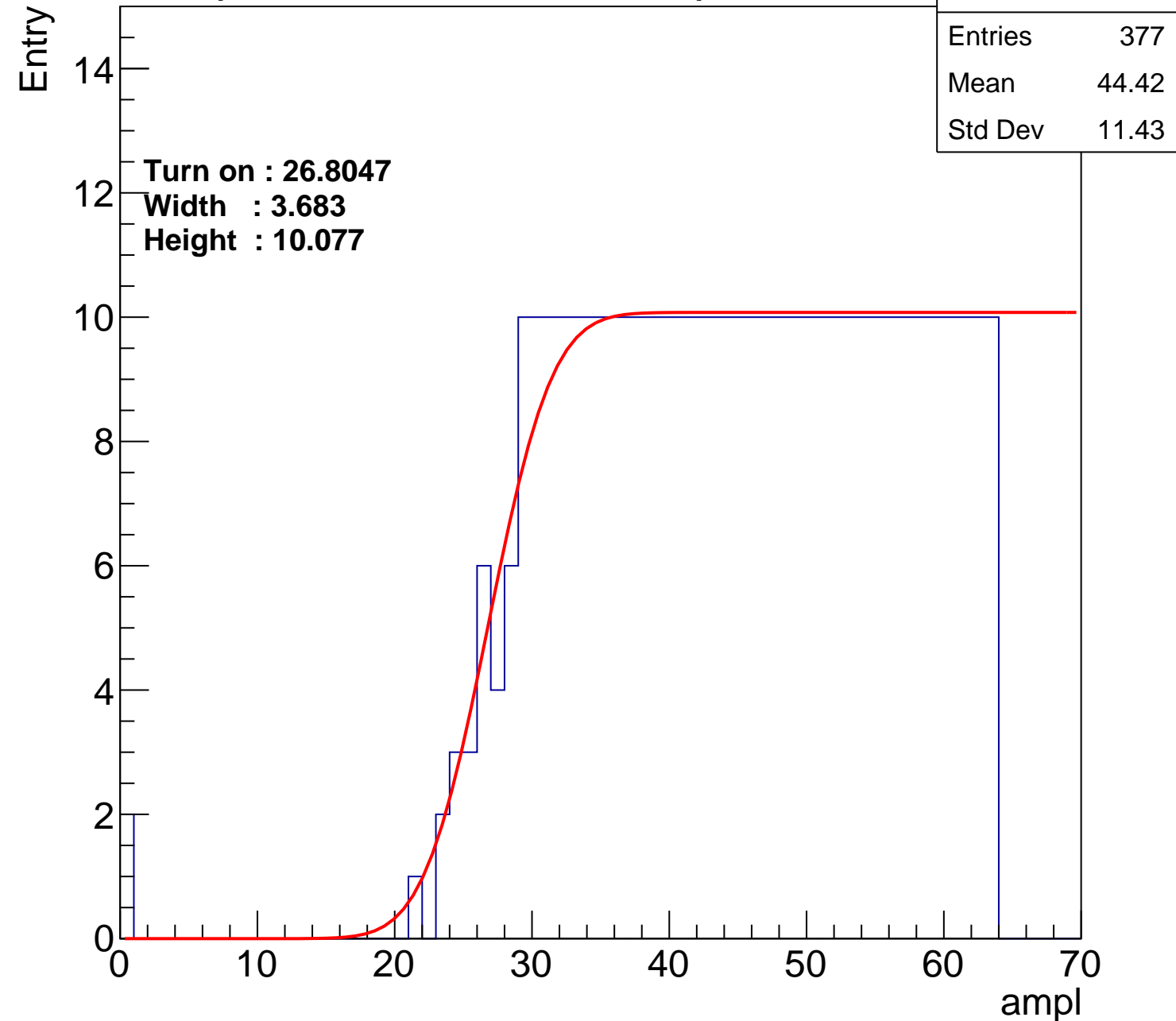
Width : 3.683

Height : 10.077

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch89

calib_packv5_042523_0143.root, FC#0, port D2

Entries	380
Mean	44.23
Std Dev	11.57

Turn on : 26.6972

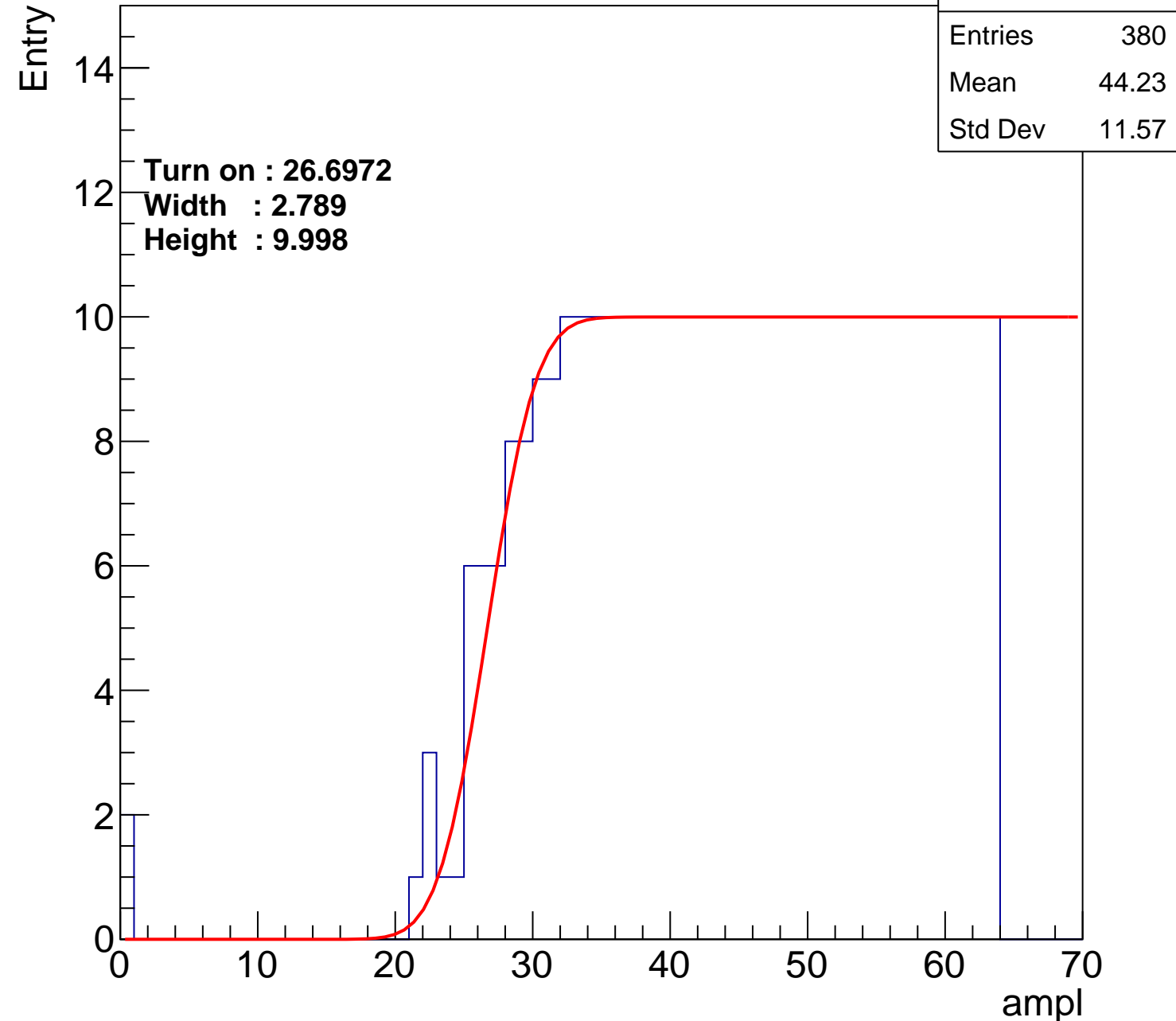
Width : 2.789

Height : 9.998

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch90

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.26
Std Dev	11.83

Turn on : 26.8222

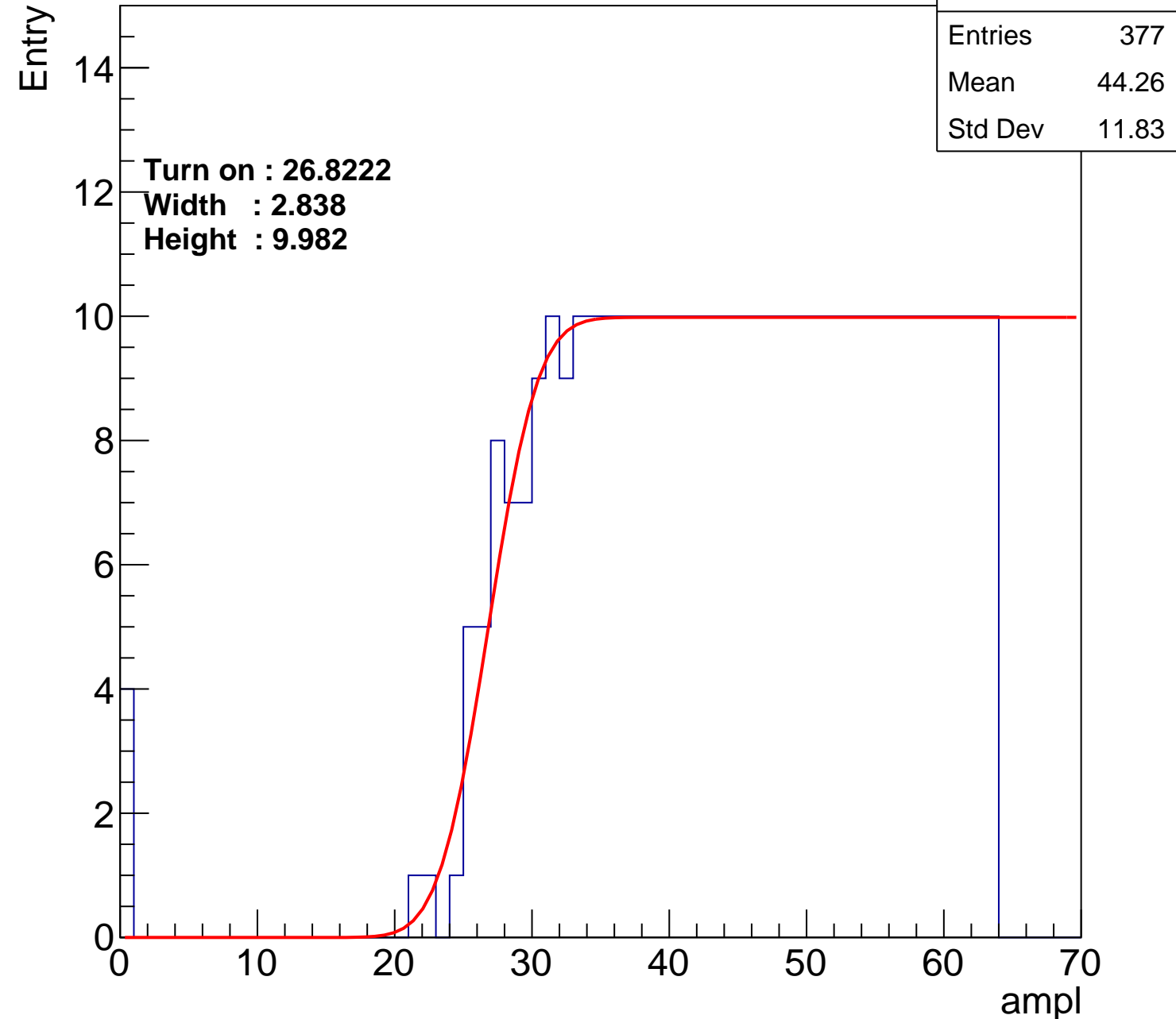
Width : 2.838

Height : 9.982

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch91

calib_packv5_042523_0143.root, FC#0, port D2

Entries	356
Mean	45.26
Std Dev	11.39

Turn on : 29.0936

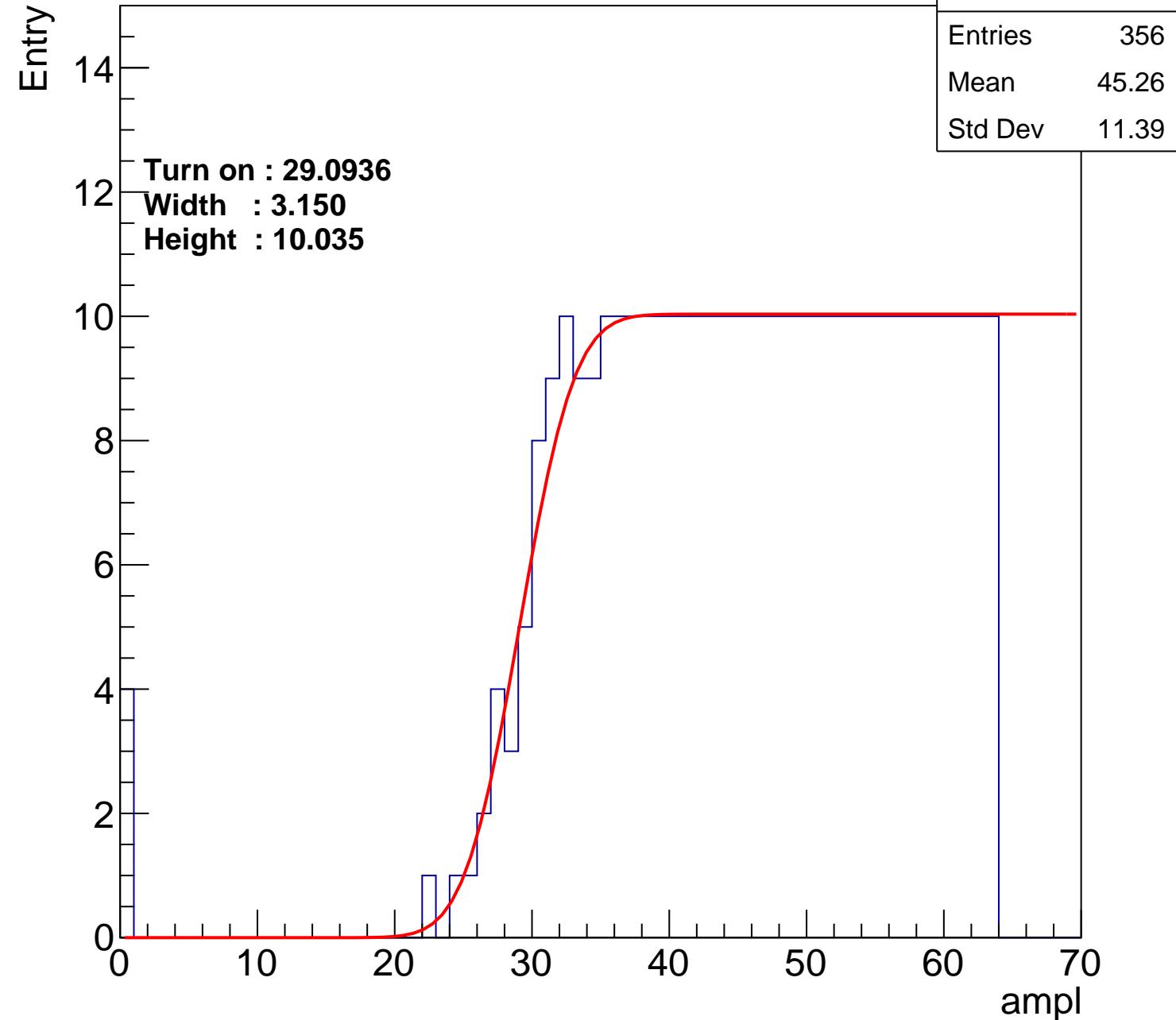
Width : 3.150

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch92

calib_packv5_042523_0143.root, FC#0, port D2

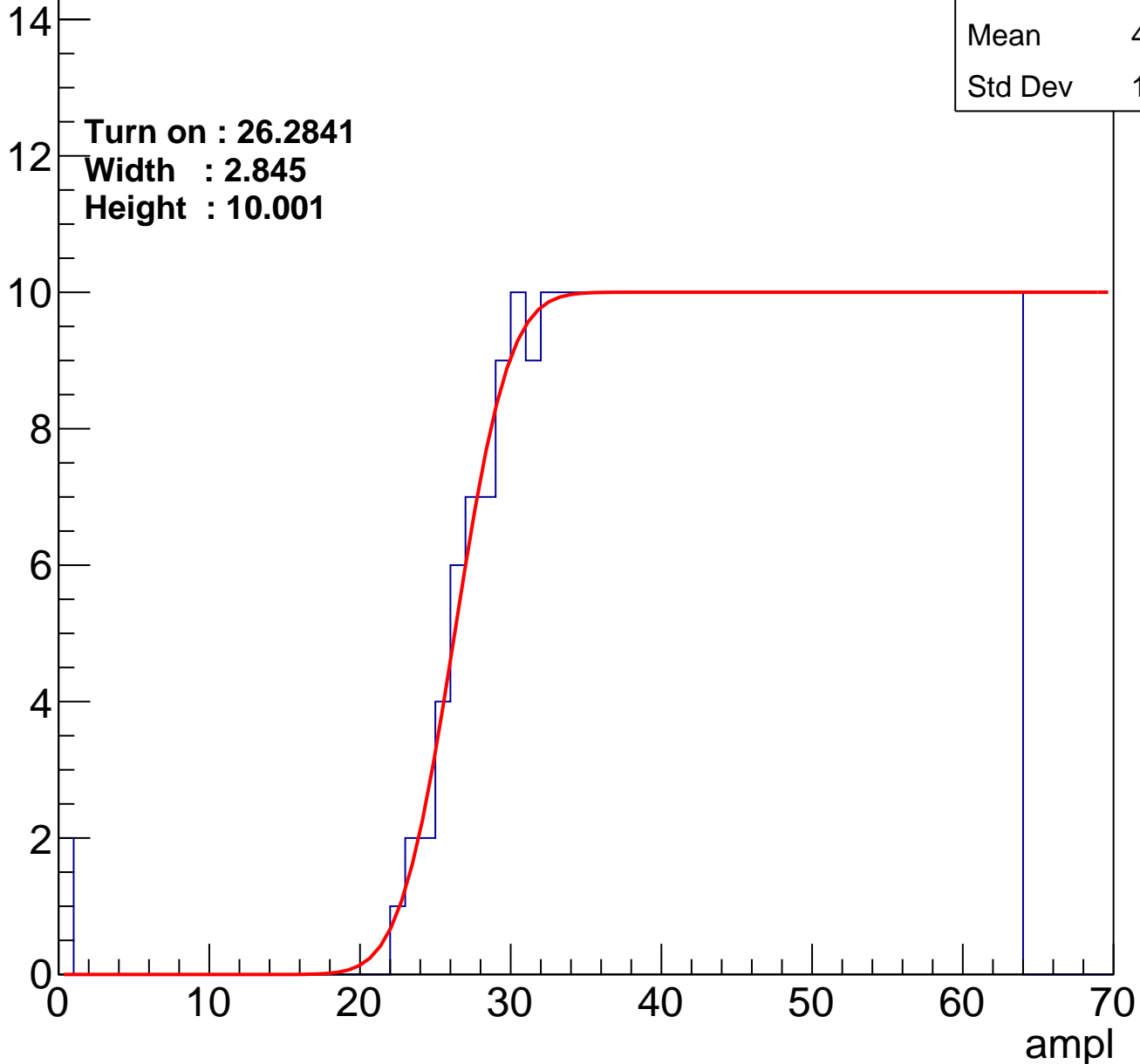
Entries	379
Mean	44.32
Std Dev	11.48

Turn on : 26.2841

Width : 2.845

Height : 10.001

Entry



B1L101S, U11-ch93

calib_packv5_042523_0143.root, FC#0, port D2

Entries	366
Mean	44.96
Std Dev	11.14

Turn on : 27.3178

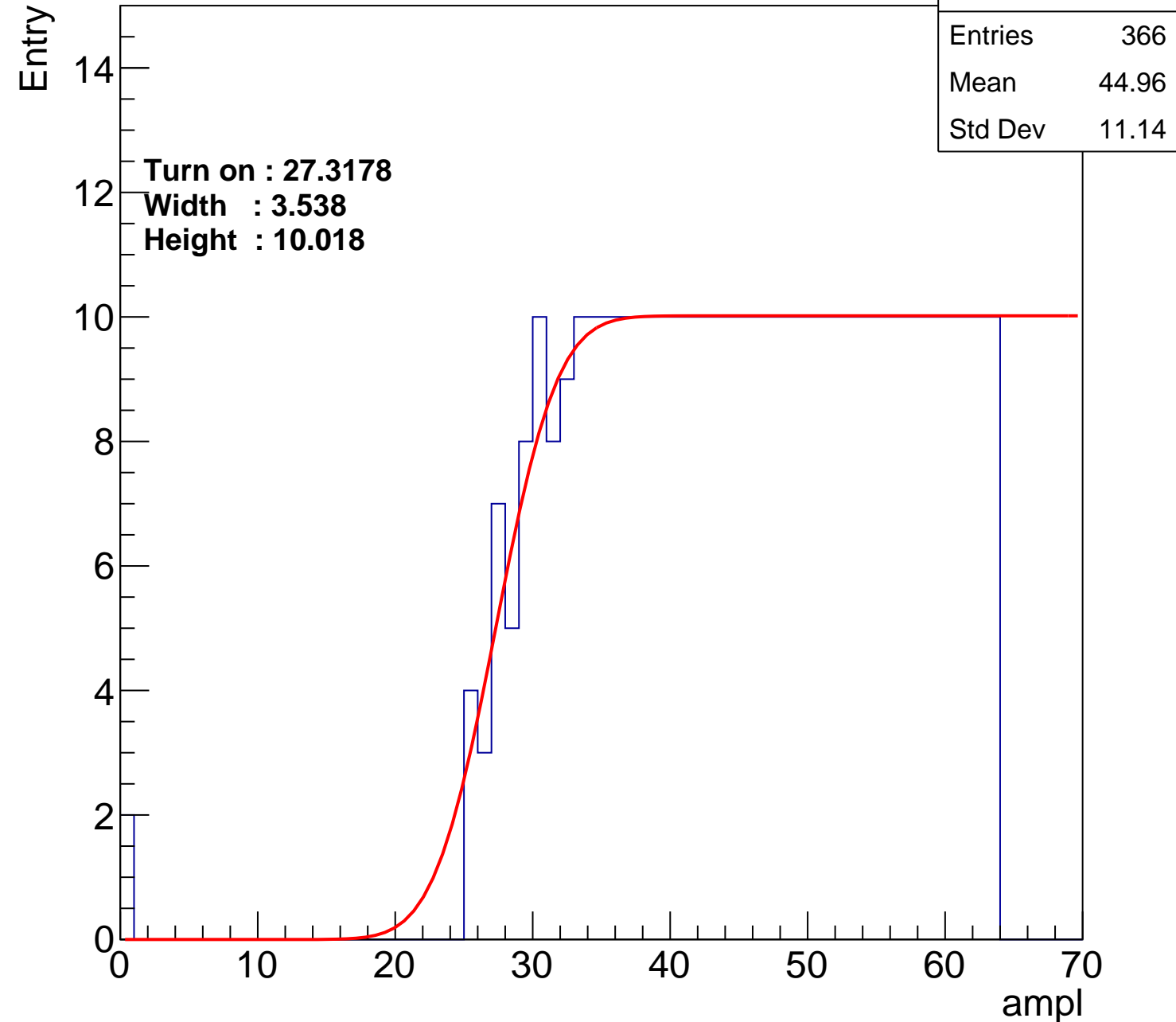
Width : 3.538

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch94

calib_packv5_042523_0143.root, FC#0, port D2

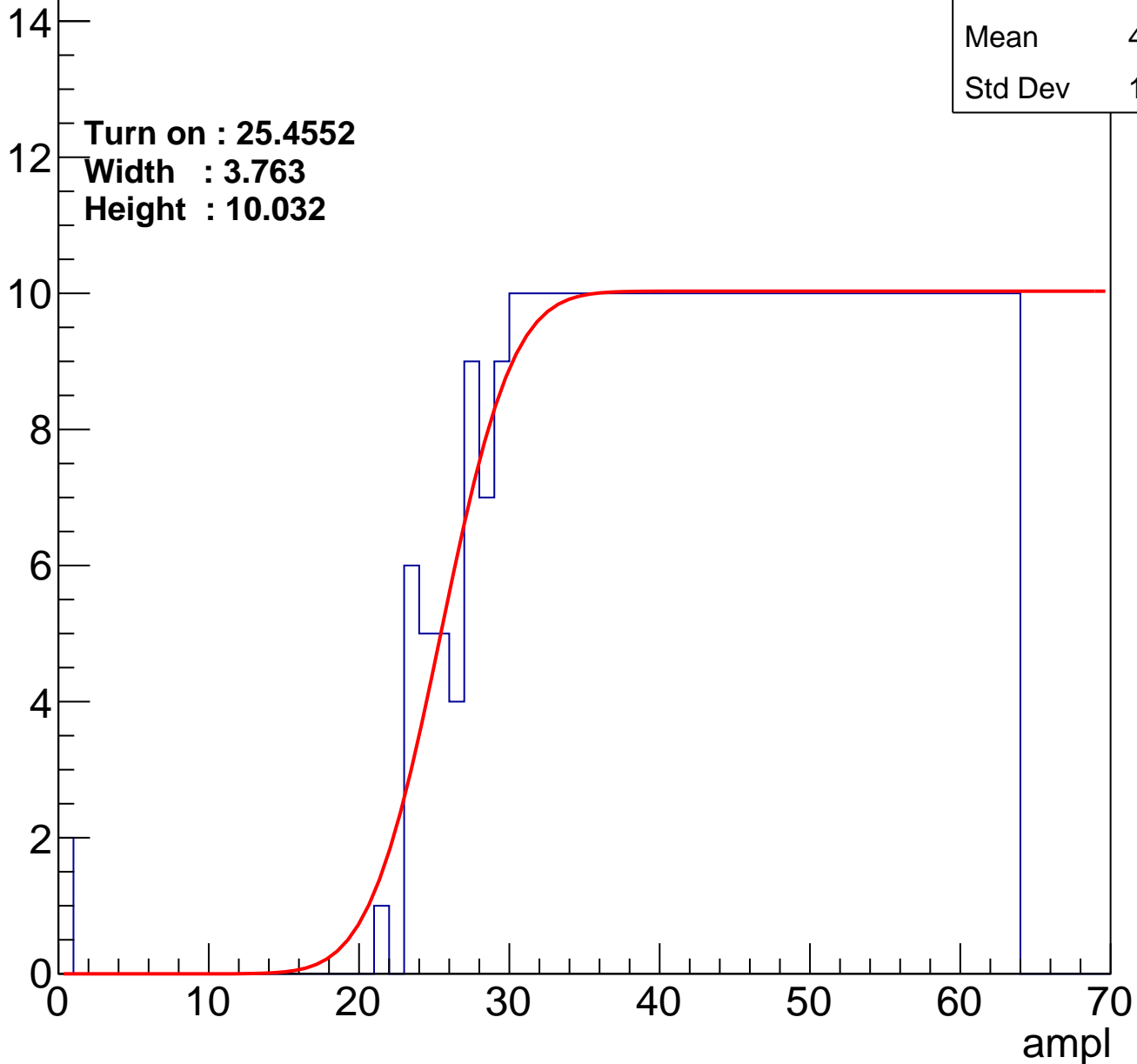
Entries	388
Mean	43.86
Std Dev	11.73

Turn on : 25.4552

Width : 3.763

Height : 10.032

Entry



B1L101S, U11-ch95

calib_packv5_042523_0143.root, FC#0, port D2

Entries	353
Mean	45.61
Std Dev	10.8

Turn on : 29.1987

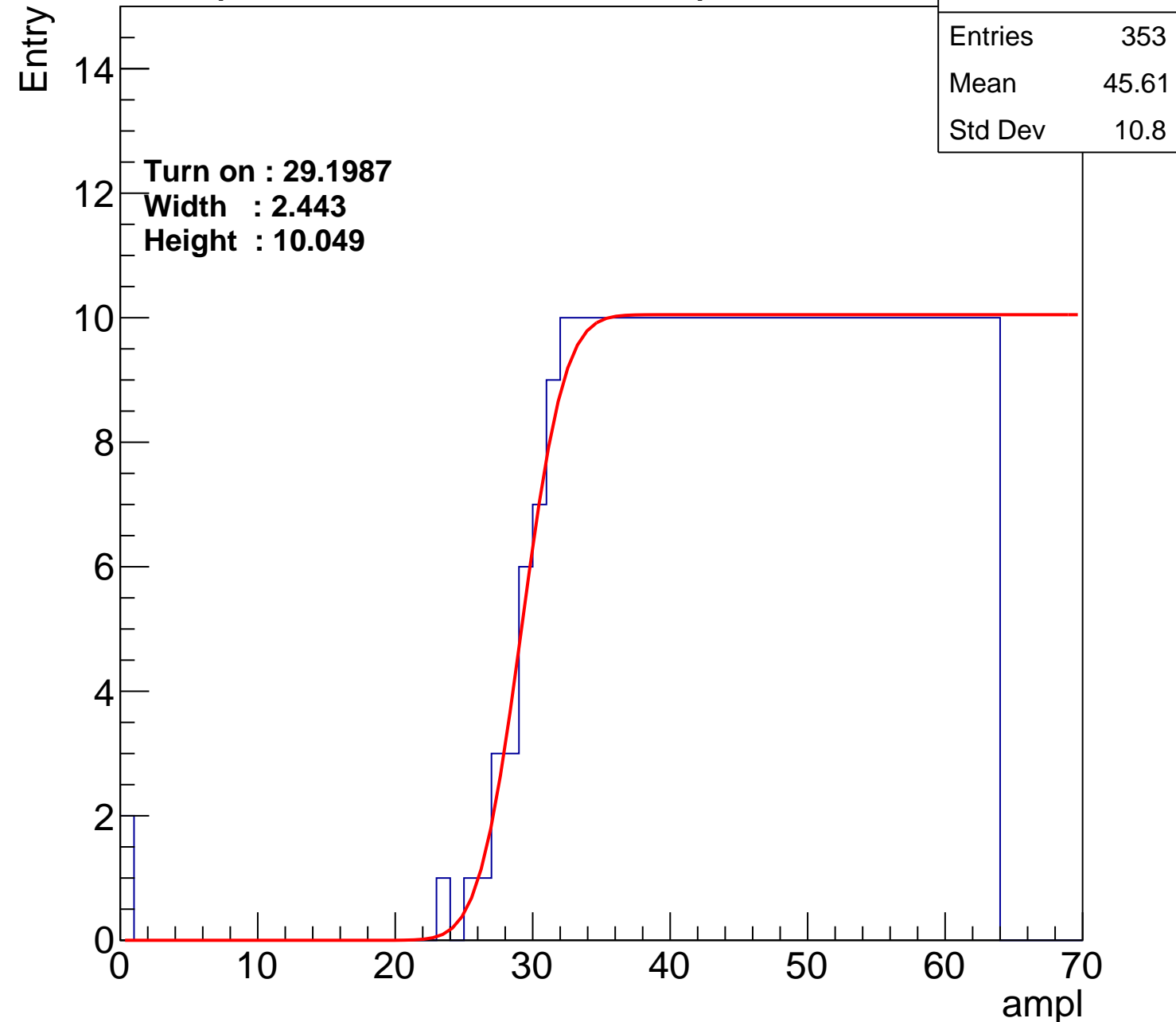
Width : 2.443

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch96

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.53
Std Dev	11.5

Turn on : 27.3662

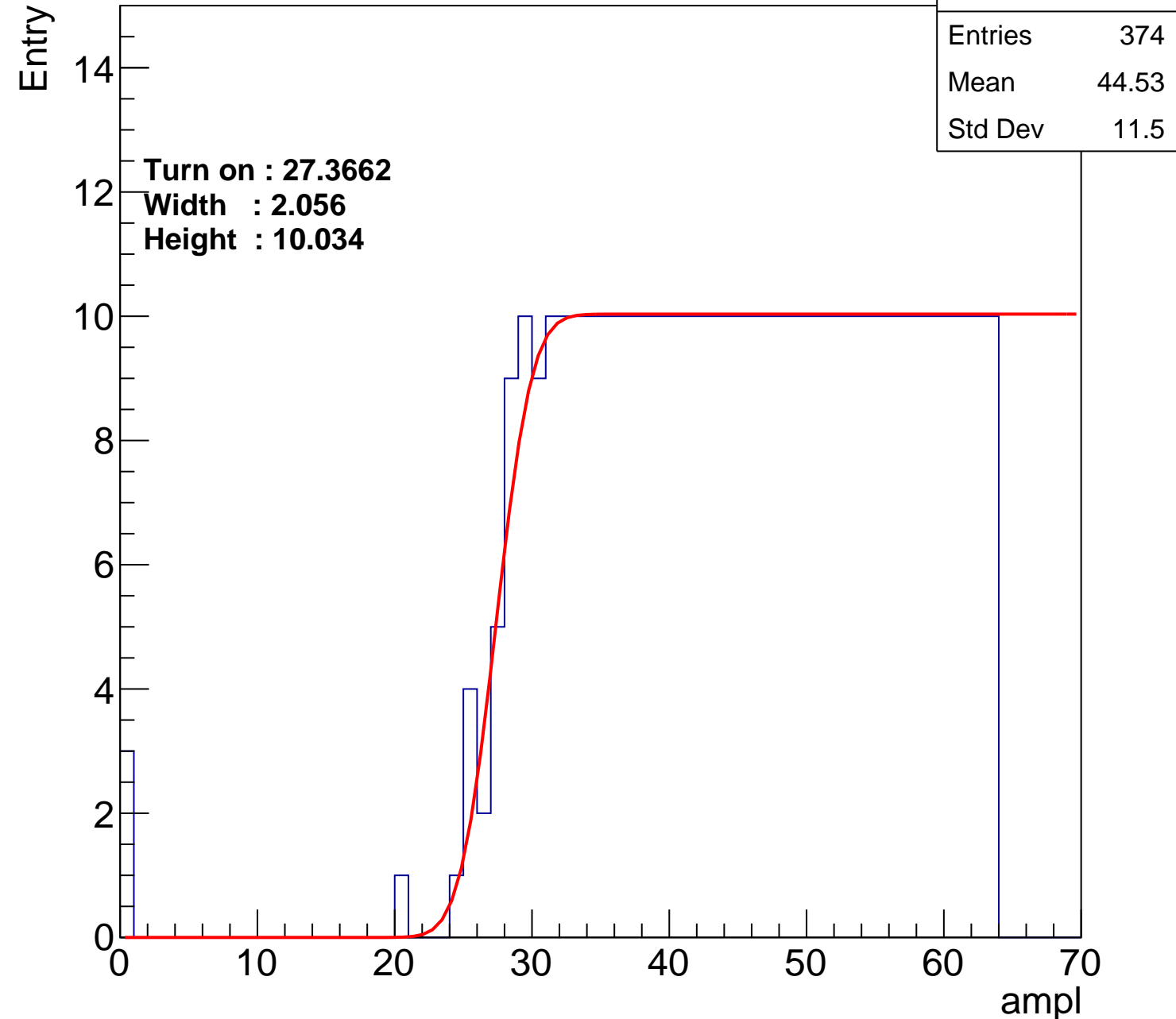
Width : 2.056

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch97

calib_packv5_042523_0143.root, FC#0, port D2

Entries	365
Mean	44.97
Std Dev	11.26

Turn on : 27.6728

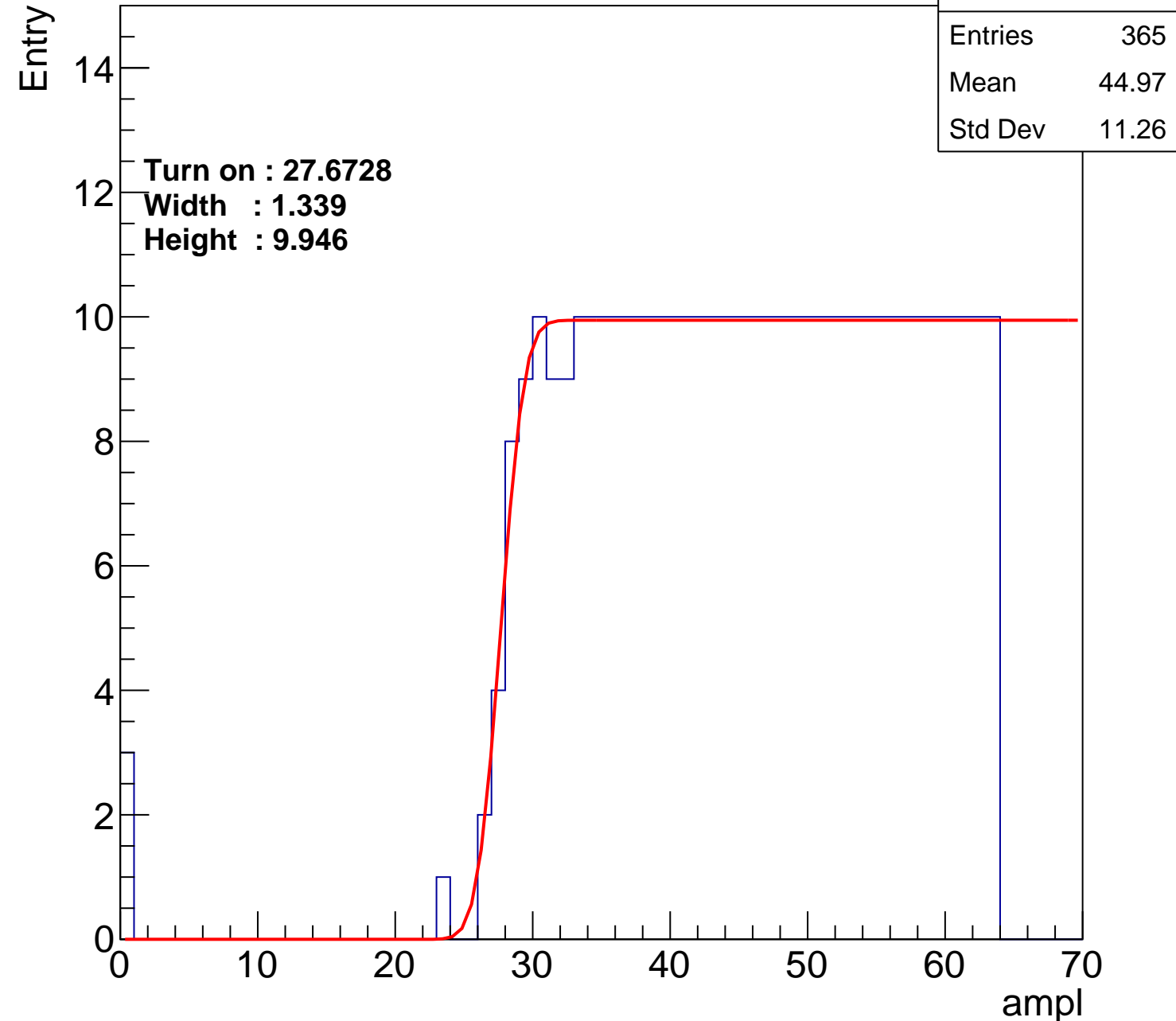
Width : 1.339

Height : 9.946

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch98

calib_packv5_042523_0143.root, FC#0, port D2

Entries	371
Mean	44.53
Std Dev	11.72

Turn on : 27.1840

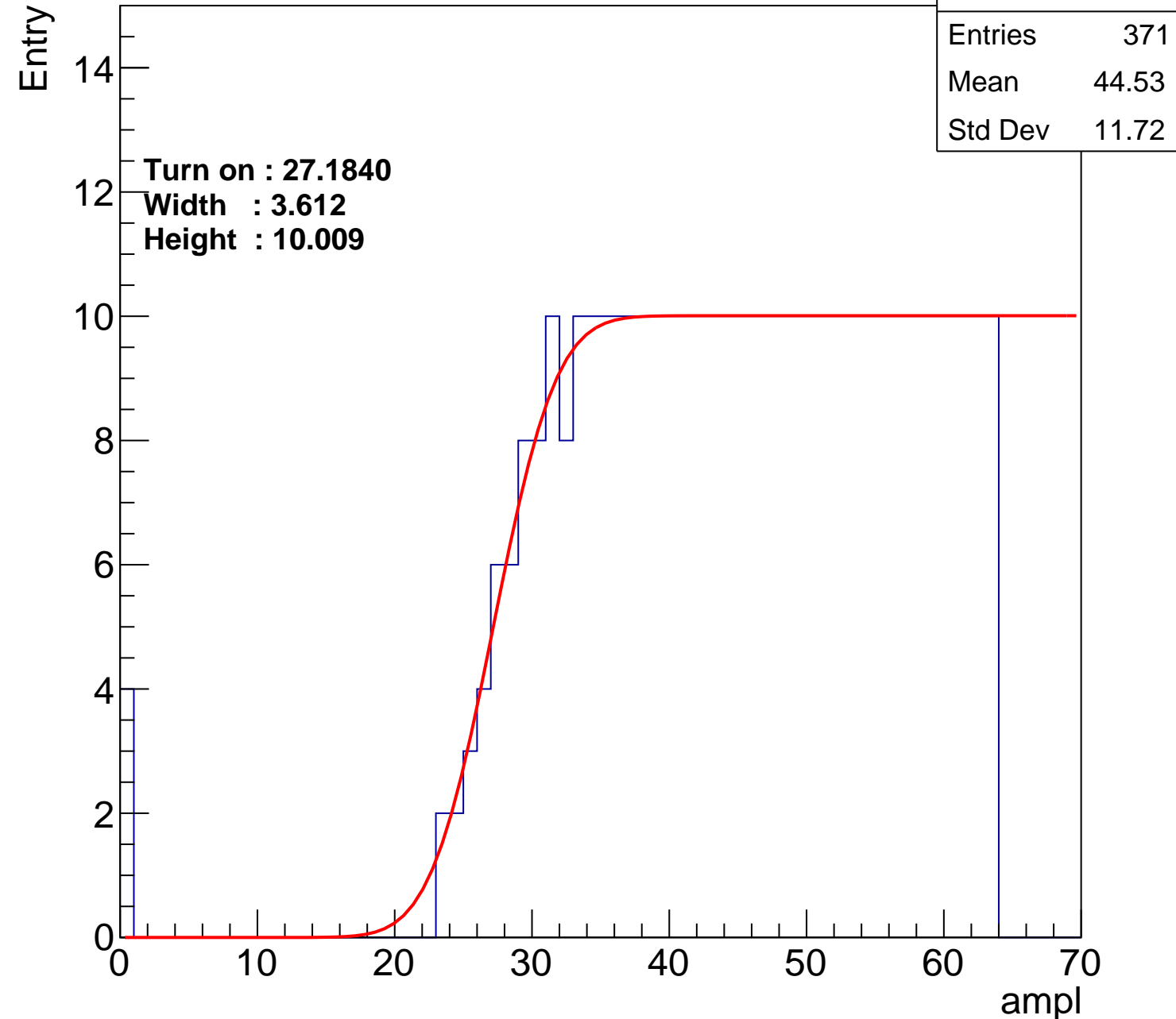
Width : 3.612

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch99

calib_packv5_042523_0143.root, FC#0, port D2

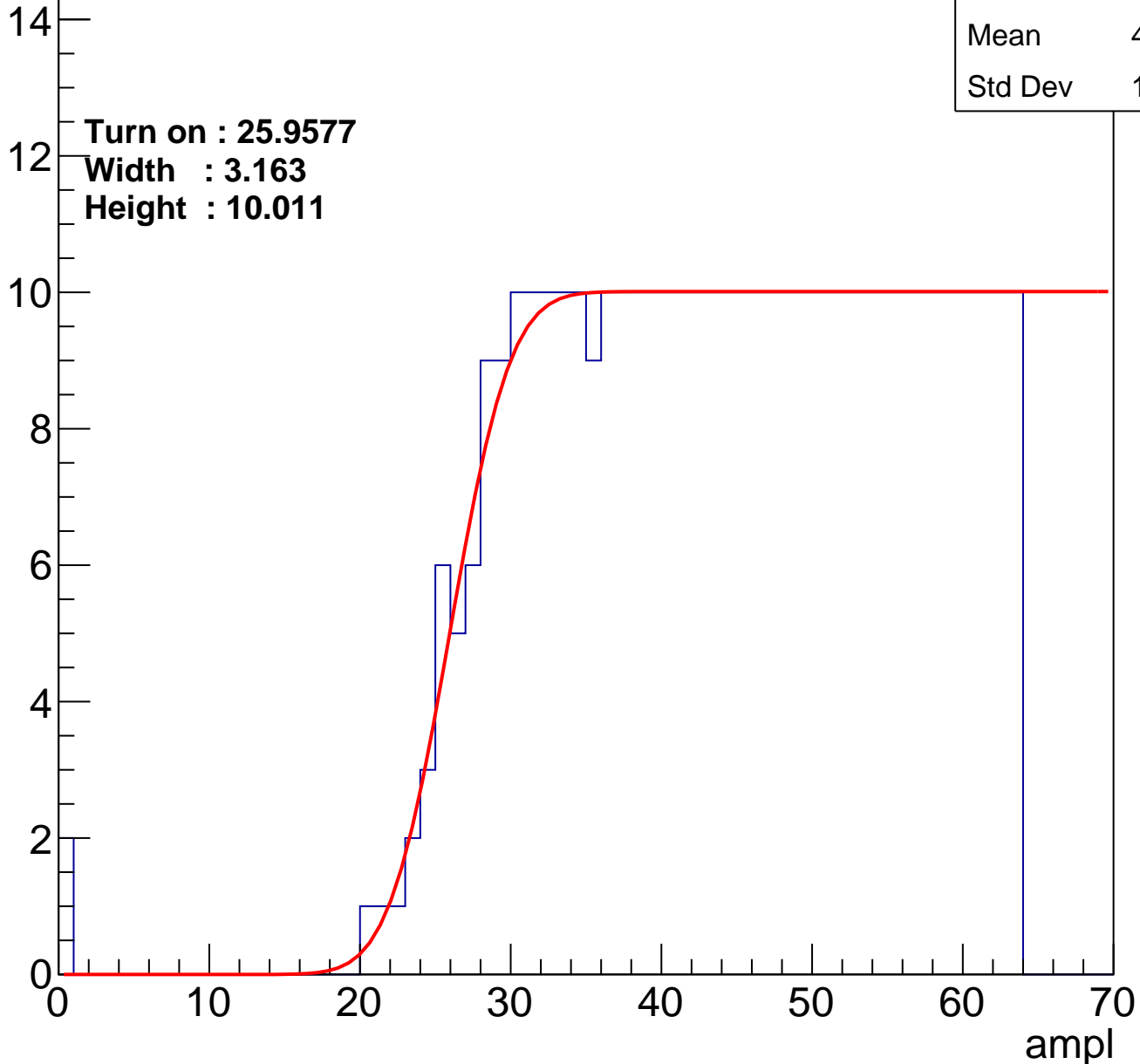
Entries	384
Mean	44.04
Std Dev	11.65

Turn on : 25.9577

Width : 3.163

Height : 10.011

Entry



B1L101S, U11-ch100

calib_packv5_042523_0143.root, FC#0, port D2

Entries	404
Mean	42.94
Std Dev	12.54

Turn on : 24.4200

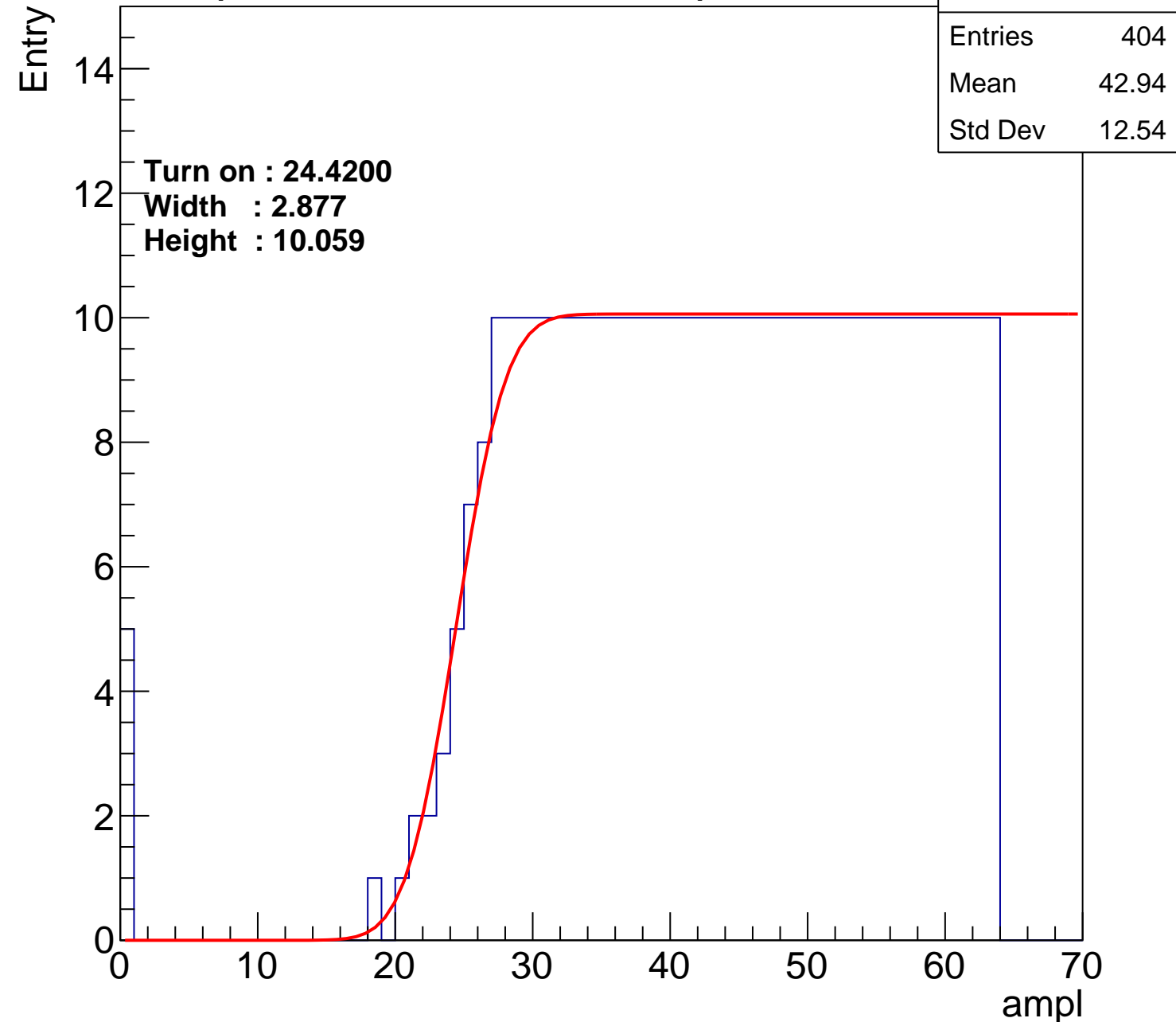
Width : 2.877

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch101

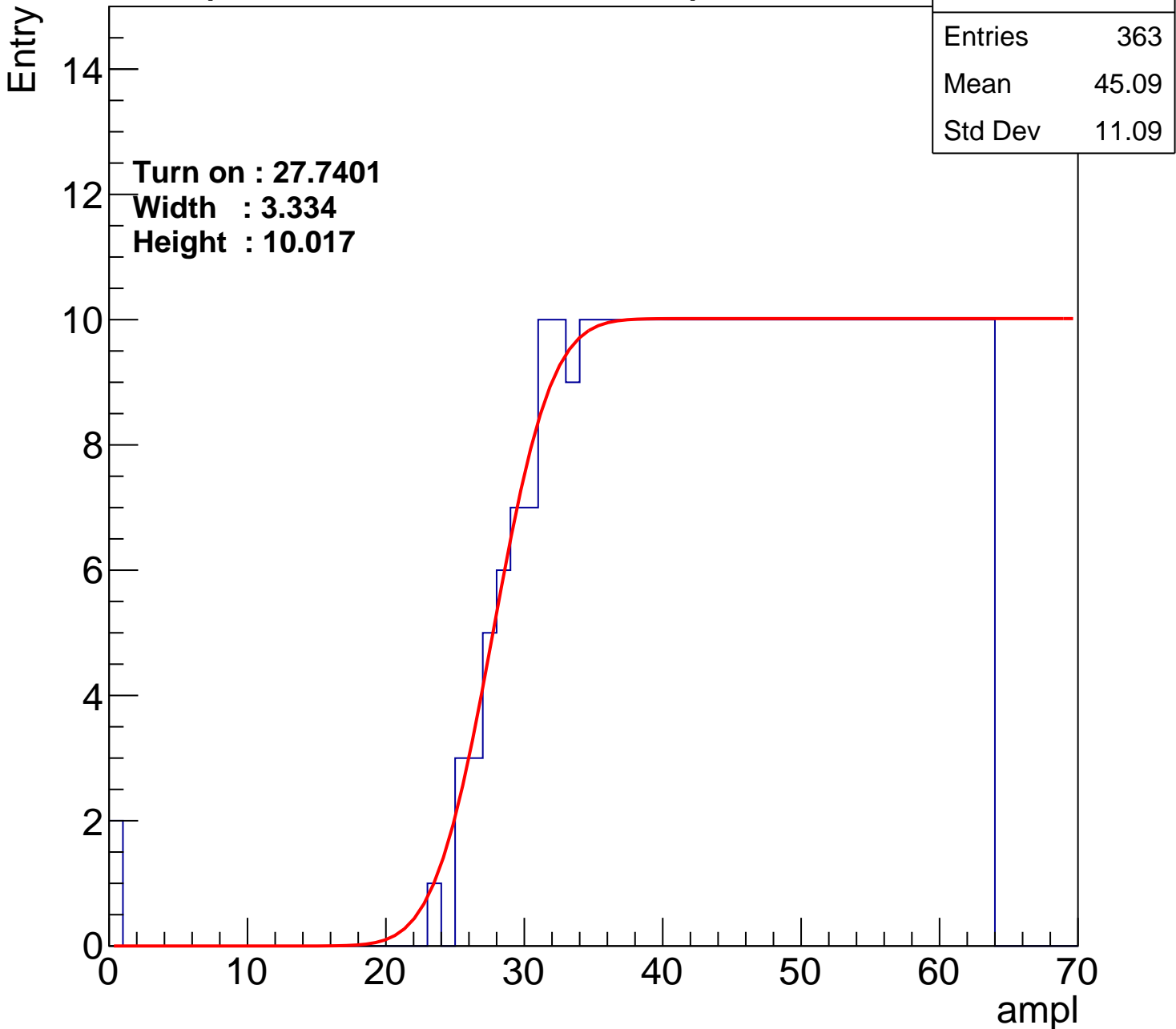
calib_packv5_042523_0143.root, FC#0, port D2

Entries	363
Mean	45.09
Std Dev	11.09

Turn on : 27.7401

Width : 3.334

Height : 10.017



B1L101S, U11-ch102

calib_packv5_042523_0143.root, FC#0, port D2

Entries	371
Mean	44.78
Std Dev	11.08

Turn on : 27.2032

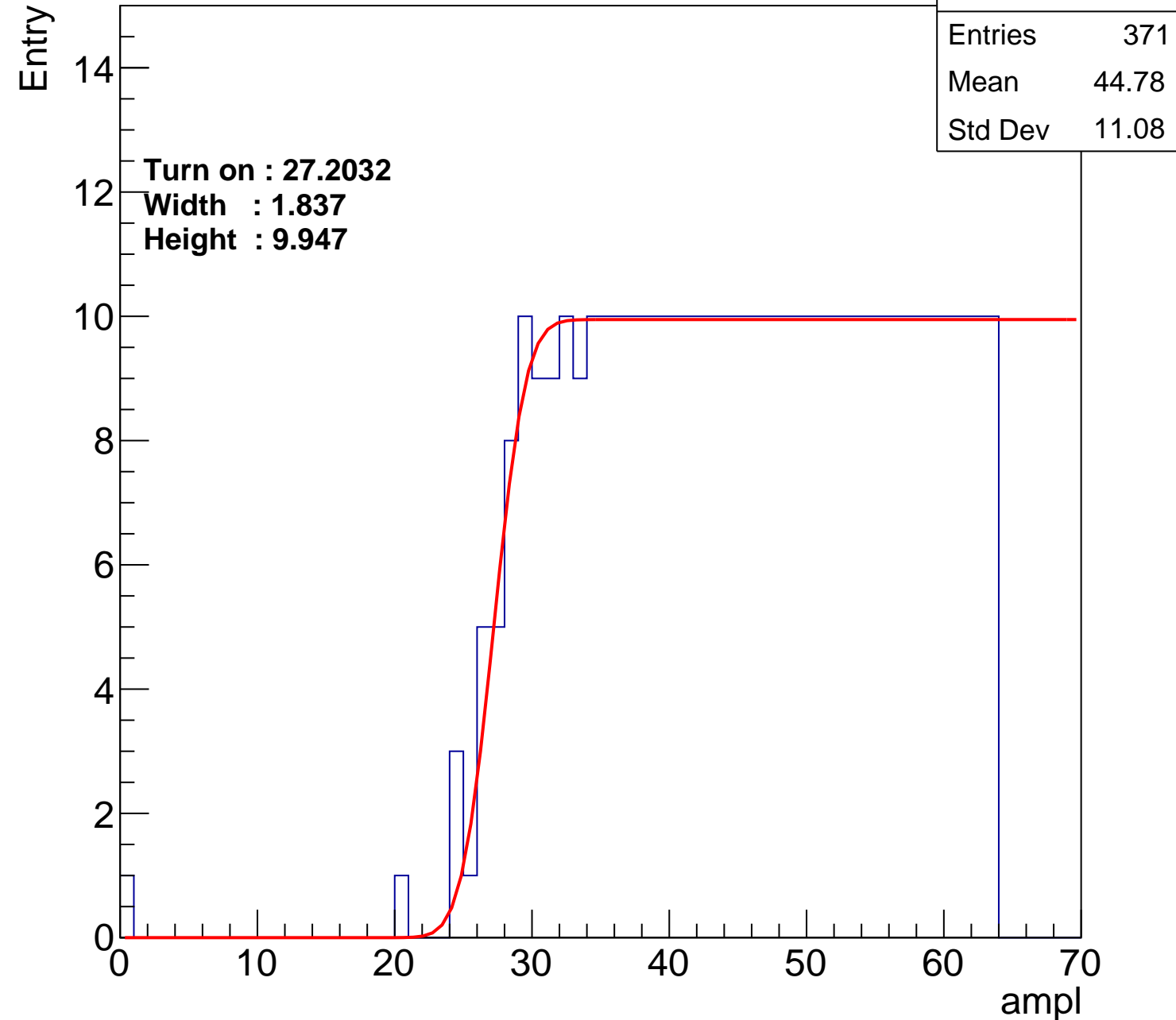
Width : 1.837

Height : 9.947

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch103

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.14
Std Dev	12.16

Turn on : 26.5771

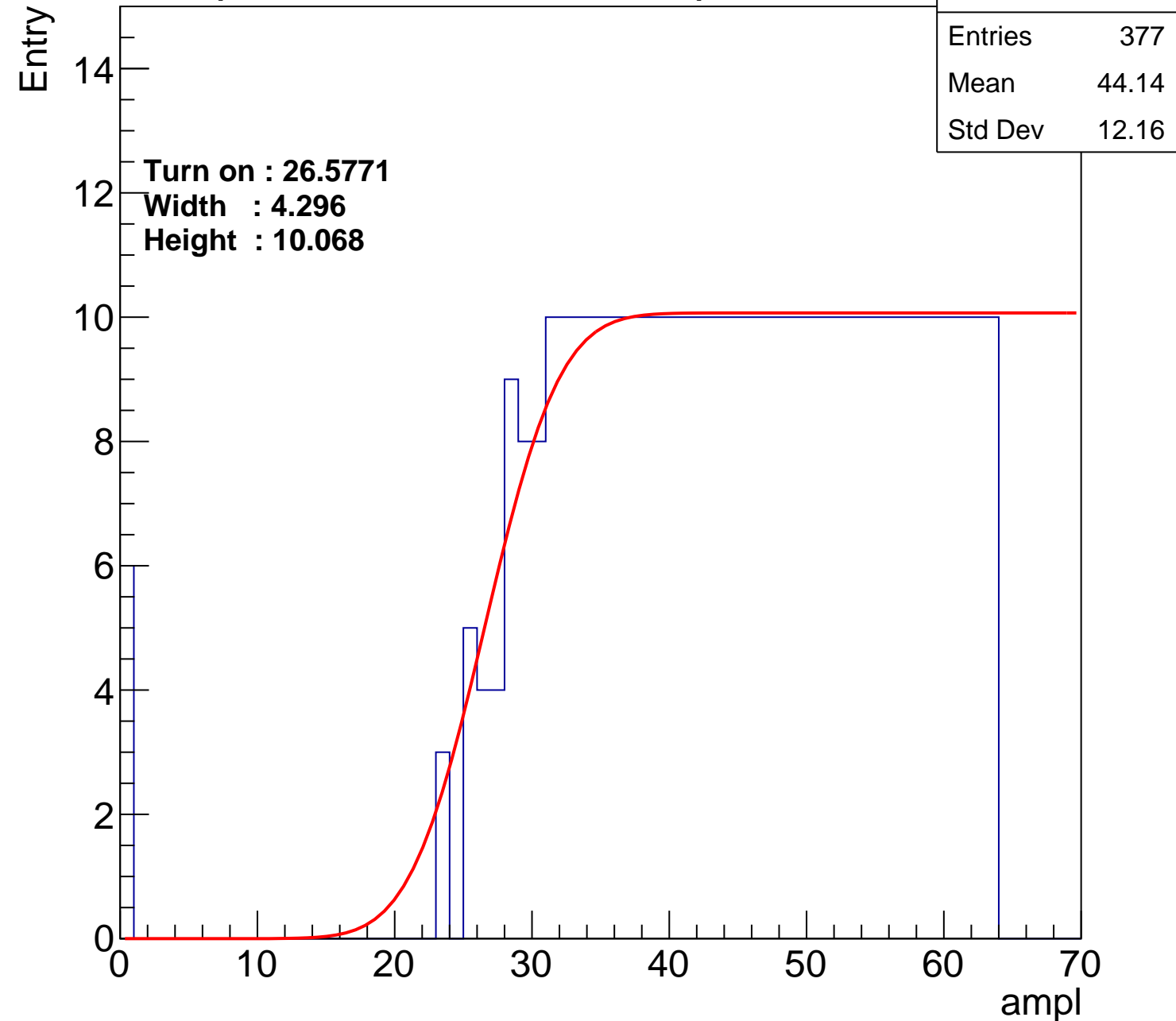
Width : 4.296

Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch104

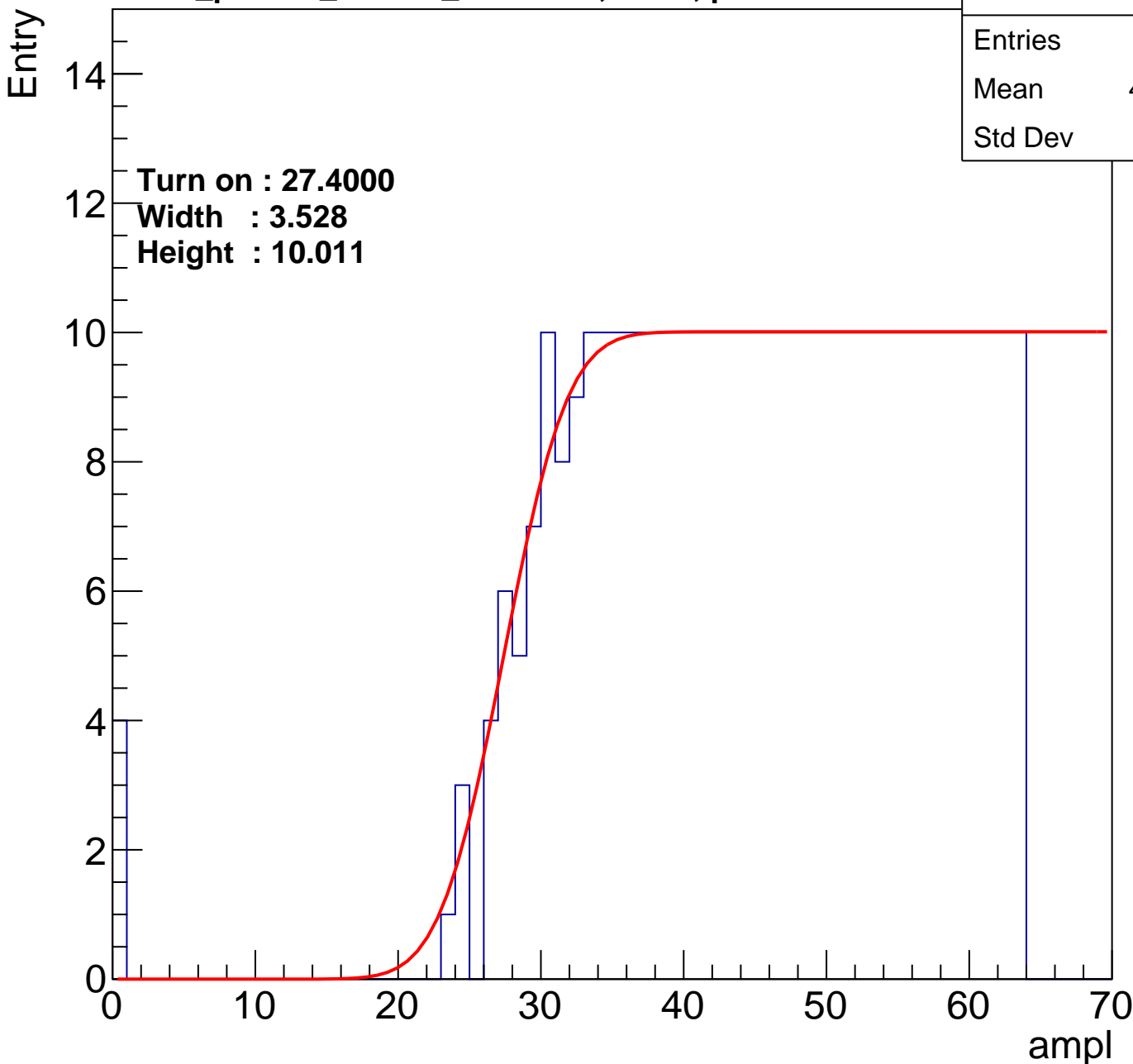
calib_packv5_042523_0143.root, FC#0, port D2

Entries	367
Mean	44.74
Std Dev	11.61

Turn on : 27.4000

Width : 3.528

Height : 10.011



B1L101S, U11-ch105

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.51
Std Dev	11.25

Turn on : 26.9410

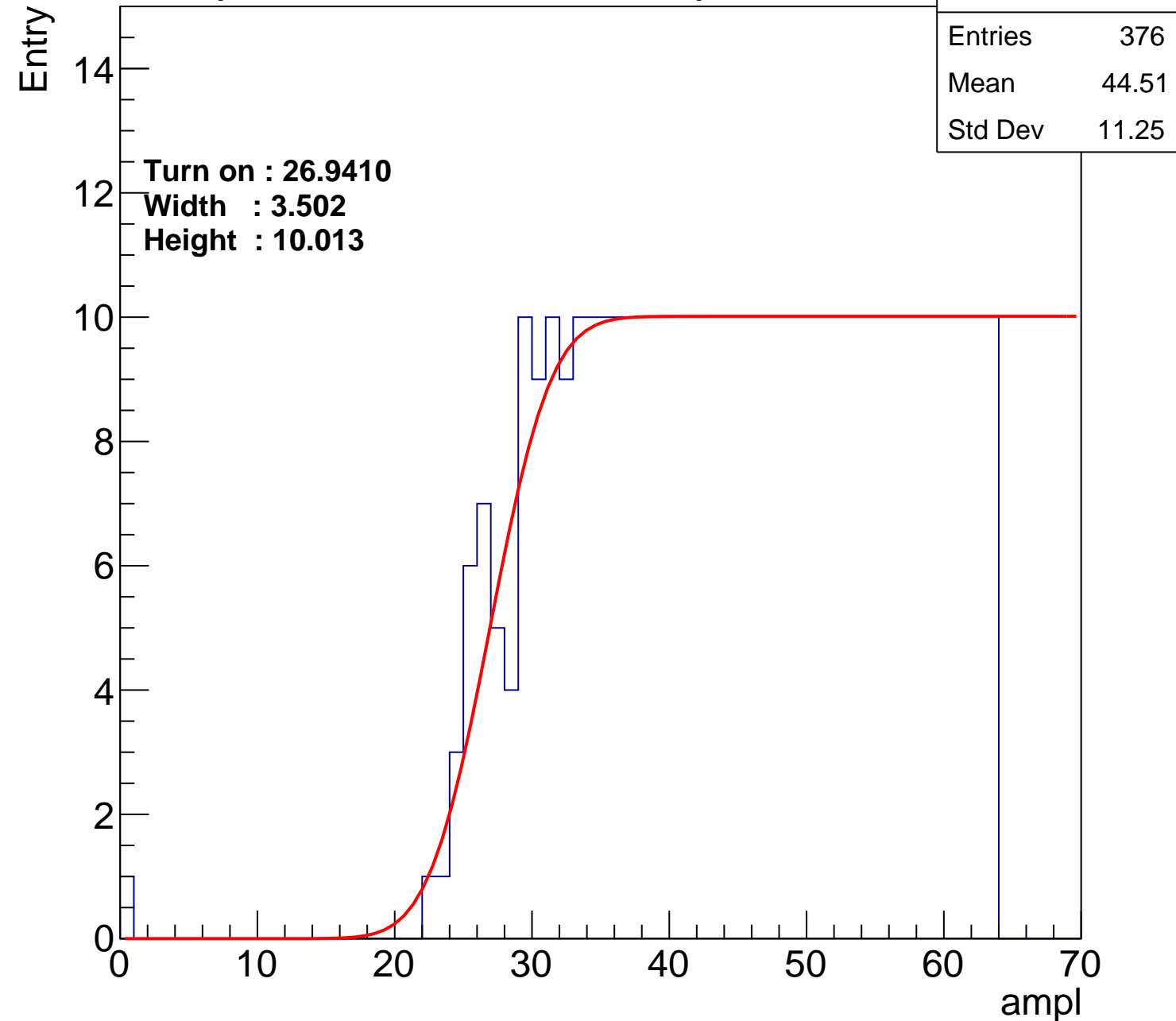
Width : 3.502

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch106

calib_packv5_042523_0143.root, FC#0, port D2

Entries	373
Mean	44.53
Std Dev	11.53

Turn on : 26.9101

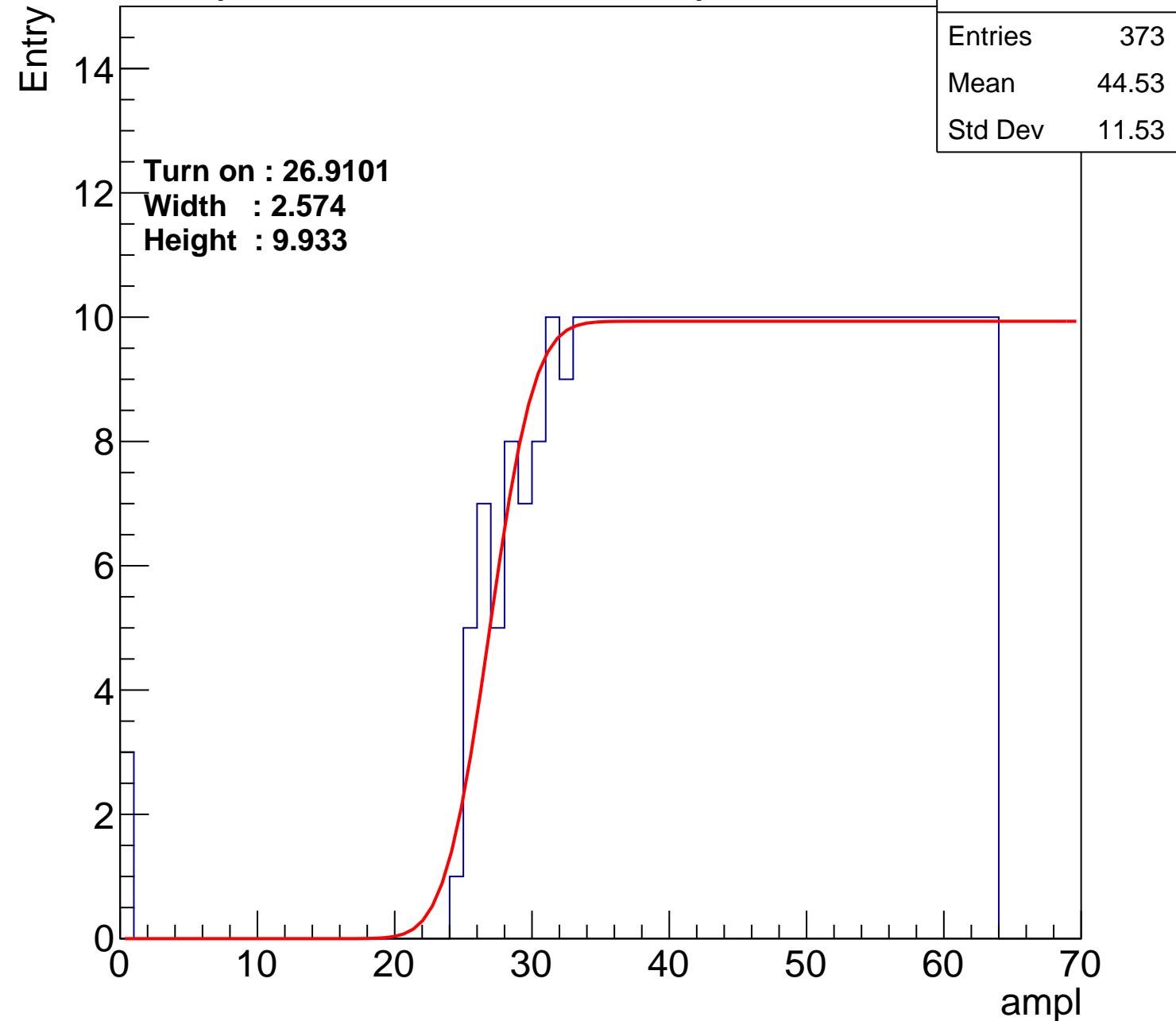
Width : 2.574

Height : 9.933

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch107

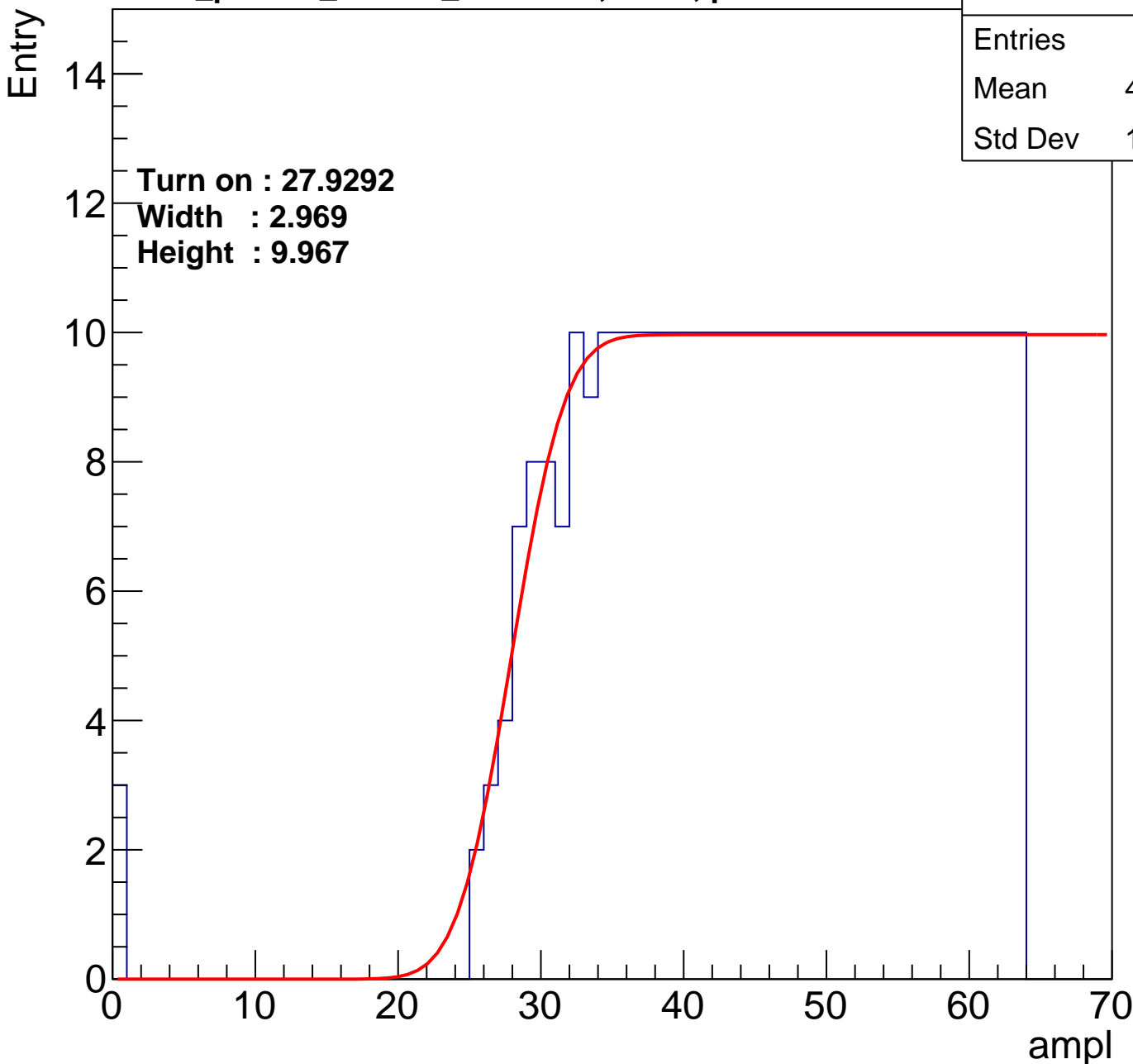
calib_packv5_042523_0143.root, FC#0, port D2

Entries	361
Mean	45.12
Std Dev	11.24

Turn on : 27.9292

Width : 2.969

Height : 9.967



B1L101S, U11-ch108

calib_packv5_042523_0143.root, FC#0, port D2

Entries	397
Mean	43.29
Std Dev	12.28

Turn on : 24.9712

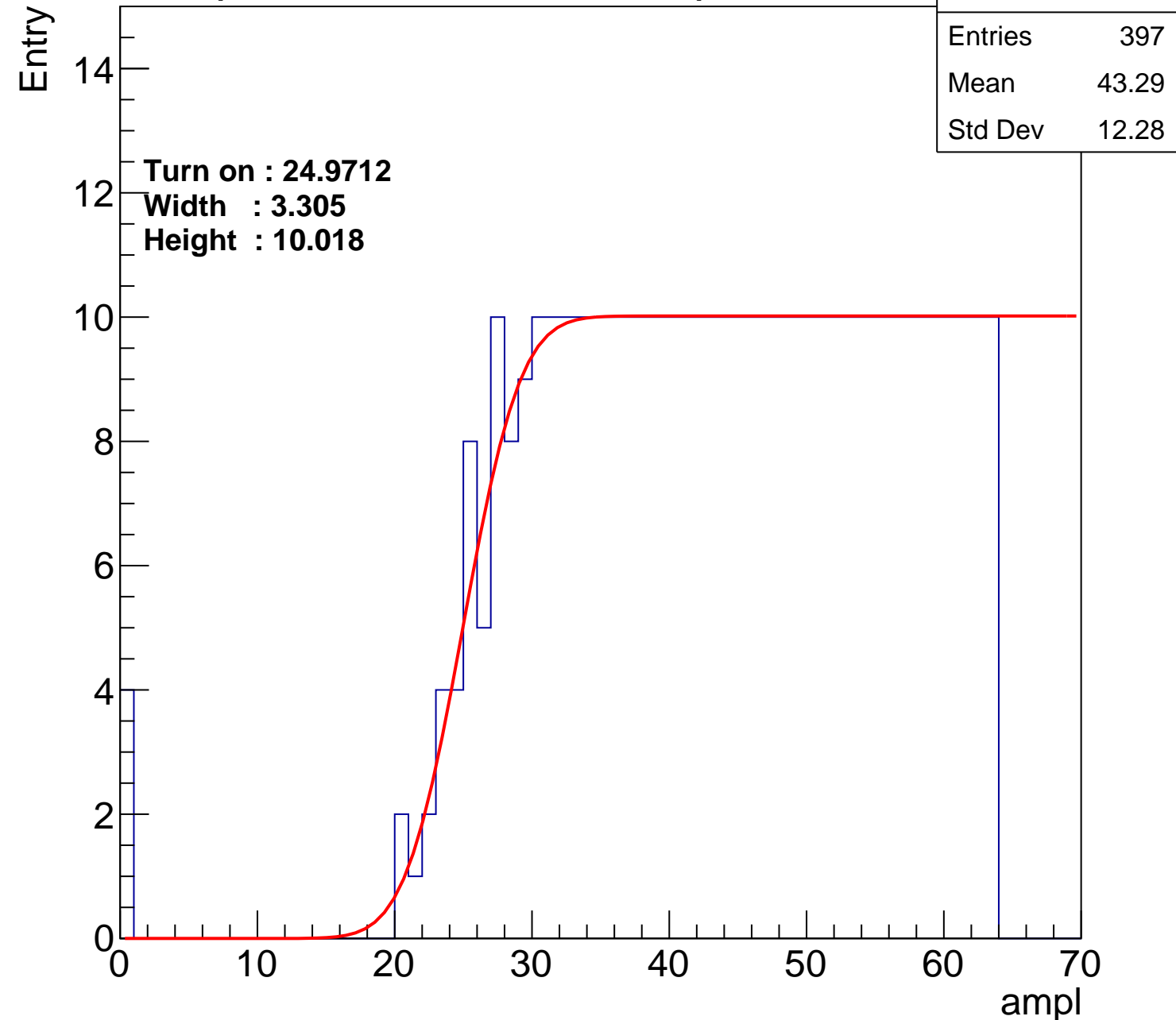
Width : 3.305

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch109

calib_packv5_042523_0143.root, FC#0, port D2

Entries	369
Mean	44.86
Std Dev	11.06

Turn on : 27.3880

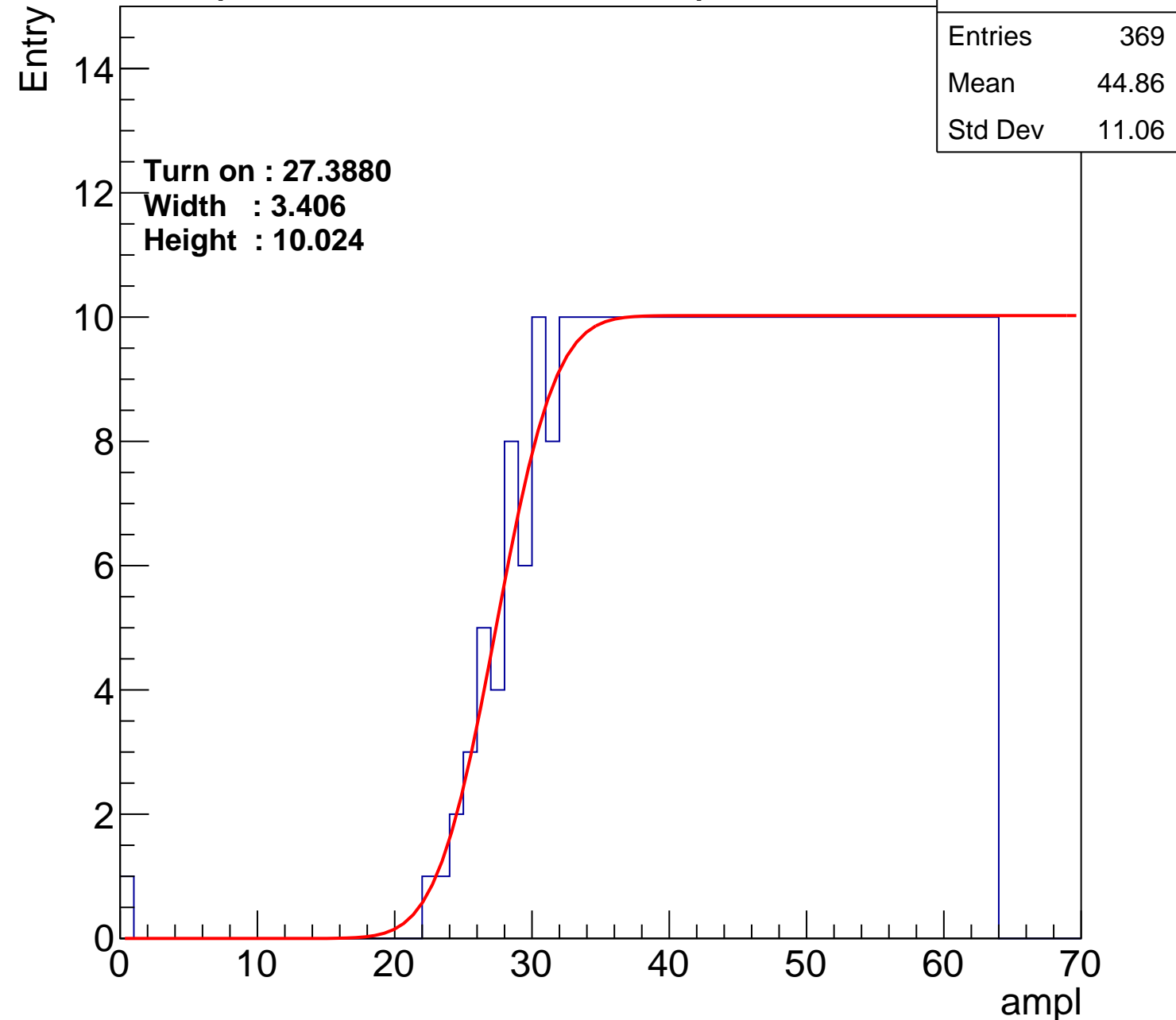
Width : 3.406

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch110

calib_packv5_042523_0143.root, FC#0, port D2

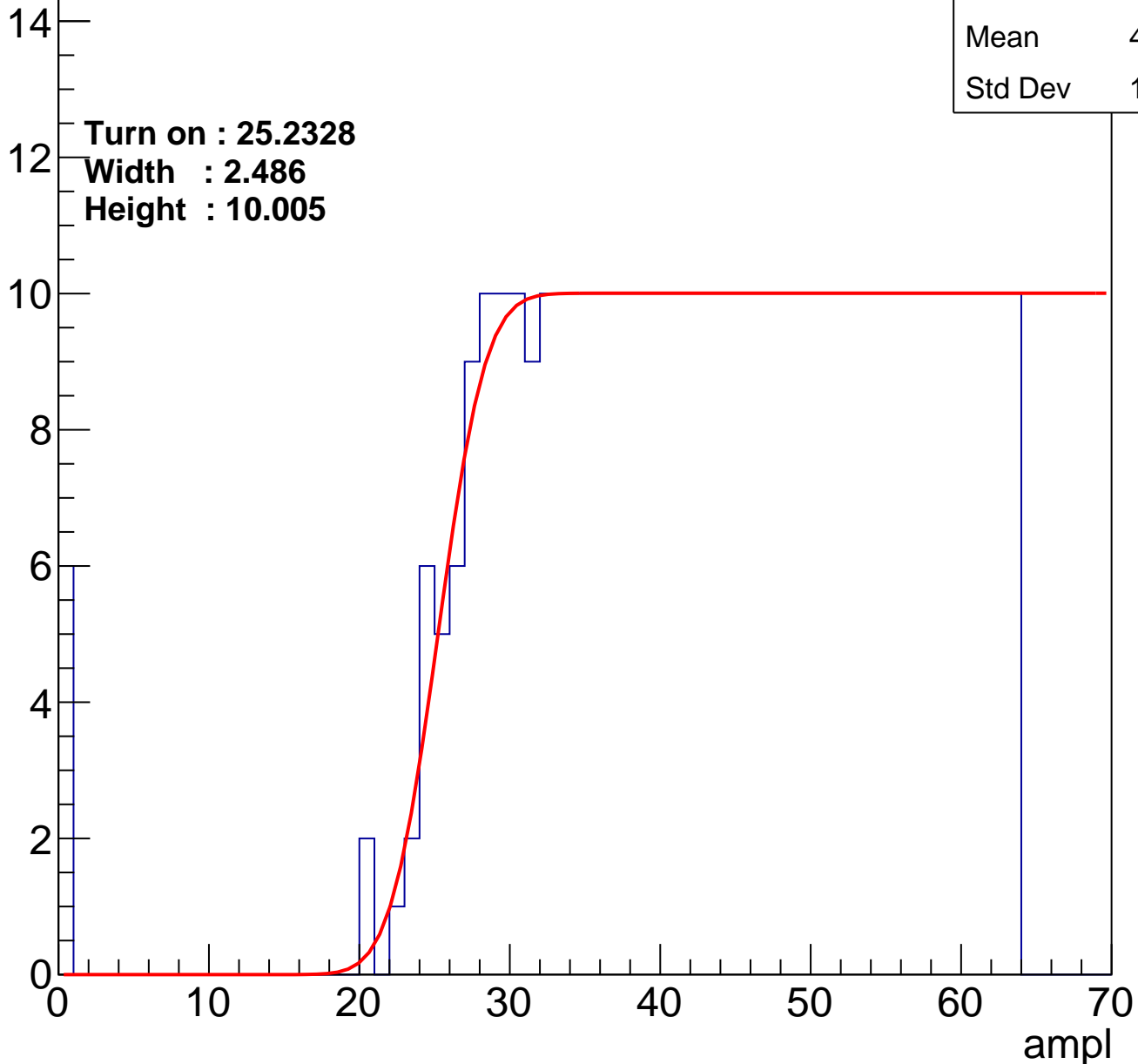
Entries	396
Mean	43.24
Std Dev	12.53

Turn on : 25.2328

Width : 2.486

Height : 10.005

Entry



B1L101S, U11-ch111

calib_packv5_042523_0143.root, FC#0, port D2

Entries	368
Mean	44.8
Std Dev	11.3

Turn on : 27.8646

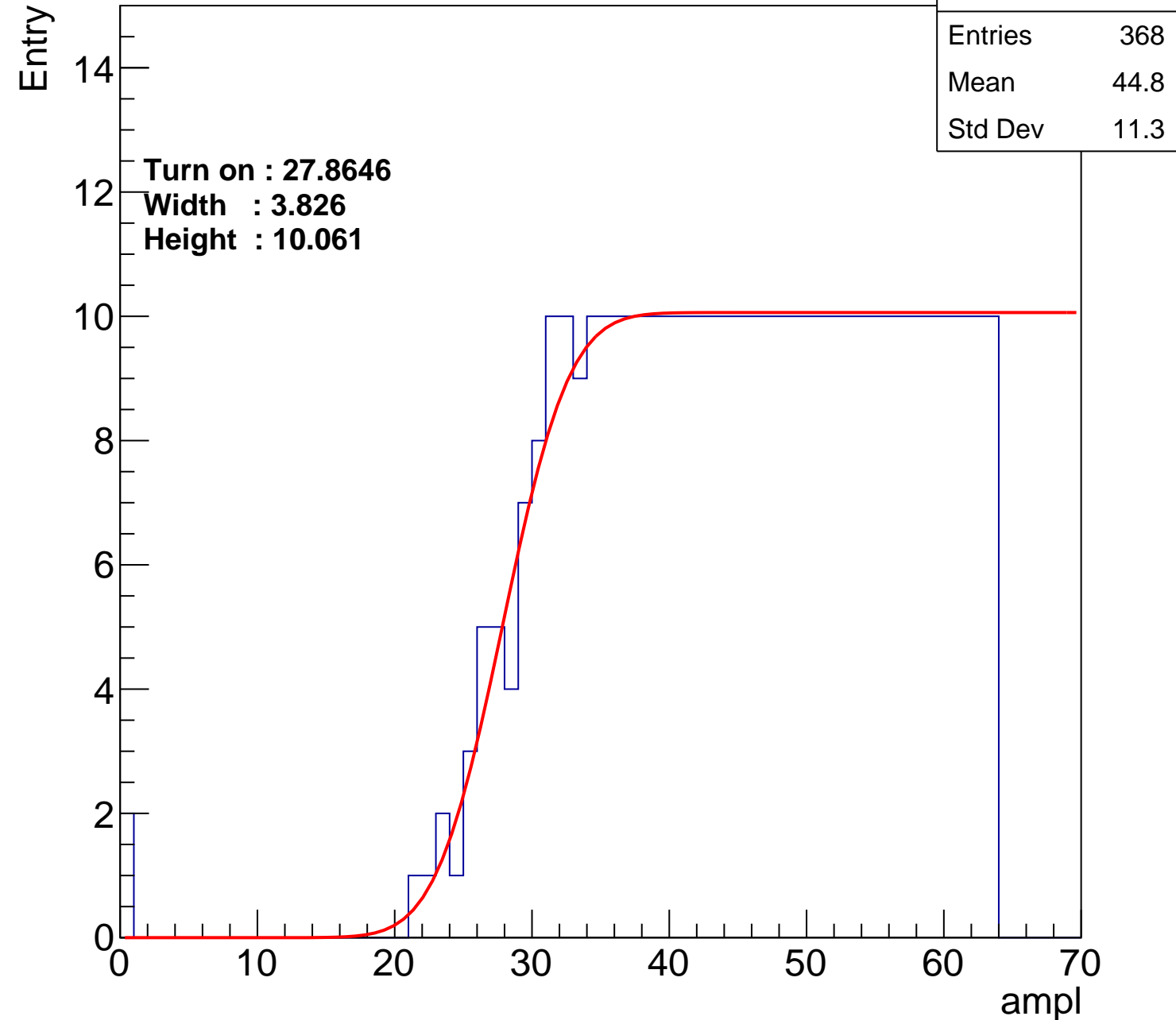
Width : 3.826

Height : 10.061

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch112

calib_packv5_042523_0143.root, FC#0, port D2

Entries	366
Mean	44.79
Std Dev	11.6

Turn on : 27.9037

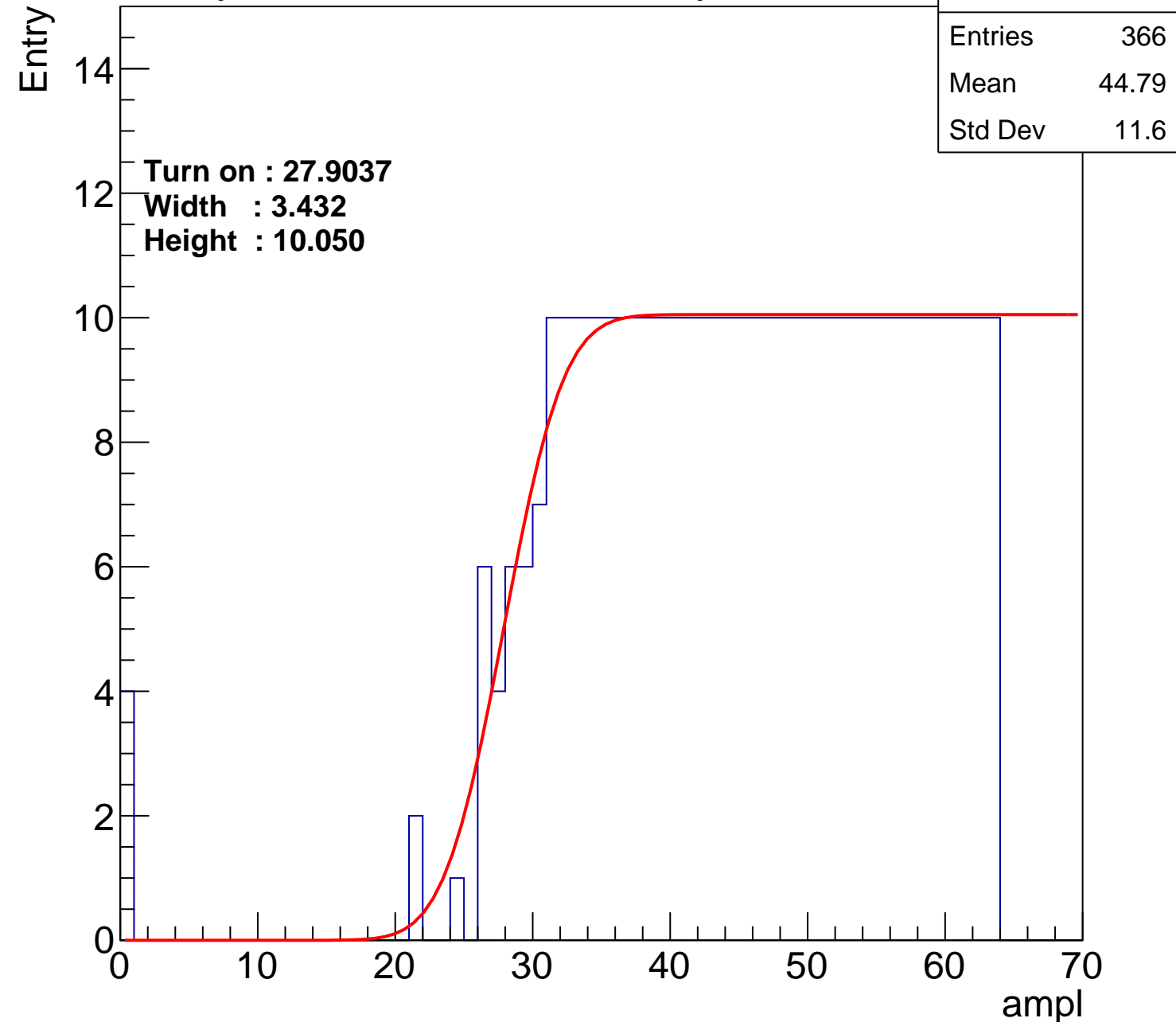
Width : 3.432

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch113

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.51
Std Dev	11.19

Turn on : 26.6739

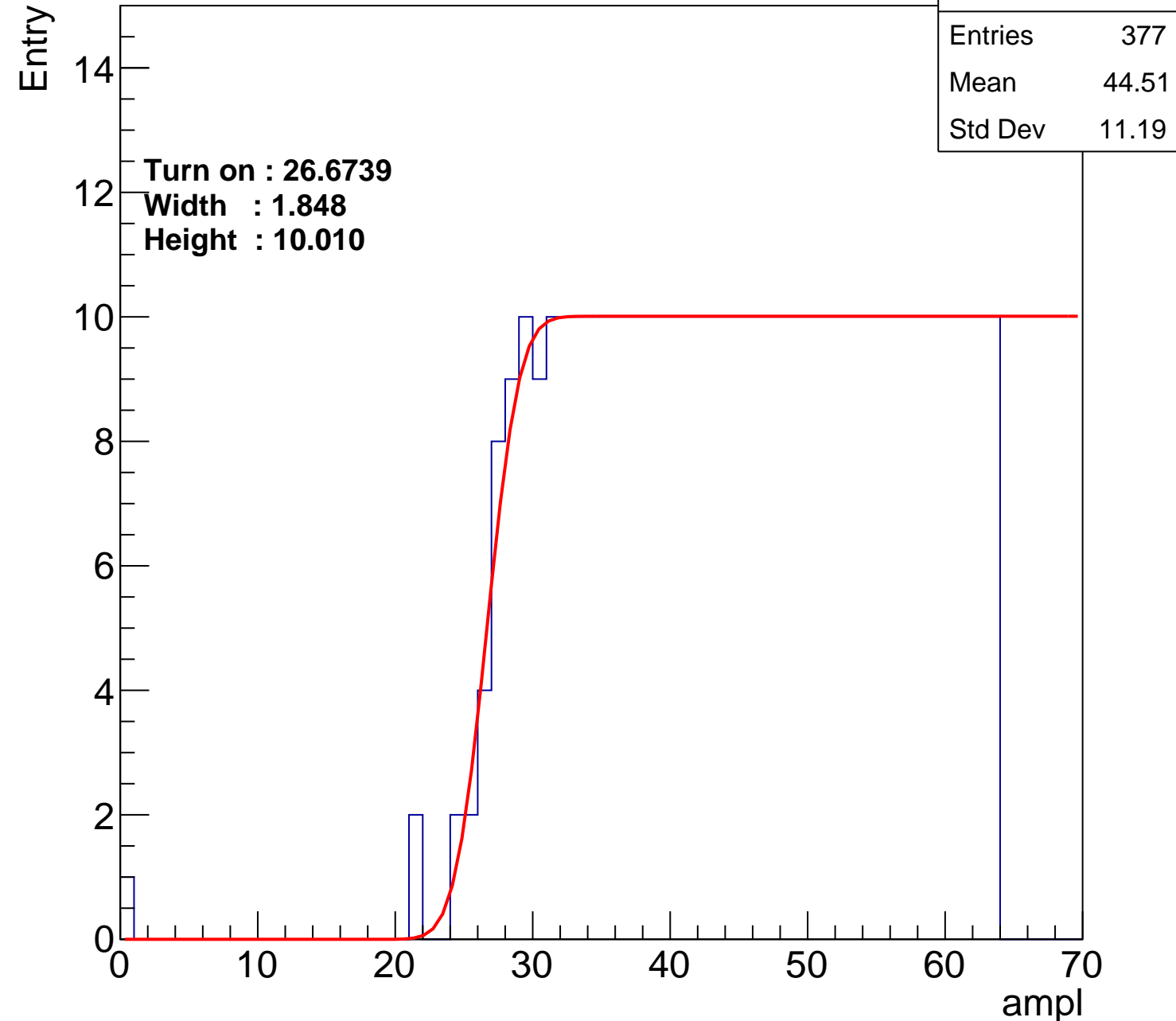
Width : 1.848

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch114

calib_packv5_042523_0143.root, FC#0, port D2

Entries	359
Mean	45.26
Std Dev	11.04

Turn on : 29.9762

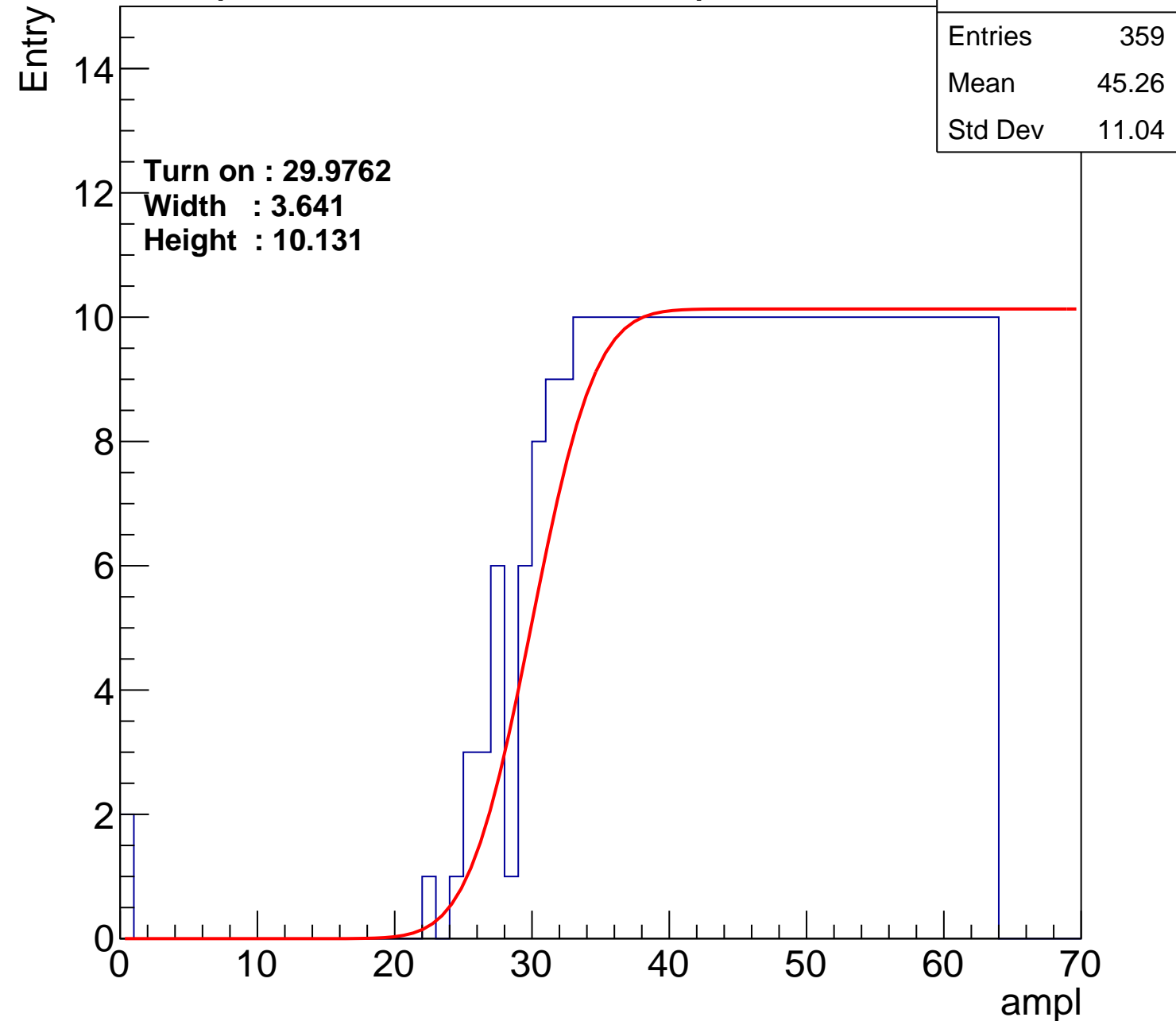
Width : 3.641

Height : 10.131

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch115

calib_packv5_042523_0143.root, FC#0, port D2

Entries	363
Mean	45.09
Std Dev	11.1

Turn on : 28.0916

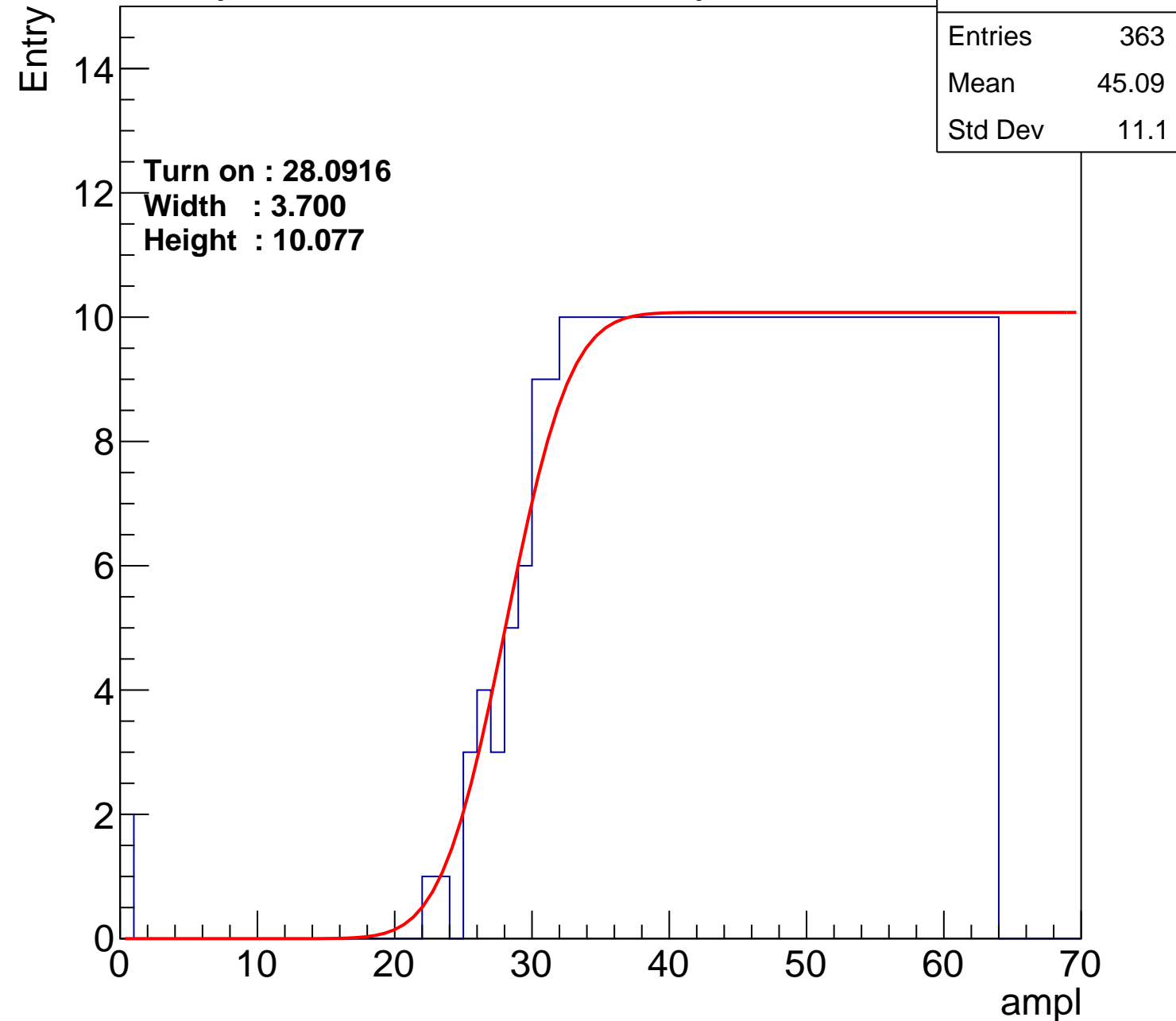
Width : 3.700

Height : 10.077

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch116

calib_packv5_042523_0143.root, FC#0, port D2

Entries	364
Mean	45.07
Std Dev	11.06

Turn on : 27.5023

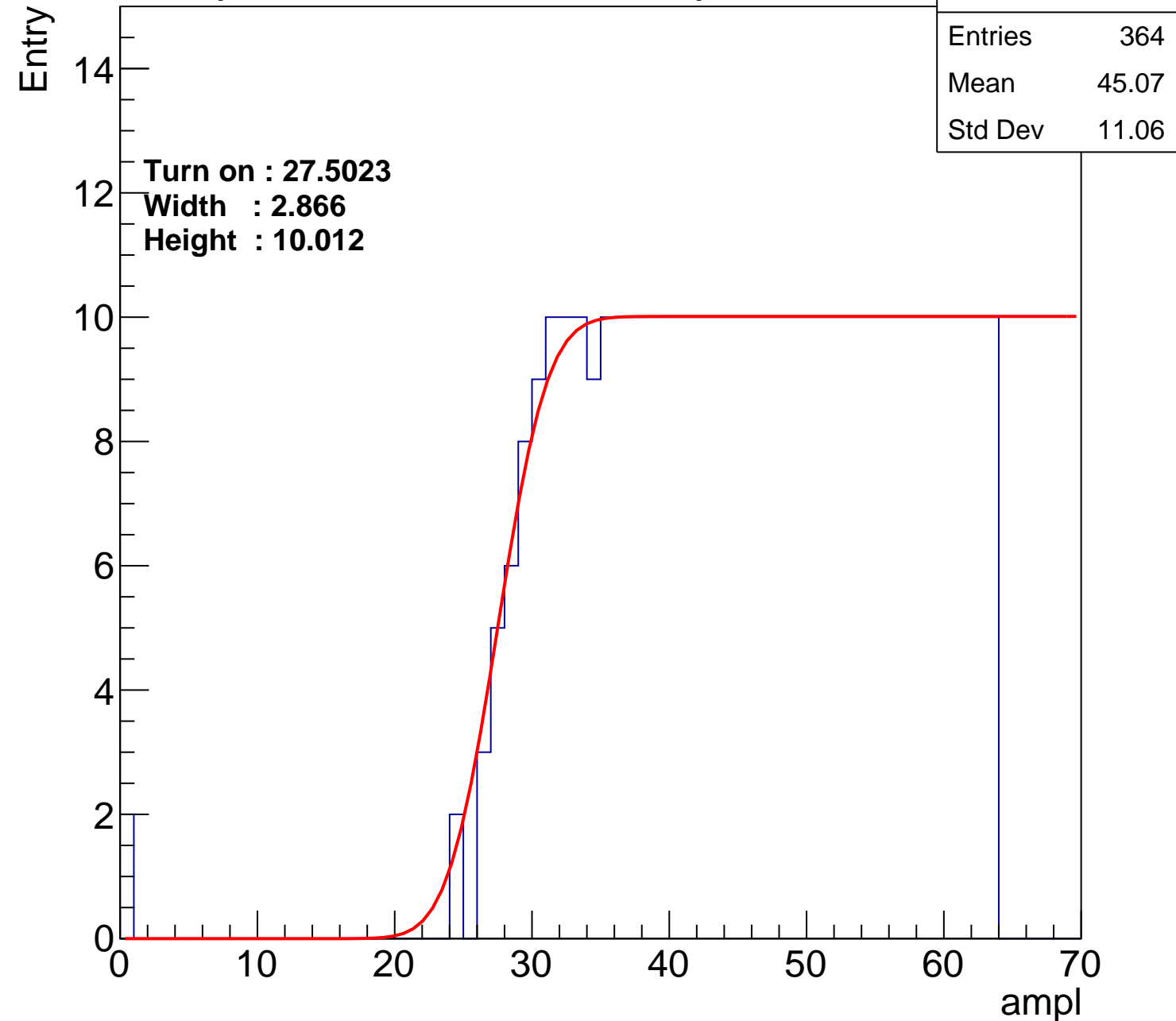
Width : 2.866

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch117

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.36
Std Dev	11.72

Turn on : 26.8330

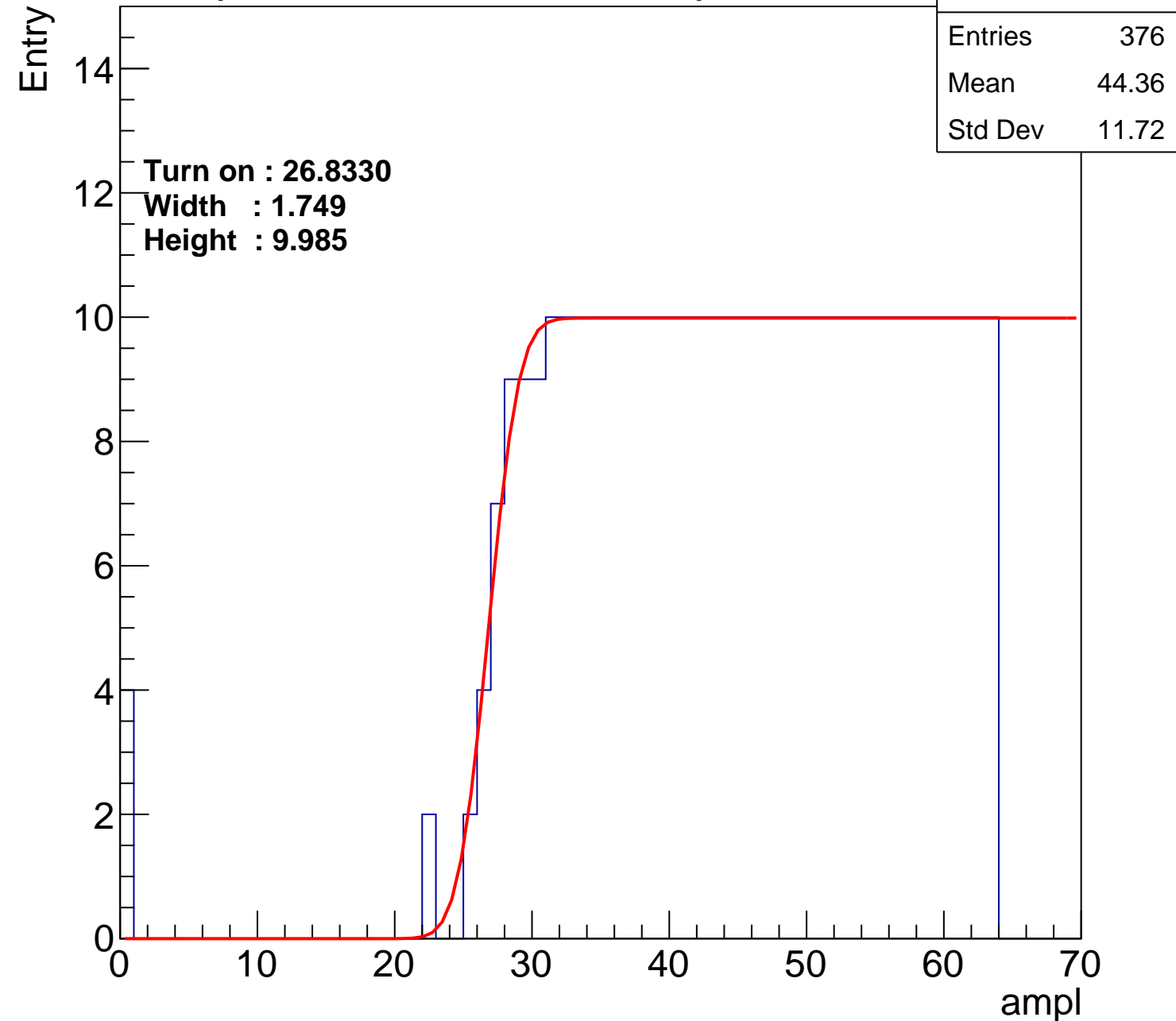
Width : 1.749

Height : 9.985

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch118

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.33
Std Dev	11.57

Turn on : 27.3842

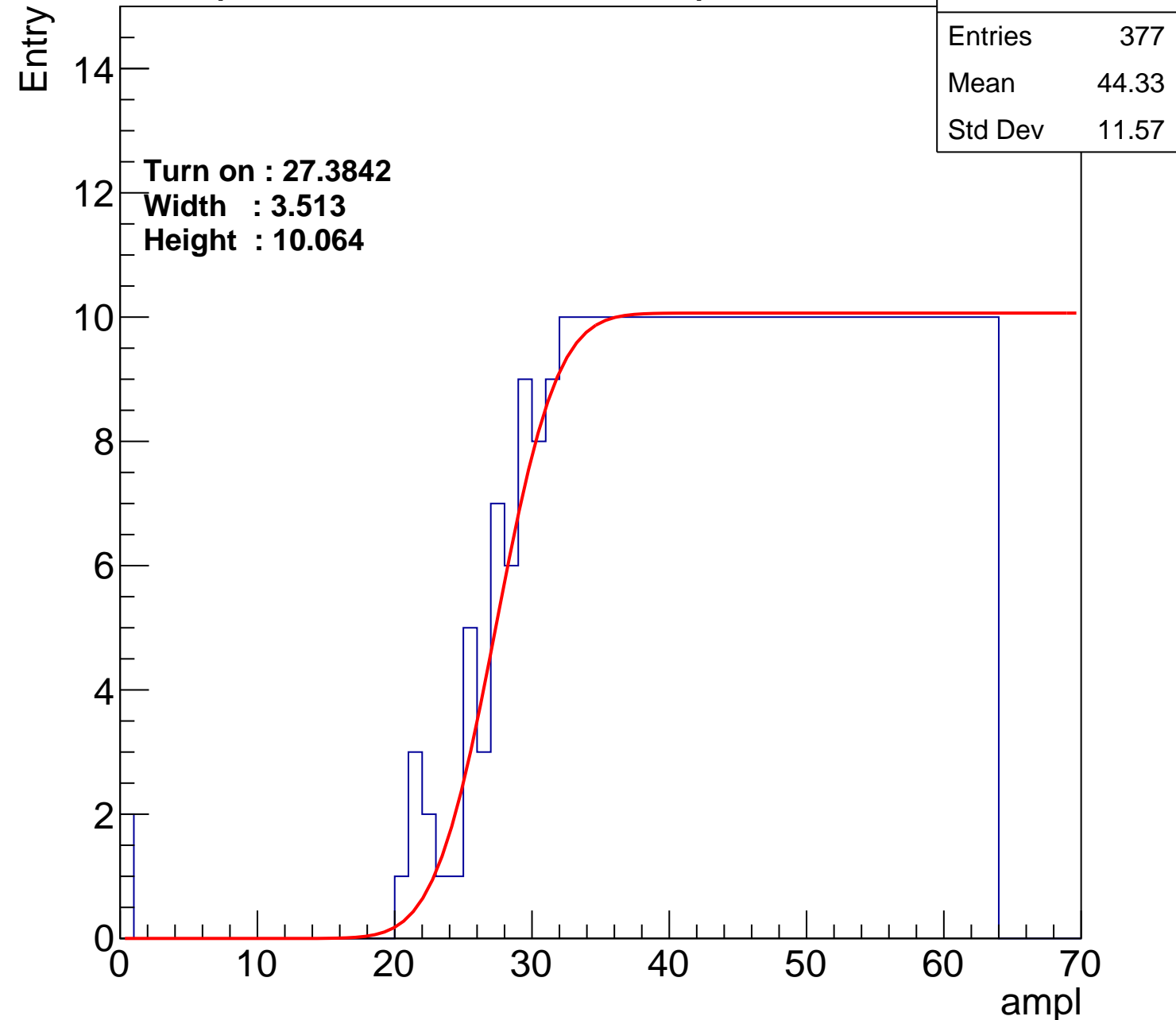
Width : 3.513

Height : 10.064

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch119

calib_packv5_042523_0143.root, FC#0, port D2

Entries	351
Mean	45.54
Std Dev	11.22

Turn on : 29.3779

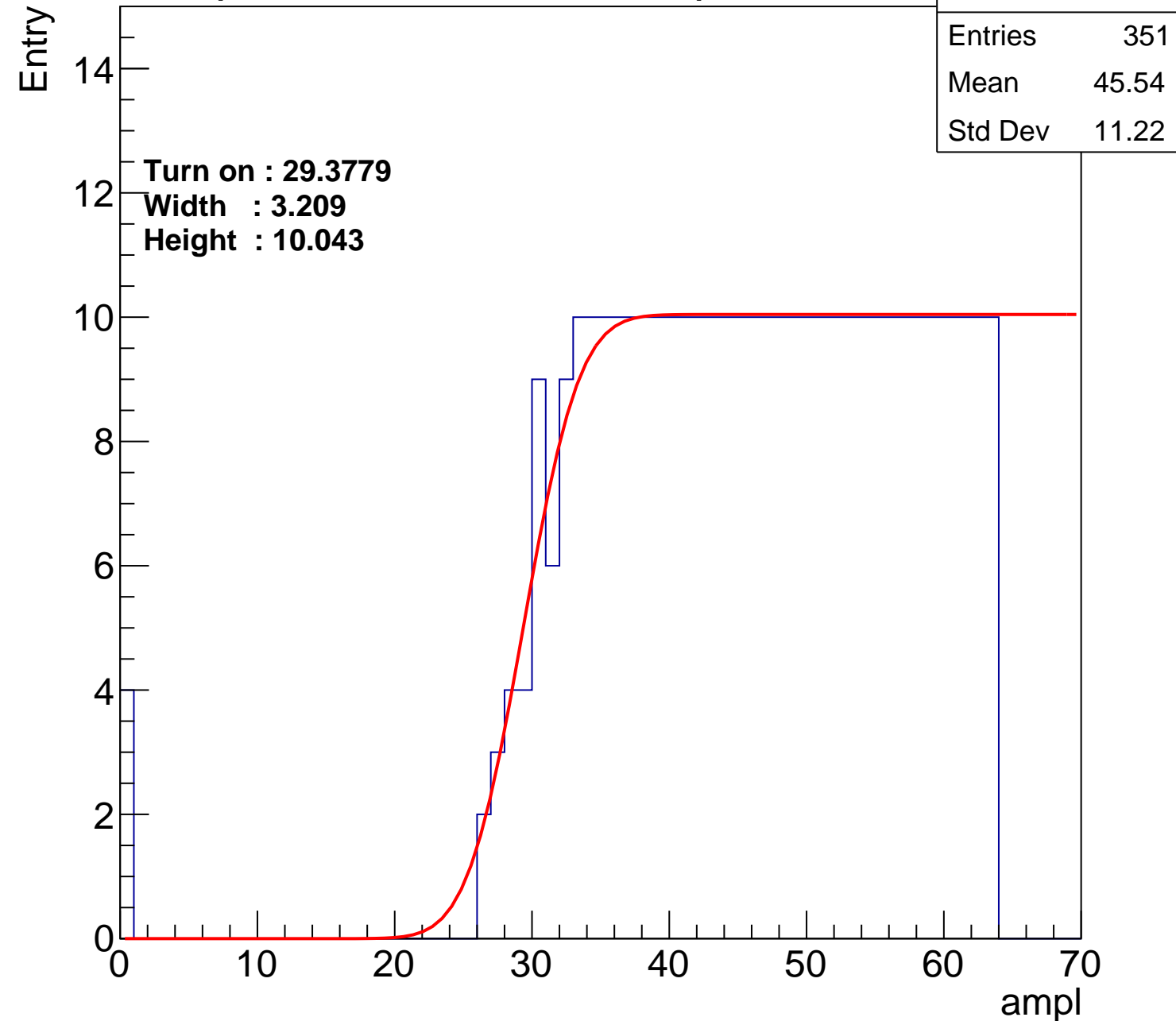
Width : 3.209

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch120

calib_packv5_042523_0143.root, FC#0, port D2

Entries	372
Mean	44.59
Std Dev	11.49

Turn on : 26.9677

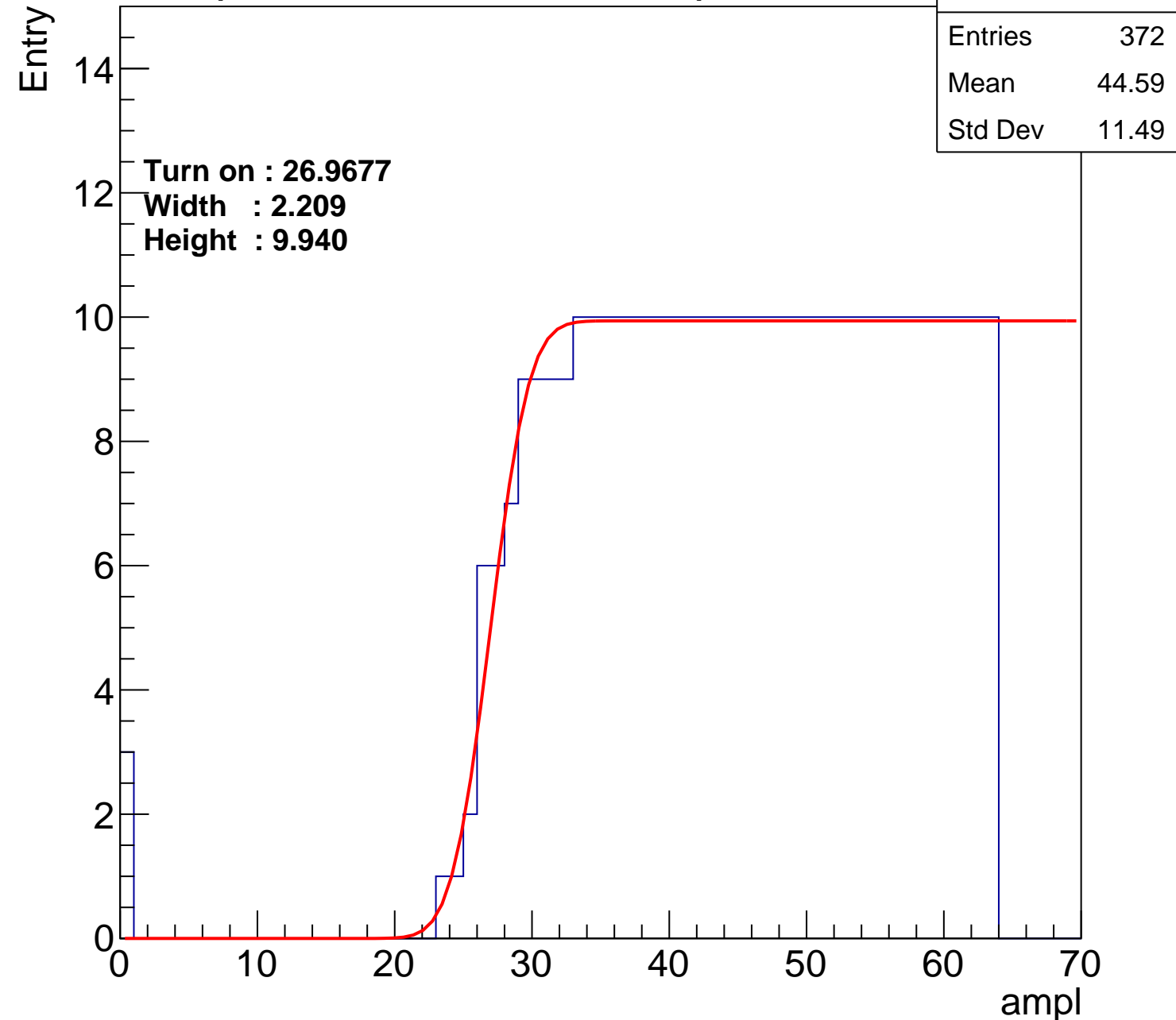
Width : 2.209

Height : 9.940

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch121

calib_packv5_042523_0143.root, FC#0, port D2

Entries	369
Mean	44.7
Std Dev	11.47

Turn on : 27.6998

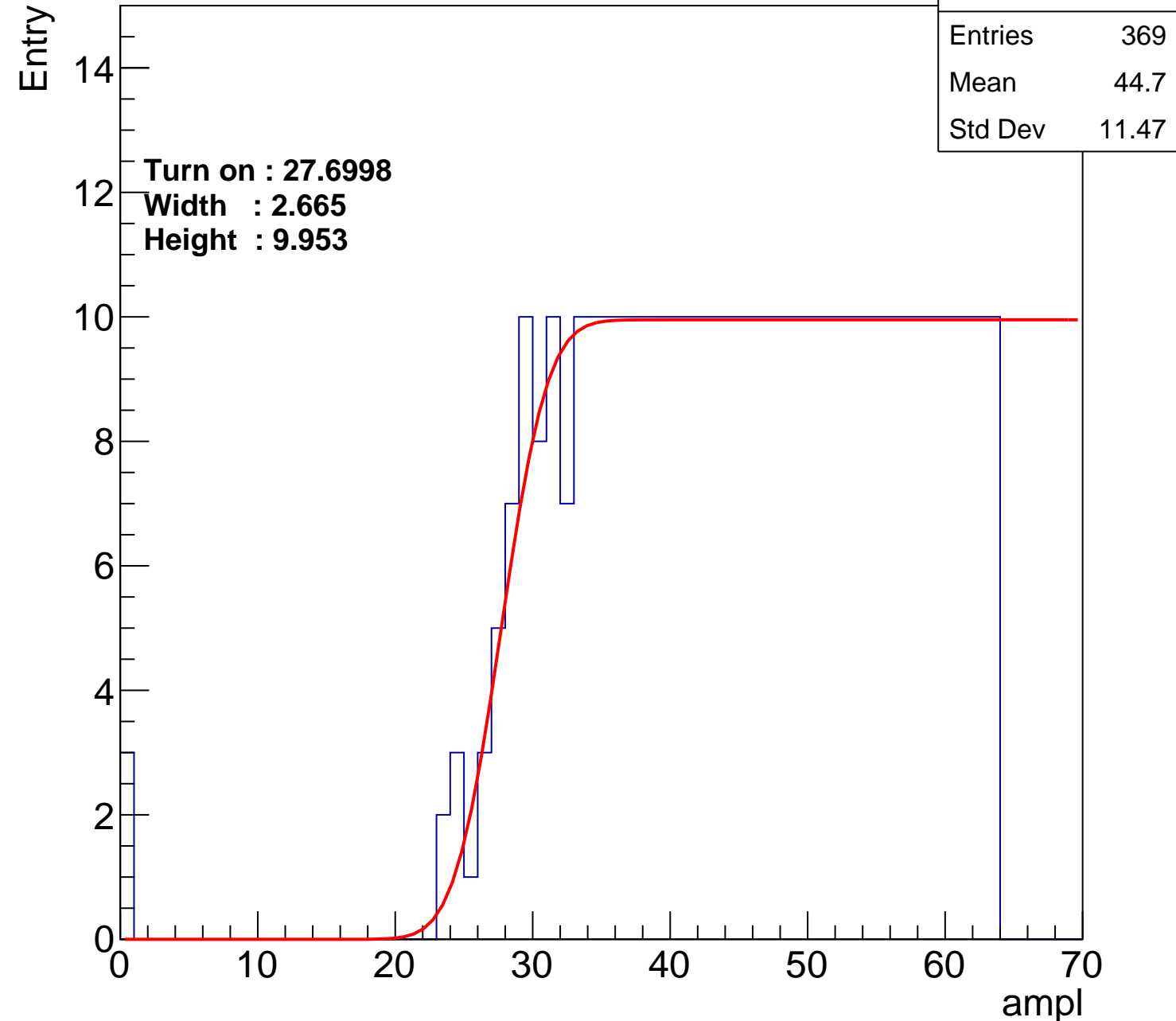
Width : 2.665

Height : 9.953

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch122

calib_packv5_042523_0143.root, FC#0, port D2

Entries	363
Mean	45.11
Std Dev	10.98

Turn on : 27.5137

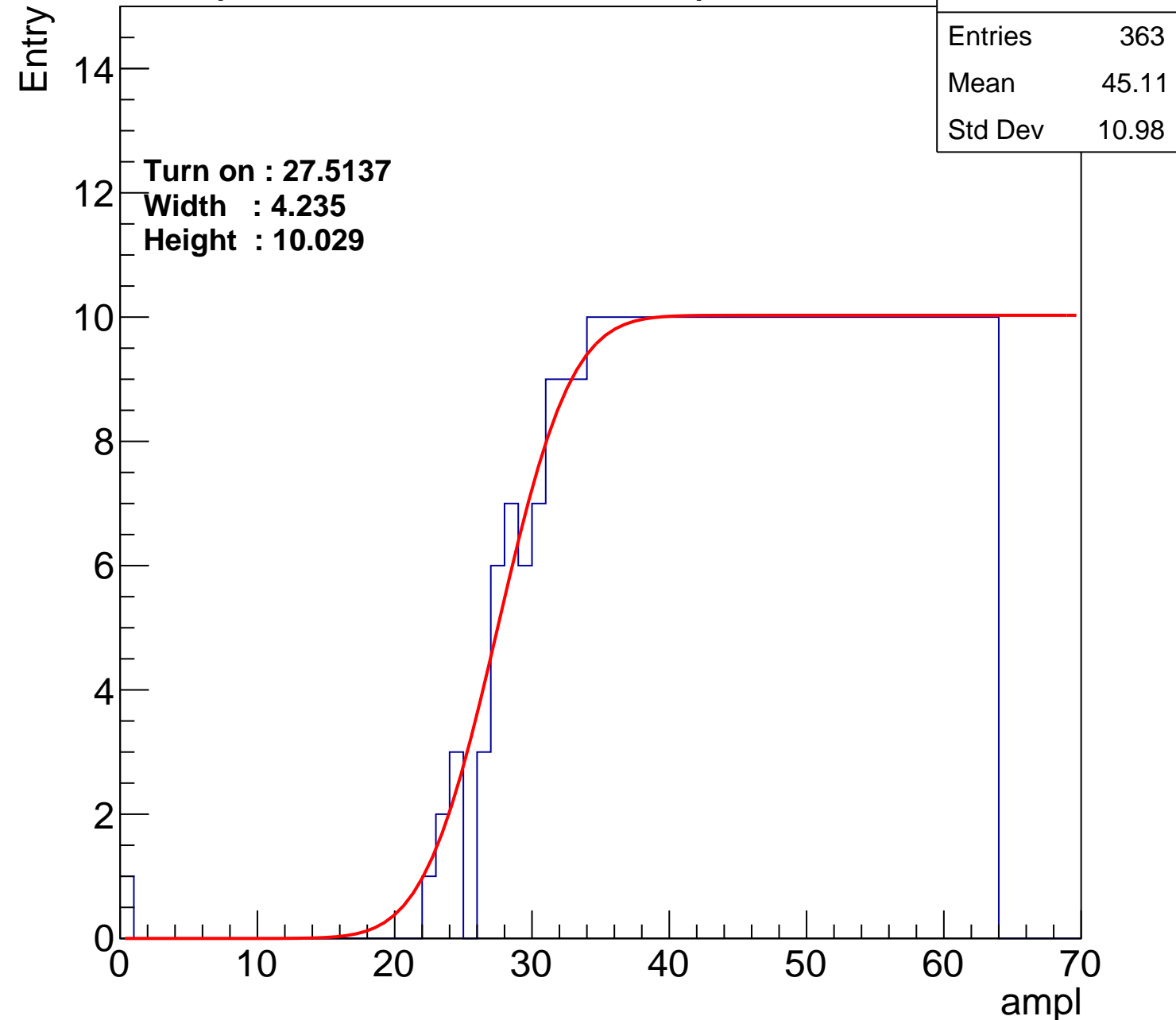
Width : 4.235

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch123

calib_packv5_042523_0143.root, FC#0, port D2

Entries	359
Mean	45.04
Std Dev	11.68

Turn on : 29.0631

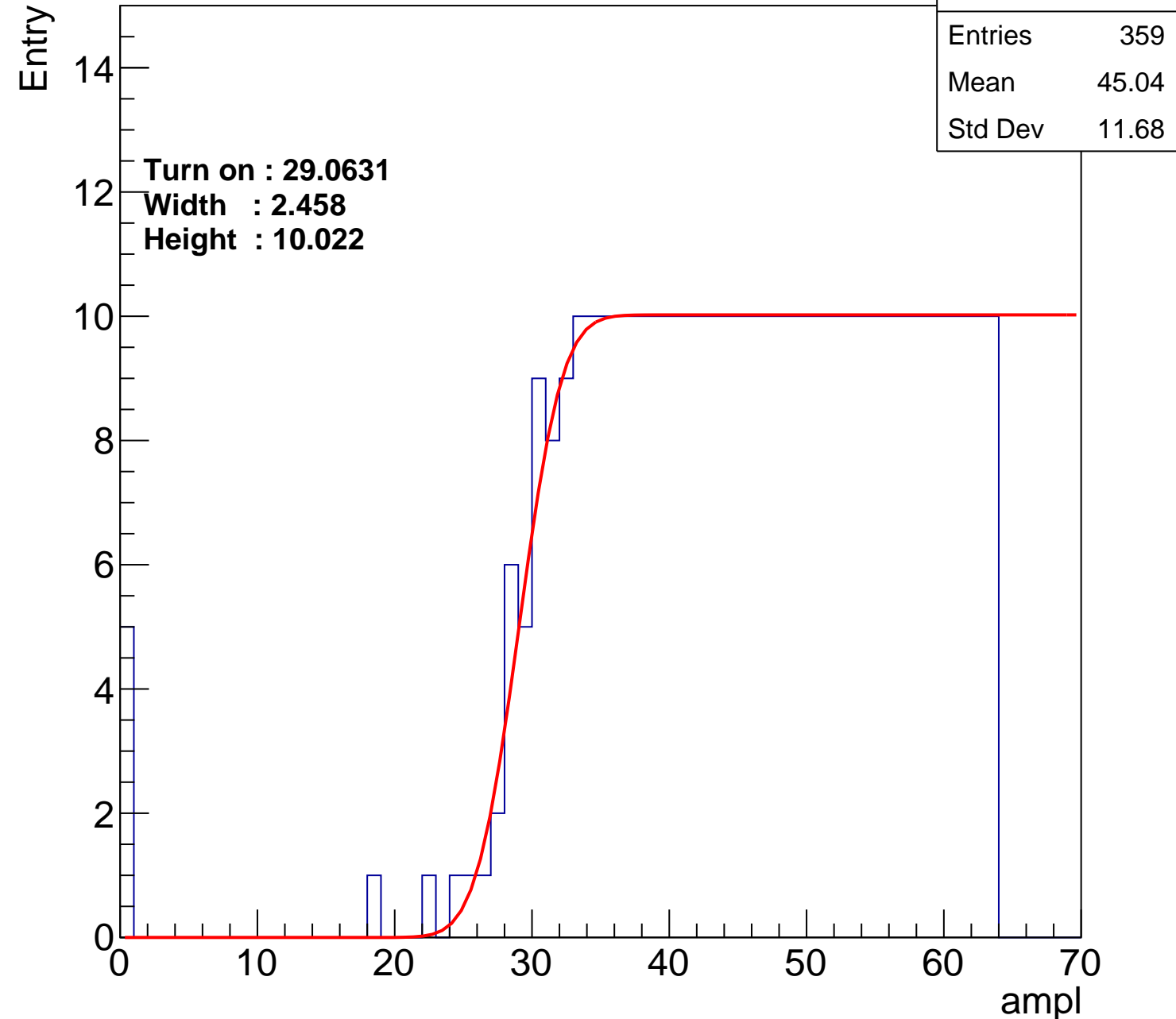
Width : 2.458

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch124

calib_packv5_042523_0143.root, FC#0, port D2

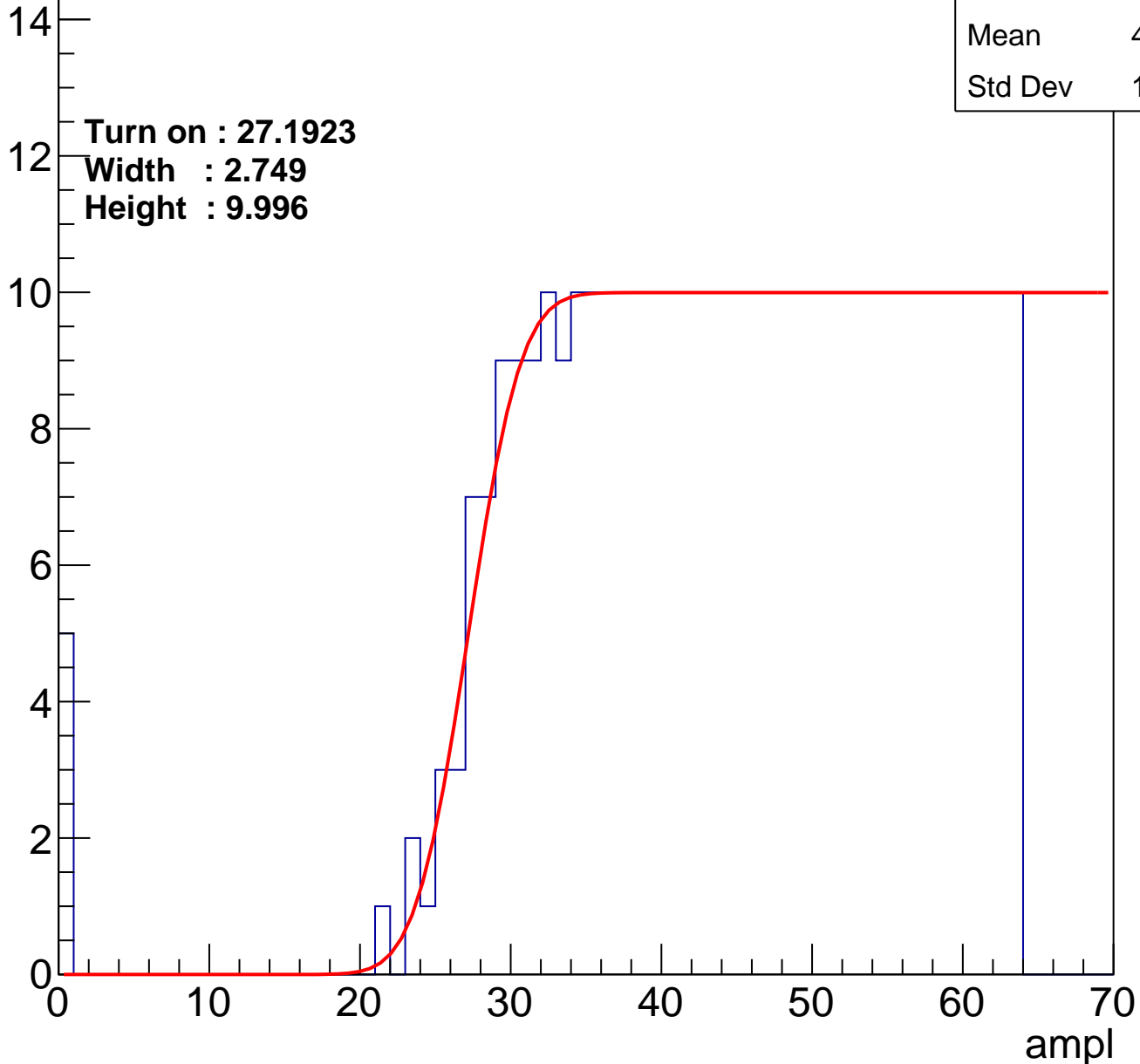
Entries	375
Mean	44.28
Std Dev	11.97

Turn on : 27.1923

Width : 2.749

Height : 9.996

Entry



B1L101S, U11-ch125

calib_packv5_042523_0143.root, FC#0, port D2

Entries	370
Mean	44.68
Std Dev	11.37

Turn on : 27.4104

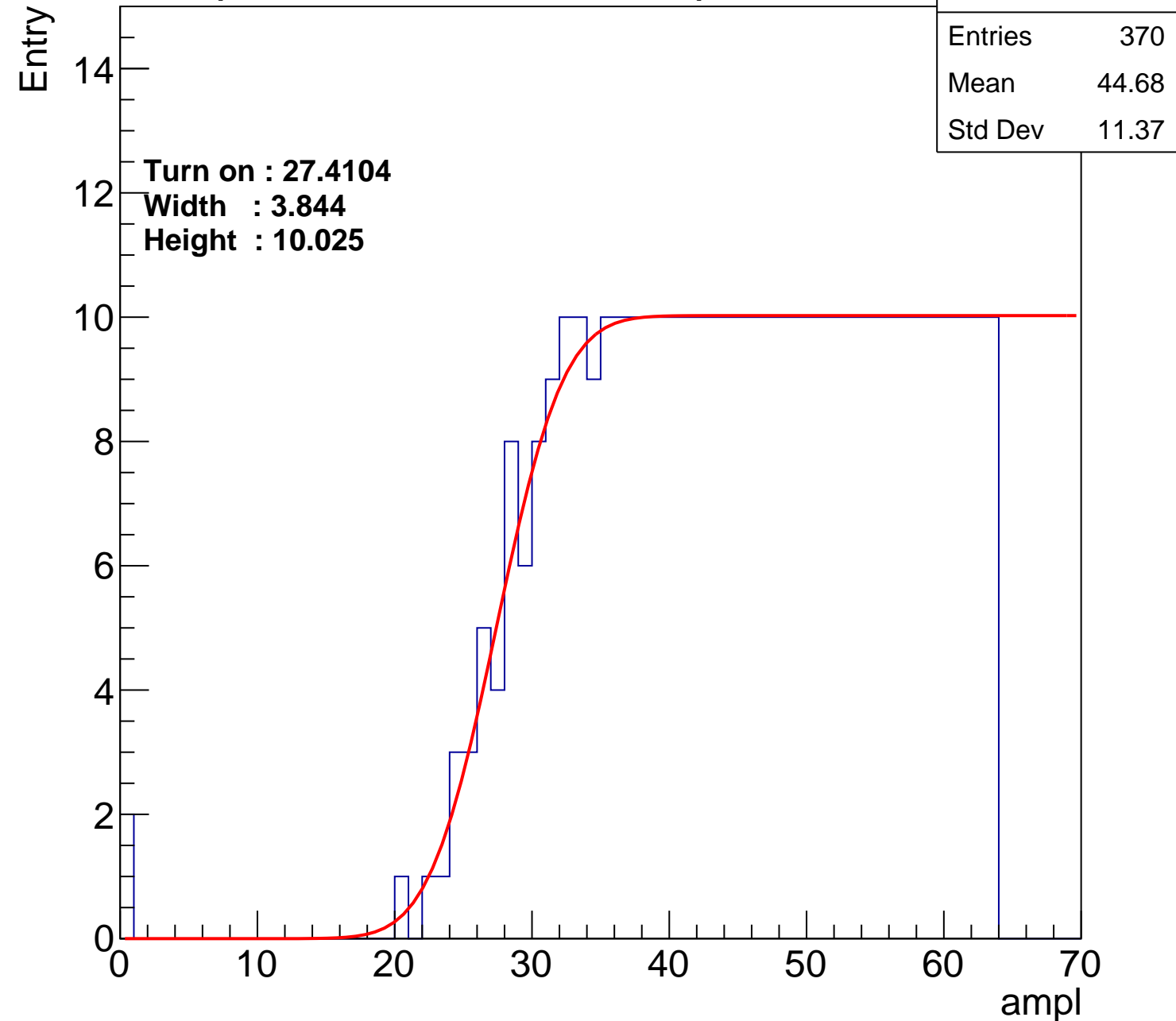
Width : 3.844

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch126

calib_packv5_042523_0143.root, FC#0, port D2

Entries	400
Mean	43.24
Std Dev	12.31

Turn on : 24.8897

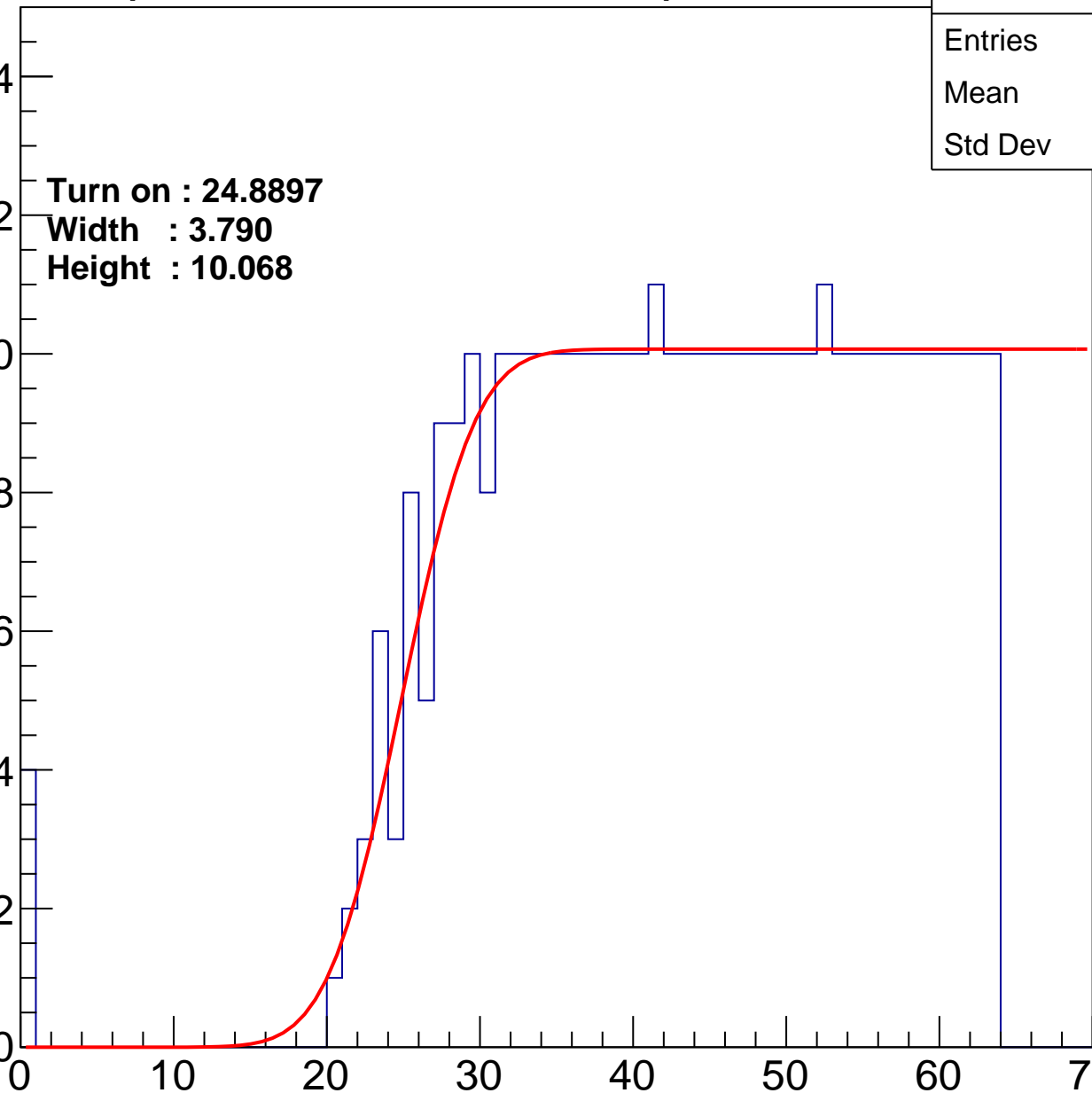
Width : 3.790

Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch127

calib_packv5_042523_0143.root, FC#0, port D2

Entries	391
Mean	43.58
Std Dev	12.15

Turn on : 25.2118

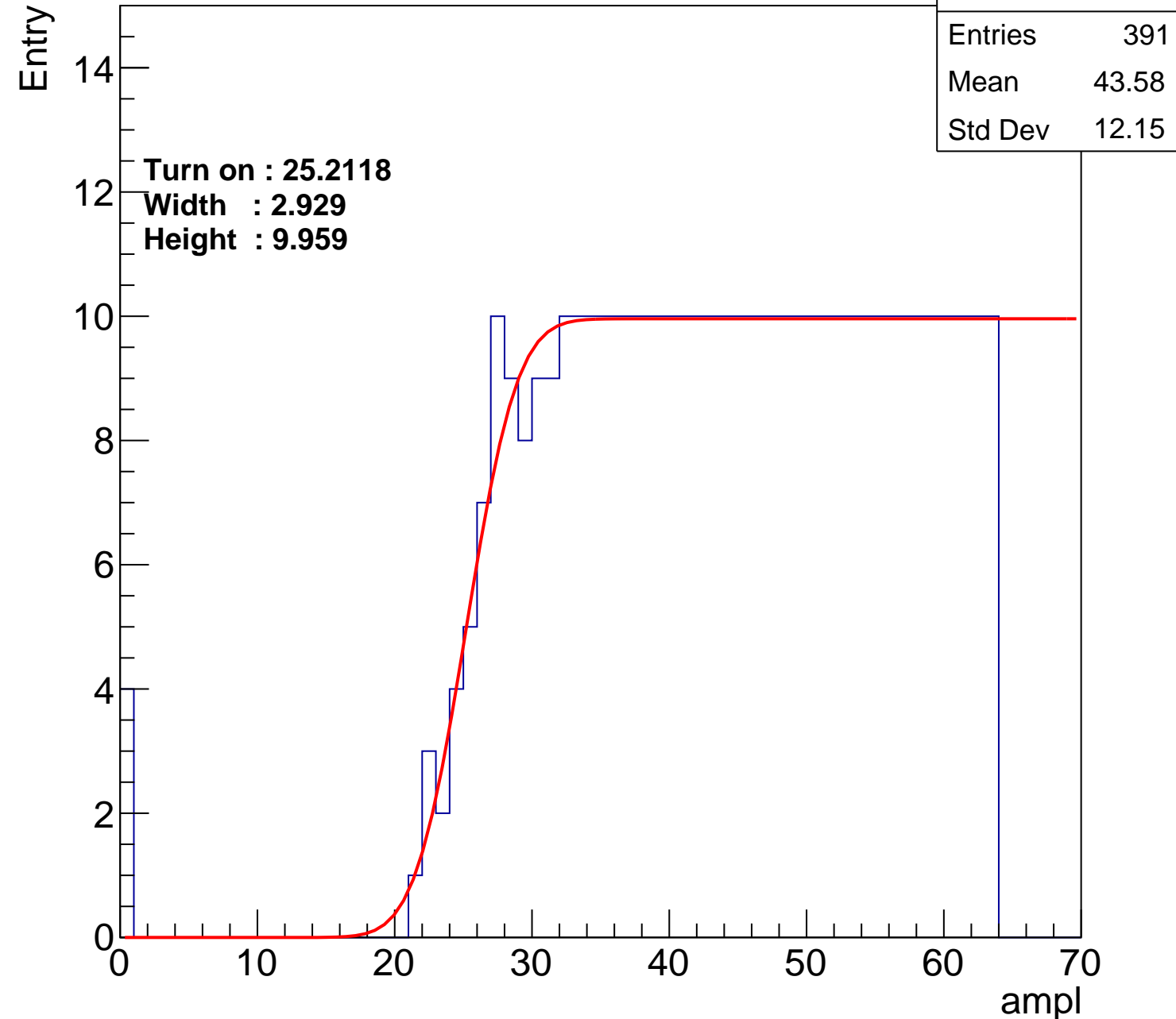
Width : 2.929

Height : 9.959

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U11-ch127

calib_packv5_042523_0143.root, FC#0, port D2

Entries	391
Mean	43.58
Std Dev	12.15

Turn on : 25.2118

Width : 2.929

Height : 9.959

Entry

14
12
10
8
6
4
2
0

ampl

