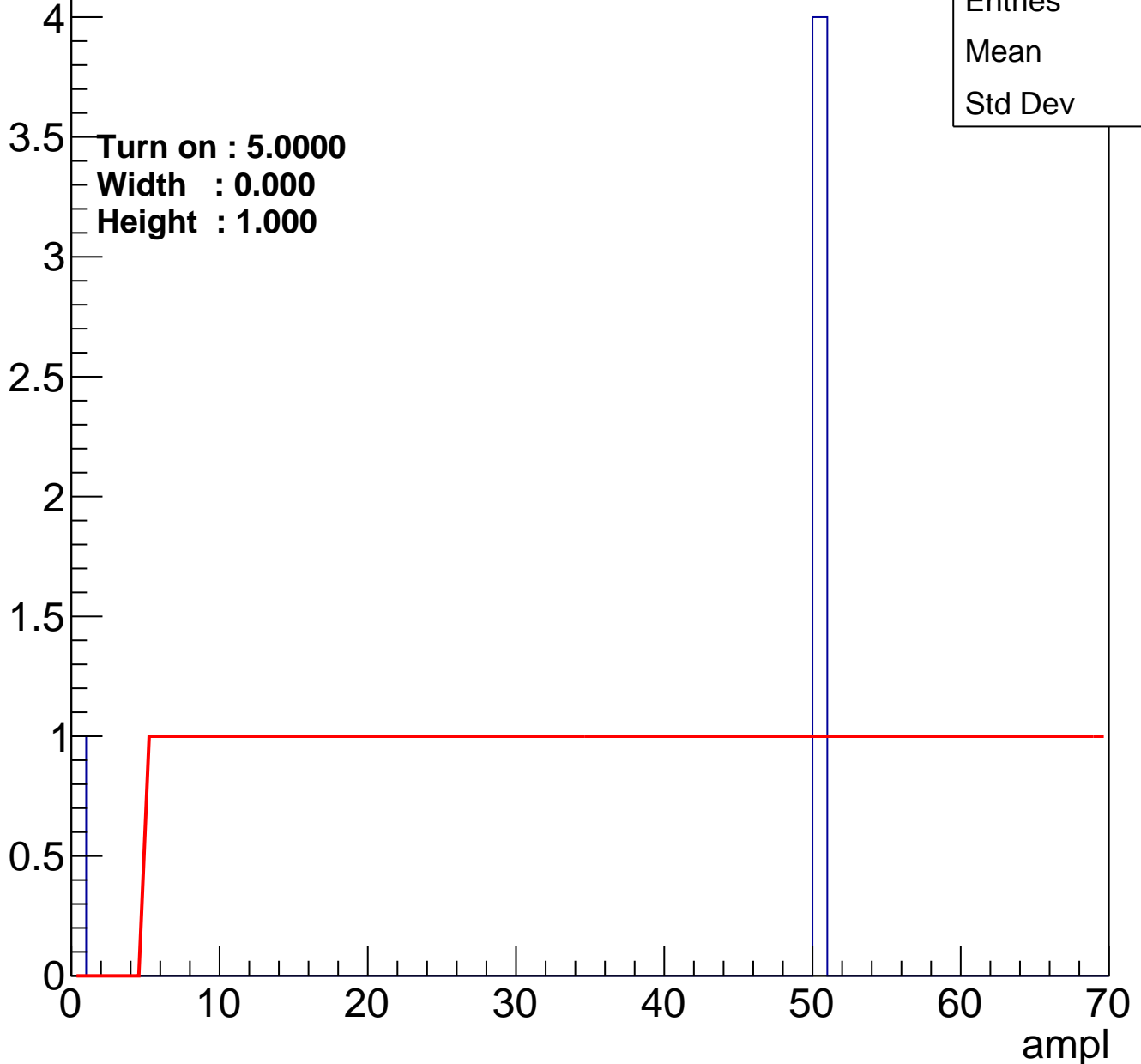




# B0L100S, U3-ch0

calib\_packv5\_042523\_0143.root, FC#6, port A1

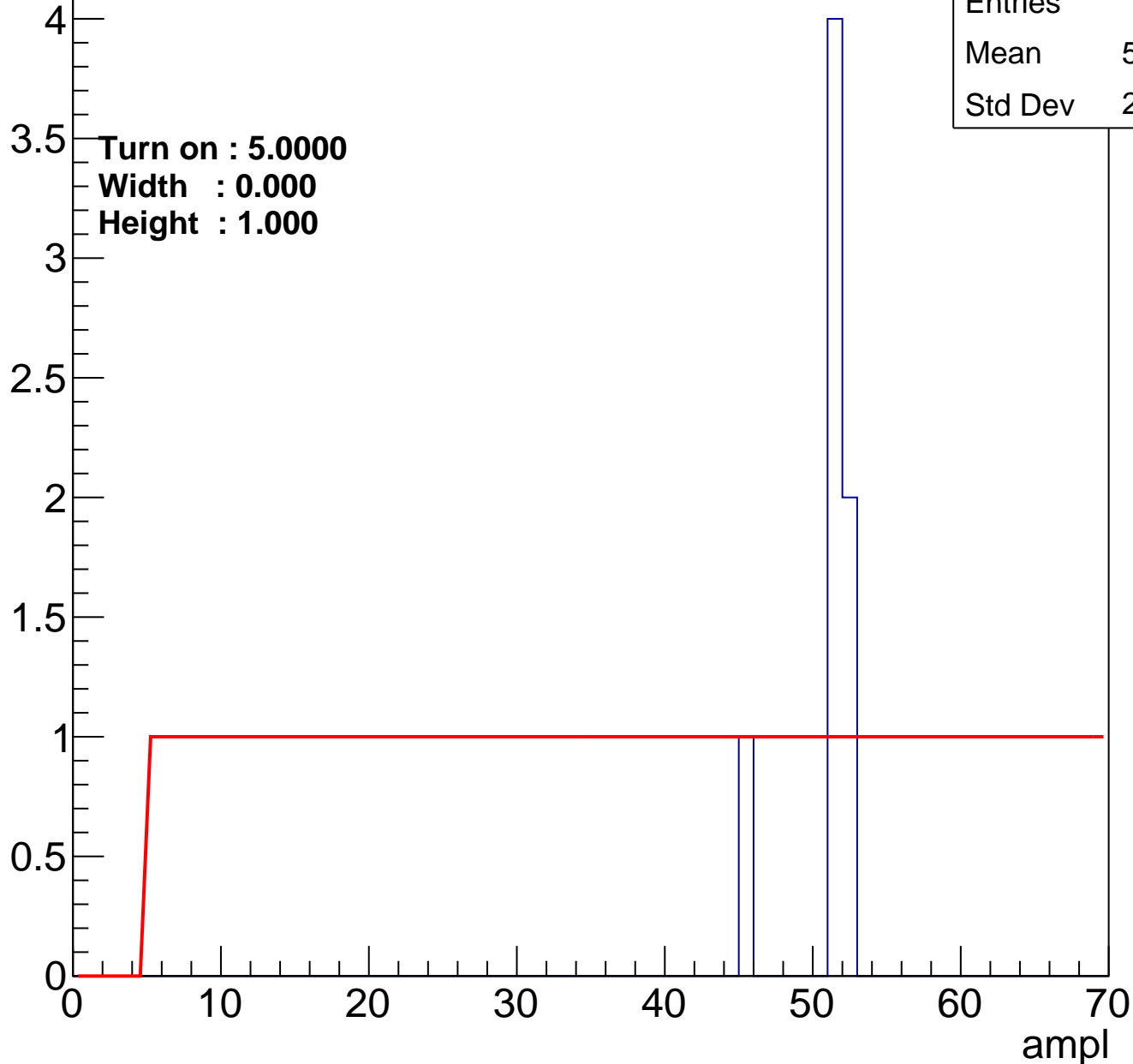
Entry



# B0L100S, U3-ch1

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	7
Mean	50.43
Std Dev	2.259

# B0L100S, U3-ch2

calib\_packv5\_042523\_0143.root, FC#6, port A1

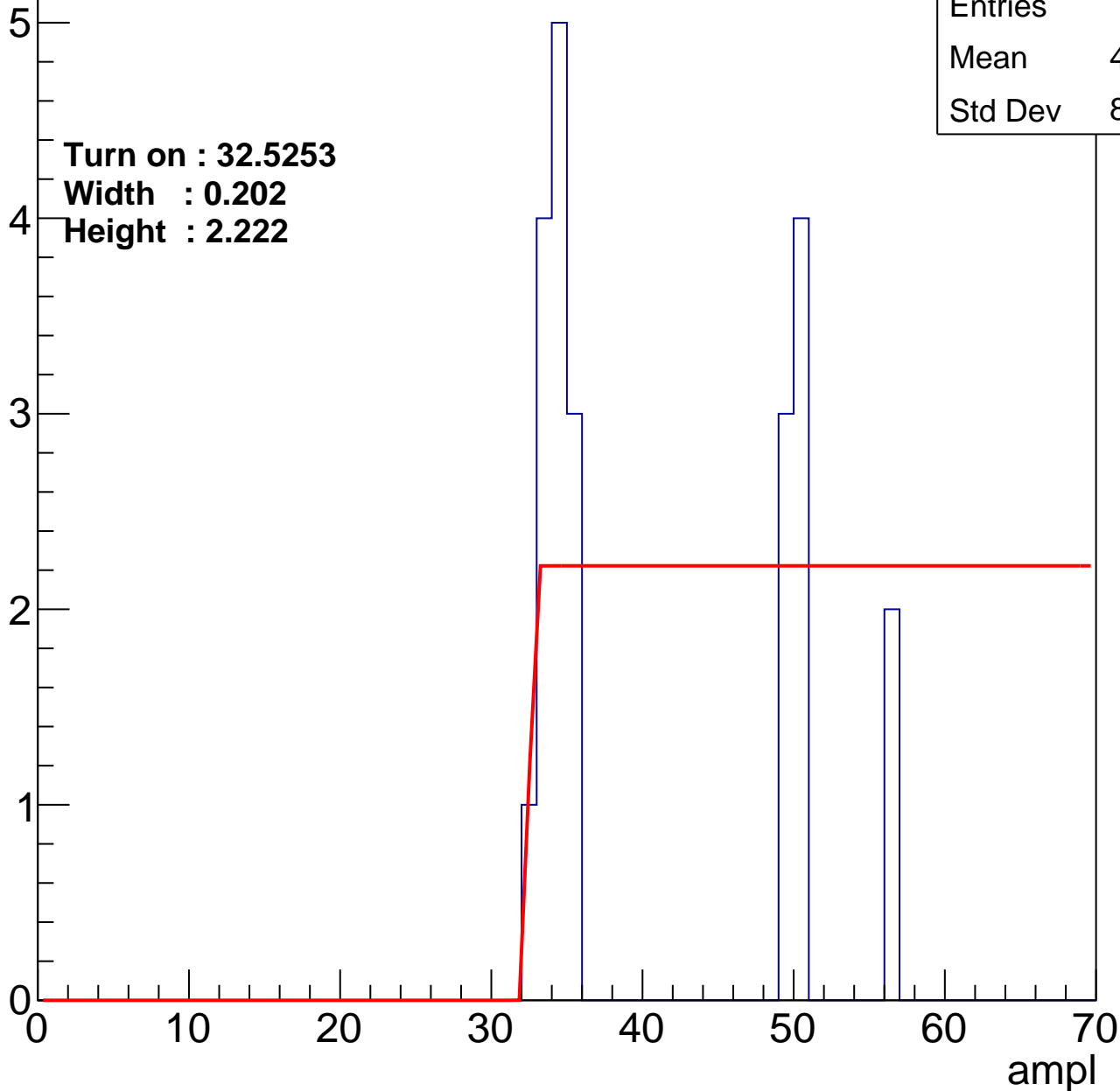
Entry

Entries	22
Mean	40.82
Std Dev	8.674

Turn on : 32.5253

Width : 0.202

Height : 2.222



# B0L100S, U3-ch3

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U3-ch4

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

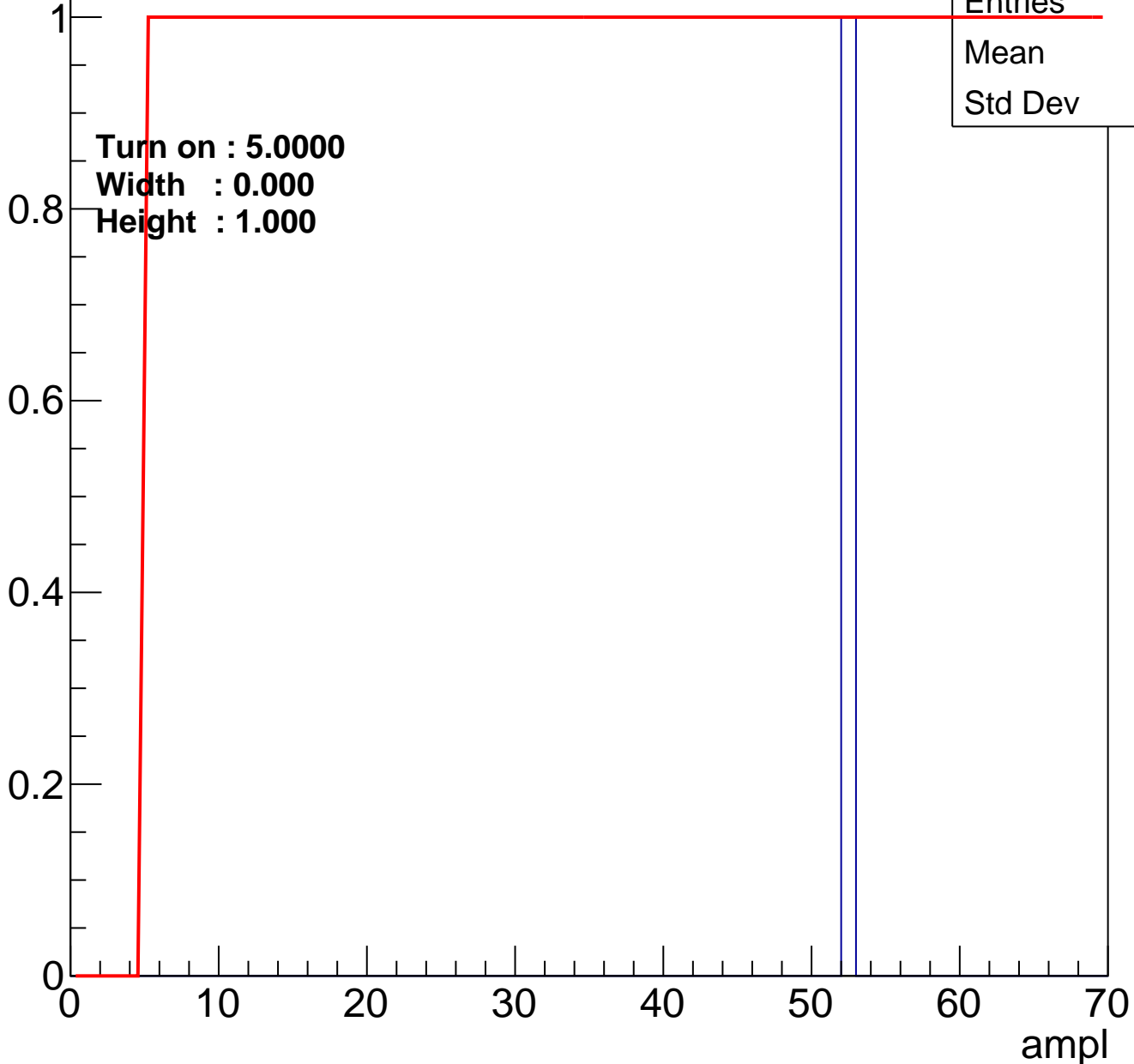


Entries	0
Mean	0
Std Dev	0

# B0L100S, U3-ch5

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U3-ch6

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L100S, U3-ch7

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U3-ch8

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U3-ch9

calib\_packv5\_042523\_0143.root, FC#6, port A1

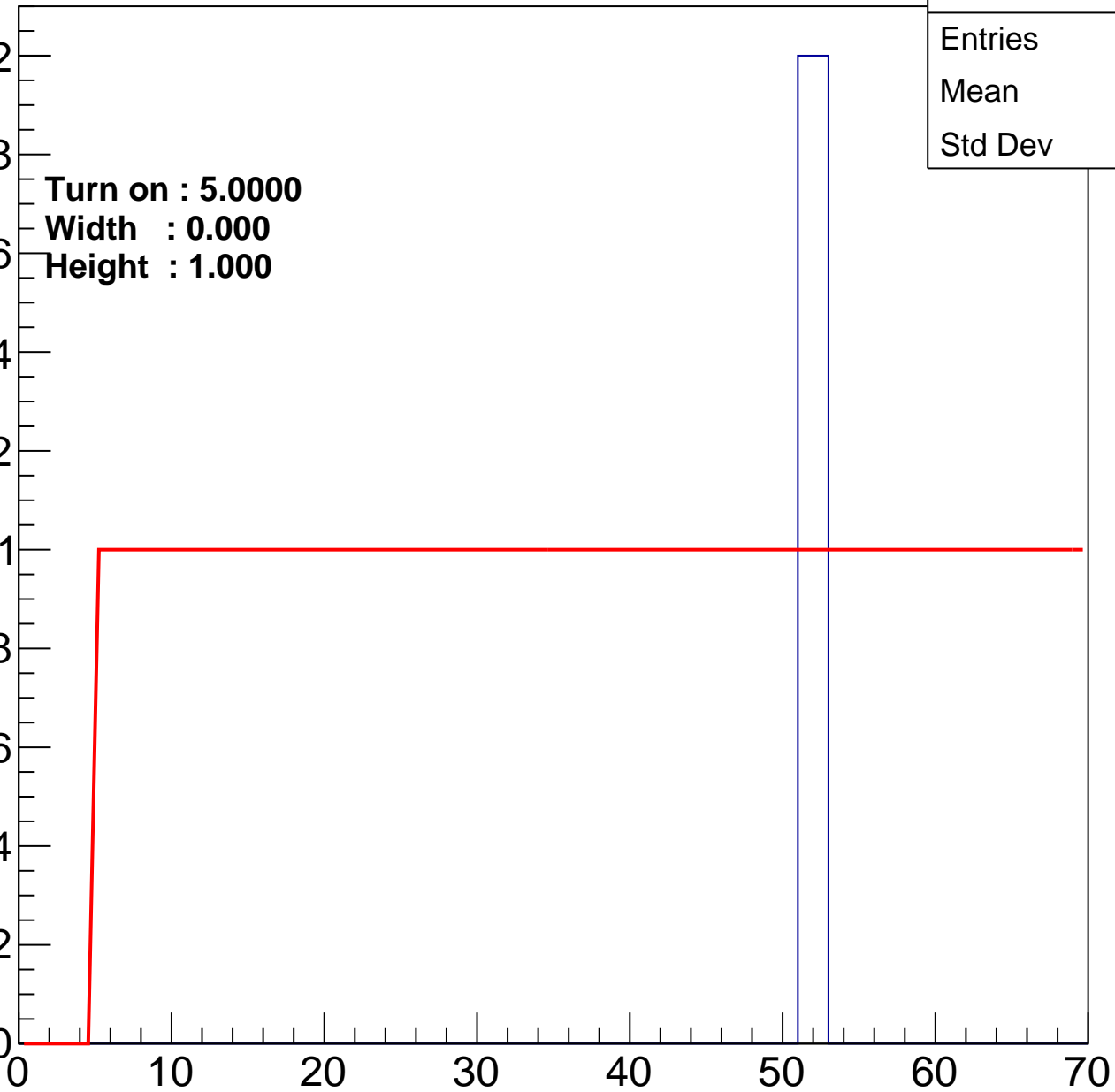
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Turn on : 5.0000  
Width : 0.000  
Height : 1.000

Entries	4
Mean	51.5
Std Dev	0.5

ampl



# B0L100S, U3-ch10

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

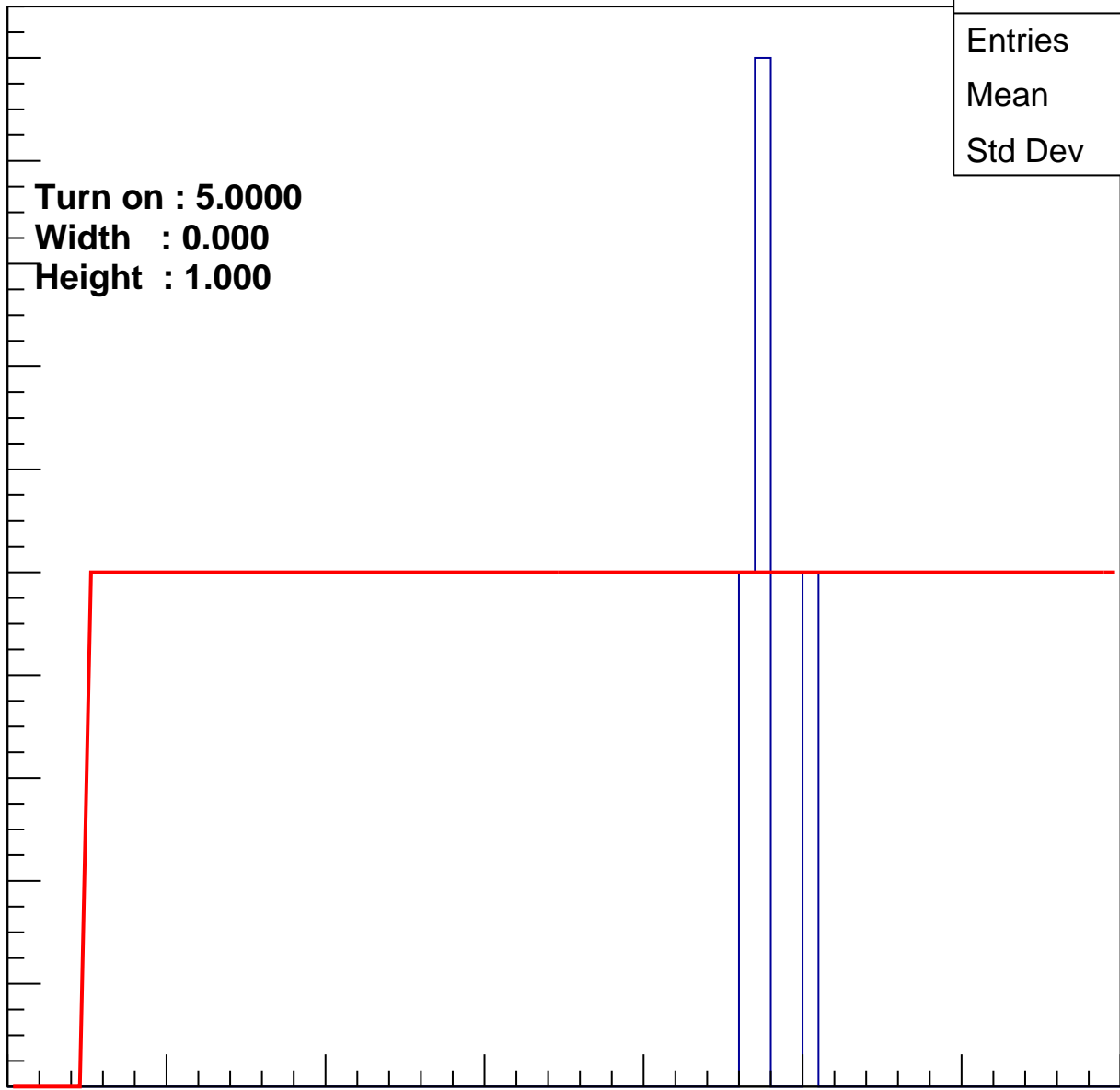
2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Turn on : 5.0000  
Width : 0.000  
Height : 1.000

Entries	4
Mean	47.5
Std Dev	1.5

0 10 20 30 40 50 60 70

ampl



# B0L100S, U3-ch11

calib\_packv5\_042523\_0143.root, FC#6, port A1

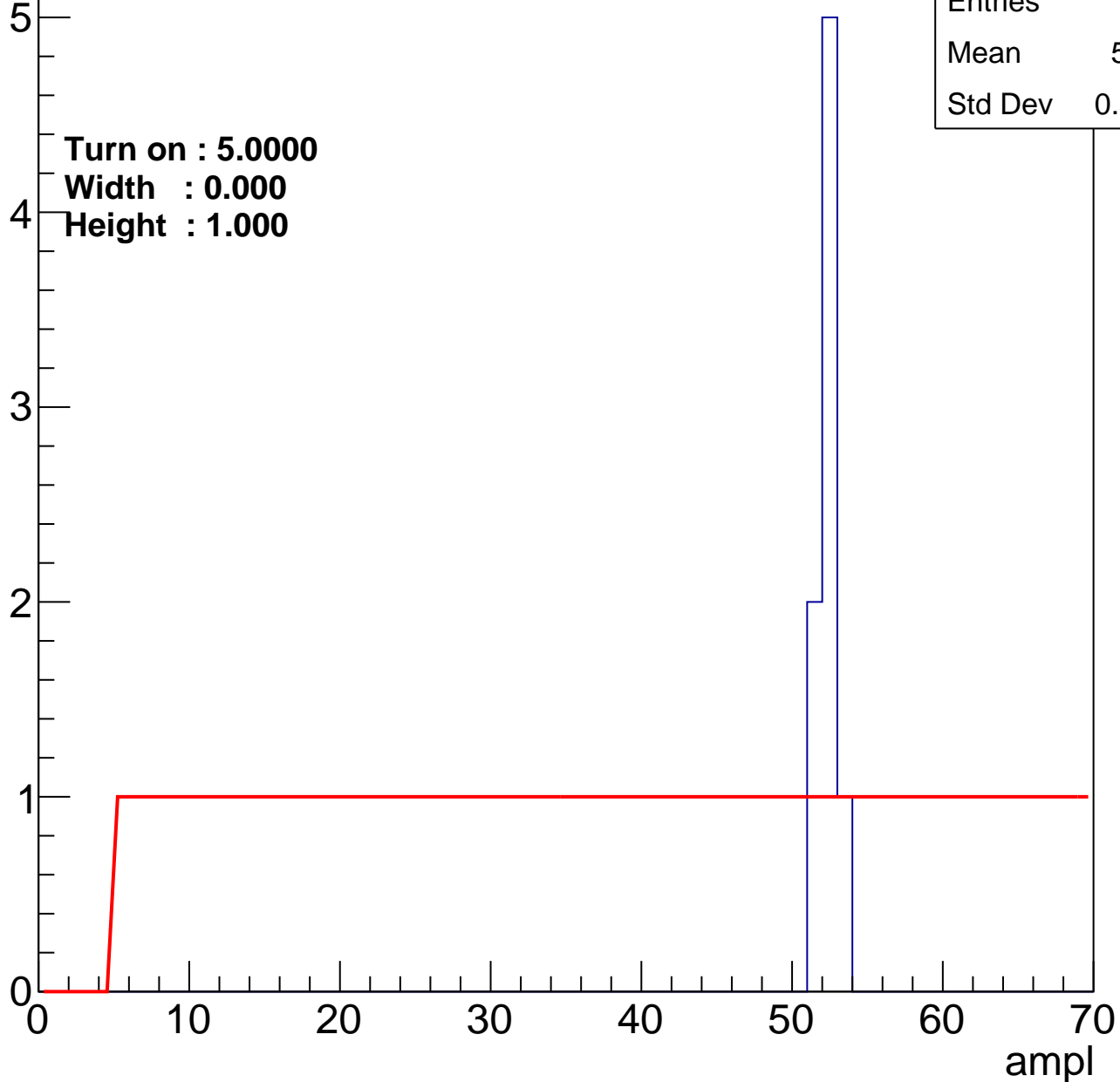
Entry



# B0L100S, U3-ch12

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	8
Mean	51.88
Std Dev	0.5995

# B0L100S, U3-ch13

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U3-ch14

calib\_packv5\_042523\_0143.root, FC#6, port A1

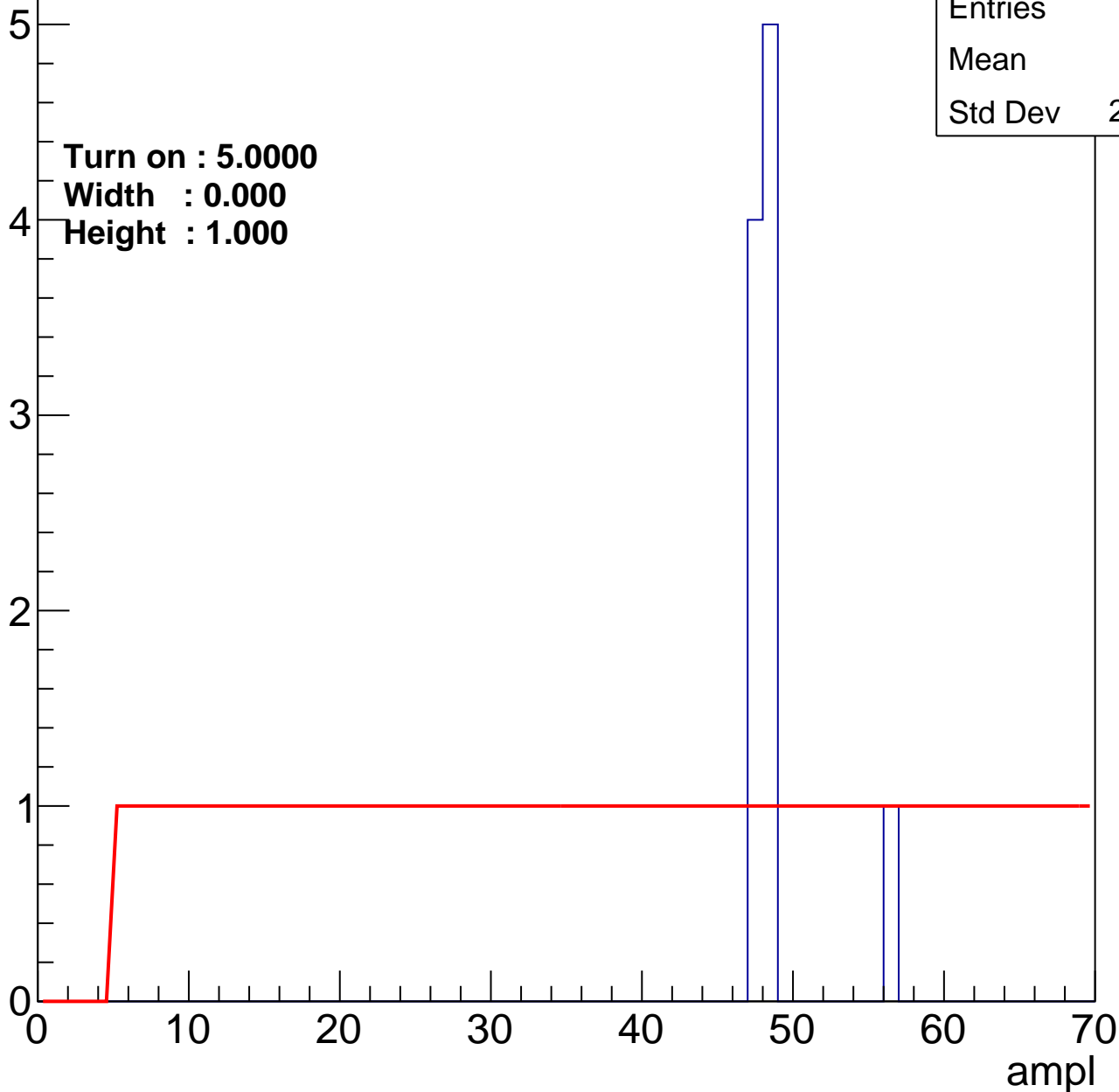
Entry

Entries	10
Mean	48.4
Std Dev	2.577

Turn on : 5.0000

Width : 0.000

Height : 1.000





# B0L100S, U3-ch15

calib\_packv5\_042523\_0143.root, FC#6, port A1

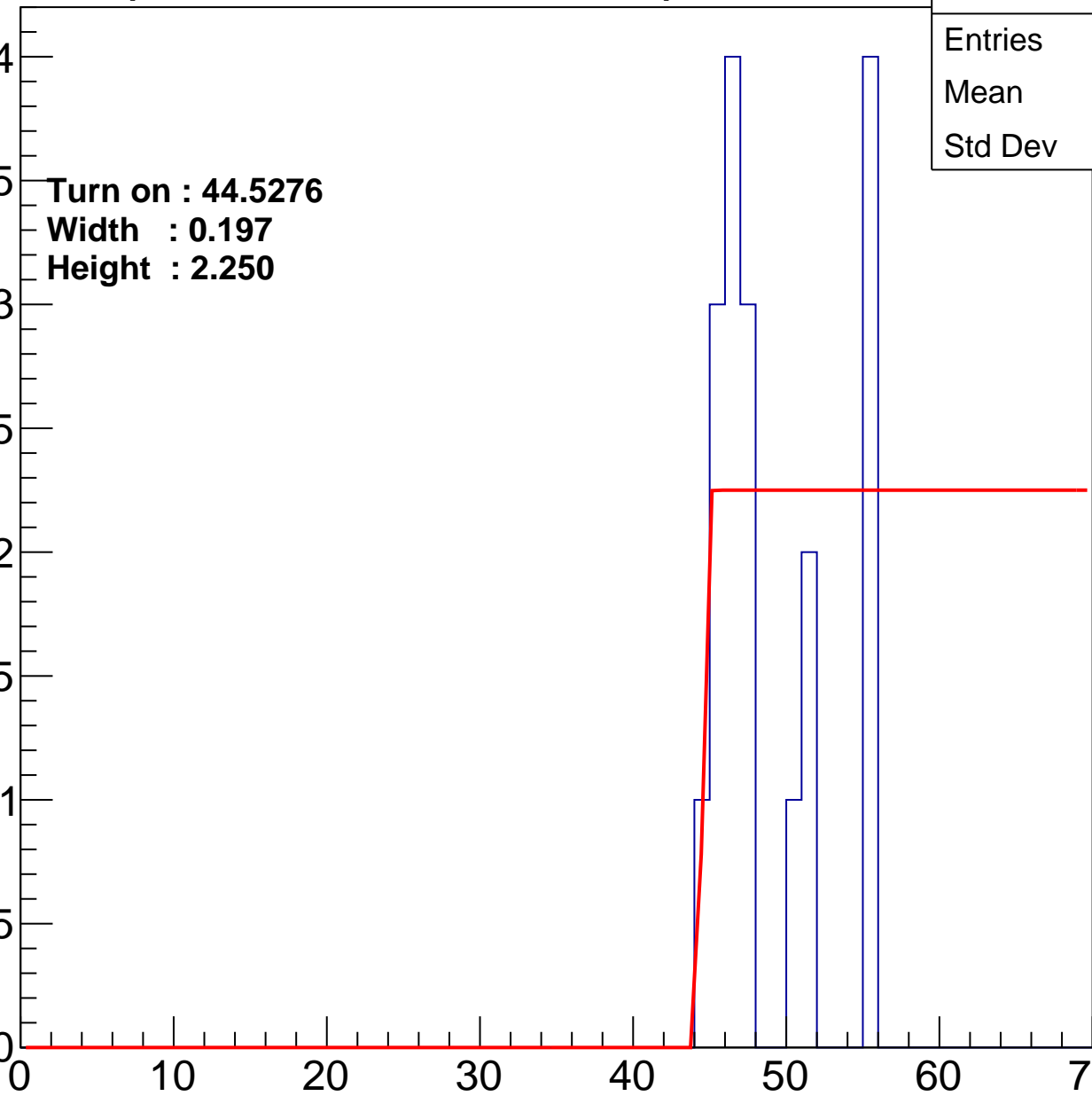
Entry

4  
3.5  
3  
2.5  
2  
1.5  
1  
0.5  
0

Turn on : 44.5276  
Width : 0.197  
Height : 2.250

Entries	18
Mean	48.67
Std Dev	3.887

ampl



# B0L100S, U3-ch16

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U3-ch17

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

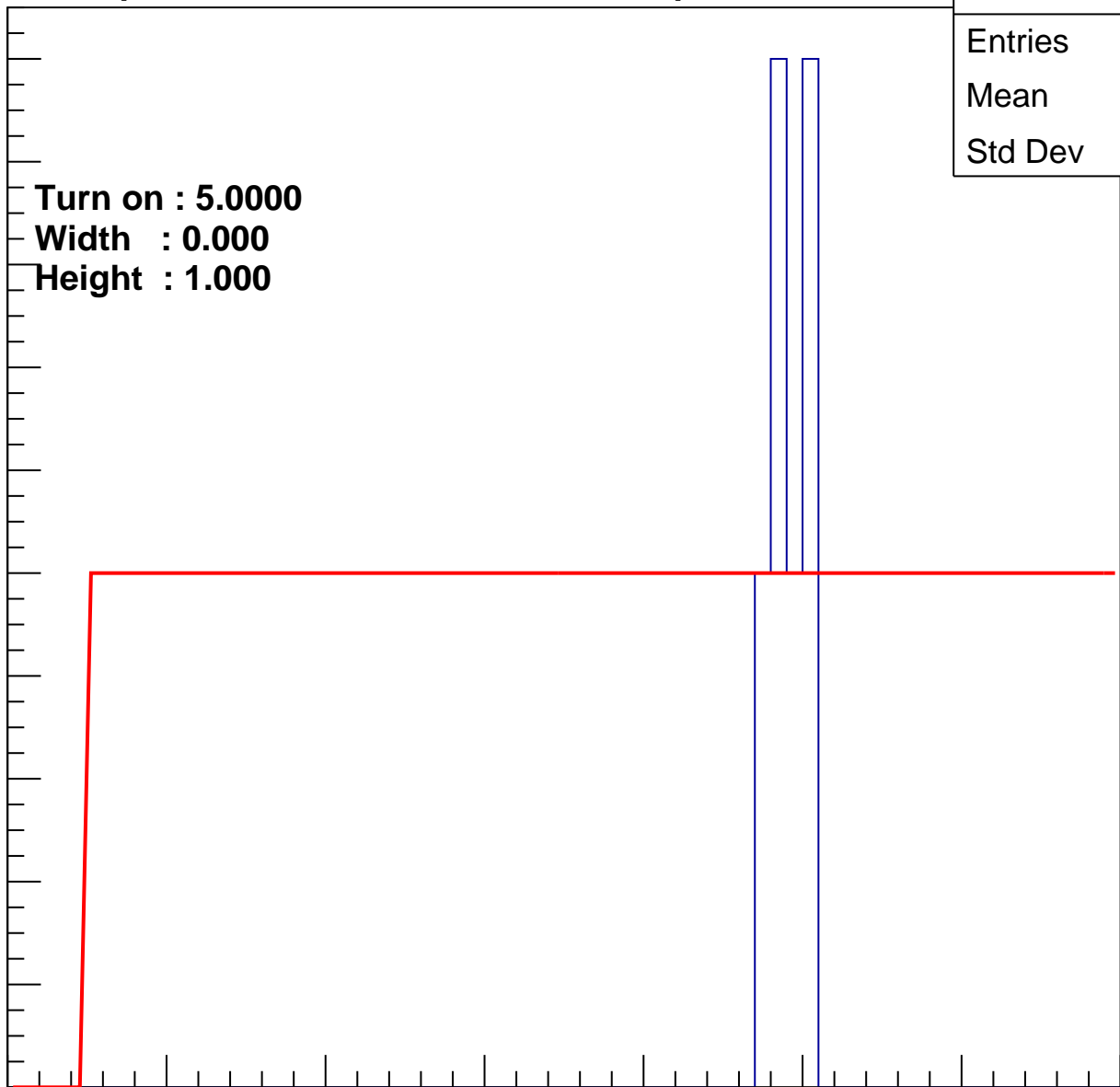
2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Turn on : 5.0000  
Width : 0.000  
Height : 1.000

Entries	6
Mean	48.67
Std Dev	1.106

0 10 20 30 40 50 60 70

ampl



# B0L100S, U3-ch18

calib\_packv5\_042523\_0143.root, FC#6, port A1

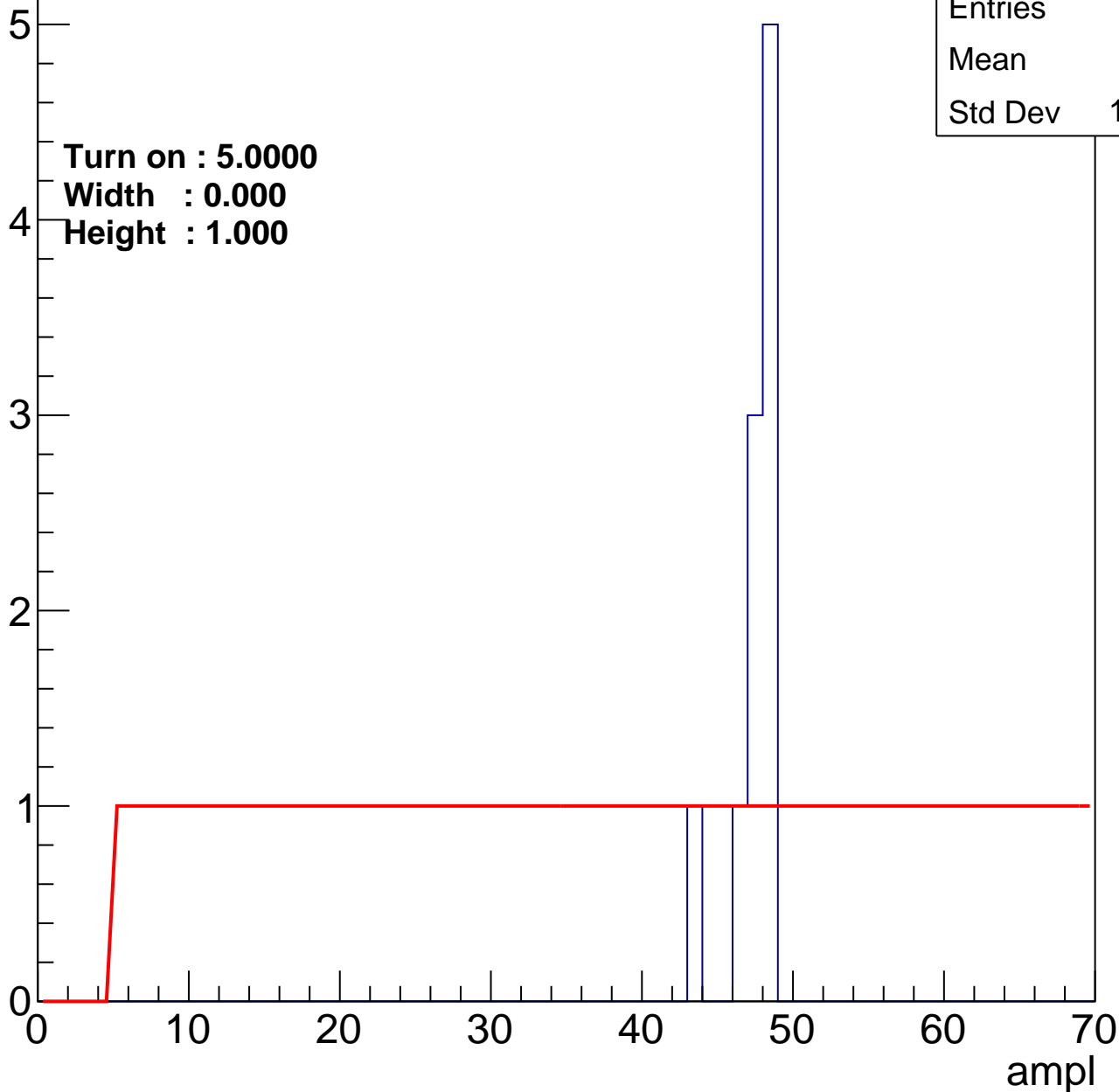
Entry

Entries	10
Mean	47
Std Dev	1.483

Turn on : 5.0000

Width : 0.000

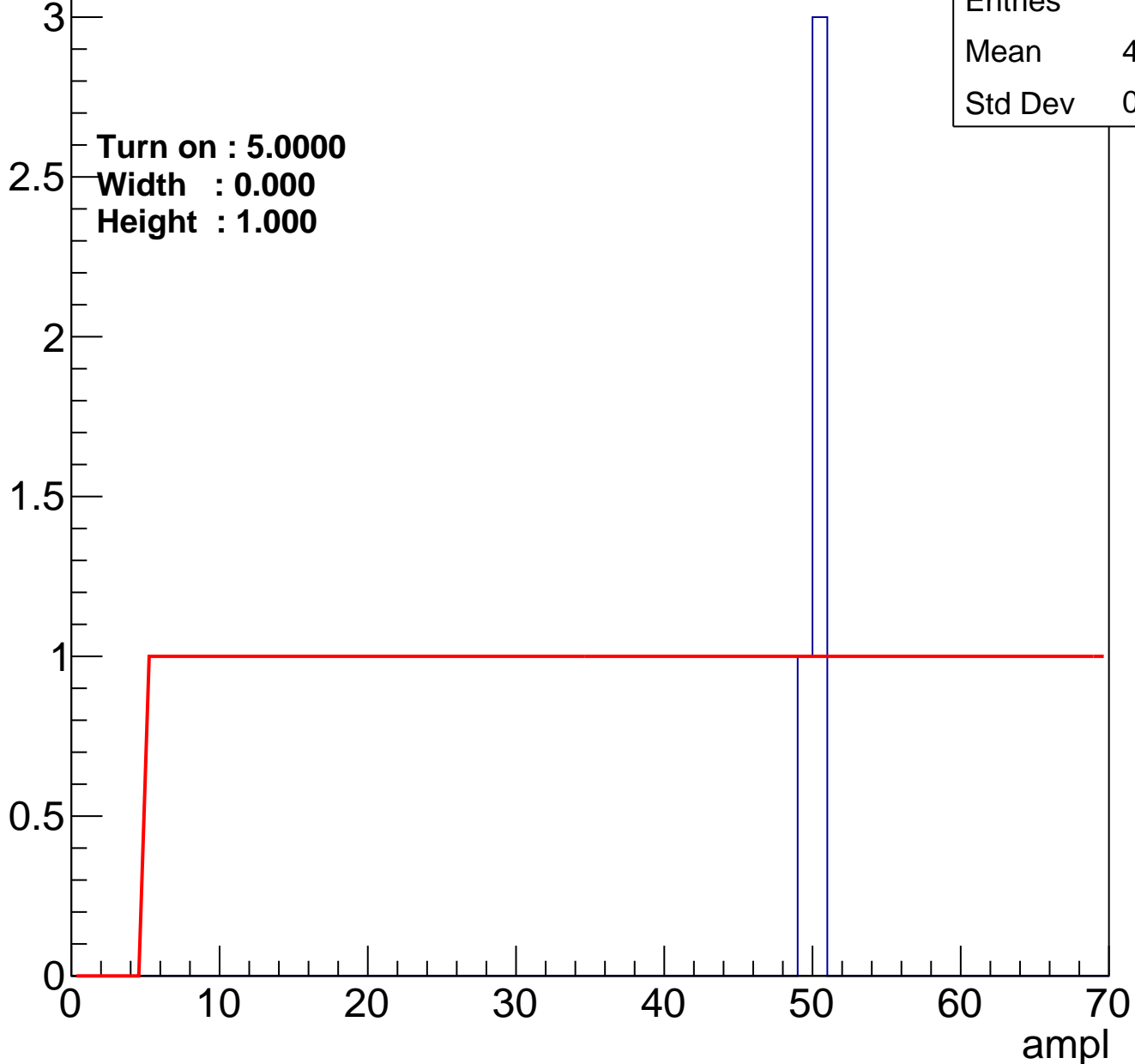
Height : 1.000



# B0L100S, U3-ch19

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U3-ch20

calib\_packv5\_042523\_0143.root, FC#6, port A1

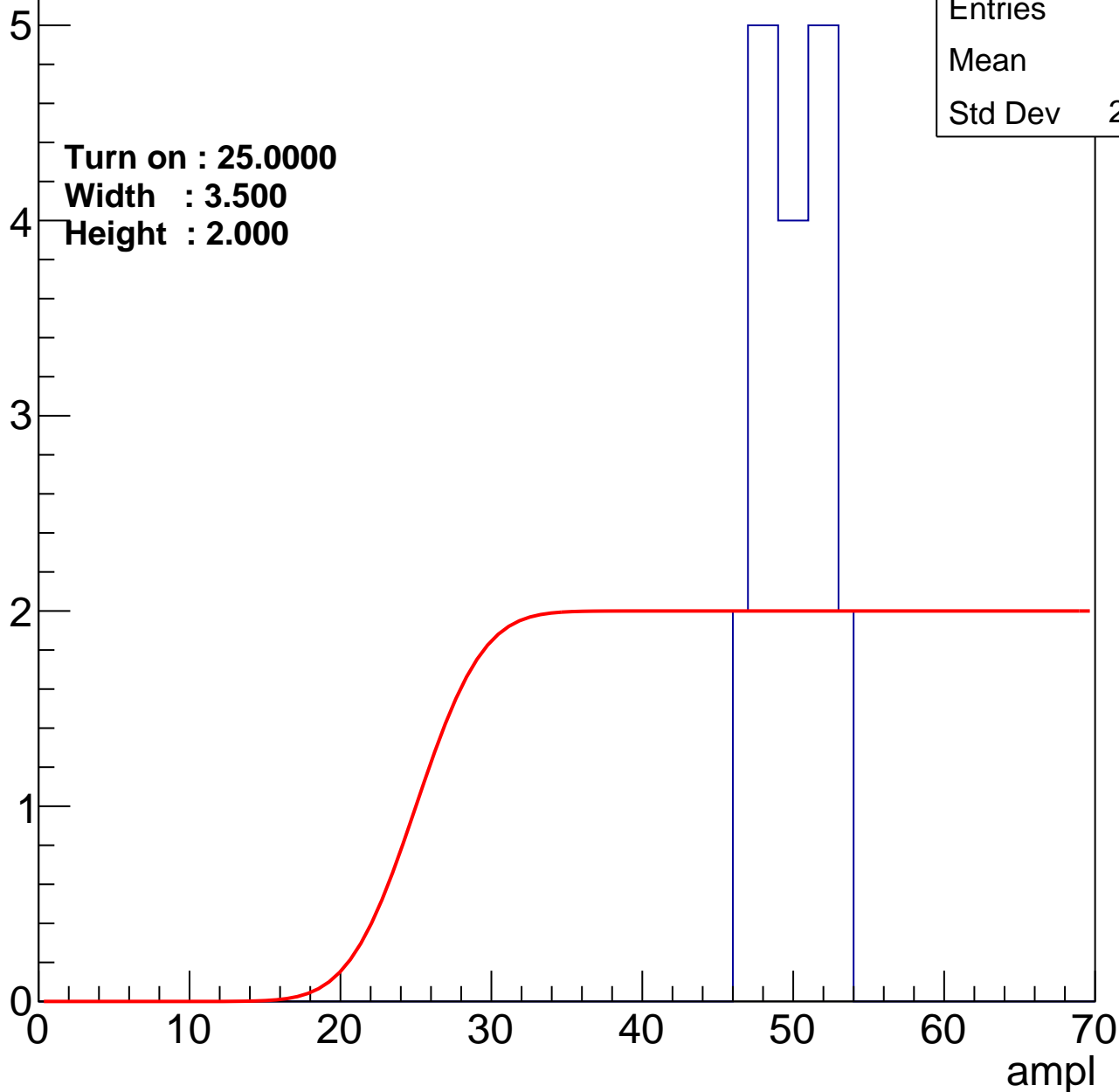
Entry

Entries	32
Mean	49.5
Std Dev	2.062

Turn on : 25.0000

Width : 3.500

Height : 2.000



# B0L100S, U3-ch21

calib\_packv5\_042523\_0143.root, FC#6, port A1

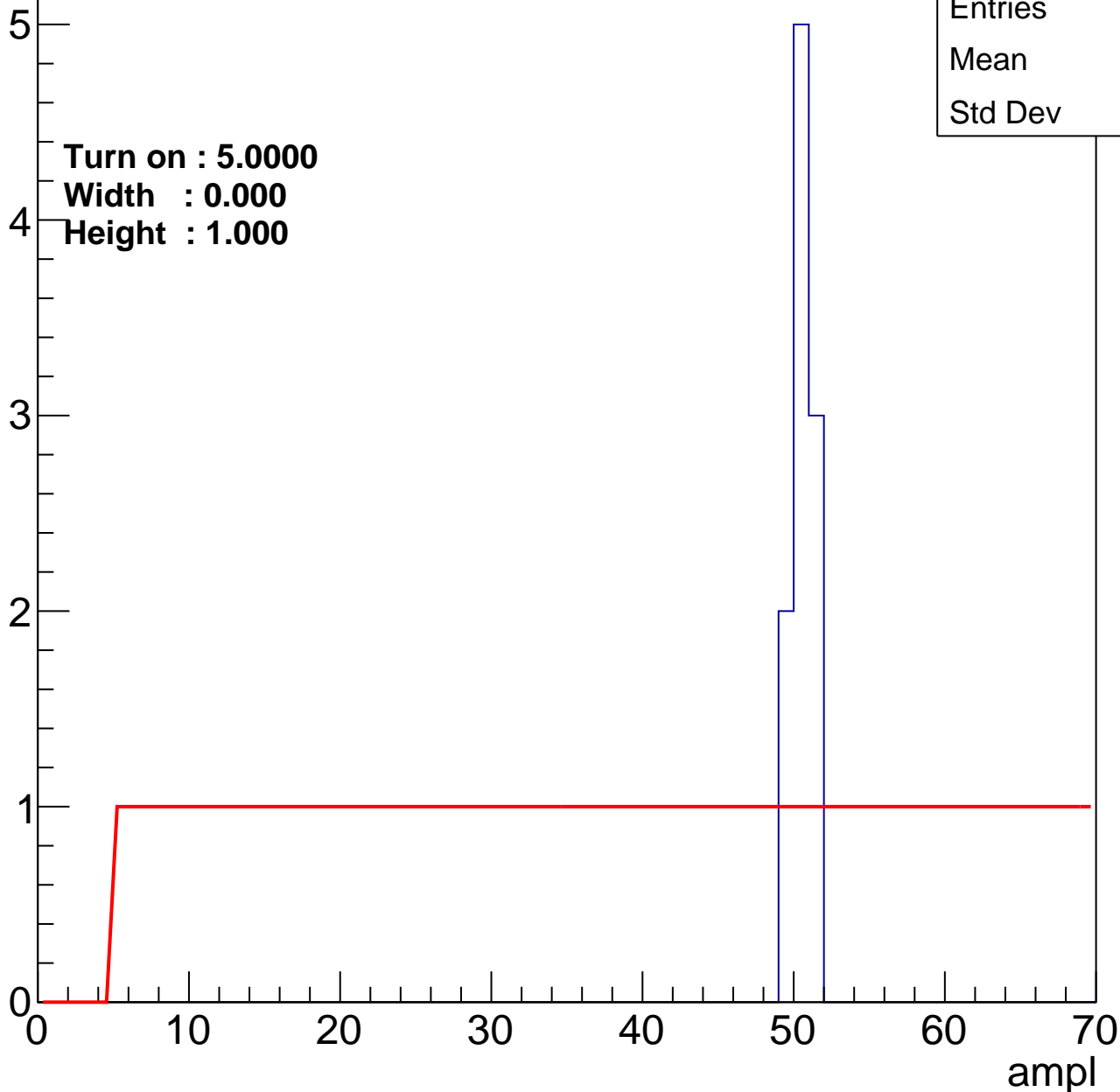
Entry

Entries	10
Mean	50.1
Std Dev	0.7

Turn on : 5.0000

Width : 0.000

Height : 1.000



# B0L100S, U3-ch22

calib\_packv5\_042523\_0143.root, FC#6, port A1

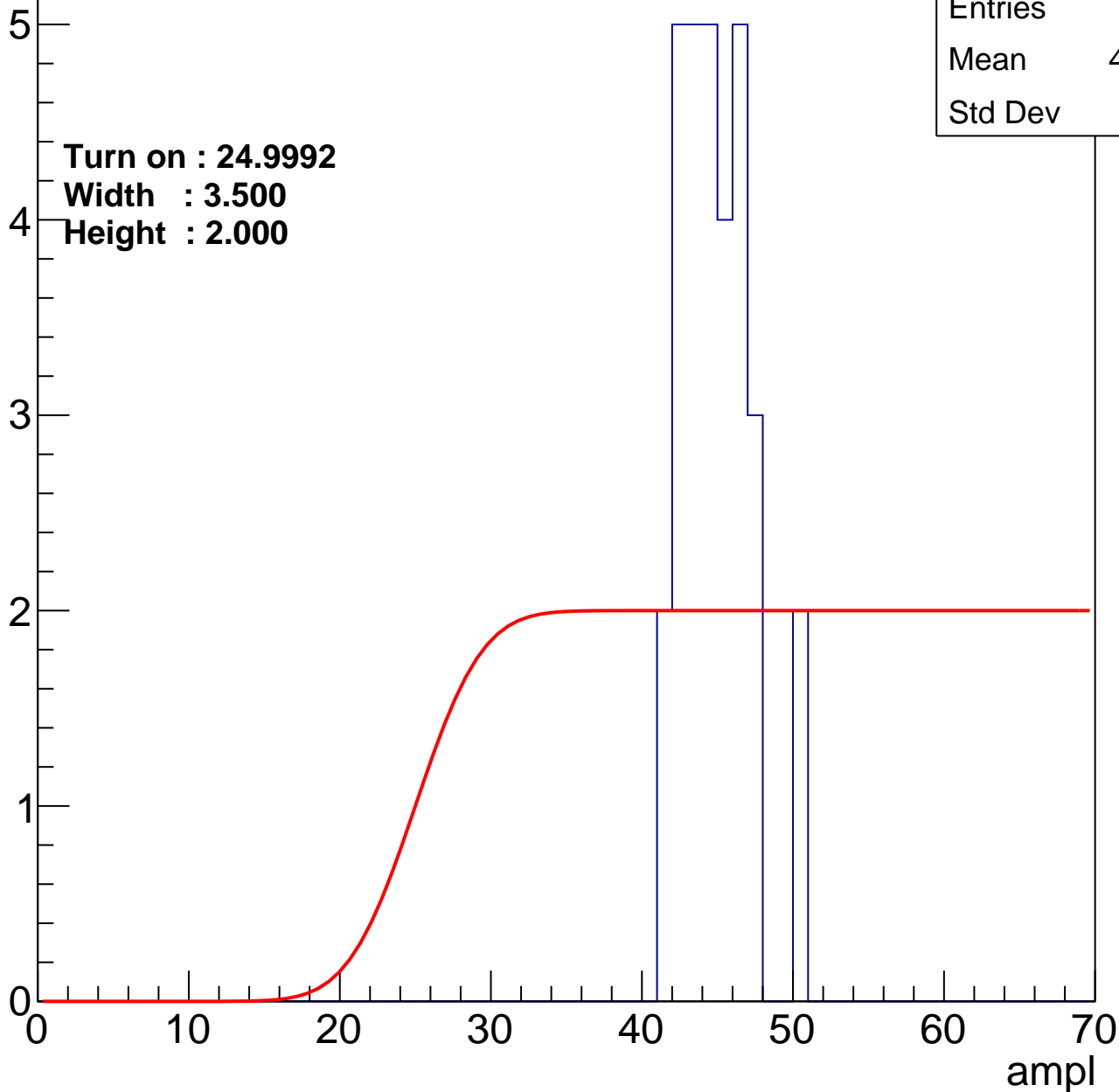
Entry

Entries	31
Mean	44.45
Std Dev	2.27

Turn on : 24.9992

Width : 3.500

Height : 2.000





# B0L100S, U3-ch23

calib\_packv5\_042523\_0143.root, FC#6, port A1

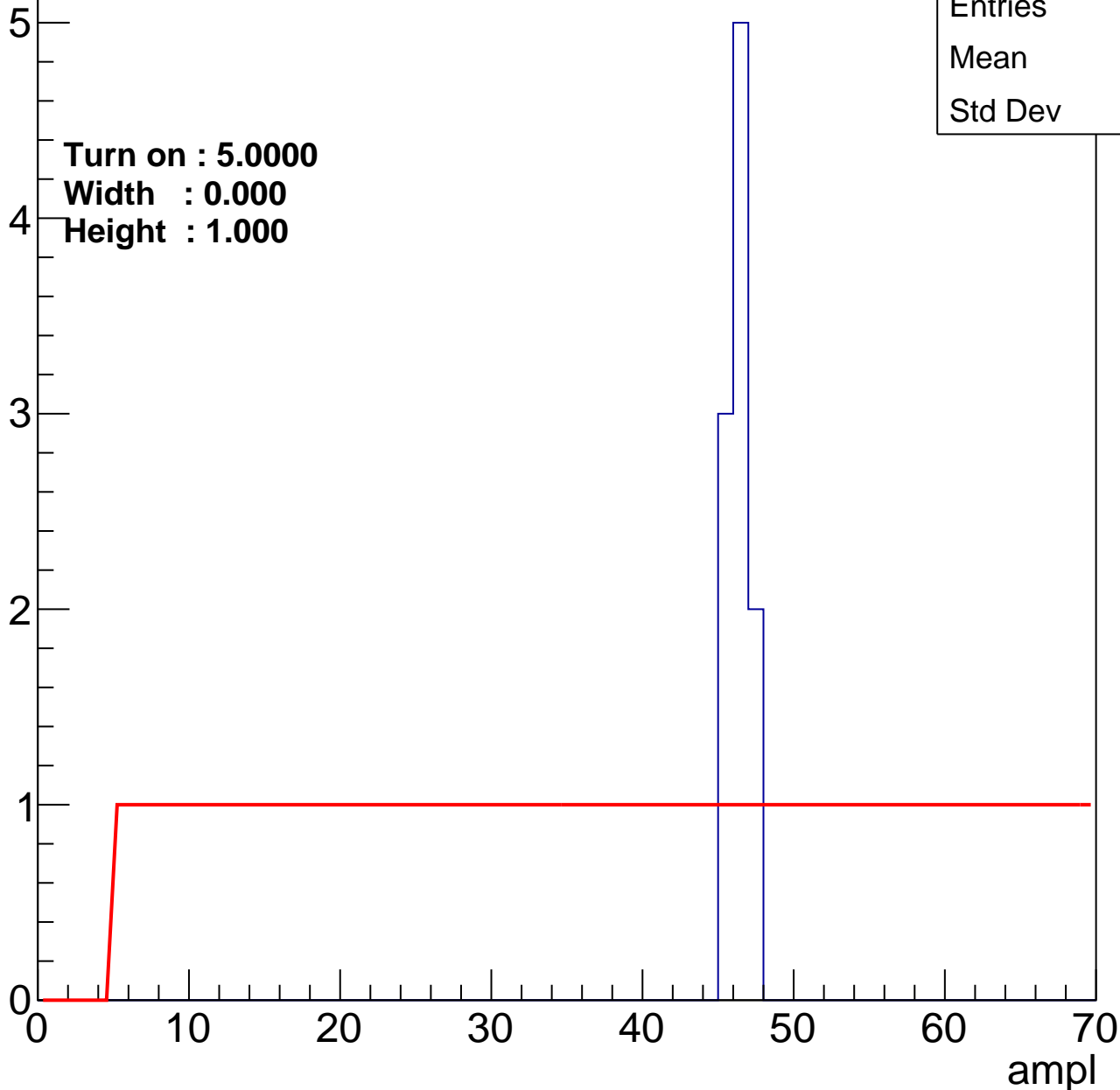
Entry

Entries	10
Mean	45.9
Std Dev	0.7

Turn on : 5.0000

Width : 0.000

Height : 1.000



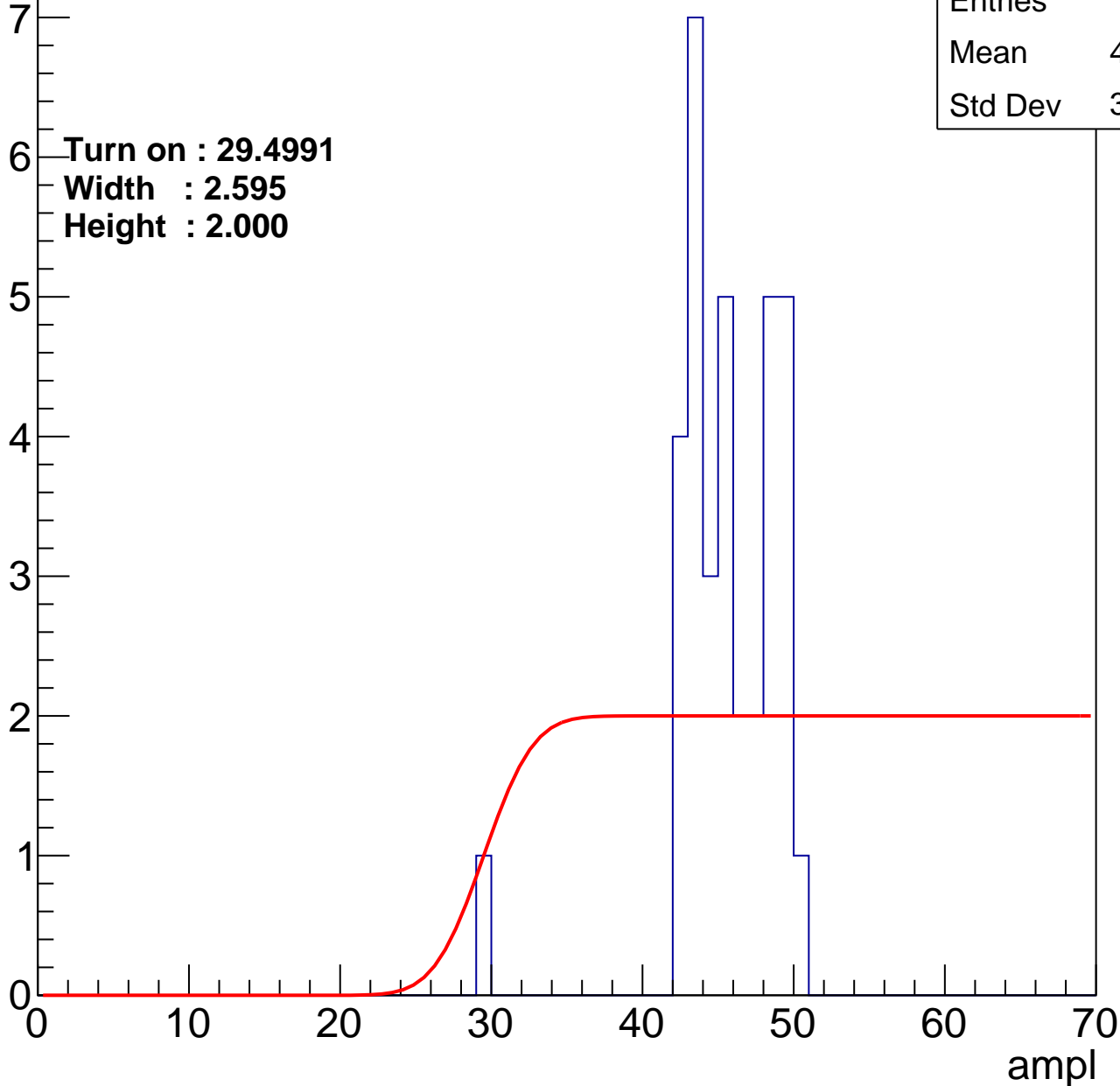
# B0L100S, U3-ch24

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

Entries	35
Mean	45.03
Std Dev	3.715

Turn on : 29.4991  
Width : 2.595  
Height : 2.000



# B0L100S, U3-ch25

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U3-ch26

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U3-ch27

calib\_packv5\_042523\_0143.root, FC#6, port A1

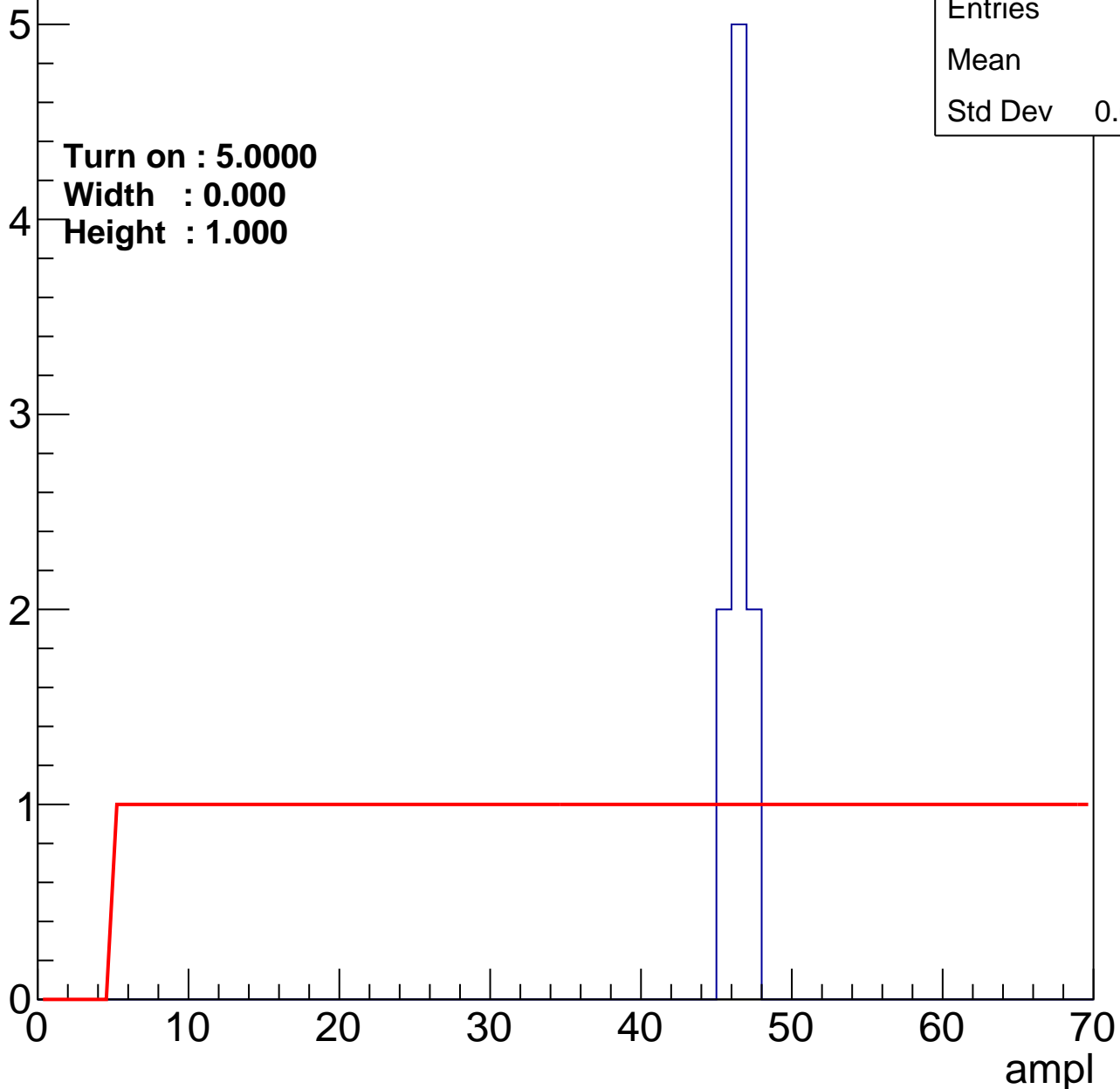
Entry

Entries	9
Mean	46
Std Dev	0.6667

Turn on : 5.0000

Width : 0.000

Height : 1.000



# B0L100S, U3-ch28

calib\_packv5\_042523\_0143.root, FC#6, port A1

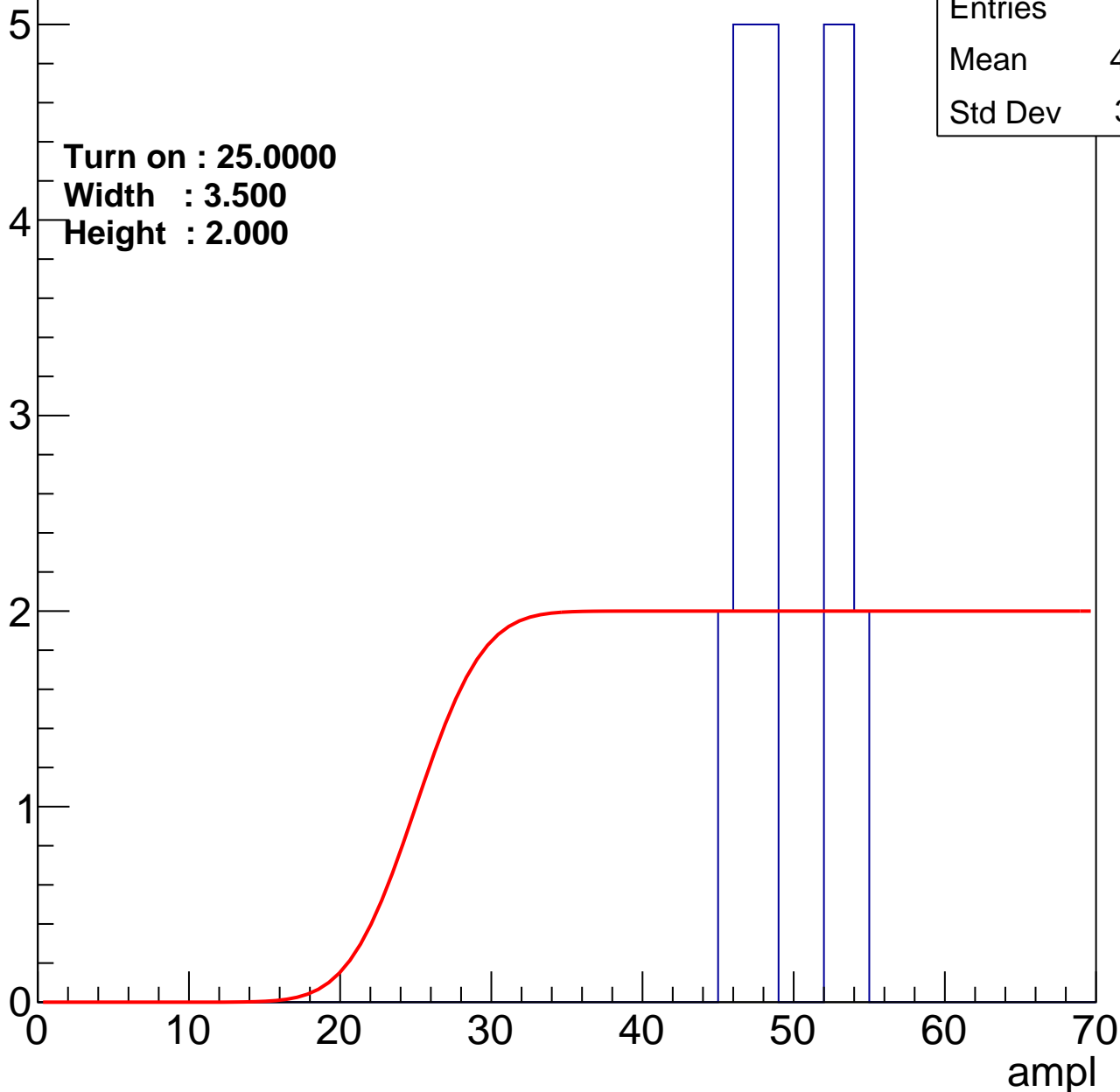
Entry

Entries	29
Mean	49.24
Std Dev	3.081

Turn on : 25.0000

Width : 3.500

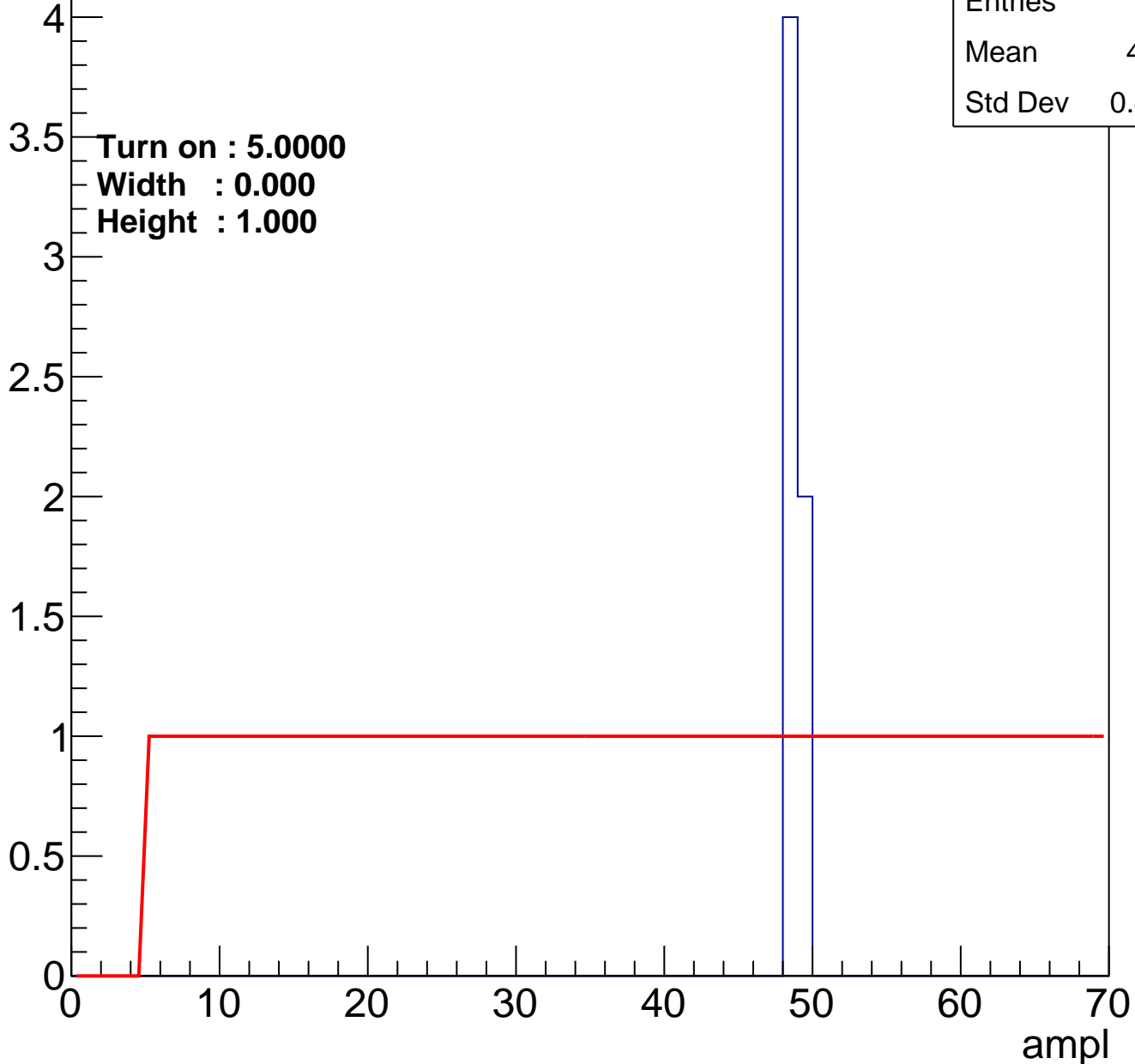
Height : 2.000



# B0L100S, U3-ch29

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Turn on : 5.0000

Width : 0.000

Height : 1.000

Entries	6
Mean	48.33
Std Dev	0.4714





# B0L100S, U3-ch31

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U3-ch32

calib\_packv5\_042523\_0143.root, FC#6, port A1

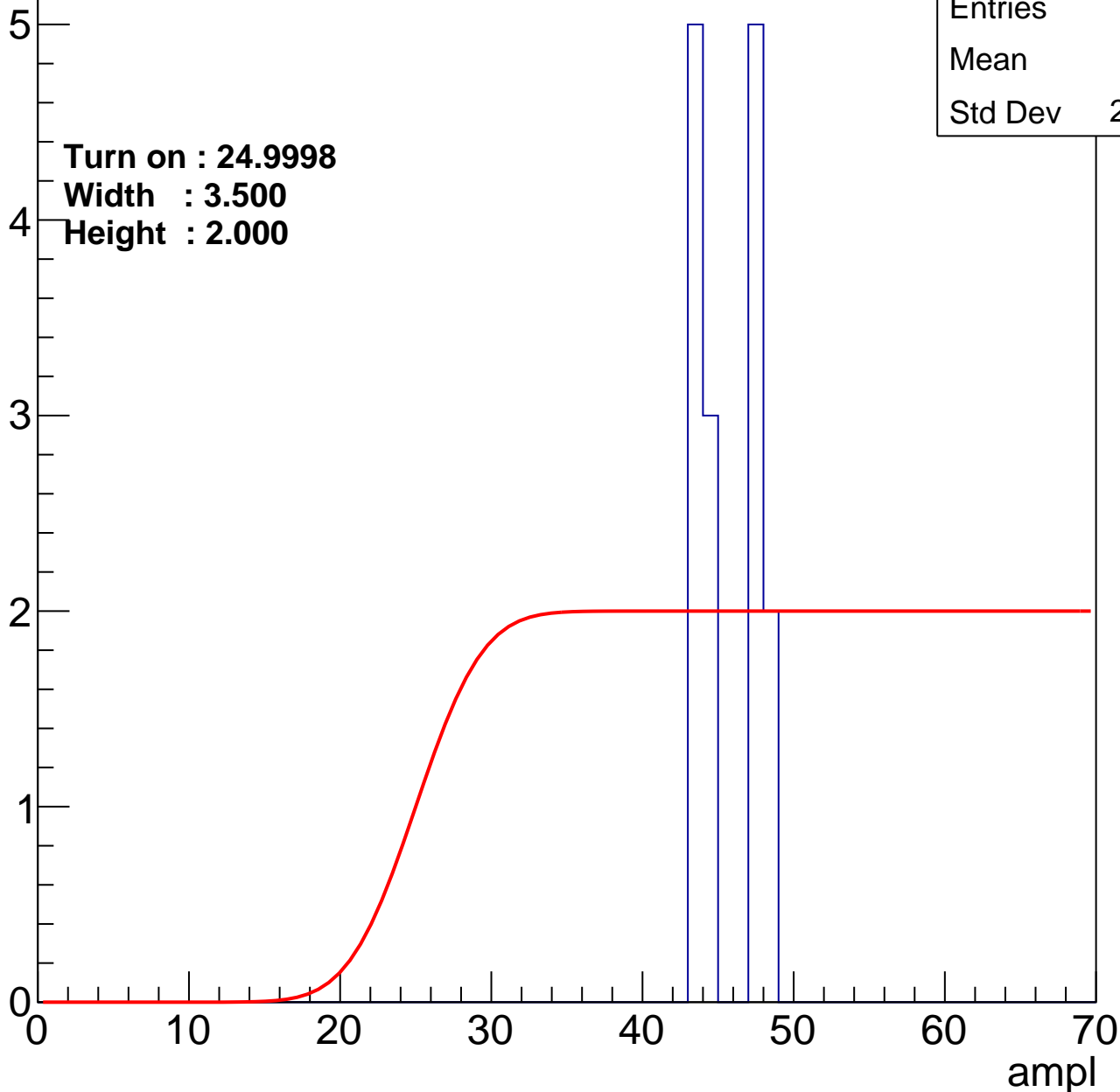
Entry

Entries	15
Mean	45.2
Std Dev	2.007

Turn on : 24.9998

Width : 3.500

Height : 2.000



# B0L100S, U3-ch33

calib\_packv5\_042523\_0143.root, FC#6, port A1

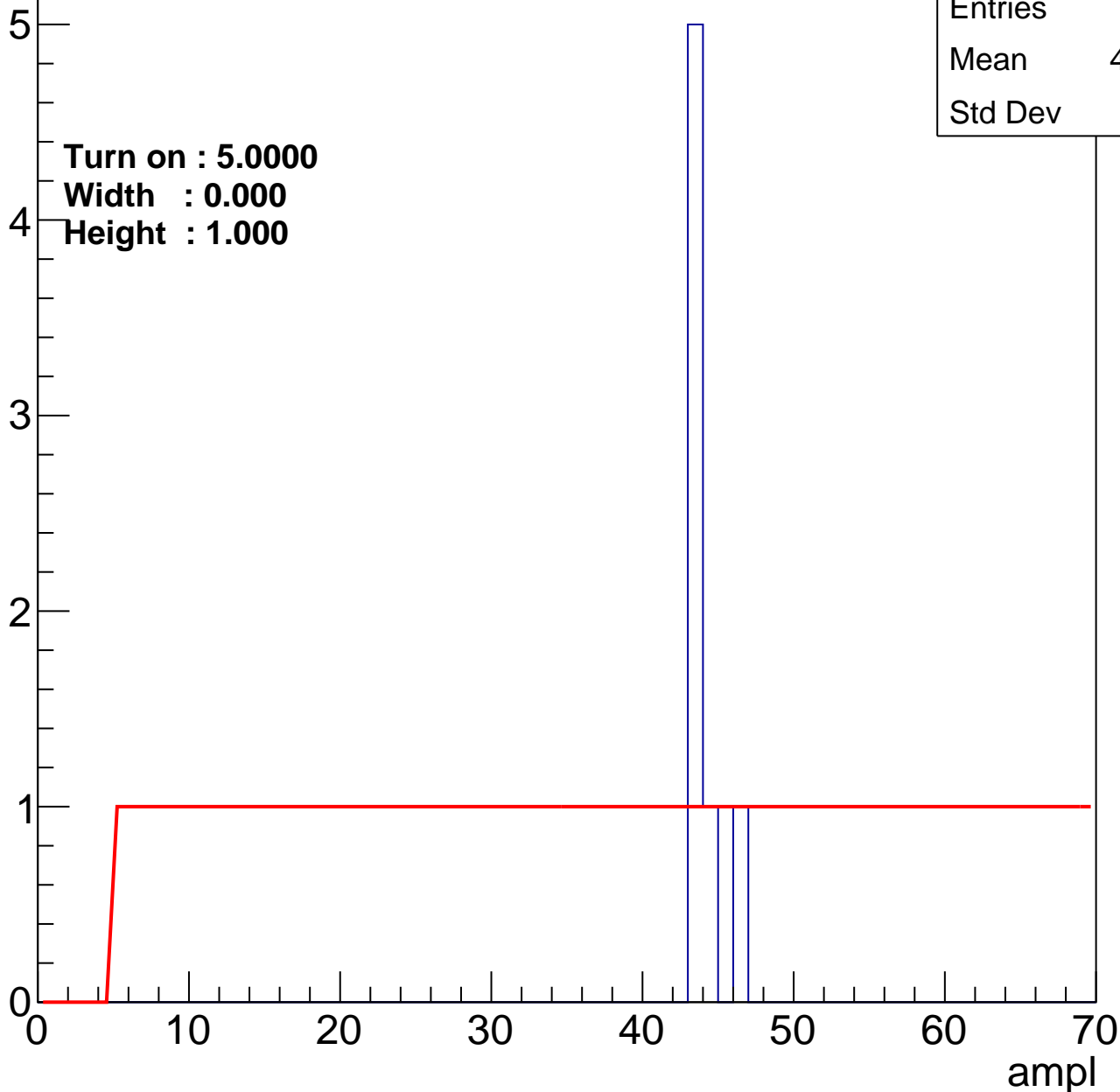
Entry

Entries	7
Mean	43.57
Std Dev	1.05

Turn on : 5.0000

Width : 0.000

Height : 1.000



# B0L100S, U3-ch34

calib\_packv5\_042523\_0143.root, FC#6, port A1

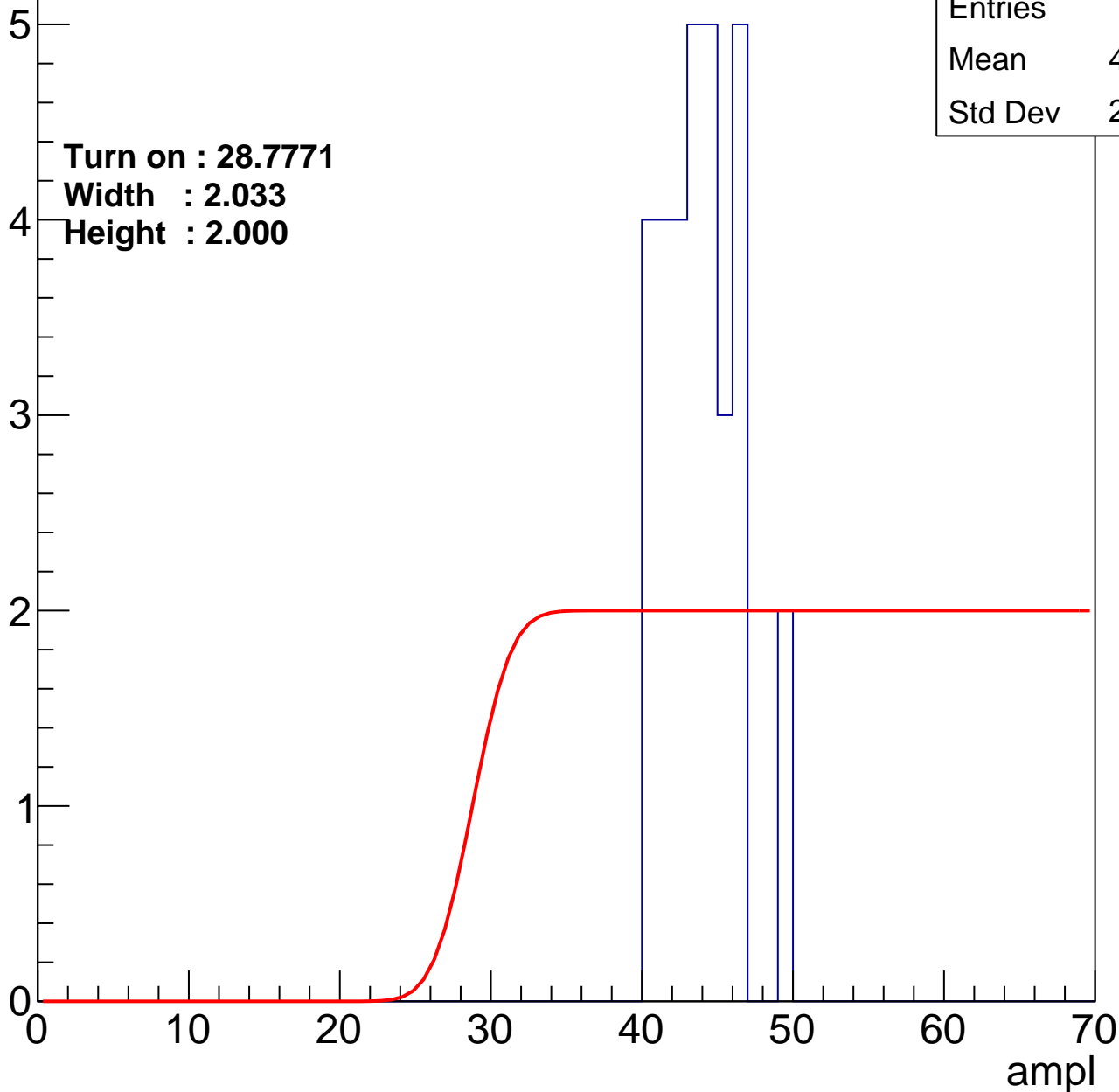
Entry

Entries	32
Mean	43.44
Std Dev	2.397

Turn on : 28.7771

Width : 2.033

Height : 2.000



# B0L100S, U3-ch35

calib\_packv5\_042523\_0143.root, FC#6, port A1

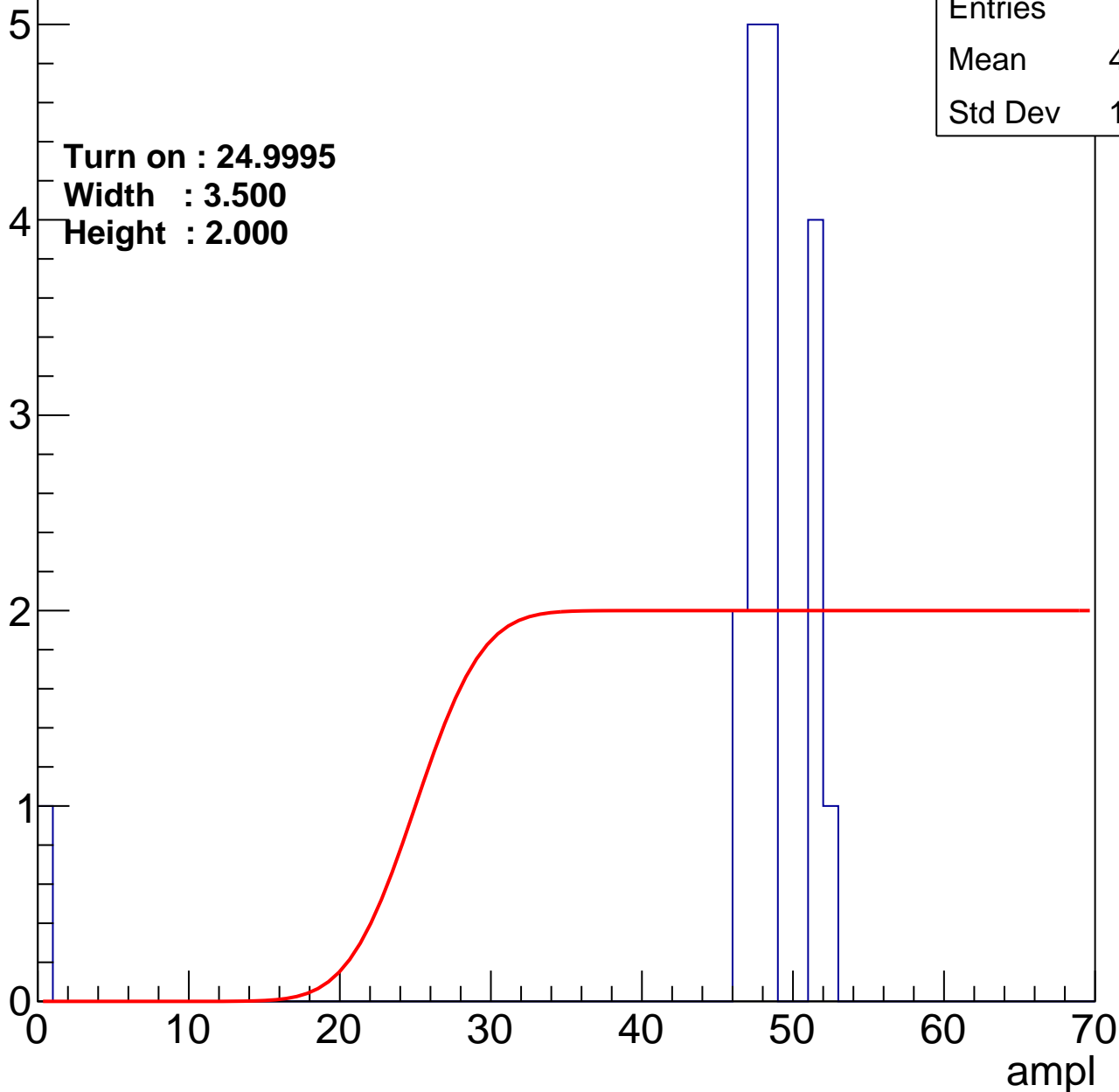
Entry

Entries	18
Mean	45.72
Std Dev	11.24

Turn on : 24.9995

Width : 3.500

Height : 2.000



# B0L100S, U3-ch36

calib\_packv5\_042523\_0143.root, FC#6, port A1

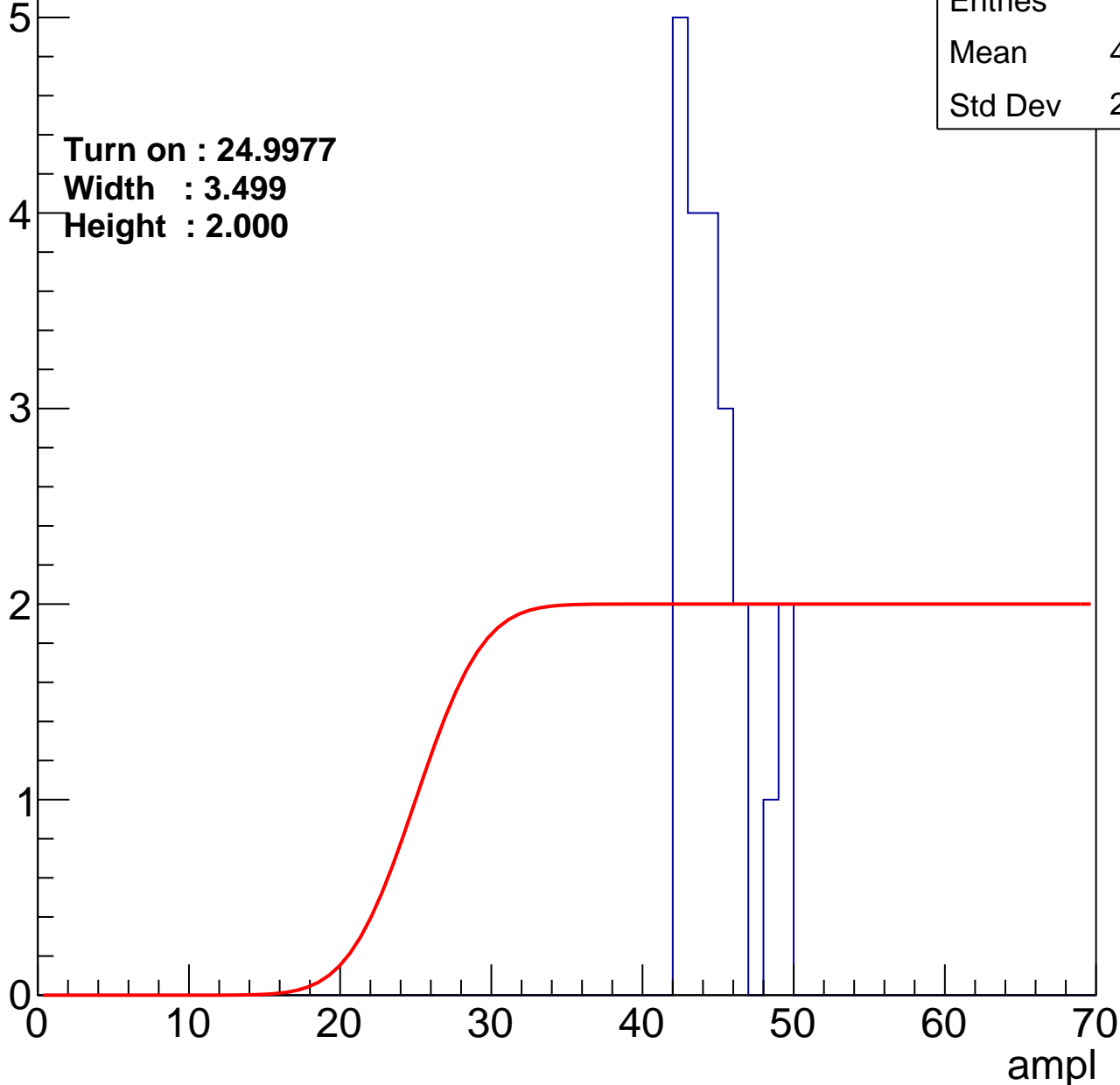
Entry

Entries	21
Mean	44.33
Std Dev	2.168

Turn on : 24.9977

Width : 3.499

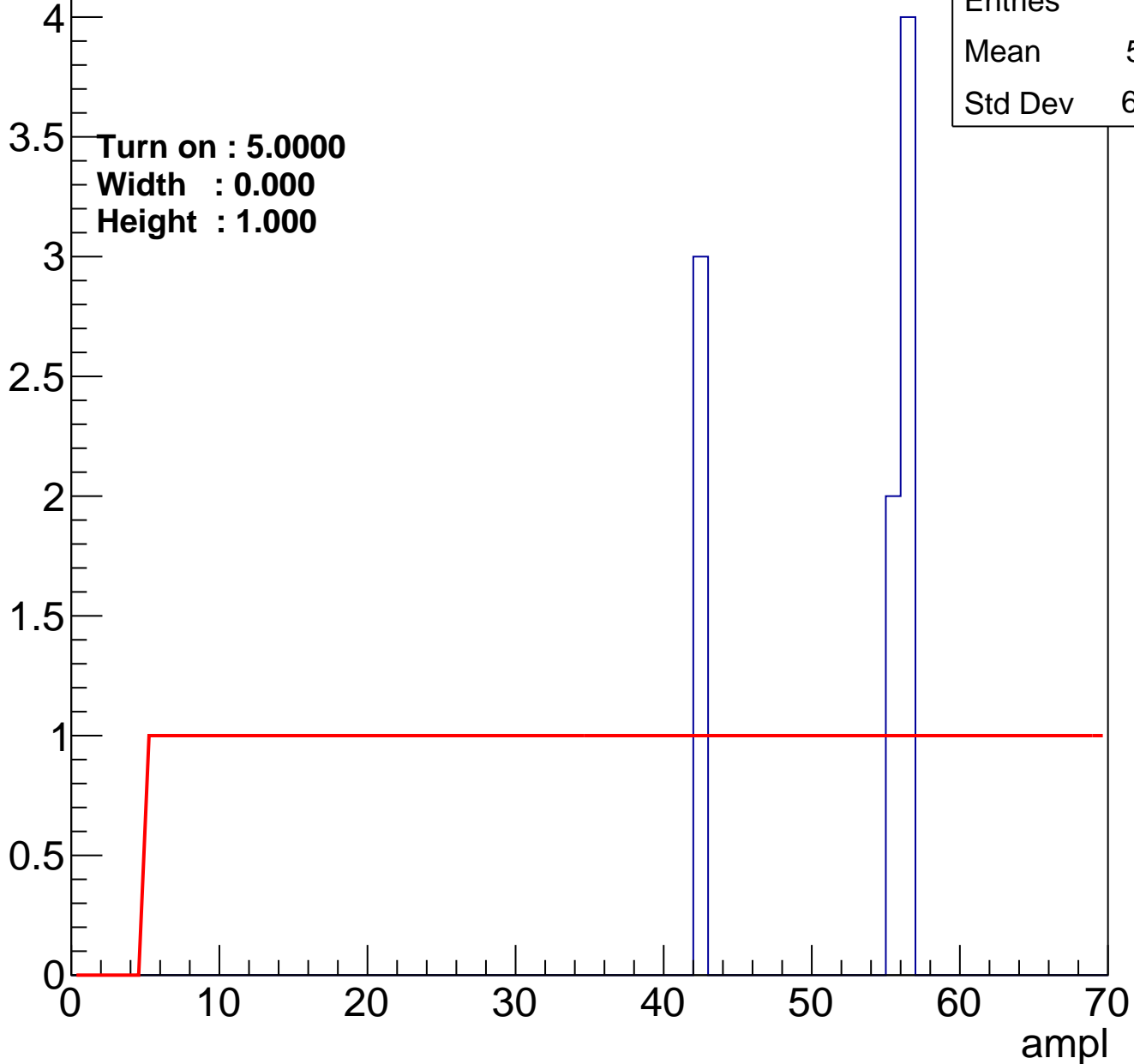
Height : 2.000



# B0L100S, U3-ch37

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	9
Mean	51.11
Std Dev	6.454

# B0L100S, U3-ch38

calib\_packv5\_042523\_0143.root, FC#6, port A1

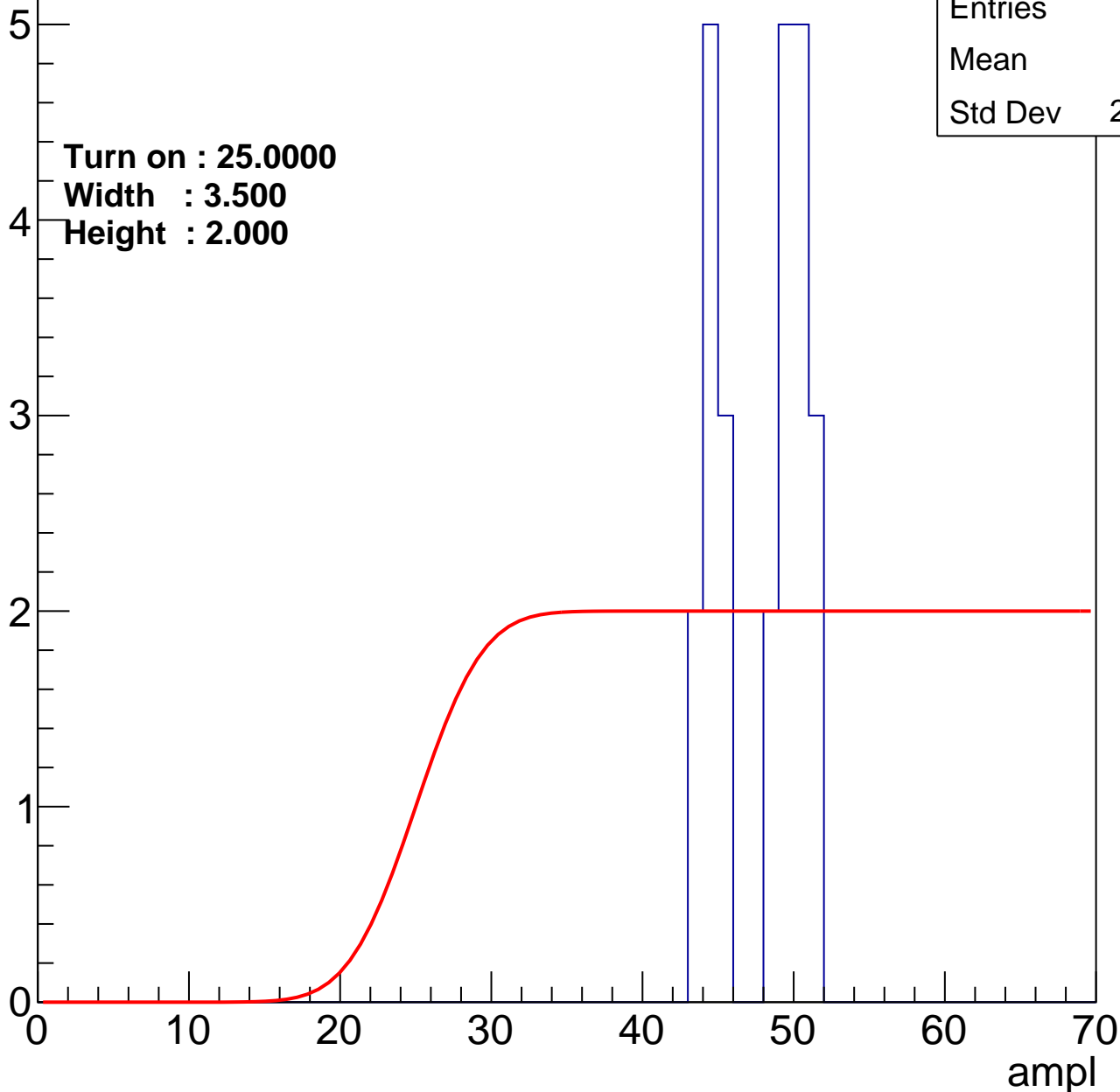
Entry

Entries	25
Mean	47.4
Std Dev	2.828

Turn on : 25.0000

Width : 3.500

Height : 2.000

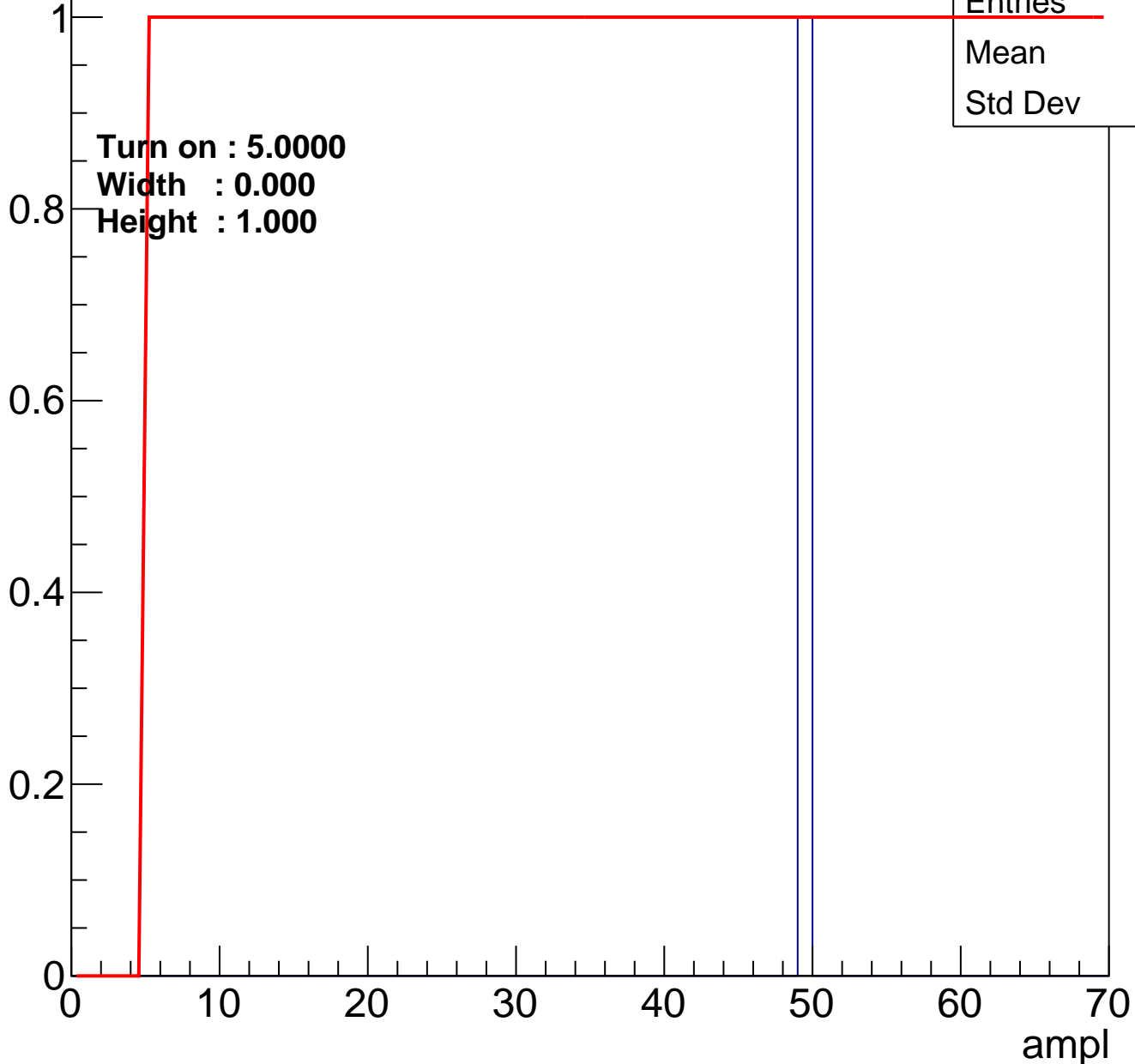




# B0L100S, U3-ch39

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U3-ch40

calib\_packv5\_042523\_0143.root, FC#6, port A1

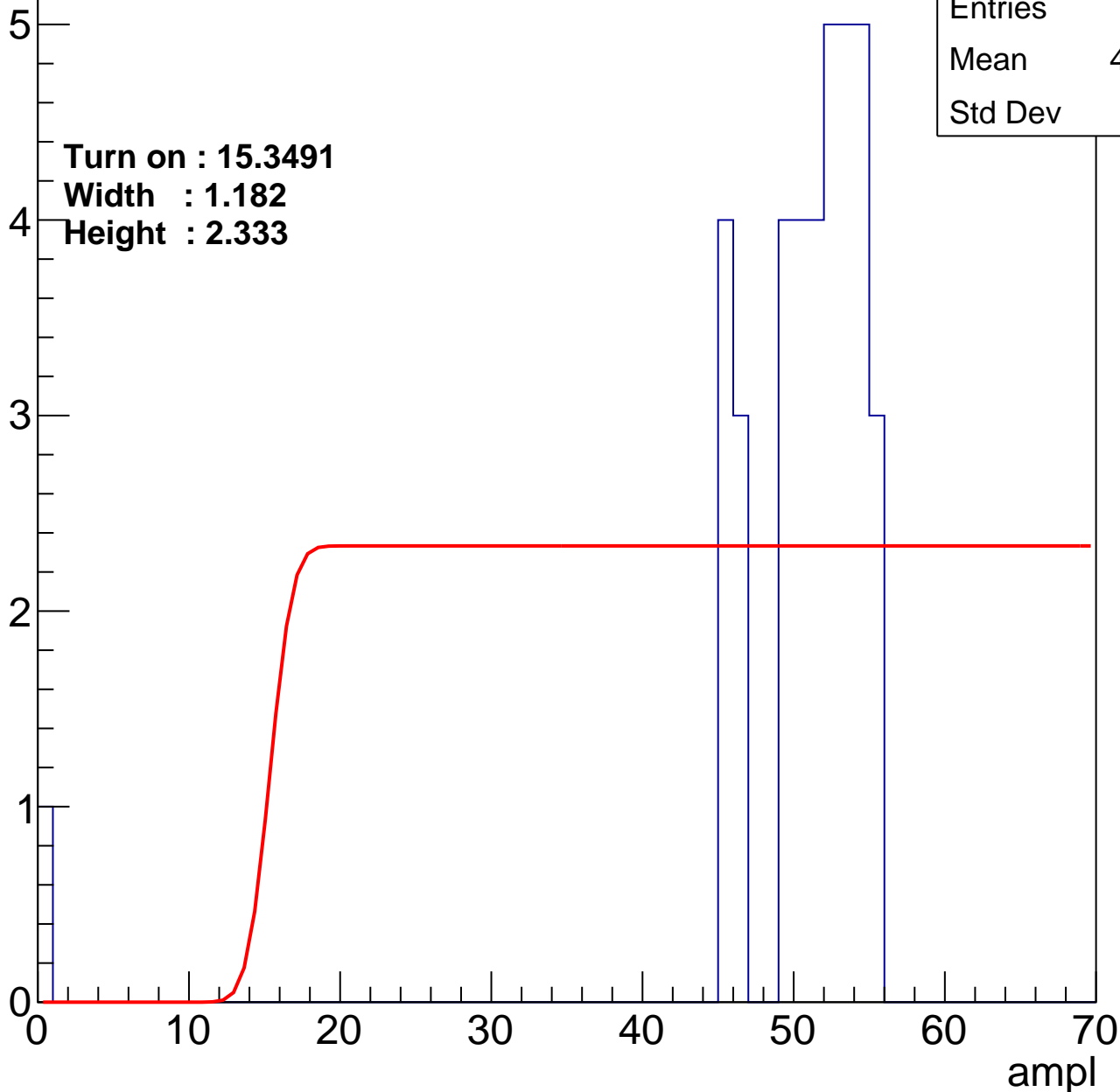
Entry

Entries	38
Mean	49.42
Std Dev	8.68

Turn on : 15.3491

Width : 1.182

Height : 2.333



# B0L100S, U3-ch41

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U3-ch42

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U3-ch43

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U3-ch44

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U3-ch45

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U3-ch46

calib\_packv5\_042523\_0143.root, FC#6, port A1

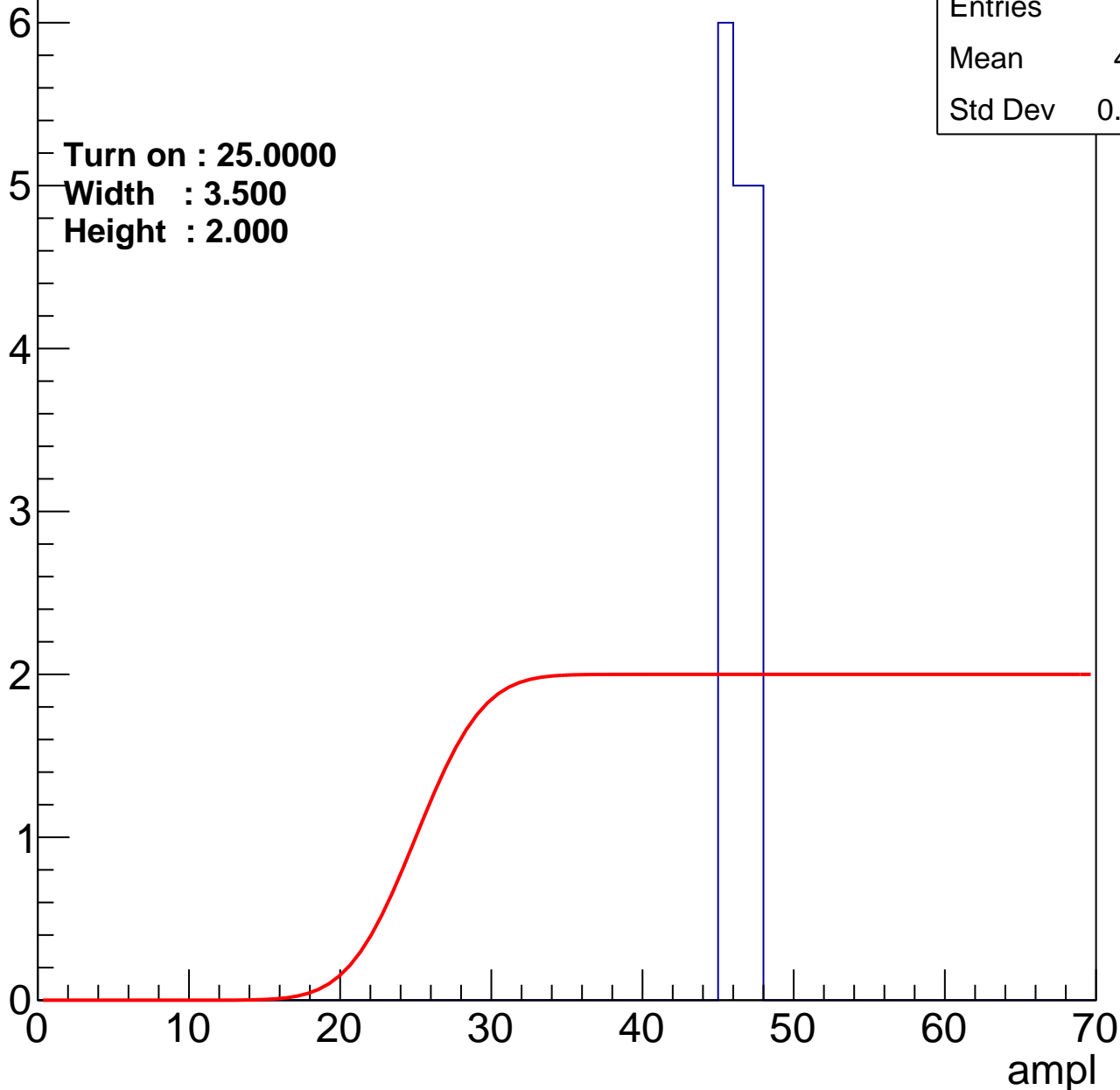
Entry

Entries	16
Mean	45.94
Std Dev	0.8268

Turn on : 25.0000

Width : 3.500

Height : 2.000





# B0L100S, U3-ch47

calib\_packv5\_042523\_0143.root, FC#6, port A1

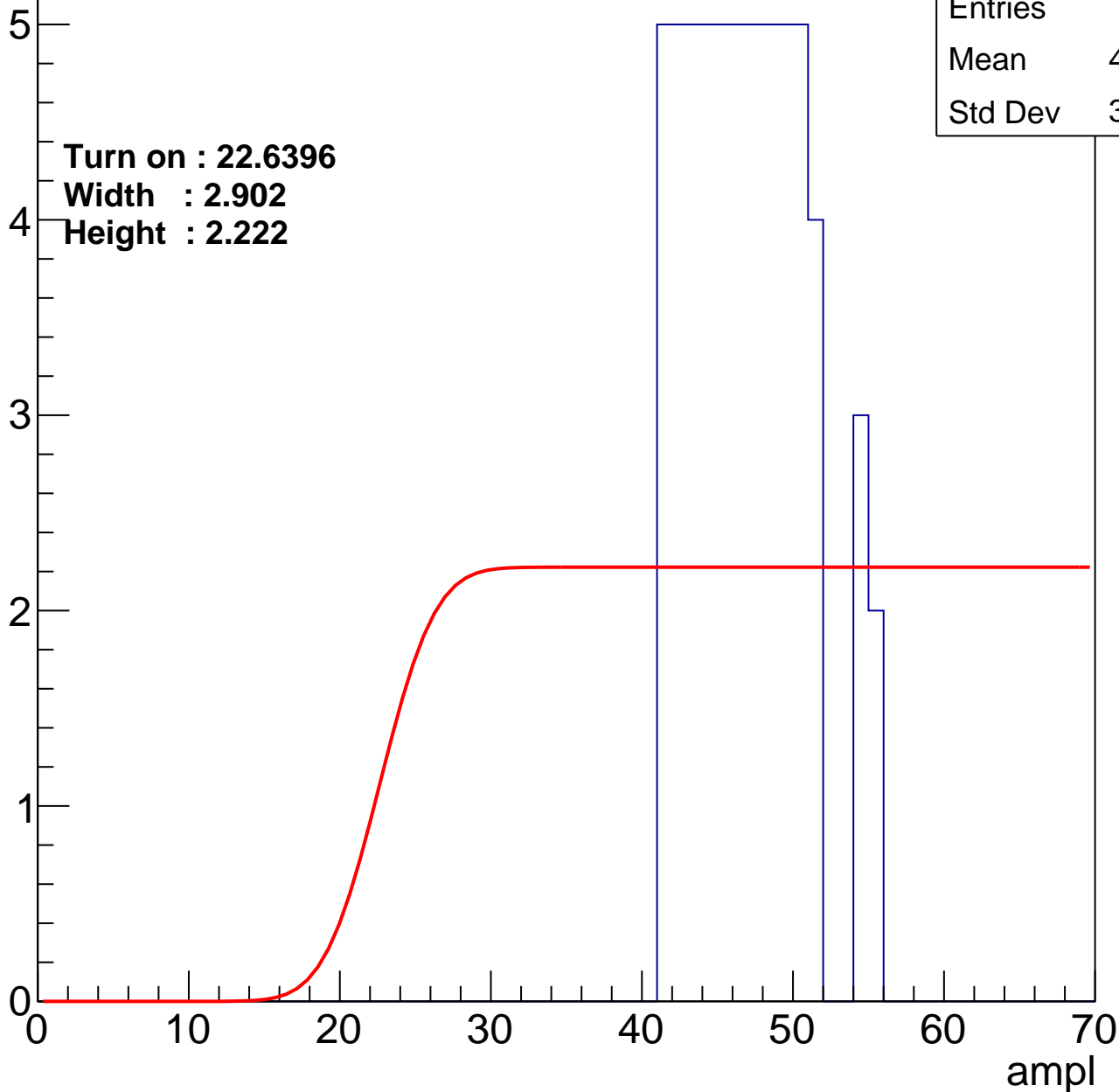
Entry

Entries	59
Mean	46.63
Std Dev	3.809

Turn on : 22.6396

Width : 2.902

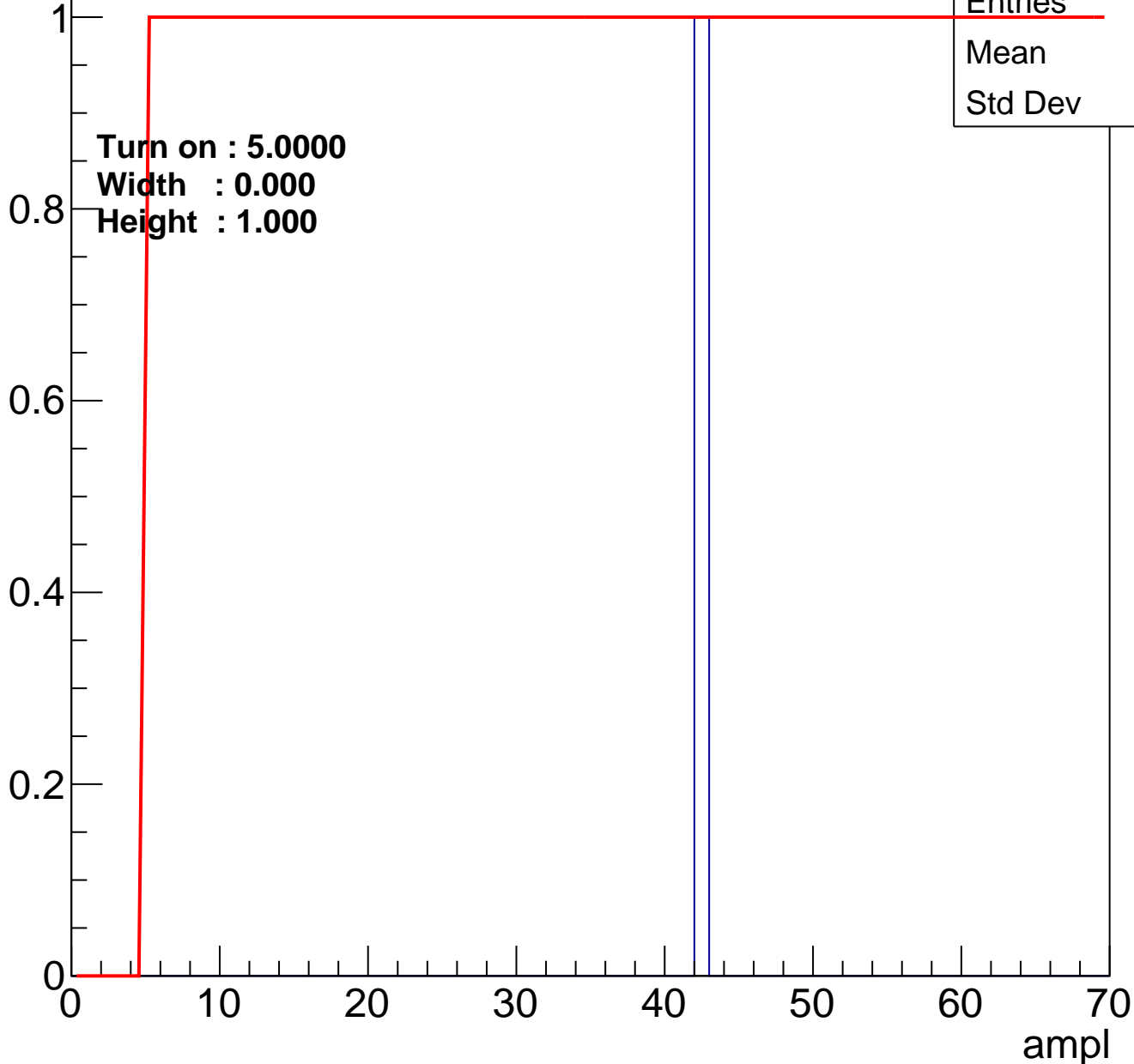
Height : 2.222



# B0L100S, U3-ch48

calib\_packv5\_042523\_0143.root, FC#6, port A1

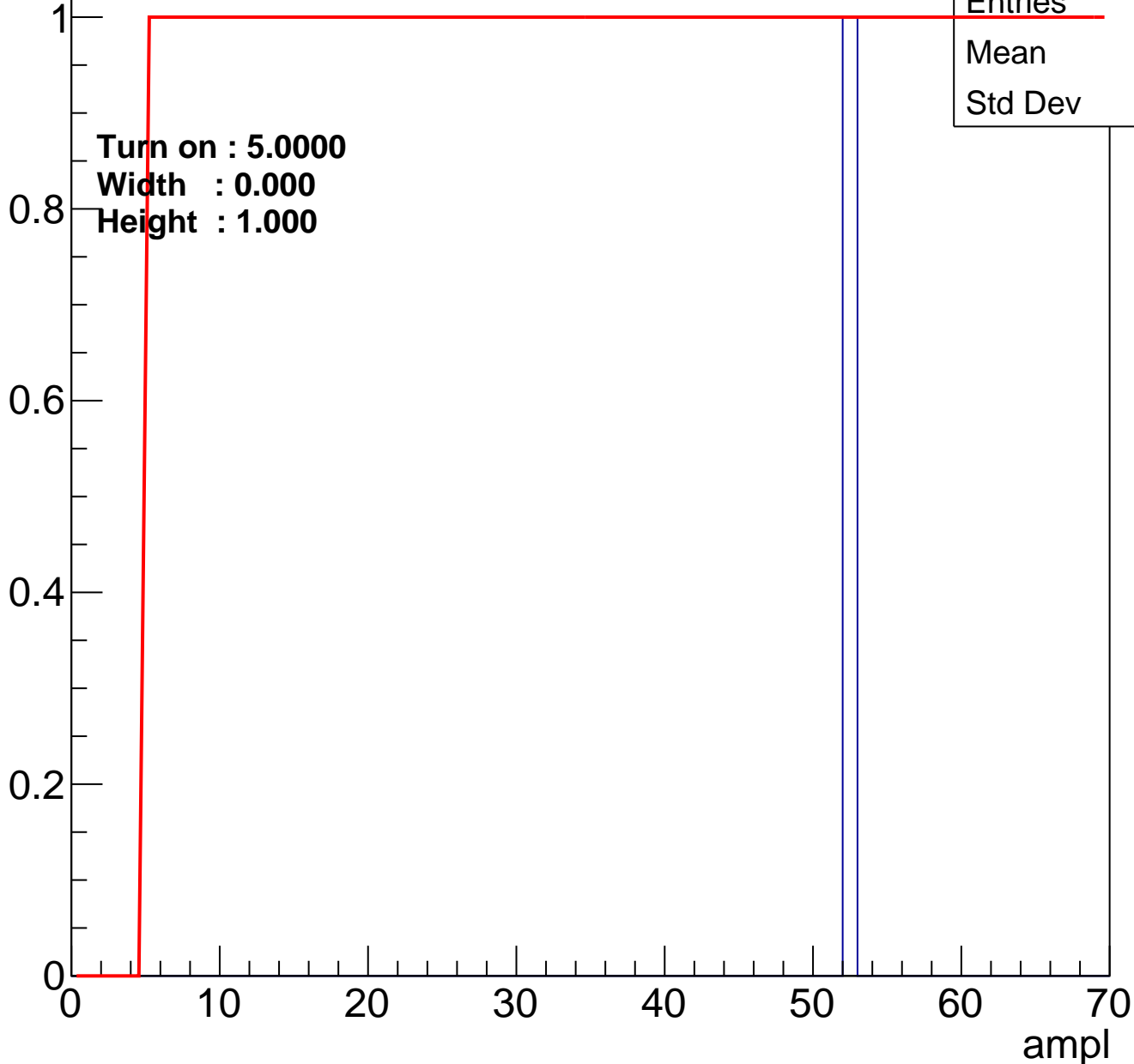
Entry



# B0L100S, U3-ch49

calib\_packv5\_042523\_0143.root, FC#6, port A1

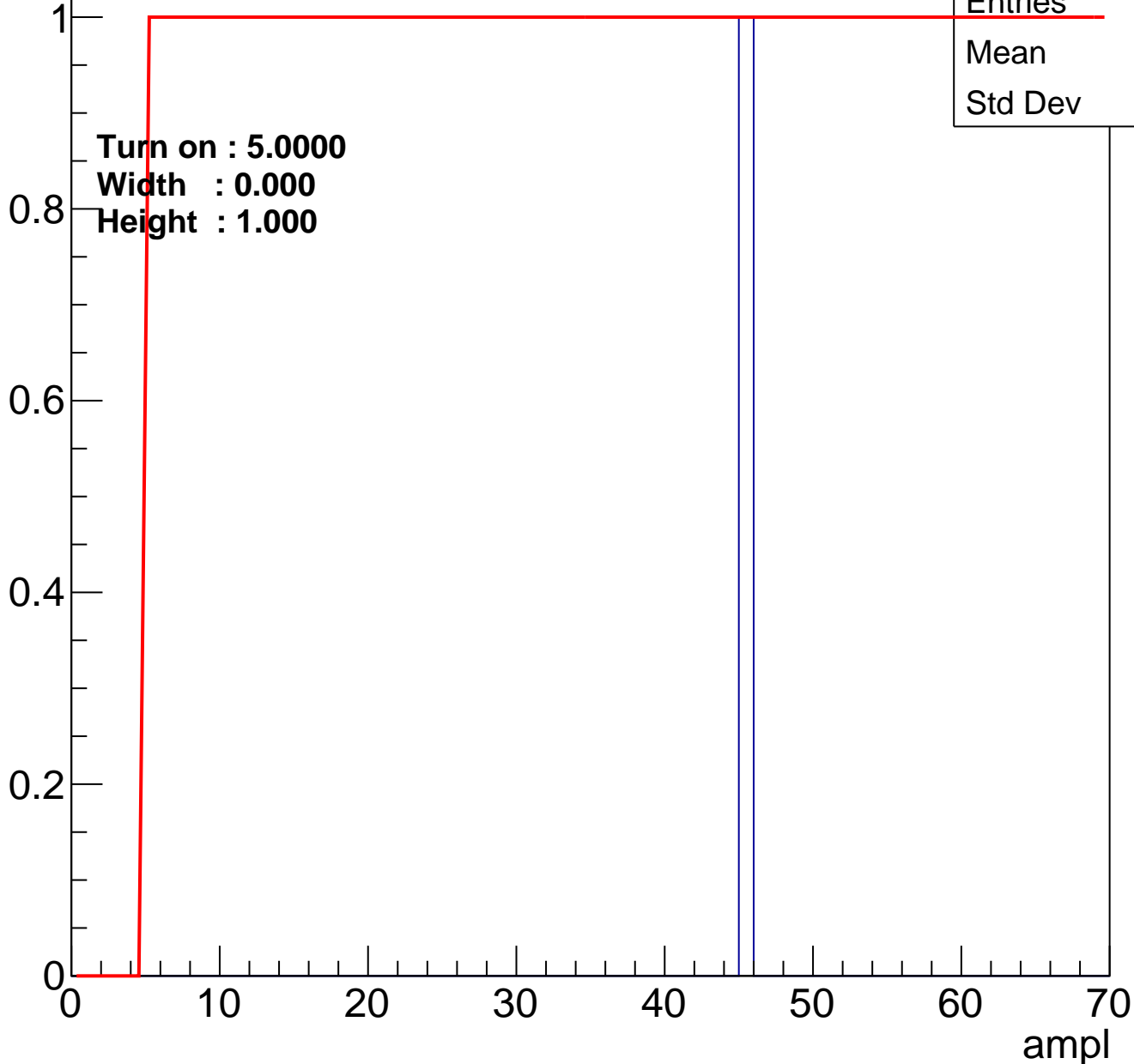
Entry



# B0L100S, U3-ch50

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	1
Mean	45
Std Dev	0

# B0L100S, U3-ch51

calib\_packv5\_042523\_0143.root, FC#6, port A1

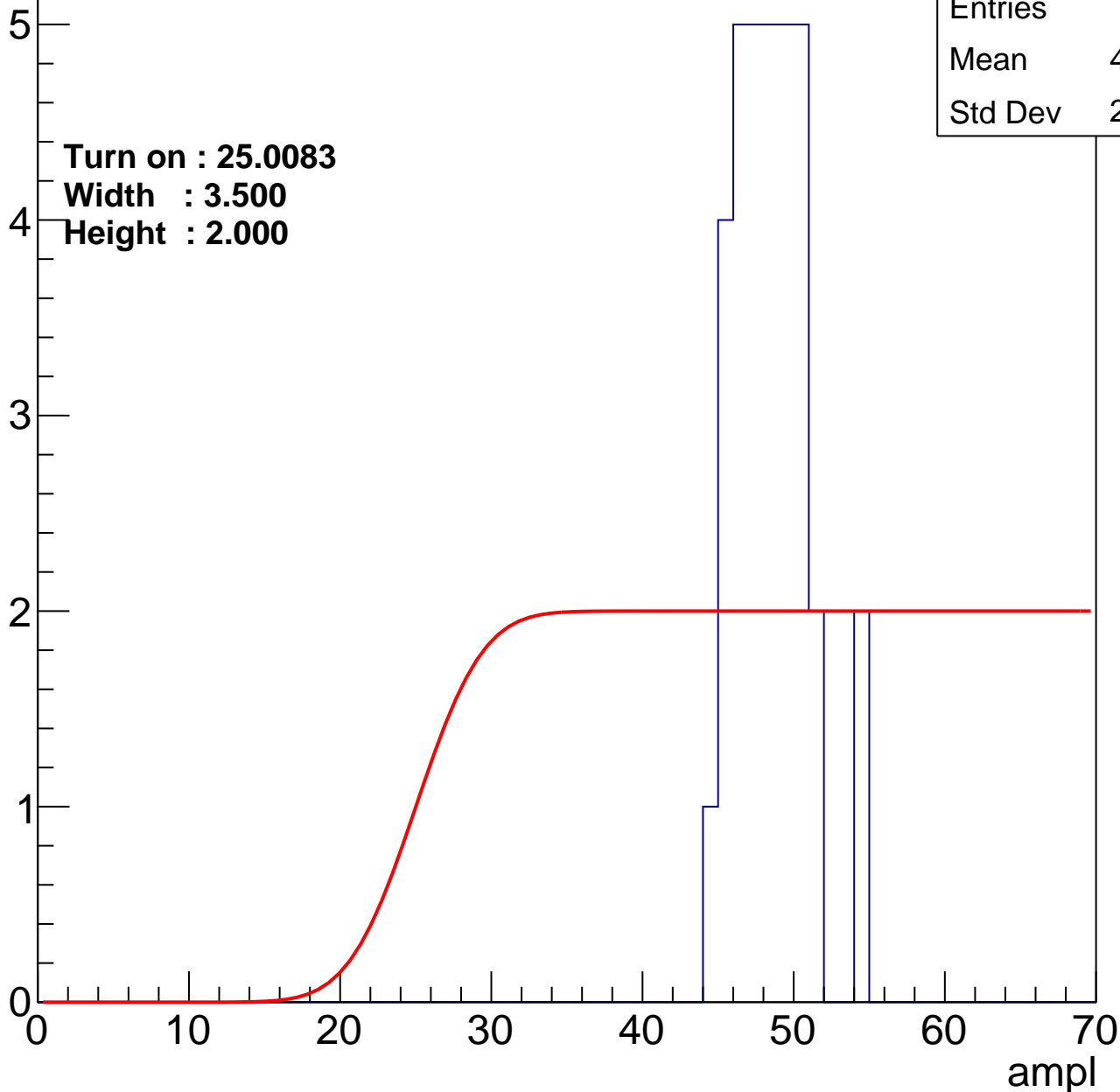
Entry

Entries	34
Mean	48.06
Std Dev	2.376

Turn on : 25.0083

Width : 3.500

Height : 2.000



# B0L100S, U3-ch52

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U3-ch53

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U3-ch54

calib\_packv5\_042523\_0143.root, FC#6, port A1

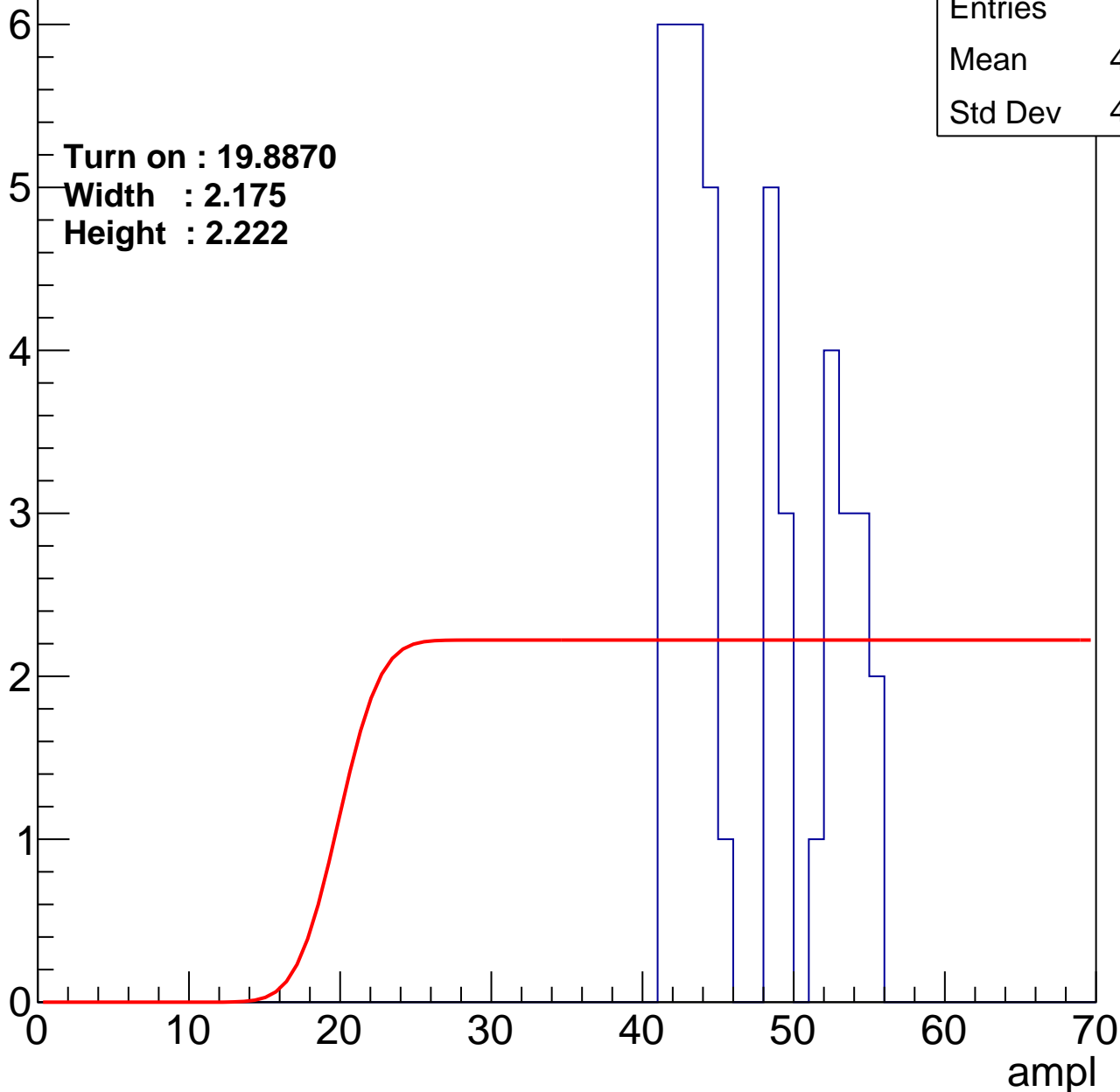
Entry

Entries	45
Mean	46.62
Std Dev	4.762

Turn on : 19.8870

Width : 2.175

Height : 2.222





# B0L100S, U3-ch55

calib\_packv5\_042523\_0143.root, FC#6, port A1

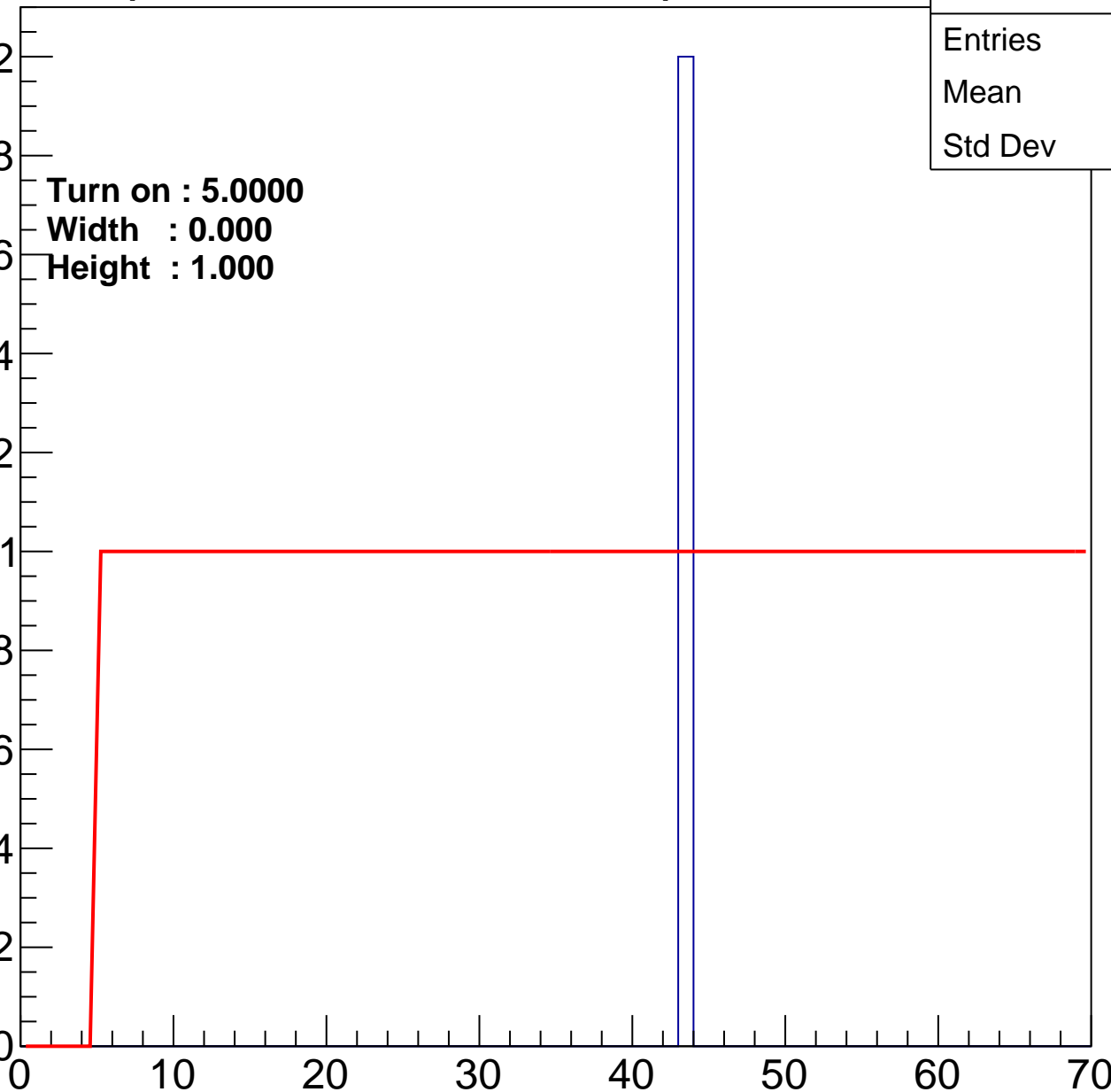
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Turn on : 5.0000  
Width : 0.000  
Height : 1.000

Entries	2
Mean	43
Std Dev	0

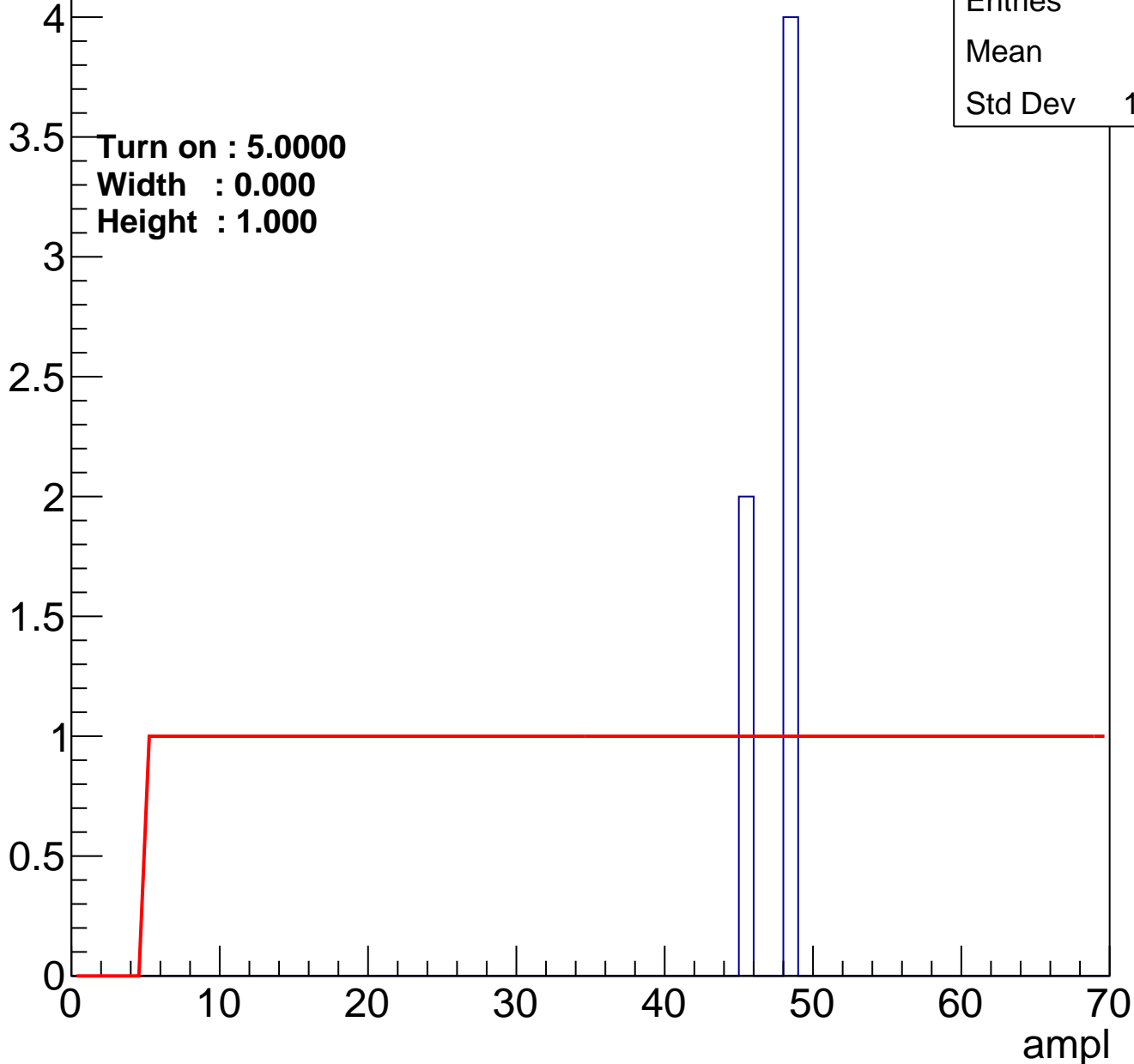
ampl



# B0L100S, U3-ch56

calib\_packv5\_042523\_0143.root, FC#6, port A1

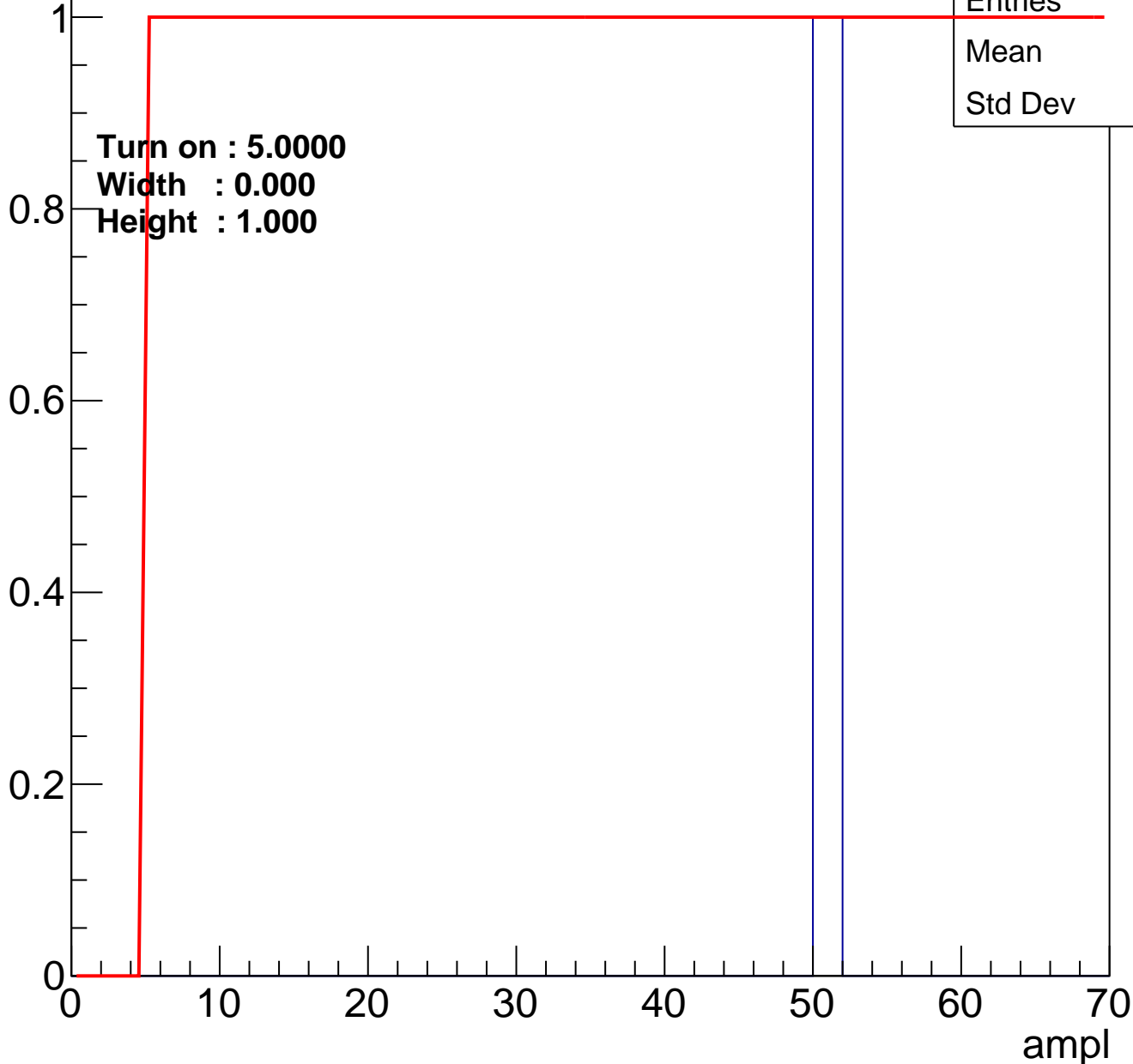
Entry



# B0L100S, U3-ch57

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	2
Mean	50.5
Std Dev	0.5

# B0L100S, U3-ch58

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

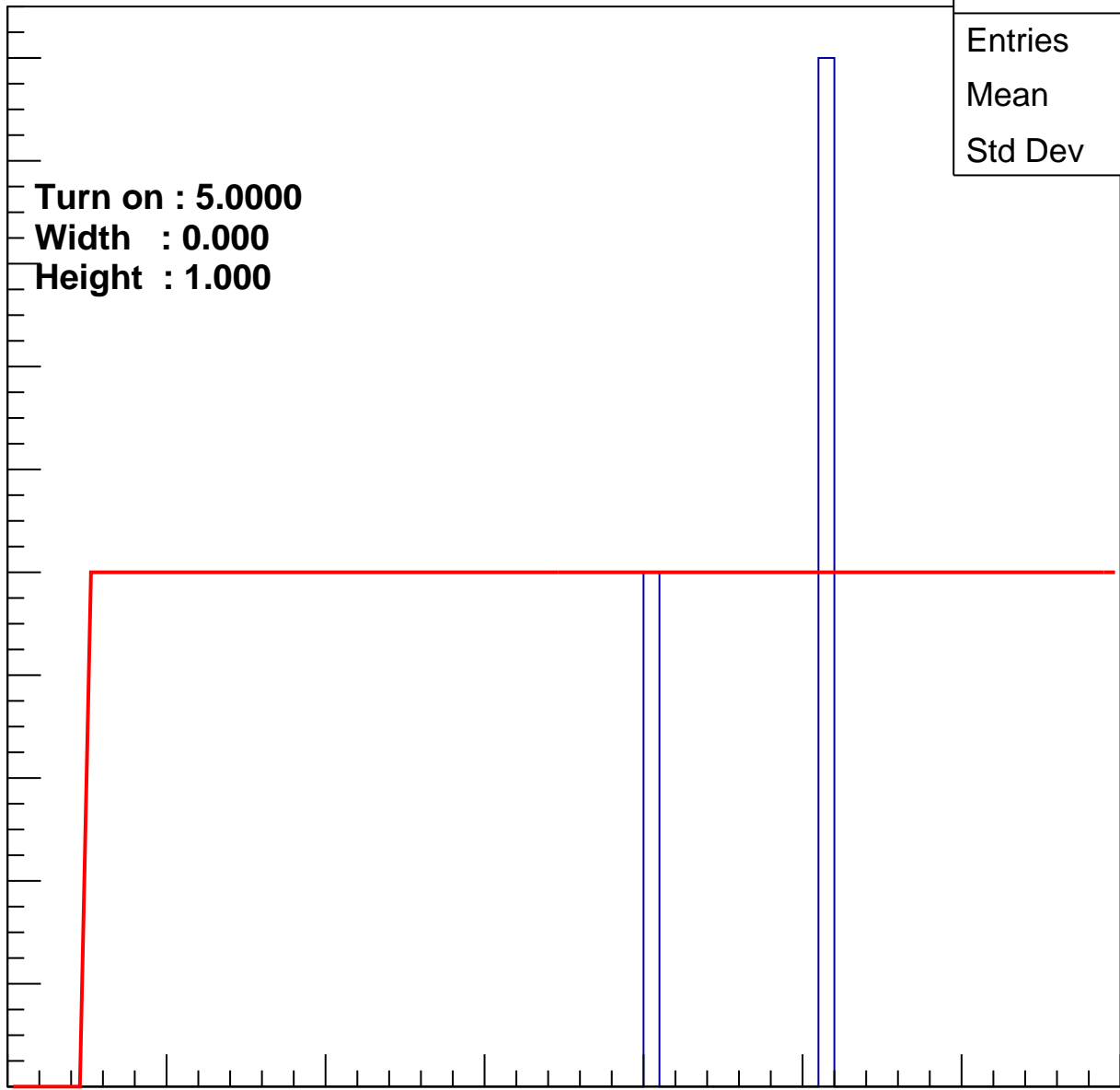
2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Turn on : 5.0000  
Width : 0.000  
Height : 1.000

Entries	3
Mean	47.33
Std Dev	5.185

0 10 20 30 40 50 60 70

ampl



# B0L100S, U3-ch59

calib\_packv5\_042523\_0143.root, FC#6, port A1

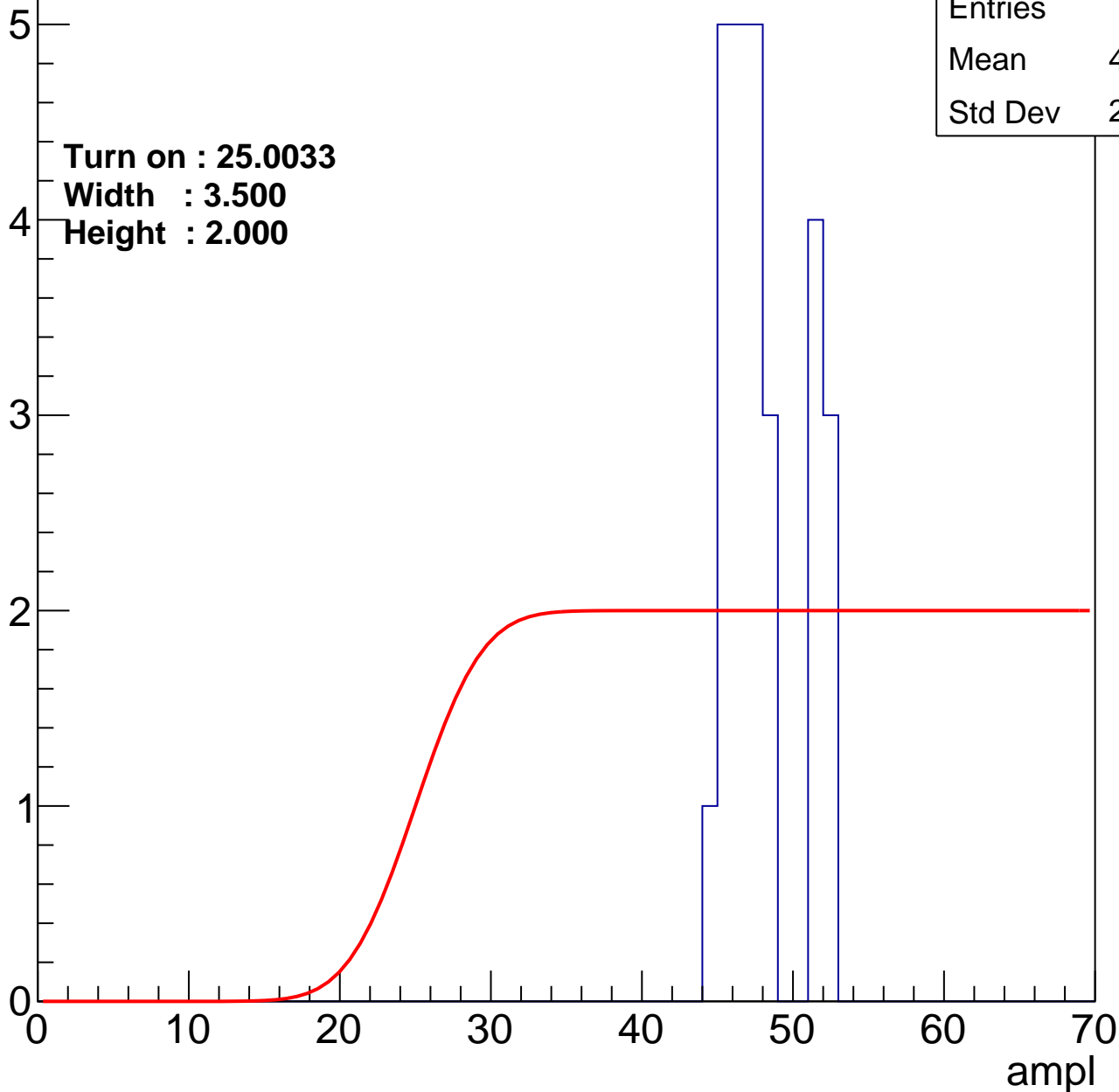
Entry

Entries	26
Mean	47.62
Std Dev	2.528

Turn on : 25.0033

Width : 3.500

Height : 2.000



# B0L100S, U3-ch60

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U3-ch61

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U3-ch62

calib\_packv5\_042523\_0143.root, FC#6, port A1

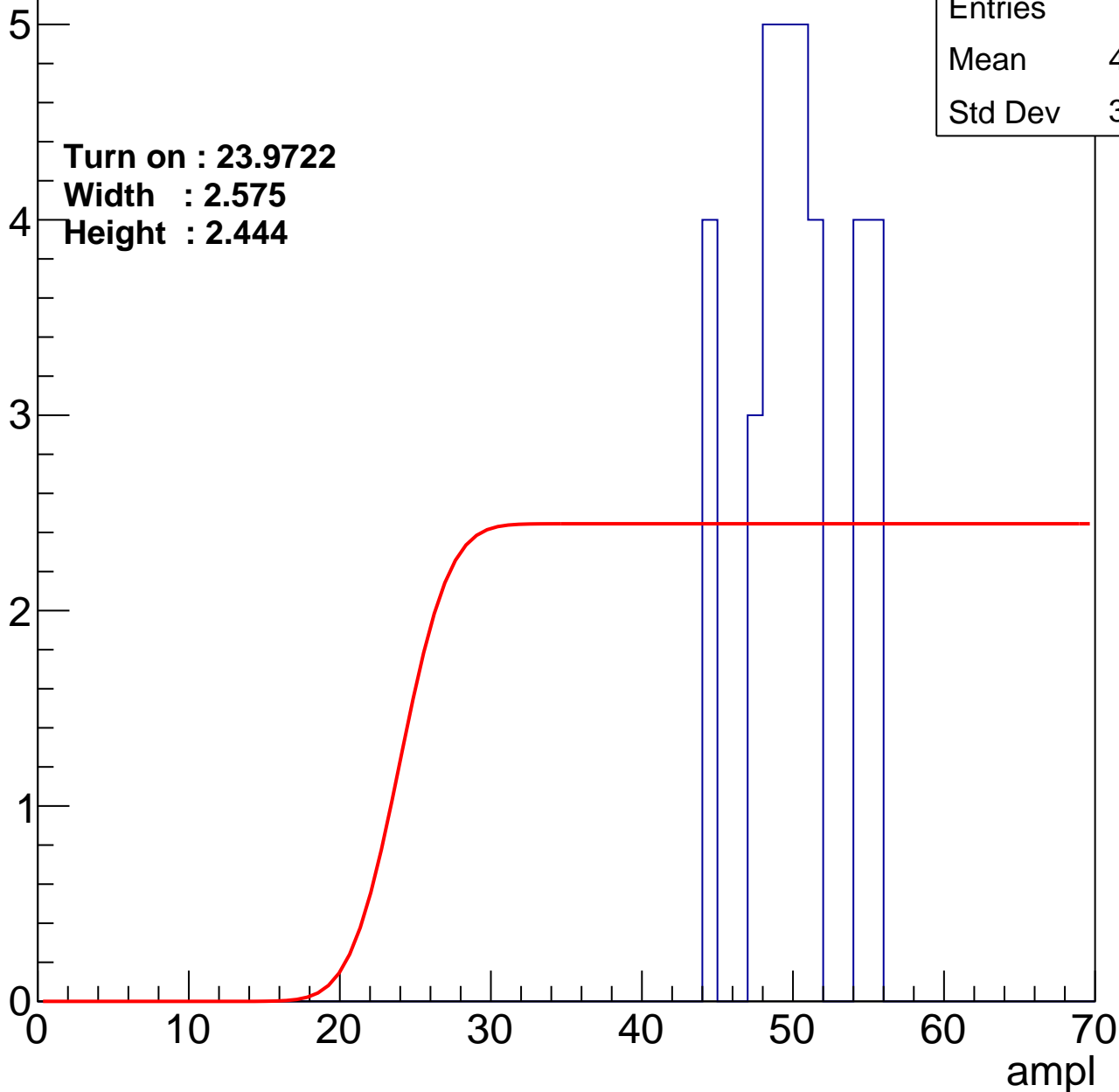
Entry

Entries	34
Mean	49.76
Std Dev	3.264

Turn on : 23.9722

Width : 2.575

Height : 2.444





# B0L100S, U3-ch63

calib\_packv5\_042523\_0143.root, FC#6, port A1

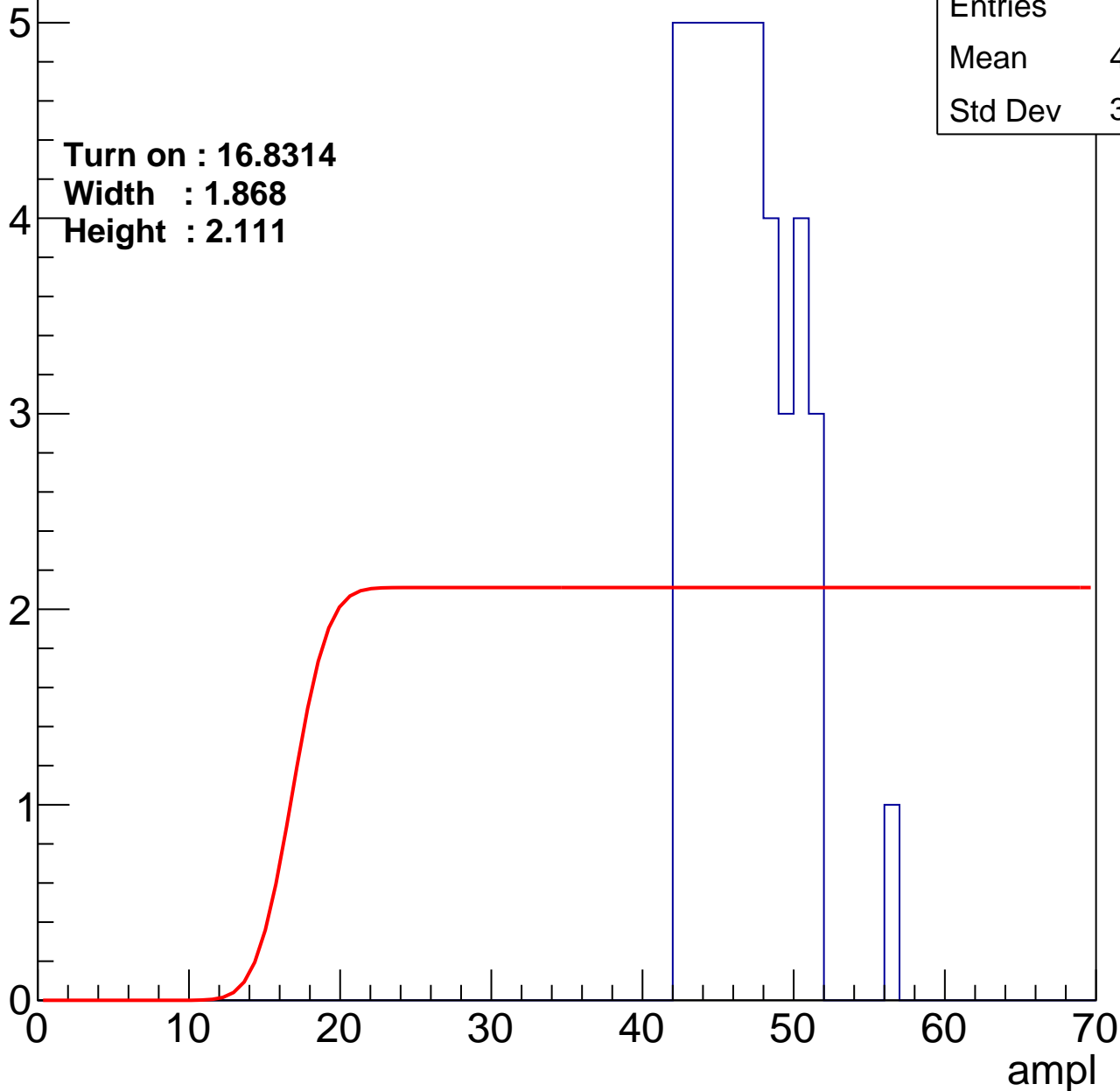
Entry

Entries	45
Mean	46.29
Std Dev	3.103

Turn on : 16.8314

Width : 1.868

Height : 2.111



# B0L100S, U3-ch64

calib\_packv5\_042523\_0143.root, FC#6, port A1

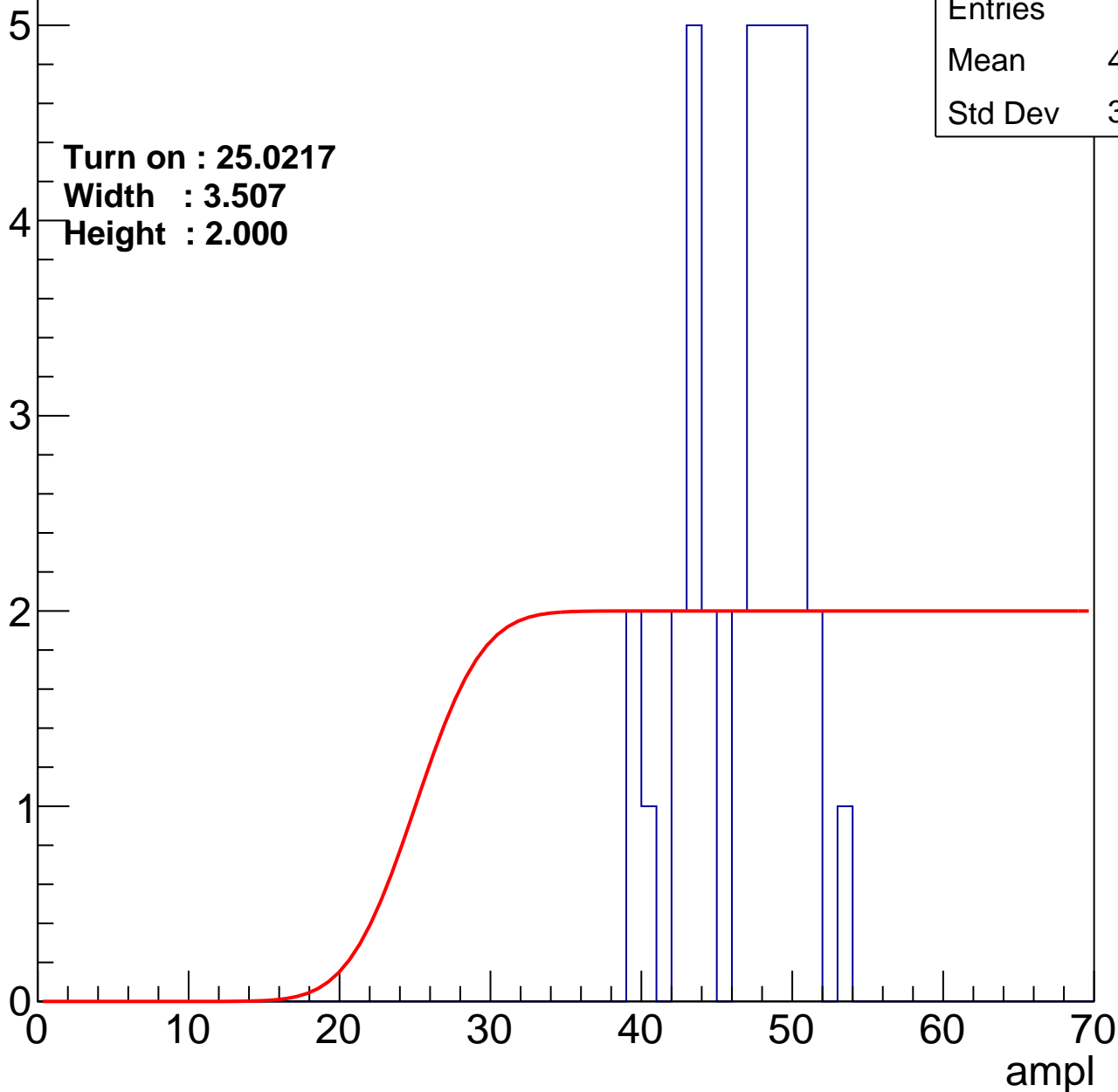
Entry

Entries	37
Mean	46.54
Std Dev	3.515

Turn on : 25.0217

Width : 3.507

Height : 2.000



# B0L100S, U3-ch65

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

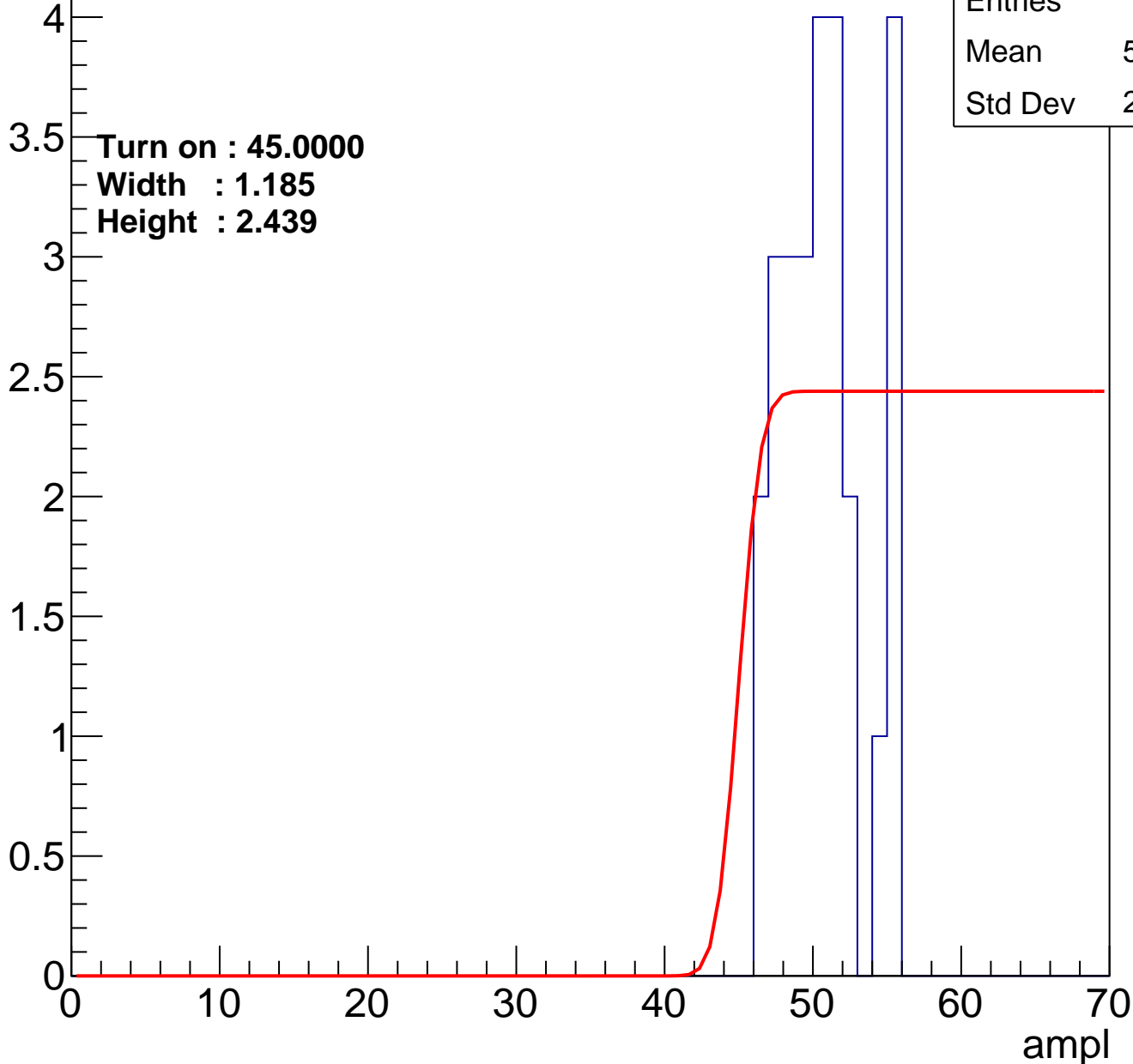


Entries	0
Mean	0
Std Dev	0

# B0L100S, U3-ch66

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U3-ch67

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

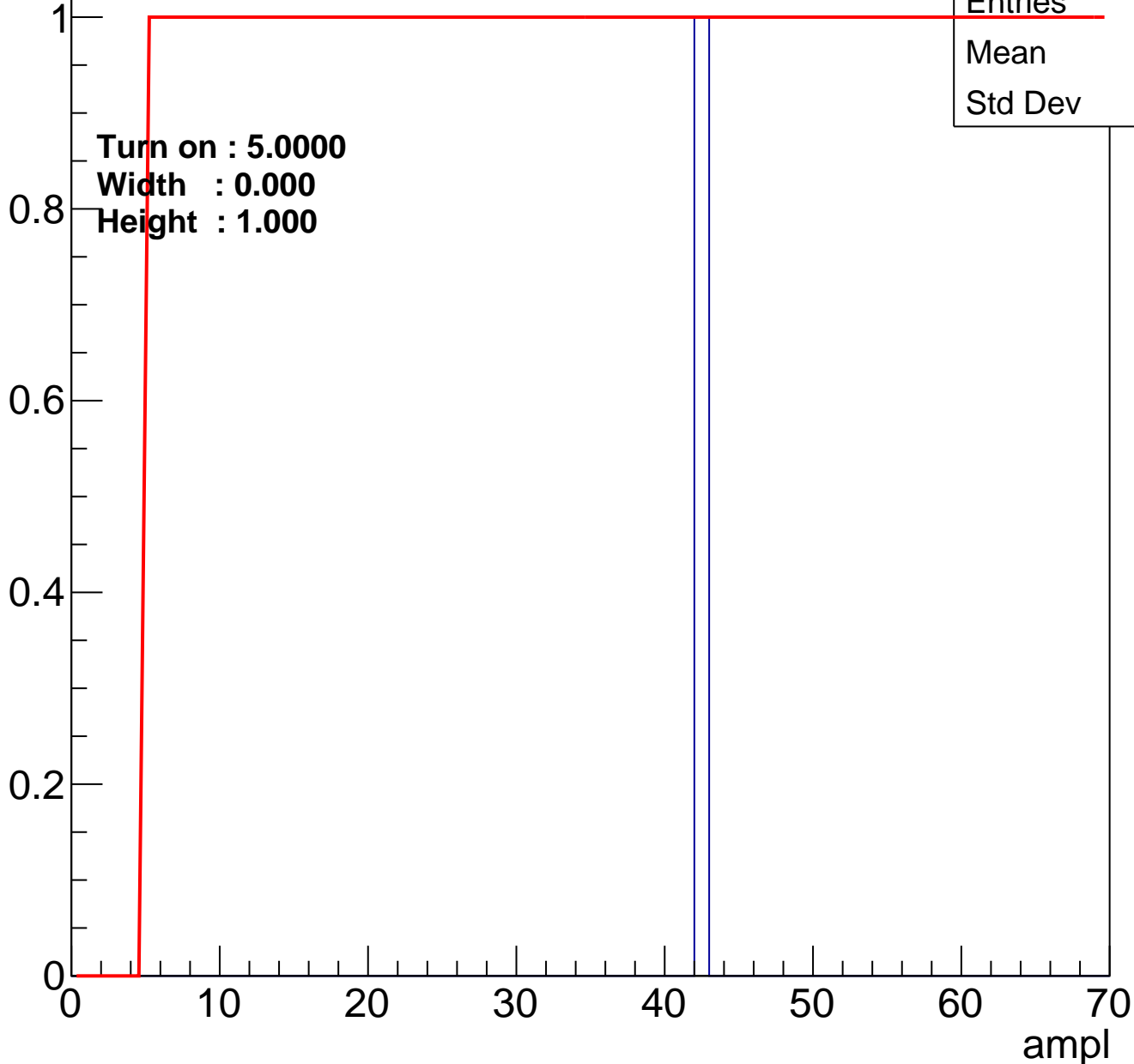


Entries	0
Mean	0
Std Dev	0

# B0L100S, U3-ch68

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	1
Mean	42
Std Dev	0

# B0L100S, U3-ch69

calib\_packv5\_042523\_0143.root, FC#6, port A1

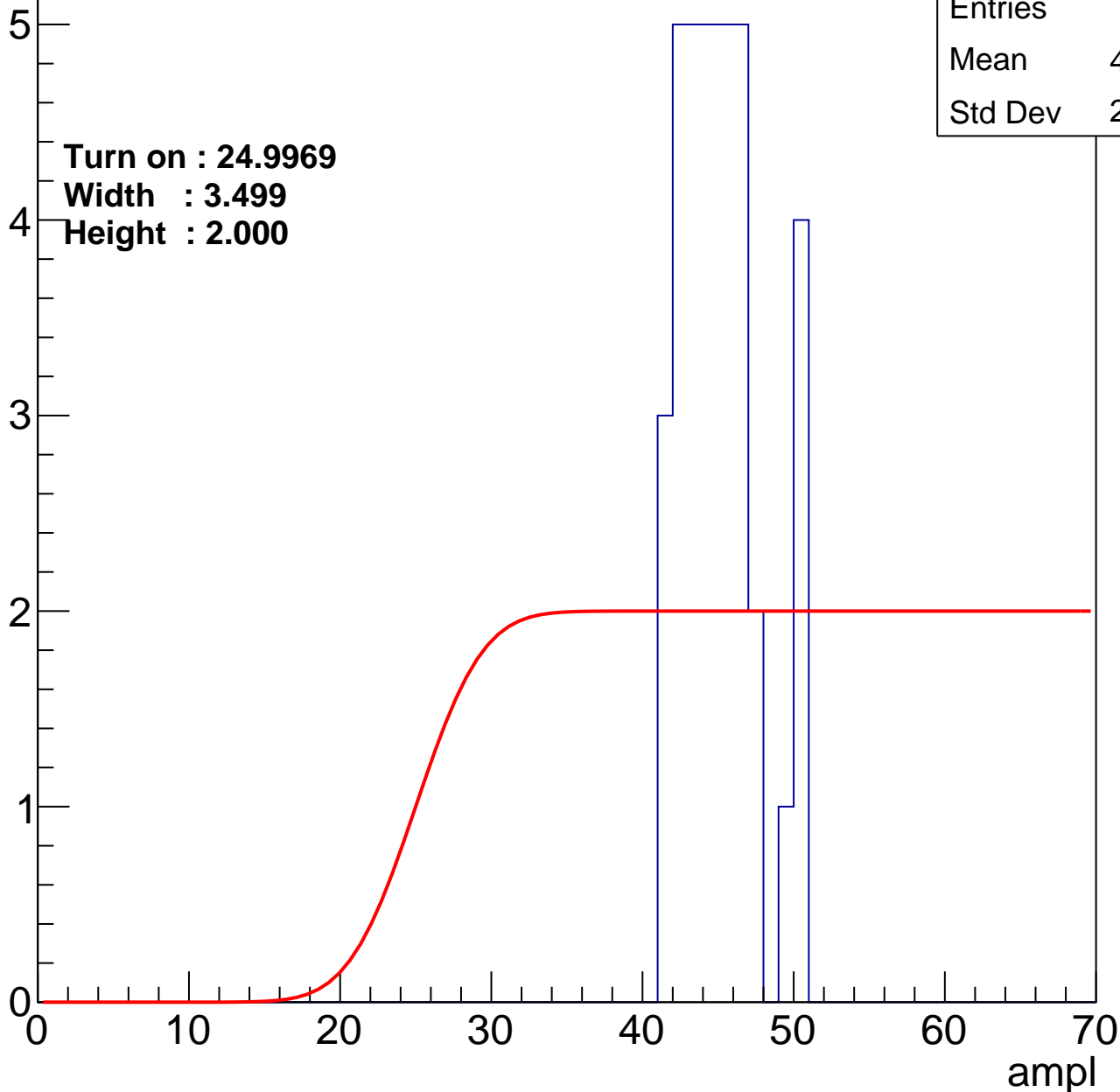
Entry

Entries	35
Mean	44.74
Std Dev	2.644

Turn on : 24.9969

Width : 3.499

Height : 2.000



# B0L100S, U3-ch70

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



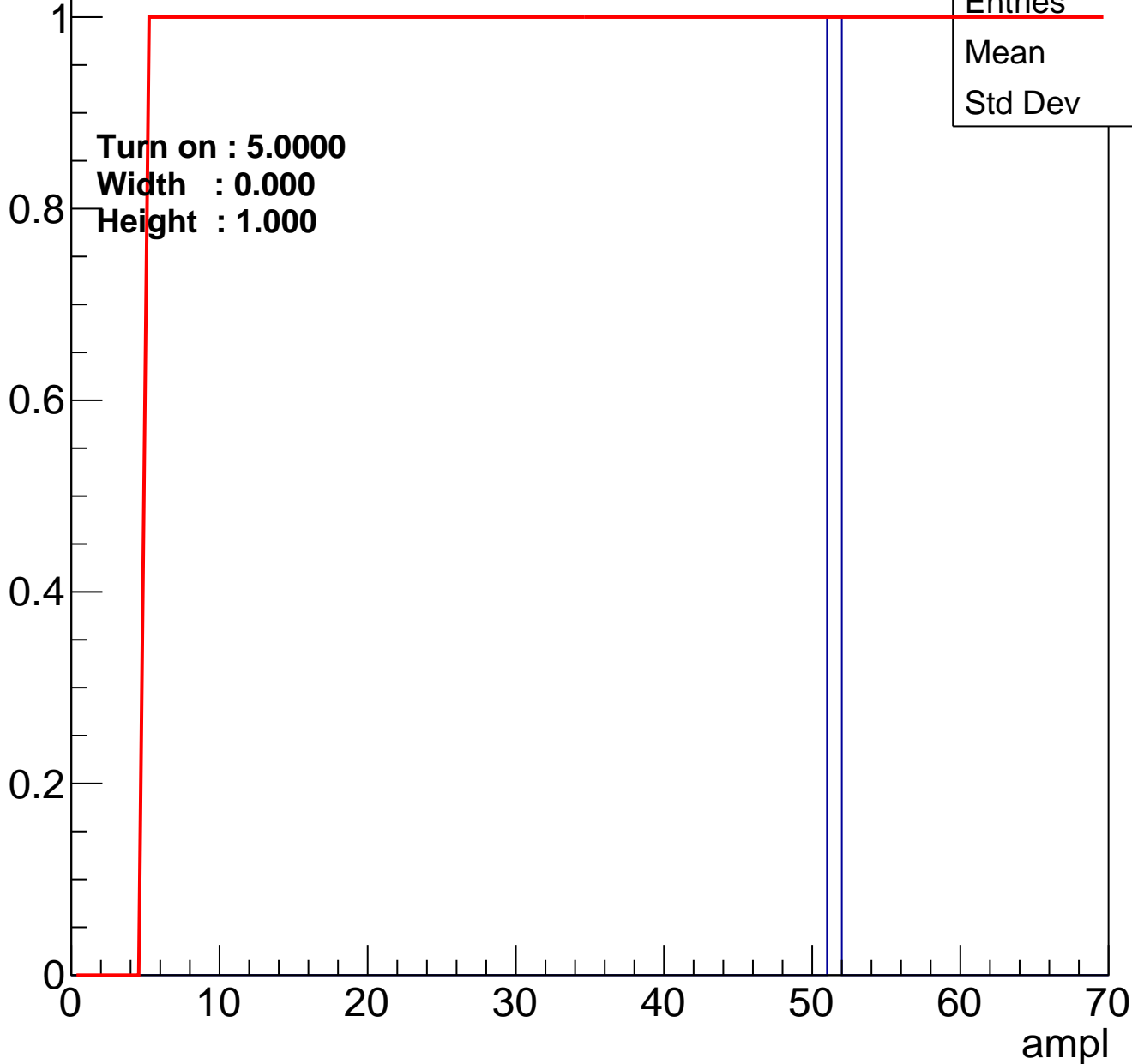
Entries	0
Mean	0
Std Dev	0



# B0L100S, U3-ch71

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U3-ch72

calib\_packv5\_042523\_0143.root, FC#6, port A1

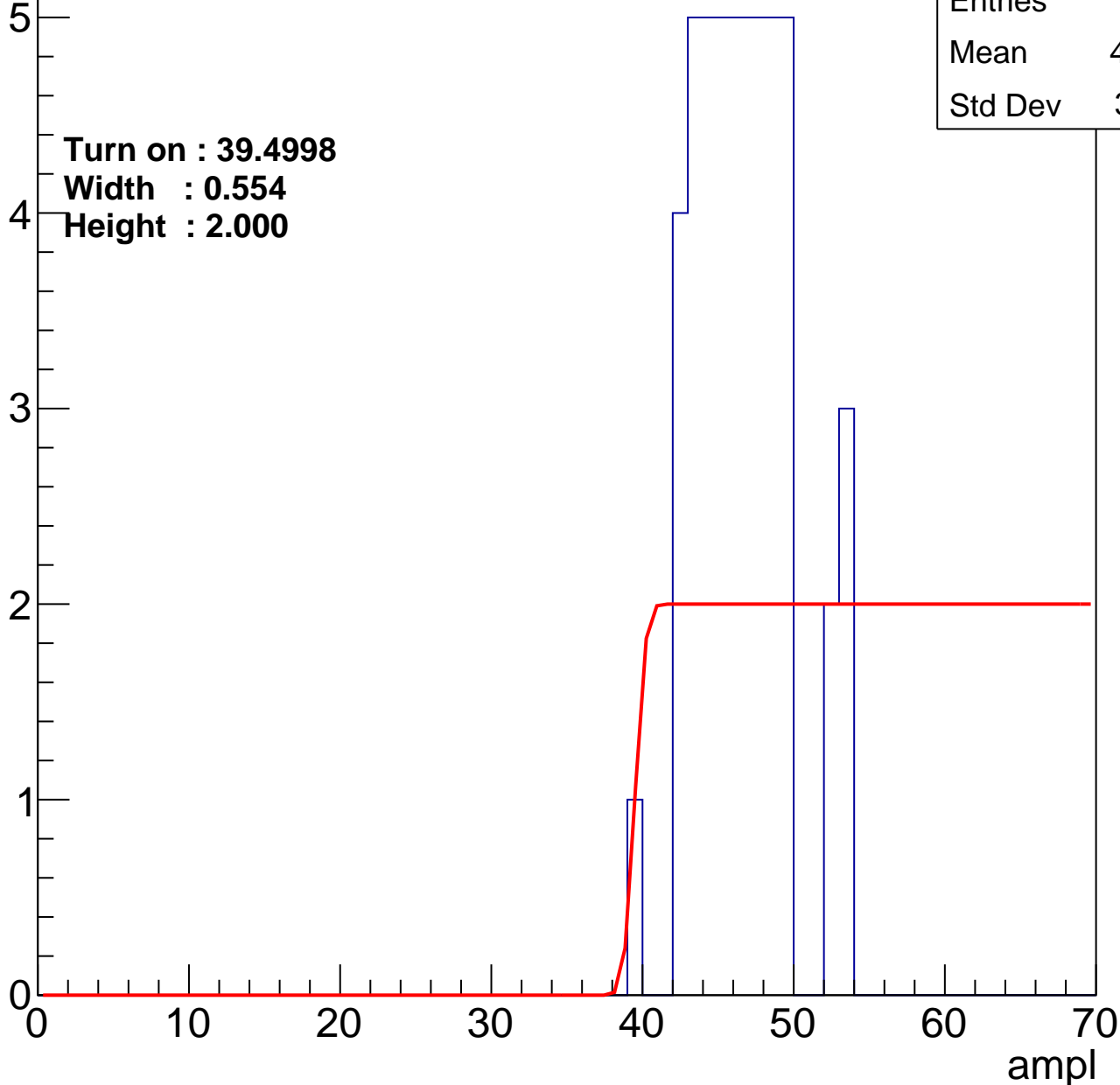
Entry

Entries	45
Mean	46.22
Std Dev	3.231

Turn on : 39.4998

Width : 0.554

Height : 2.000



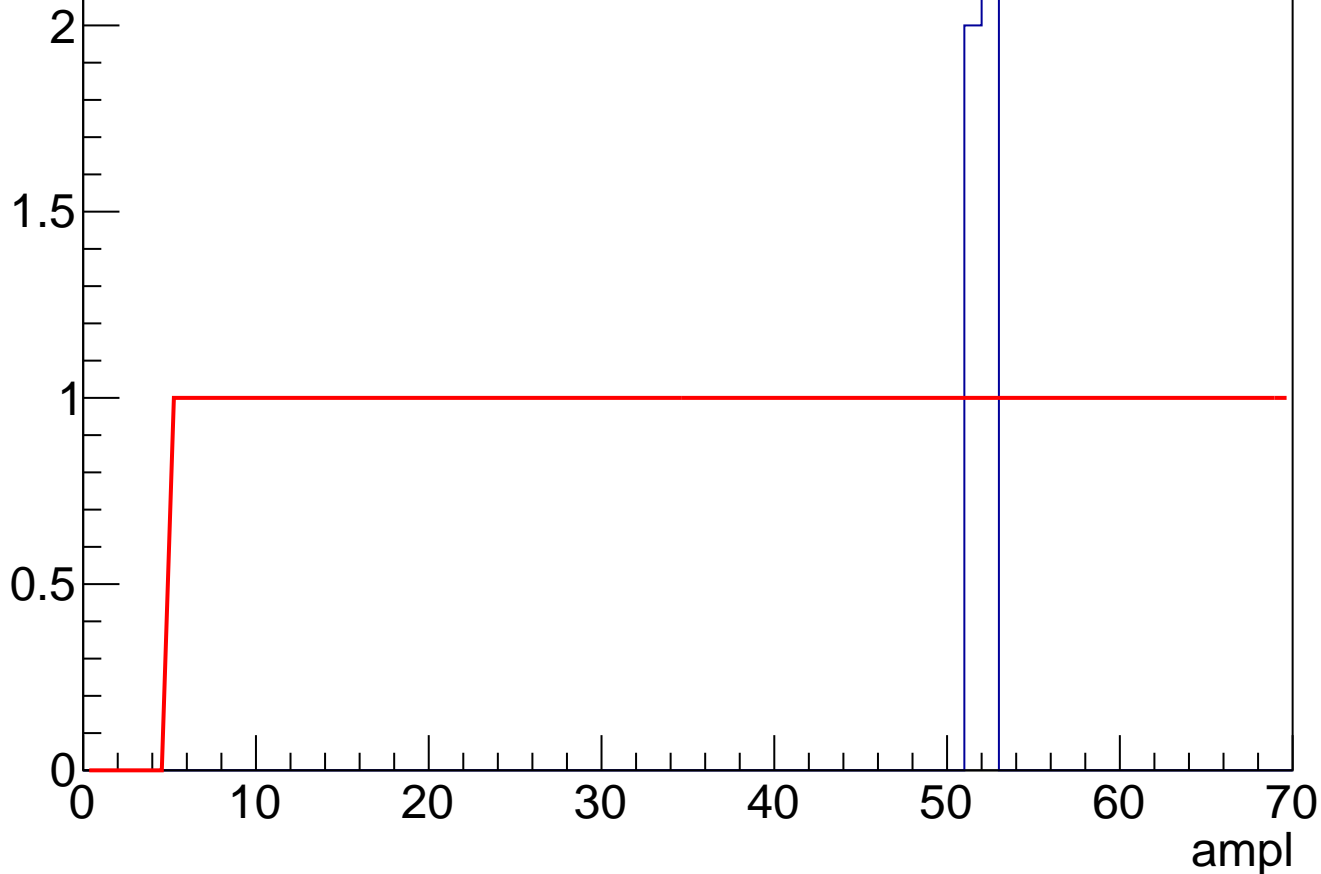
# B0L100S, U3-ch73

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

Turn on : 5.0000  
Width : 0.000  
Height : 1.000

Entries	5
Mean	51.6
Std Dev	0.4899



# B0L100S, U3-ch74

calib\_packv5\_042523\_0143.root, FC#6, port A1

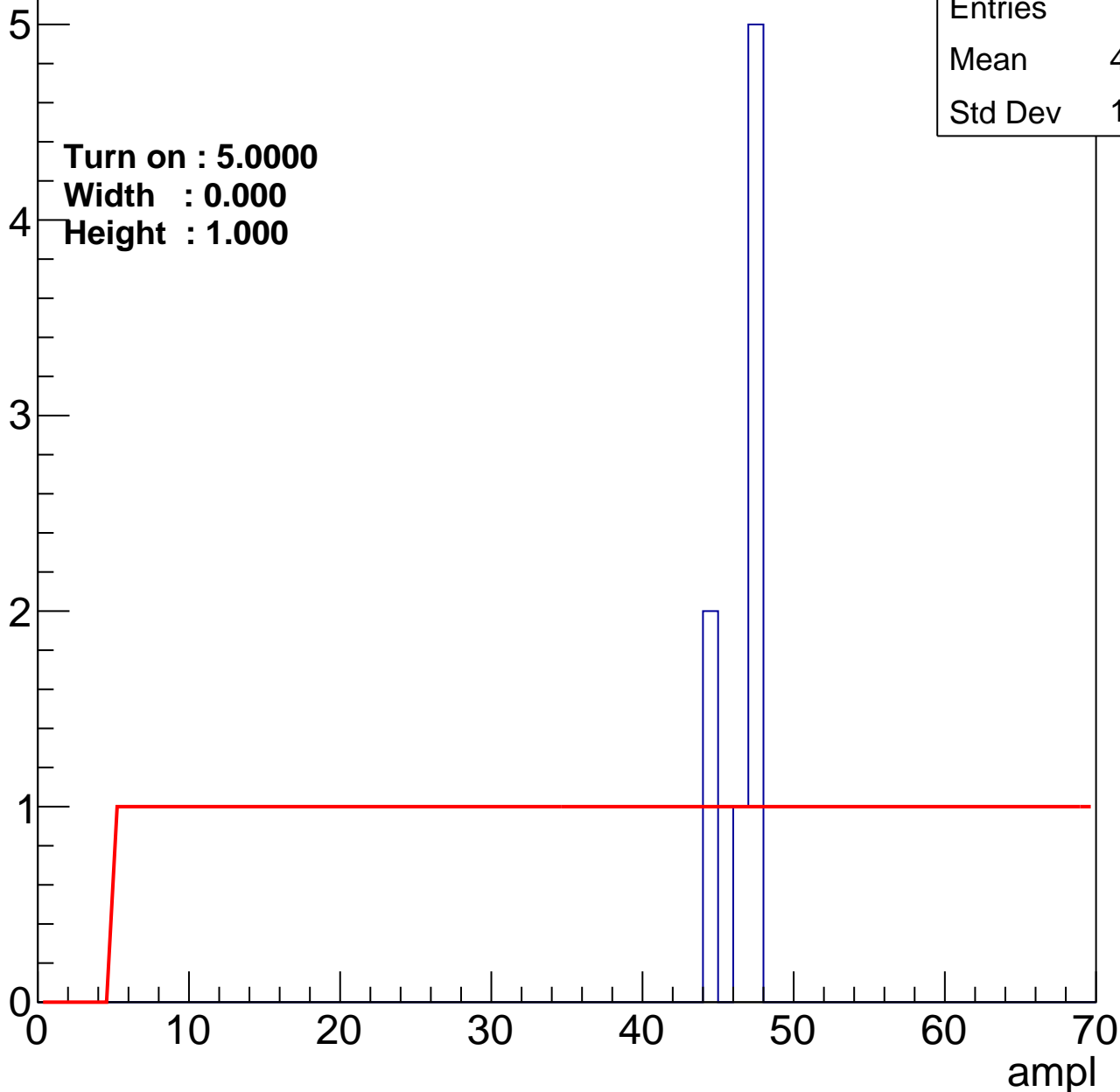
Entry

Entries	8
Mean	46.12
Std Dev	1.269

Turn on : 5.0000

Width : 0.000

Height : 1.000



# B0L100S, U3-ch75

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U3-ch76

calib\_packv5\_042523\_0143.root, FC#6, port A1

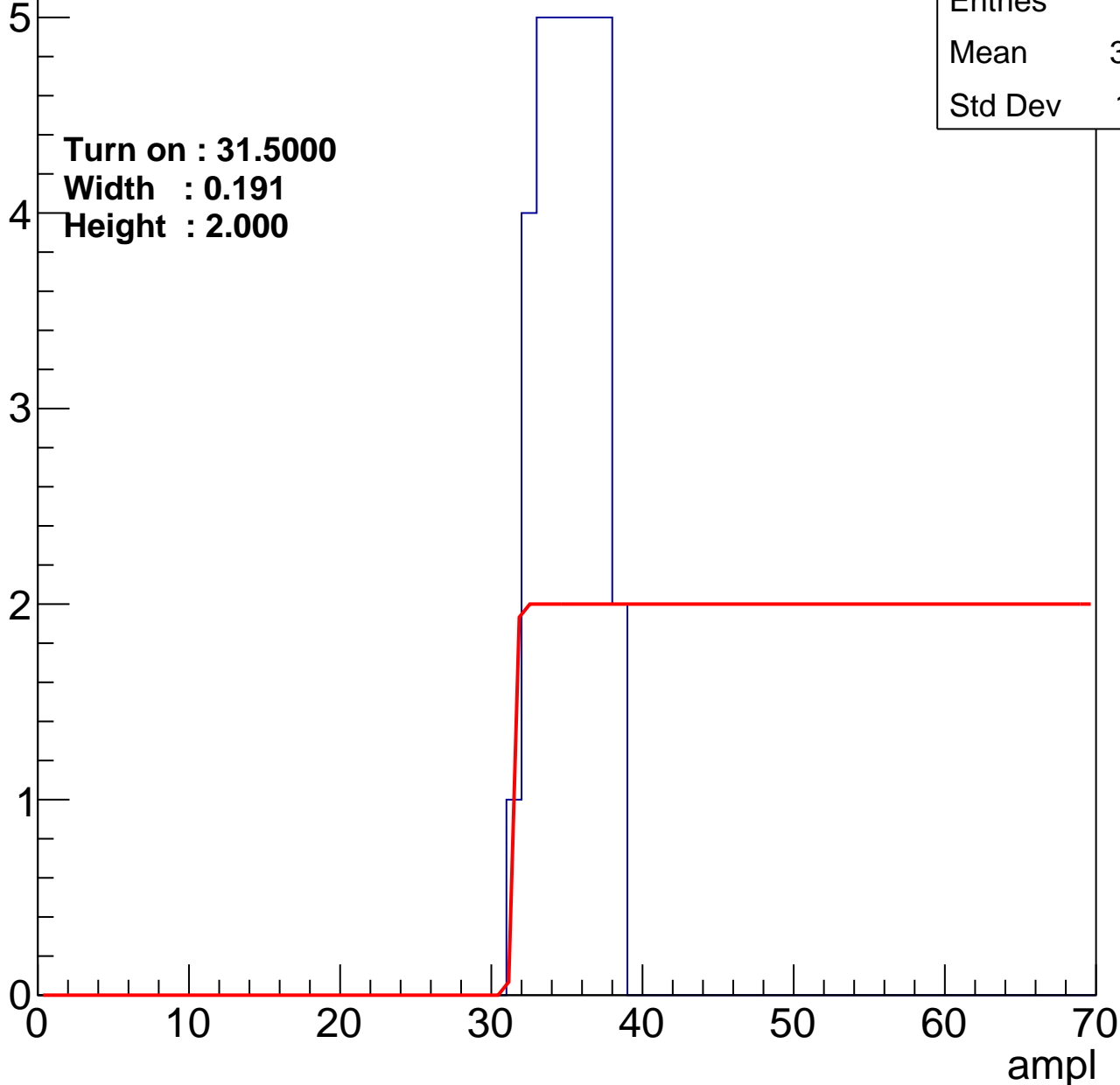
Entry

Entries	32
Mean	34.69
Std Dev	1.911

Turn on : 31.5000

Width : 0.191

Height : 2.000



# B0L100S, U3-ch77

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U3-ch78

calib\_packv5\_042523\_0143.root, FC#6, port A1

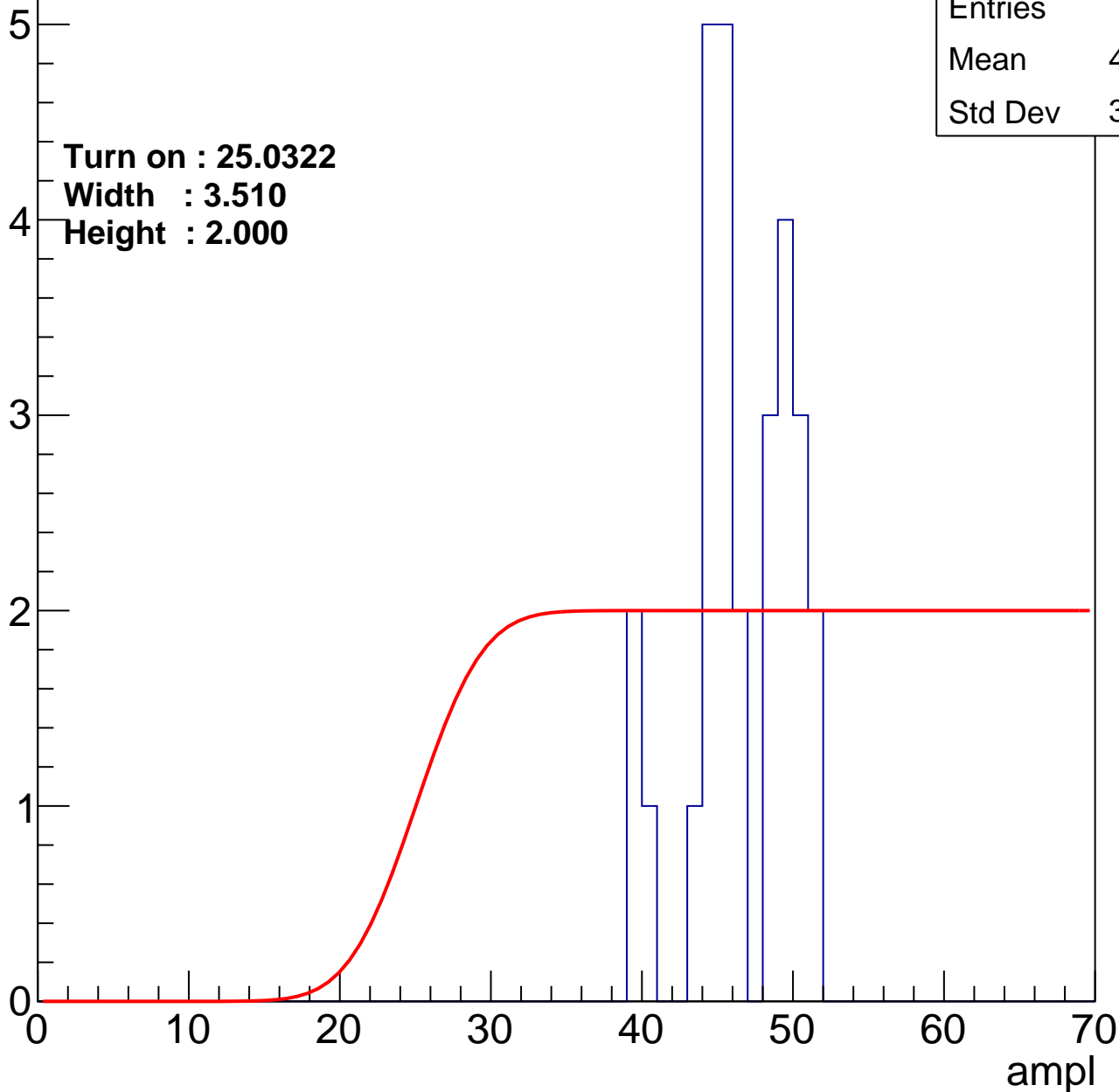
Entry

Entries	28
Mean	46.07
Std Dev	3.348

Turn on : 25.0322

Width : 3.510

Height : 2.000





# B0L100S, U3-ch79

calib\_packv5\_042523\_0143.root, FC#6, port A1

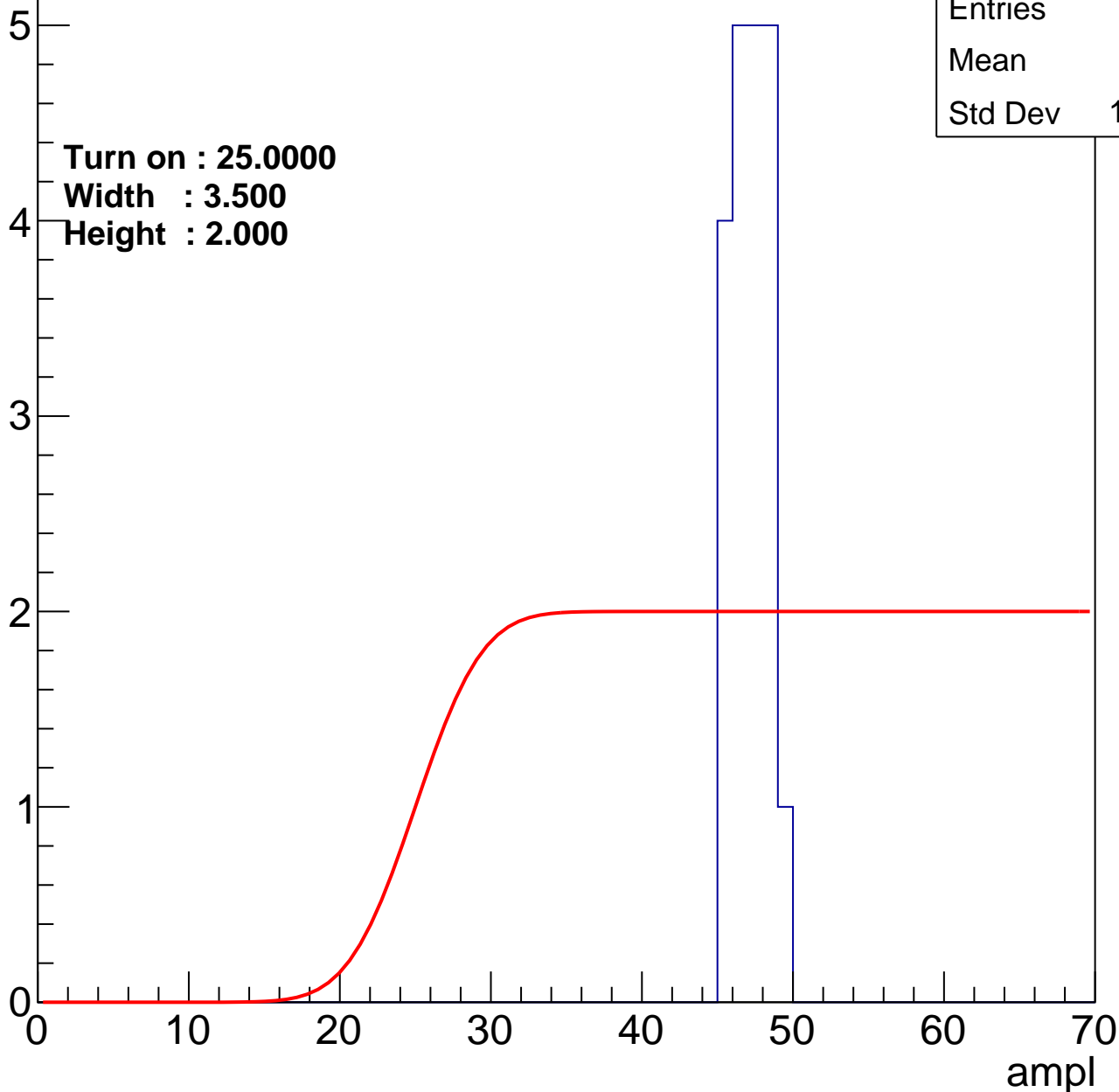
Entry

Entries	20
Mean	46.7
Std Dev	1.187

Turn on : 25.0000

Width : 3.500

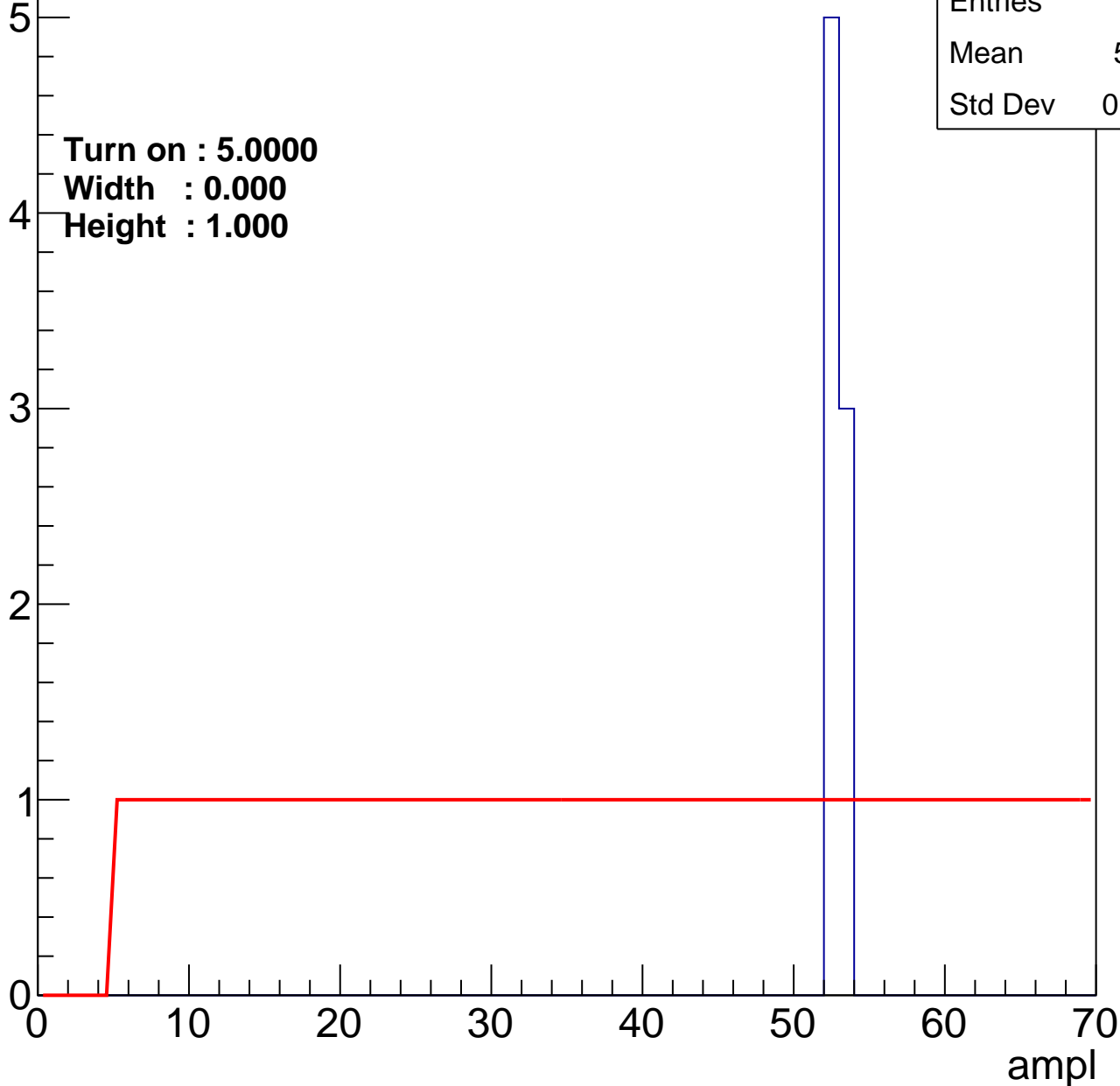
Height : 2.000



# B0L100S, U3-ch80

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



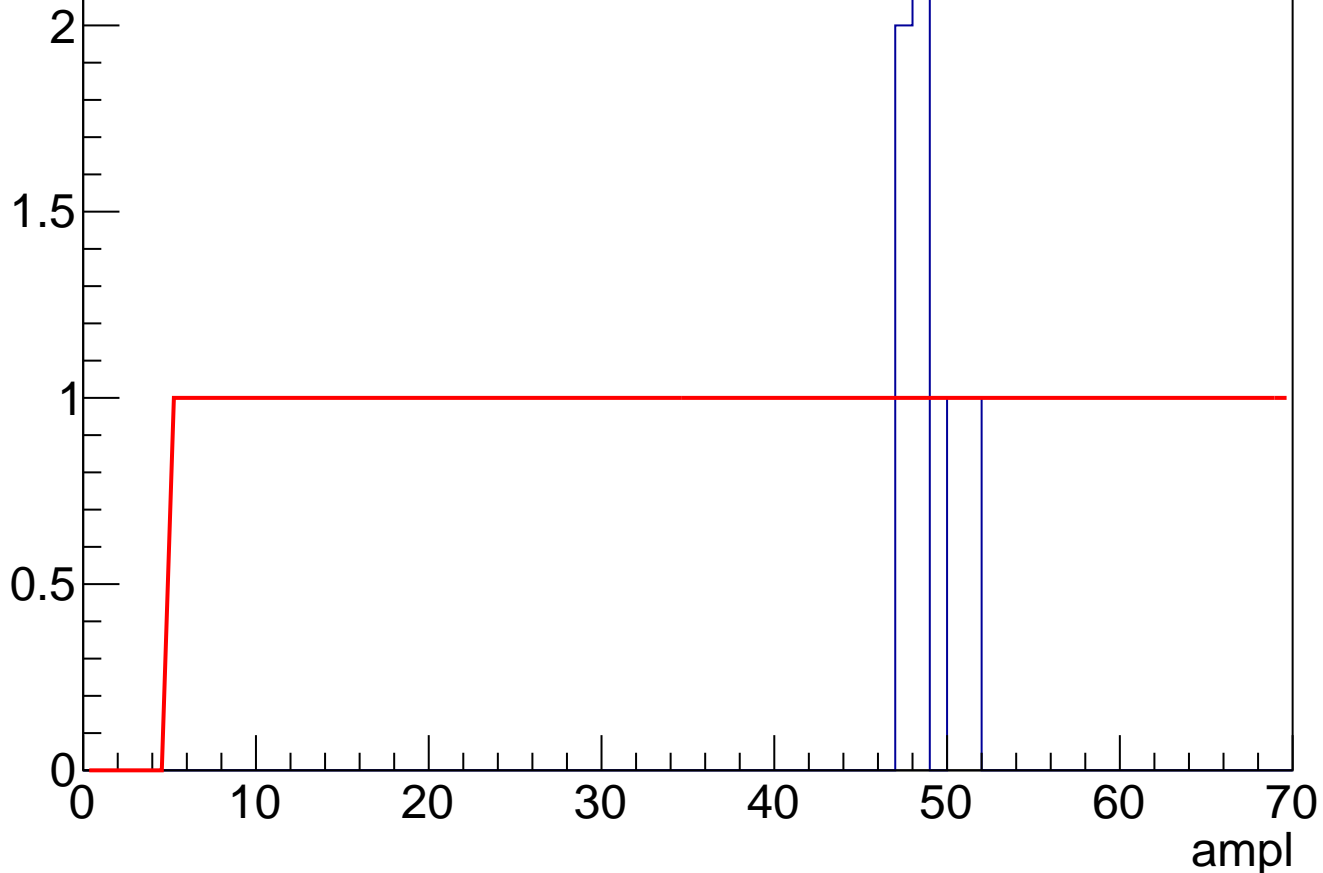
# B0L100S, U3-ch81

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

Turn on : 5.0000  
Width : 0.000  
Height : 1.000

Entries	7
Mean	48.43
Std Dev	1.4



# B0L100S, U3-ch82

calib\_packv5\_042523\_0143.root, FC#6, port A1

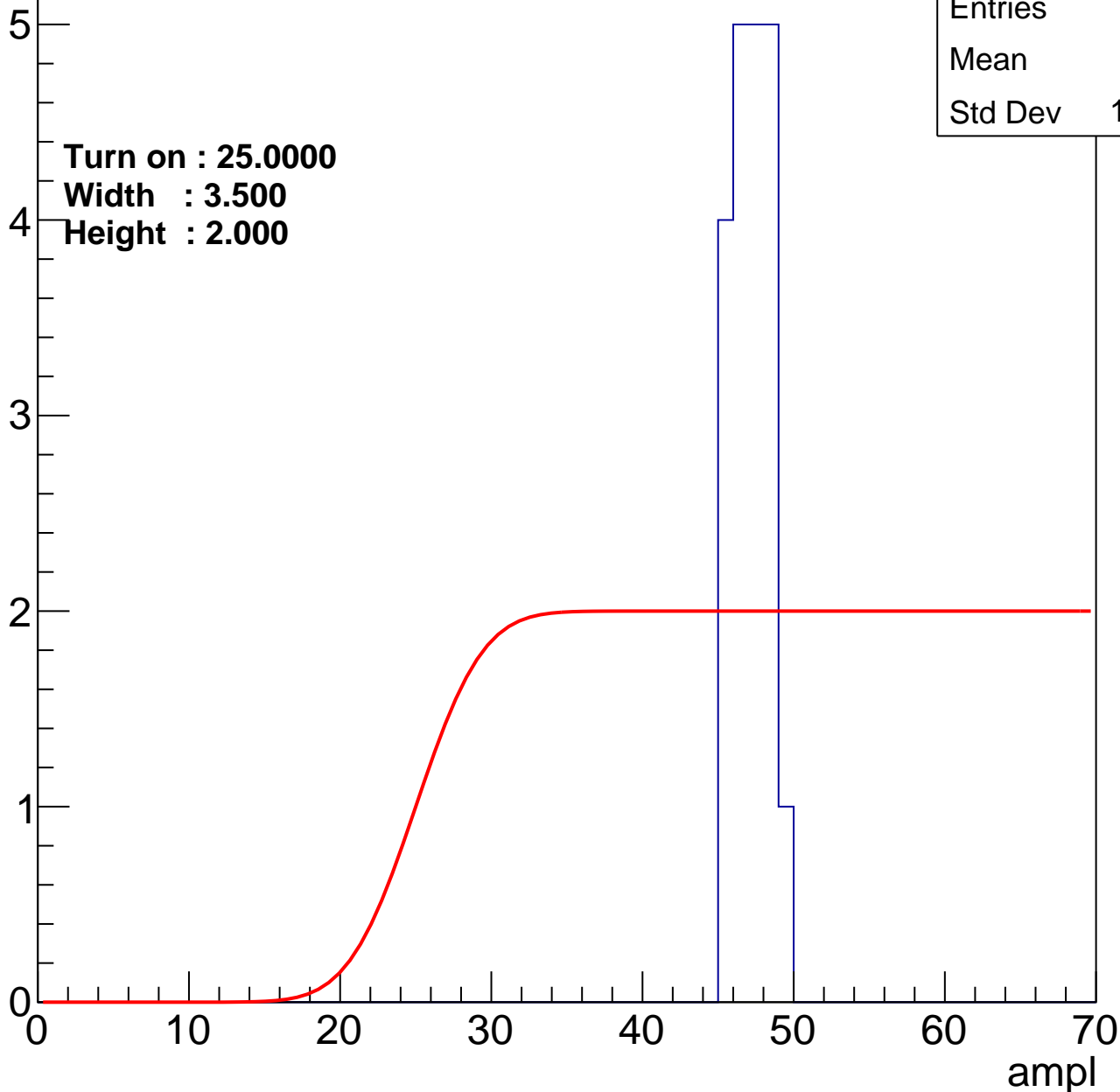
Entry

Entries	20
Mean	46.7
Std Dev	1.187

Turn on : 25.0000

Width : 3.500

Height : 2.000



# B0L100S, U3-ch83

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U3-ch84

calib\_packv5\_042523\_0143.root, FC#6, port A1

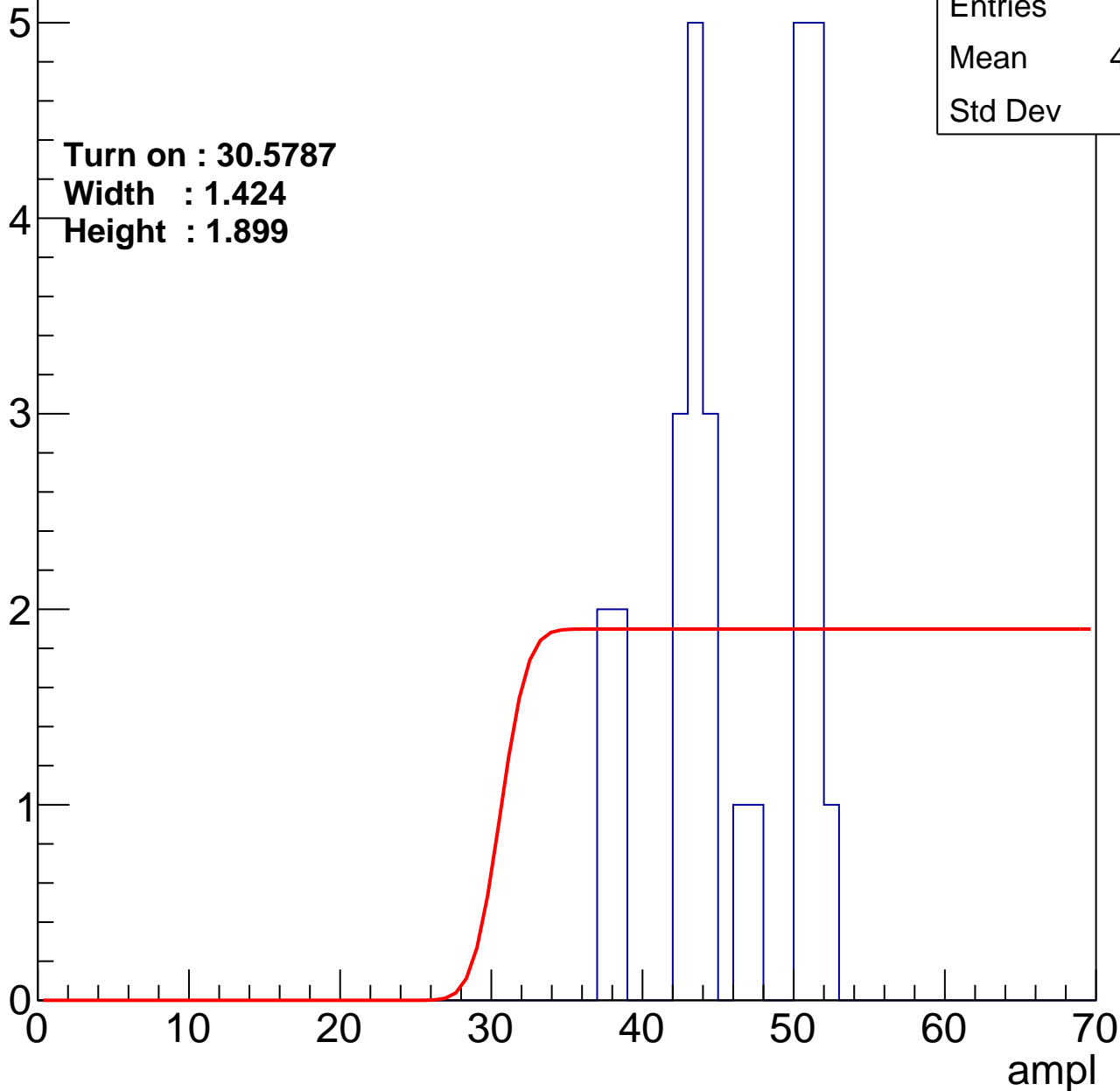
Entry

Entries	28
Mean	45.46
Std Dev	4.74

Turn on : 30.5787

Width : 1.424

Height : 1.899



# B0L100S, U3-ch85

calib\_packv5\_042523\_0143.root, FC#6, port A1

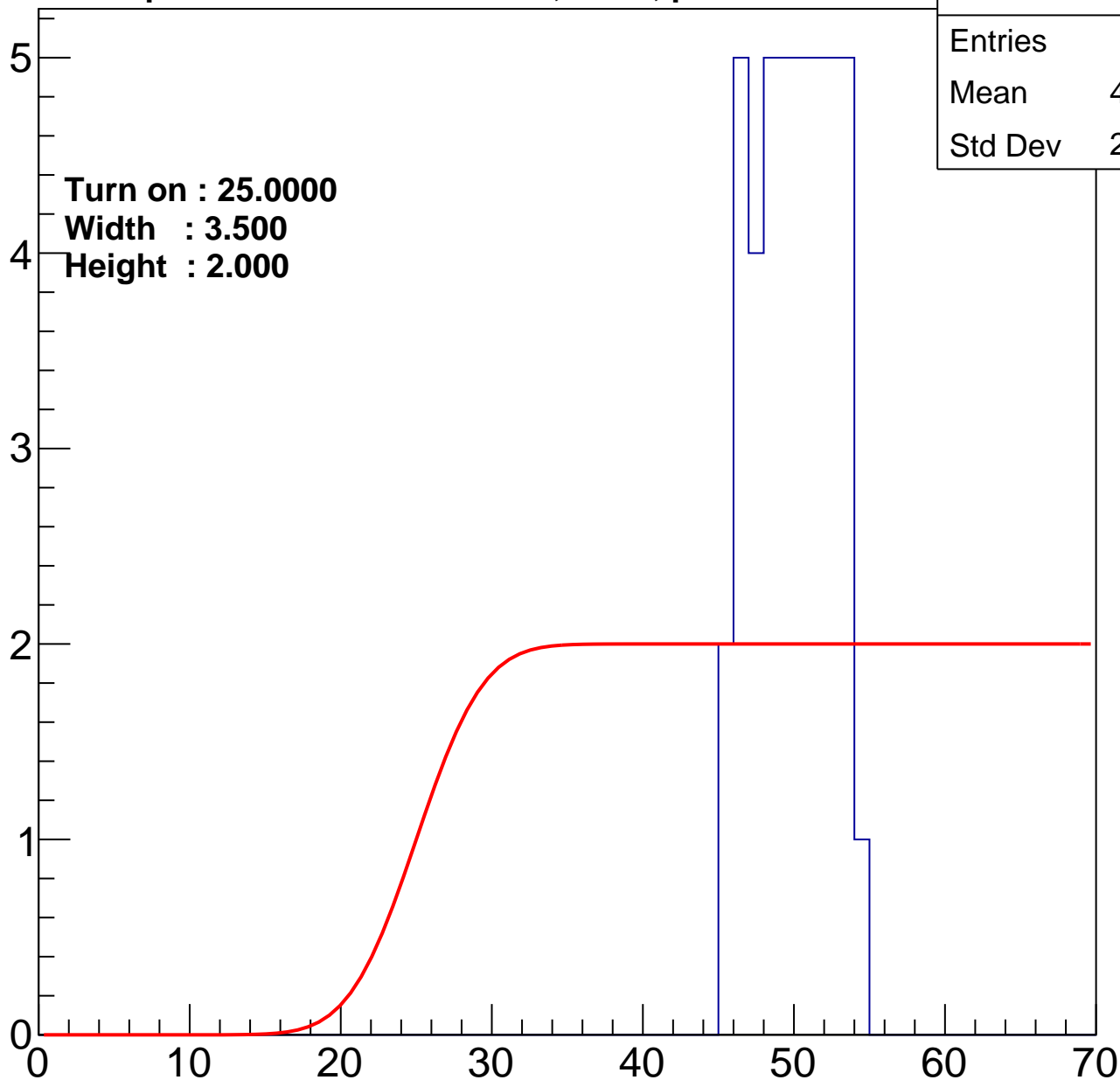
Entry

5  
4  
3  
2  
1  
0

Turn on : 25.0000  
Width : 3.500  
Height : 2.000

Entries	42
Mean	49.45
Std Dev	2.509

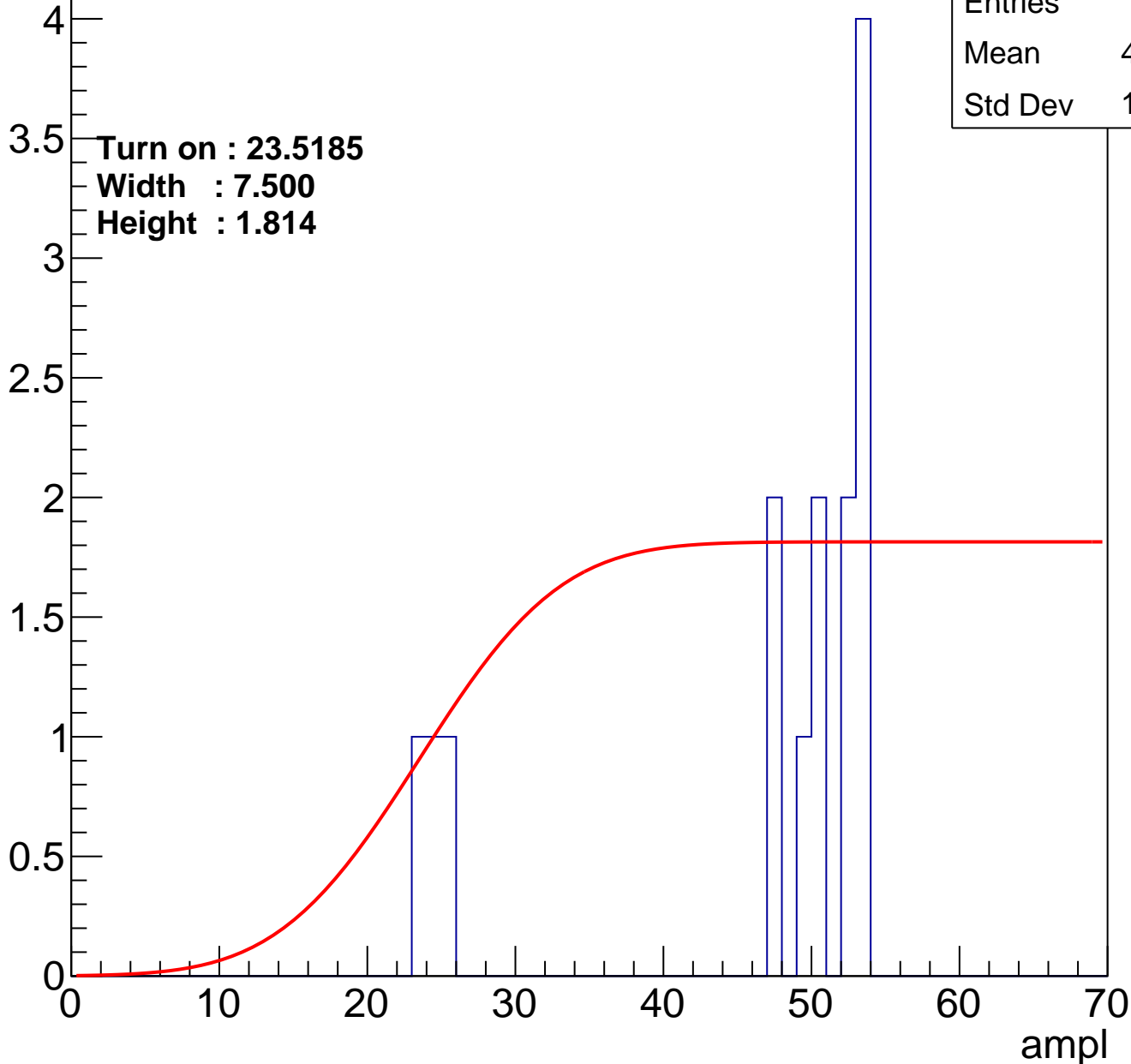
ampl



# B0L100S, U3-ch86

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry





# B0L100S, U3-ch87

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U3-ch88

calib\_packv5\_042523\_0143.root, FC#6, port A1

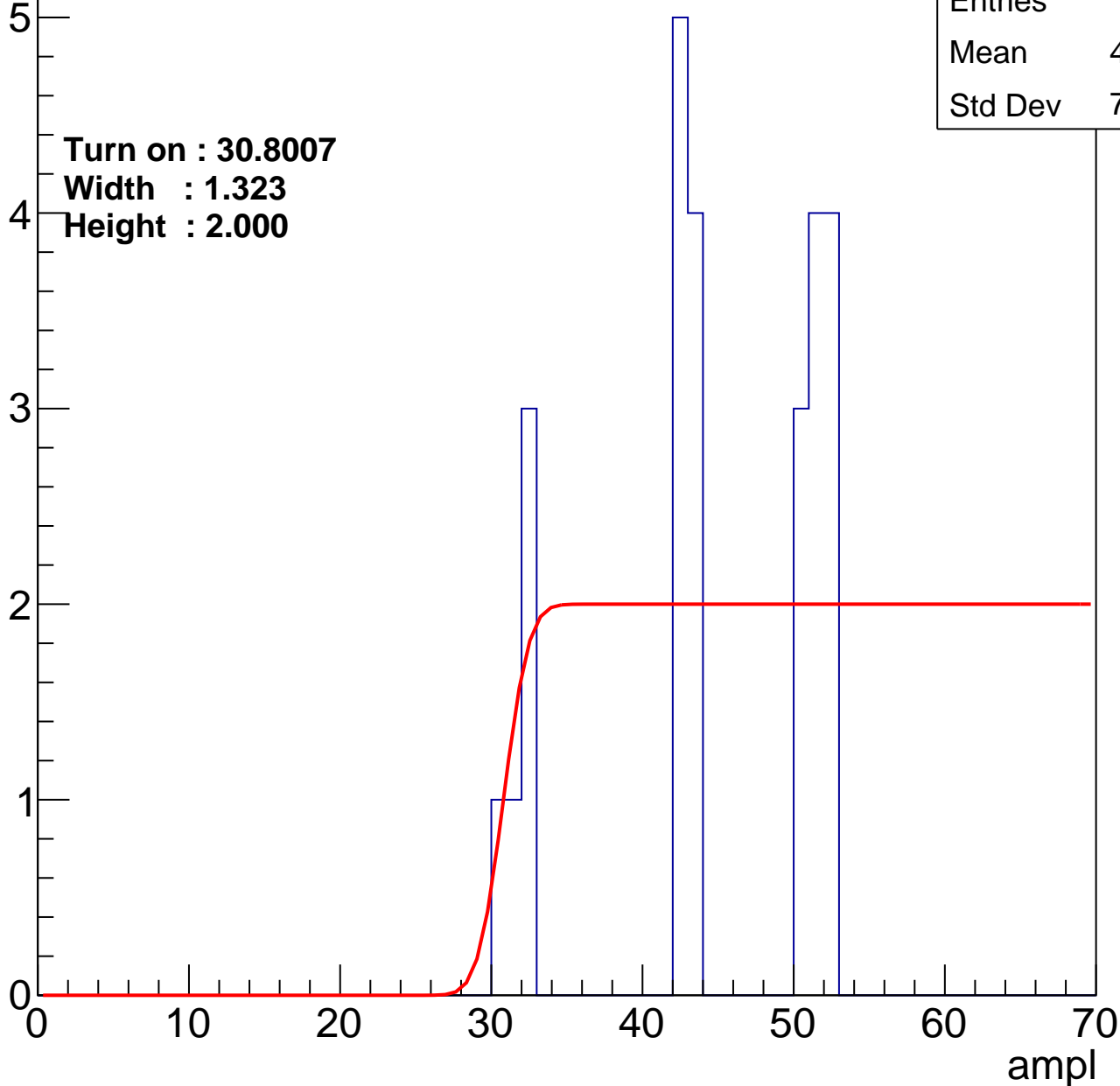
Entry

Entries	25
Mean	44.04
Std Dev	7.432

Turn on : 30.8007

Width : 1.323

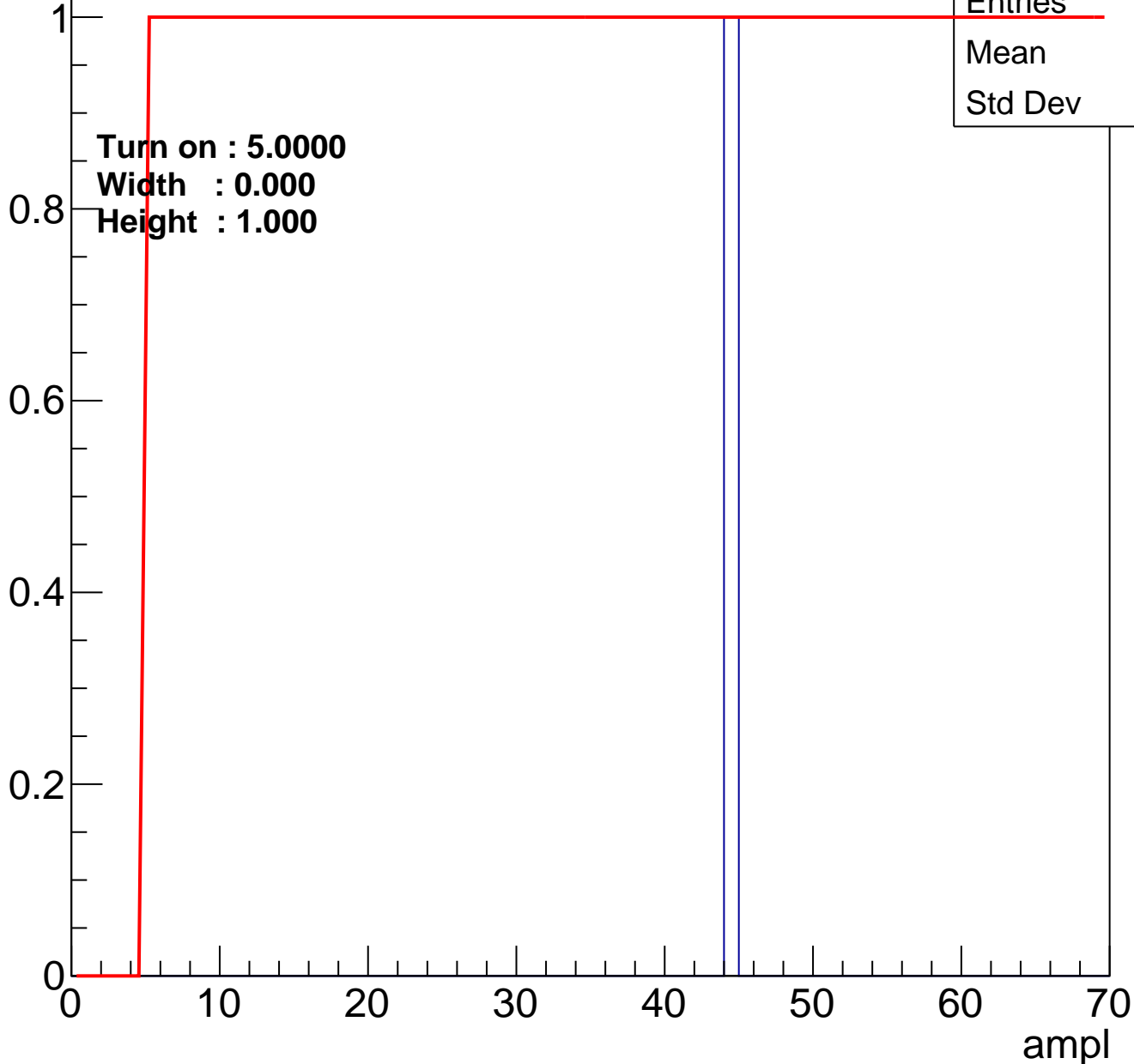
Height : 2.000



# B0L100S, U3-ch89

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U3-ch90

calib\_packv5\_042523\_0143.root, FC#6, port A1

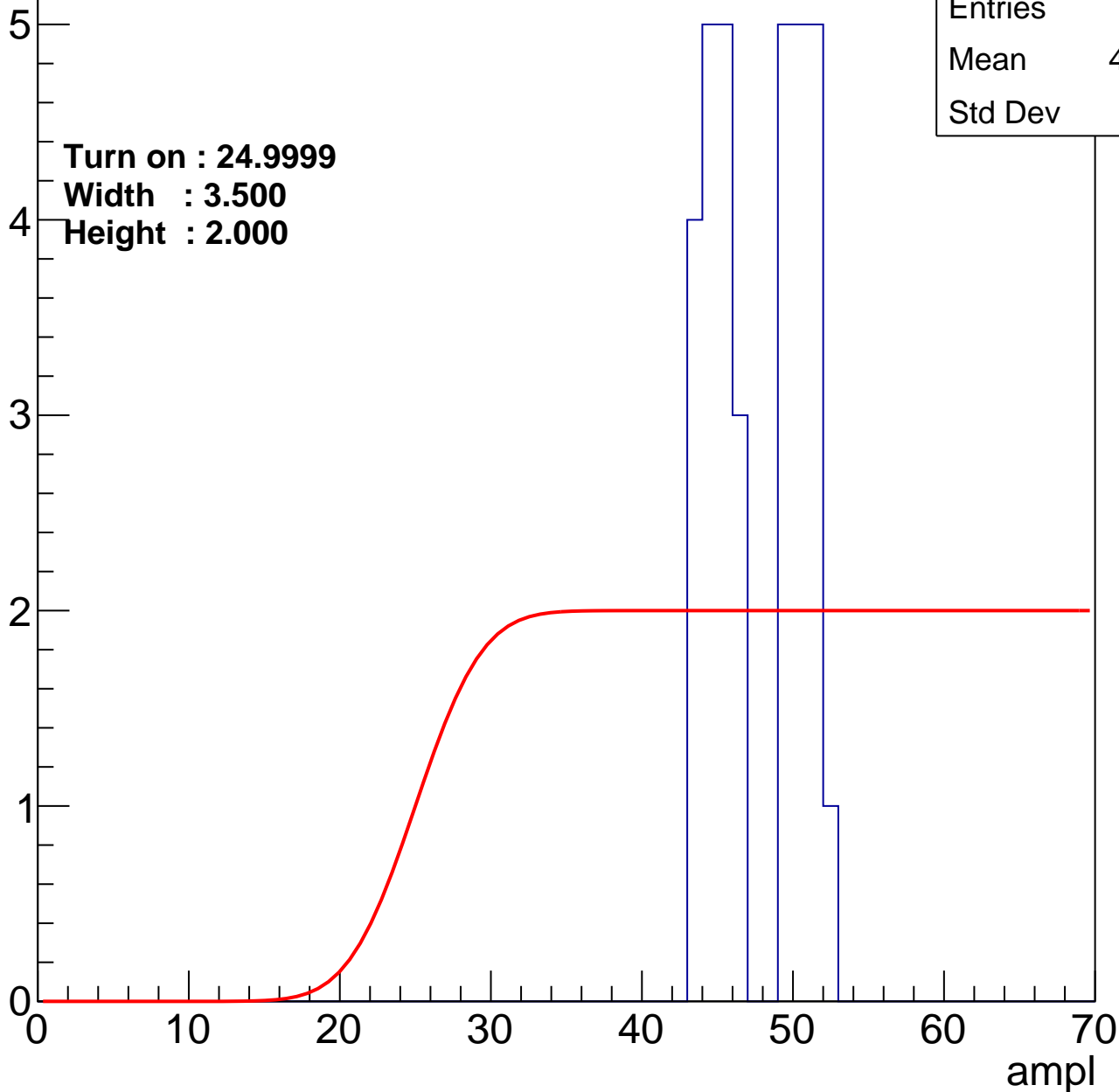
Entry

Entries	33
Mean	47.18
Std Dev	3.02

Turn on : 24.9999

Width : 3.500

Height : 2.000



# B0L100S, U3-ch91

calib\_packv5\_042523\_0143.root, FC#6, port A1

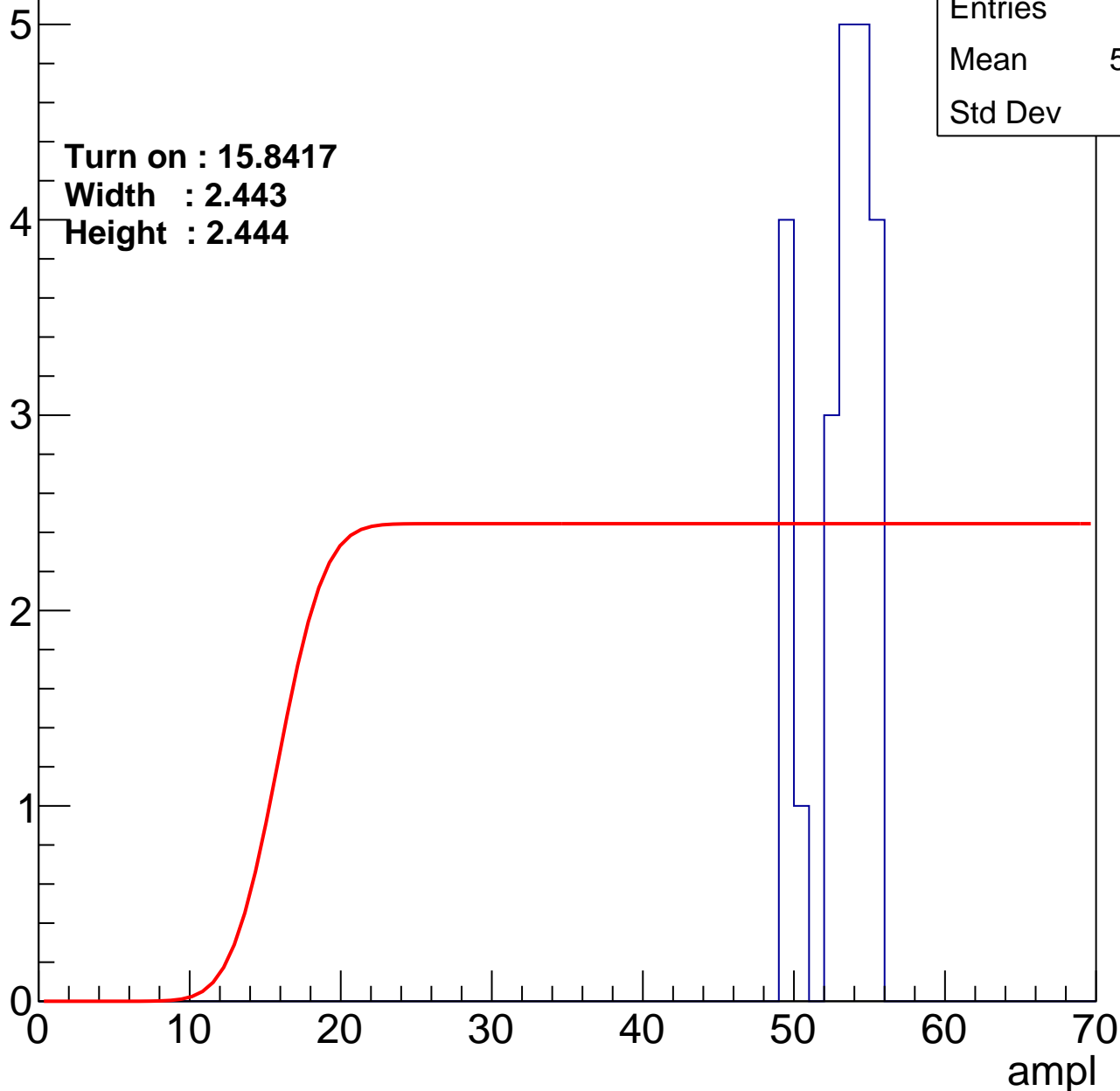
Entry

Entries	22
Mean	52.59
Std Dev	2.06

Turn on : 15.8417

Width : 2.443

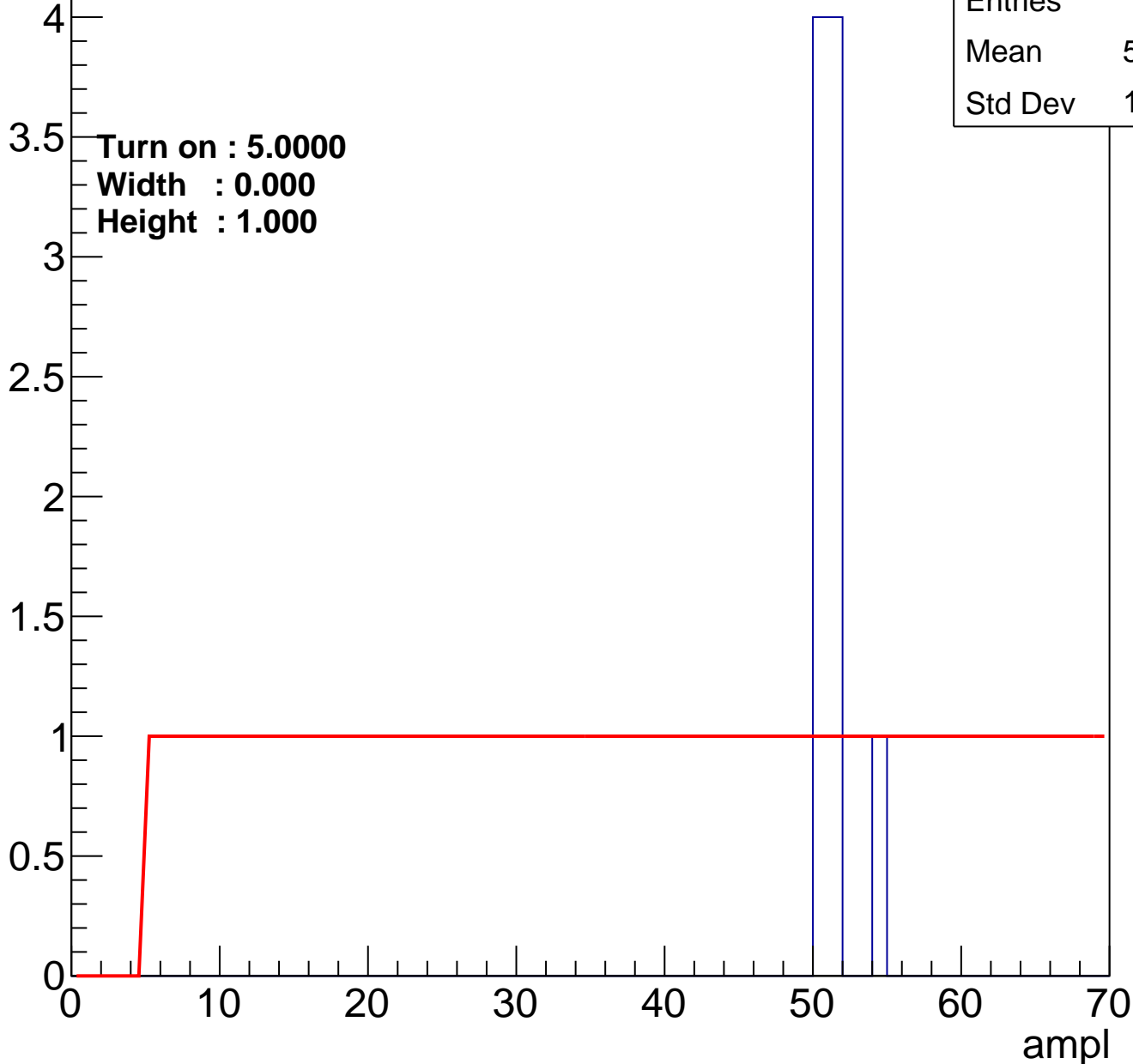
Height : 2.444



# B0L100S, U3-ch92

calib\_packv5\_042523\_0143.root, FC#6, port A1

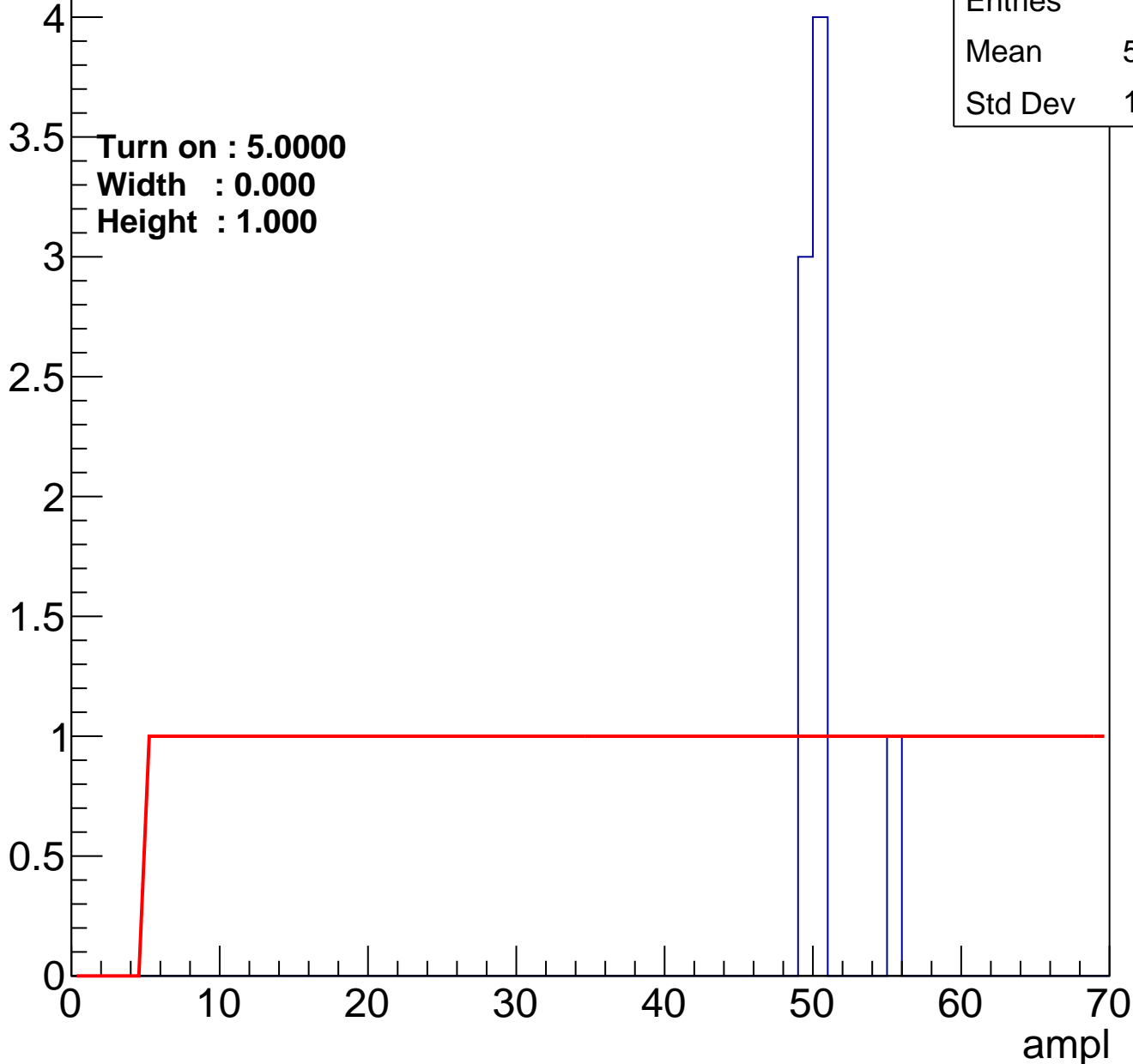
Entry



# B0L100S, U3-ch93

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	8
Mean	50.25
Std Dev	1.854

# B0L100S, U3-ch94

calib\_packv5\_042523\_0143.root, FC#6, port A1

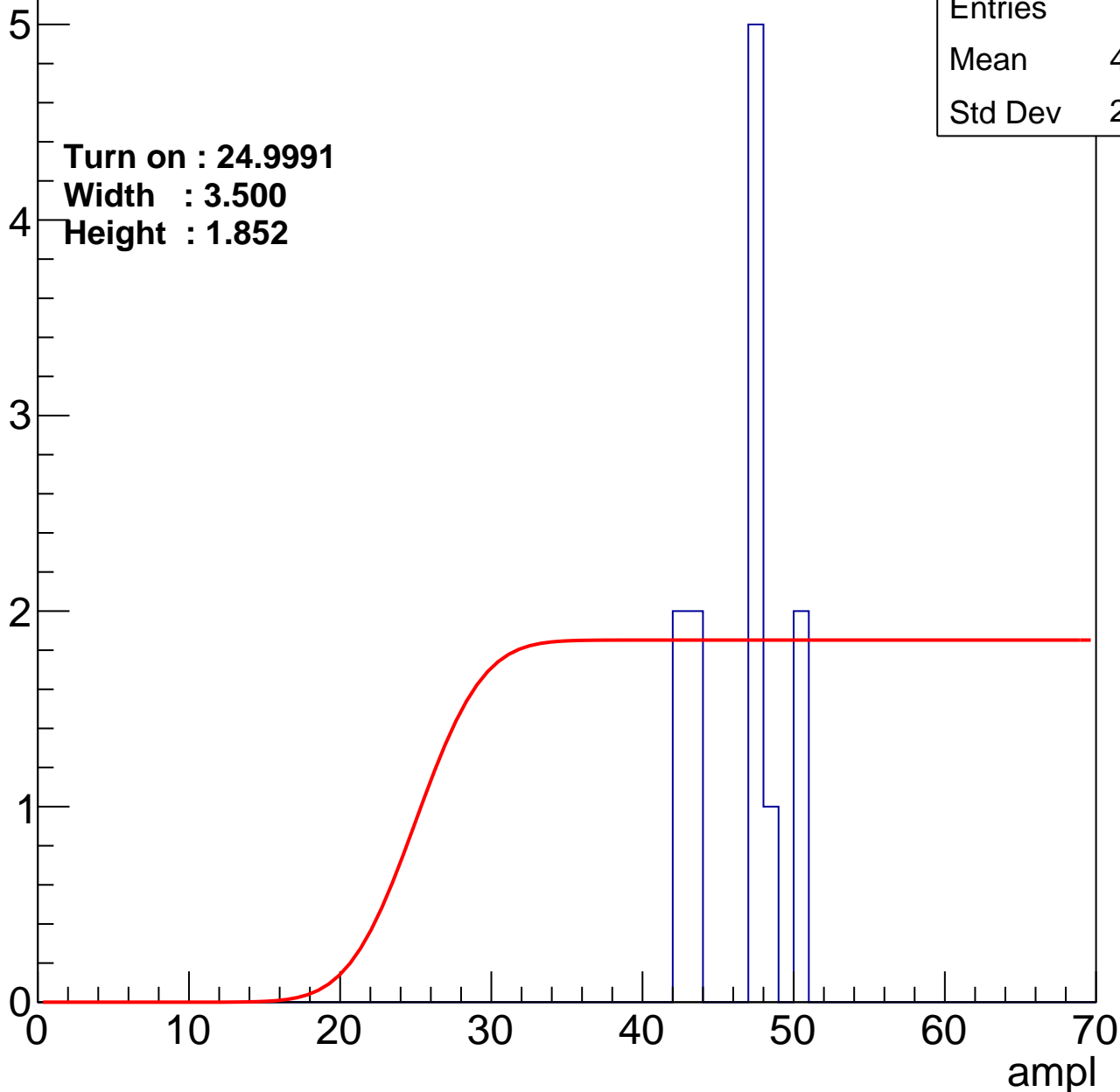
Entry

Entries	12
Mean	46.08
Std Dev	2.753

Turn on : 24.9991

Width : 3.500

Height : 1.852

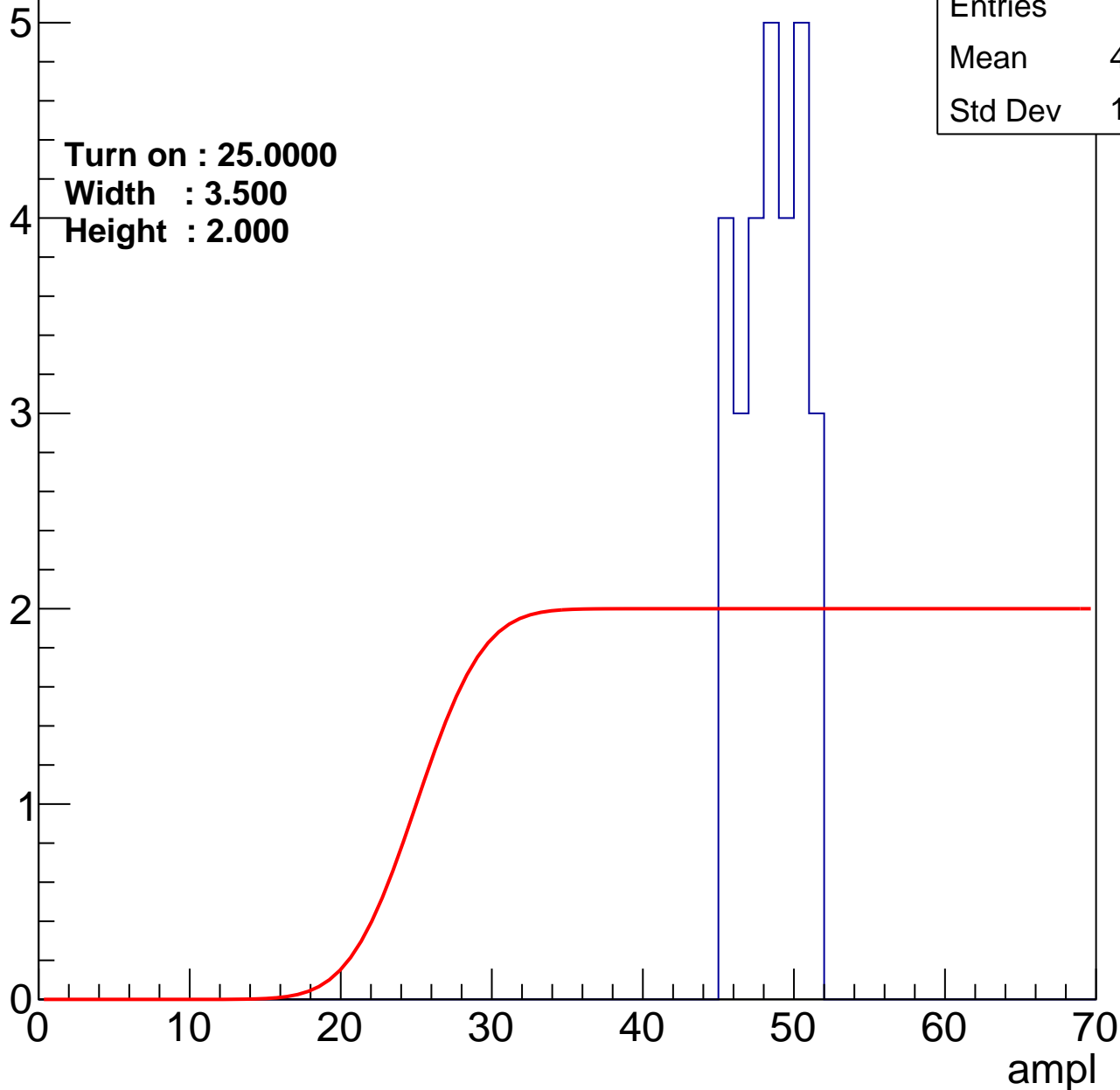




# B0L100S, U3-ch95

calib\_packv5\_042523\_0143.root, FC#6, port A1

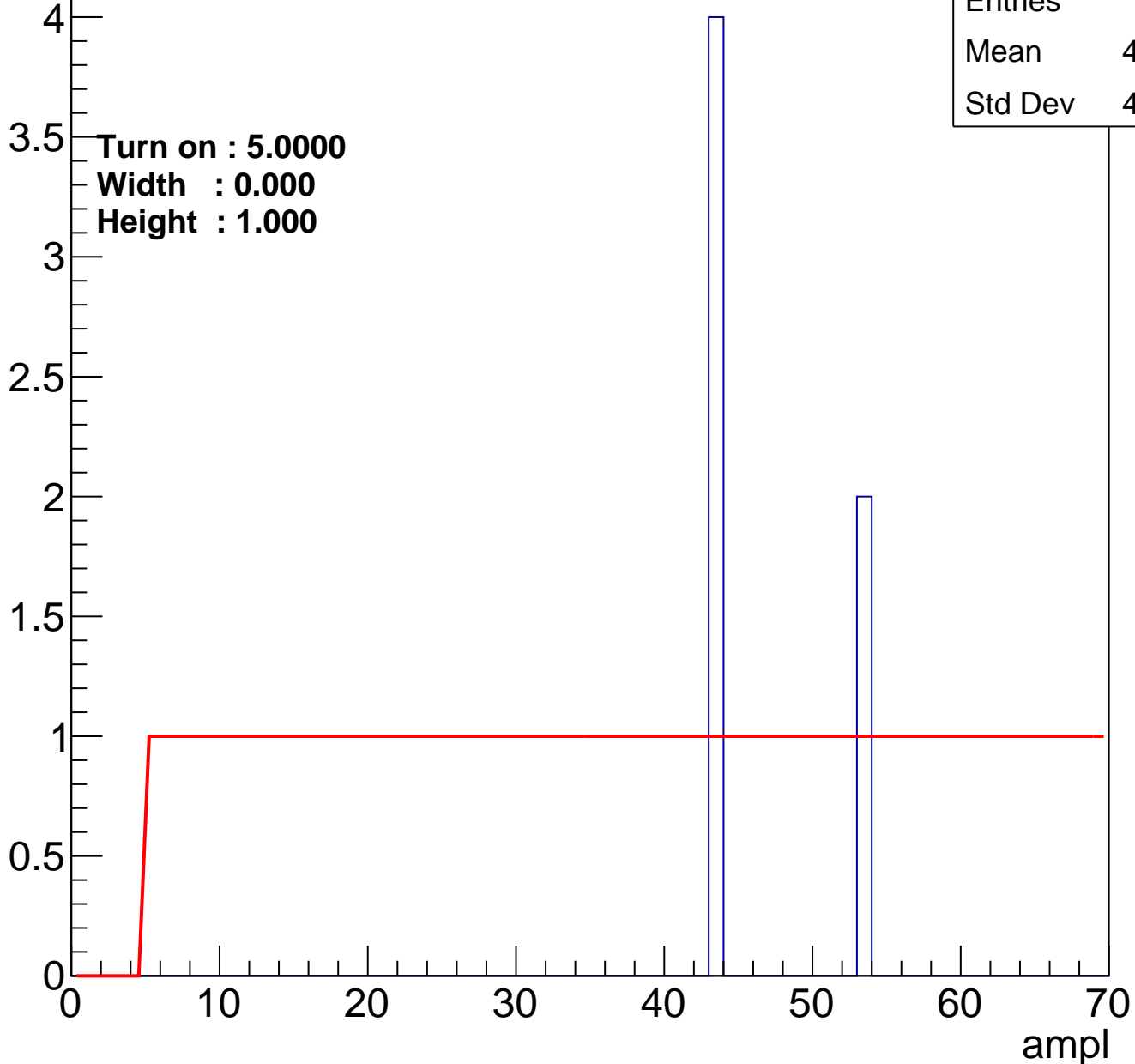
Entry



# B0L100S, U3-ch96

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Turn on : 5.0000

Width : 0.000

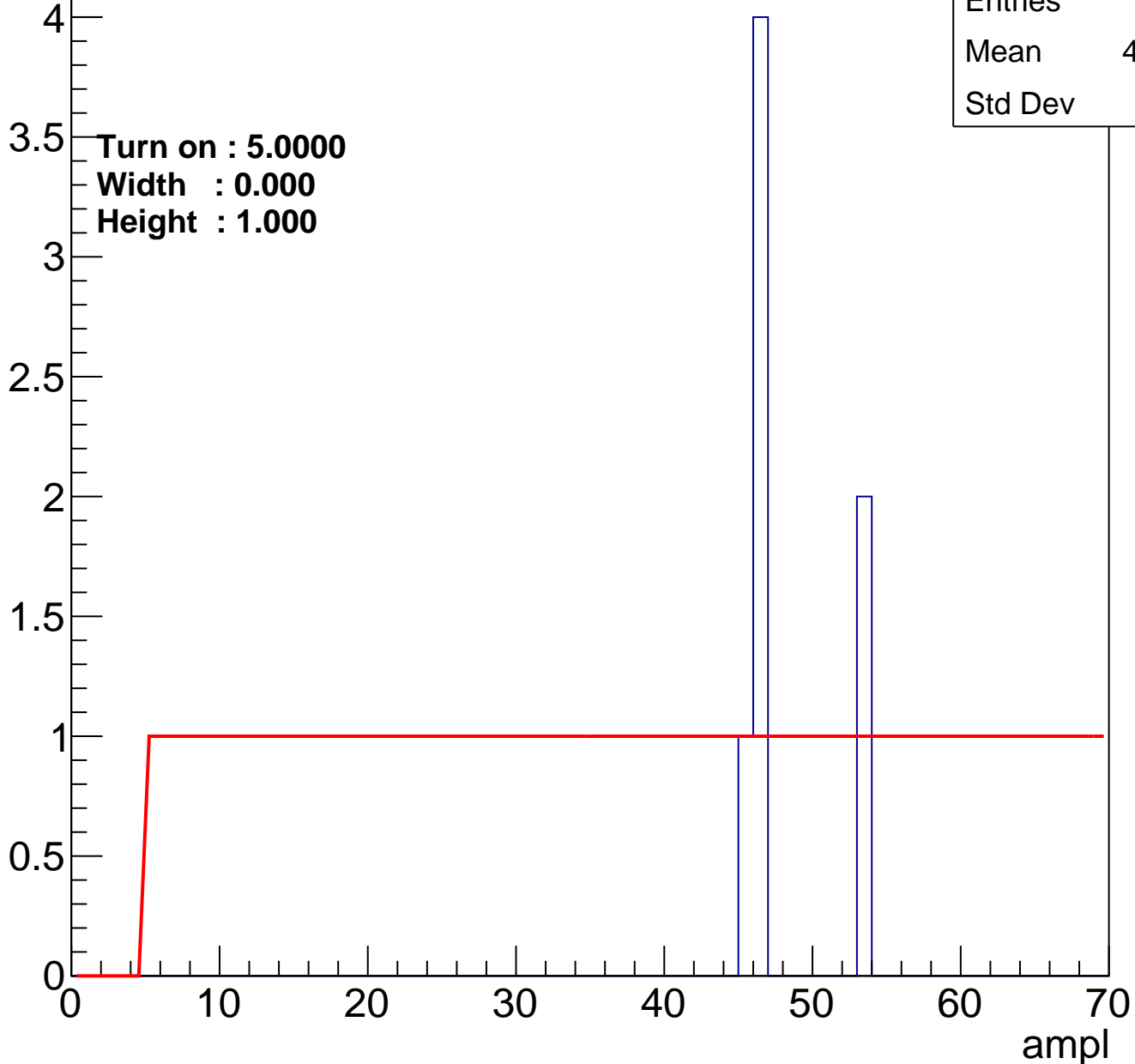
Height : 1.000

Entries	6
Mean	46.33
Std Dev	4.714

# B0L100S, U3-ch97

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	7
Mean	47.86
Std Dev	3.27

Turn on : 5.0000  
Width : 0.000  
Height : 1.000

# B0L100S, U3-ch98

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

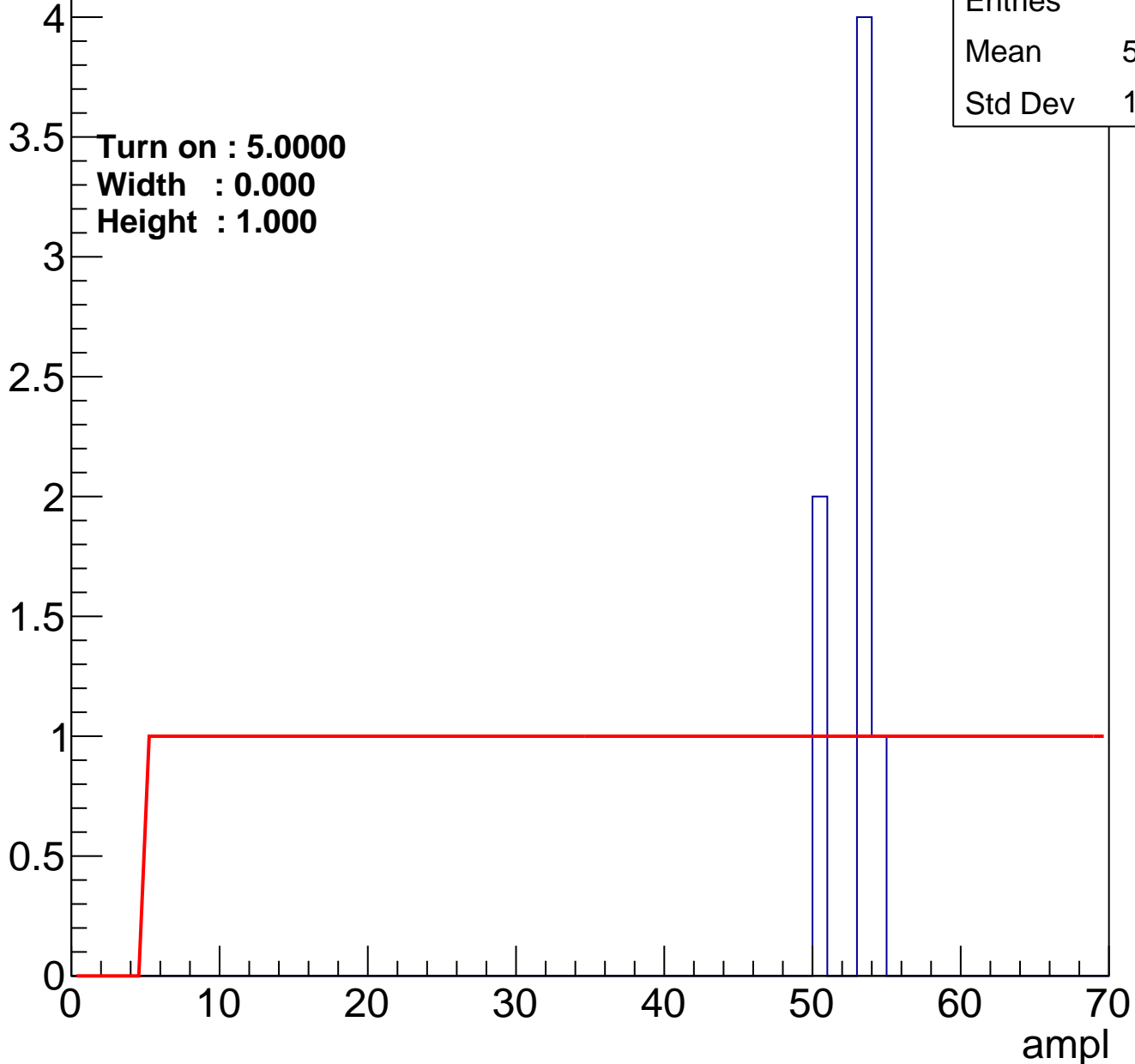


Entries	0
Mean	0
Std Dev	0

# B0L100S, U3-ch99

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

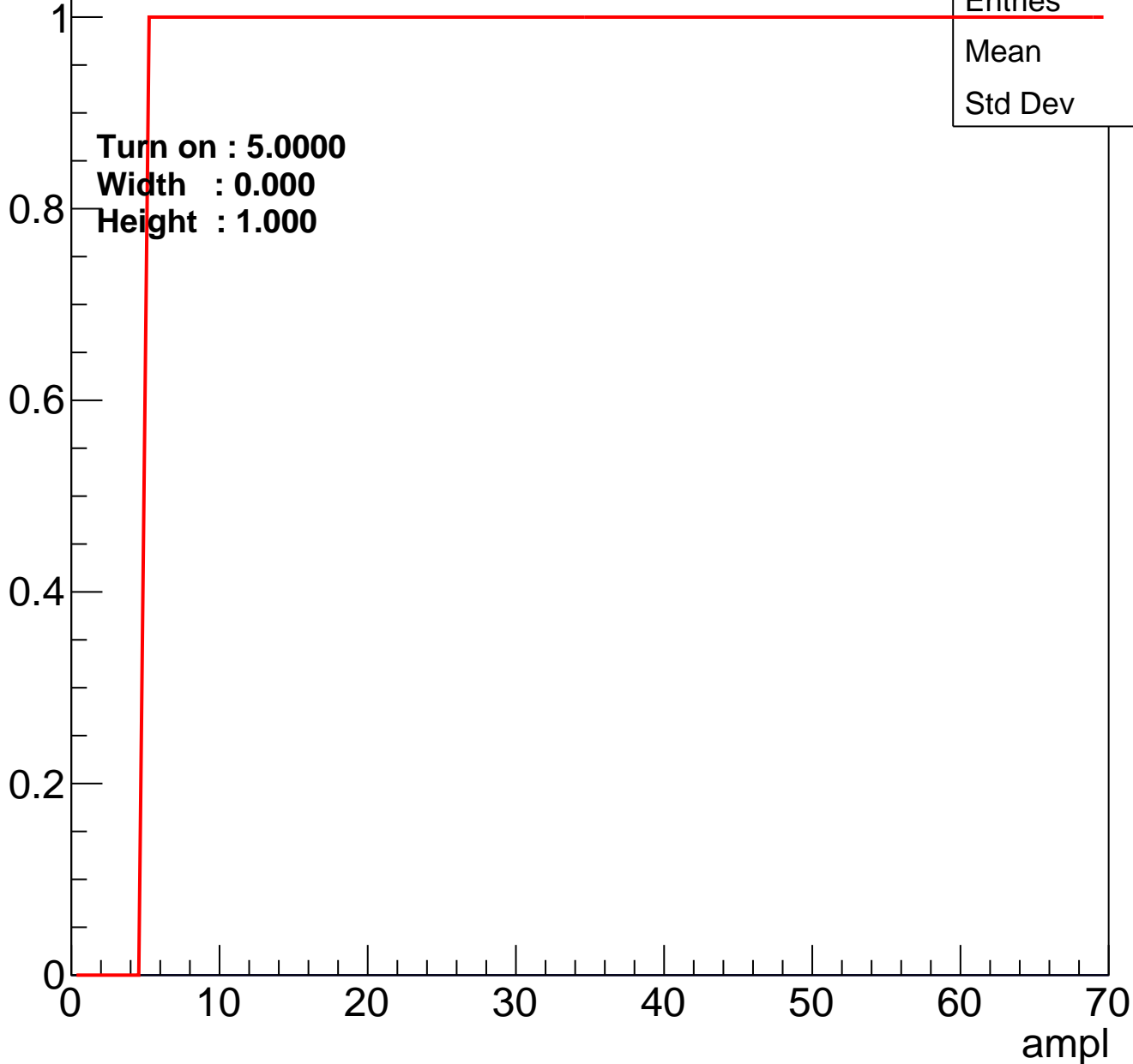


Entries	7
Mean	52.29
Std Dev	1.485

# B0L100S, U3-ch100

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

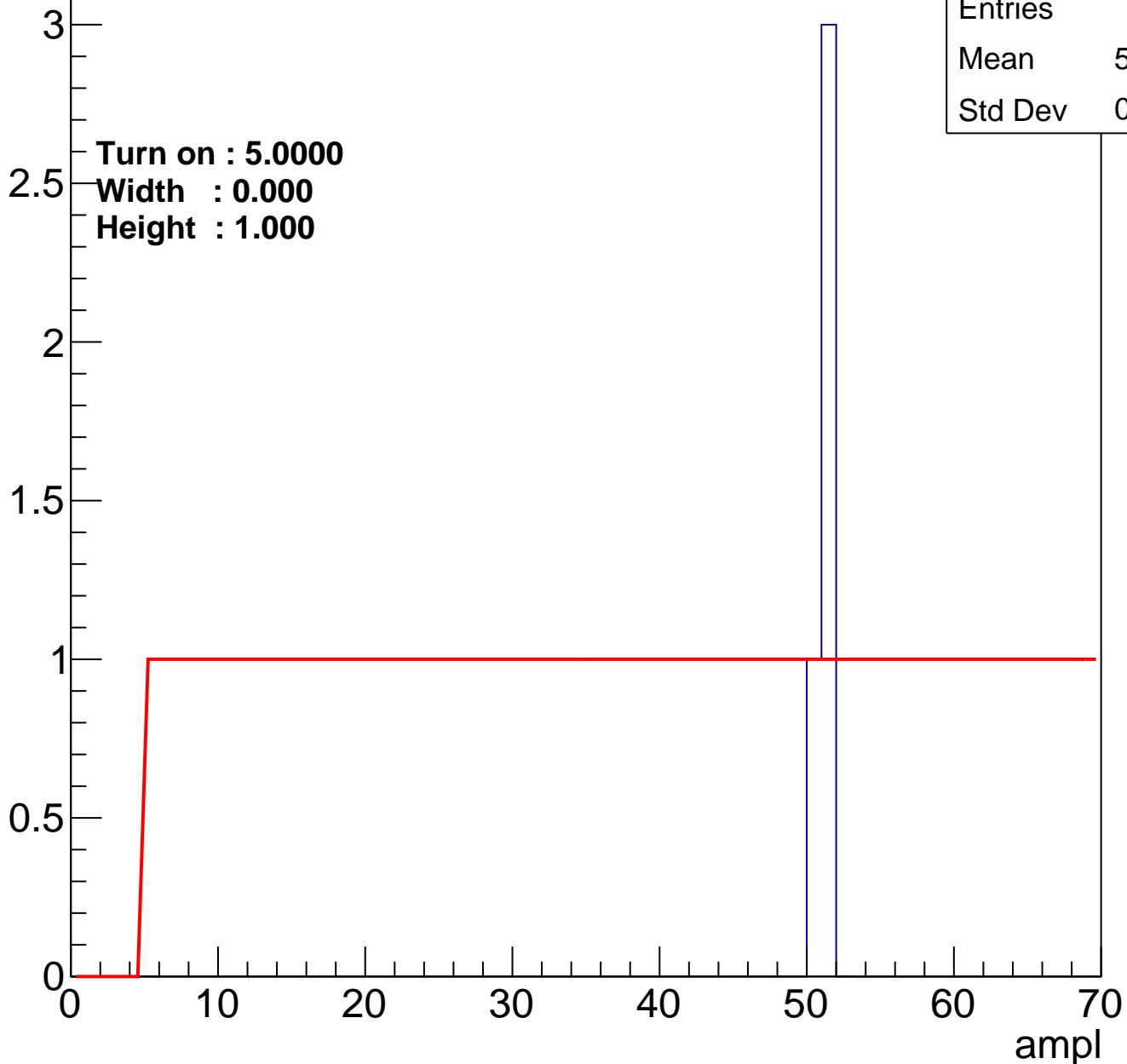


Entries	0
Mean	0
Std Dev	0

# B0L100S, U3-ch101

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U3-ch102

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L100S, U3-ch103

calib\_packv5\_042523\_0143.root, FC#6, port A1

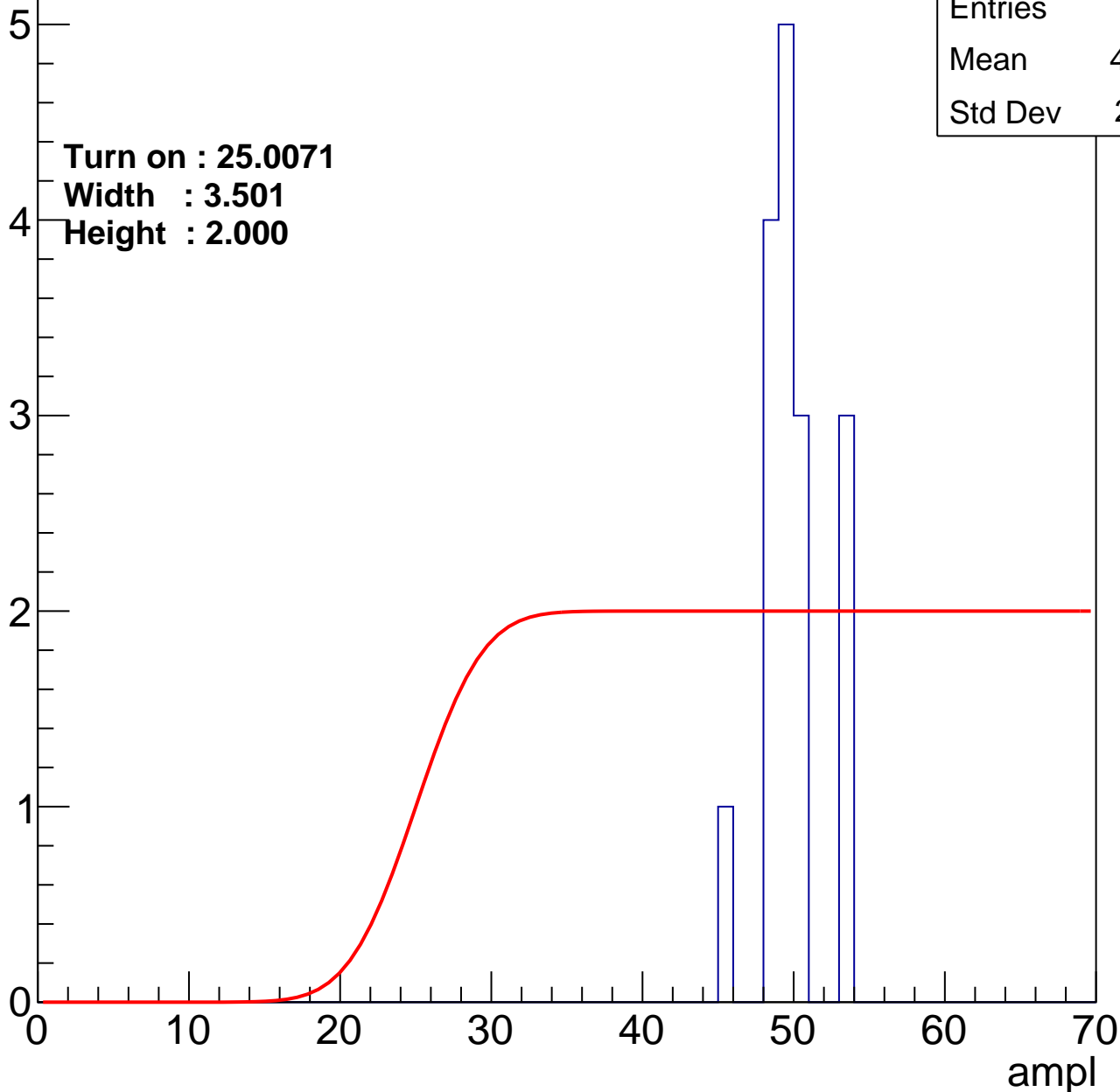
Entry

Entries	16
Mean	49.44
Std Dev	2.061

Turn on : 25.0071

Width : 3.501

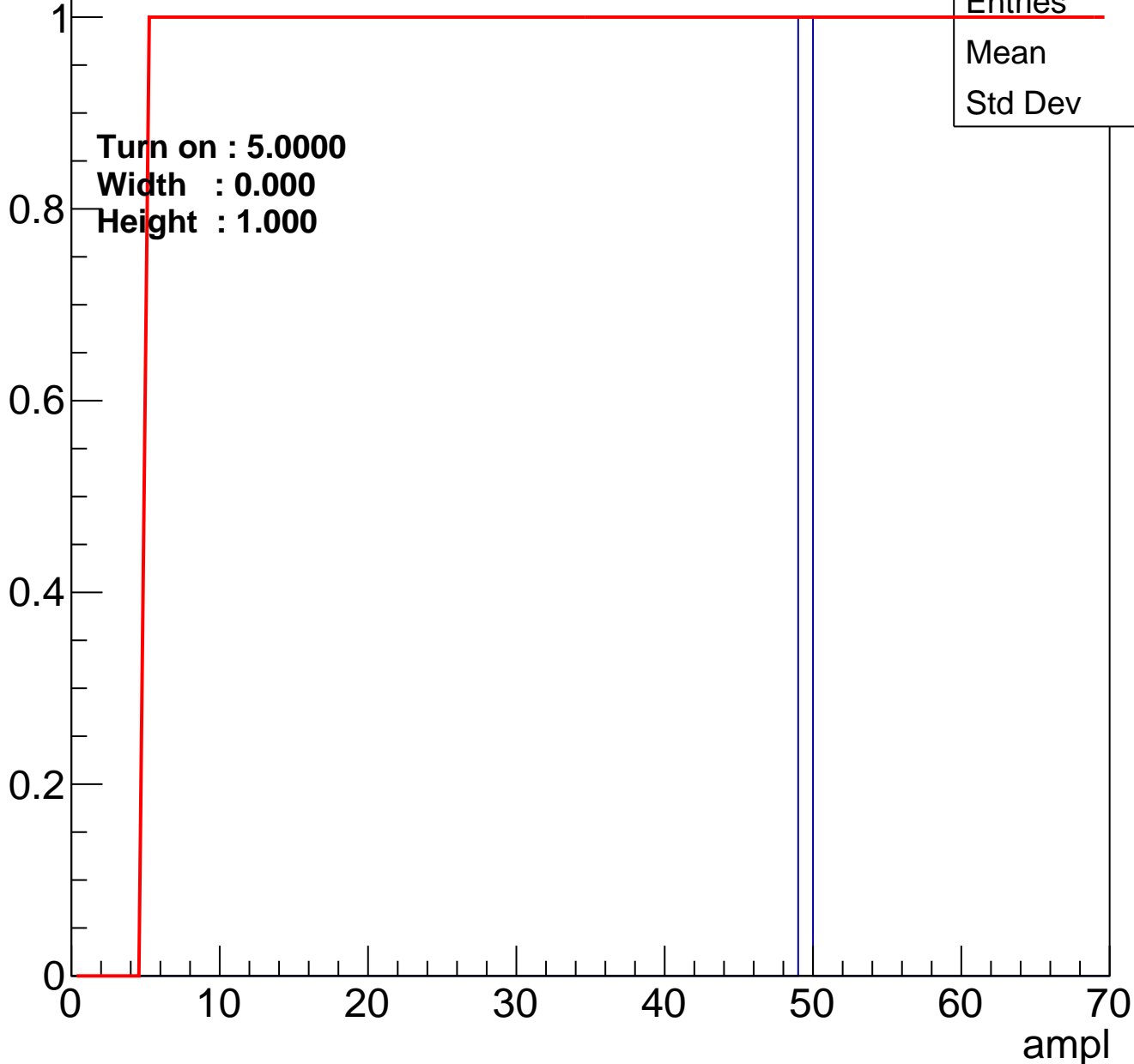
Height : 2.000



# B0L100S, U3-ch104

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U3-ch105

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U3-ch106

calib\_packv5\_042523\_0143.root, FC#6, port A1

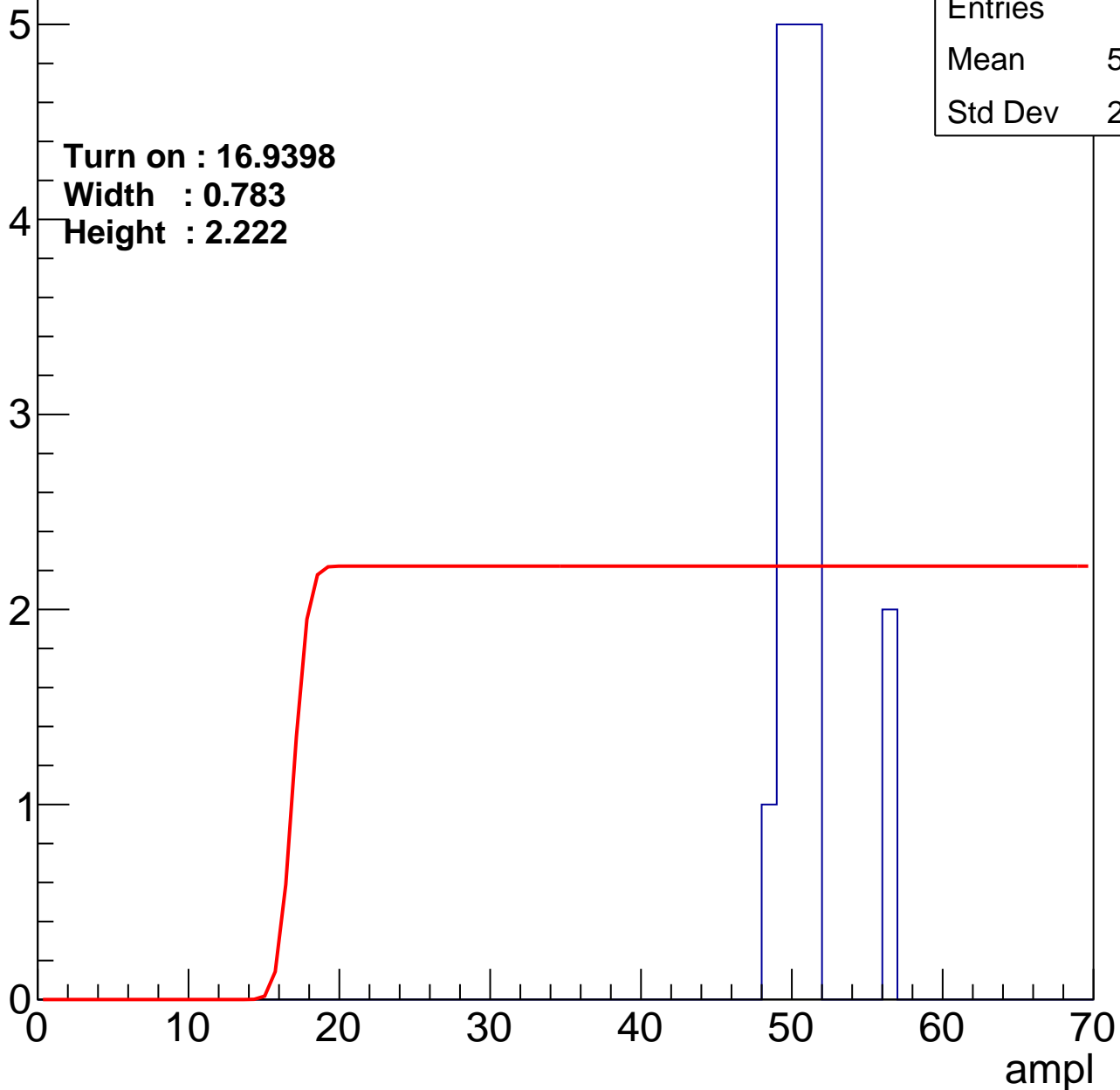
Entry

Entries	18
Mean	50.56
Std Dev	2.114

Turn on : 16.9398

Width : 0.783

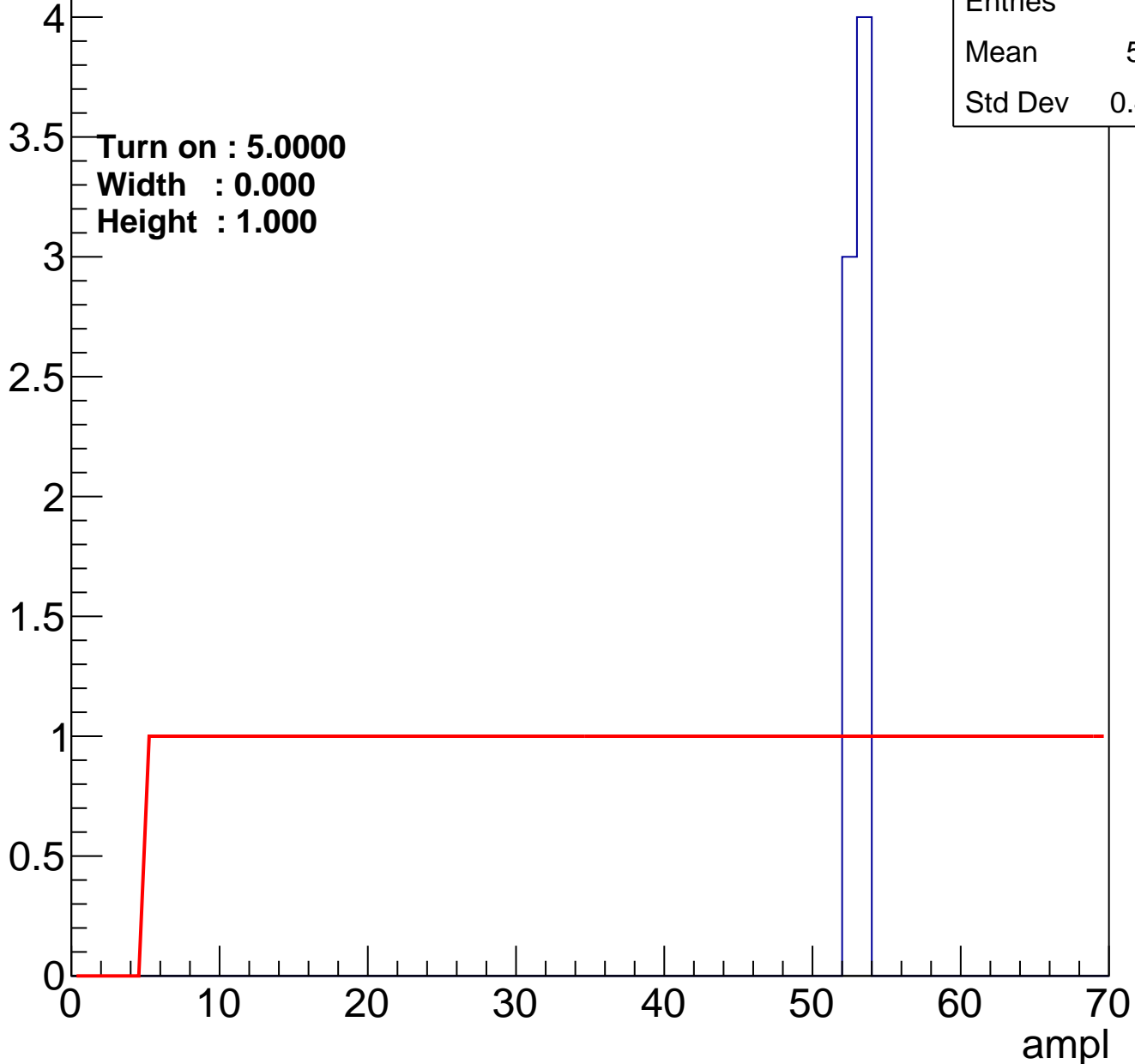
Height : 2.222



# B0L100S, U3-ch107

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U3-ch108

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U3-ch109

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U3-ch110

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry





# B0L100S, U3-ch111

calib\_packv5\_042523\_0143.root, FC#6, port A1

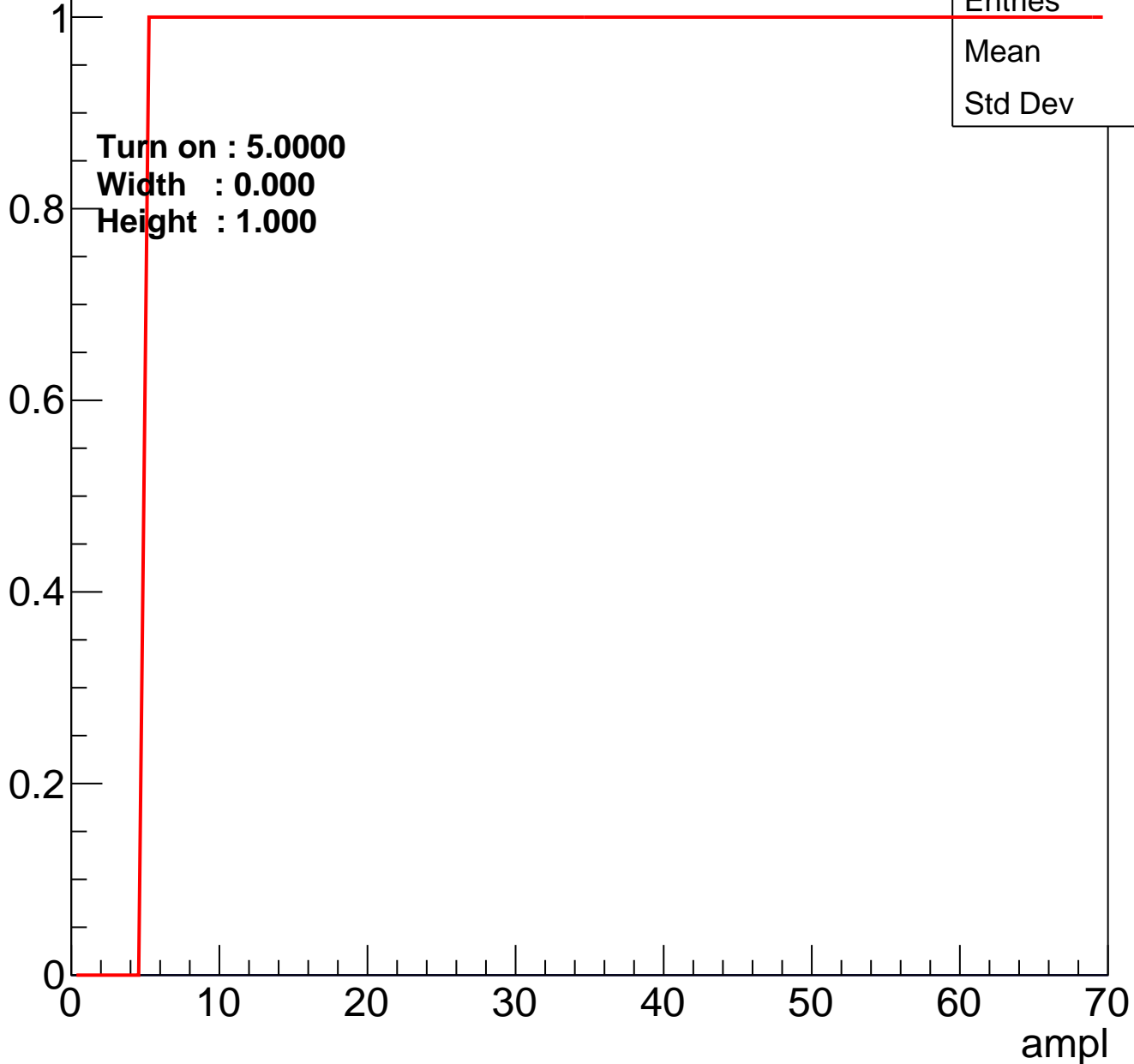
Entry



# B0L100S, U3-ch112

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U3-ch113

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U3-ch114

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L100S, U3-ch115

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

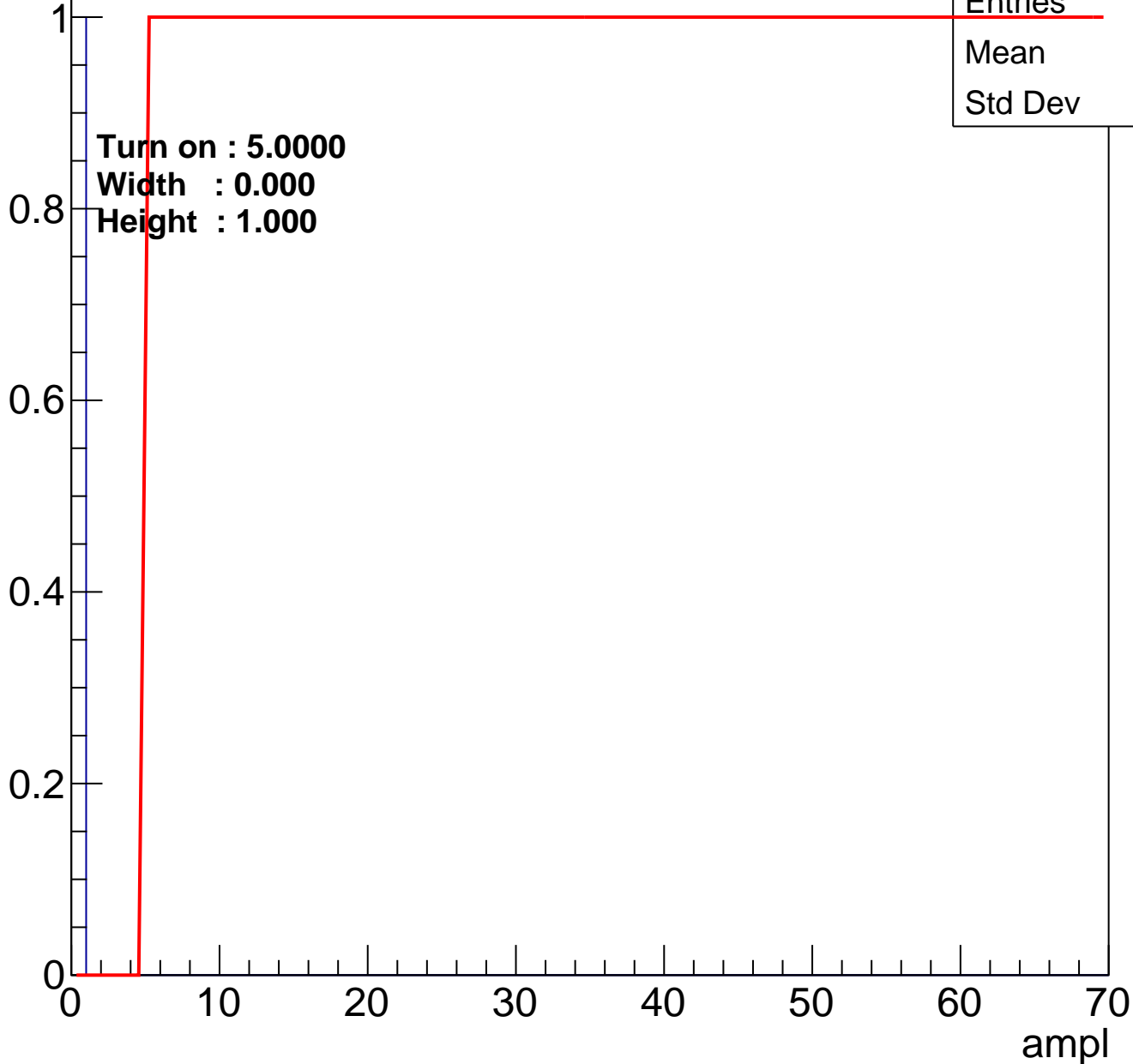


Entries	0
Mean	0
Std Dev	0

# B0L100S, U3-ch116

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L100S, U3-ch117

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L100S, U3-ch118

calib\_packv5\_042523\_0143.root, FC#6, port A1

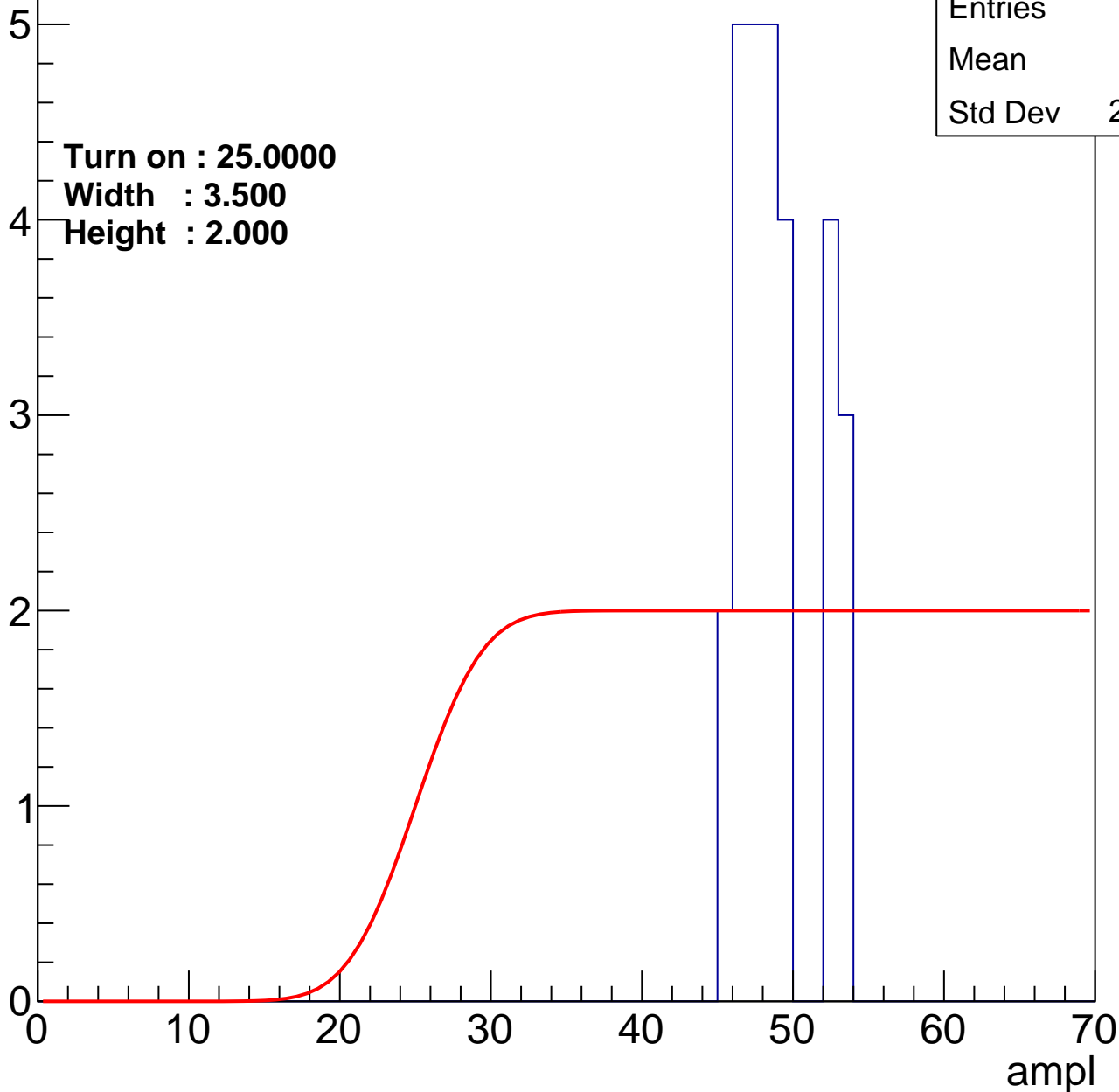
Entry

Entries	28
Mean	48.5
Std Dev	2.528

Turn on : 25.0000

Width : 3.500

Height : 2.000





# B0L100S, U3-ch119

calib\_packv5\_042523\_0143.root, FC#6, port A1

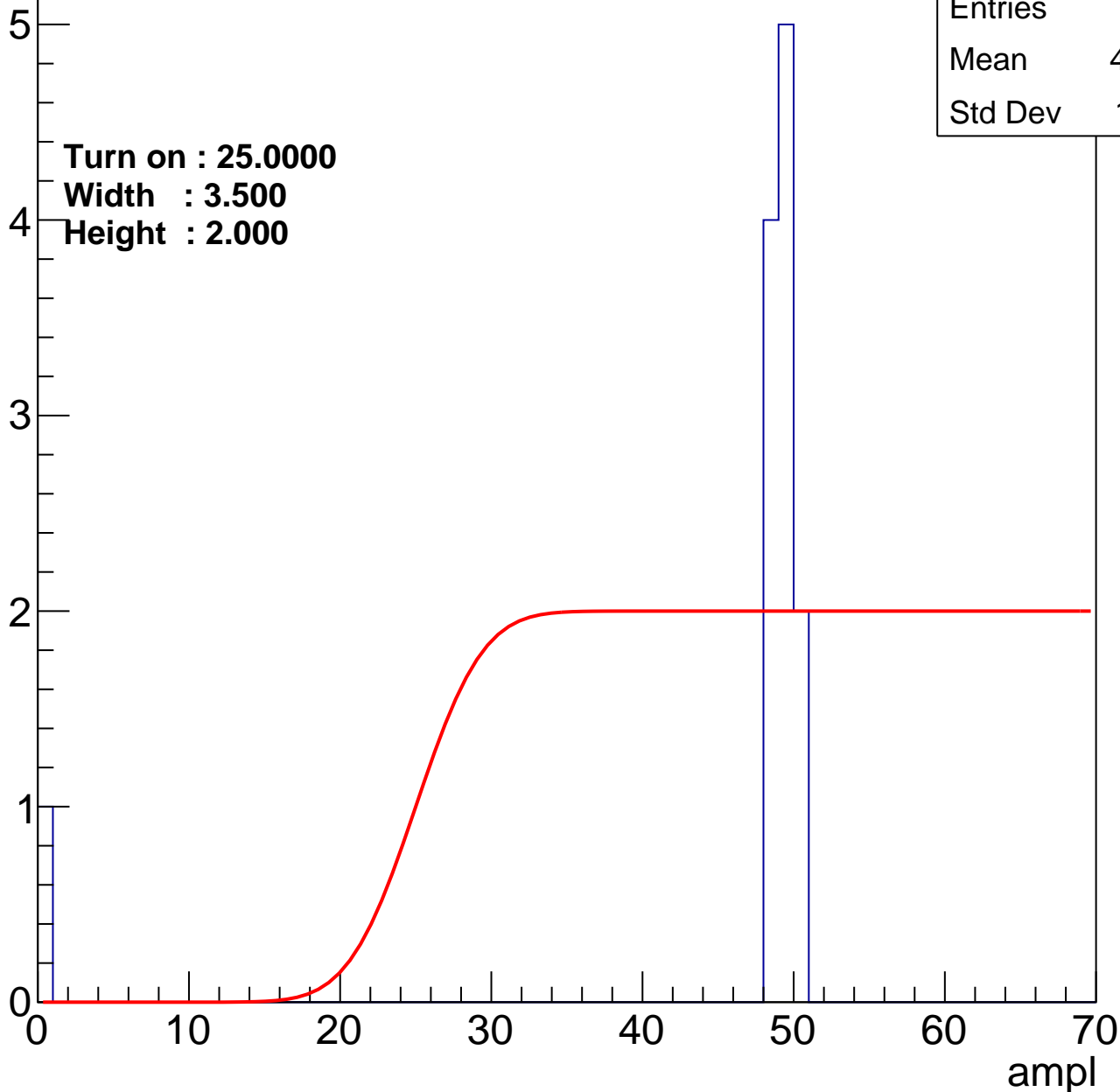
Entry

Entries	12
Mean	44.75
Std Dev	13.51

Turn on : 25.0000

Width : 3.500

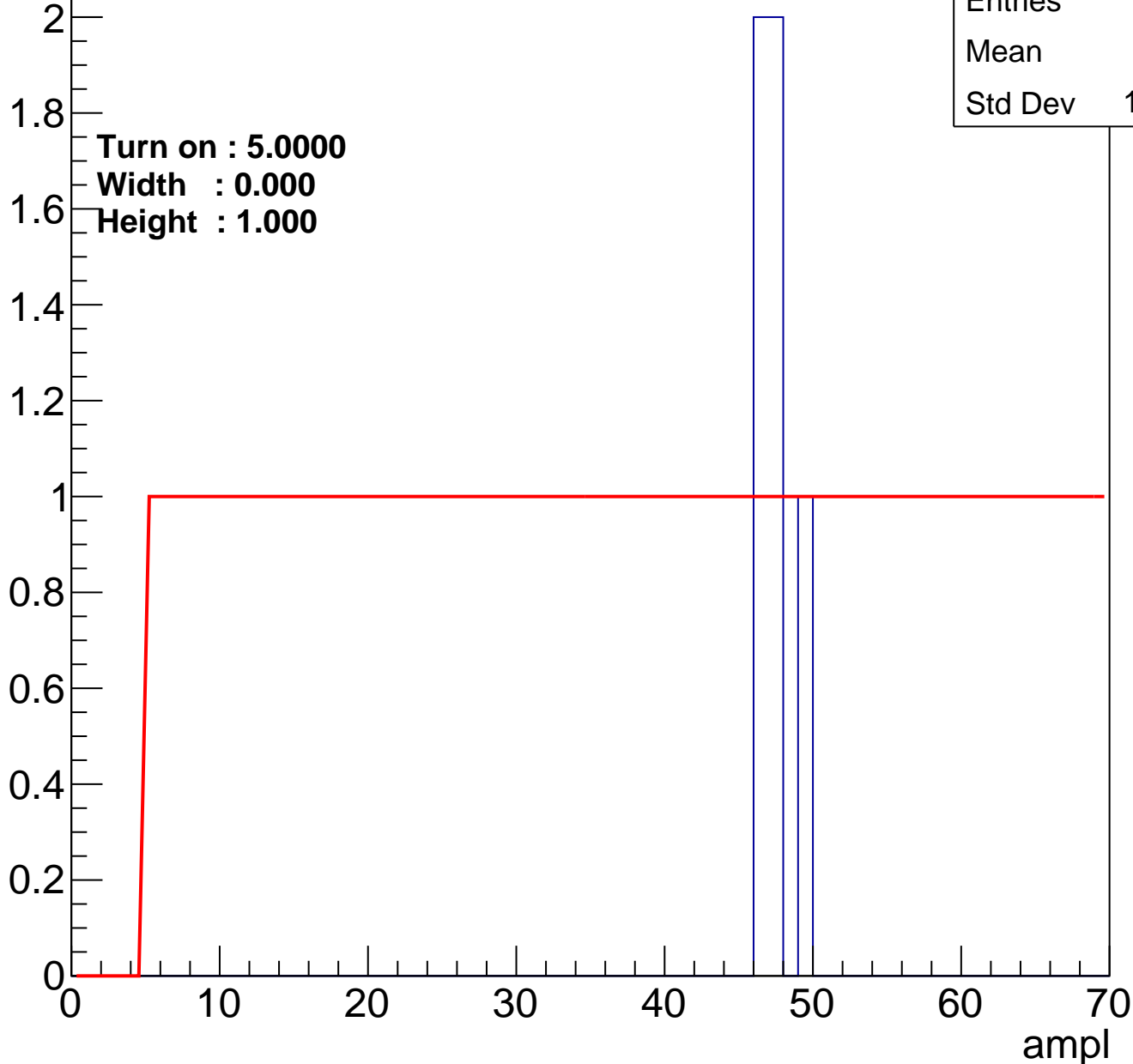
Height : 2.000



# B0L100S, U3-ch120

calib\_packv5\_042523\_0143.root, FC#6, port A1

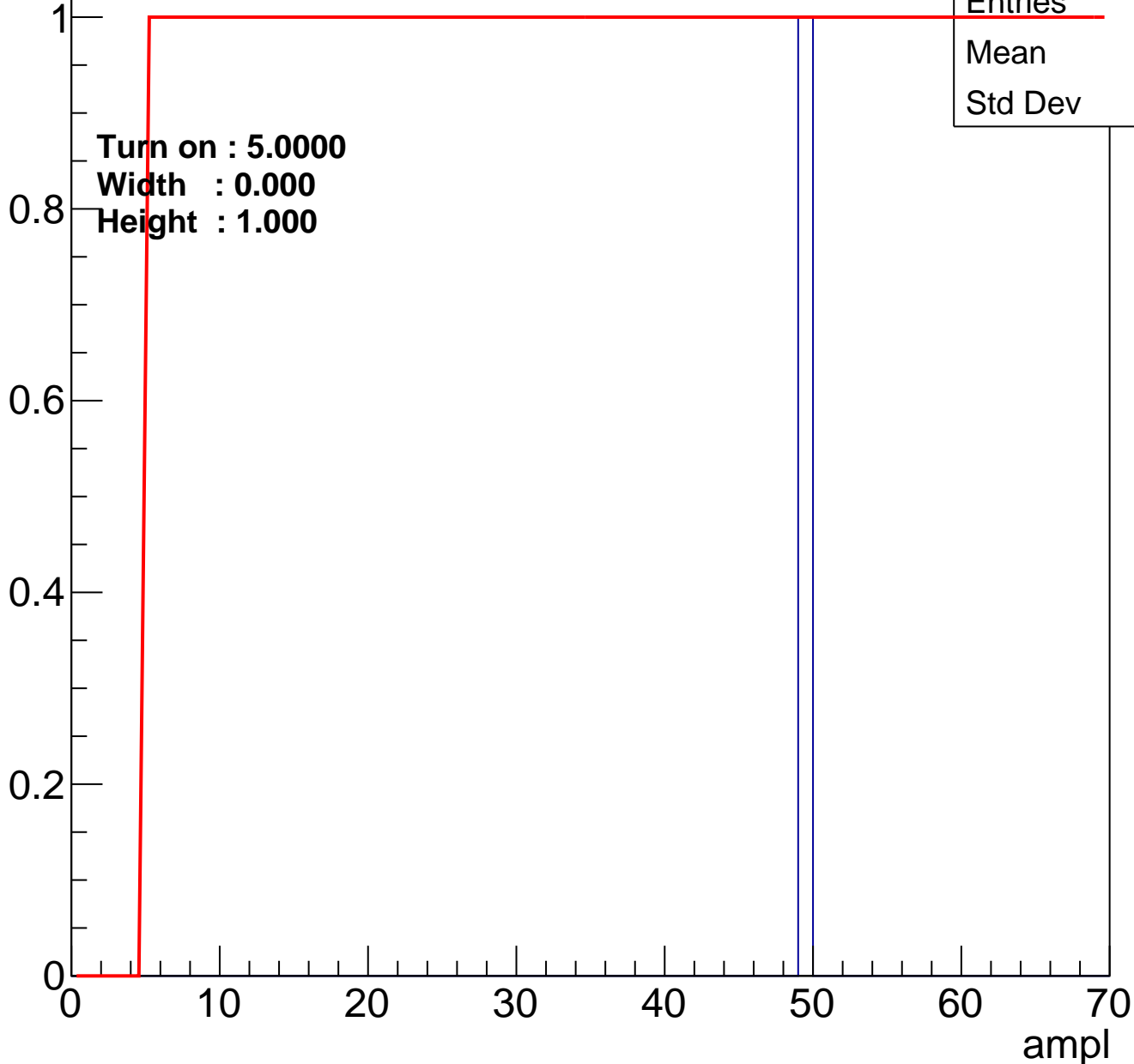
Entry



# B0L100S, U3-ch121

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	1
Mean	49
Std Dev	0

# B0L100S, U3-ch122

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

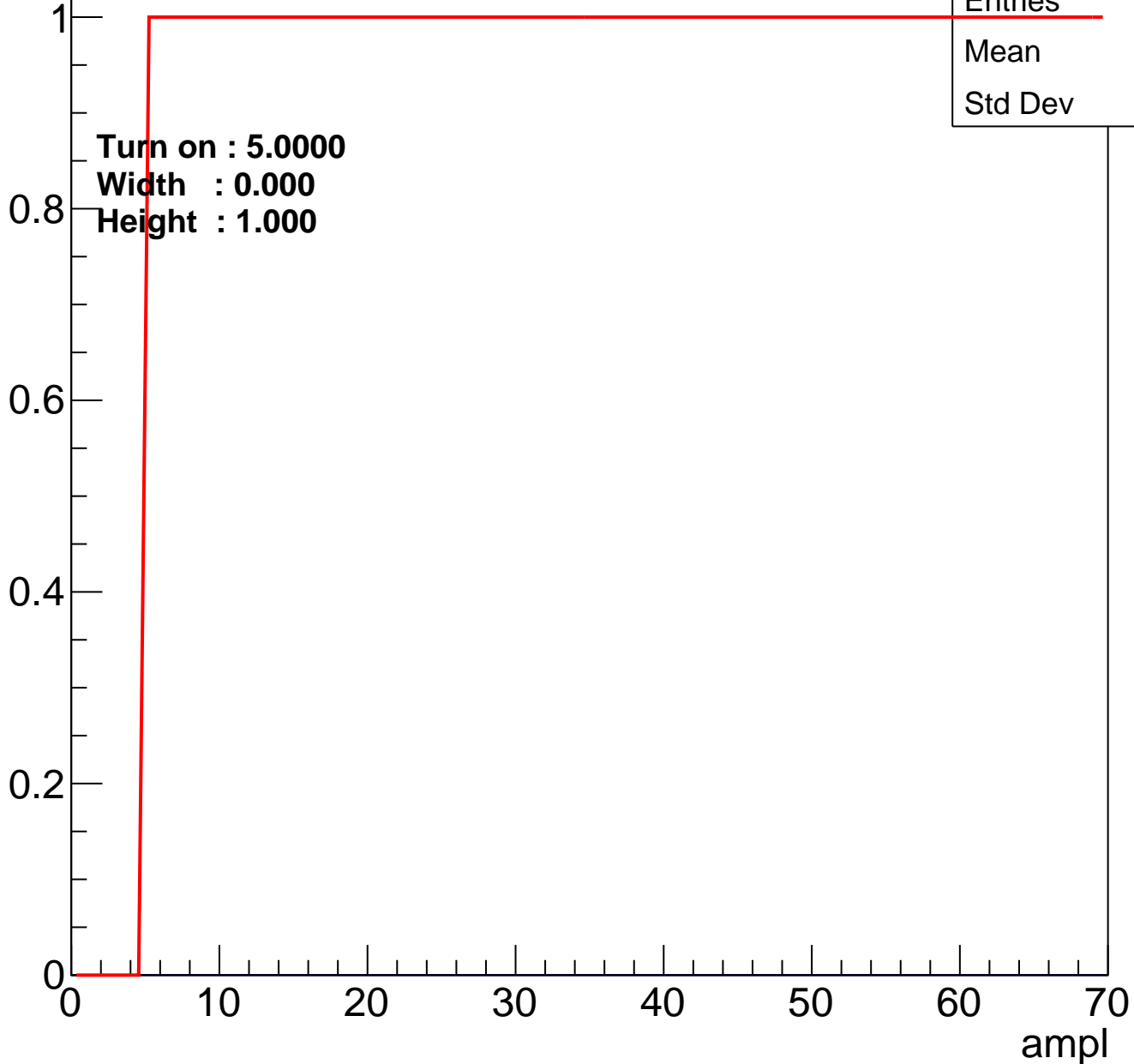


Entries	0
Mean	0
Std Dev	0

# B0L100S, U3-ch123

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U3-ch124

calib\_packv5\_042523\_0143.root, FC#6, port A1

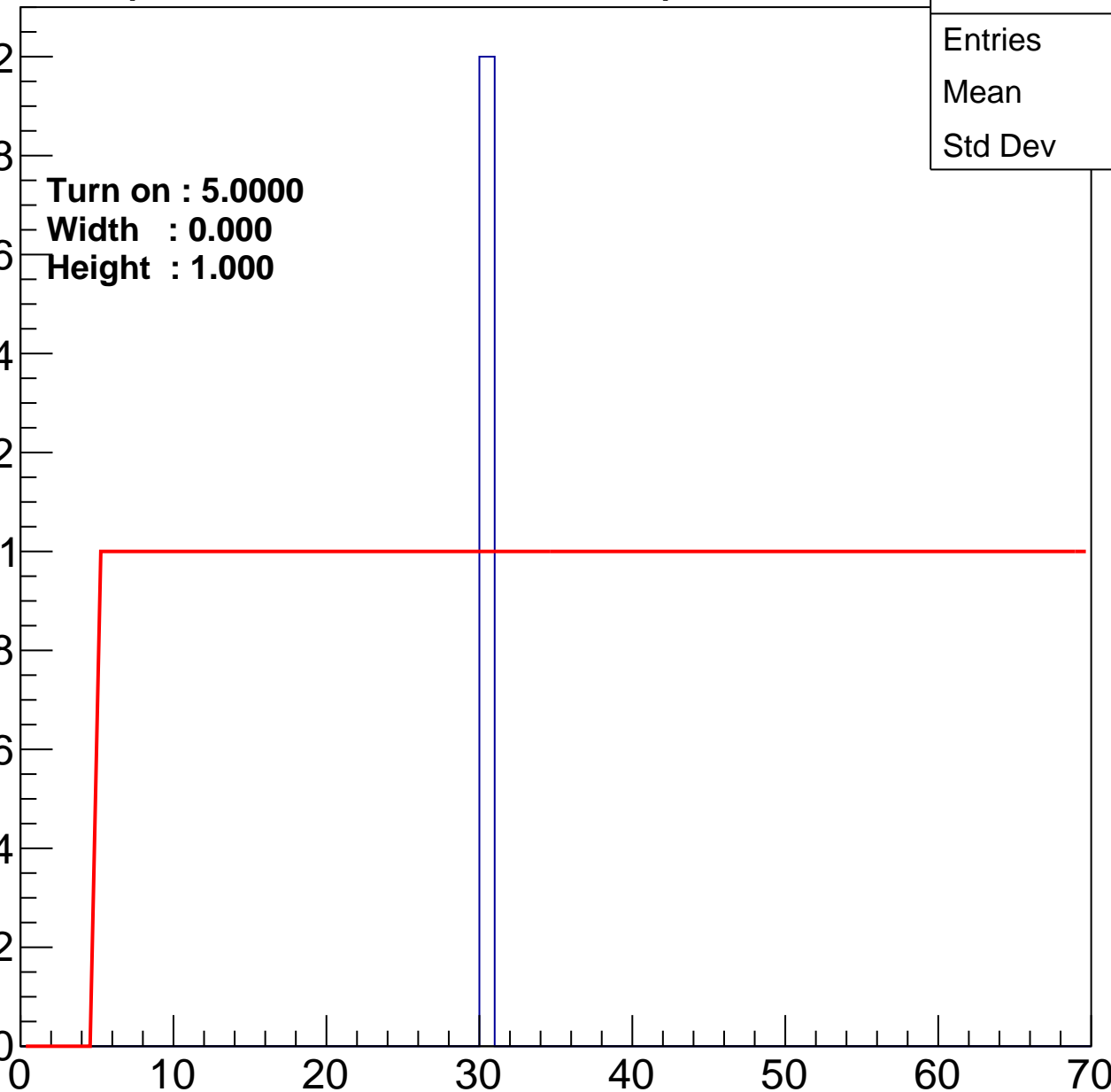
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Turn on : 5.0000  
Width : 0.000  
Height : 1.000

Entries	2
Mean	30
Std Dev	0

ampl



# B0L100S, U3-ch125

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U3-ch126

calib\_packv5\_042523\_0143.root, FC#6, port A1

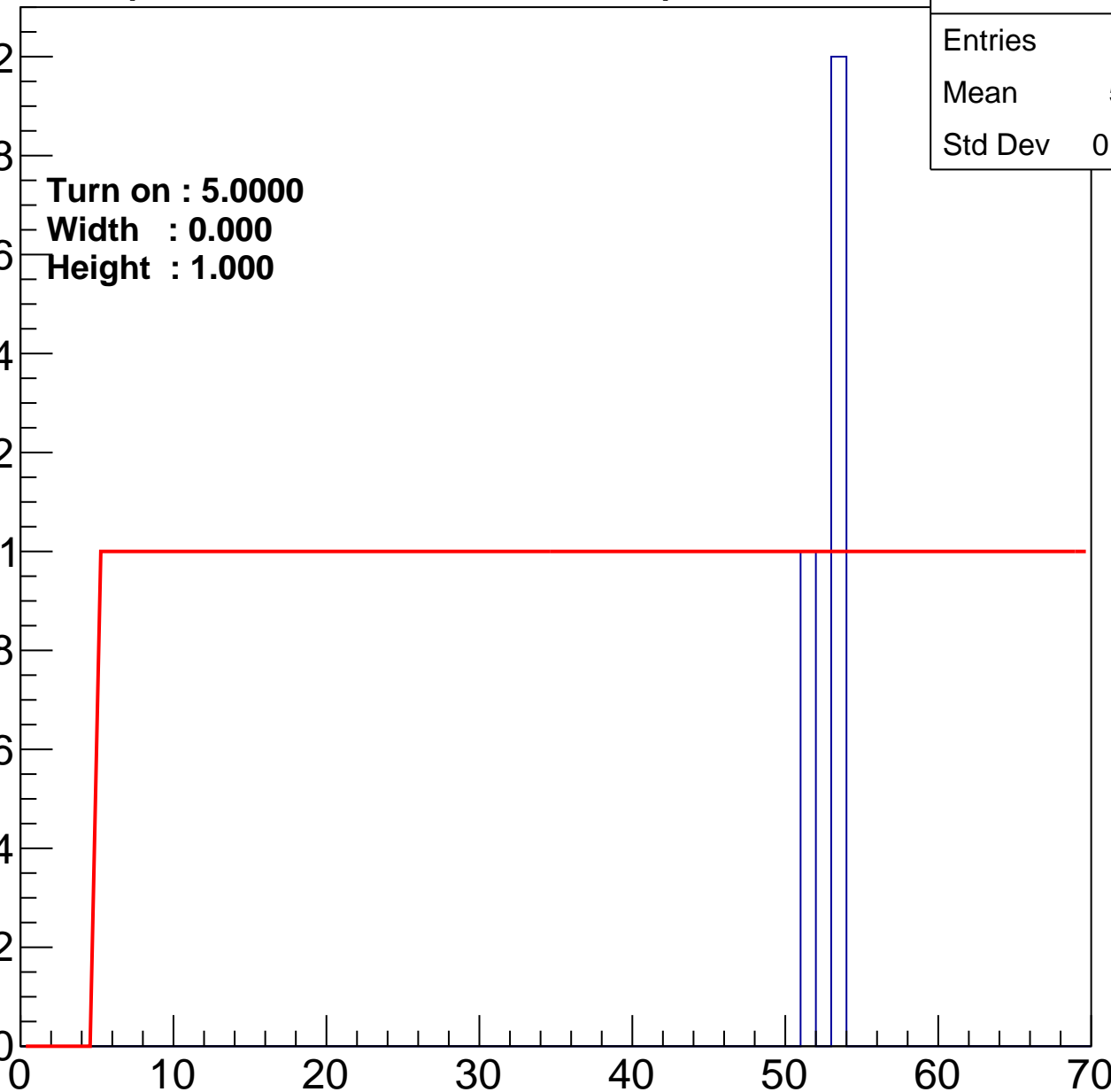
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Turn on : 5.0000  
Width : 0.000  
Height : 1.000

Entries	3
Mean	52.33
Std Dev	0.9428

ampl

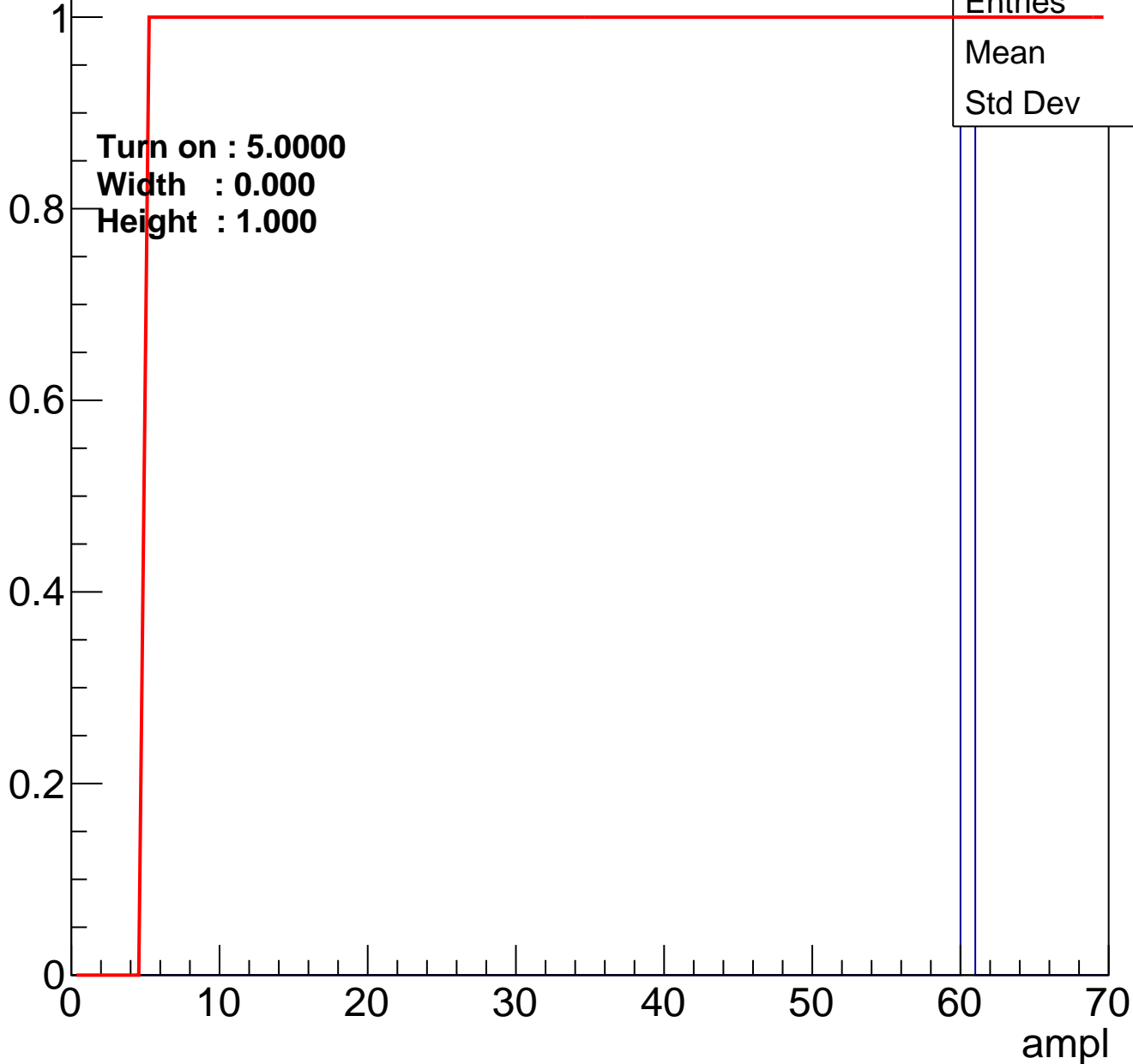




# B0L100S, U3-ch127

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	1
Mean	60
Std Dev	0

# B0L100S, U3-ch127

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

