B1L001S, U4-ch0, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch0, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch0, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch0, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entry

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch0, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch0, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch0, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch0, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch1, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch1, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch1, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch1, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch1, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch1, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch1, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entry

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch1, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch2, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch2, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch2, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch2, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch2, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch2, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch2, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch2, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch3, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	3
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch3, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch3, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch3, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch3, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch3, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch3, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch3, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entry

Entries	1
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch4, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch4, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch4, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch4, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch4, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch4, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch4, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch4, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch5, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch5, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch5, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch5, adc3

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch5, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch5, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch5, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch5, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

ampl

Entry

B1L001S, U4-ch6, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch6, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch6, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch6, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch6, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch6, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch6, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch6, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch7, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	3
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch7, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch7, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch7, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch7, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch7, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch7, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch7, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch8, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch8, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch8, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch8, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch8, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch8, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch8, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch8, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entry

ampl

Entries	0
Mean	0
Std Dev	0

B1L001S, U4-ch9, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch9, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch9, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch9, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch9, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch9, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch9, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch9, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch10, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch10, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch10, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch10, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch10, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch10, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch10, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch10, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch11, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	3
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch11, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch11, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch11, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch11, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch11, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch11, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch11, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entry

Entries	1
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch12, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	4
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch12, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch12, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch12, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch12, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch12, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch12, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch12, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entry

ampl

Entries	1
Mean	0
Std Dev	0

B1L001S, U4-ch13, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch13, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entry

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

ampl

B1L001S, U4-ch13, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch13, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch13, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch13, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch13, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

B1L001S, U4-ch13, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch14, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch14, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entry

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

ampl

B1L001S, U4-ch14, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch14, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entry

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch14, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch14, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch14, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch14, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch15, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch15, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch15, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entry

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

ampl

B1L001S, U4-ch15, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch15, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch15, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch15, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch15, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entry

ampl

Entries	1
Mean	0
Std Dev	0

B1L001S, U4-ch16, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	3
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch16, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch16, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch16, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch16, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch16, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch16, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch16, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch17, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch17, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch17, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch17, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch17, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

Entry

B1L001S, U4-ch17, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch17, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entry

ampl

Entries	0
Mean	0
Std Dev	0

B1L001S, U4-ch17, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

B1L001S, U4-ch18, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	3
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch18, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch18, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch18, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch18, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch18, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch18, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch18, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch19, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch19, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch19, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch19, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch19, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch19, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch19, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch20, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch20, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entry

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

ampl

B1L001S, U4-ch20, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch20, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch20, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch20, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch20, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch20, adc7

Entry

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch21, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch21, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch21, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch21, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch21, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch21, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch21, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch21, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	3
Mean	0
Std Dev	0

B1L001S, U4-ch22, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch22, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch22, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch22, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch22, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch22, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch22, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch22, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch23, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch23, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch23, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch23, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch23, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch23, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch23, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch23, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch24, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch24, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch24, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch24, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch24, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch24, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch24, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch24, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

B1L001S, U4-ch25, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entry

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

ampl

B1L001S, U4-ch25, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entry

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

ampl

B1L001S, U4-ch25, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch25, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

B1L001S, U4-ch25, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch25, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

B1L001S, U4-ch25, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch25, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch26, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	3
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch26, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch26, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch26, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch26, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entry

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch26, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch26, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch26, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch27, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch27, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch27, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch27, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entry

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch27, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch27, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch27, adc6

calib_packv5_042523_0143.root, FC#2, port C2

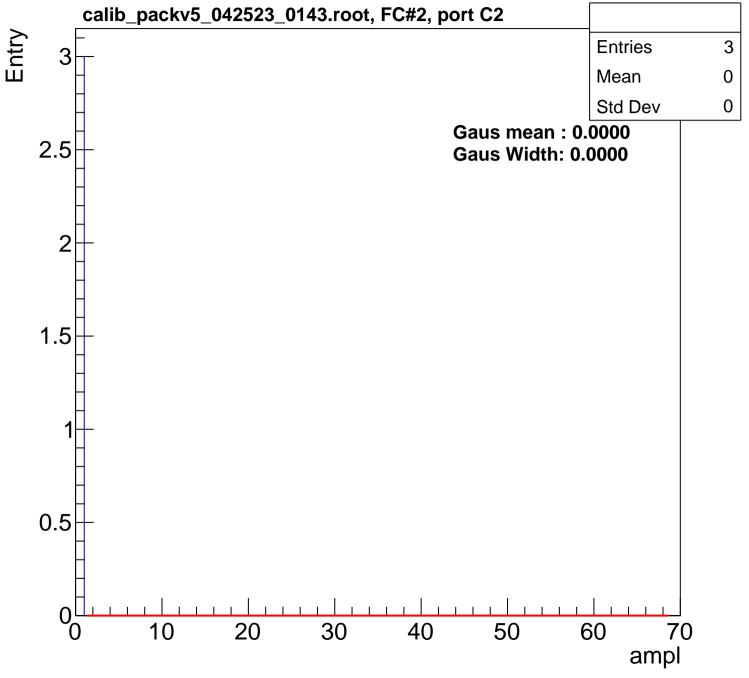|	
Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch27, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch28, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch28, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch28, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch28, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch28, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch28, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch28, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch28, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch29, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch29, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch29, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch29, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch29, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch29, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch29, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch29, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch30, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch30, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entry

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

ampl

B1L001S, U4-ch30, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch30, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch30, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch30, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch30, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch31, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch31, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch31, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch31, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch31, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch31, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch31, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch31, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entry

ampl

Entries	0
Mean	0
Std Dev	0

B1L001S, U4-ch32, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch32, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch32, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch32, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch32, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch32, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch32, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch32, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

ampl

Entry

B1L001S, U4-ch33, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch33, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch33, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch33, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch33, adc4

calib_packv5_042523_0143.root, FC#2, port C2

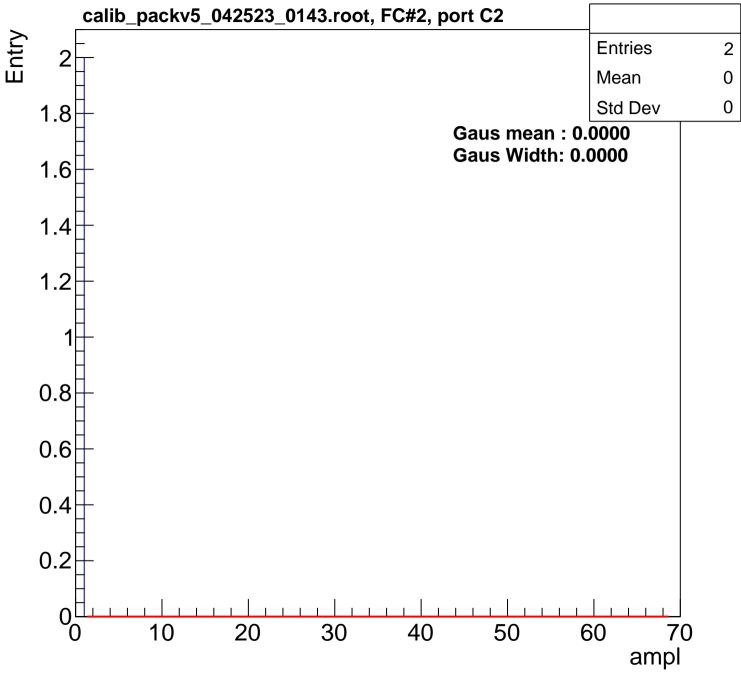|	
Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch33, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch33, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch33, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch34, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch34, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl
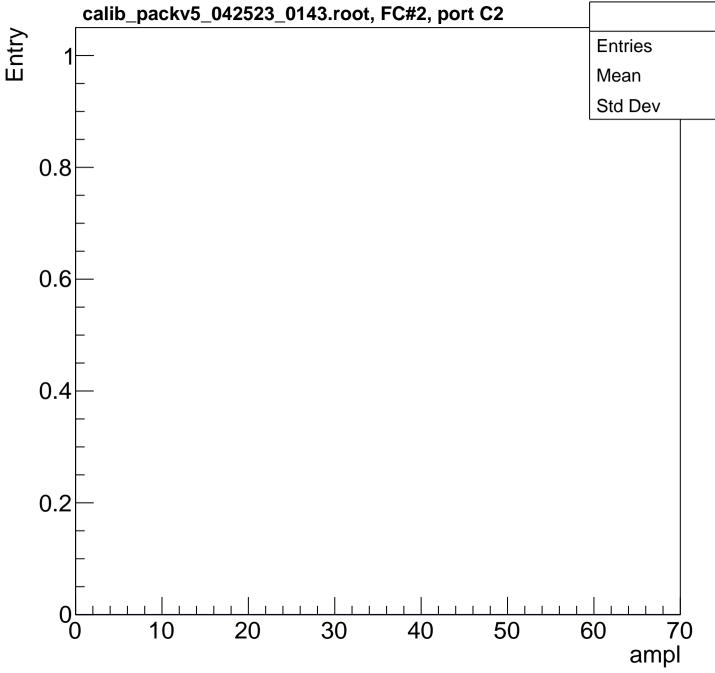
B1L001S, U4-ch34, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch34, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch34, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch34, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch34, adc6

calib_packv5_042523_0143.root, FC#2, port C2

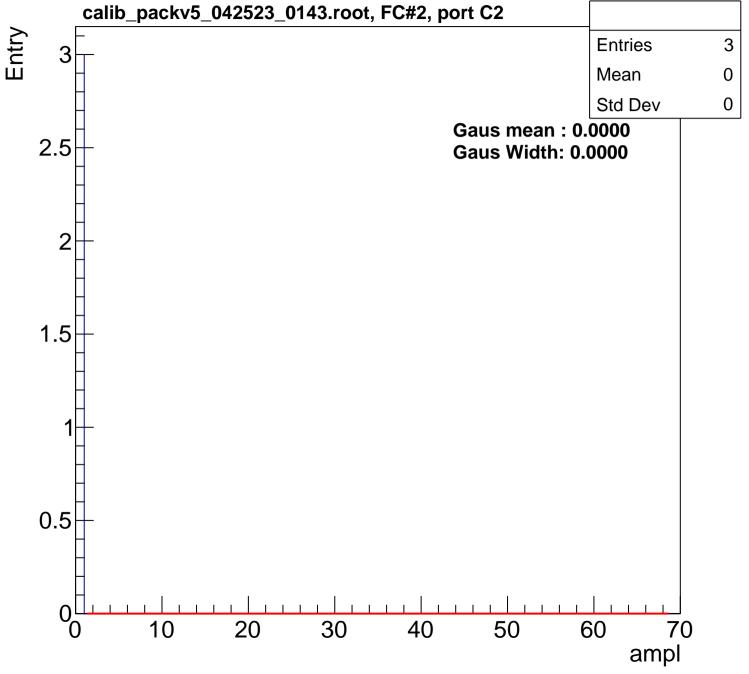|	
Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch34, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch35, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch35, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch35, adc2

calib_packv5_042523_0143.root, FC#2, port C2

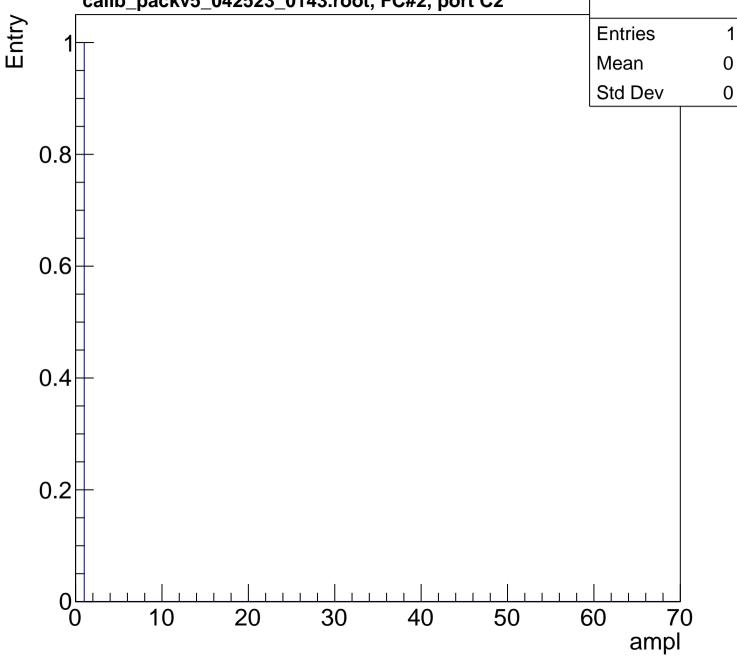|	
Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch35, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch35, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch35, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch35, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch35, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch36, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch36, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch36, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

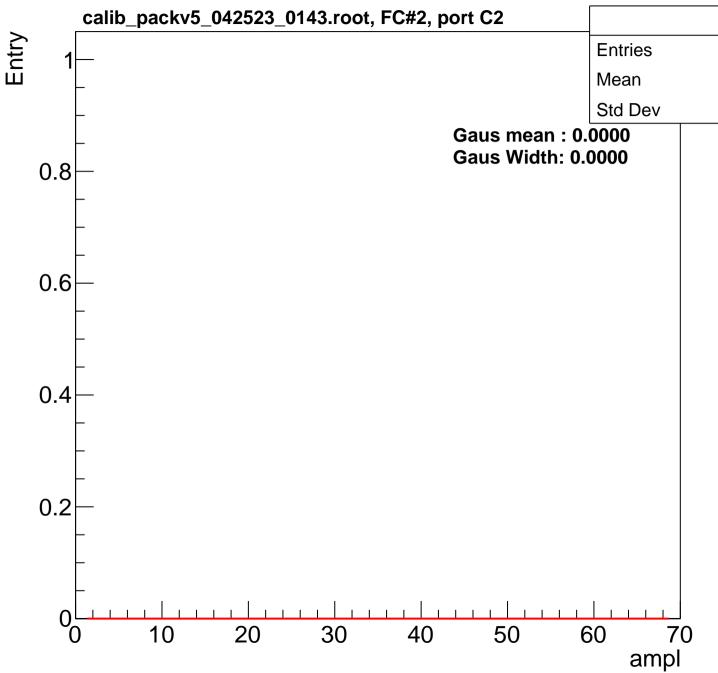# B1L001S, U4-ch36, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch36, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch36, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch36, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch36, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch37, adc0

calib_packv5_042523_0143.root, FC#2, port C2
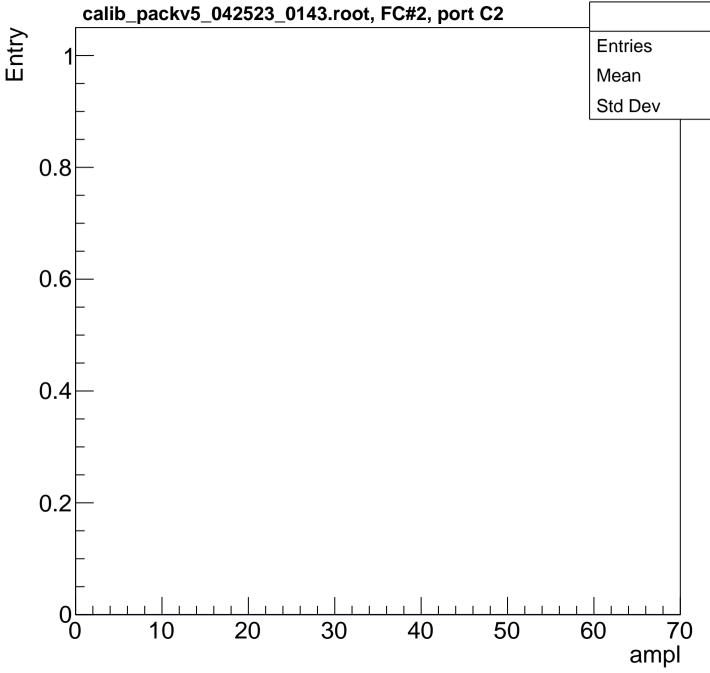
Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch37, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entry

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

ampl

B1L001S, U4-ch37, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch37, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch37, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entry

ampl

Entries	0
Mean	0
Std Dev	0

B1L001S, U4-ch37, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

B1L001S, U4-ch37, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

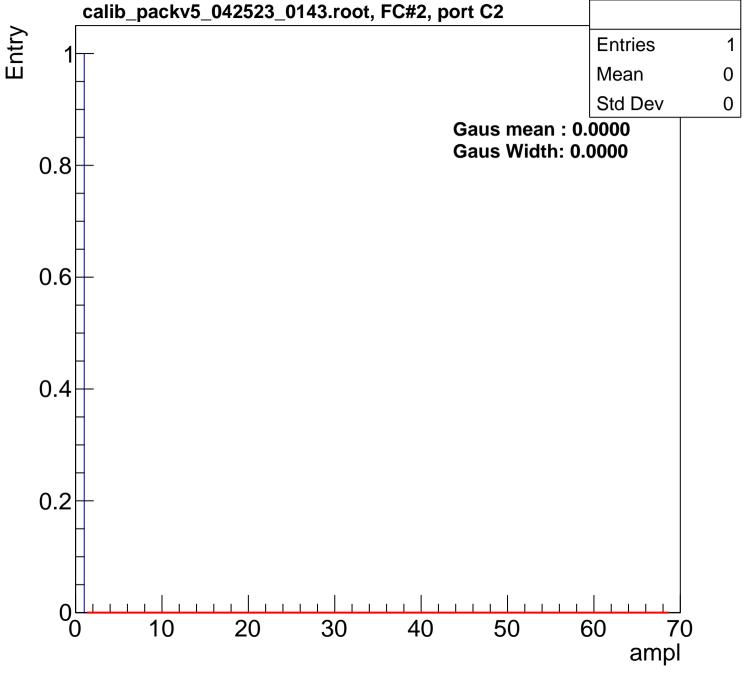# B1L001S, U4-ch37, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch38, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch38, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch38, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch38, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch38, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch38, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch38, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch39, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entry

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

ampl

B1L001S, U4-ch39, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch39, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch39, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch39, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch39, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch39, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch39, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch40, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch40, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch40, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch40, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch40, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

B1L001S, U4-ch40, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

B1L001S, U4-ch40, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch41, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entry

Entries	2
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

ampl

B1L001S, U4-ch41, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch41, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch41, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch41, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch41, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entry

ampl

Entries	0
Mean	0
Std Dev	0

B1L001S, U4-ch41, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch41, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch42, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch42, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch42, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch42, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch42, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch42, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch42, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch42, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entry

Entries	1
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch43, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch43, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch43, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch43, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch43, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch43, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch43, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch43, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	3
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch44, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	8
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch44, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch44, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch44, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch44, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch44, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch44, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch44, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch45, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch45, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch45, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch45, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch45, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entry

ampl

Entries	0
Mean	0
Std Dev	0

B1L001S, U4-ch45, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch45, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch45, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entry

ampl

Entries	1
Mean	0
Std Dev	0

B1L001S, U4-ch46, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch46, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch46, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch46, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch46, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch46, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

B1L001S, U4-ch46, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

Entry

B1L001S, U4-ch47, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch47, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch47, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch47, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch47, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch47, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch47, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch47, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch48, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch48, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch48, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch48, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch48, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch48, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch48, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch48, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch49, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch49, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch49, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch49, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch49, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch49, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch49, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch49, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch50, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	3
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch50, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch50, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch50, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch50, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch50, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch50, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch50, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

B1L001S, U4-ch51, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch51, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch51, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch51, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch51, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch51, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch51, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch51, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch52, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch52, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch52, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch52, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch52, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch52, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch52, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch52, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch53, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entry

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

ampl

B1L001S, U4-ch53, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch53, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch53, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch53, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch53, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

B1L001S, U4-ch53, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch53, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch54, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch54, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch54, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch54, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch54, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch54, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch54, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch54, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

B1L001S, U4-ch55, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch55, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch55, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch55, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch55, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch55, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entry

ampl

Entries	0
Mean	0
Std Dev	0

B1L001S, U4-ch55, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entry

Entries	1
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch56, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch56, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch56, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch56, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch56, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

B1L001S, U4-ch56, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch56, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch56, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entry

Entries	1
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch57, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch57, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch57, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch57, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch57, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch57, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch57, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch57, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

B1L001S, U4-ch58, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entry

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

ampl

B1L001S, U4-ch58, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch58, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch58, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch58, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch58, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch58, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch58, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch59, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch59, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch59, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch59, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch59, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch59, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch59, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch59, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch60, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch60, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch60, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch60, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch60, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch60, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch60, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch60, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch61, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch61, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch61, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch61, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch61, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

Entry

B1L001S, U4-ch61, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch61, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch61, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entry

ampl

Entries	1
Mean	0
Std Dev	0

B1L001S, U4-ch62, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch62, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch62, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch62, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch62, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch62, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch62, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch62, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch63, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entry

ampl

Entries	3
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch63, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch63, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch63, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch63, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch63, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch63, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch63, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

B1L001S, U4-ch64, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch64, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch64, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch64, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch64, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch64, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch64, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch64, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch65, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch65, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch65, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch65, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch65, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

B1L001S, U4-ch65, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch65, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch65, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	3
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch66, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch66, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch66, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch66, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch66, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

Entry

B1L001S, U4-ch66, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch66, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch66, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch67, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch67, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch67, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch67, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl
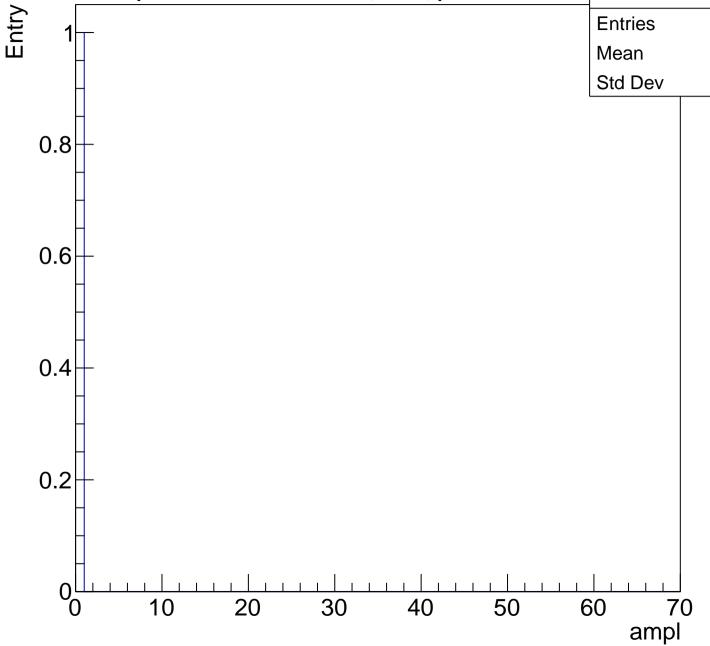
B1L001S, U4-ch67, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch67, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch67, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch67, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch68, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch68, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl
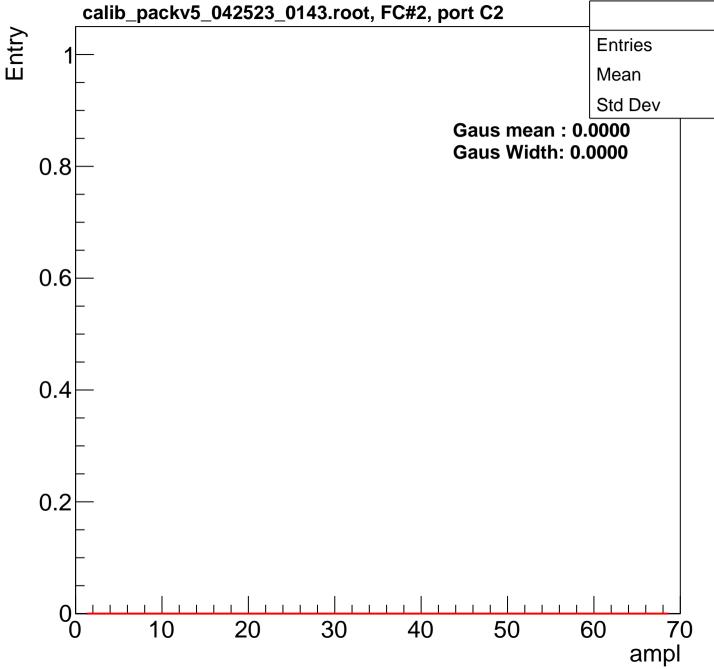
B1L001S, U4-ch68, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch68, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch68, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch68, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch68, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch68, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch69, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch69, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch69, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entry

Gaus mean : 0.0000
Gaus Width: 0.0000

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch69, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

B1L001S, U4-ch69, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch69, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch69, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch69, adc7
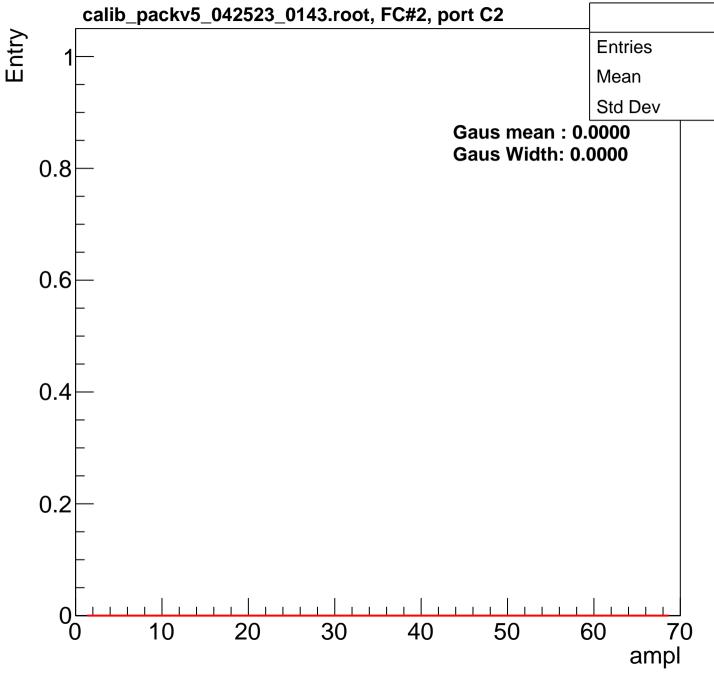
calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch70, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch70, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch70, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch70, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch70, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch70, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch70, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch70, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch71, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	3
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch71, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch71, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch71, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch71, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch71, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entry

ampl

Entries	0
Mean	0
Std Dev	0

B1L001S, U4-ch71, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch71, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch72, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch72, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch72, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch72, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch72, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch72, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch72, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch72, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch73, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch73, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch73, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch73, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch73, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch73, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch73, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch73, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch74, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch74, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch74, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch74, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch74, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch74, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch74, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch74, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch75, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch75, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch75, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch75, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch75, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch75, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch75, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch75, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch76, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch76, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch76, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch76, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch76, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch76, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch76, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch76, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch77, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch77, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch77, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch77, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch77, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

B1L001S, U4-ch77, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch77, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch77, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch78, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch78, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch78, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch78, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch78, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch78, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

Entry

B1L001S, U4-ch78, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch78, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	3
Mean	0
Std Dev	0

B1L001S, U4-ch79, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch79, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch79, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch79, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch79, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch79, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch79, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch79, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entry

ampl

Entries	2
Mean	0
Std Dev	0

B1L001S, U4-ch80, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch80, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch80, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch80, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch80, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch80, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch80, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

B1L001S, U4-ch80, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch81, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch81, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch81, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch81, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch81, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

B1L001S, U4-ch81, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch81, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

Entry

B1L001S, U4-ch81, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch82, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch82, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch82, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch82, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch82, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch82, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch82, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch82, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entry

Entries	1
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch83, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch83, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch83, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch83, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch83, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch83, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch83, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch83, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch84, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch84, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch84, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch84, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch84, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch84, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch84, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch84, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch85, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch85, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch85, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch85, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch85, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch85, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch85, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch85, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch86, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch86, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch86, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch86, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch86, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch86, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch86, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch87, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Gaus mean : 0.0000
Gaus Width: 0.0000

Entries	2
Mean	0
Std Dev	0

B1L001S, U4-ch87, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch87, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch87, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entry

ampl

Entries	0
Mean	0
Std Dev	0

B1L001S, U4-ch87, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch87, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch87, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch87, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch88, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch88, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch88, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch88, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch88, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch88, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch88, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch88, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch89, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch89, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch89, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch89, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch89, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch89, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch89, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch90, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch90, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl
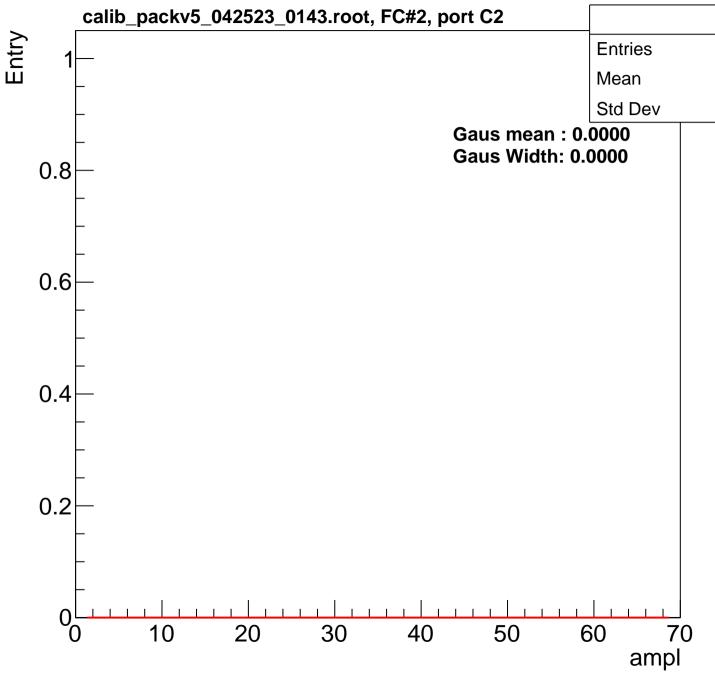
B1L001S, U4-ch90, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch90, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch90, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

Entry

B1L001S, U4-ch90, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch90, adc6

calib_packv5_042523_0143.root, FC#2, port C2

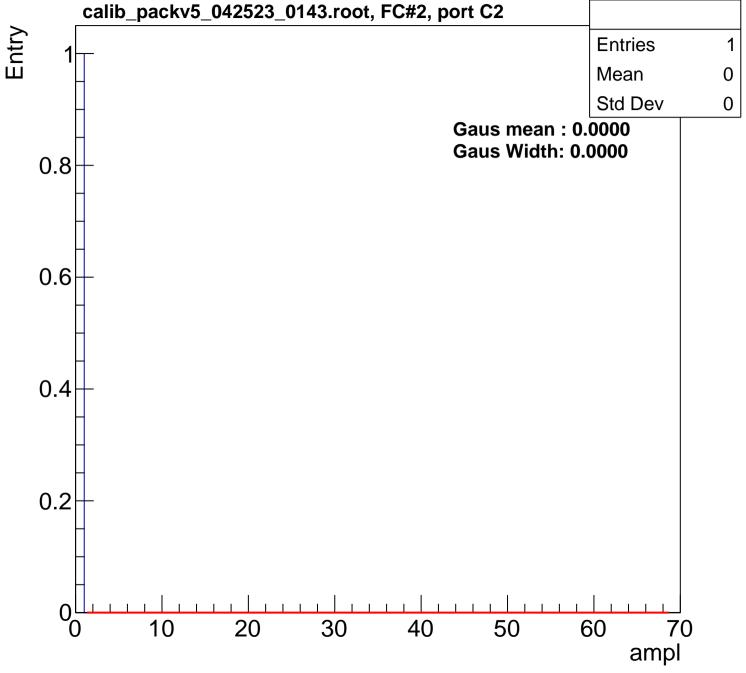|	
Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch90, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch91, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch91, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entry

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

ampl

B1L001S, U4-ch91, adc2

calib_packv5_042523_0143.root, FC#2, port C2

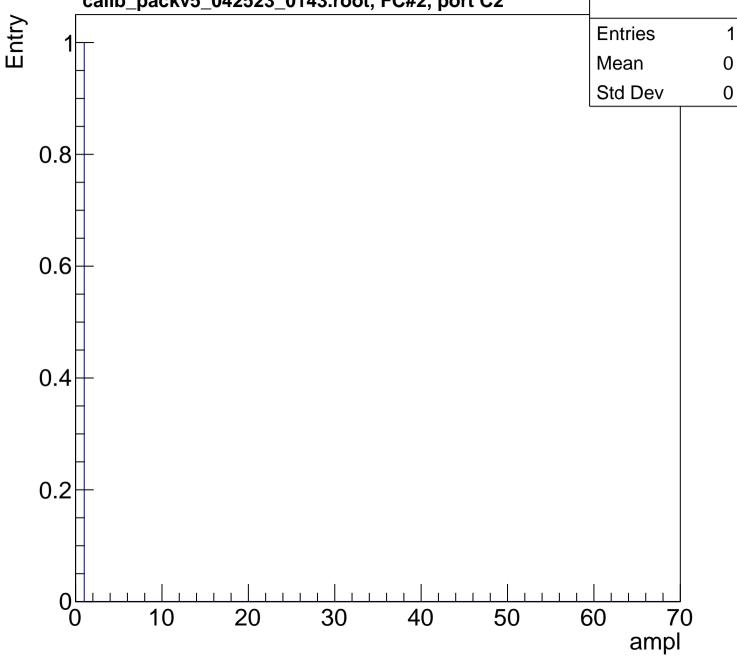|	
Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch91, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch91, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch91, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch91, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

B1L001S, U4-ch91, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	3
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch92, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch92, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl
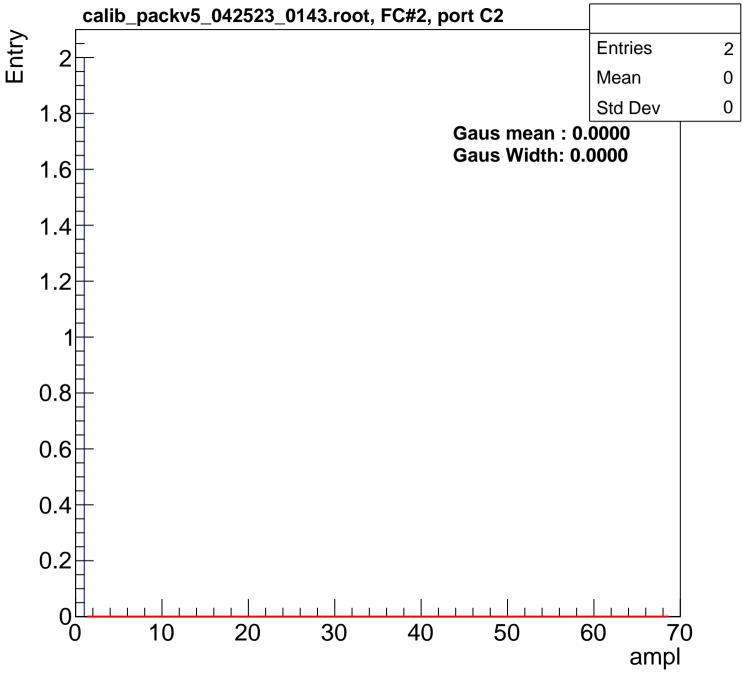
B1L001S, U4-ch92, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch92, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch92, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch92, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch92, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch92, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

ampl

Entry

B1L001S, U4-ch93, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch93, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch93, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch93, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch93, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch93, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch93, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

B1L001S, U4-ch93, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

ampl

Entry

B1L001S, U4-ch94, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch94, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch94, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch94, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch94, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch94, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch94, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch94, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch95, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	3
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch95, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch95, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch95, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch95, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch95, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch95, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch95, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch96, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch96, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch96, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch96, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch96, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch96, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch96, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch96, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch97, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch97, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch97, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch97, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch97, adc4

calib_packv5_042523_0143.root, FC#2, port C2

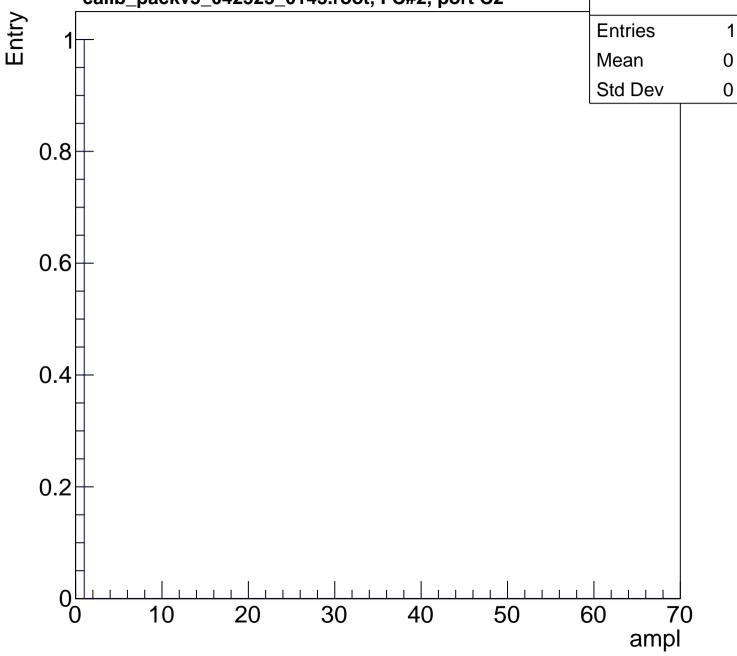|	
Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch97, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

B1L001S, U4-ch97, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch97, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch98, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch98, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000
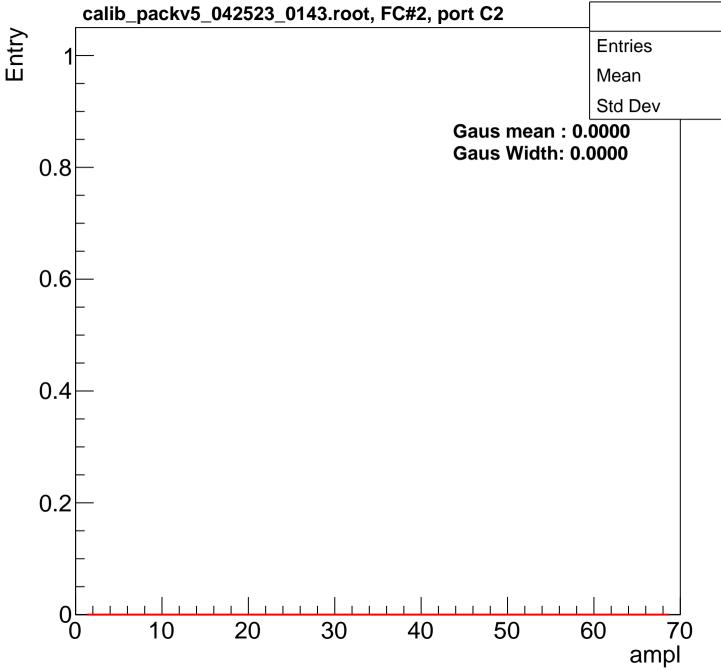
B1L001S, U4-ch98, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch98, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch98, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch98, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch98, adc6

calib_packv5_042523_0143.root, FC#2, port C2

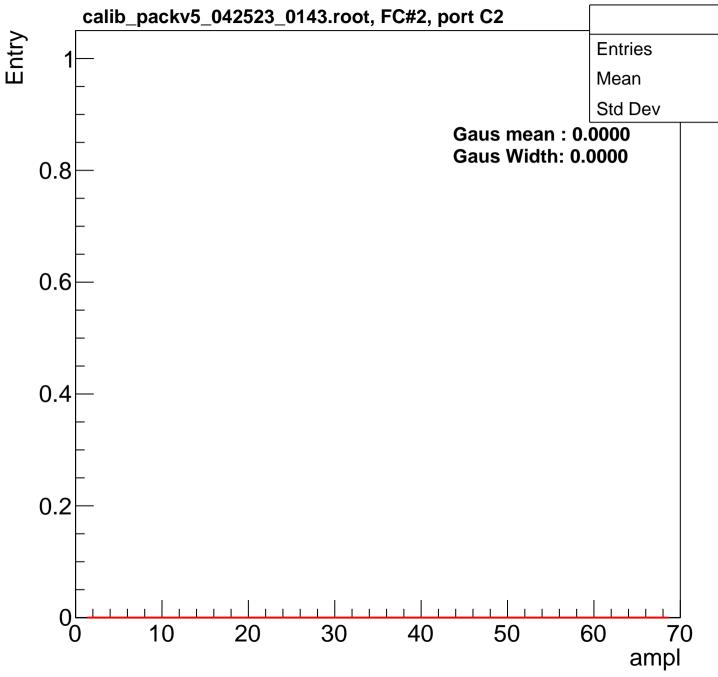|	
Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch98, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch99, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch99, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch99, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch99, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch99, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch99, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch99, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch99, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch100, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch100, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch100, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch100, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch100, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

Entry

B1L001S, U4-ch100, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch100, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch100, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch101, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch101, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch101, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch101, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch101, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch101, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch101, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch101, adc7
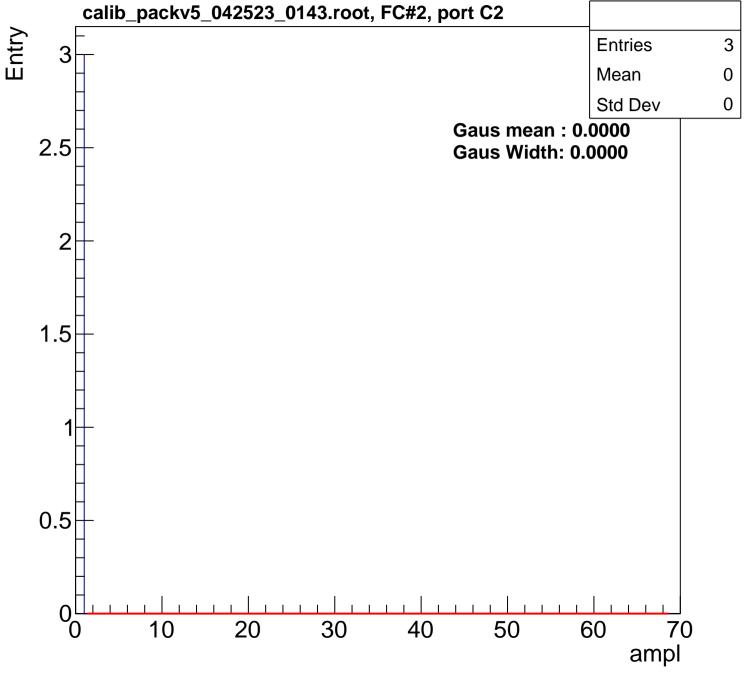
calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch102, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch102, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch102, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch102, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch102, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch102, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch102, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch102, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch103, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch103, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch103, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch103, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch103, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch103, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch103, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch103, adc7

Entry

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch104, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	4
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch104, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch104, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch104, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch104, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch104, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch104, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch105, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch105, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entry

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

ampl

B1L001S, U4-ch105, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch105, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch105, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch105, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch105, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch105, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

B1L001S, U4-ch106, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch106, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch106, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch106, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch106, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch106, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch106, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch106, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch107, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	3
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch107, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch107, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch107, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

B1L001S, U4-ch107, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch107, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch107, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch107, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch108, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch108, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch108, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch108, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch108, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch108, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch108, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch108, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch109, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch109, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch109, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch109, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch109, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch109, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch109, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch109, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch110, adc1

calib_packv5_042523_0143.root, FC#2, port C2

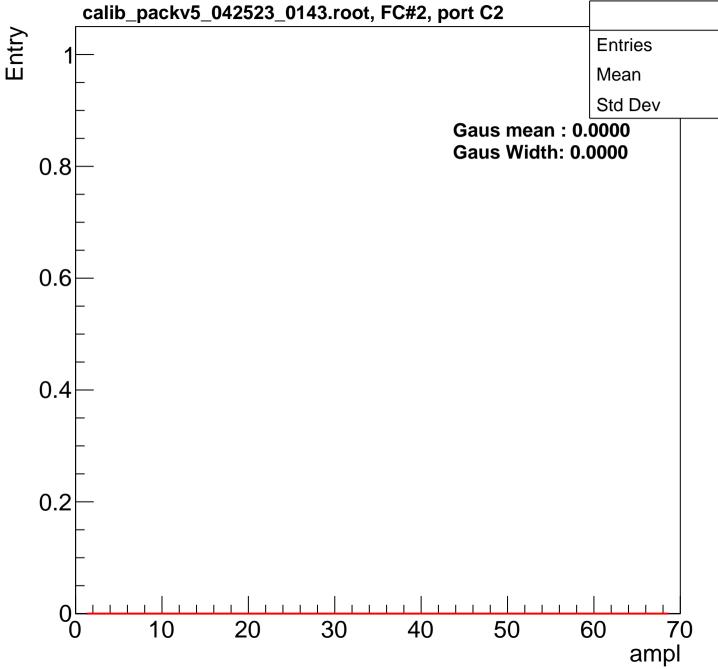|	
Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch110, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch110, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch110, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch110, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch110, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch110, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch111, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	3
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch111, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entry

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

ampl

B1L001S, U4-ch111, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch111, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch111, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch111, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch111, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch111, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch112, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch112, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entry

ampl

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch112, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch112, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch112, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch112, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

Entry

B1L001S, U4-ch112, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch112, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entry

ampl

Entries	1
Mean	0
Std Dev	0

B1L001S, U4-ch113, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch113, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch113, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch113, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch113, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch113, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch113, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch113, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch114, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	3
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch114, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entry

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

ampl

B1L001S, U4-ch114, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

B1L001S, U4-ch114, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch114, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch114, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch114, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch115, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch115, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch115, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch115, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch115, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch115, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch115, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch115, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch116, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch116, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch116, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch116, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch116, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch116, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch116, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch116, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch117, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entry

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

ampl

B1L001S, U4-ch117, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entry

ampl

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch117, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

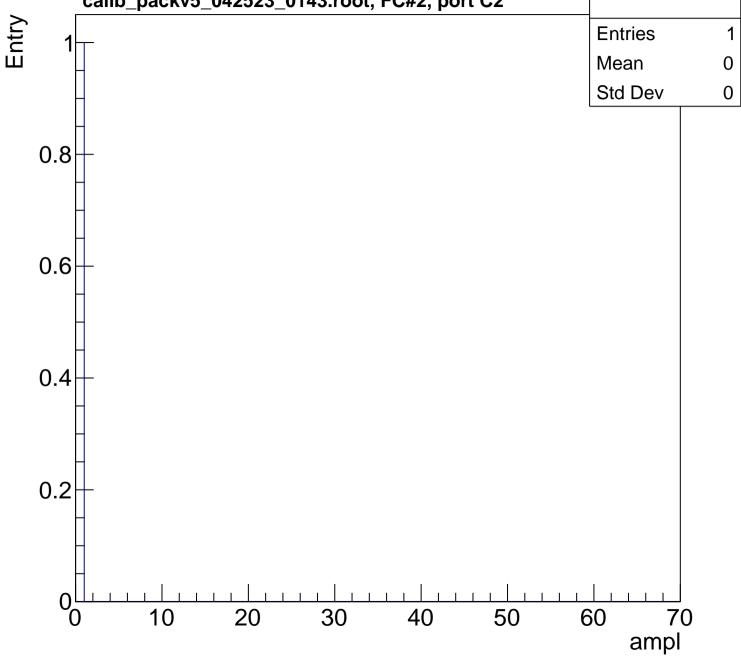**Gaus mean : 0.0000**
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch117, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch117, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch117, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch117, adc6

calib_packv5_042523_0143.root, FC#2, port C2

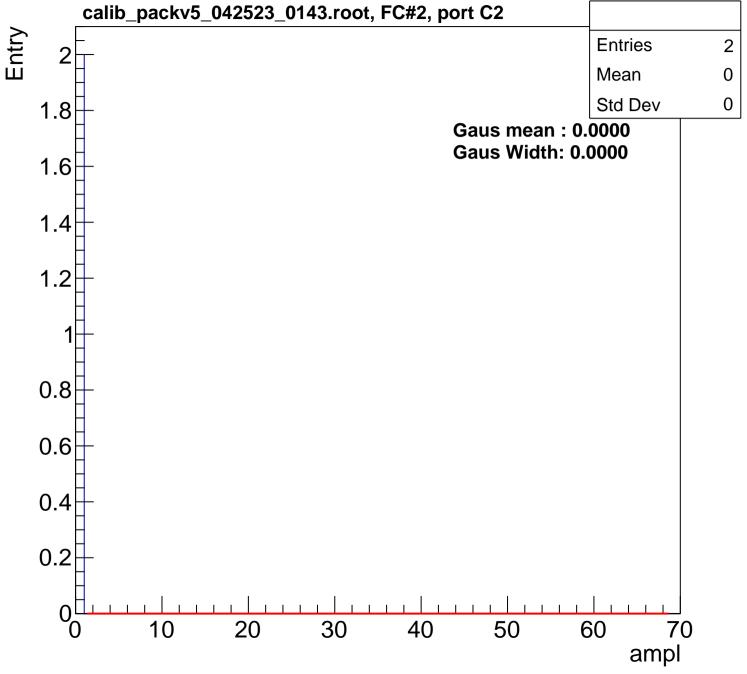|	
Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch117, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch118, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch118, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch118, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch118, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch118, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch118, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch118, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch118, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch119, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch119, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch119, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch119, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch119, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entry

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch119, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch119, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch119, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch120, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch120, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch120, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch120, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch120, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch120, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch120, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch120, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch121, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch121, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch121, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch121, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch121, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch121, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

B1L001S, U4-ch121, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch121, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch122, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch122, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch122, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch122, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch122, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

Entry

B1L001S, U4-ch122, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch122, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch122, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

Entry

B1L001S, U4-ch123, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch123, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch123, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch123, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

B1L001S, U4-ch123, adc4

calib_packv5_042523_0143.root, FC#2, port C2

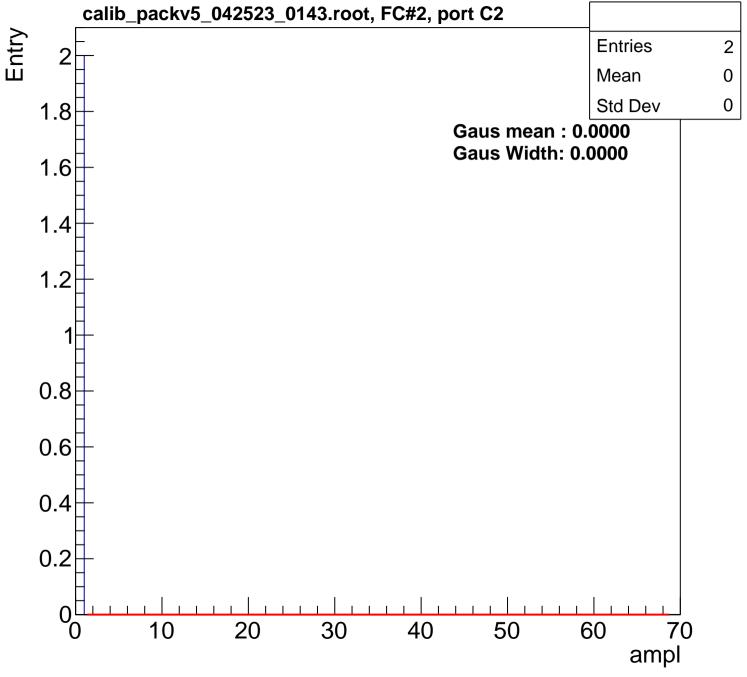|	
Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch123, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch123, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

Entry

B1L001S, U4-ch123, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch124, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch124, adc1

calib_packv5_042523_0143.root, FC#2, port C2

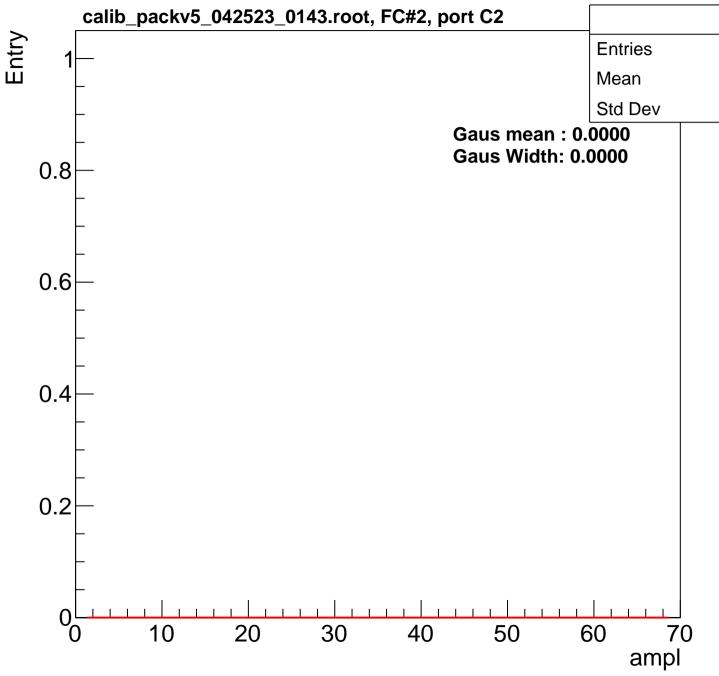|	
Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch124, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch124, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch124, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch124, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch124, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch124, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	4
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch125, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch125, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entry

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

ampl

B1L001S, U4-ch125, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch125, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch125, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch125, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch125, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch125, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch126, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	2
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl

B1L001S, U4-ch126, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch126, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
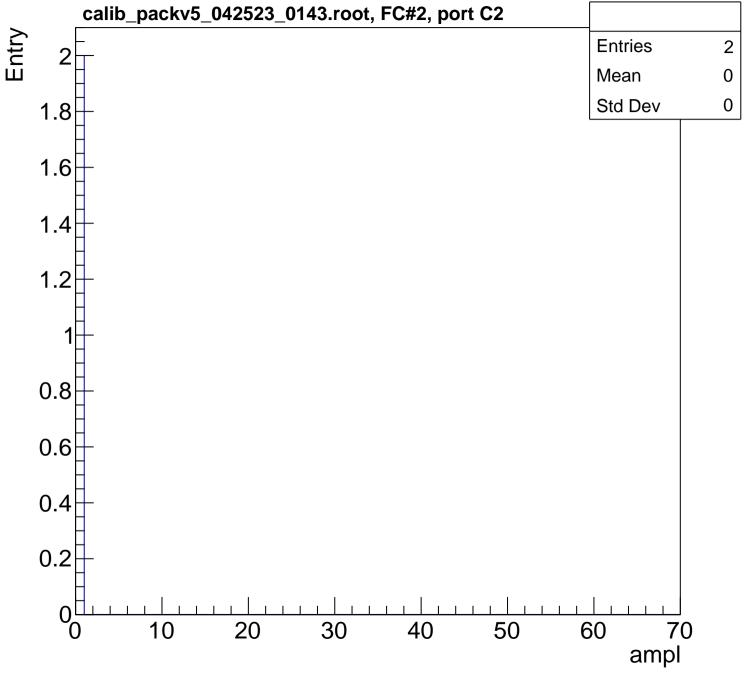**Gaus Width: 0.0000**

Entry

ampl

B1L001S, U4-ch126, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch126, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch126, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch126, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch126, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch127, adc0

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

Entry

ampl
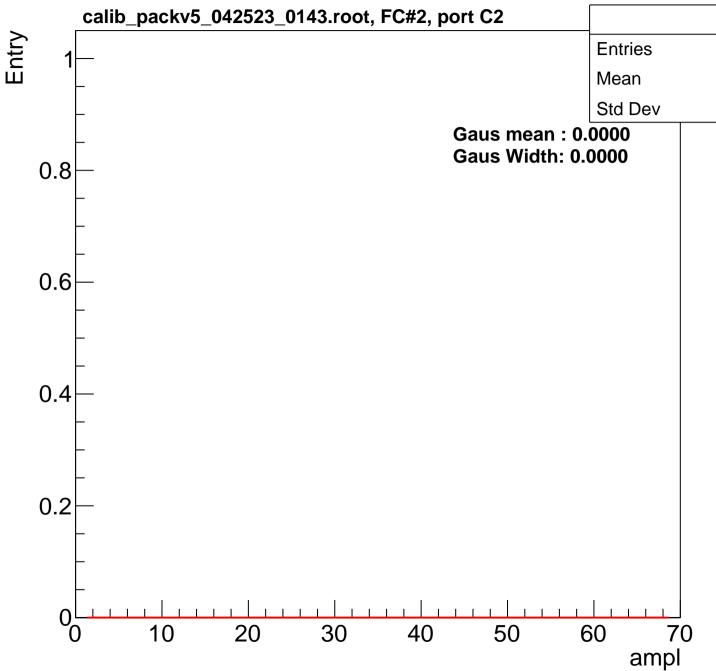
B1L001S, U4-ch127, adc1

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch127, adc2

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Gaus mean : 0.0000
Gaus Width: 0.0000

B1L001S, U4-ch127, adc3

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

ampl

B1L001S, U4-ch127, adc4

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch127, adc5

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch127, adc6

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B1L001S, U4-ch127, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

B1L001S, U4-ch127, adc7

calib_packv5_042523_0143.root, FC#2, port C2

Entries	0
Mean	0
Std Dev	0

Entry

ampl