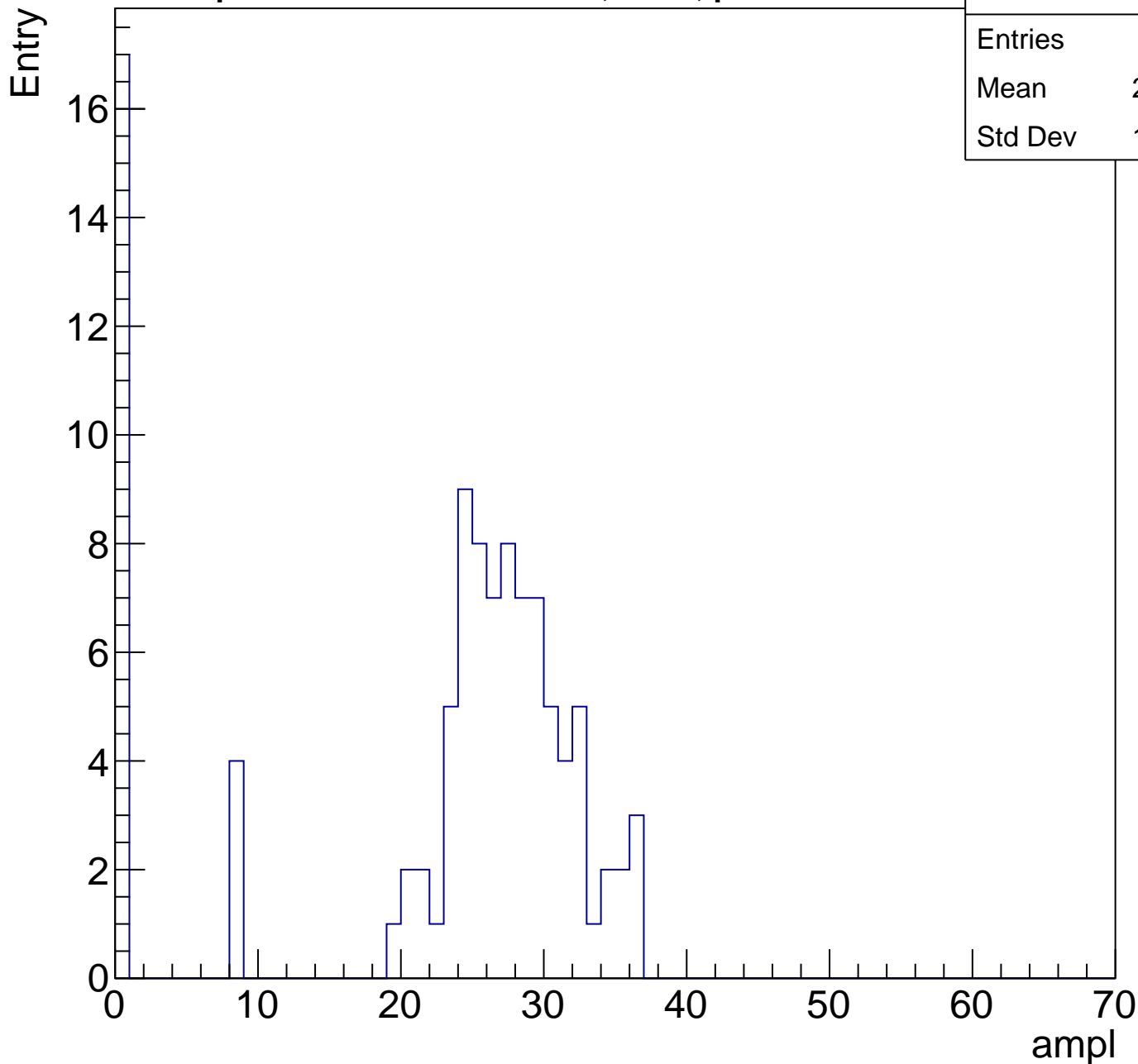


B1L103S, U9-ch0, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	100
Mean	21.96
Std Dev	11.19

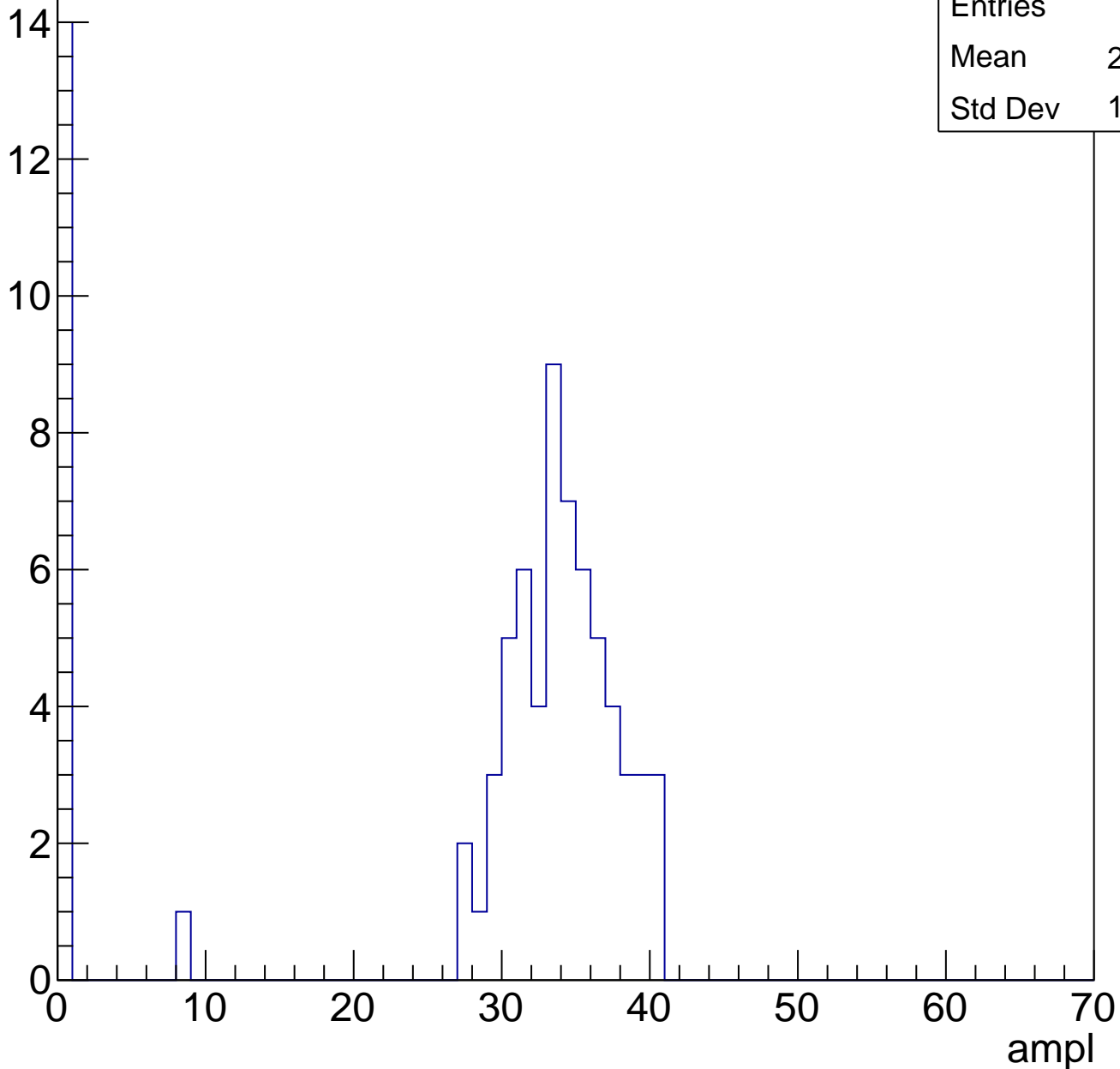


B1L103S, U9-ch0, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	76
Mean	27.17
Std Dev	13.56

Entry

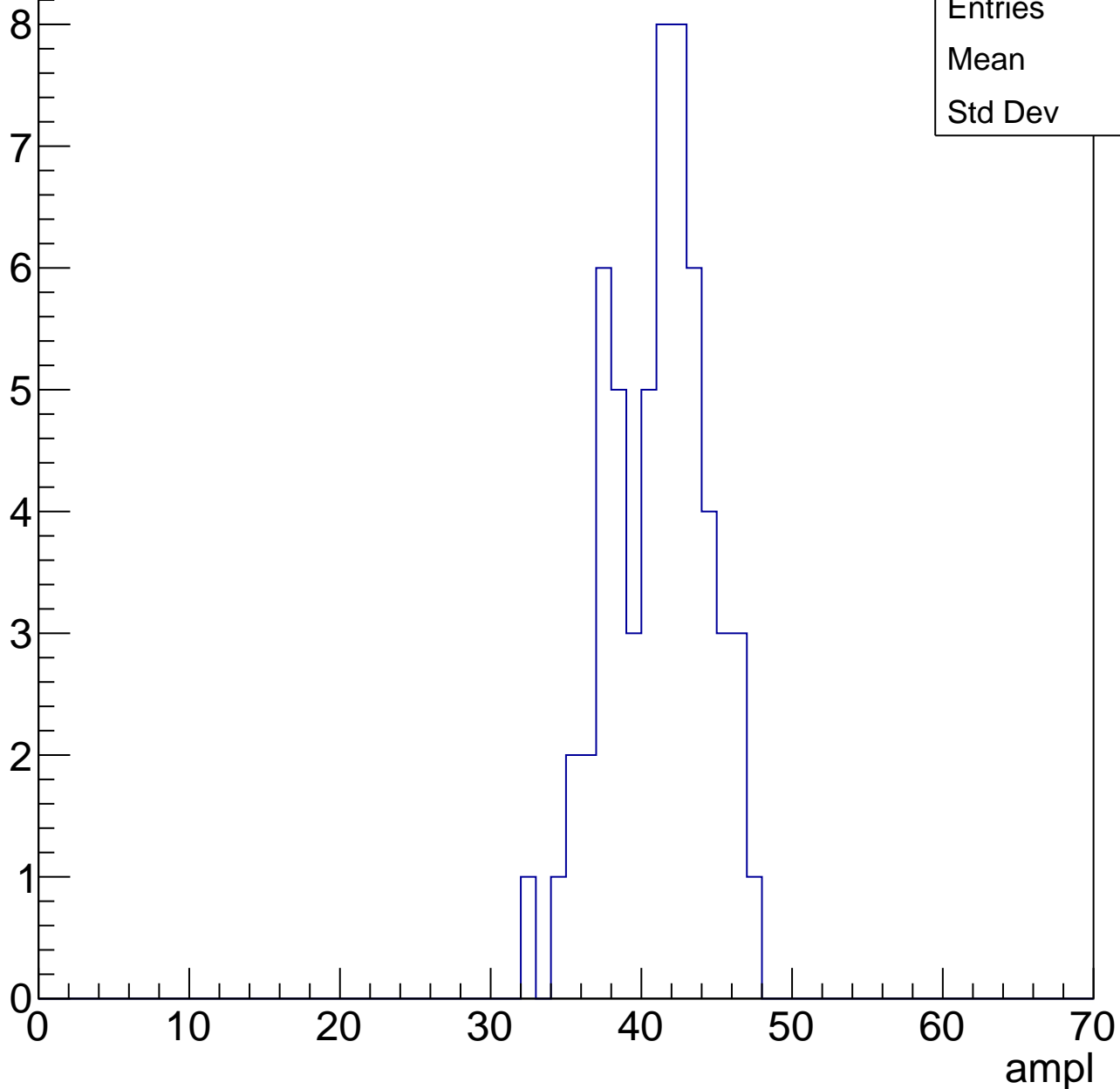


B1L103S, U9-ch0, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	40.6
Std Dev	3.29

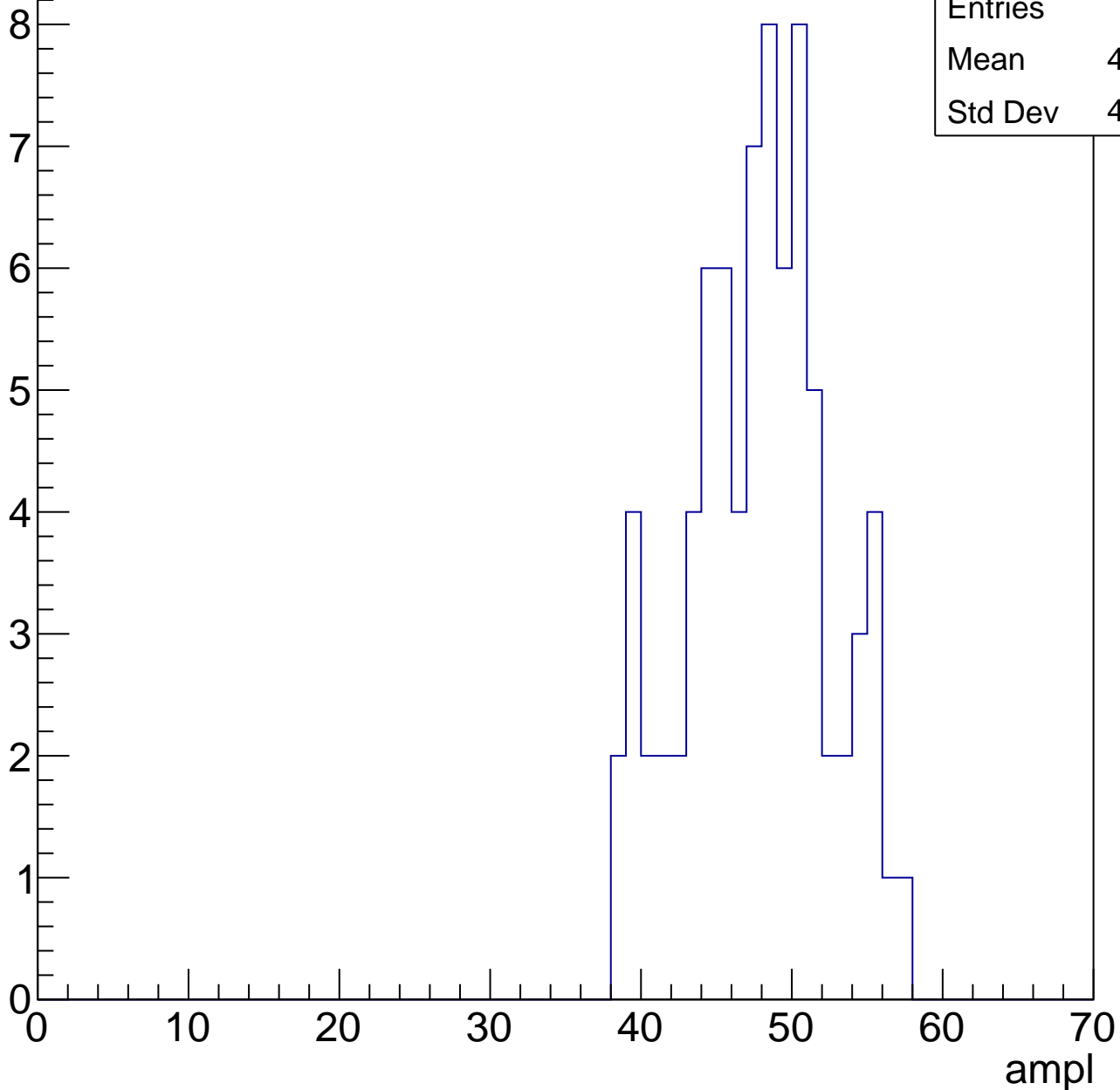


B1L103S, U9-ch0, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	79
Mean	47.28
Std Dev	4.595

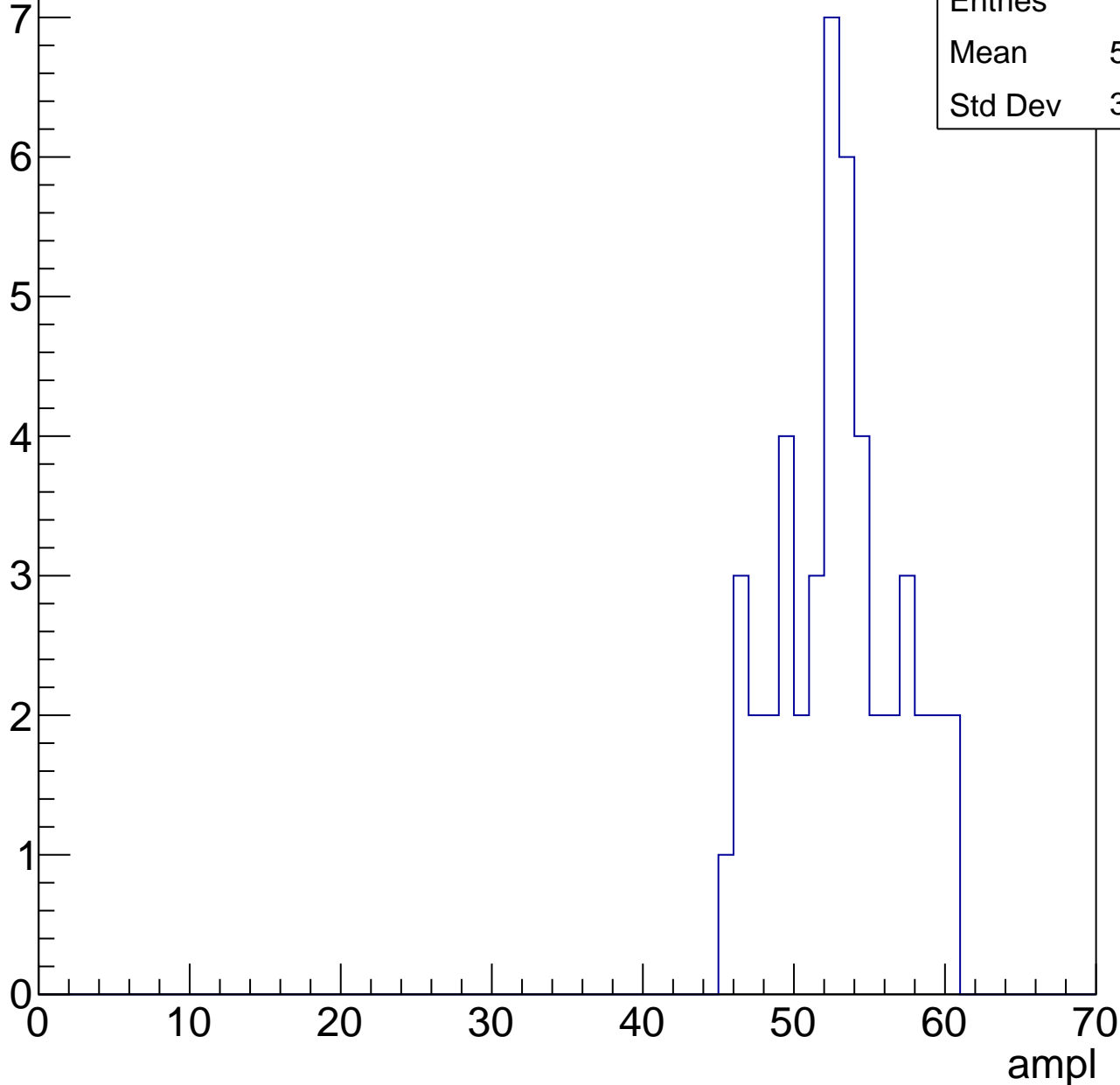


B1L103S, U9-ch0, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

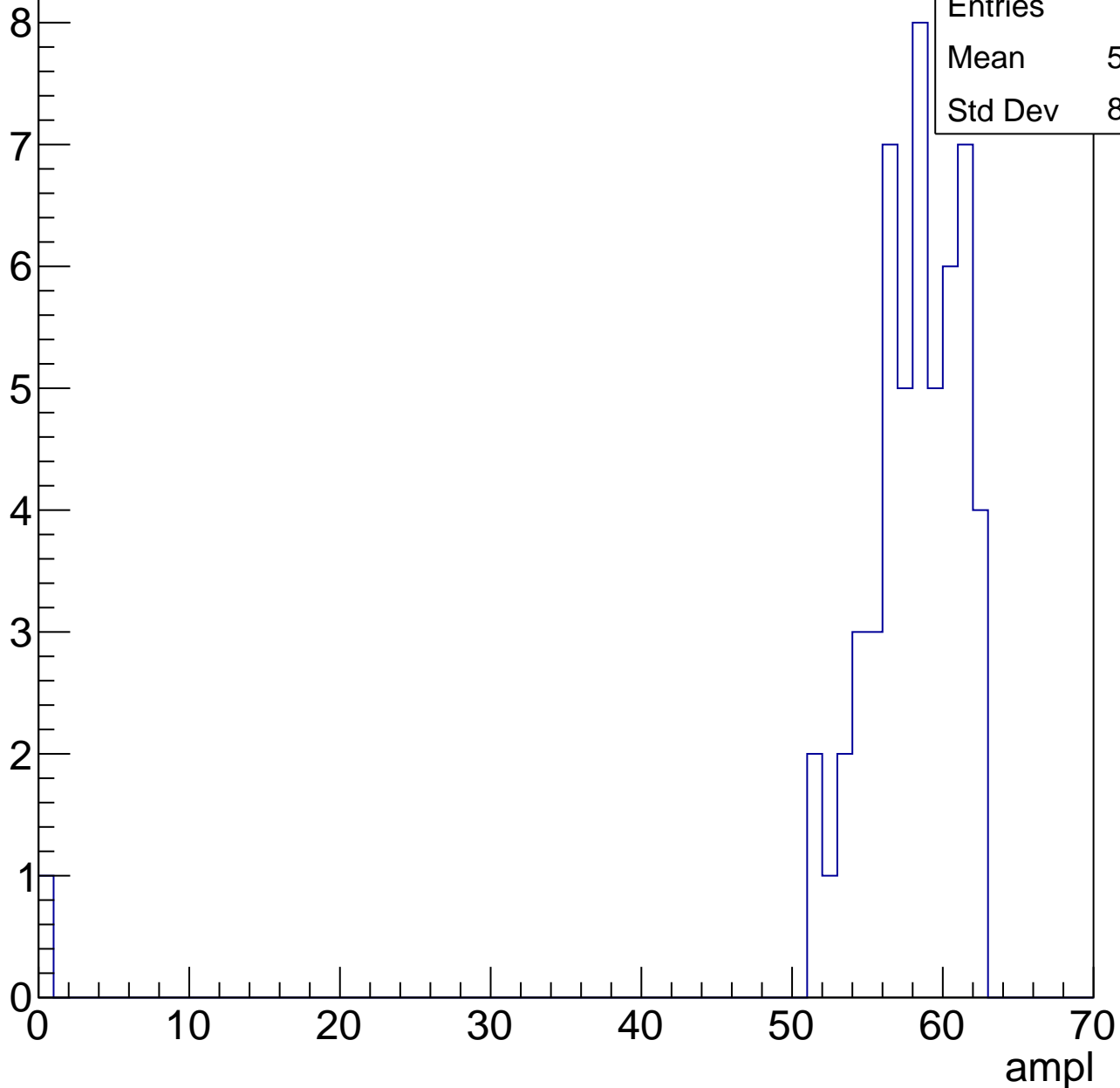
Entries	47
Mean	52.49
Std Dev	3.913



B1L103S, U9-ch0, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch0, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entries	25
Mean	61.32
Std Dev	2.092

Entry

10

8

6

4

2

0

0

10

20

30

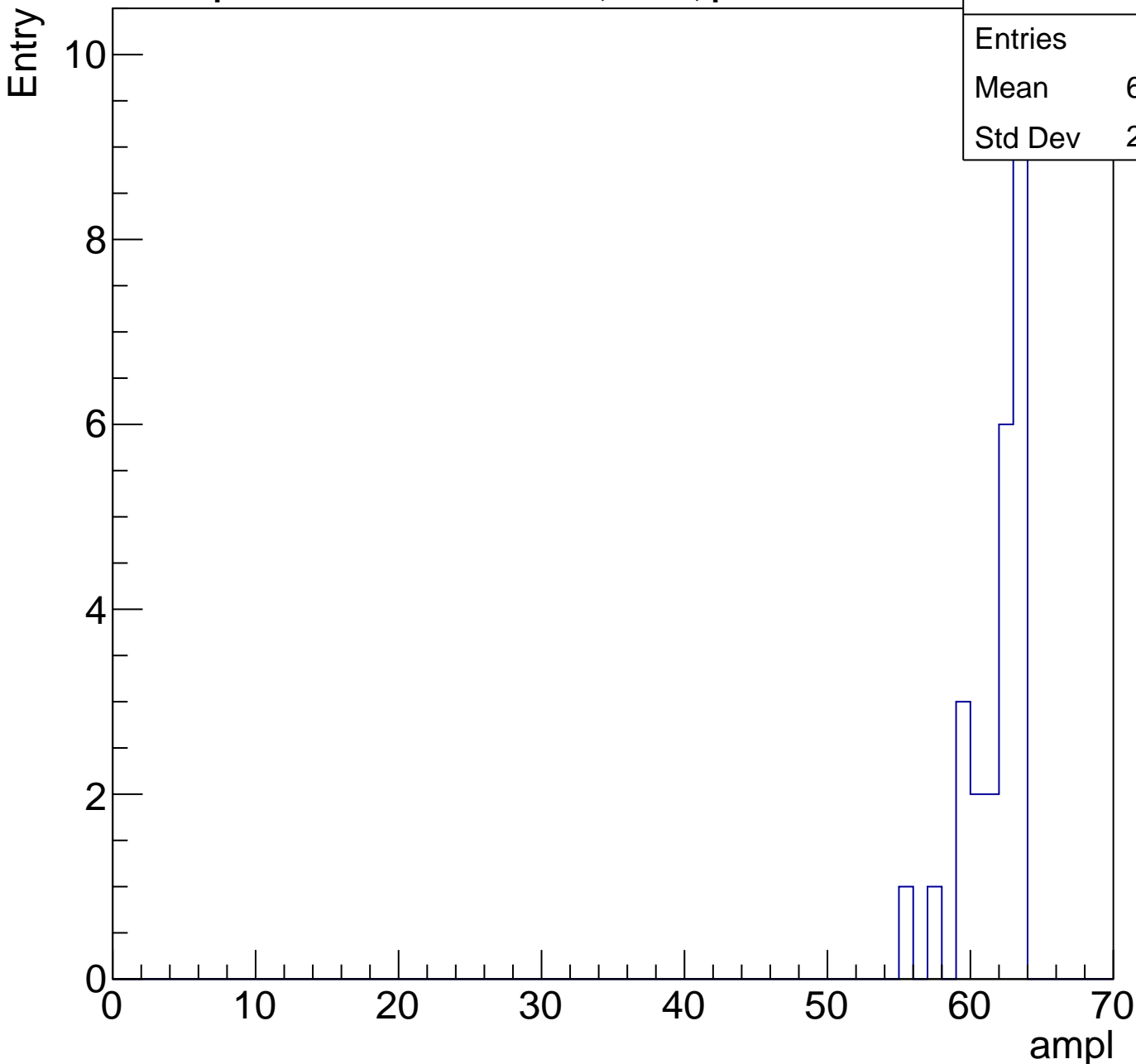
40

50

60

ampl

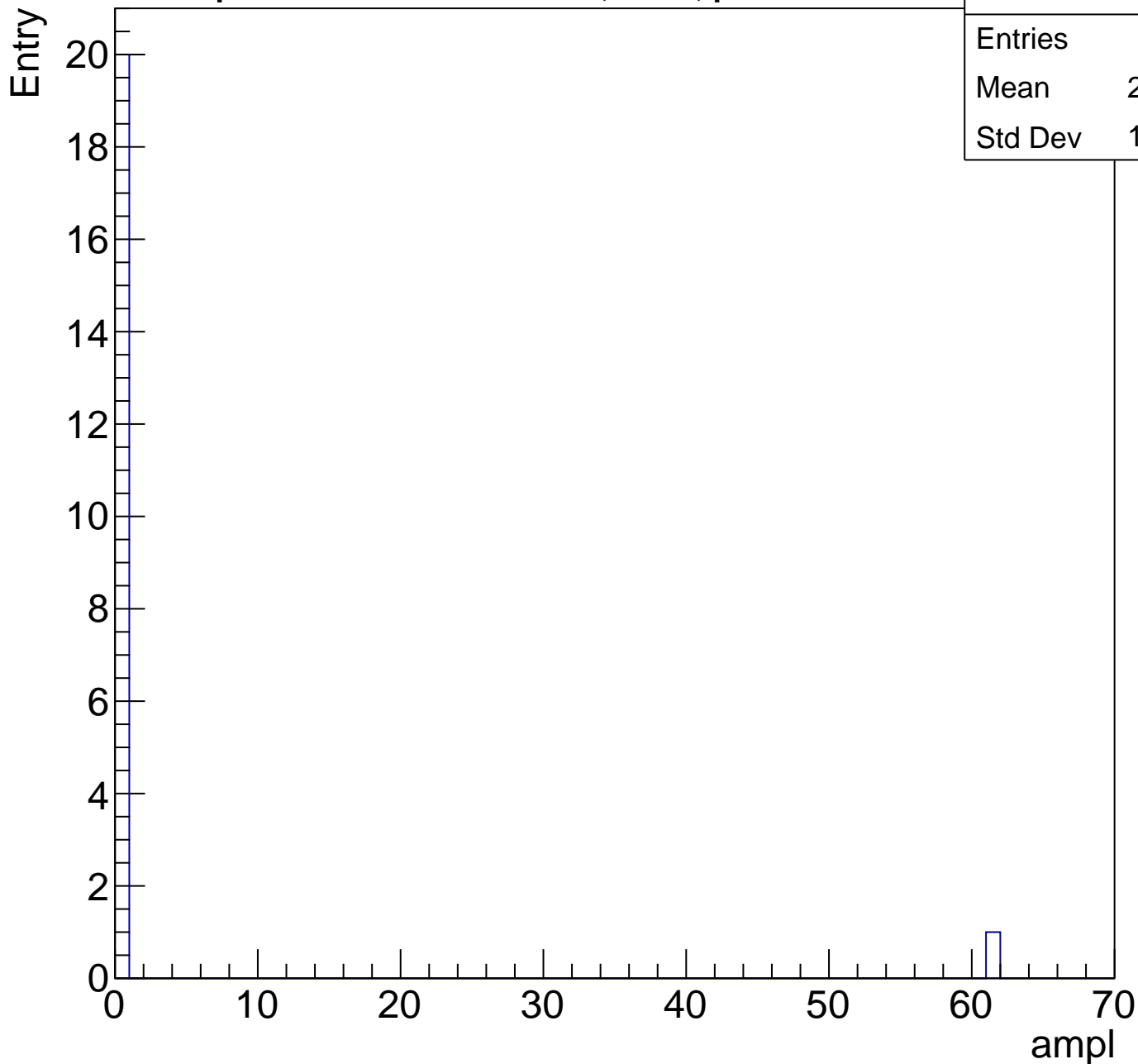
70



B1L103S, U9-ch0, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	2.905
Std Dev	12.99

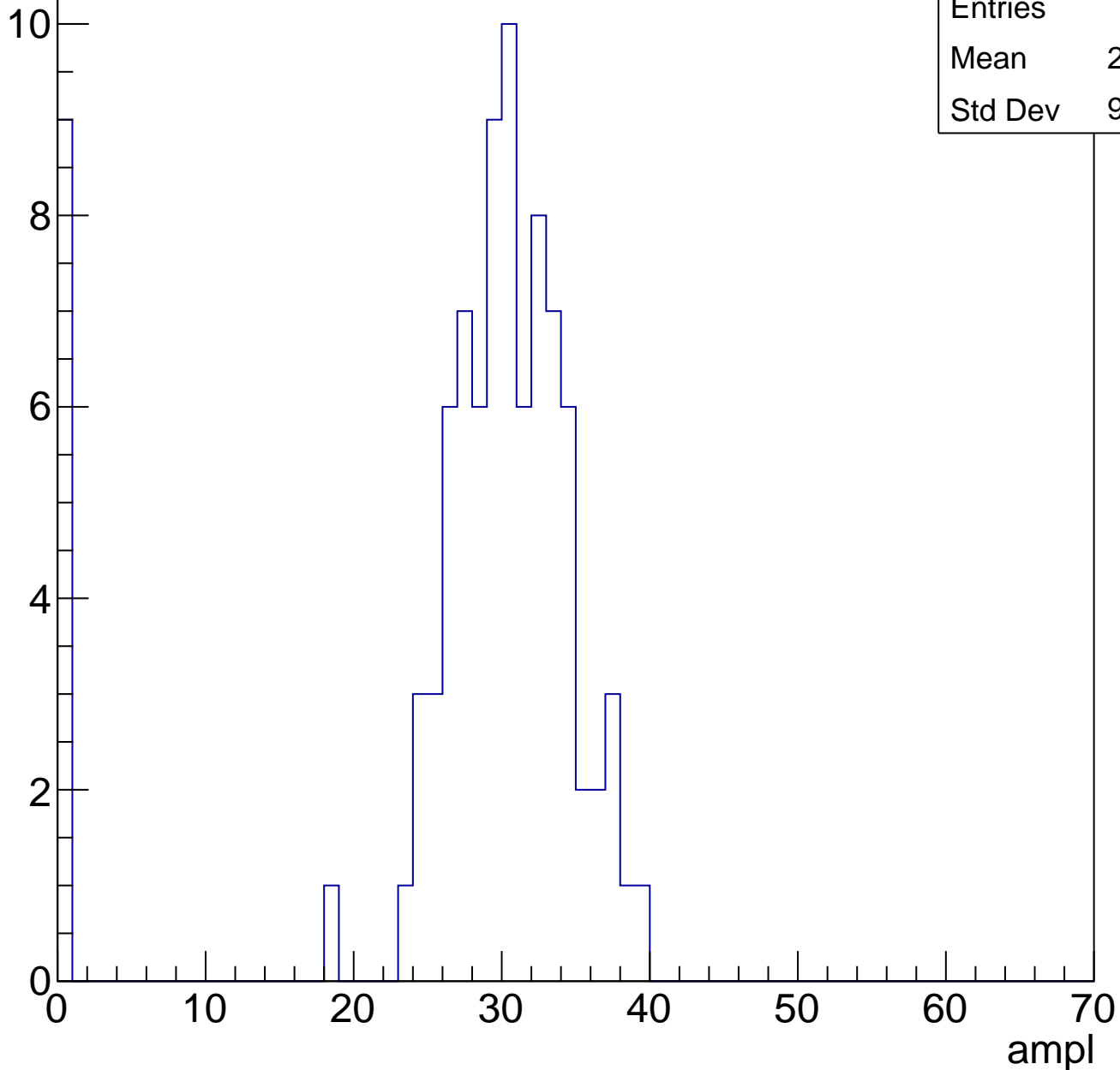


B1L103S, U9-ch1, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	91
Mean	27.13
Std Dev	9.682

Entry

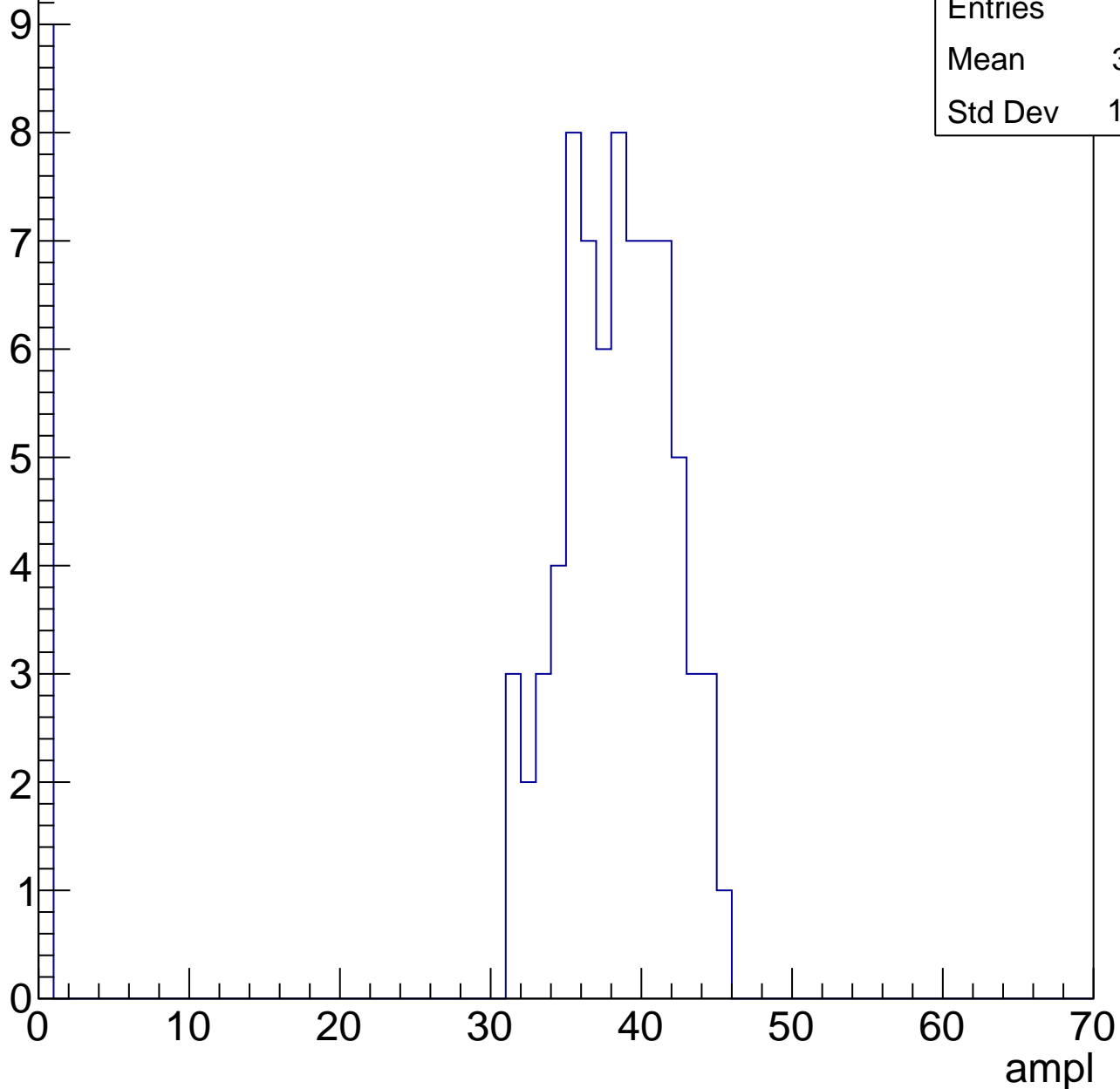


B1L103S, U9-ch1, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

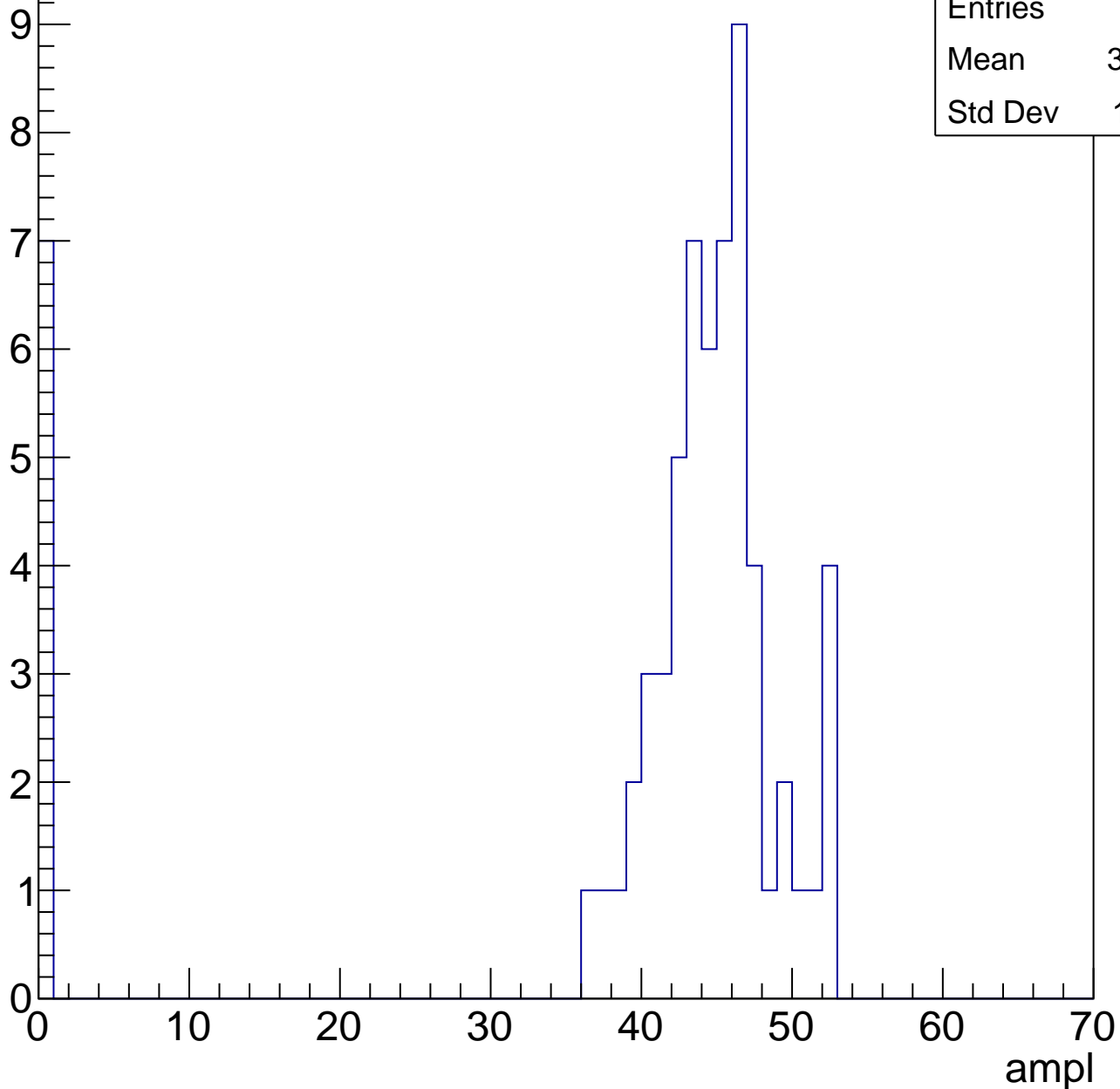
Entries	83
Mean	33.81
Std Dev	12.23



B1L103S, U9-ch1, adc2

calib_packv5_041523_1651.root, FC#0, port C2

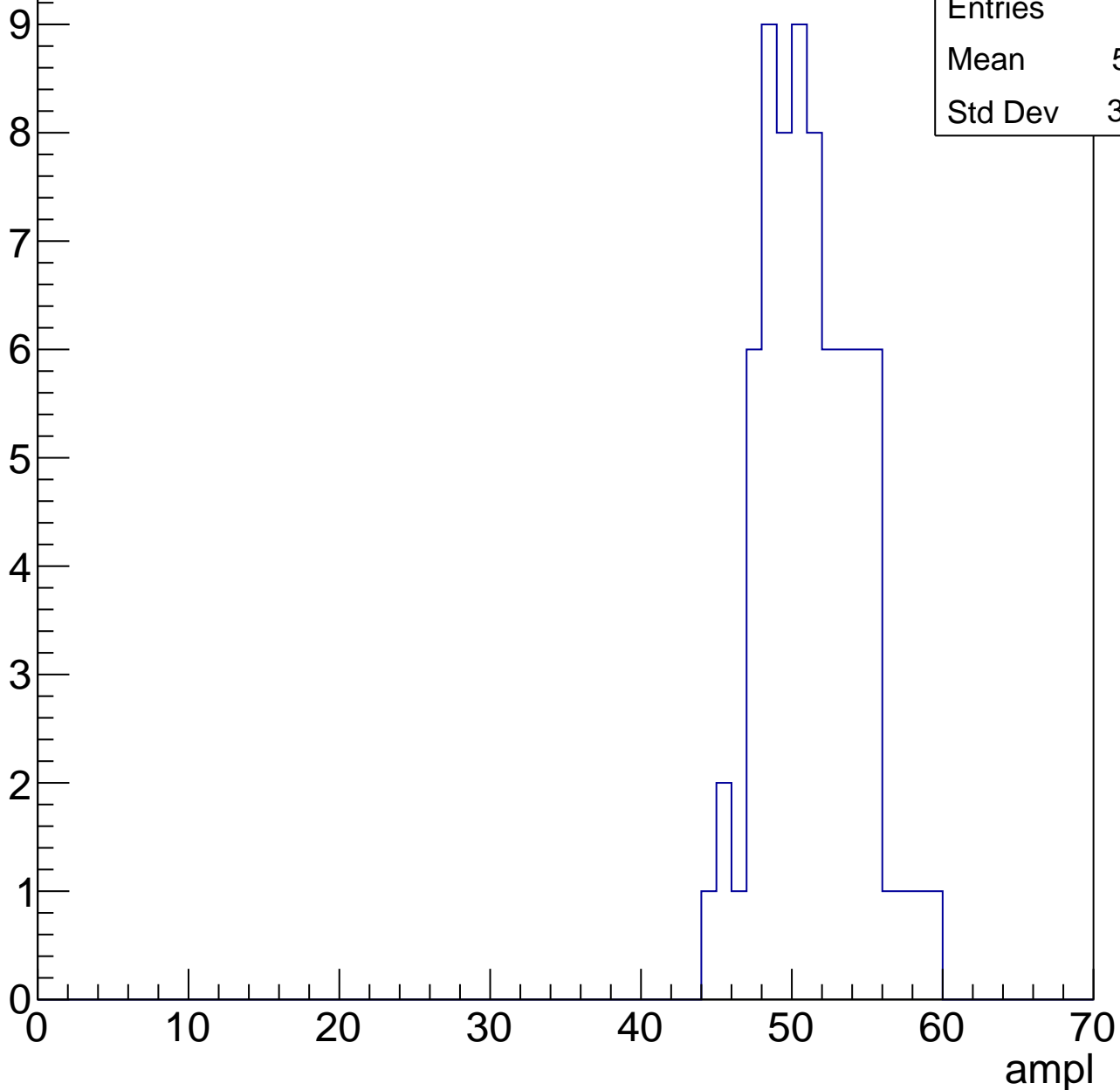
Entry



B1L103S, U9-ch1, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry



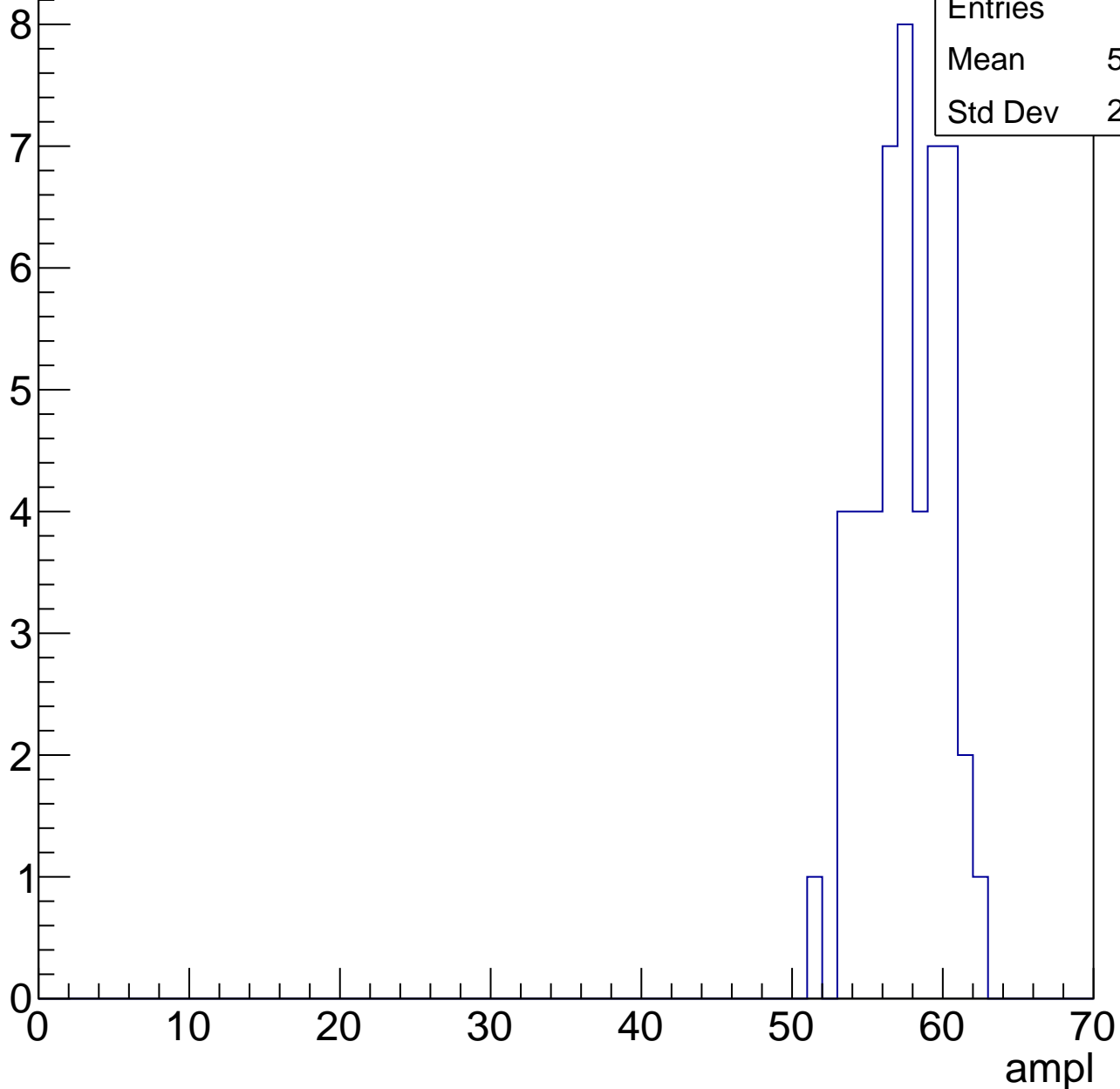
Entries	72
Mean	50.81
Std Dev	3.152

B1L103S, U9-ch1, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	57.06
Std Dev	2.519

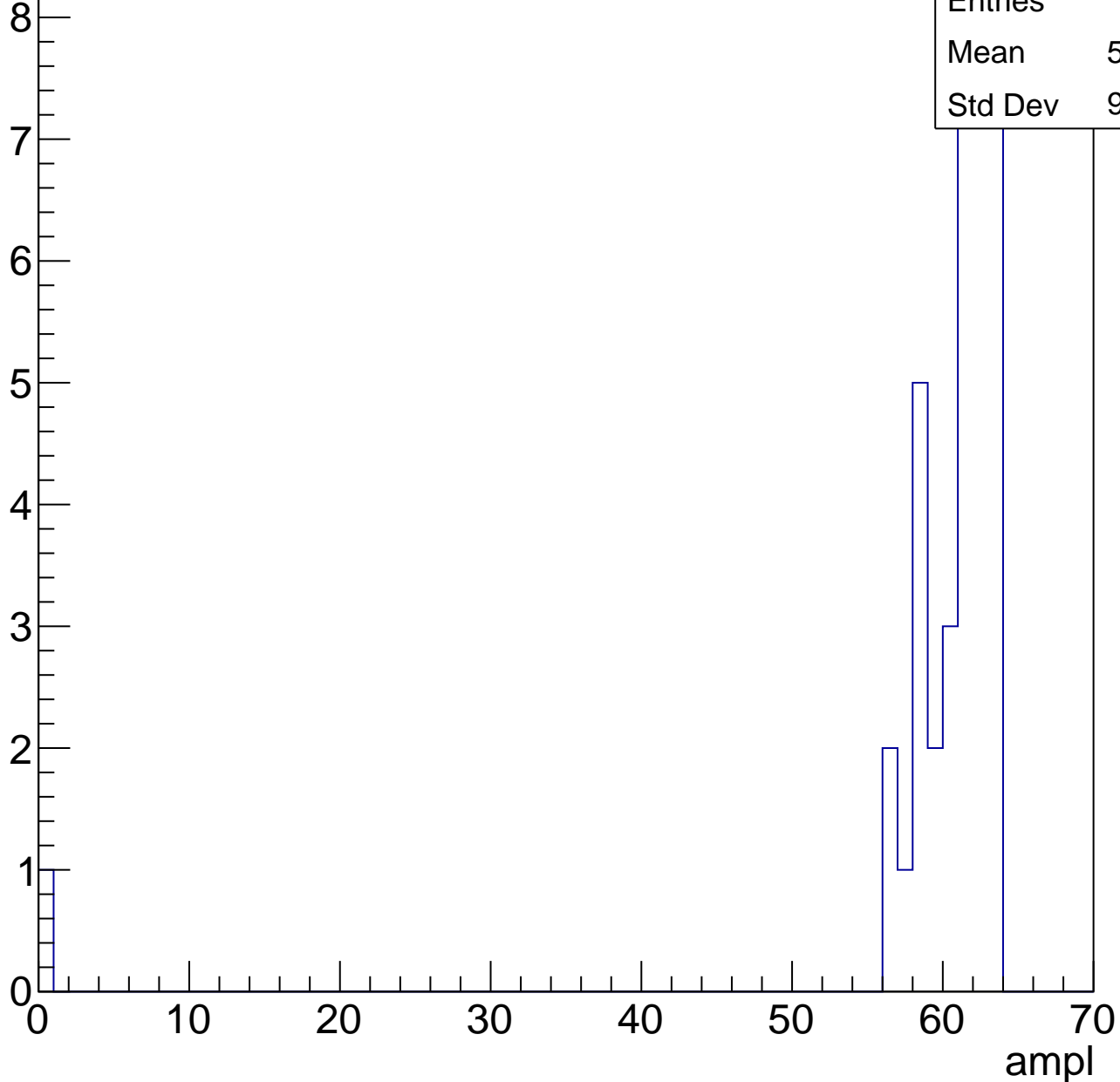


B1L103S, U9-ch1, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	38
Mean	59.08
Std Dev	9.924



B1L103S, U9-ch1, adc6

calib_packv5_041523_1651.root, FC#0, port C2

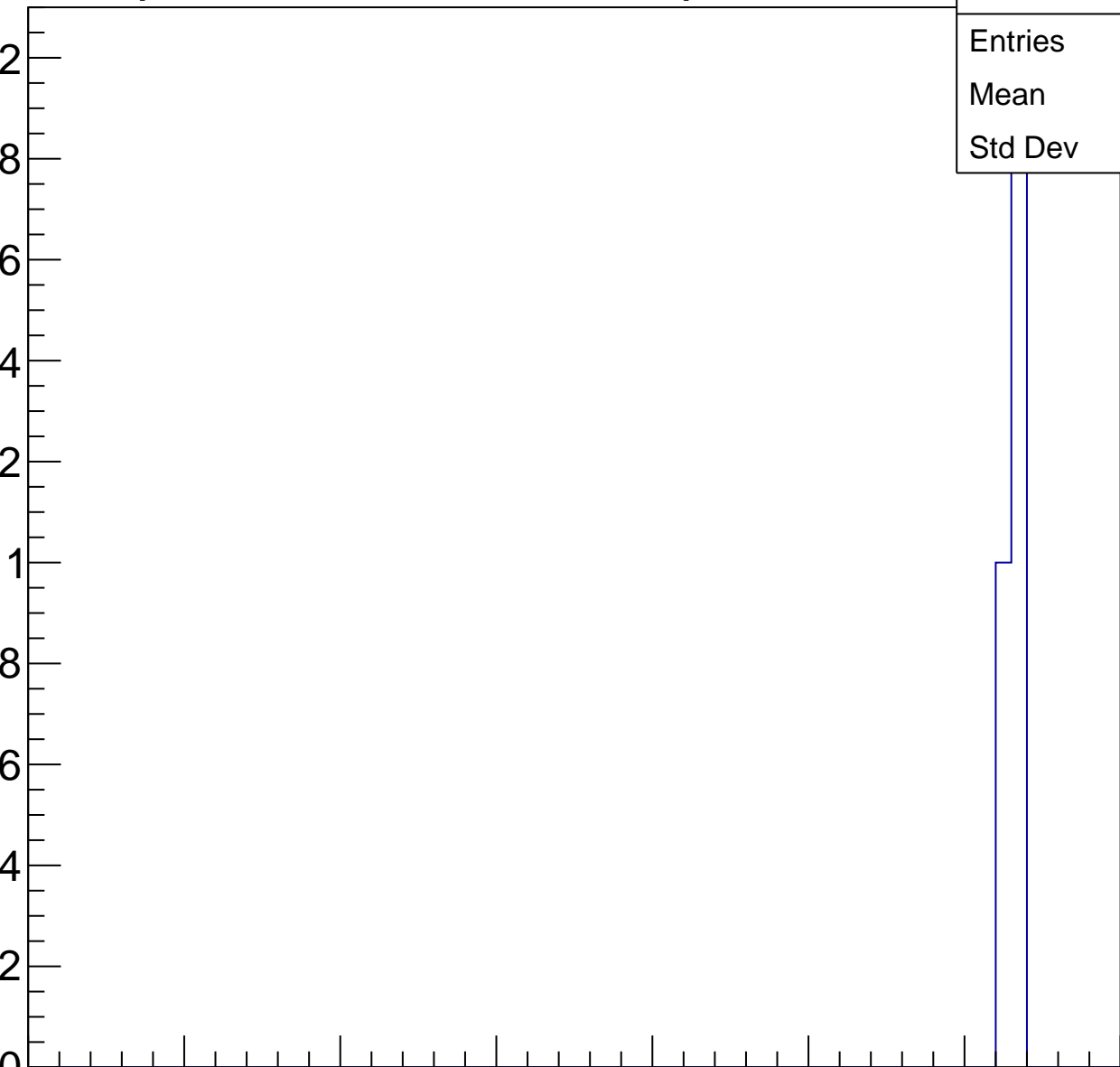
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	3
Mean	62.67
Std Dev	0.4714

0 10 20 30 40 50 60 70

ampl



B1L103S, U9-ch1, adc7

calib_packv5_041523_1651.root, FC#0, port C2

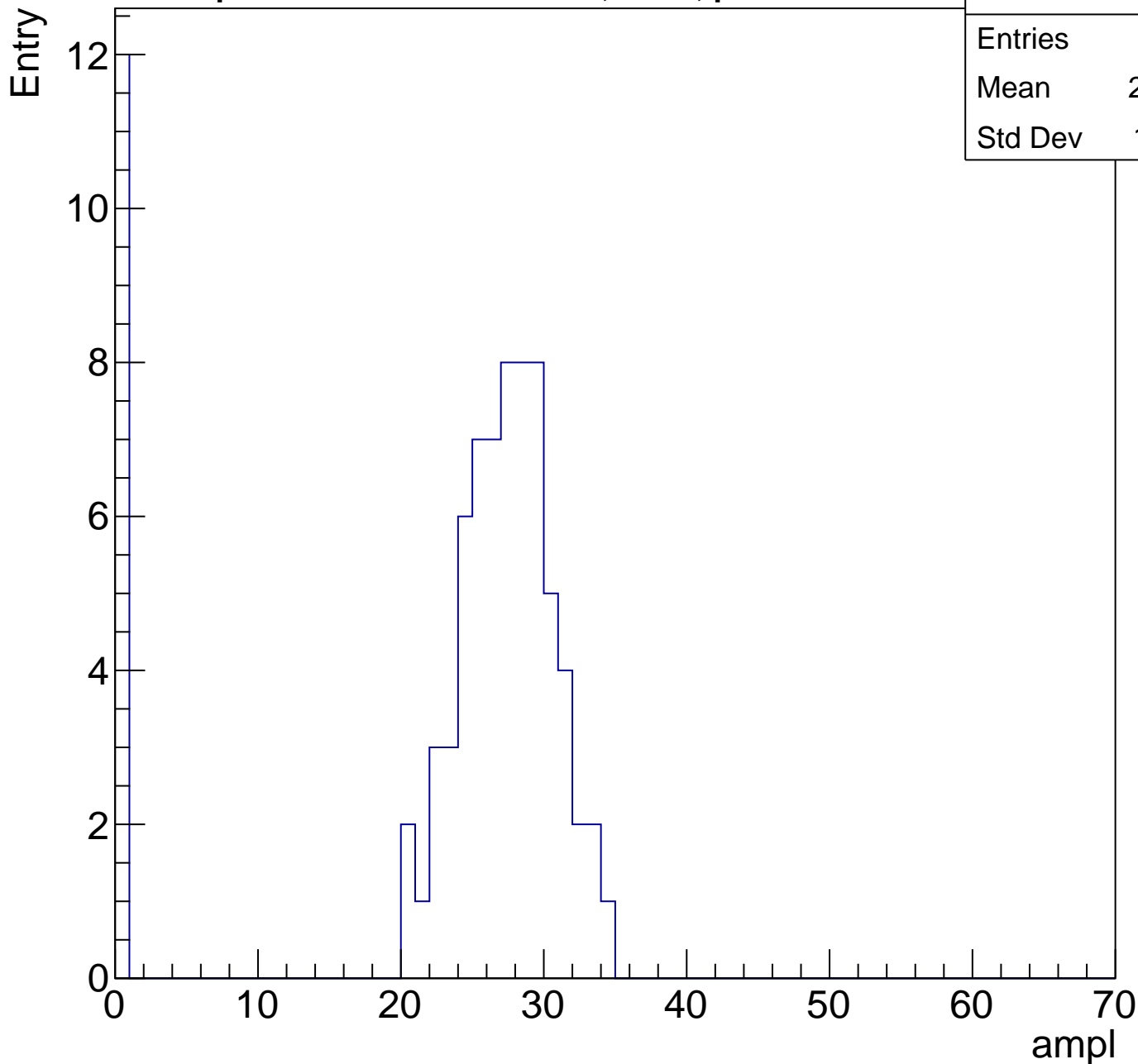
Entries	19
Mean	0
Std Dev	0



B1L103S, U9-ch2, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	79
Mean	22.87
Std Dev	10.11

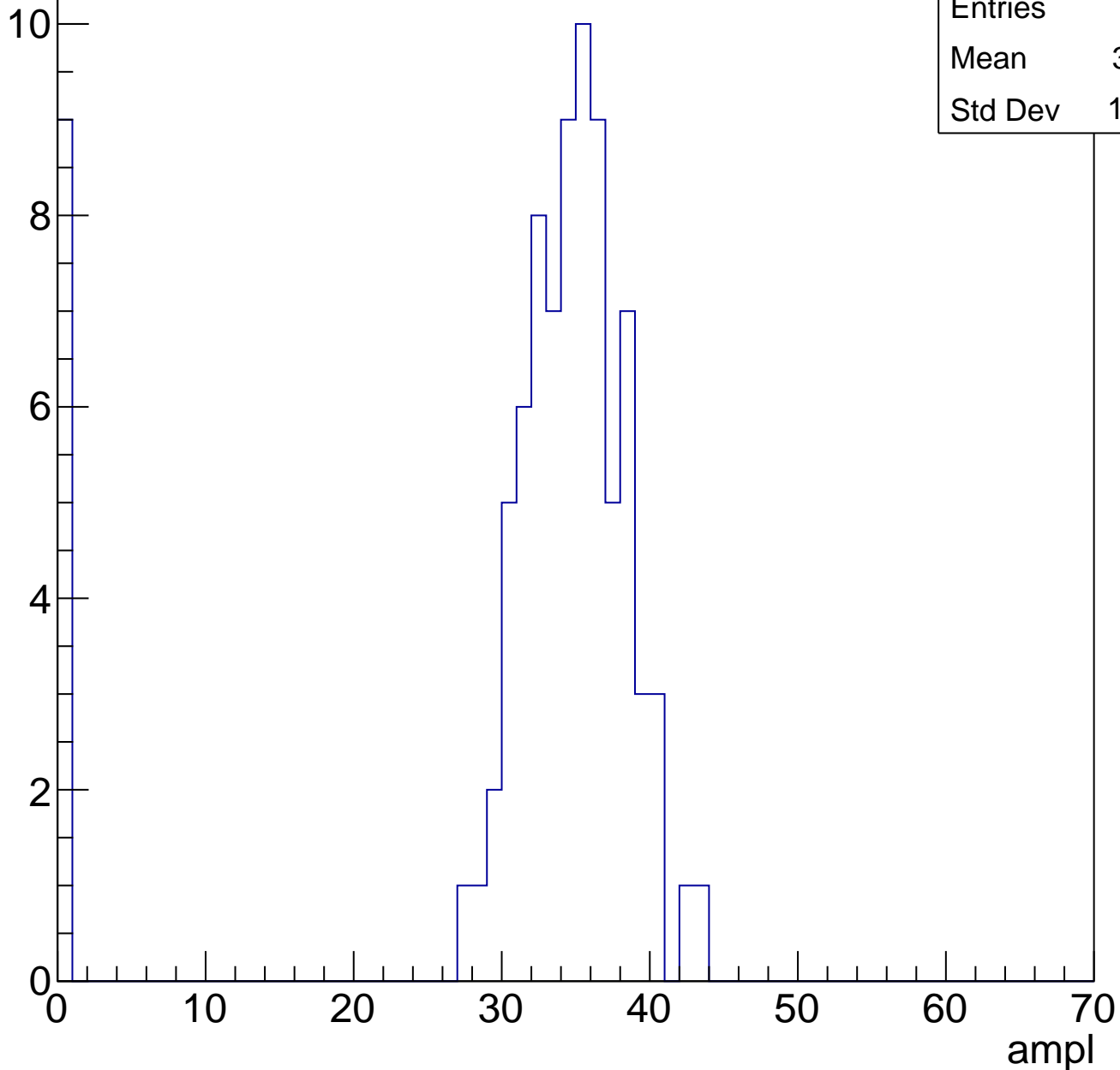


B1L103S, U9-ch2, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	87
Mean	30.91
Std Dev	10.94

Entry

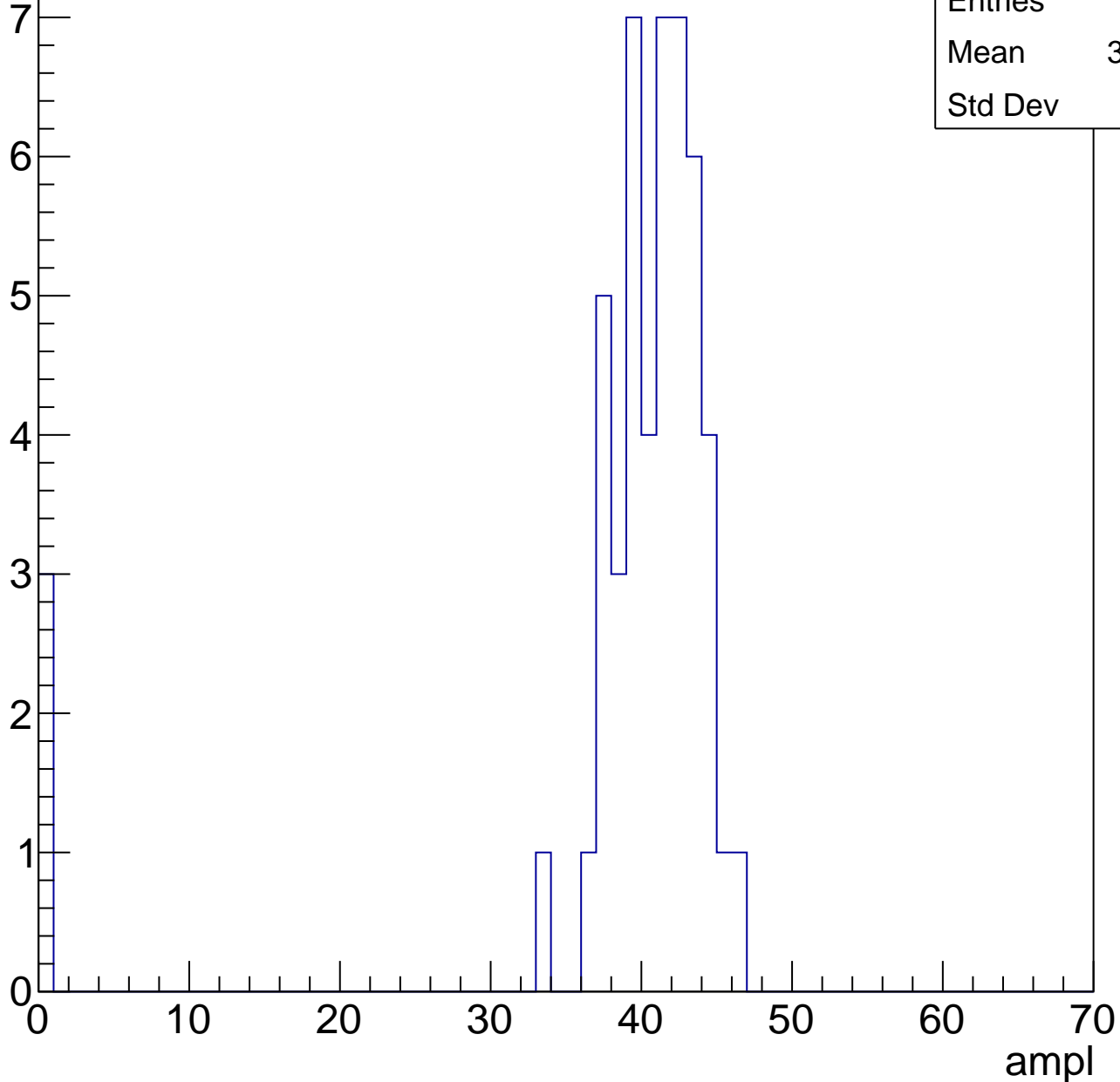


B1L103S, U9-ch2, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

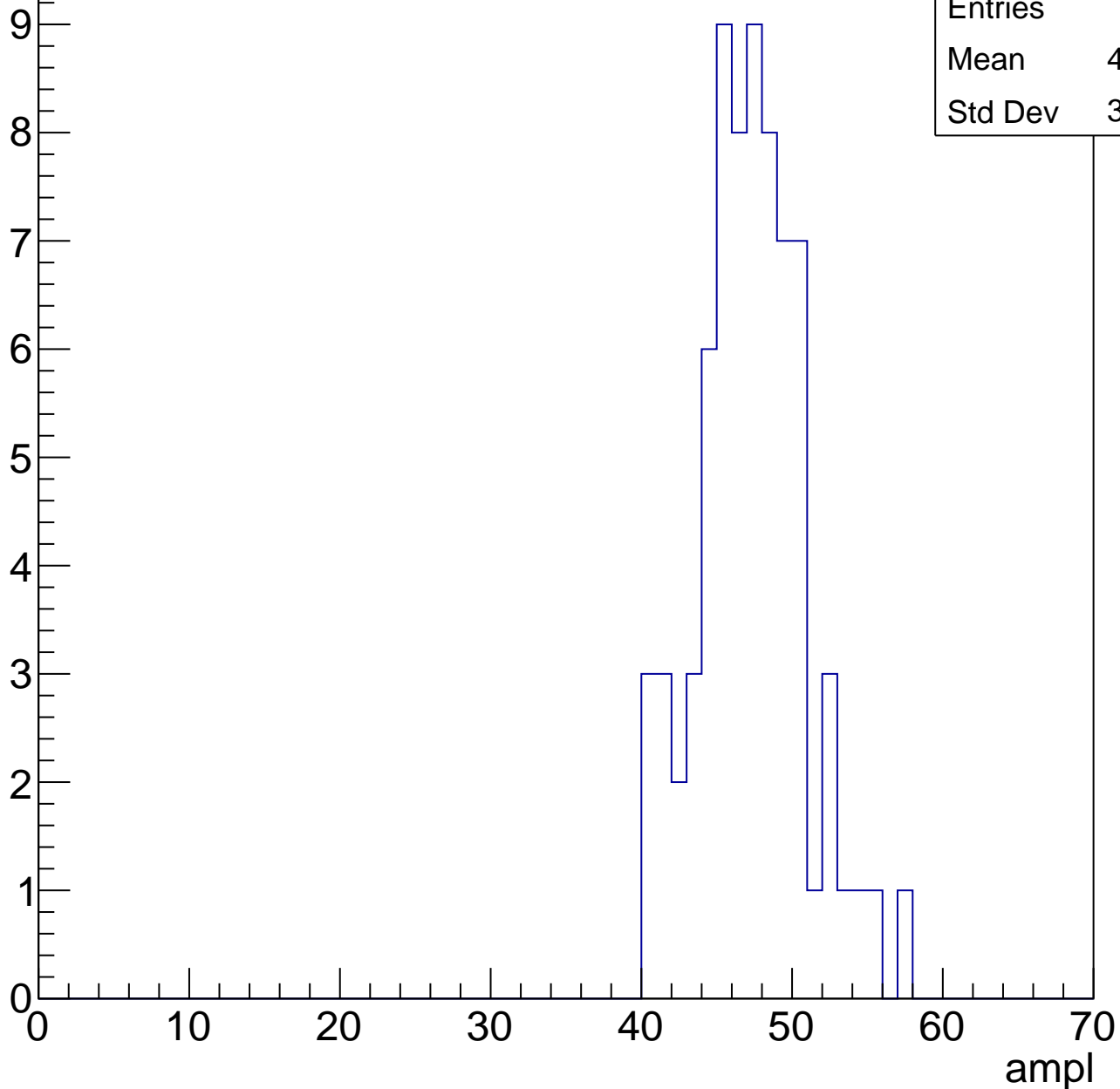
Entries	50
Mean	38.14
Std Dev	9.97



B1L103S, U9-ch2, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry



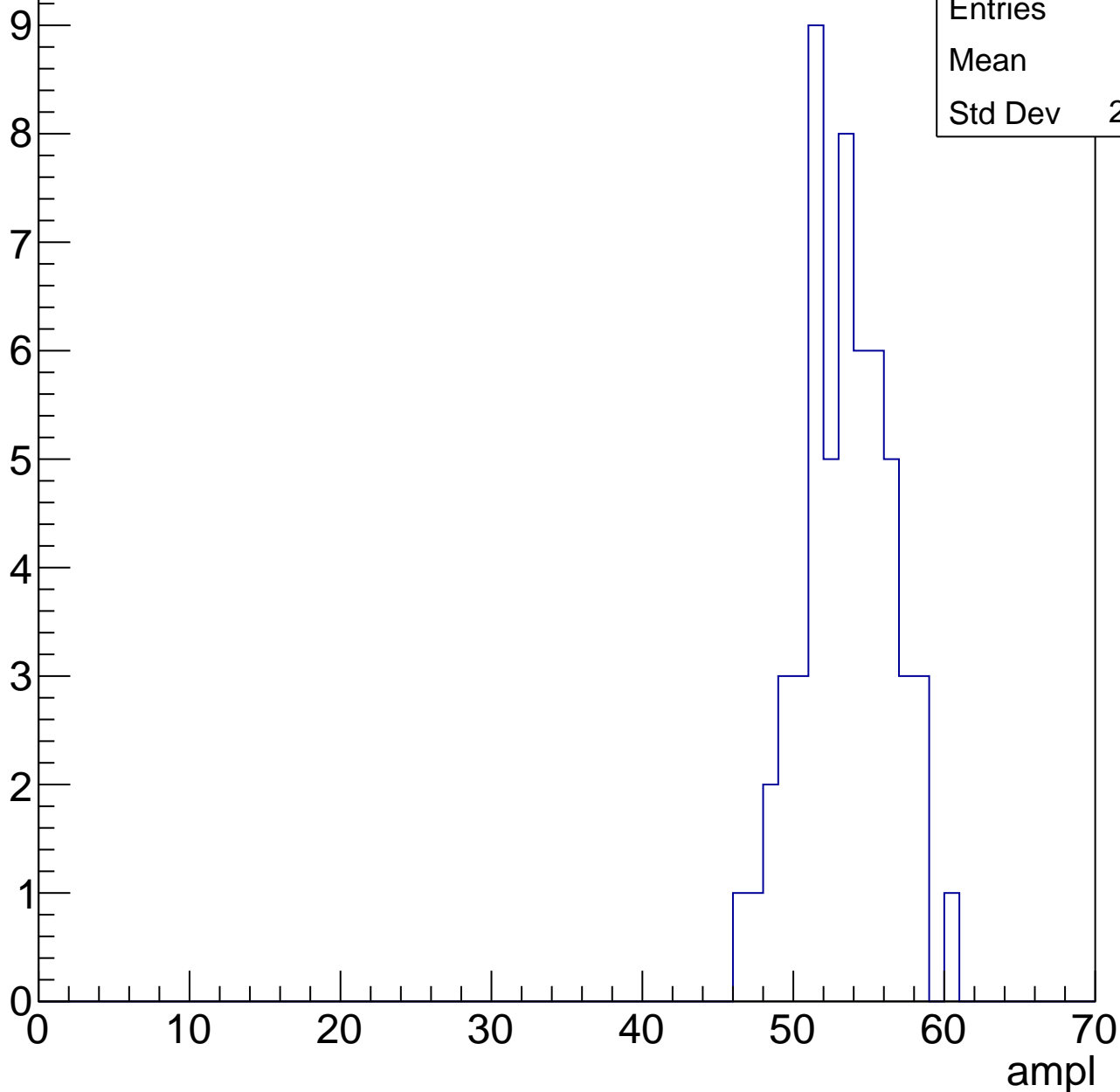
Entries	73
Mean	46.84
Std Dev	3.488

B1L103S, U9-ch2, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

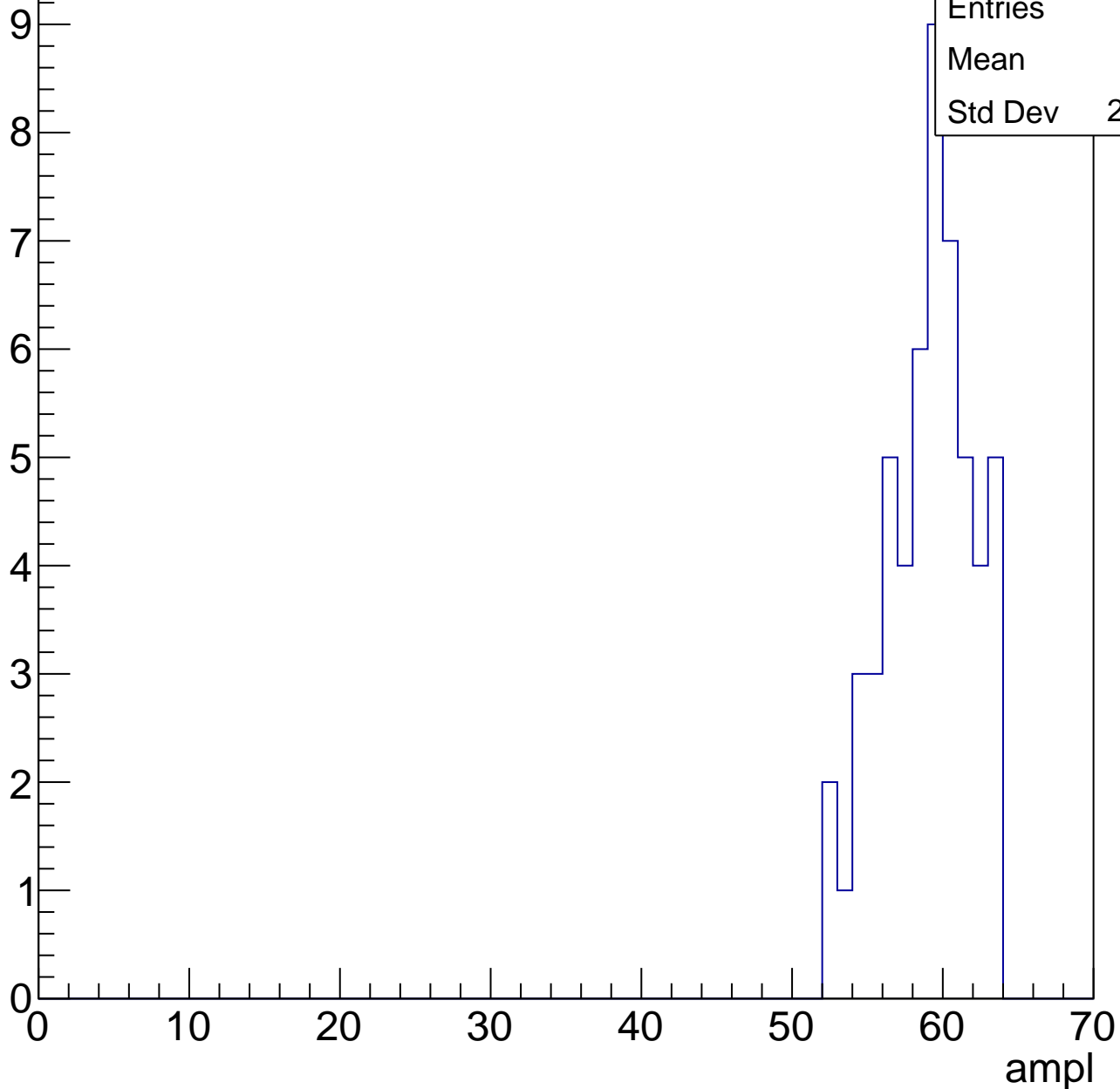
Entries	56
Mean	53
Std Dev	2.982



B1L103S, U9-ch2, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



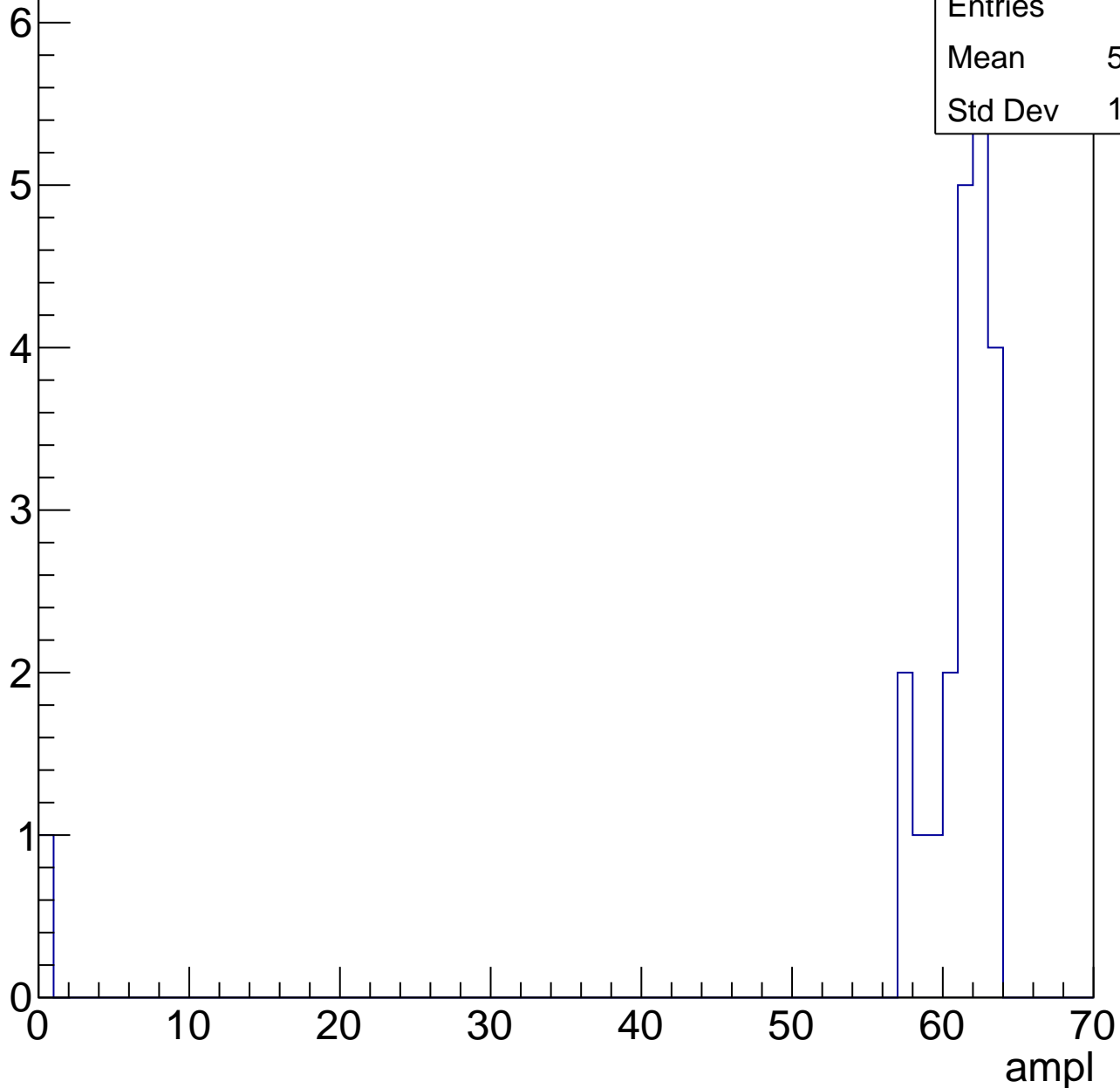
Entries	54
Mean	58.5
Std Dev	2.898

B1L103S, U9-ch2, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

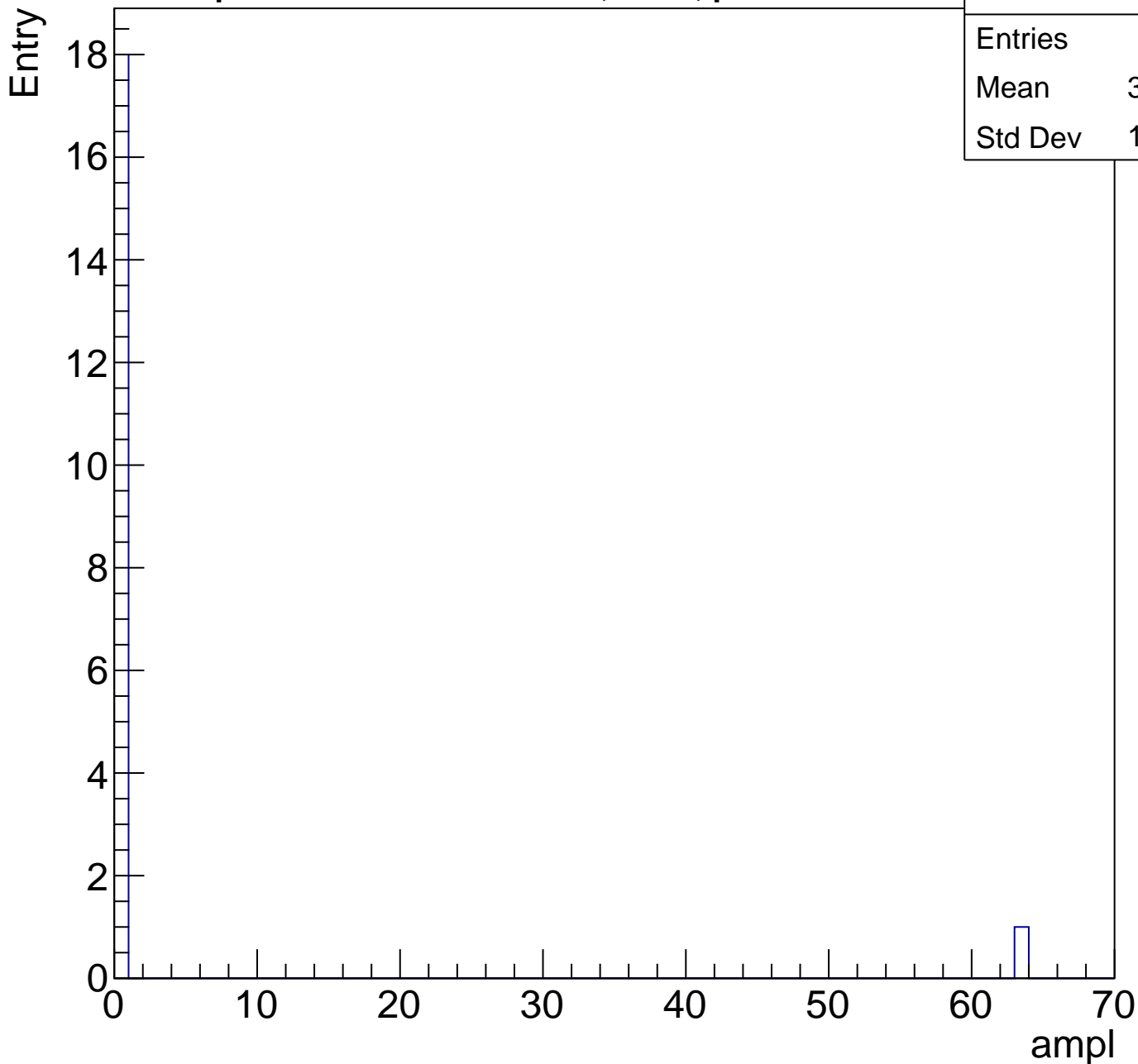
Entries	22
Mean	58.18
Std Dev	12.82



B1L103S, U9-ch2, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	3.316
Std Dev	14.07

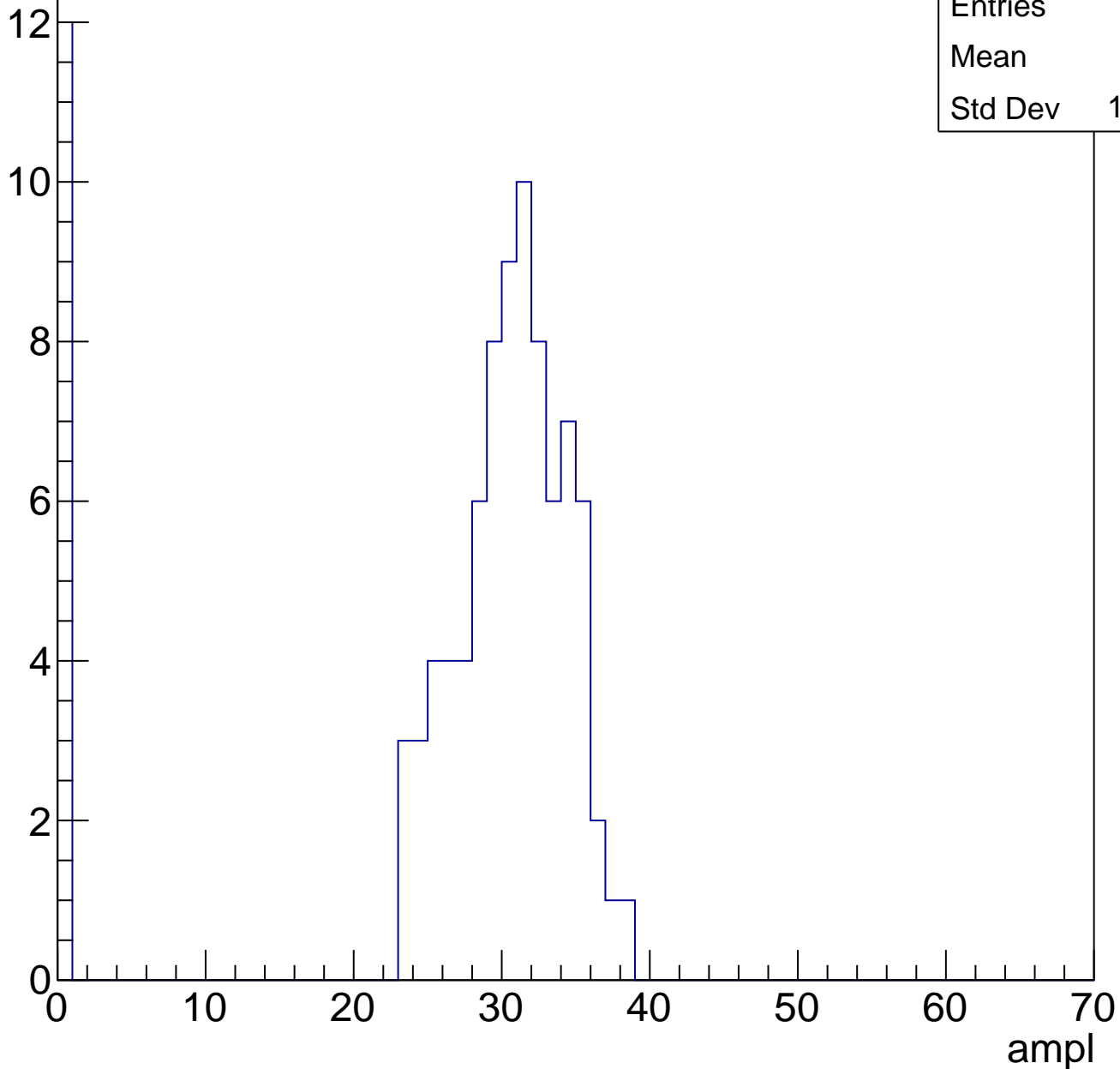


B1L103S, U9-ch3, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	94
Mean	26.4
Std Dev	10.63

Entry

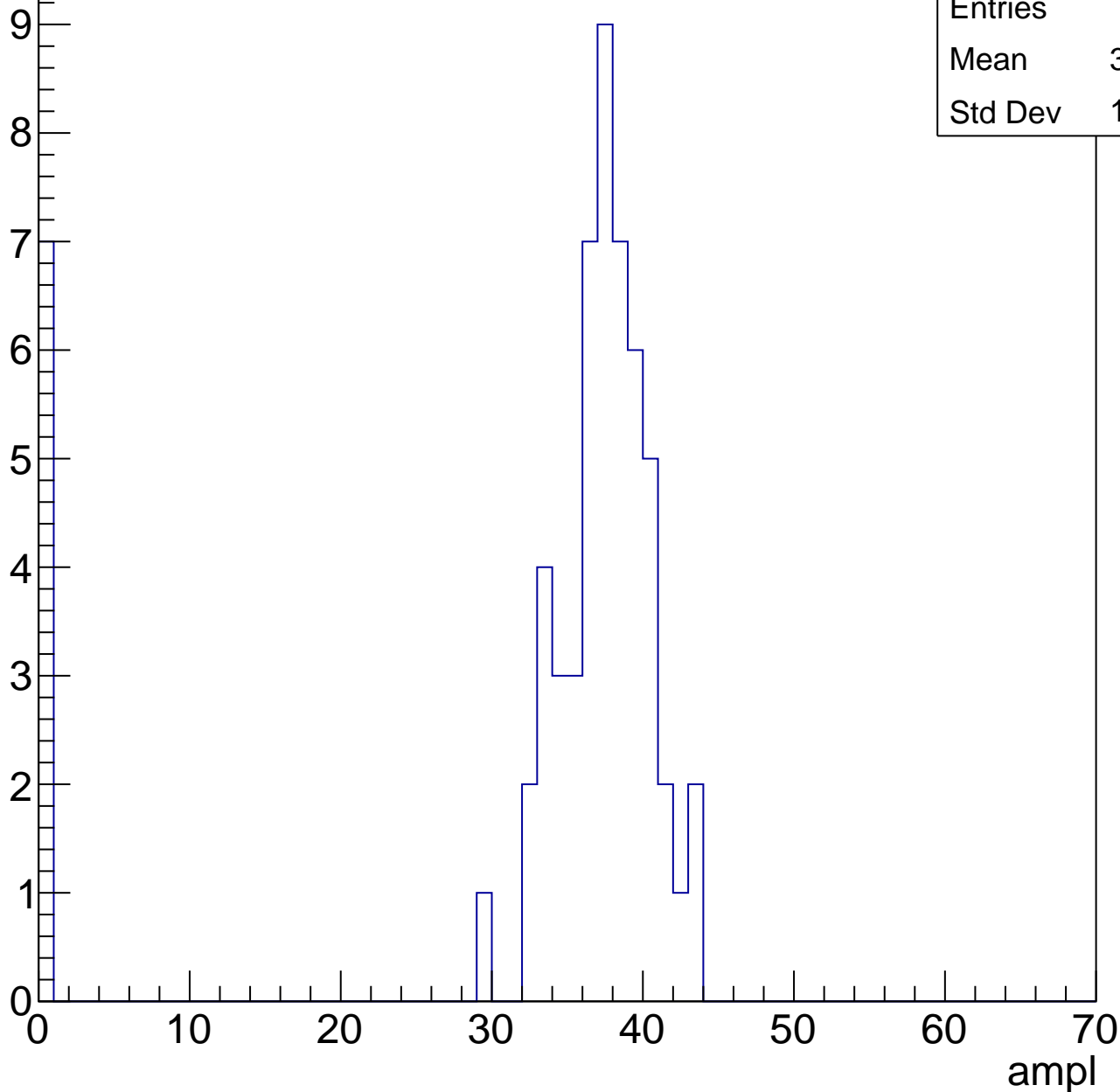


B1L103S, U9-ch3, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	32.66
Std Dev	12.28

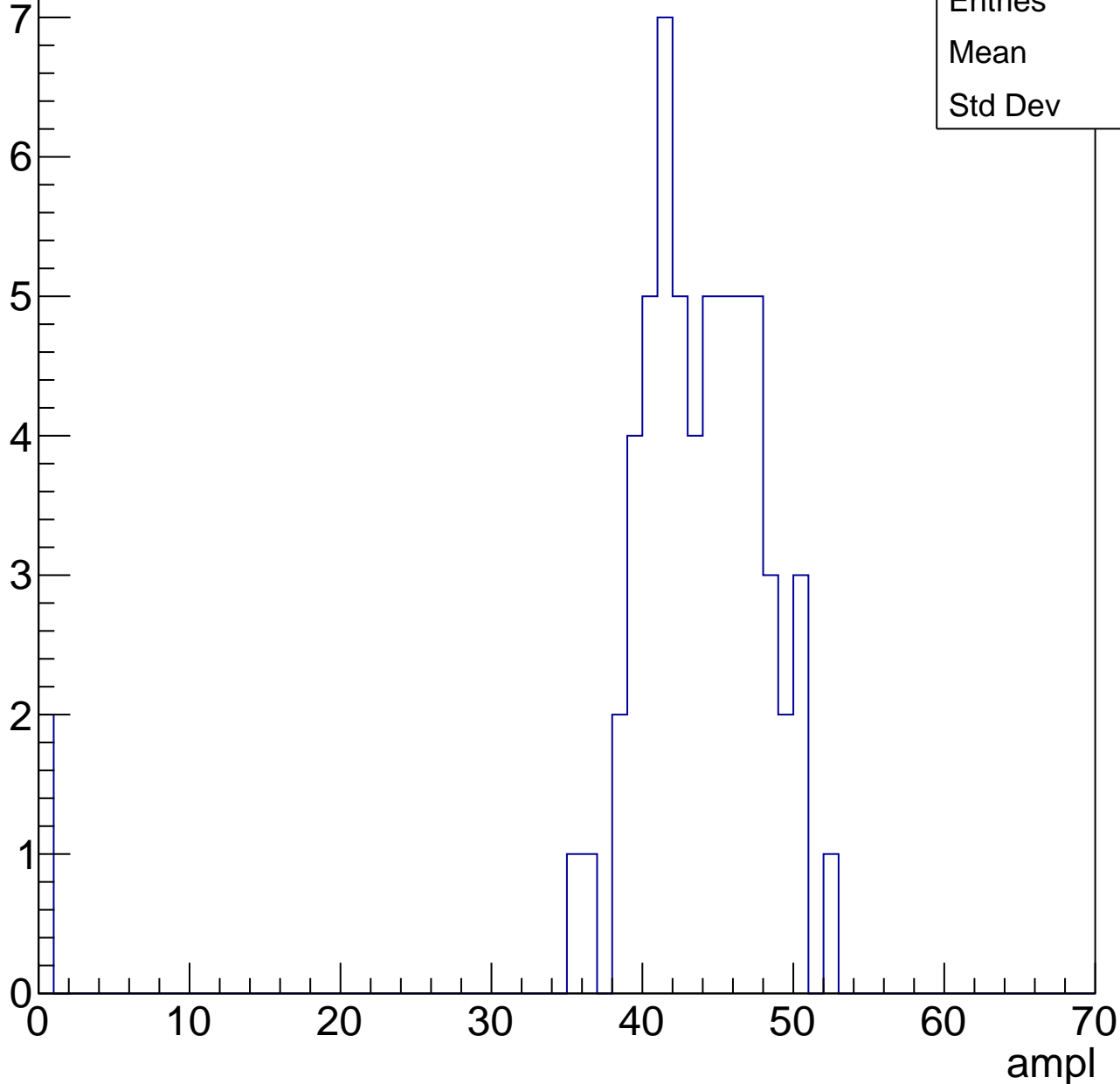


B1L103S, U9-ch3, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	42.1
Std Dev	8.64

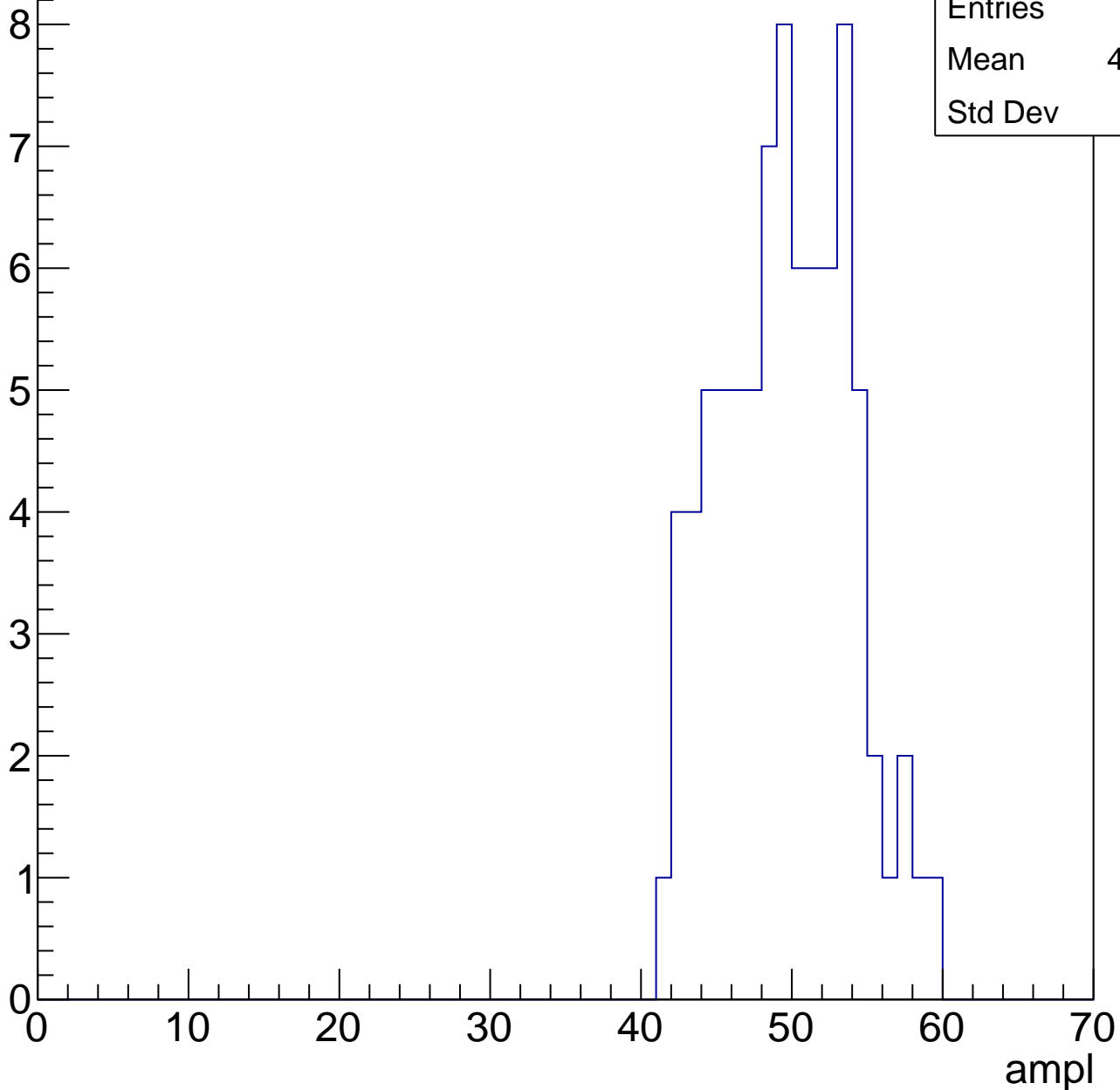


B1L103S, U9-ch3, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	82
Mean	49.12
Std Dev	4.2

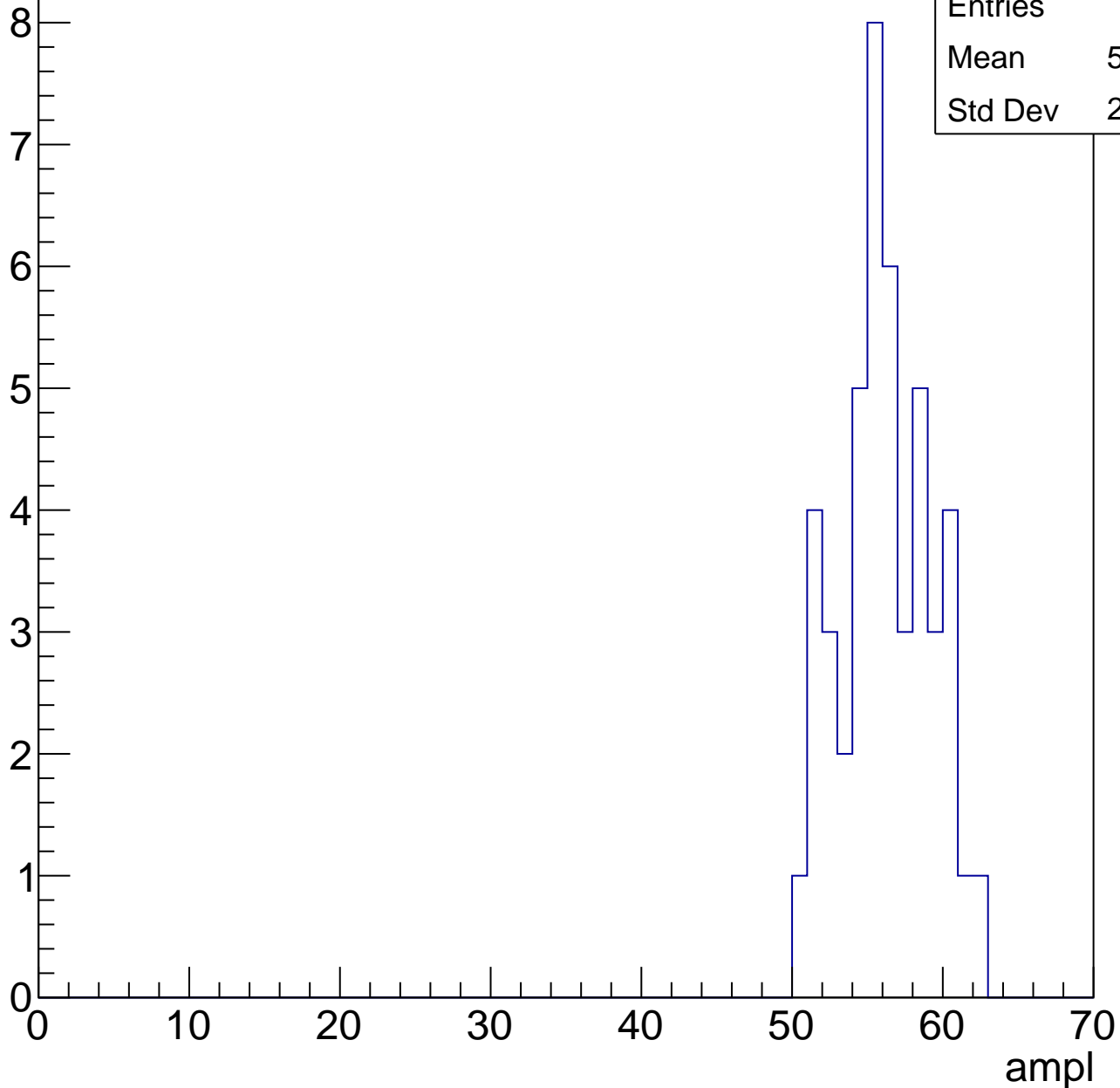


B1L103S, U9-ch3, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	46
Mean	55.72
Std Dev	2.954

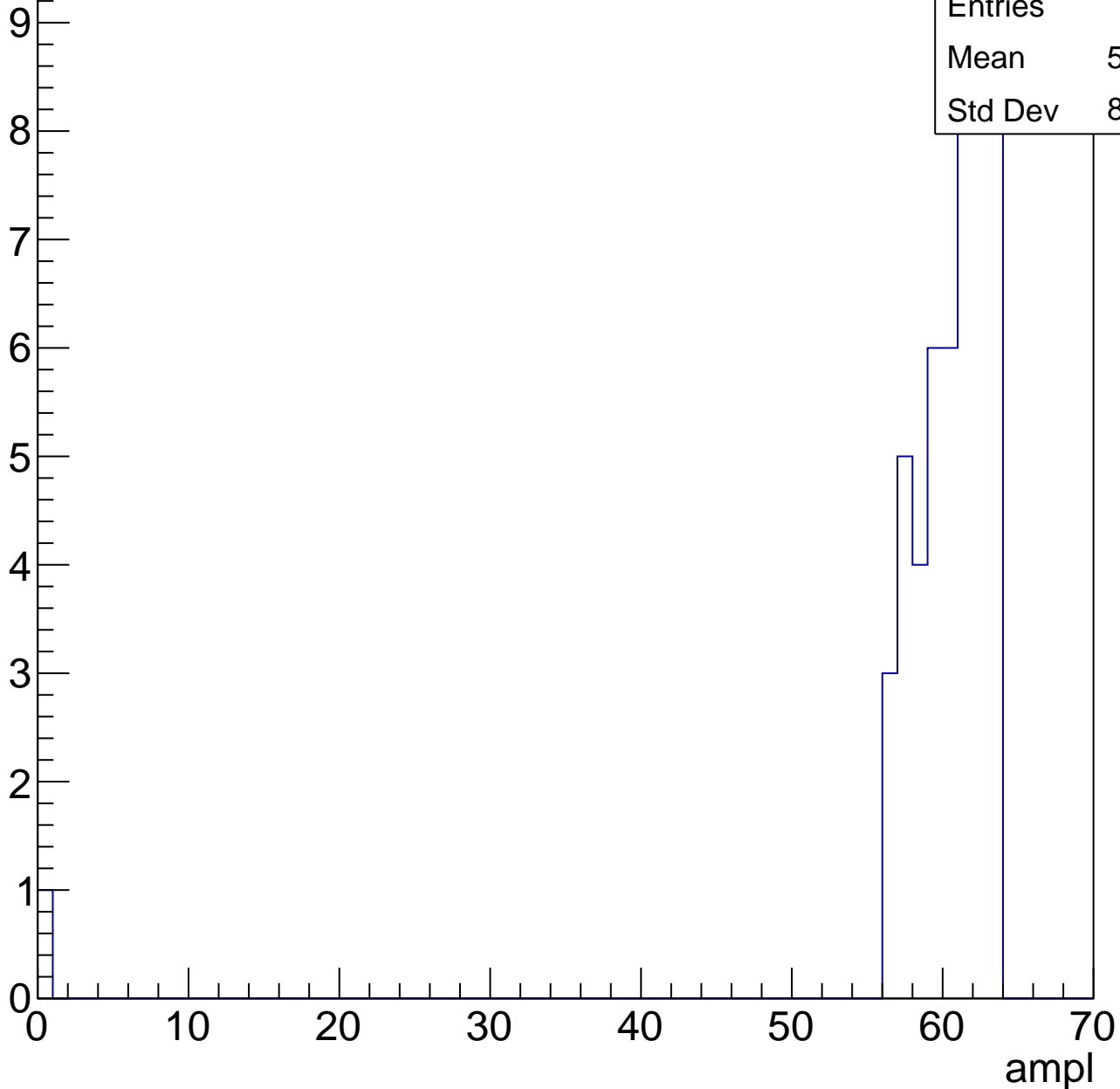


B1L103S, U9-ch3, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	58.96
Std Dev	8.688



B1L103S, U9-ch3, adc6

calib_packv5_041523_1651.root, FC#0, port C2

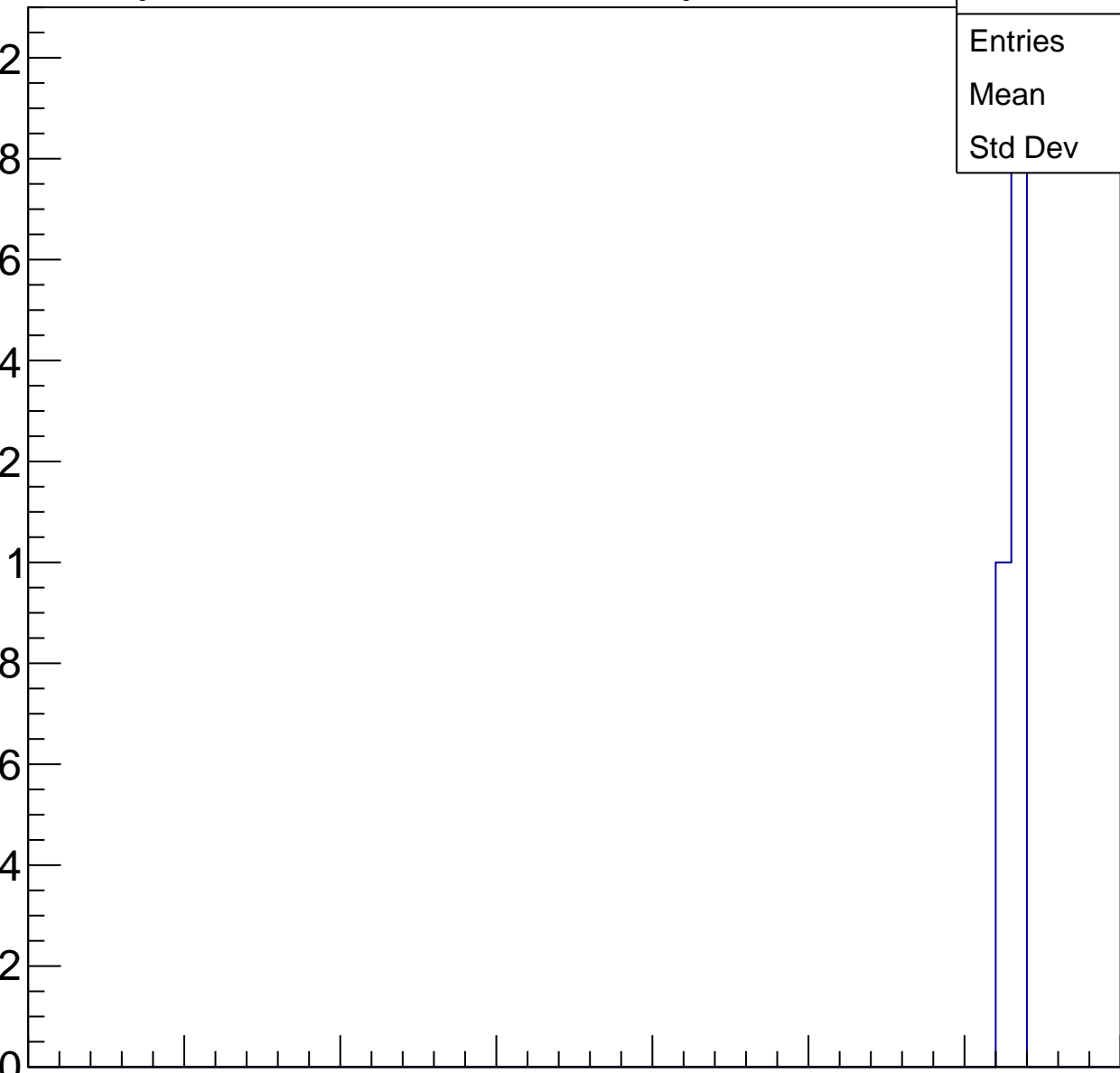
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	3
Mean	62.67
Std Dev	0.4714

0 10 20 30 40 50 60 70

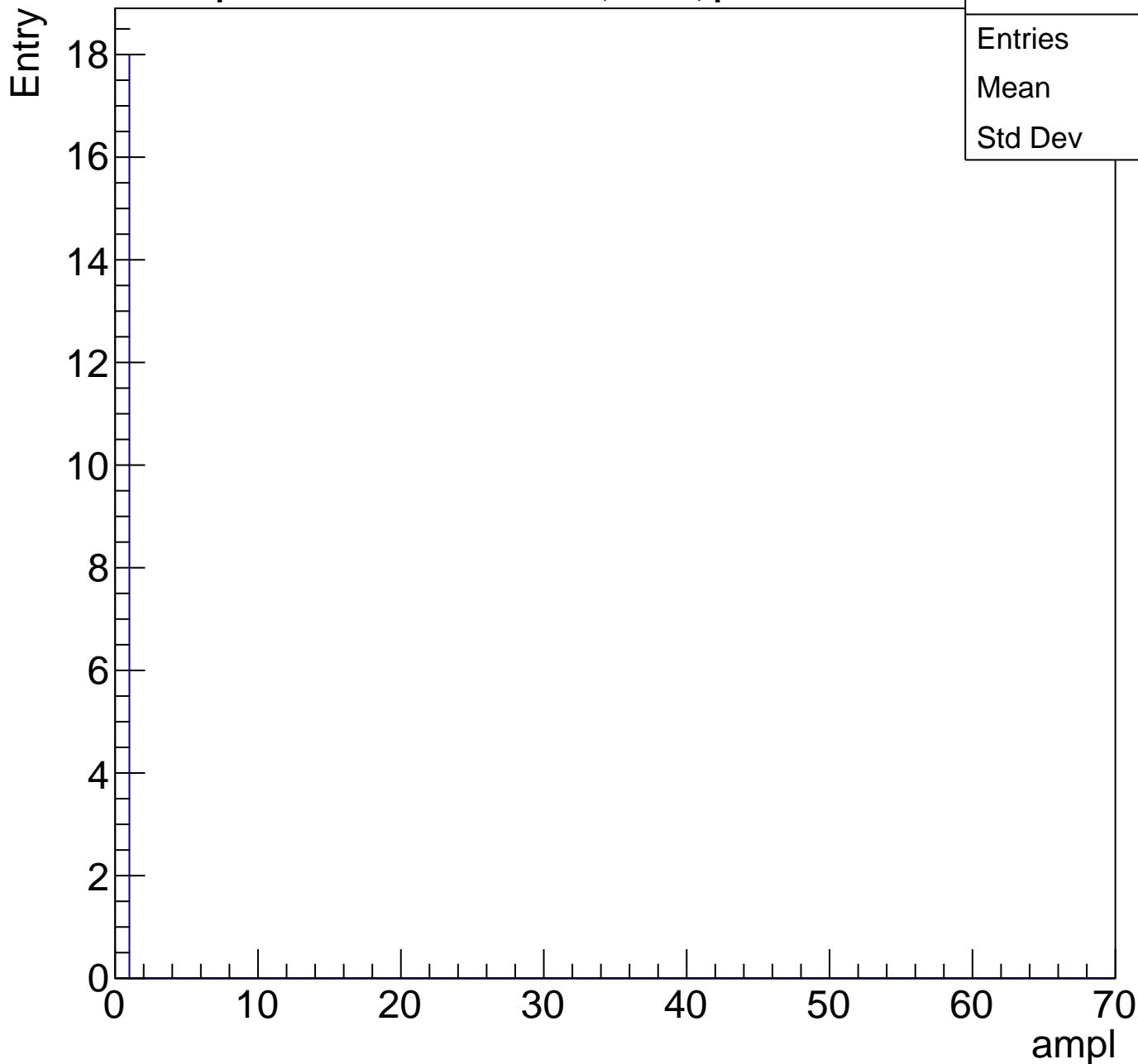
ampl



B1L103S, U9-ch3, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	18
Mean	0
Std Dev	0

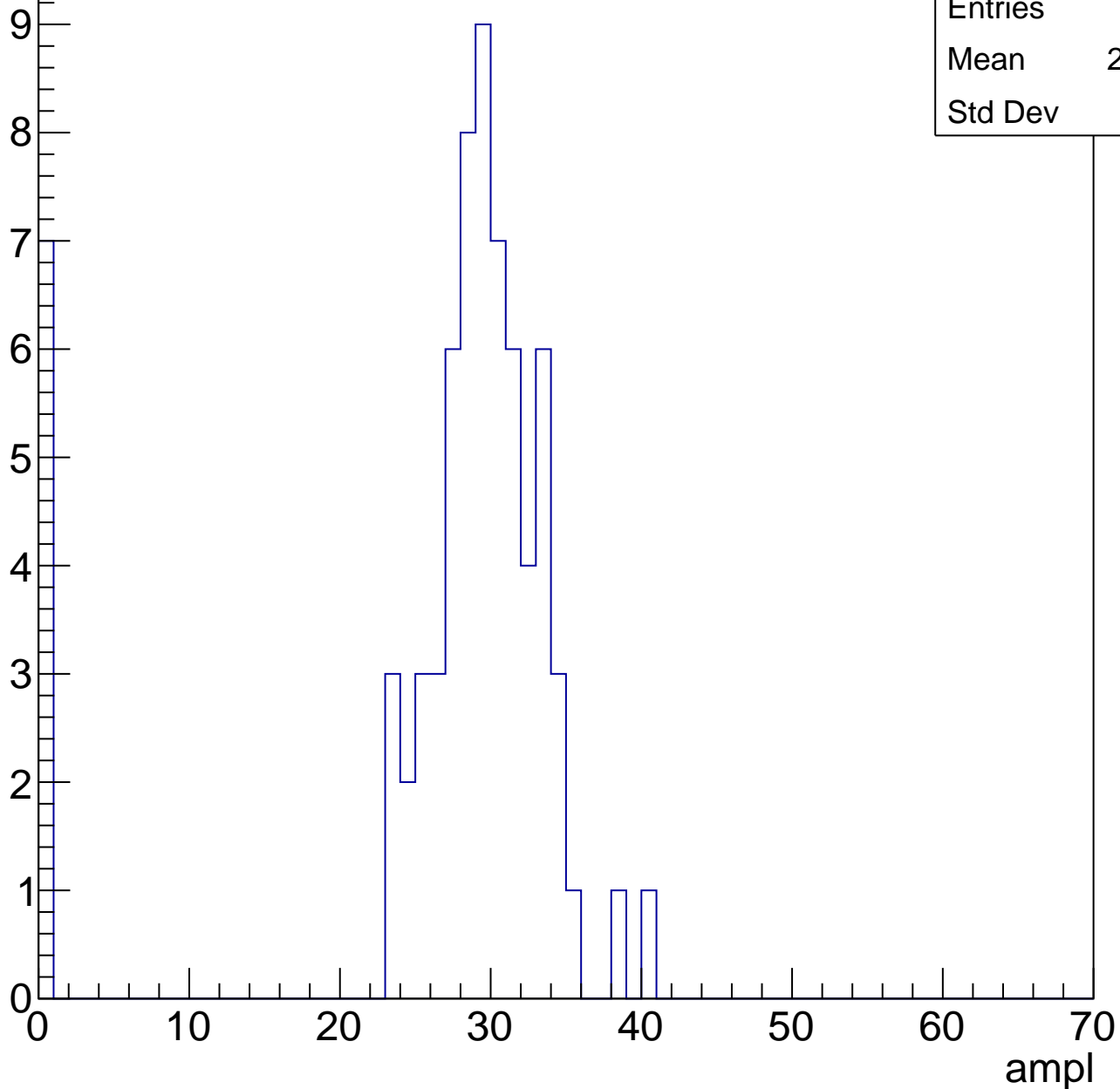


B1L103S, U9-ch4, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	26.49
Std Dev	9.4

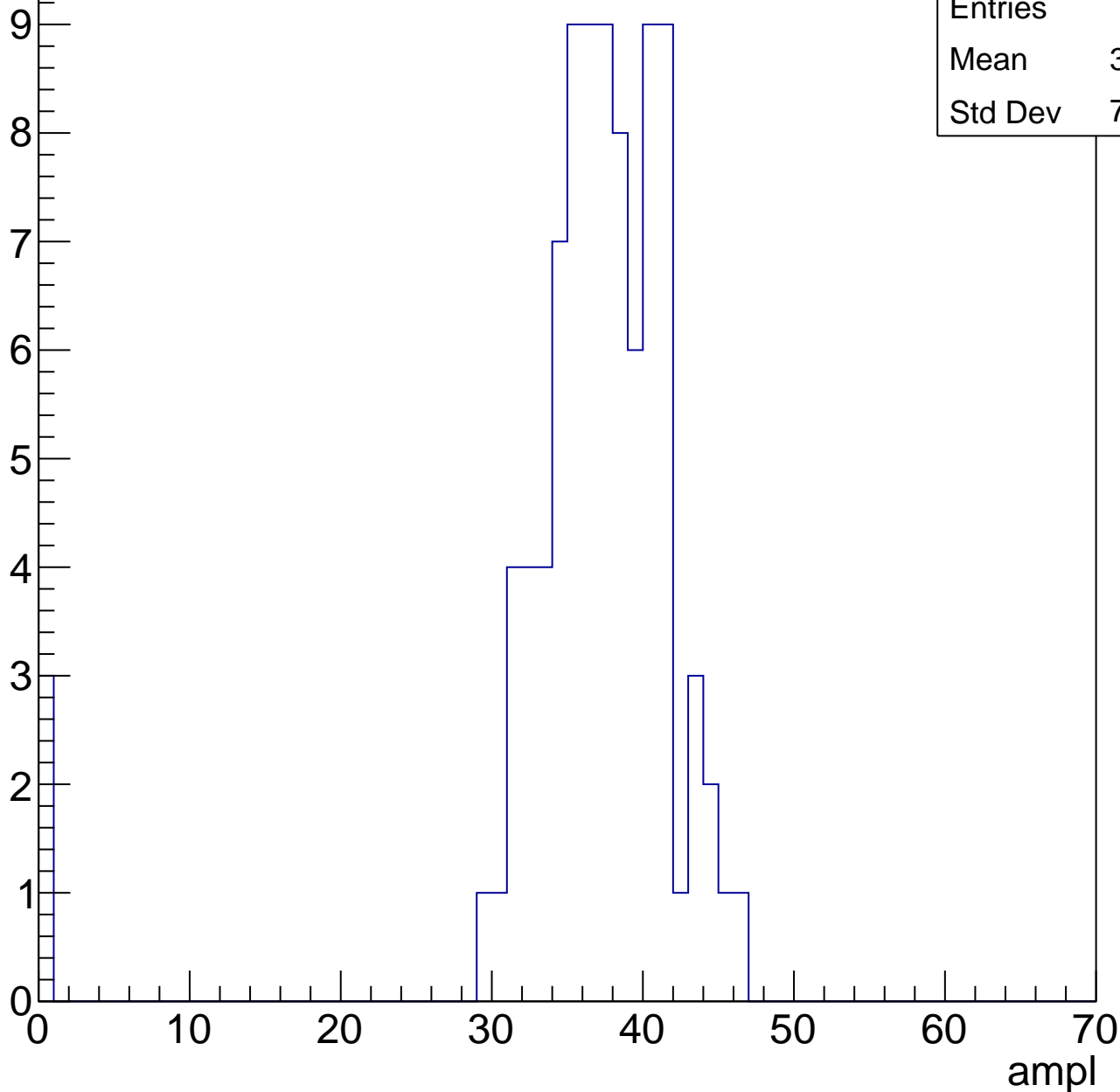


B1L103S, U9-ch4, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

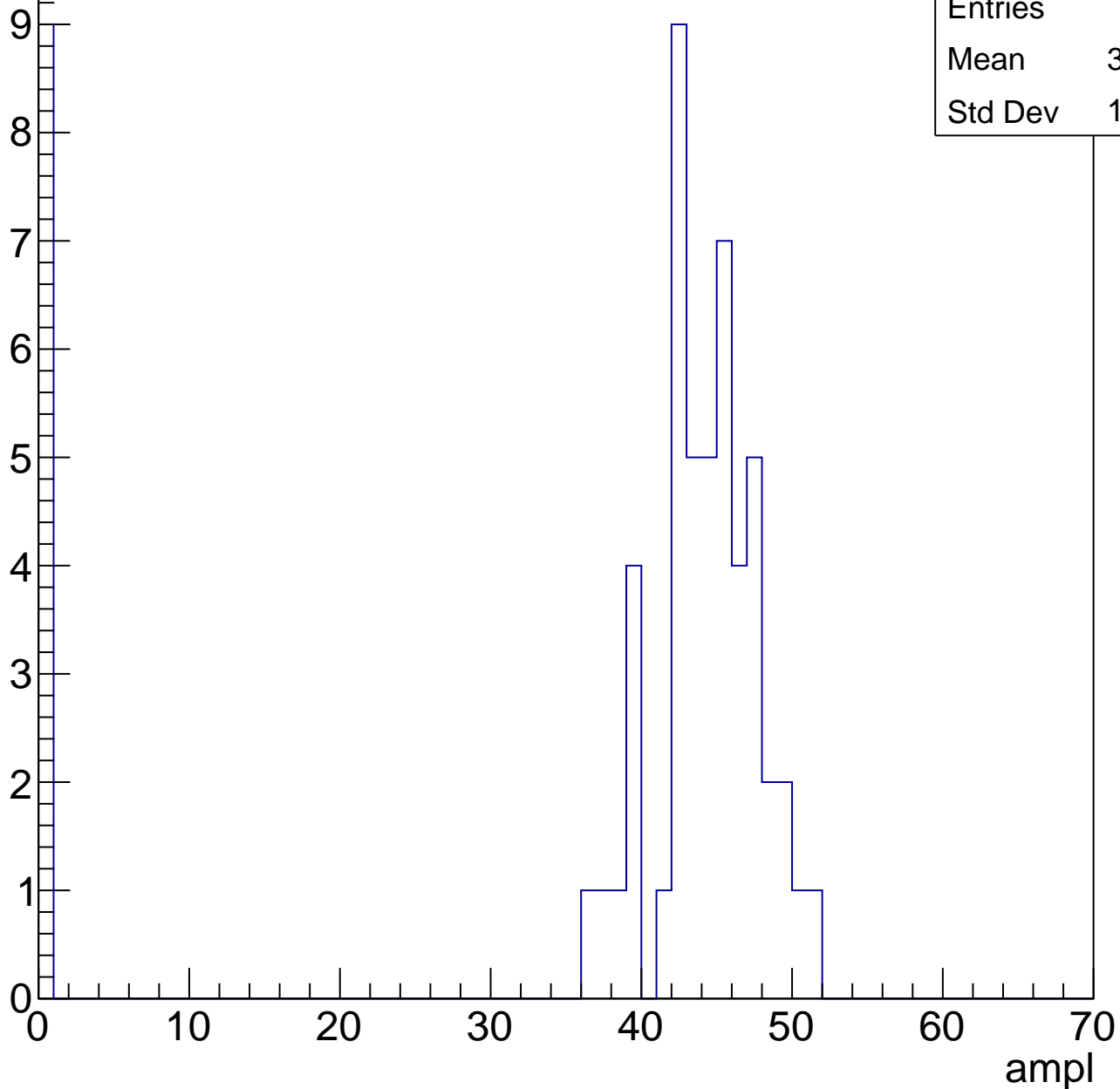
Entries	91
Mean	35.93
Std Dev	7.534



B1L103S, U9-ch4, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

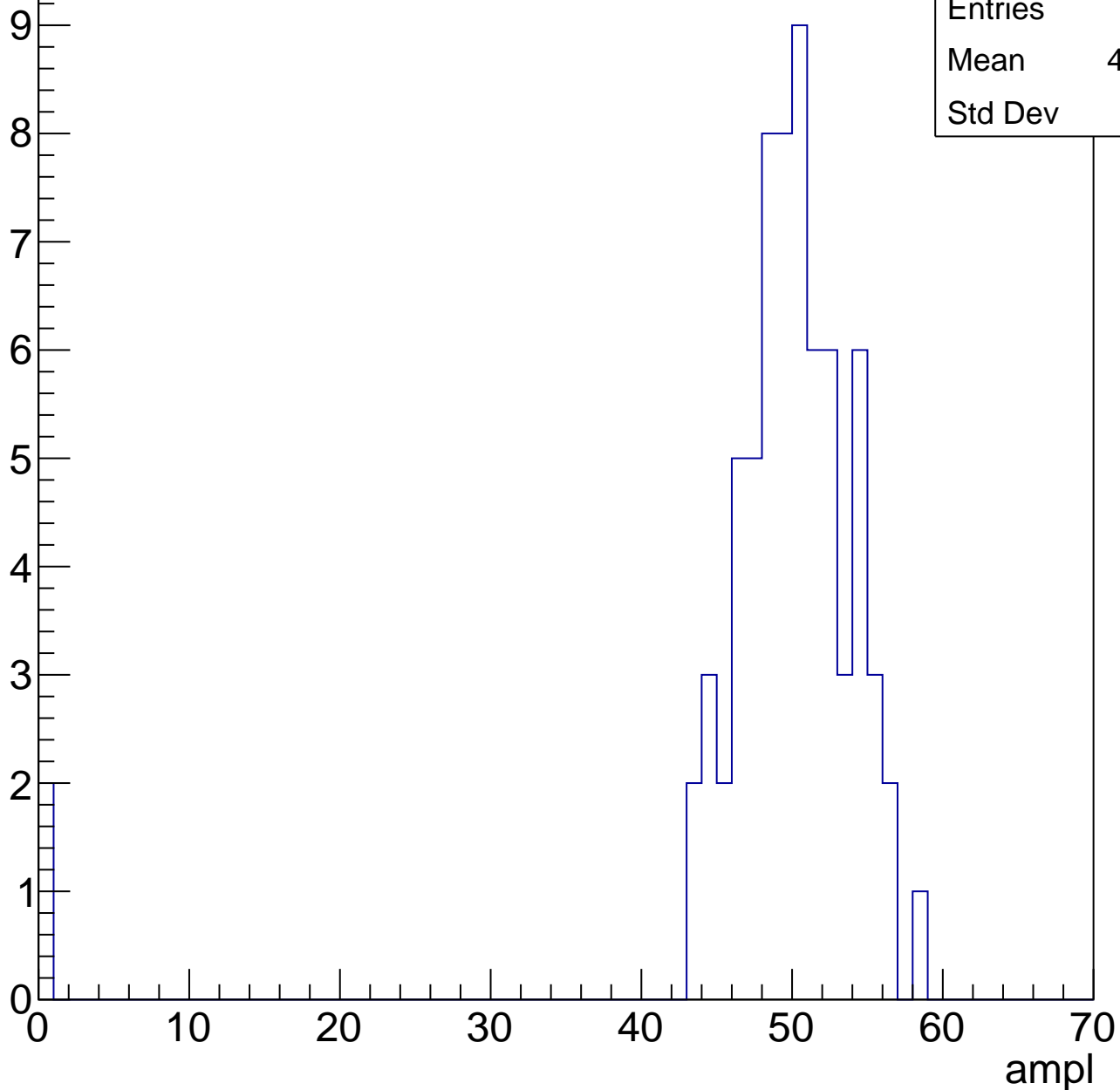


Entries	58
Mean	37.07
Std Dev	16.17

B1L103S, U9-ch4, adc3

calib_packv5_041523_1651.root, FC#0, port C2

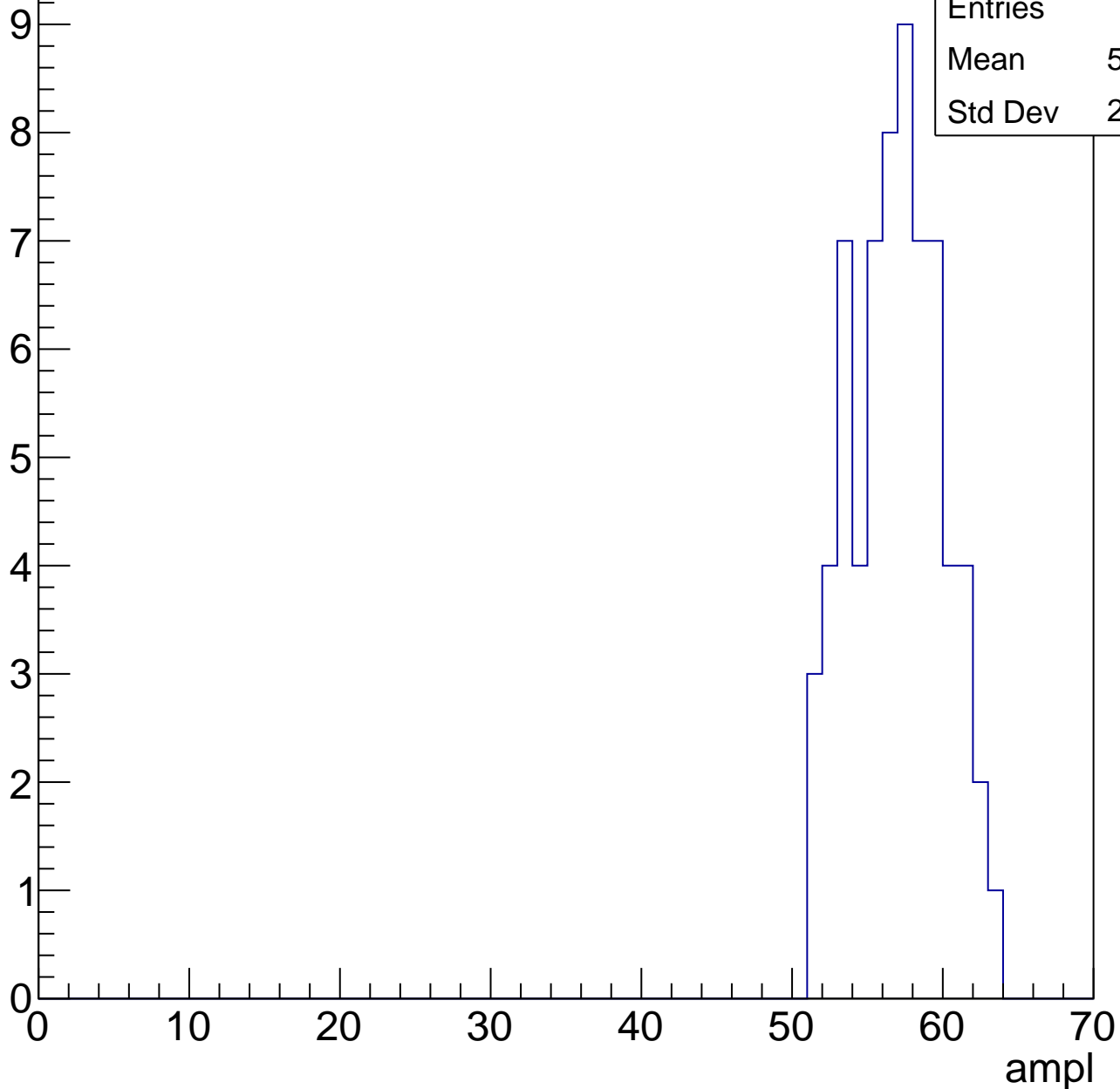
Entry



B1L103S, U9-ch4, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



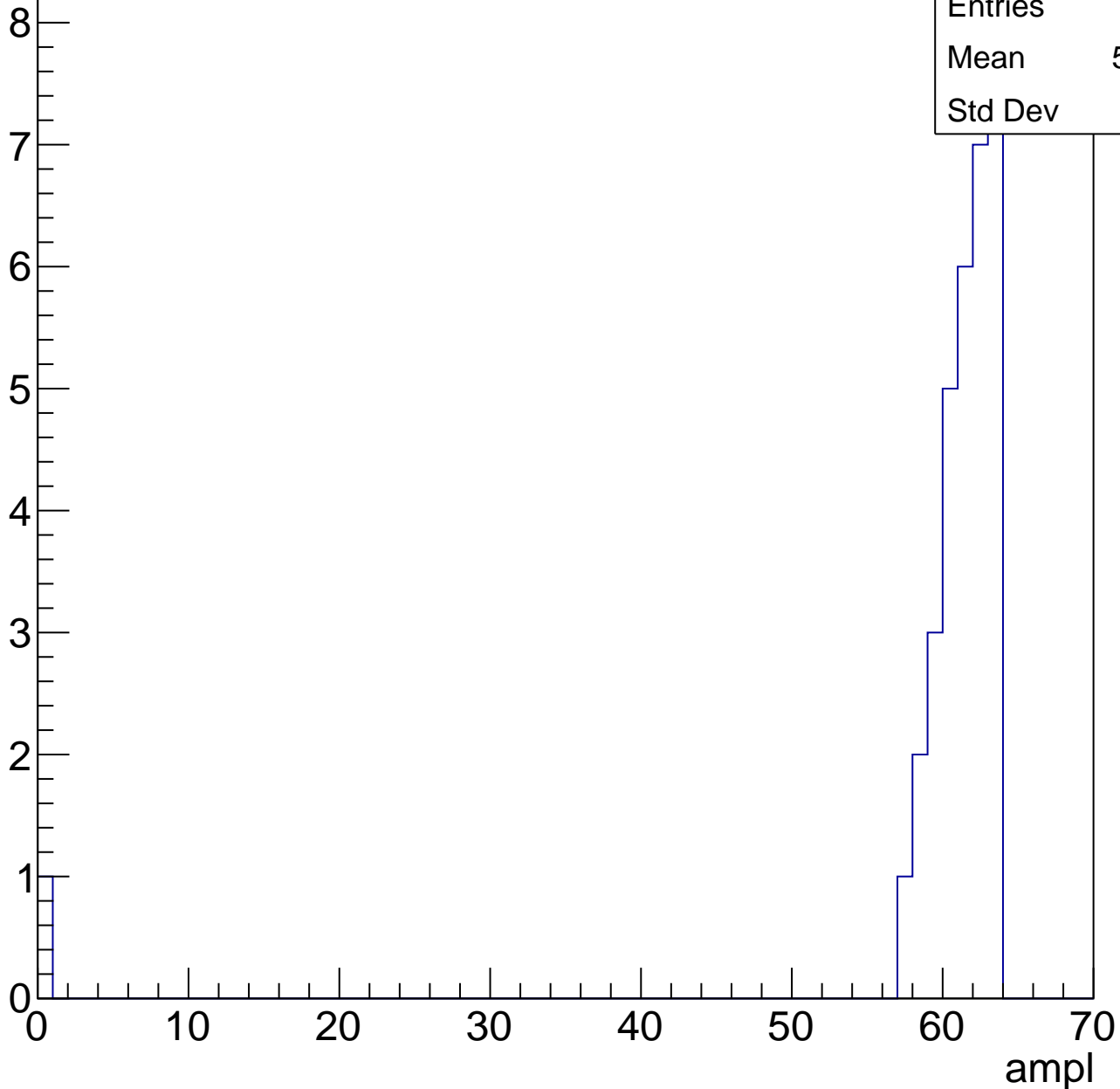
Entries	67
Mean	56.48
Std Dev	2.979

B1L103S, U9-ch4, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	33
Mean	59.21
Std Dev	10.6



B1L103S, U9-ch4, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

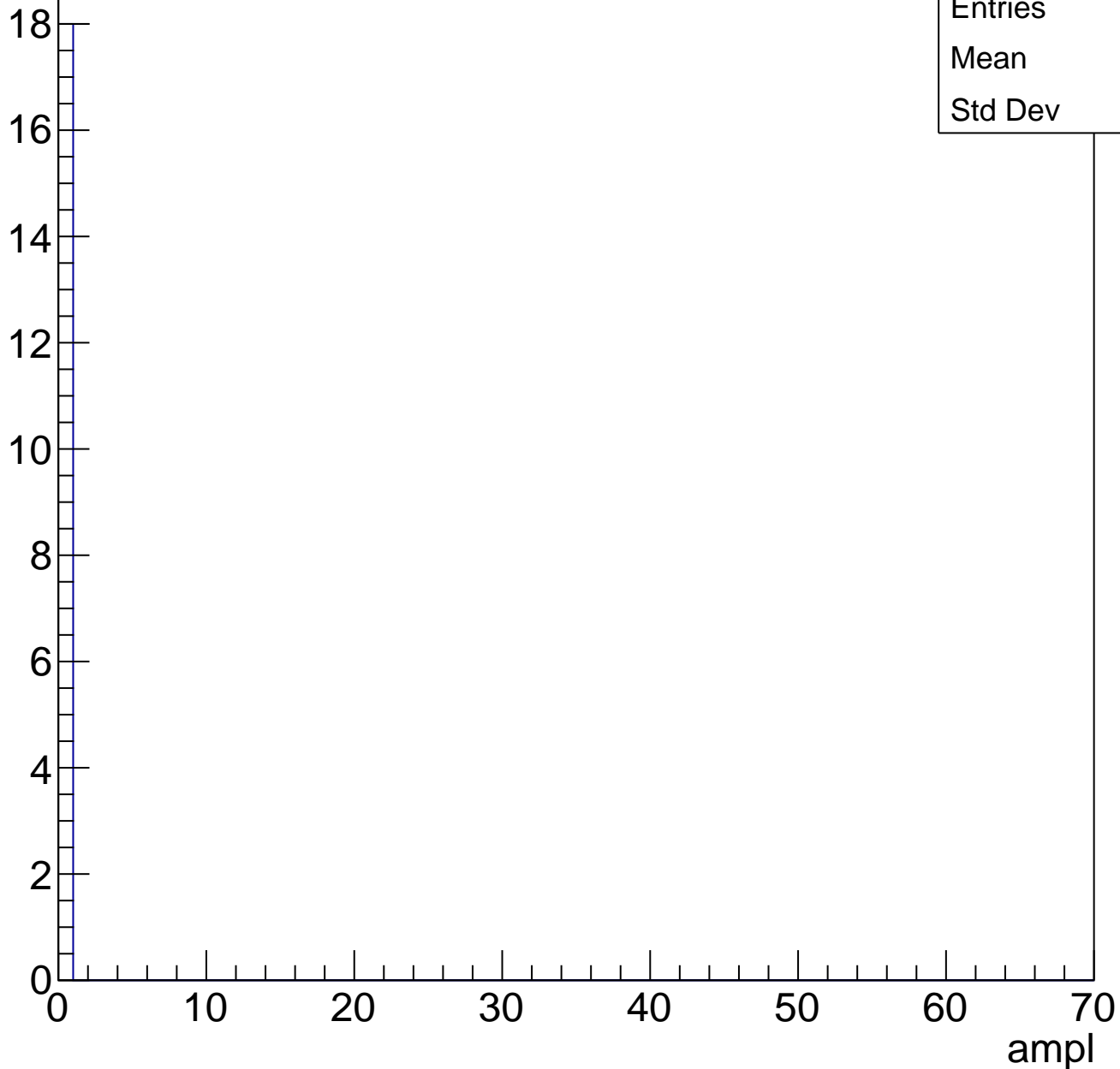


B1L103S, U9-ch4, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	18
Mean	0
Std Dev	0

Entry

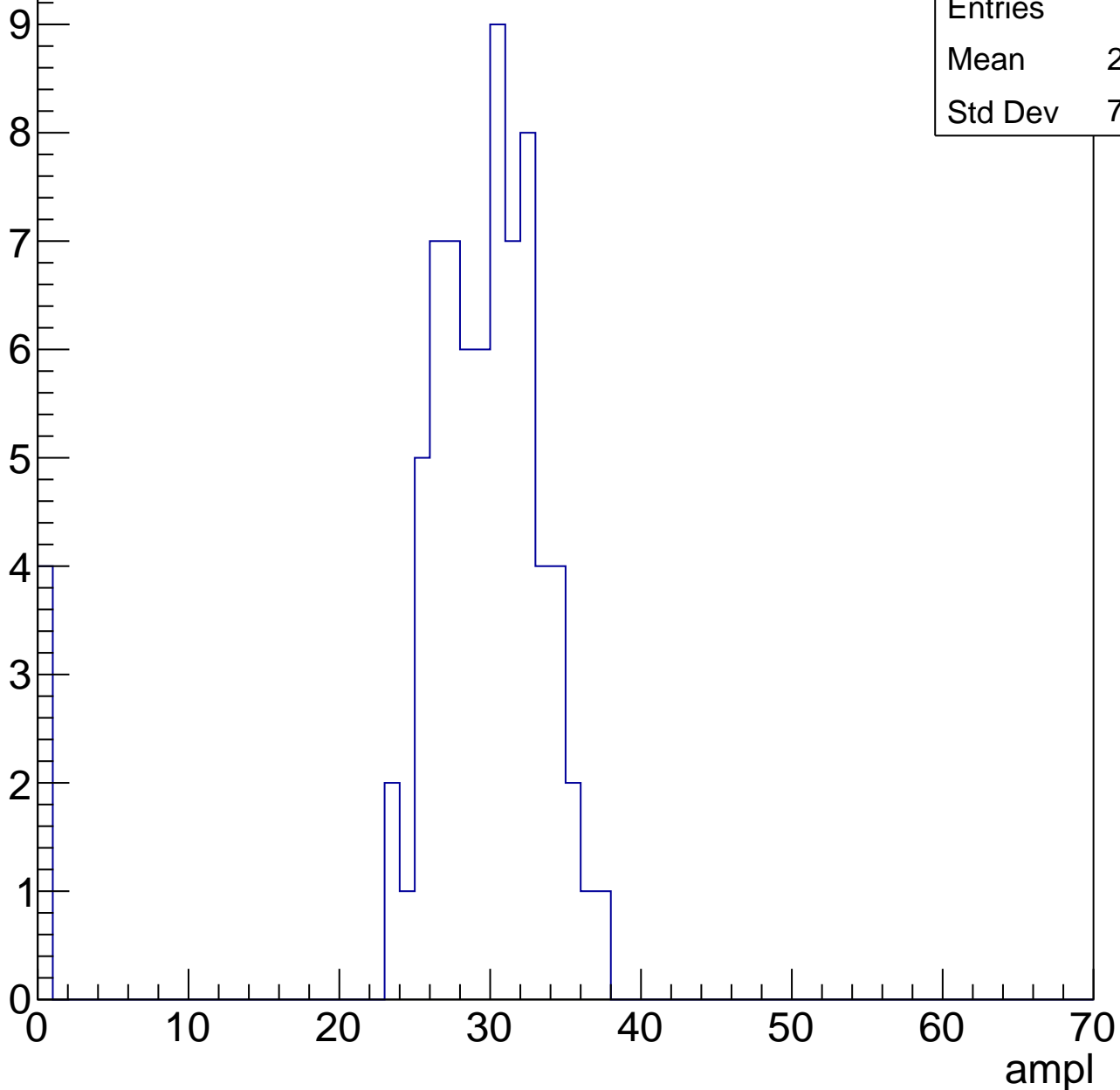


B1L103S, U9-ch5, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	27.86
Std Dev	7.353

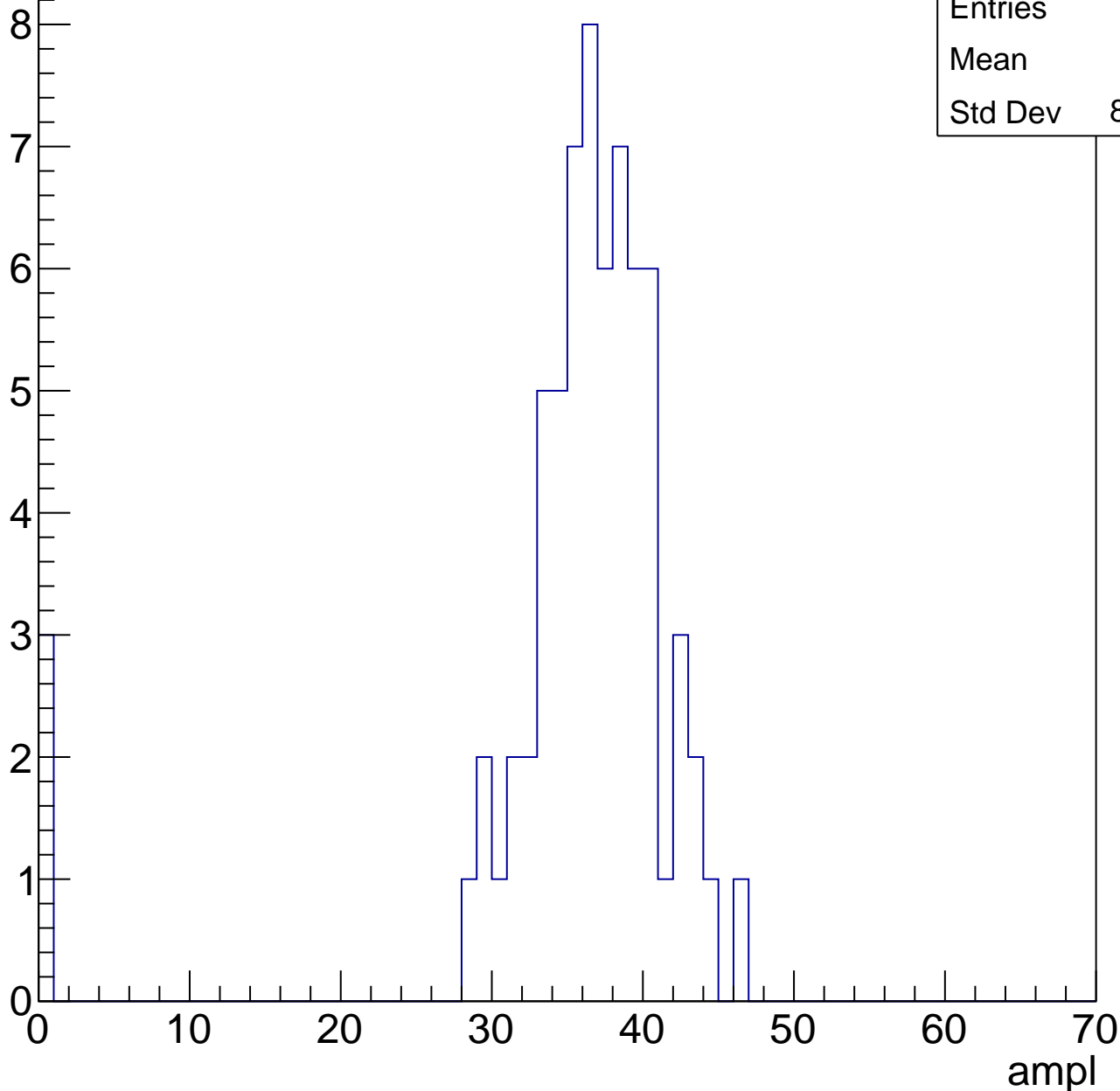


B1L103S, U9-ch5, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	35
Std Dev	8.297

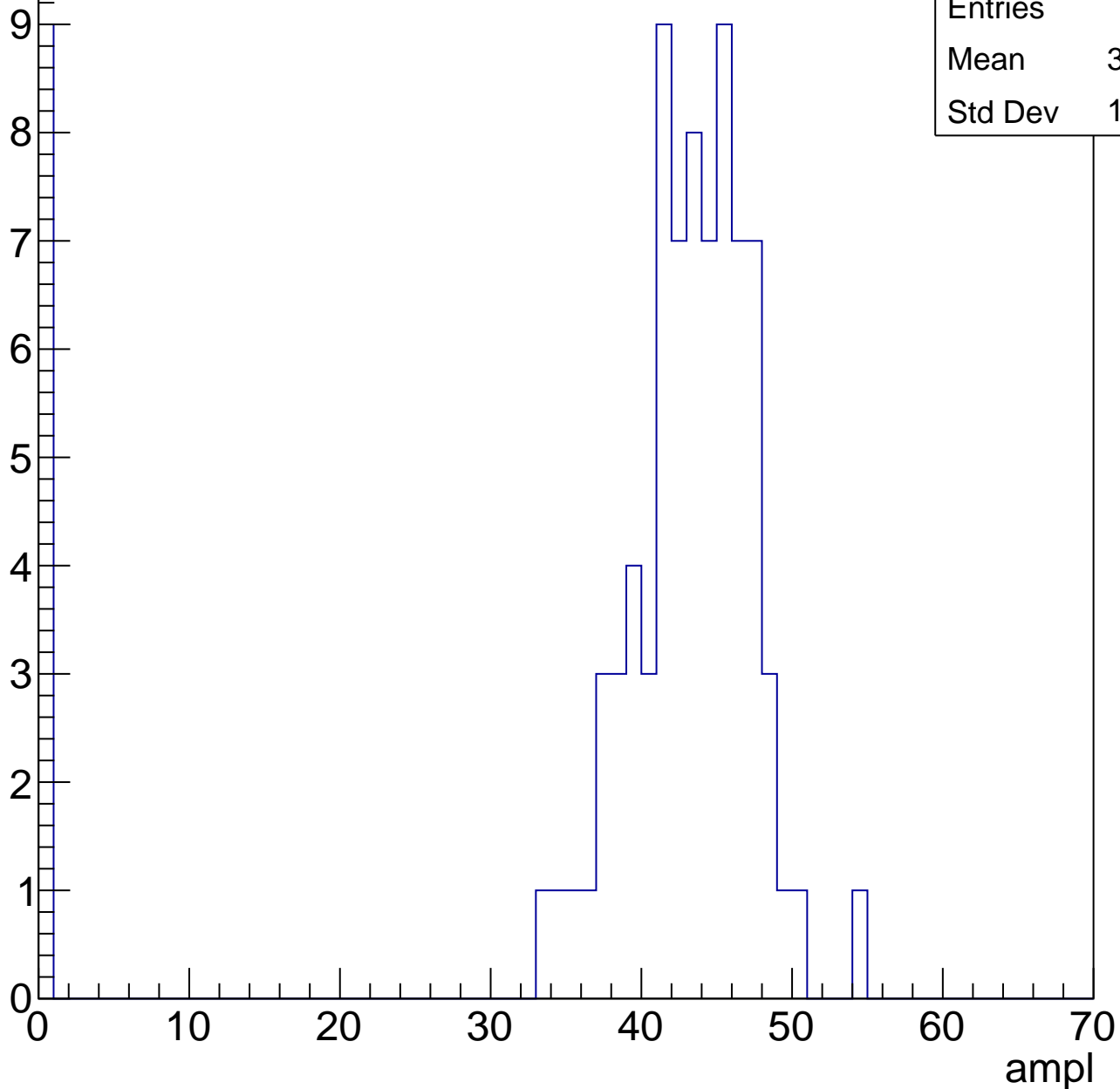


B1L103S, U9-ch5, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	86
Mean	38.45
Std Dev	13.63

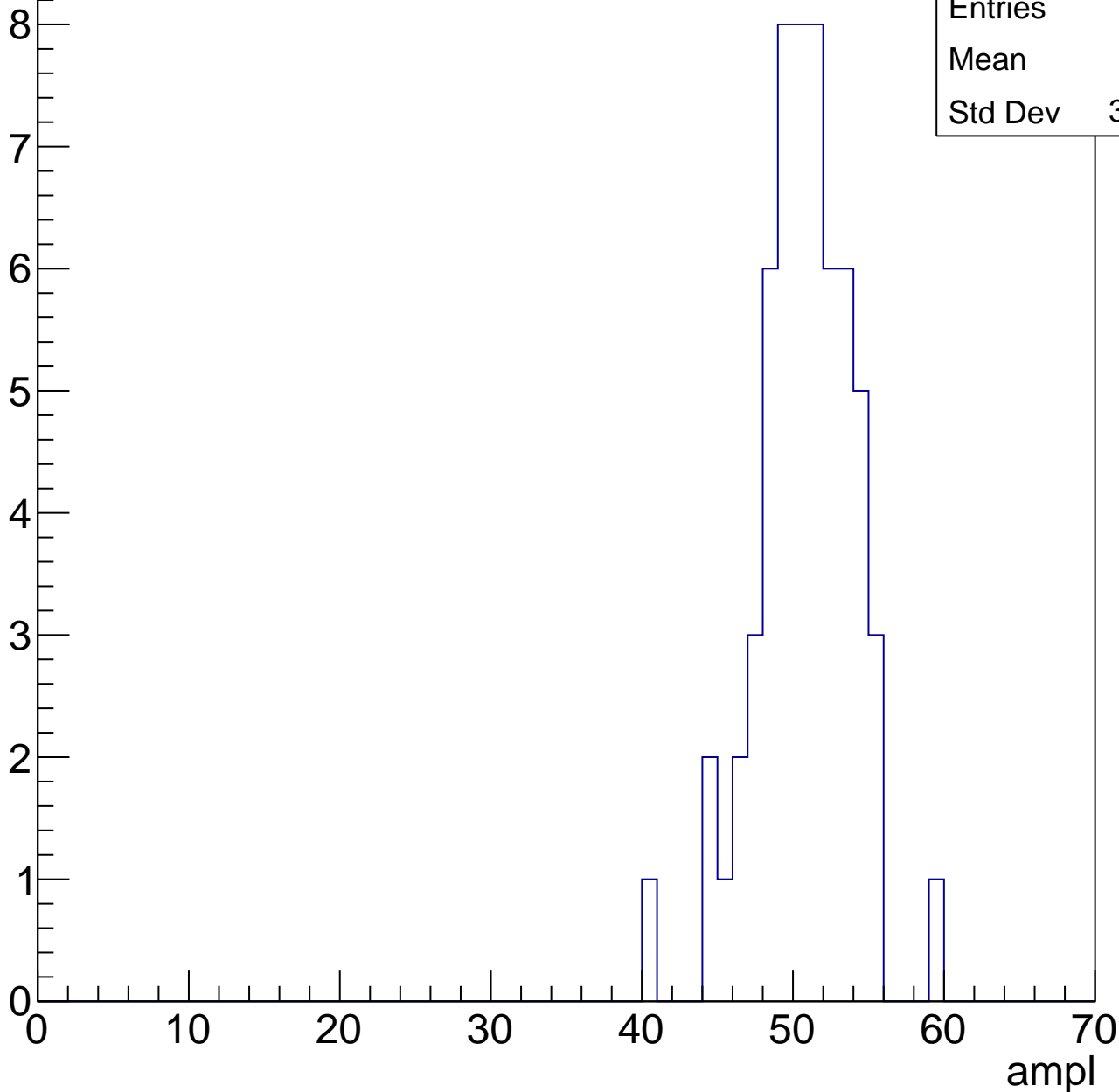


B1L103S, U9-ch5, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	50.3
Std Dev	3.174

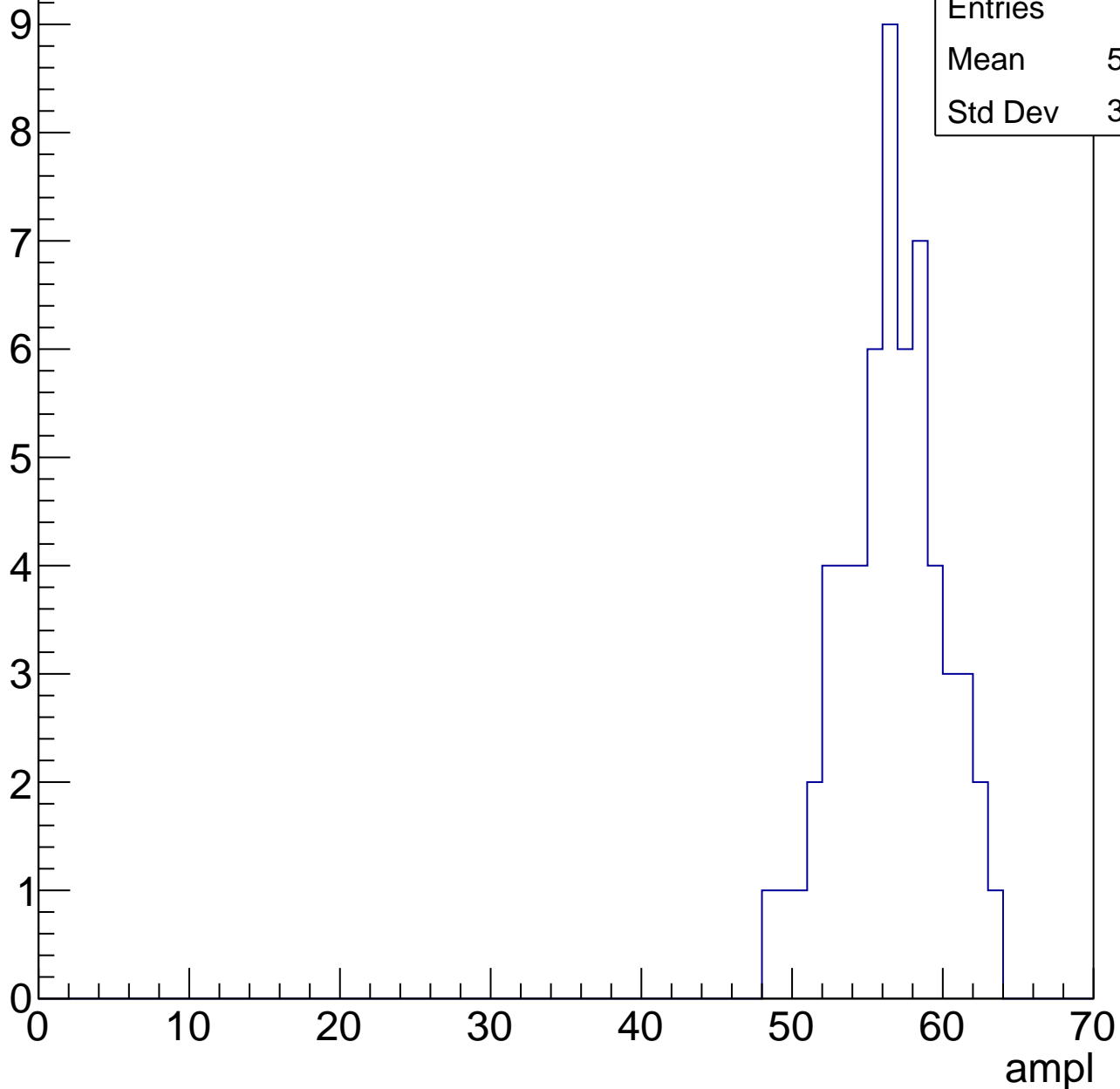


B1L103S, U9-ch5, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	56.09
Std Dev	3.308



B1L103S, U9-ch5, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

8
7
6
5
4
3
2
1
0

Entries	41
Mean	58.76
Std Dev	9.54

ampl

0

10

20

30

40

50

60

70

B1L103S, U9-ch5, adc6

calib_packv5_041523_1651.root, FC#0, port C2

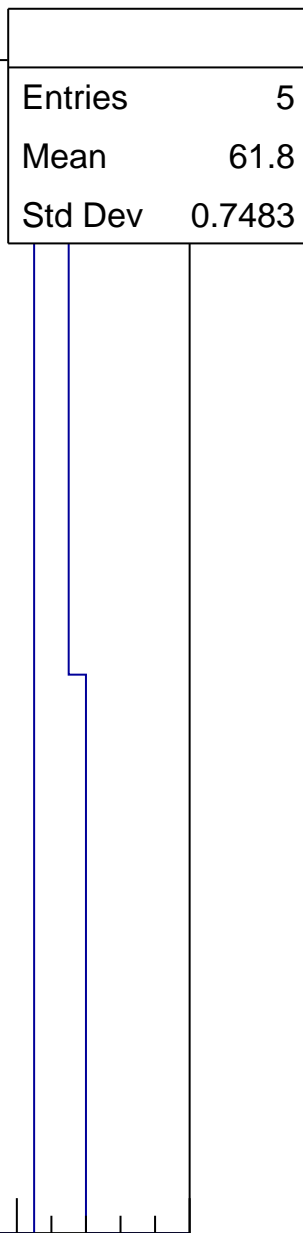
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	5
Mean	61.8
Std Dev	0.7483

0 10 20 30 40 50 60 70

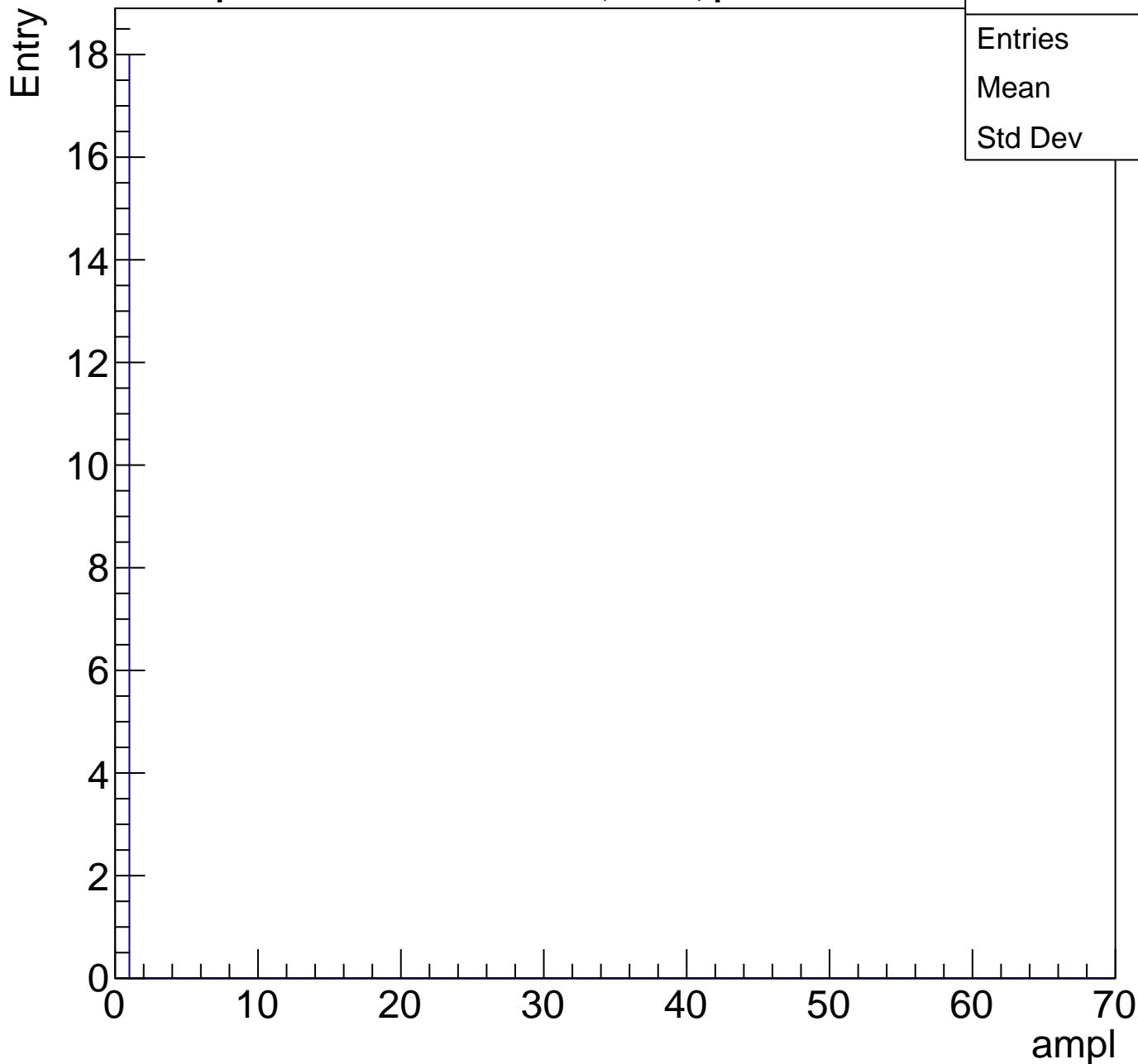
ampl



B1L103S, U9-ch5, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	18
Mean	0
Std Dev	0

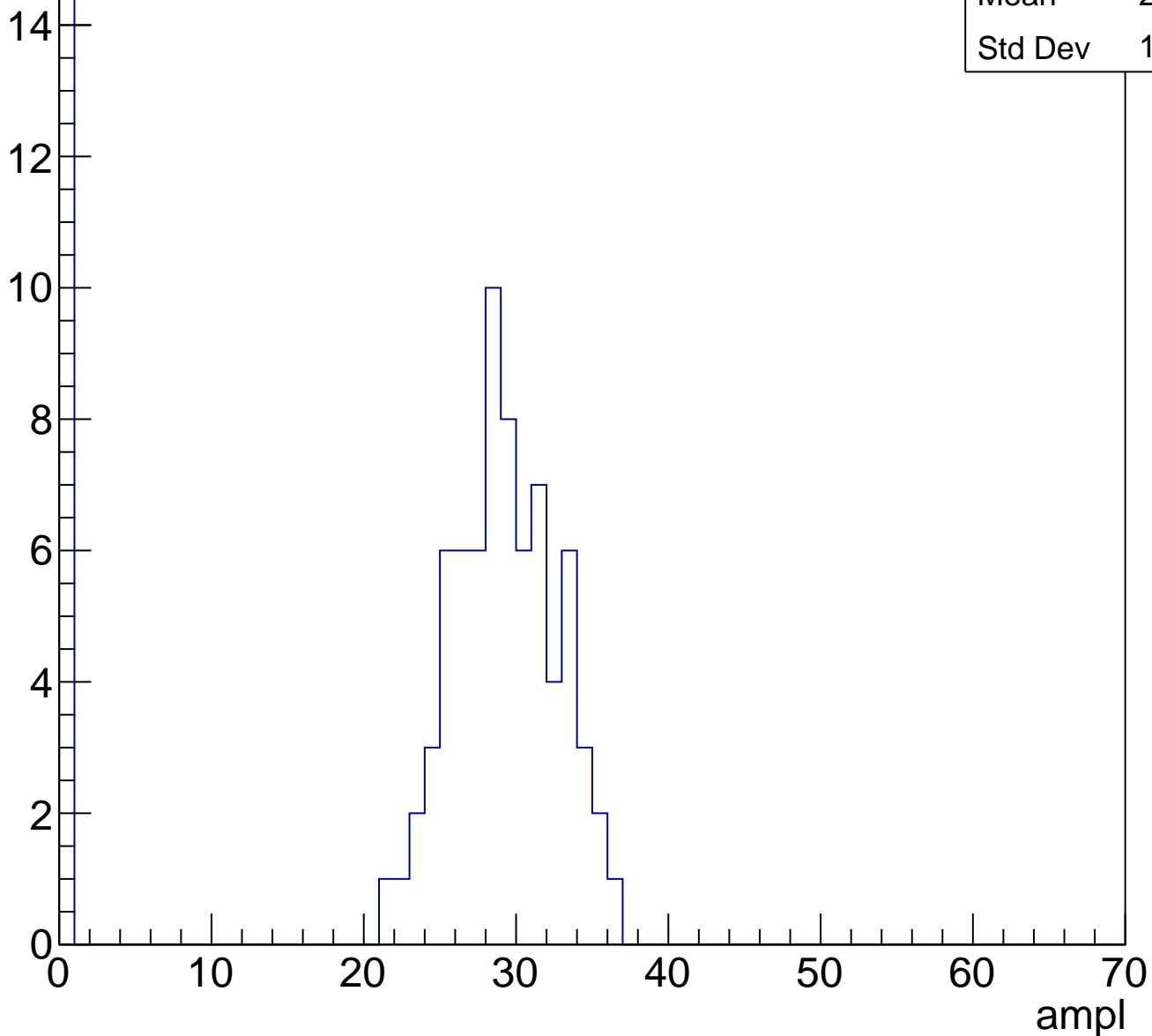


B1L103S, U9-ch6, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	87
Mean	23.82
Std Dev	11.29

Entry

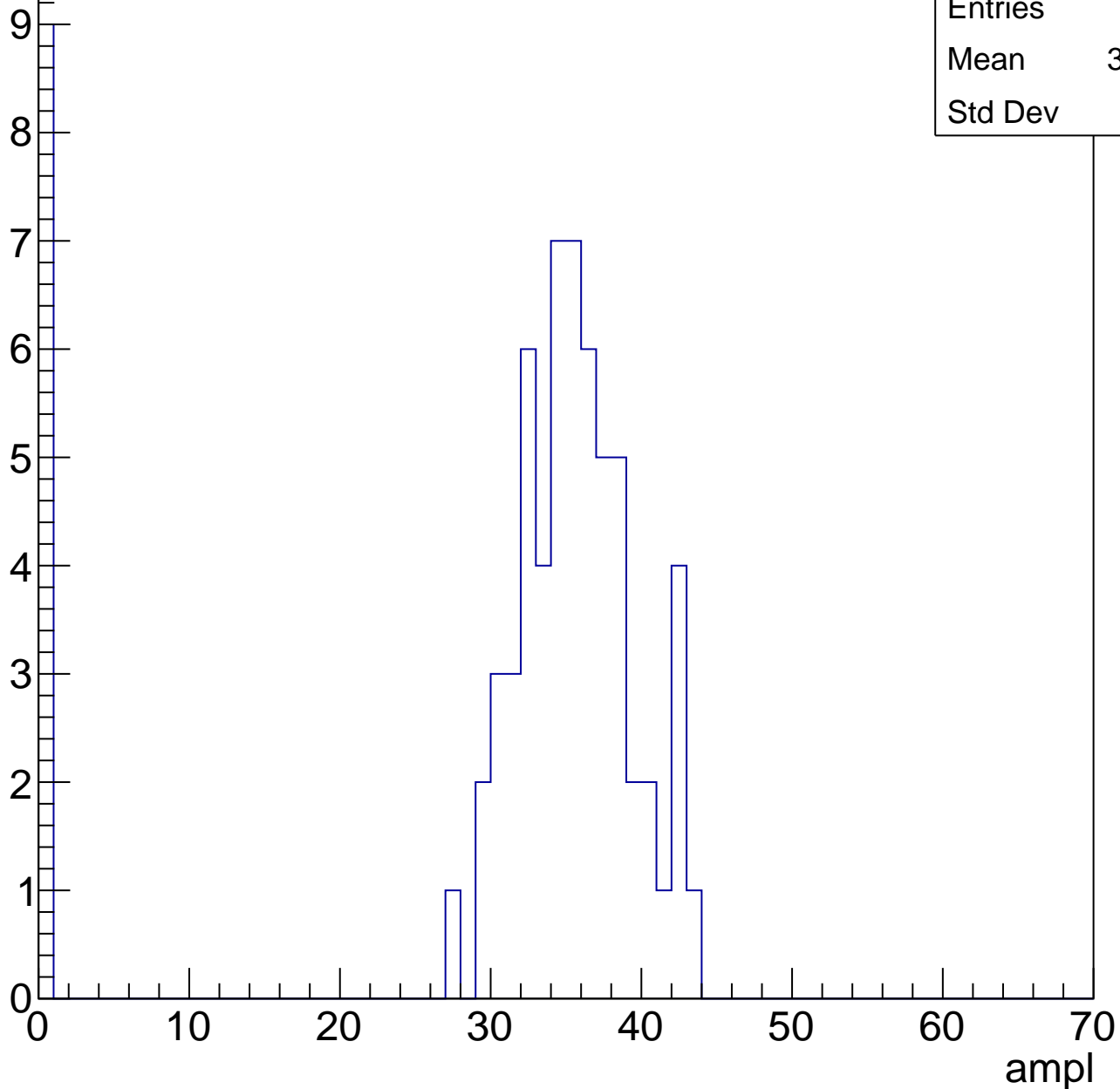


B1L103S, U9-ch6, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	30.53
Std Dev	12.4

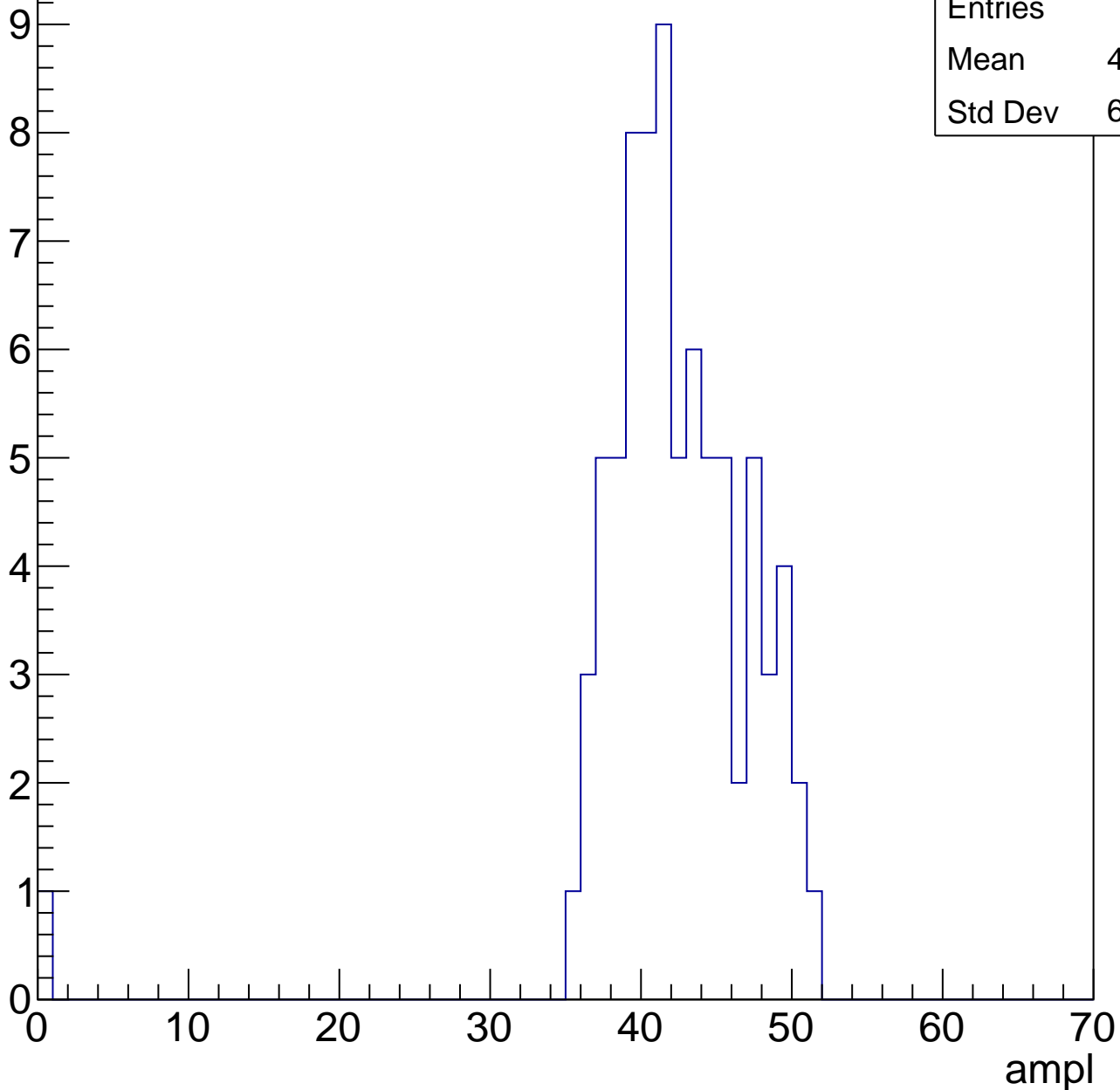


B1L103S, U9-ch6, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	41.67
Std Dev	6.172

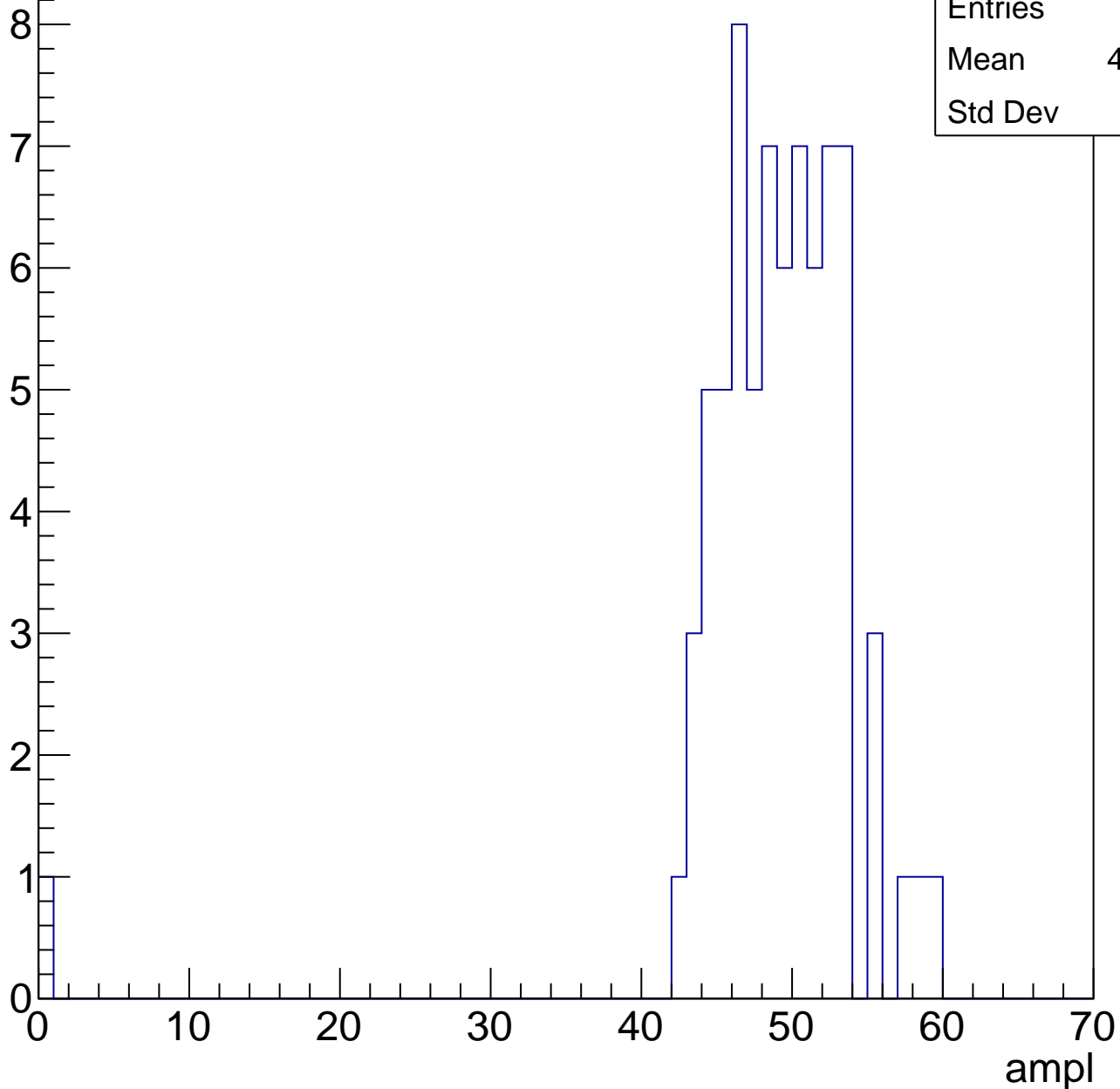


B1L103S, U9-ch6, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	48.36
Std Dev	6.77

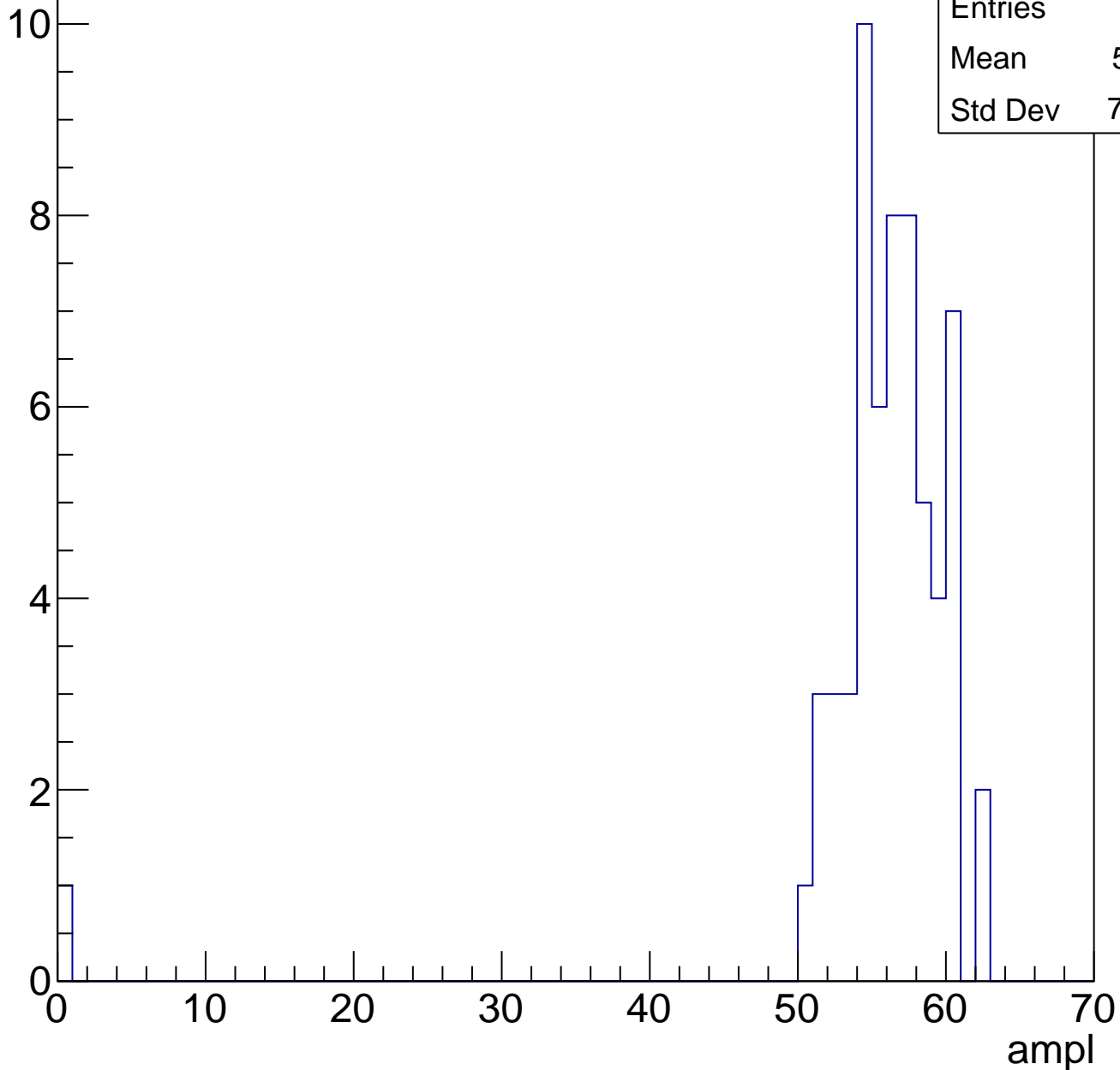


B1L103S, U9-ch6, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	61
Mean	55.11
Std Dev	7.648

Entry

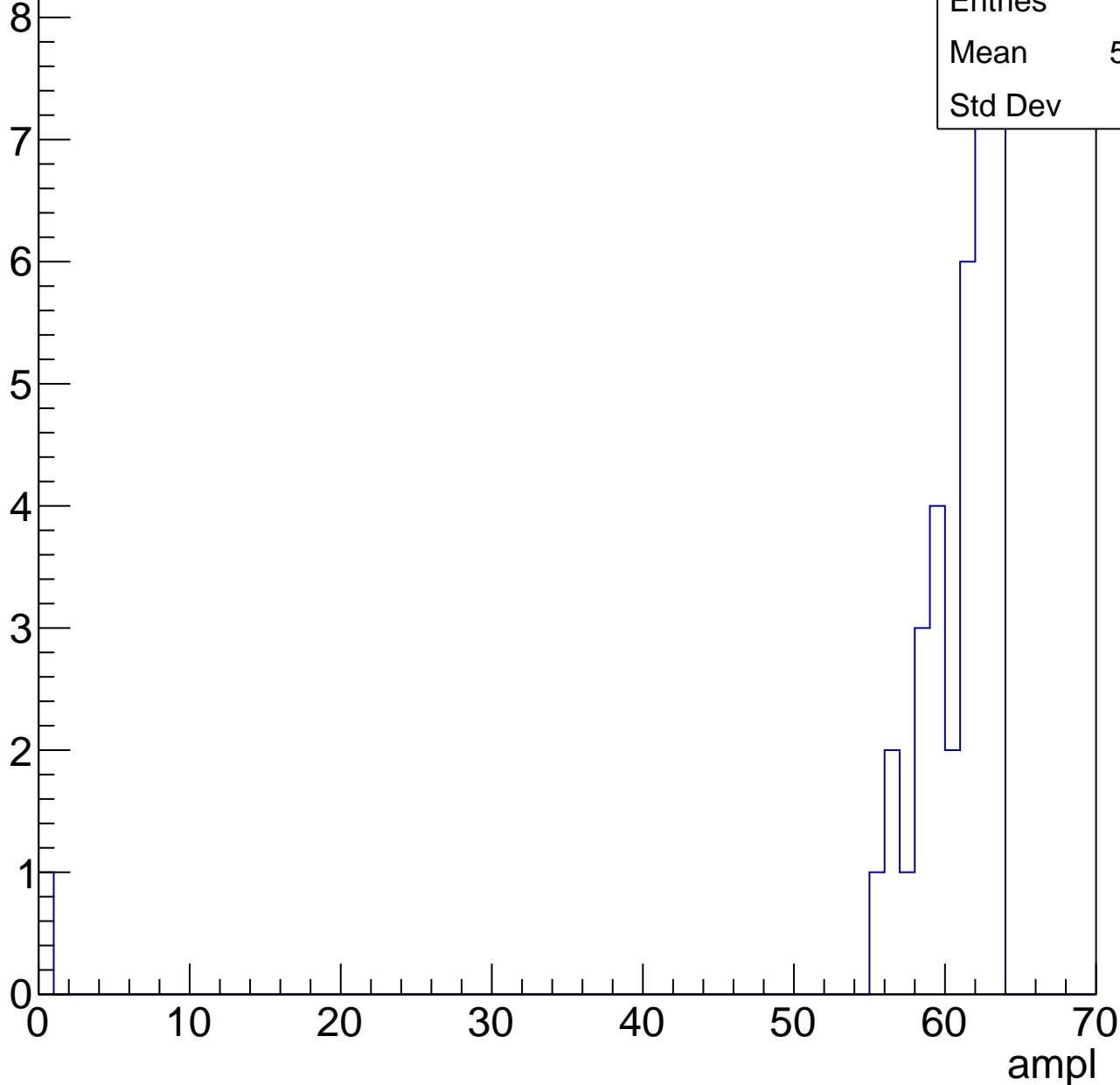


B1L103S, U9-ch6, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

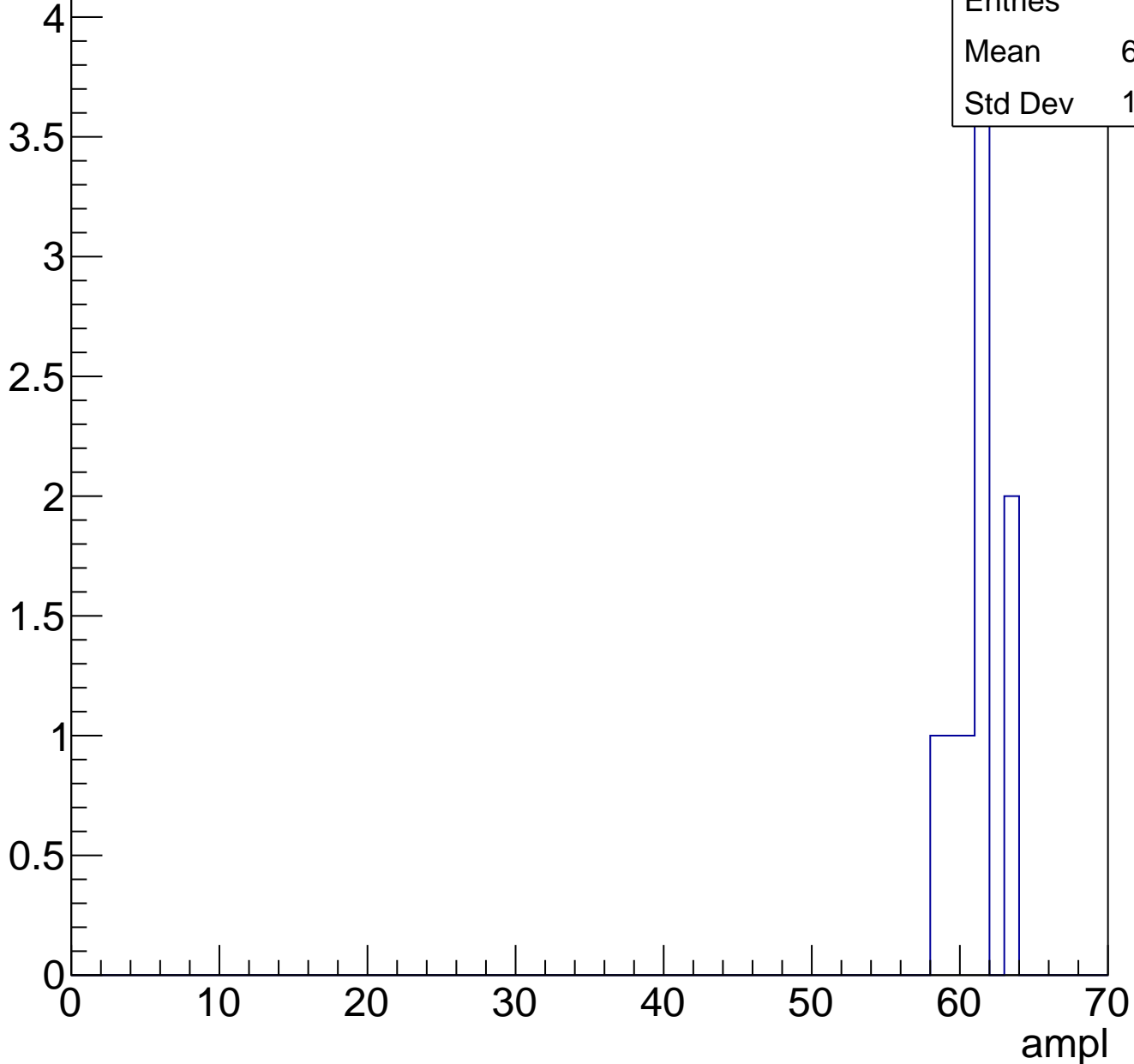
Entries	36
Mean	58.89
Std Dev	10.2



B1L103S, U9-ch6, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch6, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	0
Std Dev	0



B1L103S, U9-ch7, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	70
Mean	26.09
Std Dev	11.56

Entry

10

8

6

4

2

0

0

10

20

30

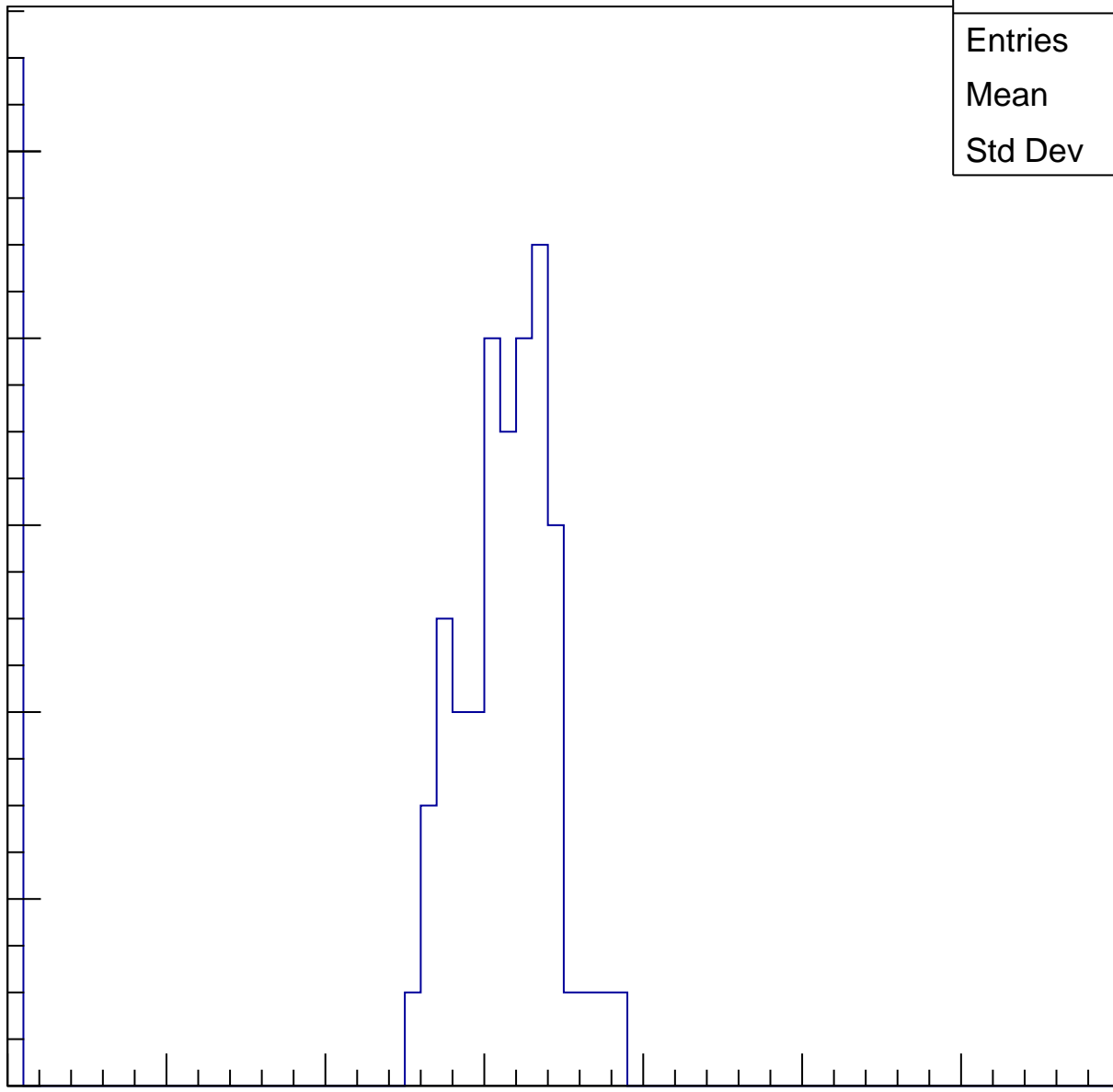
40

50

60

70

ampl

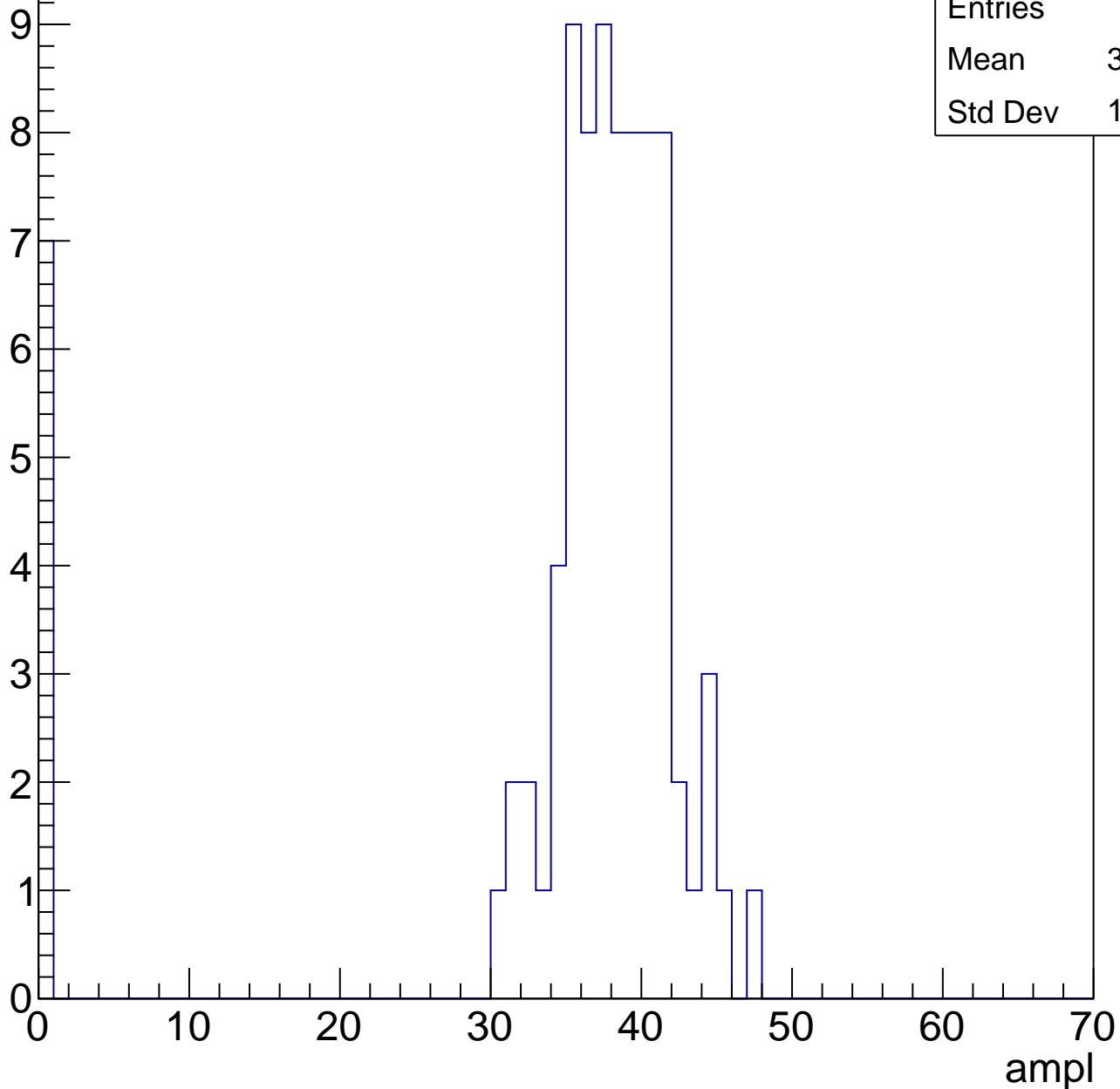


B1L103S, U9-ch7, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	83
Mean	34.65
Std Dev	10.99

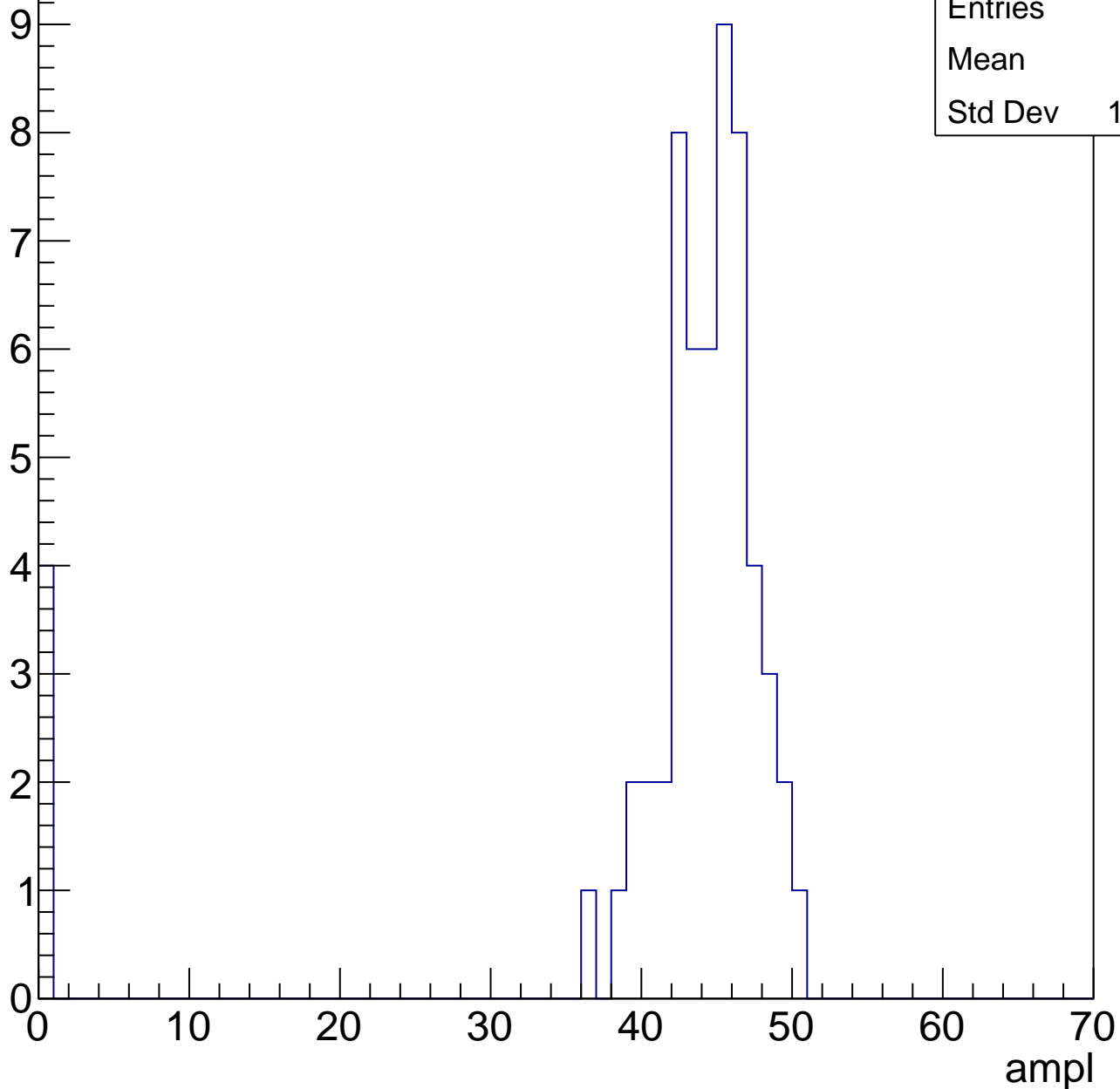


B1L103S, U9-ch7, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	41.1
Std Dev	11.42

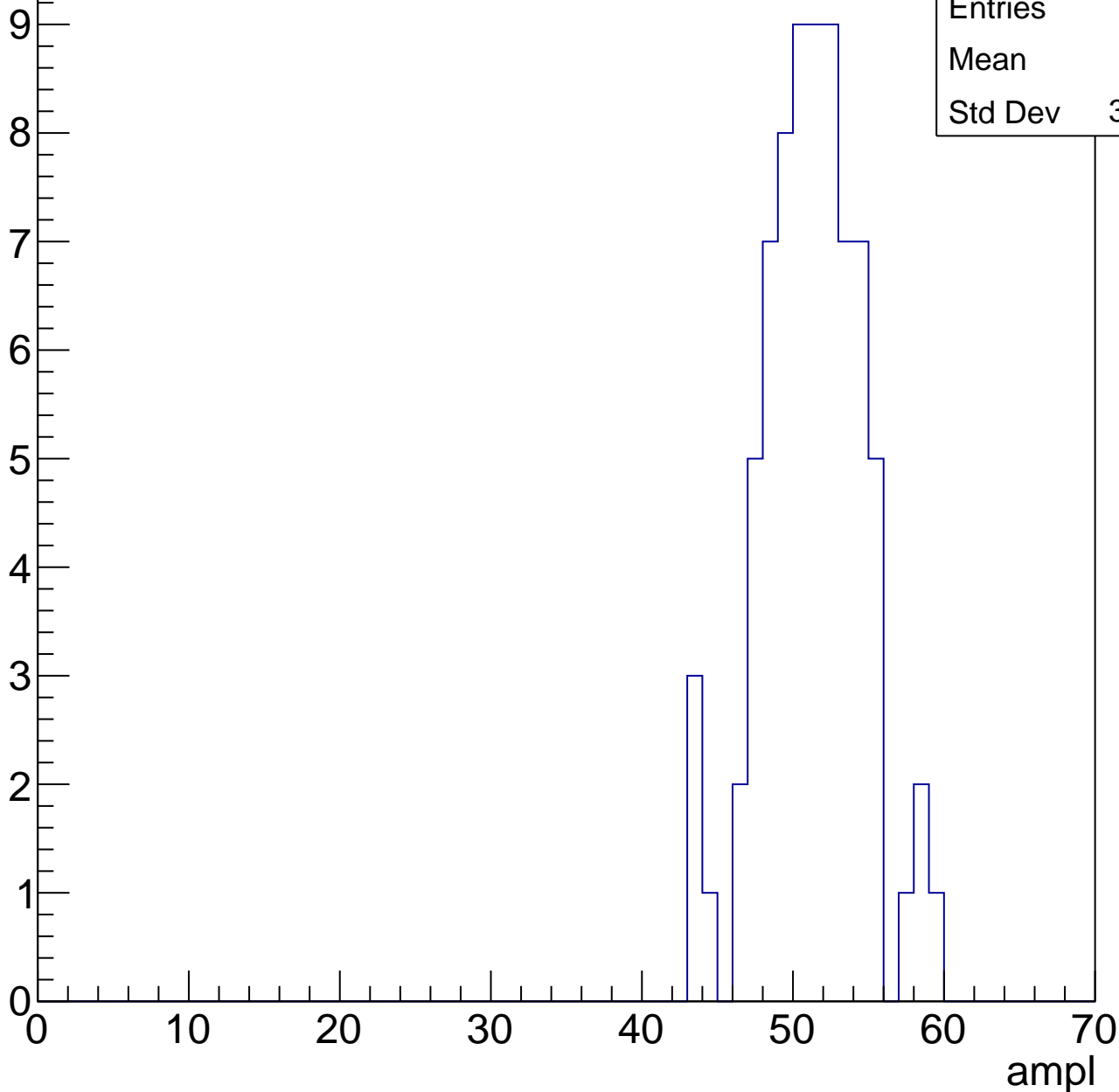


B1L103S, U9-ch7, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

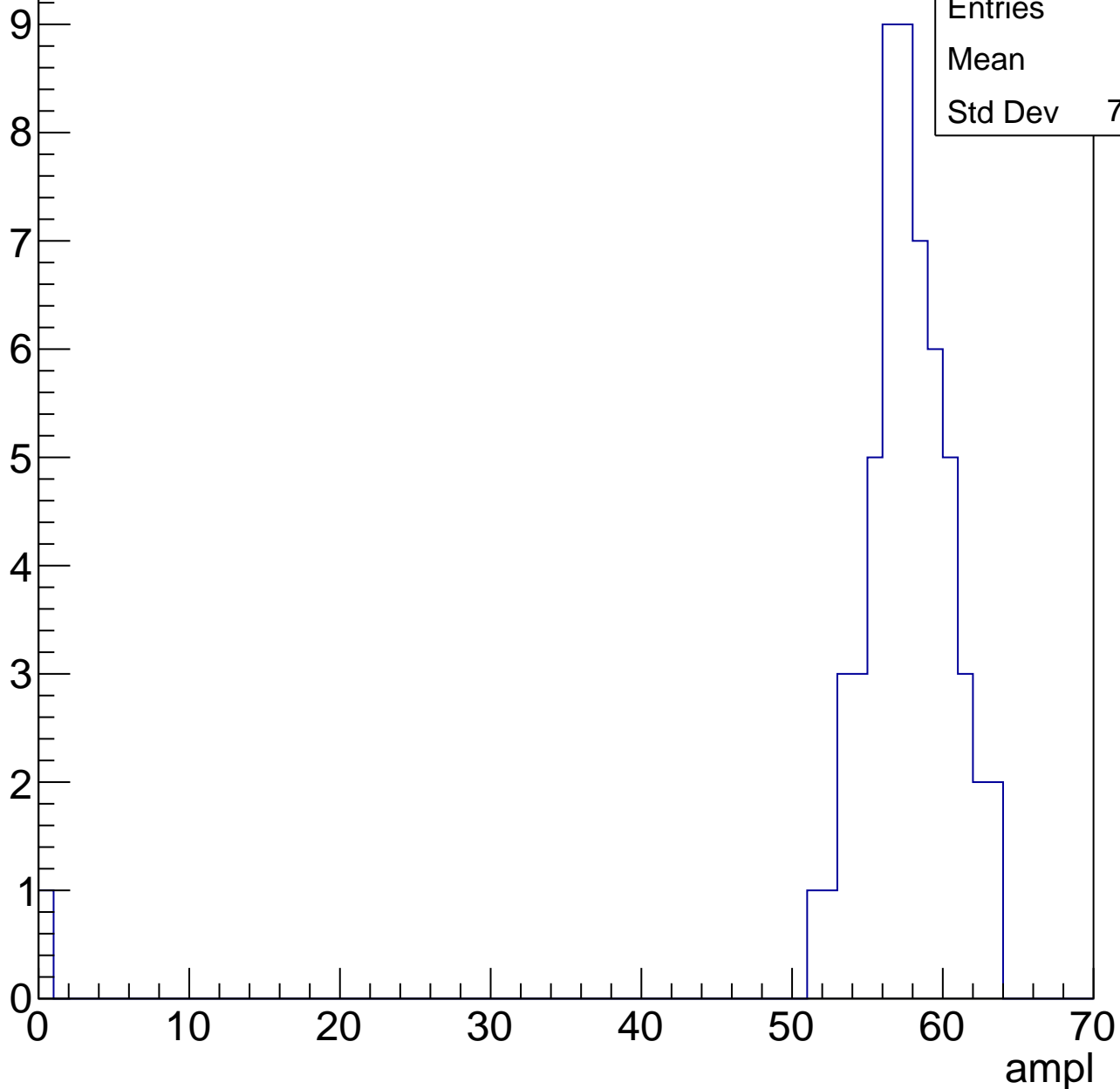
Entries	76
Mean	50.8
Std Dev	3.344



B1L103S, U9-ch7, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

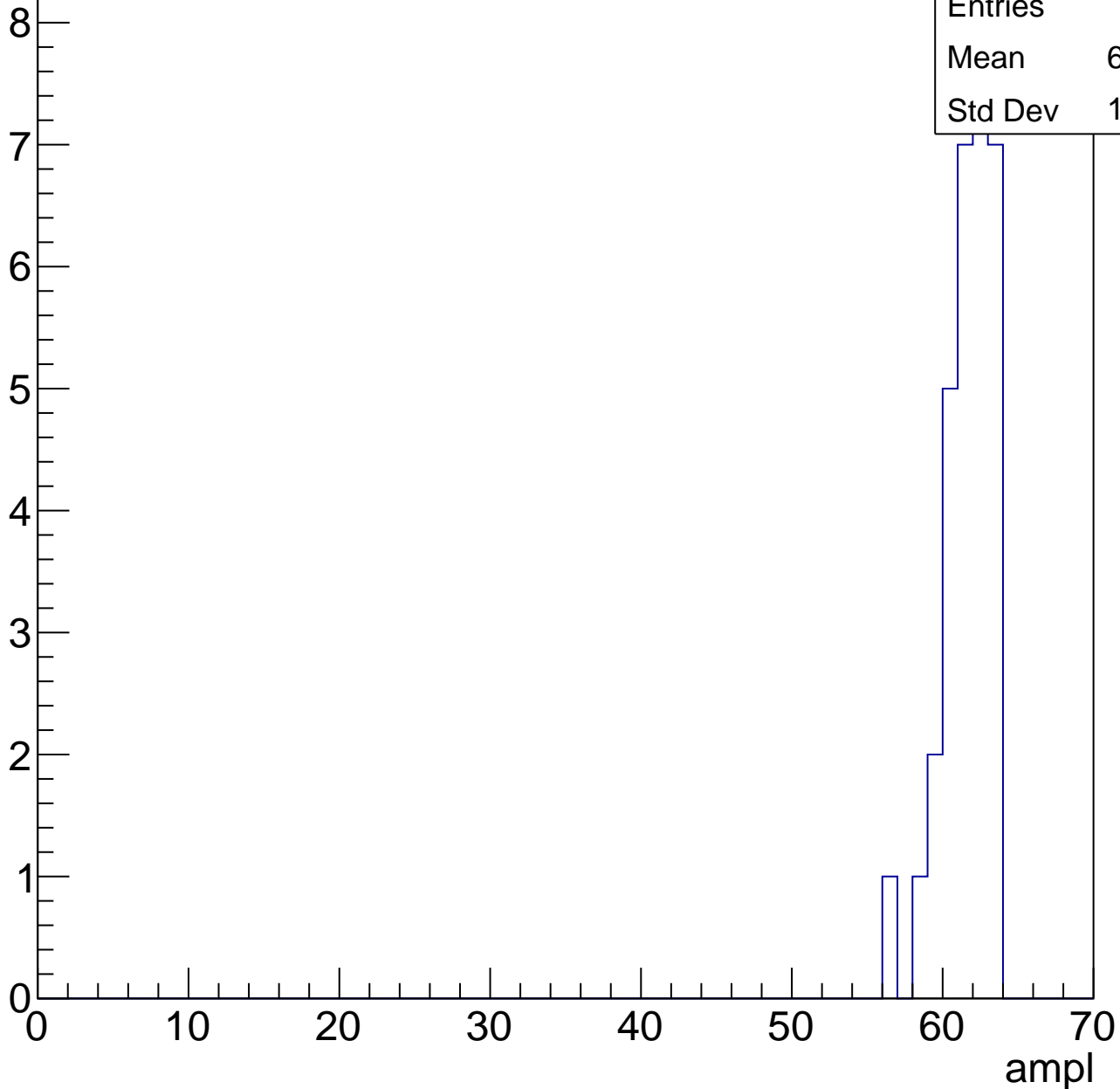


B1L103S, U9-ch7, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

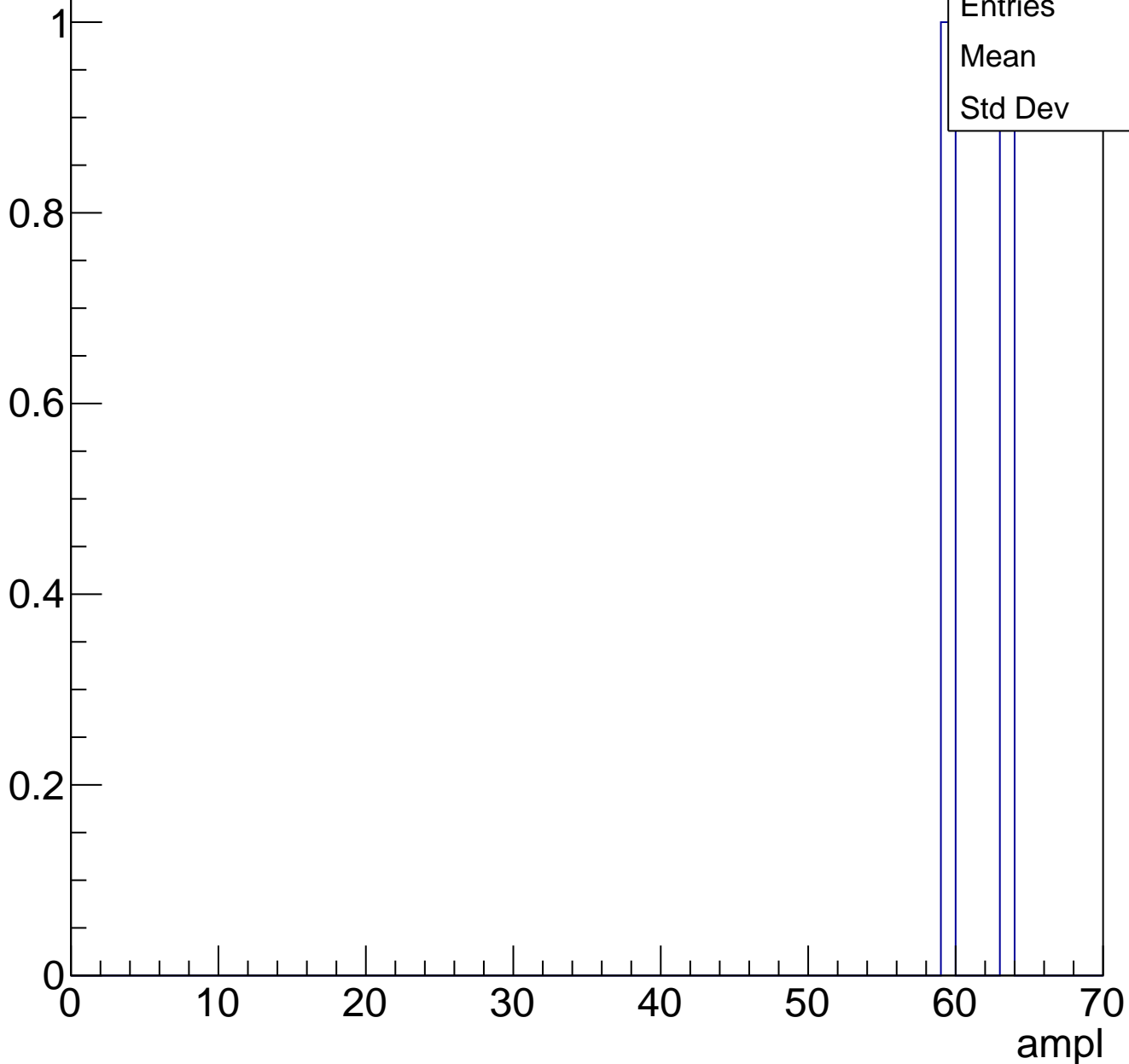
Entries	31
Mean	61.16
Std Dev	1.628



B1L103S, U9-ch7, adc6

calib_packv5_041523_1651.root, FC#0, port C2

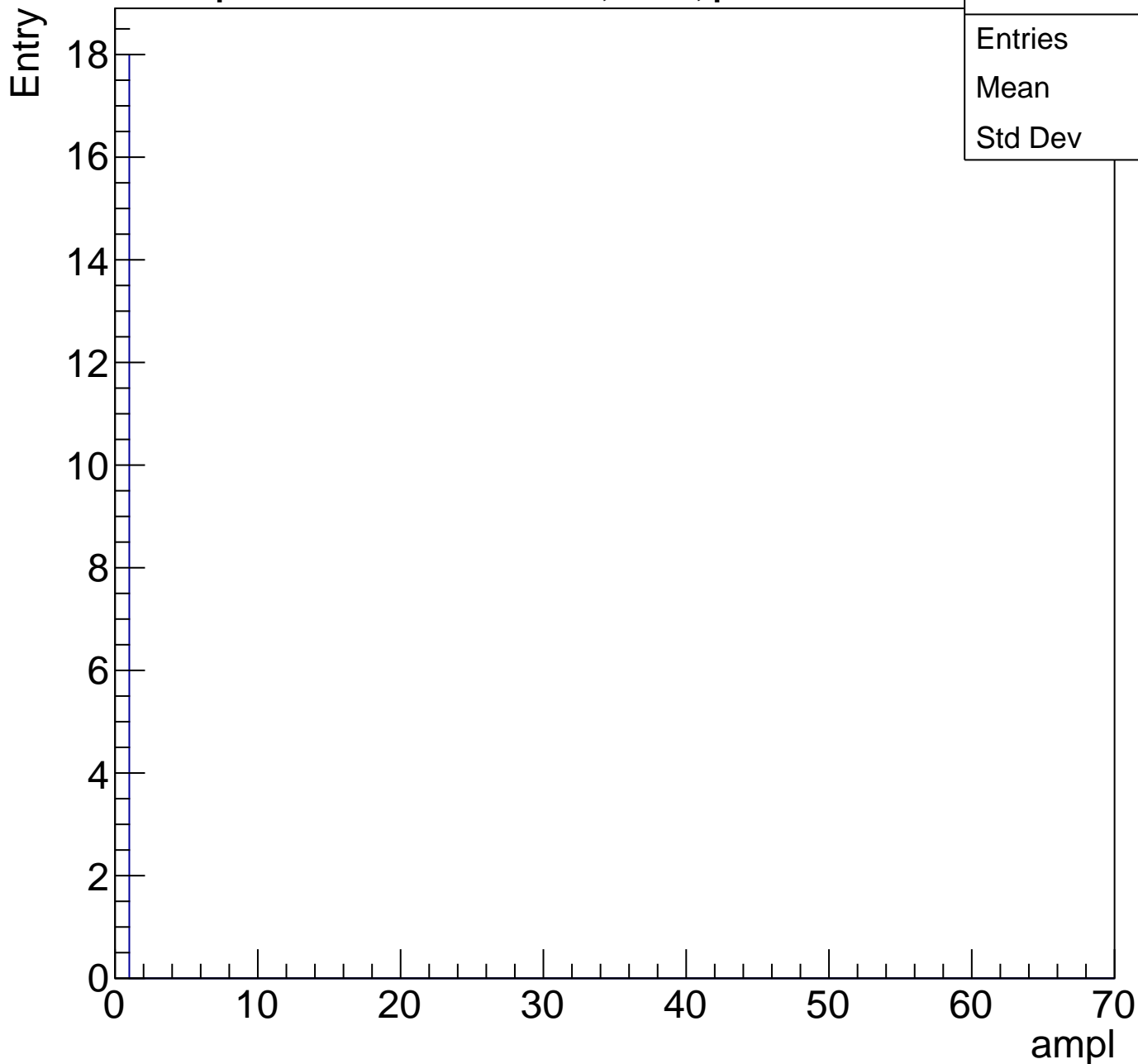
Entry



B1L103S, U9-ch7, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	18
Mean	0
Std Dev	0

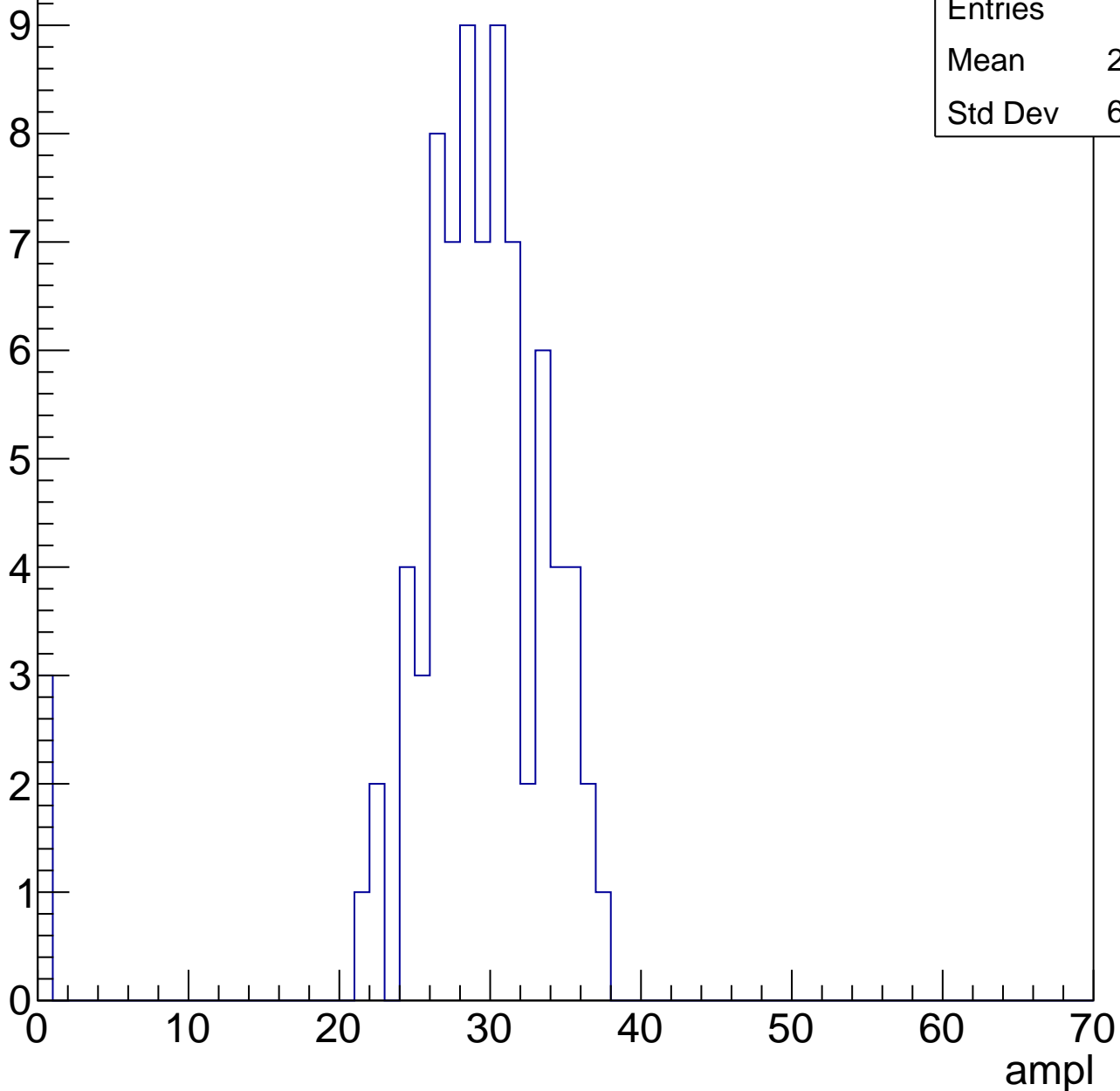


B1L103S, U9-ch8, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	79
Mean	28.13
Std Dev	6.598



B1L103S, U9-ch8, adc1

calib_packv5_041523_1651.root, FC#0, port C2

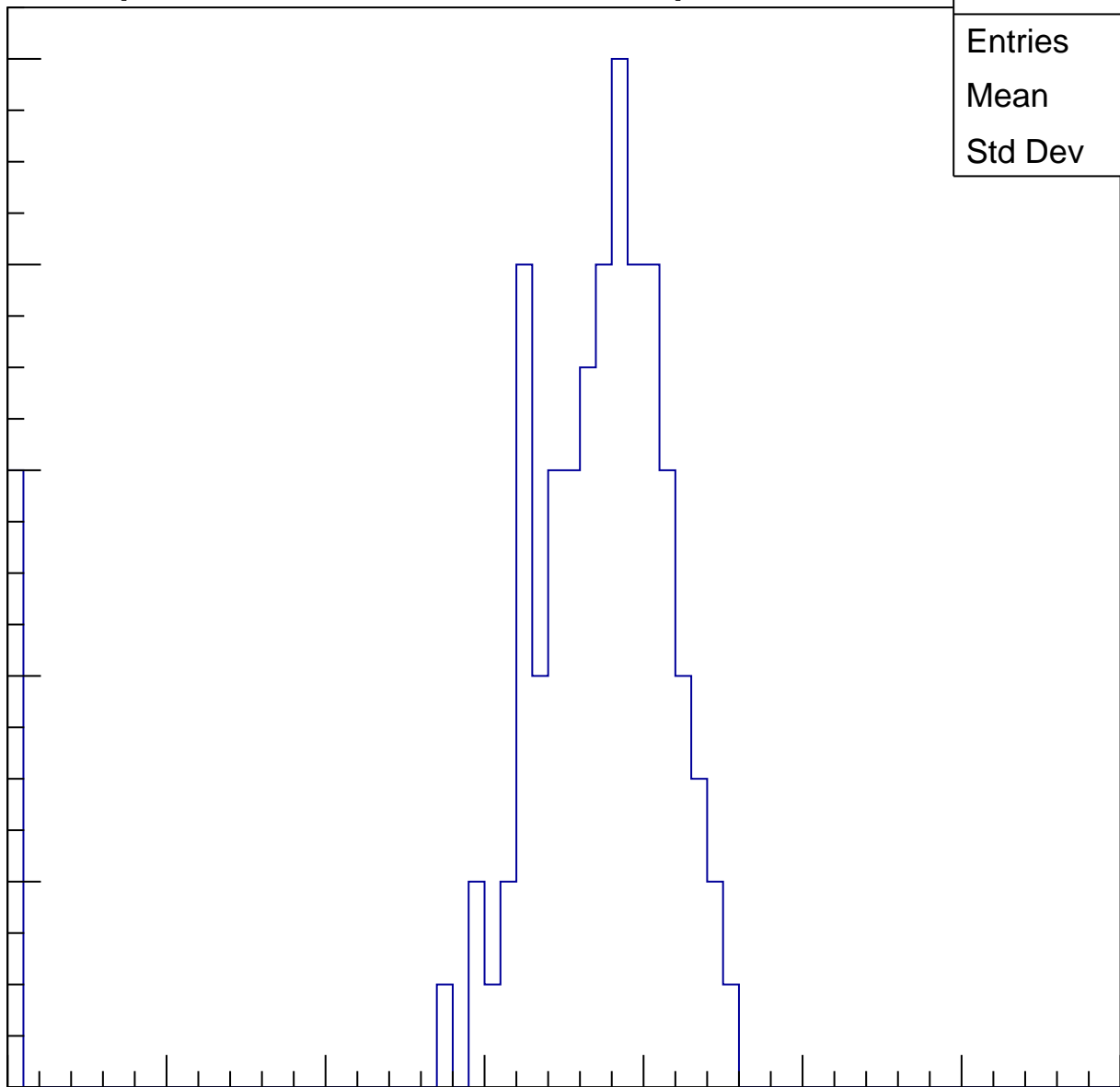
Entries	93
Mean	34.57
Std Dev	9.806

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

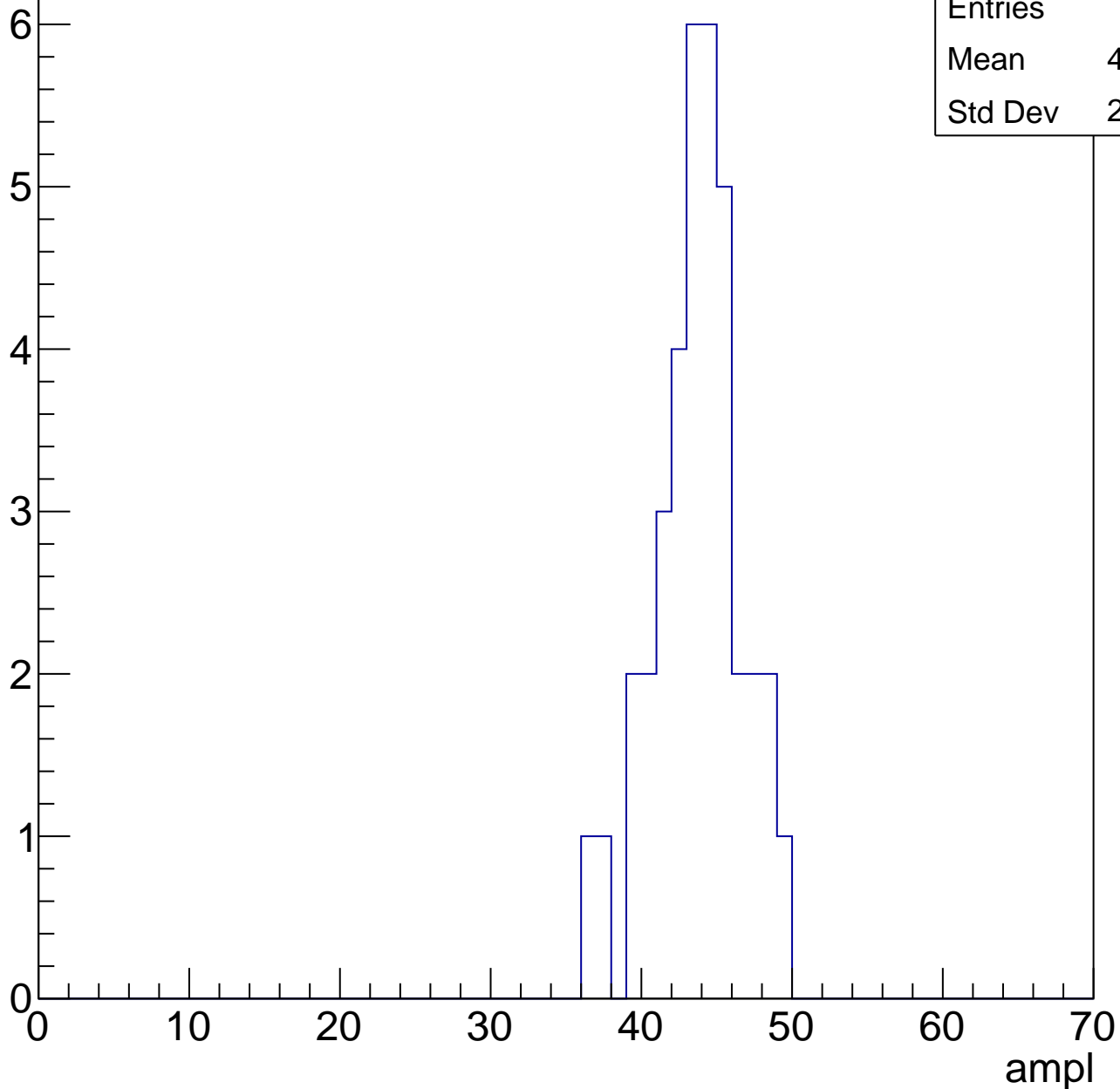


B1L103S, U9-ch8, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	37
Mean	43.24
Std Dev	2.898

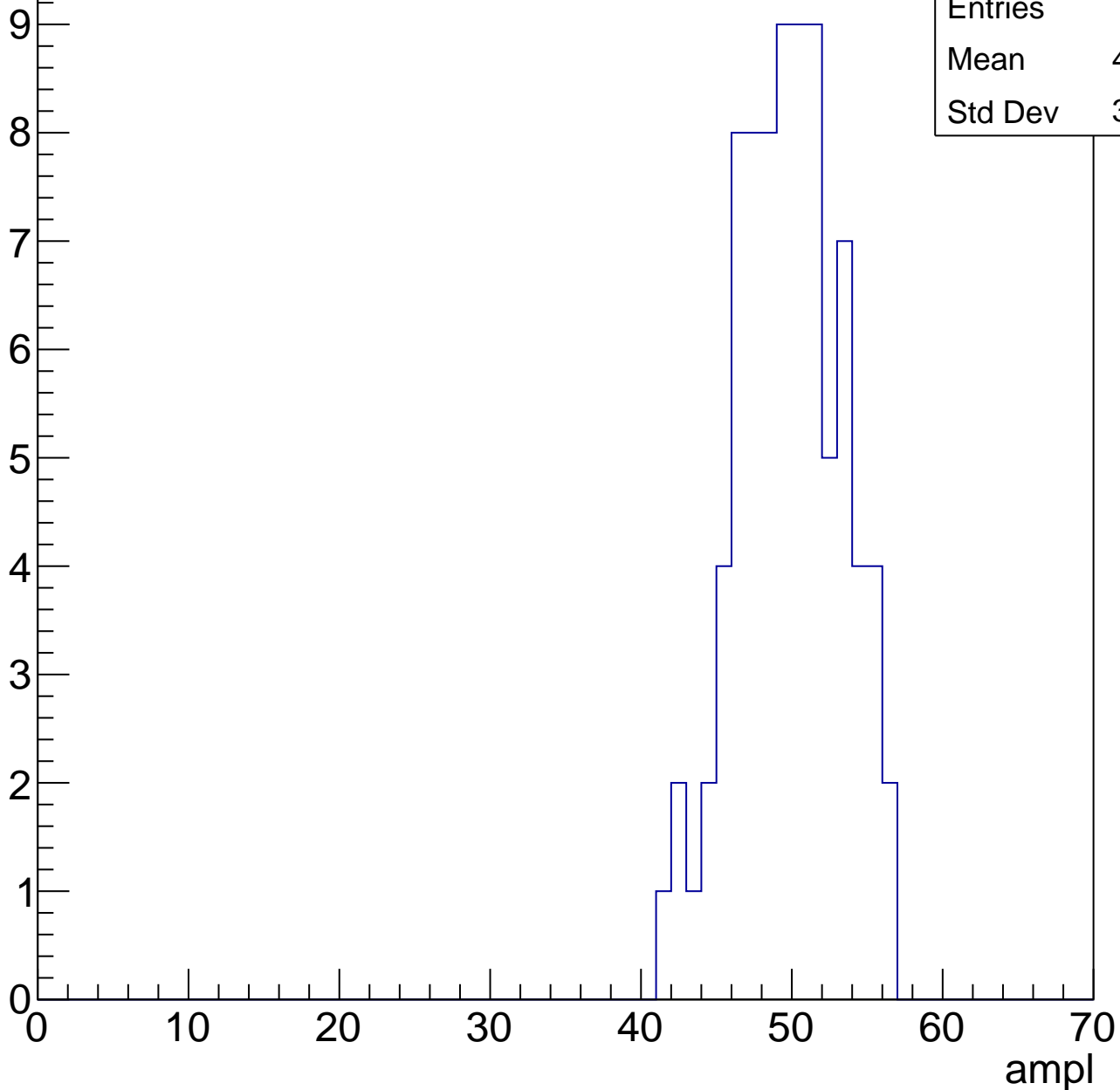


B1L103S, U9-ch8, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	83
Mean	49.31
Std Dev	3.401



B1L103S, U9-ch8, adc4

calib_packv5_041523_1651.root, FC#0, port C2

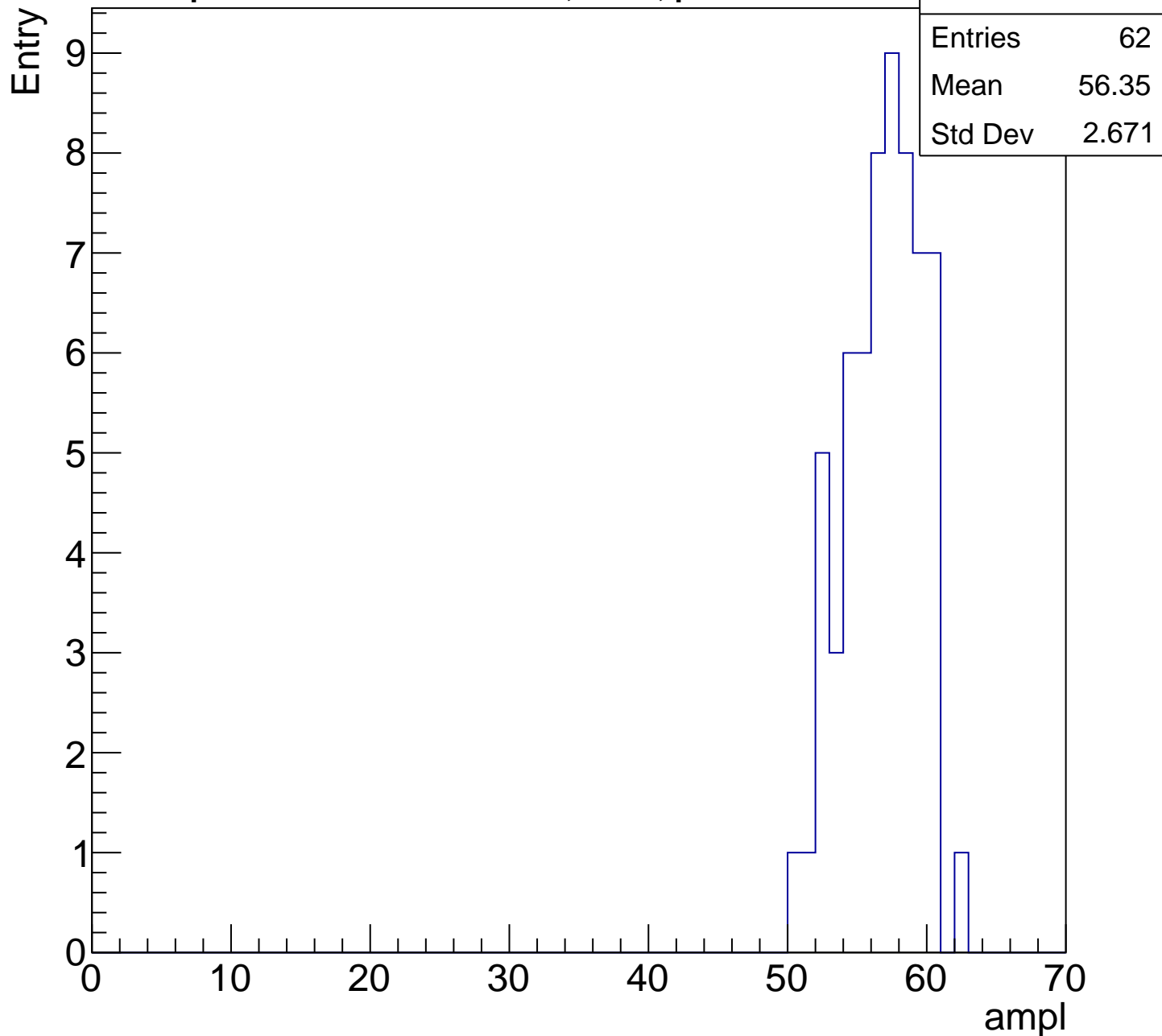
Entry

9
8
7
6
5
4
3
2
1
0

Entries	62
Mean	56.35
Std Dev	2.671

ampl

0 10 20 30 40 50 60 70

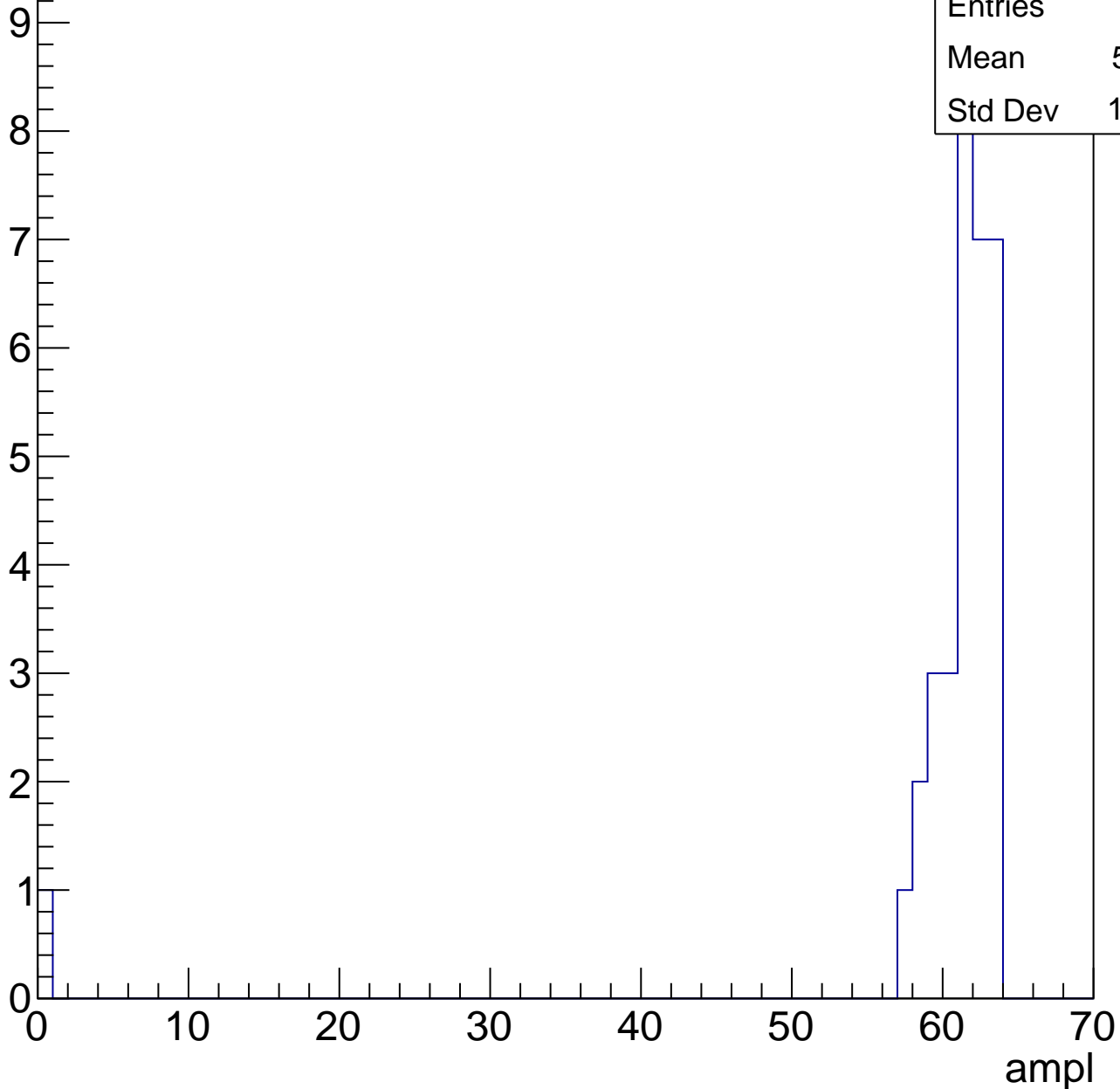


B1L103S, U9-ch8, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	33
Mean	59.21
Std Dev	10.59



B1L103S, U9-ch8, adc6

calib_packv5_041523_1651.root, FC#0, port C2

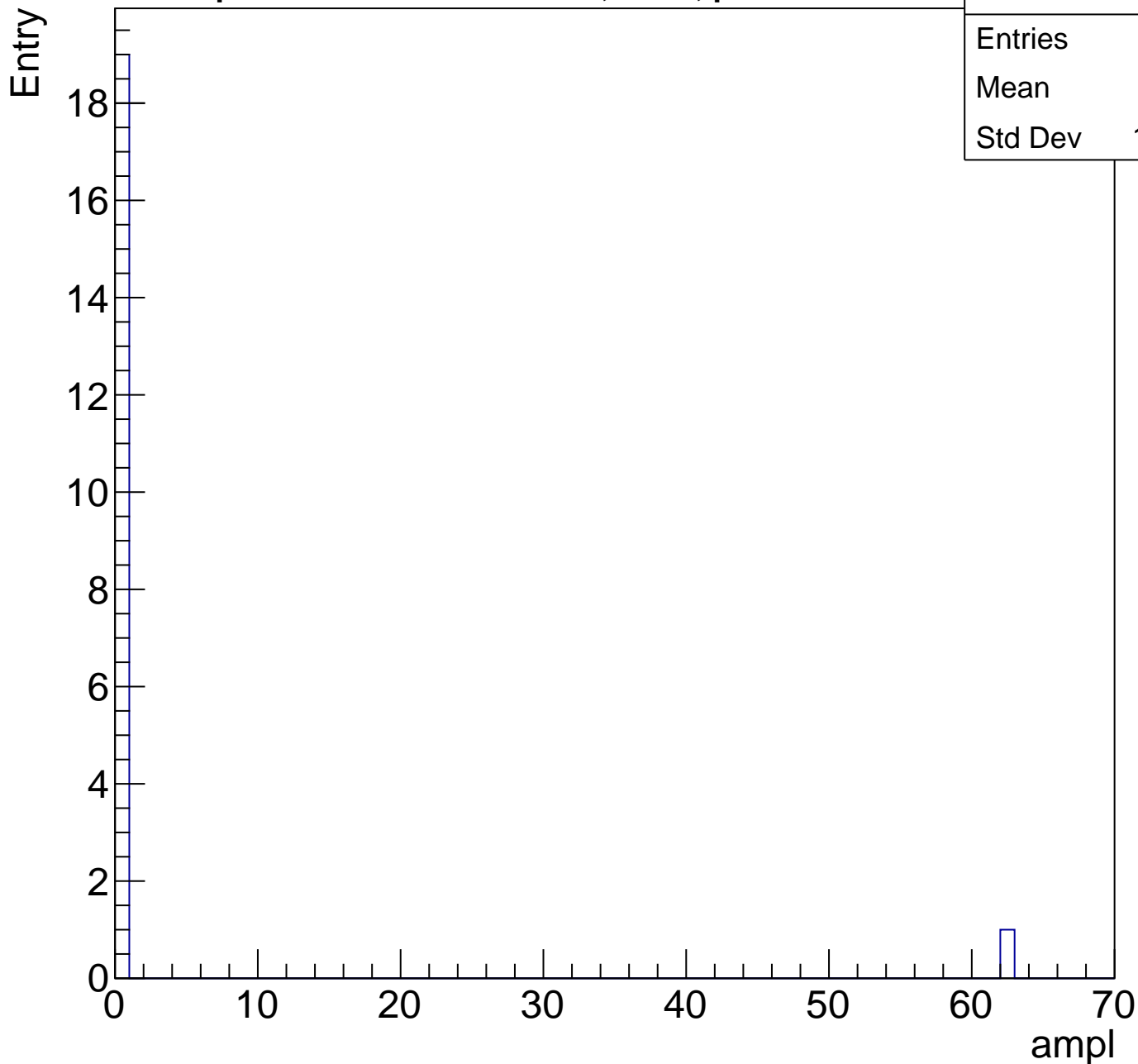
Entry



B1L103S, U9-ch8, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51



B1L103S, U9-ch9, adc0

calib_packv5_041523_1651.root, FC#0, port C2

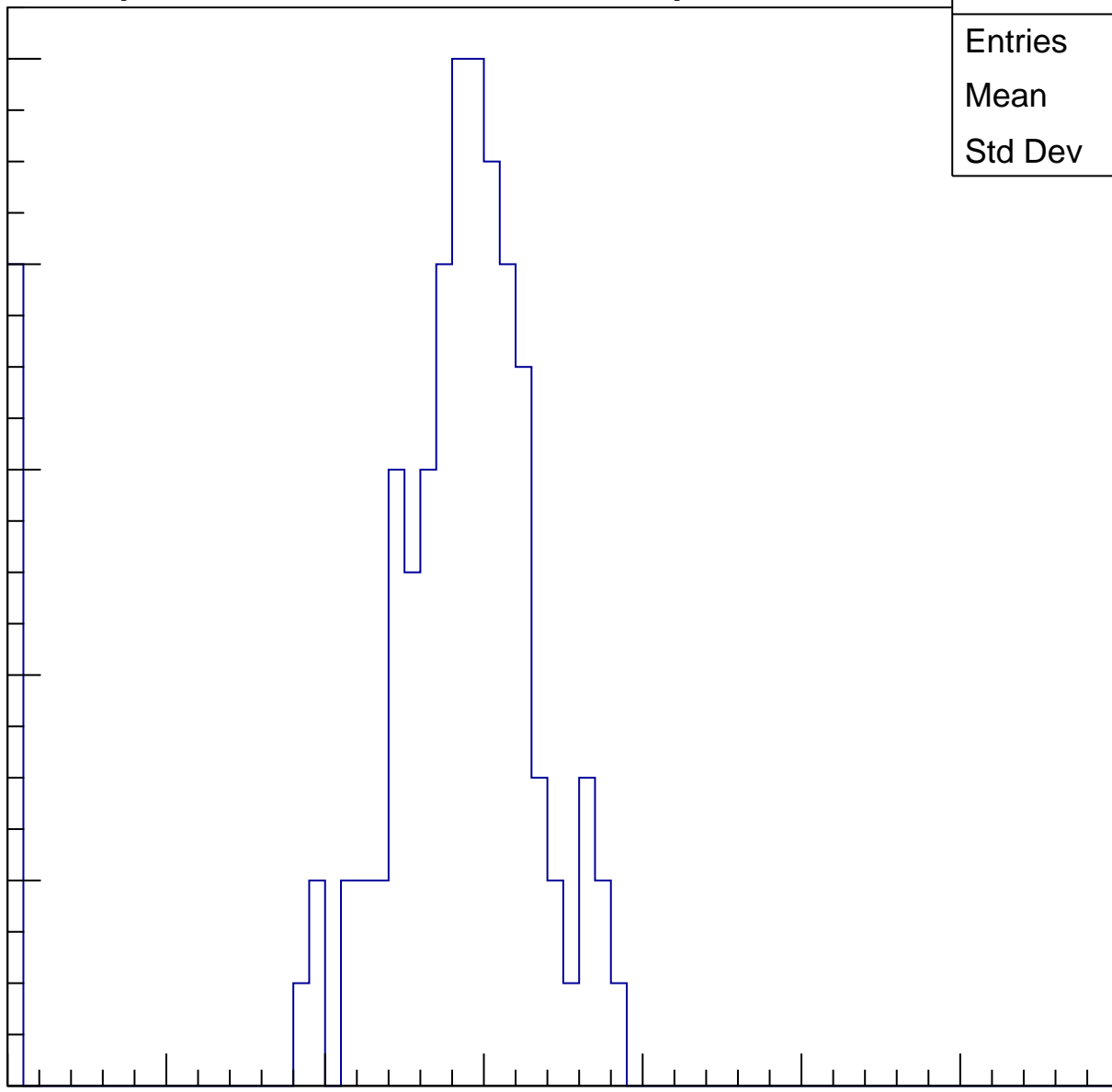
Entries	98
Mean	26.15
Std Dev	8.732

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

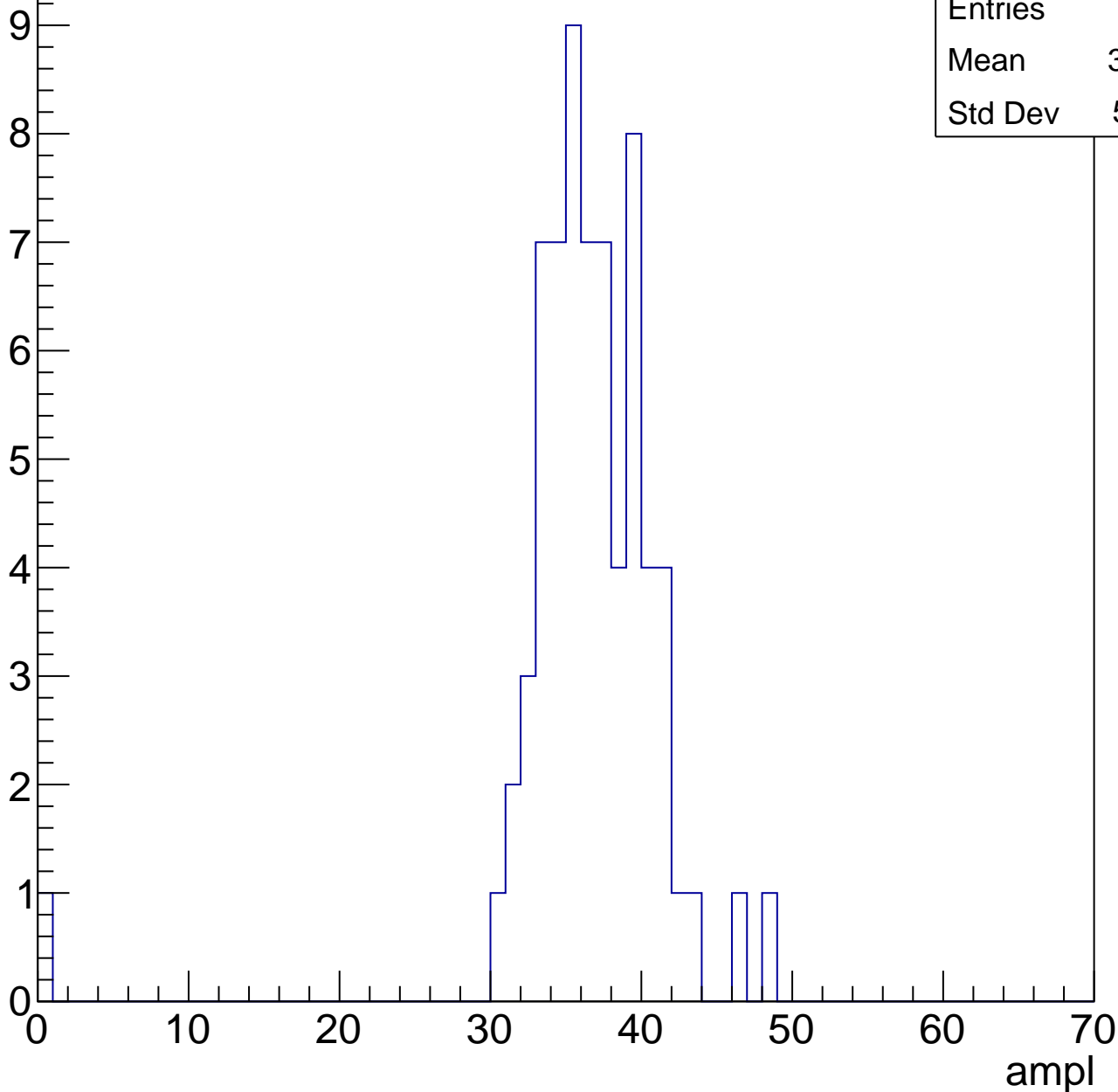


B1L103S, U9-ch9, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	36.03
Std Dev	5.581

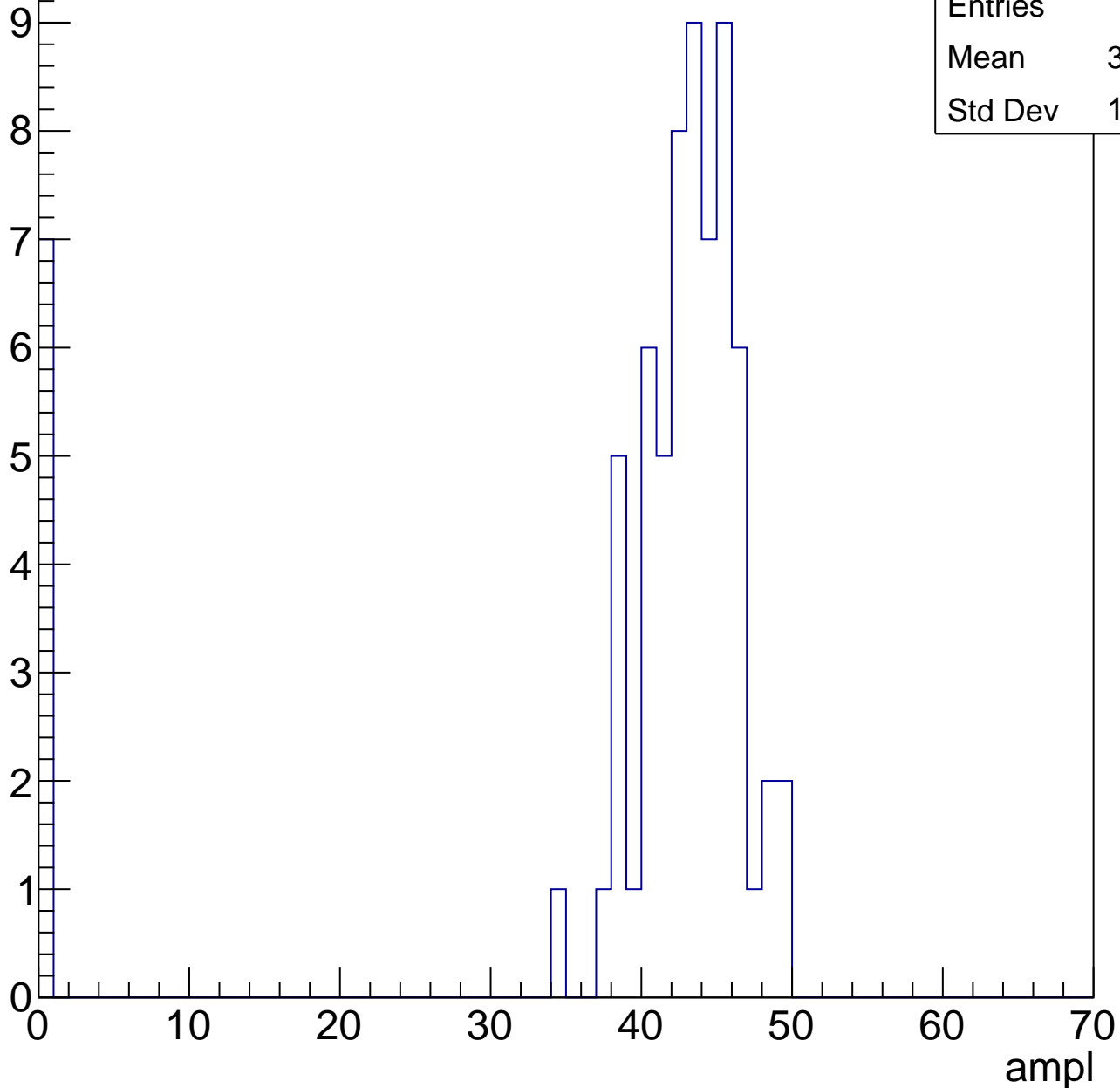


B1L103S, U9-ch9, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	38.54
Std Dev	13.16



B1L103S, U9-ch9, adc3

calib_packv5_041523_1651.root, FC#0, port C2

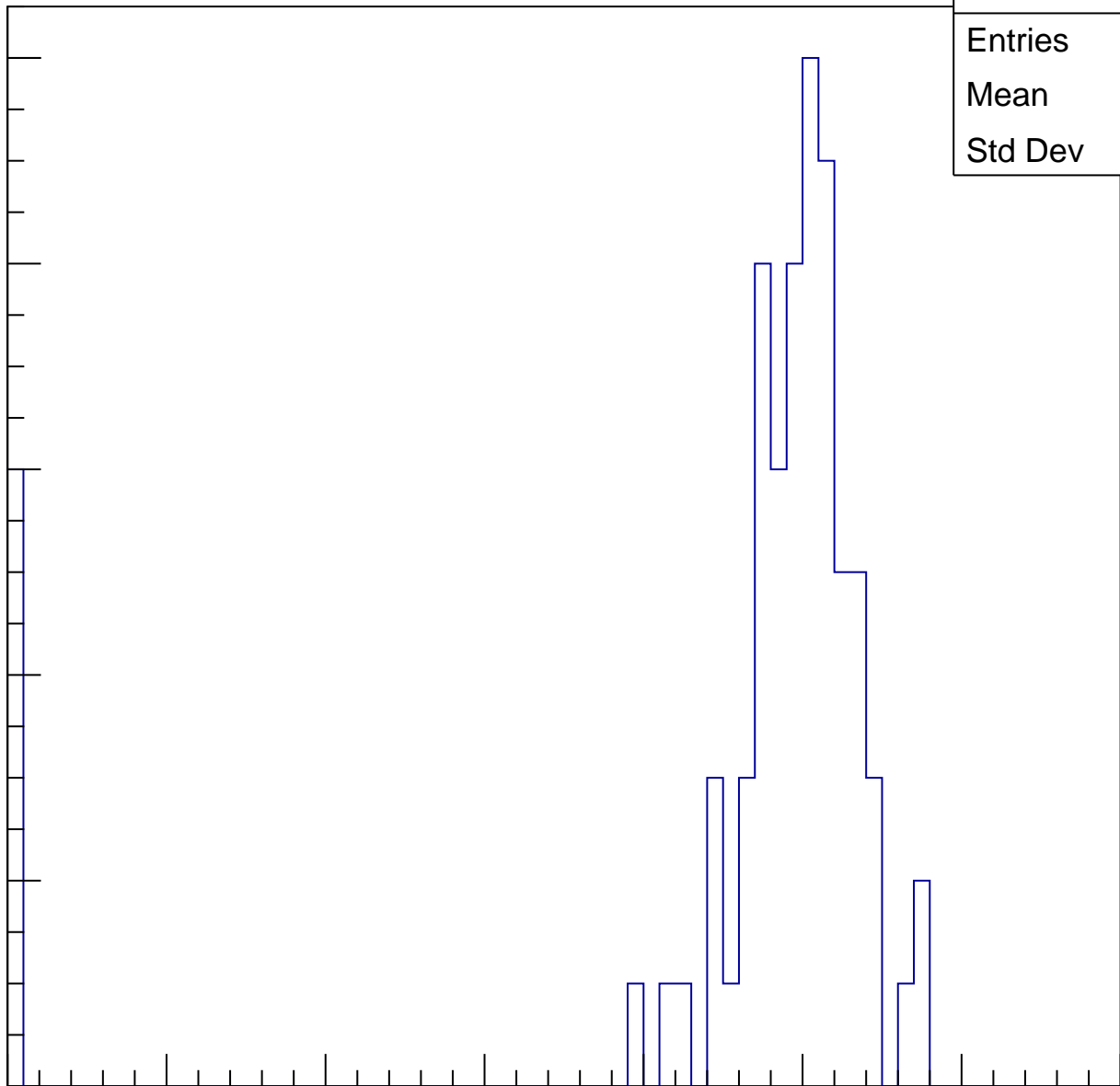
Entries	73
Mean	45.33
Std Dev	13.95

Entry

10
8
6
4
2
0

ampl

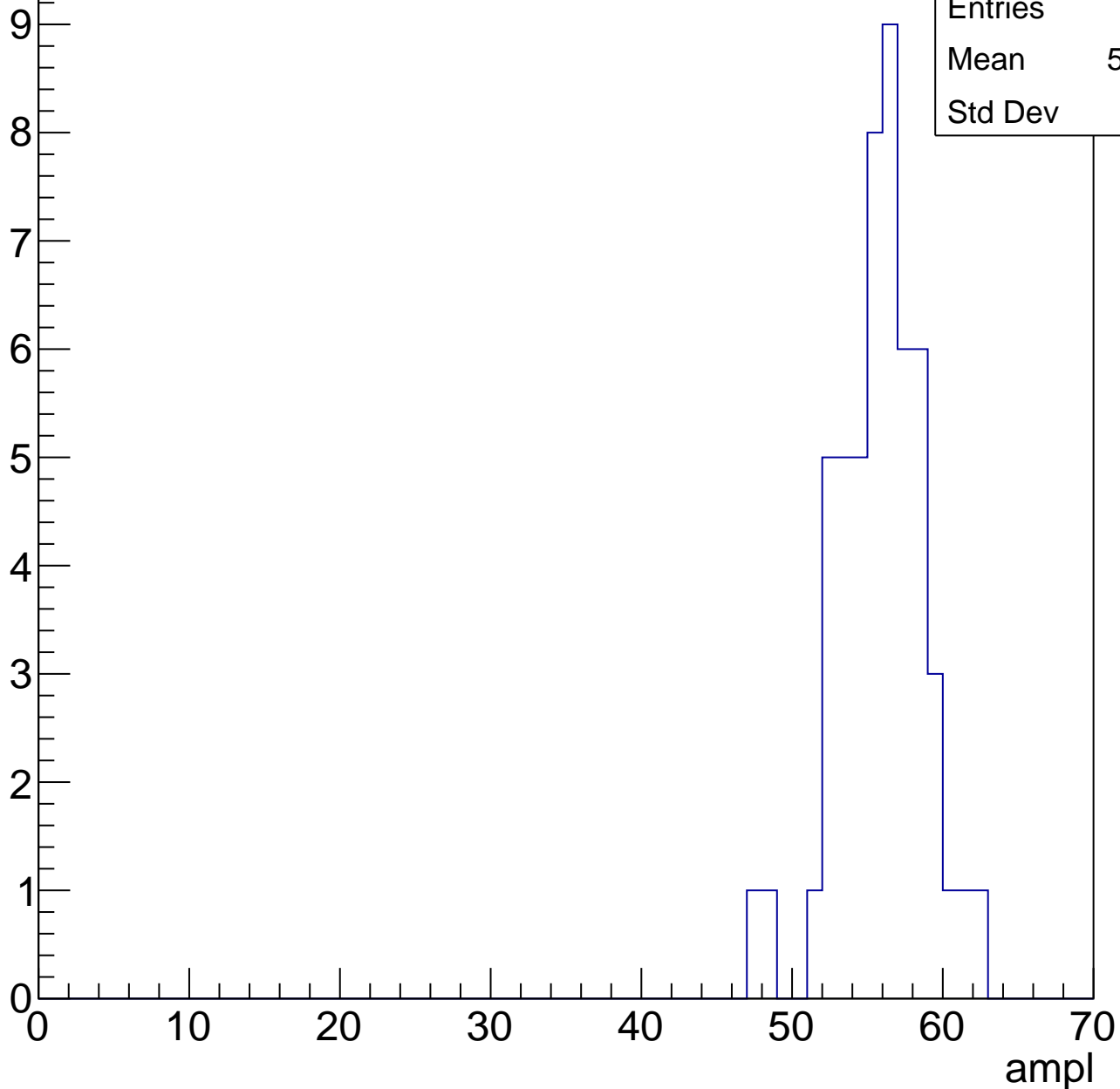
0 10 20 30 40 50 60 70



B1L103S, U9-ch9, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

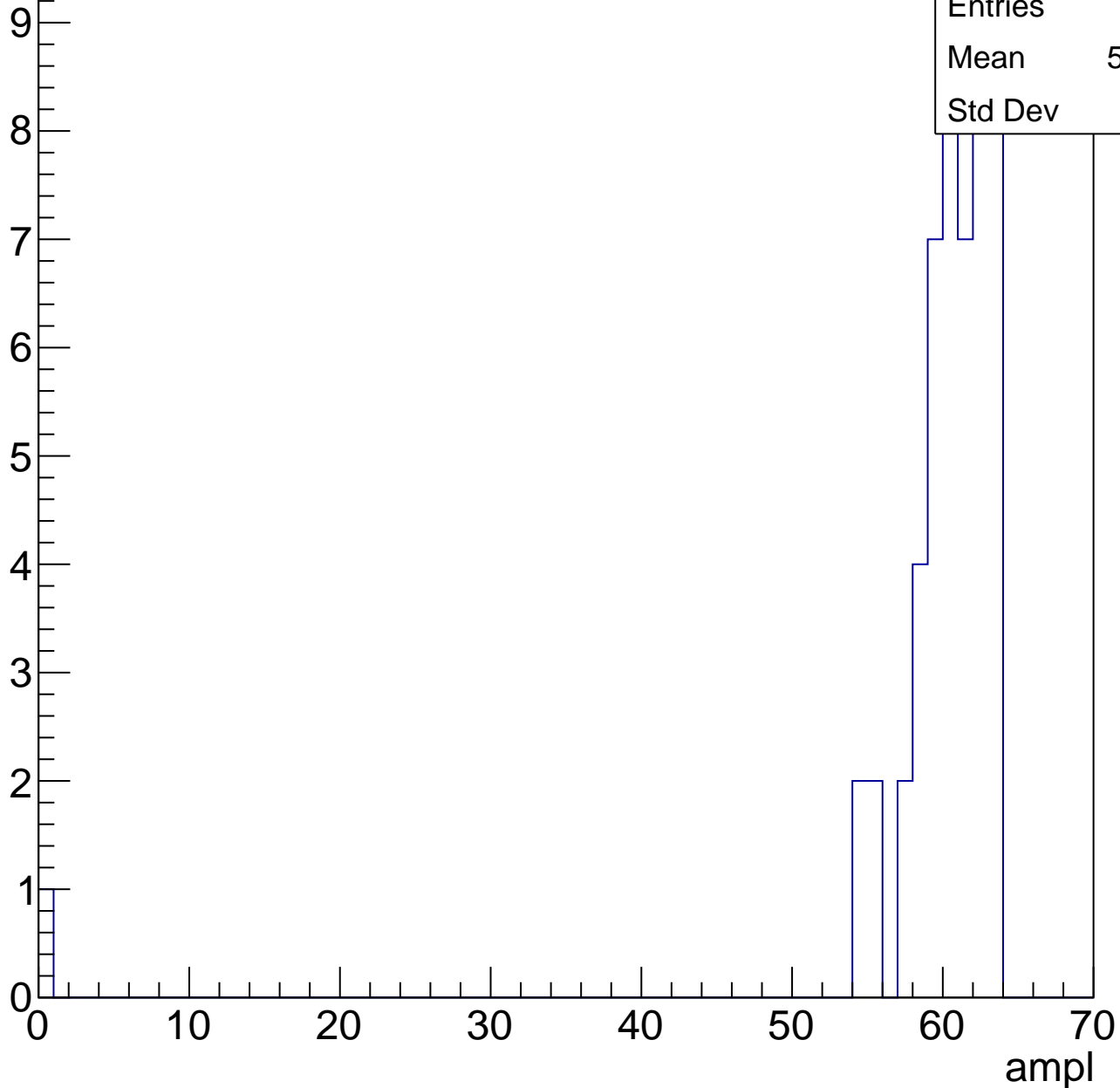


Entries	53
Mean	55.38
Std Dev	2.87

B1L103S, U9-ch9, adc5

calib_packv5_041523_1651.root, FC#0, port C2

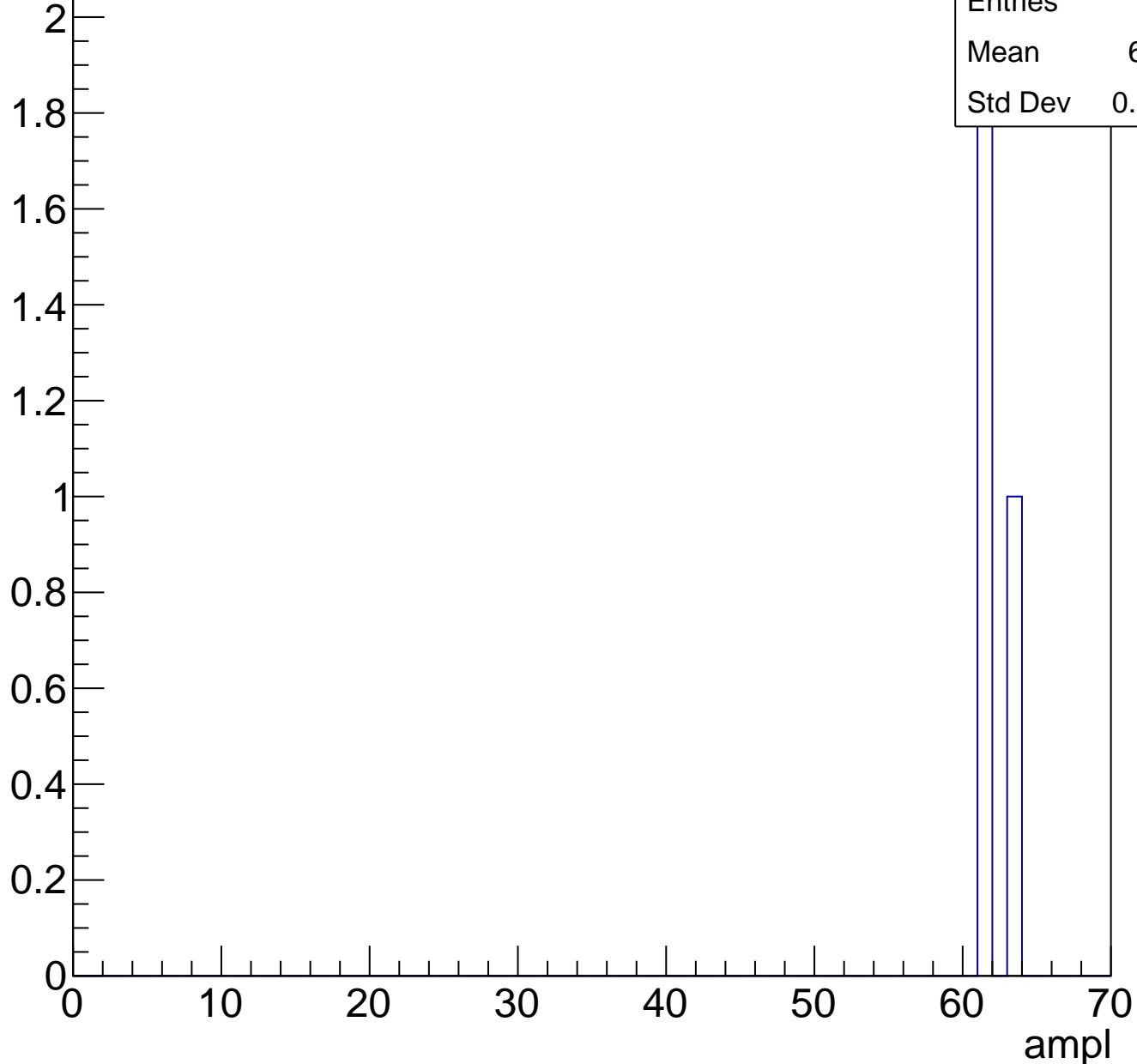
Entry



B1L103S, U9-ch9, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



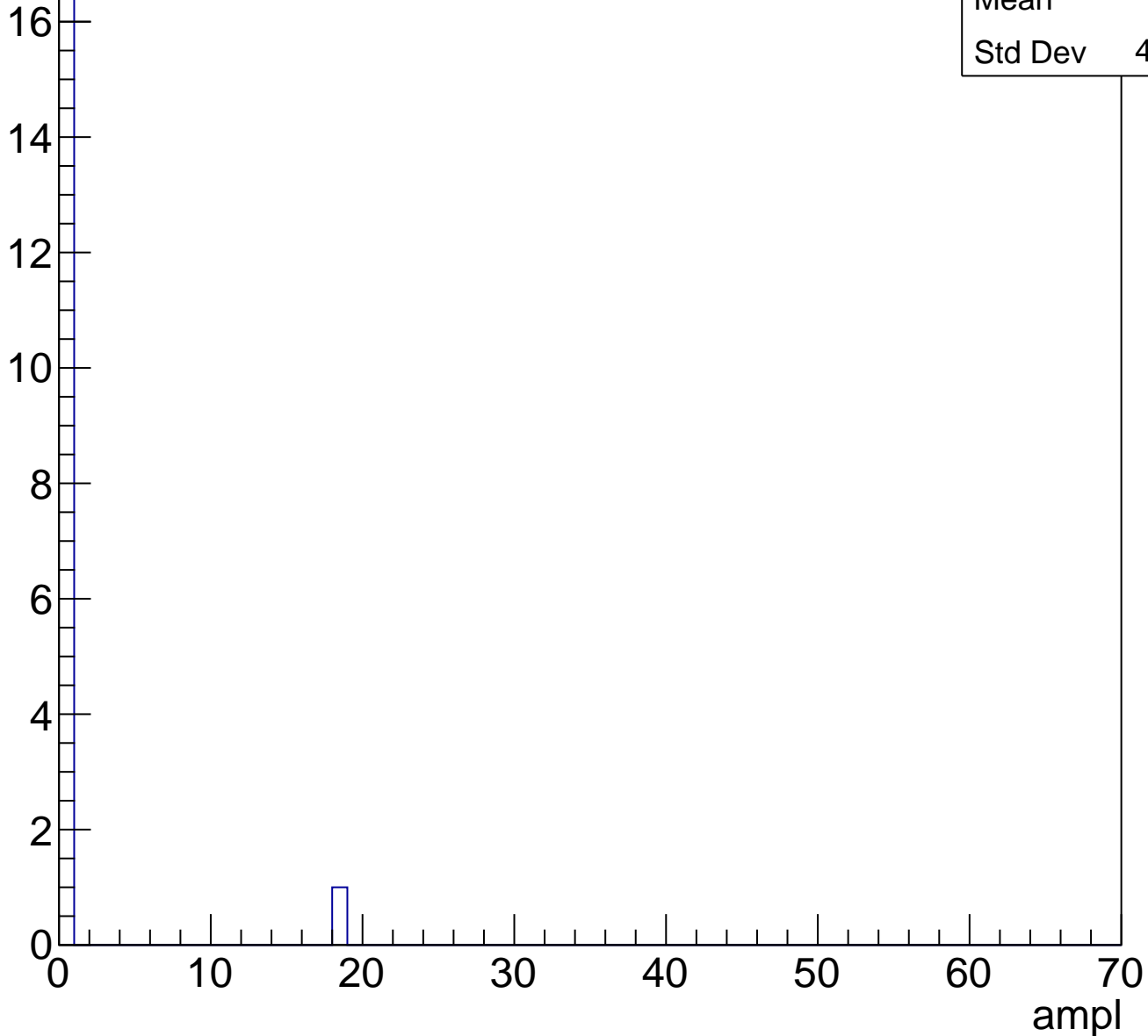
Entries	3
Mean	61.67
Std Dev	0.9428

B1L103S, U9-ch9, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	18
Mean	1
Std Dev	4.123

Entry

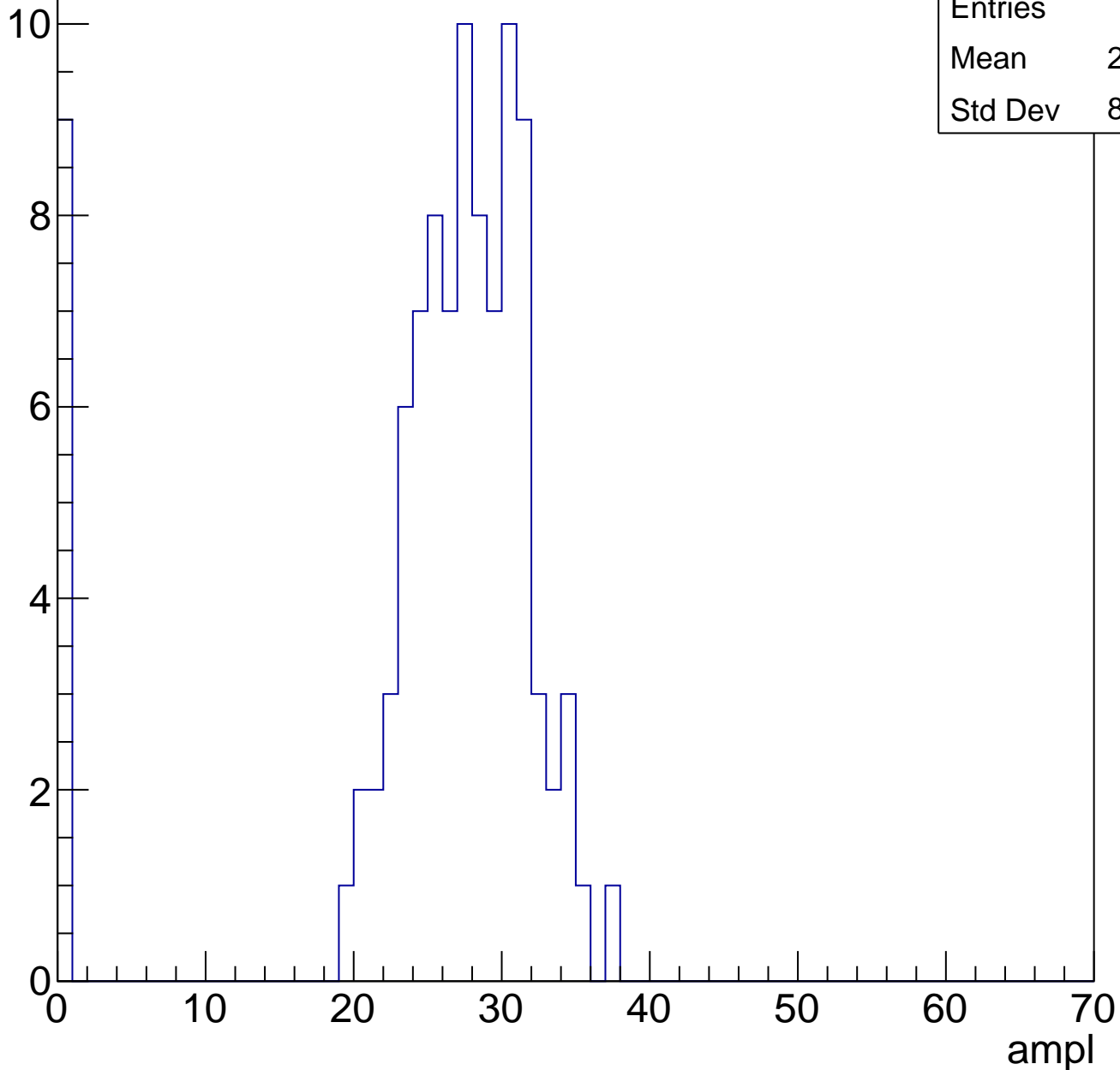


B1L103S, U9-ch10, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	99
Mean	24.92
Std Dev	8.627

Entry

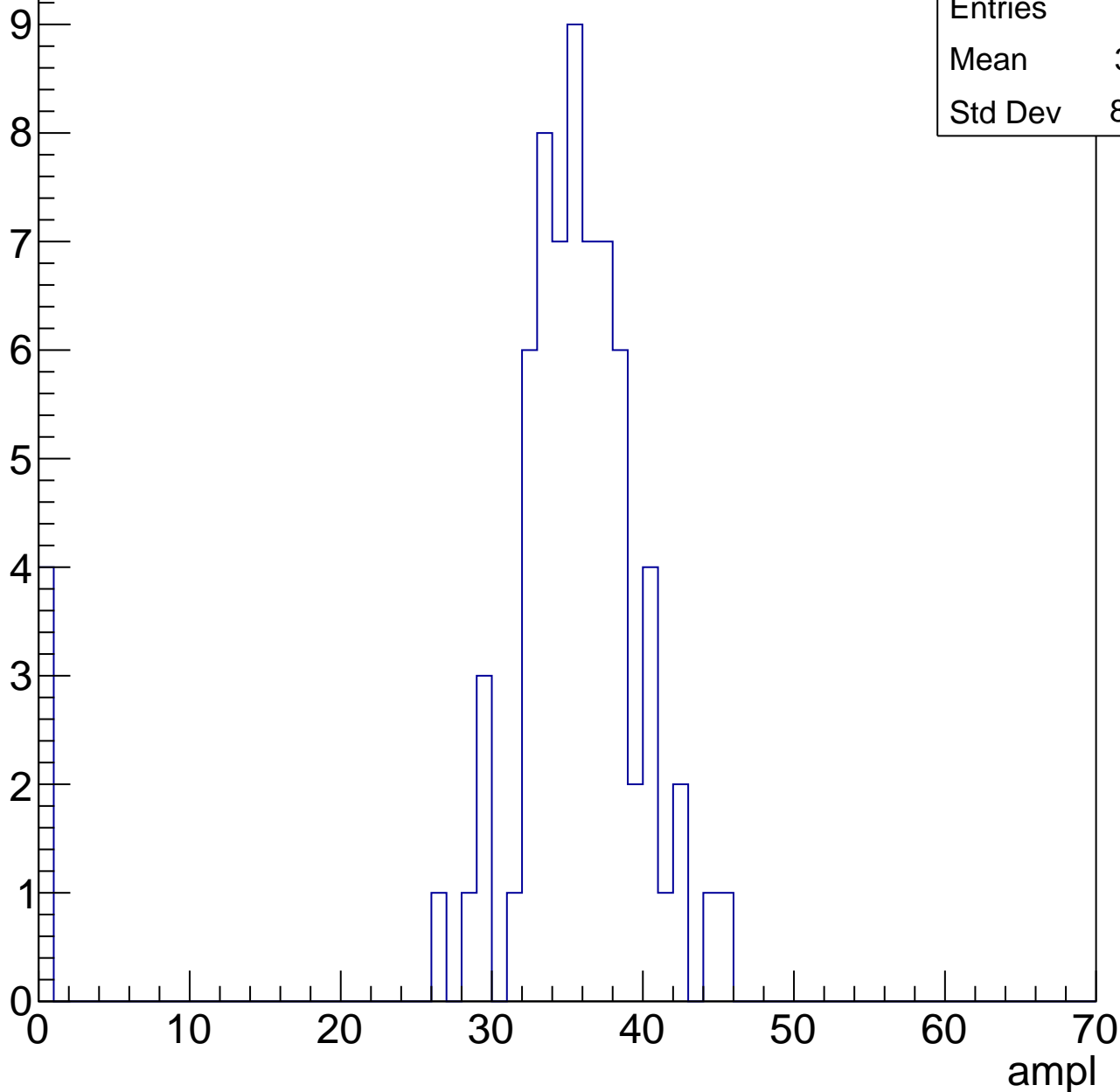


B1L103S, U9-ch10, adc1

calib_packv5_041523_1651.root, FC#0, port C2

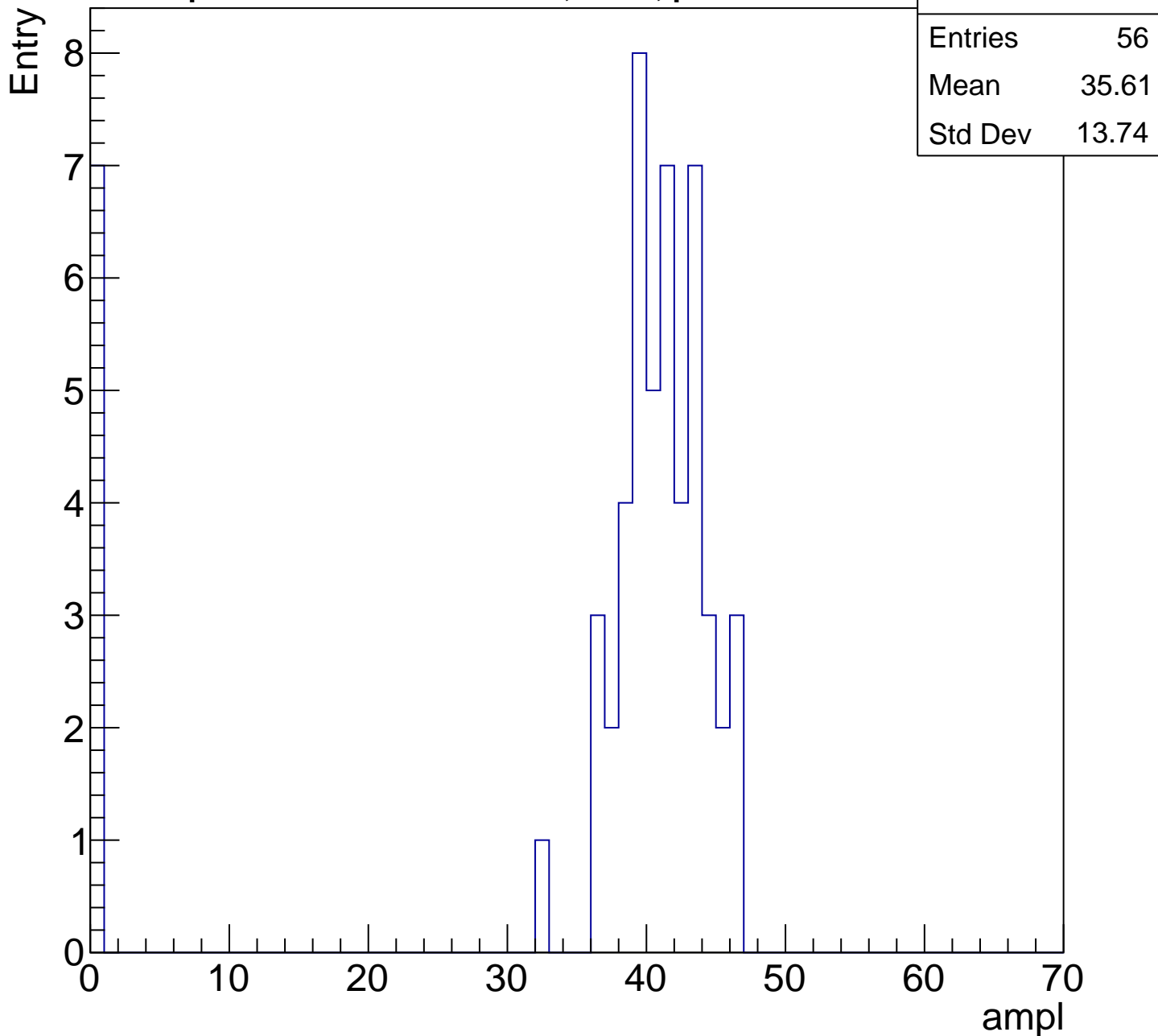
Entry

Entries	71
Mean	33.41
Std Dev	8.884



B1L103S, U9-ch10, adc2

calib_packv5_041523_1651.root, FC#0, port C2

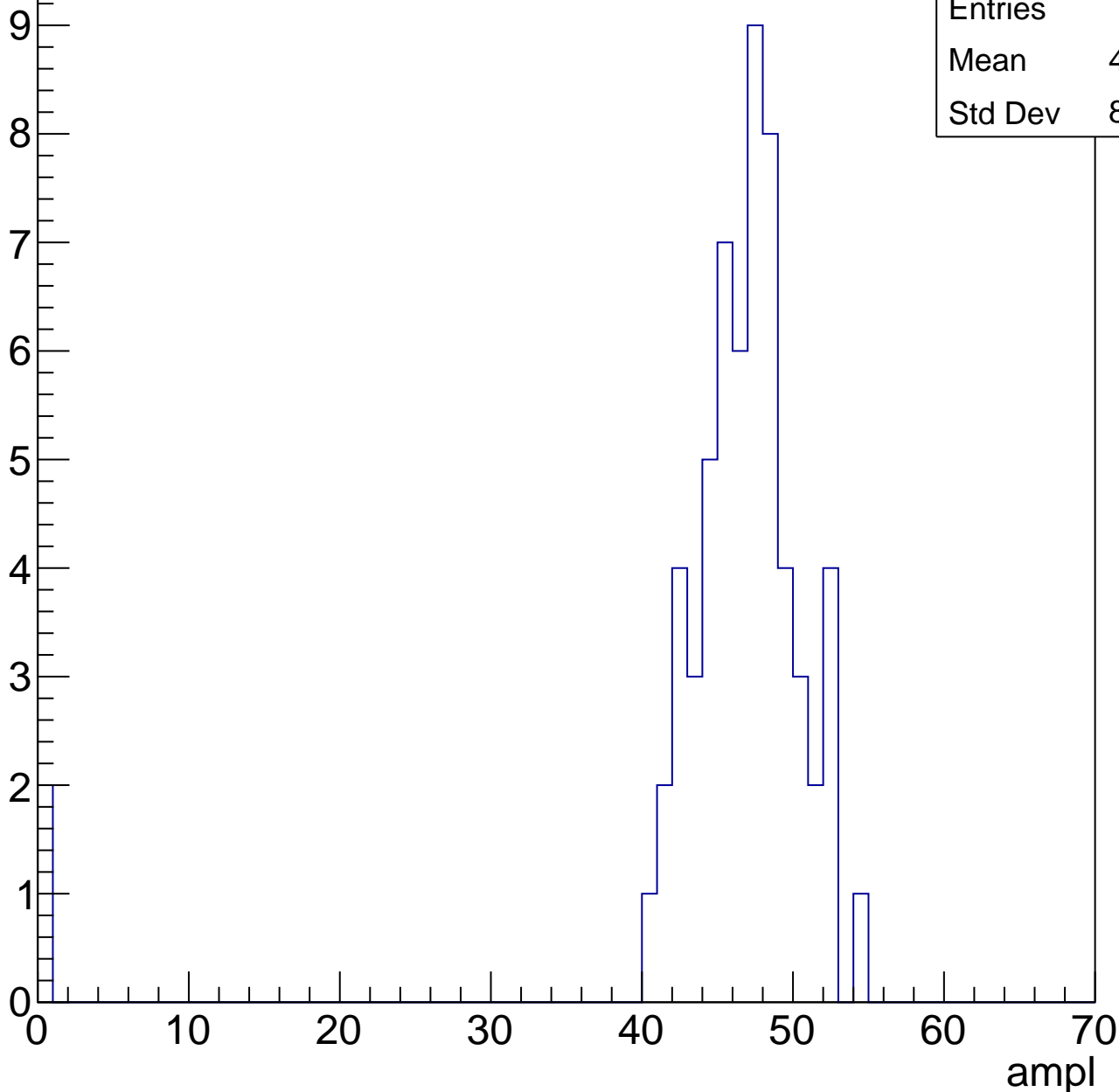


B1L103S, U9-ch10, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	45.03
Std Dev	8.835

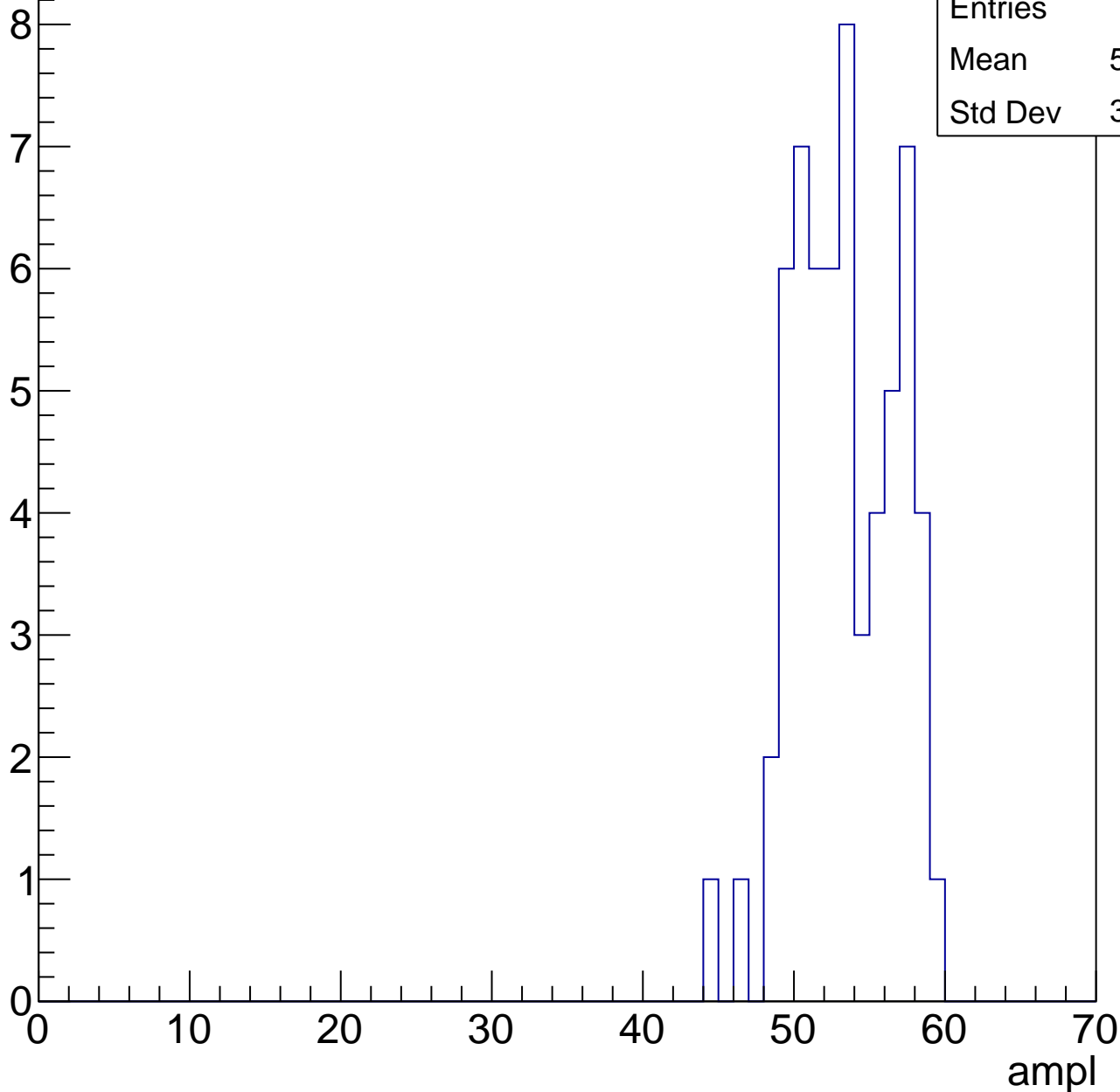


B1L103S, U9-ch10, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	52.85
Std Dev	3.338

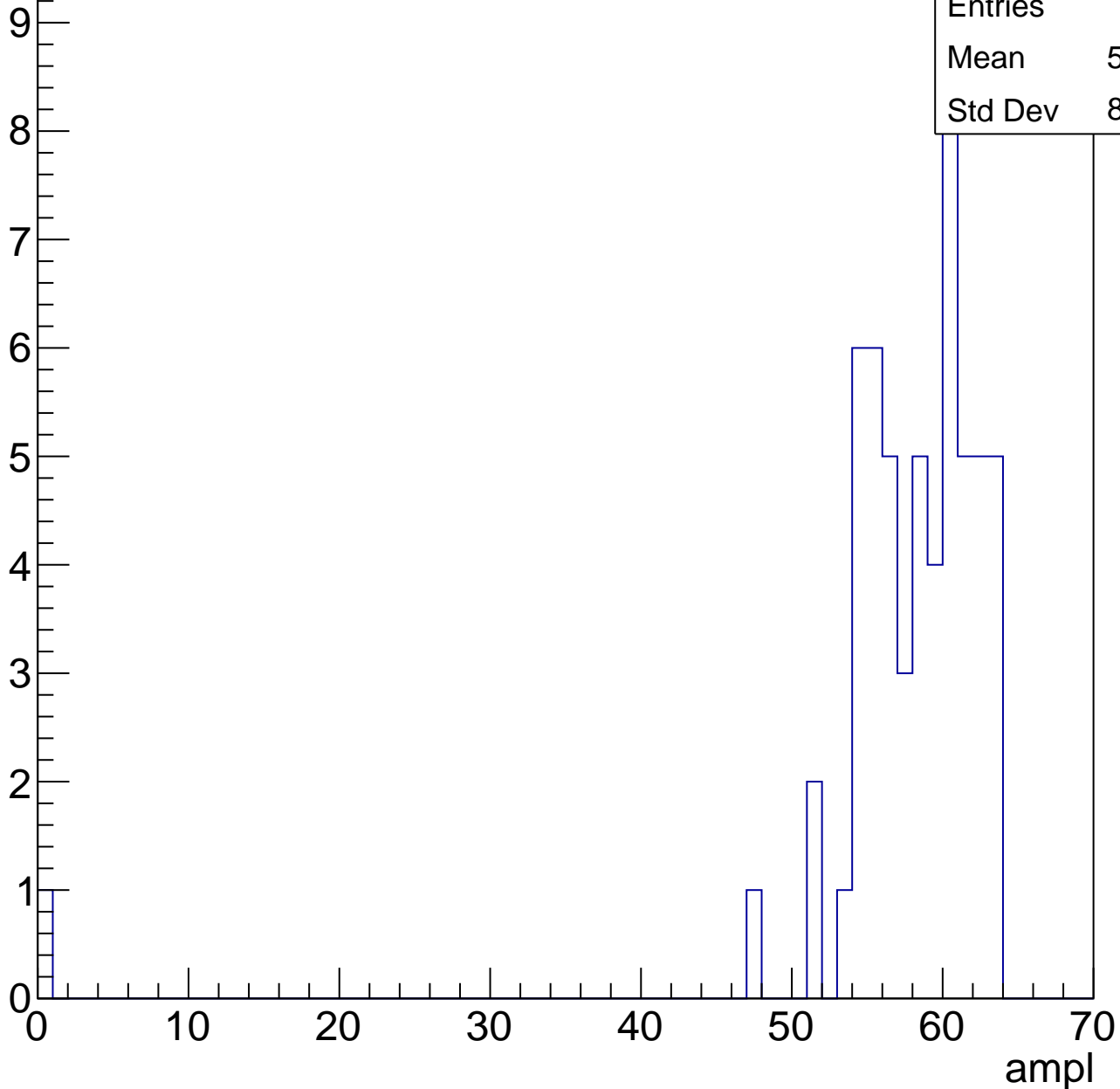


B1L103S, U9-ch10, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

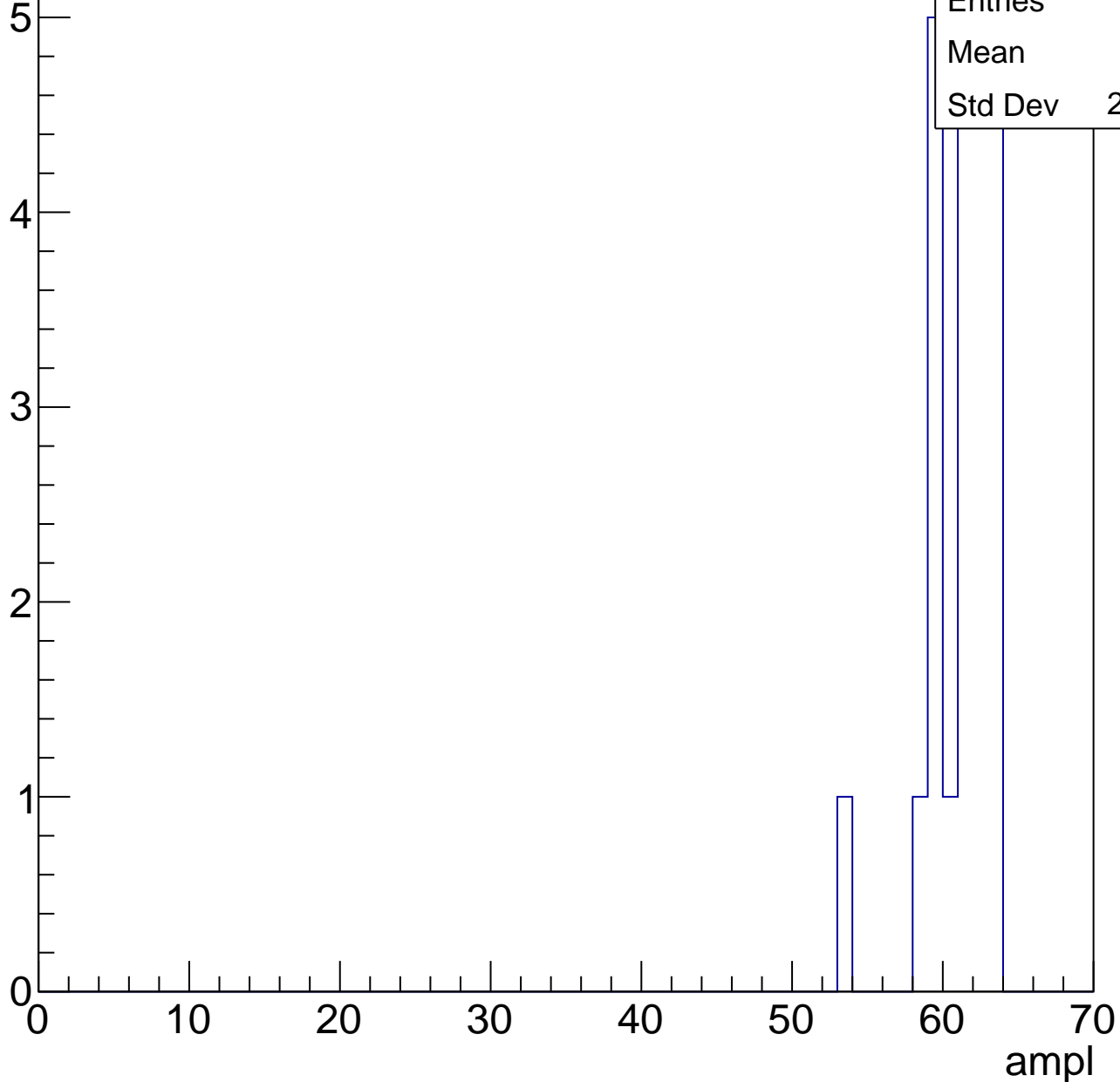
Entries	58
Mean	56.95
Std Dev	8.312



B1L103S, U9-ch10, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch10, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

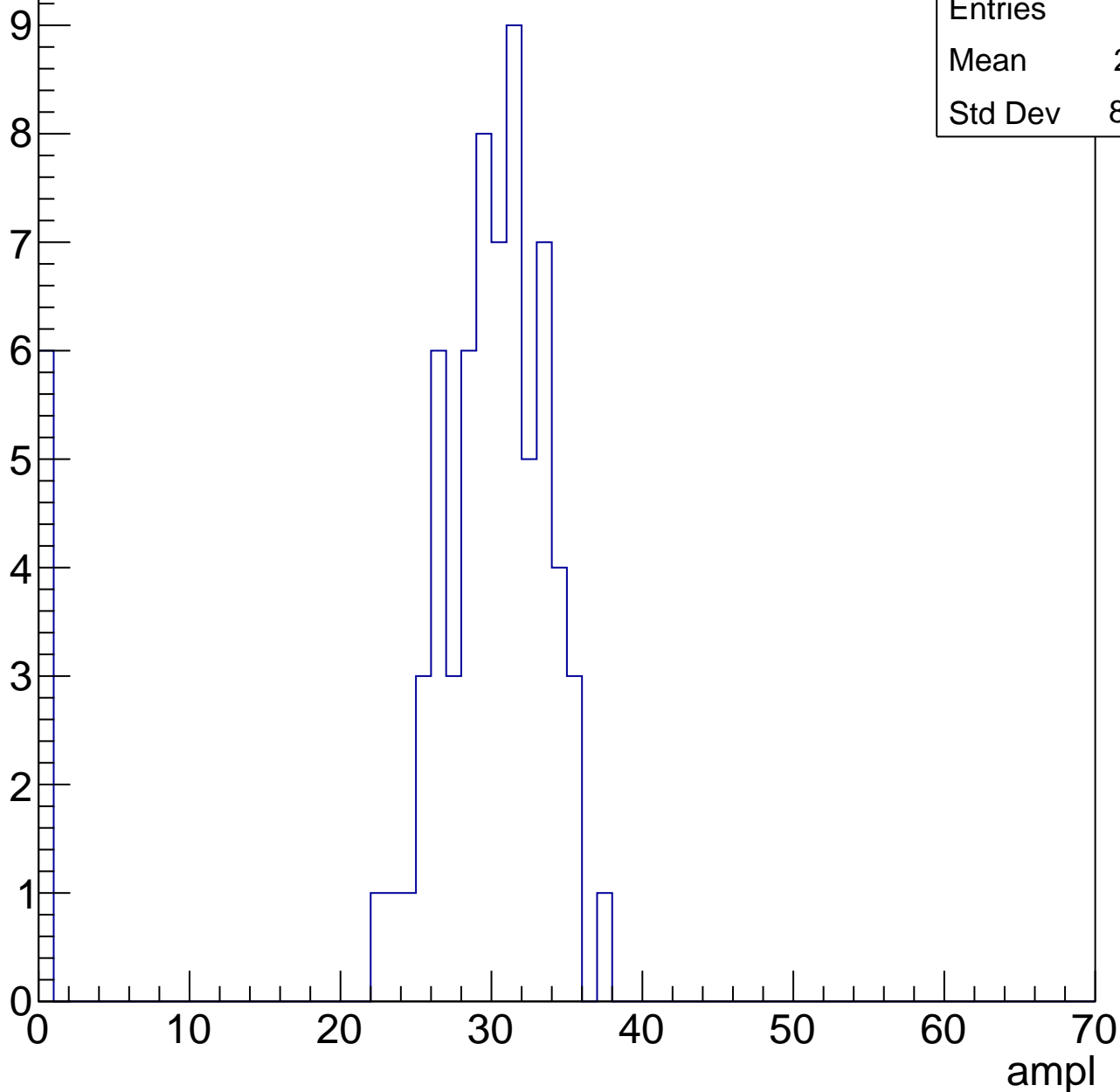
ampl

B1L103S, U9-ch11, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	27.31
Std Dev	8.837

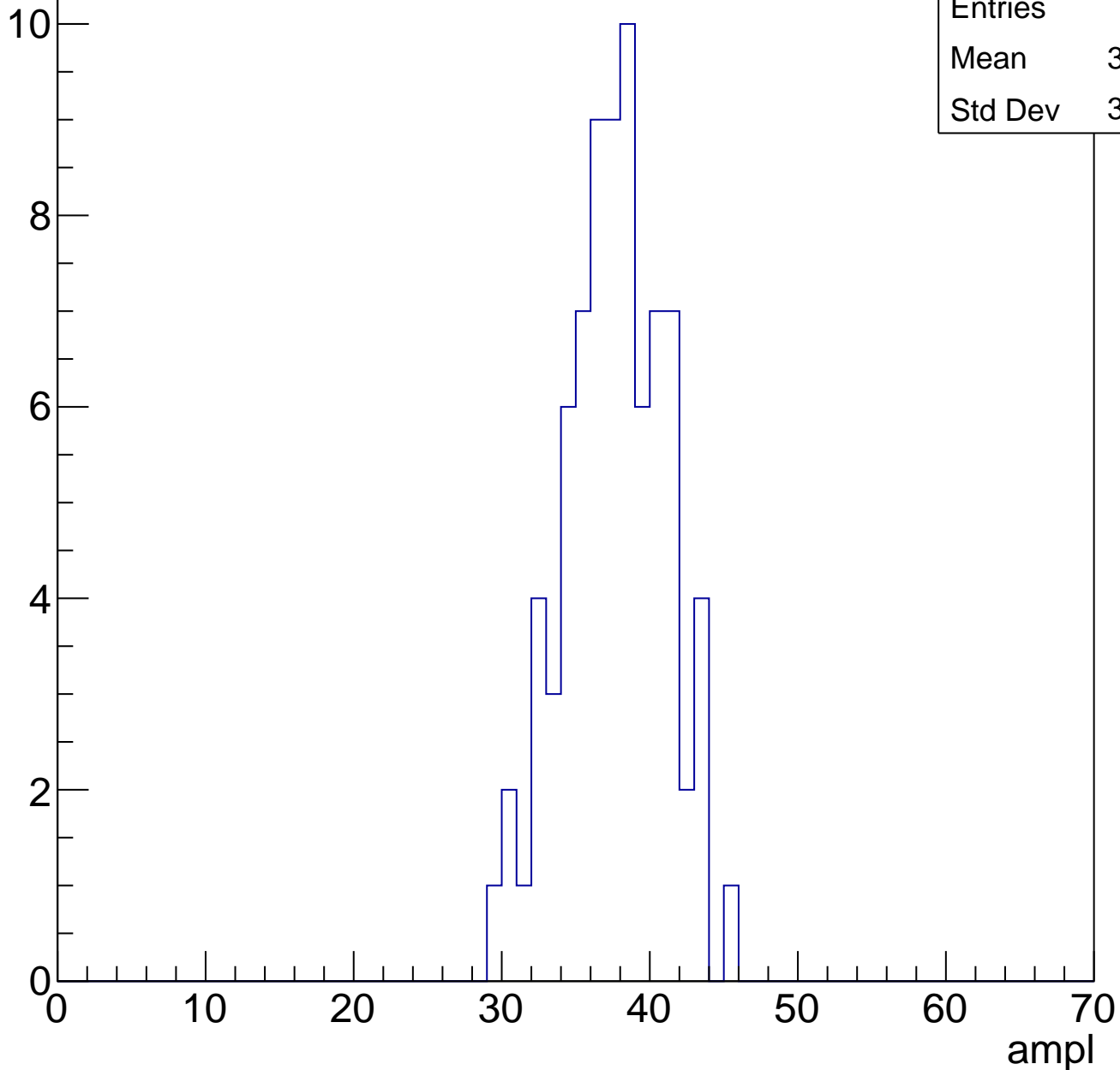


B1L103S, U9-ch11, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	79
Mean	37.15
Std Dev	3.379

Entry

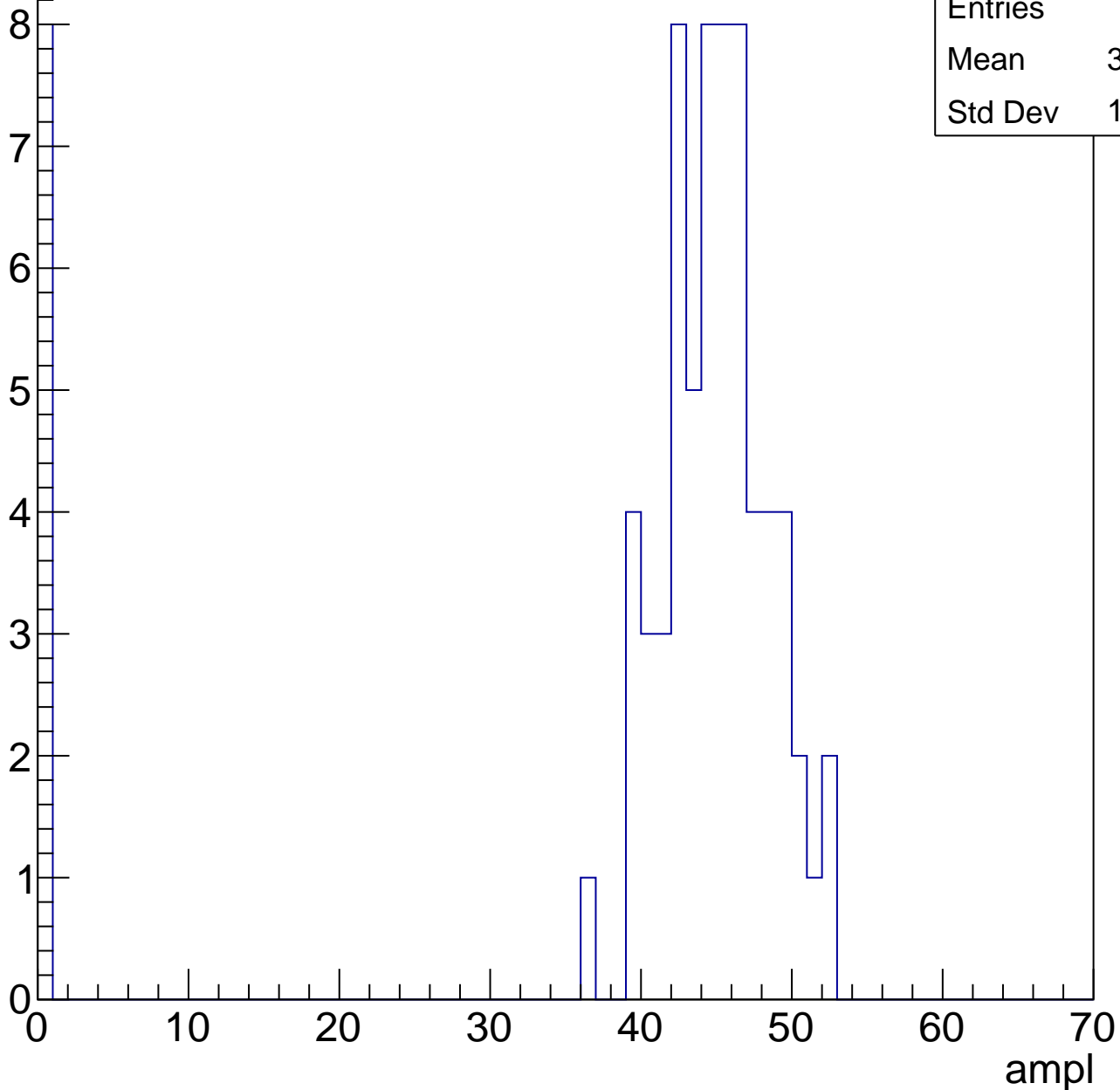


B1L103S, U9-ch11, adc2

calib_packv5_041523_1651.root, FC#0, port C2

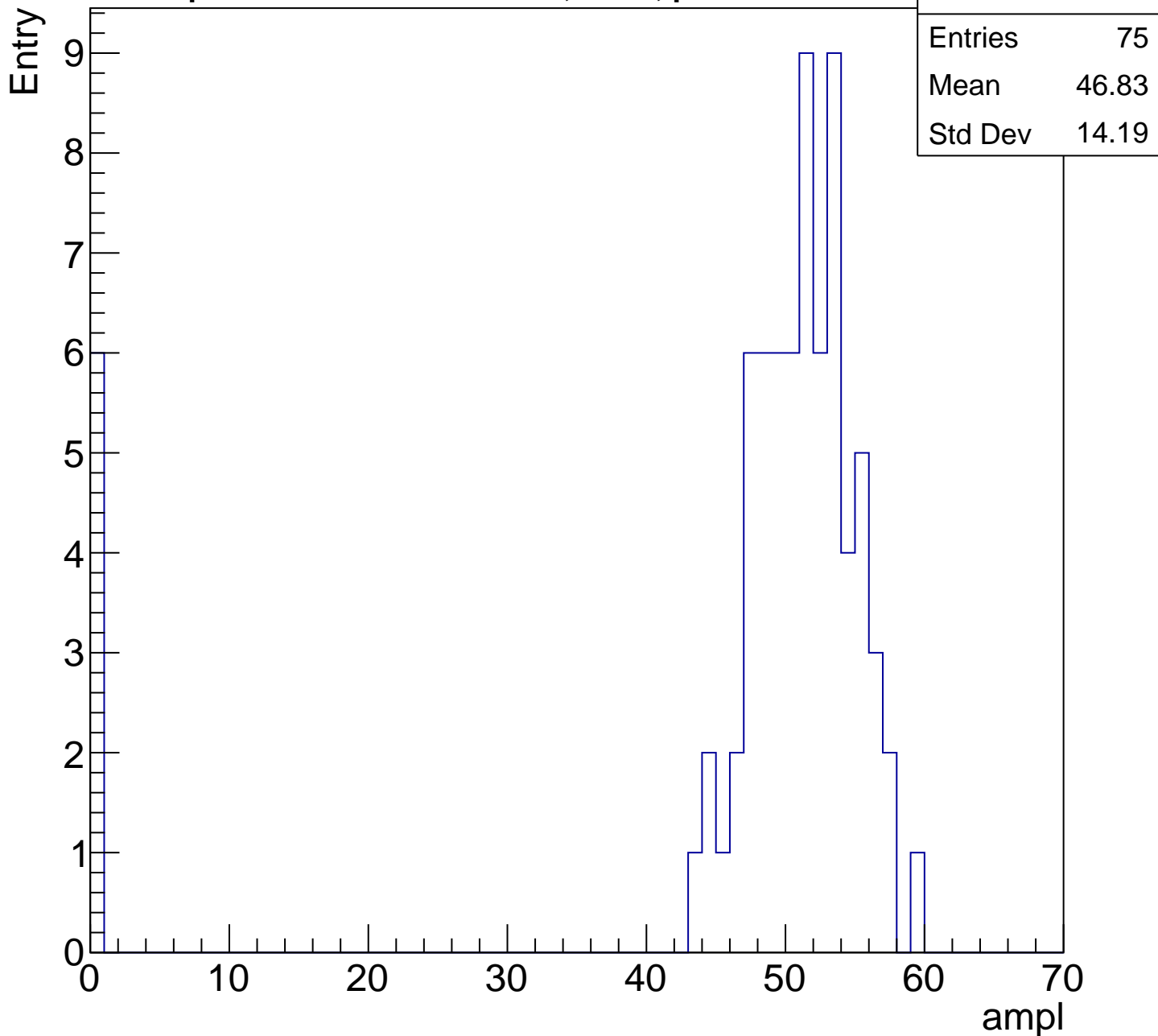
Entry

Entries	73
Mean	39.68
Std Dev	14.28



B1L103S, U9-ch11, adc3

calib_packv5_041523_1651.root, FC#0, port C2

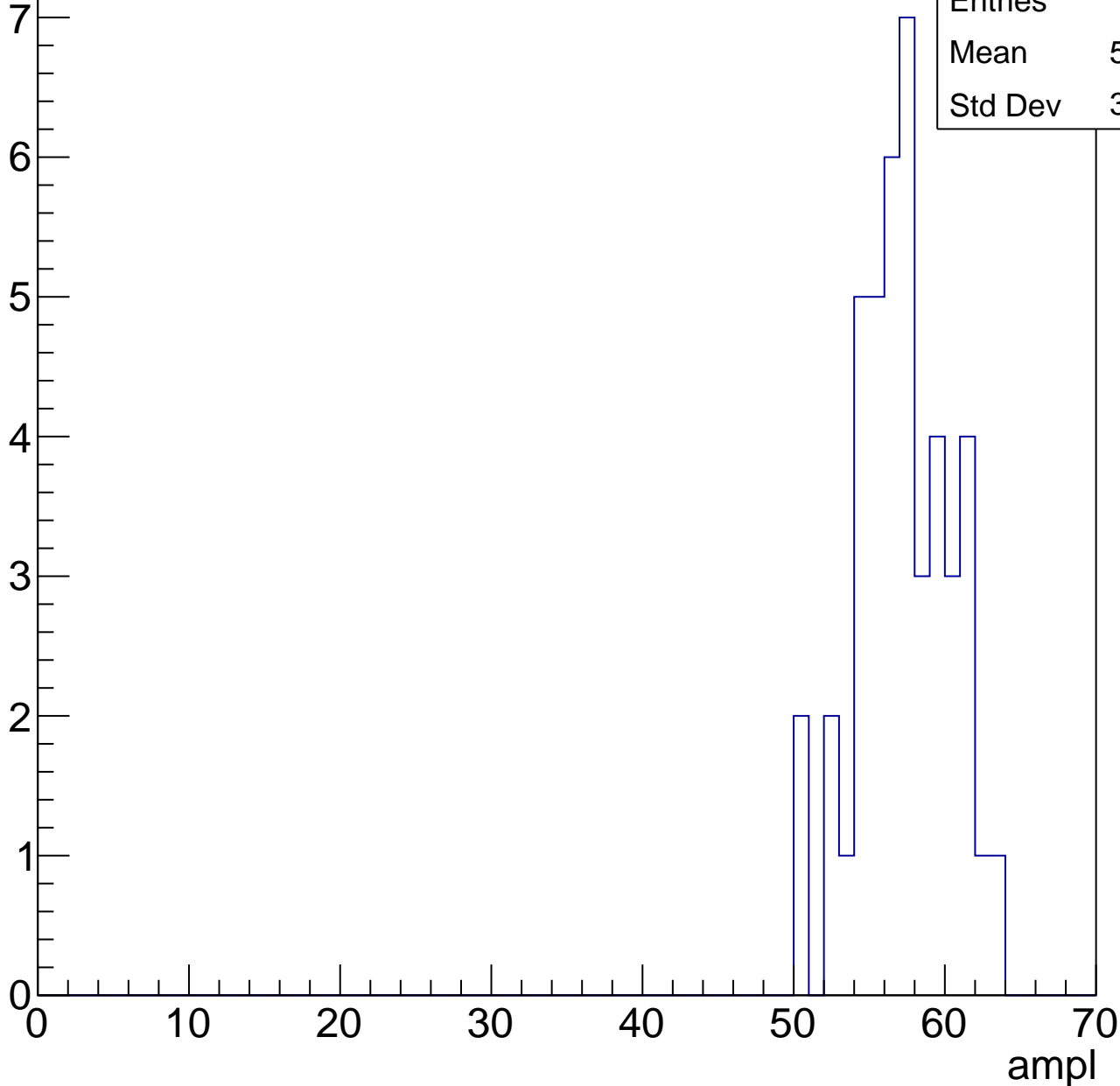


B1L103S, U9-ch11, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	44
Mean	56.73
Std Dev	3.025

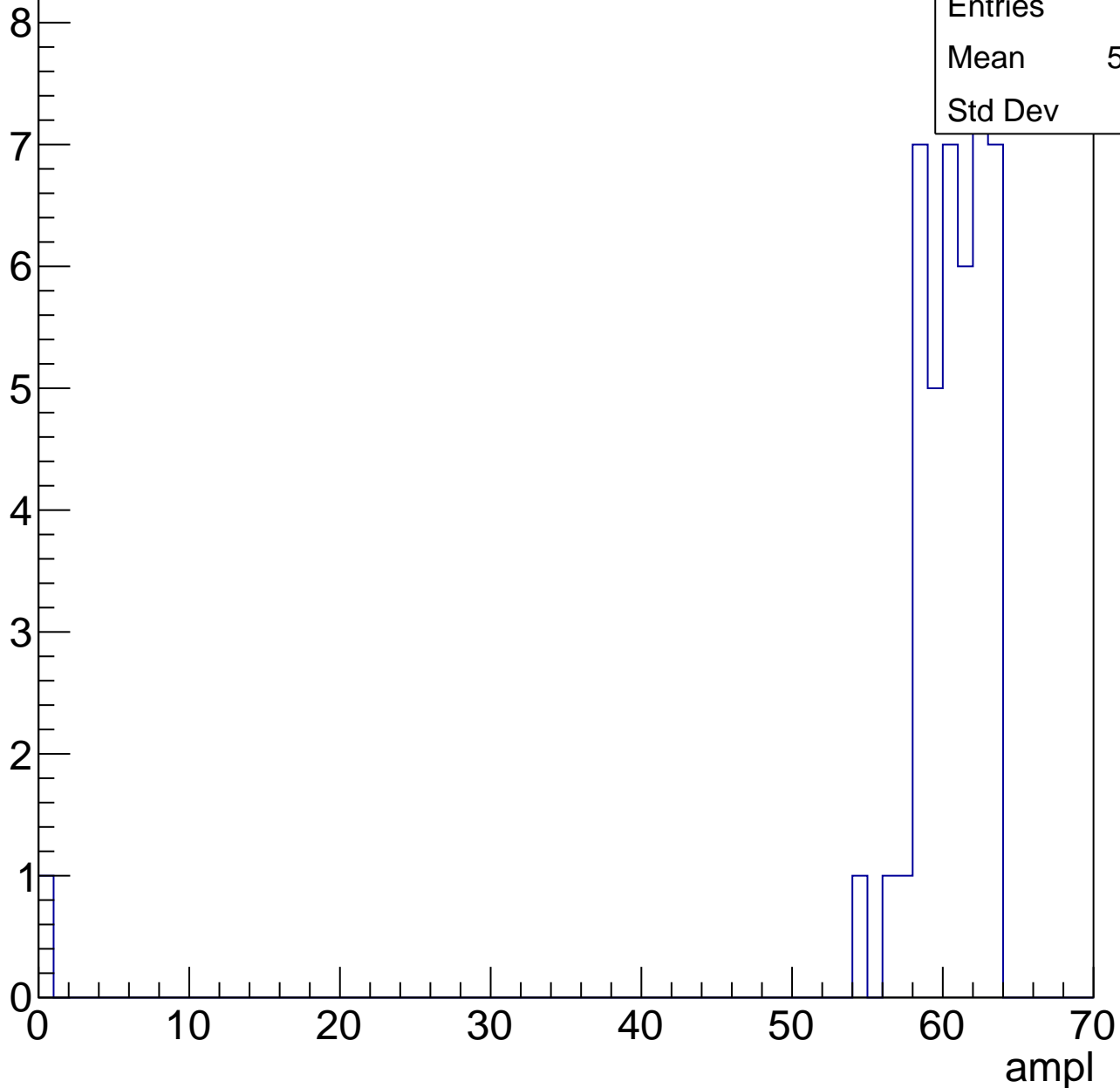


B1L103S, U9-ch11, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	44
Mean	58.89
Std Dev	9.22



B1L103S, U9-ch11, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch11, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

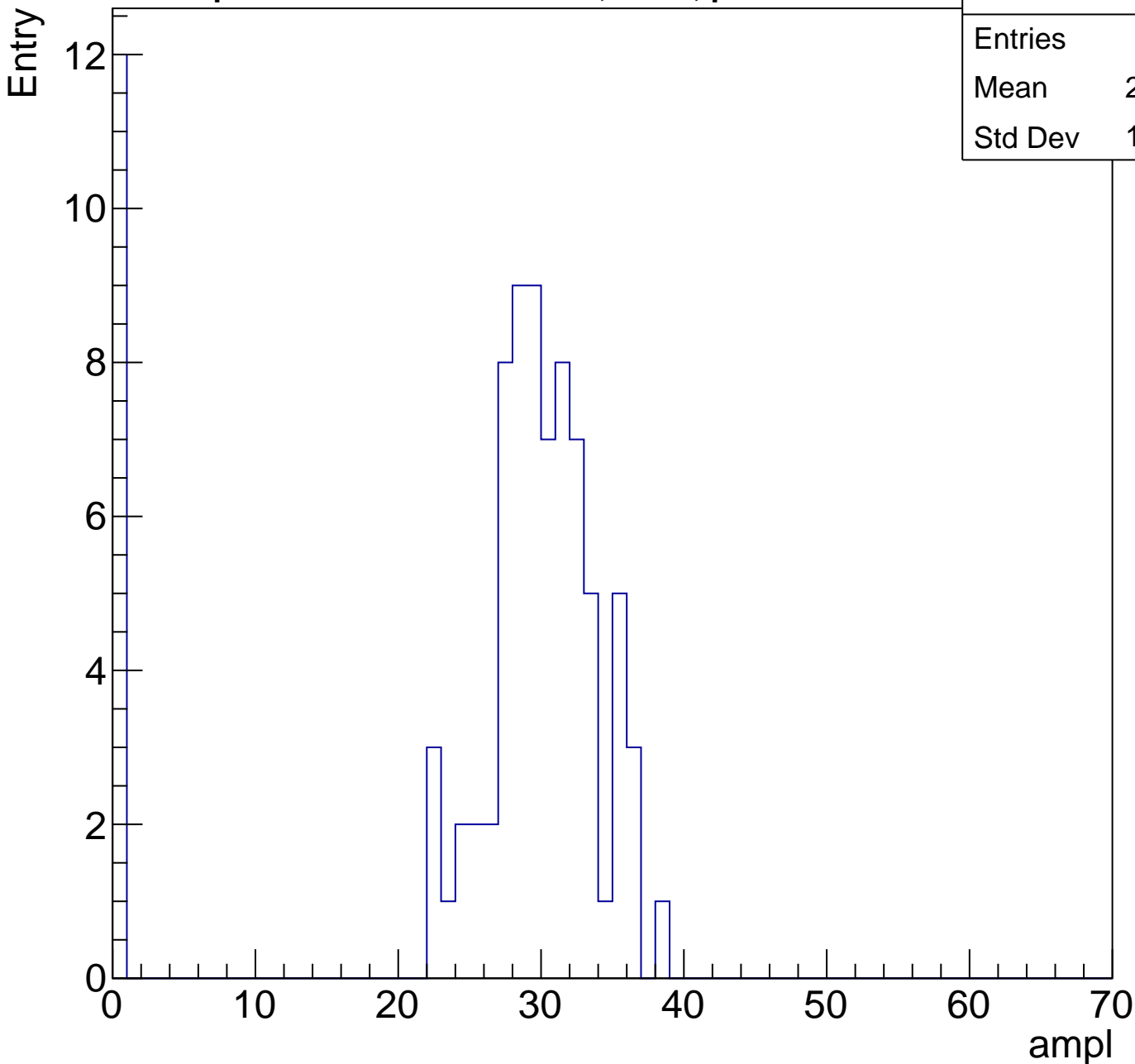
Entries	18
Mean	0
Std Dev	0

ampl

B1L103S, U9-ch12, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	85
Mean	25.53
Std Dev	10.85



B1L103S, U9-ch12, adc1

calib_packv5_041523_1651.root, FC#0, port C2

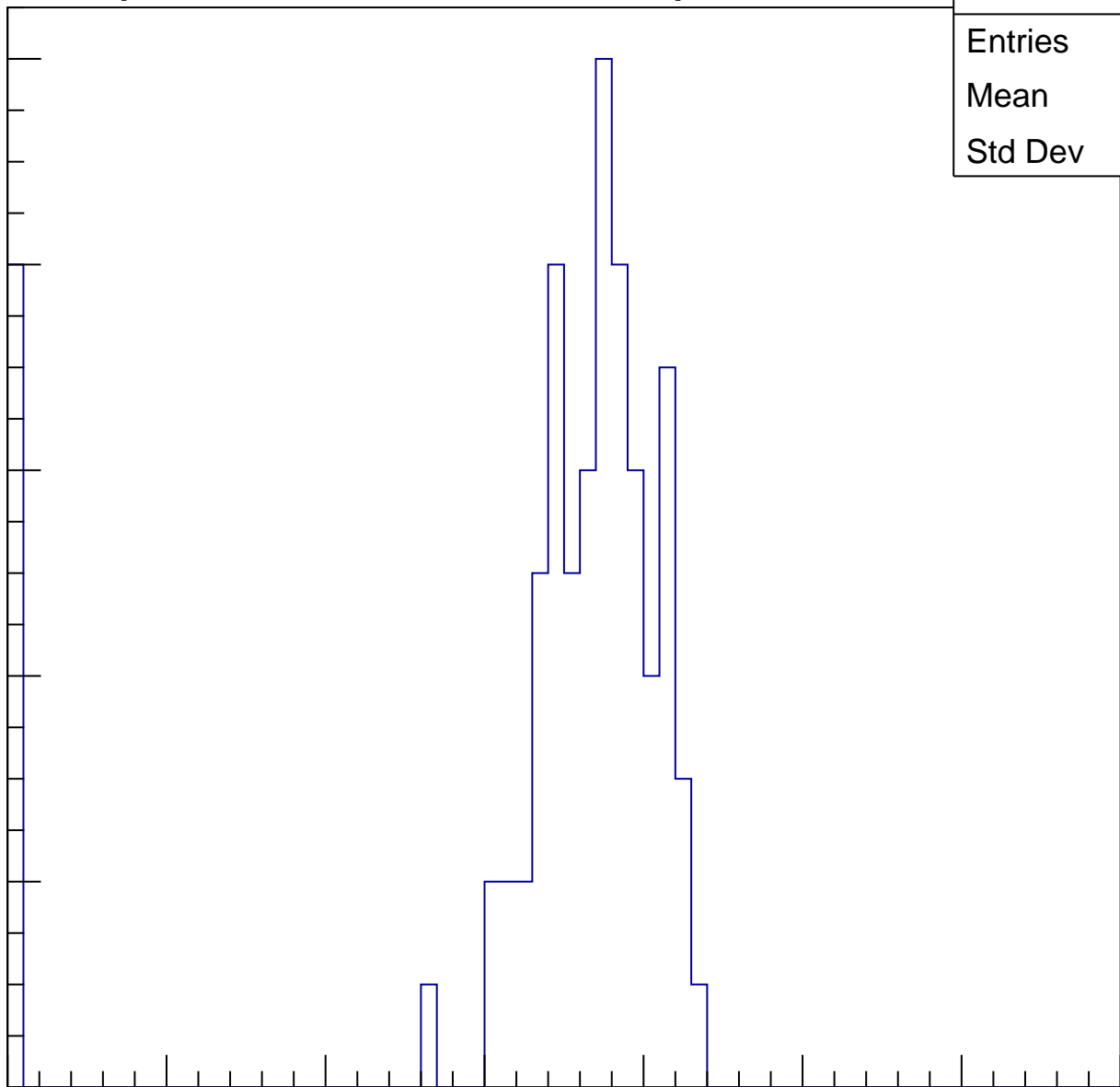
Entries	78
Mean	32.87
Std Dev	11.57

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

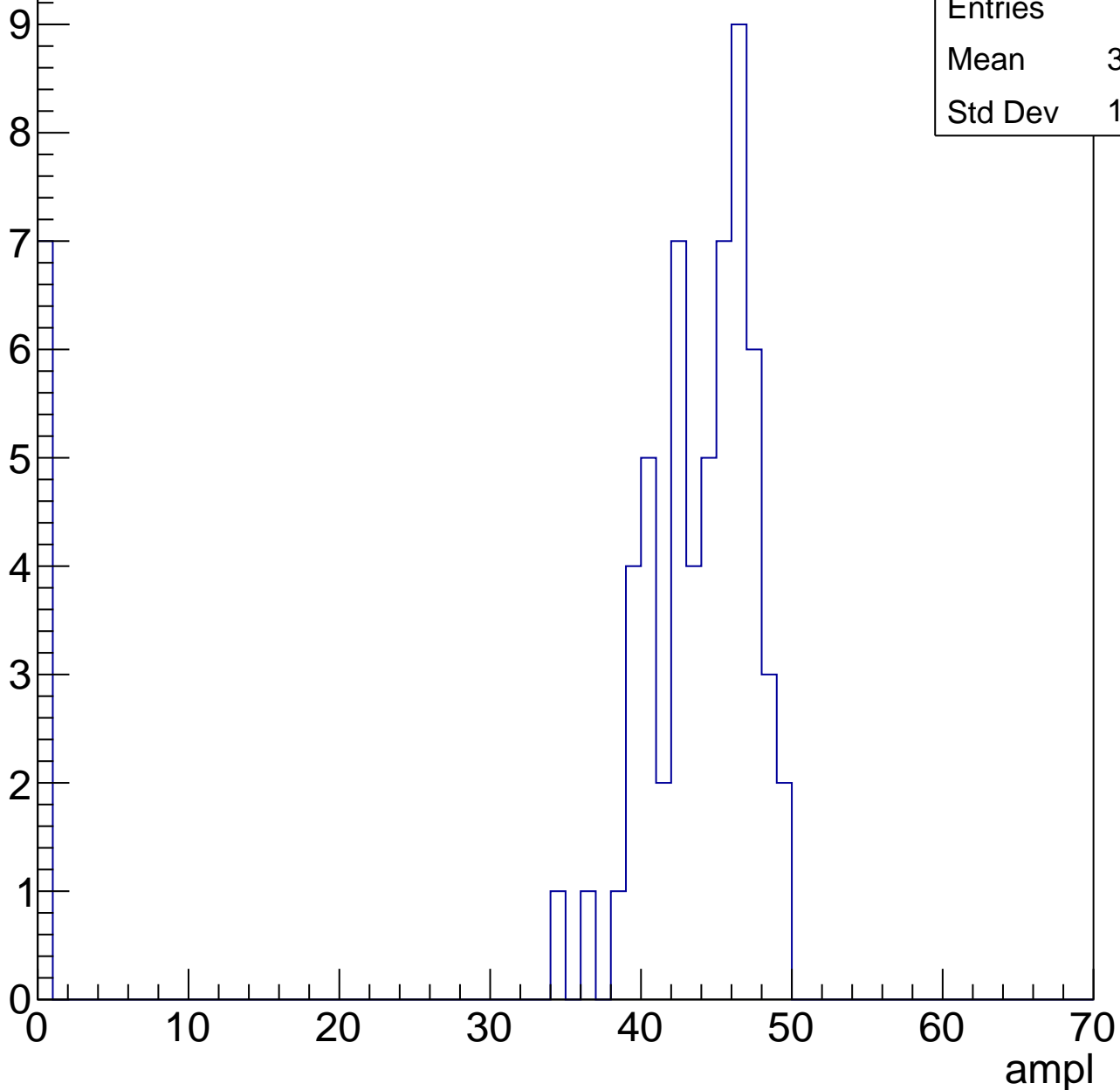


B1L103S, U9-ch12, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	38.83
Std Dev	13.96

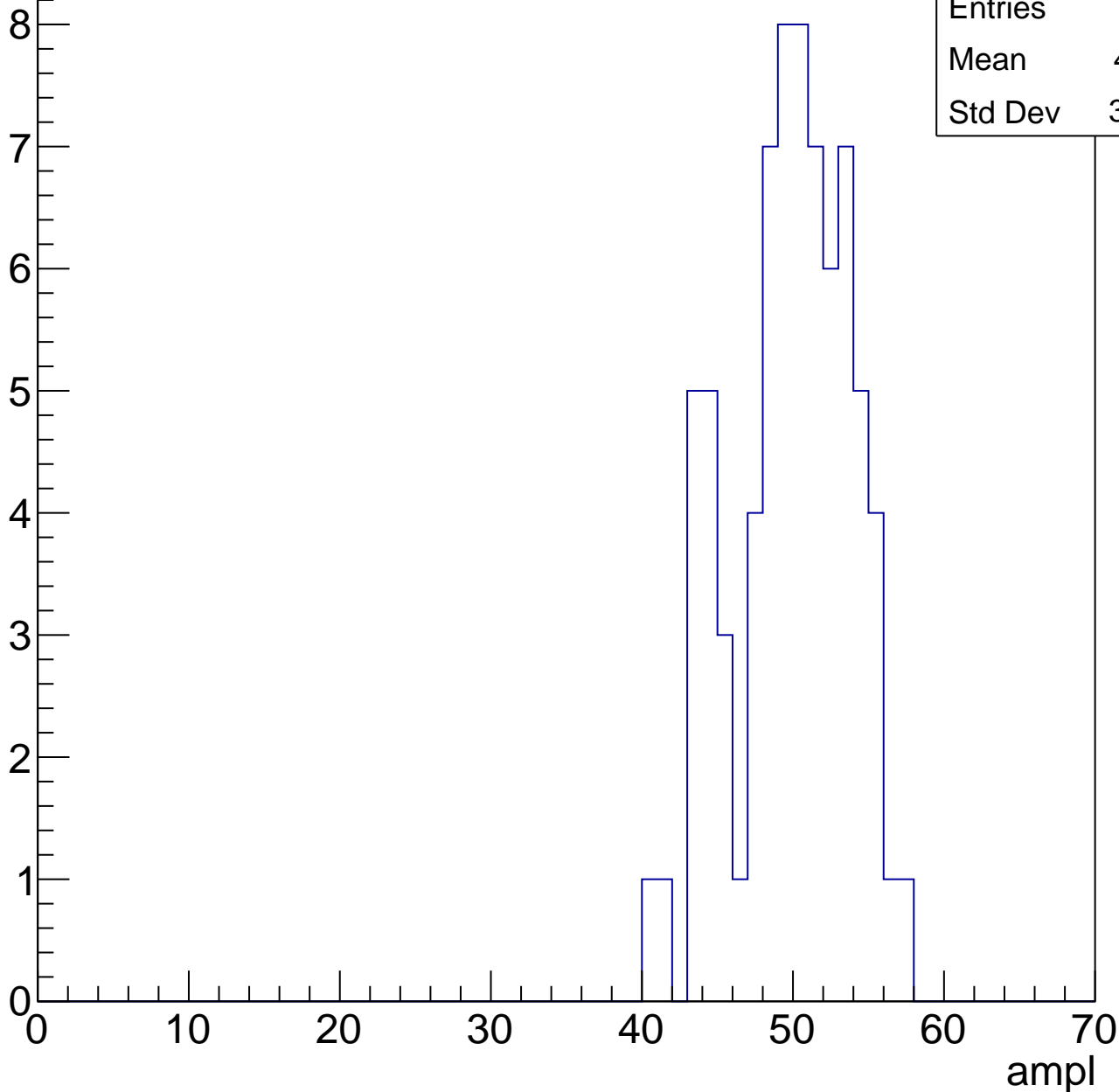


B1L103S, U9-ch12, adc3

calib_packv5_041523_1651.root, FC#0, port C2

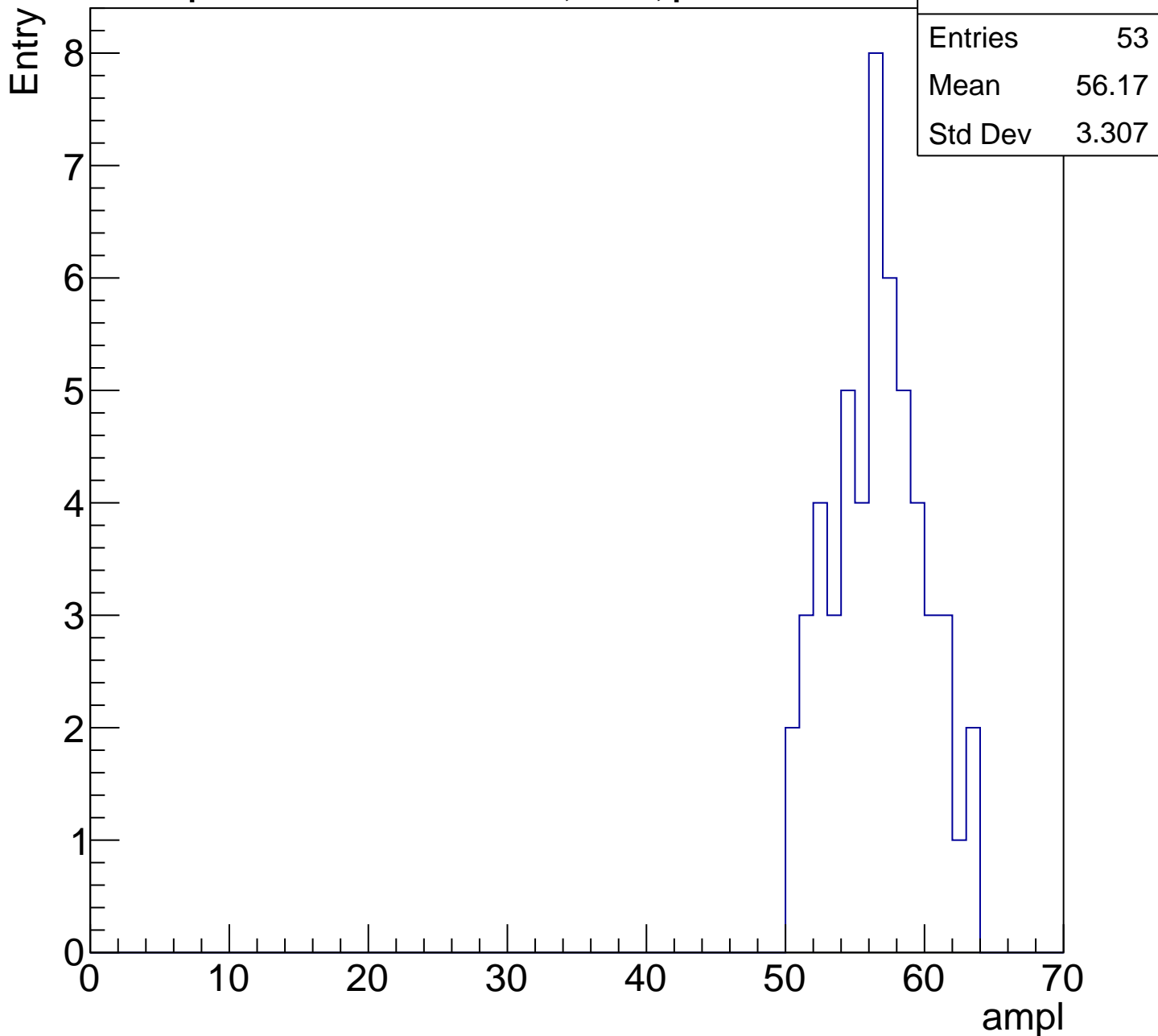
Entry

Entries	74
Mean	49.41
Std Dev	3.859



B1L103S, U9-ch12, adc4

calib_packv5_041523_1651.root, FC#0, port C2

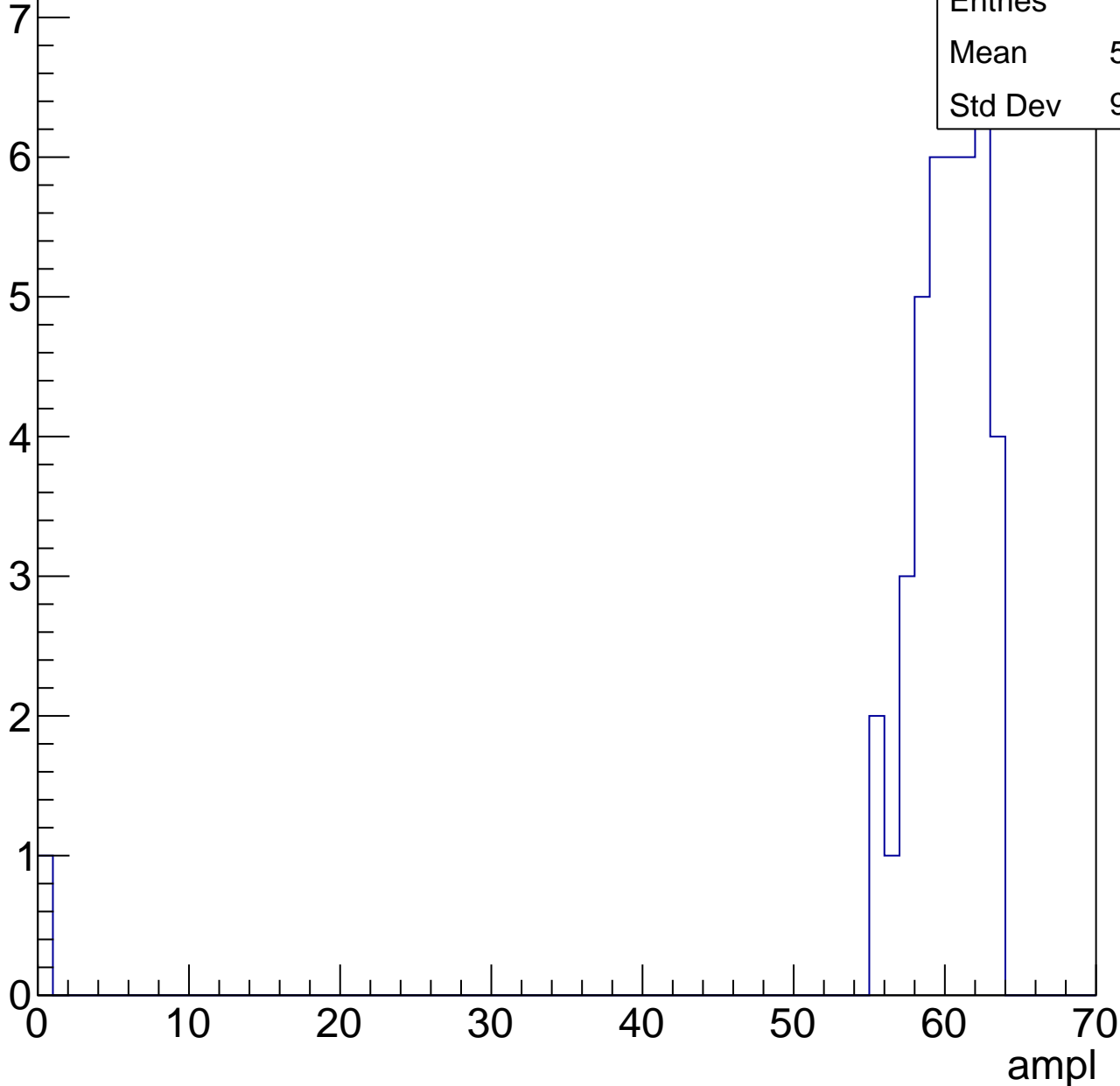


B1L103S, U9-ch12, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	41
Mean	58.37
Std Dev	9.473



B1L103S, U9-ch12, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch12, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

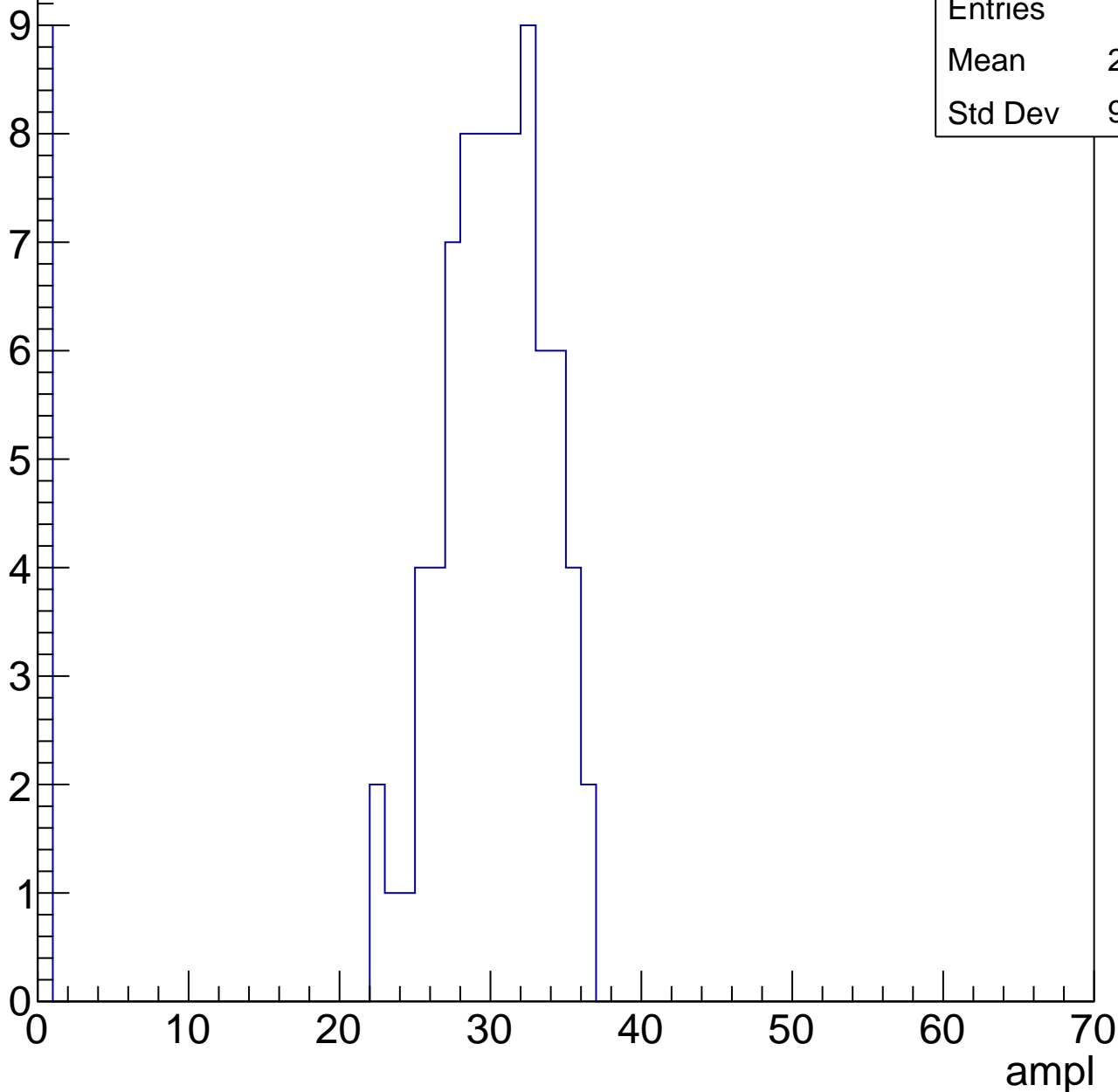
Entries	19
Mean	0
Std Dev	0

B1L103S, U9-ch13, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	87
Mean	26.78
Std Dev	9.616

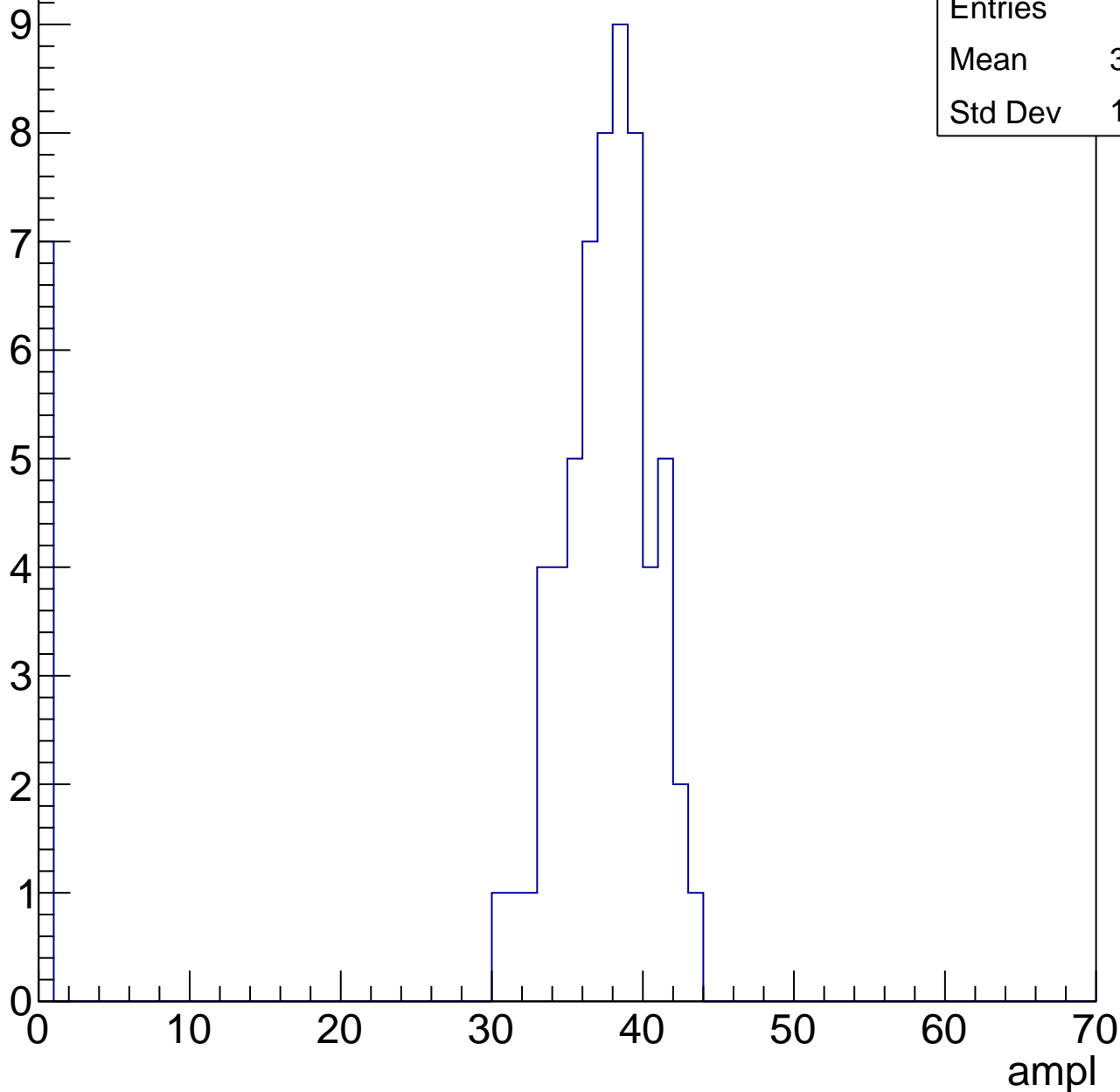


B1L103S, U9-ch13, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	33.28
Std Dev	11.68

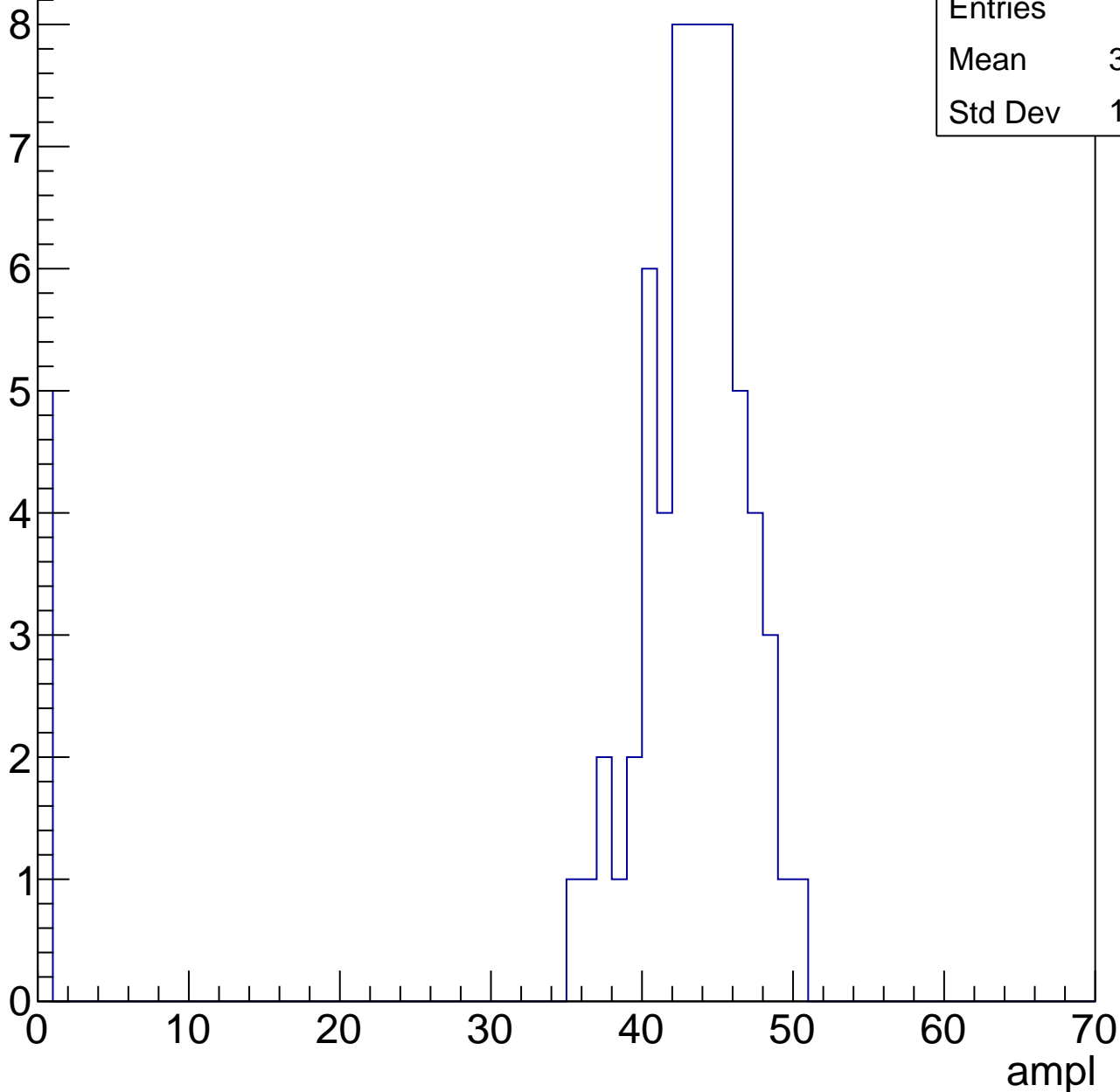


B1L103S, U9-ch13, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	39.97
Std Dev	11.66

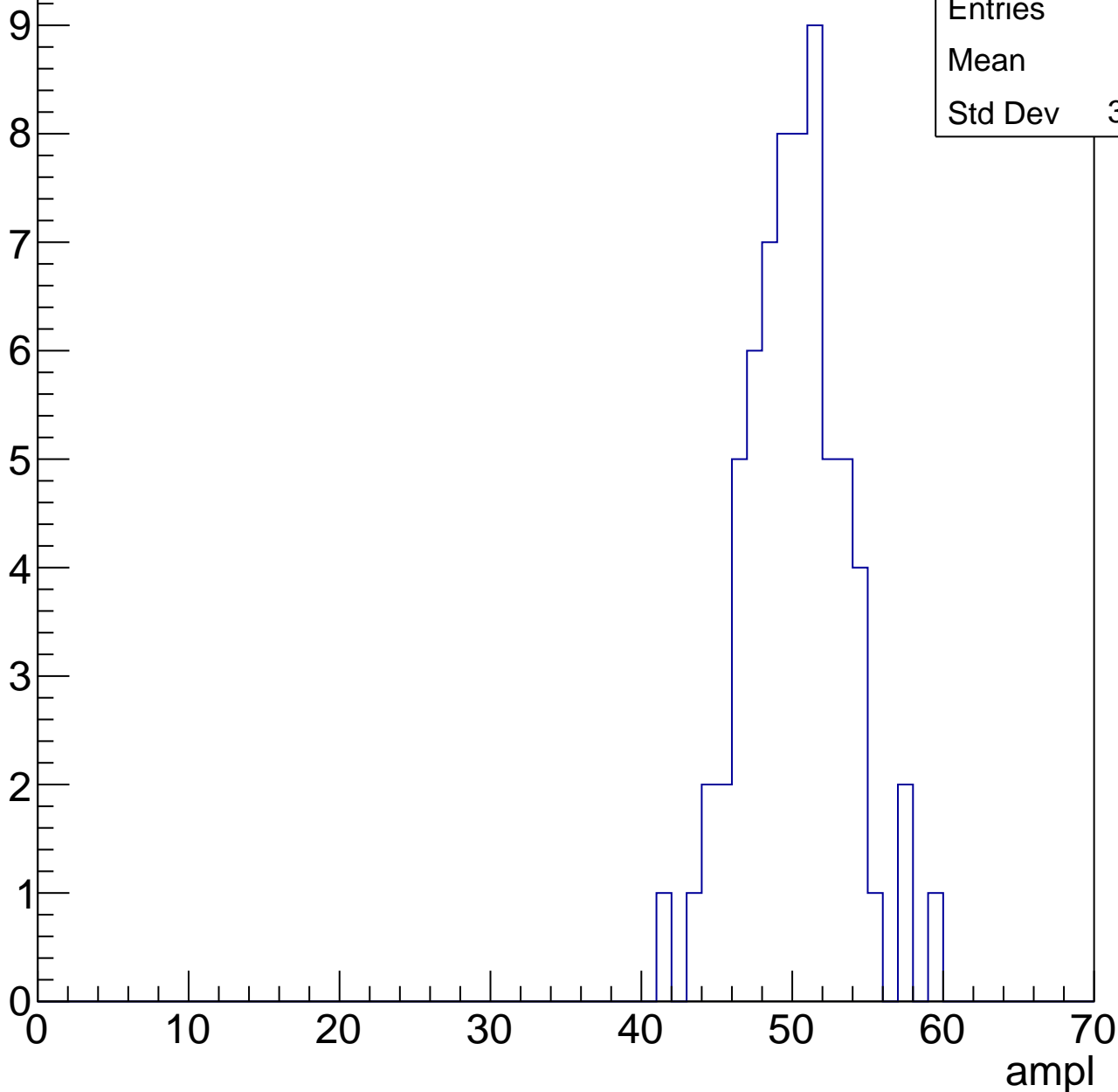


B1L103S, U9-ch13, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	49.7
Std Dev	3.364

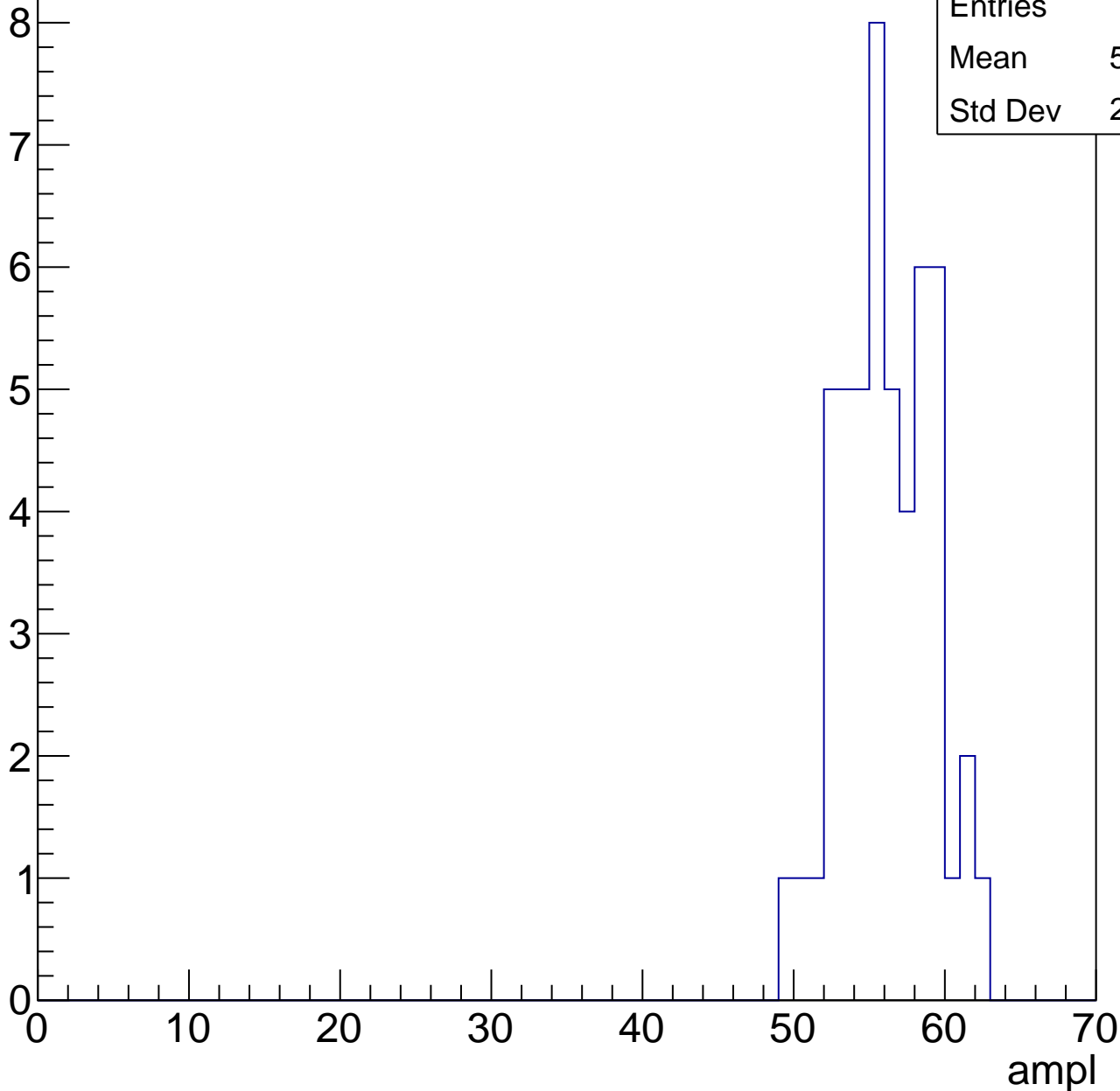


B1L103S, U9-ch13, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	55.67
Std Dev	2.942



B1L103S, U9-ch13, adc5

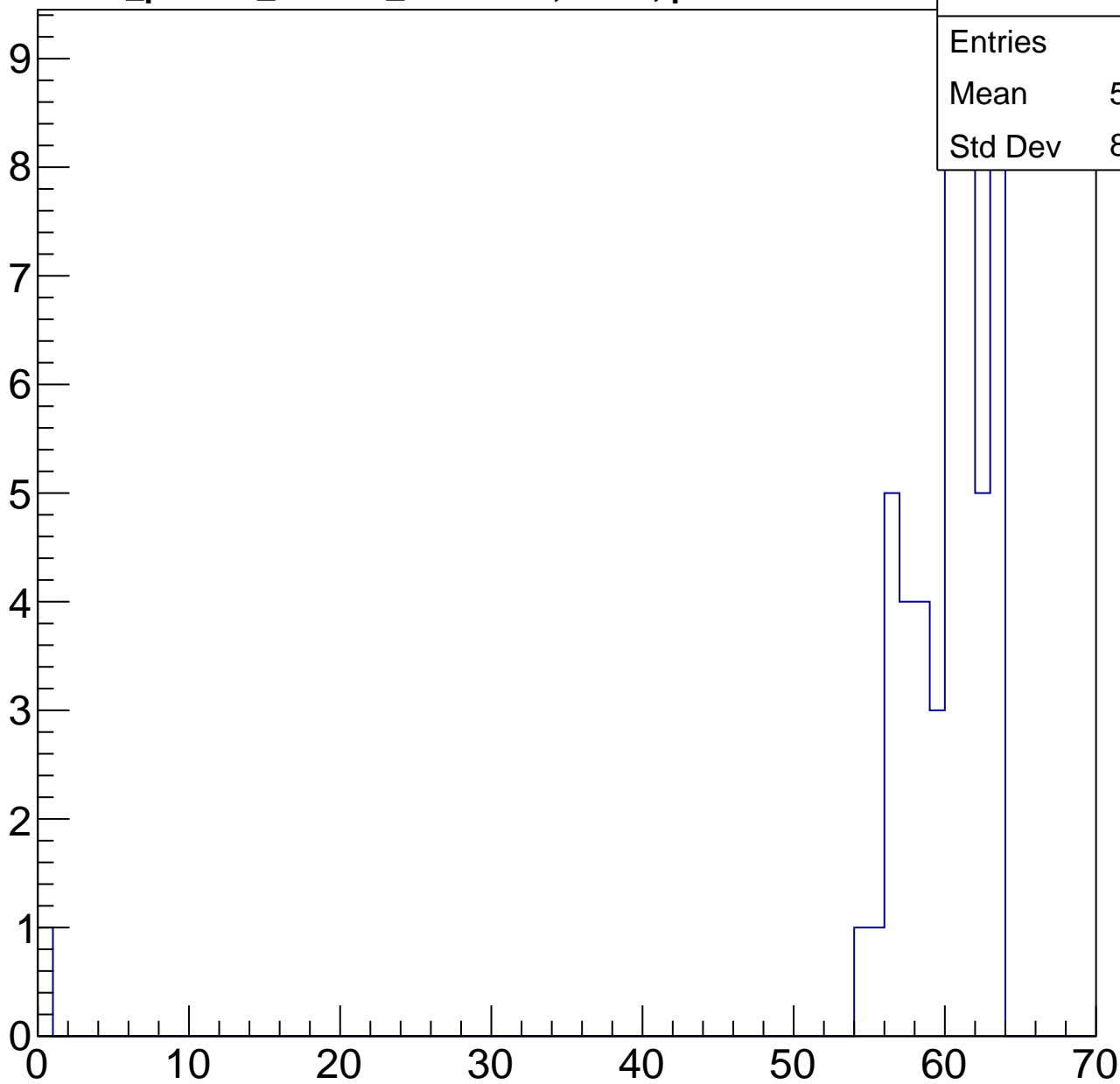
calib_packv5_041523_1651.root, FC#0, port C2

Entry

9
8
7
6
5
4
3
2
1
0

Entries	49
Mean	58.53
Std Dev	8.795

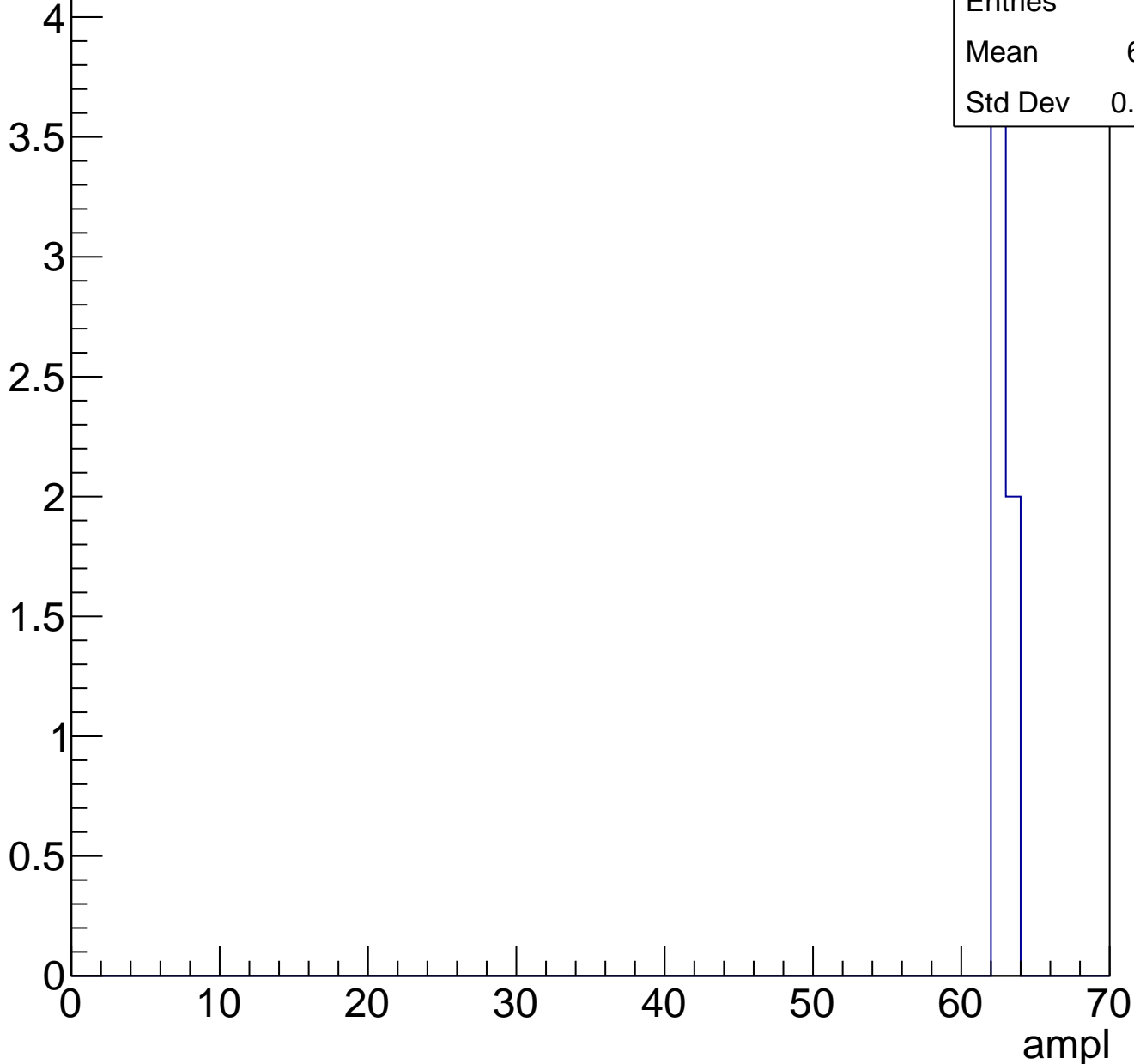
ampl



B1L103S, U9-ch13, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch13, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

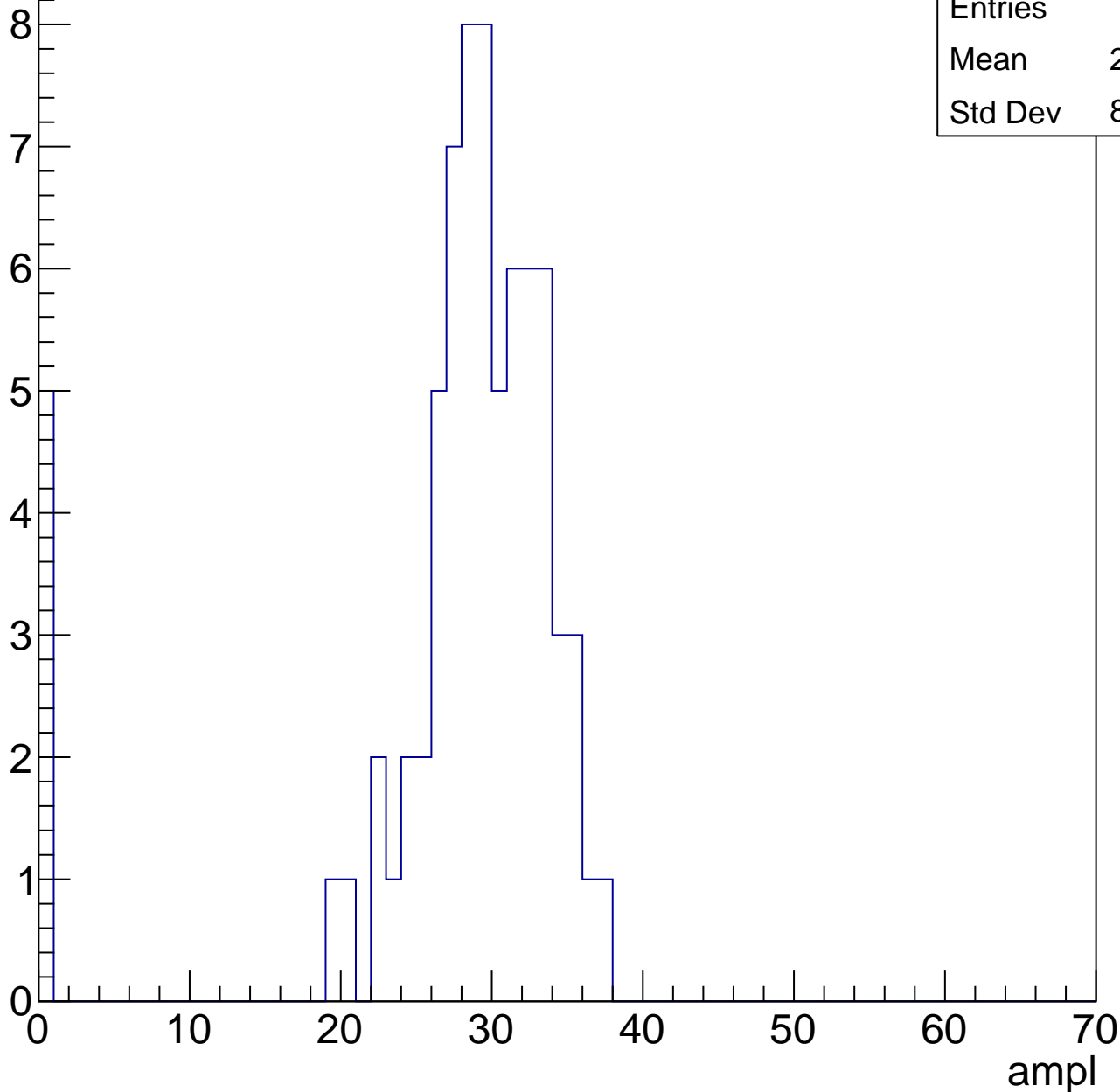


B1L103S, U9-ch14, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	27.19
Std Dev	8.209

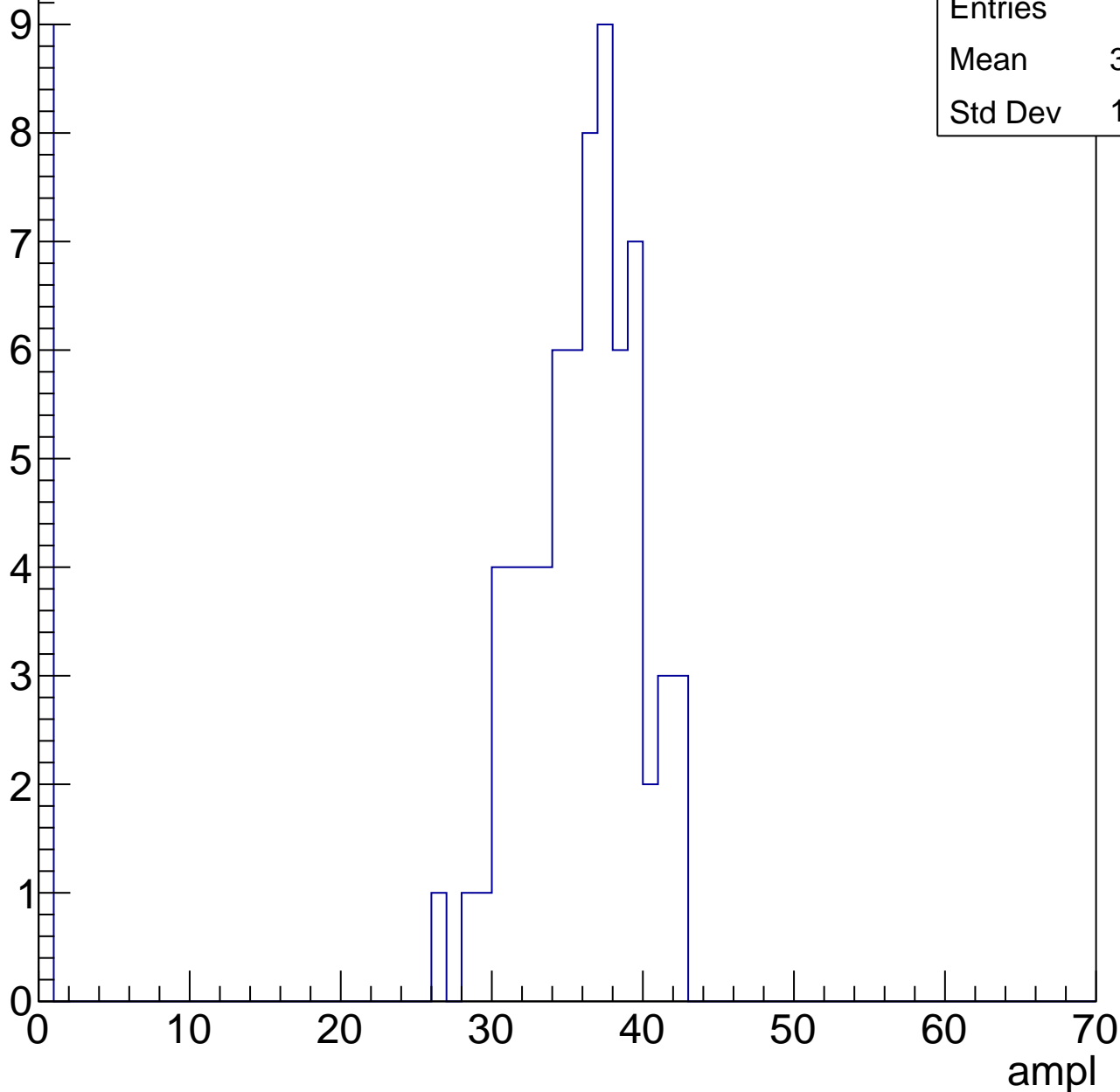


B1L103S, U9-ch14, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	31.44
Std Dev	11.84

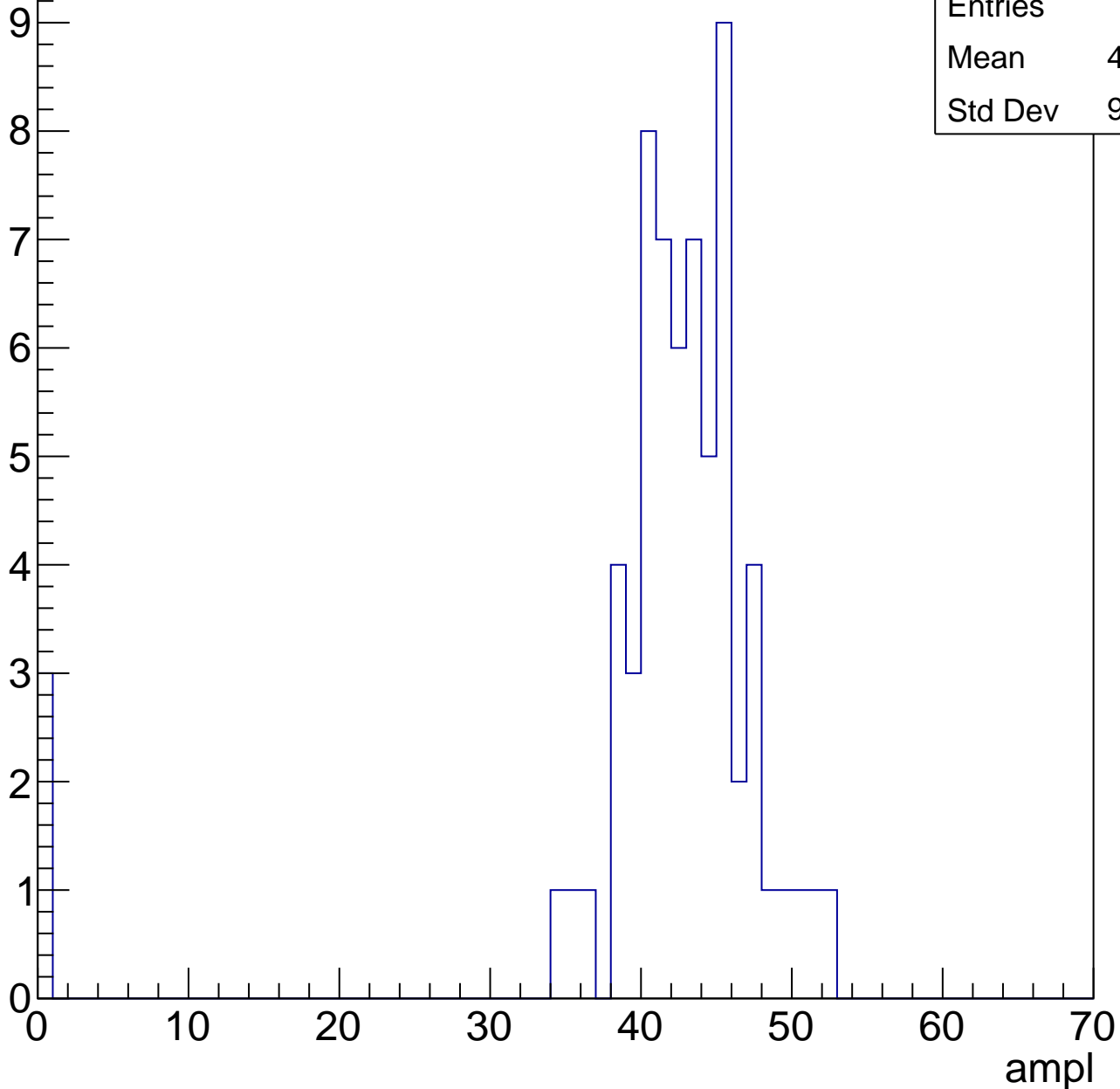


B1L103S, U9-ch14, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	40.74
Std Dev	9.564

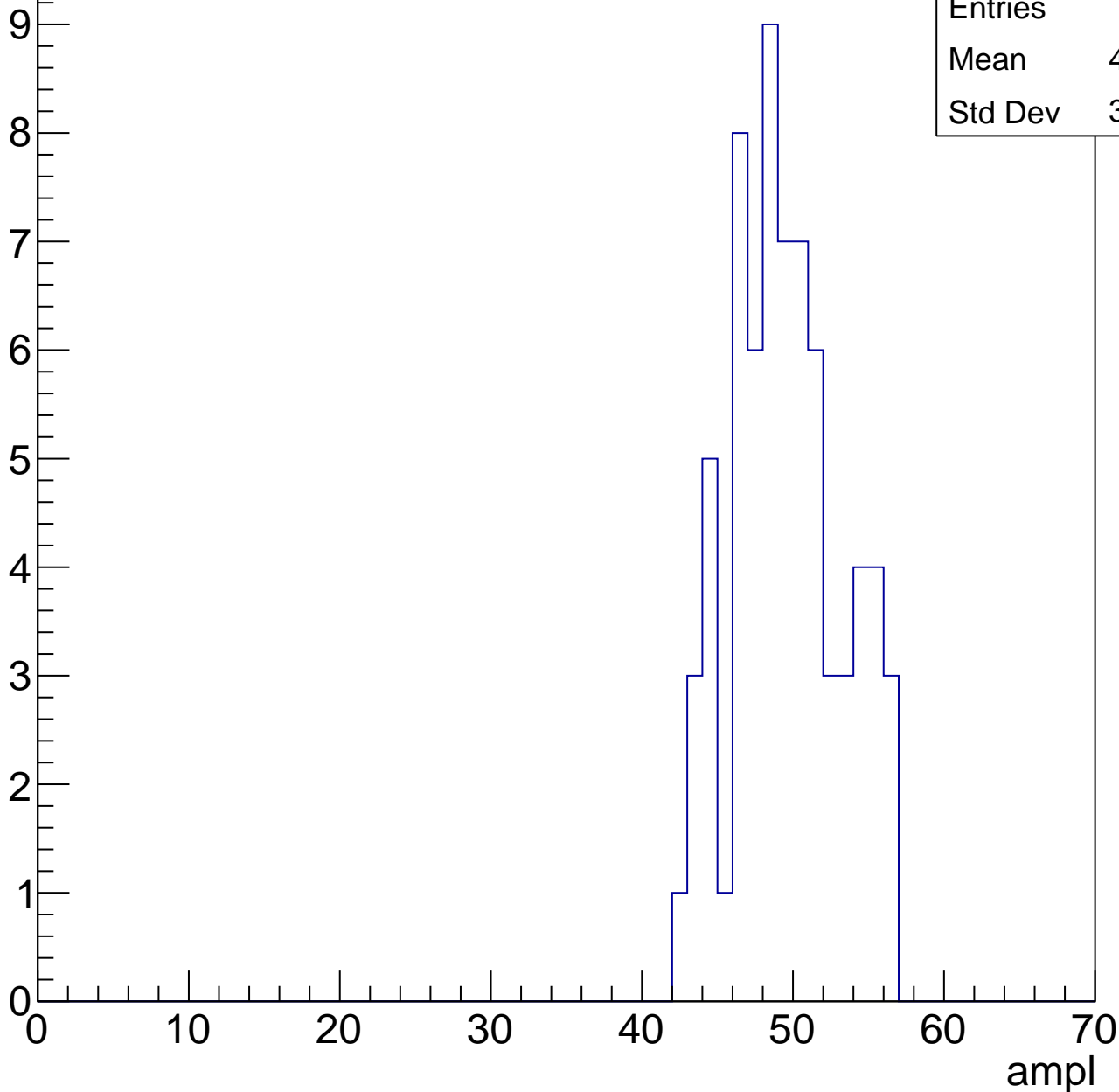


B1L103S, U9-ch14, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	49.09
Std Dev	3.585

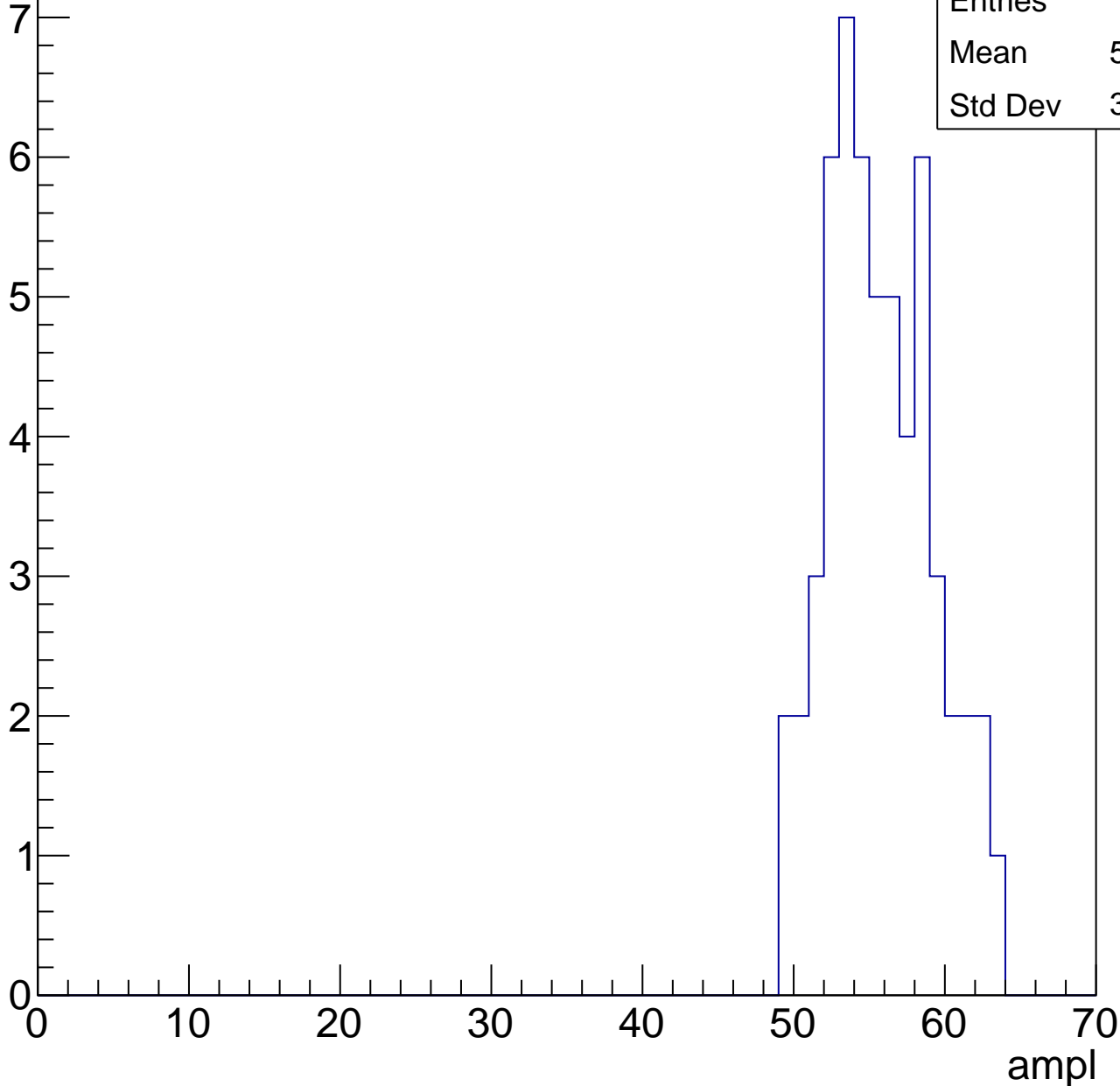


B1L103S, U9-ch14, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	55.27
Std Dev	3.436

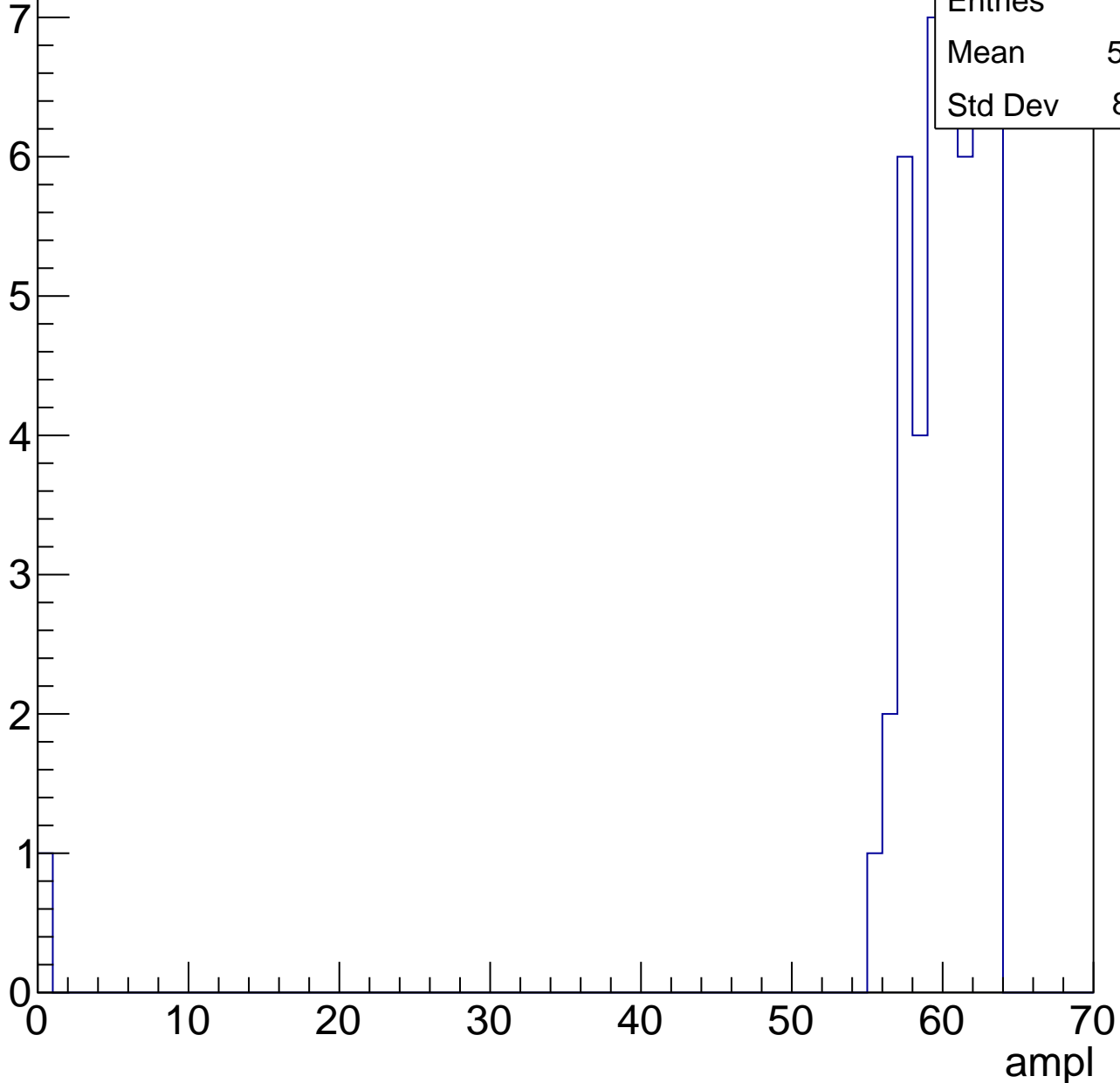


B1L103S, U9-ch14, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	48
Mean	58.65
Std Dev	8.831



B1L103S, U9-ch14, adc6

calib_packv5_041523_1651.root, FC#0, port C2

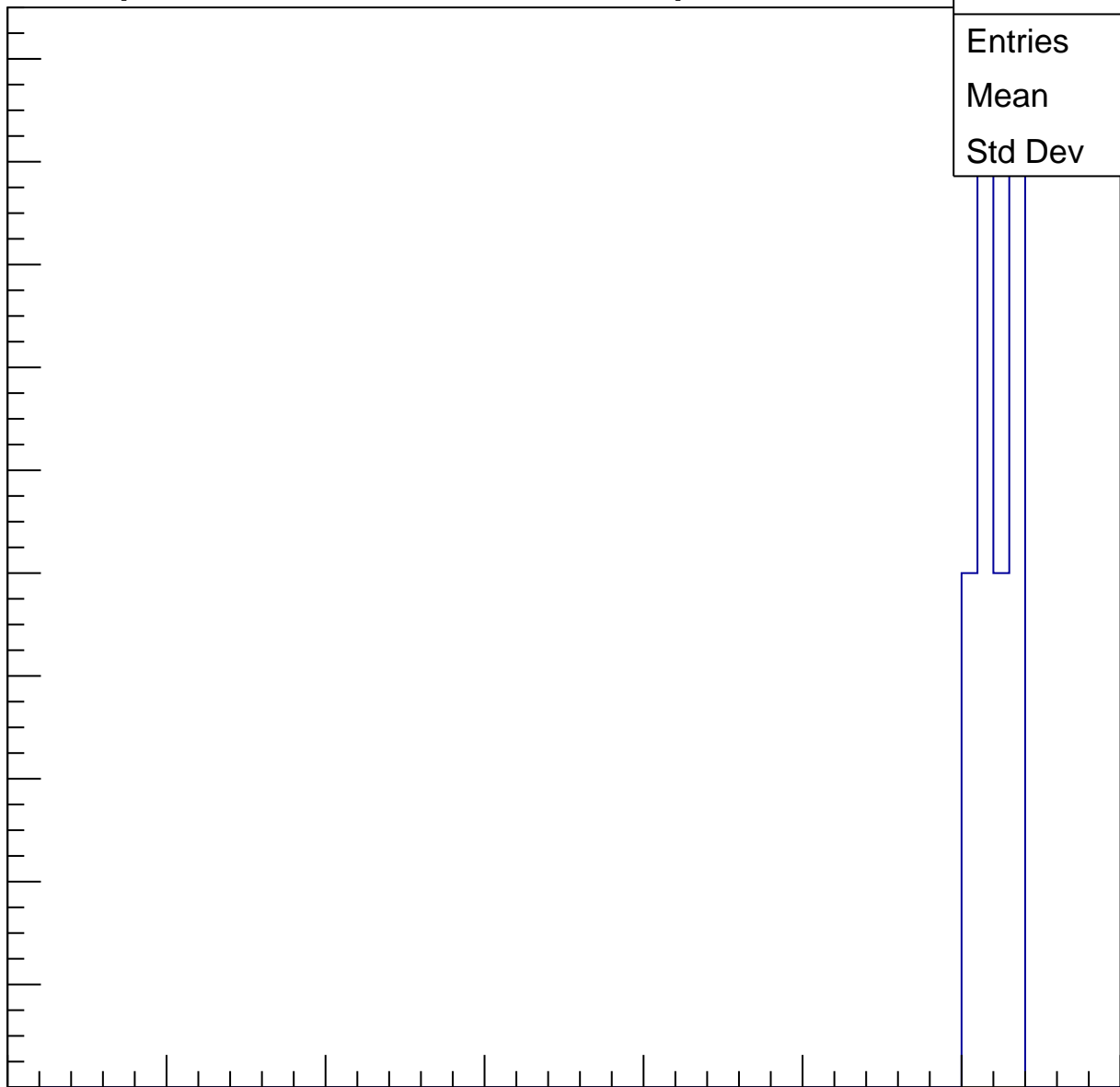
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	6
Mean	61.67
Std Dev	1.106

0 10 20 30 40 50 60 70

ampl



B1L103S, U9-ch14, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

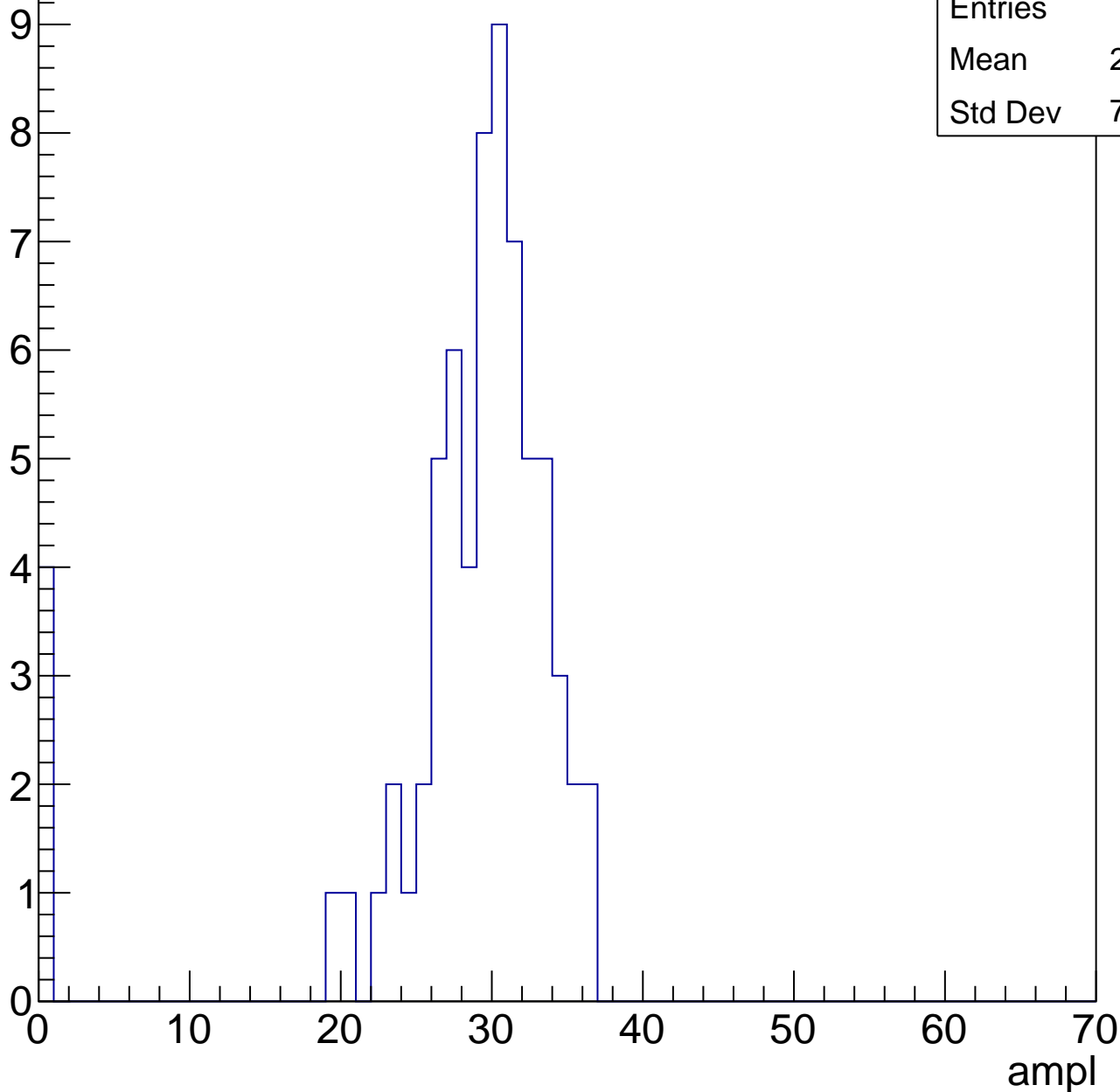


B1L103S, U9-ch15, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	27.54
Std Dev	7.726

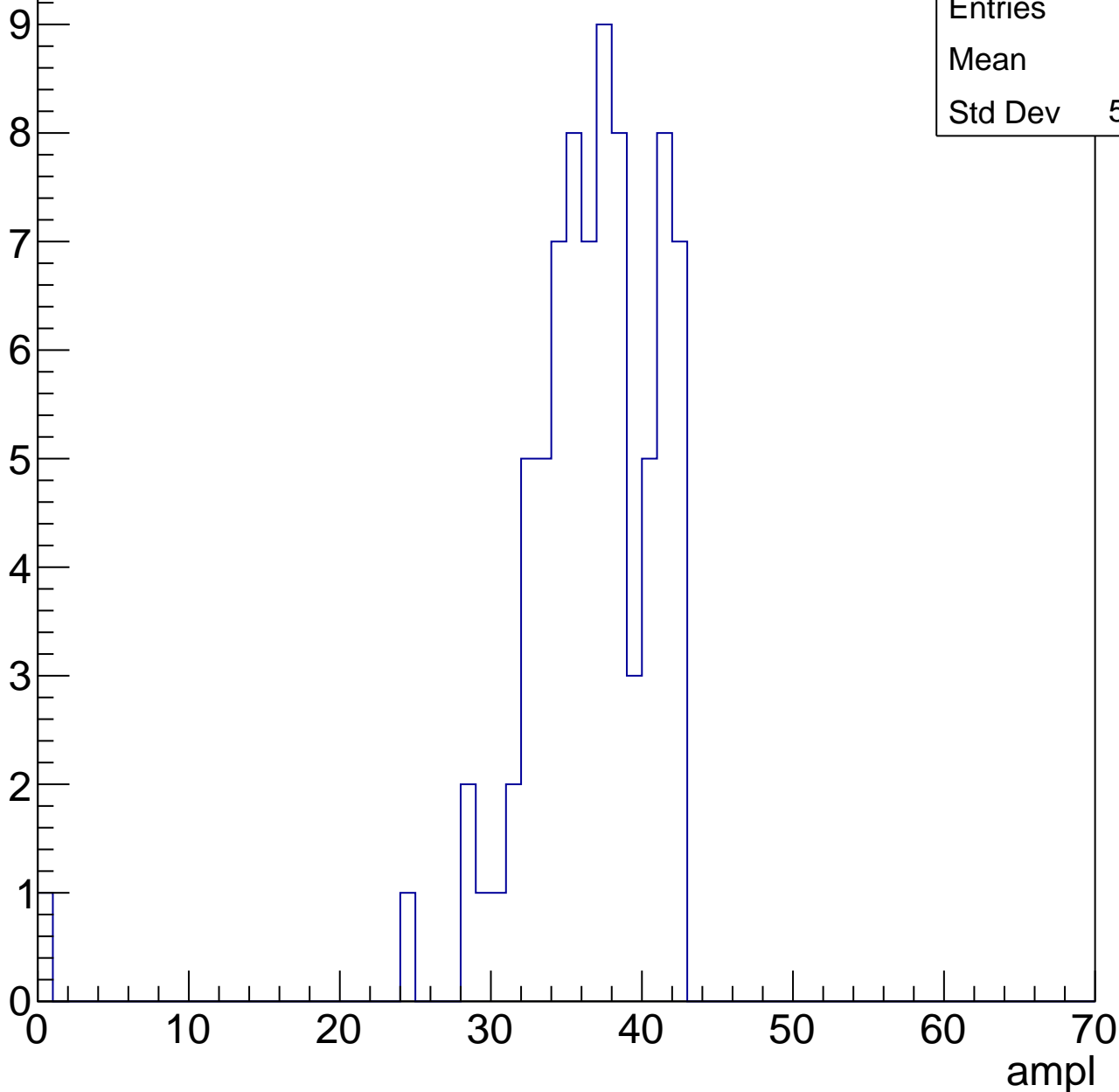


B1L103S, U9-ch15, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	80
Mean	35.9
Std Dev	5.549

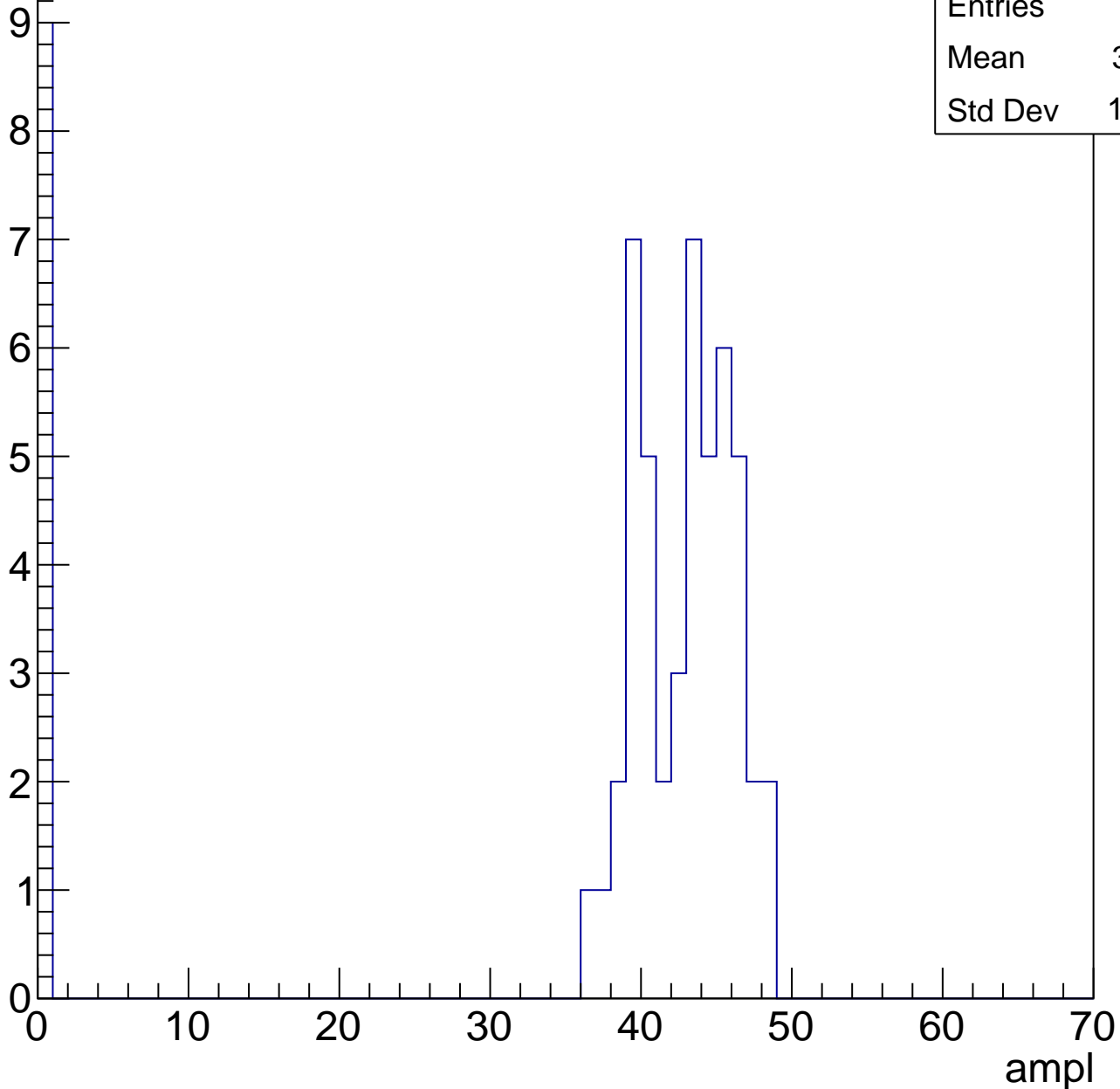


B1L103S, U9-ch15, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	35.81
Std Dev	15.76

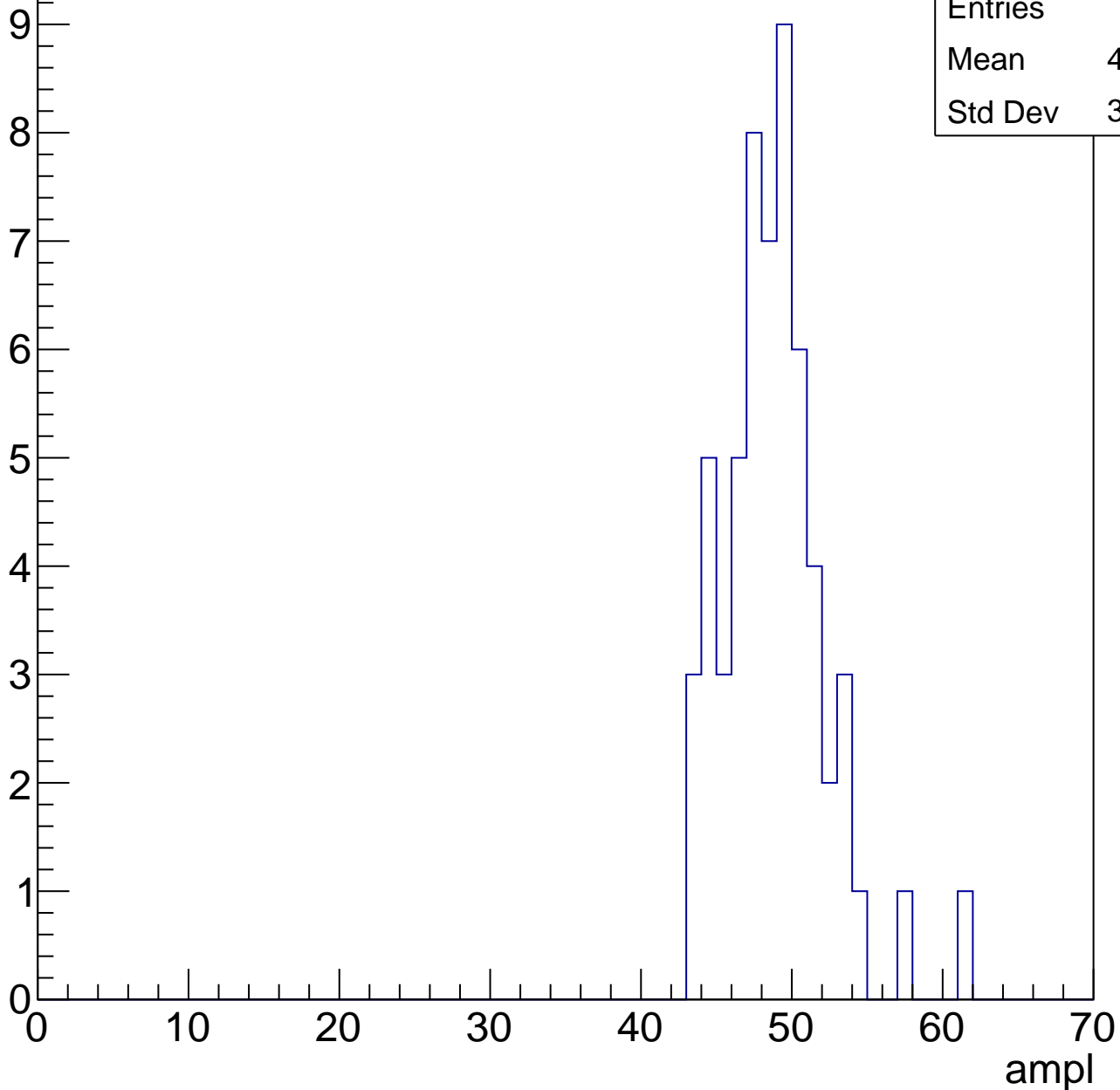


B1L103S, U9-ch15, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	48.38
Std Dev	3.383

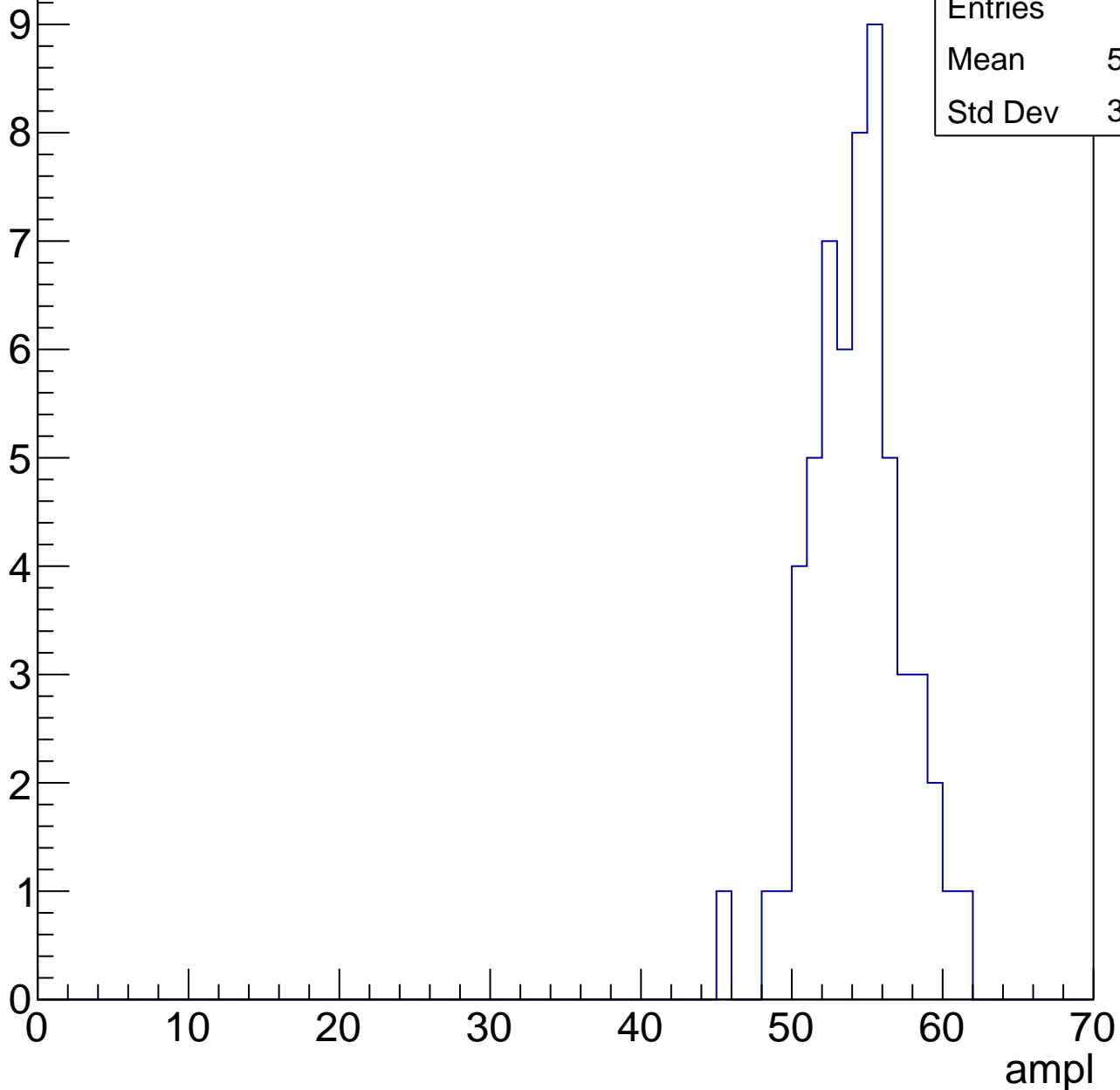


B1L103S, U9-ch15, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	53.86
Std Dev	3.029



B1L103S, U9-ch15, adc5

calib_packv5_041523_1651.root, FC#0, port C2

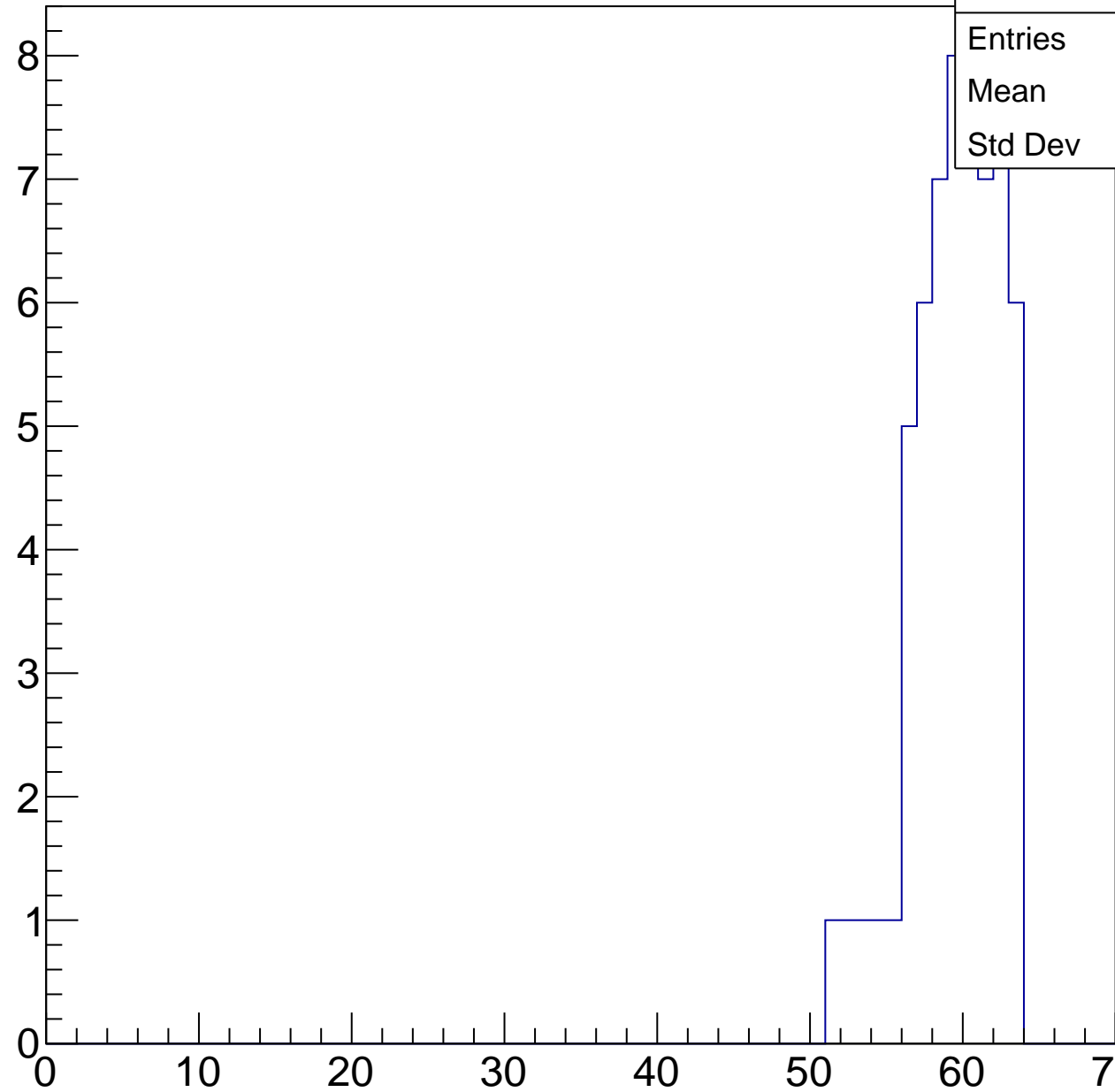
Entry

8
7
6
5
4
3
2
1
0

Entries	60
Mean	59.1
Std Dev	2.797

ampl

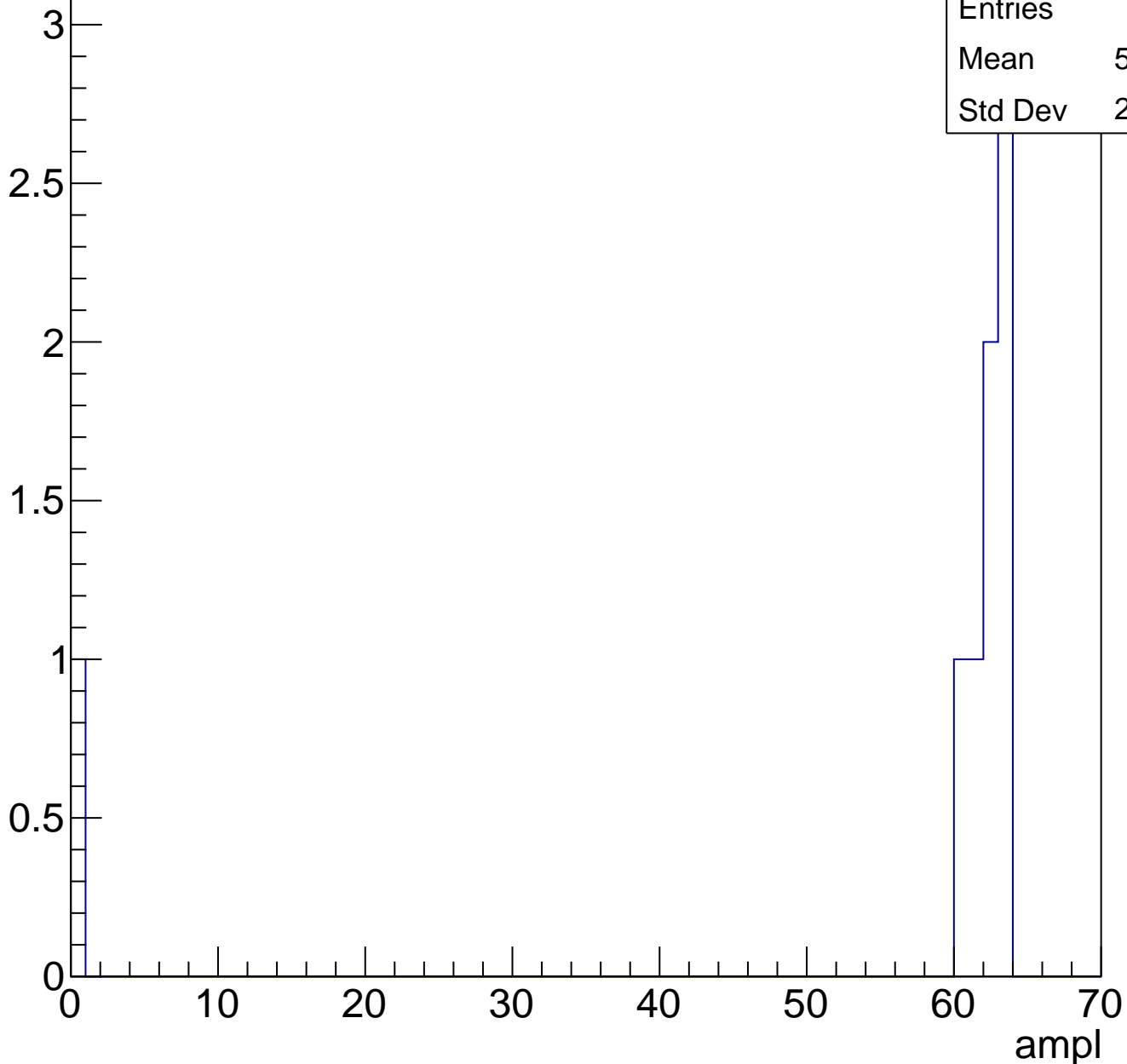
0 10 20 30 40 50 60 70



B1L103S, U9-ch15, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	8
Mean	54.25
Std Dev	20.53

B1L103S, U9-ch15, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	3.316
Std Dev	14.07

Entry

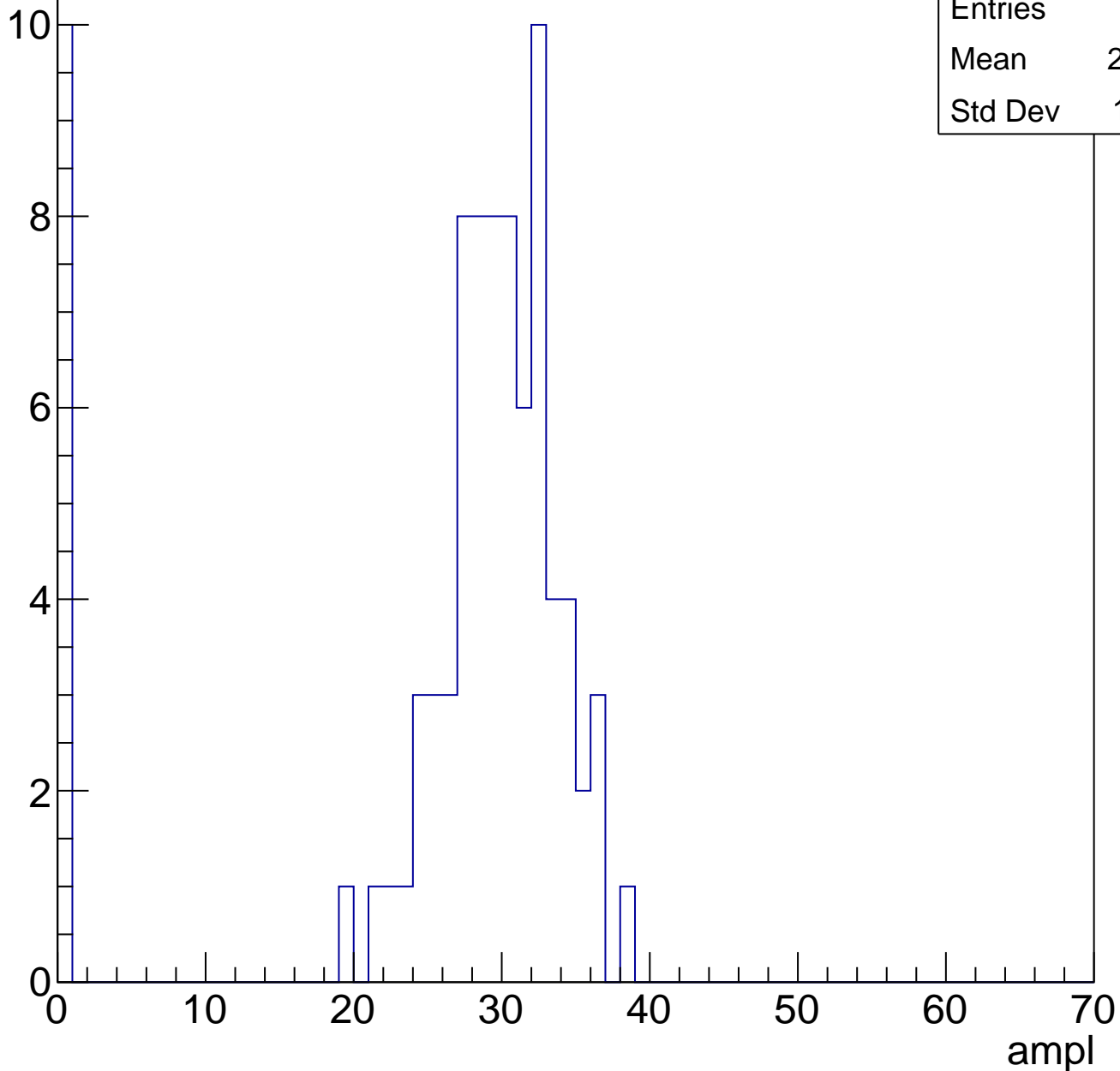


B1L103S, U9-ch16, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	85
Mean	26.02
Std Dev	10.11

Entry

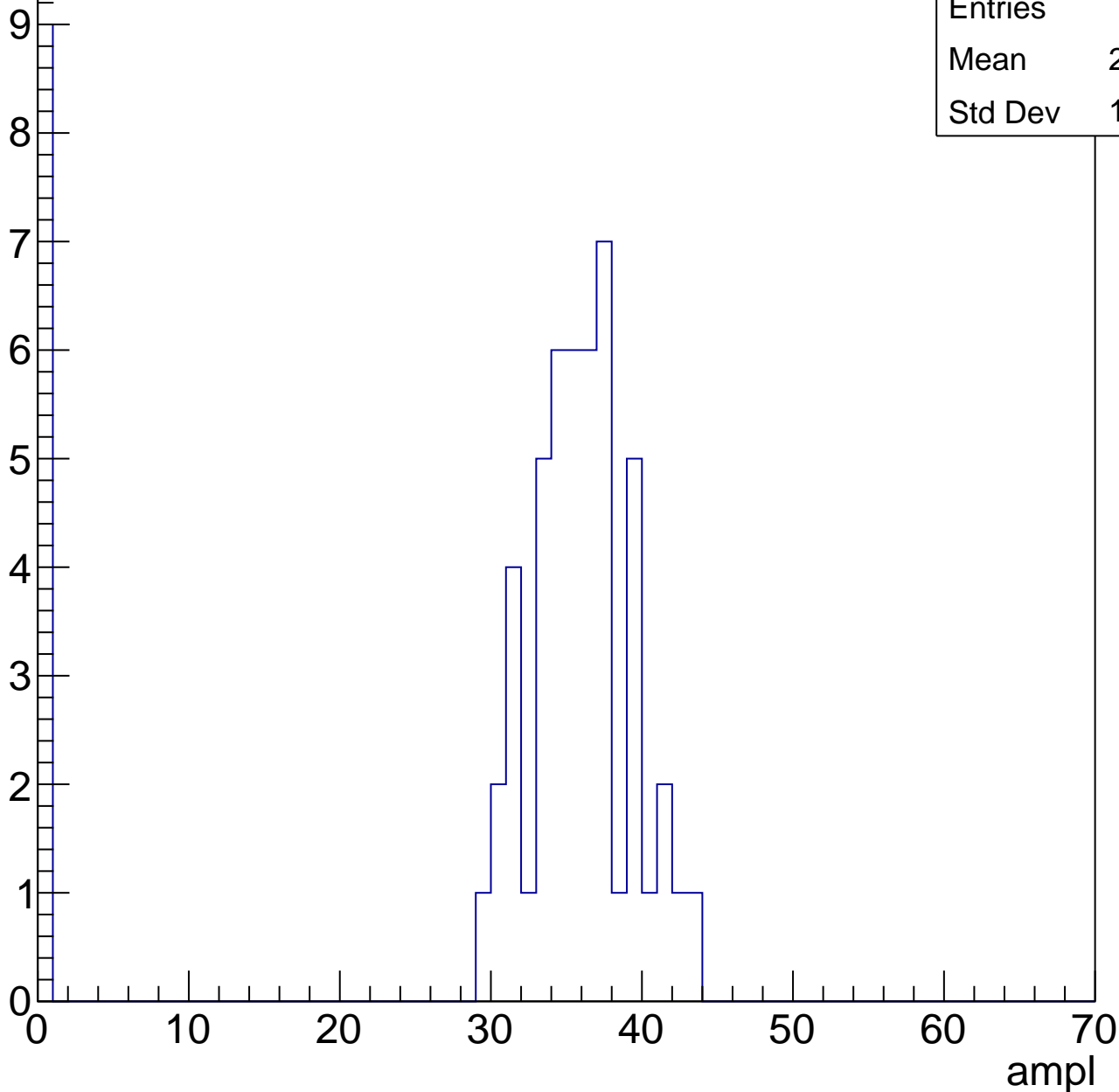


B1L103S, U9-ch16, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	29.98
Std Dev	13.19

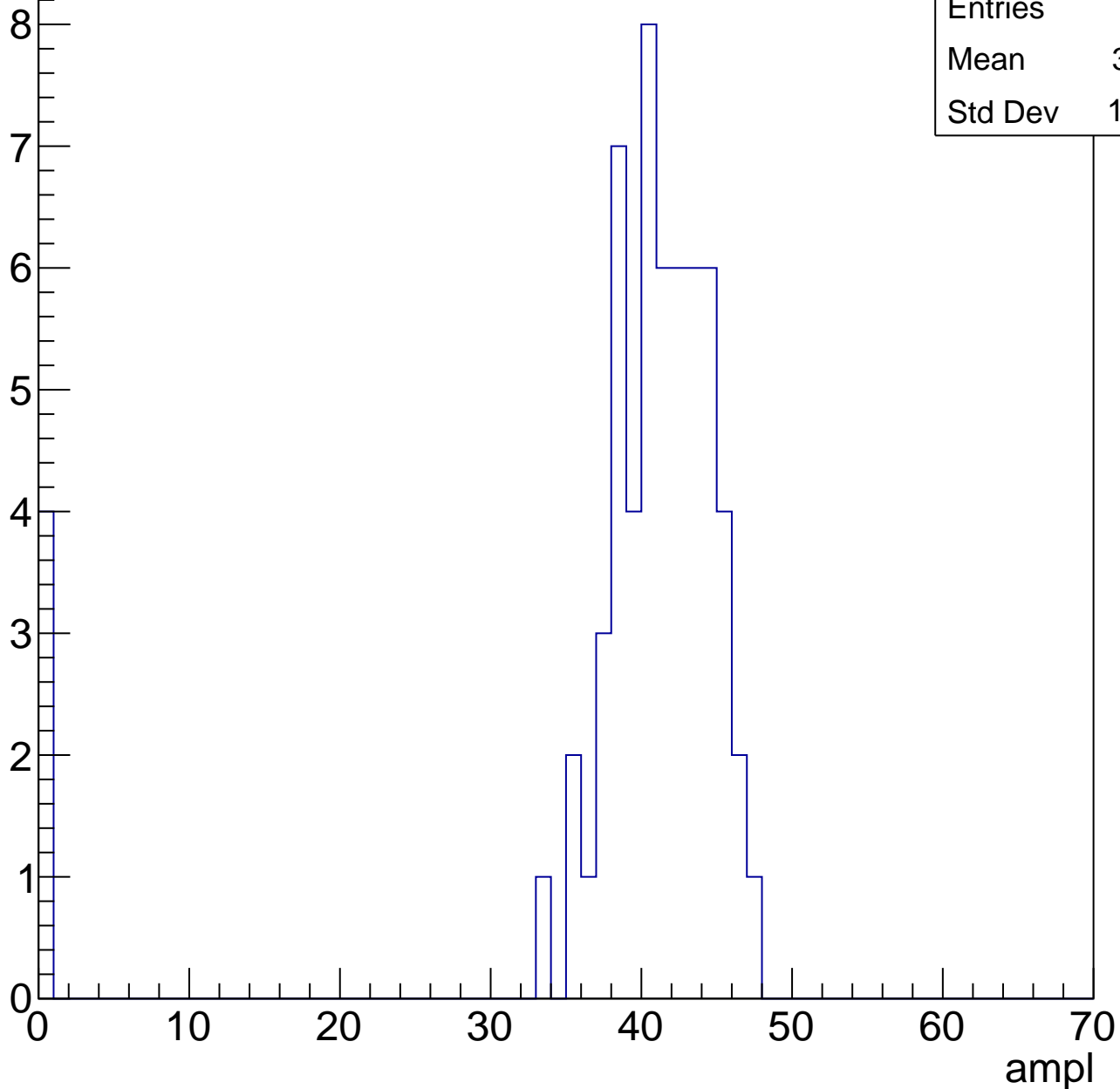


B1L103S, U9-ch16, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

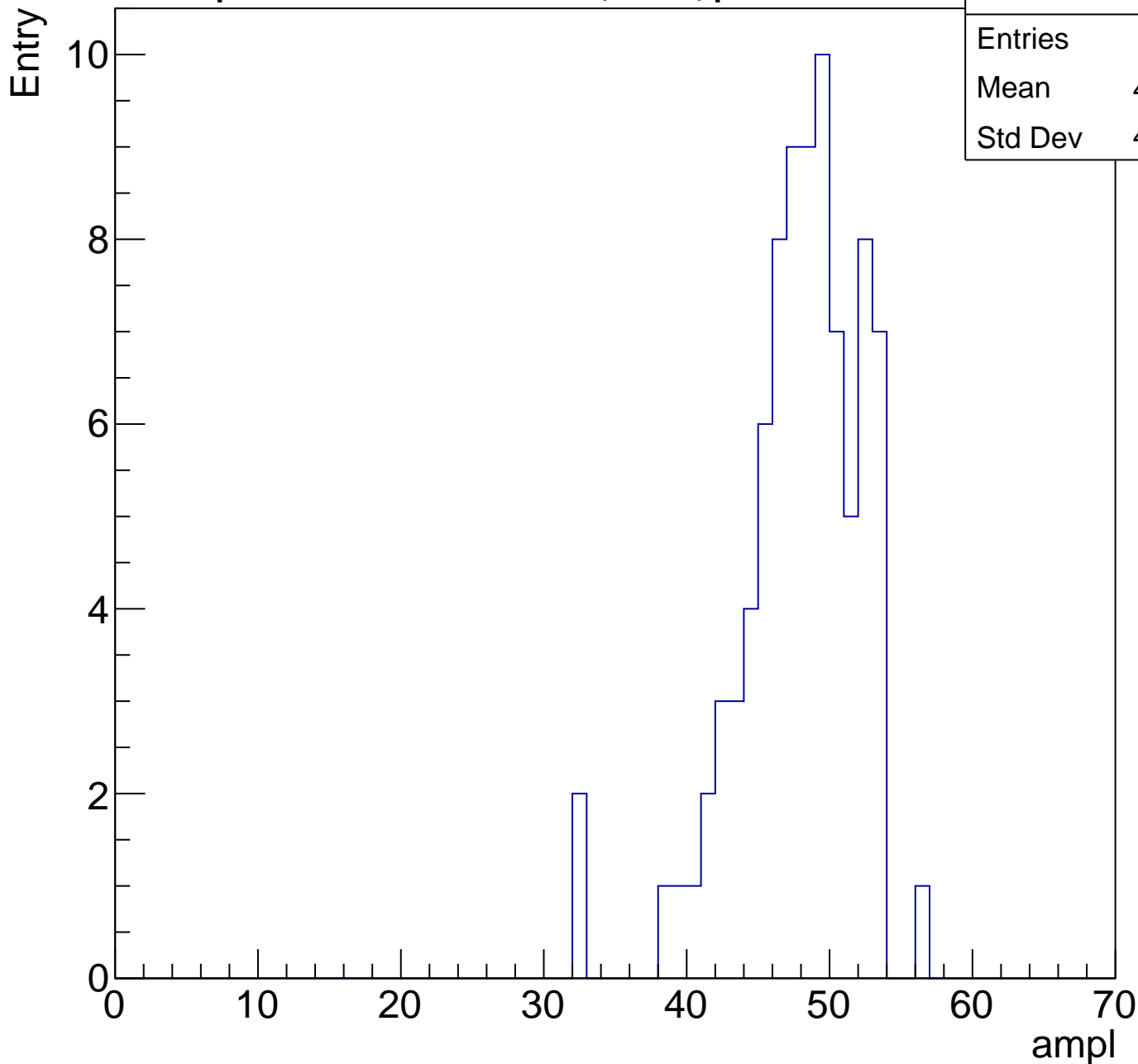
Entries	61
Mean	38.21
Std Dev	10.54



B1L103S, U9-ch16, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	87
Mean	47.41
Std Dev	4.311

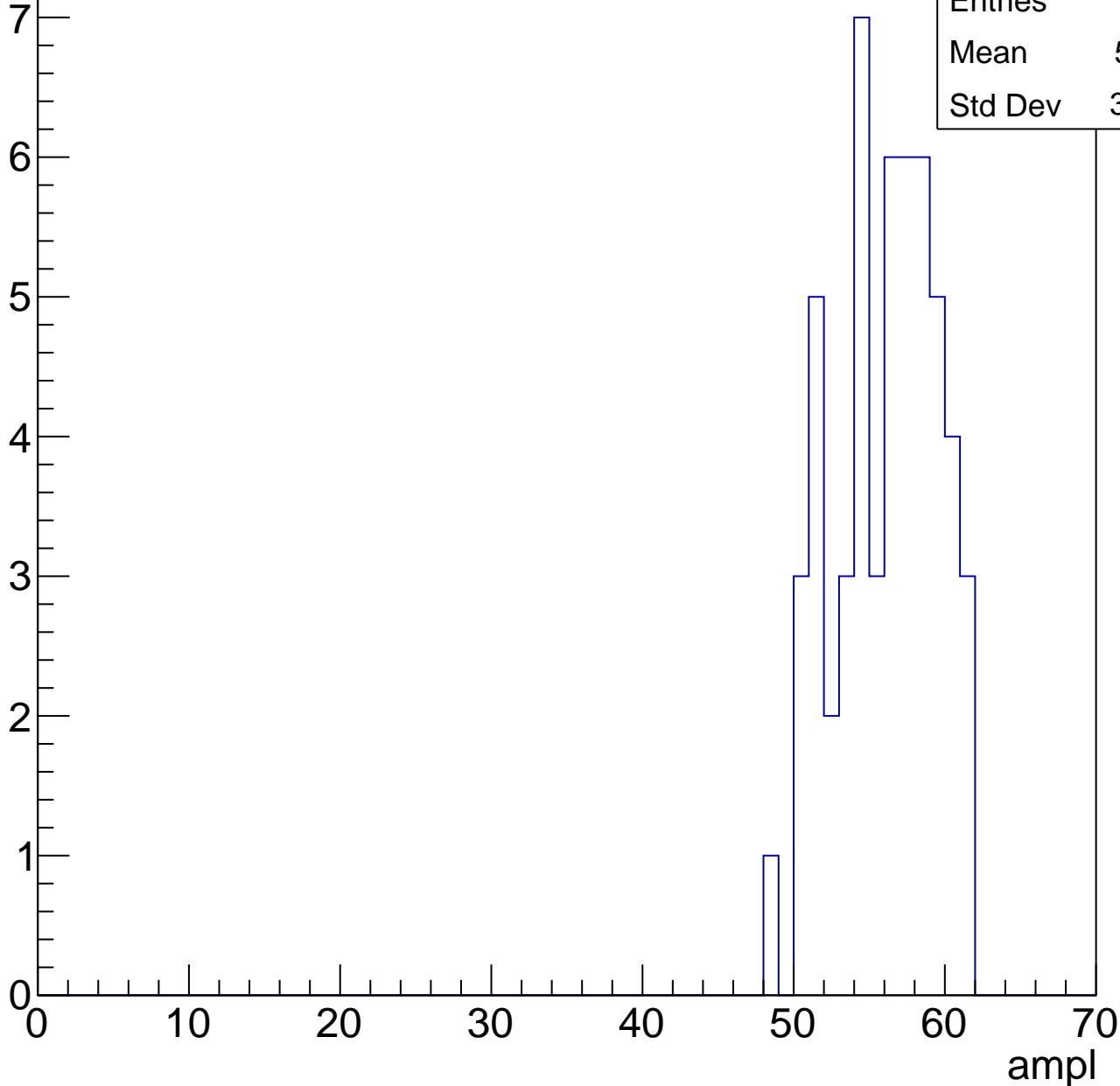


B1L103S, U9-ch16, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

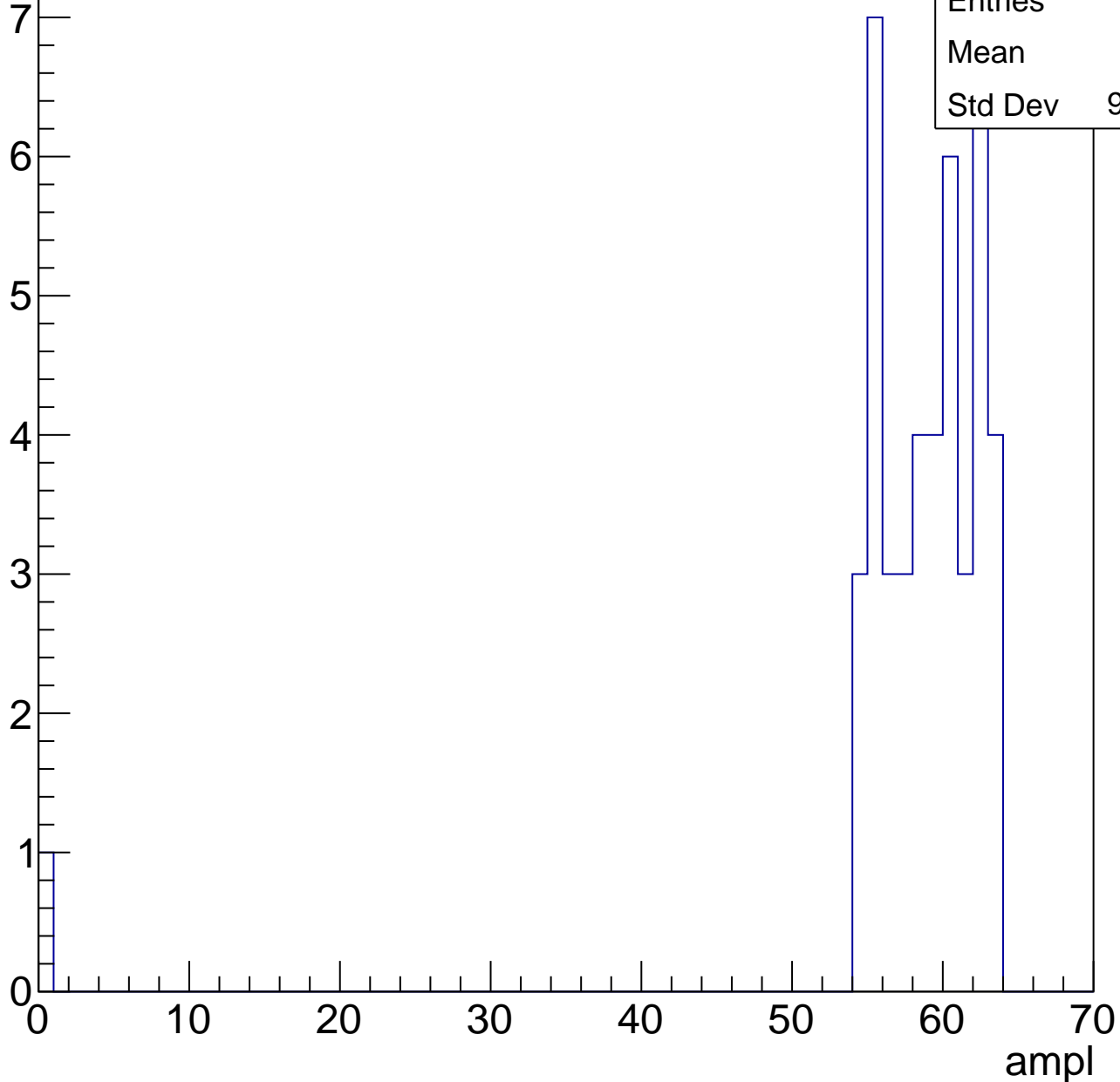
Entries	54
Mean	55.61
Std Dev	3.313



B1L103S, U9-ch16, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

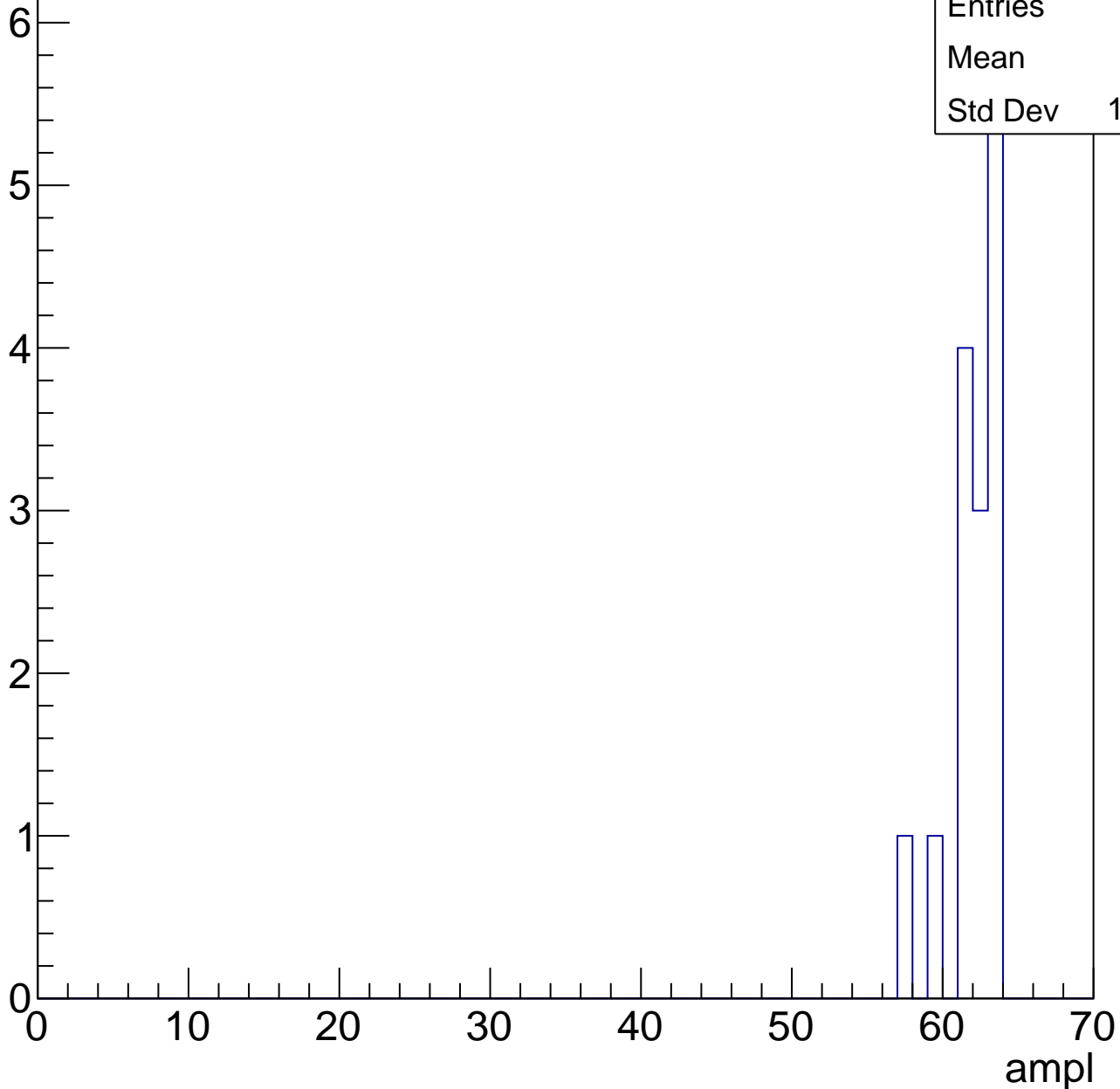


B1L103S, U9-ch16, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

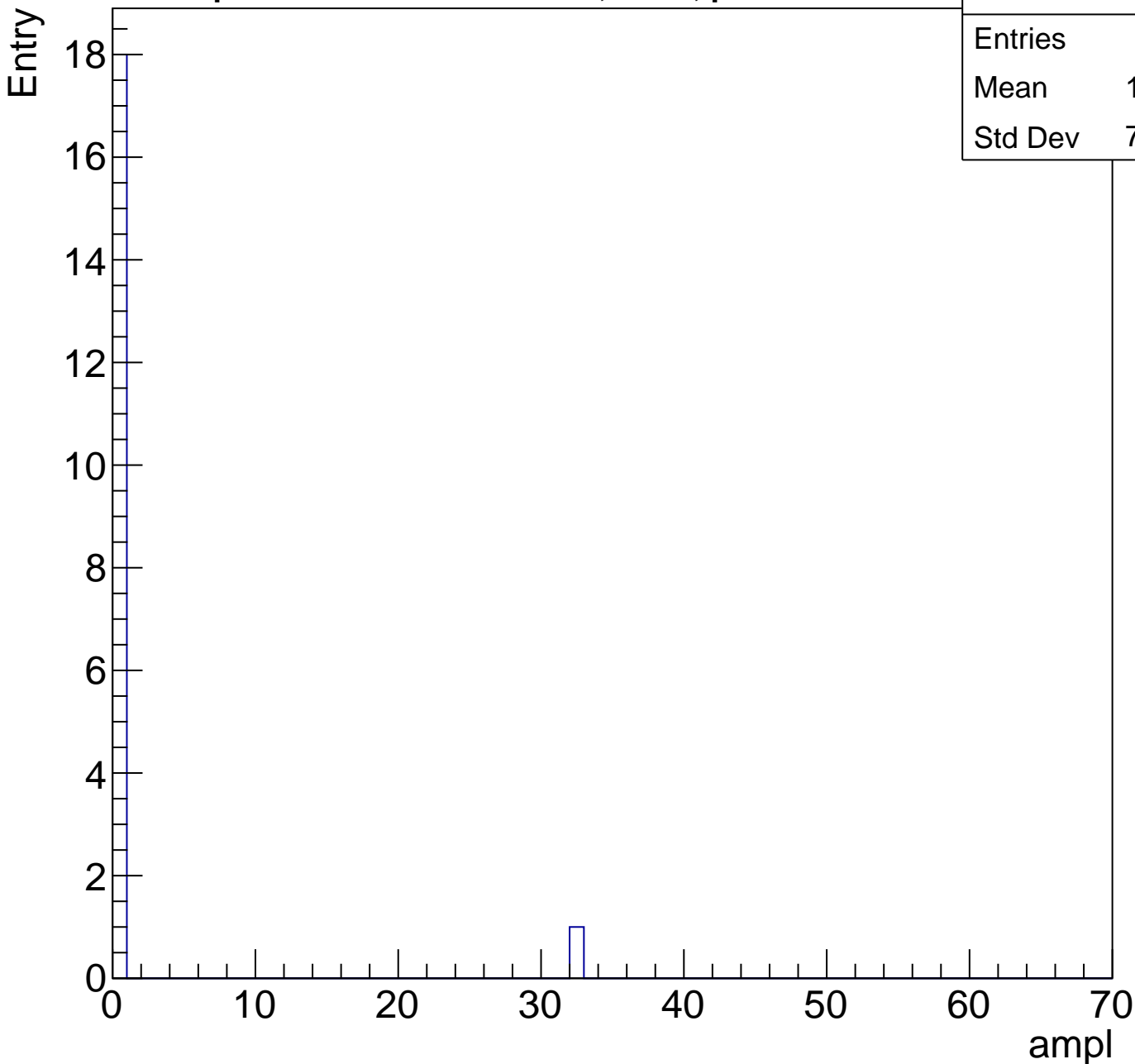
Entries	15
Mean	61.6
Std Dev	1.665



B1L103S, U9-ch16, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.684
Std Dev	7.146

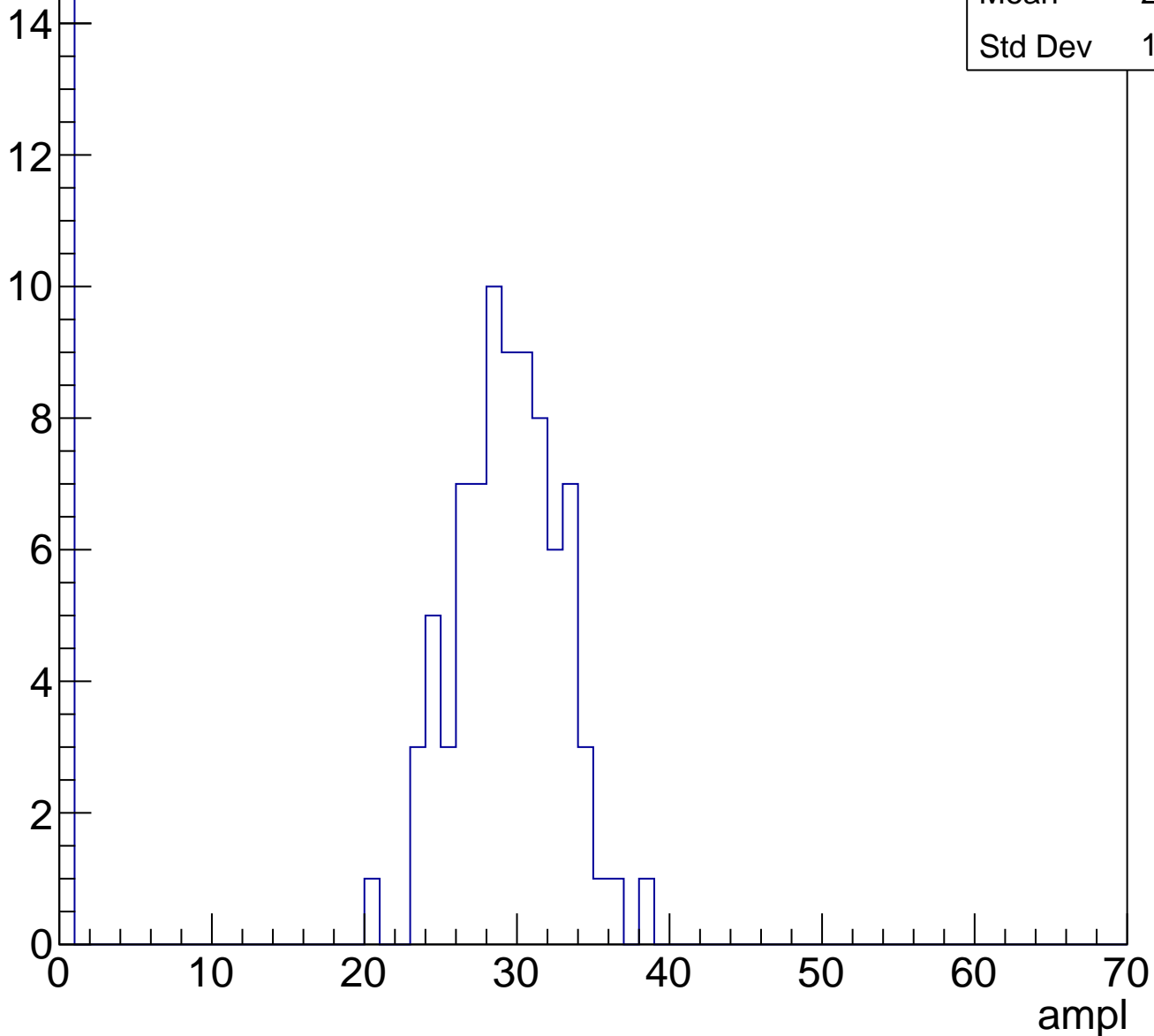


B1L103S, U9-ch17, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	96
Mean	24.46
Std Dev	10.97

Entry



B1L103S, U9-ch17, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	97
Mean	31.45
Std Dev	13.85

Entry

14
12
10
8
6
4
2
0

0

10

20

30

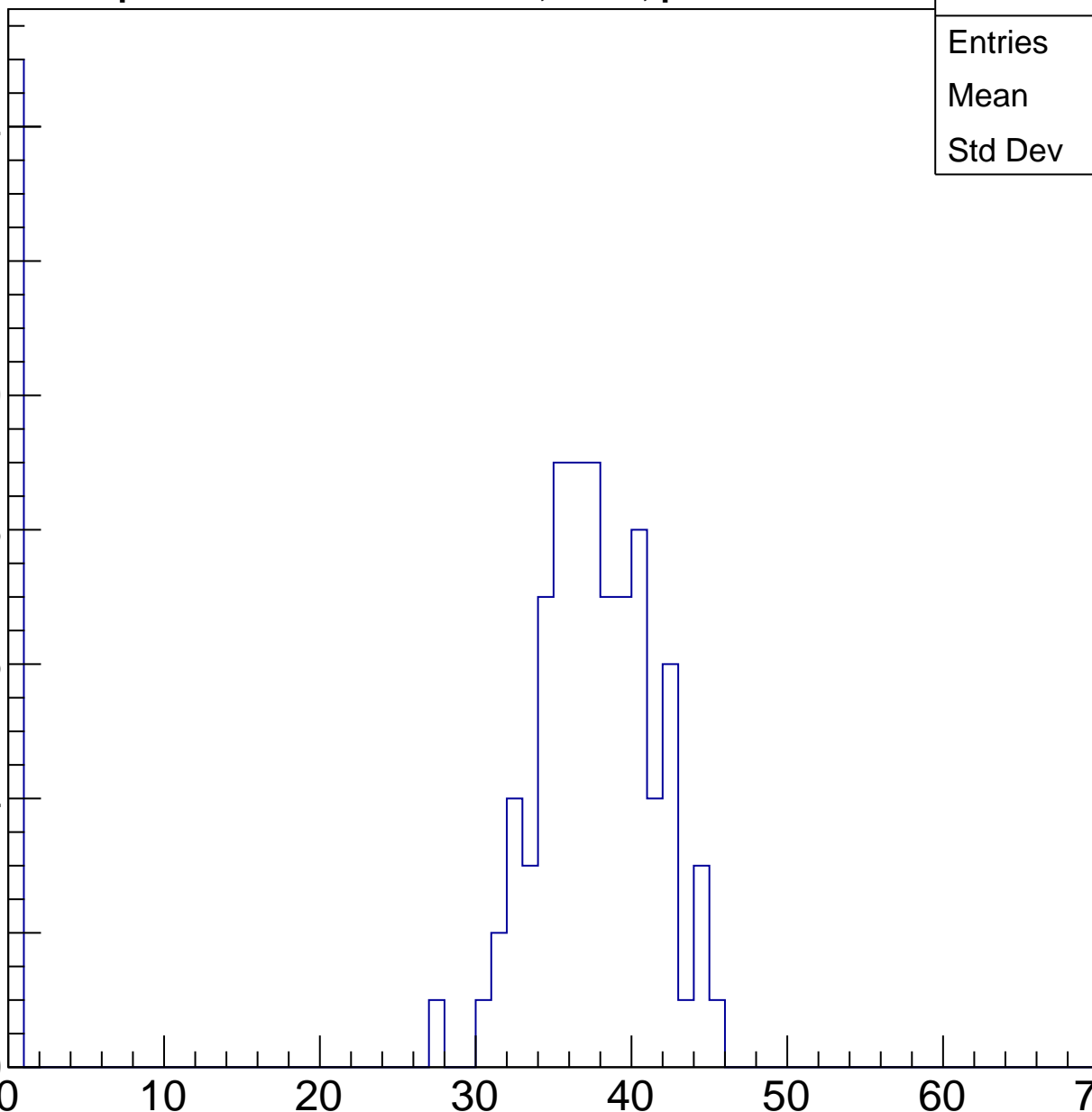
40

50

60

70

ampl

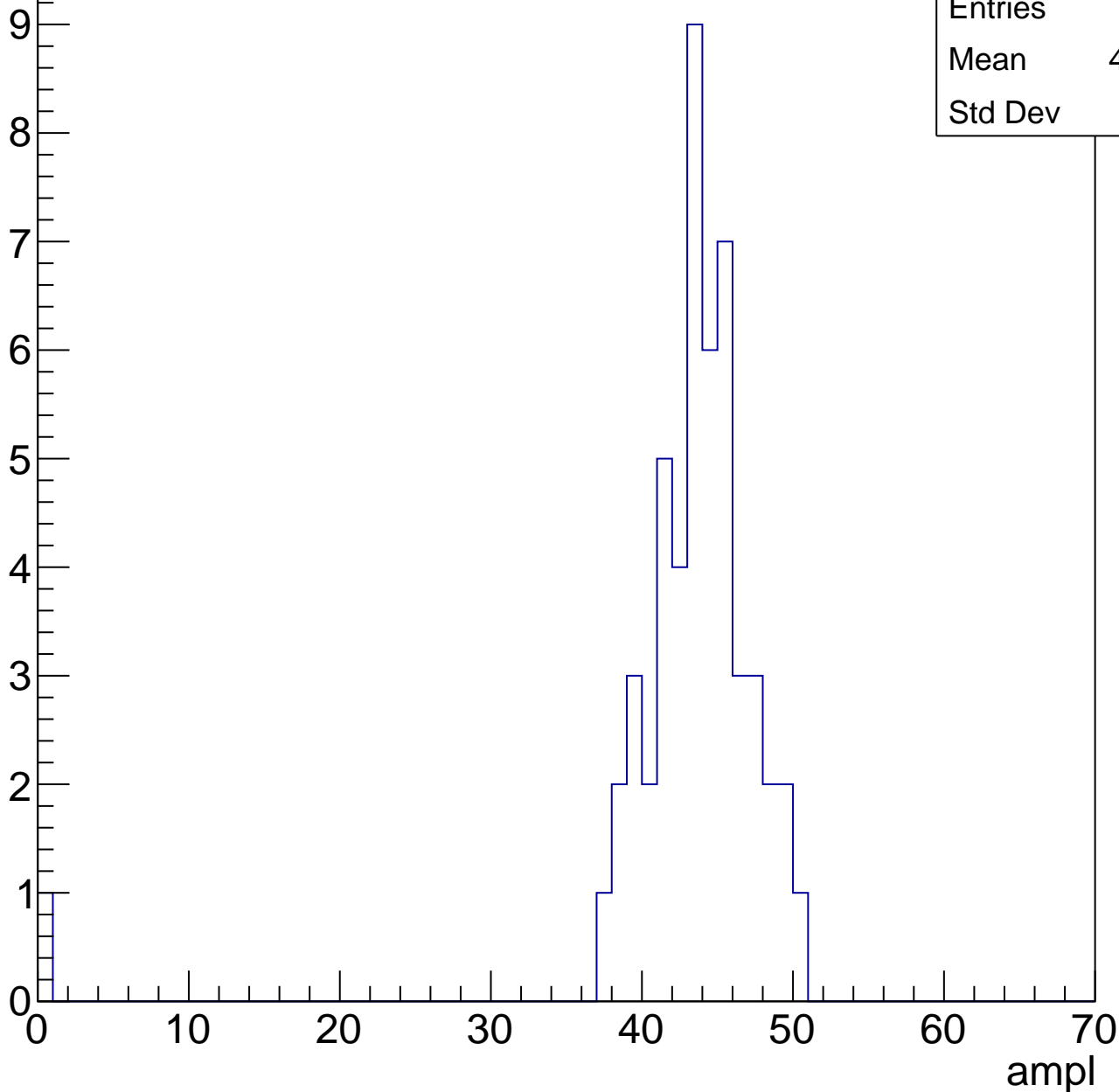


B1L103S, U9-ch17, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	42.59
Std Dev	6.71

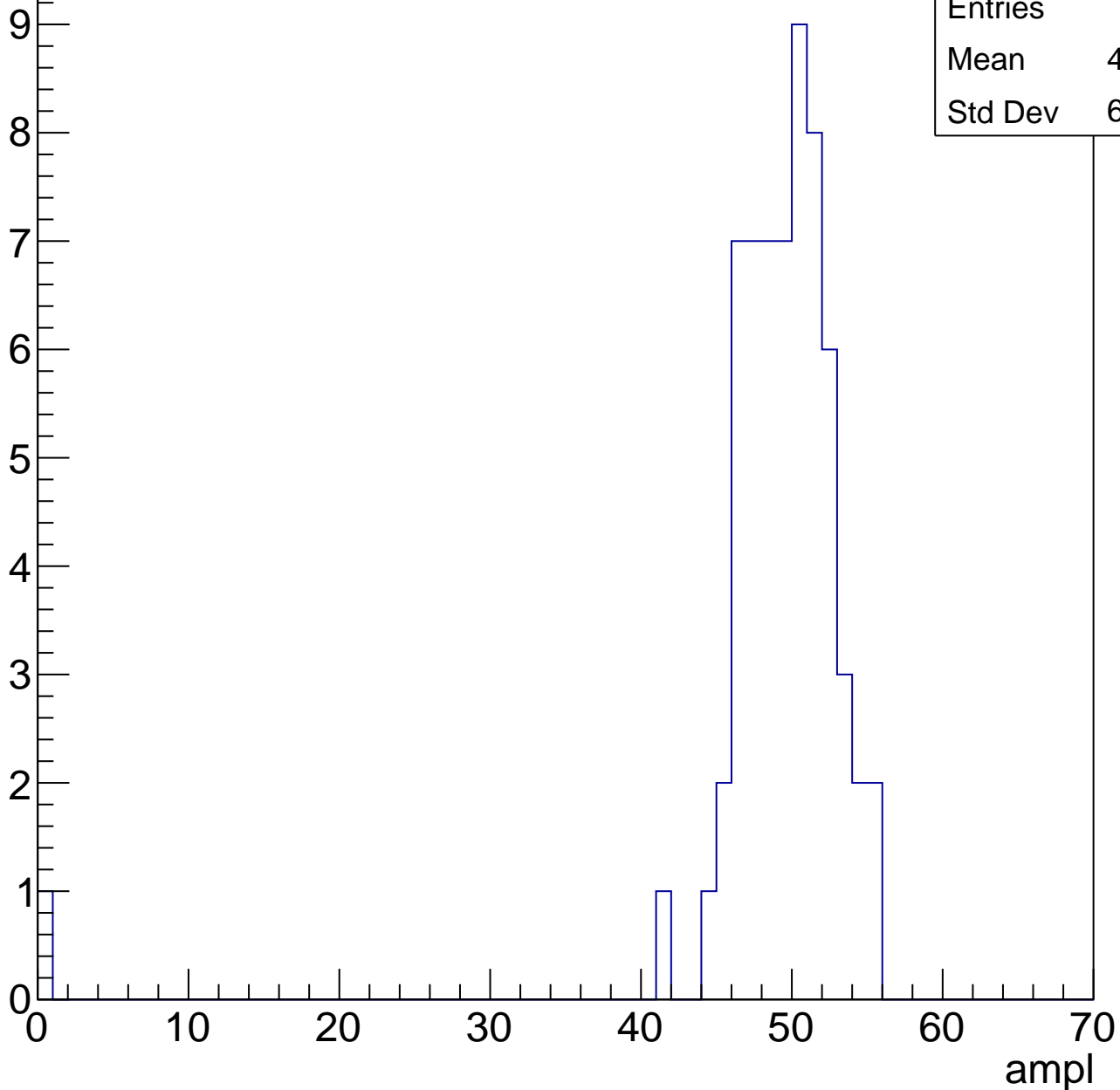


B1L103S, U9-ch17, adc3

calib_packv5_041523_1651.root, FC#0, port C2

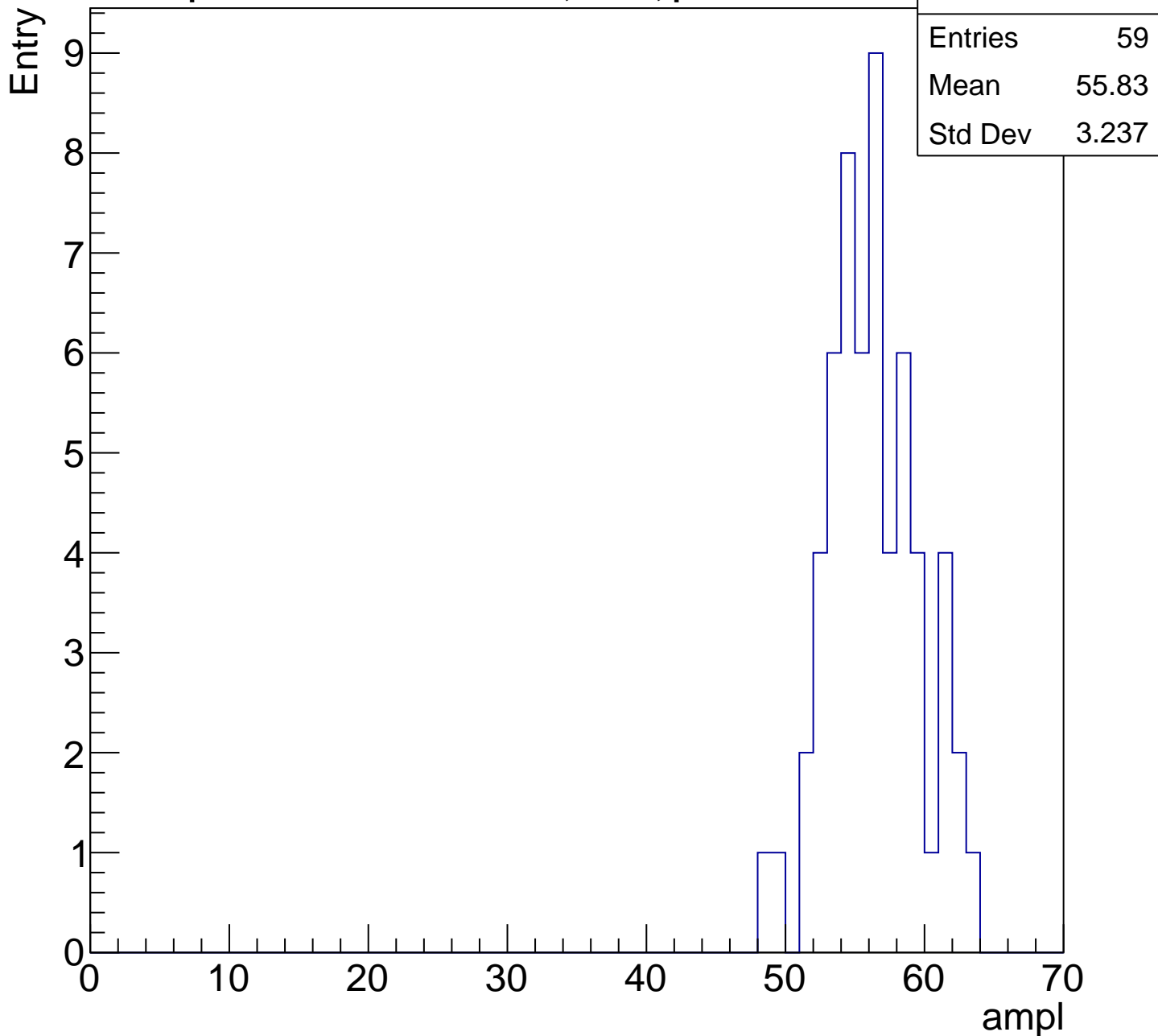
Entry

Entries	63
Mean	48.44
Std Dev	6.744



B1L103S, U9-ch17, adc4

calib_packv5_041523_1651.root, FC#0, port C2

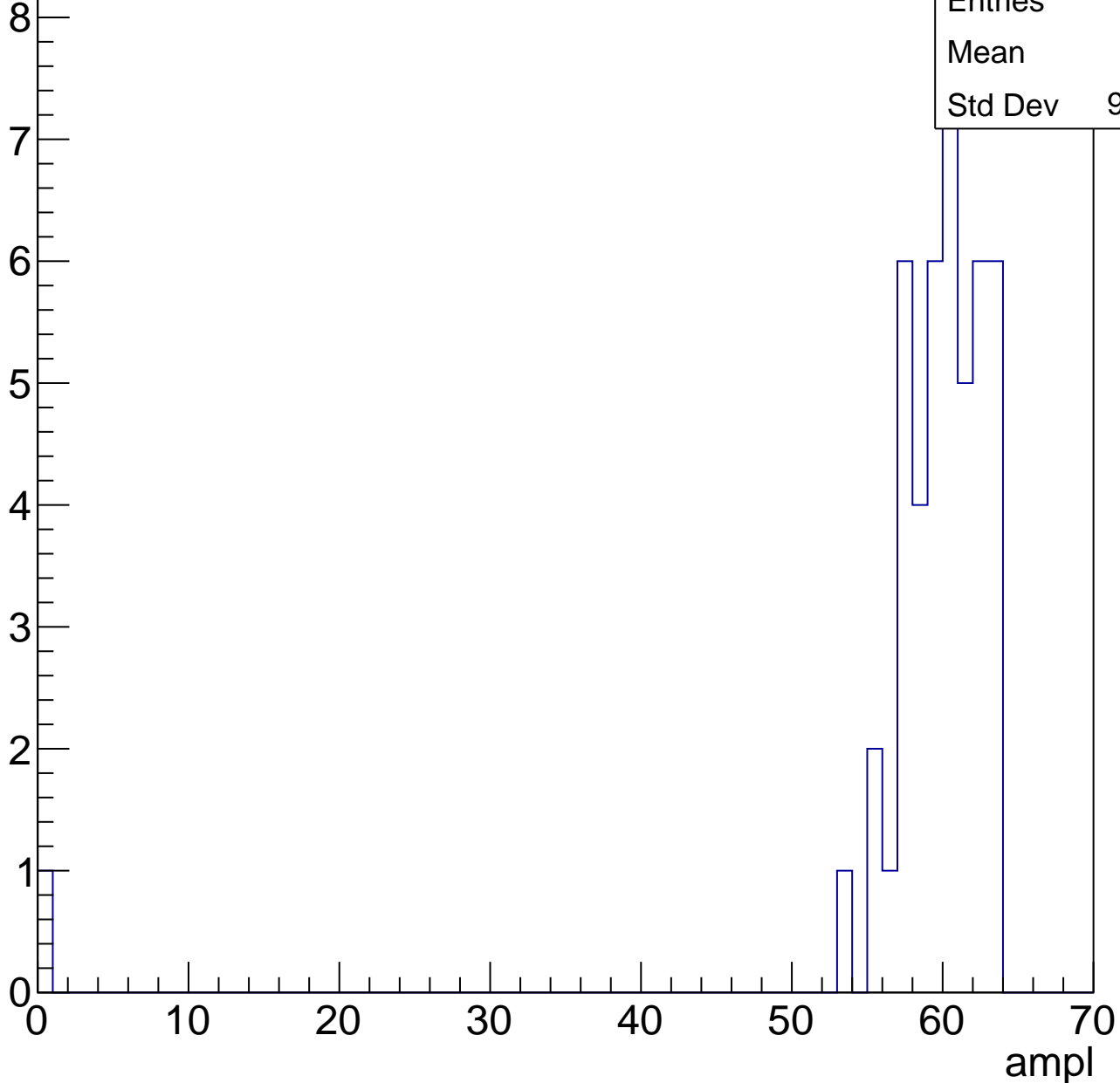


B1L103S, U9-ch17, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	46
Mean	58.3
Std Dev	9.019



B1L103S, U9-ch17, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch17, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch18, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	73
Mean	24.81
Std Dev	11.85

Entry

12

10

8

6

4

2

0

0

10

20

30

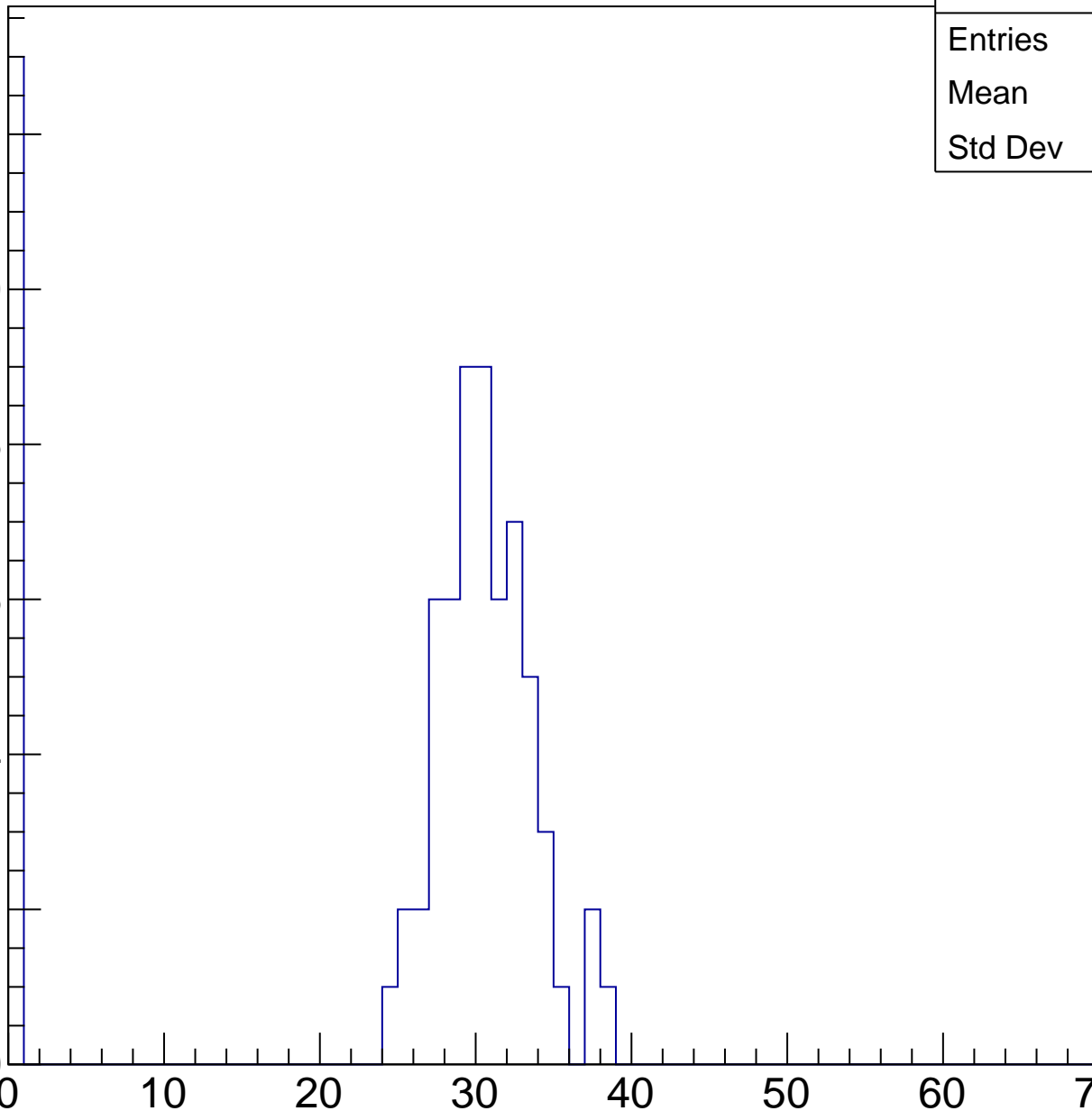
40

50

60

70

ampl

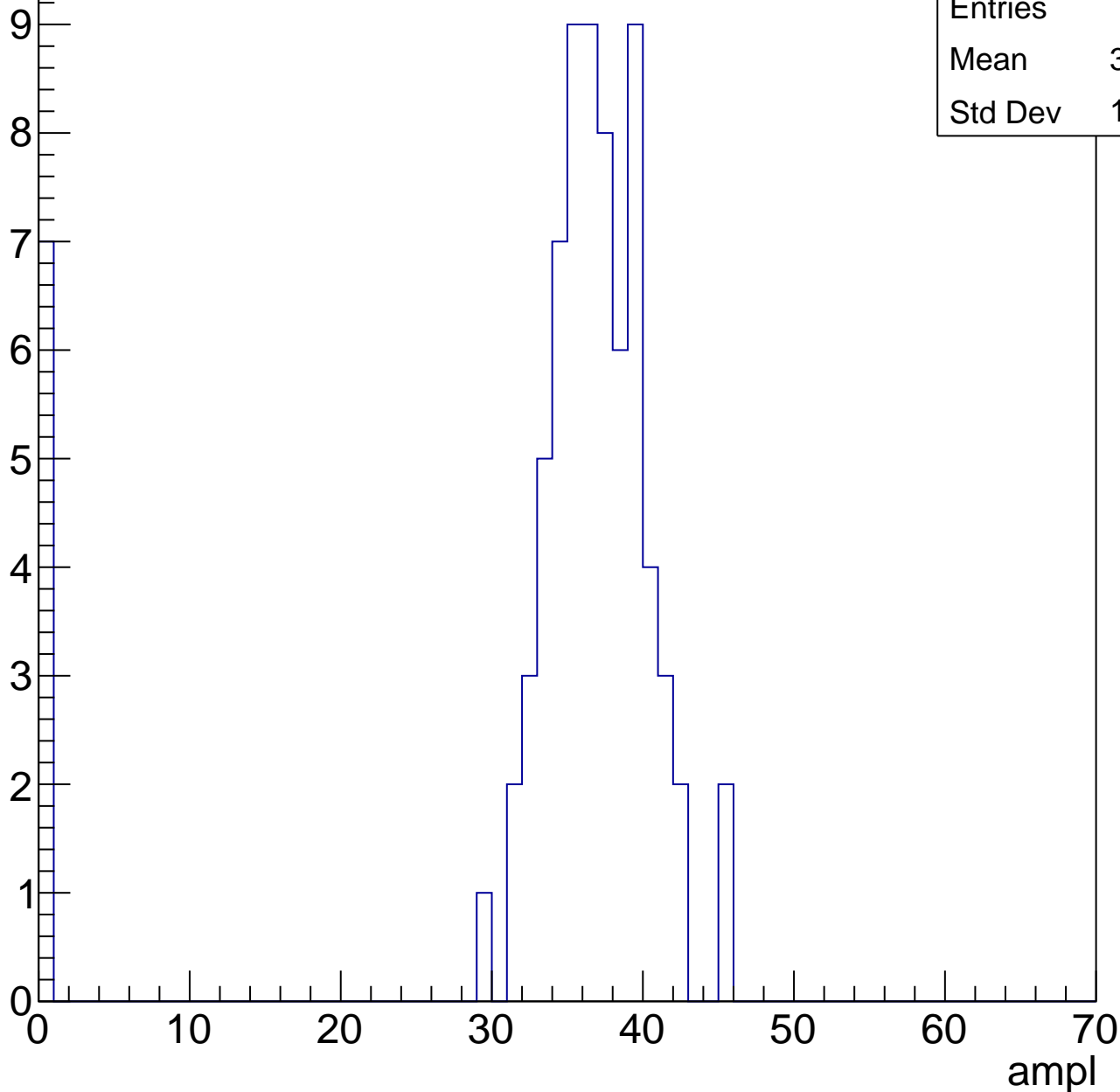


B1L103S, U9-ch18, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	33.26
Std Dev	10.94

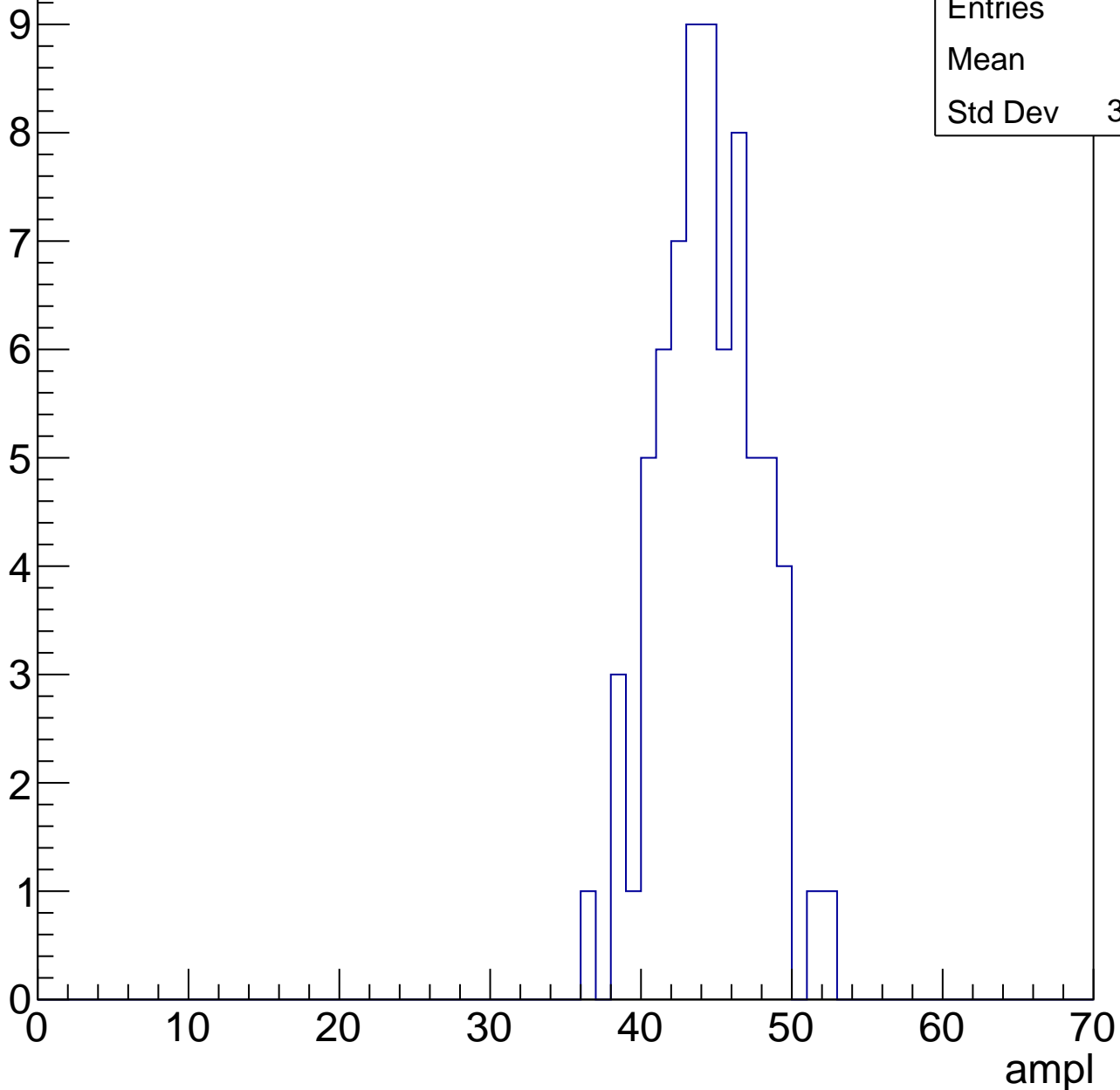


B1L103S, U9-ch18, adc2

calib_packv5_041523_1651.root, FC#0, port C2

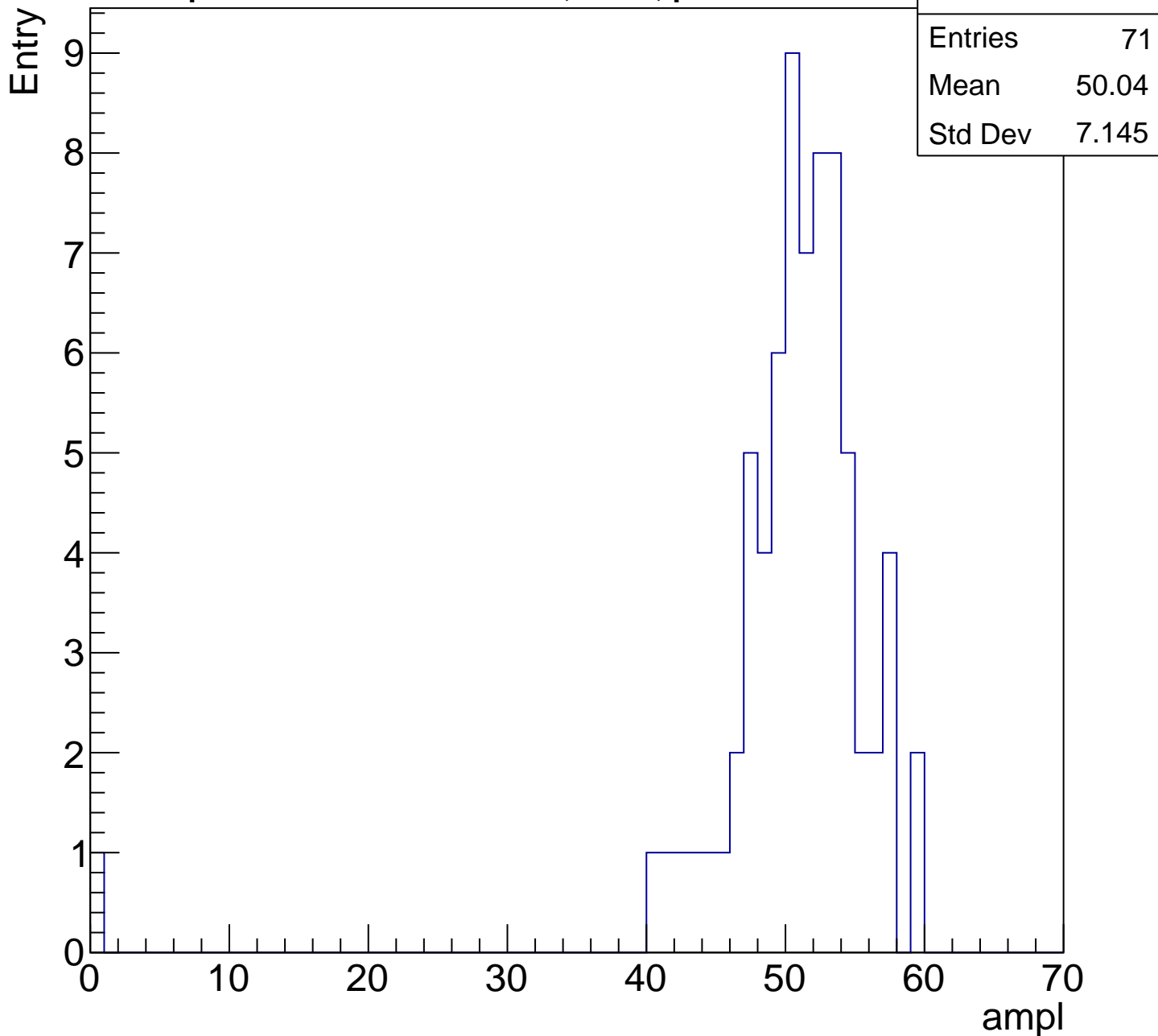
Entry

Entries	71
Mean	44
Std Dev	3.237



B1L103S, U9-ch18, adc3

calib_packv5_041523_1651.root, FC#0, port C2

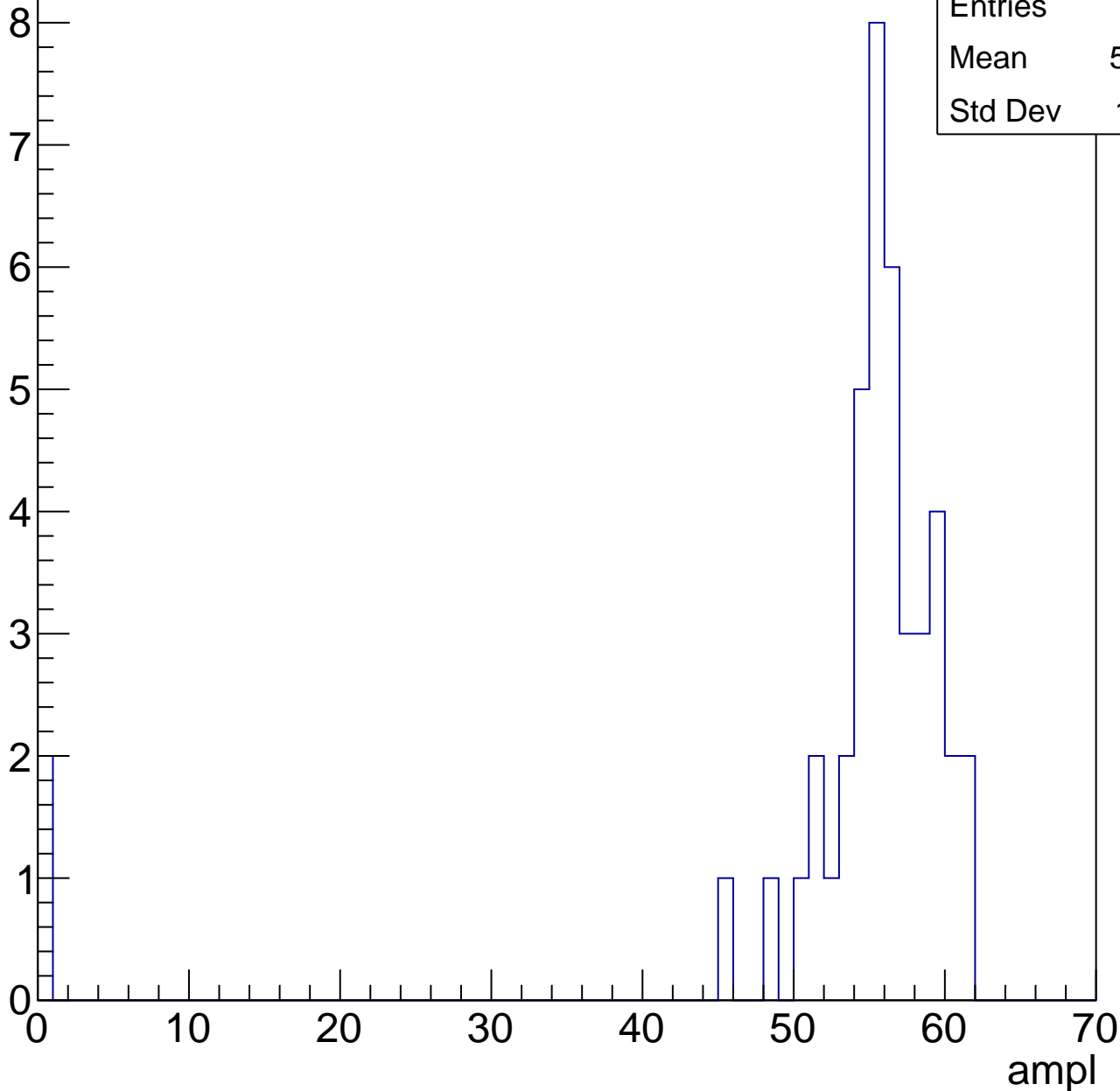


B1L103S, U9-ch18, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	43
Mean	52.84
Std Dev	12.11

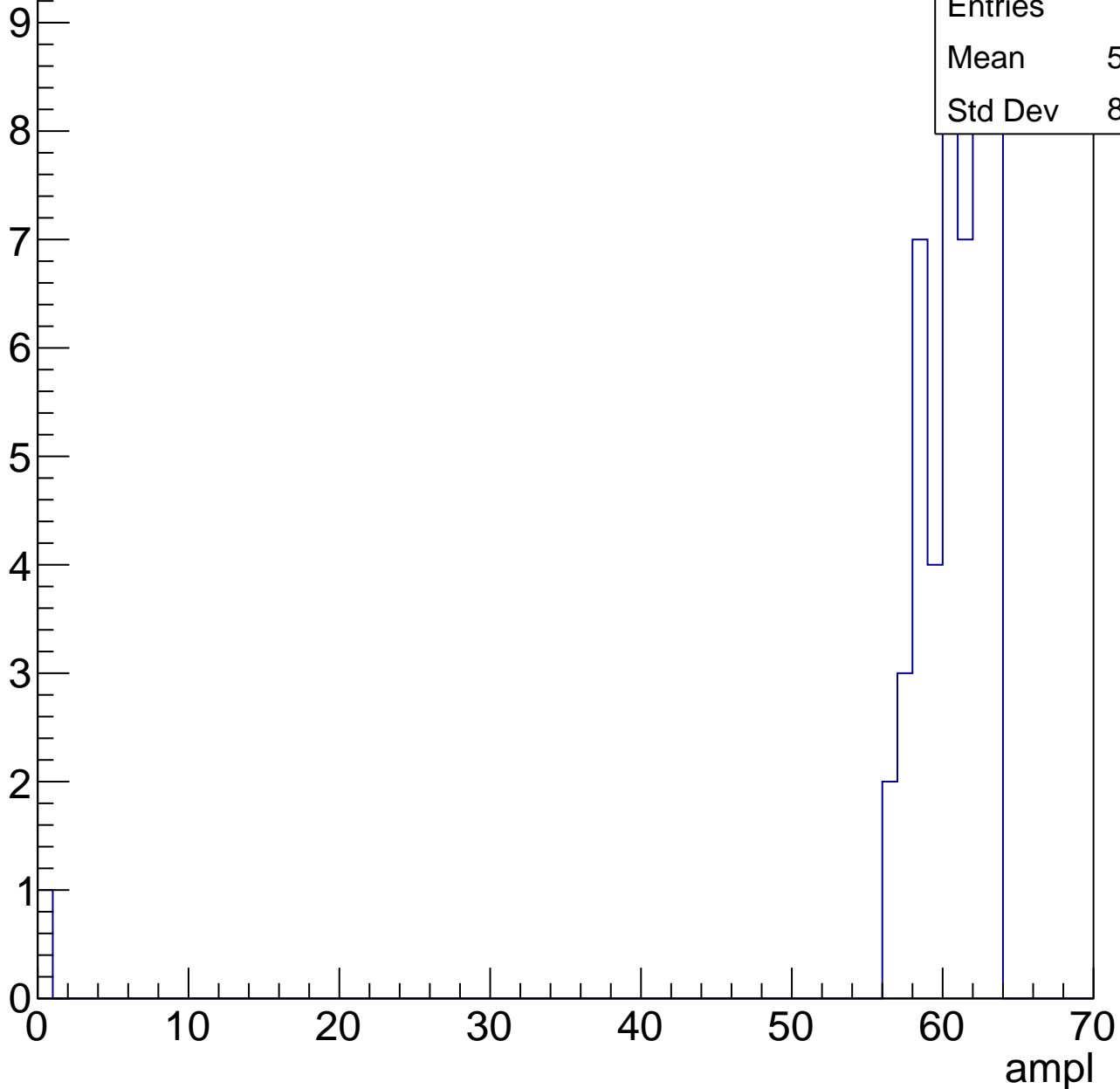


B1L103S, U9-ch18, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	59.06
Std Dev	8.763



B1L103S, U9-ch18, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	4
Mean	62.25
Std Dev	0.8292

B1L103S, U9-ch18, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U9-ch19, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	84
Mean	27.12
Std Dev	10.99

Entry

10

8

6

4

2

0

0

10

20

30

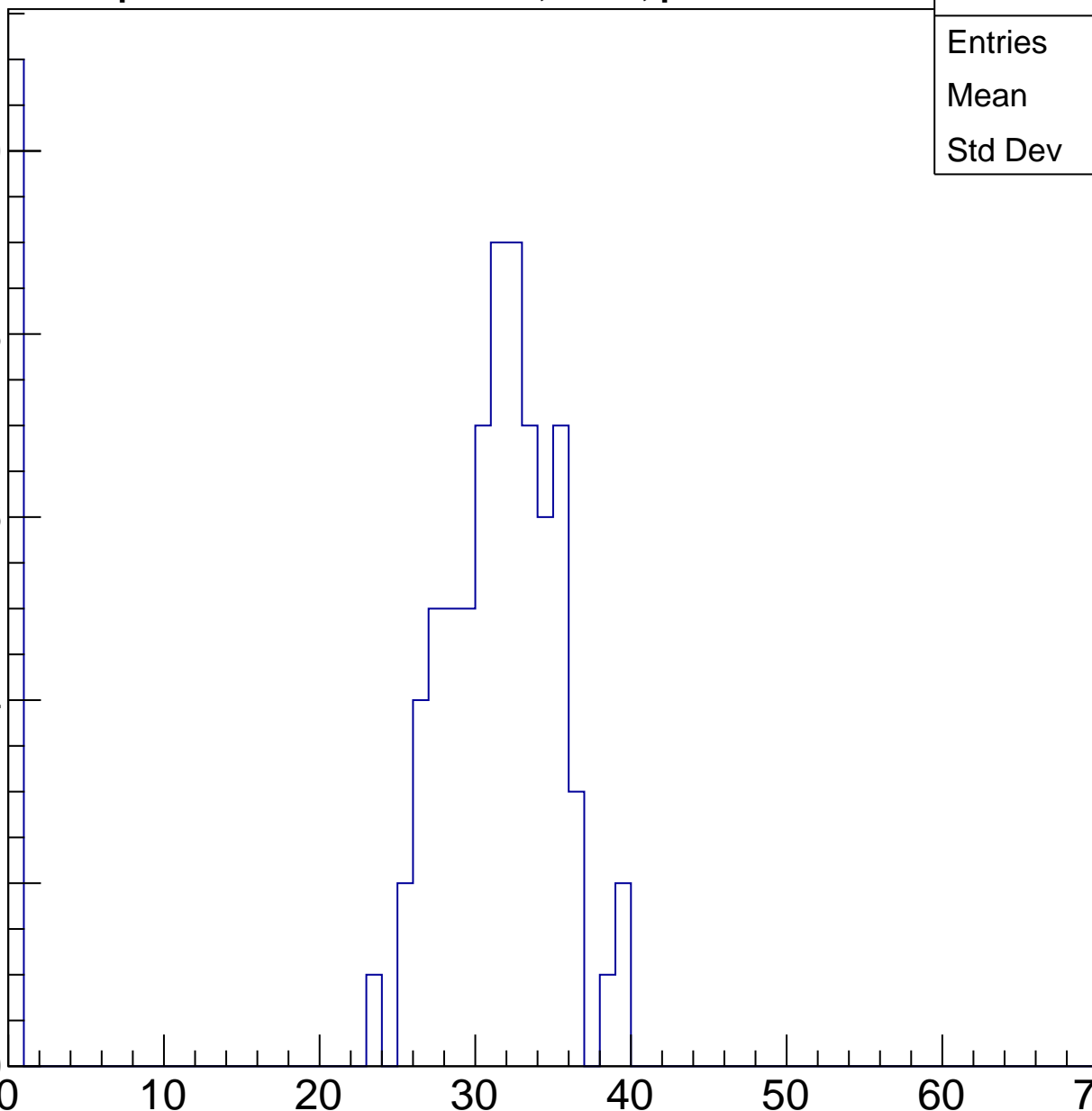
40

50

60

70

ampl

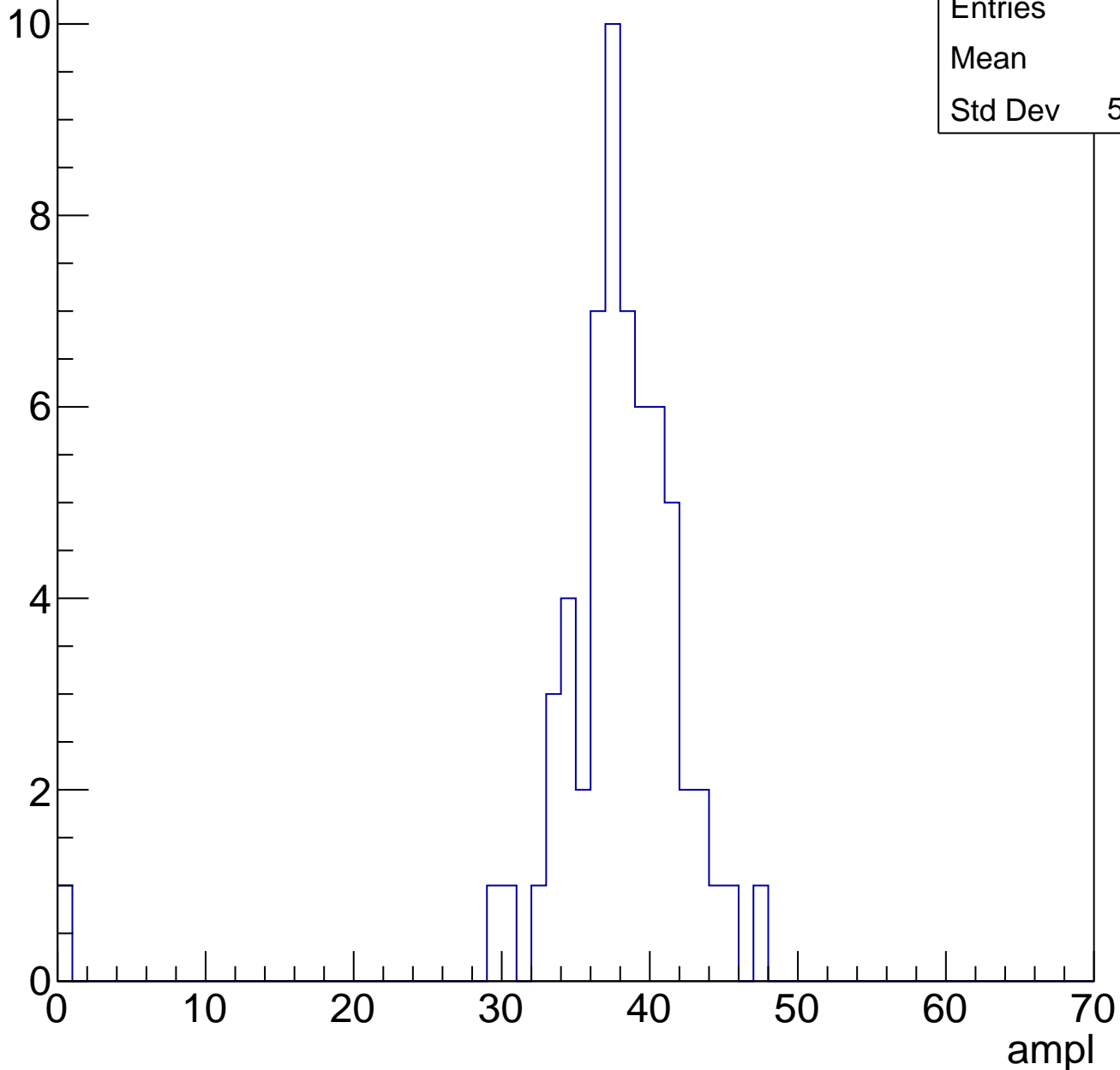


B1L103S, U9-ch19, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	61
Mean	37.2
Std Dev	5.872

Entry

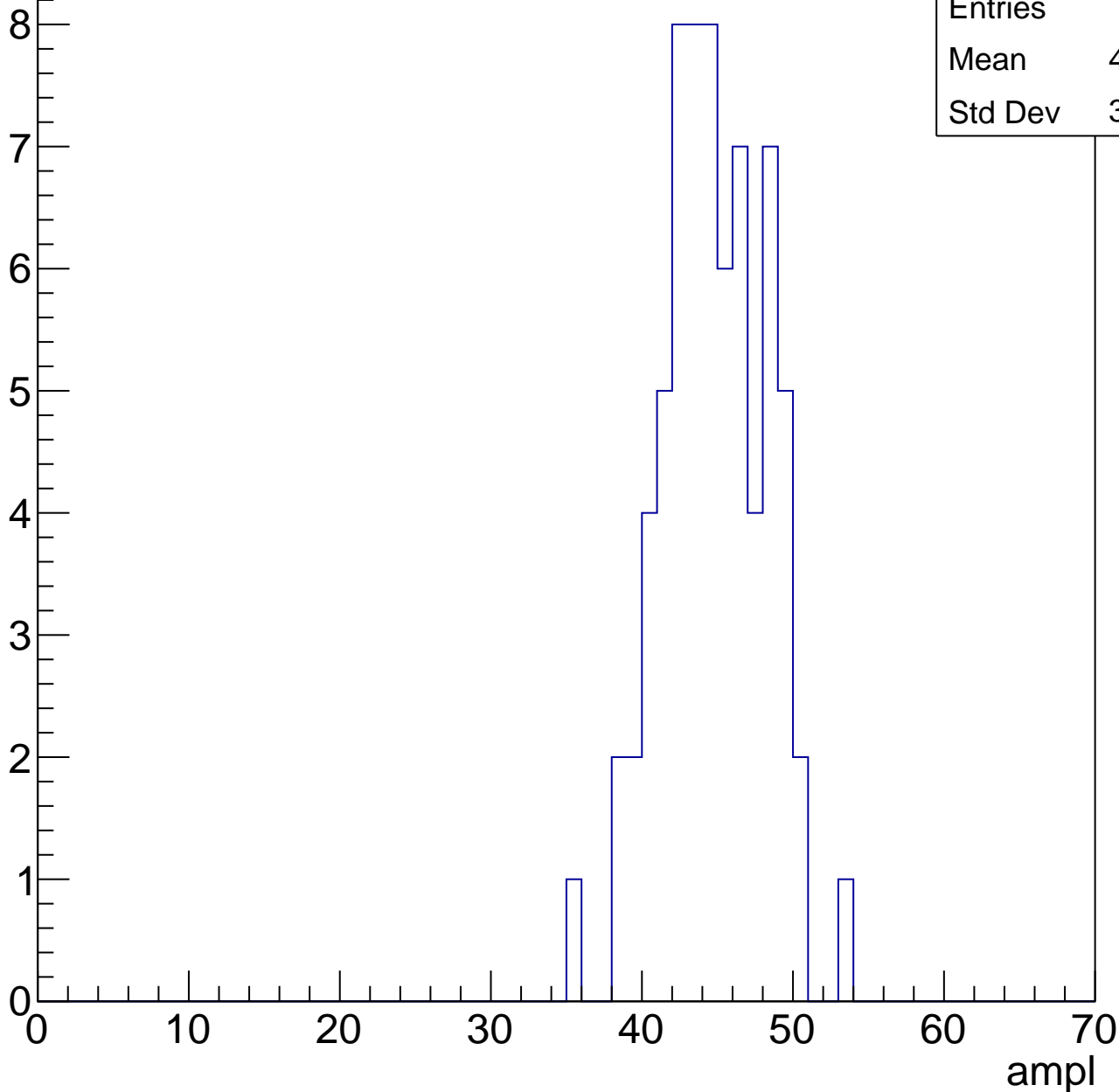


B1L103S, U9-ch19, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

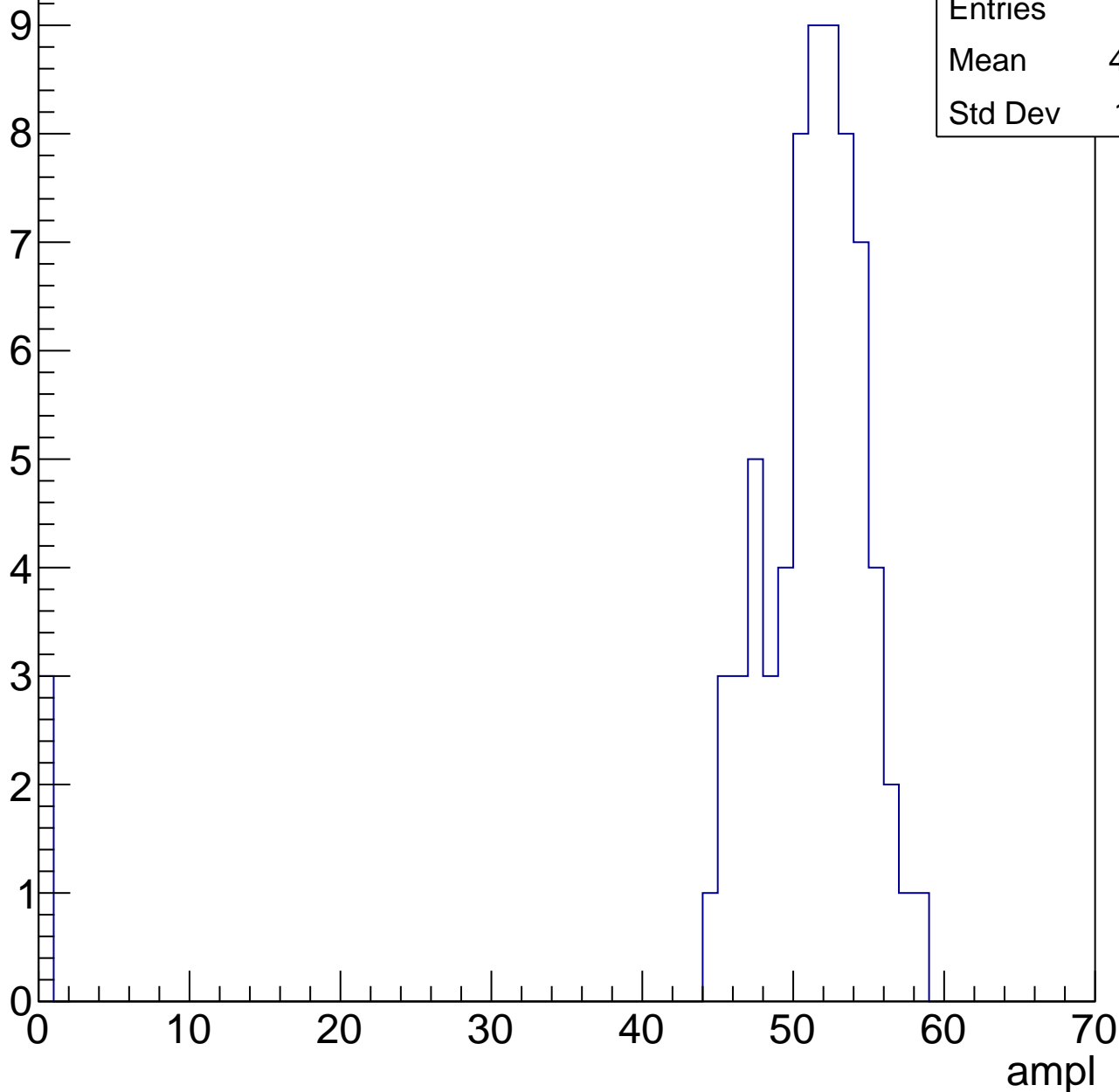
Entries	70
Mean	44.29
Std Dev	3.394



B1L103S, U9-ch19, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

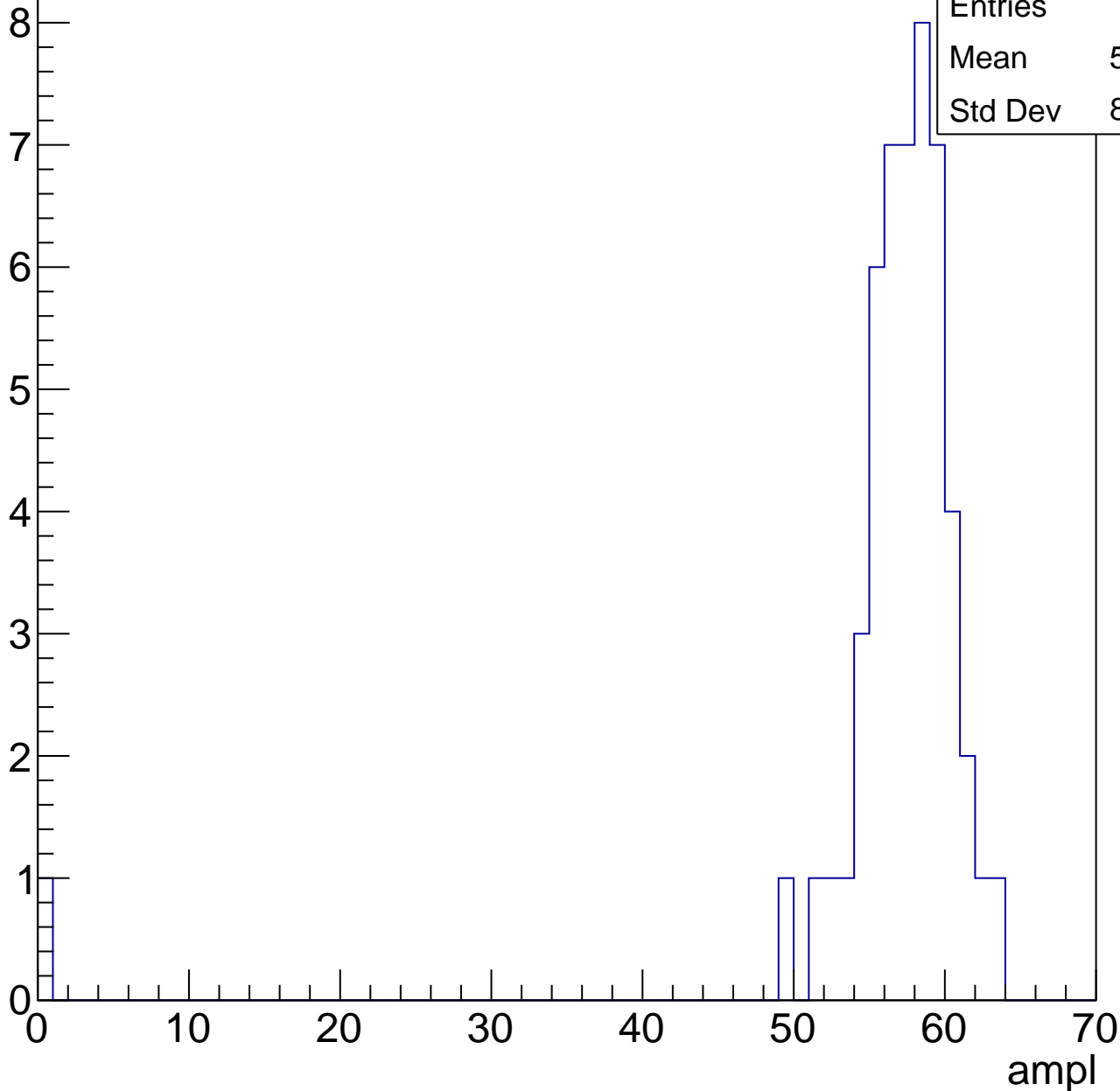


B1L103S, U9-ch19, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	55.92
Std Dev	8.347

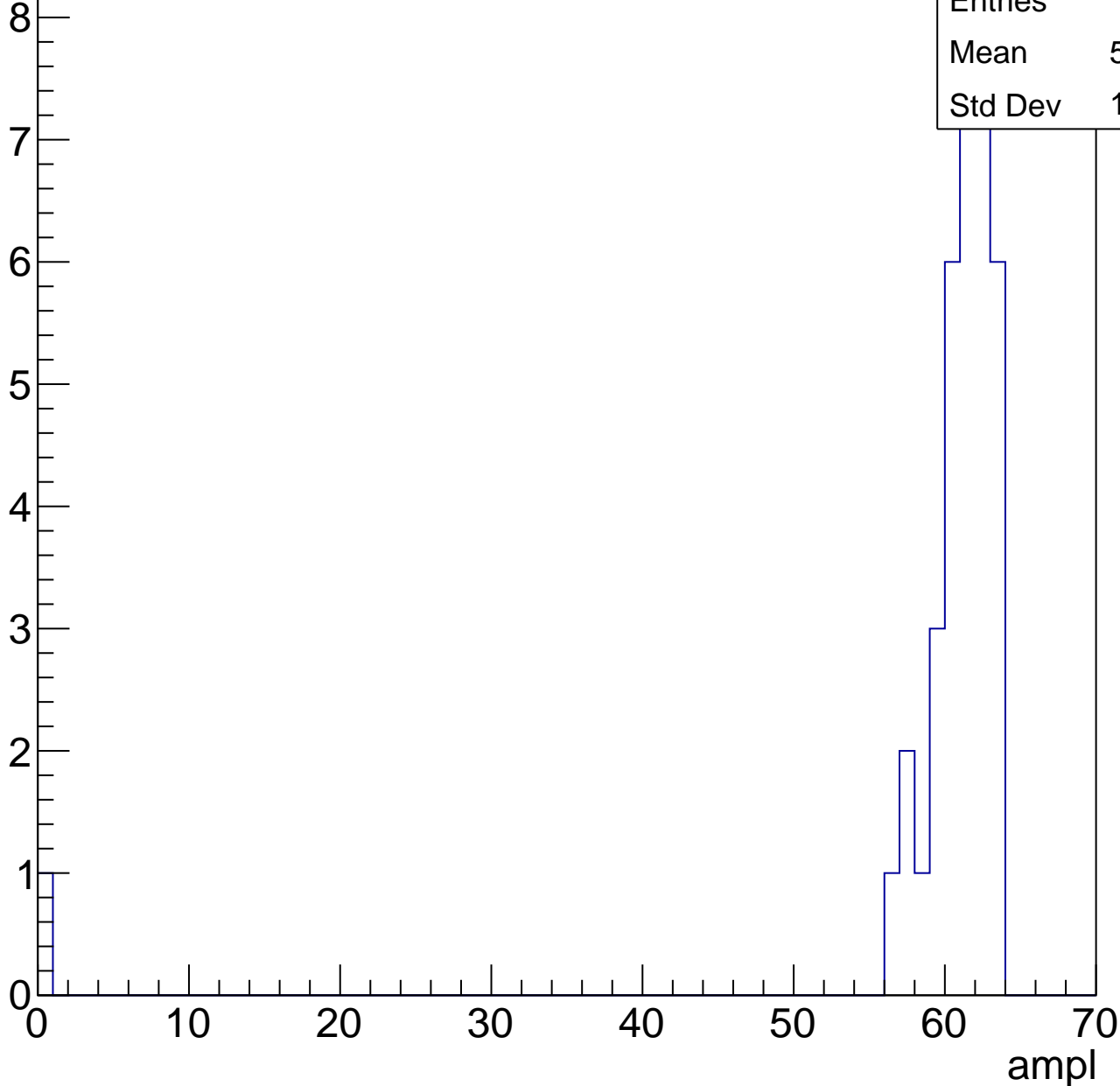


B1L103S, U9-ch19, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

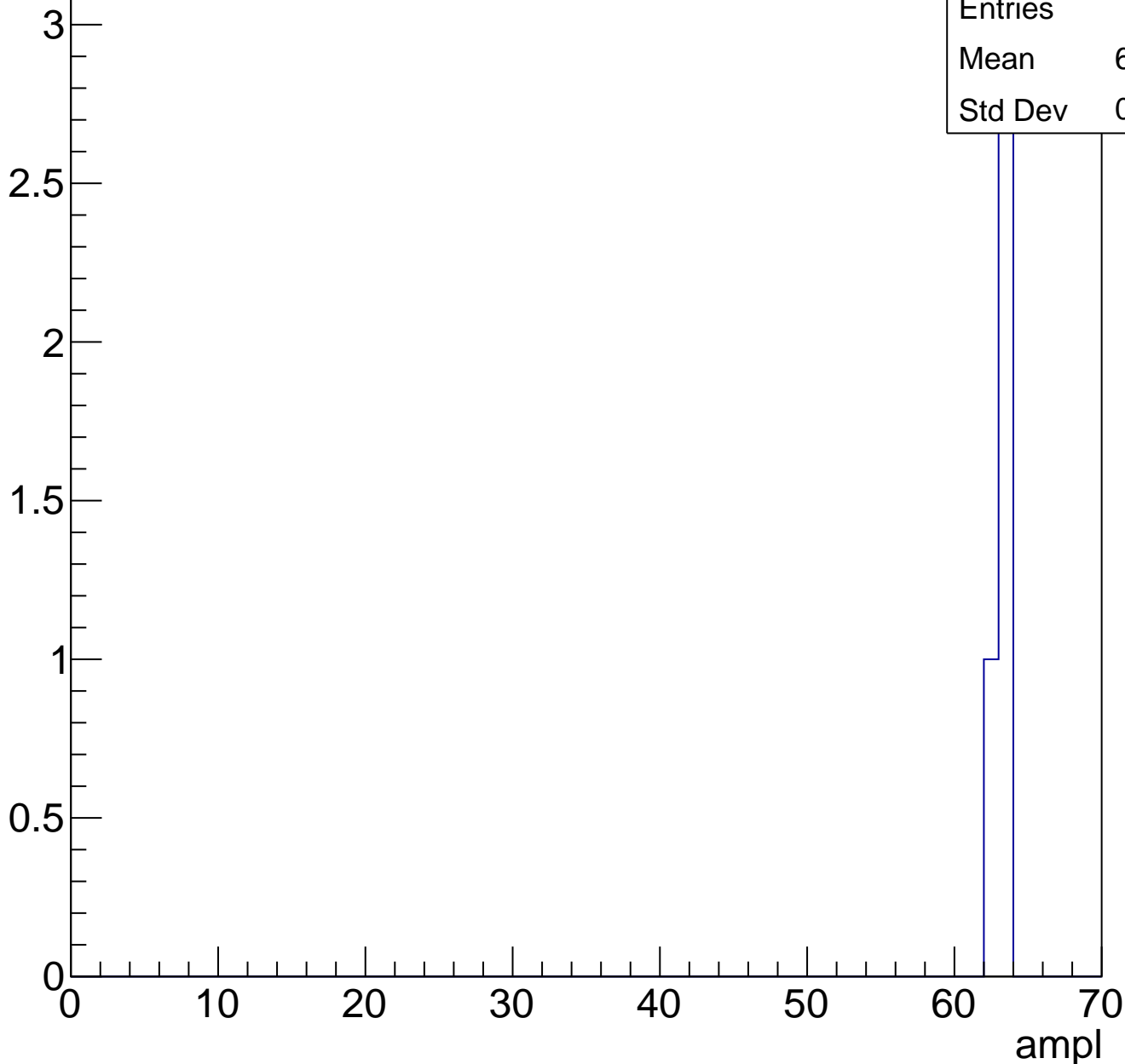
Entries	36
Mean	59.08
Std Dev	10.14



B1L103S, U9-ch19, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	4
Mean	62.75
Std Dev	0.433

B1L103S, U9-ch19, adc7

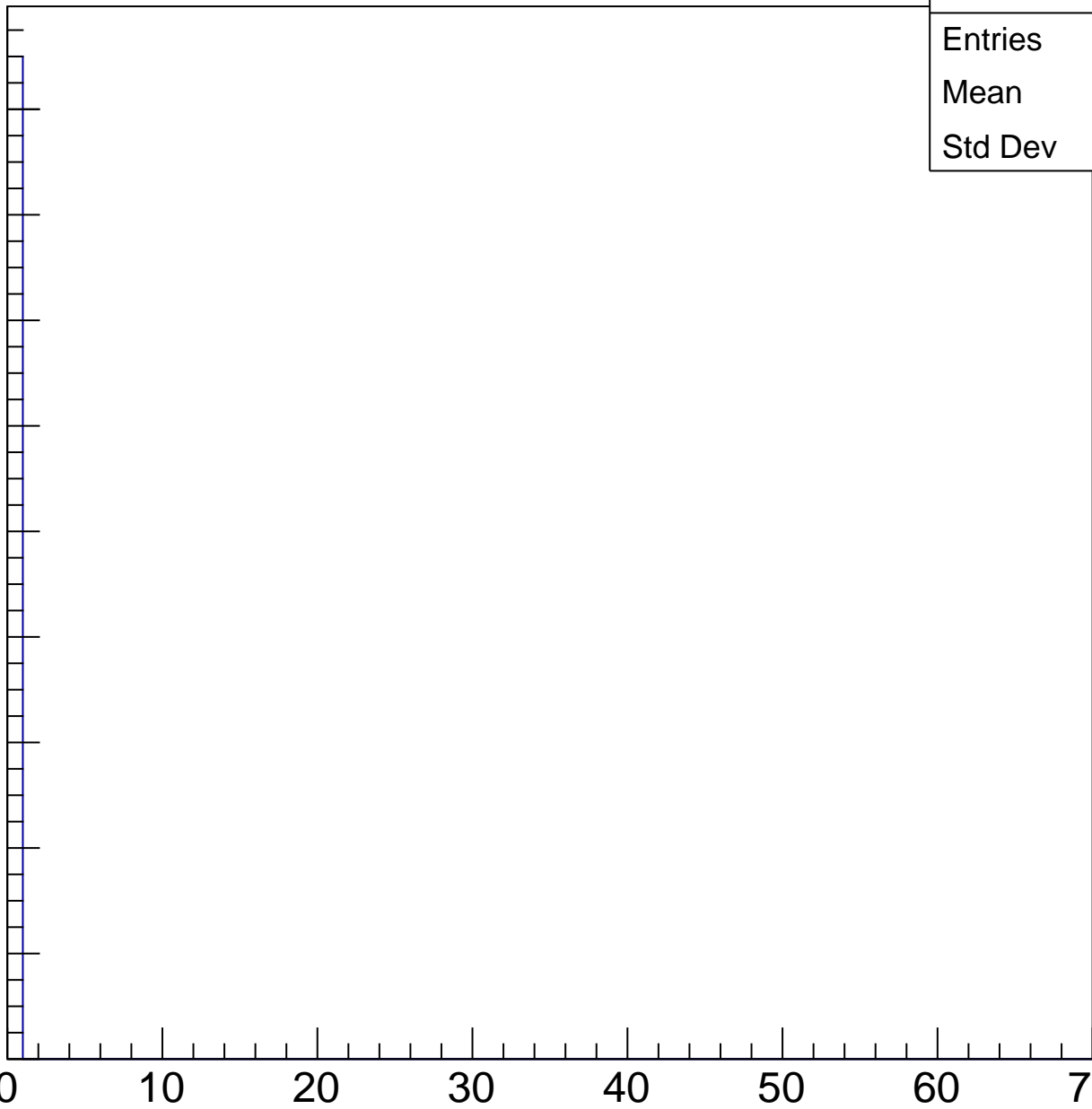
calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

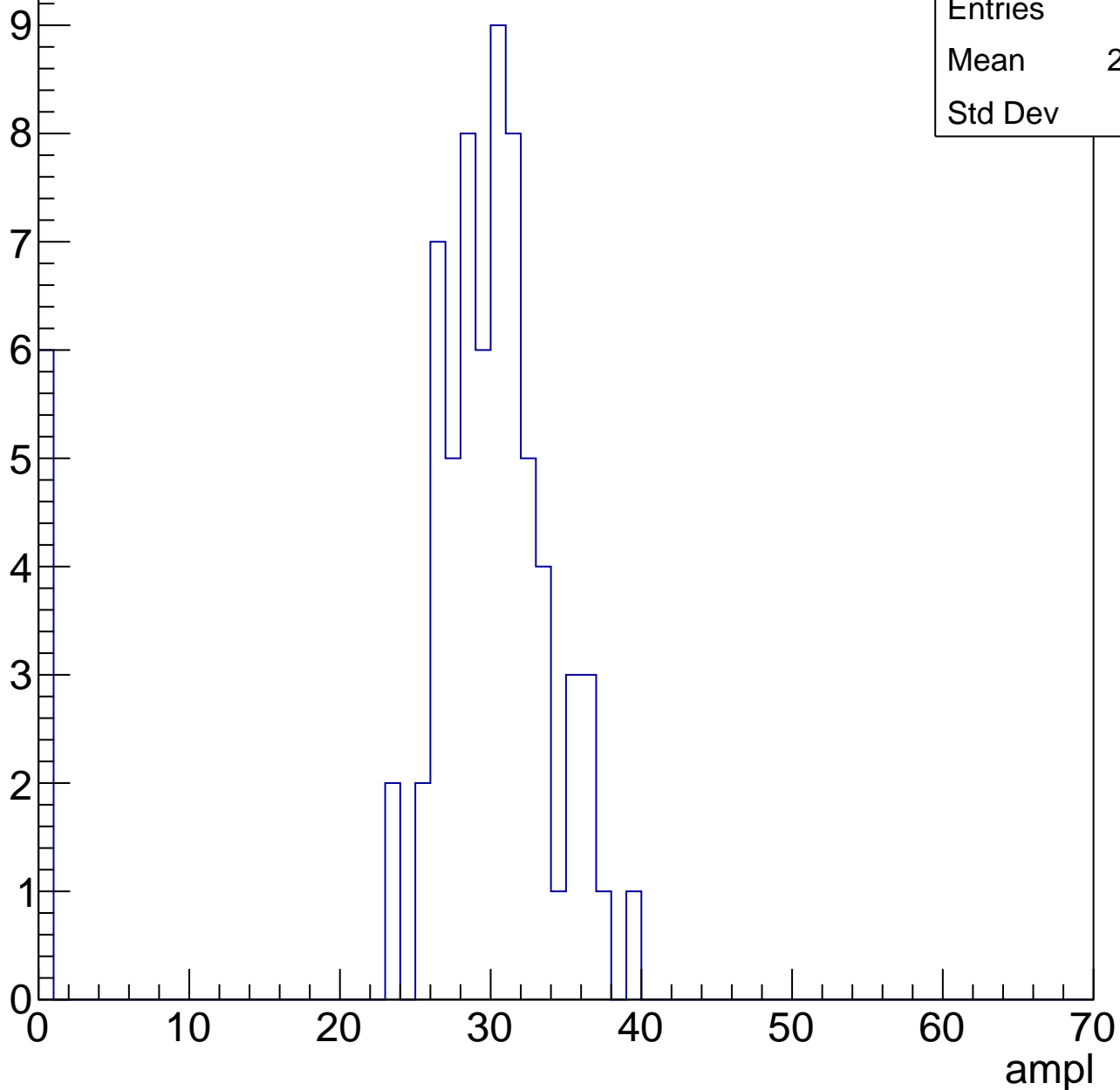


B1L103S, U9-ch20, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	27.38
Std Dev	8.92

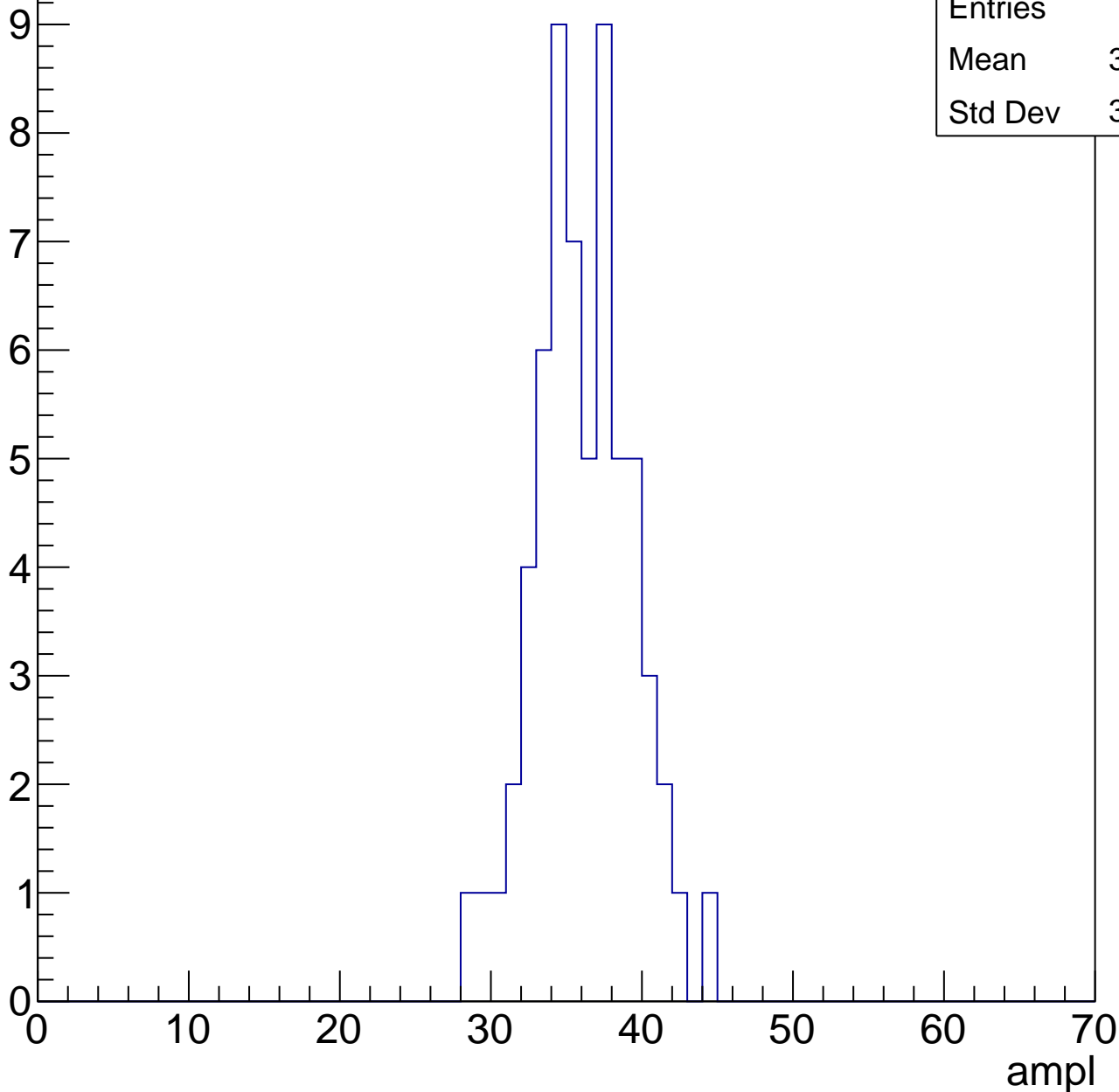


B1L103S, U9-ch20, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	35.68
Std Dev	3.176



B1L103S, U9-ch20, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	77
Mean	34.83
Std Dev	15.92

Entry

12

10

8

6

4

2

0

0

10

20

30

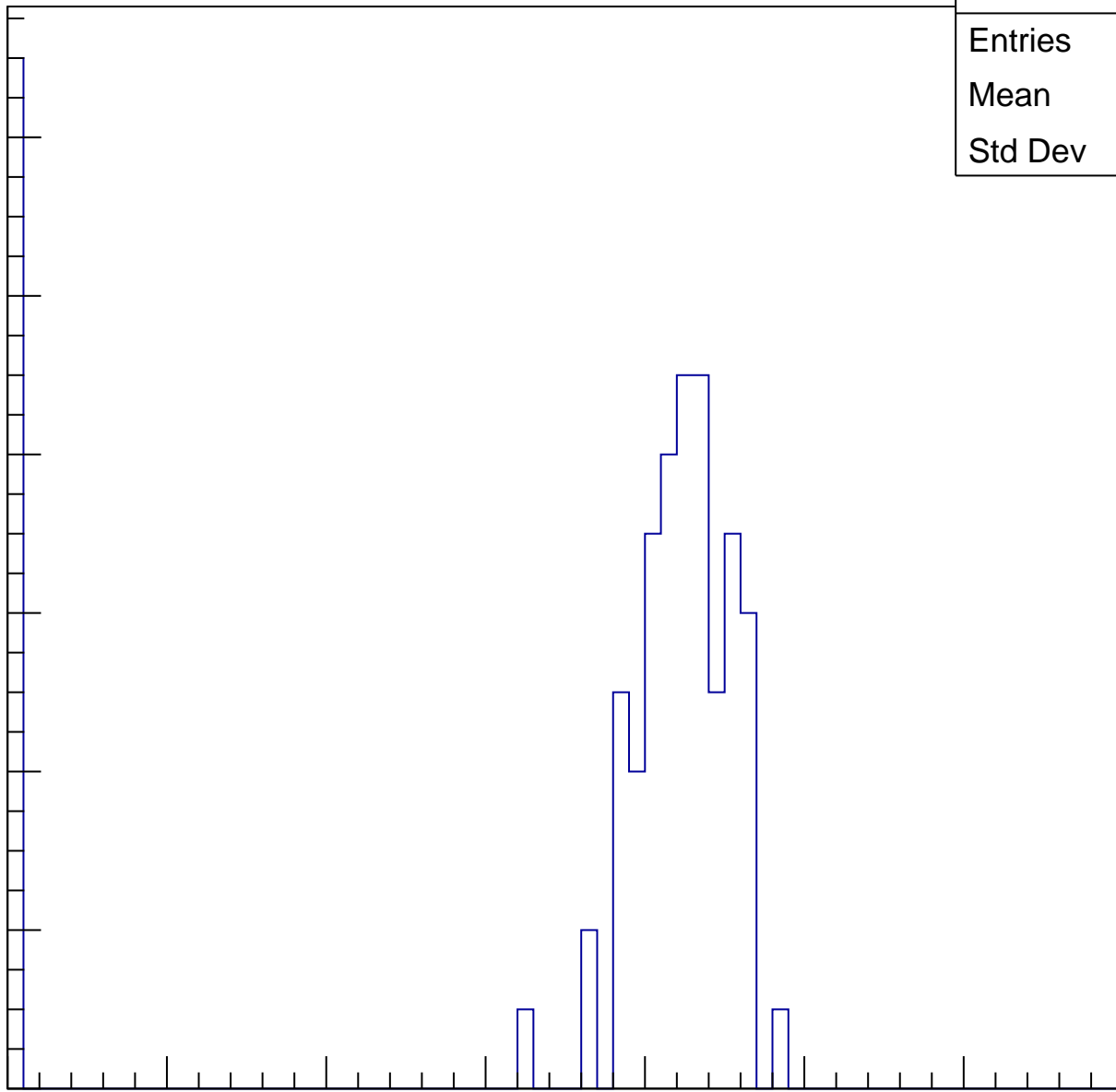
40

50

60

70

ampl

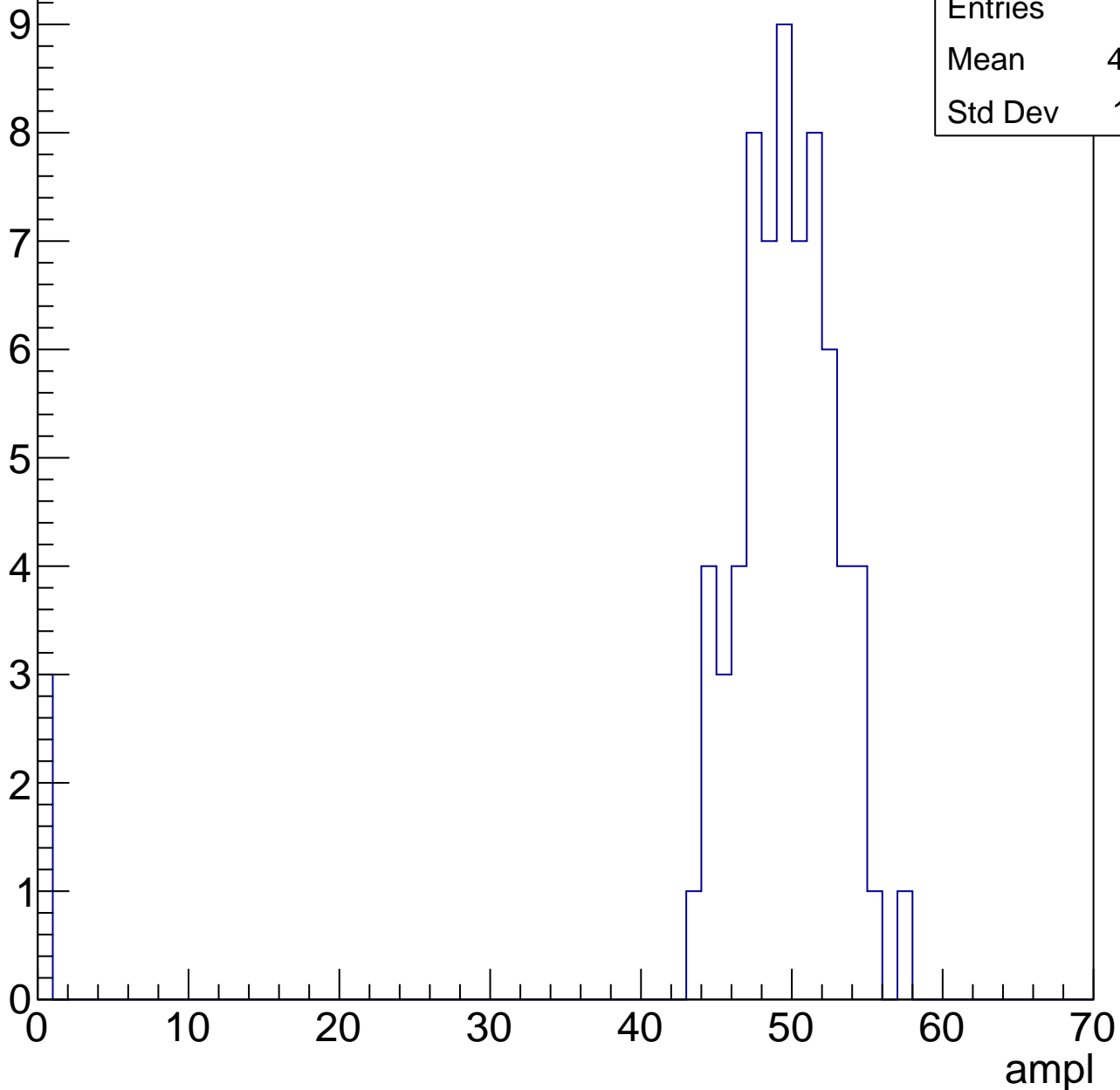


B1L103S, U9-ch20, adc3

calib_packv5_041523_1651.root, FC#0, port C2

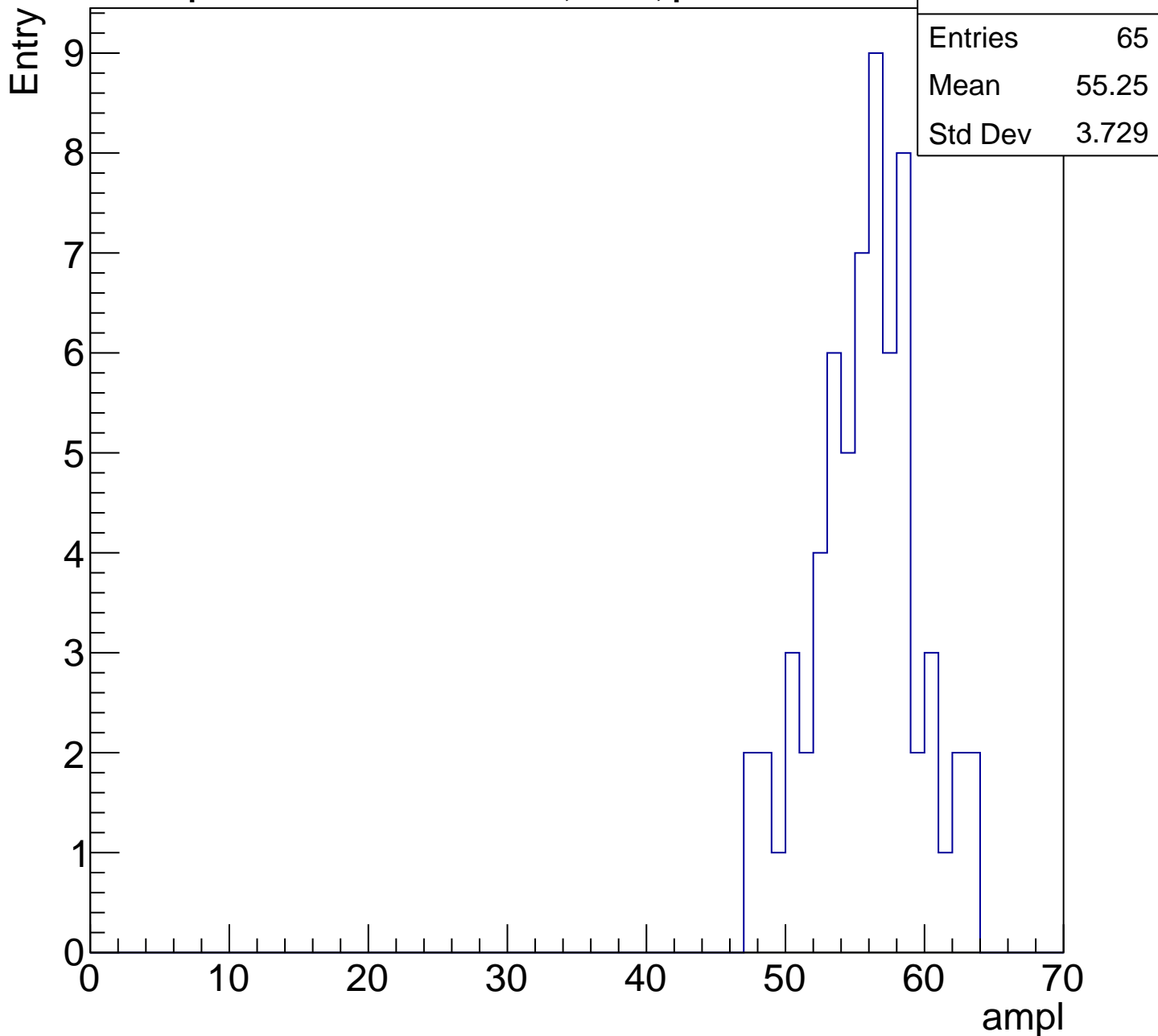
Entry

Entries	70
Mean	47.16
Std Dev	10.41



B1L103S, U9-ch20, adc4

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U9-ch20, adc5

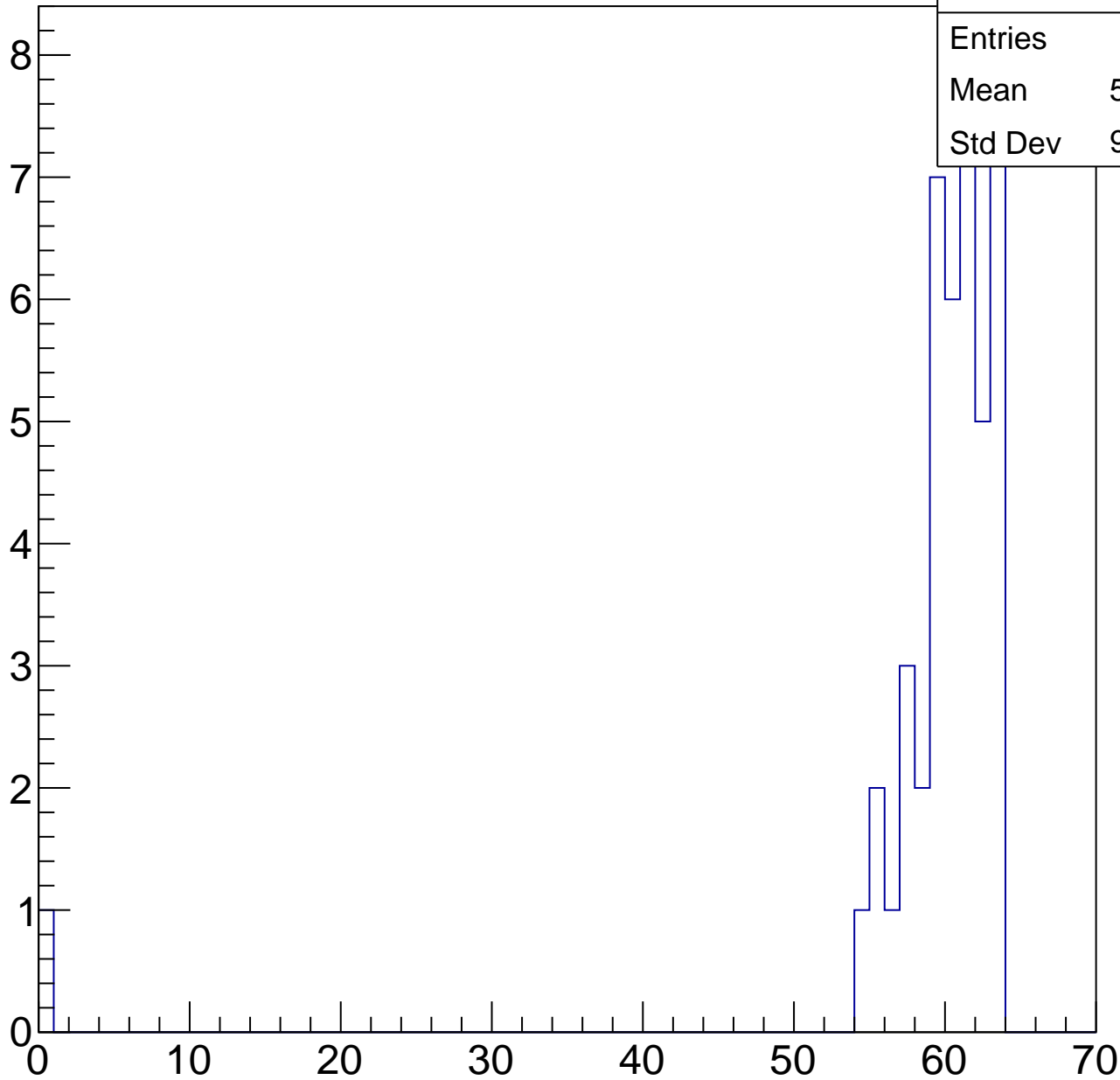
calib_packv5_041523_1651.root, FC#0, port C2

Entry

8
7
6
5
4
3
2
1
0

Entries	44
Mean	58.68
Std Dev	9.253

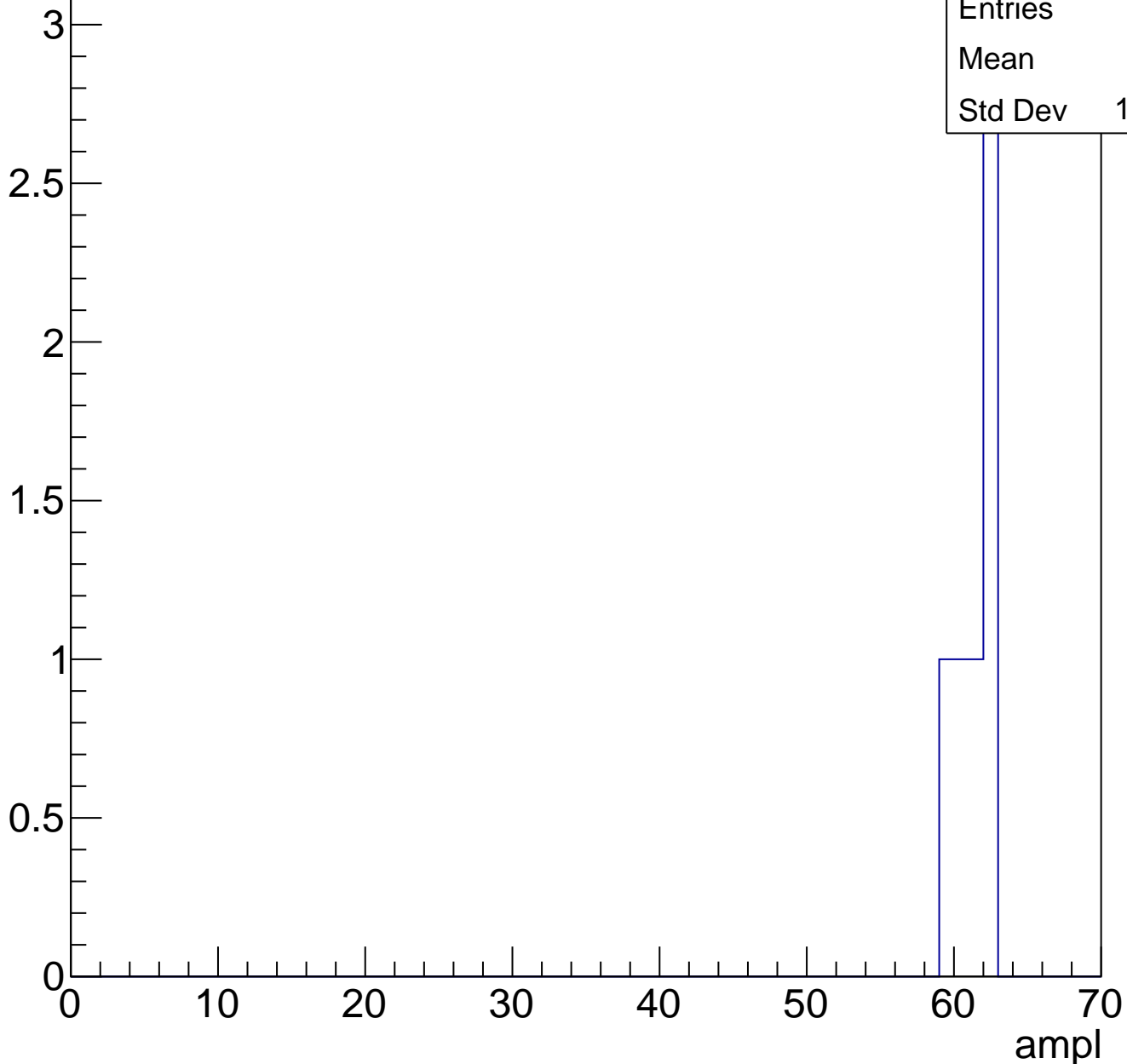
ampl



B1L103S, U9-ch20, adc6

calib_packv5_041523_1651.root, FC#0, port C2

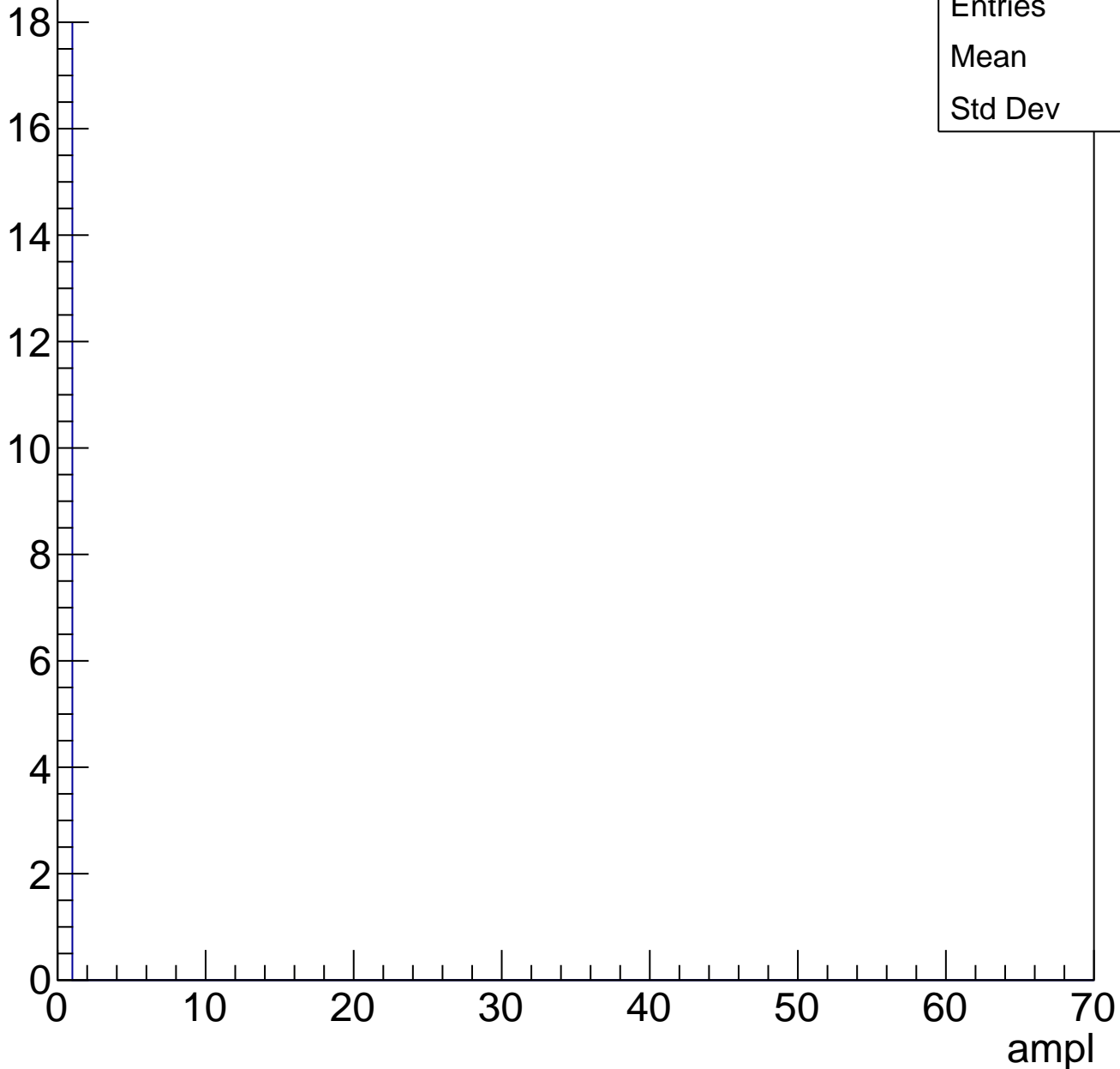
Entry



B1L103S, U9-ch20, adc7

calib_packv5_041523_1651.root, FC#0, port C2

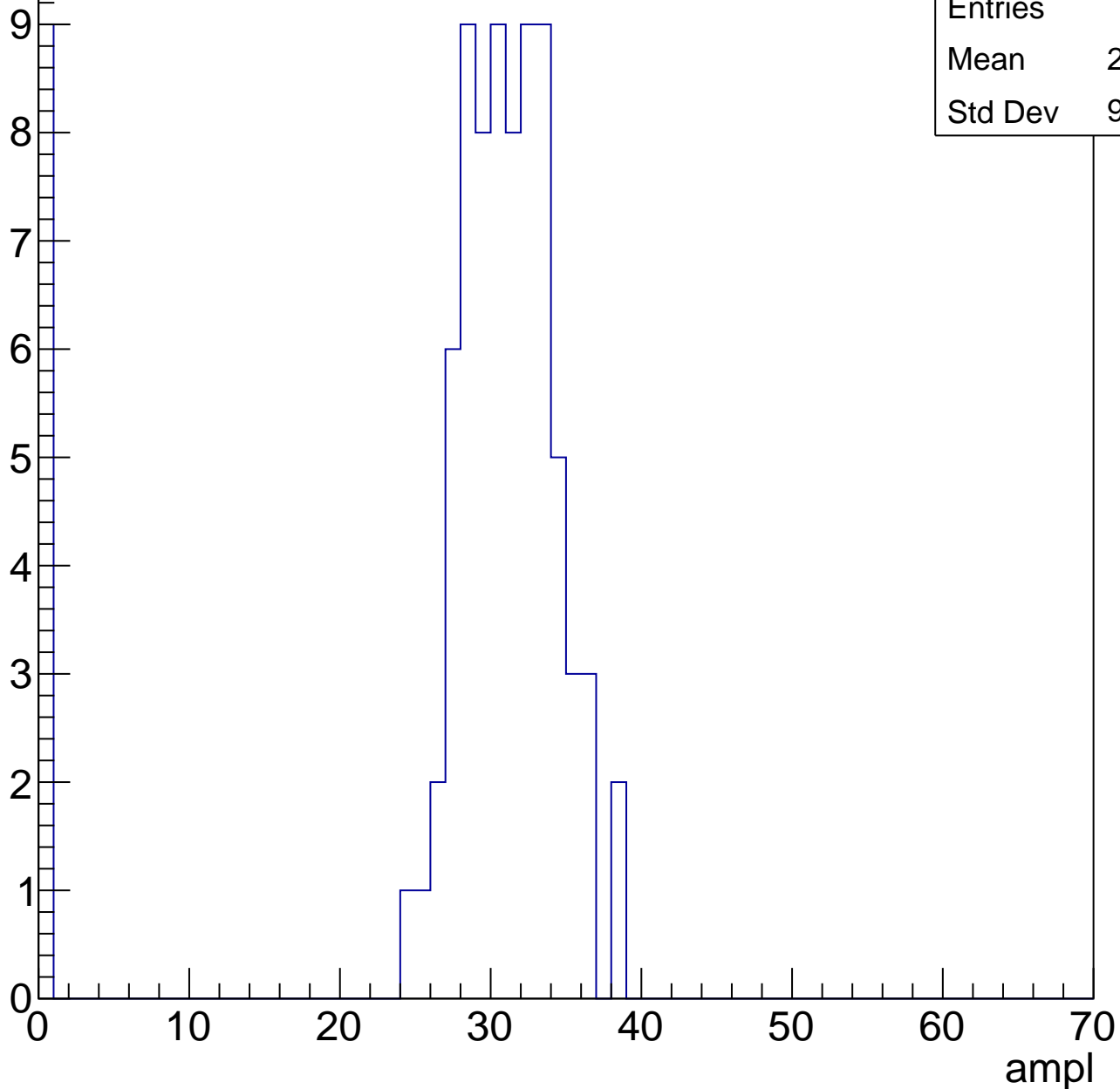
Entry



B1L103S, U9-ch21, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry



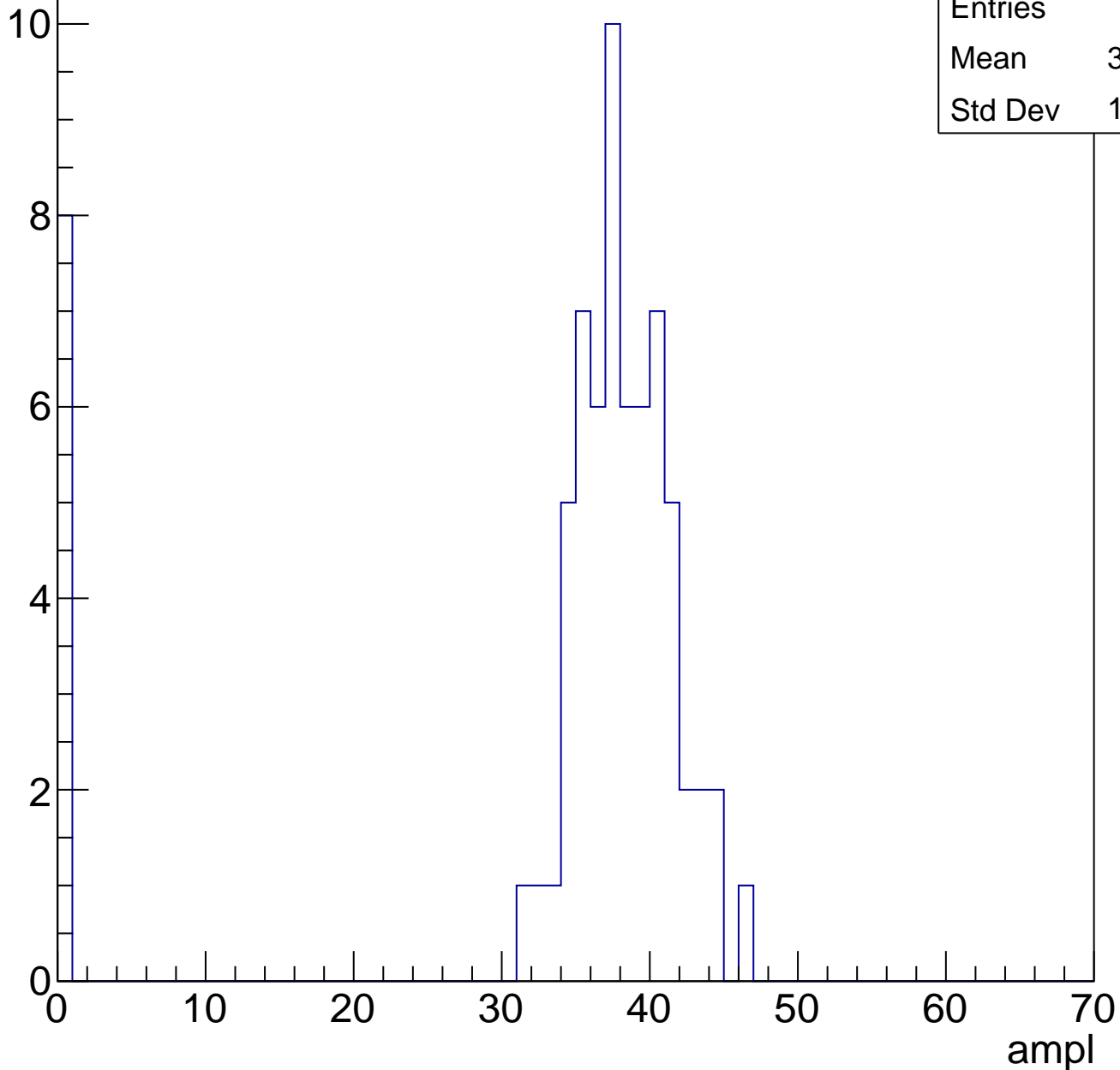
Entries	84
Mean	27.49
Std Dev	9.927

B1L103S, U9-ch21, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	70
Mean	33.54
Std Dev	12.39

Entry

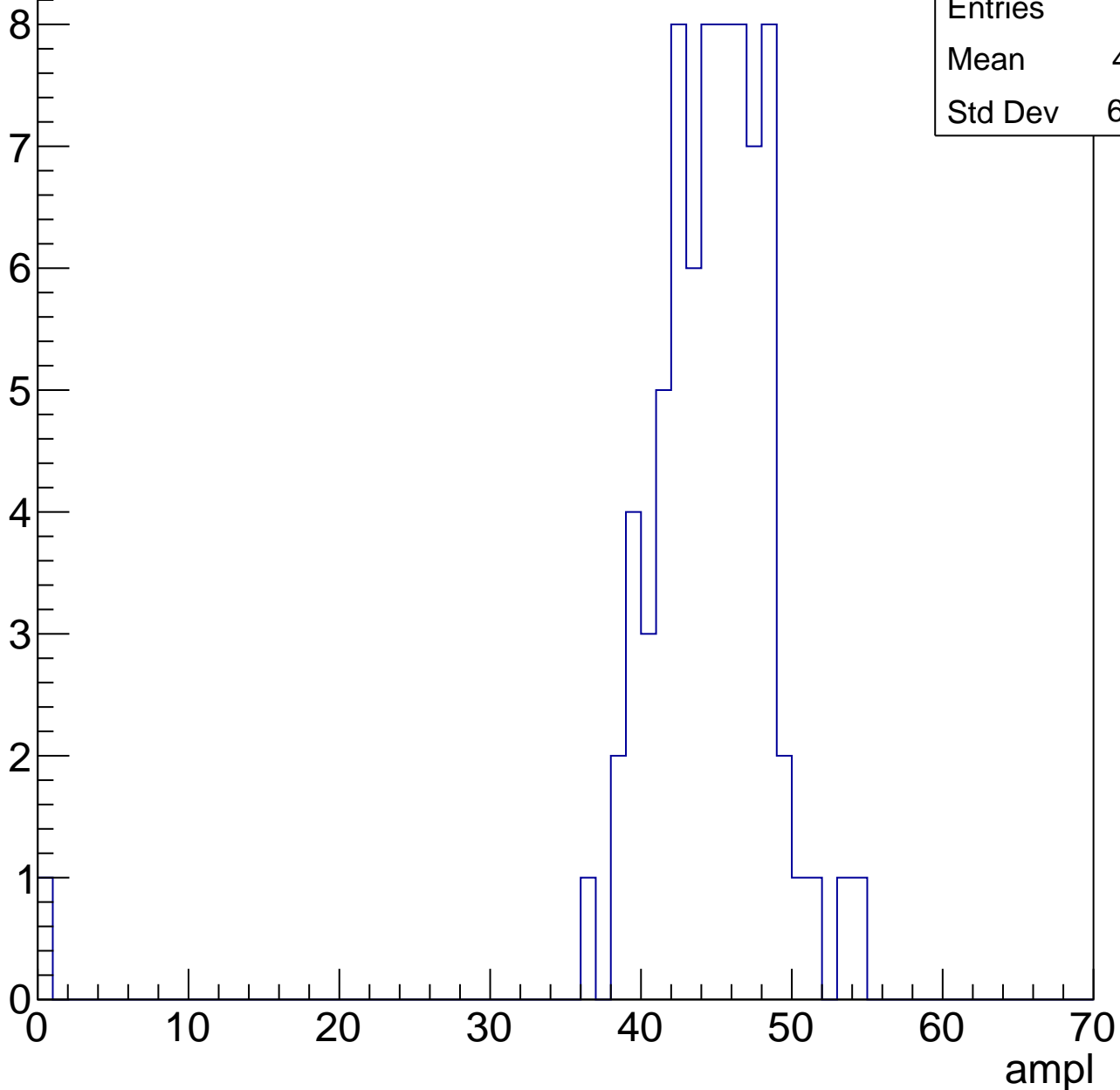


B1L103S, U9-ch21, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	43.81
Std Dev	6.162

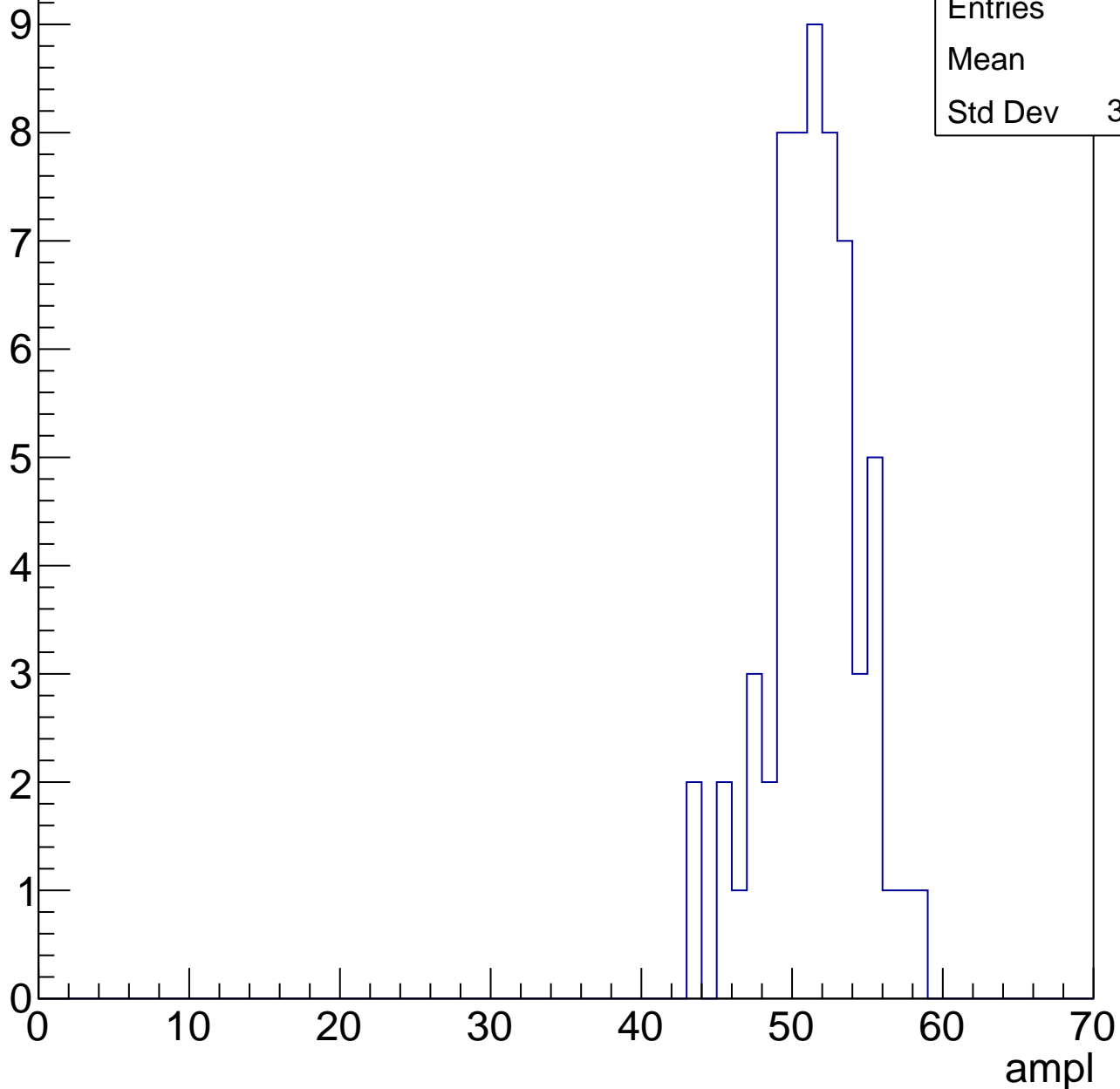


B1L103S, U9-ch21, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	50.9
Std Dev	3.093

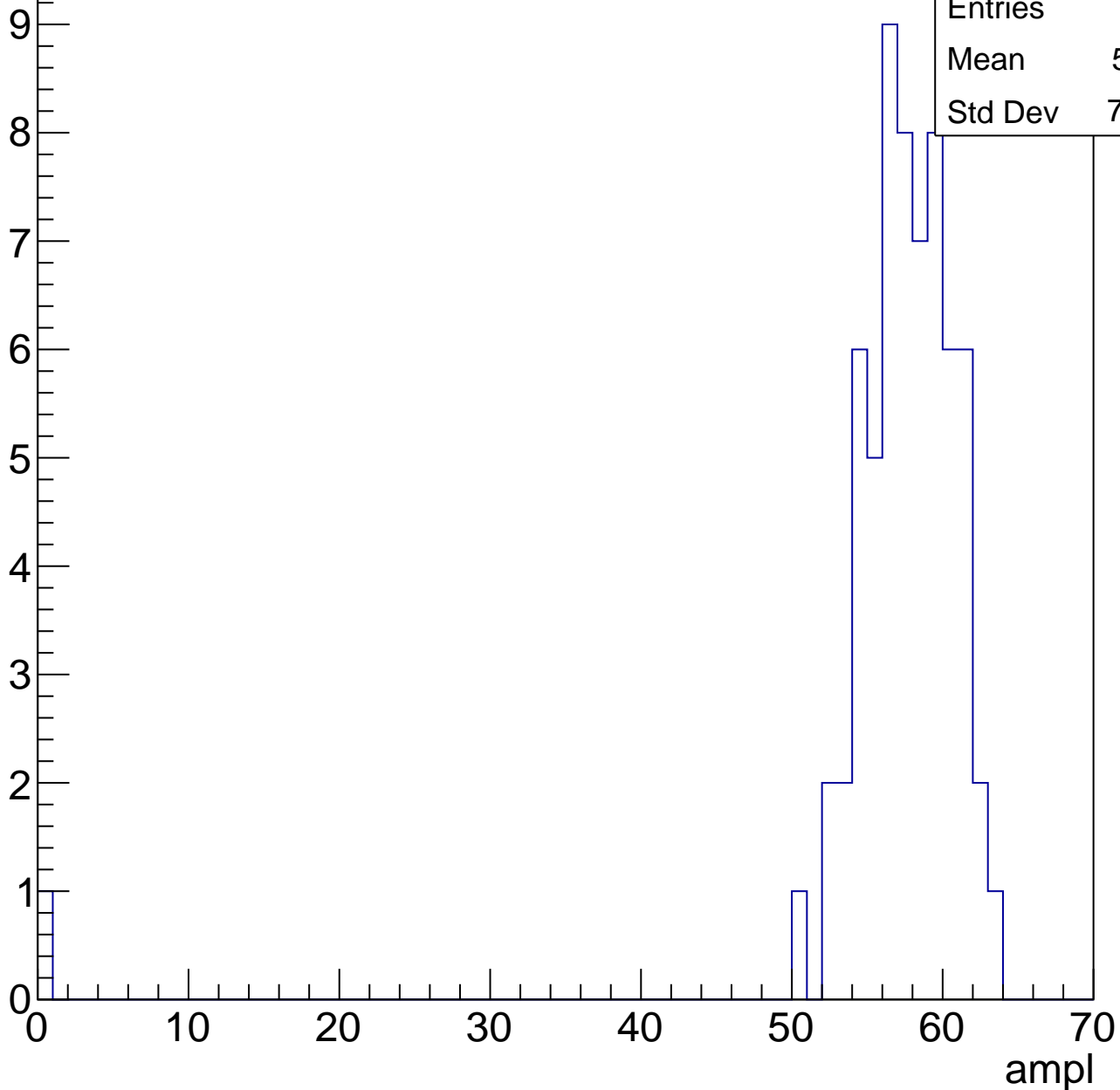


B1L103S, U9-ch21, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	56.41
Std Dev	7.619



B1L103S, U9-ch21, adc5

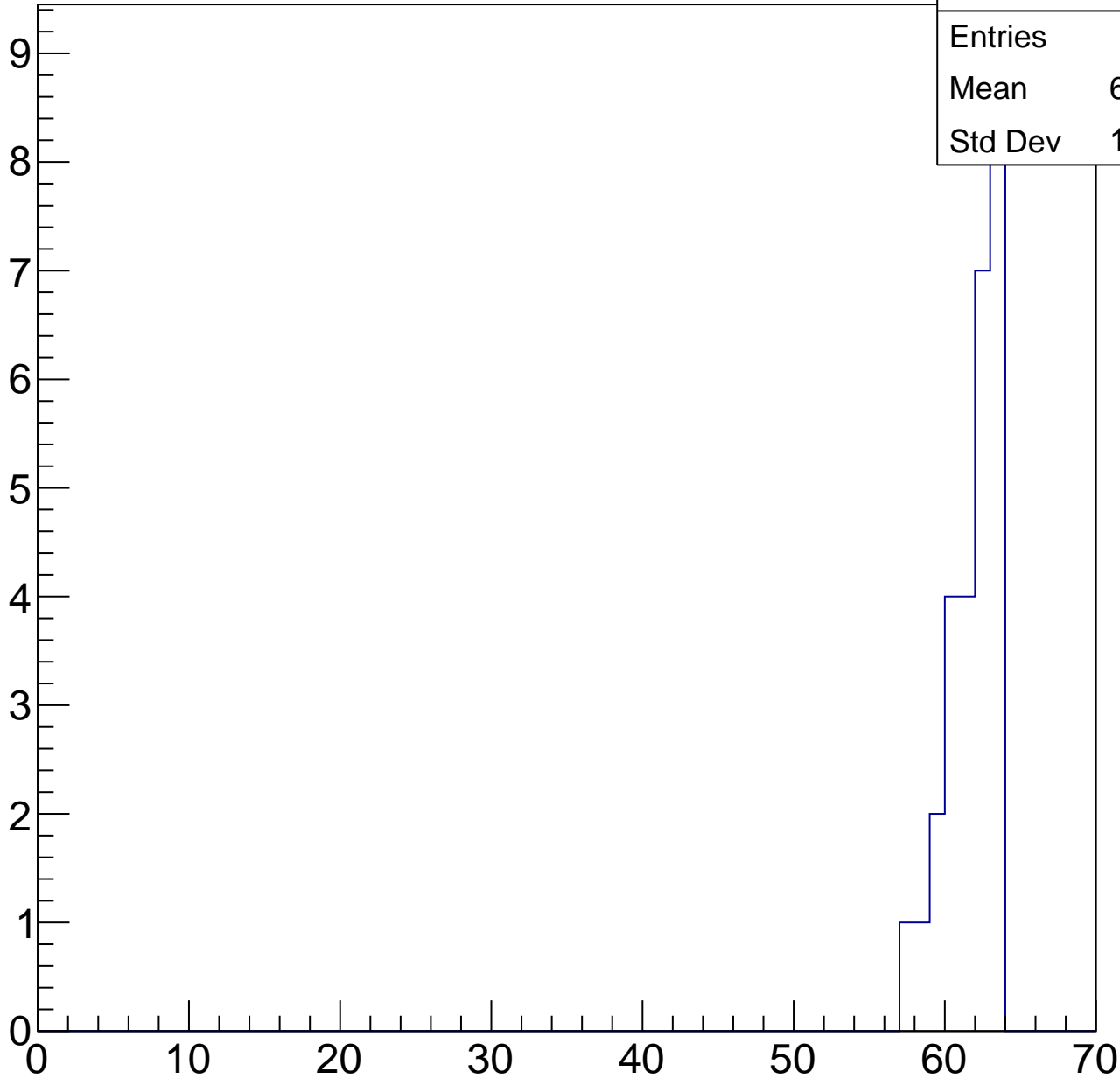
calib_packv5_041523_1651.root, FC#0, port C2

Entry

9
8
7
6
5
4
3
2
1
0

Entries	28
Mean	61.36
Std Dev	1.652

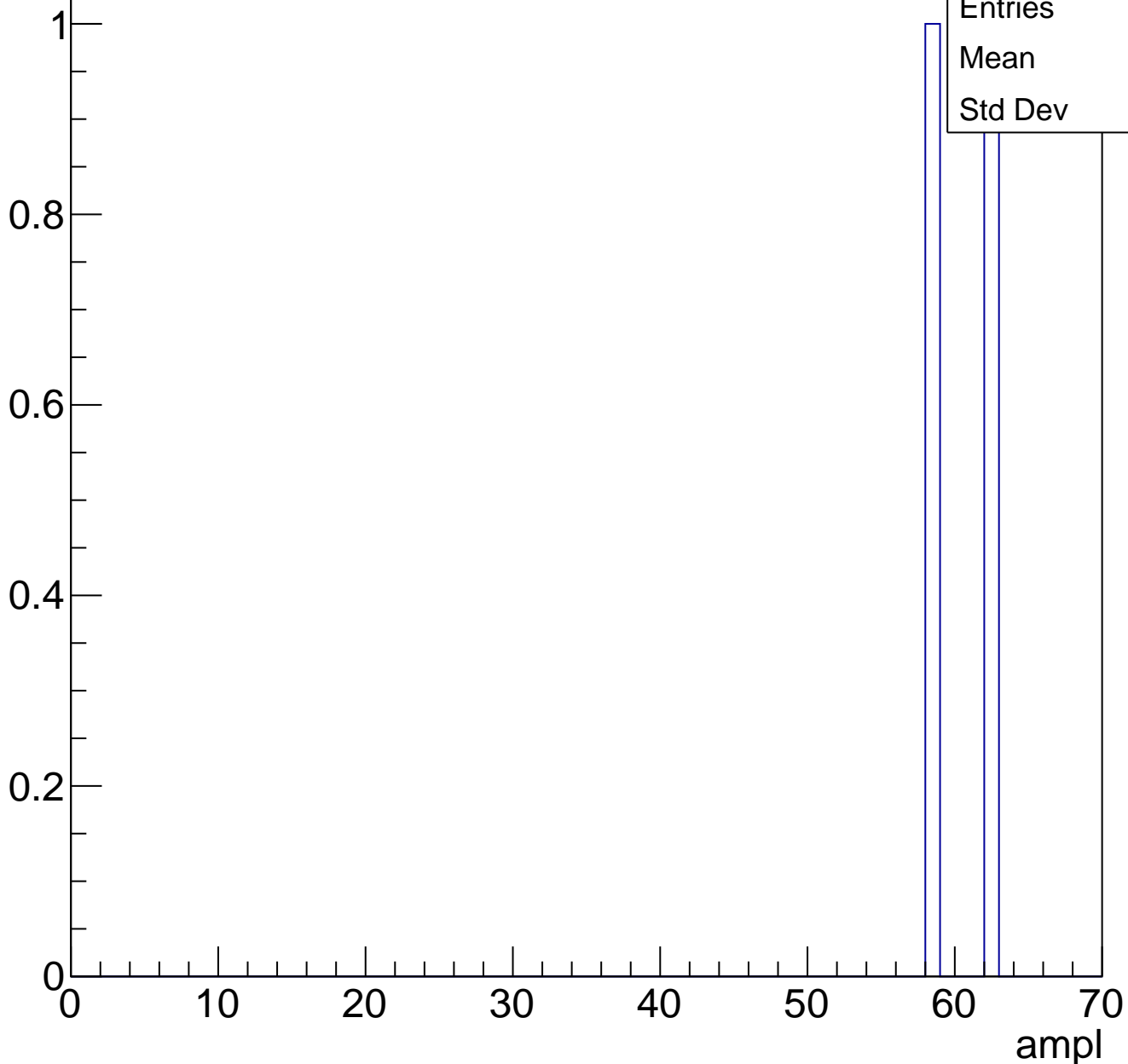
ampl



B1L103S, U9-ch21, adc6

calib_packv5_041523_1651.root, FC#0, port C2

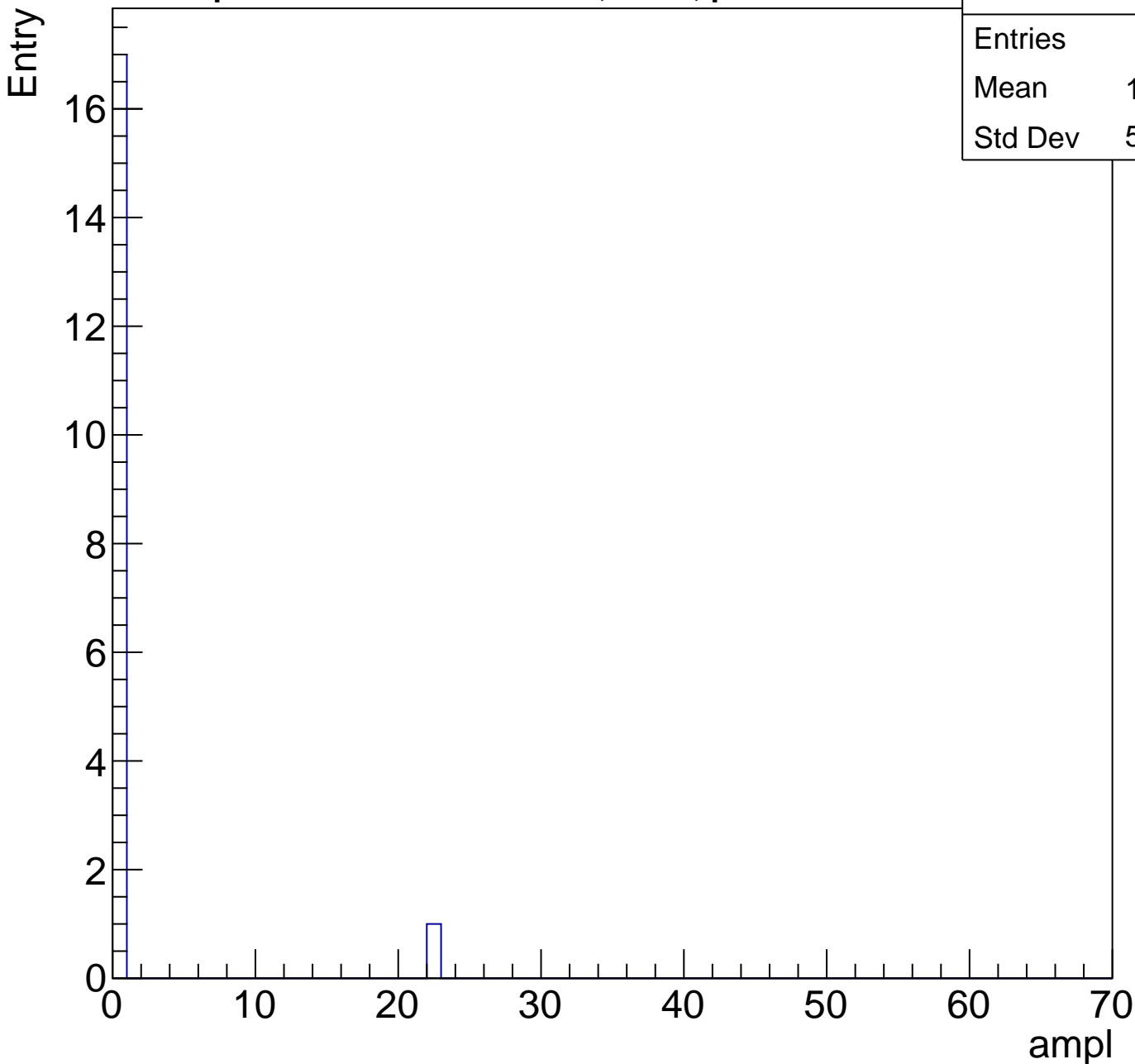
Entry



B1L103S, U9-ch21, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	18
Mean	1.222
Std Dev	5.039

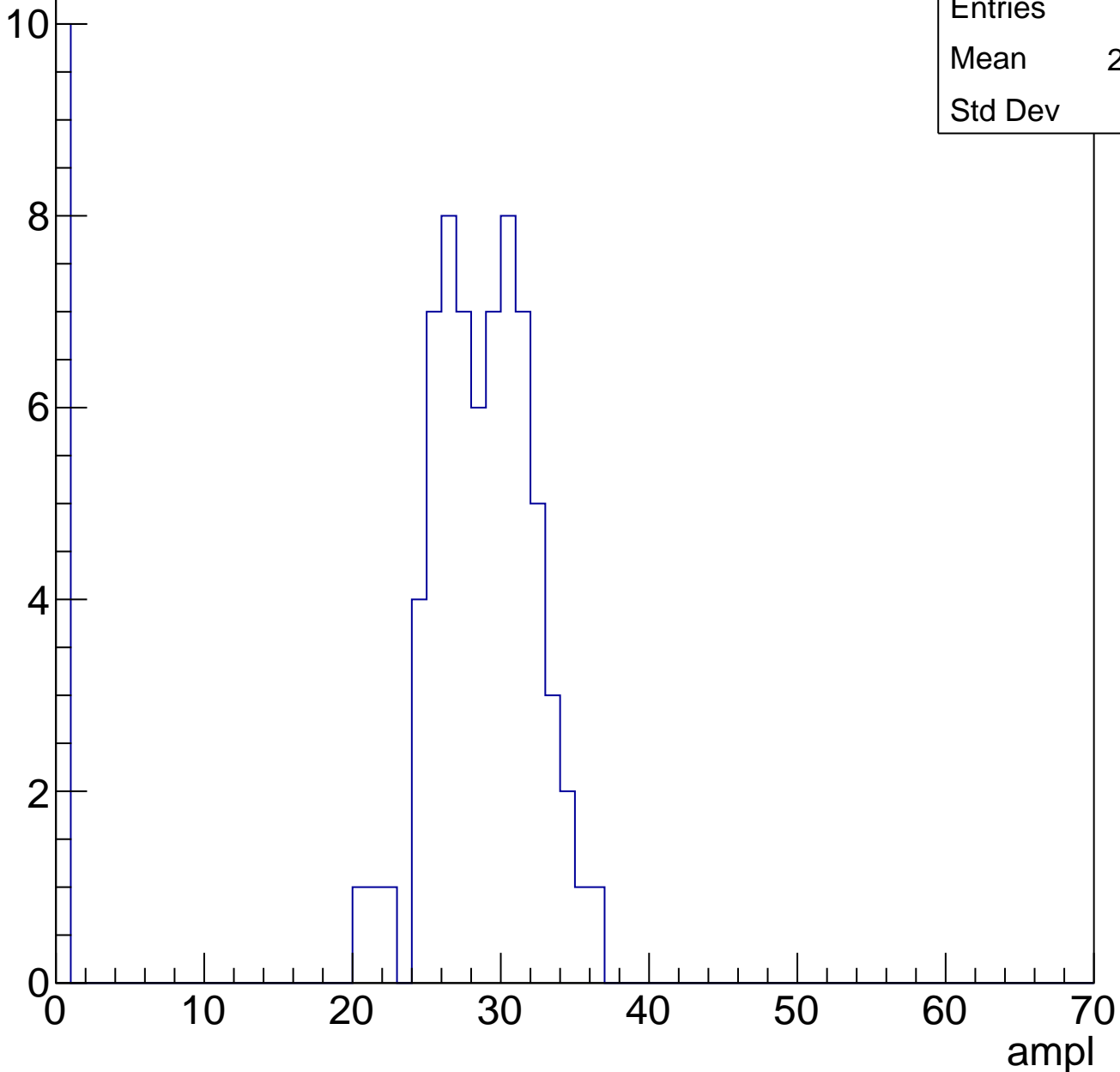


B1L103S, U9-ch22, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	79
Mean	24.77
Std Dev	9.92

Entry



B1L103S, U9-ch22, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

8

6

4

2

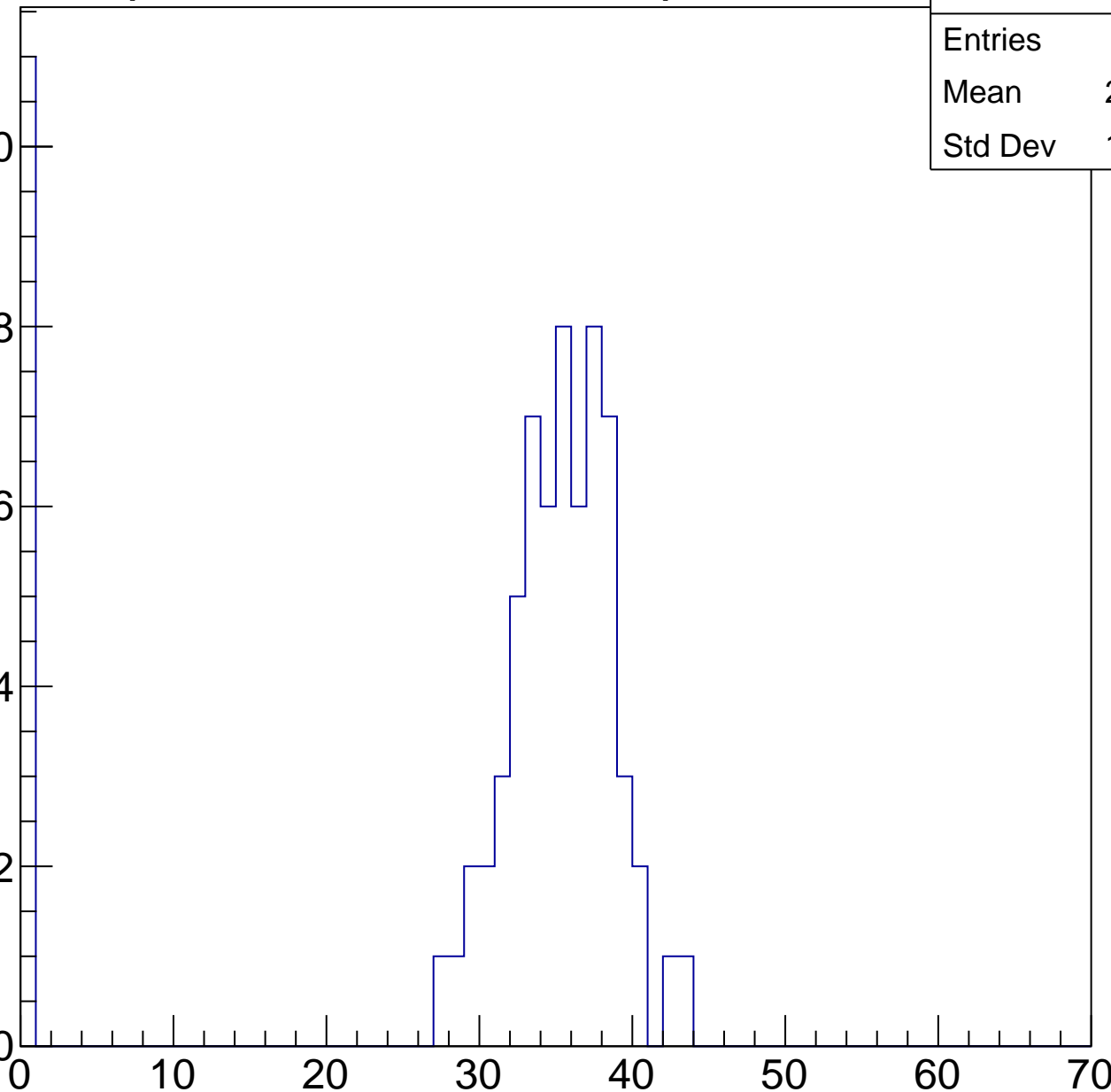
0

Entries 74

Mean 29.74

Std Dev 12.79

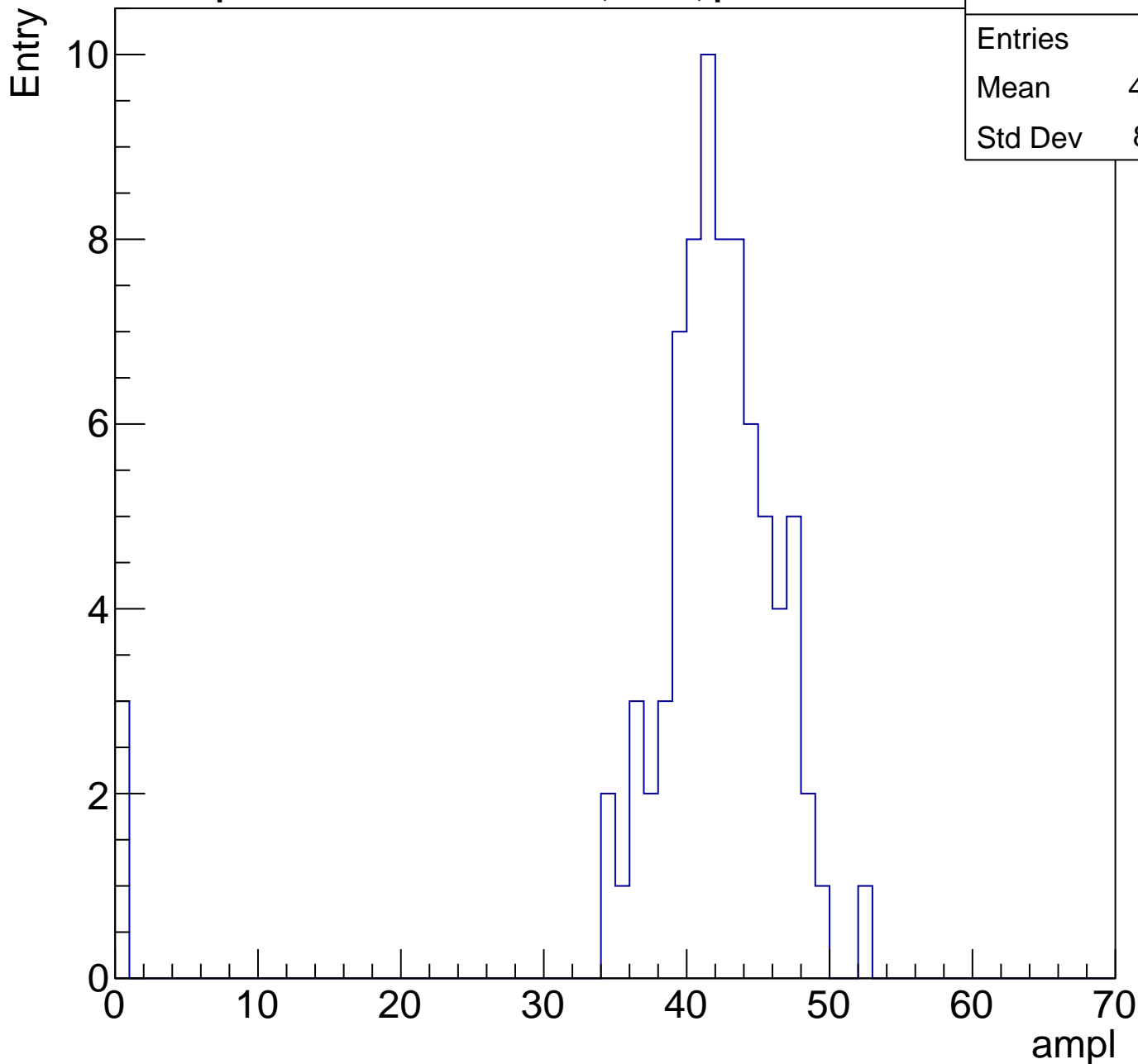
ampl



B1L103S, U9-ch22, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	79
Mean	40.34
Std Dev	8.751

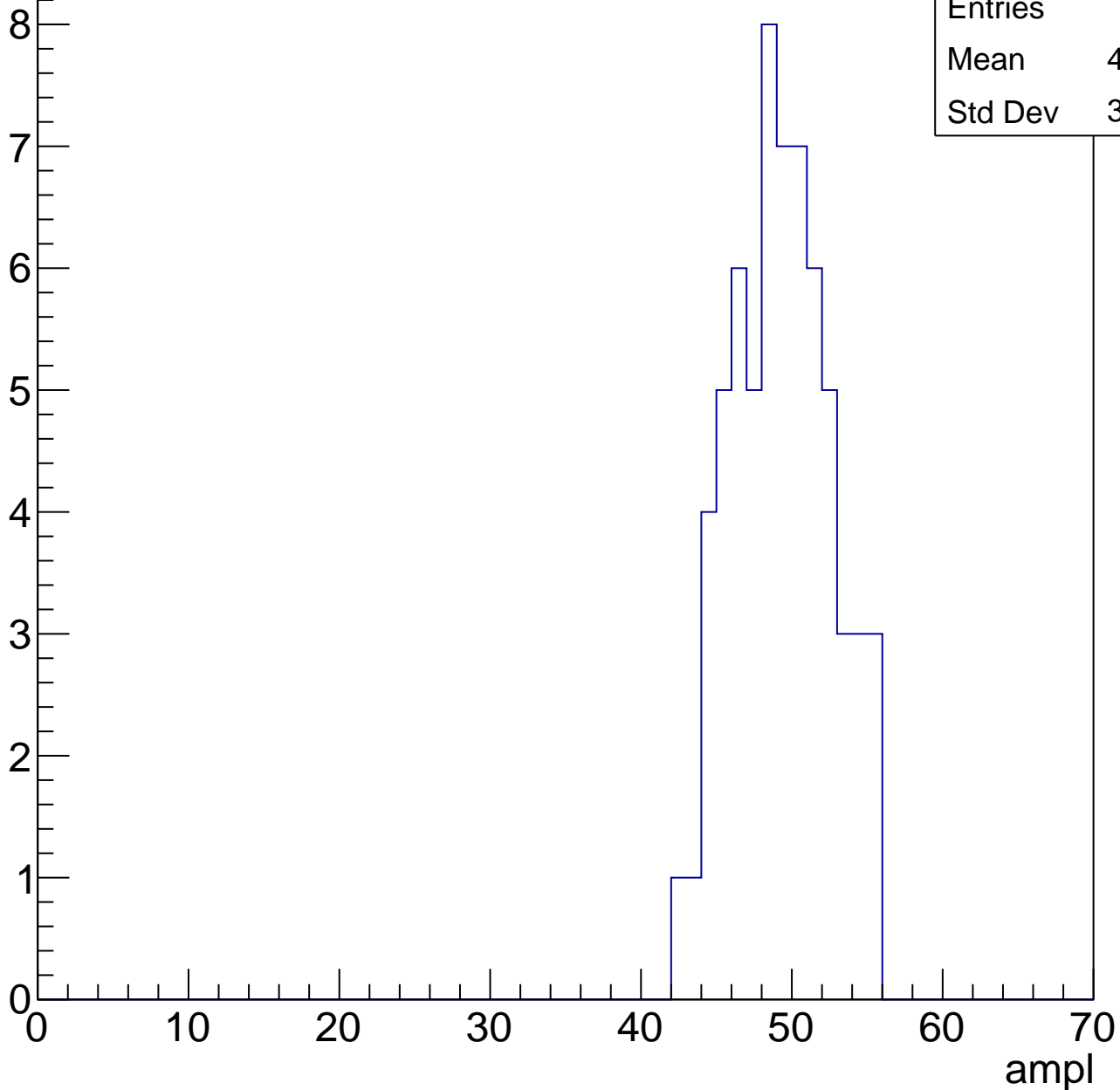


B1L103S, U9-ch22, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	48.84
Std Dev	3.193

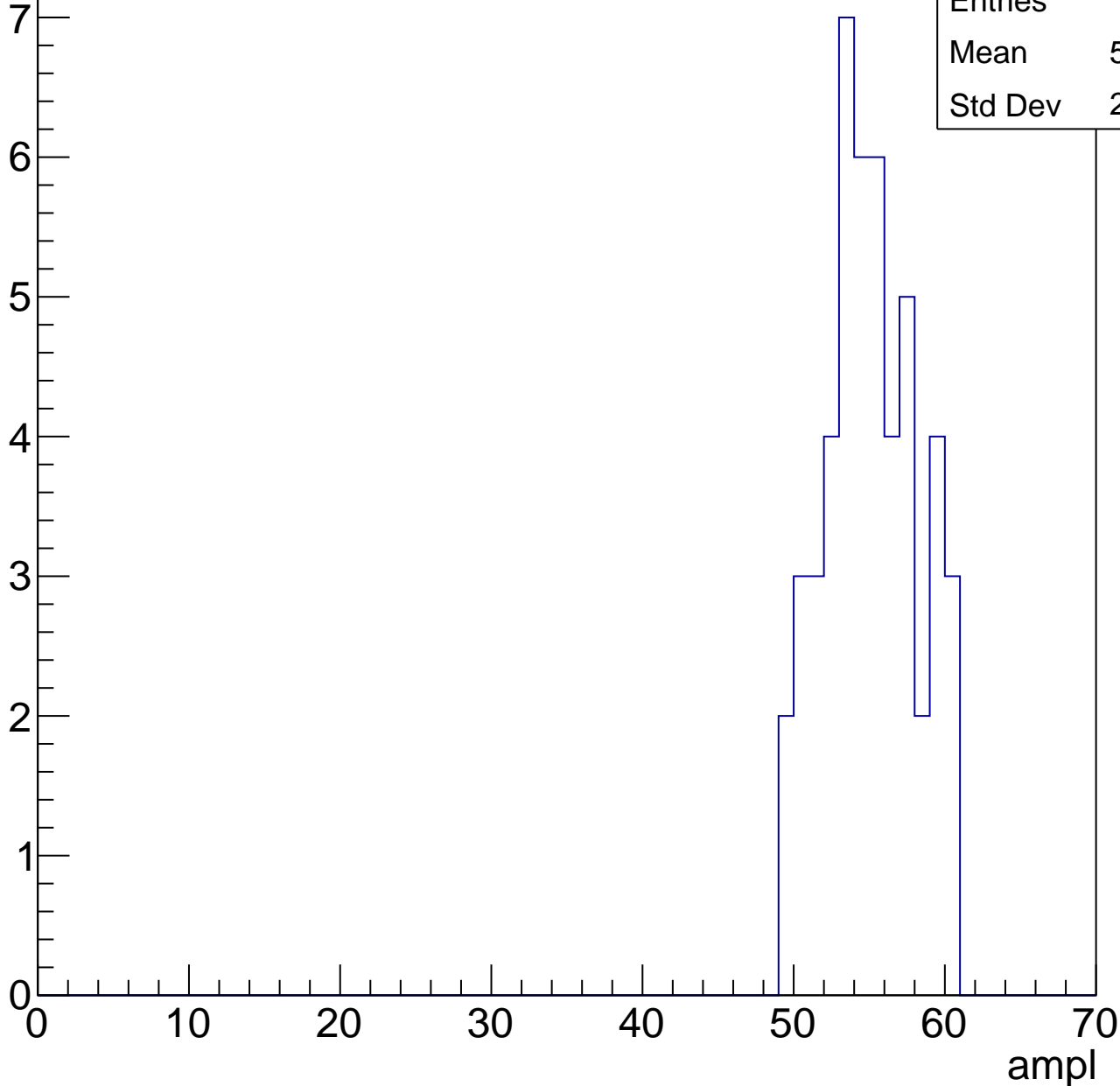


B1L103S, U9-ch22, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	54.59
Std Dev	2.989

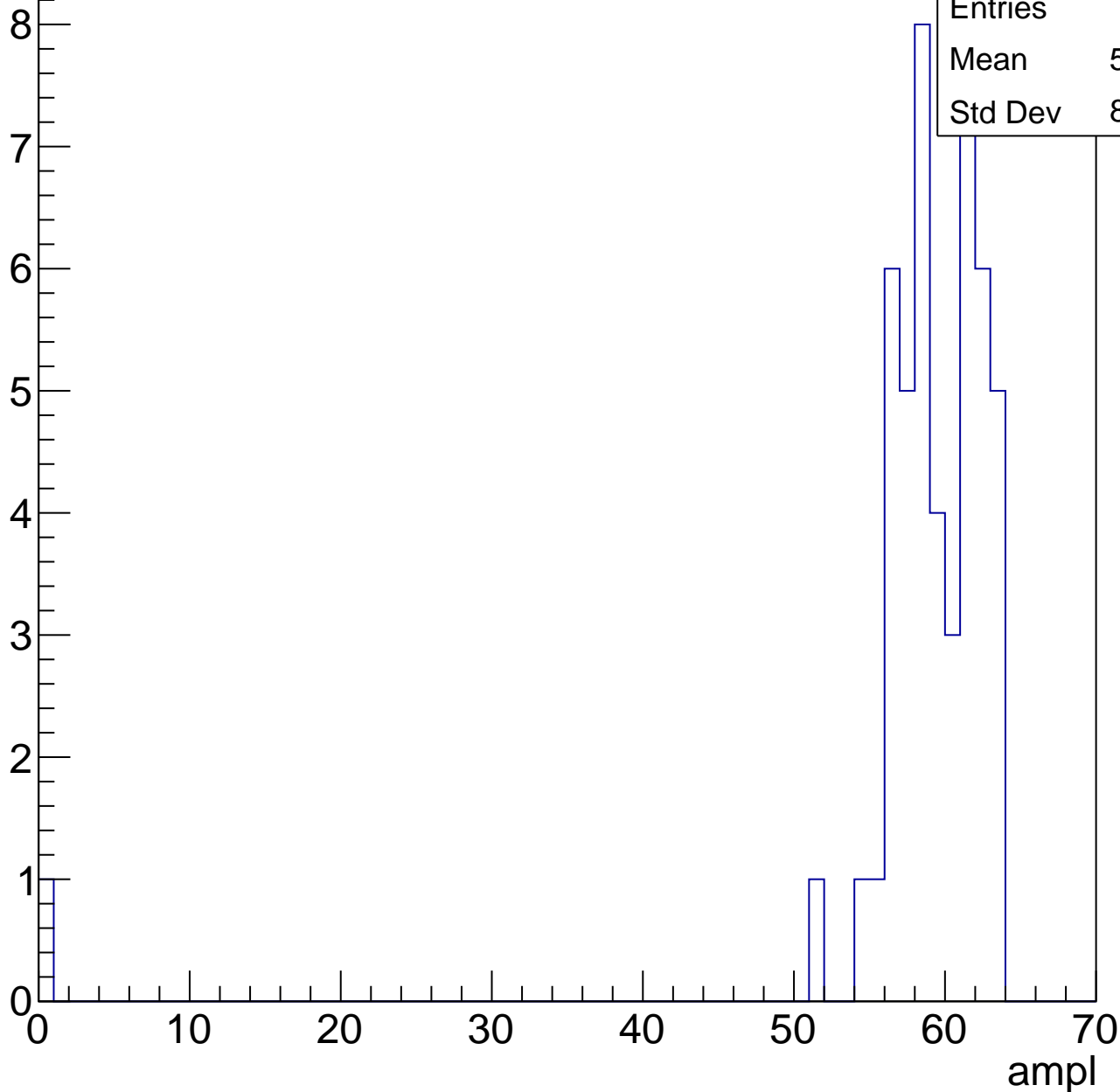


B1L103S, U9-ch22, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

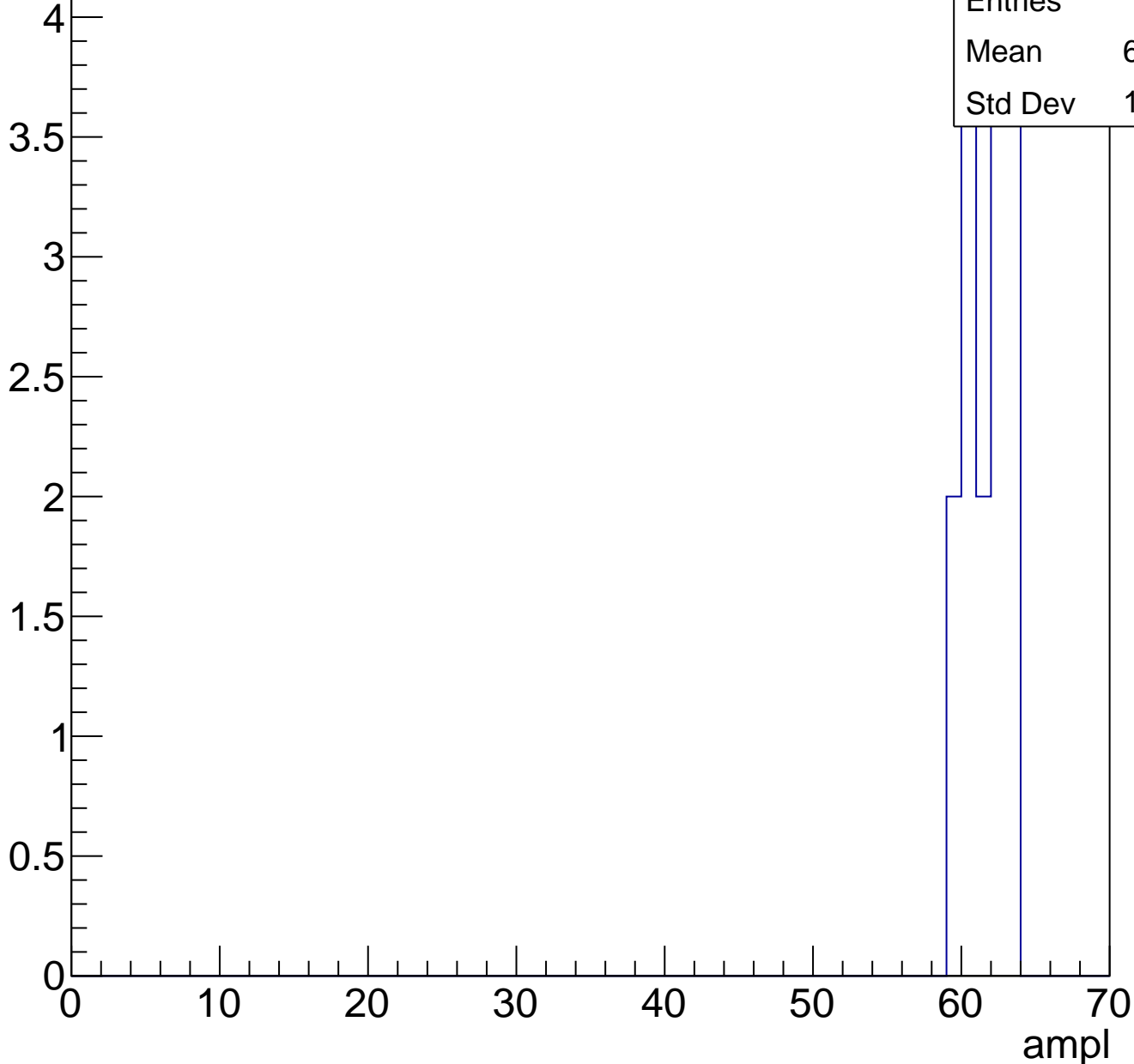
Entries	49
Mean	57.88
Std Dev	8.778



B1L103S, U9-ch22, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch22, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	3.316
Std Dev	14.07

Entry

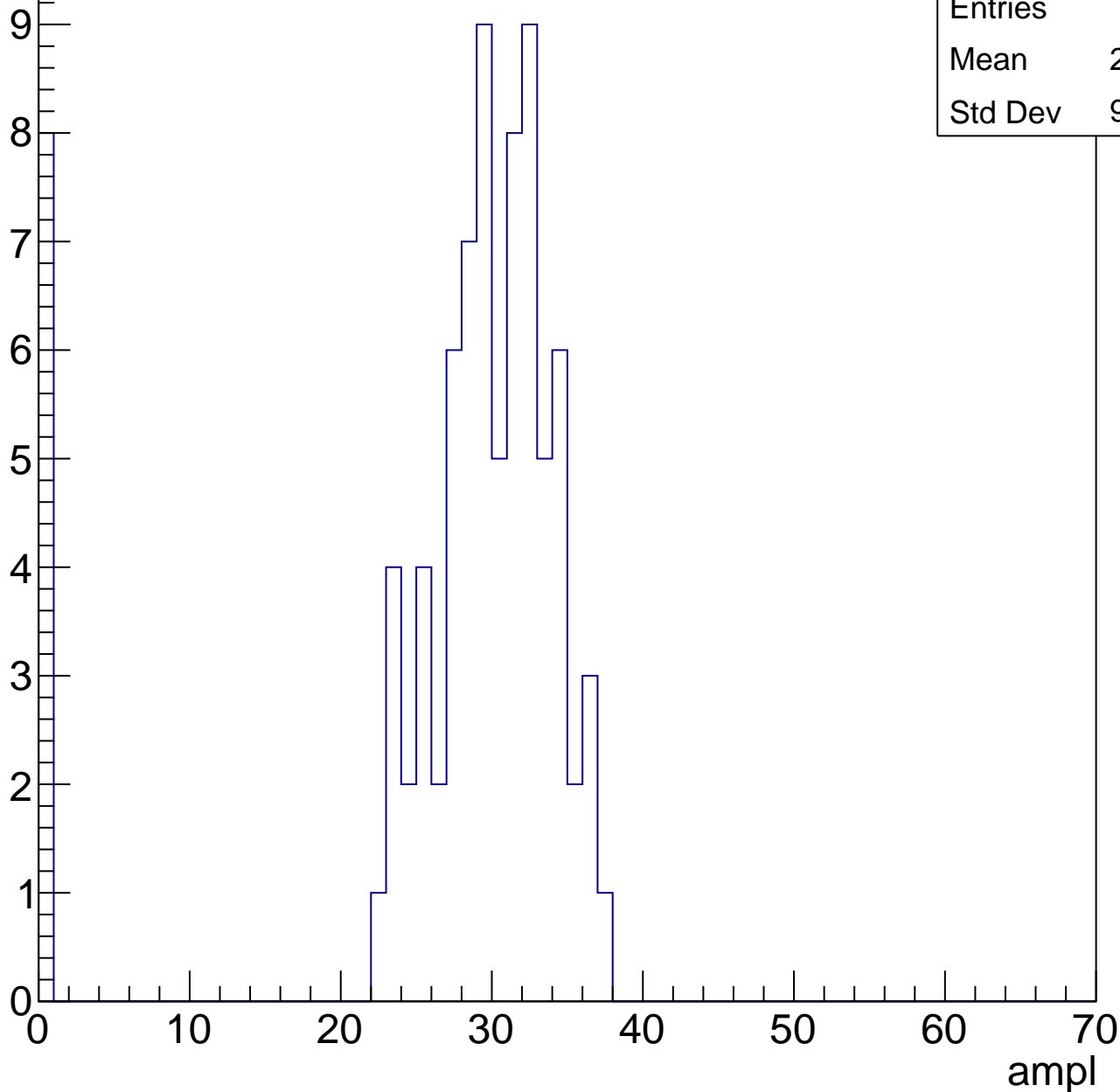


B1L103S, U9-ch23, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	82
Mean	26.87
Std Dev	9.462

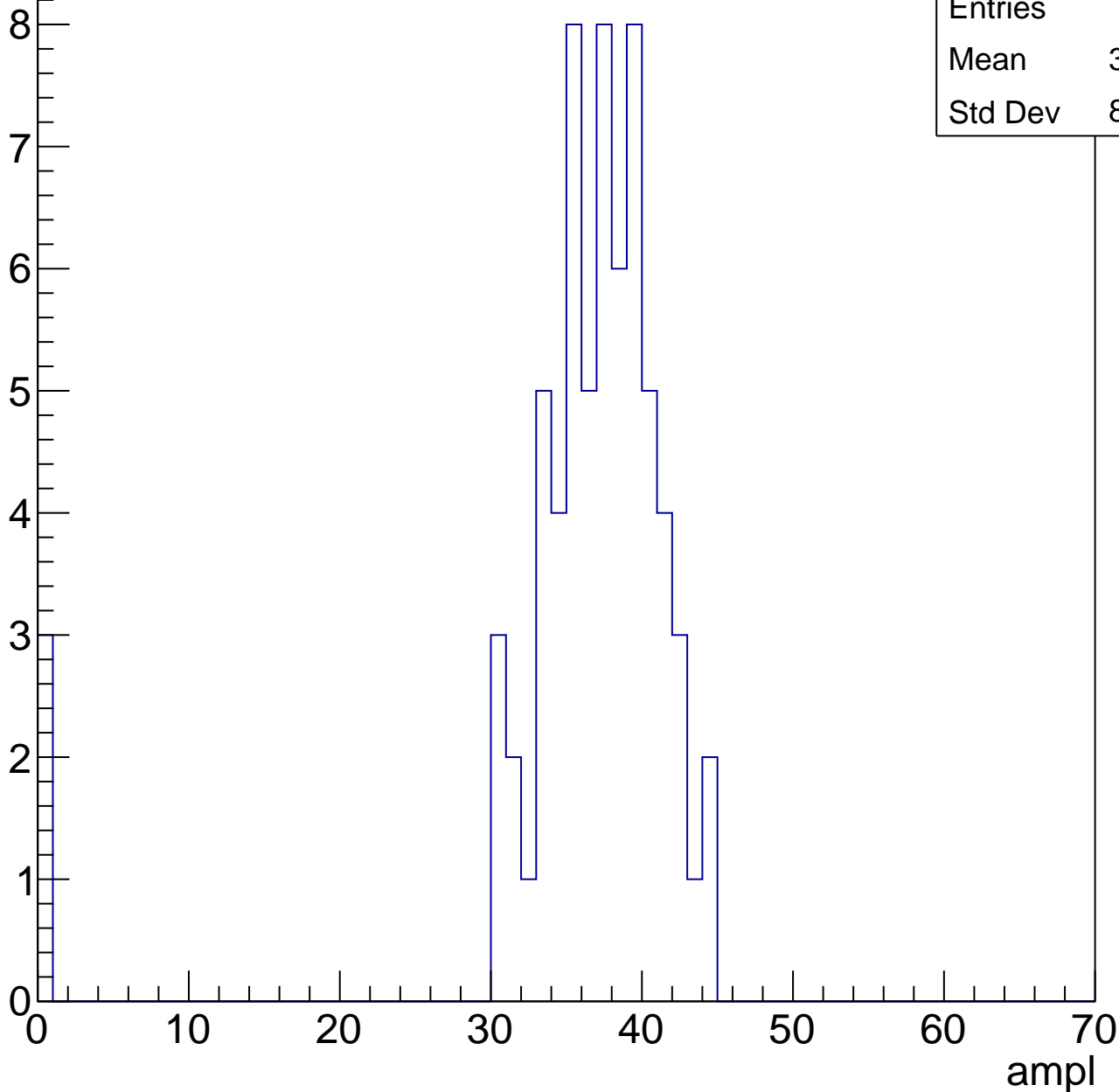


B1L103S, U9-ch23, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	35.32
Std Dev	8.286

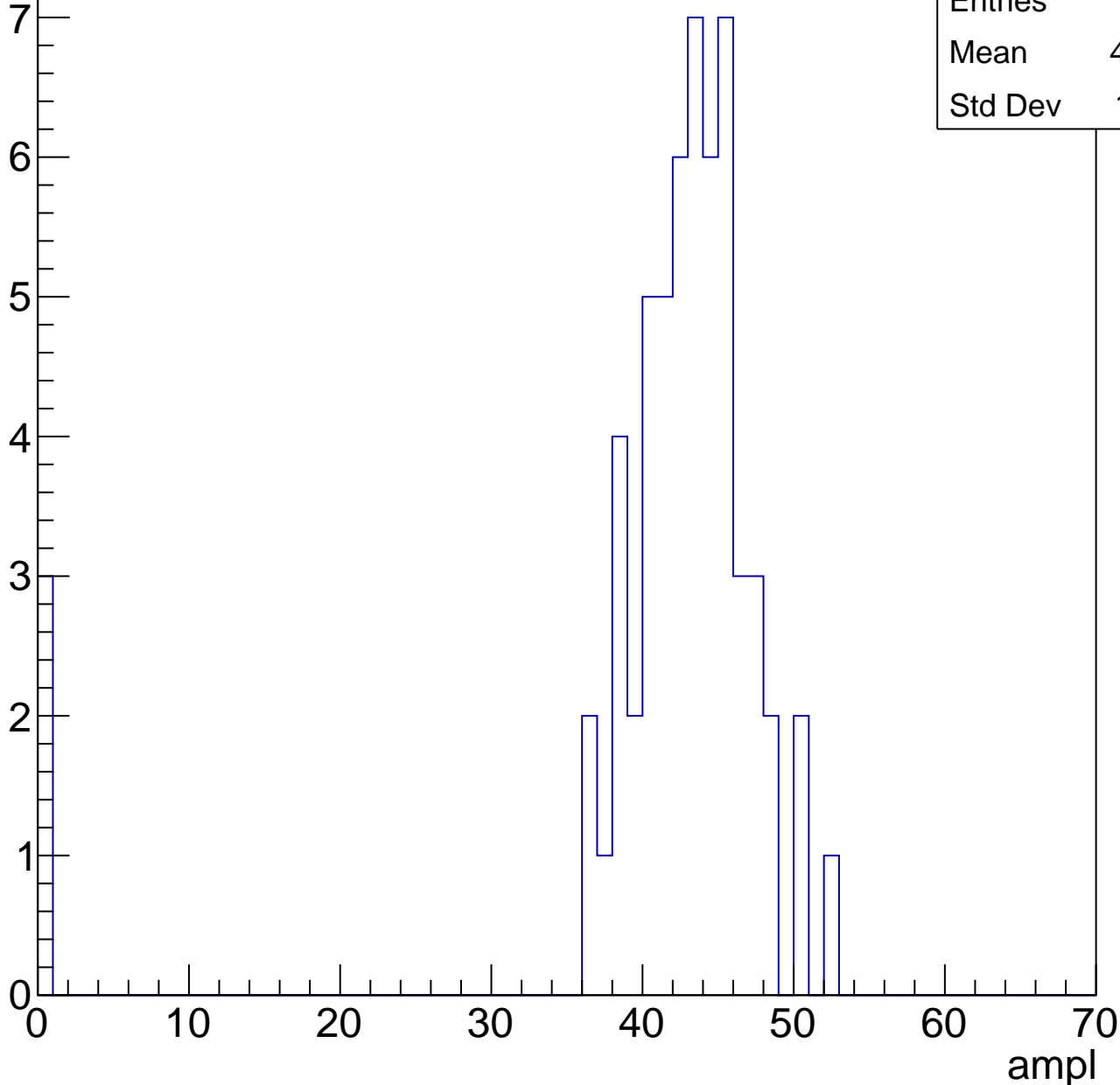


B1L103S, U9-ch23, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	40.73
Std Dev	10.01

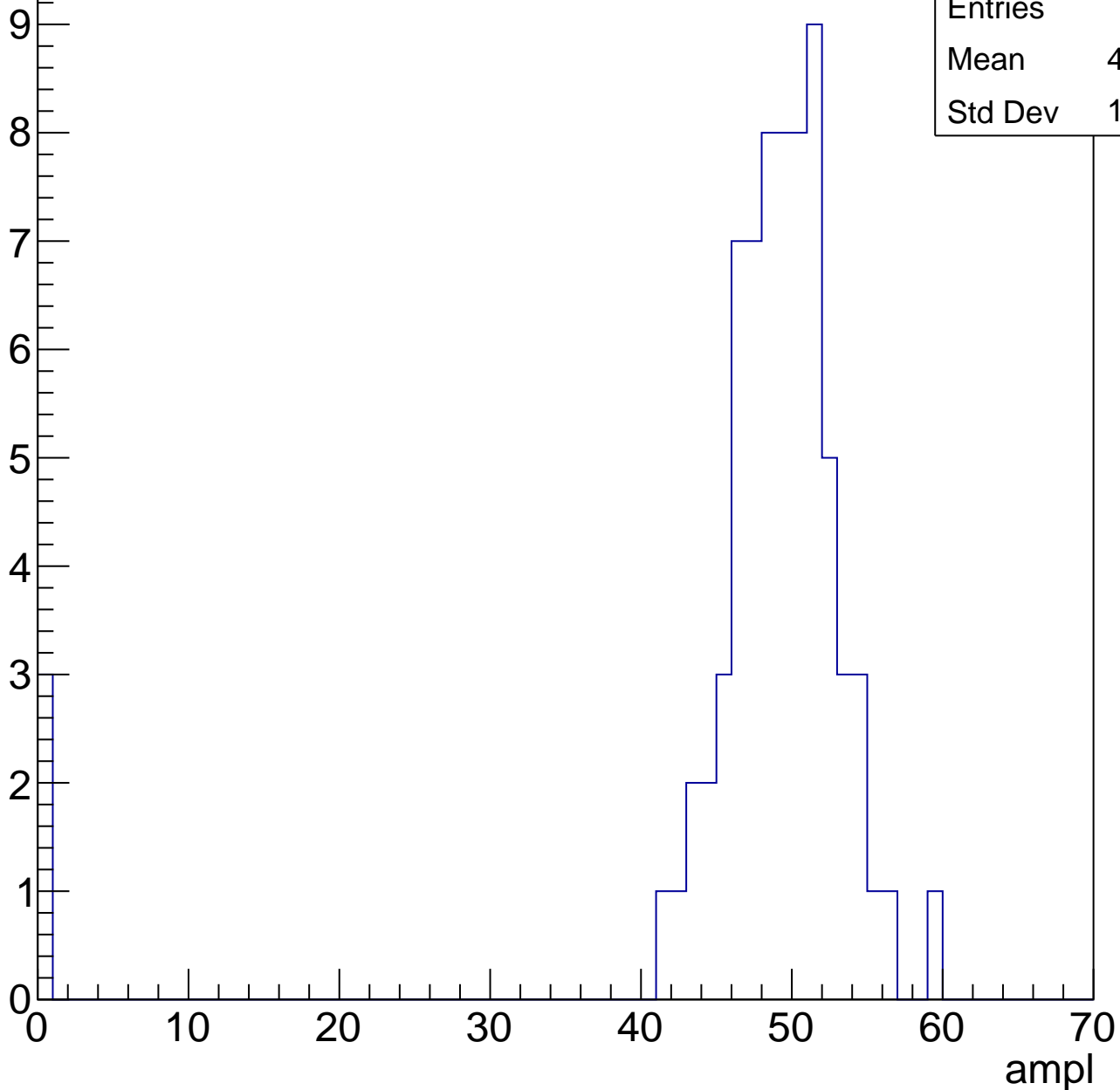


B1L103S, U9-ch23, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	46.97
Std Dev	10.26

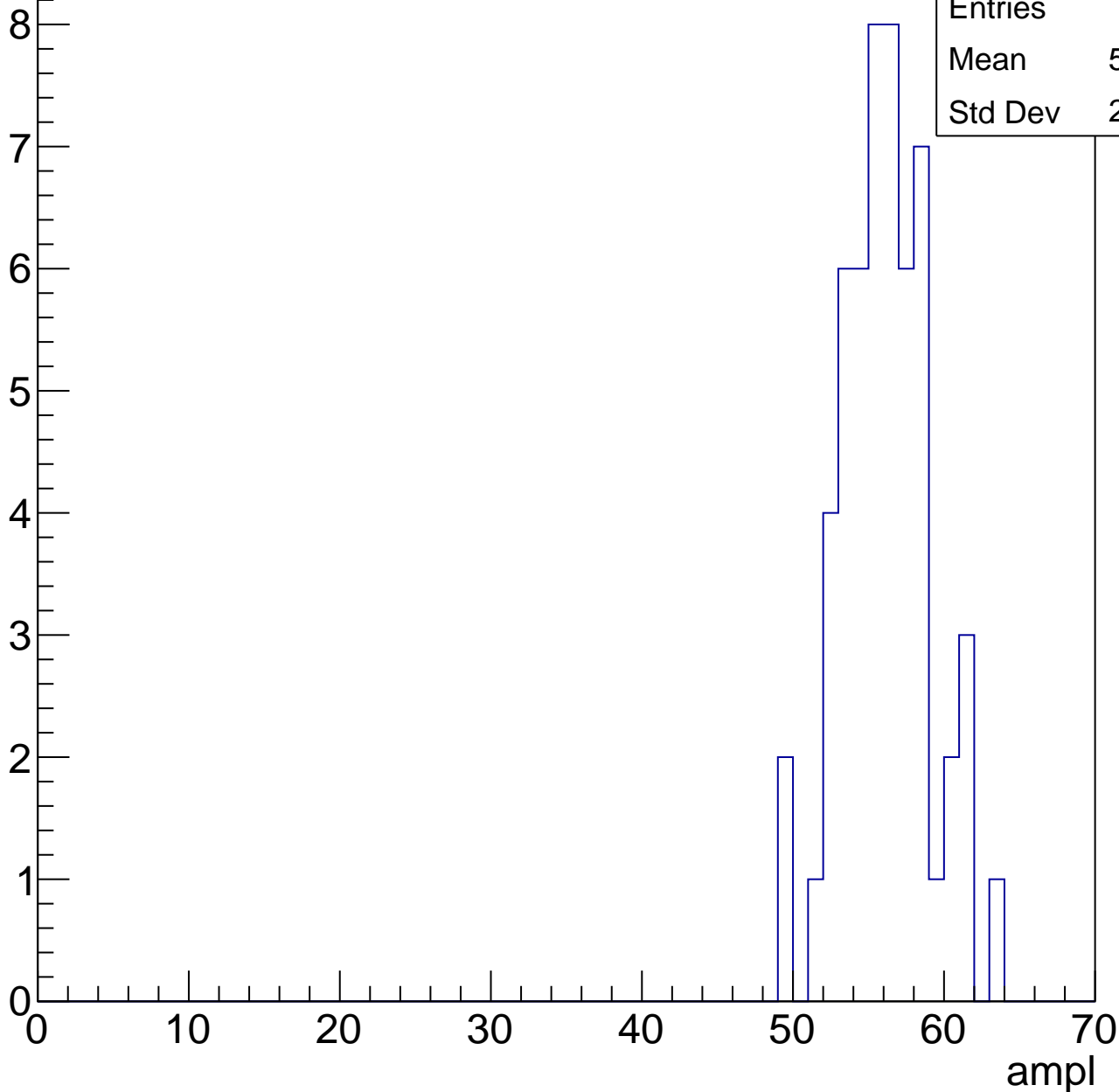


B1L103S, U9-ch23, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	55.64
Std Dev	2.907

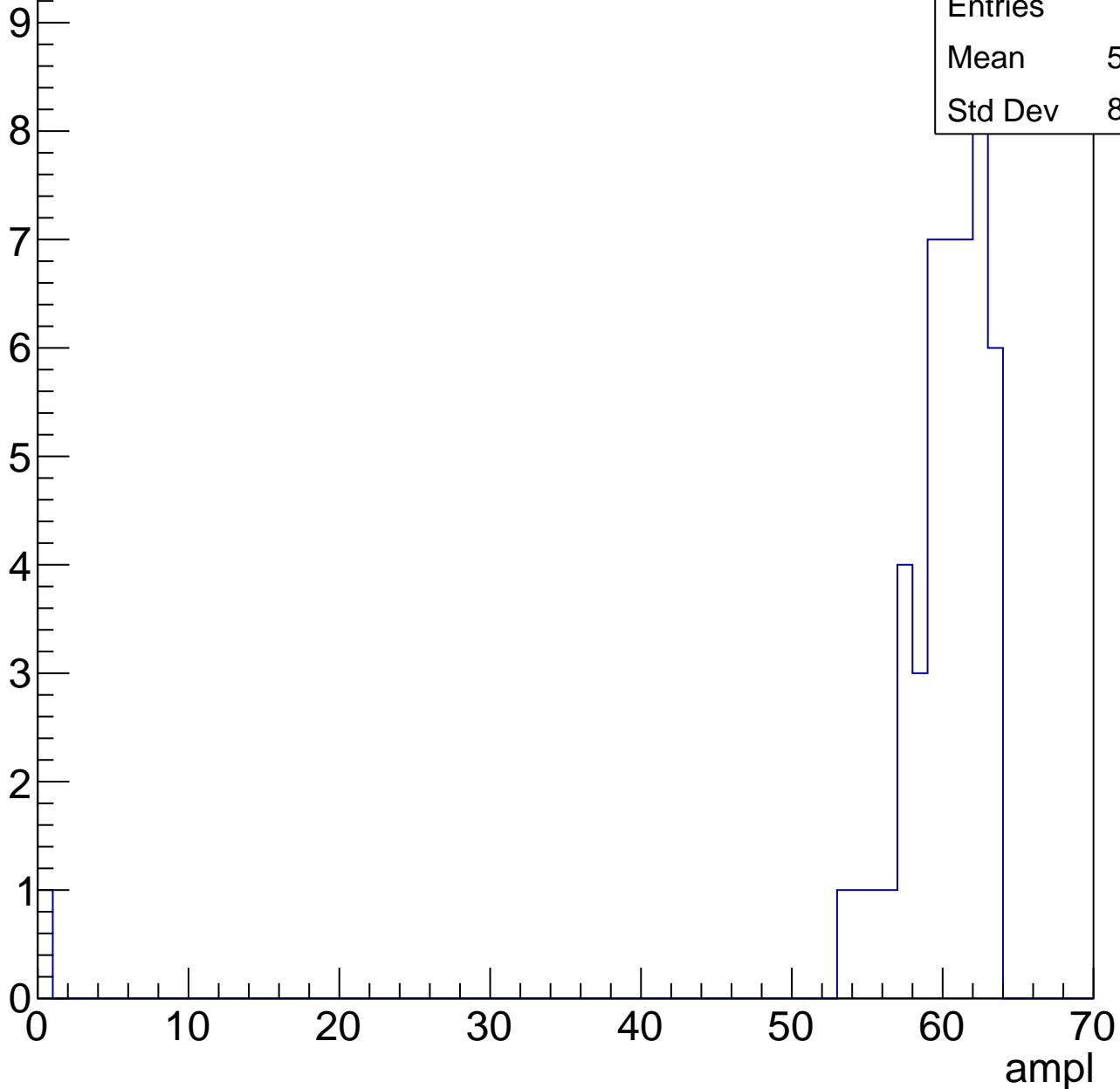


B1L103S, U9-ch23, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

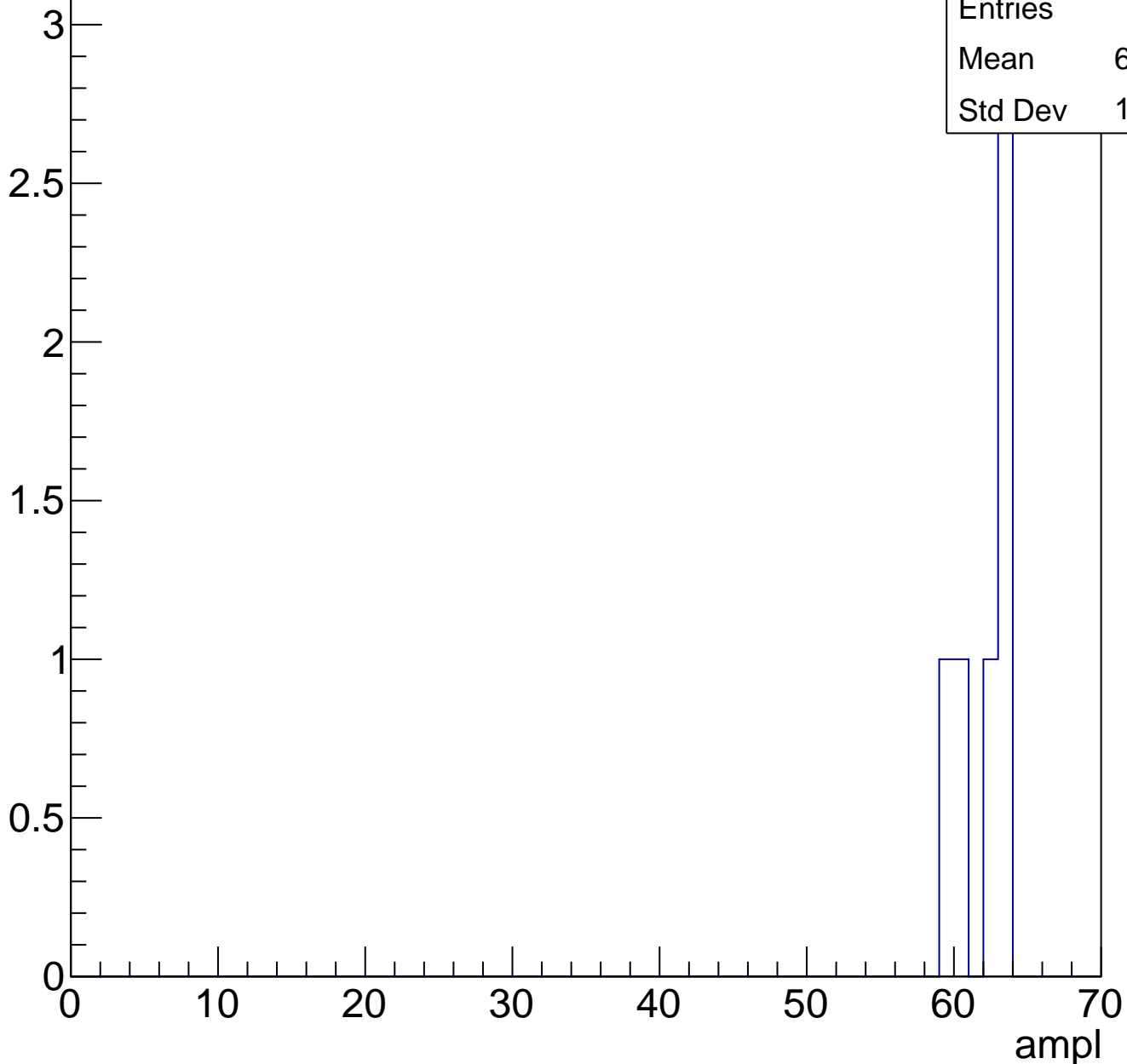
Entries	48
Mean	58.67
Std Dev	8.889



B1L103S, U9-ch23, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

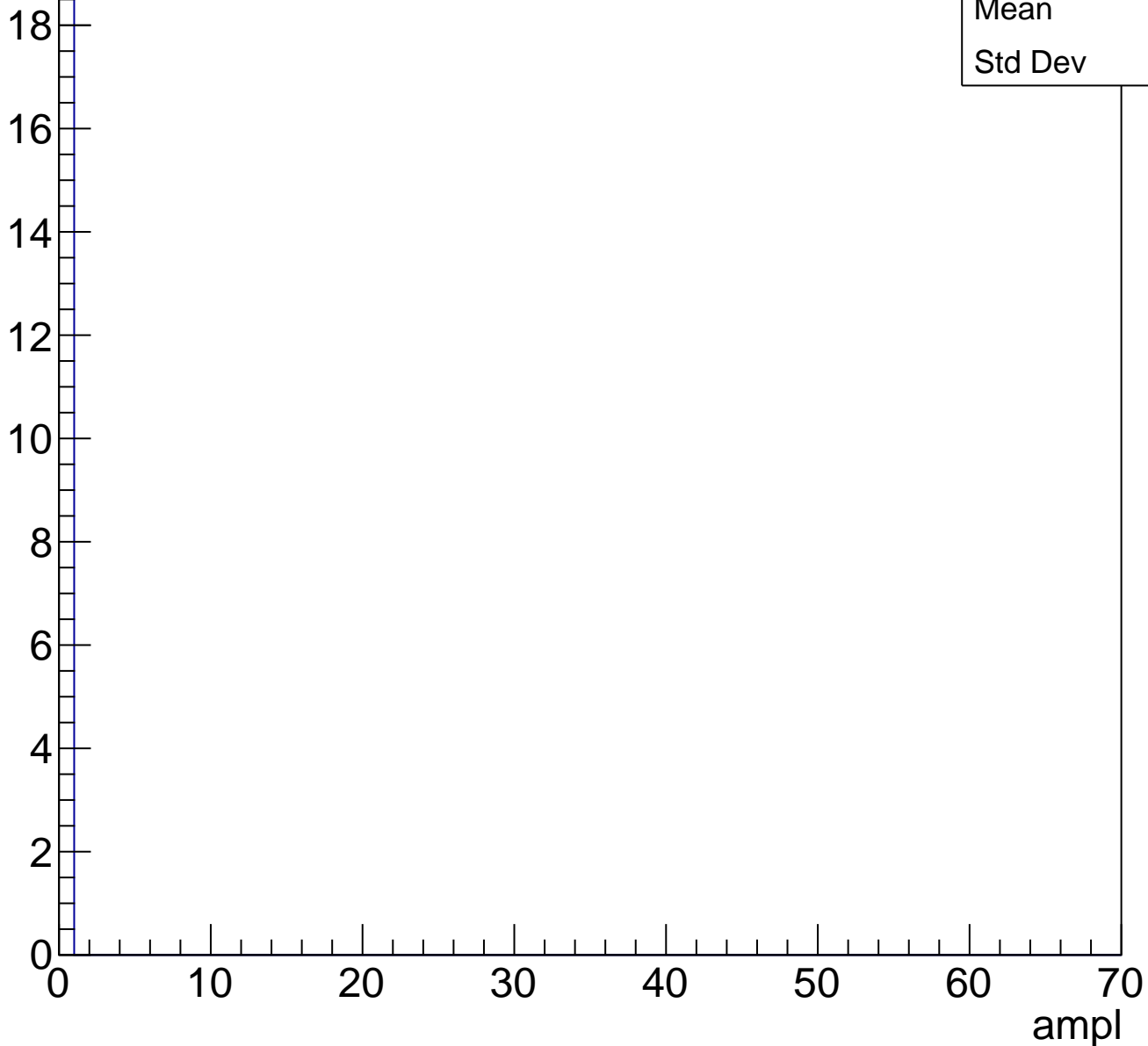


B1L103S, U9-ch23, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	0
Std Dev	0

Entry

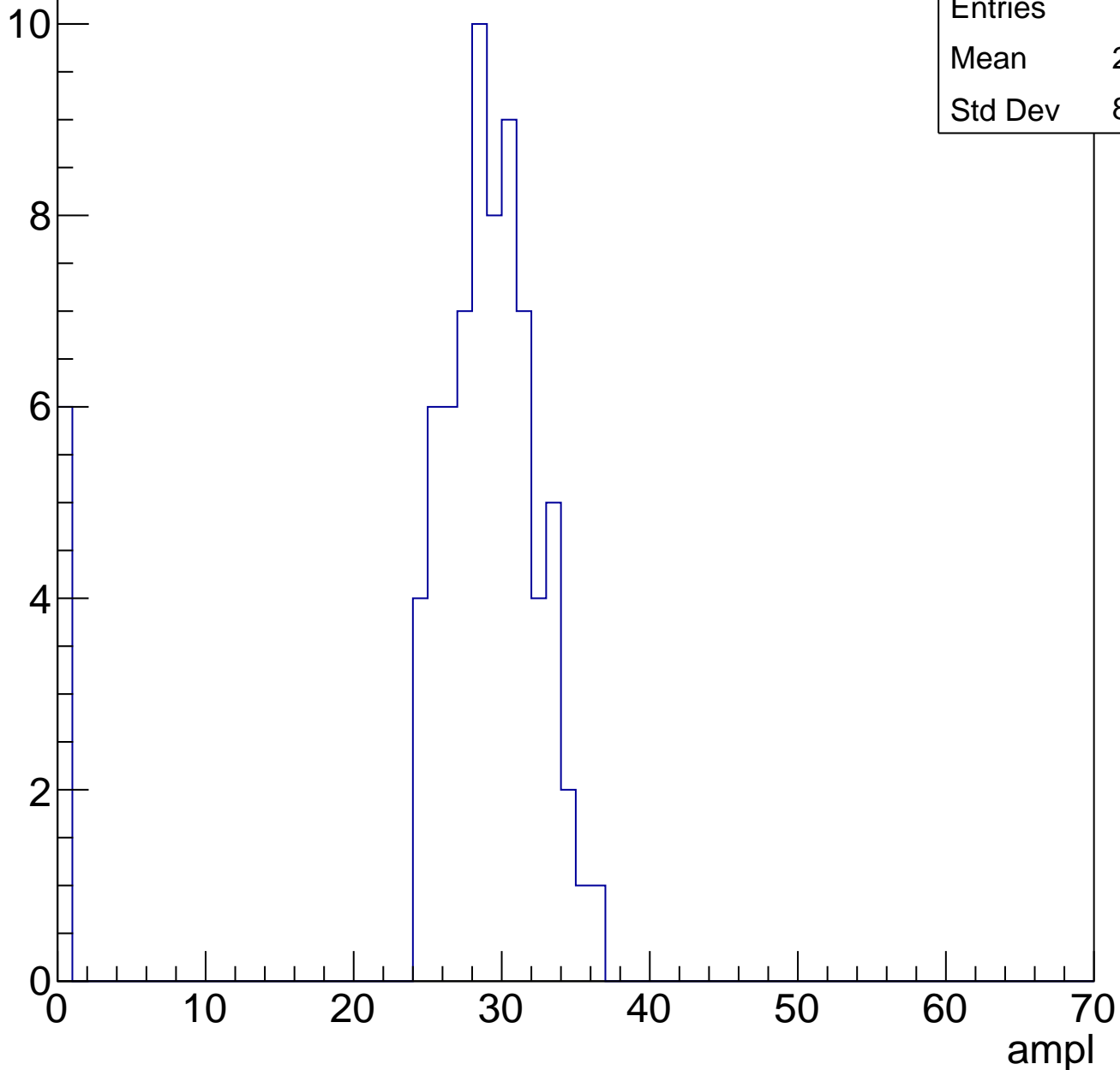


B1L103S, U9-ch24, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	76
Mean	26.61
Std Dev	8.261

Entry

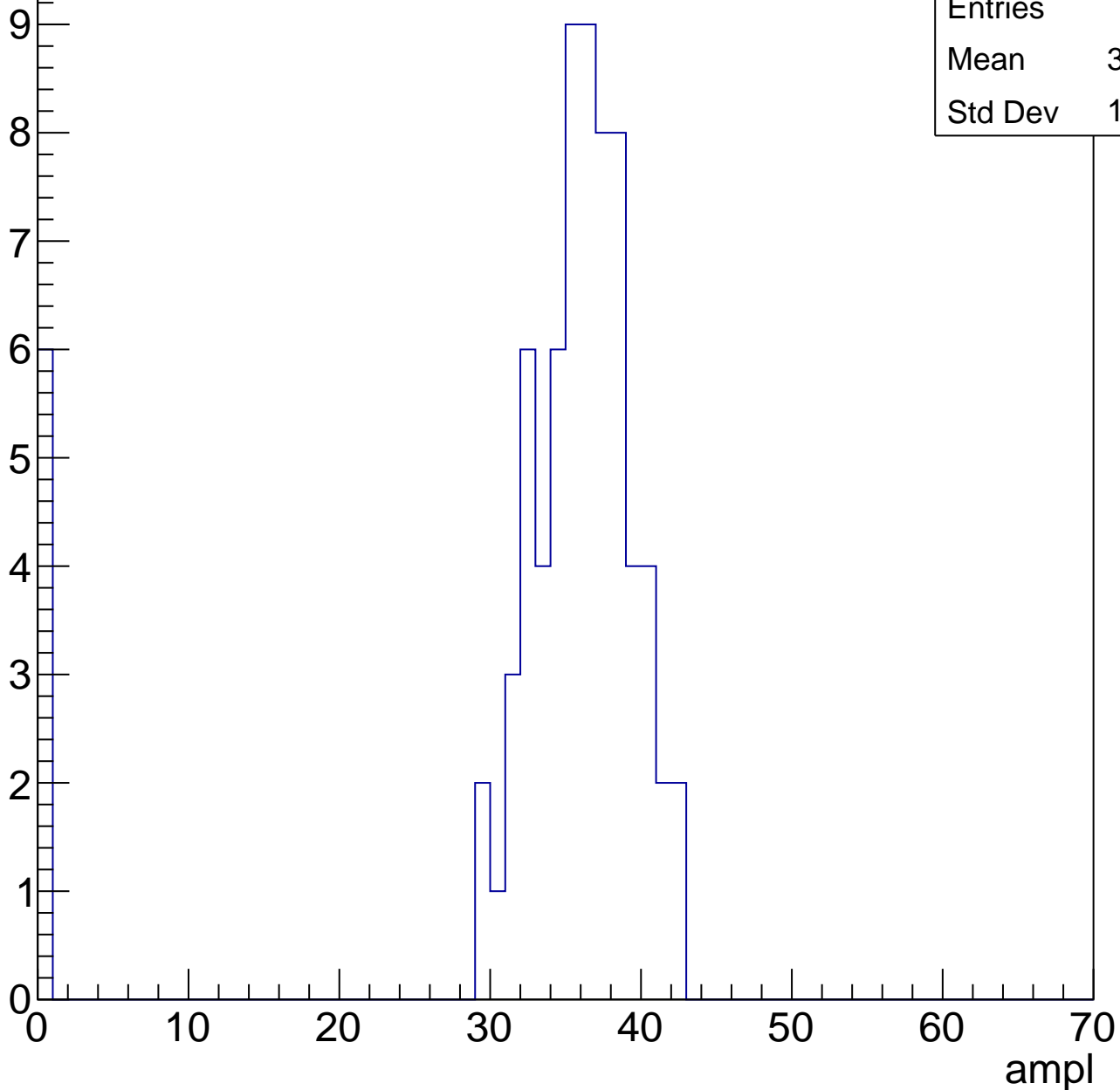


B1L103S, U9-ch24, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	32.84
Std Dev	10.18

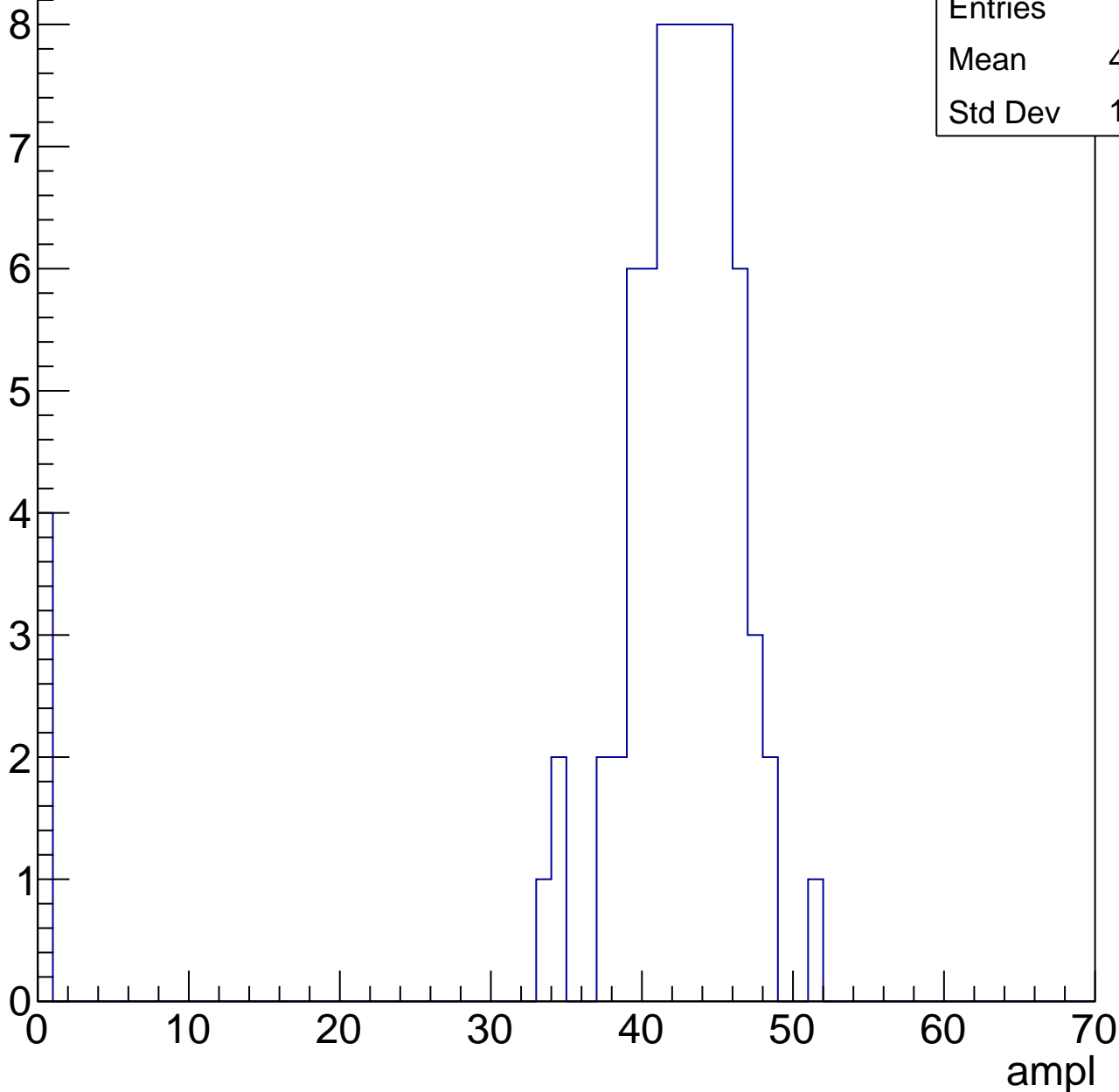


B1L103S, U9-ch24, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	40.12
Std Dev	10.07

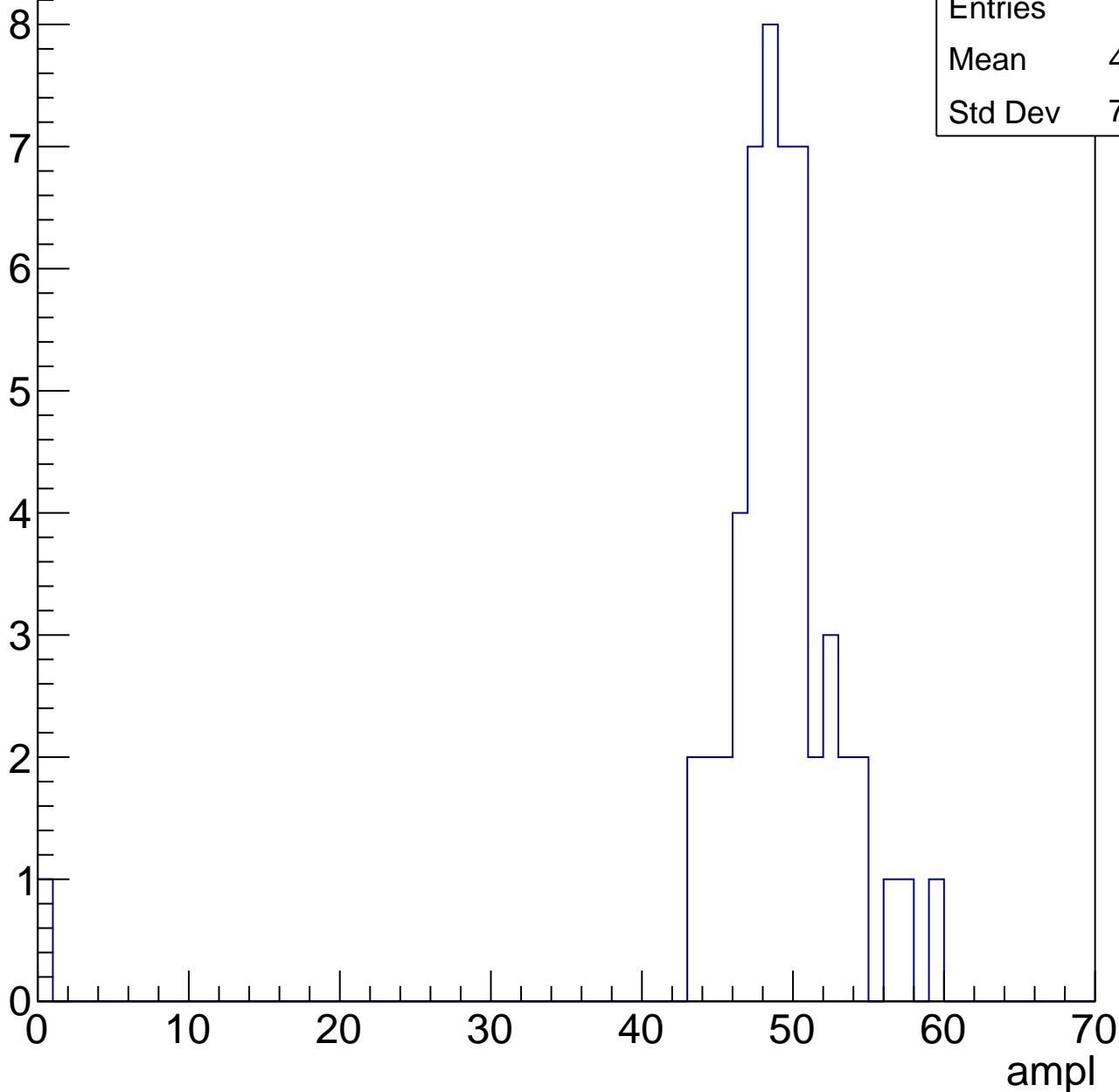


B1L103S, U9-ch24, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	48.04
Std Dev	7.488

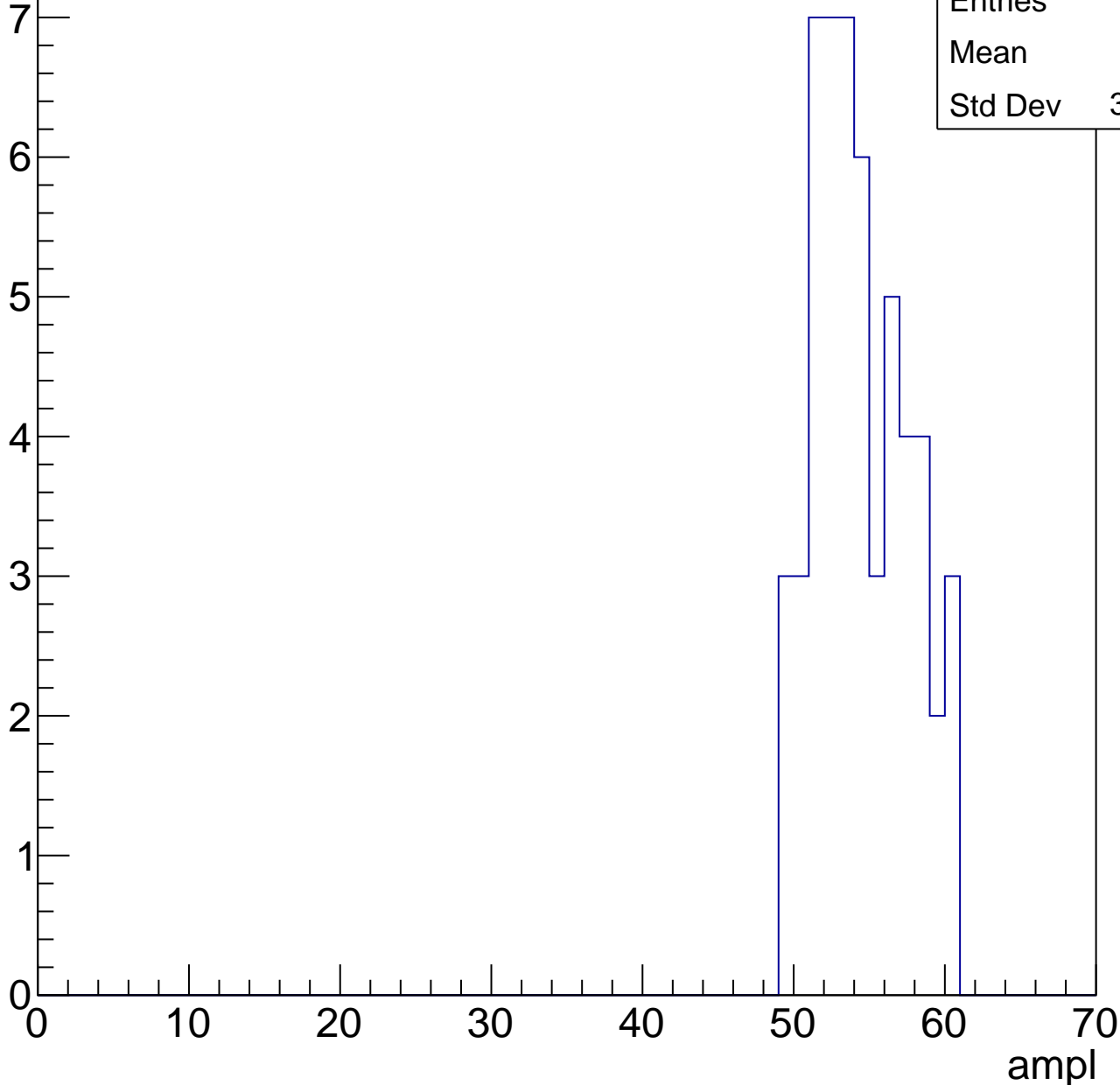


B1L103S, U9-ch24, adc4

calib_packv5_041523_1651.root, FC#0, port C2

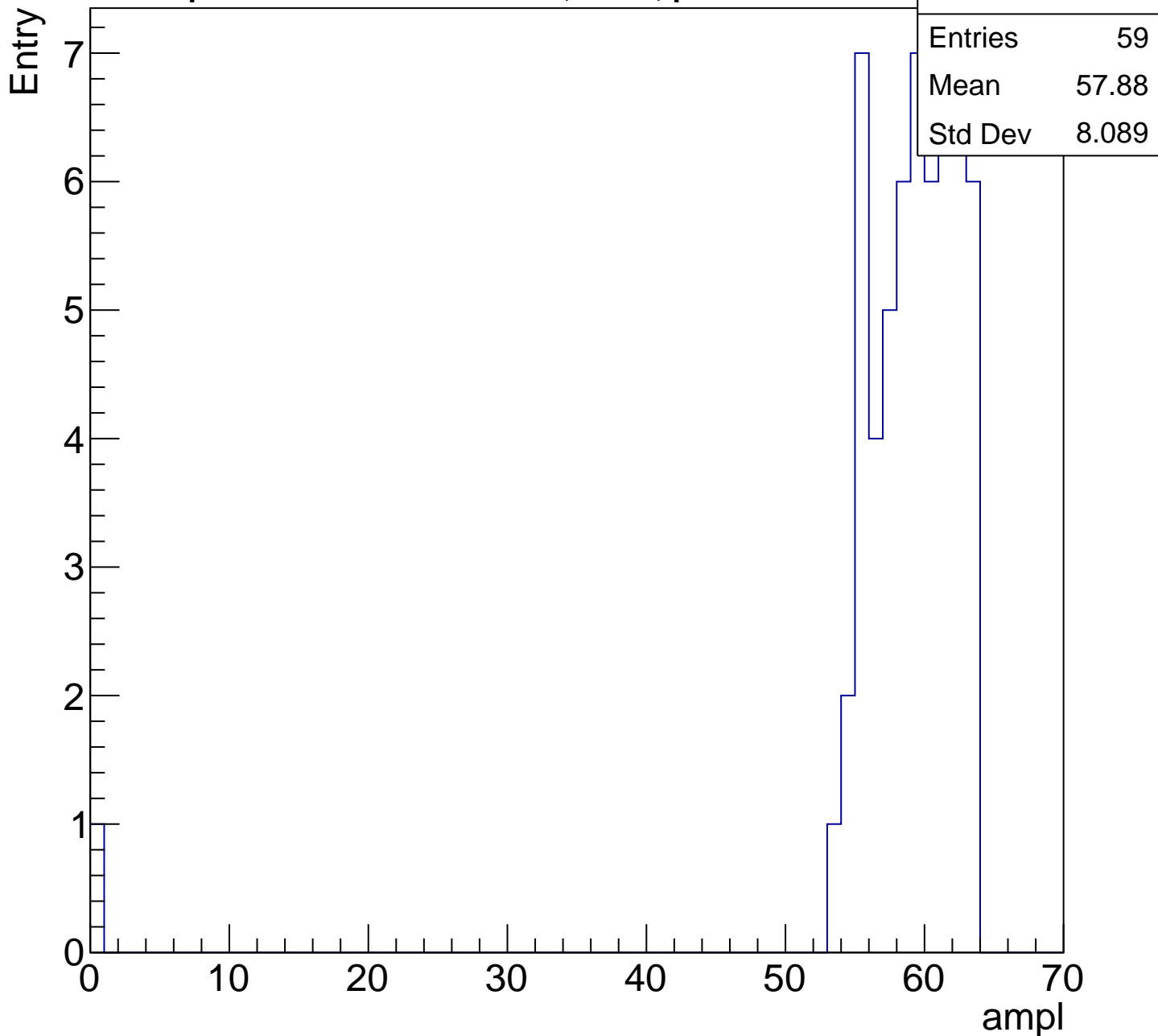
Entry

Entries	54
Mean	54
Std Dev	3.049



B1L103S, U9-ch24, adc5

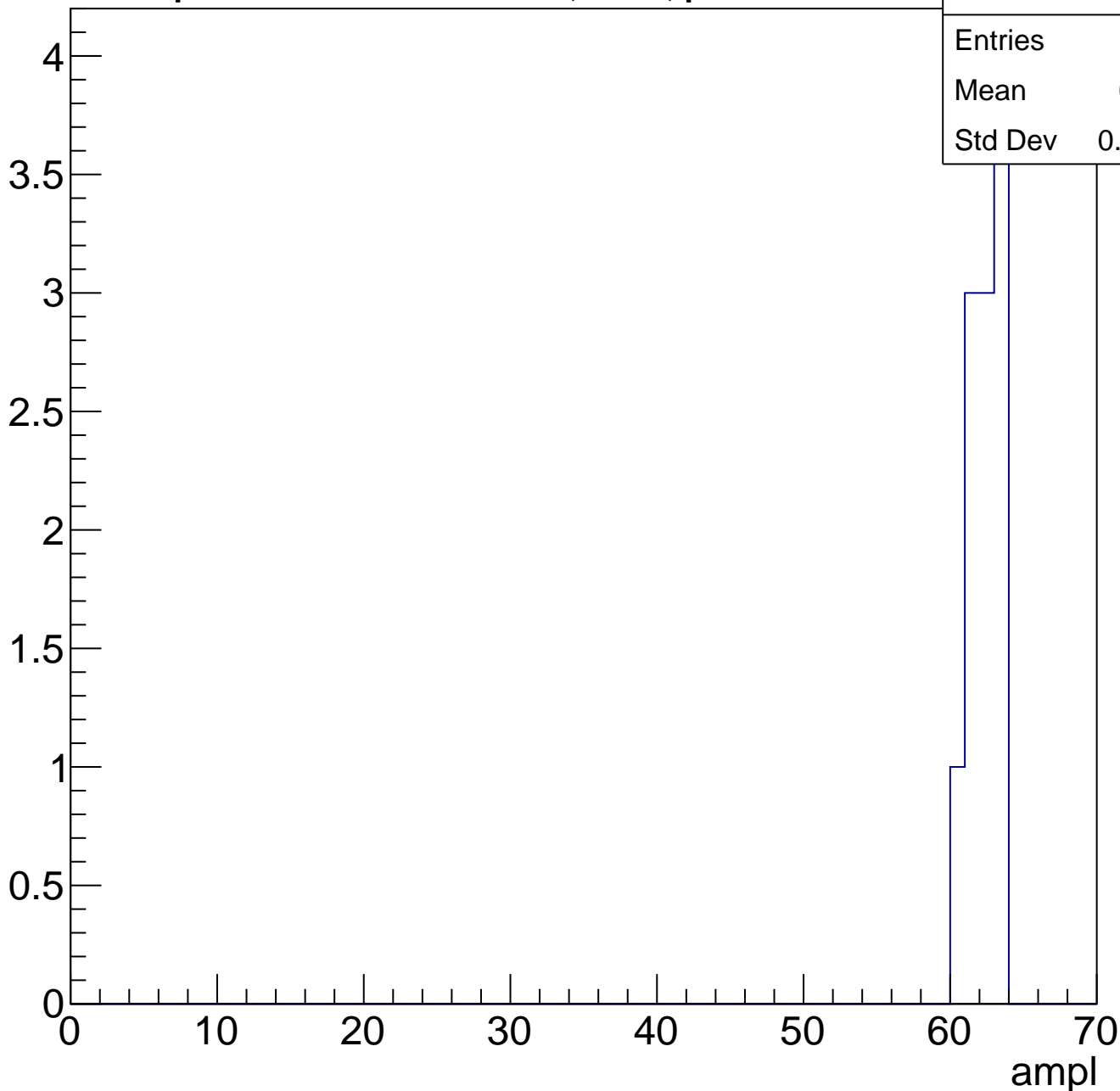
calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U9-ch24, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch24, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.158
Std Dev	4.913

Entry

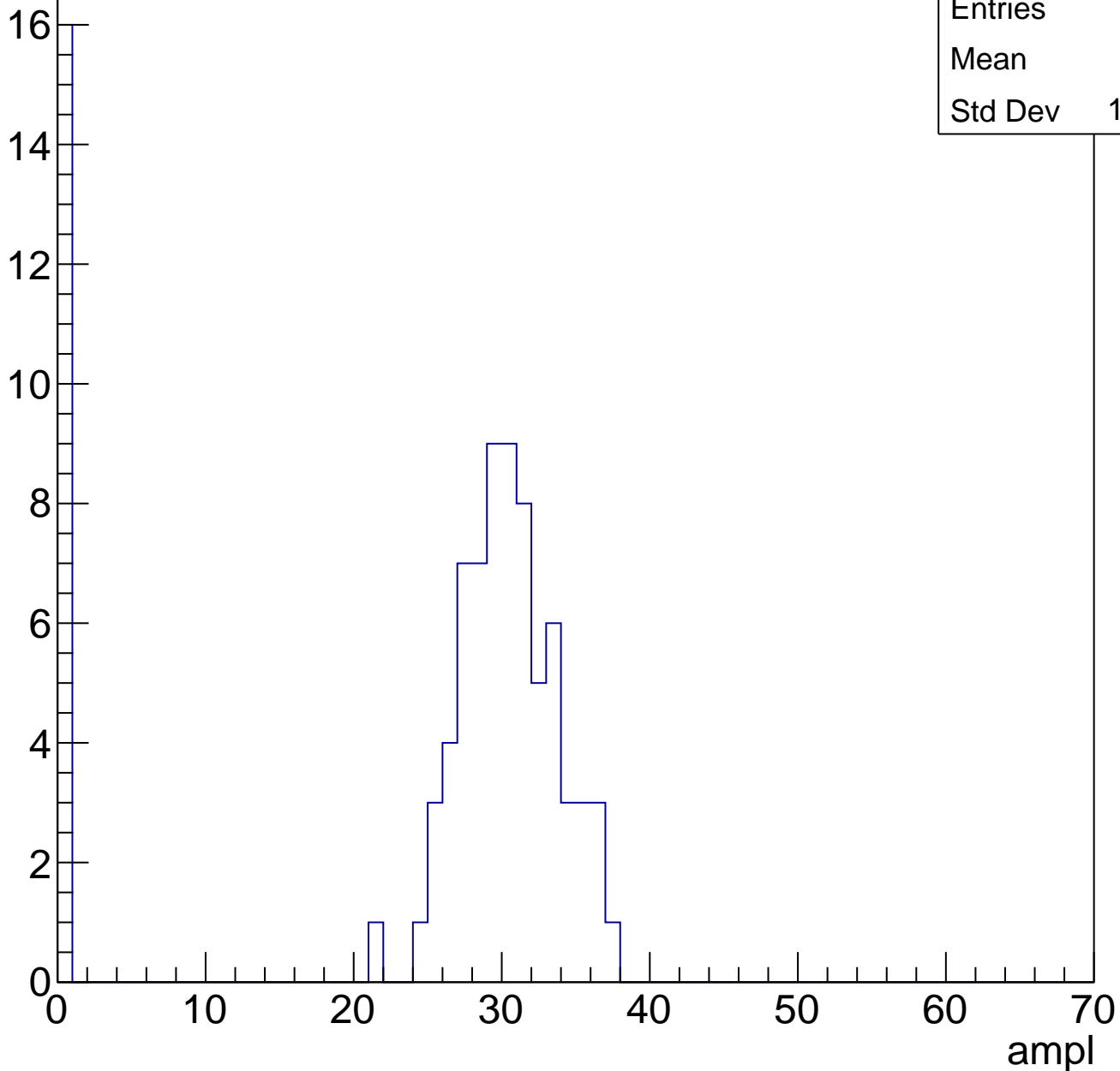


B1L103S, U9-ch25, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	86
Mean	24.4
Std Dev	12.02

Entry

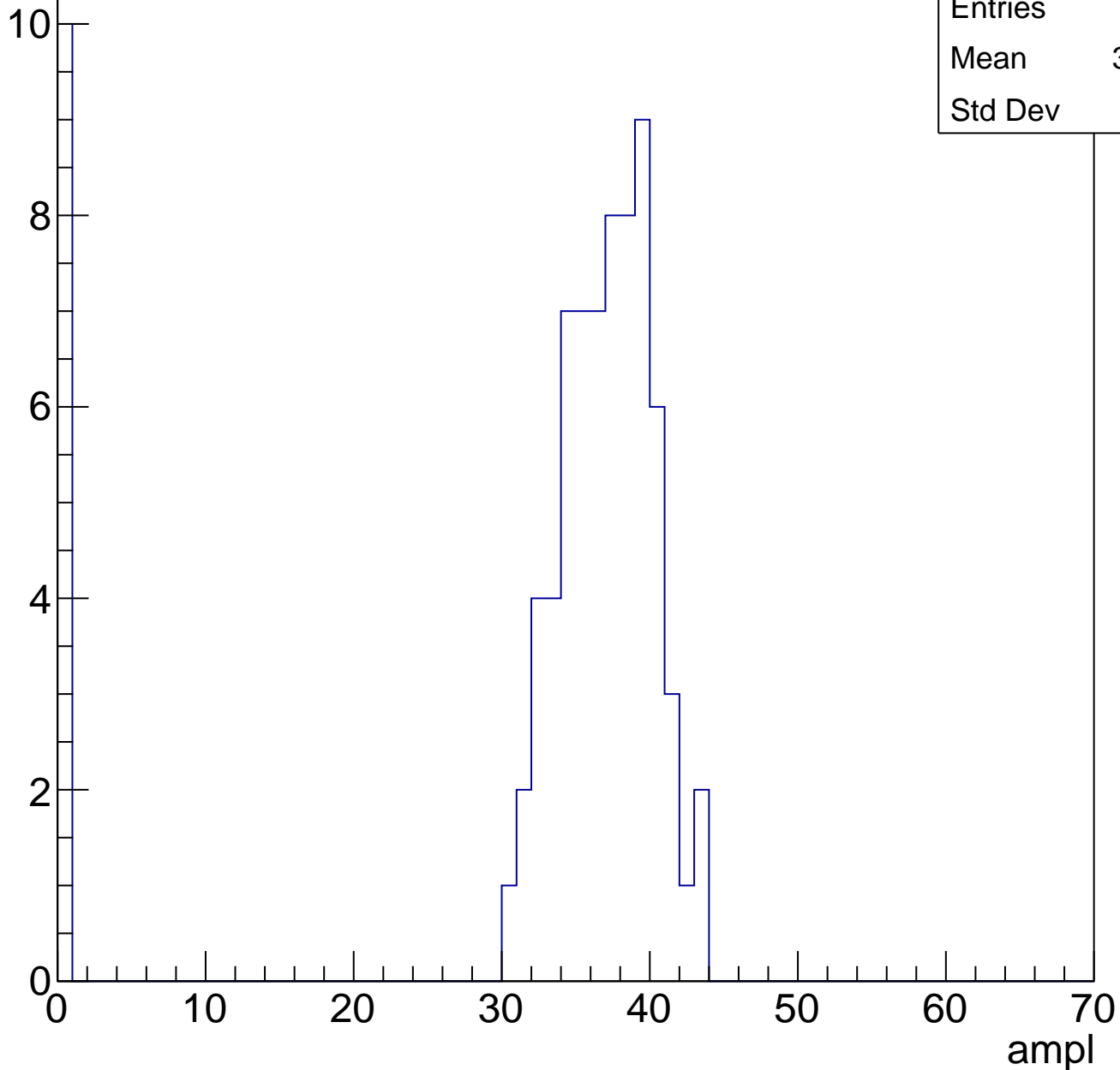


B1L103S, U9-ch25, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	79
Mean	32.01
Std Dev	12.5

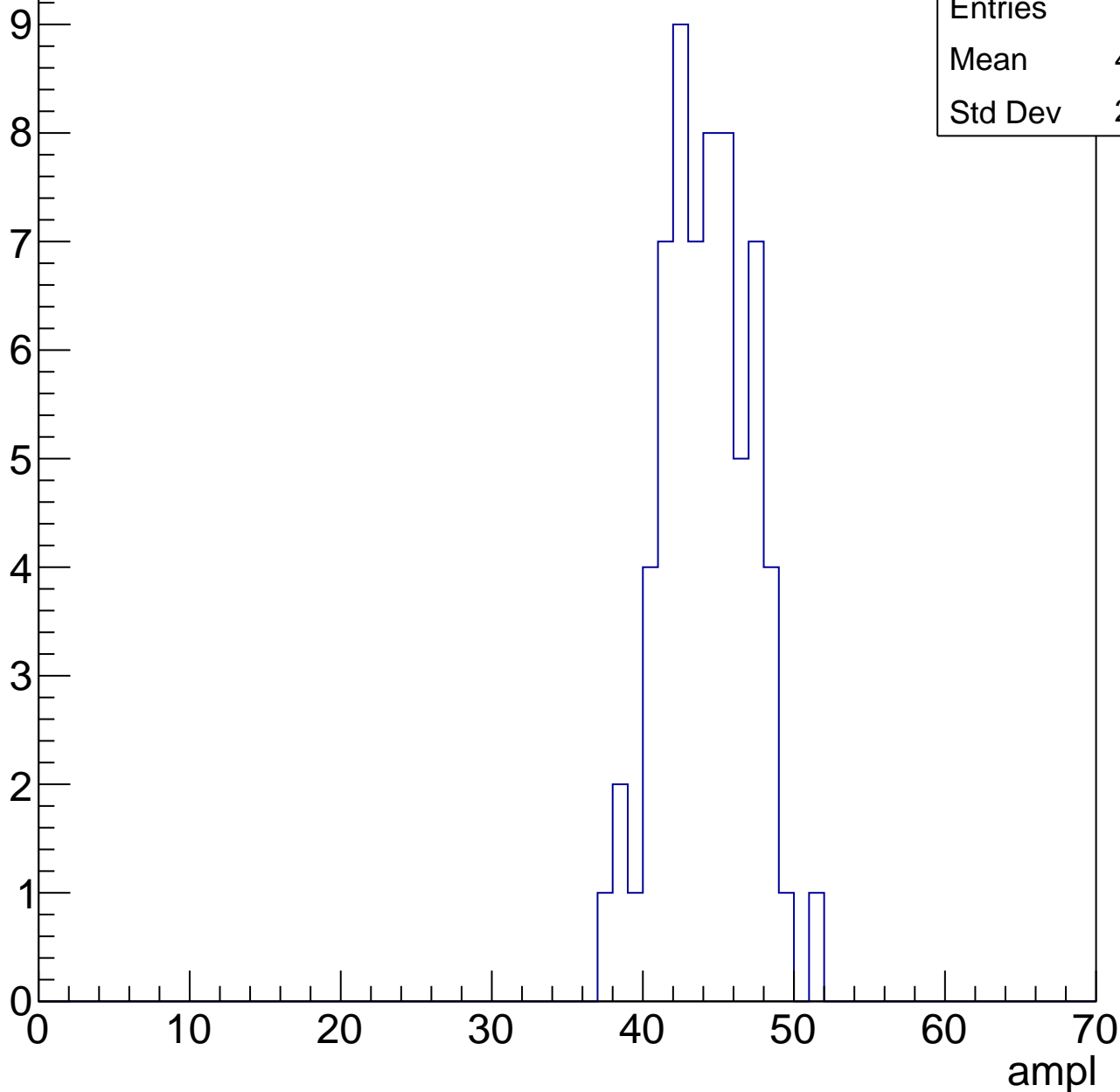
Entry



B1L103S, U9-ch25, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry



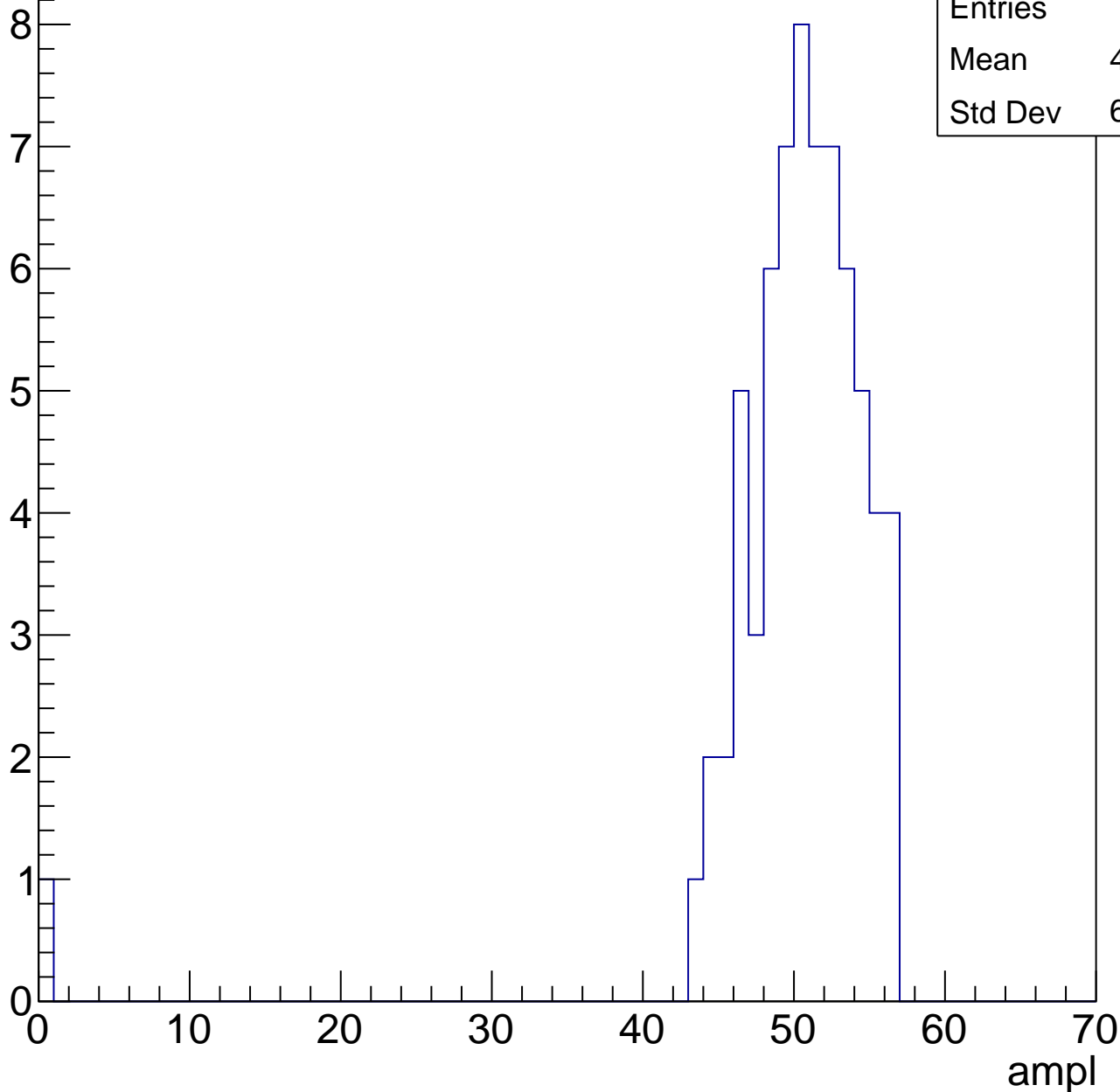
Entries	65
Mean	43.71
Std Dev	2.881

B1L103S, U9-ch25, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	49.65
Std Dev	6.874

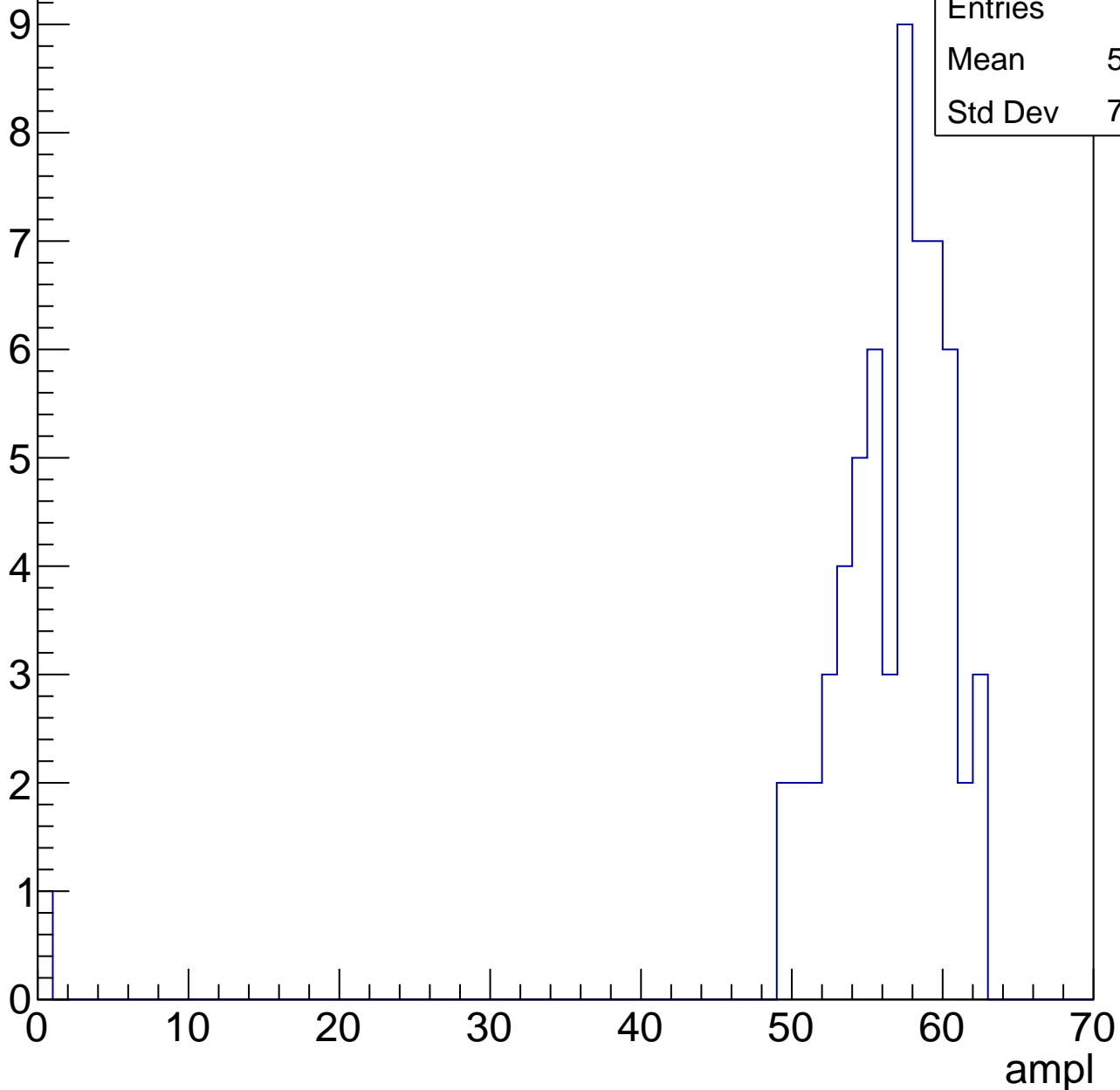


B1L103S, U9-ch25, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	55.42
Std Dev	7.828



B1L103S, U9-ch25, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

Entries 38

Mean 60.68

Std Dev 2.153

8

6

4

2

0

0

10

20

30

40

50

ampl

B1L103S, U9-ch25, adc6

calib_packv5_041523_1651.root, FC#0, port C2

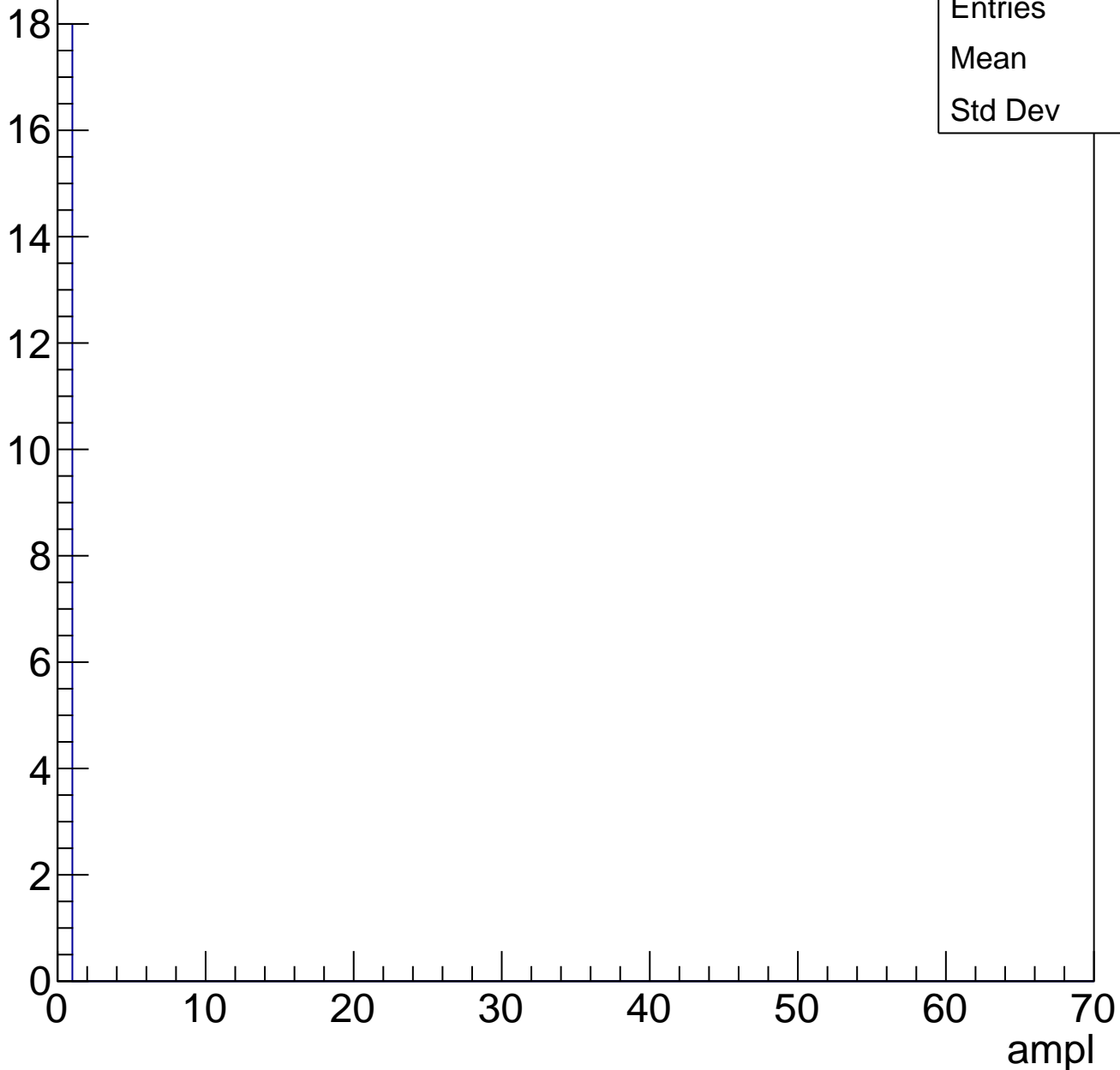
Entry



B1L103S, U9-ch25, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch26, adc0

calib_packv5_041523_1651.root, FC#0, port C2

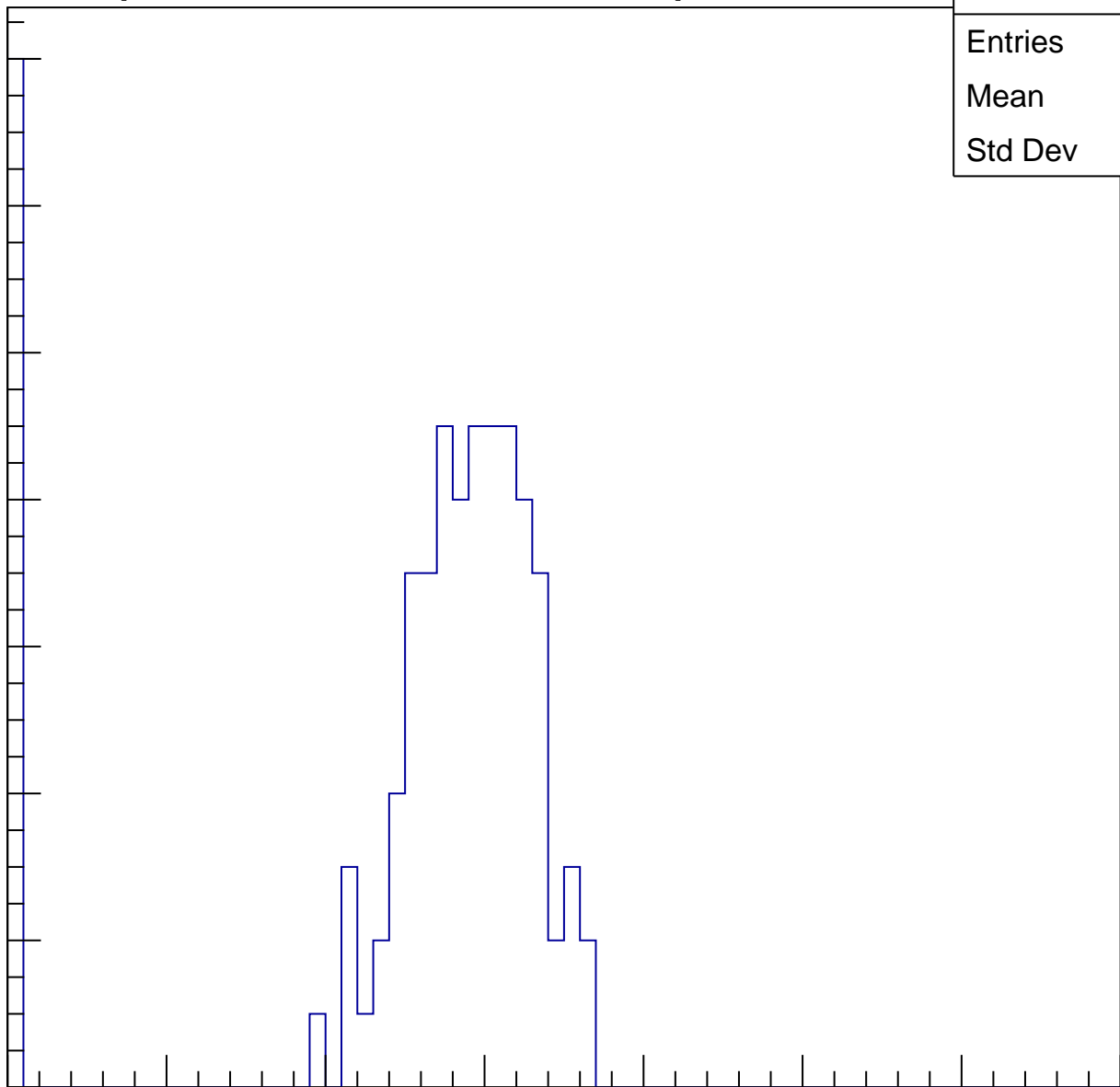
Entries	105
Mean	24.88
Std Dev	10.33

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

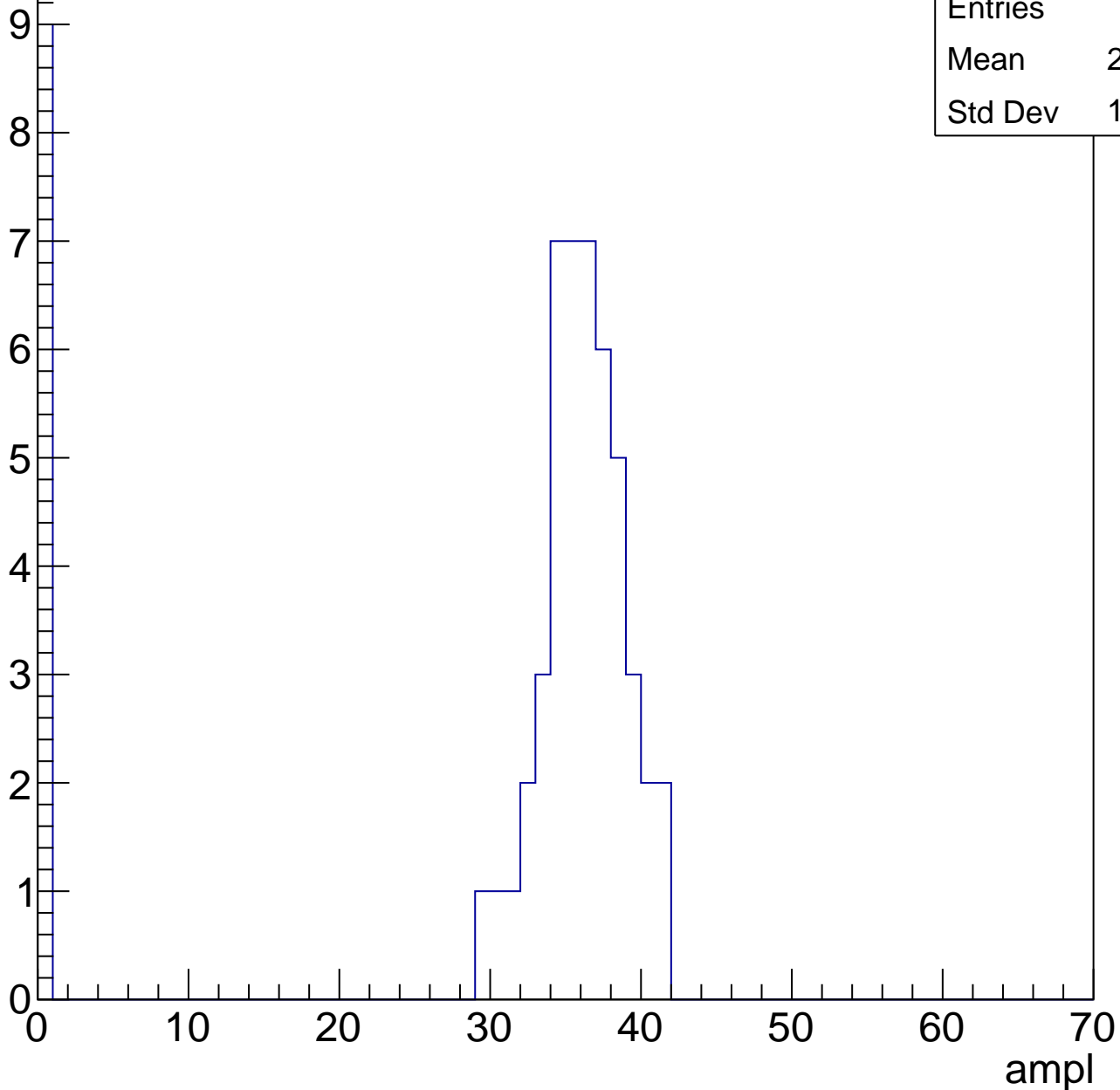


B1L103S, U9-ch26, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	29.98
Std Dev	13.35

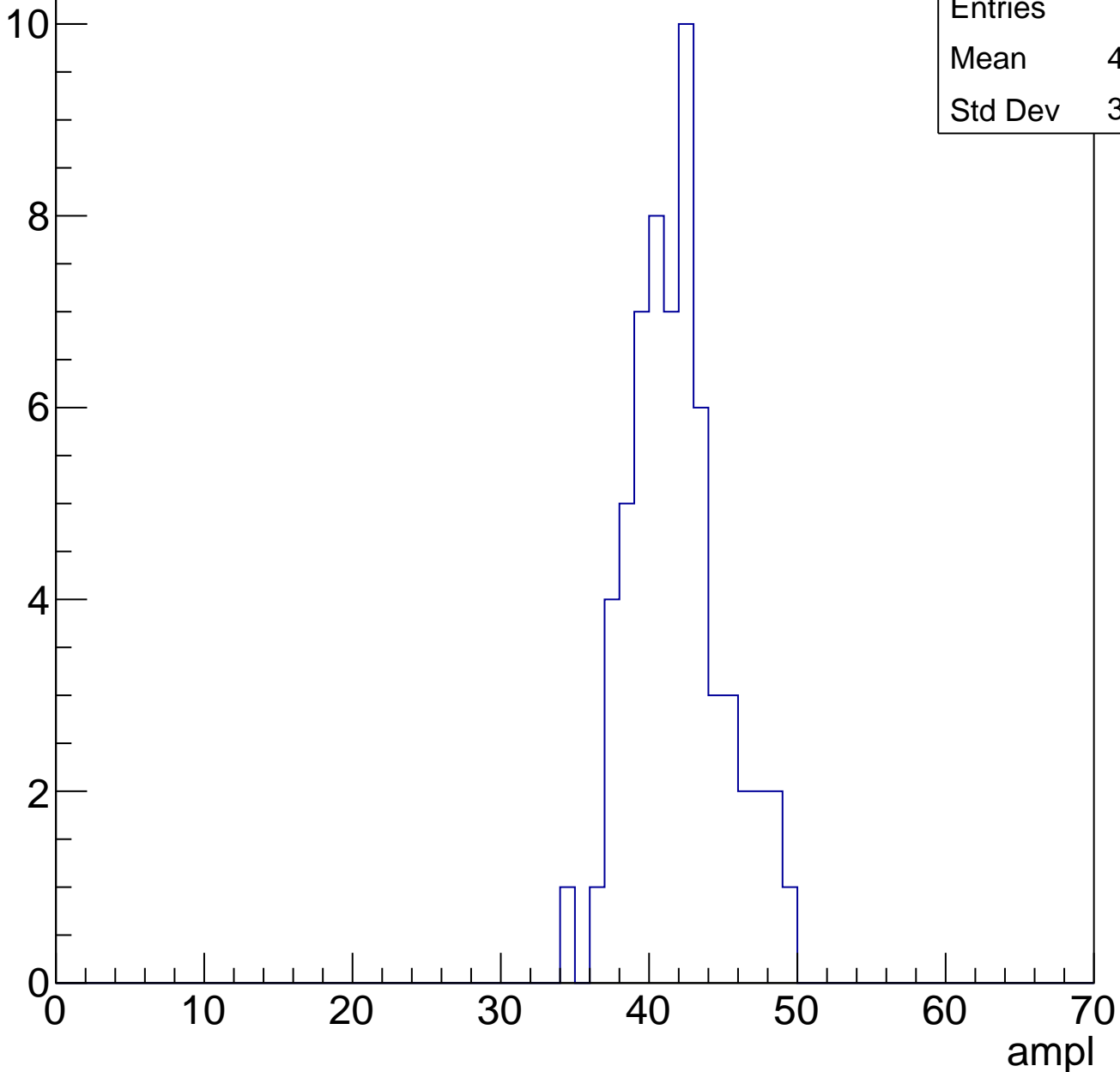


B1L103S, U9-ch26, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	62
Mean	41.35
Std Dev	3.122

Entry

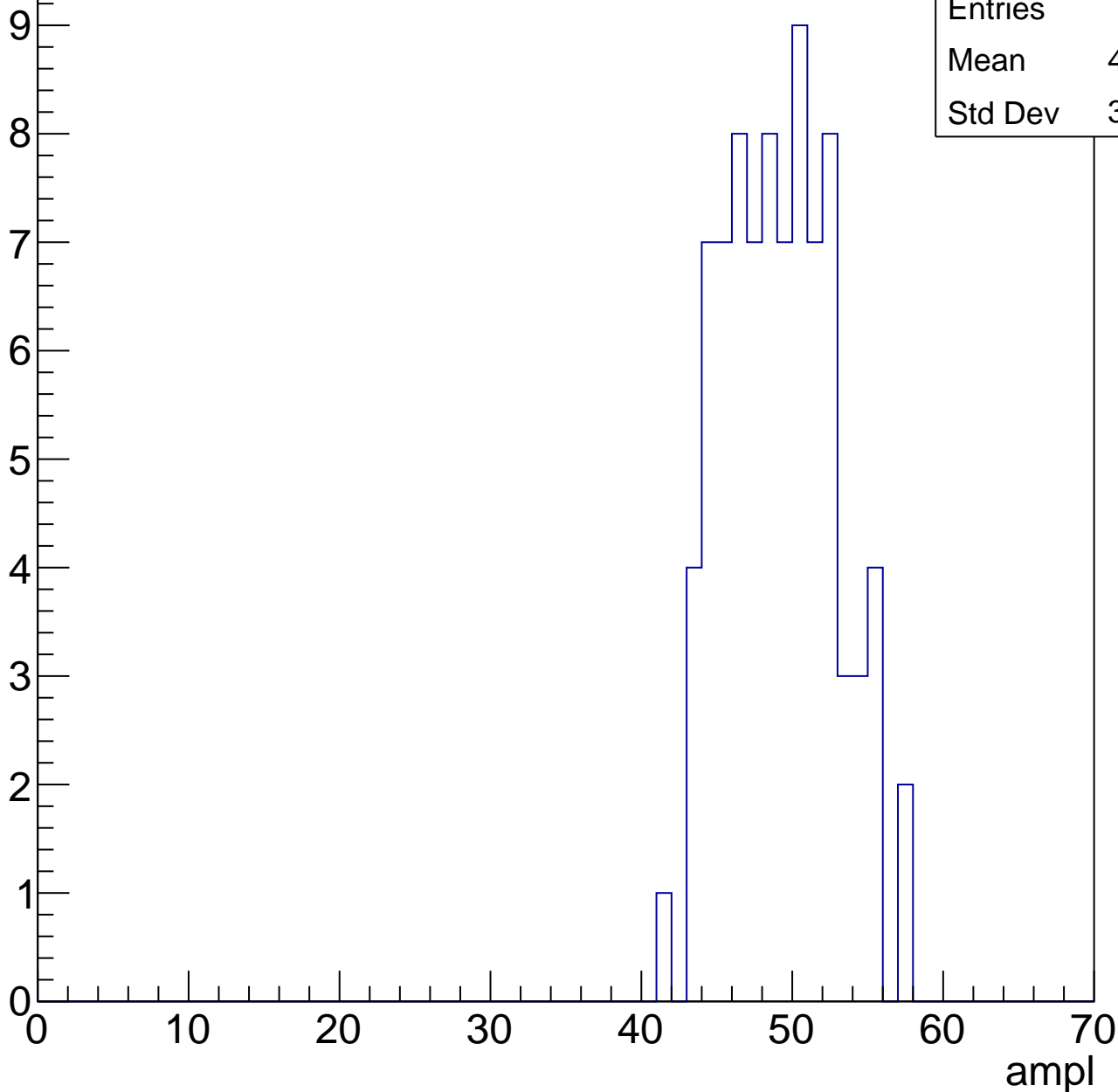


B1L103S, U9-ch26, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	85
Mean	48.68
Std Dev	3.595

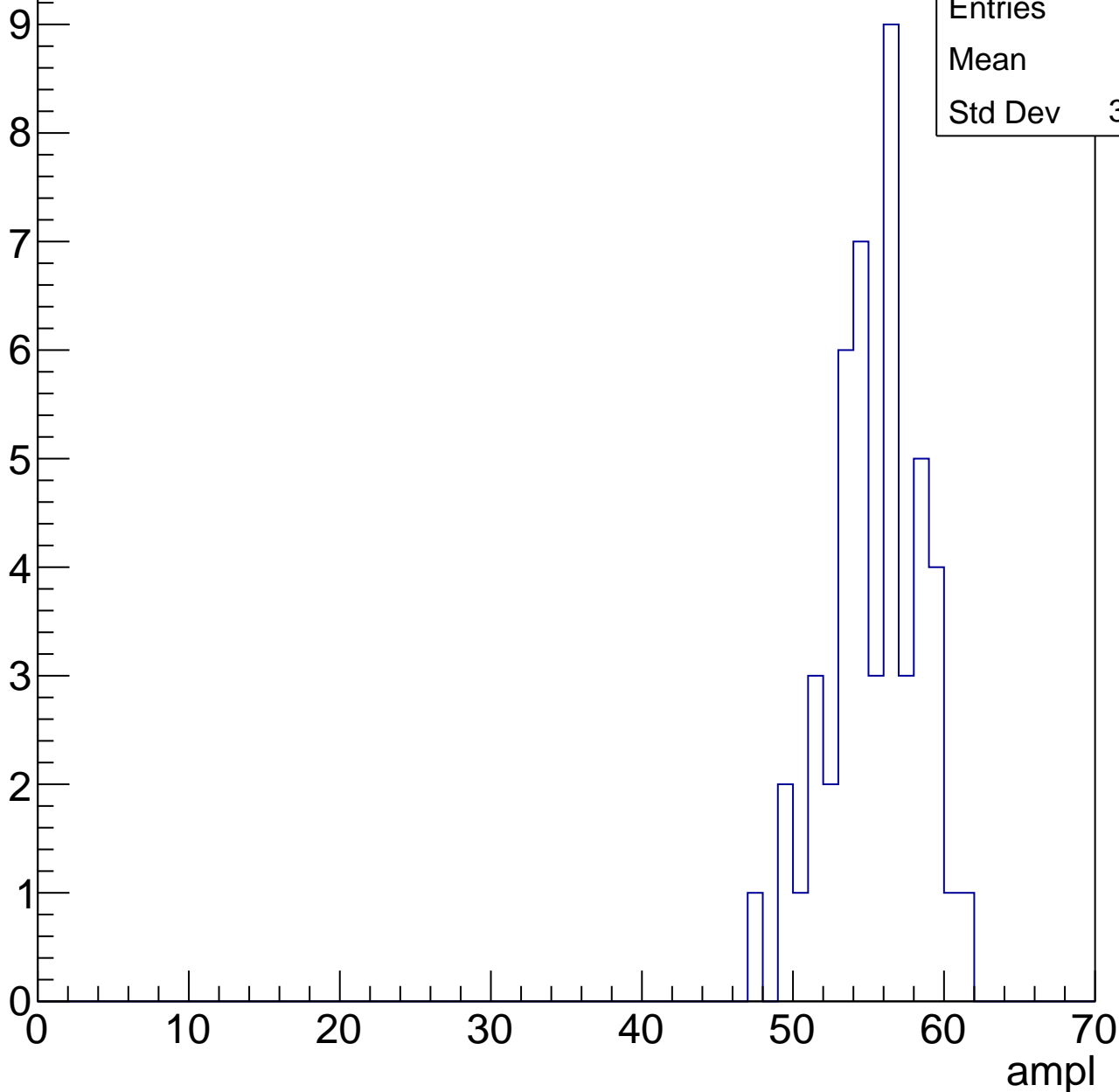


B1L103S, U9-ch26, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	48
Mean	54.9
Std Dev	3.057

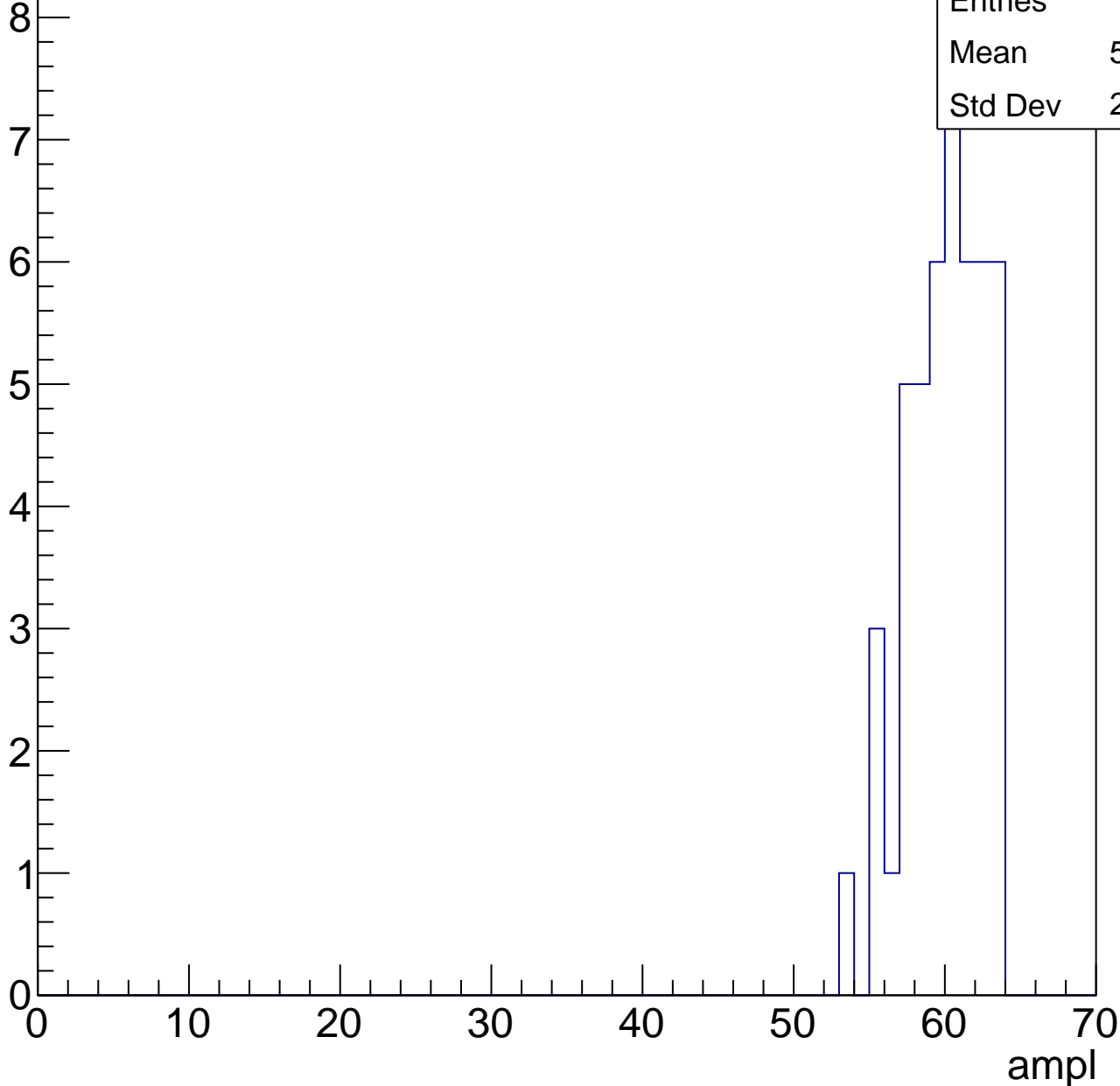


B1L103S, U9-ch26, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

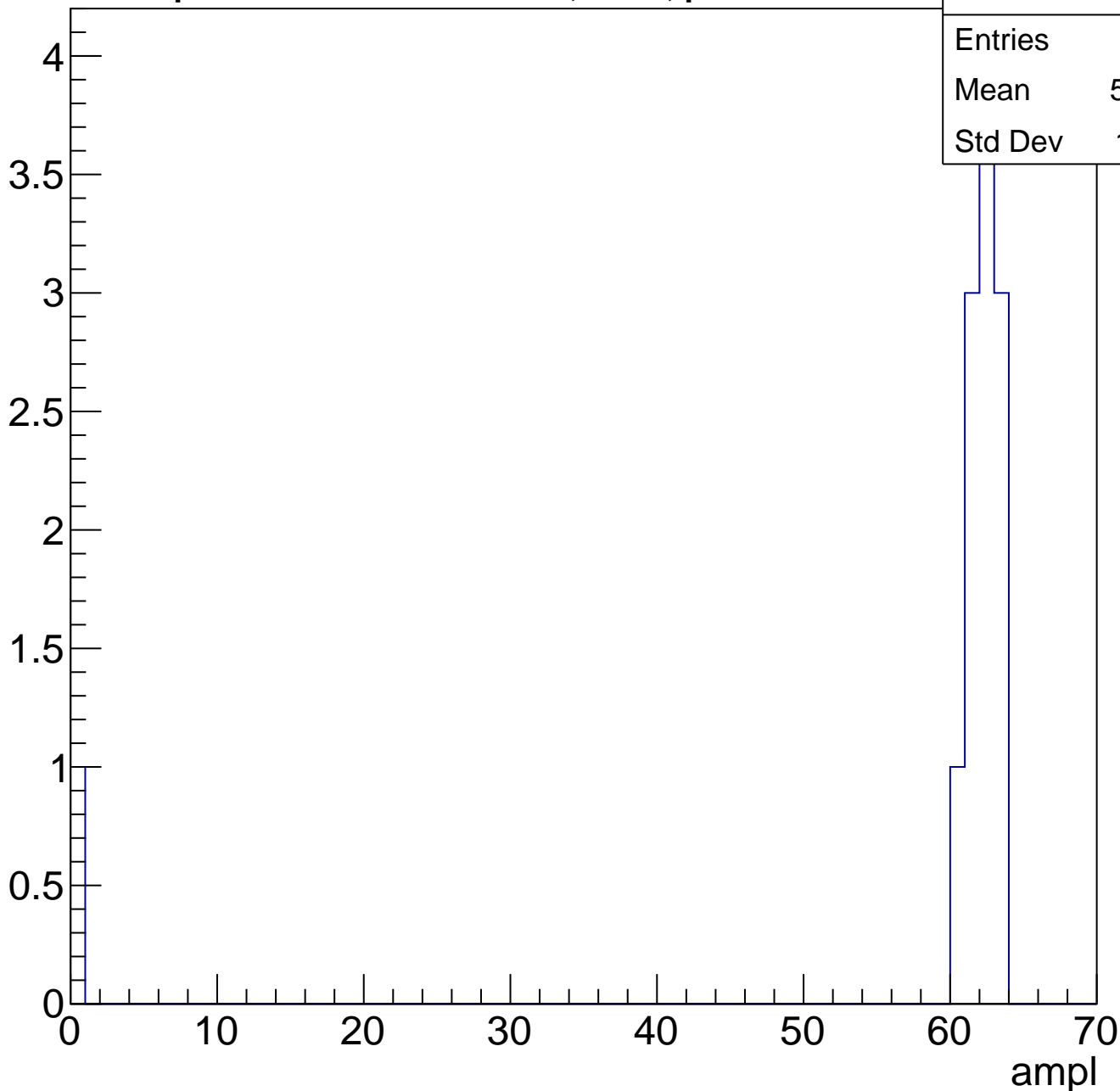
Entries	47
Mean	59.55
Std Dev	2.465



B1L103S, U9-ch26, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch26, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry



B1L103S, U9-ch27, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	70
Mean	25.16
Std Dev	11.22

Entry

10

8

6

4

2

0

0

10

20

30

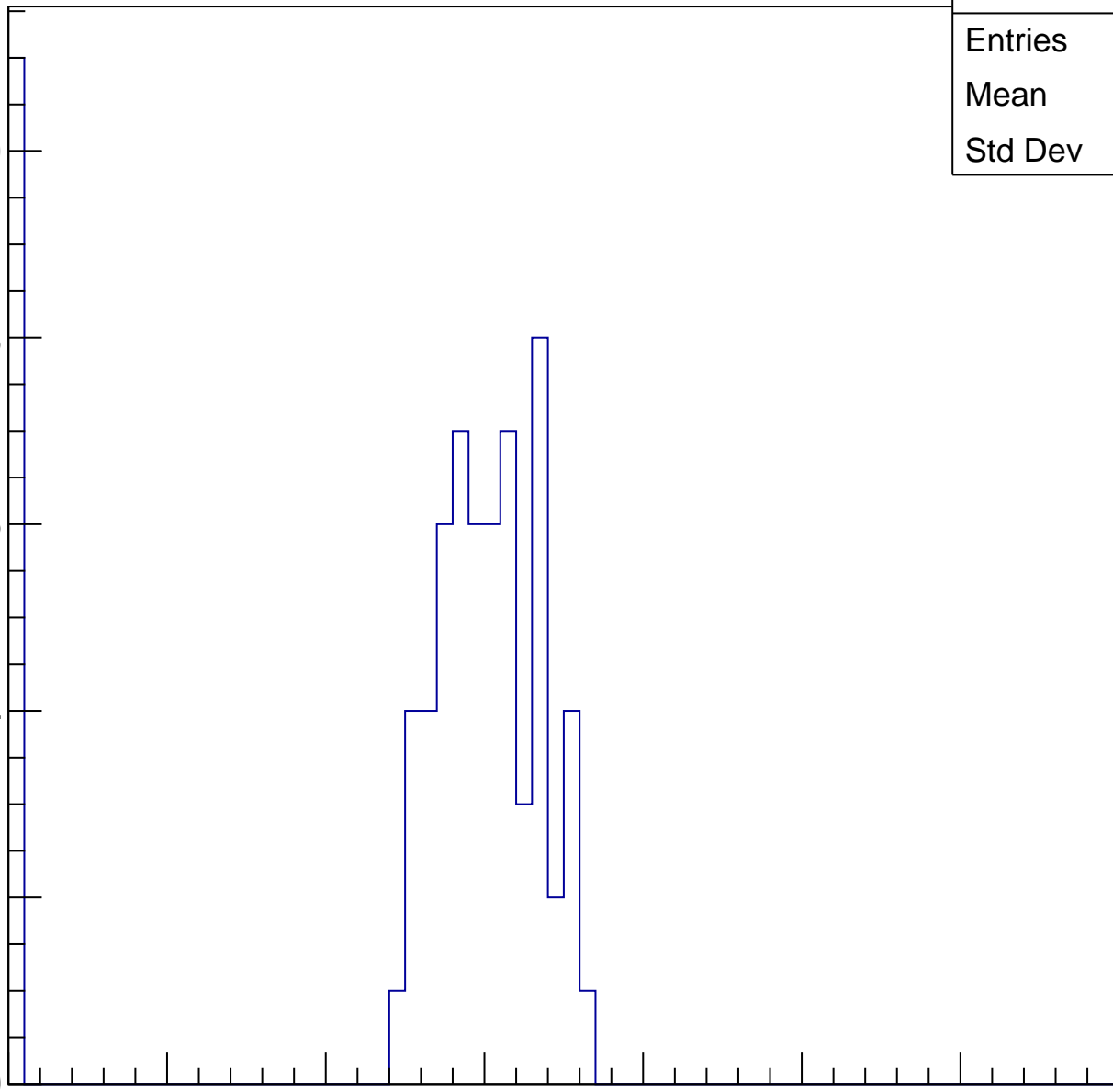
40

50

60

70

ampl



B1L103S, U9-ch27, adc1

calib_packv5_041523_1651.root, FC#0, port C2

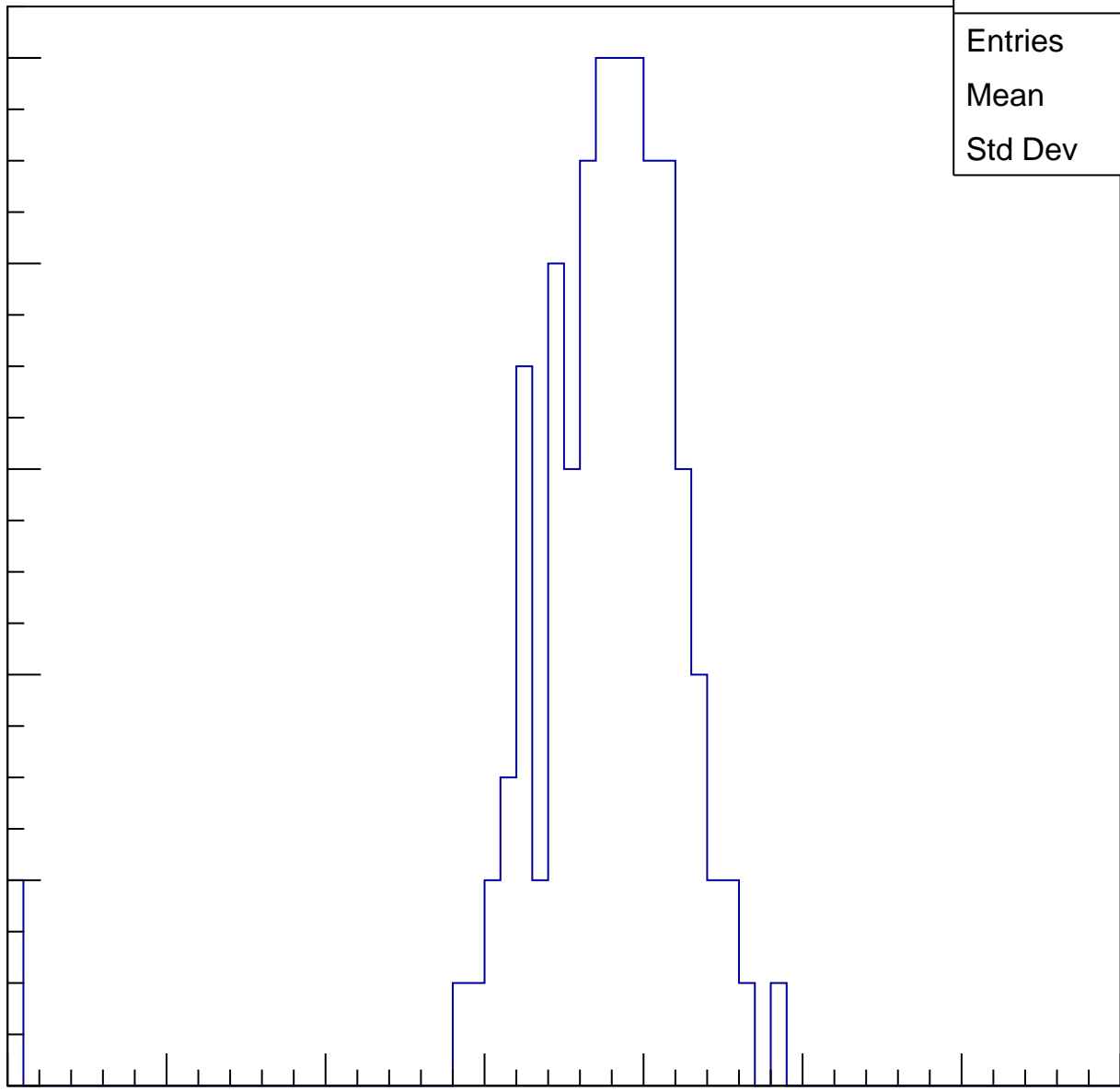
Entries	105
Mean	36.87
Std Dev	6.471

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl



B1L103S, U9-ch27, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

8

6

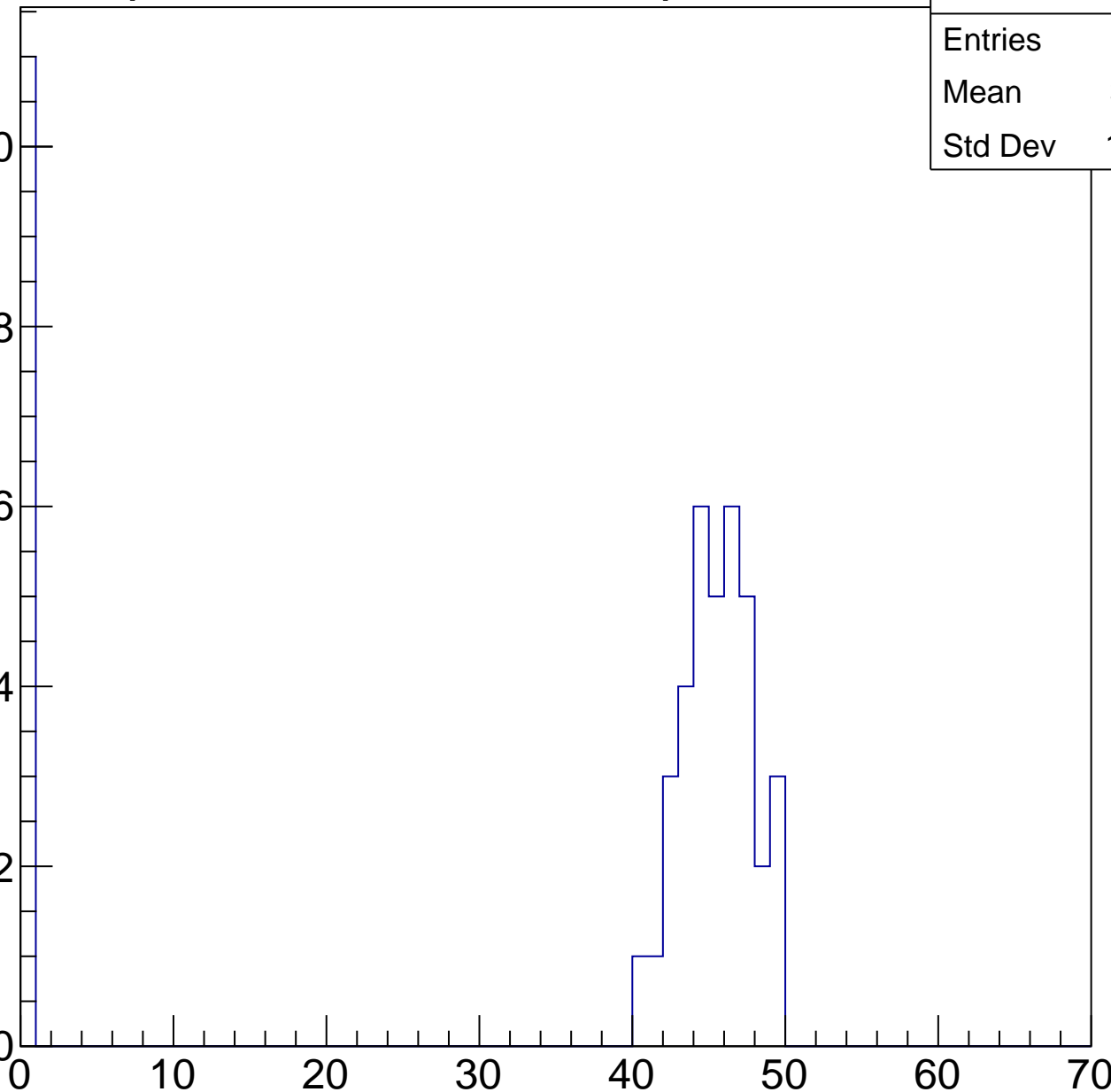
4

2

0

Entries	47
Mean	34.51
Std Dev	19.18

ampl

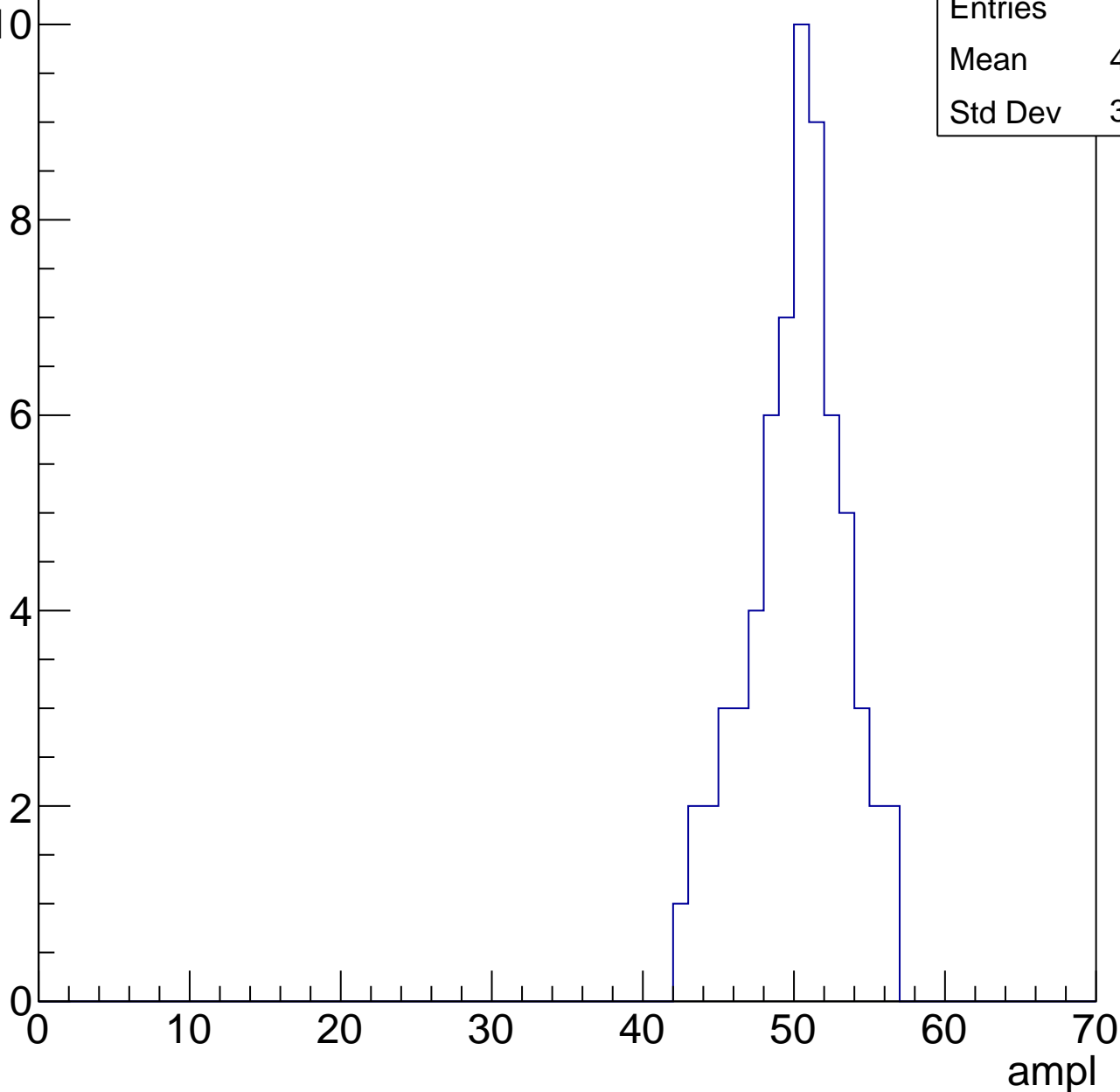


B1L103S, U9-ch27, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	49.66
Std Dev	3.197

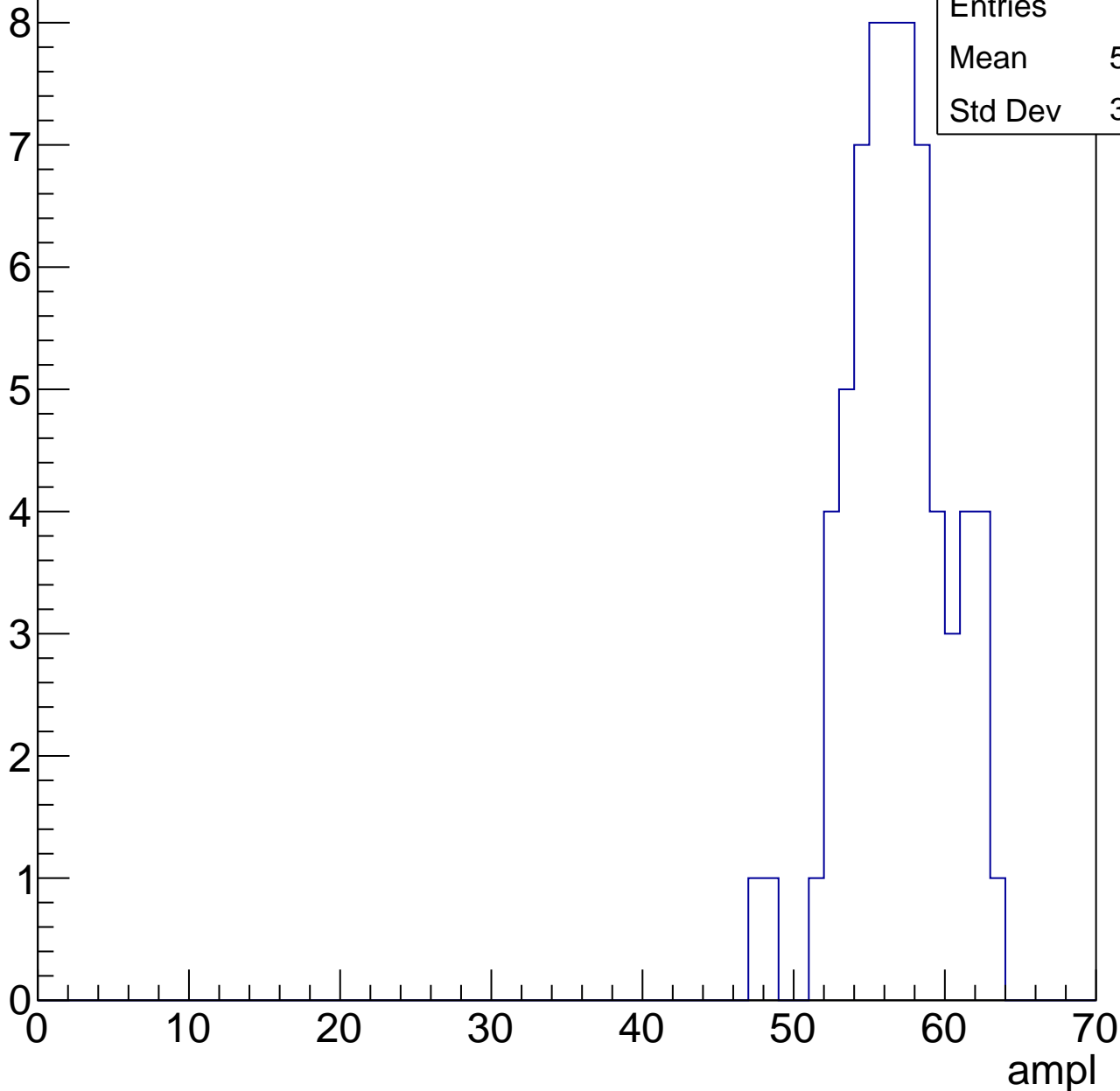


B1L103S, U9-ch27, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	56.33
Std Dev	3.304

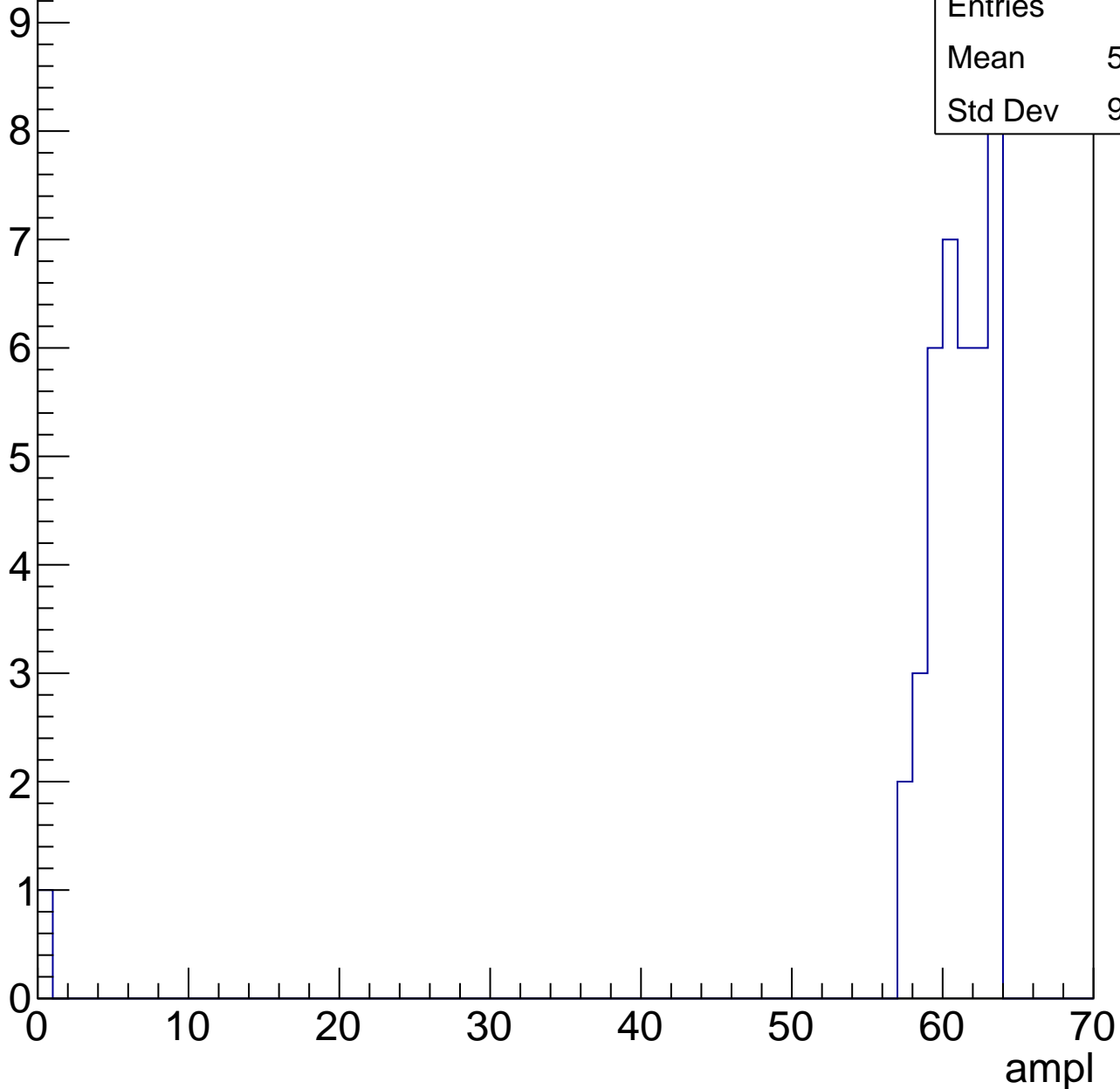


B1L103S, U9-ch27, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	59.17
Std Dev	9.643



B1L103S, U9-ch27, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



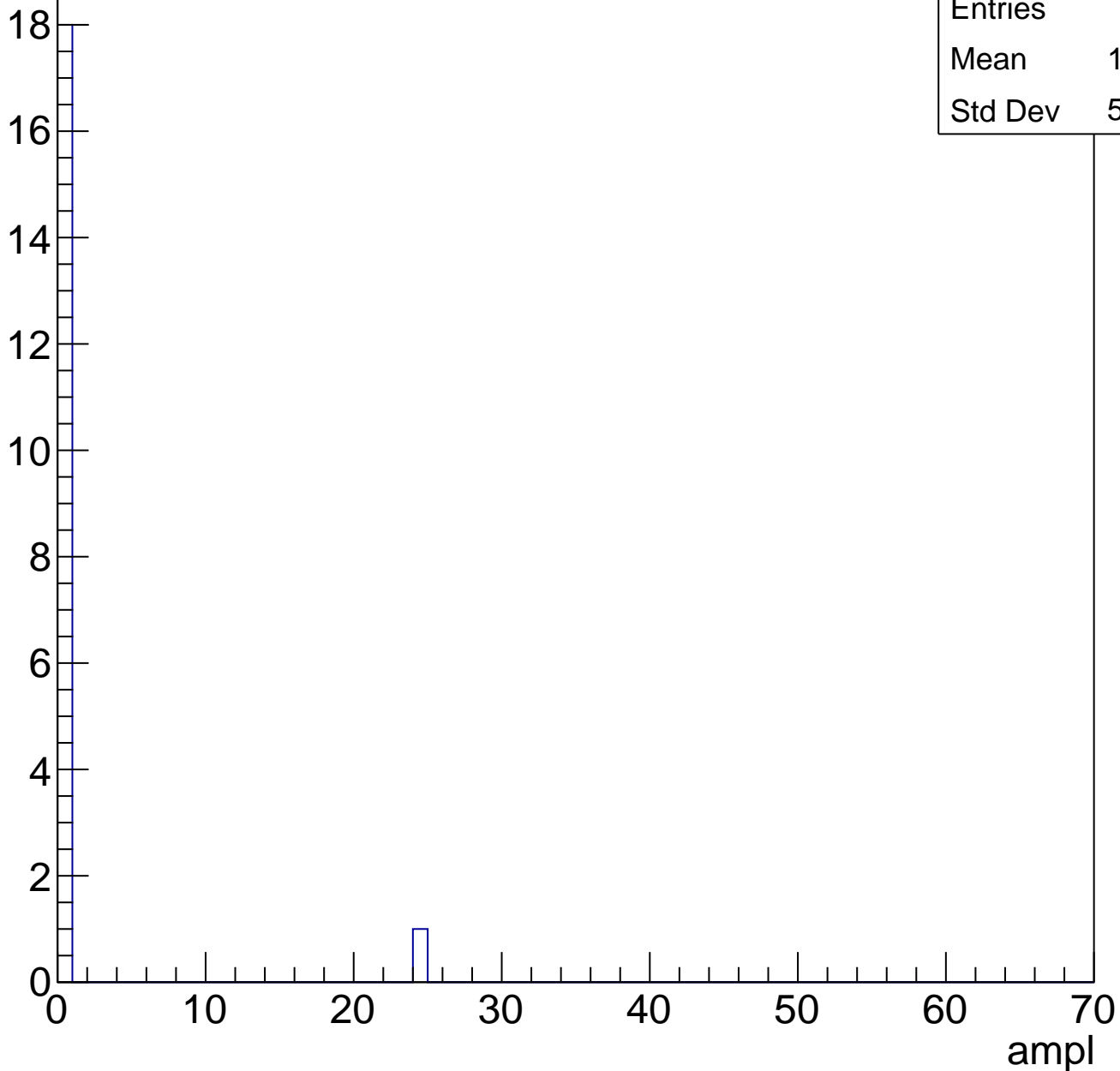
Entries	0
Mean	0
Std Dev	0

B1L103S, U9-ch27, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.263
Std Dev	5.359

Entry

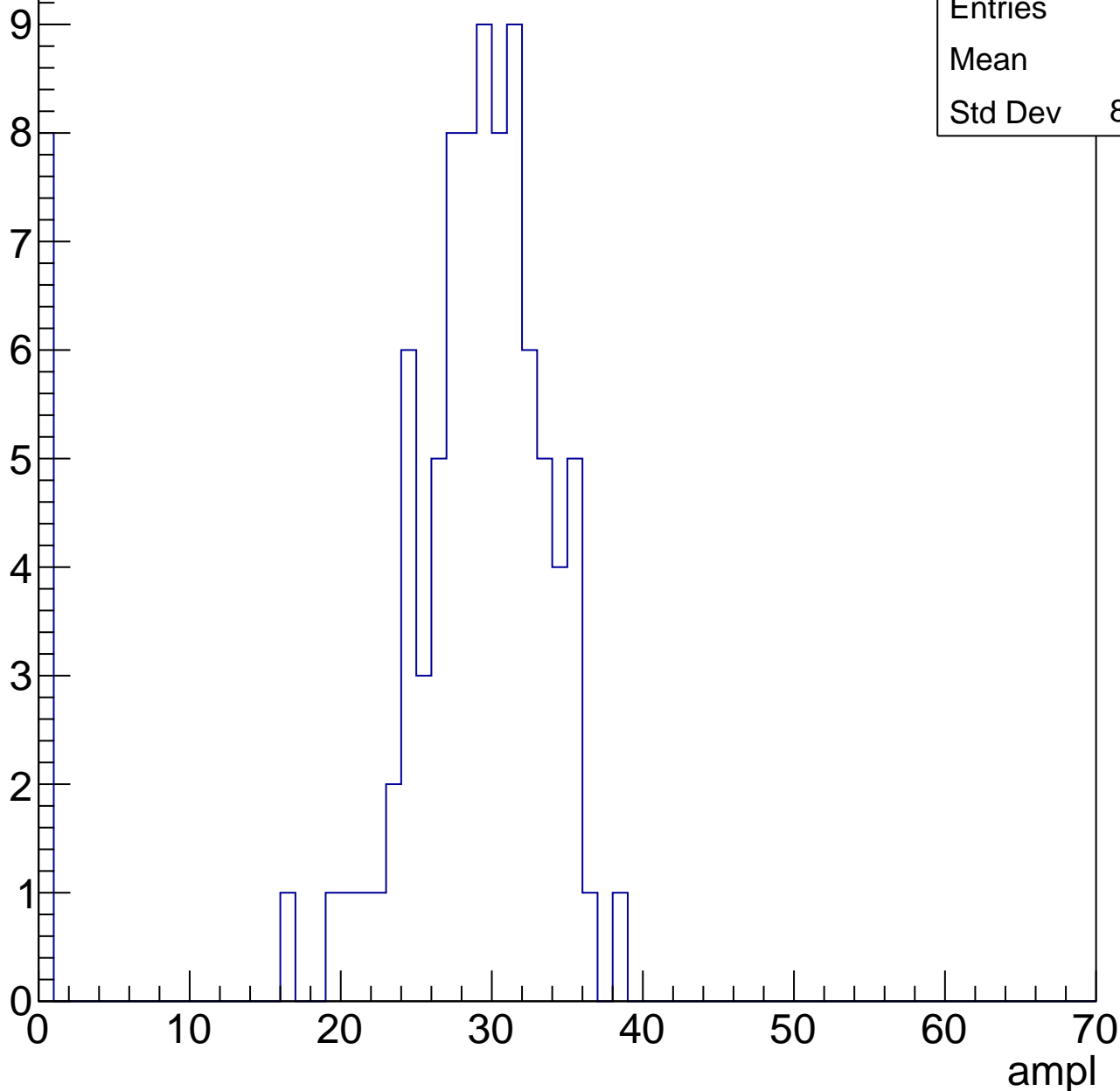


B1L103S, U9-ch28, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	93
Mean	26.4
Std Dev	8.983



B1L103S, U9-ch28, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	77
Mean	30.99
Std Dev	13.05

Entry

10

8

6

4

2

0

0

10

20

30

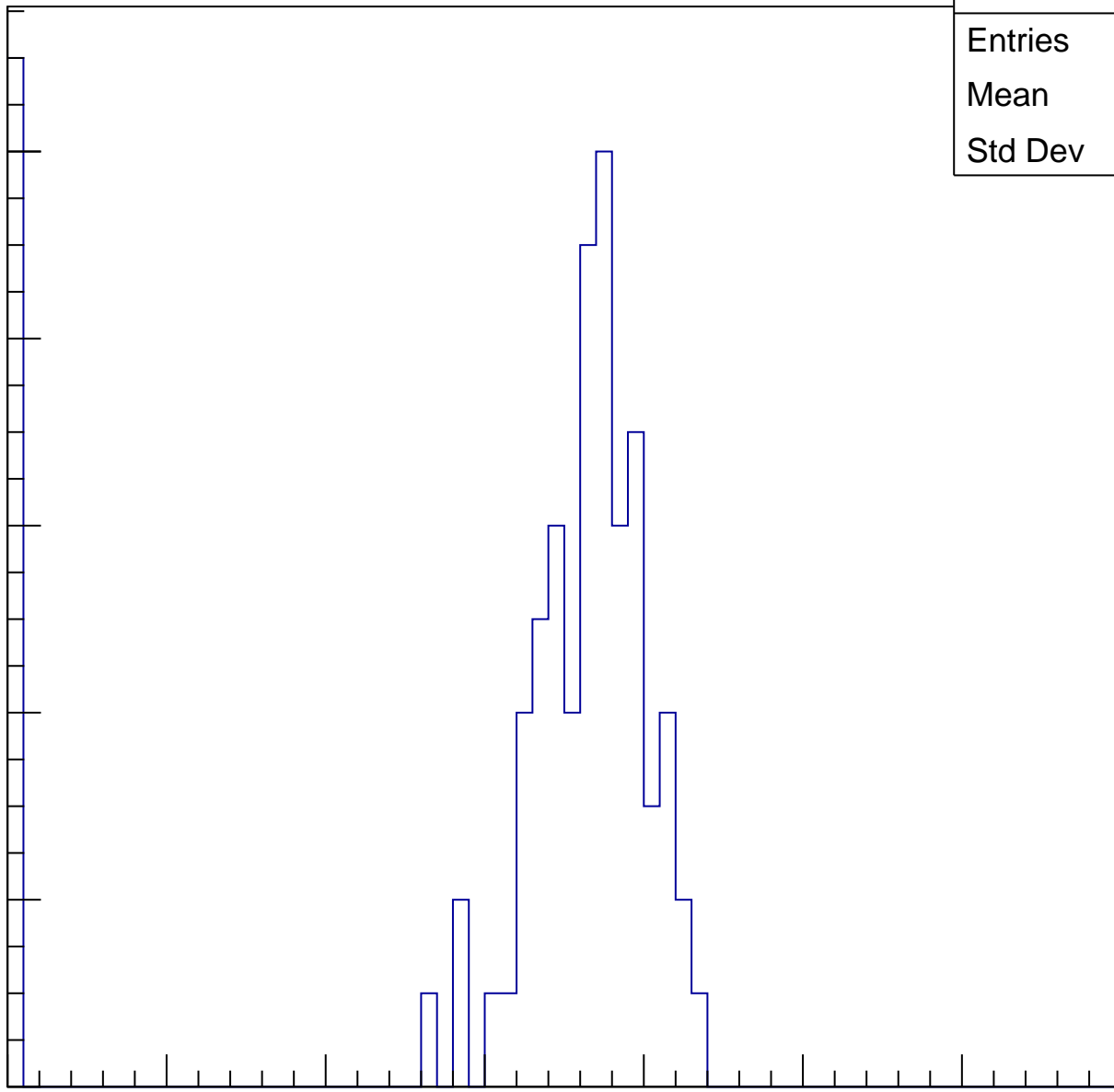
40

50

60

70

ampl

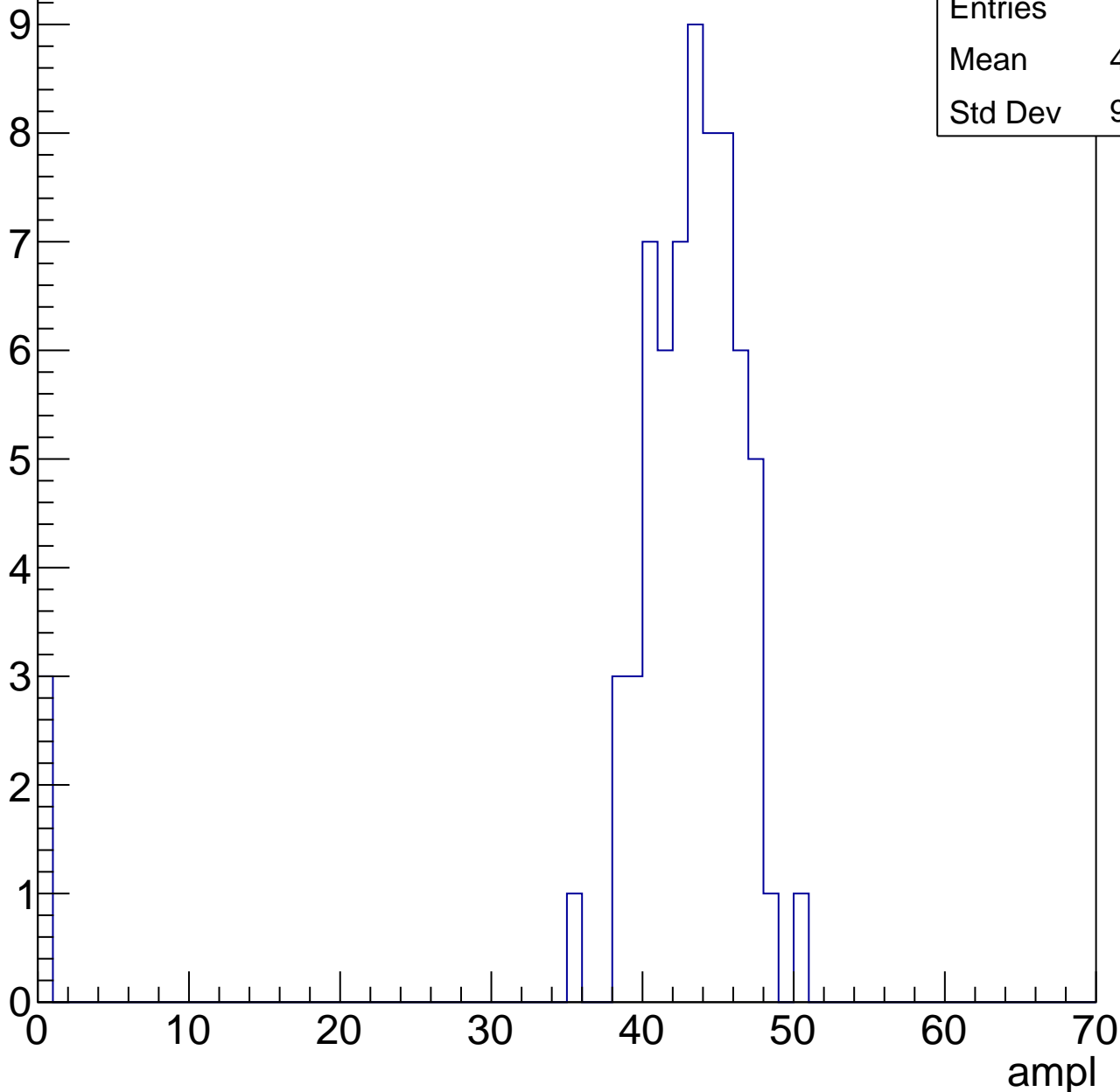


B1L103S, U9-ch28, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

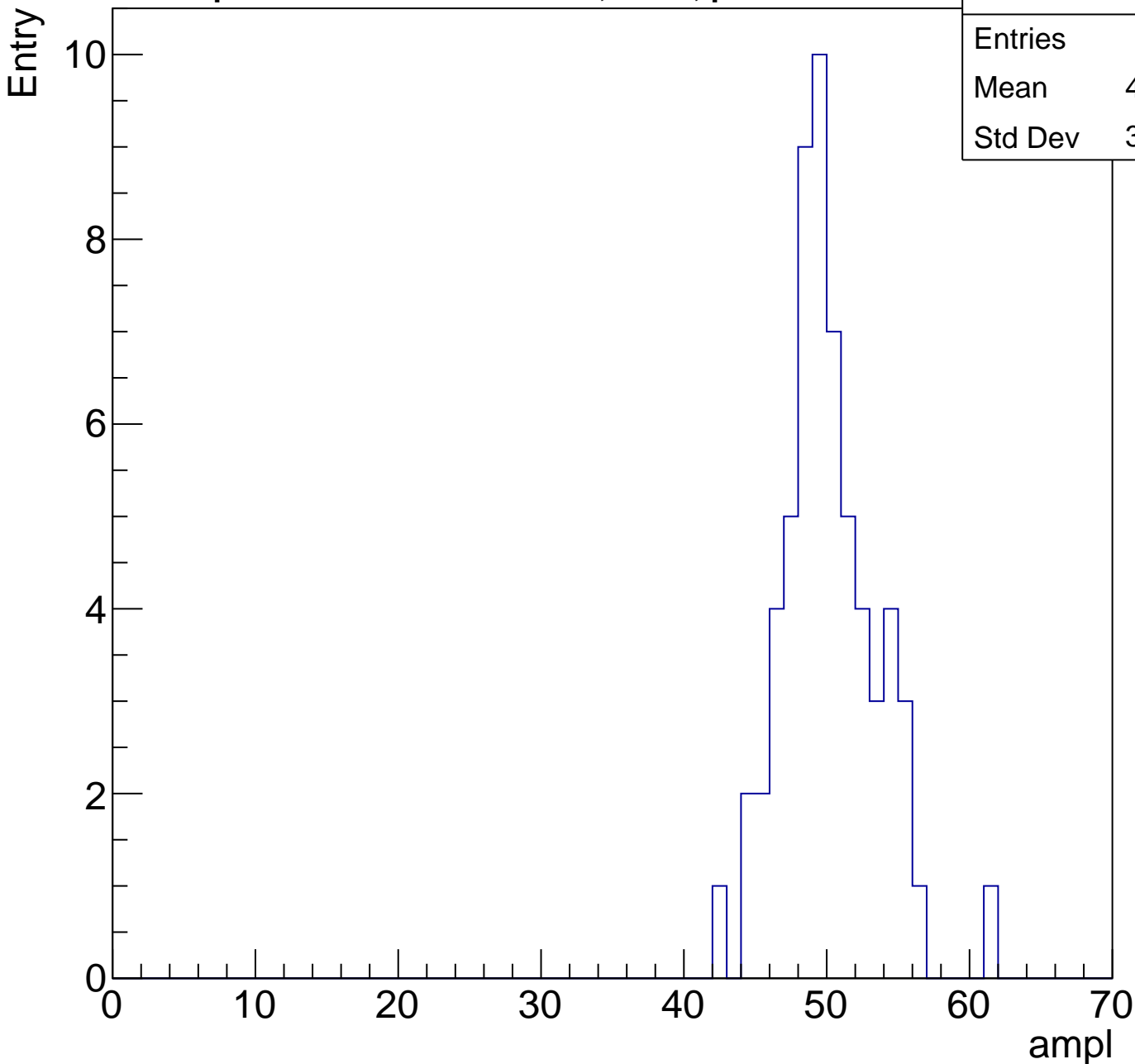
Entries	68
Mean	41.09
Std Dev	9.257



B1L103S, U9-ch28, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	61
Mean	49.69
Std Dev	3.337

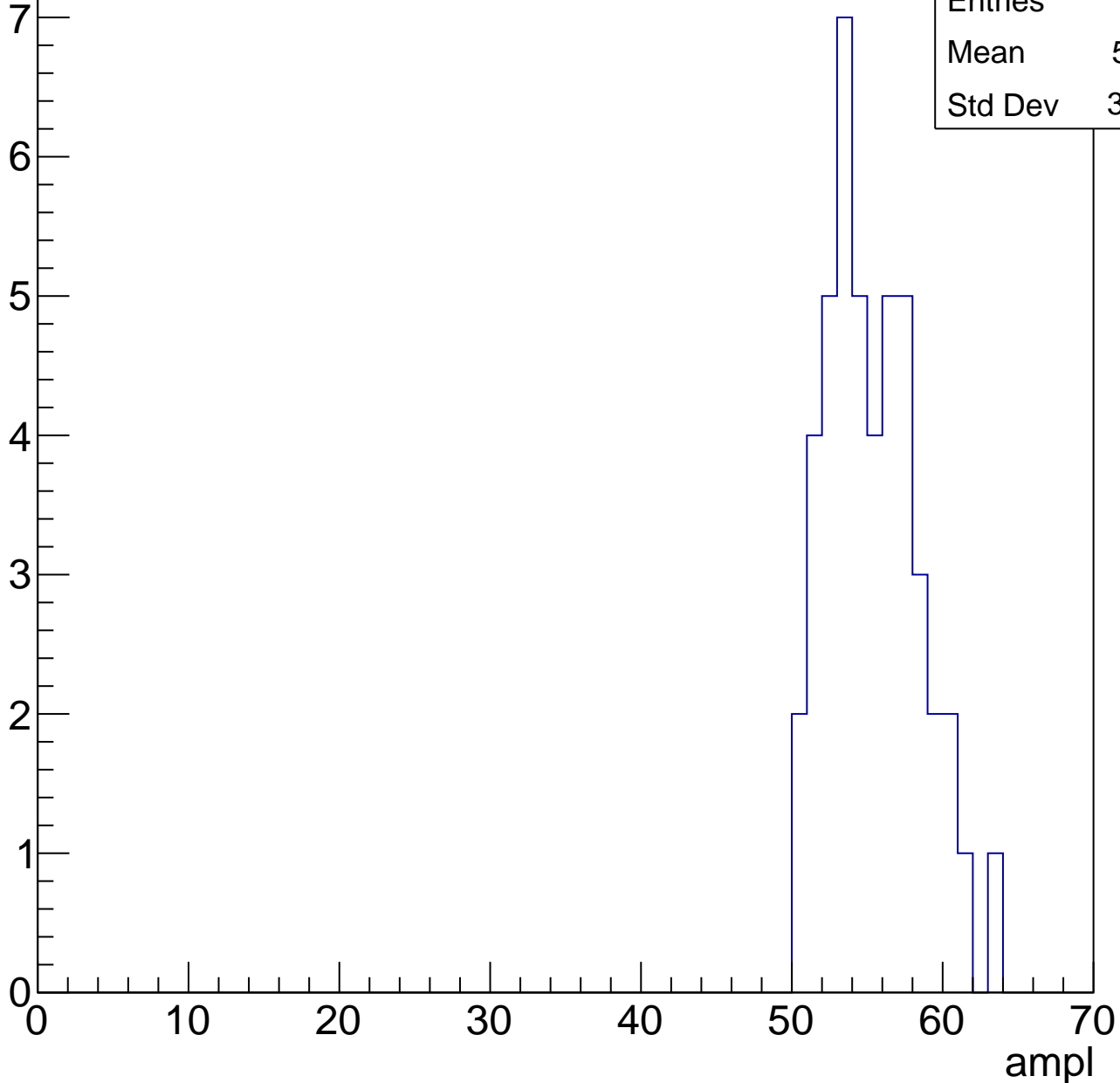


B1L103S, U9-ch28, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	46
Mean	54.91
Std Dev	3.042

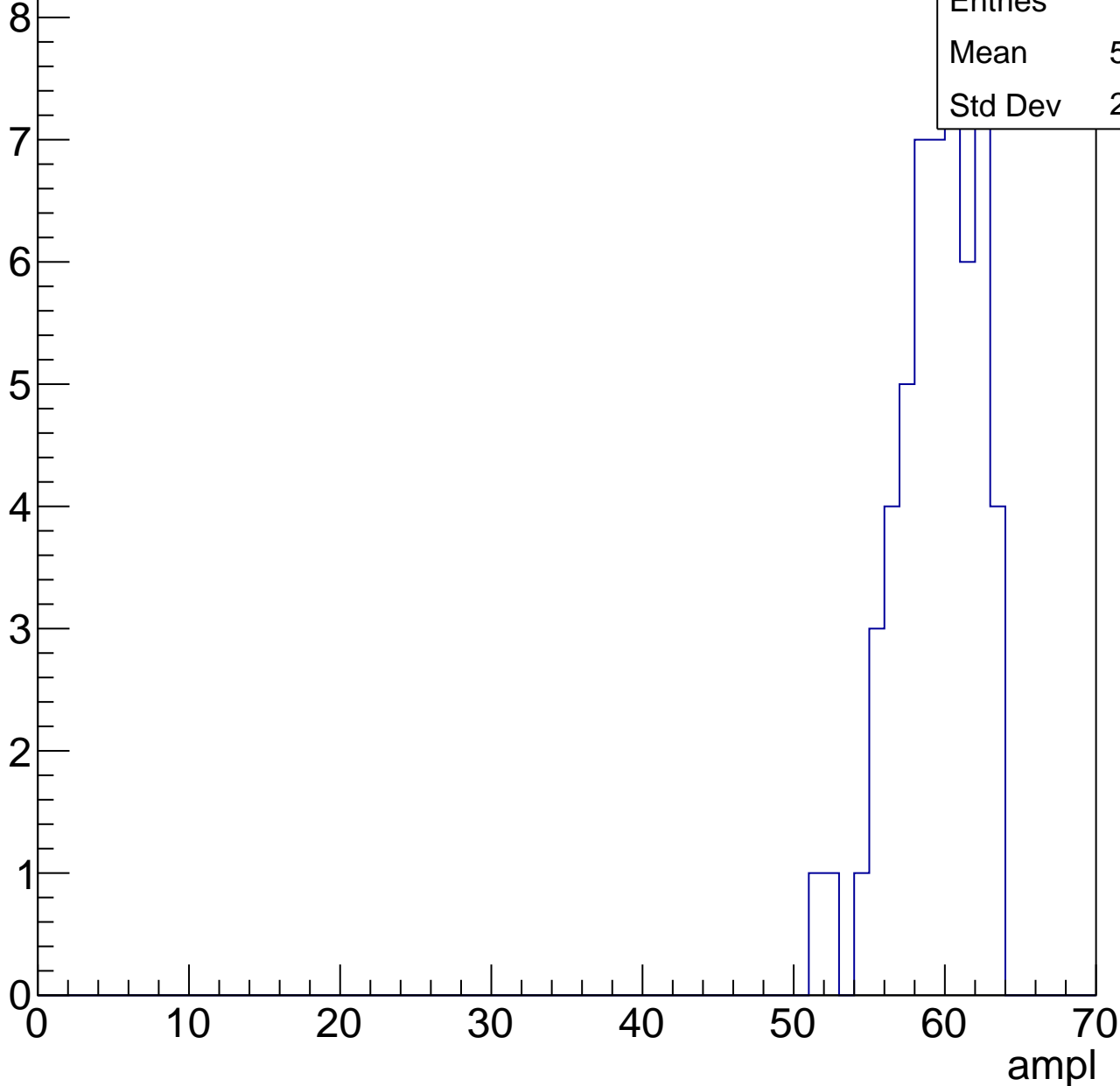


B1L103S, U9-ch28, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	58.98
Std Dev	2.753

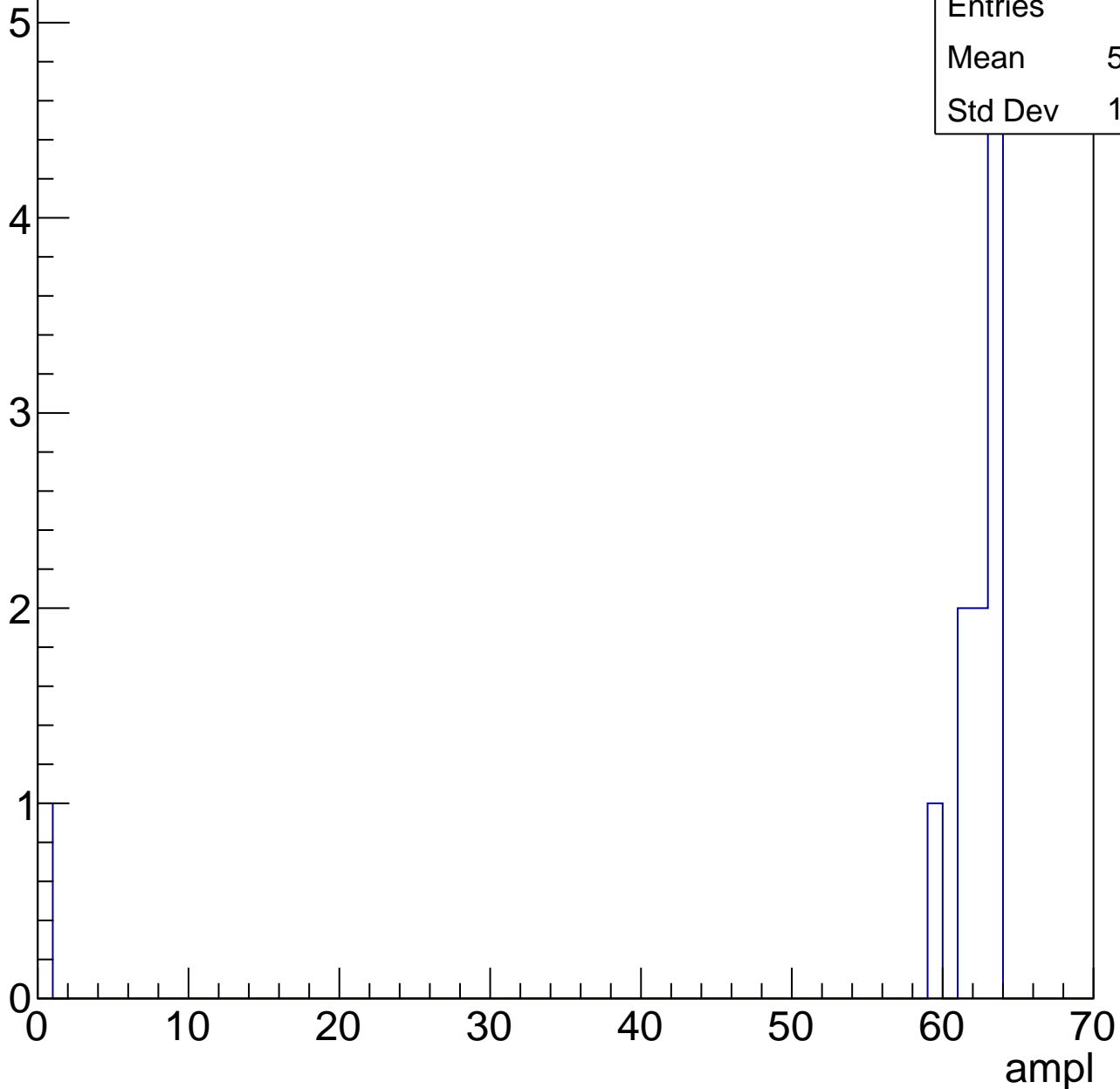


B1L103S, U9-ch28, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	11
Mean	56.36
Std Dev	17.86



B1L103S, U9-ch28, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

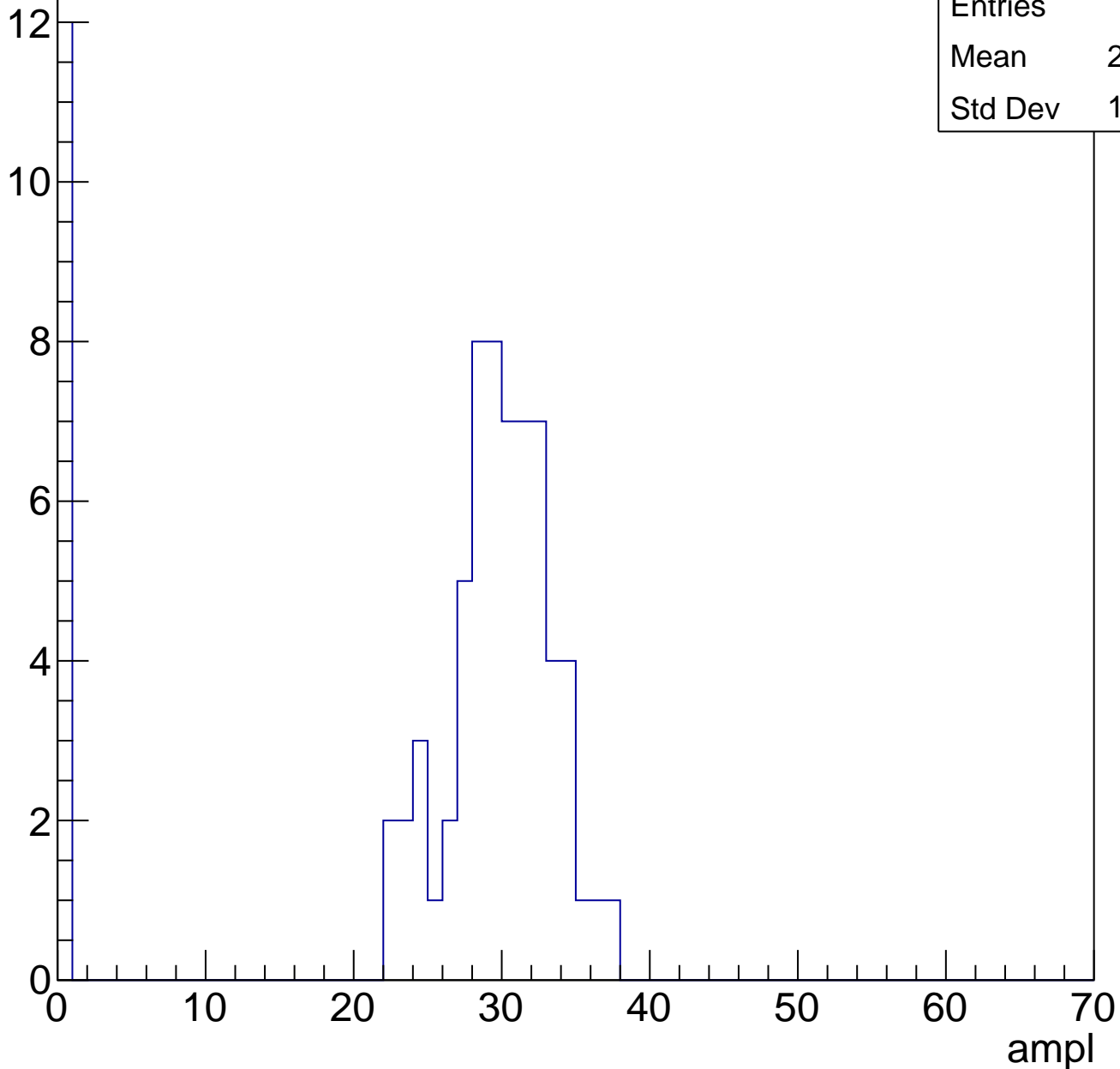
ampl

B1L103S, U9-ch29, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	24.76
Std Dev	11.23

Entry



B1L103S, U9-ch29, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	98
Mean	32.26
Std Dev	13.06

Entry

12

10

8

6

4

2

0

0

10

20

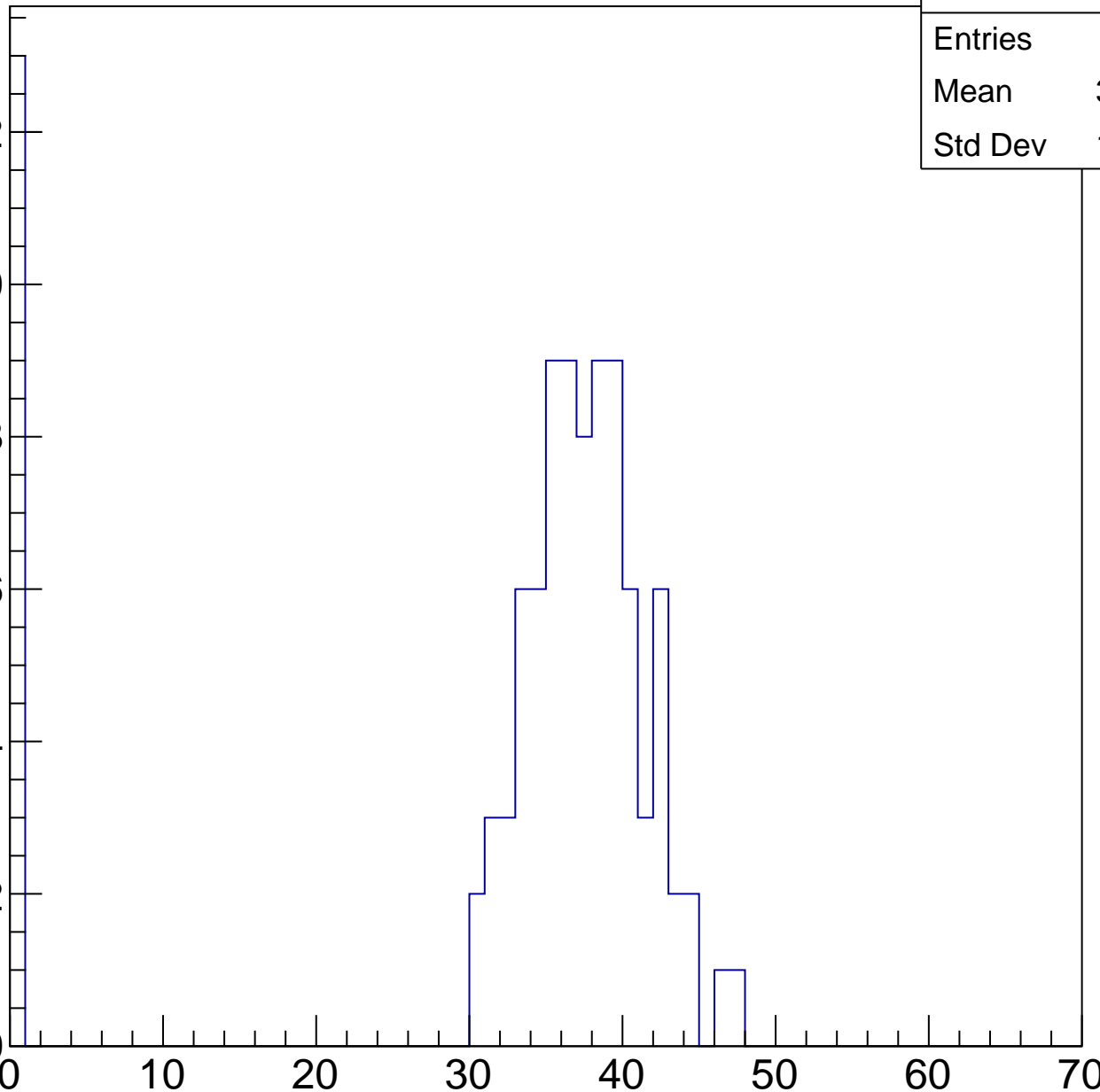
30

40

50

60

ampl

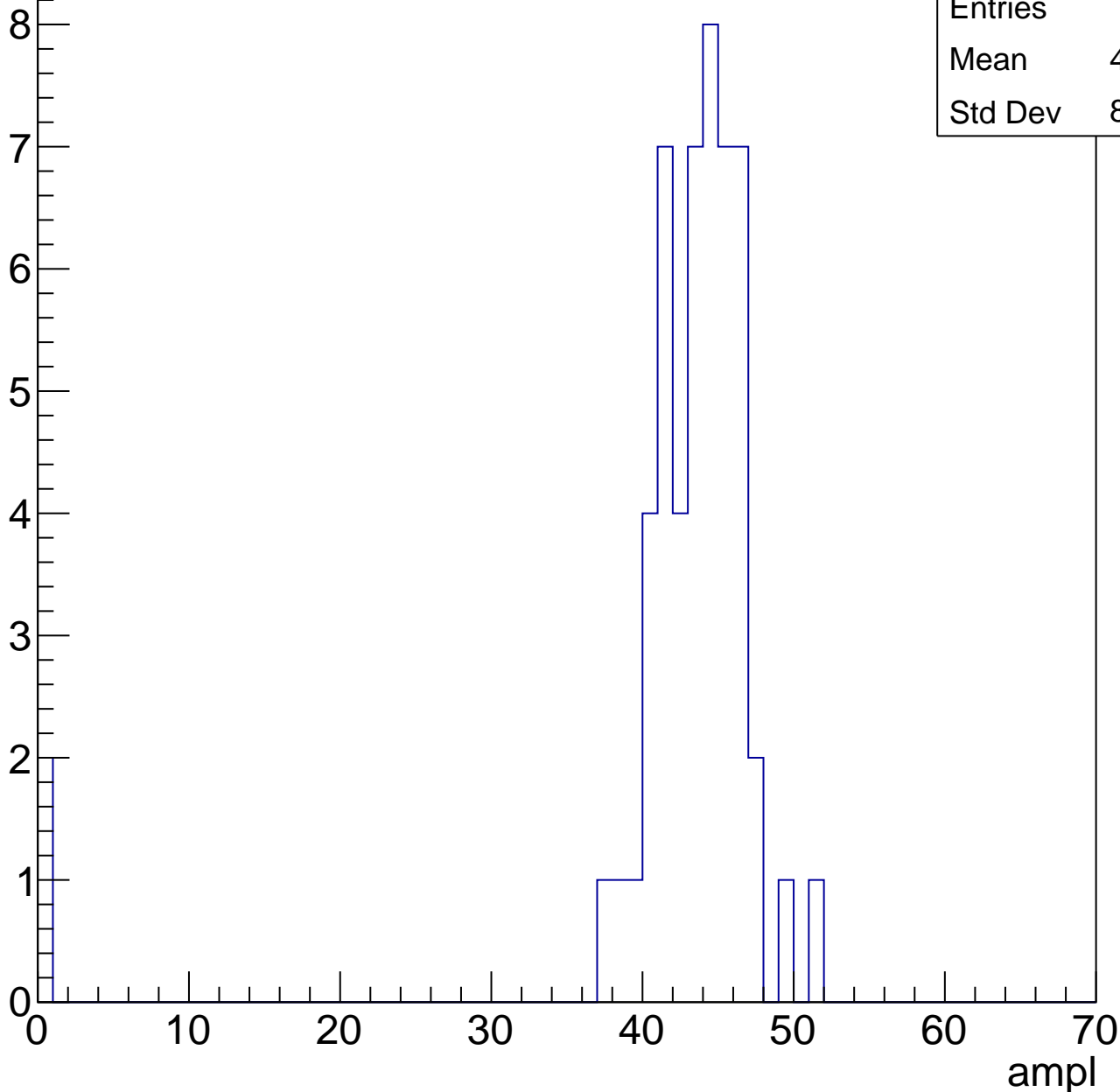


B1L103S, U9-ch29, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	41.75
Std Dev	8.679



B1L103S, U9-ch29, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	74
Mean	50.14
Std Dev	2.905

Entry

10

8

6

4

2

0

0

10

20

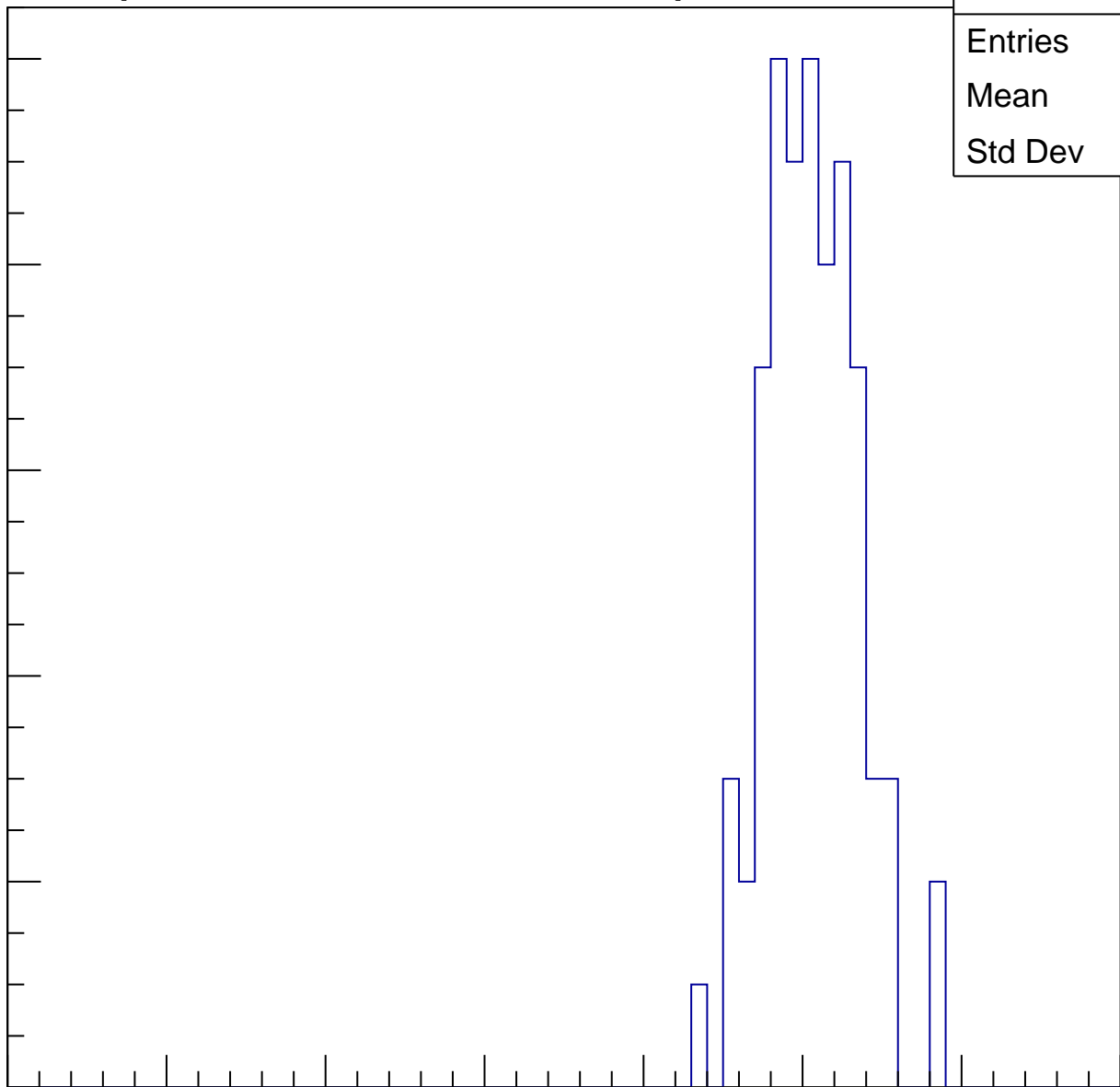
30

40

50

60

ampl



B1L103S, U9-ch29, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

8

6

4

2

0

0

10

20

30

40

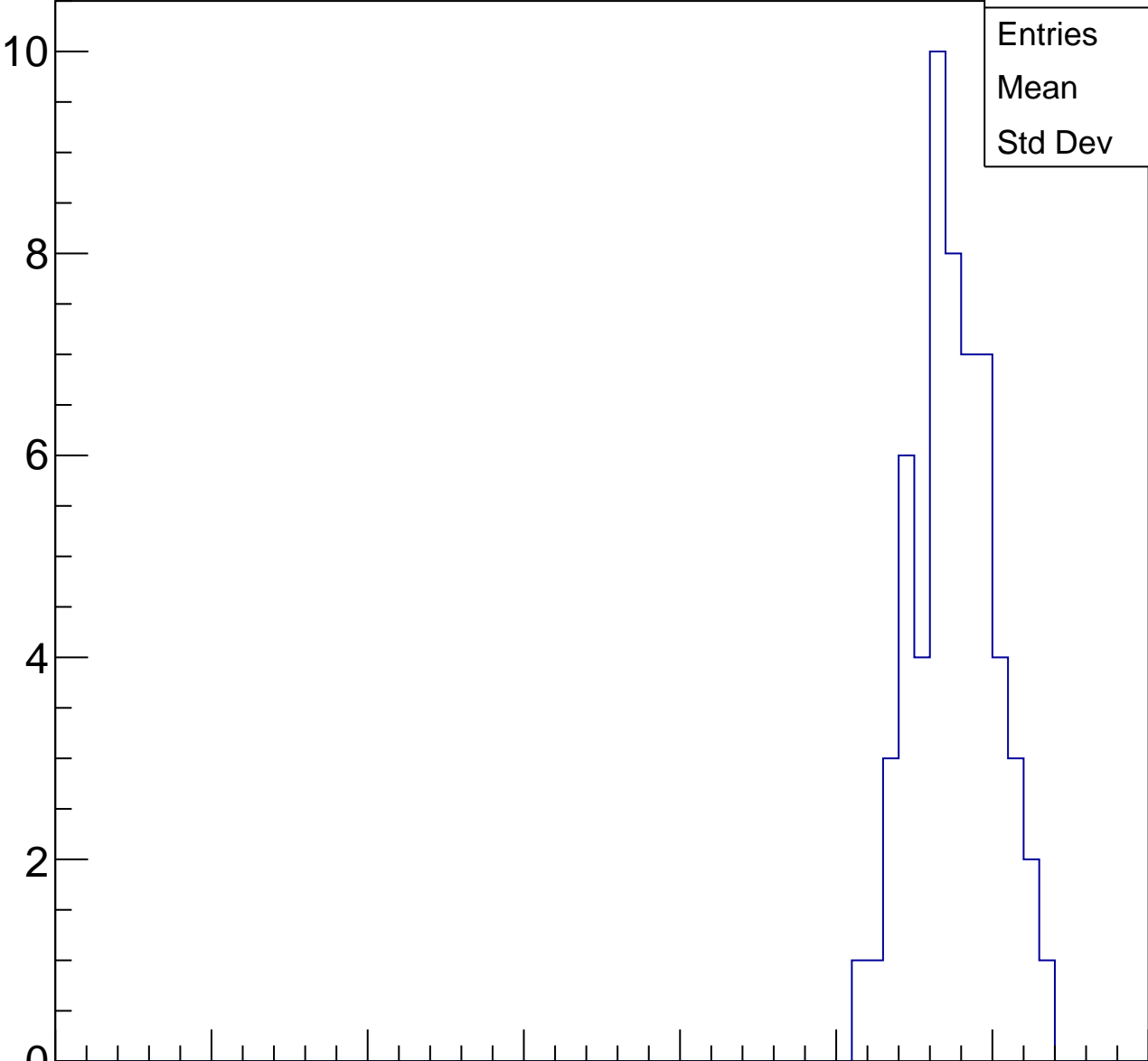
50

60

70

ampl

Entries	57
Mean	57.04
Std Dev	2.629

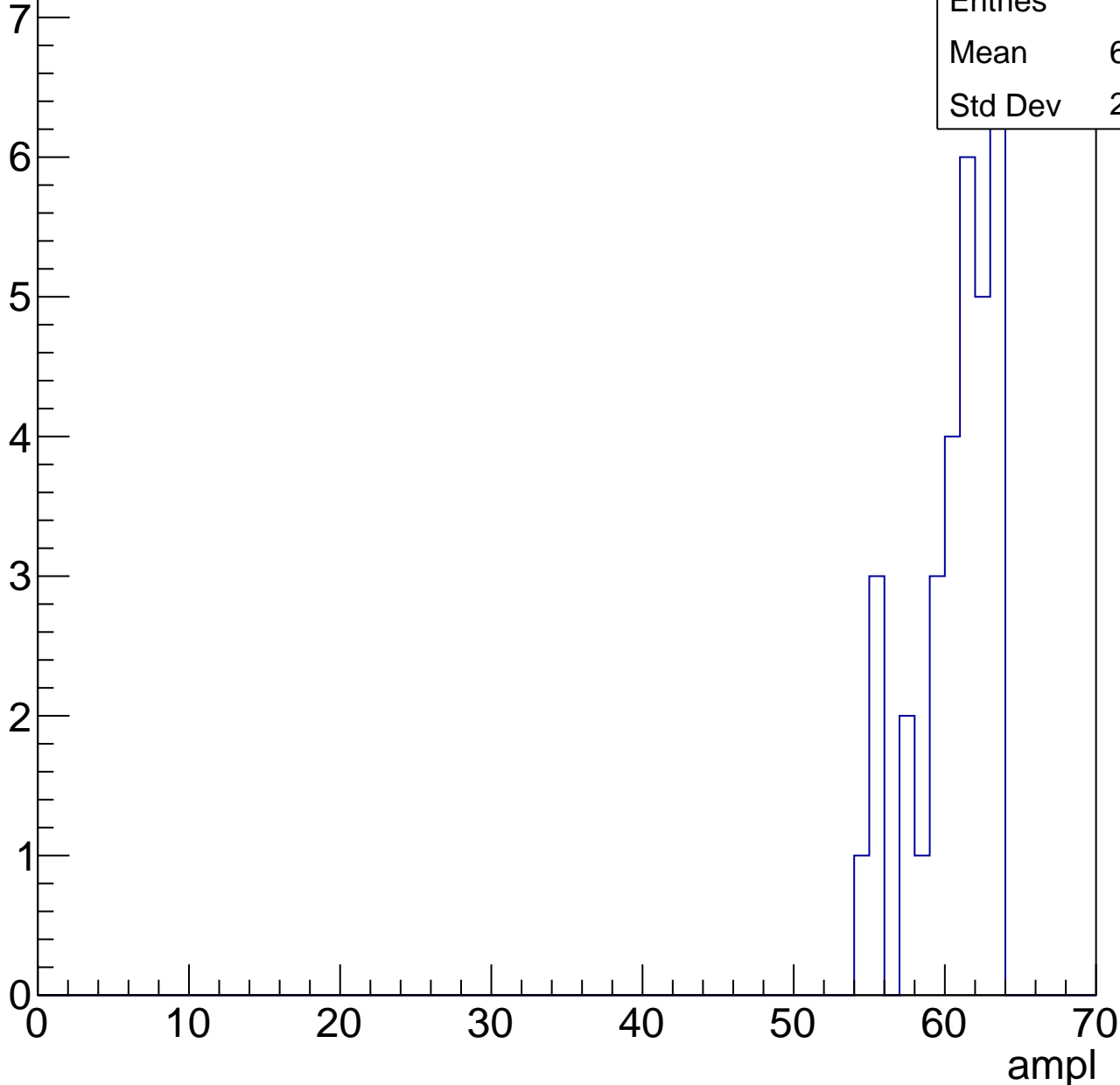


B1L103S, U9-ch29, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

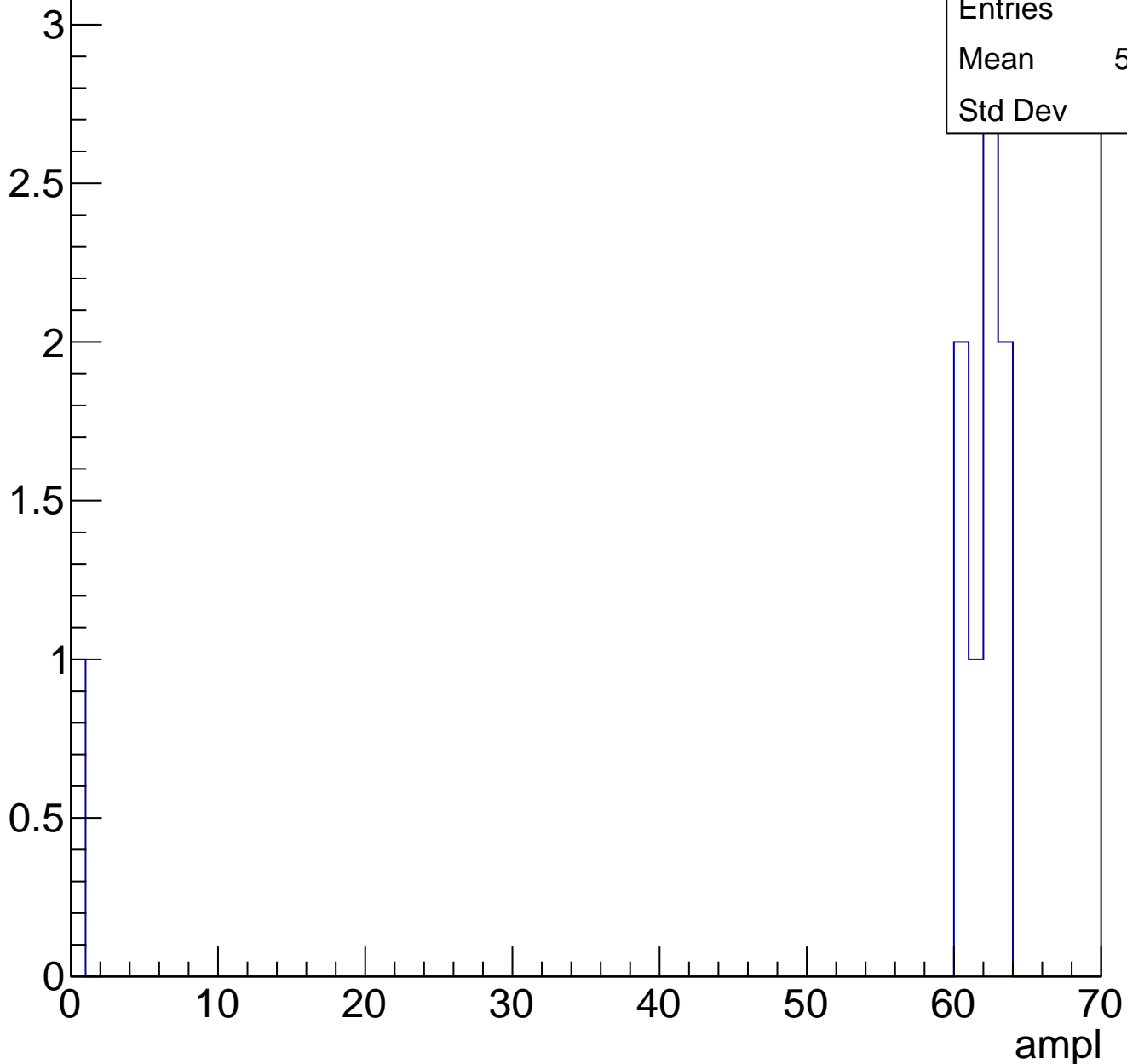
Entries	32
Mean	60.16
Std Dev	2.647



B1L103S, U9-ch29, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch29, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



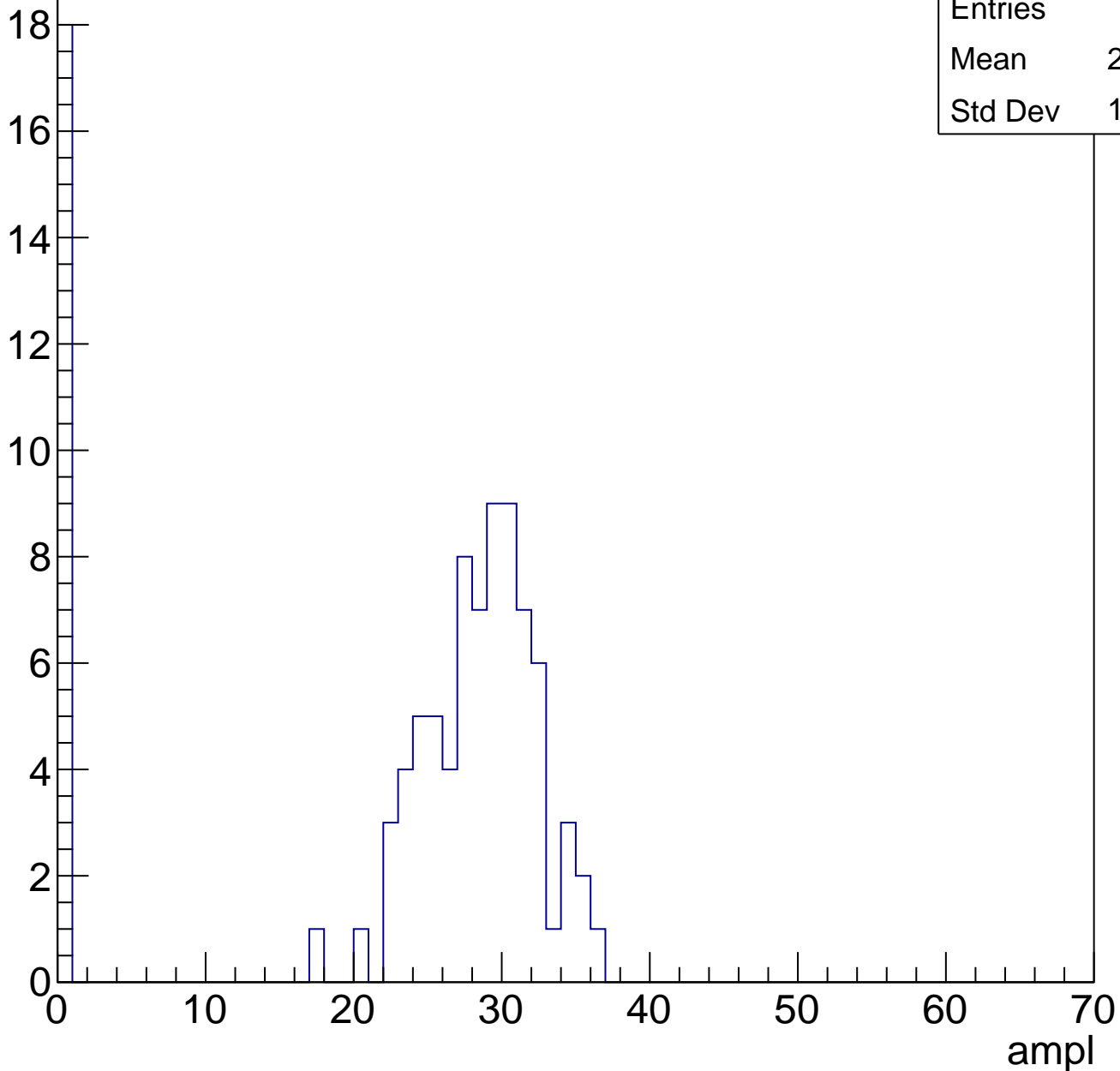
Entries	19
Mean	0
Std Dev	0

B1L103S, U9-ch30, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	94
Mean	22.73
Std Dev	11.55

Entry

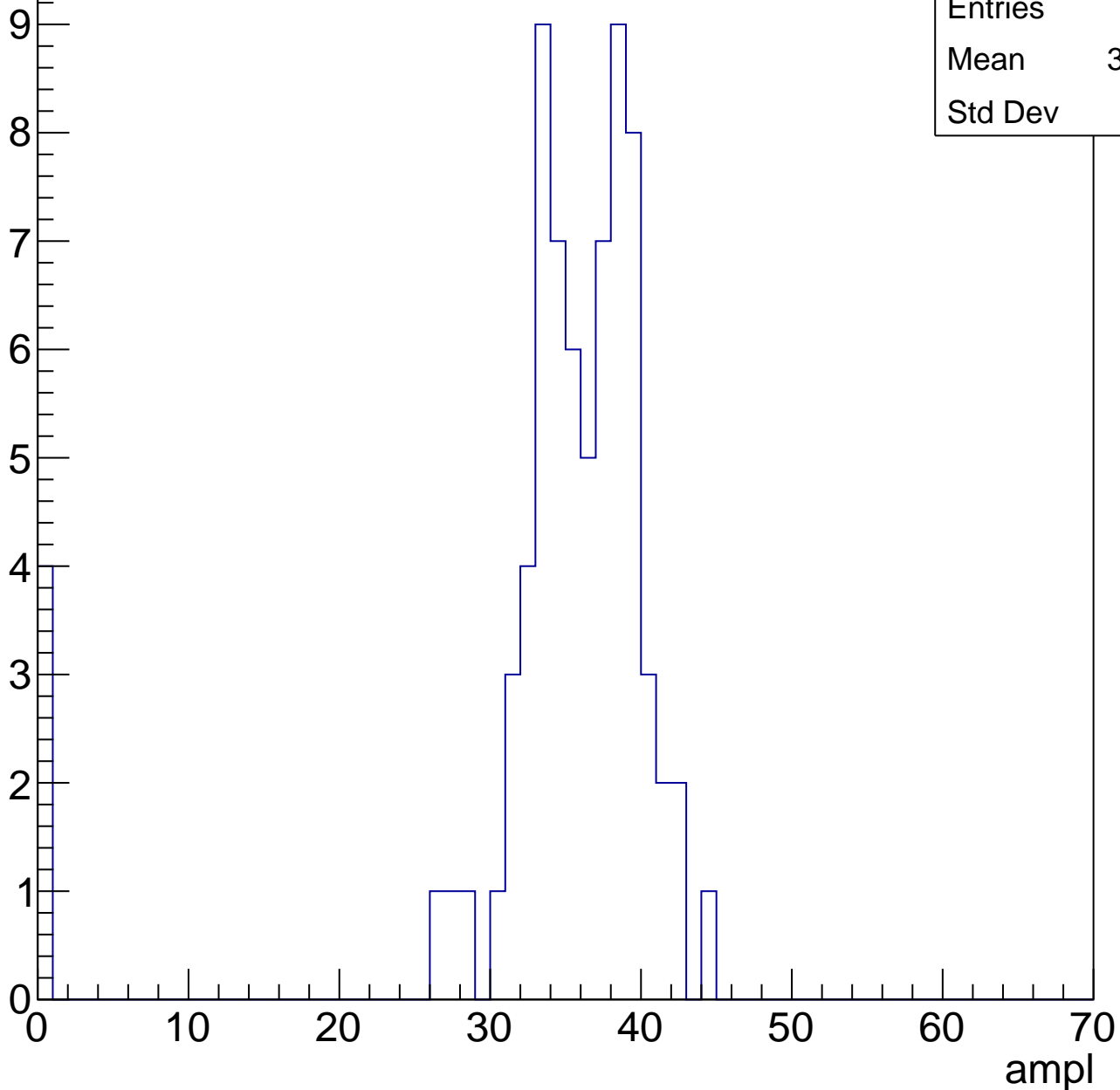


B1L103S, U9-ch30, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	33.78
Std Dev	8.78

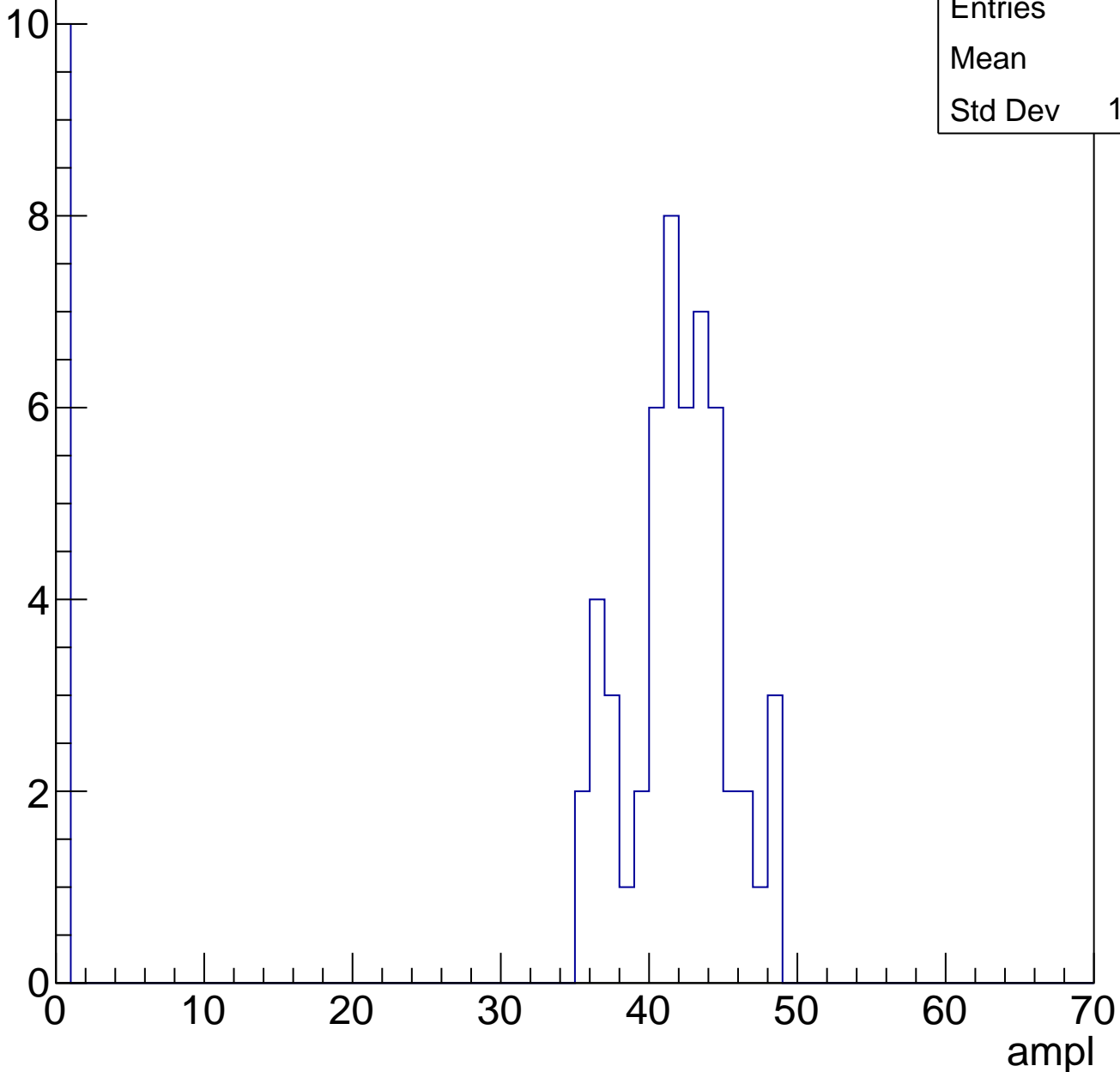


B1L103S, U9-ch30, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	63
Mean	34.9
Std Dev	15.46

Entry

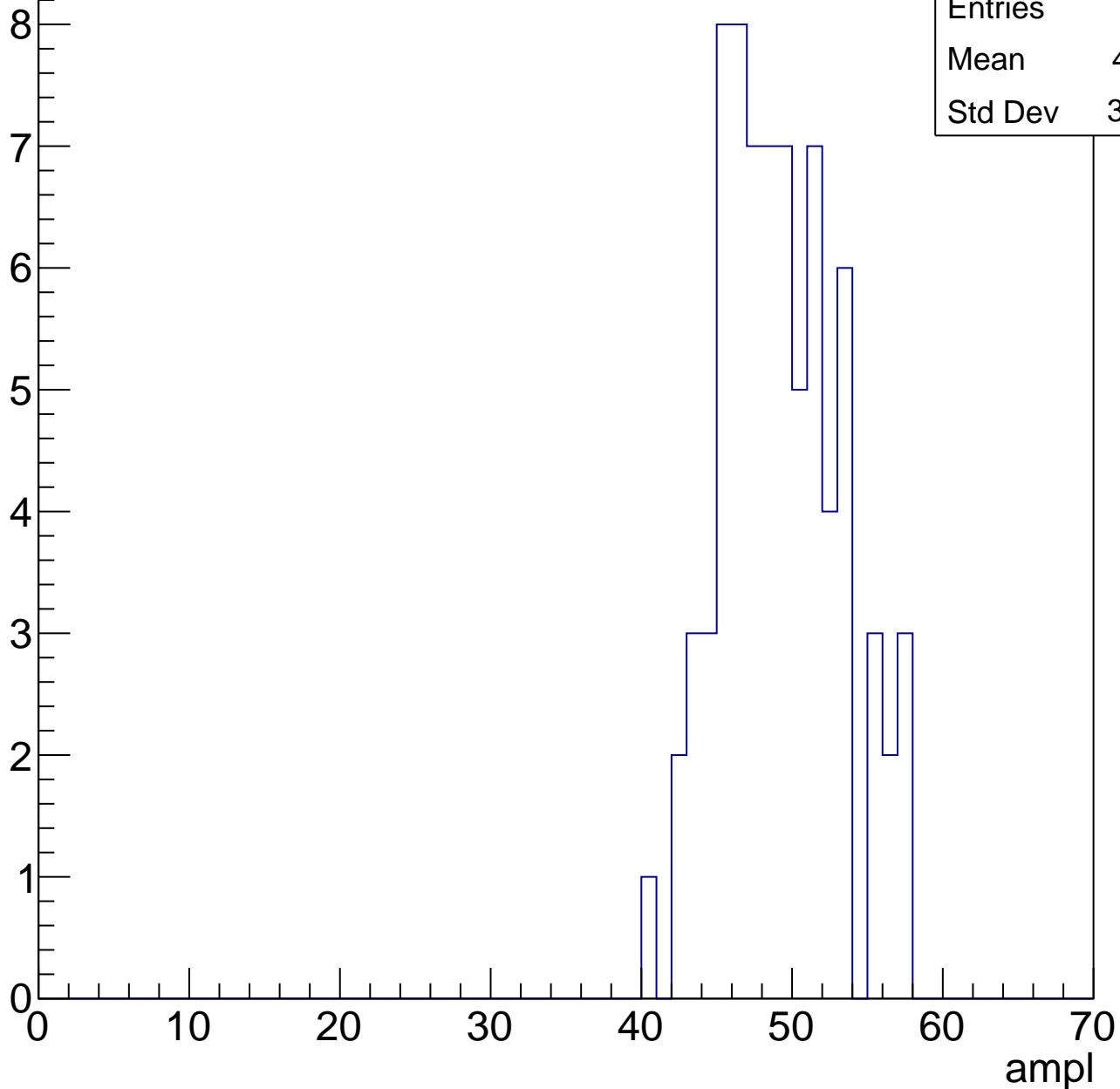


B1L103S, U9-ch30, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	48.71
Std Dev	3.896

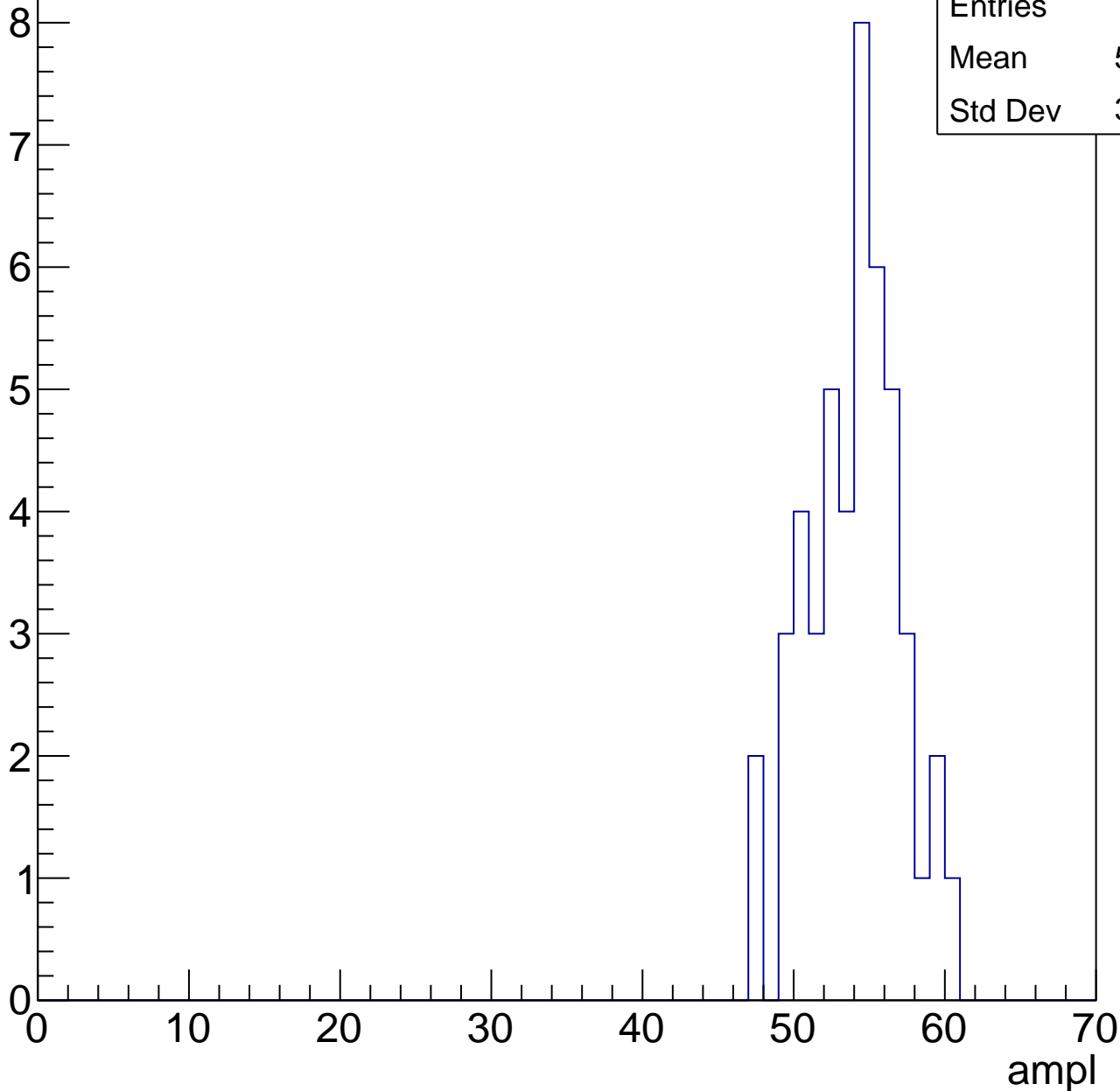


B1L103S, U9-ch30, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	47
Mean	53.51
Std Dev	3.031

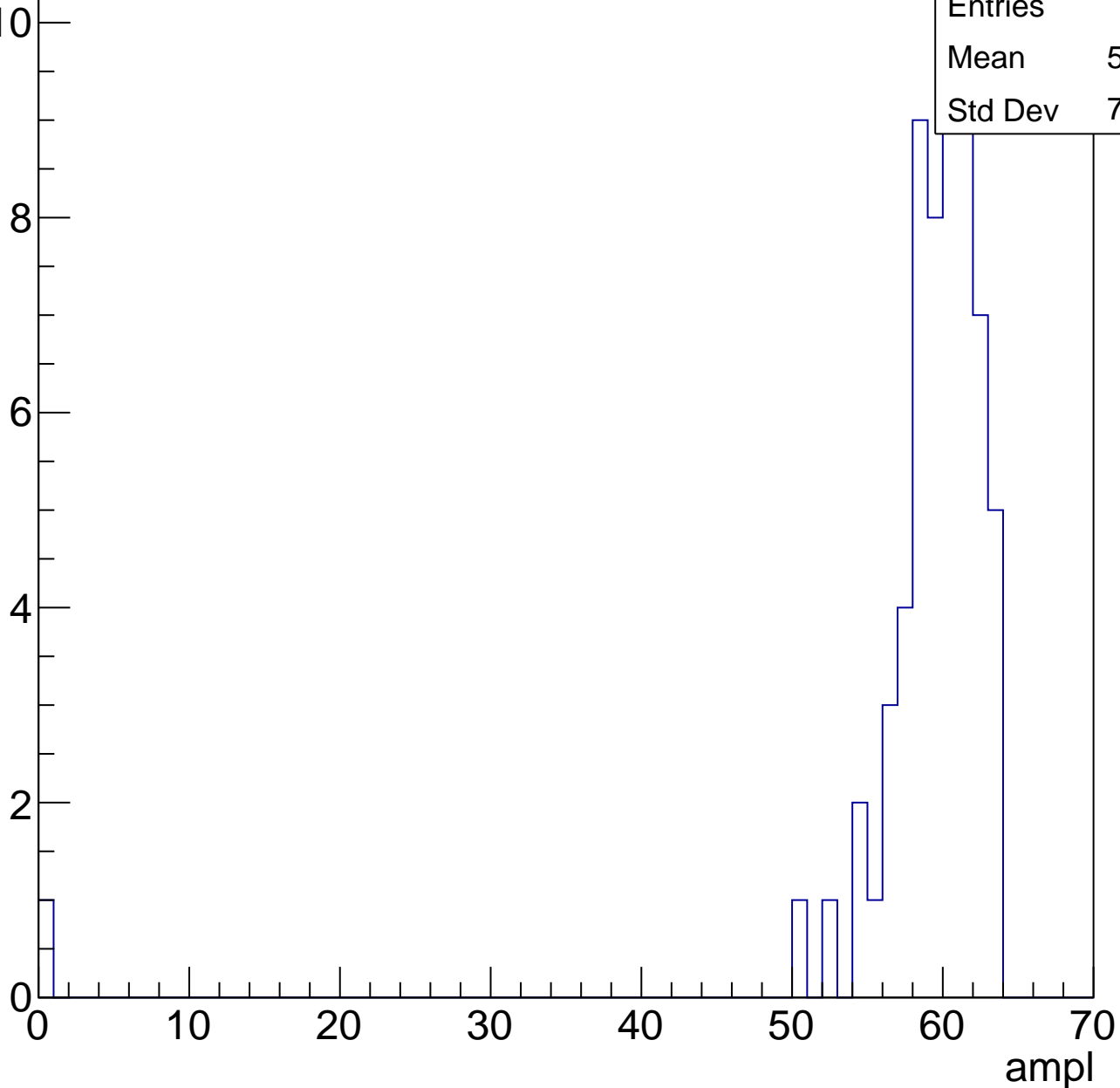


B1L103S, U9-ch30, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	58.26
Std Dev	7.983

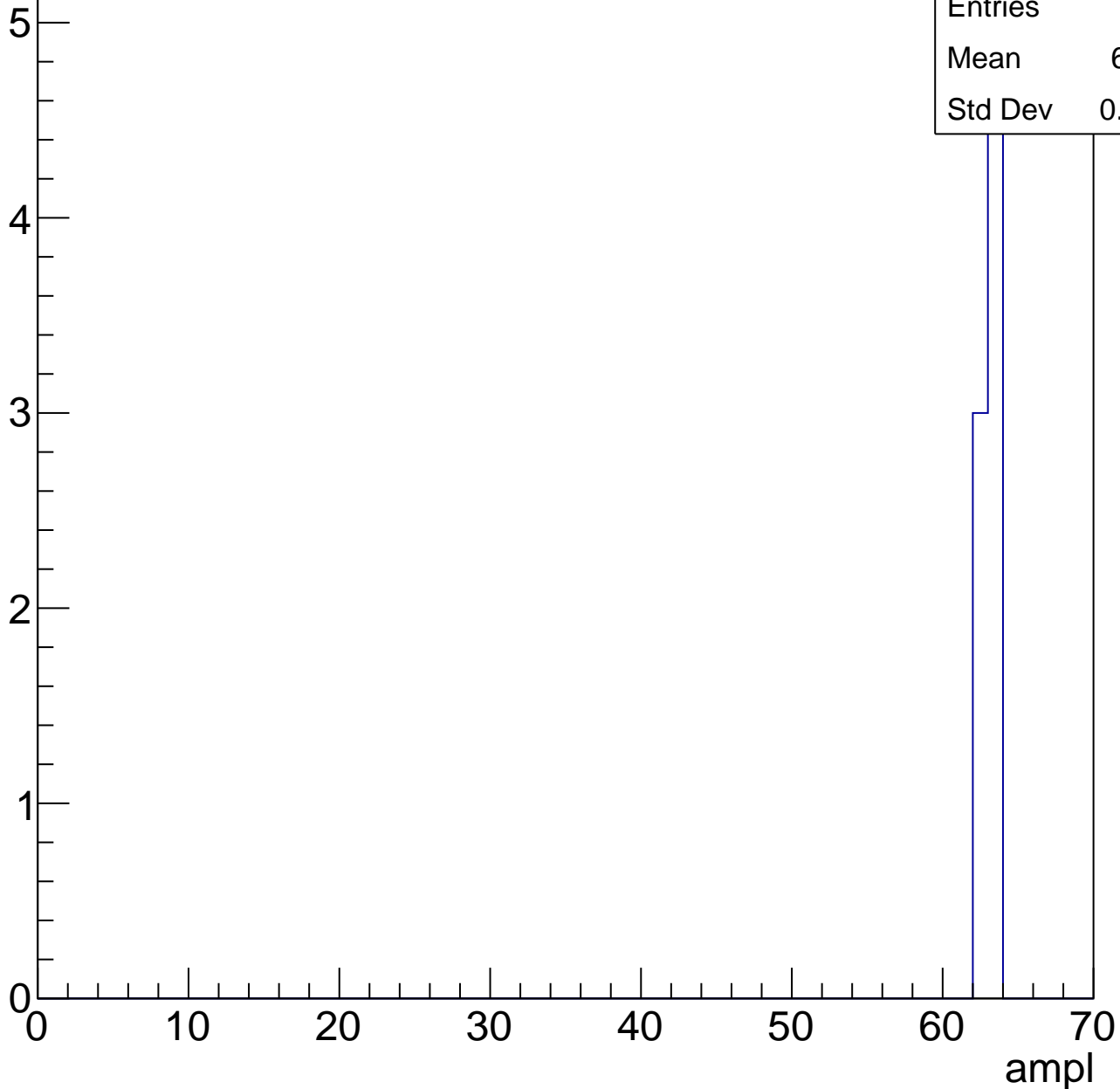


B1L103S, U9-ch30, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	8
Mean	62.62
Std Dev	0.4841



B1L103S, U9-ch30, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

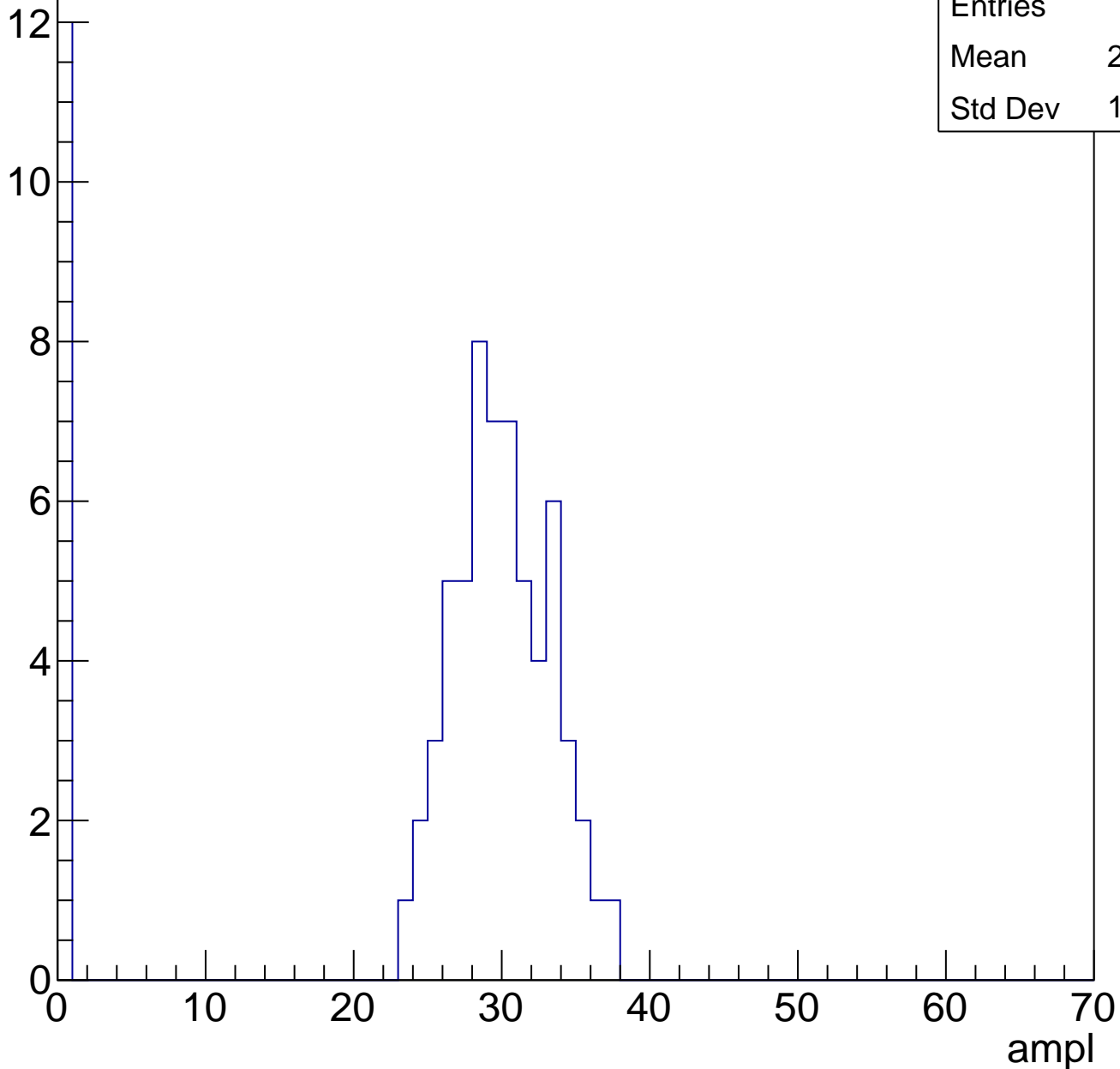
ampl

B1L103S, U9-ch31, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	72
Mean	24.64
Std Dev	11.39

Entry

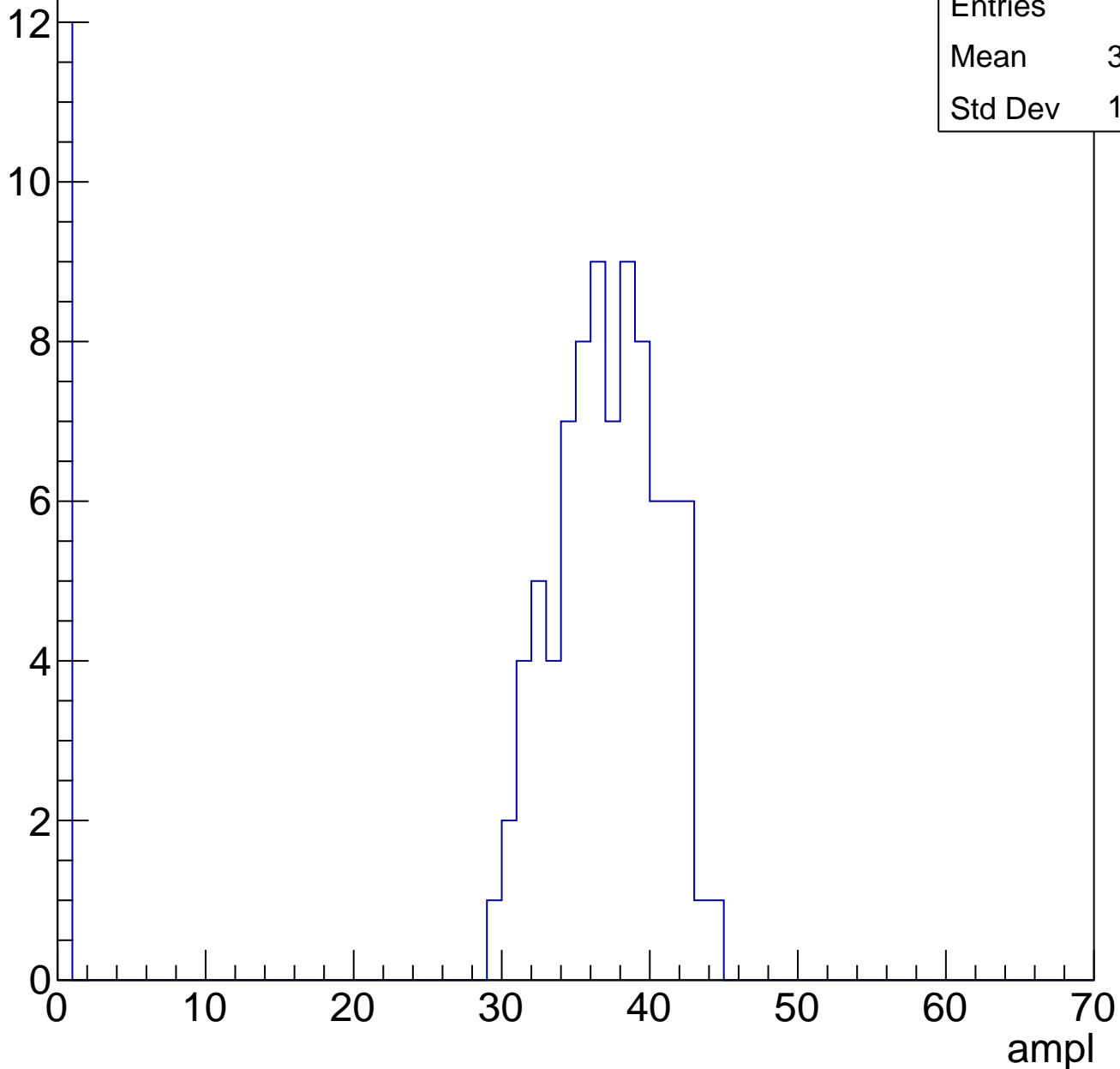


B1L103S, U9-ch31, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	96
Mean	32.14
Std Dev	12.58

Entry

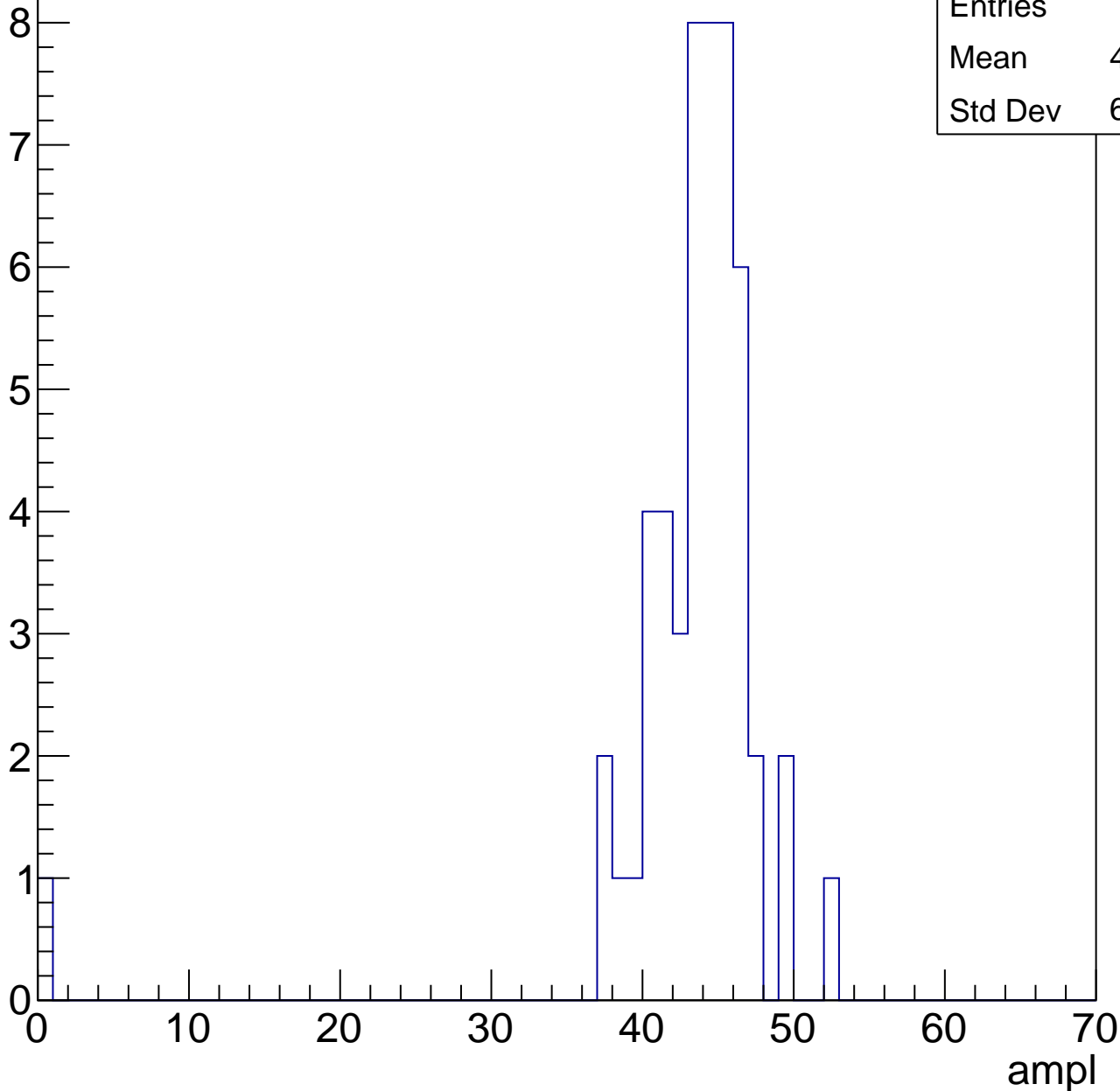


B1L103S, U9-ch31, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

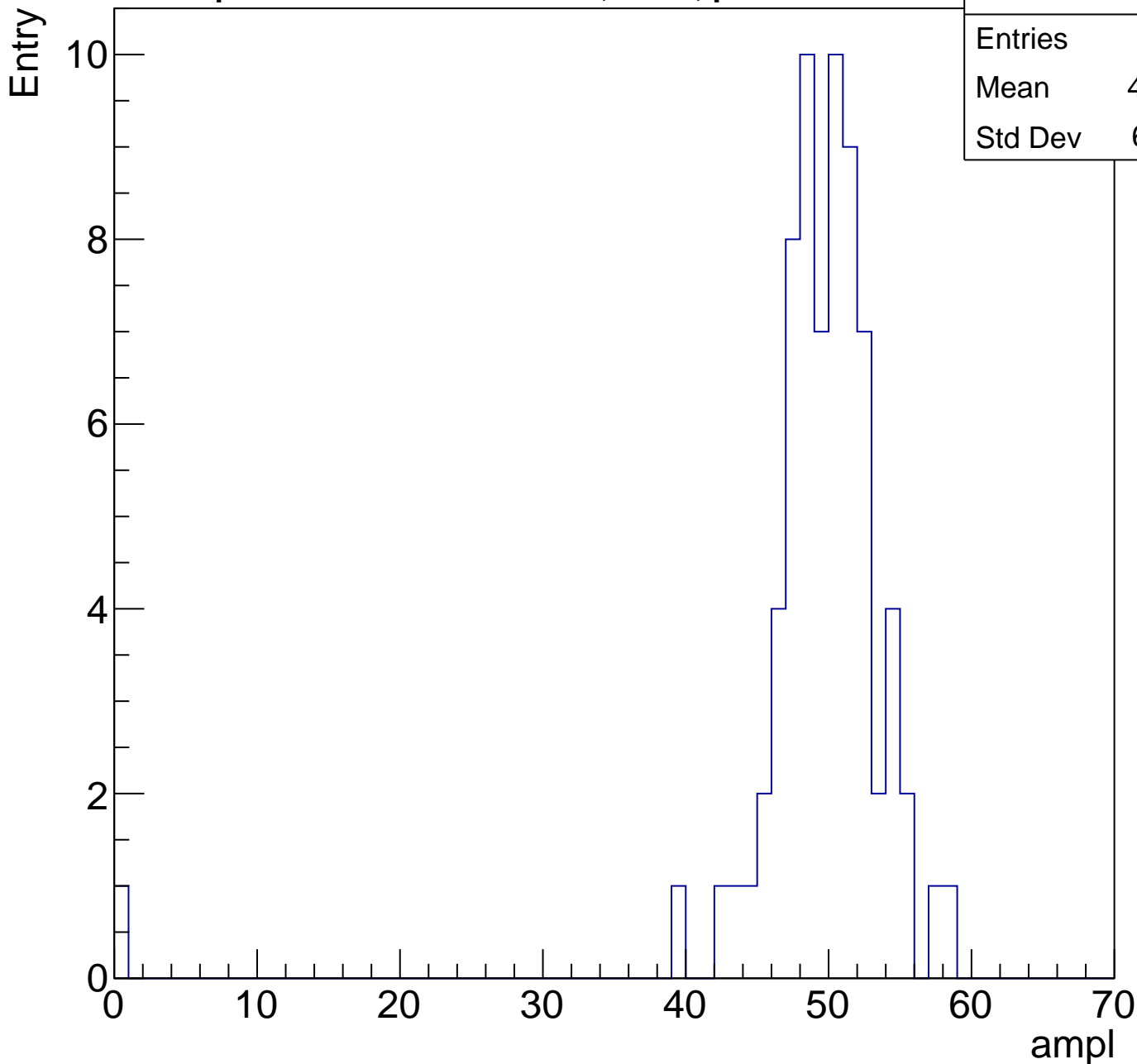
Entries	51
Mean	42.69
Std Dev	6.702



B1L103S, U9-ch31, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	72
Mean	48.76
Std Dev	6.641

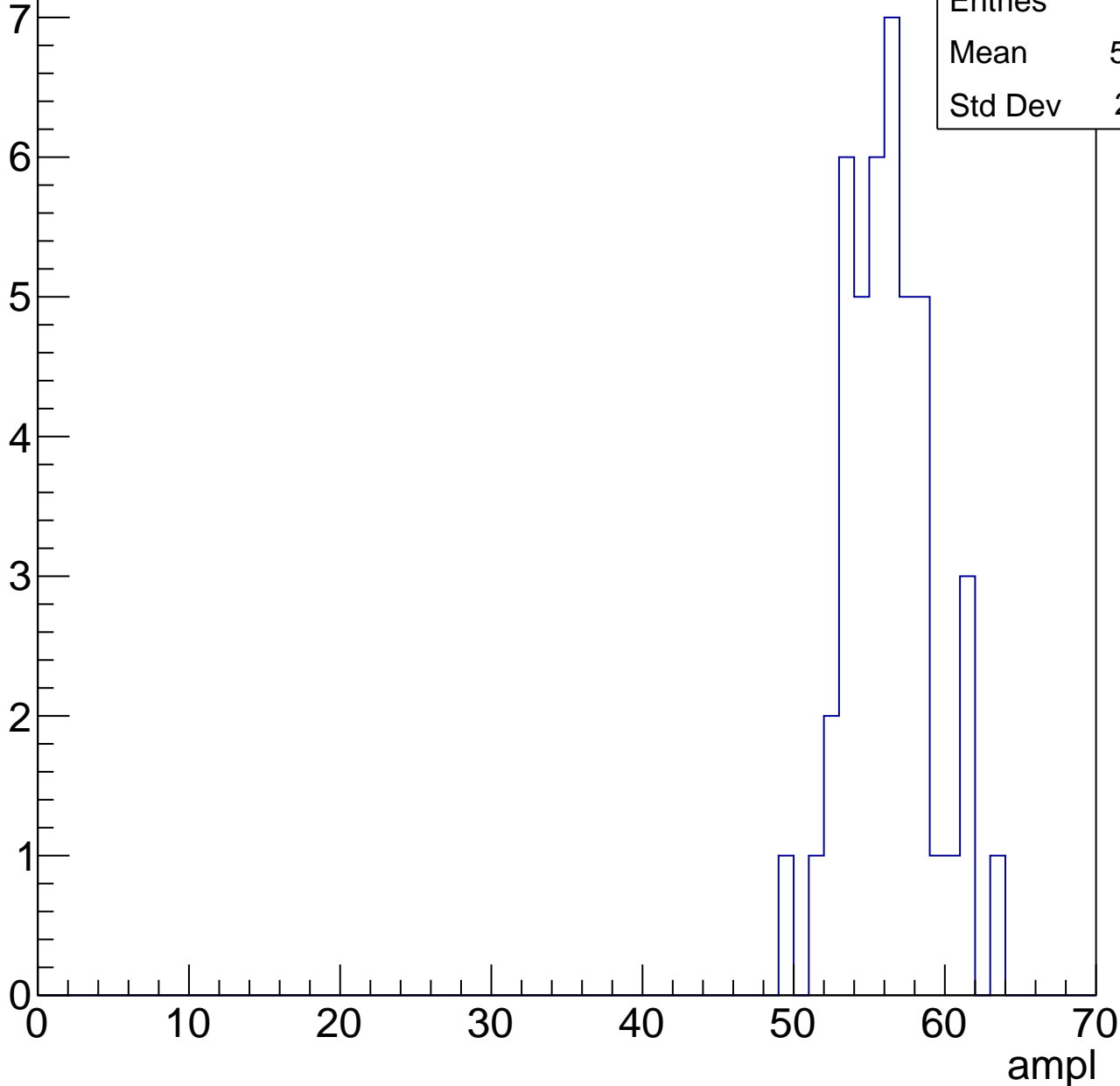


B1L103S, U9-ch31, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	44
Mean	55.77
Std Dev	2.851



B1L103S, U9-ch31, adc5

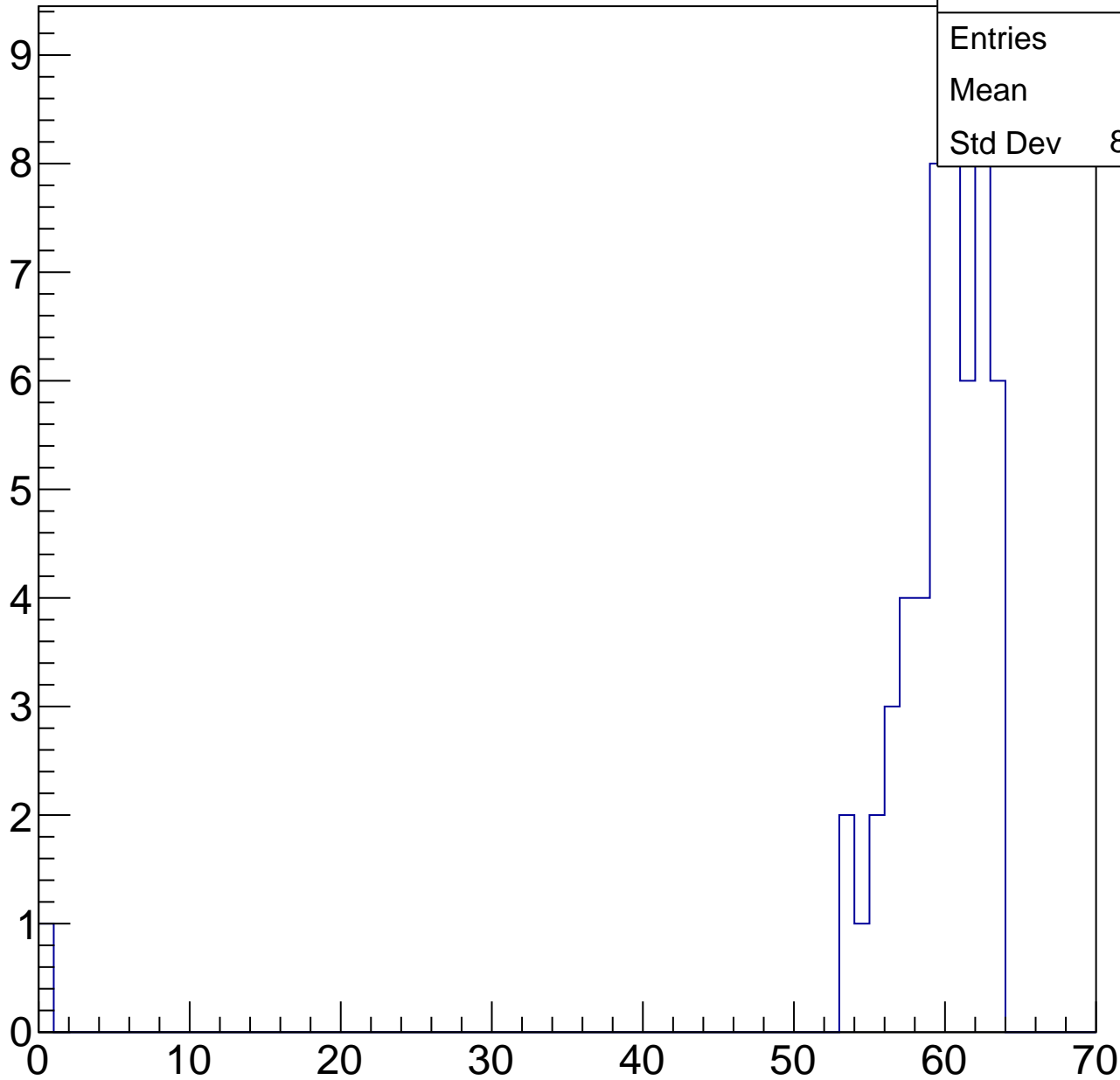
calib_packv5_041523_1651.root, FC#0, port C2

Entry

9
8
7
6
5
4
3
2
1
0

Entries	55
Mean	58.4
Std Dev	8.364

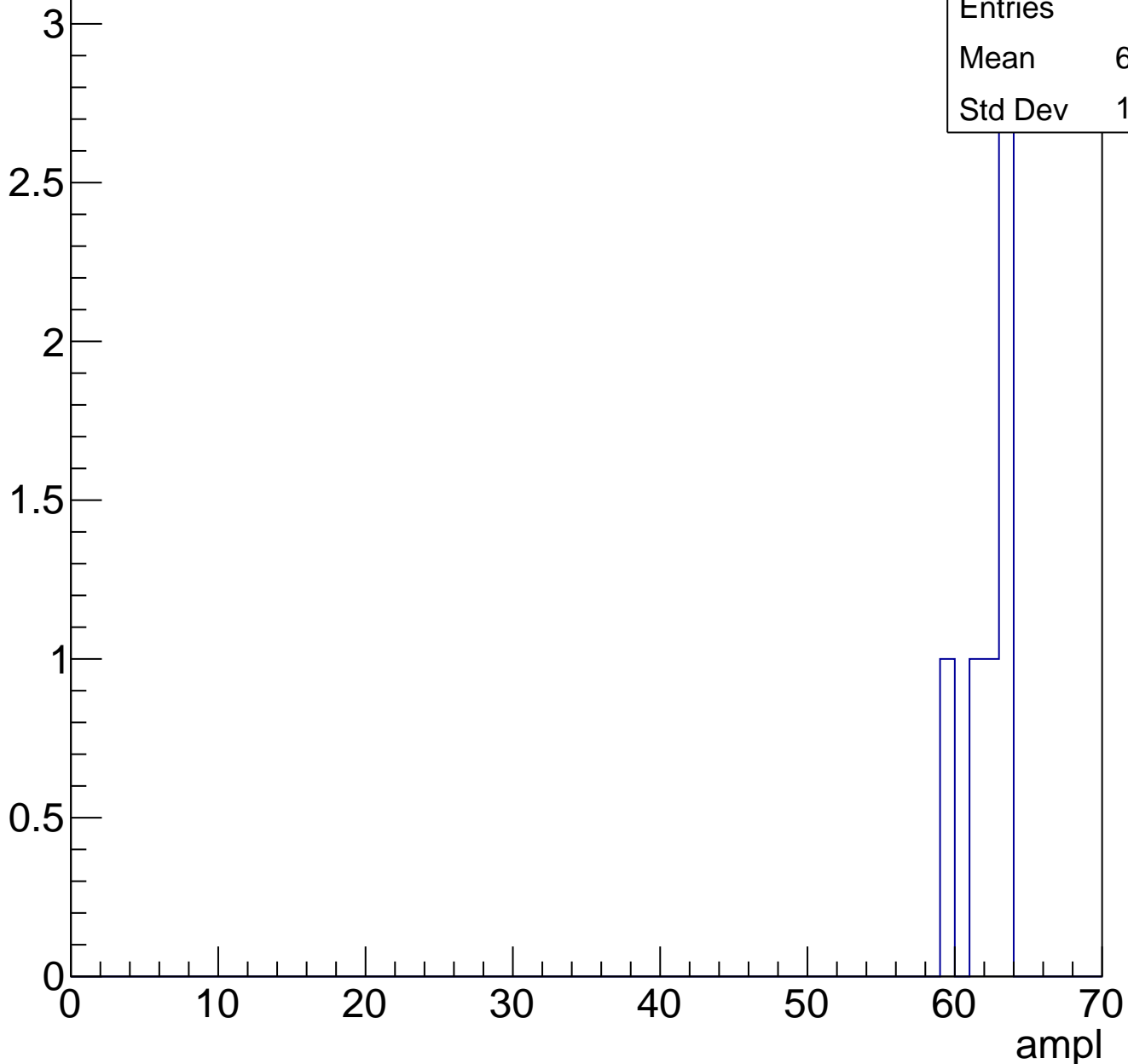
ampl



B1L103S, U9-ch31, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

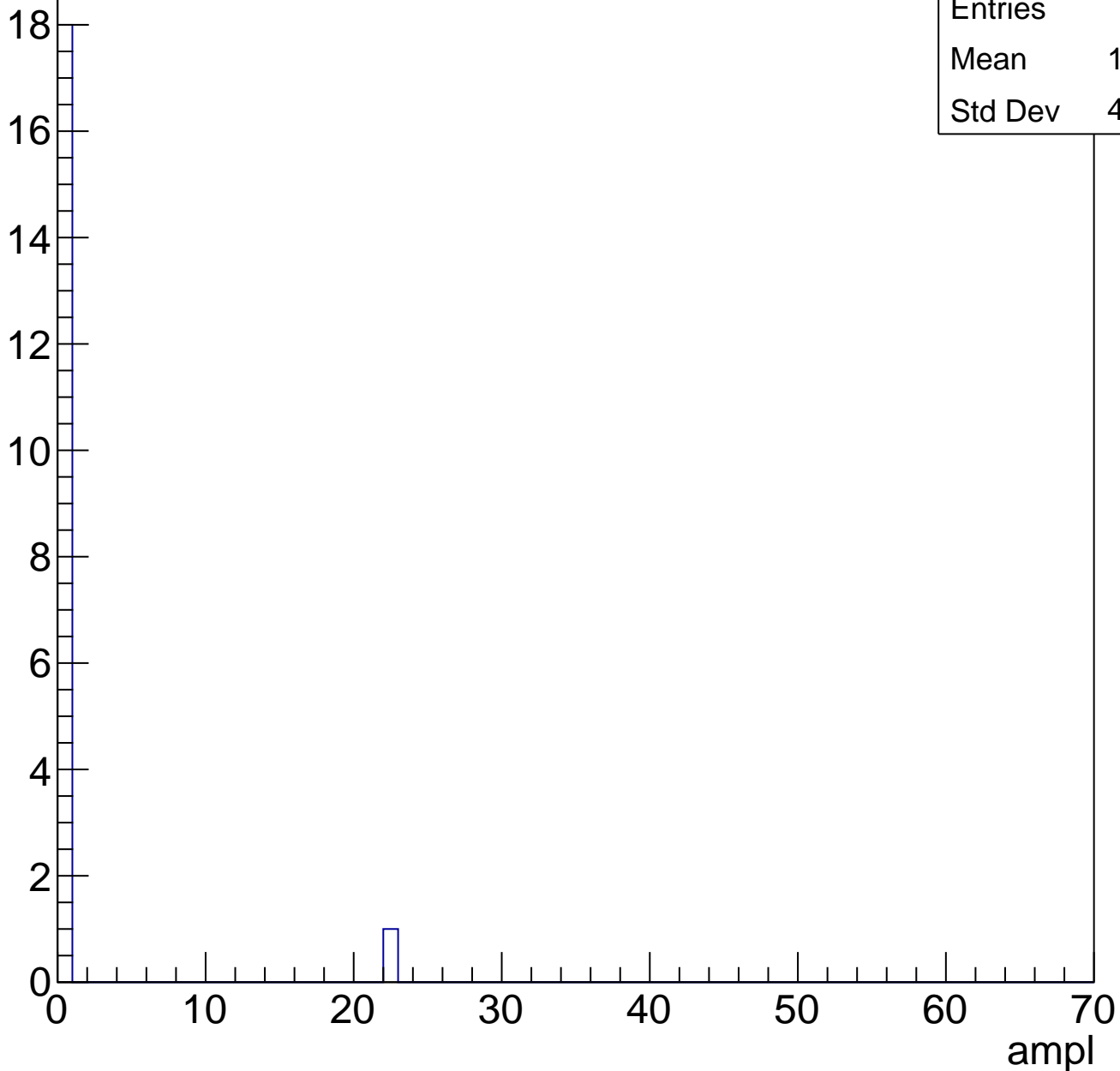


Entries	6
Mean	61.83
Std Dev	1.462

B1L103S, U9-ch31, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



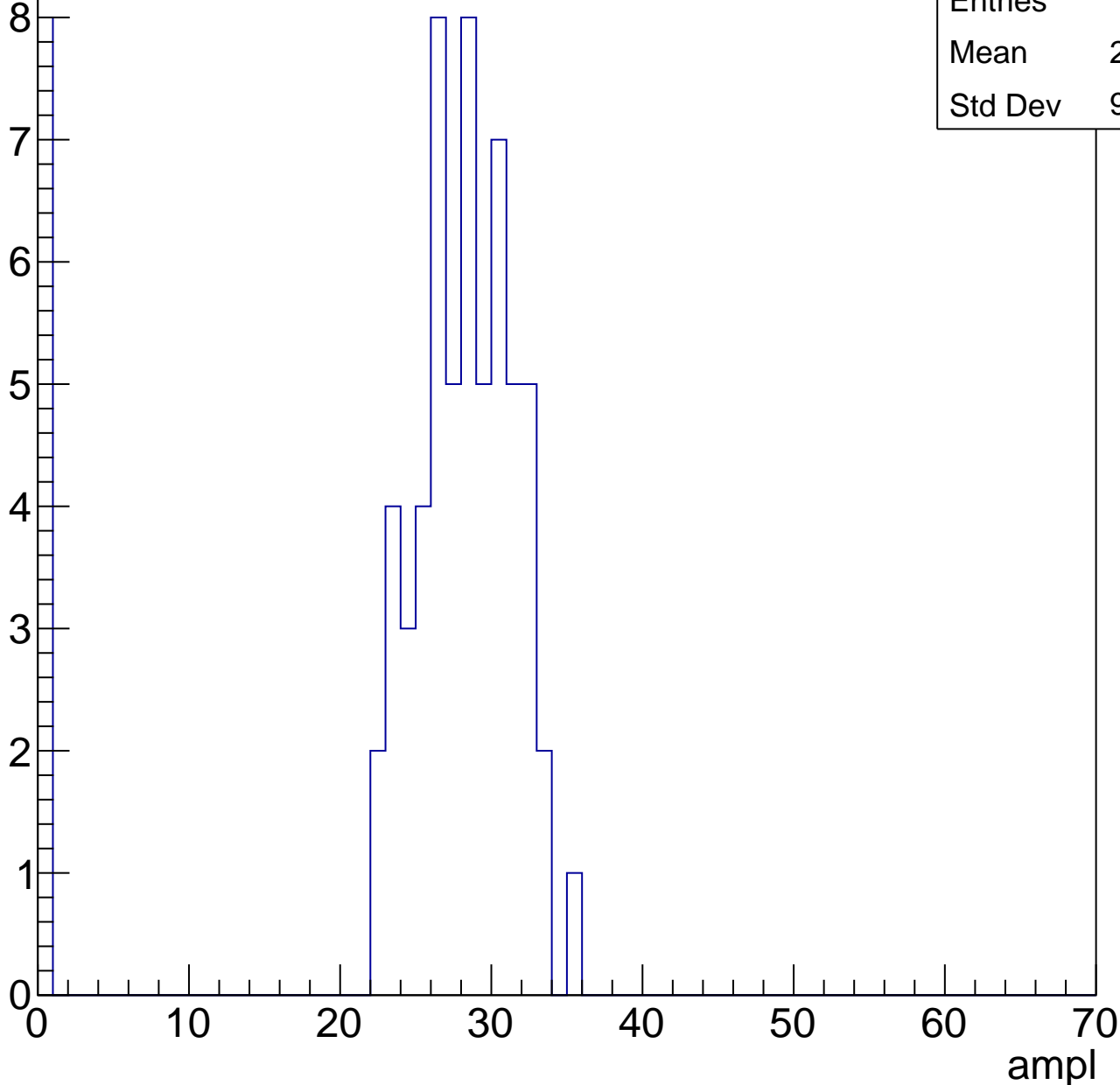
Entries	19
Mean	1.158
Std Dev	4.913

B1L103S, U9-ch32, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	24.57
Std Dev	9.489

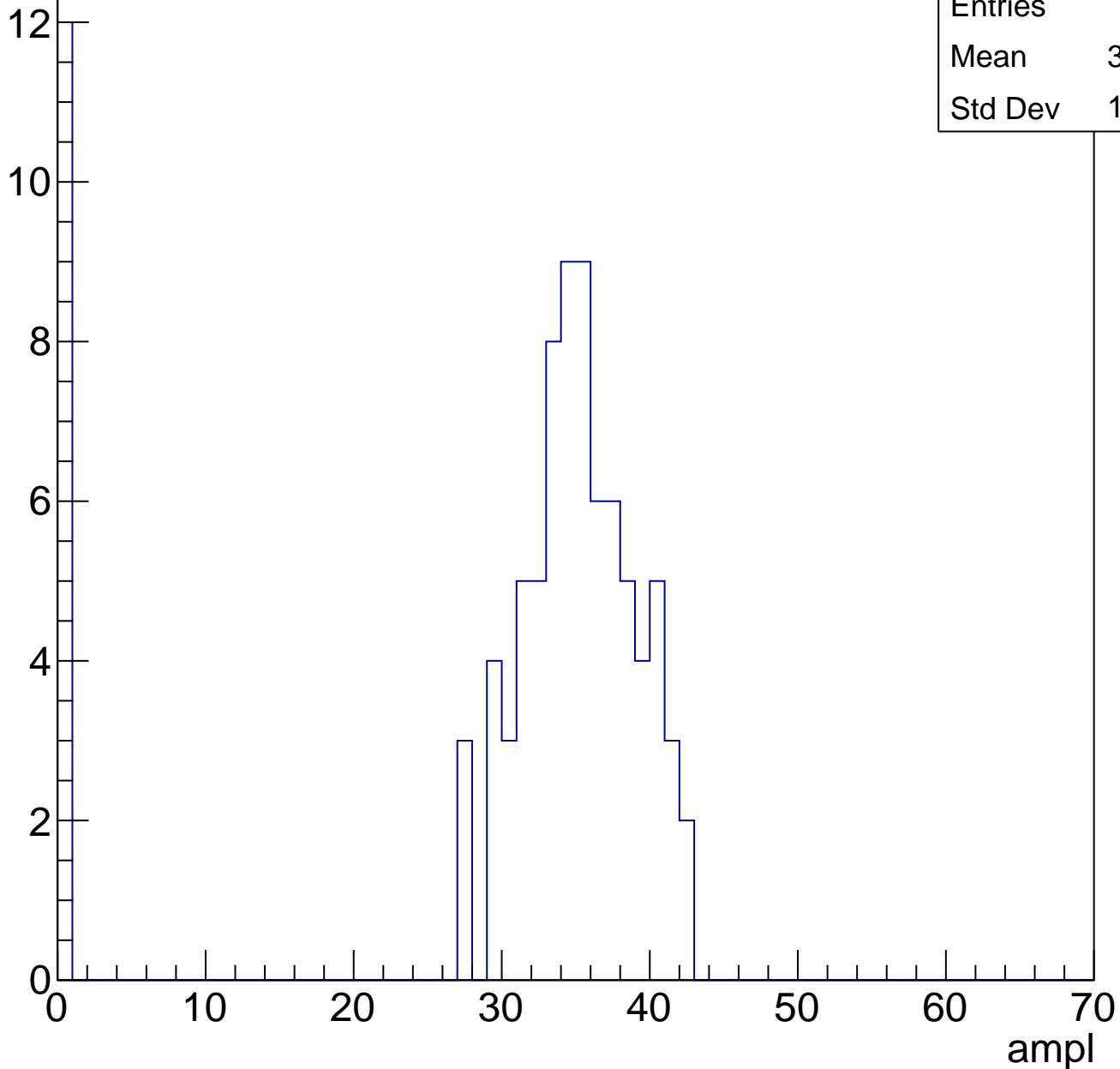


B1L103S, U9-ch32, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	30.09
Std Dev	12.36

Entry

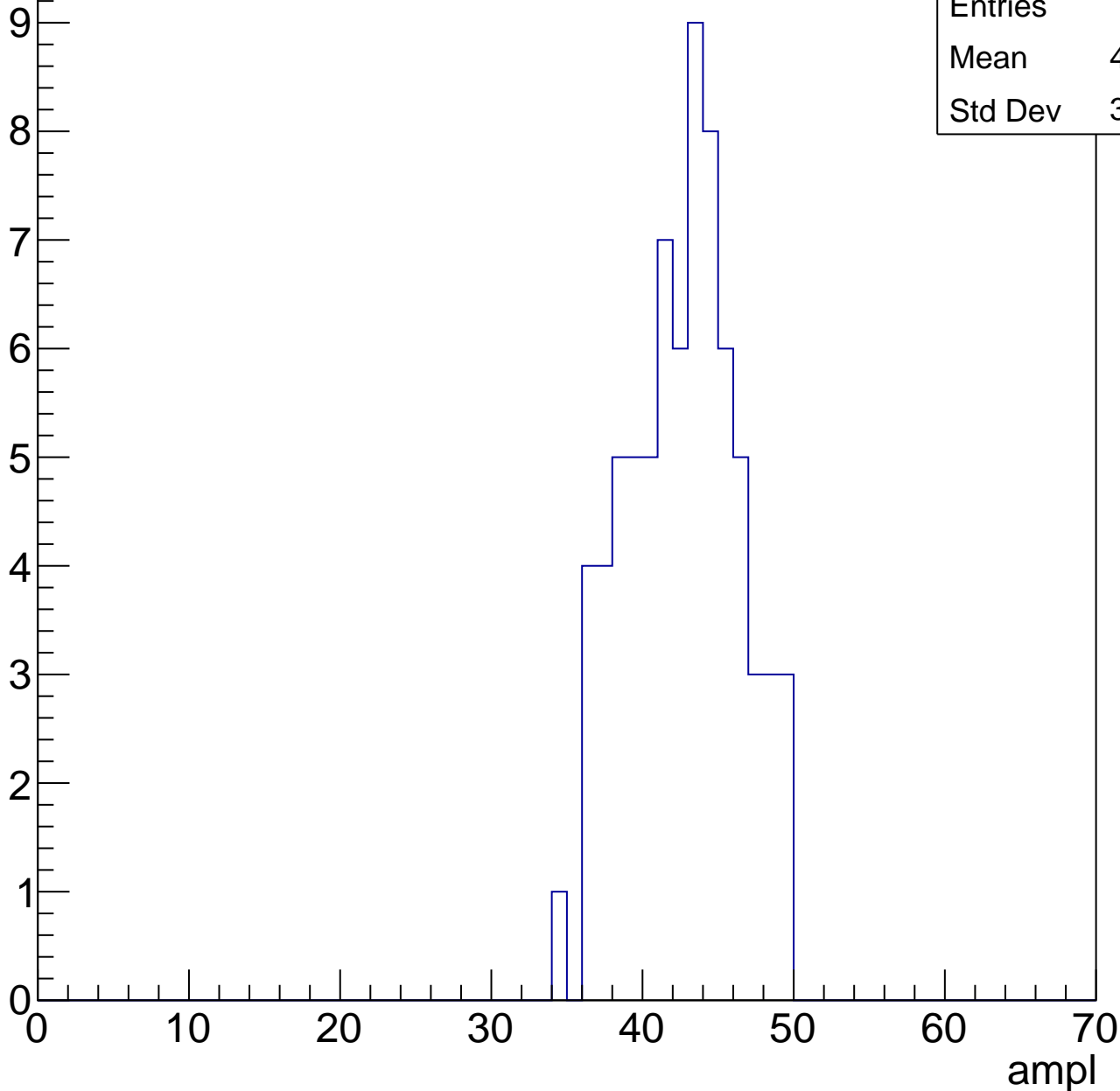


B1L103S, U9-ch32, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	42.18
Std Dev	3.607

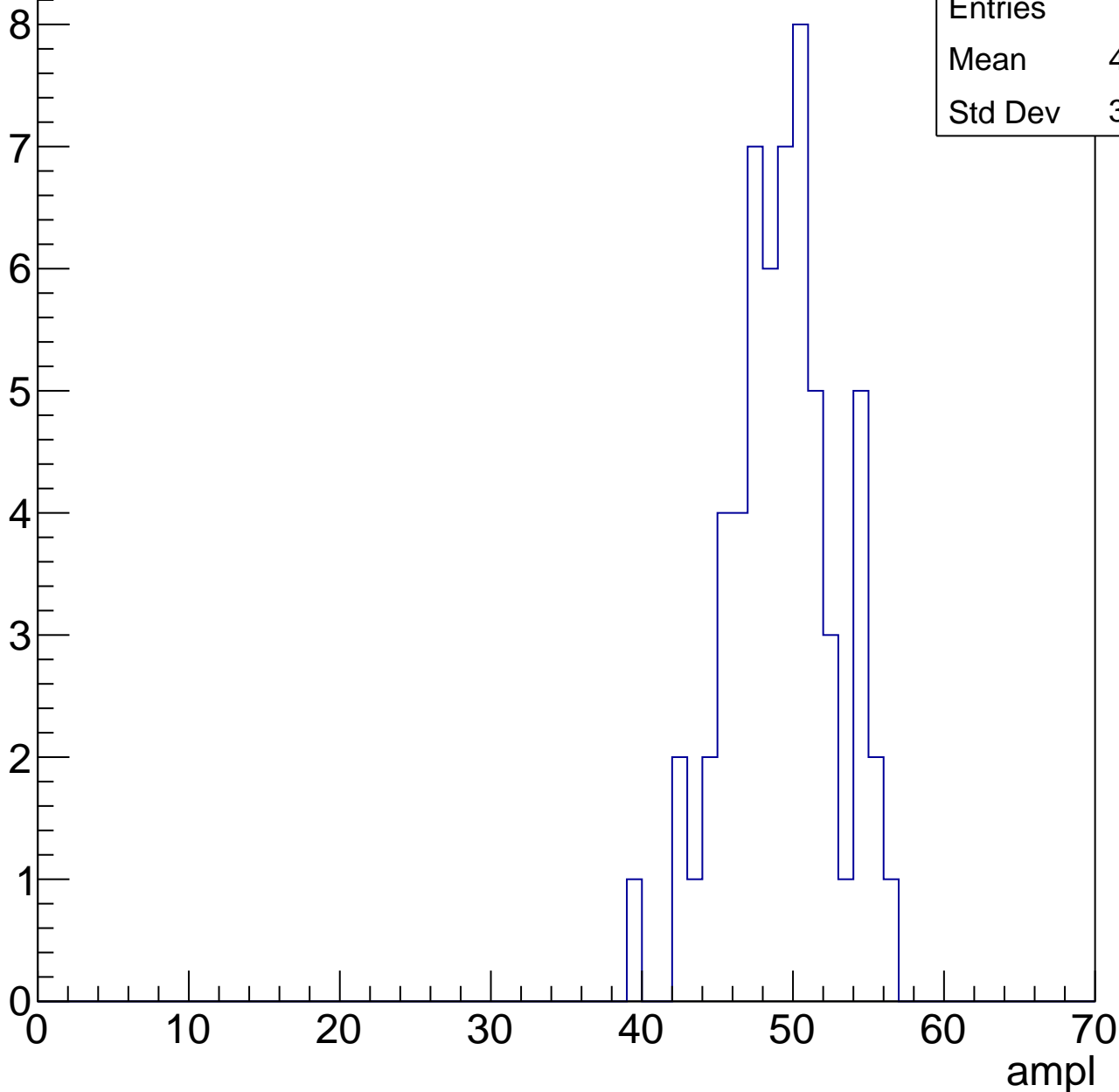


B1L103S, U9-ch32, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	48.78
Std Dev	3.523

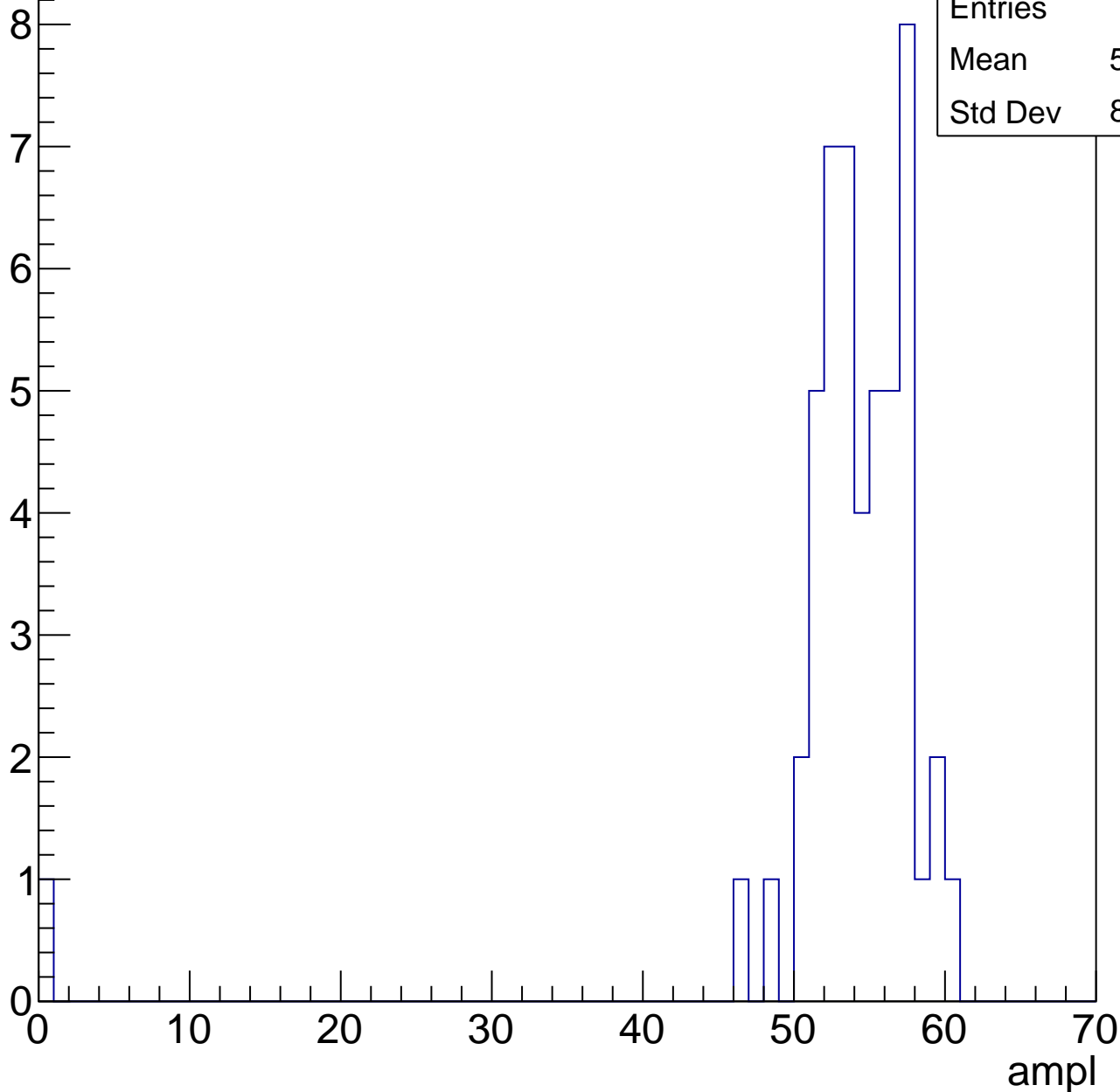


B1L103S, U9-ch32, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

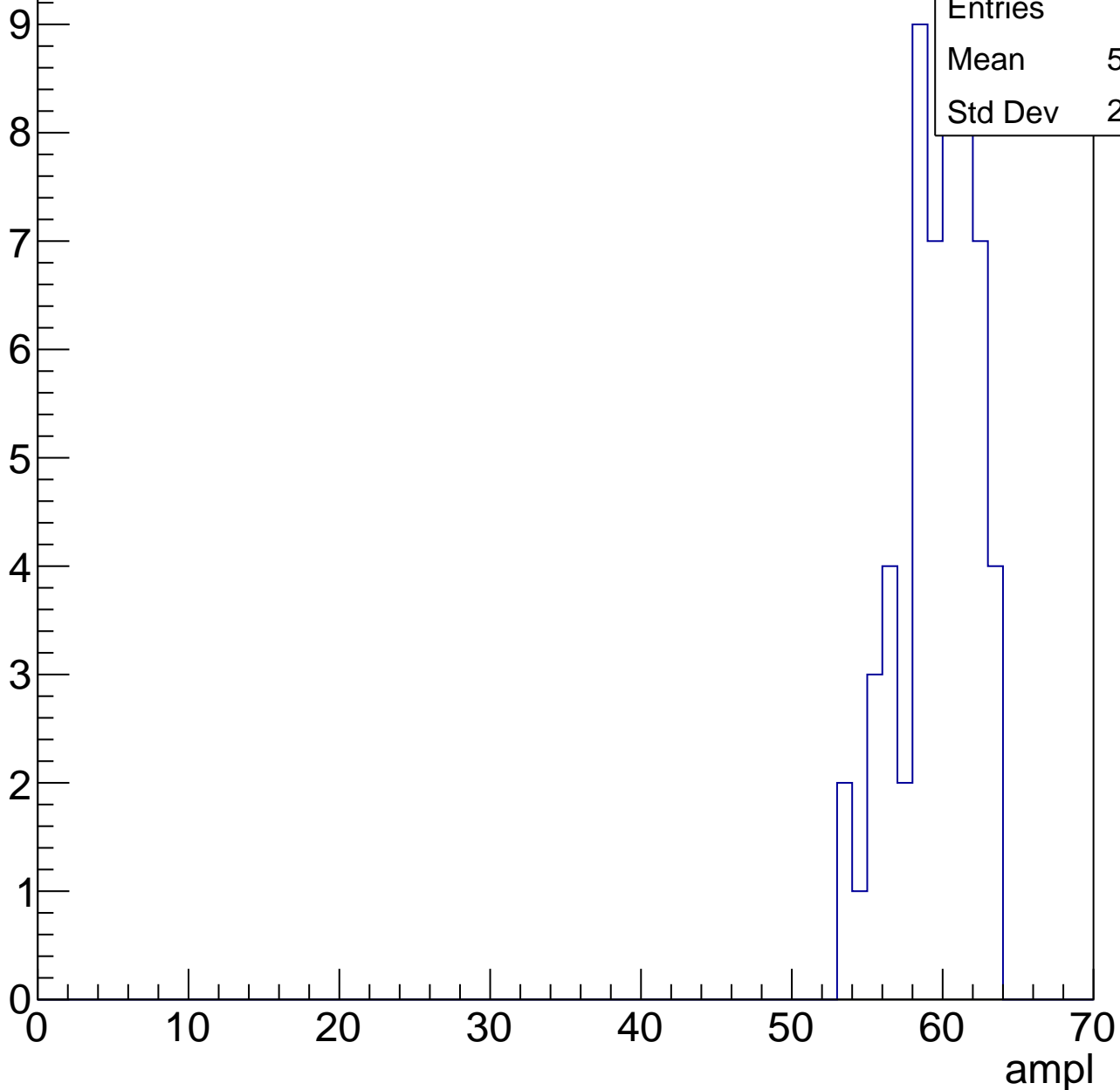
Entries	50
Mean	52.94
Std Dev	8.088



B1L103S, U9-ch32, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

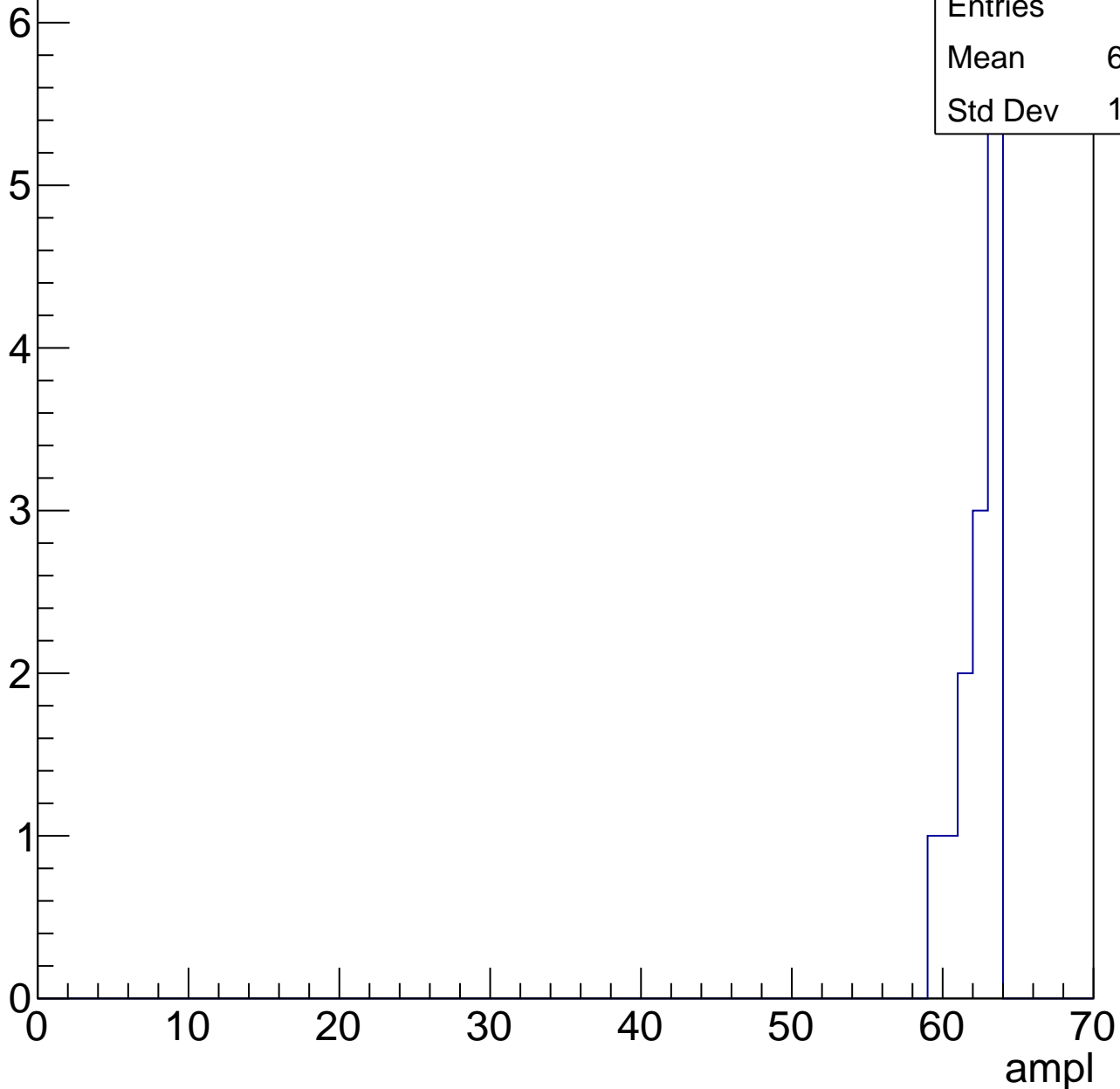


B1L103S, U9-ch32, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	13
Mean	61.92
Std Dev	1.269



B1L103S, U9-ch32, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.105
Std Dev	4.689

Entry

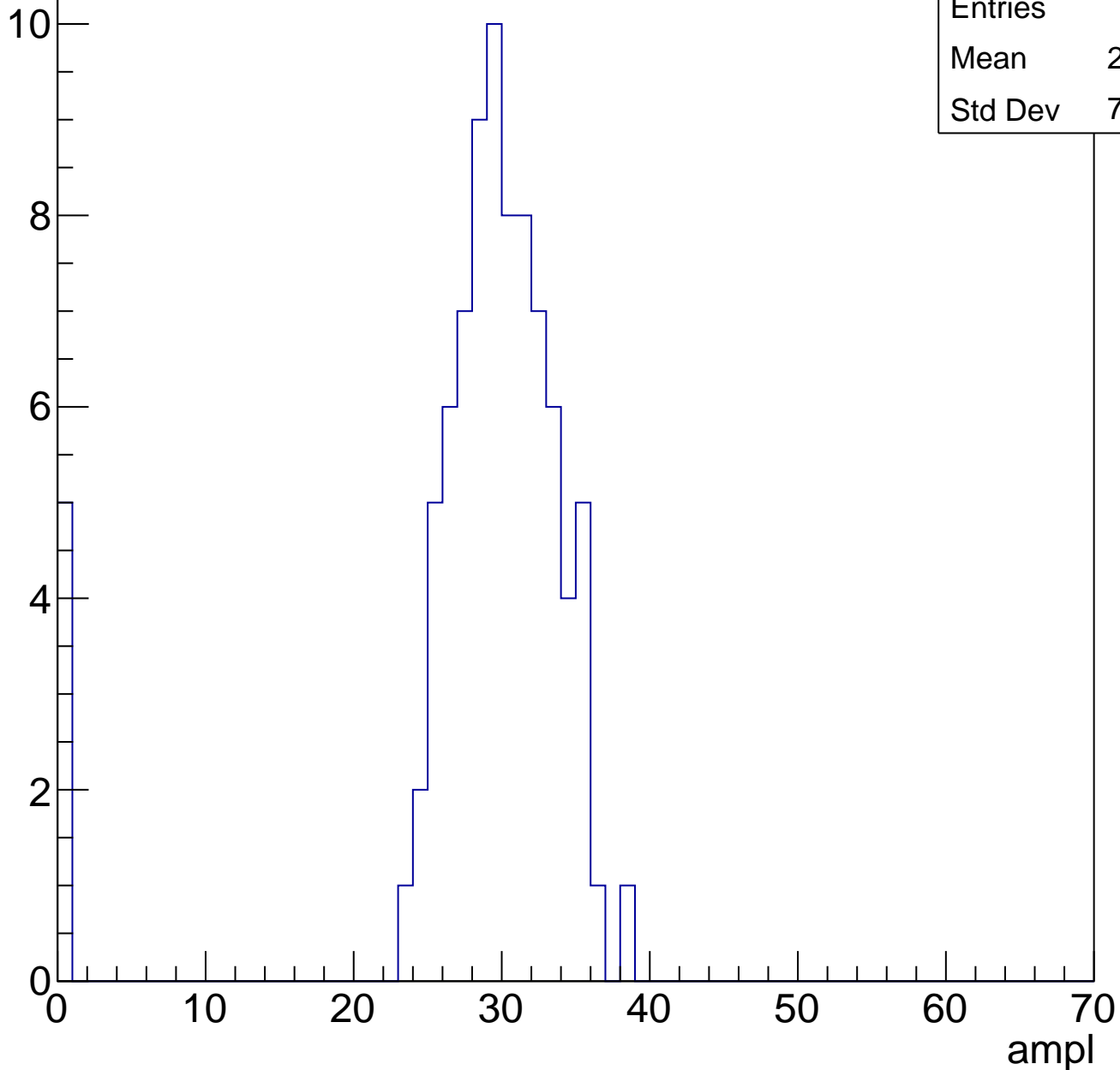


B1L103S, U9-ch33, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	85
Mean	27.98
Std Dev	7.656

Entry

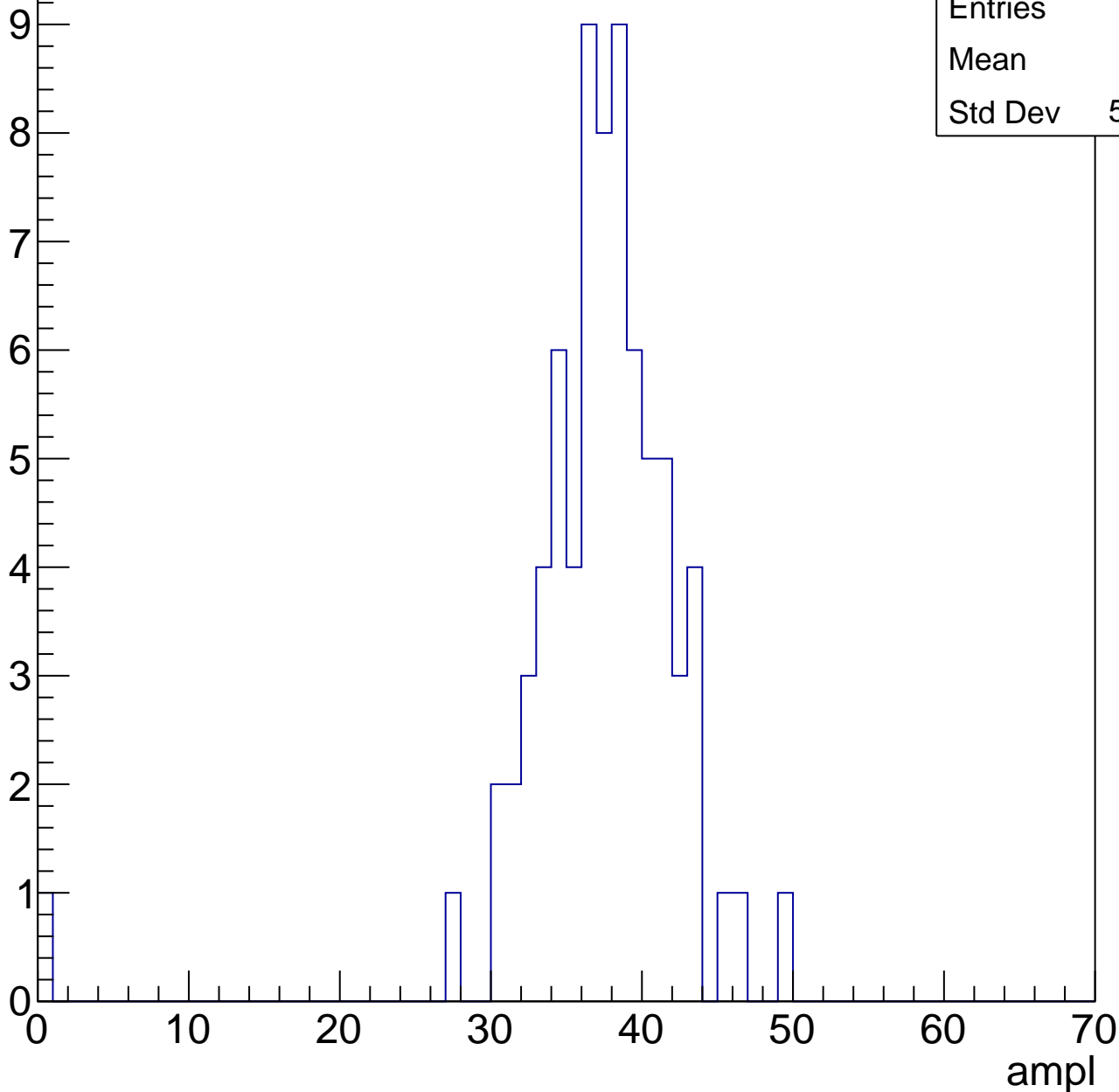


B1L103S, U9-ch33, adc1

calib_packv5_041523_1651.root, FC#0, port C2

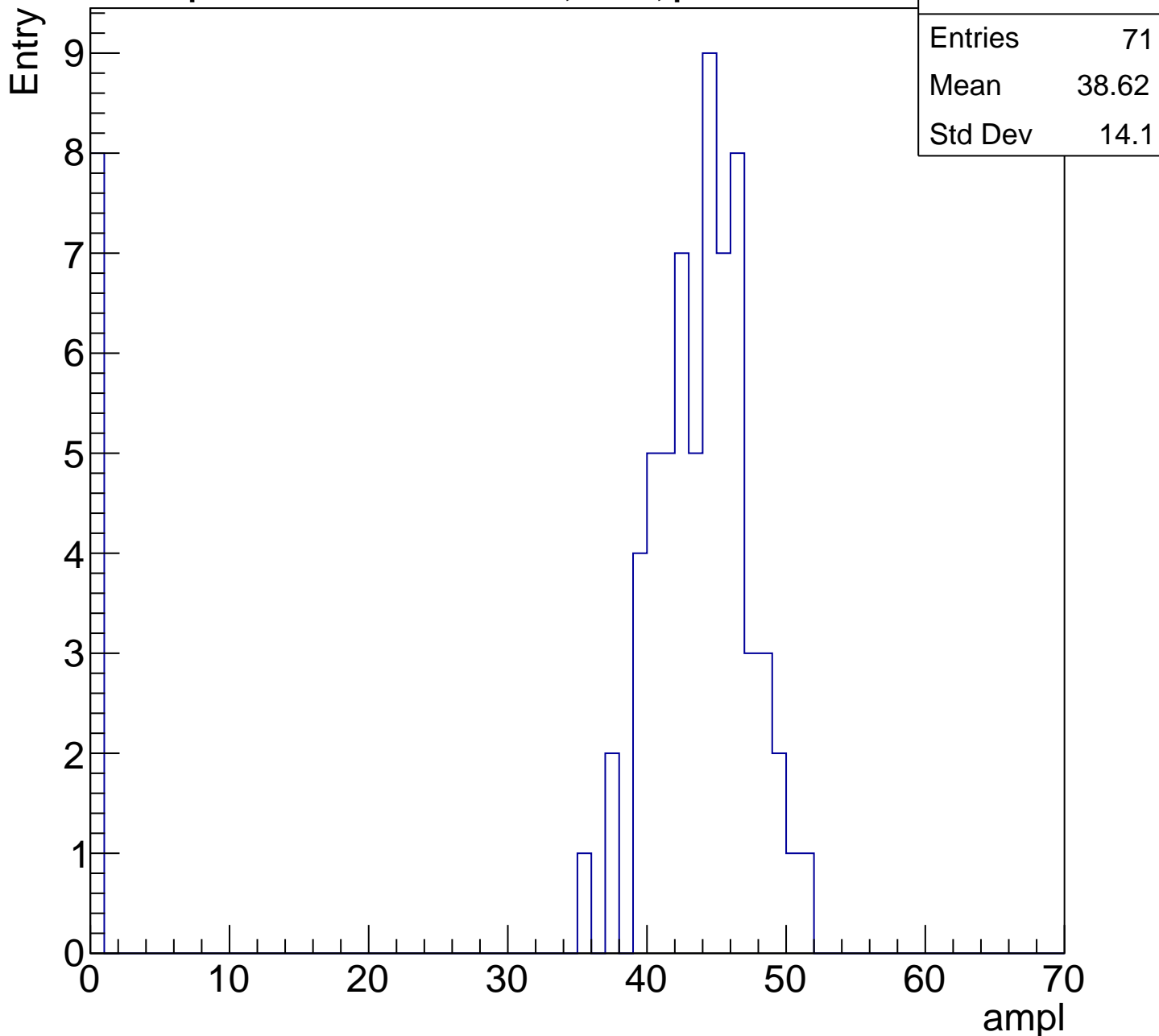
Entry

Entries	75
Mean	36.8
Std Dev	5.797



B1L103S, U9-ch33, adc2

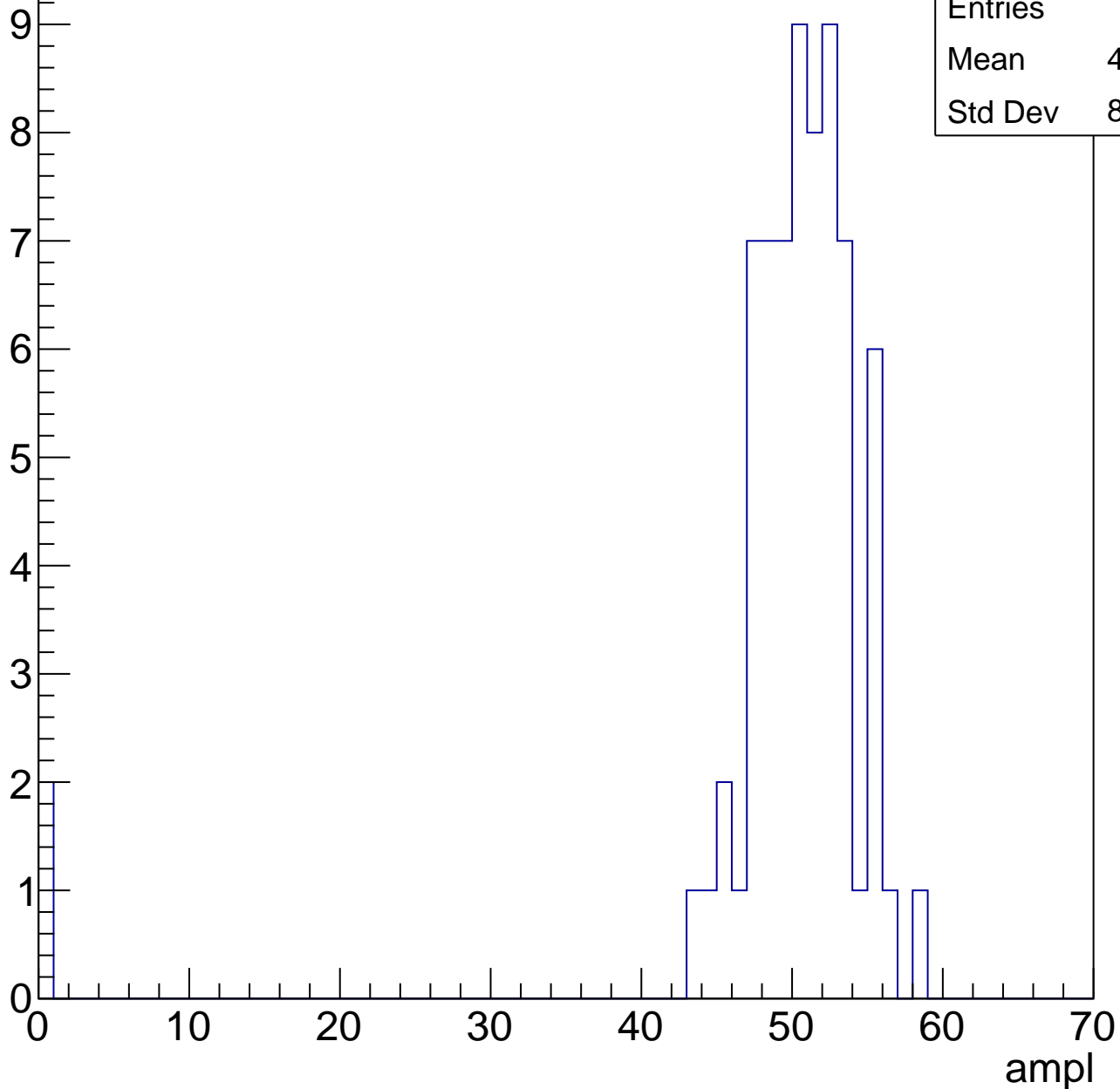
calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U9-ch33, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

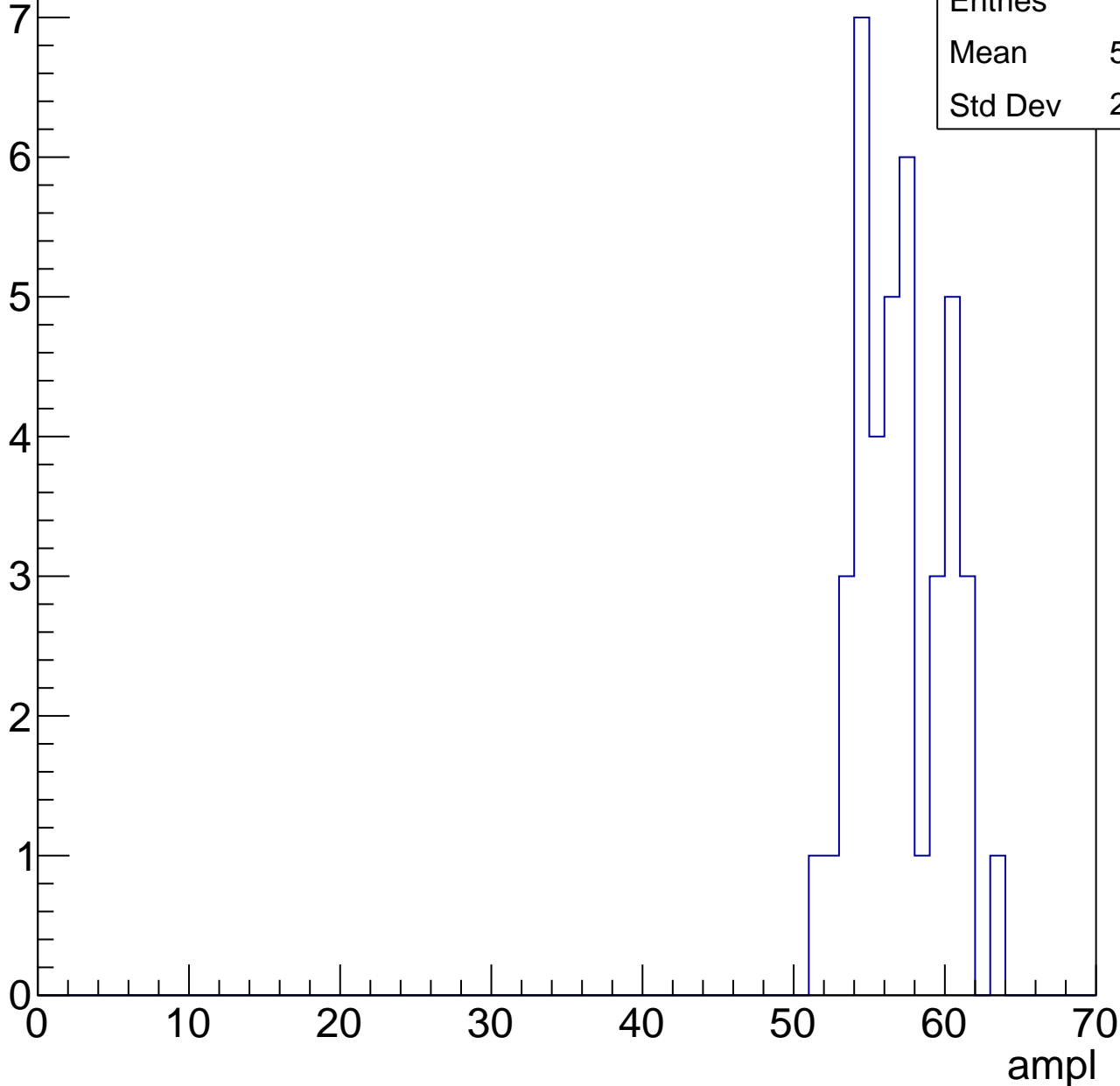


B1L103S, U9-ch33, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	56.58
Std Dev	2.863



B1L103S, U9-ch33, adc5

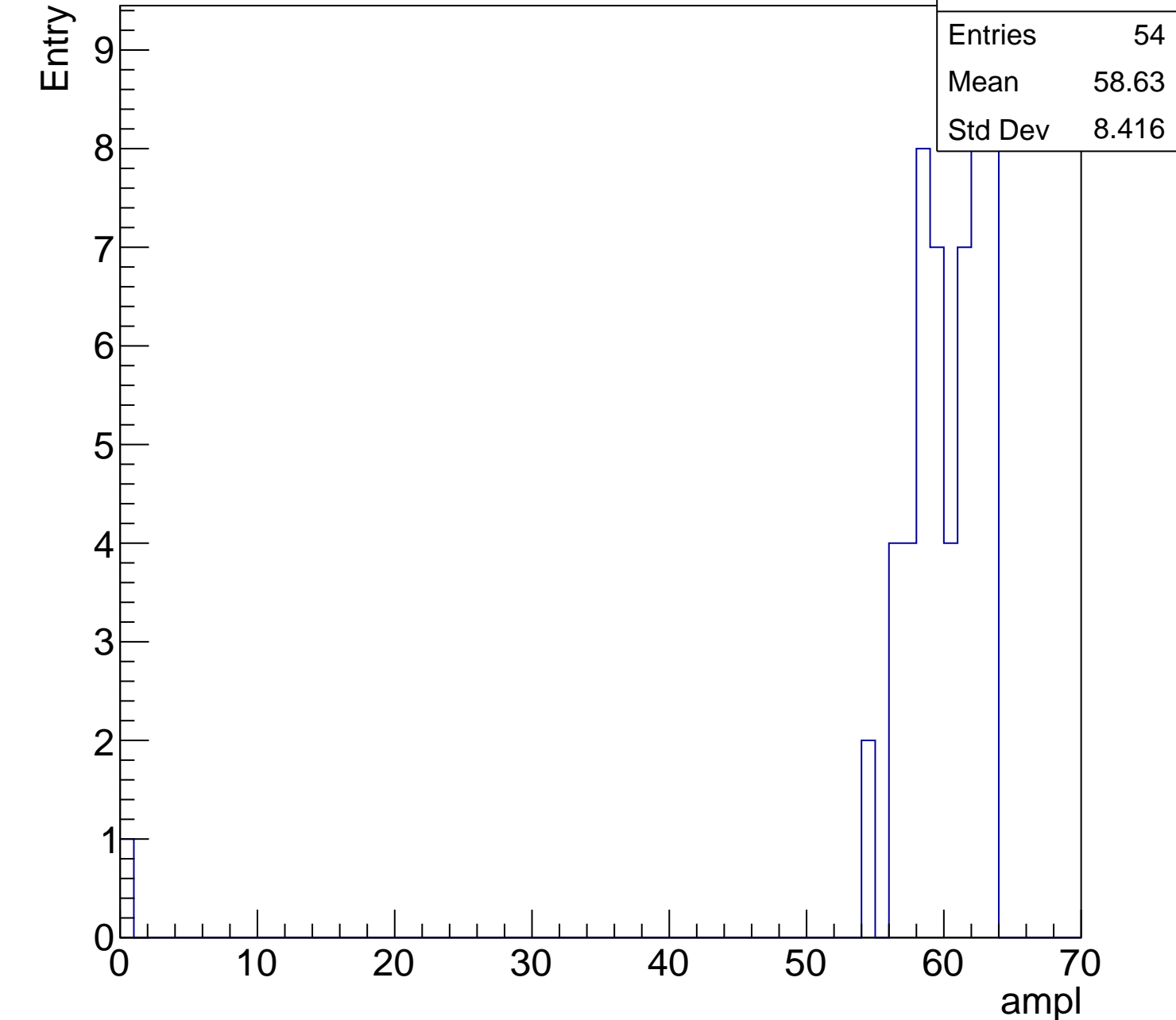
calib_packv5_041523_1651.root, FC#0, port C2

Entry

9
8
7
6
5
4
3
2
1
0

Entries	54
Mean	58.63
Std Dev	8.416

ampl



B1L103S, U9-ch33, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

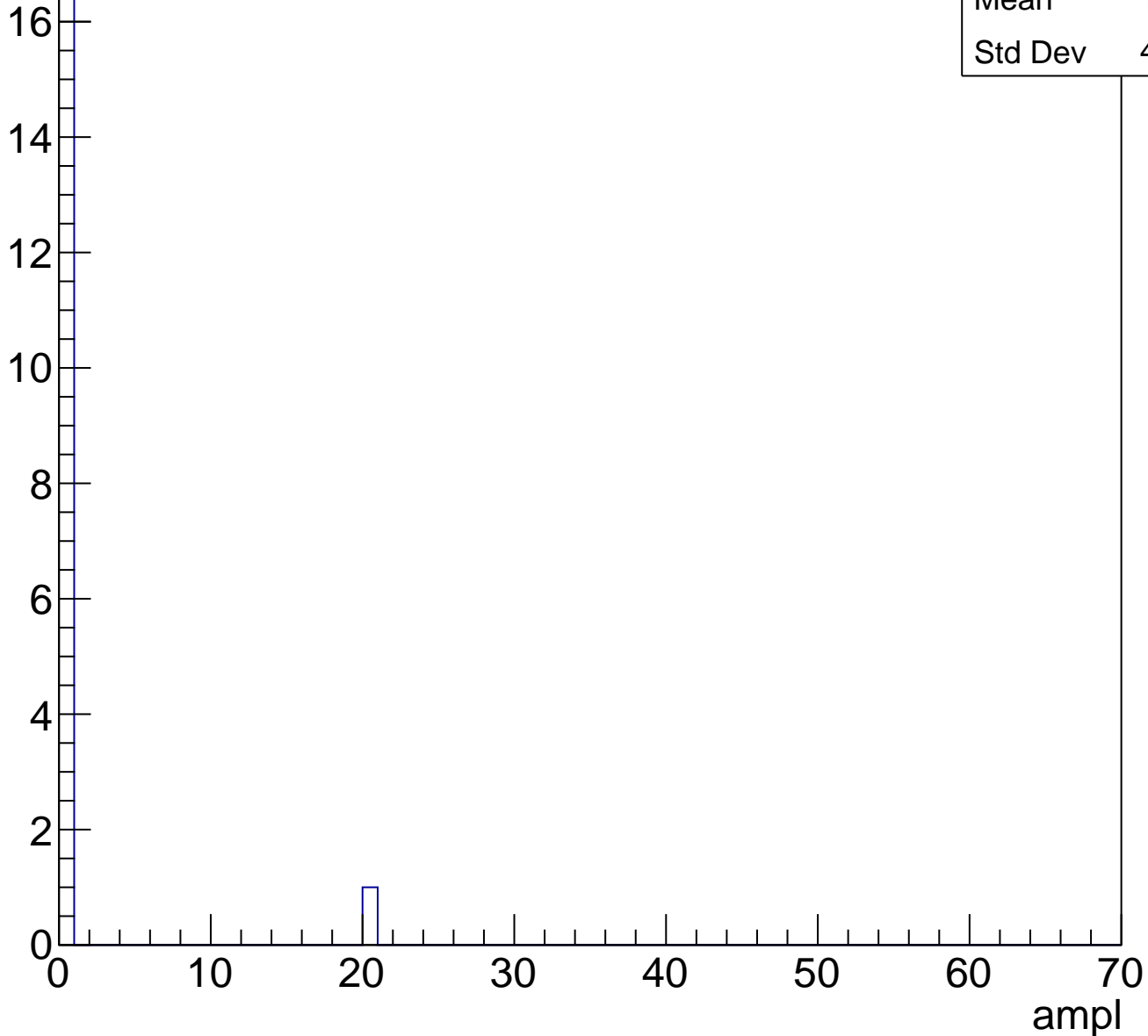


B1L103S, U9-ch33, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	18
Mean	1.111
Std Dev	4.581

Entry

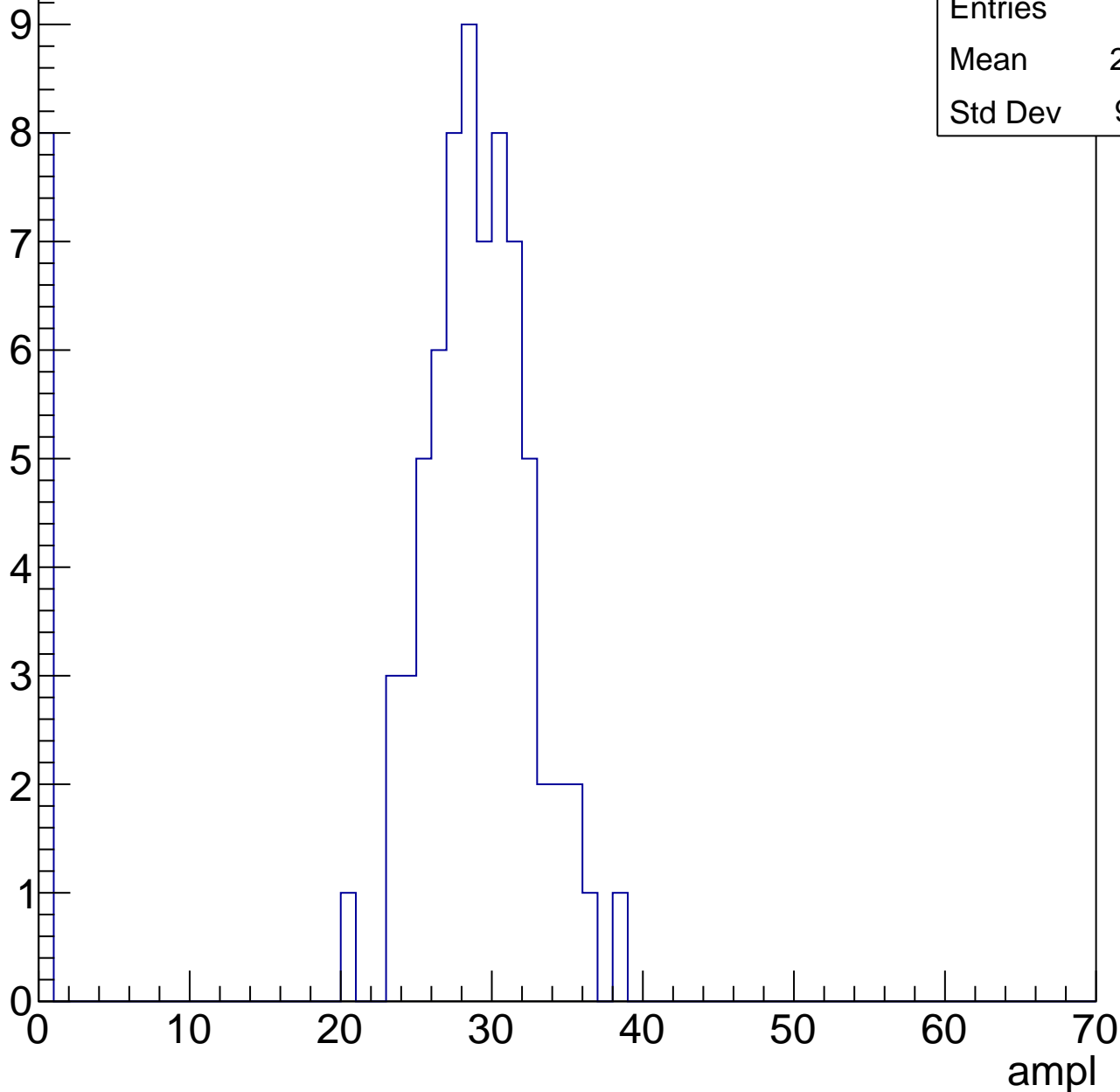


B1L103S, U9-ch34, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	25.74
Std Dev	9.271

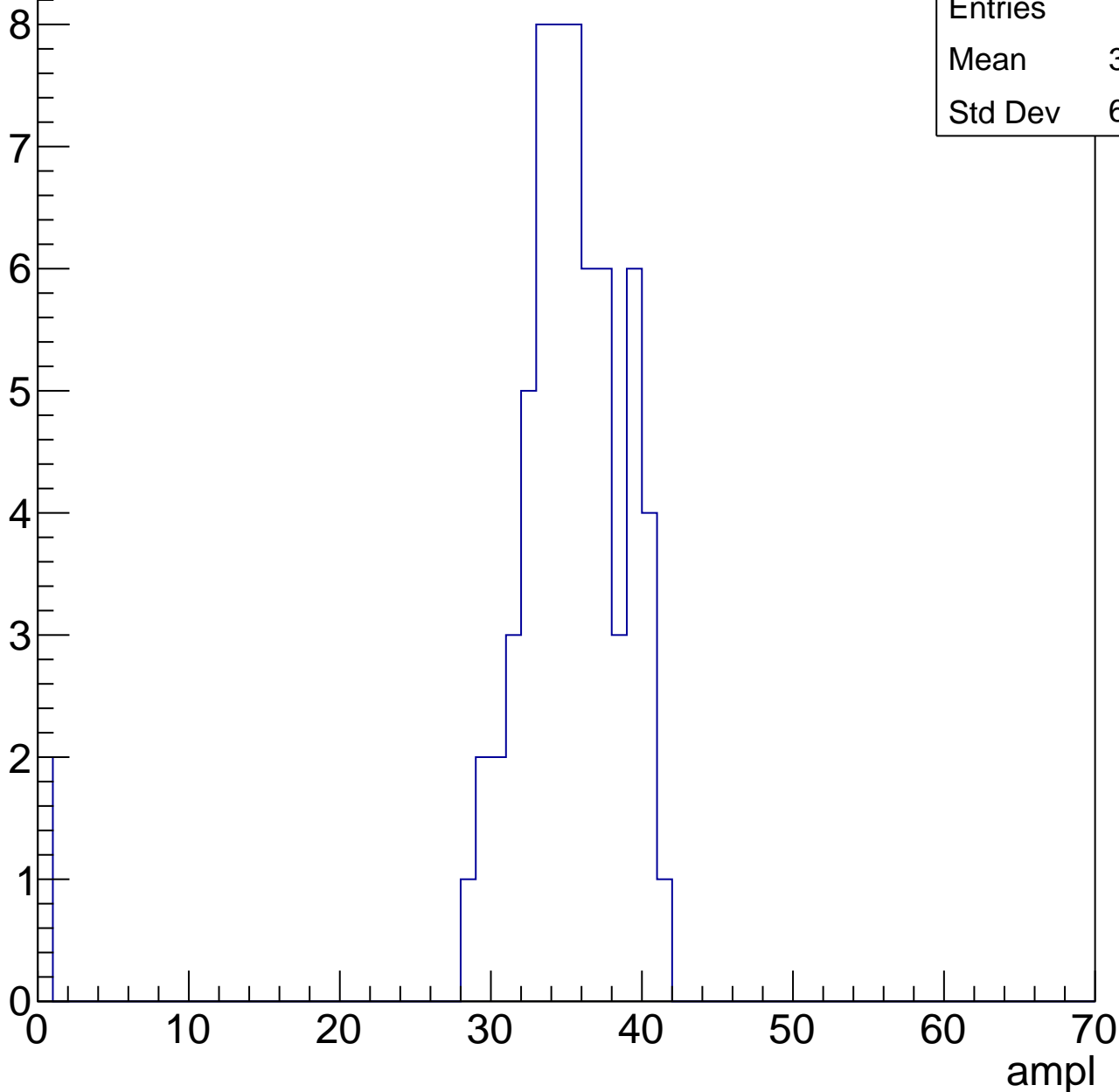


B1L103S, U9-ch34, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	33.88
Std Dev	6.749

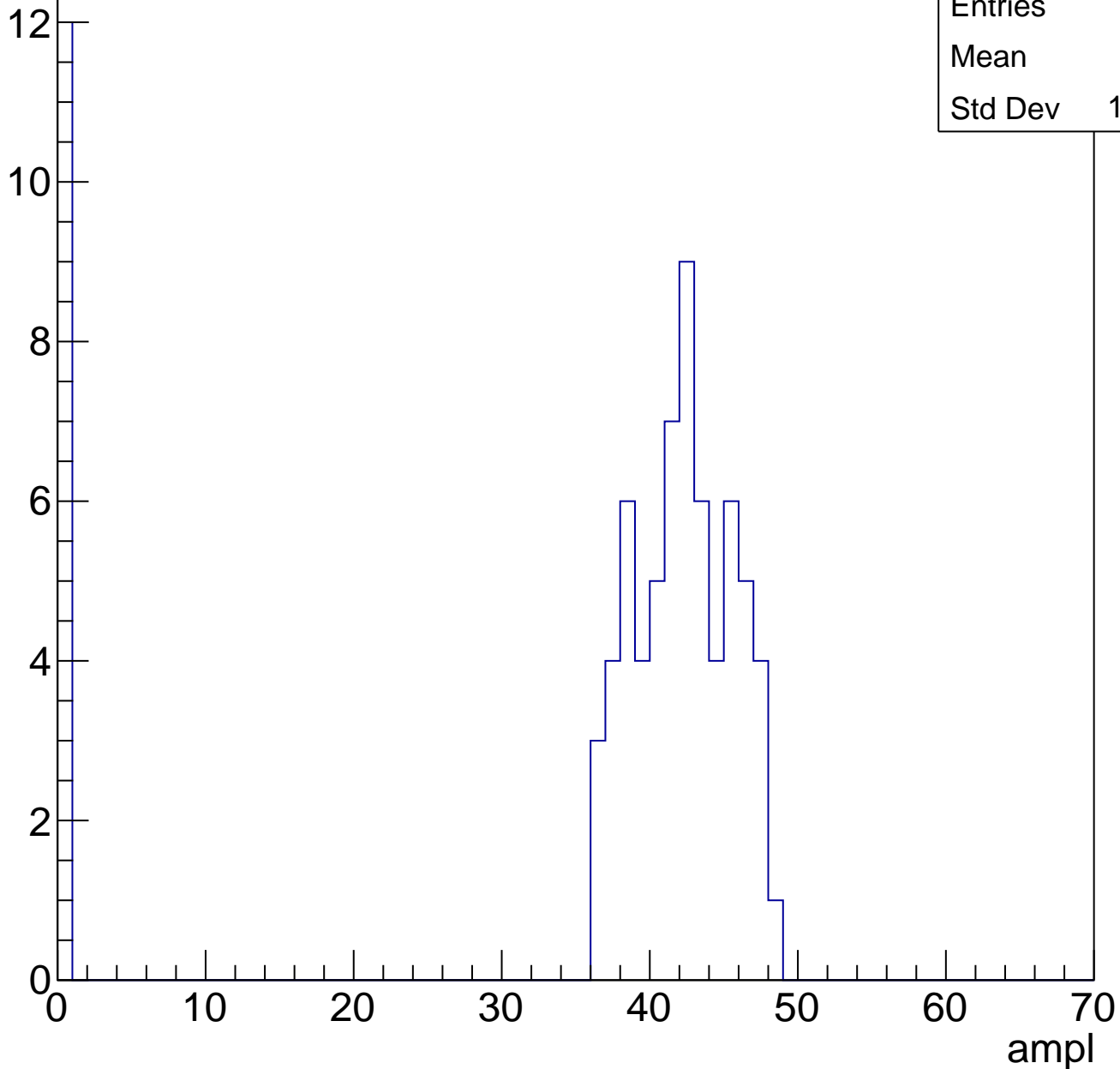


B1L103S, U9-ch34, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	76
Mean	35.2
Std Dev	15.52

Entry

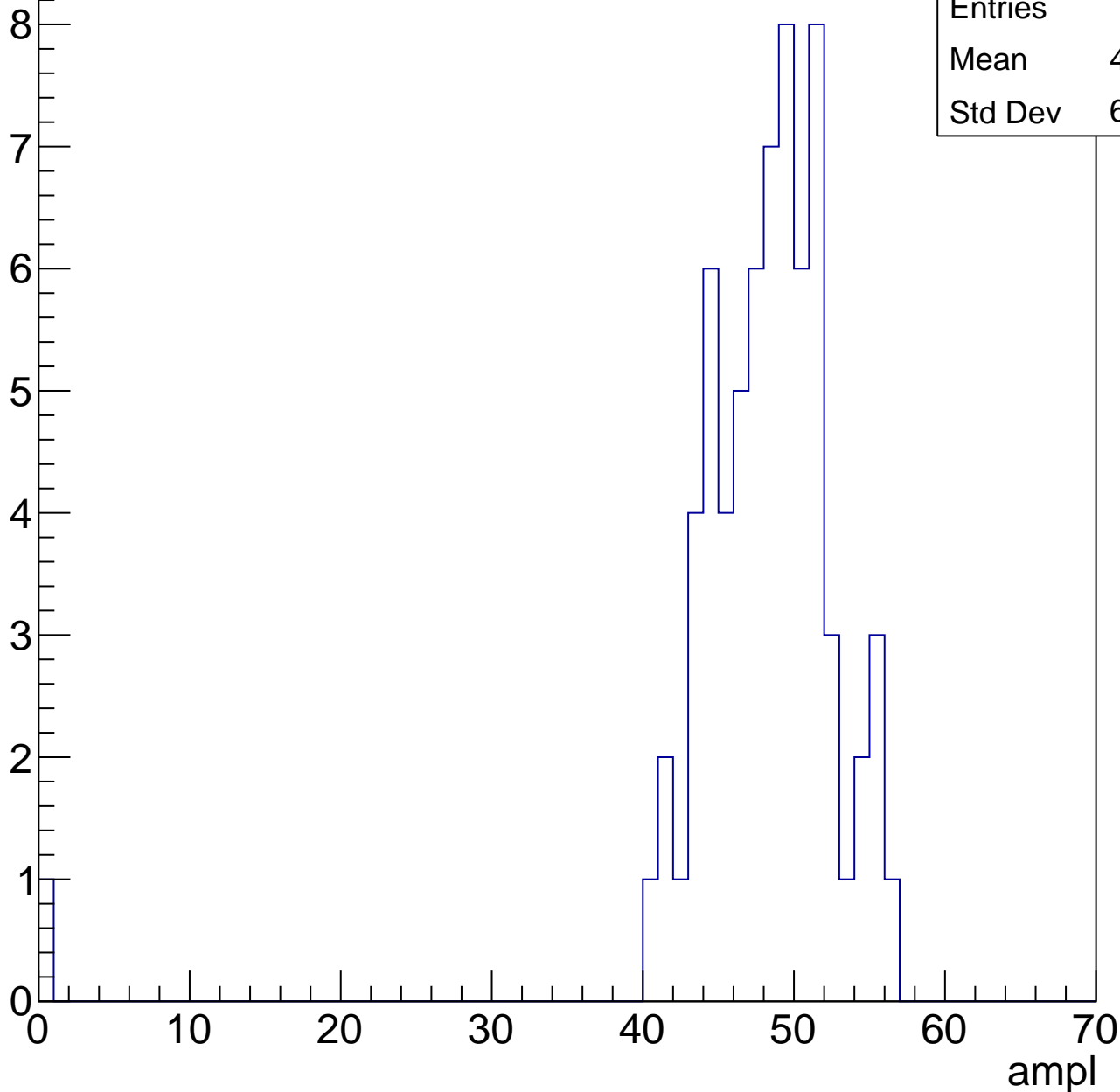


B1L103S, U9-ch34, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	47.33
Std Dev	6.799

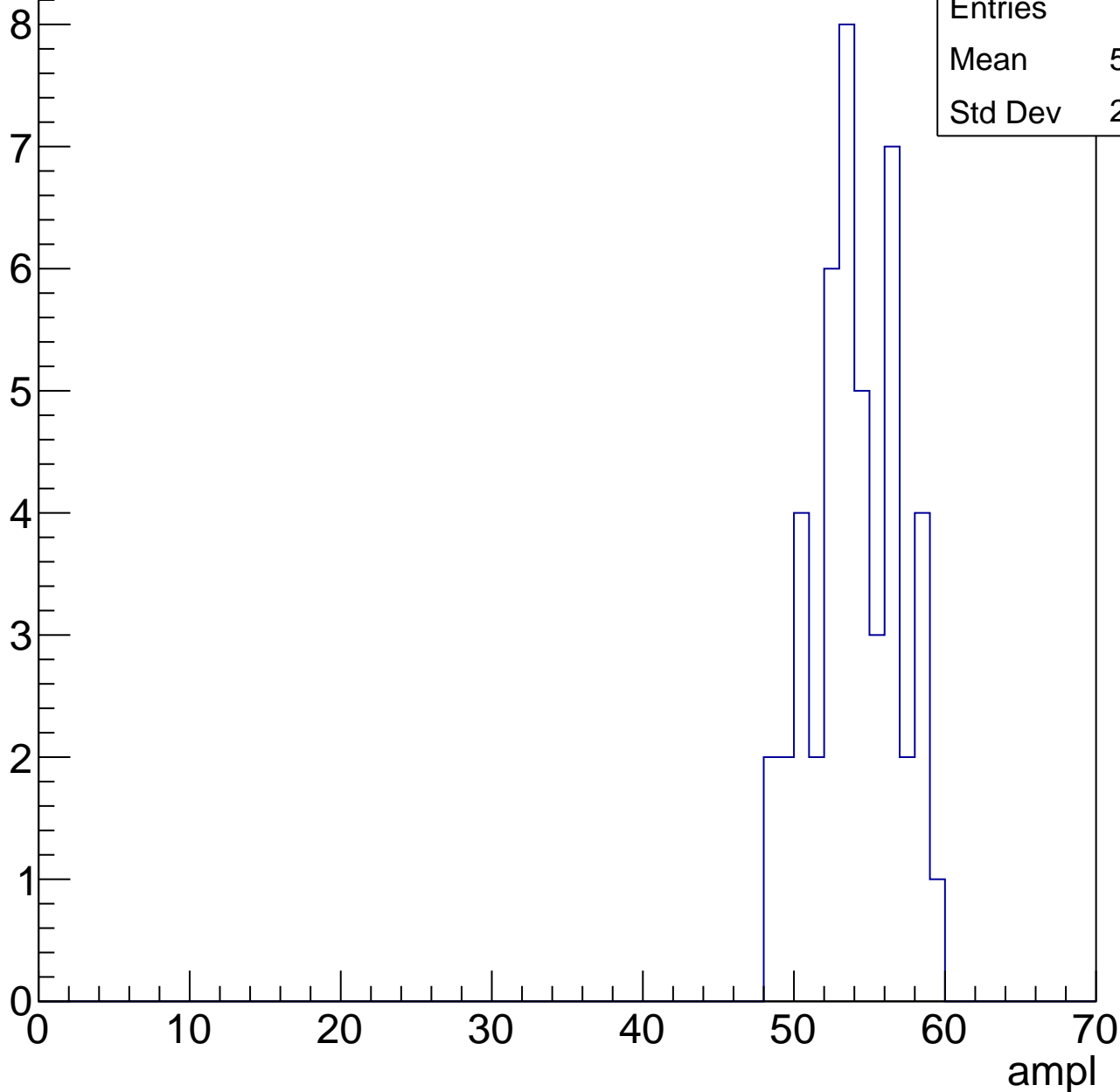


B1L103S, U9-ch34, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	46
Mean	53.57
Std Dev	2.818

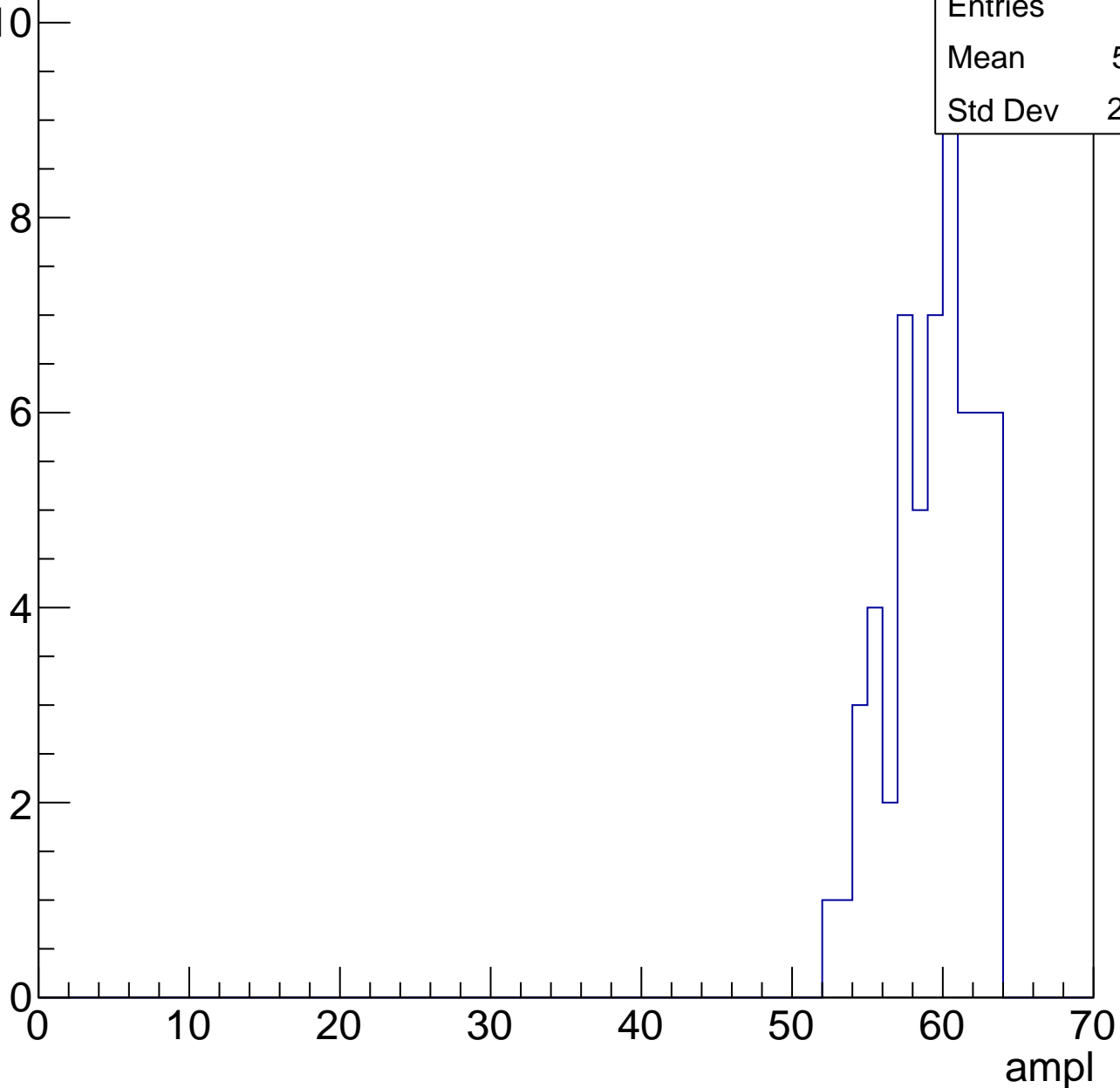


B1L103S, U9-ch34, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

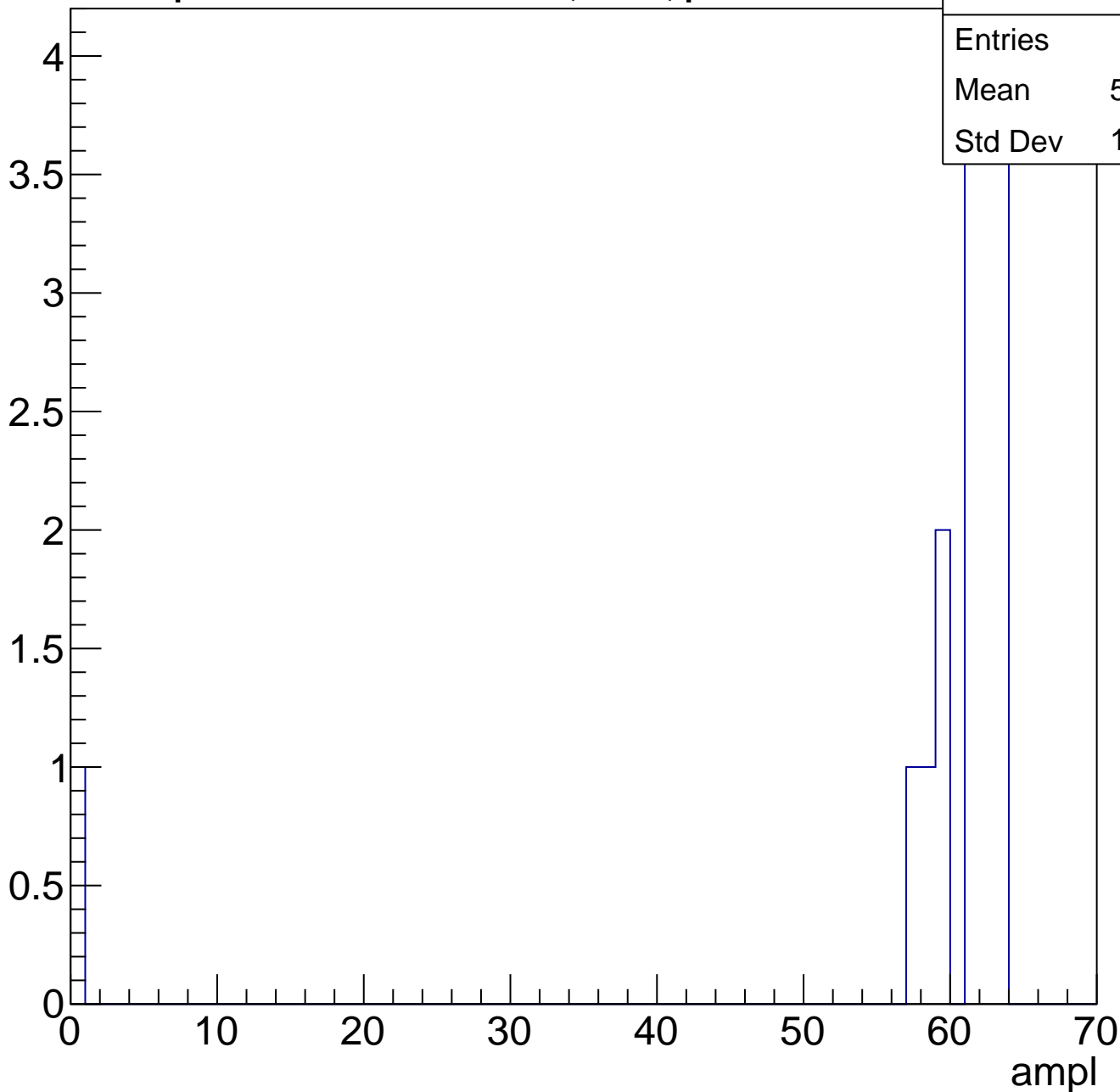
Entries	58
Mean	58.91
Std Dev	2.812



B1L103S, U9-ch34, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch34, adc7

calib_packv5_041523_1651.root, FC#0, port C2

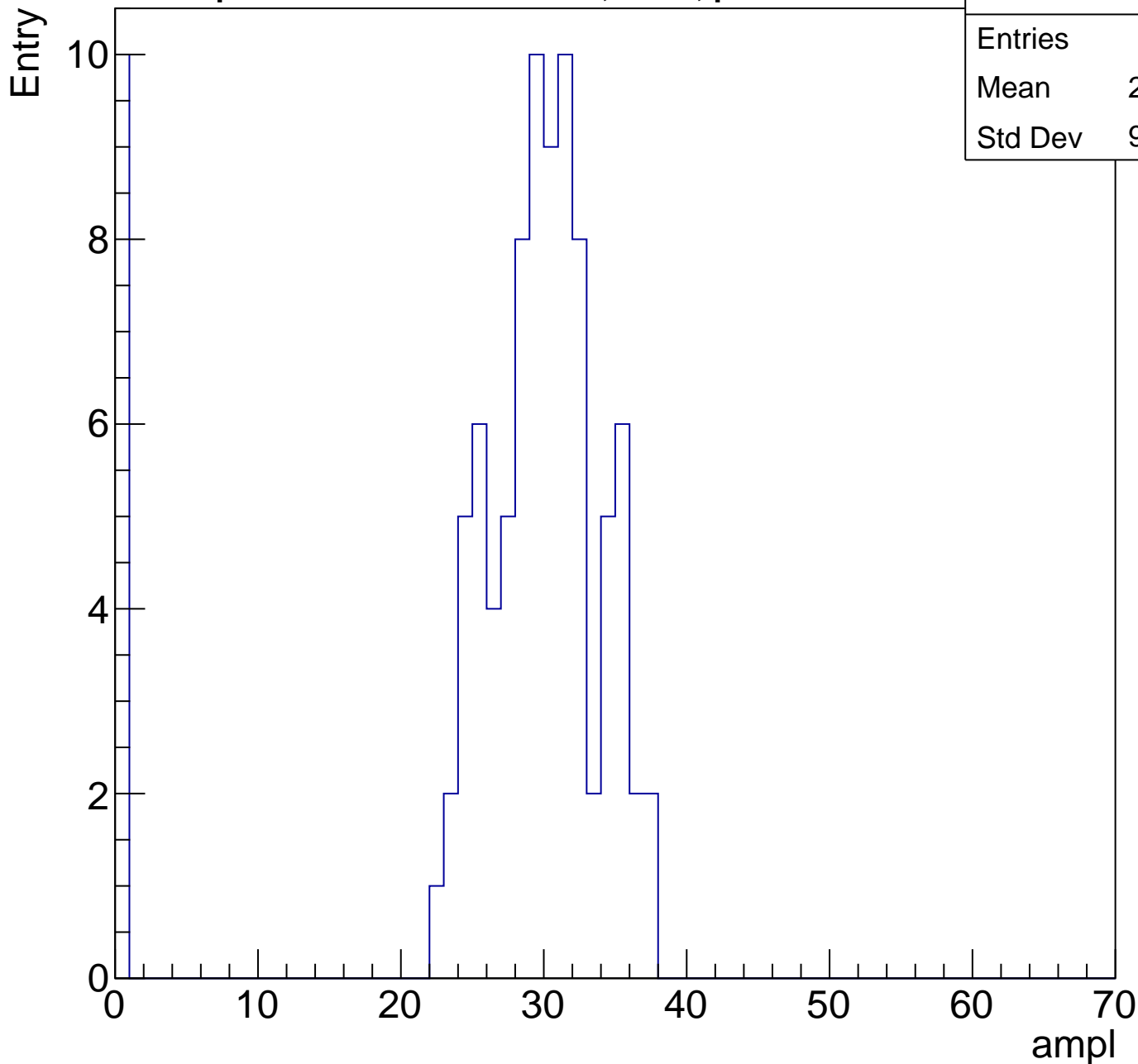
Entry



B1L103S, U9-ch35, adc0

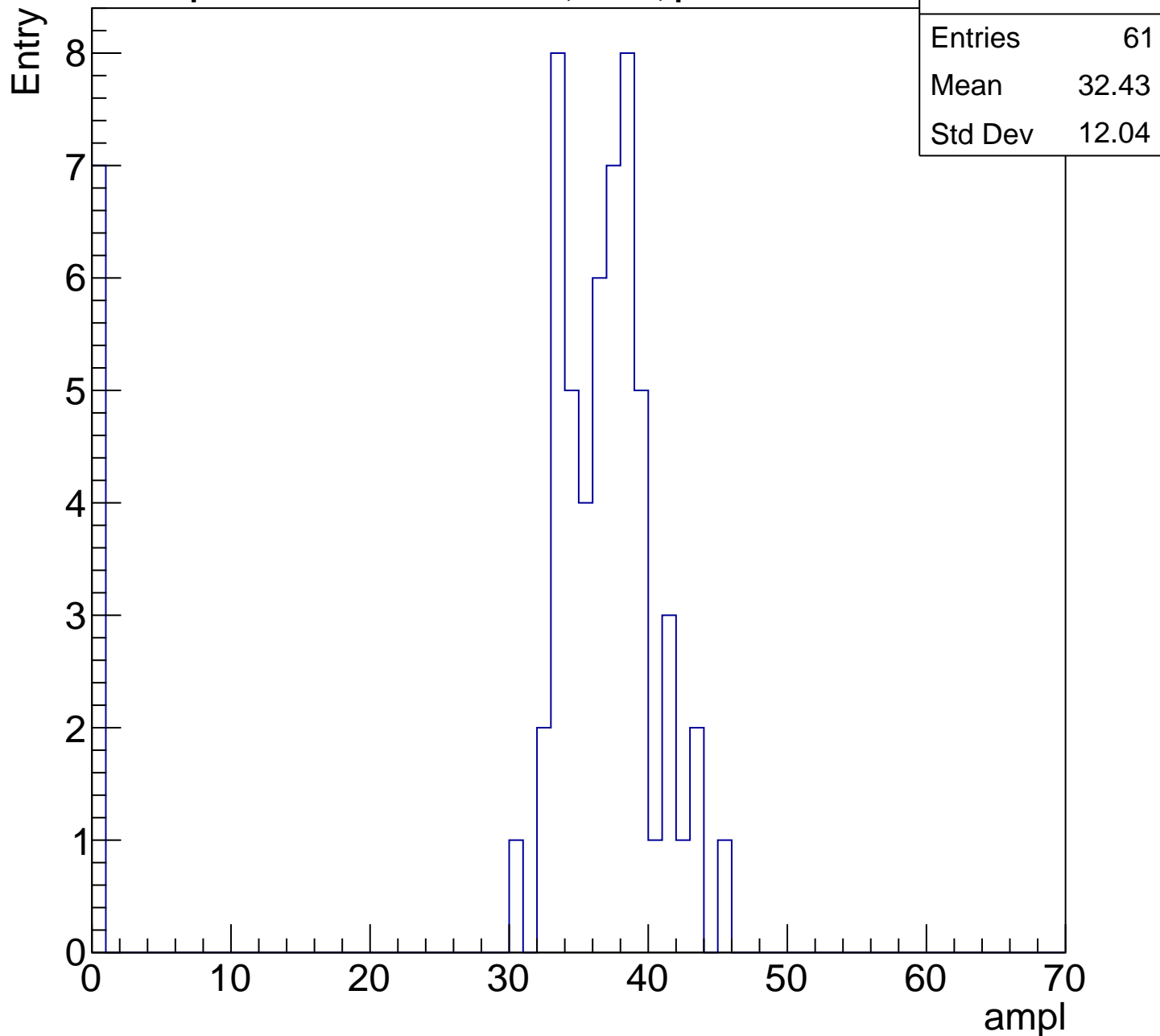
calib_packv5_041523_1651.root, FC#0, port C2

Entries	95
Mean	26.52
Std Dev	9.706



B1L103S, U9-ch35, adc1

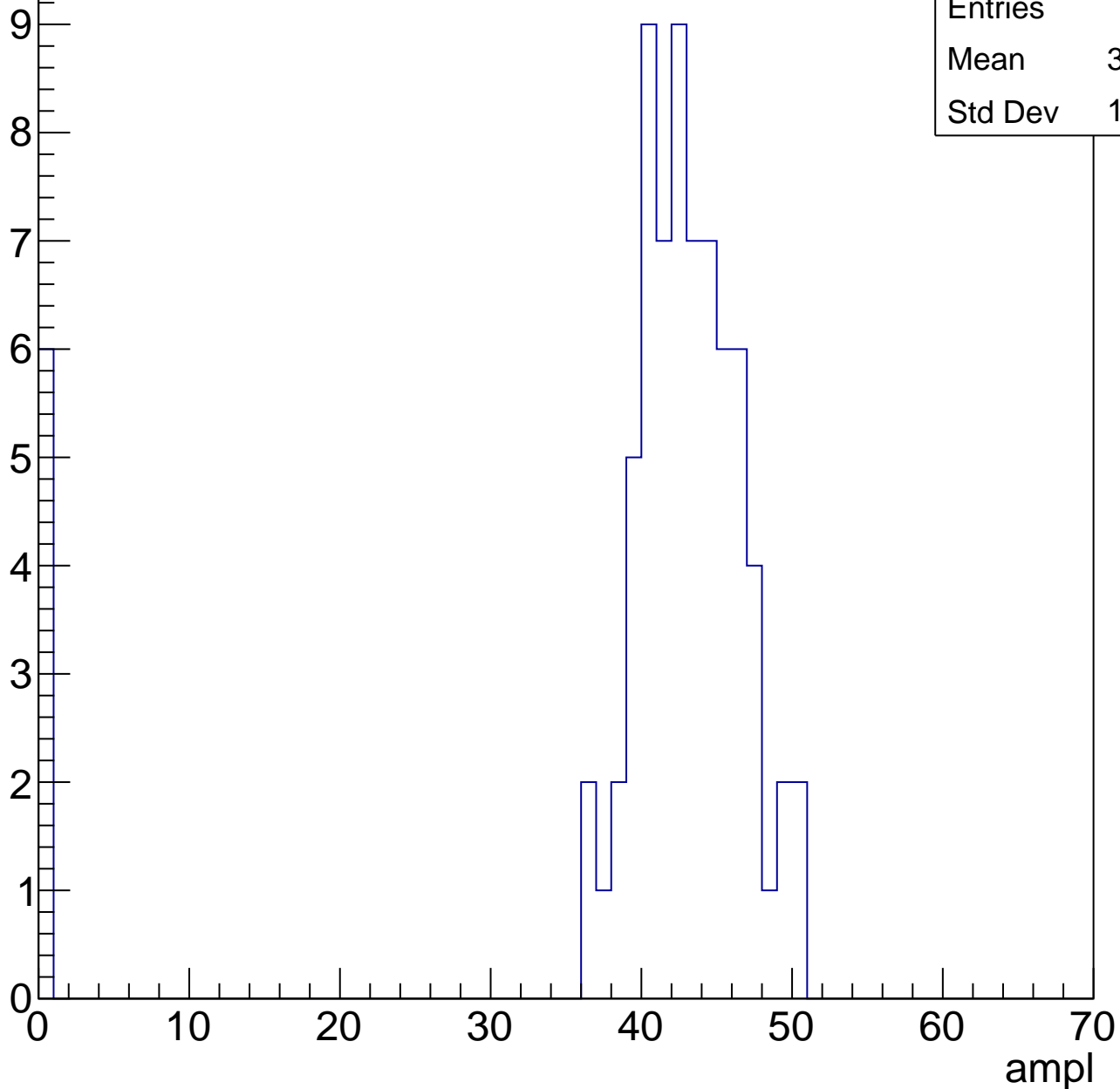
calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U9-ch35, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

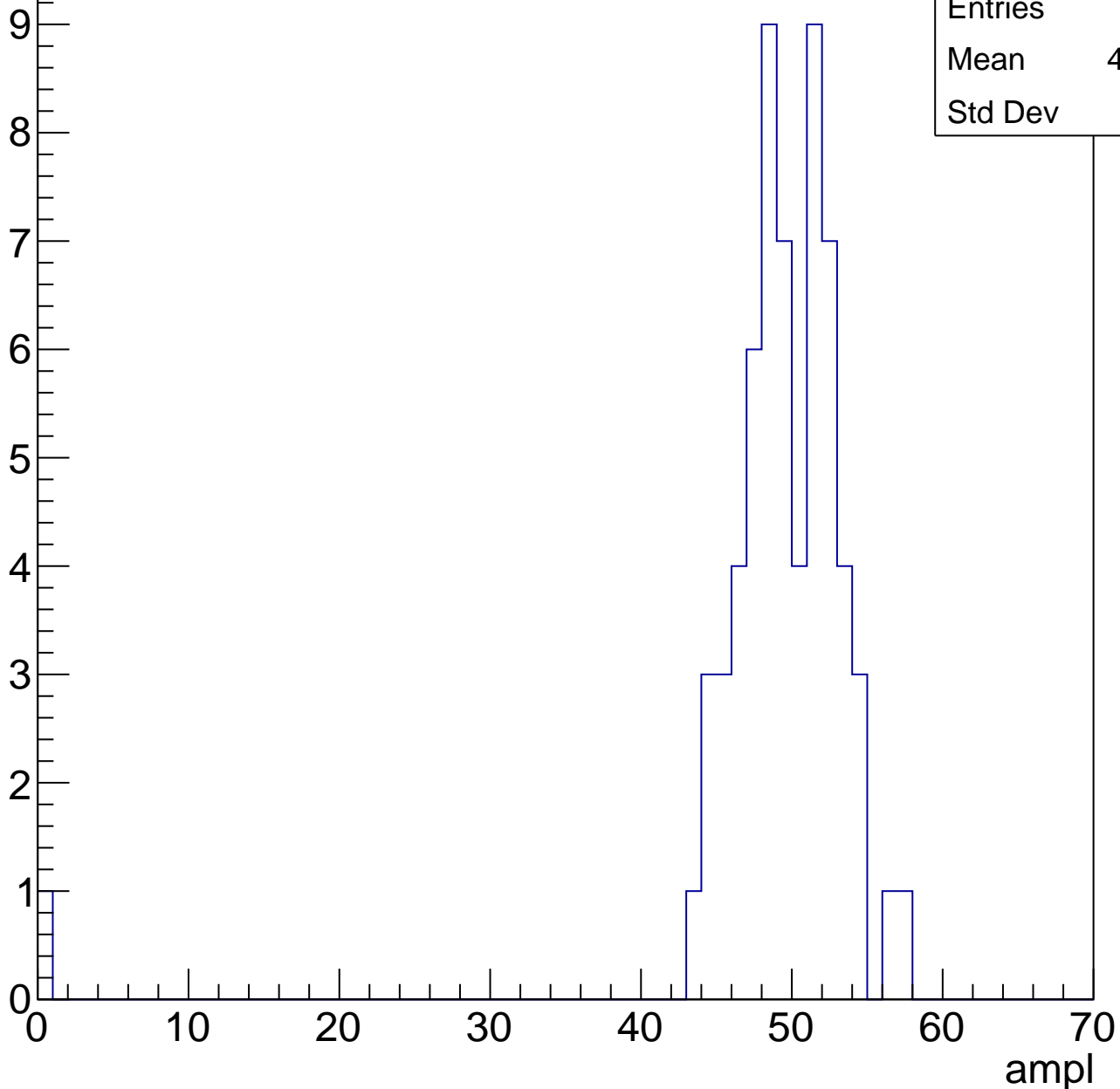


B1L103S, U9-ch35, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	48.59
Std Dev	6.87

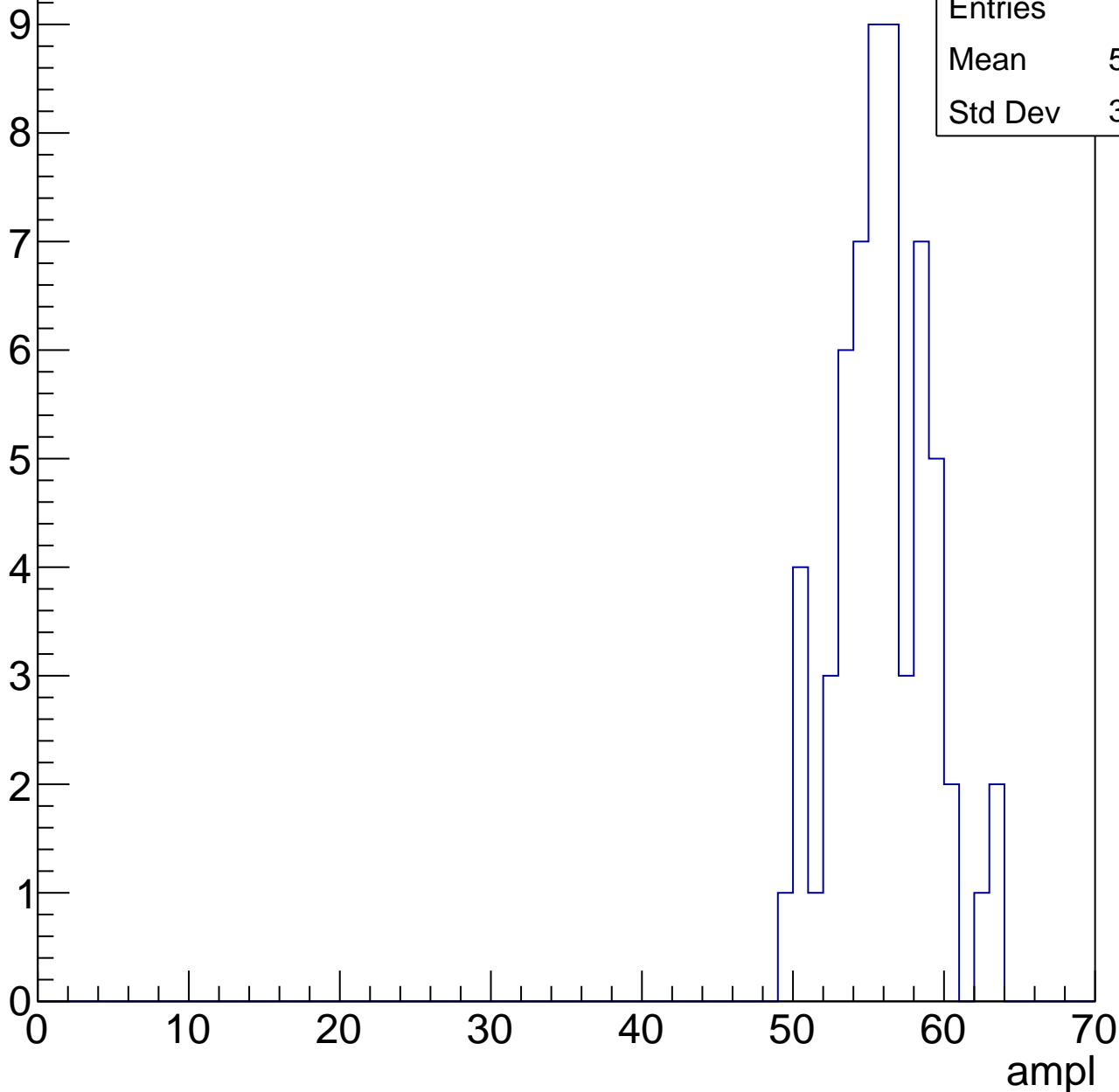


B1L103S, U9-ch35, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	55.52
Std Dev	3.122

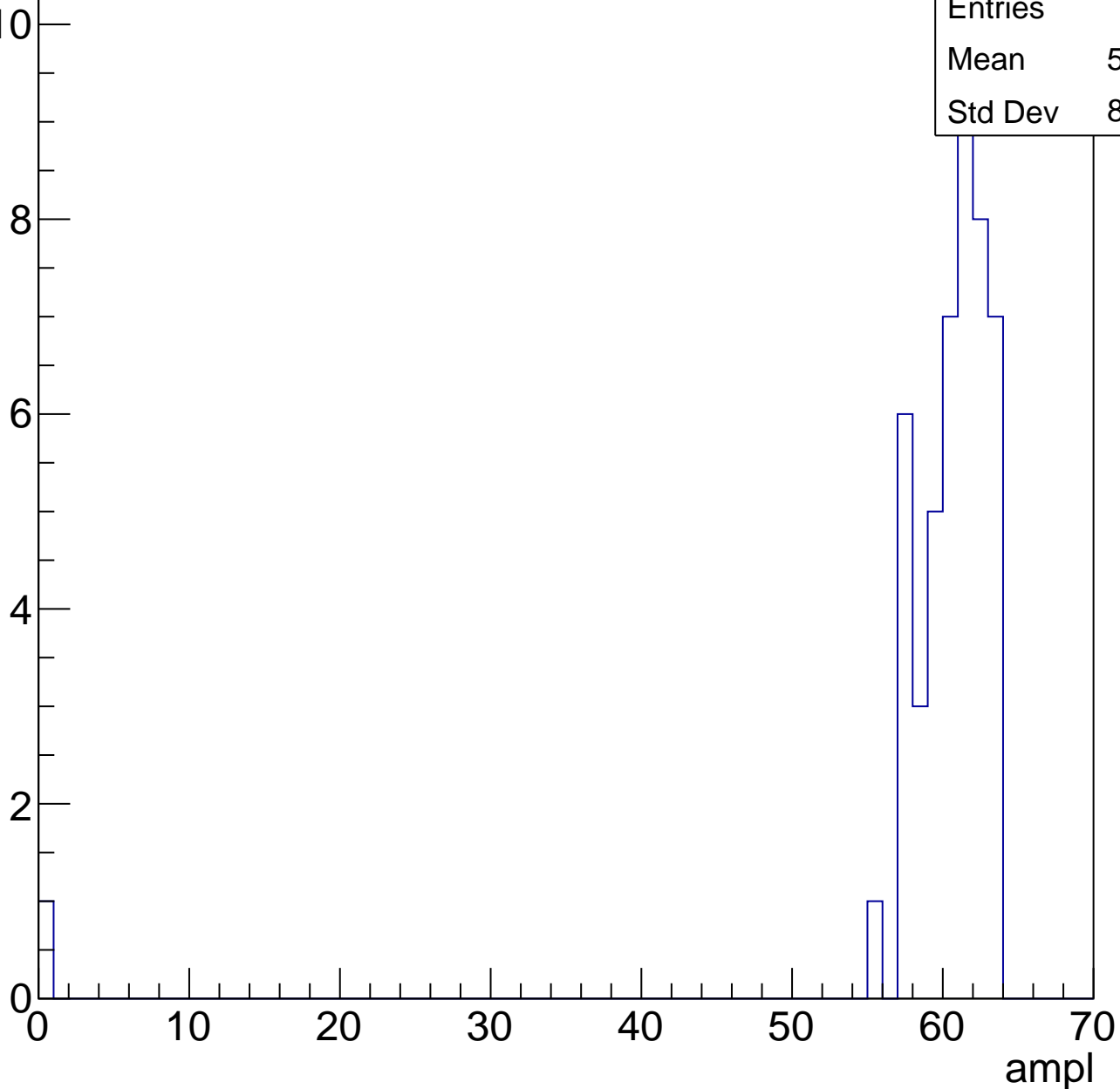


B1L103S, U9-ch35, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

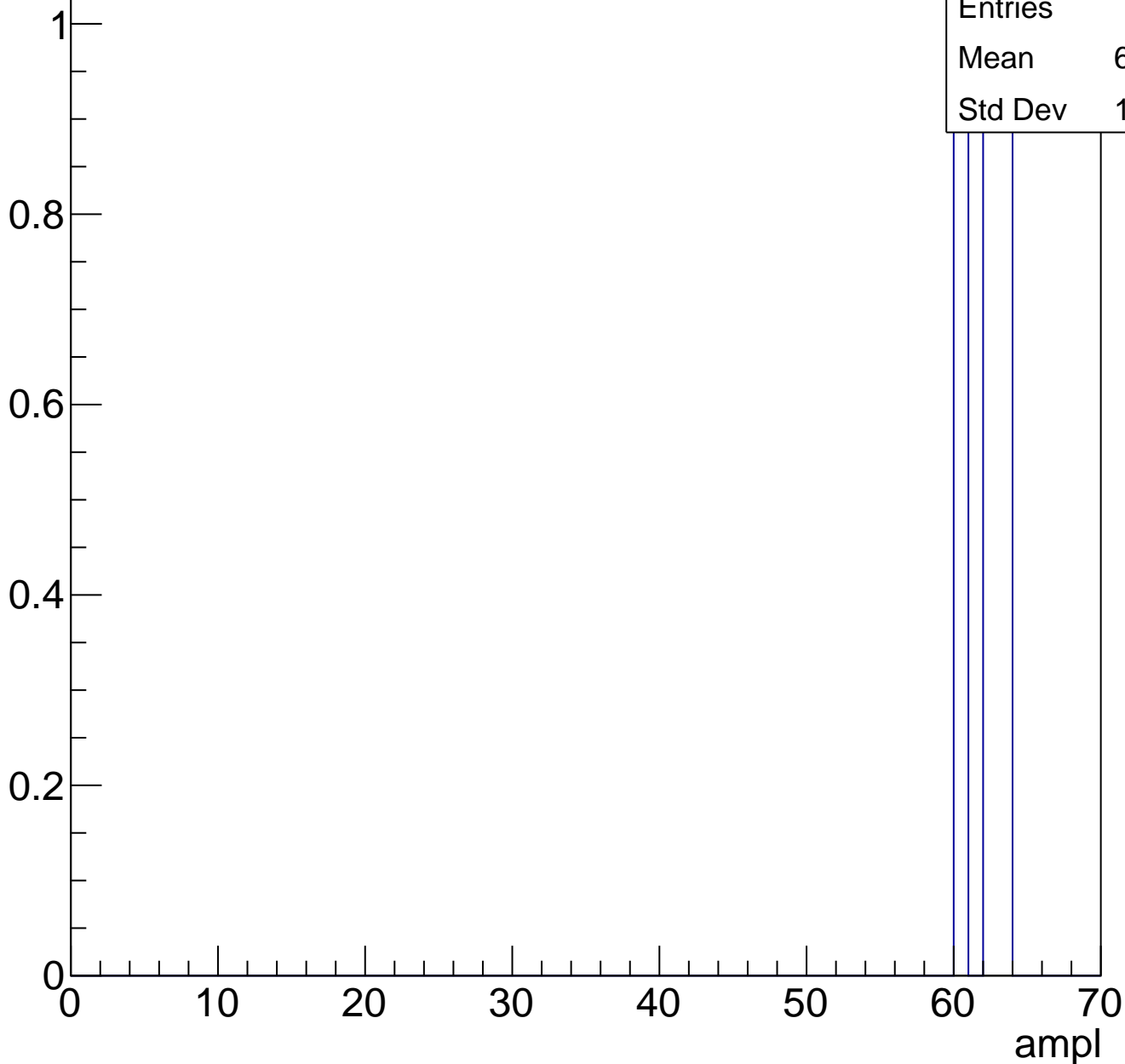
Entries	48
Mean	59.02
Std Dev	8.845



B1L103S, U9-ch35, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch35, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

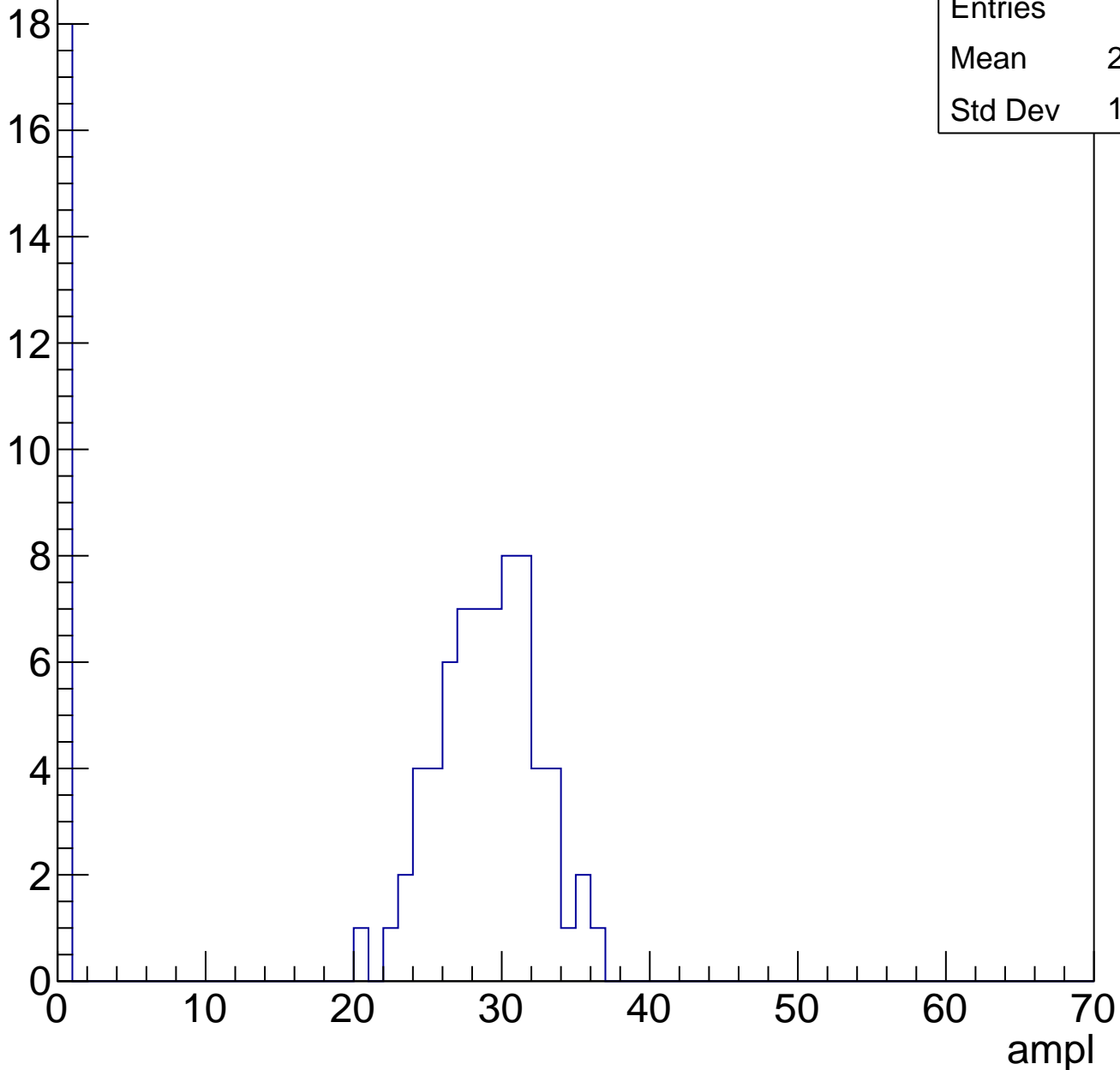


B1L103S, U9-ch36, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	85
Mean	22.54
Std Dev	12.05

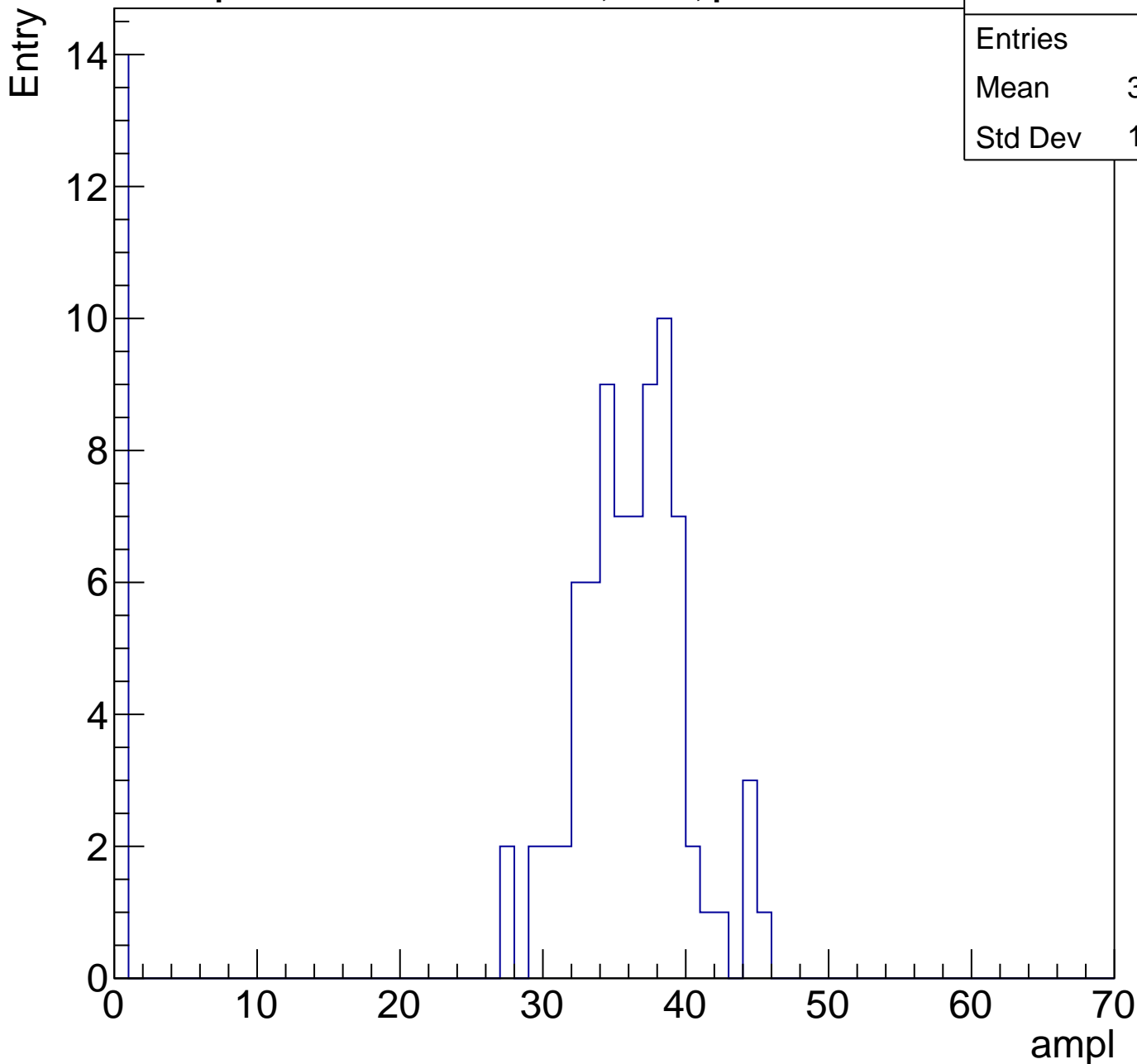
Entry



B1L103S, U9-ch36, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	91
Mean	30.25
Std Dev	13.34

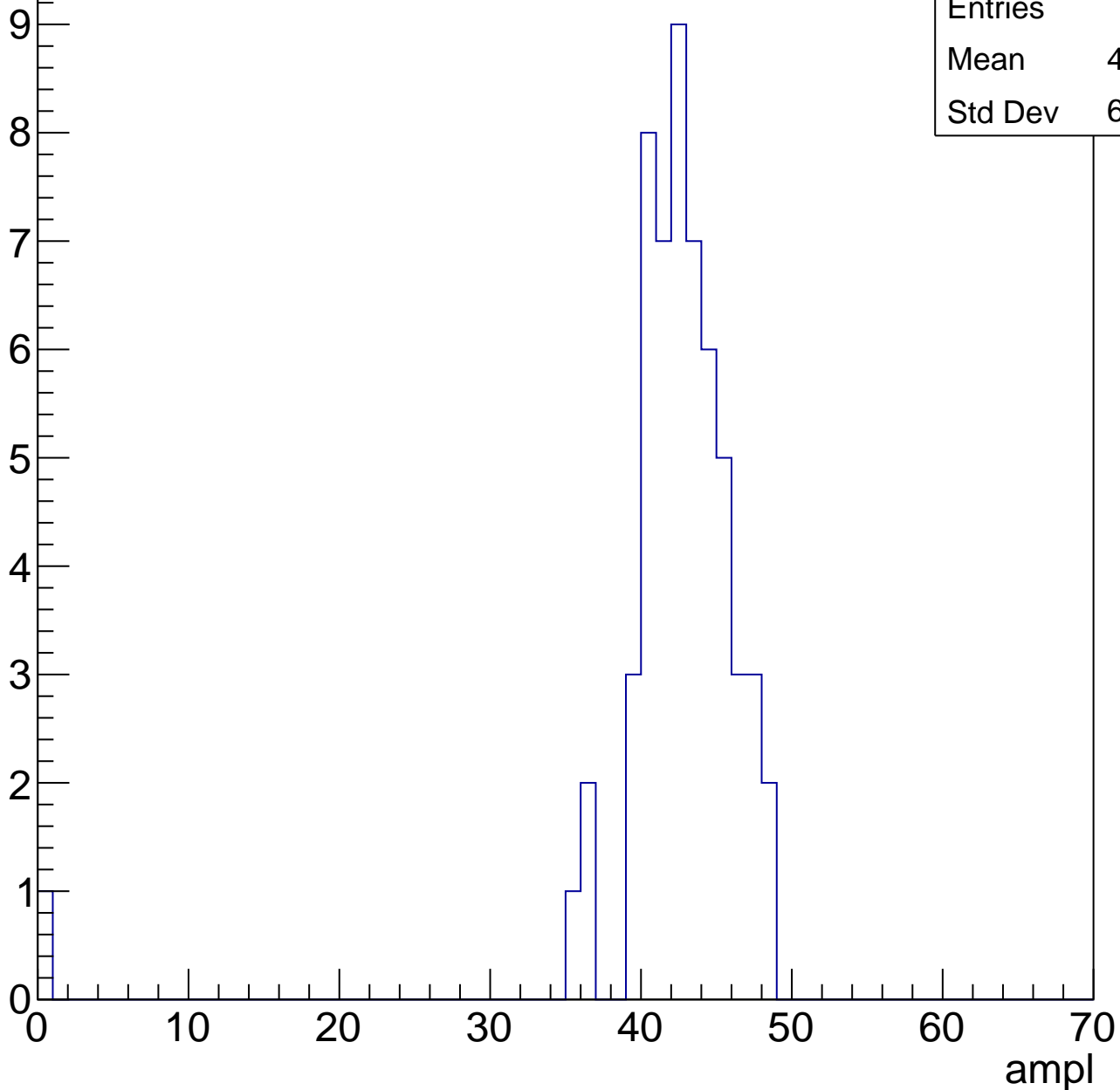


B1L103S, U9-ch36, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	41.65
Std Dev	6.234



B1L103S, U9-ch36, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	58
Mean	47.1
Std Dev	7.153

Entry

10

8

6

4

2

0

0

10

20

30

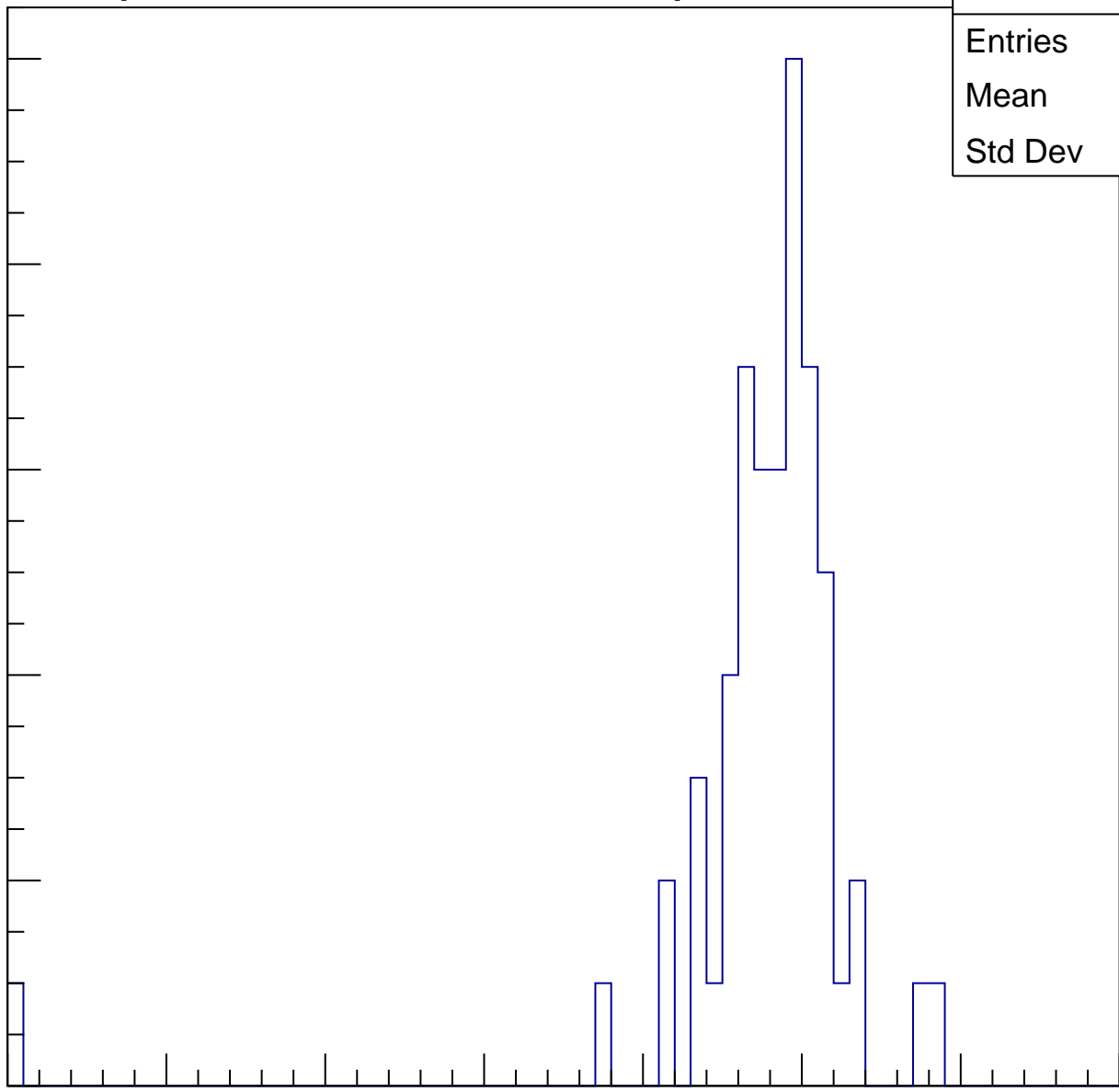
40

50

60

70

ampl

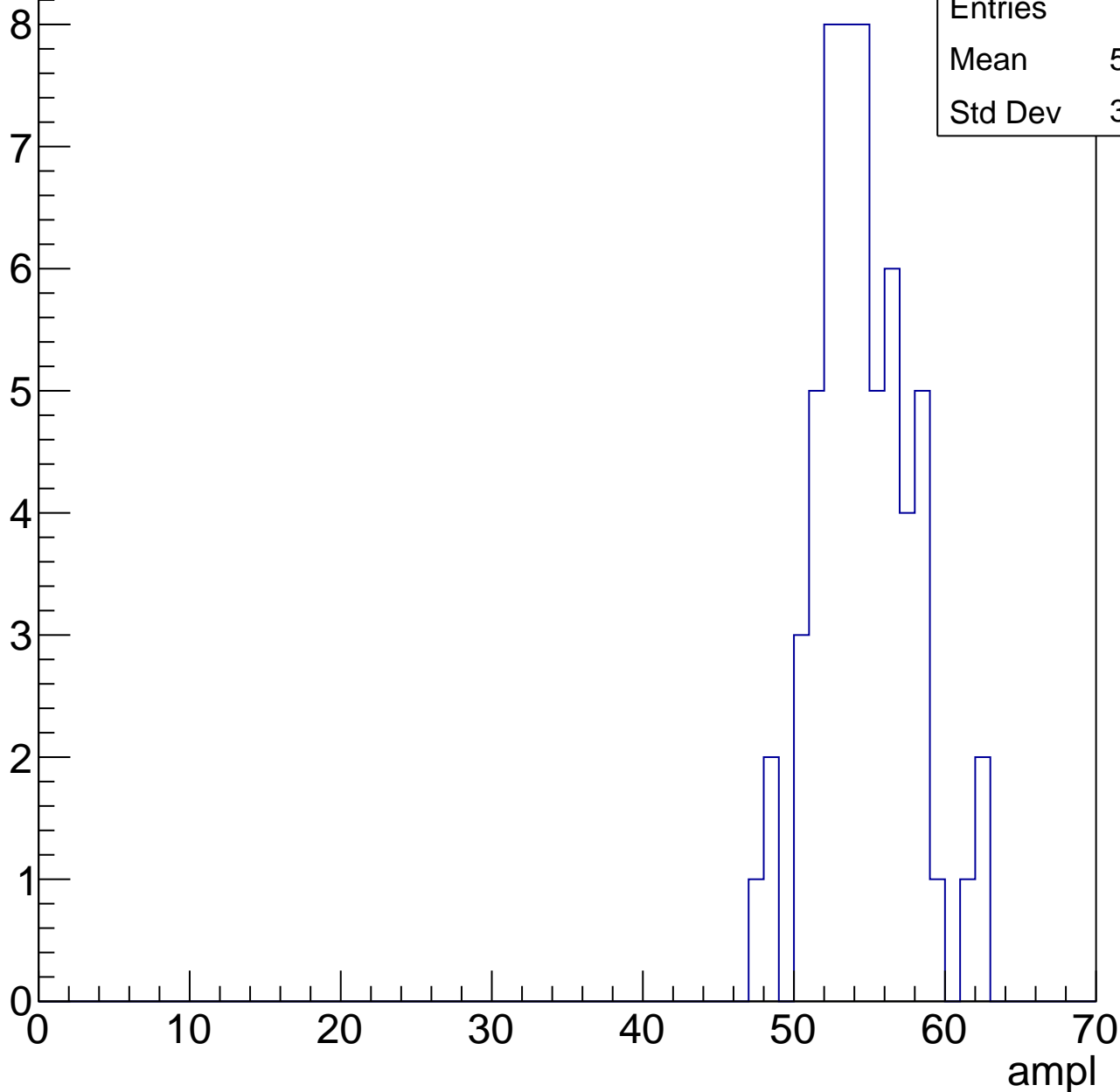


B1L103S, U9-ch36, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	54.12
Std Dev	3.189

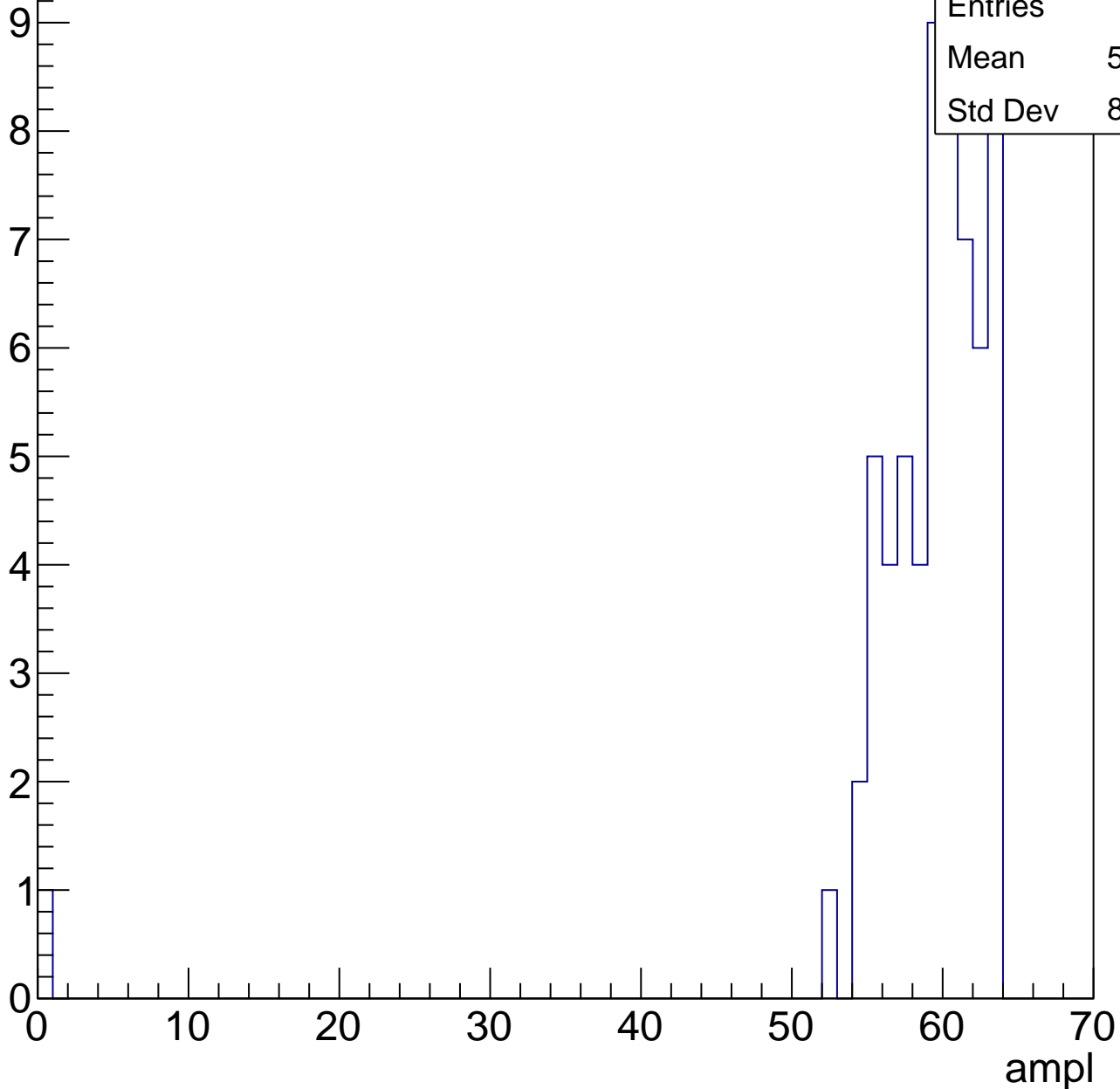


B1L103S, U9-ch36, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

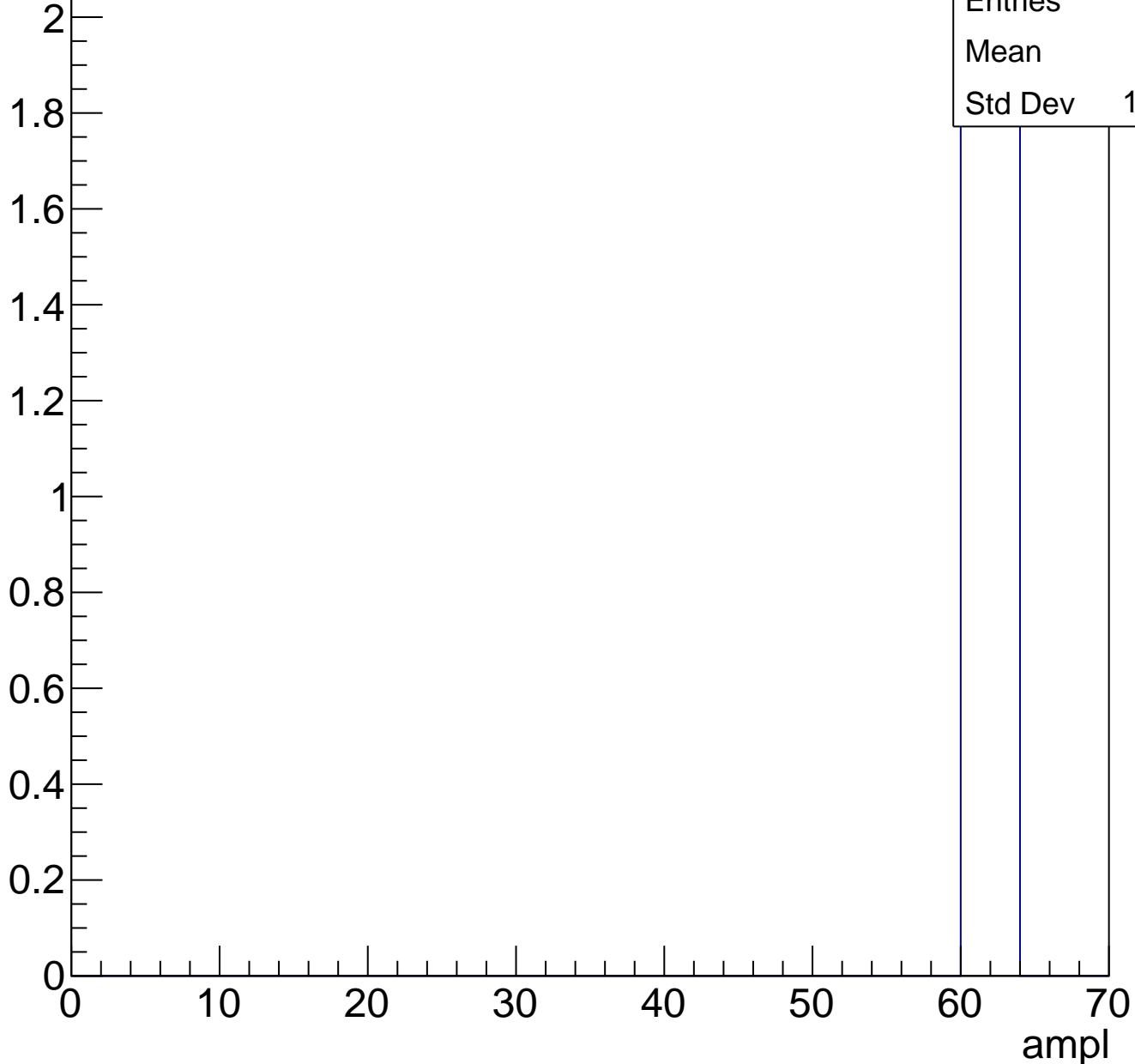
Entries	60
Mean	58.17
Std Dev	8.058



B1L103S, U9-ch36, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

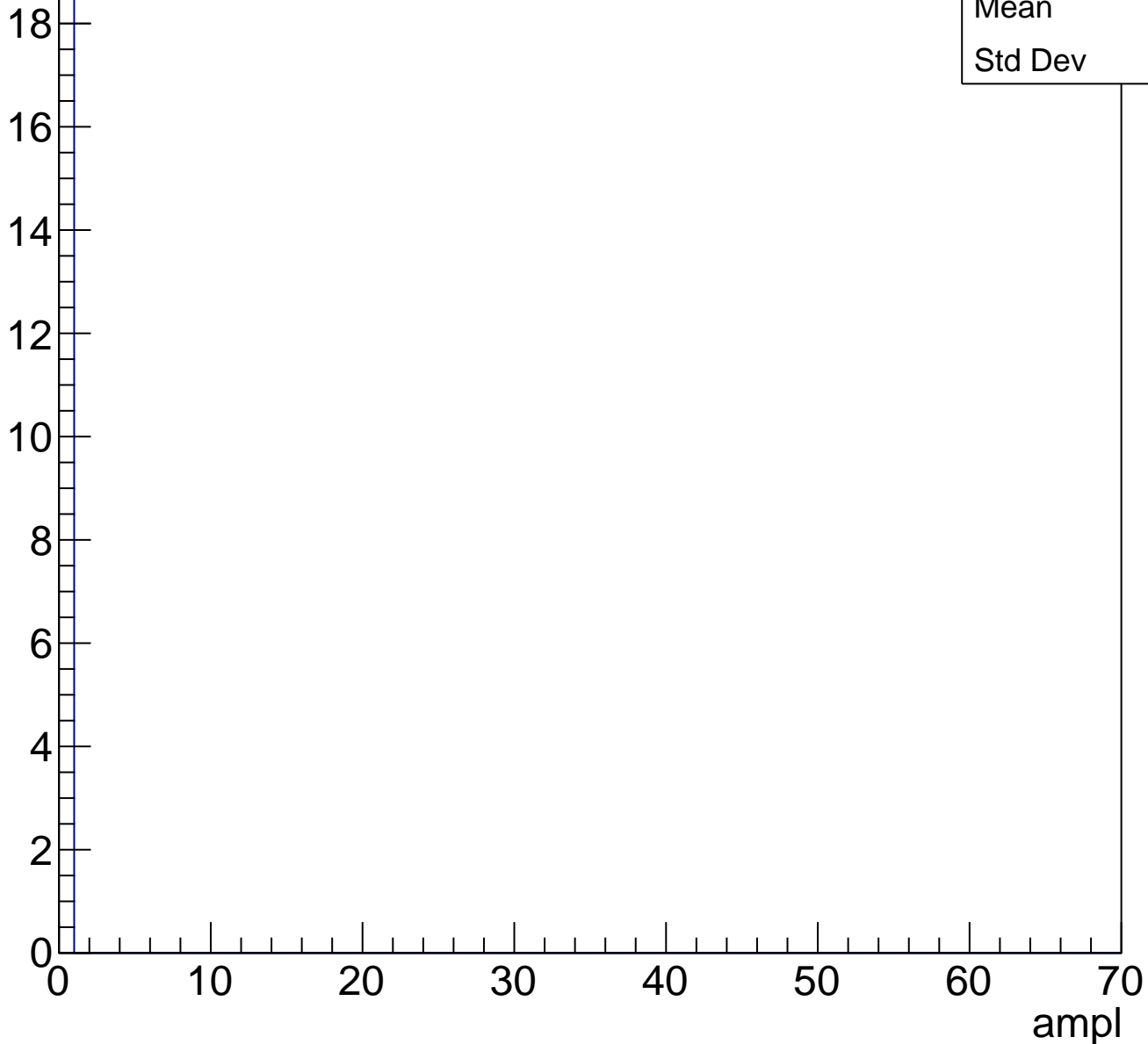


B1L103S, U9-ch36, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	0
Std Dev	0

Entry



B1L103S, U9-ch37, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	28.18
Std Dev	9.171

Entry

10

8

6

4

2

0

0

10

20

30

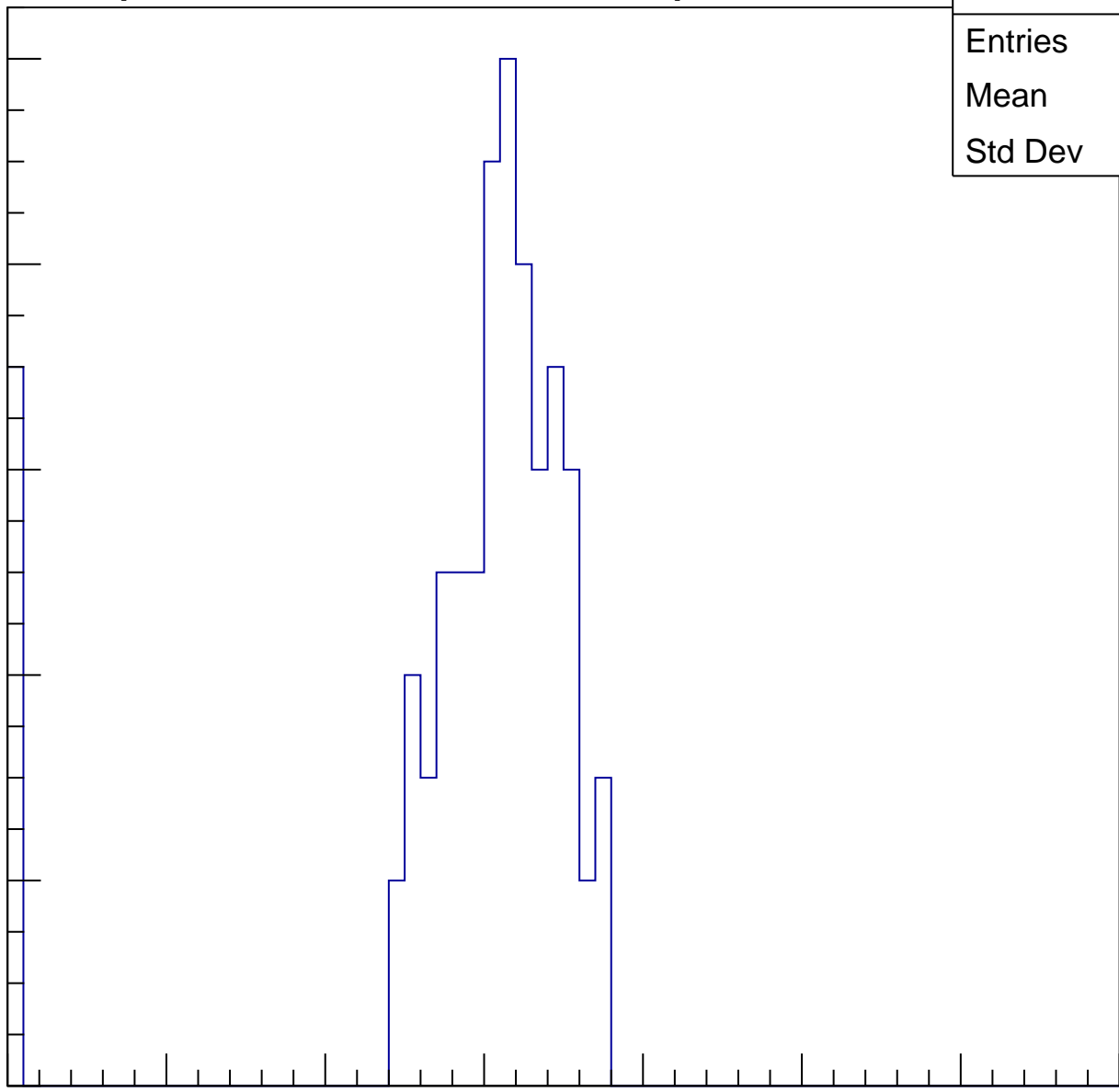
40

50

60

70

ampl

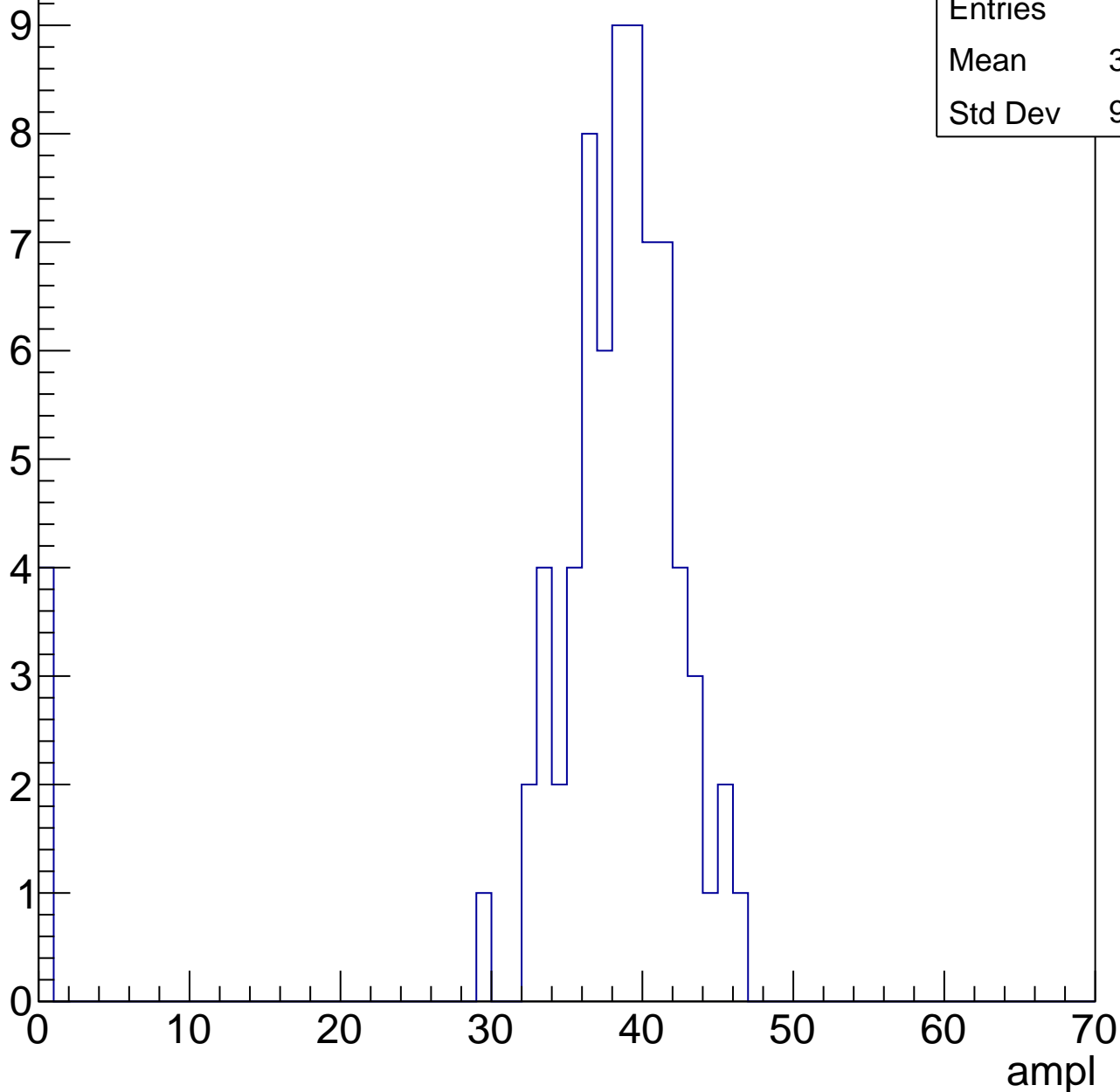


B1L103S, U9-ch37, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	36.22
Std Dev	9.254

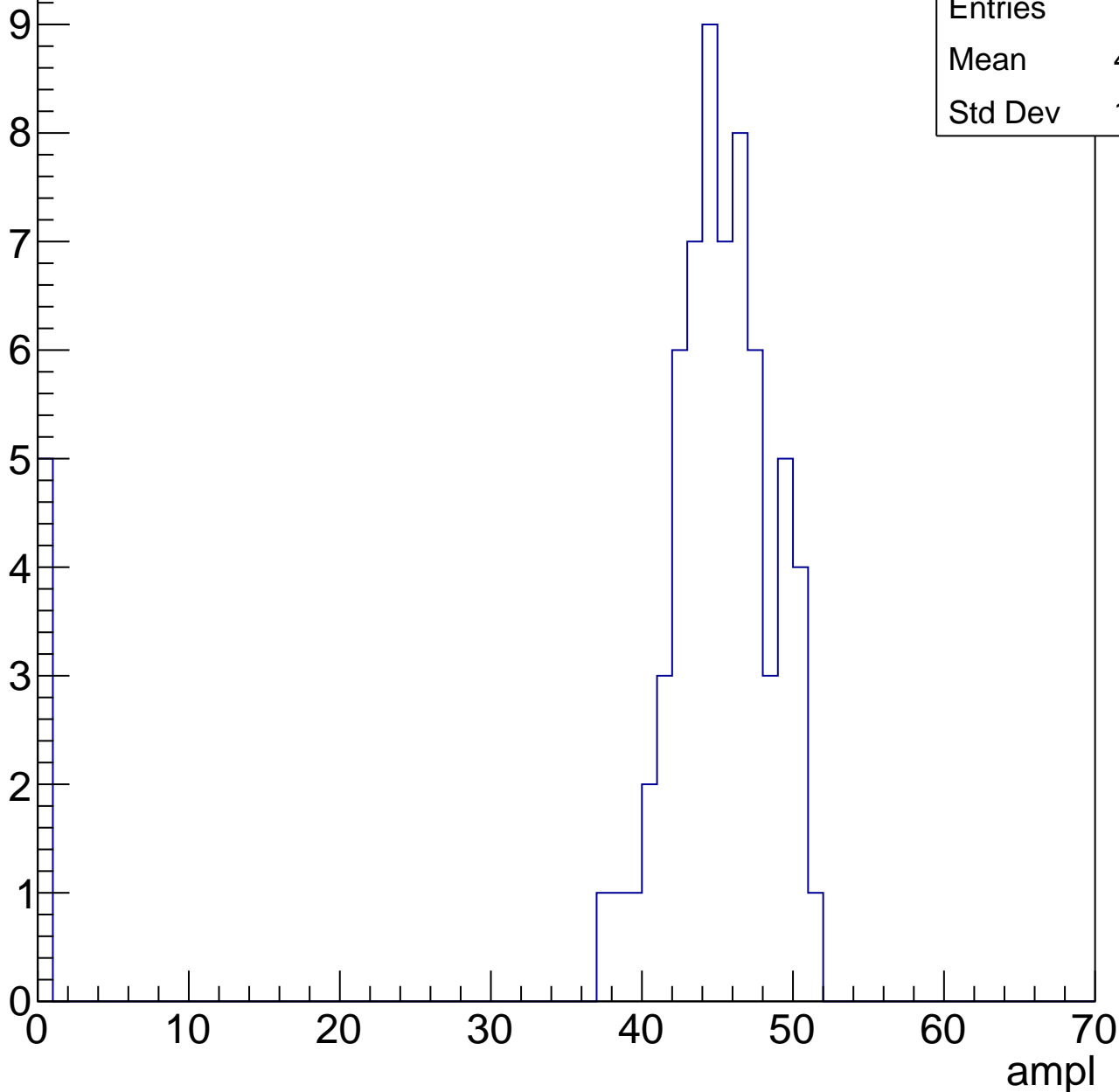


B1L103S, U9-ch37, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	41.61
Std Dev	12.01

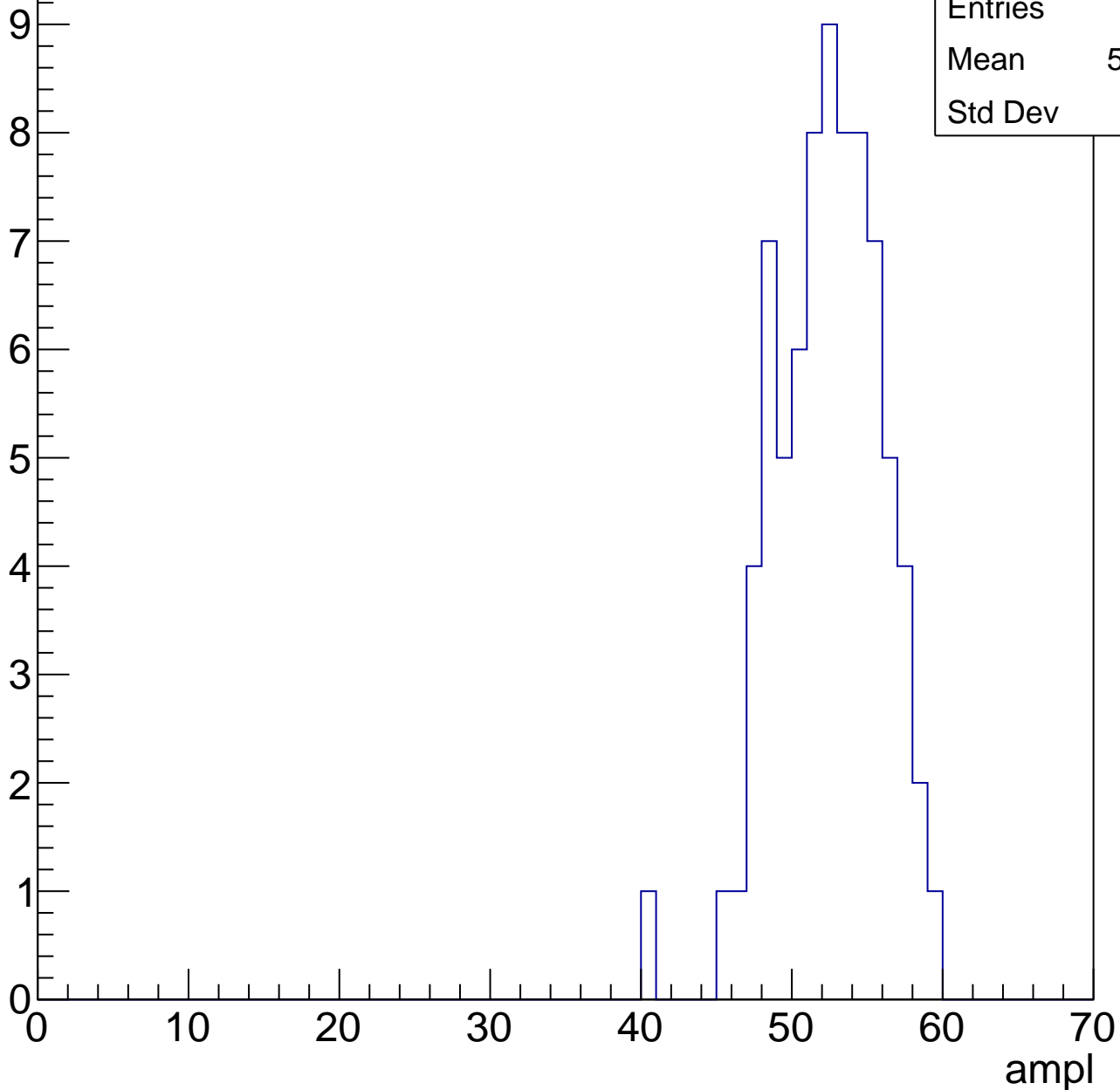


B1L103S, U9-ch37, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	51.95
Std Dev	3.46

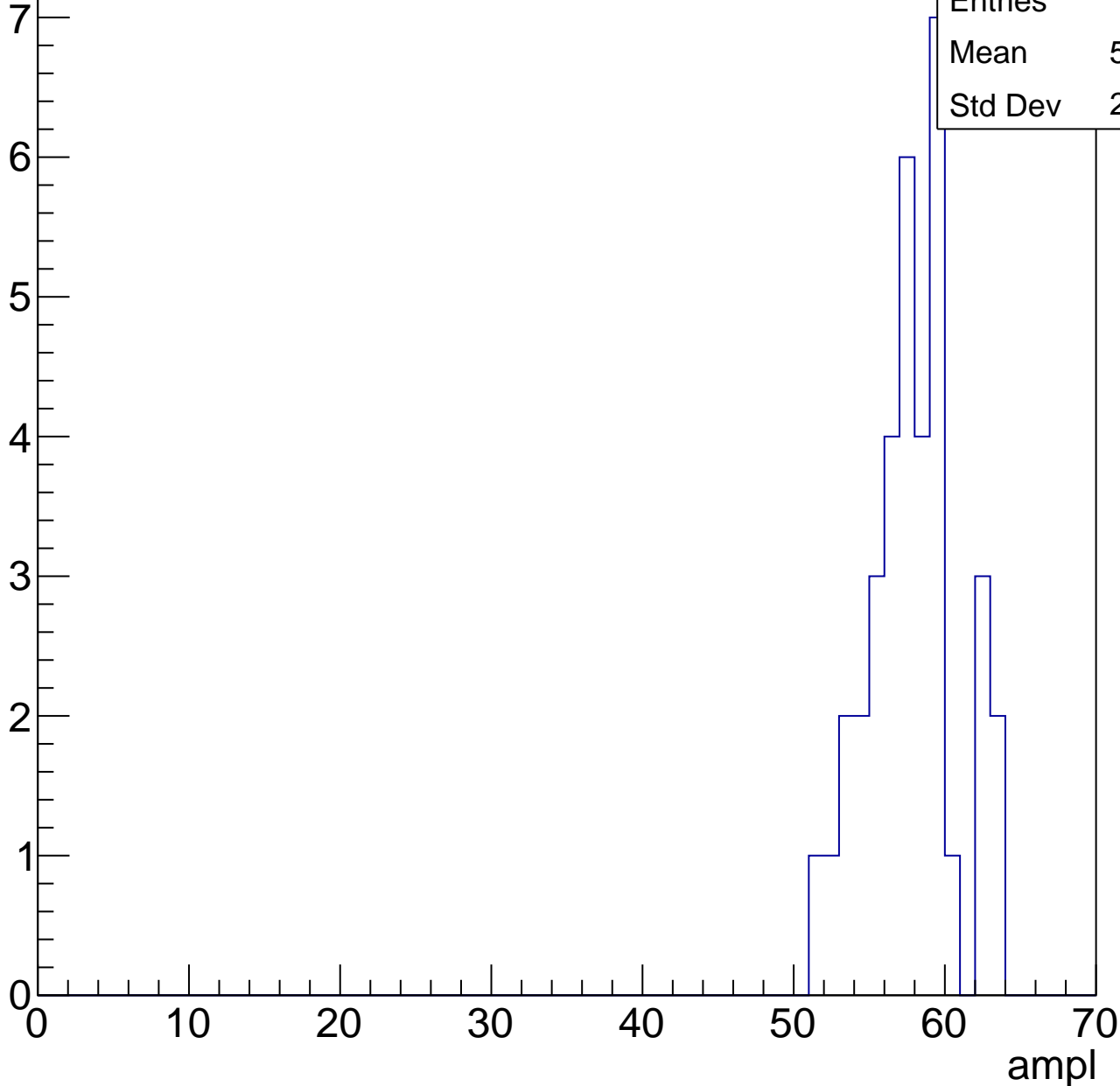


B1L103S, U9-ch37, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	36
Mean	57.36
Std Dev	2.936

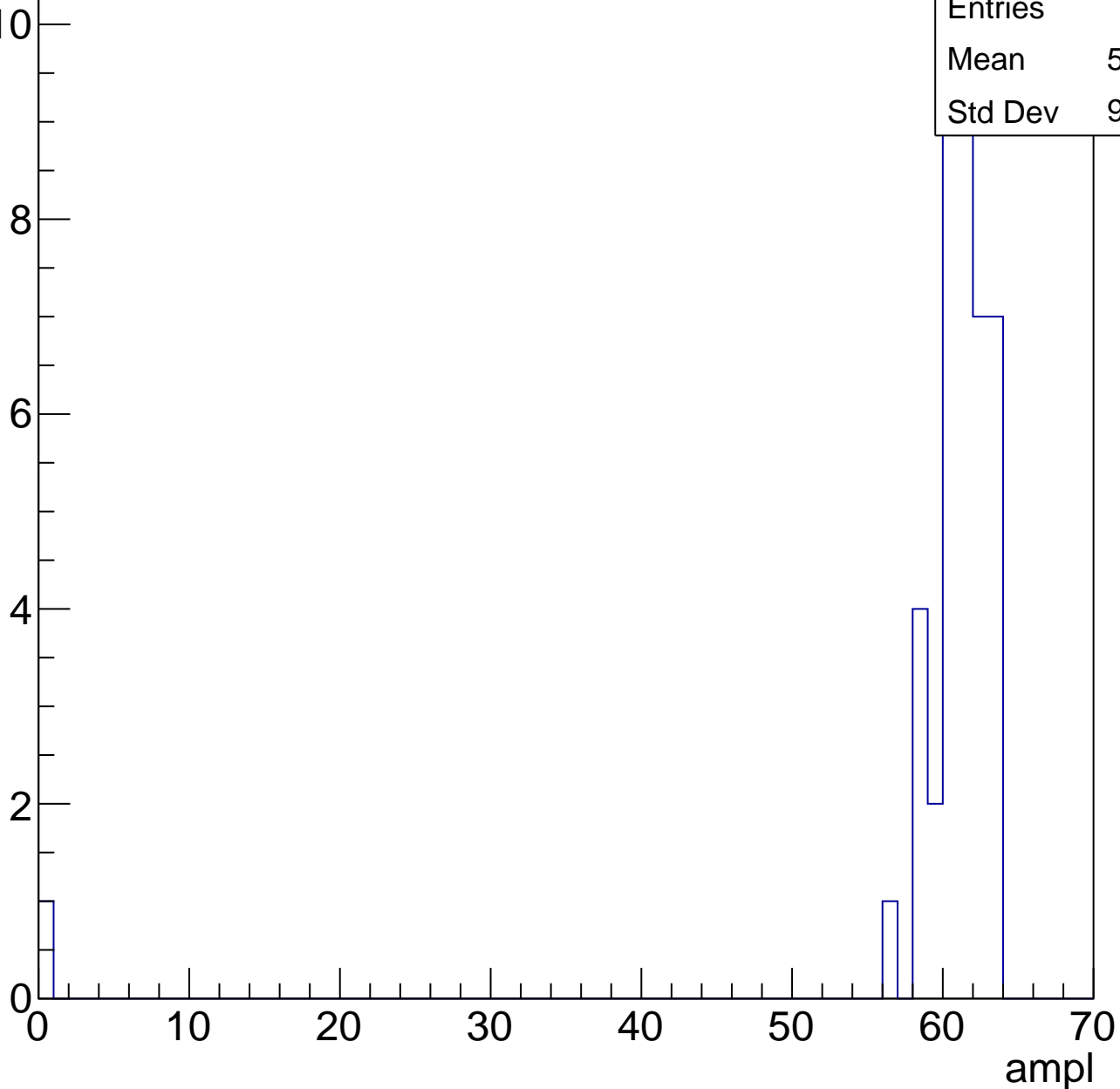


B1L103S, U9-ch37, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

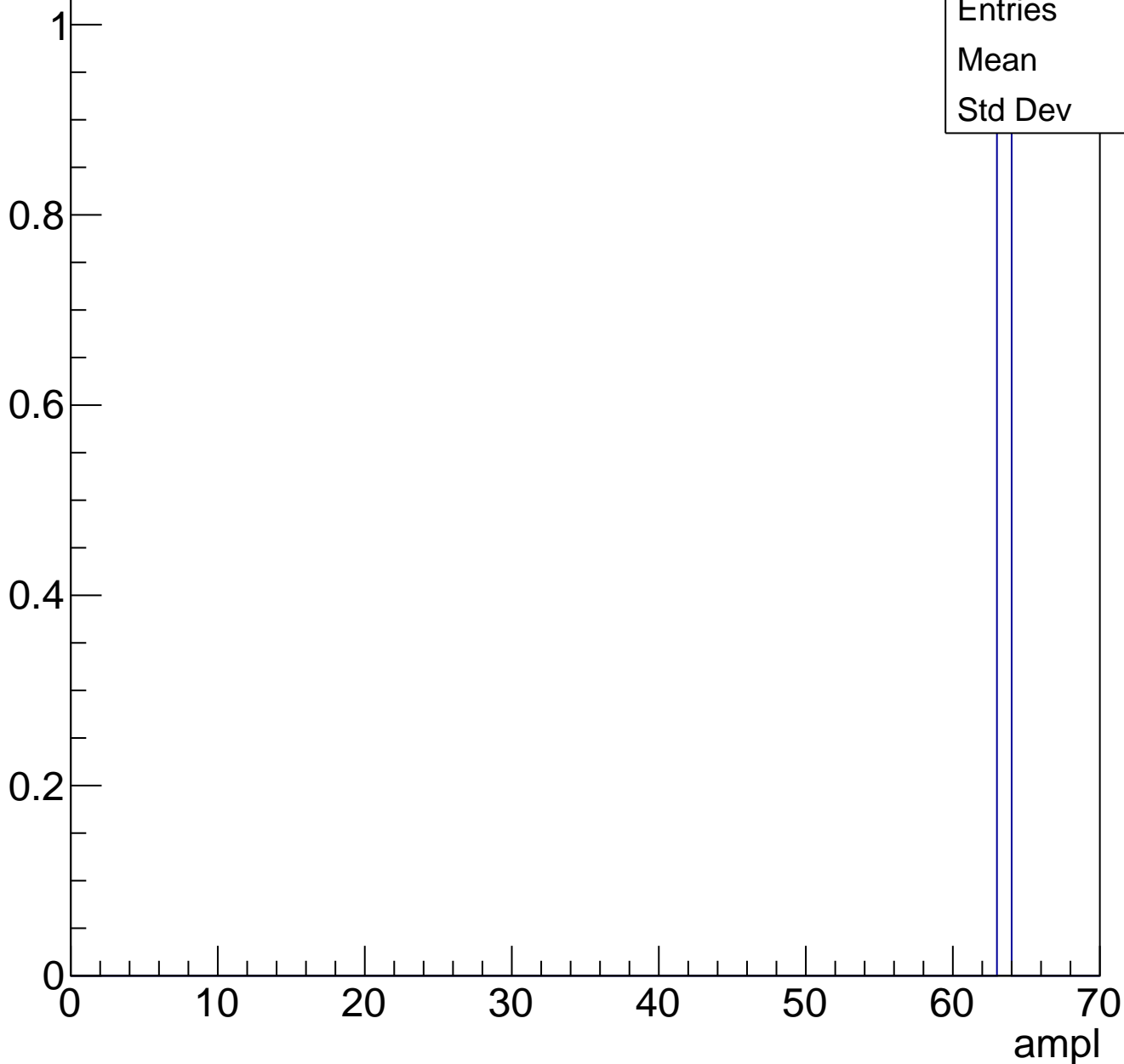
Entries	41
Mean	59.29
Std Dev	9.518



B1L103S, U9-ch37, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch37, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

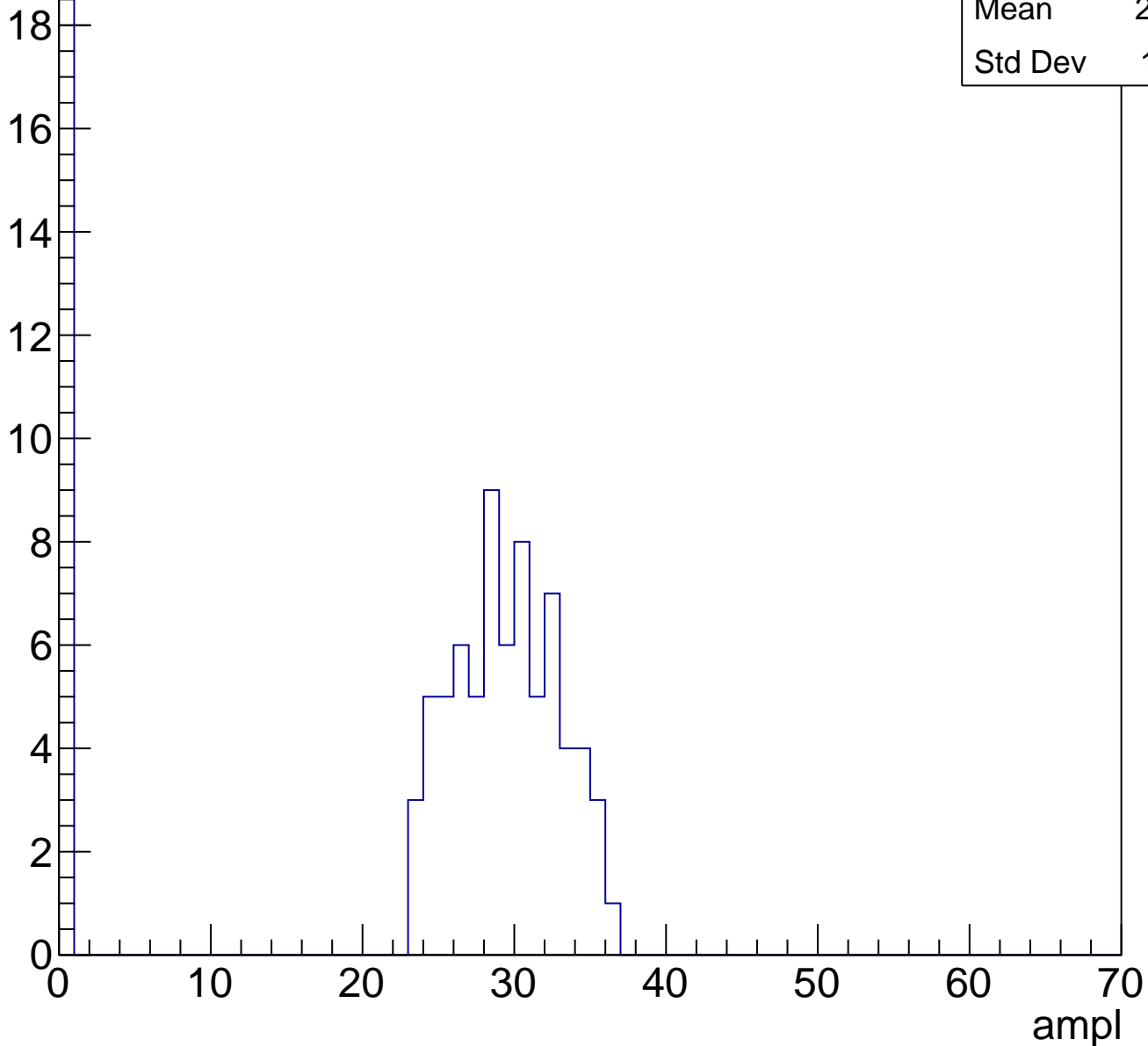
ampl

B1L103S, U9-ch38, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	90
Mean	22.88
Std Dev	12.21

Entry

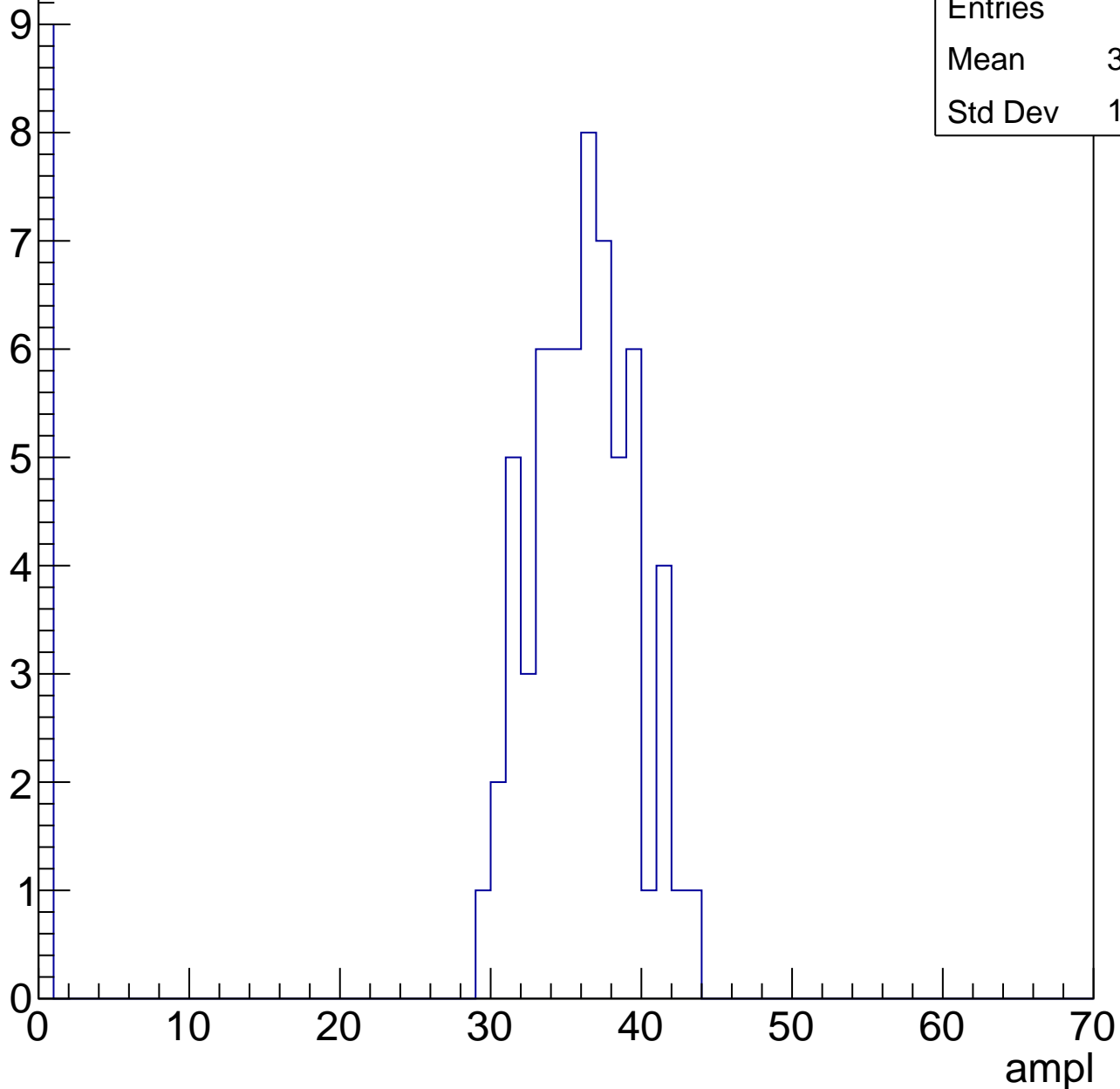


B1L103S, U9-ch38, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	31.15
Std Dev	12.25

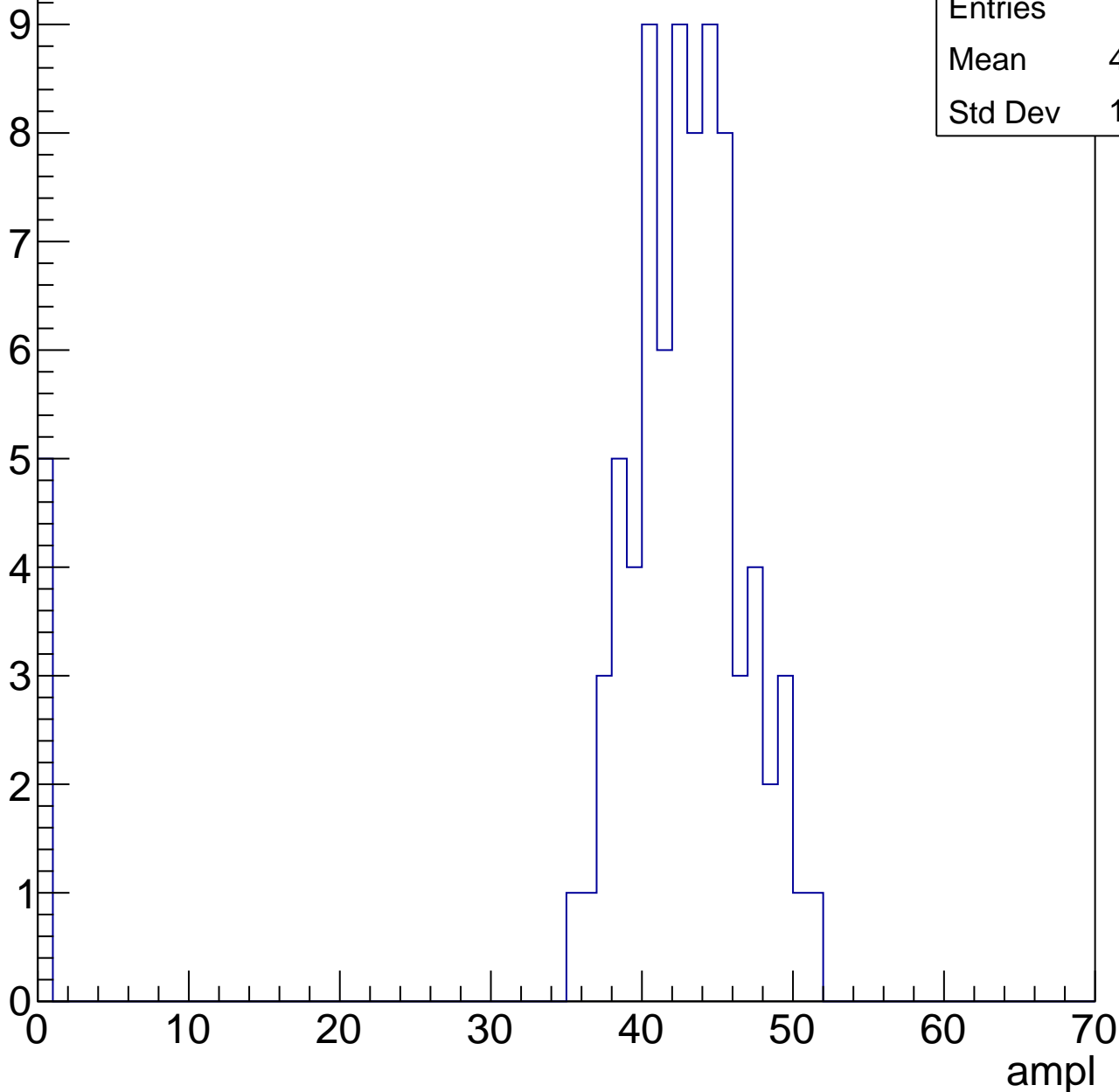


B1L103S, U9-ch38, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	82
Mean	40.02
Std Dev	10.73

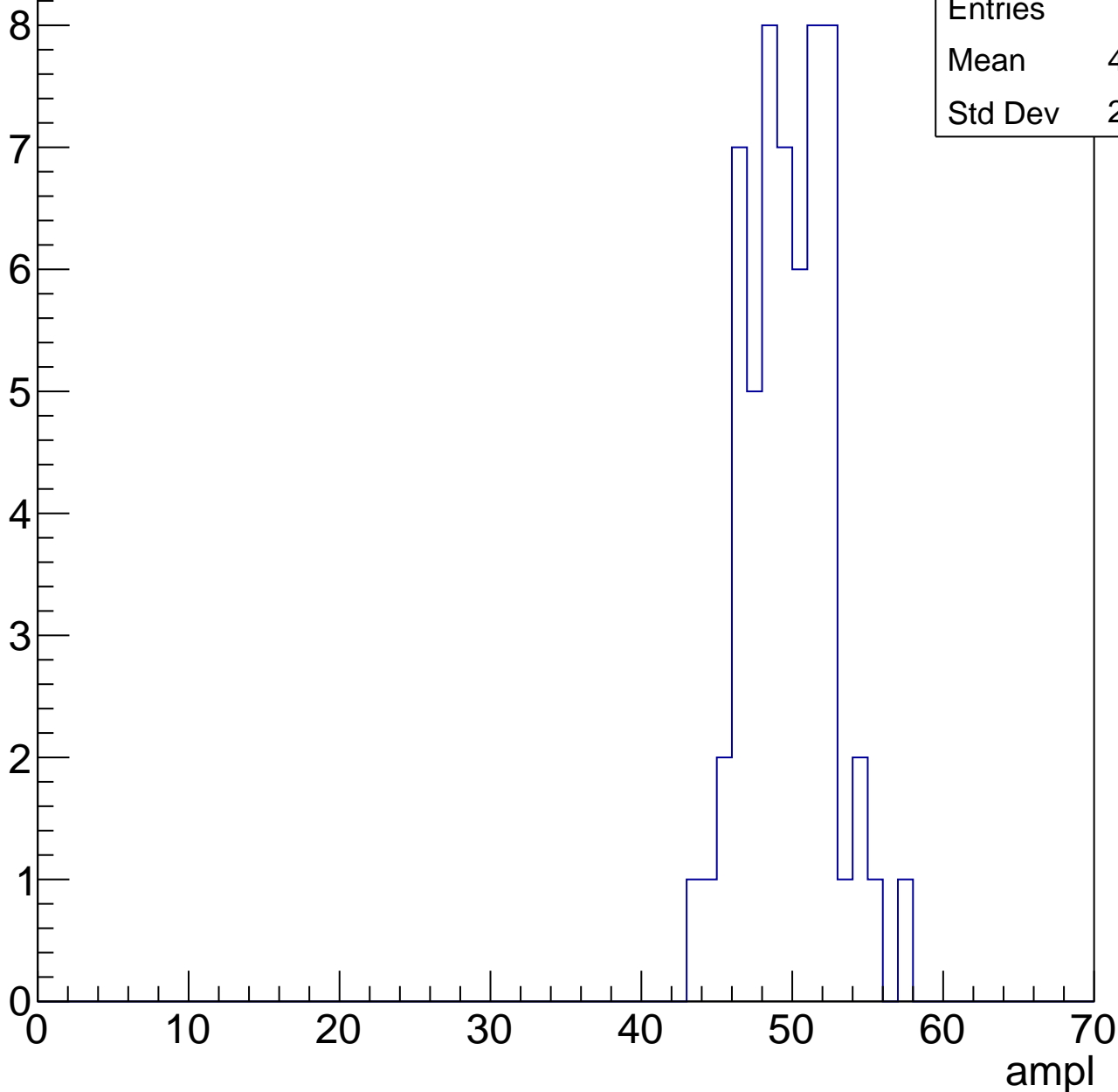


B1L103S, U9-ch38, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	49.28
Std Dev	2.803

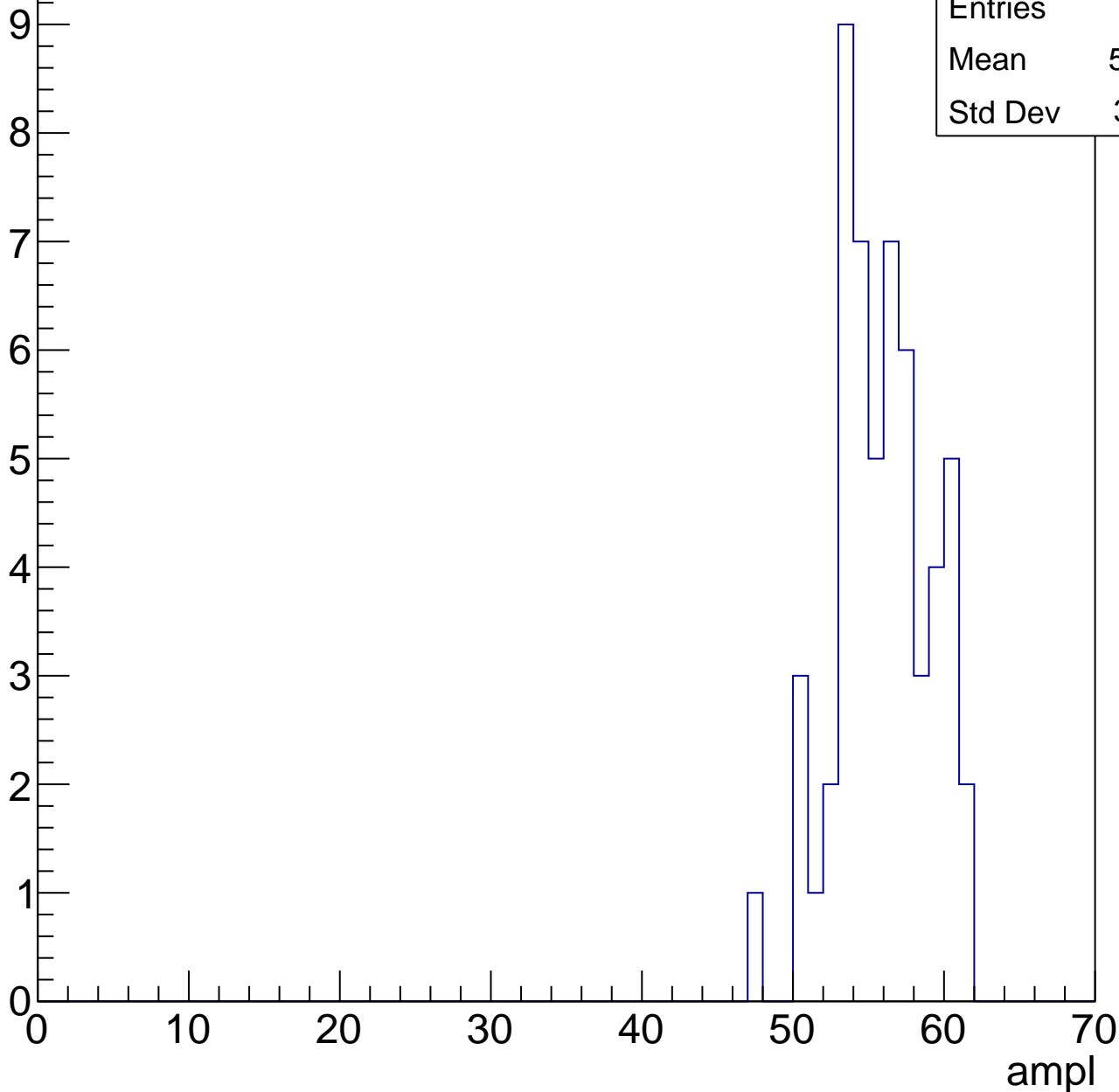


B1L103S, U9-ch38, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	55.42
Std Dev	3.091

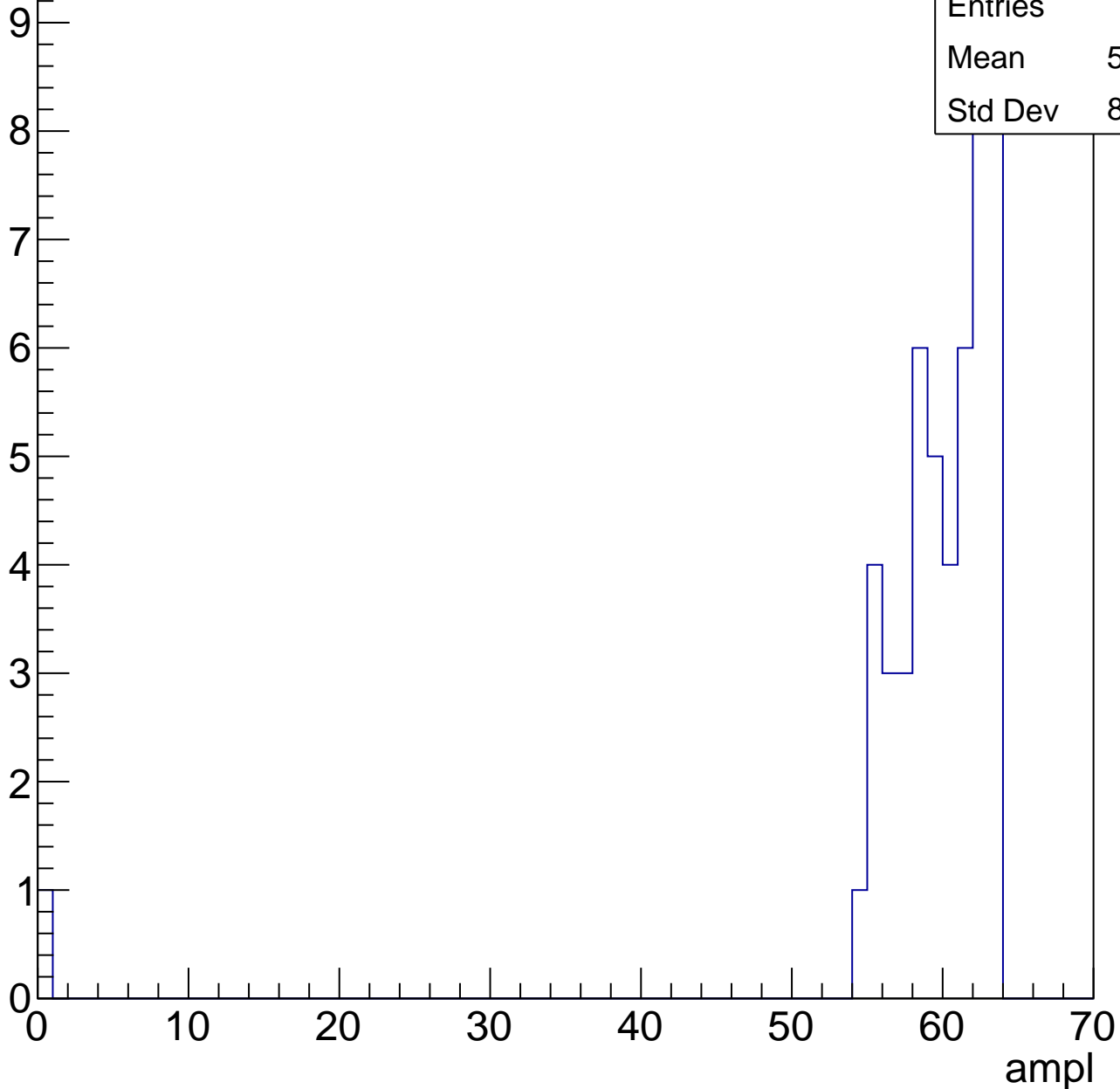


B1L103S, U9-ch38, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	58.57
Std Dev	8.698



B1L103S, U9-ch38, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	6
Mean	60.17
Std Dev	1.344

ampl

0 10 20 30 40 50 60 70

0

B1L103S, U9-ch38, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	20
Mean	3.15
Std Dev	13.73

ampl

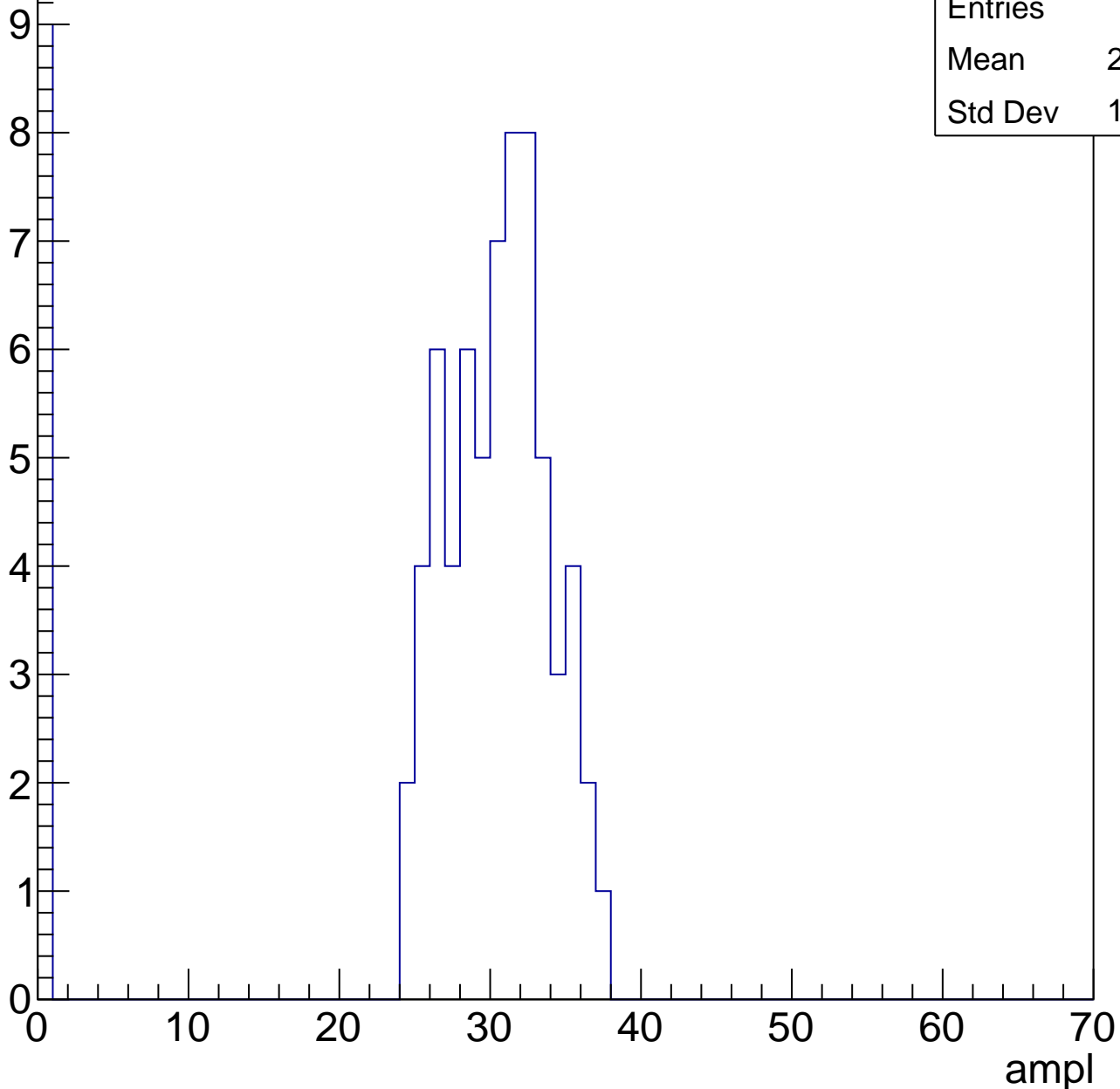
0 10 20 30 40 50 60 70

B1L103S, U9-ch39, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	26.42
Std Dev	10.29

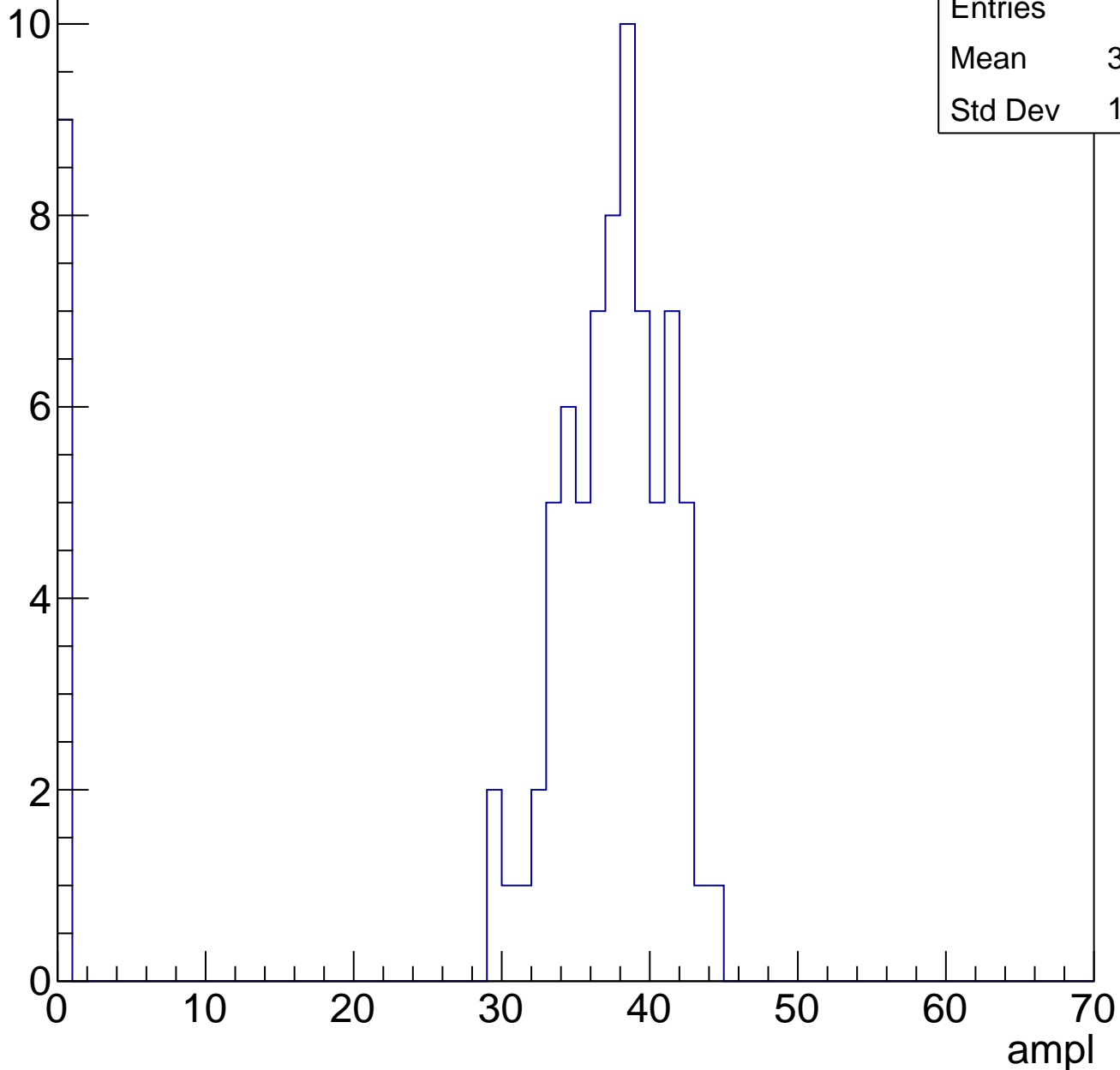


B1L103S, U9-ch39, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	33.07
Std Dev	12.04

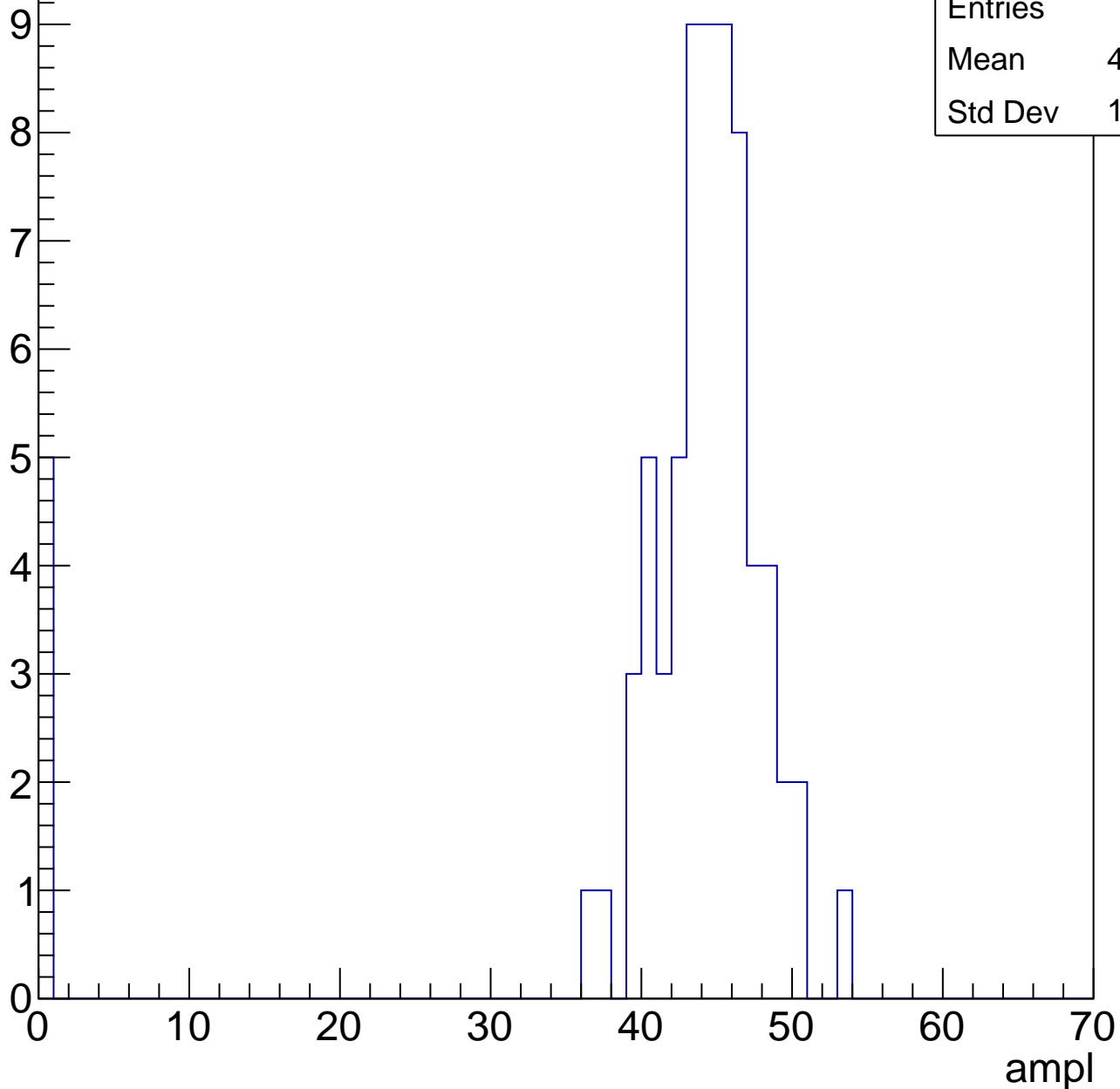
Entry



B1L103S, U9-ch39, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

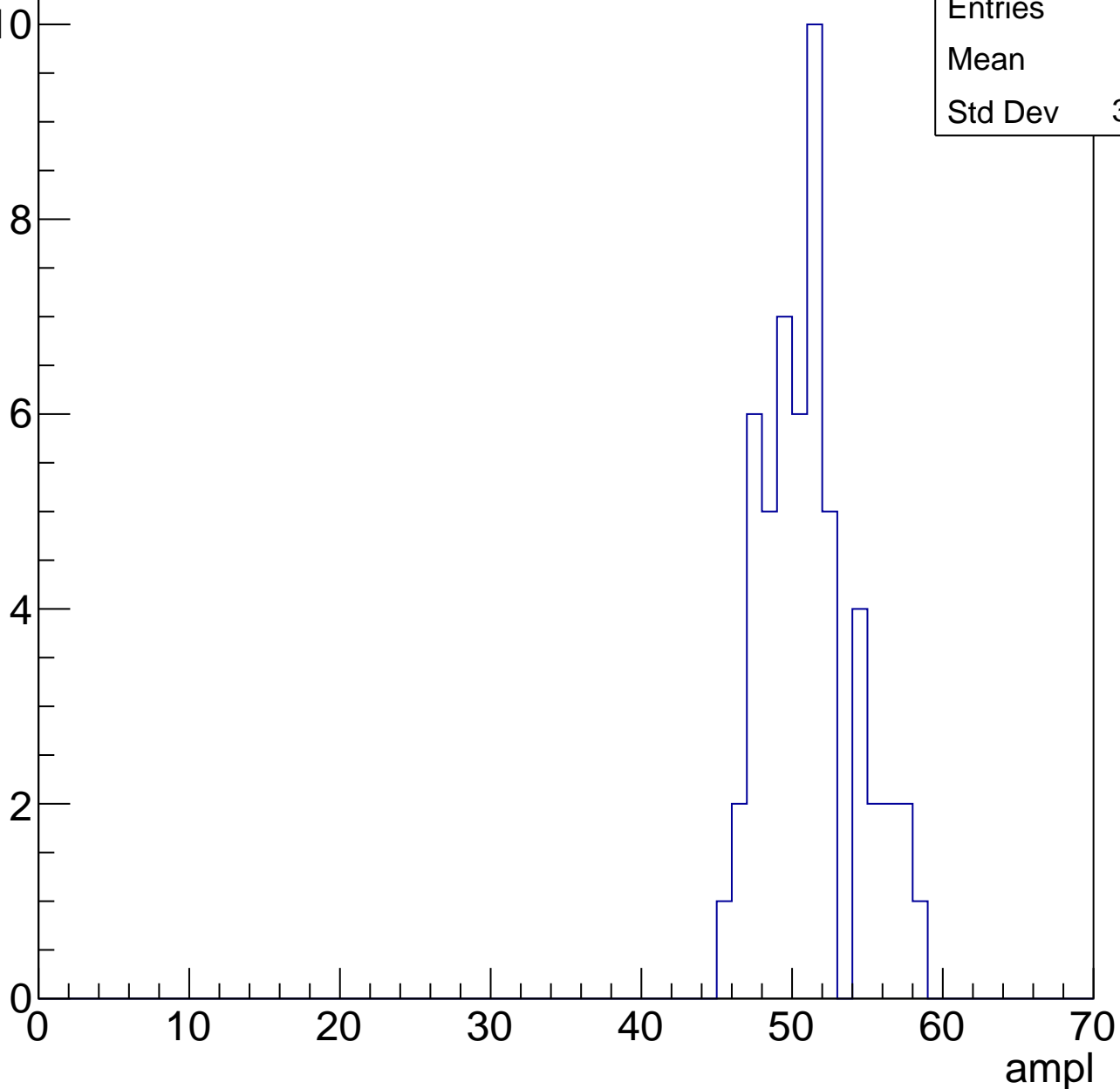


B1L103S, U9-ch39, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	50.6
Std Dev	3.061

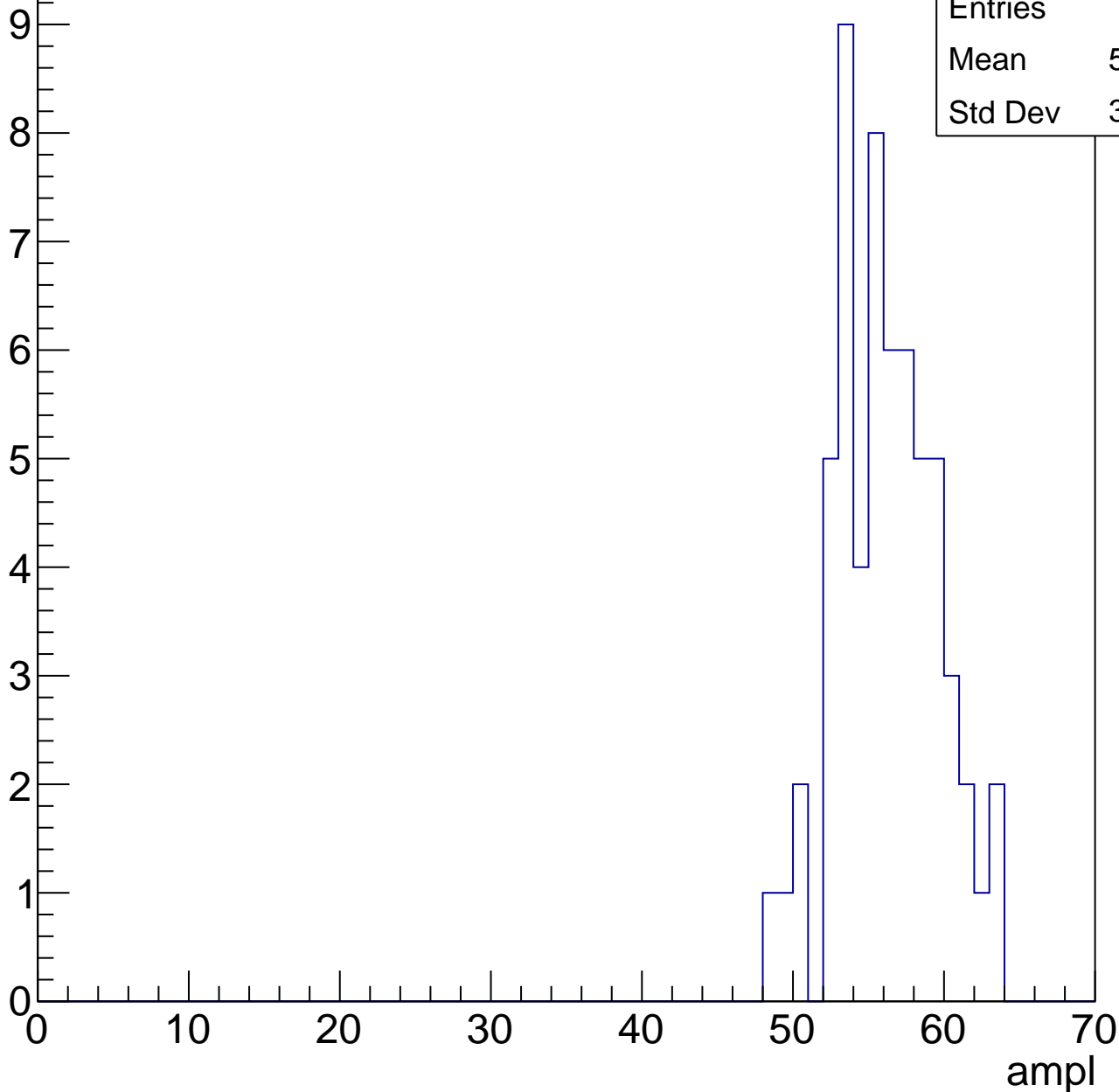


B1L103S, U9-ch39, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	55.72
Std Dev	3.337

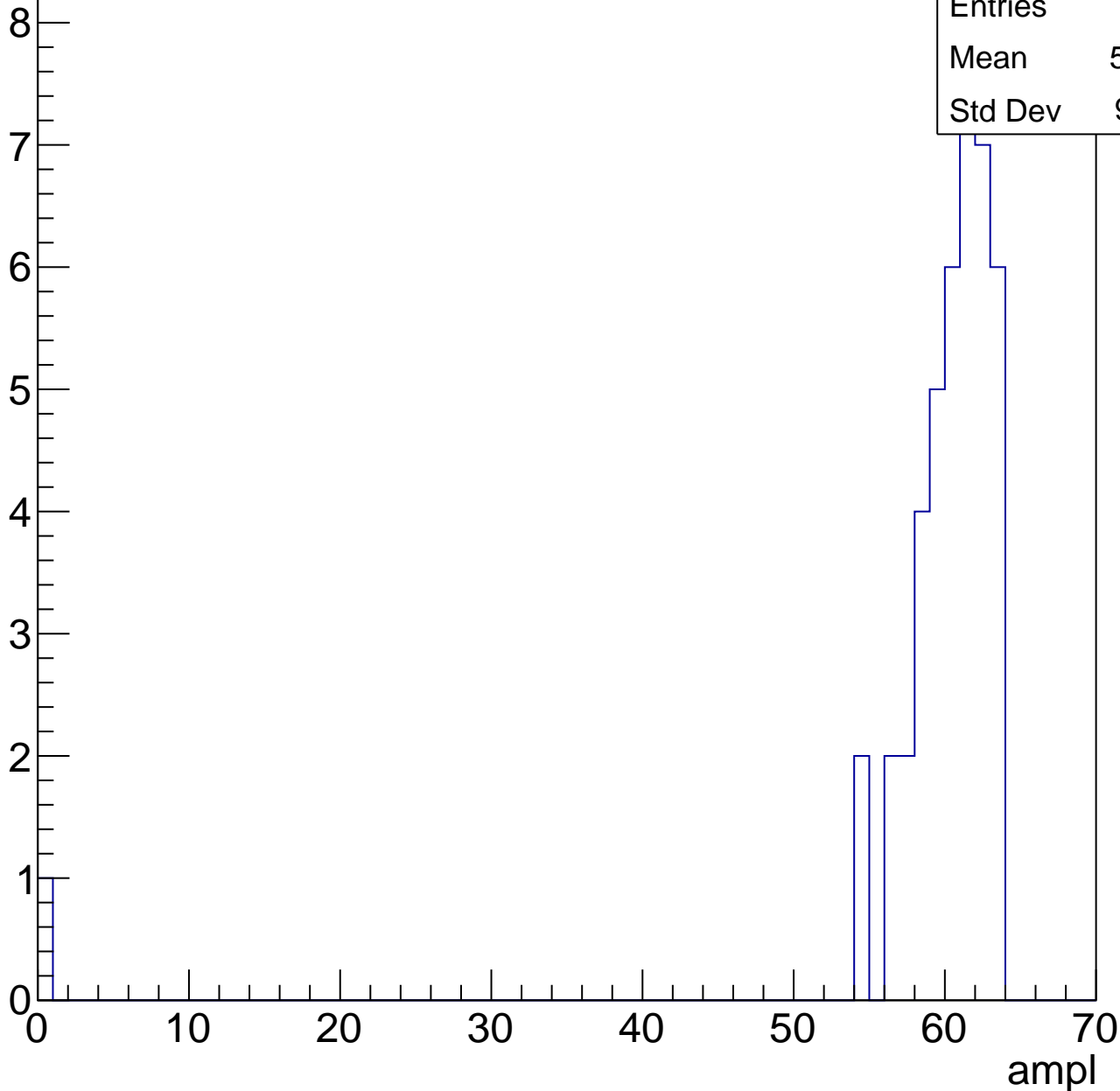


B1L103S, U9-ch39, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	43
Mean	58.63
Std Dev	9.341



B1L103S, U9-ch39, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

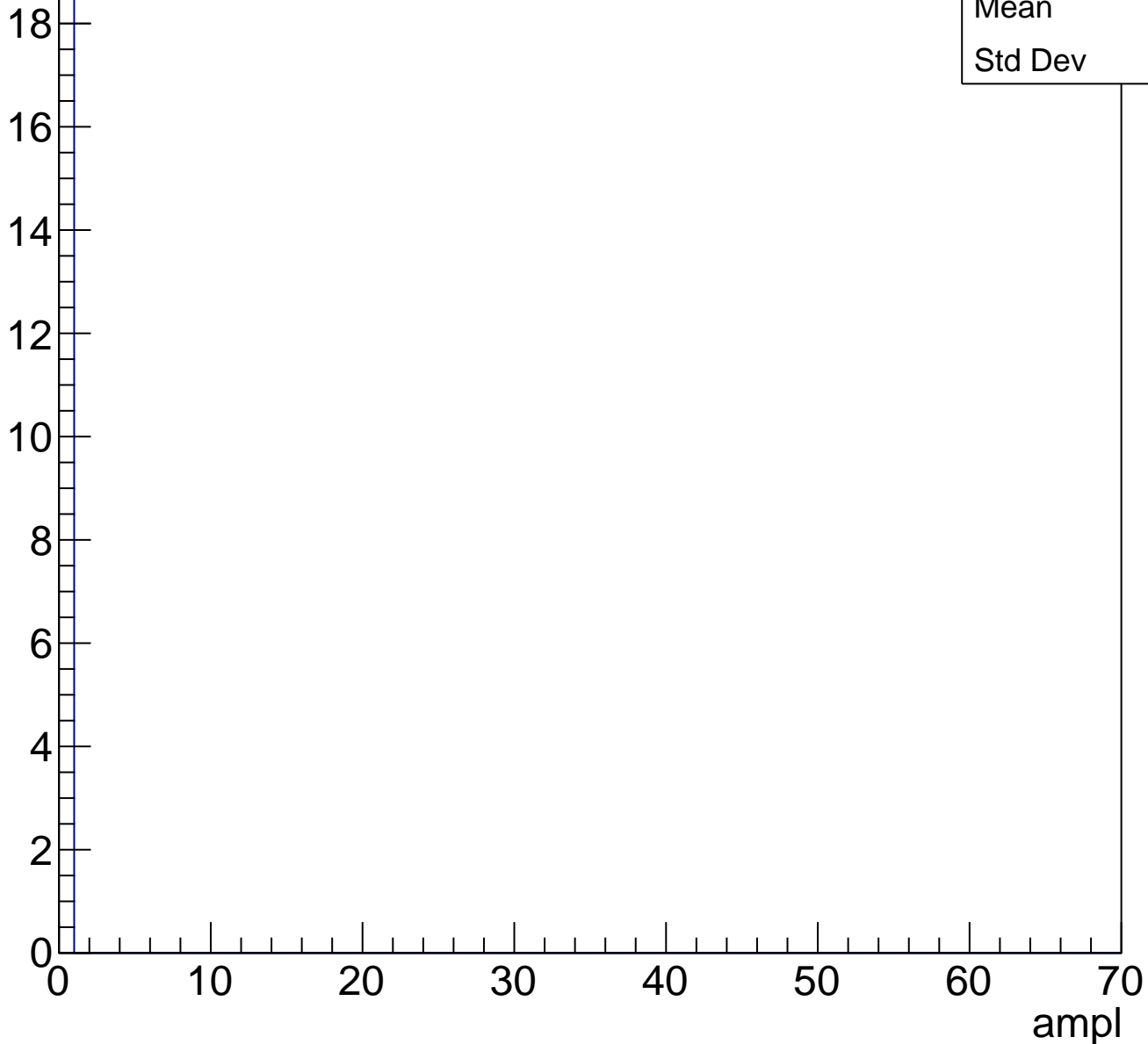


B1L103S, U9-ch39, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	0
Std Dev	0

Entry

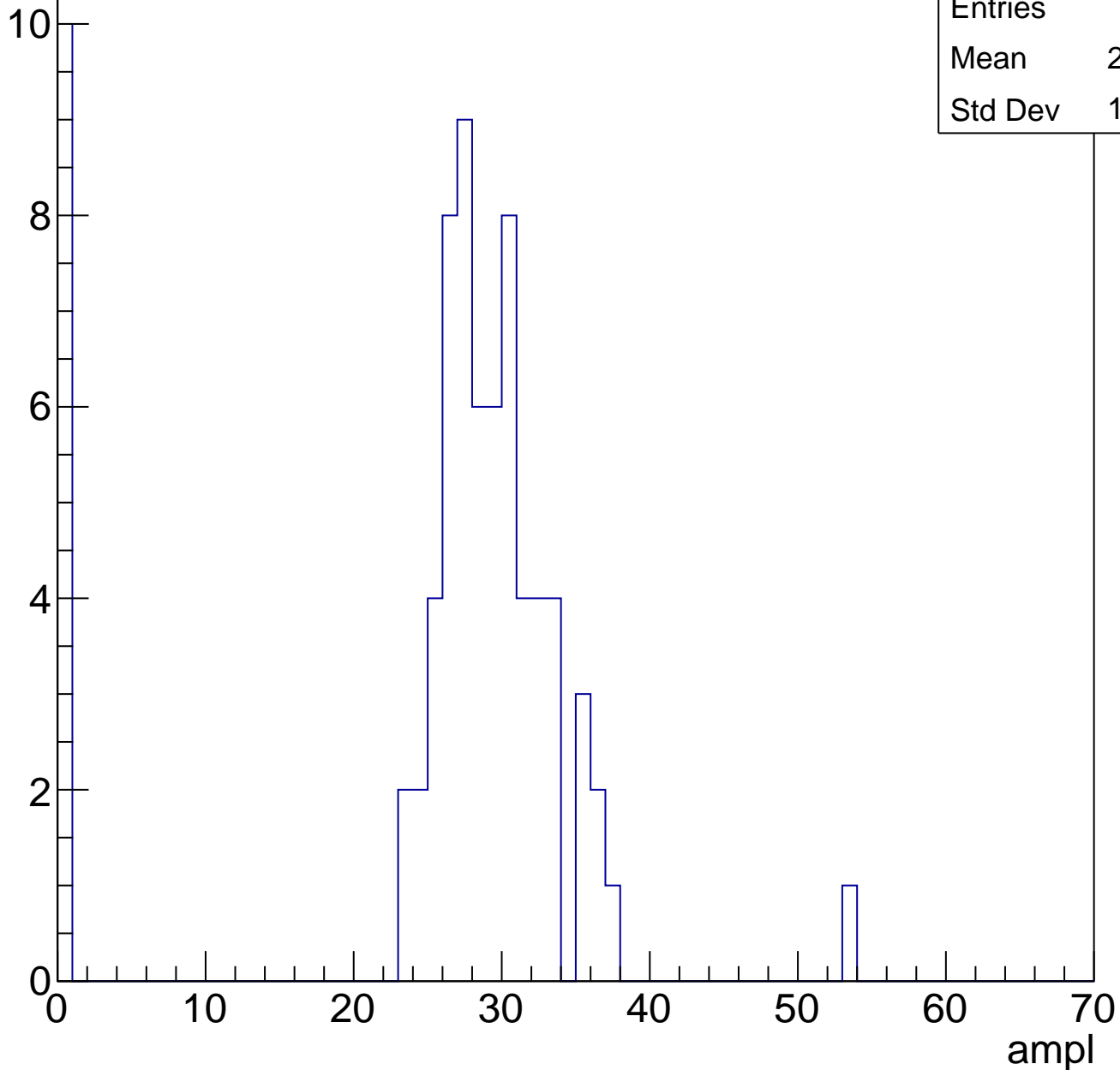


B1L103S, U9-ch40, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	74
Mean	25.38
Std Dev	10.85

Entry

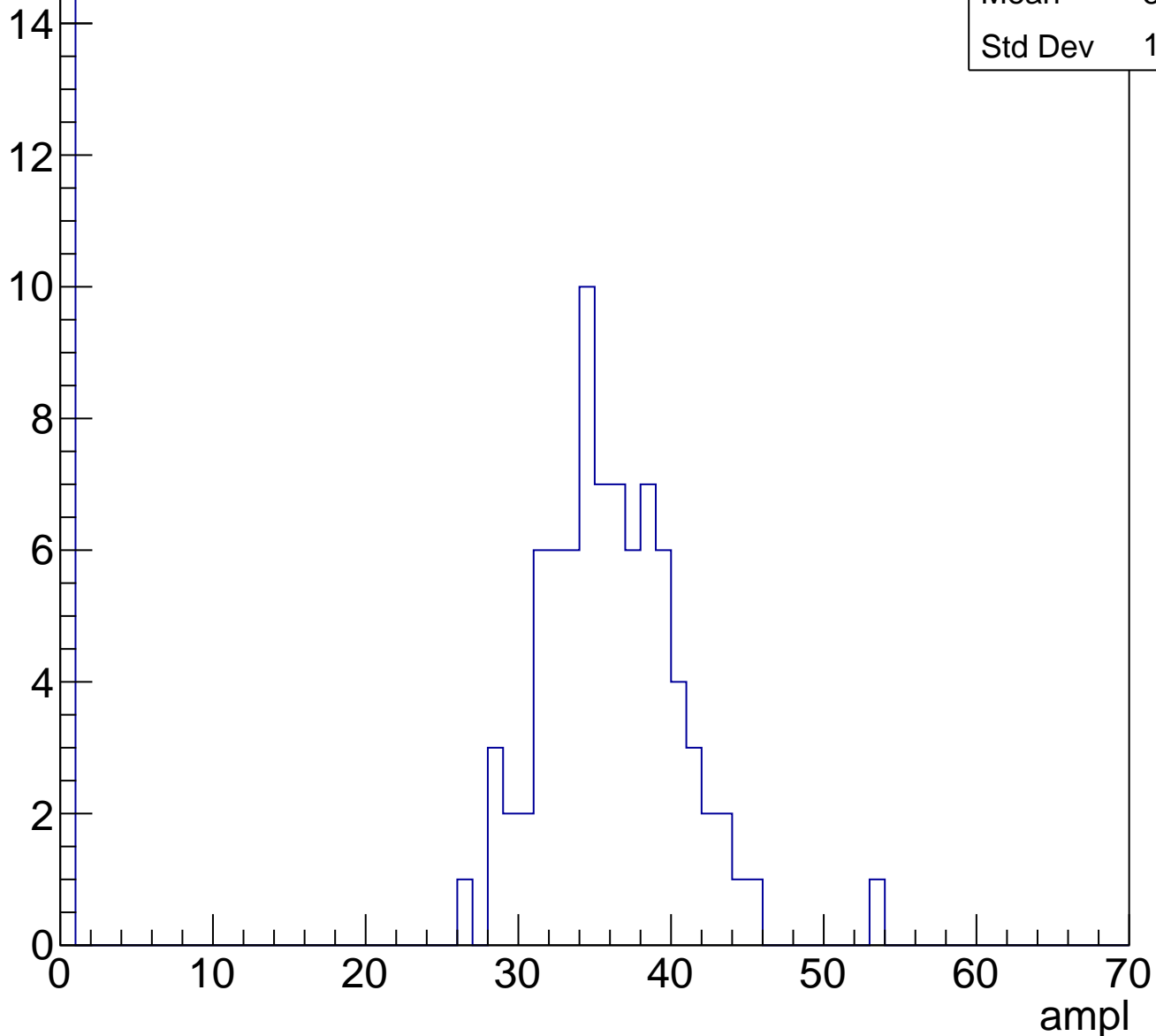


B1L103S, U9-ch40, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	98
Mean	30.18
Std Dev	13.46

Entry

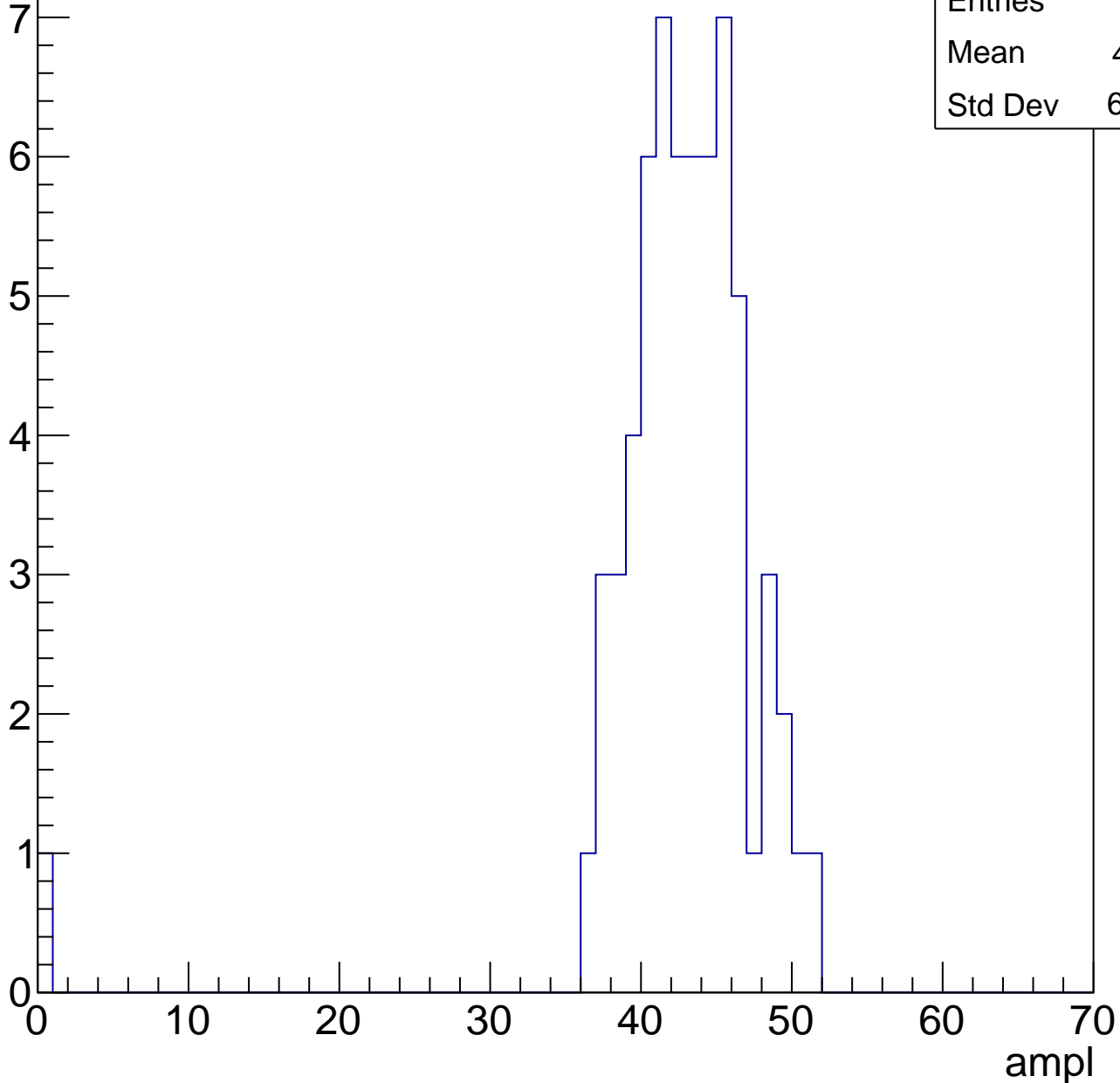


B1L103S, U9-ch40, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

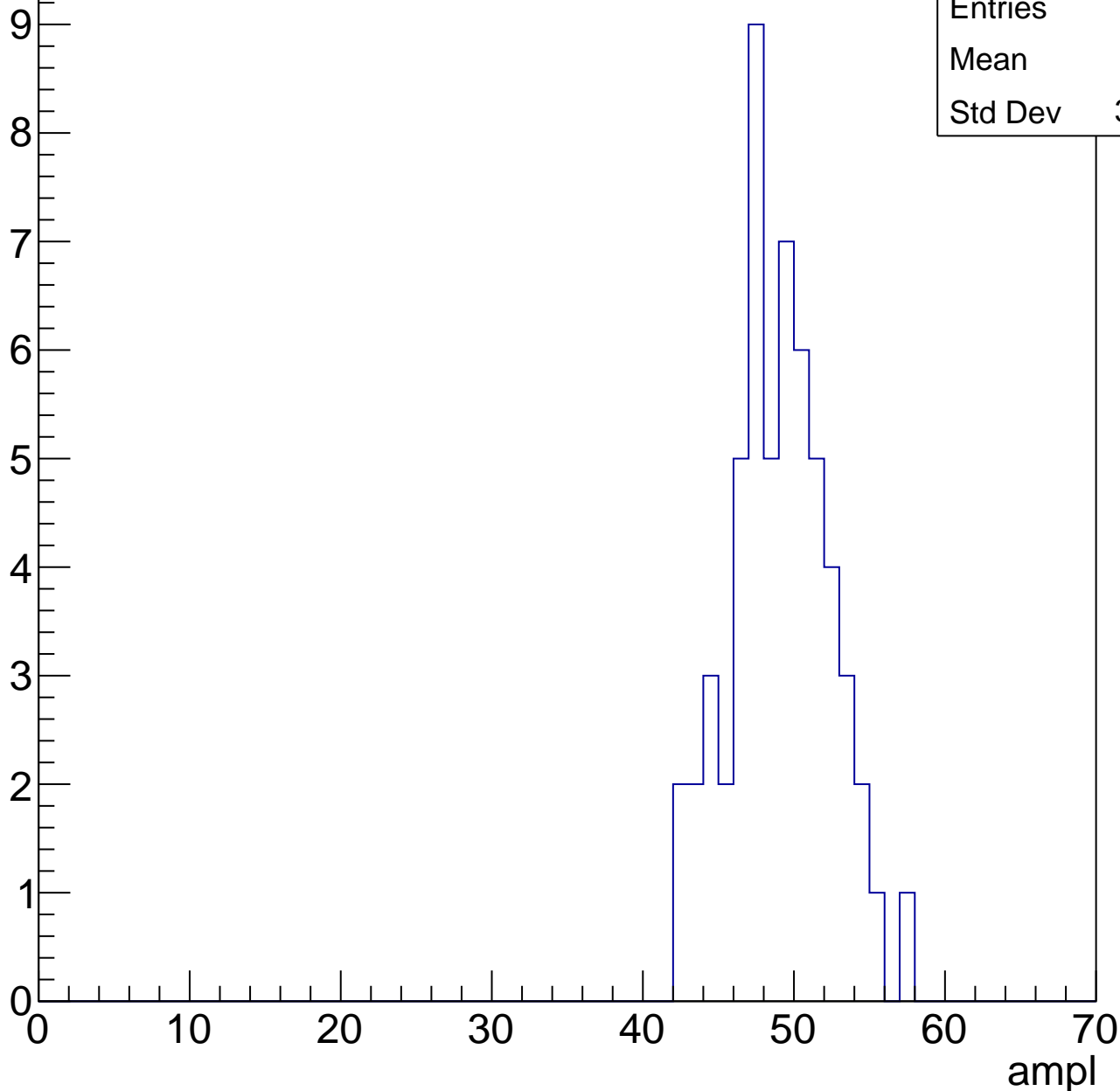
Entries	63
Mean	42.11
Std Dev	6.347



B1L103S, U9-ch40, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry



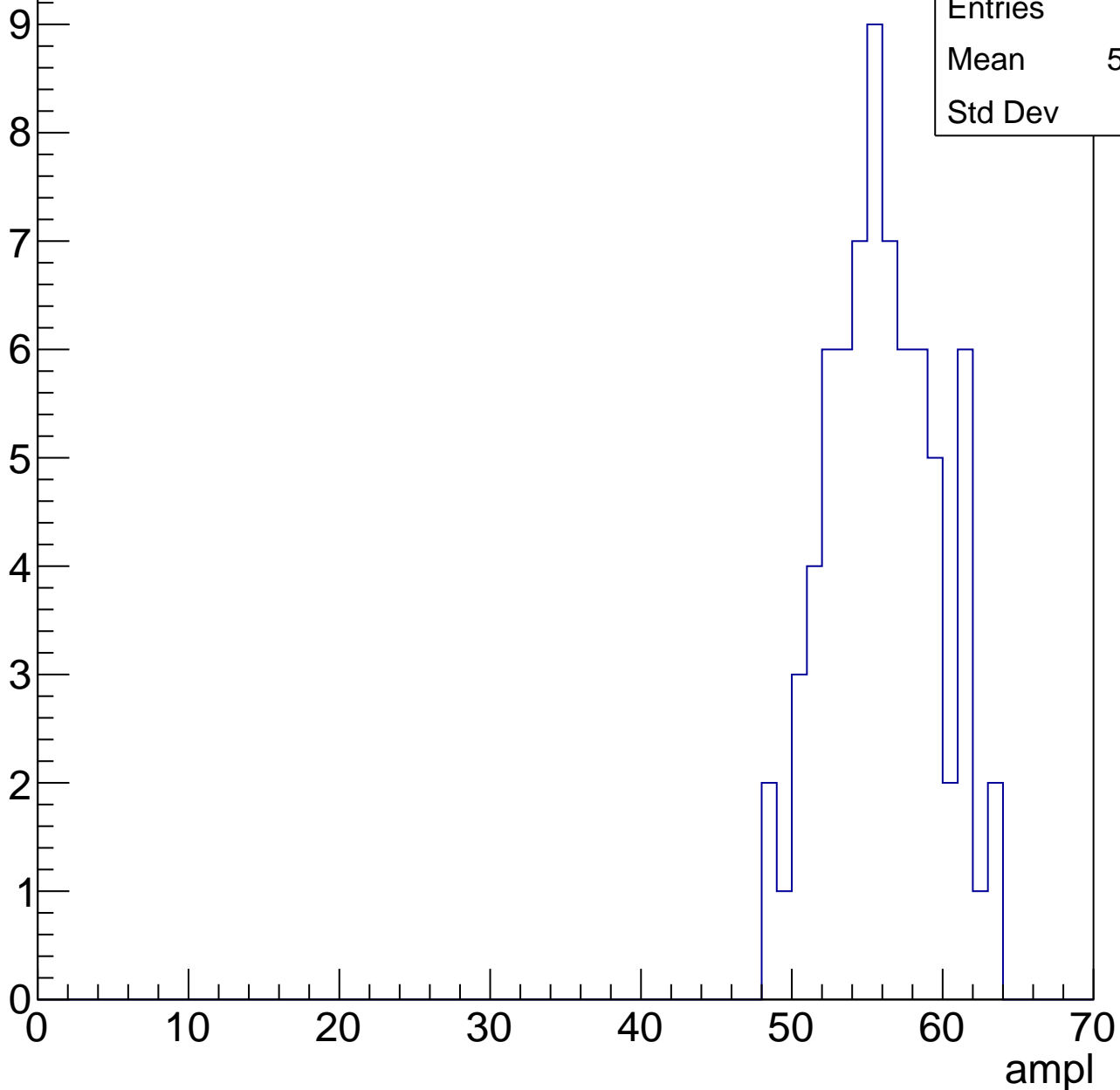
Entries	57
Mean	48.6
Std Dev	3.281

B1L103S, U9-ch40, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	55.52
Std Dev	3.6

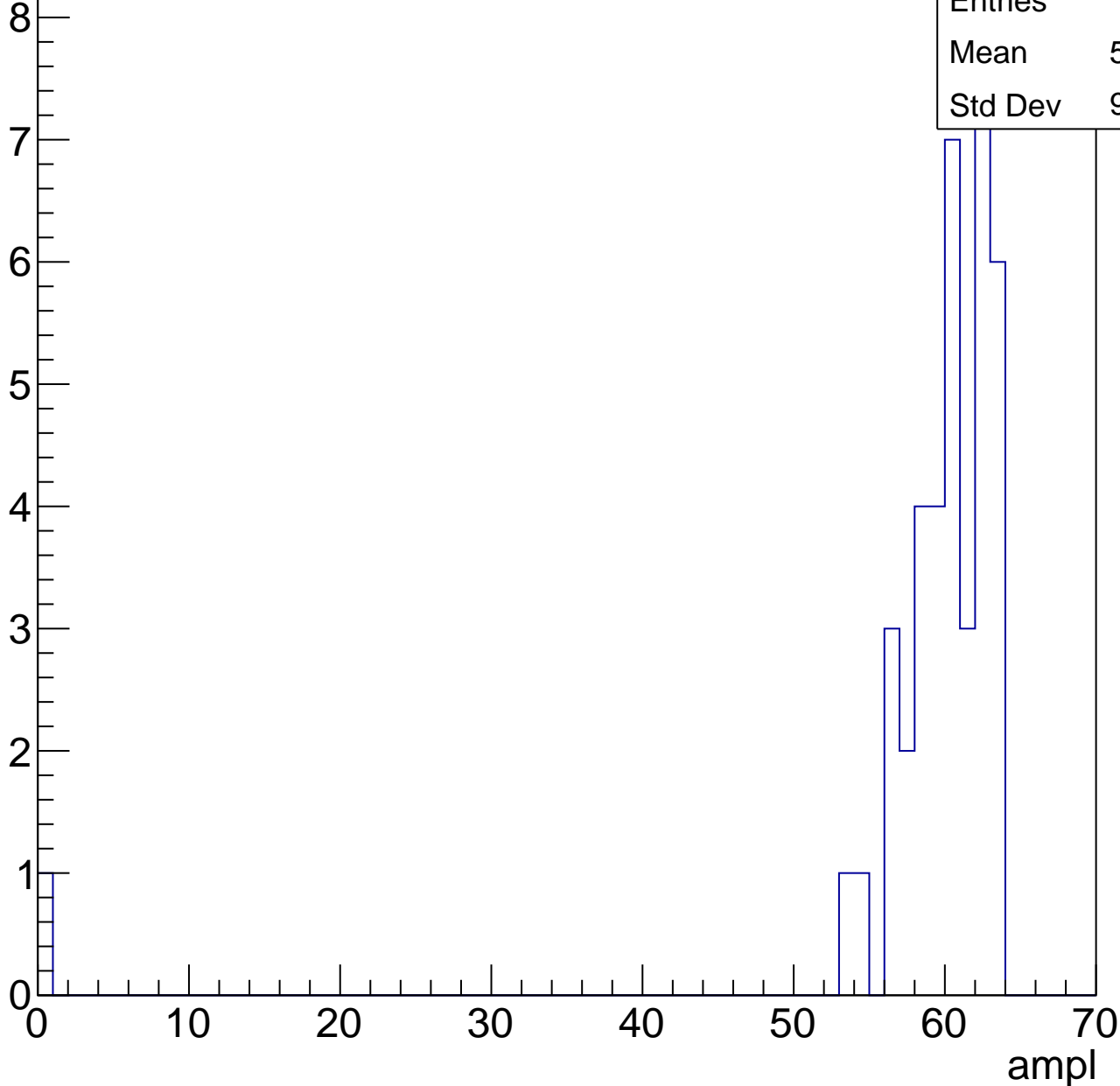


B1L103S, U9-ch40, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	58.35
Std Dev	9.684



B1L103S, U9-ch40, adc6

calib_packv5_041523_1651.root, FC#0, port C2

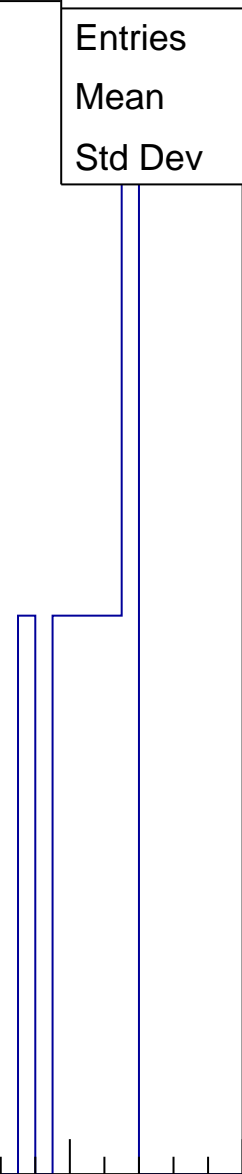
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	7
Mean	60.71
Std Dev	2.05

0 10 20 30 40 50 60 70

ampl



B1L103S, U9-ch40, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



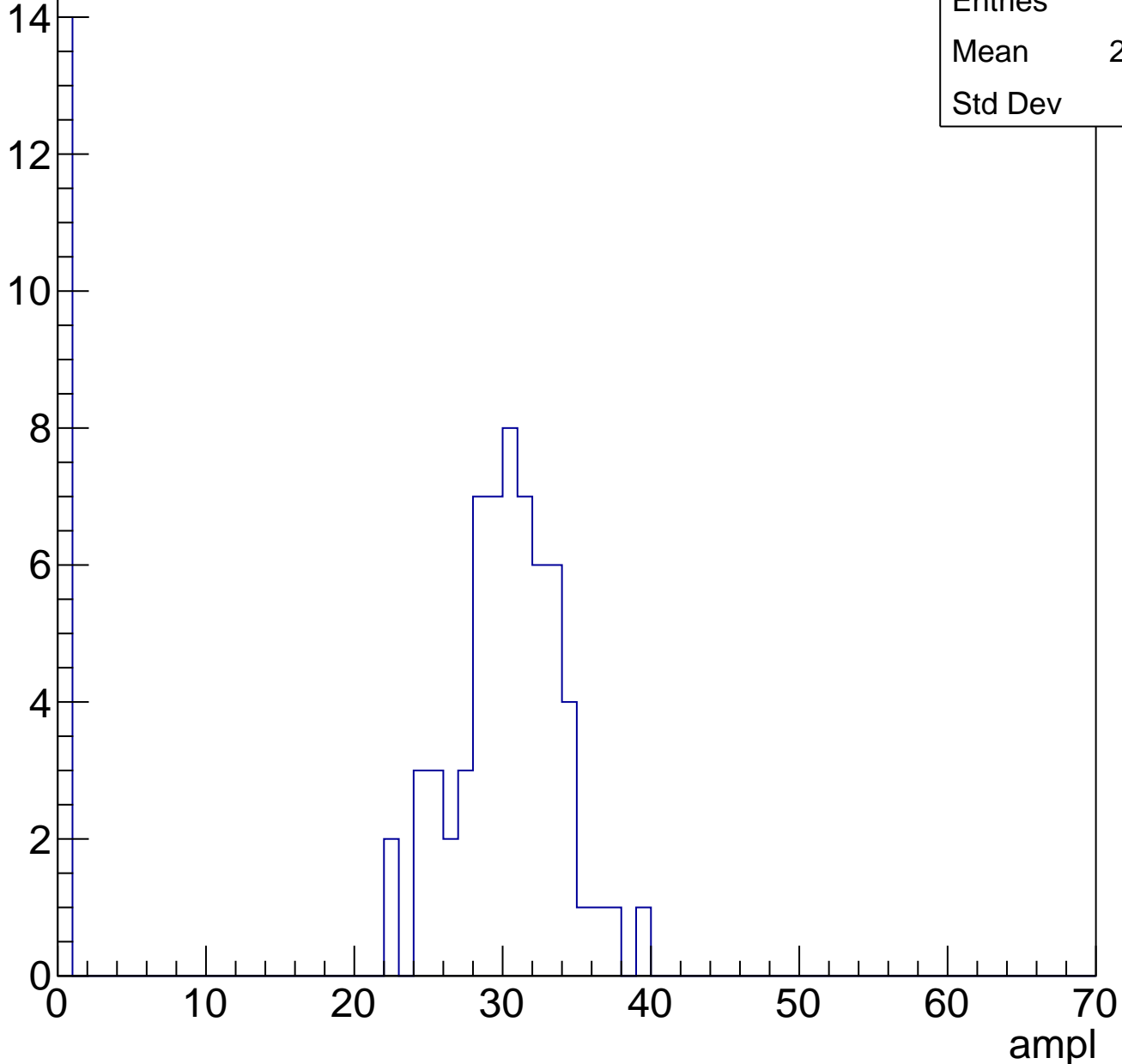
Entries	19
Mean	0
Std Dev	0

B1L103S, U9-ch41, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	76
Mean	24.38
Std Dev	12

Entry



B1L103S, U9-ch41, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	30.07
Std Dev	14.05

Entry

12

10

8

6

4

2

0

0

10

20

30

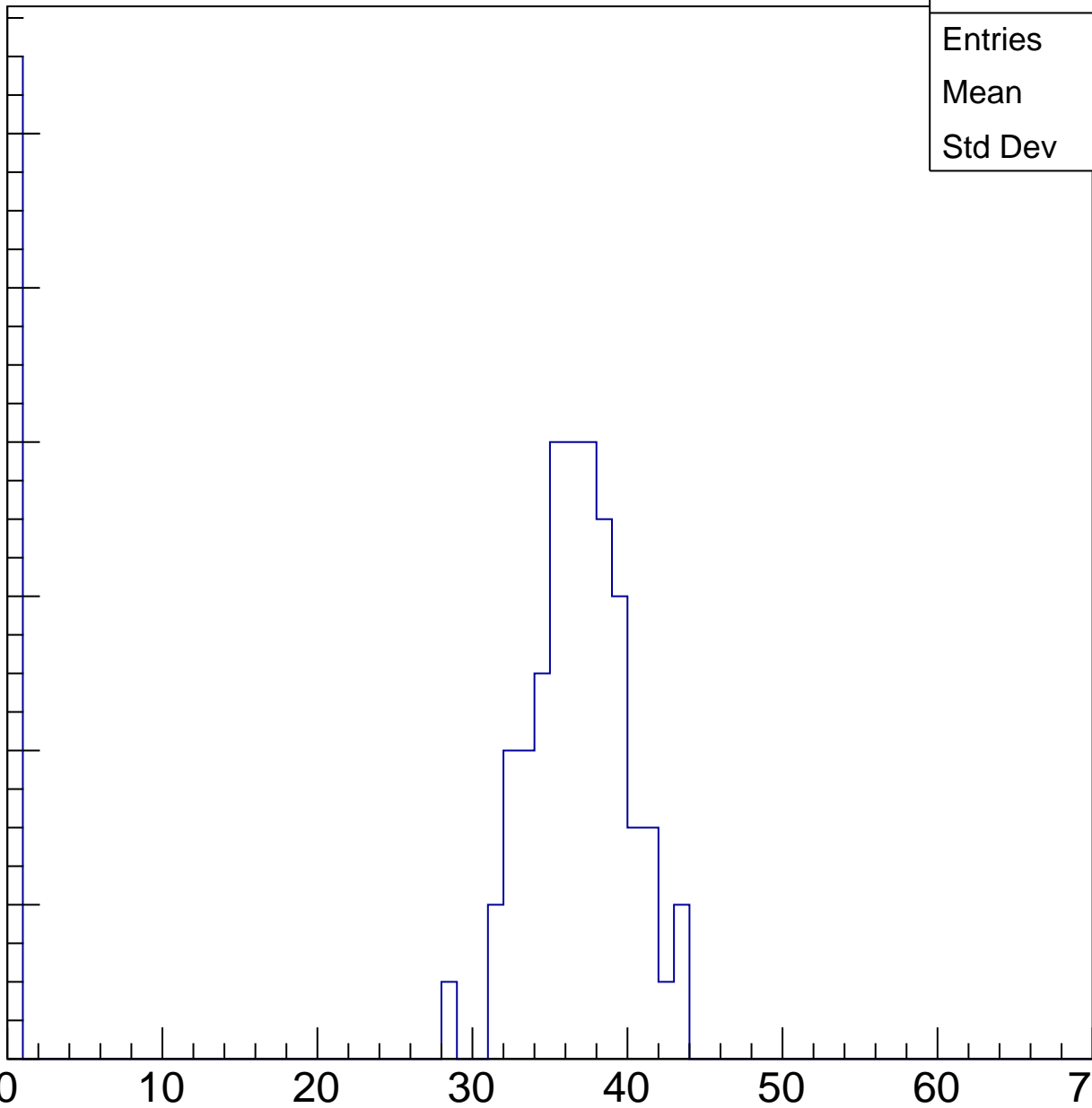
40

50

60

70

ampl

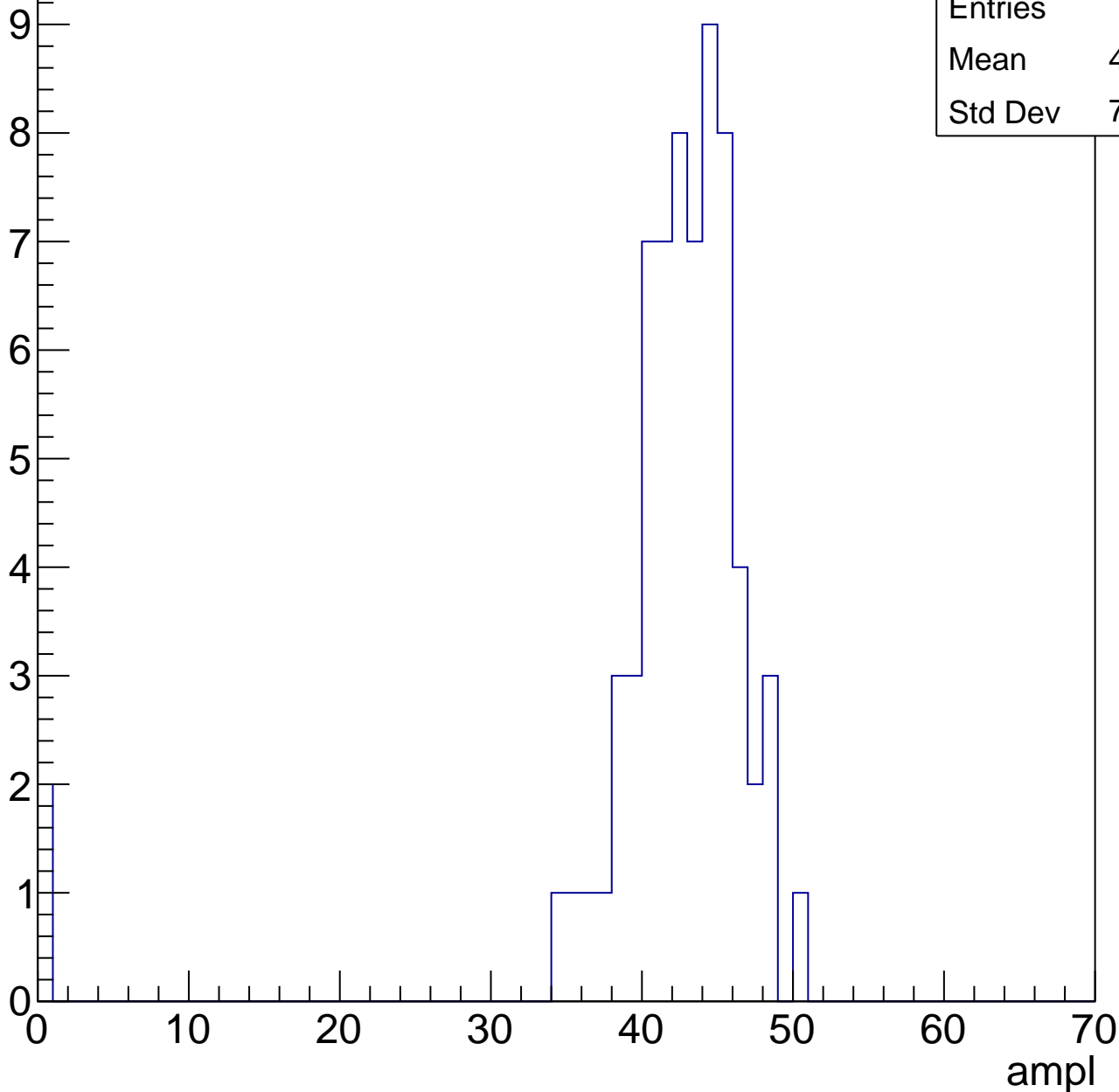


B1L103S, U9-ch41, adc2

calib_packv5_041523_1651.root, FC#0, port C2

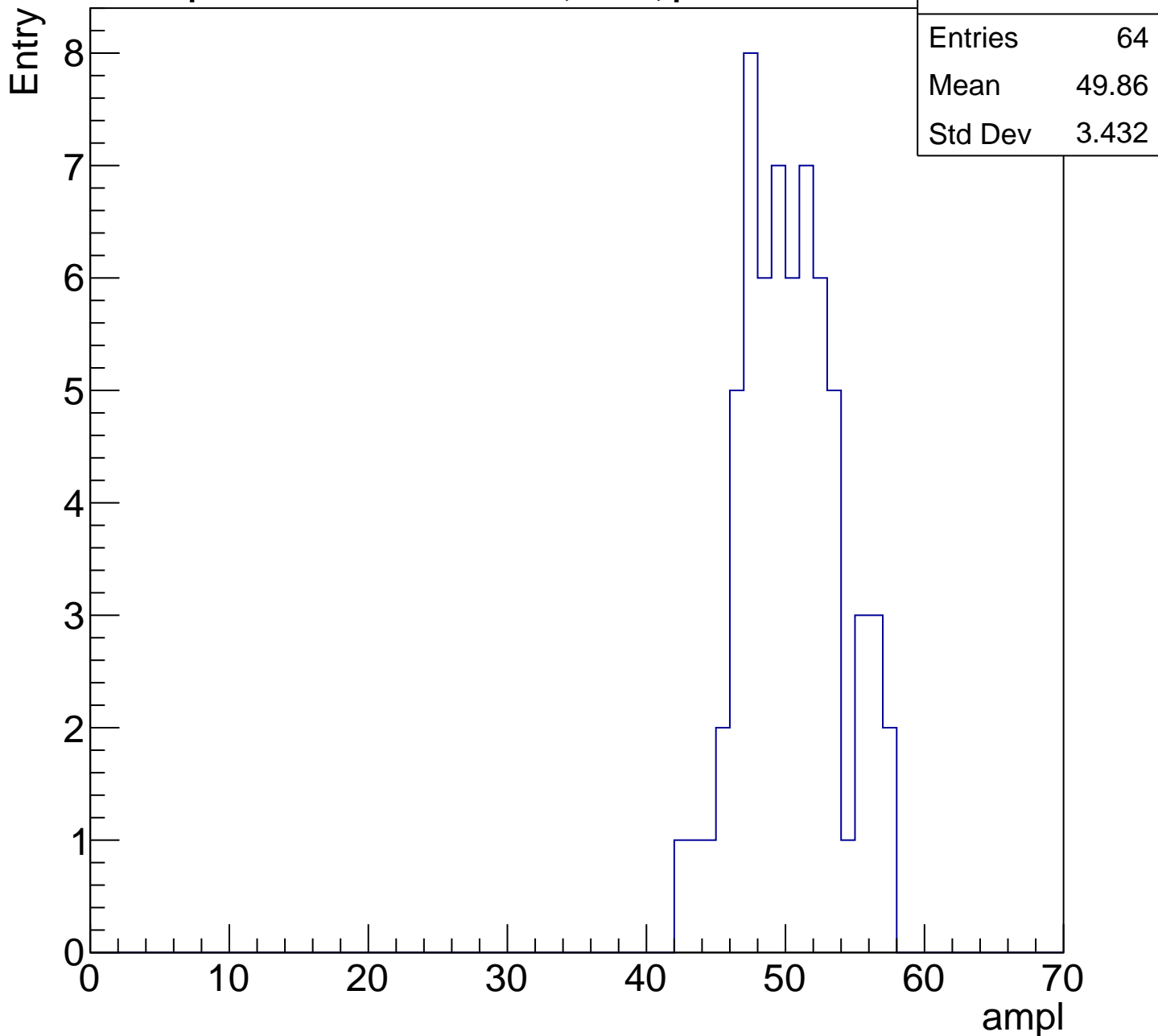
Entry

Entries	68
Mean	41.25
Std Dev	7.835



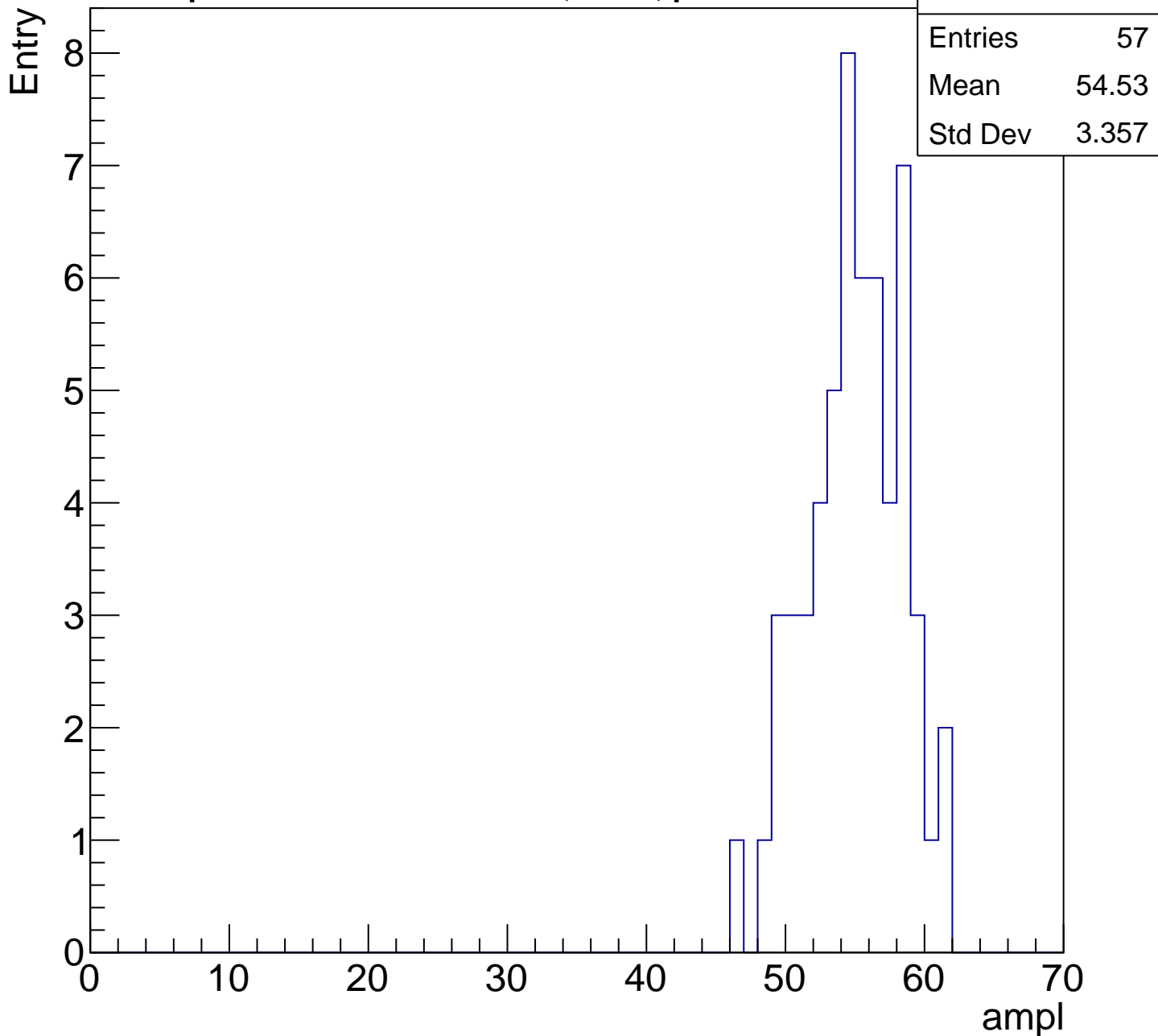
B1L103S, U9-ch41, adc3

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U9-ch41, adc4

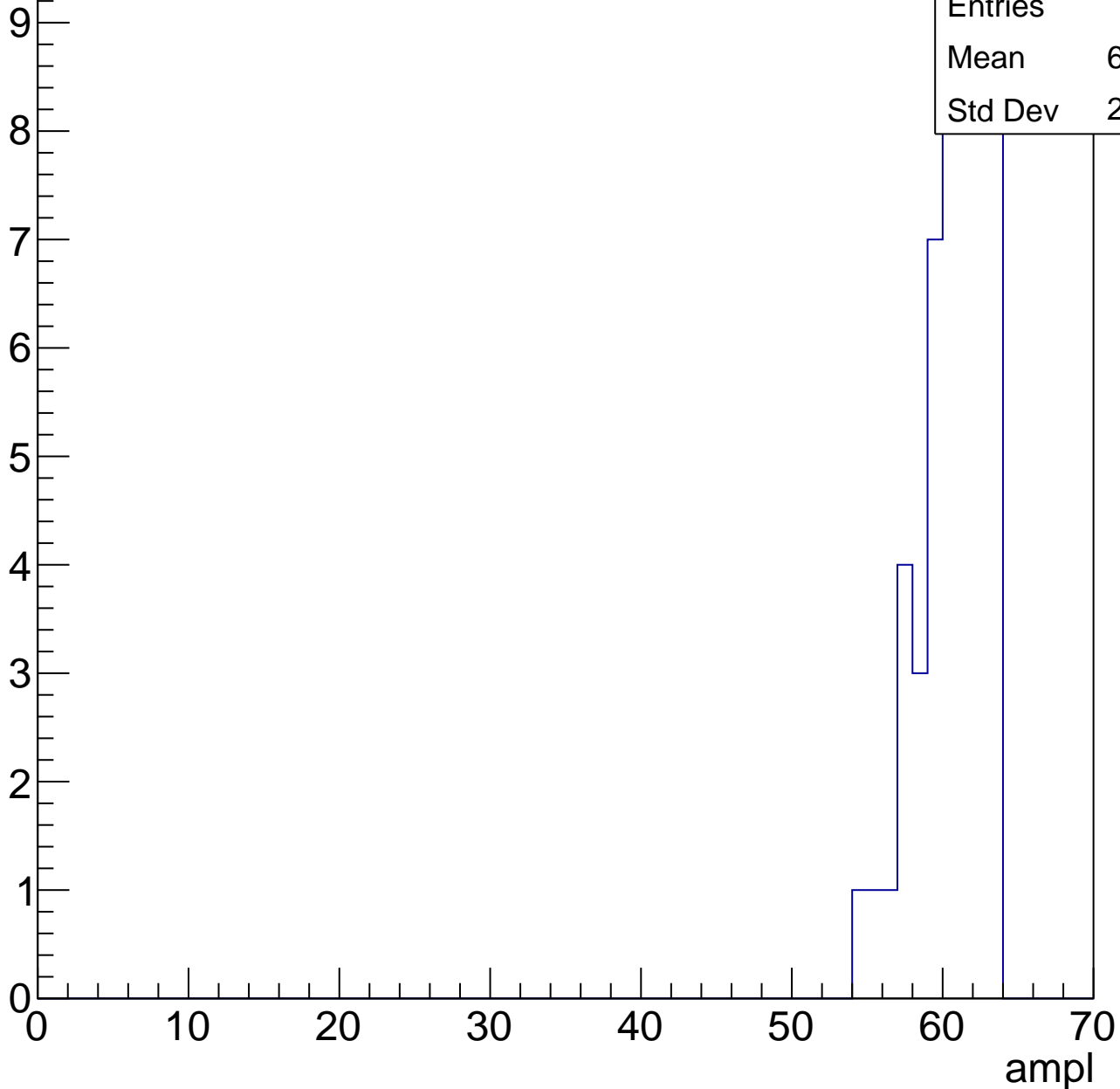
calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U9-ch41, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch41, adc6

calib_packv5_041523_1651.root, FC#0, port C2

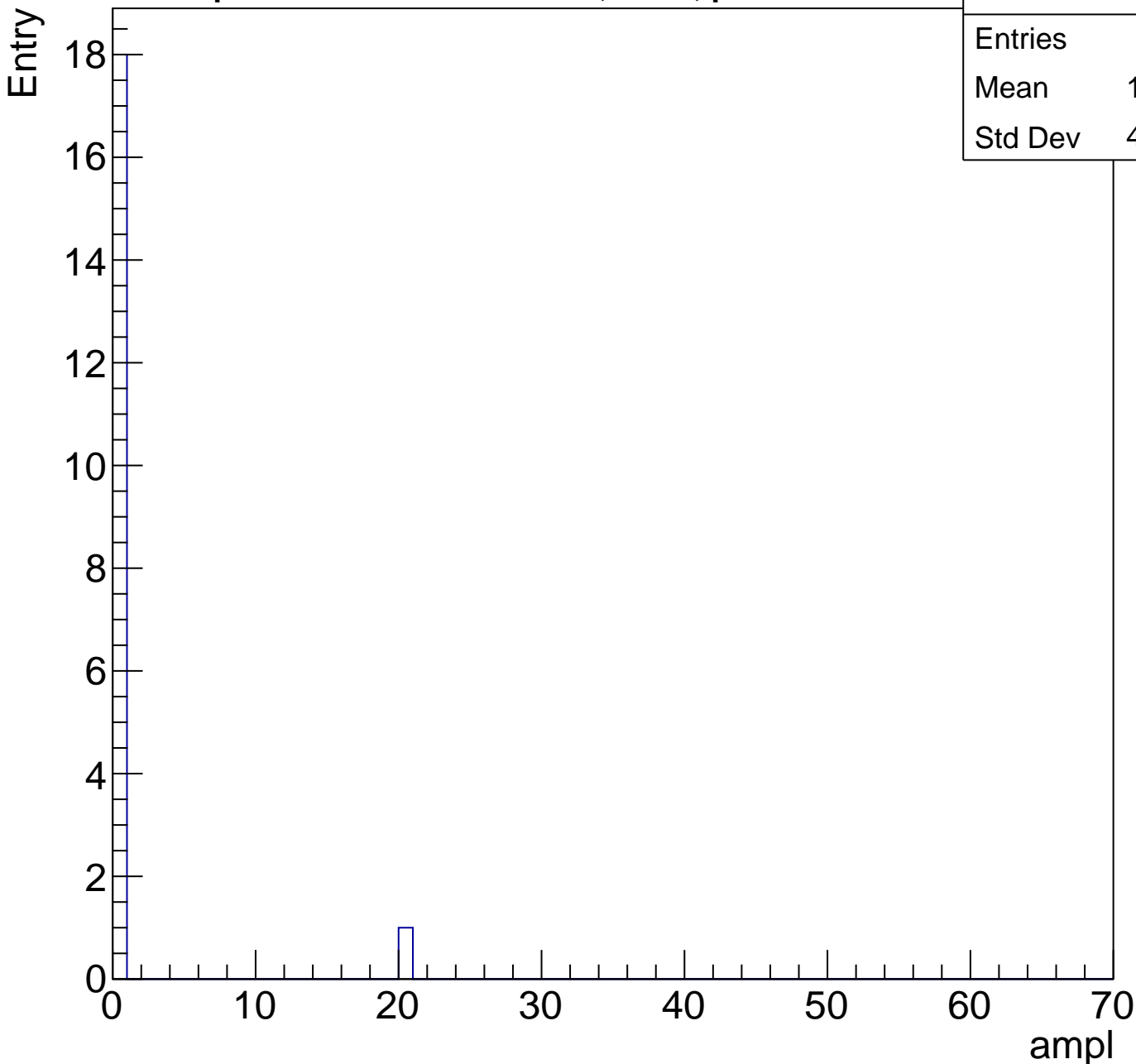
Entry



B1L103S, U9-ch41, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.053
Std Dev	4.466

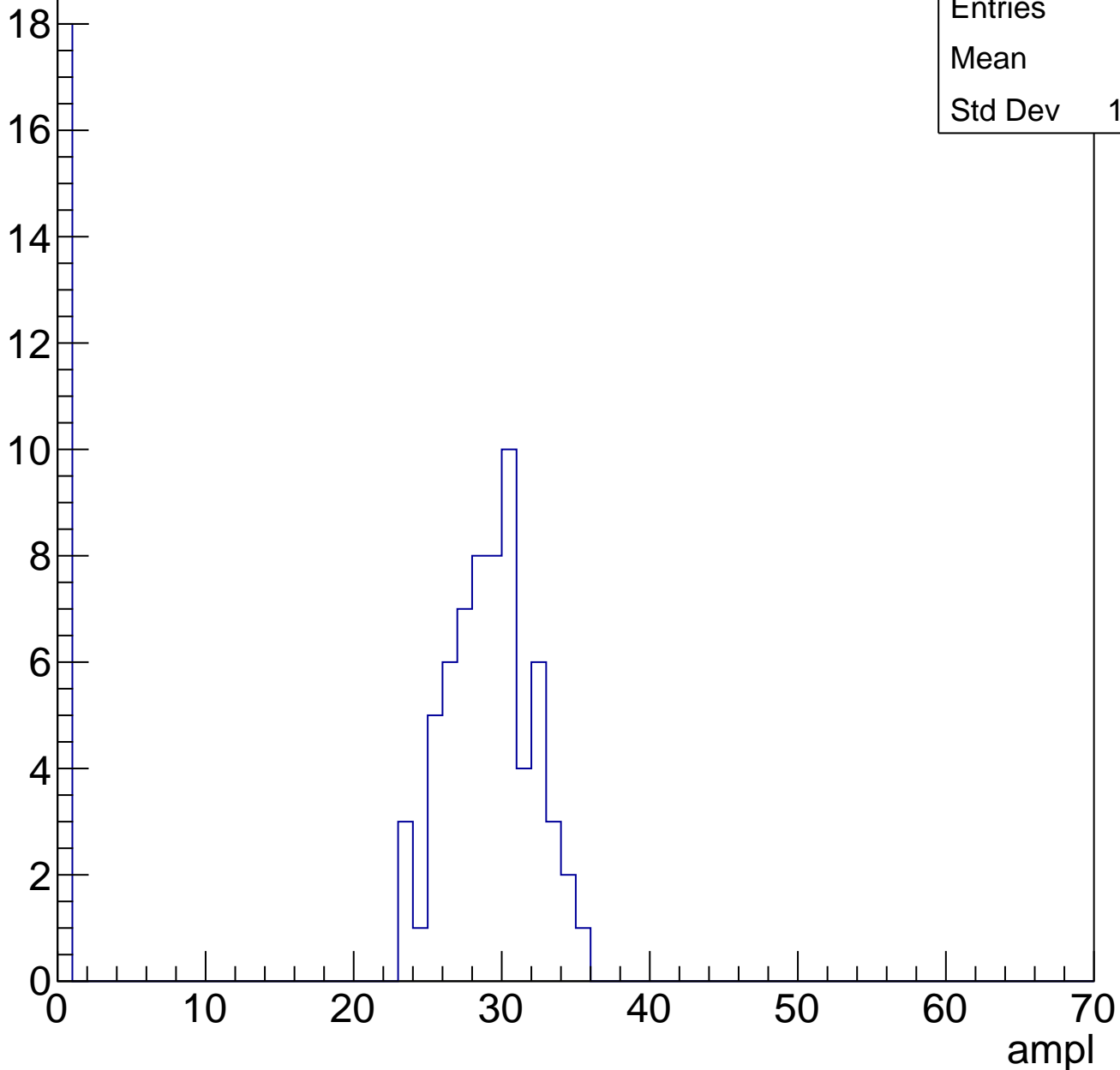


B1L103S, U9-ch42, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	22.4
Std Dev	12.14

Entry



B1L103S, U9-ch42, adc1

calib_packv5_041523_1651.root, FC#0, port C2

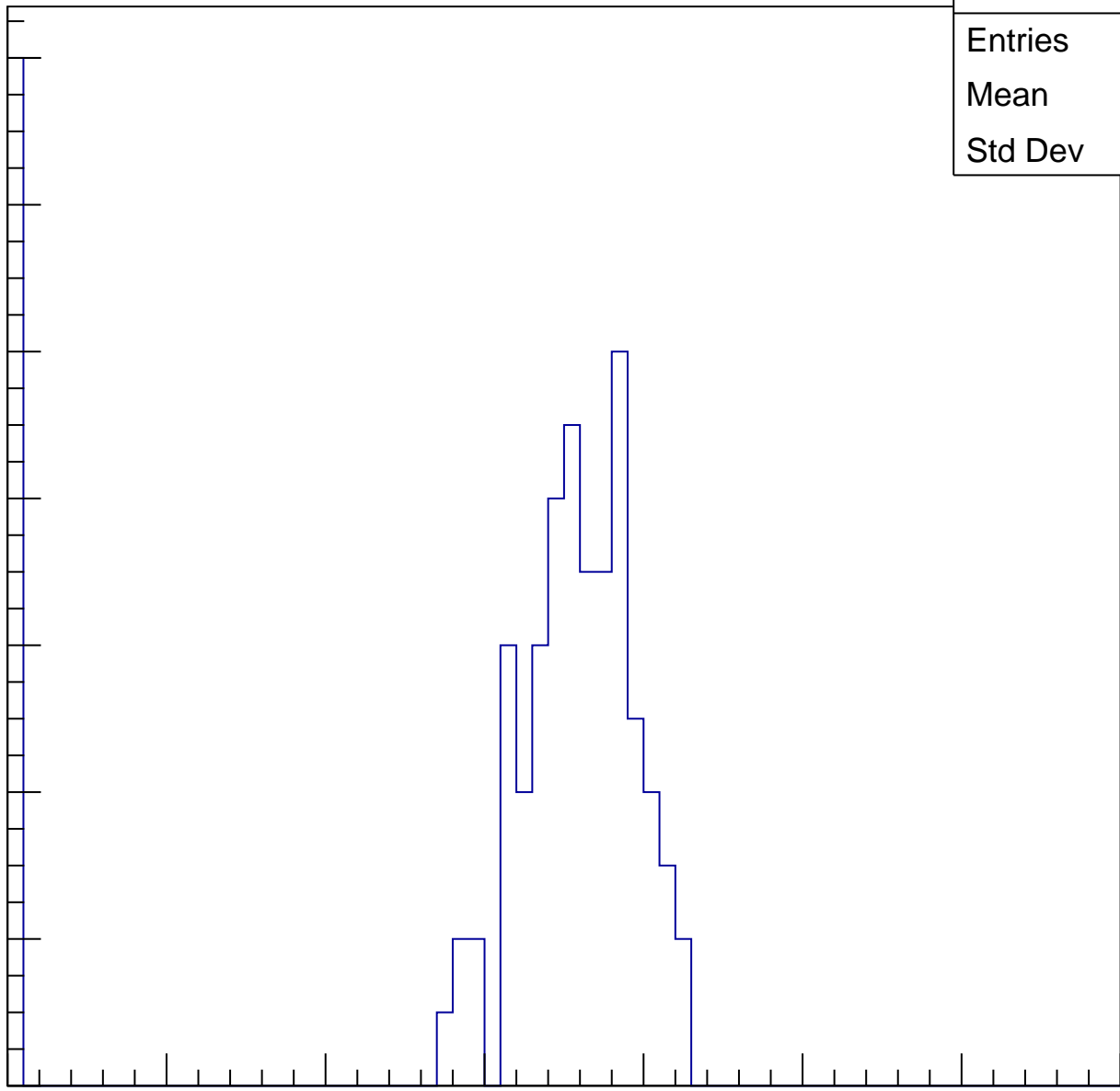
Entries	90
Mean	29.92
Std Dev	13.22

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

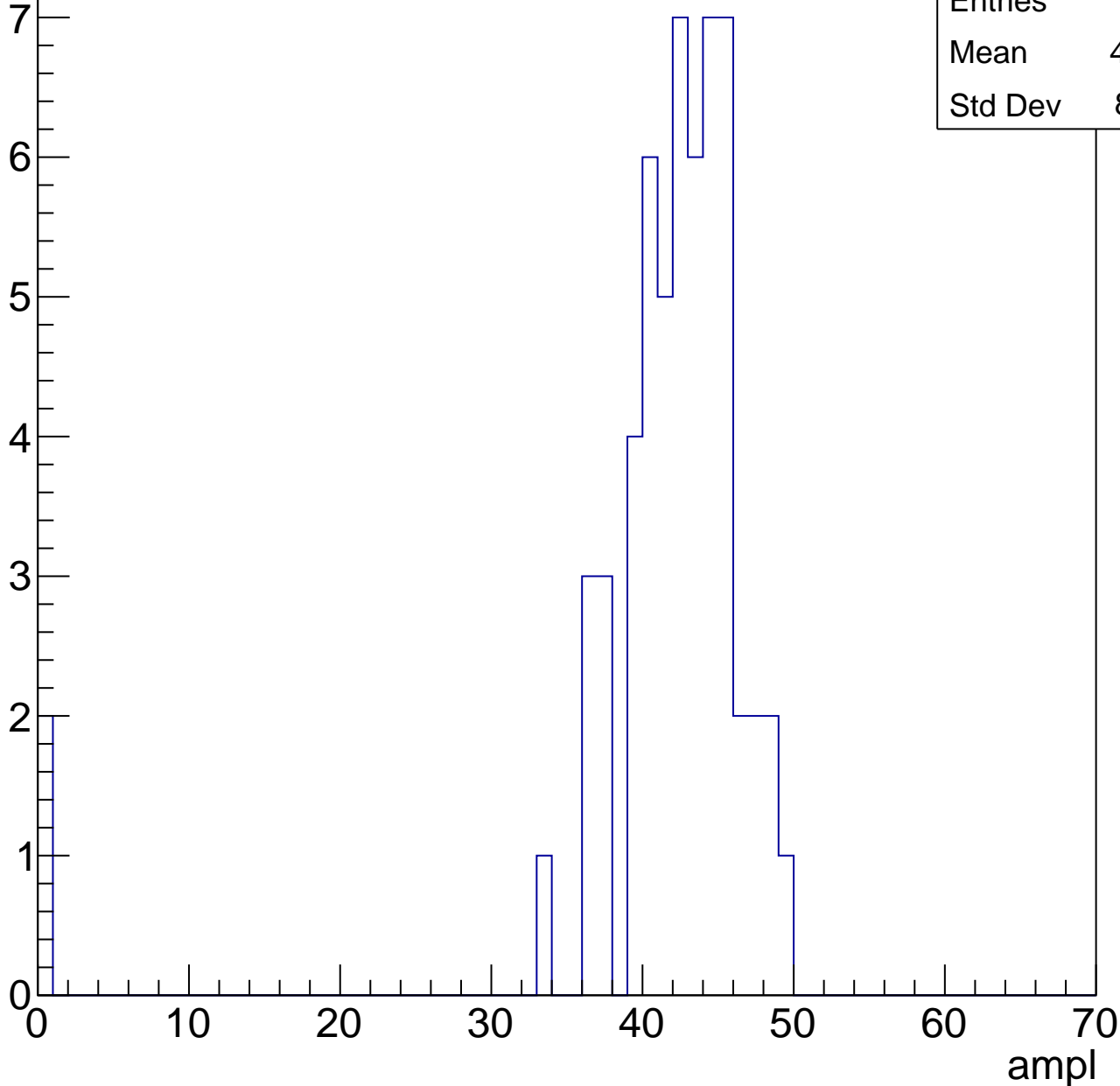


B1L103S, U9-ch42, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	40.67
Std Dev	8.361

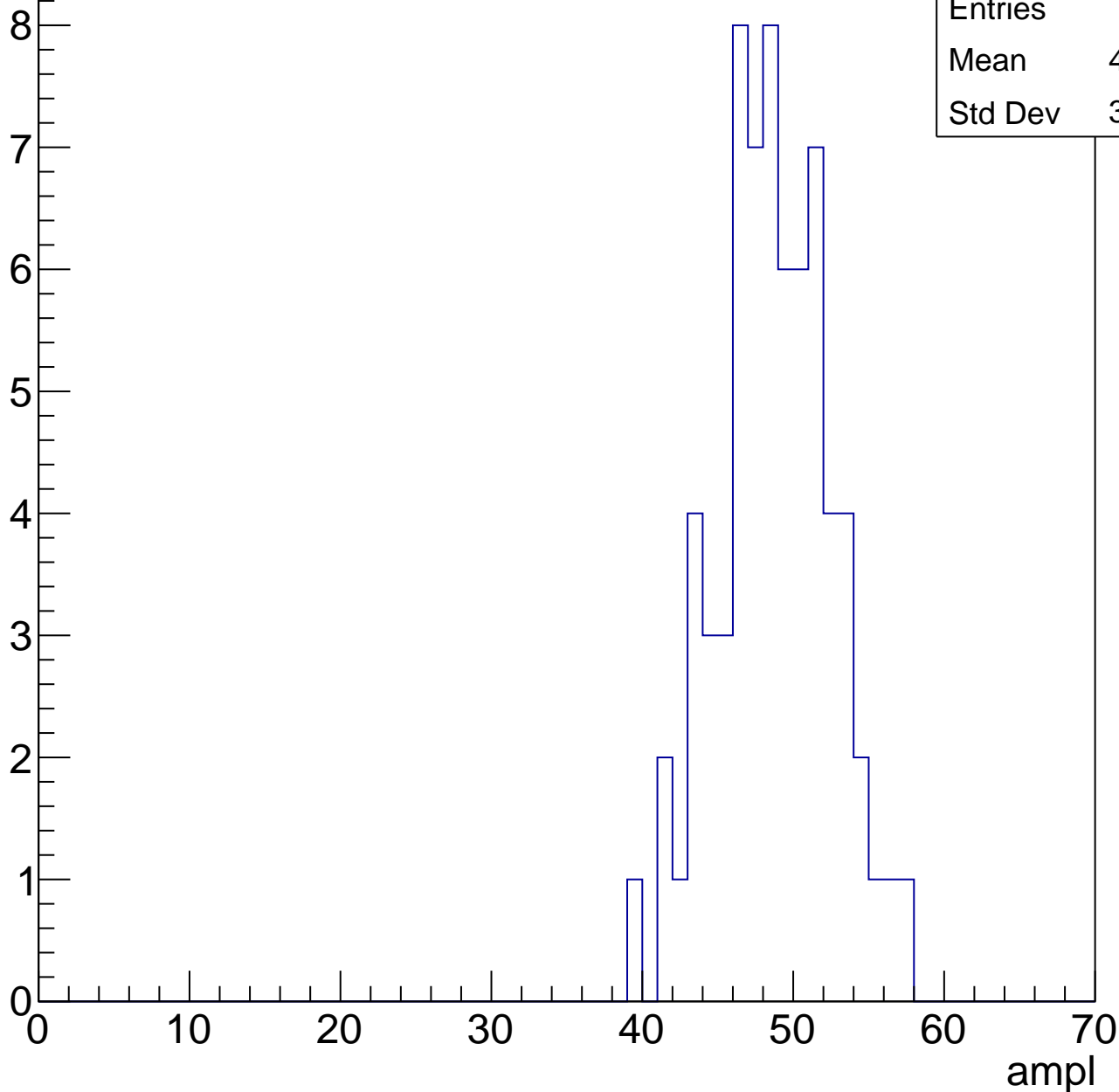


B1L103S, U9-ch42, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

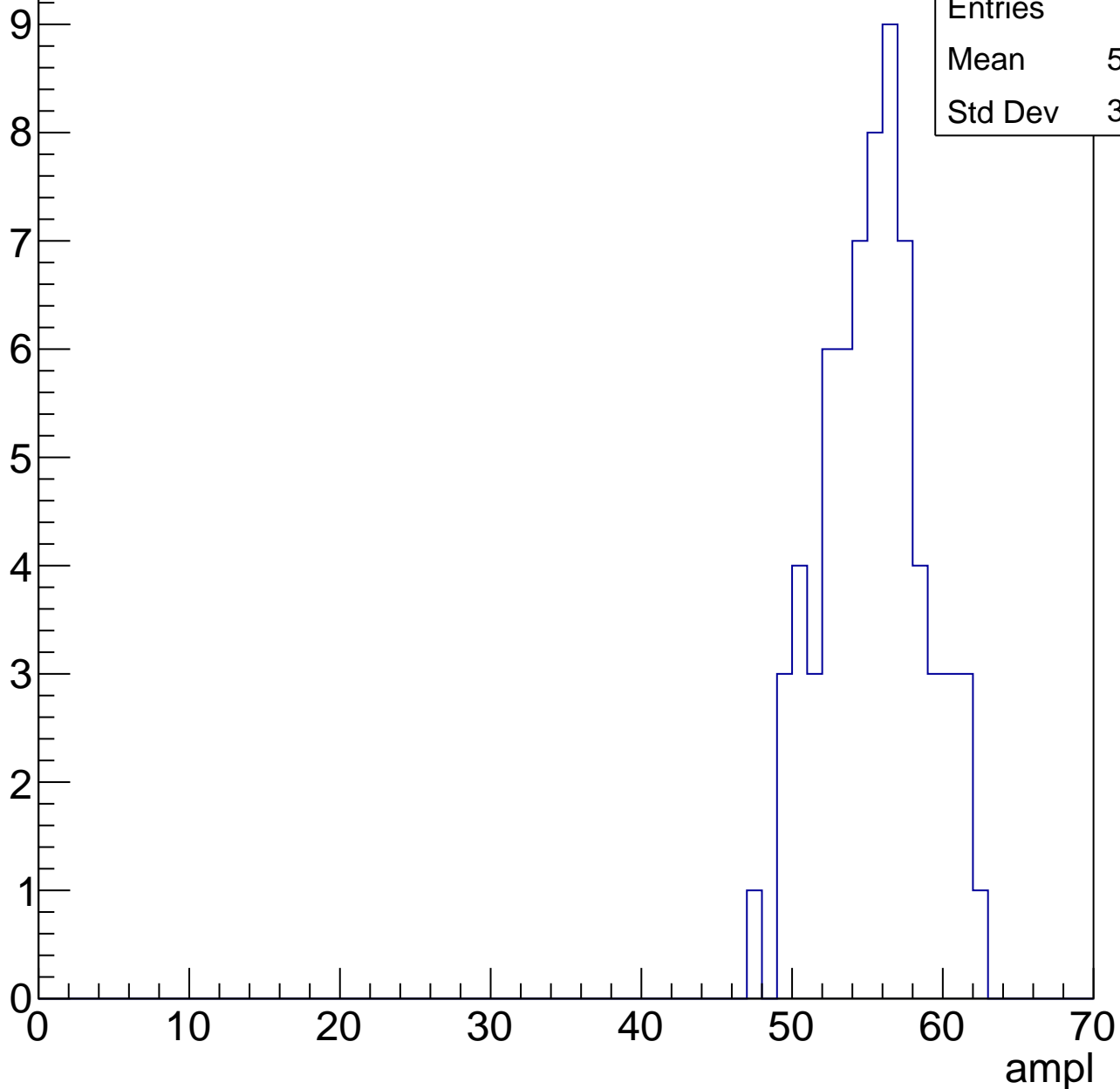
Entries	69
Mean	48.26
Std Dev	3.705



B1L103S, U9-ch42, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

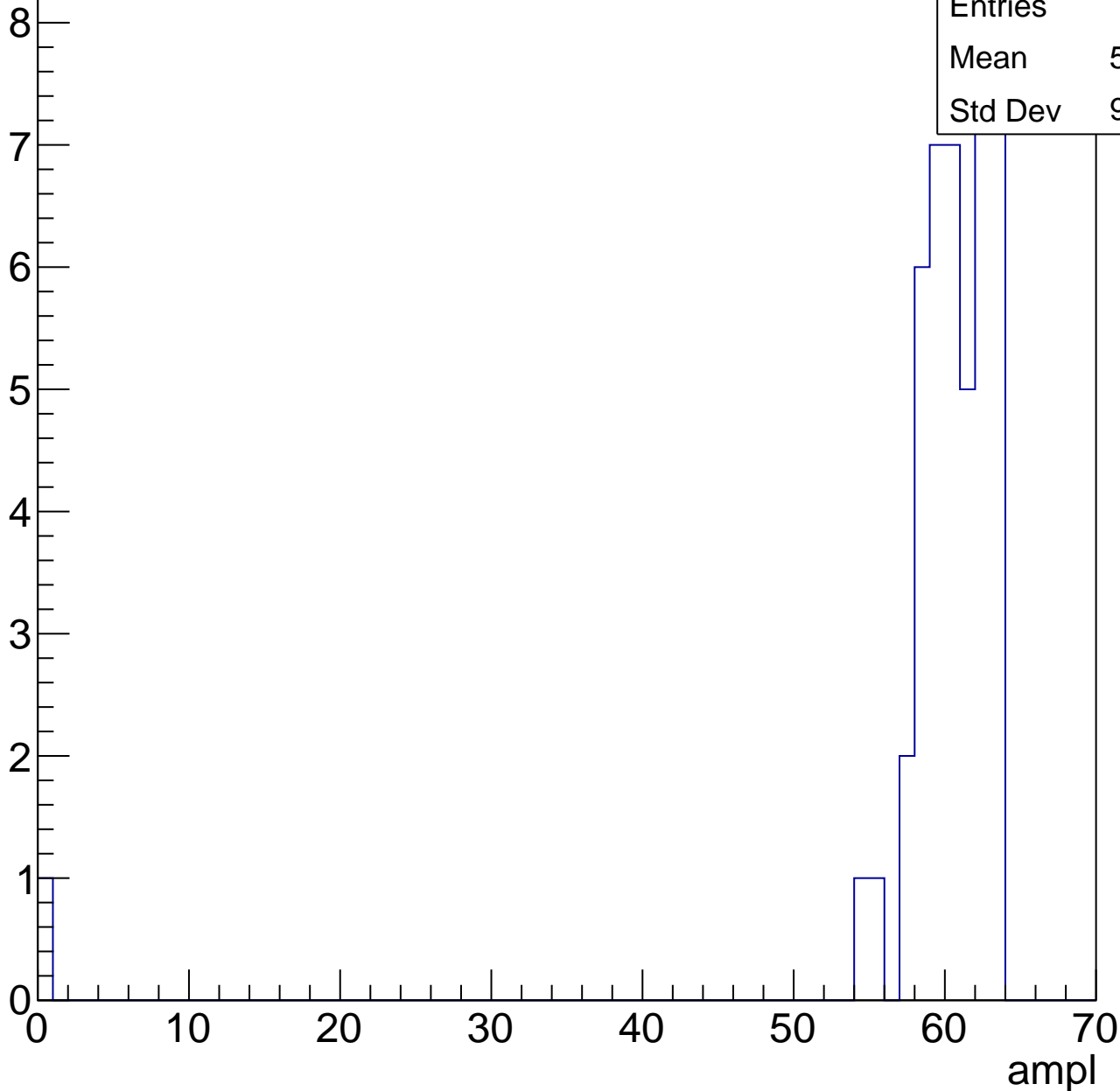


B1L103S, U9-ch42, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	46
Mean	58.89
Std Dev	9.044



B1L103S, U9-ch42, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	5
Mean	62
Std Dev	0.8944

ampl

B1L103S, U9-ch42, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.105
Std Dev	4.689

Entry

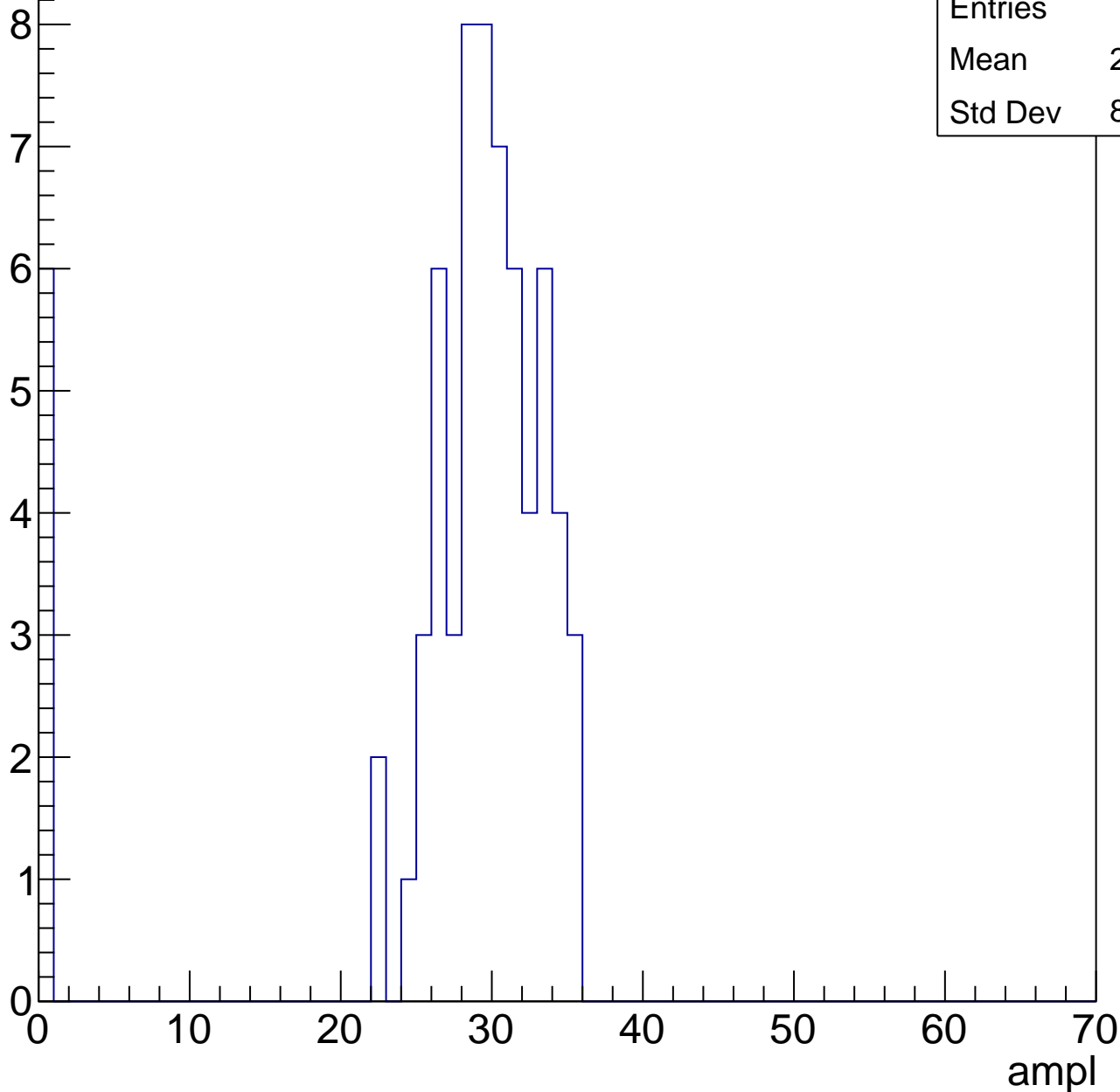


B1L103S, U9-ch43, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

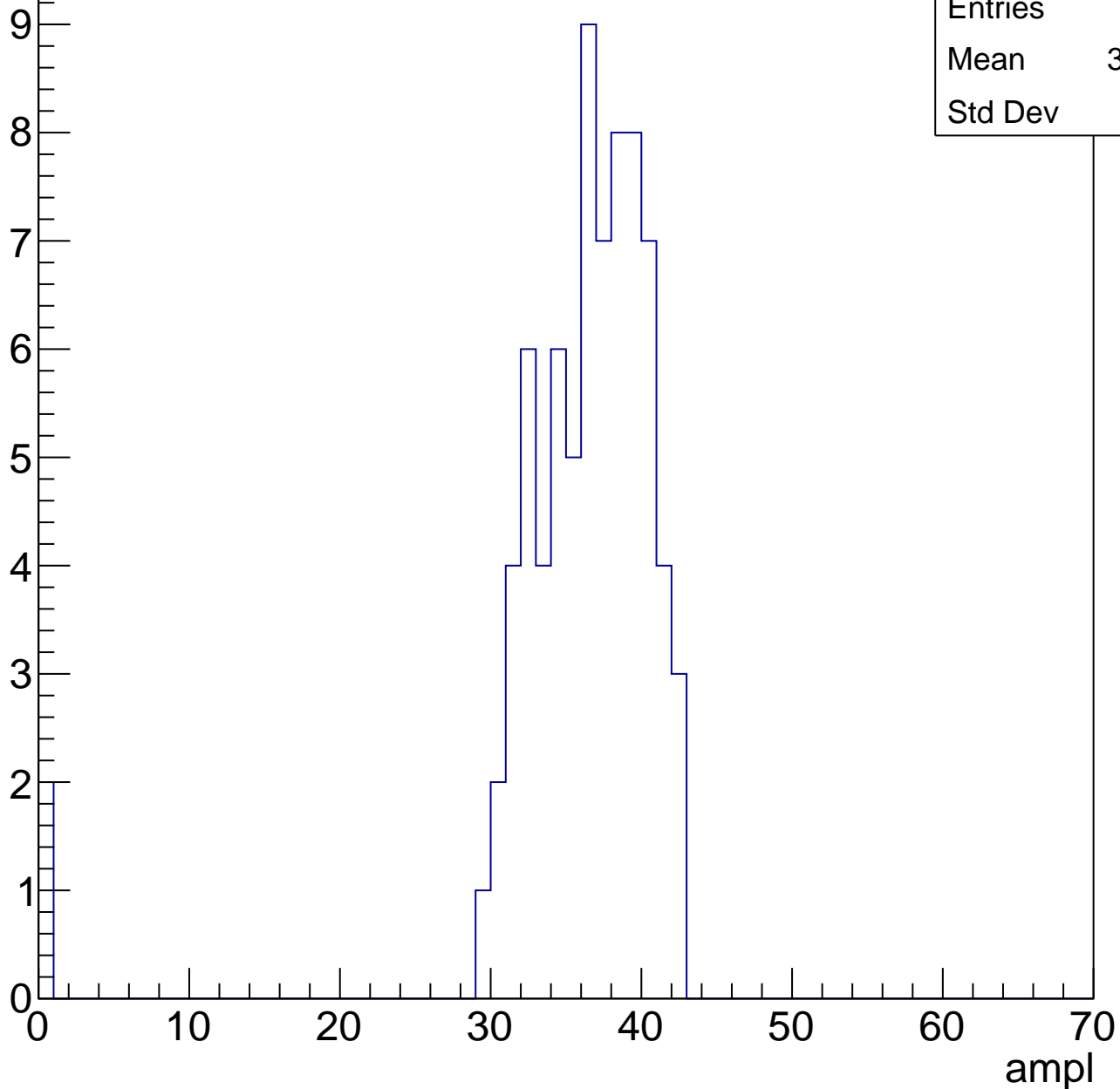
Entries	67
Mean	26.85
Std Dev	8.938



B1L103S, U9-ch43, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry



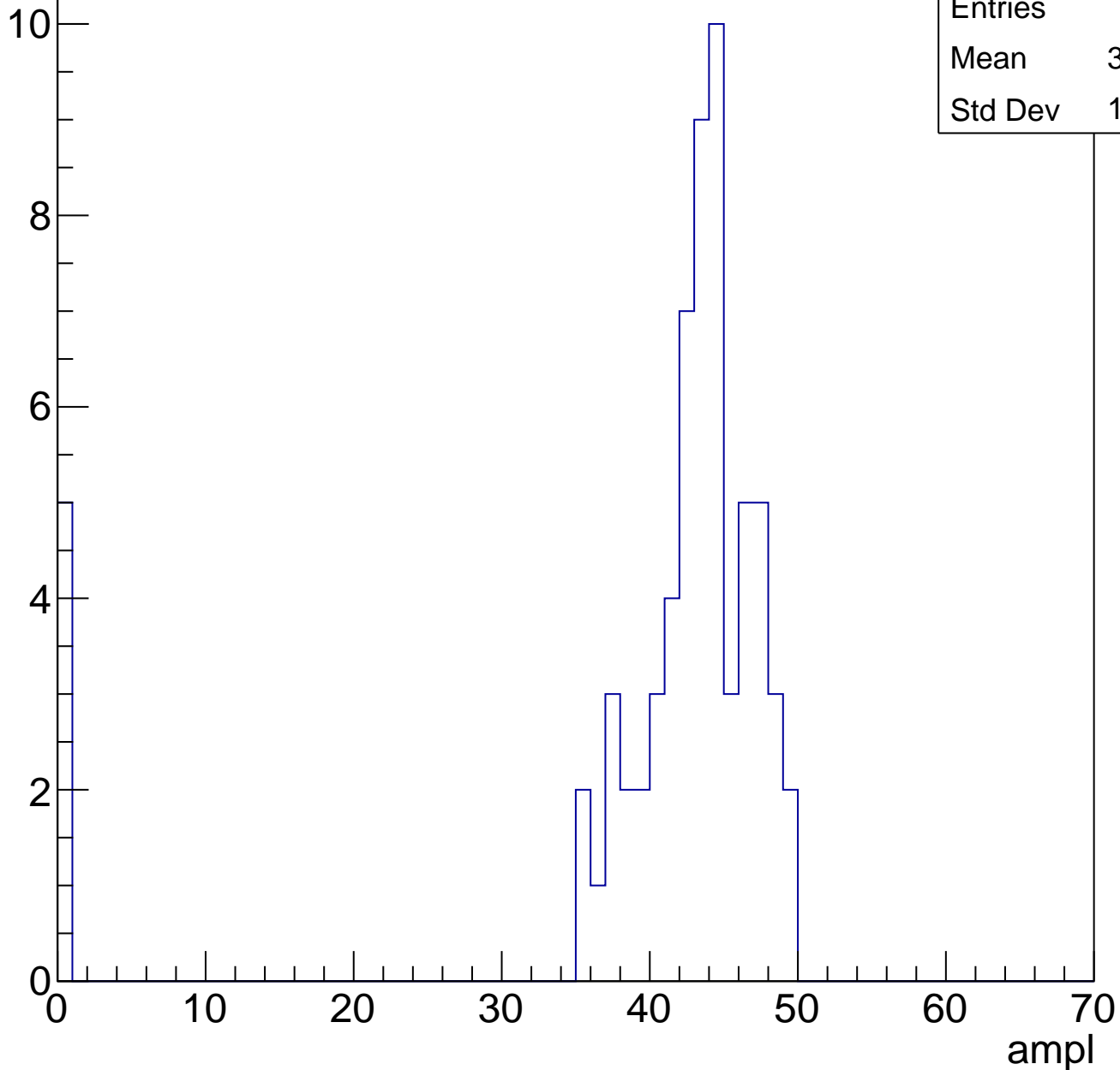
Entries	76
Mean	35.33
Std Dev	6.66

B1L103S, U9-ch43, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	66
Mean	39.67
Std Dev	11.82

Entry

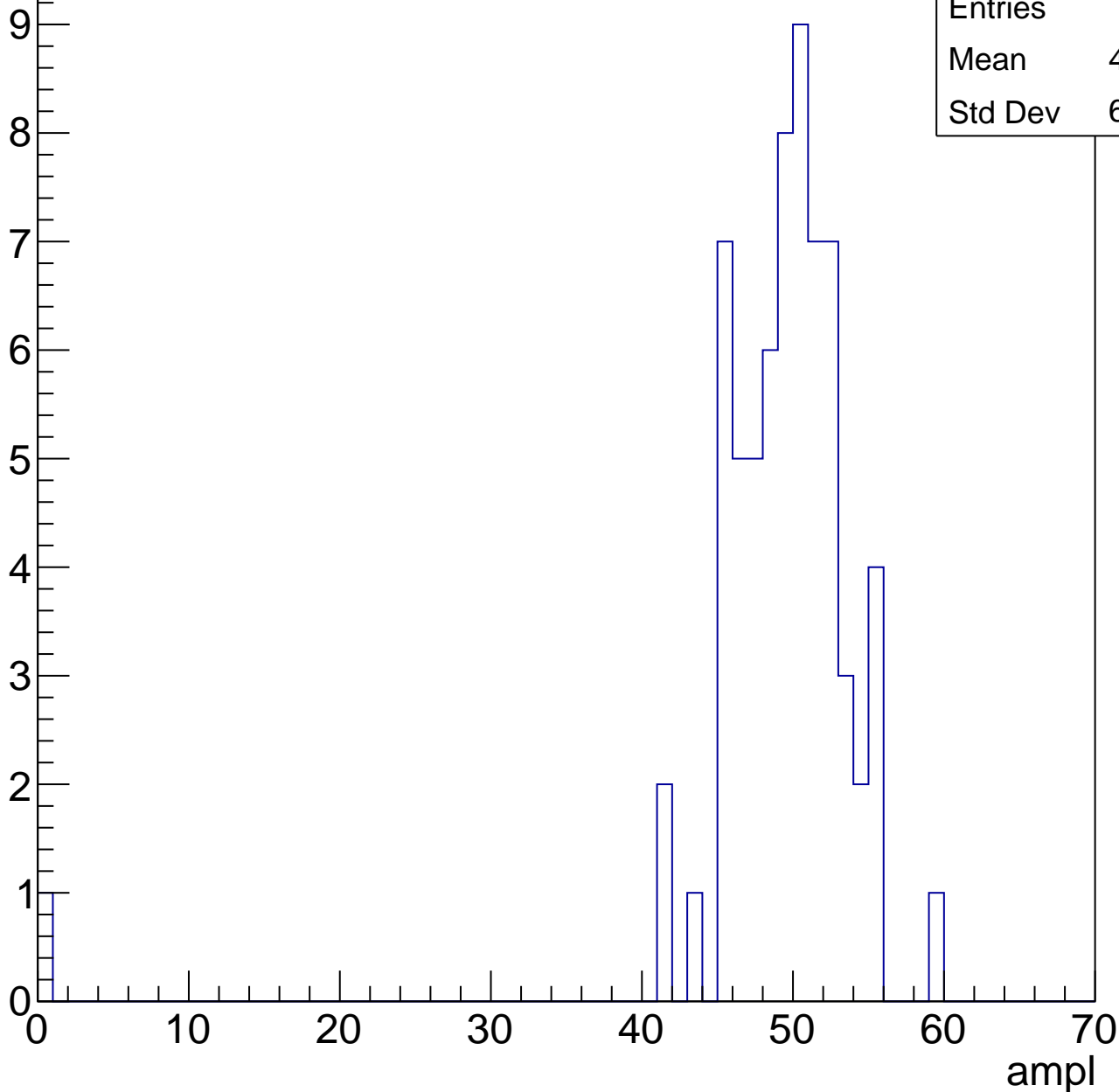


B1L103S, U9-ch43, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	48.56
Std Dev	6.835

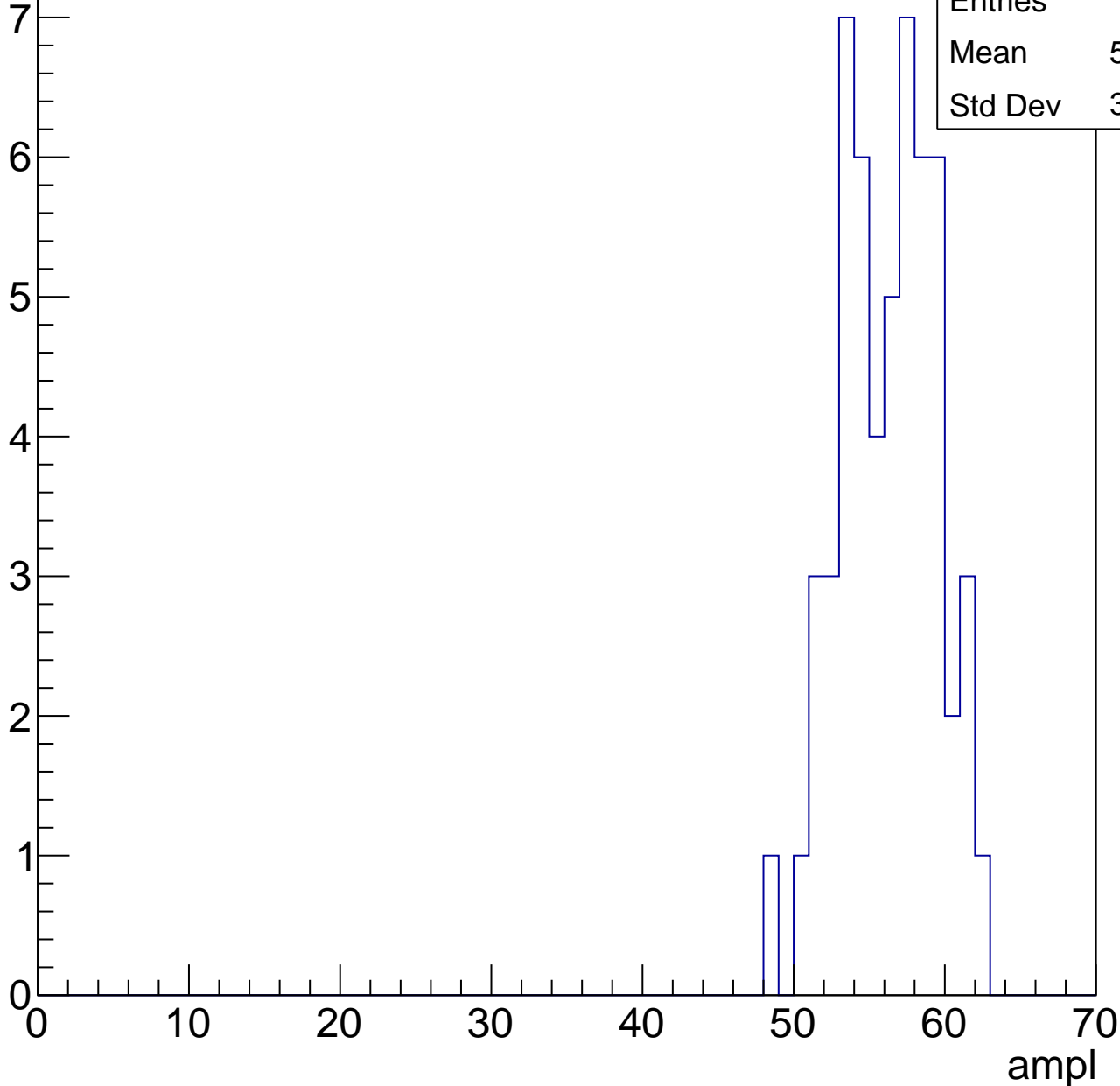


B1L103S, U9-ch43, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	55.78
Std Dev	3.132



B1L103S, U9-ch43, adc5

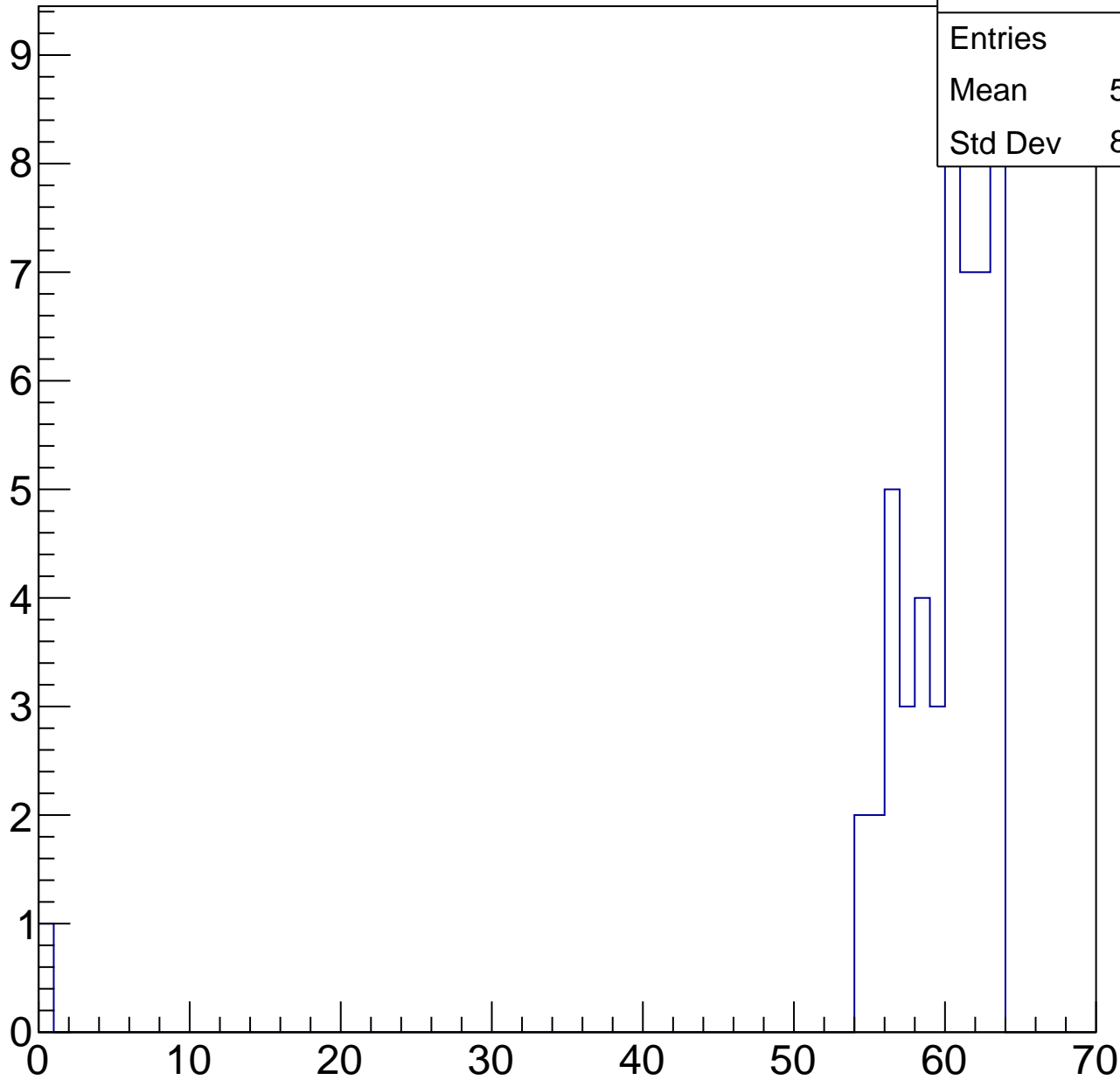
calib_packv5_041523_1651.root, FC#0, port C2

Entry

9
8
7
6
5
4
3
2
1
0

Entries	51
Mean	58.55
Std Dev	8.696

ampl



B1L103S, U9-ch43, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	3
Mean	62.33
Std Dev	0.4714

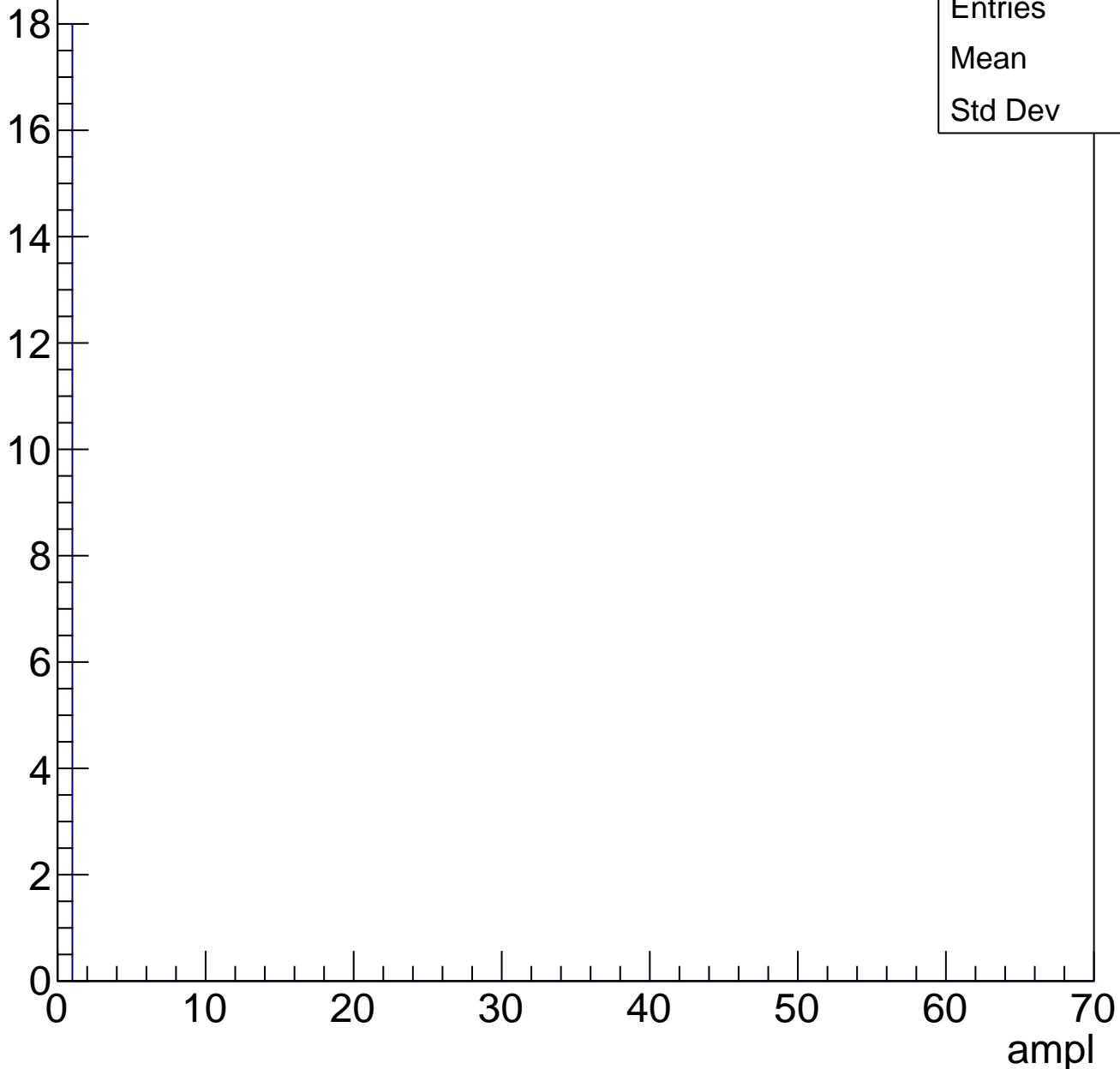
ampl

0 10 20 30 40 50 60 70

B1L103S, U9-ch43, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



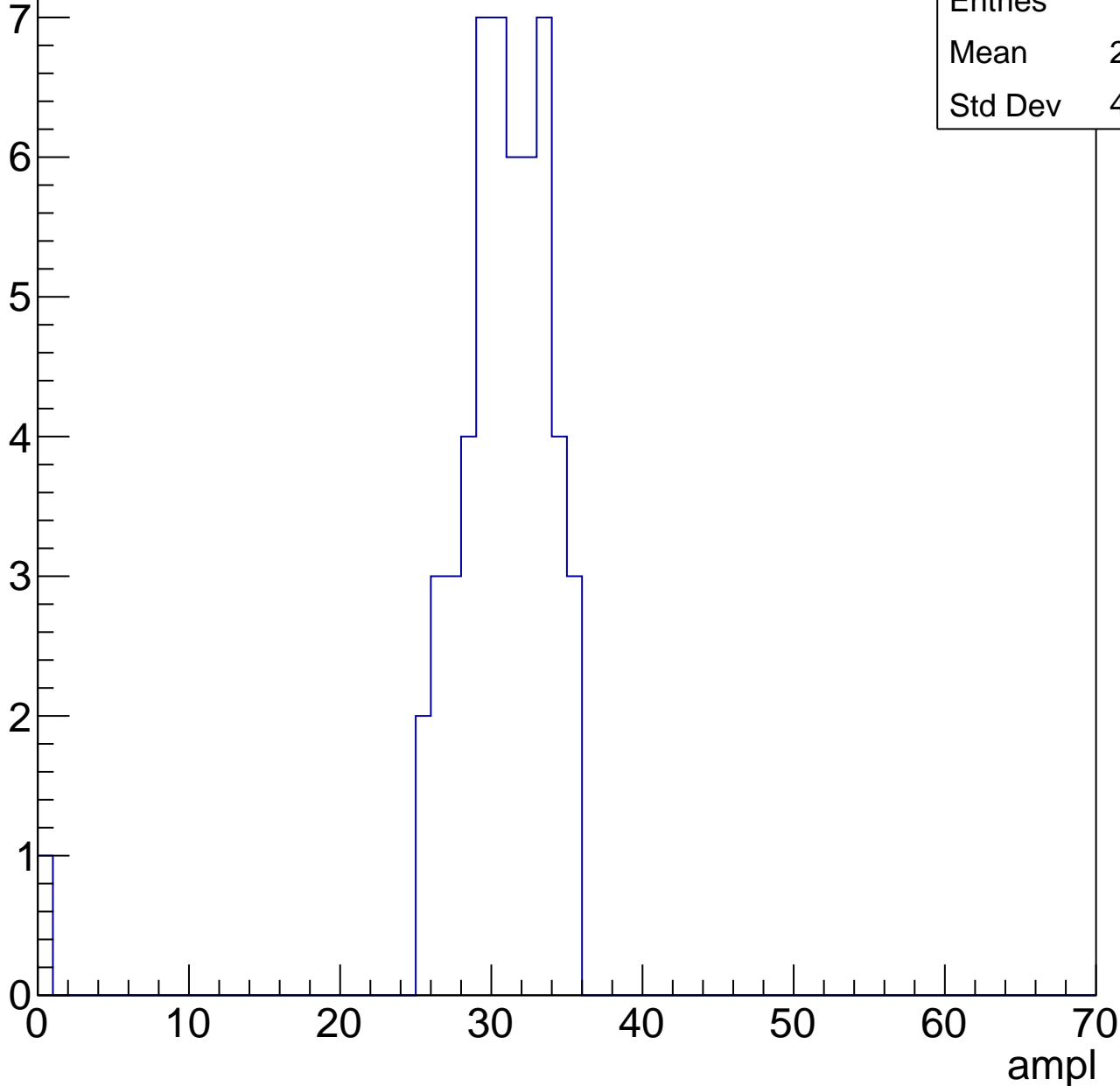
Entries	18
Mean	0
Std Dev	0

B1L103S, U9-ch44, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	29.89
Std Dev	4.913



B1L103S, U9-ch44, adc1

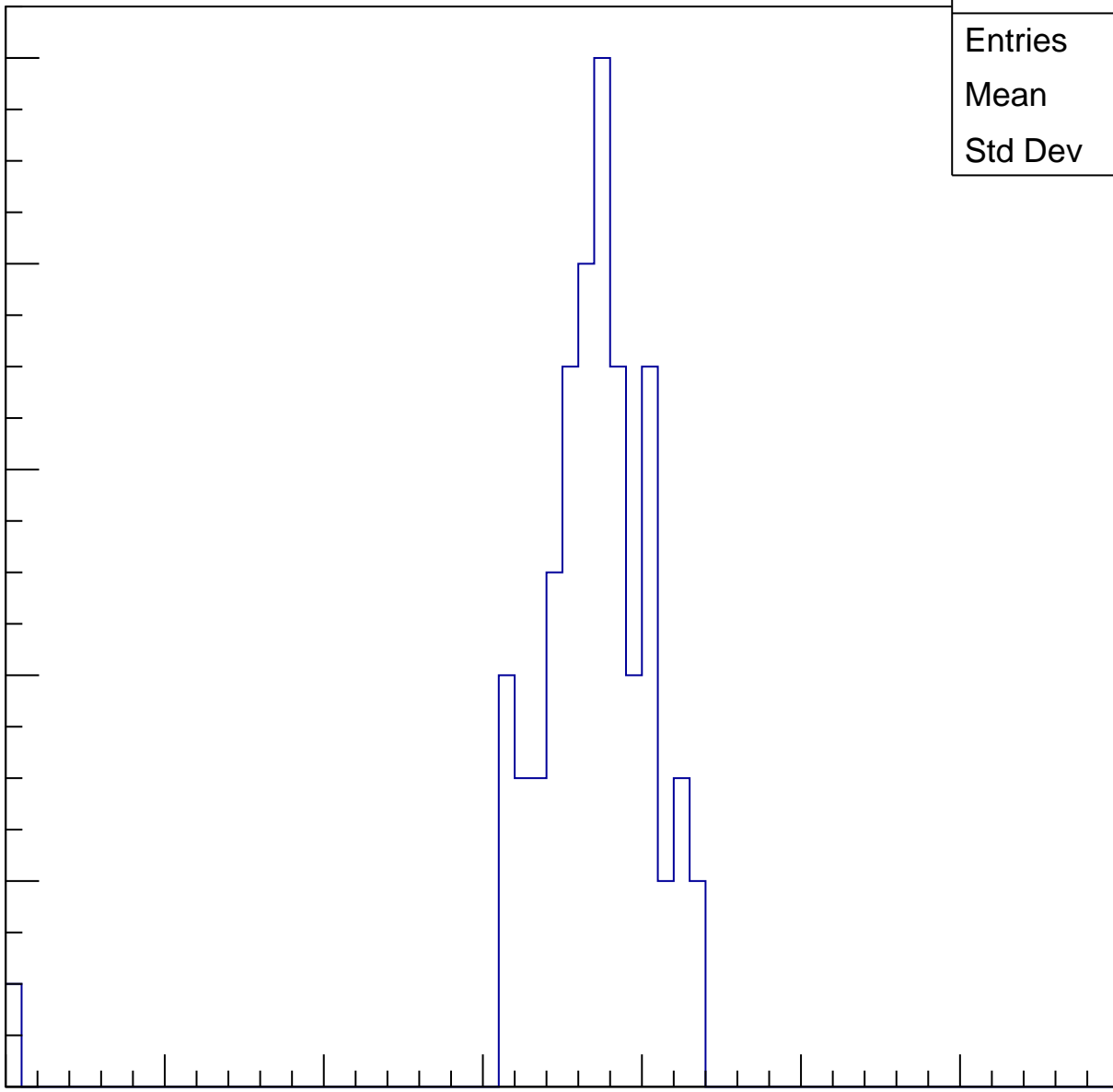
calib_packv5_041523_1651.root, FC#0, port C2

Entries	66
Mean	36.18
Std Dev	5.419

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70
ampl



B1L103S, U9-ch44, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

8

6

4

2

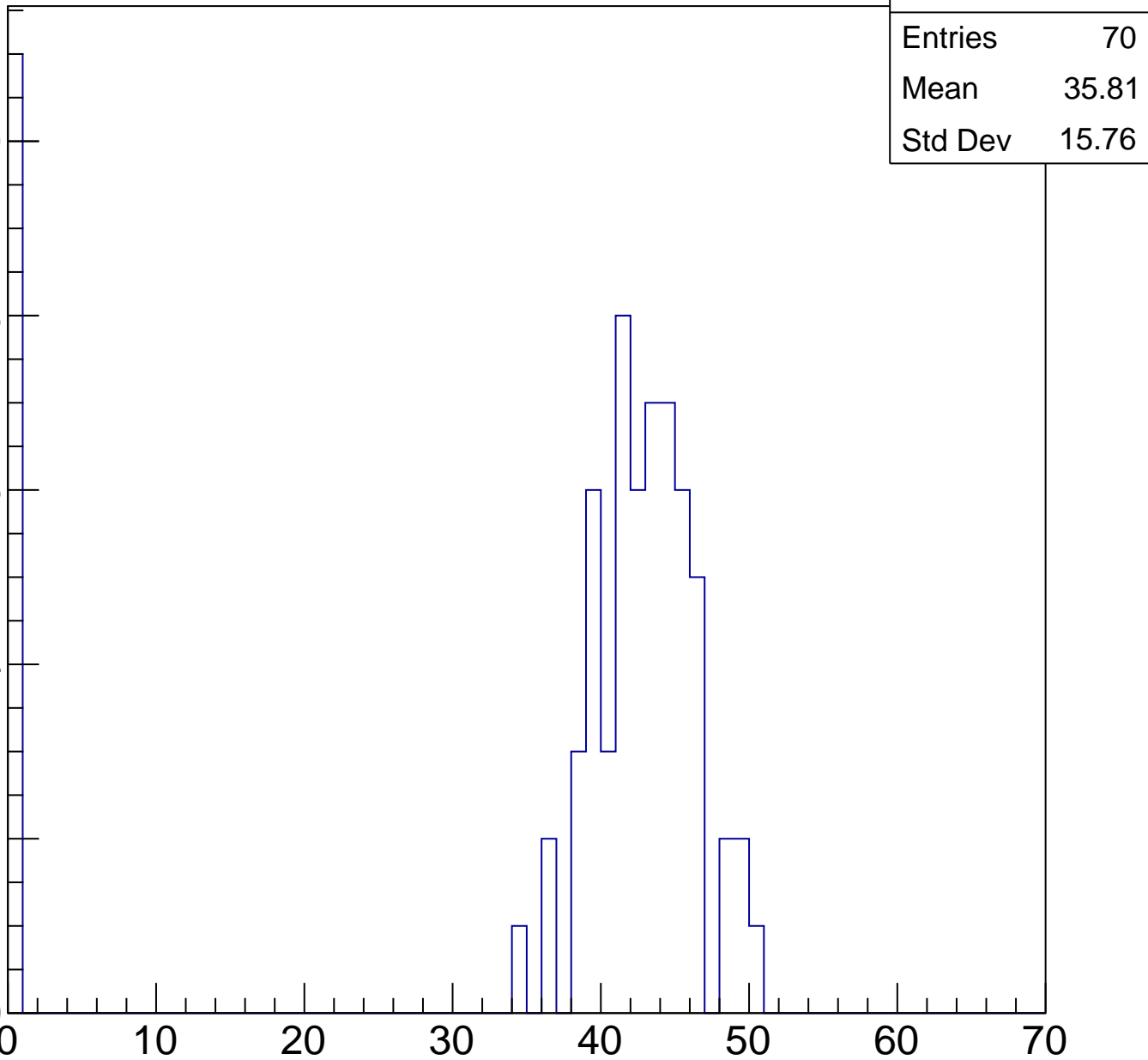
0

Entries 70

Mean 35.81

Std Dev 15.76

ampl



B1L103S, U9-ch44, adc3

calib_packv5_041523_1651.root, FC#0, port C2

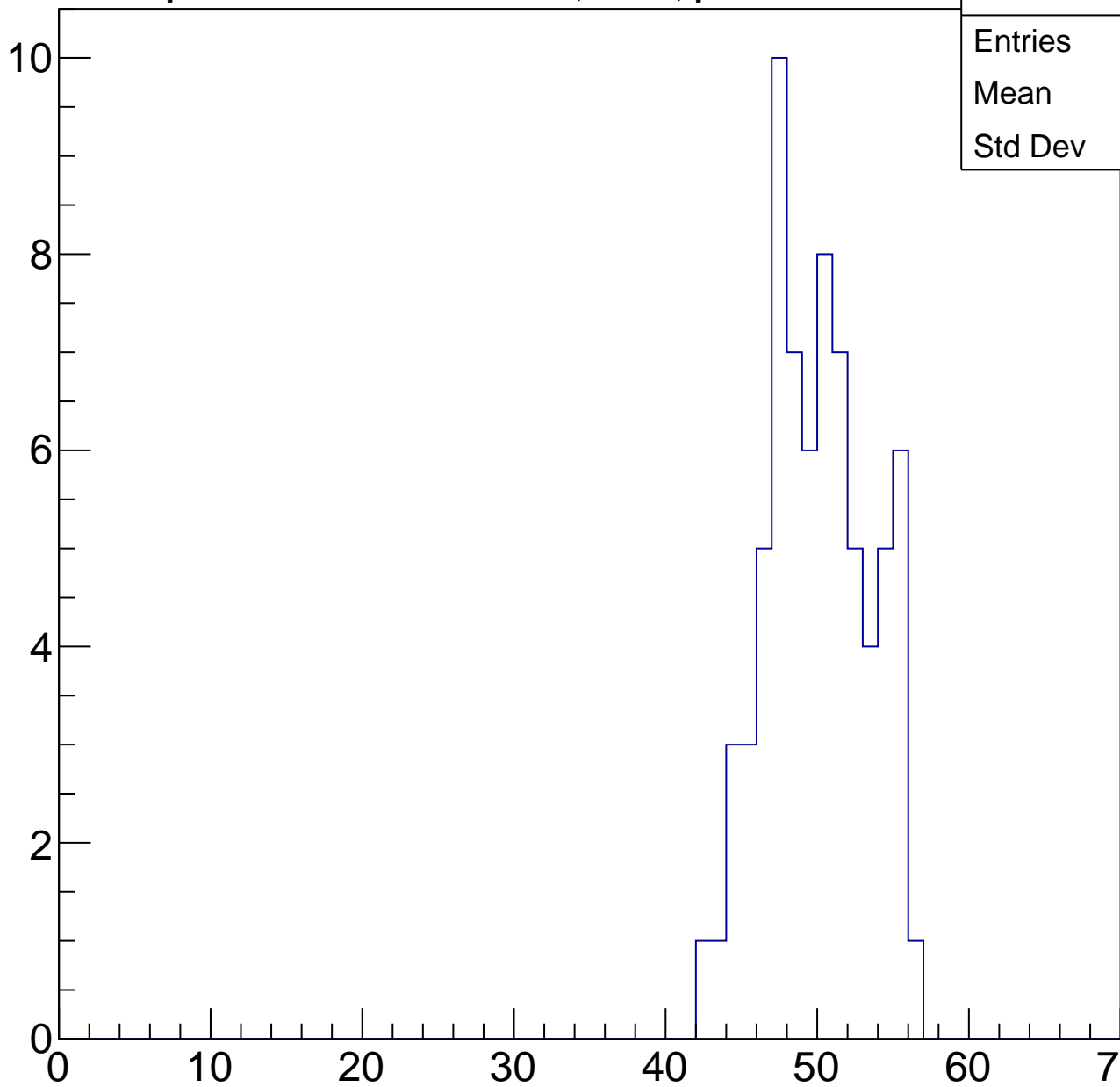
Entries	72
Mean	49.54
Std Dev	3.362

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

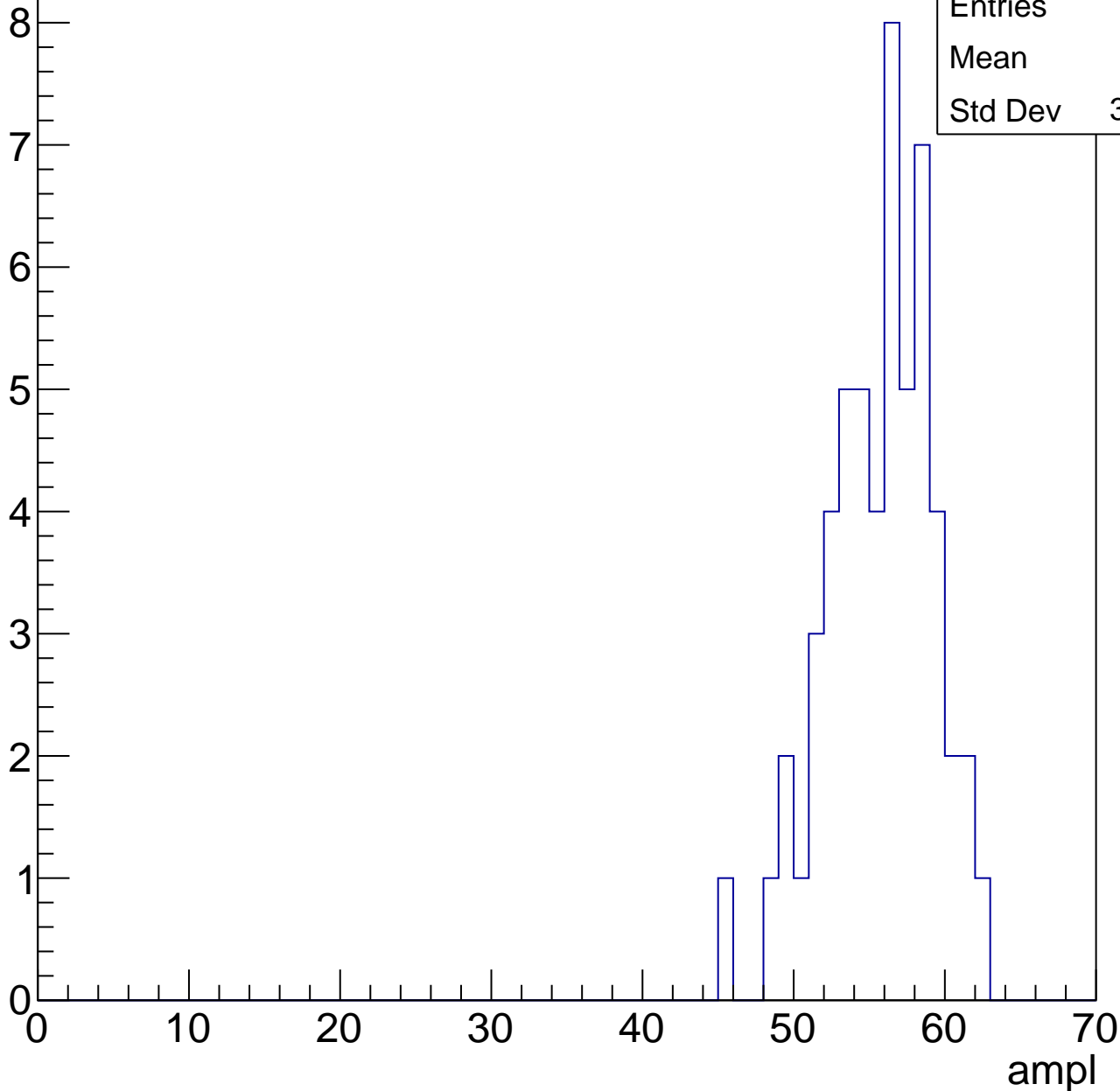


B1L103S, U9-ch44, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	55.2
Std Dev	3.513

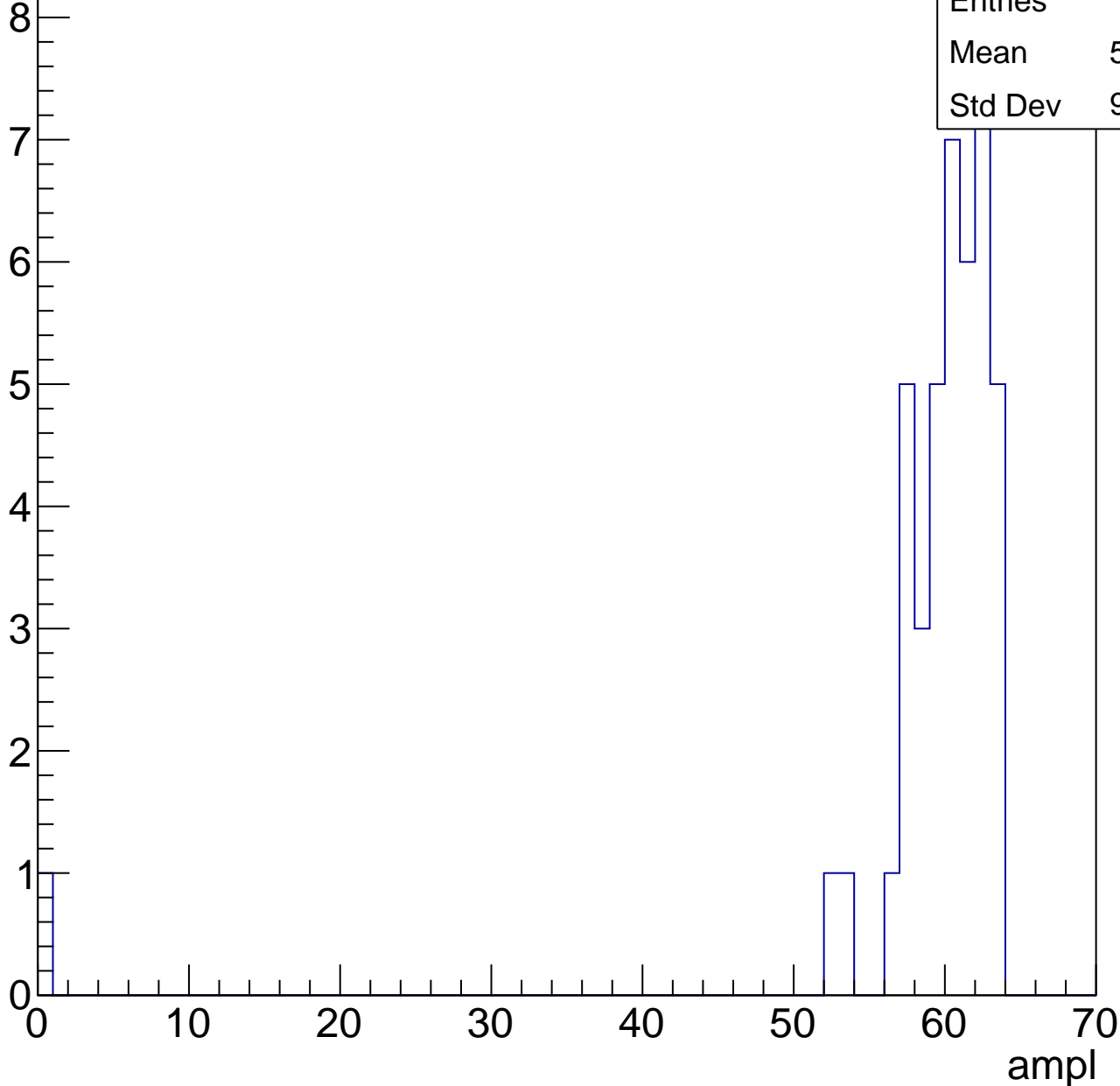


B1L103S, U9-ch44, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	43
Mean	58.42
Std Dev	9.359

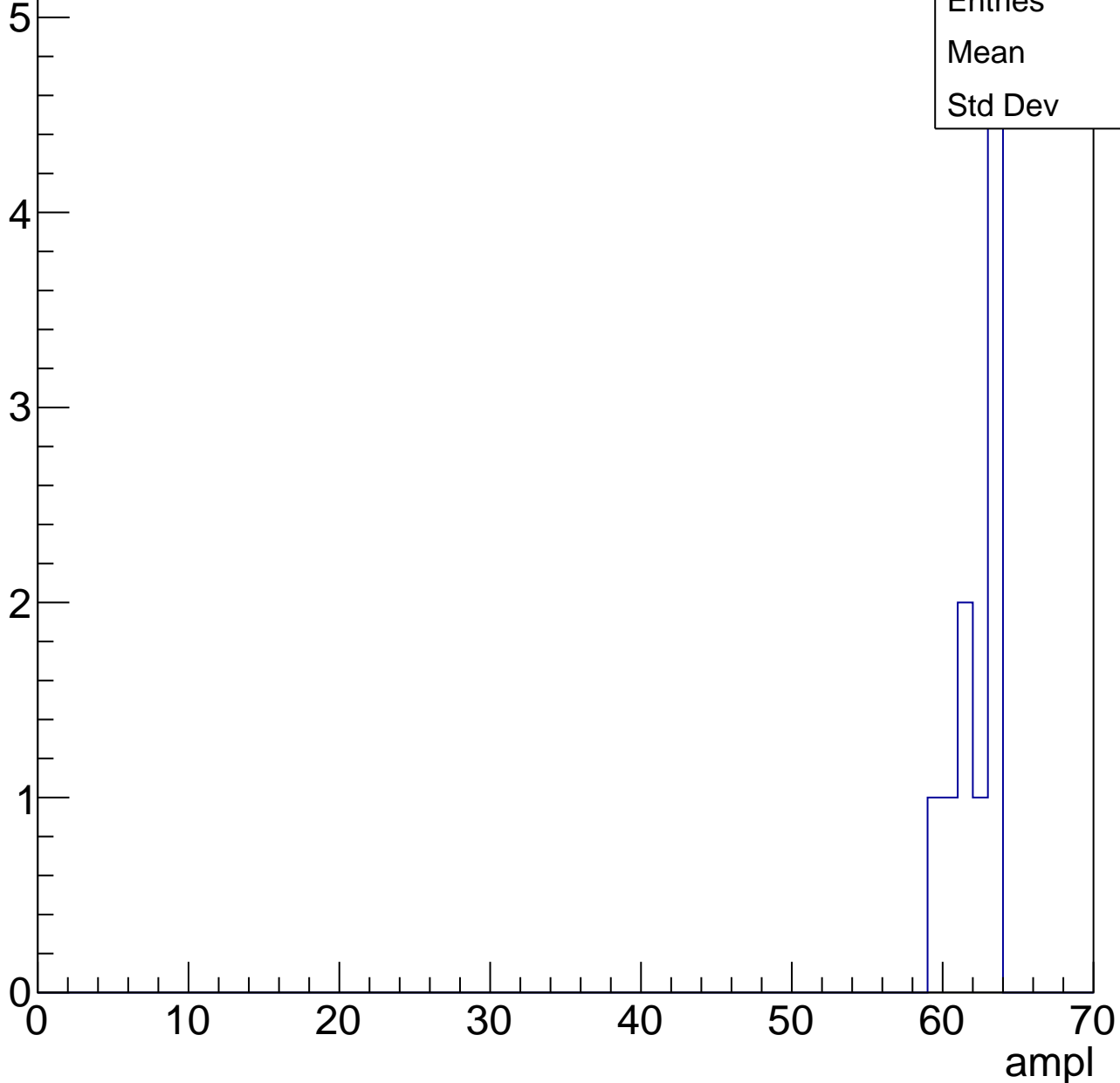


B1L103S, U9-ch44, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	10
Mean	61.8
Std Dev	1.4



B1L103S, U9-ch44, adc7

calib_packv5_041523_1651.root, FC#0, port C2

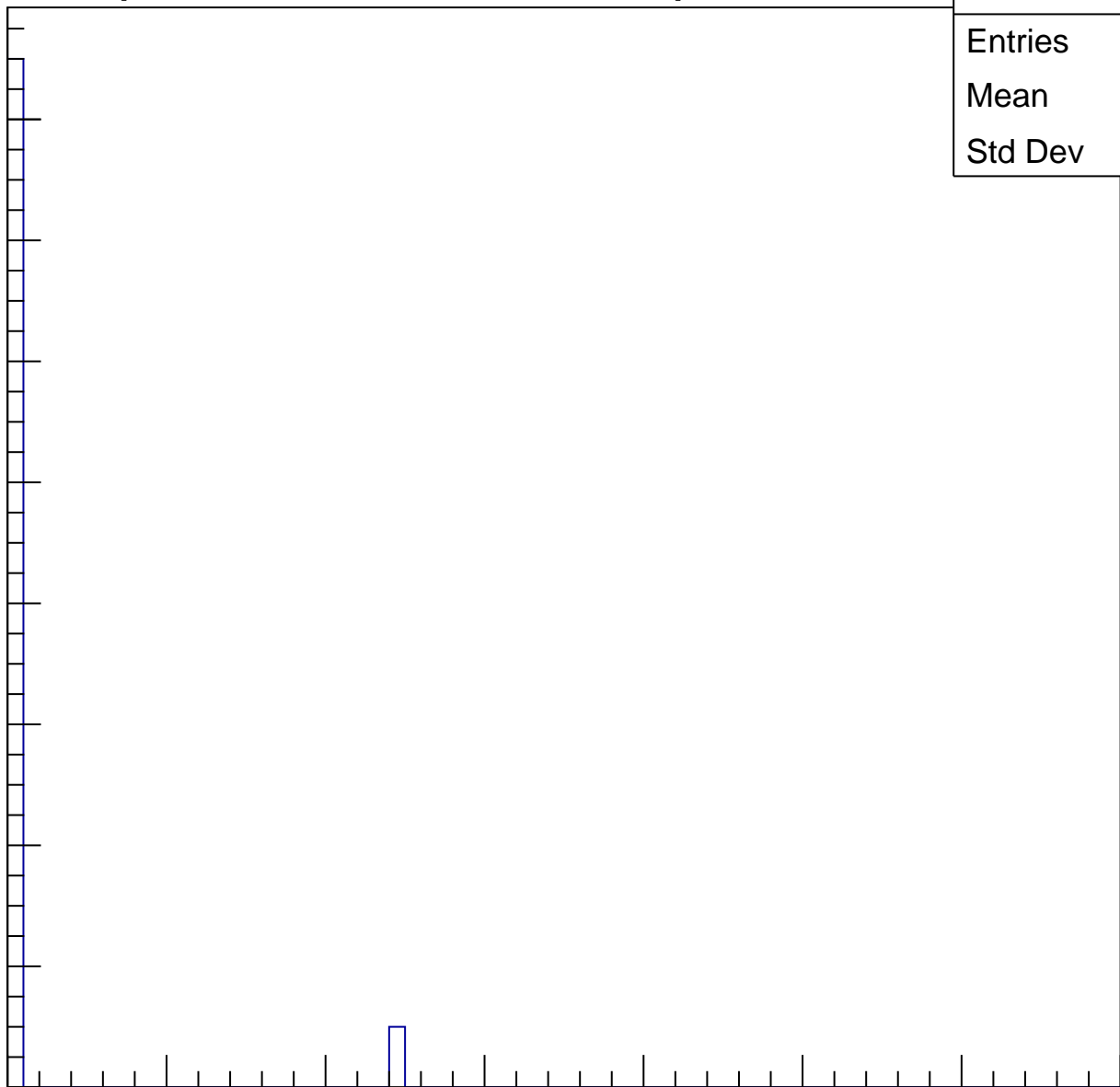
Entries	18
Mean	1.333
Std Dev	5.497

Entry

16
14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U9-ch45, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	67
Mean	24.85
Std Dev	11.5

Entry

10

8

6

4

2

0

0

10

20

30

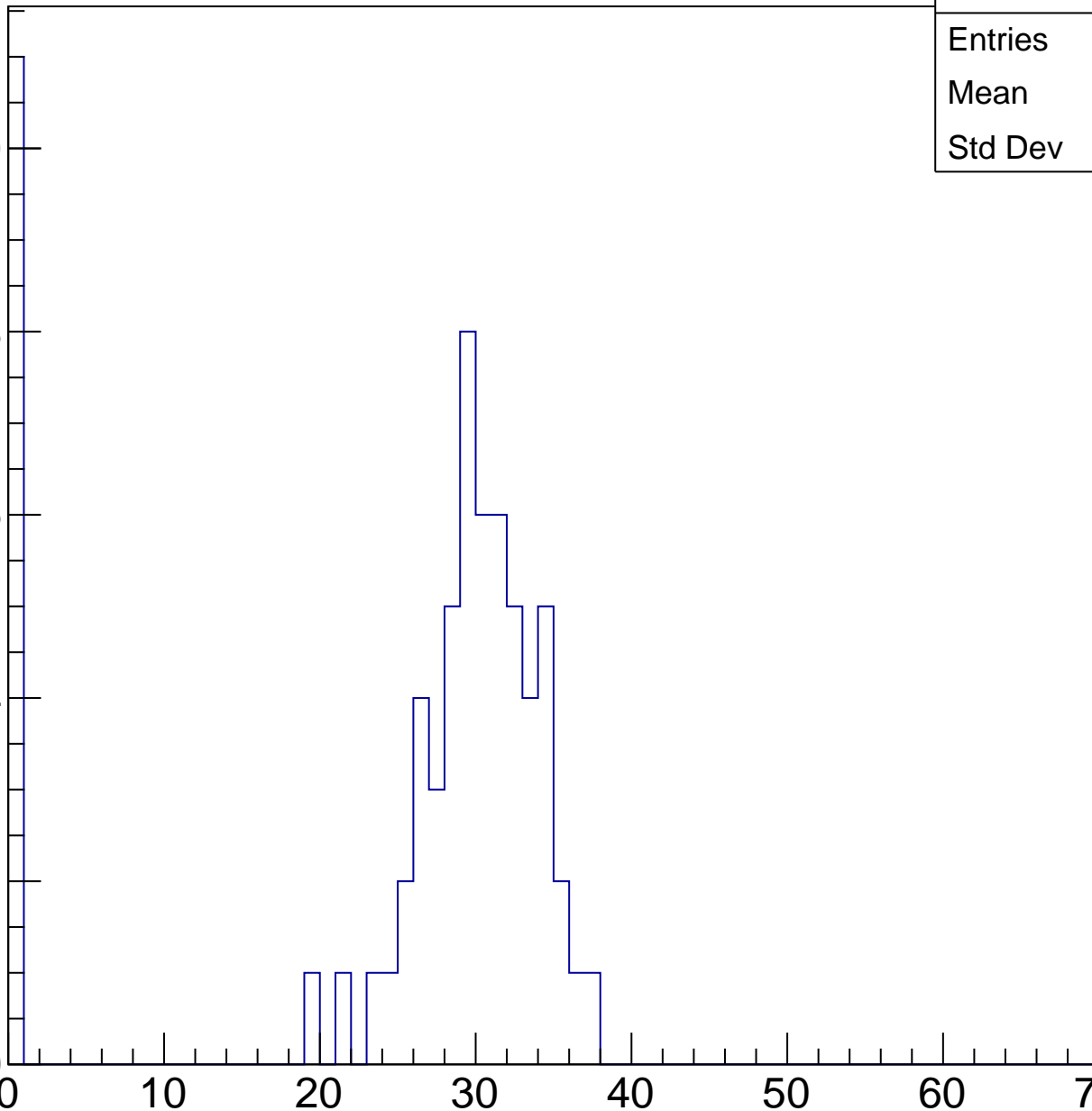
40

50

60

70

ampl

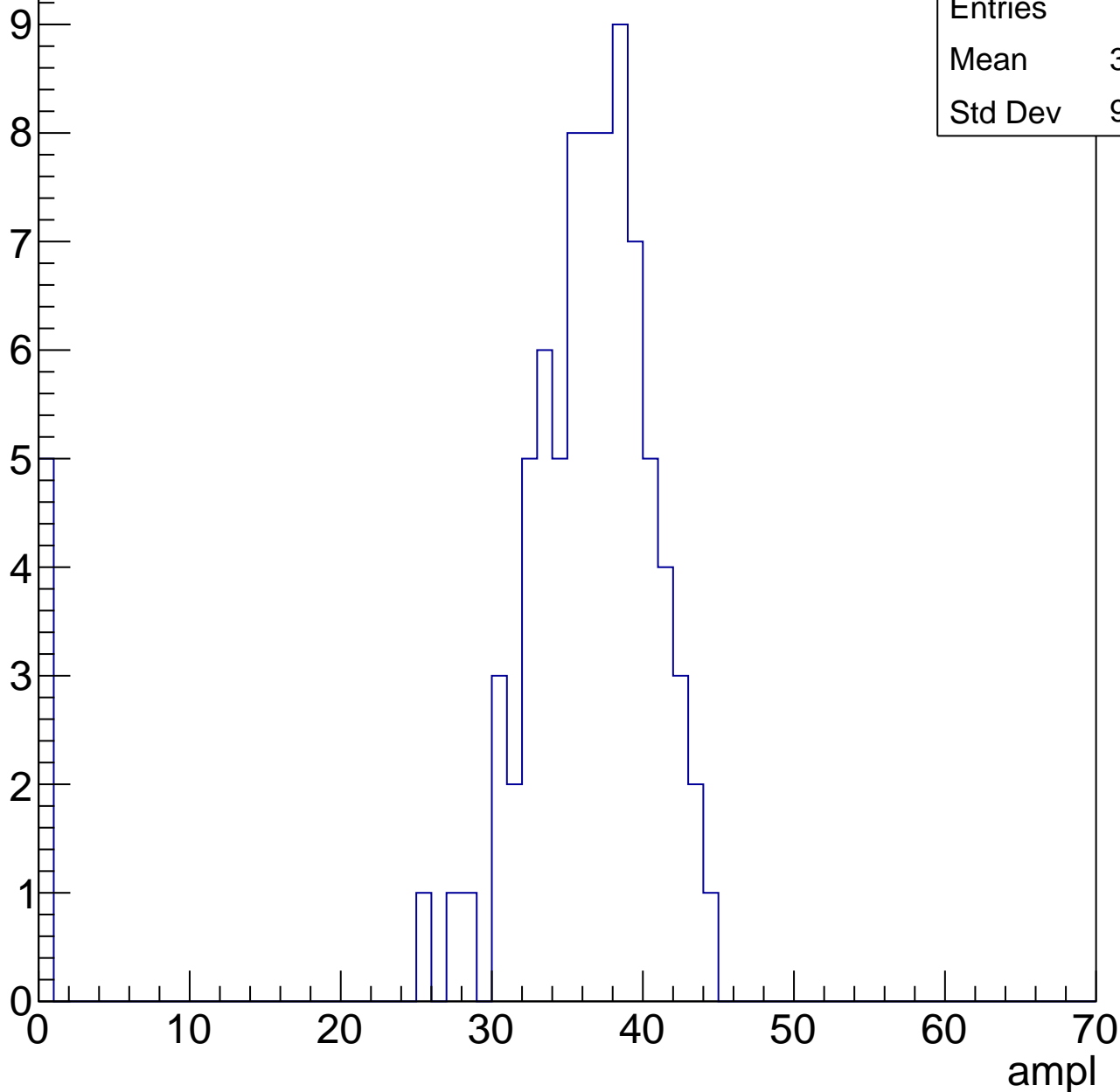


B1L103S, U9-ch45, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

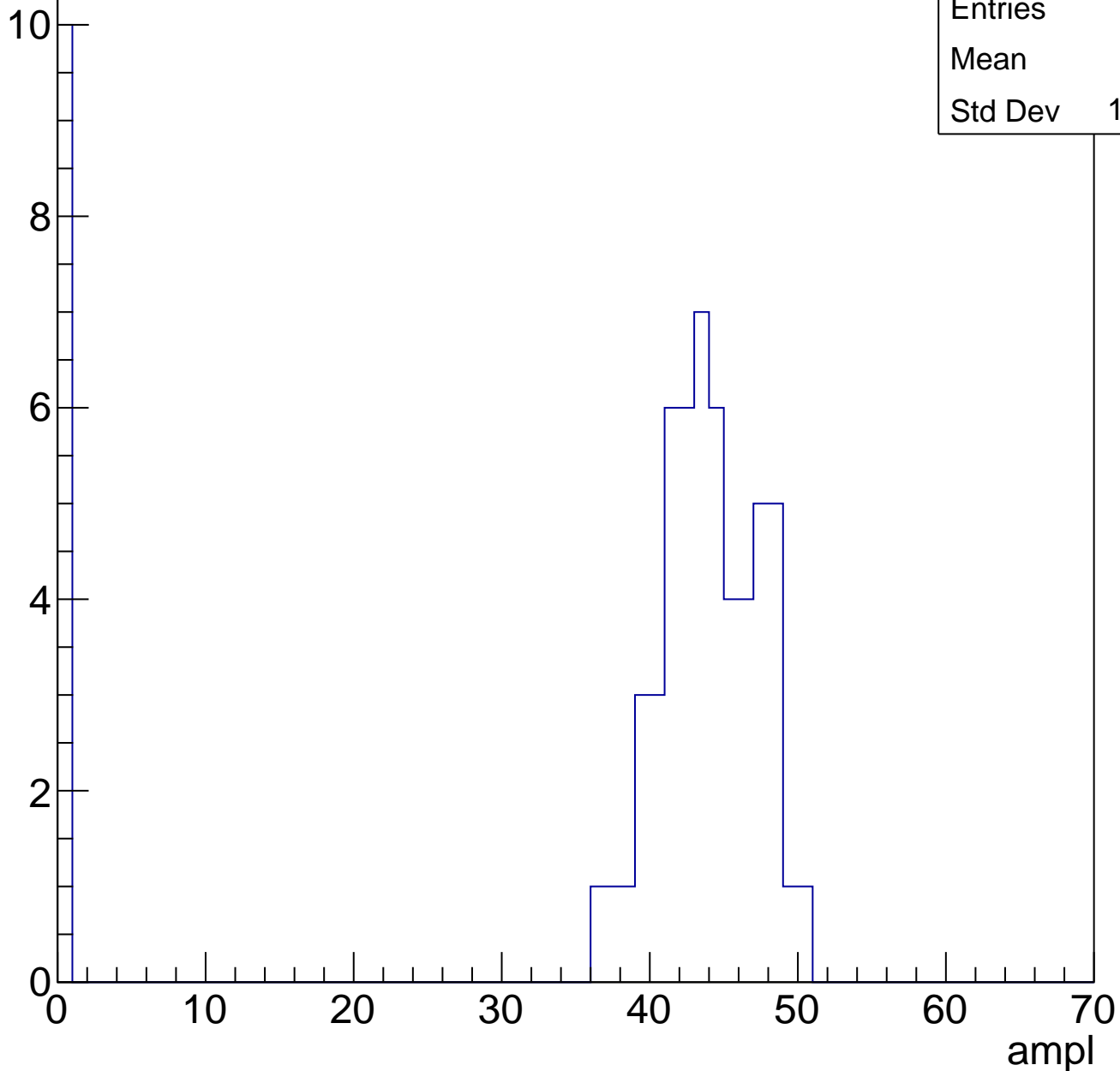
Entries	84
Mean	34.04
Std Dev	9.322



B1L103S, U9-ch45, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

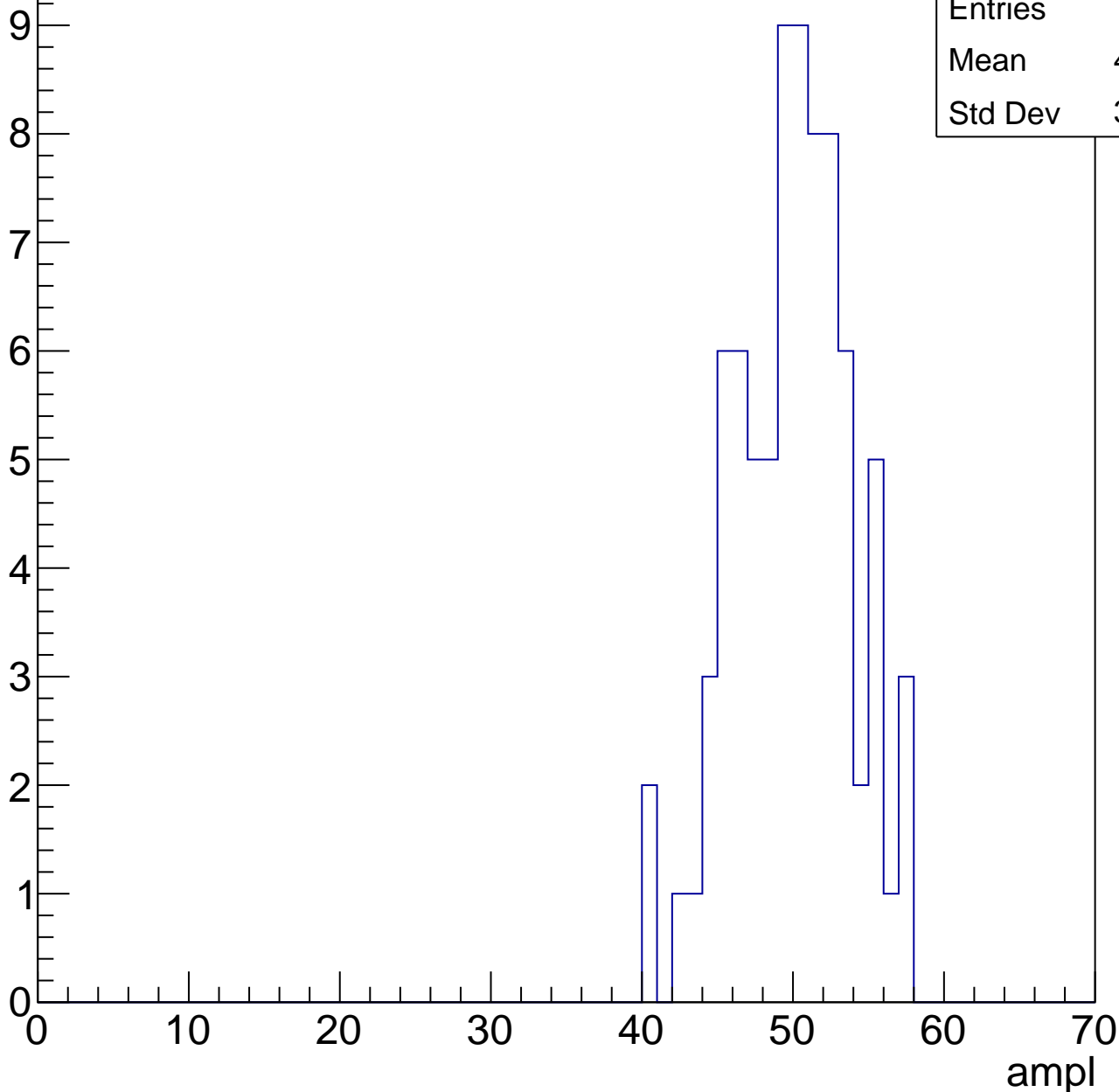


B1L103S, U9-ch45, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	80
Mean	49.51
Std Dev	3.801



B1L103S, U9-ch45, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

7

6

5

4

3

2

1

0

Entries 44

Mean 56.09

Std Dev 2.778

0

10

20

30

40

50

60

ampl

0

10

20

30

40

50

60

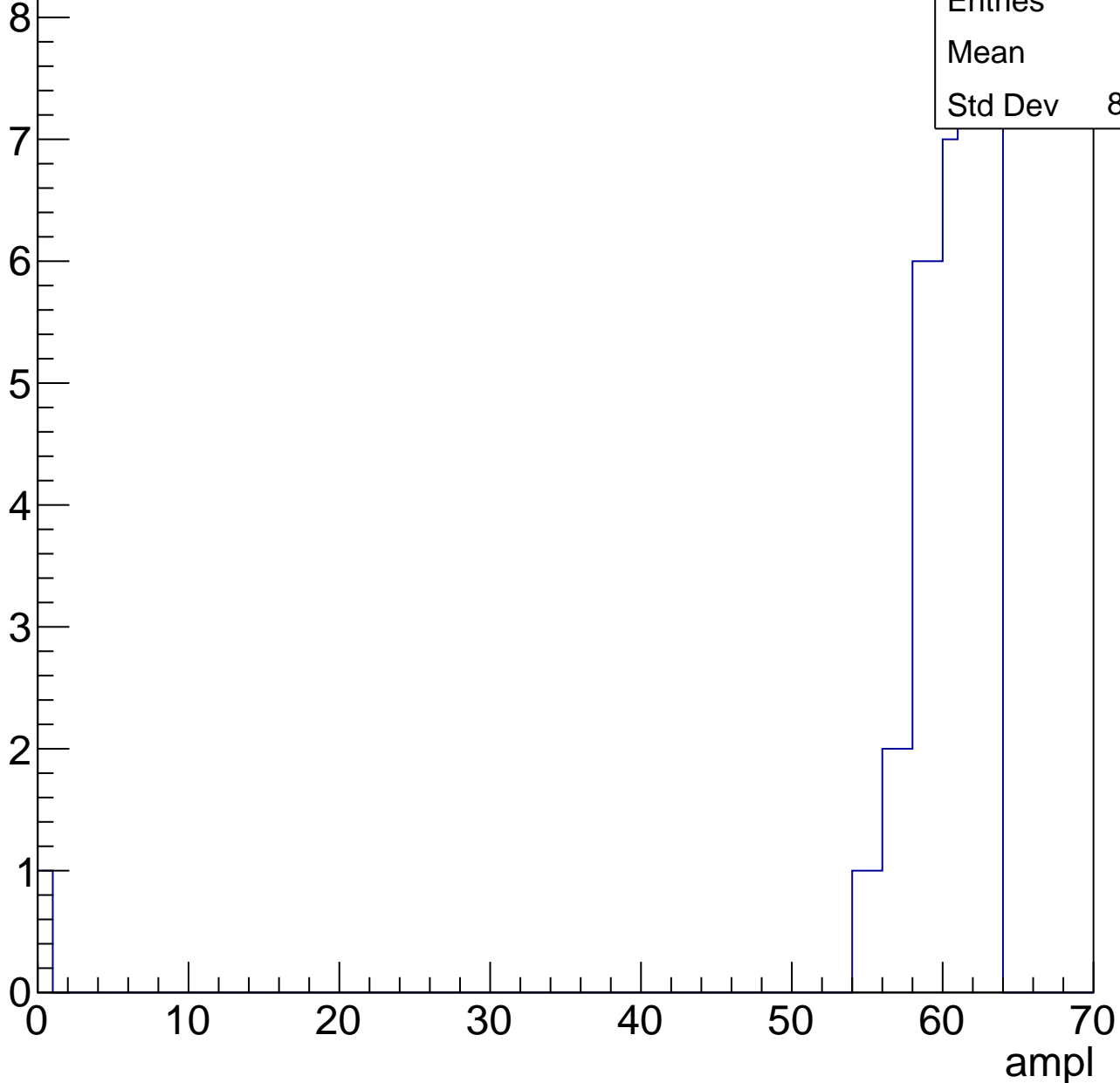
70

B1L103S, U9-ch45, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	58.9
Std Dev	8.709



B1L103S, U9-ch45, adc6

calib_packv5_041523_1651.root, FC#0, port C2

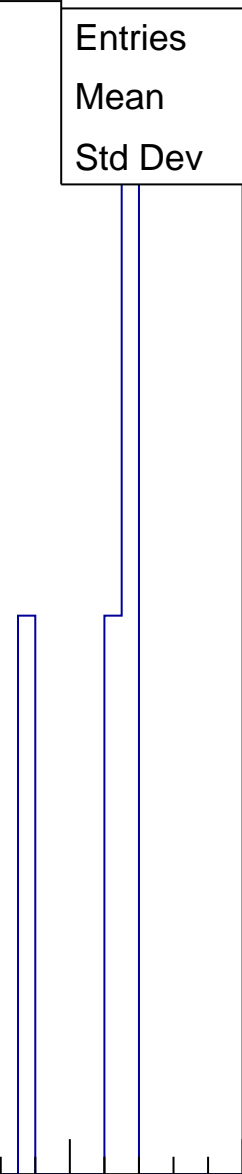
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	4
Mean	61.25
Std Dev	2.487

ampl

0 10 20 30 40 50 60 70



B1L103S, U9-ch45, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

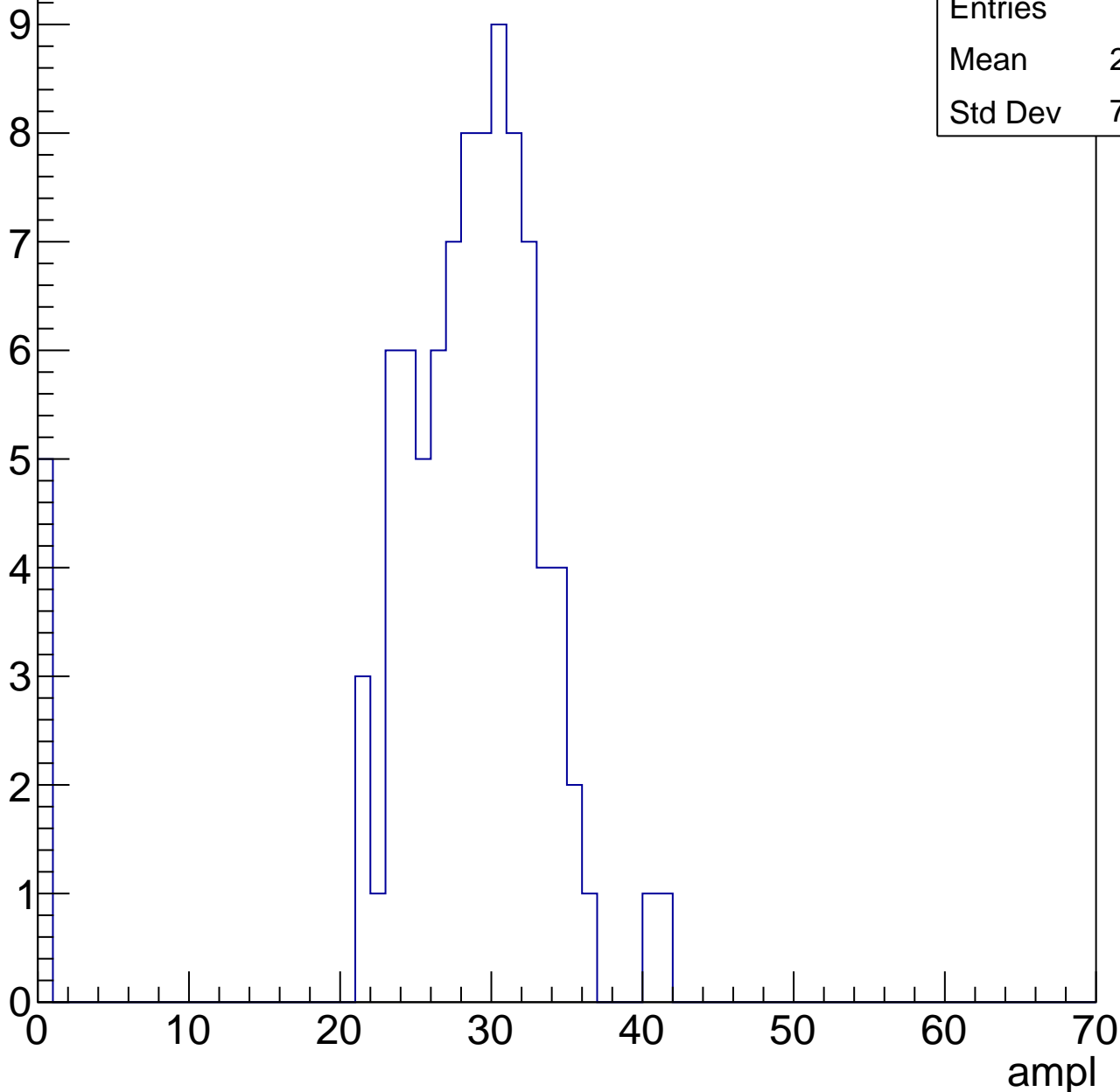
ampl

B1L103S, U9-ch46, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	92
Mean	27.07
Std Dev	7.584

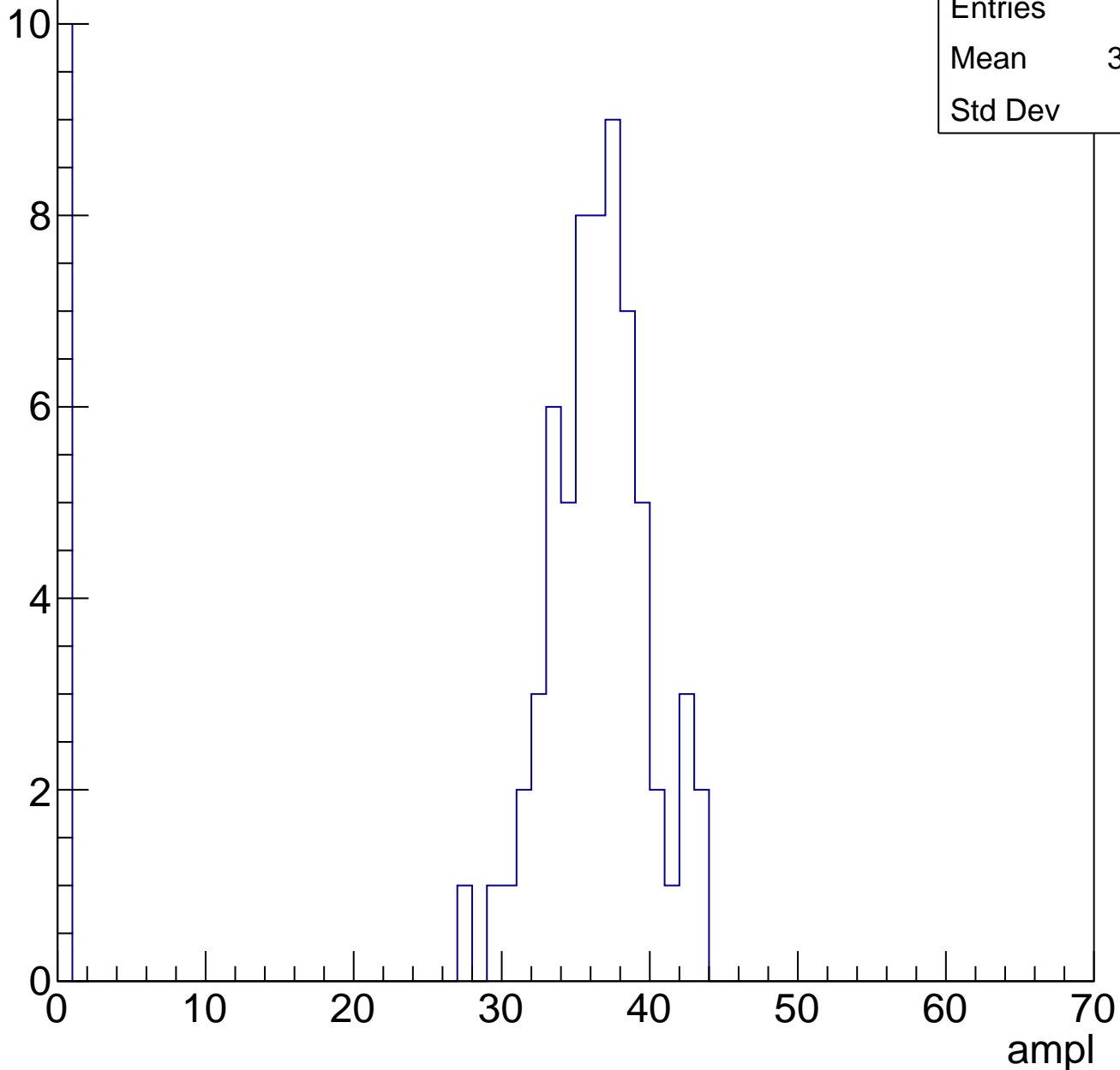


B1L103S, U9-ch46, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	74
Mean	31.18
Std Dev	12.7

Entry

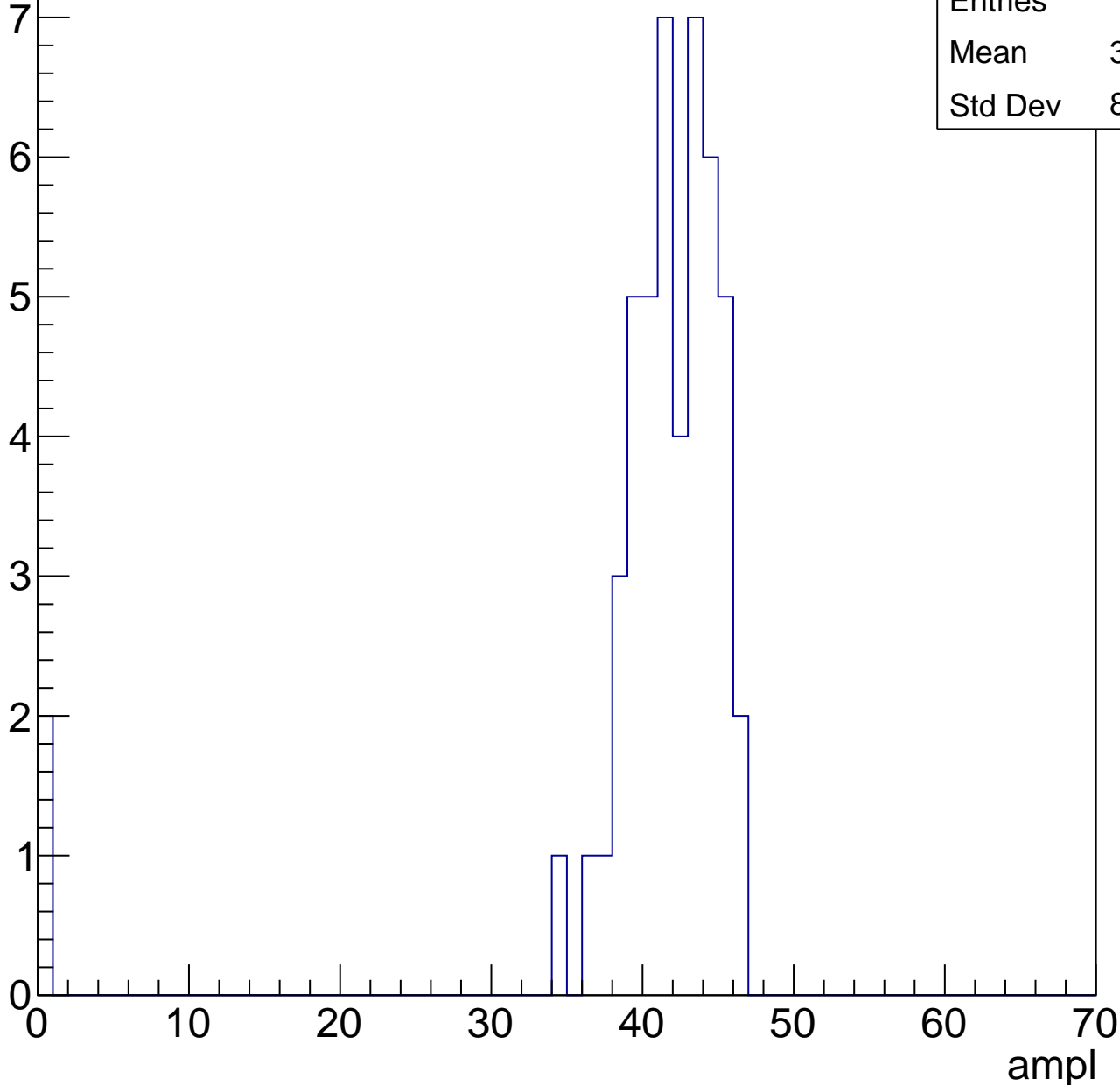


B1L103S, U9-ch46, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

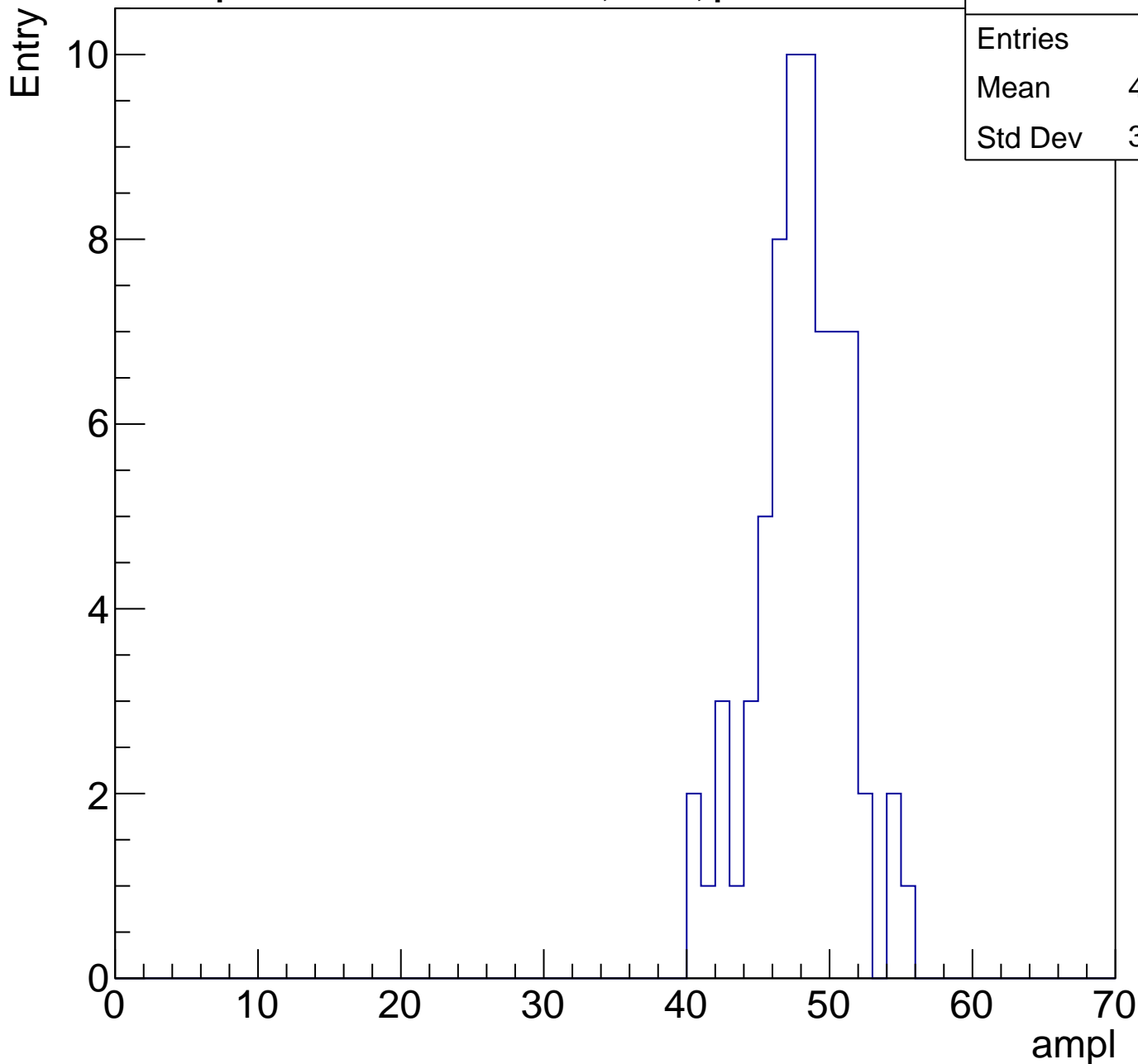
Entries	49
Mean	39.86
Std Dev	8.638



B1L103S, U9-ch46, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	69
Mean	47.57
Std Dev	3.146

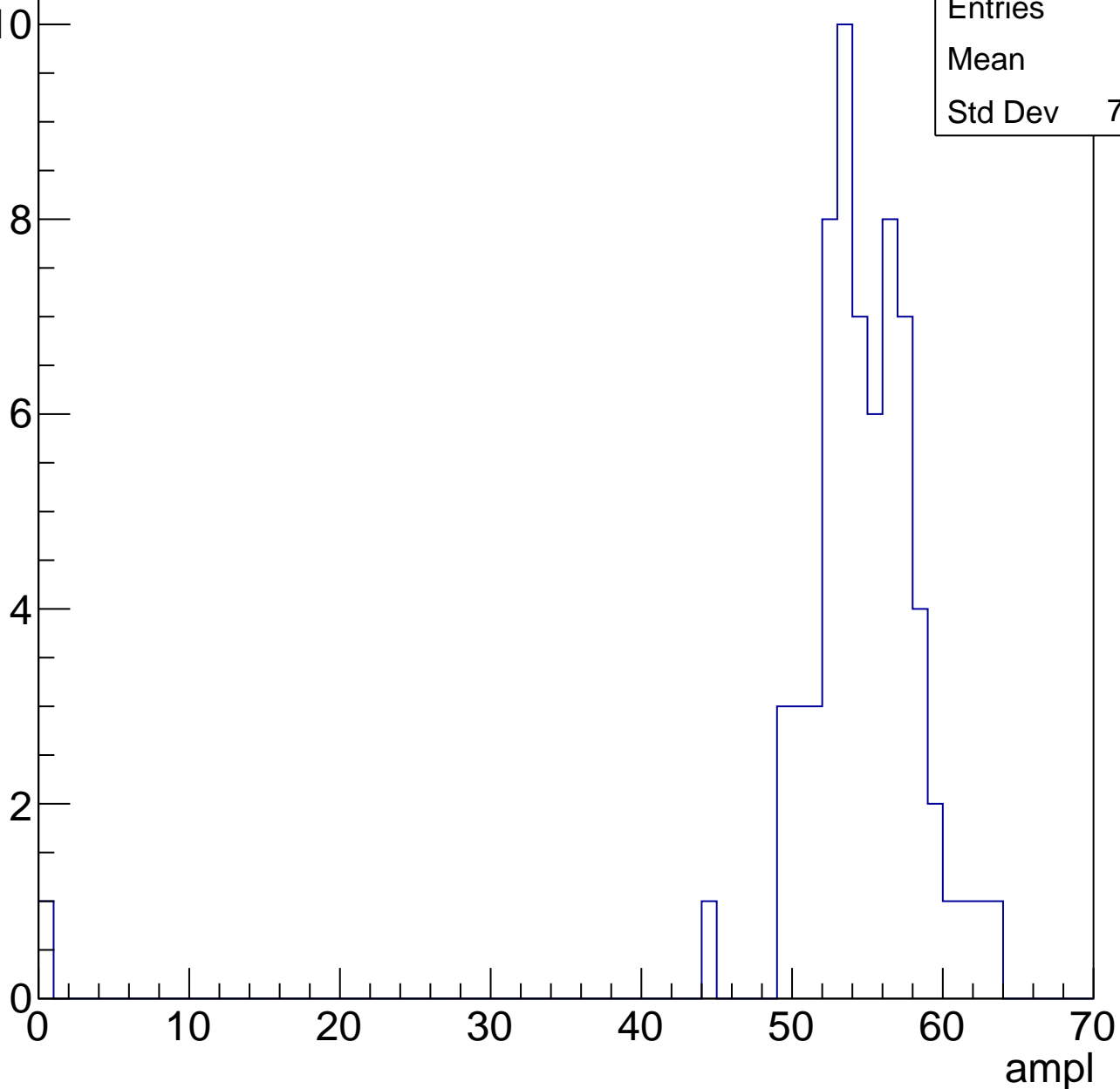


B1L103S, U9-ch46, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	53.6
Std Dev	7.373

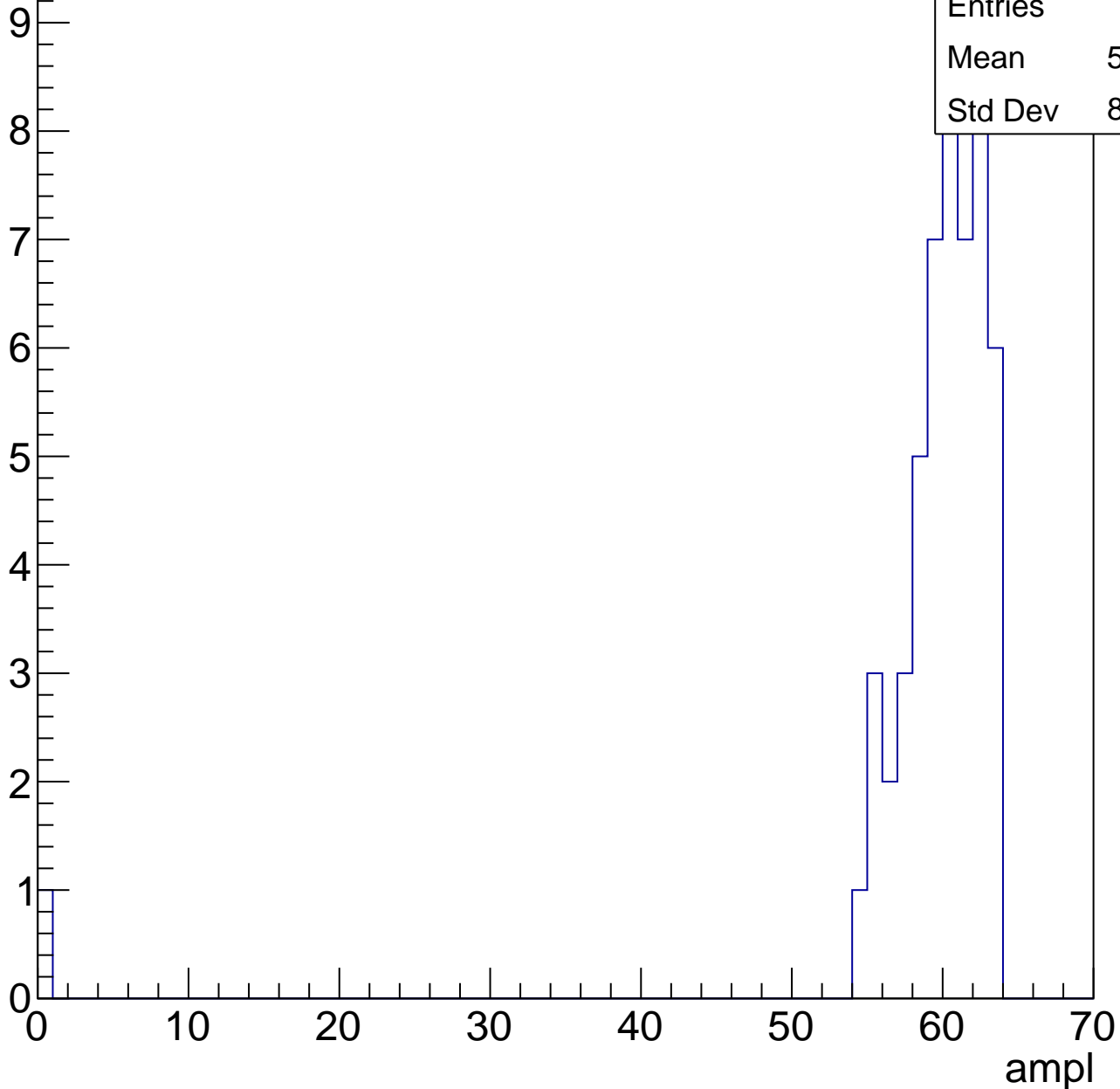


B1L103S, U9-ch46, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

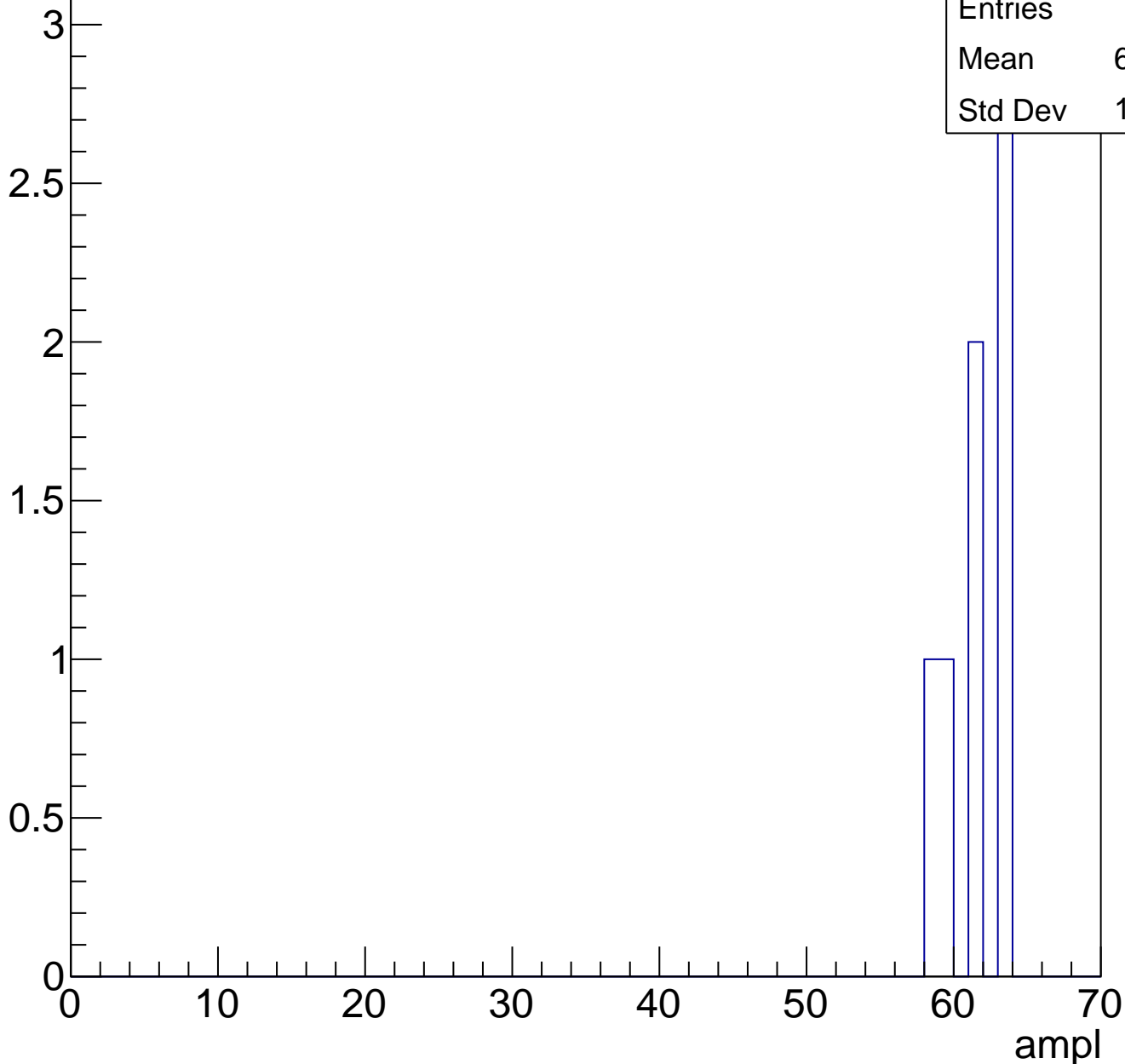
Entries	53
Mean	58.64
Std Dev	8.463



B1L103S, U9-ch46, adc6

calib_packv5_041523_1651.root, FC#0, port C2

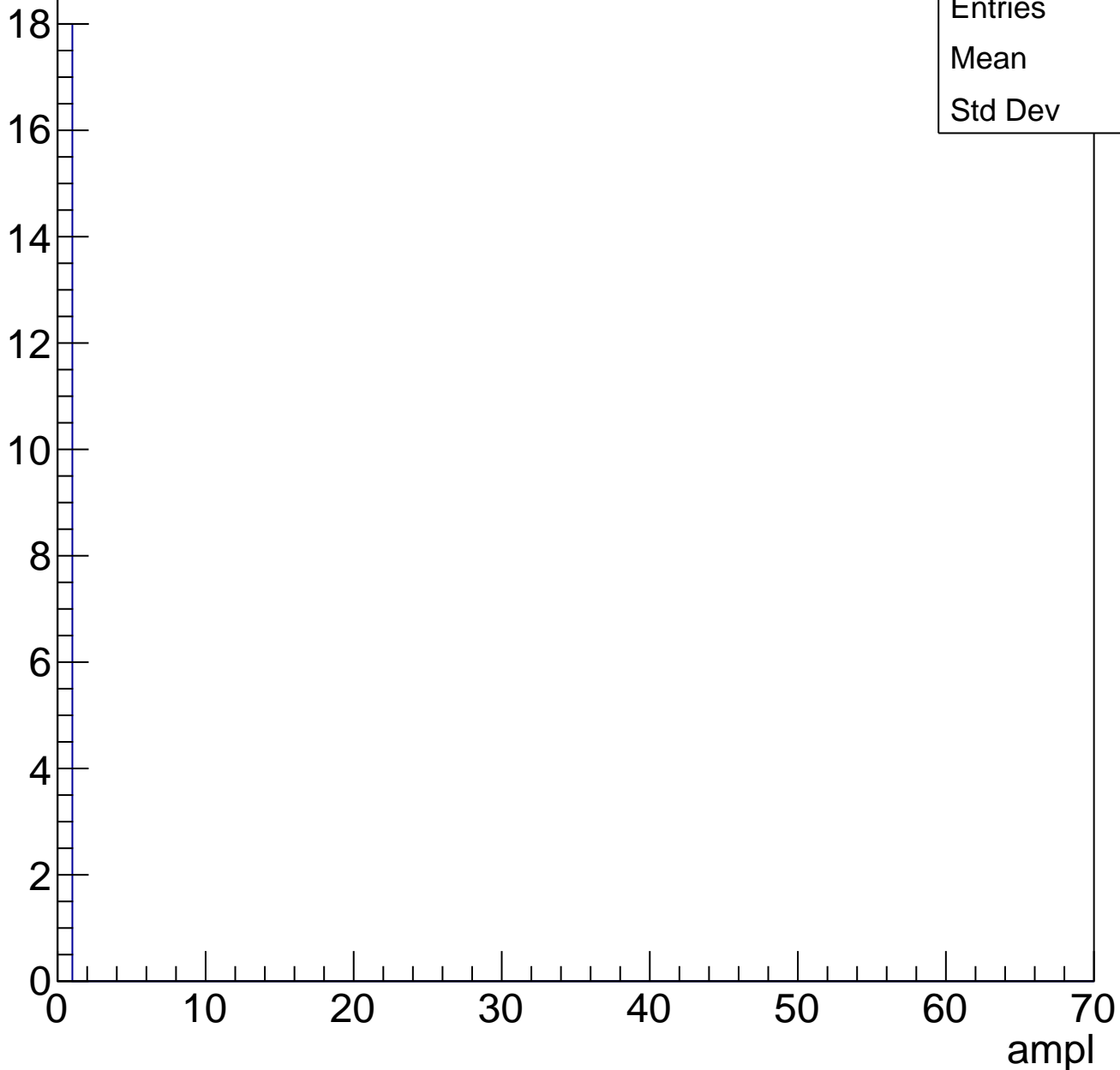
Entry



B1L103S, U9-ch46, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch47, adc0

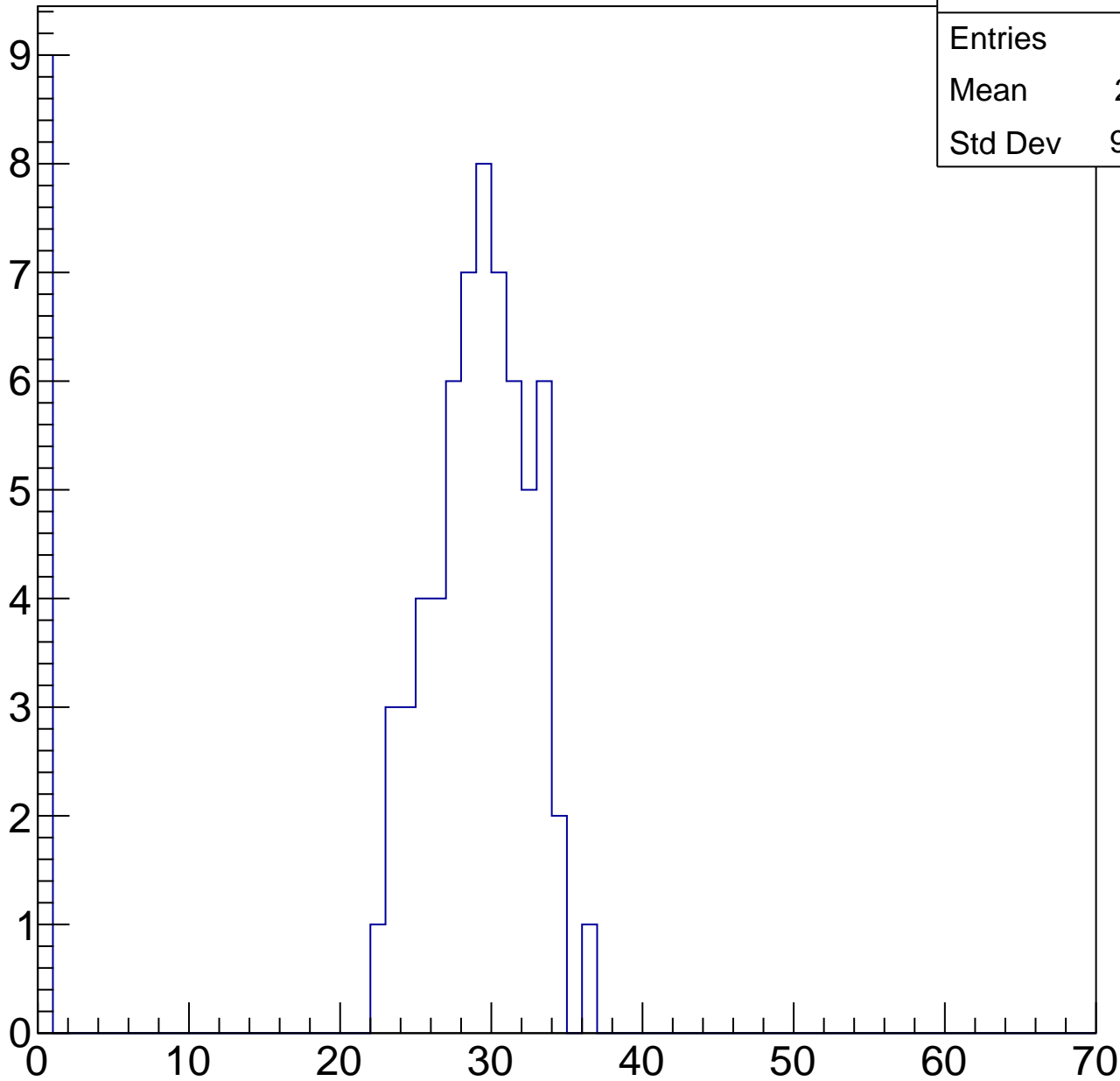
calib_packv5_041523_1651.root, FC#0, port C2

Entry

9
8
7
6
5
4
3
2
1
0

Entries	72
Mean	25.21
Std Dev	9.978

ampl

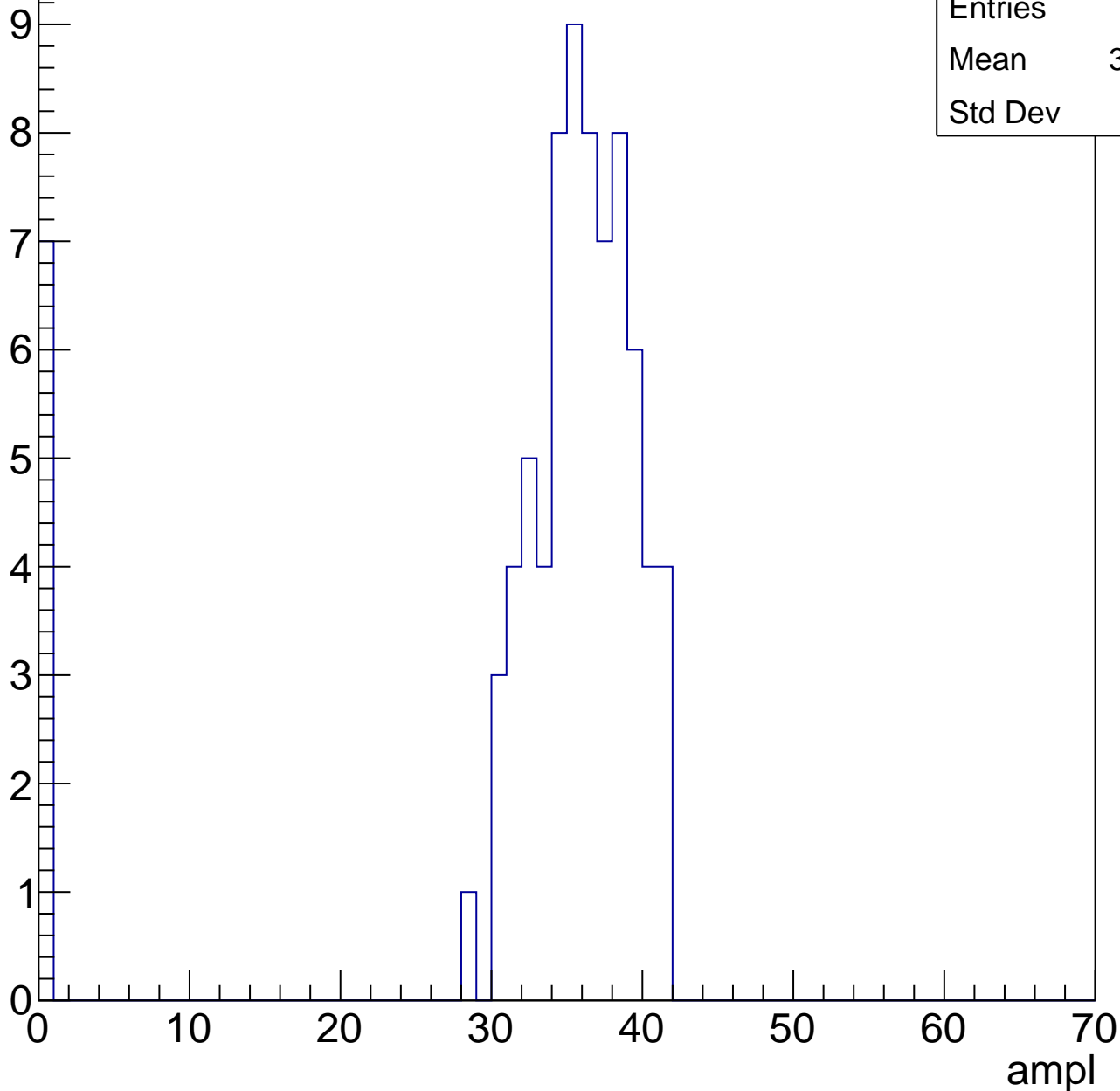


B1L103S, U9-ch47, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	32.44
Std Dev	10.6



B1L103S, U9-ch47, adc2

calib_packv5_041523_1651.root, FC#0, port C2

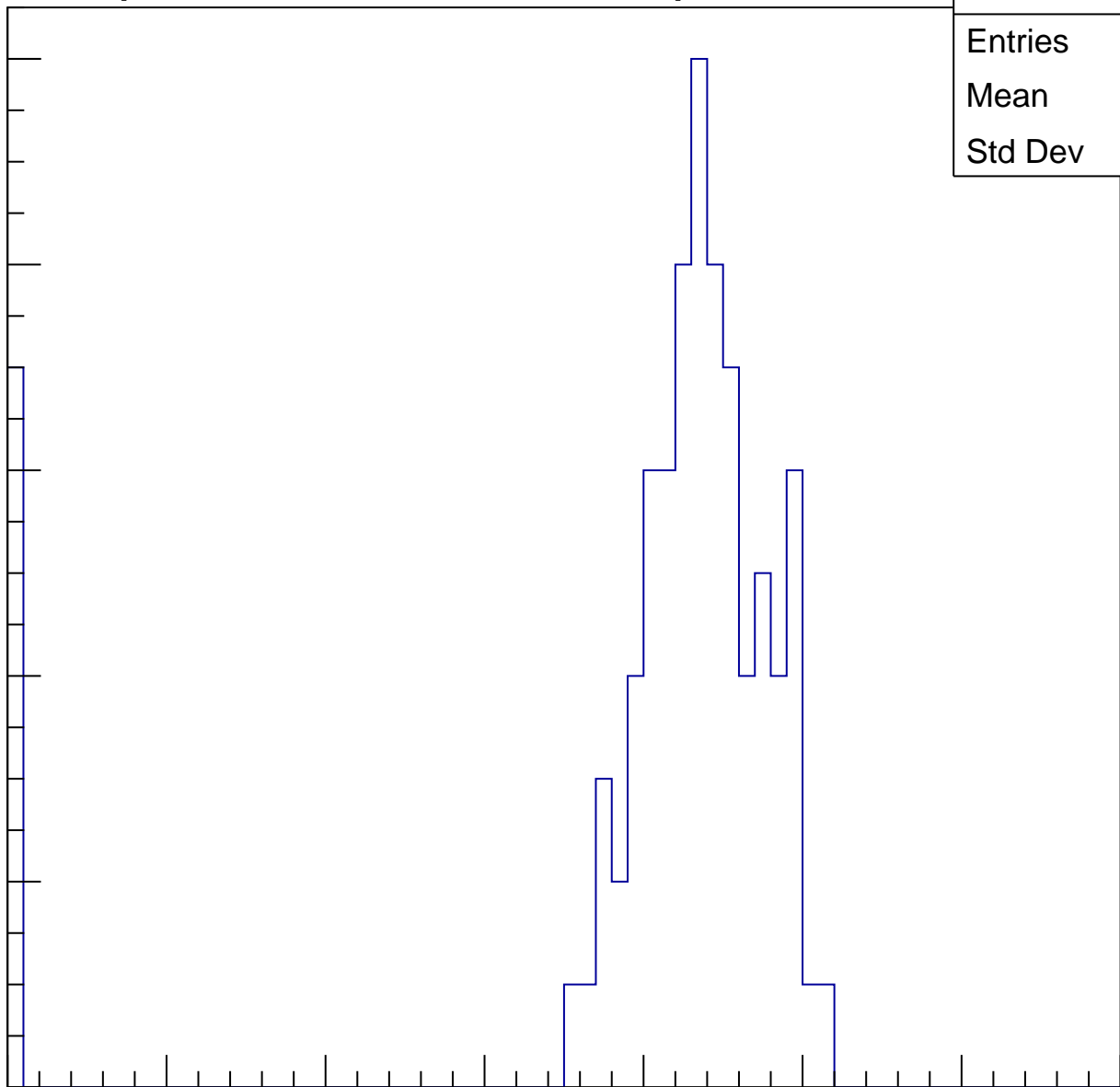
Entries	84
Mean	39.75
Std Dev	12.47

Entry

10
8
6
4
2
0

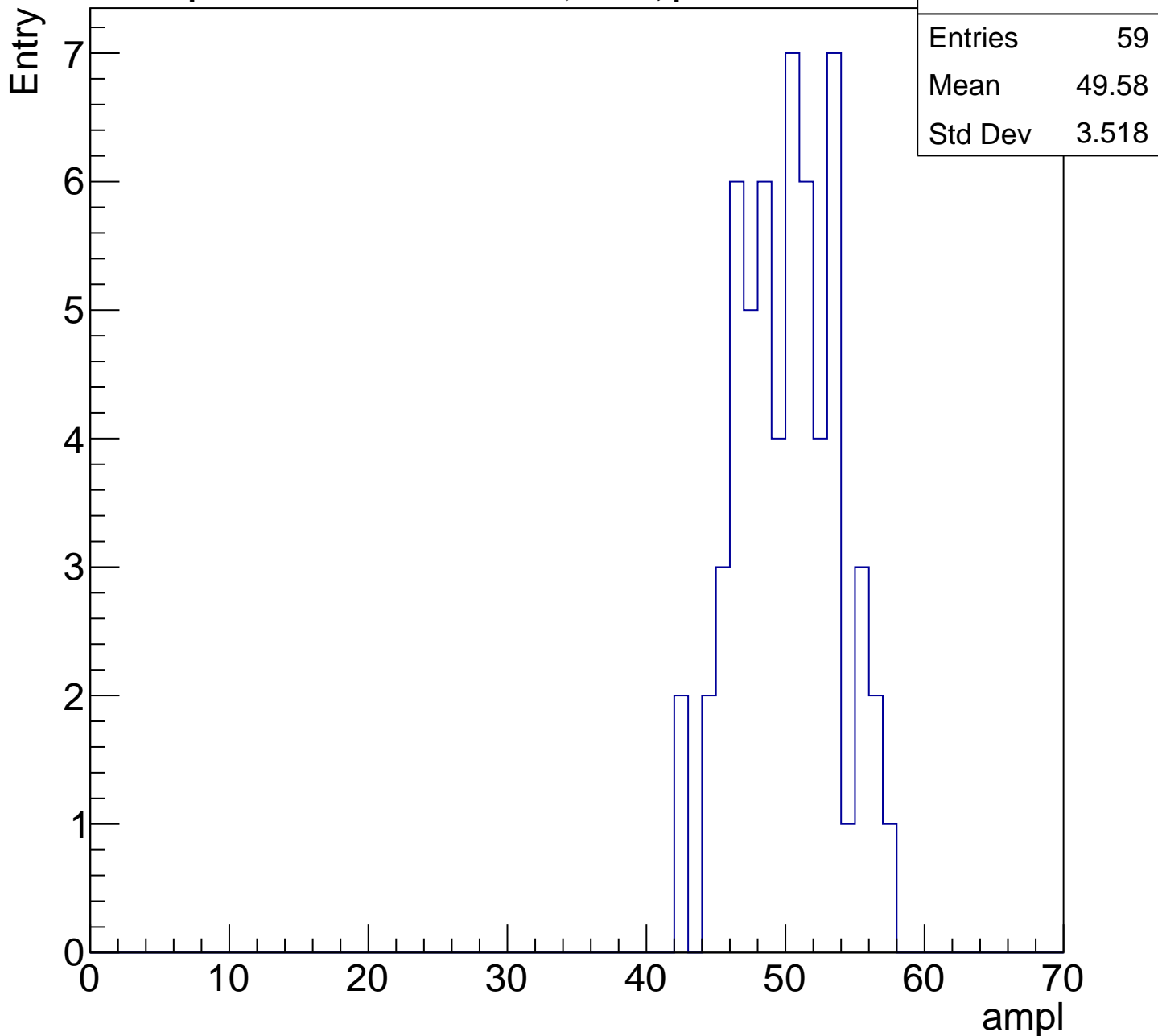
0 10 20 30 40 50 60 70

ampl



B1L103S, U9-ch47, adc3

calib_packv5_041523_1651.root, FC#0, port C2

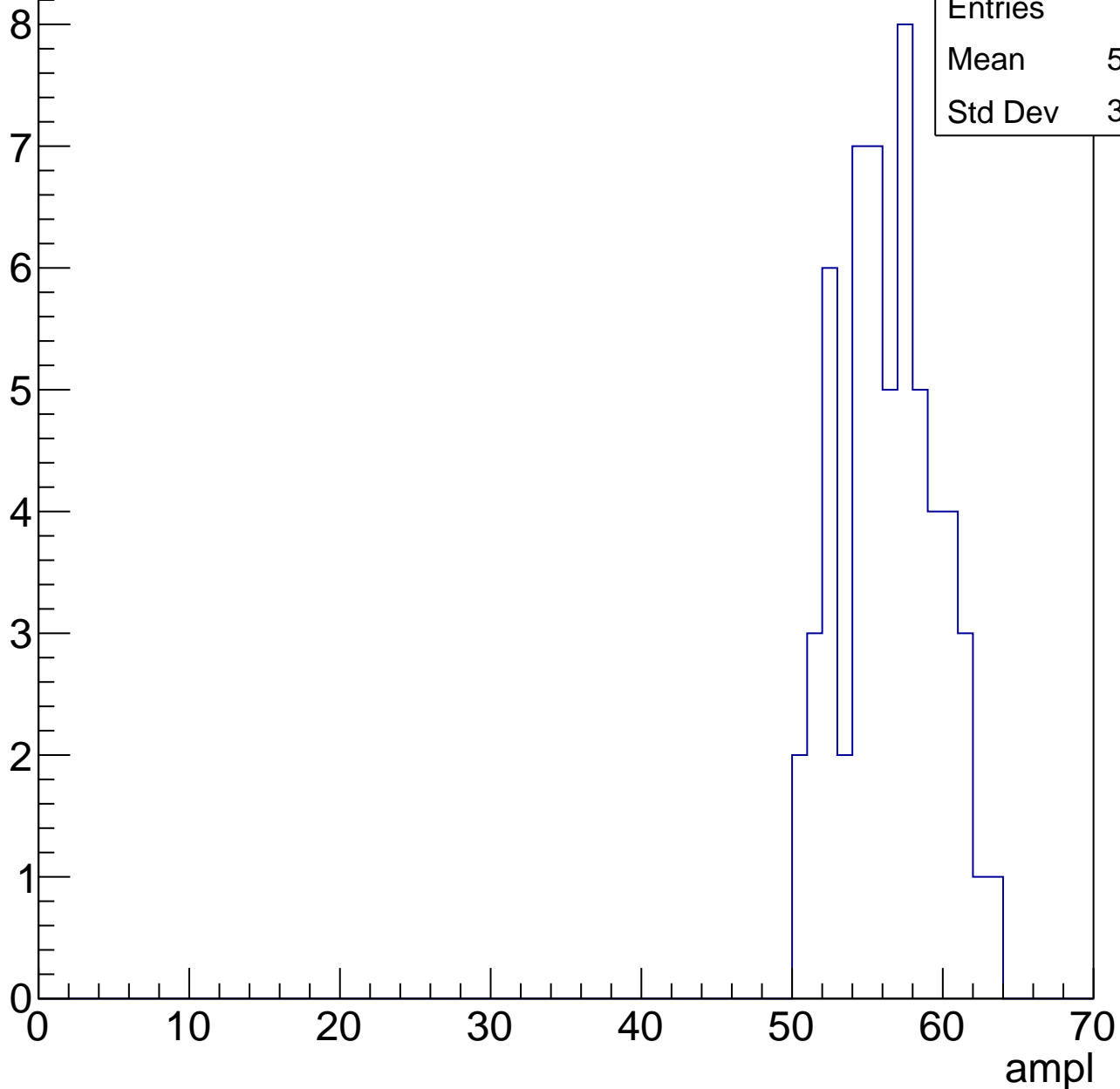


B1L103S, U9-ch47, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	55.93
Std Dev	3.172

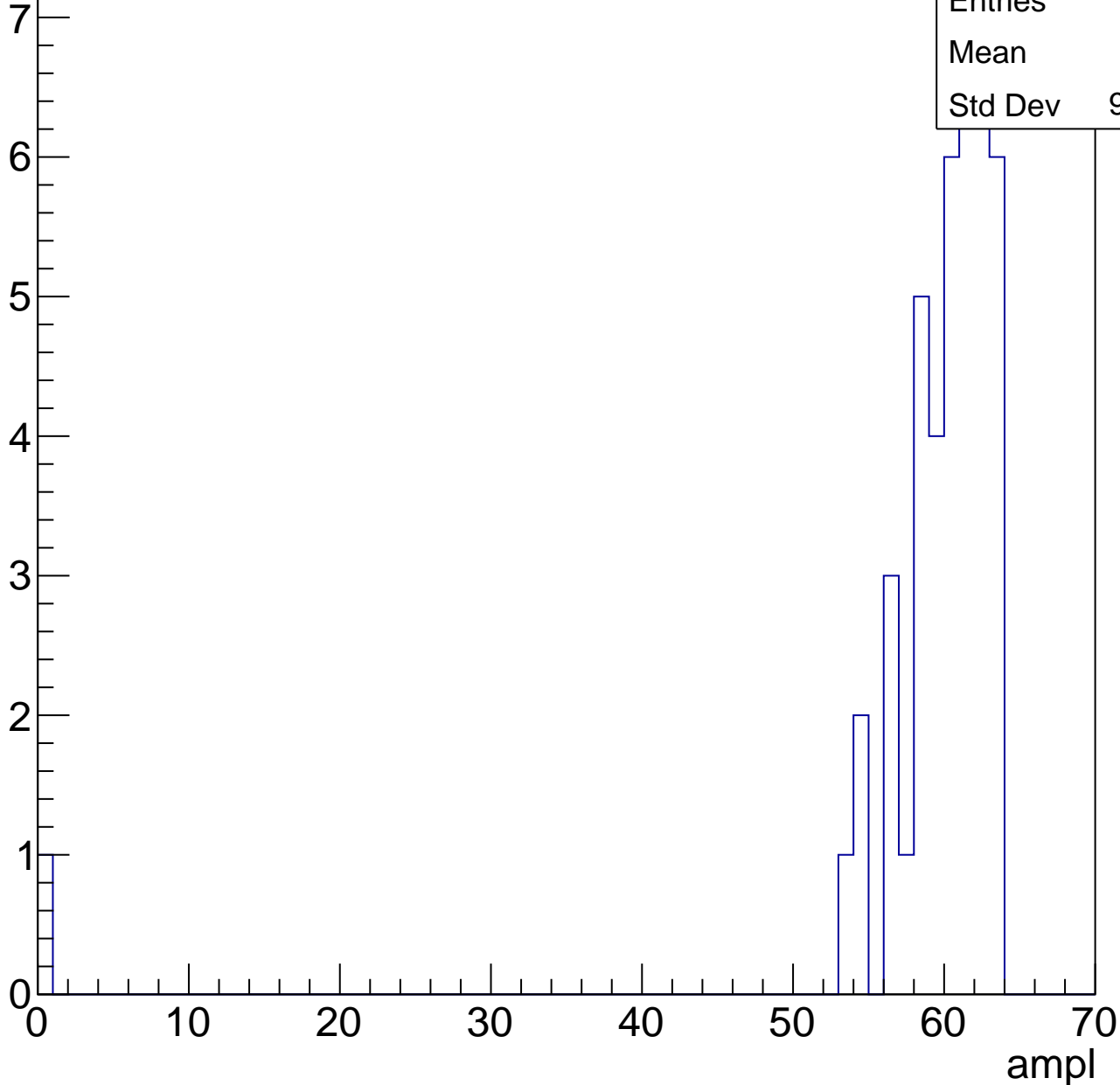


B1L103S, U9-ch47, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

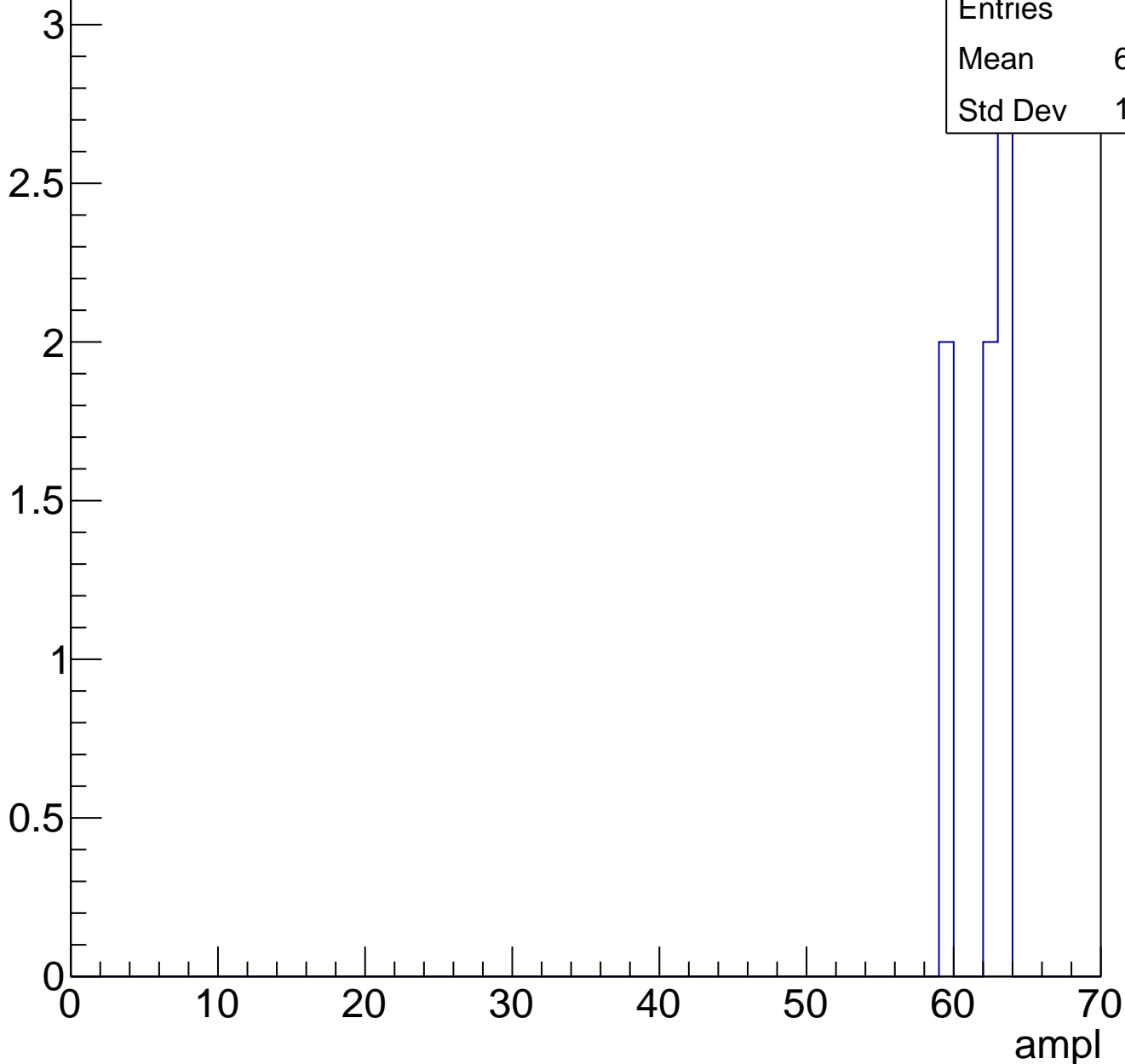
Entries	43
Mean	58.4
Std Dev	9.376



B1L103S, U9-ch47, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

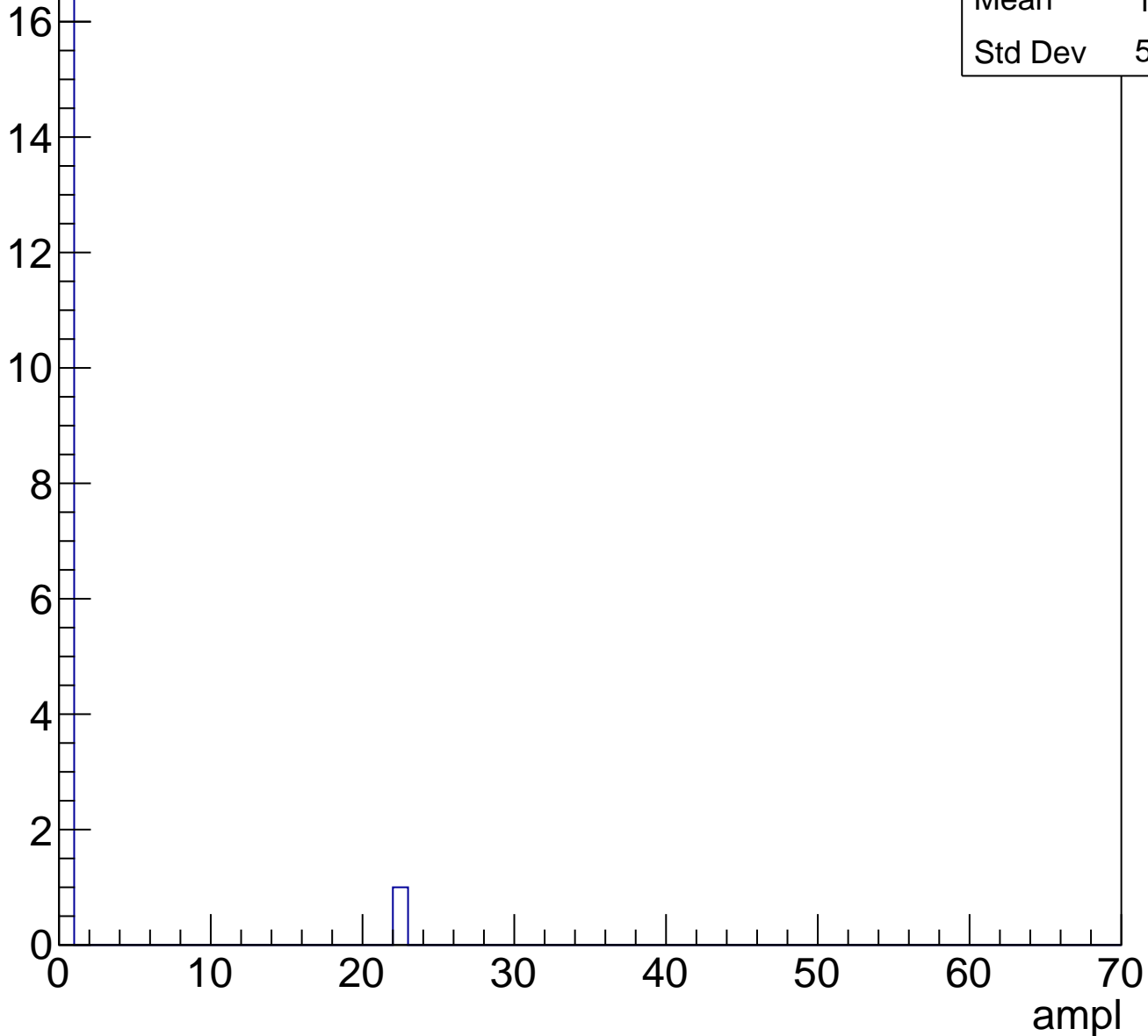


B1L103S, U9-ch47, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	18
Mean	1.222
Std Dev	5.039

Entry



B1L103S, U9-ch48, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	93
Mean	24.75
Std Dev	10.5

Entry

12

10

8

6

4

2

0

0

10

20

30

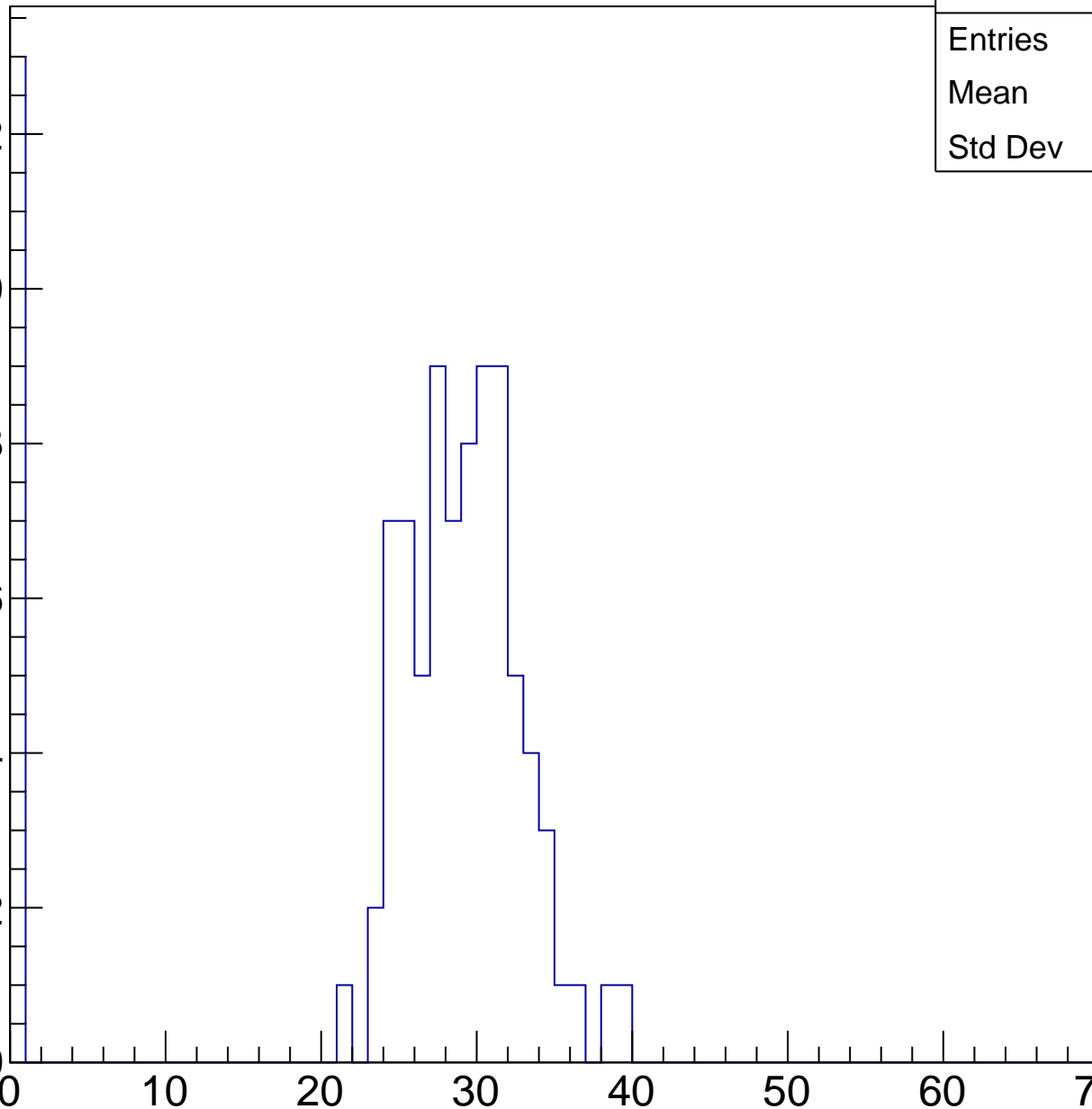
40

50

60

70

ampl

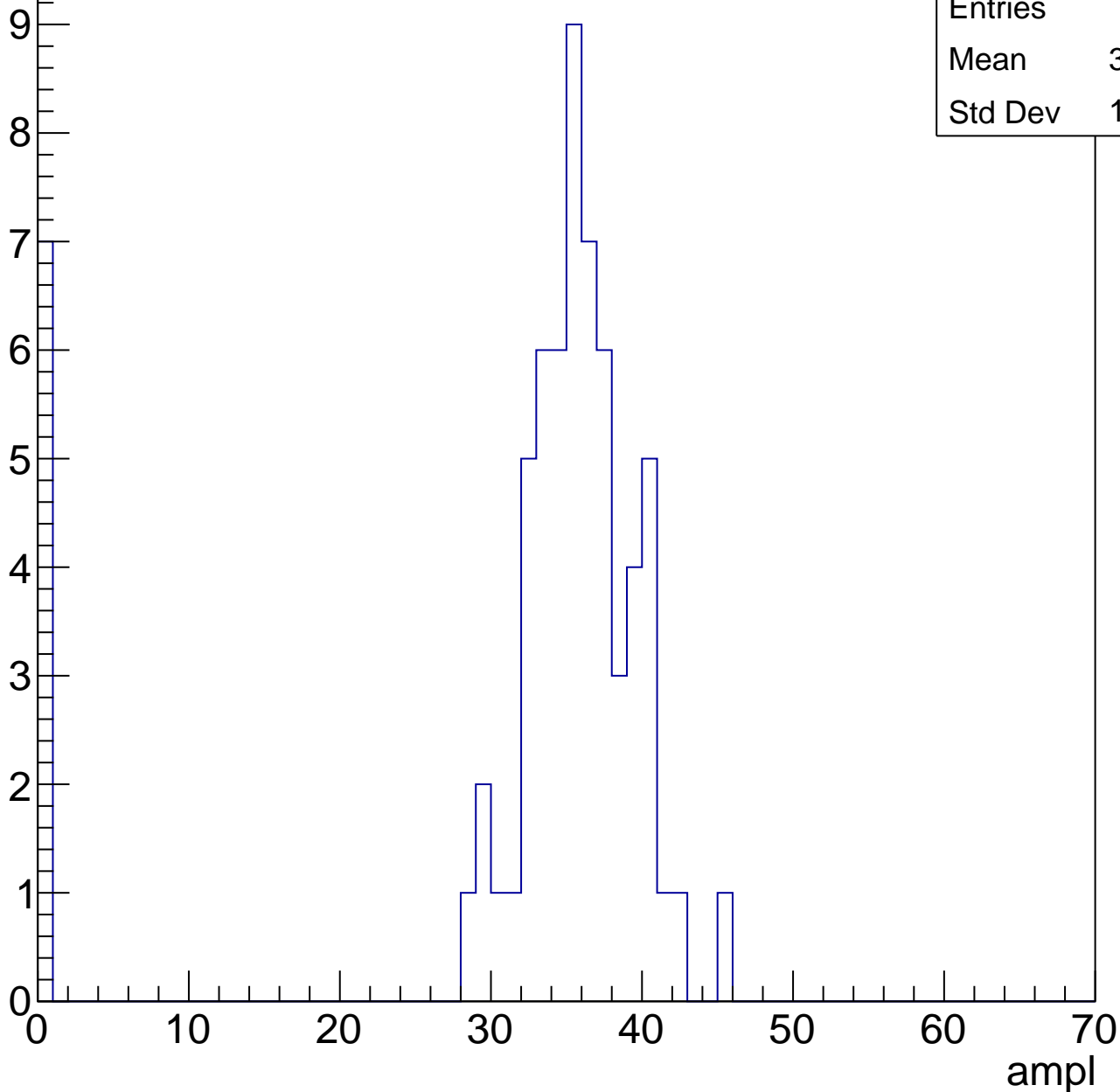


B1L103S, U9-ch48, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	31.76
Std Dev	11.38

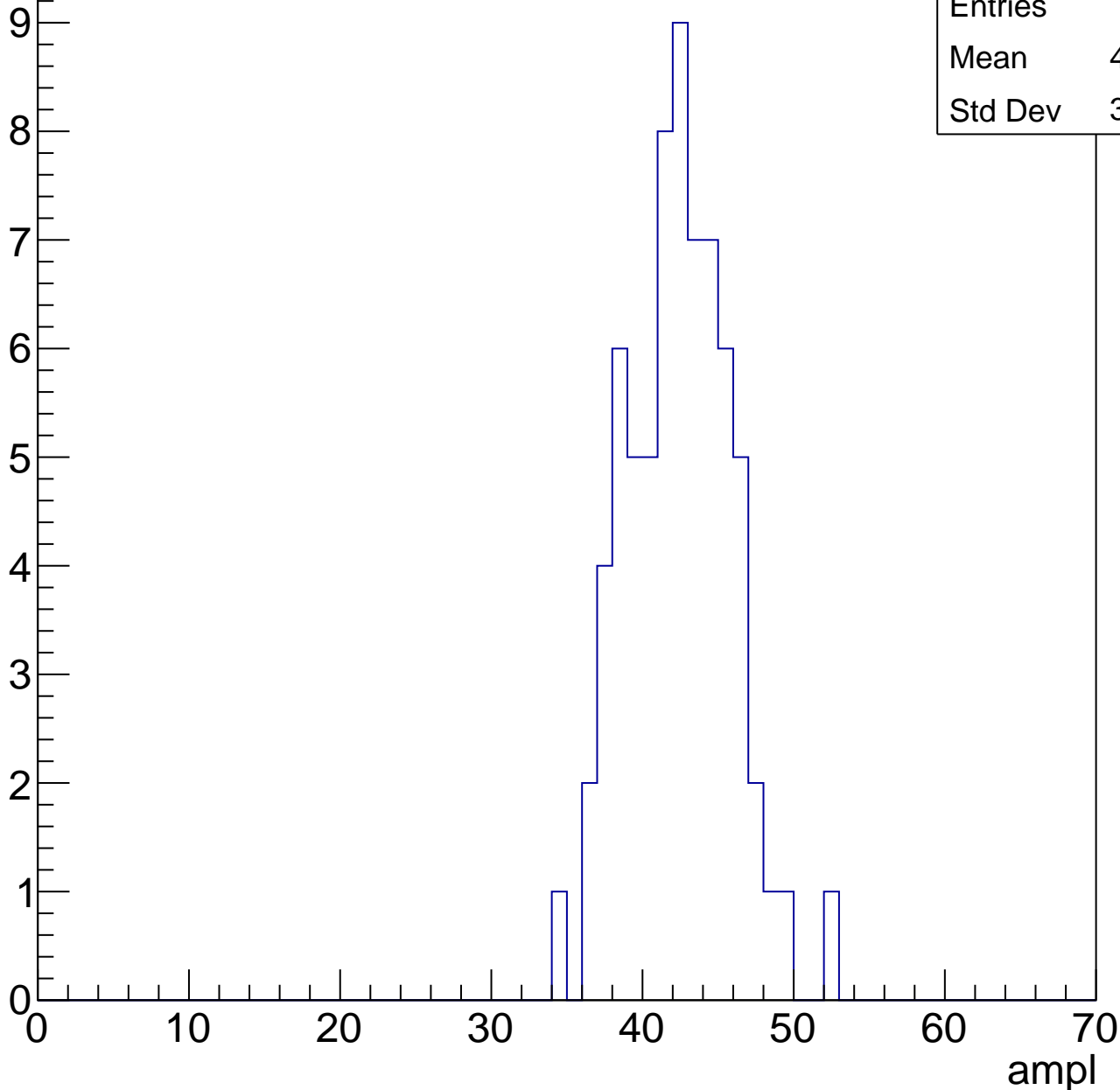


B1L103S, U9-ch48, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	41.93
Std Dev	3.399

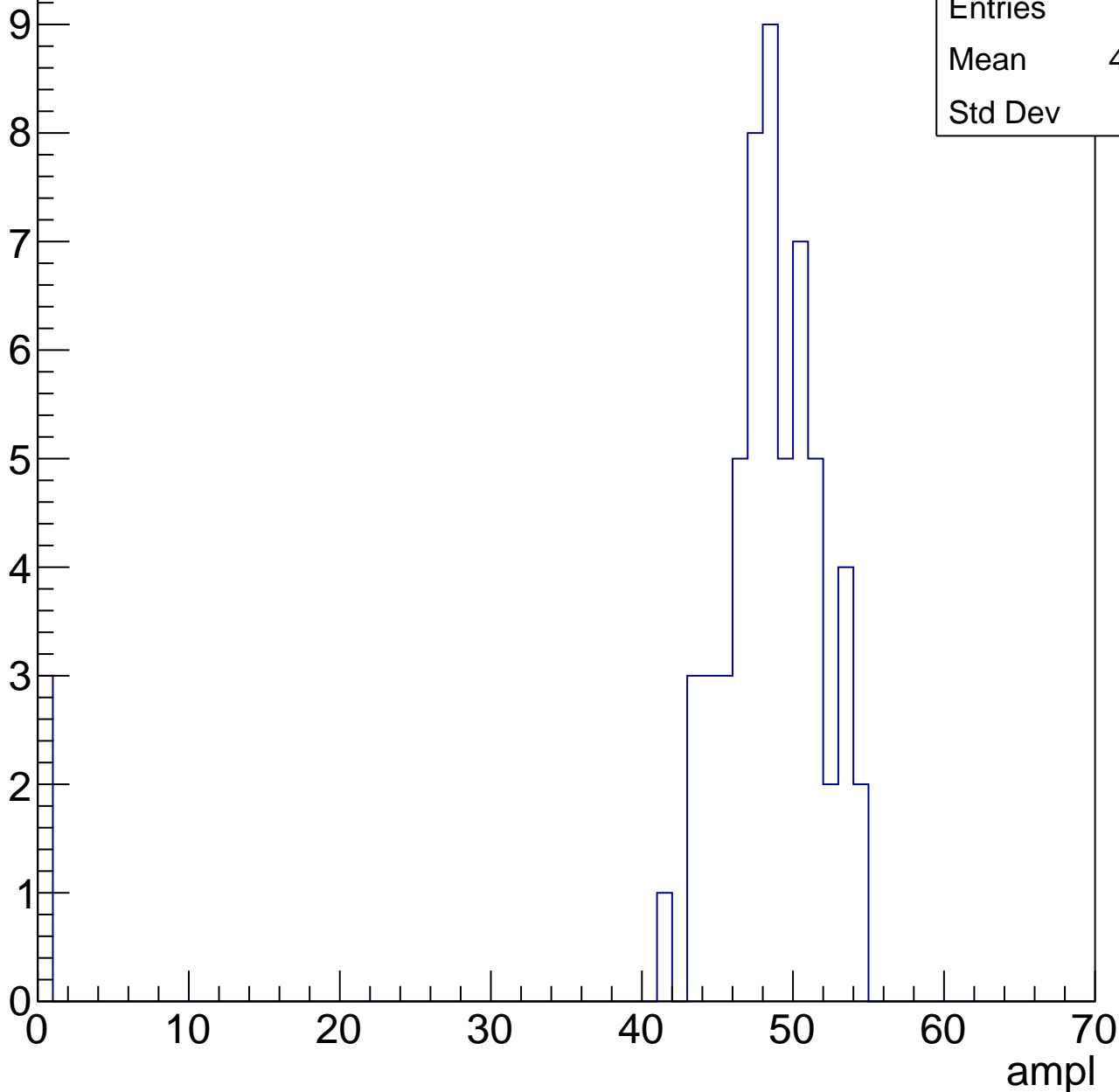


B1L103S, U9-ch48, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	45.82
Std Dev	10.9

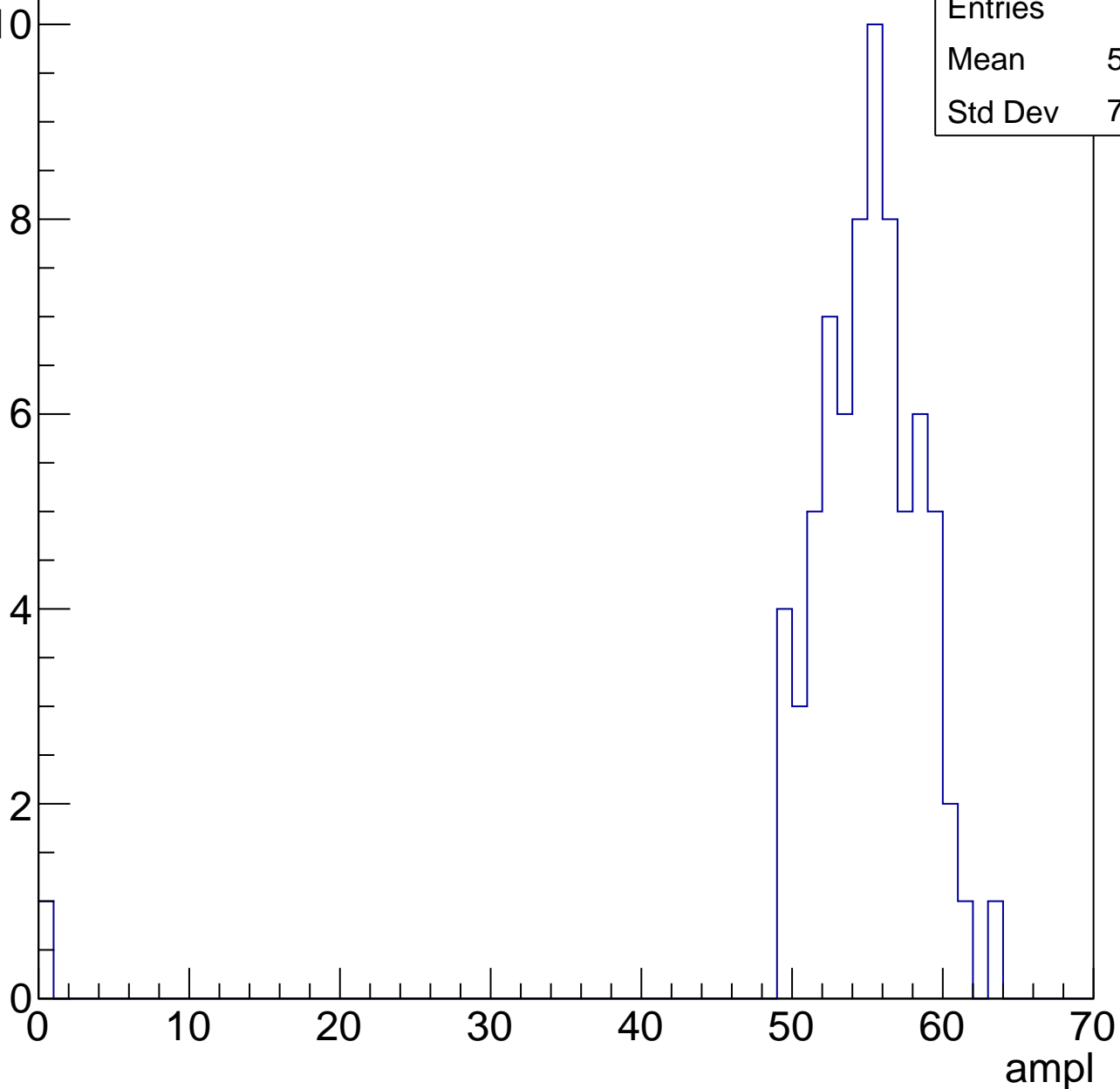


B1L103S, U9-ch48, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	53.96
Std Dev	7.123



B1L103S, U9-ch48, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

9
8
7
6
5
4
3
2
1
0

Entries	46
Mean	58.91
Std Dev	9.009

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

7

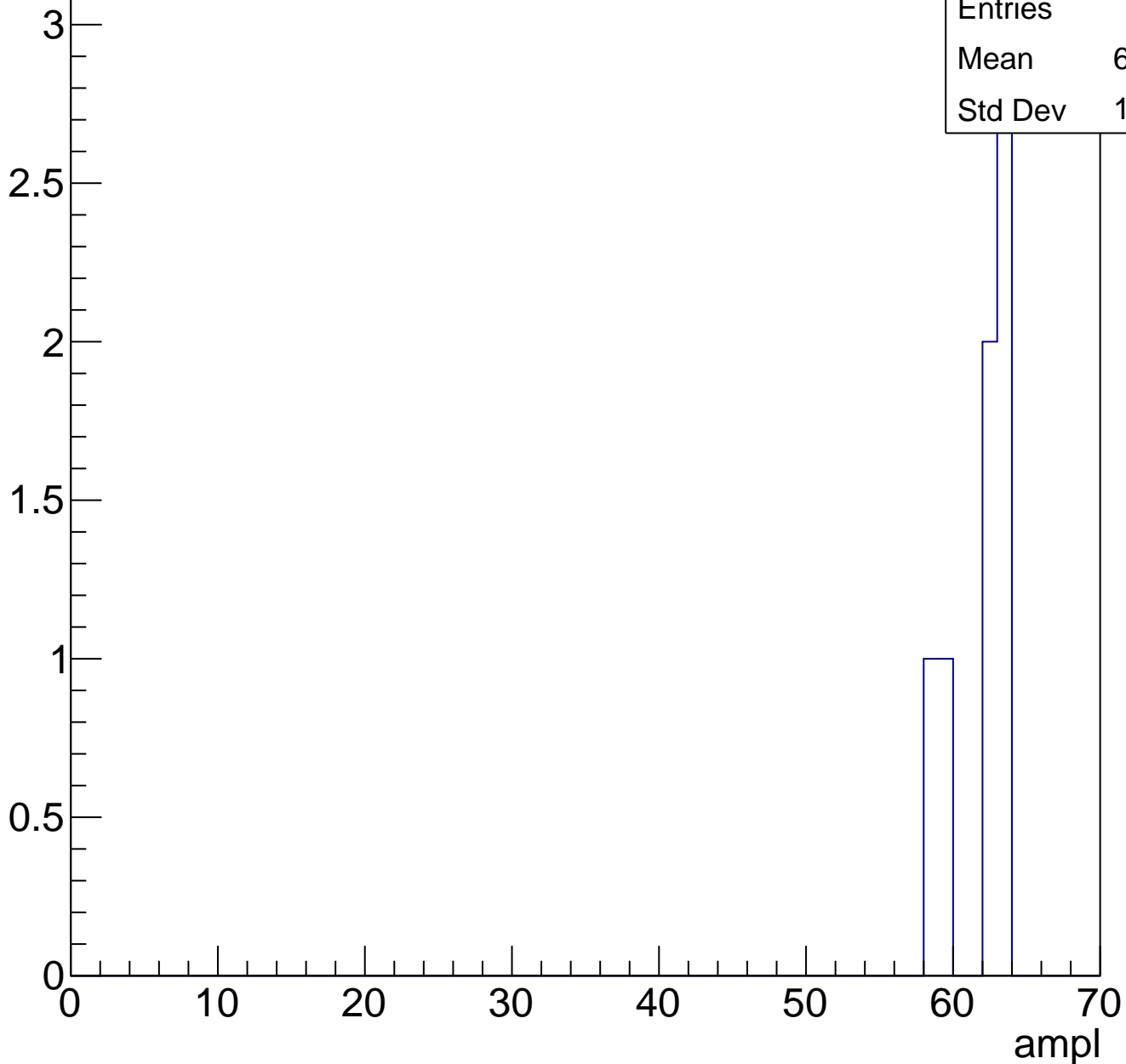
8

9

B1L103S, U9-ch48, adc6

calib_packv5_041523_1651.root, FC#0, port C2

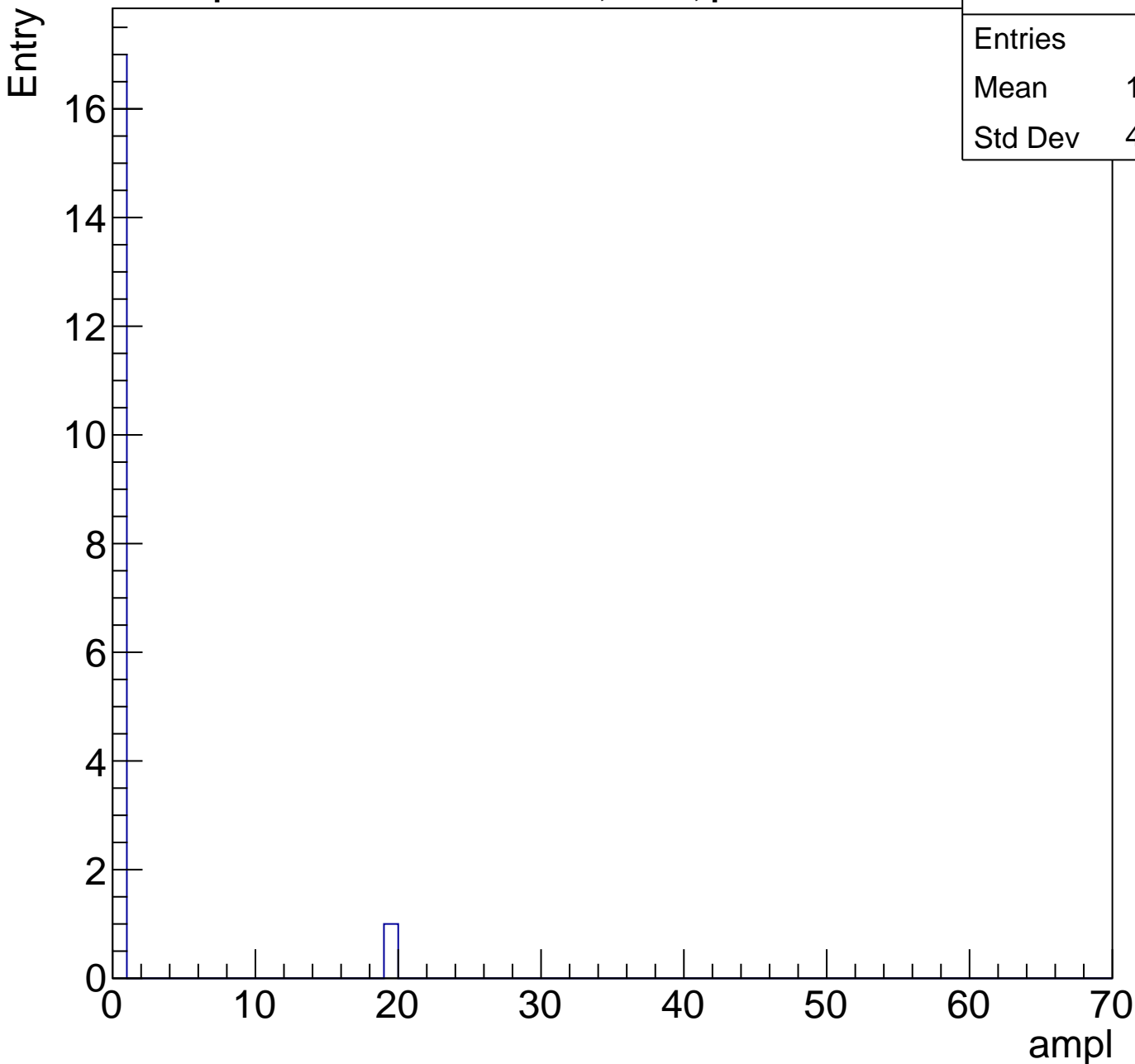
Entry



B1L103S, U9-ch48, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	18
Mean	1.056
Std Dev	4.352



B1L103S, U9-ch49, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	29.93
Std Dev	5.892

Entry

10

8

6

4

2

0

0

10

20

30

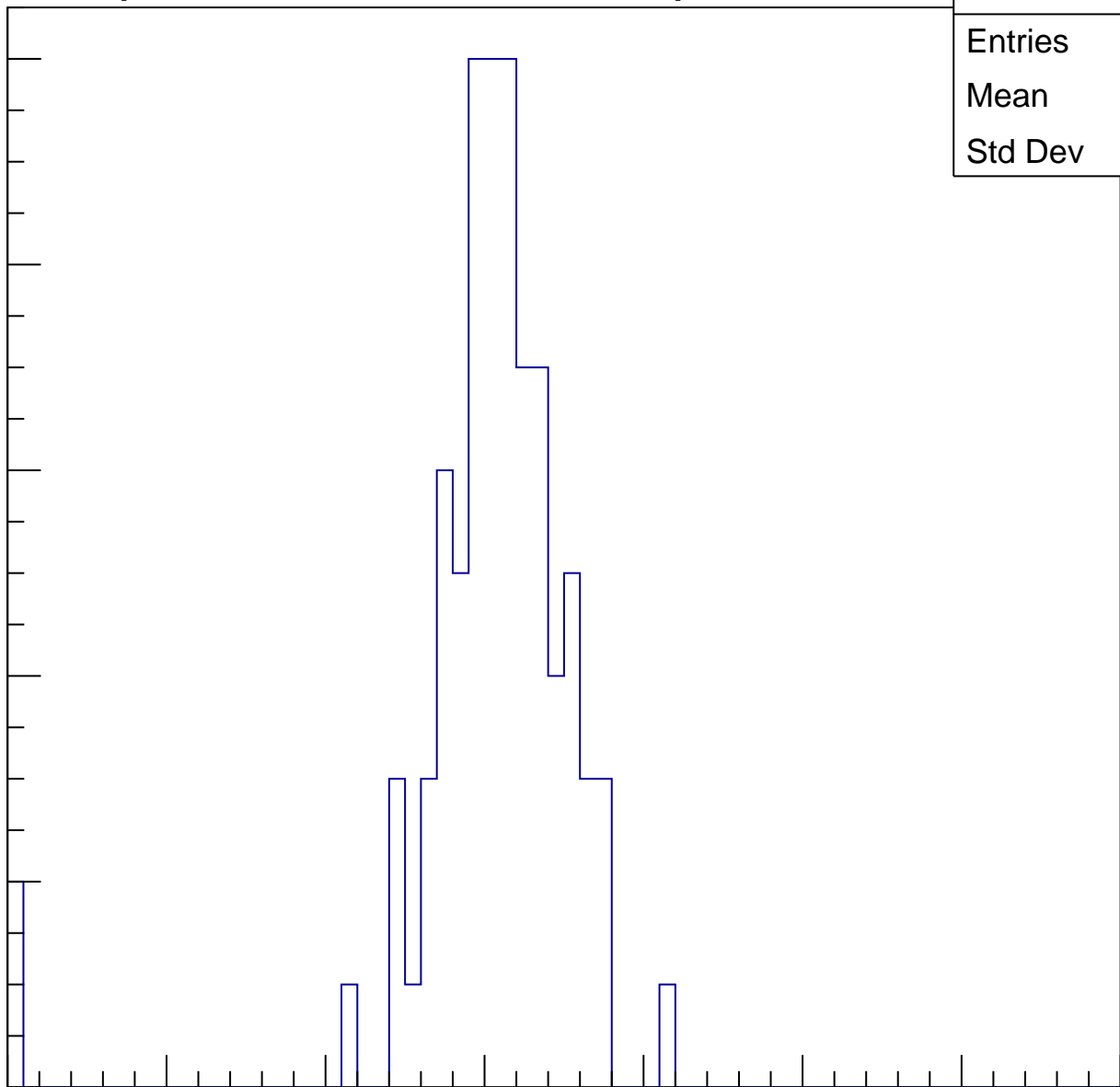
40

50

60

70

ampl

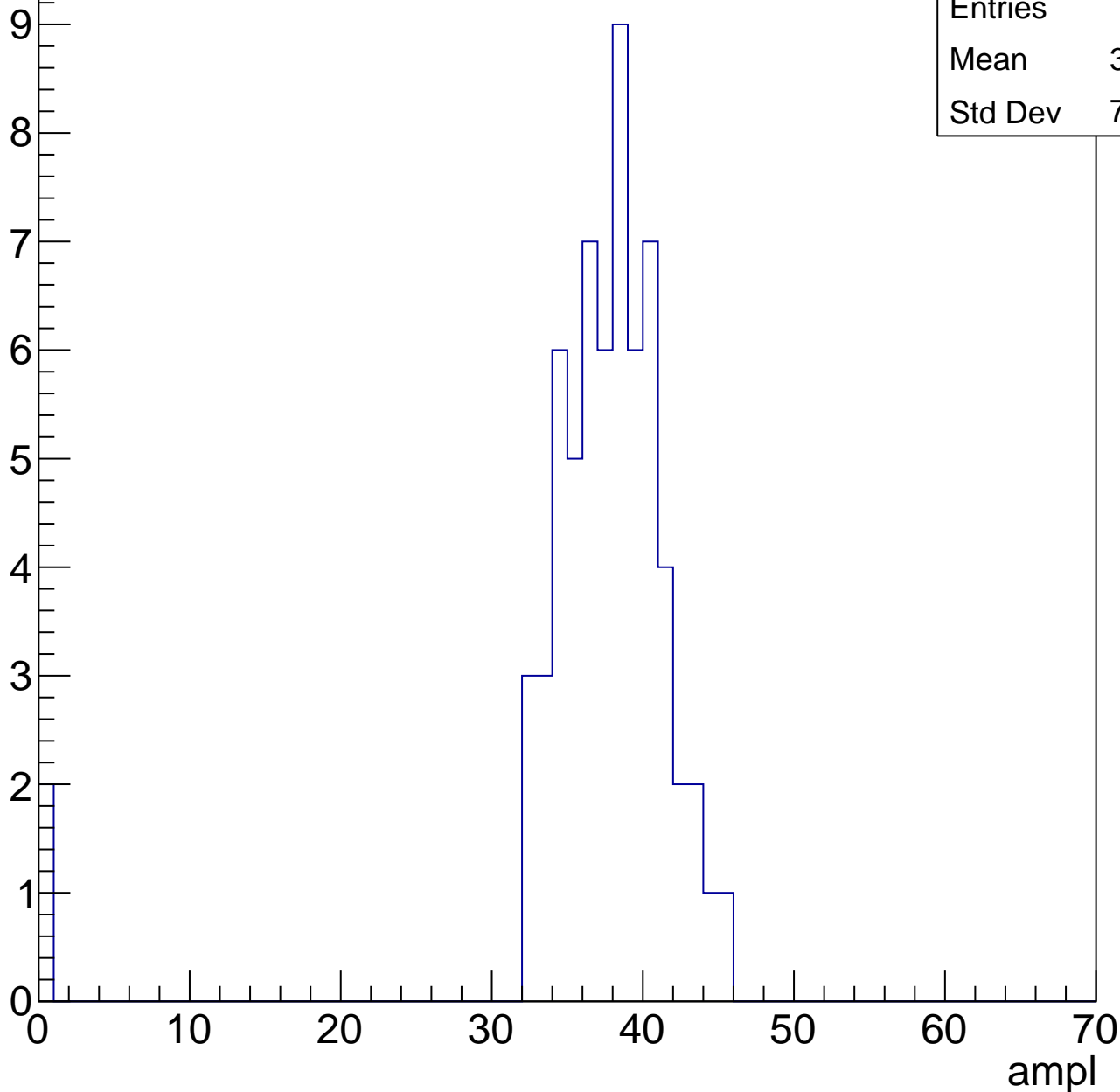


B1L103S, U9-ch49, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	36.36
Std Dev	7.192

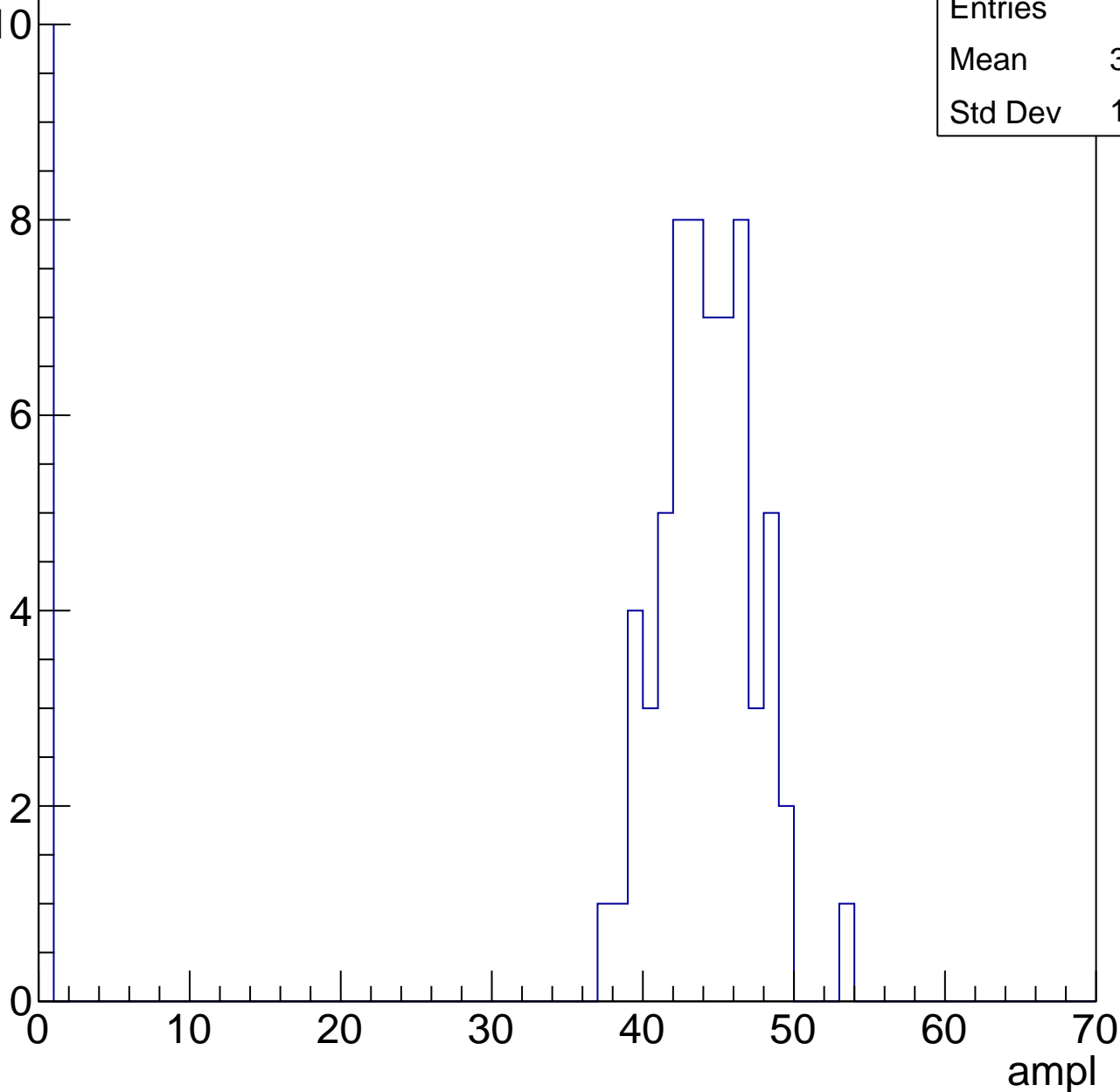


B1L103S, U9-ch49, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	37.79
Std Dev	15.32



B1L103S, U9-ch49, adc3

calib_packv5_041523_1651.root, FC#0, port C2

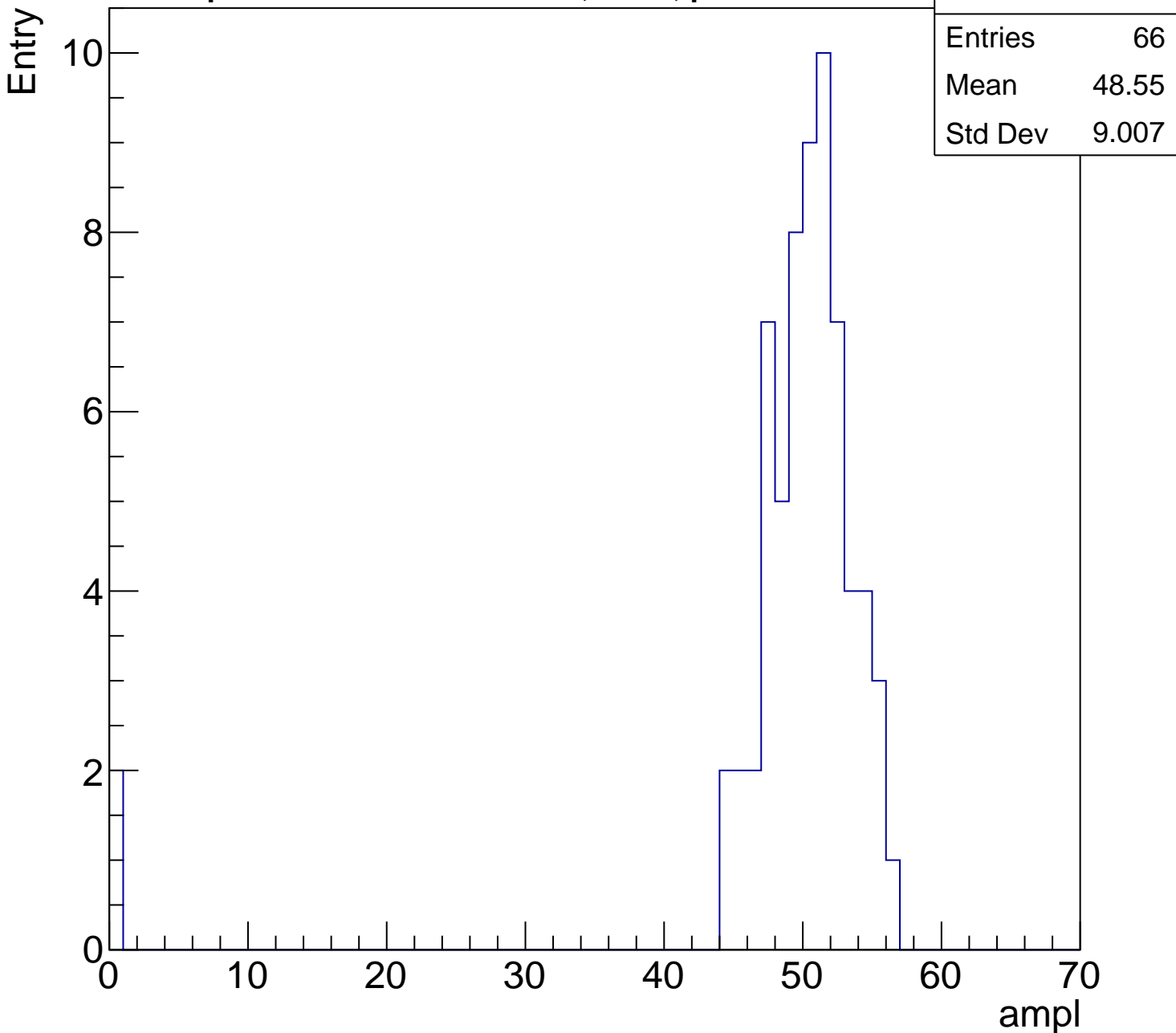
Entries	66
Mean	48.55
Std Dev	9.007

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

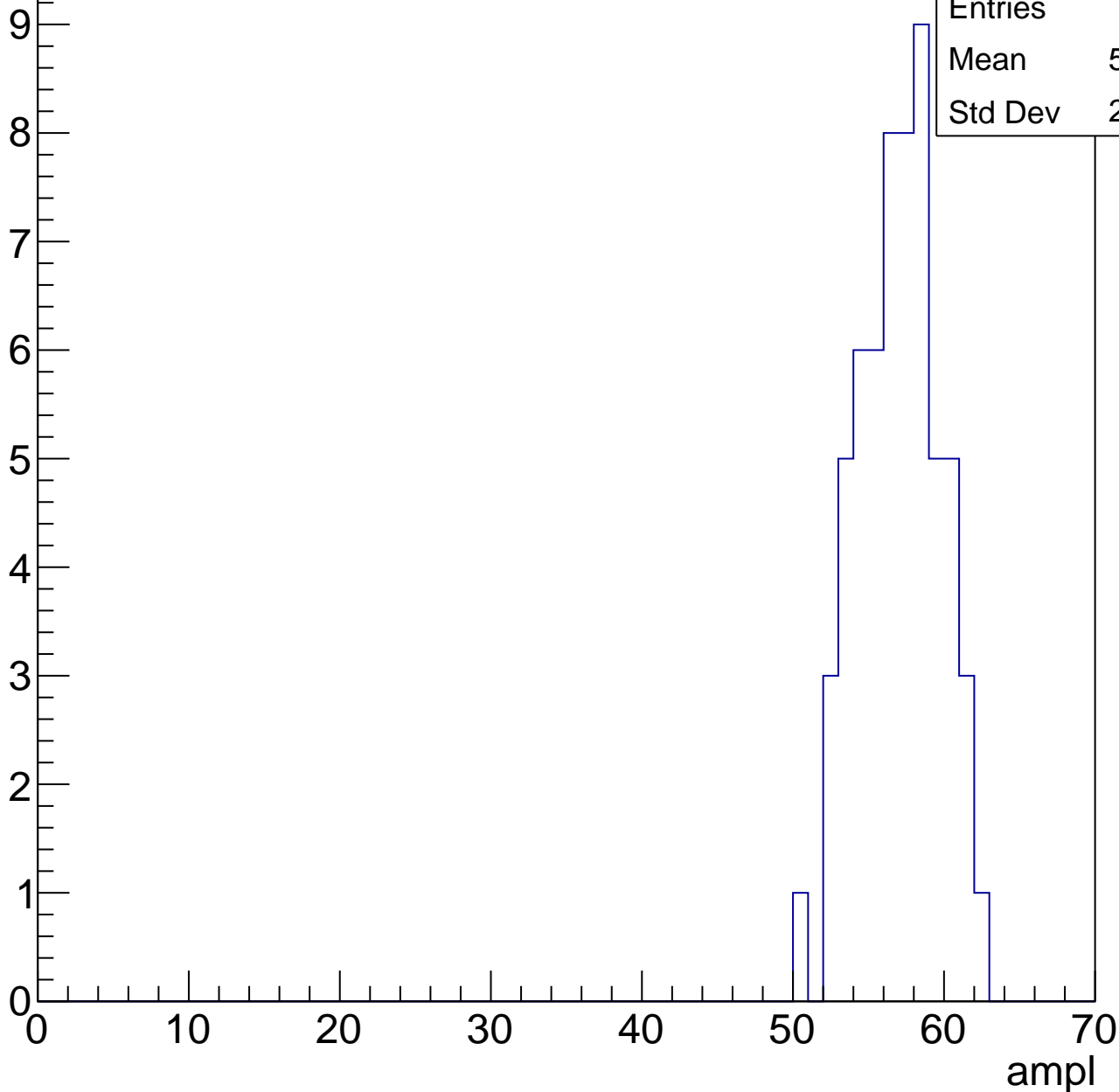


B1L103S, U9-ch49, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	56.52
Std Dev	2.655

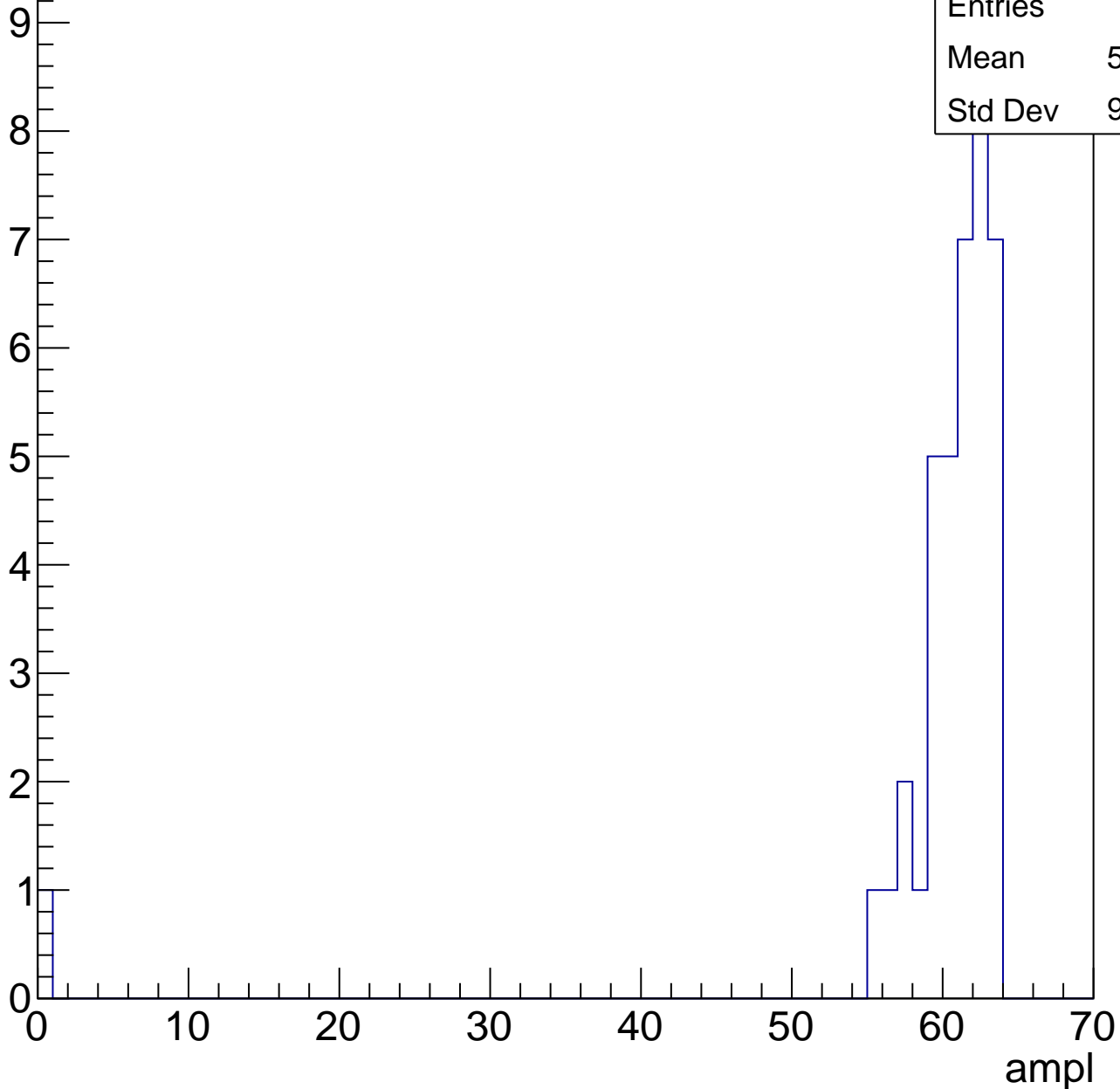


B1L103S, U9-ch49, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	59.08
Std Dev	9.794



B1L103S, U9-ch49, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch49, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

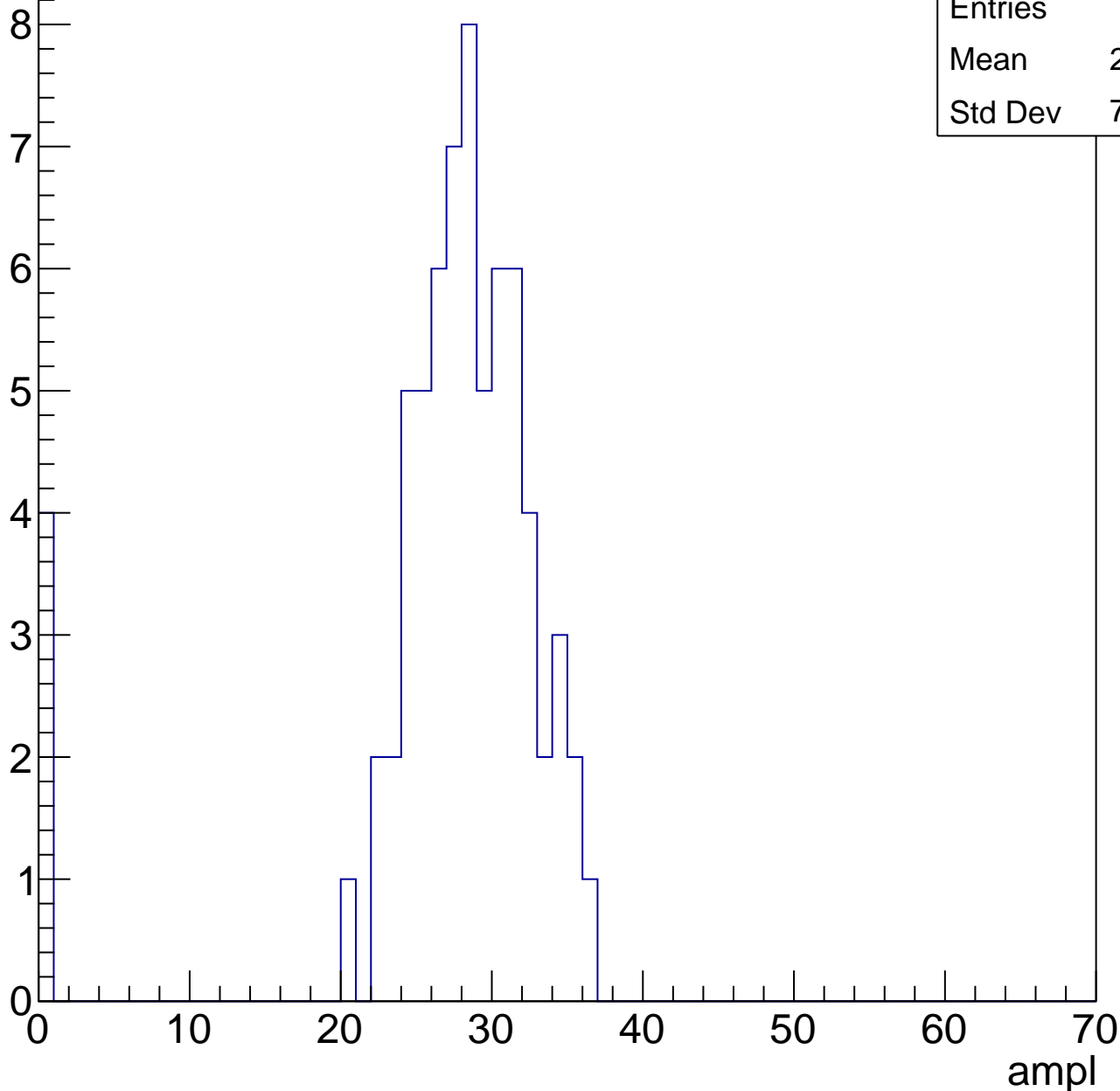
ampl

B1L103S, U9-ch50, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	26.62
Std Dev	7.435

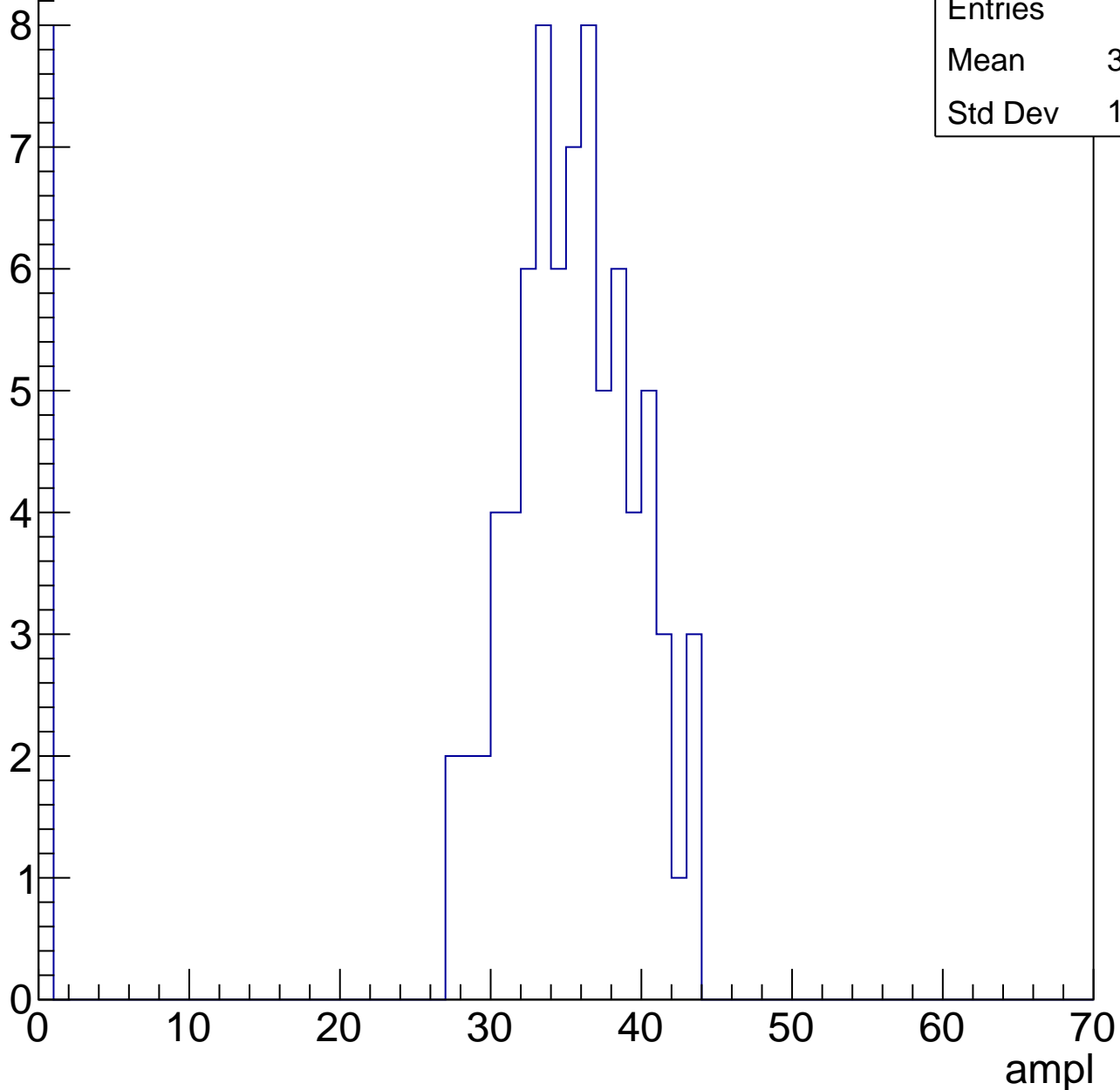


B1L103S, U9-ch50, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	84
Mean	31.76
Std Dev	10.96

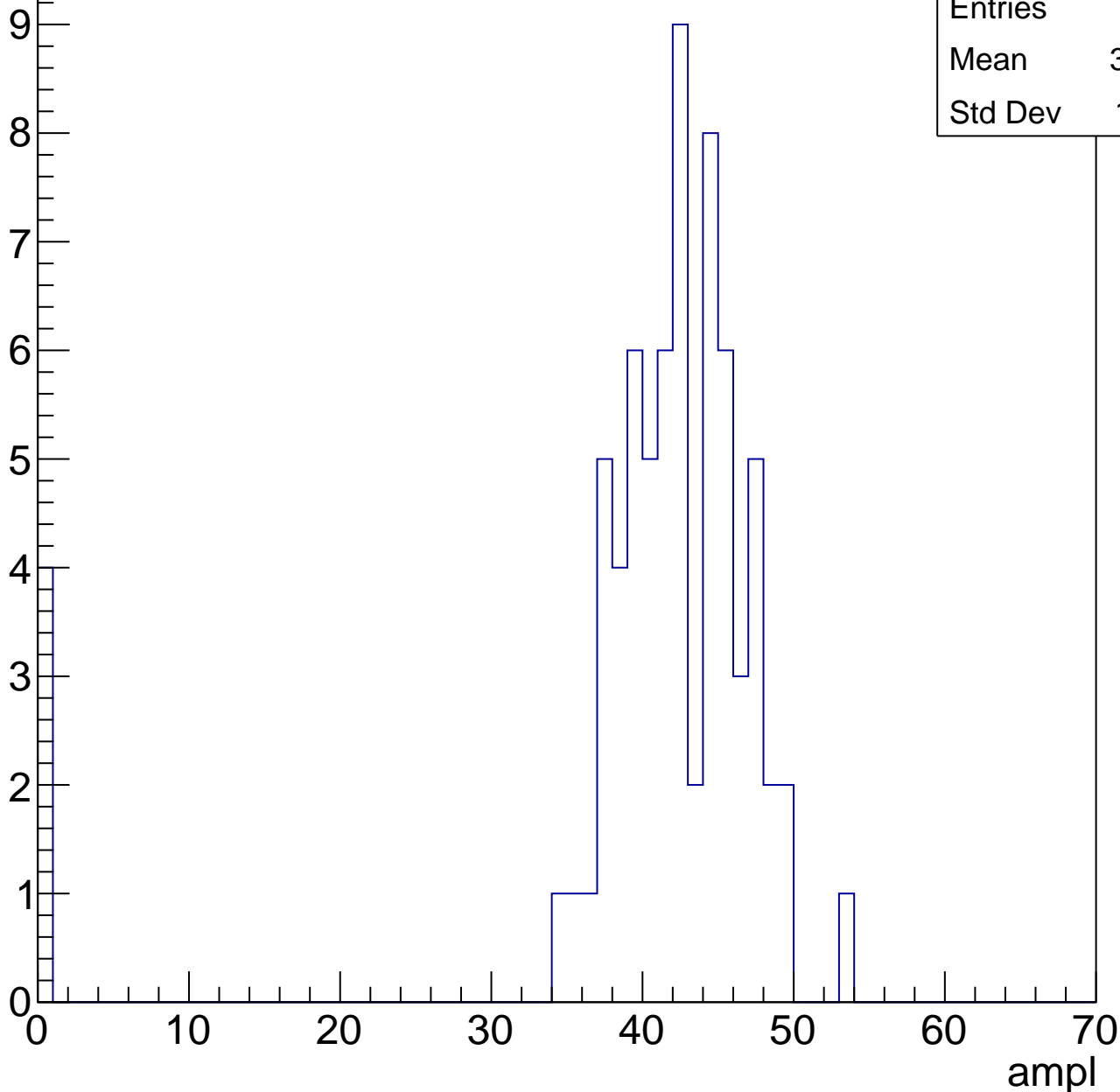


B1L103S, U9-ch50, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	39.83
Std Dev	10.41

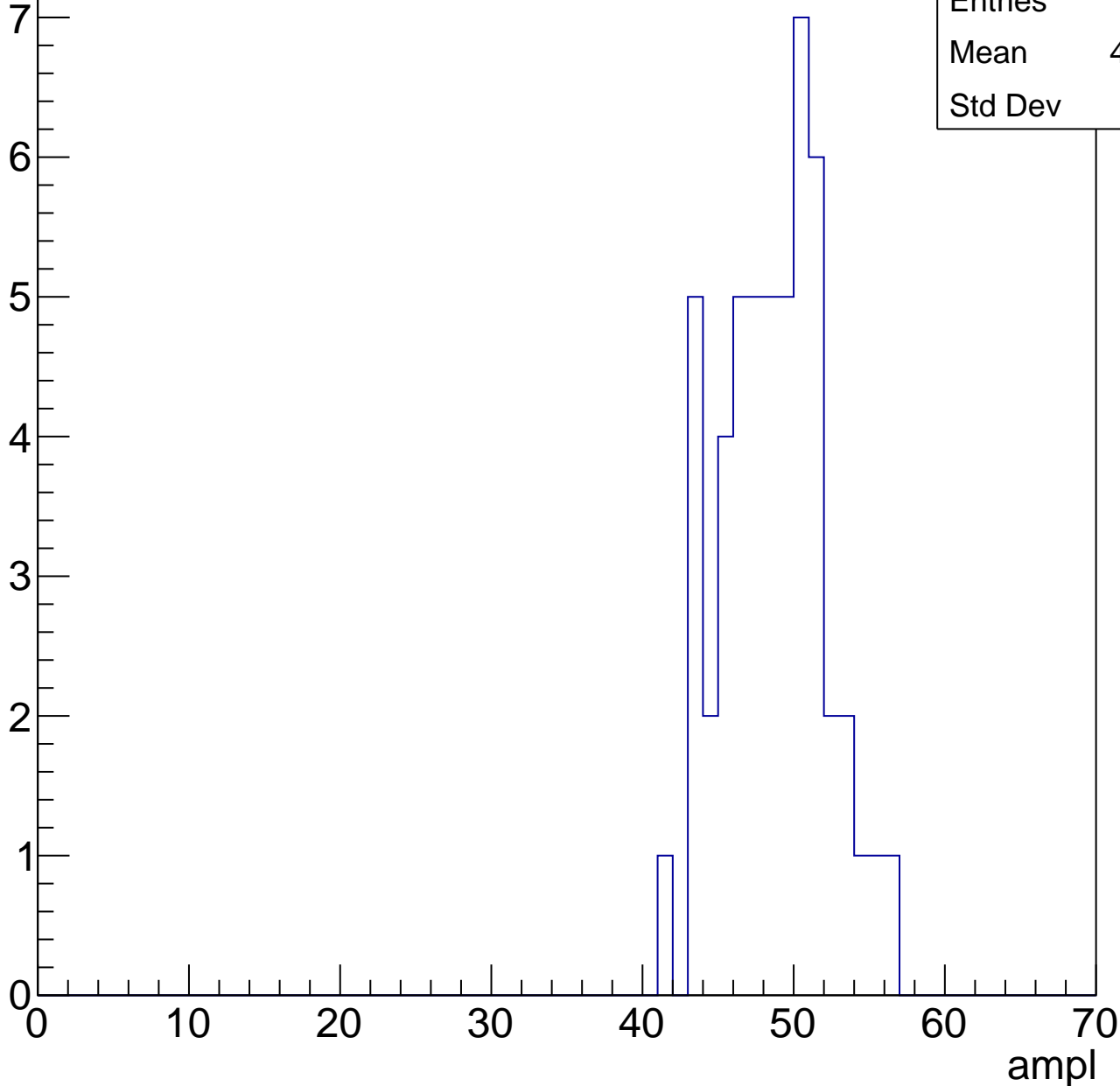


B1L103S, U9-ch50, adc3

calib_packv5_041523_1651.root, FC#0, port C2

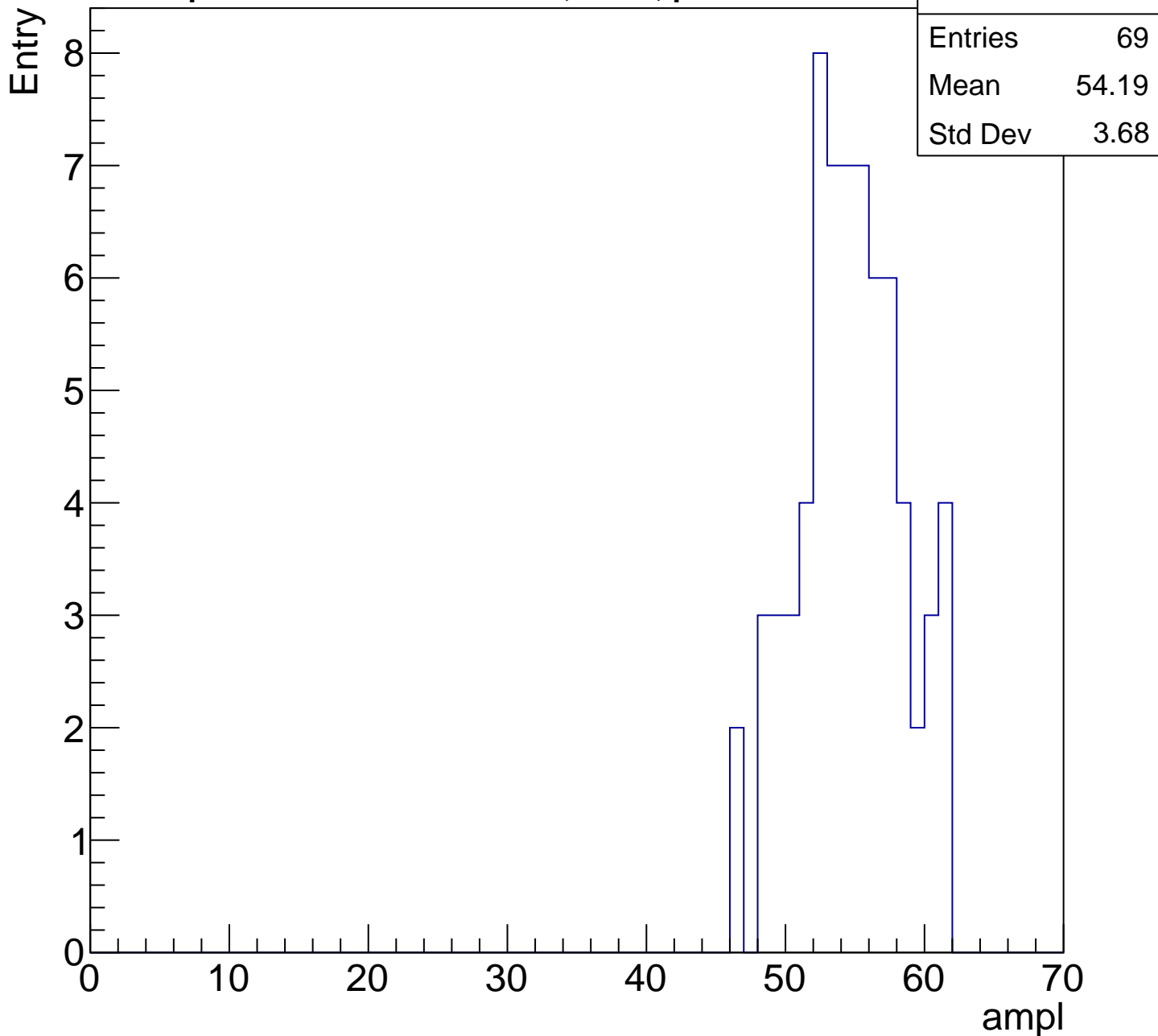
Entry

Entries	52
Mean	48.17
Std Dev	3.35



B1L103S, U9-ch50, adc4

calib_packv5_041523_1651.root, FC#0, port C2

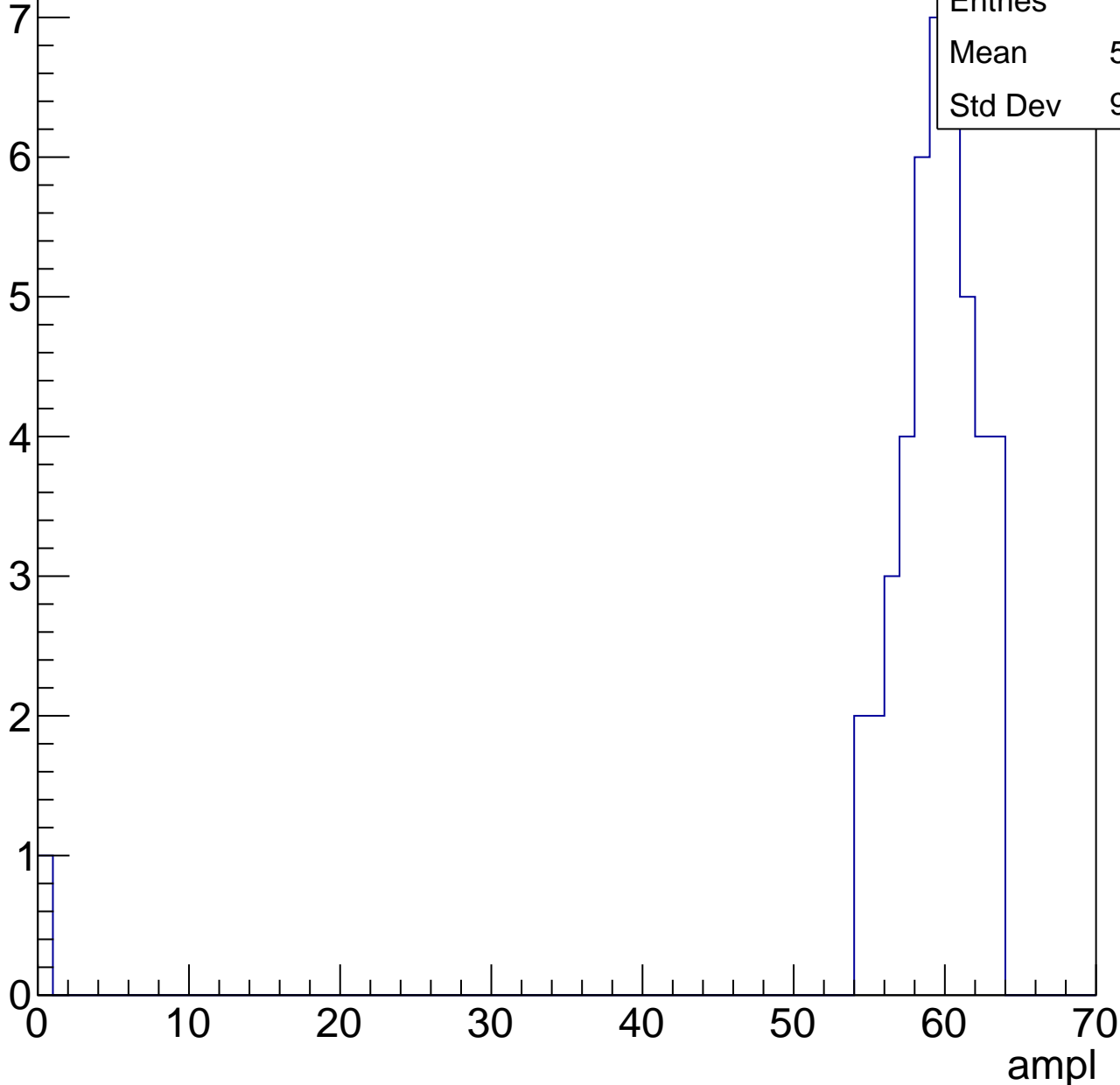


B1L103S, U9-ch50, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	45
Mean	57.78
Std Dev	9.033

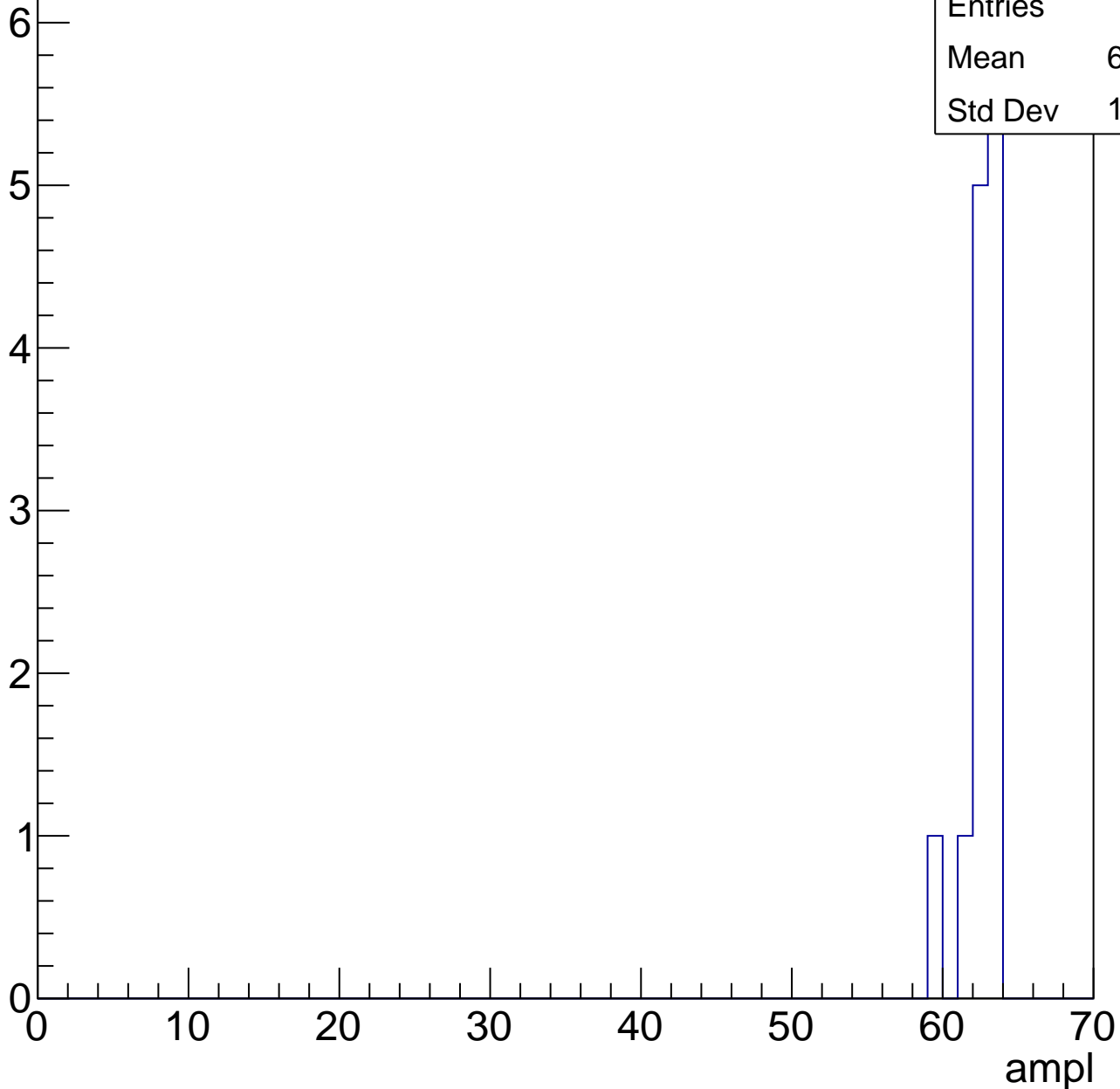


B1L103S, U9-ch50, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	13
Mean	62.15
Std Dev	1.099



B1L103S, U9-ch50, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	3.263
Std Dev	13.84

Entry



B1L103S, U9-ch51, adc0

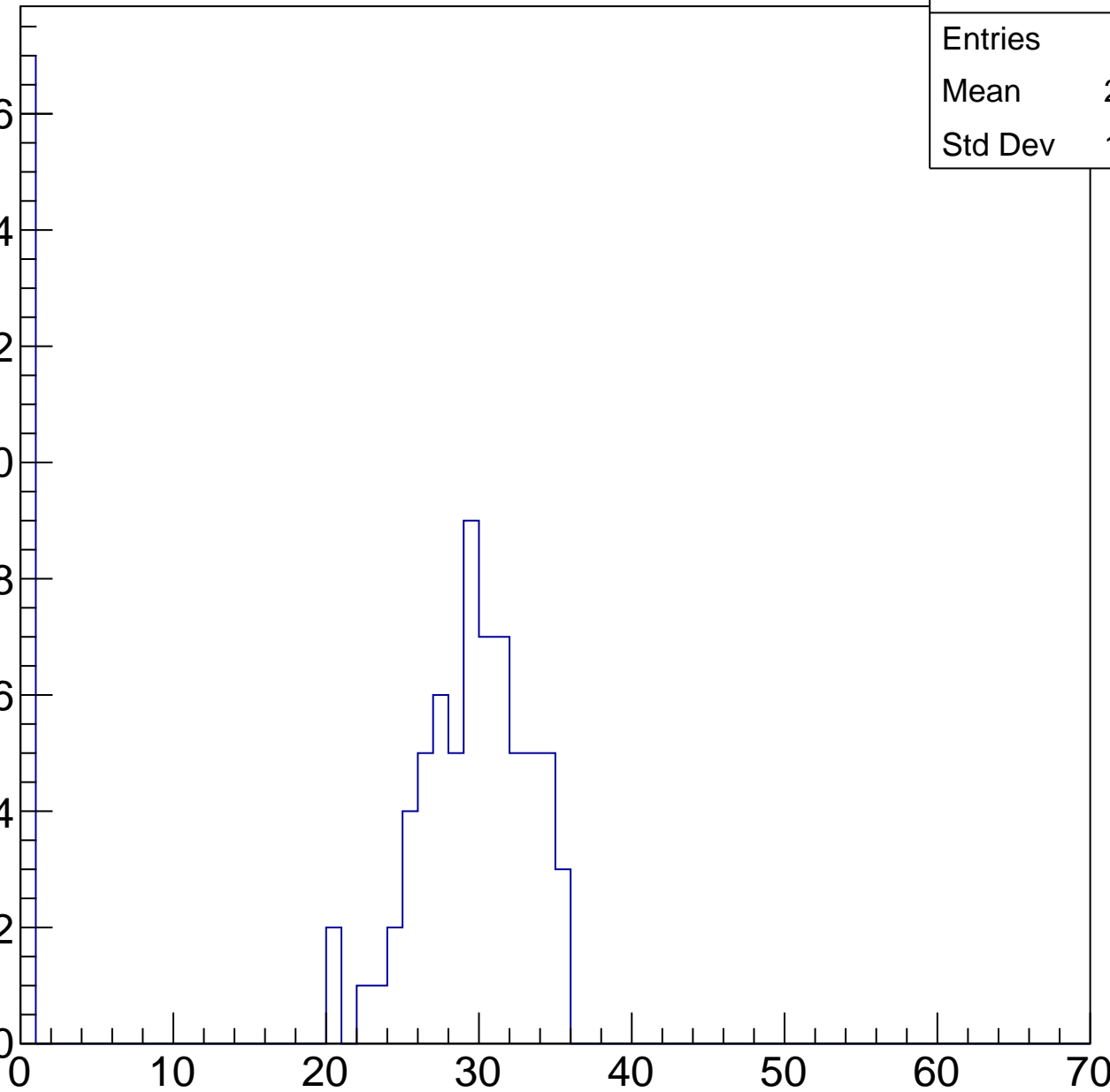
calib_packv5_041523_1651.root, FC#0, port C2

Entries	84
Mean	23.25
Std Dev	12.12

Entry

16
14
12
10
8
6
4
2
0

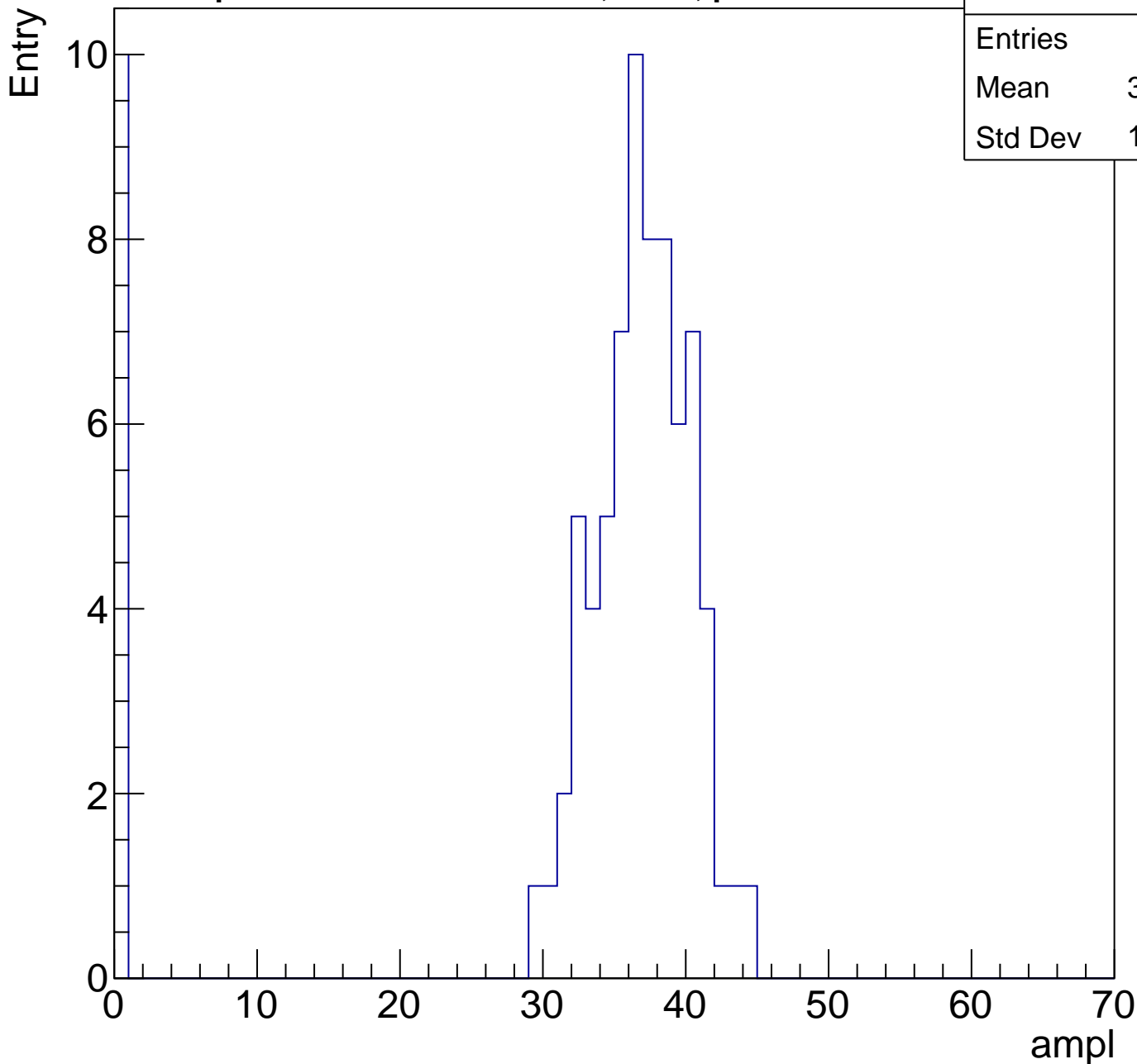
ampl



B1L103S, U9-ch51, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	32.04
Std Dev	12.38

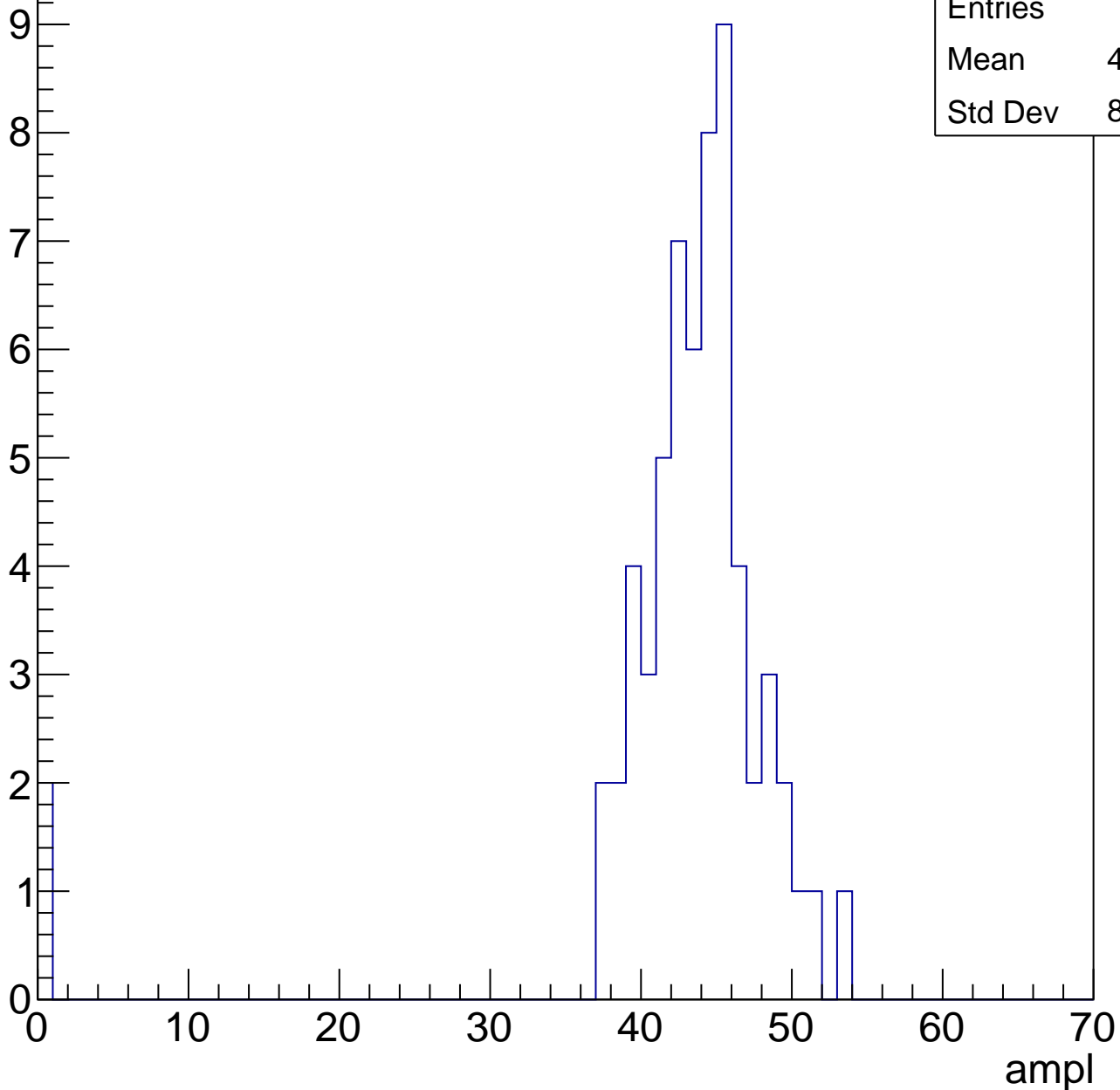


B1L103S, U9-ch51, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	42.16
Std Dev	8.392

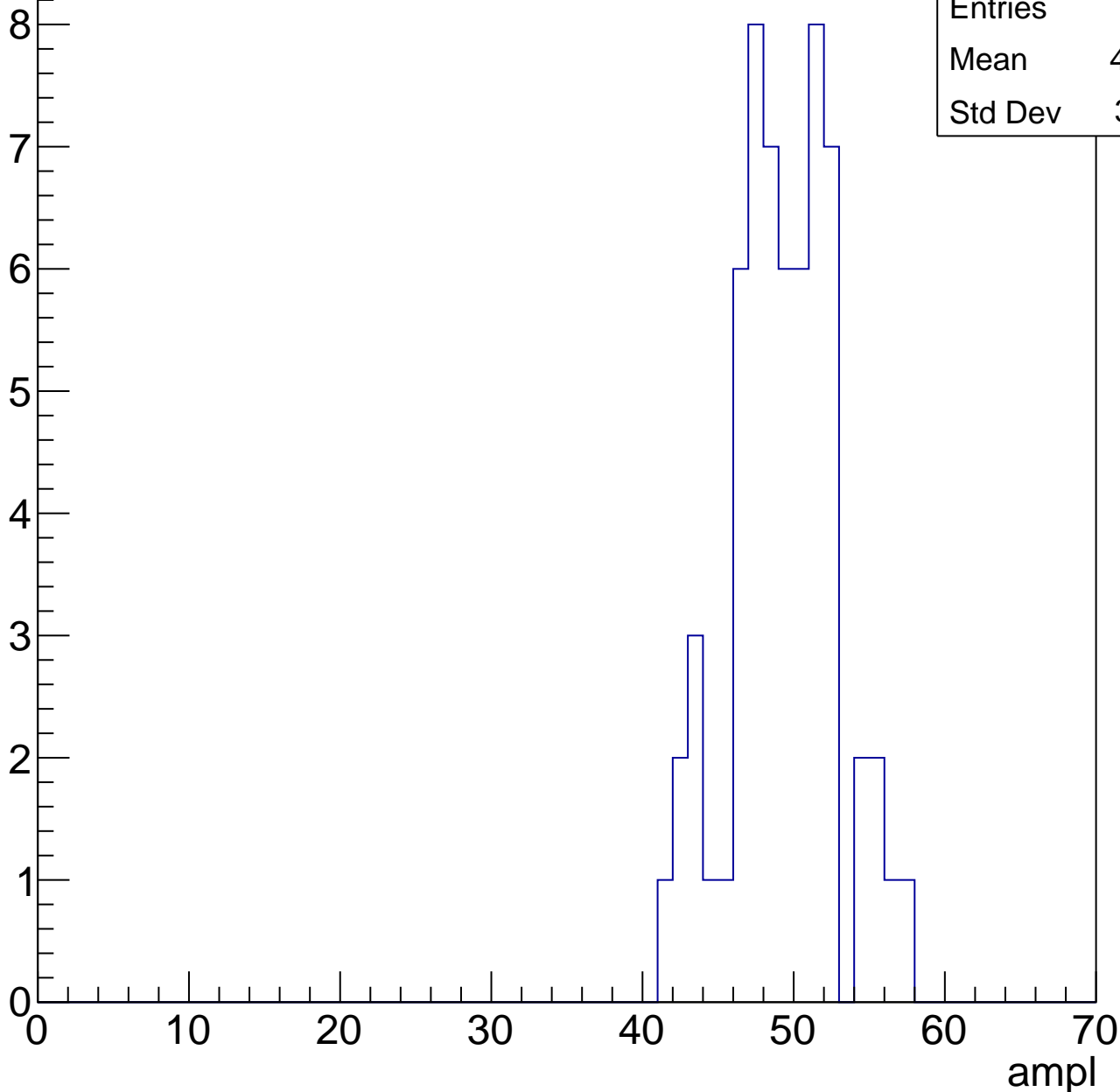


B1L103S, U9-ch51, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	48.84
Std Dev	3.451

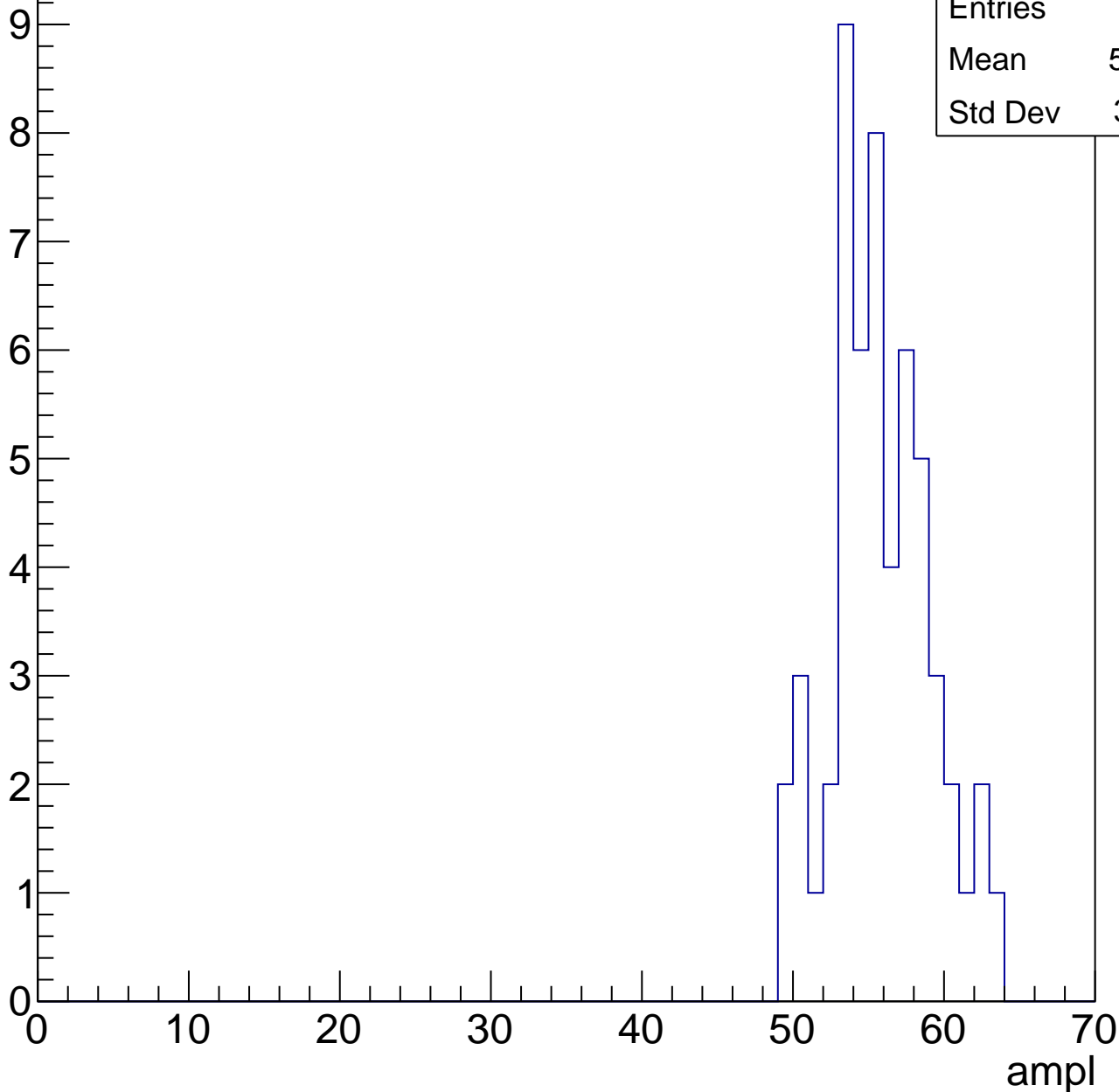


B1L103S, U9-ch51, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	55.36
Std Dev	3.261

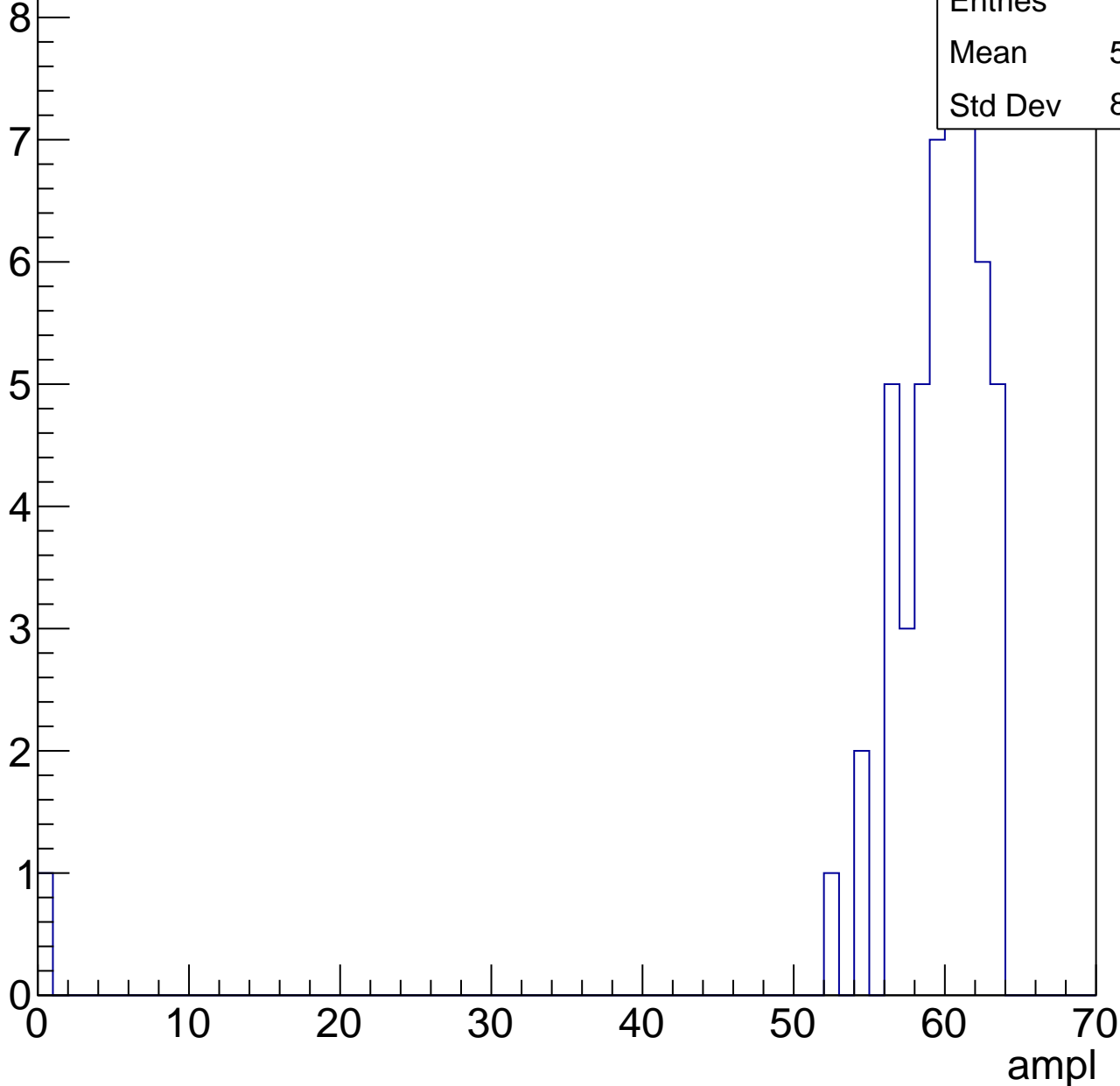


B1L103S, U9-ch51, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

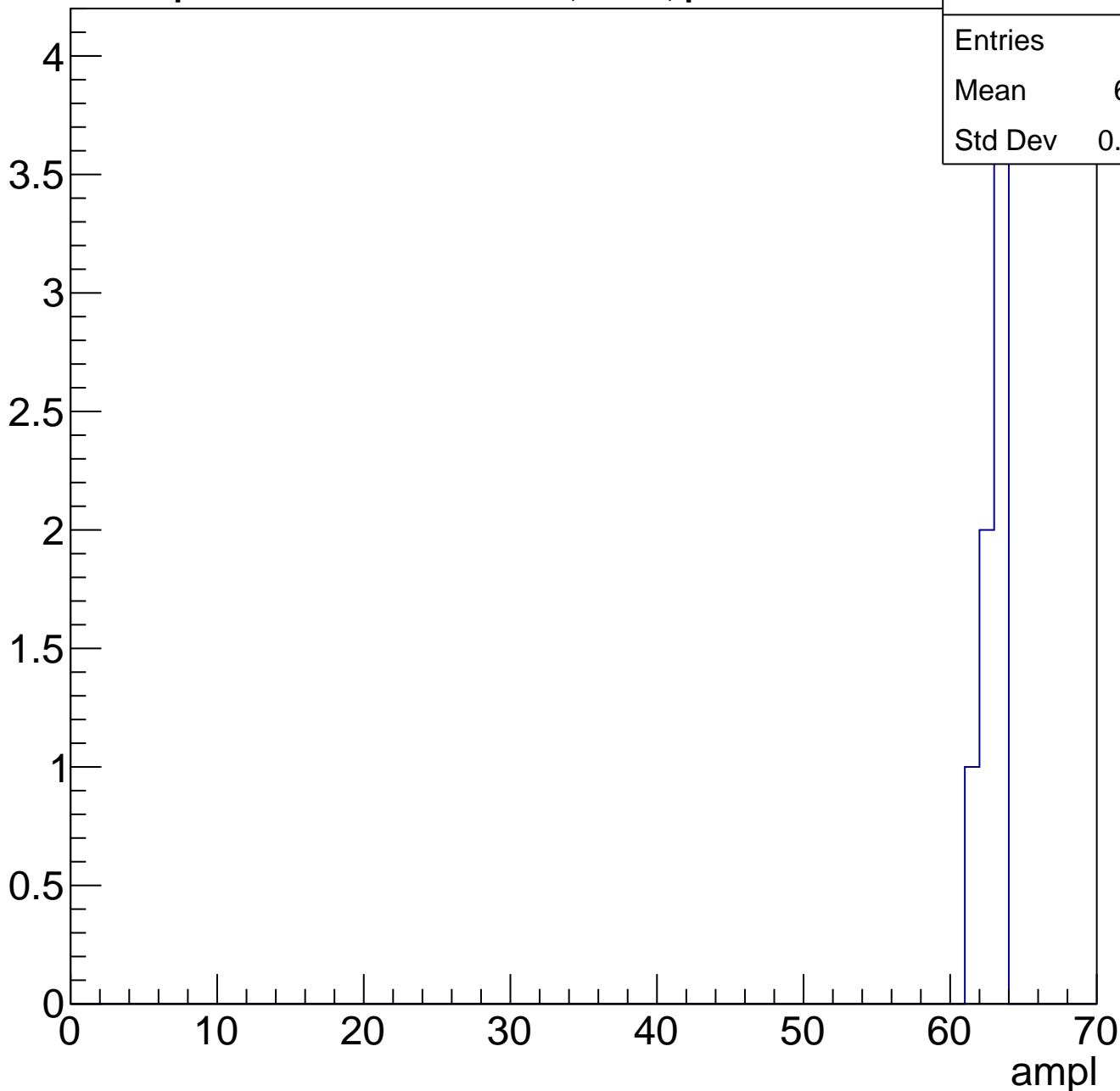
Entries	51
Mean	58.22
Std Dev	8.614



B1L103S, U9-ch51, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch51, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch52, adc0

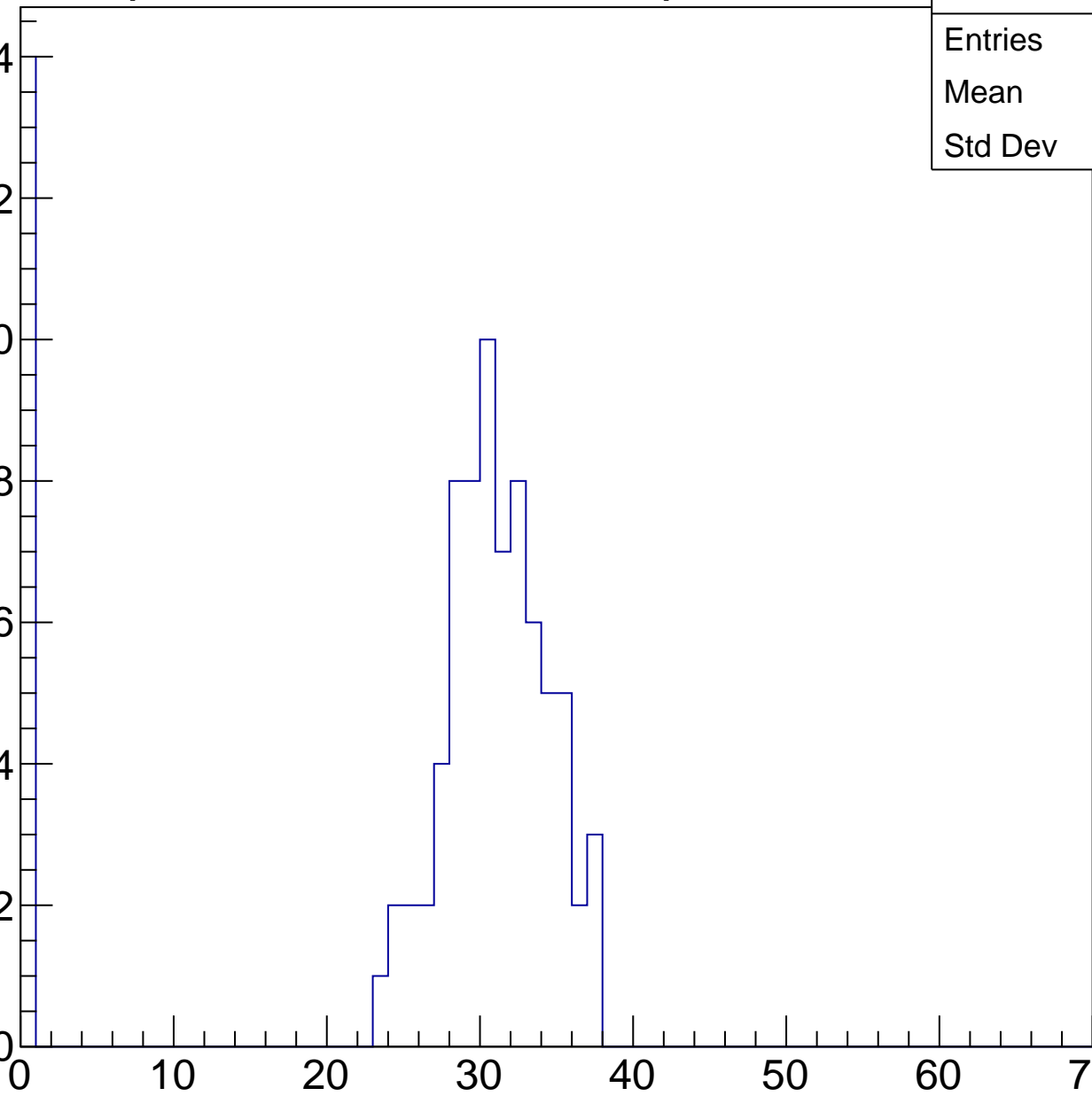
calib_packv5_041523_1651.root, FC#0, port C2

Entries	87
Mean	25.7
Std Dev	11.64

Entry

14
12
10
8
6
4
2
0

ampl

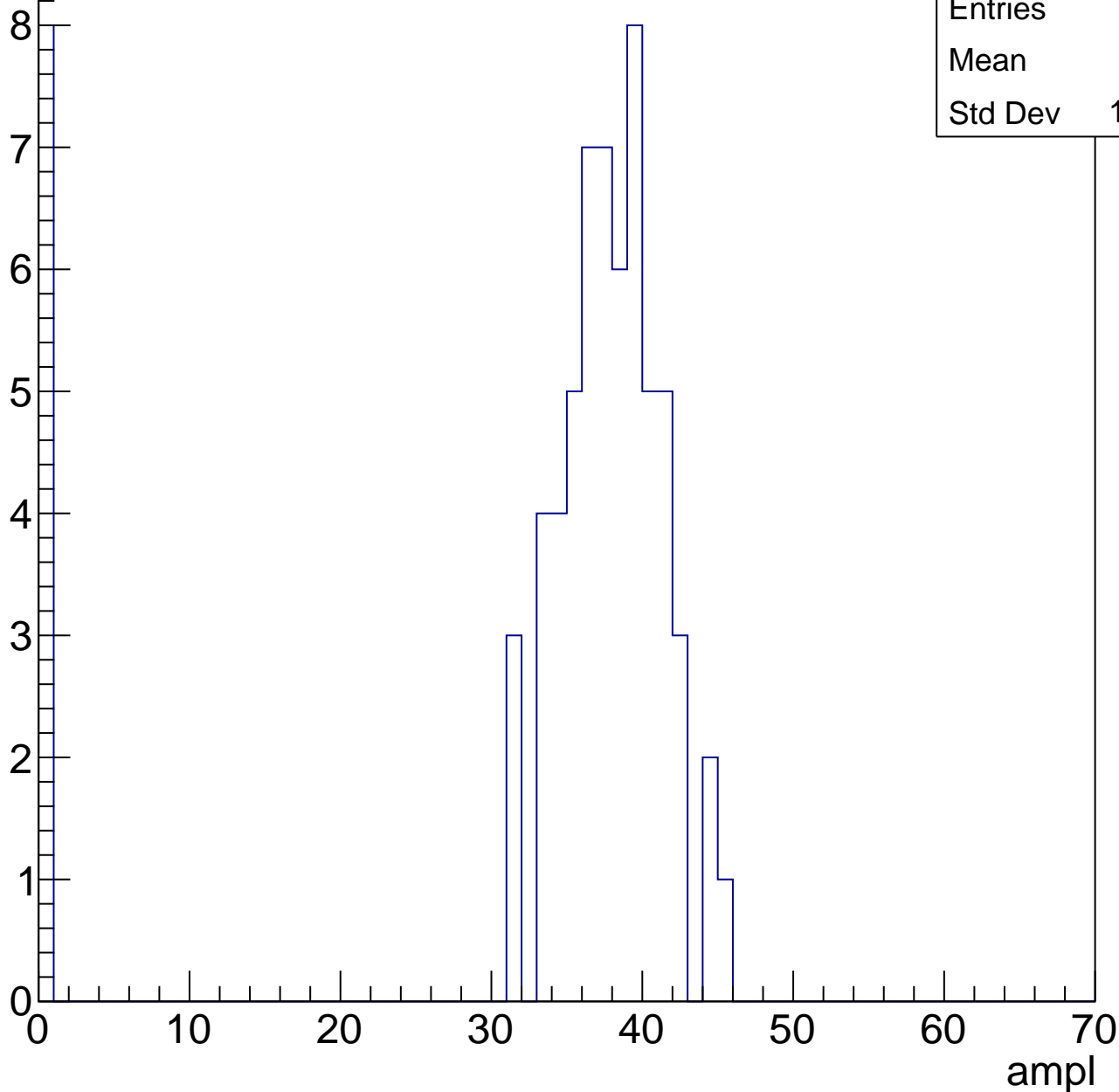


B1L103S, U9-ch52, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	33.1
Std Dev	12.46

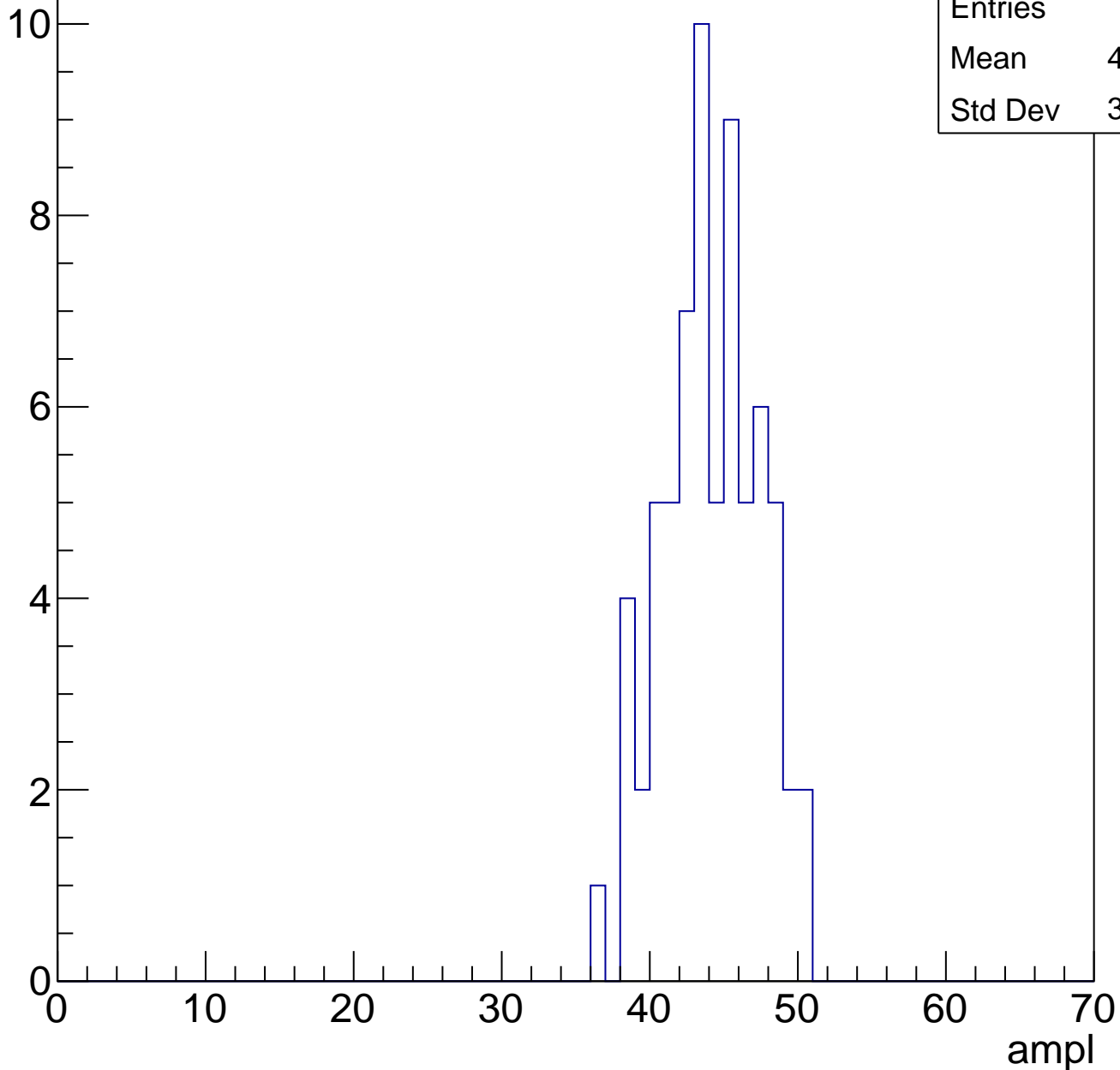


B1L103S, U9-ch52, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	68
Mean	43.68
Std Dev	3.206

Entry

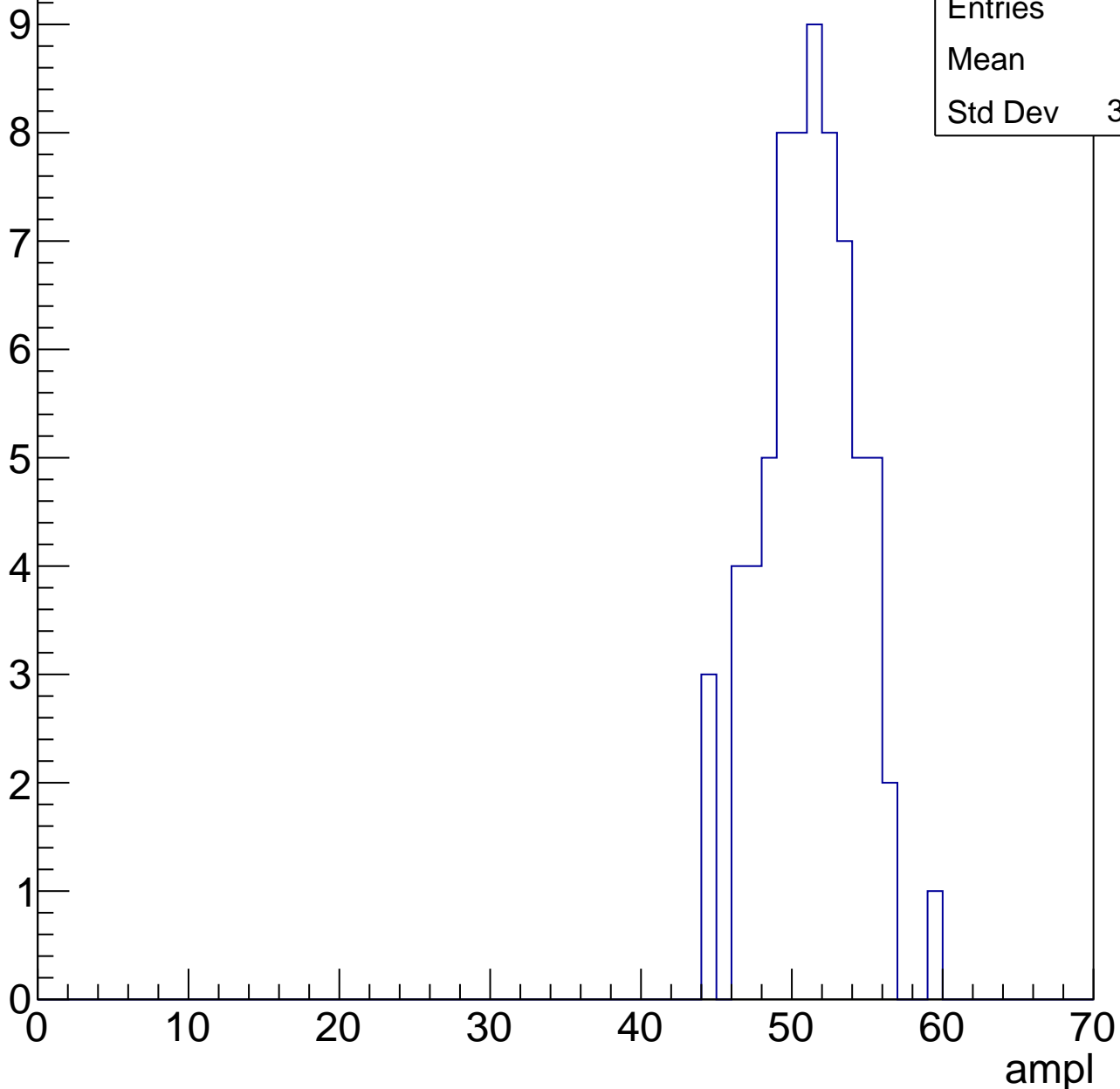


B1L103S, U9-ch52, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	50.7
Std Dev	3.104

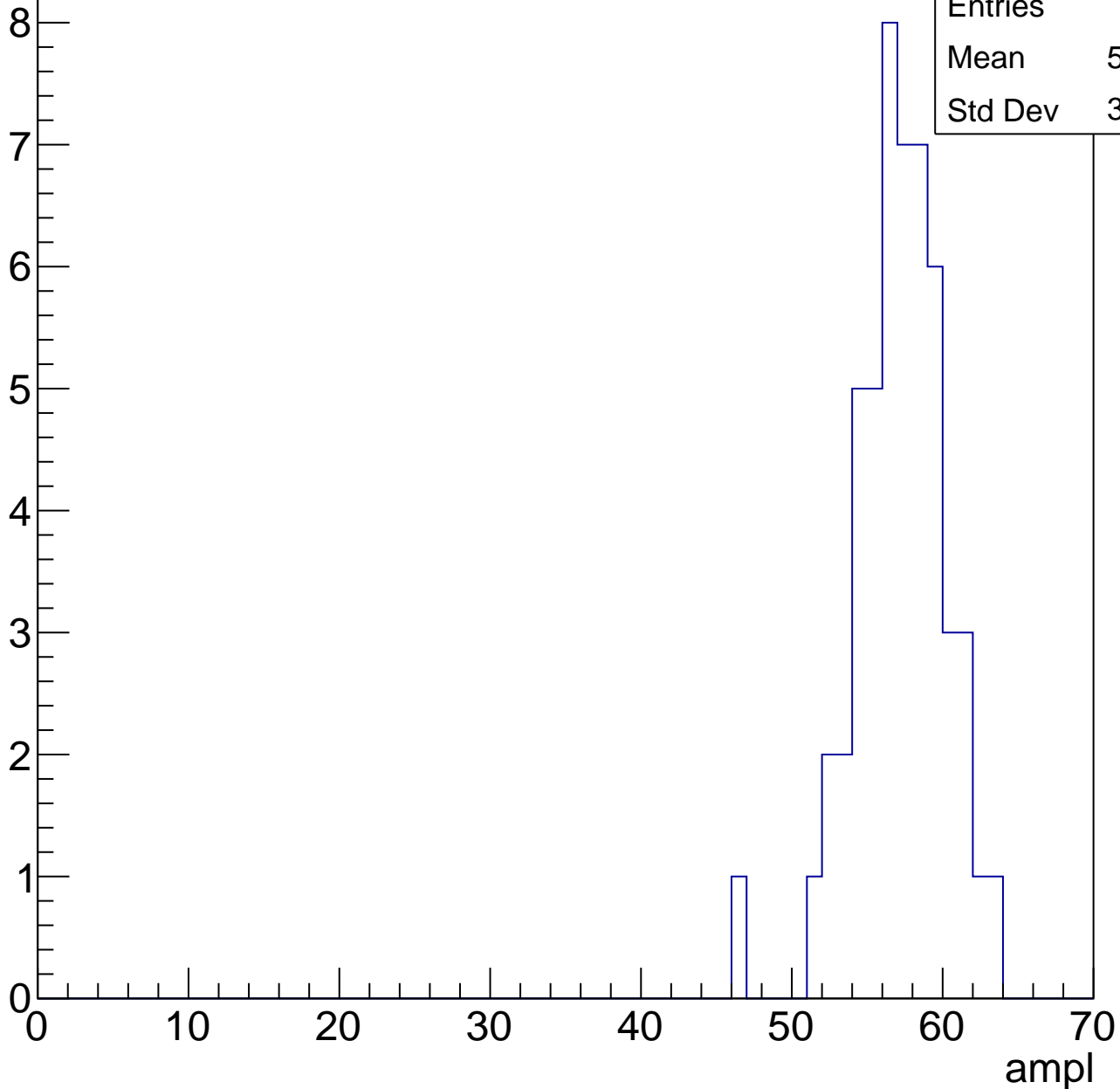


B1L103S, U9-ch52, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	56.67
Std Dev	3.017

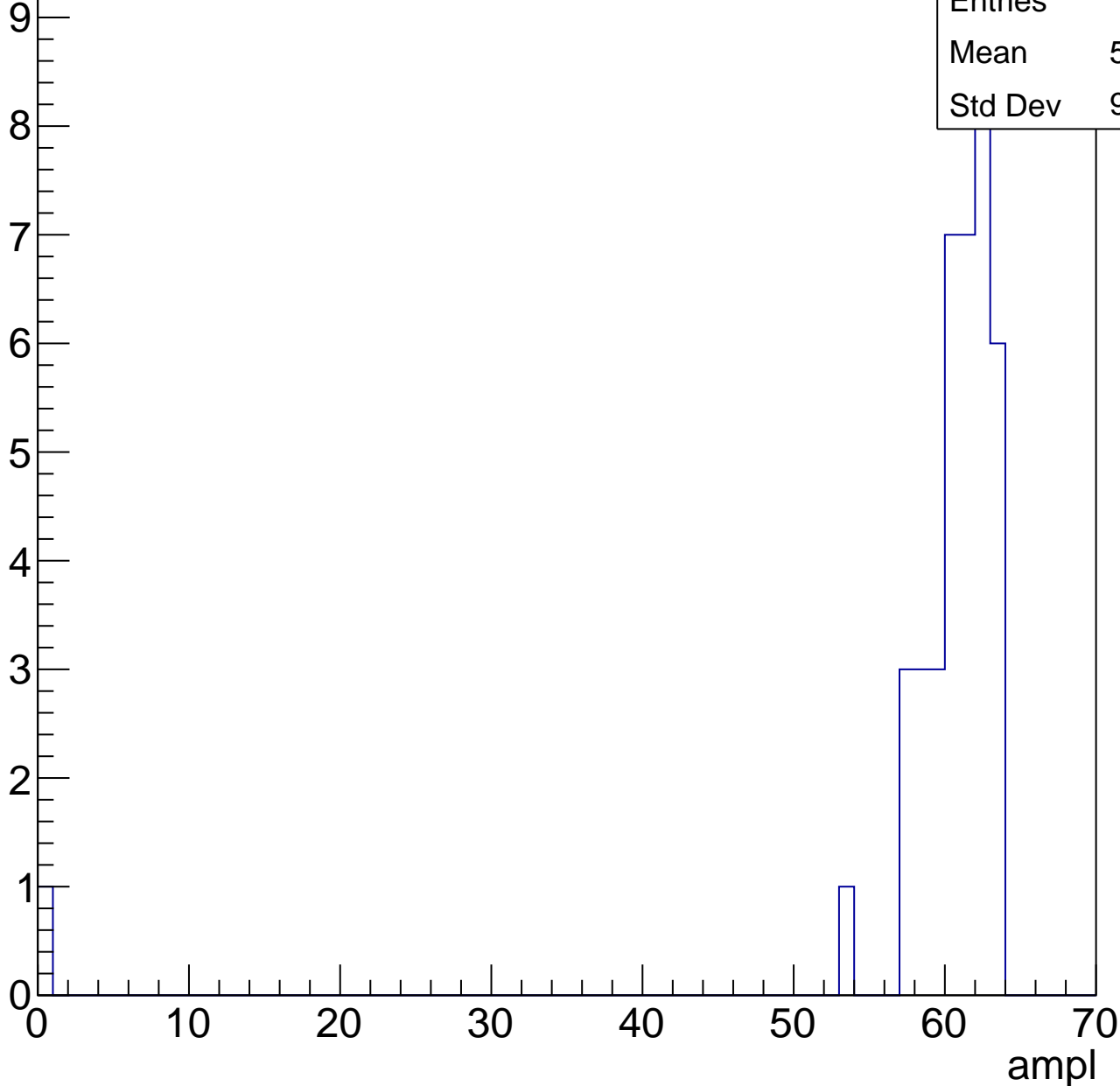


B1L103S, U9-ch52, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	58.95
Std Dev	9.675



B1L103S, U9-ch52, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

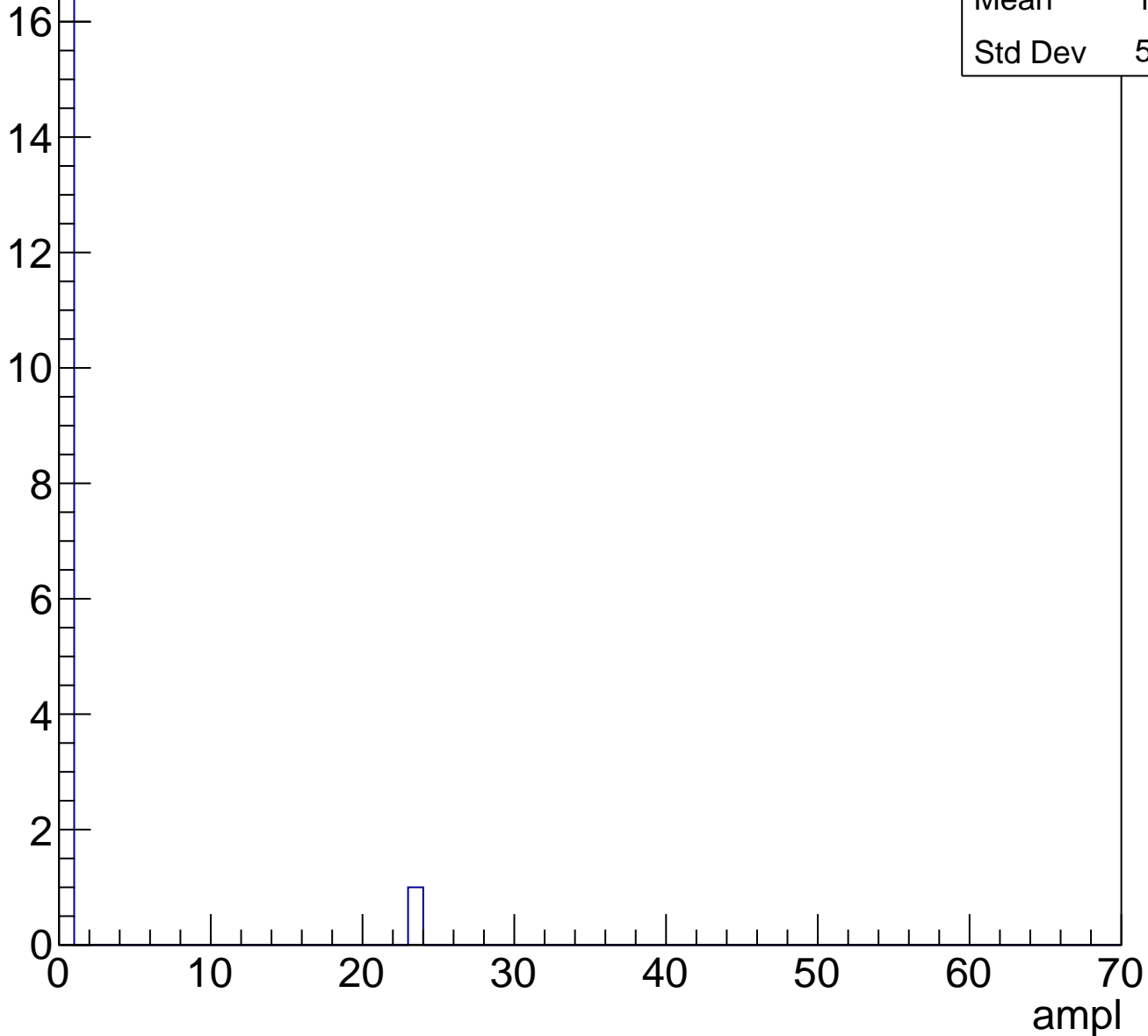


B1L103S, U9-ch52, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	18
Mean	1.278
Std Dev	5.268

Entry



B1L103S, U9-ch53, adc0

calib_packv5_041523_1651.root, FC#0, port C2

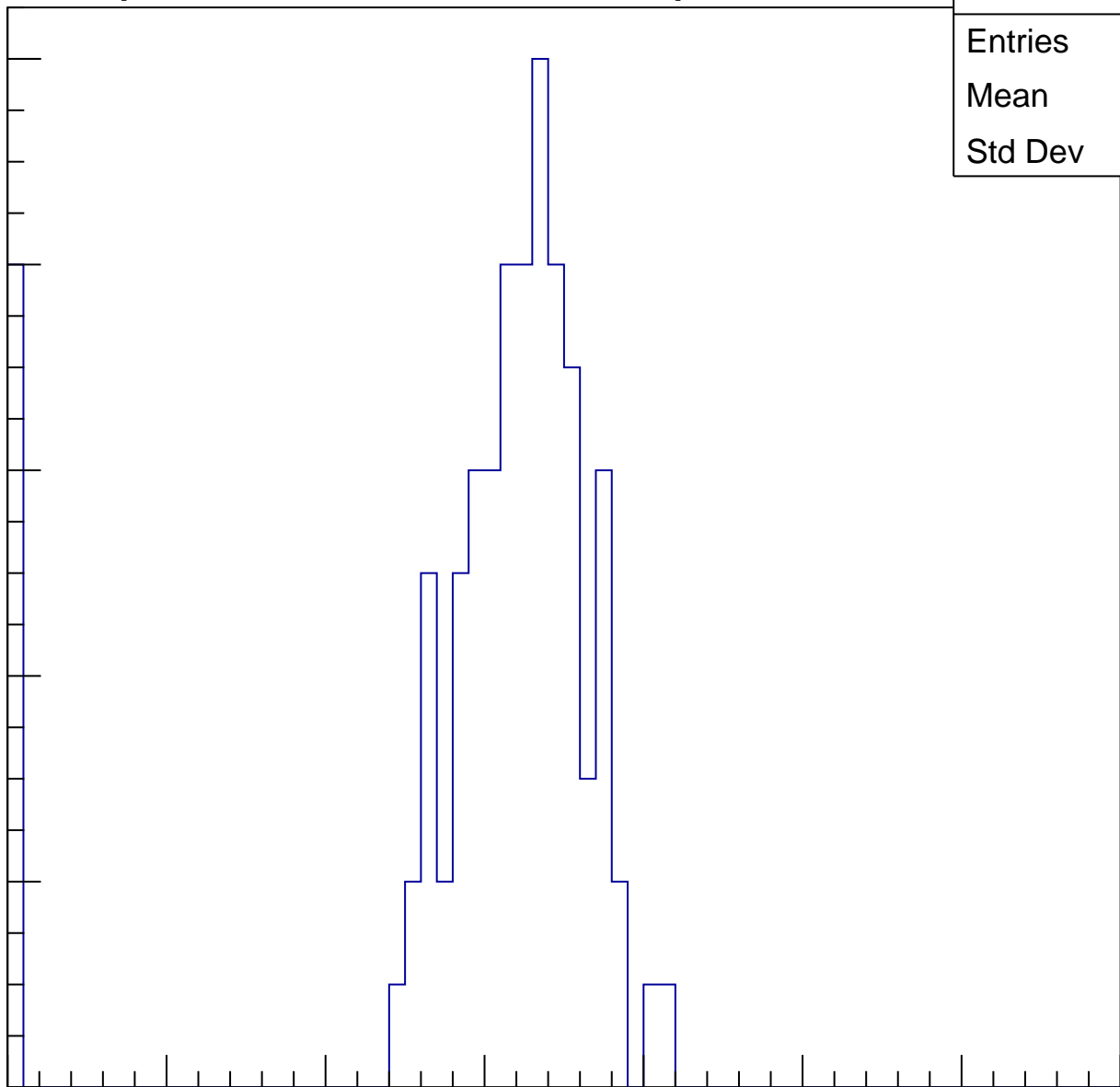
Entries	89
Mean	29.1
Std Dev	9.785

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl



B1L103S, U9-ch53, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	70
Mean	33.1
Std Dev	14.53

Entry

10

8

6

4

2

0

0

10

20

30

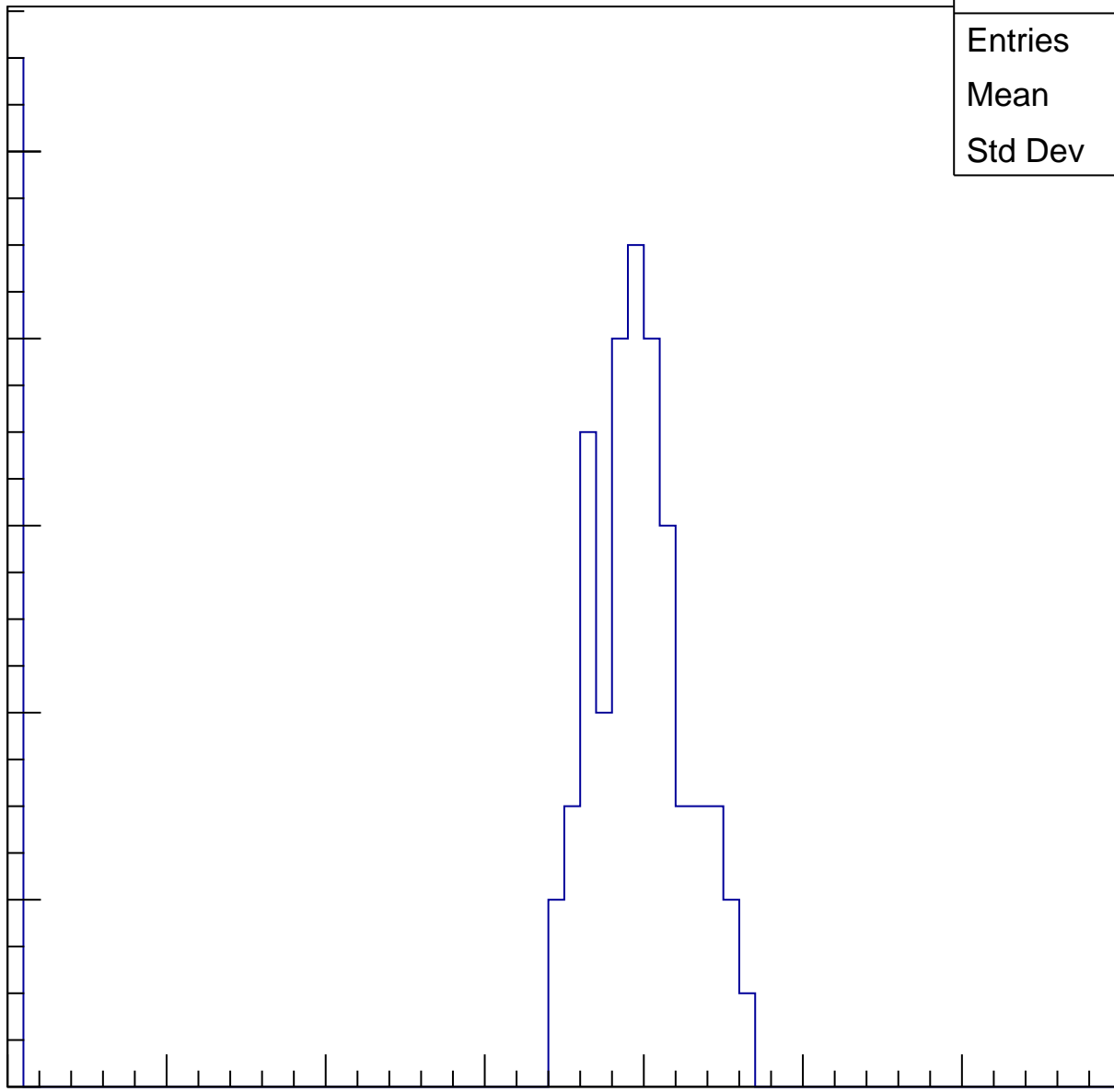
40

50

60

70

ampl



B1L103S, U9-ch53, adc2

calib_packv5_041523_1651.root, FC#0, port C2

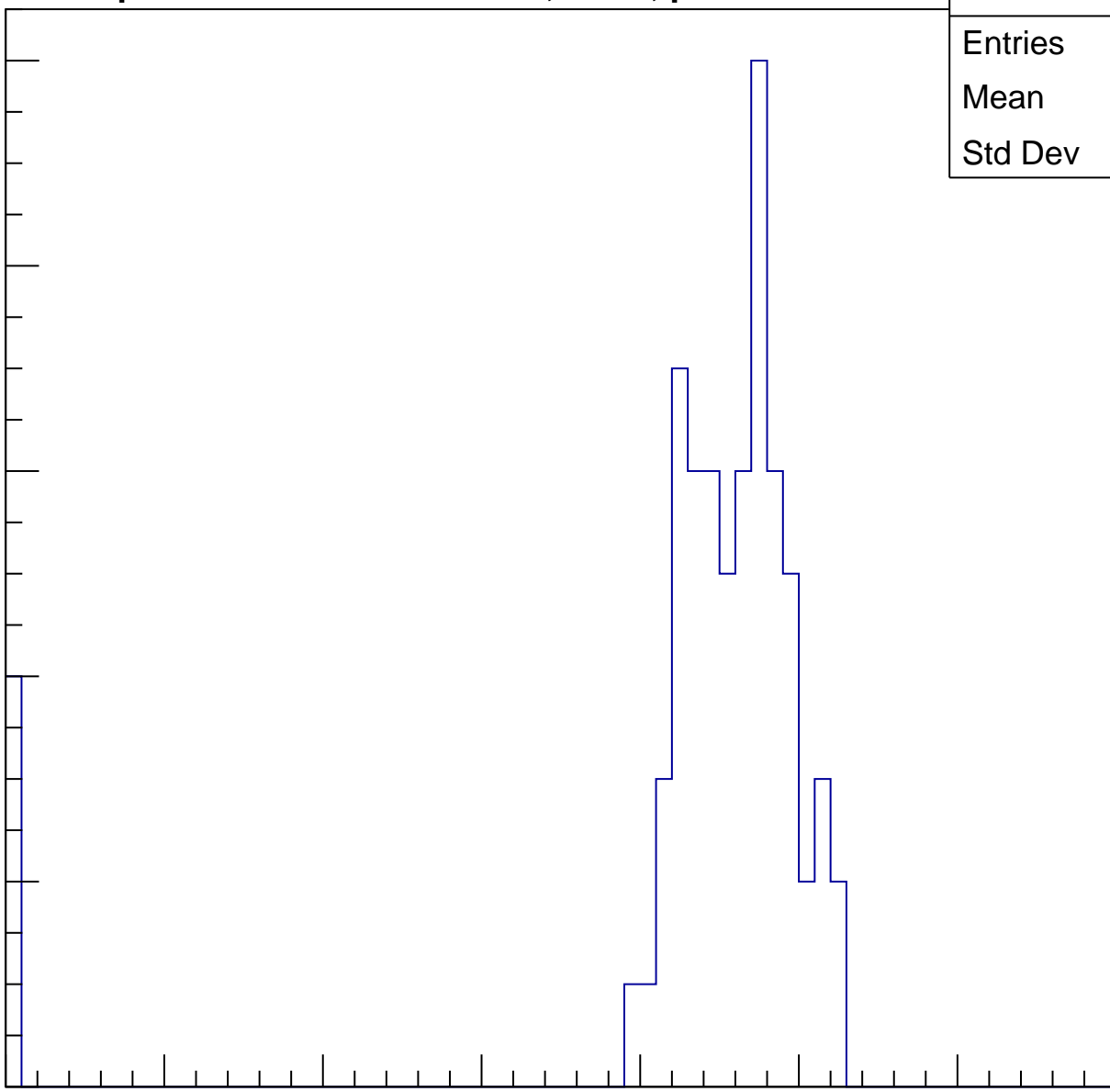
Entries	67
Mean	42.97
Std Dev	11.24

Entry

10
8
6
4
2
0

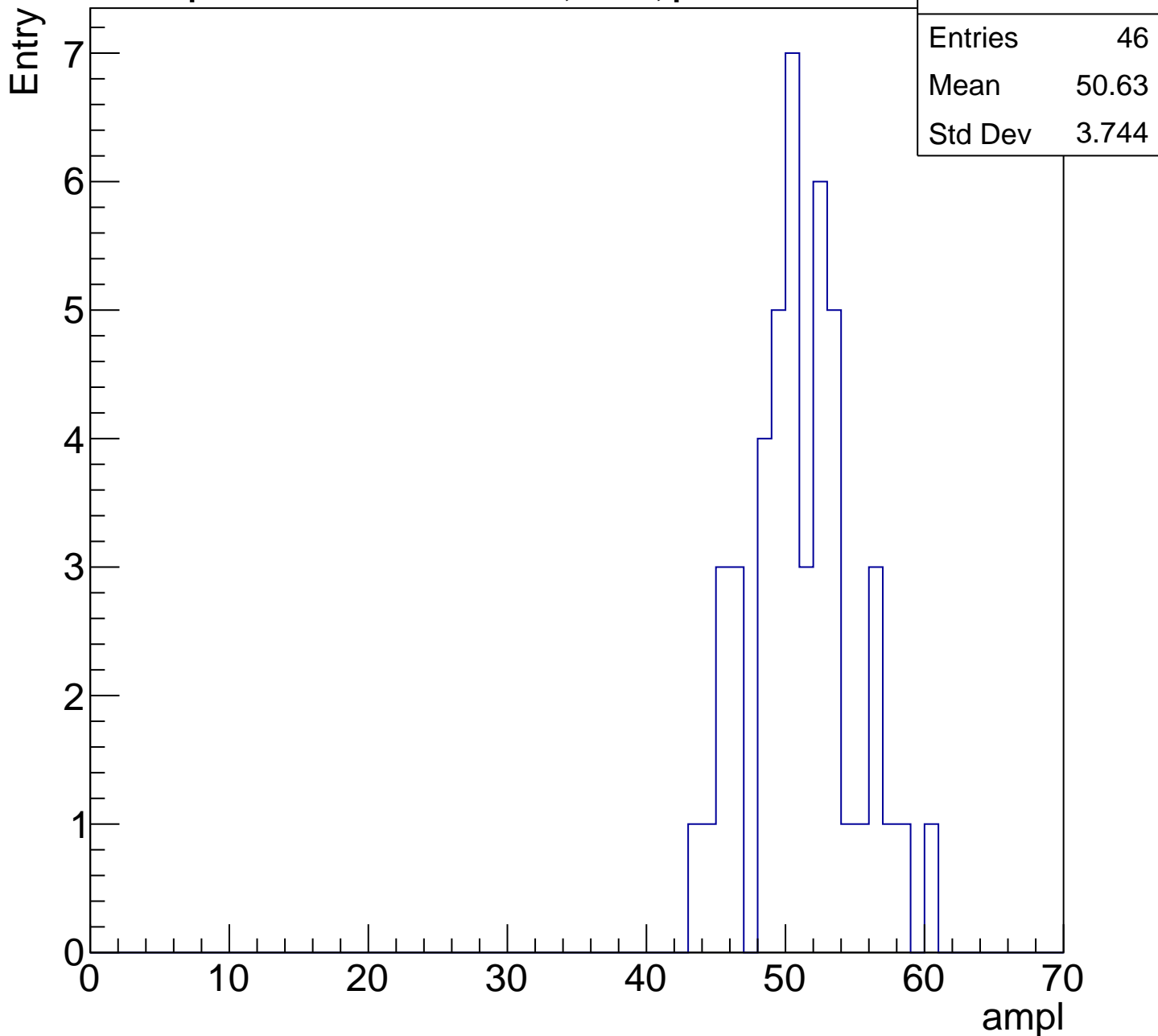
0 10 20 30 40 50 60 70

ampl



B1L103S, U9-ch53, adc3

calib_packv5_041523_1651.root, FC#0, port C2

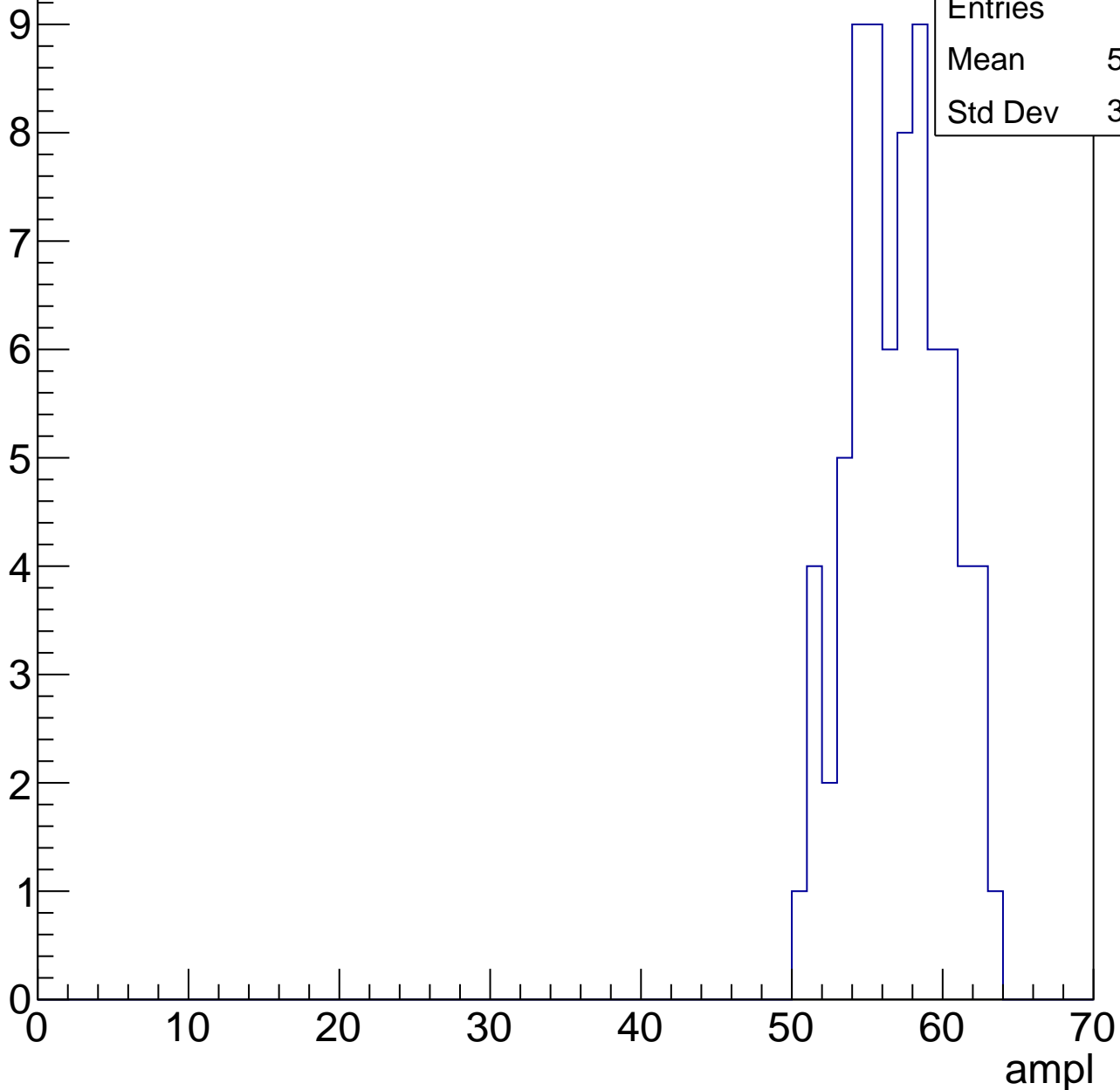


B1L103S, U9-ch53, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	56.58
Std Dev	3.119

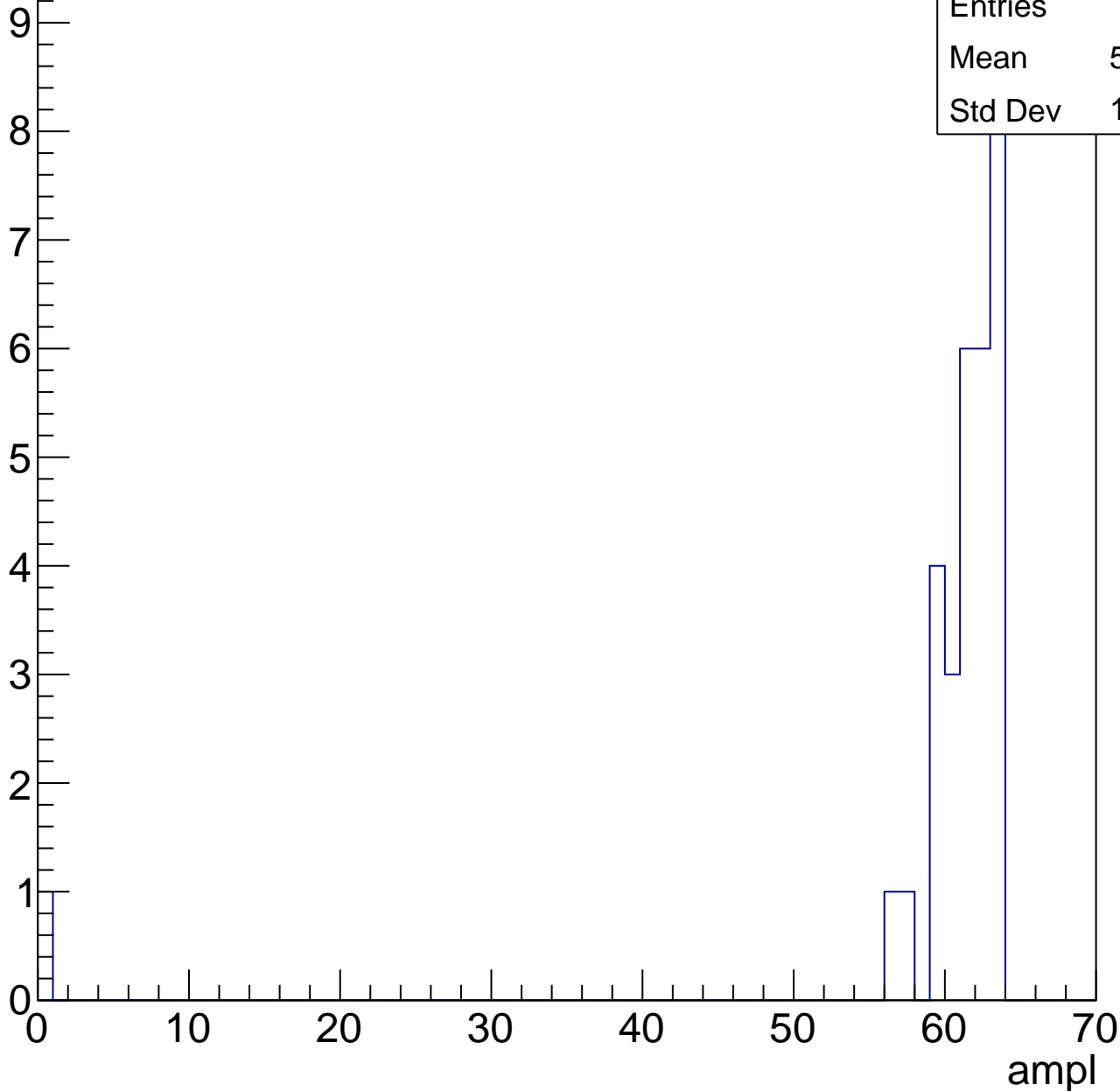


B1L103S, U9-ch53, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	31
Mean	59.16
Std Dev	10.95



B1L103S, U9-ch53, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

0

Mean

0

Std Dev

0

B1L103S, U9-ch53, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

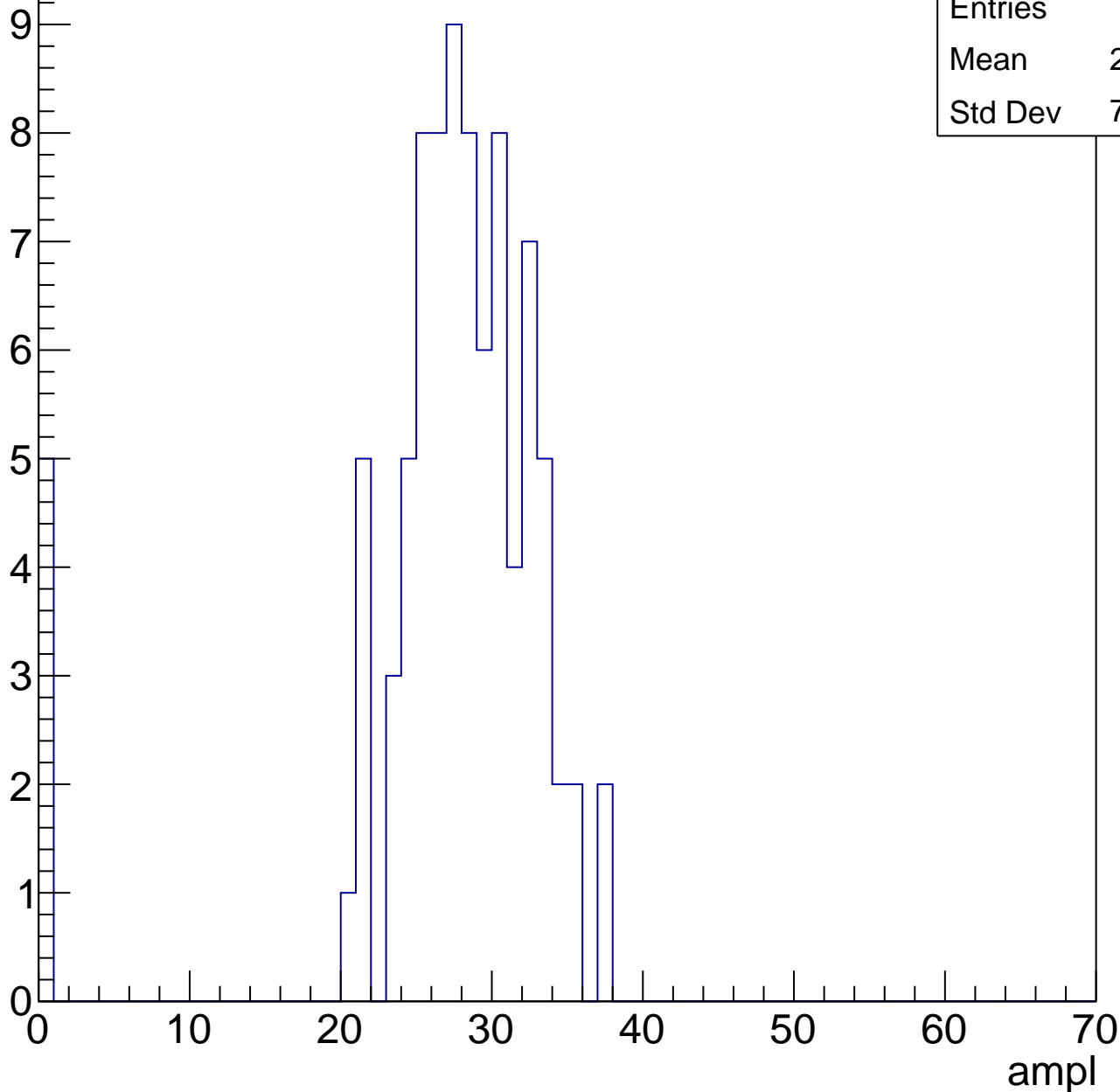


B1L103S, U9-ch54, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	88
Mean	26.45
Std Dev	7.485

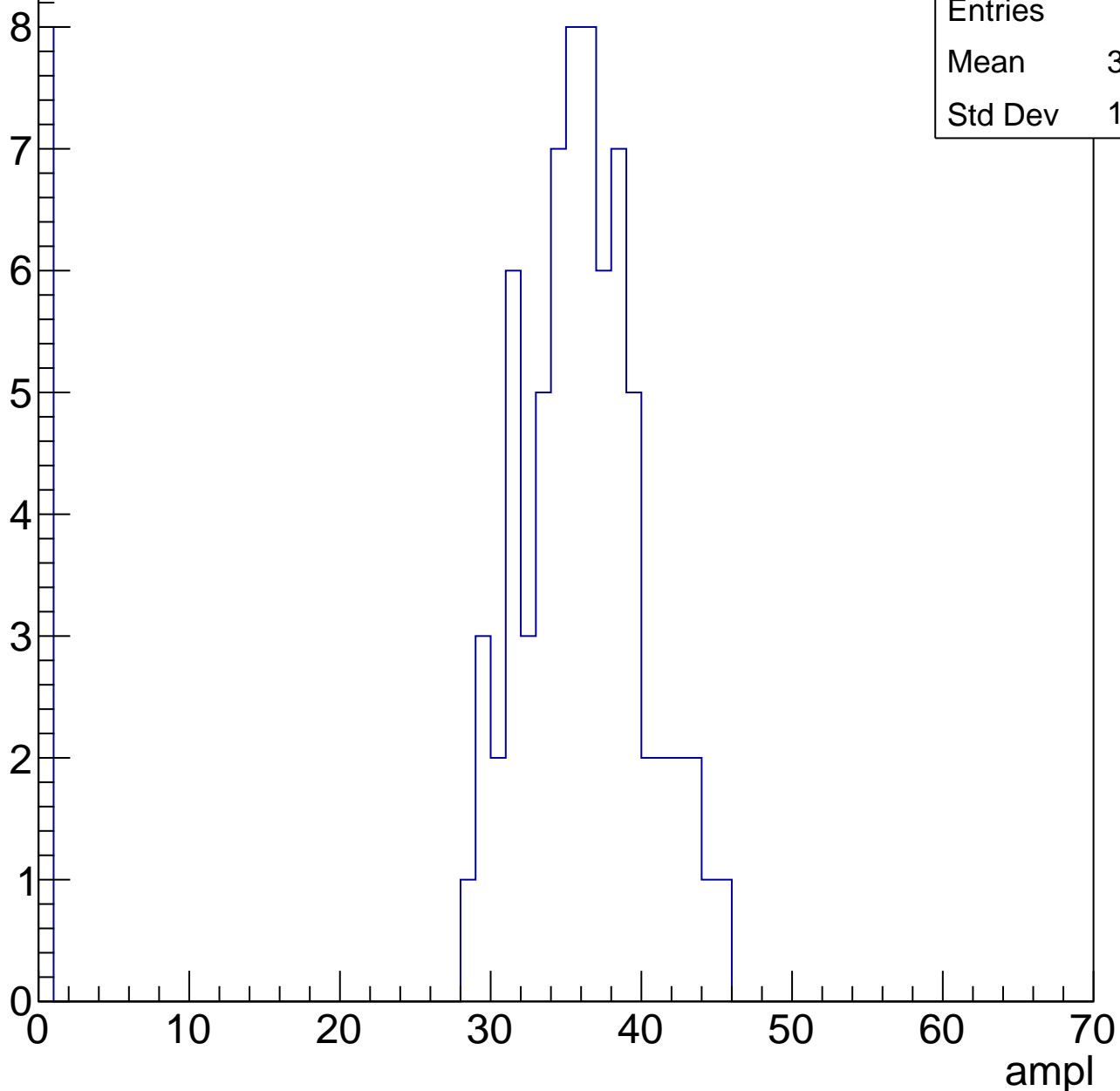


B1L103S, U9-ch54, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	79
Mean	32.05
Std Dev	11.35

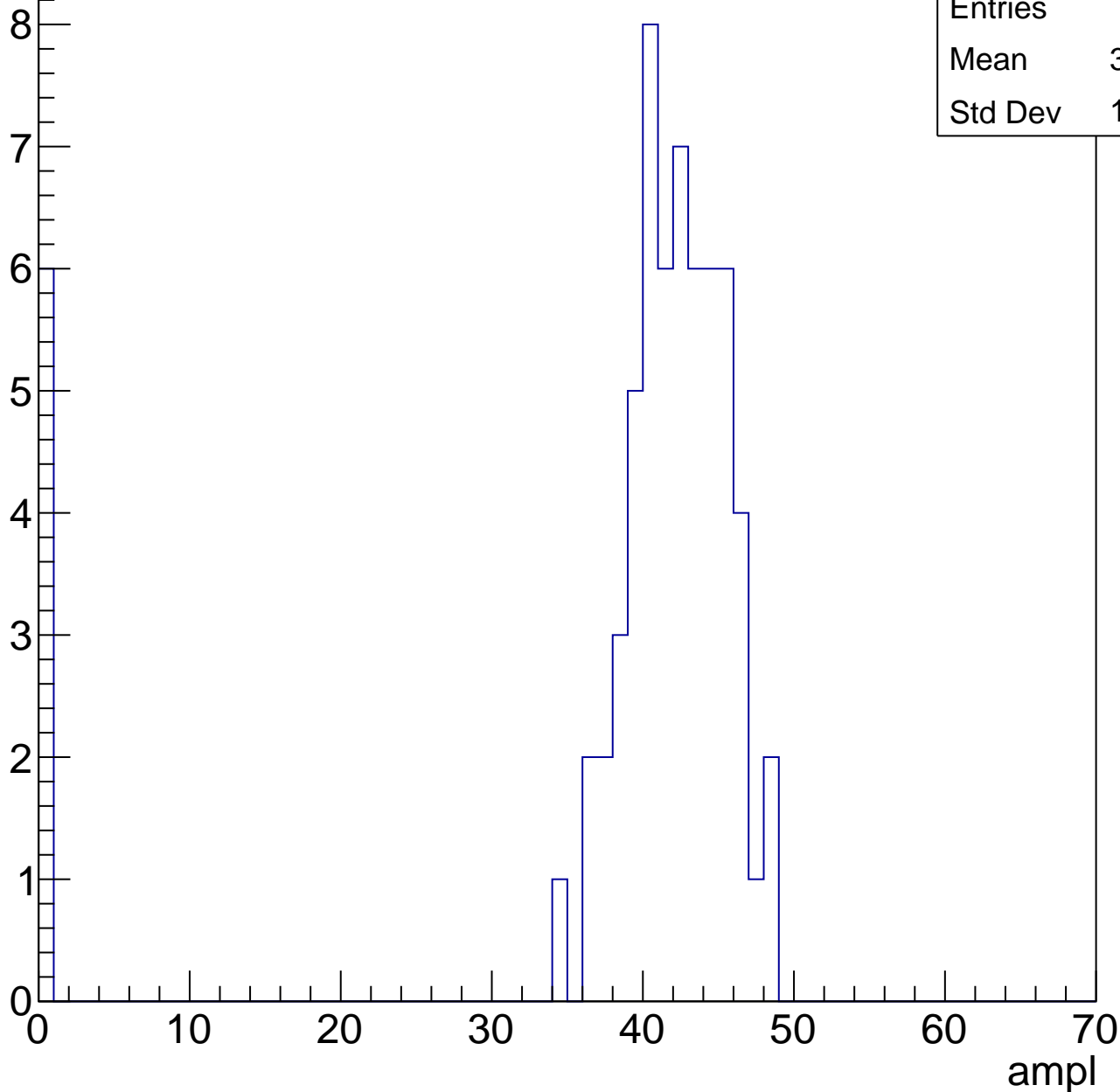


B1L103S, U9-ch54, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	37.97
Std Dev	12.46

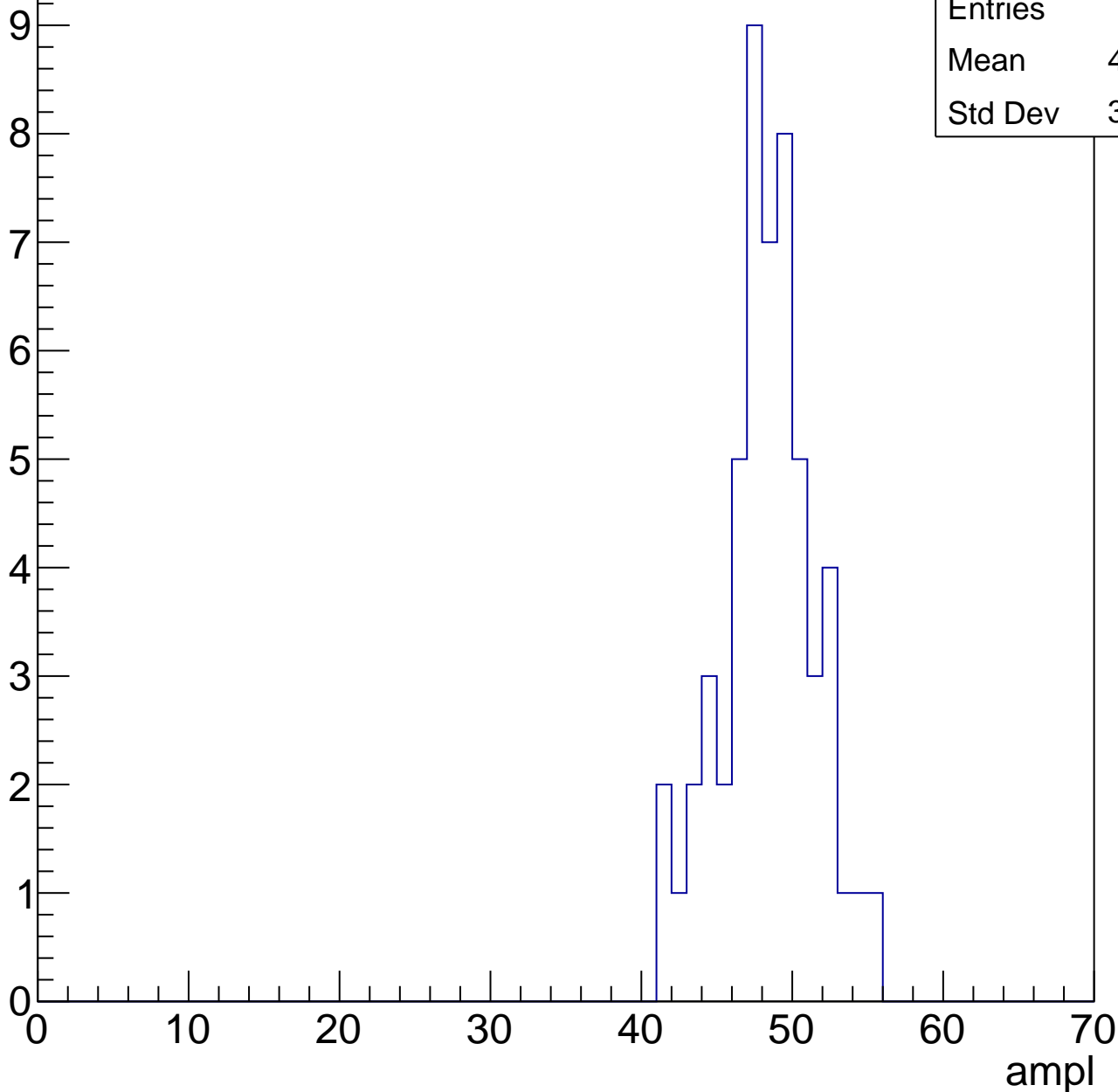


B1L103S, U9-ch54, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	47.89
Std Dev	3.065

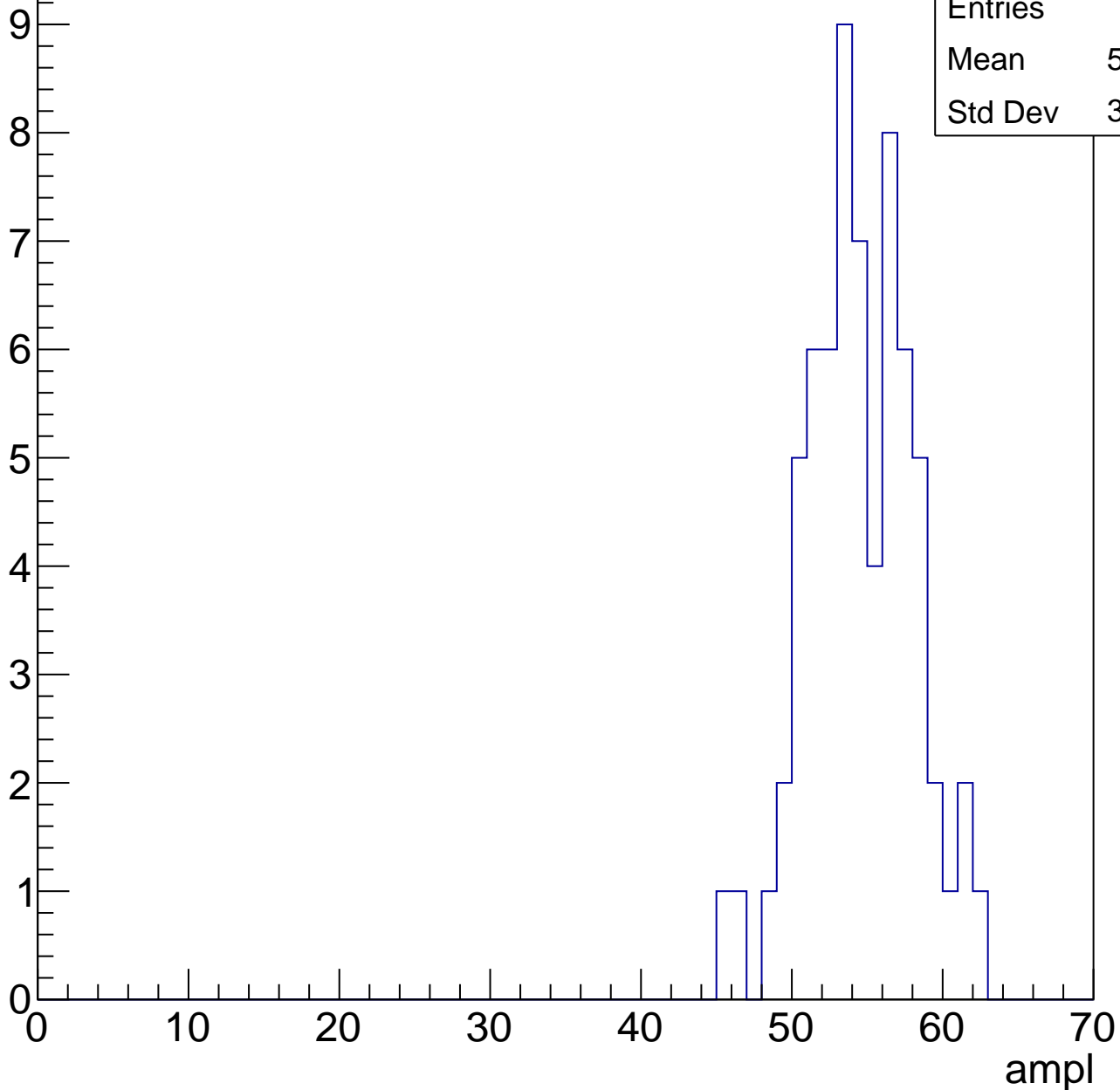


B1L103S, U9-ch54, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	54.06
Std Dev	3.489



B1L103S, U9-ch54, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

7

6

5

4

3

2

1

0

Entries 51

Mean 59.06

Std Dev 2.824

ampl

0

10

20

30

40

50

60

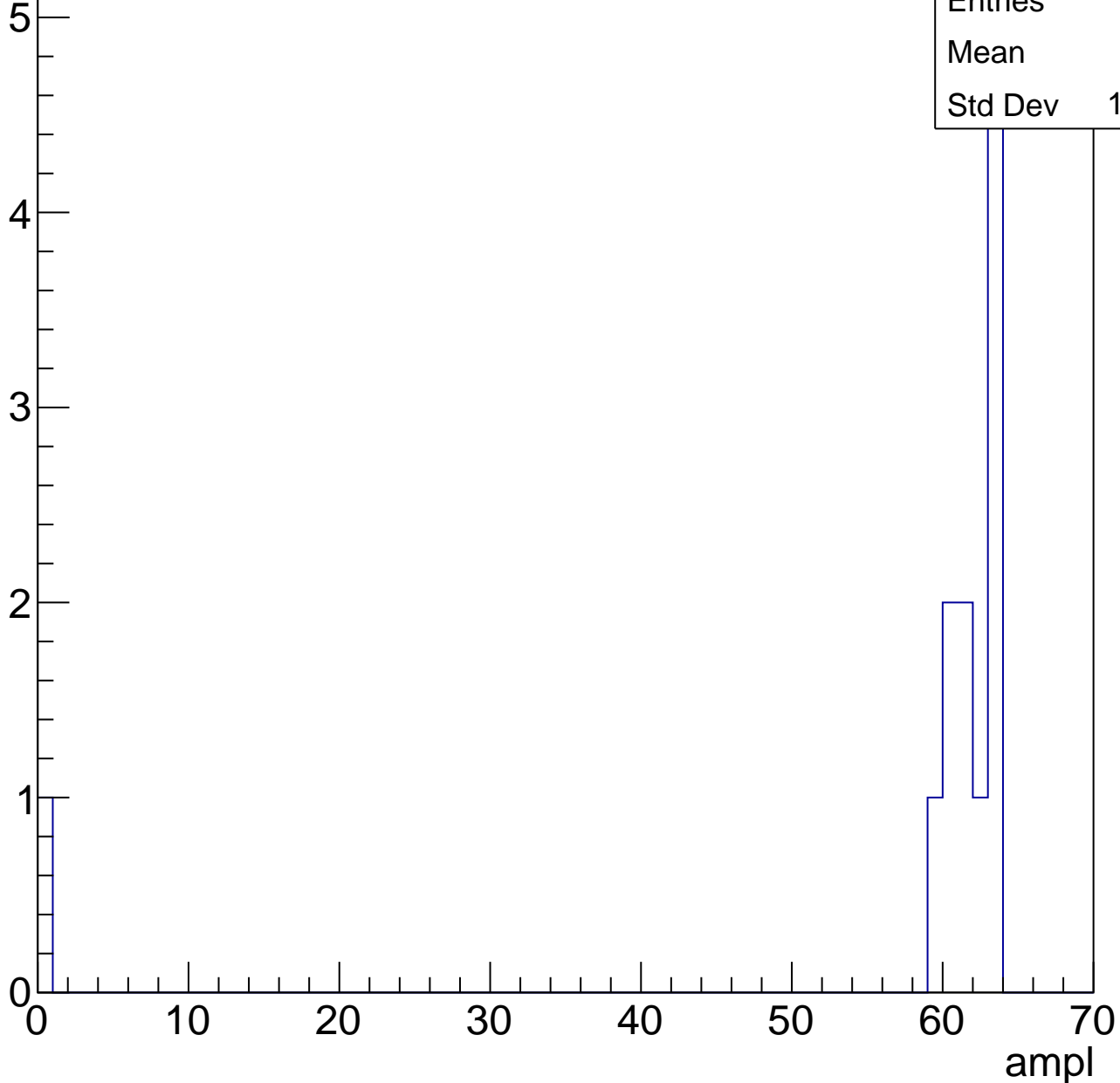
70

B1L103S, U9-ch54, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	12
Mean	56.5
Std Dev	17.09

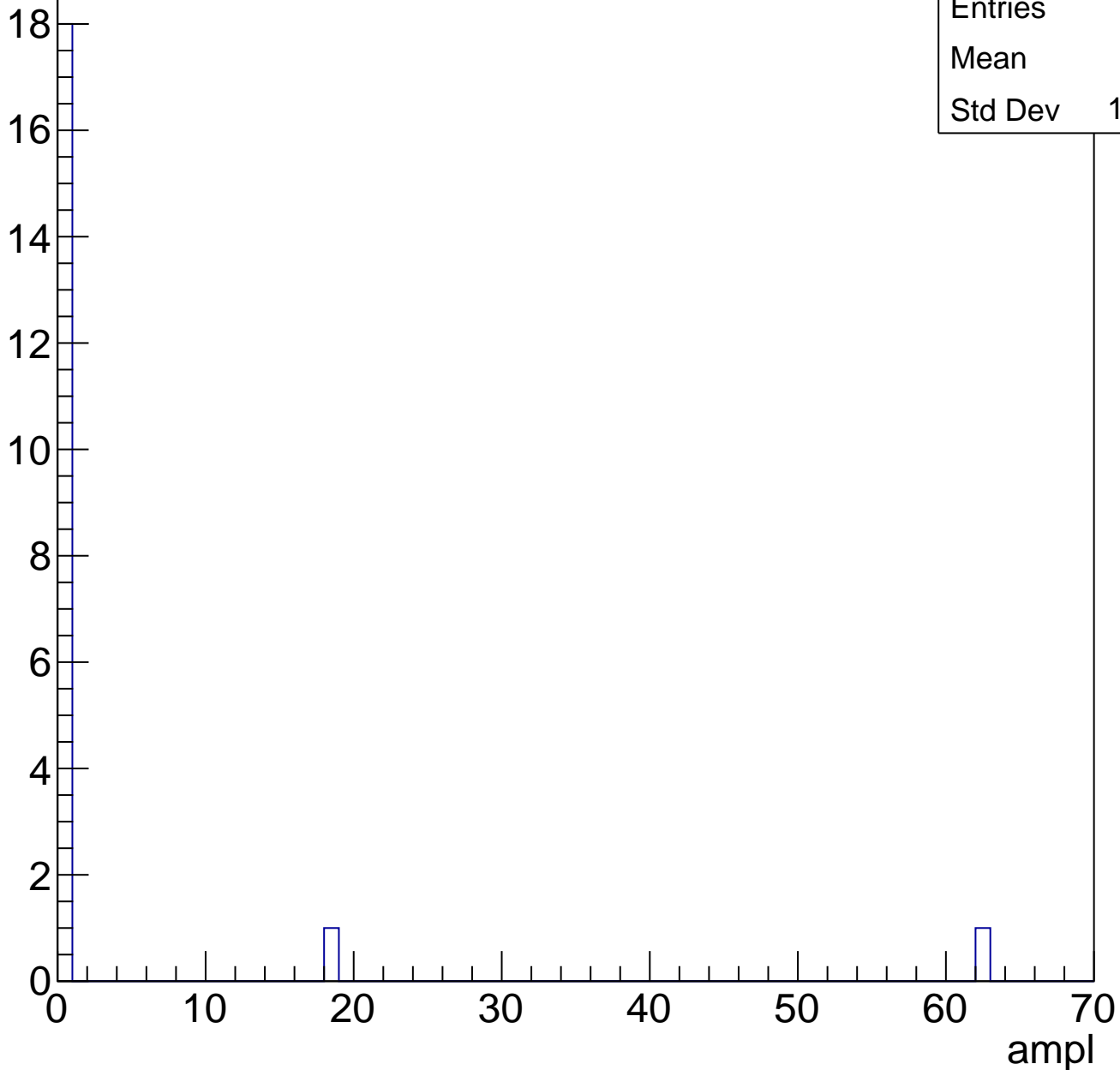


B1L103S, U9-ch54, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	4
Std Dev	13.87

Entry

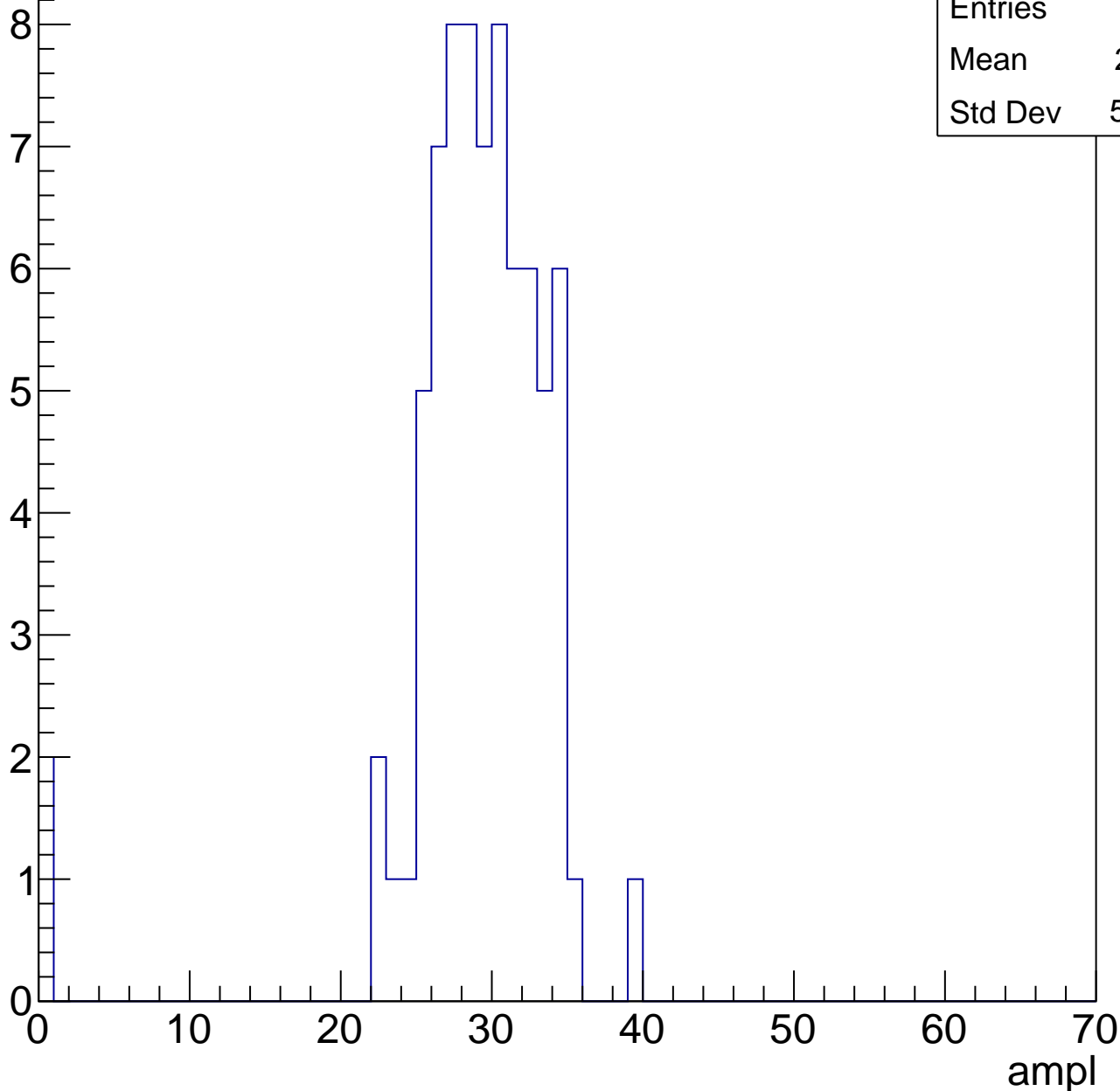


B1L103S, U9-ch55, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	28.41
Std Dev	5.754

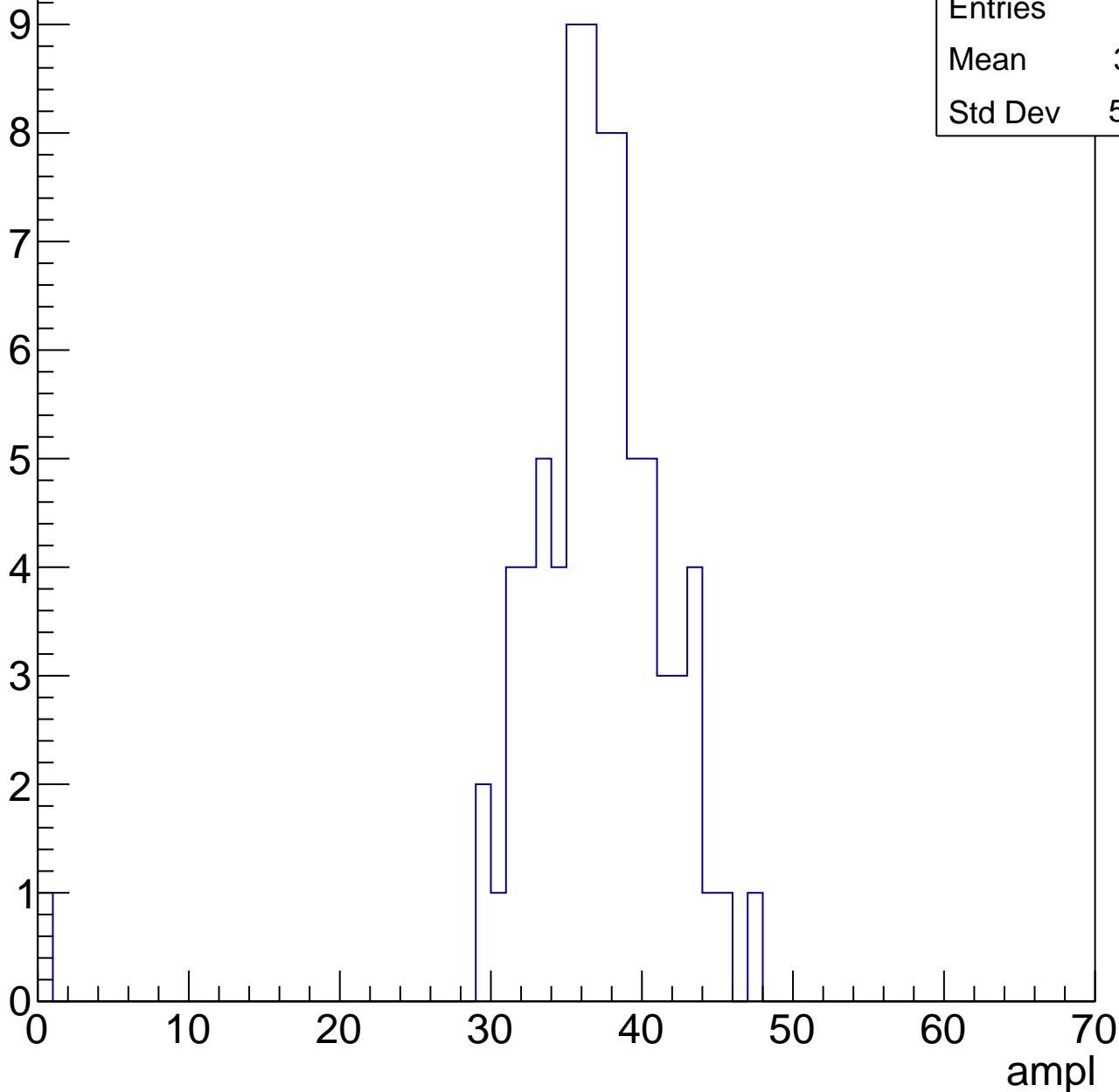


B1L103S, U9-ch55, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	36.31
Std Dev	5.623

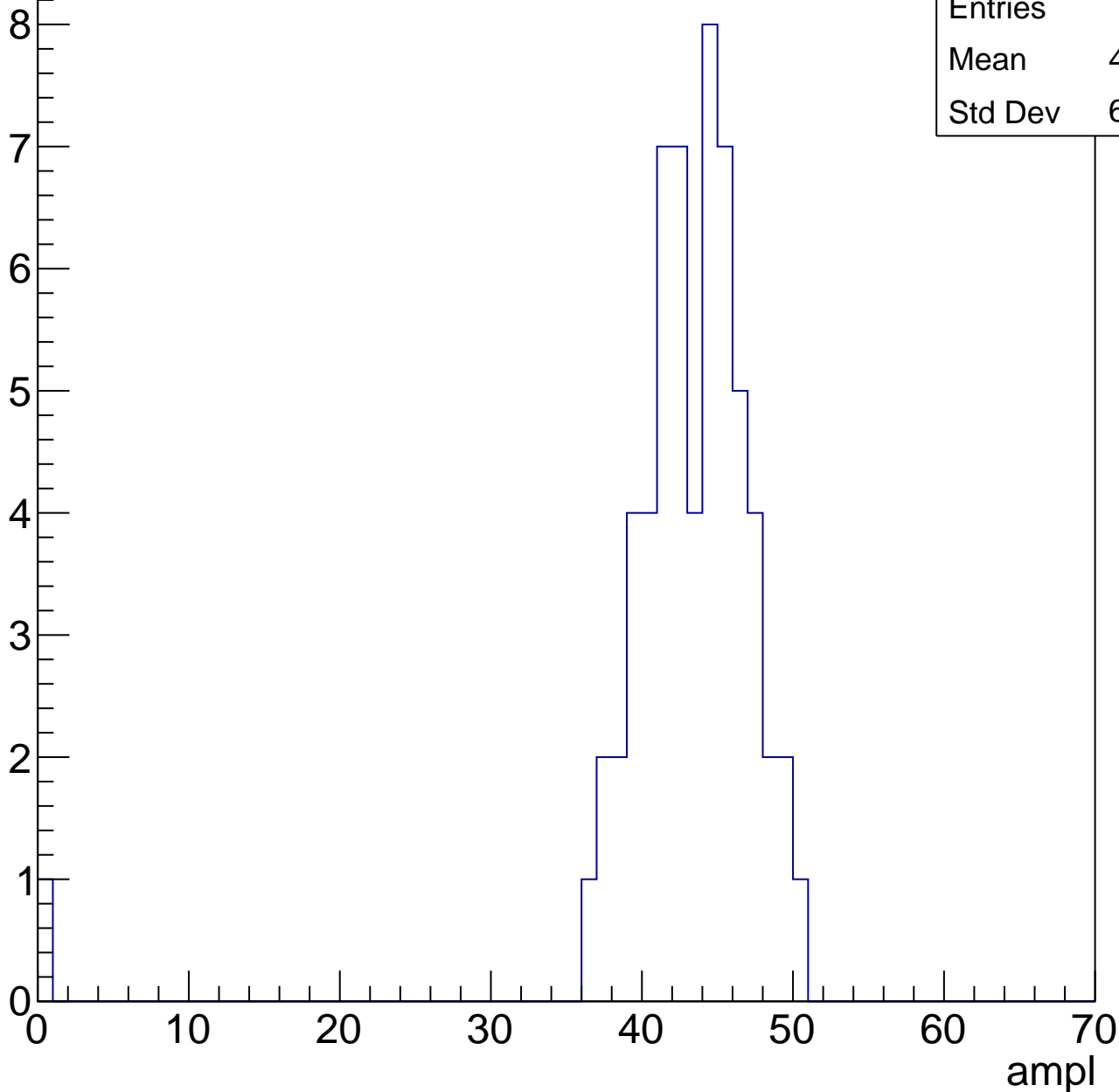


B1L103S, U9-ch55, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	42.36
Std Dev	6.332

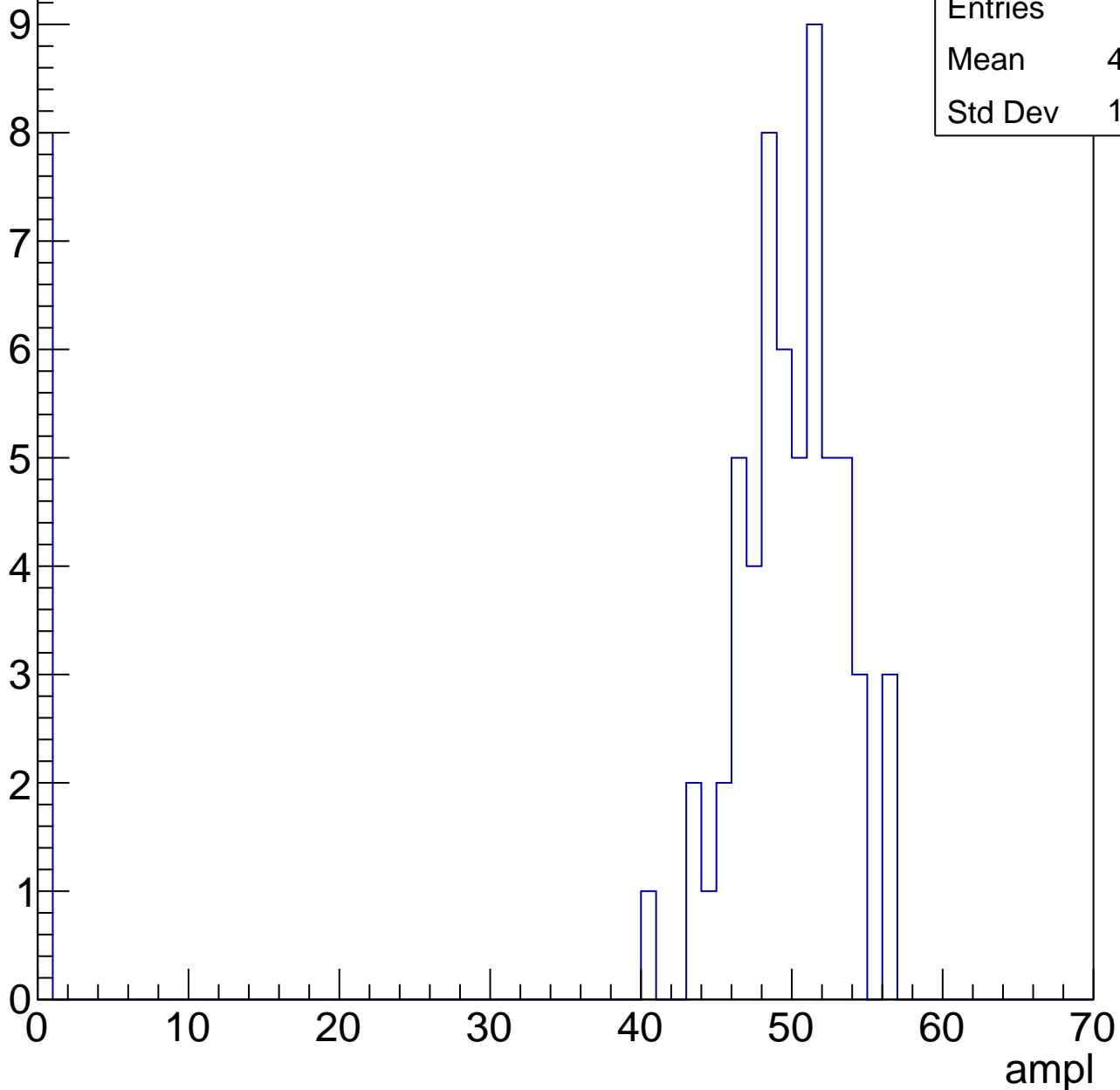


B1L103S, U9-ch55, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	43.58
Std Dev	16.35

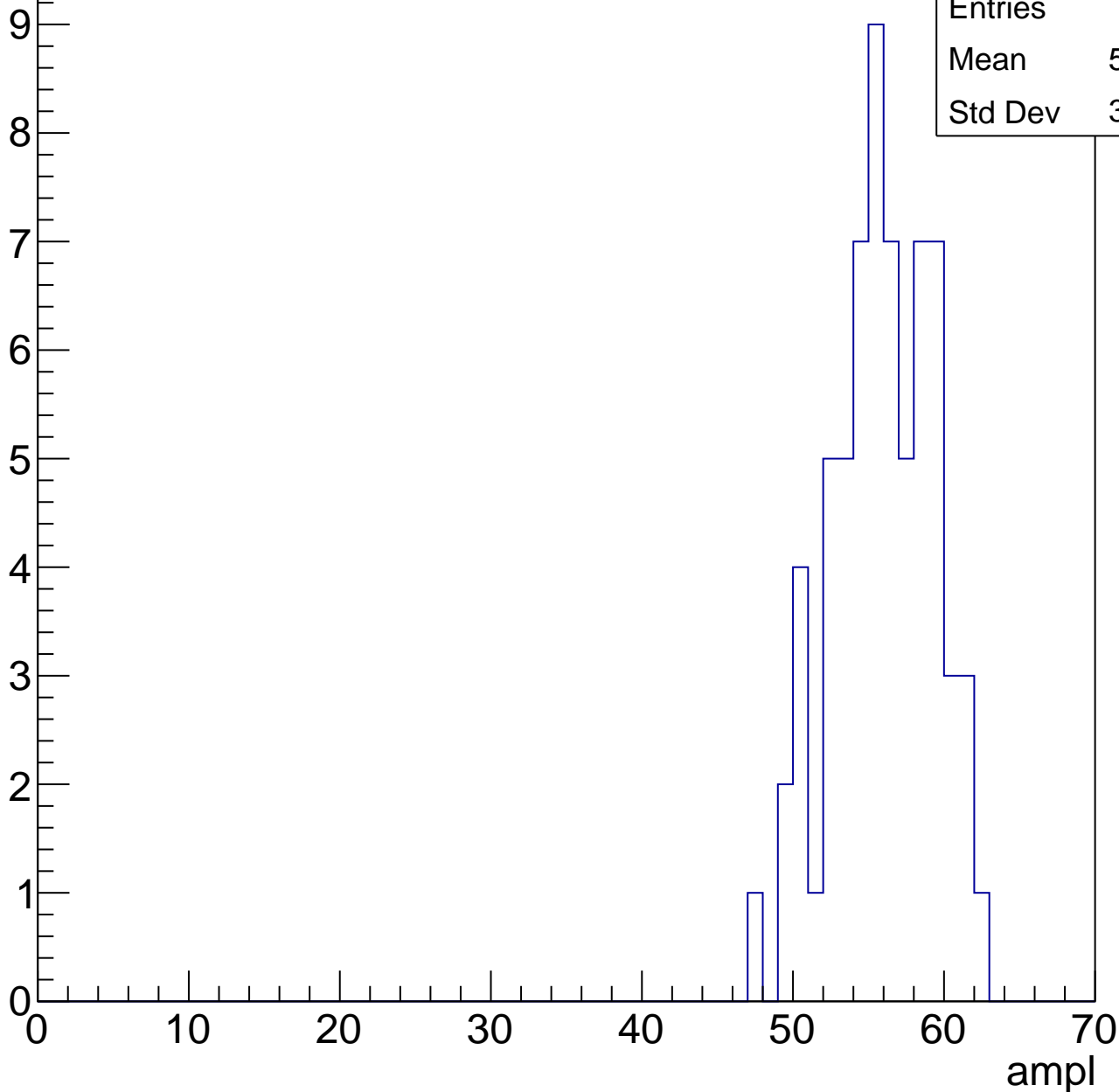


B1L103S, U9-ch55, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	55.45
Std Dev	3.334



B1L103S, U9-ch55, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

Entries 46

Mean 59.26

Std Dev 9.08

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

1

2

3

4

5

6

7

8

9

10

B1L103S, U9-ch55, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

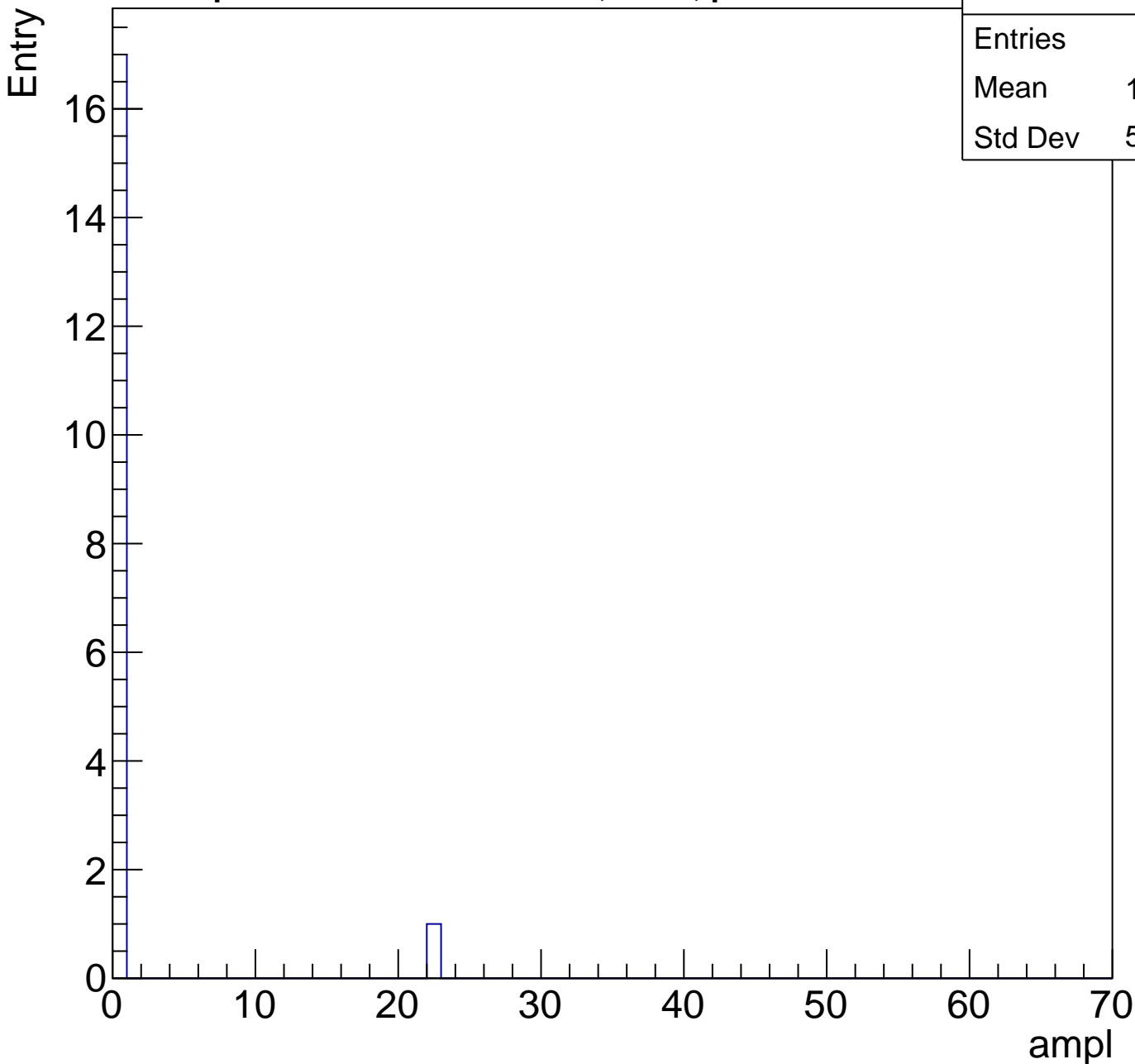


Entries	0
Mean	0
Std Dev	0

B1L103S, U9-ch55, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	18
Mean	1.222
Std Dev	5.039



B1L103S, U9-ch56, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	65
Mean	23.46
Std Dev	11.15

Entry

10

8

6

4

2

0

0

10

20

30

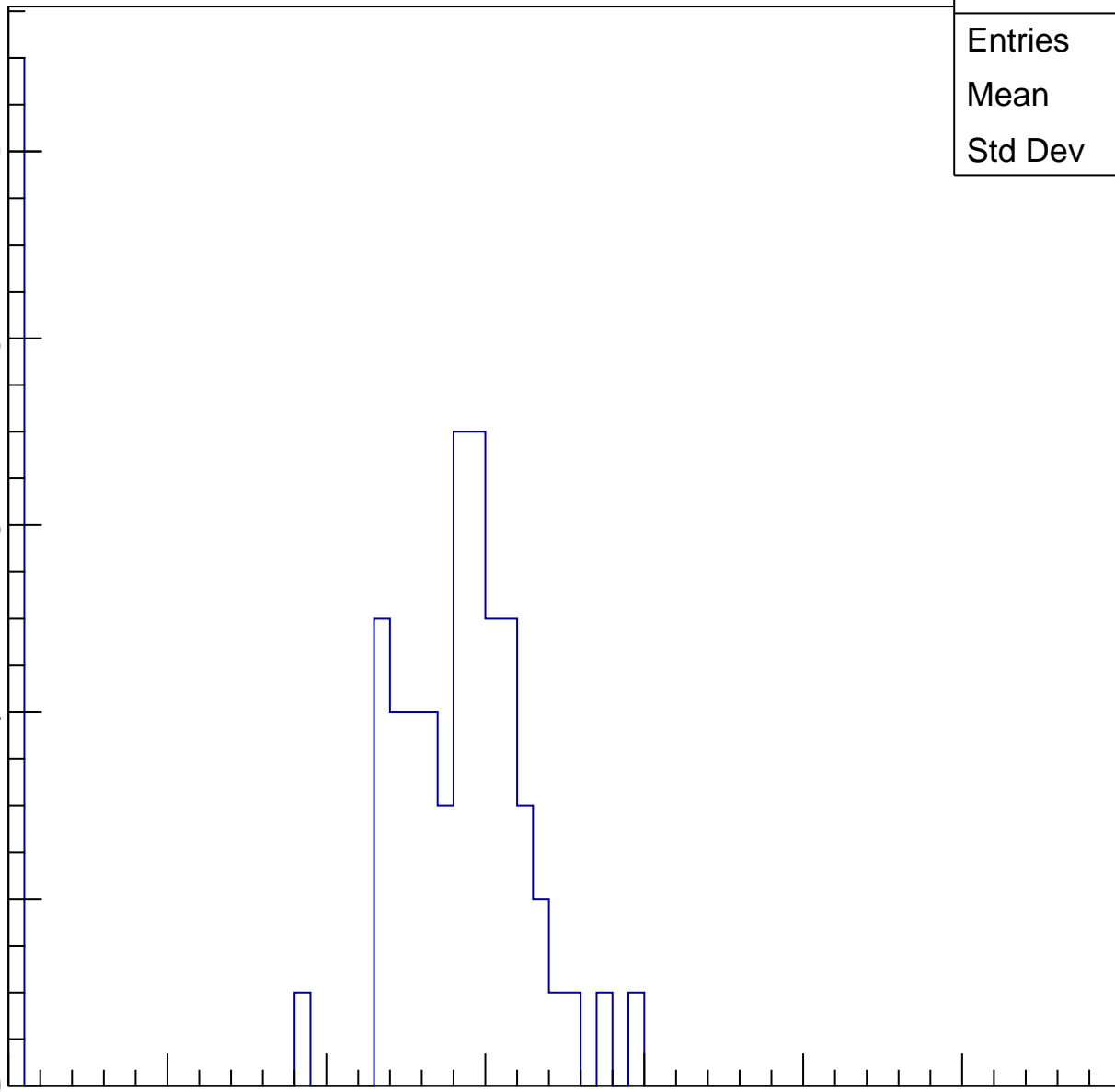
40

50

60

70

ampl

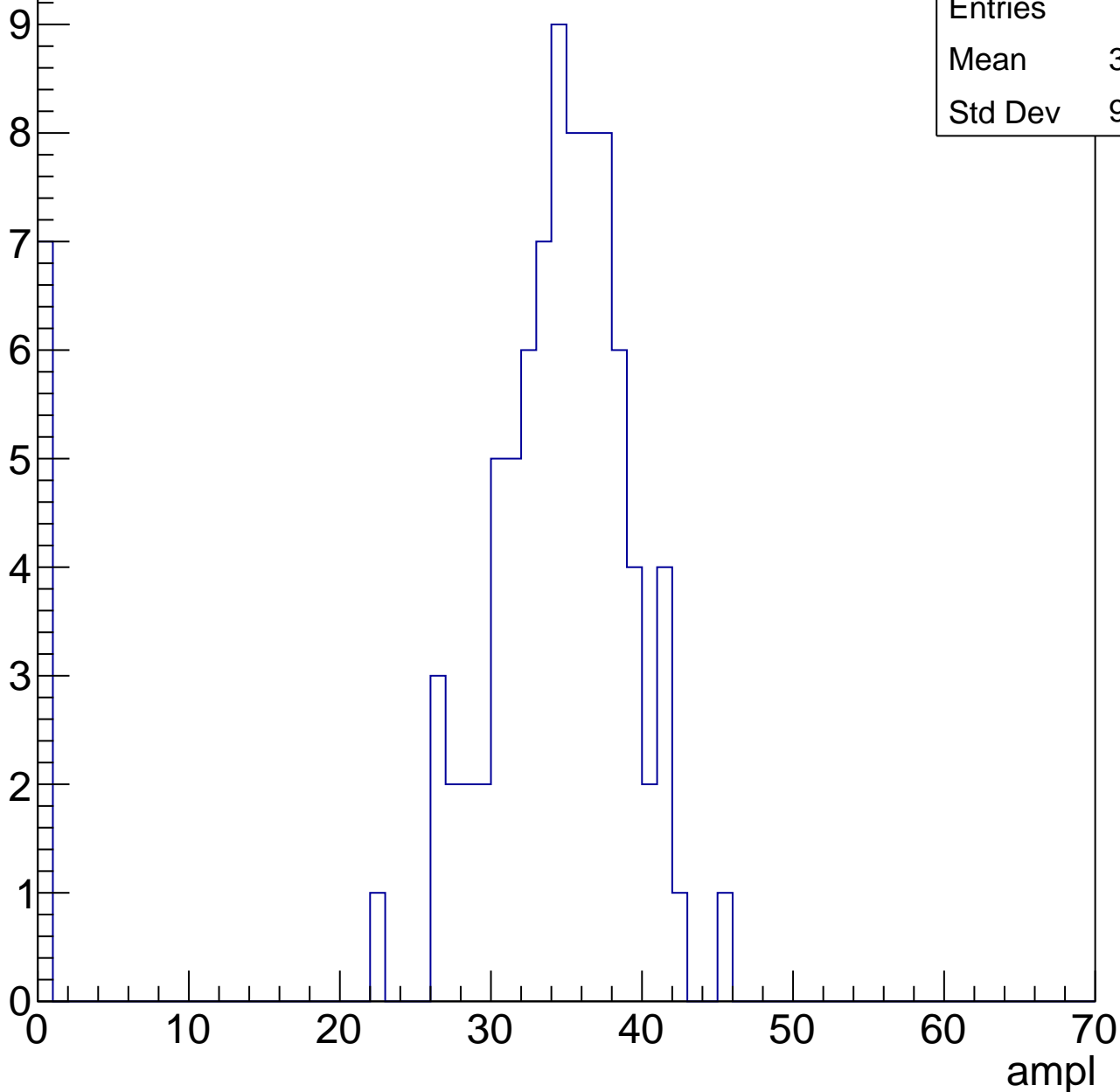


B1L103S, U9-ch56, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	91
Mean	31.66
Std Dev	9.982

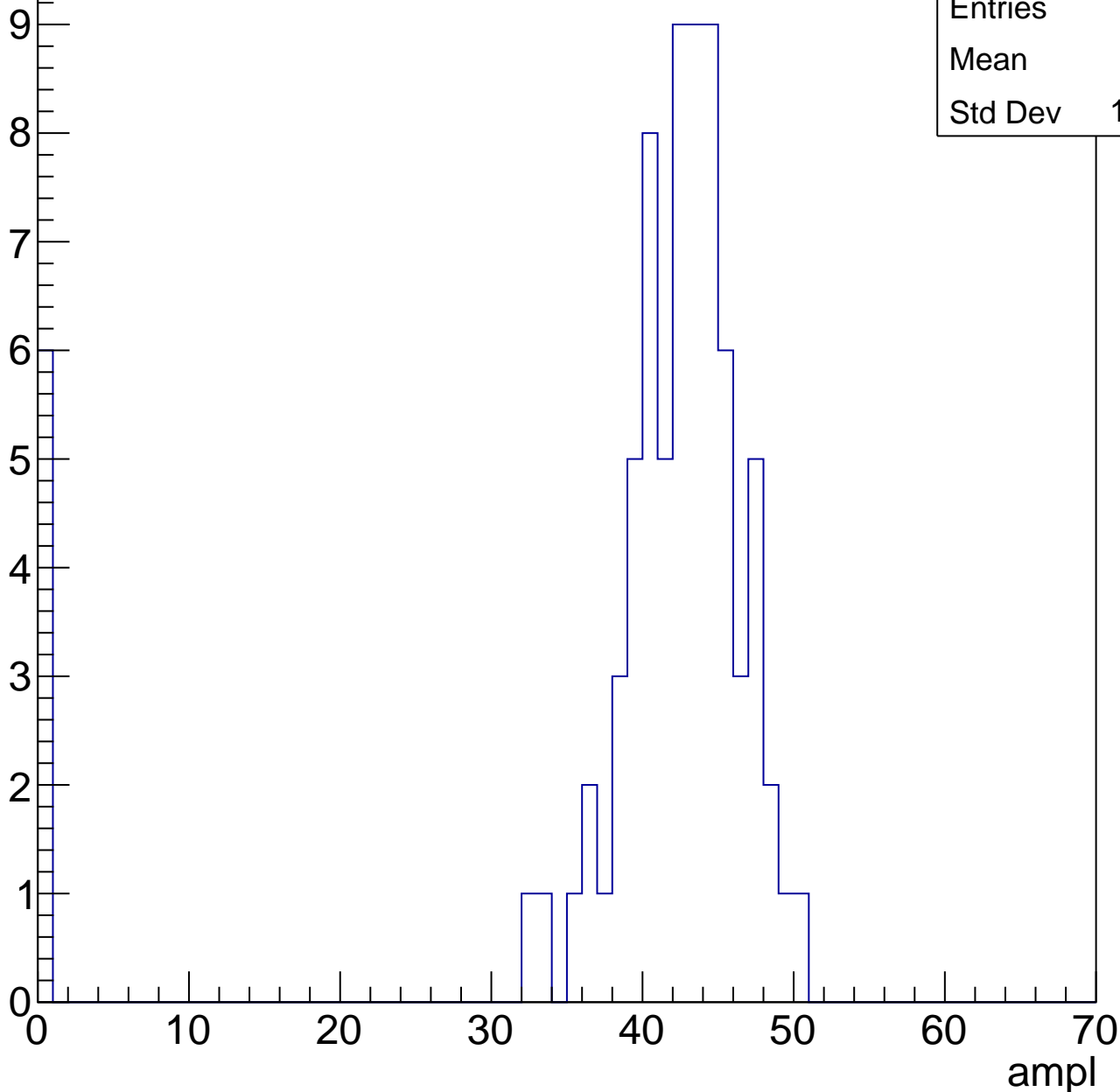


B1L103S, U9-ch56, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	39
Std Dev	11.76

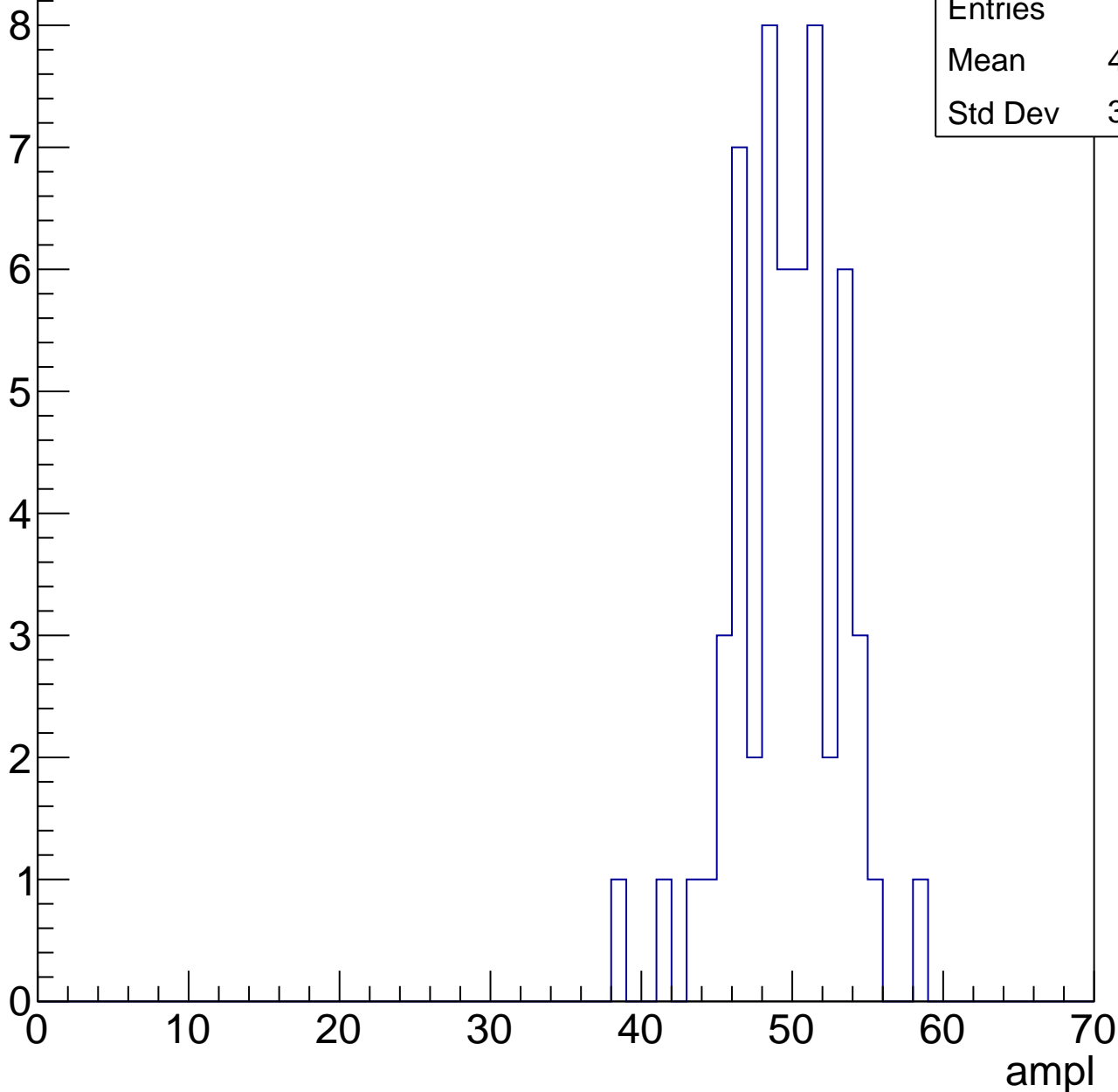


B1L103S, U9-ch56, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	49.12
Std Dev	3.545

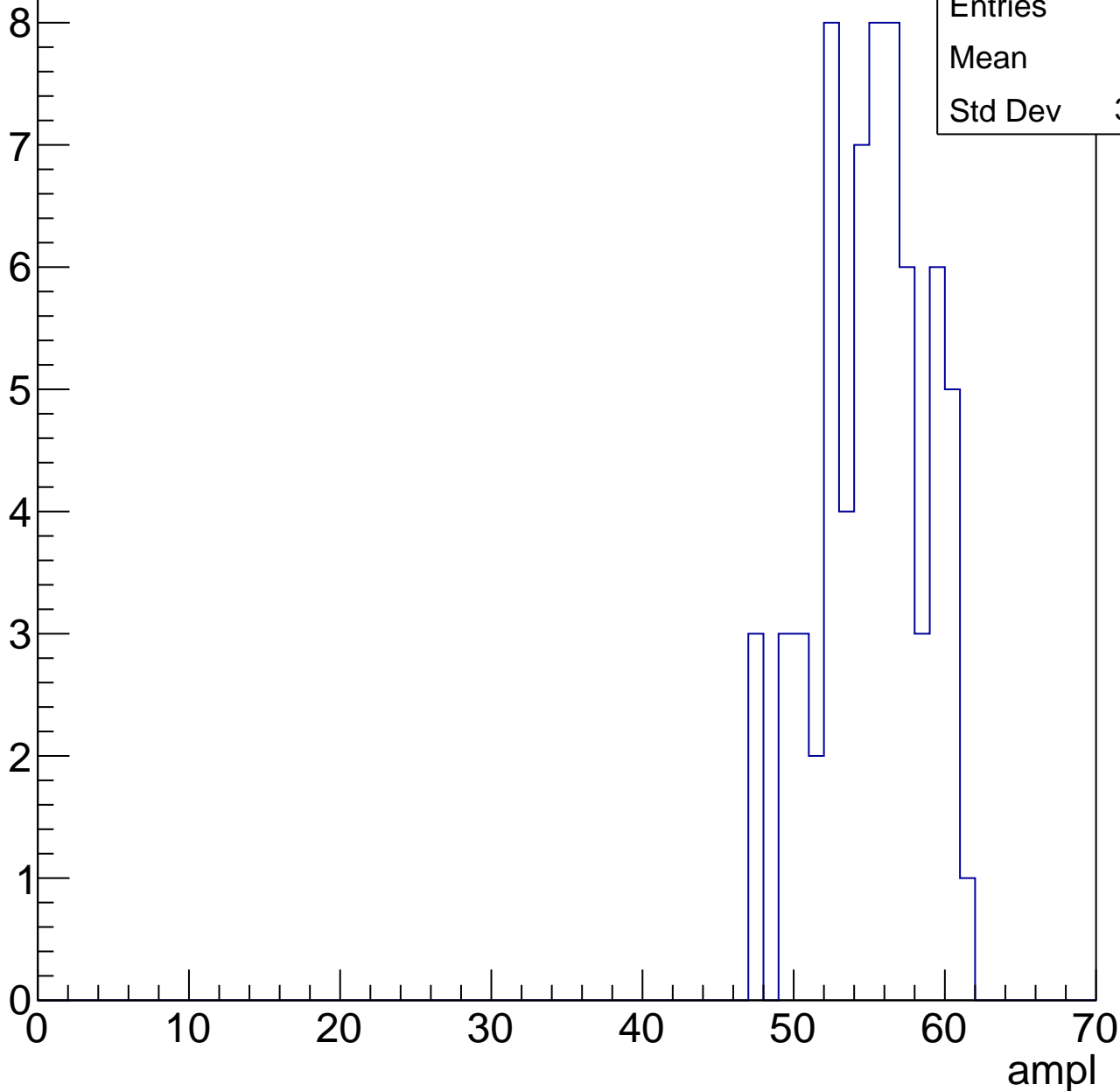


B1L103S, U9-ch56, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	54.7
Std Dev	3.481

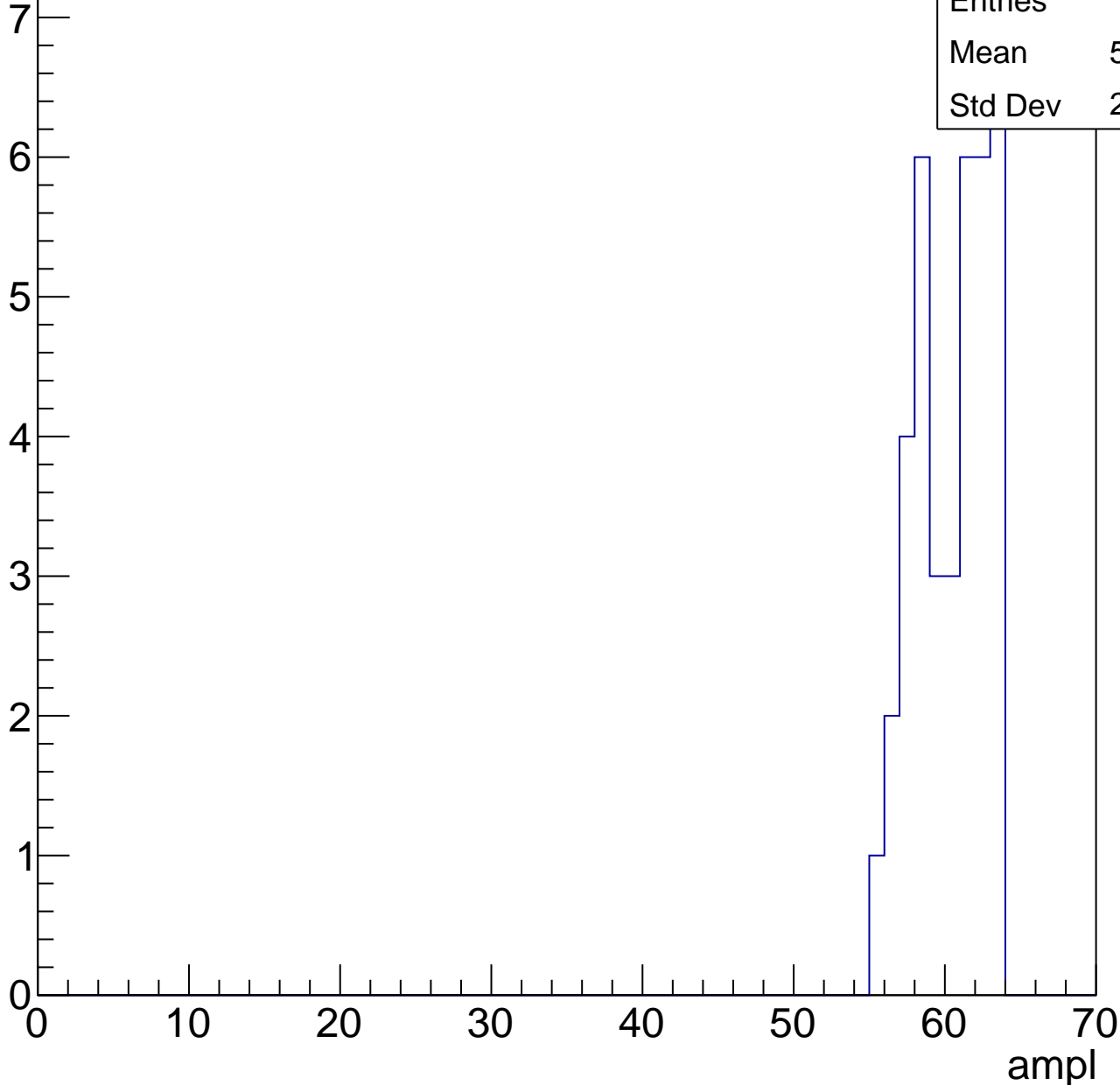


B1L103S, U9-ch56, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

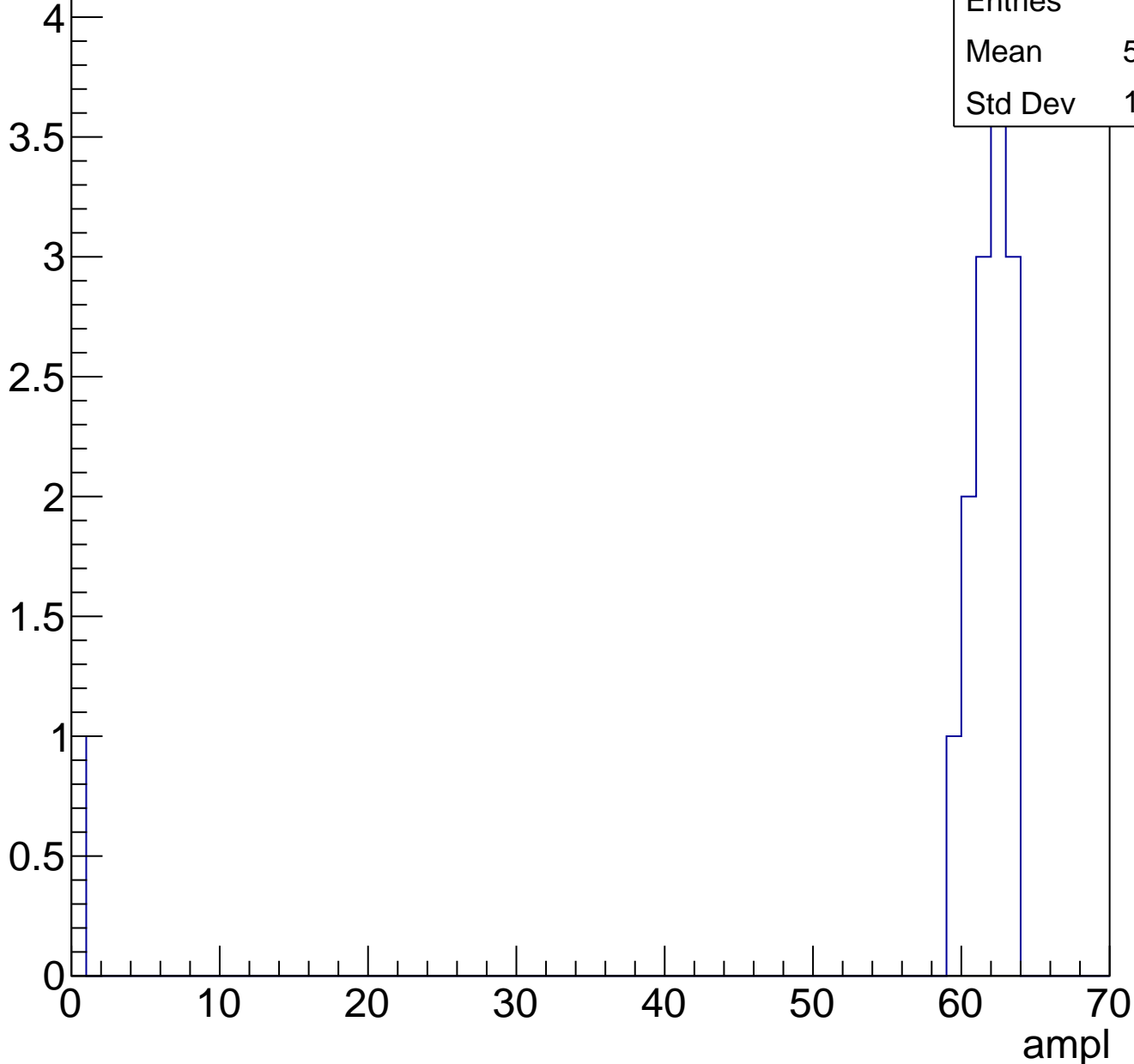
Entries	38
Mean	59.97
Std Dev	2.367



B1L103S, U9-ch56, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch56, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



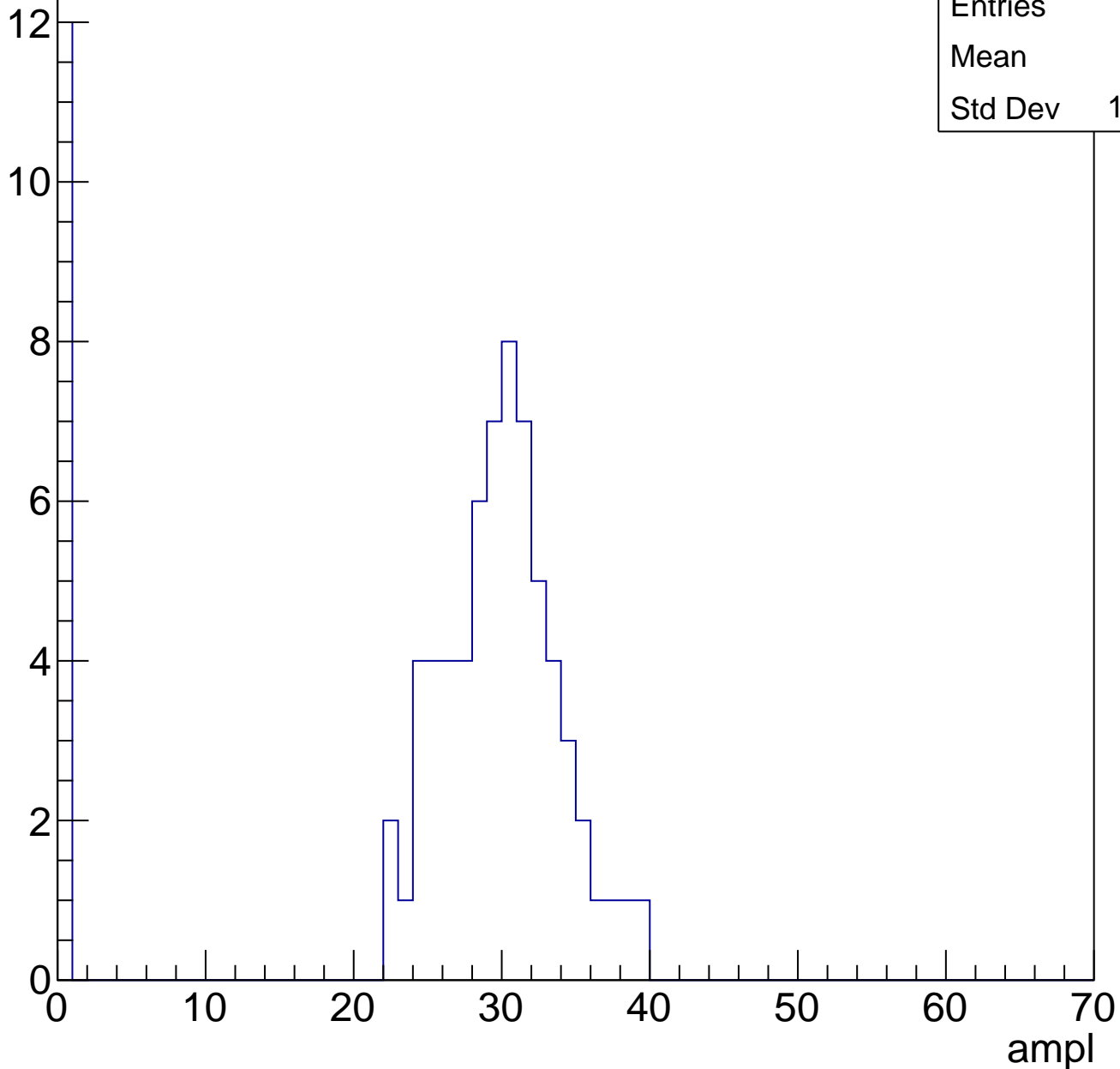
Entries	19
Mean	0
Std Dev	0

B1L103S, U9-ch57, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	77
Mean	24.9
Std Dev	11.25

Entry

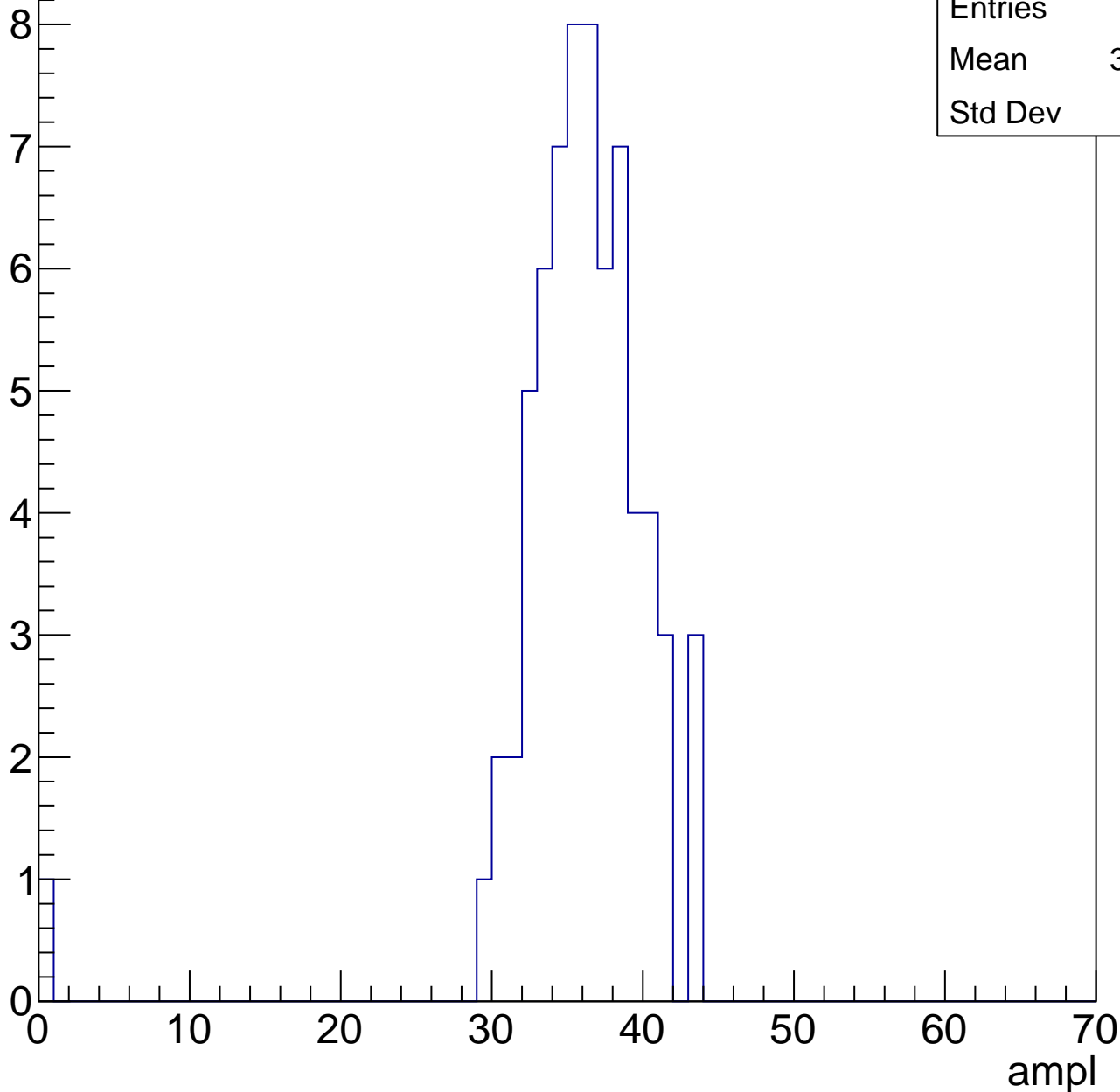


B1L103S, U9-ch57, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	35.39
Std Dev	5.42

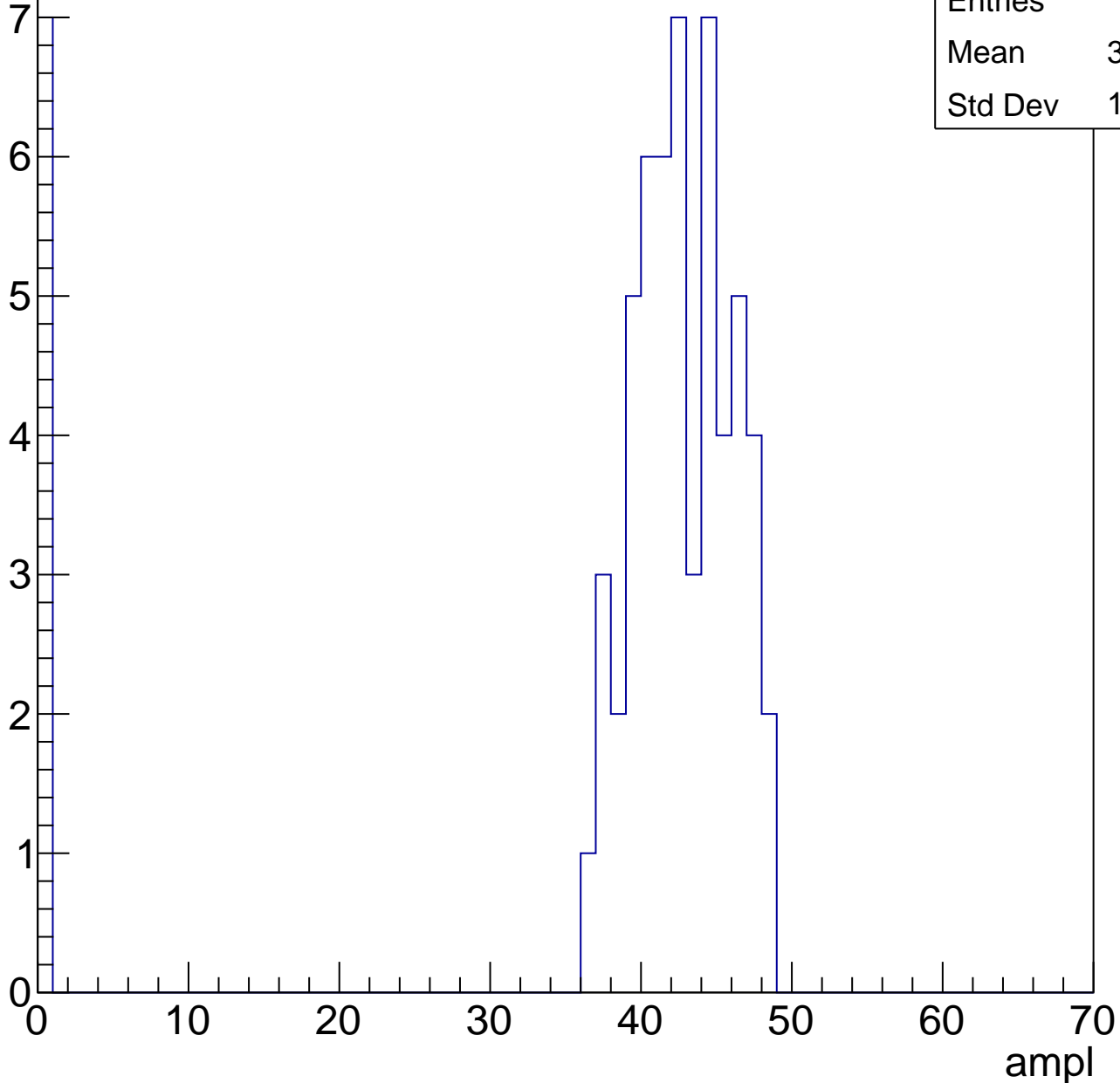


B1L103S, U9-ch57, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	37.56
Std Dev	13.72

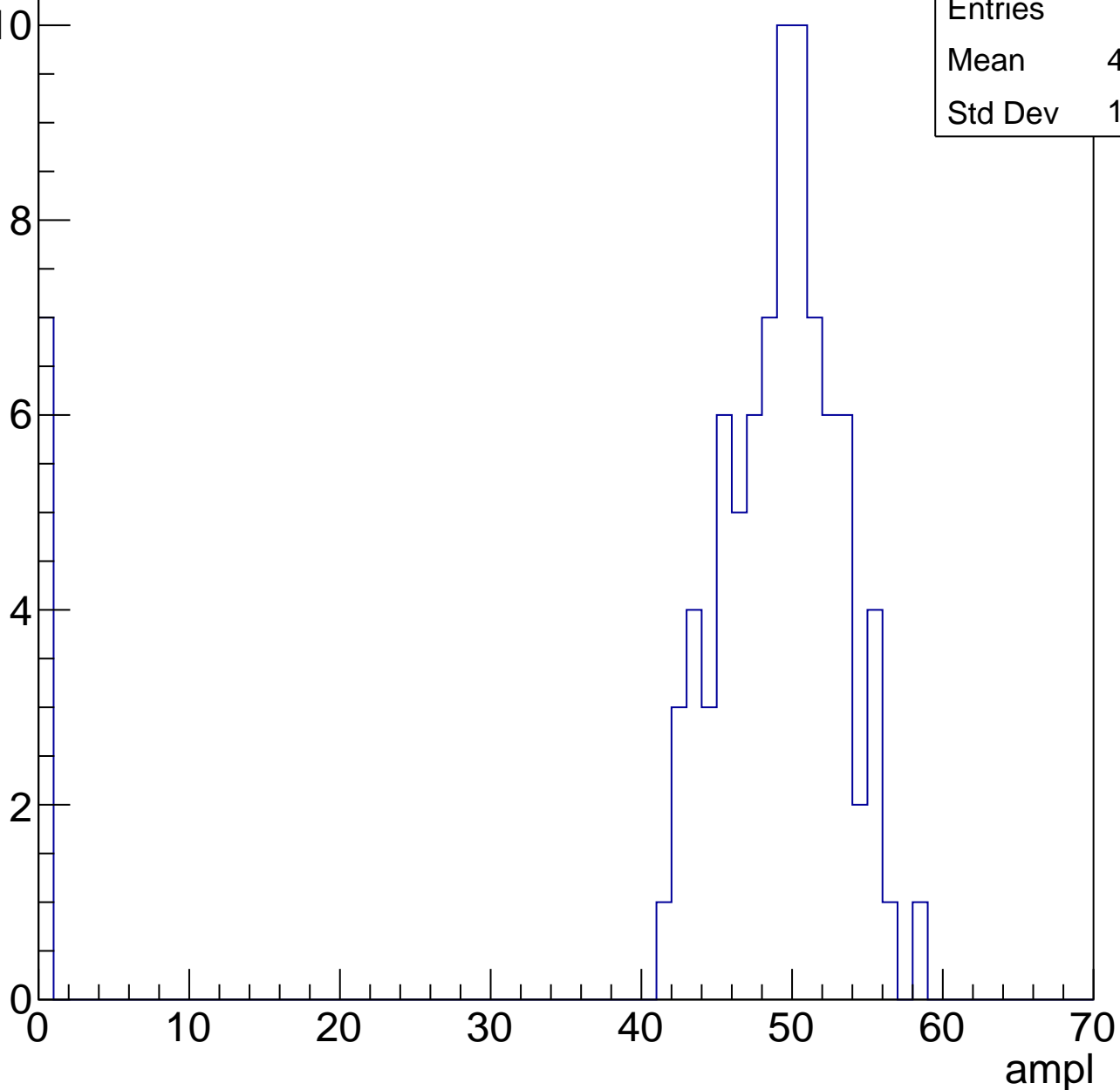


B1L103S, U9-ch57, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	89
Mean	45.03
Std Dev	13.62



B1L103S, U9-ch57, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

Entries 71

Mean 56.51

Std Dev 3.135

8

6

4

2

0

0

10

20

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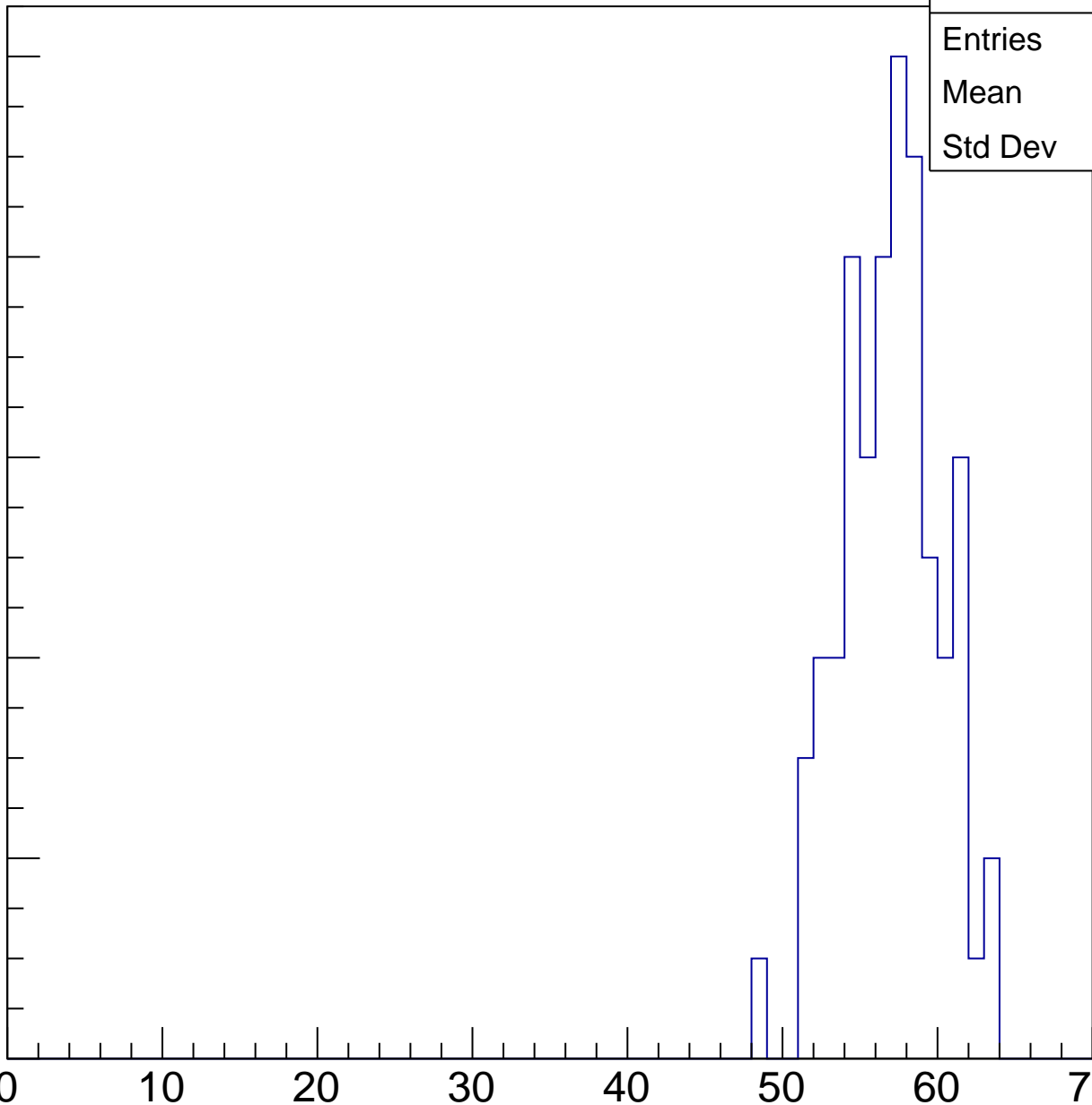
40

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70

ampl



B1L103S, U9-ch57, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

6

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4

3

2

1

0

Entries

27

Mean

58.7

Std Dev

11.64

0

10

20

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60

ampl

0

1

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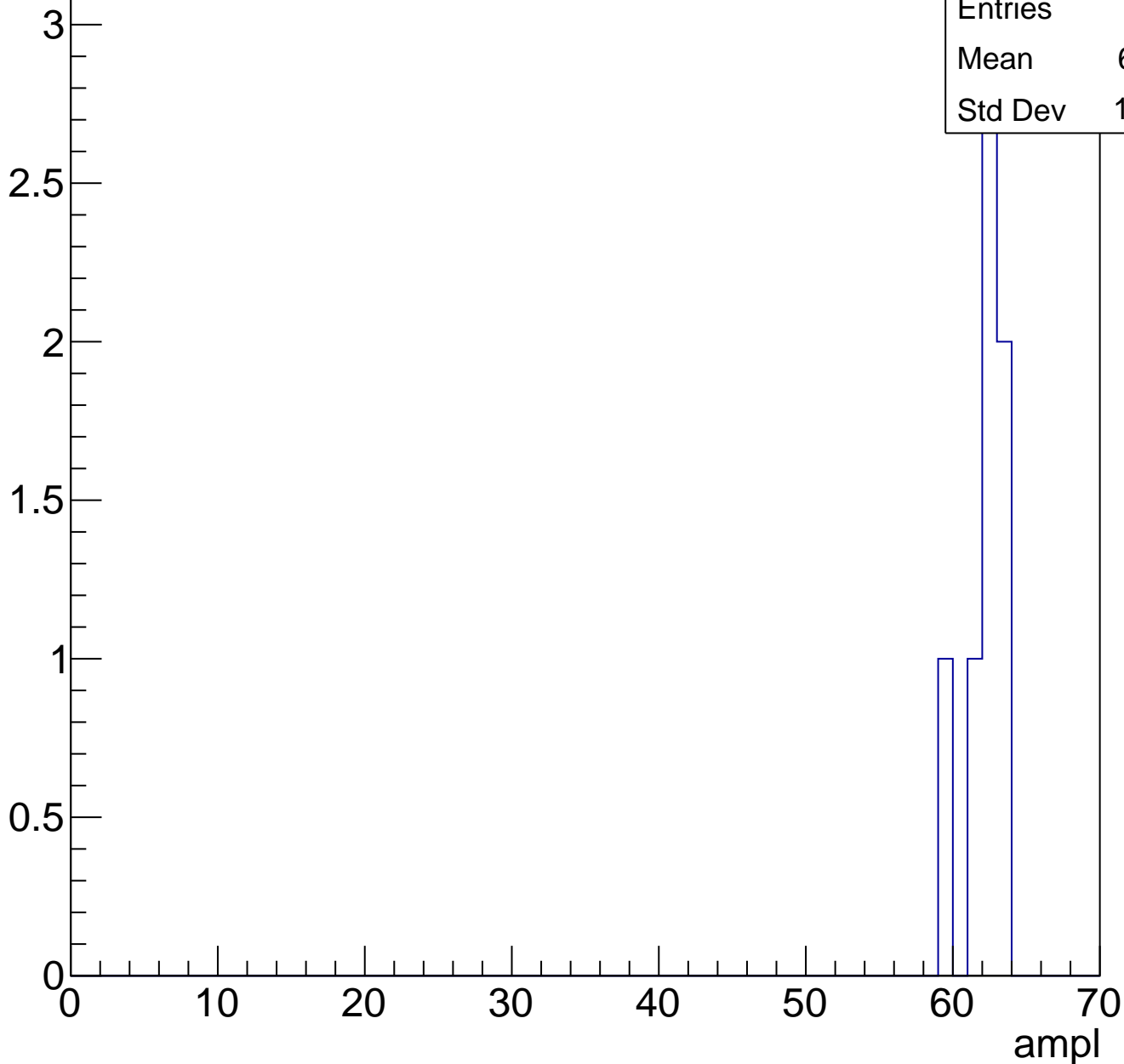
340

341

B1L103S, U9-ch57, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch57, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U9-ch58, adc0

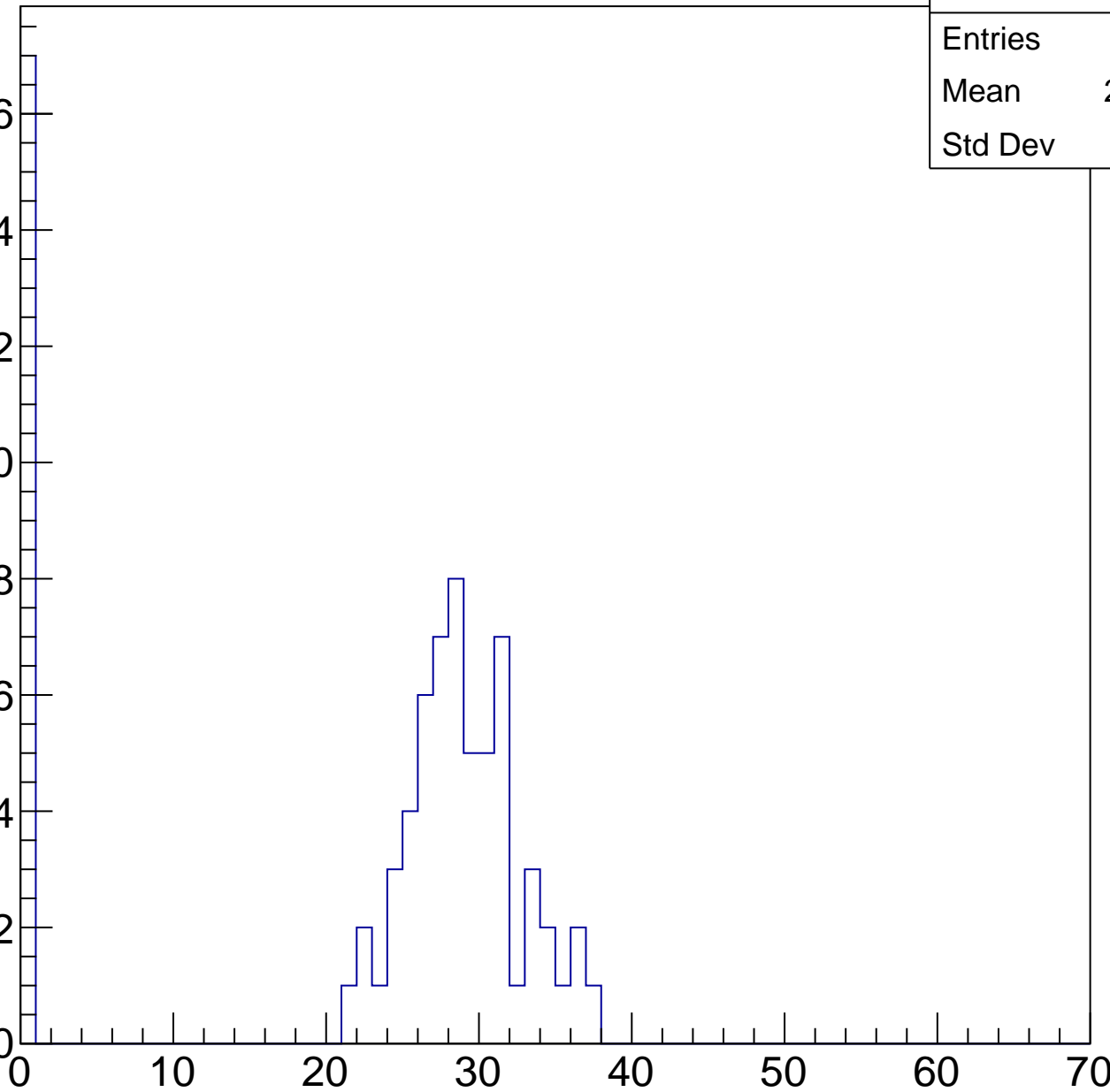
calib_packv5_041523_1651.root, FC#0, port C2

Entries	76
Mean	22.16
Std Dev	12.3

Entry

16
14
12
10
8
6
4
2
0

ampl

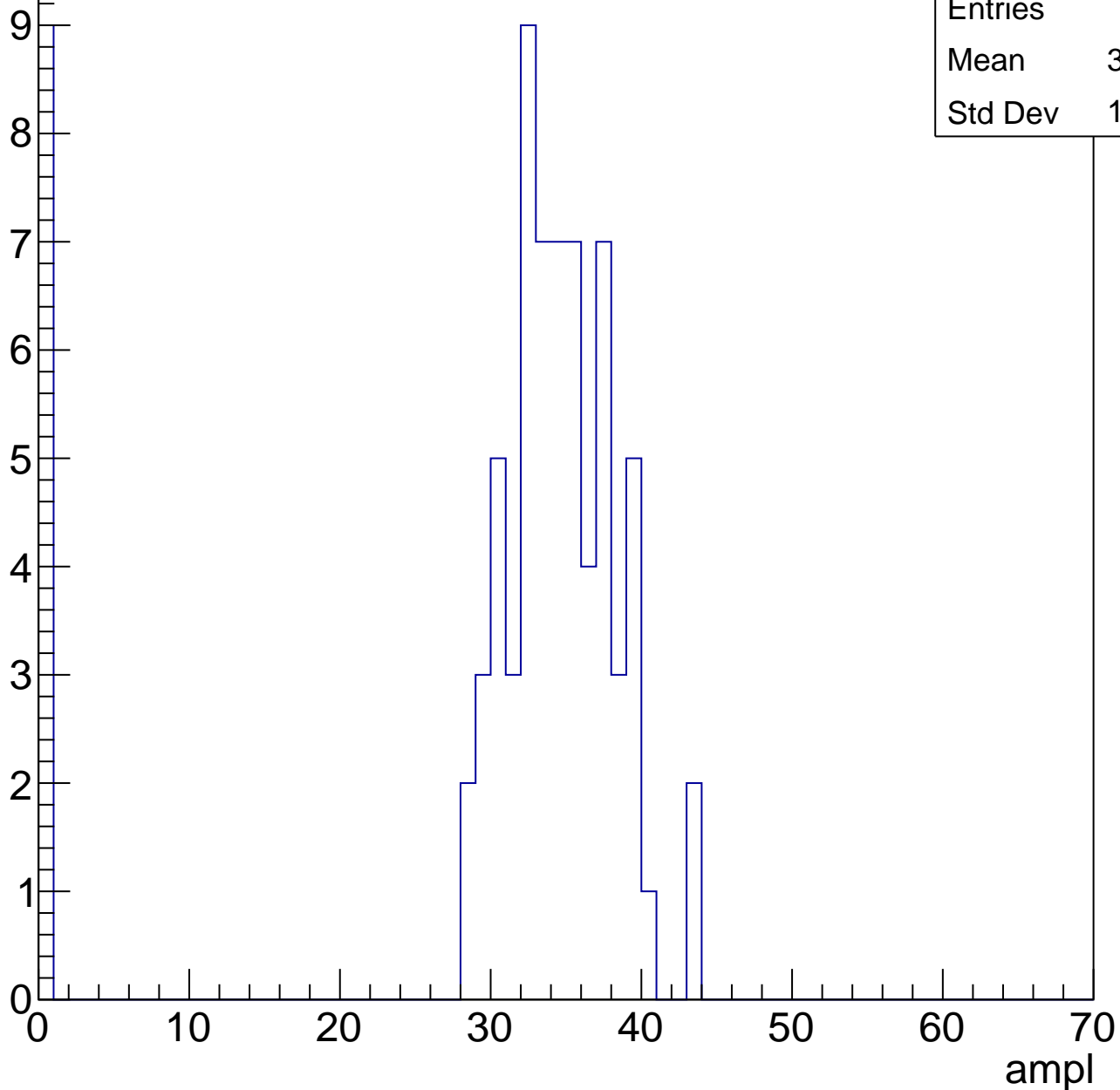


B1L103S, U9-ch58, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	30.08
Std Dev	11.64

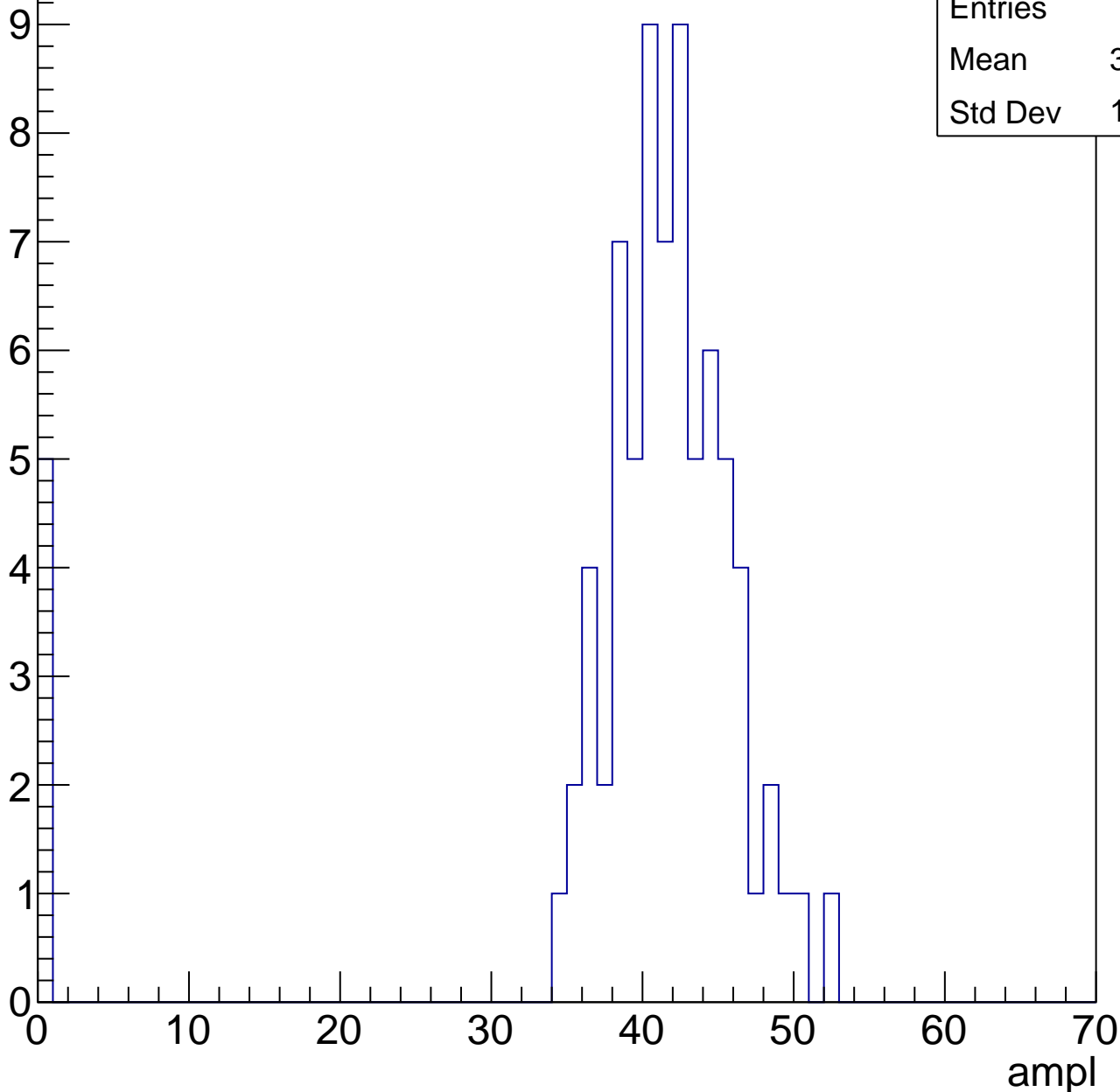


B1L103S, U9-ch58, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	38.83
Std Dev	10.84

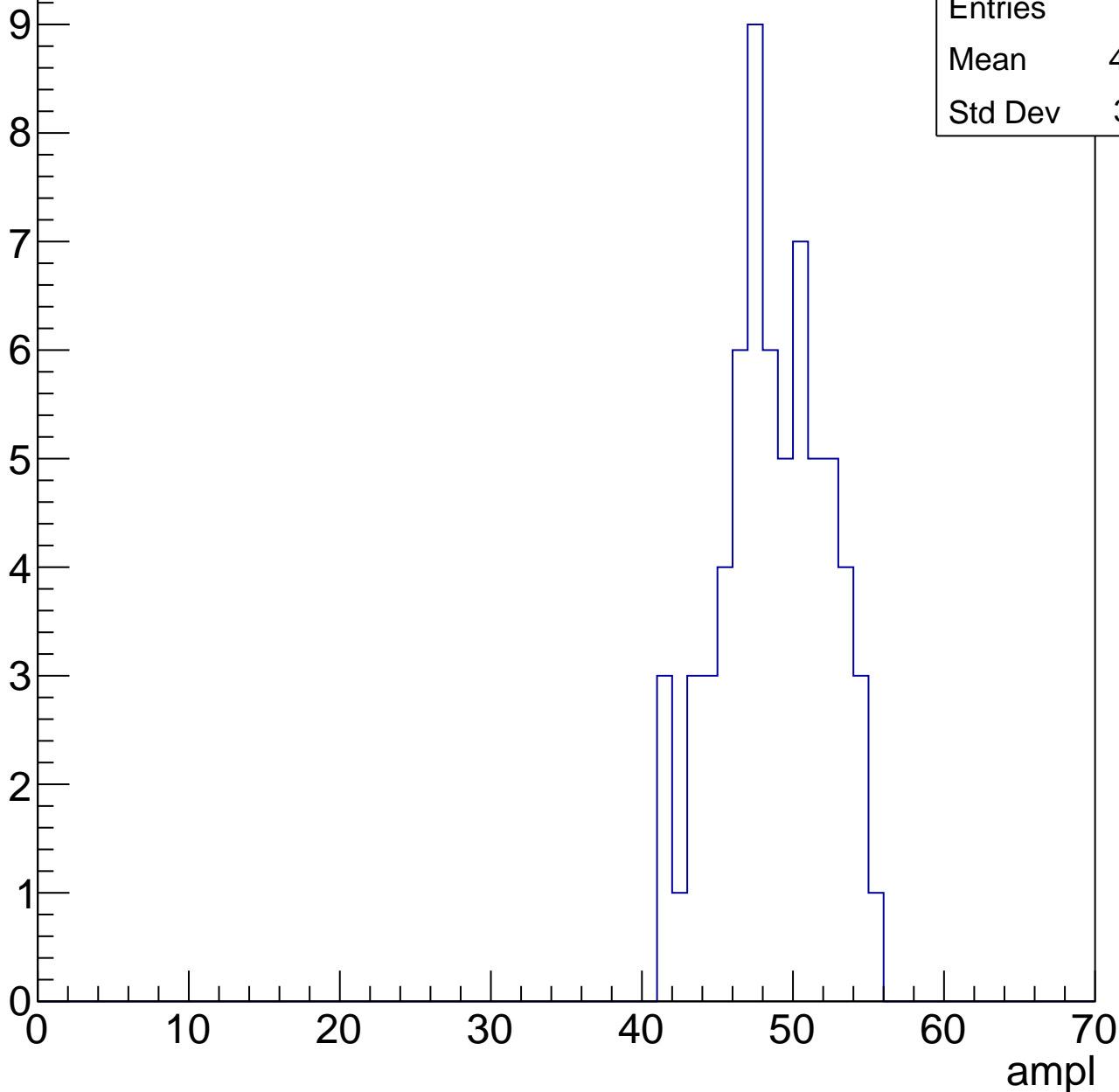


B1L103S, U9-ch58, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	48.18
Std Dev	3.481

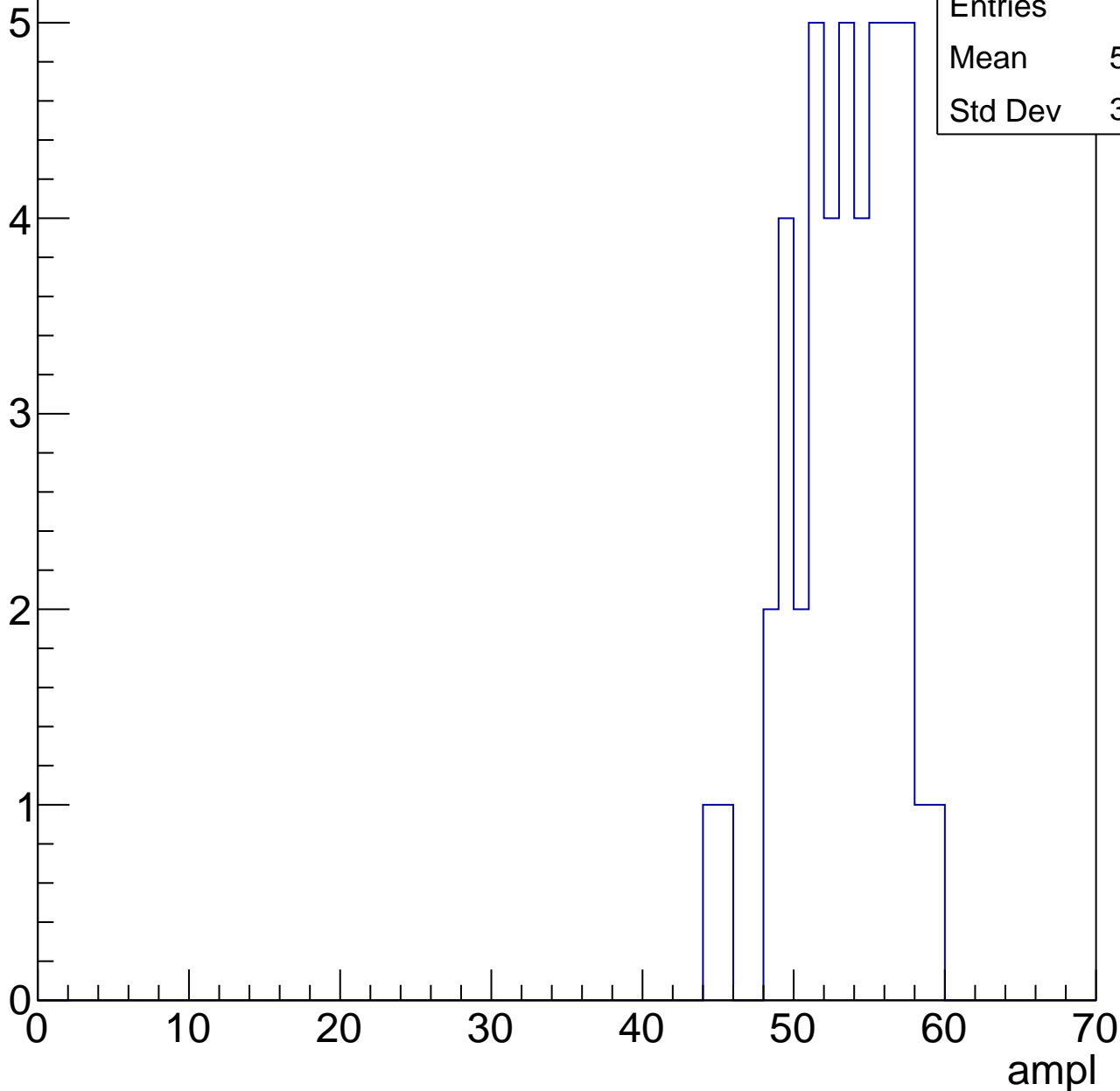


B1L103S, U9-ch58, adc4

calib_packv5_041523_1651.root, FC#0, port C2

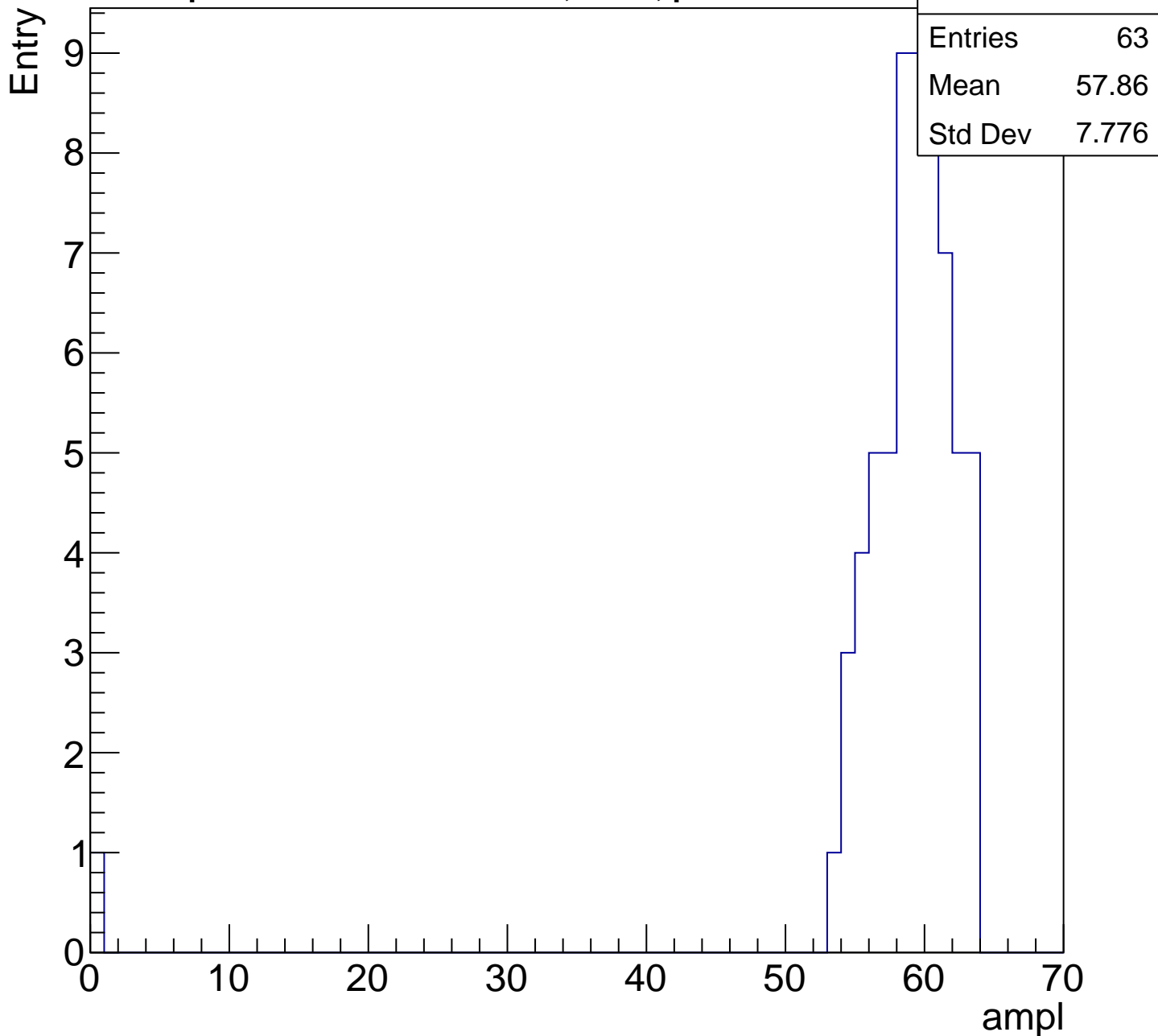
Entry

Entries	45
Mean	52.93
Std Dev	3.369



B1L103S, U9-ch58, adc5

calib_packv5_041523_1651.root, FC#0, port C2

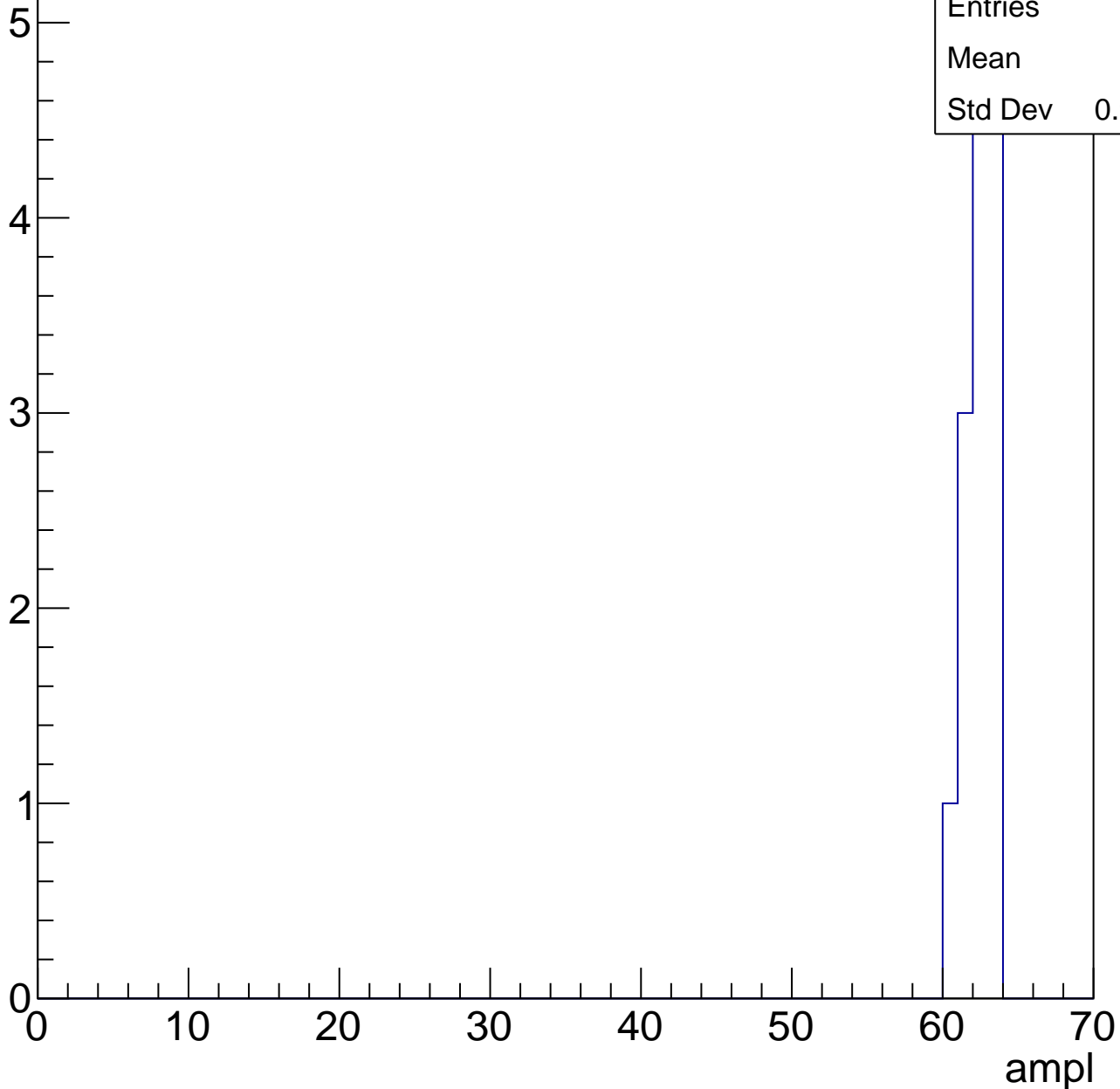


B1L103S, U9-ch58, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	14
Mean	62
Std Dev	0.9258



B1L103S, U9-ch58, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

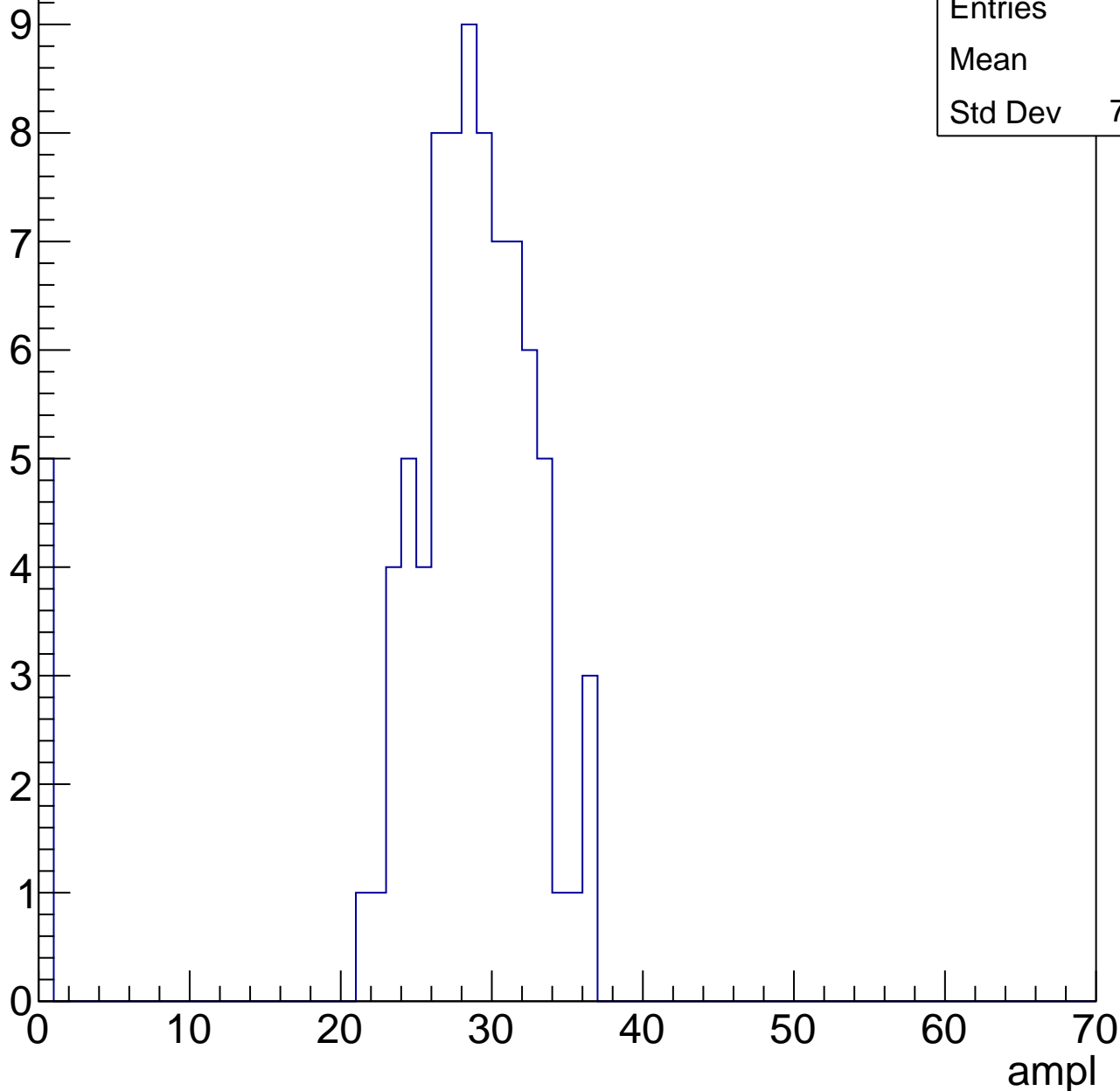


B1L103S, U9-ch59, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	83
Mean	26.8
Std Dev	7.555

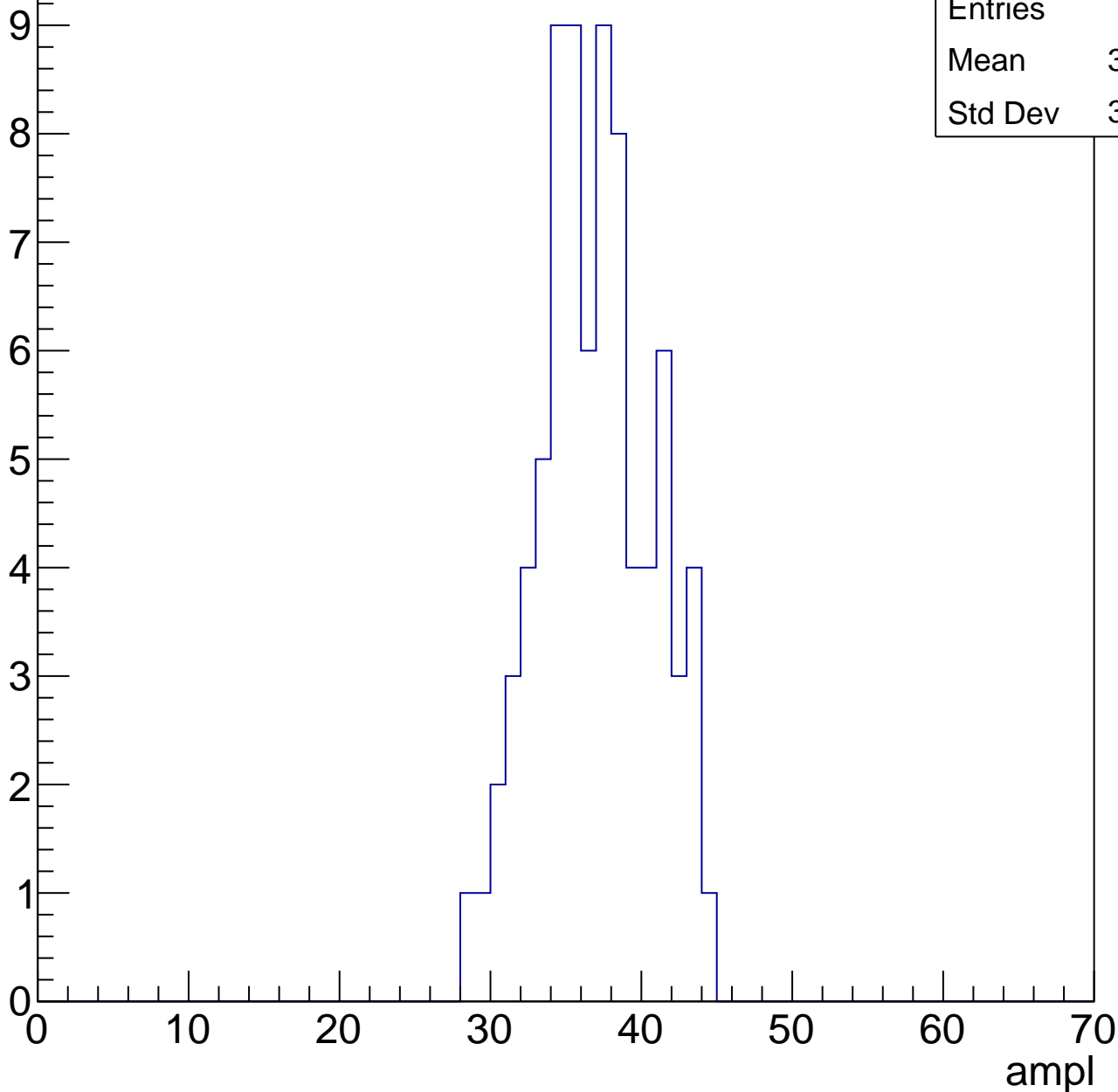


B1L103S, U9-ch59, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	79
Mean	36.47
Std Dev	3.656

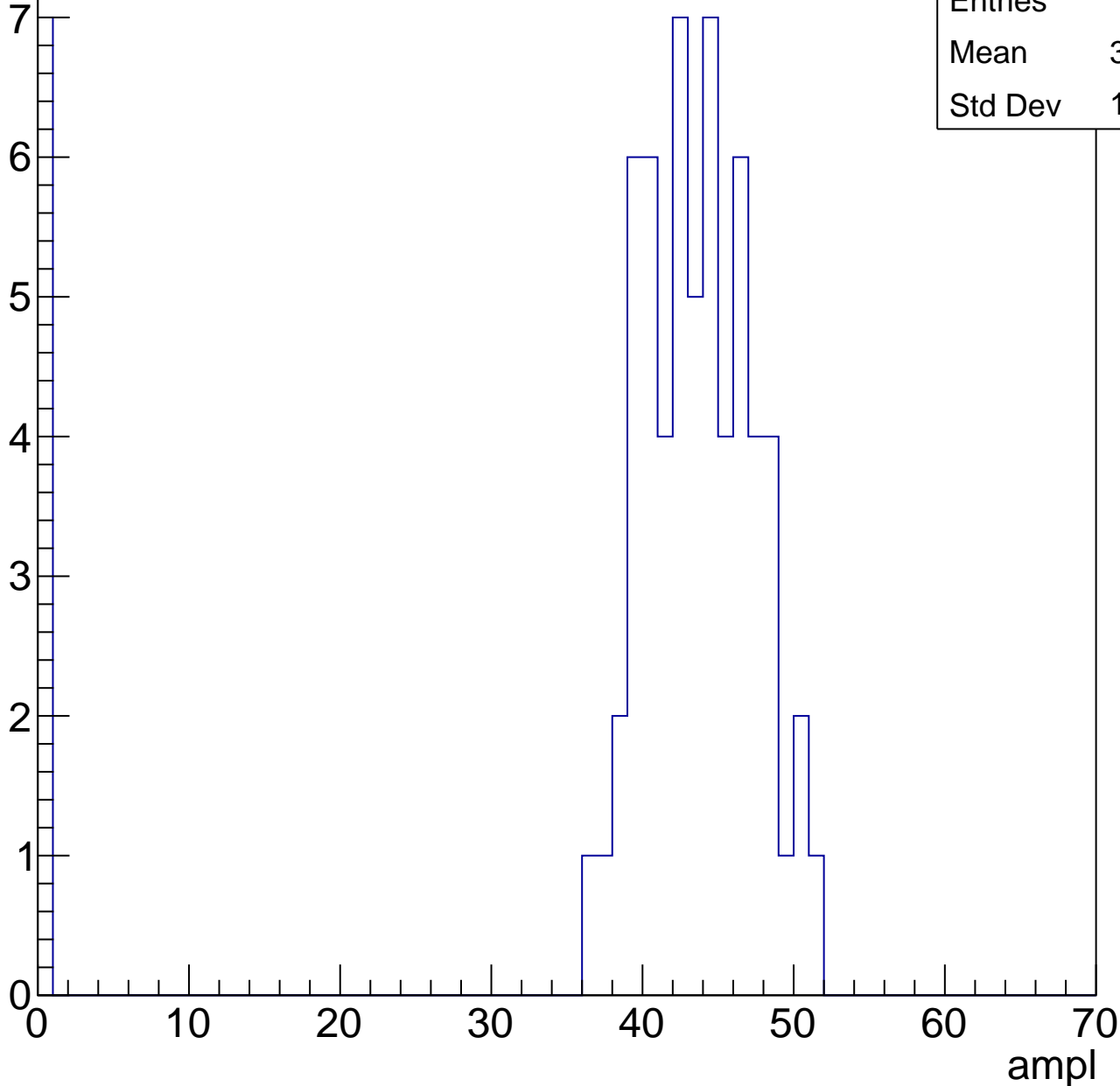


B1L103S, U9-ch59, adc2

calib_packv5_041523_1651.root, FC#0, port C2

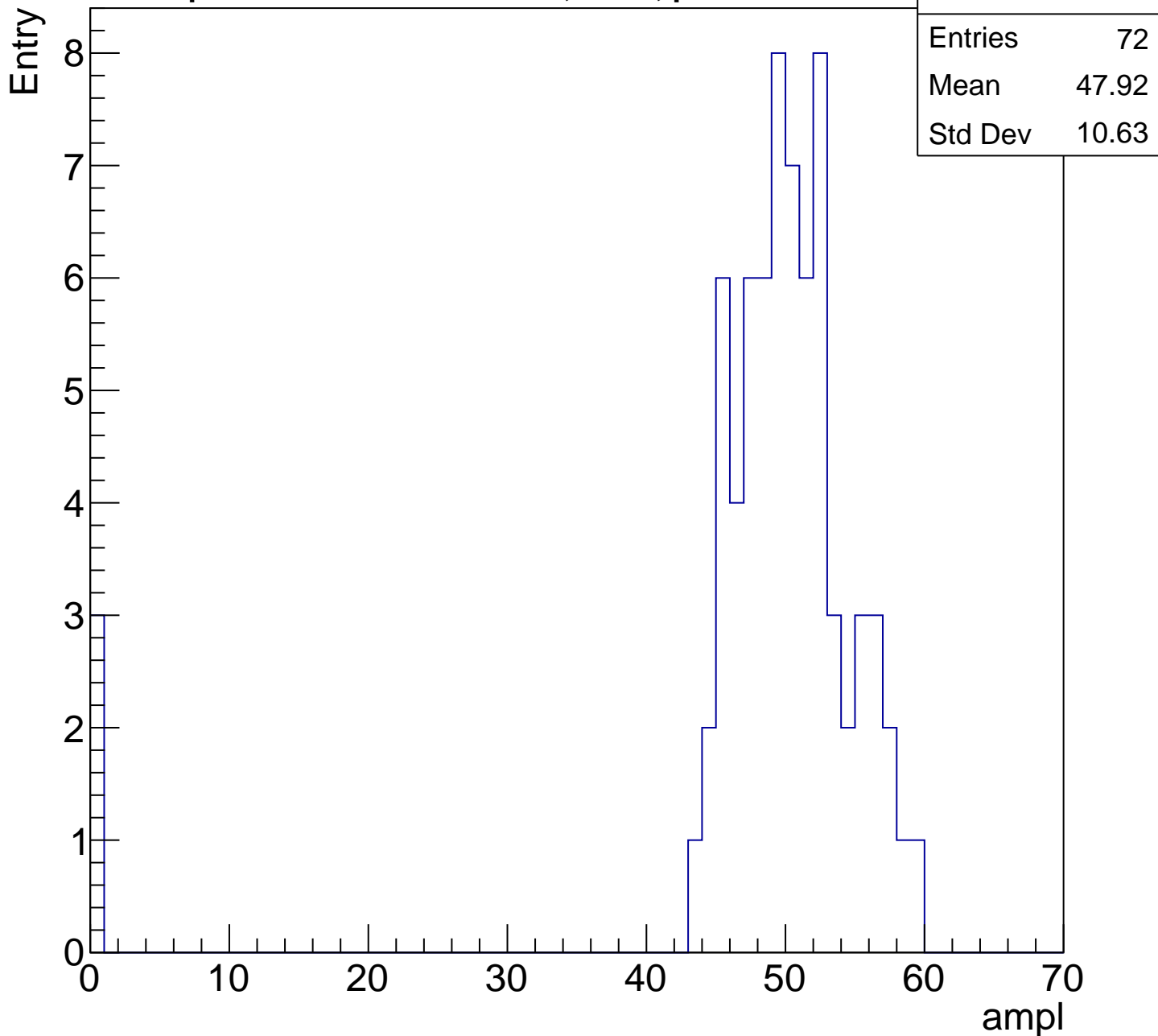
Entry

Entries	68
Mean	38.82
Std Dev	13.56



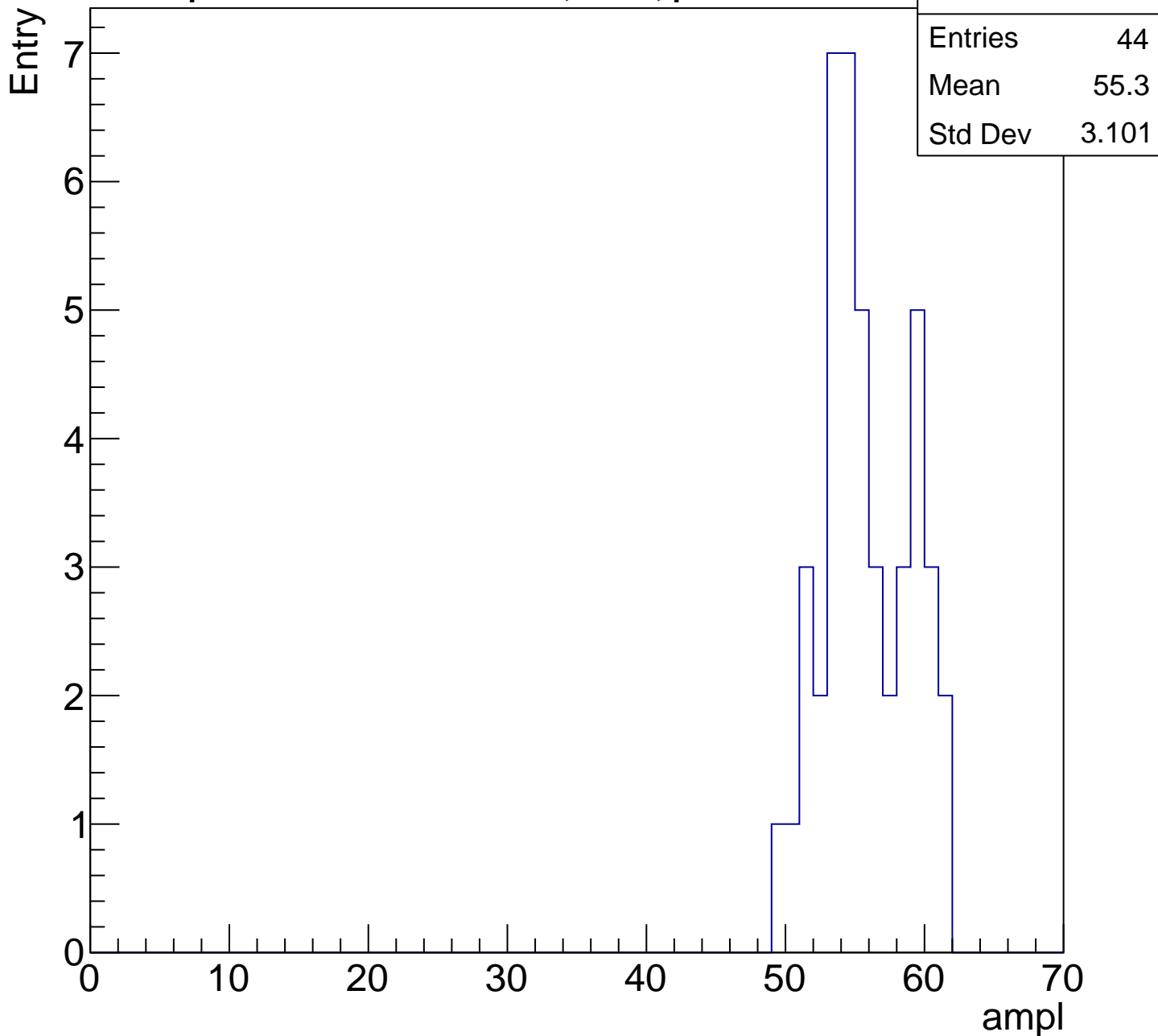
B1L103S, U9-ch59, adc3

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U9-ch59, adc4

calib_packv5_041523_1651.root, FC#0, port C2

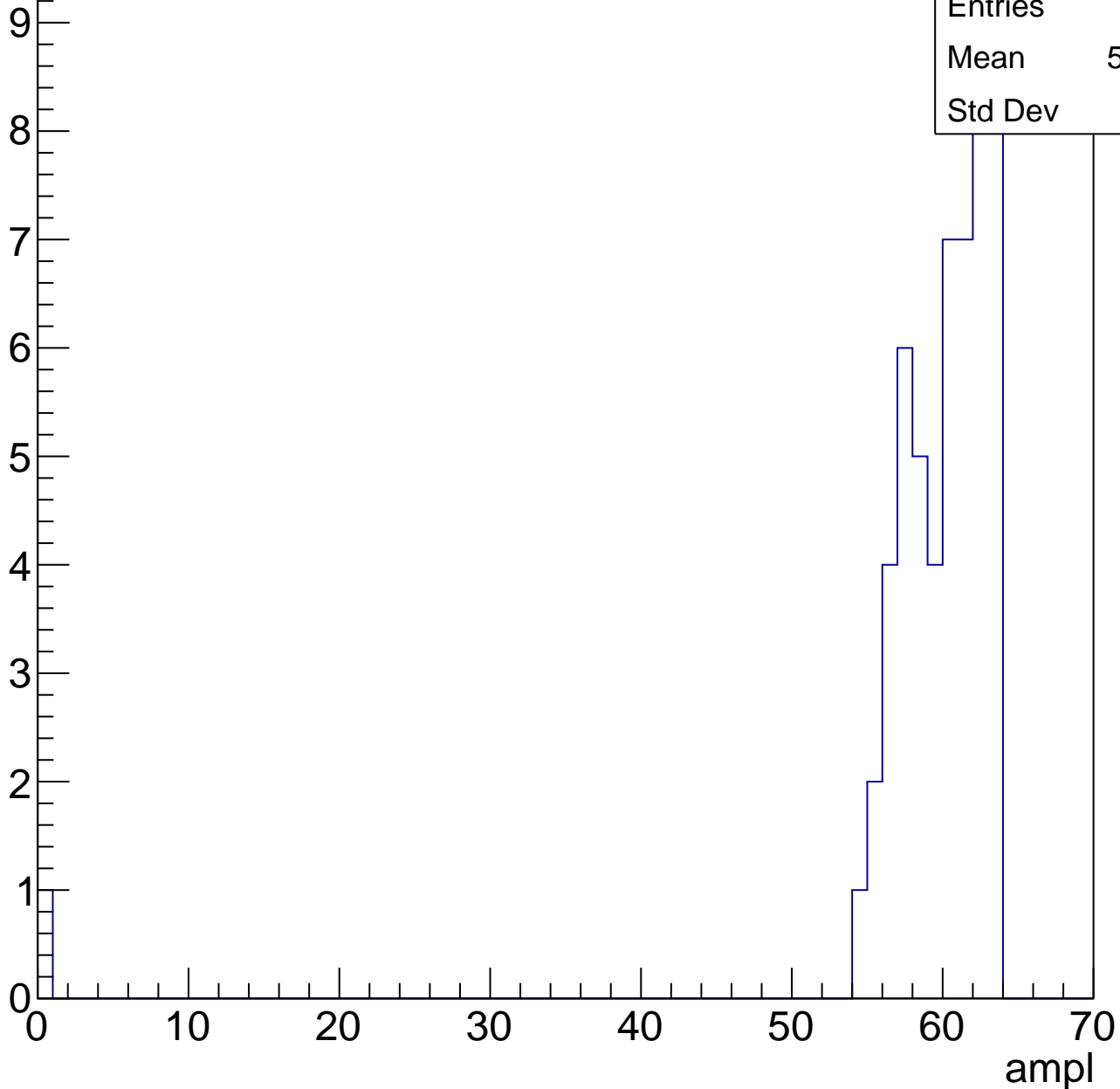


B1L103S, U9-ch59, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

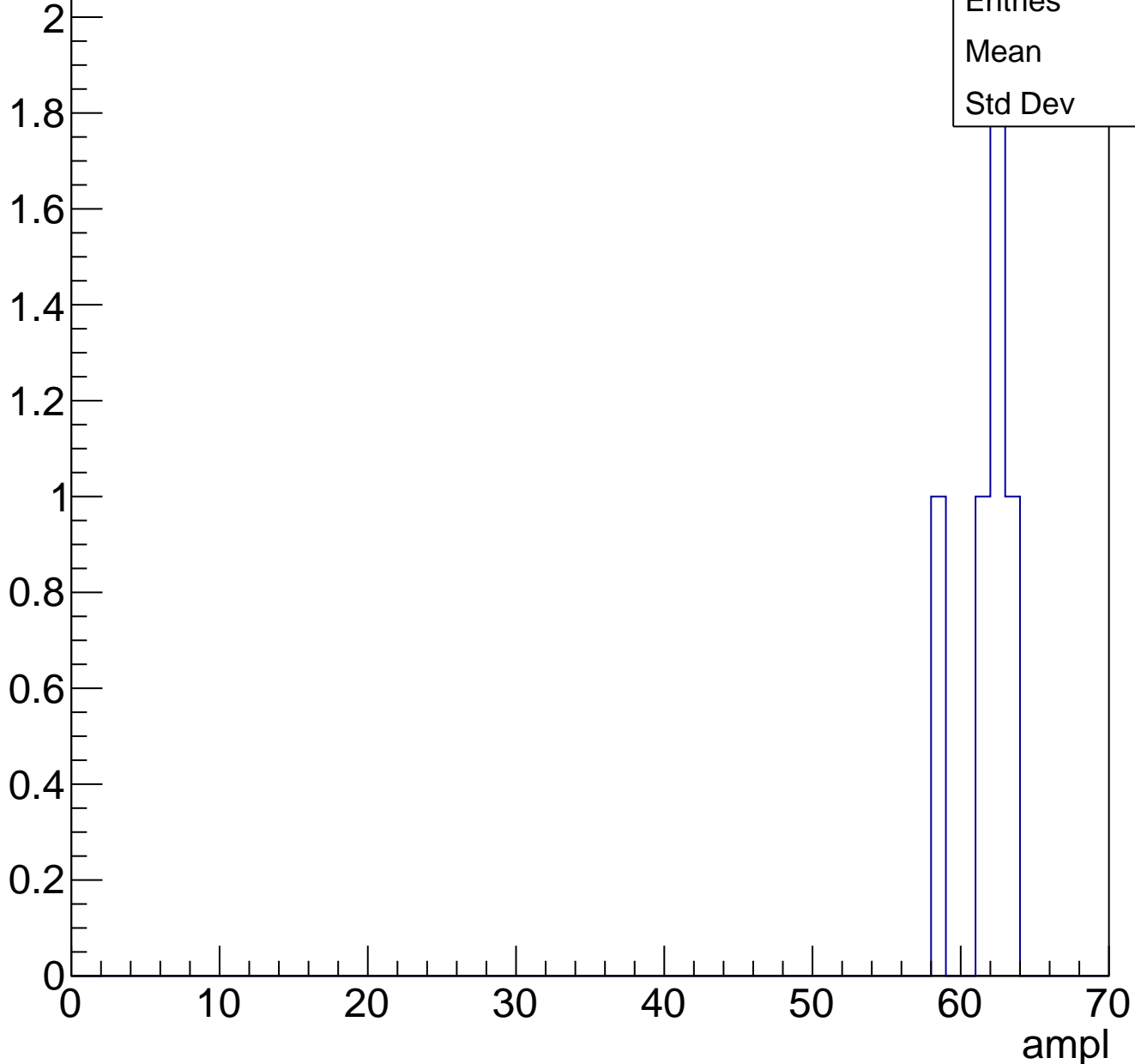
Entries	54
Mean	58.63
Std Dev	8.44



B1L103S, U9-ch59, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch59, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

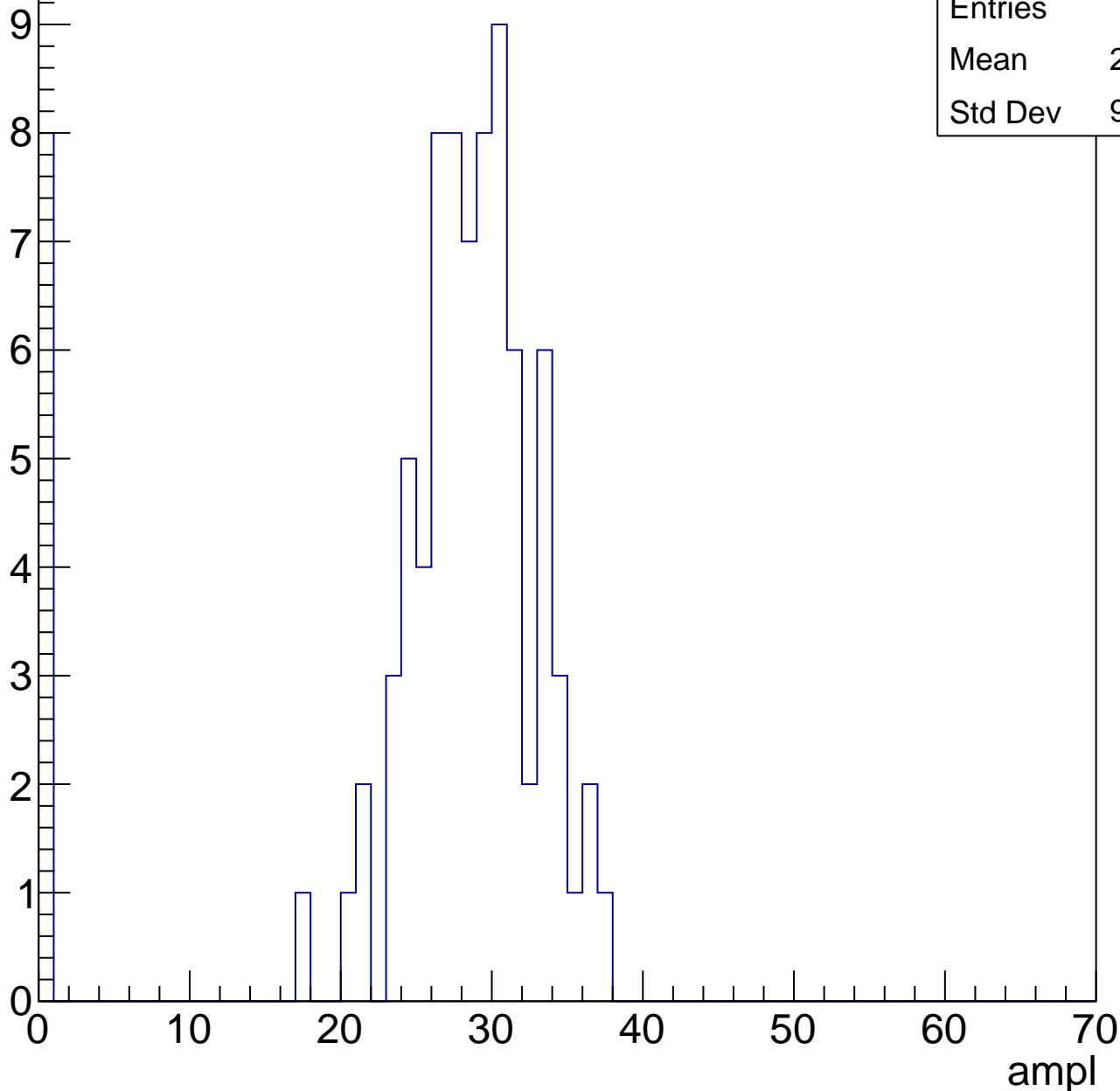


B1L103S, U9-ch60, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	85
Mean	25.69
Std Dev	9.062

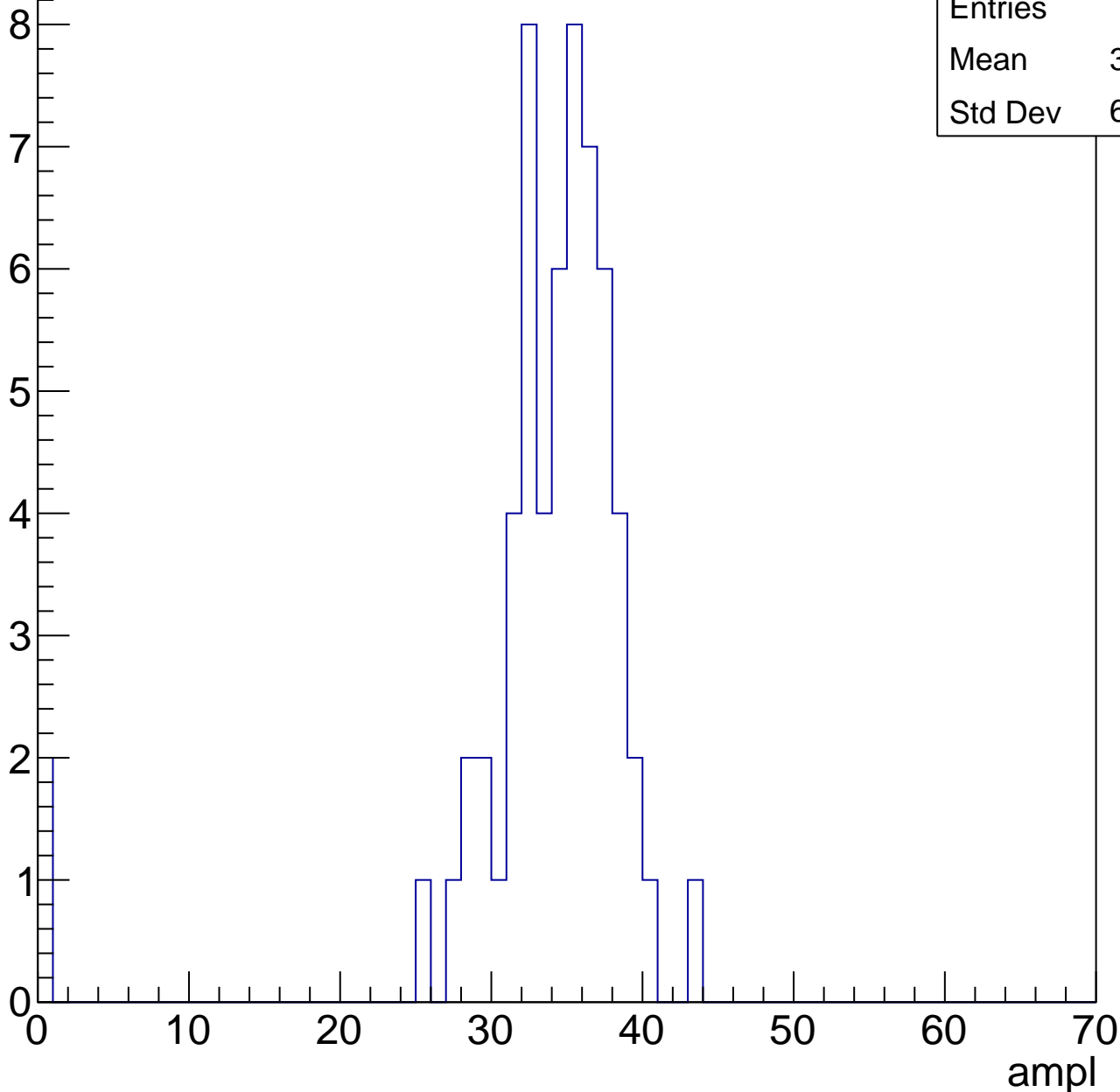


B1L103S, U9-ch60, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	32.98
Std Dev	6.965

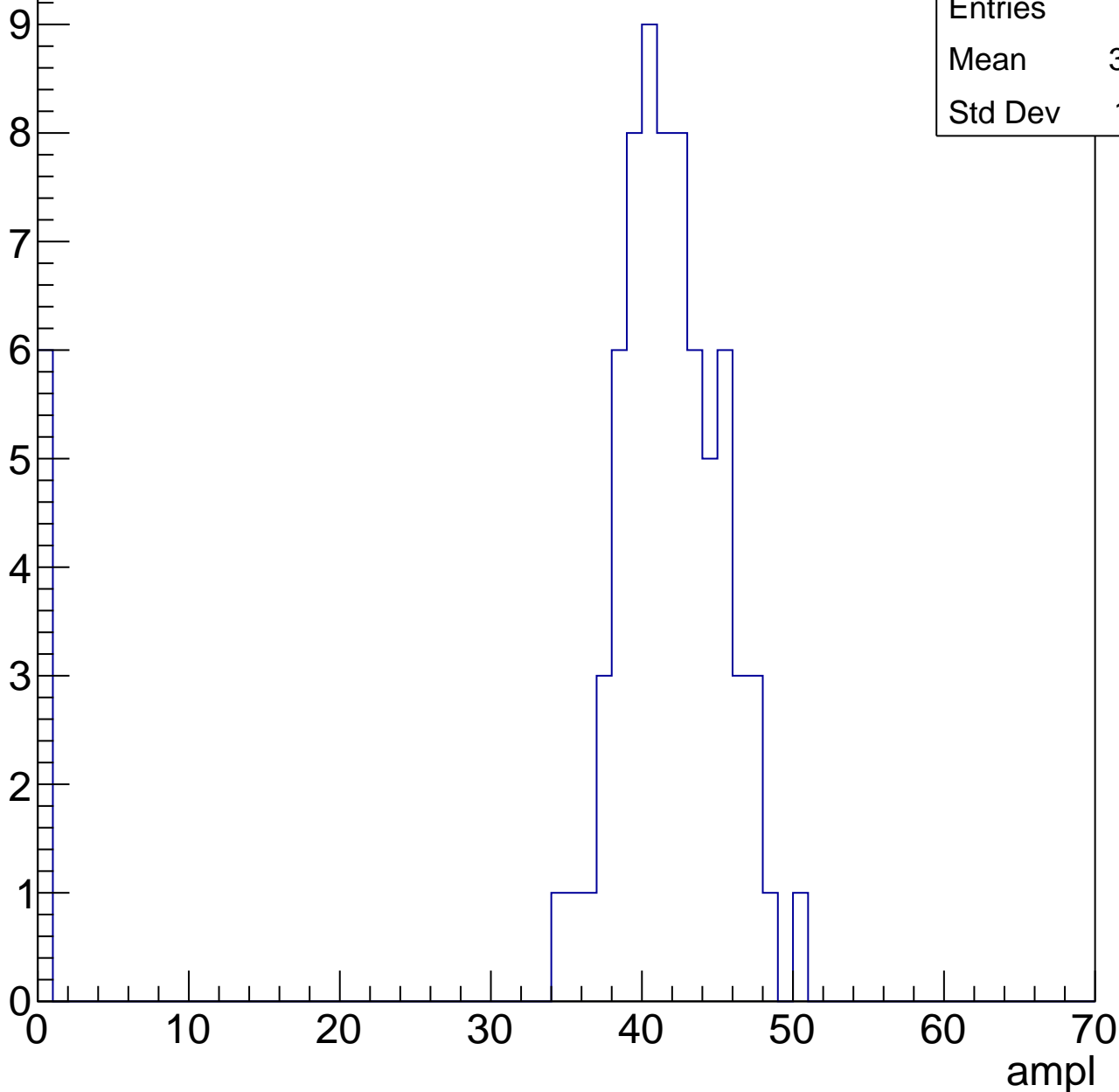


B1L103S, U9-ch60, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	38.22
Std Dev	11.61

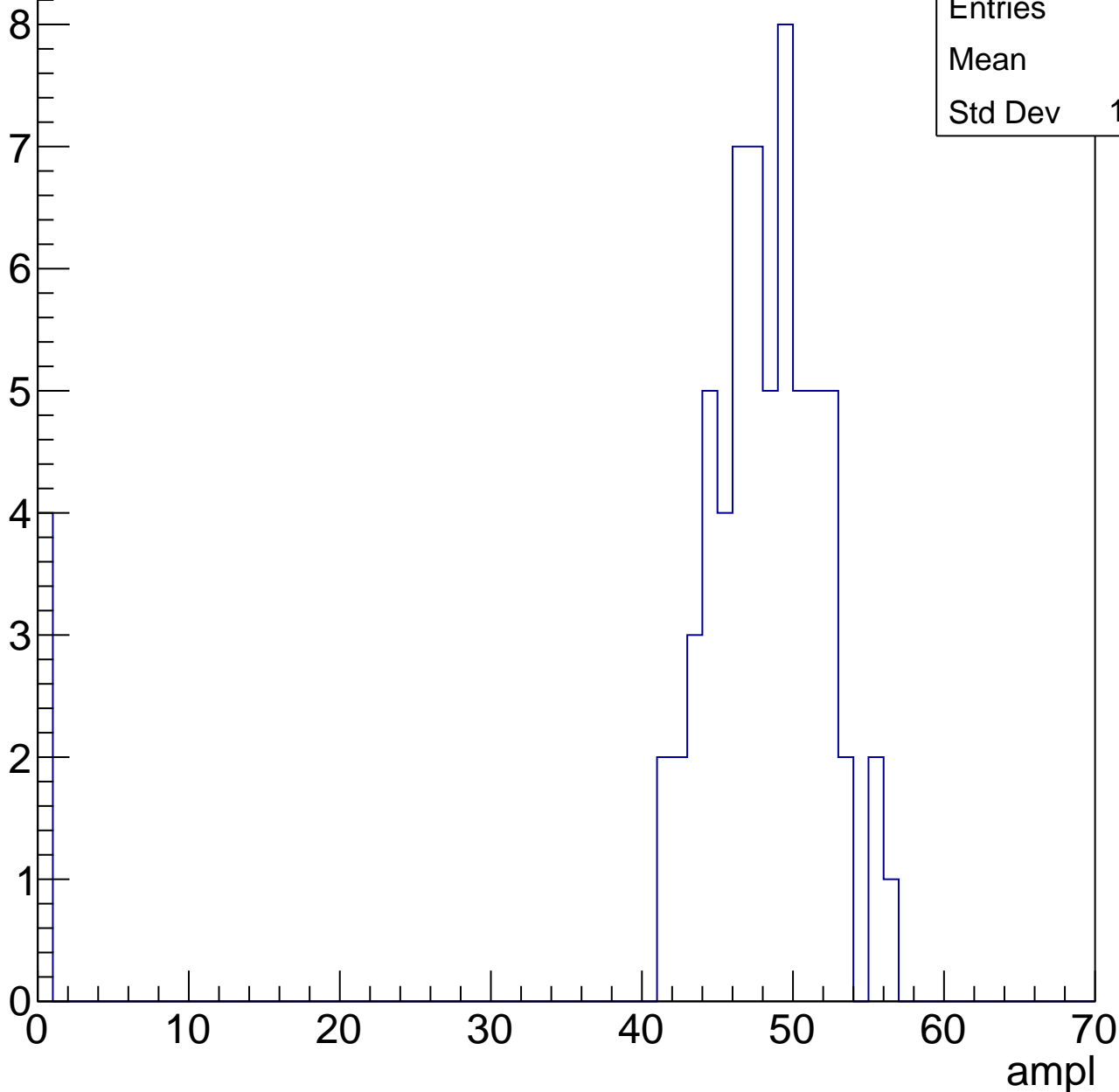


B1L103S, U9-ch60, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

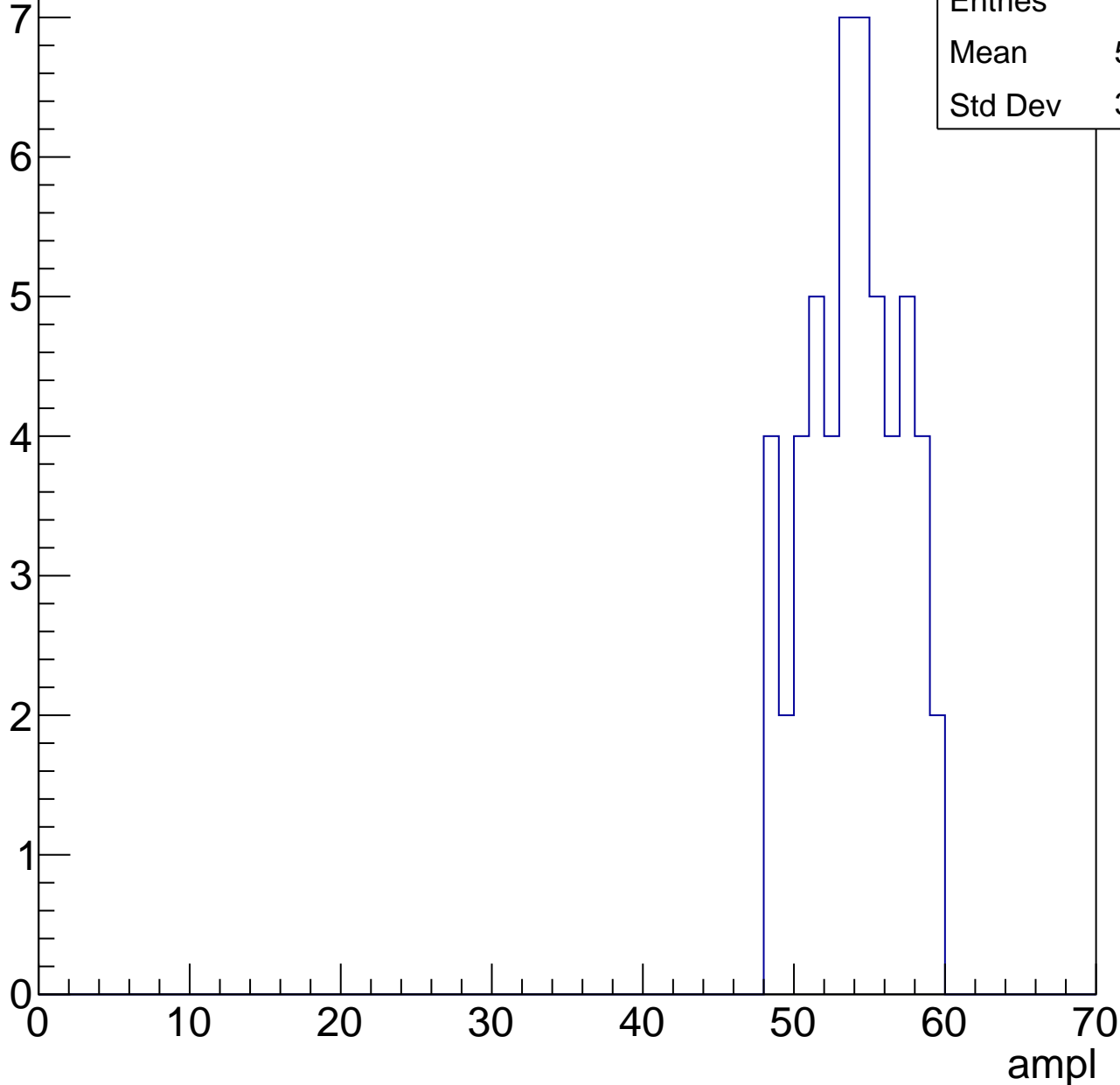
Entries	67
Mean	45
Std Dev	11.83



B1L103S, U9-ch60, adc4

calib_packv5_041523_1651.root, FC#0, port C2

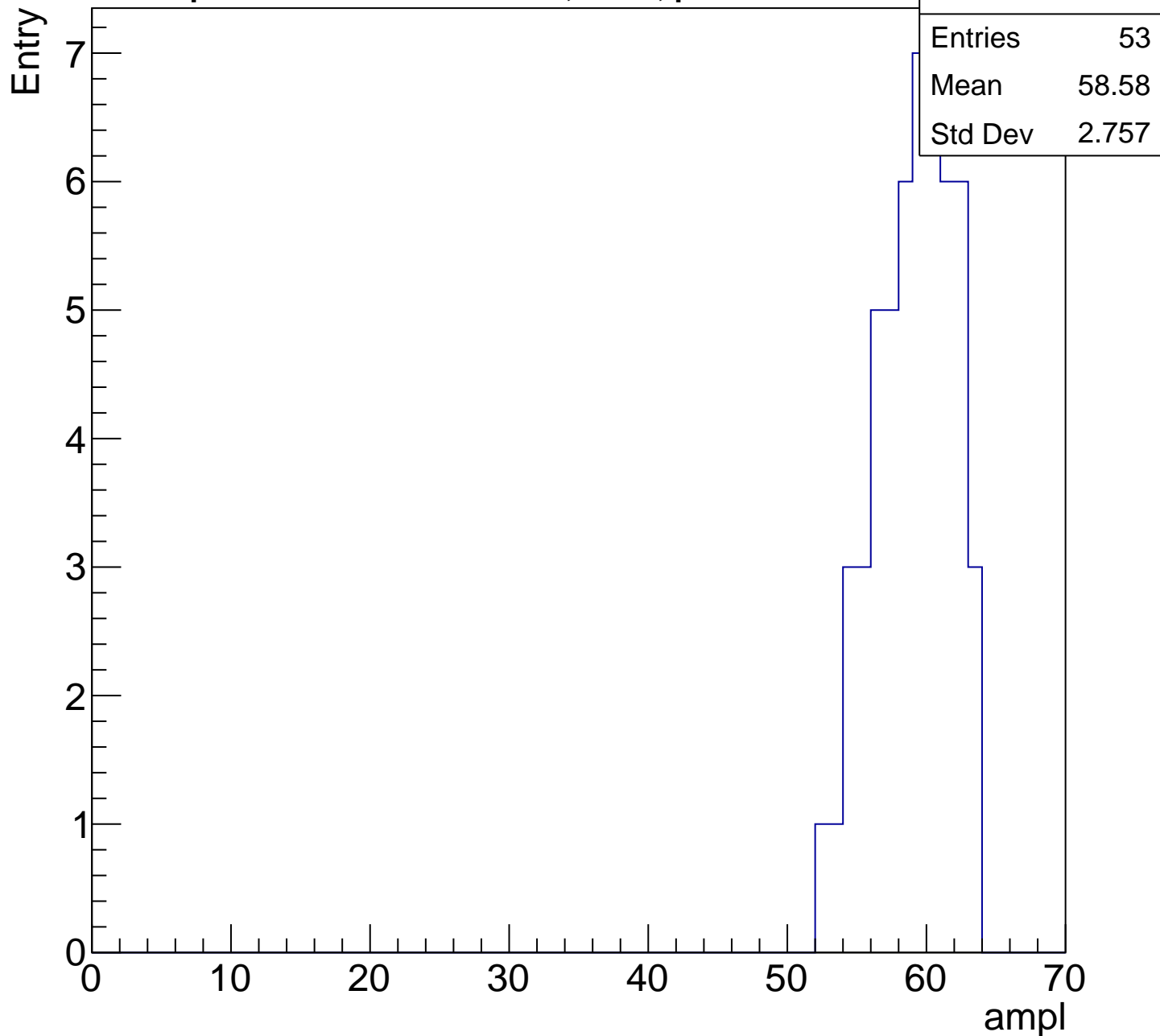
Entry



Entries	53
Mean	53.51
Std Dev	3.051

B1L103S, U9-ch60, adc5

calib_packv5_041523_1651.root, FC#0, port C2

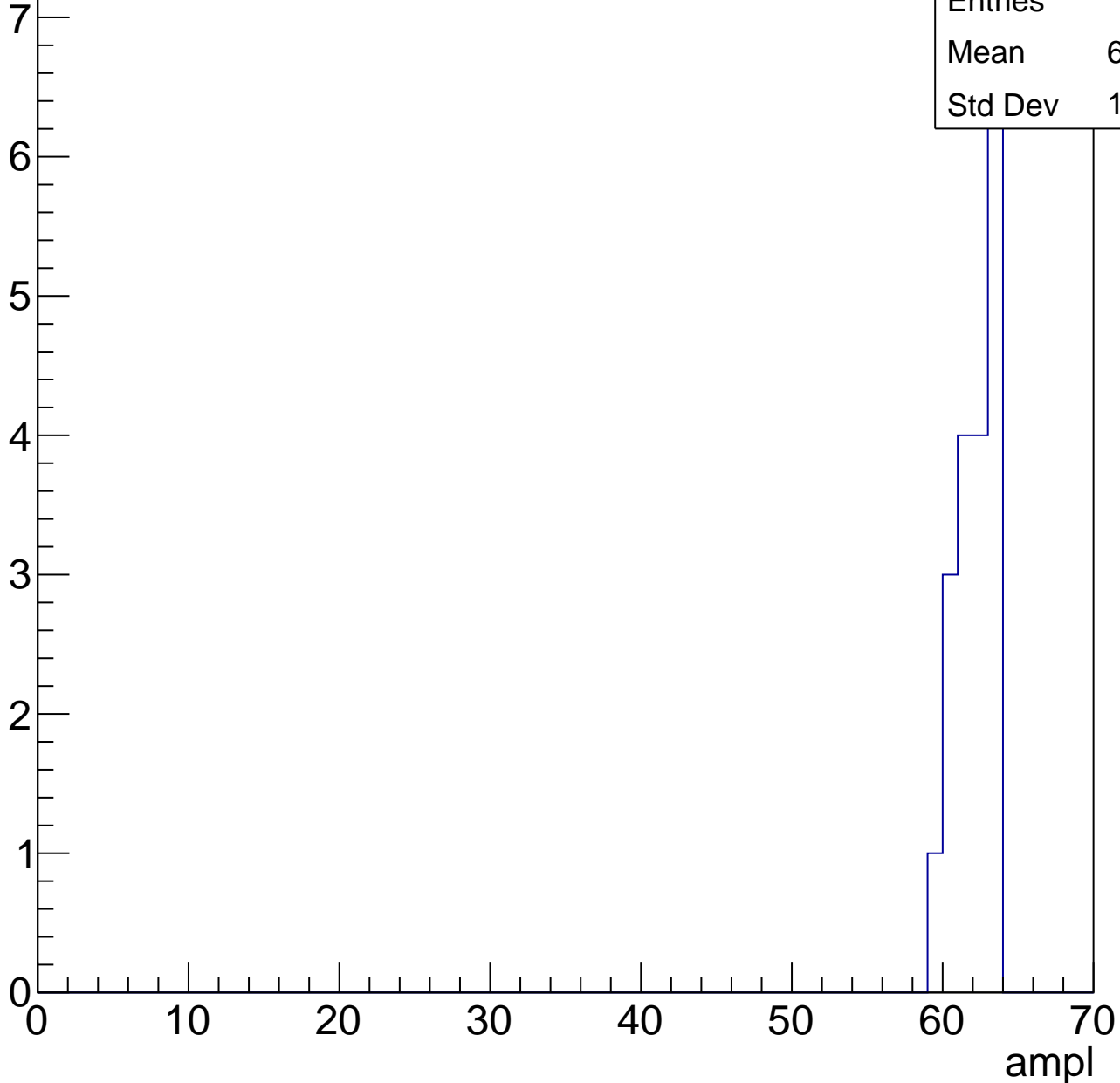


B1L103S, U9-ch60, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

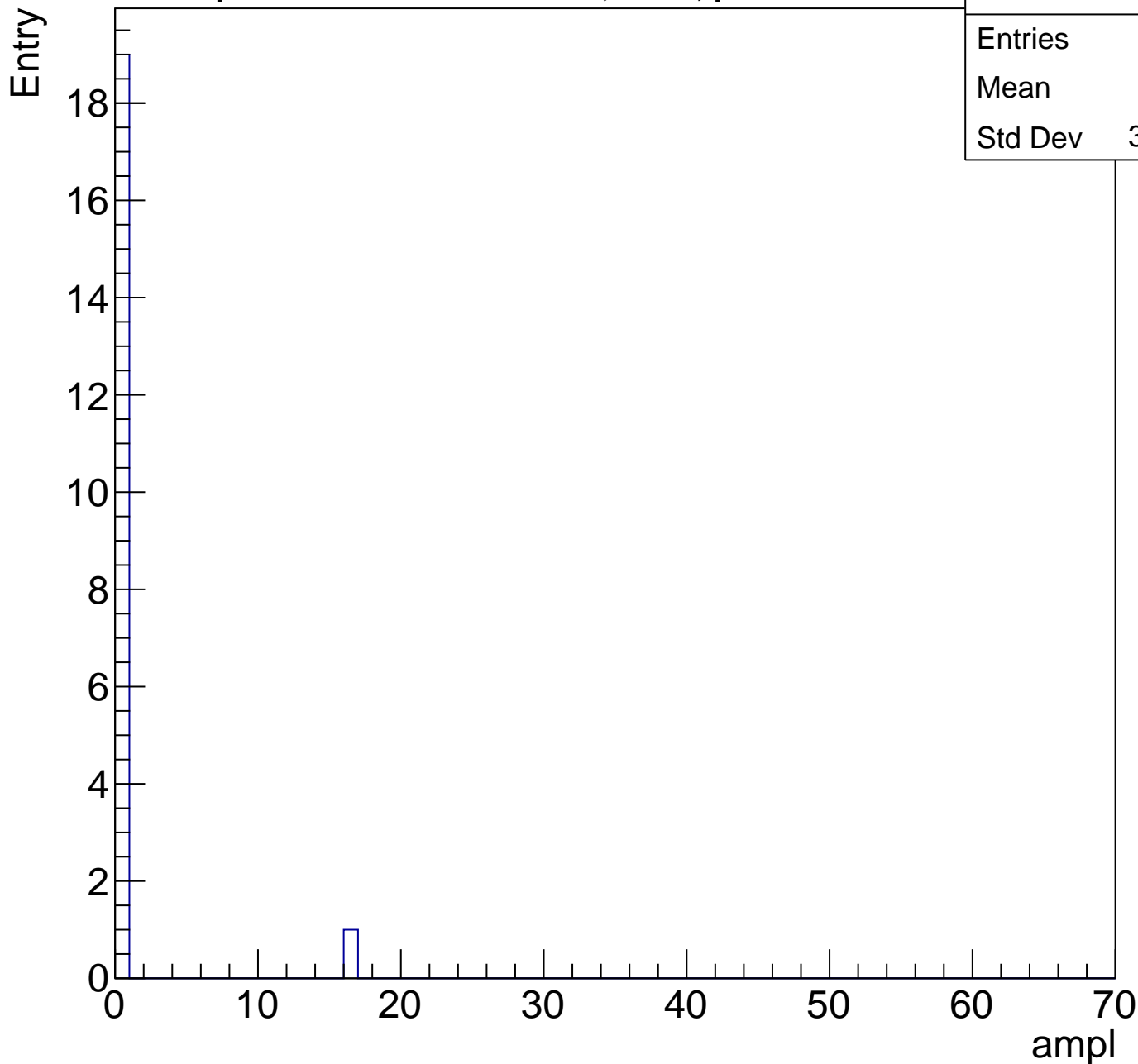
Entries	19
Mean	61.68
Std Dev	1.259



B1L103S, U9-ch60, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	0.8
Std Dev	3.487

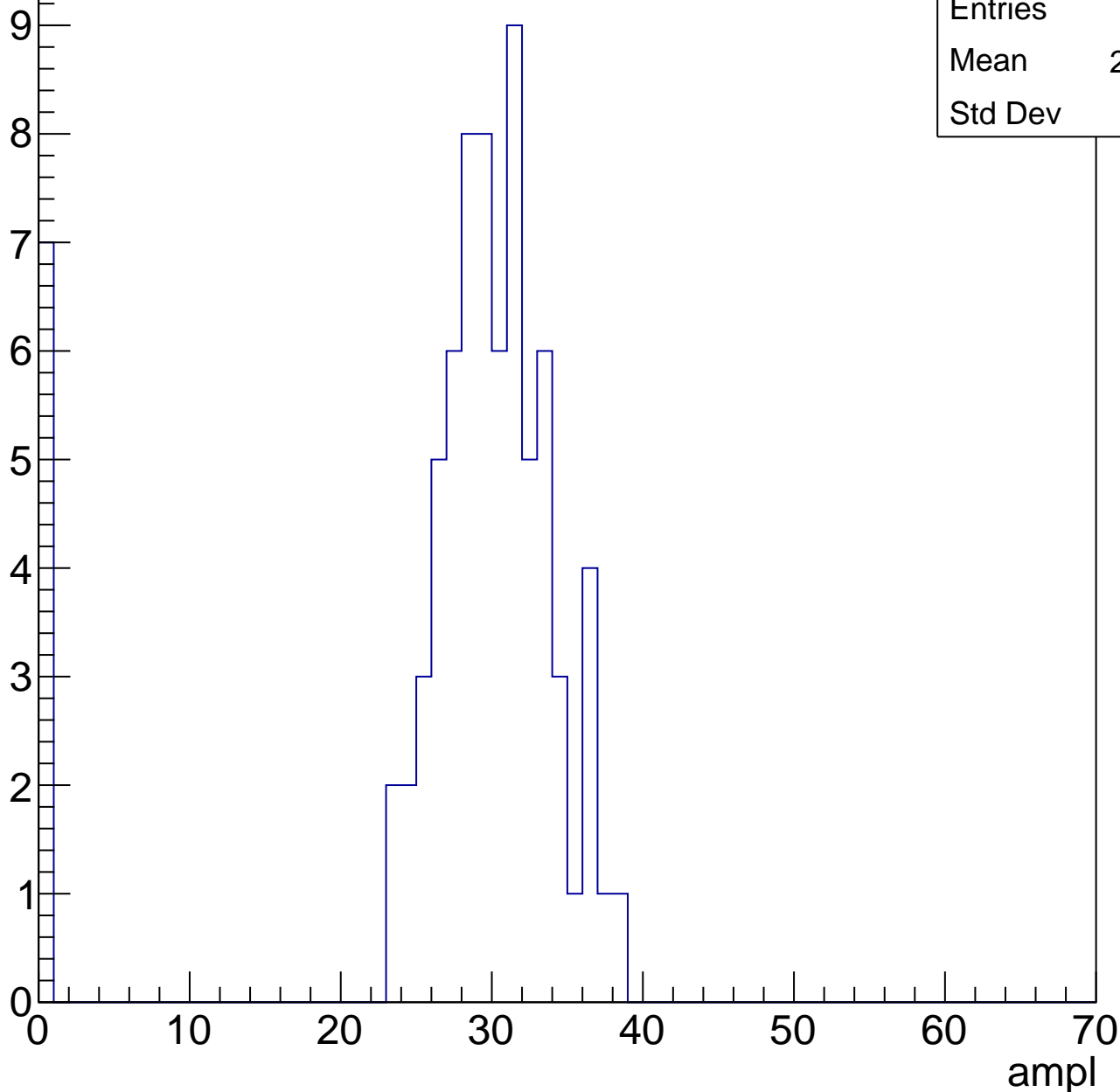


B1L103S, U9-ch61, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	27.14
Std Dev	9.19

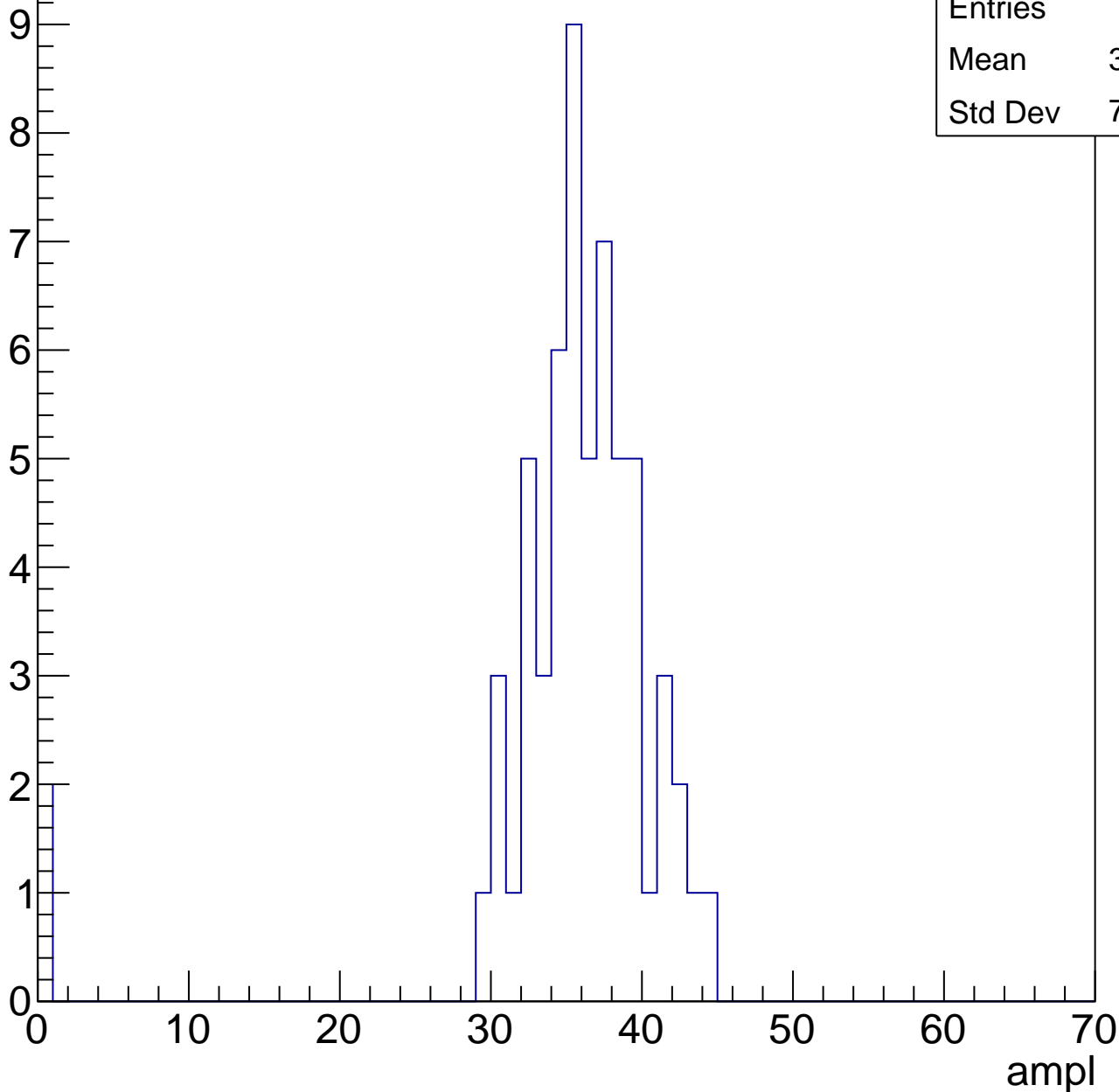


B1L103S, U9-ch61, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	34.77
Std Dev	7.269

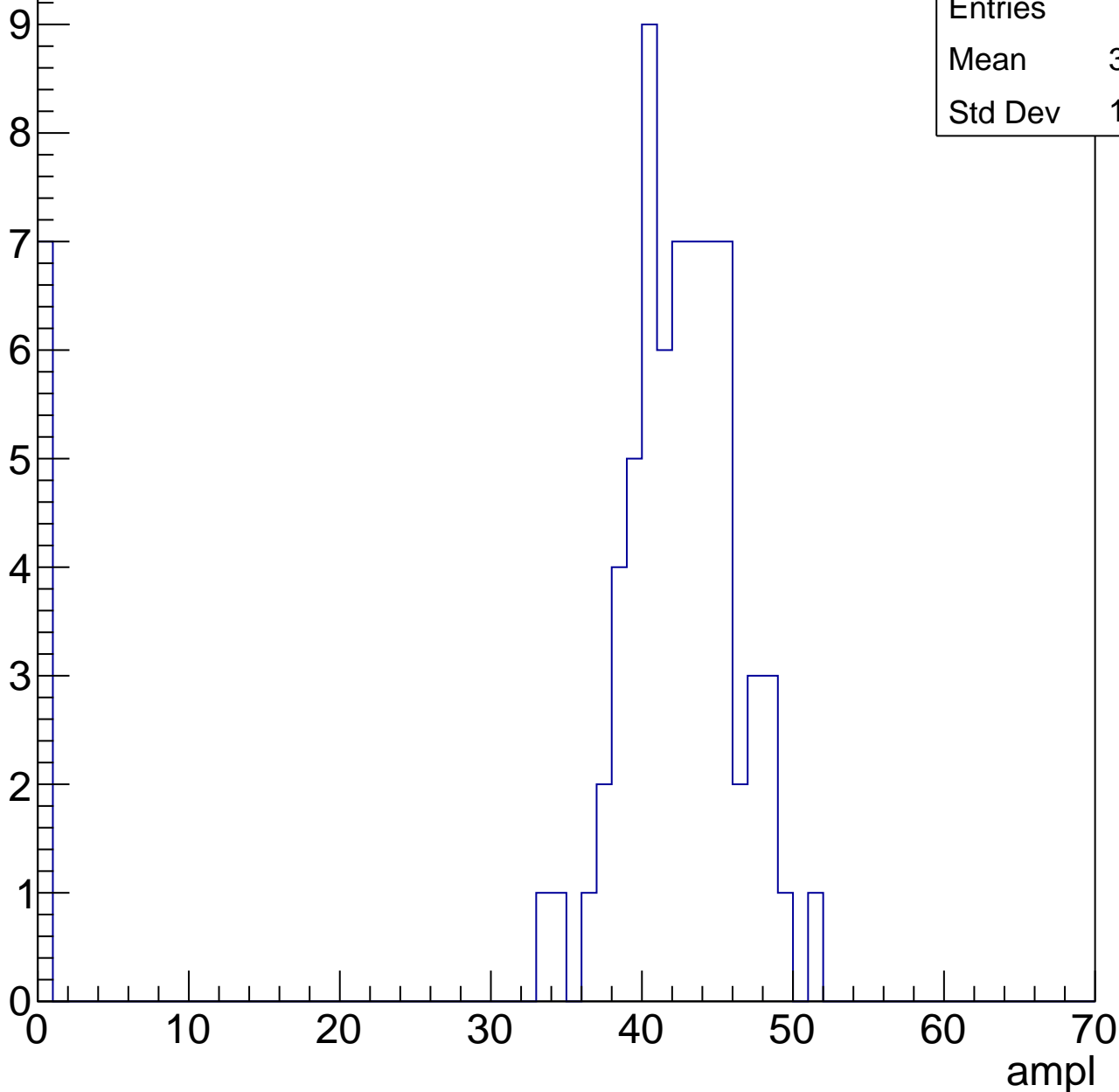


B1L103S, U9-ch61, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	38.18
Std Dev	12.78

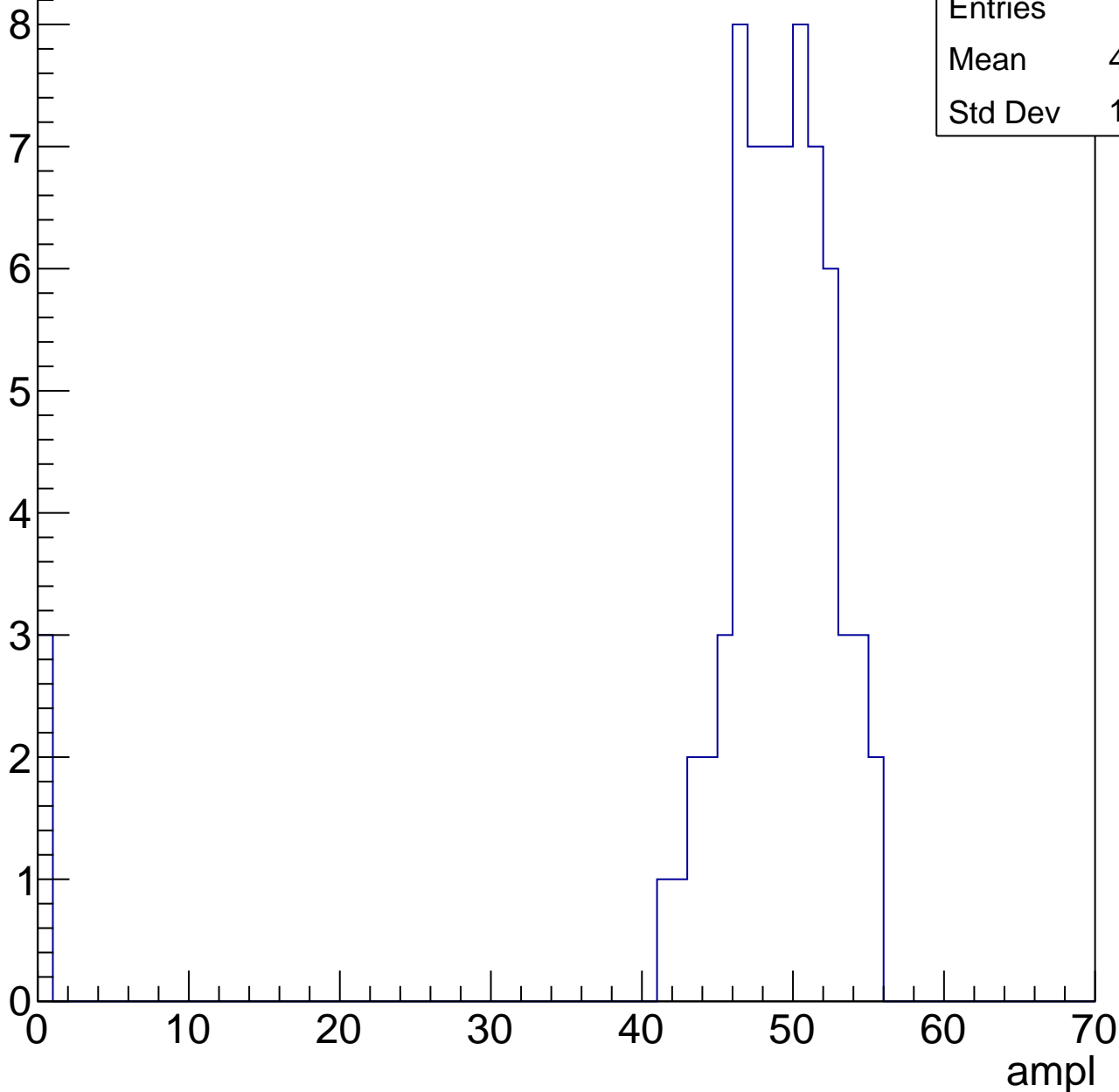


B1L103S, U9-ch61, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	46.69
Std Dev	10.35

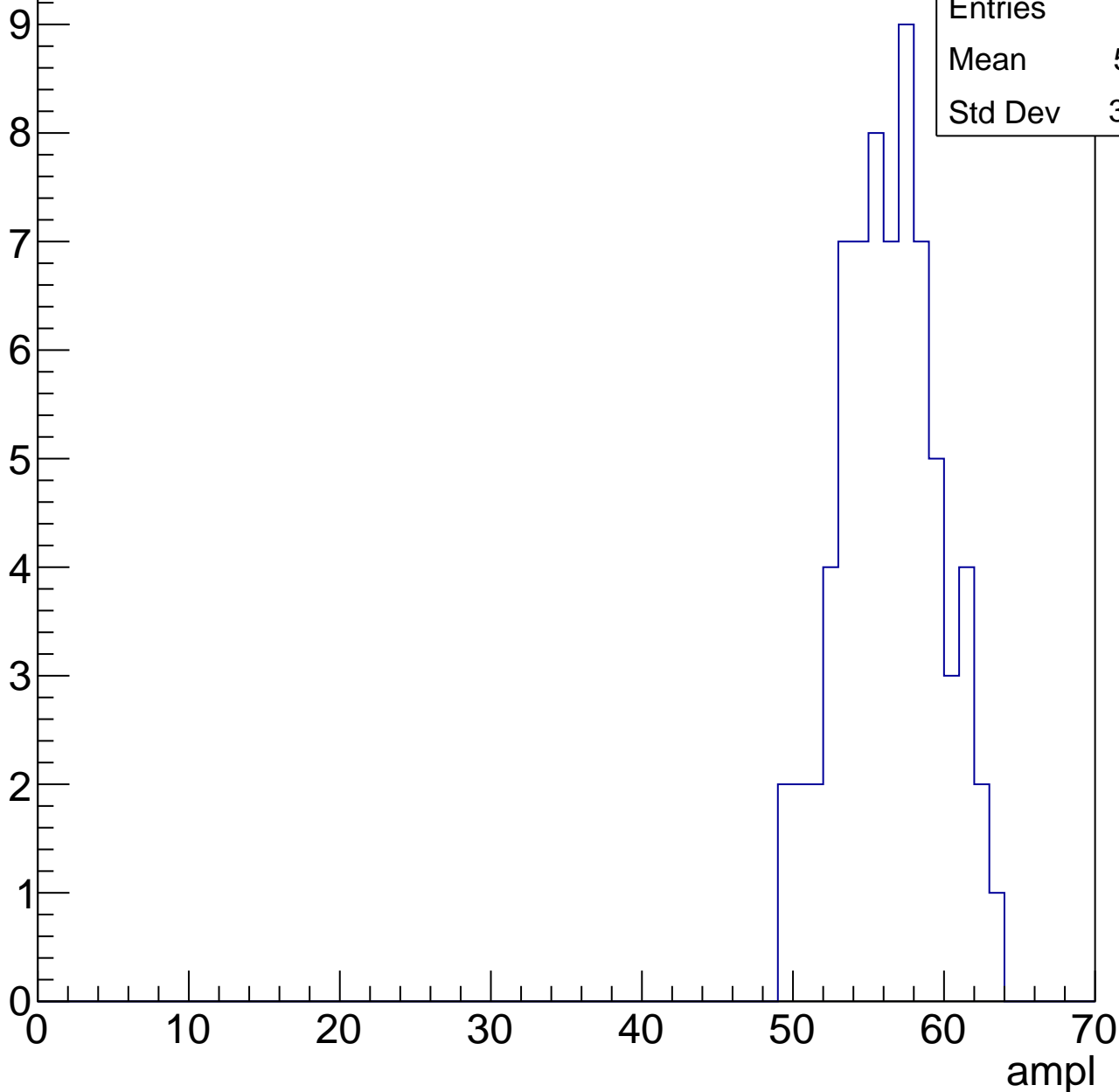


B1L103S, U9-ch61, adc4

calib_packv5_041523_1651.root, FC#0, port C2

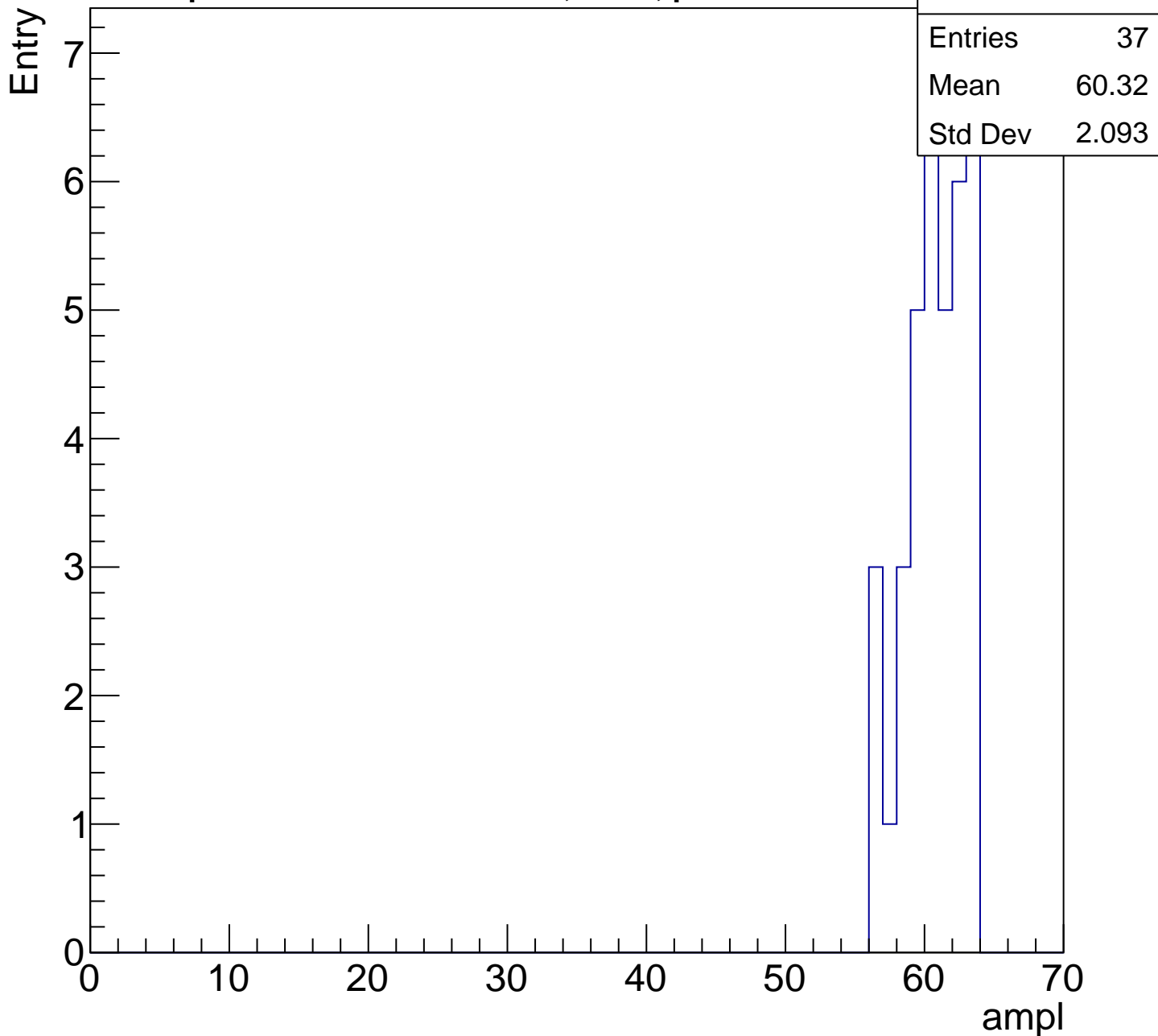
Entry

Entries	70
Mean	55.91
Std Dev	3.237



B1L103S, U9-ch61, adc5

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U9-ch61, adc6

calib_packv5_041523_1651.root, FC#0, port C2

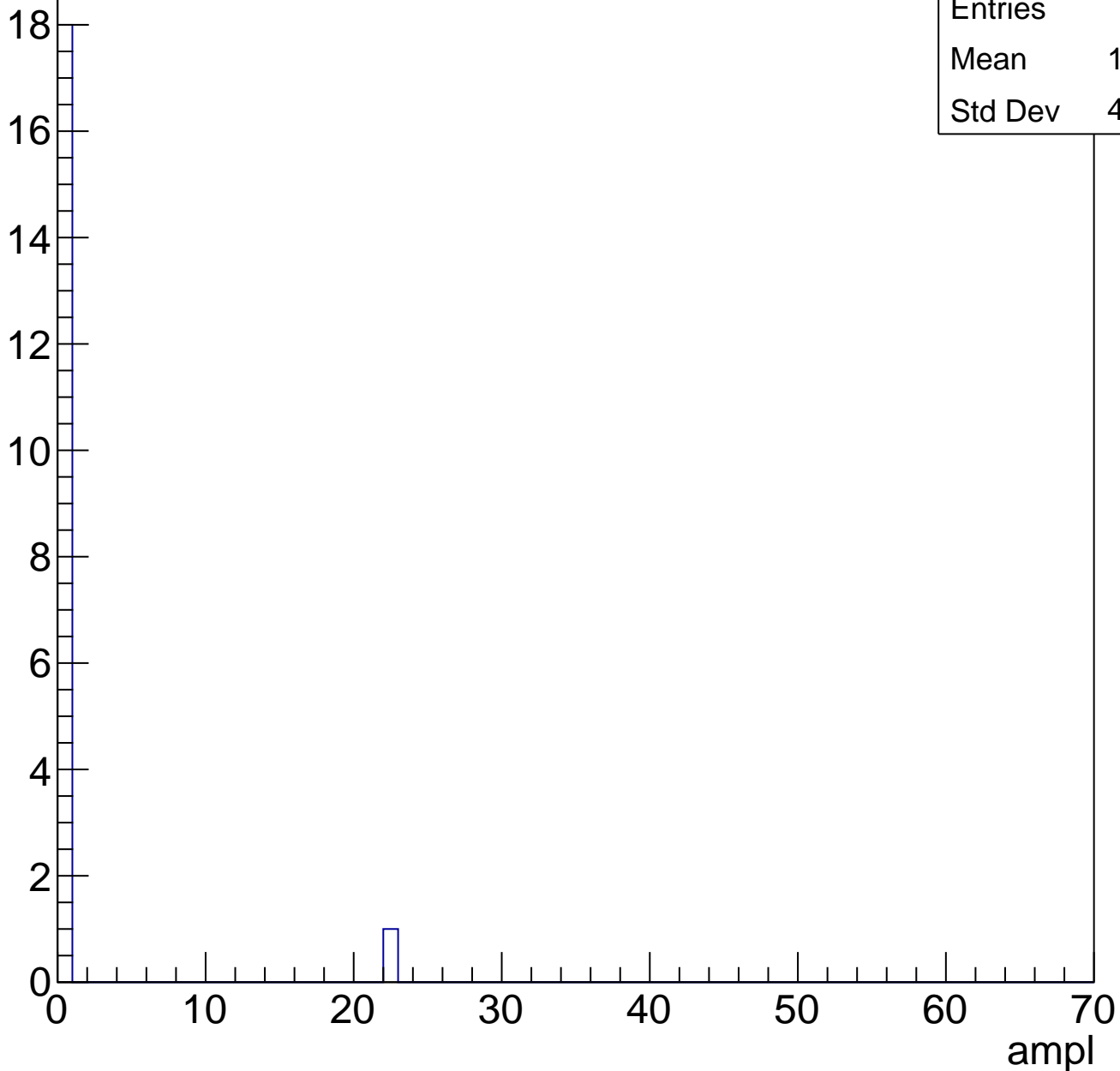
Entry



B1L103S, U9-ch61, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



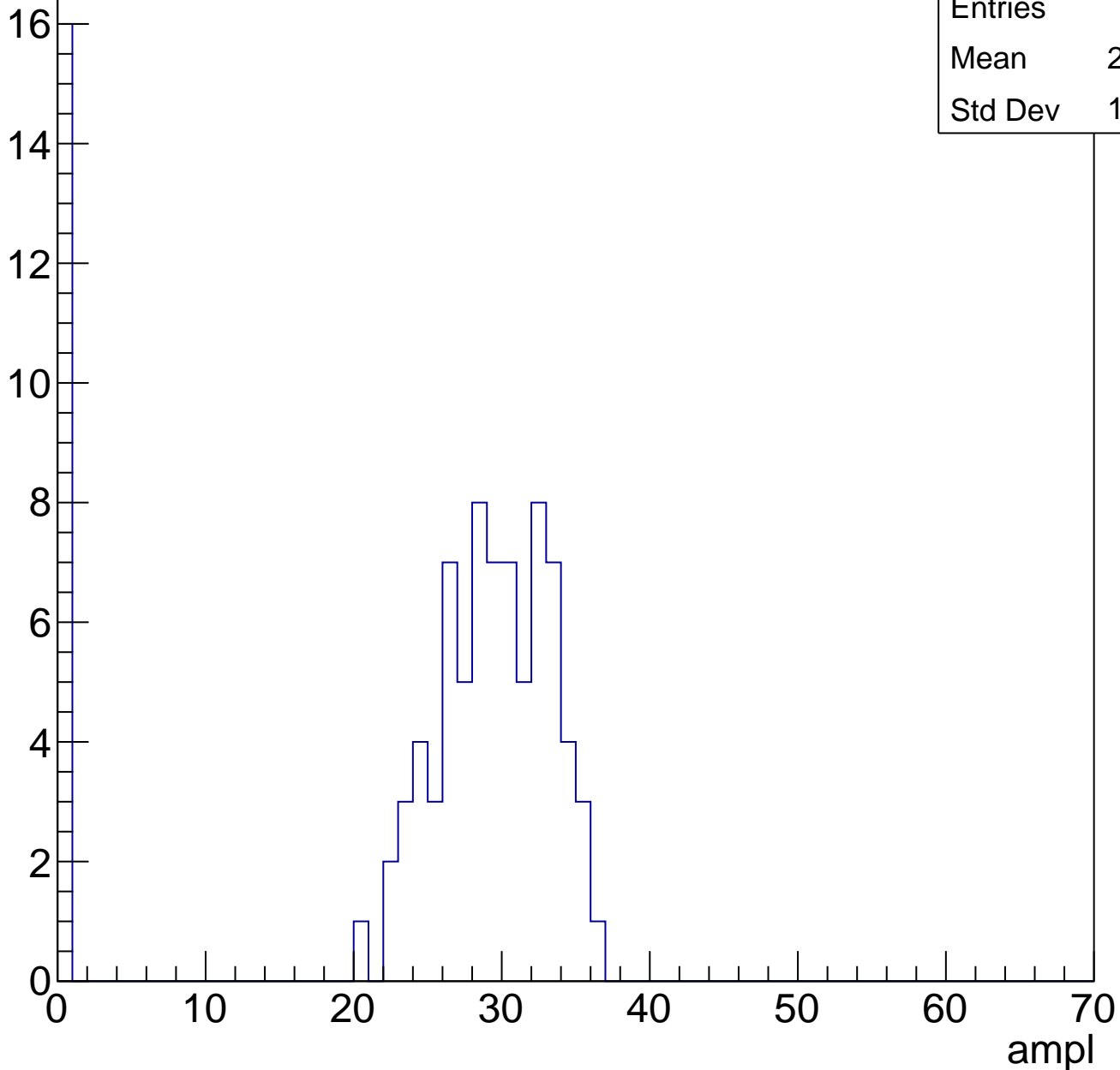
Entries	19
Mean	1.158
Std Dev	4.913

B1L103S, U9-ch62, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	91
Mean	23.92
Std Dev	11.53

Entry

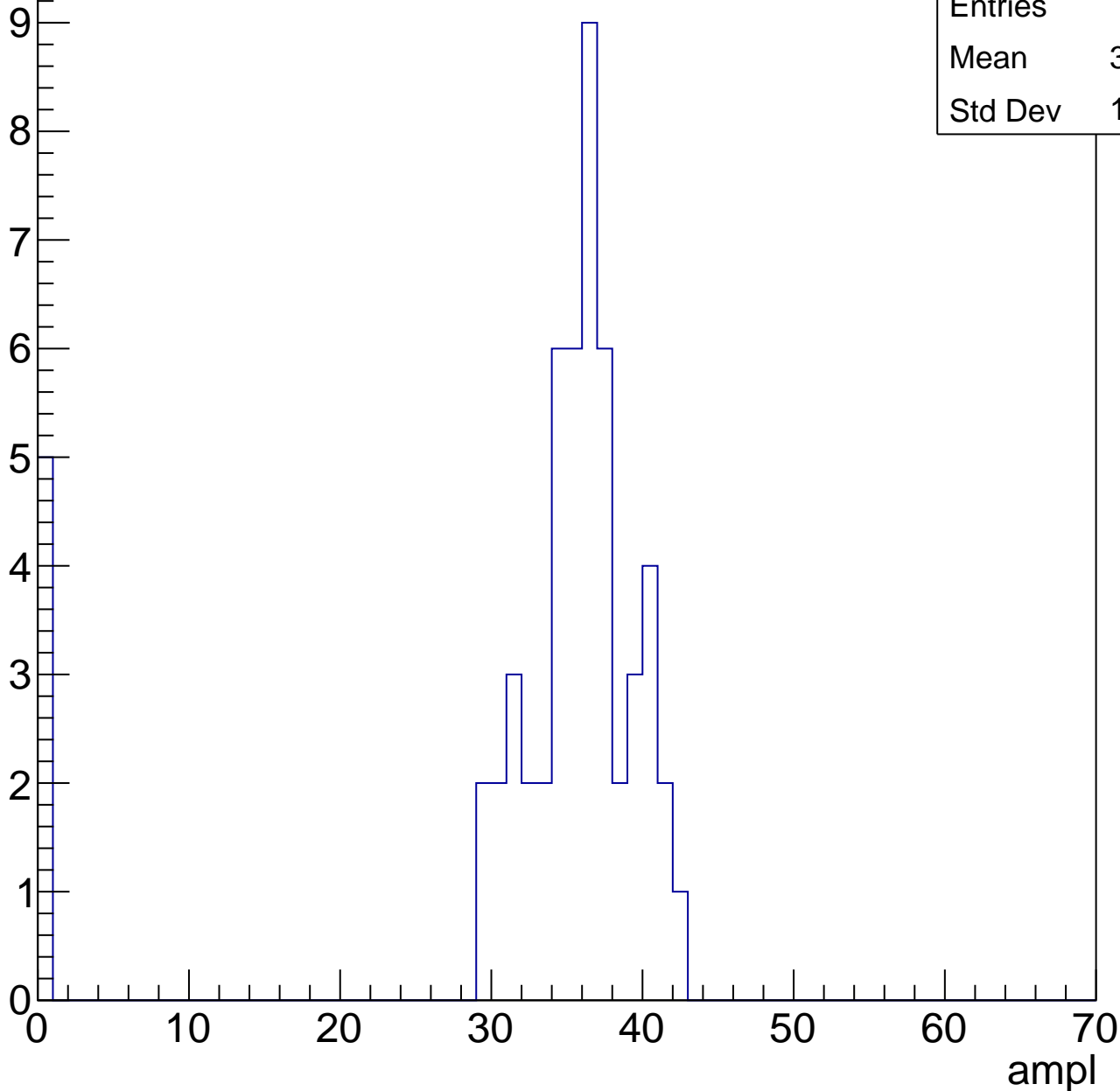


B1L103S, U9-ch62, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	32.33
Std Dev	10.66

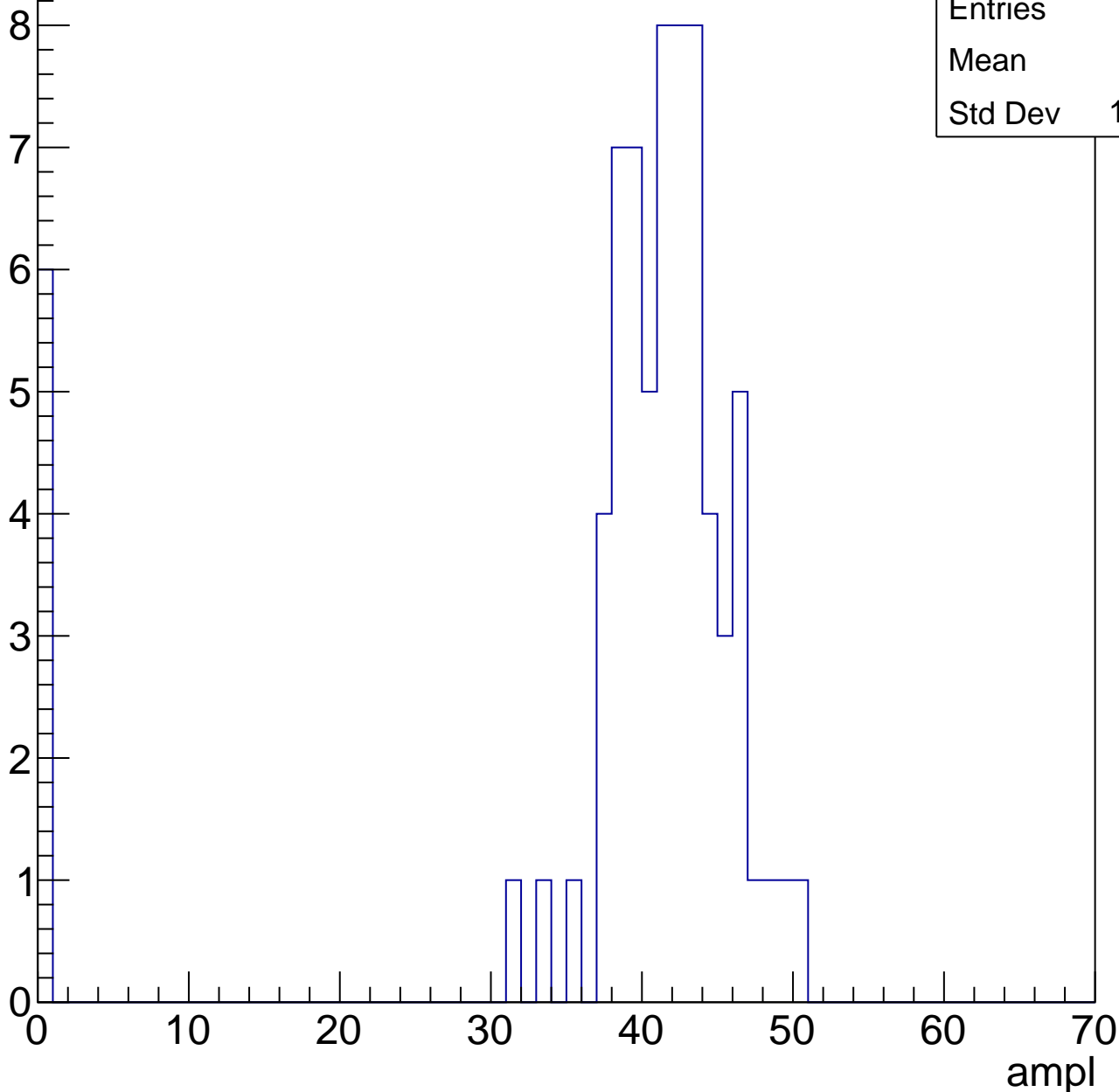


B1L103S, U9-ch62, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	37.9
Std Dev	11.92

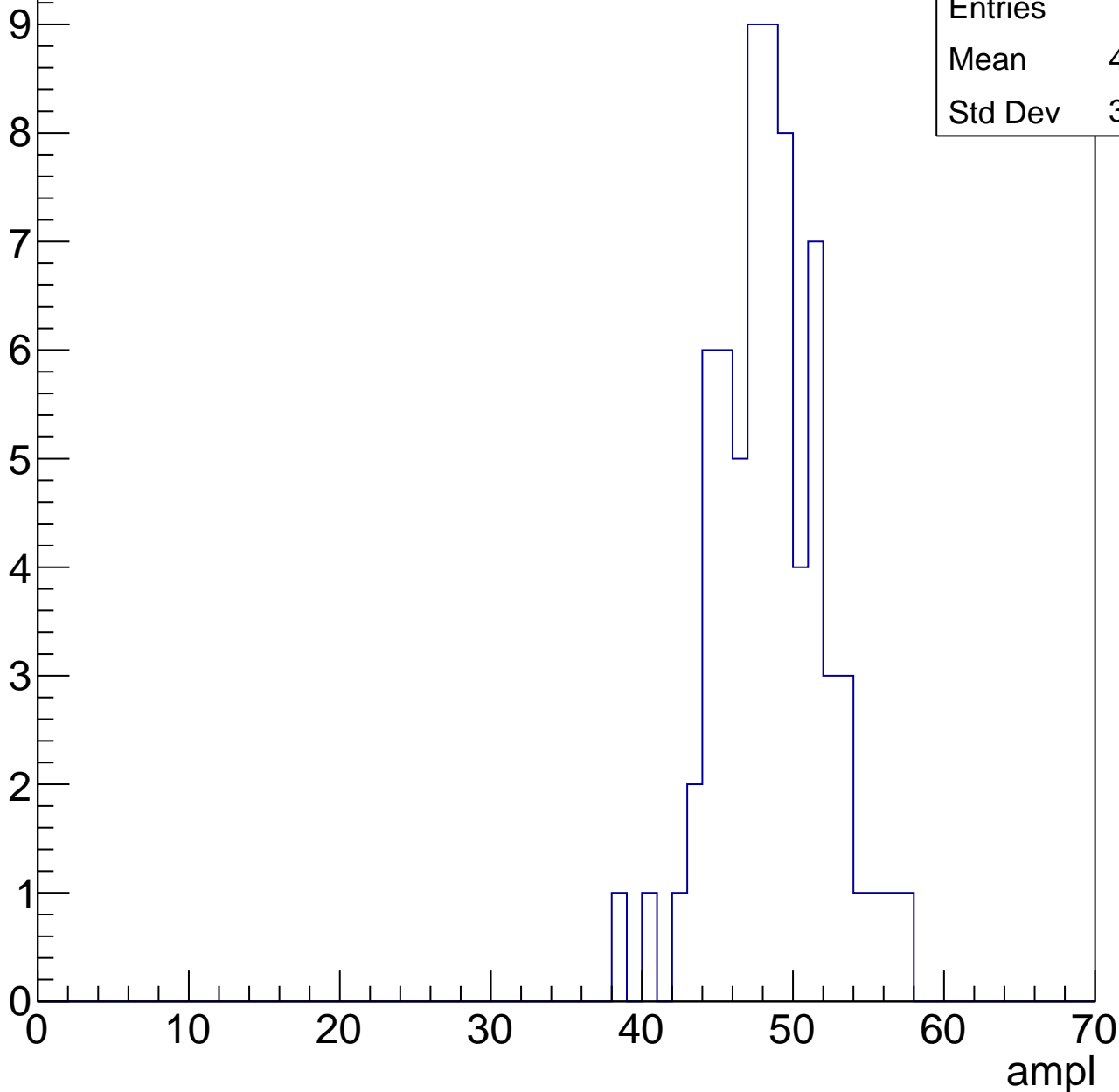


B1L103S, U9-ch62, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	47.99
Std Dev	3.549

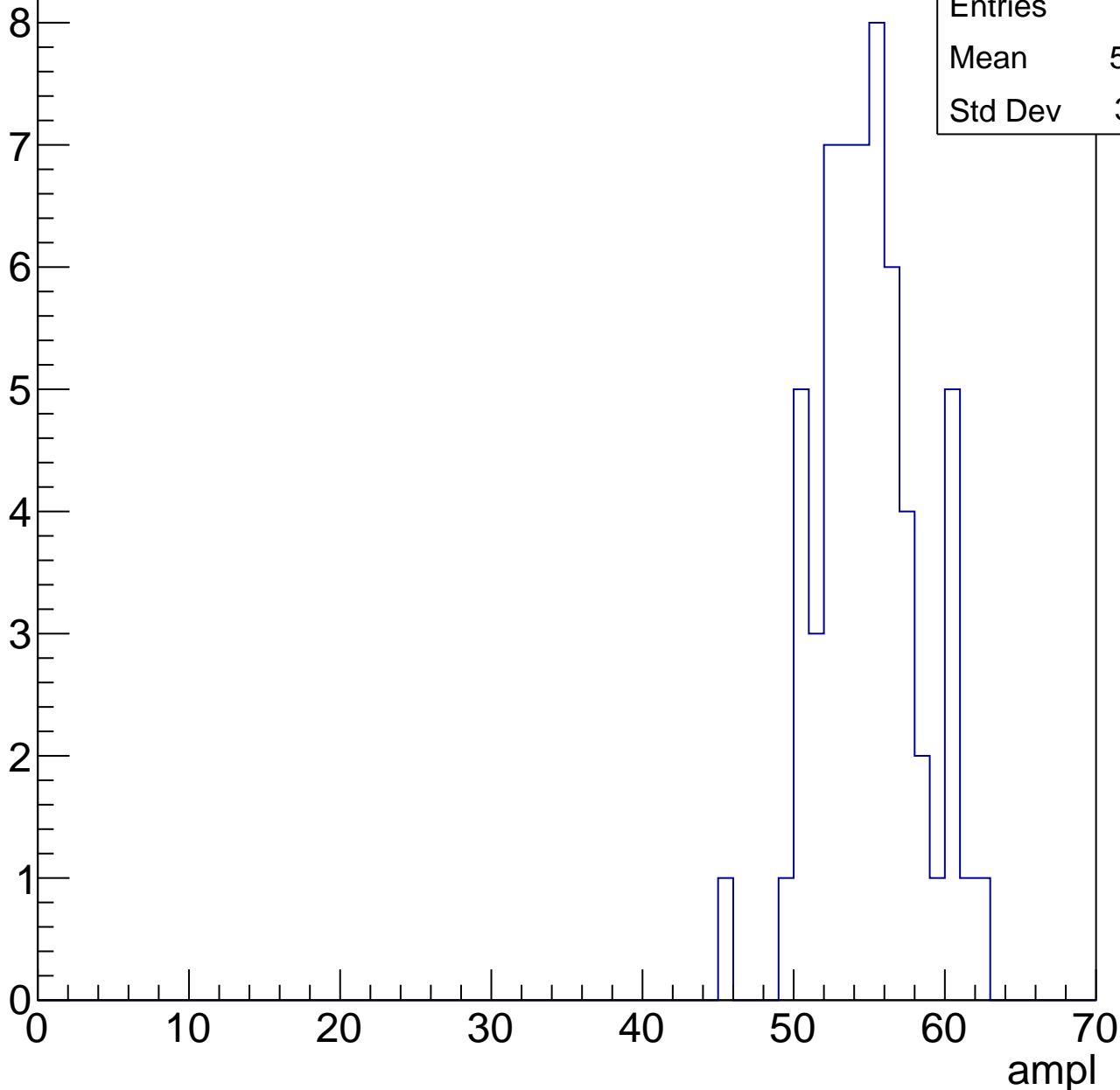


B1L103S, U9-ch62, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

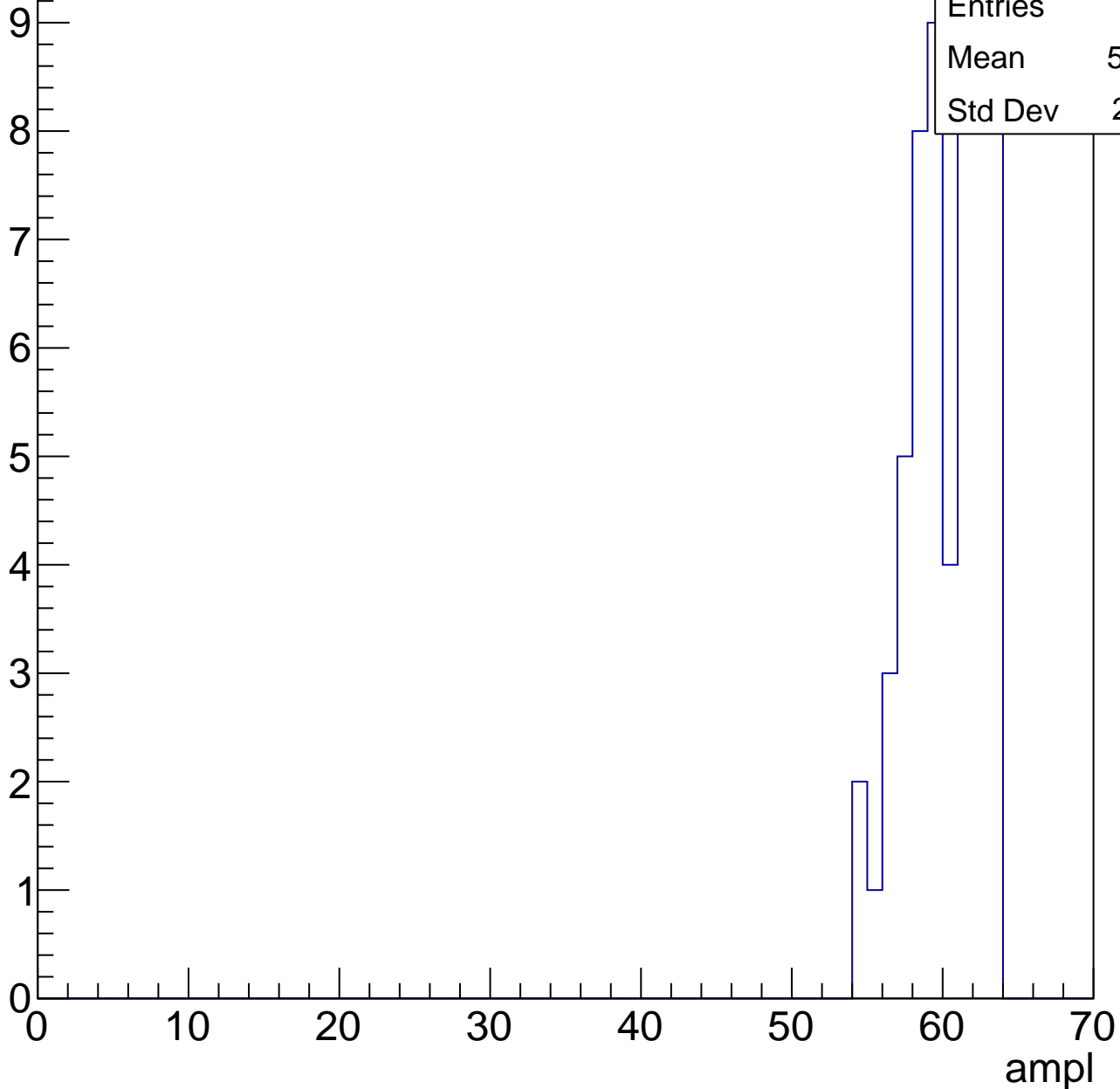
Entries	59
Mean	54.44
Std Dev	3.331



B1L103S, U9-ch62, adc5

calib_packv5_041523_1651.root, FC#0, port C2

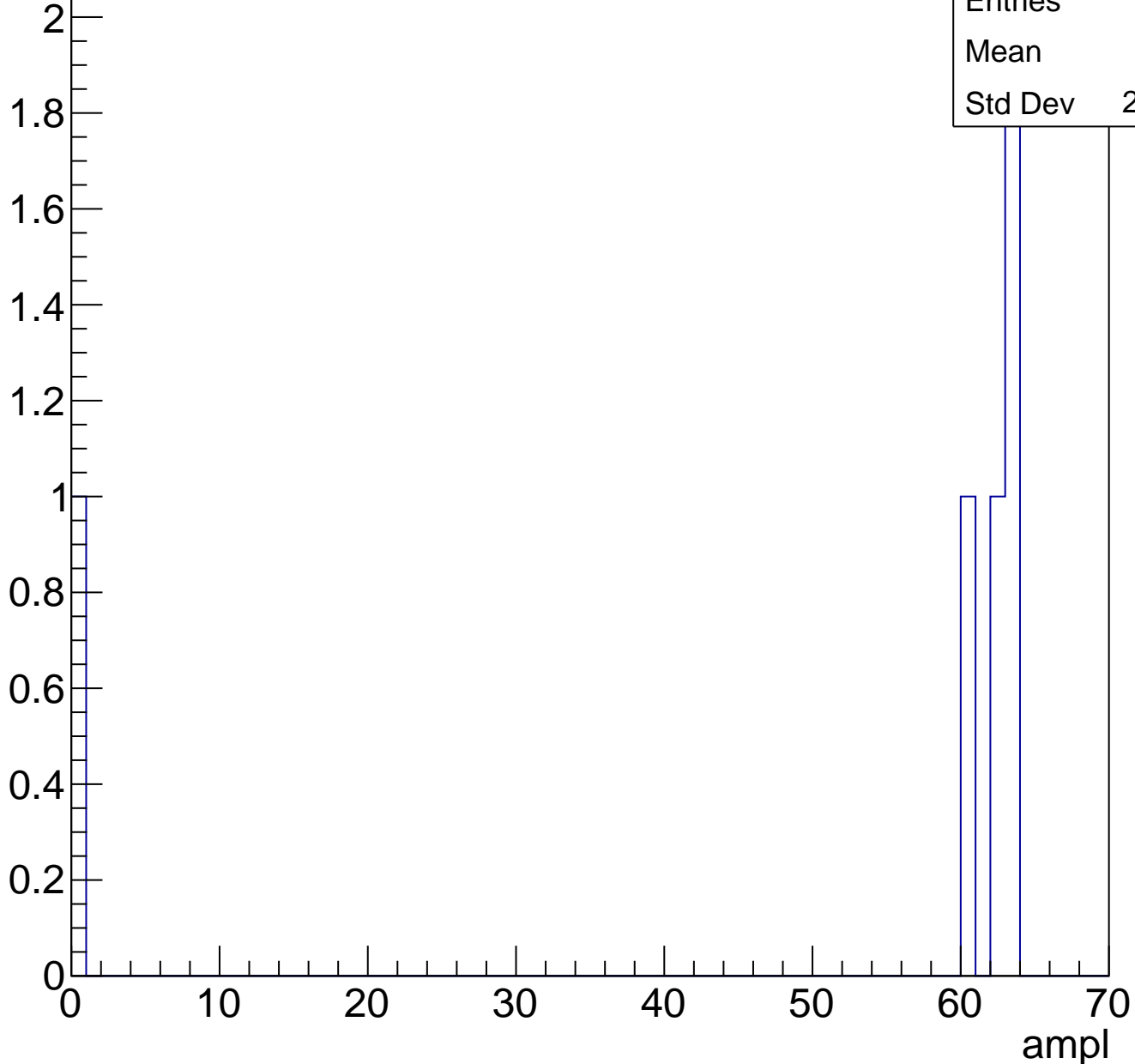
Entry



B1L103S, U9-ch62, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch62, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	19
Mean	0
Std Dev	0

B1L103S, U9-ch63, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	56
Mean	23.07
Std Dev	12.91

Entry

12

10

8

6

4

2

0

0

10

20

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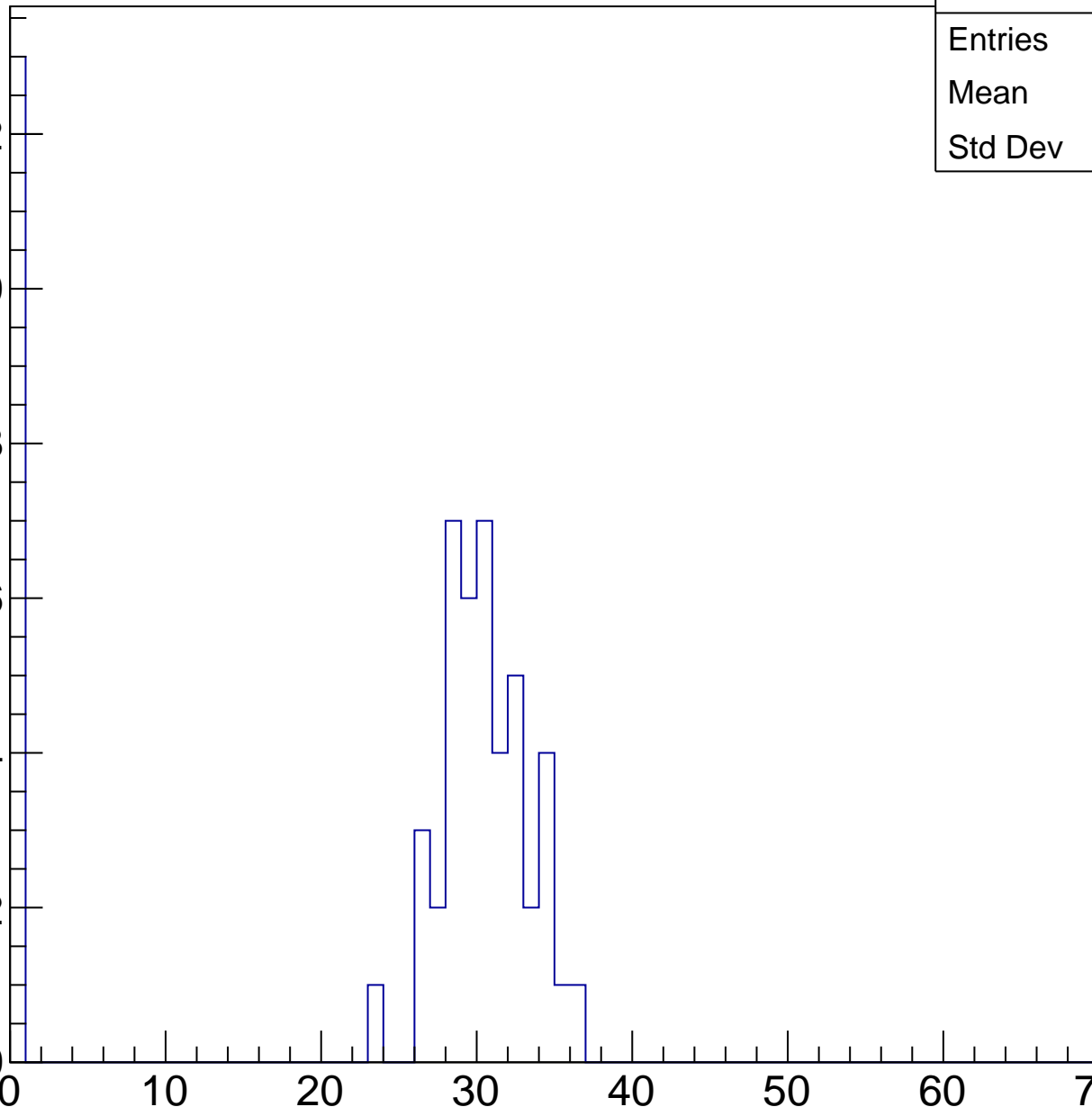
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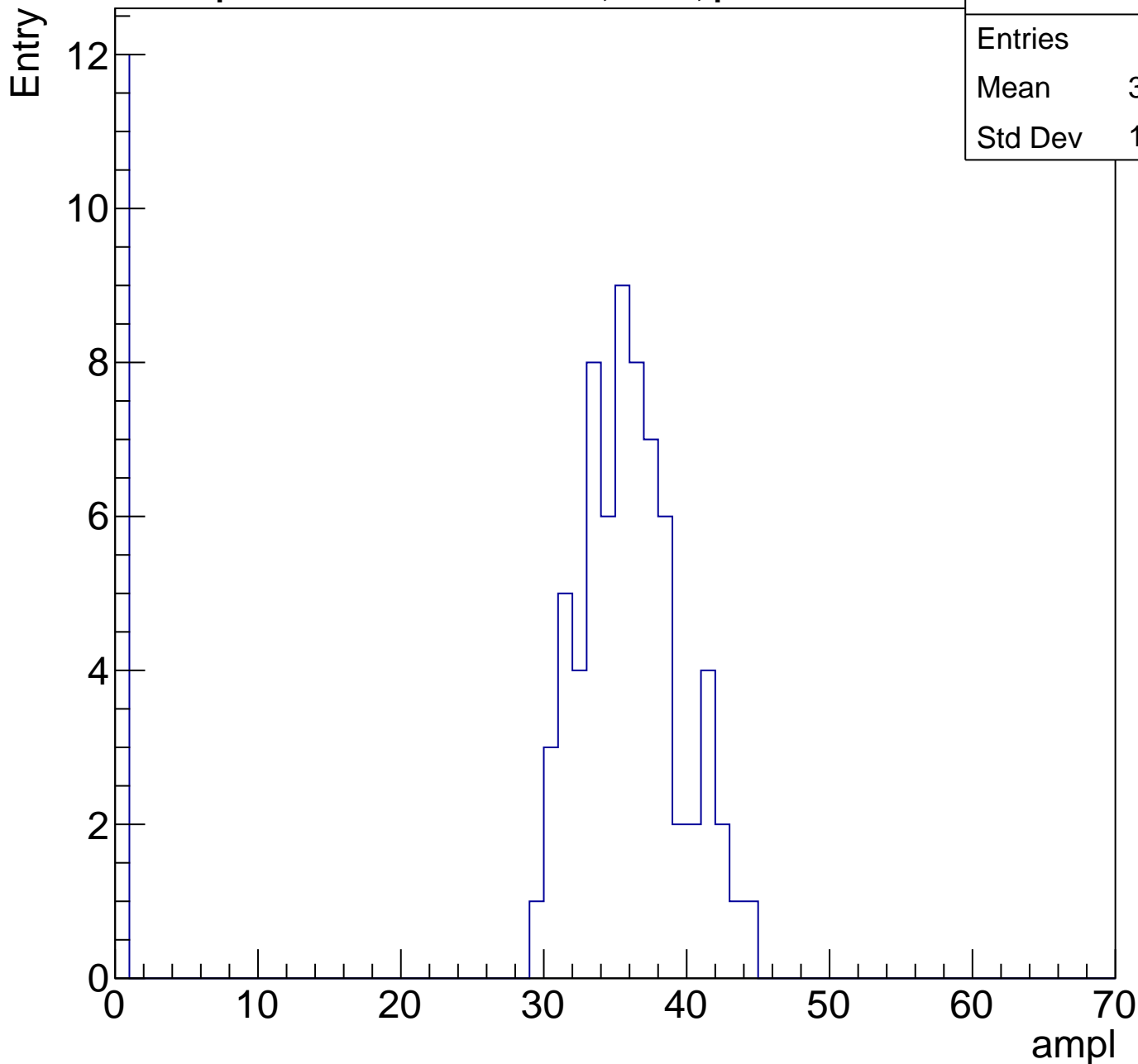
ampl



B1L103S, U9-ch63, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	30.28
Std Dev	13.02

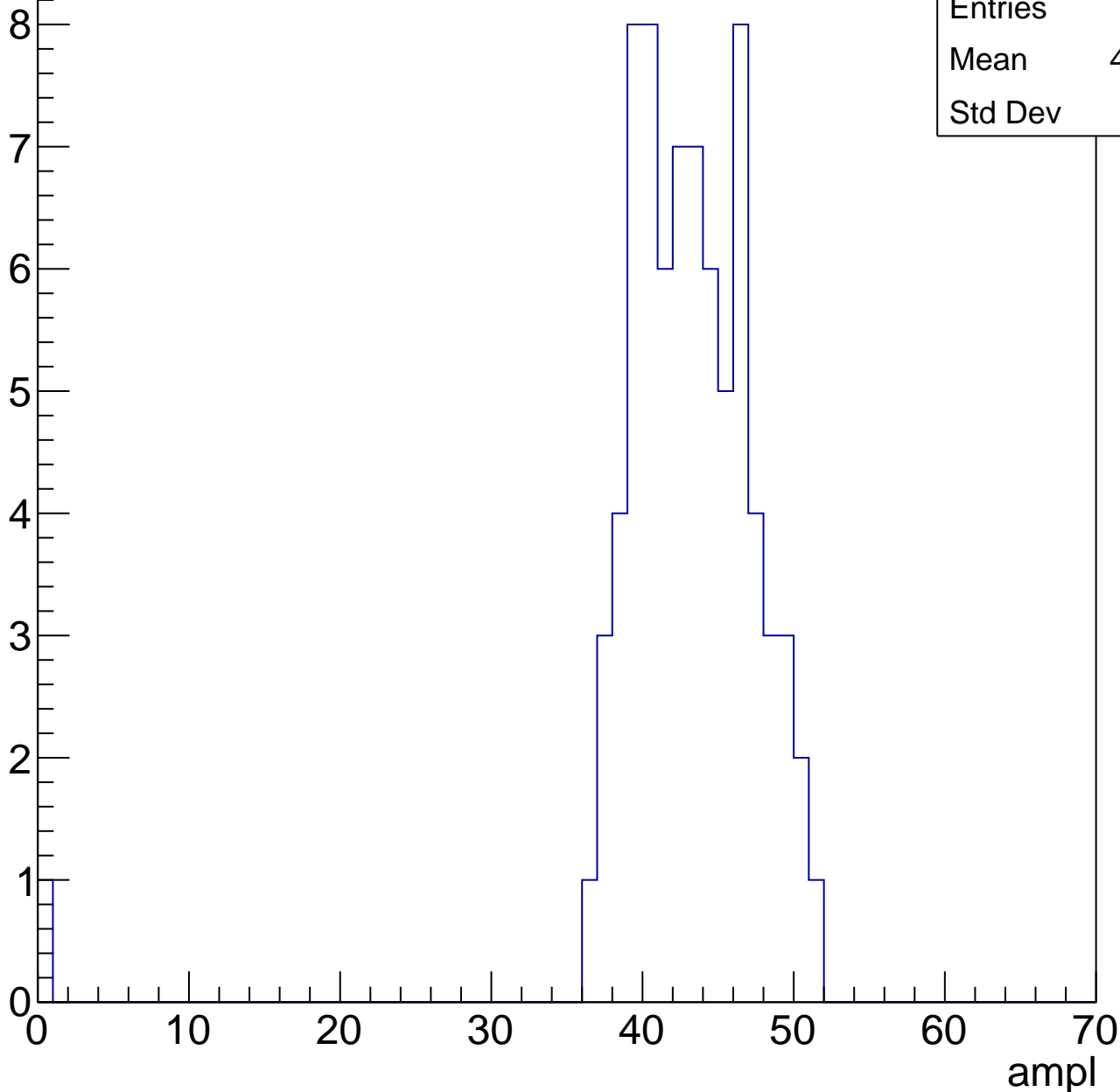


B1L103S, U9-ch63, adc2

calib_packv5_041523_1651.root, FC#0, port C2

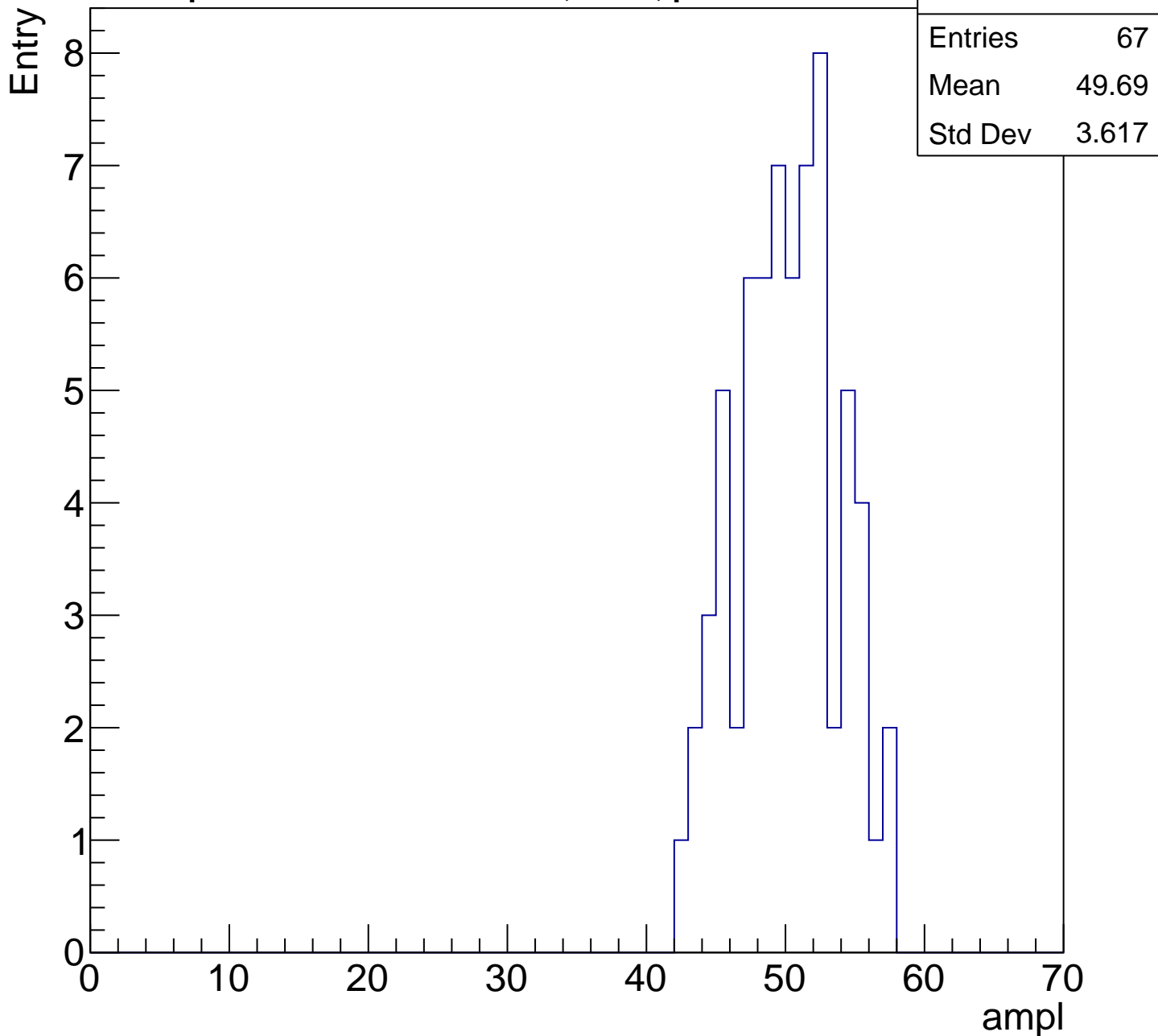
Entry

Entries	77
Mean	42.32
Std Dev	6.04



B1L103S, U9-ch63, adc3

calib_packv5_041523_1651.root, FC#0, port C2

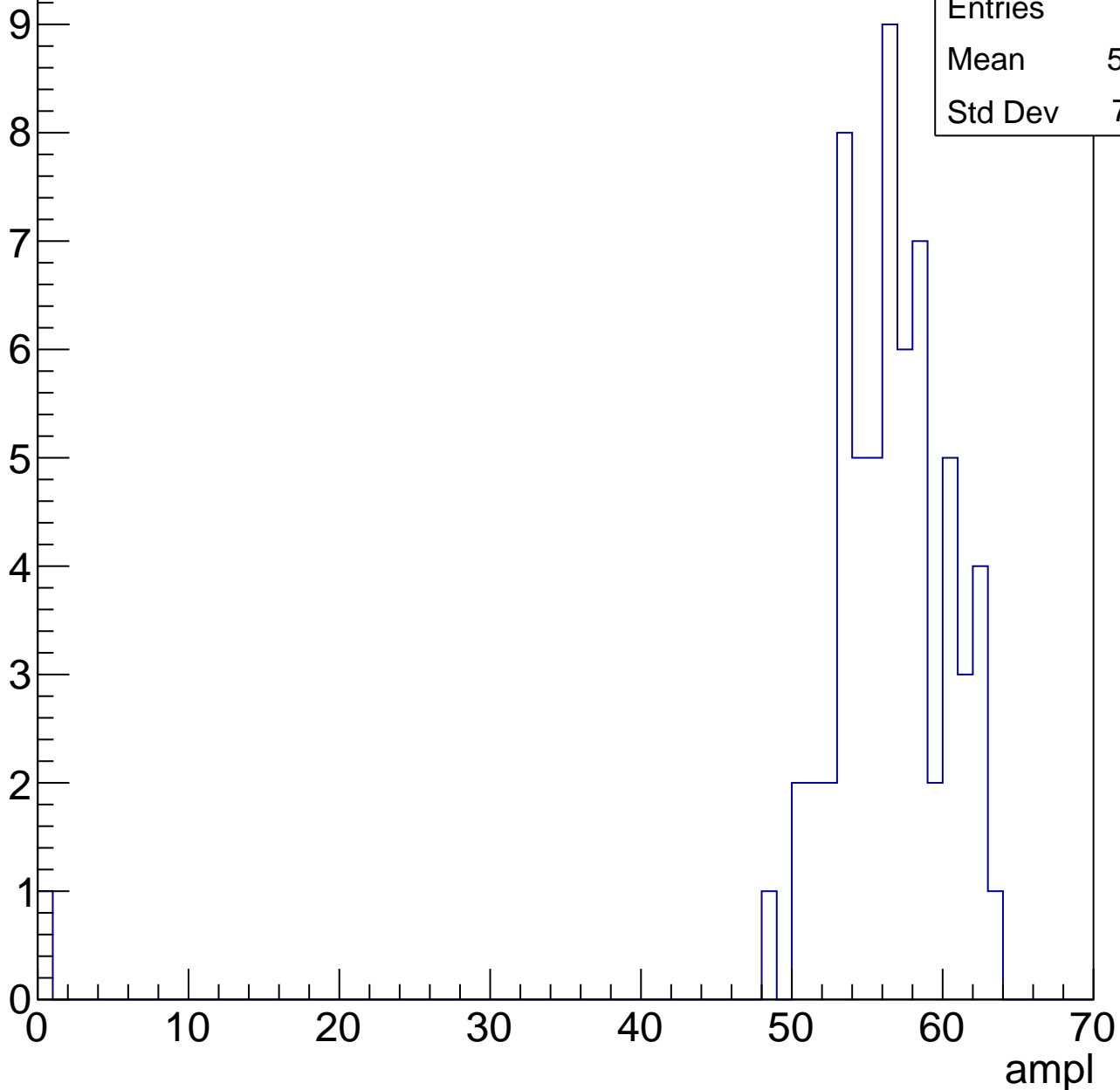


B1L103S, U9-ch63, adc4

calib_packv5_041523_1651.root, FC#0, port C2

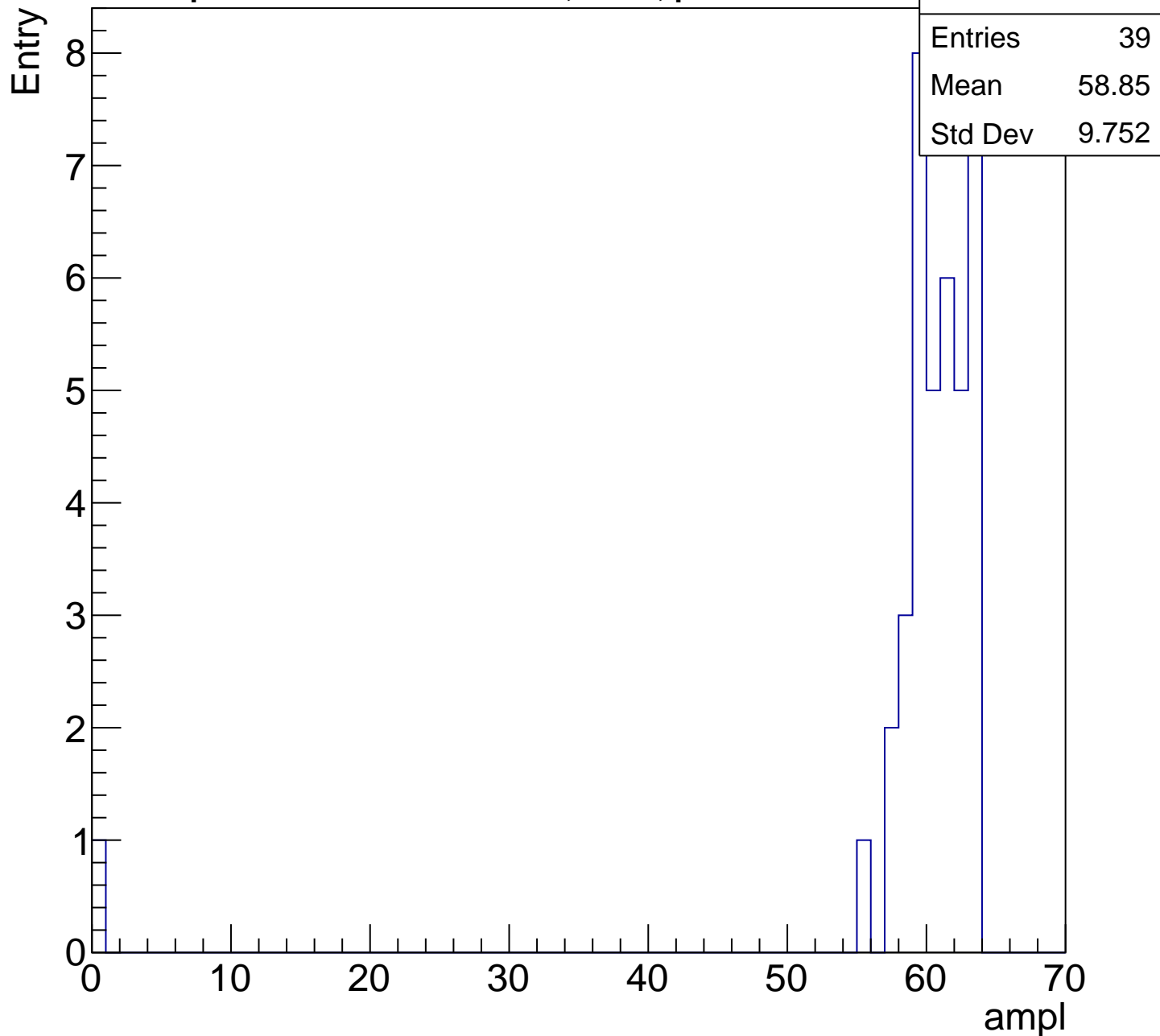
Entry

Entries	63
Mean	55.35
Std Dev	7.791



B1L103S, U9-ch63, adc5

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U9-ch63, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch63, adc7

calib_packv5_041523_1651.root, FC#0, port C2

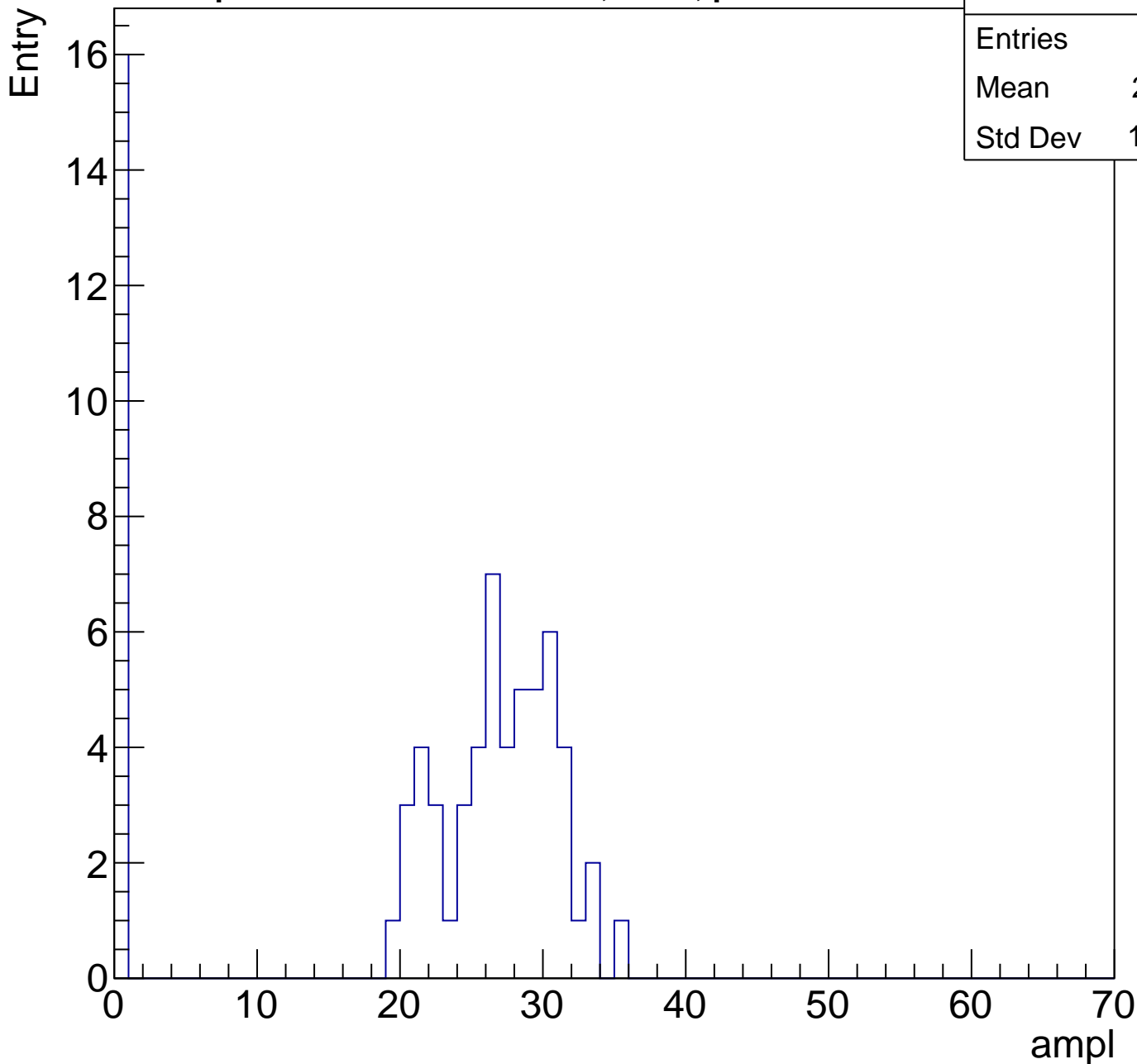
Entry



B1L103S, U9-ch64, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	70
Mean	20.51
Std Dev	11.66

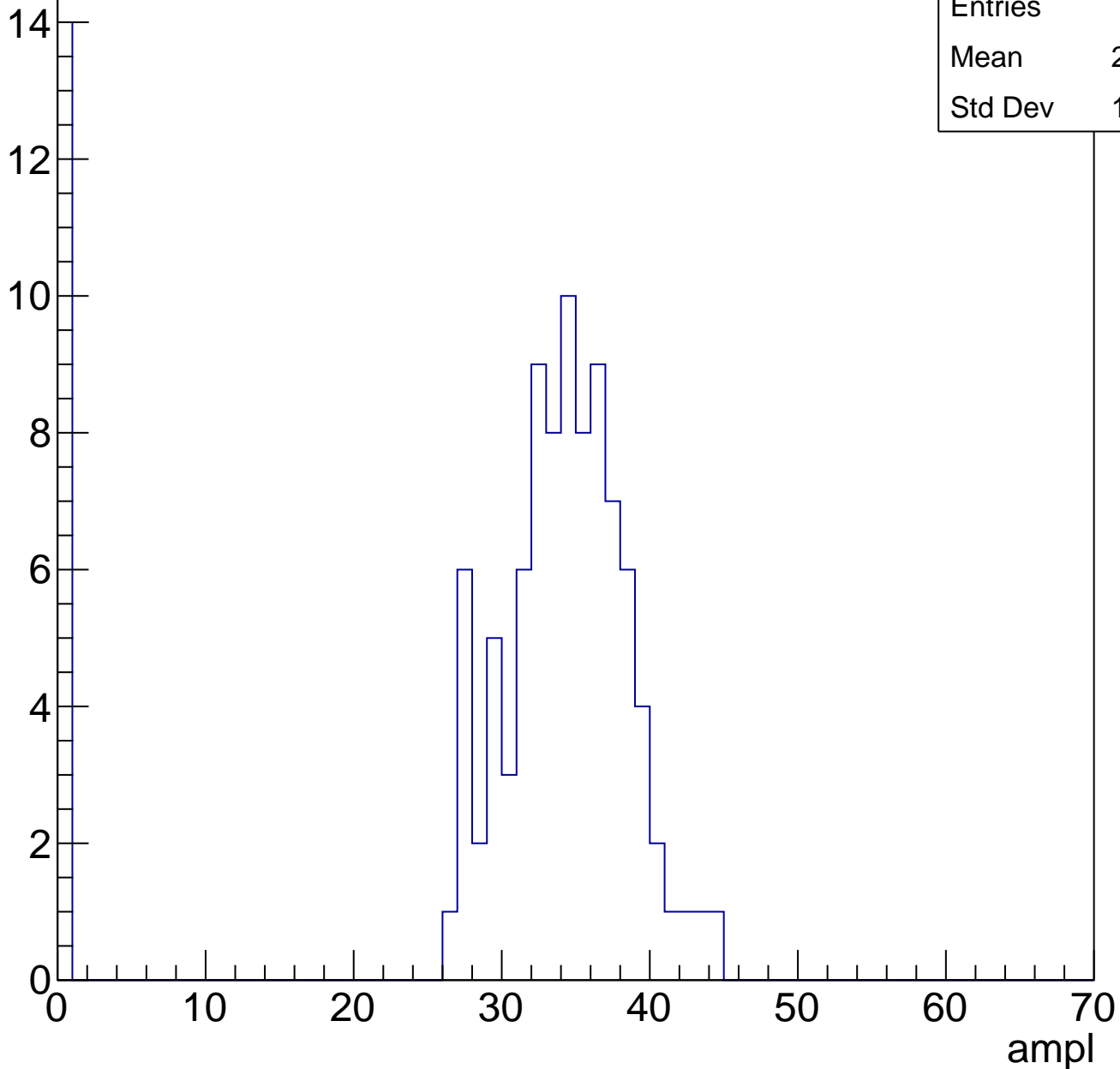


B1L103S, U9-ch64, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	104
Mean	29.37
Std Dev	12.14

Entry

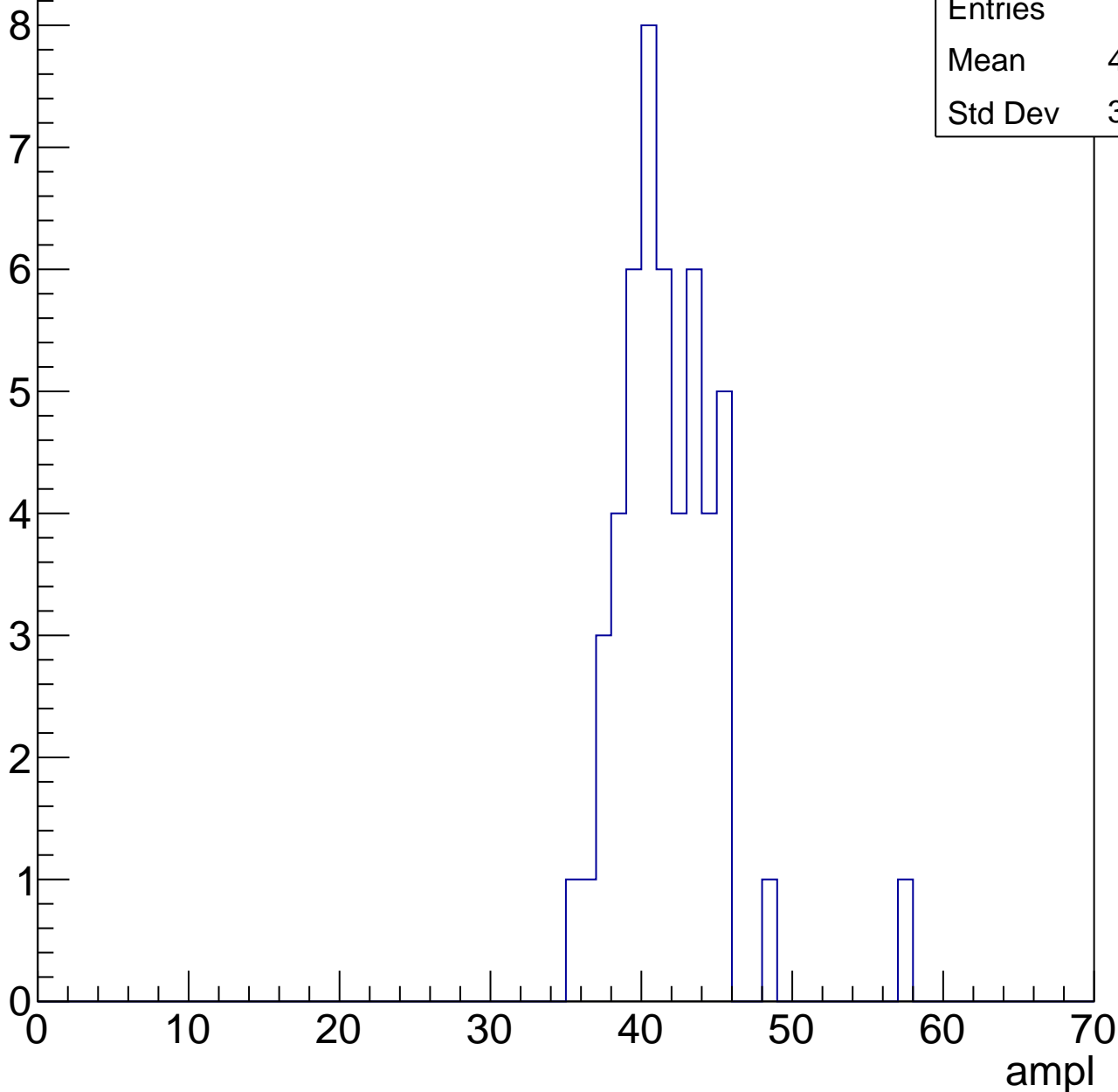


B1L103S, U9-ch64, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

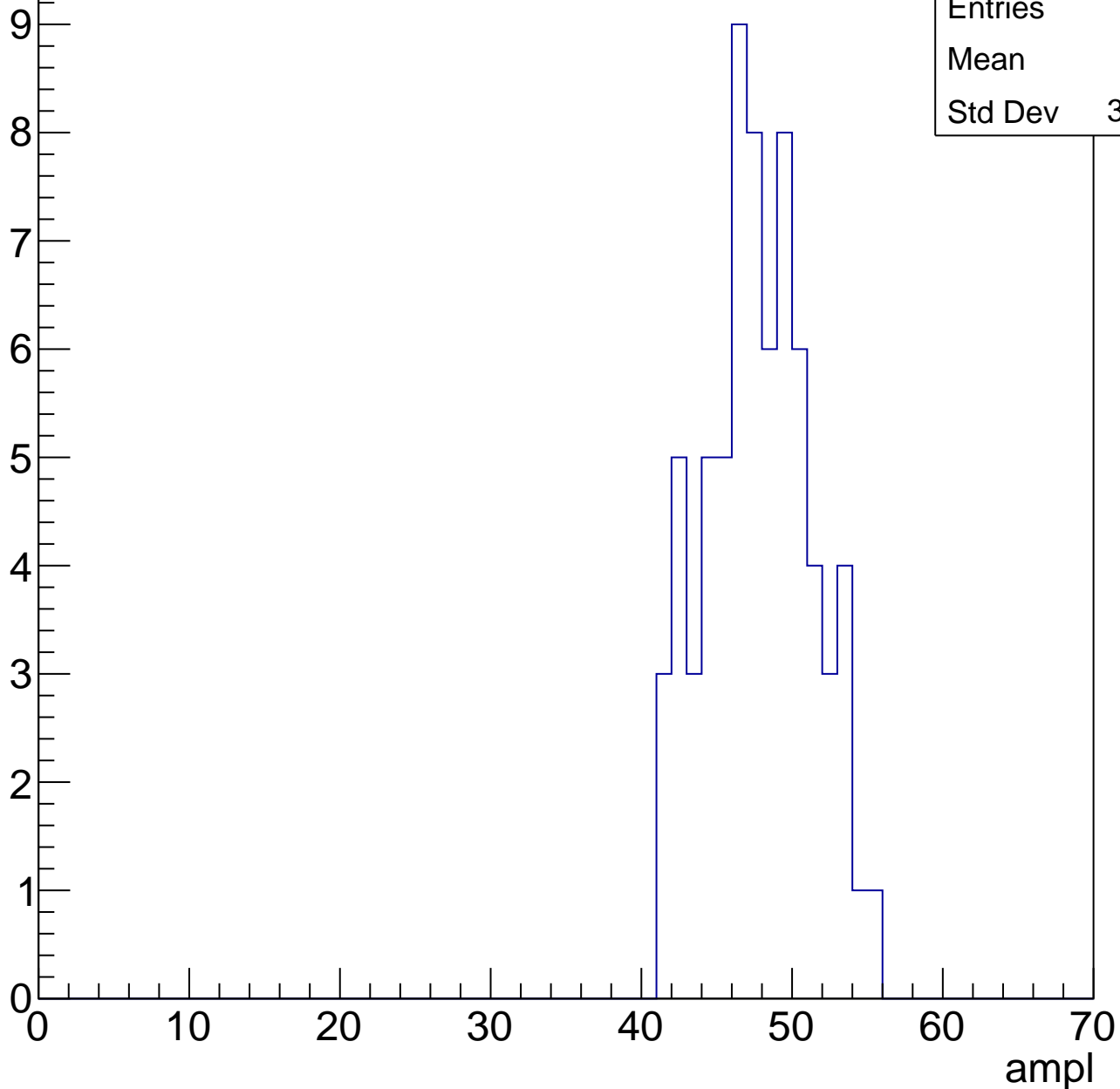
Entries	50
Mean	41.32
Std Dev	3.524



B1L103S, U9-ch64, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry



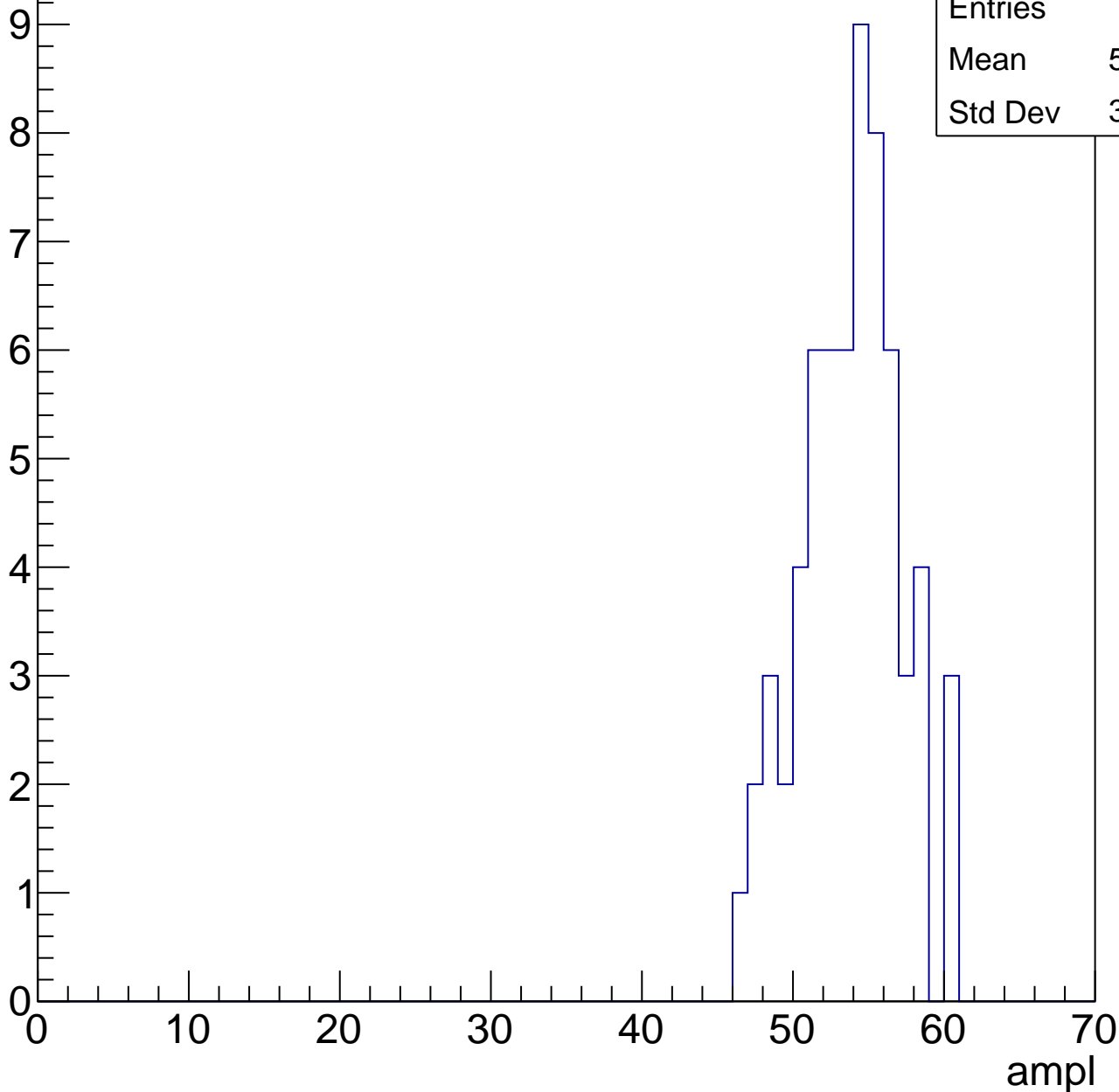
Entries	71
Mean	47.3
Std Dev	3.433

B1L103S, U9-ch64, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	53.38
Std Dev	3.273



B1L103S, U9-ch64, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entries	51
Mean	58.22
Std Dev	8.583

Entry

10

8

6

4

2

0

0

10

20

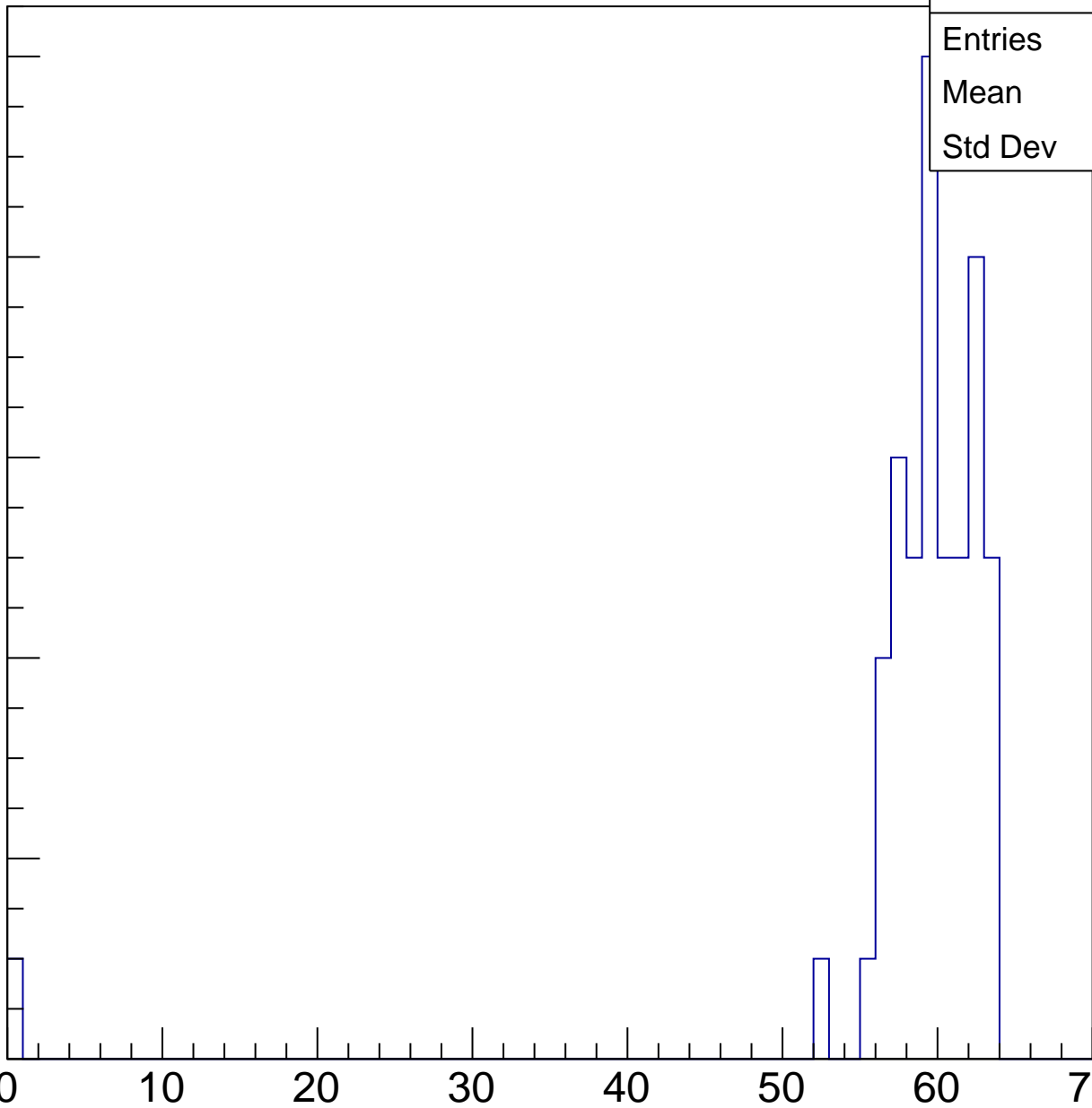
30

40

50

60

ampl

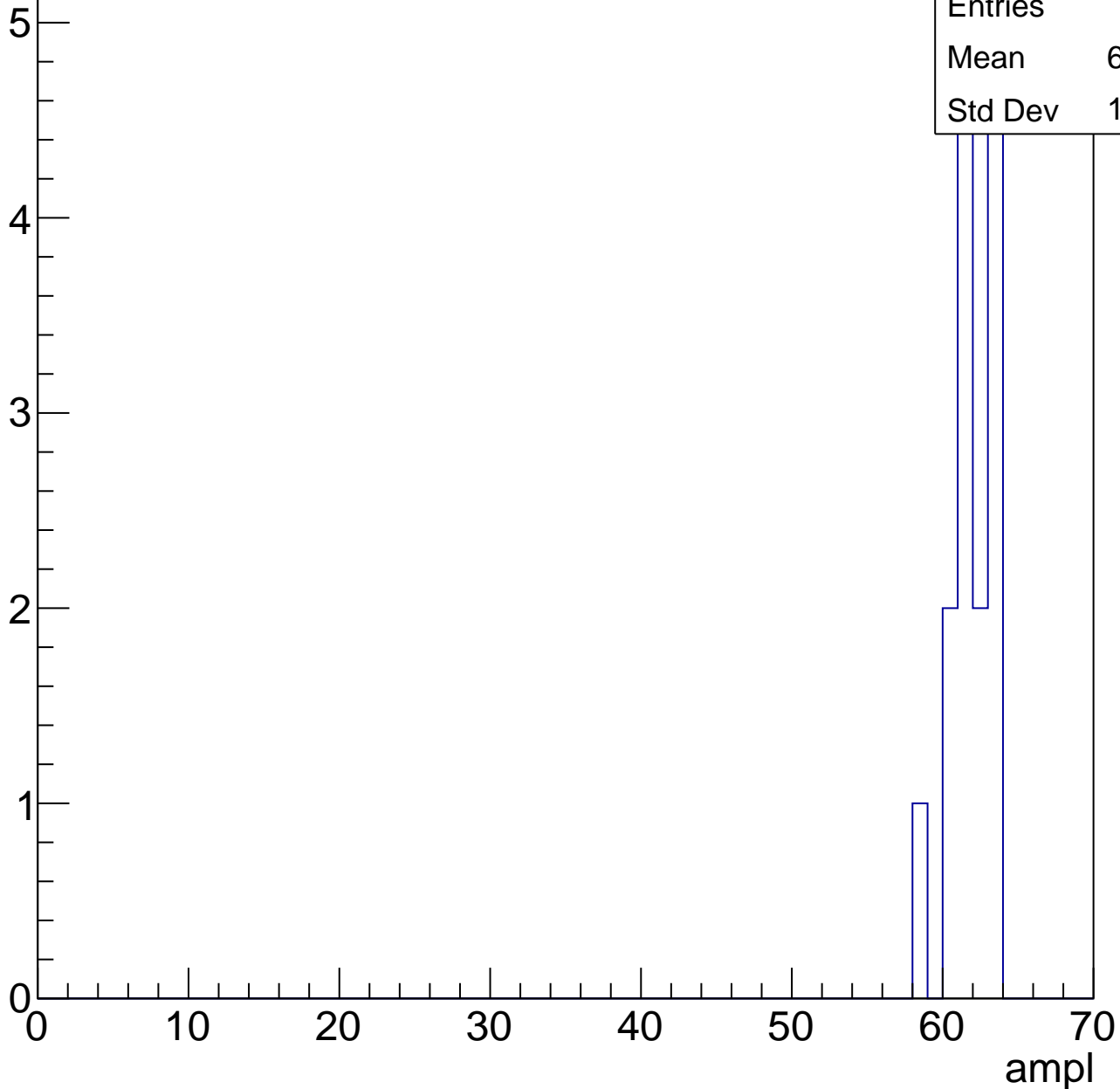


B1L103S, U9-ch64, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	15
Mean	61.47
Std Dev	1.408



B1L103S, U9-ch64, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



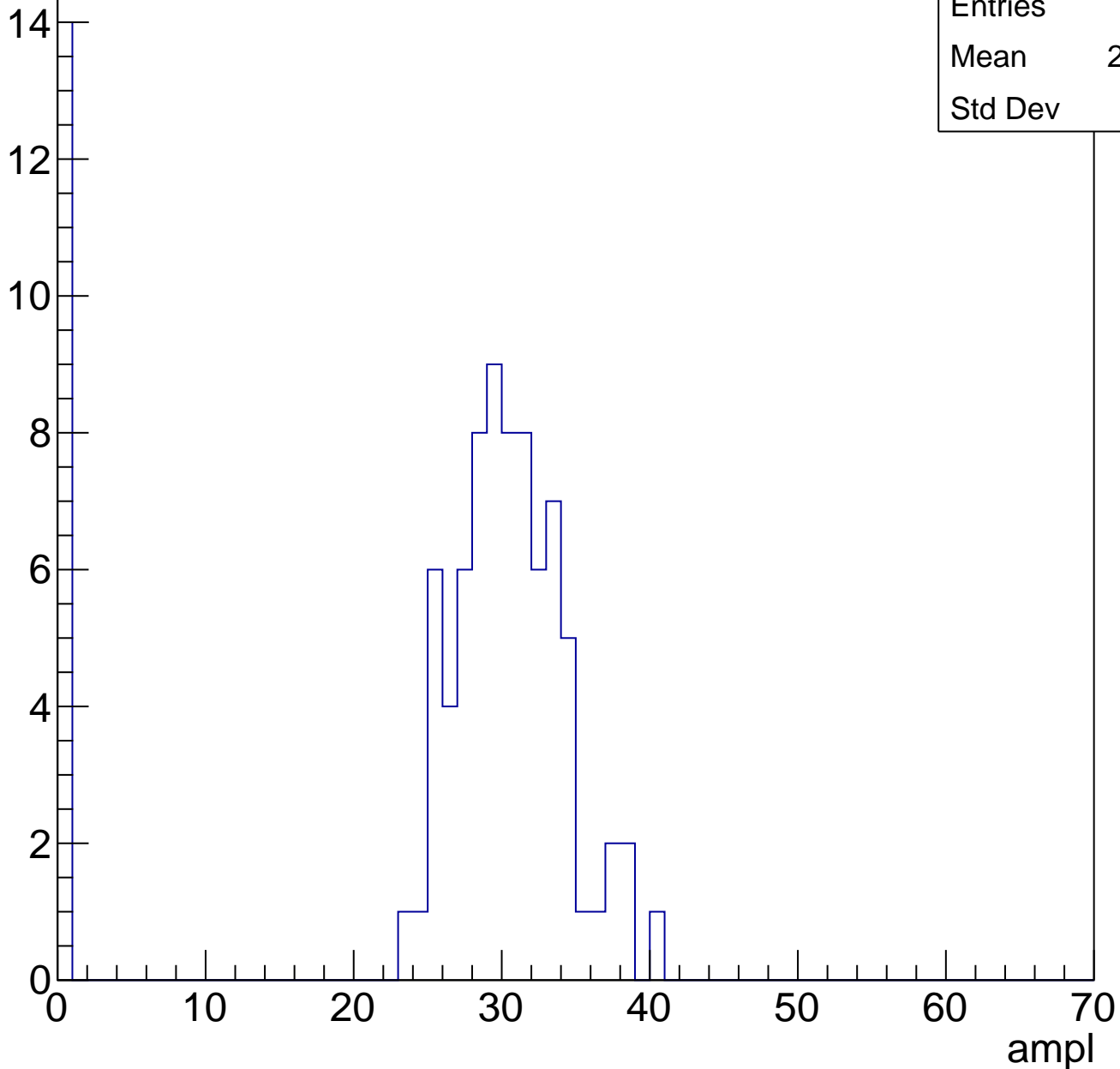
Entries	19
Mean	0
Std Dev	0

B1L103S, U9-ch65, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	90
Mean	25.44
Std Dev	11.4

Entry

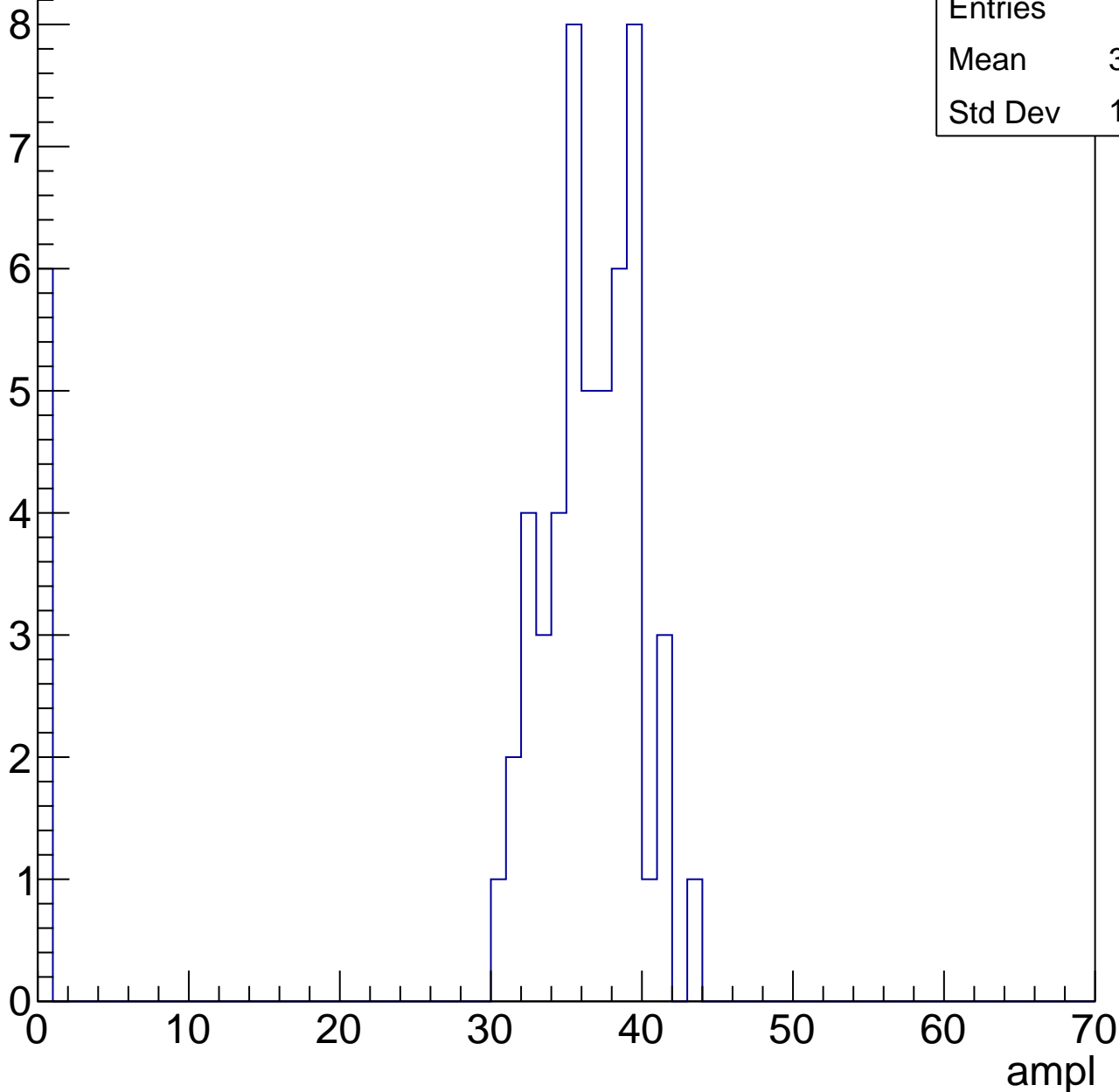


B1L103S, U9-ch65, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	32.39
Std Dev	11.45

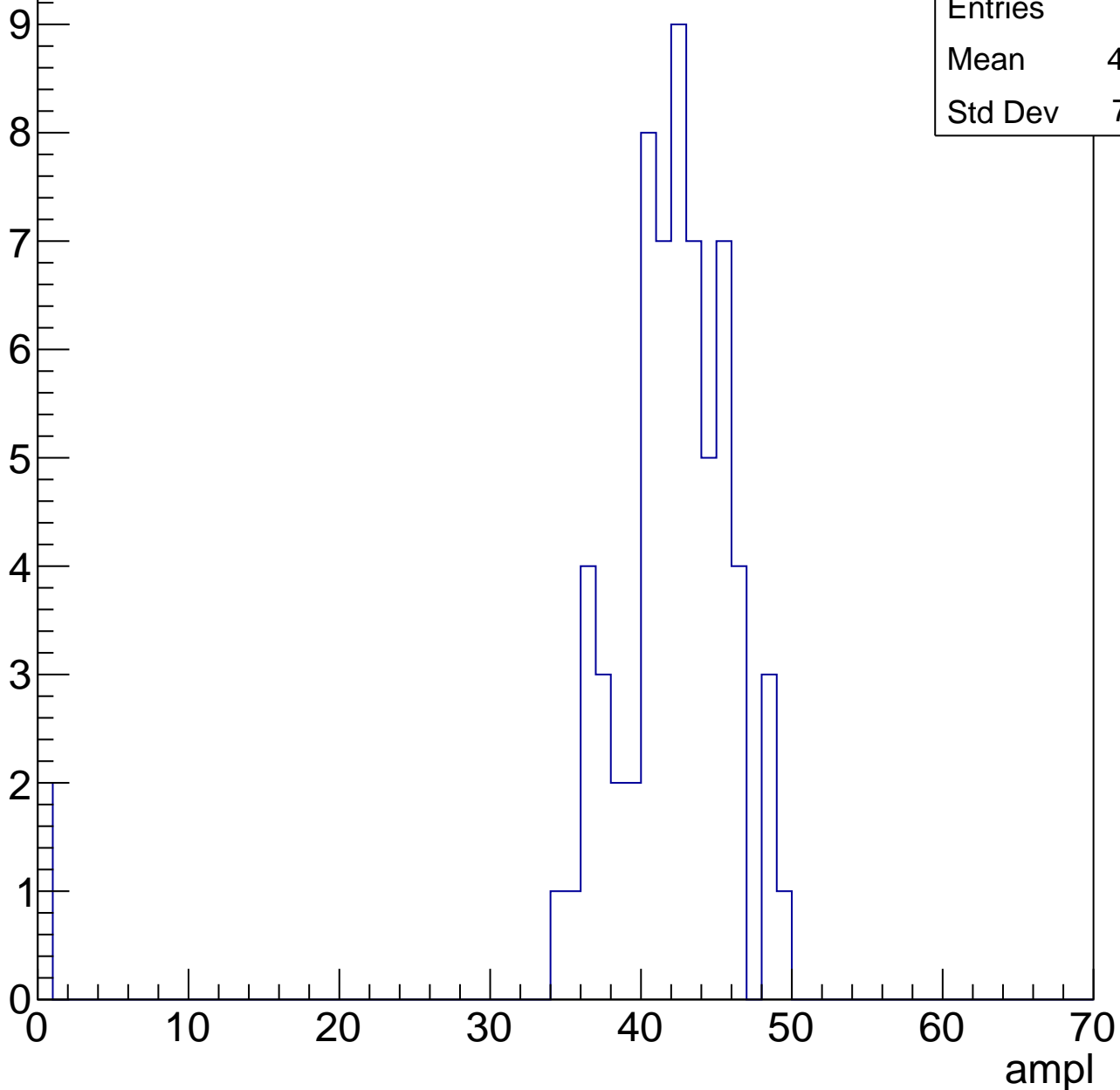


B1L103S, U9-ch65, adc2

calib_packv5_041523_1651.root, FC#0, port C2

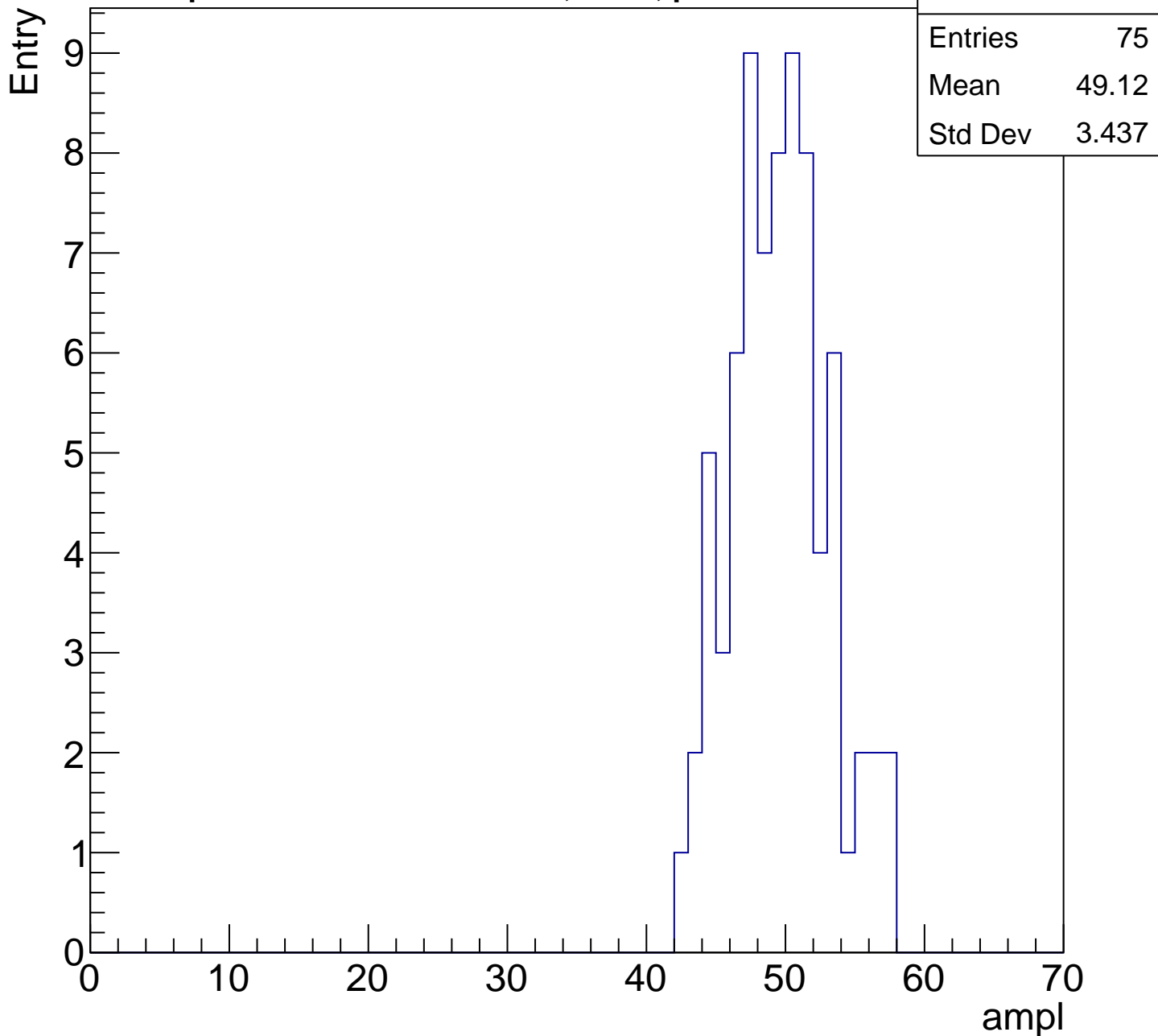
Entry

Entries	66
Mean	40.55
Std Dev	7.901



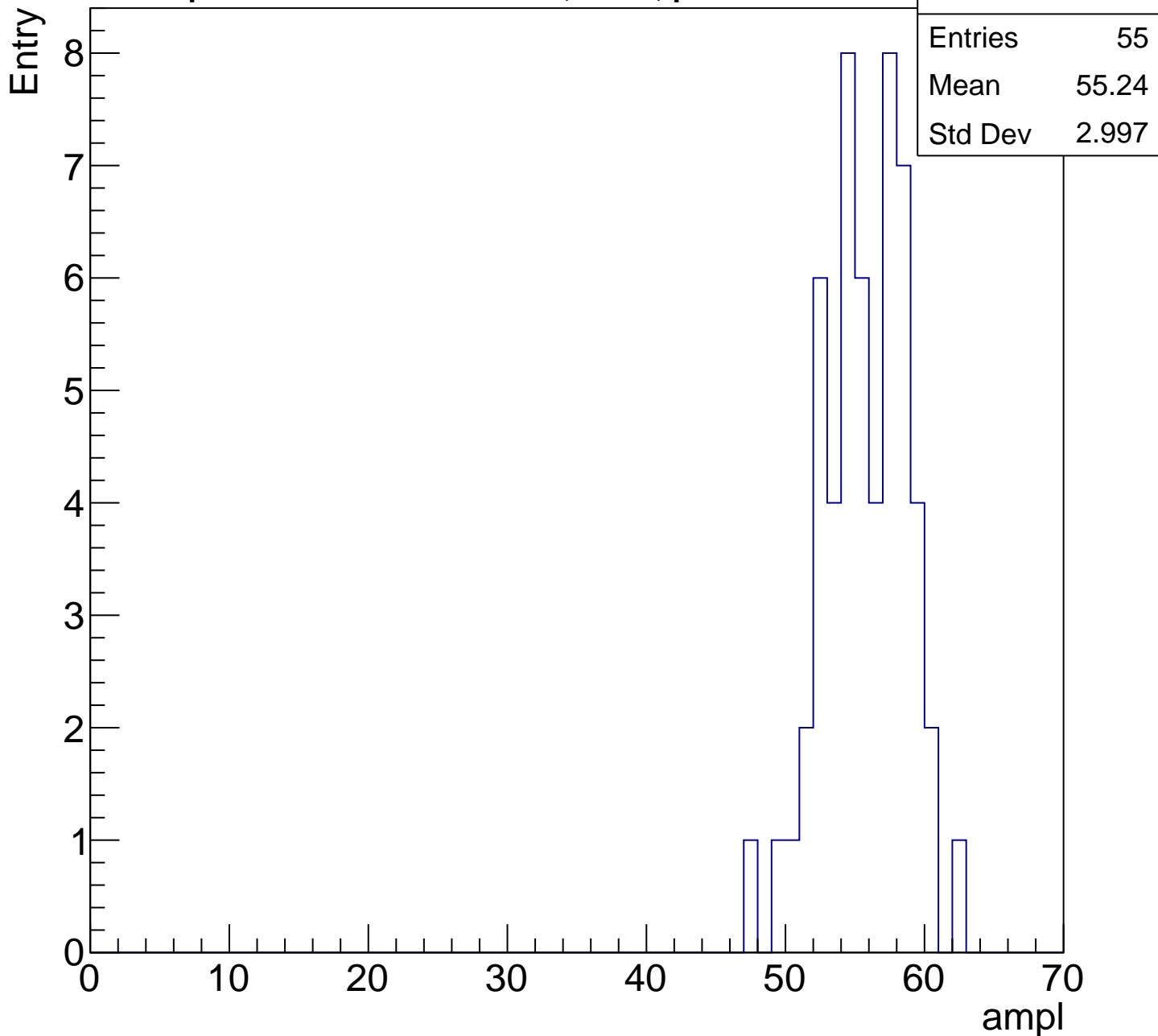
B1L103S, U9-ch65, adc3

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U9-ch65, adc4

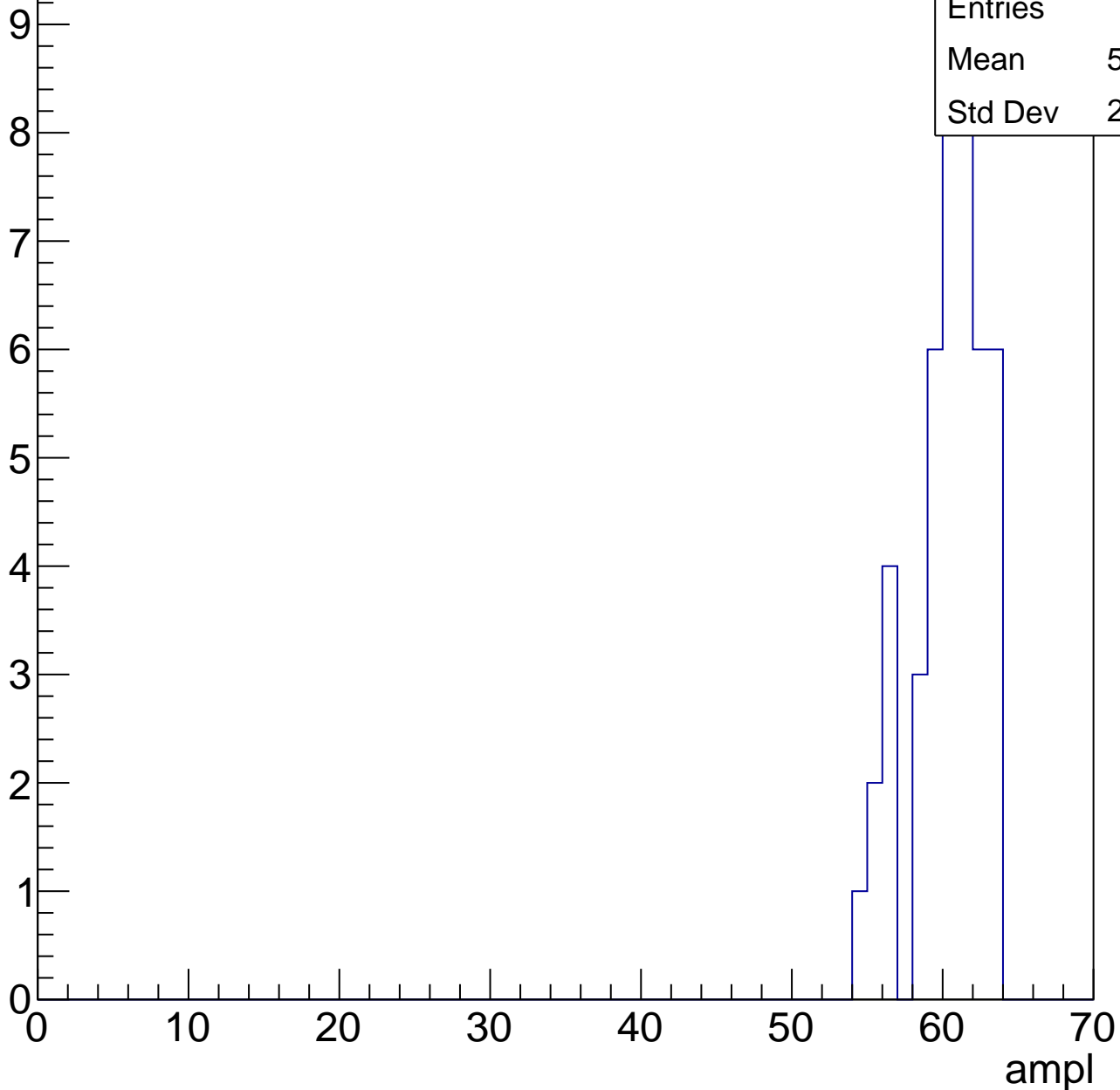
calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U9-ch65, adc5

calib_packv5_041523_1651.root, FC#0, port C2

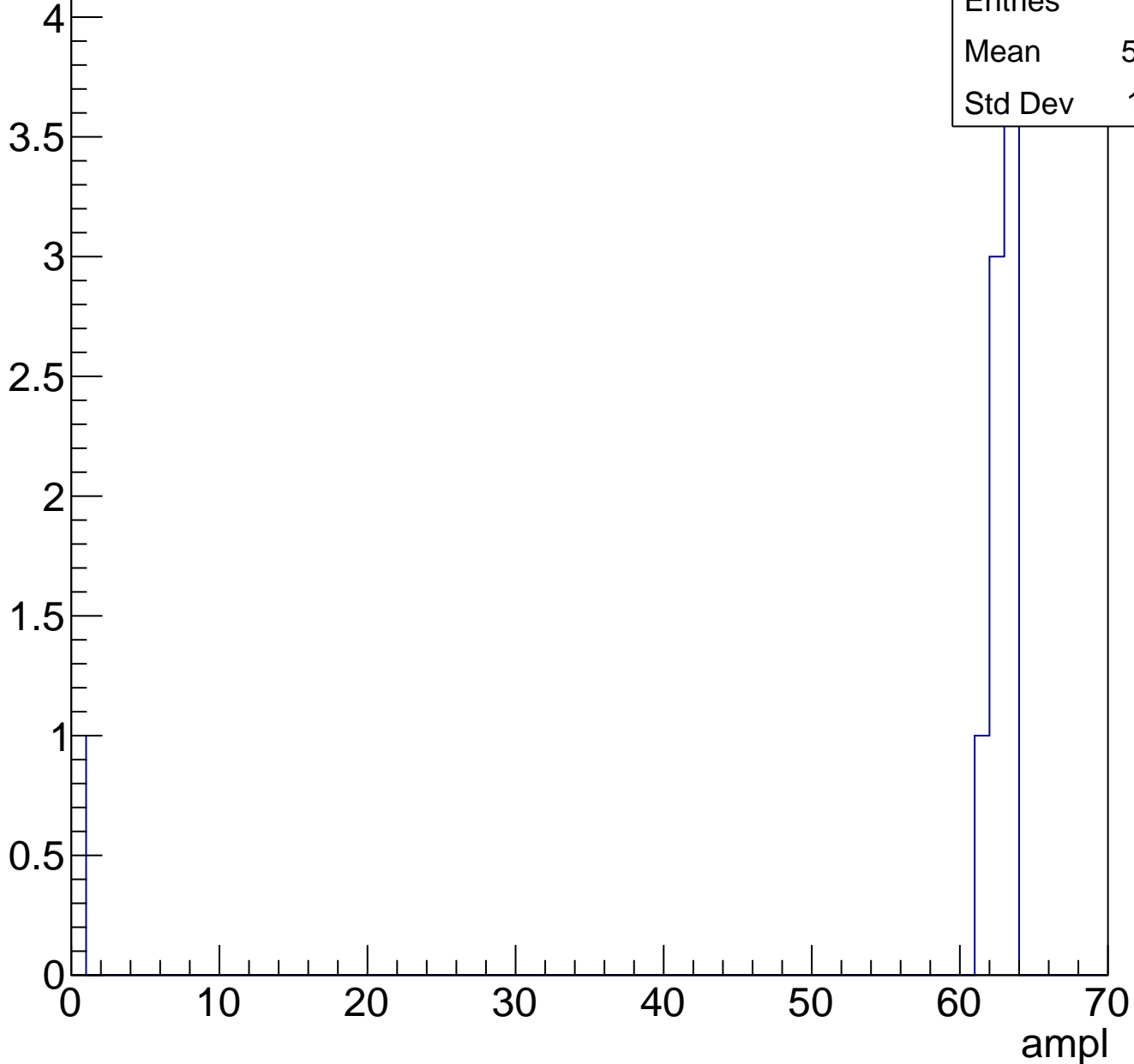
Entry



B1L103S, U9-ch65, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch65, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	18
Mean	0
Std Dev	0

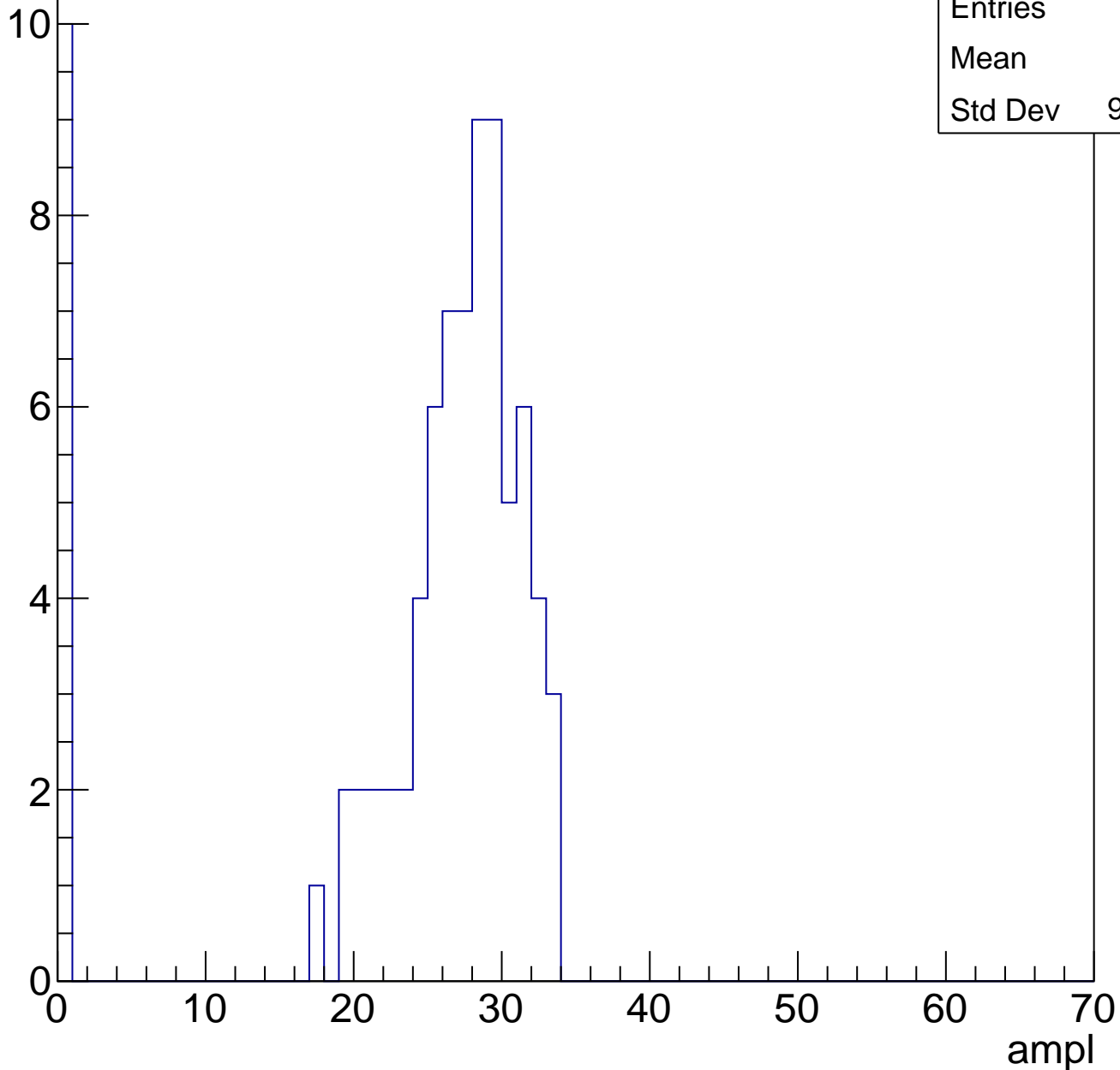
ampl

B1L103S, U9-ch66, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	23.7
Std Dev	9.526

Entry



B1L103S, U9-ch66, adc1

calib_packv5_041523_1651.root, FC#0, port C2

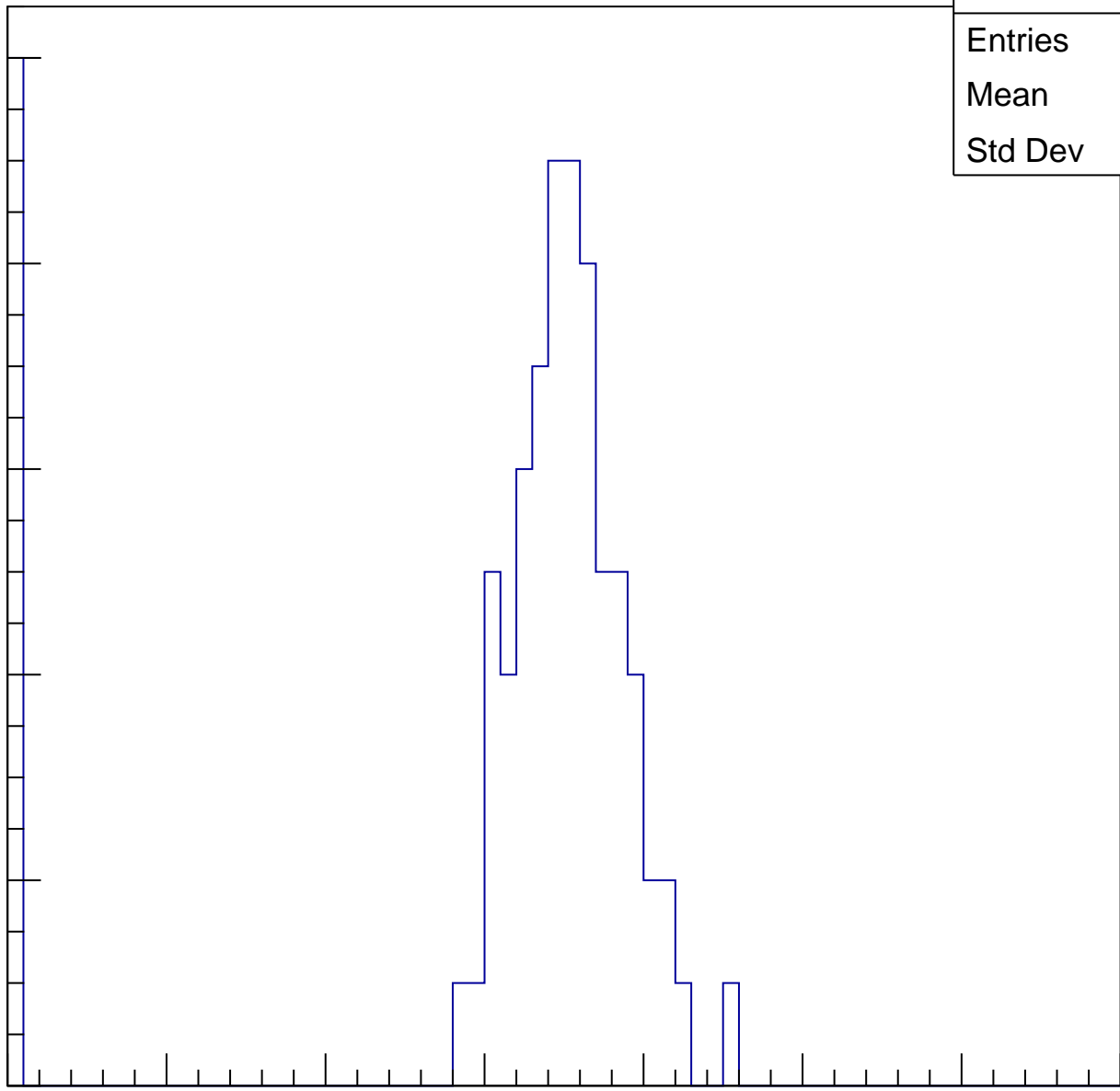
Entries	80
Mean	30.54
Std Dev	11.95

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

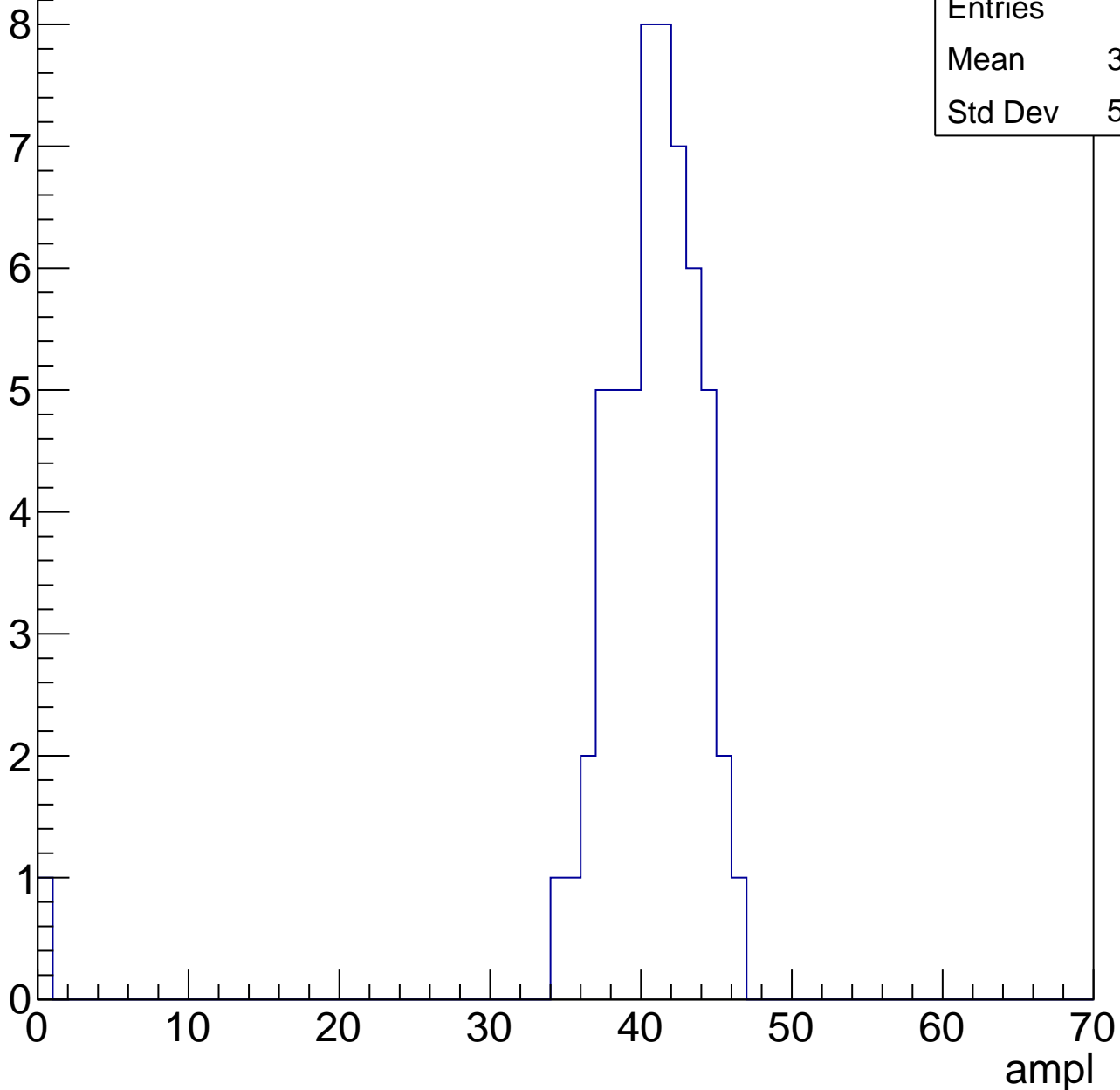


B1L103S, U9-ch66, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	39.77
Std Dev	5.947



B1L103S, U9-ch66, adc3

calib_packv5_041523_1651.root, FC#0, port C2

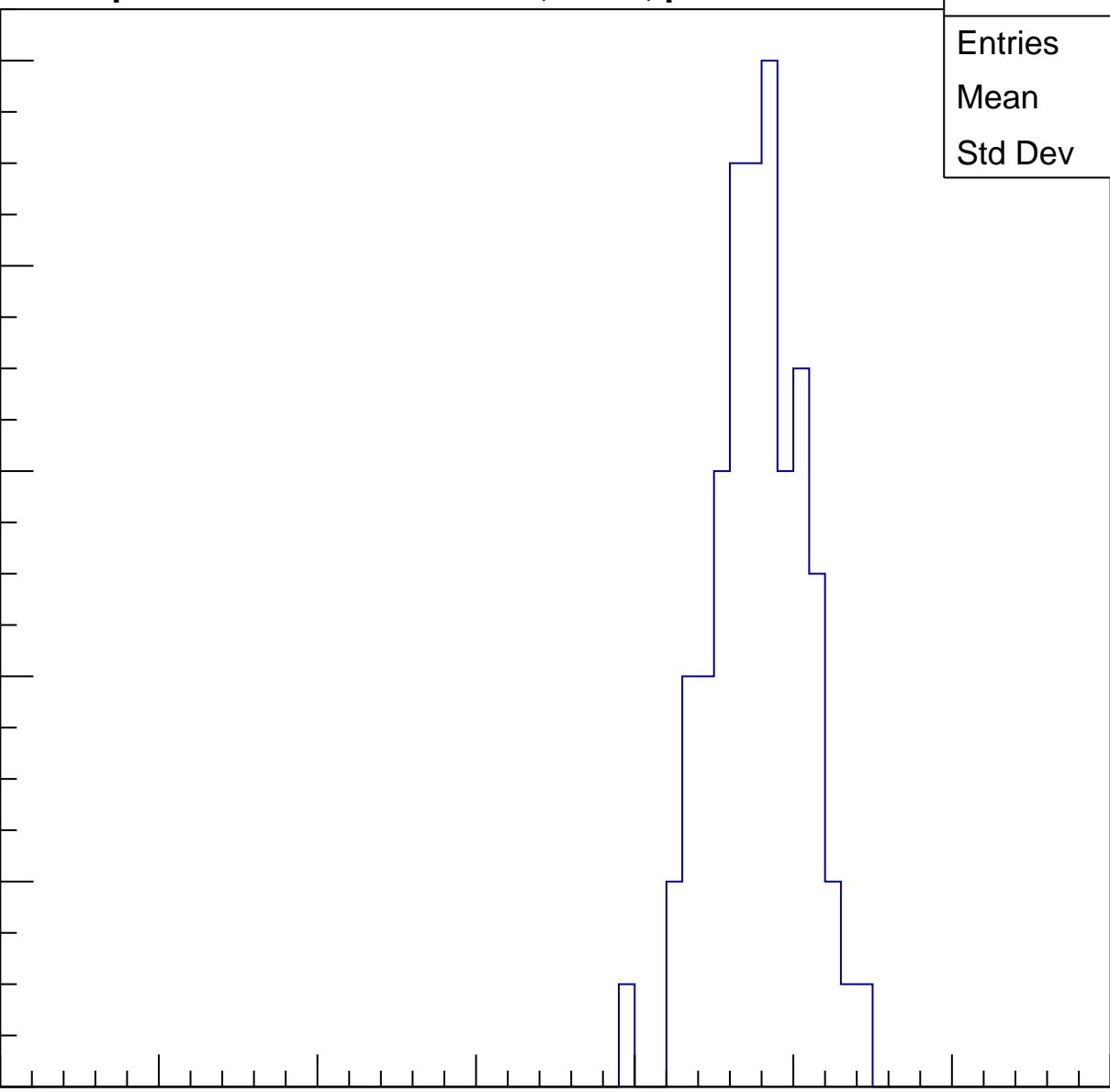
Entries	67
Mean	47.28
Std Dev	2.875

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

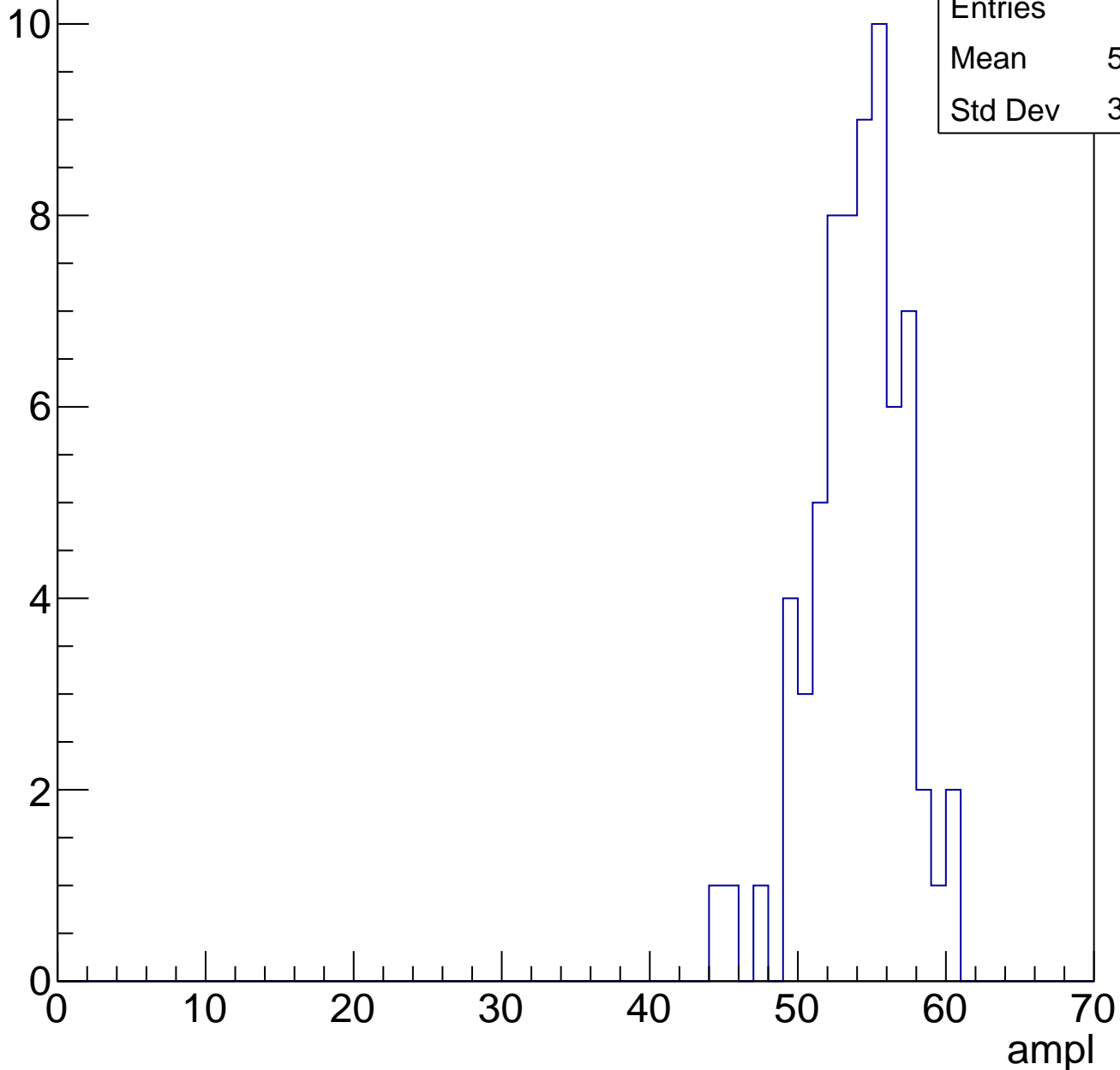


B1L103S, U9-ch66, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	68
Mean	53.57
Std Dev	3.154

Entry

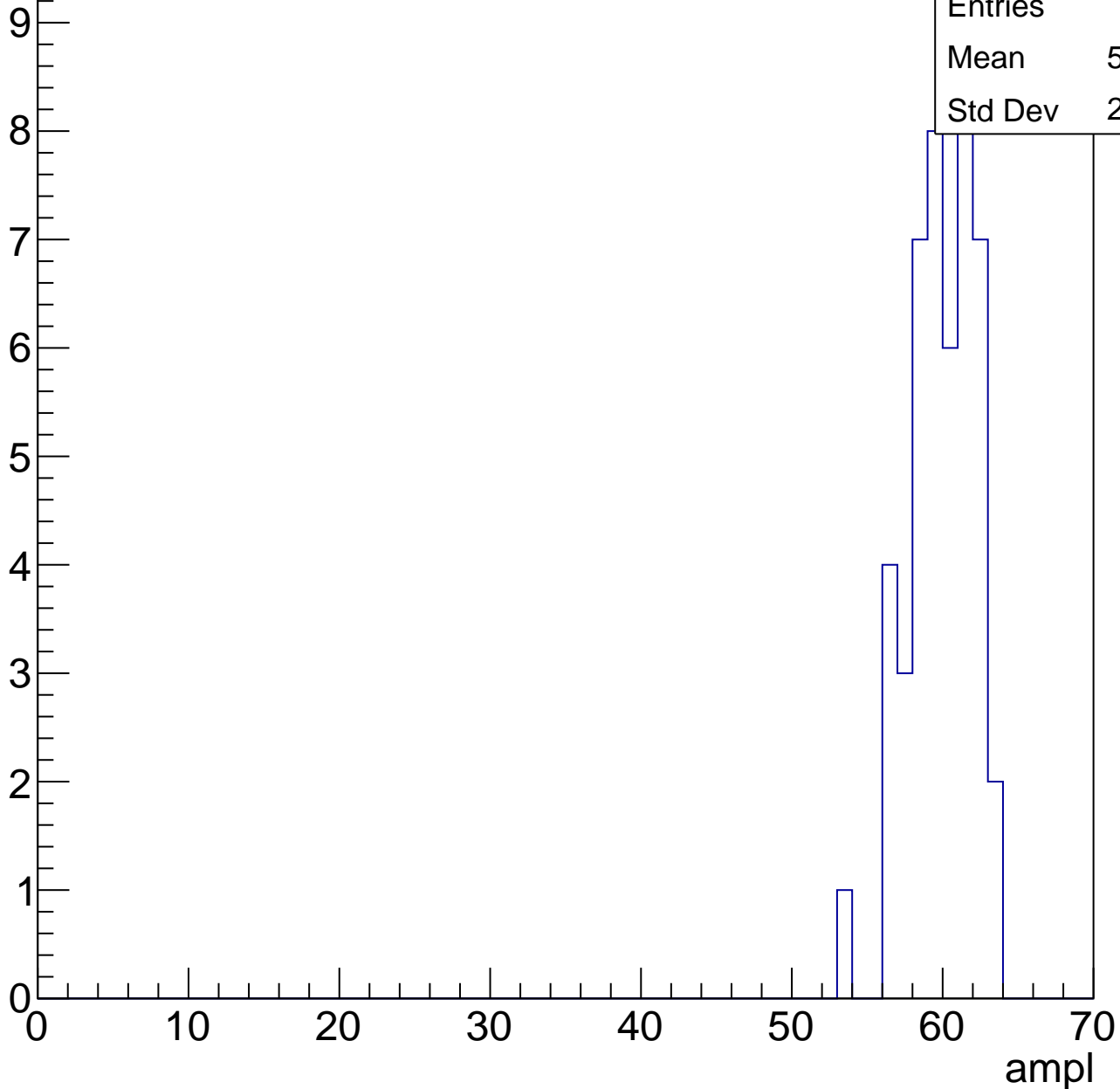


B1L103S, U9-ch66, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	47
Mean	59.47
Std Dev	2.152

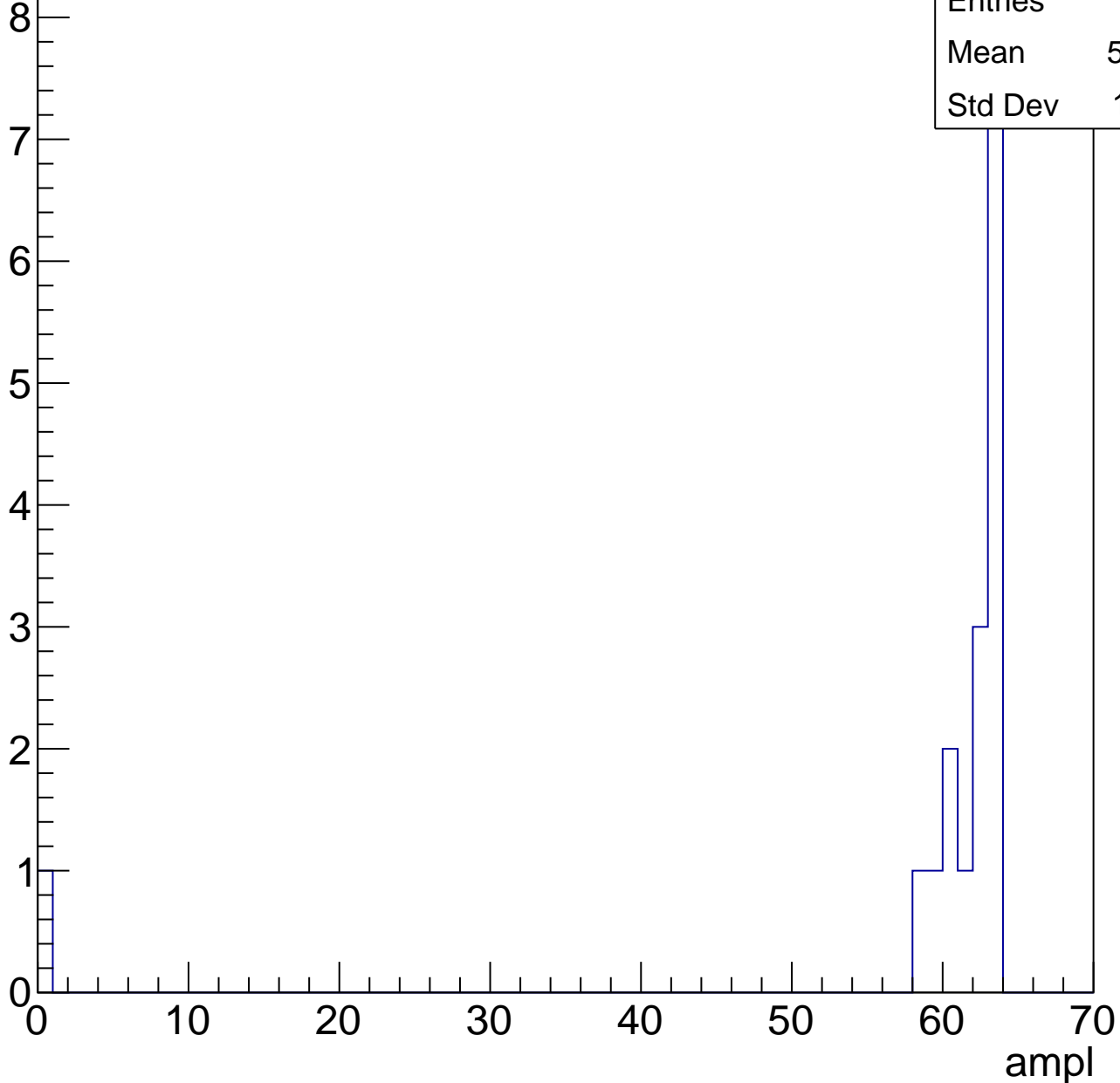


B1L103S, U9-ch66, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	17
Mean	58.12
Std Dev	14.61



B1L103S, U9-ch66, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

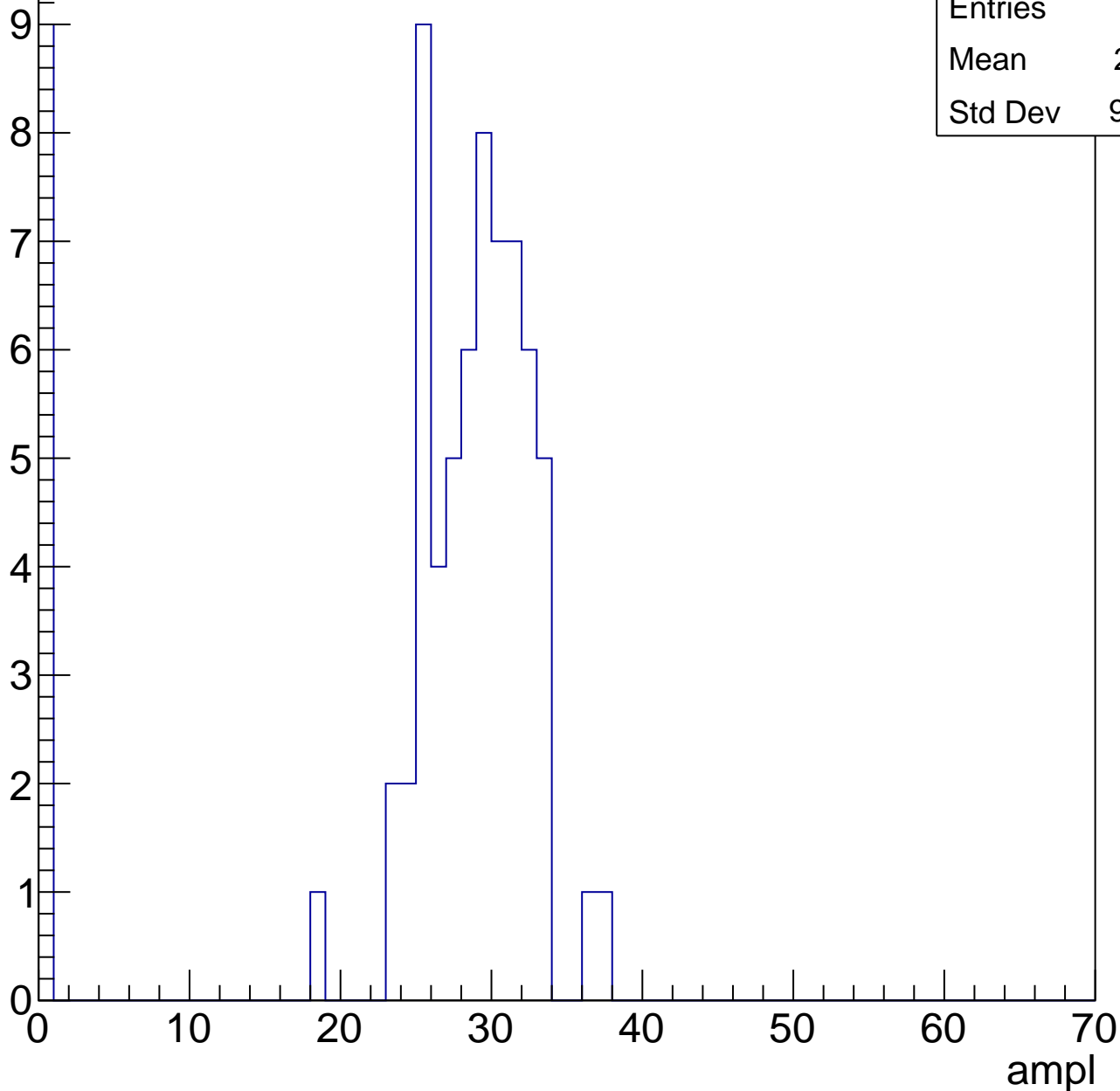
Entries	19
Mean	0
Std Dev	0

B1L103S, U9-ch67, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	25.11
Std Dev	9.928

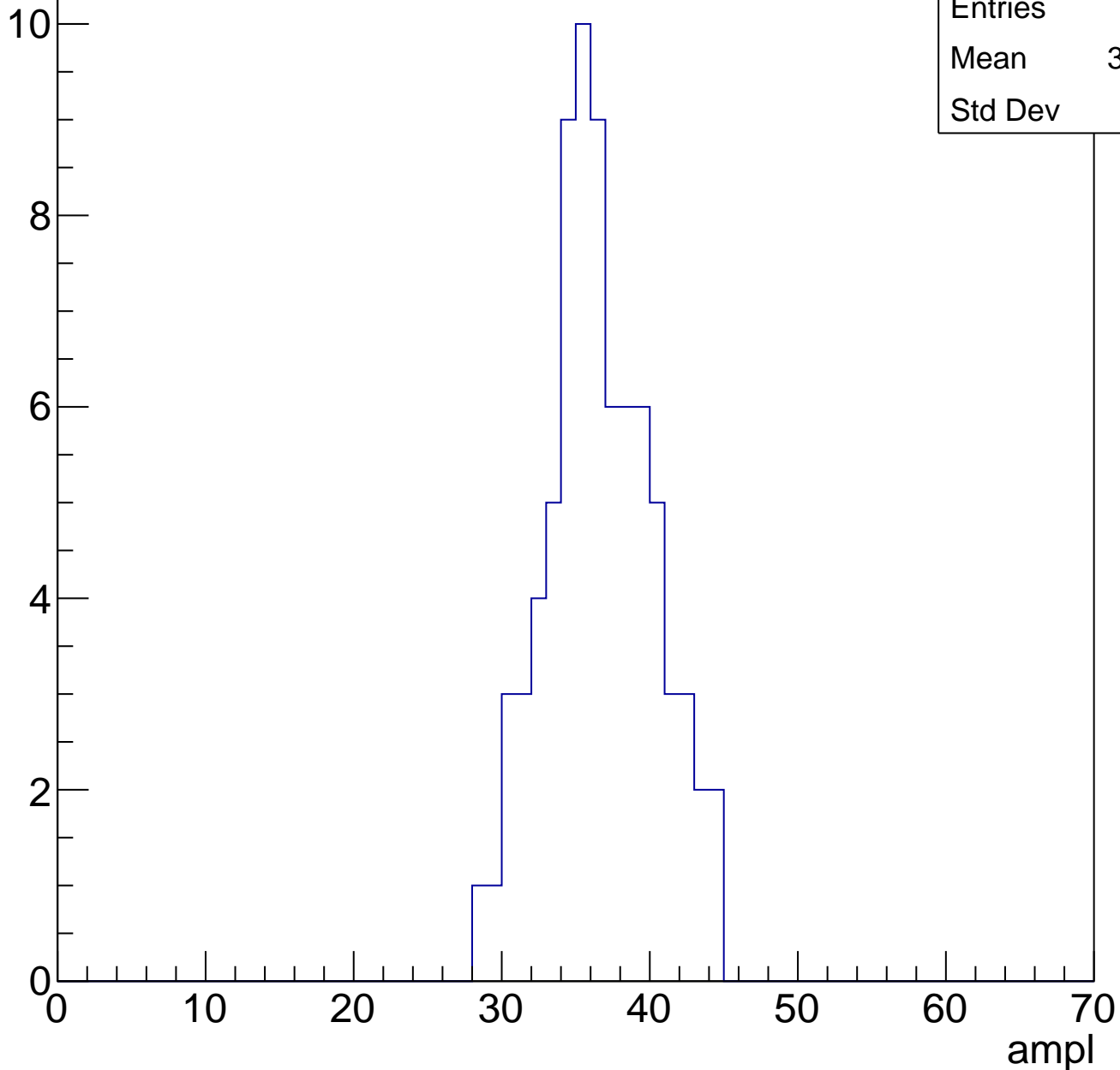


B1L103S, U9-ch67, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	78
Mean	36.15
Std Dev	3.62

Entry

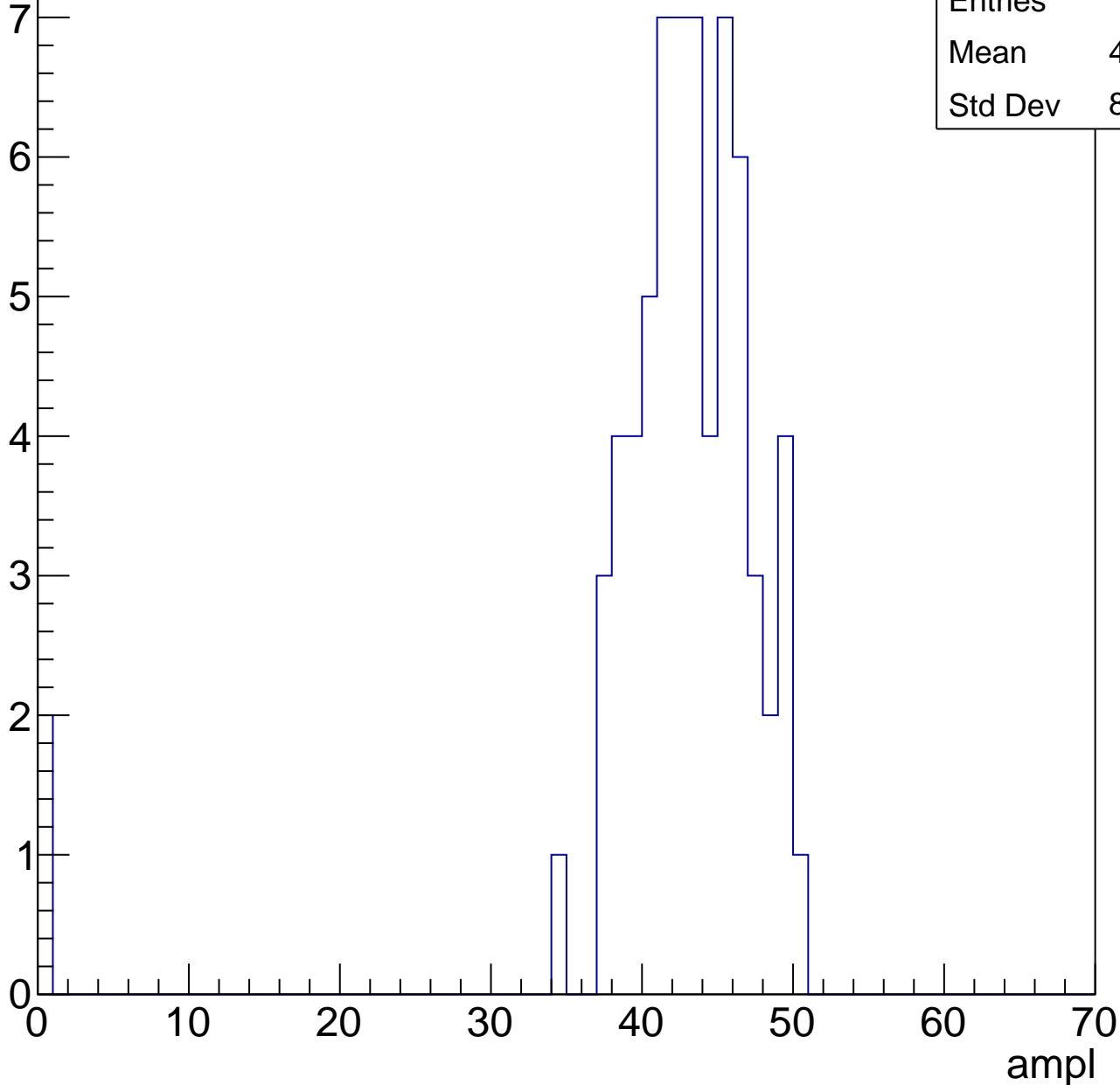


B1L103S, U9-ch67, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	41.57
Std Dev	8.077



B1L103S, U9-ch67, adc3

calib_packv5_041523_1651.root, FC#0, port C2

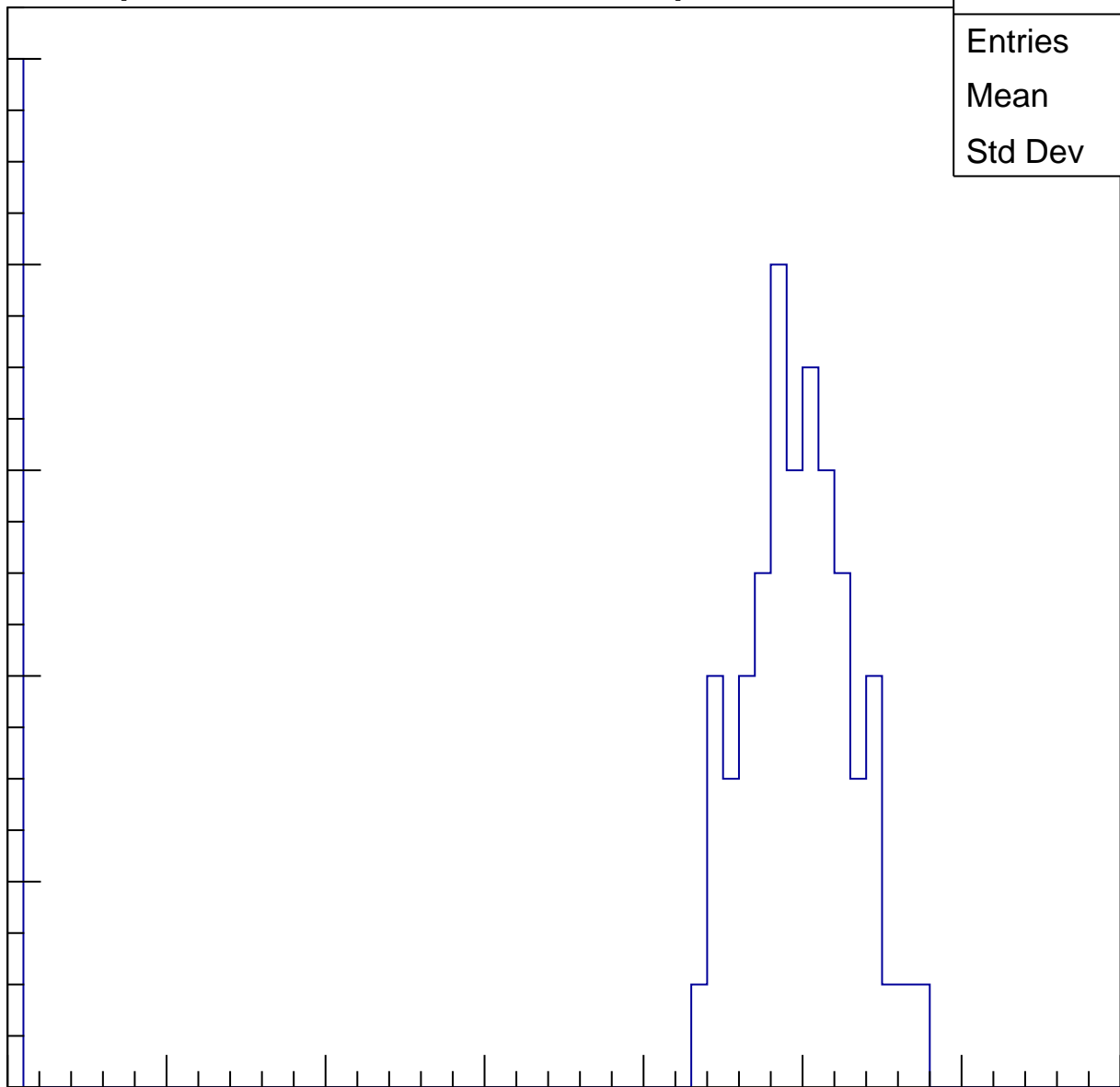
Entries	69
Mean	42.17
Std Dev	17.62

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

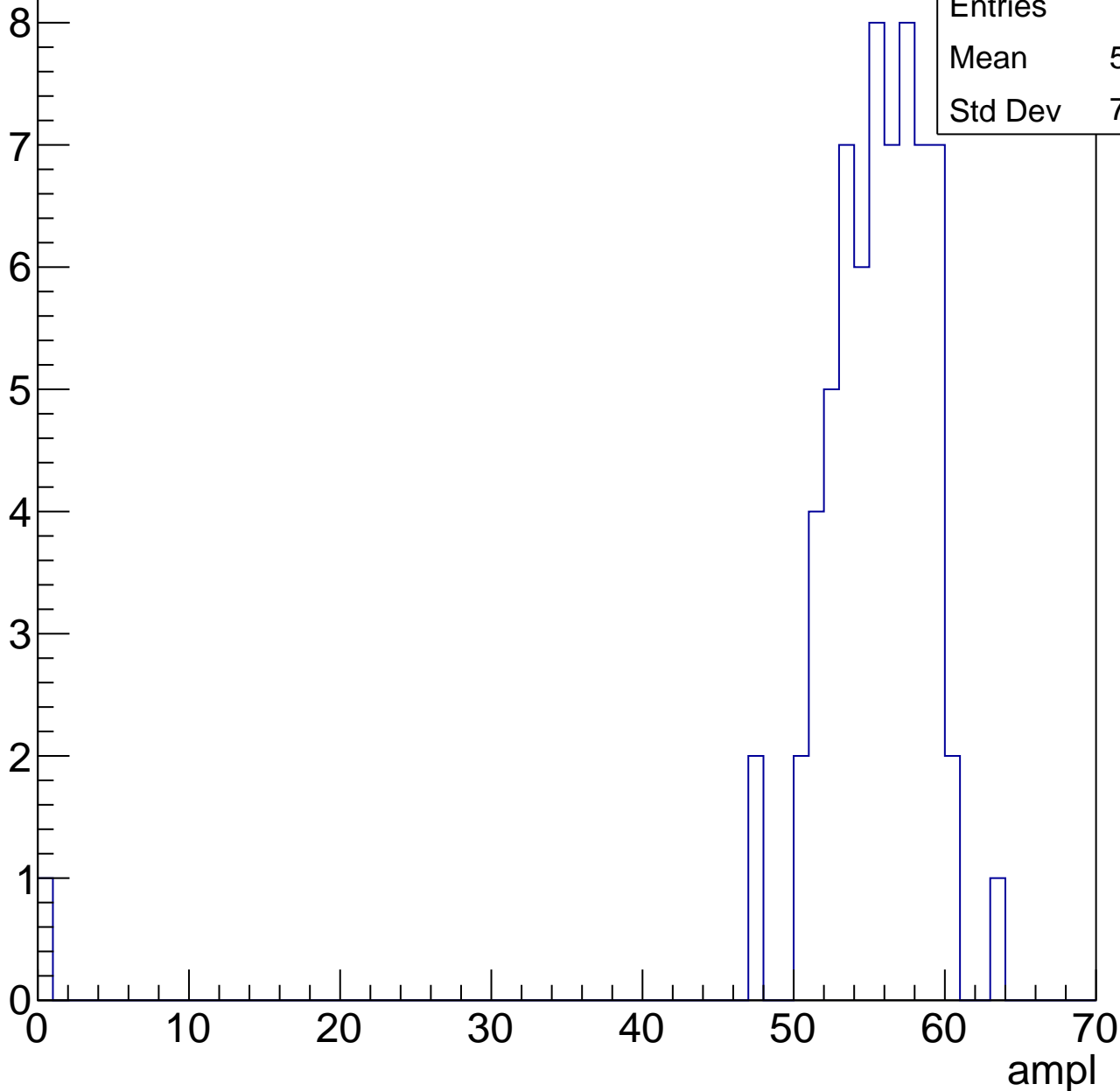


B1L103S, U9-ch67, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

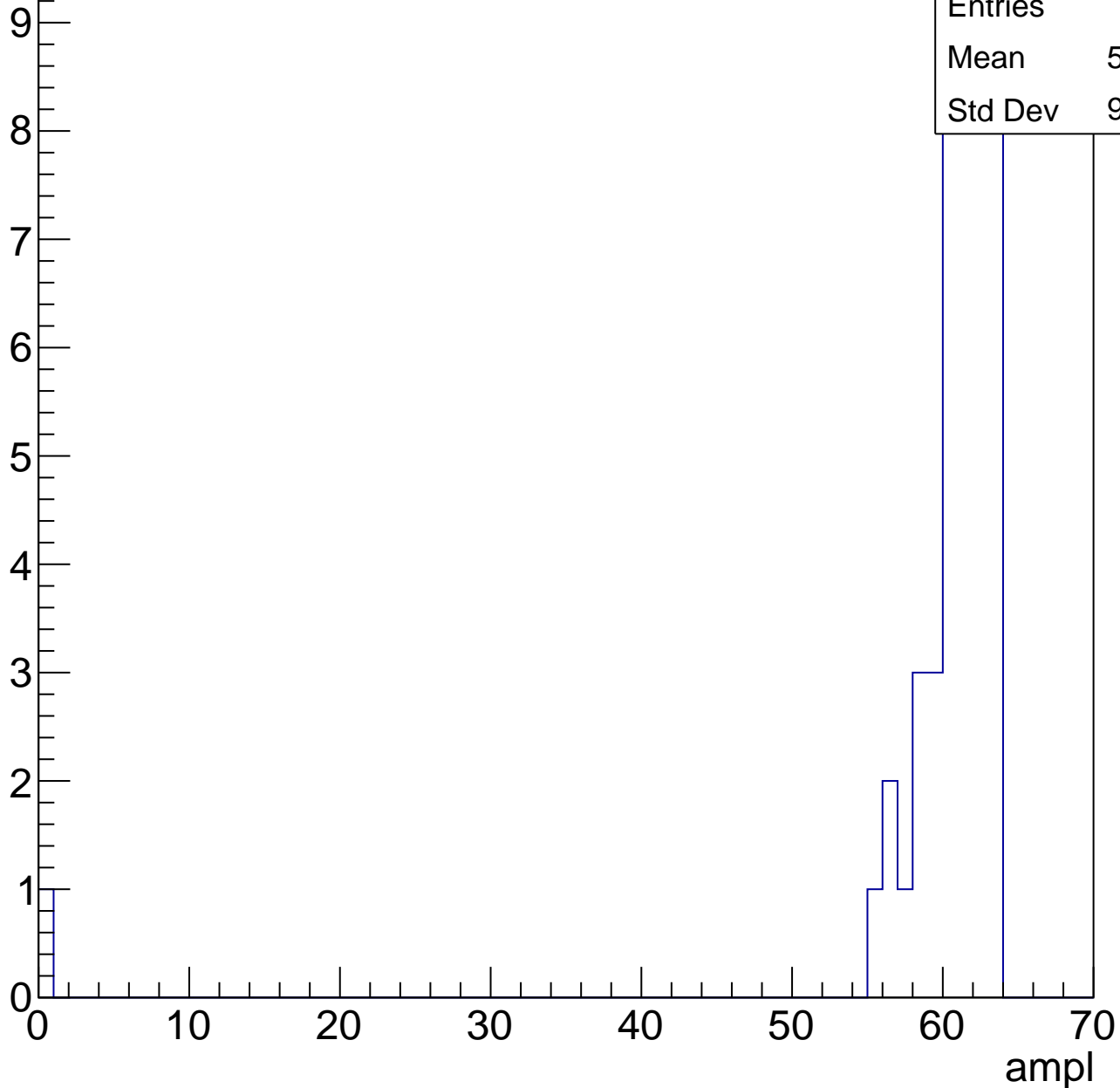
Entries	67
Mean	54.37
Std Dev	7.379



B1L103S, U9-ch67, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch67, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch67, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

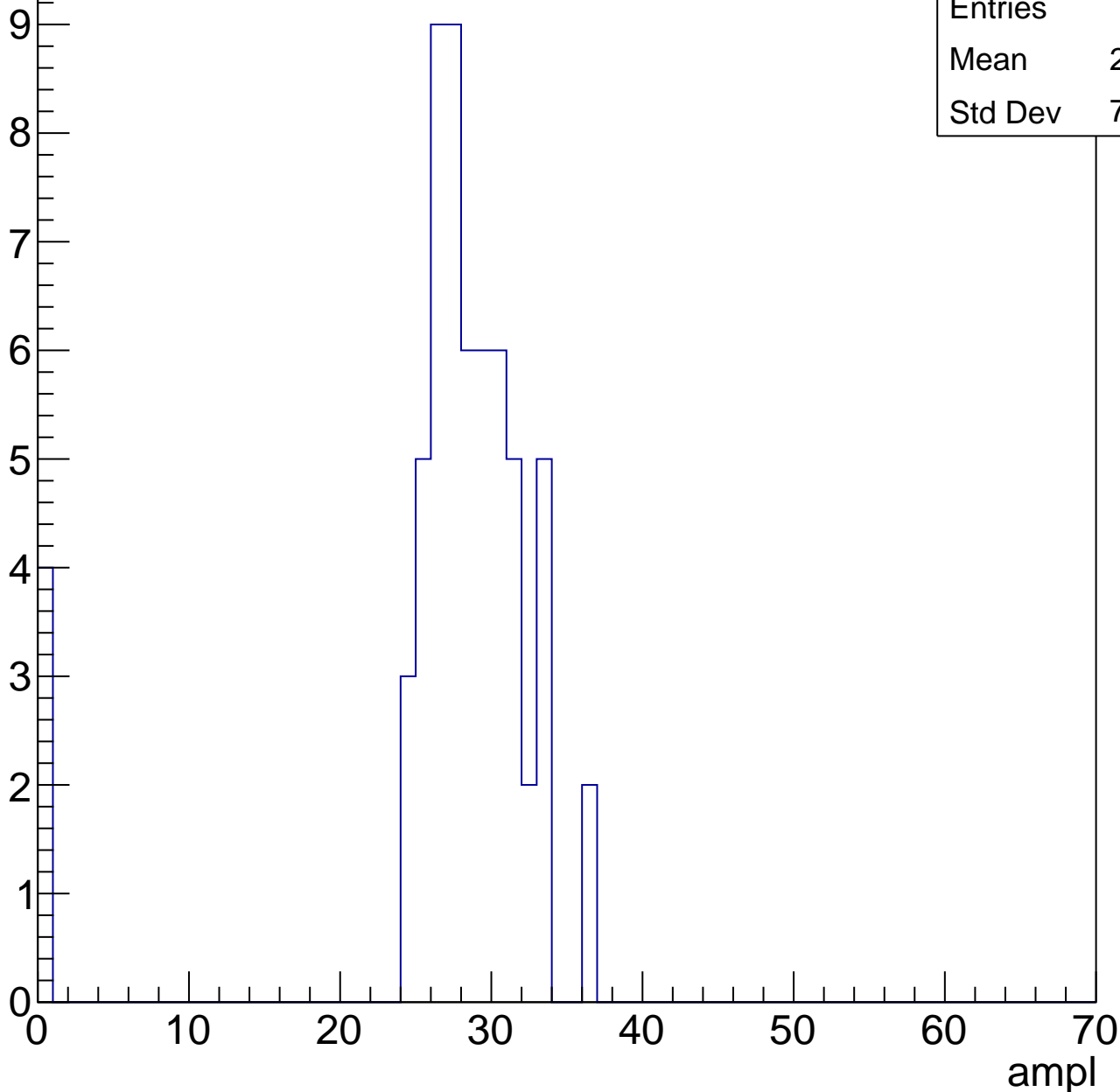
ampl

B1L103S, U9-ch68, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	26.65
Std Dev	7.535

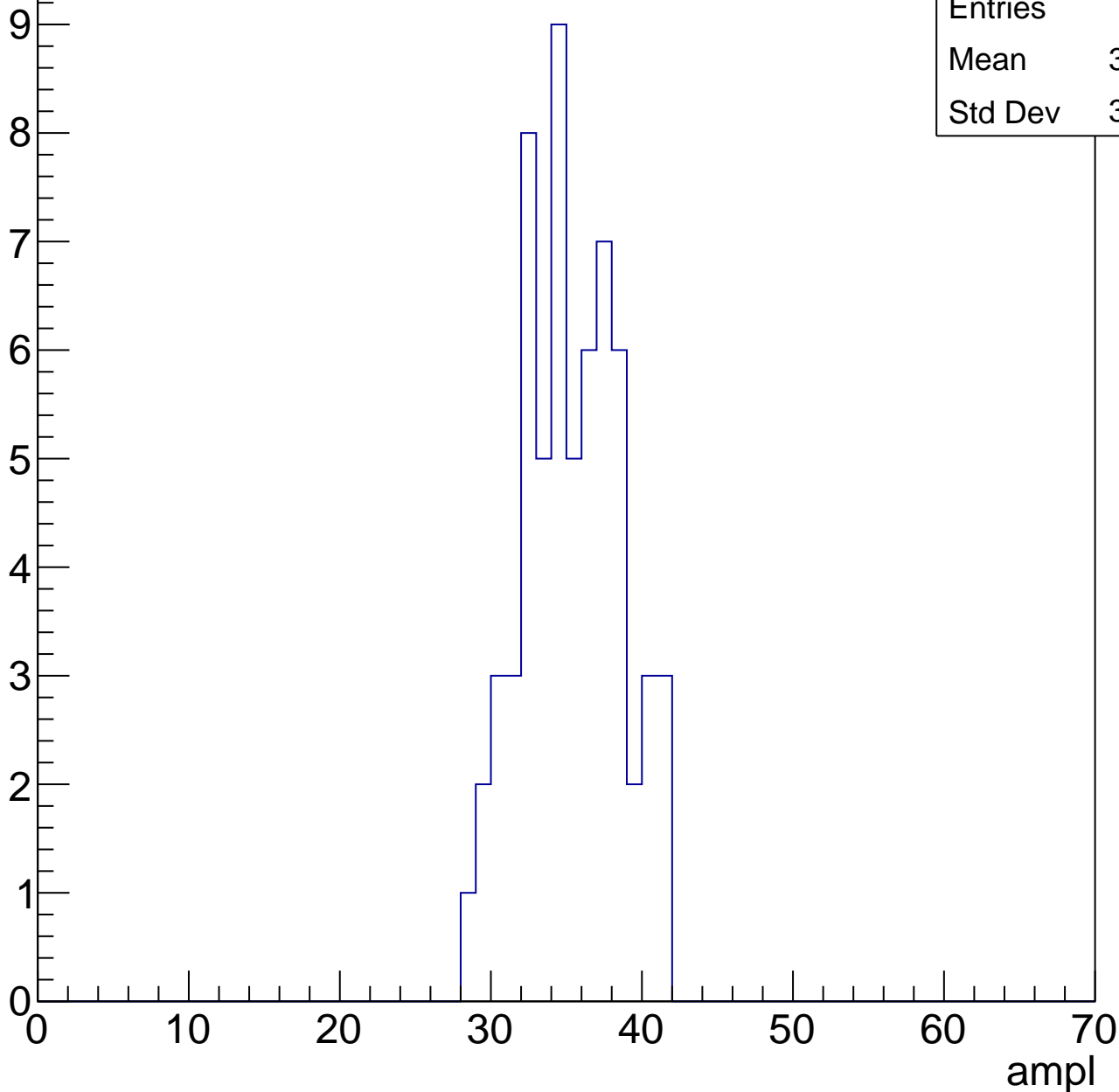


B1L103S, U9-ch68, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	34.84
Std Dev	3.203

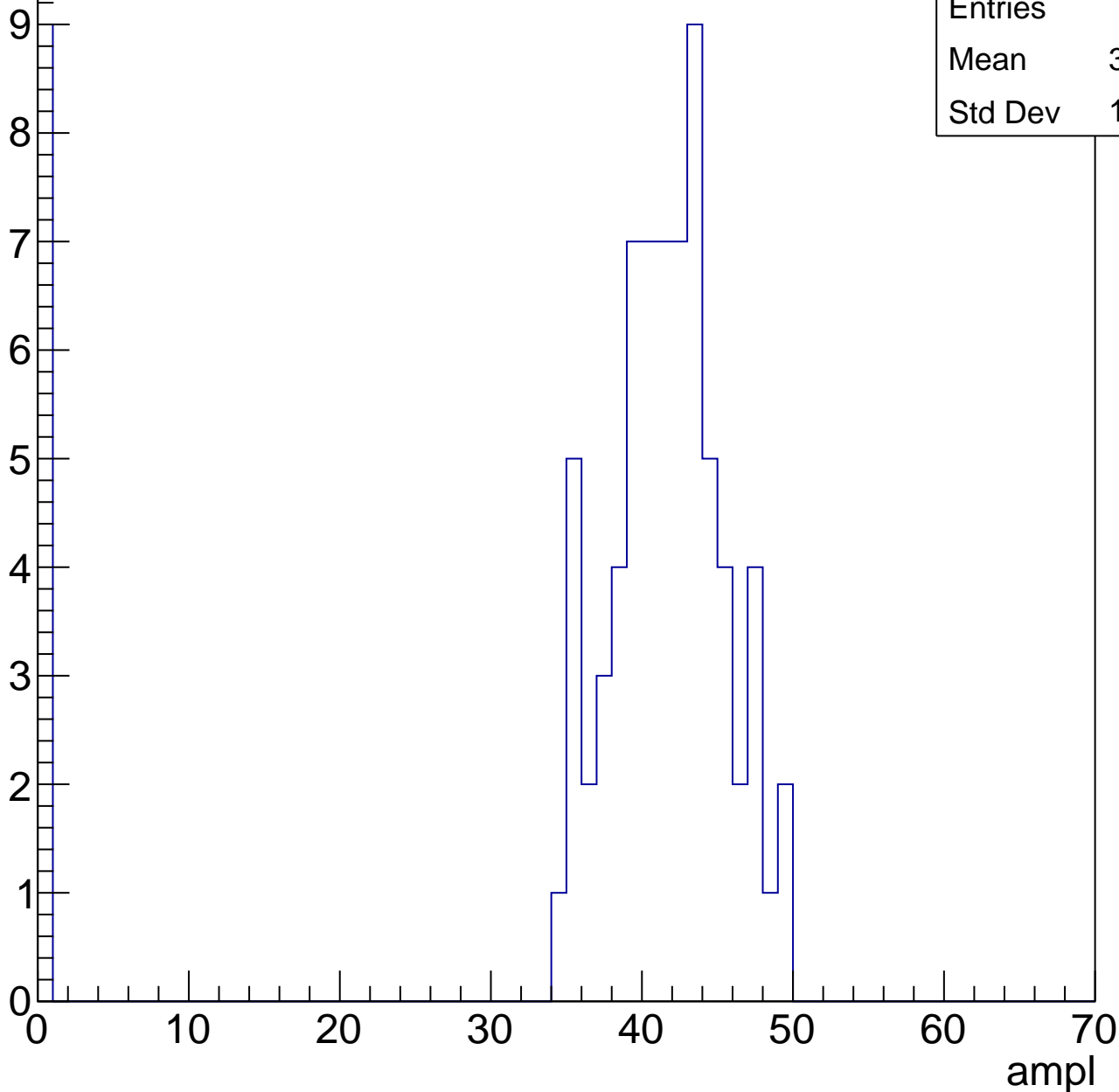


B1L103S, U9-ch68, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

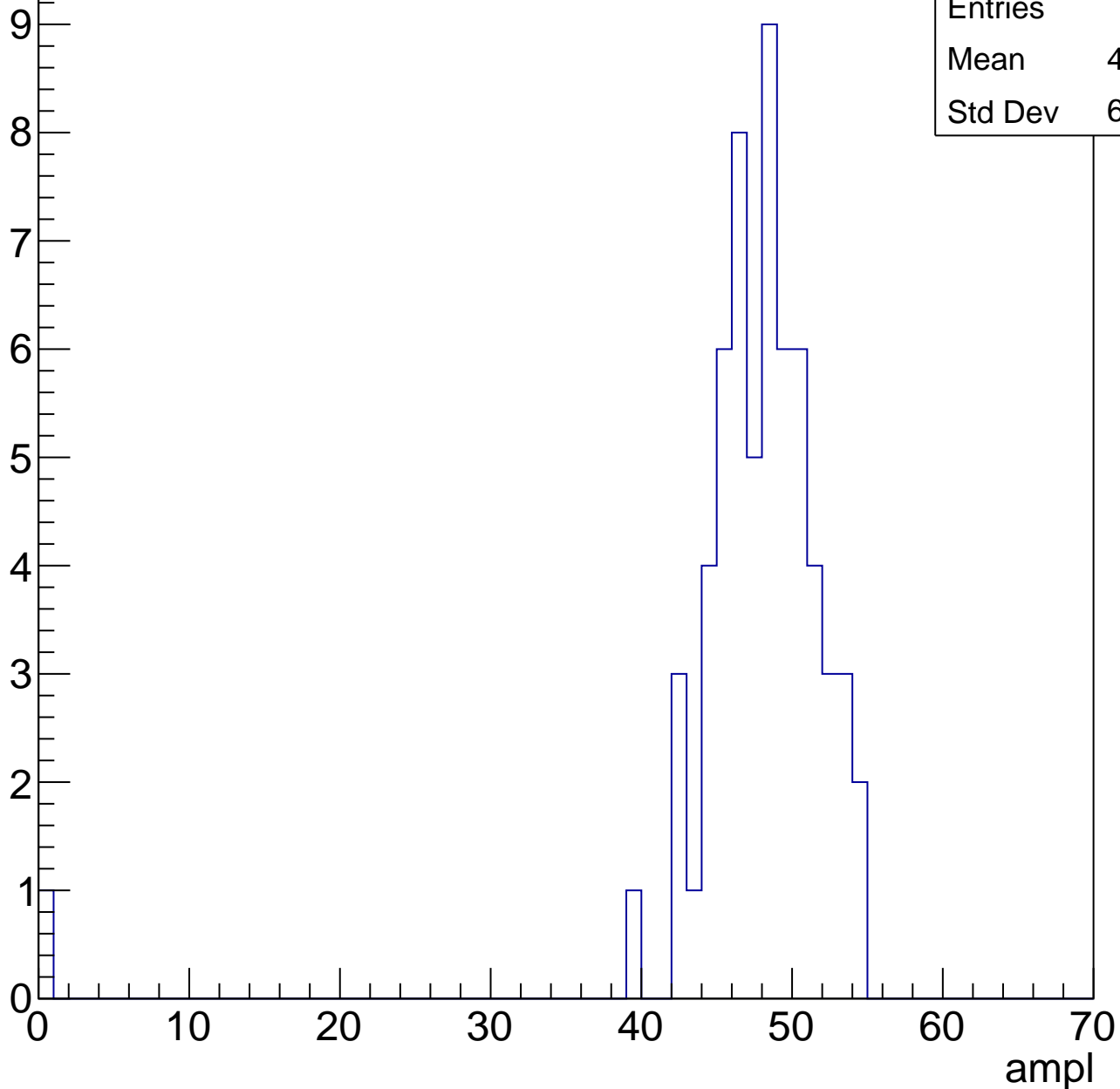
Entries	79
Mean	36.59
Std Dev	13.56



B1L103S, U9-ch68, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

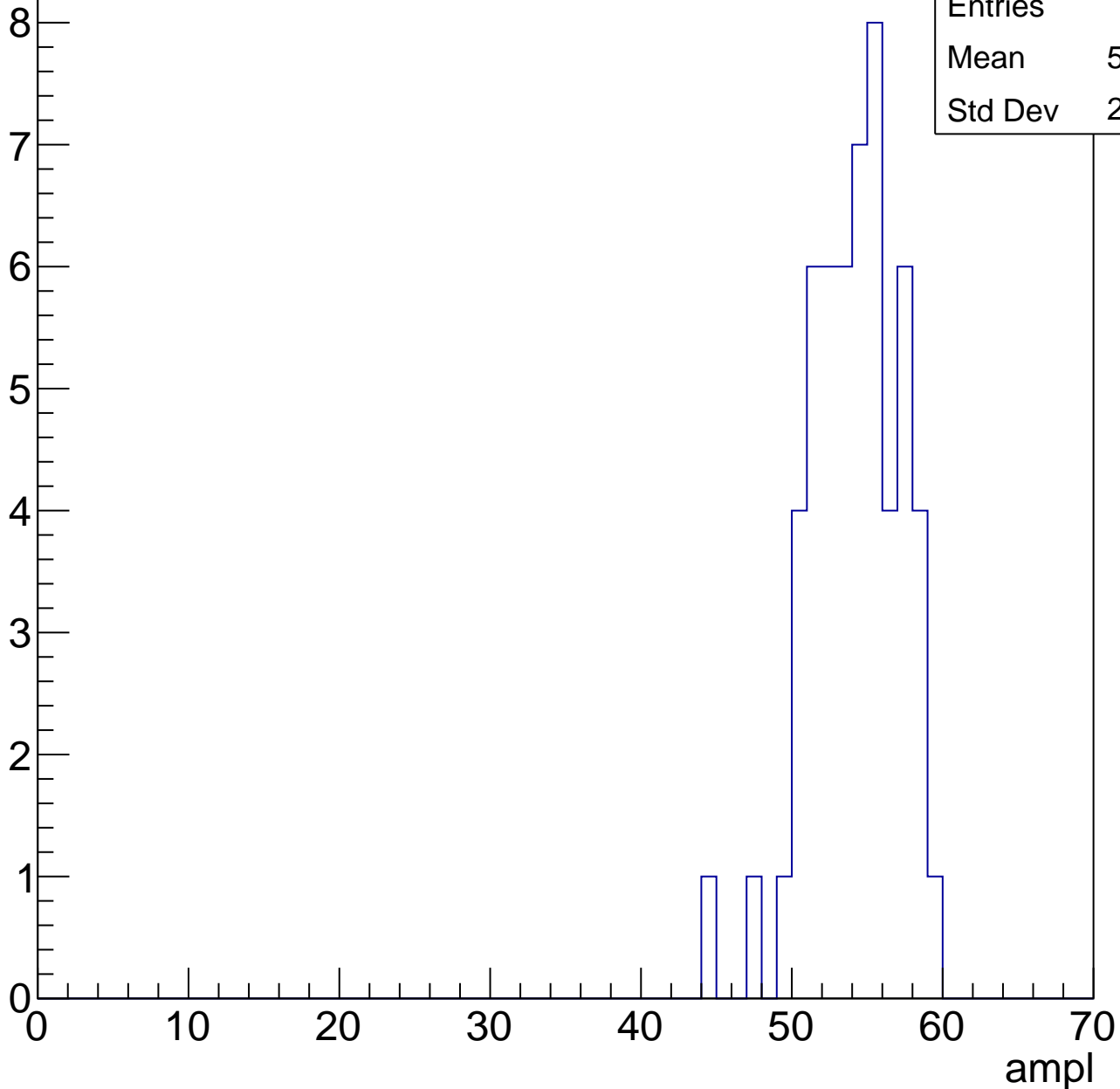


B1L103S, U9-ch68, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	53.65
Std Dev	2.962

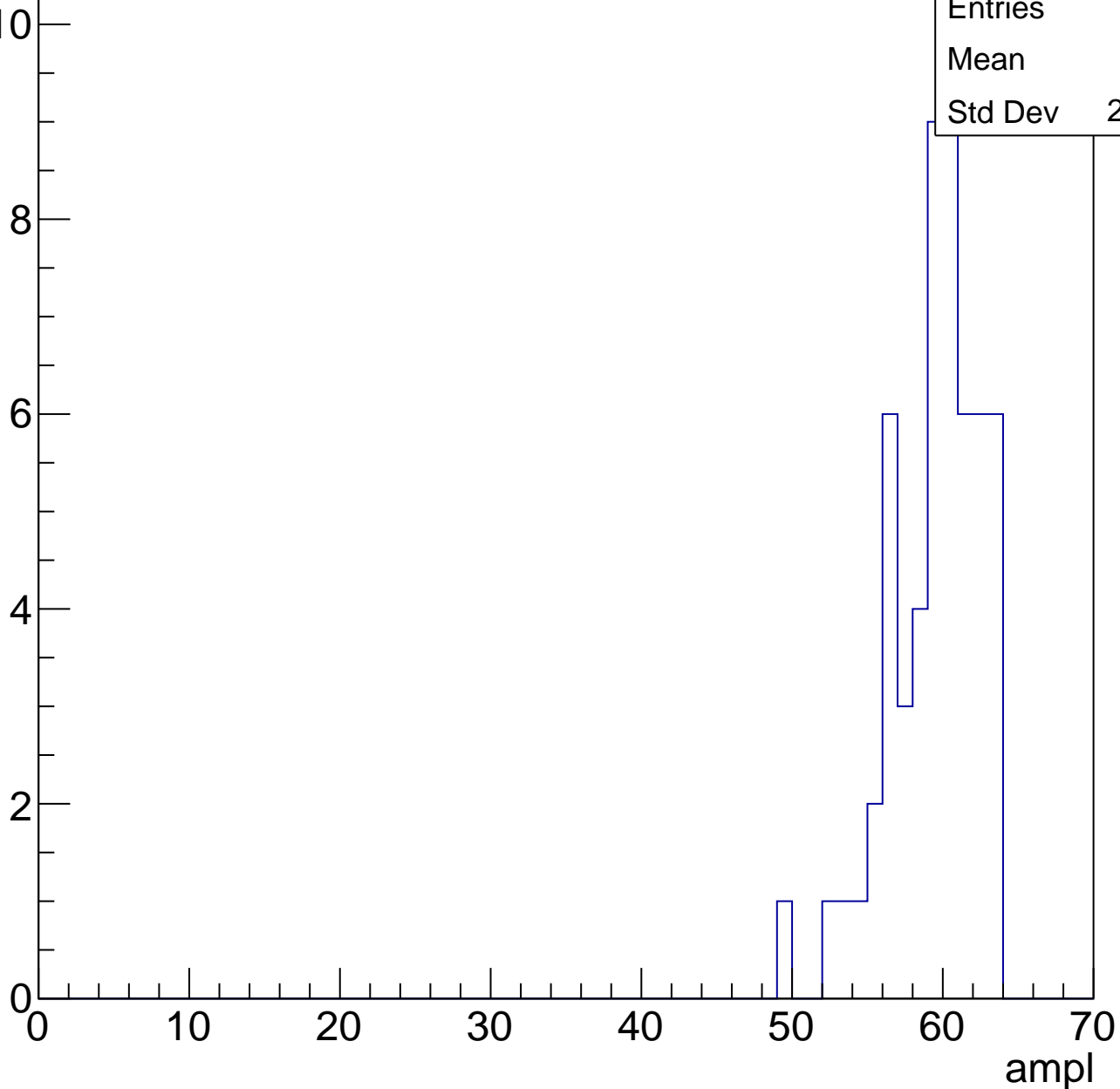


B1L103S, U9-ch68, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

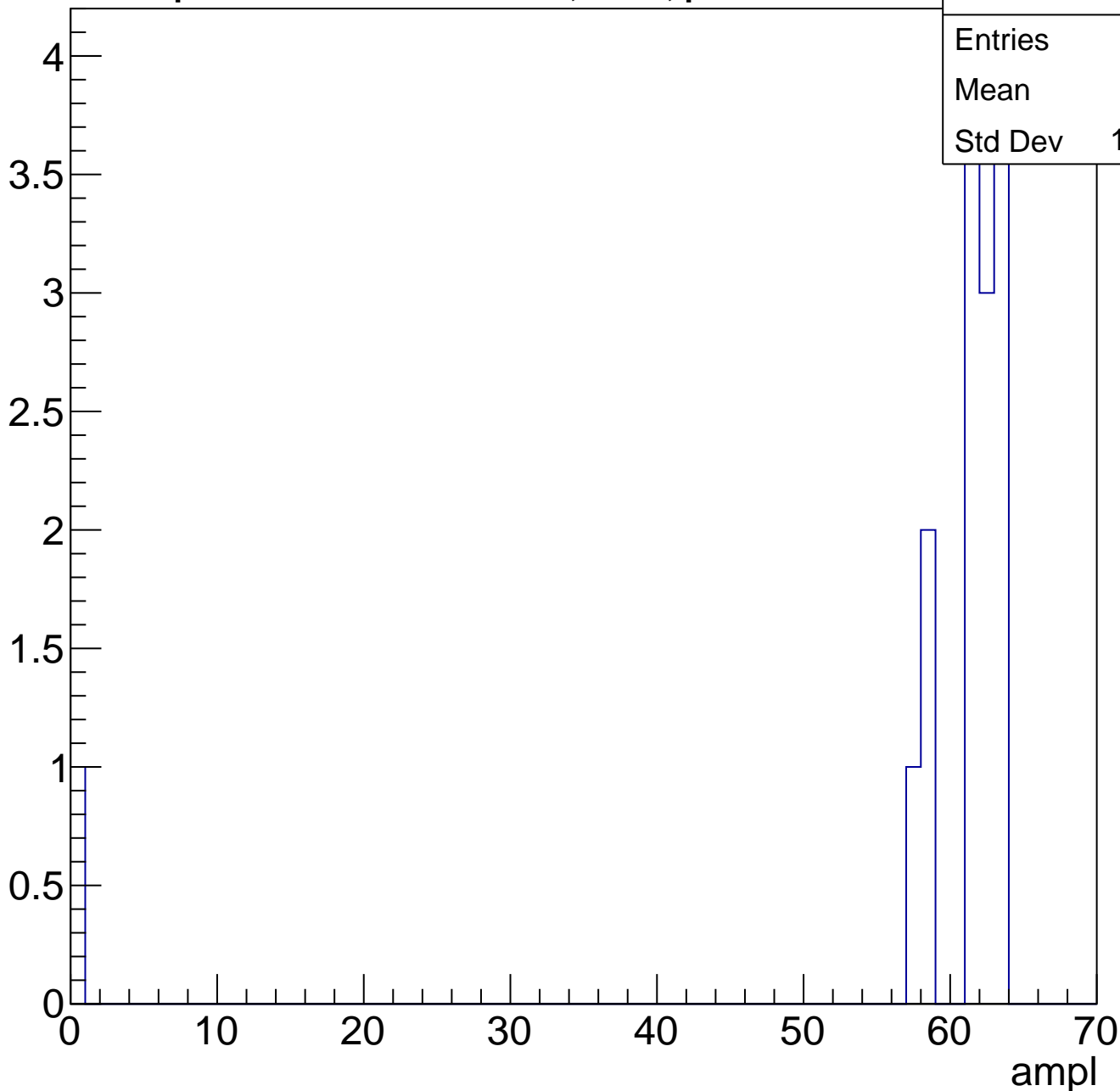
Entries	56
Mean	59
Std Dev	2.976



B1L103S, U9-ch68, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

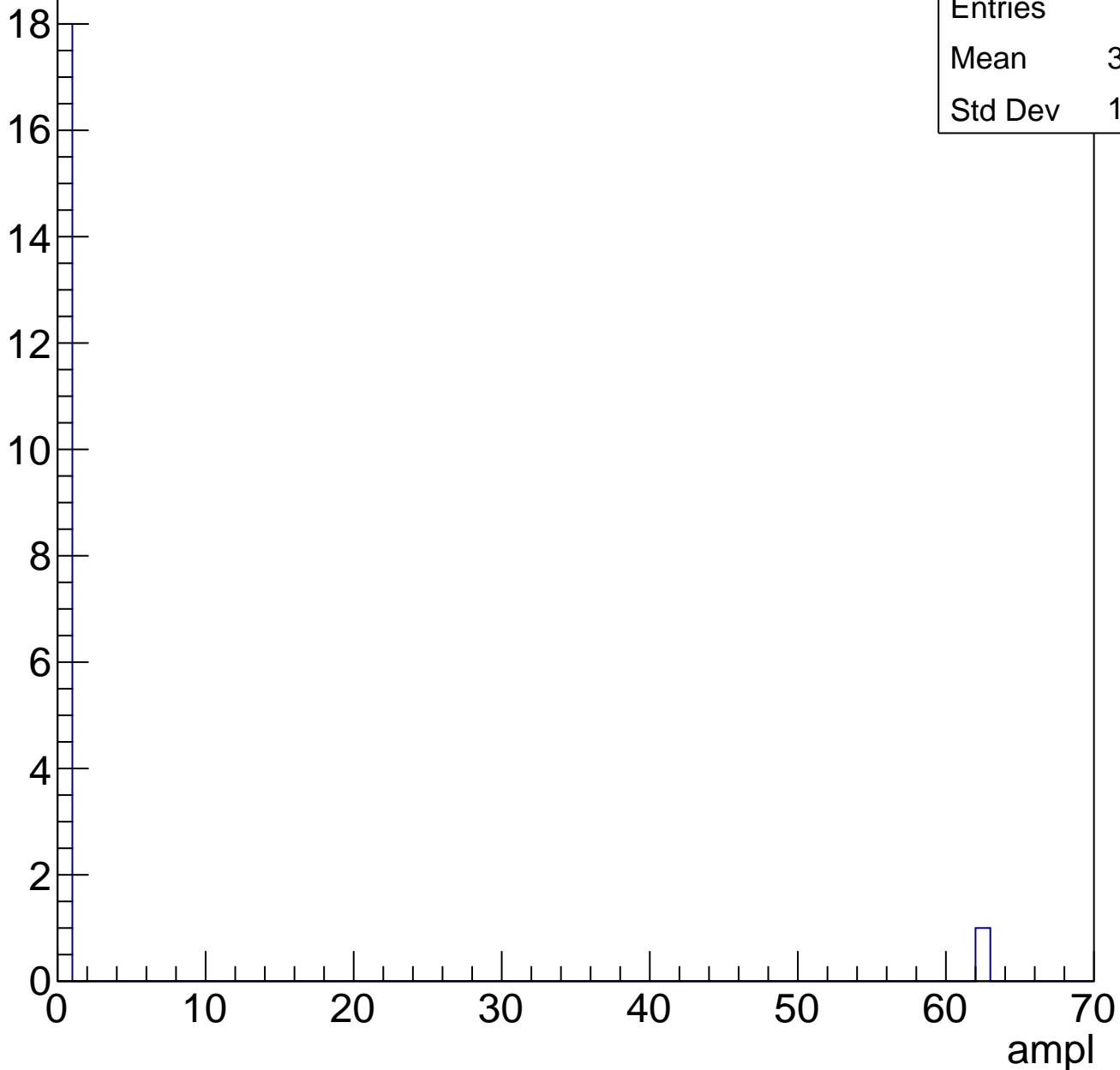


B1L103S, U9-ch68, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	3.263
Std Dev	13.84

Entry

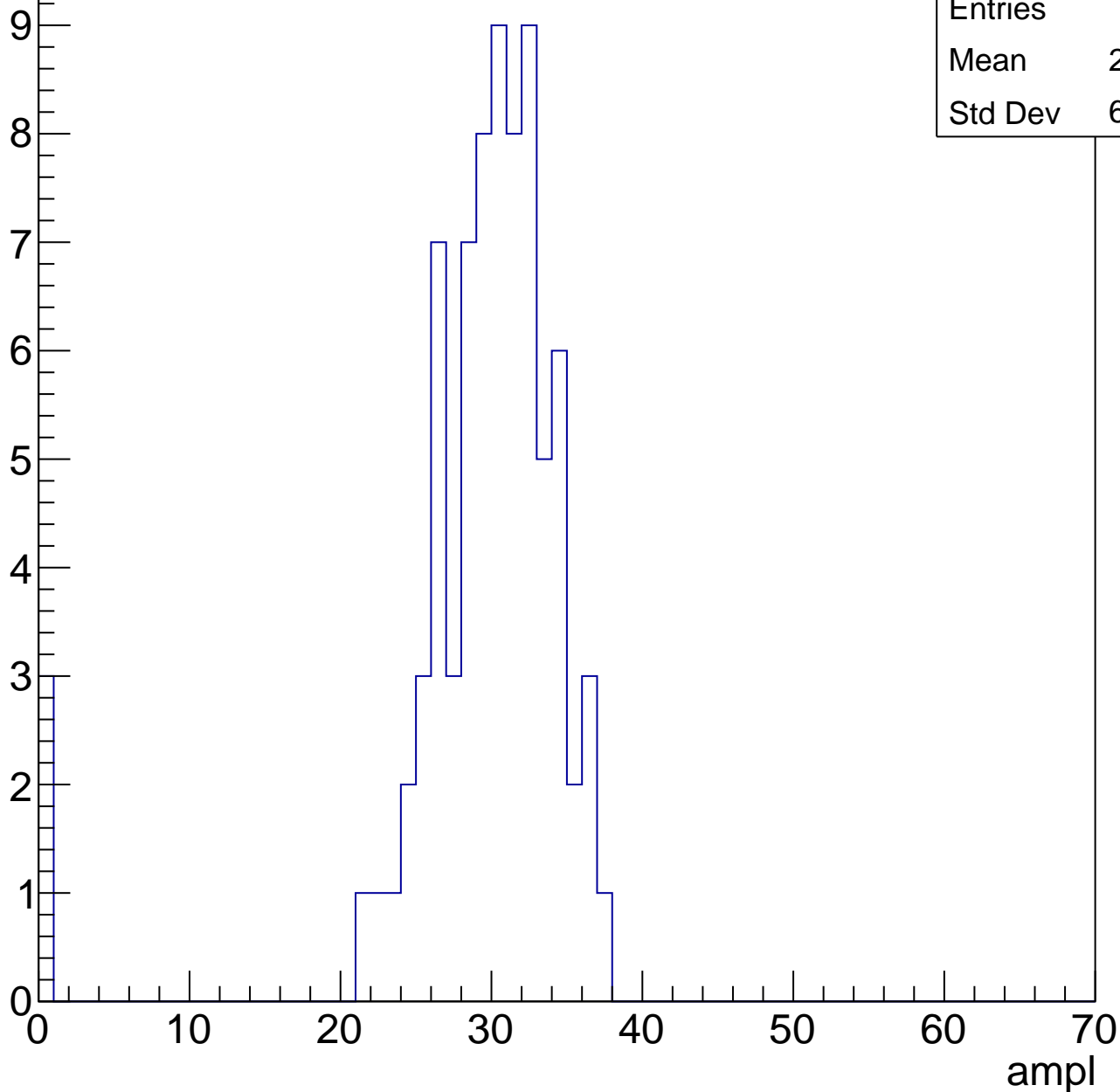


B1L103S, U9-ch69, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	79
Mean	28.73
Std Dev	6.638

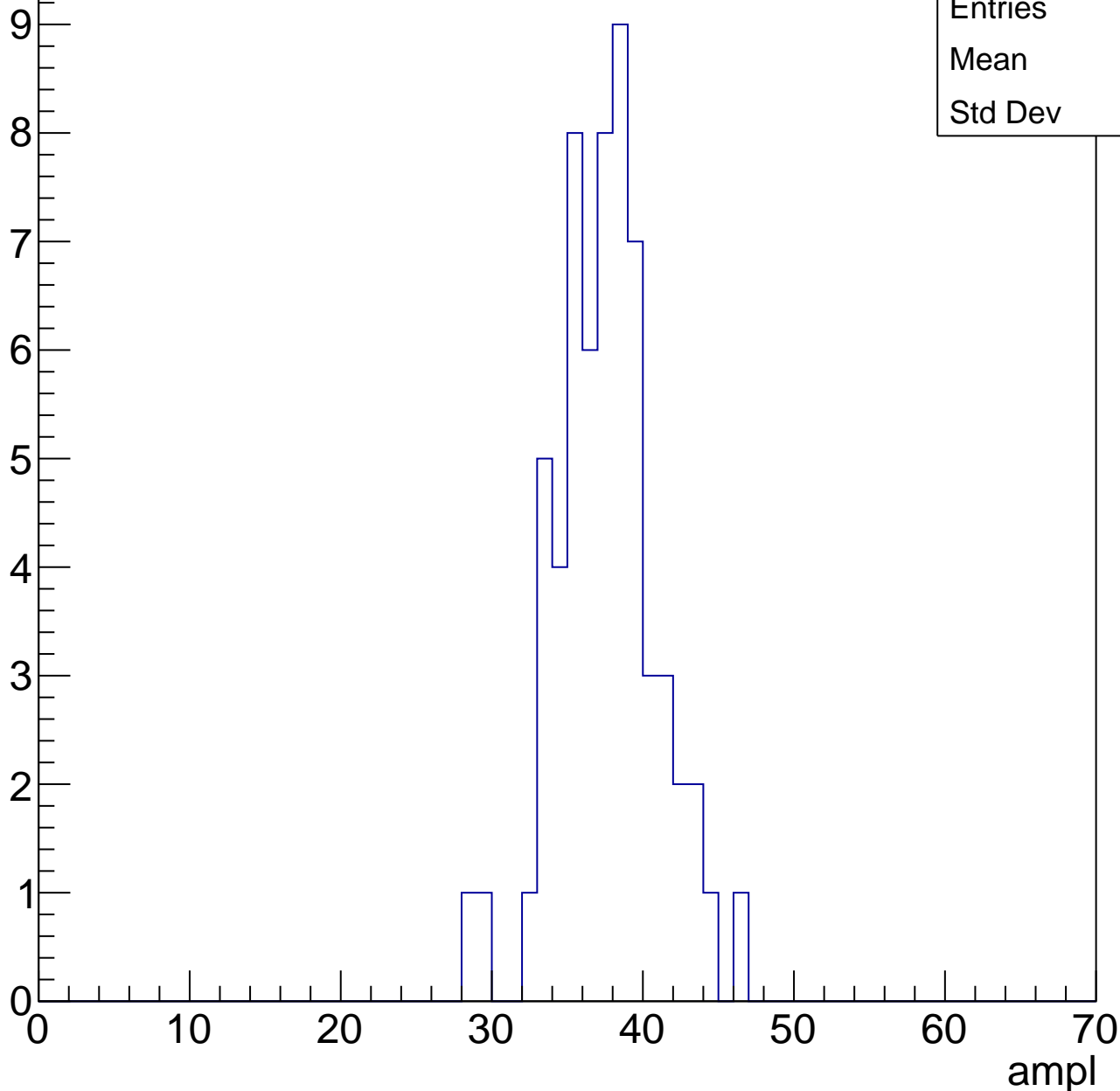


B1L103S, U9-ch69, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	37.1
Std Dev	3.33

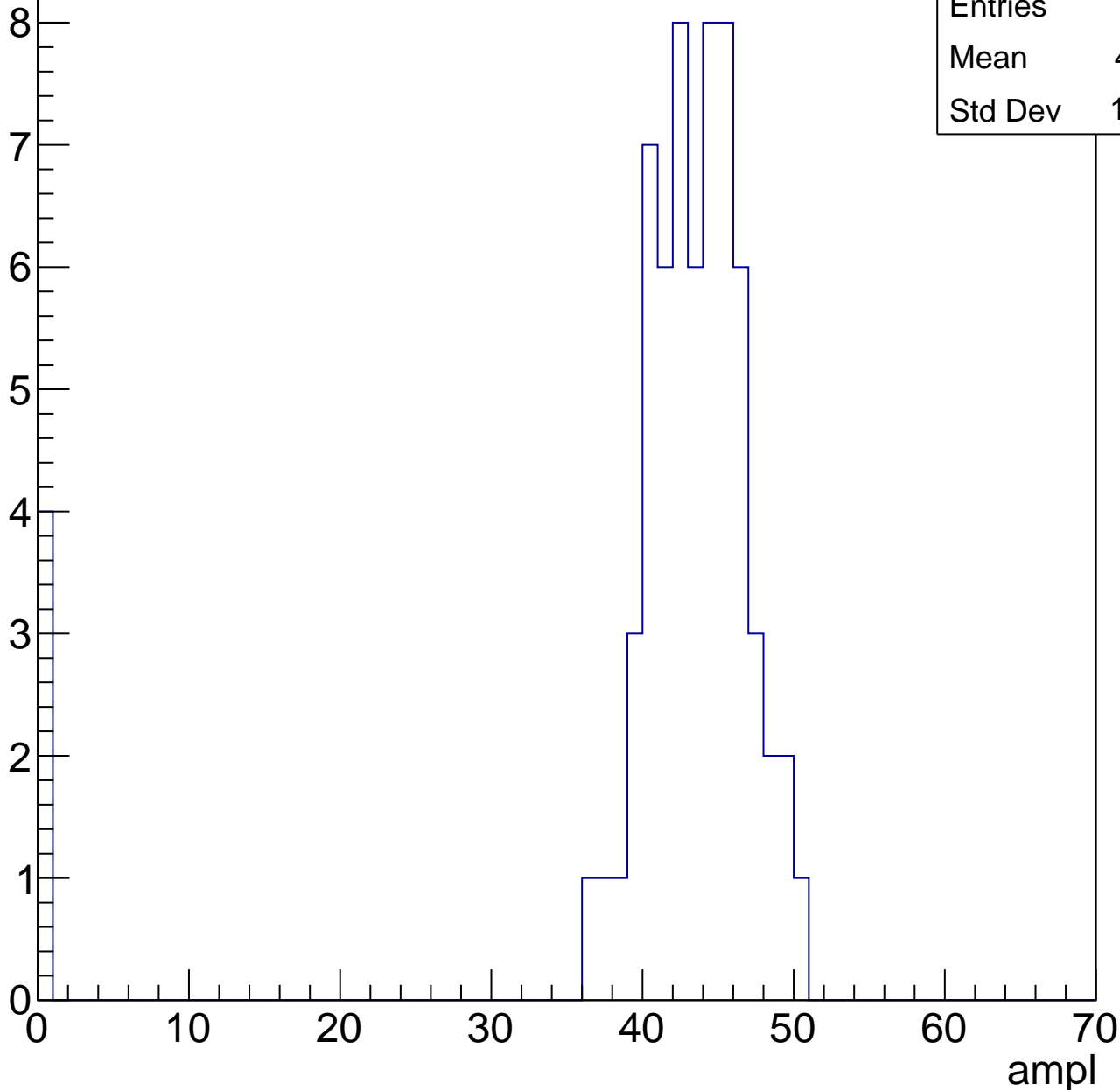


B1L103S, U9-ch69, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	40.61
Std Dev	10.64

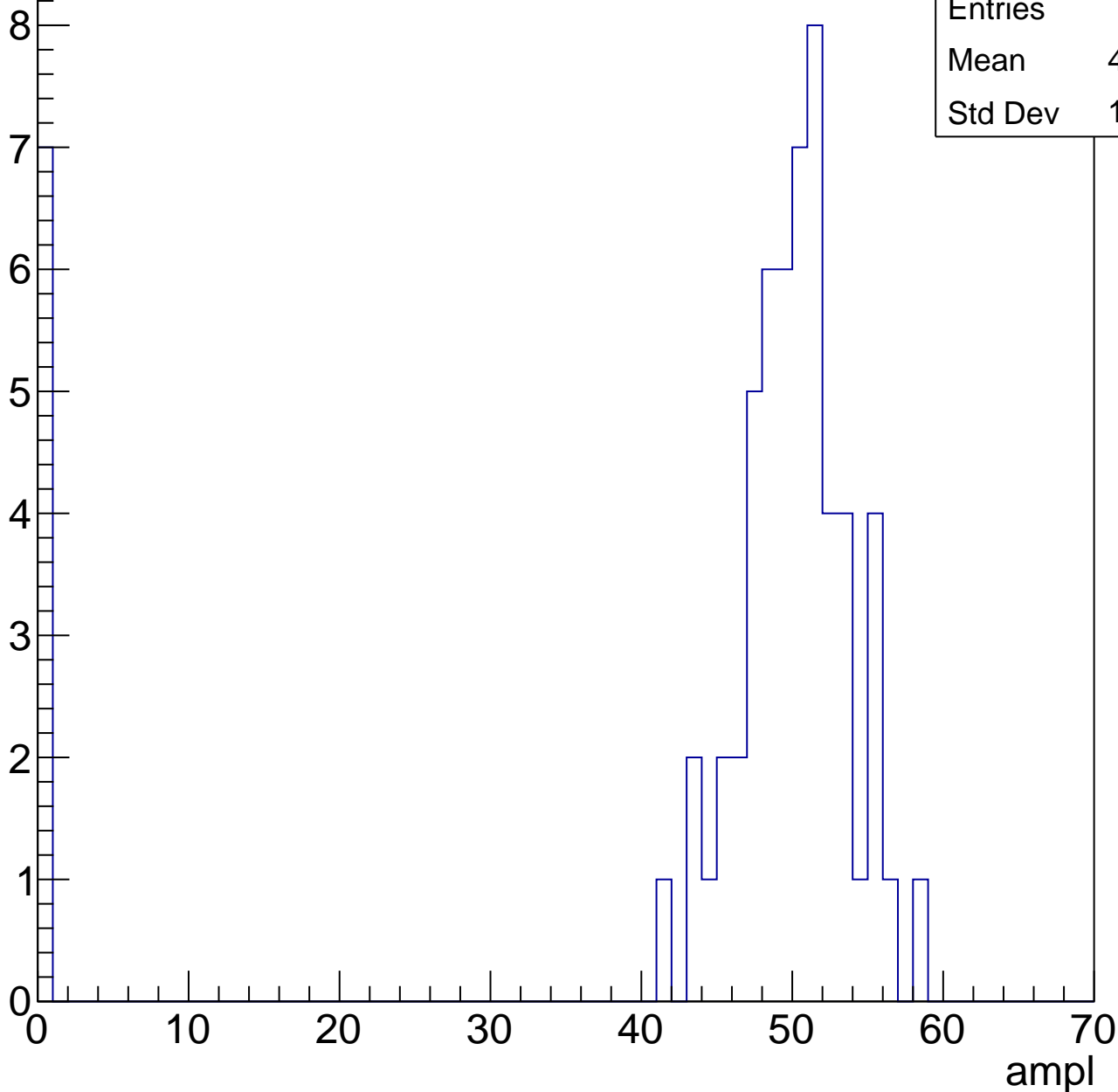


B1L103S, U9-ch69, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	44.13
Std Dev	16.07



B1L103S, U9-ch69, adc4

calib_packv5_041523_1651.root, FC#0, port C2

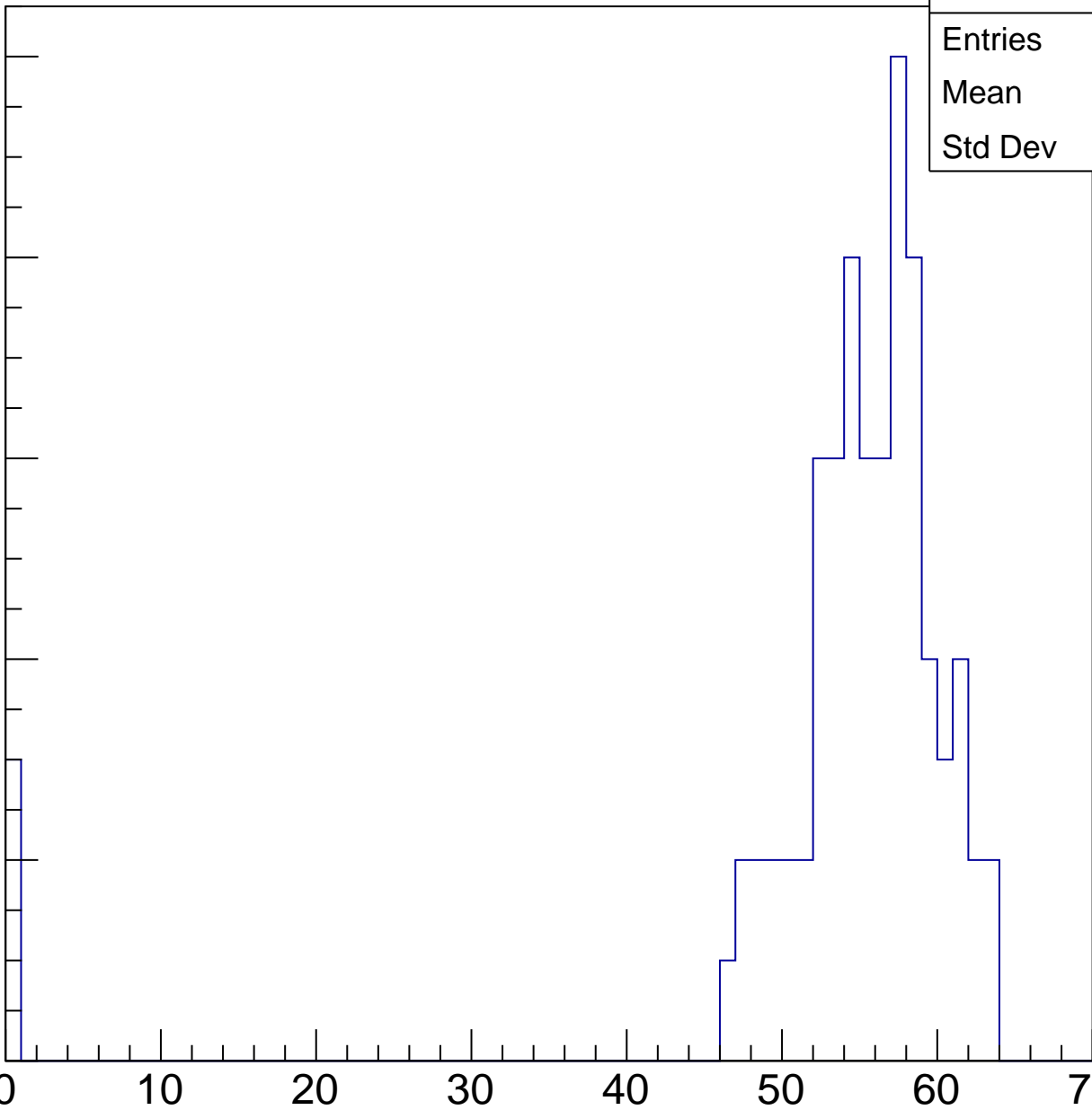
Entries	79
Mean	53.27
Std Dev	11.26

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

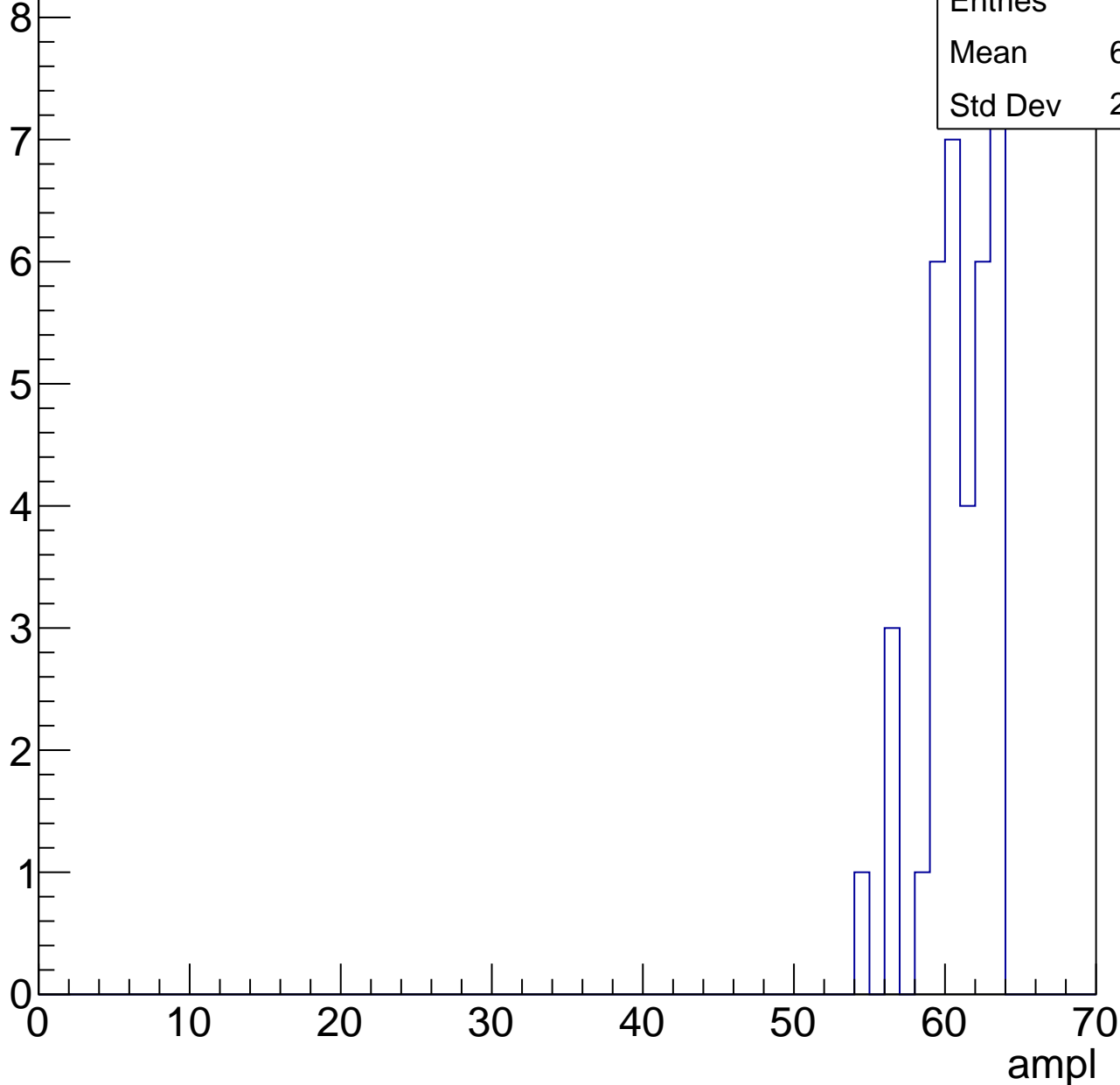


B1L103S, U9-ch69, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

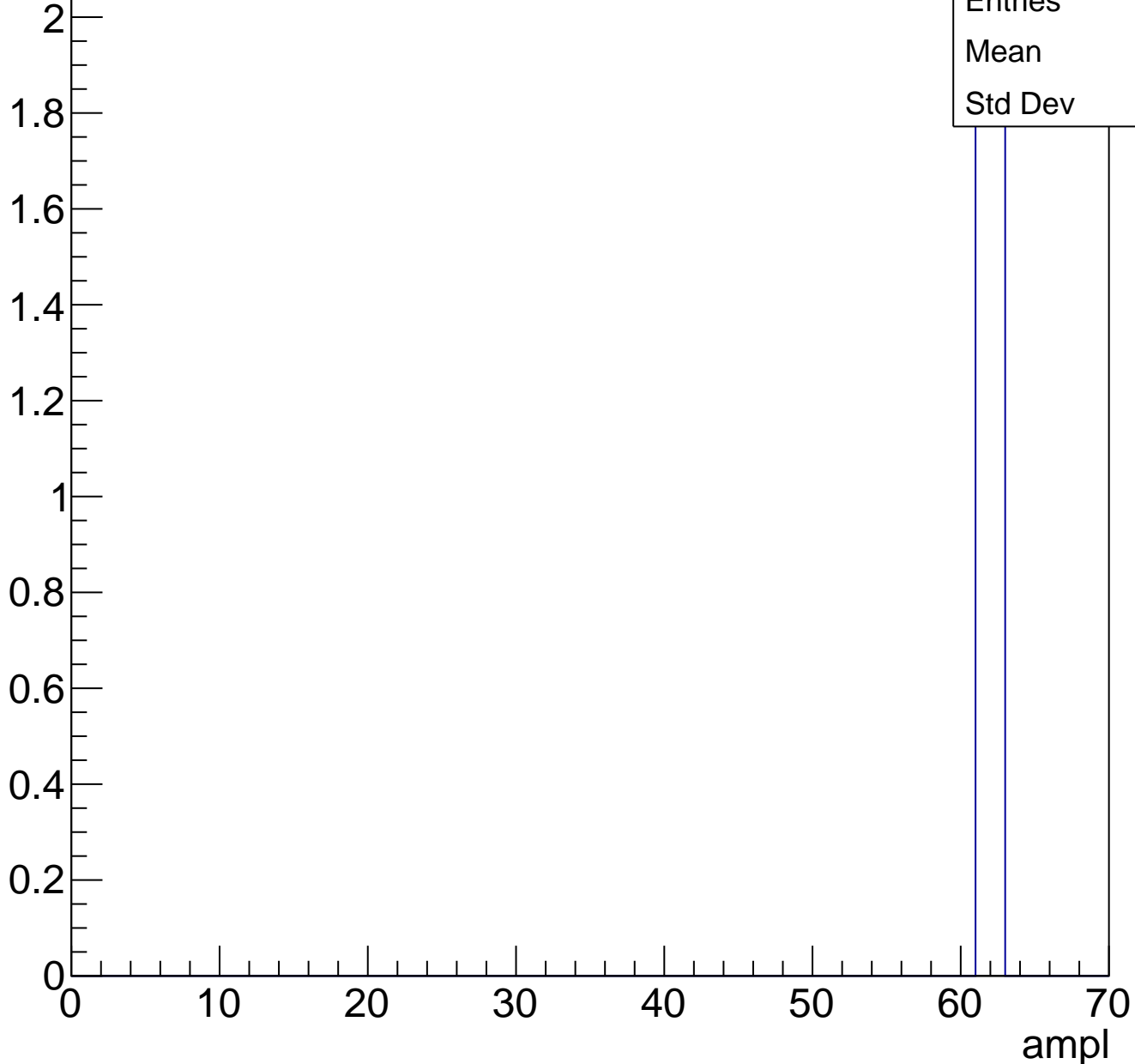
Entries	36
Mean	60.39
Std Dev	2.289



B1L103S, U9-ch69, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch69, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

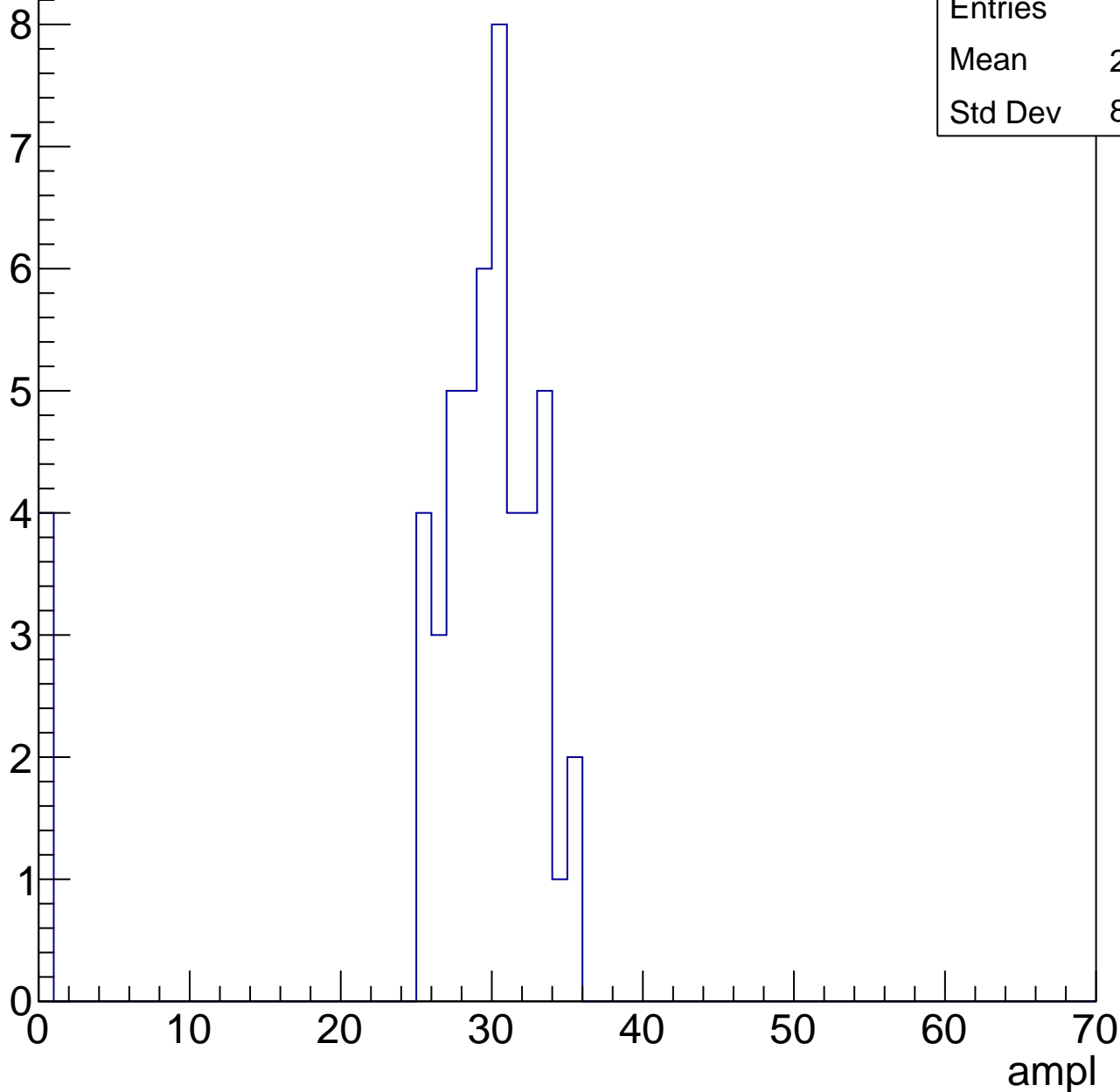
ampl

B1L103S, U9-ch70, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	27.22
Std Dev	8.349

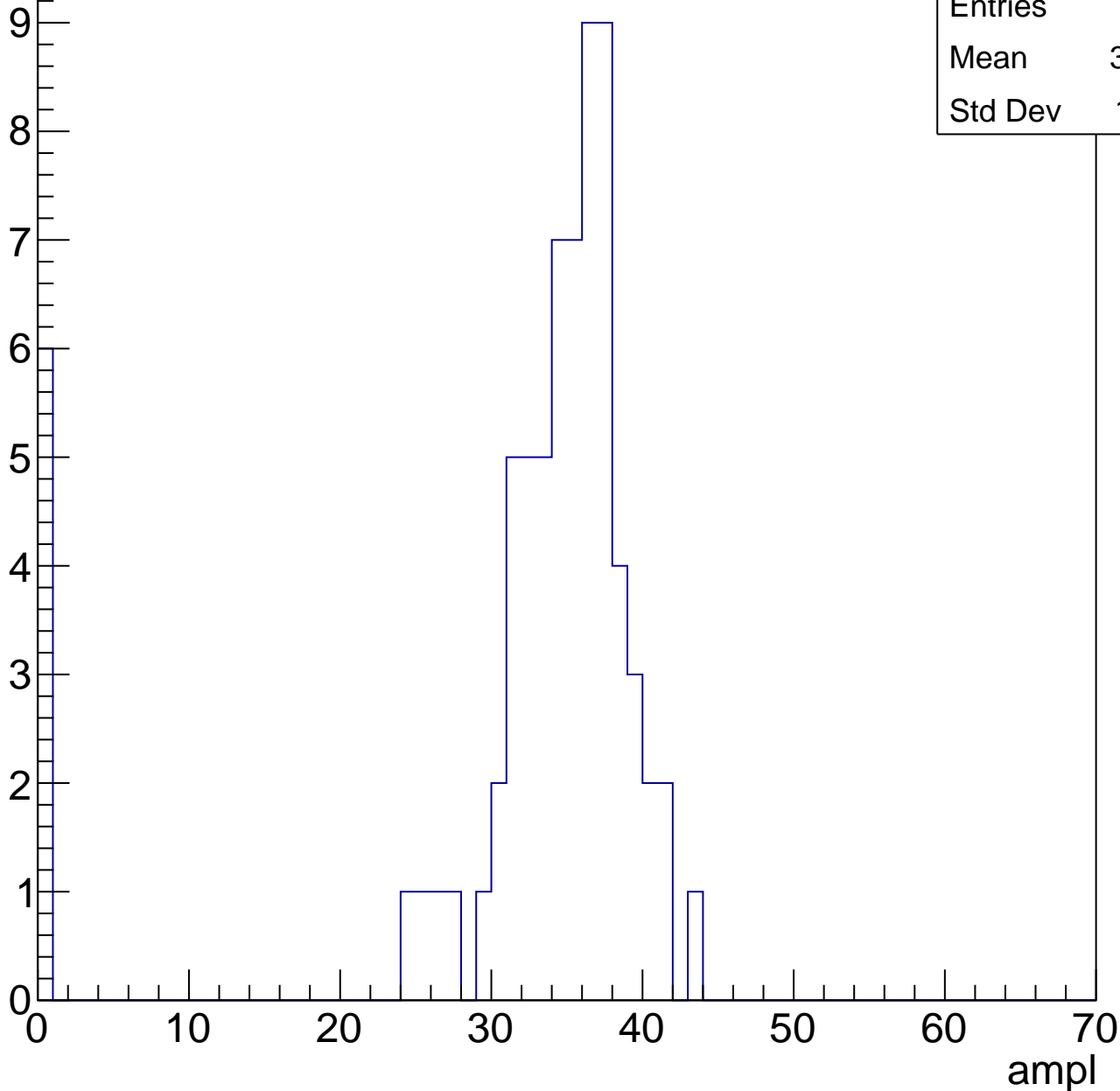


B1L103S, U9-ch70, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	31.74
Std Dev	10.21

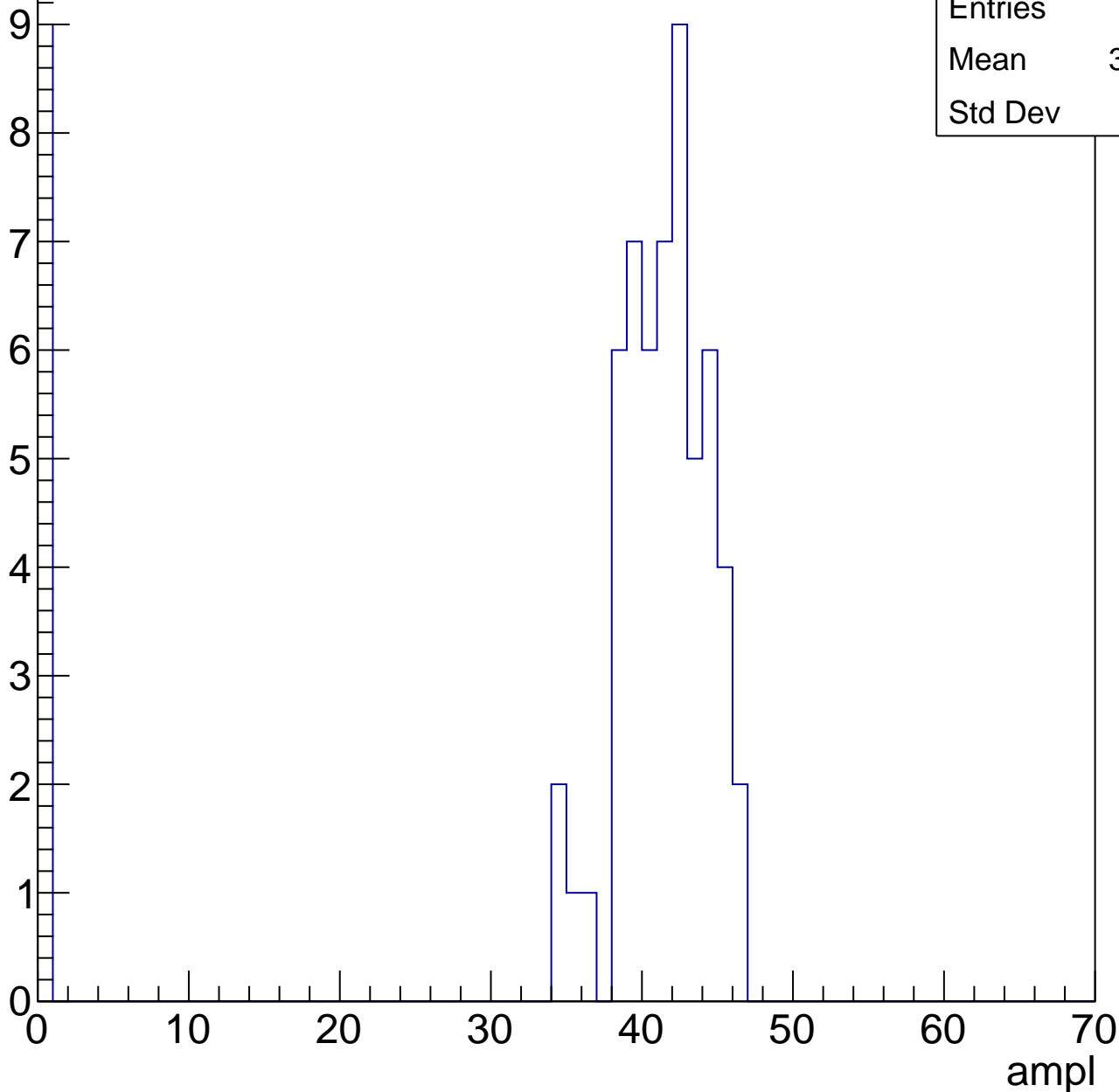


B1L103S, U9-ch70, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	35.32
Std Dev	14.4



B1L103S, U9-ch70, adc3

calib_packv5_041523_1651.root, FC#0, port C2

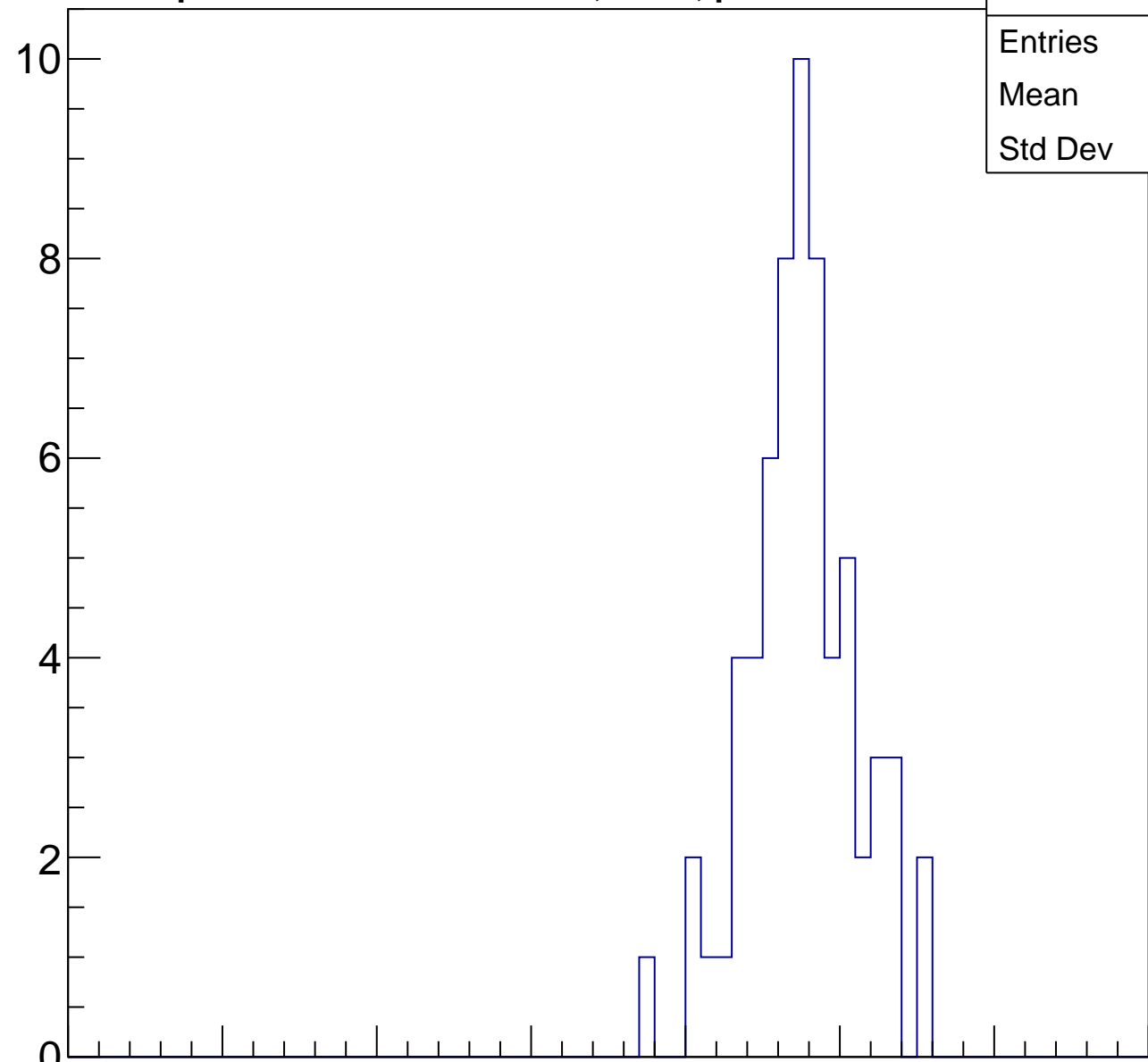
Entries	64
Mean	47.08
Std Dev	3.541

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

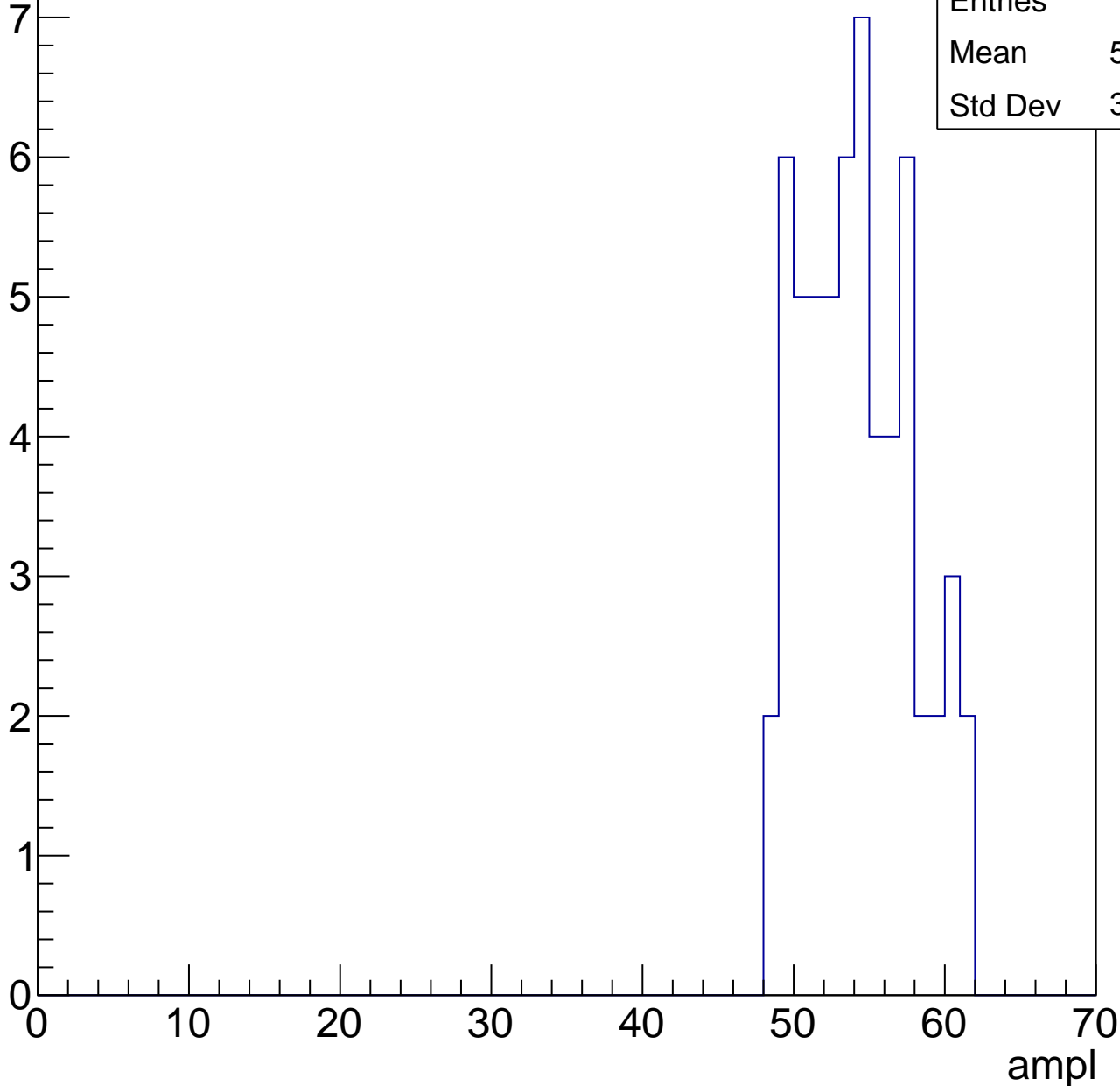


B1L103S, U9-ch70, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	53.78
Std Dev	3.523

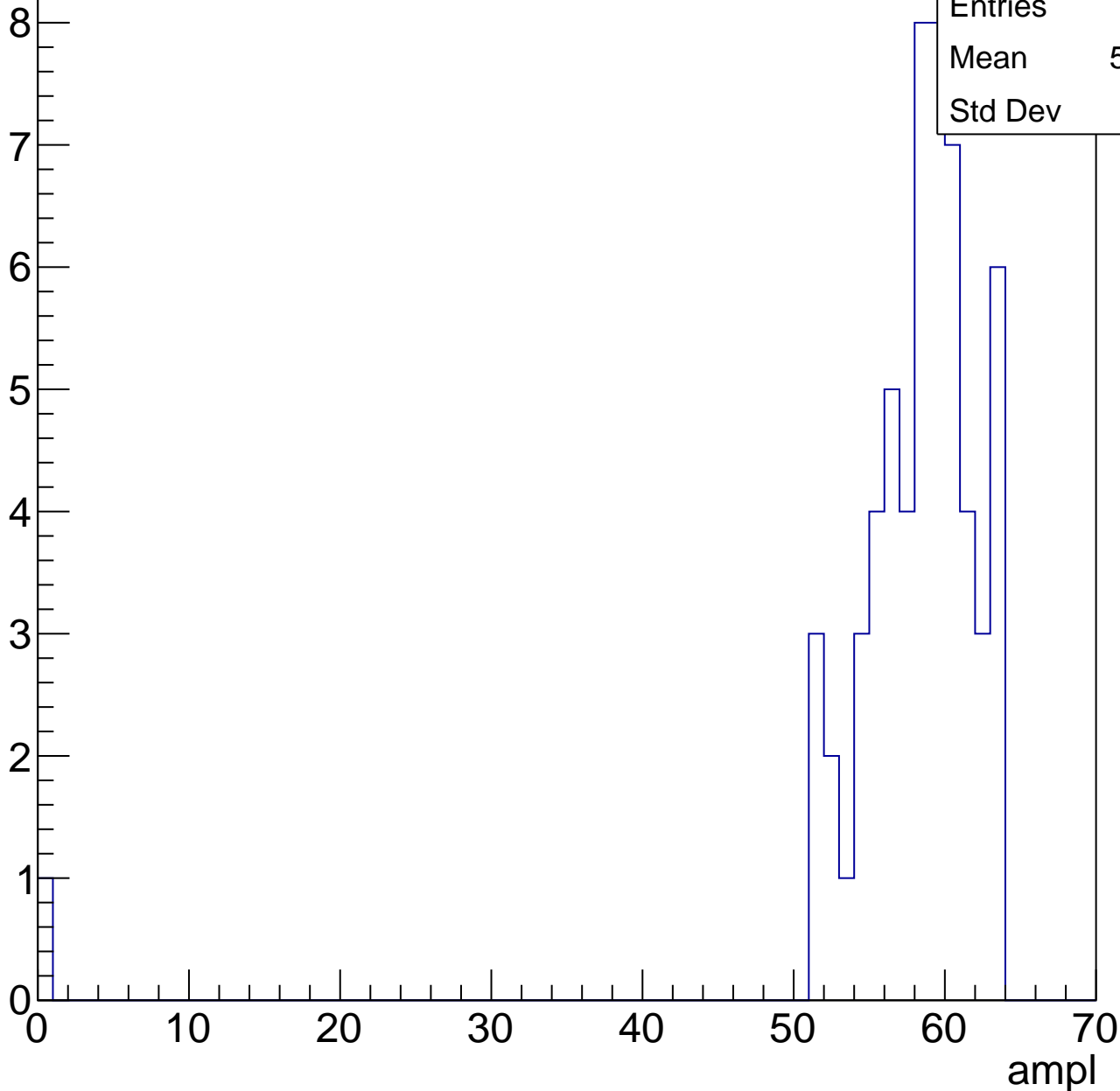


B1L103S, U9-ch70, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	57.02
Std Dev	8.16

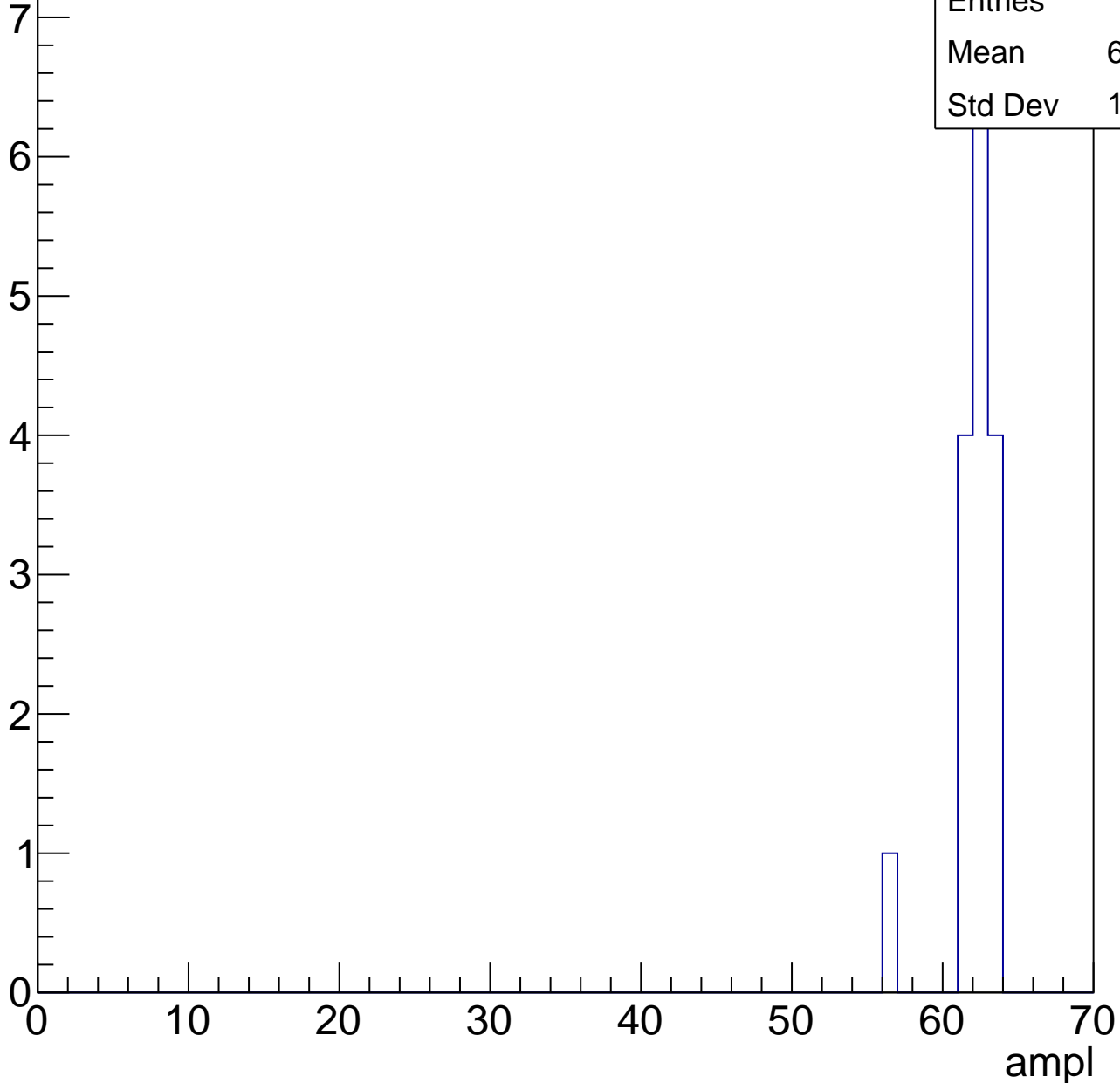


B1L103S, U9-ch70, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

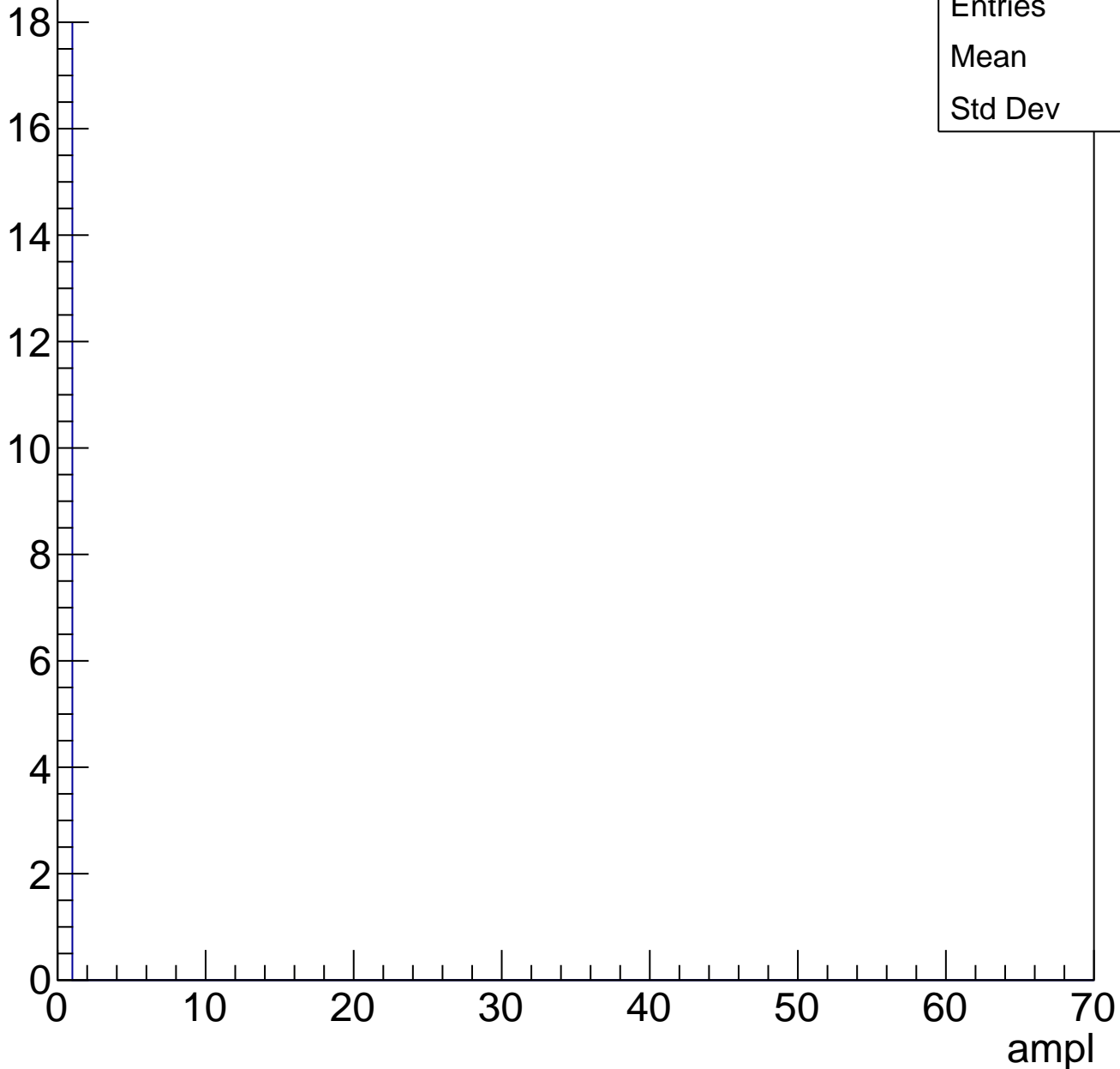
Entries	16
Mean	61.62
Std Dev	1.615



B1L103S, U9-ch70, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch71, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	96
Mean	24.92
Std Dev	10.47

Entry

12

10

8

6

4

2

0

0

10

20

30

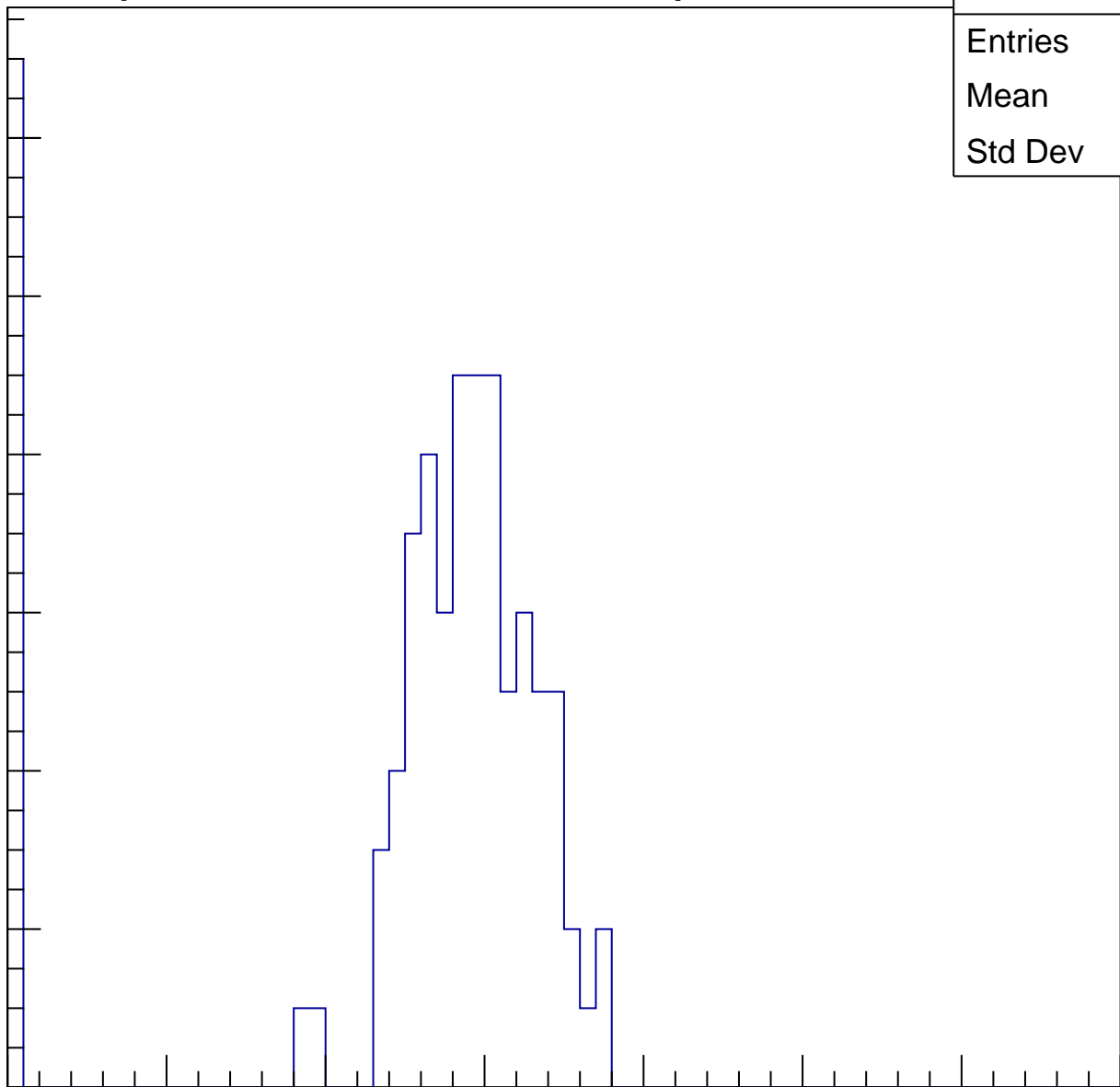
40

50

60

70

ampl

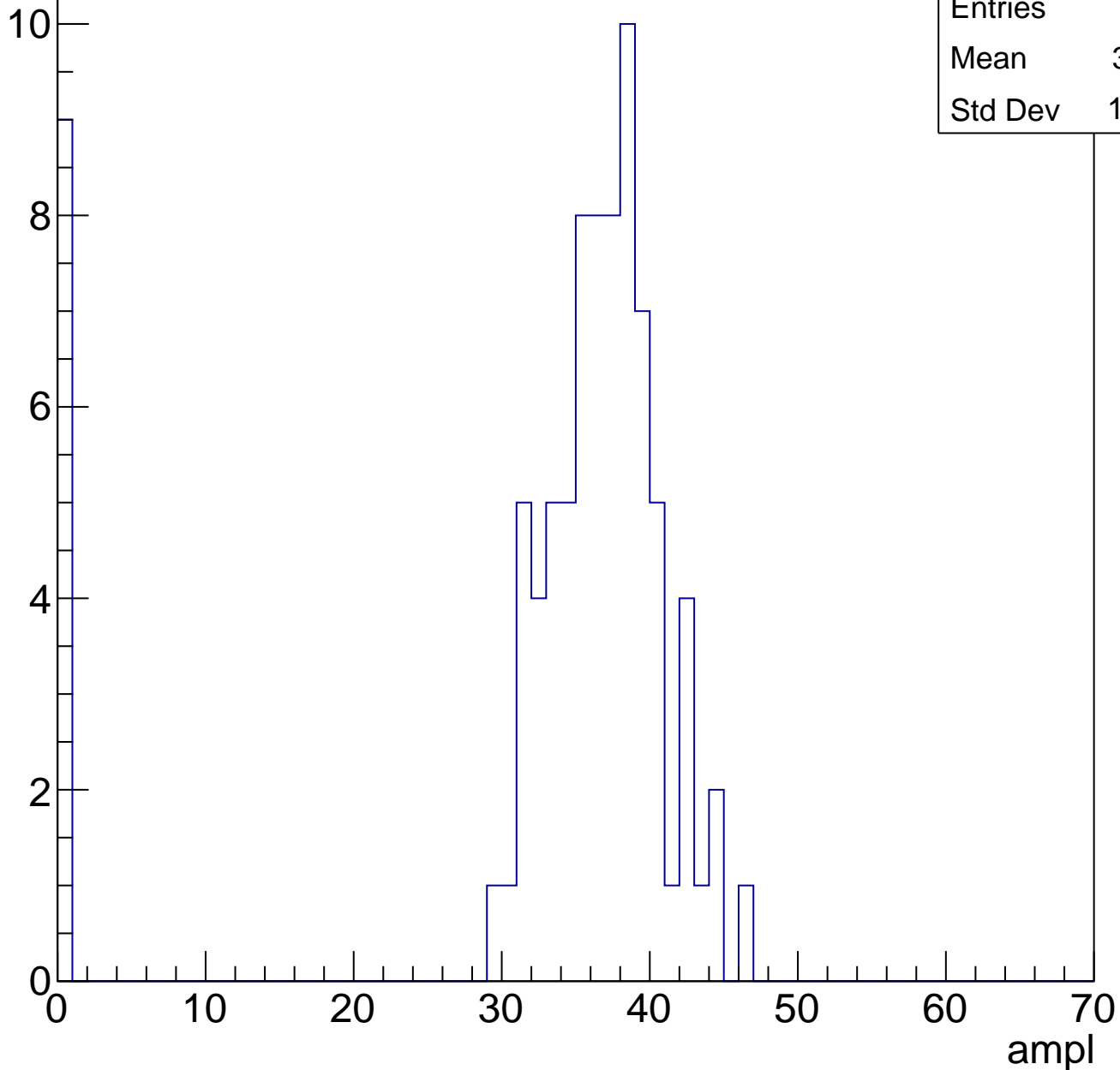


B1L103S, U9-ch71, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	85
Mean	32.71
Std Dev	11.75

Entry

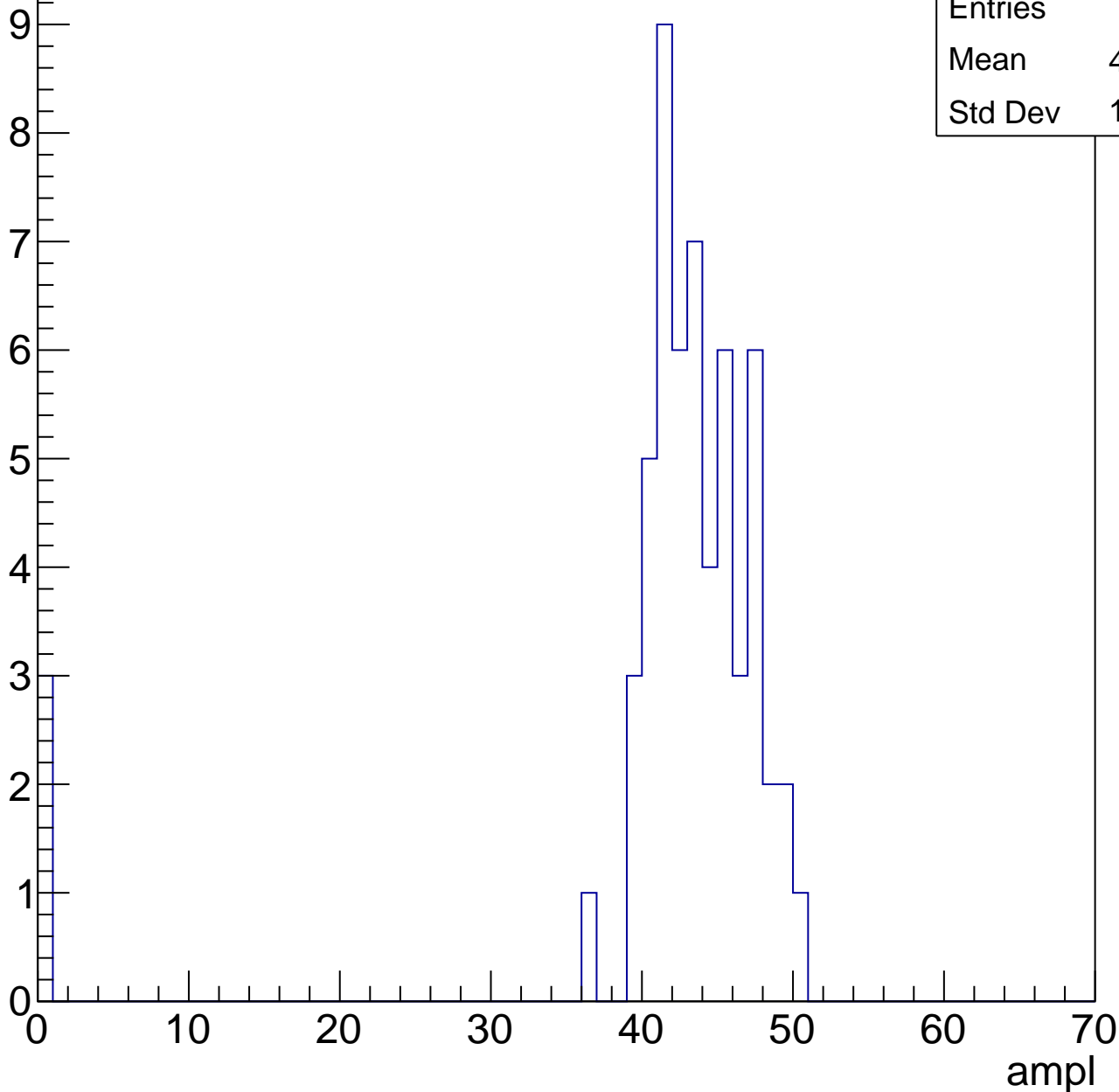


B1L103S, U9-ch71, adc2

calib_packv5_041523_1651.root, FC#0, port C2

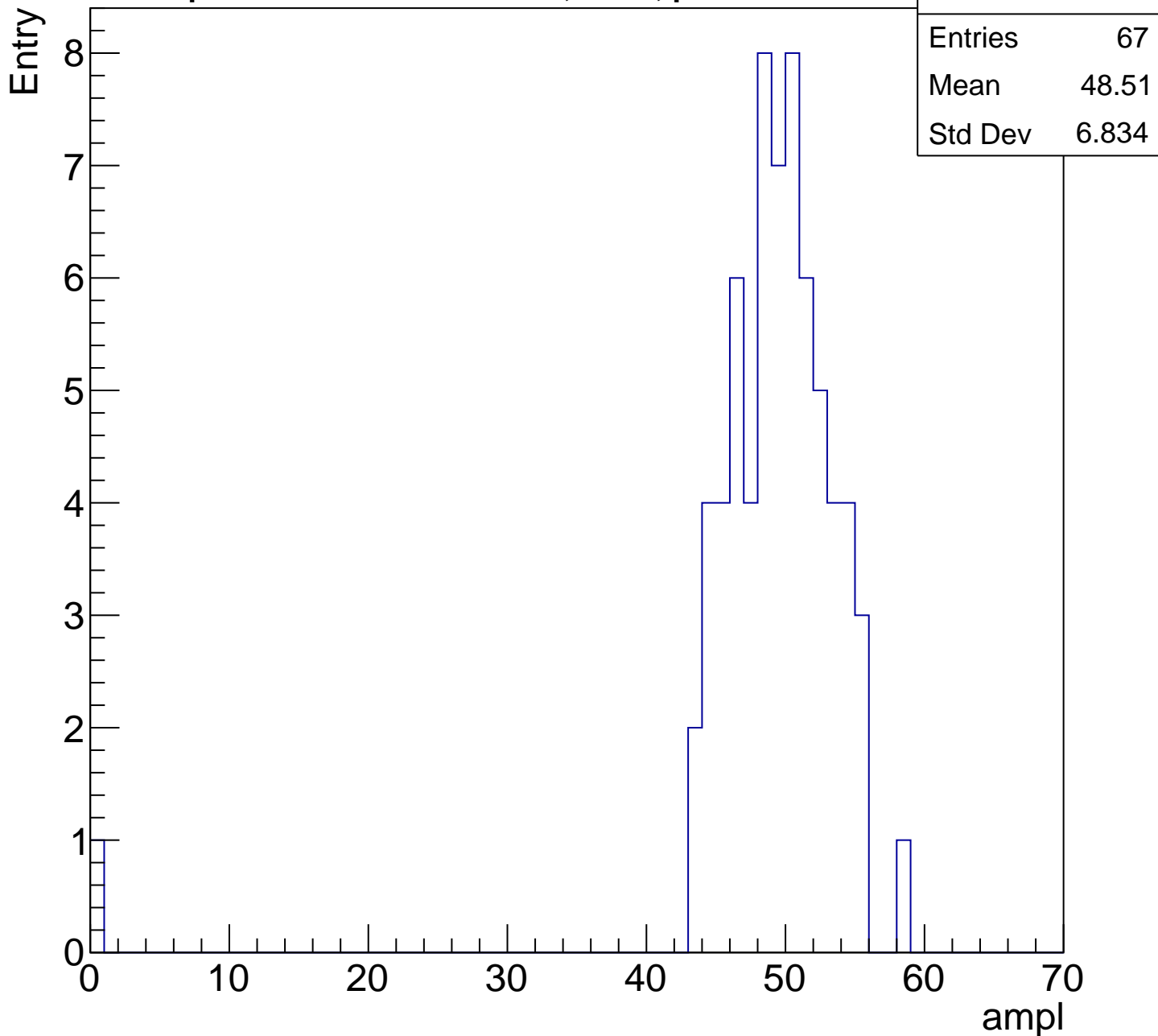
Entry

Entries	58
Mean	41.12
Std Dev	10.04



B1L103S, U9-ch71, adc3

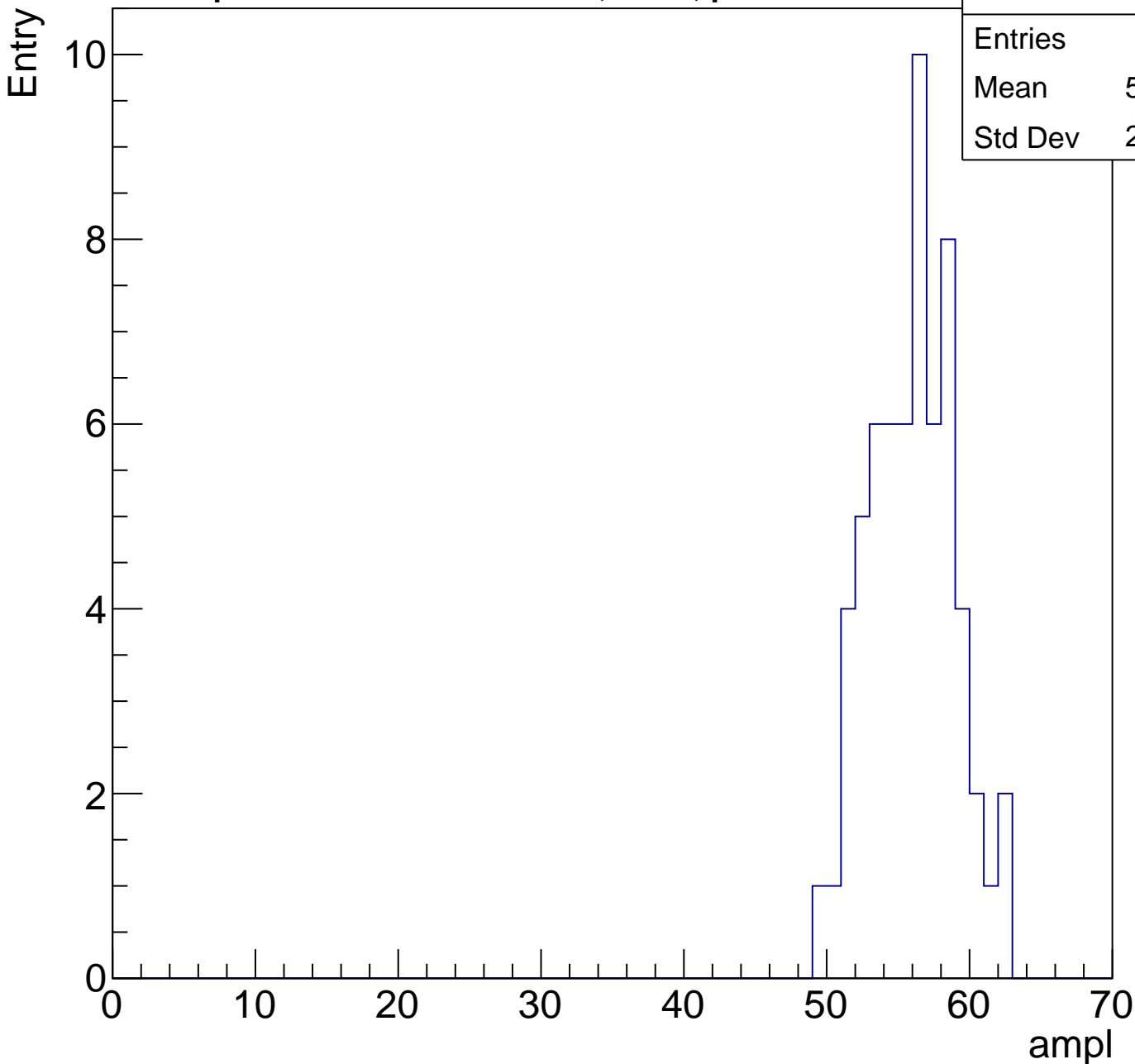
calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U9-ch71, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	62
Mean	55.52
Std Dev	2.944

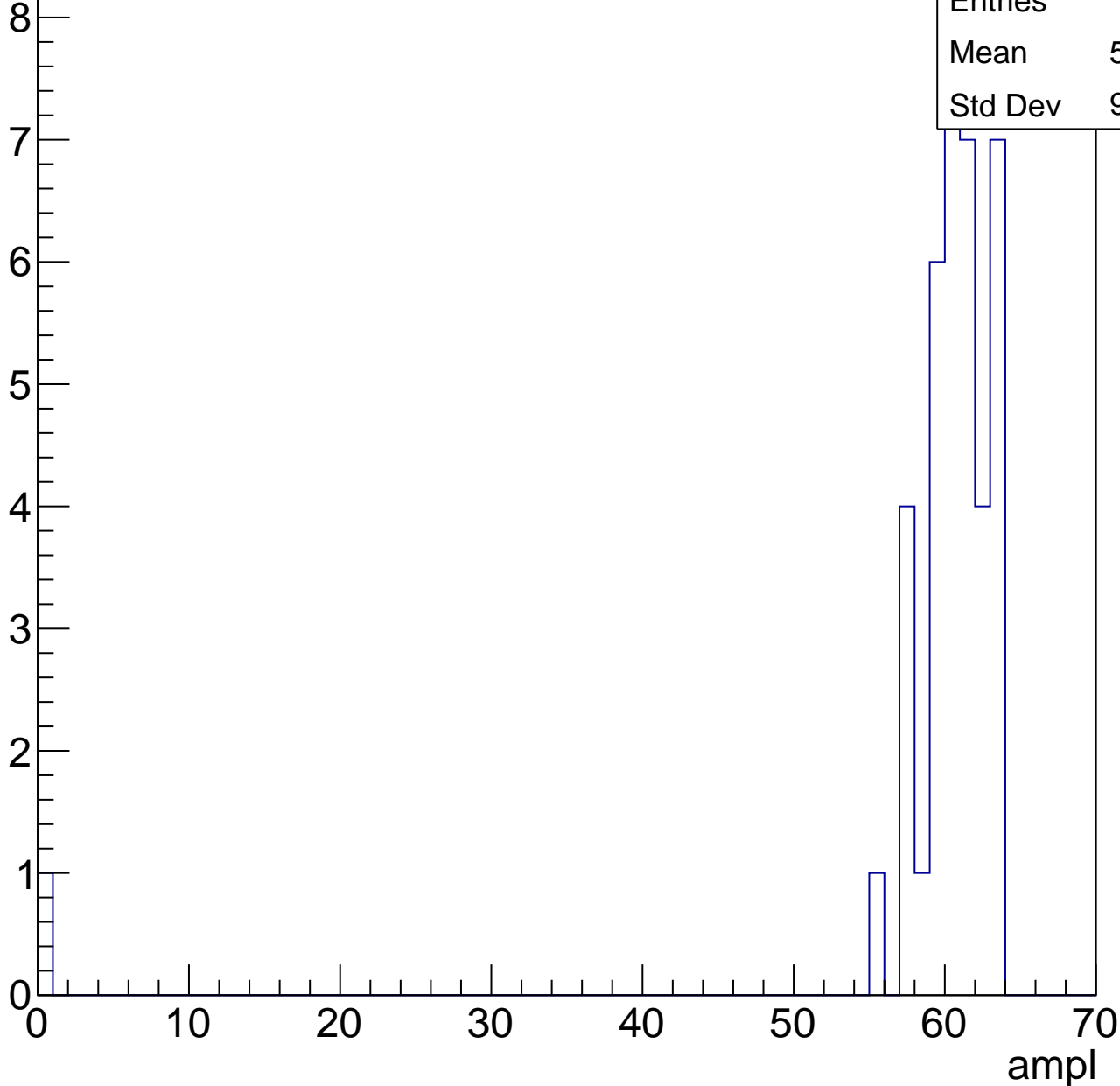


B1L103S, U9-ch71, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	58.74
Std Dev	9.734



B1L103S, U9-ch71, adc6

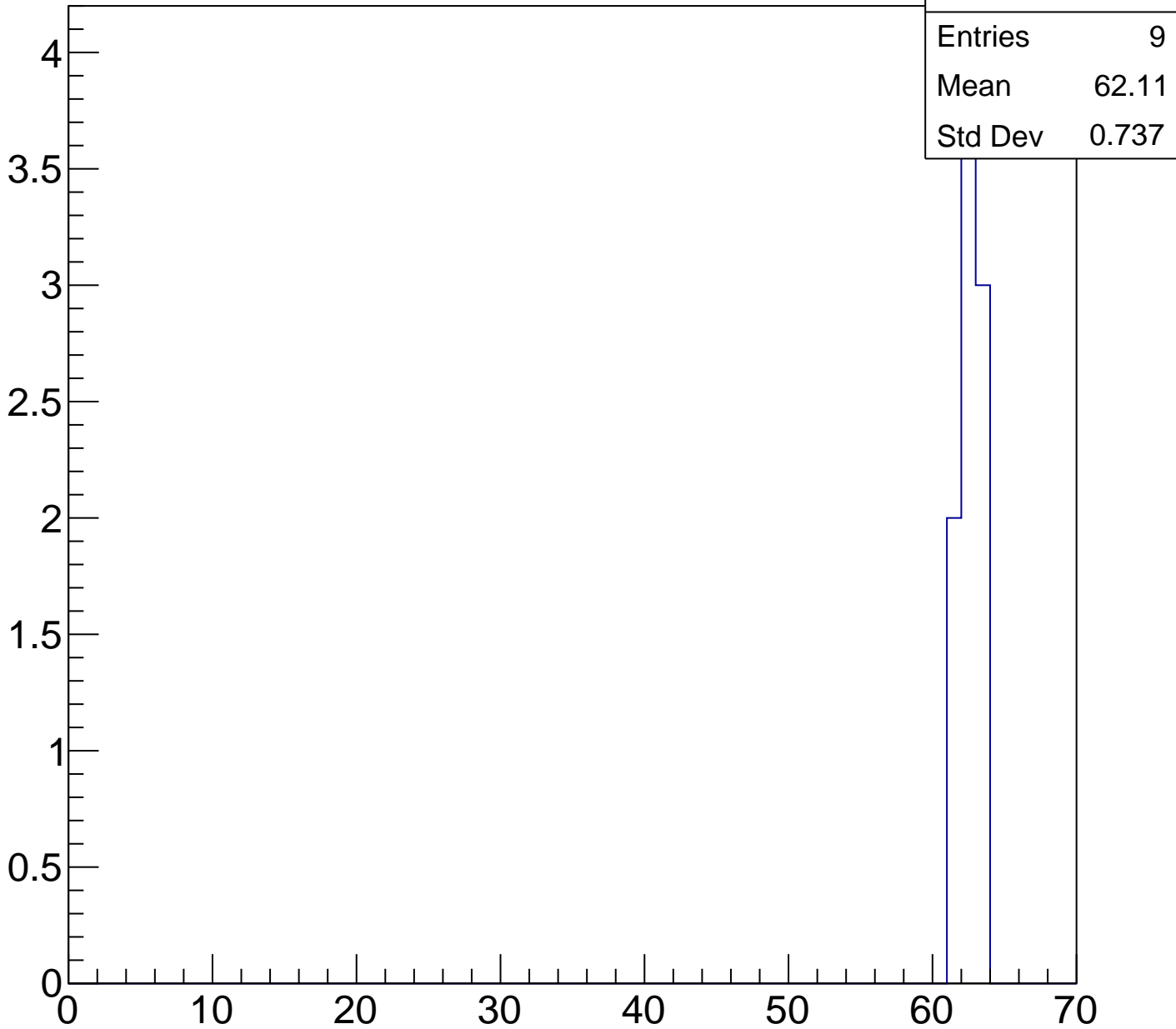
calib_packv5_041523_1651.root, FC#0, port C2

Entry

4
3.5
3
2.5
2
1.5
1
0.5
0

Entries	9
Mean	62.11
Std Dev	0.737

ampl



B1L103S, U9-ch71, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

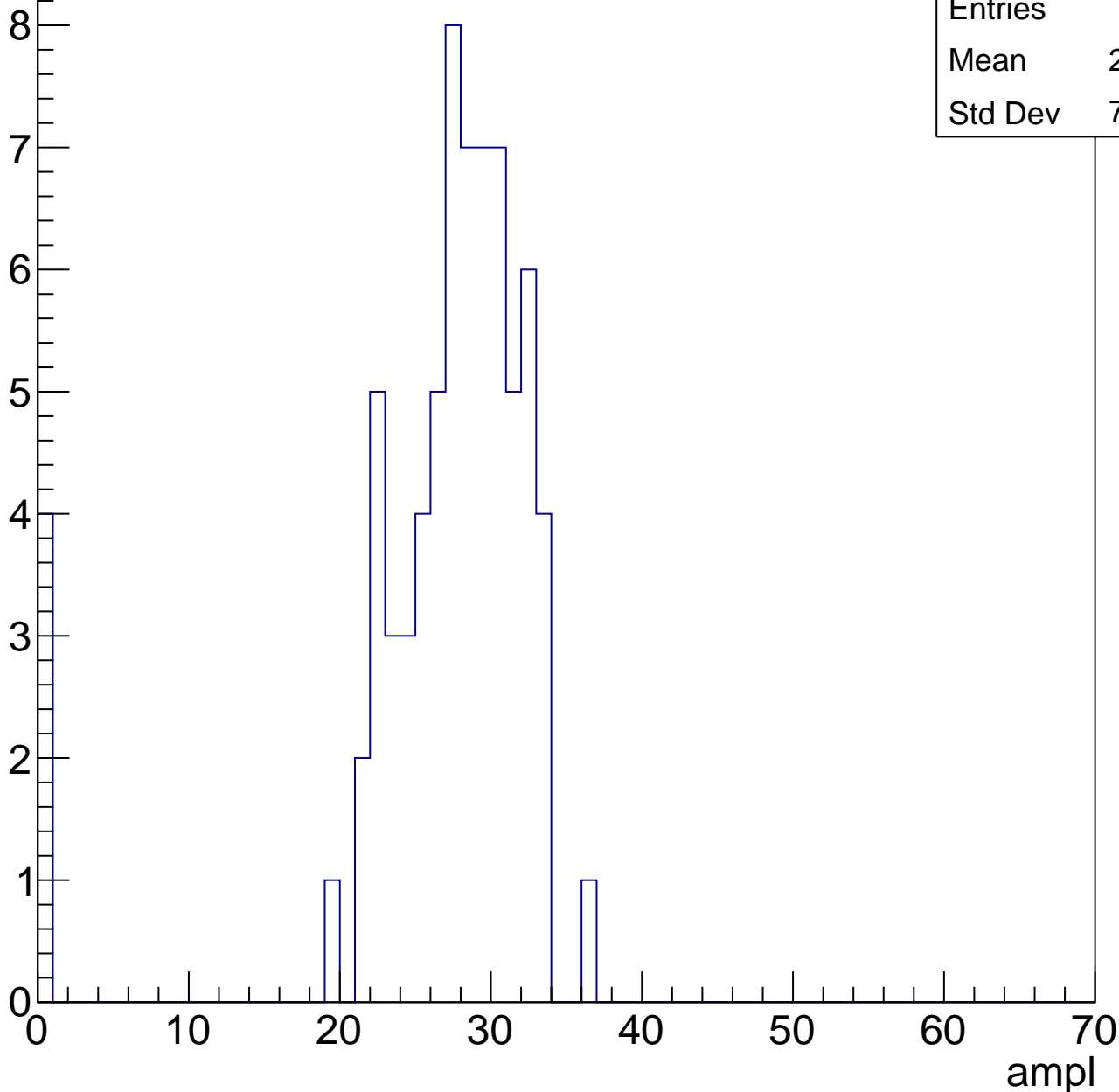


B1L103S, U9-ch72, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	26.14
Std Dev	7.239



B1L103S, U9-ch72, adc1

calib_packv5_041523_1651.root, FC#0, port C2

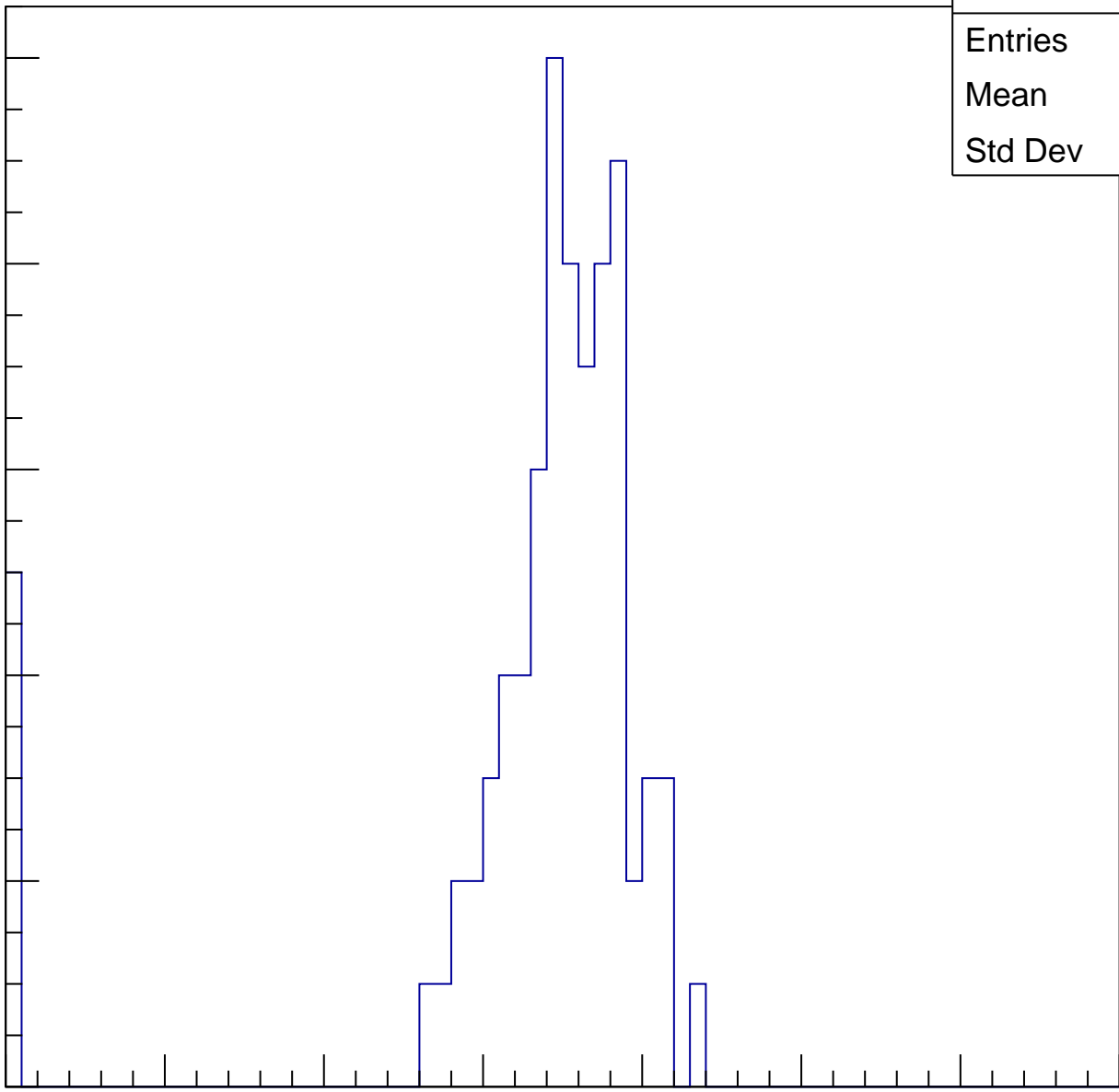
Entries	79
Mean	32.67
Std Dev	9.154

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

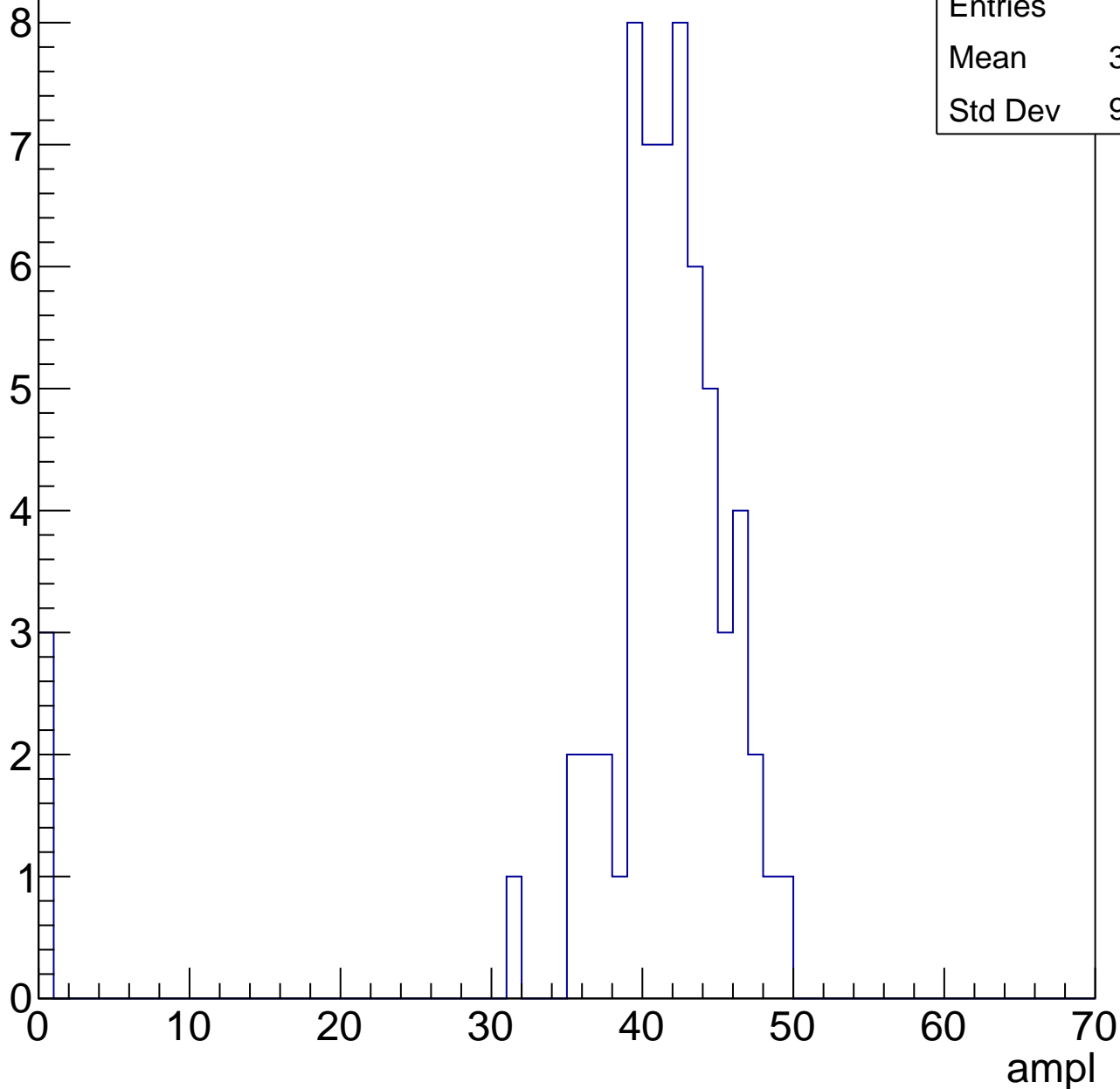


B1L103S, U9-ch72, adc2

calib_packv5_041523_1651.root, FC#0, port C2

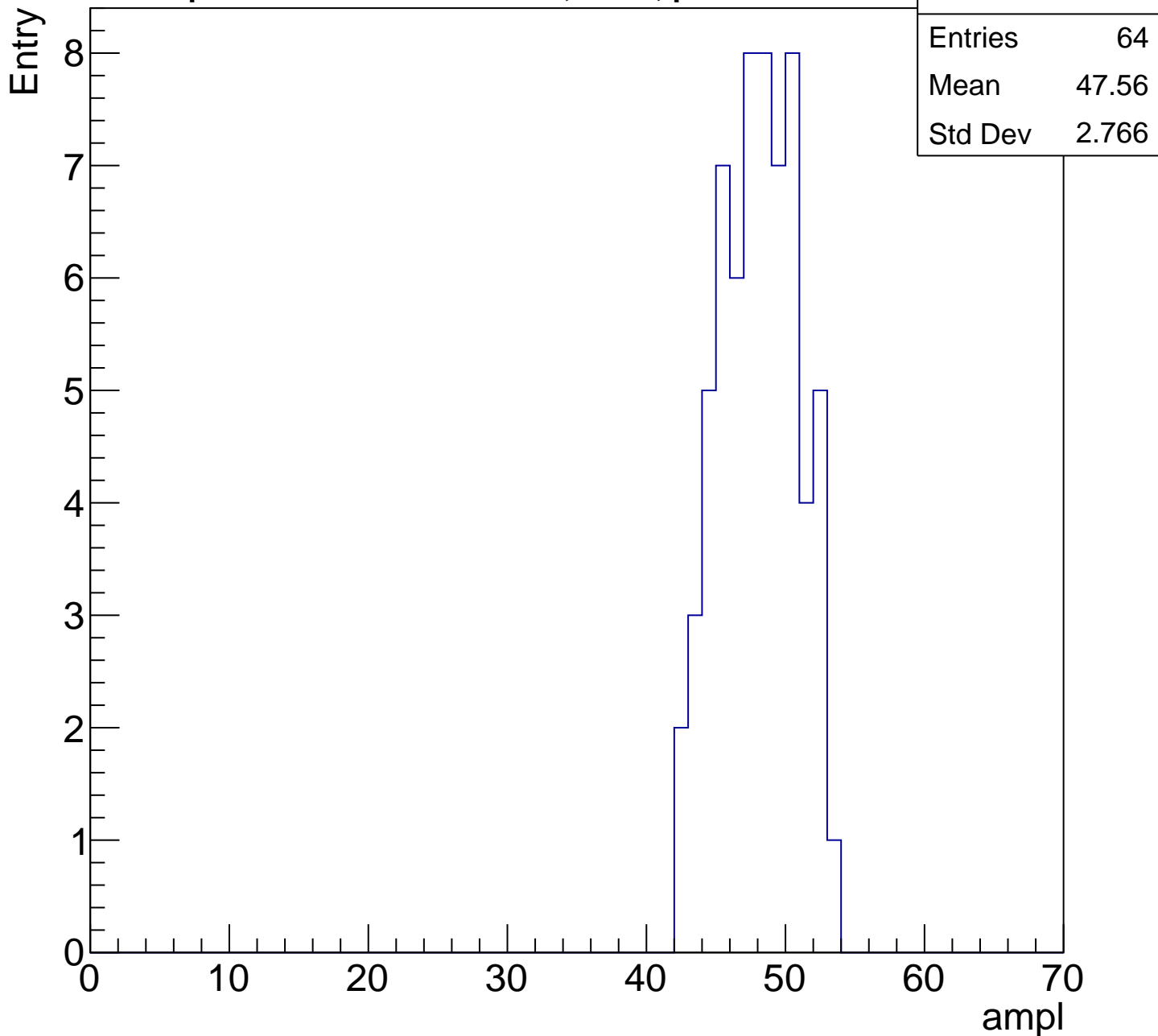
Entry

Entries	63
Mean	39.49
Std Dev	9.438



B1L103S, U9-ch72, adc3

calib_packv5_041523_1651.root, FC#0, port C2

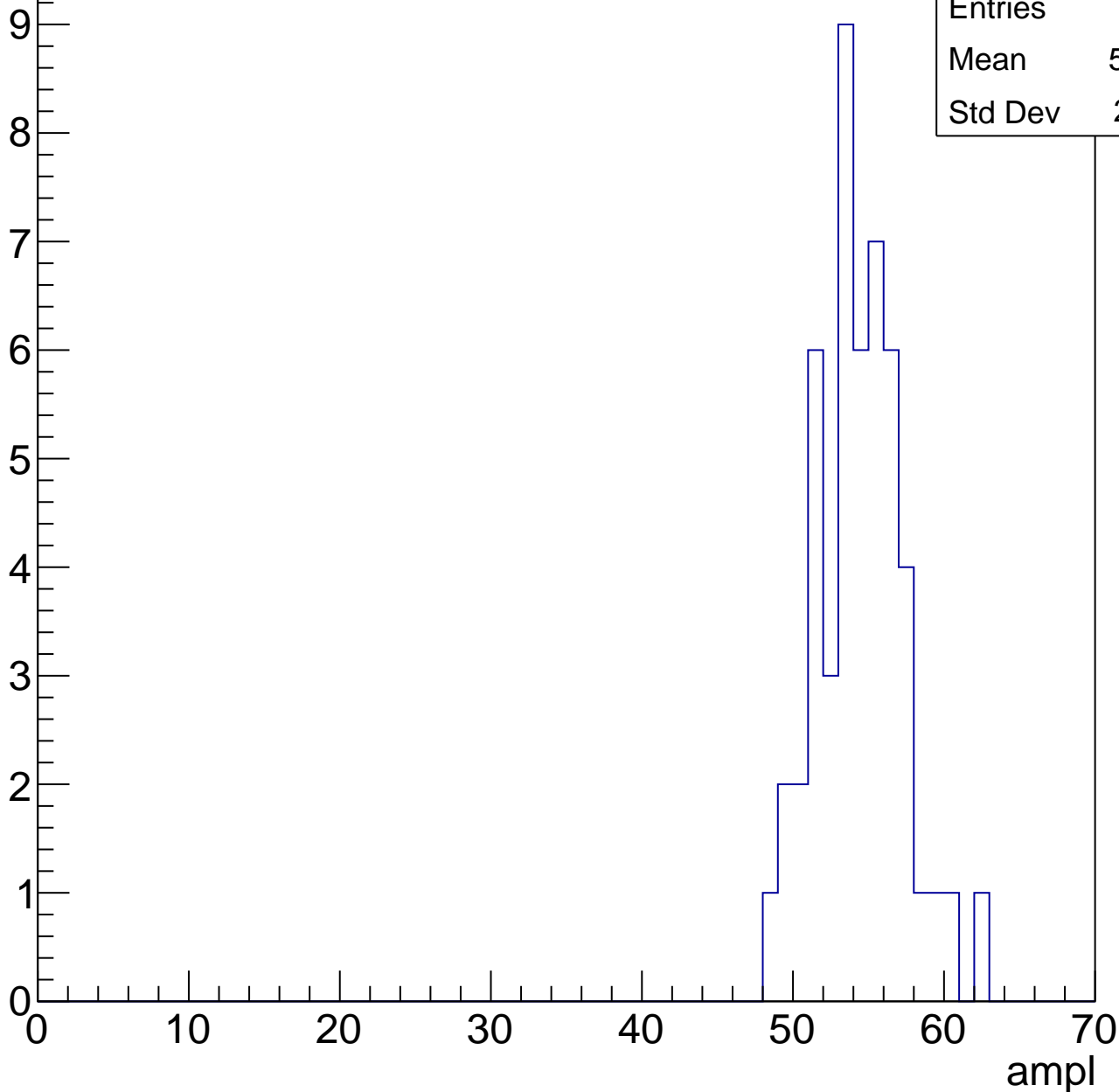


B1L103S, U9-ch72, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

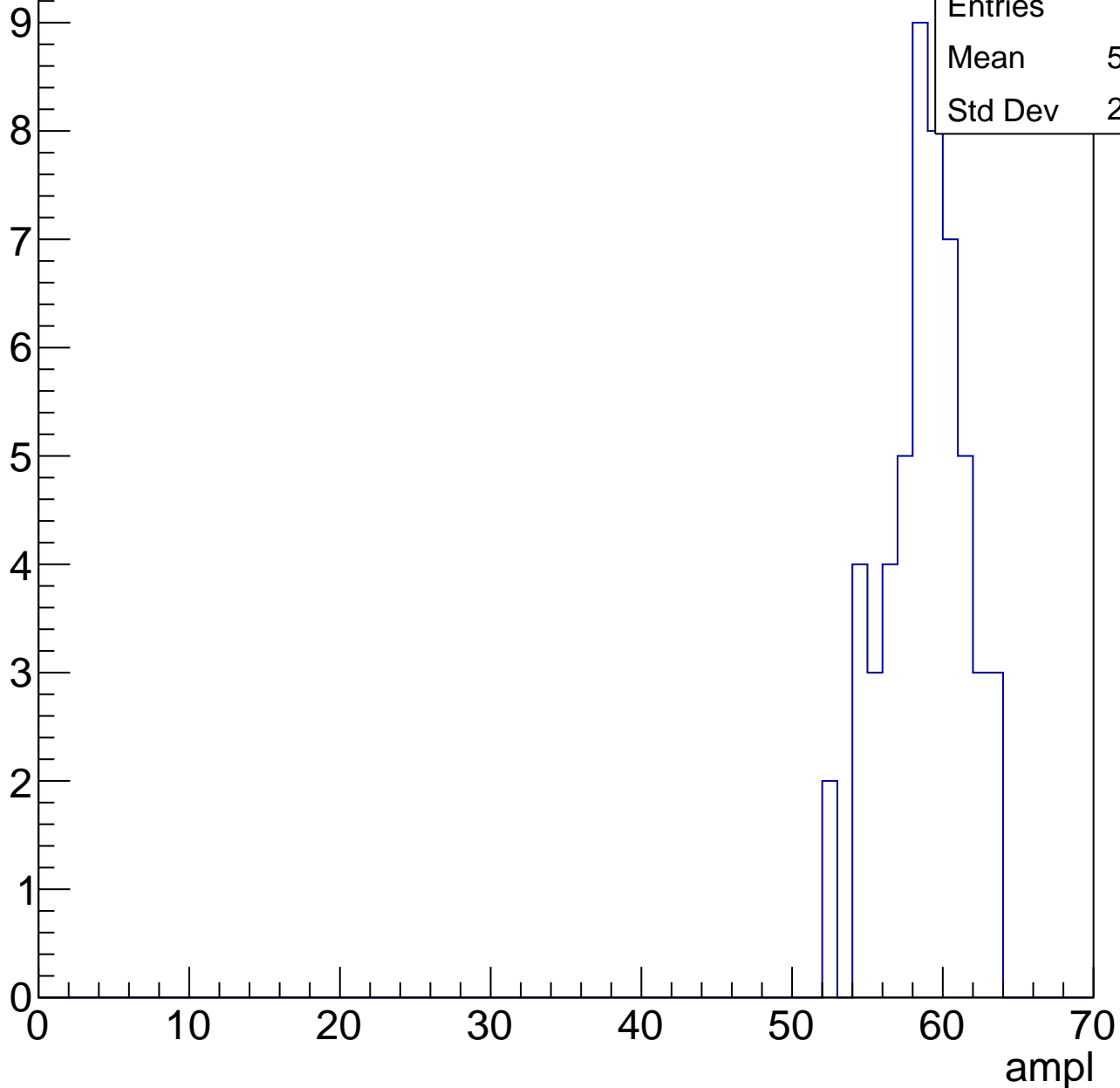
Entries	50
Mean	53.94
Std Dev	2.831



B1L103S, U9-ch72, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

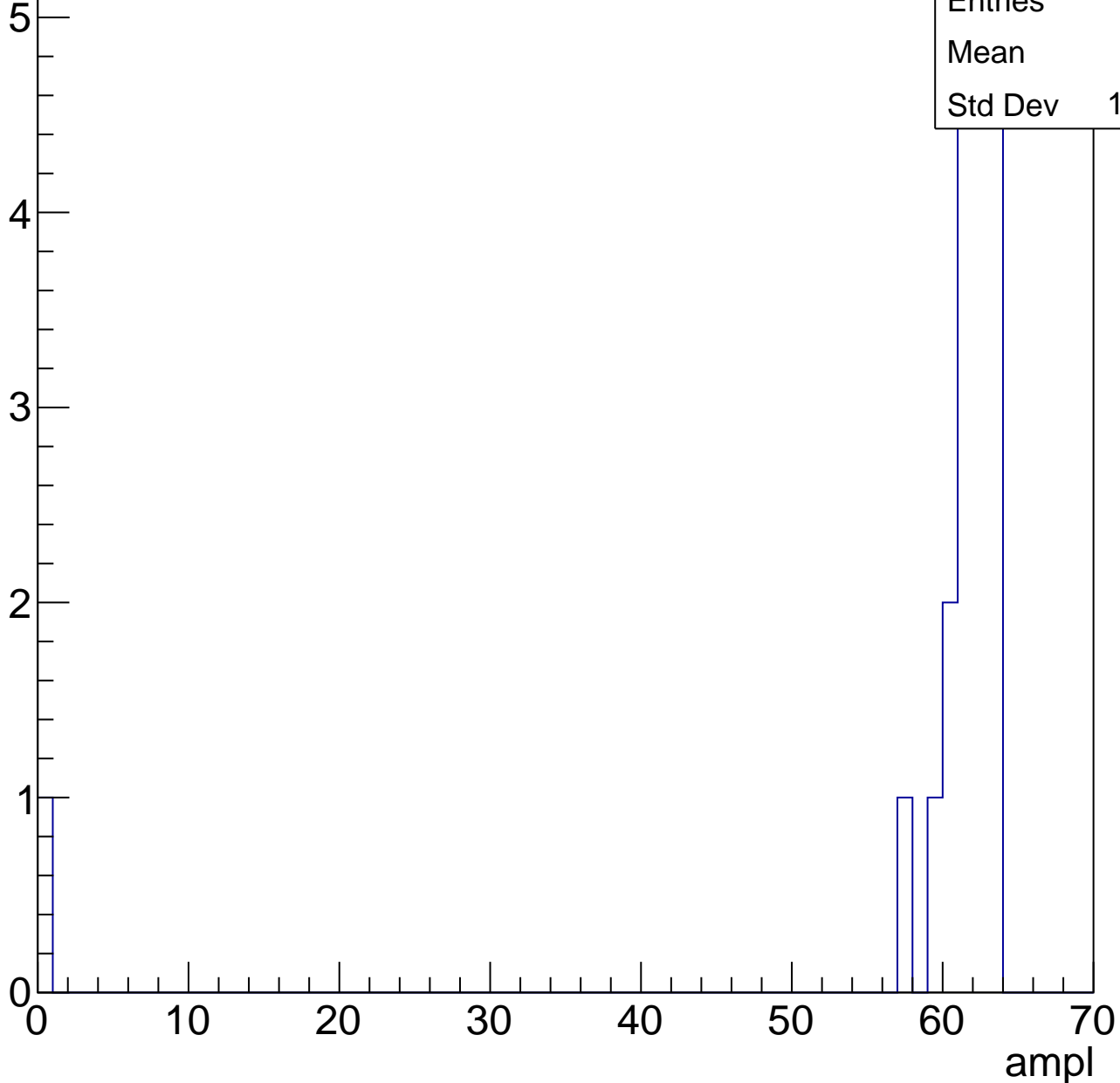


B1L103S, U9-ch72, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	20
Mean	58.3
Std Dev	13.46



B1L103S, U9-ch72, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	22
Mean	8.545
Std Dev	21.51

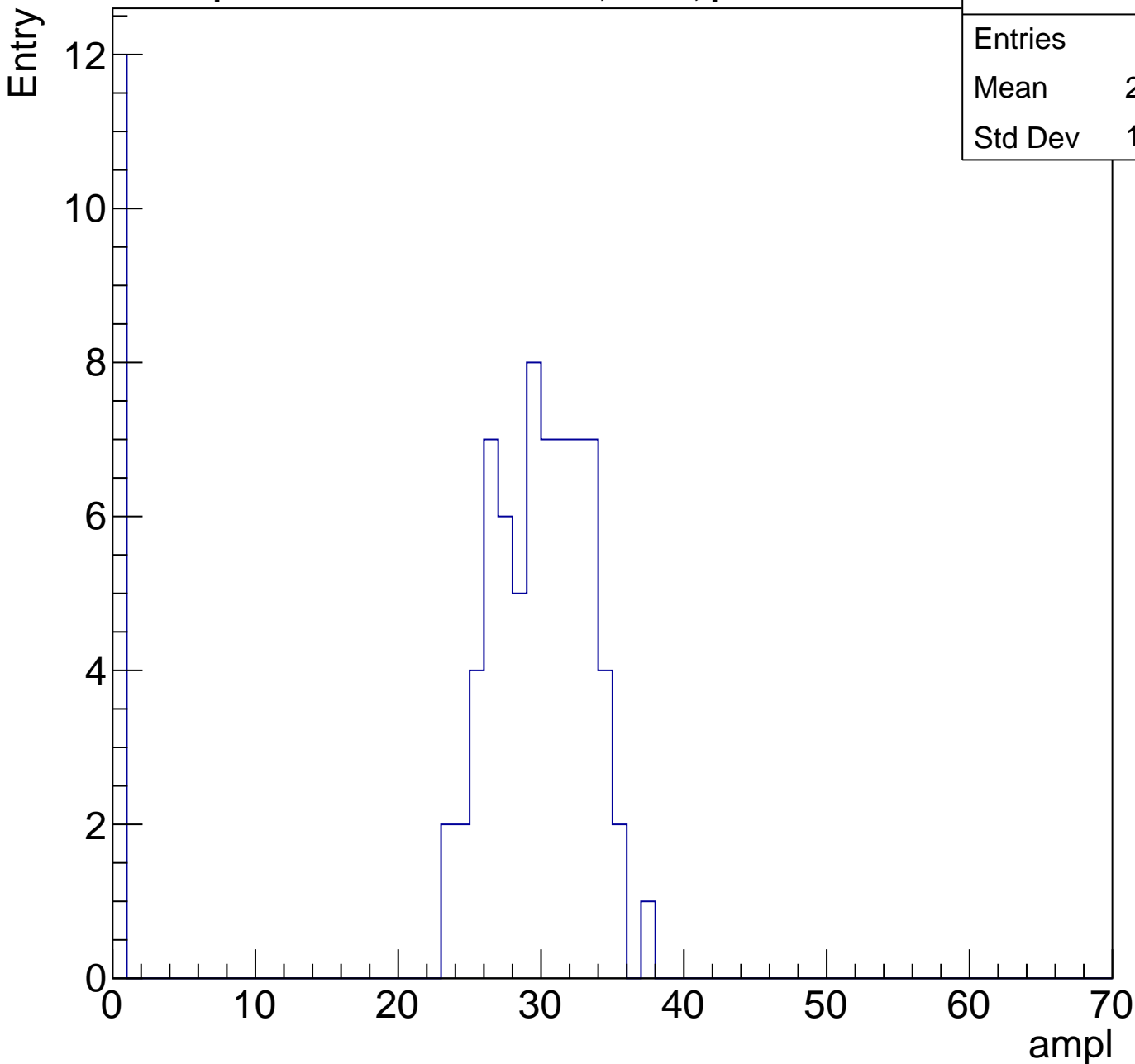
Entry



B1L103S, U9-ch73, adc0

calib_packv5_041523_1651.root, FC#0, port C2

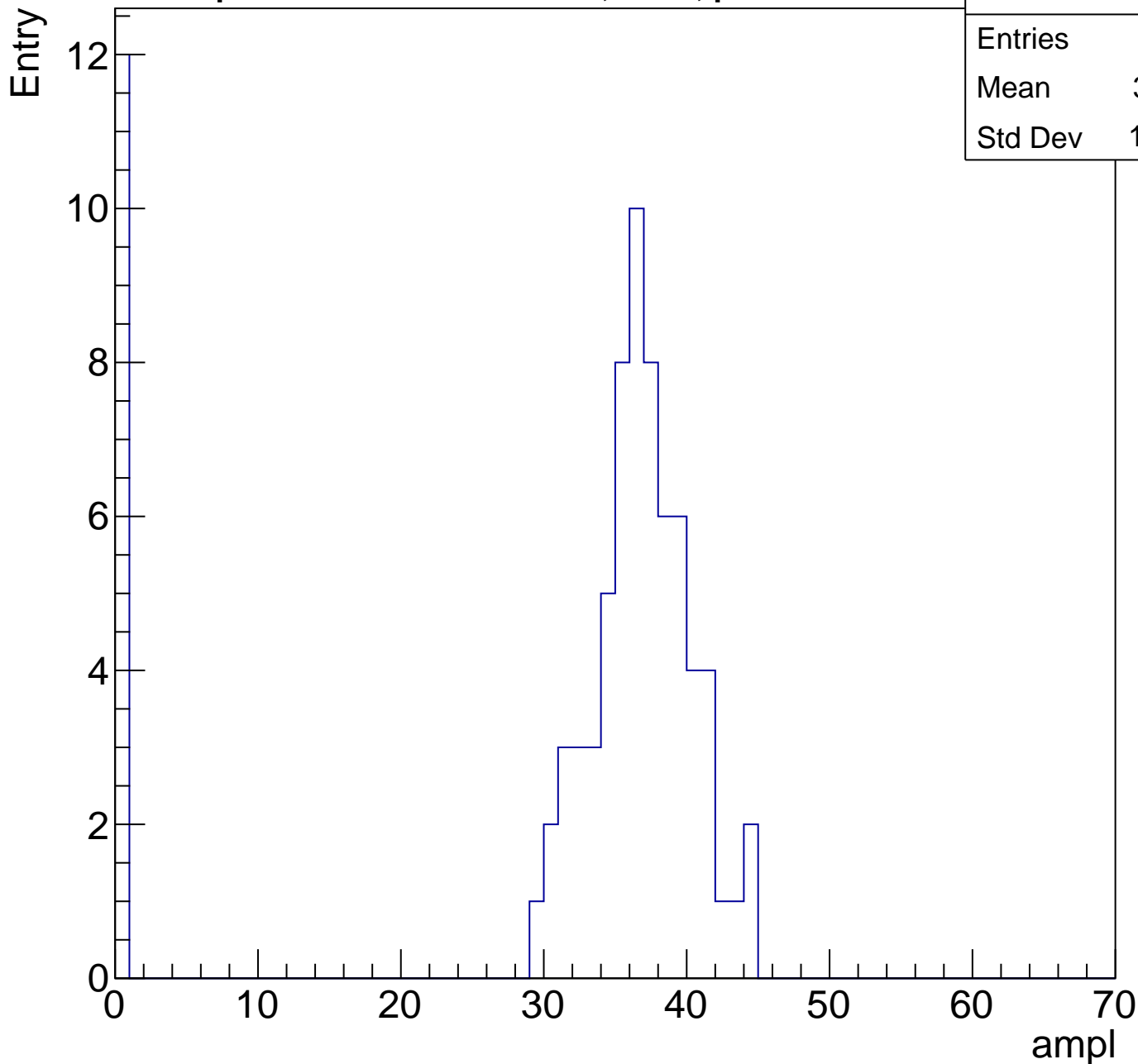
Entries	81
Mean	25.12
Std Dev	10.89



B1L103S, U9-ch73, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	79
Mean	30.91
Std Dev	13.44

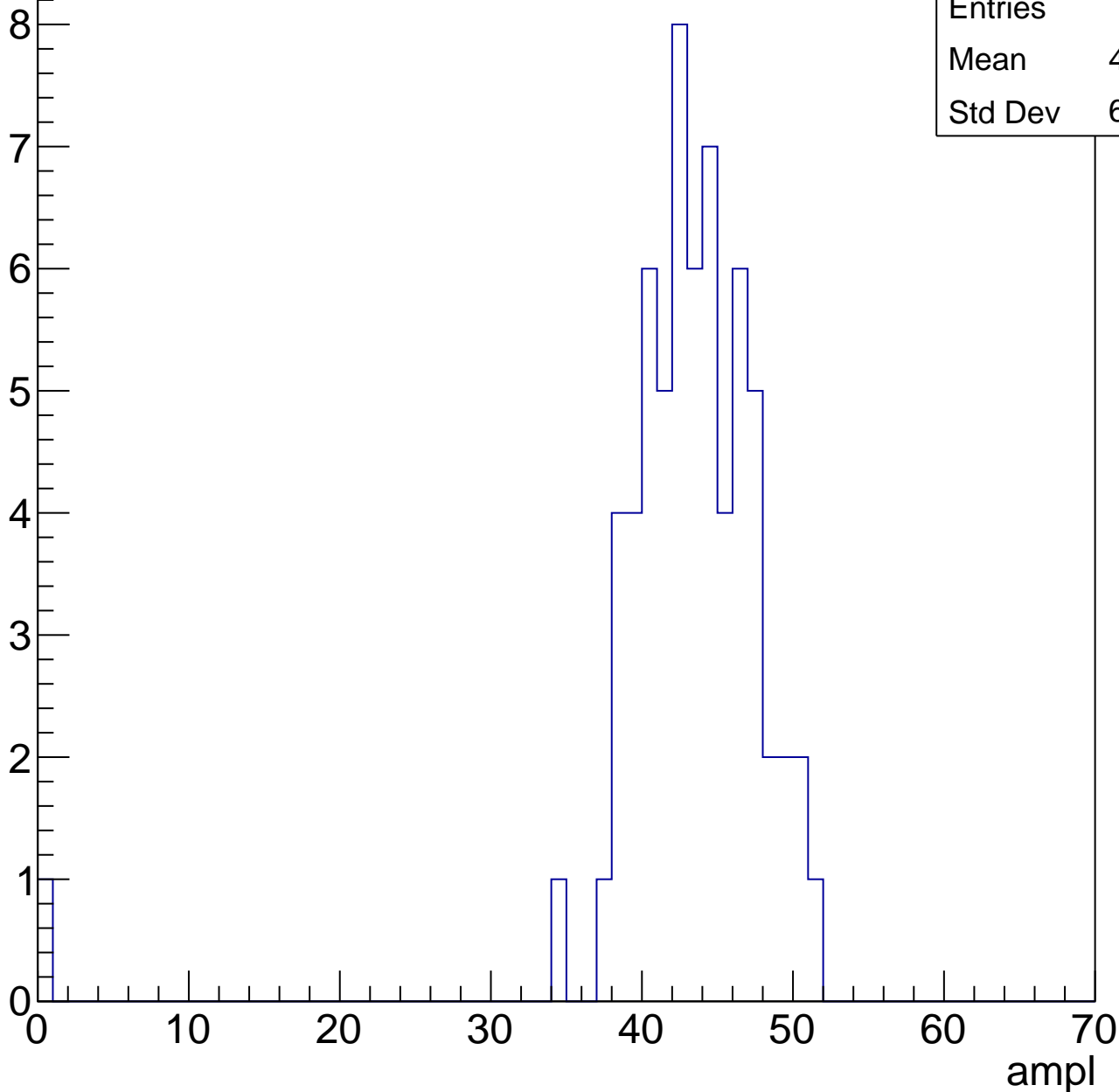


B1L103S, U9-ch73, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	42.49
Std Dev	6.368

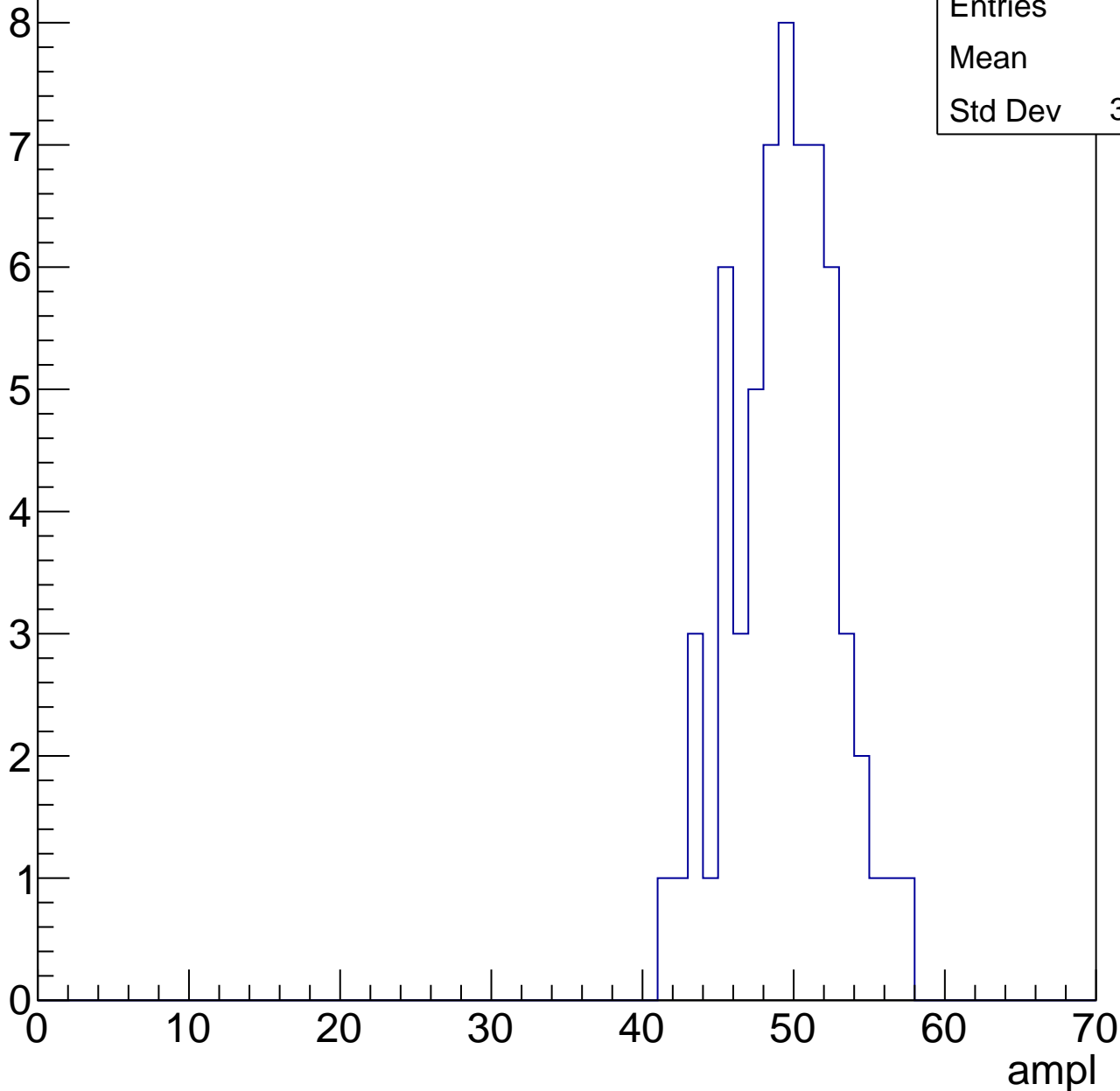


B1L103S, U9-ch73, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	48.9
Std Dev	3.407

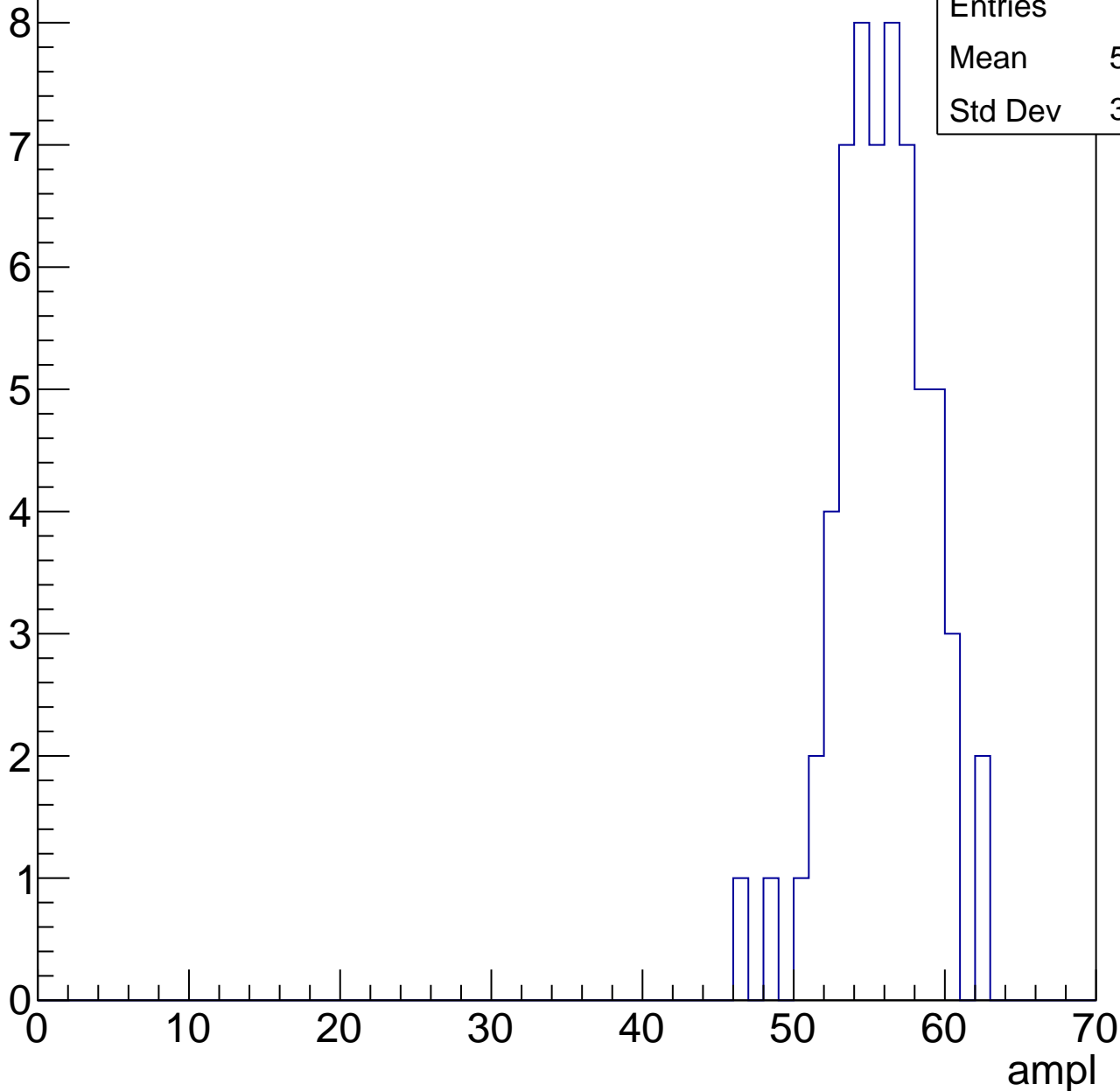


B1L103S, U9-ch73, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	55.38
Std Dev	3.095



B1L103S, U9-ch73, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

Entries	45
Mean	58.78
Std Dev	9.104

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

B1L103S, U9-ch73, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch73, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

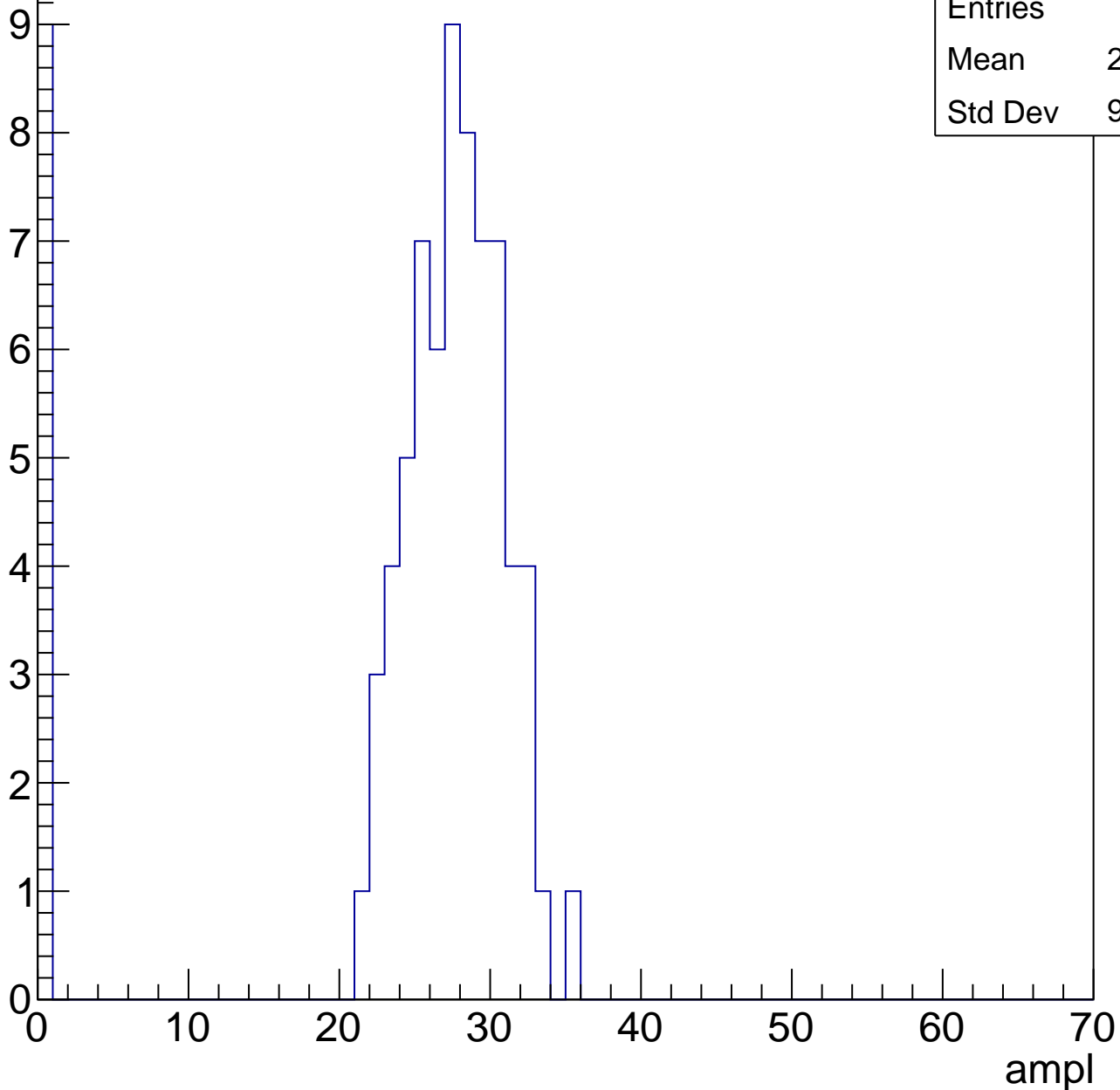


B1L103S, U9-ch74, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	24.08
Std Dev	9.269

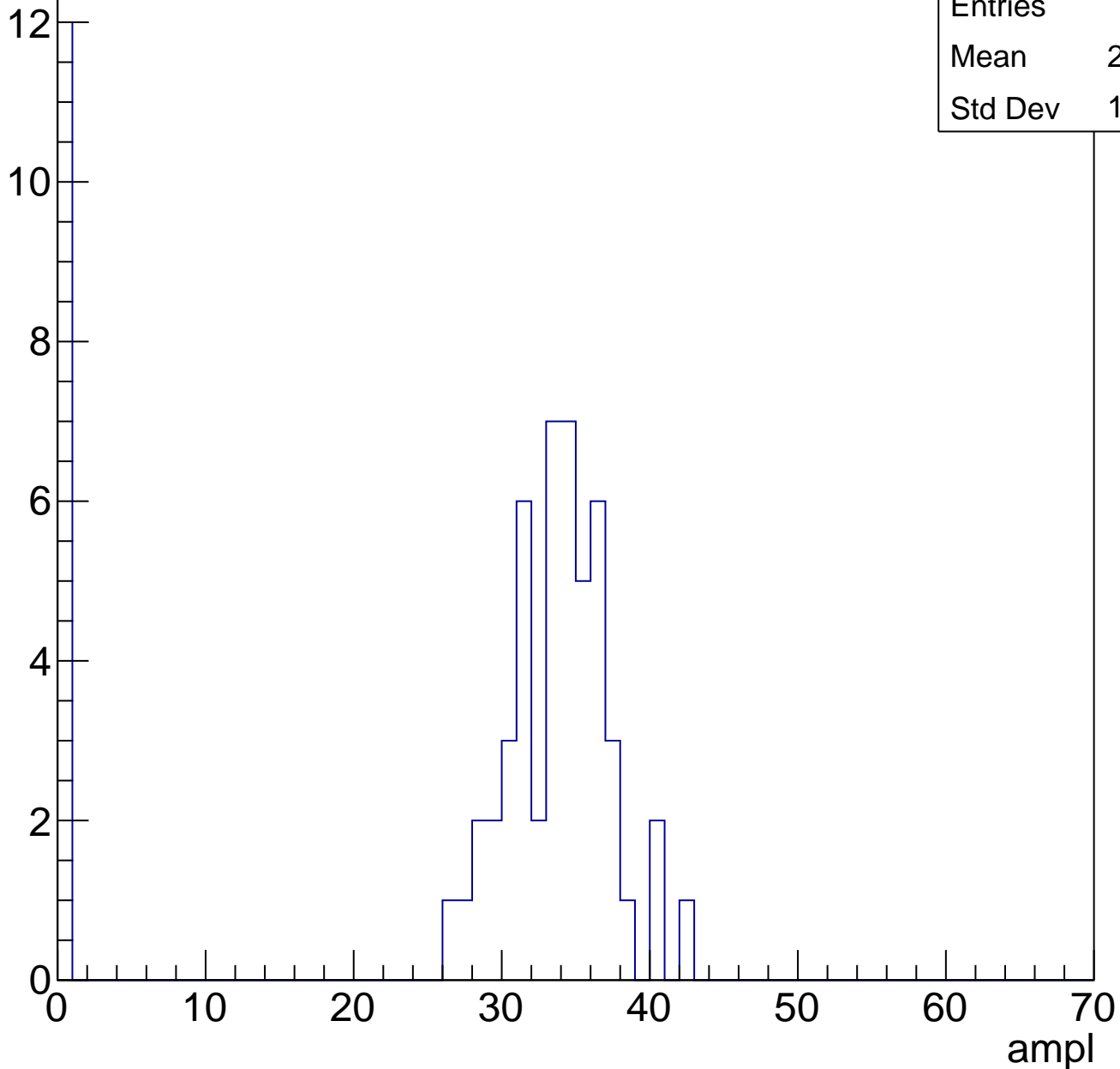


B1L103S, U9-ch74, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	61
Mean	26.85
Std Dev	13.62

Entry

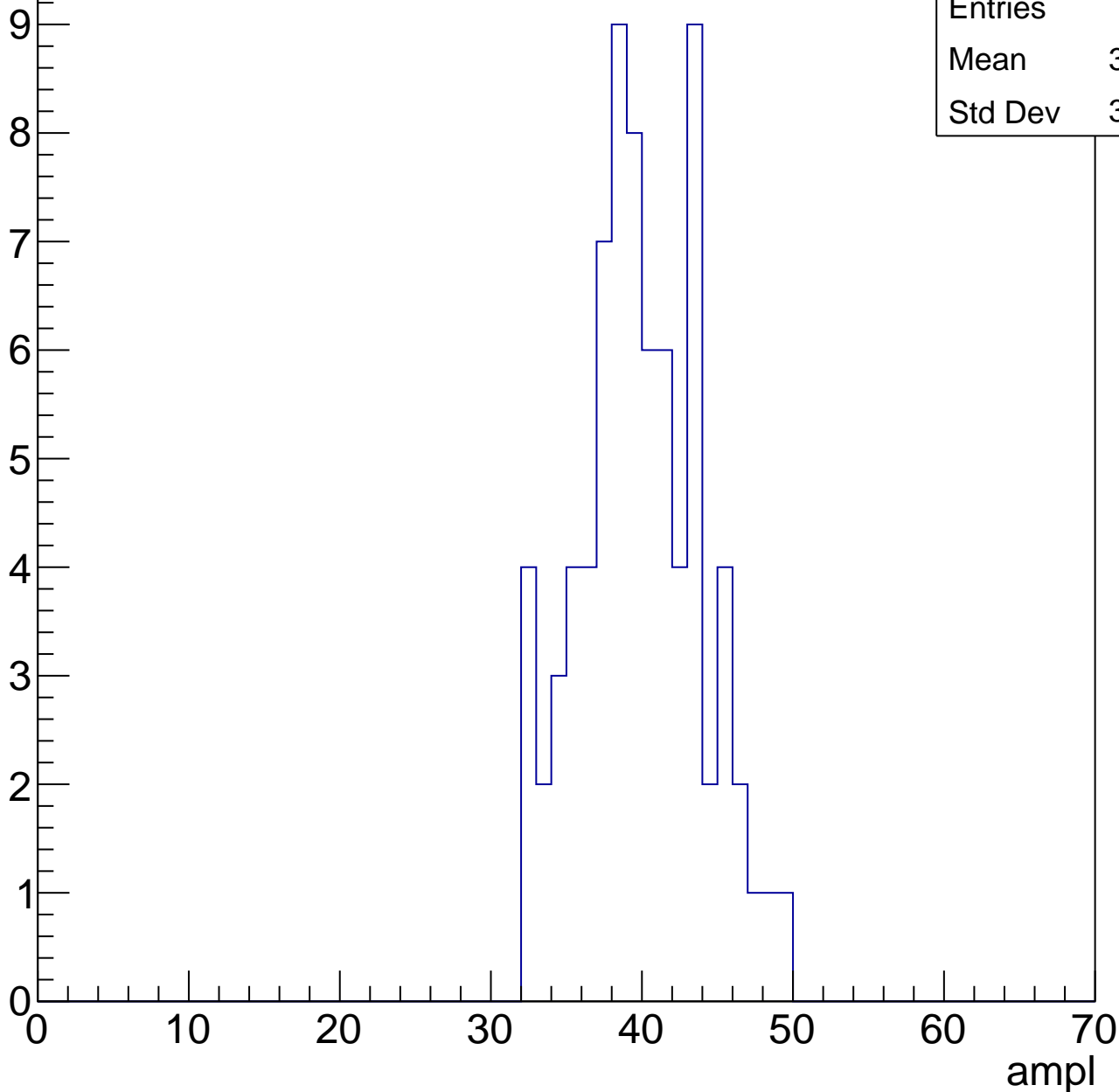


B1L103S, U9-ch74, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	39.45
Std Dev	3.966

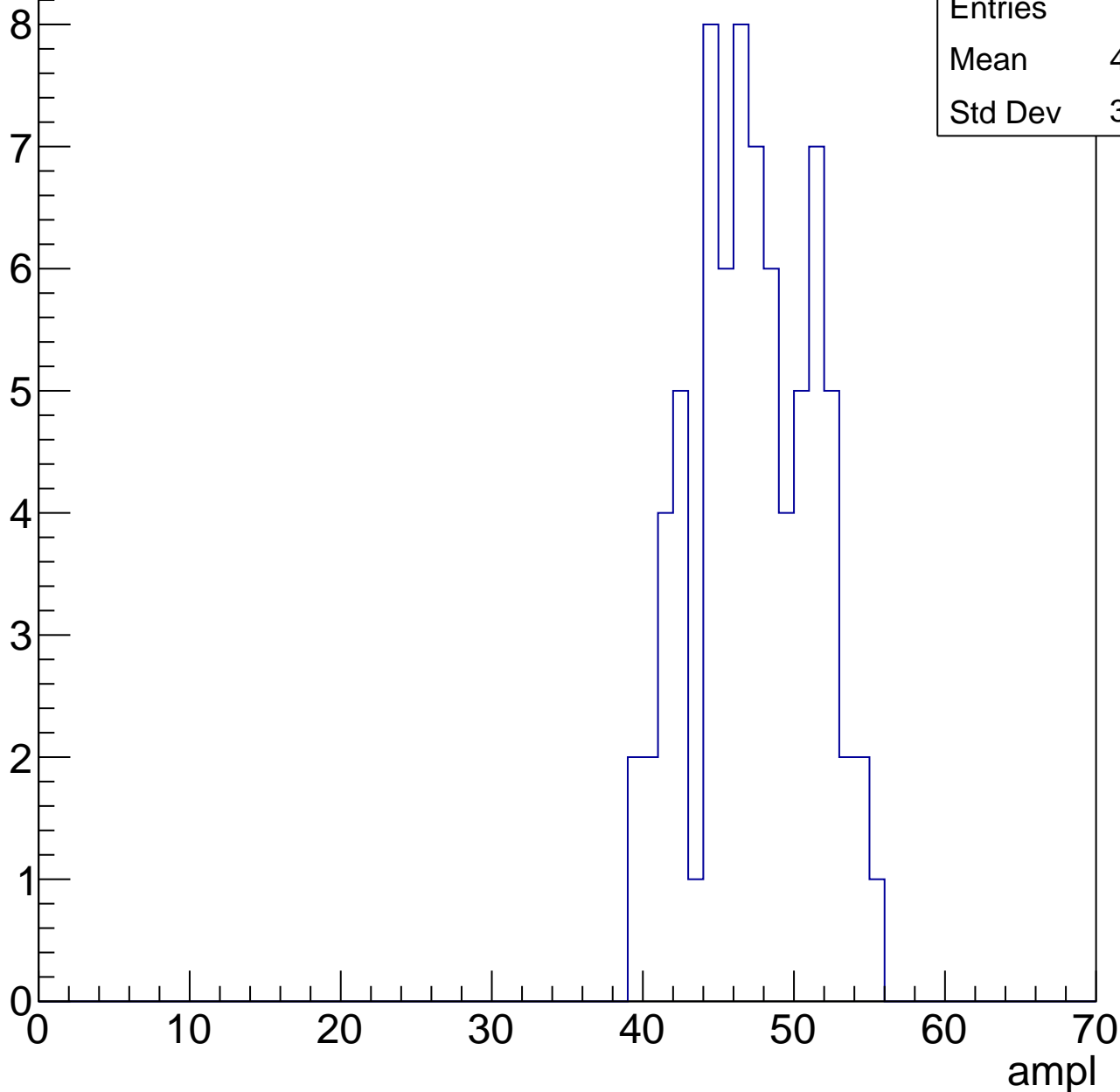


B1L103S, U9-ch74, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	46.85
Std Dev	3.918

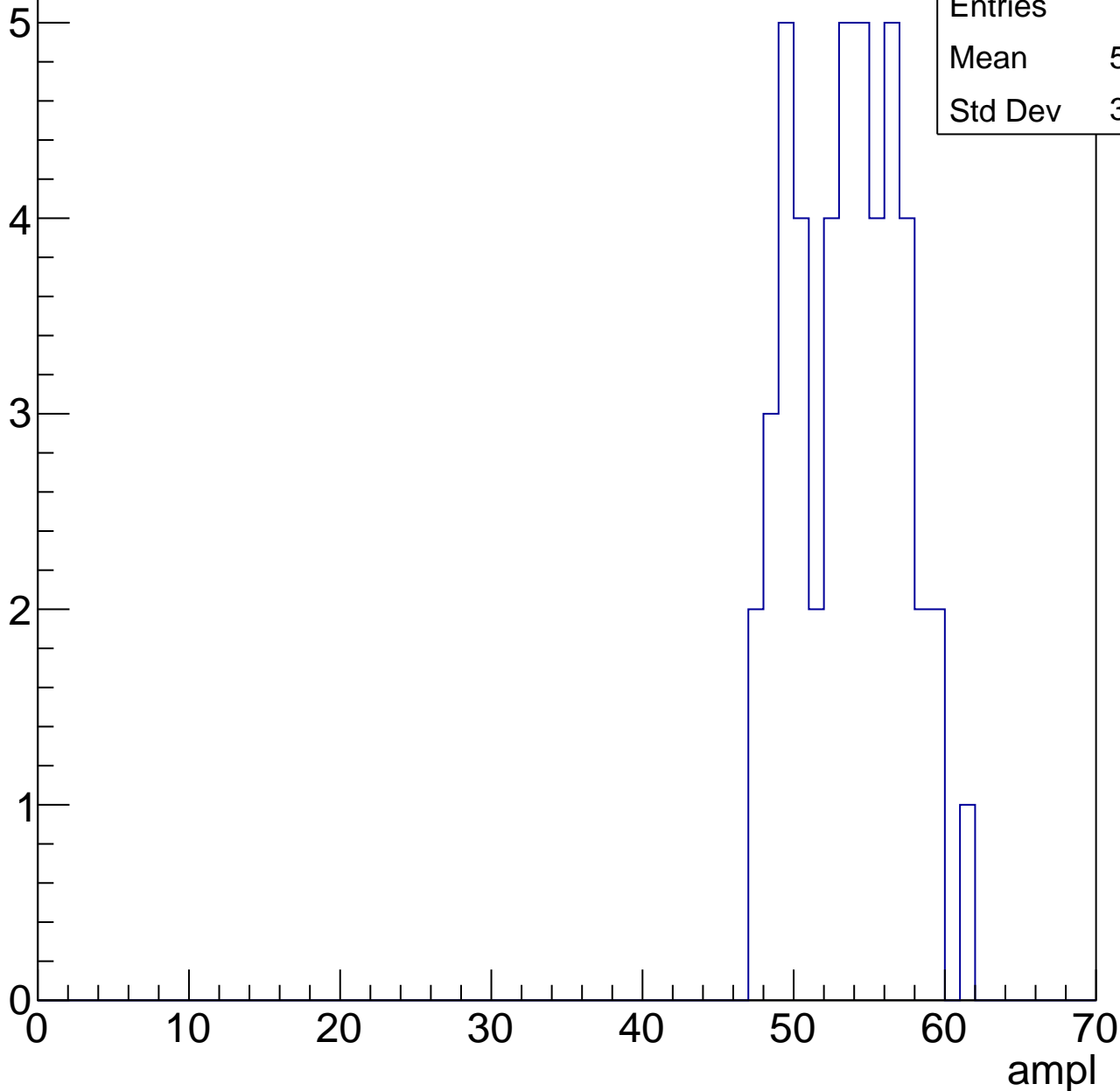


B1L103S, U9-ch74, adc4

calib_packv5_041523_1651.root, FC#0, port C2

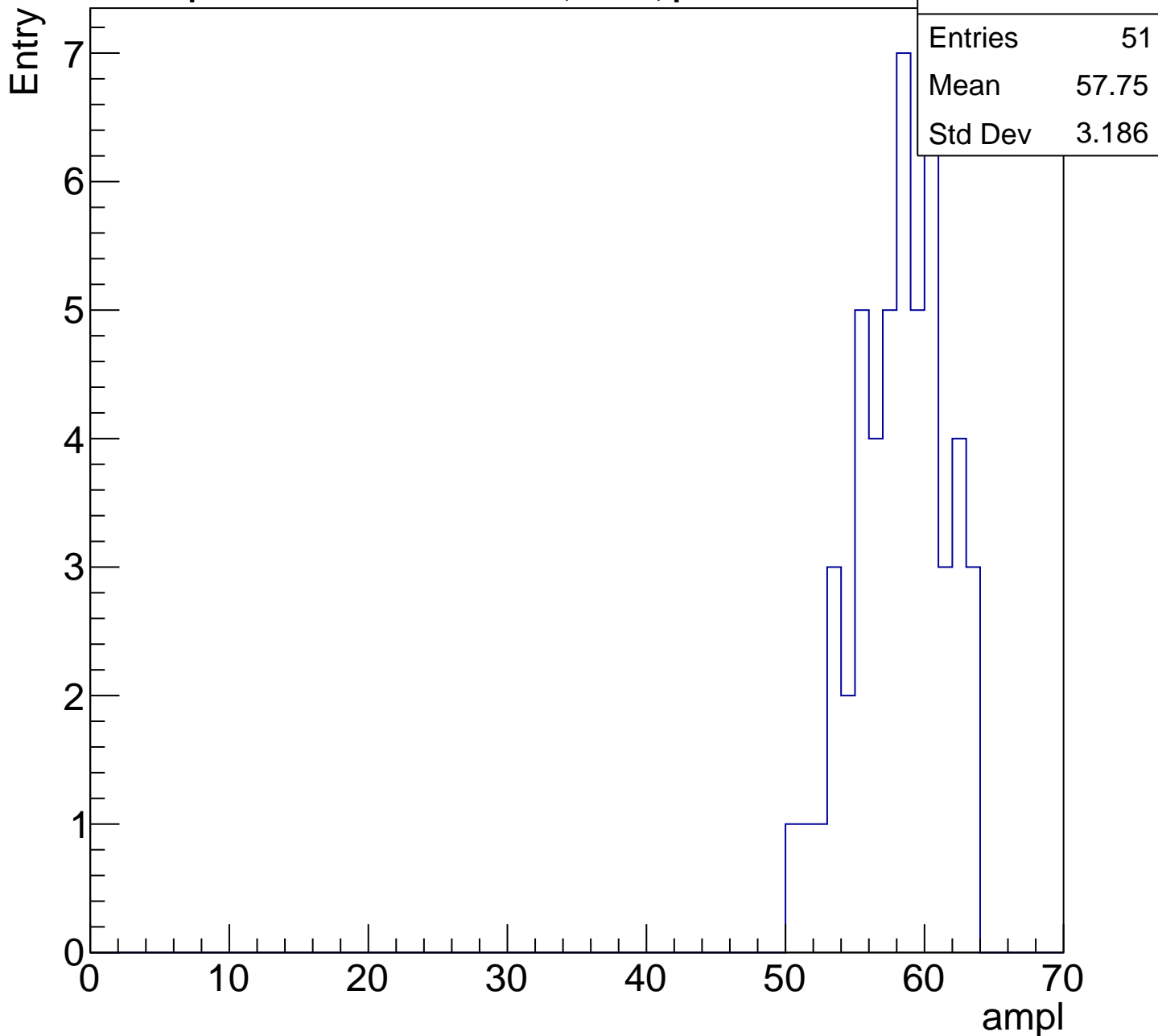
Entry

Entries	48
Mean	53.15
Std Dev	3.506



B1L103S, U9-ch74, adc5

calib_packv5_041523_1651.root, FC#0, port C2

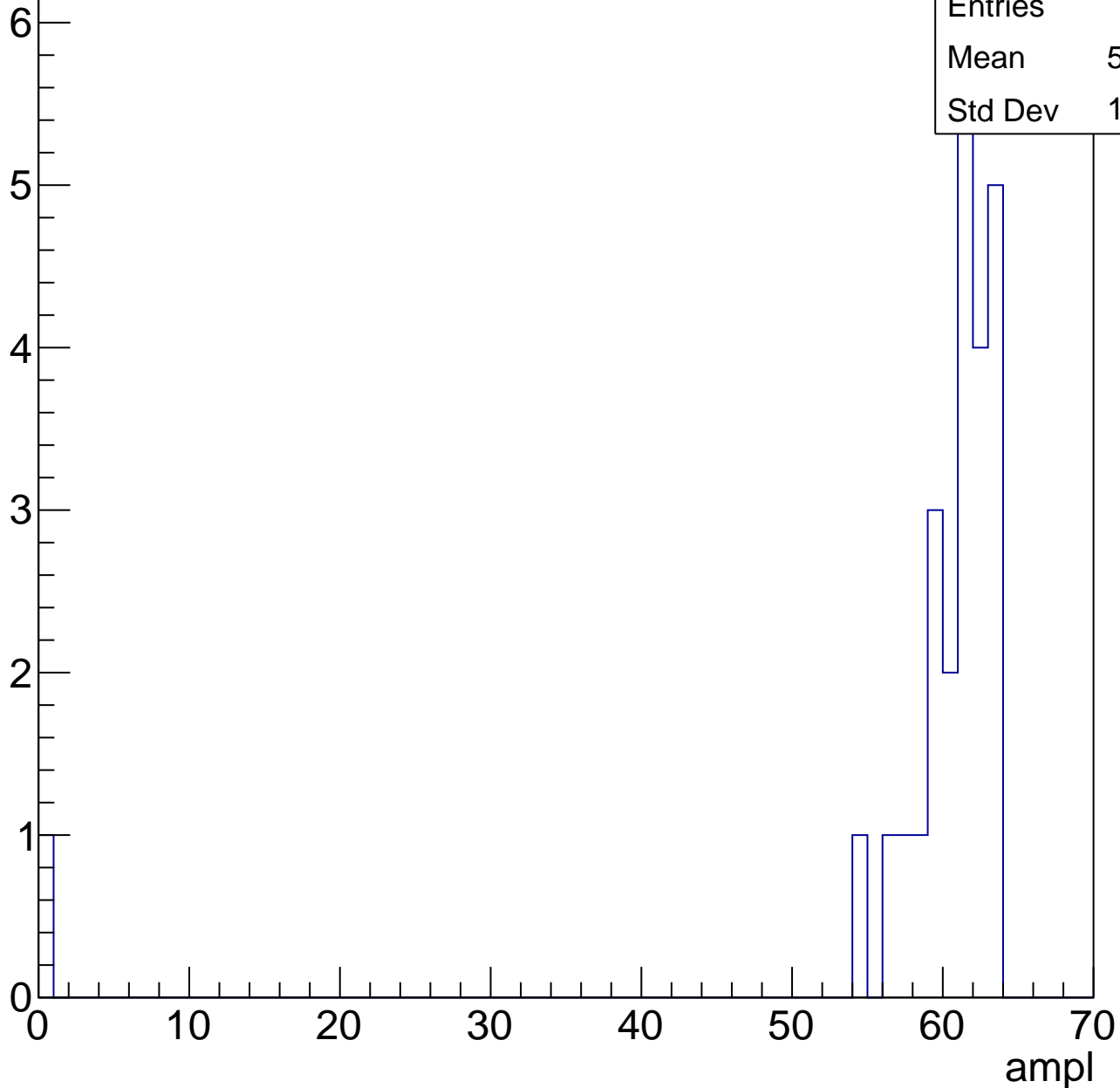


B1L103S, U9-ch74, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	25
Mean	58.04
Std Dev	12.06

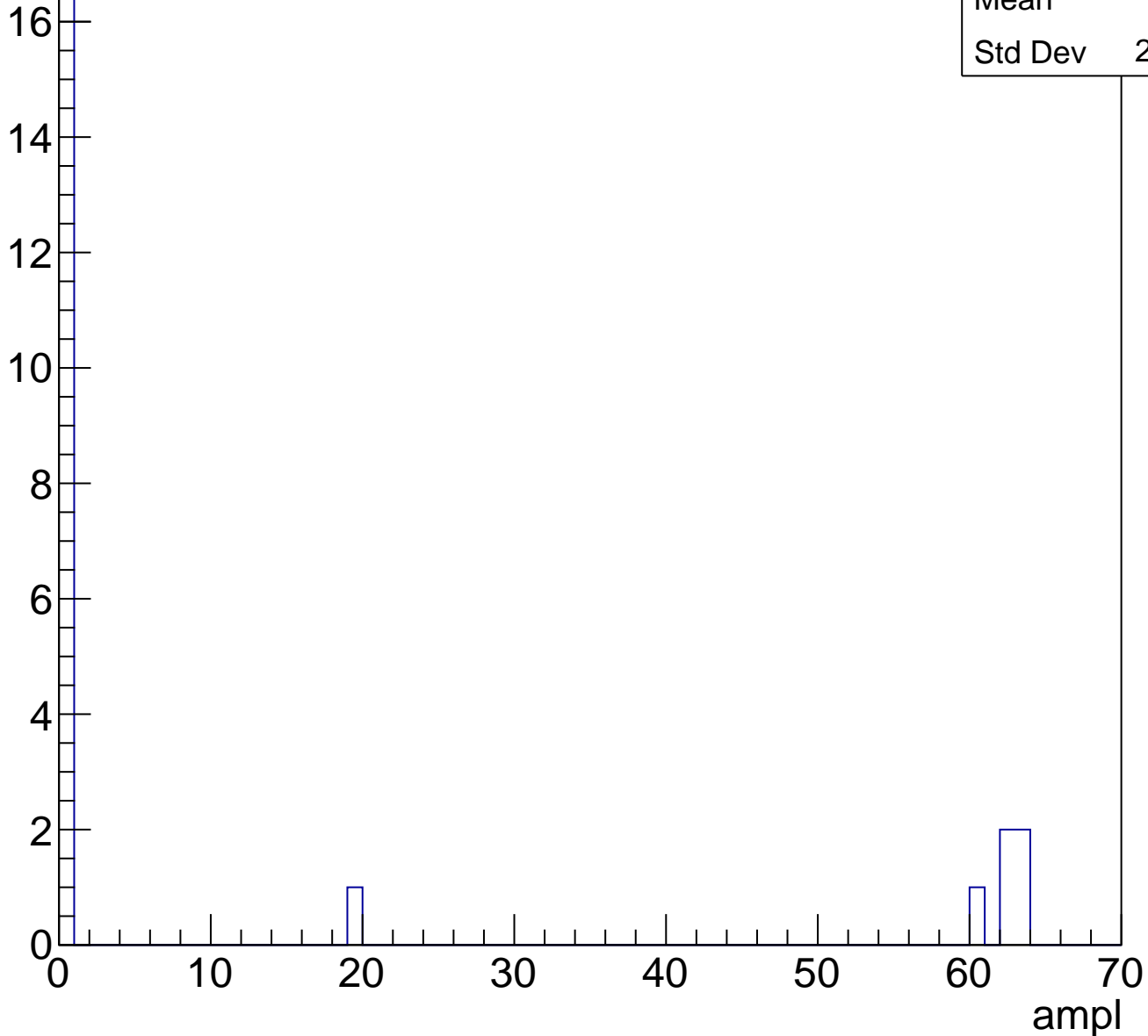


B1L103S, U9-ch74, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	23
Mean	14.3
Std Dev	25.44

Entry



B1L103S, U9-ch75, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	97
Mean	24.71
Std Dev	10.29

Entry

12

10

8

6

4

2

0

0

10

20

30

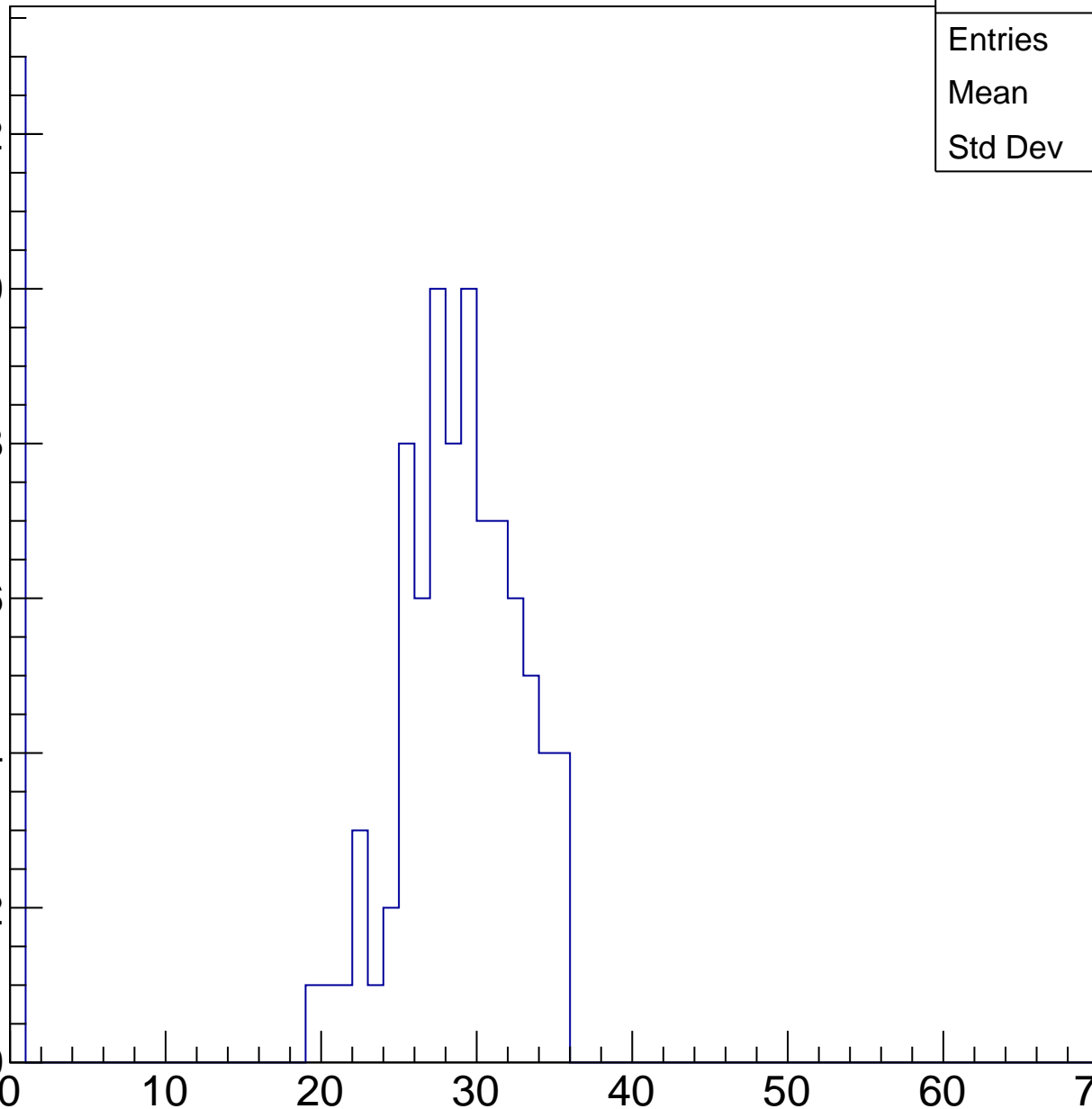
40

50

60

70

ampl

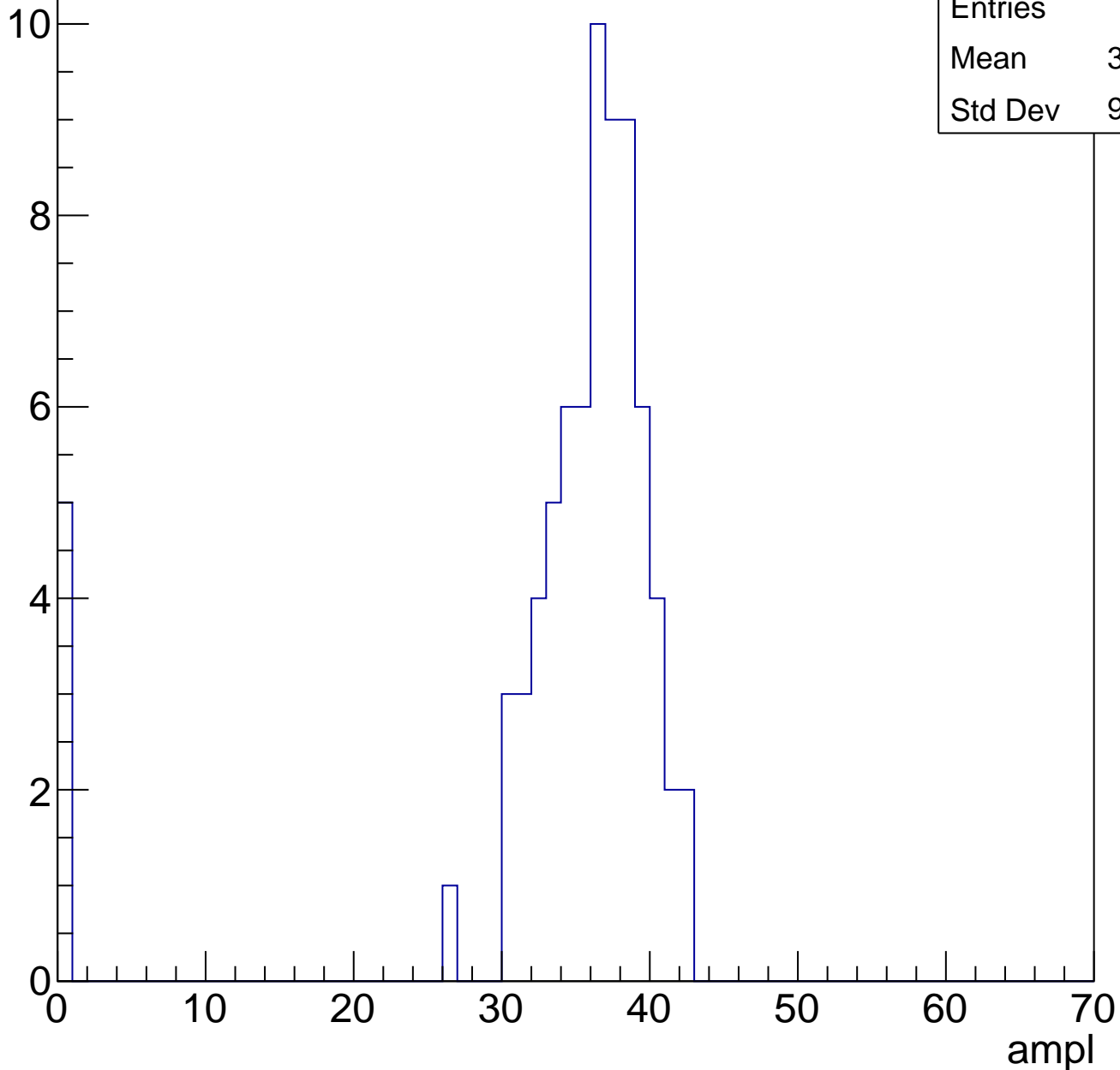


B1L103S, U9-ch75, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	33.48
Std Dev	9.459

Entry

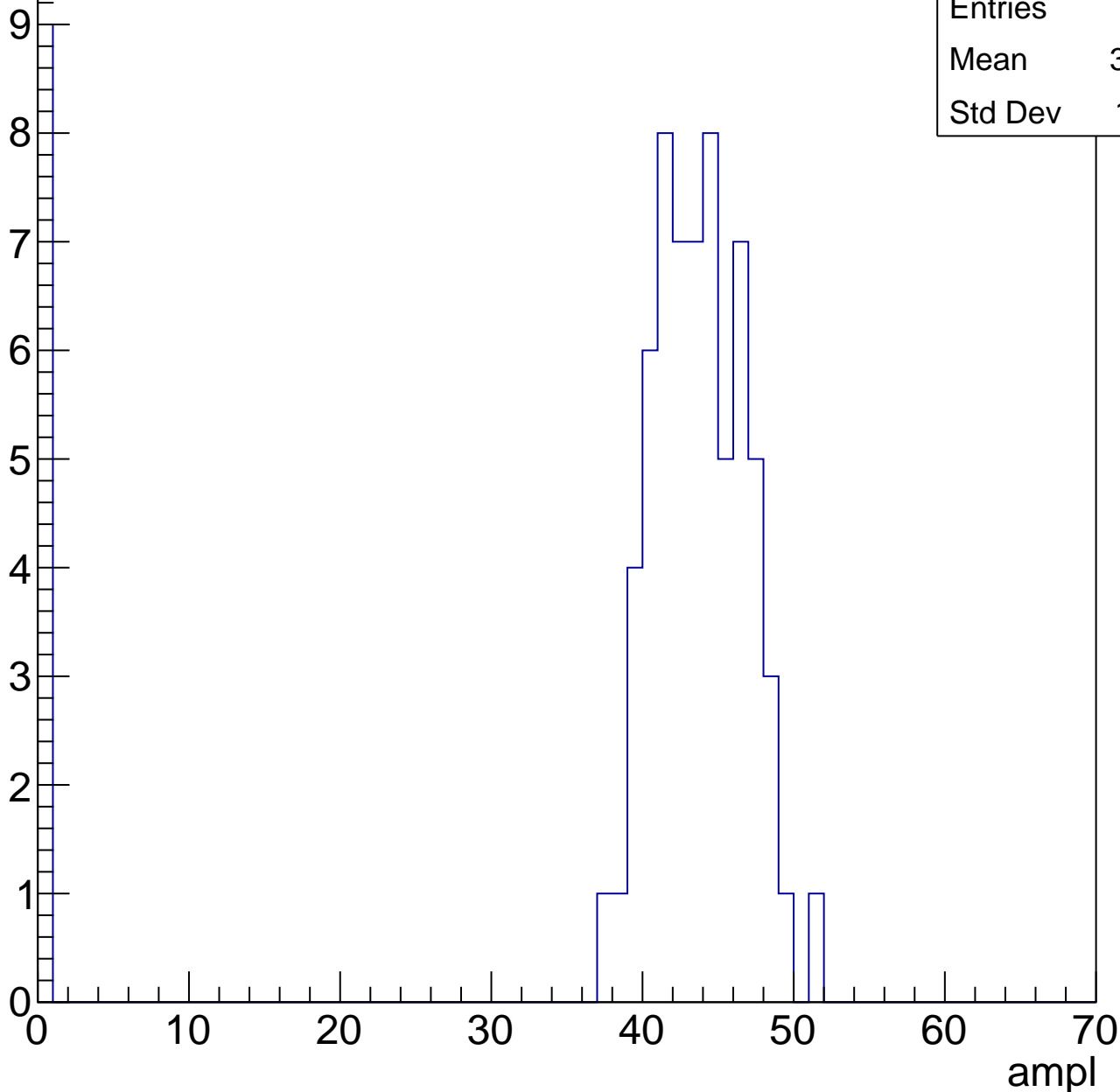


B1L103S, U9-ch75, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	37.97
Std Dev	14.51

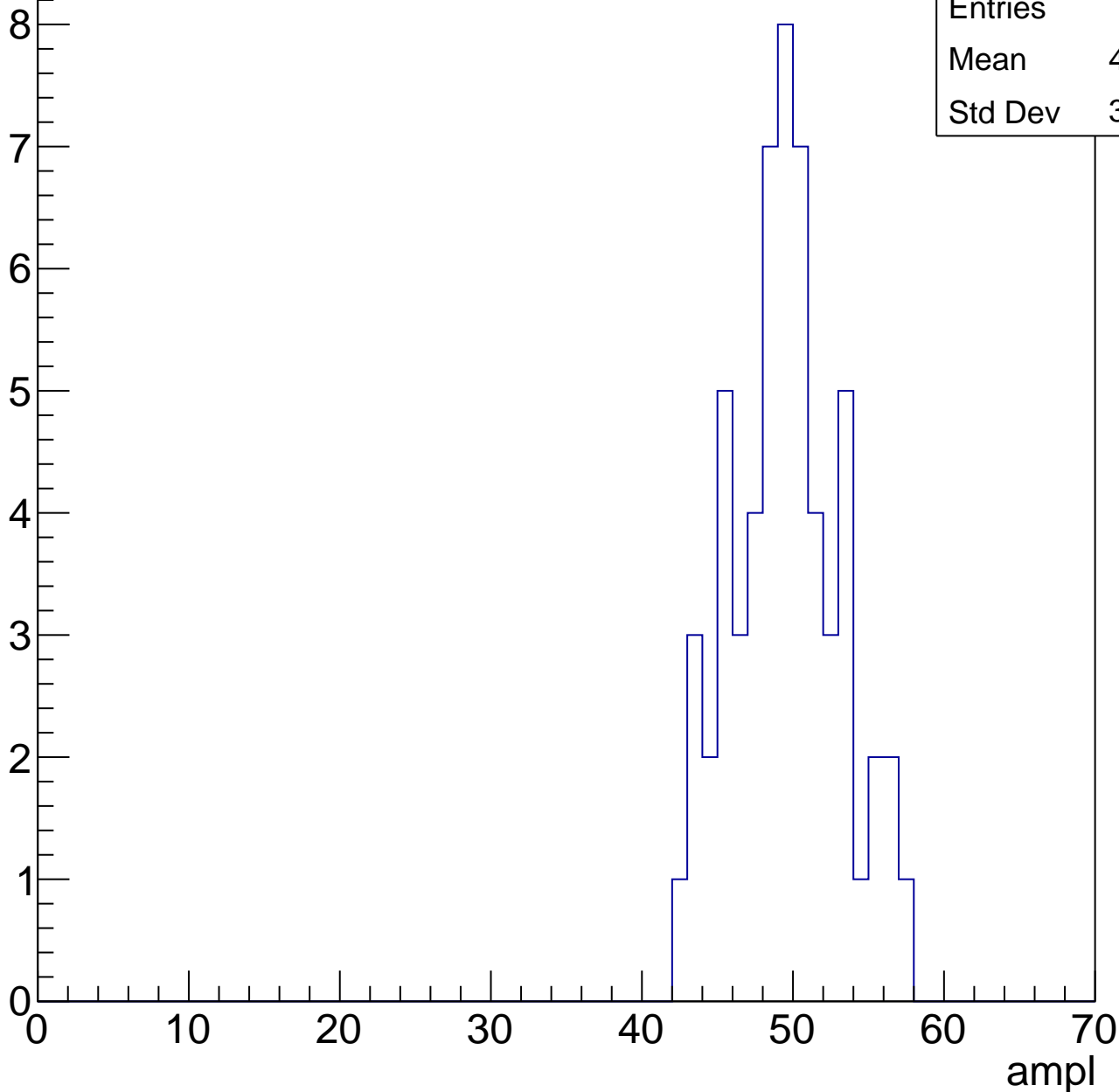


B1L103S, U9-ch75, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	49.07
Std Dev	3.537

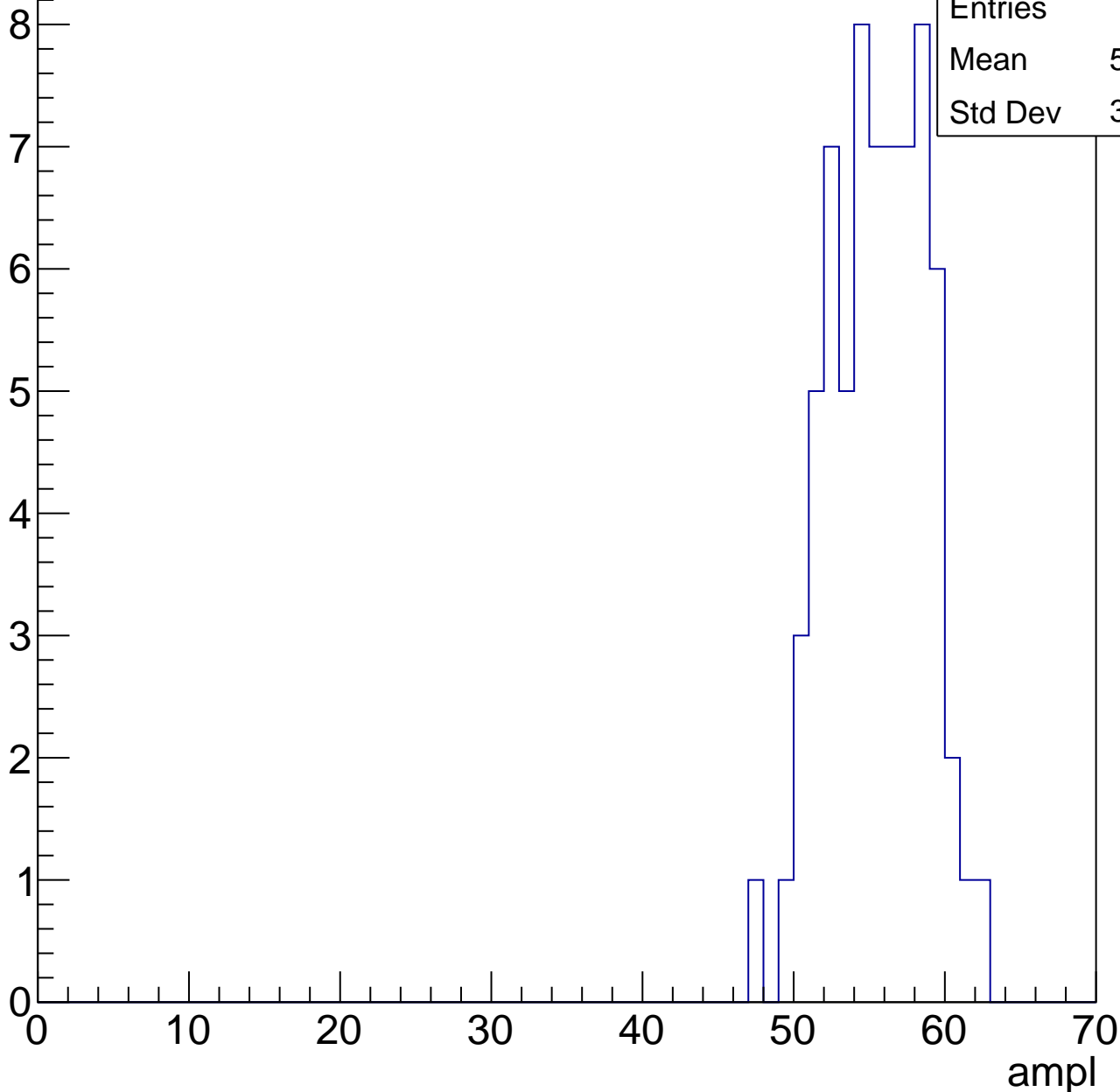


B1L103S, U9-ch75, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

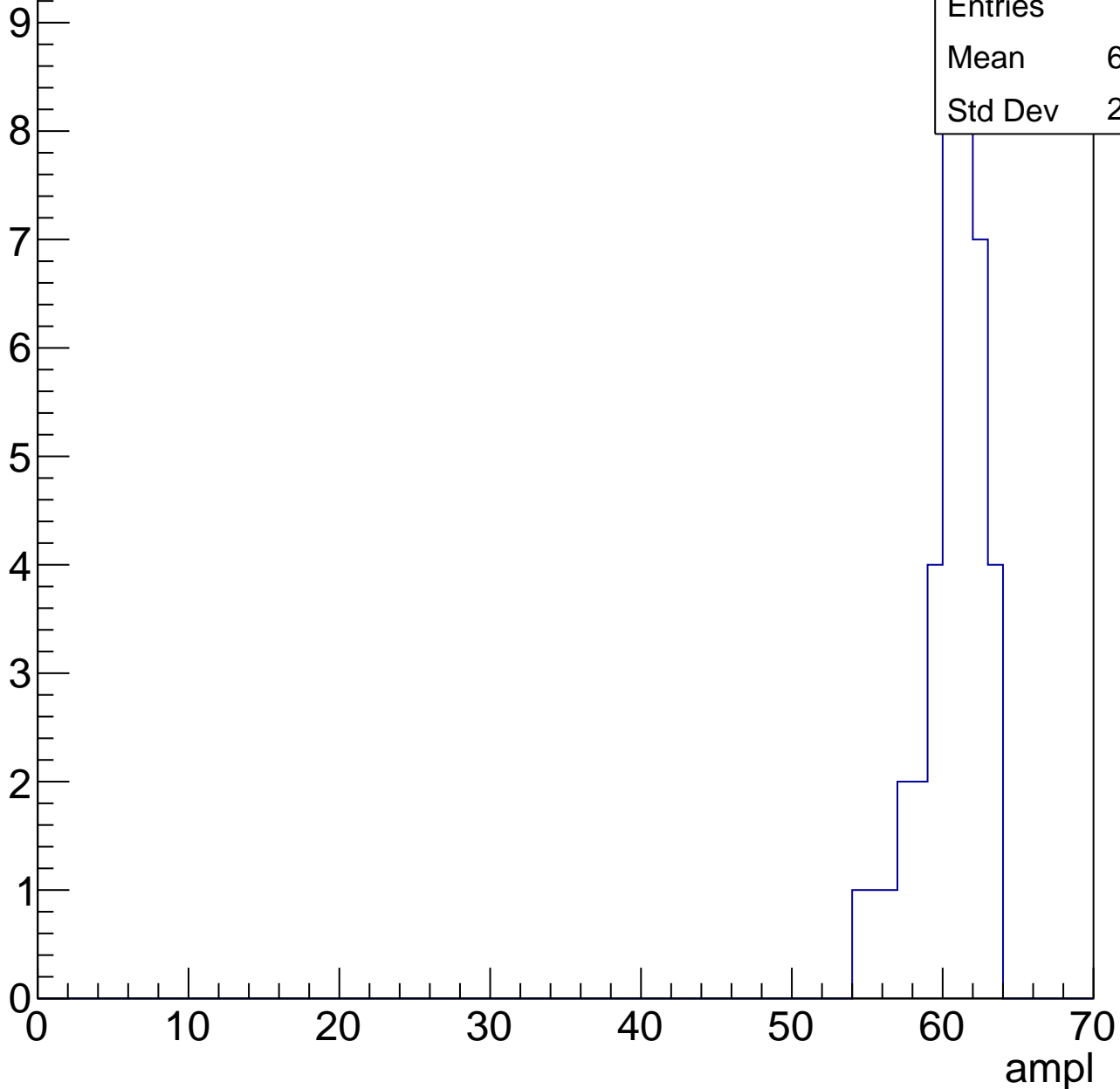
Entries	69
Mean	55.06
Std Dev	3.148



B1L103S, U9-ch75, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

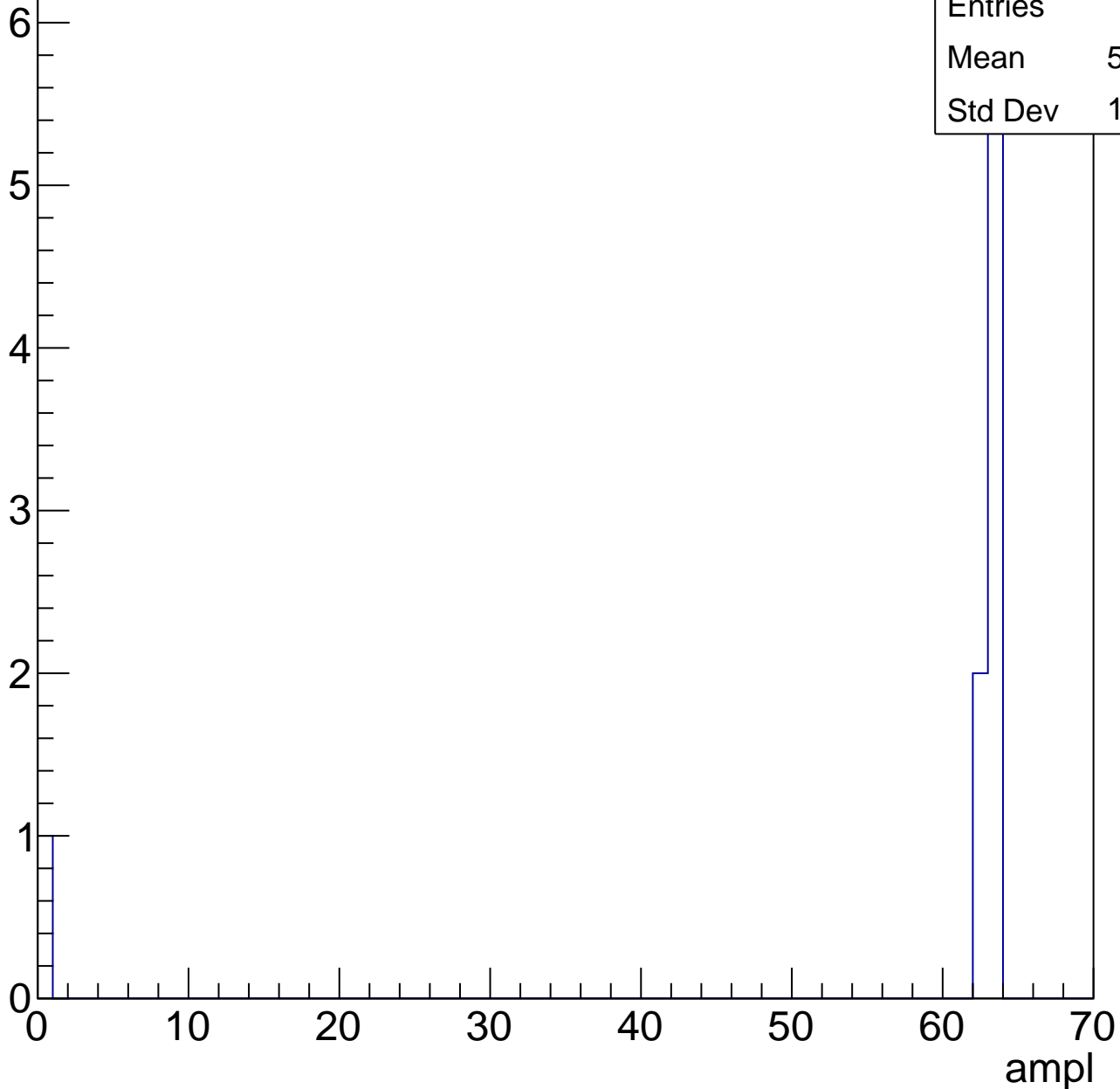


B1L103S, U9-ch75, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	9
Mean	55.78
Std Dev	19.72

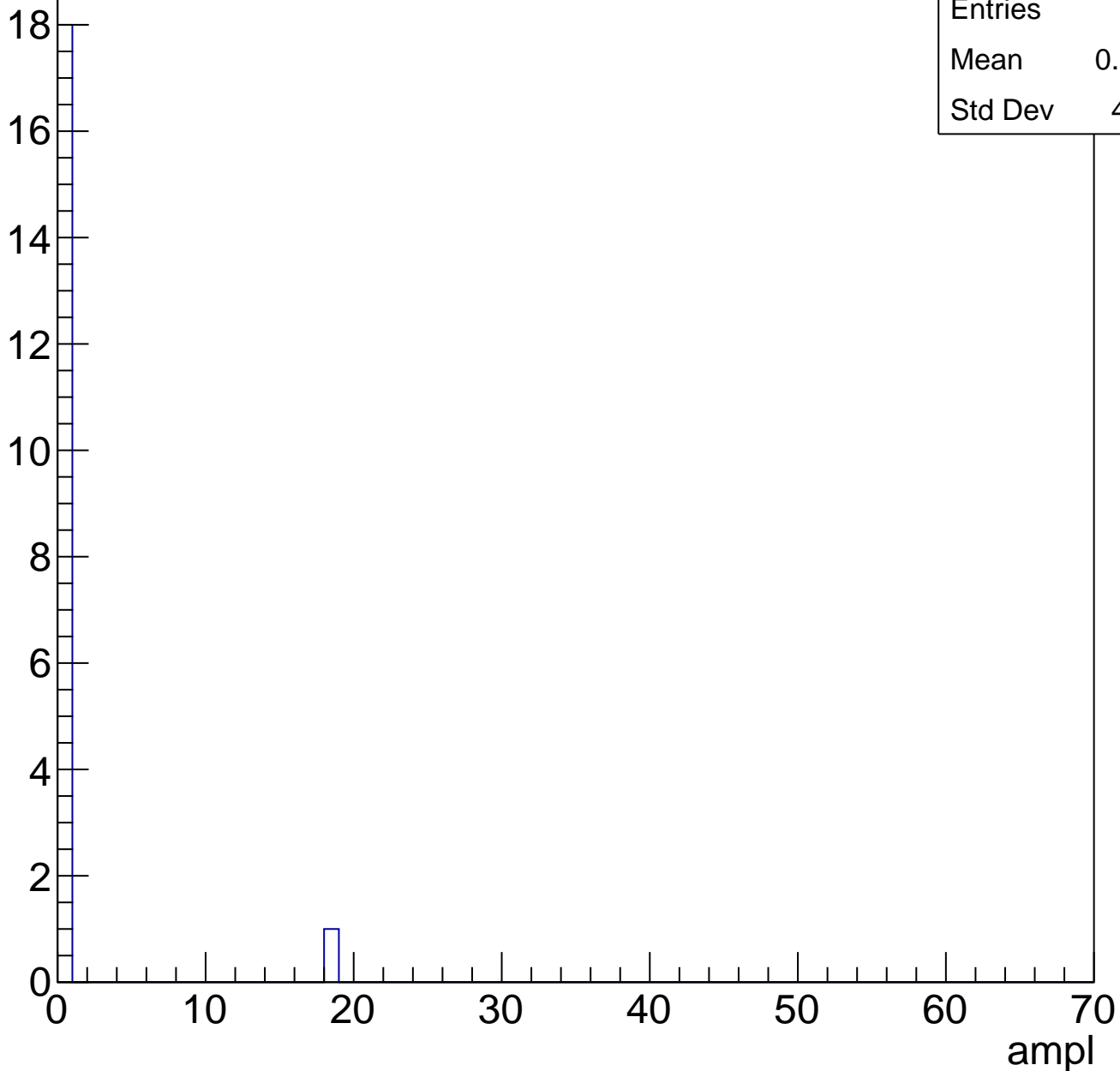


B1L103S, U9-ch75, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	0.9474
Std Dev	4.019

Entry

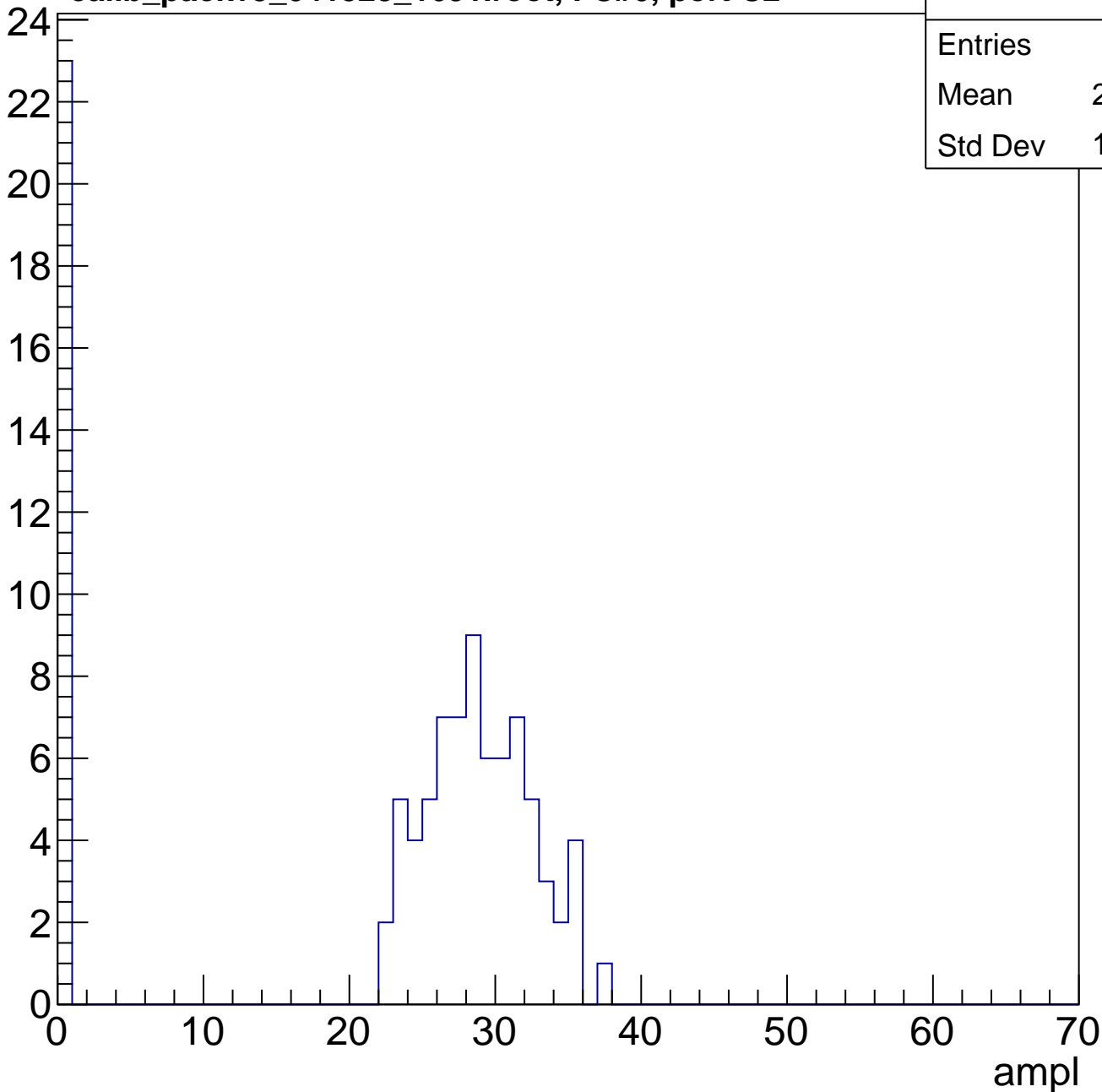


B1L103S, U9-ch76, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	96
Mean	21.65
Std Dev	12.54

Entry

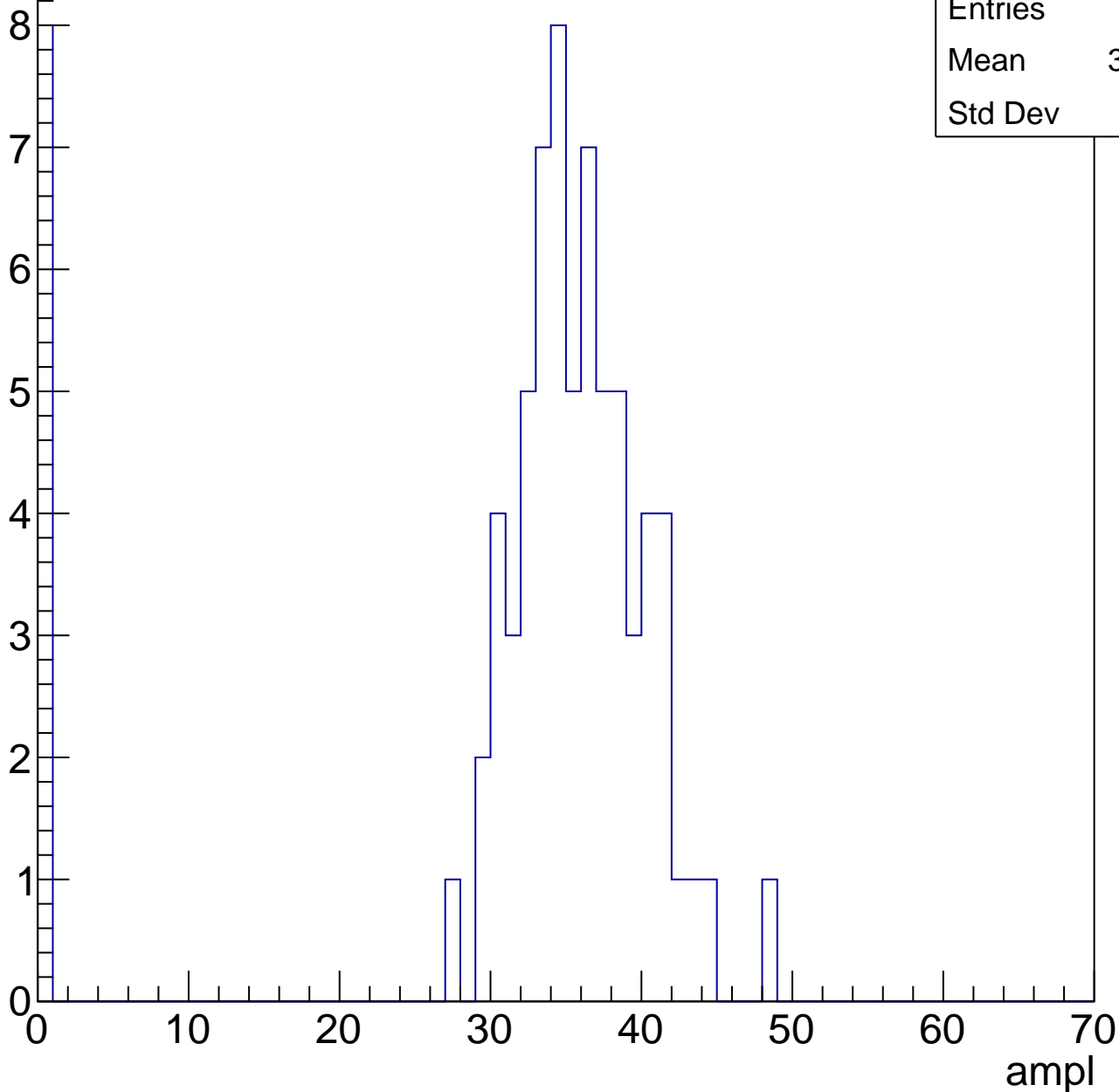


B1L103S, U9-ch76, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	31.75
Std Dev	11.6

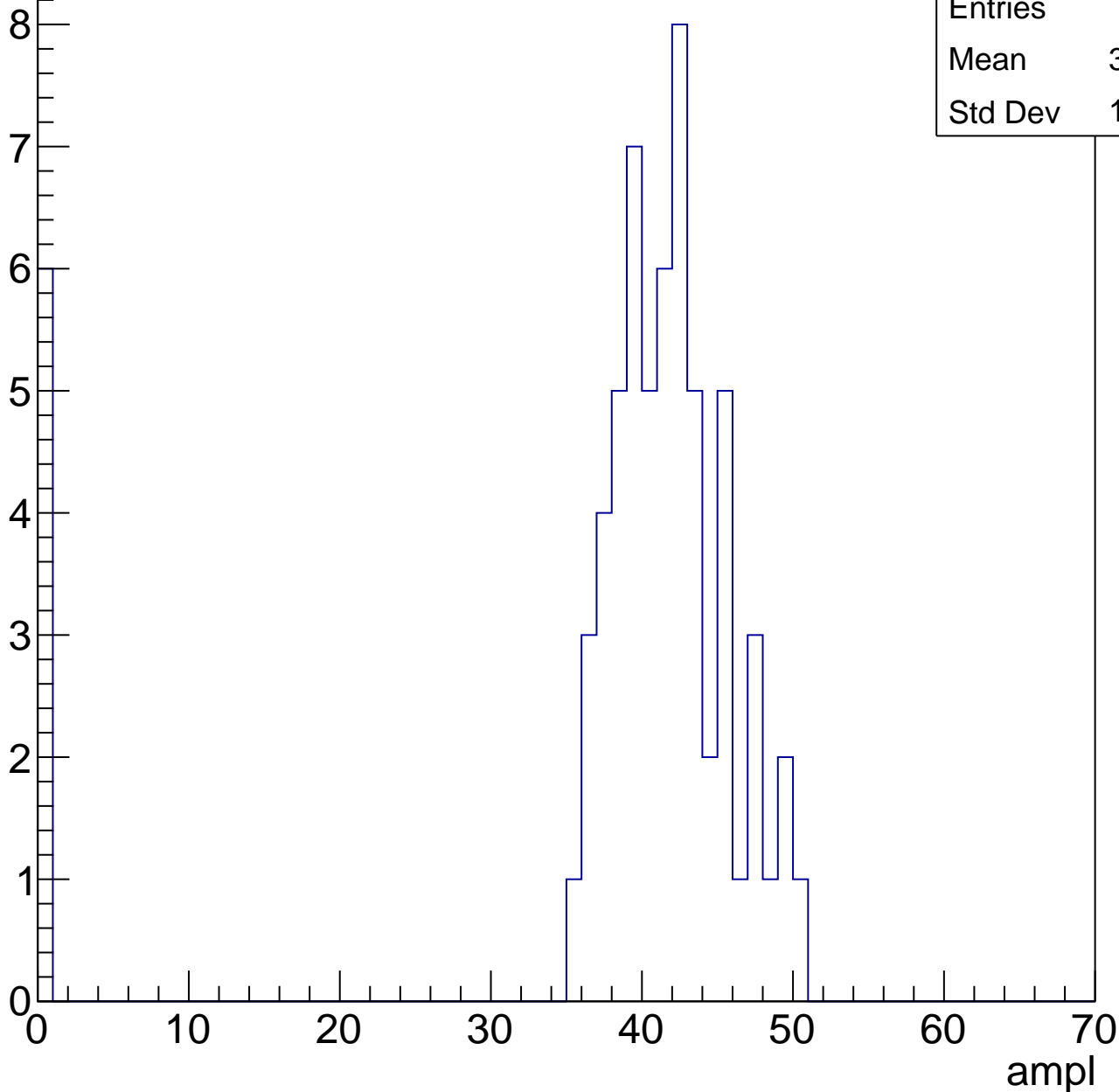


B1L103S, U9-ch76, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	37.65
Std Dev	12.48

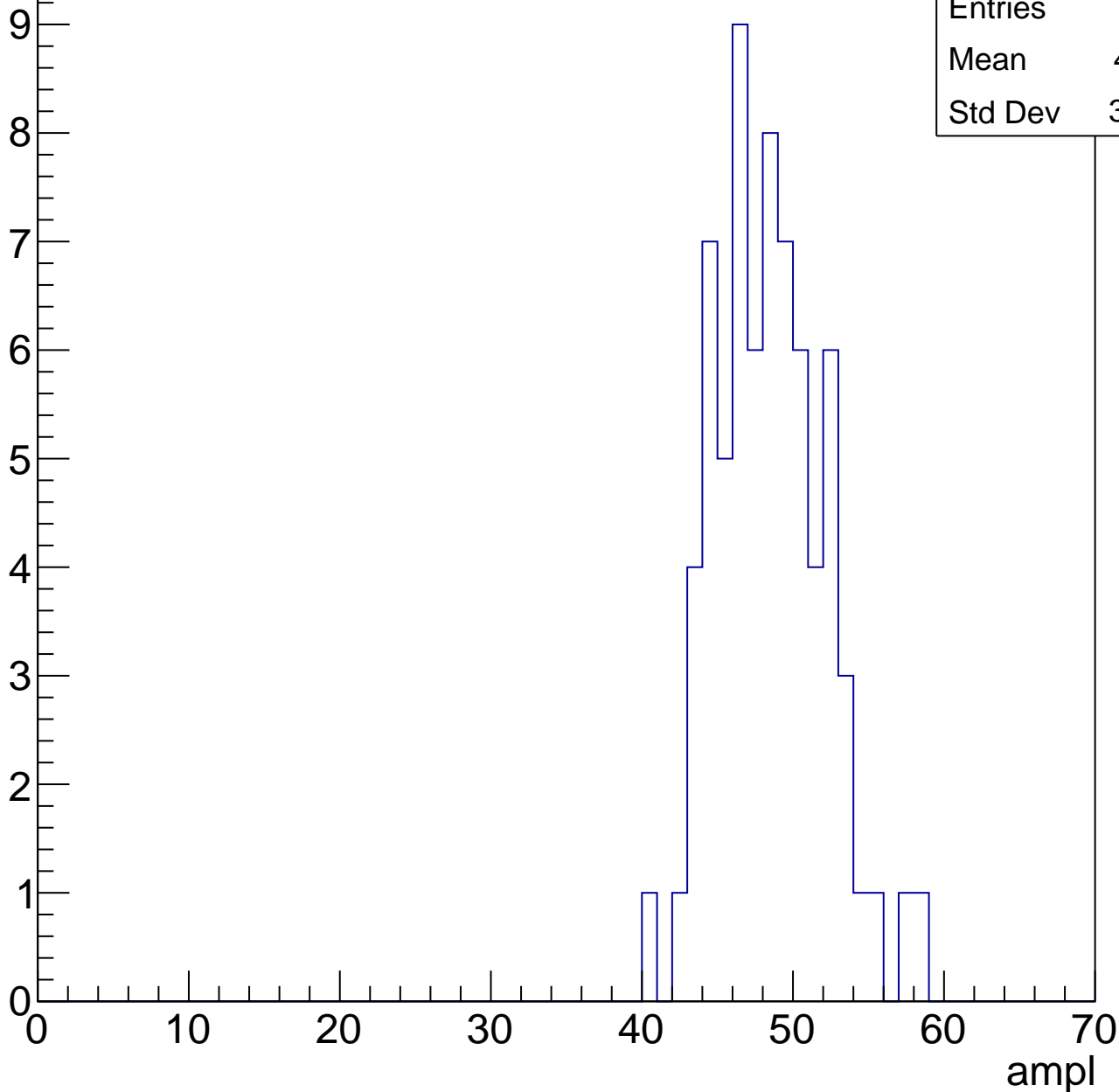


B1L103S, U9-ch76, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	48.01
Std Dev	3.566

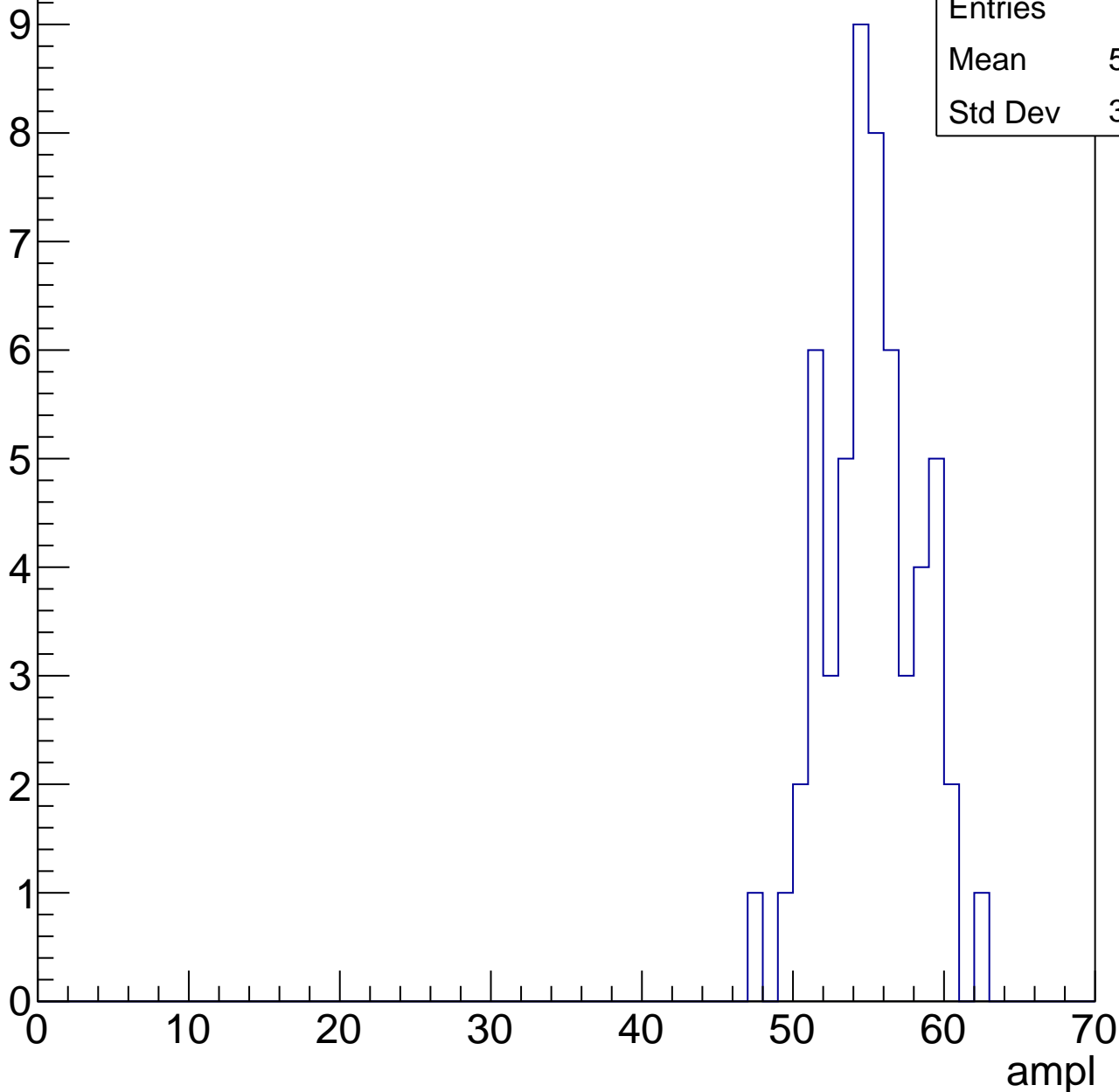


B1L103S, U9-ch76, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	54.73
Std Dev	3.079

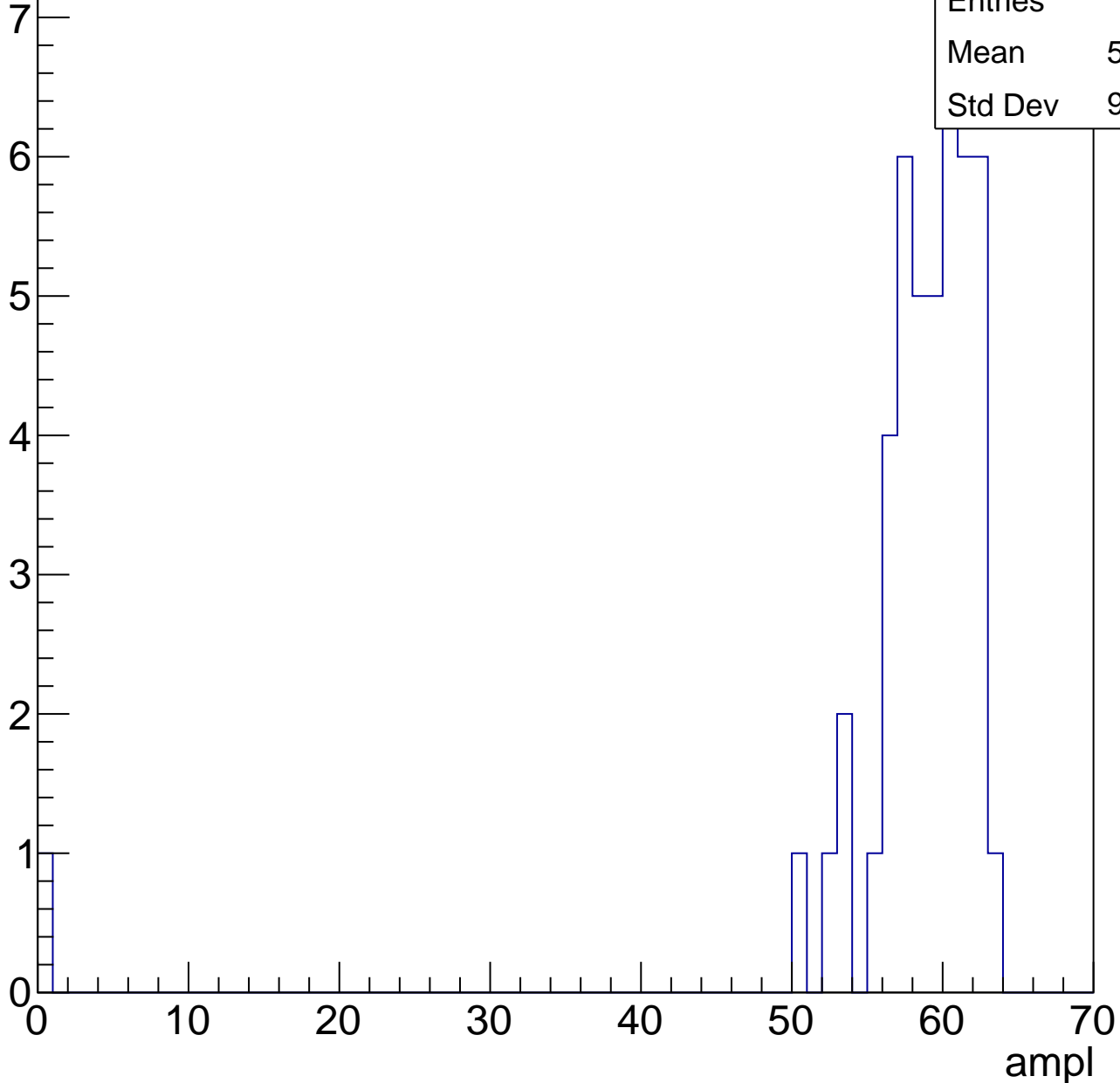


B1L103S, U9-ch76, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	46
Mean	57.28
Std Dev	9.004

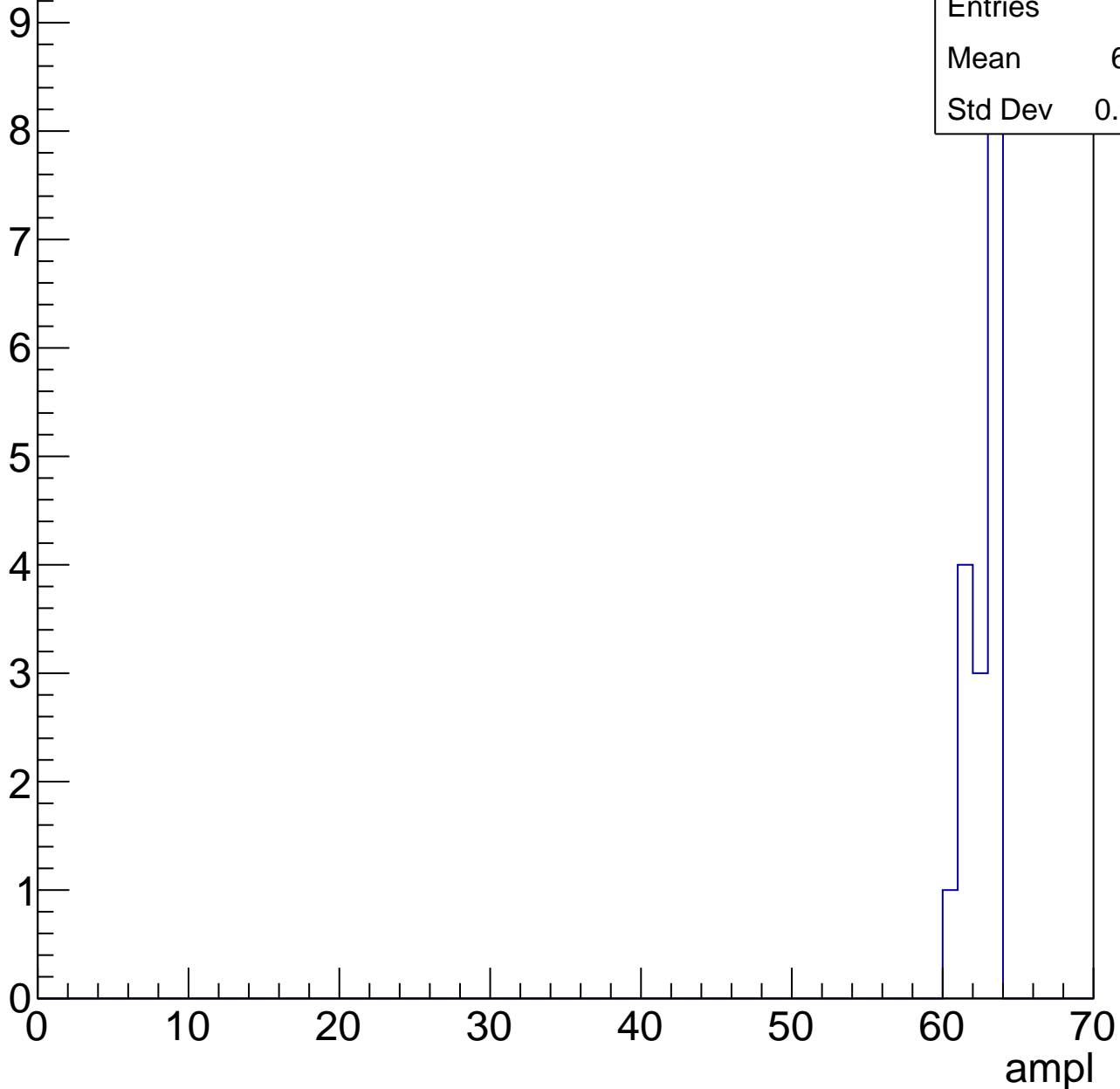


B1L103S, U9-ch76, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

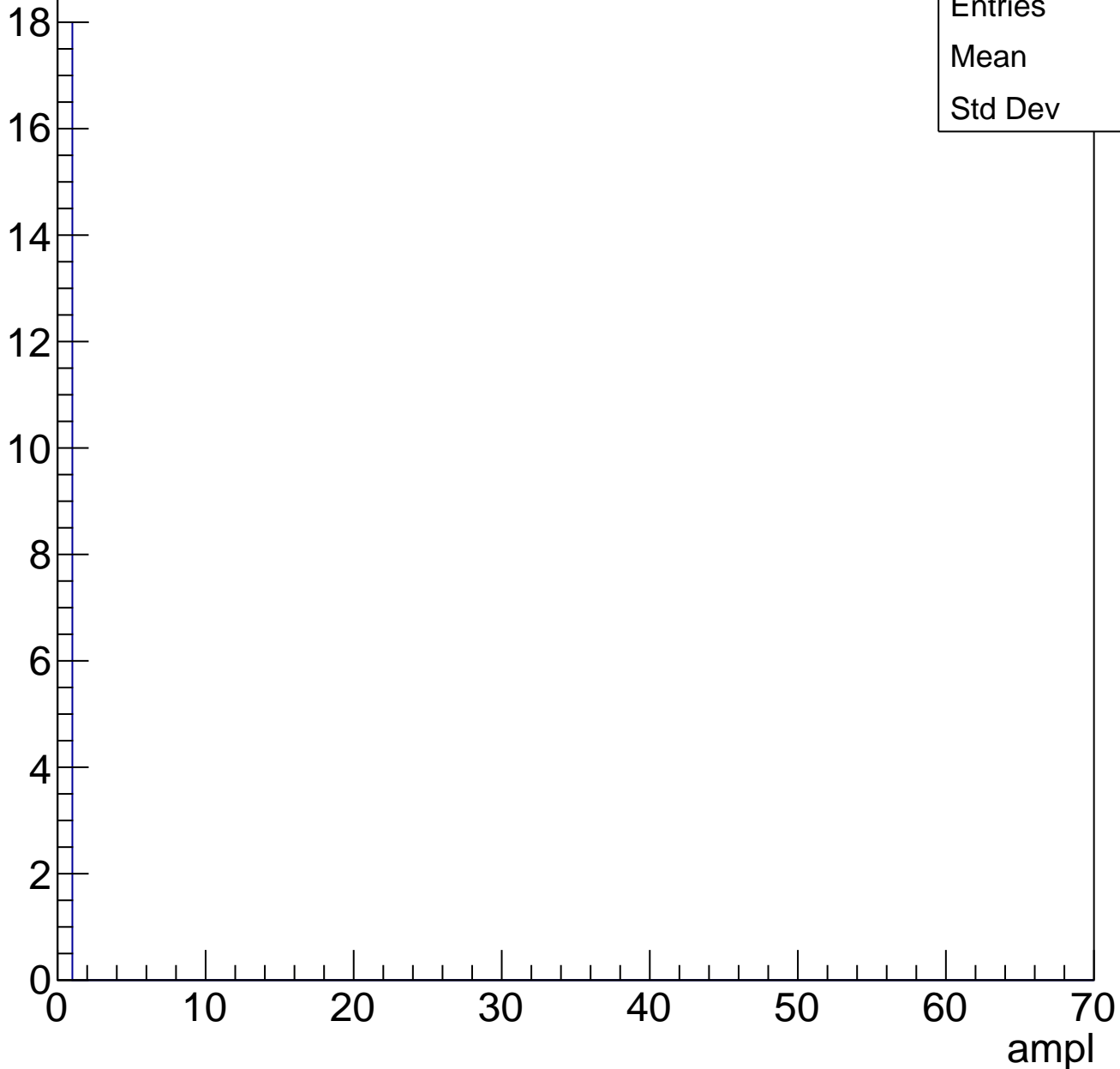
Entries	17
Mean	62.18
Std Dev	0.9843



B1L103S, U9-ch76, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

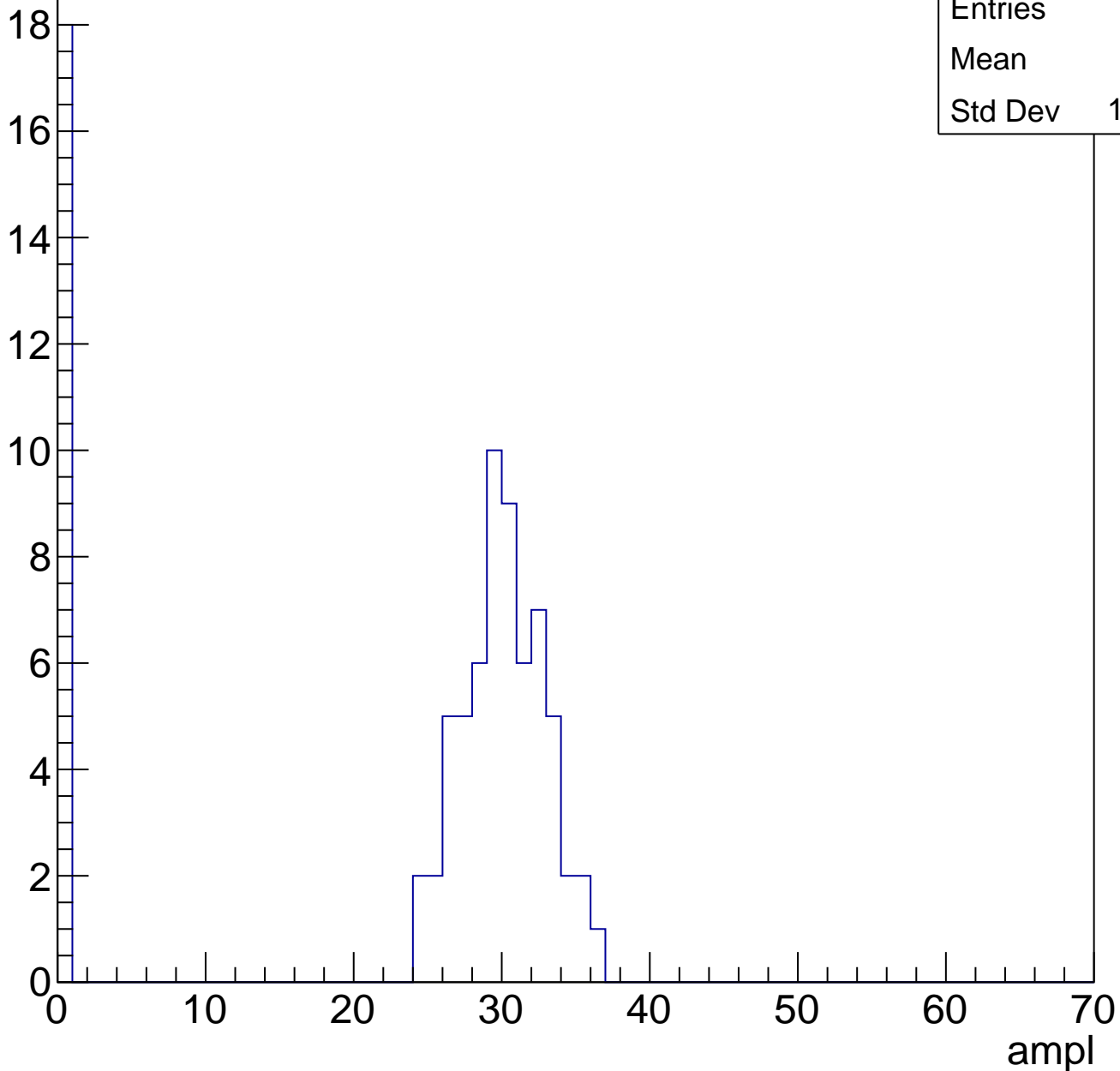


B1L103S, U9-ch77, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	23
Std Dev	12.63

Entry

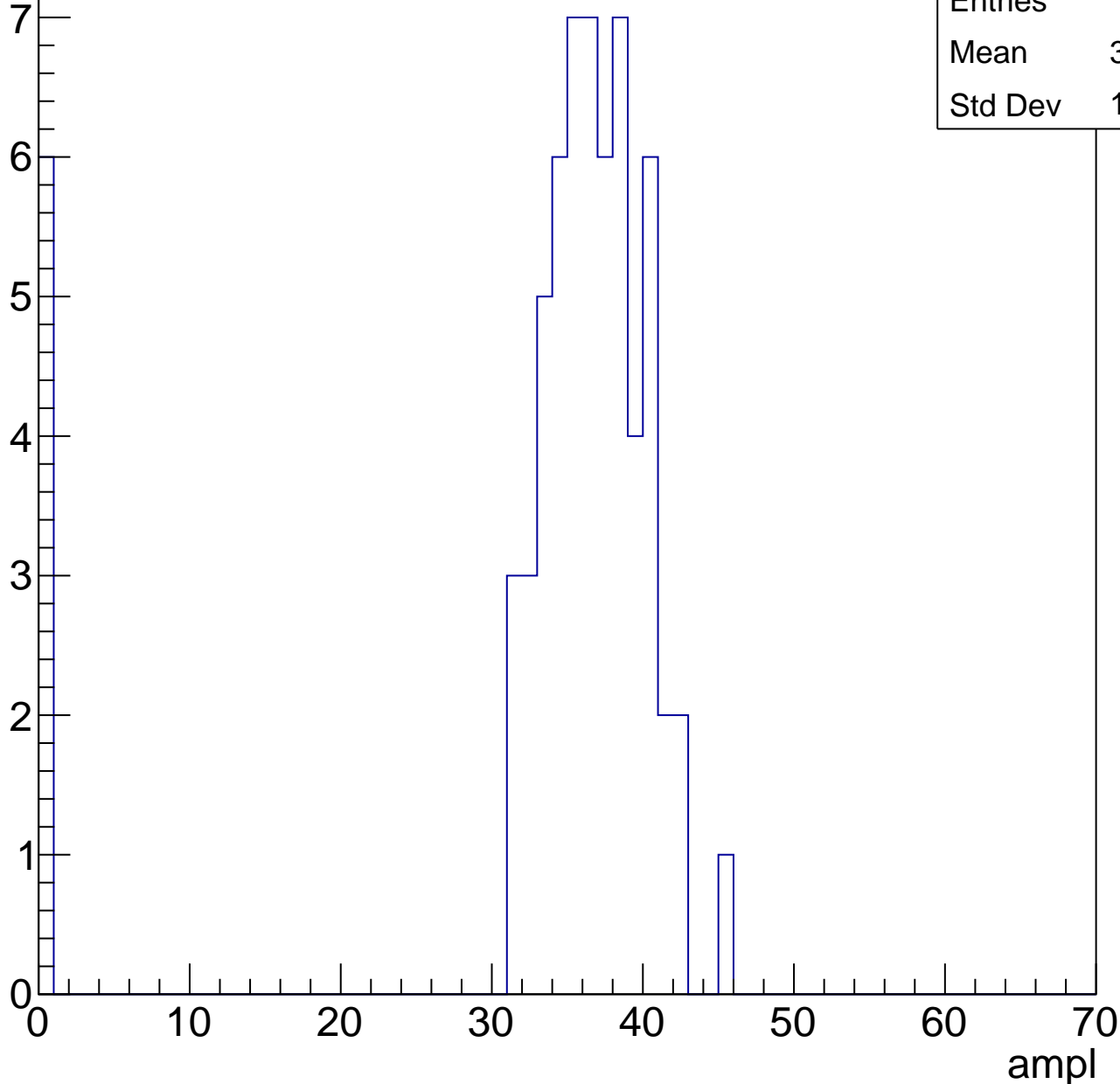


B1L103S, U9-ch77, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	33.08
Std Dev	10.95



B1L103S, U9-ch77, adc2

calib_packv5_041523_1651.root, FC#0, port C2

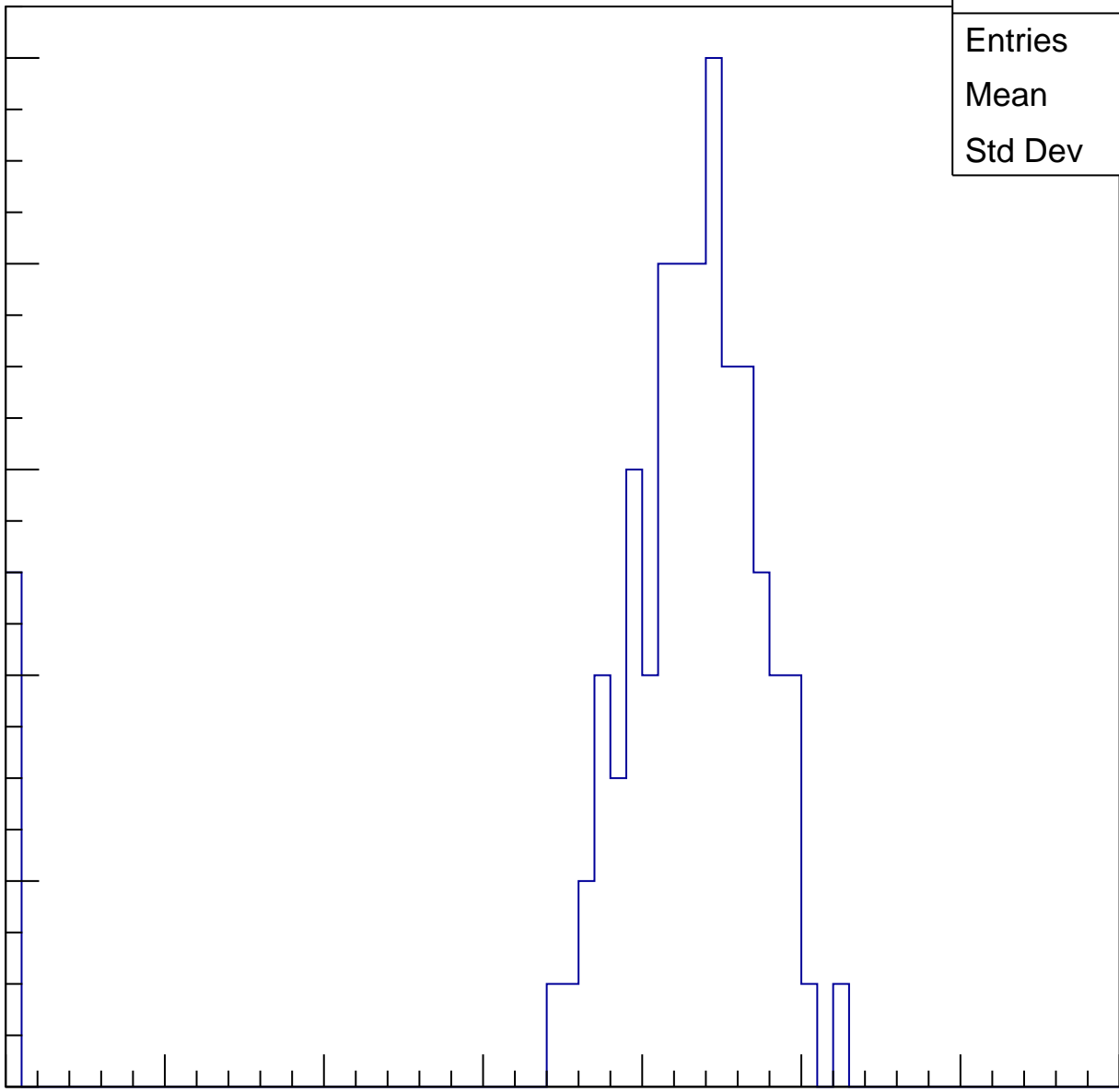
Entries	89
Mean	40.53
Std Dev	10.54

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

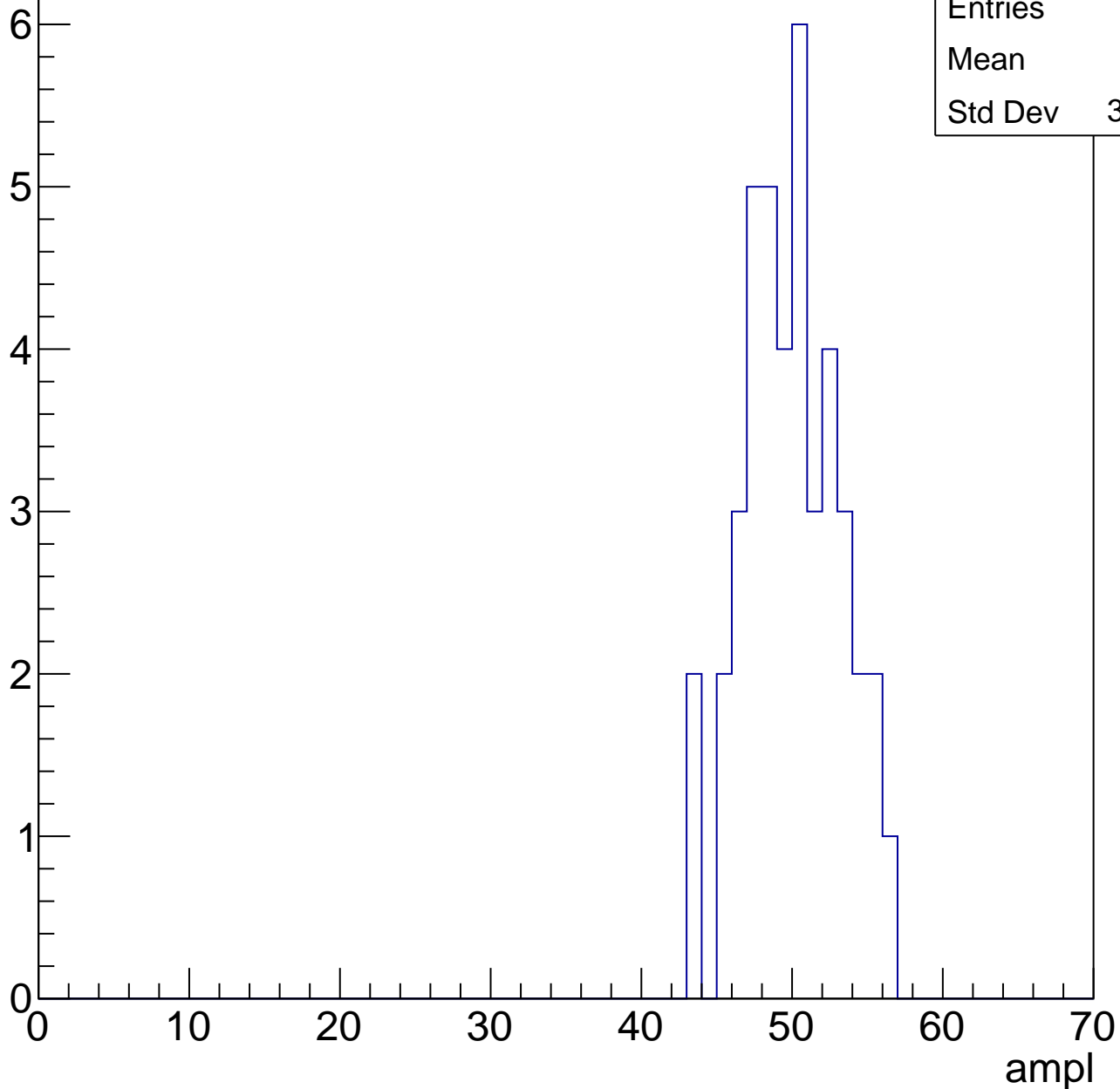


B1L103S, U9-ch77, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	42
Mean	49.5
Std Dev	3.157

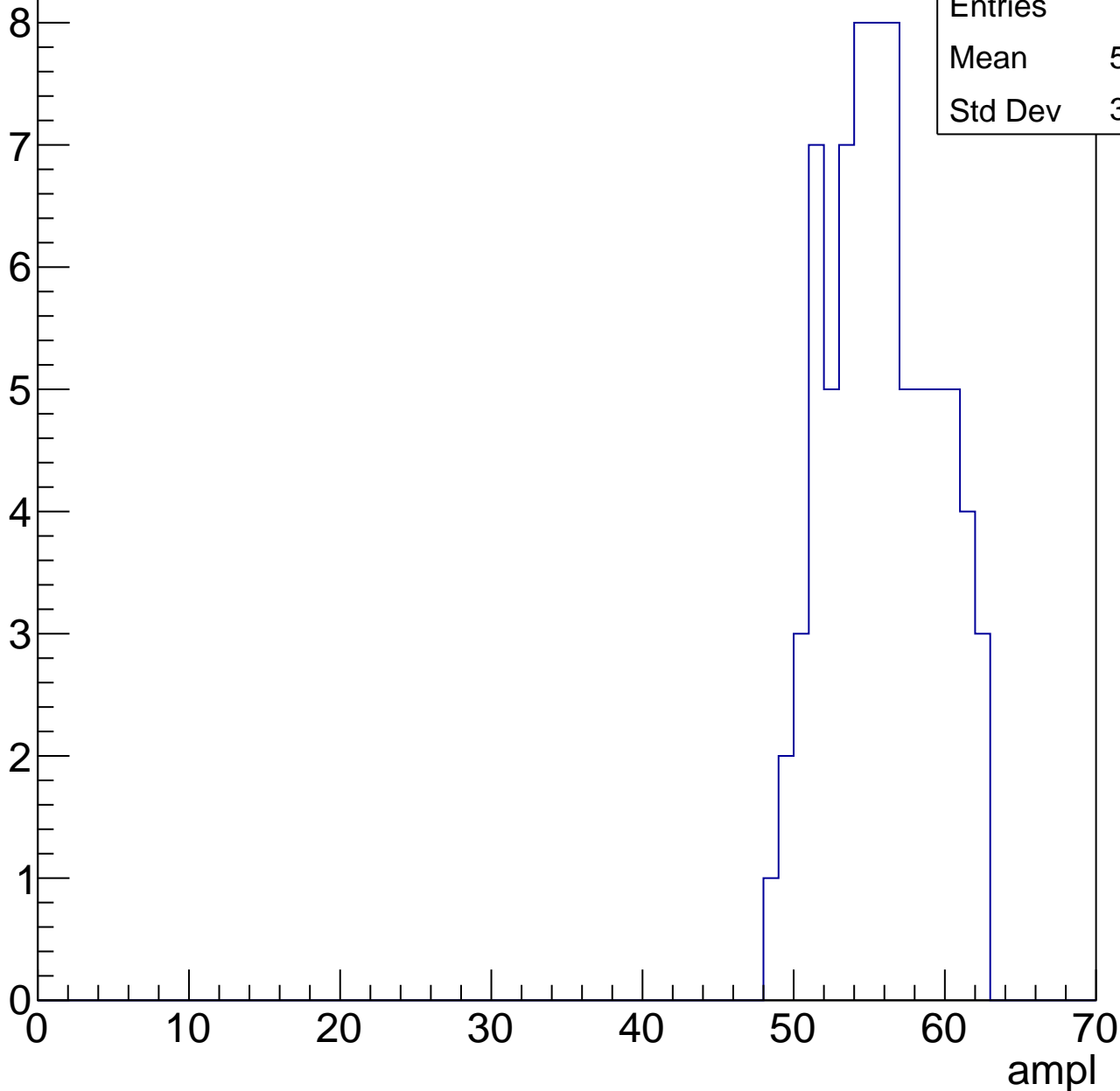


B1L103S, U9-ch77, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	55.32
Std Dev	3.536

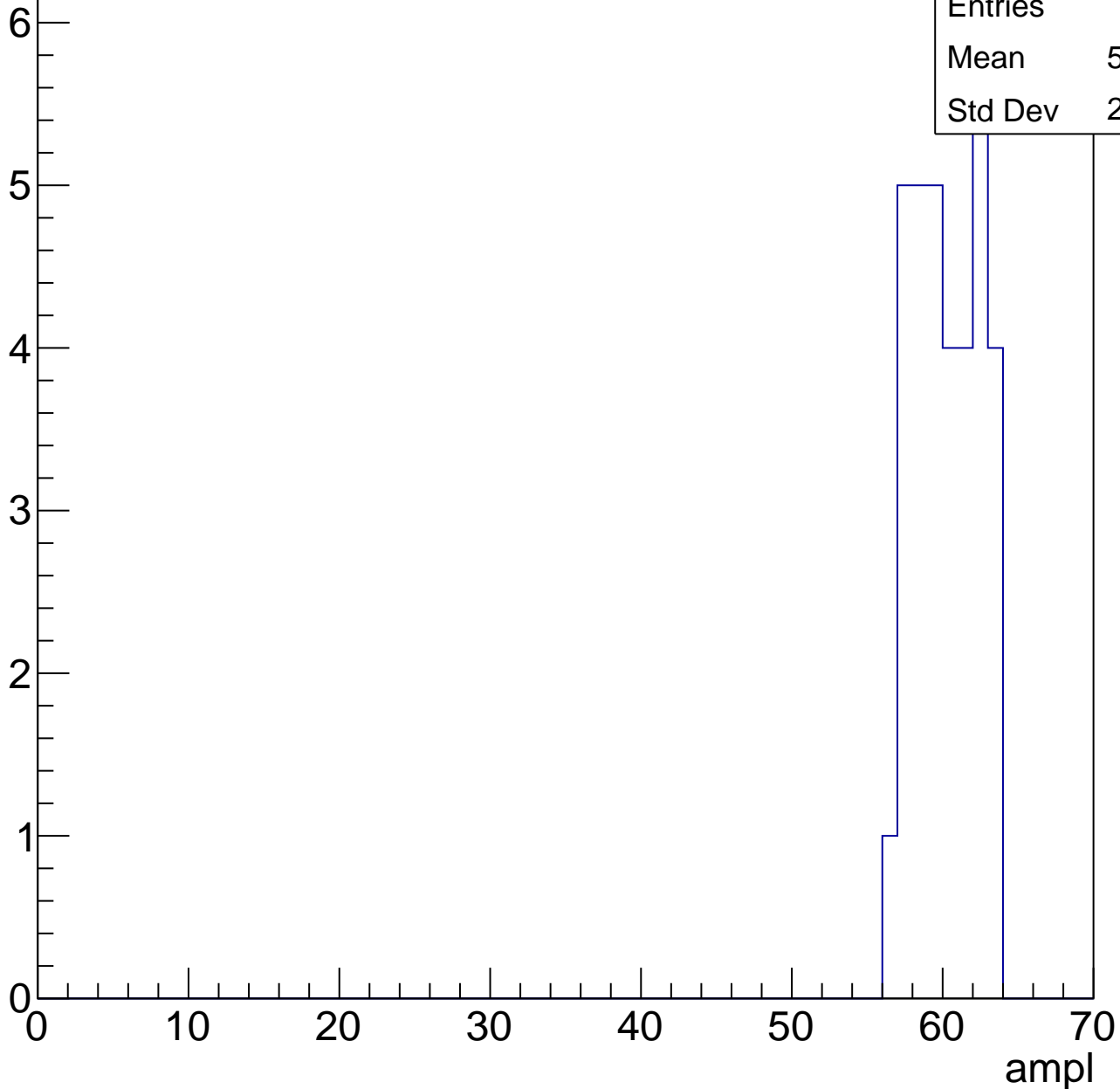


B1L103S, U9-ch77, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	34
Mean	59.82
Std Dev	2.093

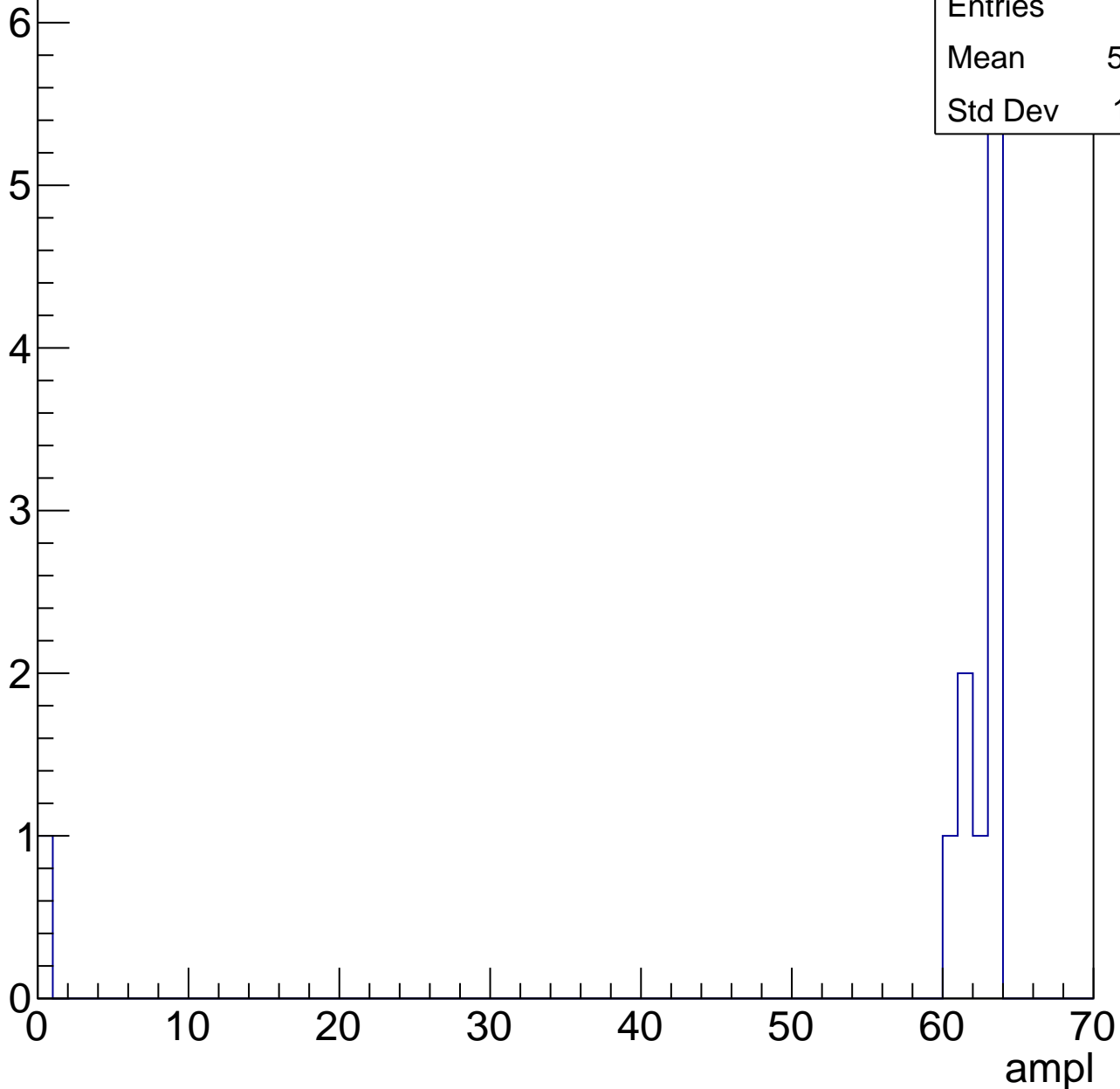


B1L103S, U9-ch77, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	11
Mean	56.55
Std Dev	17.91



B1L103S, U9-ch77, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

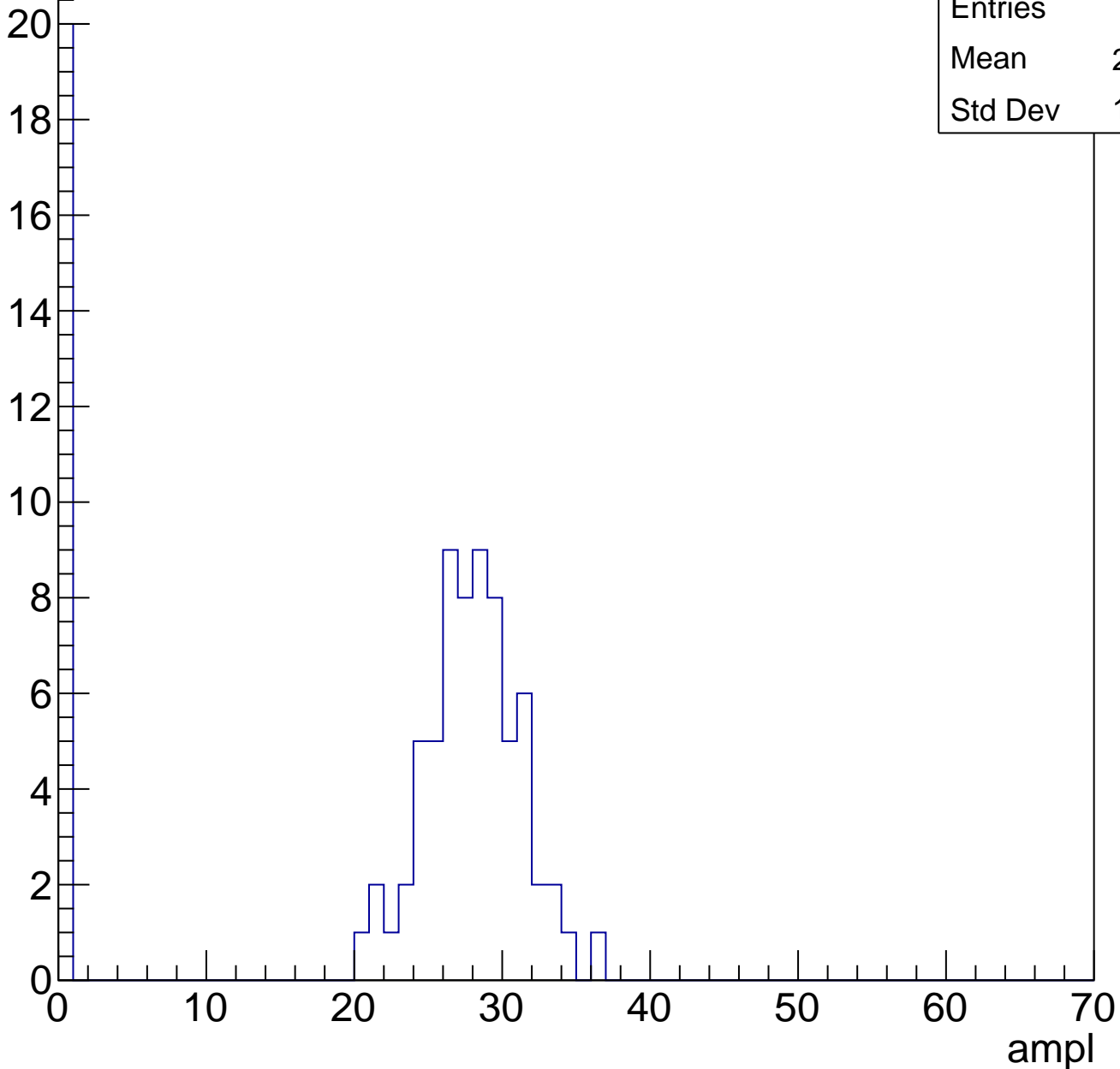
ampl

B1L103S, U9-ch78, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	87
Mean	21.21
Std Dev	11.91

Entry



B1L103S, U9-ch78, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	94
Mean	30.5
Std Dev	12.61

Entry

12

10

8

6

4

2

0

0

10

20

30

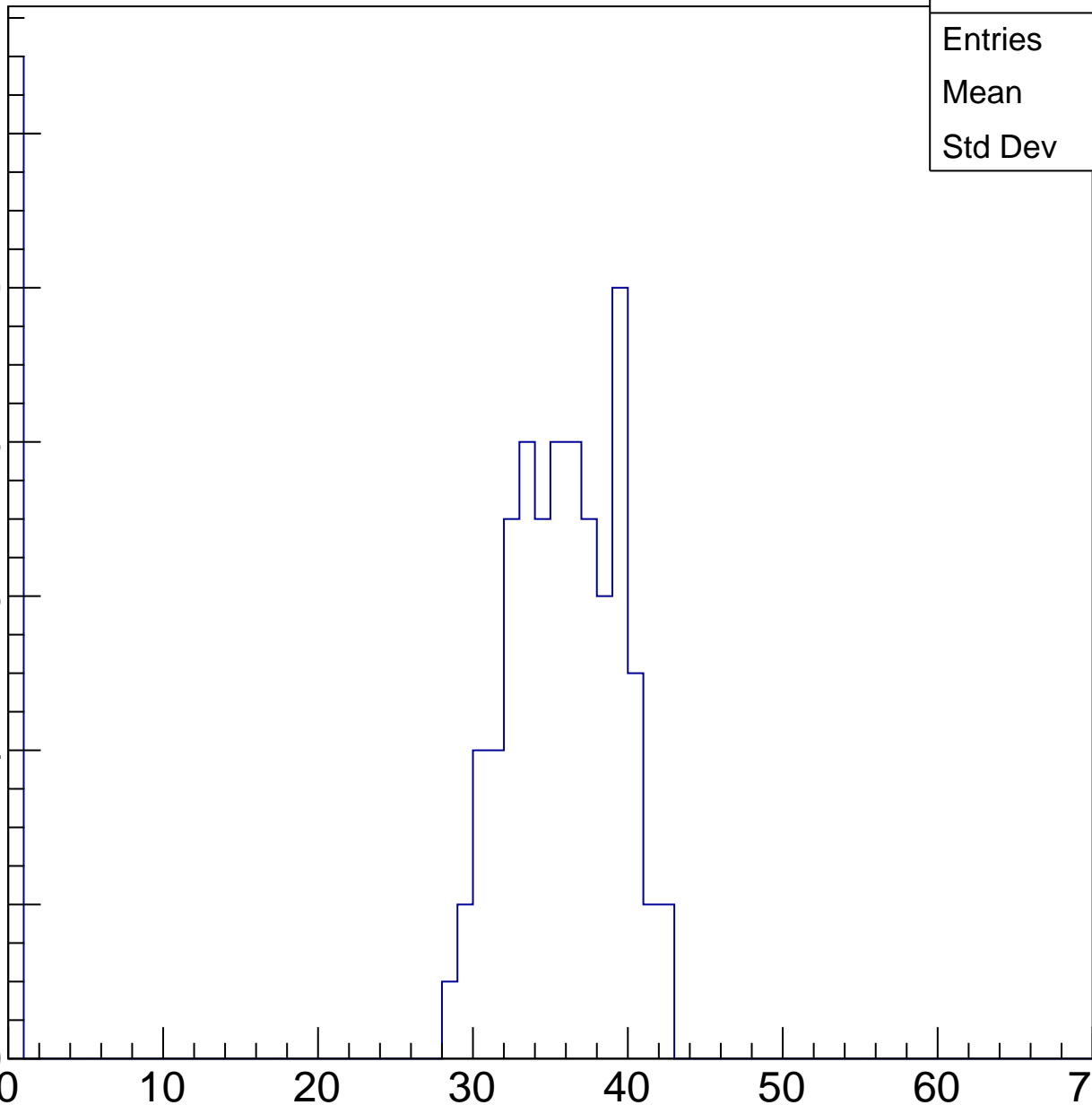
40

50

60

70

ampl

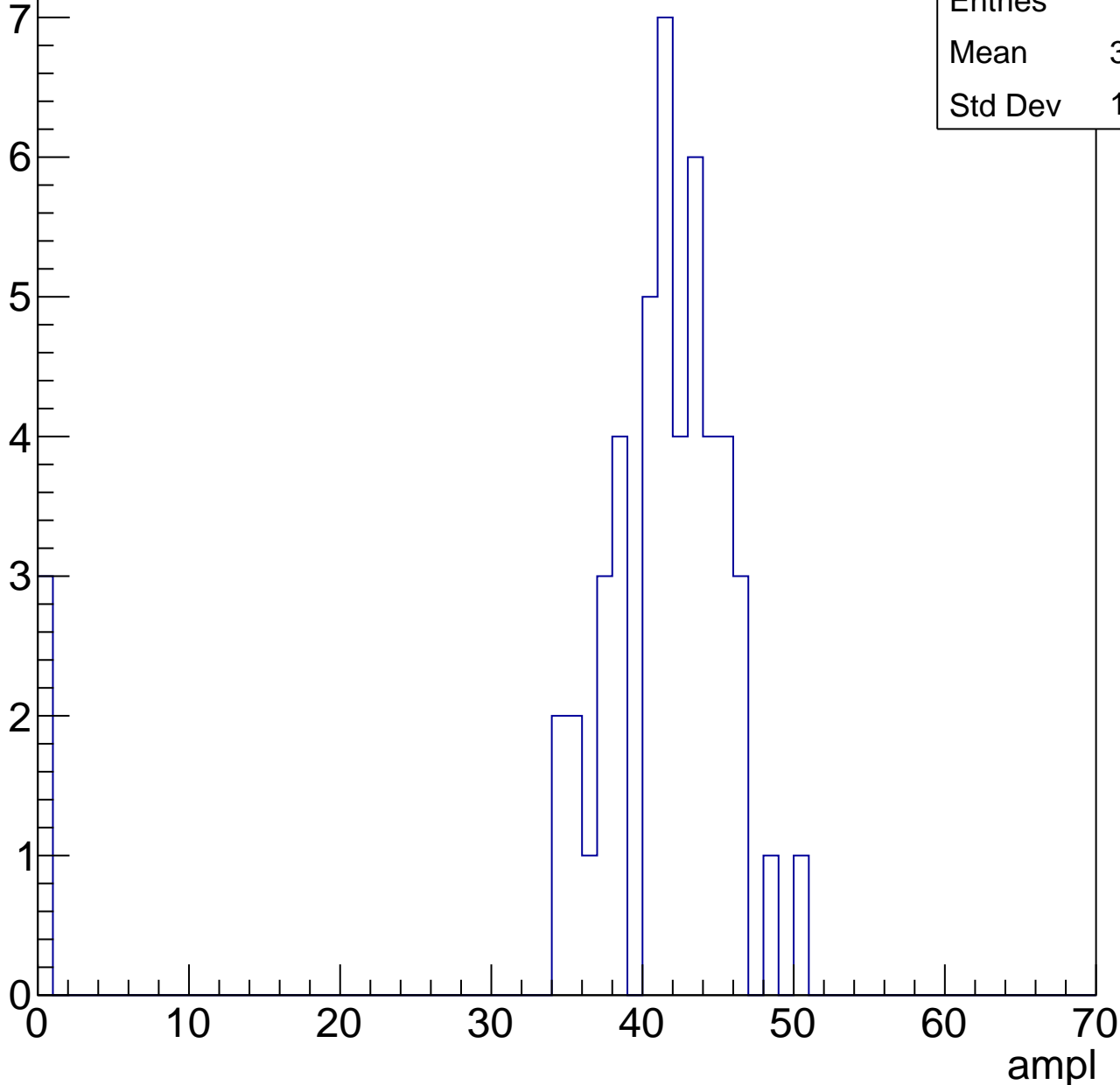


B1L103S, U9-ch78, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

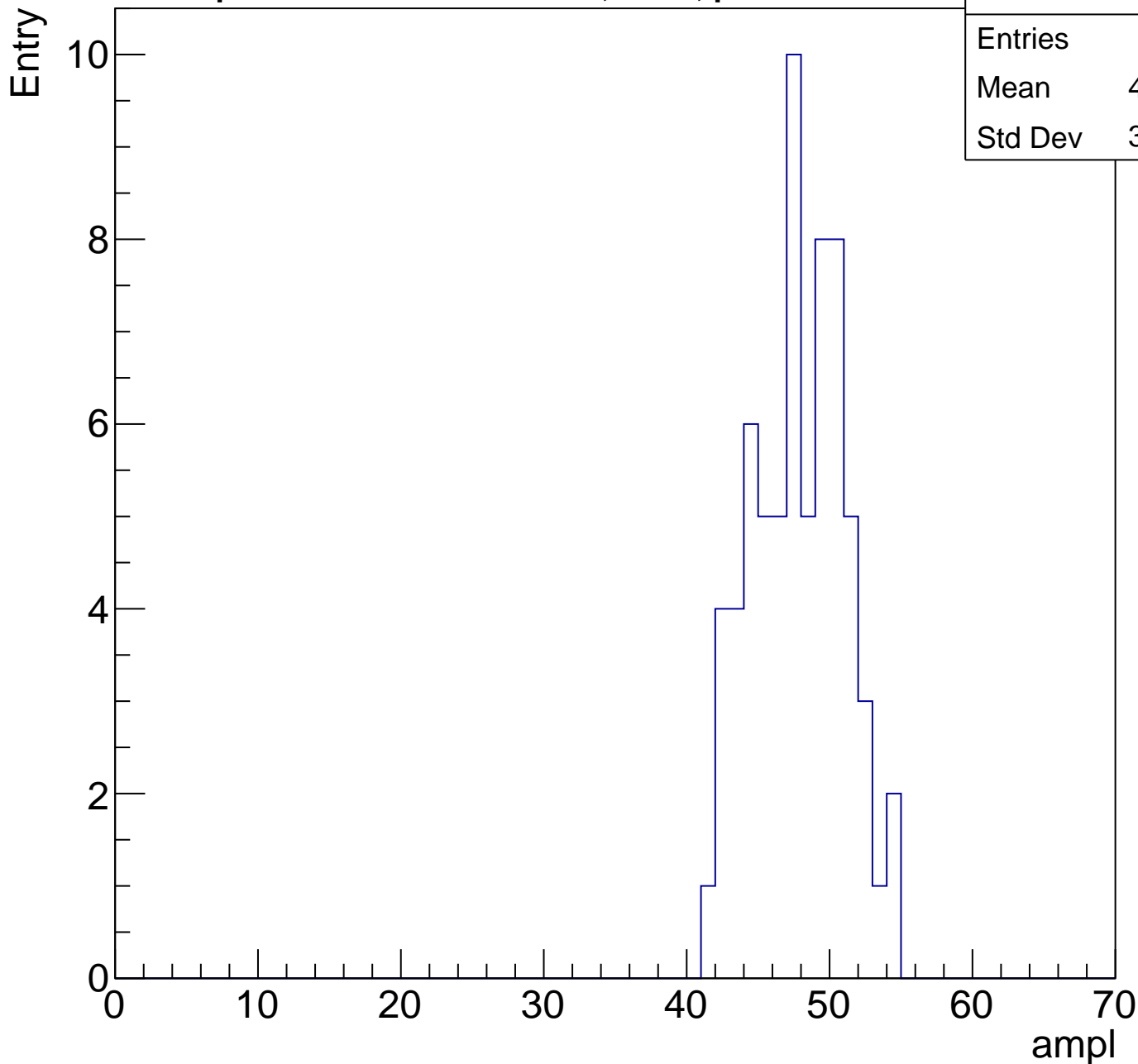
Entries	50
Mean	38.84
Std Dev	10.42



B1L103S, U9-ch78, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	67
Mean	47.37
Std Dev	3.157

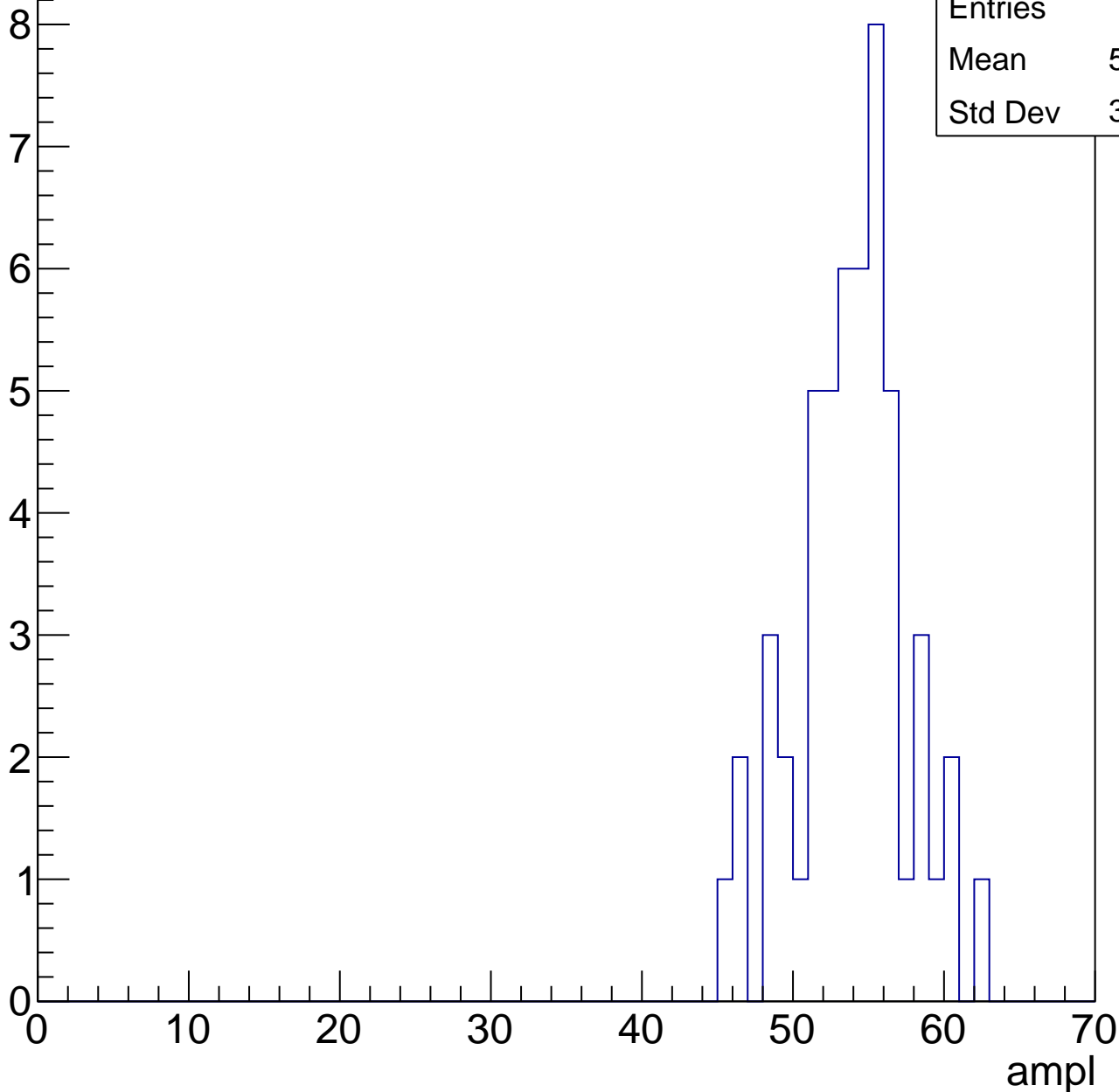


B1L103S, U9-ch78, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	53.42
Std Dev	3.623

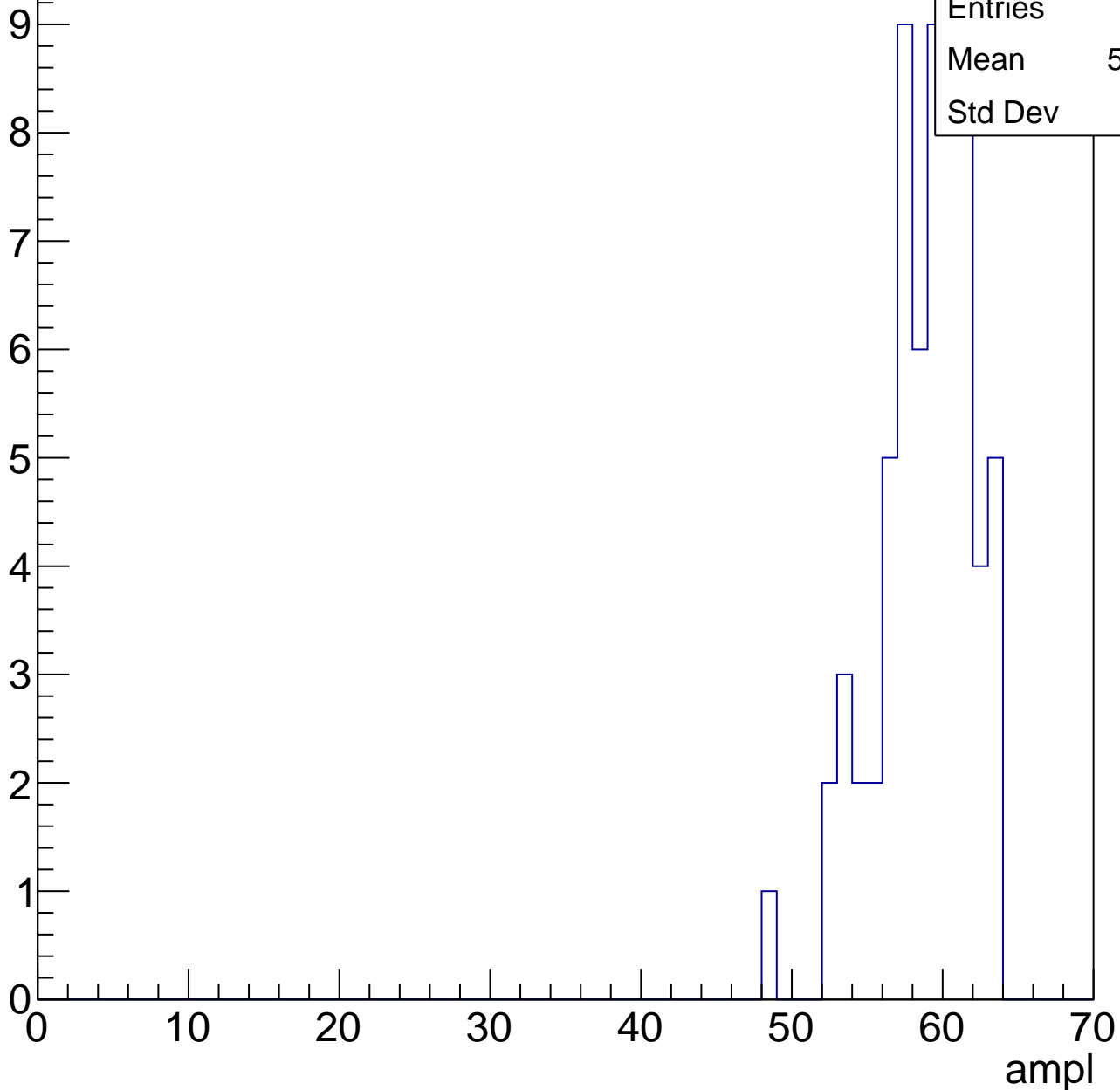


B1L103S, U9-ch78, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	58.35
Std Dev	3.11

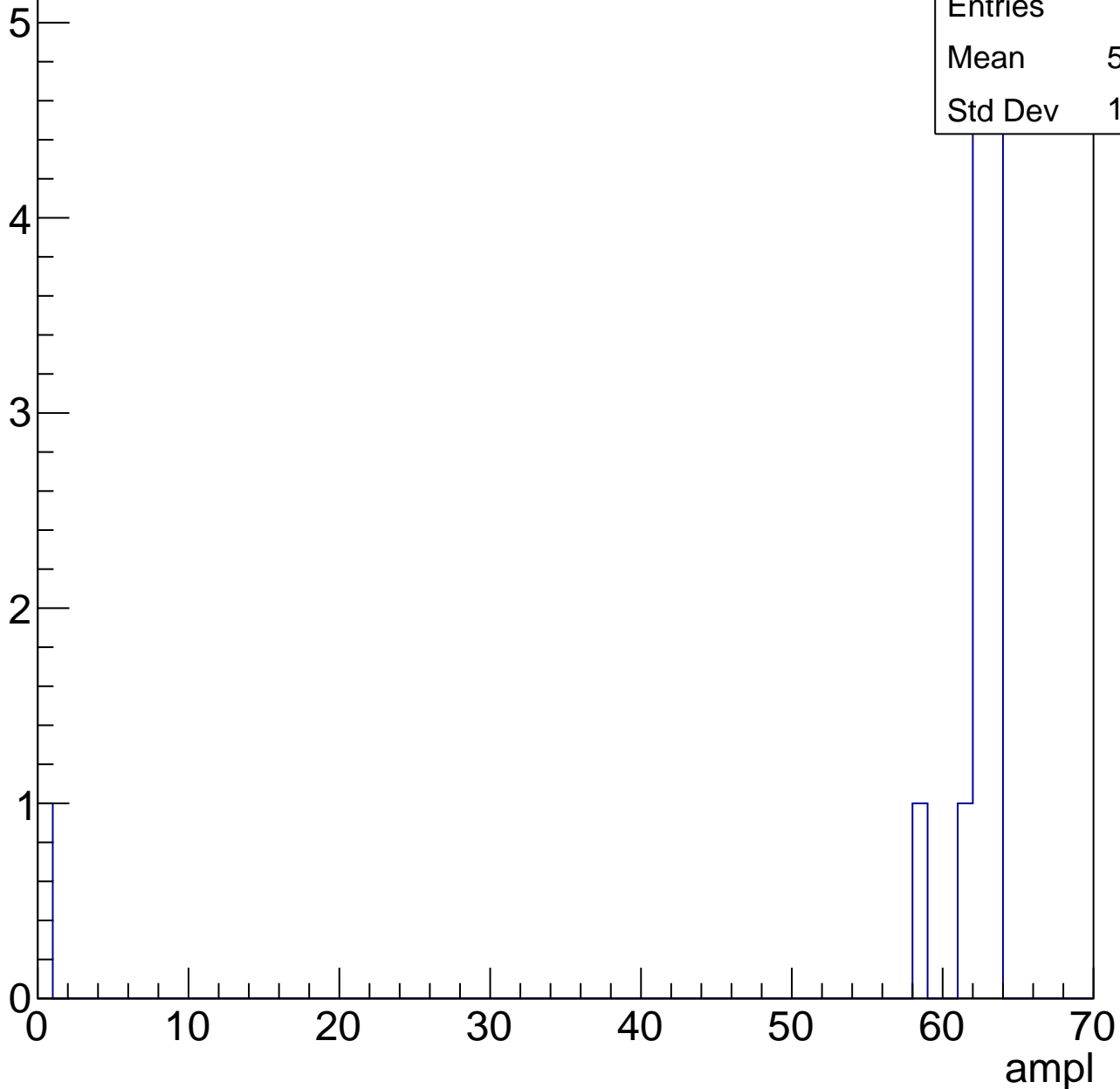


B1L103S, U9-ch78, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	13
Mean	57.23
Std Dev	16.57



B1L103S, U9-ch78, adc7

calib_packv5_041523_1651.root, FC#0, port C2

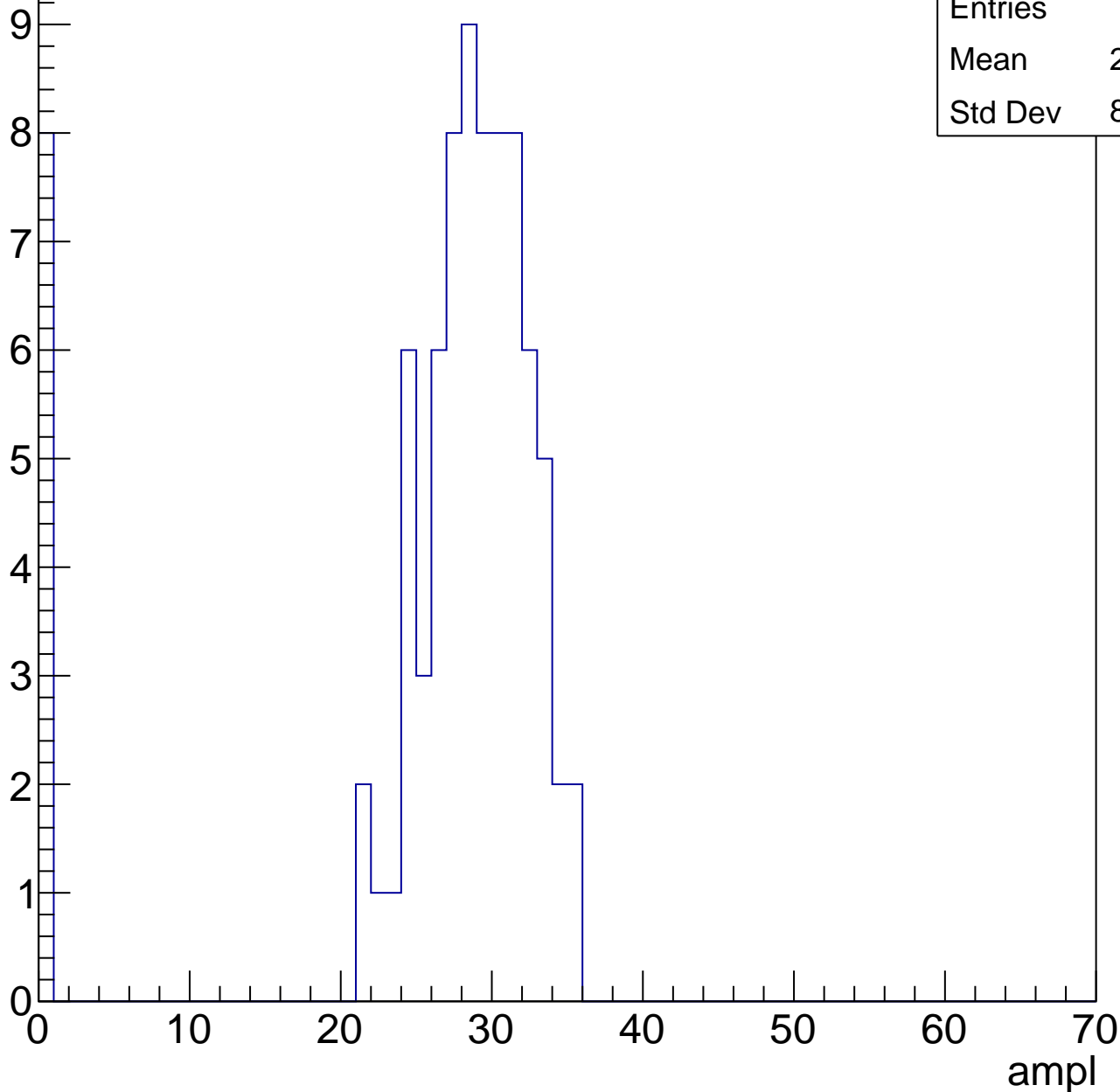
Entry



B1L103S, U9-ch79, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch79, adc1

calib_packv5_041523_1651.root, FC#0, port C2

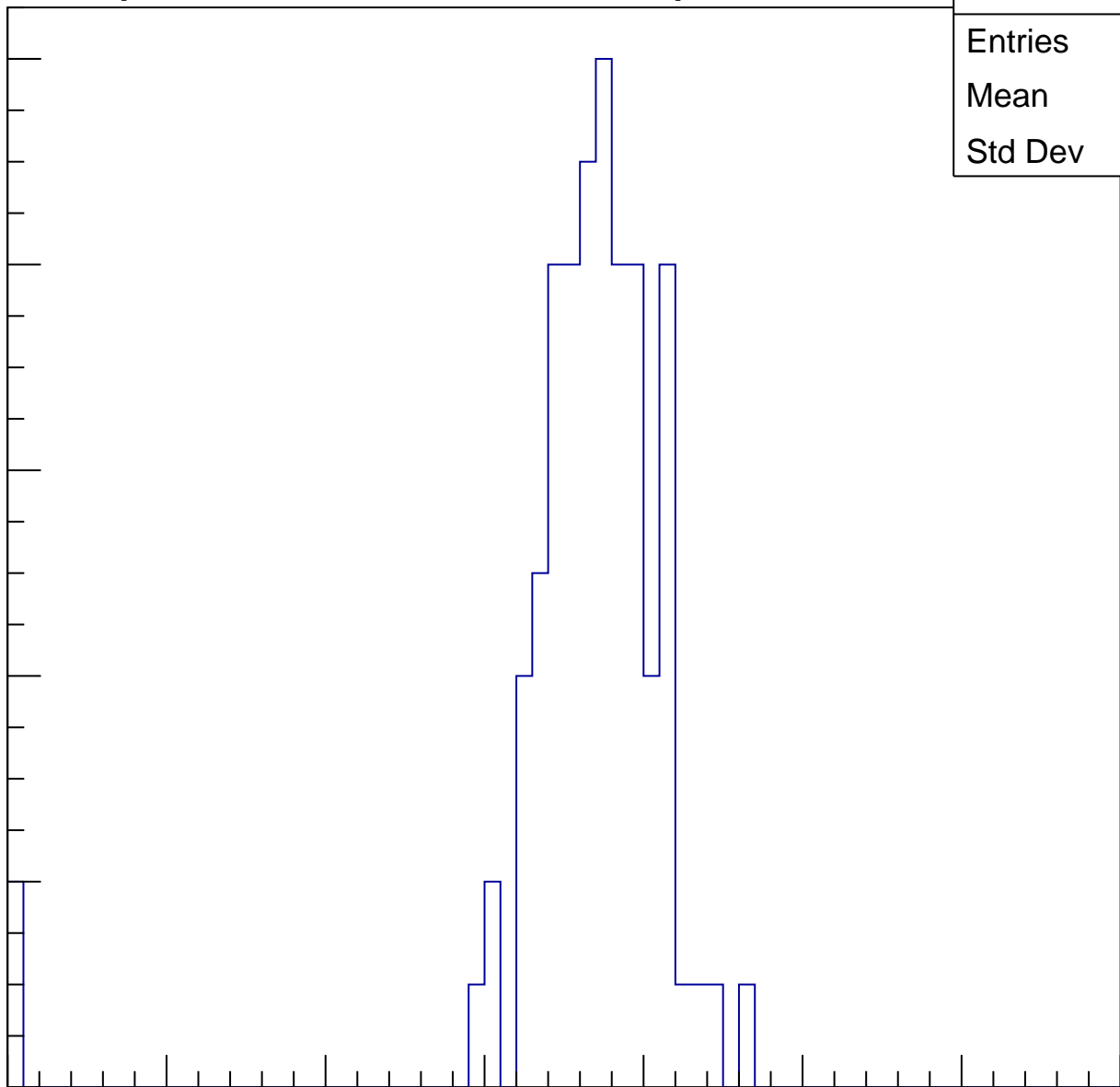
Entries	81
Mean	35.89
Std Dev	6.562

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl



B1L103S, U9-ch79, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	53
Mean	34.21
Std Dev	17.74

Entry

10

8

6

4

2

0

0

10

20

30

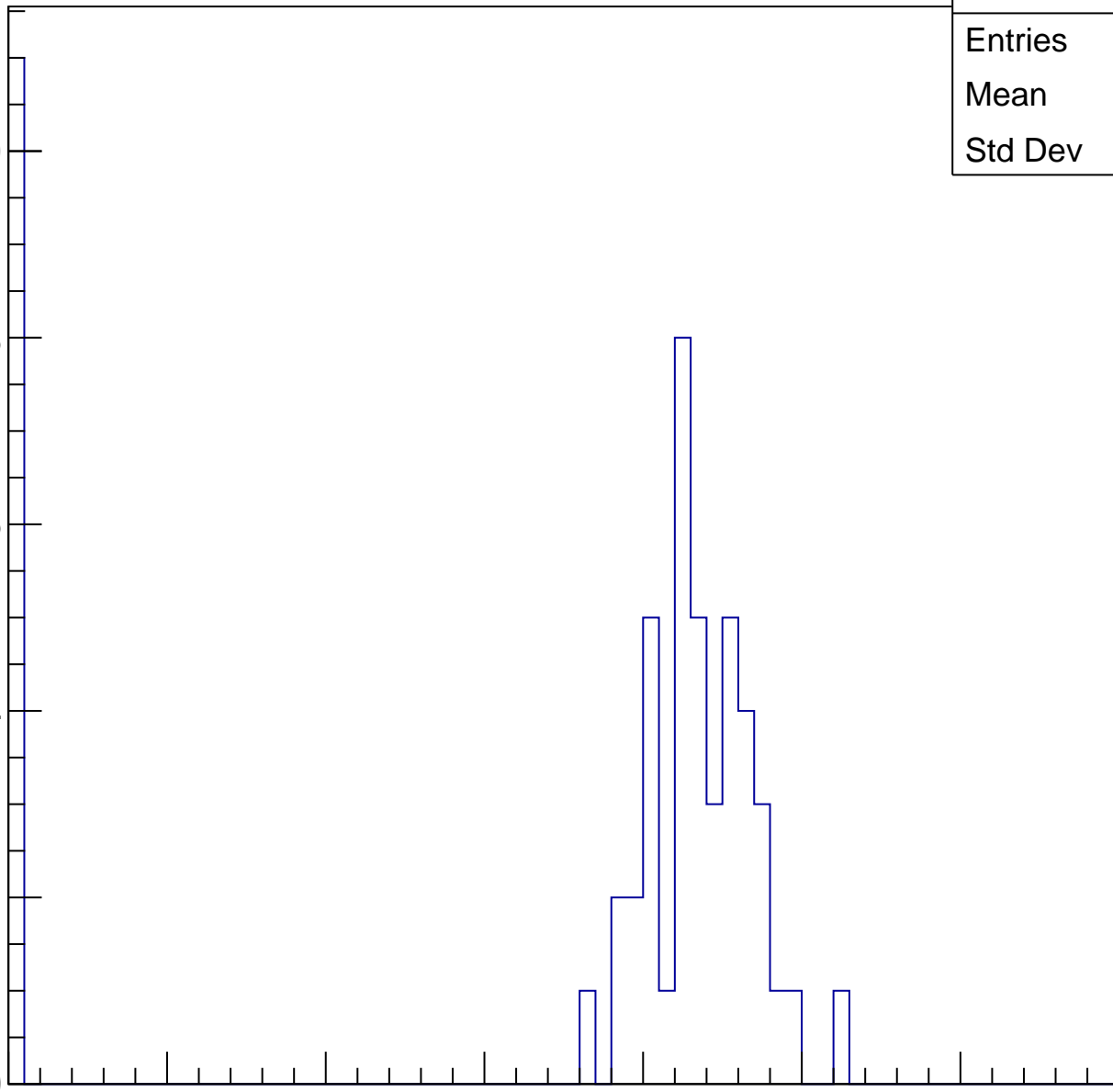
40

50

60

70

ampl

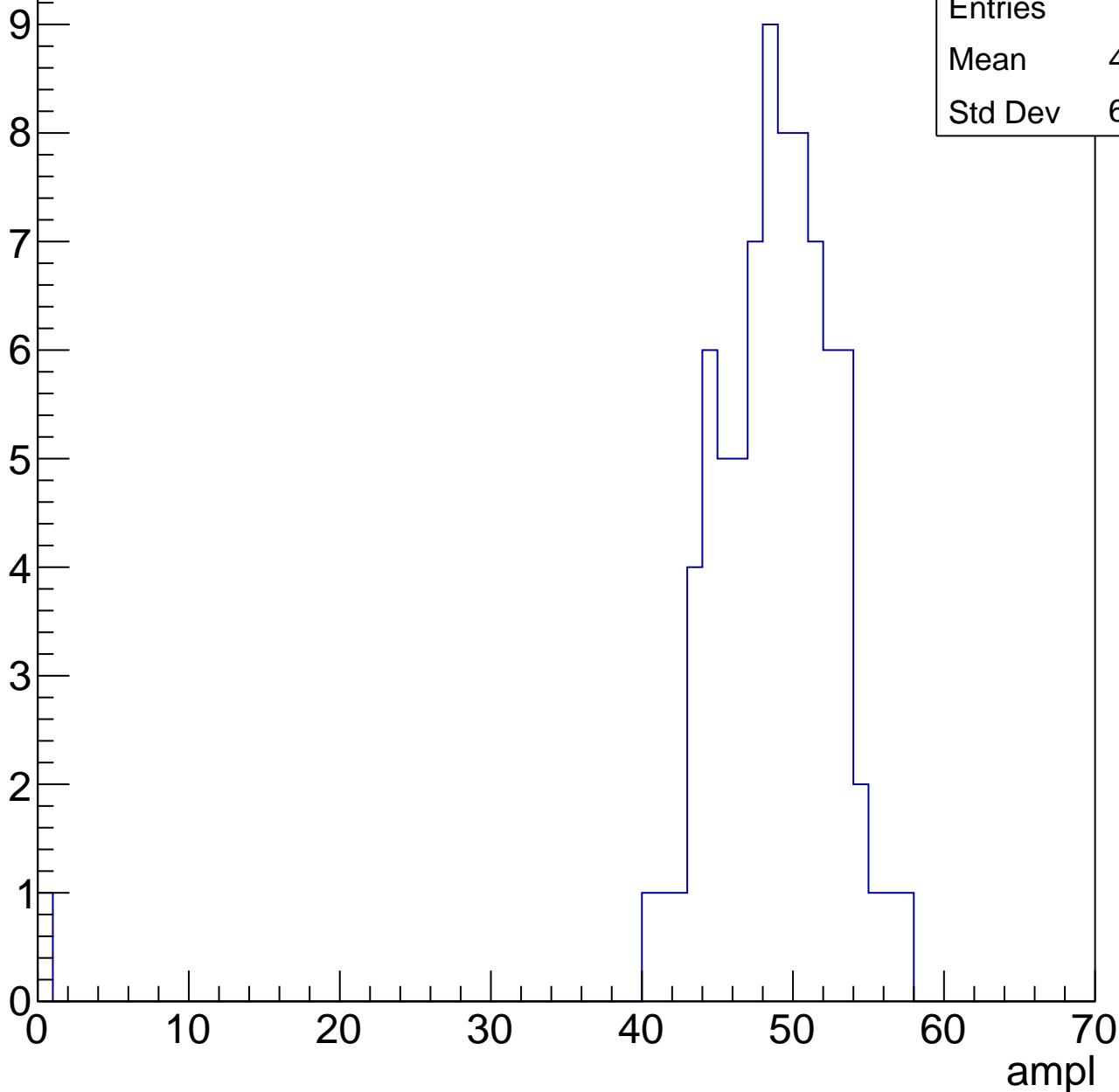


B1L103S, U9-ch79, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	80
Mean	47.88
Std Dev	6.456

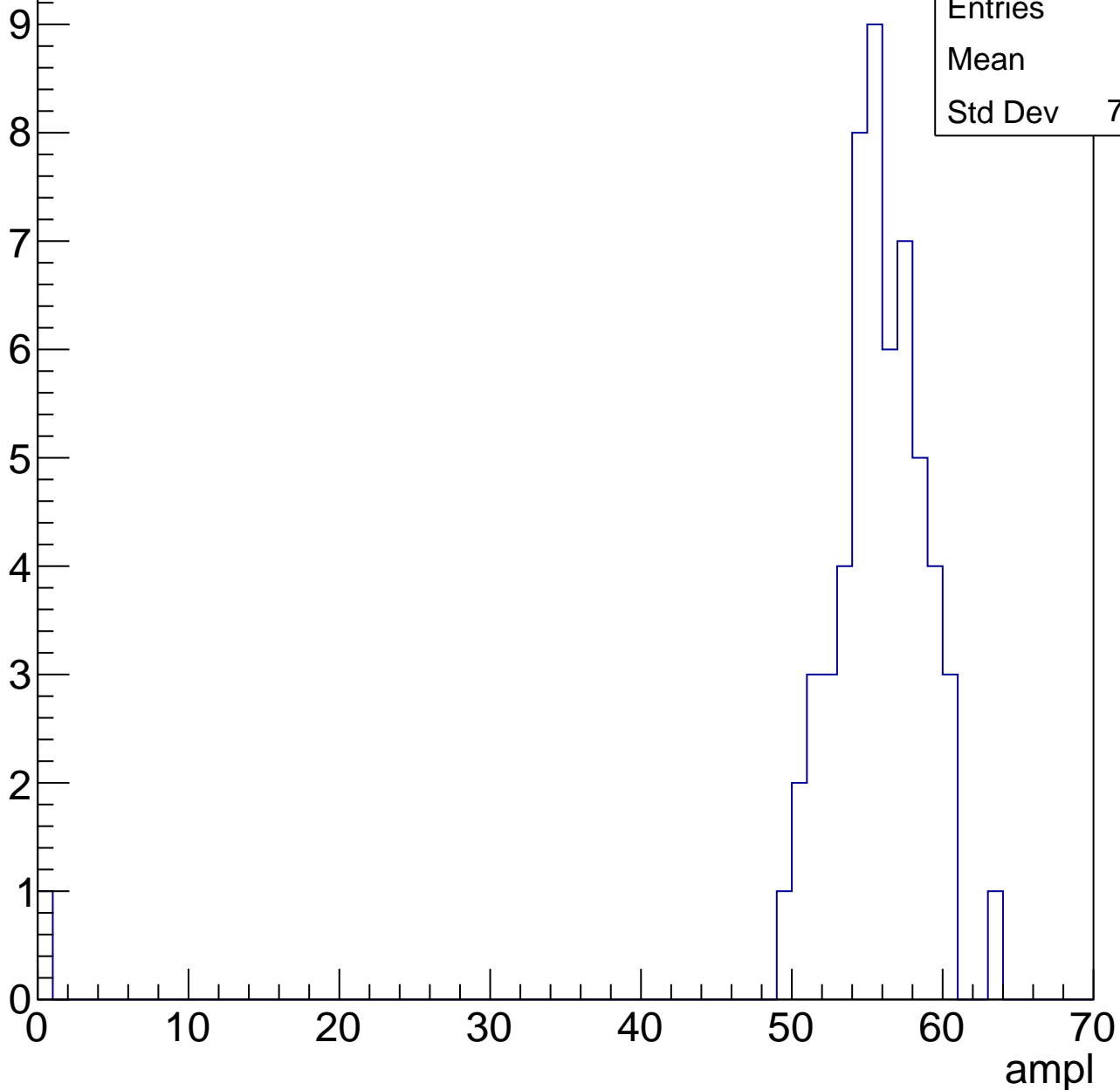


B1L103S, U9-ch79, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	54.4
Std Dev	7.804

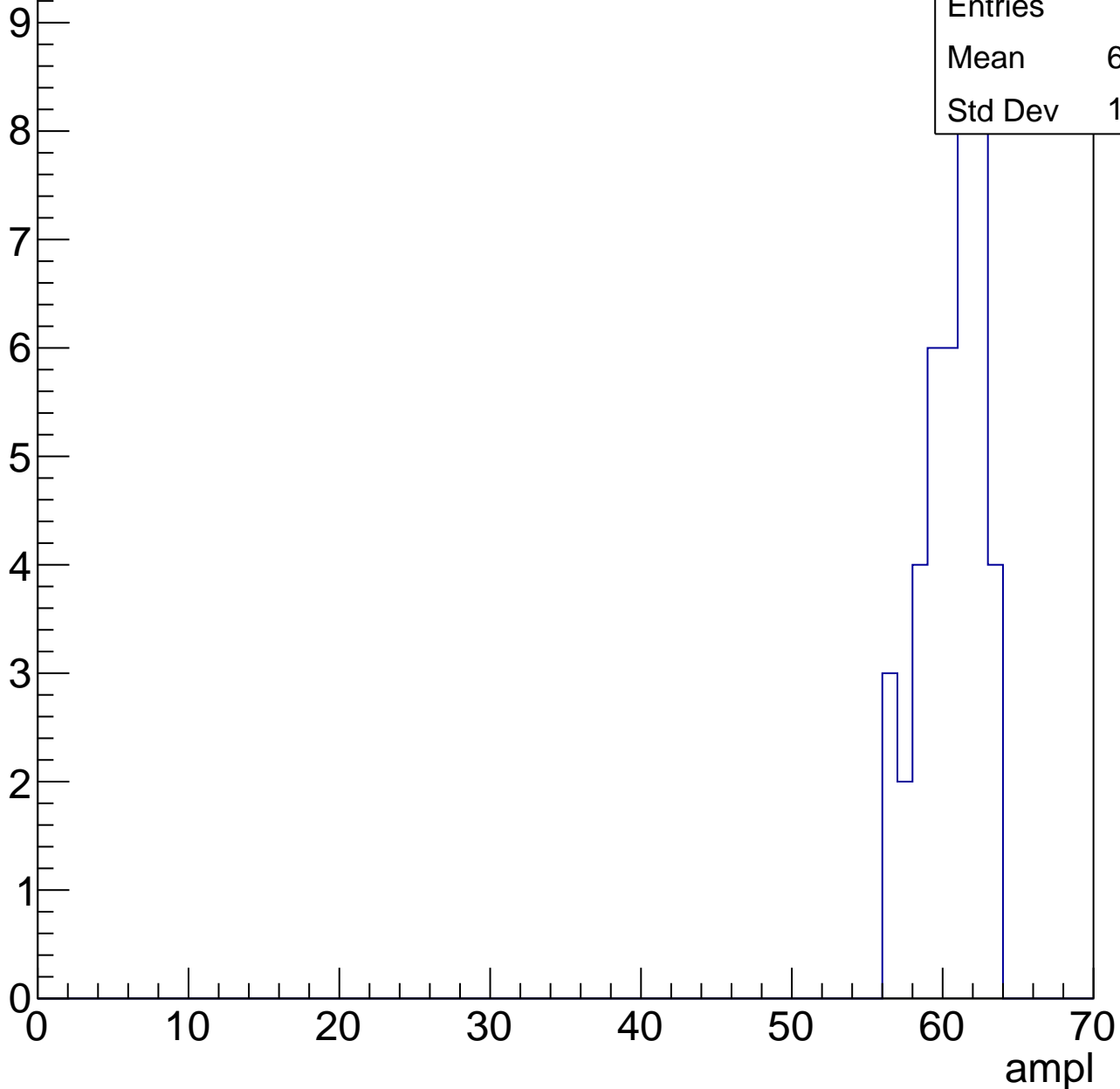


B1L103S, U9-ch79, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	43
Mean	60.16
Std Dev	1.976

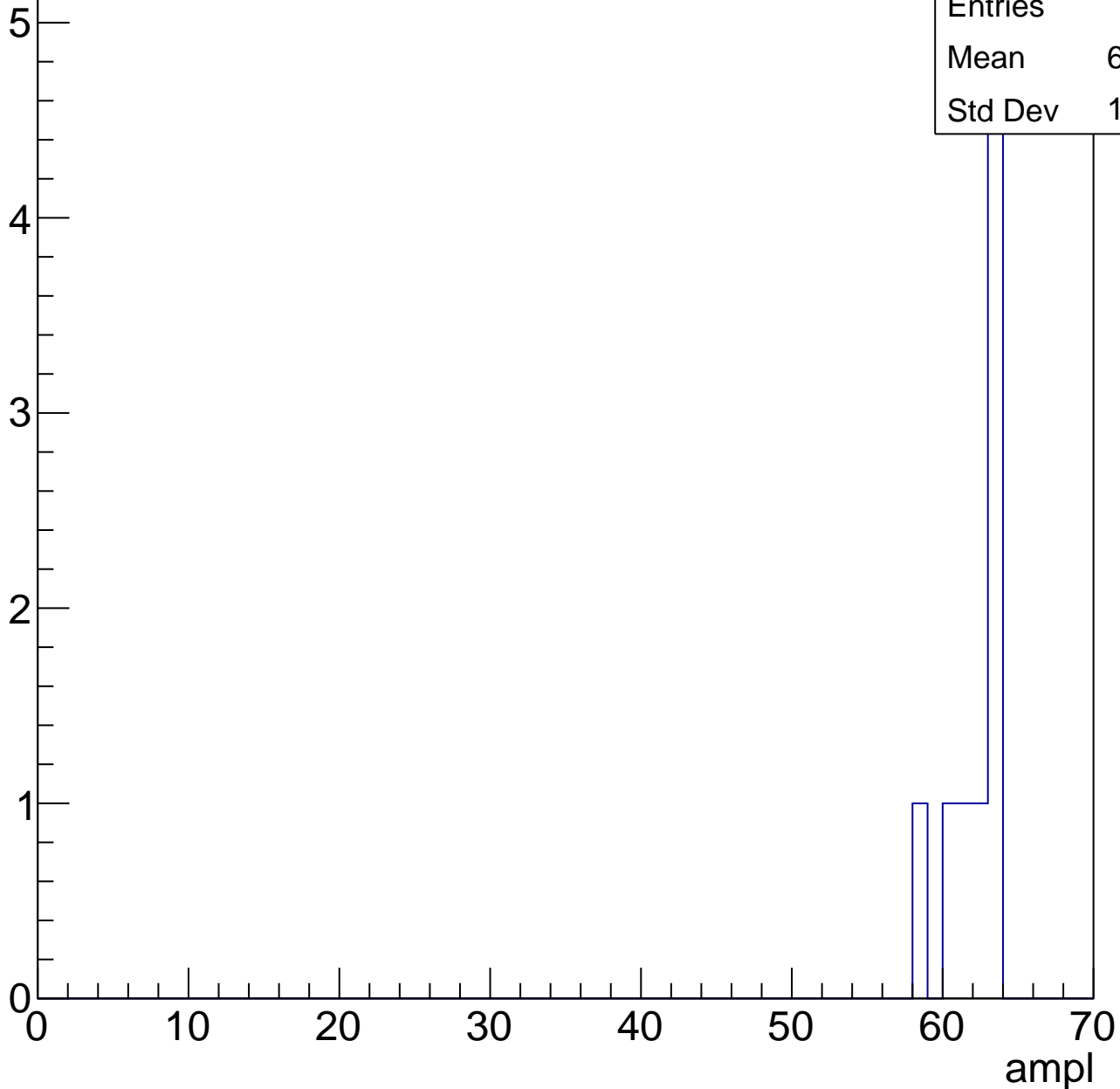


B1L103S, U9-ch79, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

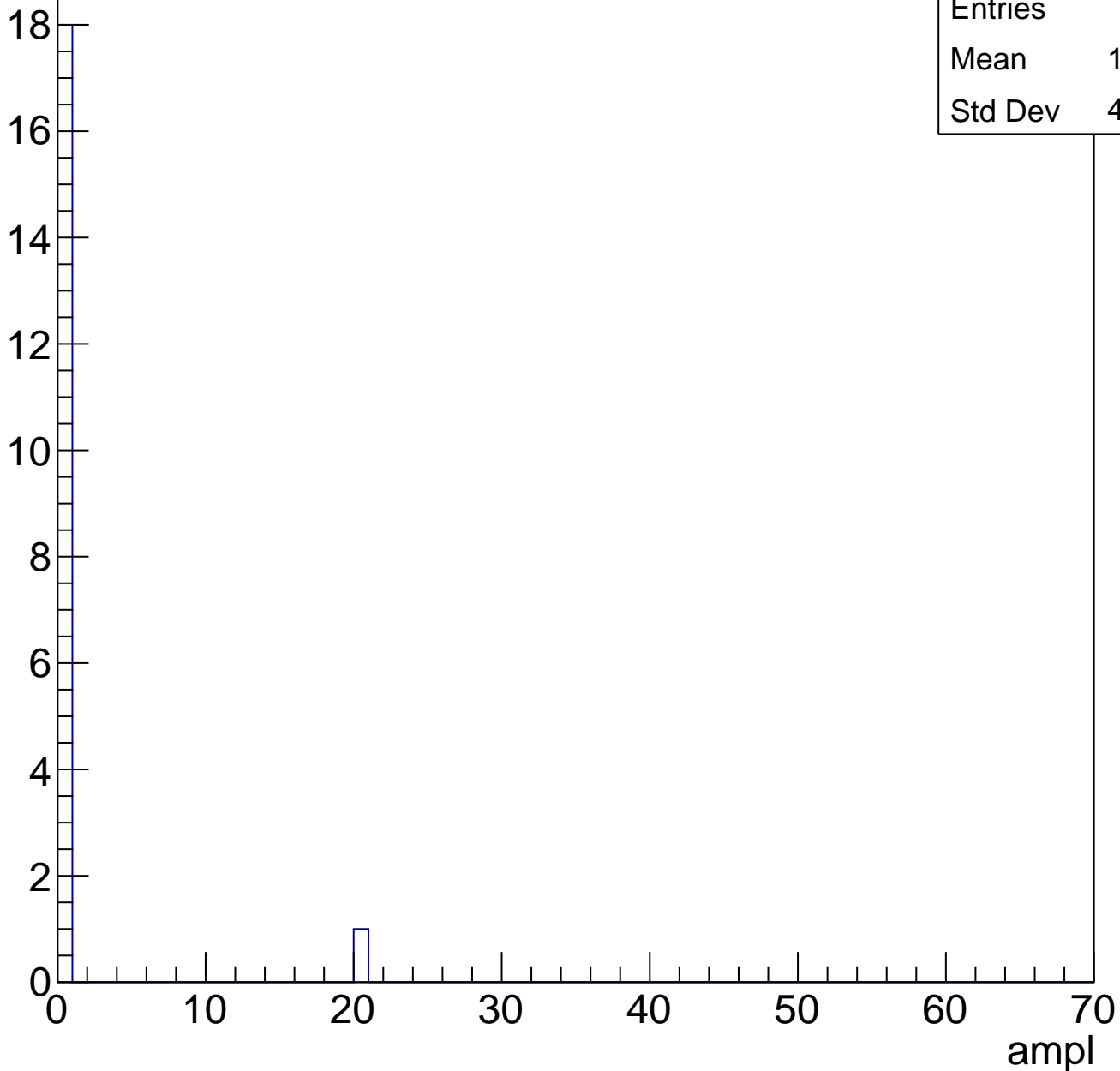
Entries	9
Mean	61.78
Std Dev	1.685



B1L103S, U9-ch79, adc7

calib_packv5_041523_1651.root, FC#0, port C2

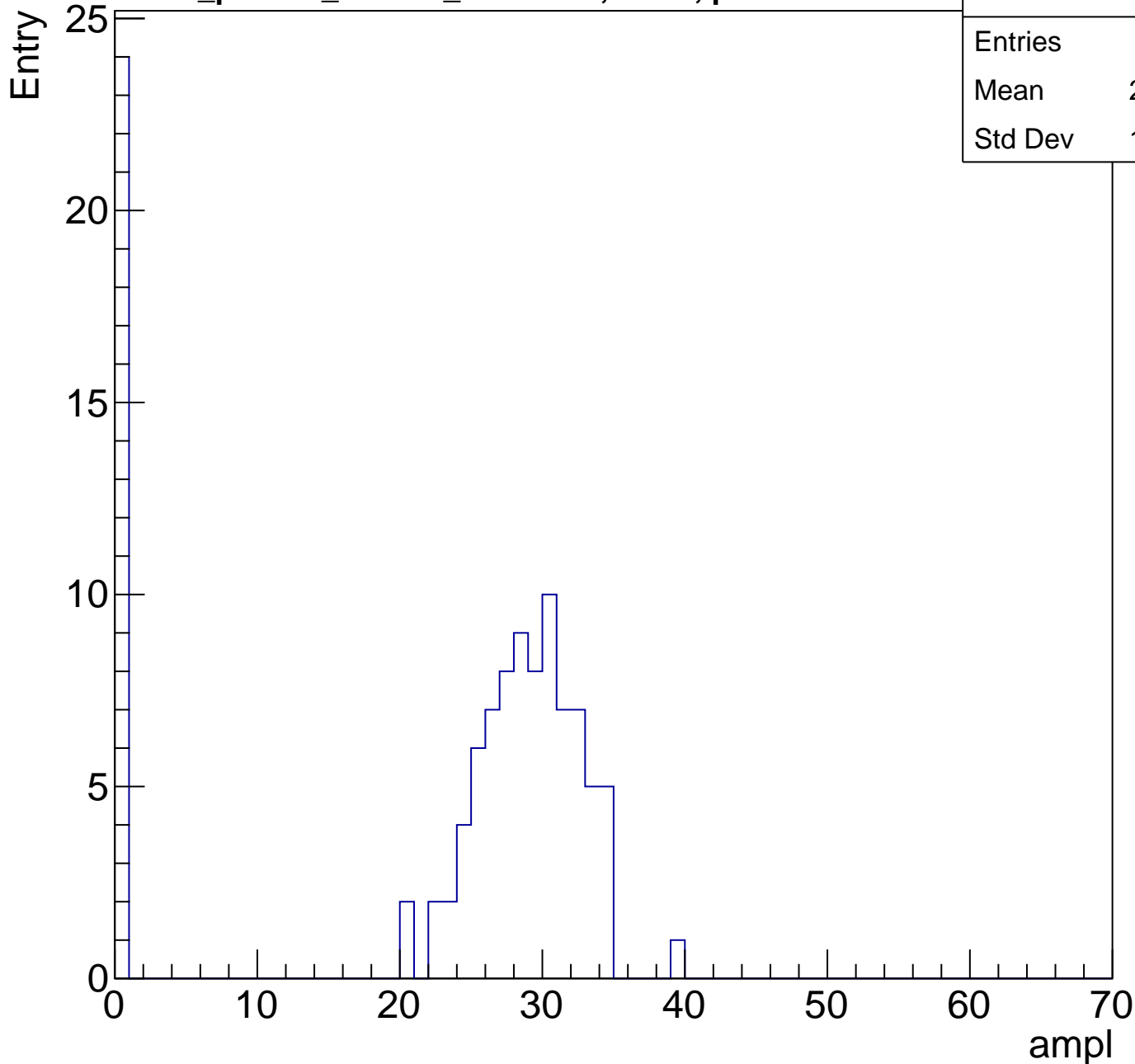
Entry



B1L103S, U9-ch80, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	107
Mean	22.18
Std Dev	12.32

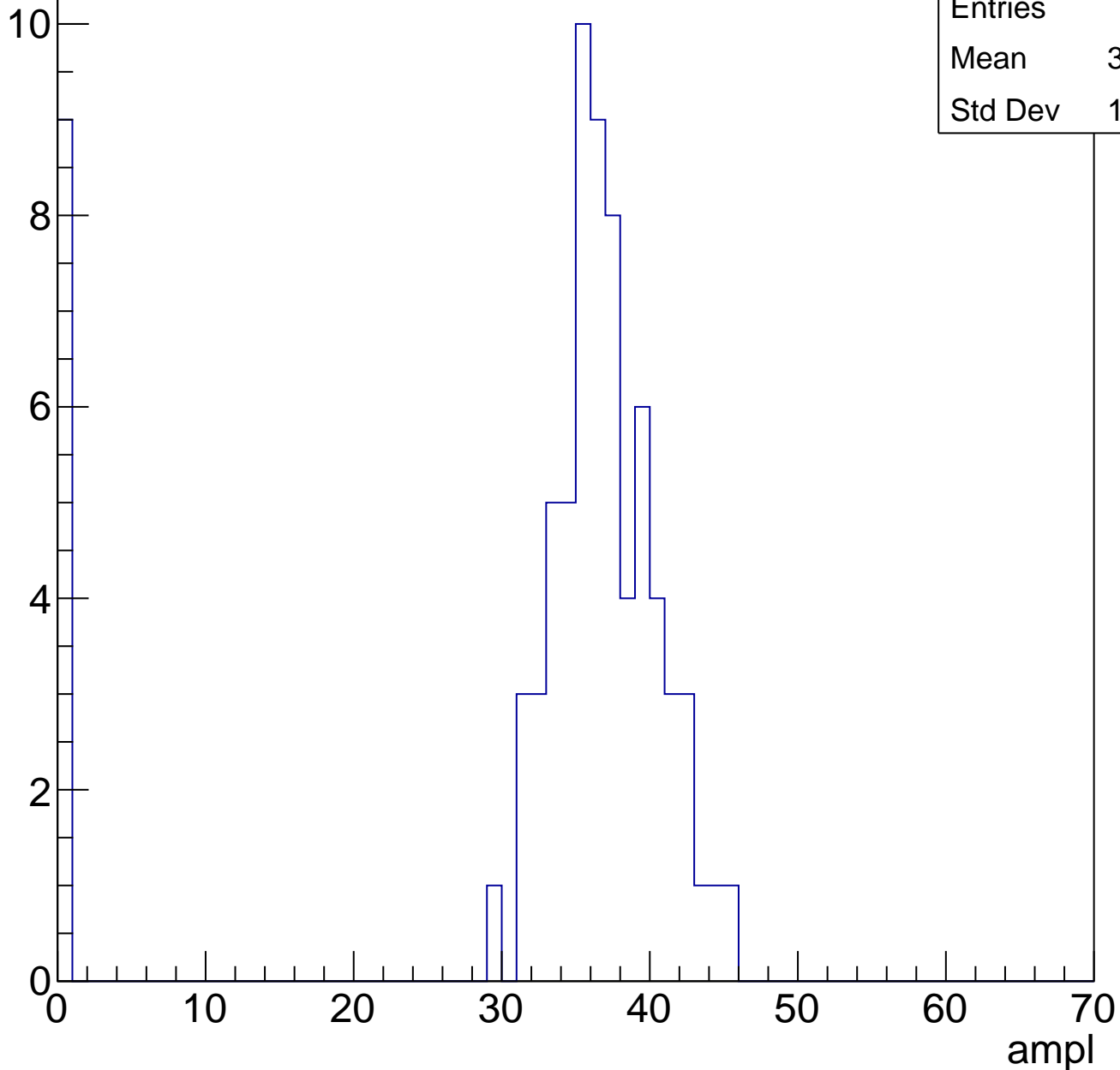


B1L103S, U9-ch80, adc1

calib_packv5_041523_1651.root, FC#0, port C2

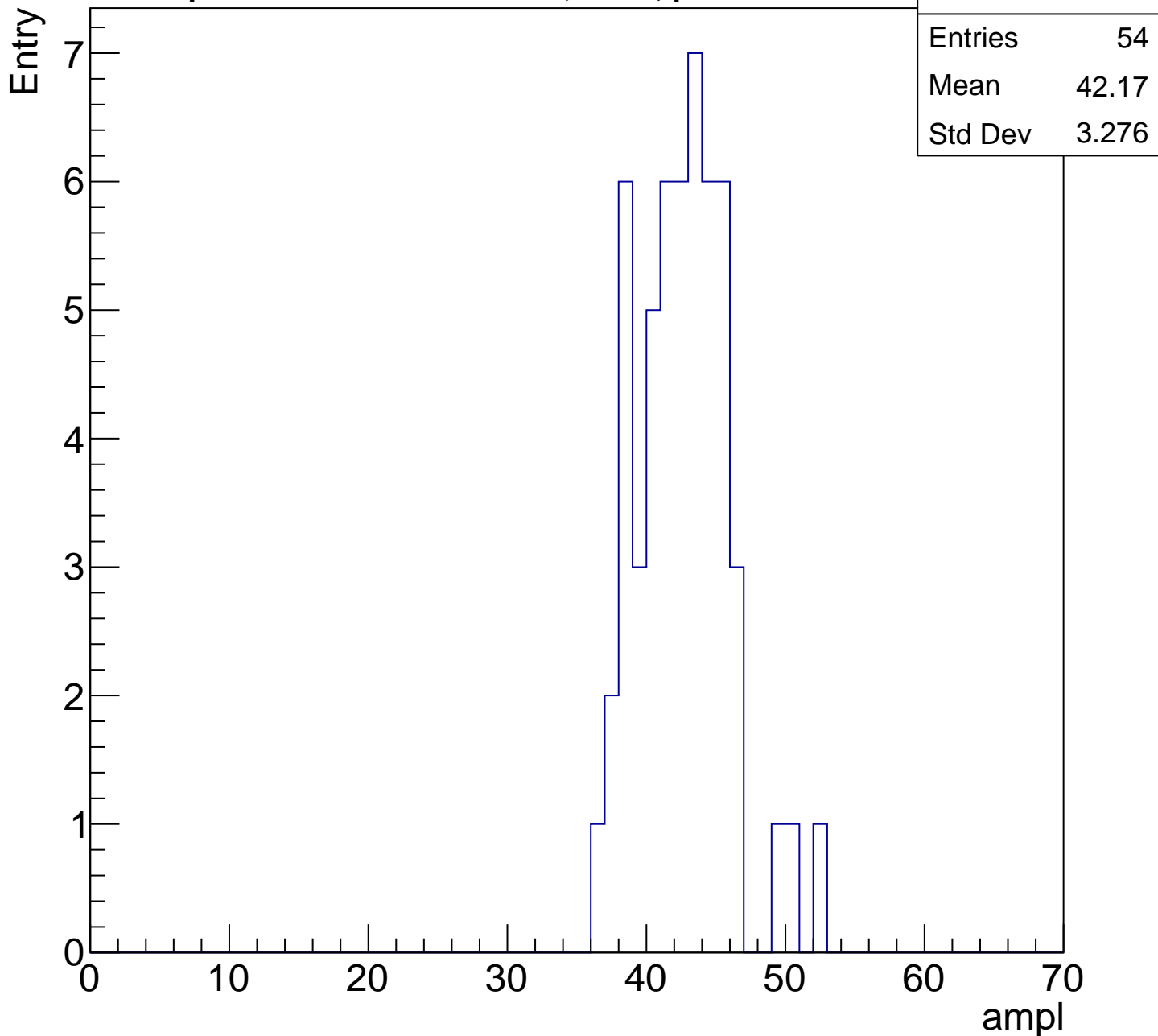
Entries	76
Mean	32.24
Std Dev	12.22

Entry



B1L103S, U9-ch80, adc2

calib_packv5_041523_1651.root, FC#0, port C2

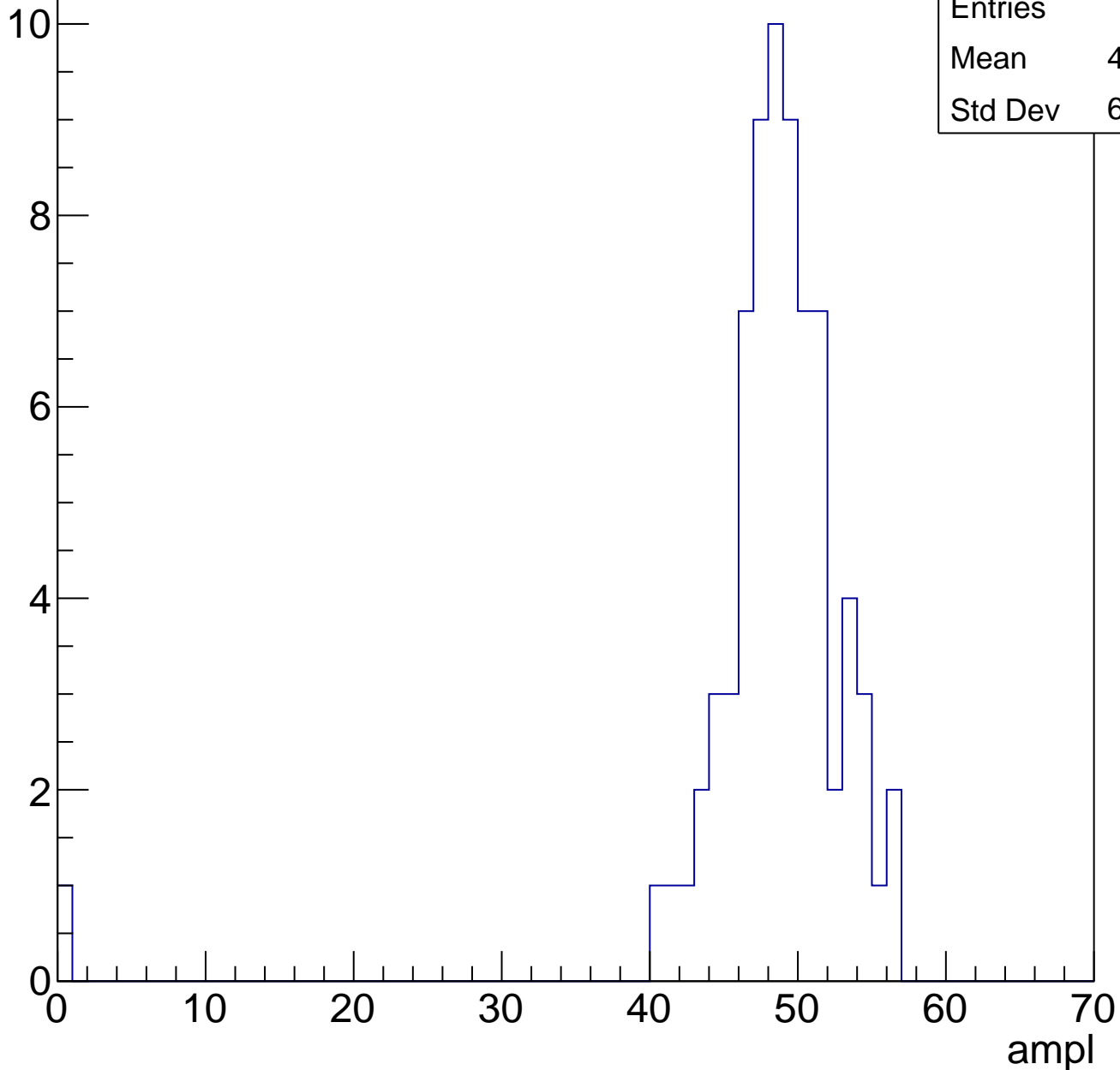


B1L103S, U9-ch80, adc3

calib_packv5_041523_1651.root, FC#0, port C2

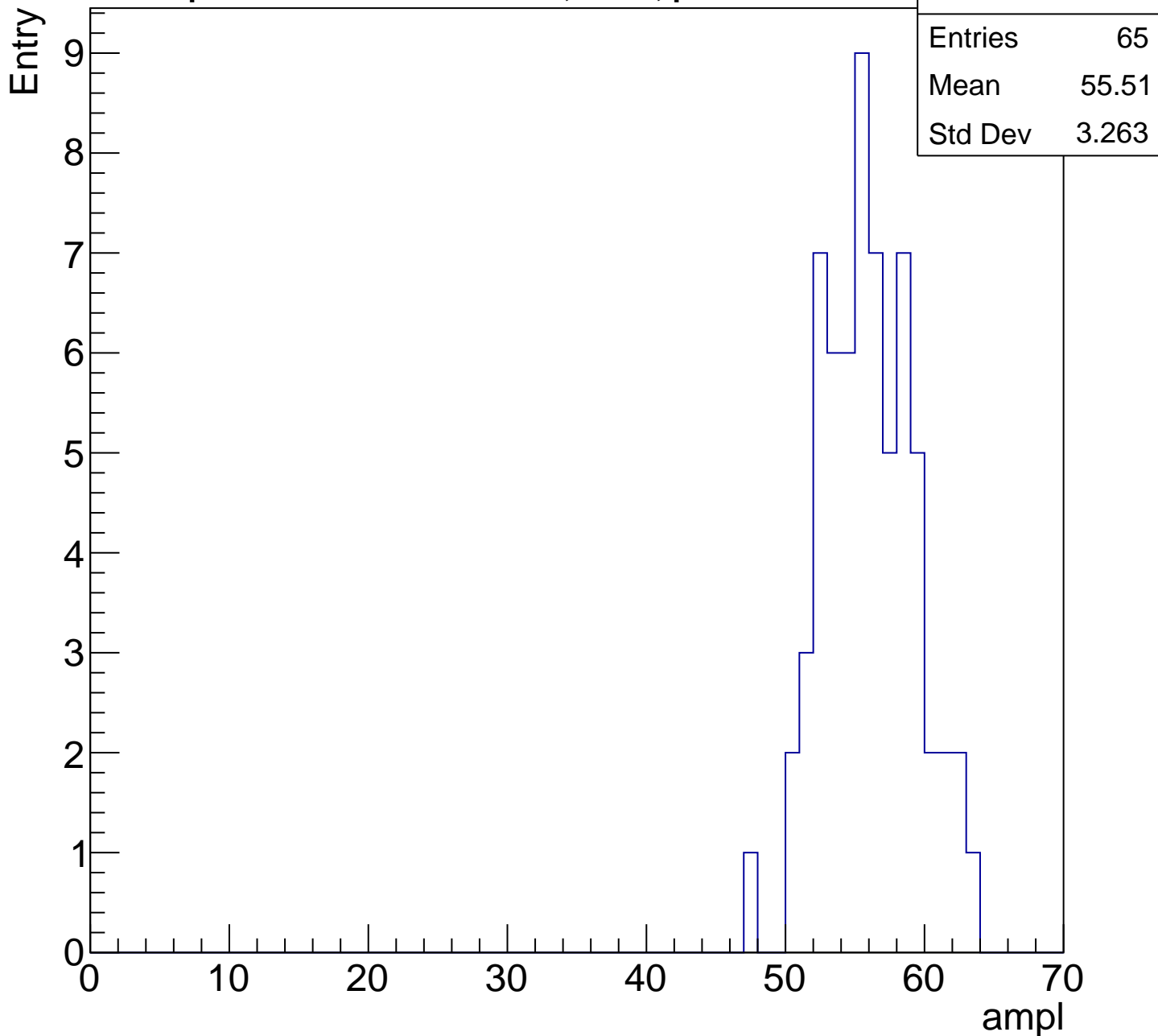
Entries	73
Mean	47.86
Std Dev	6.549

Entry



B1L103S, U9-ch80, adc4

calib_packv5_041523_1651.root, FC#0, port C2

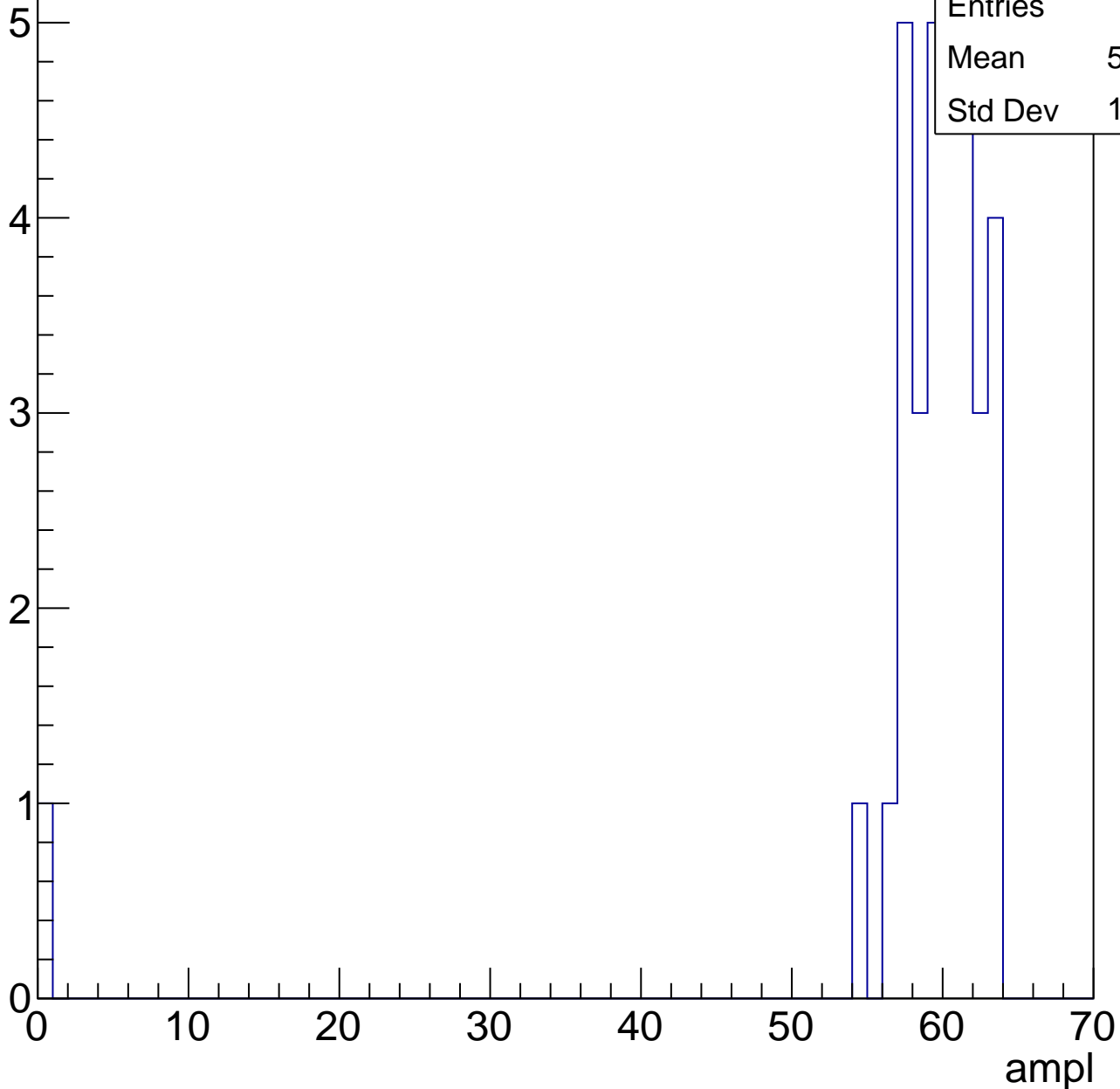


B1L103S, U9-ch80, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	33
Mean	57.79
Std Dev	10.45

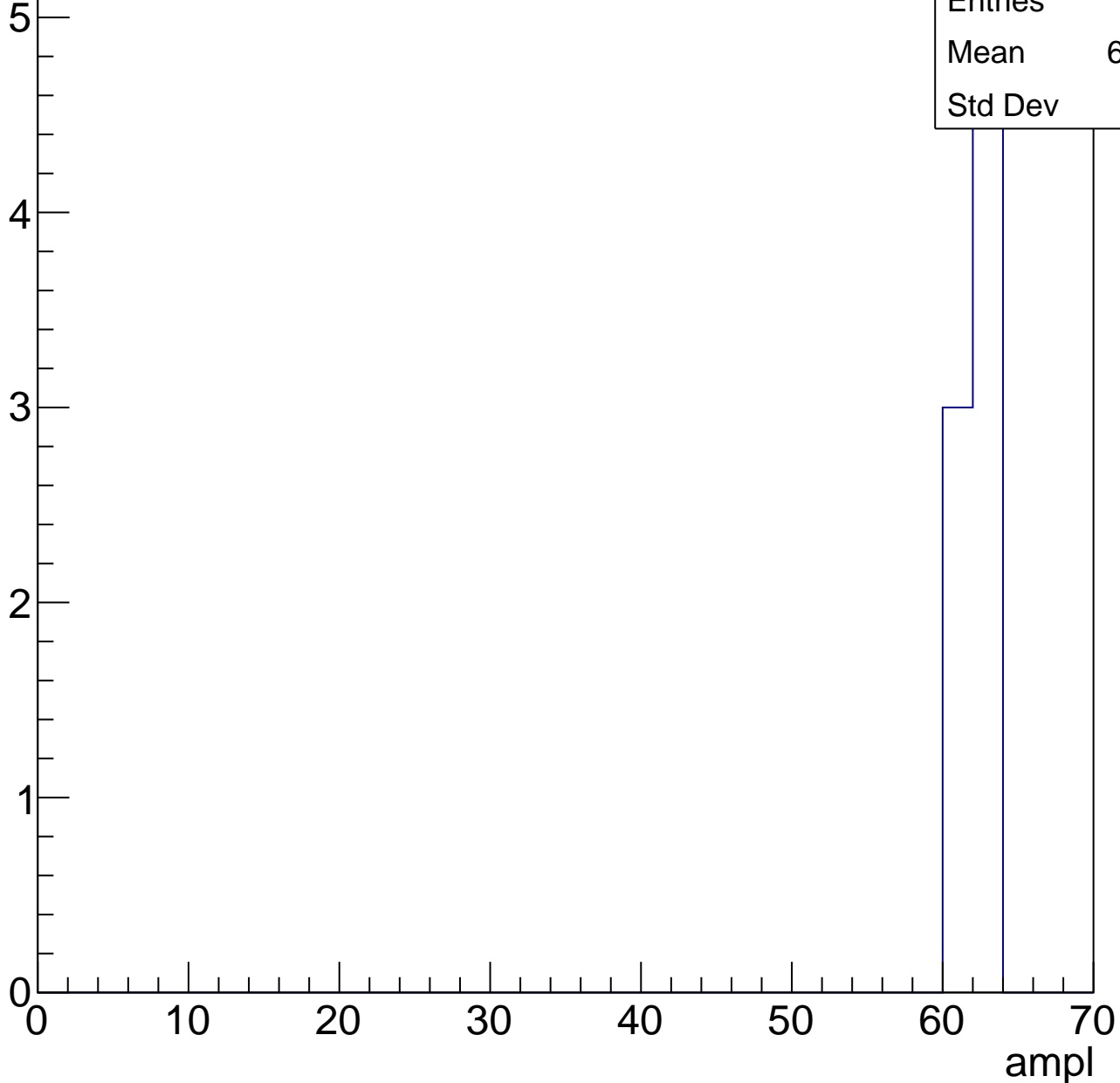


B1L103S, U9-ch80, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	16
Mean	61.75
Std Dev	1.09



B1L103S, U9-ch80, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U9-ch81, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	26.26
Std Dev	8.735

Entry

10
8
6
4
2
0

ampl

0

10

20

30

40

50

60

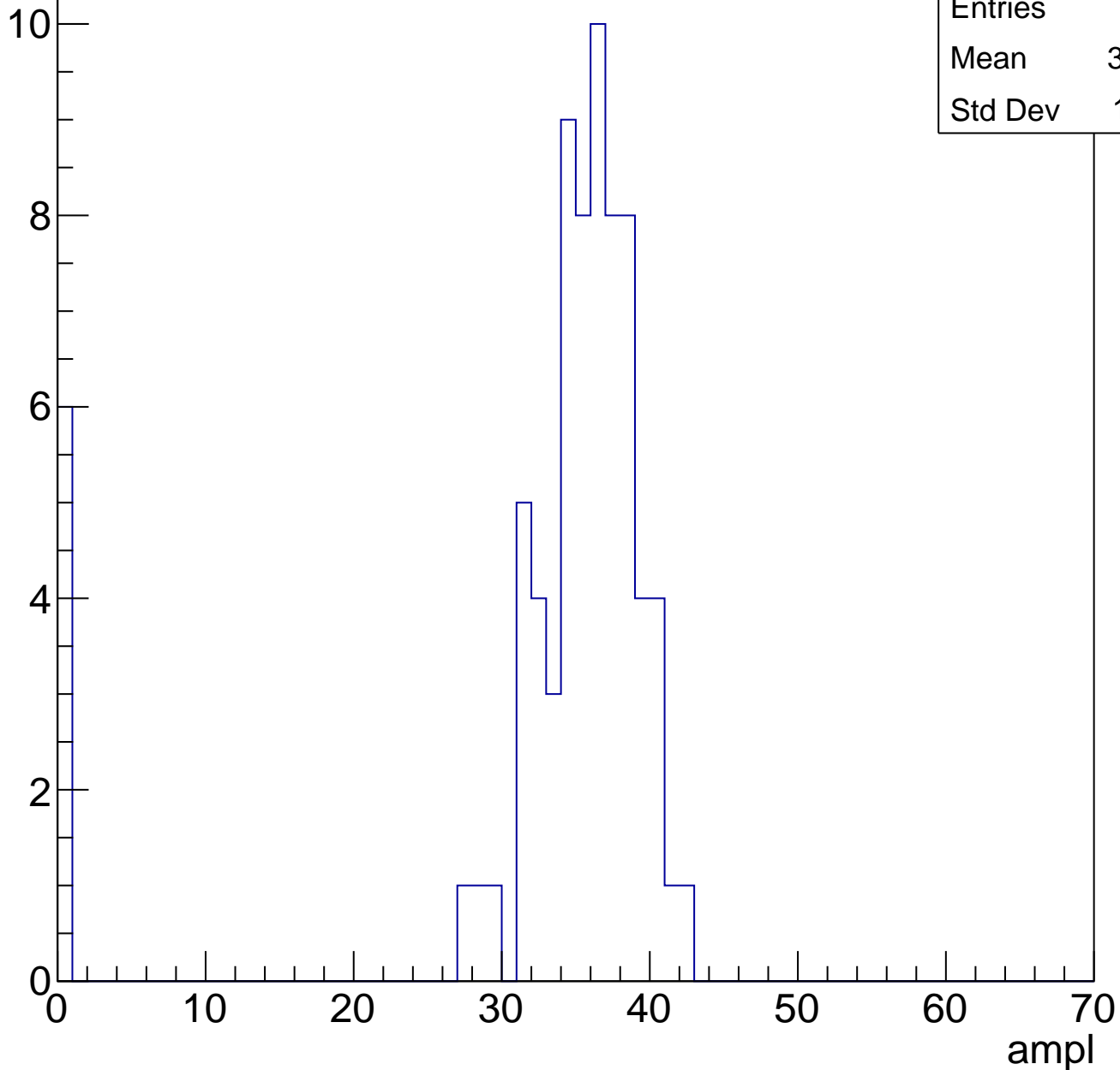
70

B1L103S, U9-ch81, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	74
Mean	32.58
Std Dev	10.11

Entry

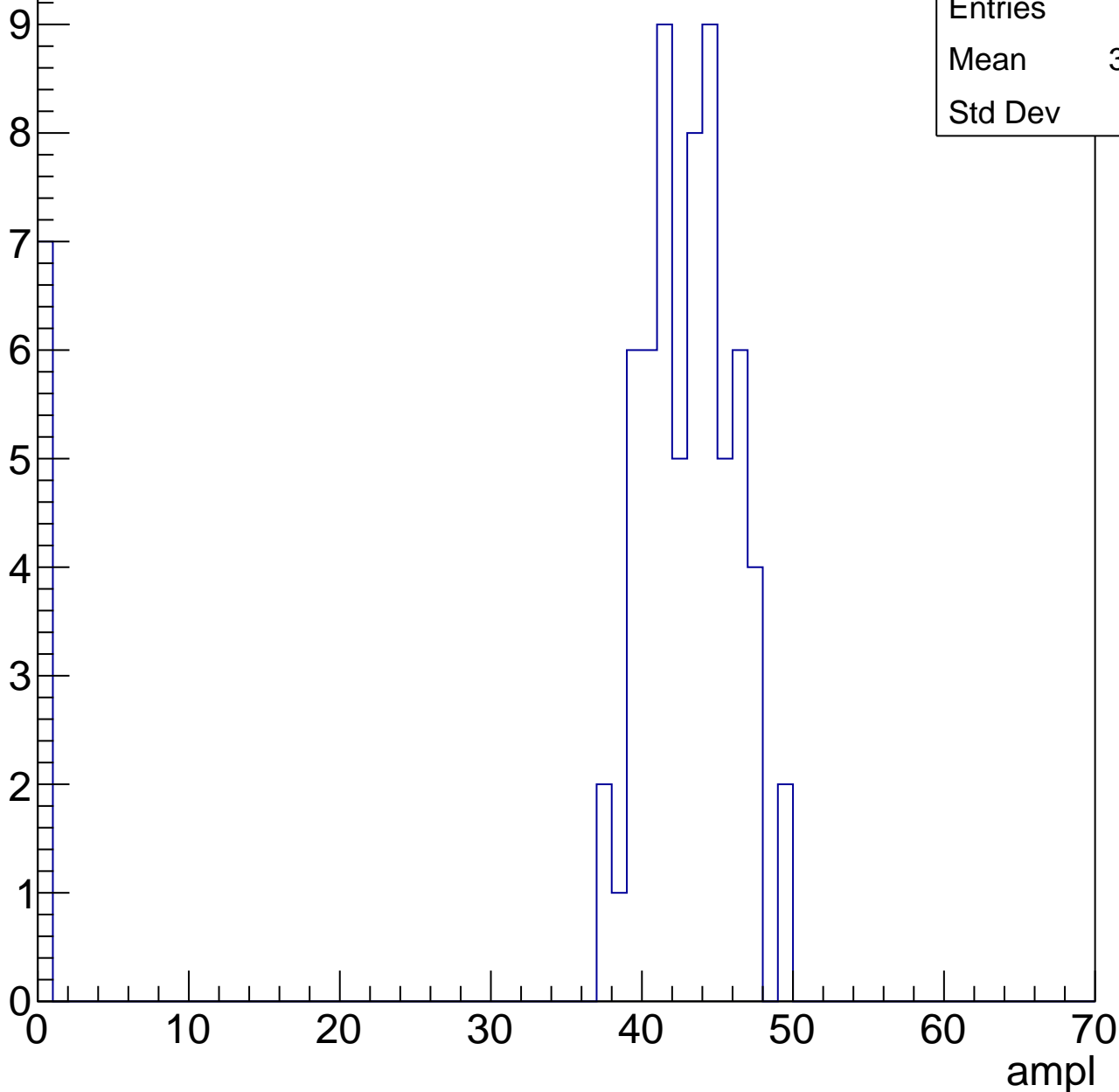


B1L103S, U9-ch81, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	38.46
Std Dev	13.1

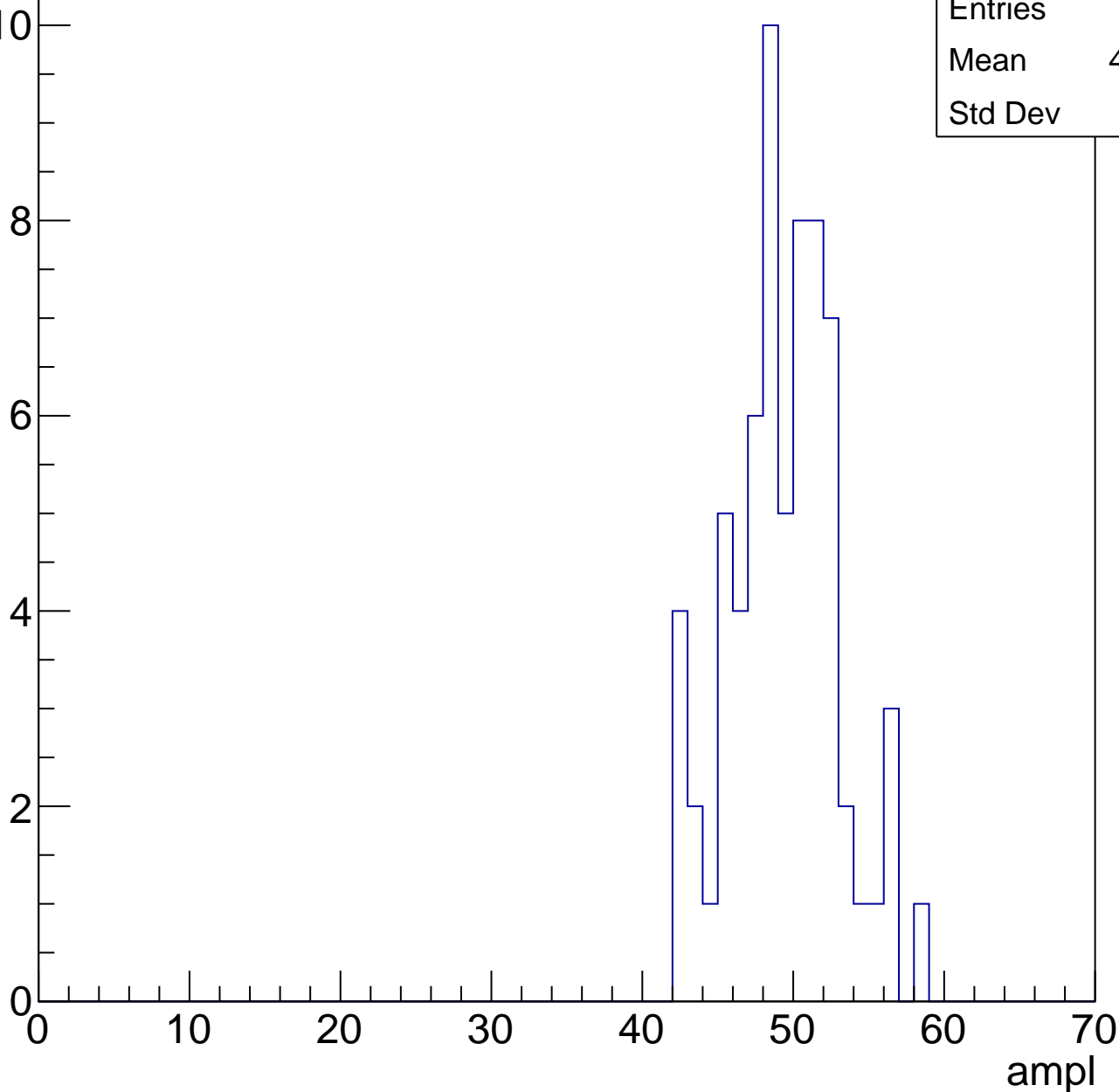


B1L103S, U9-ch81, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	48.93
Std Dev	3.57

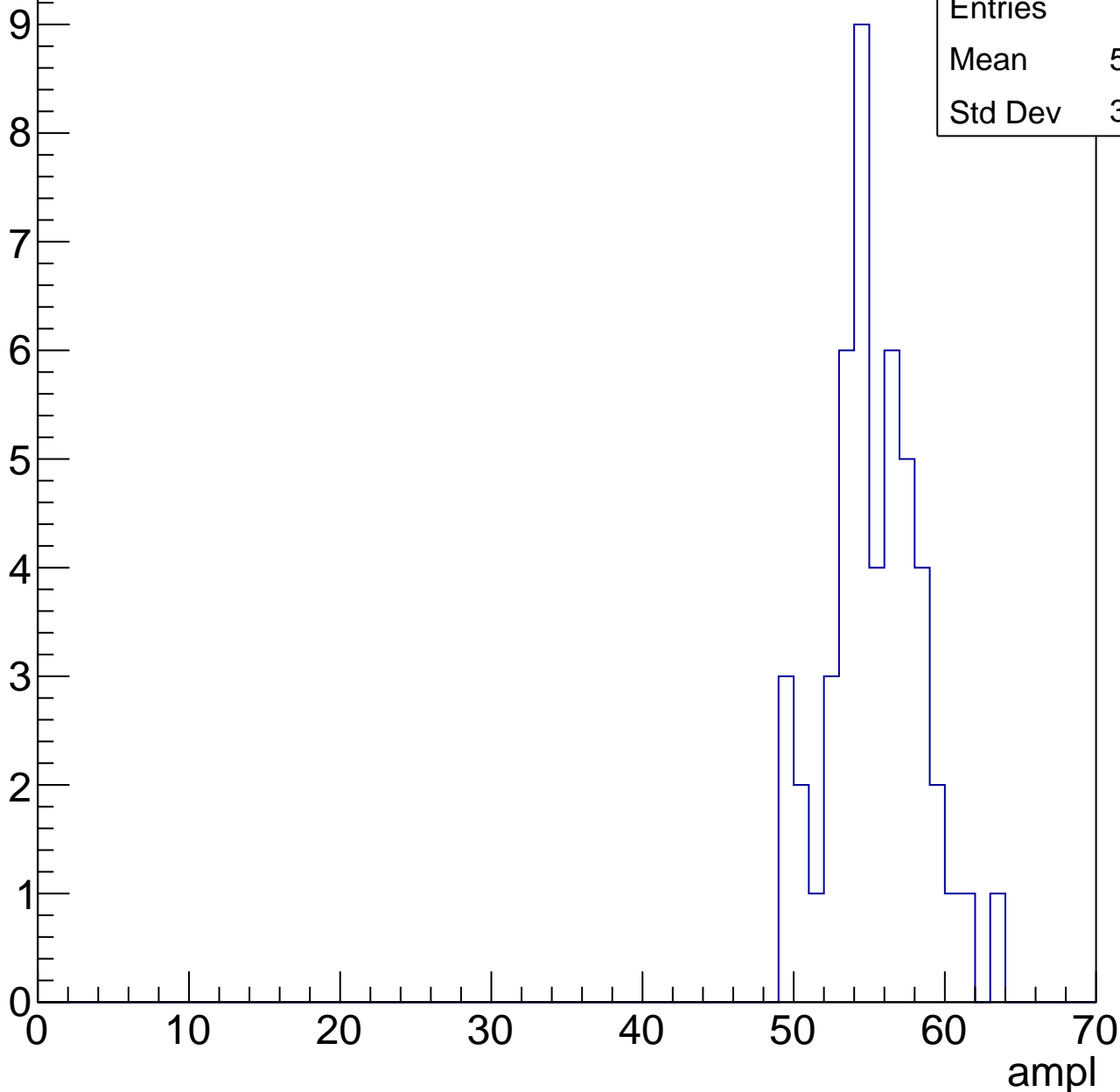


B1L103S, U9-ch81, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	48
Mean	54.85
Std Dev	3.069

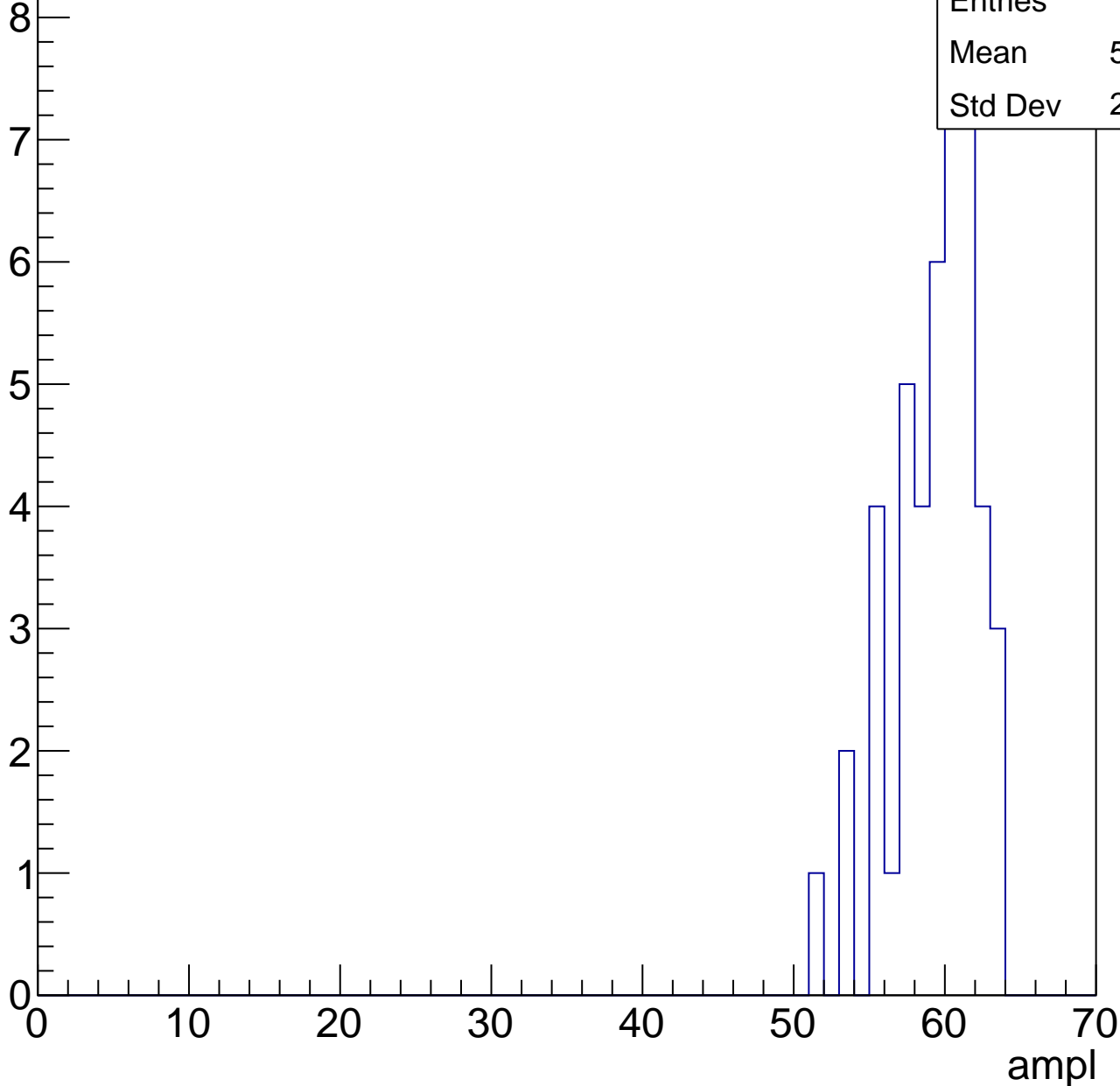


B1L103S, U9-ch81, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	46
Mean	58.89
Std Dev	2.784

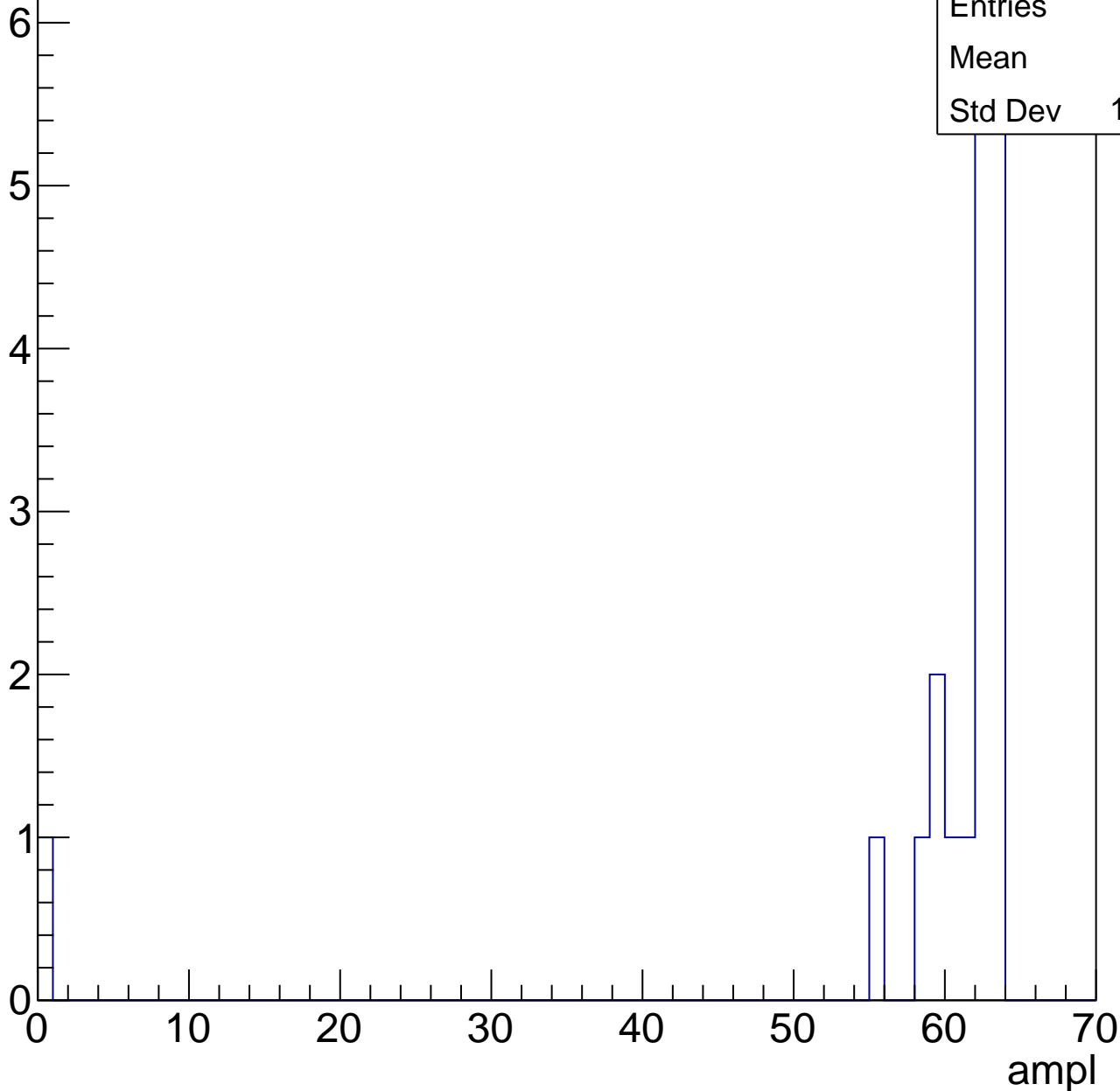


B1L103S, U9-ch81, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	19
Mean	58
Std Dev	13.83

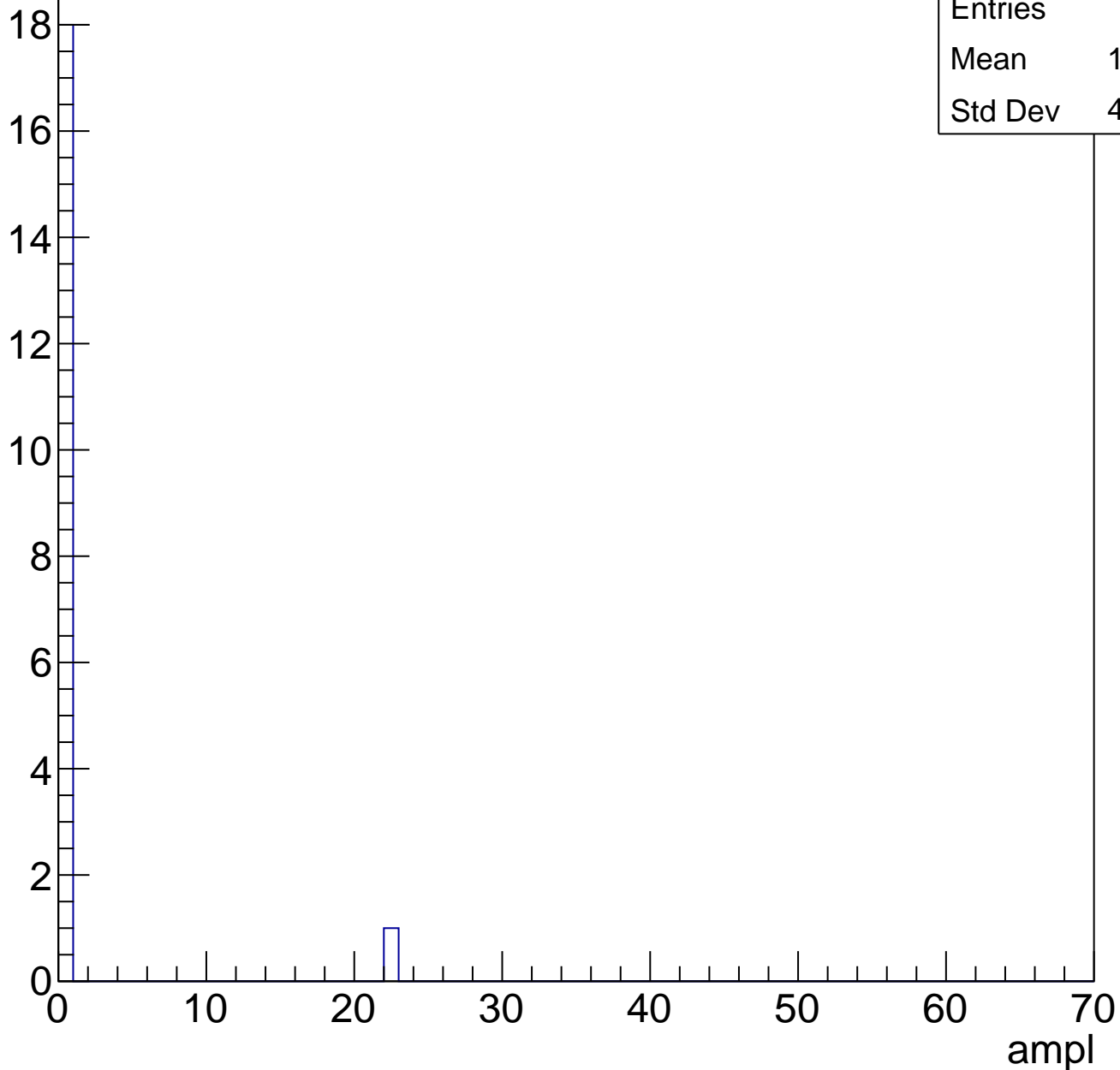


B1L103S, U9-ch81, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.158
Std Dev	4.913

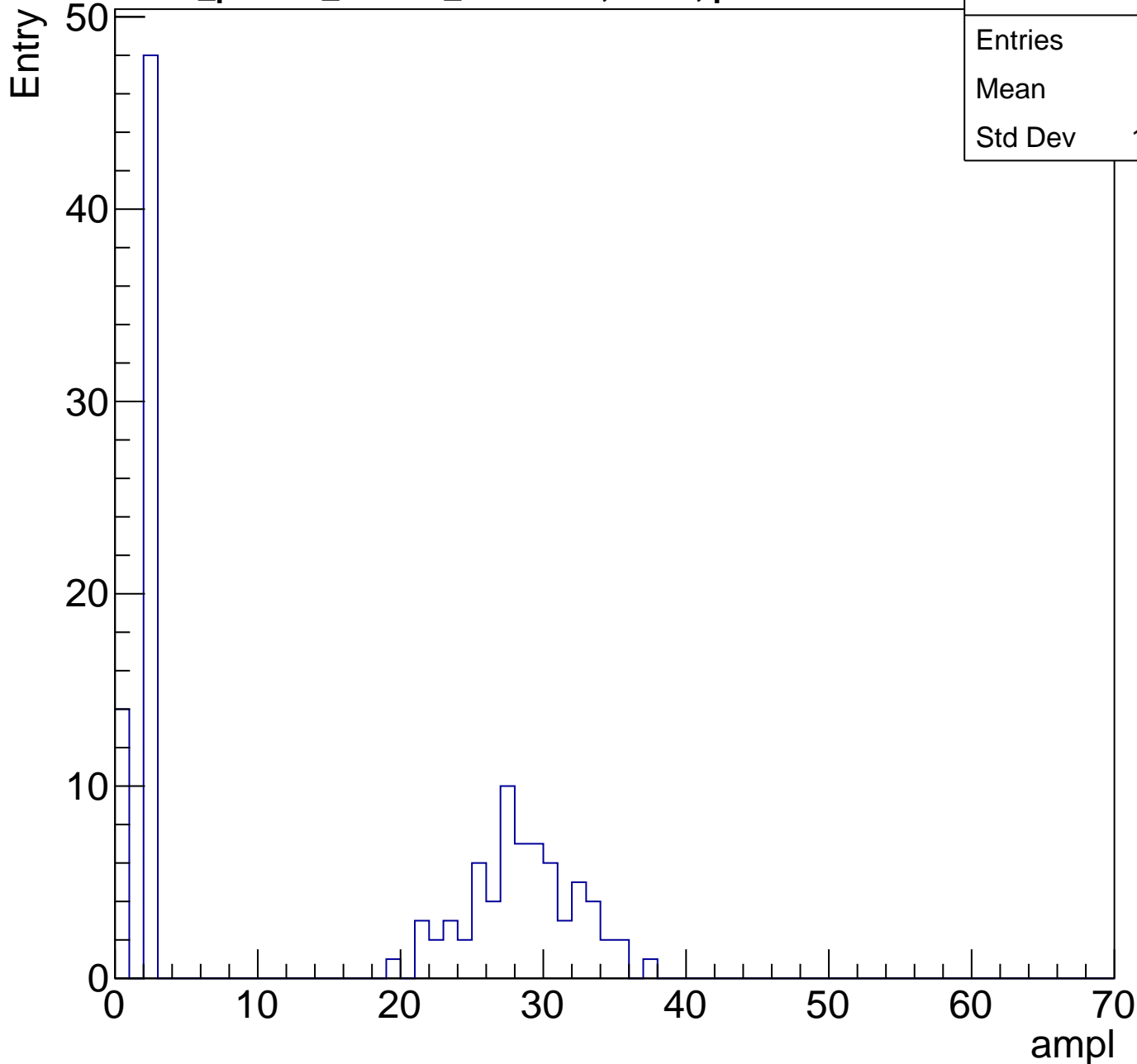
Entry



B1L103S, U9-ch82, adc0

calib_packv5_041523_1651.root, FC#0, port C2

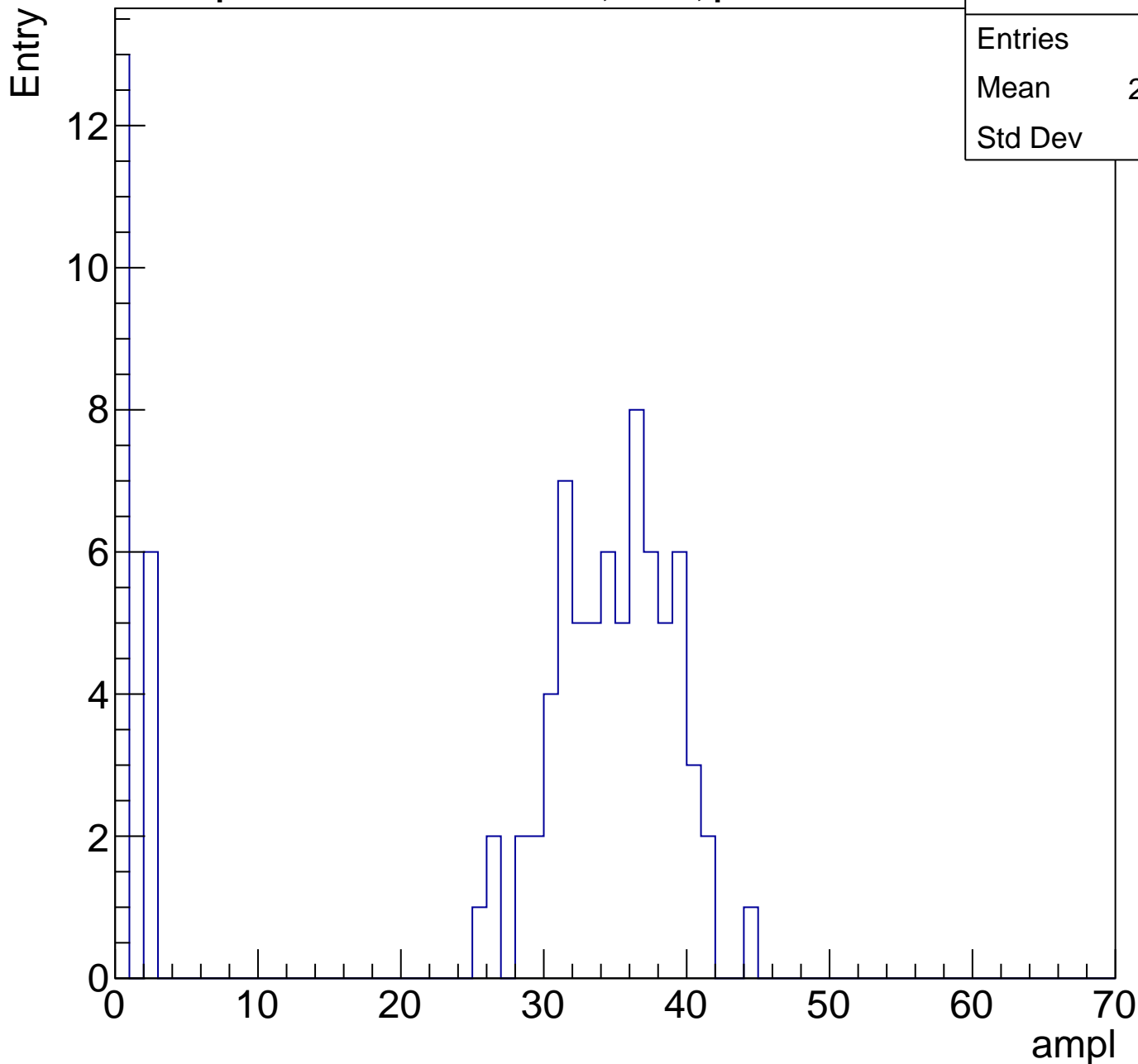
Entries	130
Mean	15.4
Std Dev	13.52



B1L103S, U9-ch82, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	27.24
Std Dev	14.3

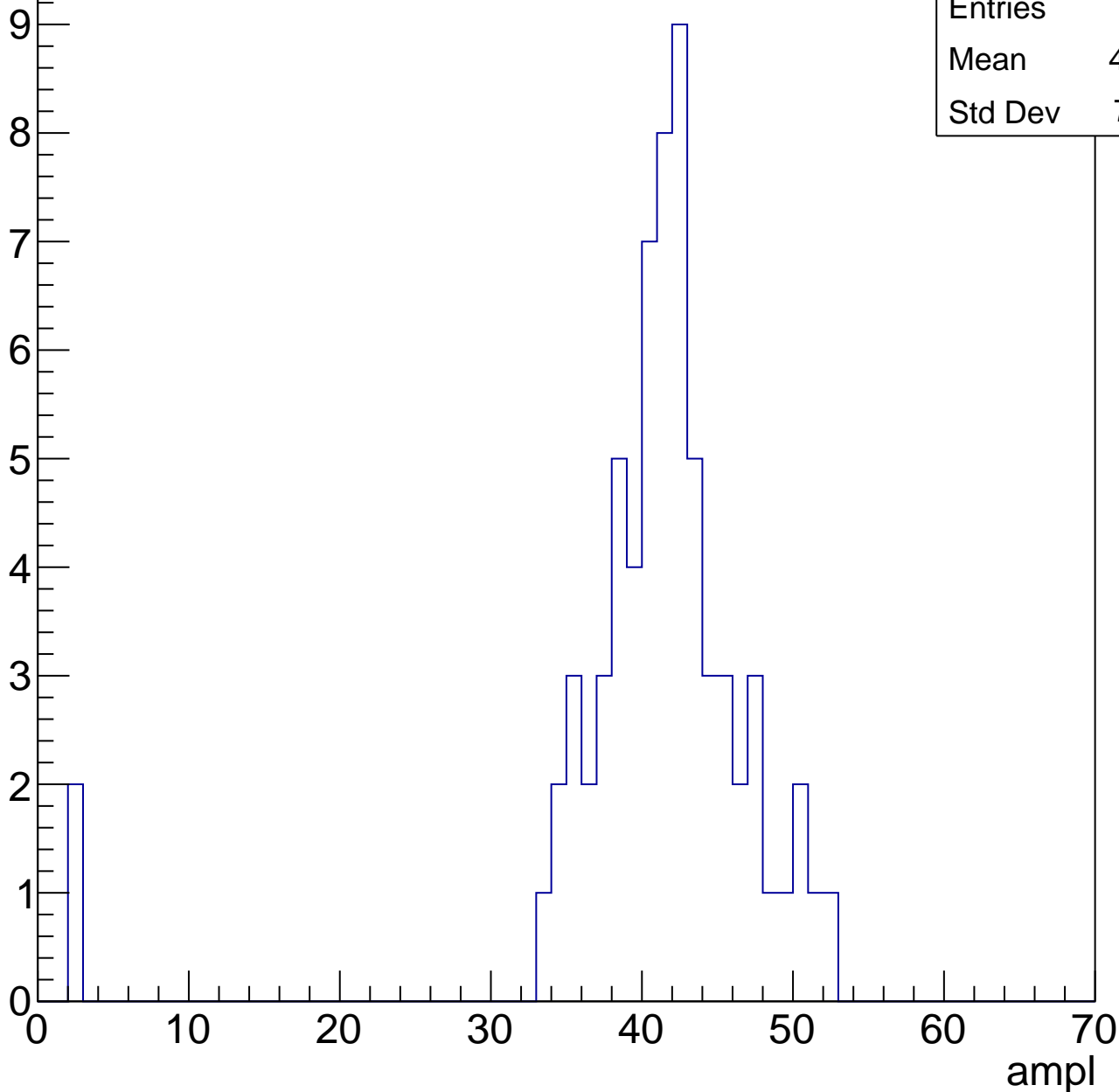


B1L103S, U9-ch82, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	40.29
Std Dev	7.861

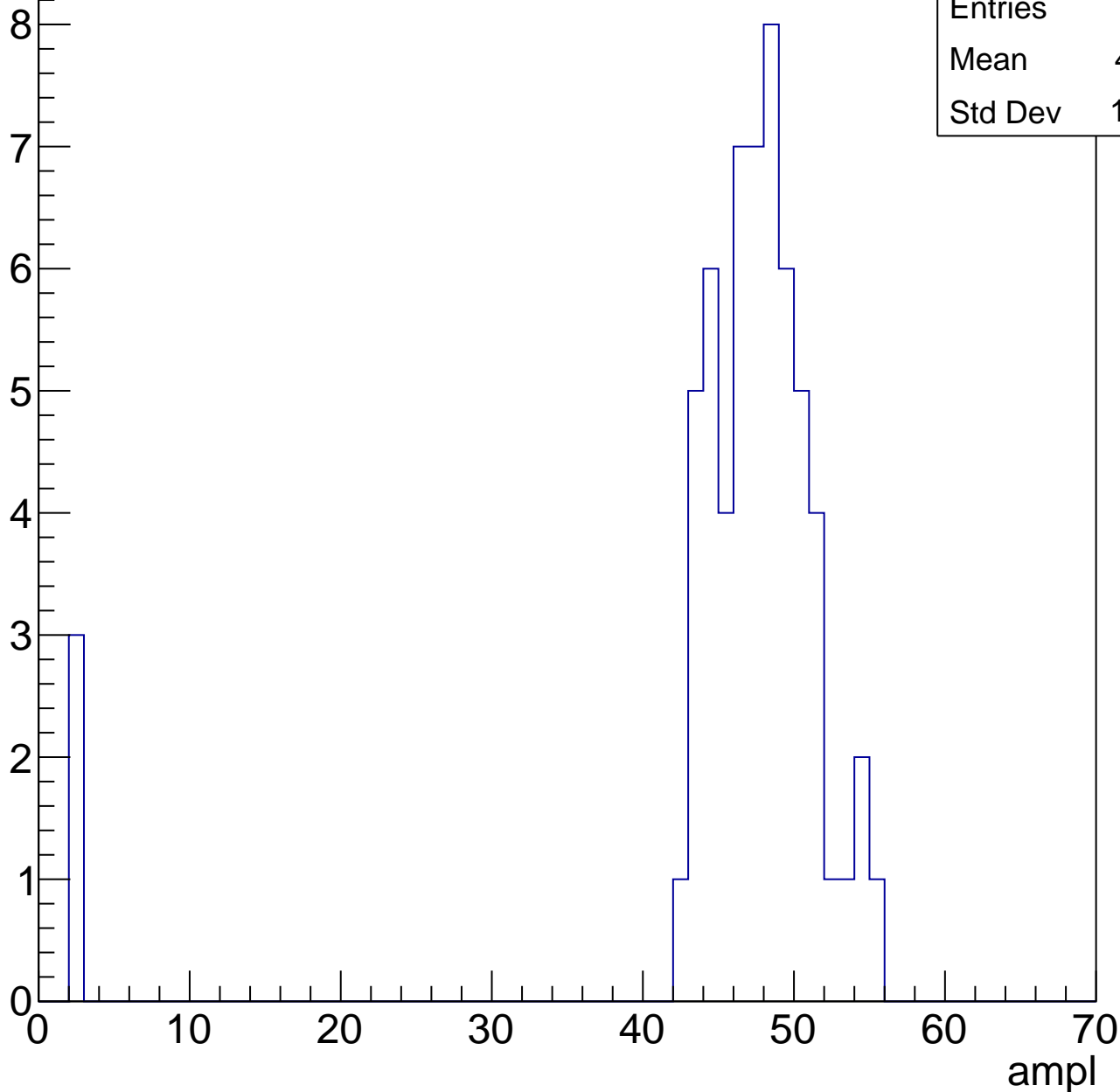


B1L103S, U9-ch82, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	45.21
Std Dev	10.26

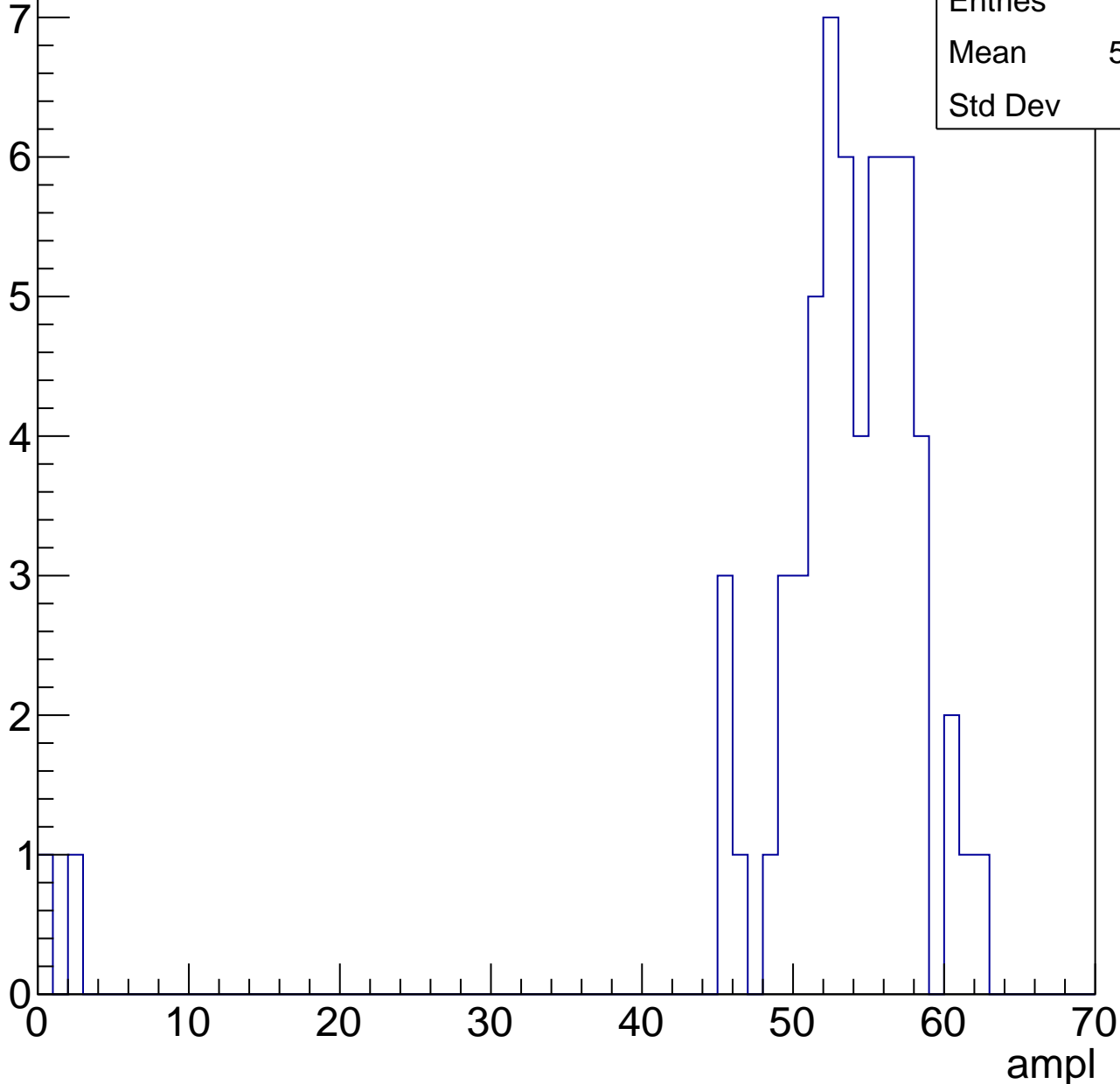


B1L103S, U9-ch82, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

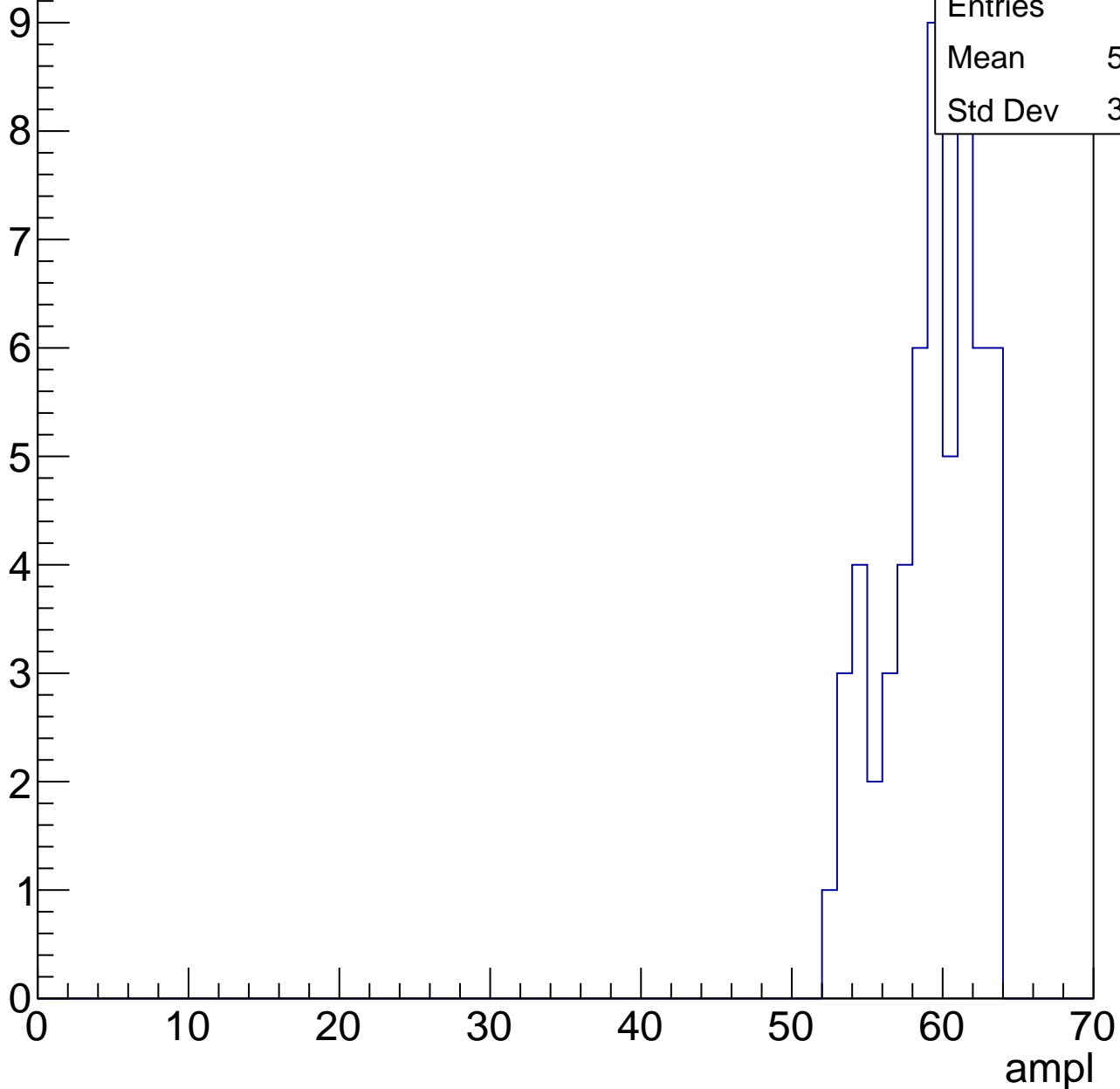
Entries	61
Mean	51.87
Std Dev	10.1



B1L103S, U9-ch82, adc5

calib_packv5_041523_1651.root, FC#0, port C2

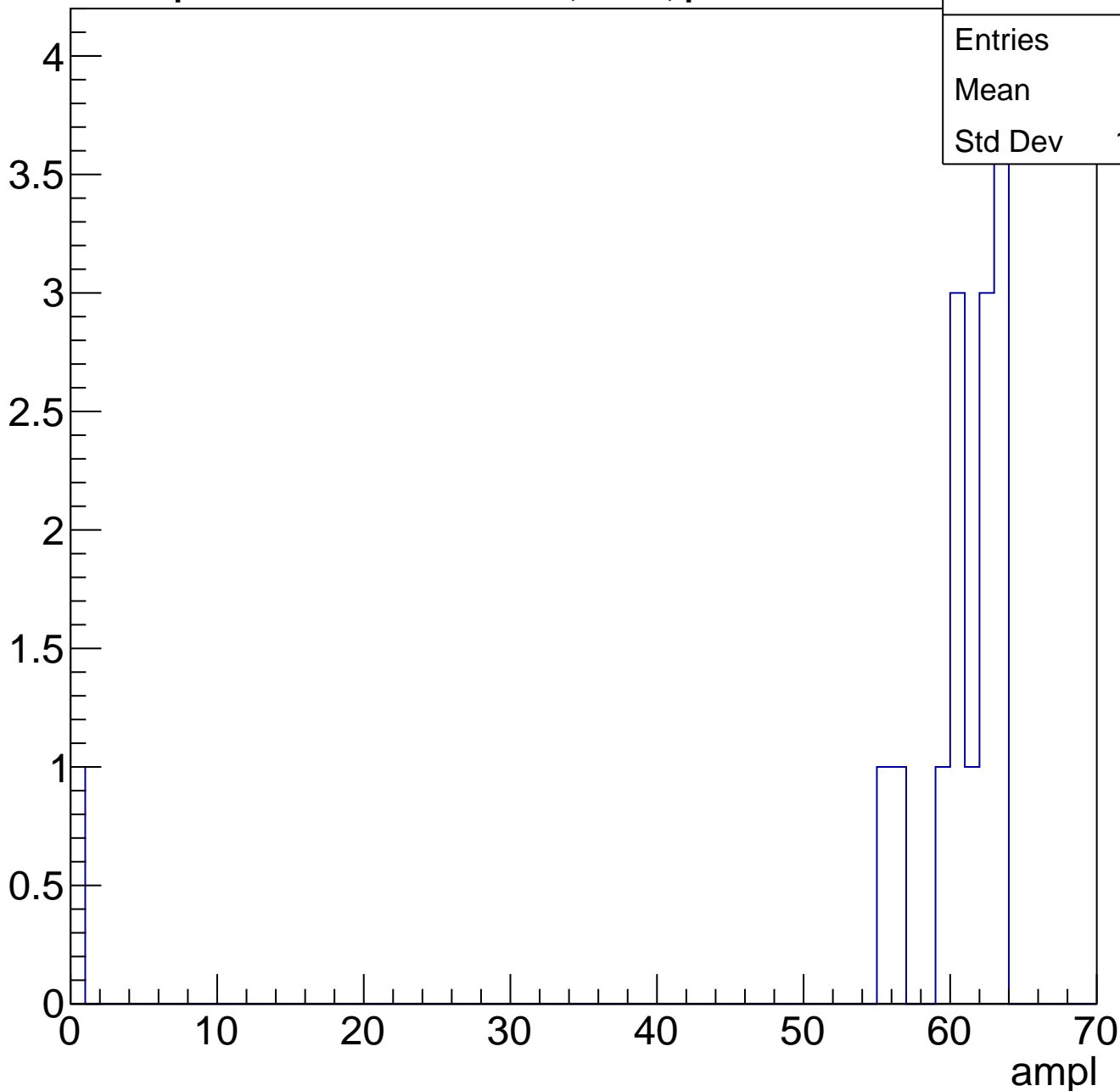
Entry



B1L103S, U9-ch82, adc6

calib_packv5_041523_1651.root, FC#0, port C2

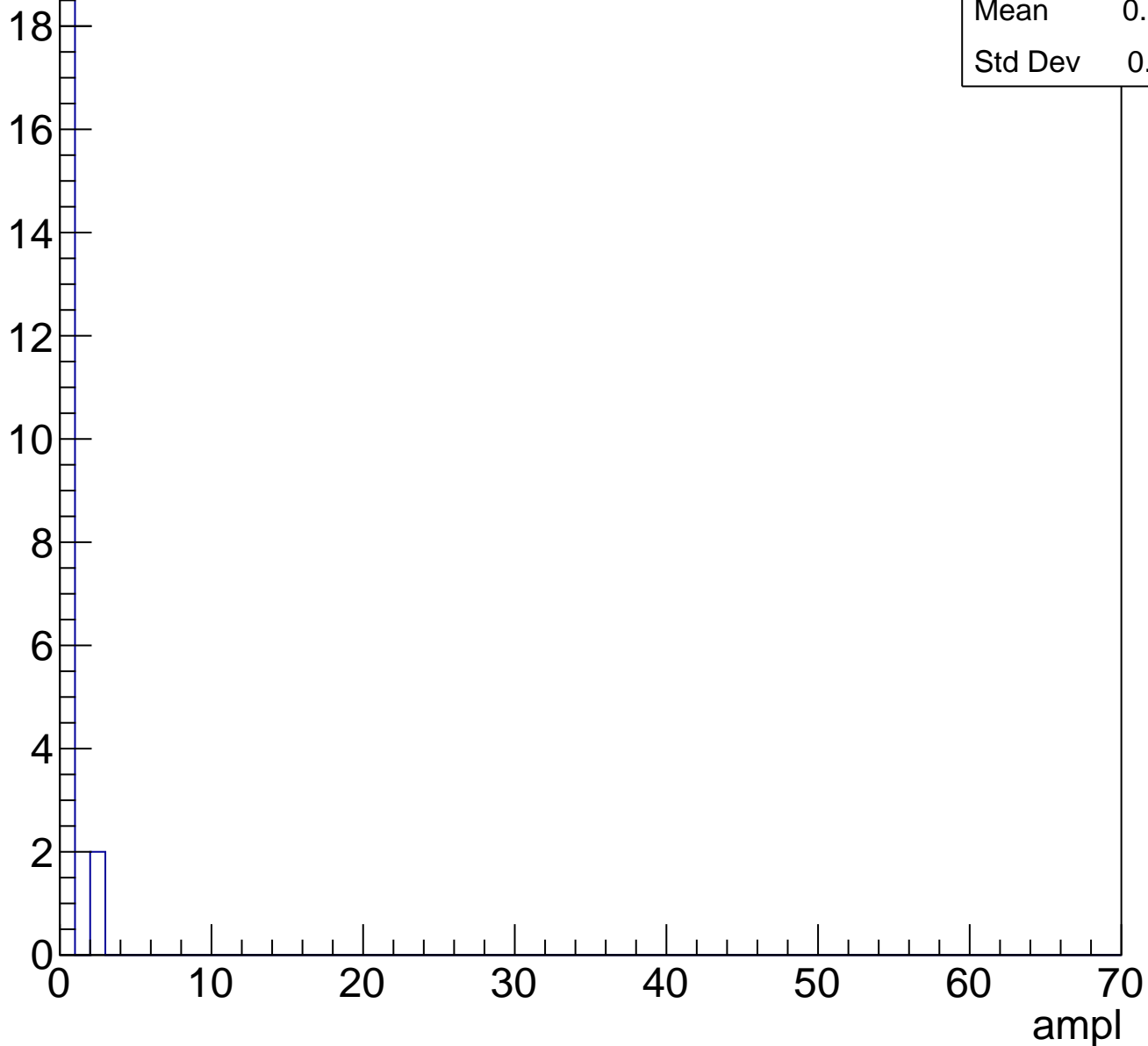
Entry



B1L103S, U9-ch82, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

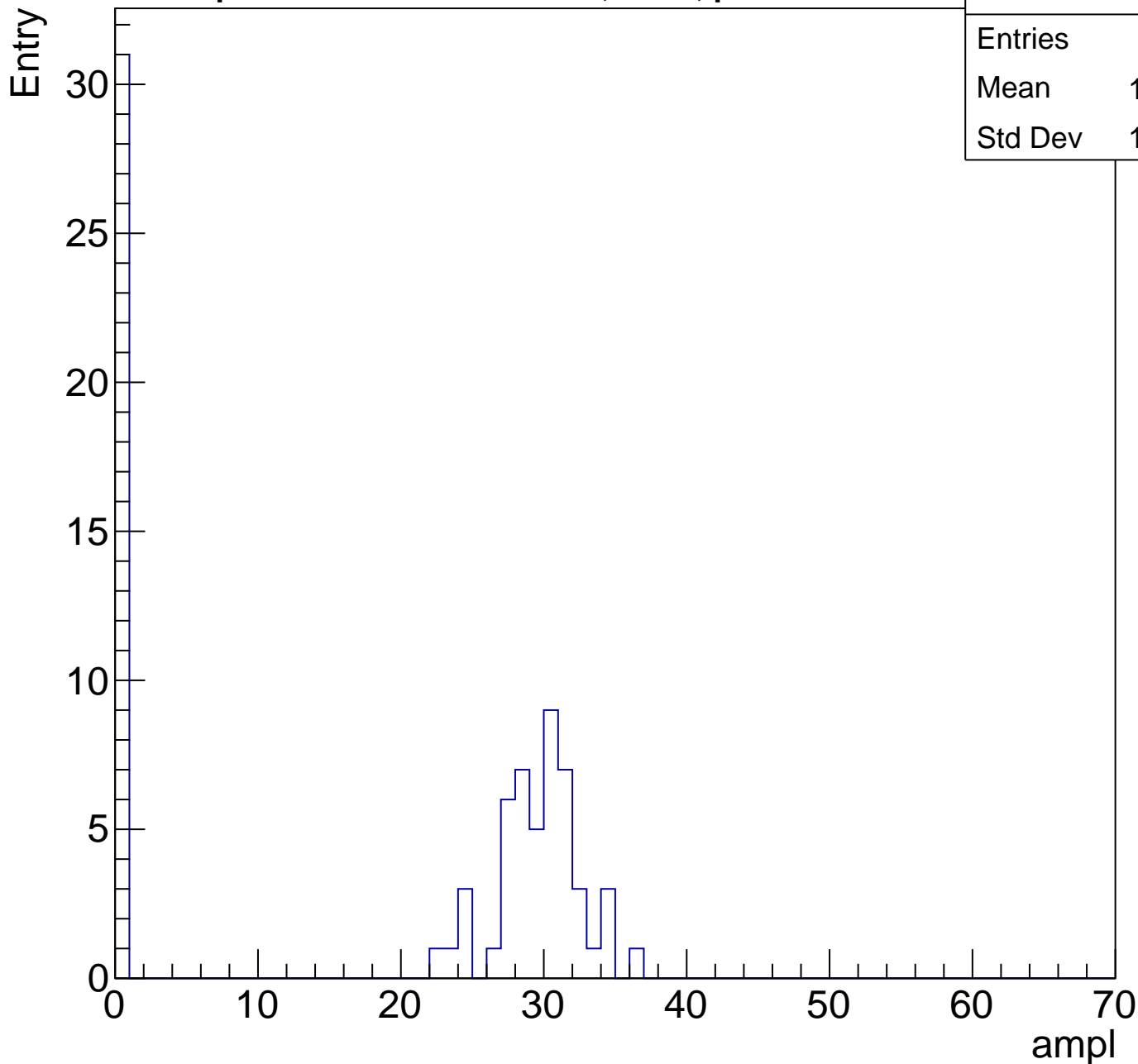


Entries	21
Mean	0.1905
Std Dev	0.5871

B1L103S, U9-ch83, adc0

calib_packv5_041523_1651.root, FC#0, port C2

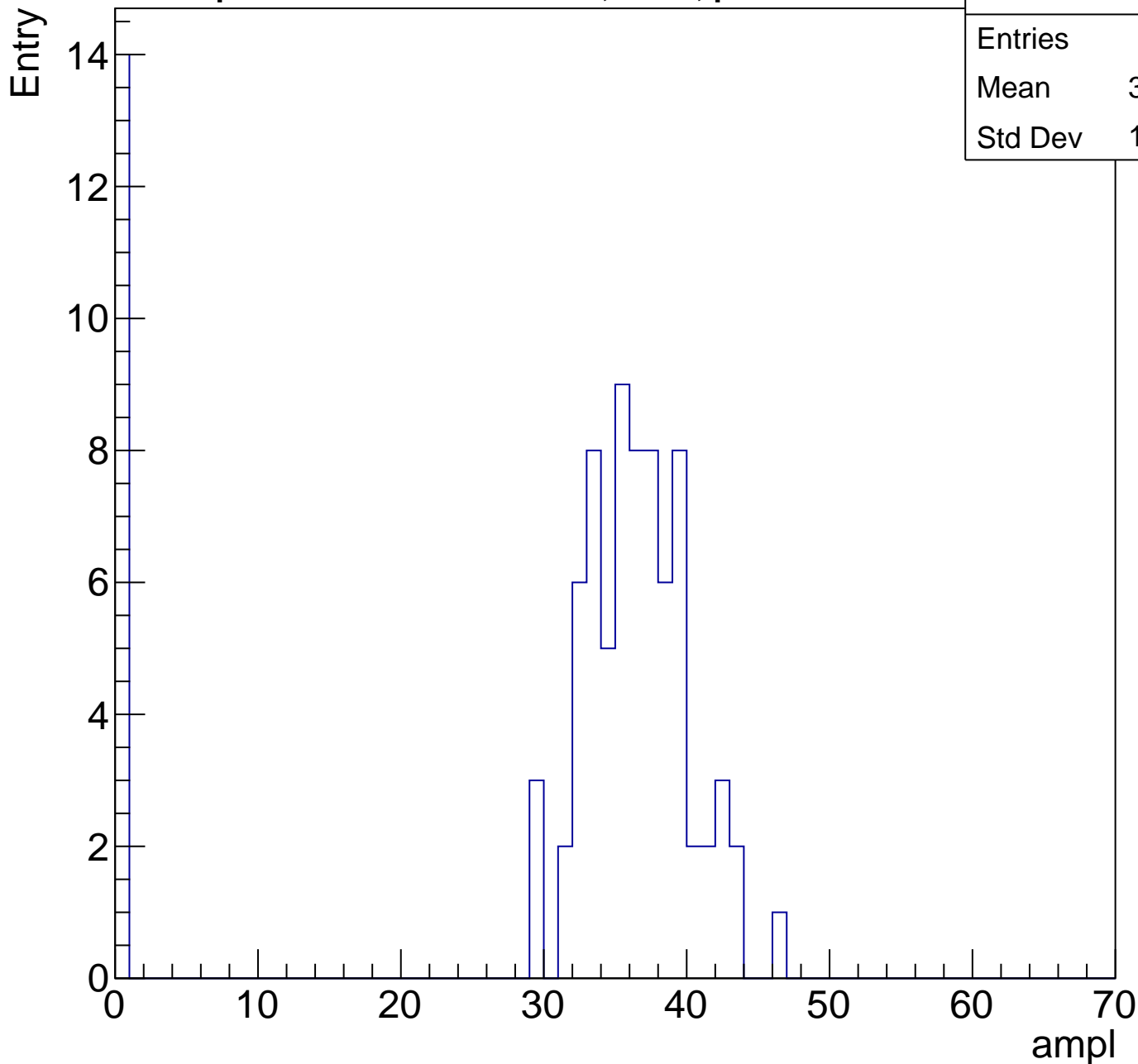
Entries	79
Mean	17.72
Std Dev	14.42



B1L103S, U9-ch83, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	87
Mean	30.28
Std Dev	13.64

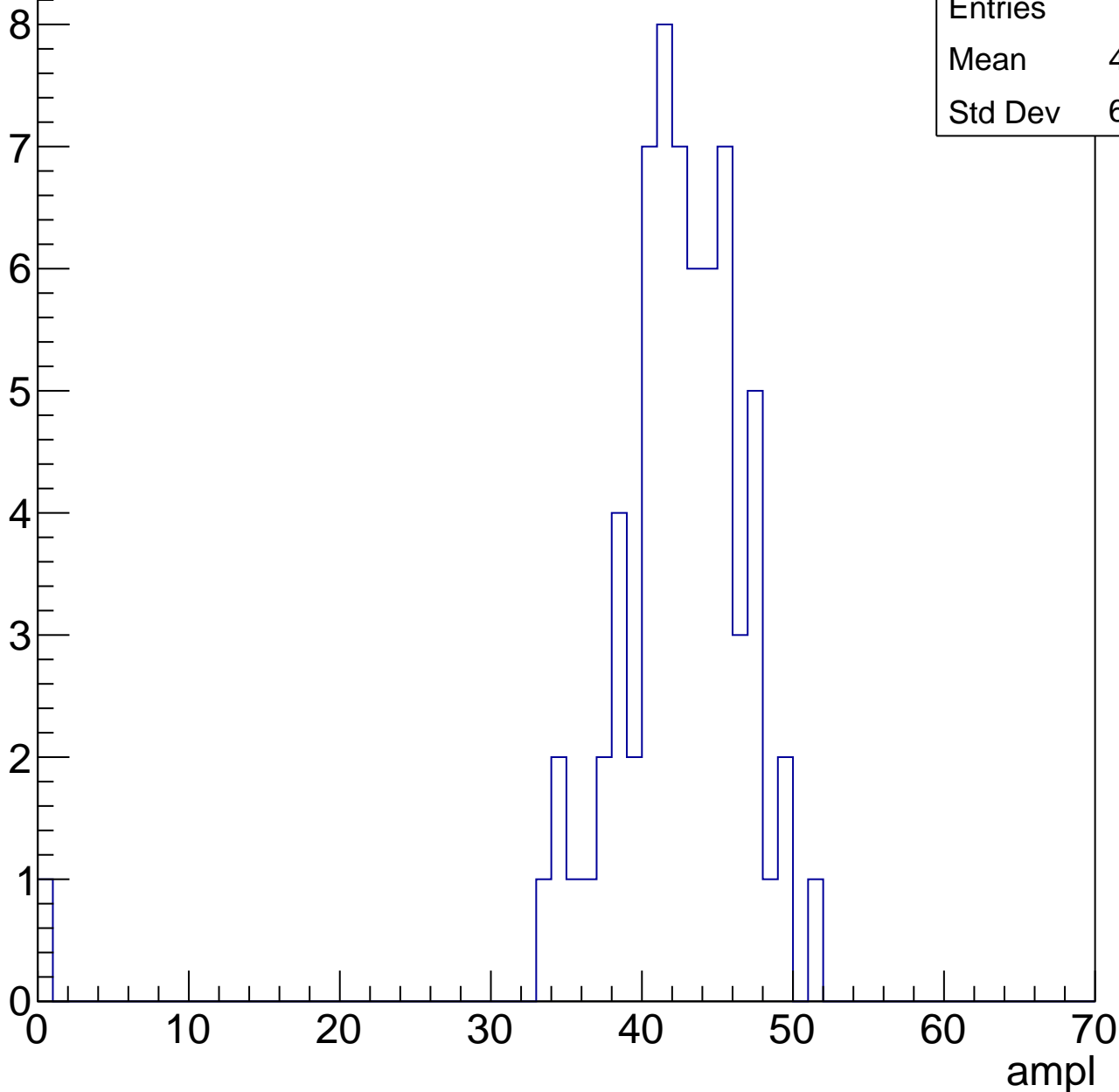


B1L103S, U9-ch83, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	41.57
Std Dev	6.342

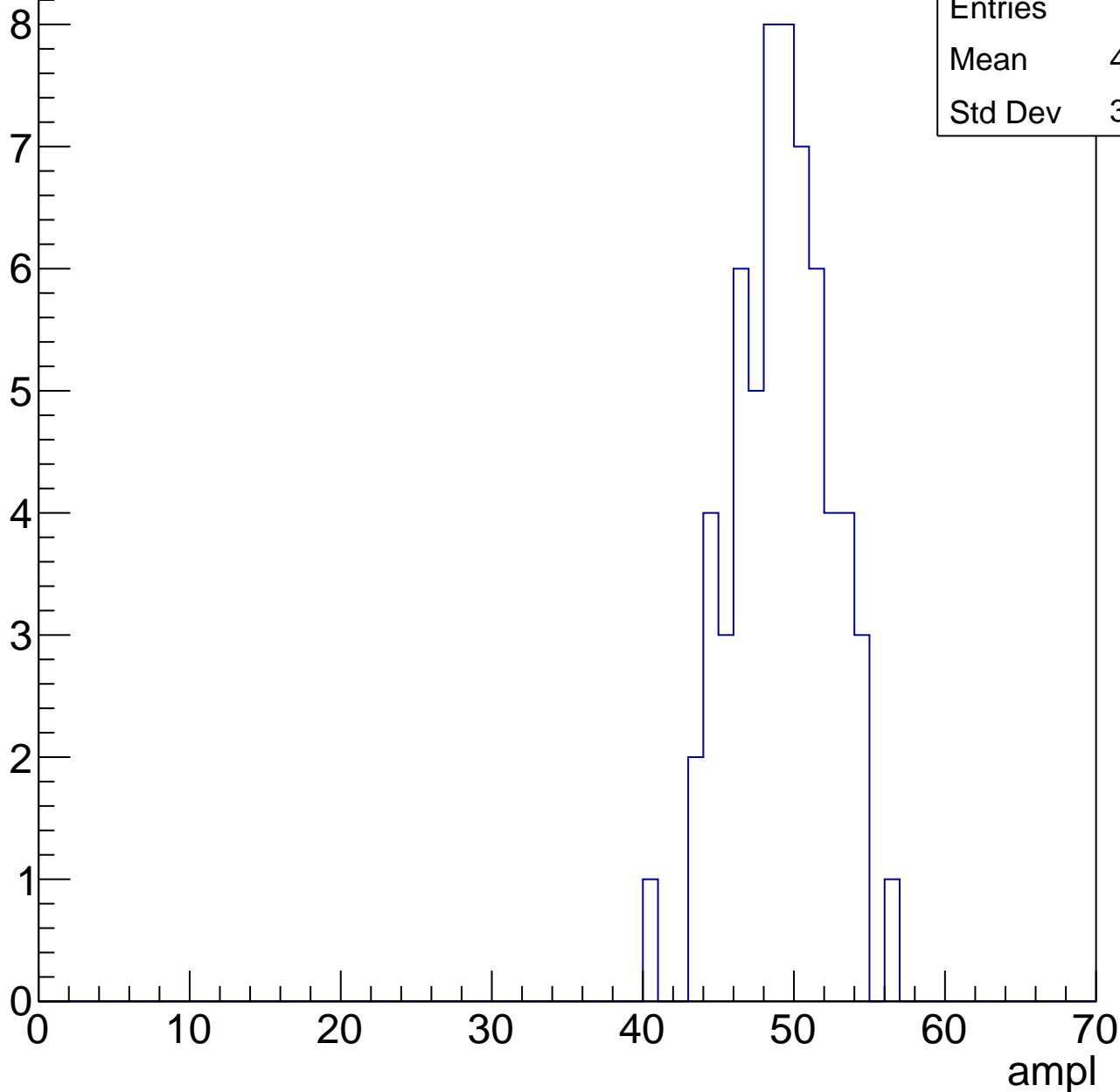


B1L103S, U9-ch83, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	48.68
Std Dev	3.192

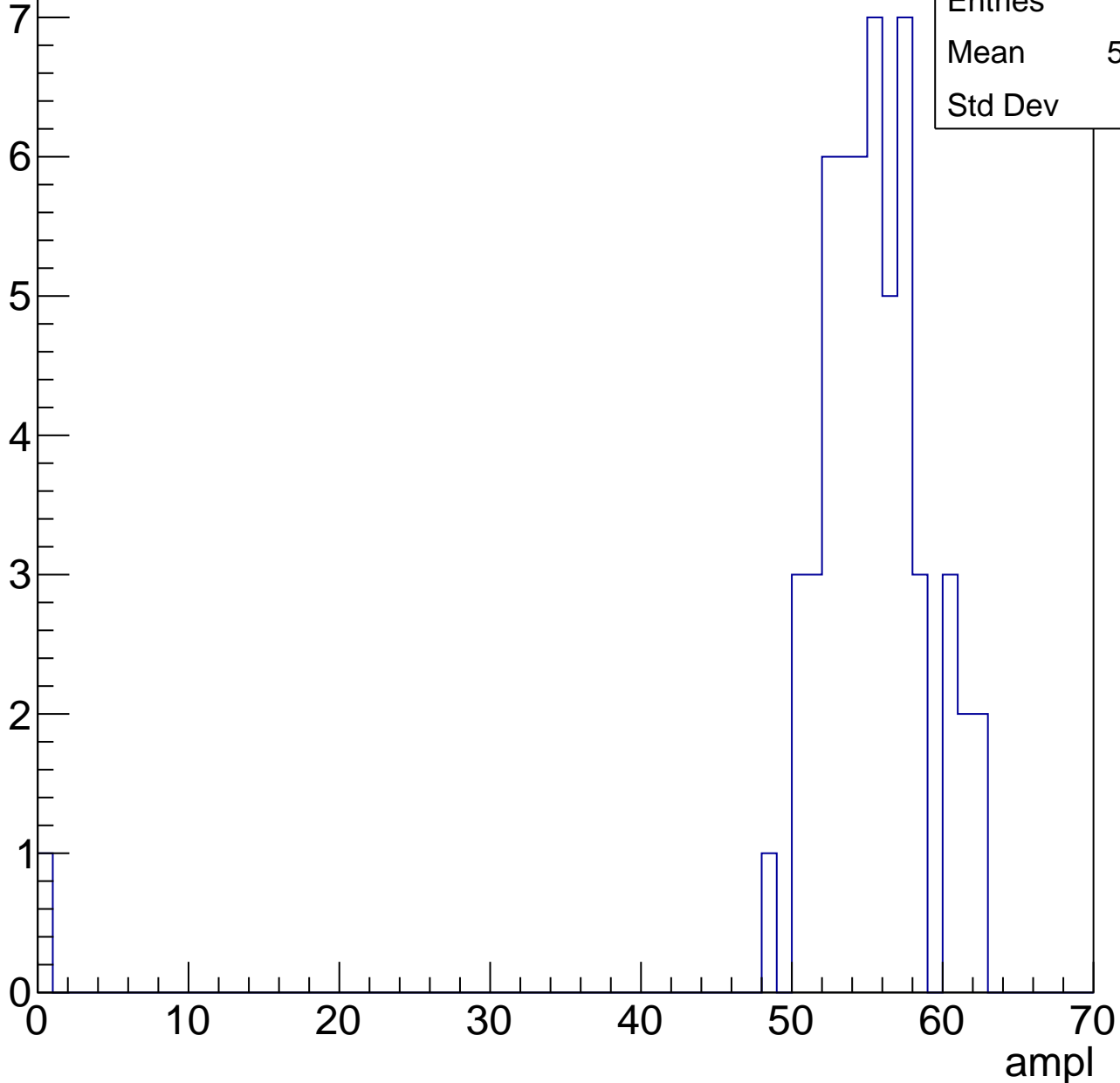


B1L103S, U9-ch83, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	53.98
Std Dev	8.01

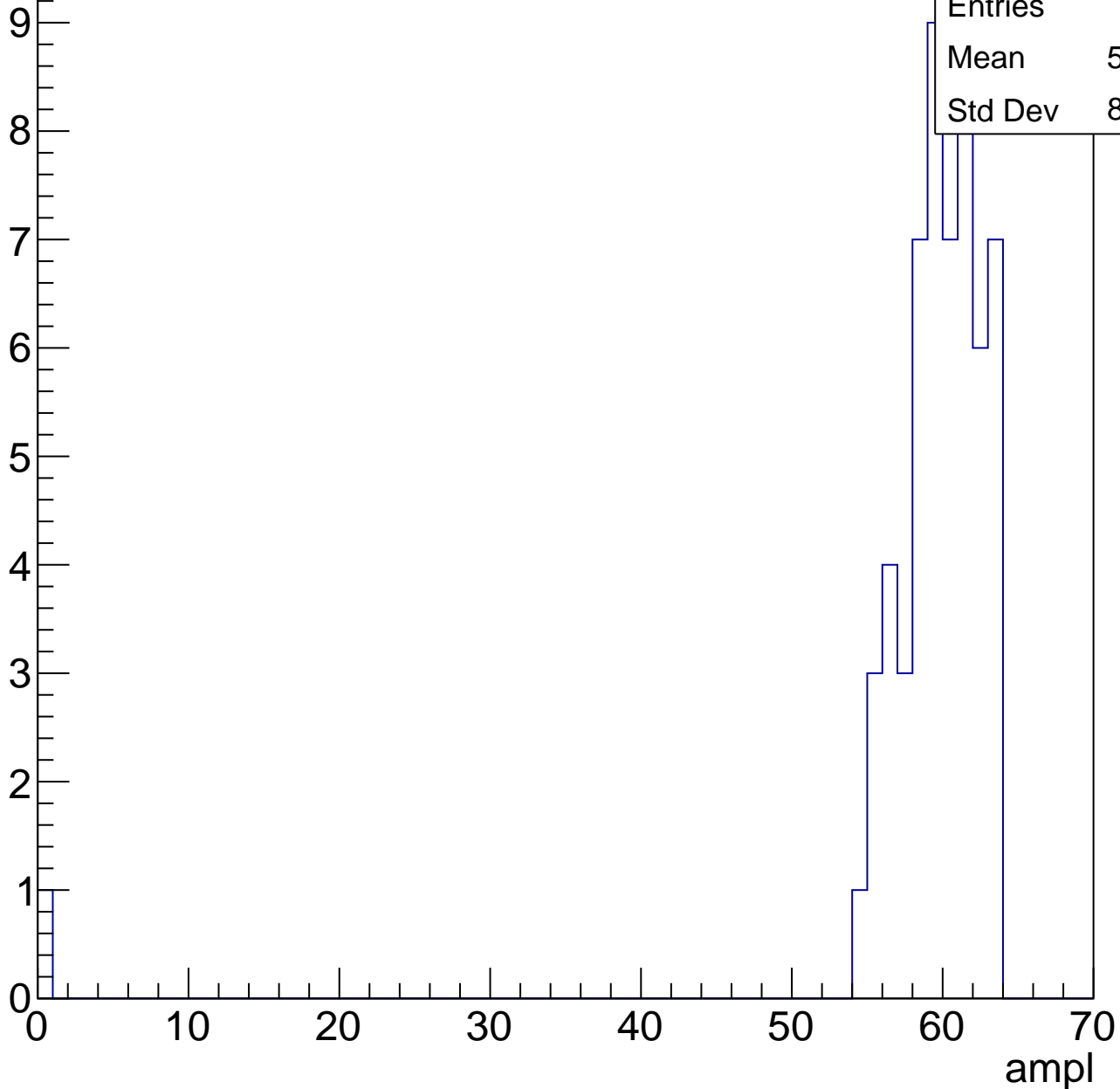


B1L103S, U9-ch83, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

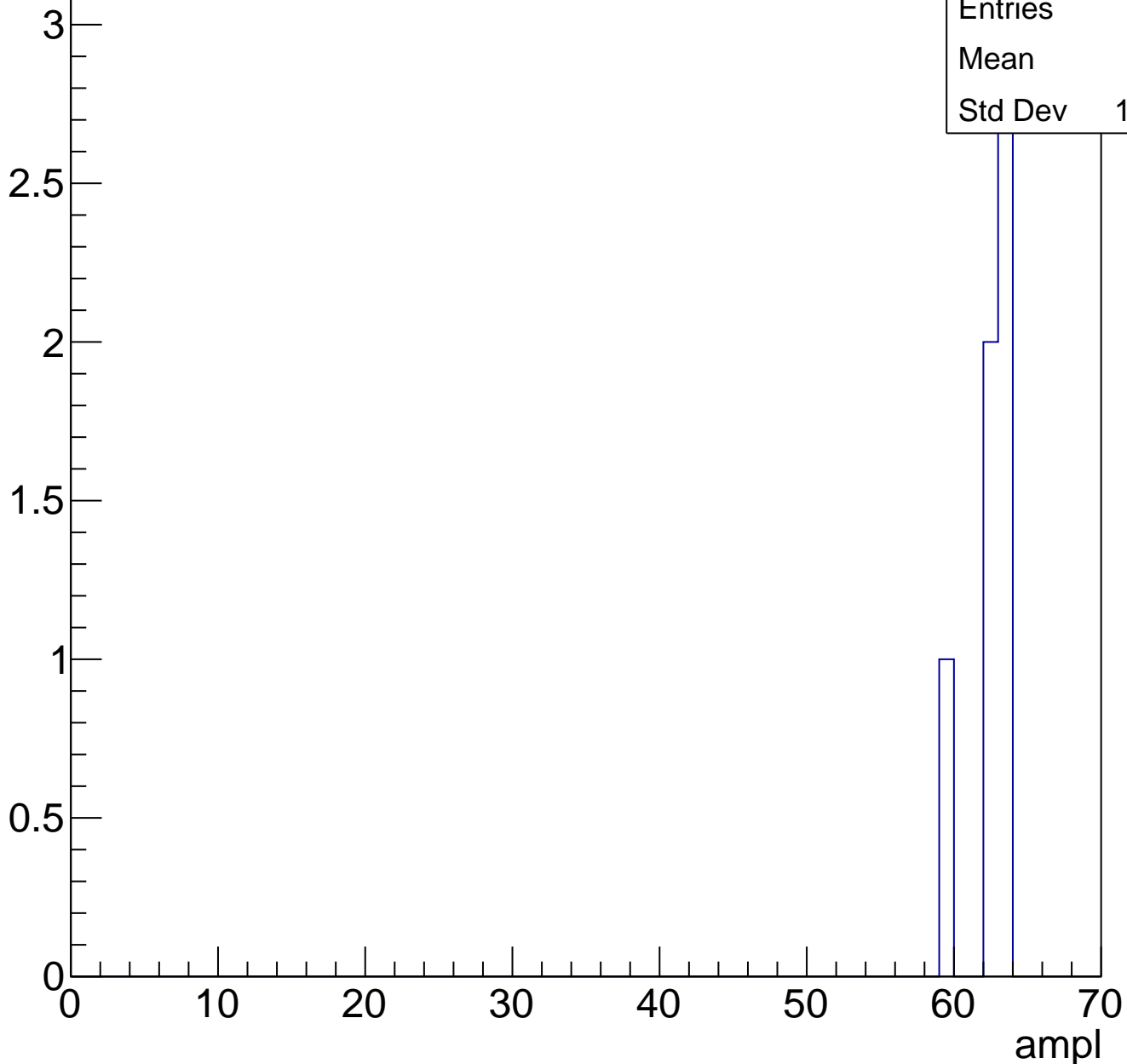
Entries	56
Mean	58.43
Std Dev	8.233



B1L103S, U9-ch83, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch83, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch84, adc0

calib_packv5_041523_1651.root, FC#0, port C2

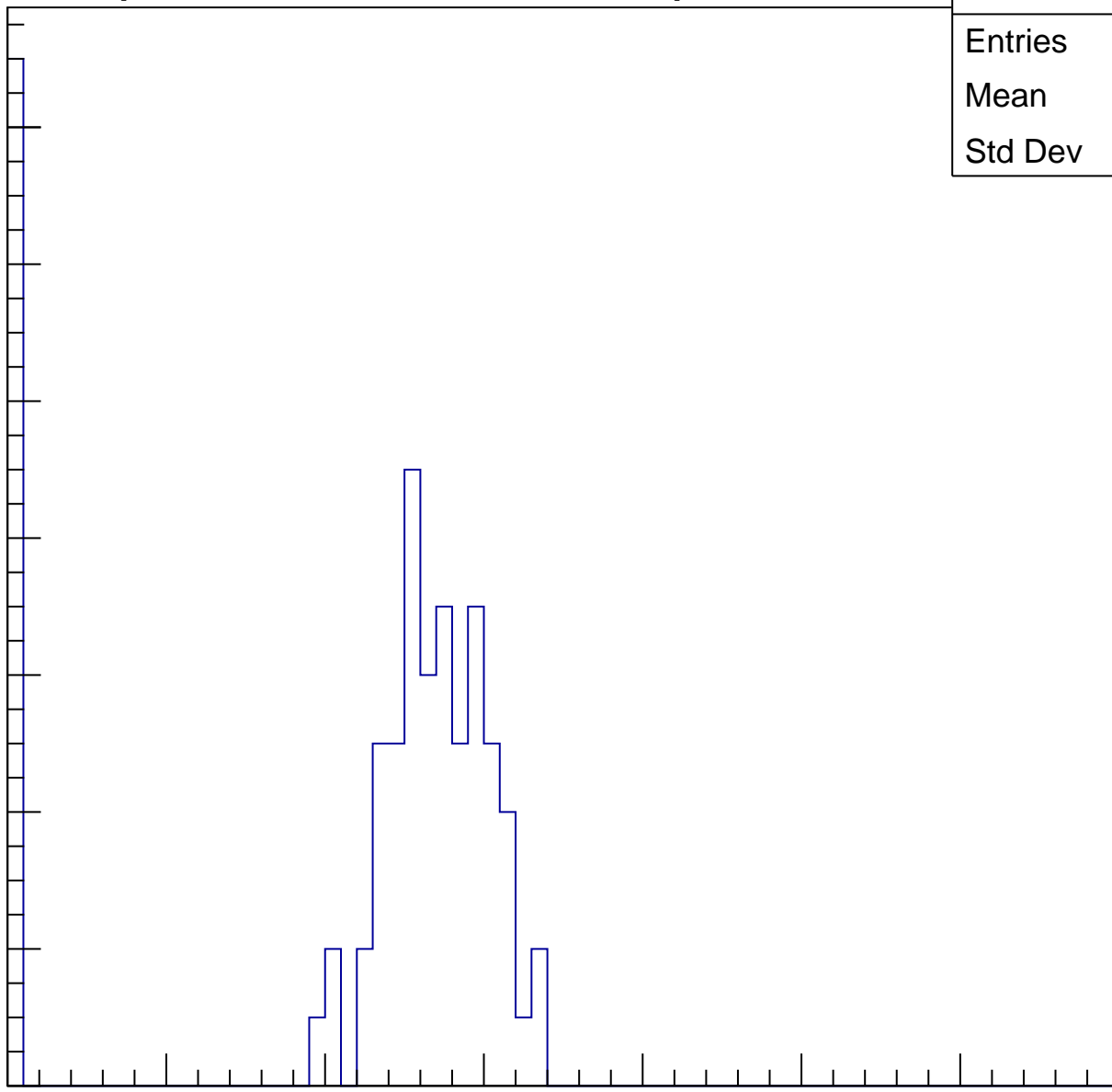
Entries	76
Mean	21.36
Std Dev	10.96

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

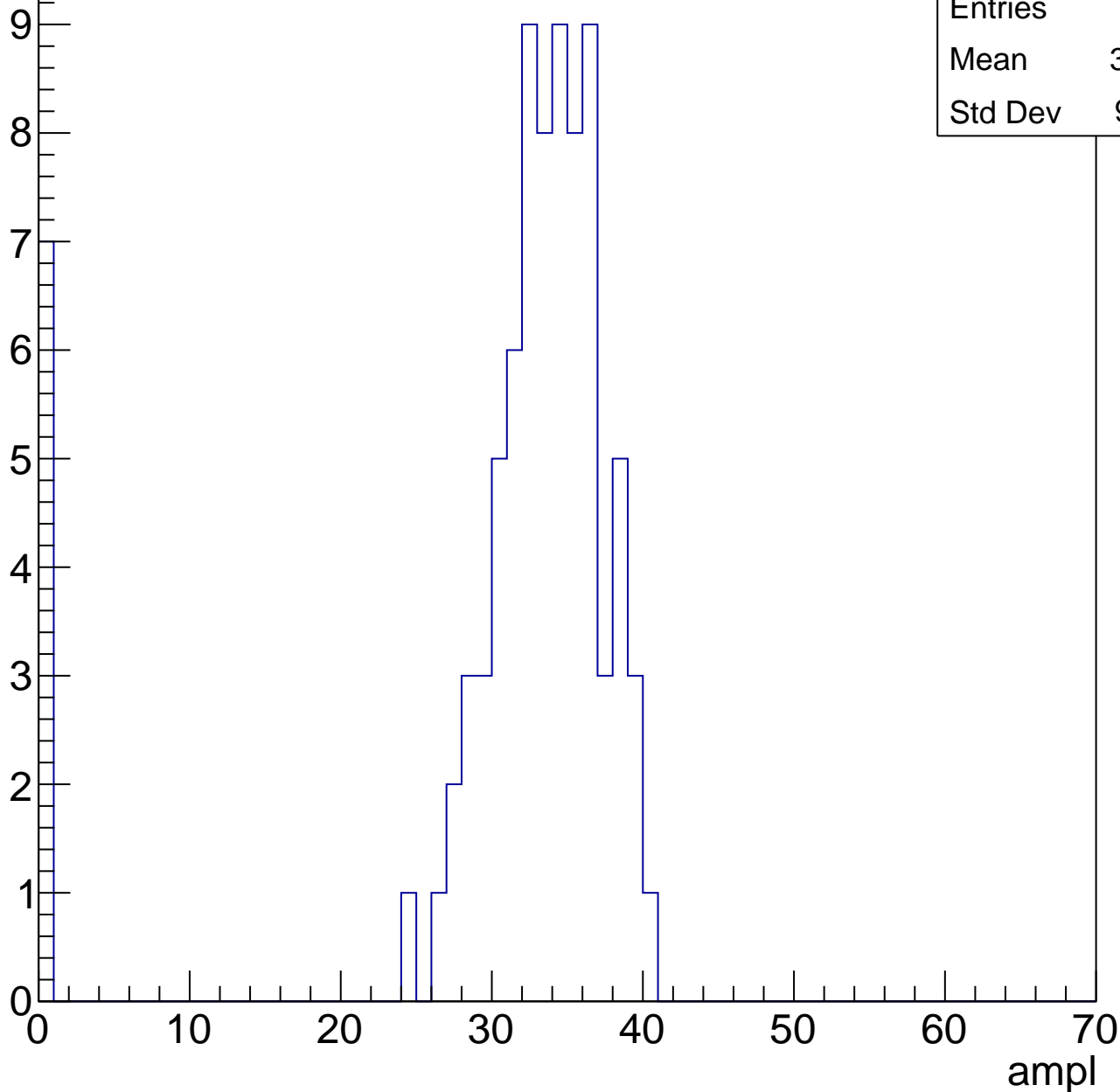


B1L103S, U9-ch84, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	83
Mean	30.49
Std Dev	9.791

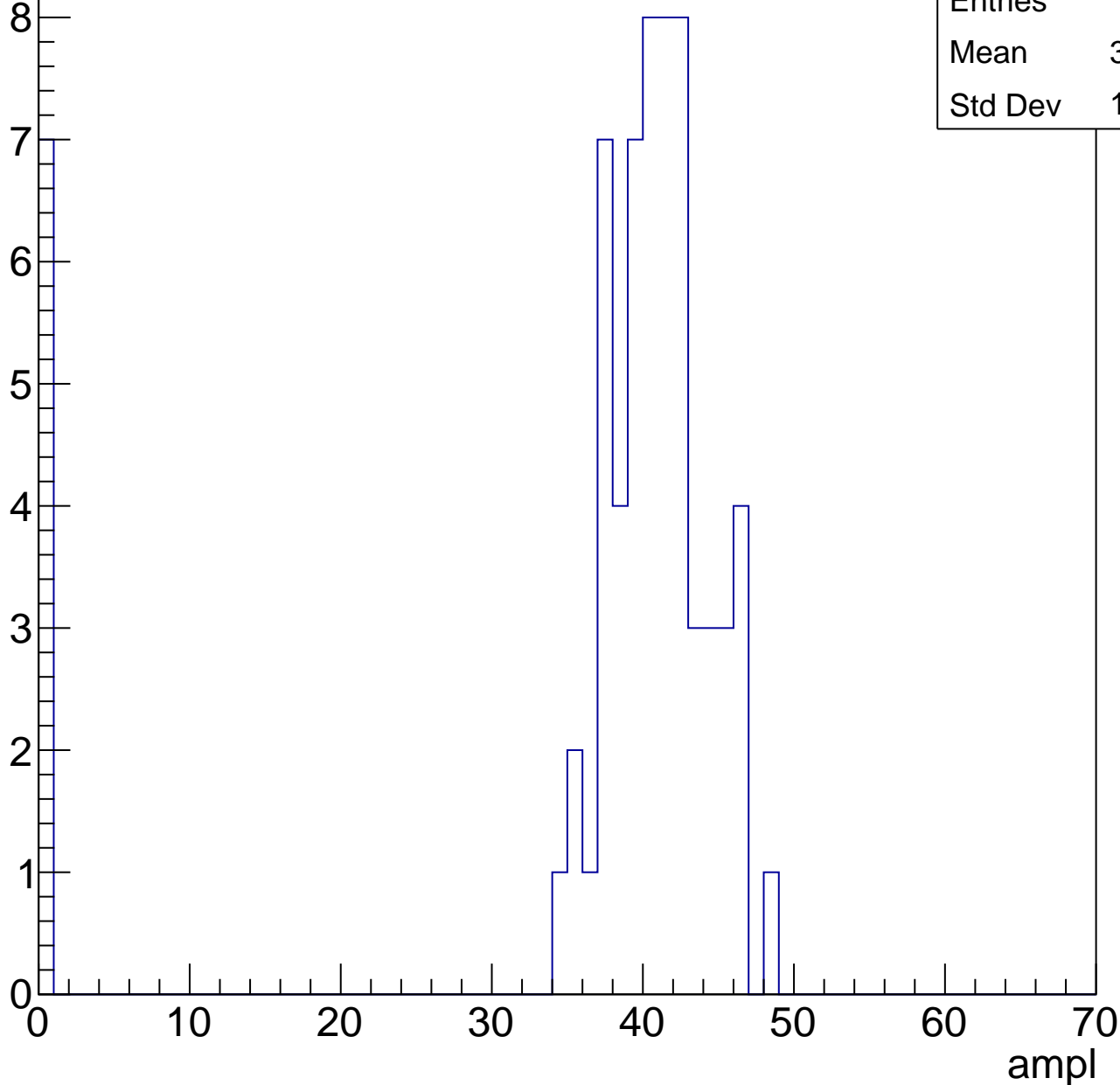


B1L103S, U9-ch84, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	36.36
Std Dev	12.75

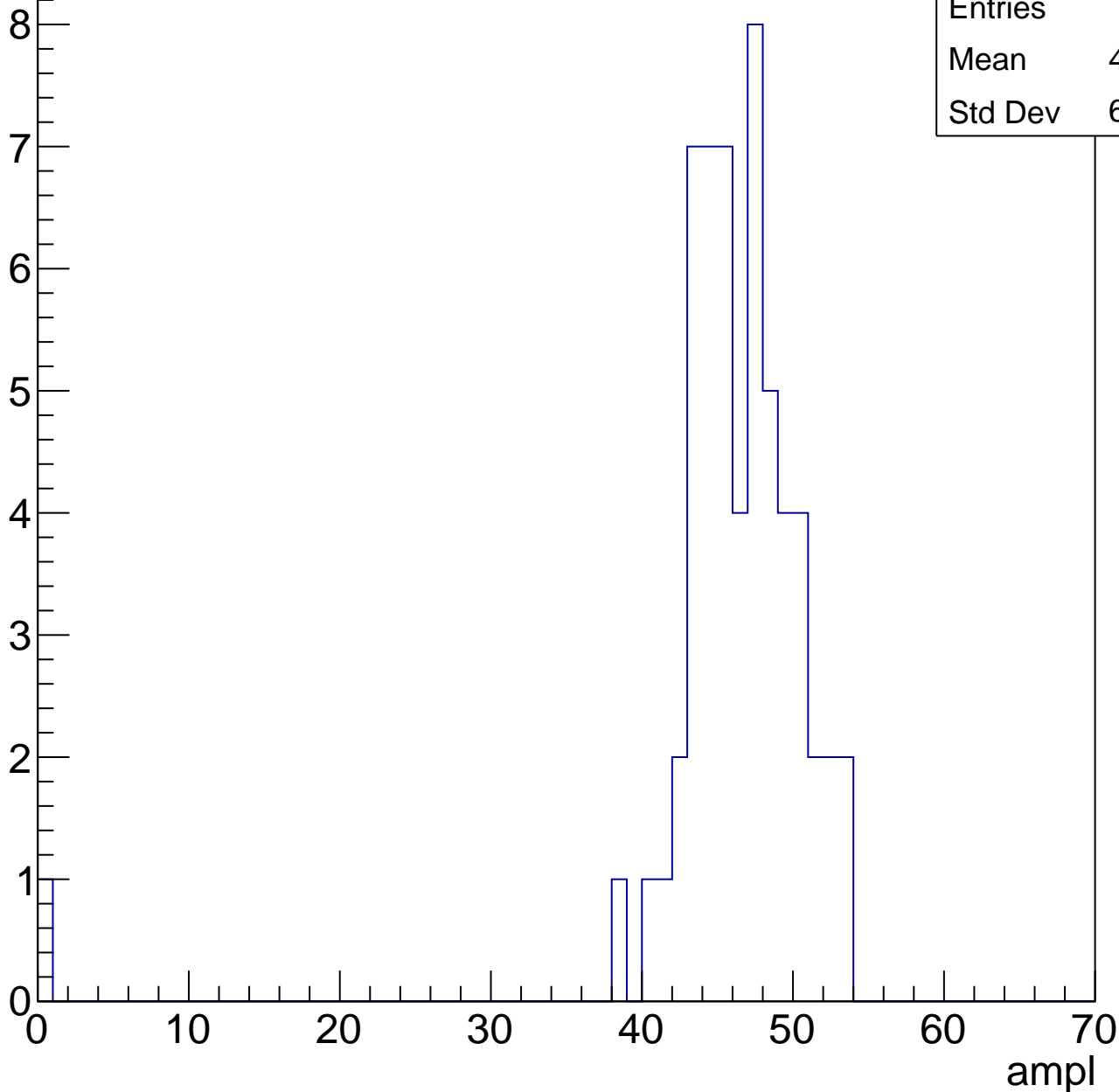


B1L103S, U9-ch84, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	45.43
Std Dev	6.823

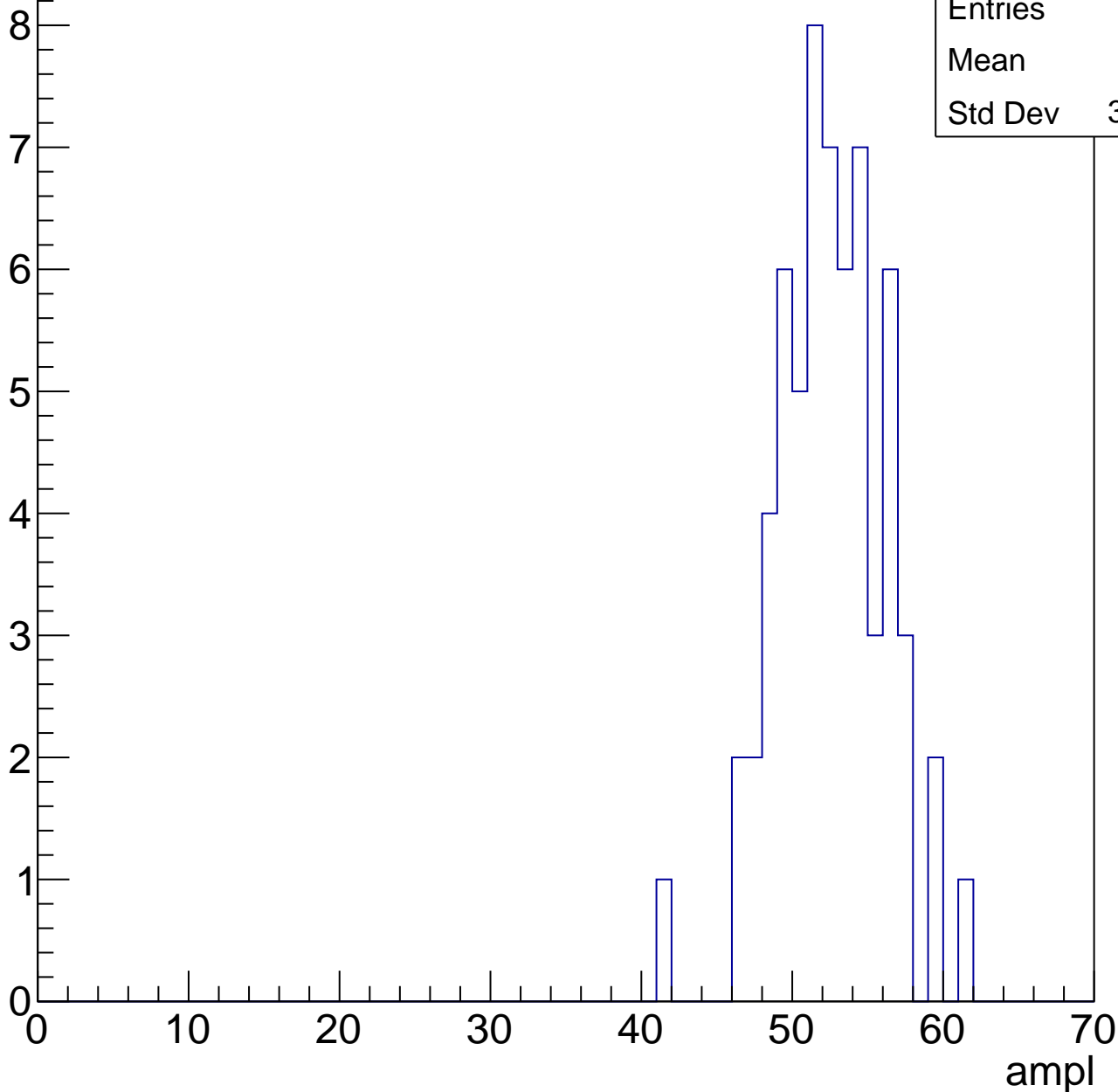


B1L103S, U9-ch84, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	52.1
Std Dev	3.562

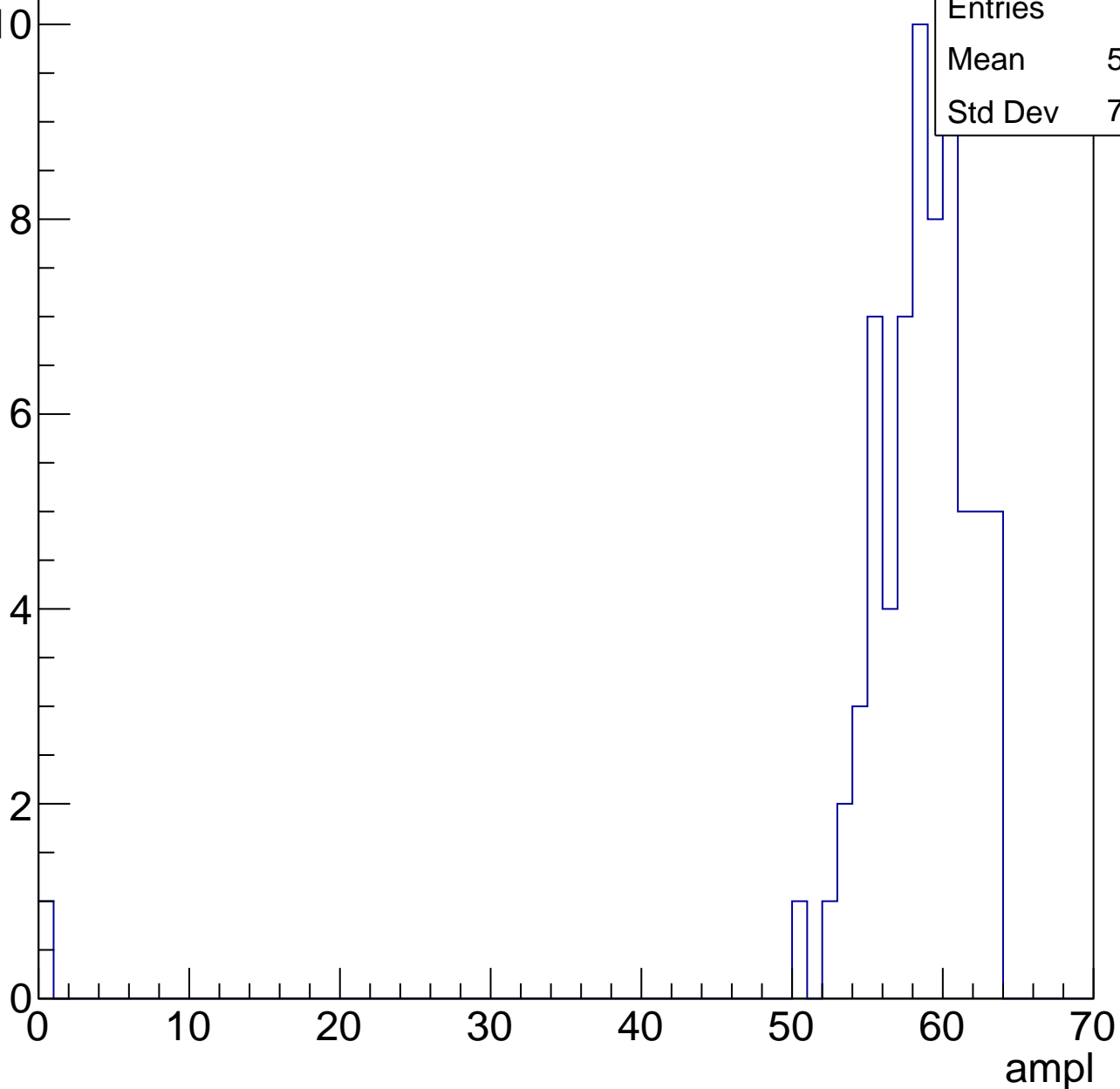


B1L103S, U9-ch84, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	57.35
Std Dev	7.586

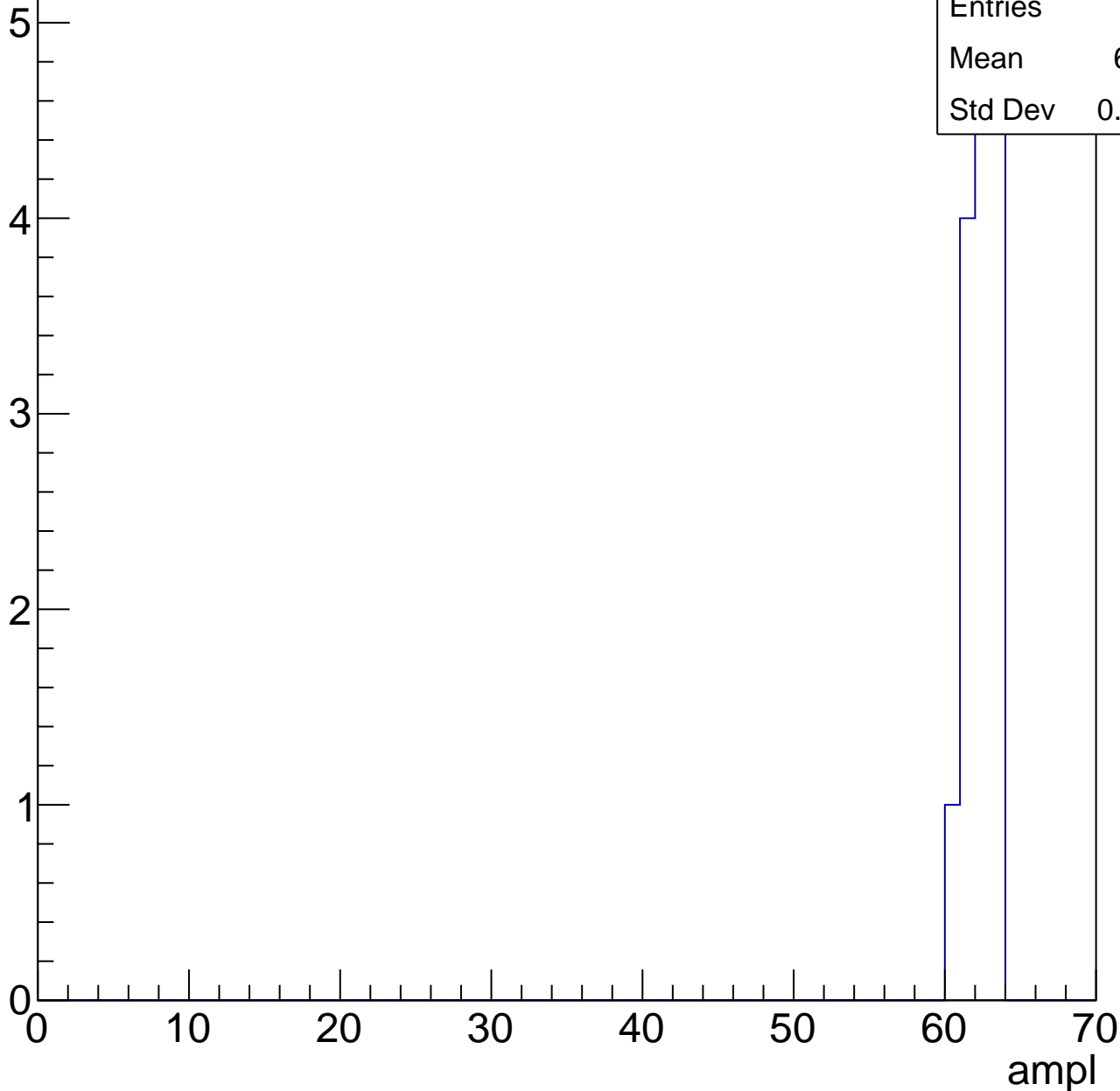


B1L103S, U9-ch84, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	15
Mean	61.93
Std Dev	0.9286



B1L103S, U9-ch84, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	18
Mean	0.9444
Std Dev	3.894

Entry

16
14
12
10
8
6
4
2
0

ampl

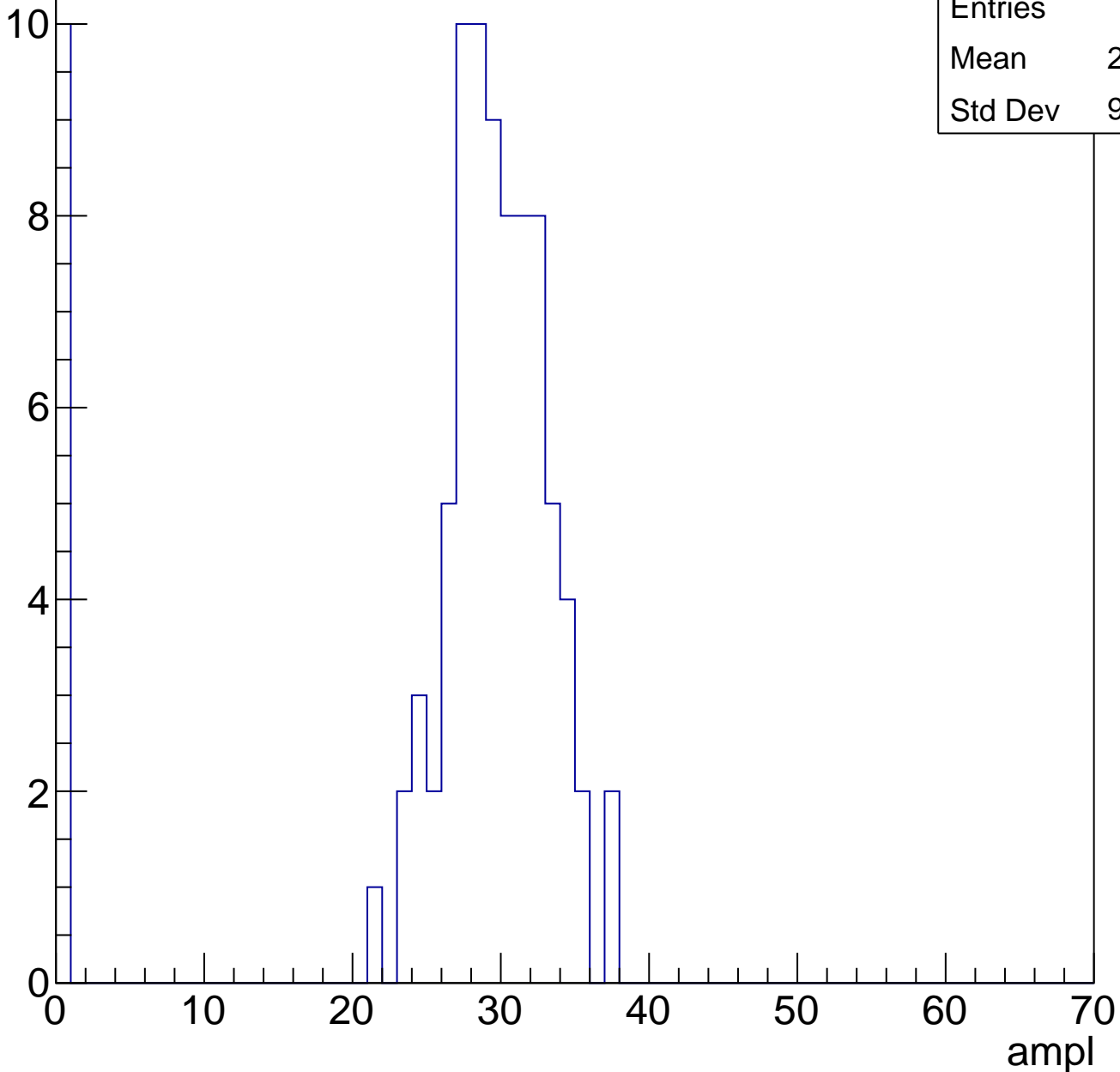
0 10 20 30 40 50 60 70

B1L103S, U9-ch85, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	26.06
Std Dev	9.755

Entry



B1L103S, U9-ch85, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	35.7
Std Dev	7.867

Entry

10

8

6

4

2

0

0

10

20

30

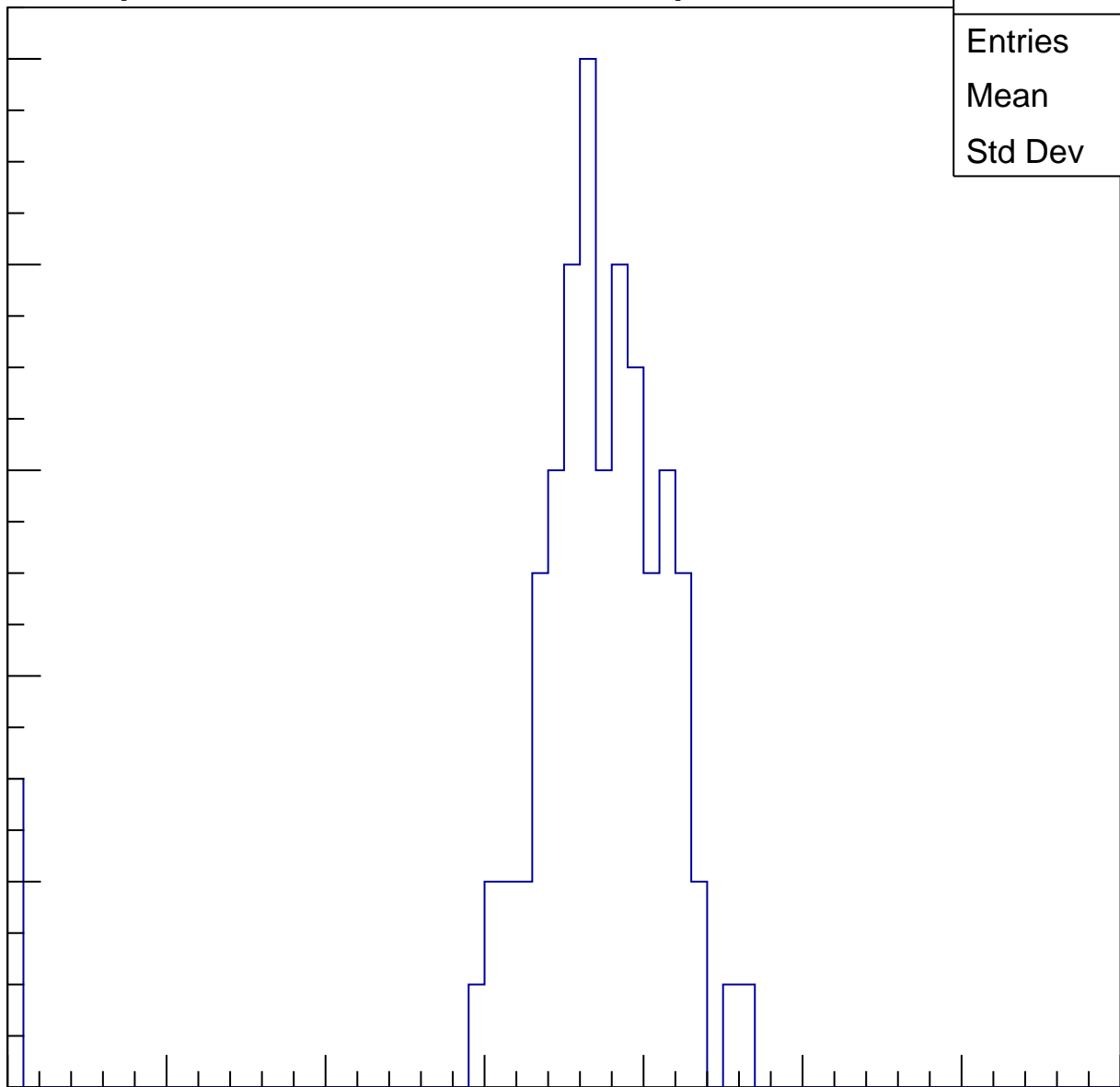
40

50

60

70

ampl

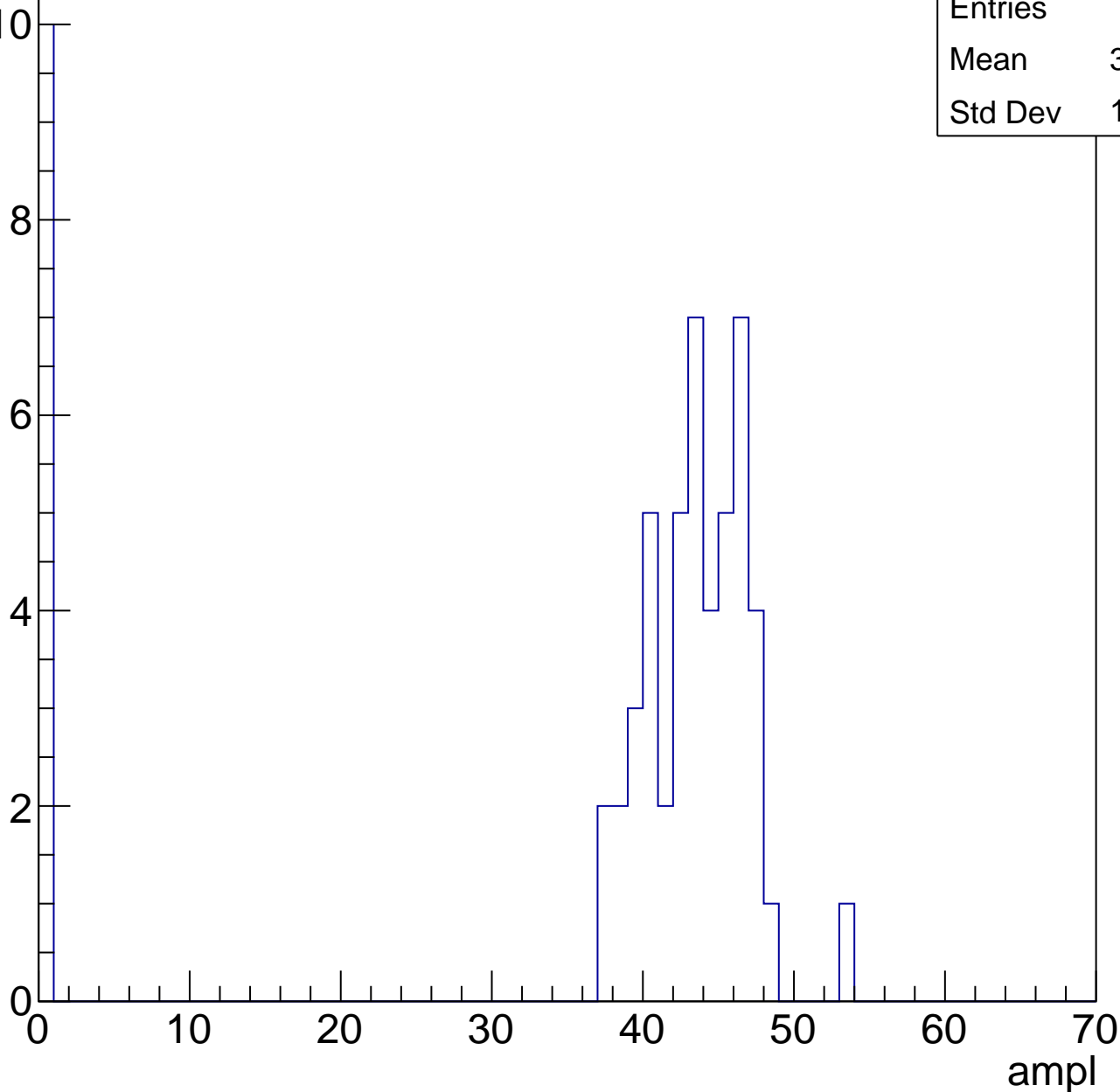


B1L103S, U9-ch85, adc2

calib_packv5_041523_1651.root, FC#0, port C2

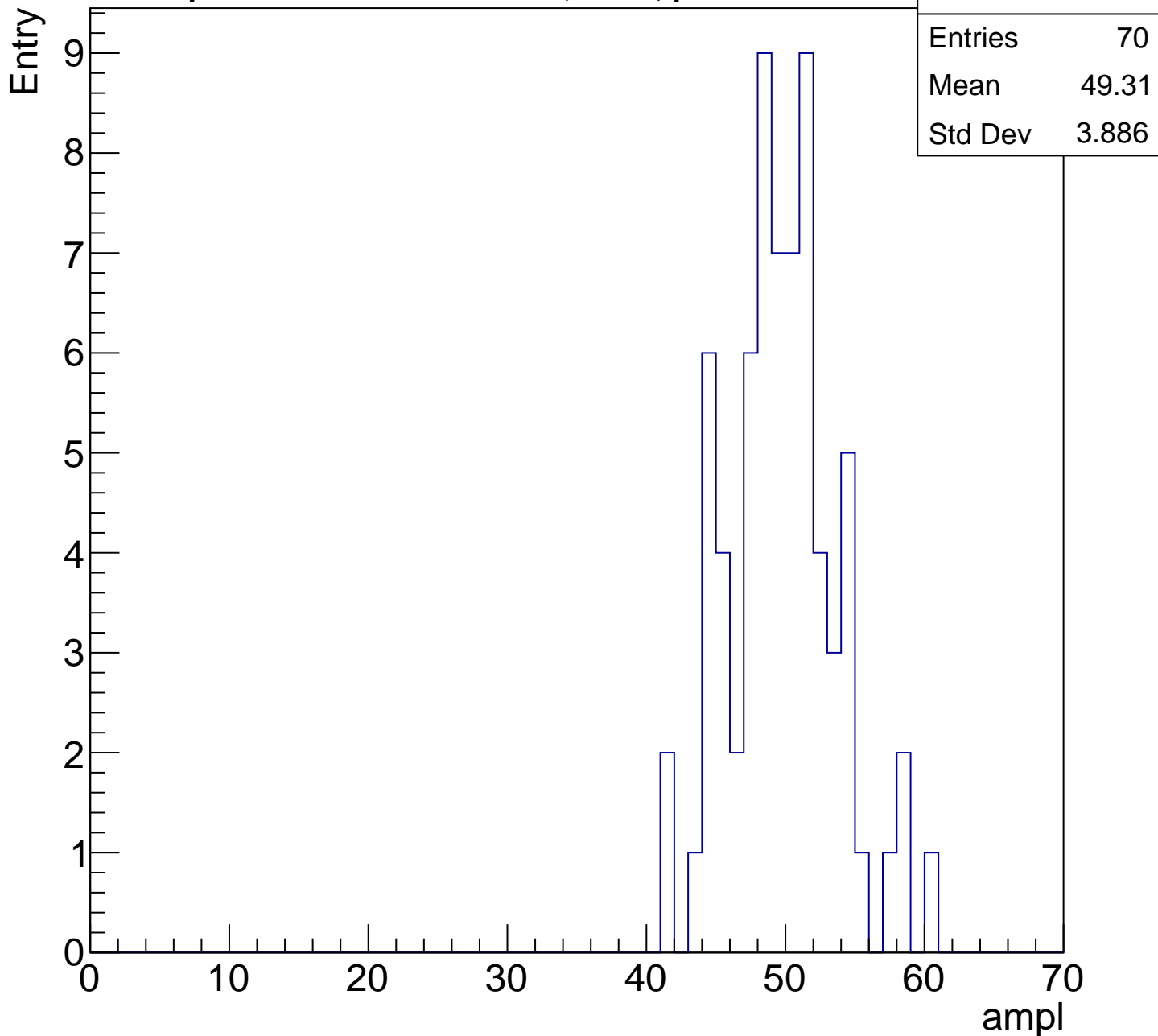
Entry

Entries	58
Mean	35.72
Std Dev	16.57



B1L103S, U9-ch85, adc3

calib_packv5_041523_1651.root, FC#0, port C2

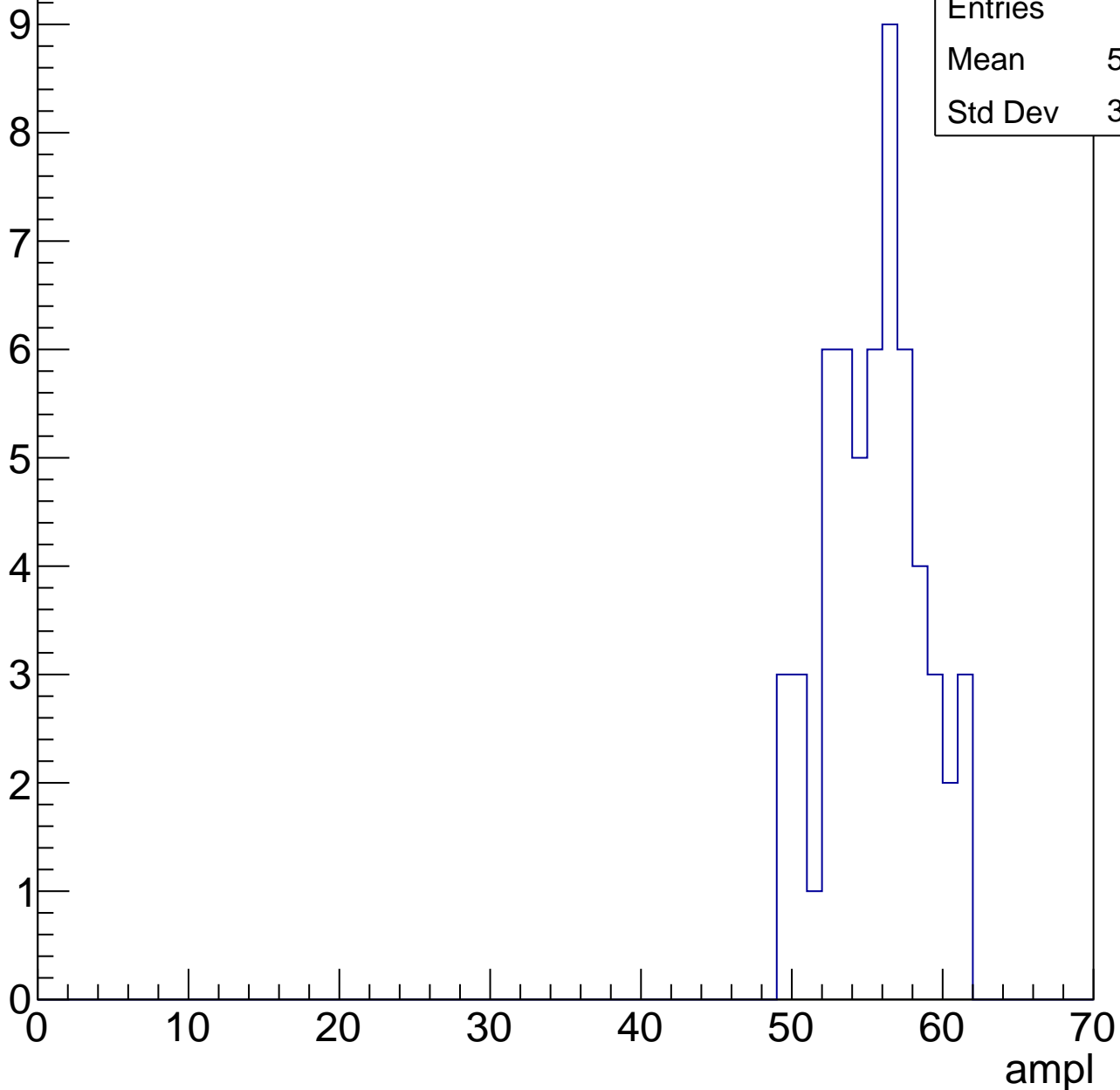


B1L103S, U9-ch85, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	55.02
Std Dev	3.126

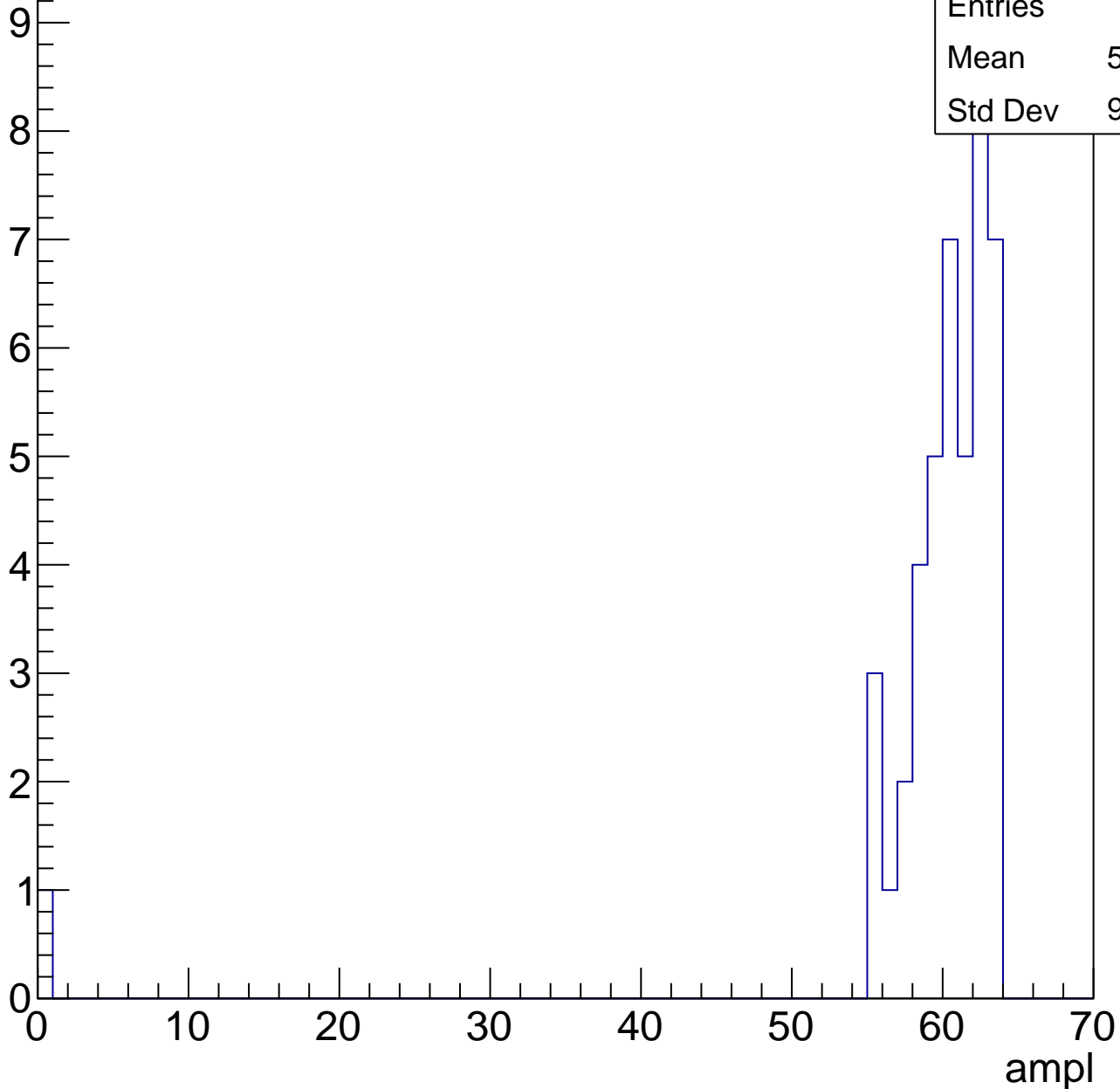


B1L103S, U9-ch85, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

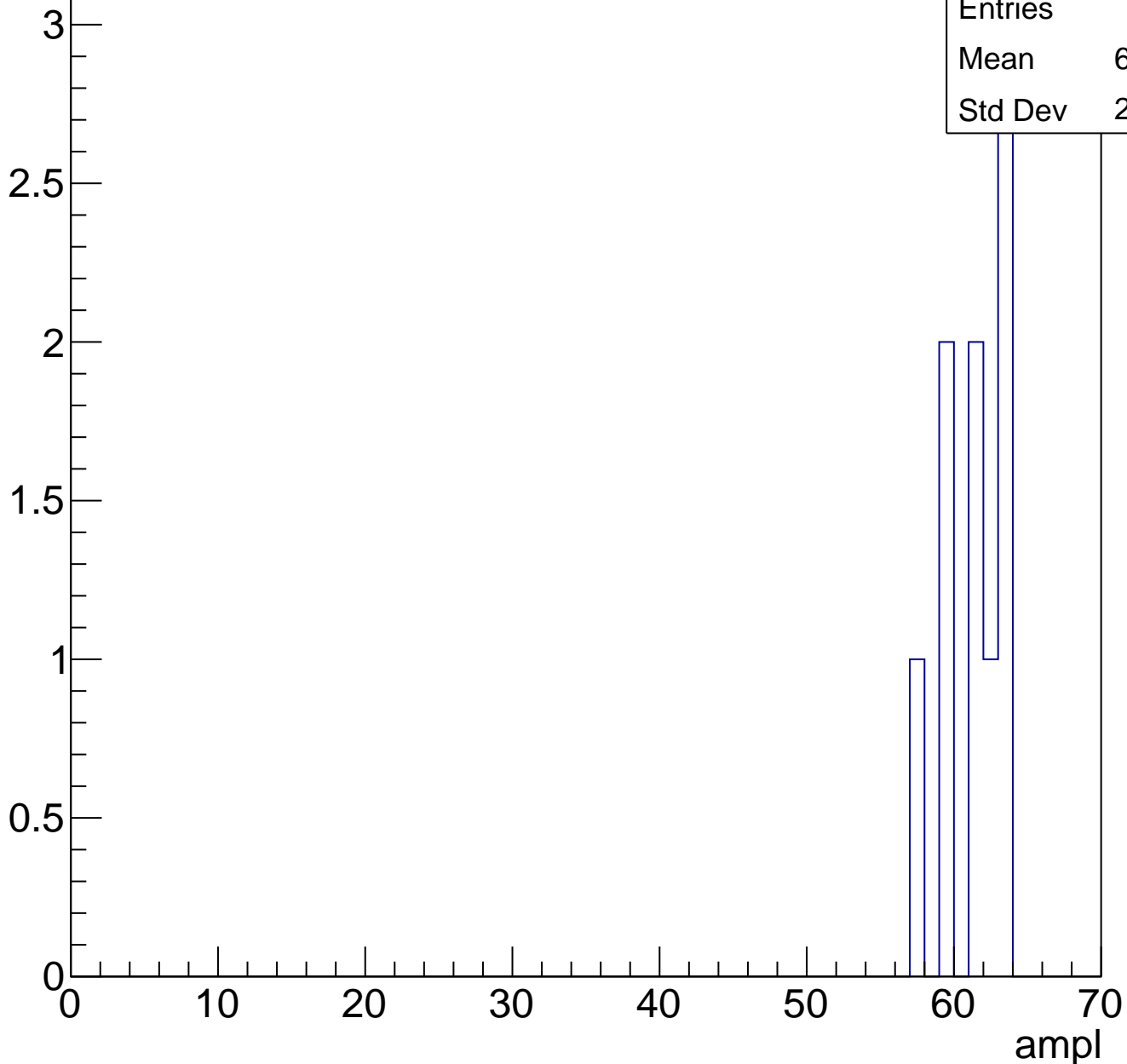
Entries	44
Mean	58.77
Std Dev	9.254



B1L103S, U9-ch85, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch85, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

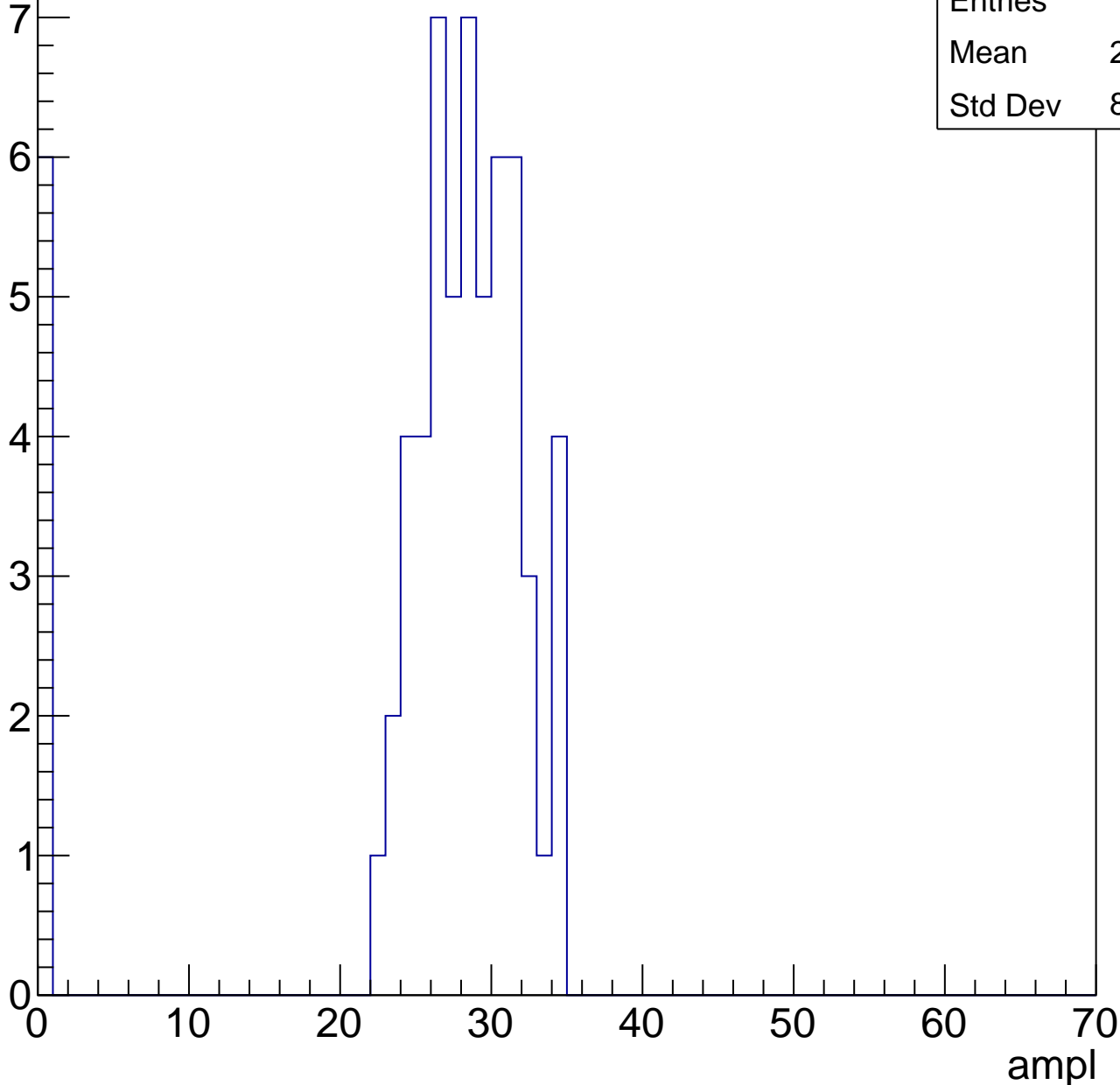
ampl

B1L103S, U9-ch86, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	25.46
Std Dev	8.898

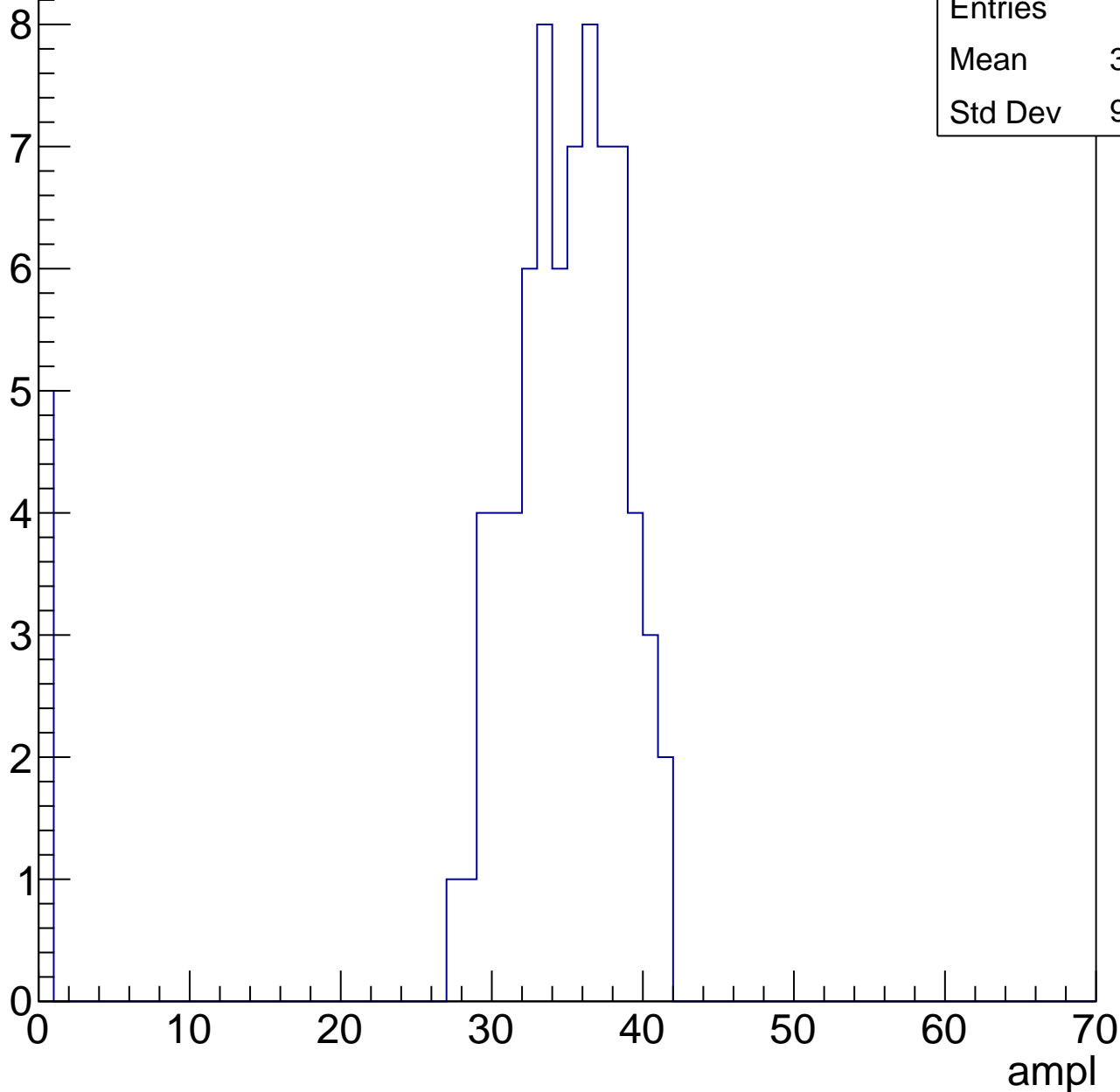


B1L103S, U9-ch86, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	32.35
Std Dev	9.122

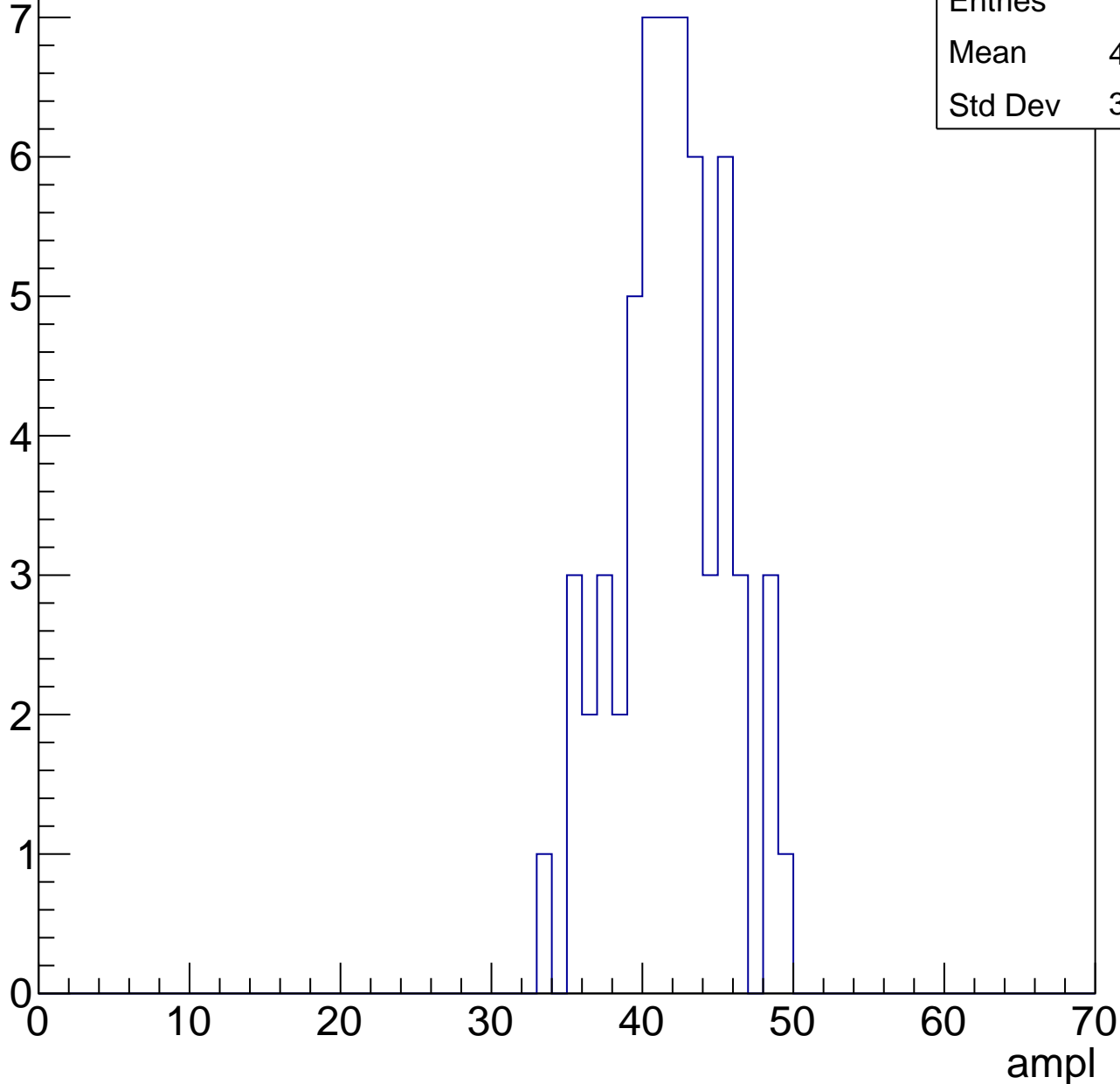


B1L103S, U9-ch86, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	41.42
Std Dev	3.552

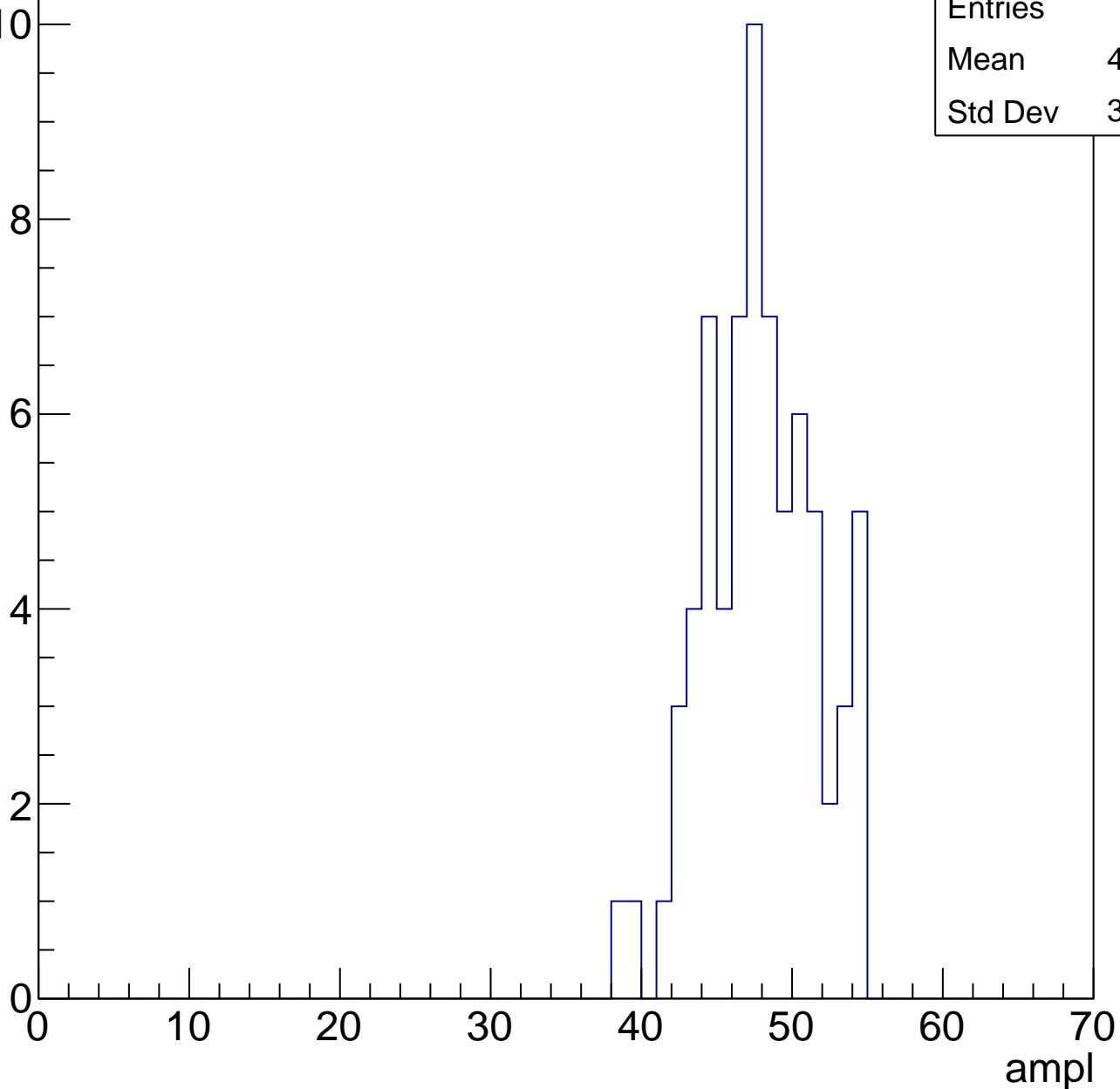


B1L103S, U9-ch86, adc3

calib_packv5_041523_1651.root, FC#0, port C2

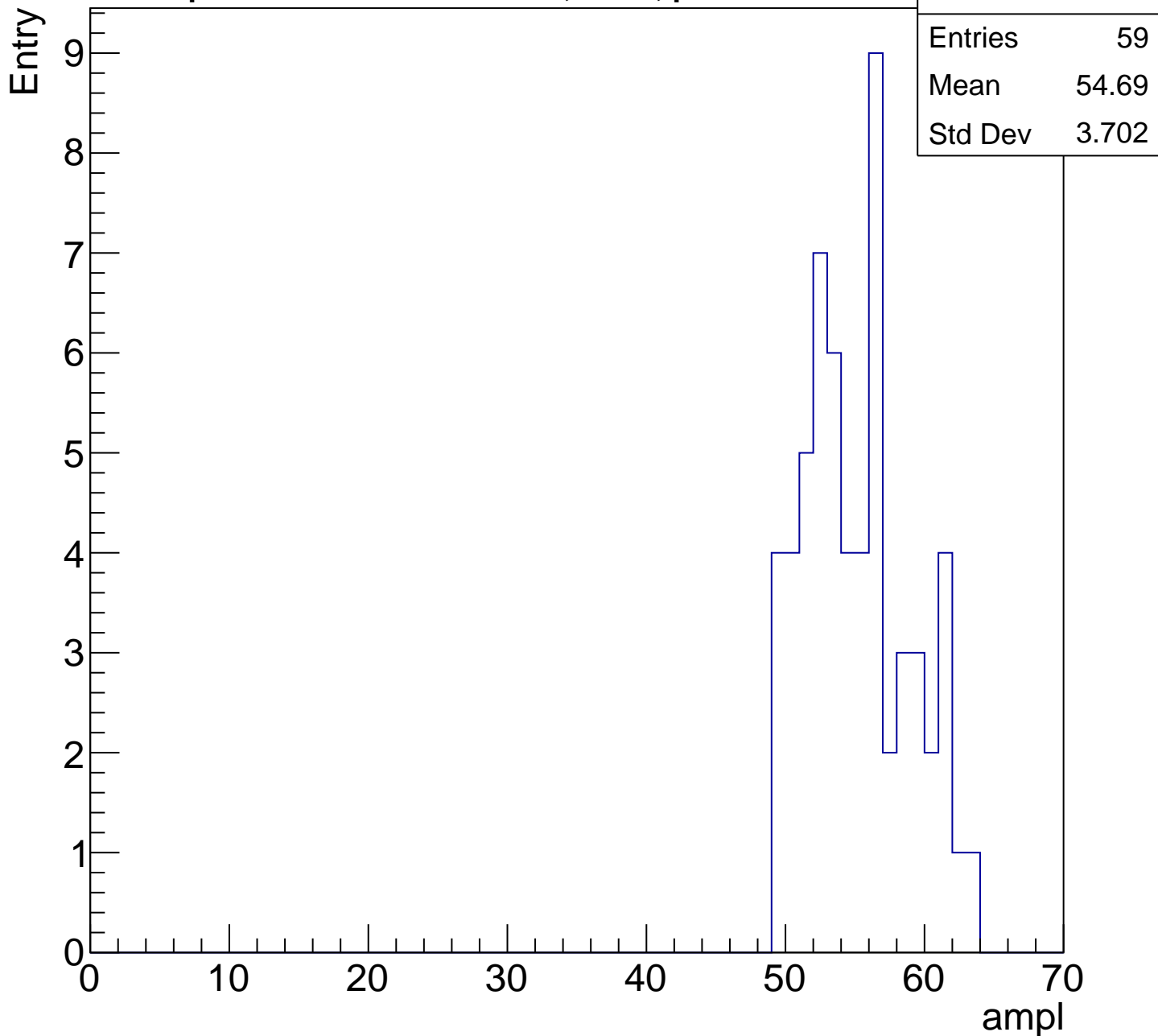
Entry

Entries	71
Mean	47.39
Std Dev	3.675



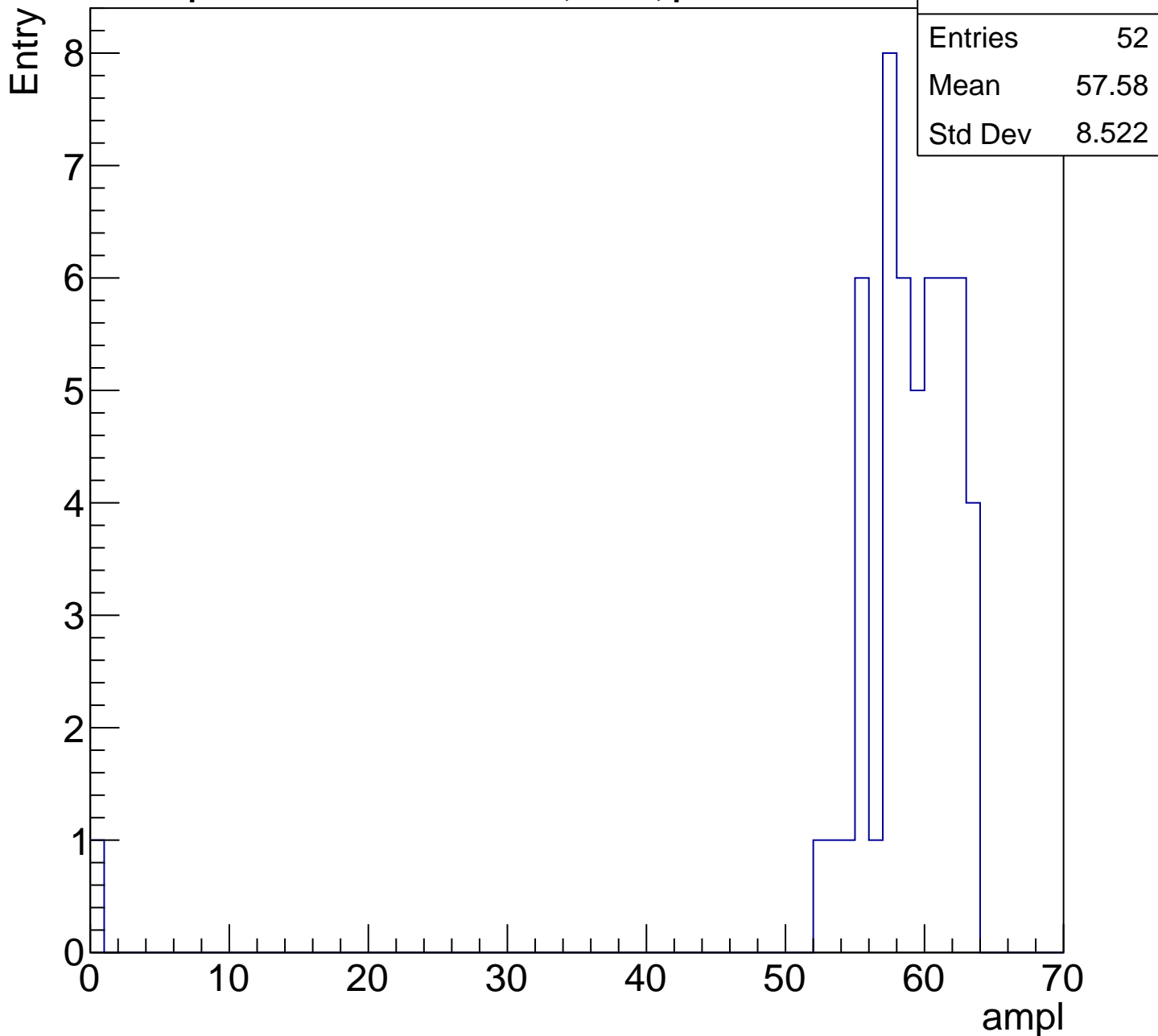
B1L103S, U9-ch86, adc4

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U9-ch86, adc5

calib_packv5_041523_1651.root, FC#0, port C2

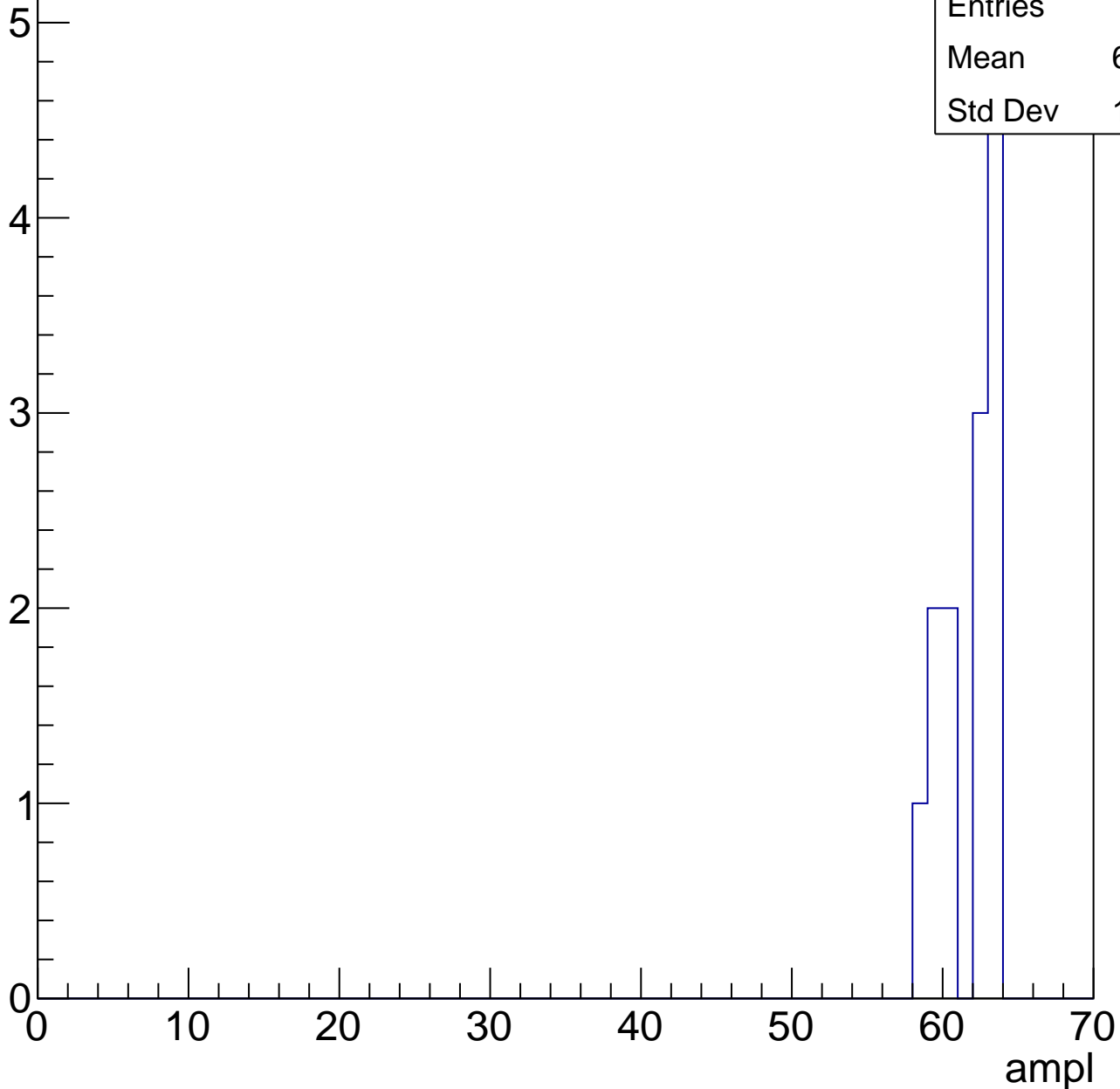


B1L103S, U9-ch86, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	13
Mean	61.31
Std Dev	1.771



B1L103S, U9-ch86, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

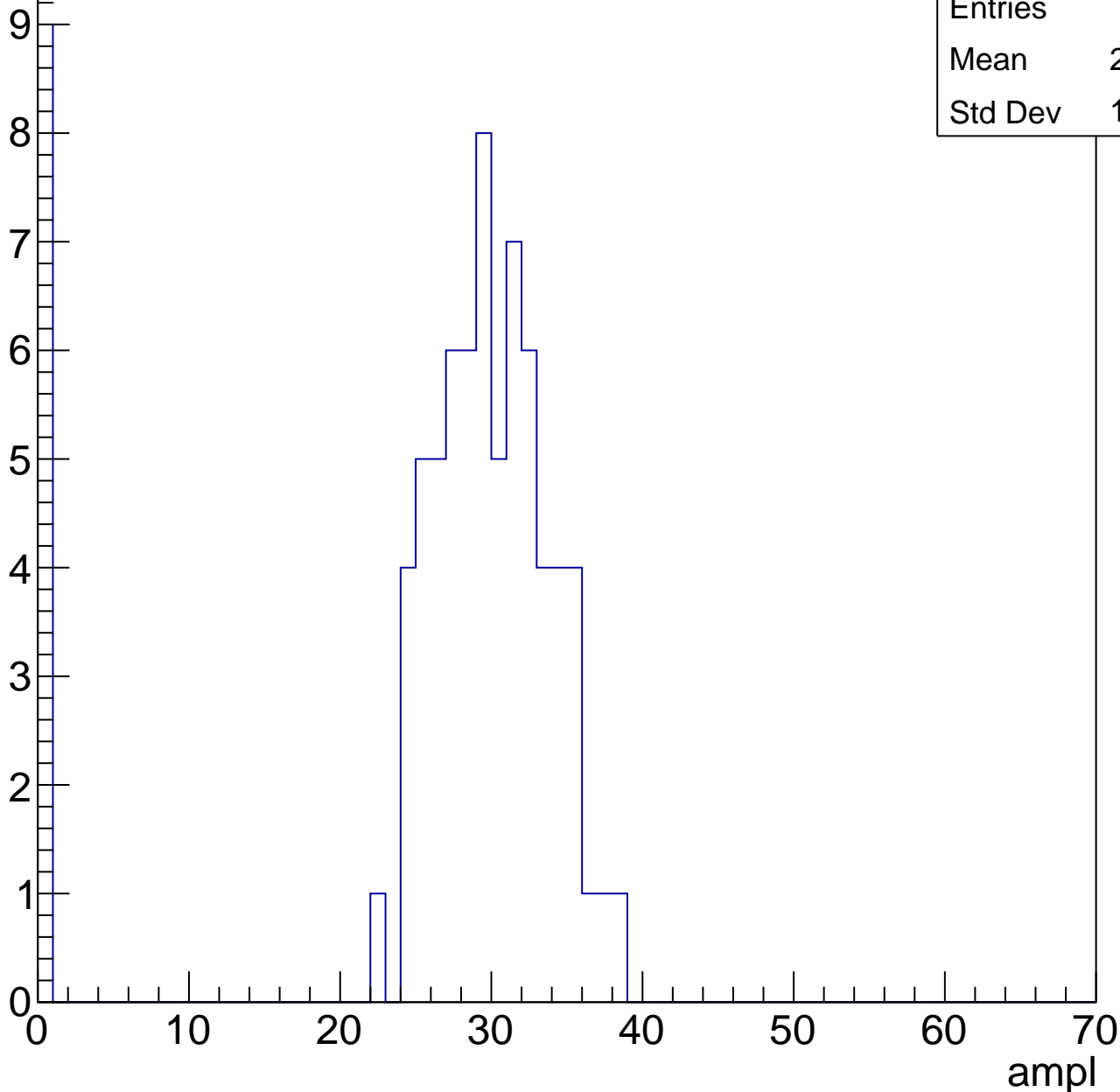


B1L103S, U9-ch87, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	26.14
Std Dev	10.09

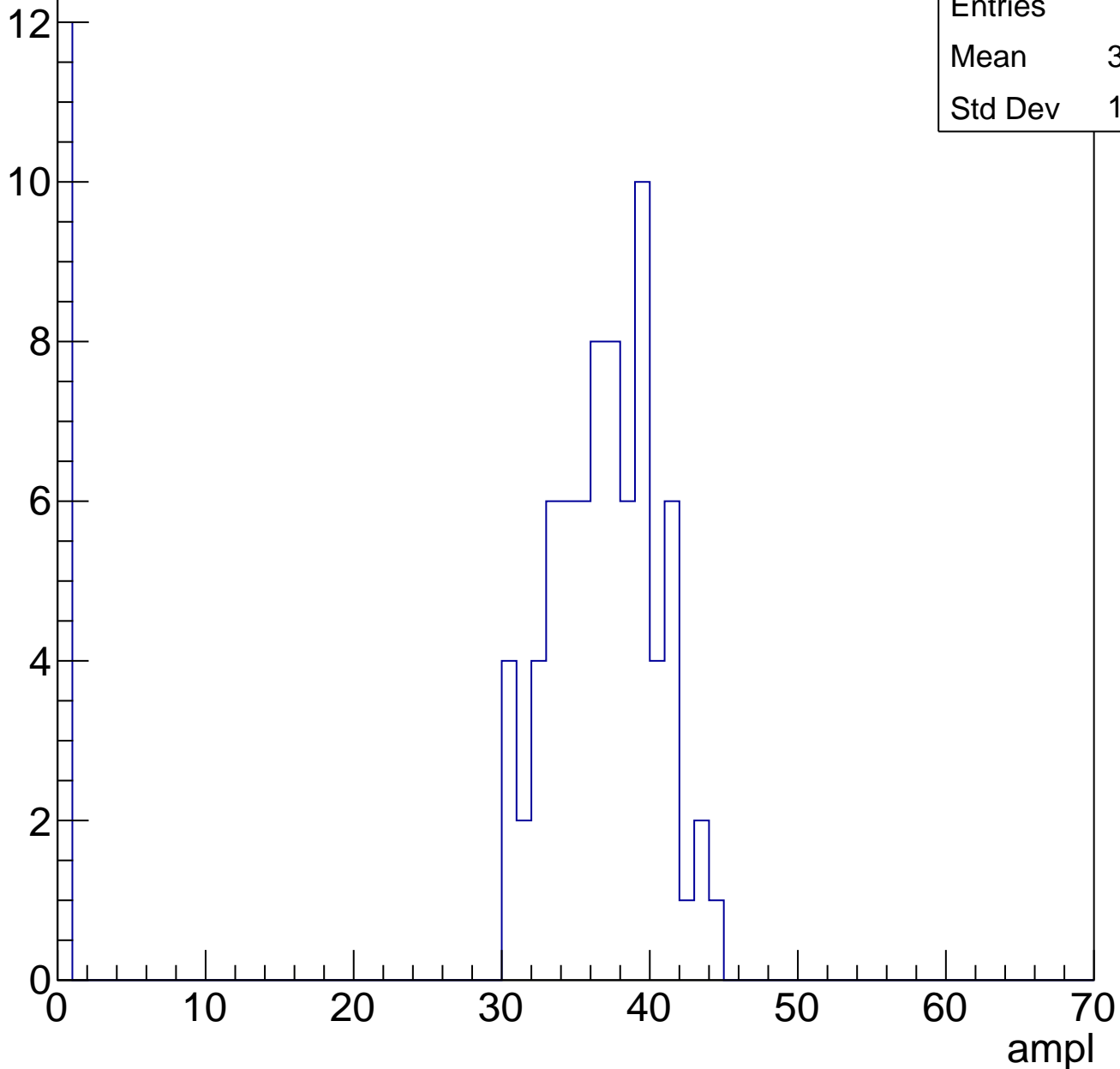


B1L103S, U9-ch87, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	86
Mean	31.42
Std Dev	13.04

Entry

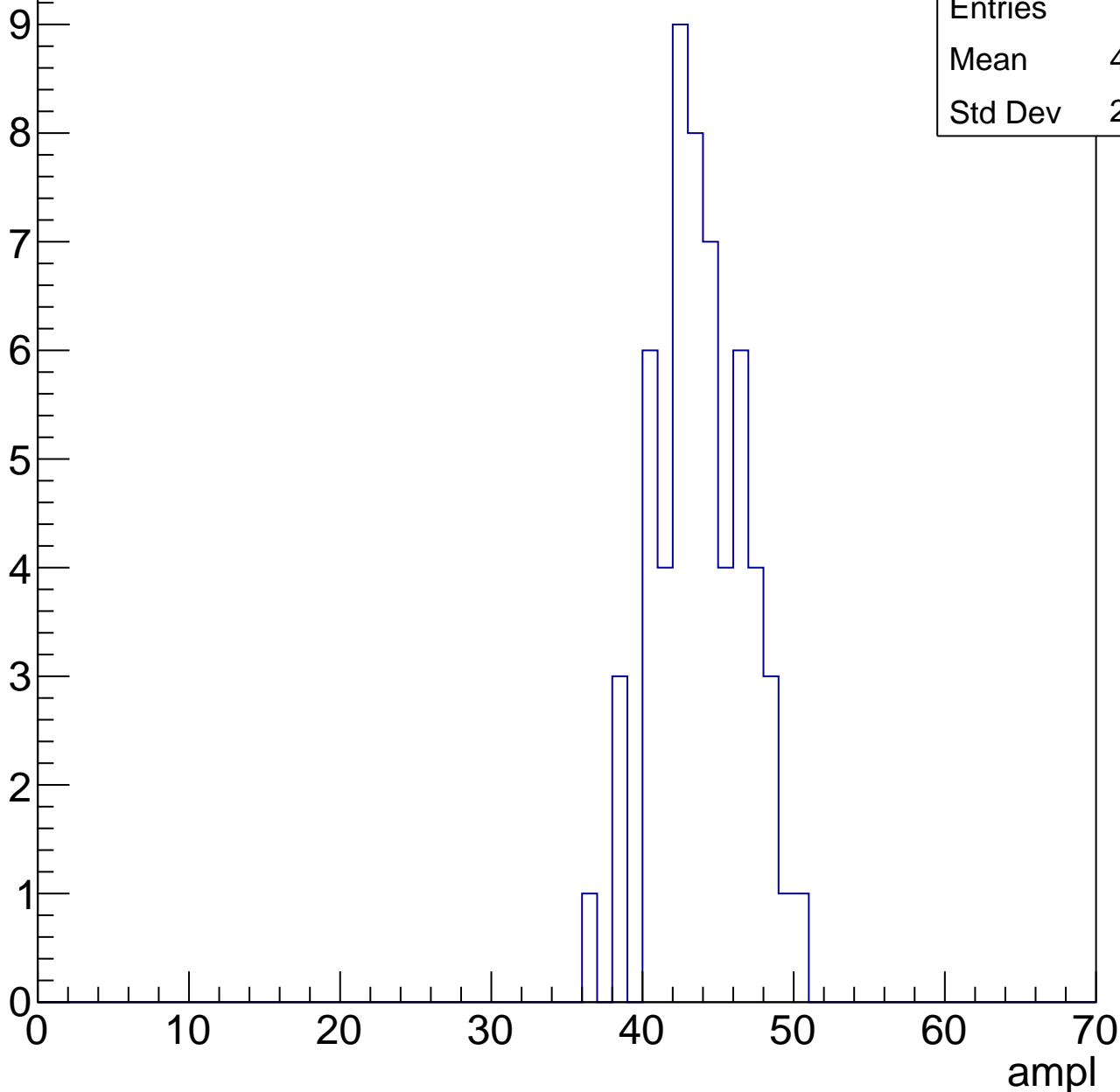


B1L103S, U9-ch87, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	43.35
Std Dev	2.953

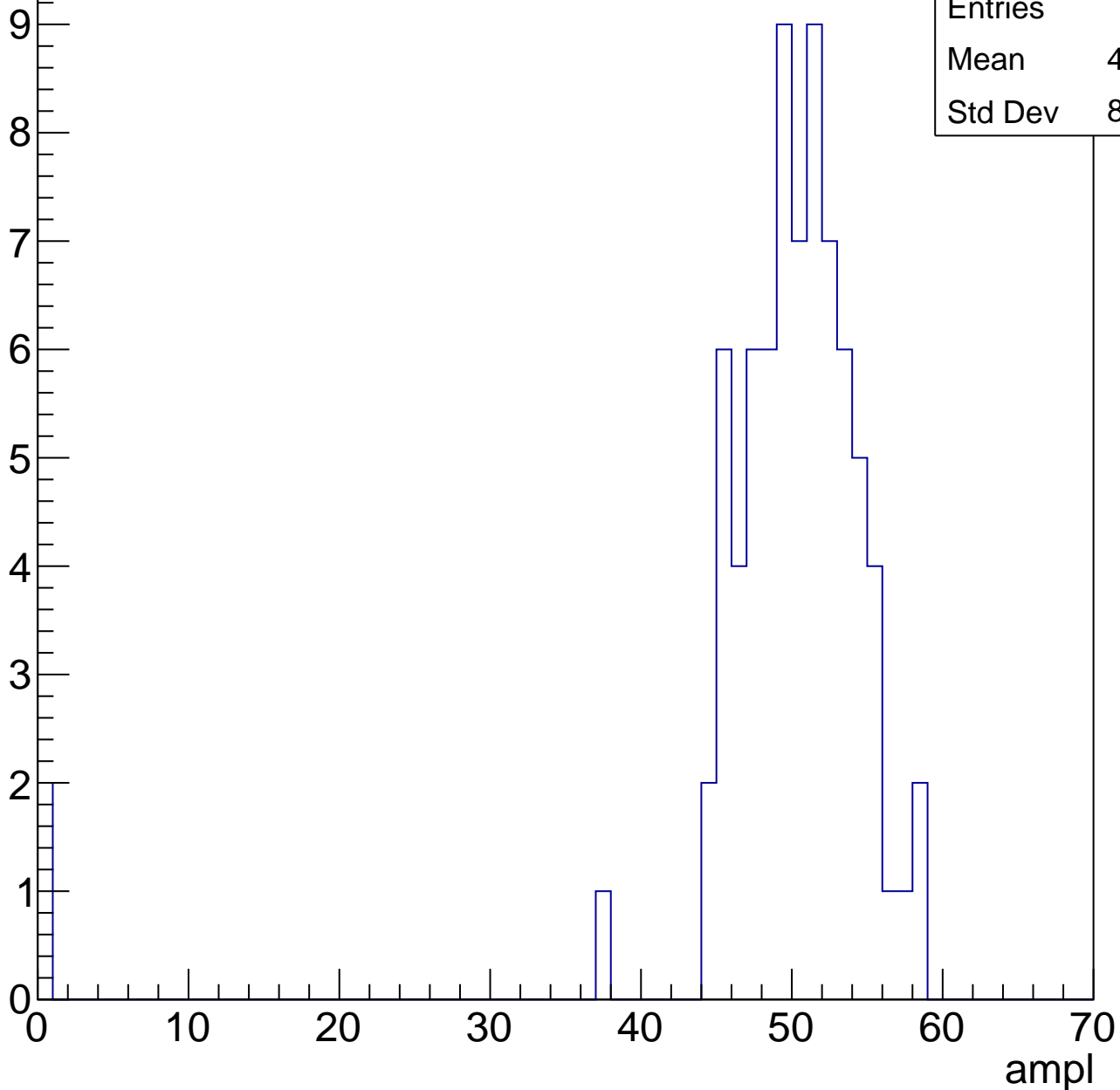


B1L103S, U9-ch87, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	48.72
Std Dev	8.696

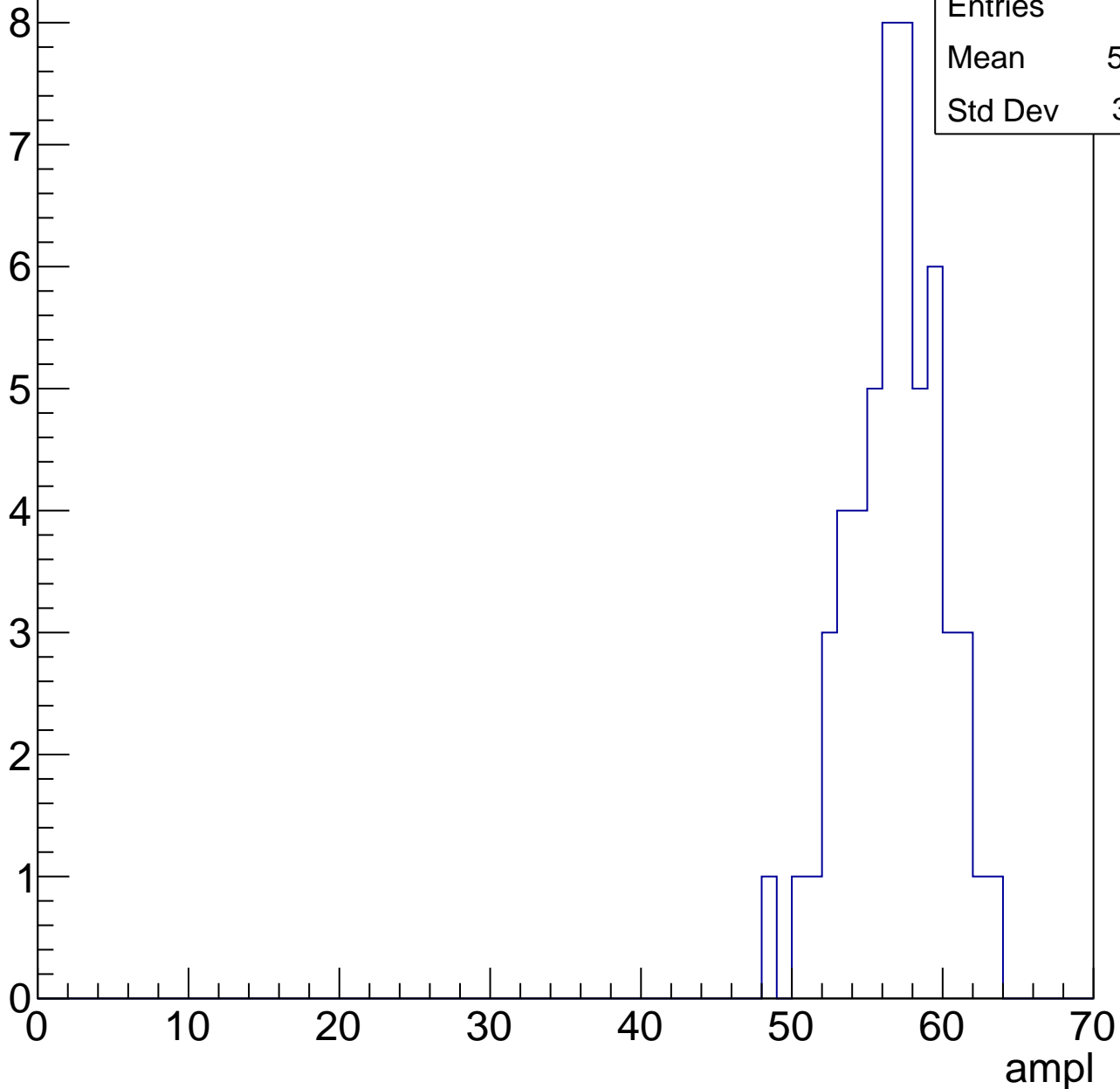


B1L103S, U9-ch87, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	56.37
Std Dev	3.081



B1L103S, U9-ch87, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

7

6

5

4

3

2

1

0

Entries

35

Mean

59.8

Std Dev

2.786

0

10

20

30

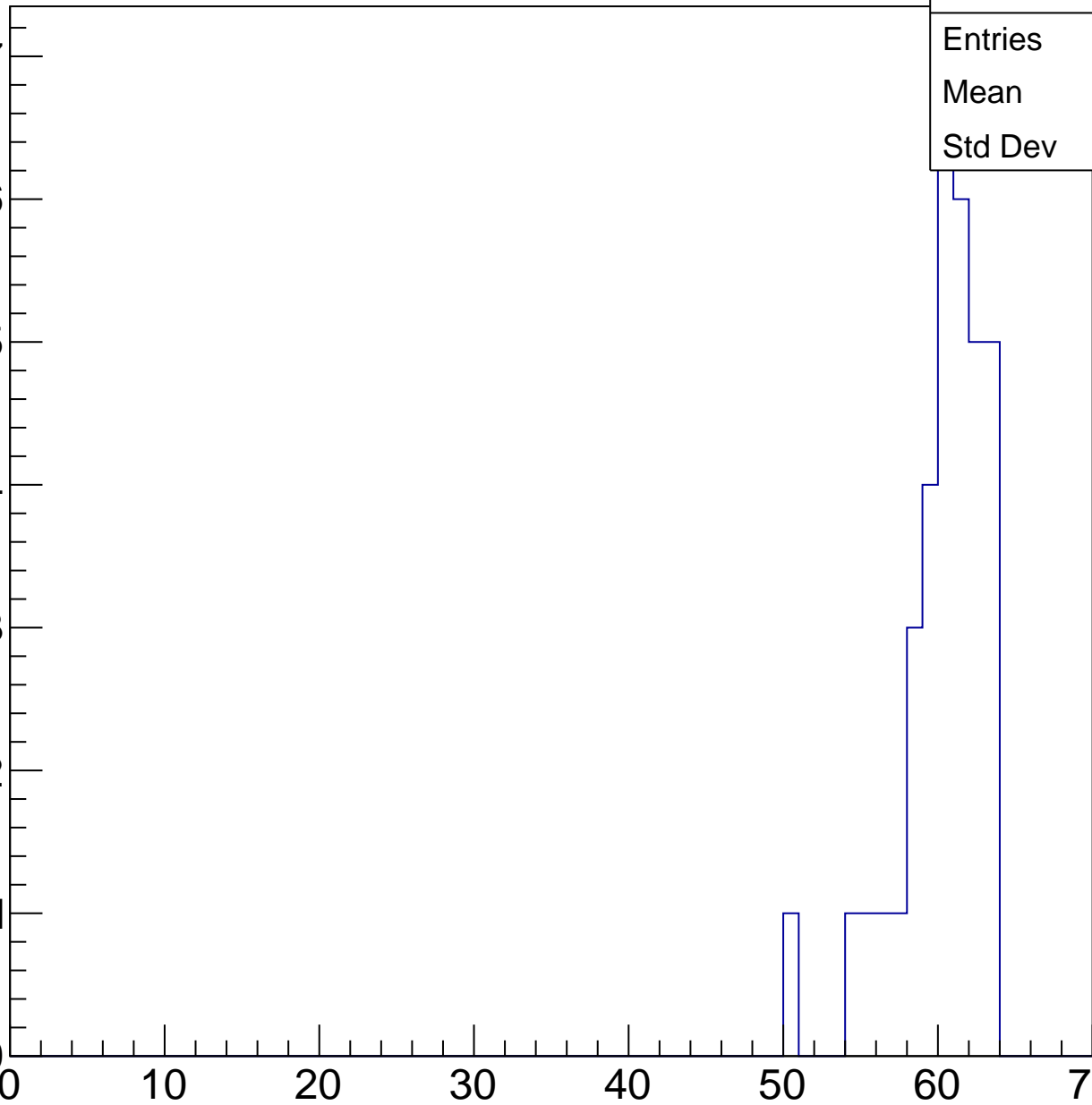
40

50

60

70

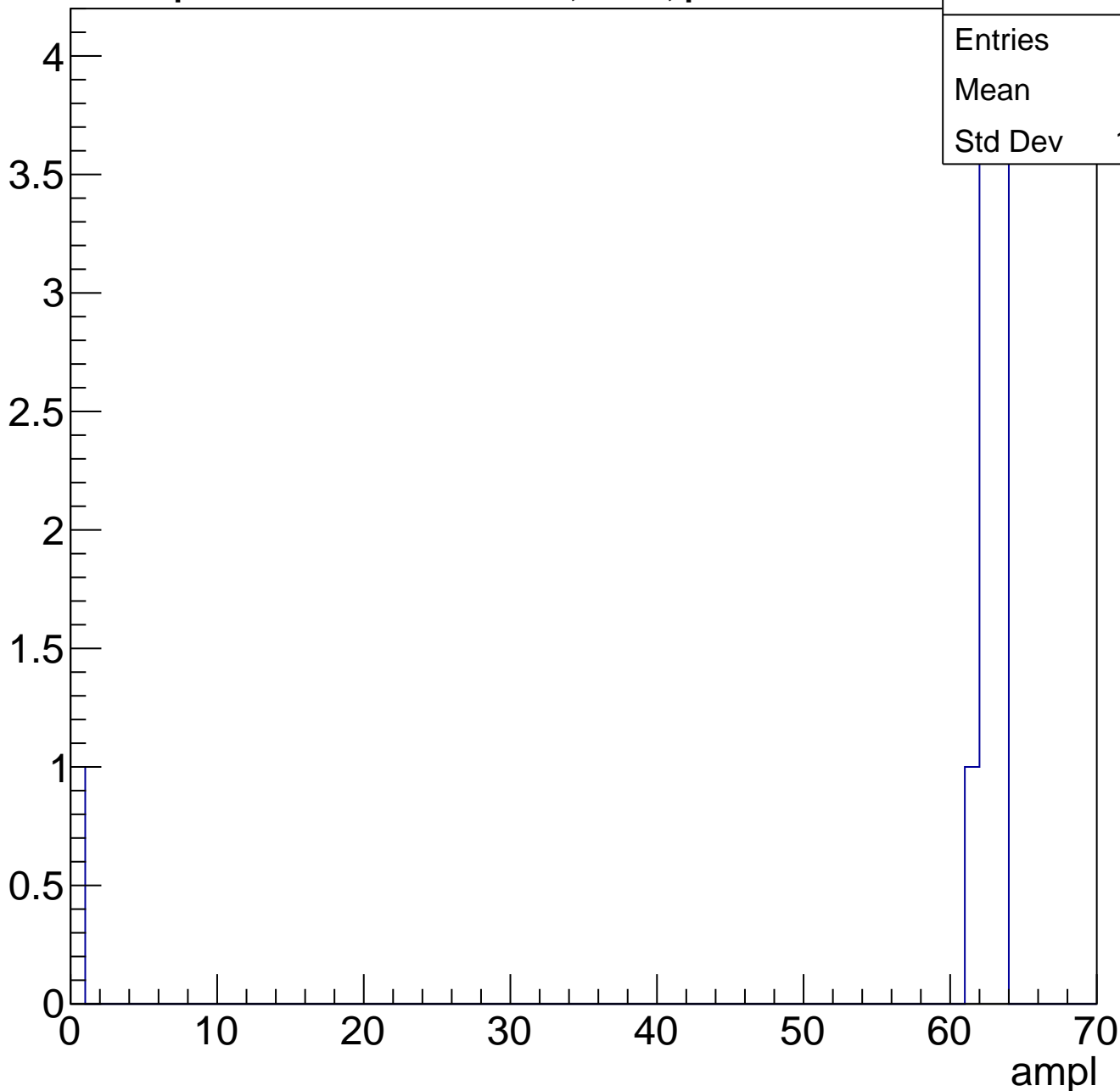
ampl



B1L103S, U9-ch87, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	10
Mean	56.1
Std Dev	18.71

B1L103S, U9-ch87, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

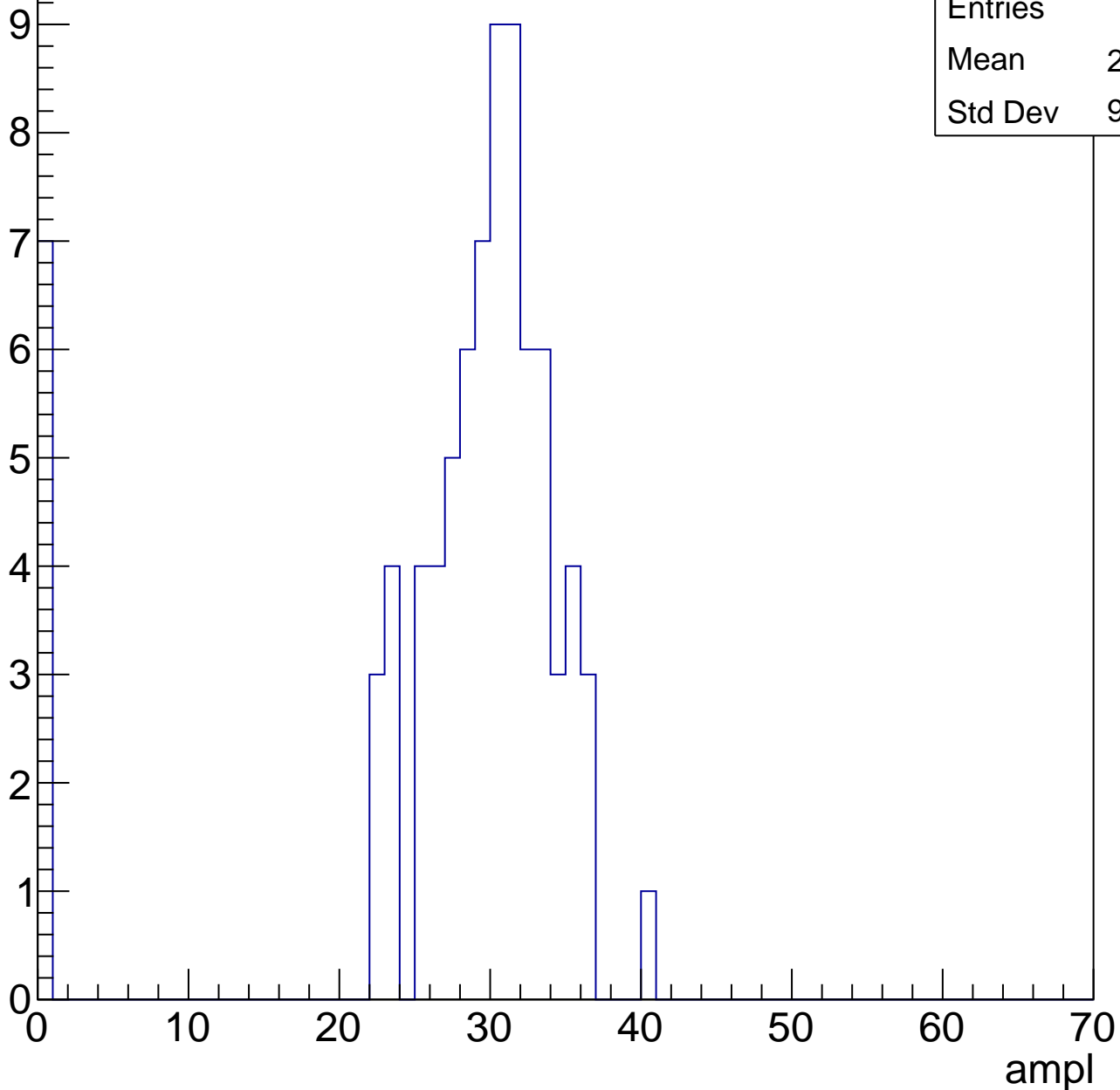
ampl

B1L103S, U9-ch88, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	81
Mean	27.12
Std Dev	9.095

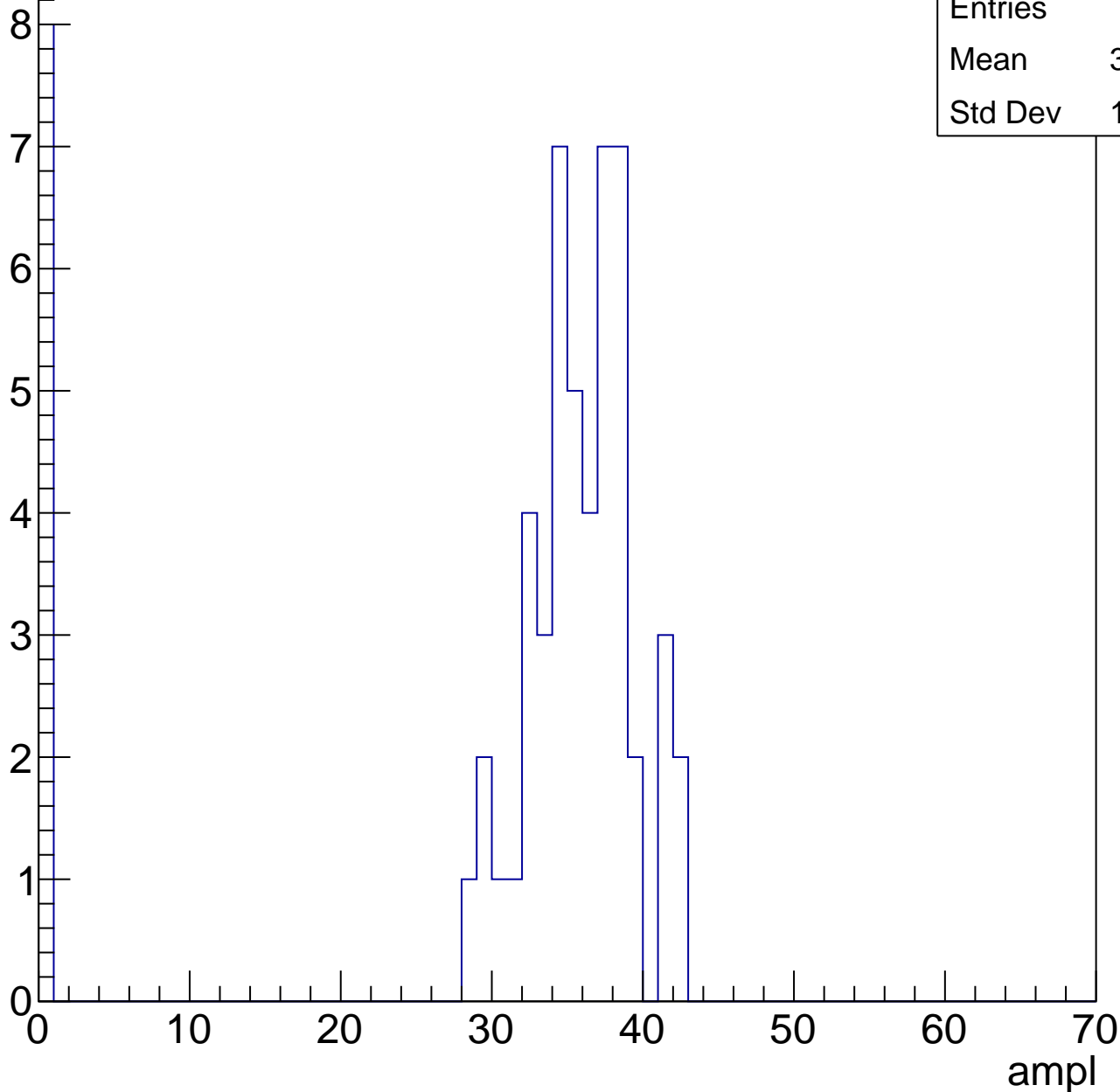


B1L103S, U9-ch88, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	30.54
Std Dev	12.72

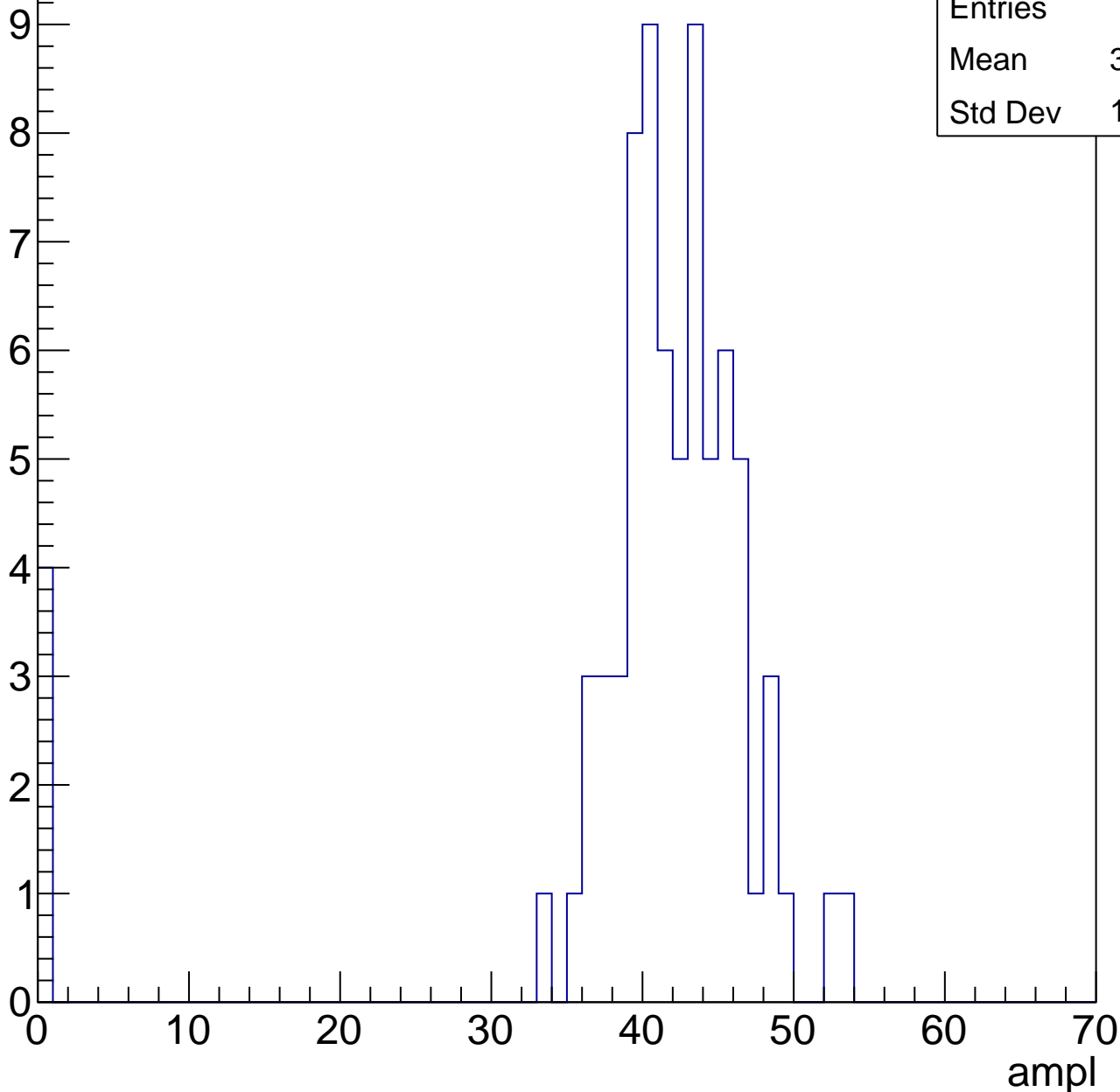


B1L103S, U9-ch88, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	39.75
Std Dev	10.14

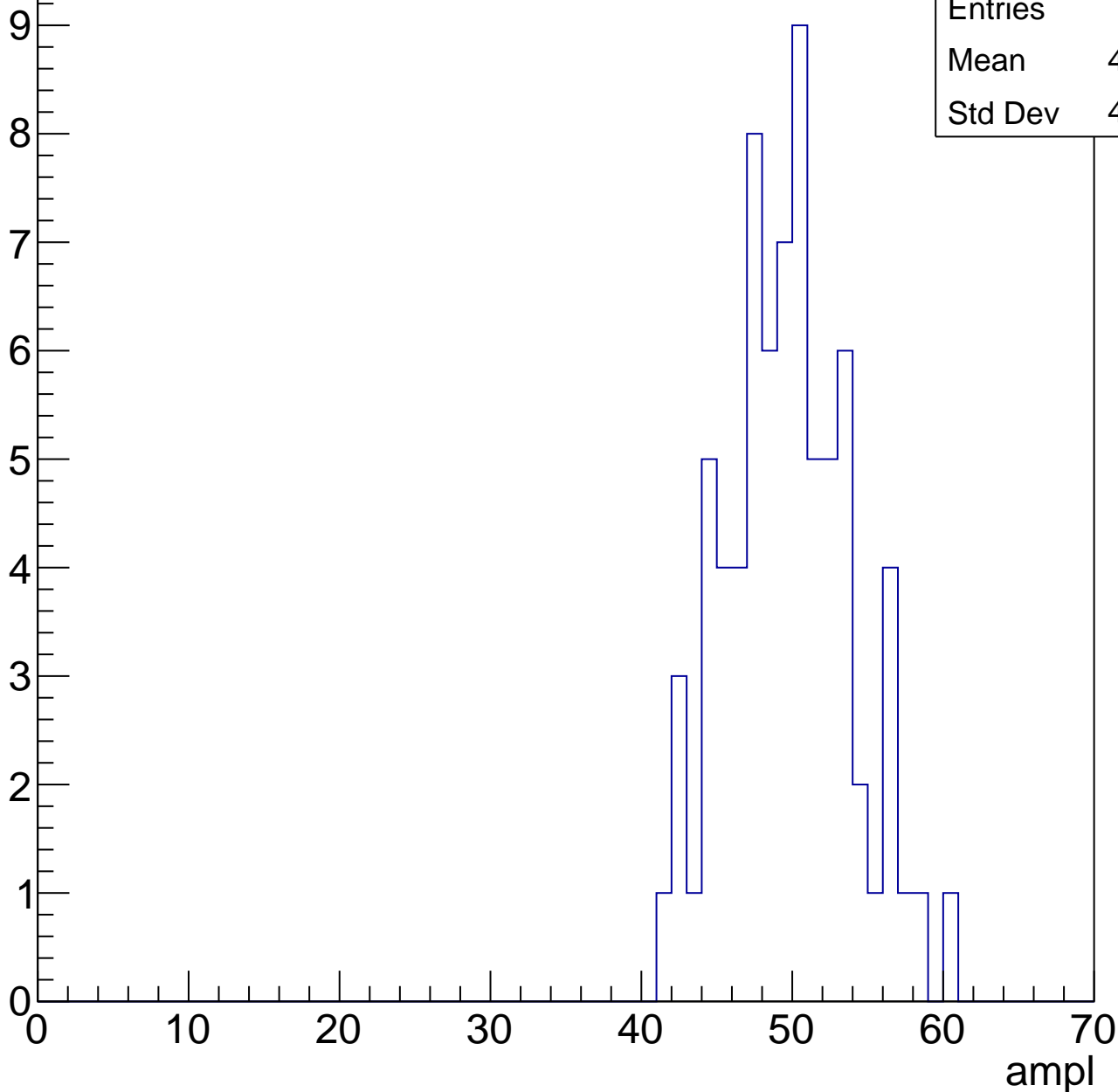


B1L103S, U9-ch88, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	49.27
Std Dev	4.065

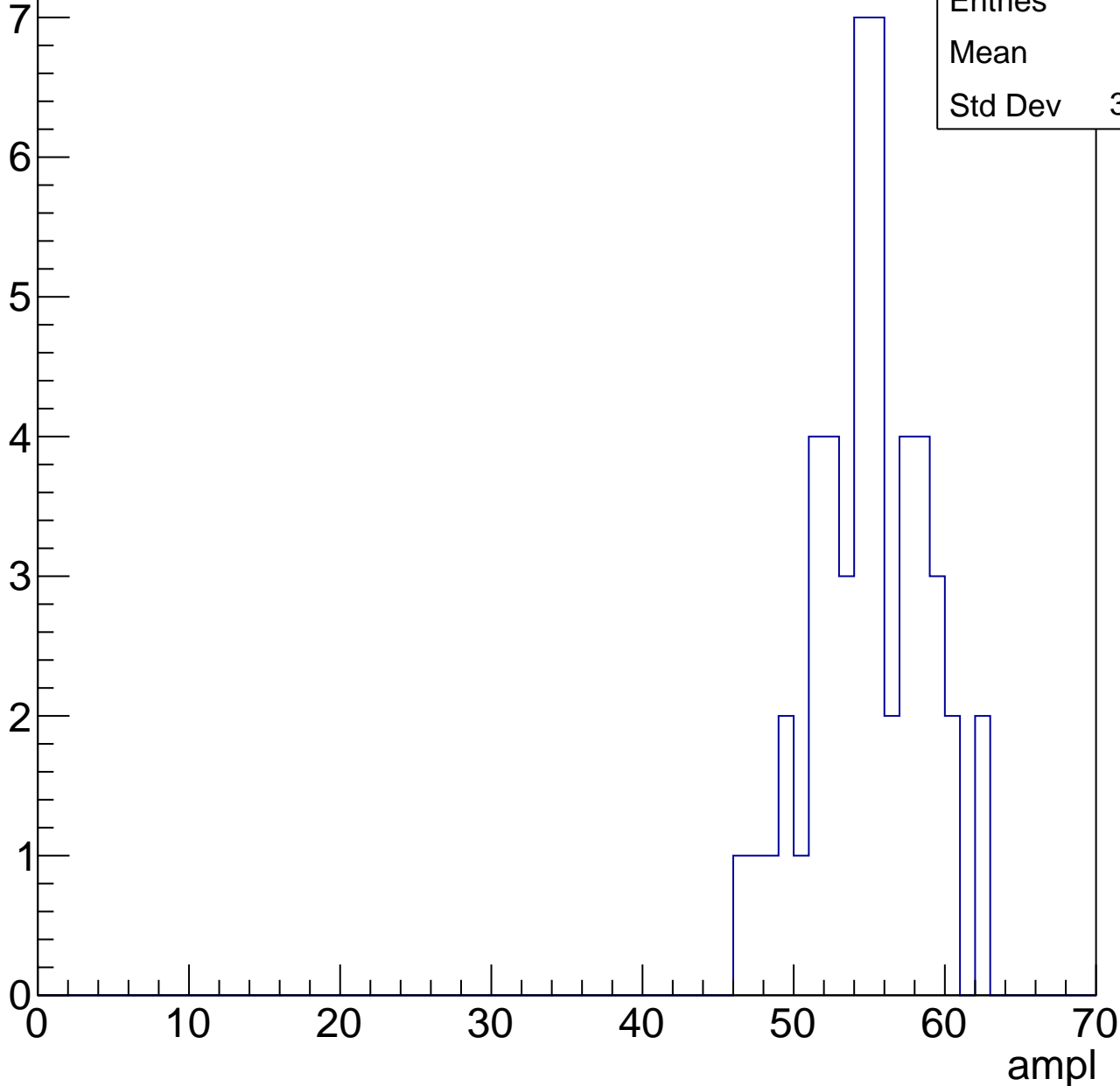


B1L103S, U9-ch88, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	48
Mean	54.5
Std Dev	3.674

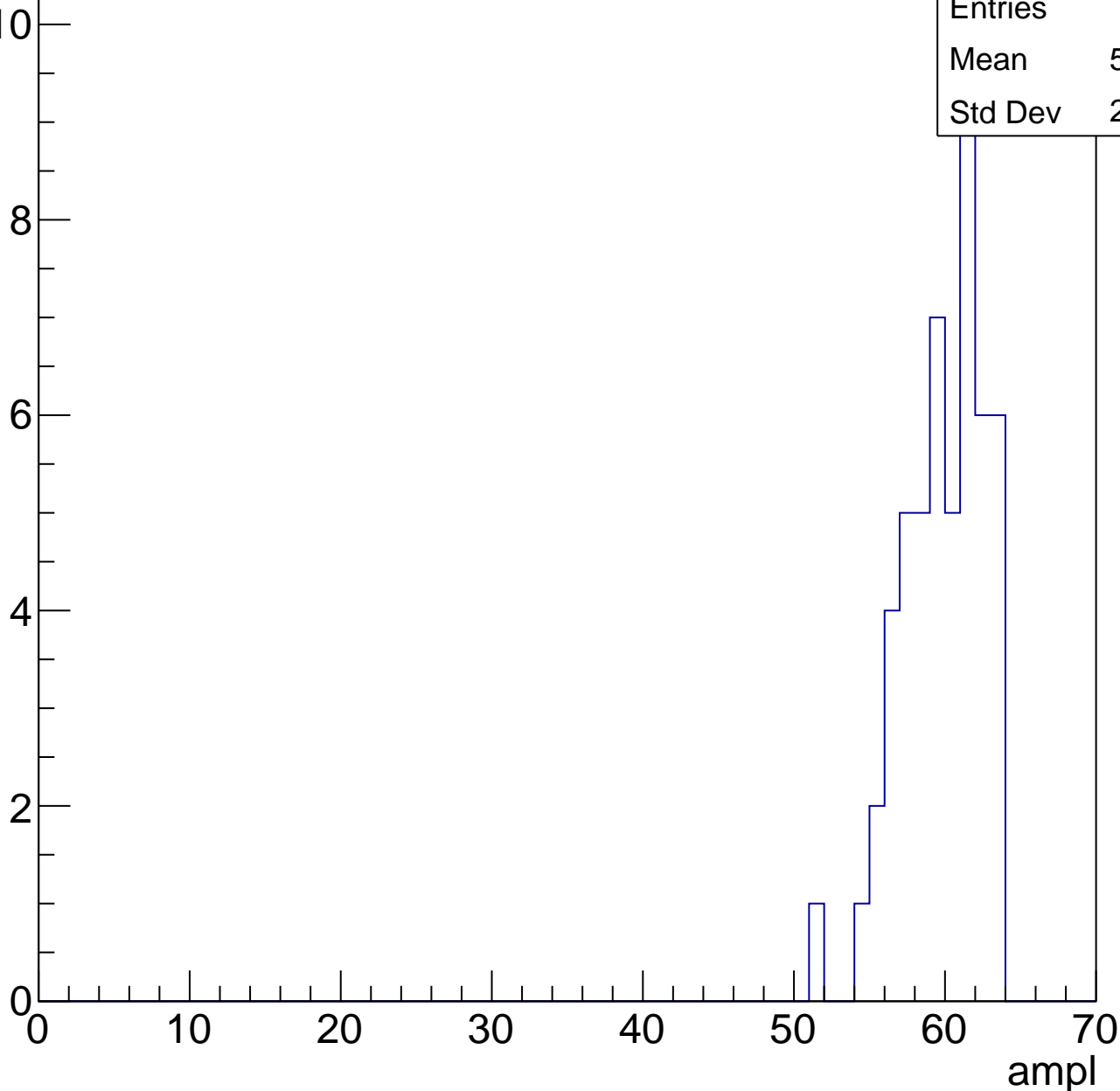


B1L103S, U9-ch88, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

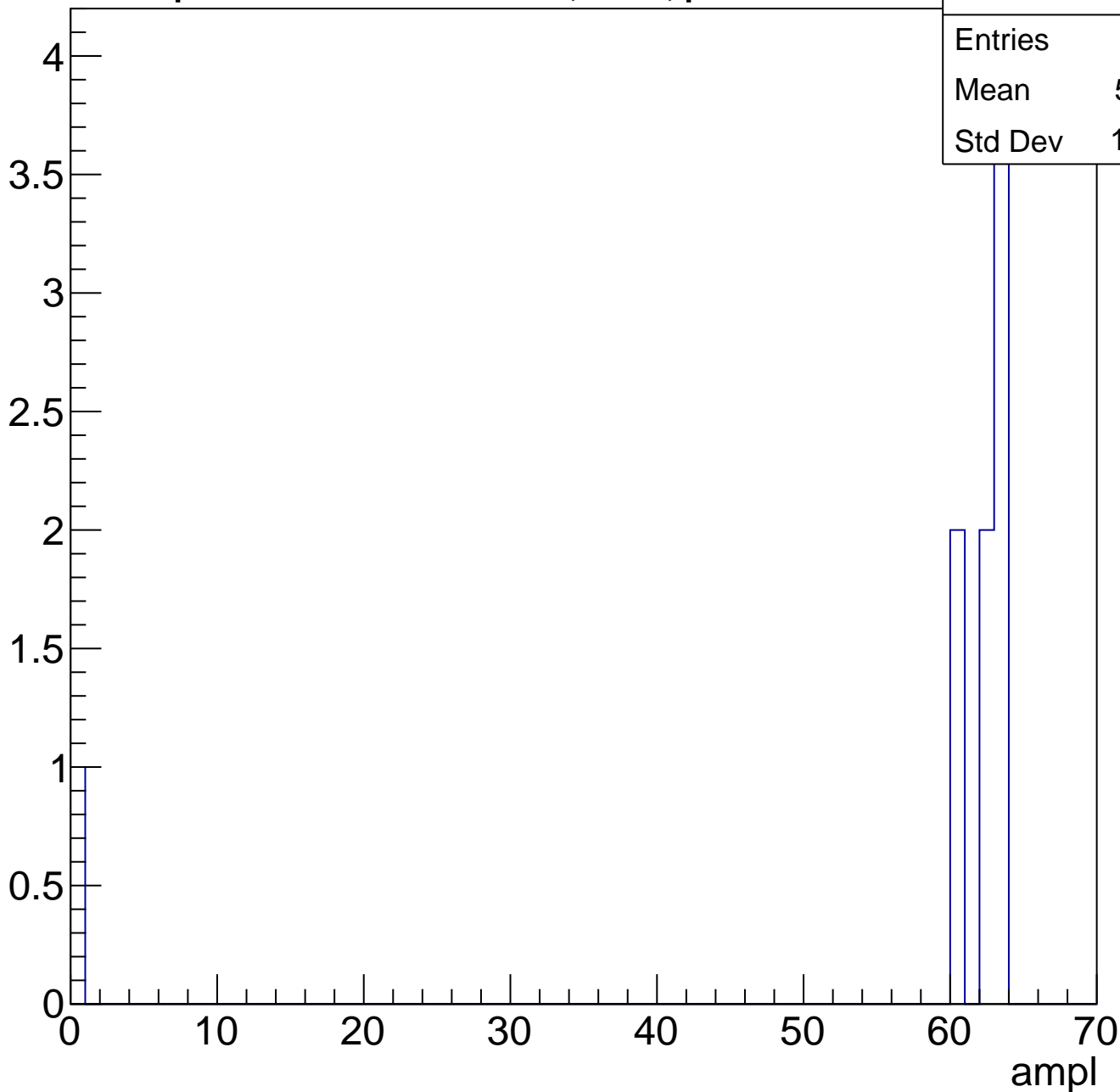
Entries	52
Mean	59.37
Std Dev	2.668



B1L103S, U9-ch88, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch88, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

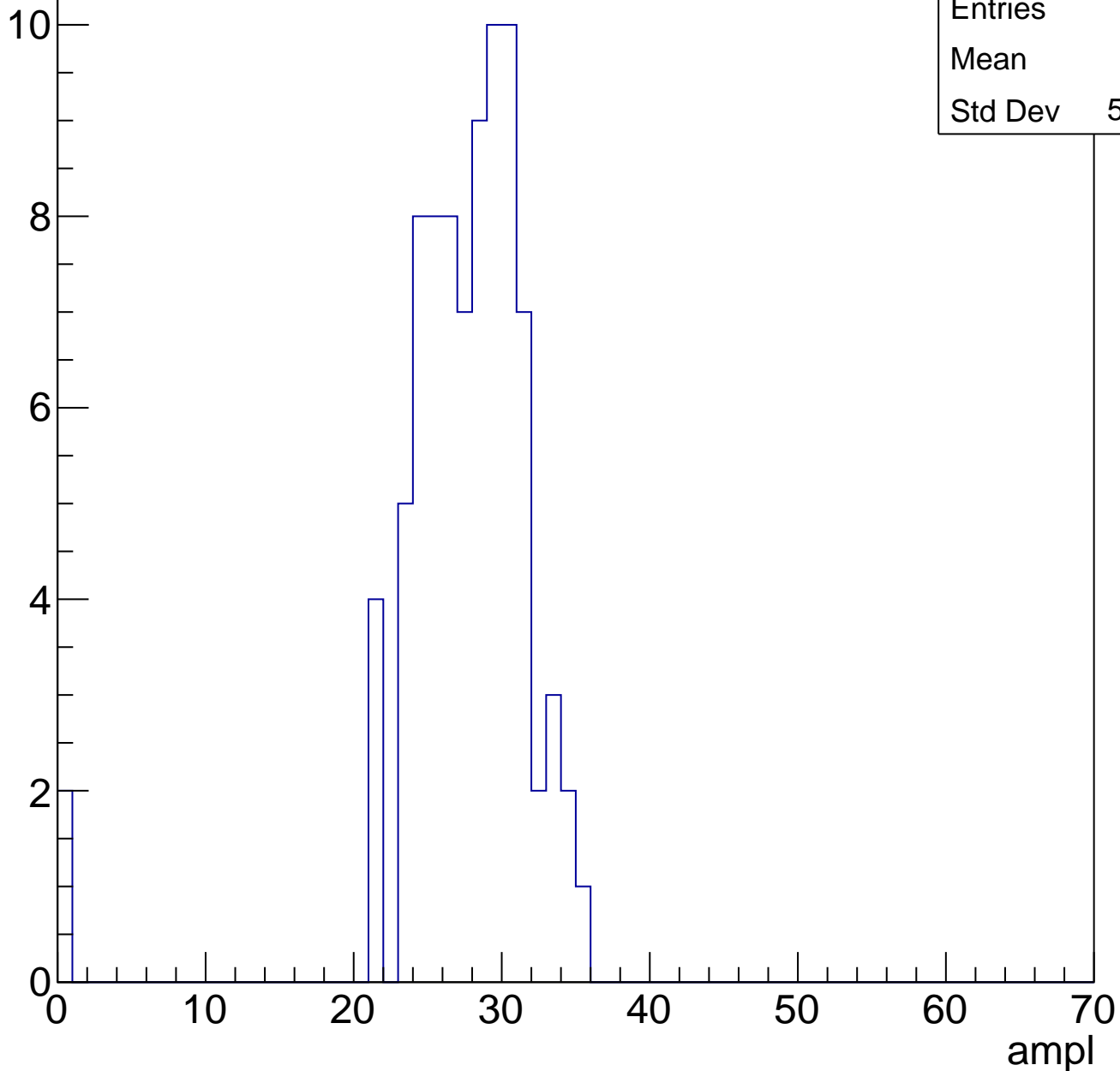


B1L103S, U9-ch89, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	86
Mean	26.9
Std Dev	5.243

Entry

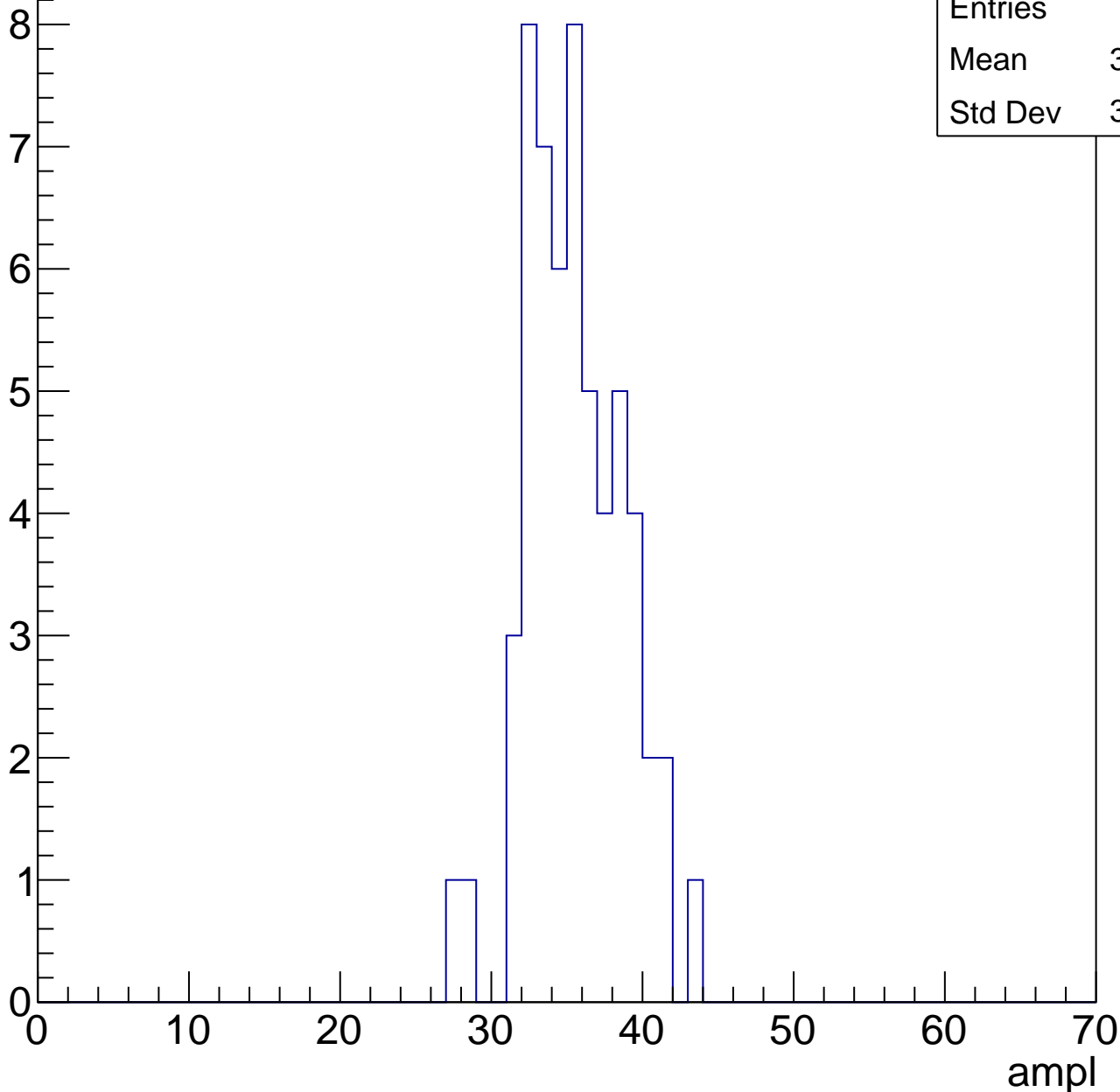


B1L103S, U9-ch89, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	35.05
Std Dev	3.198

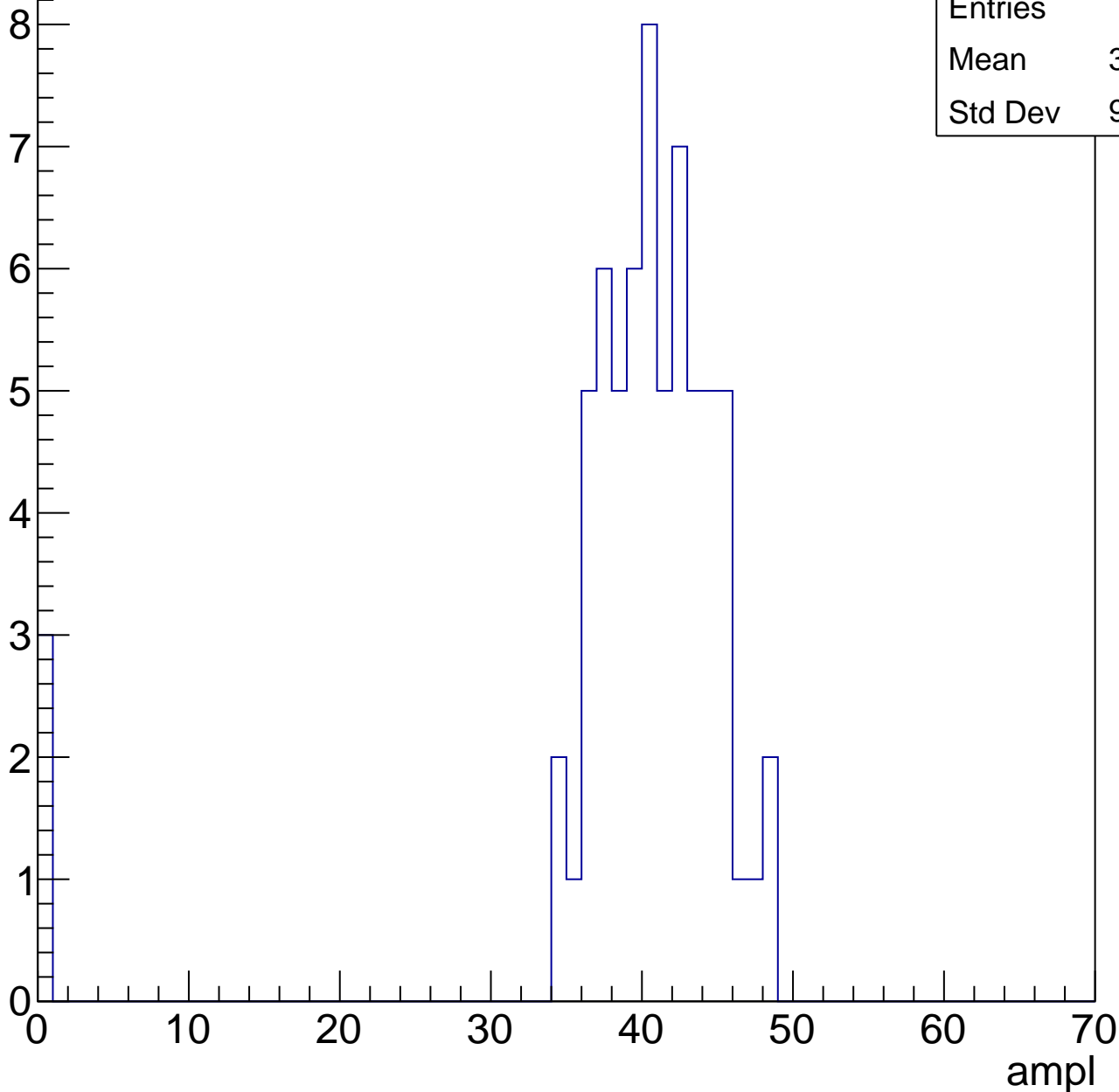


B1L103S, U9-ch89, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	38.76
Std Dev	9.019

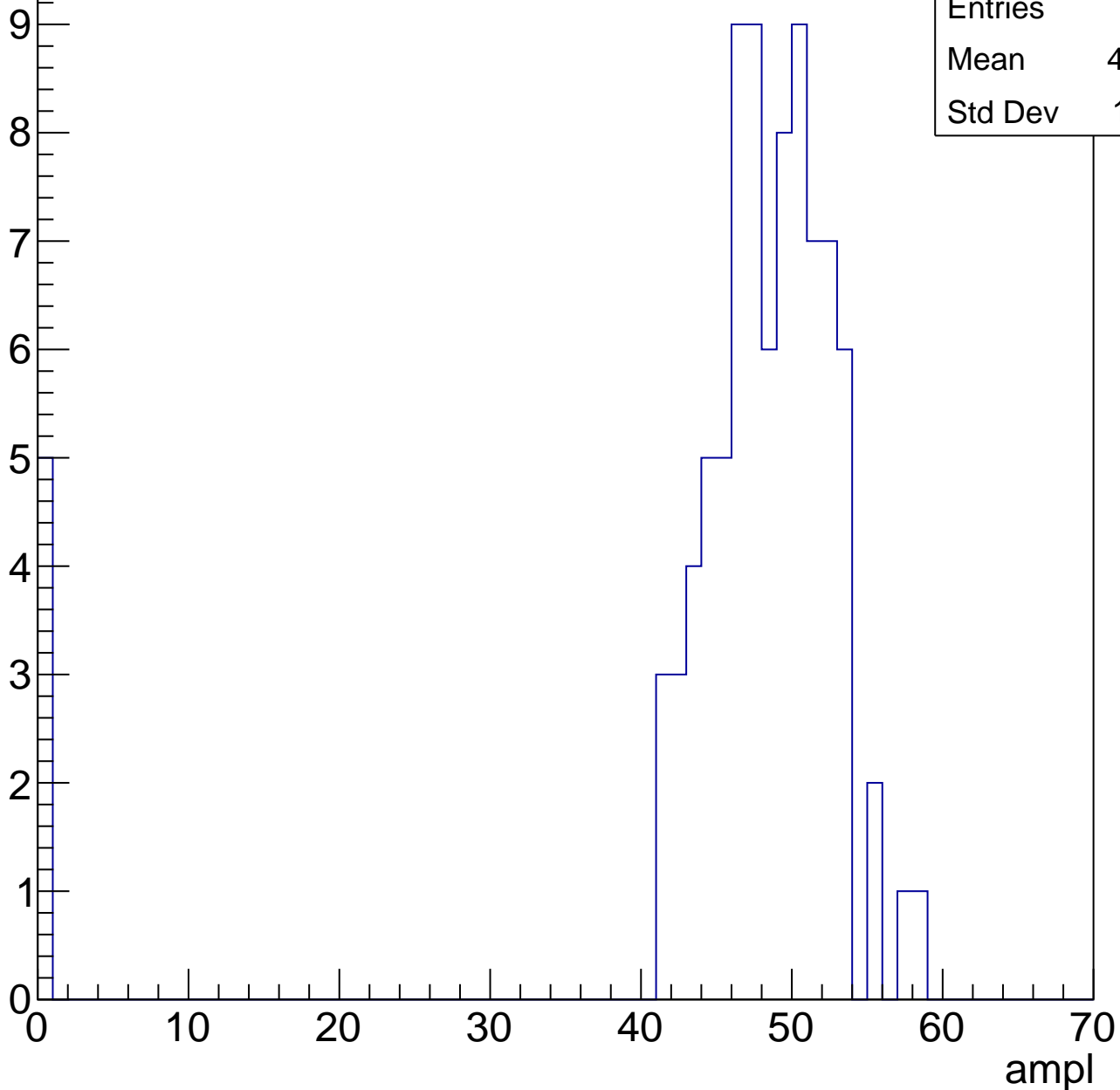


B1L103S, U9-ch89, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	90
Mean	45.52
Std Dev	11.61

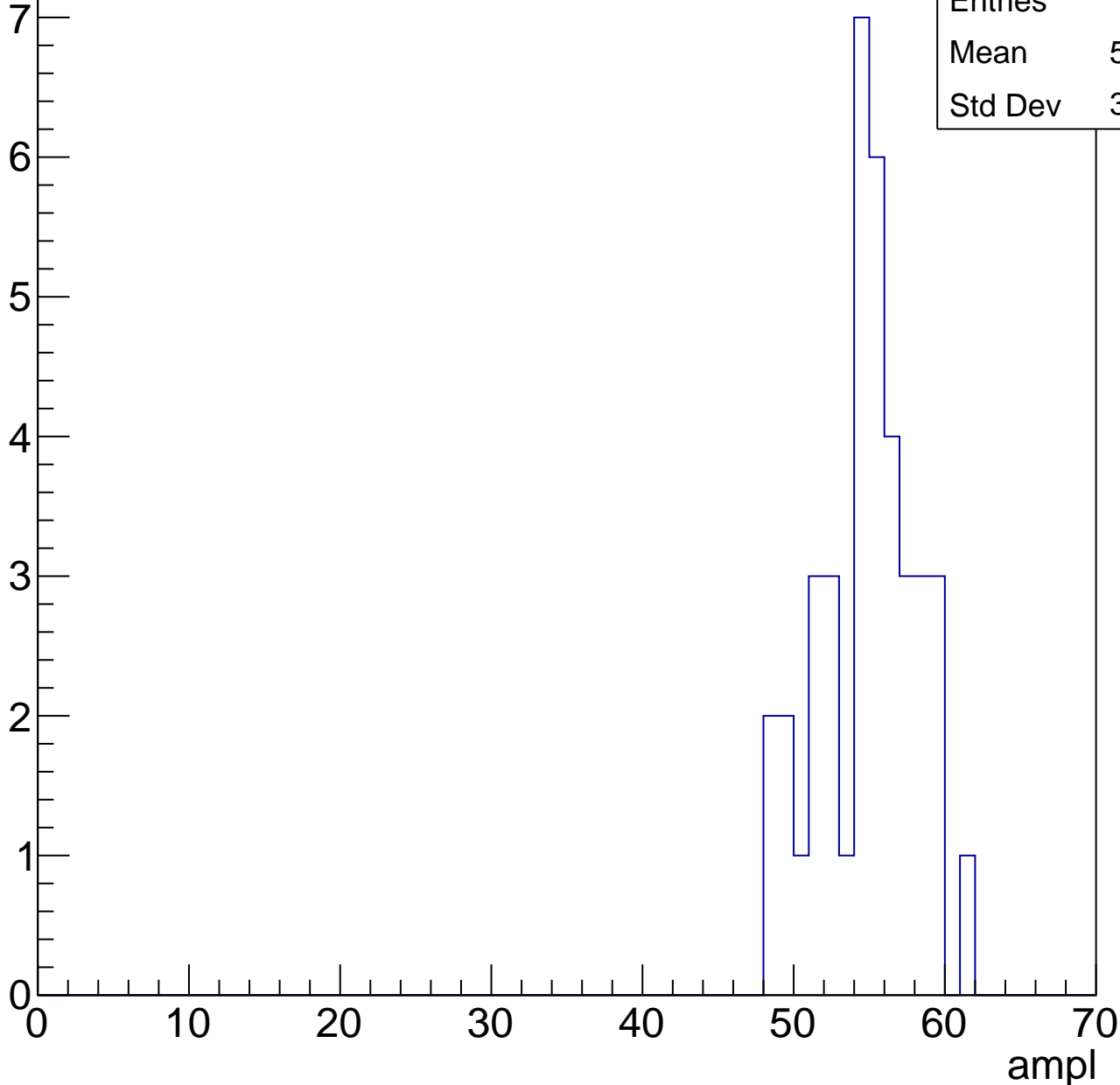


B1L103S, U9-ch89, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	54.38
Std Dev	3.175

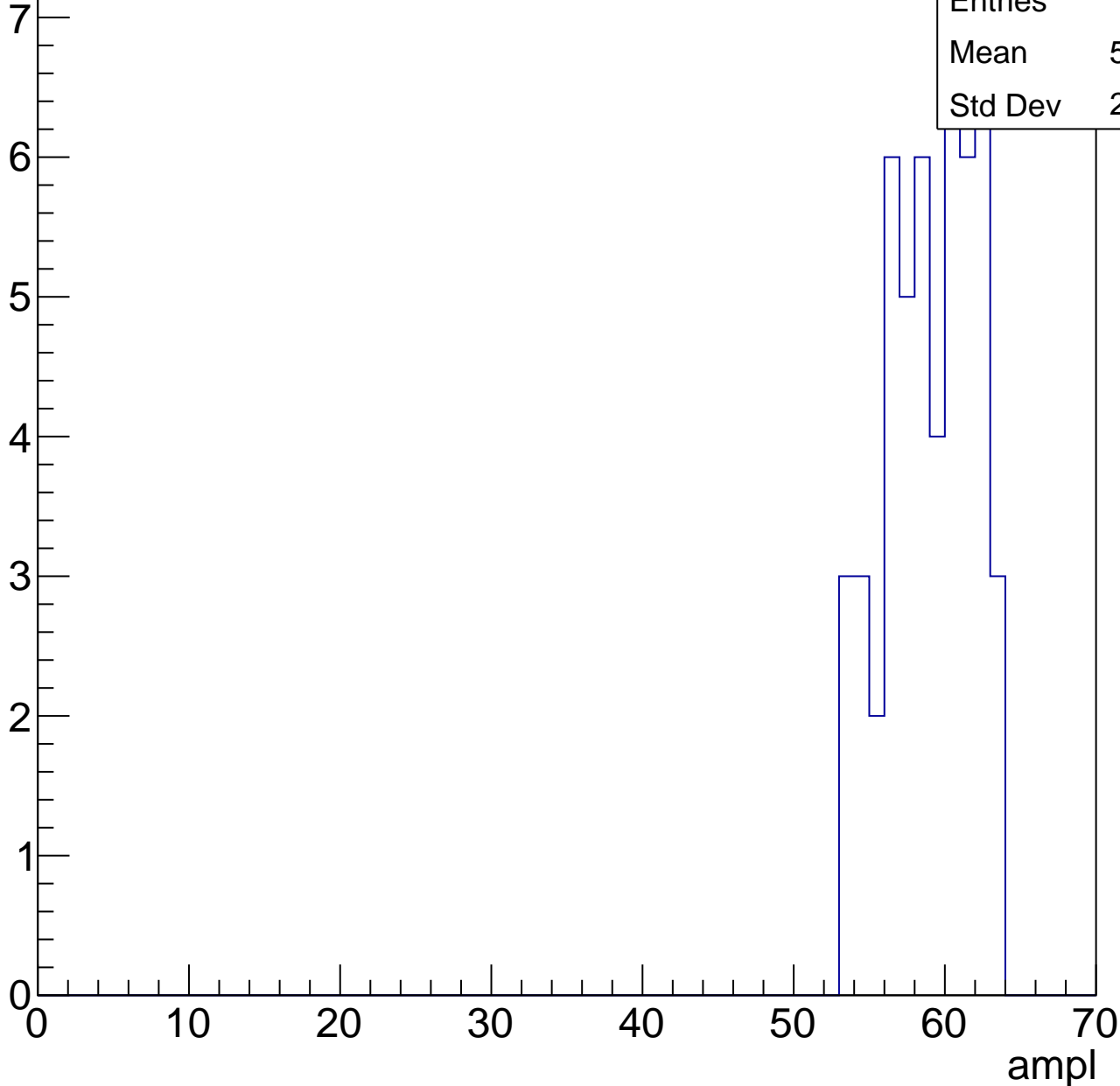


B1L103S, U9-ch89, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

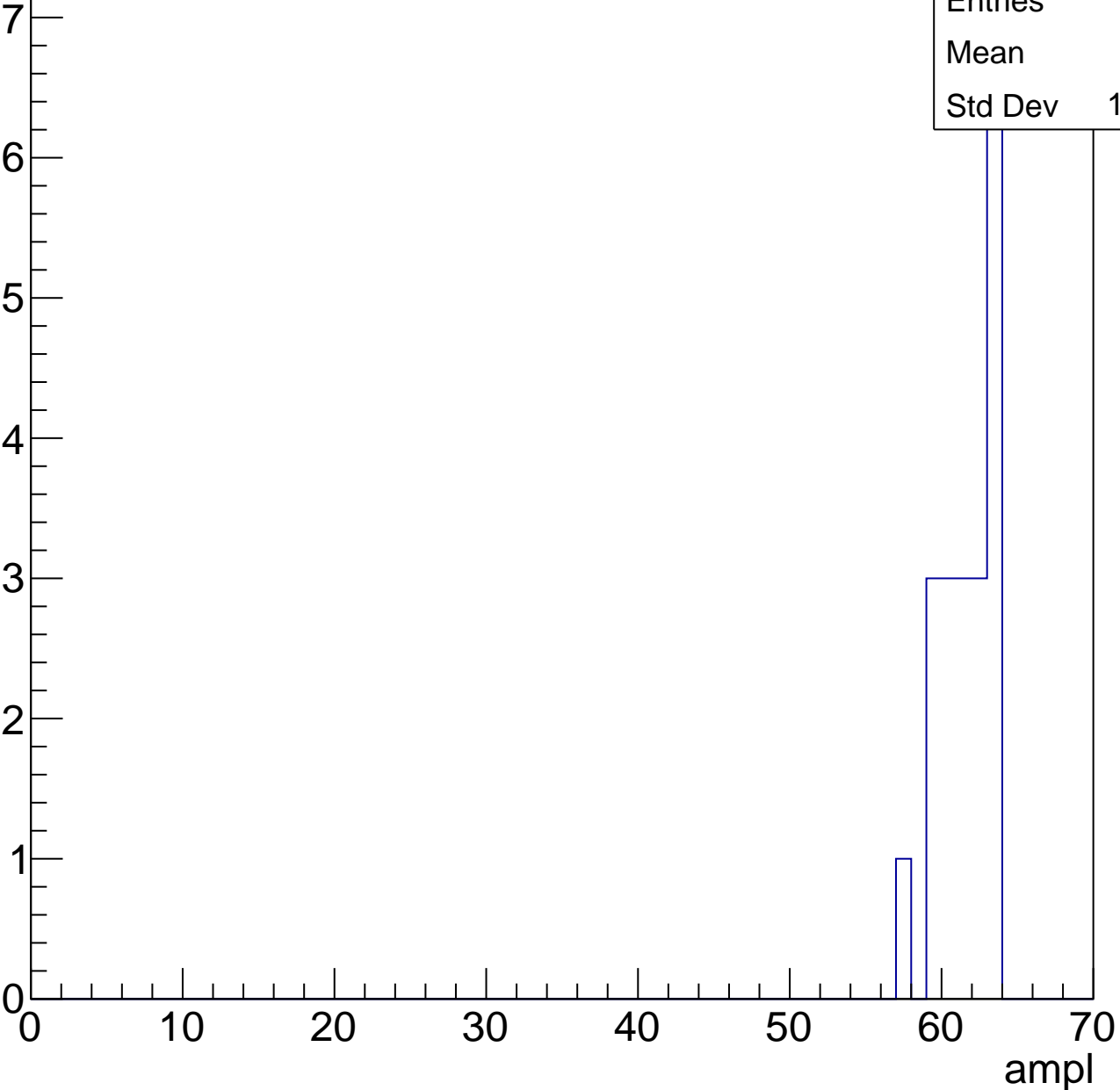
Entries	52
Mean	58.56
Std Dev	2.865



B1L103S, U9-ch89, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



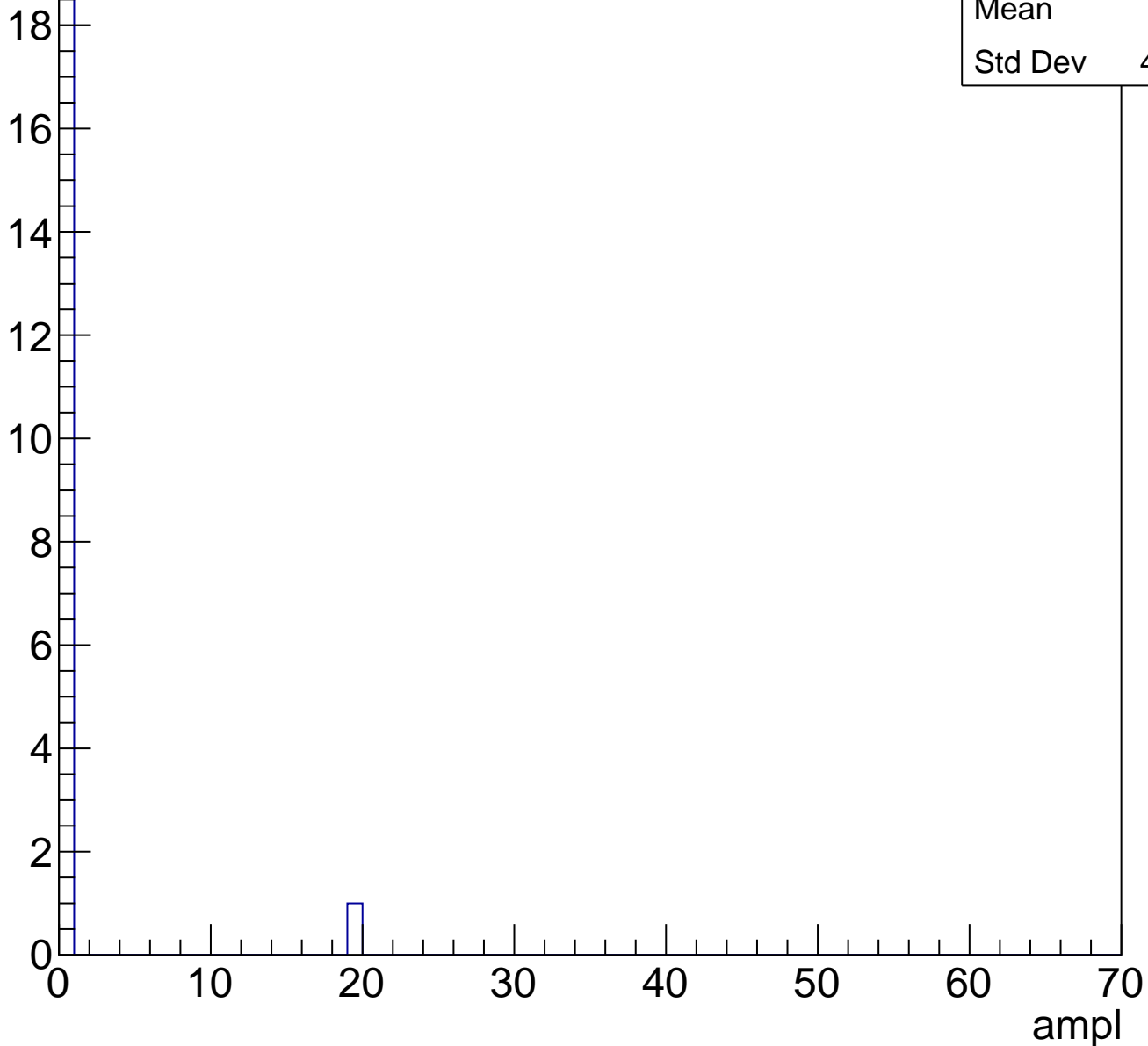
Entries	20
Mean	61.2
Std Dev	1.749

B1L103S, U9-ch89, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	0.95
Std Dev	4.141

Entry

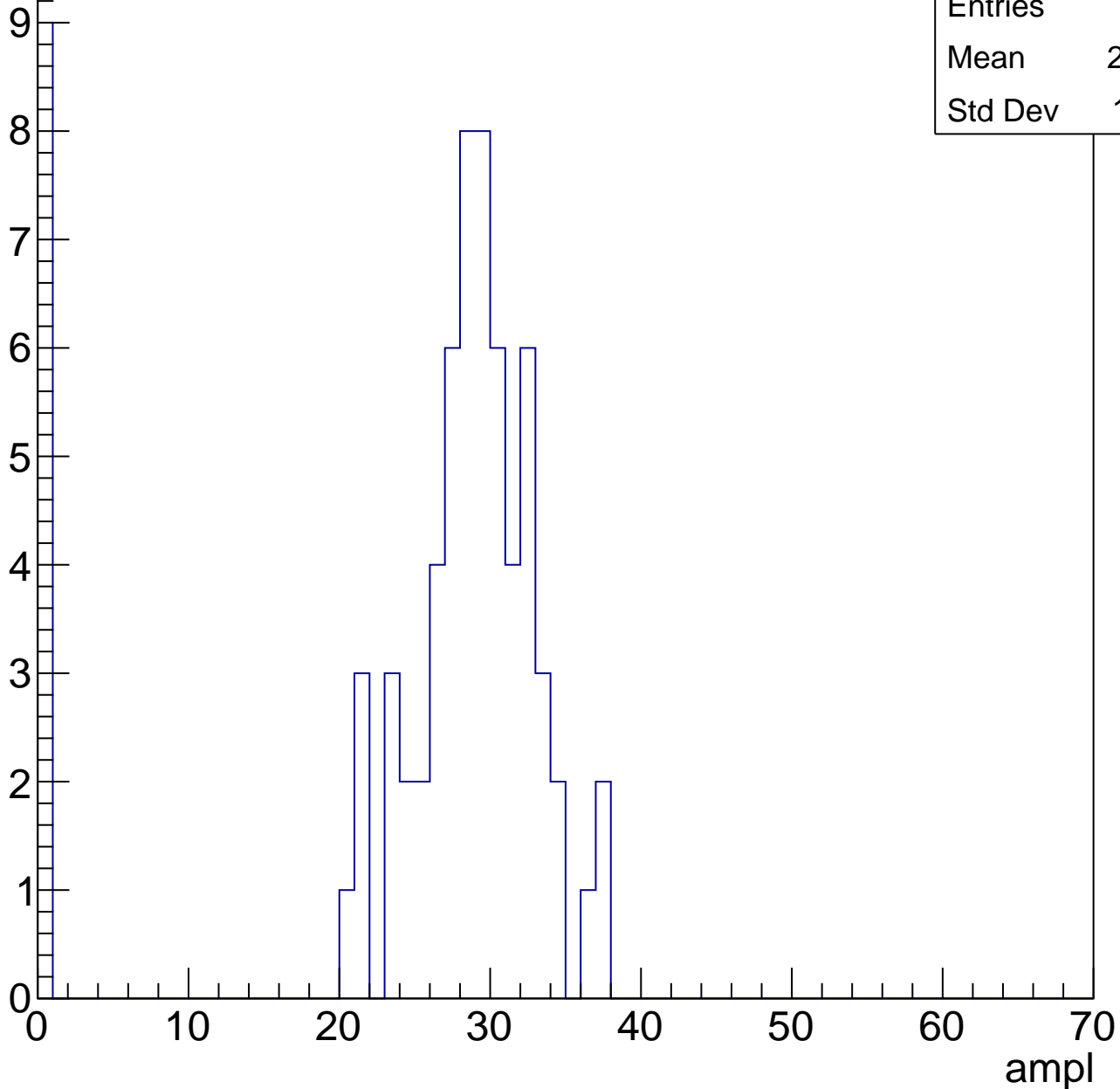


B1L103S, U9-ch90, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

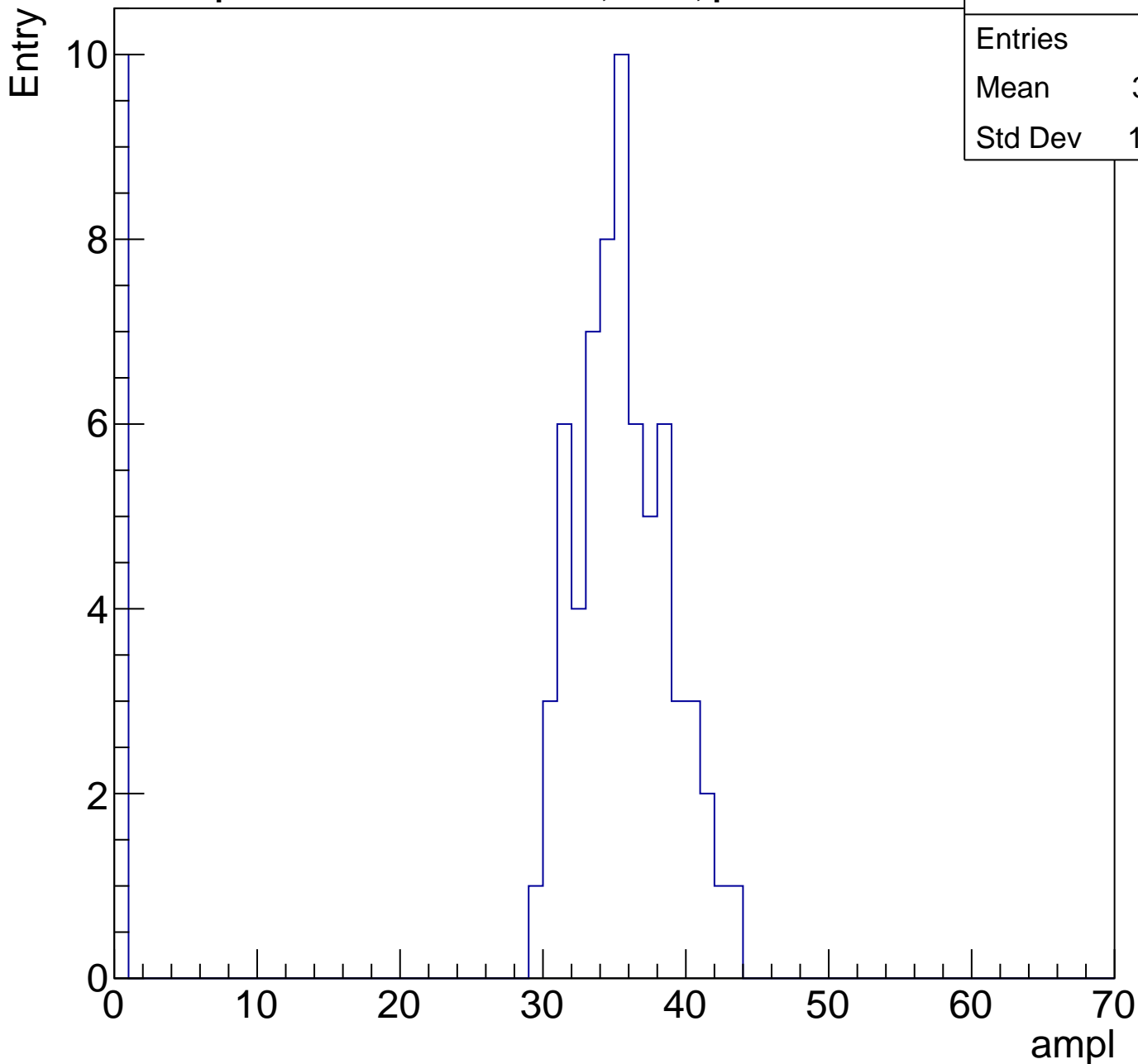
Entries	70
Mean	24.93
Std Dev	10.21



B1L103S, U9-ch90, adc1

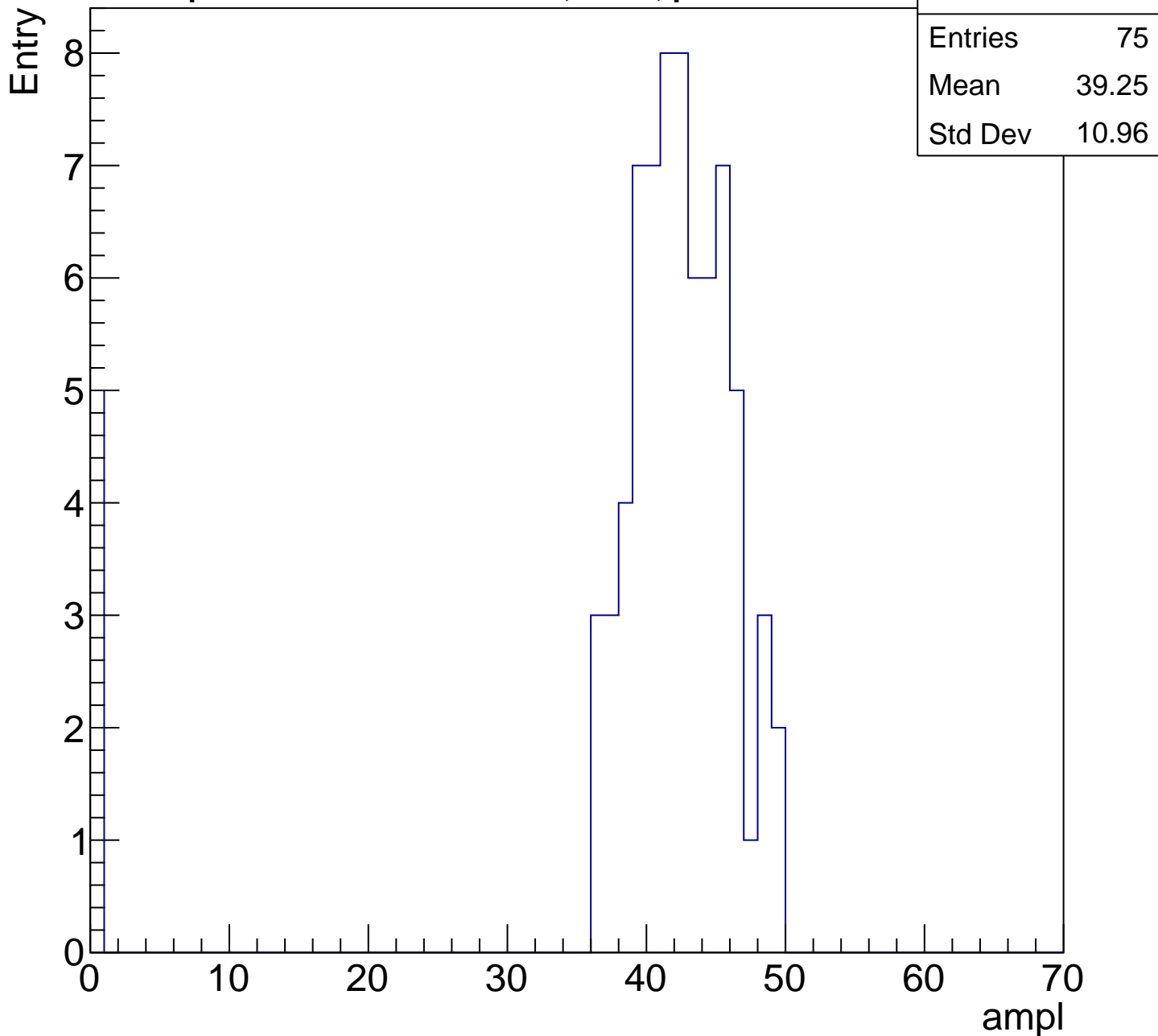
calib_packv5_041523_1651.root, FC#0, port C2

Entries	76
Mean	30.51
Std Dev	12.24



B1L103S, U9-ch90, adc2

calib_packv5_041523_1651.root, FC#0, port C2

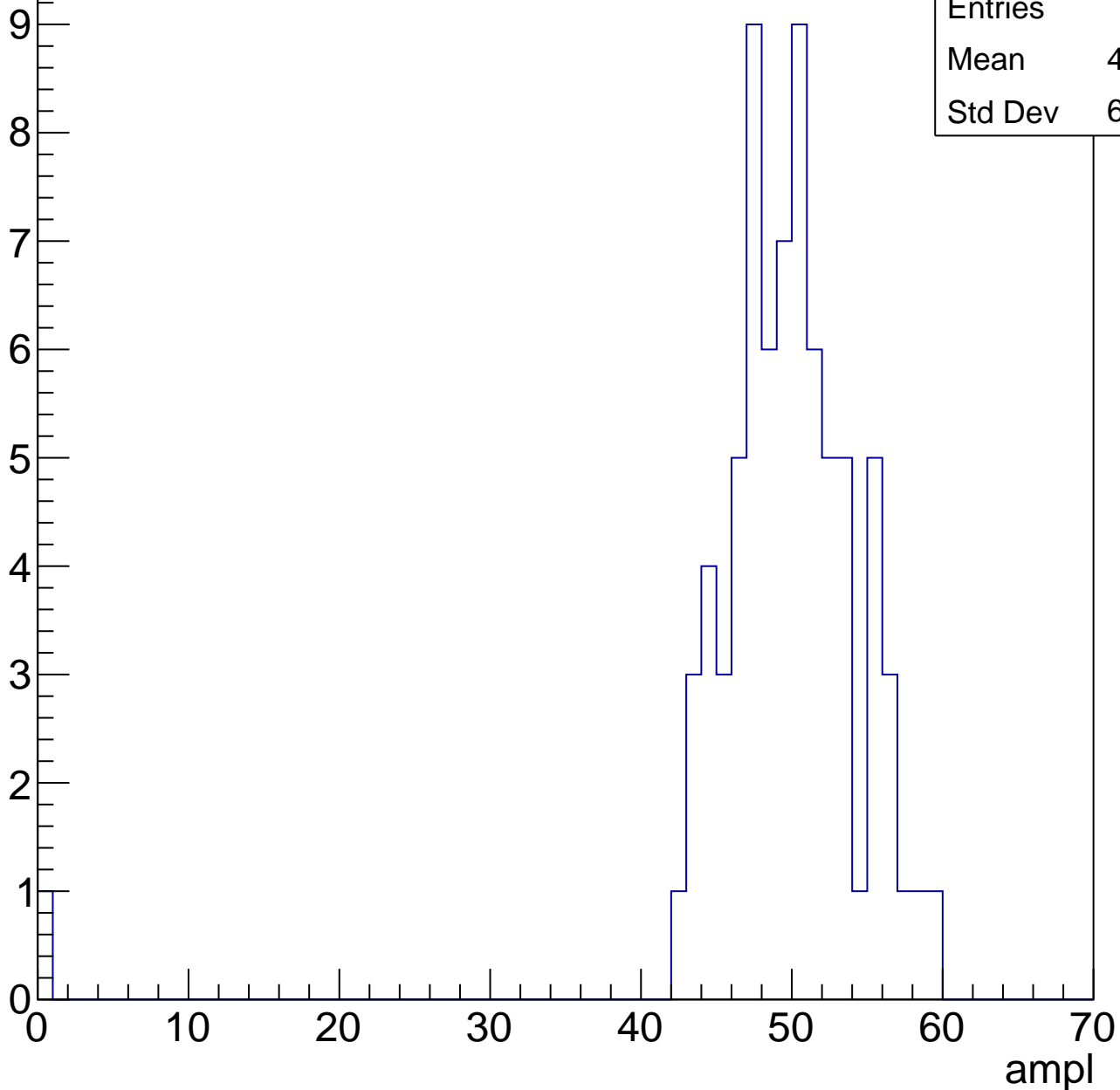


B1L103S, U9-ch90, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	48.92
Std Dev	6.832

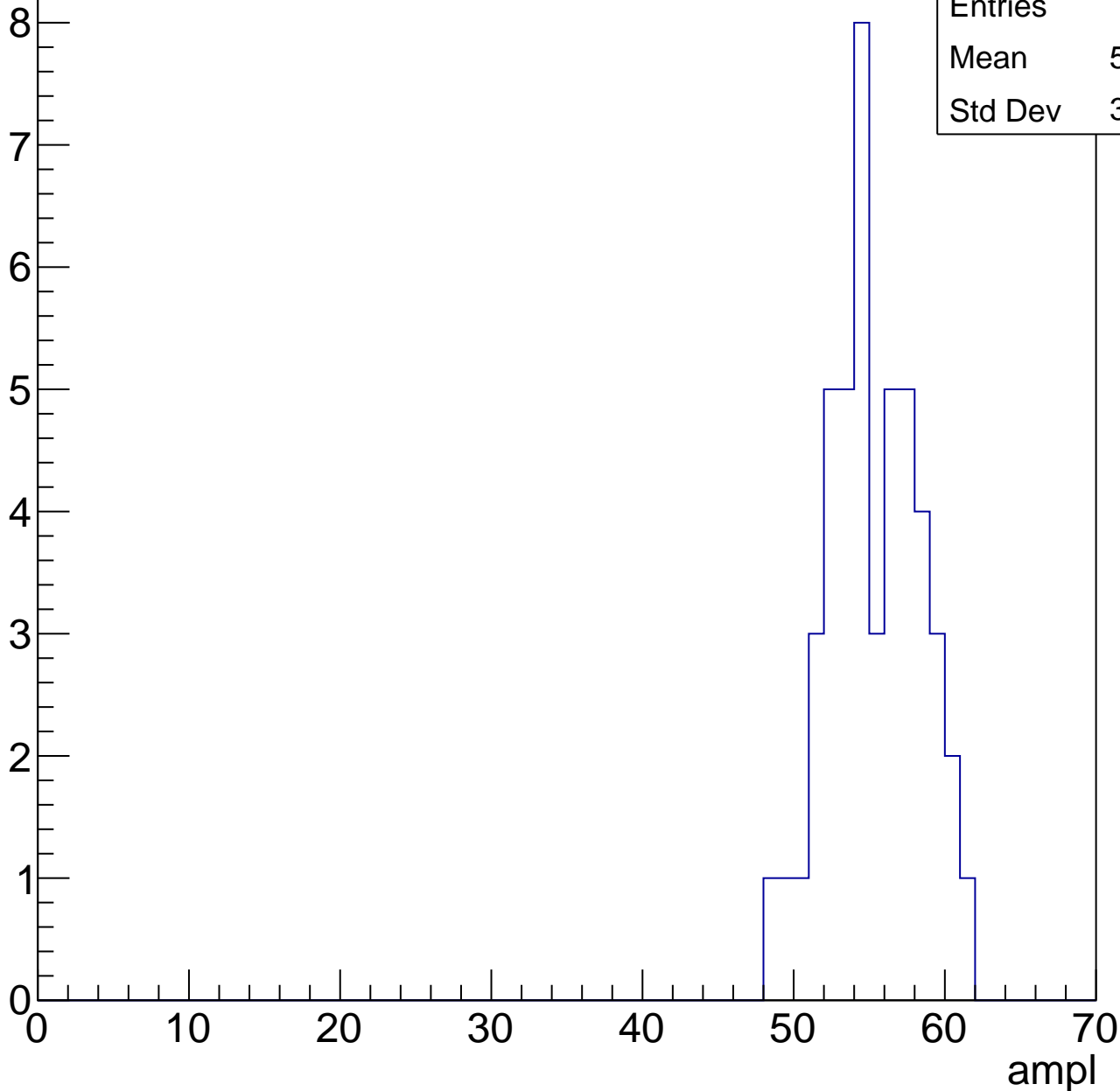


B1L103S, U9-ch90, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	47
Mean	54.83
Std Dev	3.006

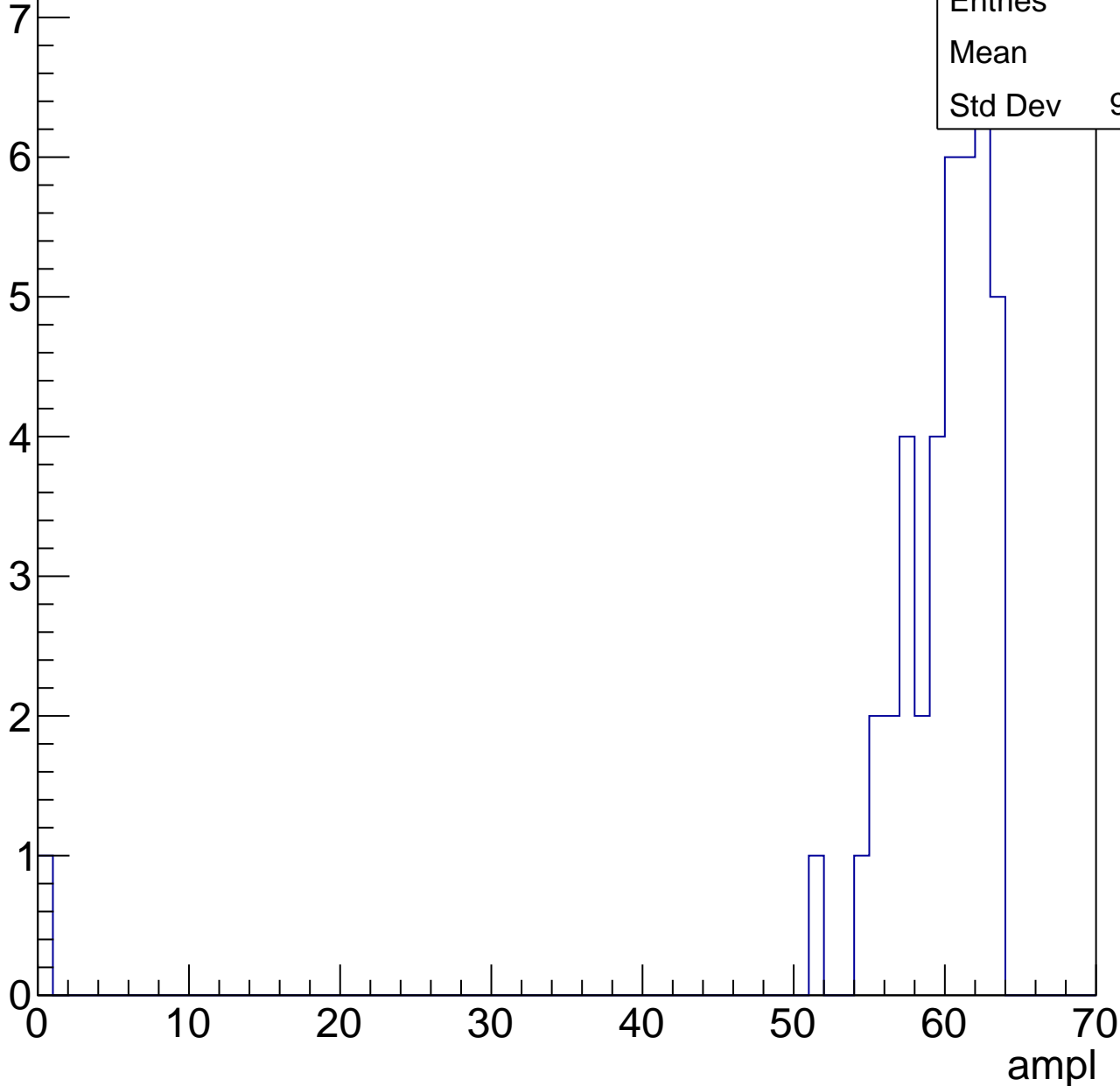


B1L103S, U9-ch90, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	41
Mean	58.1
Std Dev	9.599

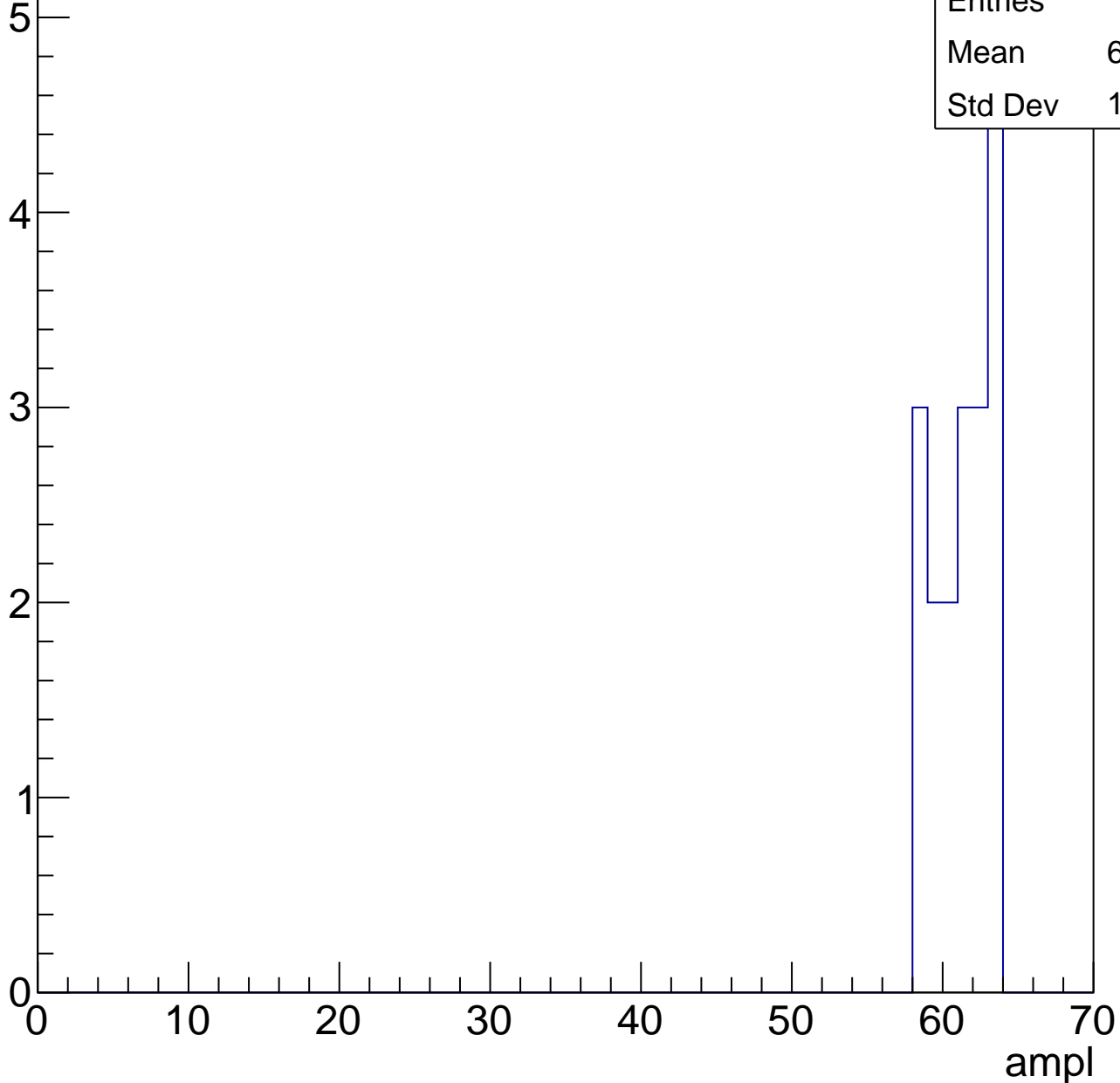


B1L103S, U9-ch90, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	18
Mean	60.89
Std Dev	1.822



B1L103S, U9-ch90, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

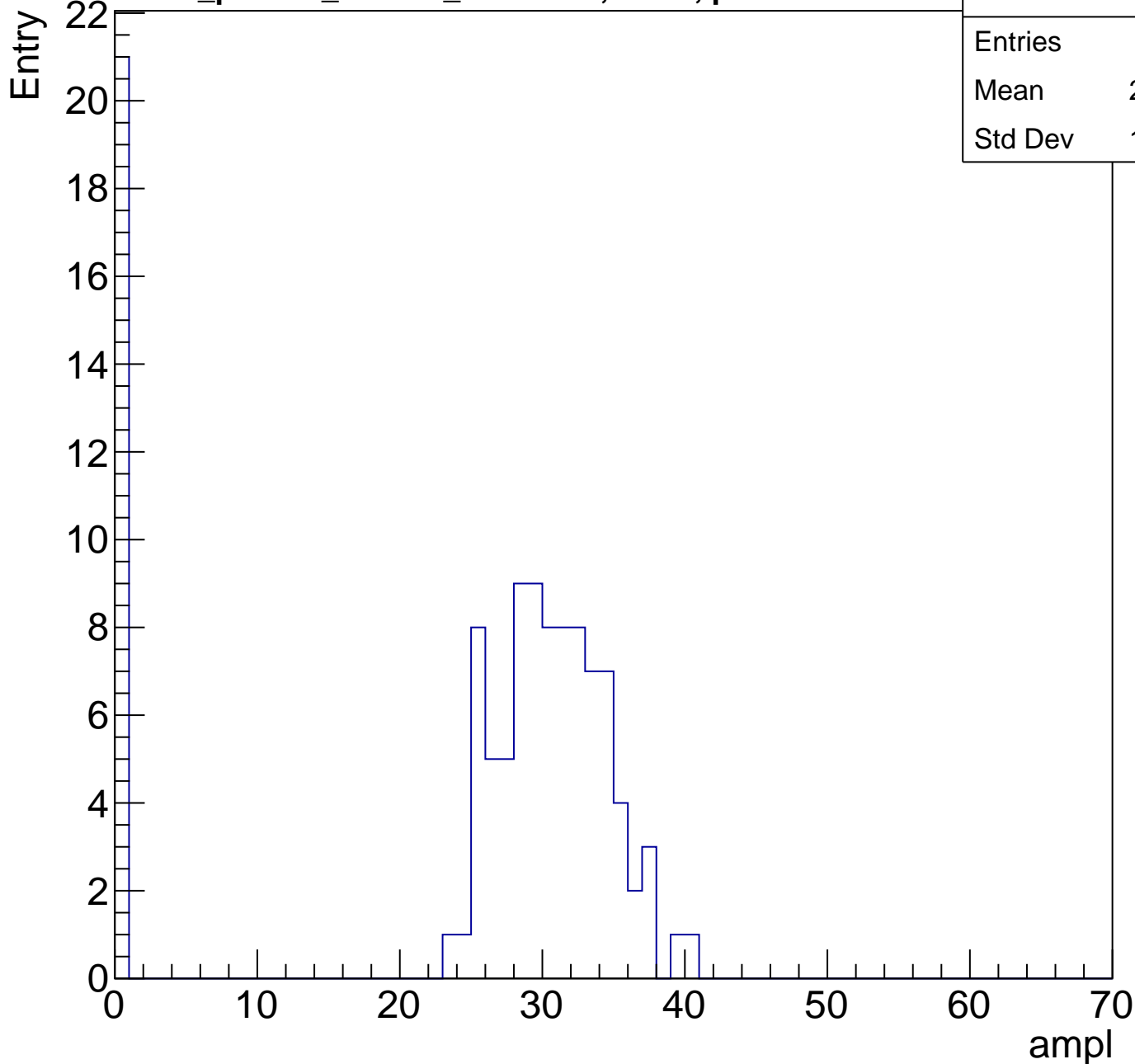
Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U9-ch91, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	108
Mean	24.44
Std Dev	12.45

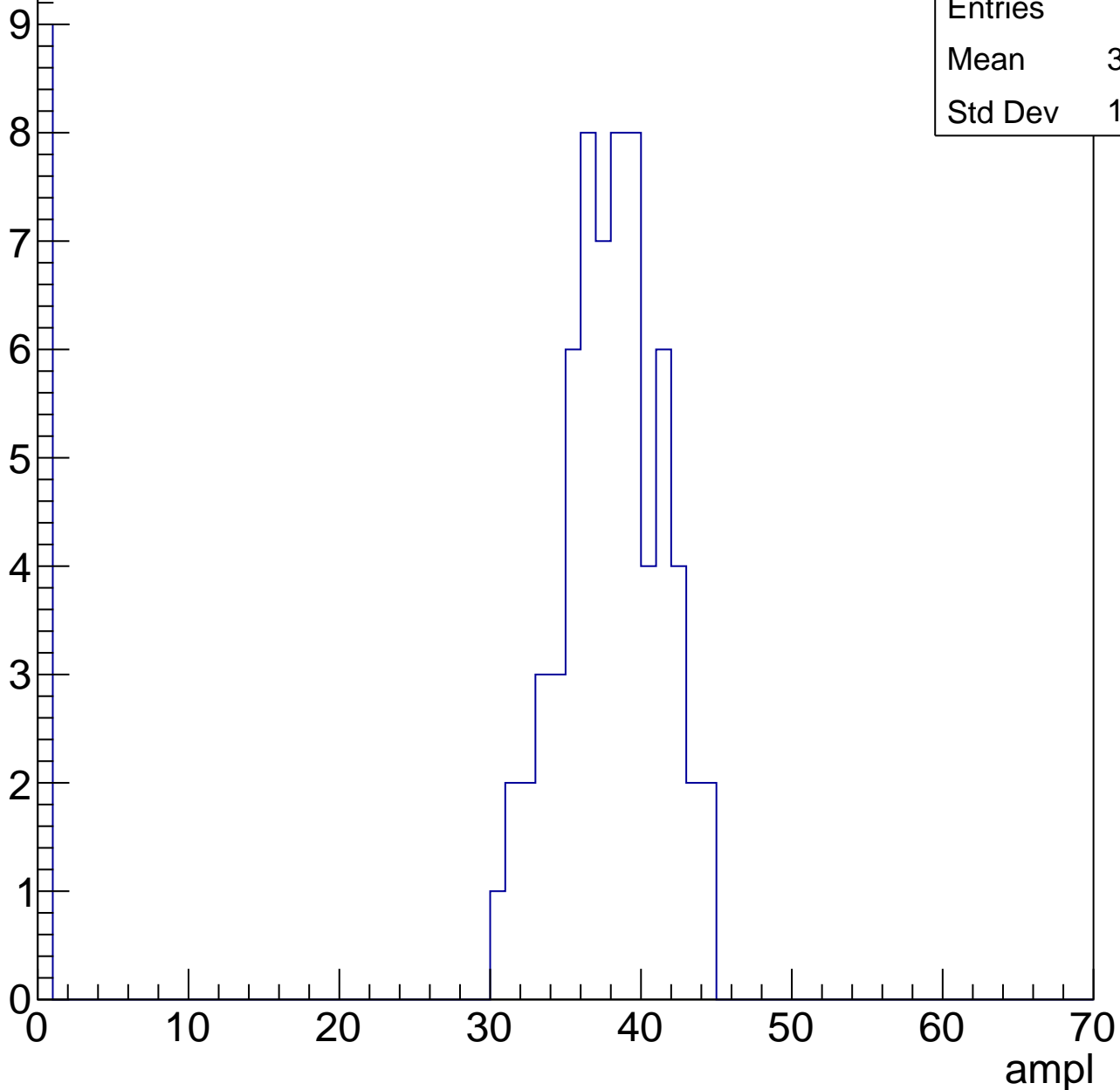


B1L103S, U9-ch91, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

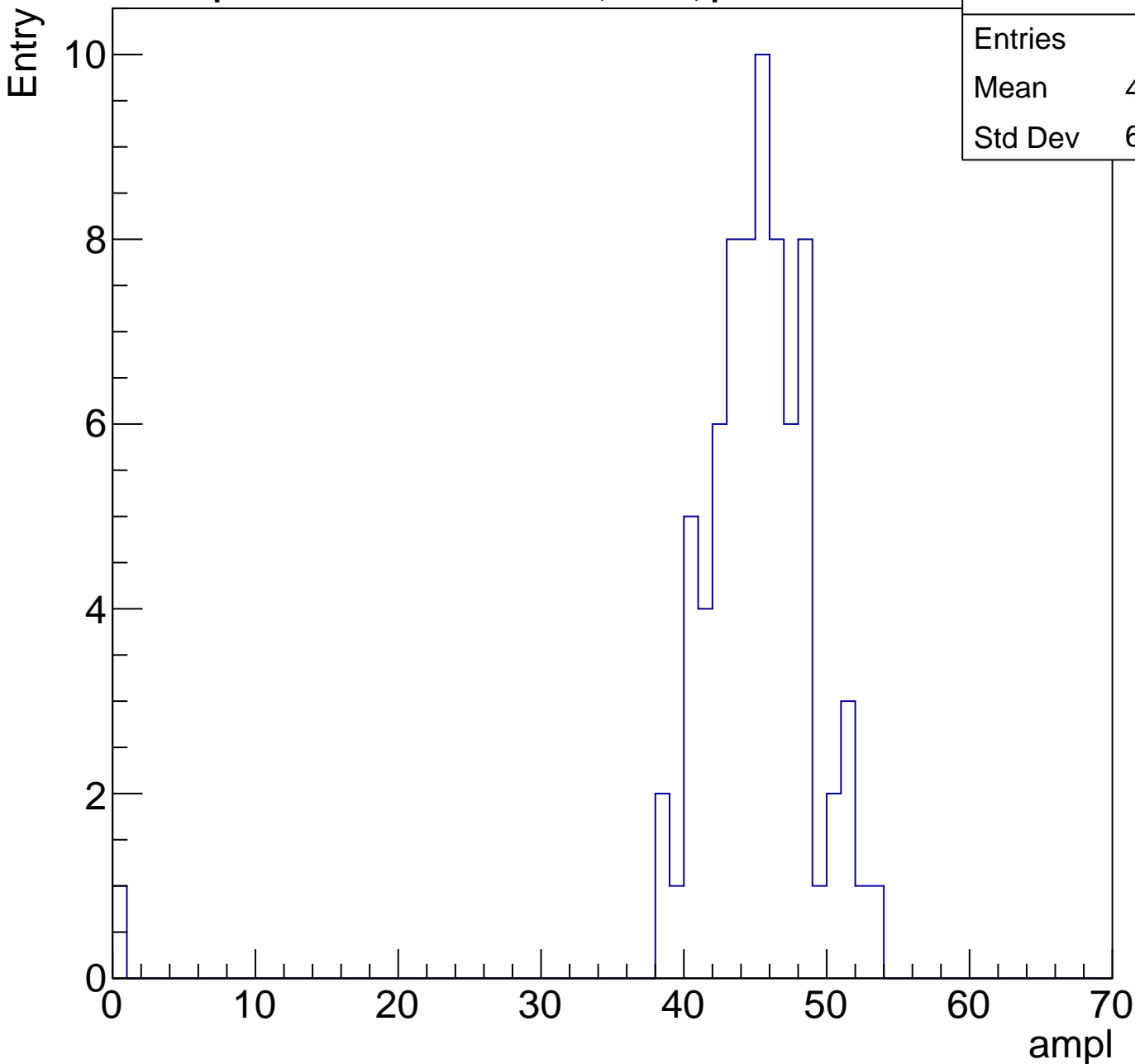
Entries	75
Mean	33.04
Std Dev	12.58



B1L103S, U9-ch91, adc2

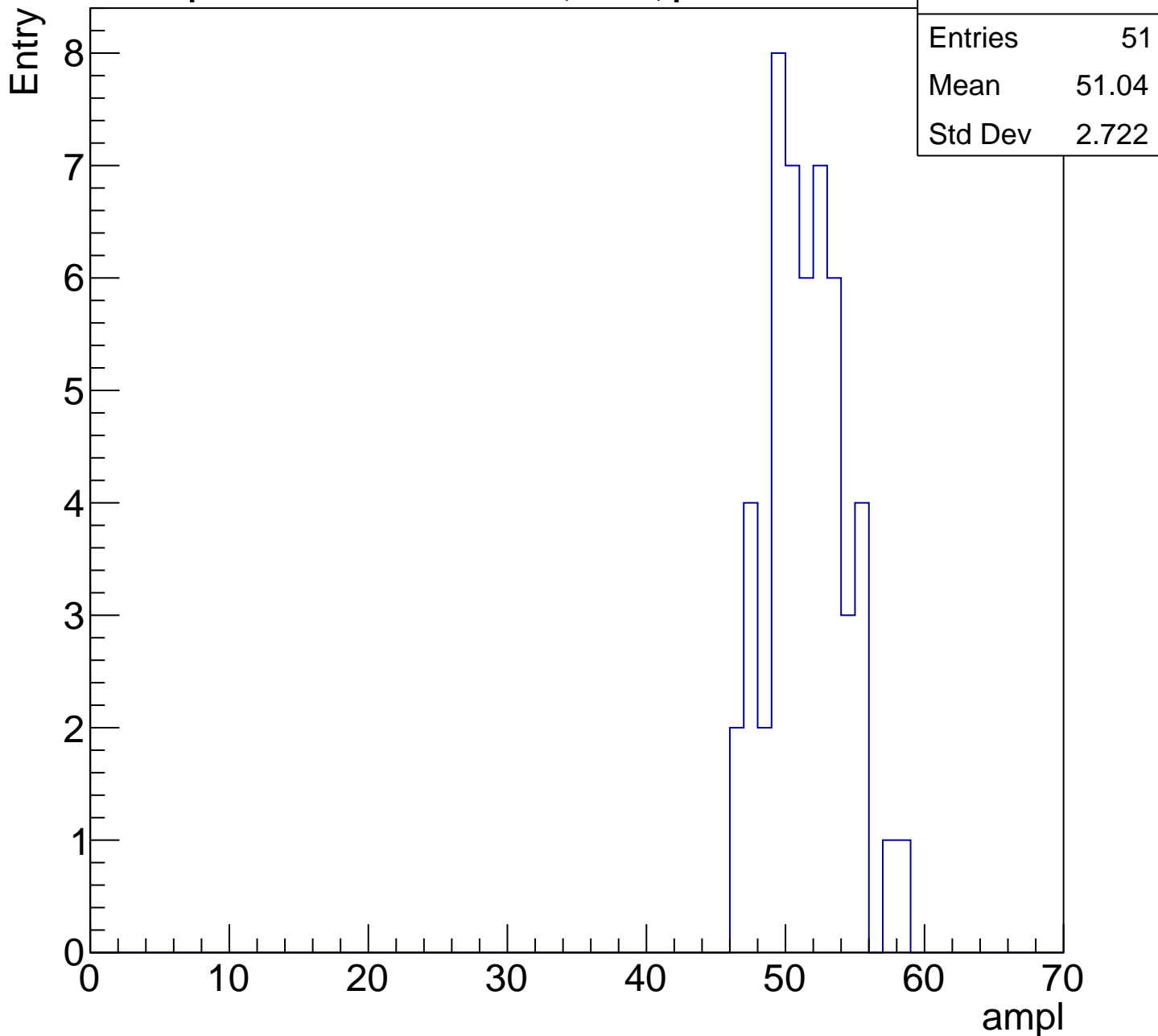
calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	44.24
Std Dev	6.099



B1L103S, U9-ch91, adc3

calib_packv5_041523_1651.root, FC#0, port C2

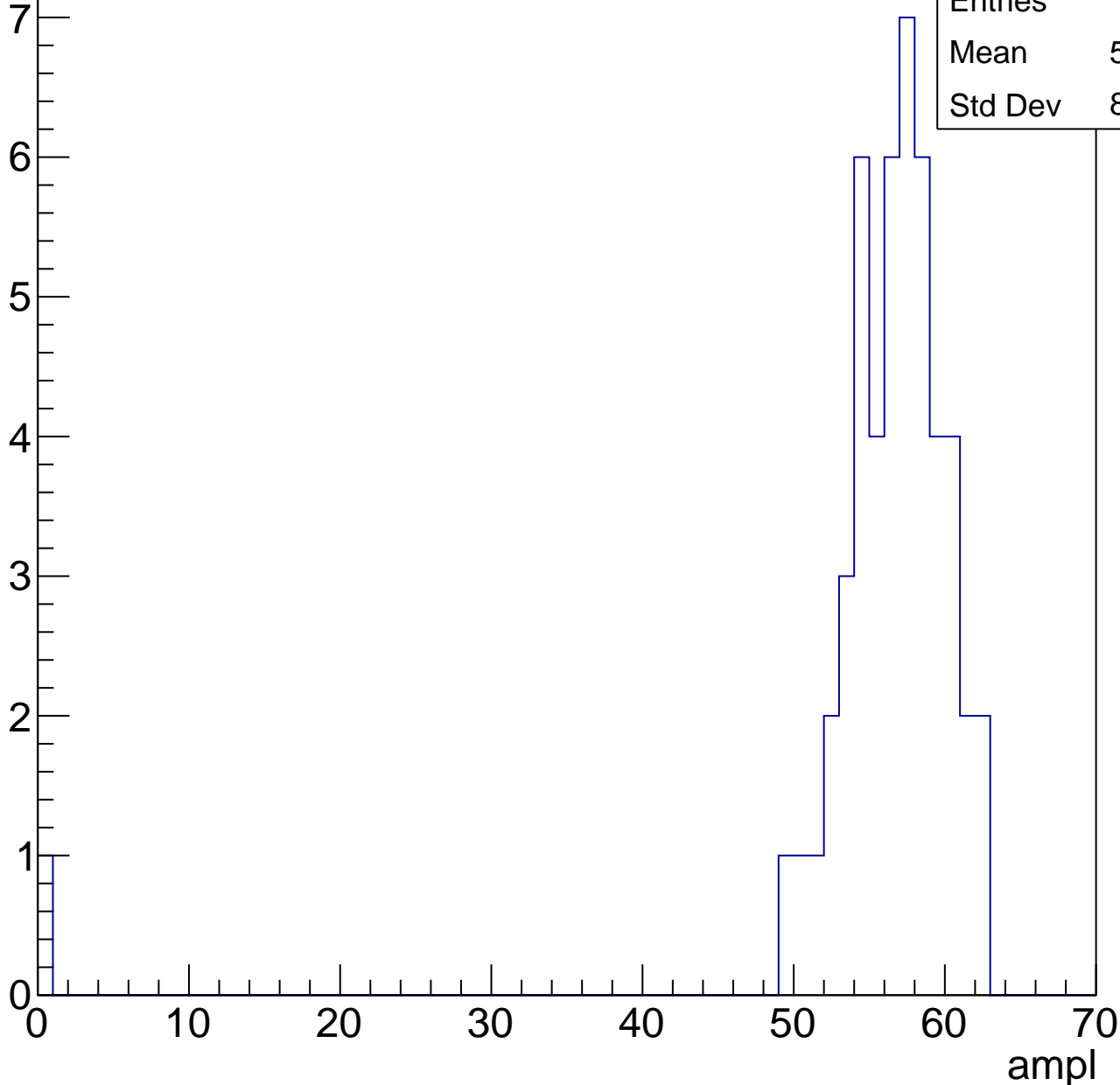


B1L103S, U9-ch91, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	55.24
Std Dev	8.435

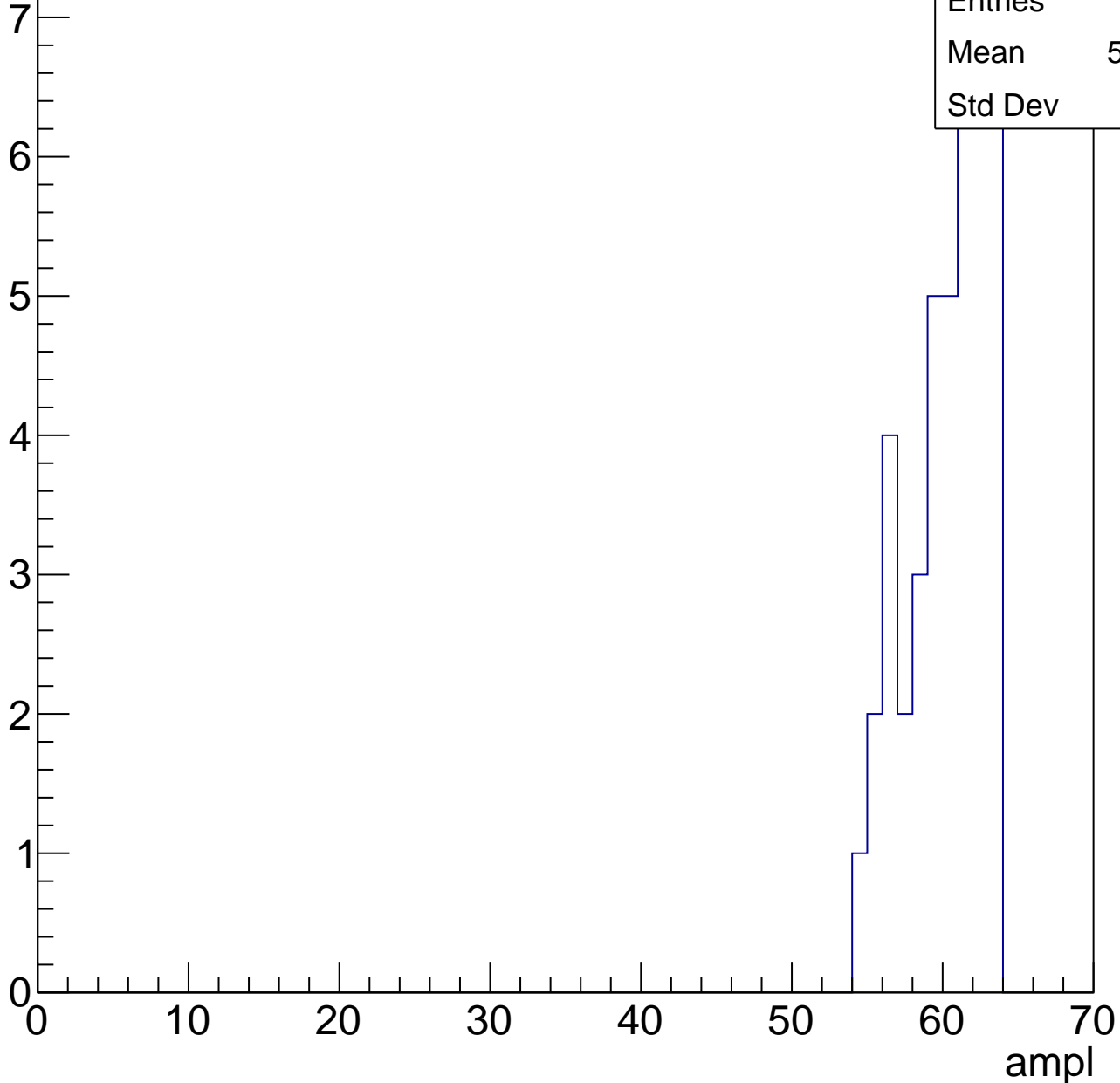


B1L103S, U9-ch91, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

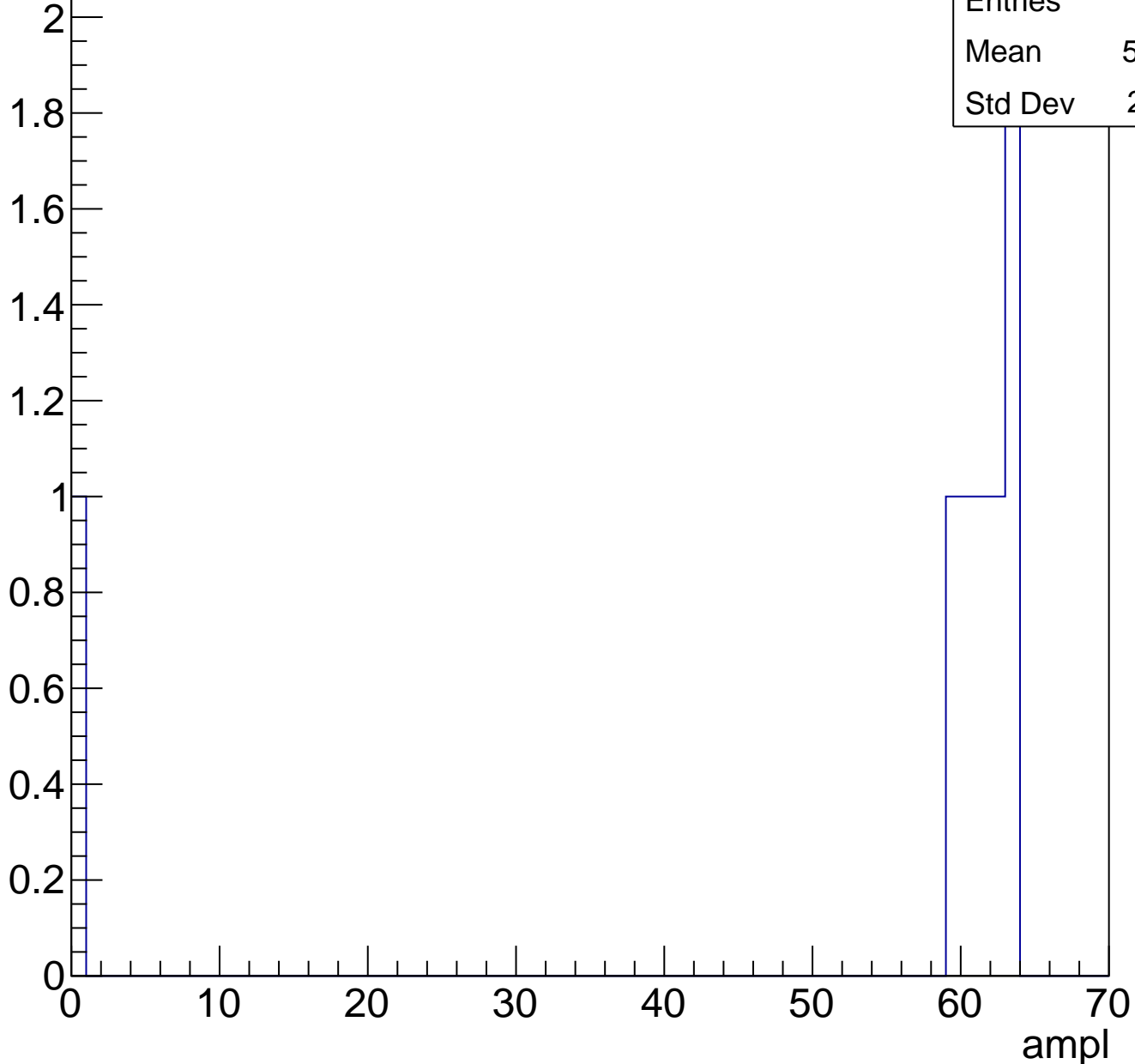
Entries	43
Mean	59.84
Std Dev	2.56



B1L103S, U9-ch91, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	7
Mean	52.57
Std Dev	21.51

B1L103S, U9-ch91, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

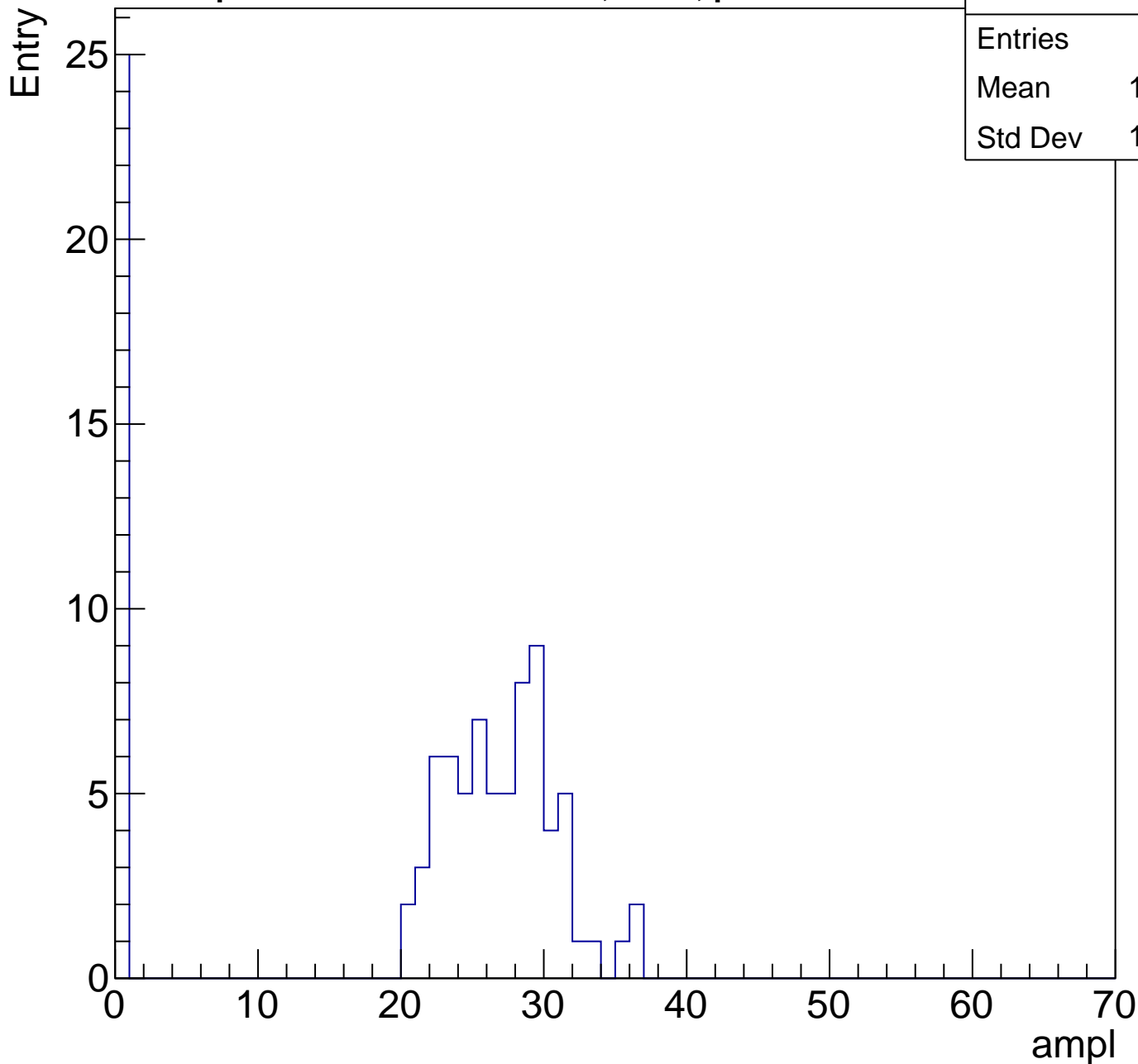
Entry



B1L103S, U9-ch92, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	95
Mean	19.63
Std Dev	12.16

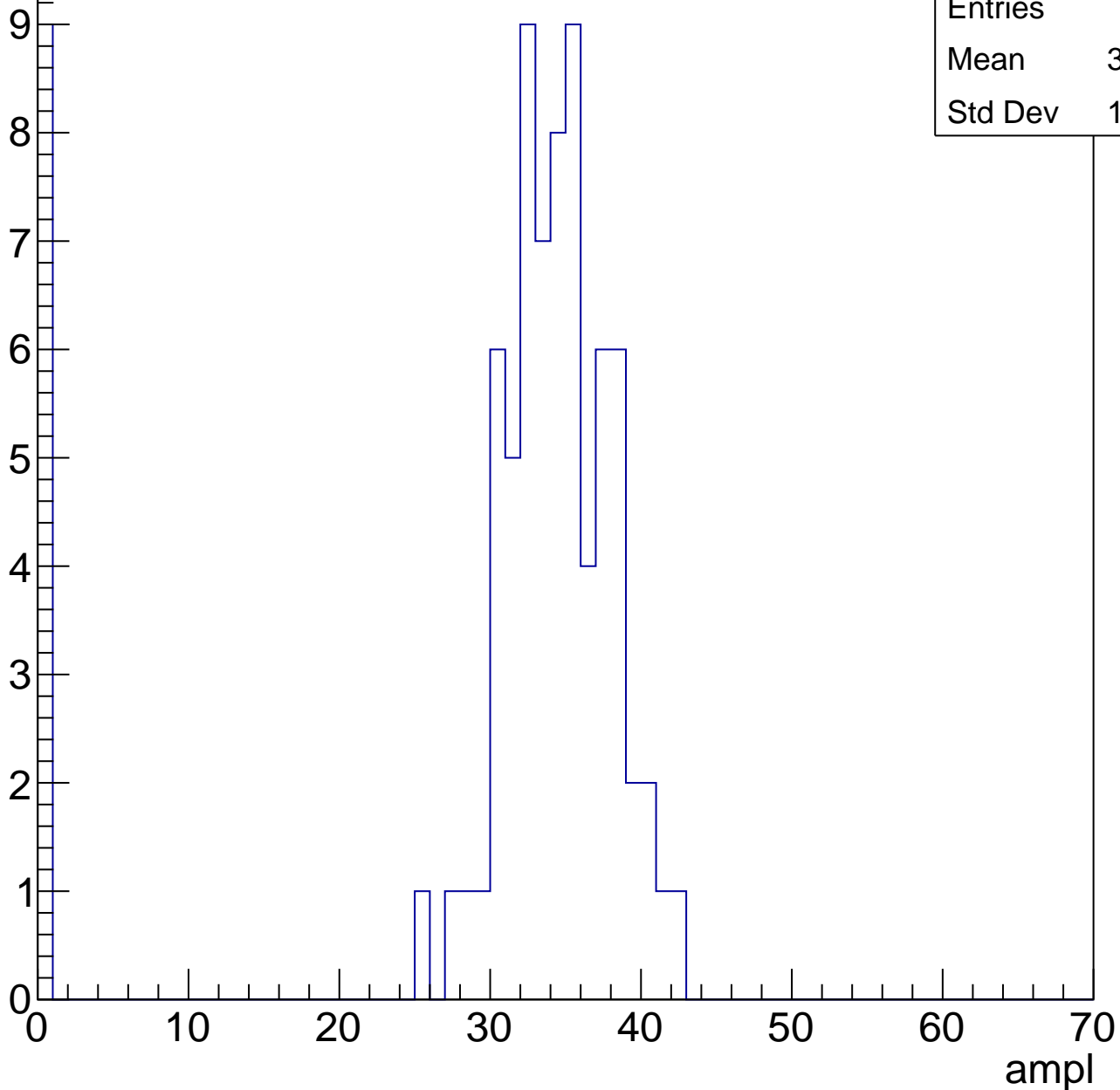


B1L103S, U9-ch92, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	79
Mean	30.19
Std Dev	11.27

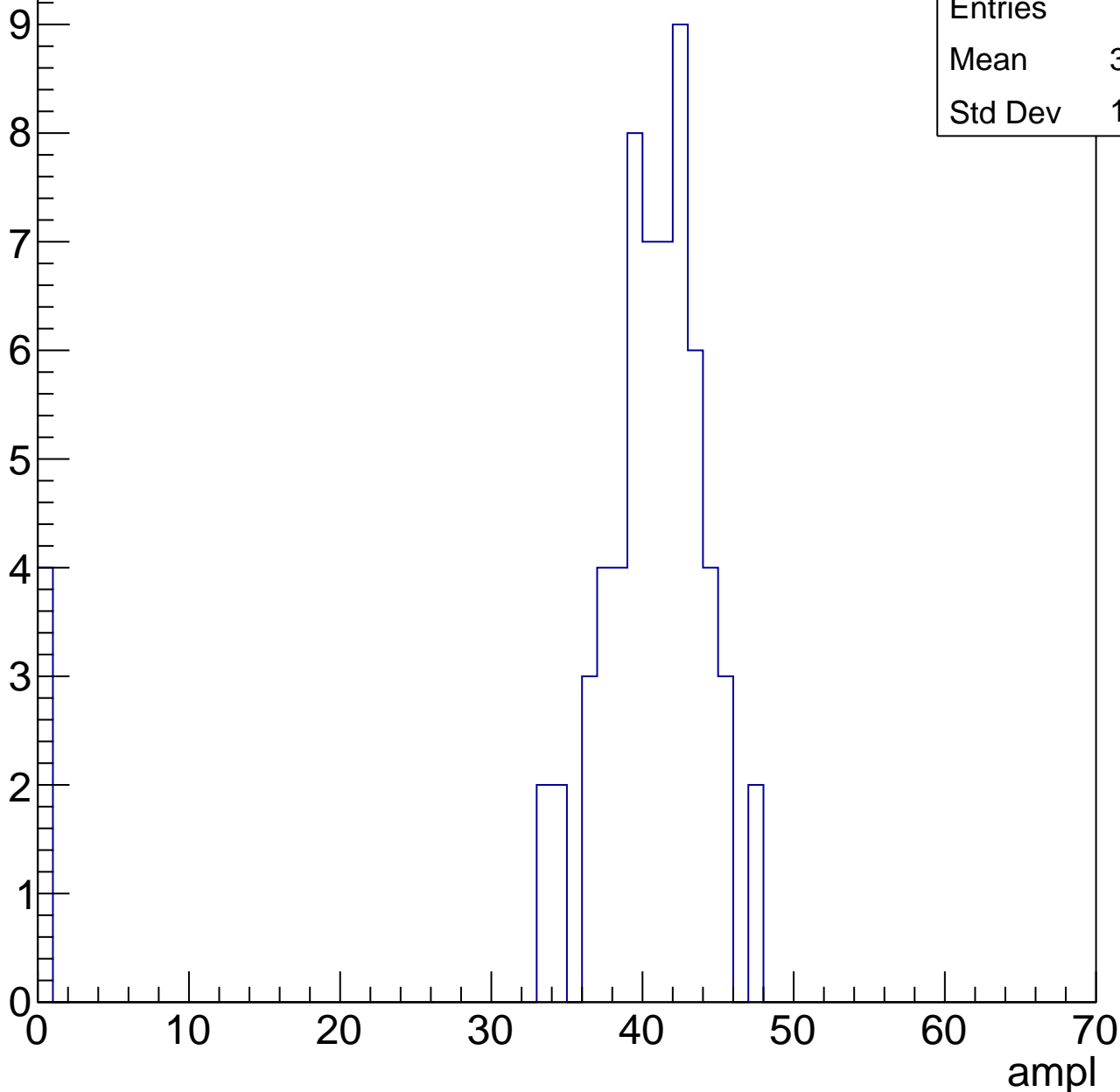


B1L103S, U9-ch92, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	37.88
Std Dev	10.17



B1L103S, U9-ch92, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	47.12
Std Dev	6.435

Entry

10

8

6

4

2

0

0

10

20

30

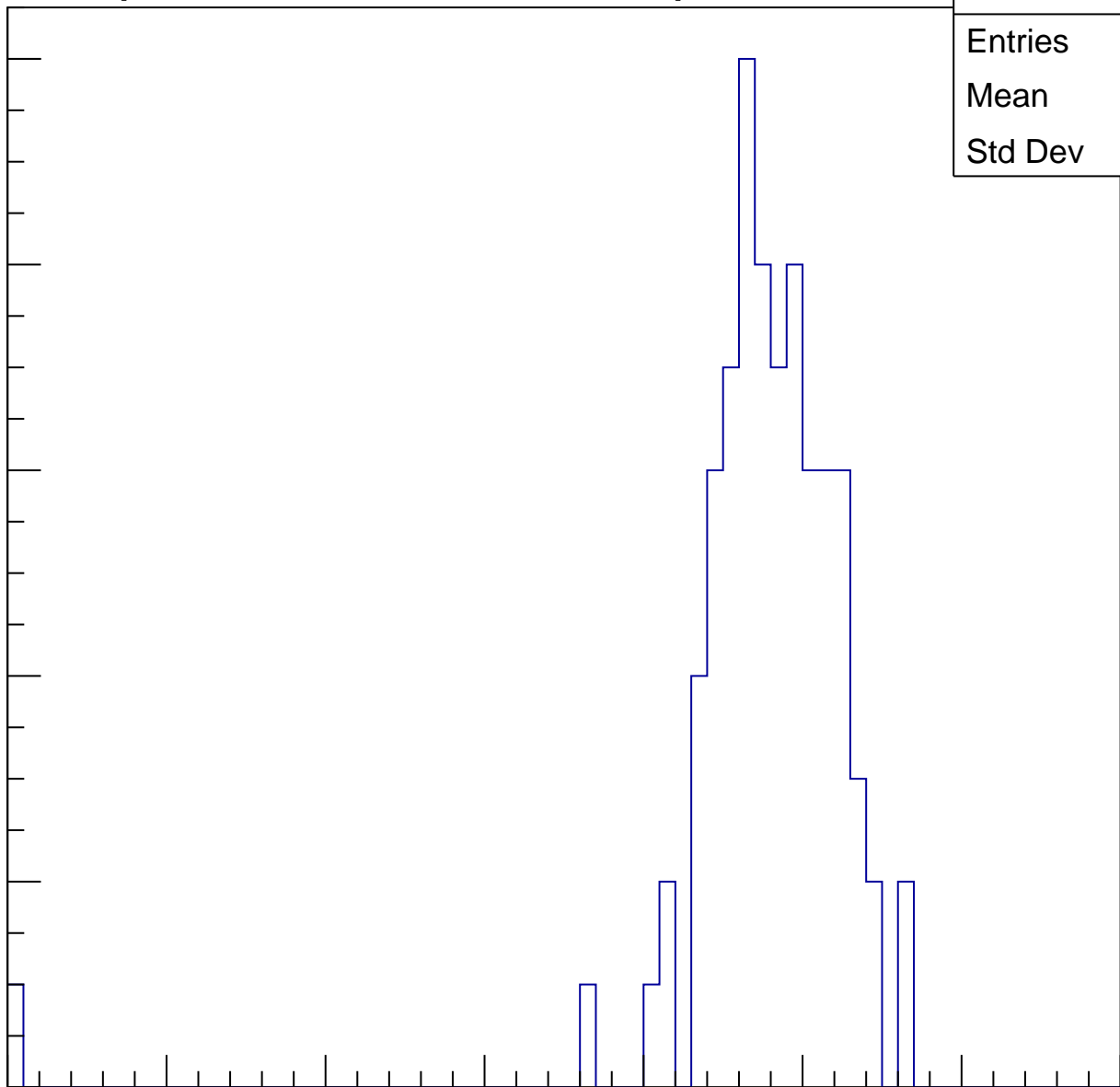
40

50

60

70

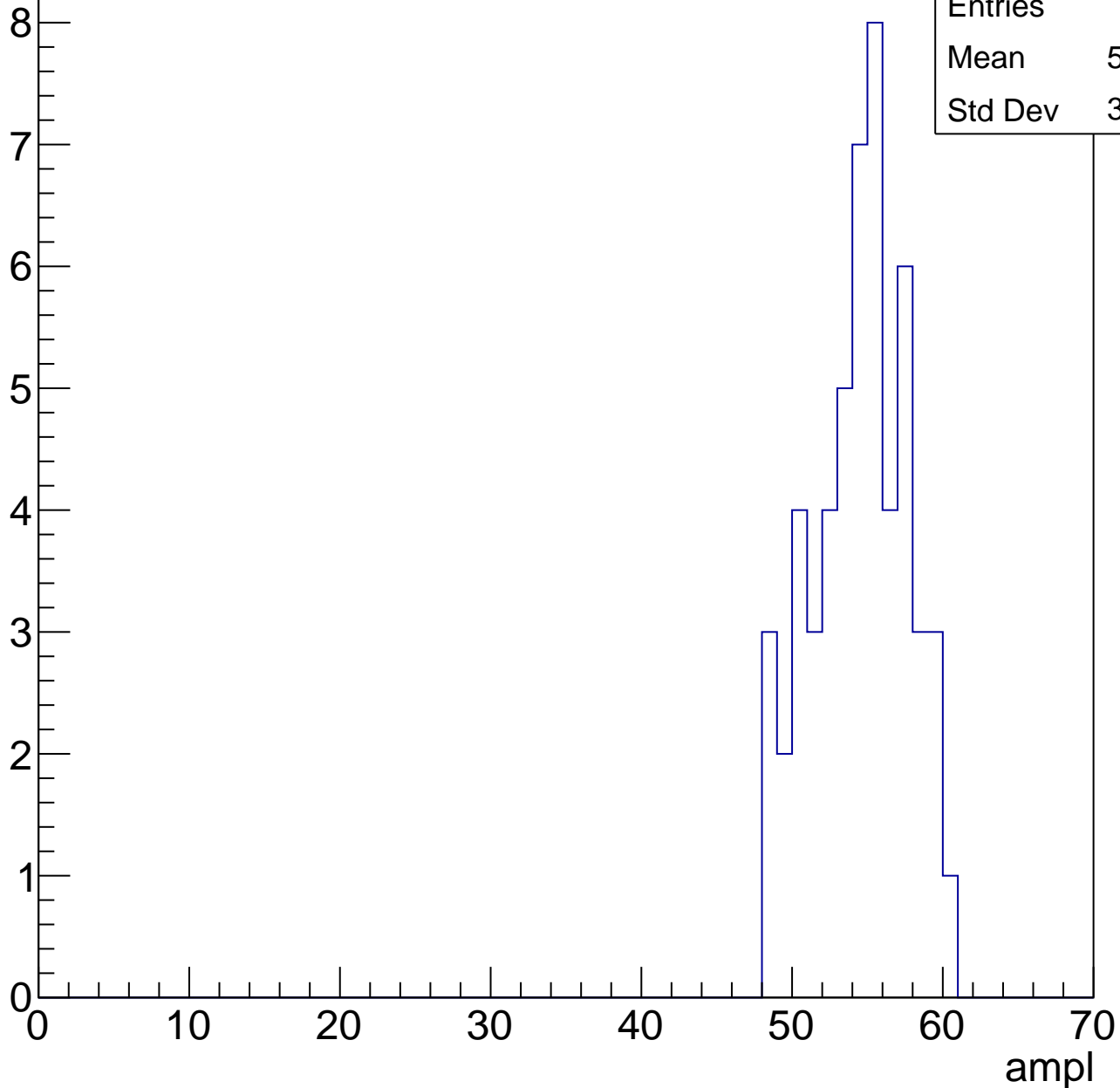
ampl



B1L103S, U9-ch92, adc4

calib_packv5_041523_1651.root, FC#0, port C2

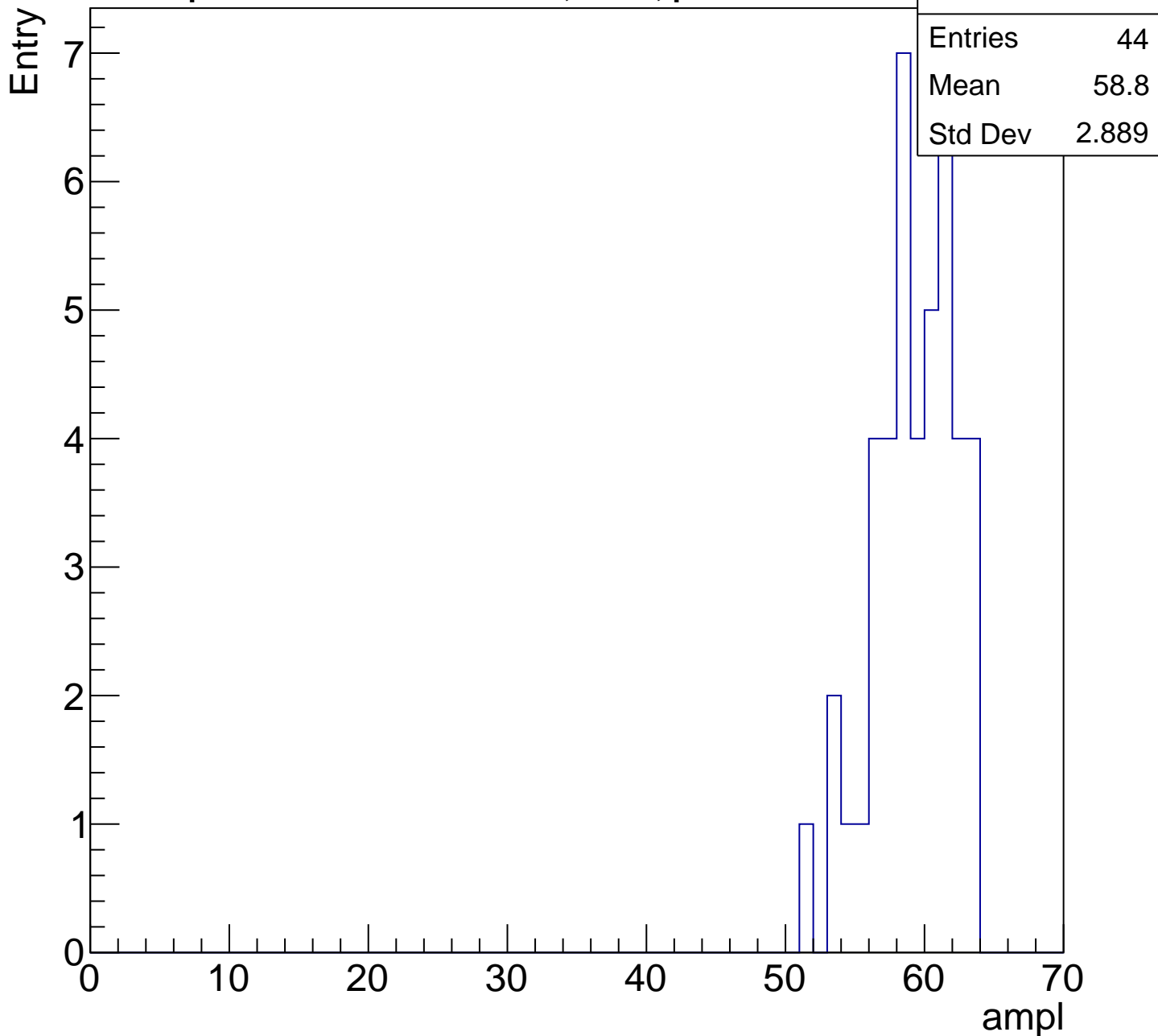
Entry



Entries	53
Mean	54.02
Std Dev	3.093

B1L103S, U9-ch92, adc5

calib_packv5_041523_1651.root, FC#0, port C2

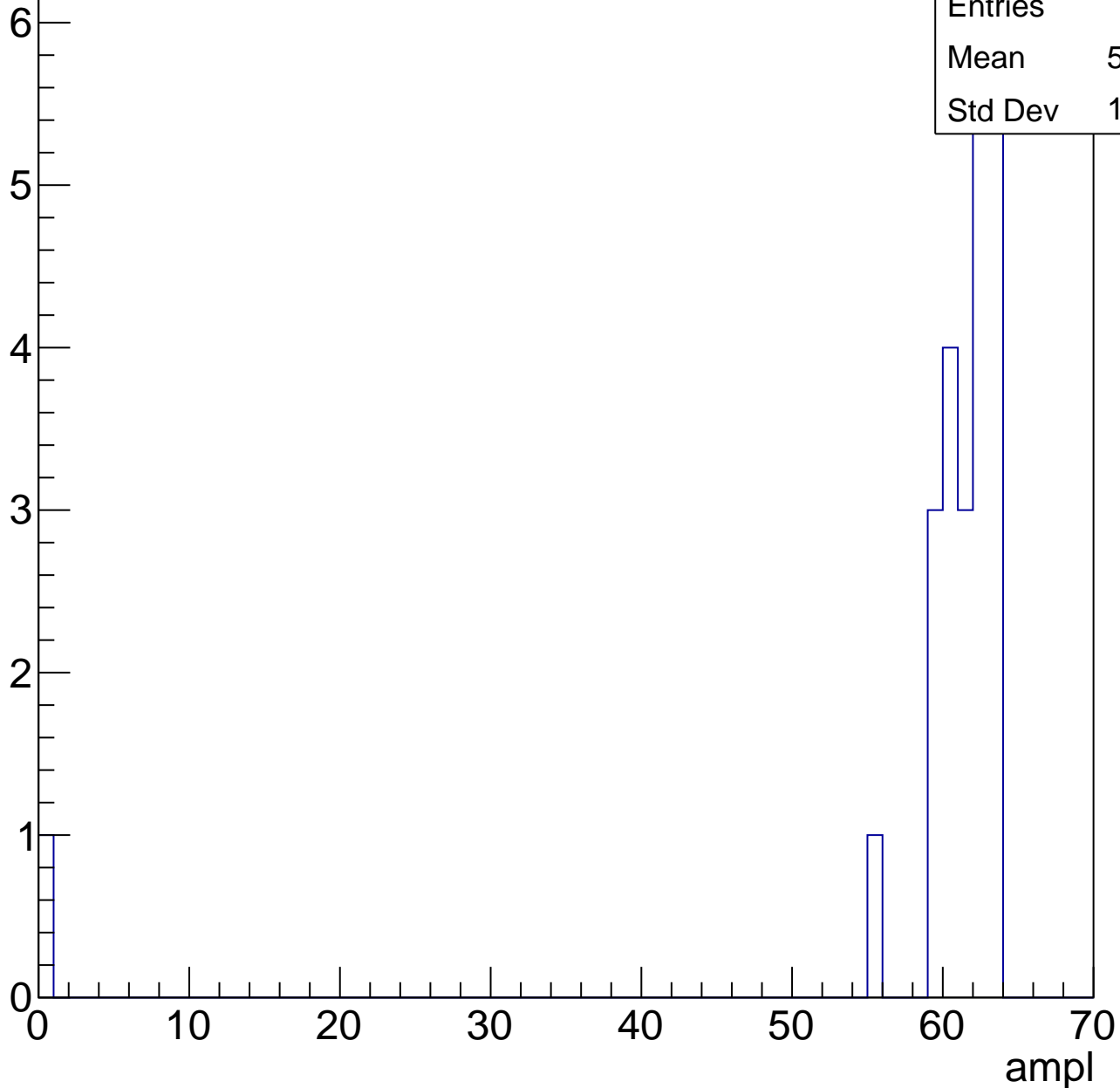


B1L103S, U9-ch92, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	24
Mean	58.54
Std Dev	12.35



B1L103S, U9-ch92, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

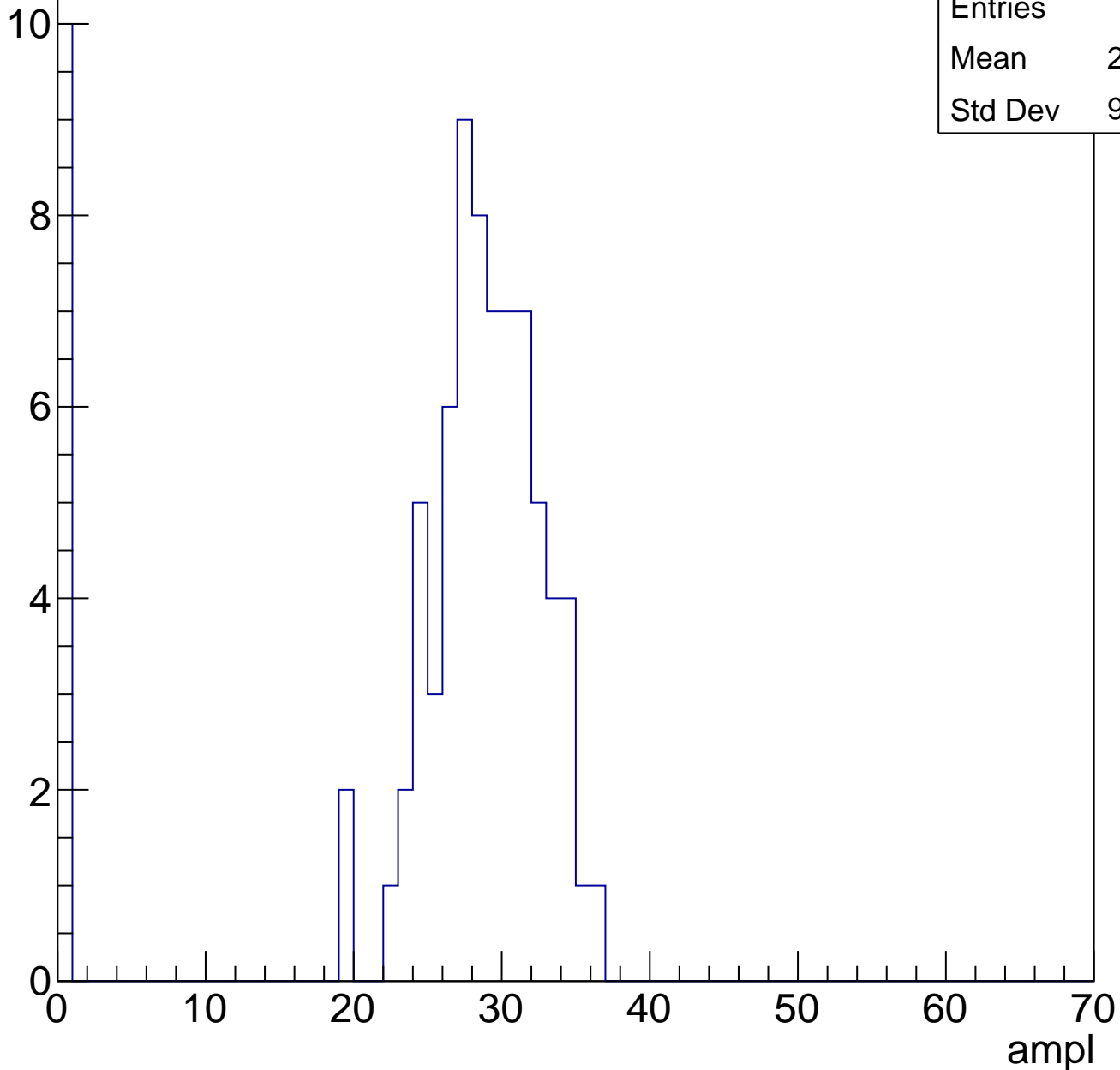


B1L103S, U9-ch93, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	25.04
Std Dev	9.904

Entry

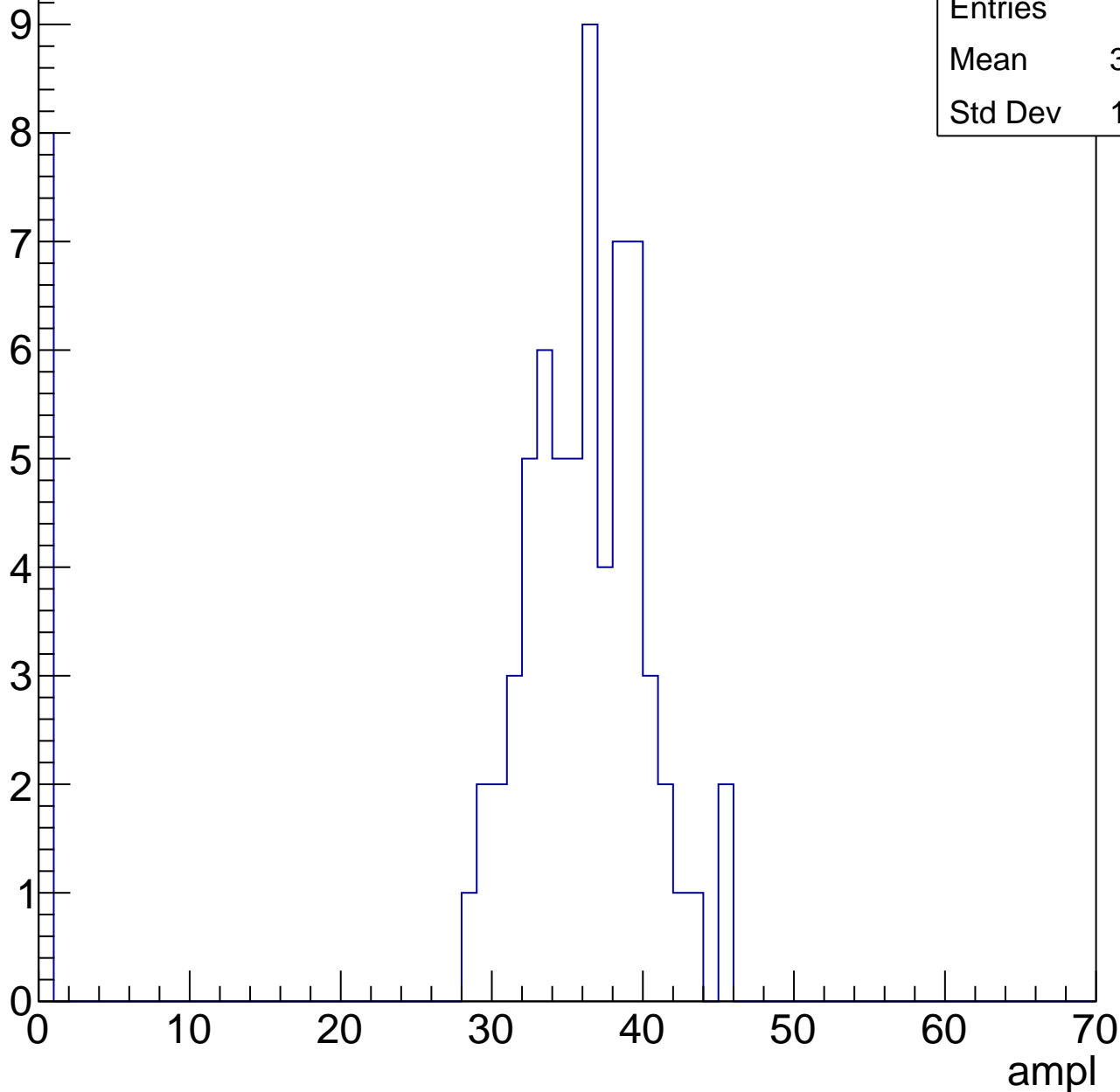


B1L103S, U9-ch93, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	31.92
Std Dev	11.74

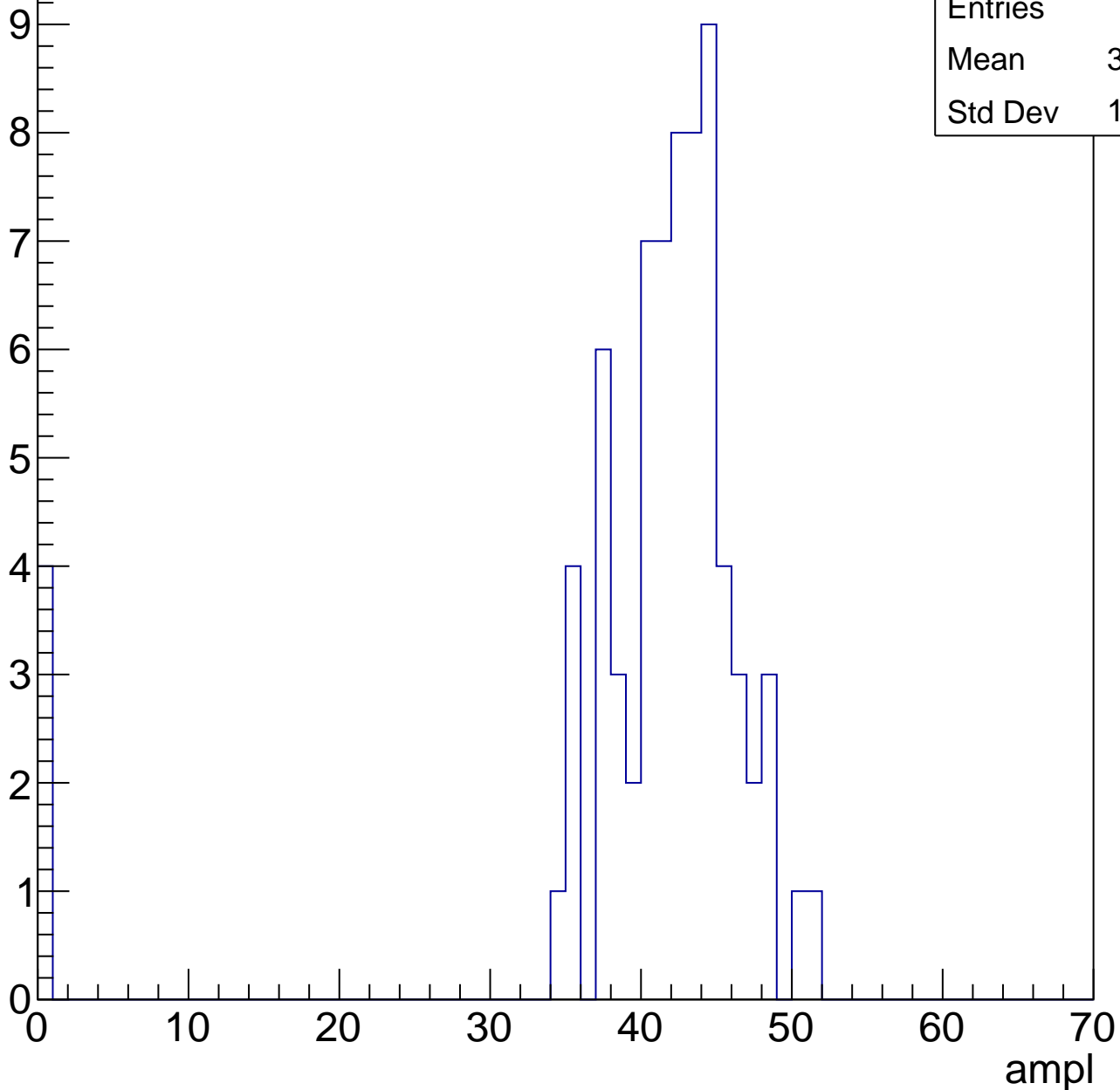


B1L103S, U9-ch93, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	39.56
Std Dev	10.18

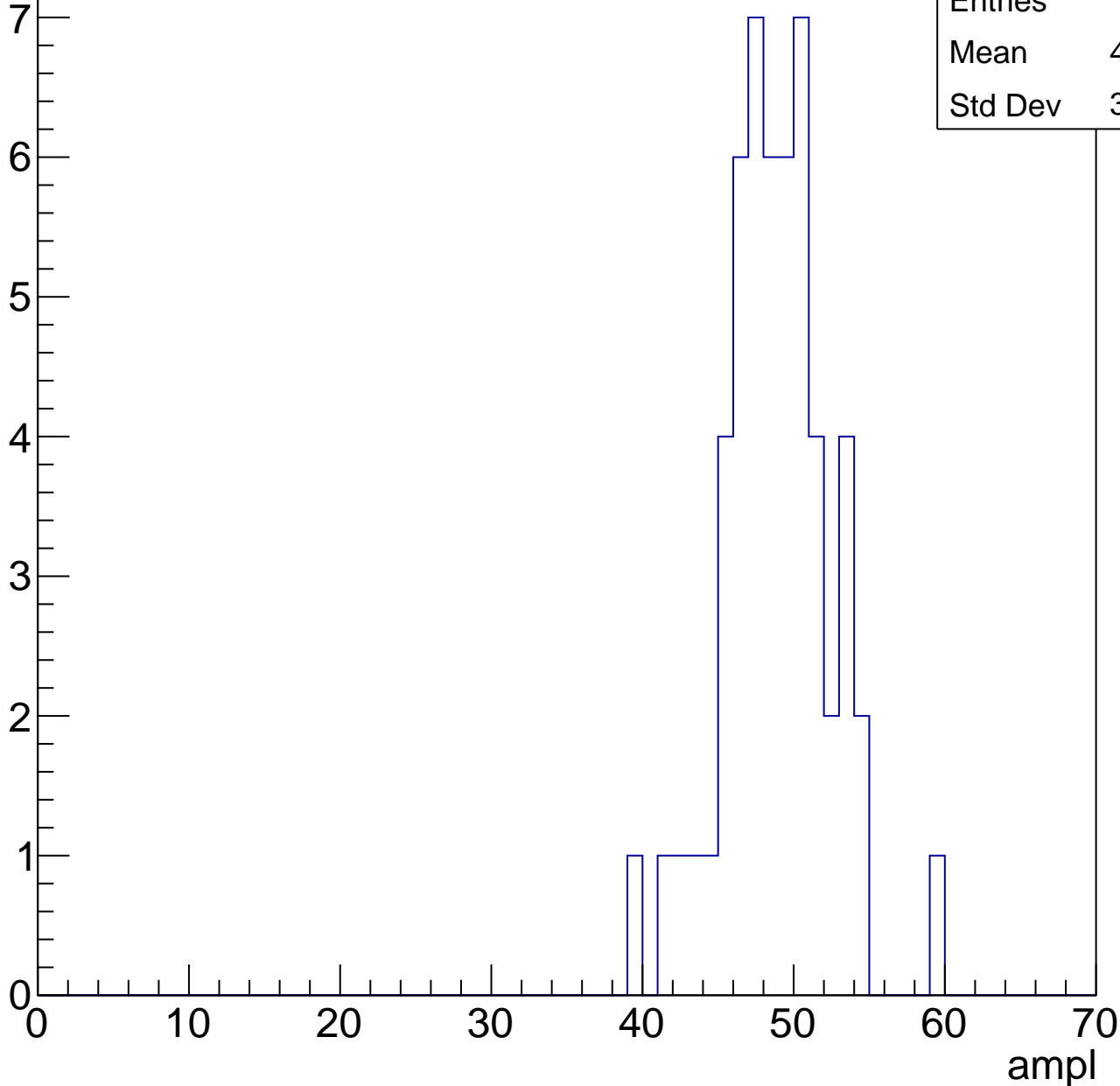


B1L103S, U9-ch93, adc3

calib_packv5_041523_1651.root, FC#0, port C2

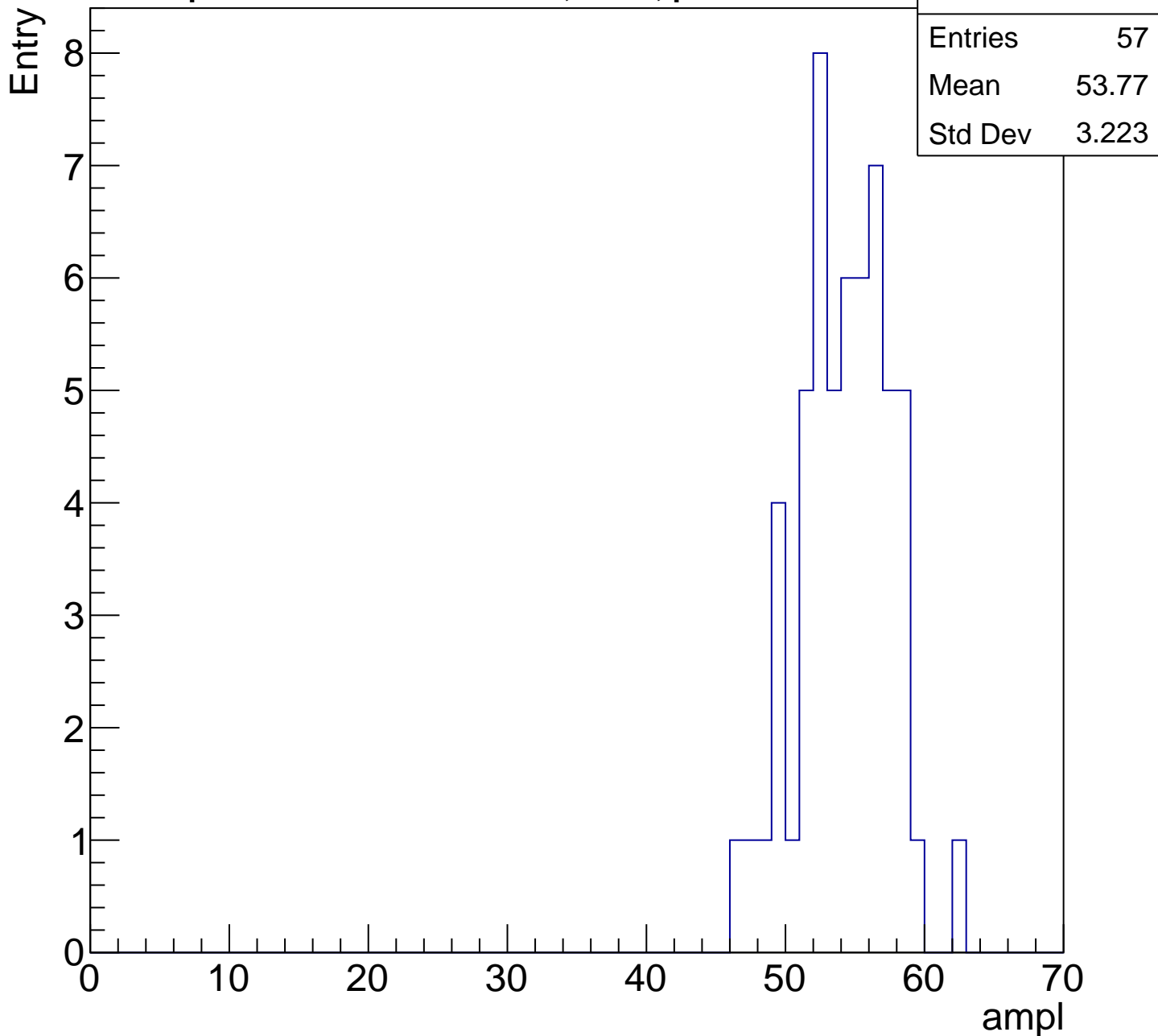
Entry

Entries	54
Mean	48.39
Std Dev	3.498



B1L103S, U9-ch93, adc4

calib_packv5_041523_1651.root, FC#0, port C2

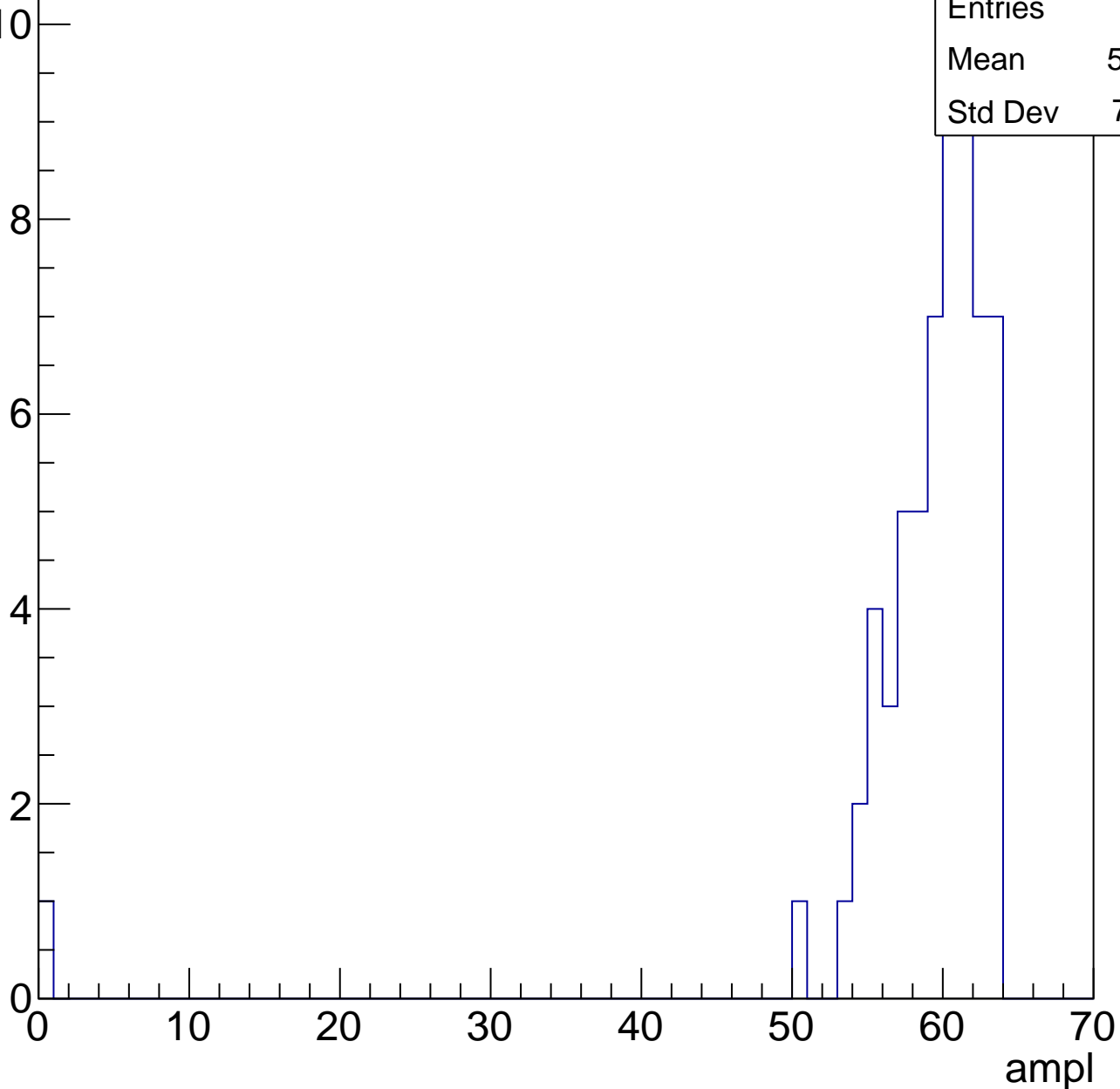


B1L103S, U9-ch93, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

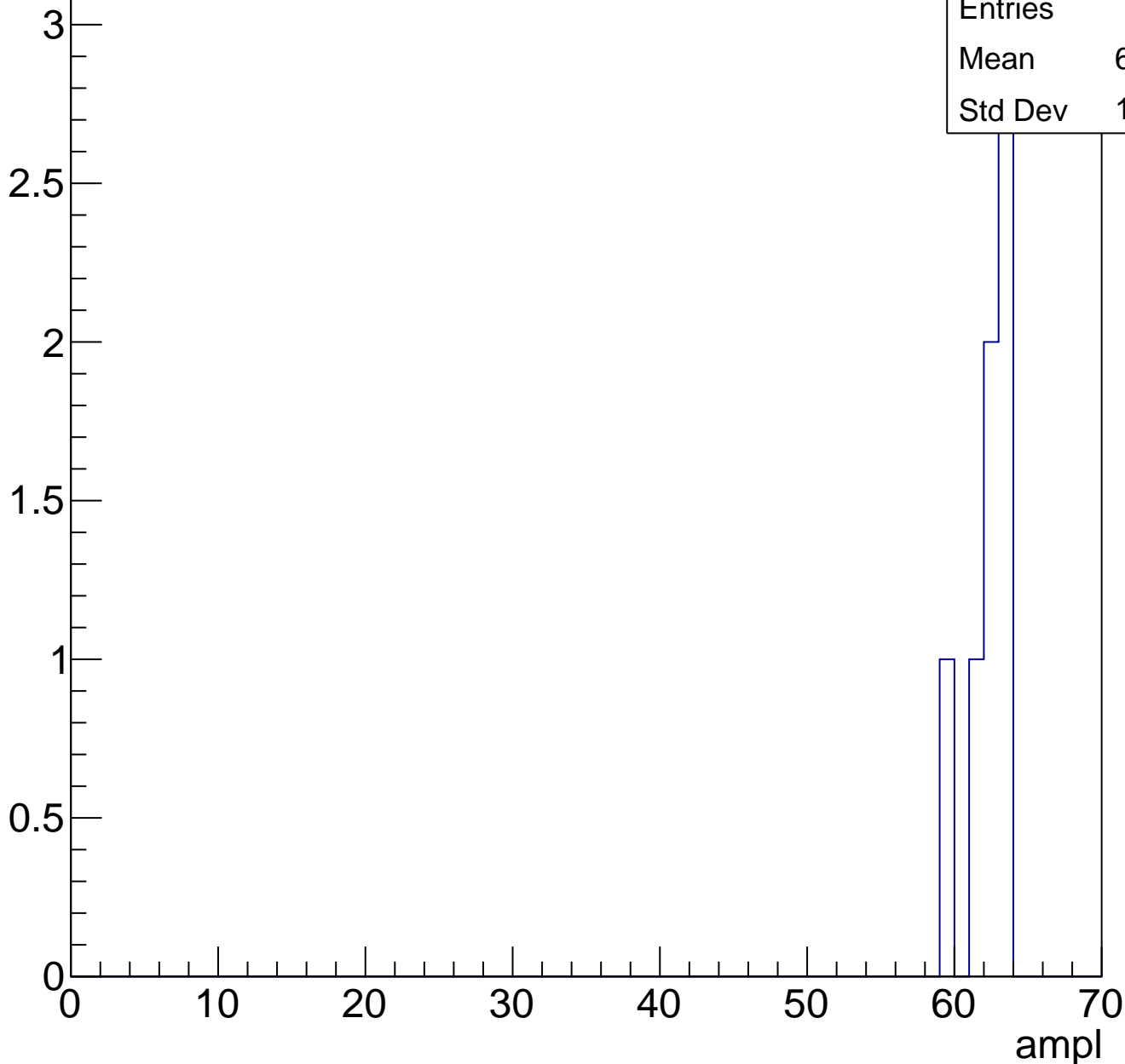
Entries	62
Mean	58.24
Std Dev	7.981



B1L103S, U9-ch93, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	7
Mean	61.86
Std Dev	1.355

B1L103S, U9-ch93, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

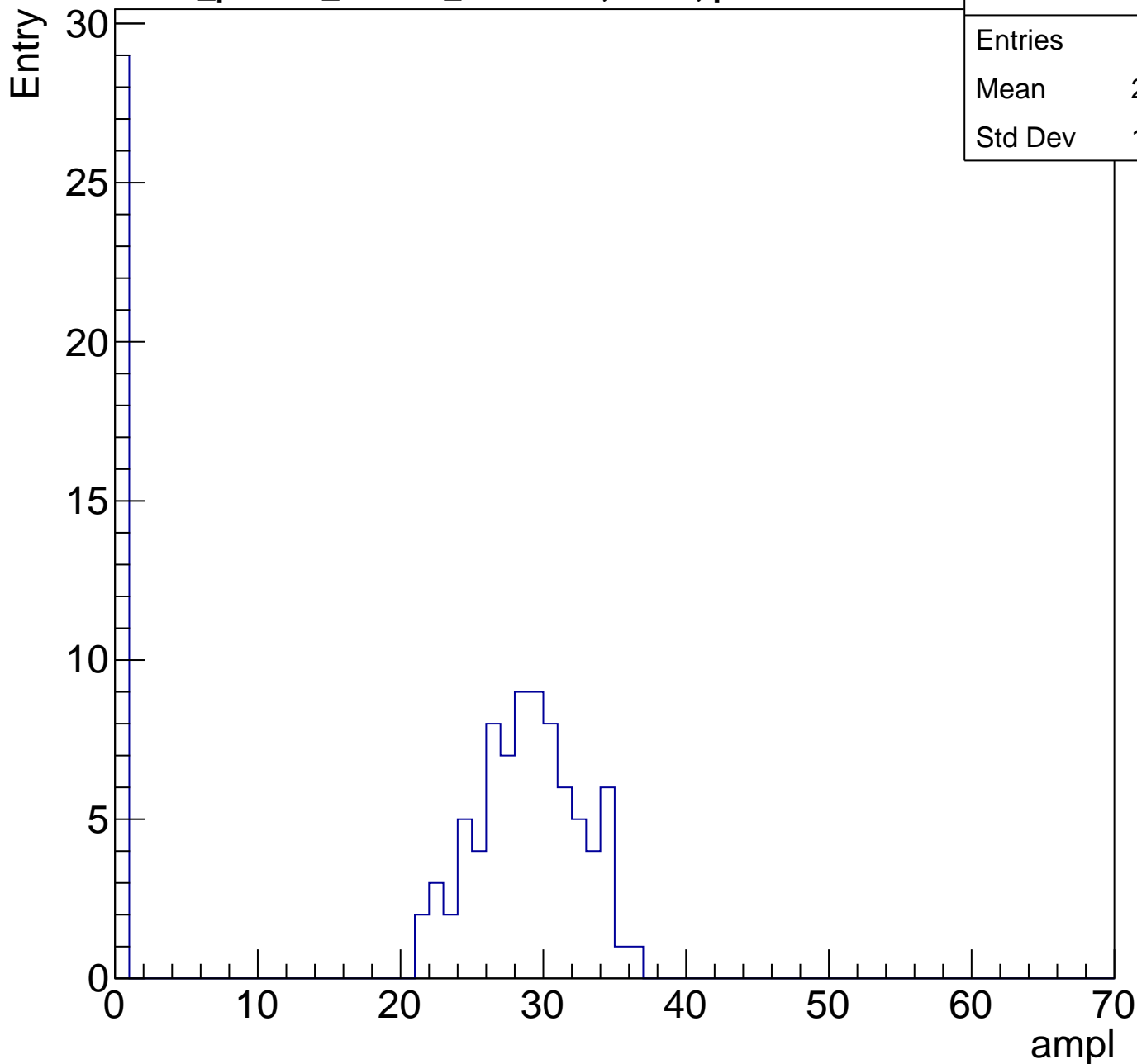
Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U9-ch94, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	109
Mean	20.89
Std Dev	12.94

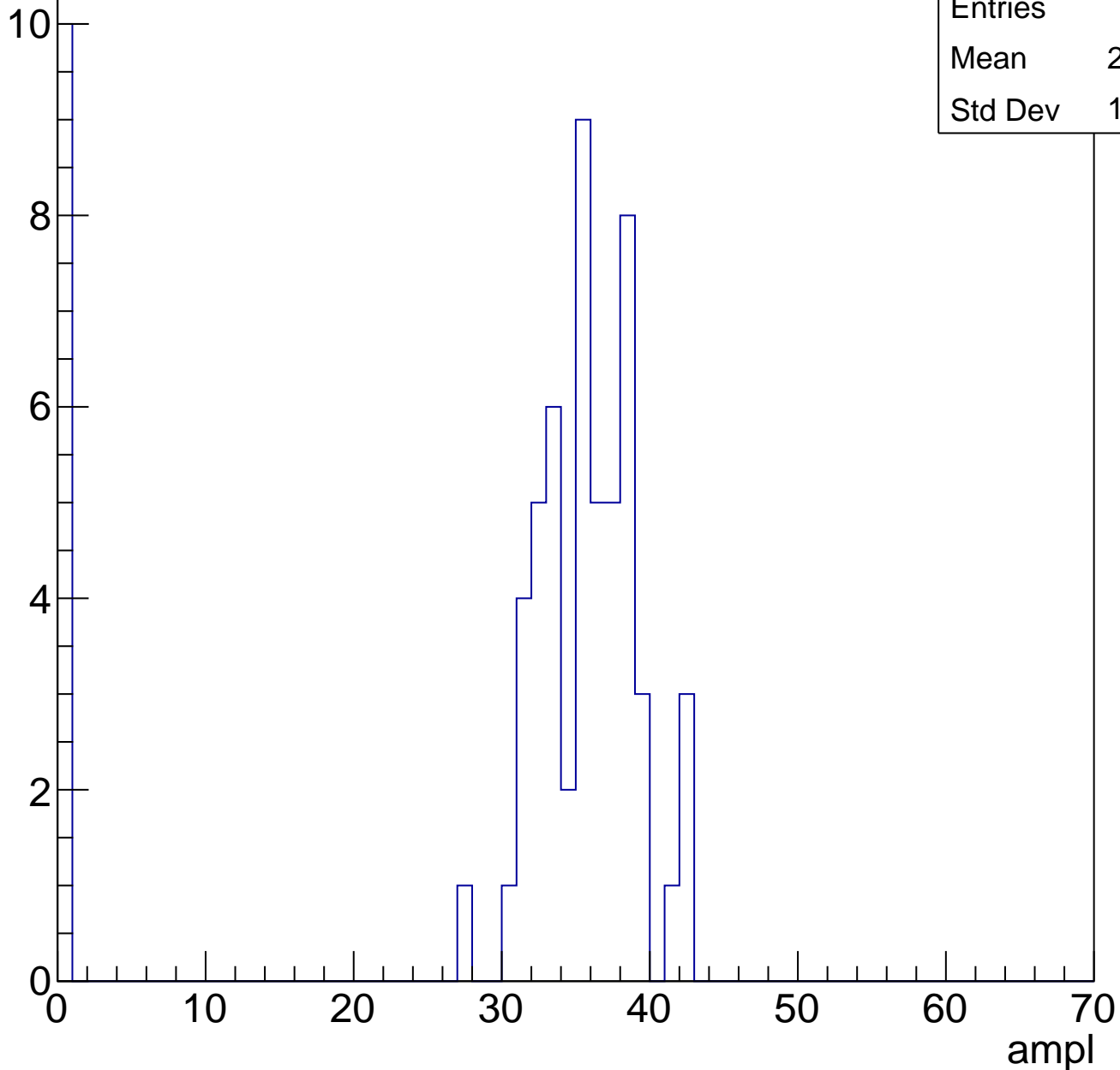


B1L103S, U9-ch94, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	63
Mean	29.76
Std Dev	13.26

Entry

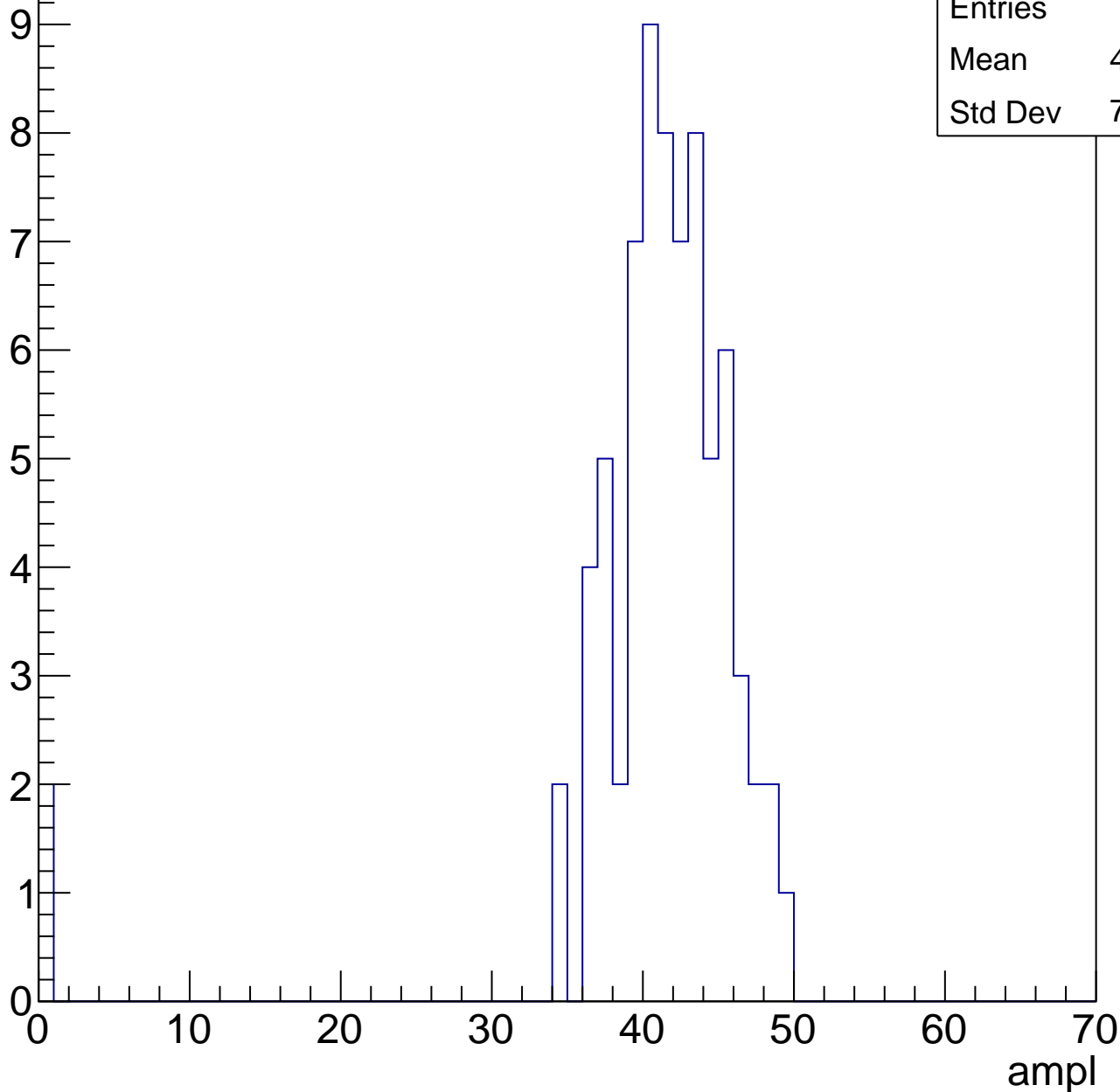


B1L103S, U9-ch94, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	40.26
Std Dev	7.534

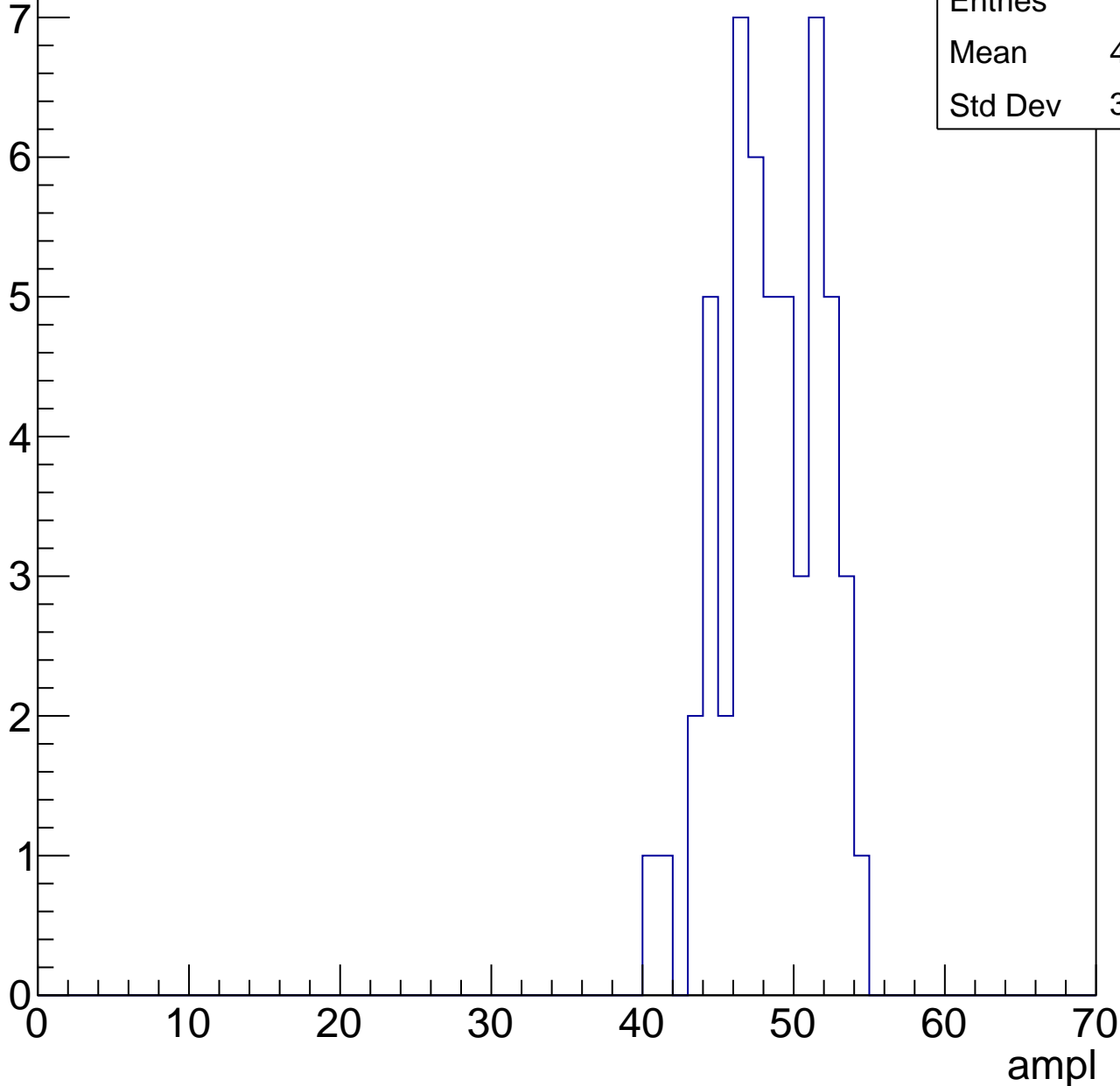


B1L103S, U9-ch94, adc3

calib_packv5_041523_1651.root, FC#0, port C2

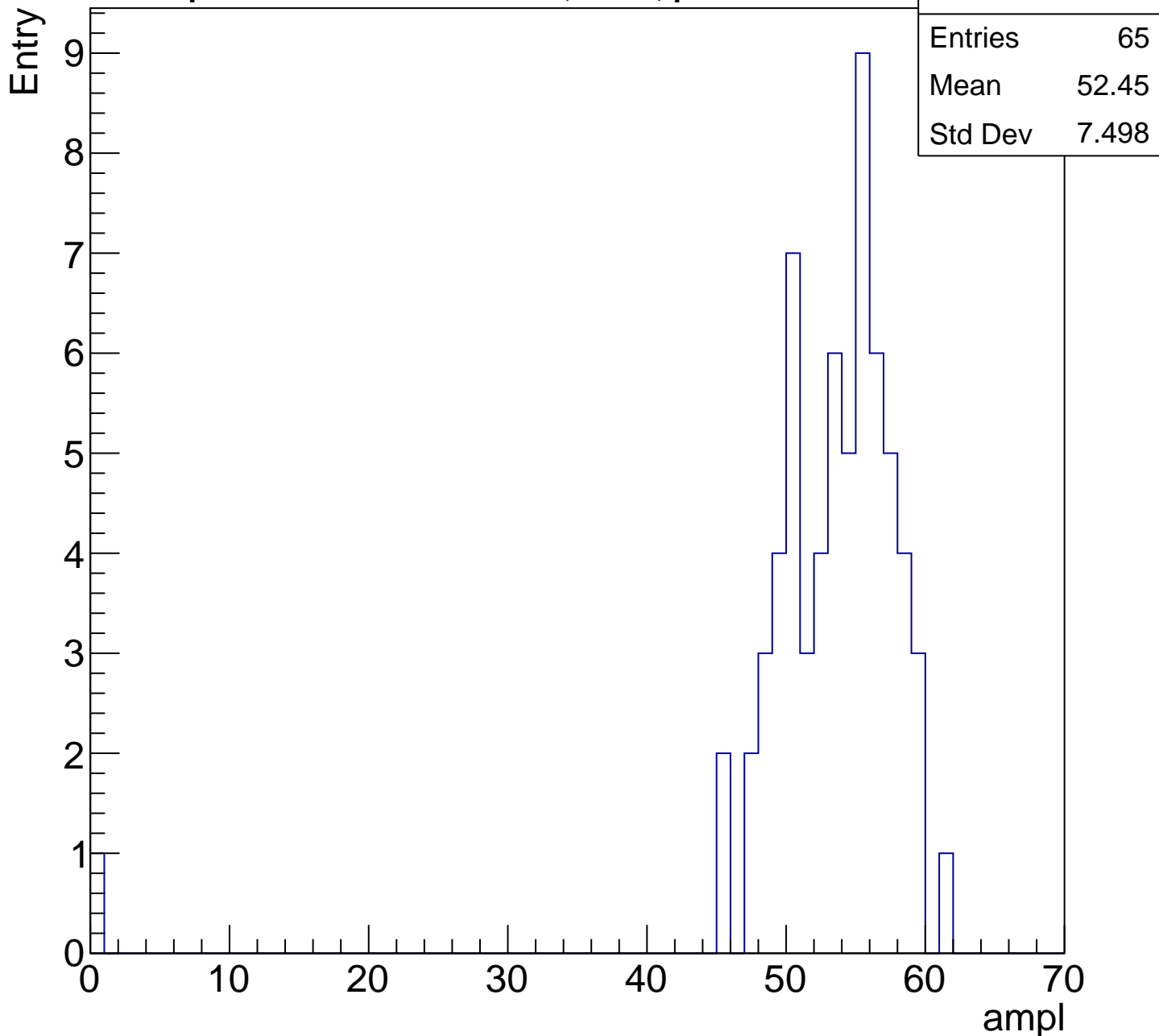
Entry

Entries	53
Mean	48.04
Std Dev	3.268



B1L103S, U9-ch94, adc4

calib_packv5_041523_1651.root, FC#0, port C2

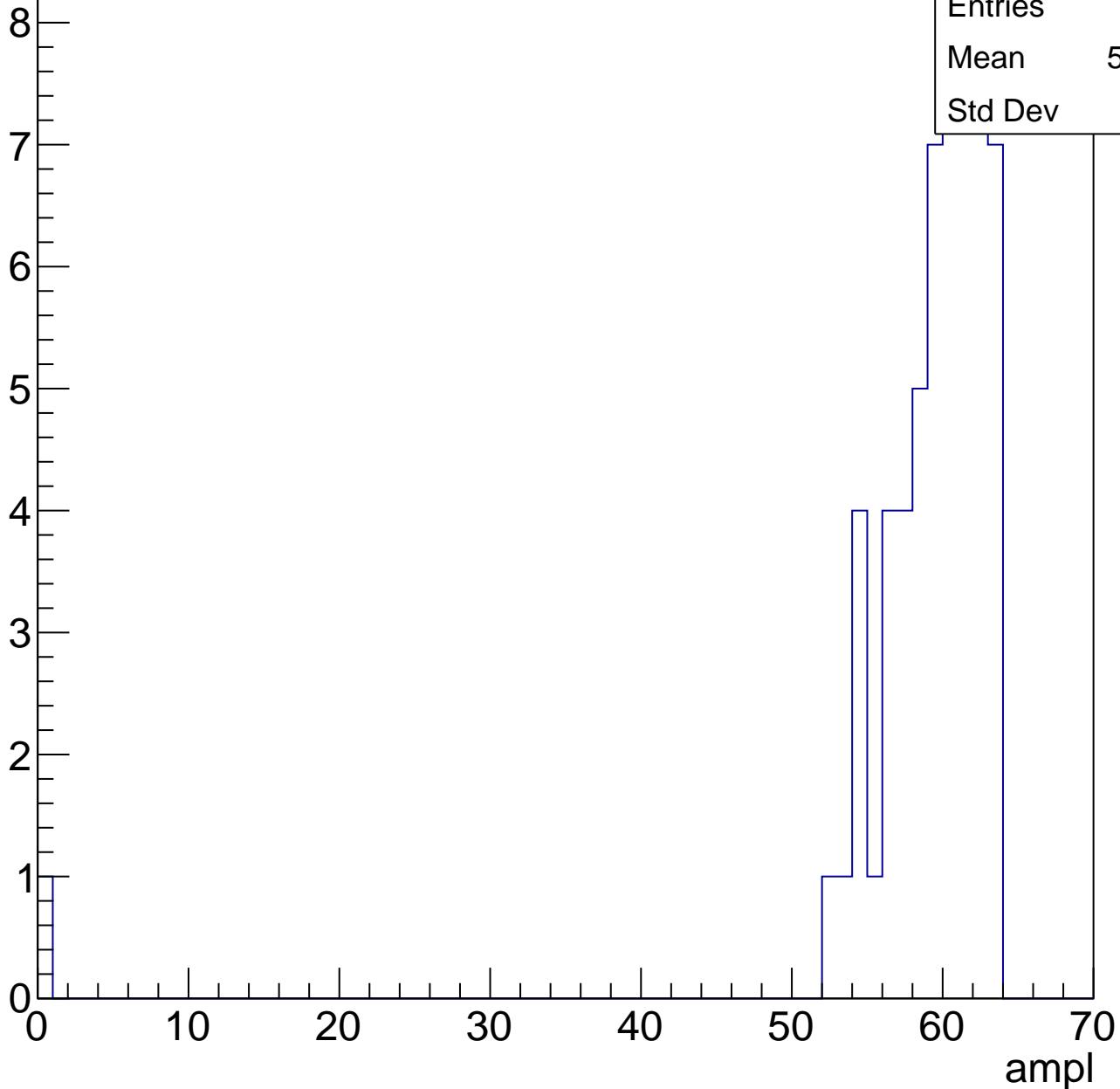


B1L103S, U9-ch94, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

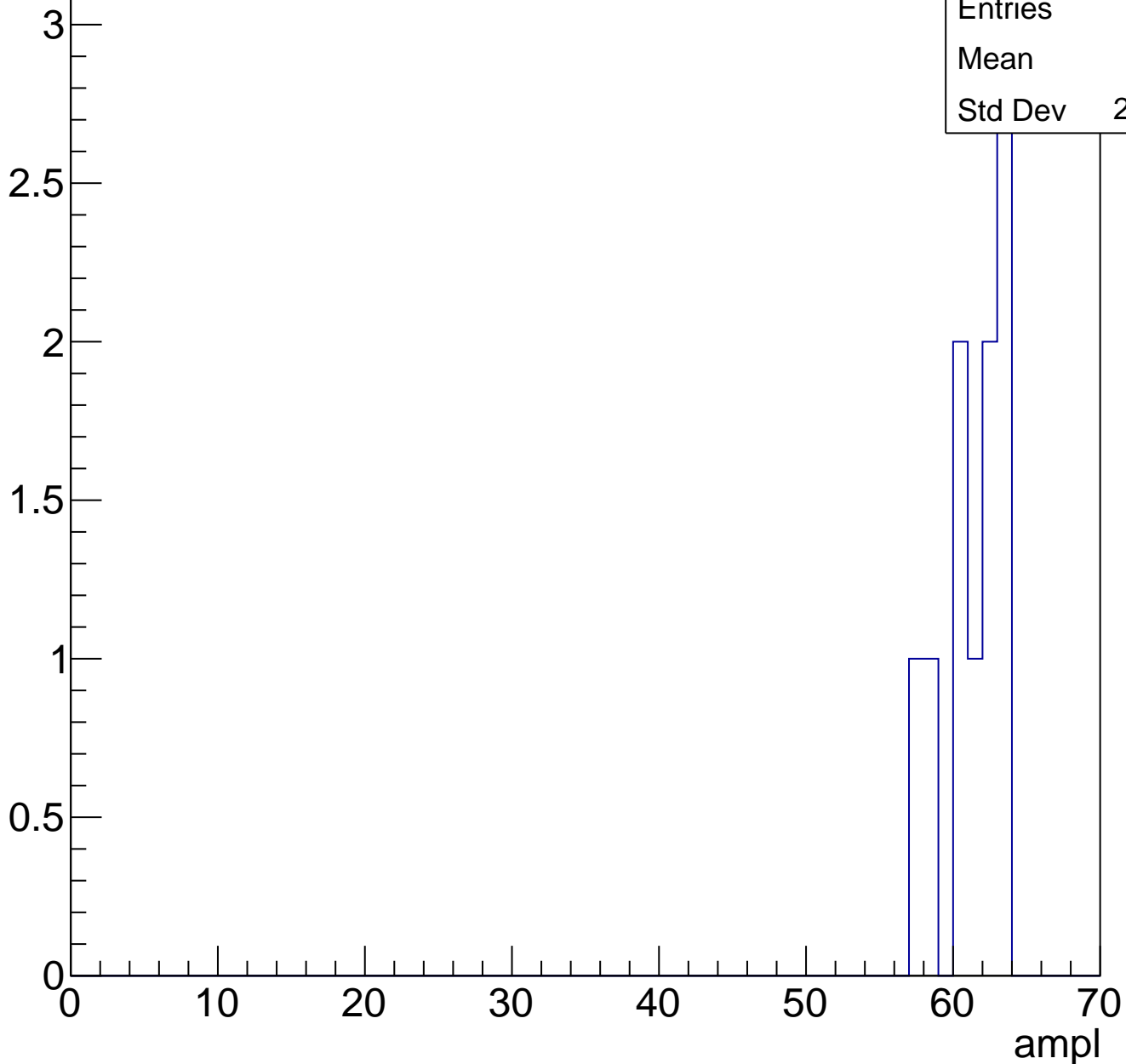
Entries	59
Mean	58.24
Std Dev	8.16



B1L103S, U9-ch94, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch94, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

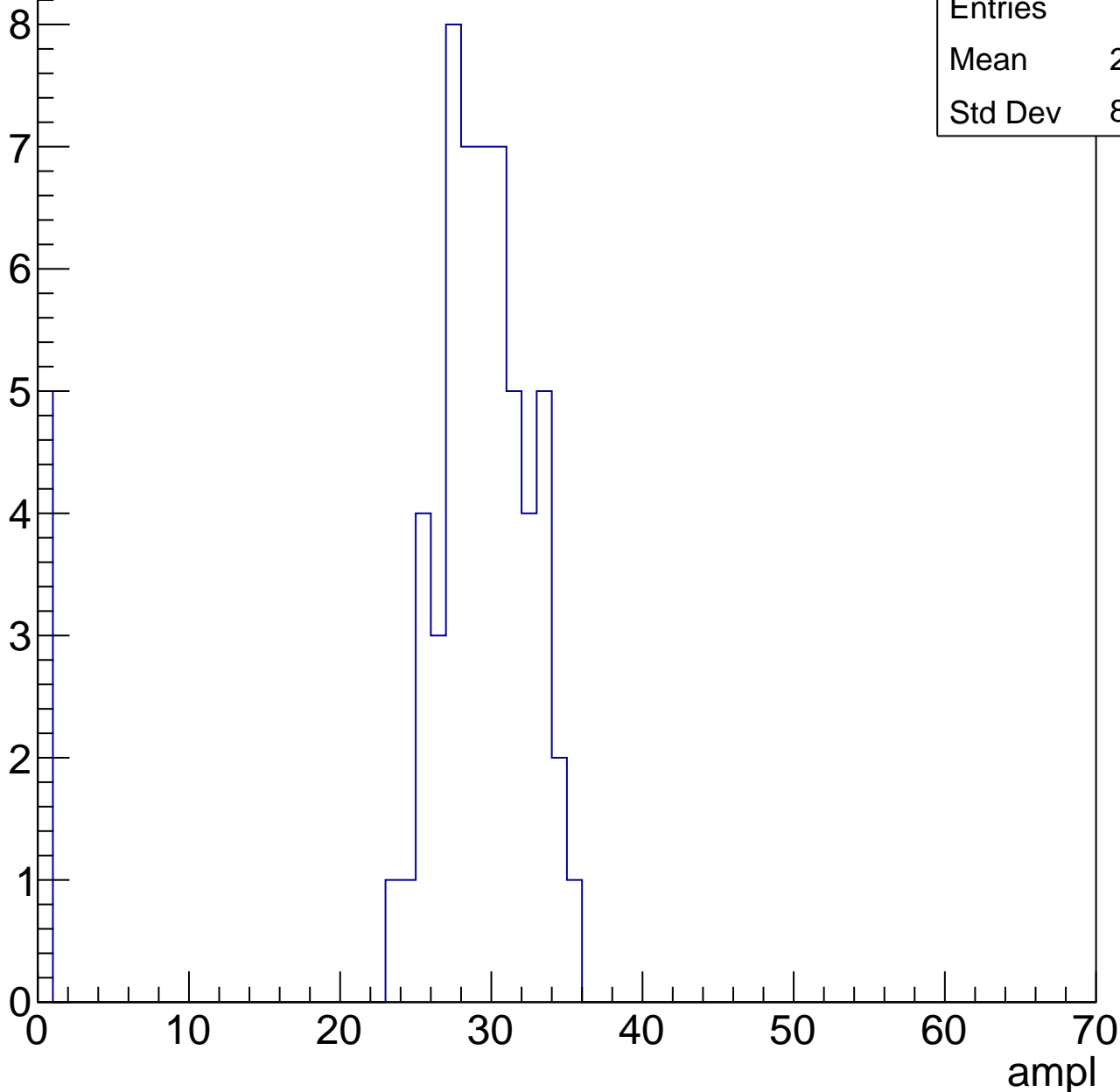
ampl

B1L103S, U9-ch95, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	26.68
Std Dev	8.469

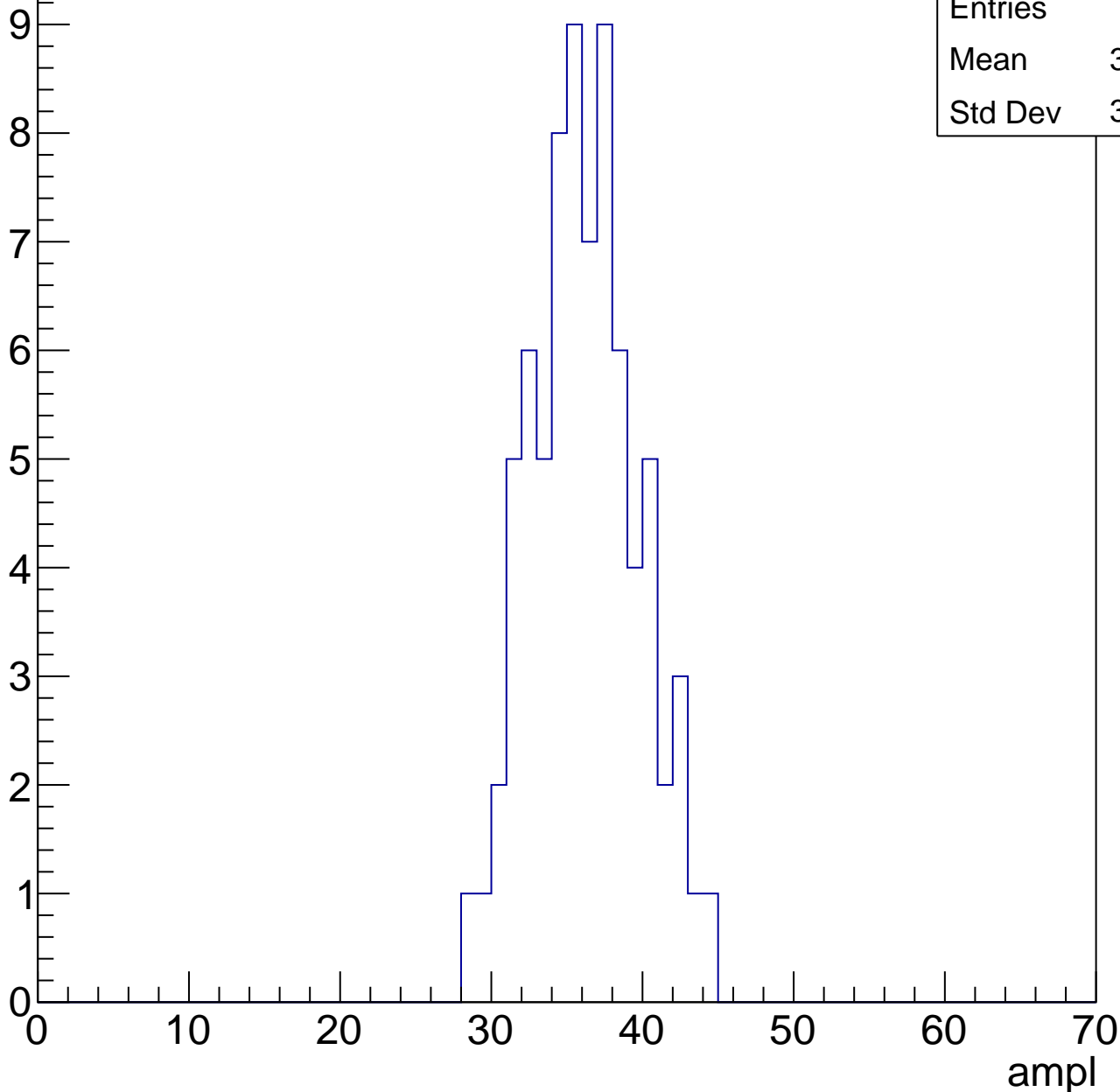


B1L103S, U9-ch95, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	35.73
Std Dev	3.477

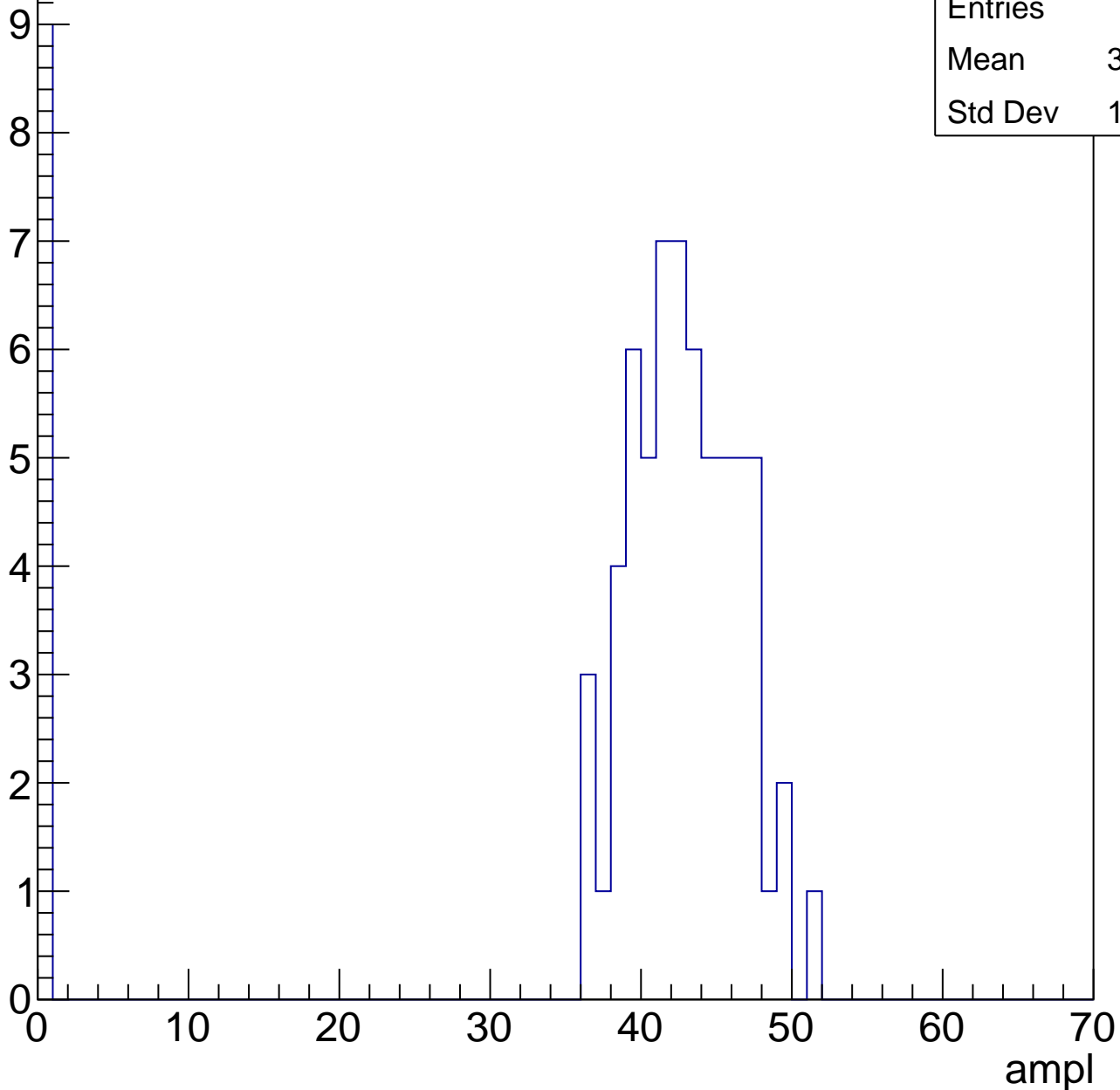


B1L103S, U9-ch95, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	37.18
Std Dev	14.42

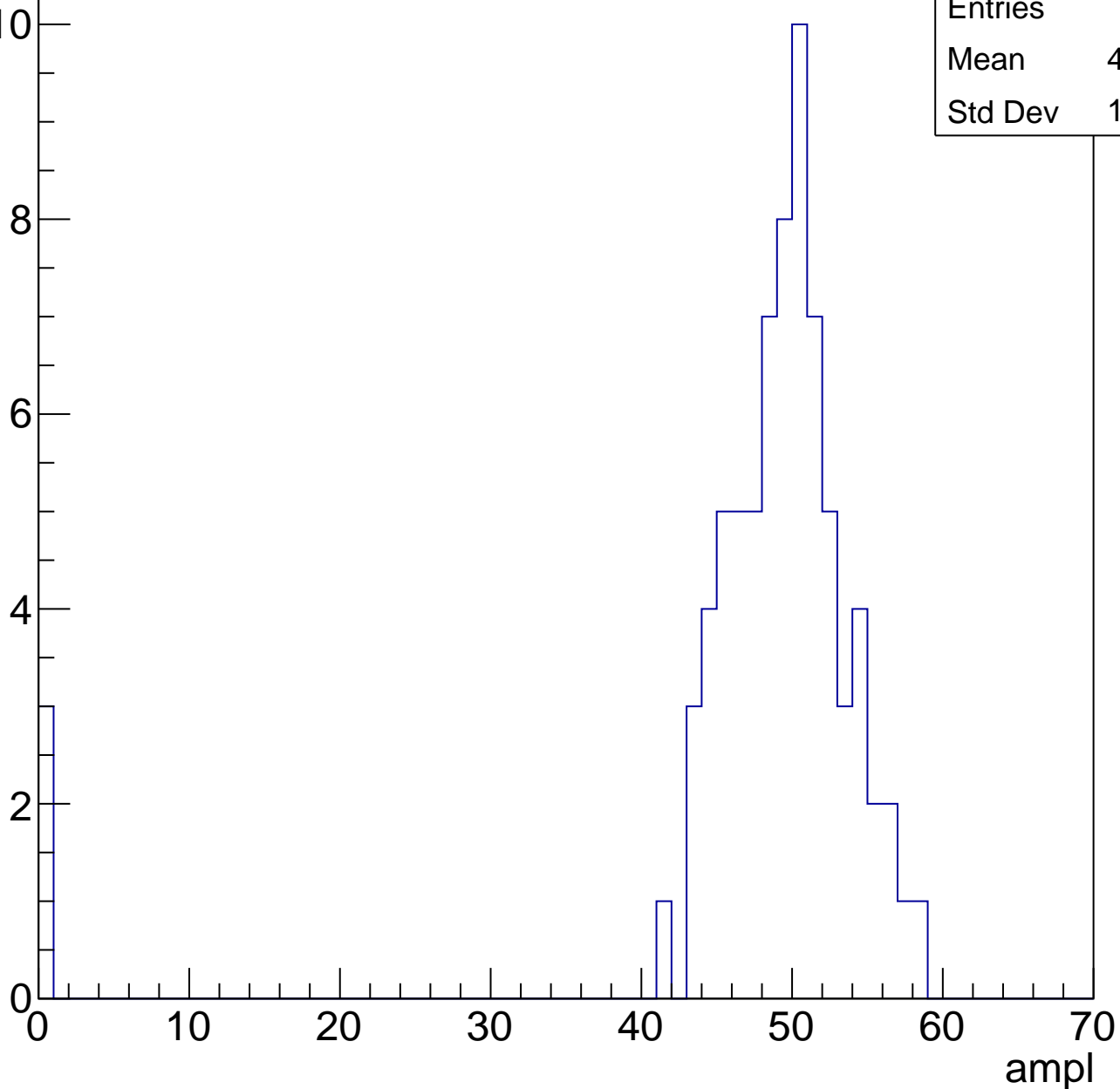


B1L103S, U9-ch95, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	47.28
Std Dev	10.23

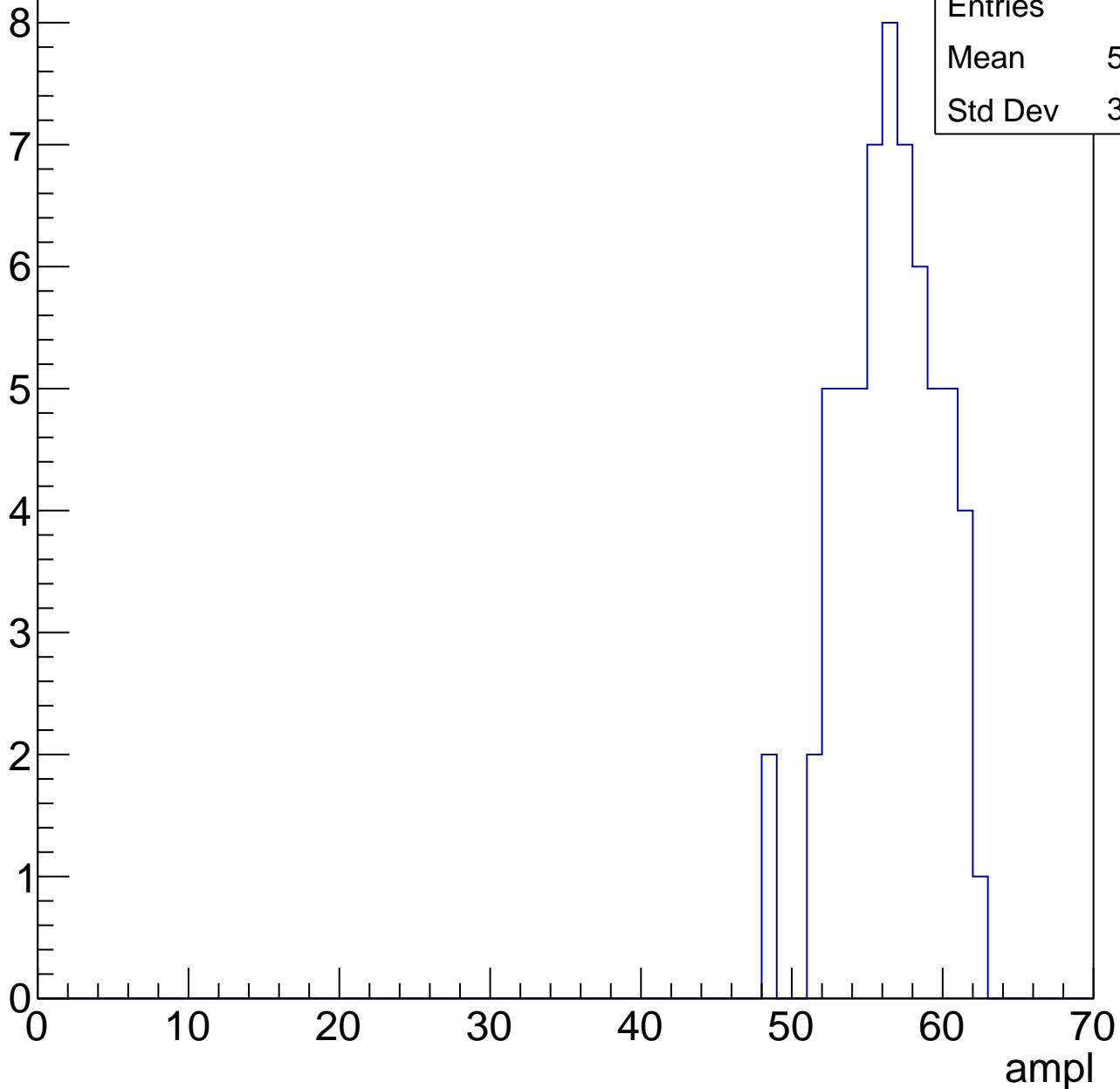


B1L103S, U9-ch95, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	56.03
Std Dev	3.167

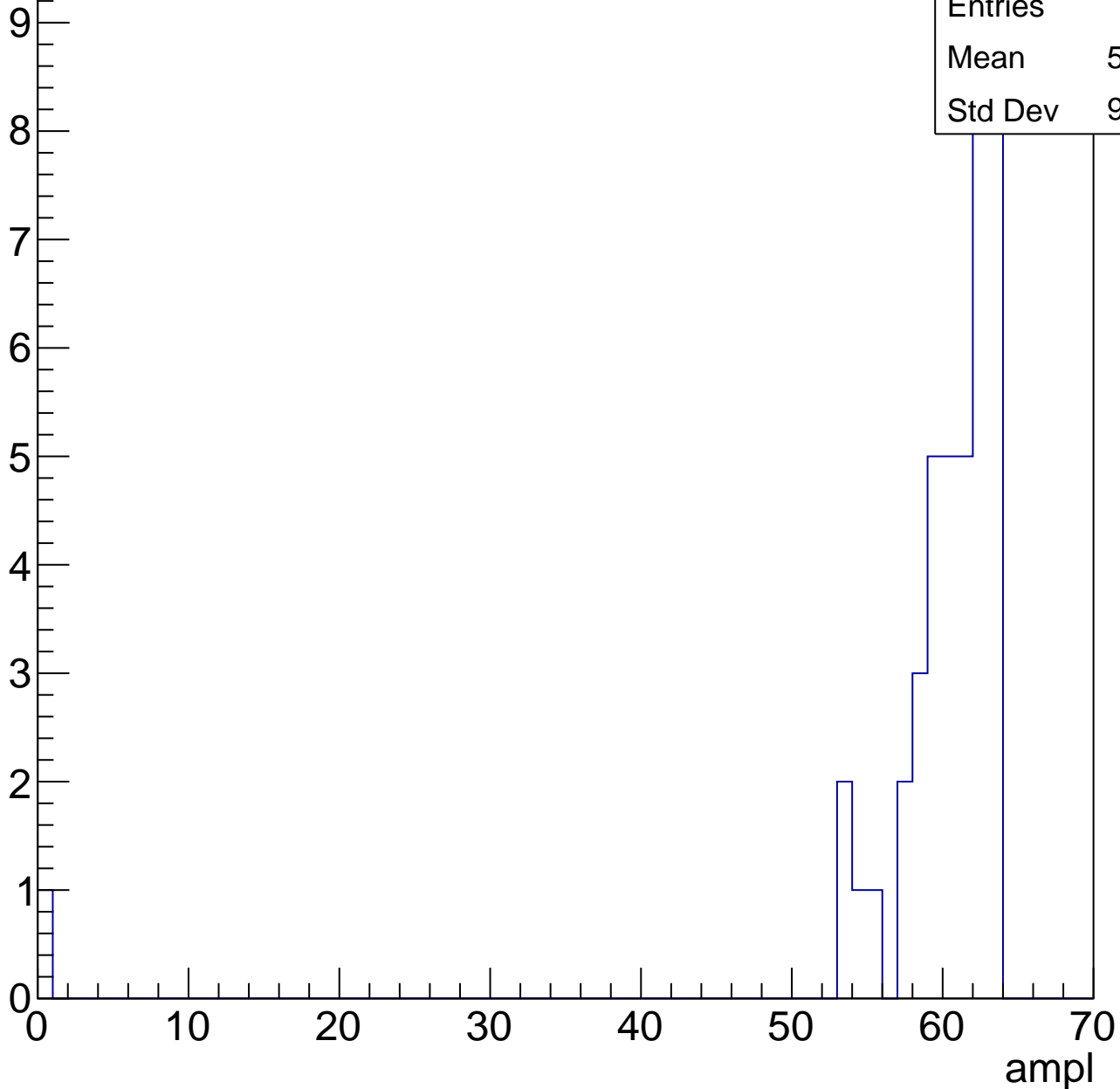


B1L103S, U9-ch95, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	42
Mean	58.69
Std Dev	9.556



B1L103S, U9-ch95, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch95, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.211
Std Dev	5.136

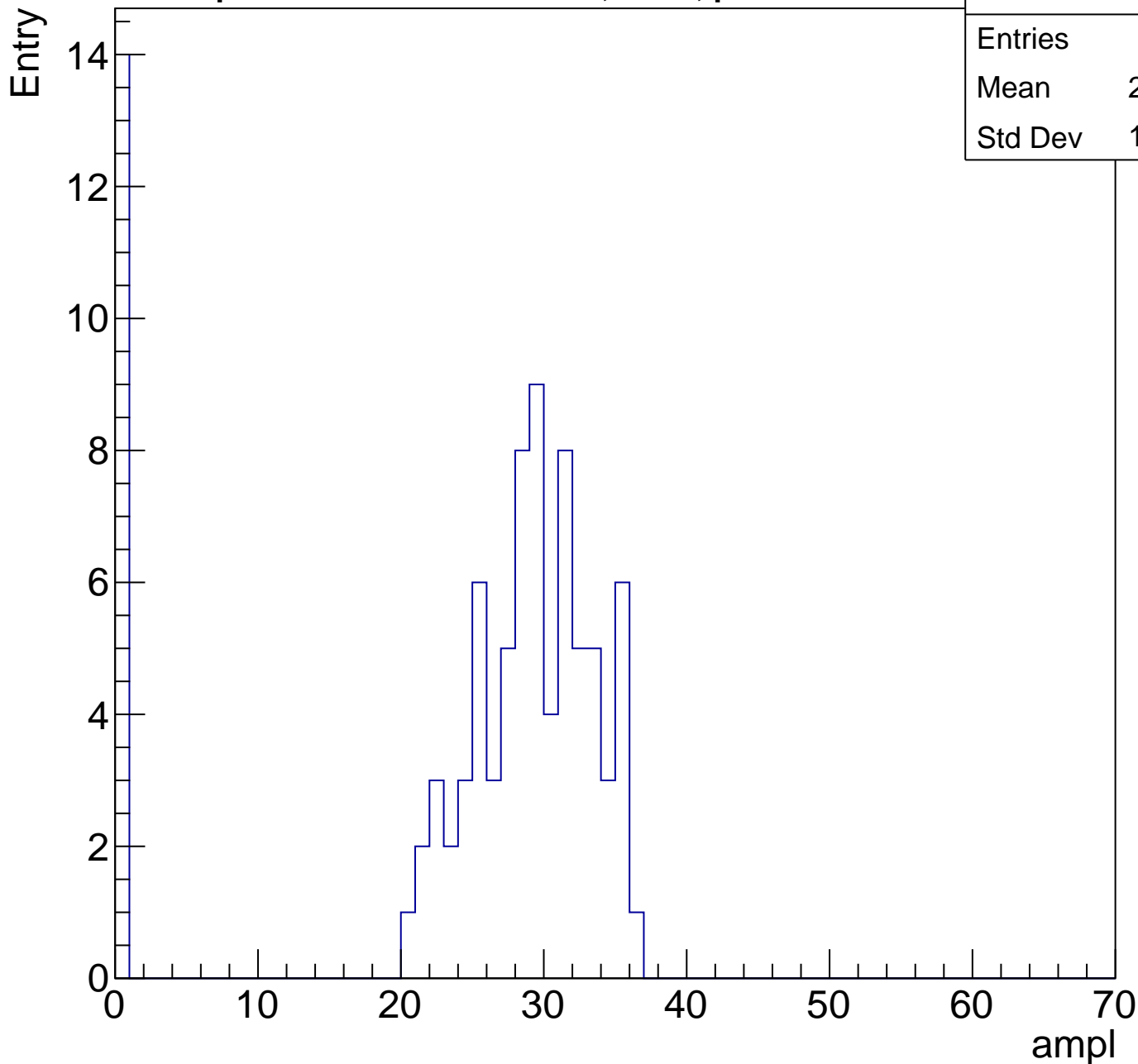
Entry



B1L103S, U9-ch96, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	88
Mean	24.26
Std Dev	11.16

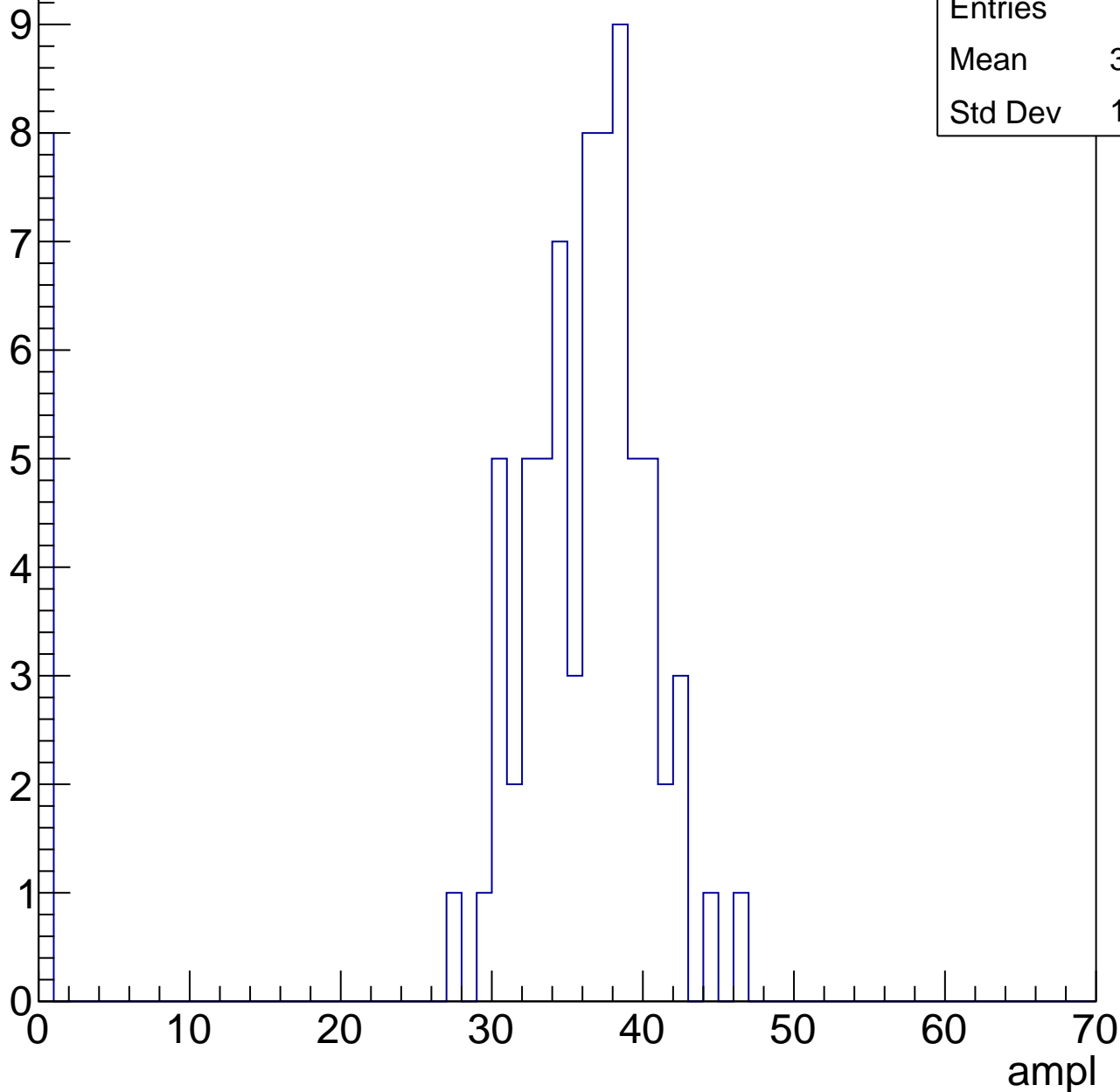


B1L103S, U9-ch96, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	79
Mean	32.34
Std Dev	11.43

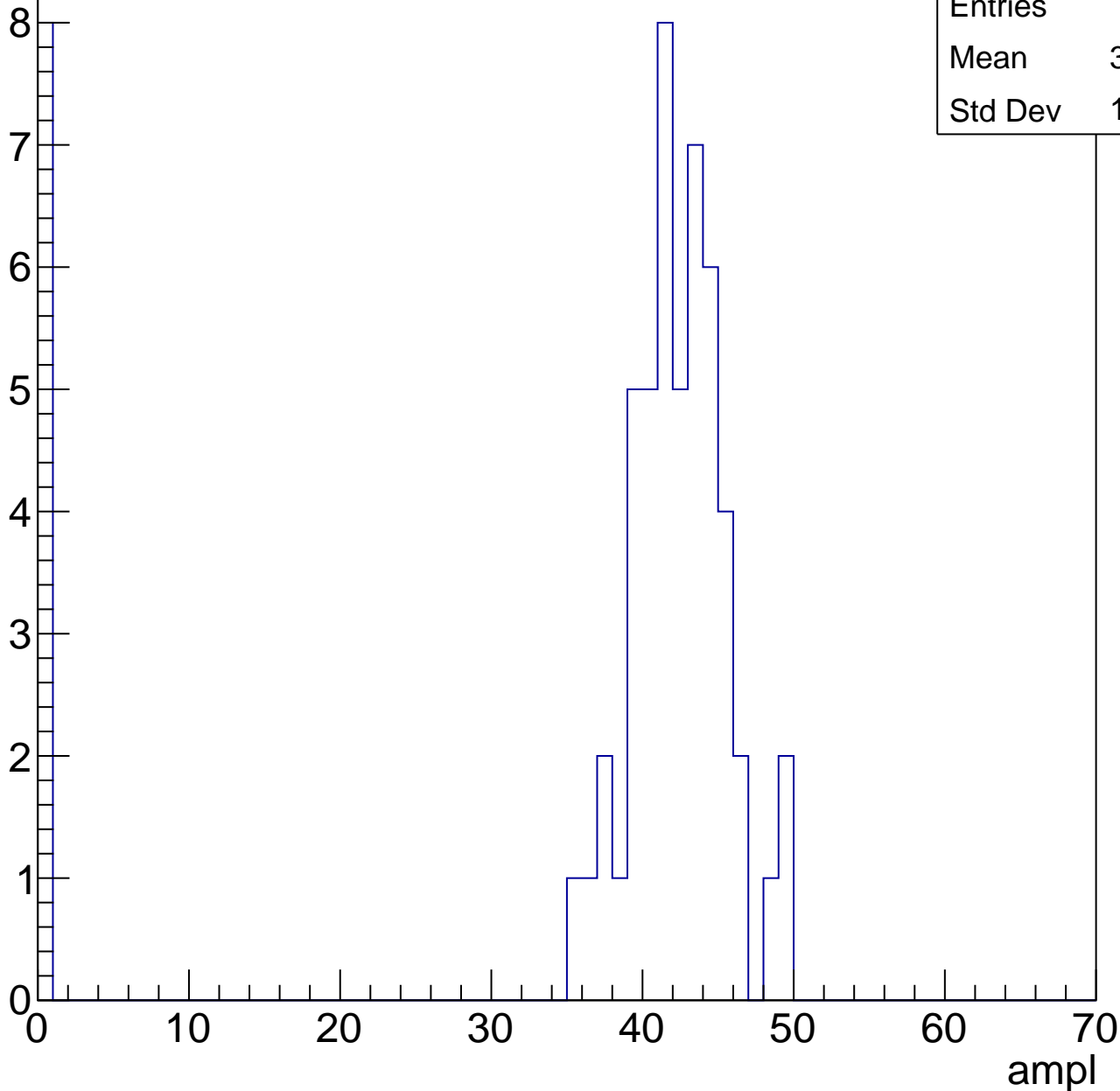


B1L103S, U9-ch96, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	36.19
Std Dev	14.75

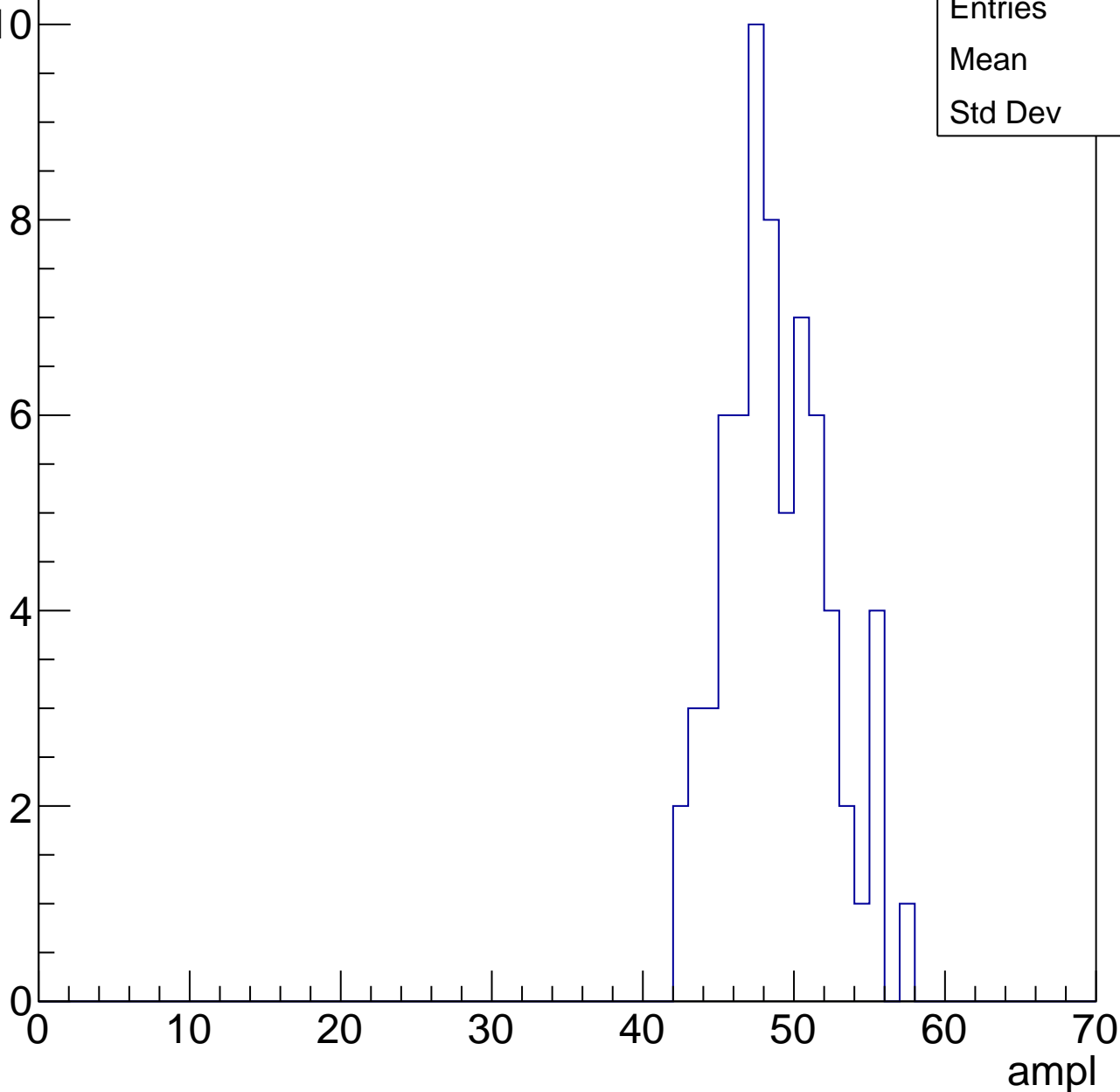


B1L103S, U9-ch96, adc3

calib_packv5_041523_1651.root, FC#0, port C2

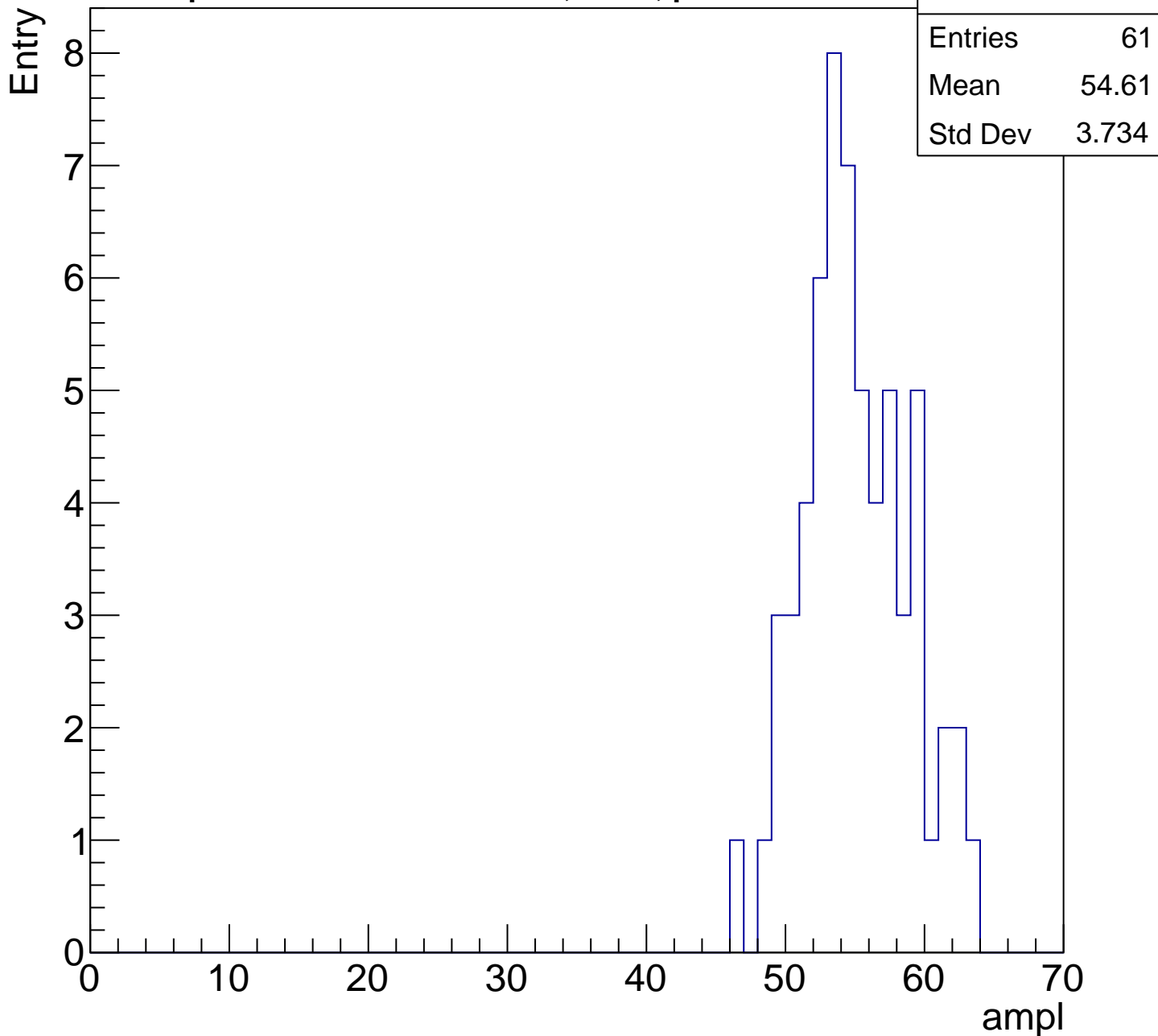
Entry

Entries	68
Mean	48.4
Std Dev	3.4



B1L103S, U9-ch96, adc4

calib_packv5_041523_1651.root, FC#0, port C2

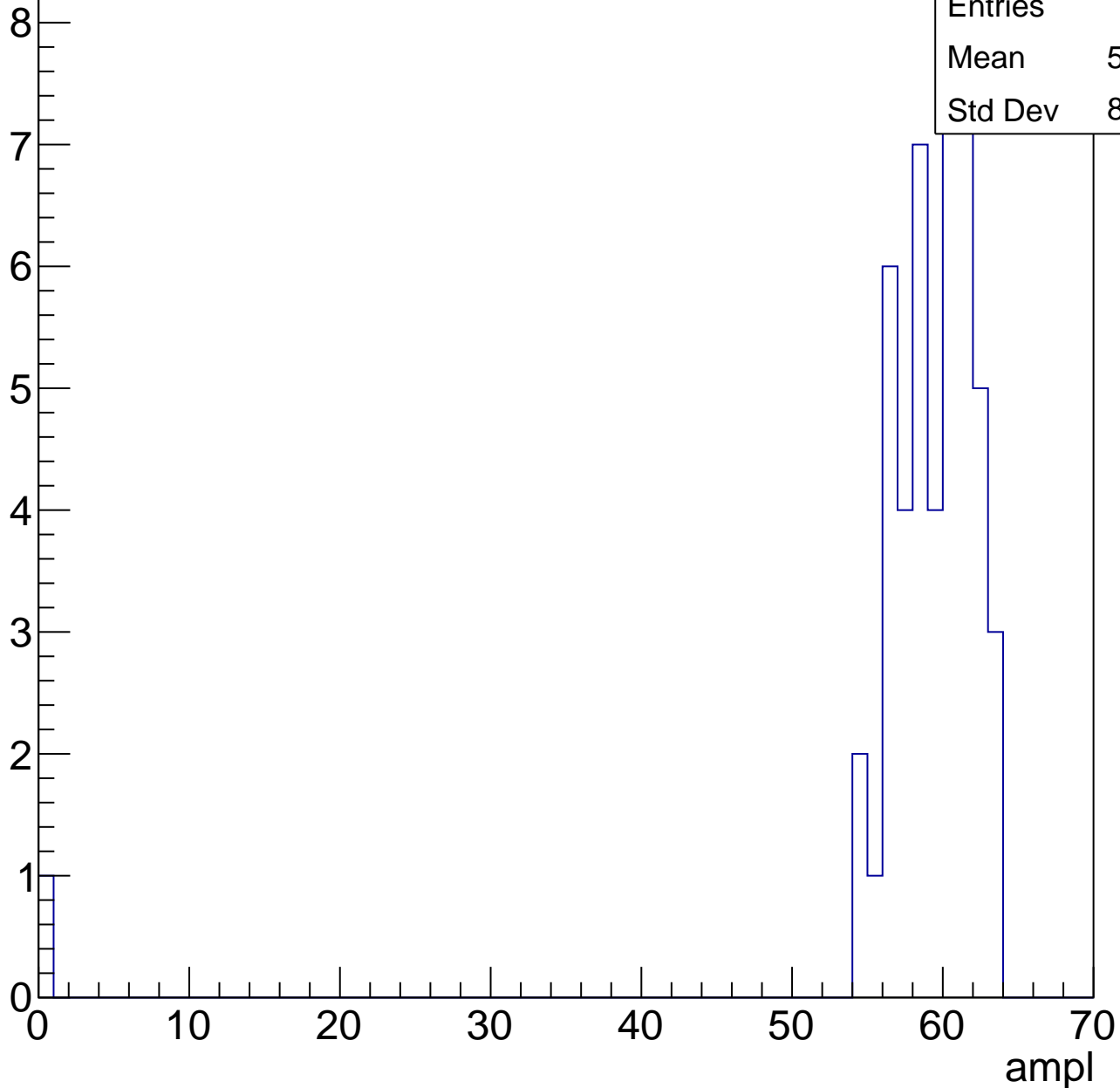


B1L103S, U9-ch96, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	57.88
Std Dev	8.684

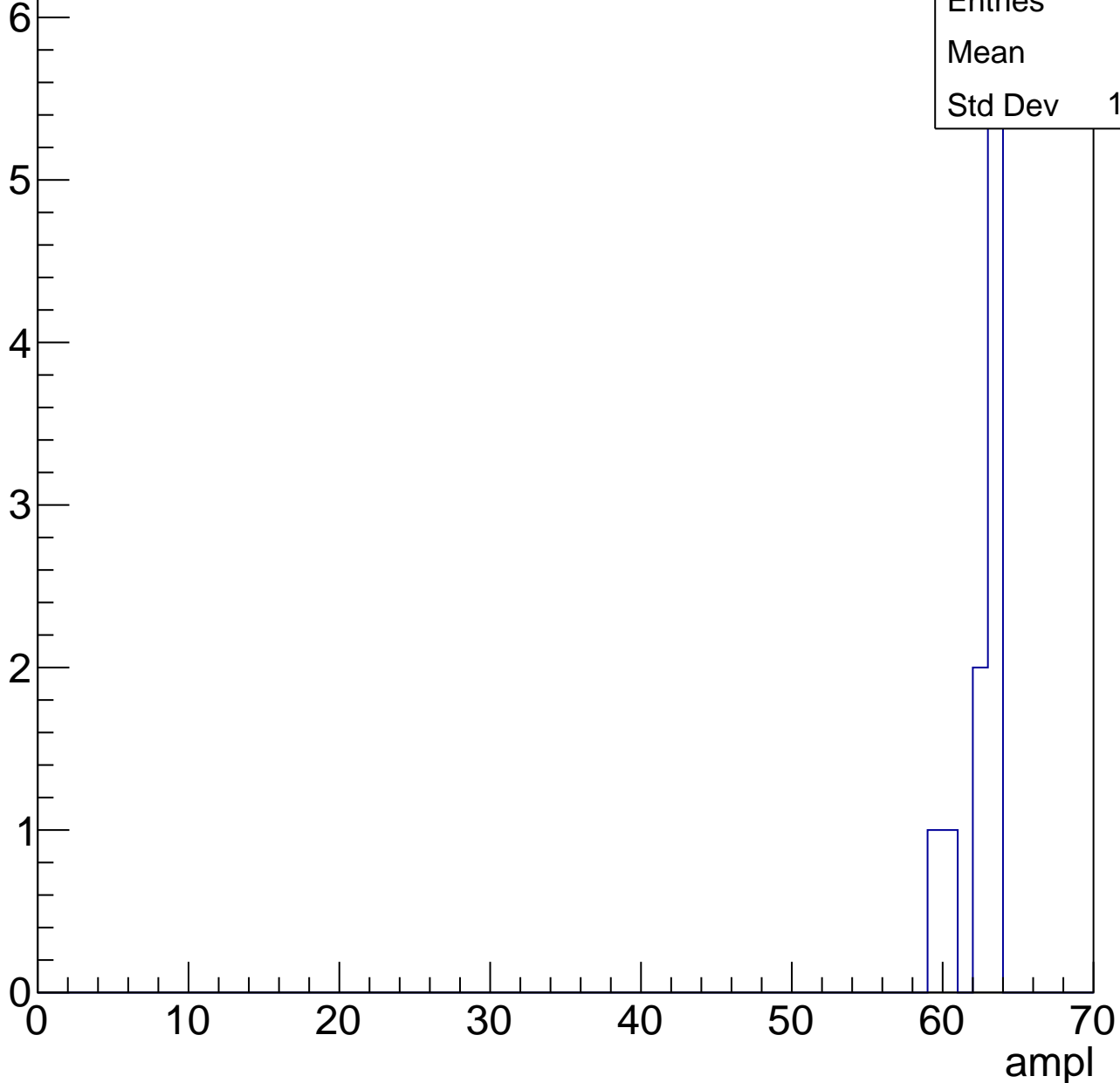


B1L103S, U9-ch96, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	10
Mean	62.1
Std Dev	1.375



B1L103S, U9-ch96, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51

Entry

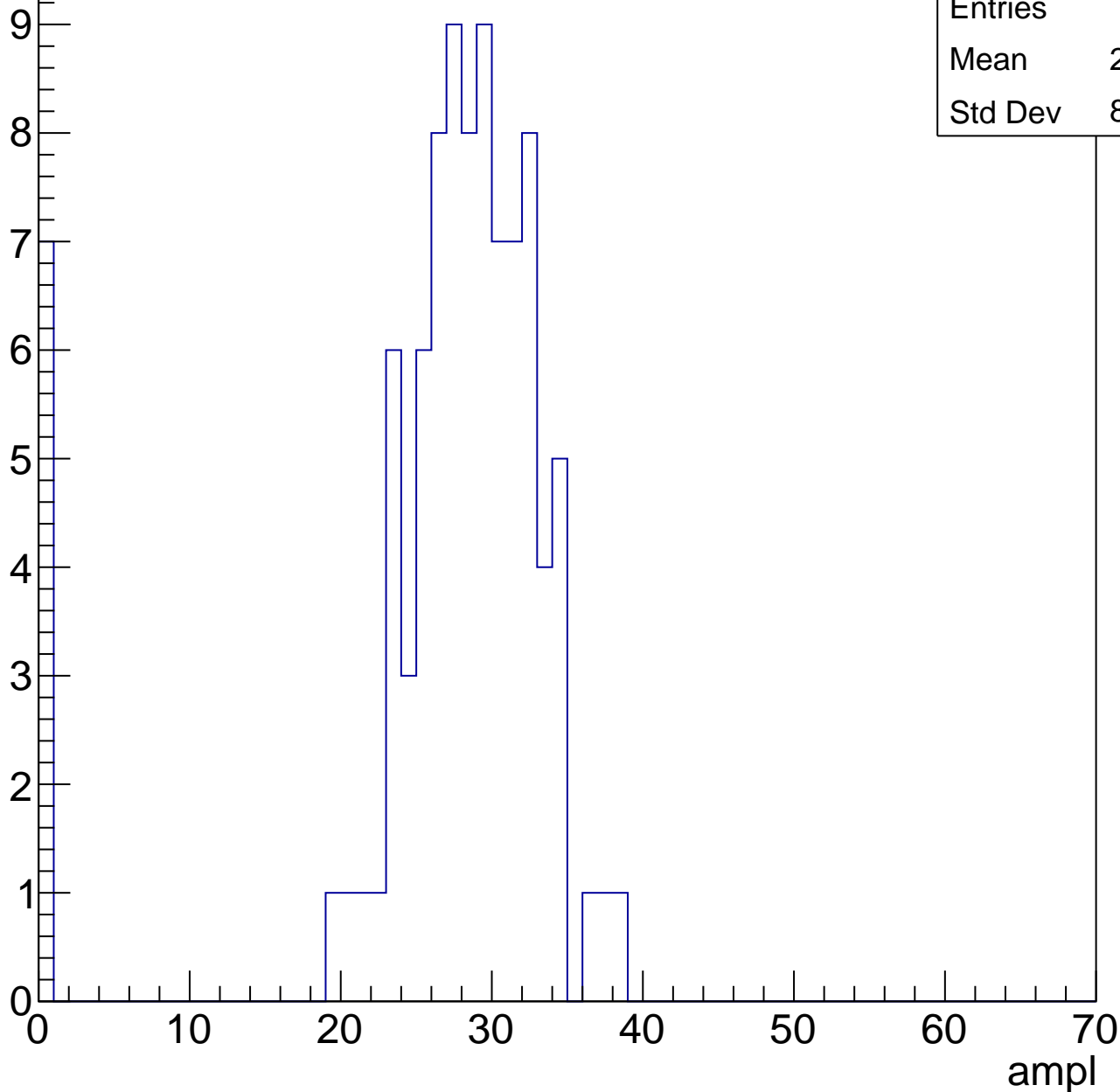


B1L103S, U9-ch97, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	94
Mean	26.32
Std Dev	8.315

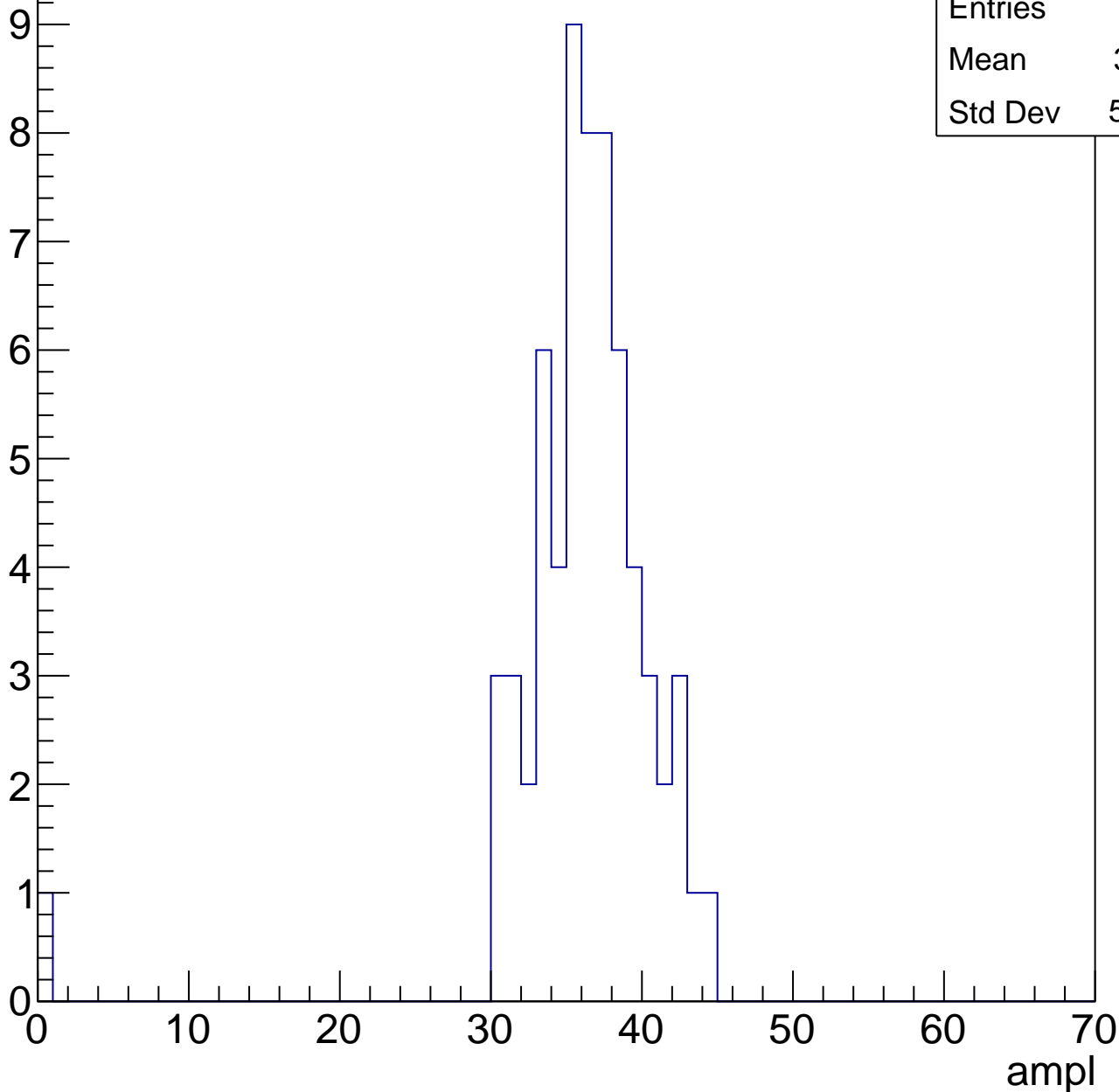


B1L103S, U9-ch97, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	35.61
Std Dev	5.544

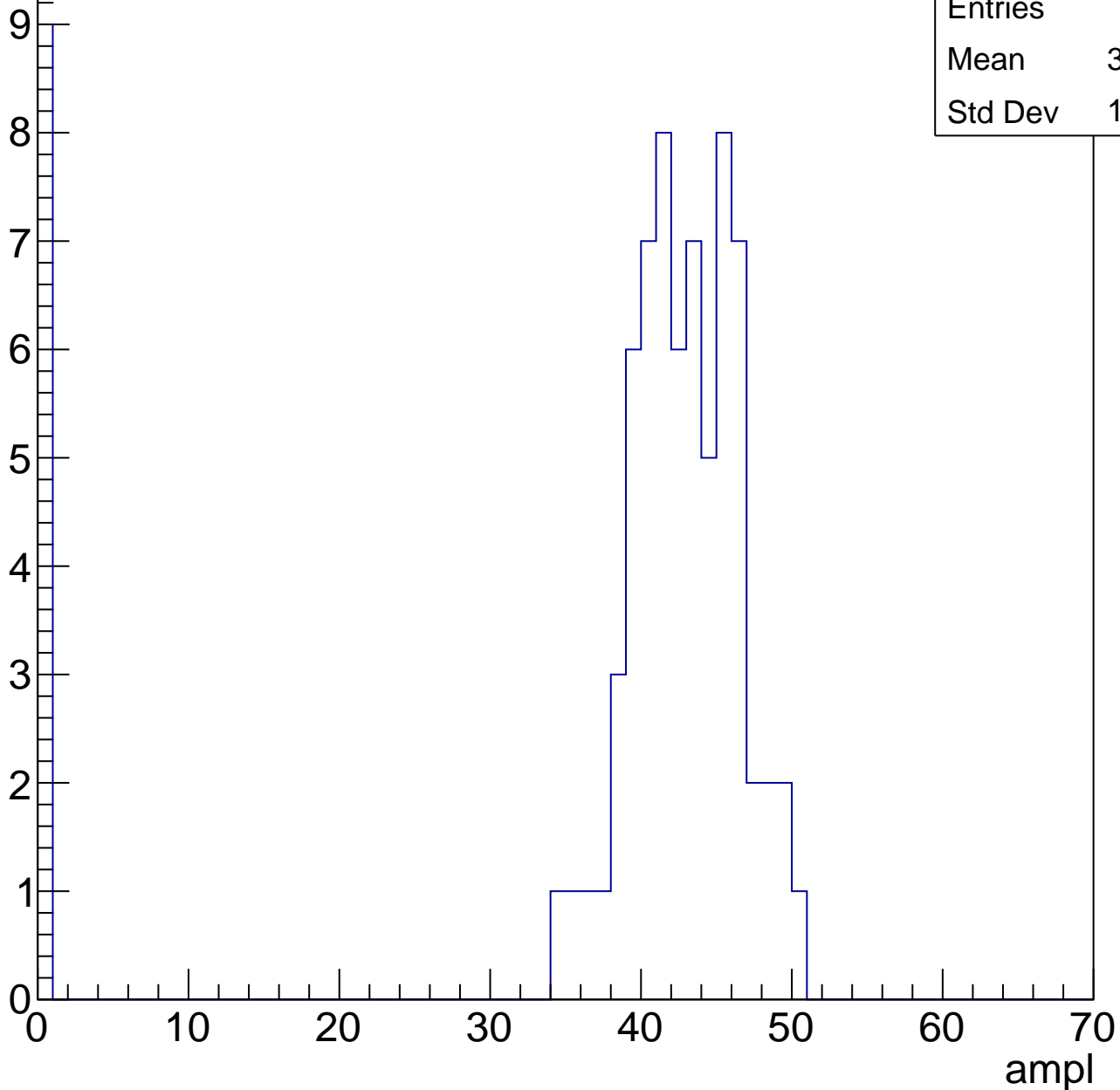


B1L103S, U9-ch97, adc2

calib_packv5_041523_1651.root, FC#0, port C2

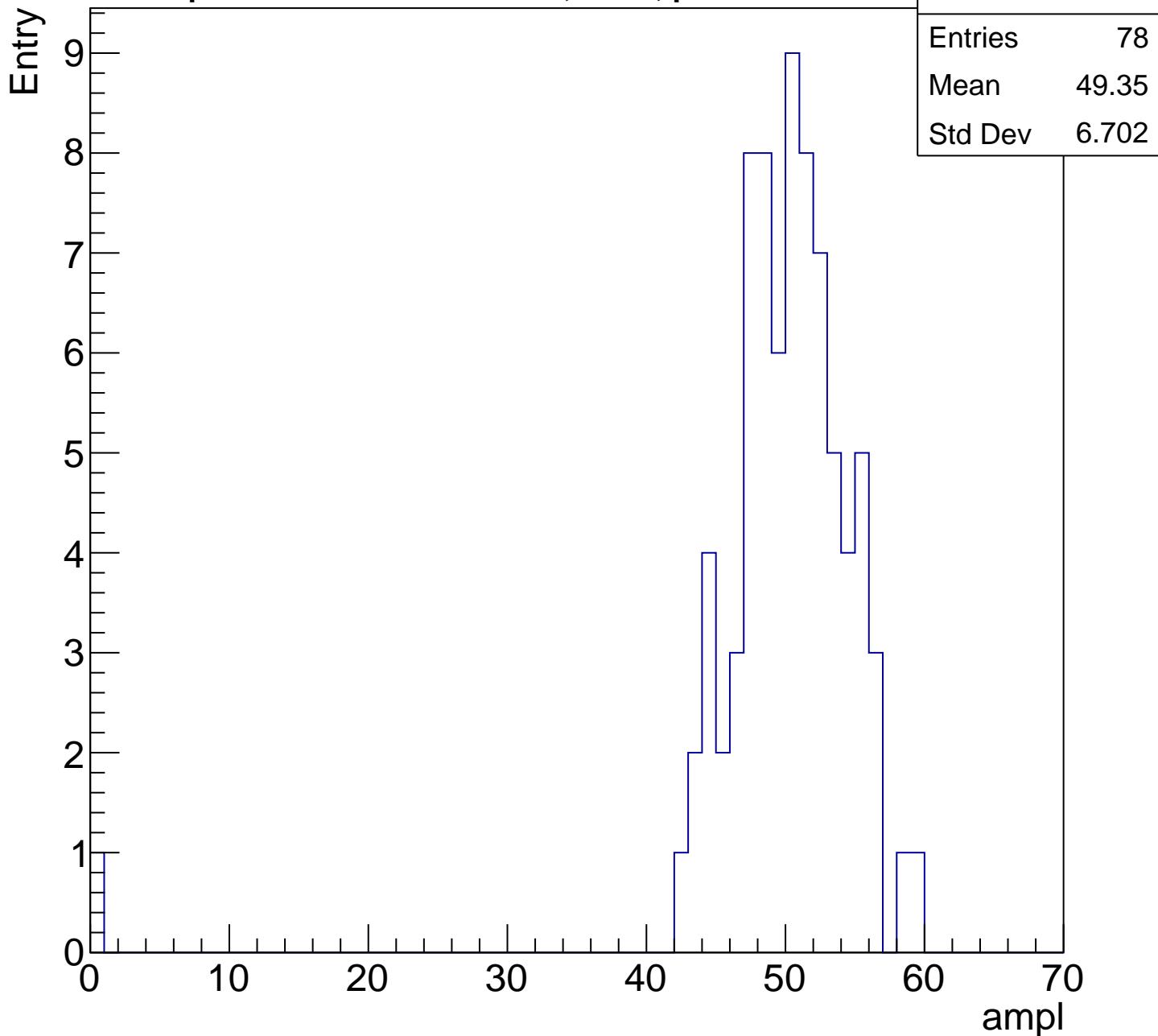
Entry

Entries	77
Mean	37.55
Std Dev	14.03



B1L103S, U9-ch97, adc3

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U9-ch97, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	61
Mean	56.66
Std Dev	3.284

Entry

10

8

6

4

2

0

0

10

20

30

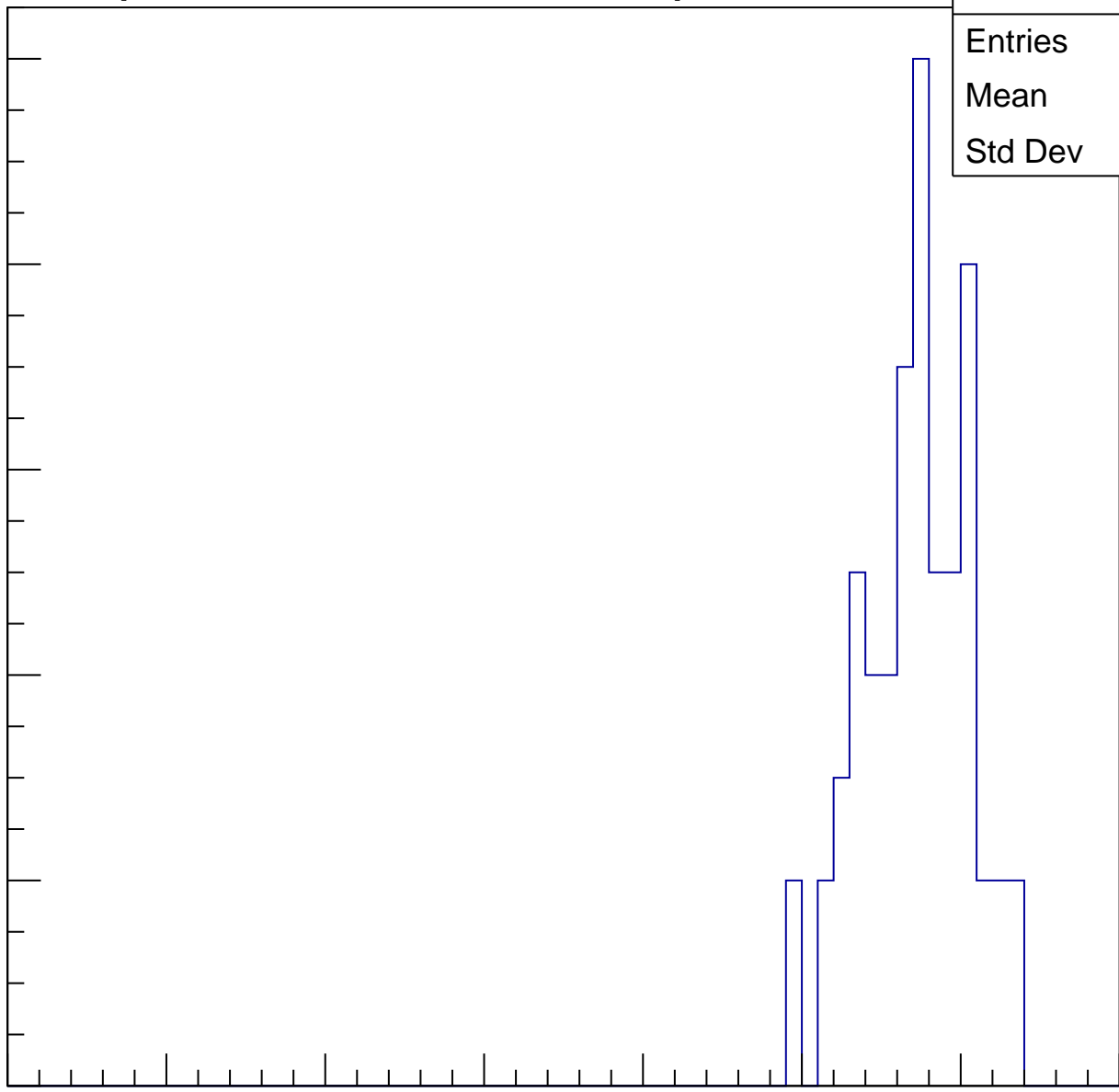
40

50

60

70

ampl

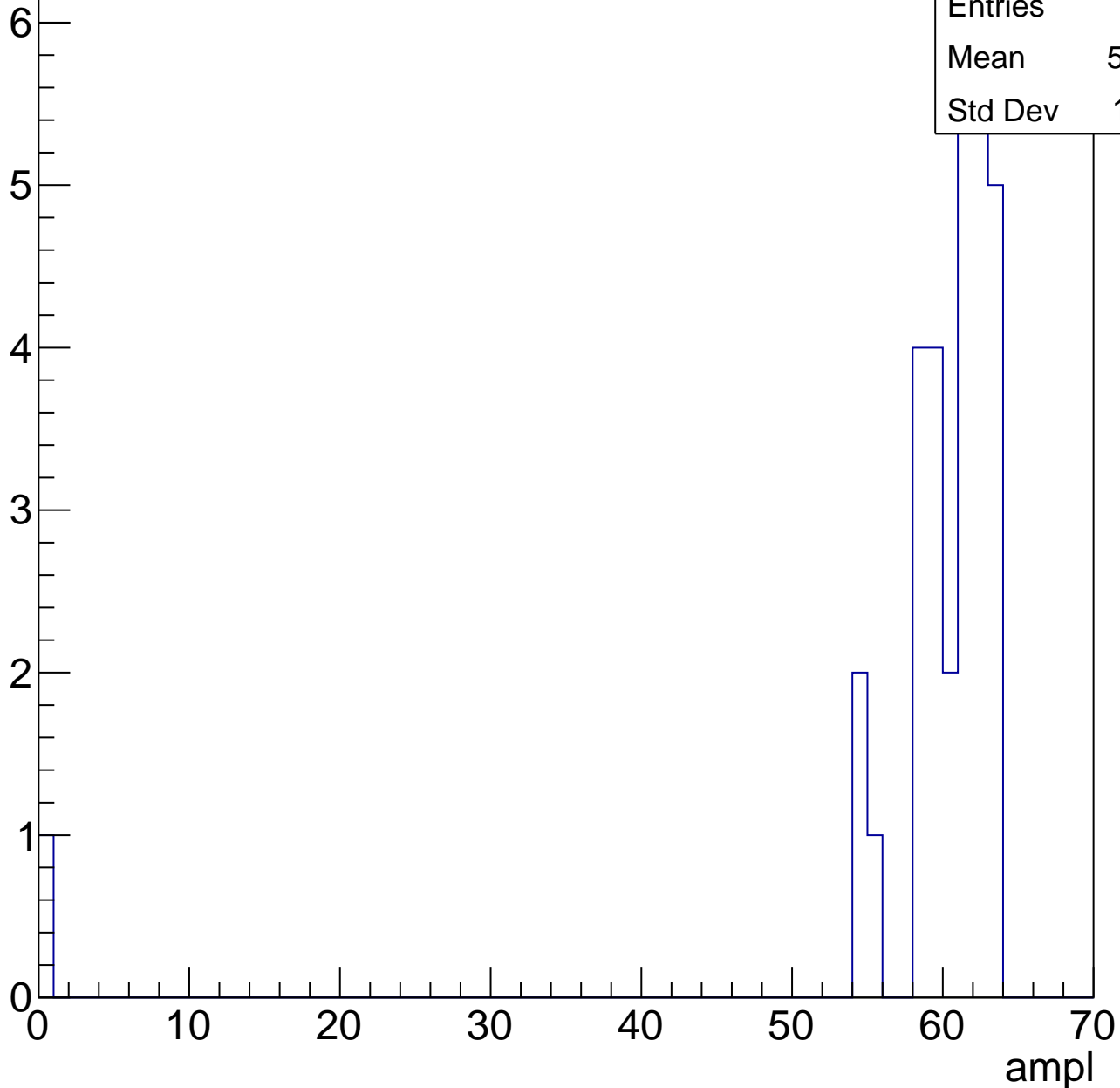


B1L103S, U9-ch97, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

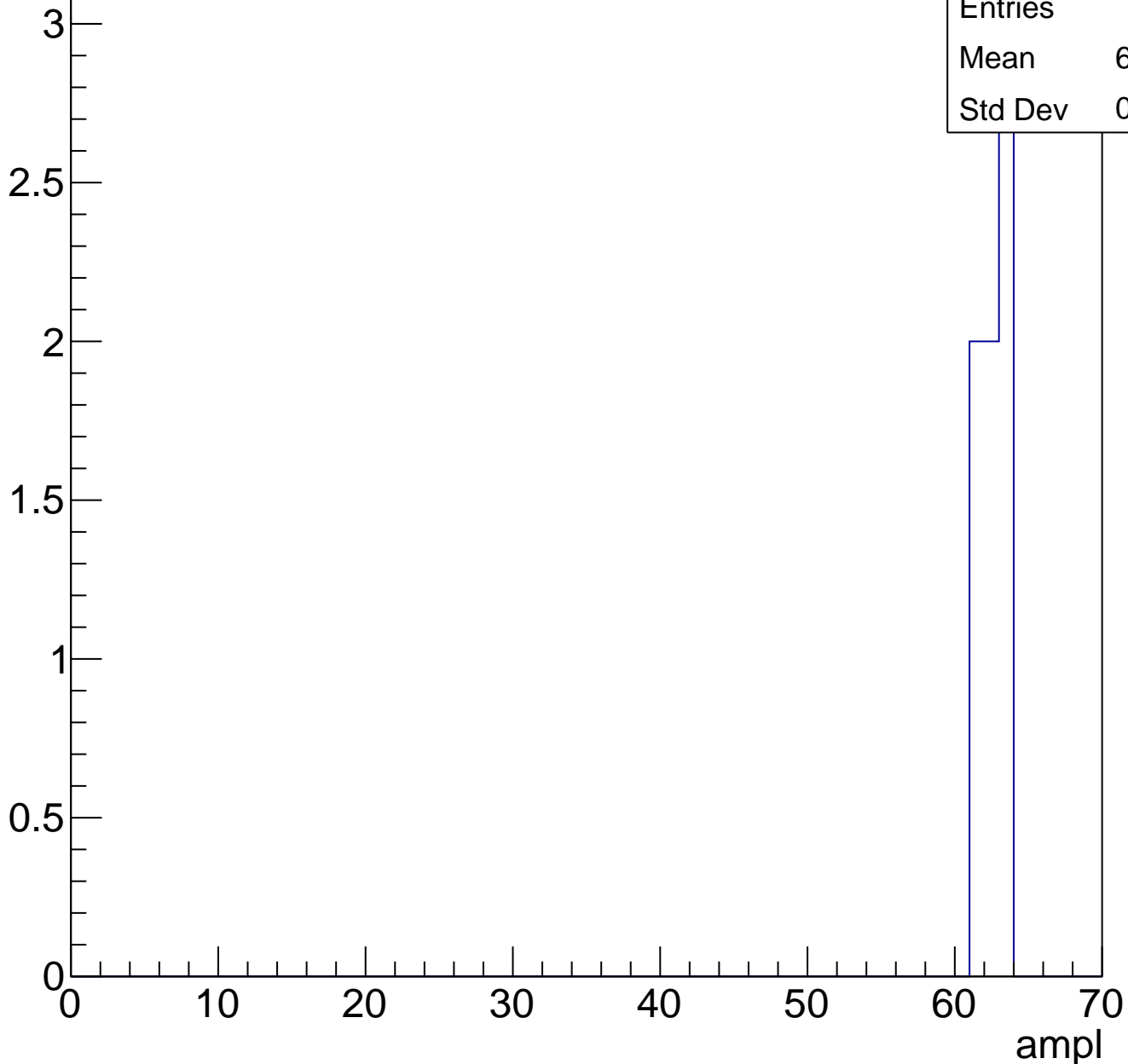
Entries	31
Mean	58.19
Std Dev	10.91



B1L103S, U9-ch97, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch97, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



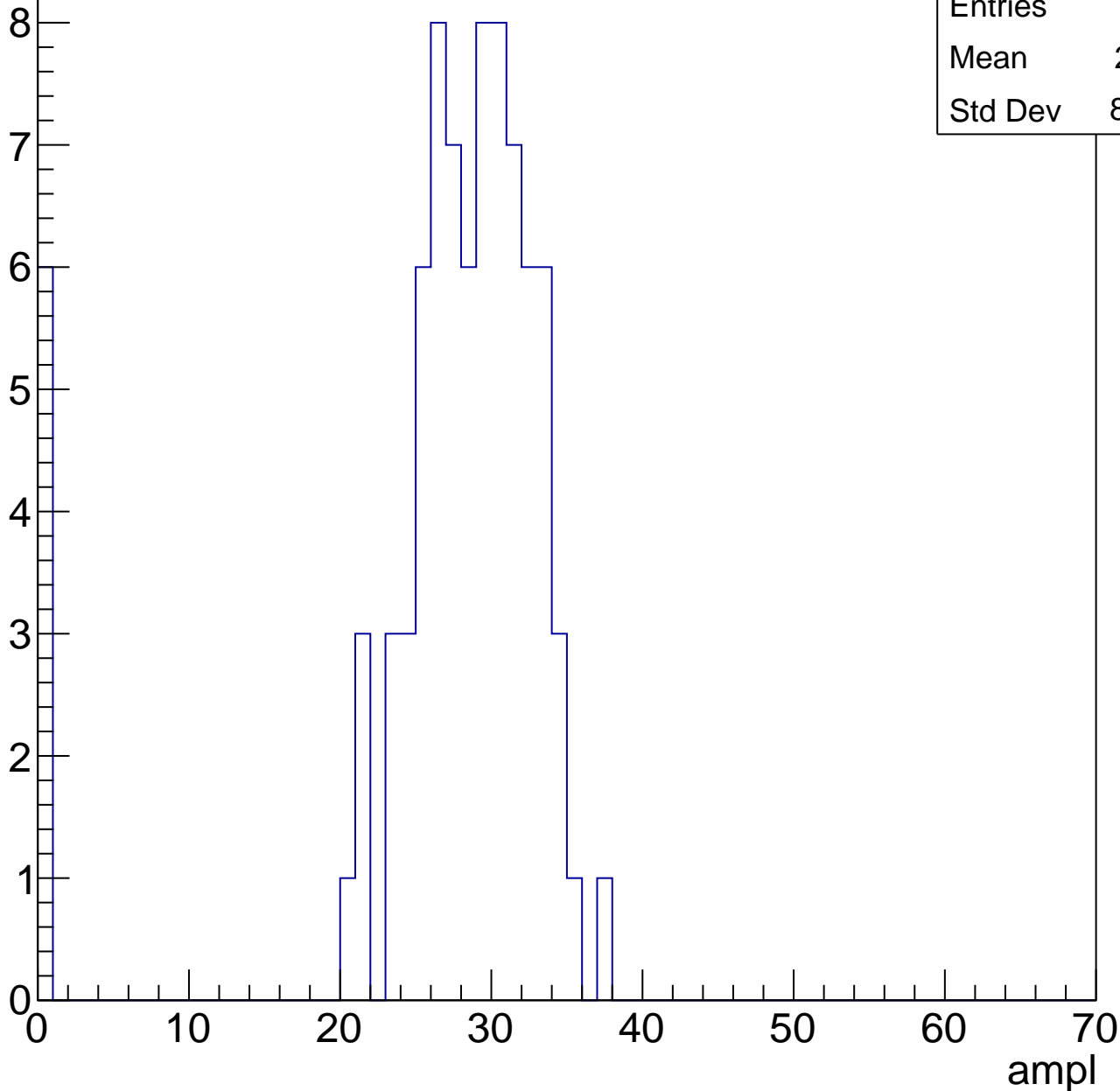
Entries	19
Mean	0
Std Dev	0

B1L103S, U9-ch98, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	83
Mean	26.41
Std Dev	8.146

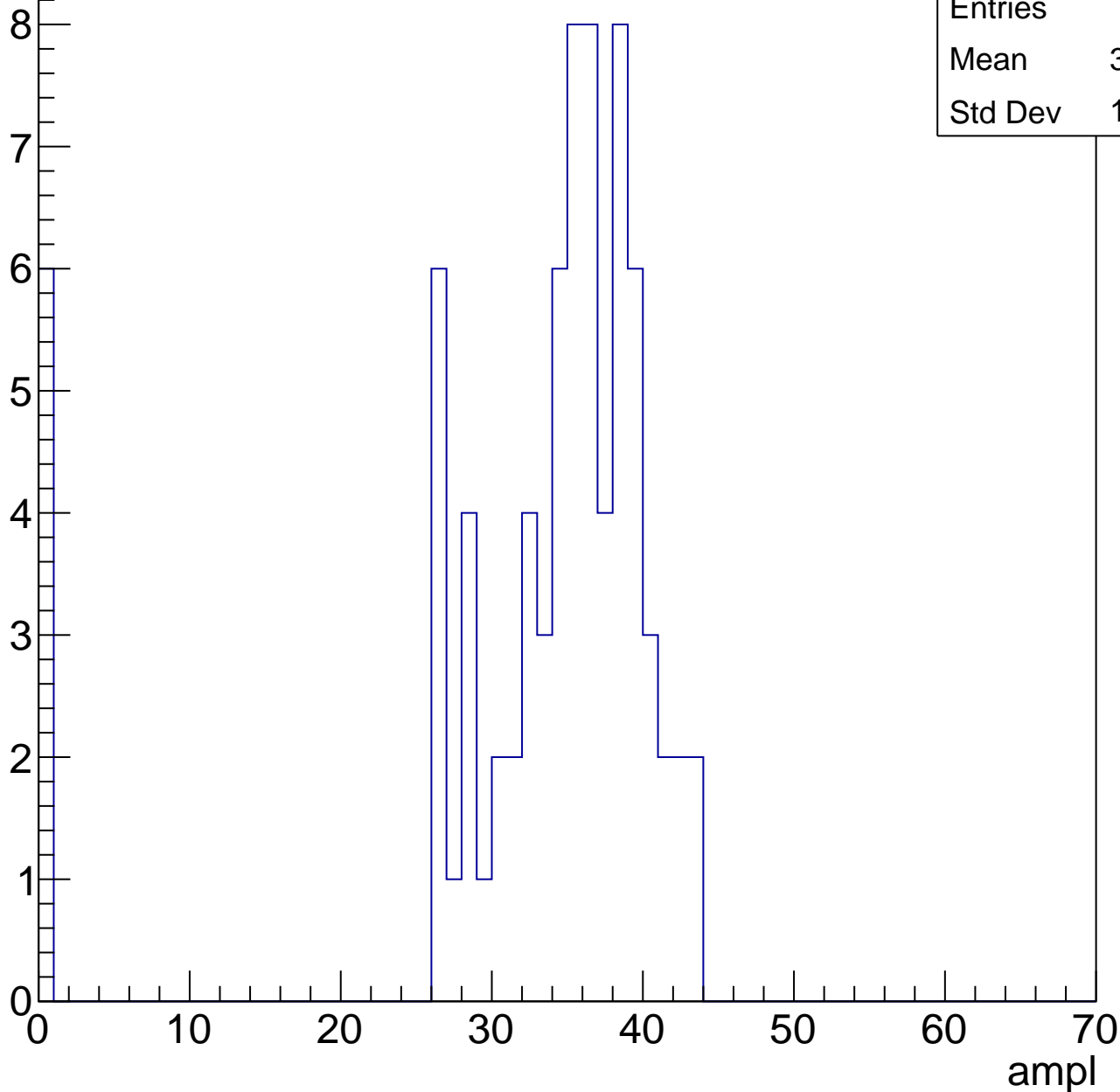


B1L103S, U9-ch98, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	32.09
Std Dev	10.24

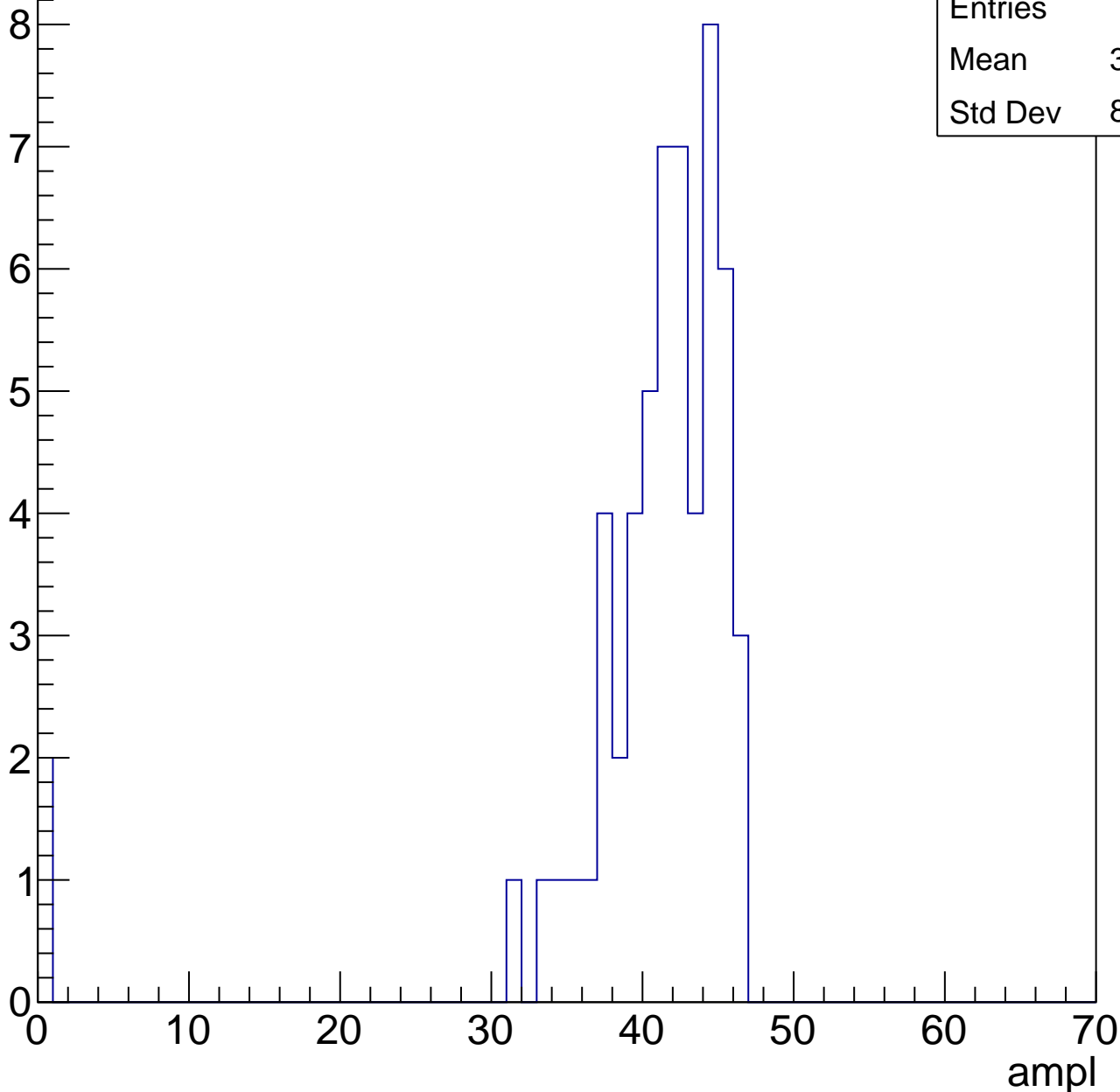


B1L103S, U9-ch98, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	39.68
Std Dev	8.278

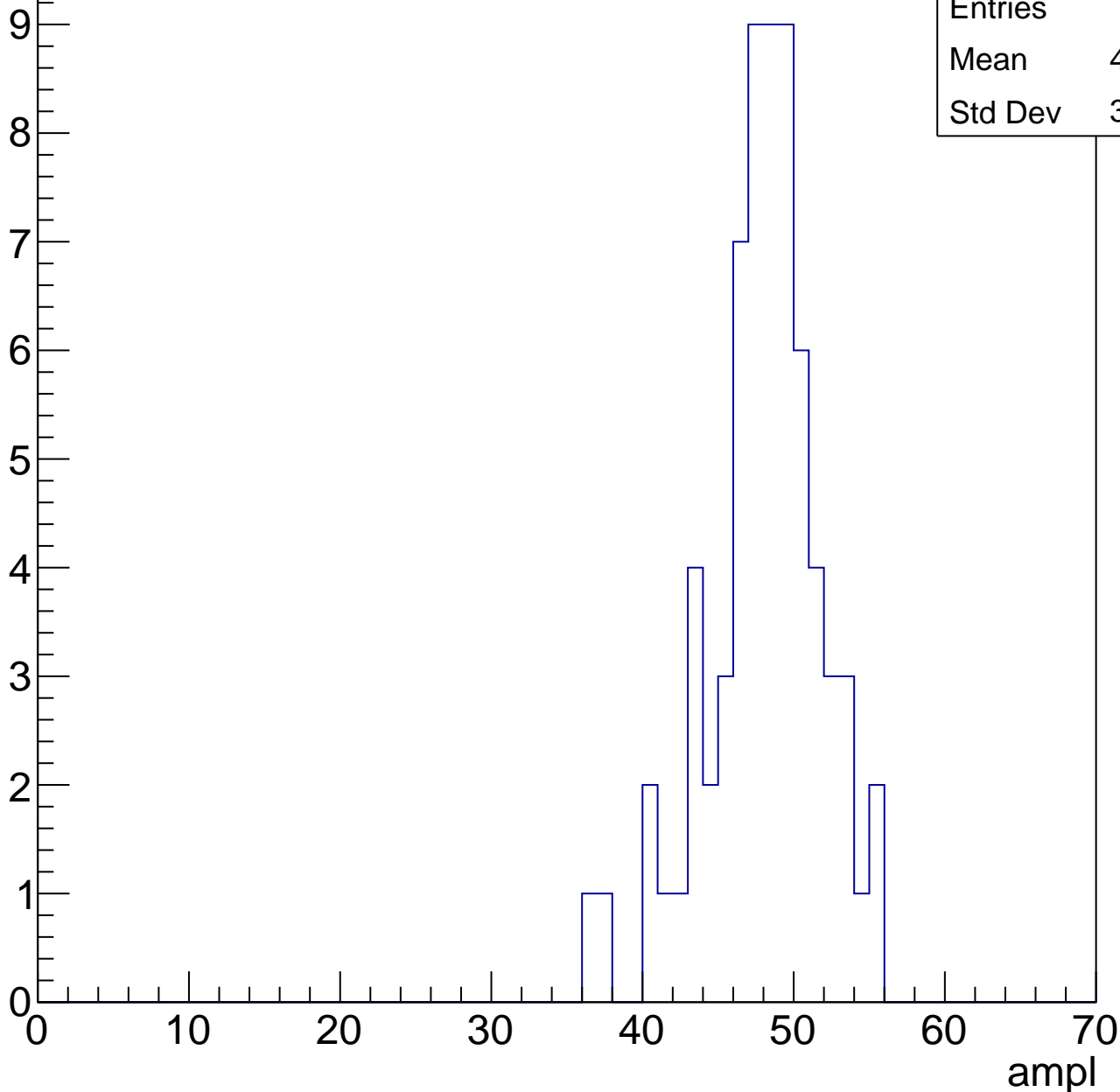


B1L103S, U9-ch98, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	47.53
Std Dev	3.806

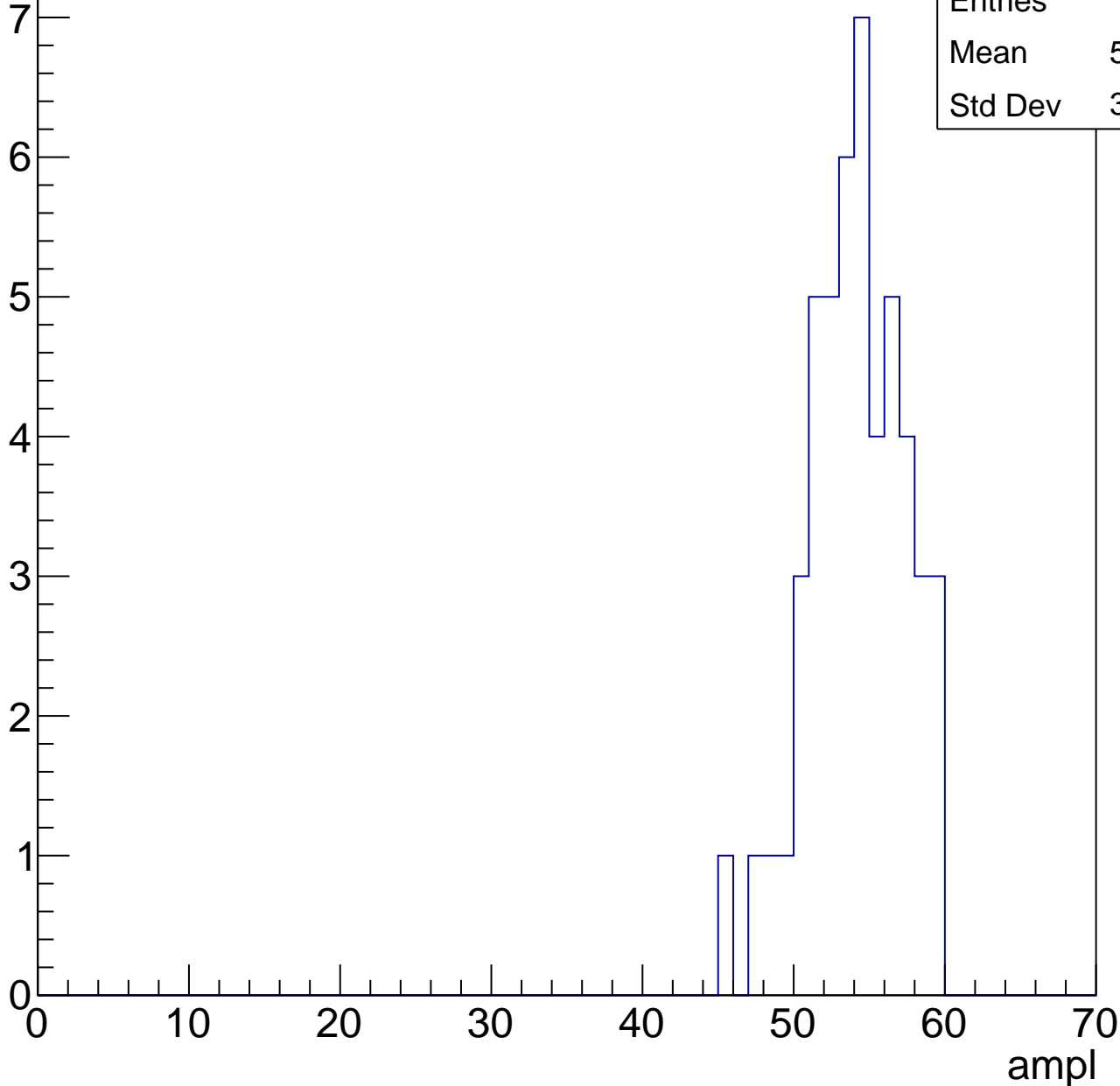


B1L103S, U9-ch98, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	53.65
Std Dev	3.153

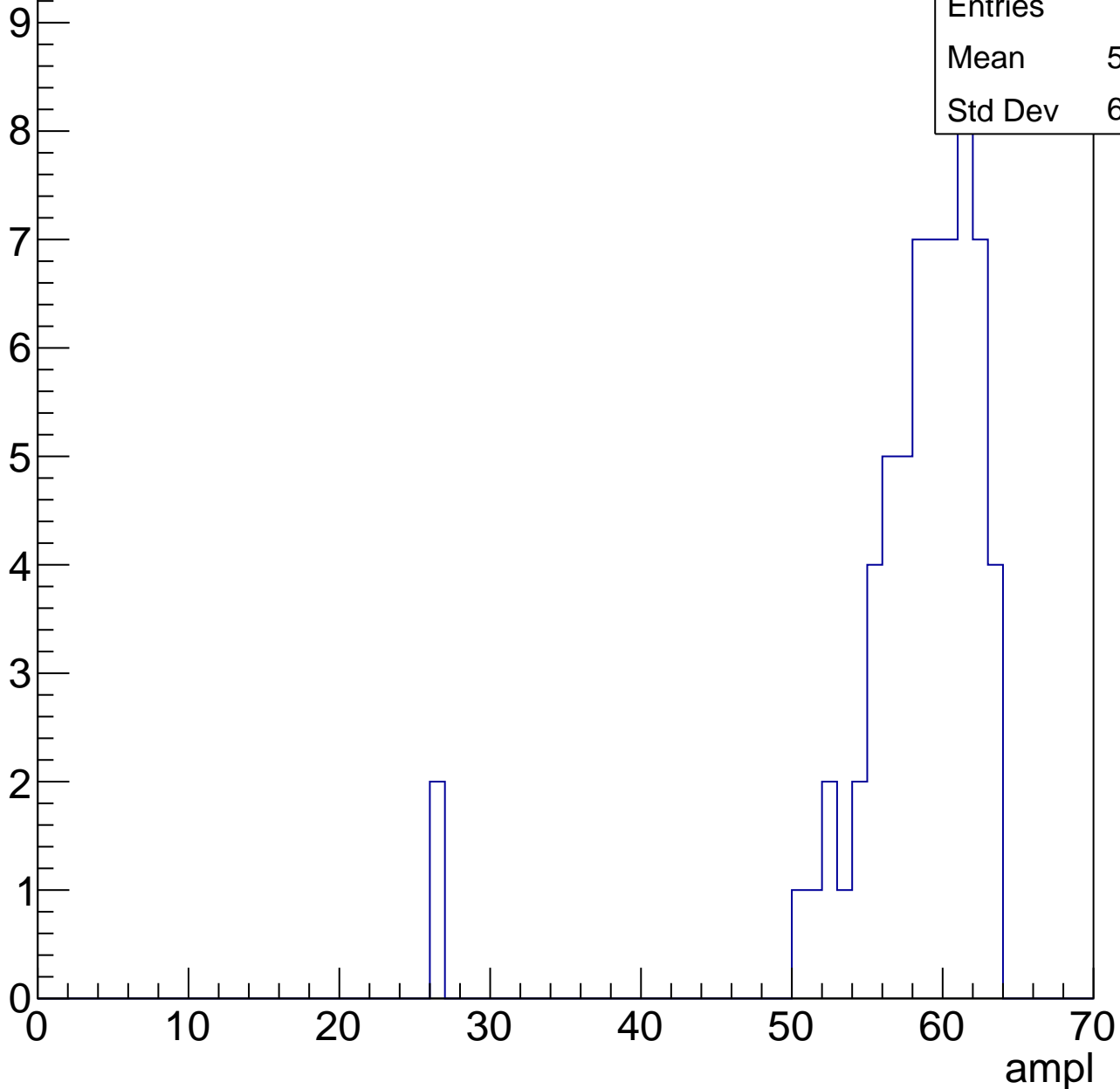


B1L103S, U9-ch98, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	57.45
Std Dev	6.447

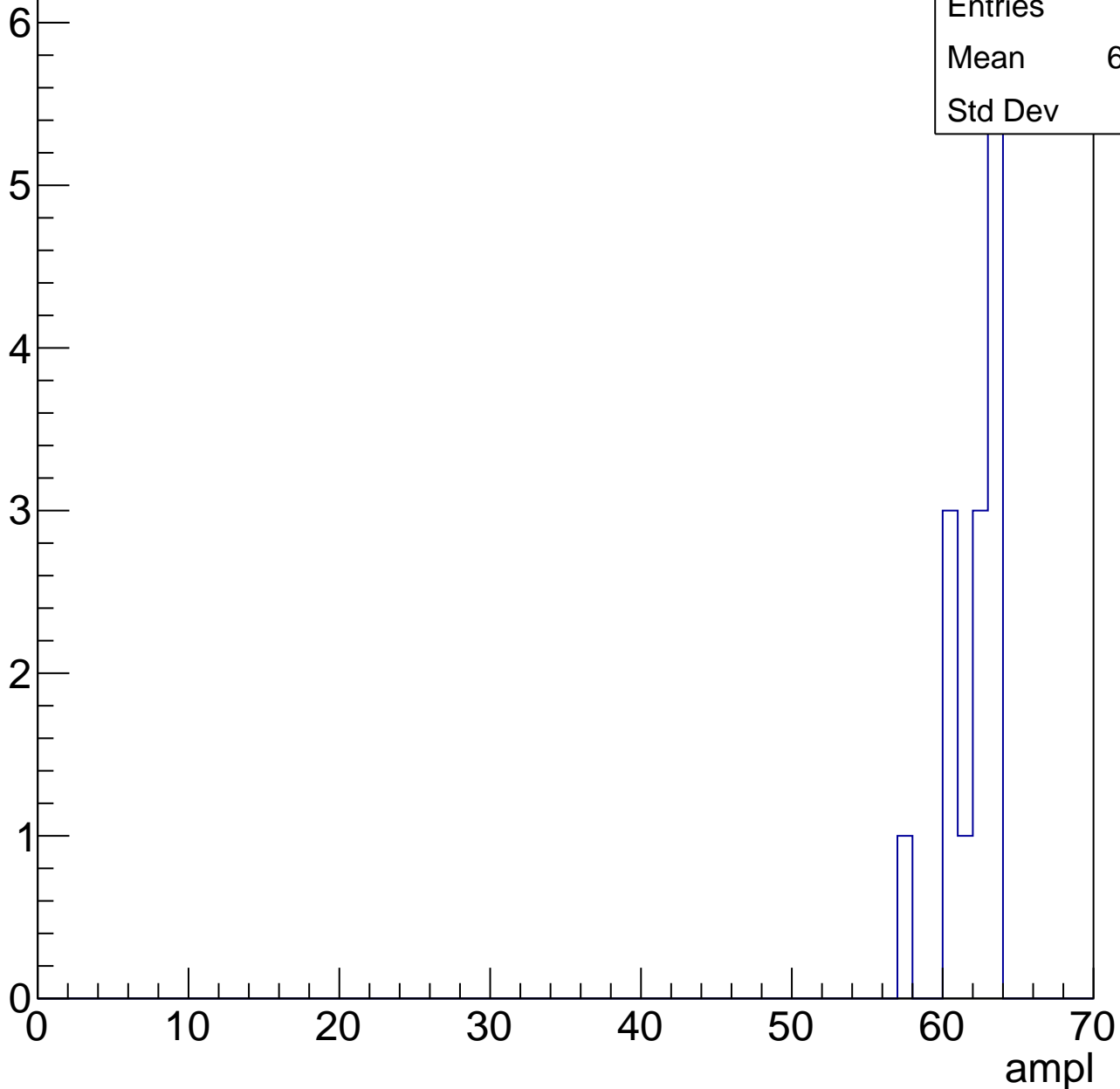


B1L103S, U9-ch98, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	14
Mean	61.57
Std Dev	1.72

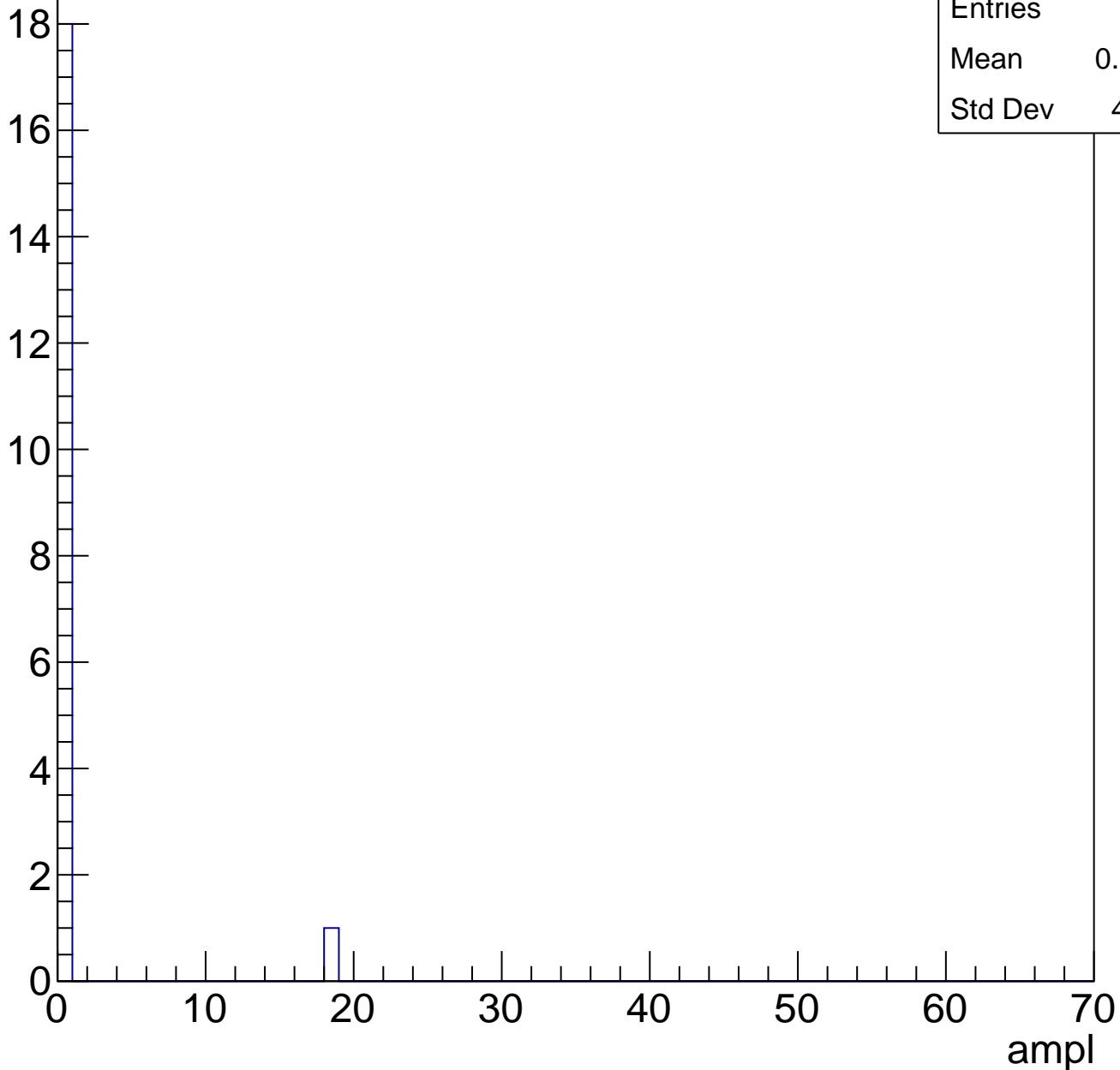


B1L103S, U9-ch98, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	0.9474
Std Dev	4.019

Entry



B1L103S, U9-ch99, adc0

calib_packv5_041523_1651.root, FC#0, port C2

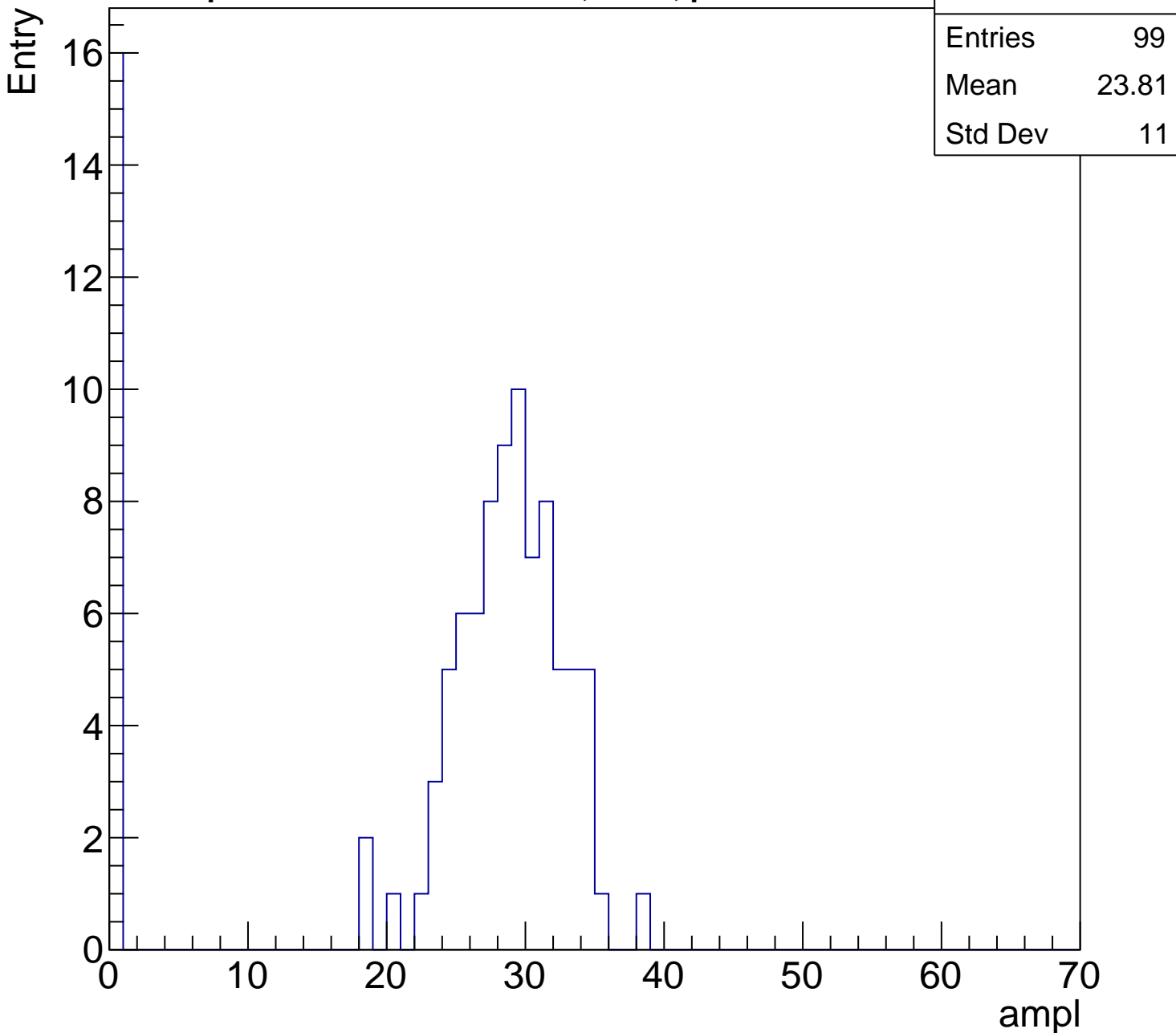
Entries	99
Mean	23.81
Std Dev	11

Entry

16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

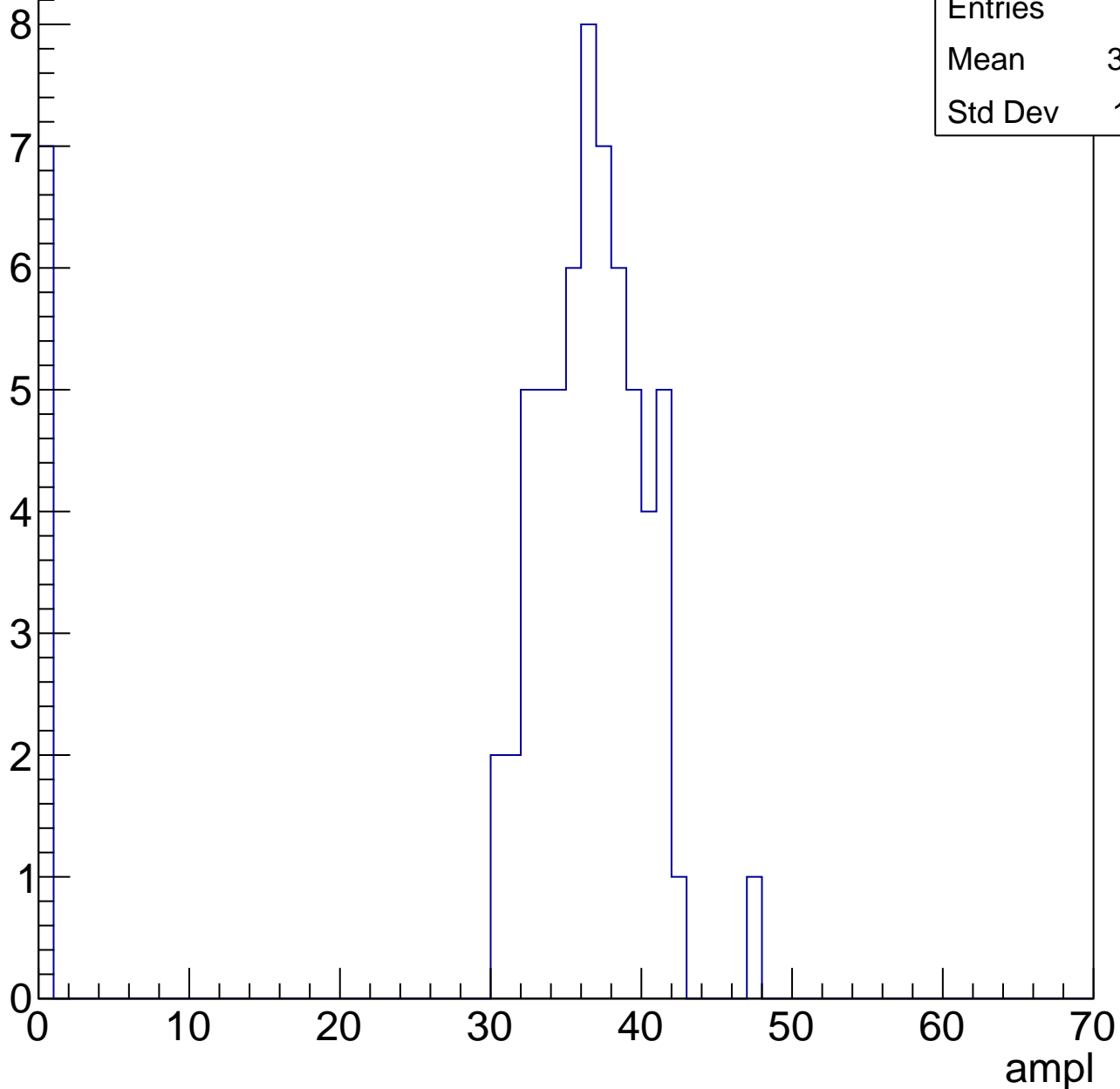


B1L103S, U9-ch99, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	32.62
Std Dev	11.41

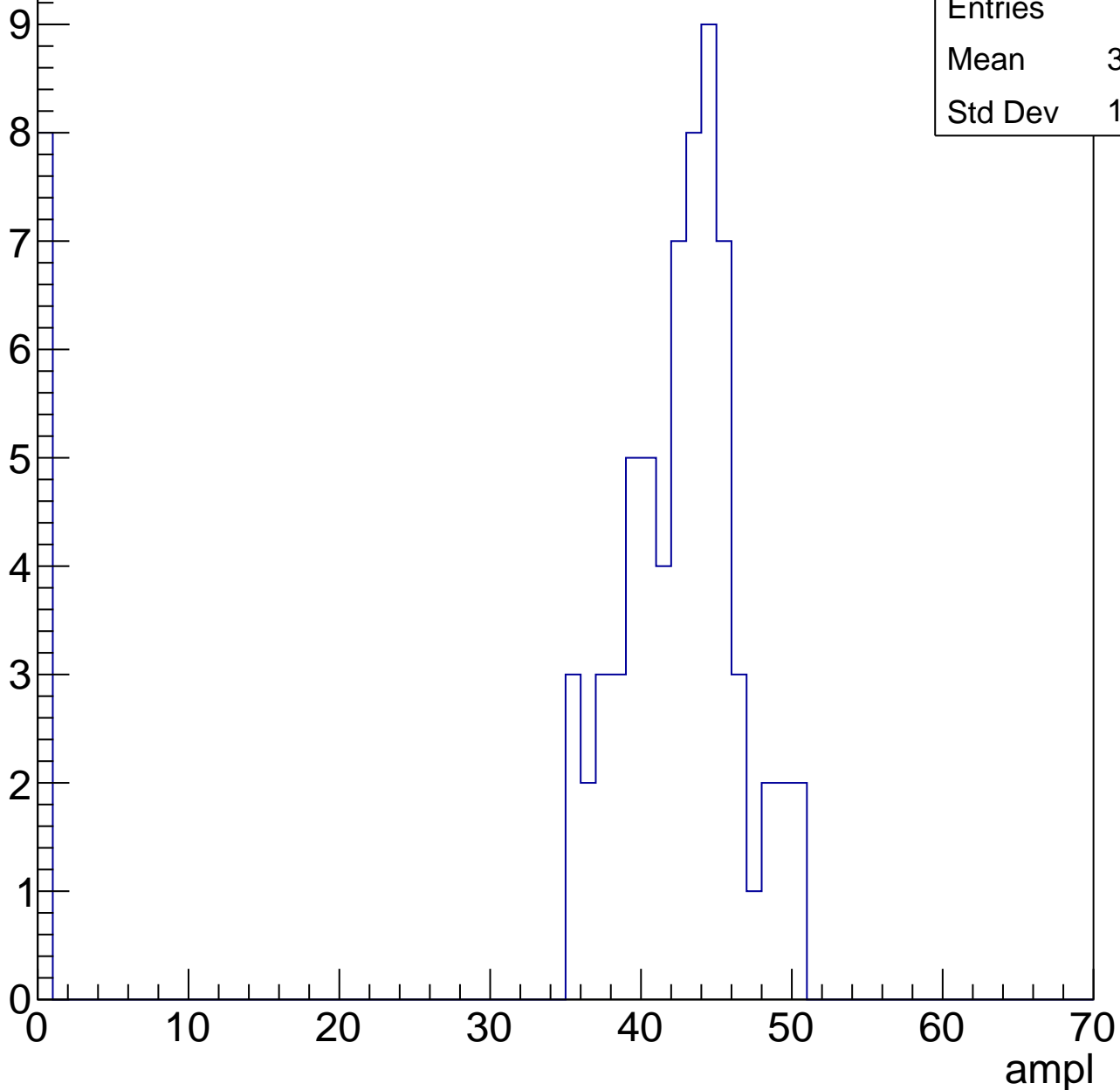


B1L103S, U9-ch99, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	37.69
Std Dev	13.57

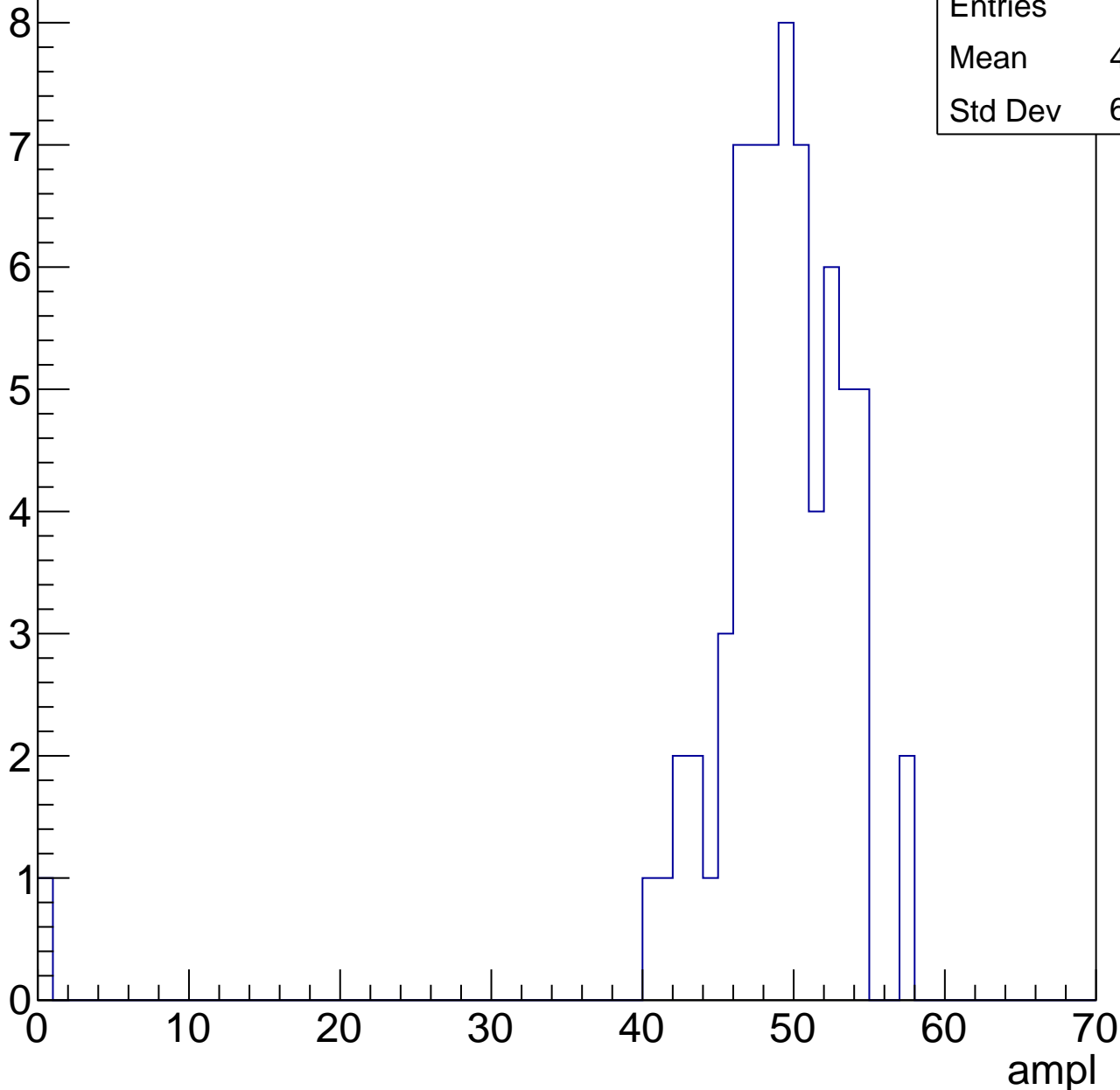


B1L103S, U9-ch99, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	48.17
Std Dev	6.863



B1L103S, U9-ch99, adc4

calib_packv5_041523_1651.root, FC#0, port C2

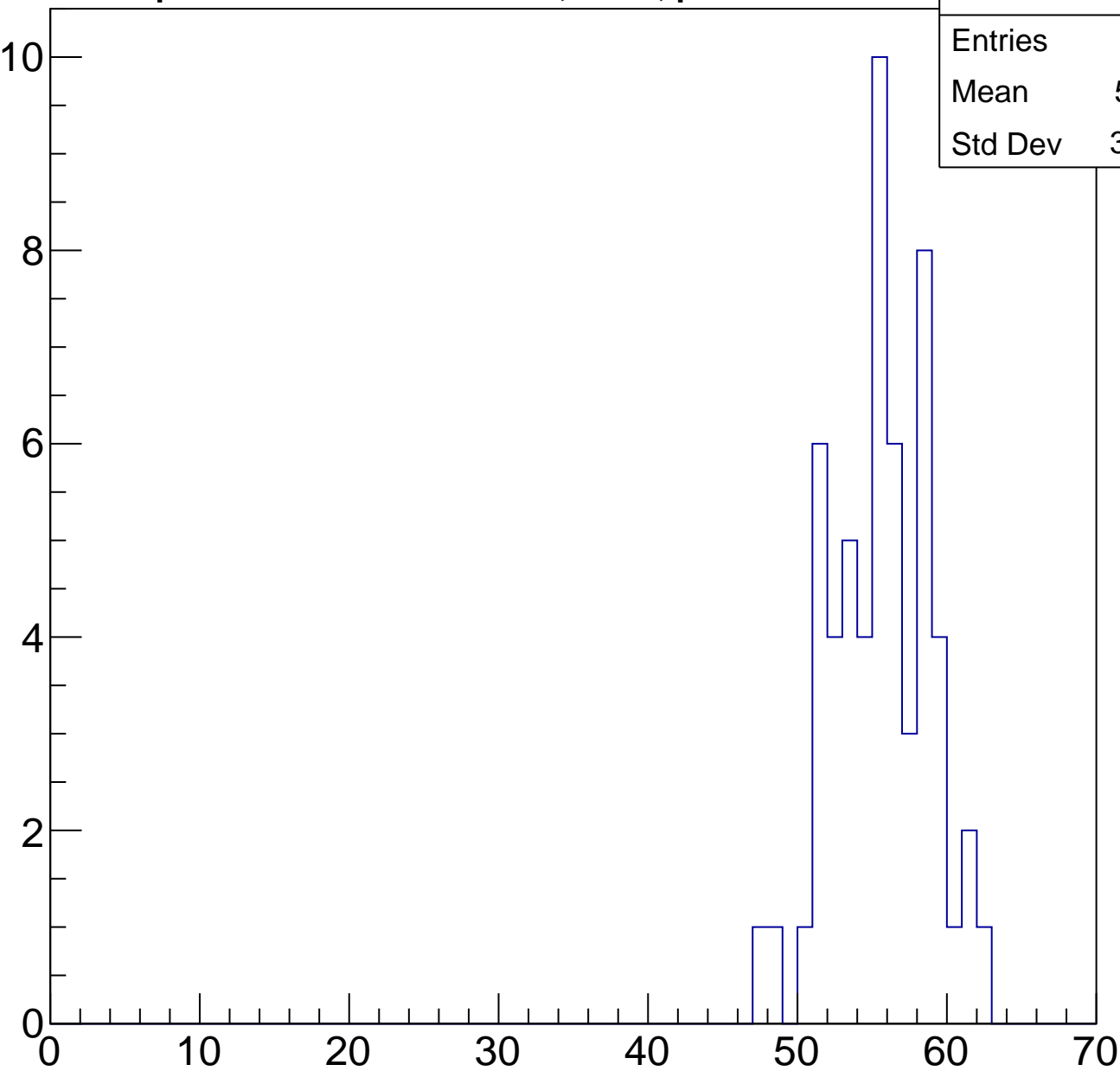
Entries	57
Mean	55.11
Std Dev	3.226

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

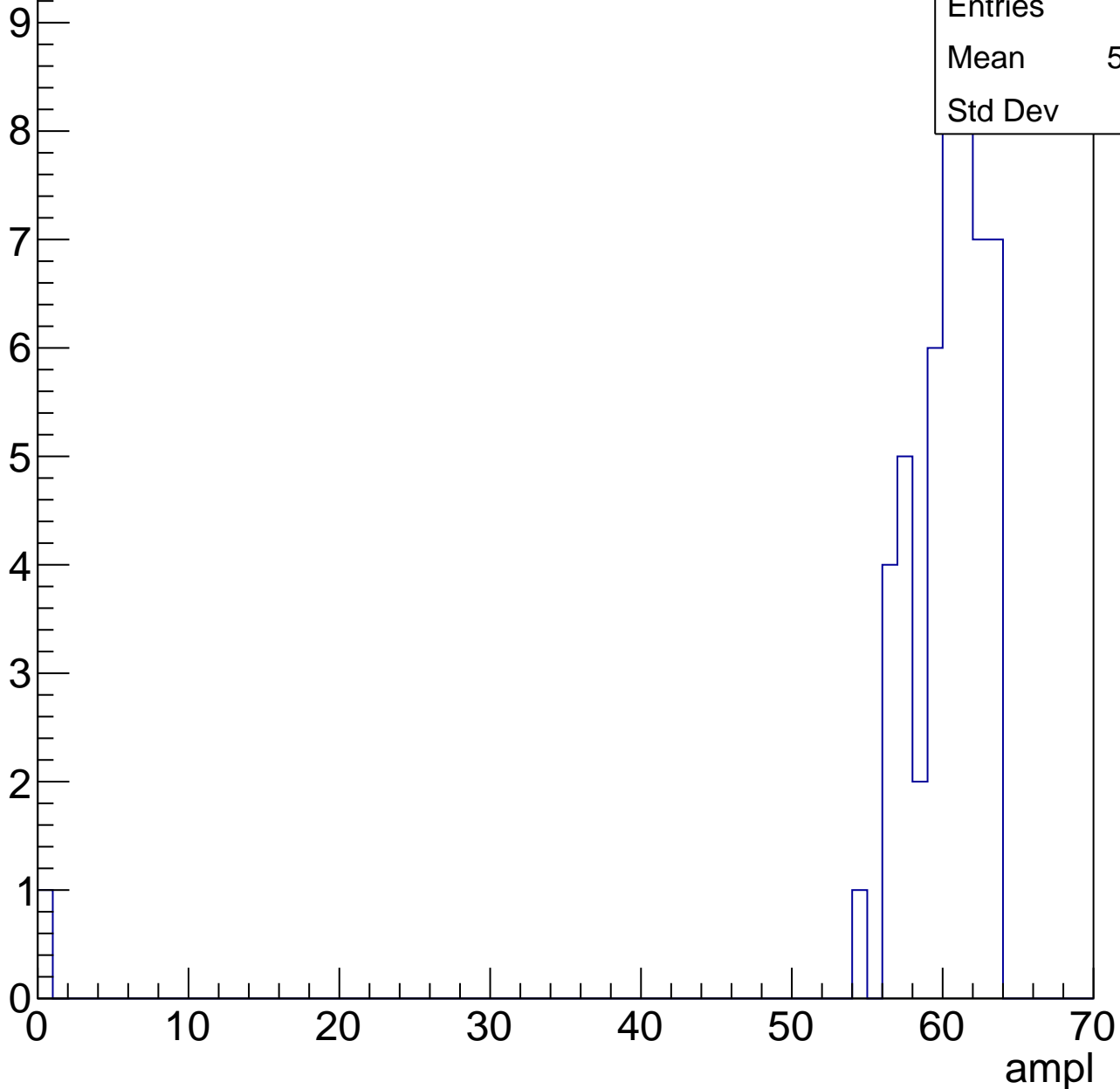


B1L103S, U9-ch99, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	58.72
Std Dev	8.69



B1L103S, U9-ch99, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	4
Mean	62.5
Std Dev	0.5

B1L103S, U9-ch99, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	3.316
Std Dev	14.07

ampl

0 10 20 30 40 50 60 70

B1L103S, U9-ch100, adc0

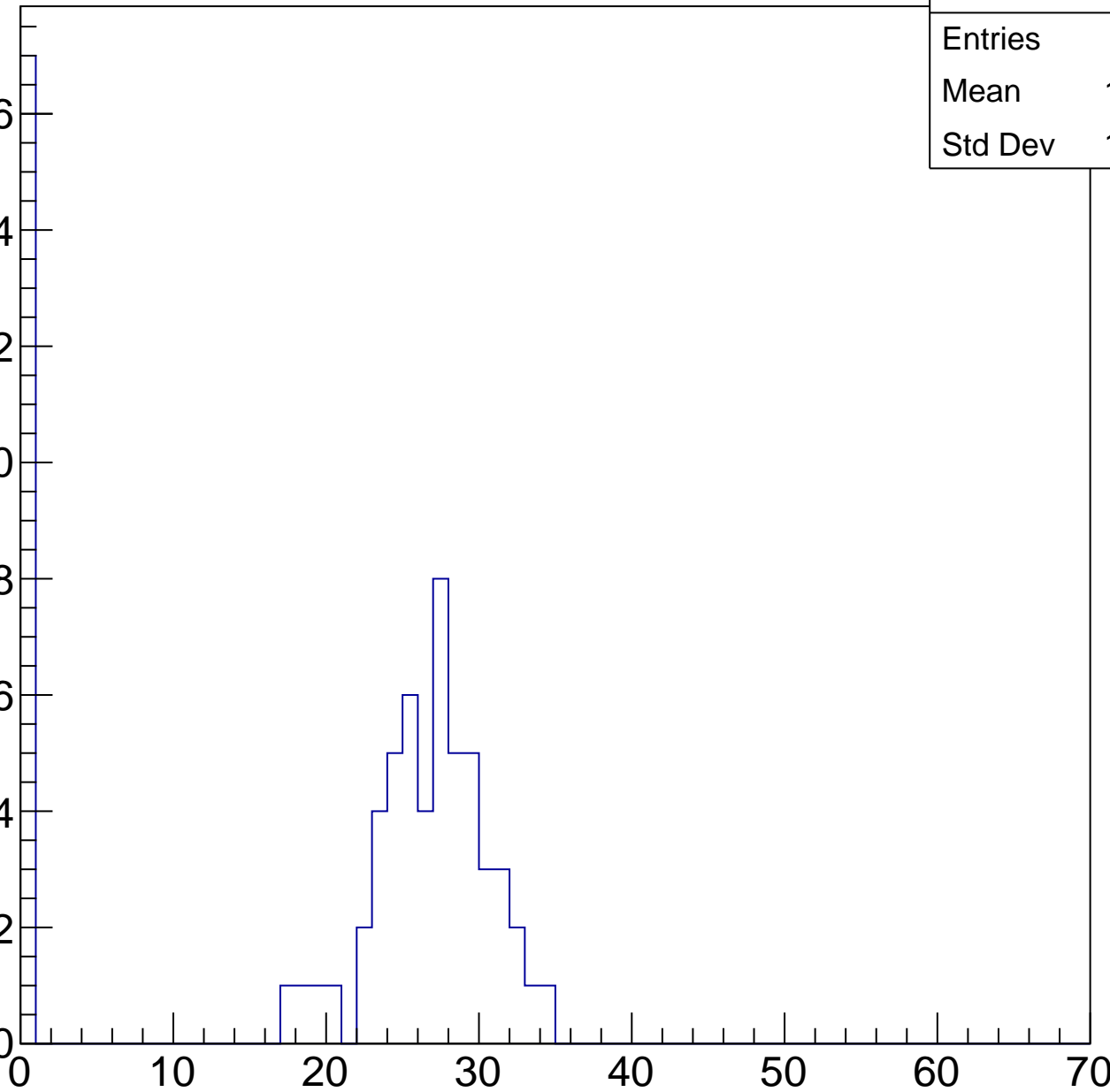
calib_packv5_041523_1651.root, FC#0, port C2

Entries	70
Mean	19.99
Std Dev	11.75

Entry

16
14
12
10
8
6
4
2
0

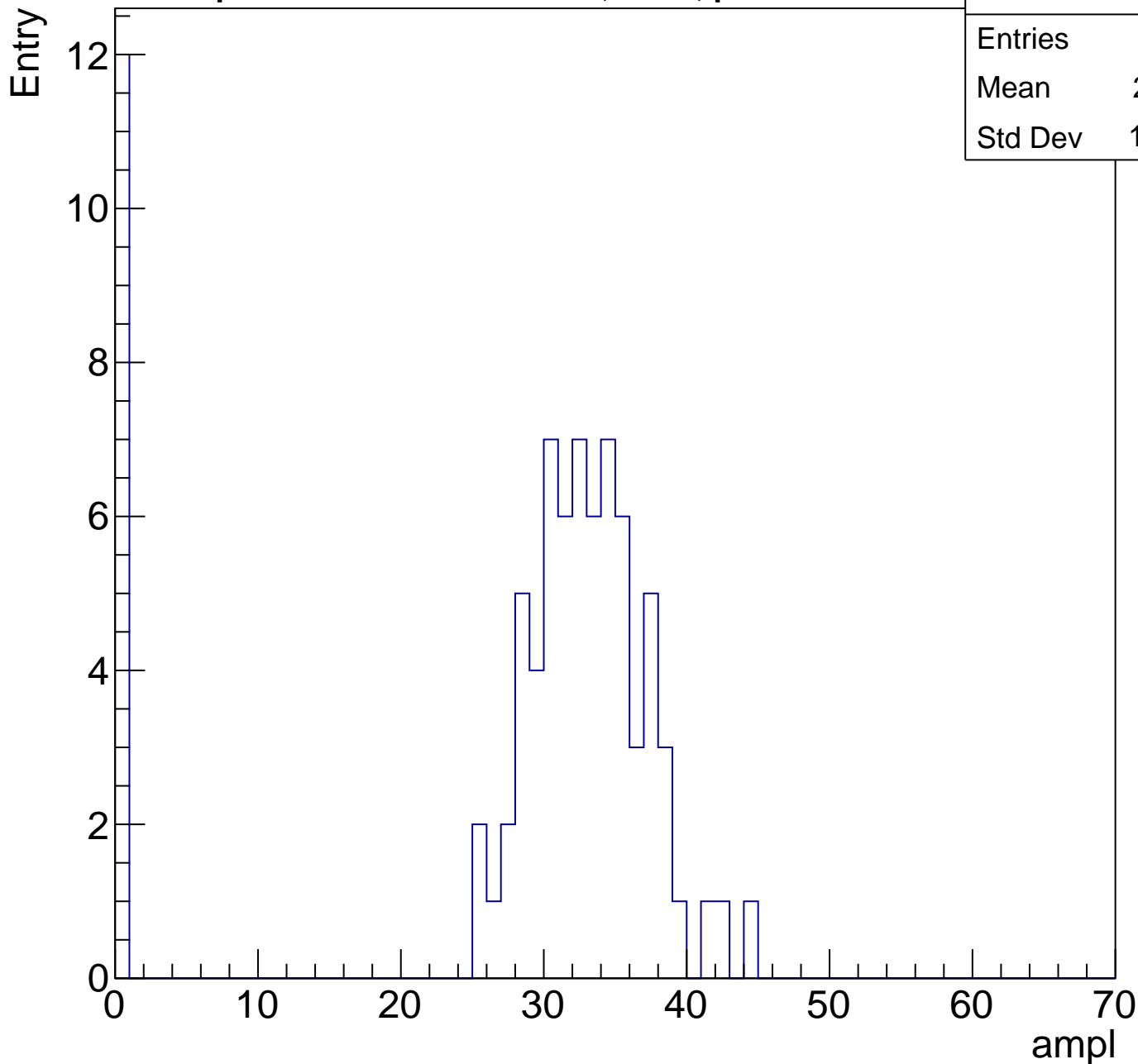
ampl



B1L103S, U9-ch100, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	27.81
Std Dev	12.23

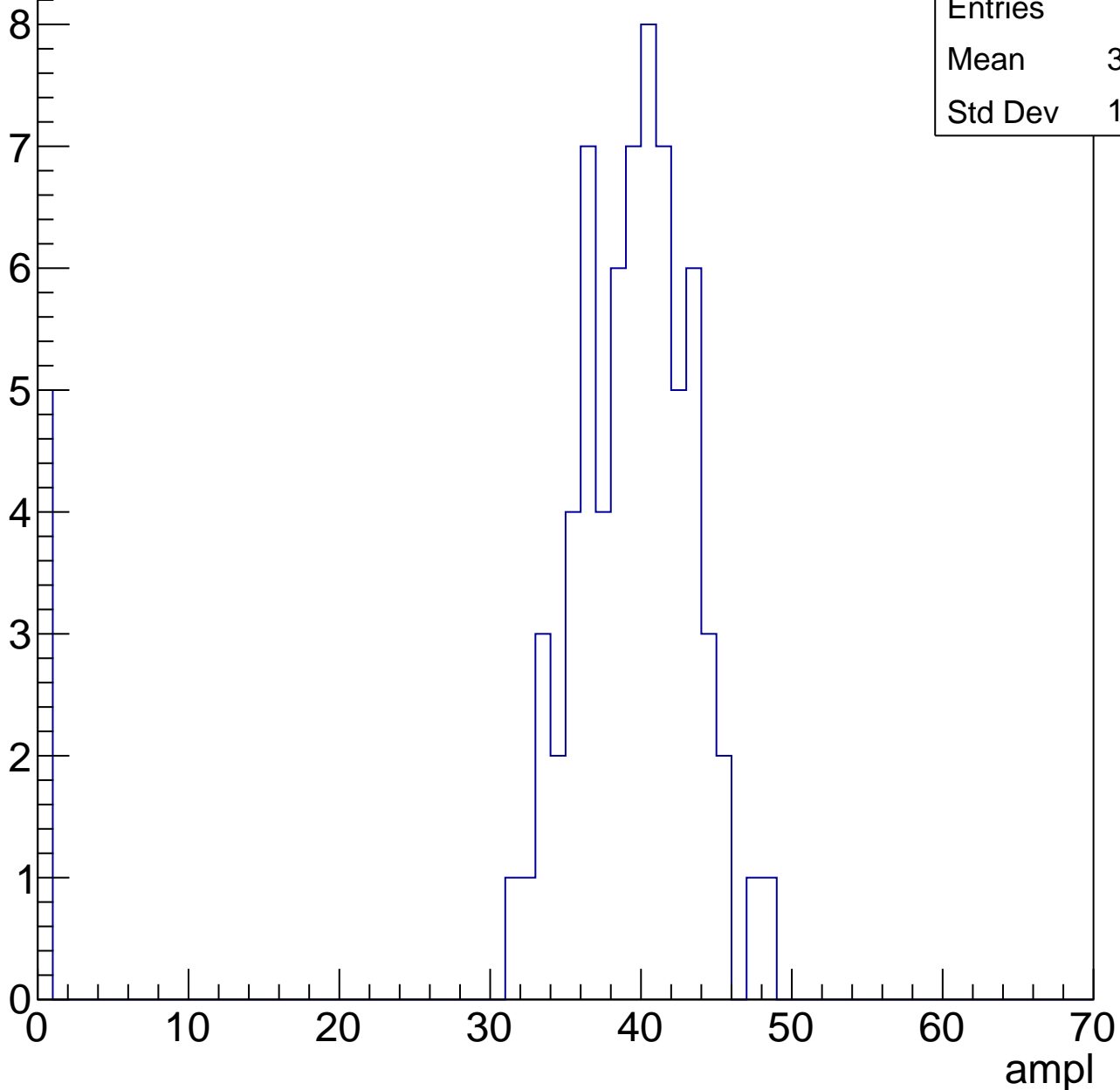


B1L103S, U9-ch100, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	36.48
Std Dev	10.49

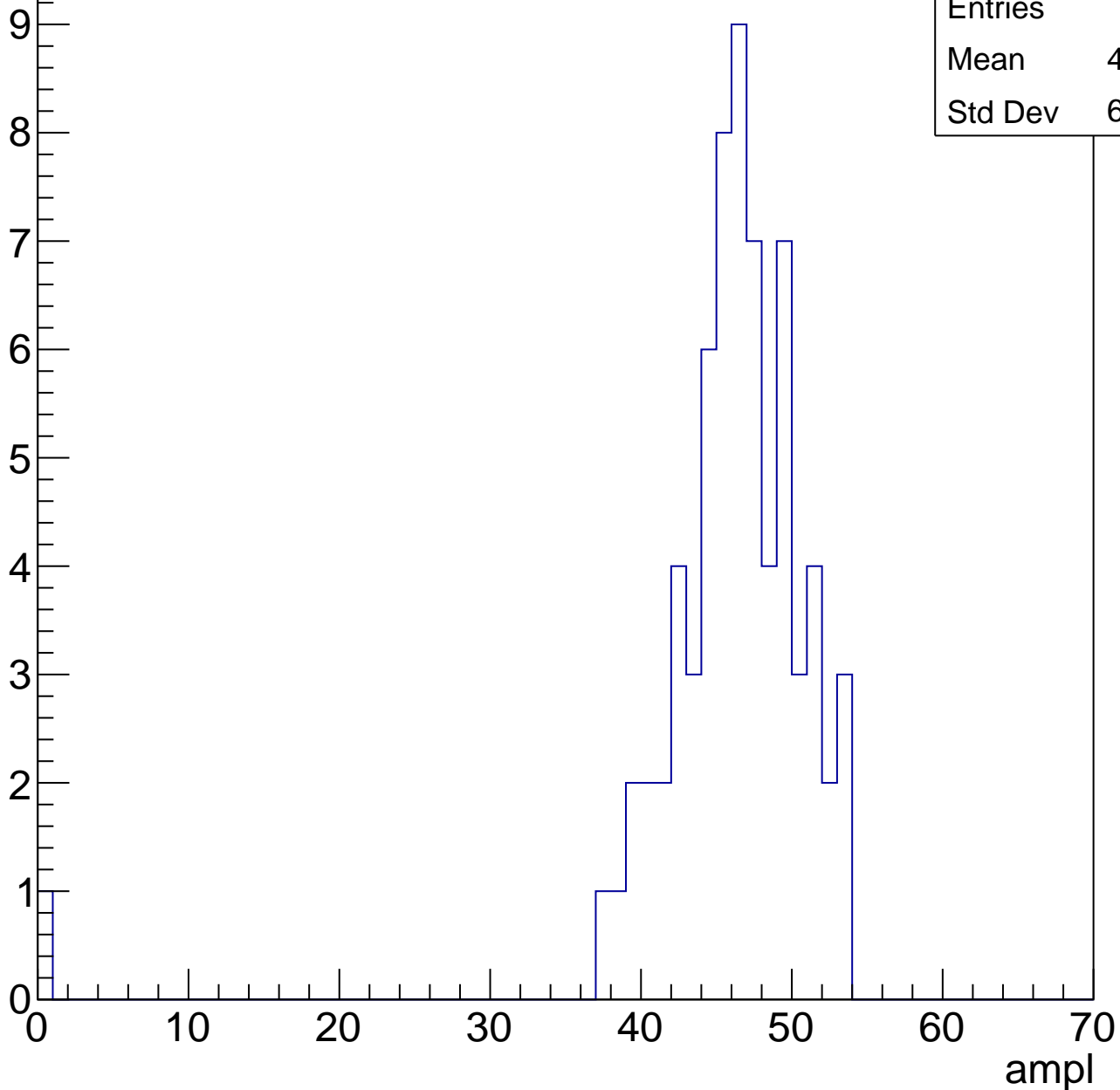


B1L103S, U9-ch100, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	45.38
Std Dev	6.627

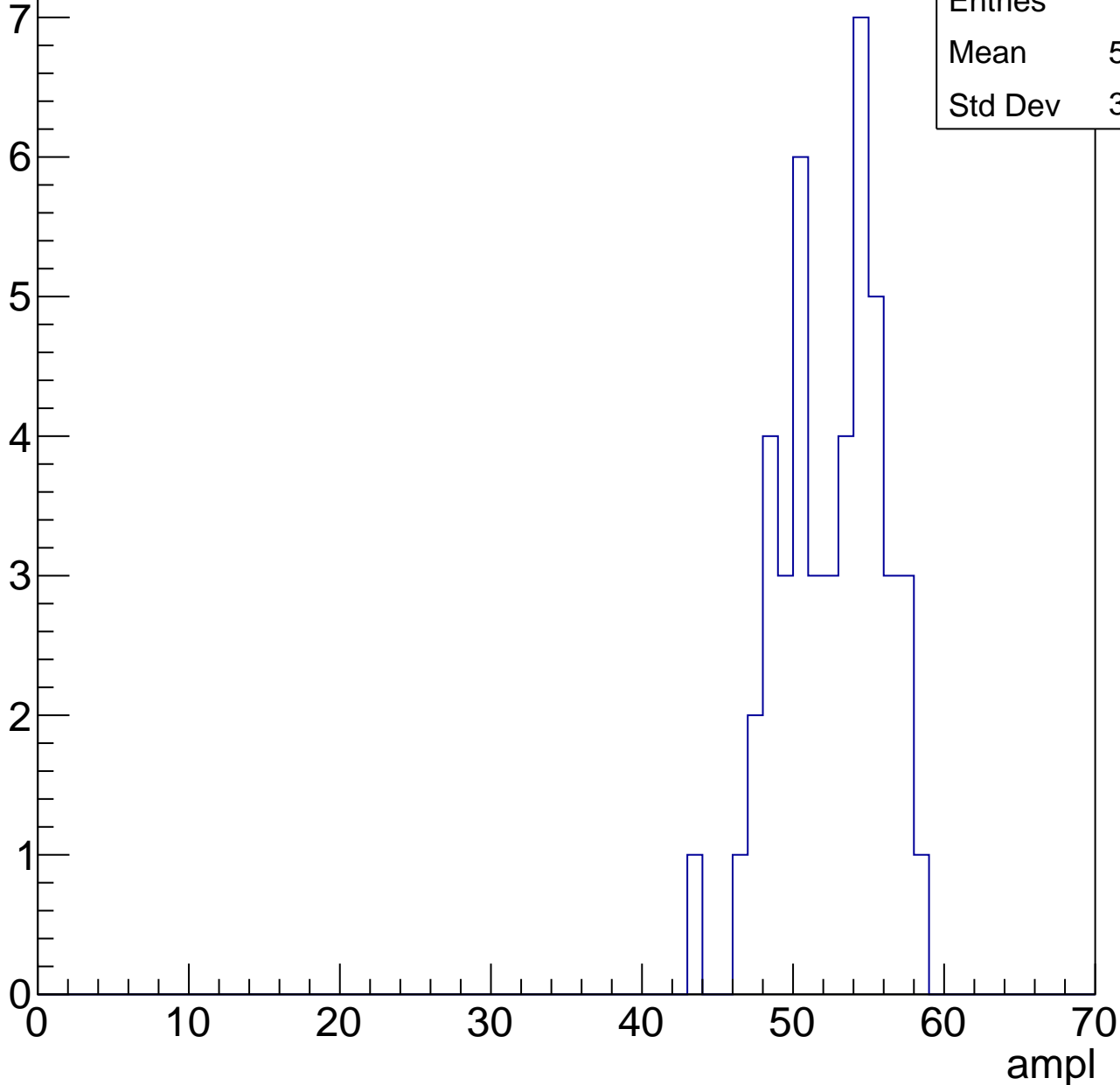


B1L103S, U9-ch100, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	46
Mean	52.02
Std Dev	3.365

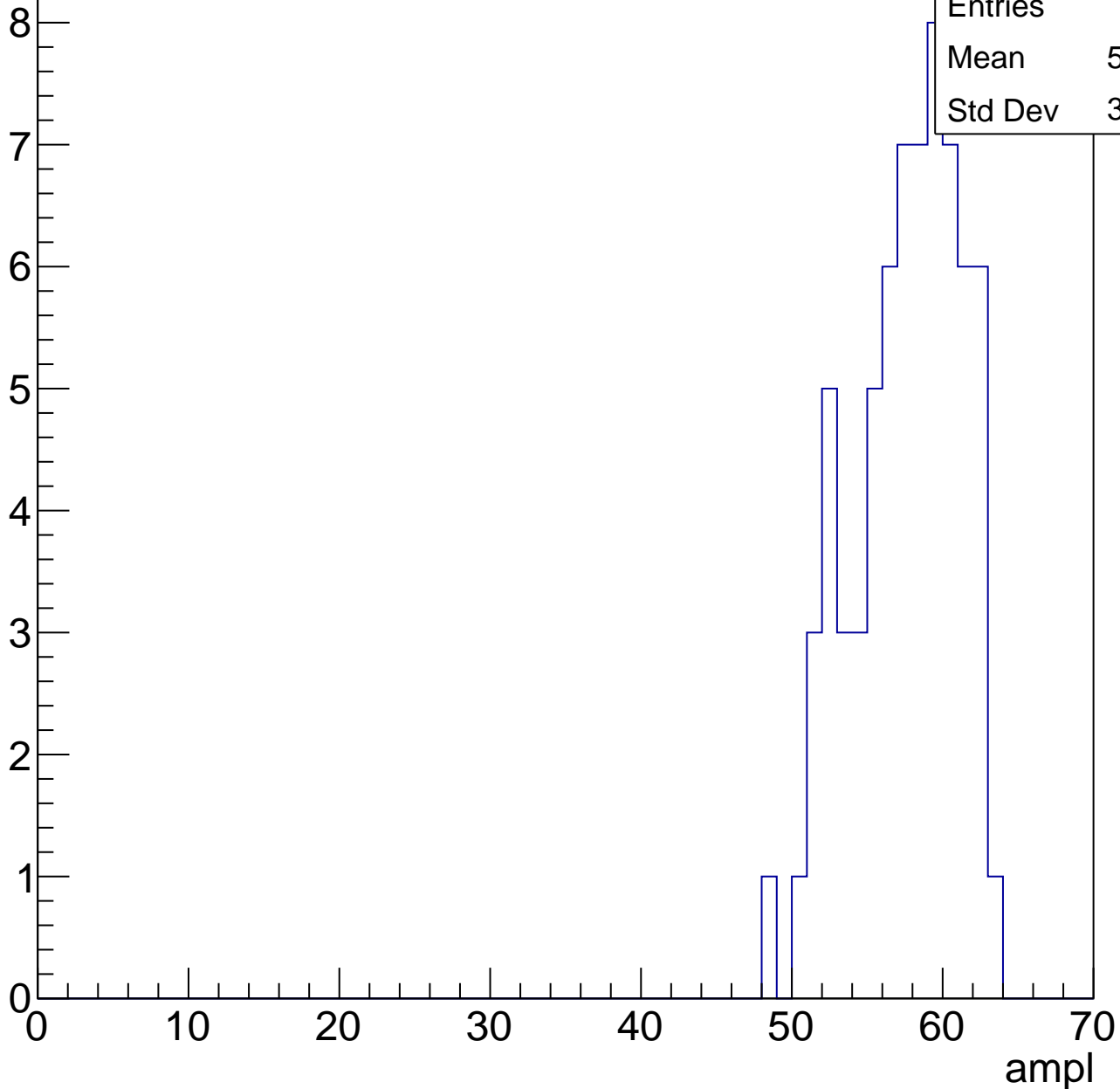


B1L103S, U9-ch100, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	57.12
Std Dev	3.504

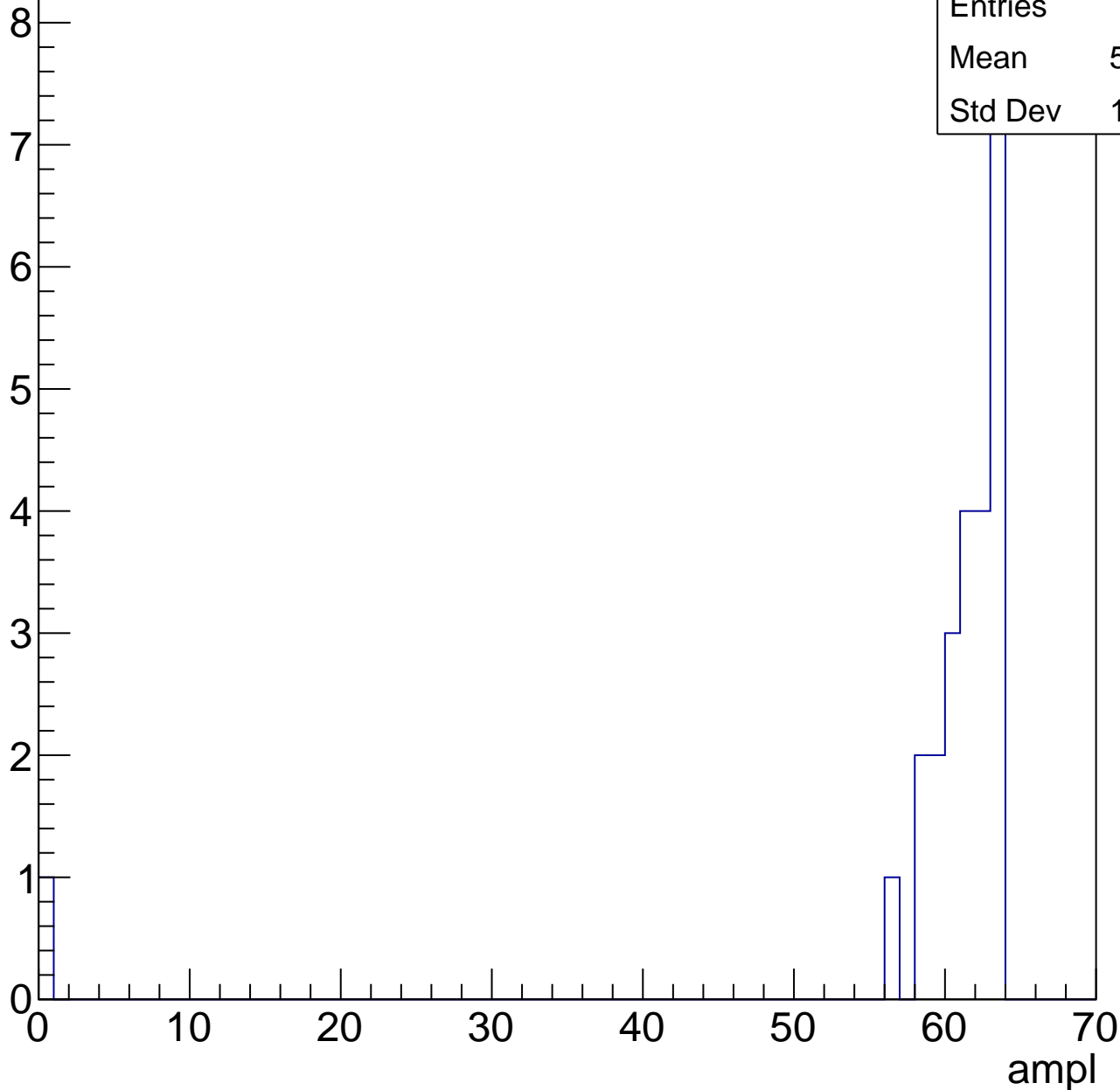


B1L103S, U9-ch100, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	25
Mean	58.64
Std Dev	12.12



B1L103S, U9-ch100, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry



B1L103S, U9-ch101, adc0

calib_packv5_041523_1651.root, FC#0, port C2

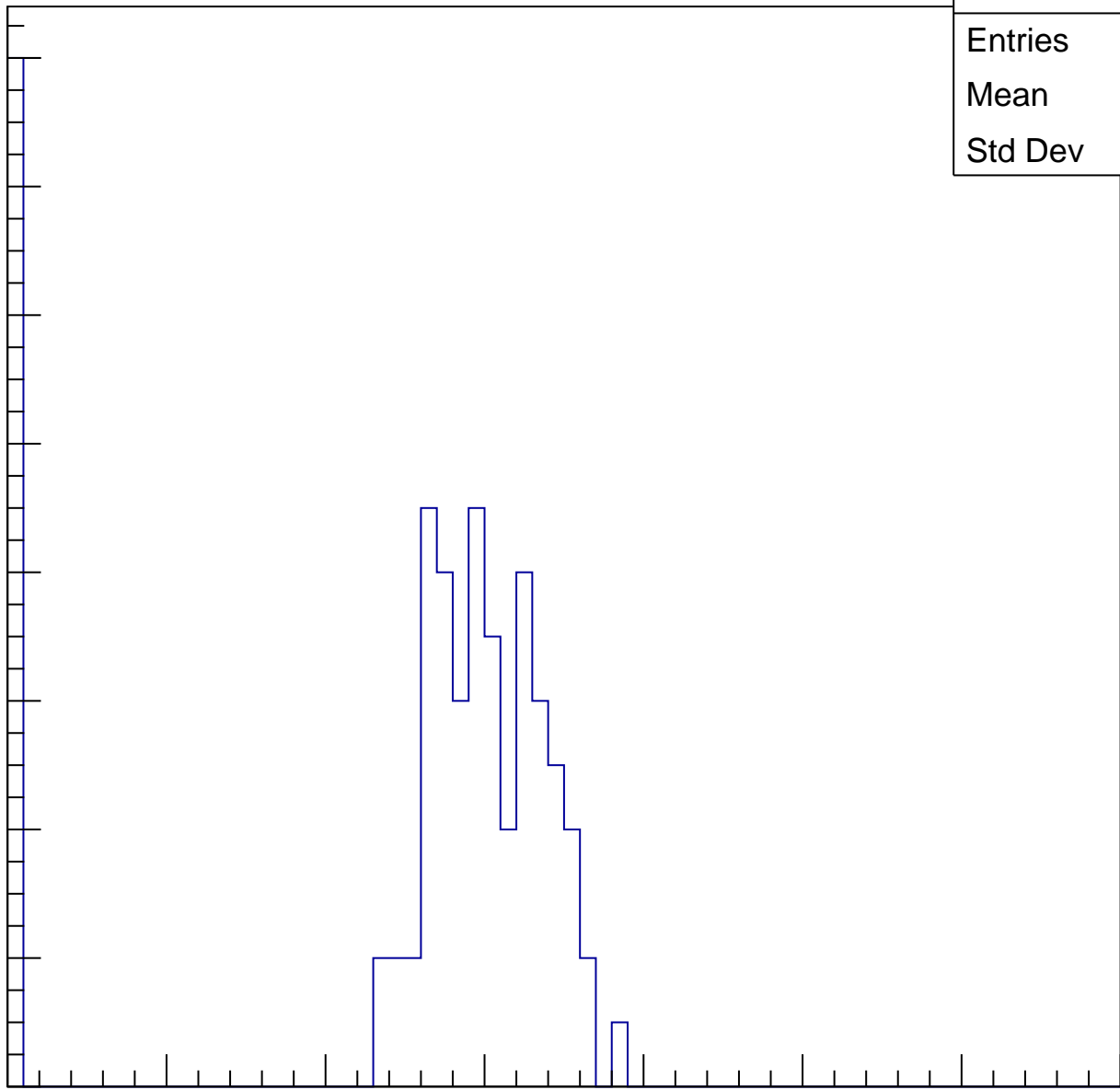
Entries	91
Mean	24.52
Std Dev	11.74

Entry

16
14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

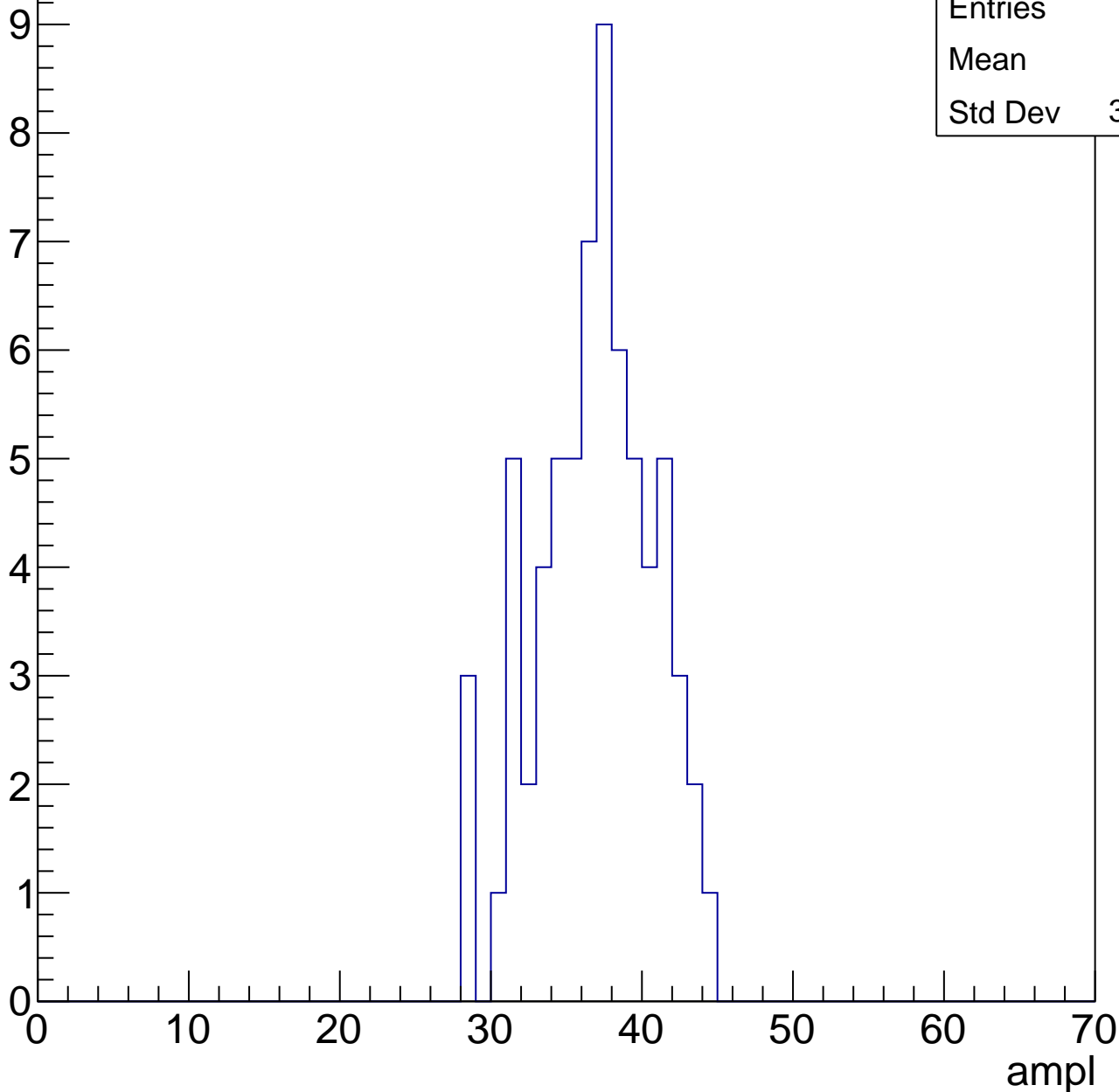


B1L103S, U9-ch101, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	36.4
Std Dev	3.809

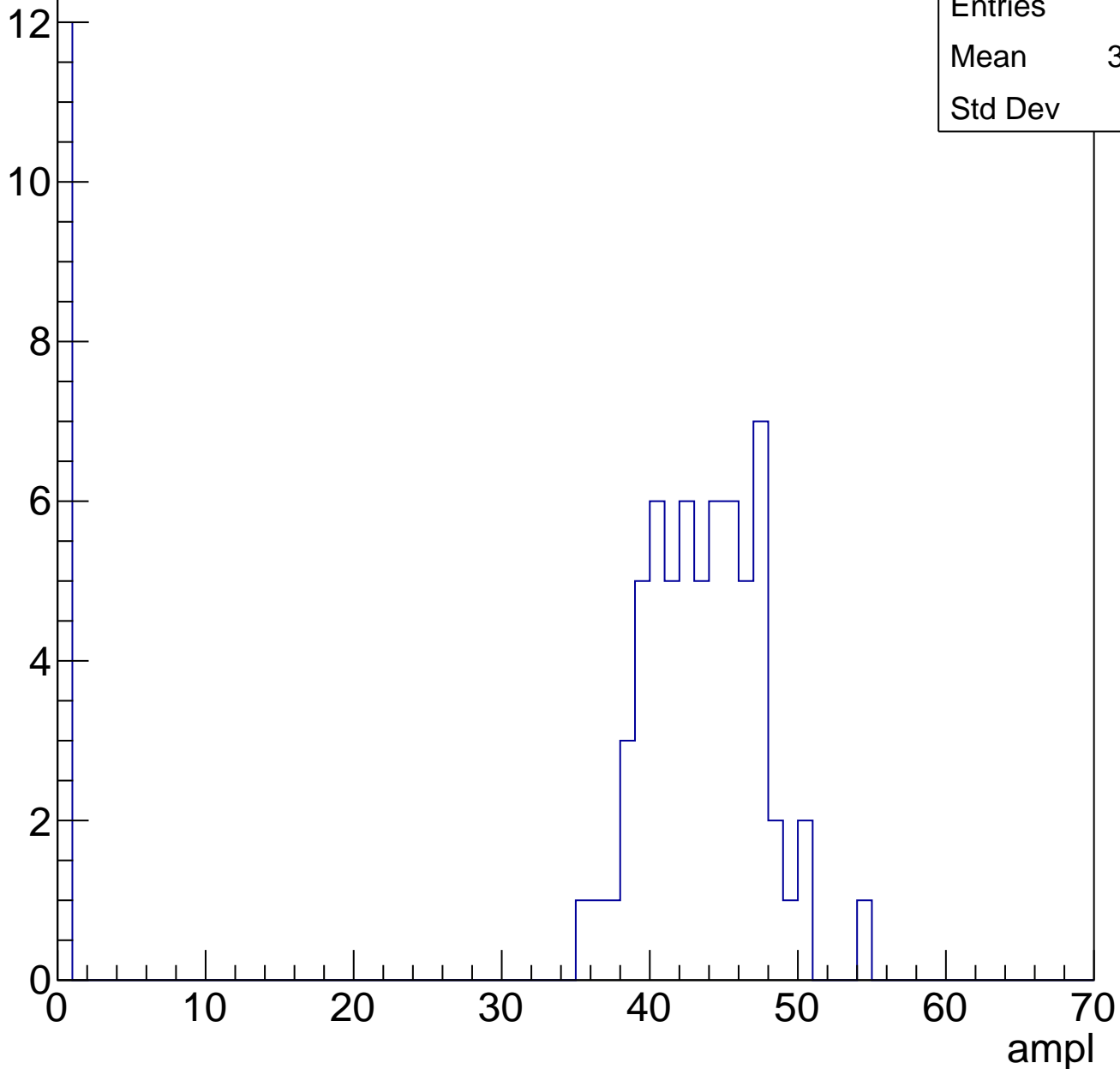


B1L103S, U9-ch101, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	36.28
Std Dev	16.2

Entry

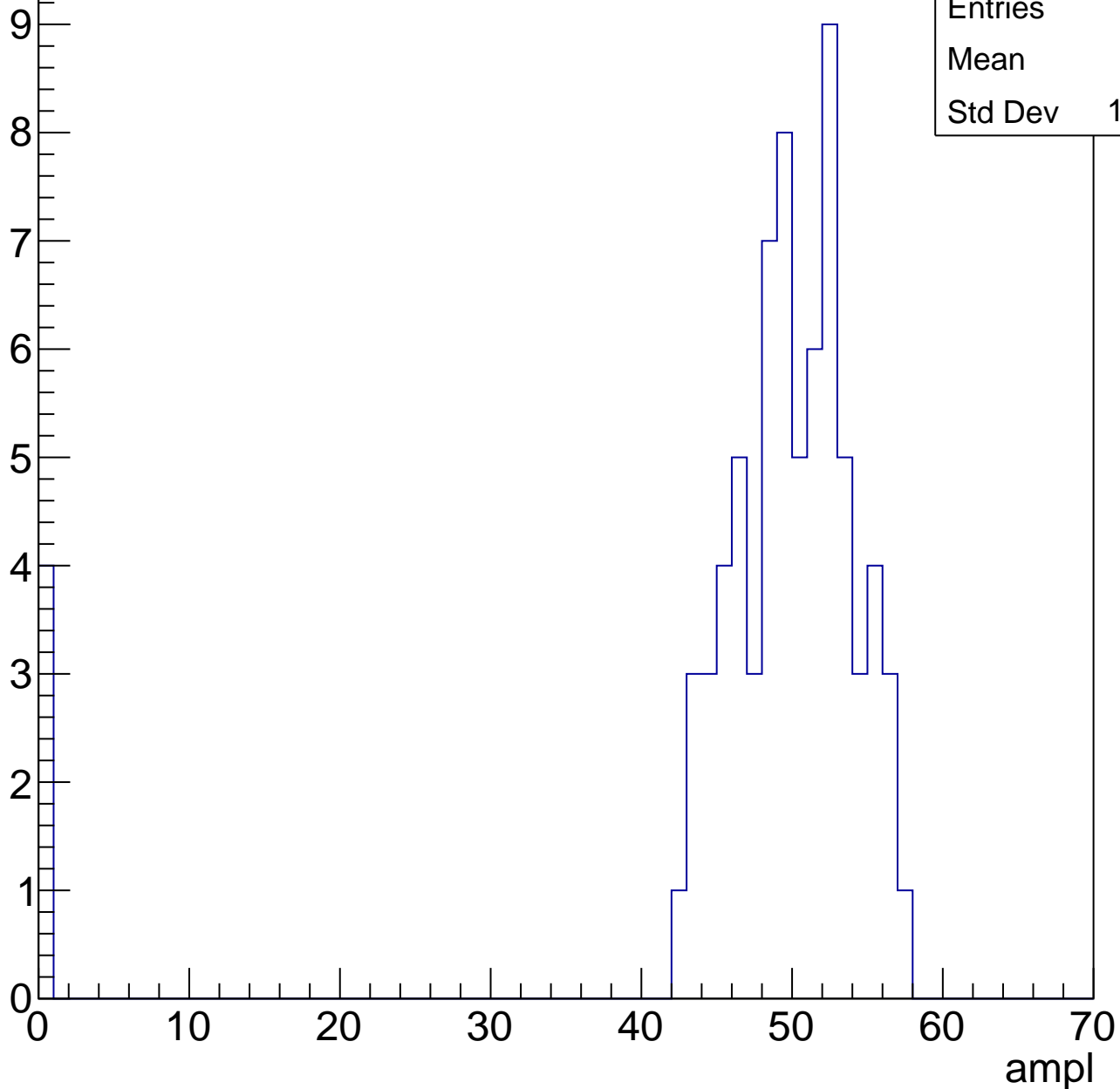


B1L103S, U9-ch101, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

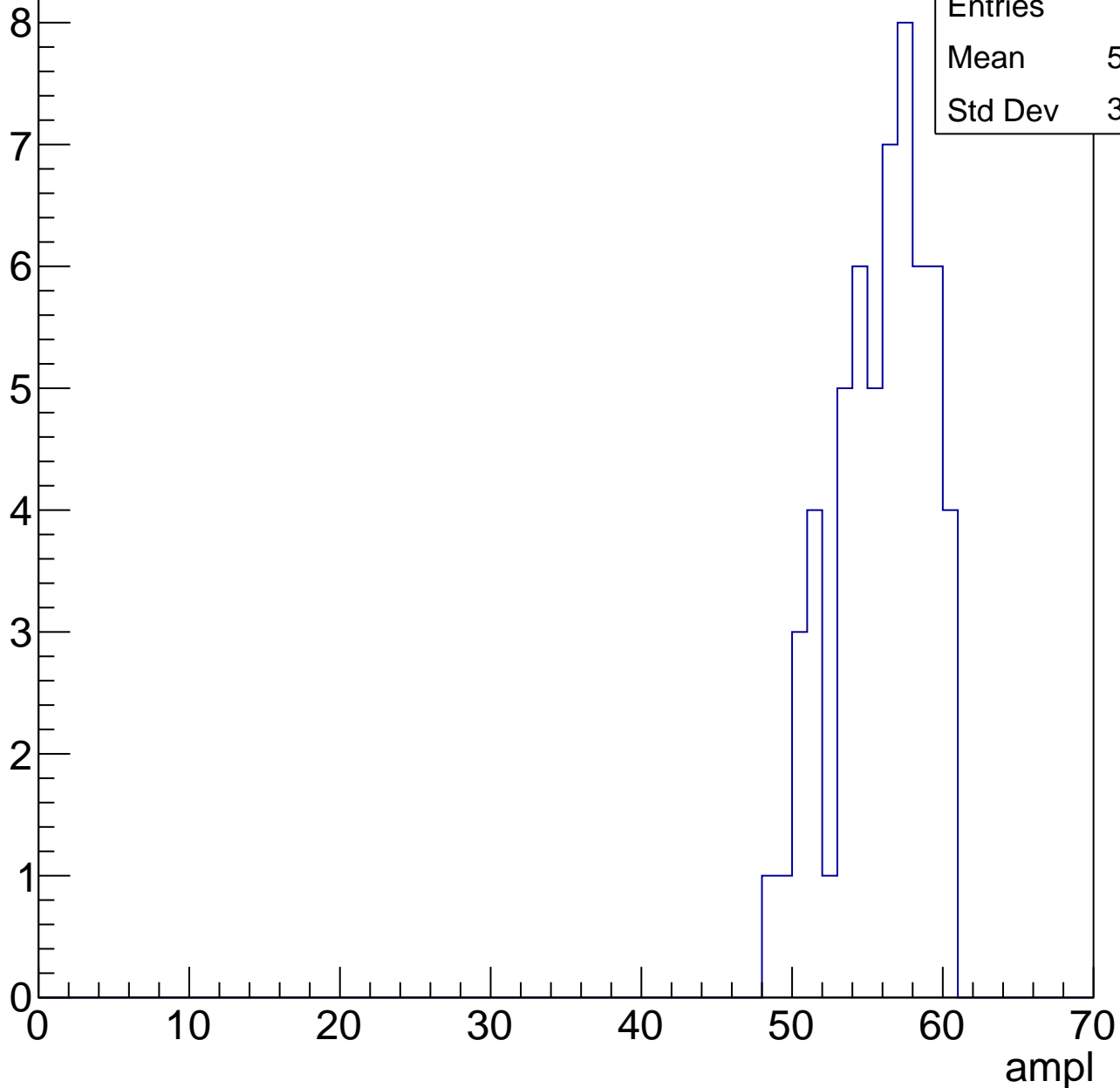
Entries	74
Mean	47
Std Dev	11.79



B1L103S, U9-ch101, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



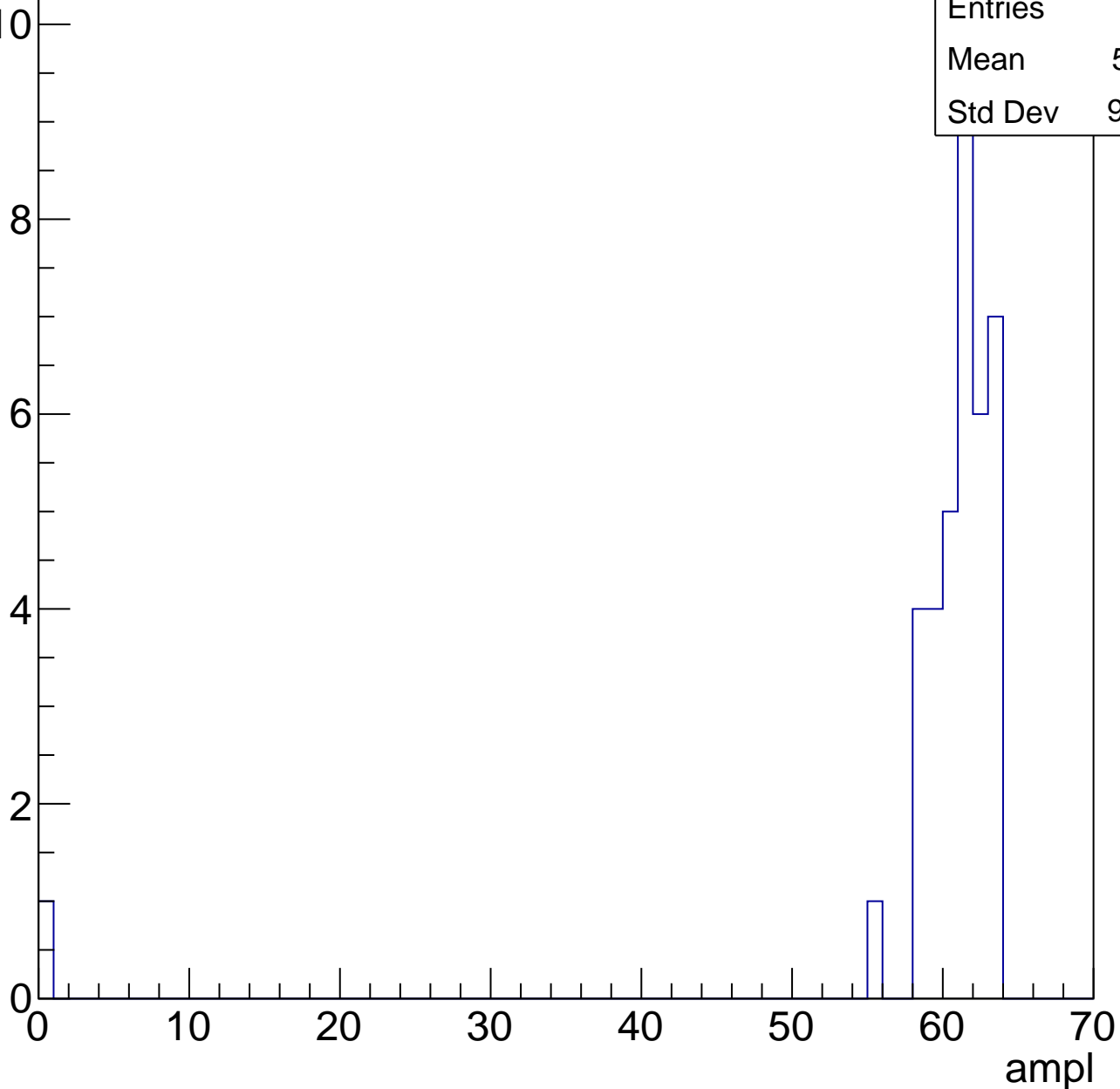
Entries	57
Mean	55.39
Std Dev	3.077

B1L103S, U9-ch101, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

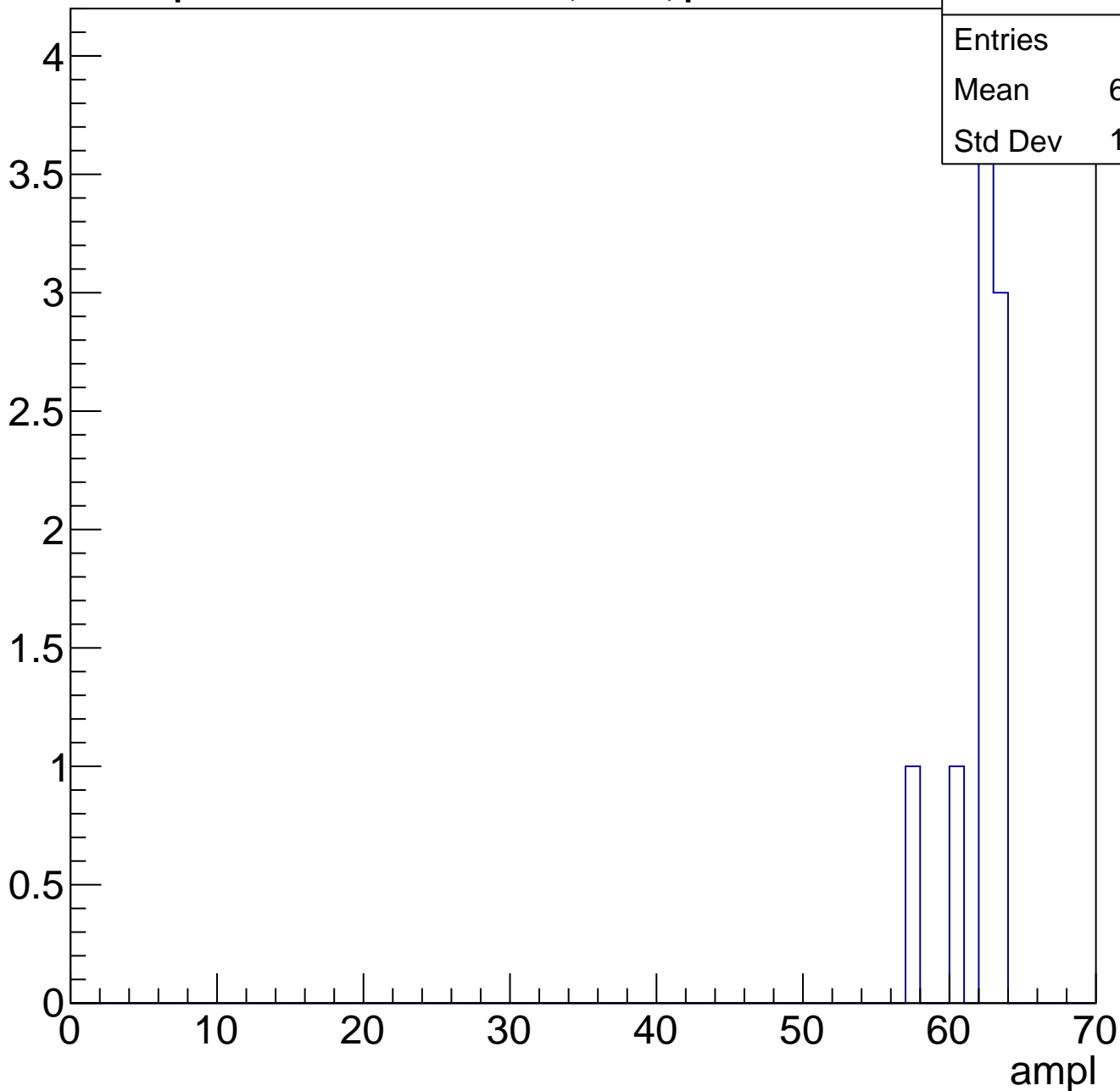
Entries	38
Mean	59.11
Std Dev	9.883



B1L103S, U9-ch101, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch101, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



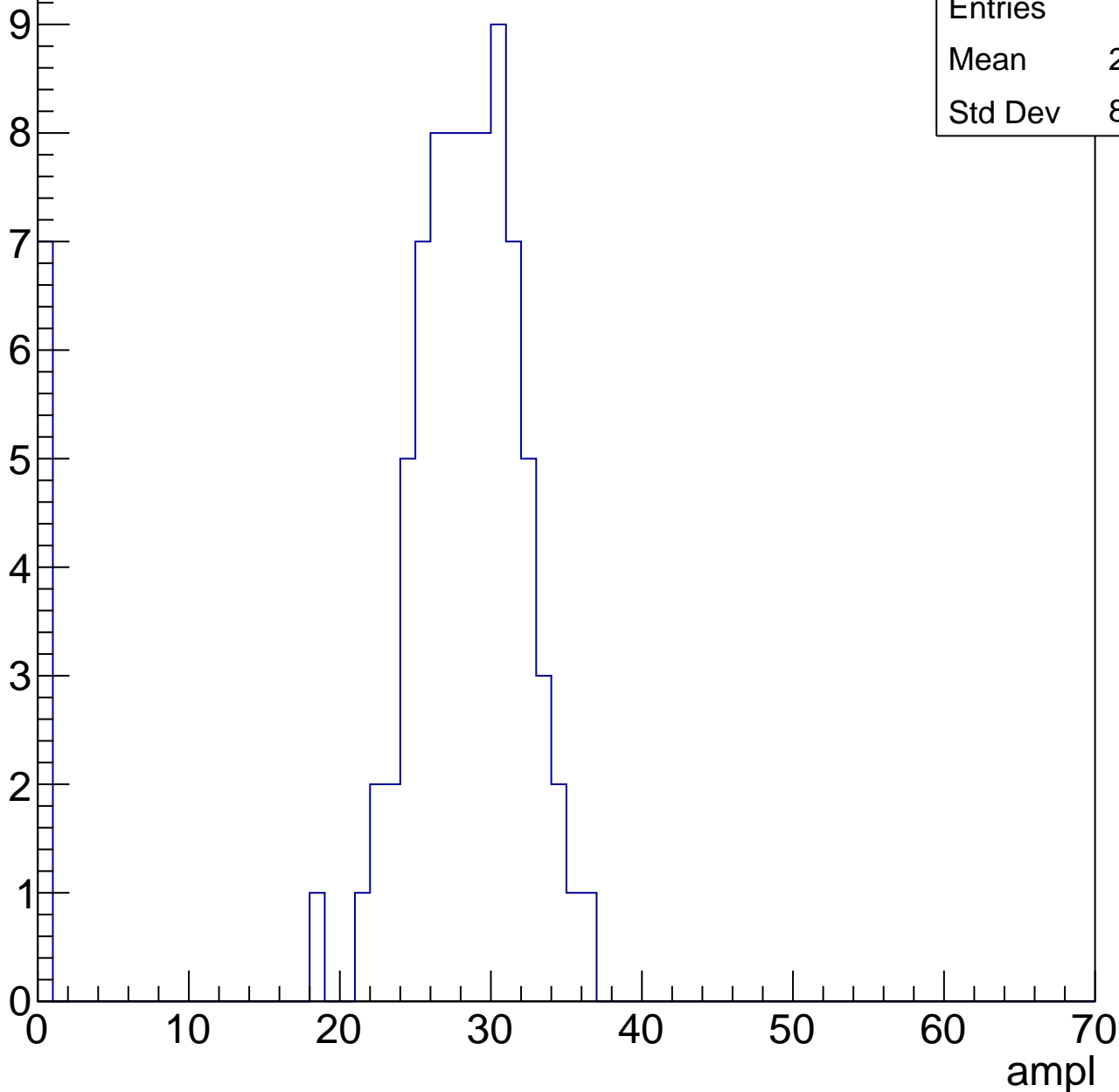
Entries	19
Mean	0
Std Dev	0

B1L103S, U9-ch102, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	85
Mean	25.75
Std Dev	8.373

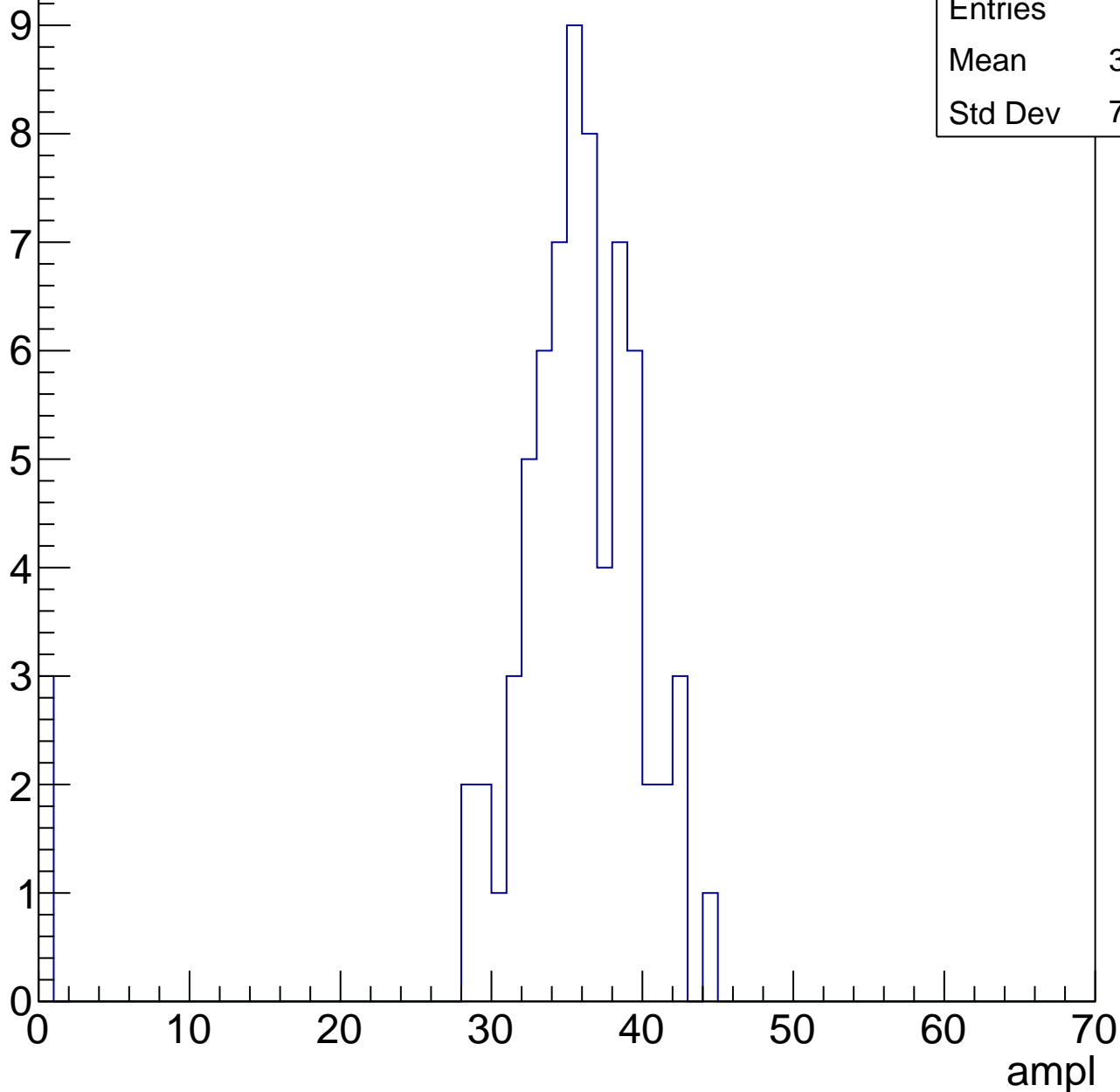


B1L103S, U9-ch102, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	34.03
Std Dev	7.926

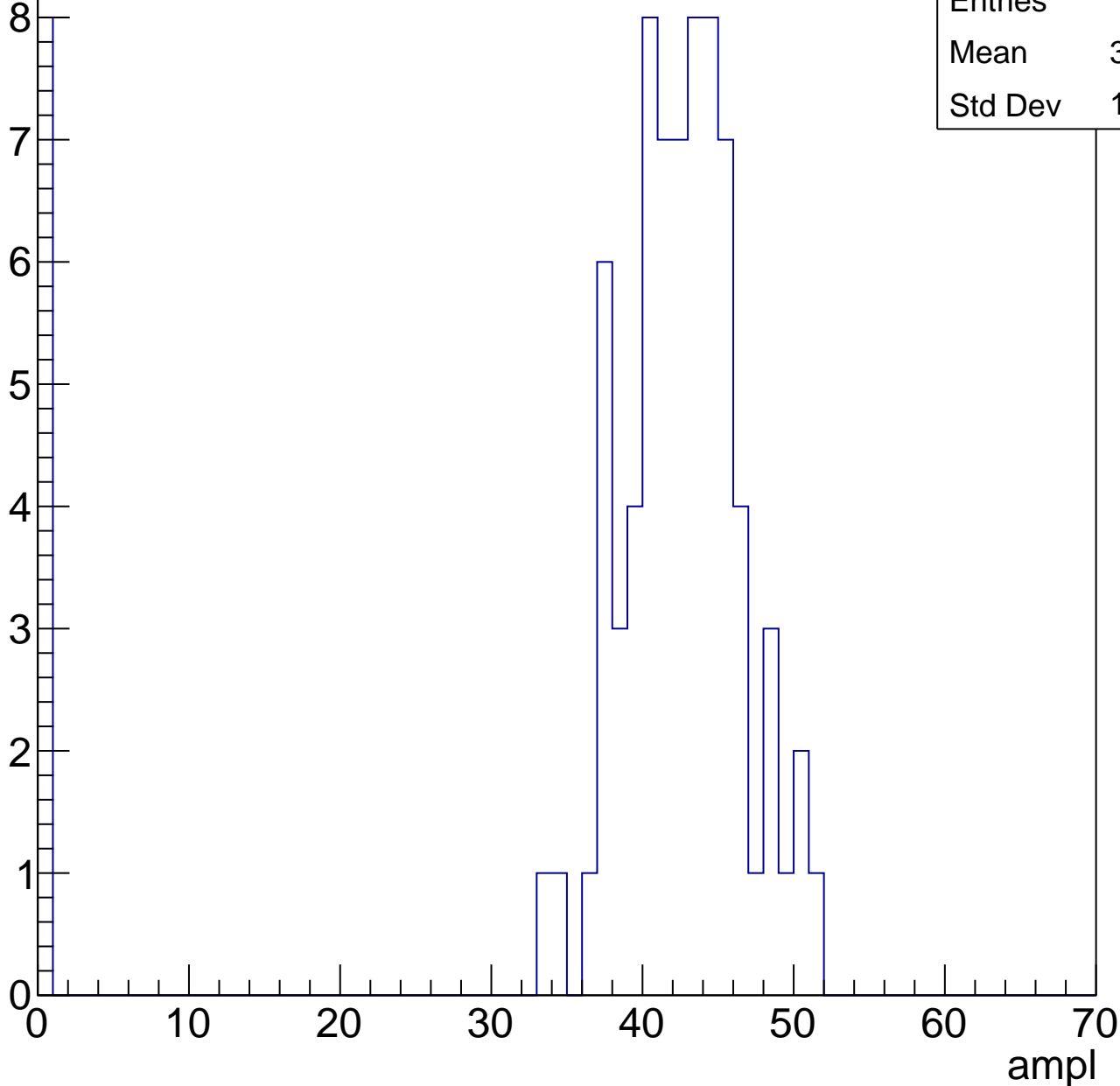


B1L103S, U9-ch102, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	81
Mean	38.05
Std Dev	13.08

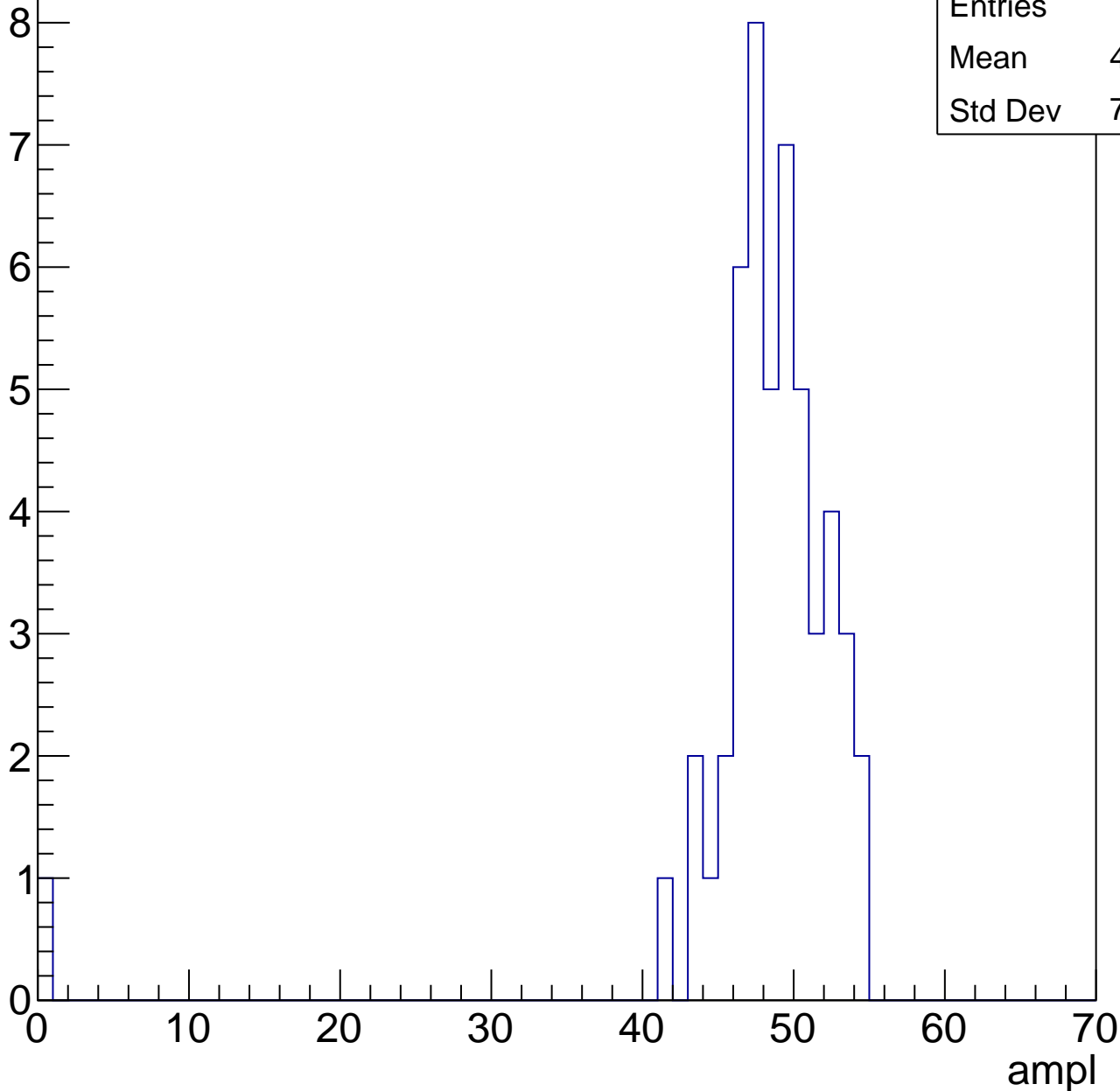


B1L103S, U9-ch102, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	47.48
Std Dev	7.376

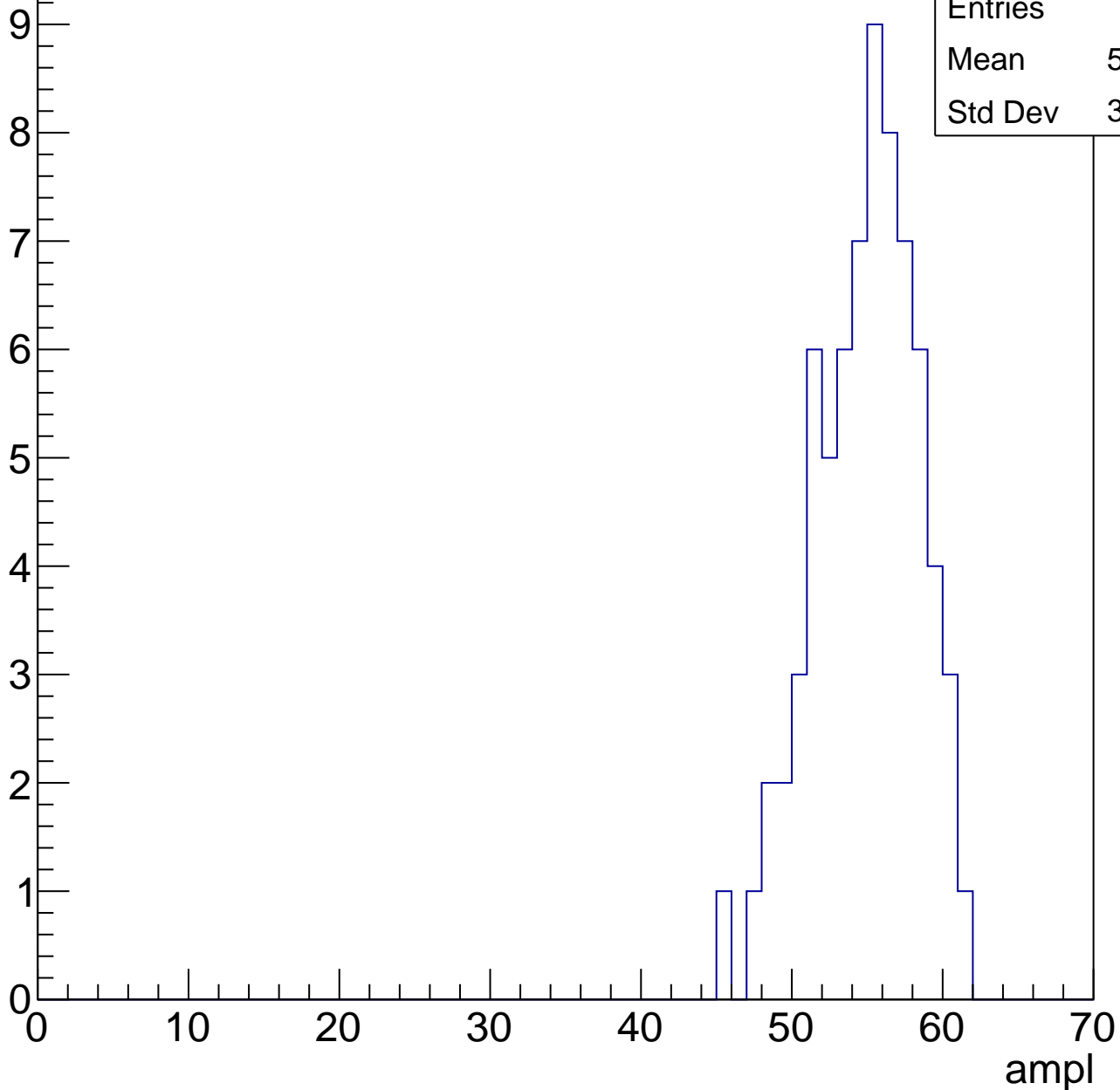


B1L103S, U9-ch102, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	54.44
Std Dev	3.406

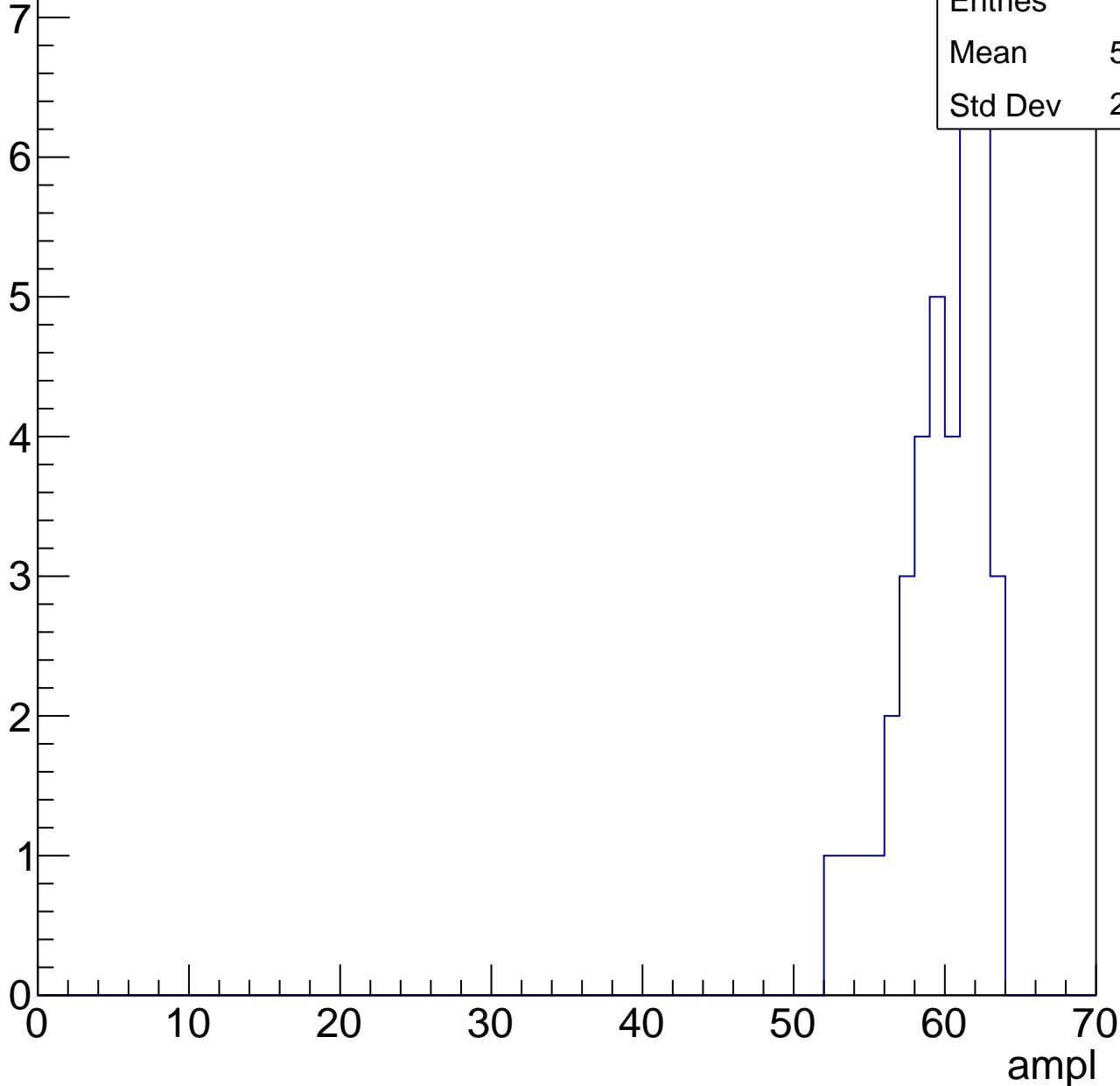


B1L103S, U9-ch102, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	59.33
Std Dev	2.767

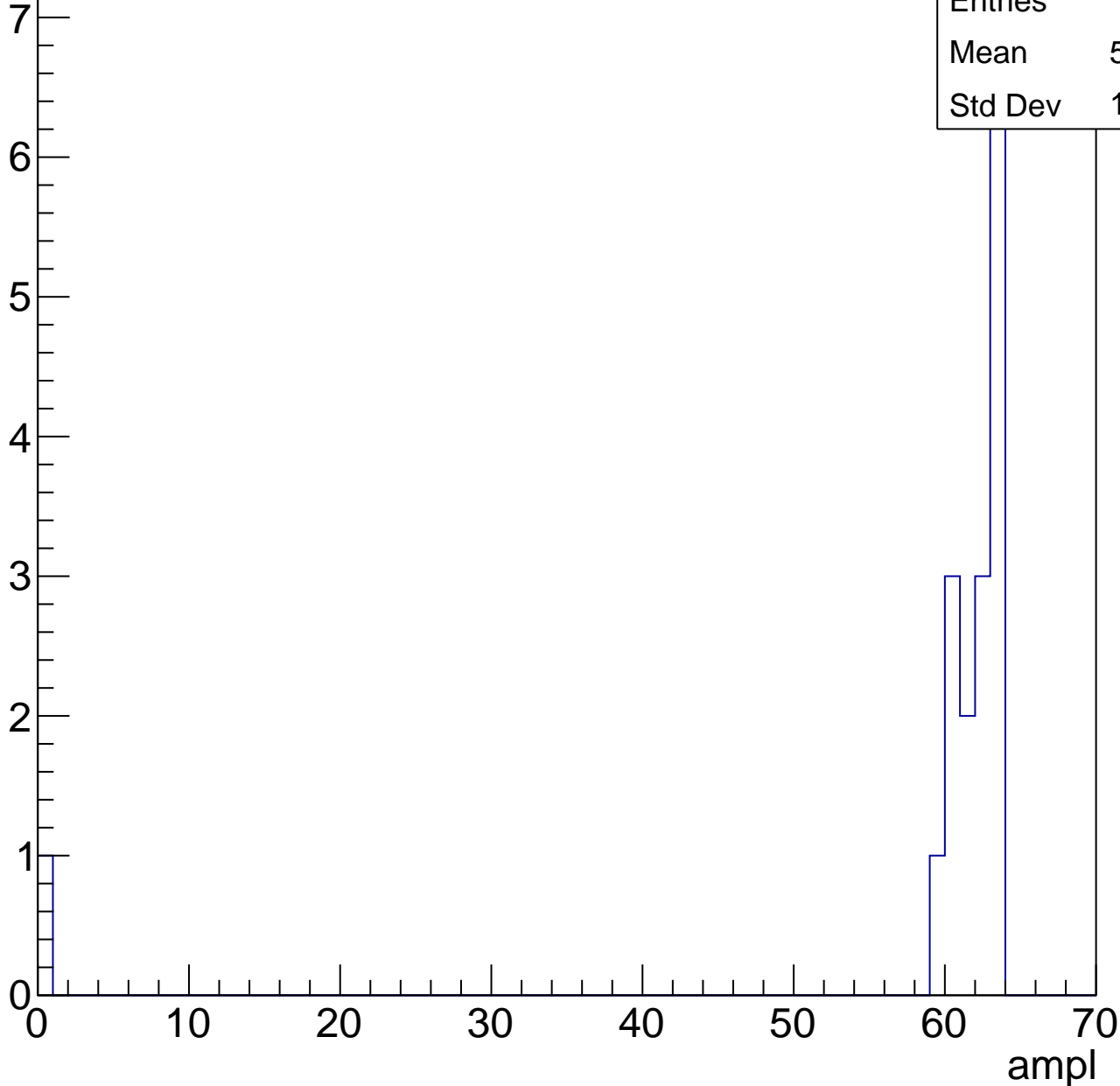


B1L103S, U9-ch102, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	17
Mean	58.12
Std Dev	14.59



B1L103S, U9-ch102, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	0
Std Dev	0



B1L103S, U9-ch103, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	77
Mean	23.49
Std Dev	12.49

Entry

16
14
12
10
8
6
4
2
0

0

10

20

30

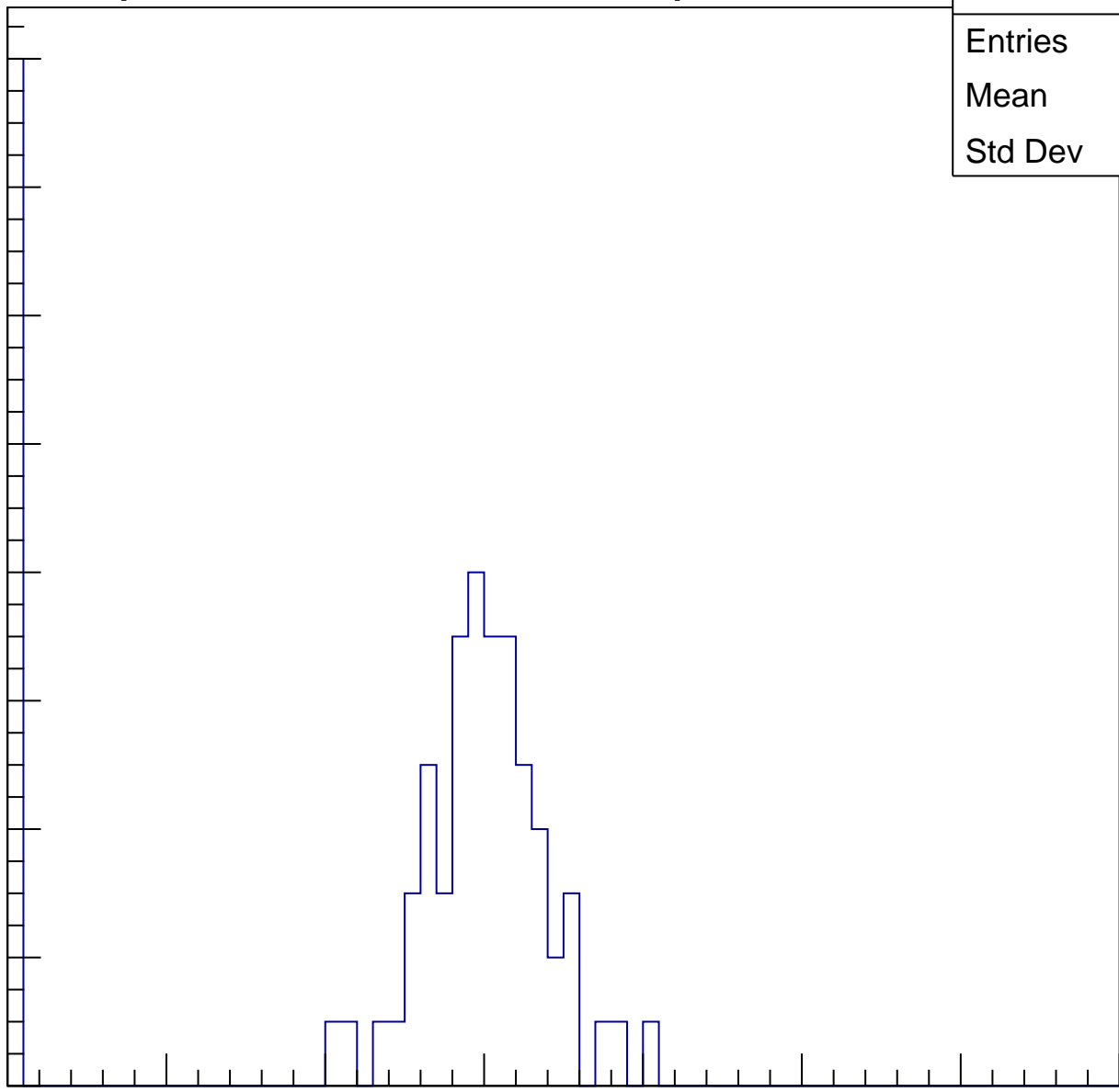
40

50

60

70

ampl

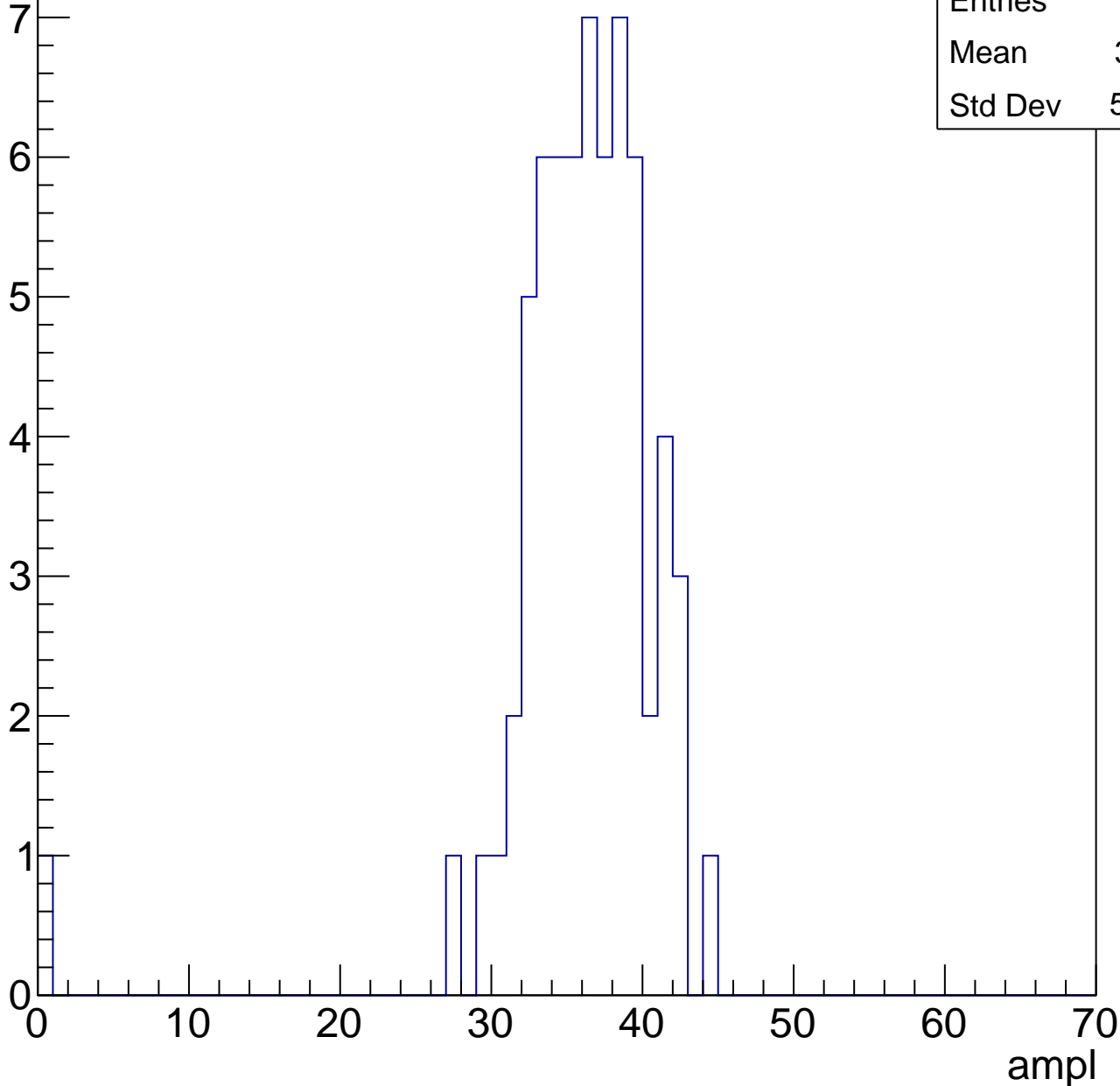


B1L103S, U9-ch103, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	35.51
Std Dev	5.619

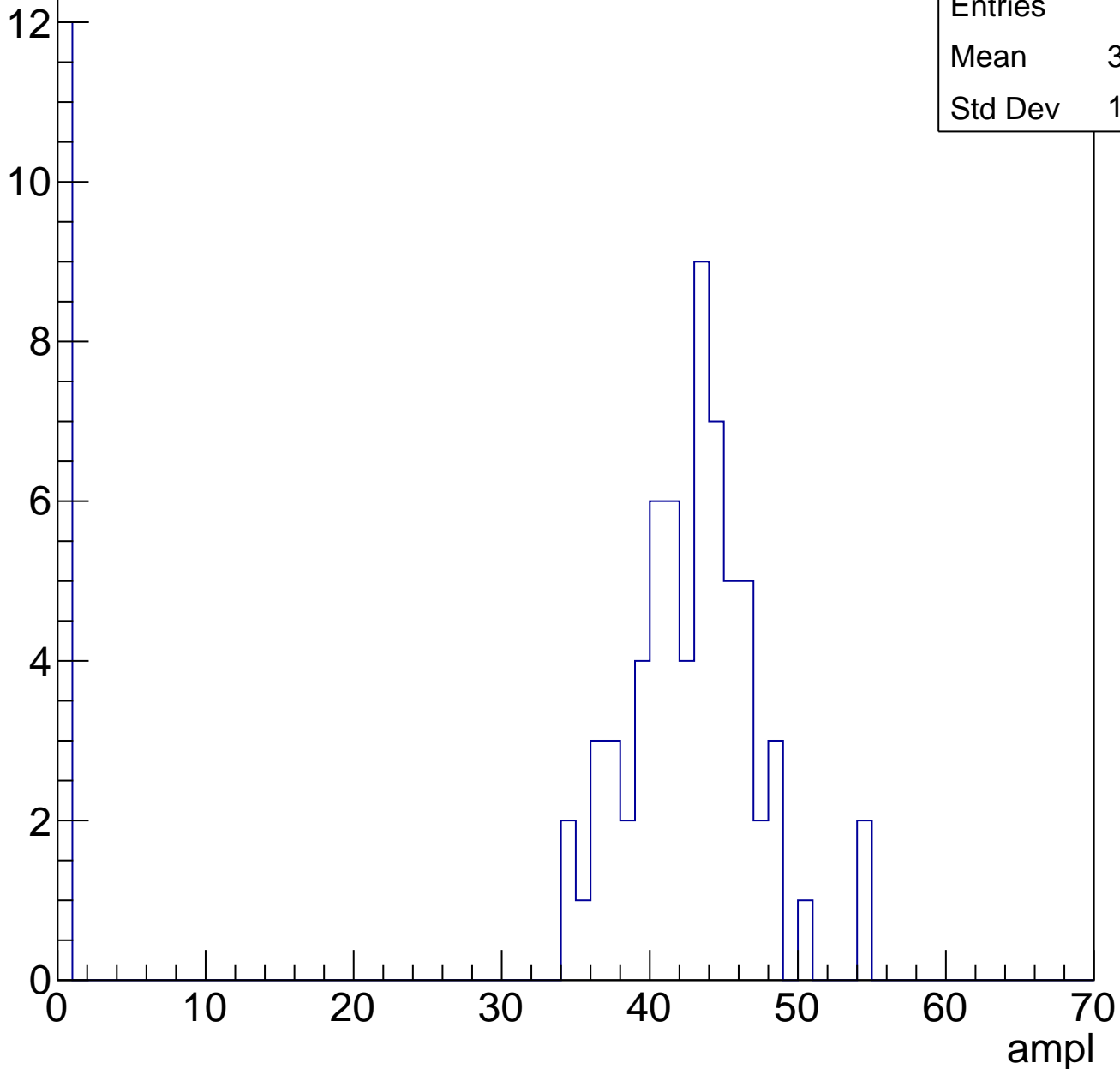


B1L103S, U9-ch103, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	77
Mean	35.77
Std Dev	15.83

Entry

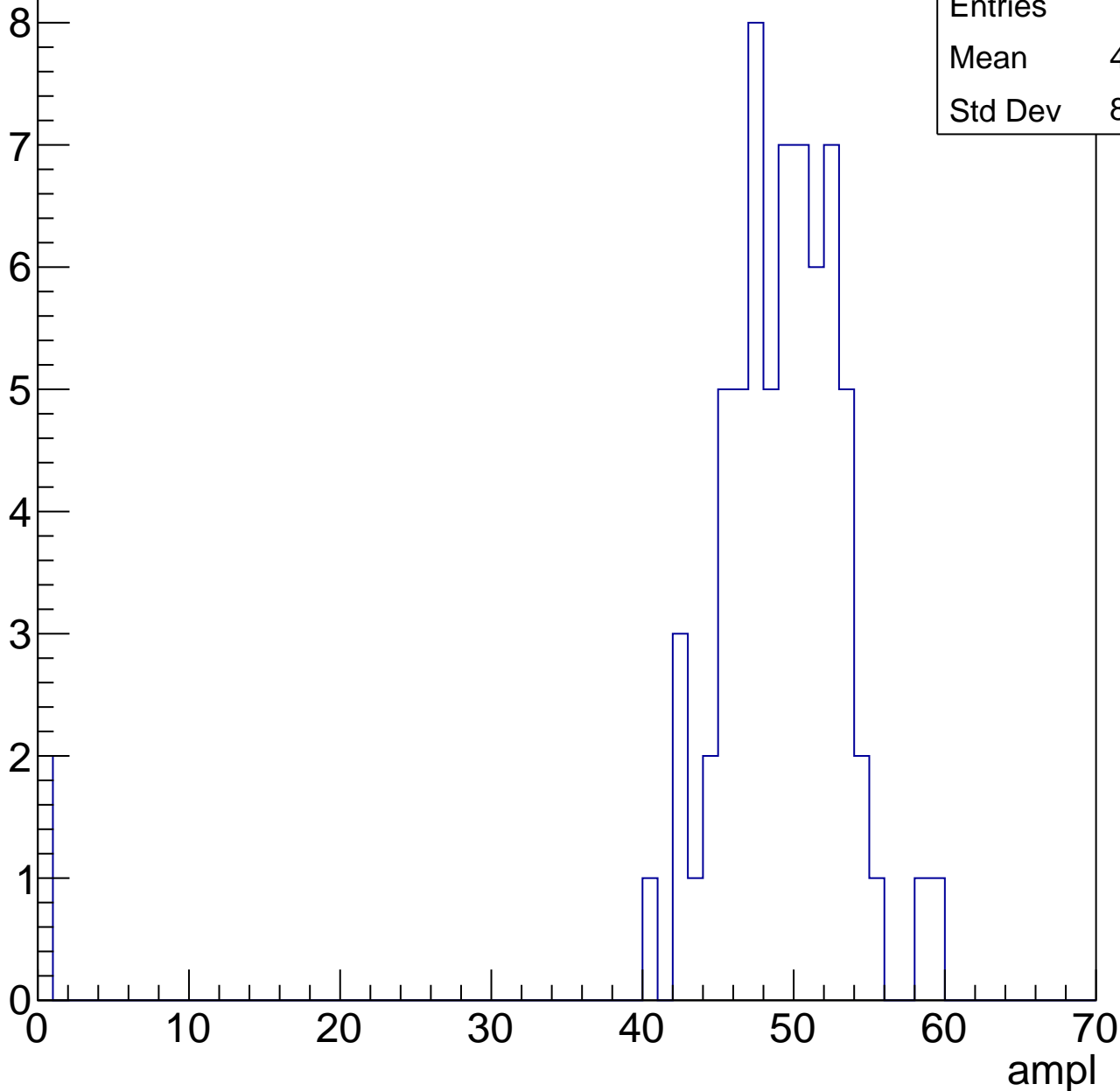


B1L103S, U9-ch103, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

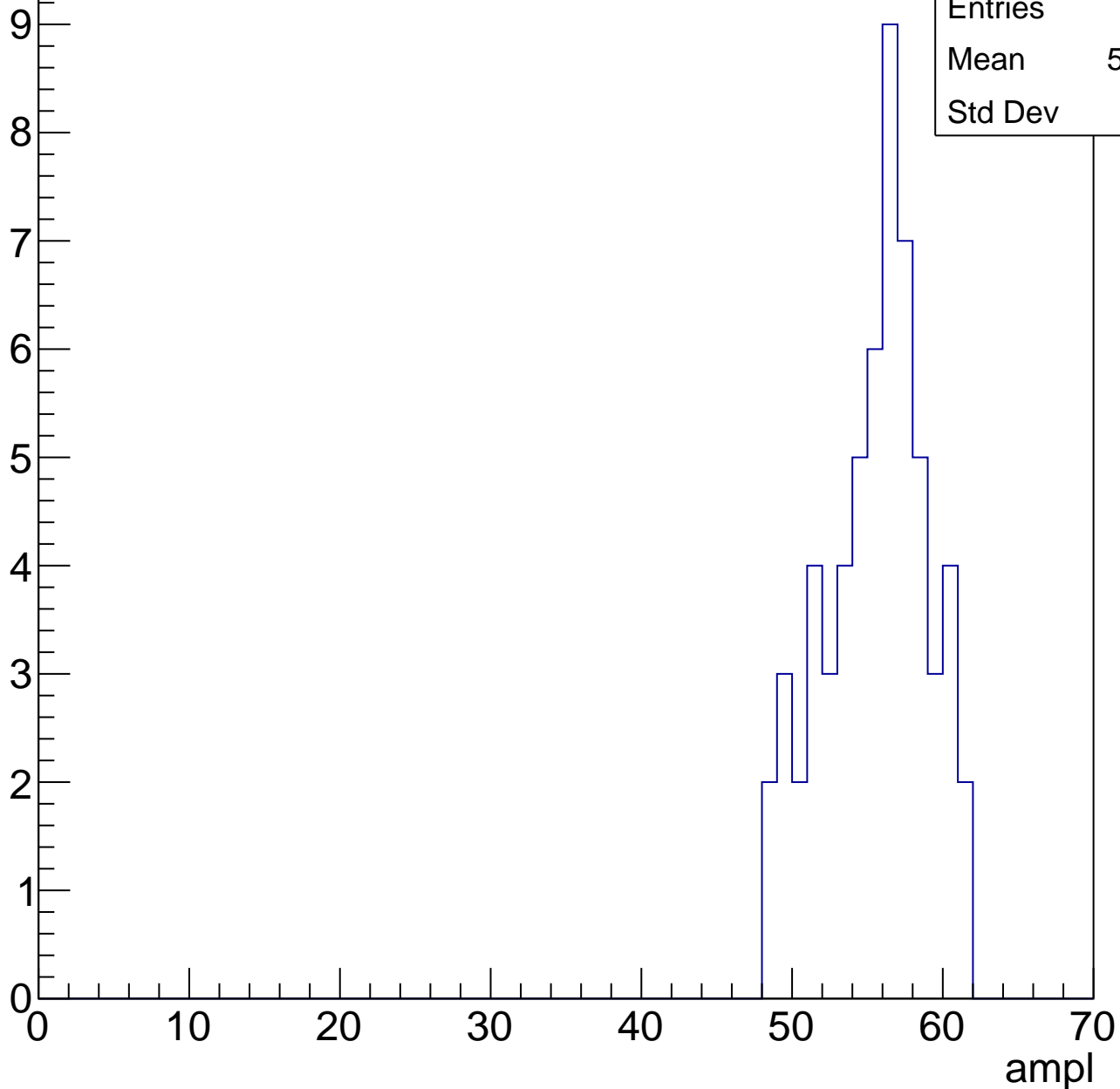
Entries	69
Mean	47.48
Std Dev	8.976



B1L103S, U9-ch103, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

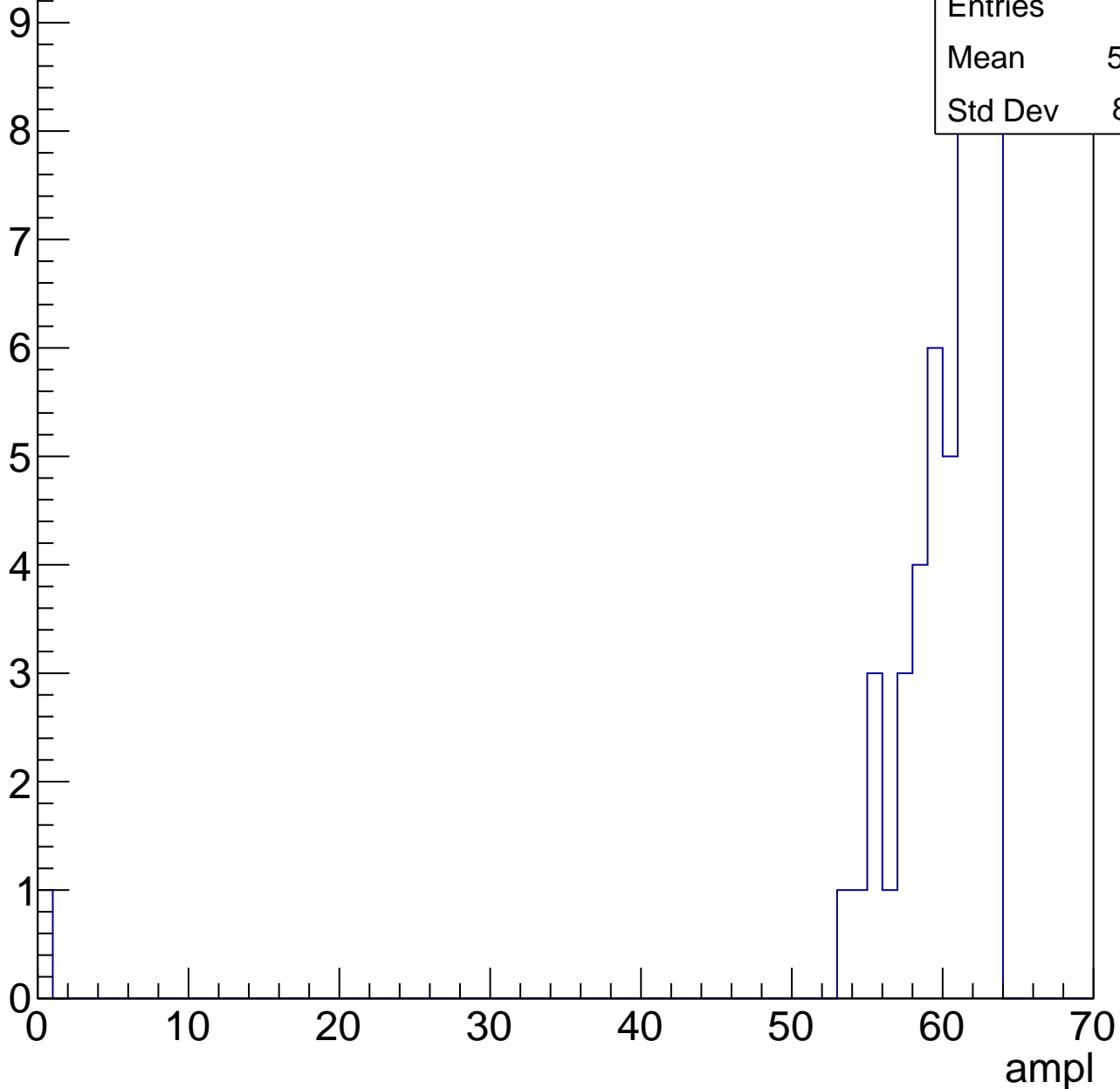


B1L103S, U9-ch103, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

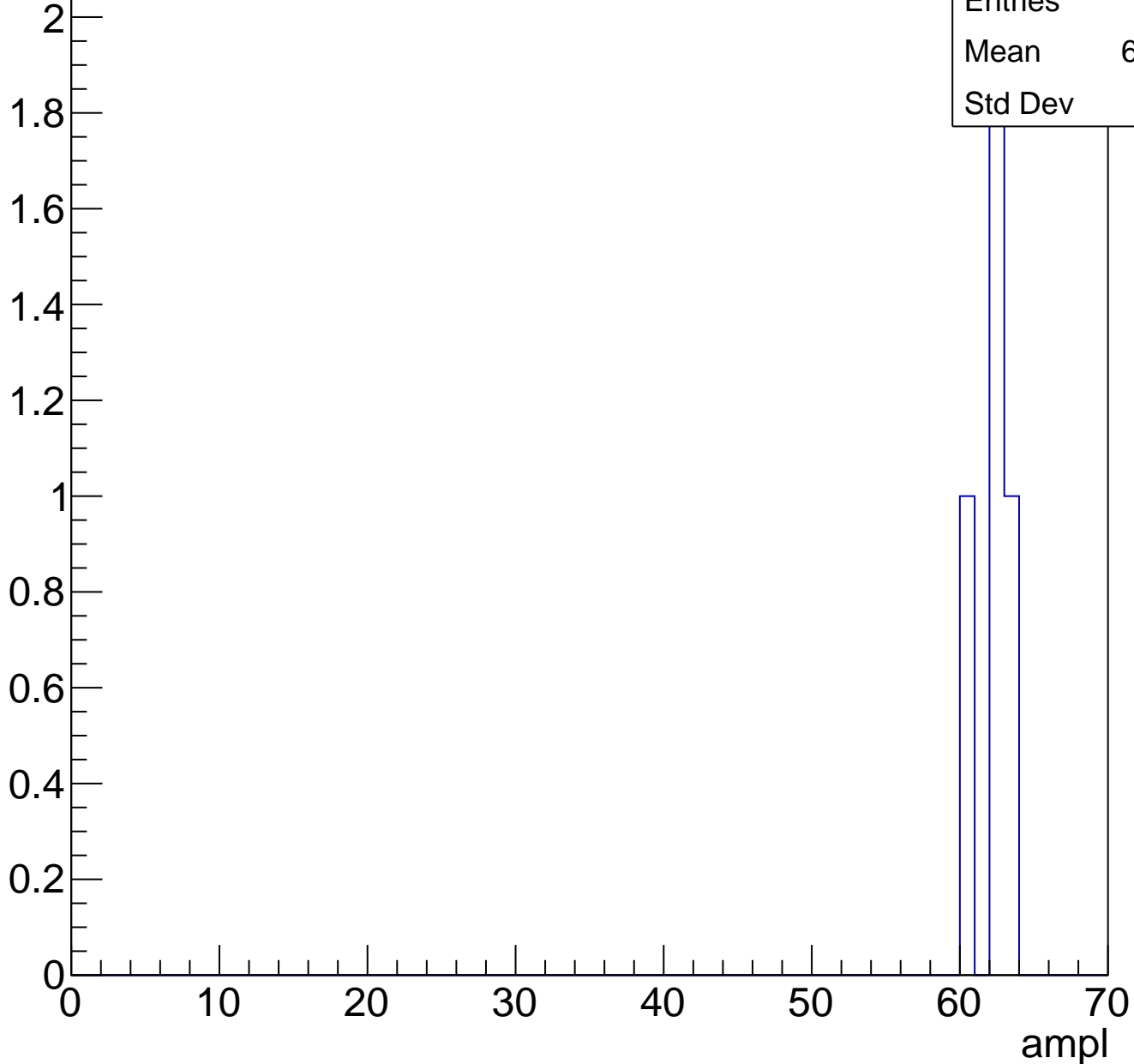
Entries	50
Mean	58.72
Std Dev	8.791



B1L103S, U9-ch103, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

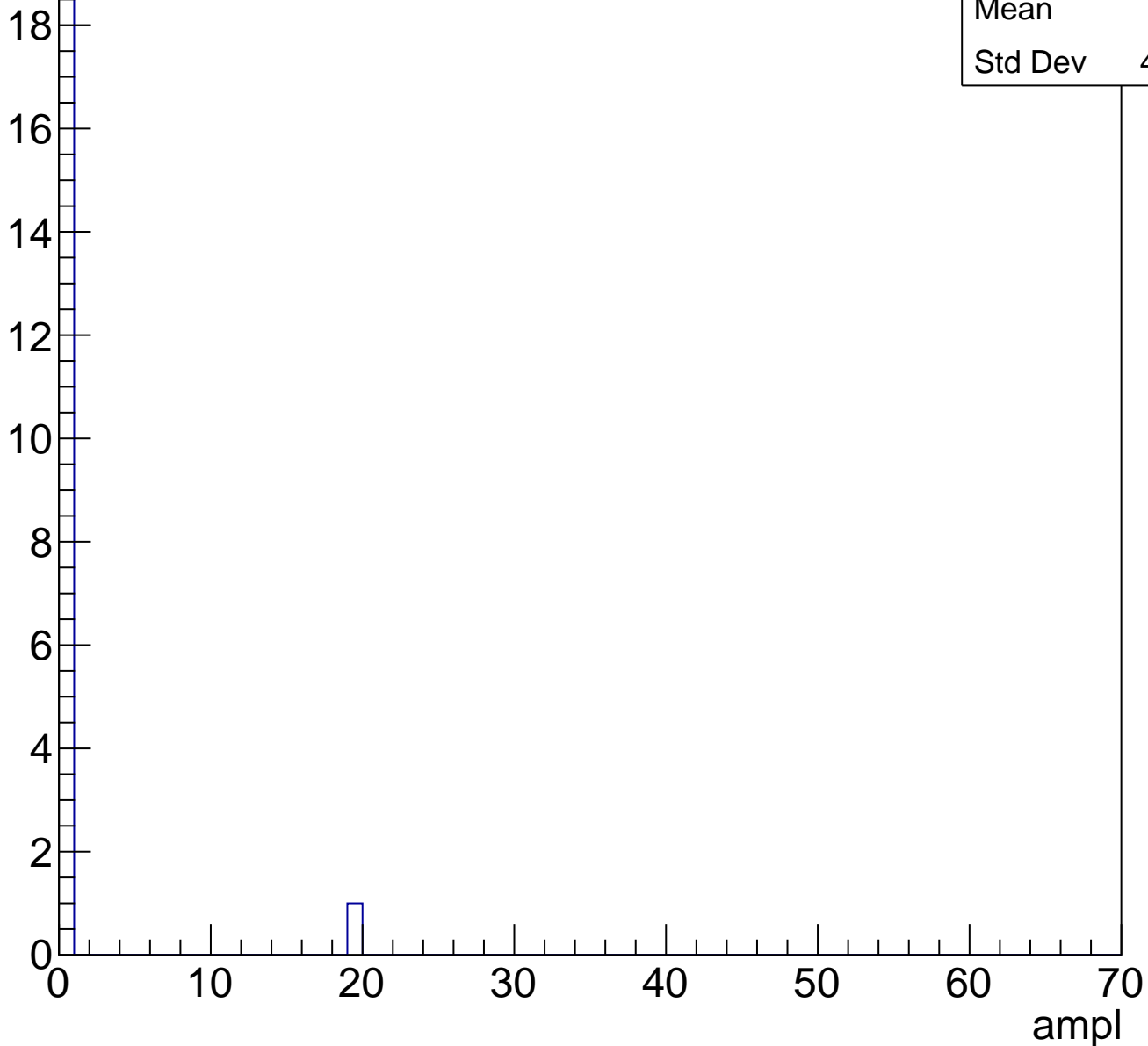


B1L103S, U9-ch103, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	0.95
Std Dev	4.141

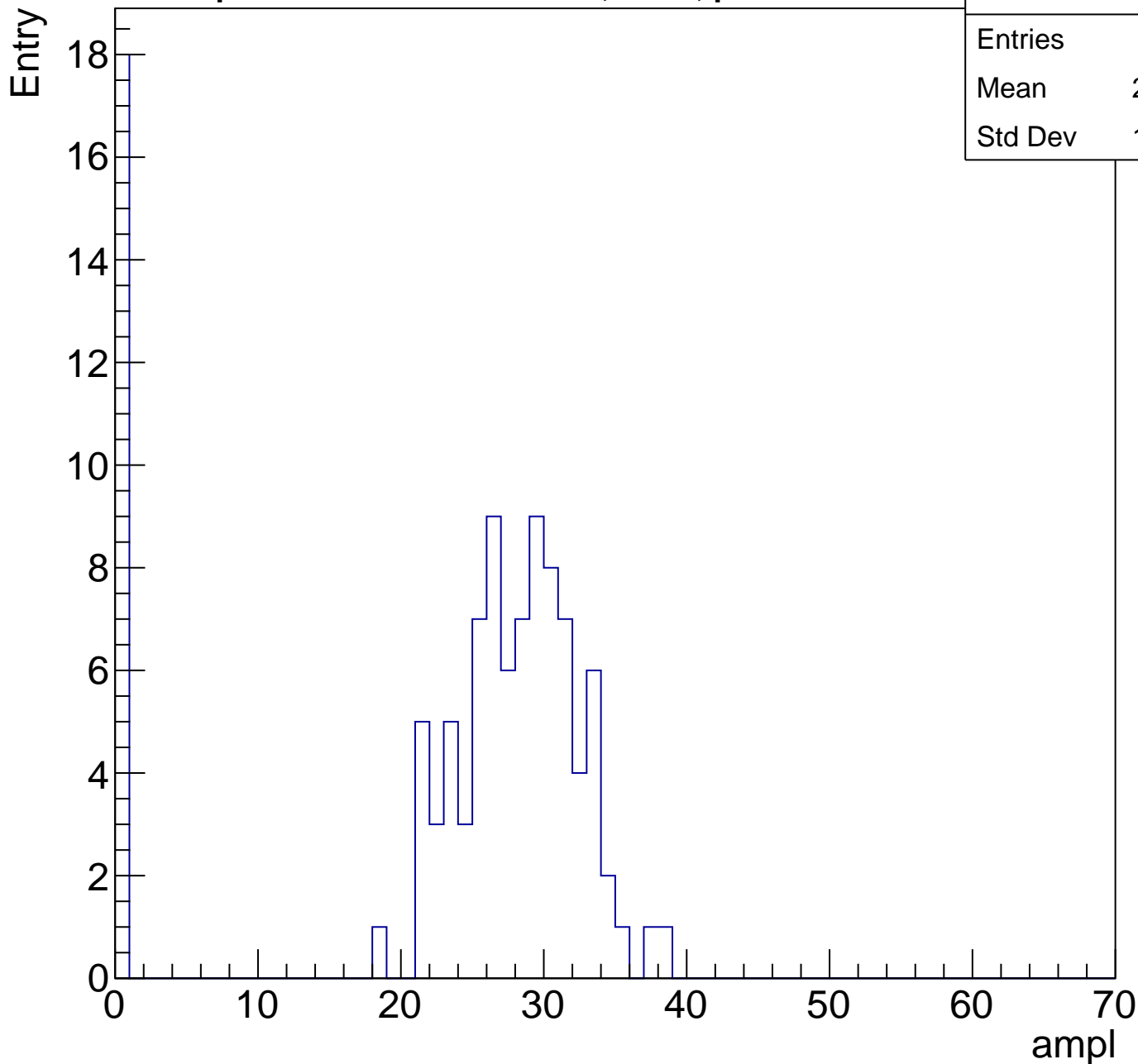
Entry



B1L103S, U9-ch104, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	103
Mean	22.96
Std Dev	11.17

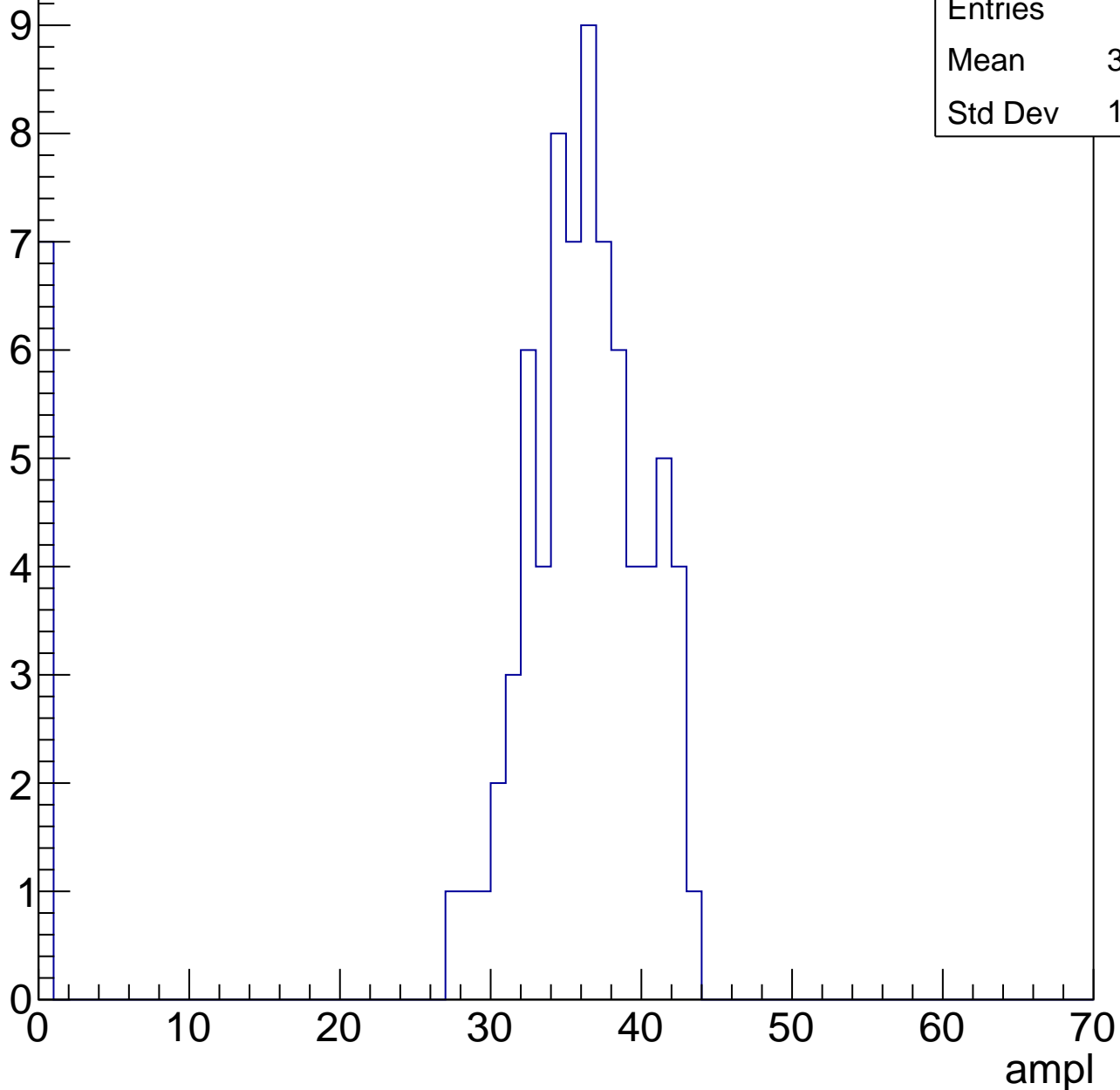


B1L103S, U9-ch104, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	80
Mean	32.76
Std Dev	10.72

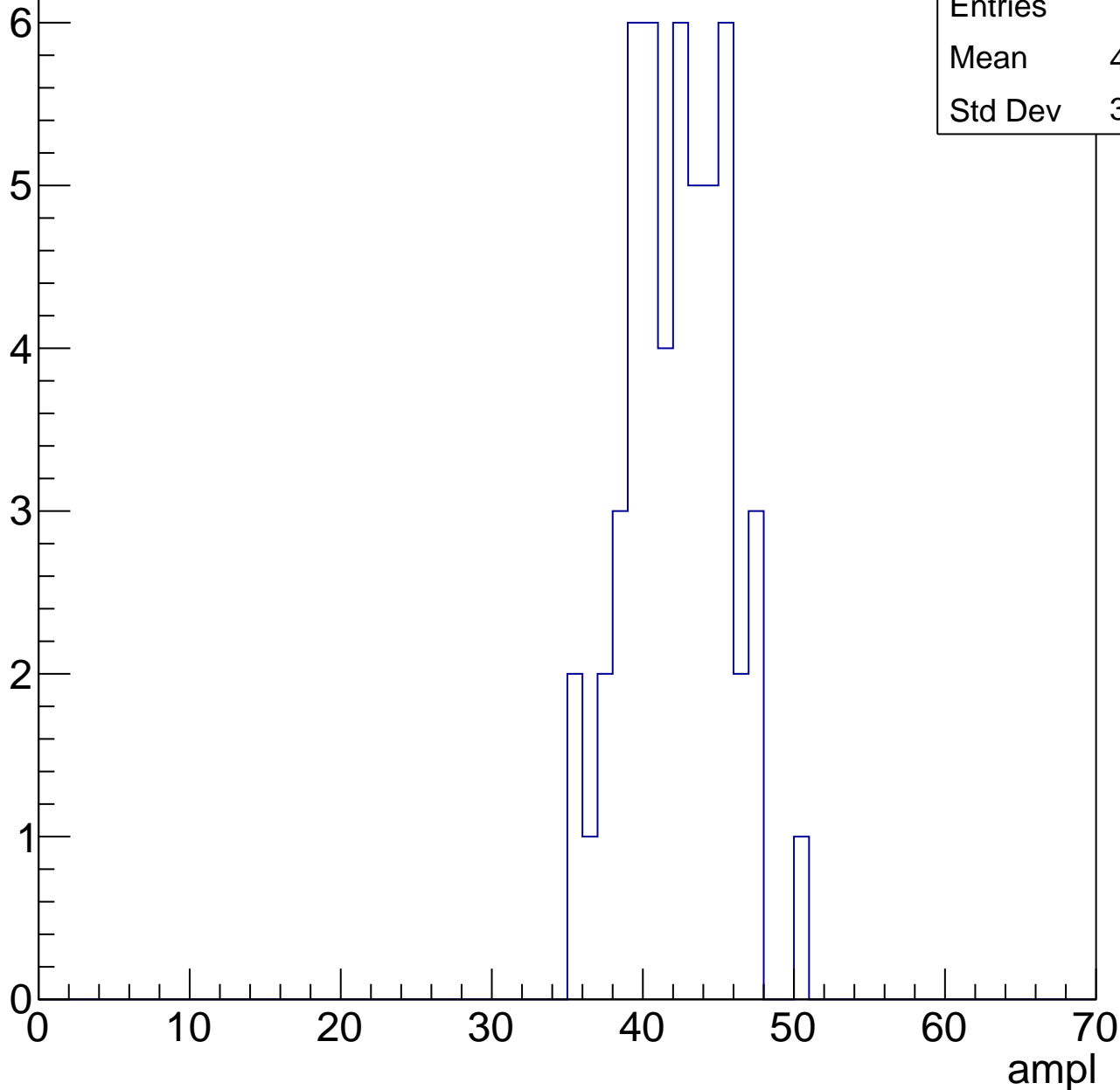


B1L103S, U9-ch104, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	41.77
Std Dev	3.285

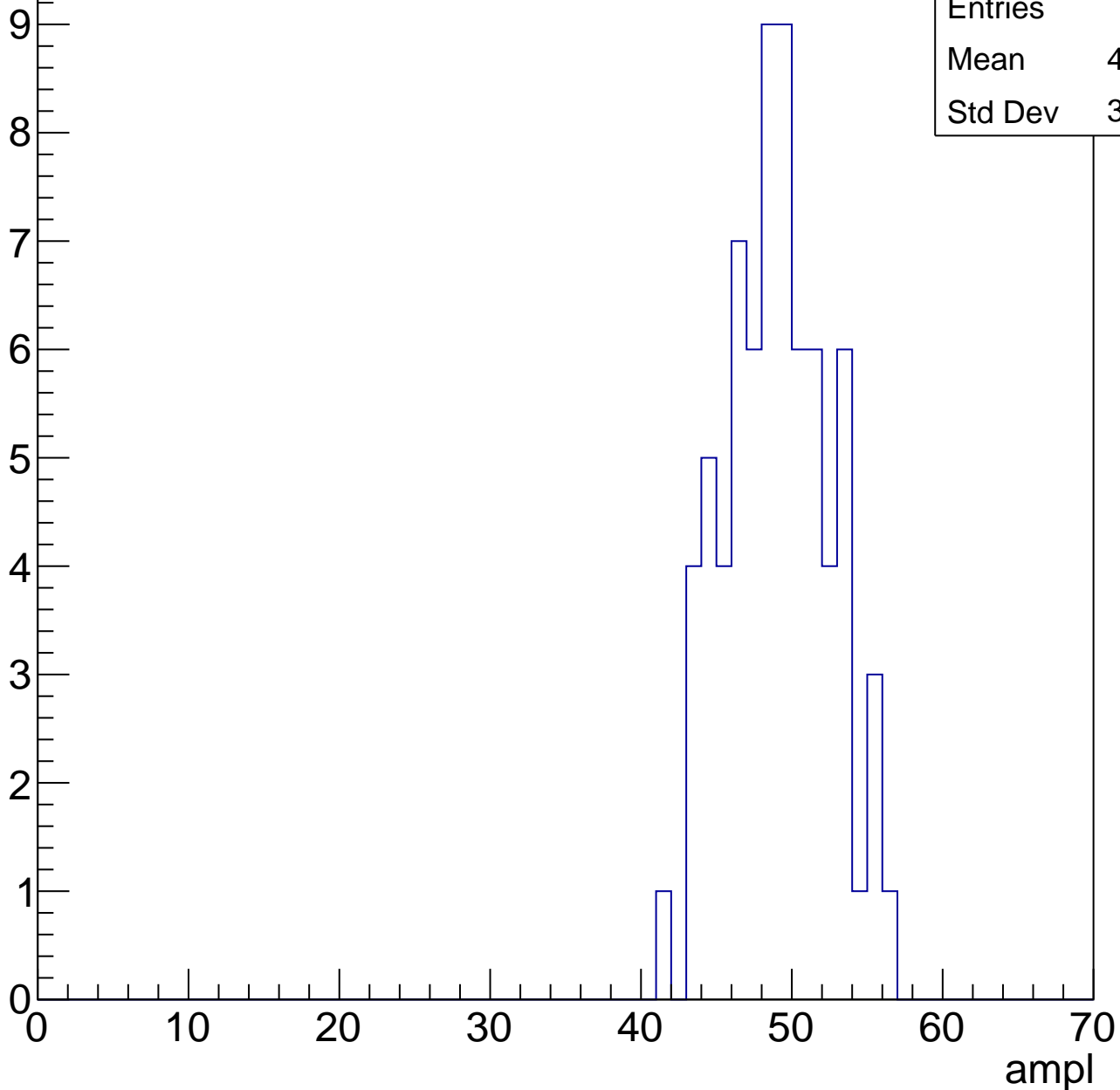


B1L103S, U9-ch104, adc3

calib_packv5_041523_1651.root, FC#0, port C2

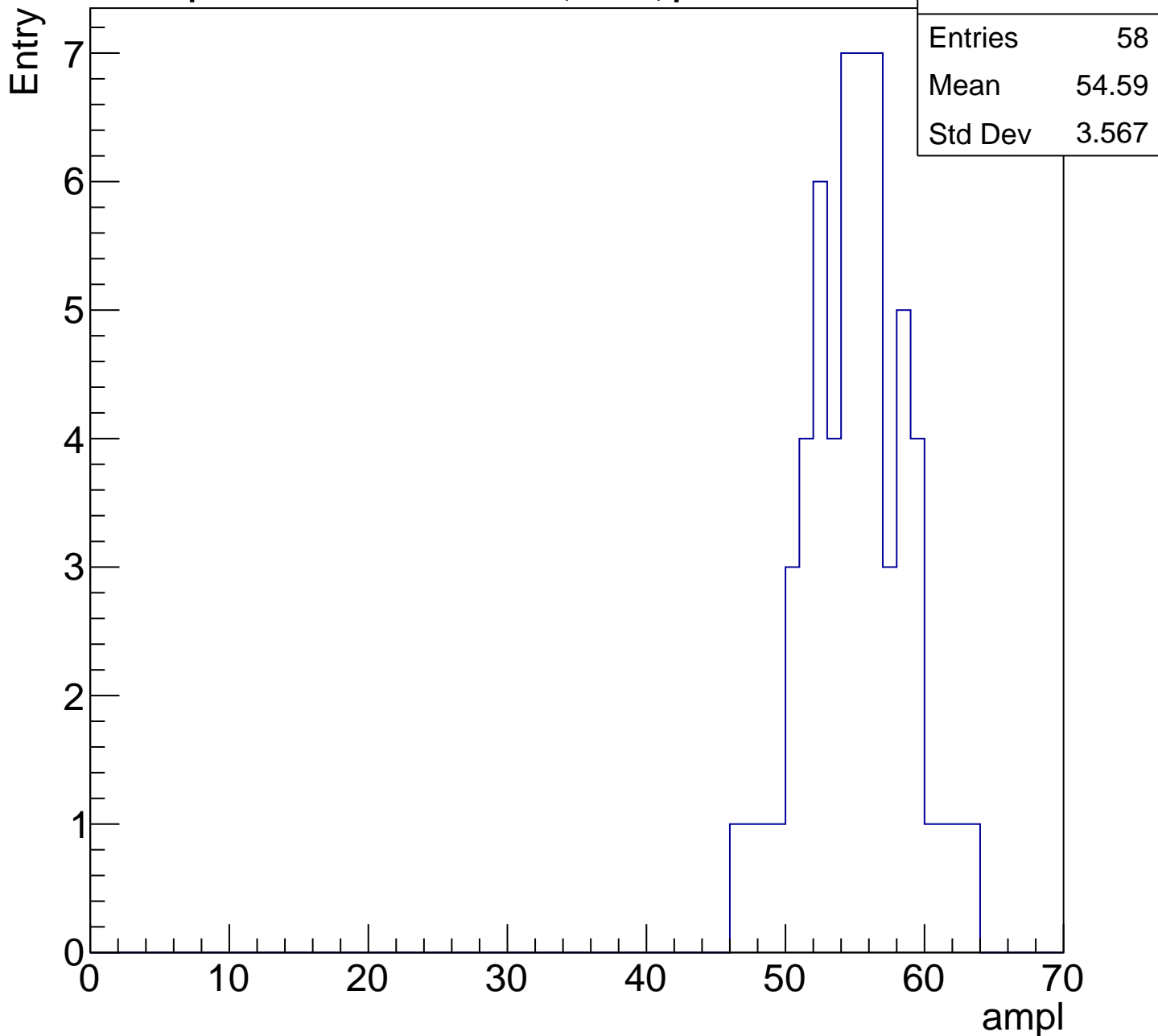
Entry

Entries	72
Mean	48.57
Std Dev	3.382



B1L103S, U9-ch104, adc4

calib_packv5_041523_1651.root, FC#0, port C2

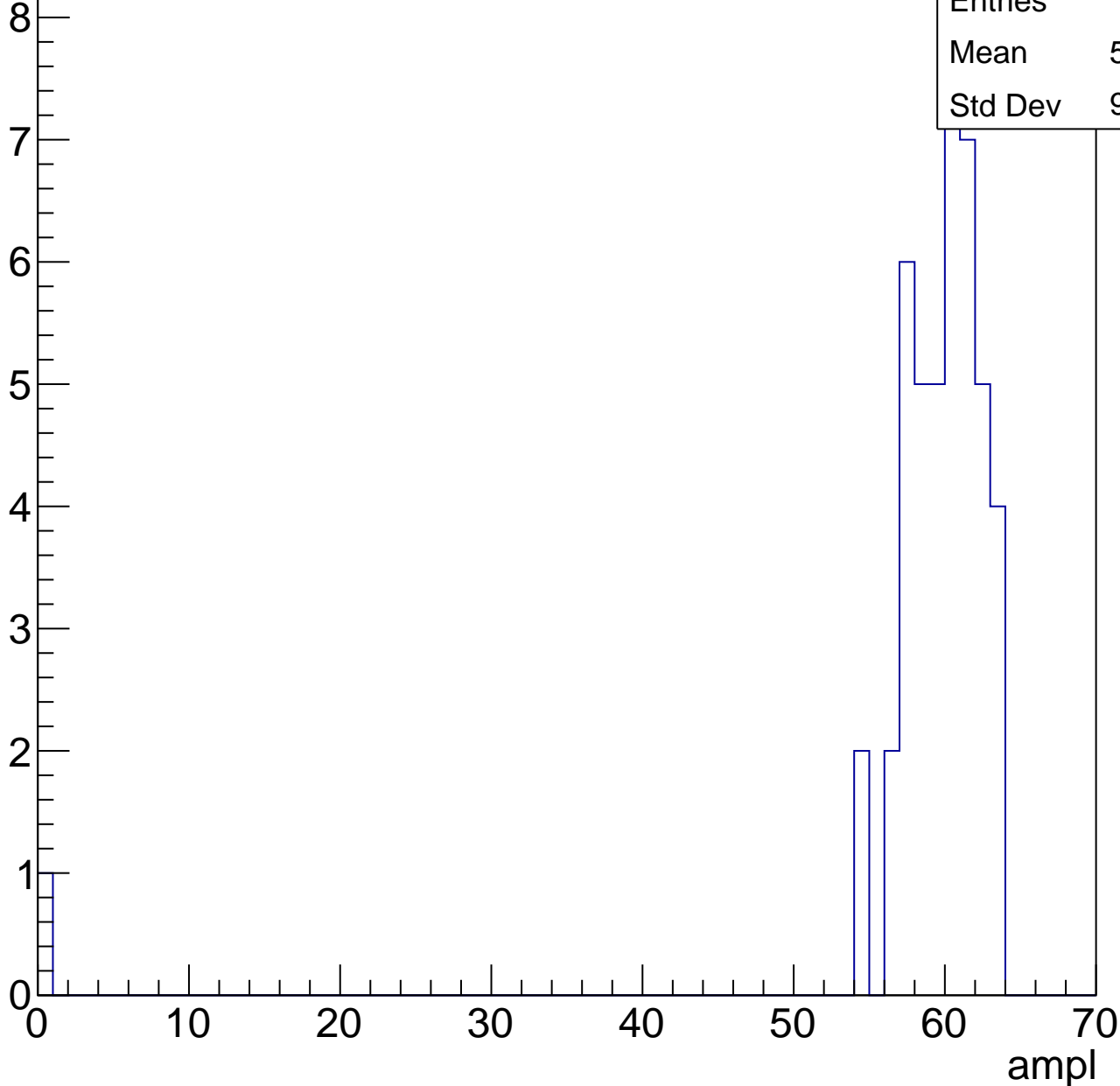


B1L103S, U9-ch104, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	45
Mean	58.13
Std Dev	9.054

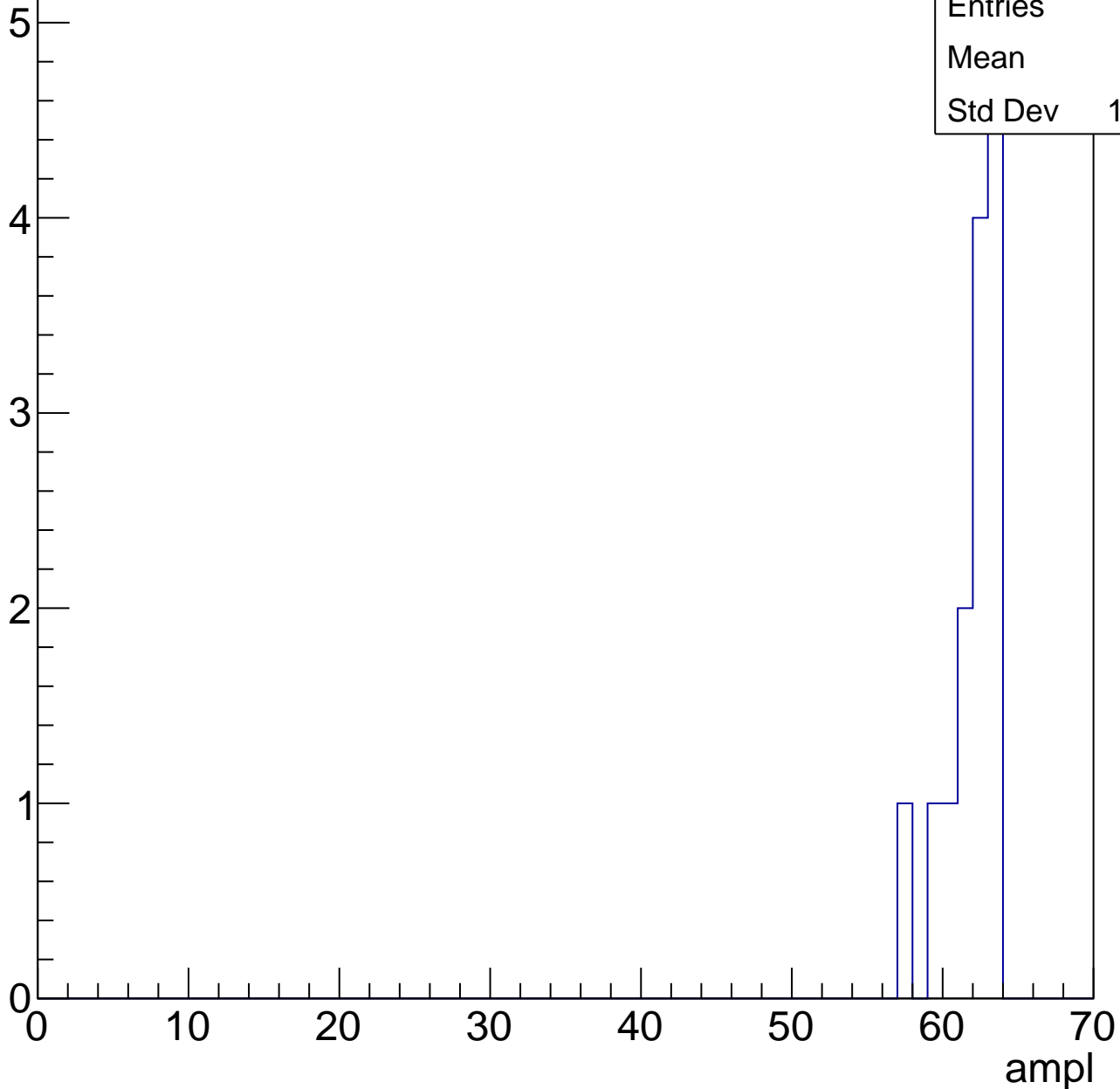


B1L103S, U9-ch104, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	14
Mean	61.5
Std Dev	1.722

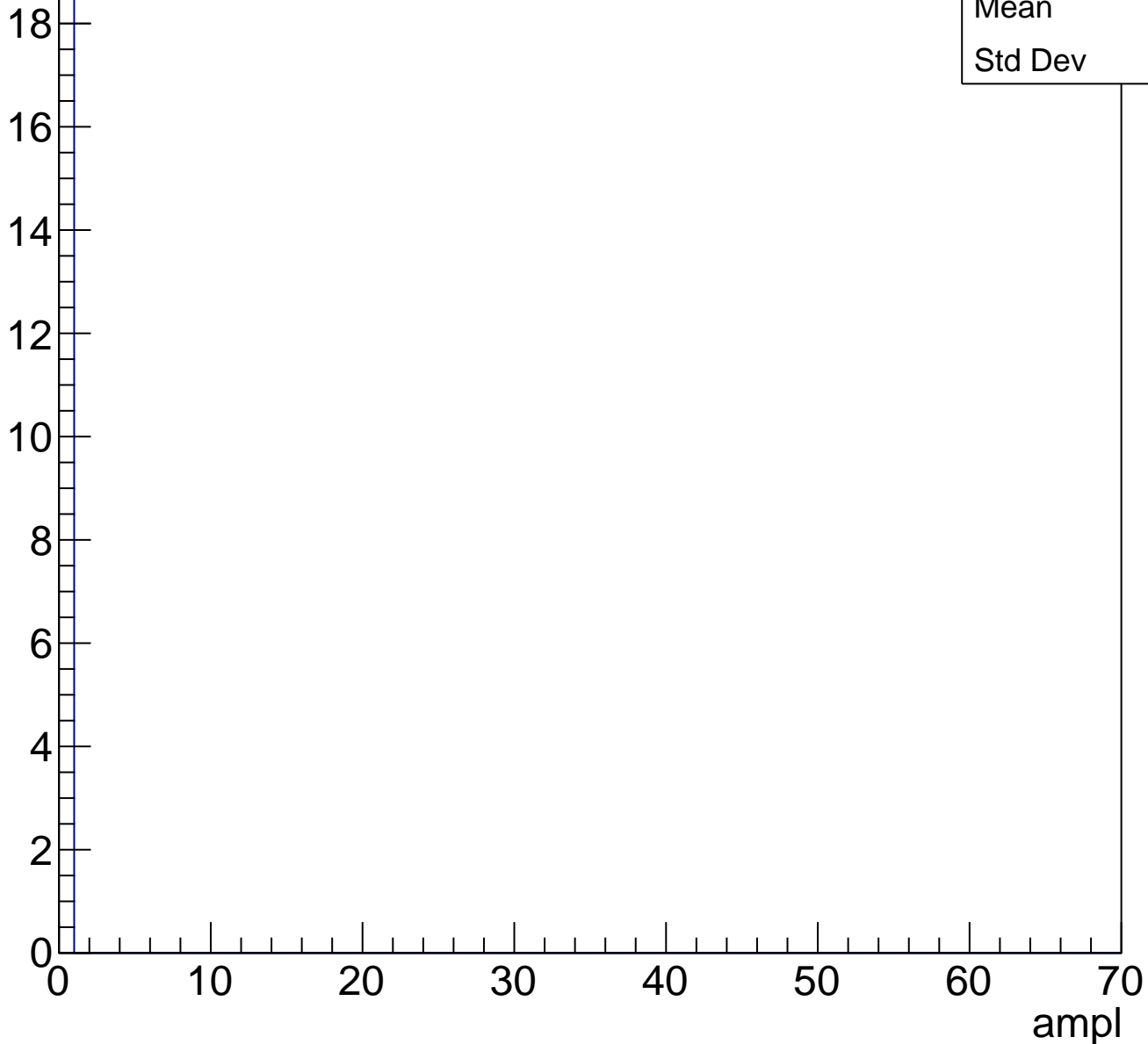


B1L103S, U9-ch104, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	0
Std Dev	0

Entry

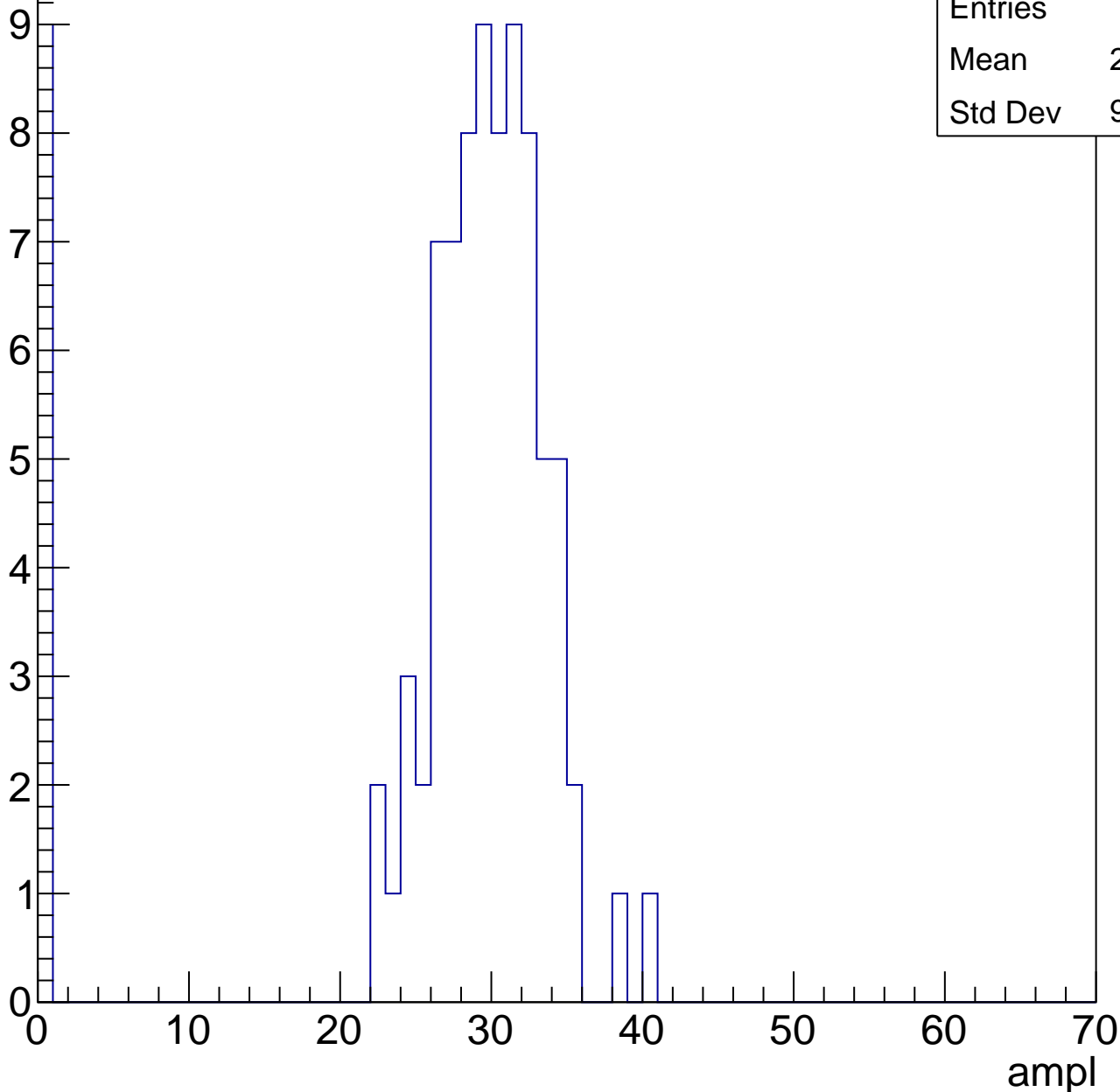


B1L103S, U9-ch105, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

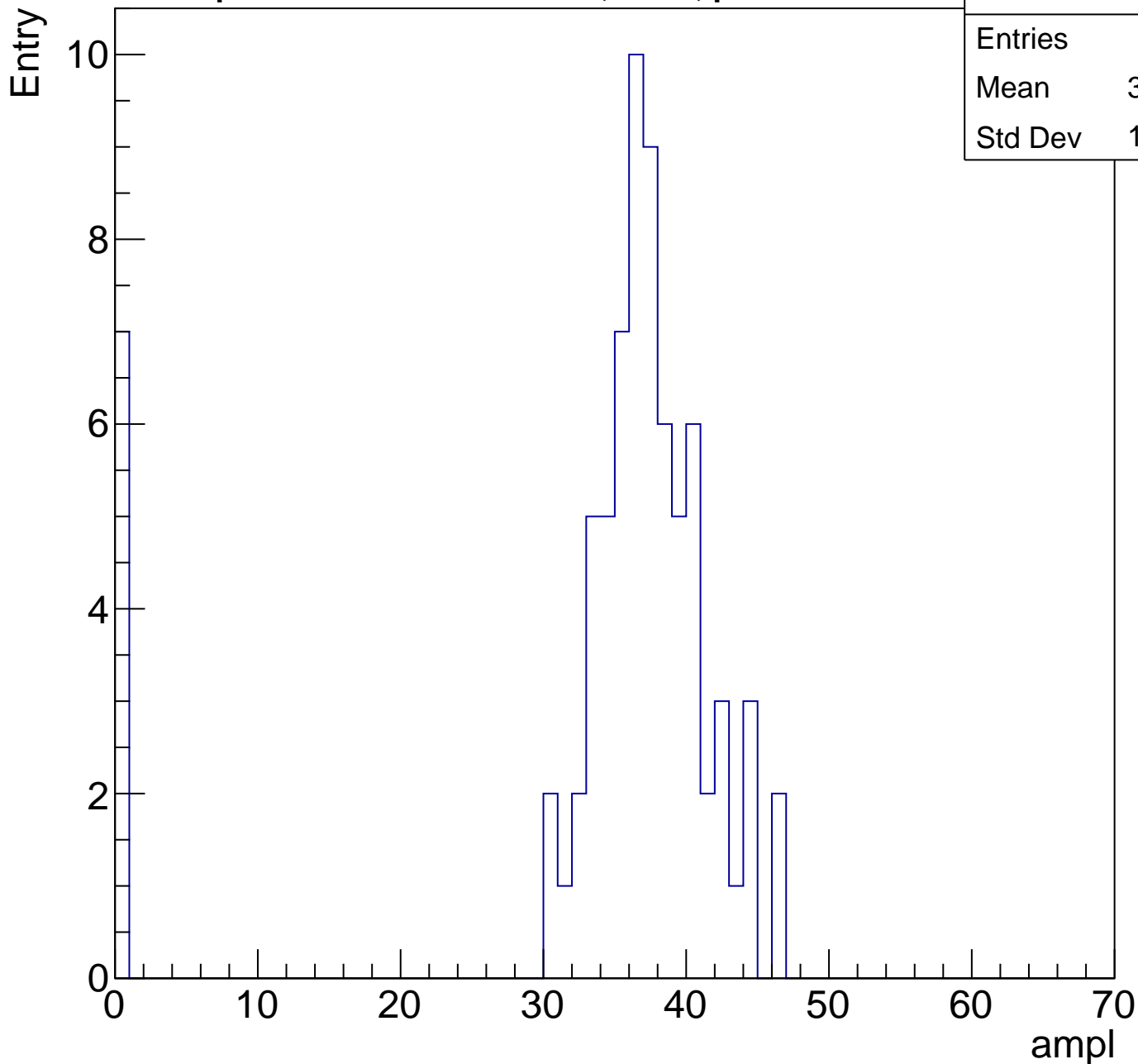
Entries	87
Mean	26.47
Std Dev	9.558



B1L103S, U9-ch105, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	76
Mean	33.76
Std Dev	11.28

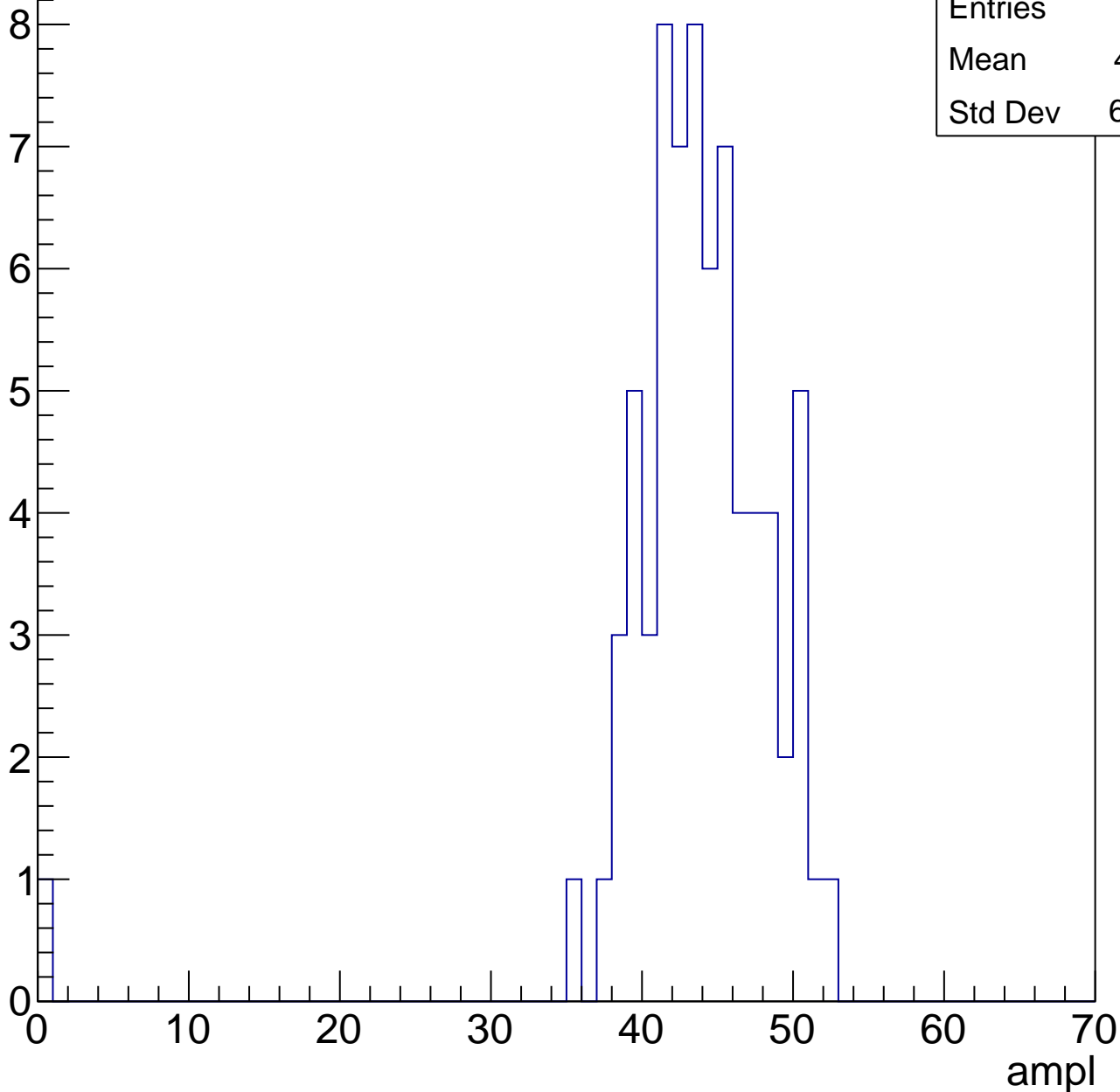


B1L103S, U9-ch105, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	43.11
Std Dev	6.352

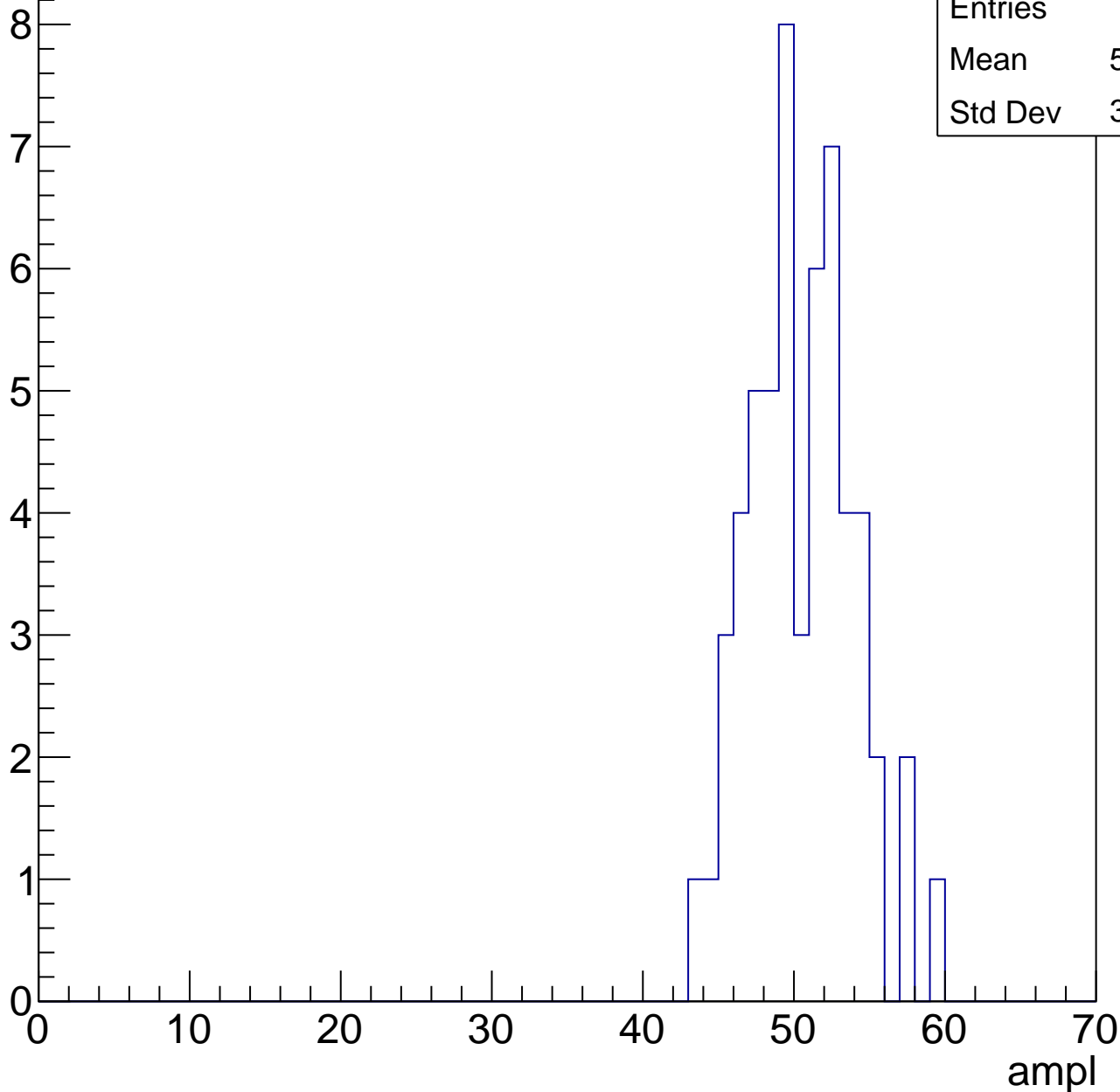


B1L103S, U9-ch105, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	50.07
Std Dev	3.432



B1L103S, U9-ch105, adc4

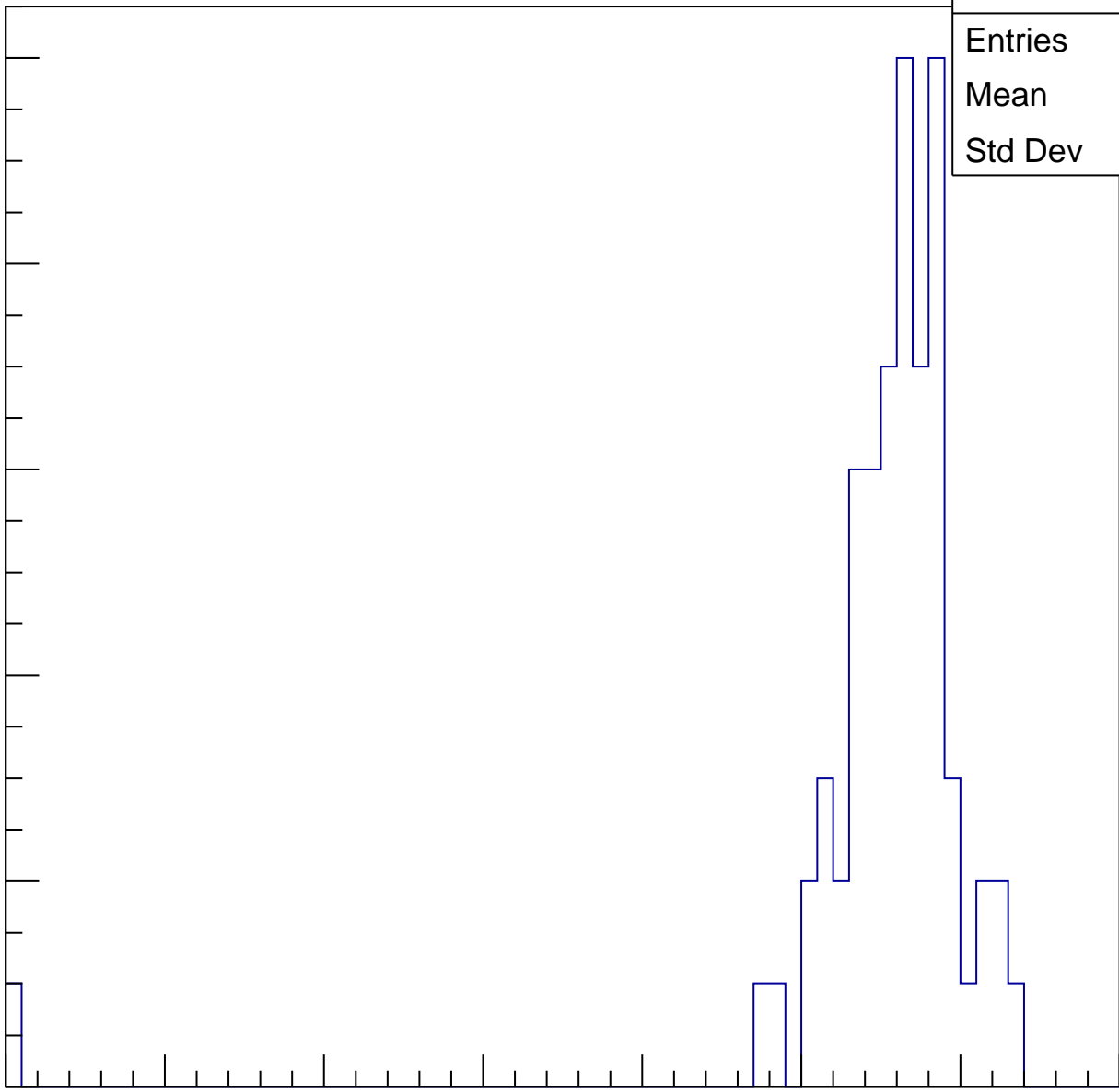
calib_packv5_041523_1651.root, FC#0, port C2

Entries	65
Mean	54.83
Std Dev	7.562

Entry

10
8
6
4
2
0

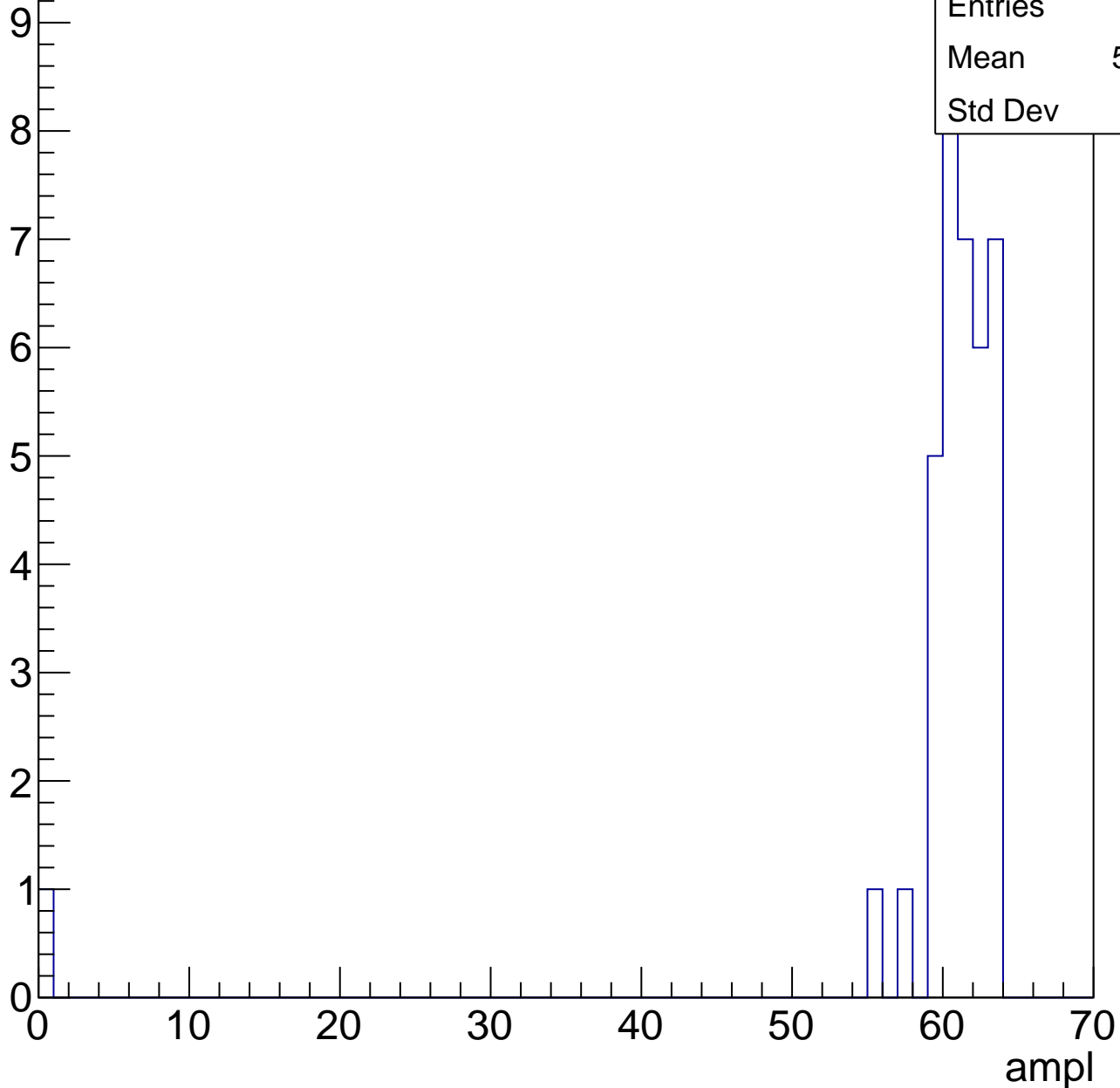
0 10 20 30 40 50 60 70
ampl



B1L103S, U9-ch105, adc5

calib_packv5_041523_1651.root, FC#0, port C2

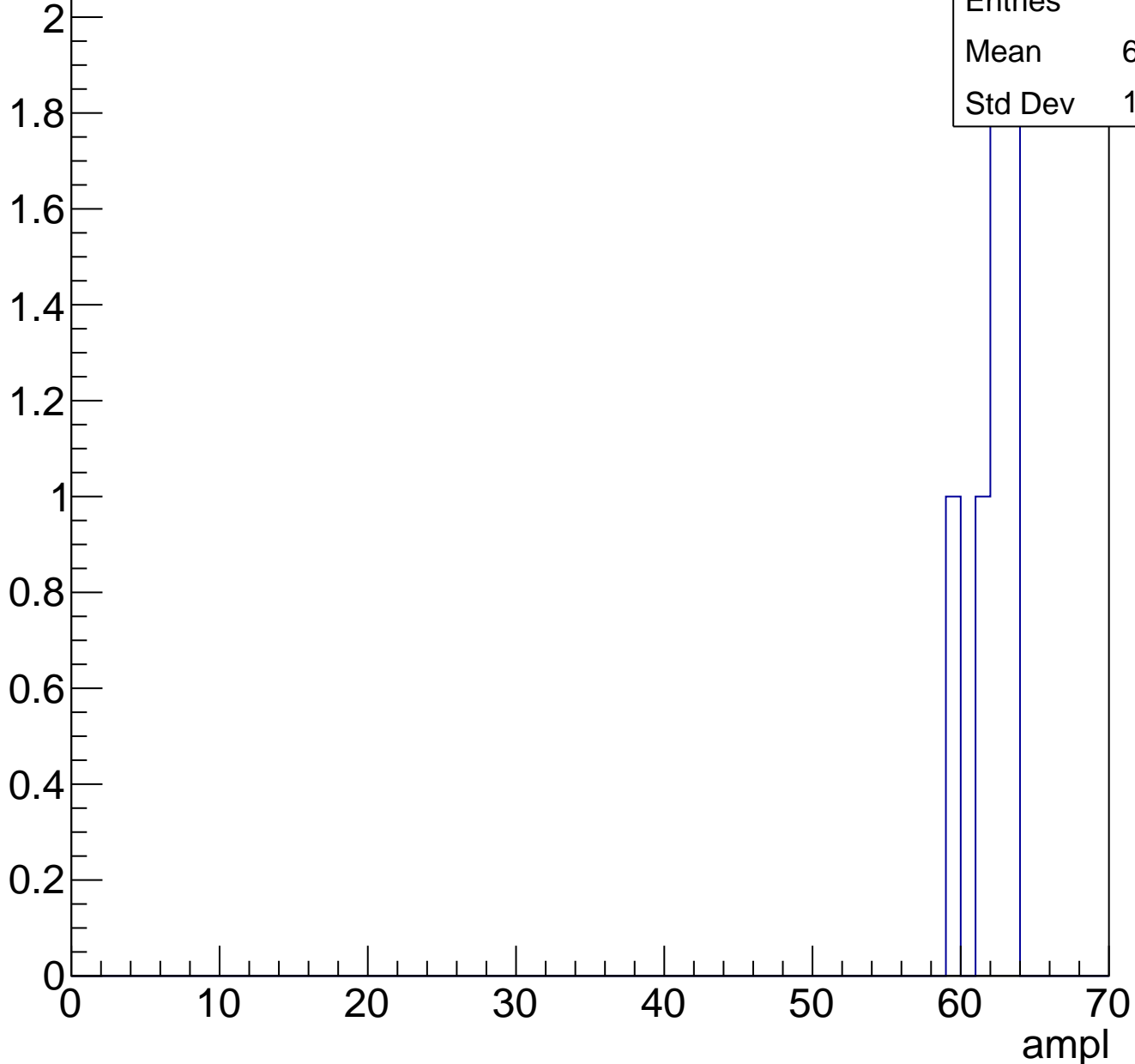
Entry



B1L103S, U9-ch105, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch105, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

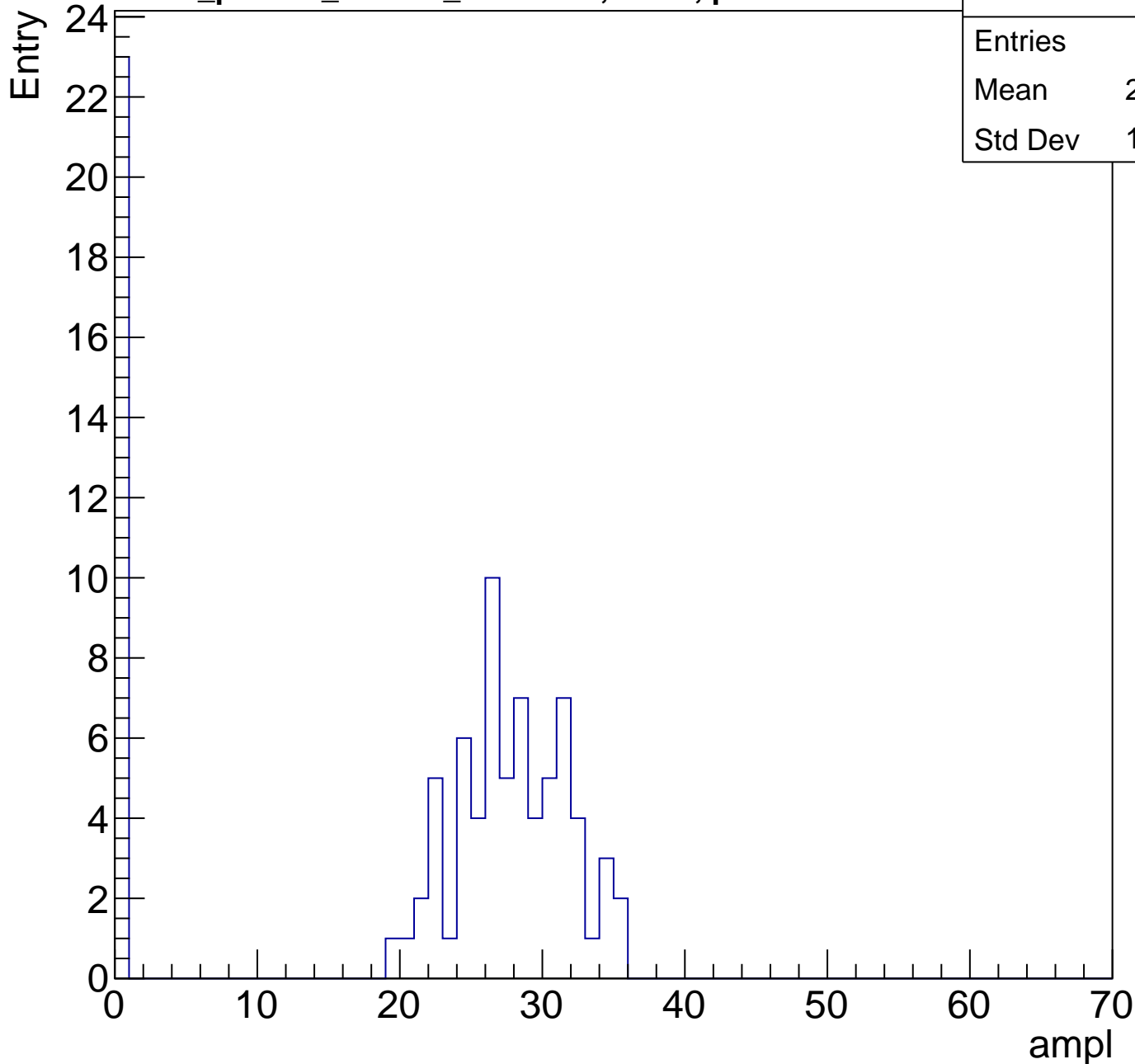
ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U9-ch106, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	91
Mean	20.49
Std Dev	12.36

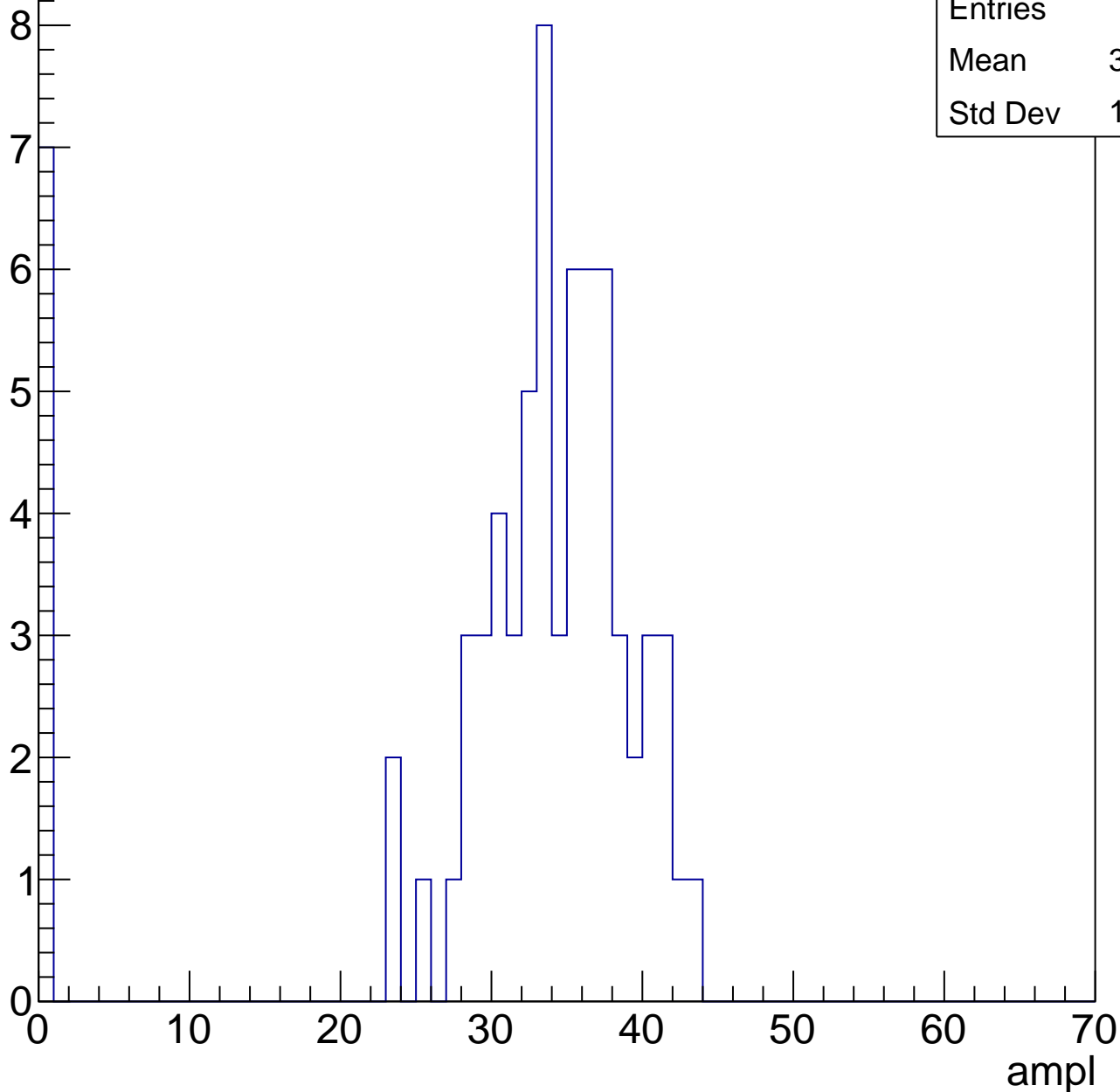


B1L103S, U9-ch106, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	30.65
Std Dev	10.97

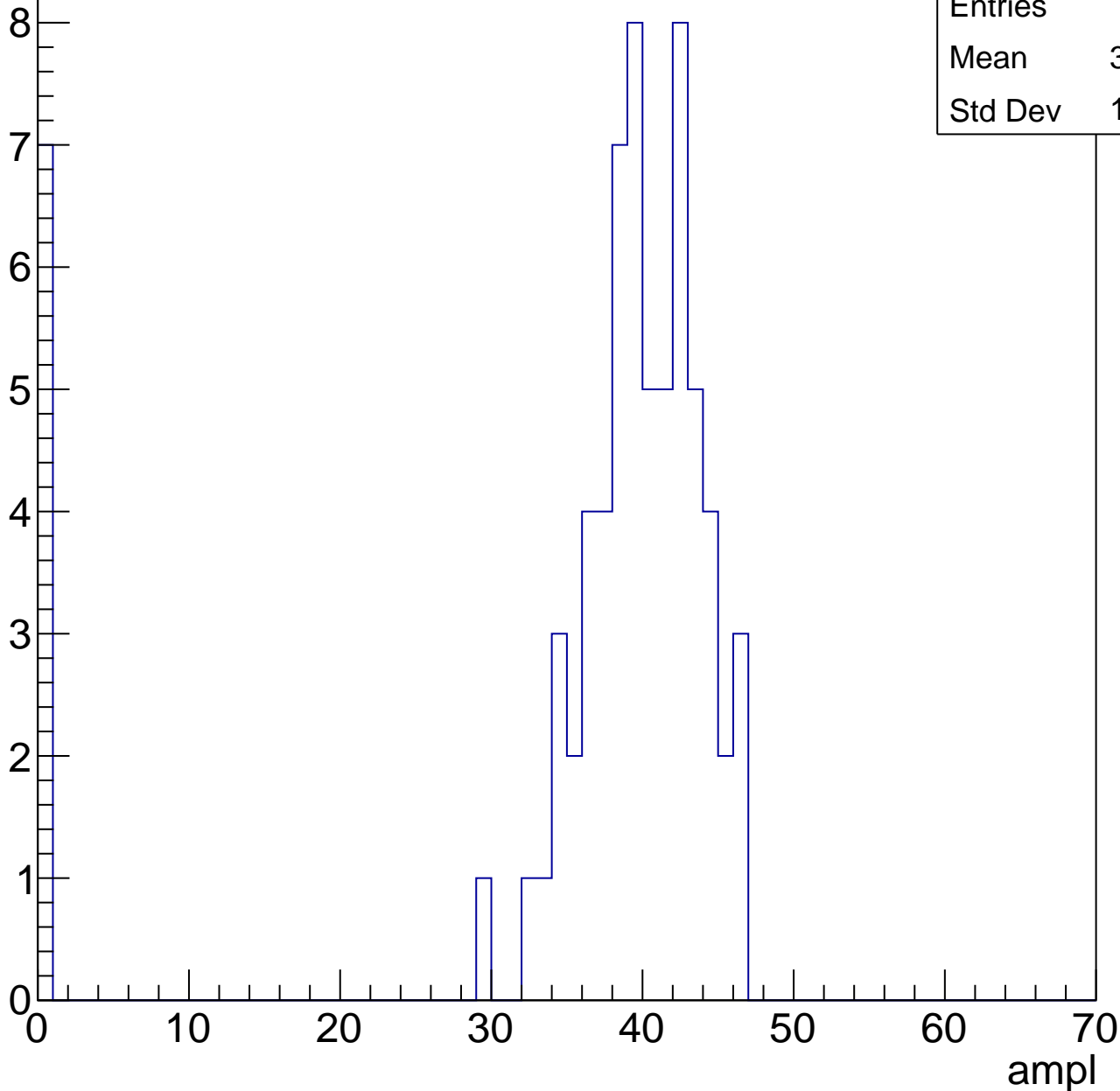


B1L103S, U9-ch106, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	35.66
Std Dev	12.37



B1L103S, U9-ch106, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	73
Mean	47.11
Std Dev	3.237

Entry

10

8

6

4

2

0

0

10

20

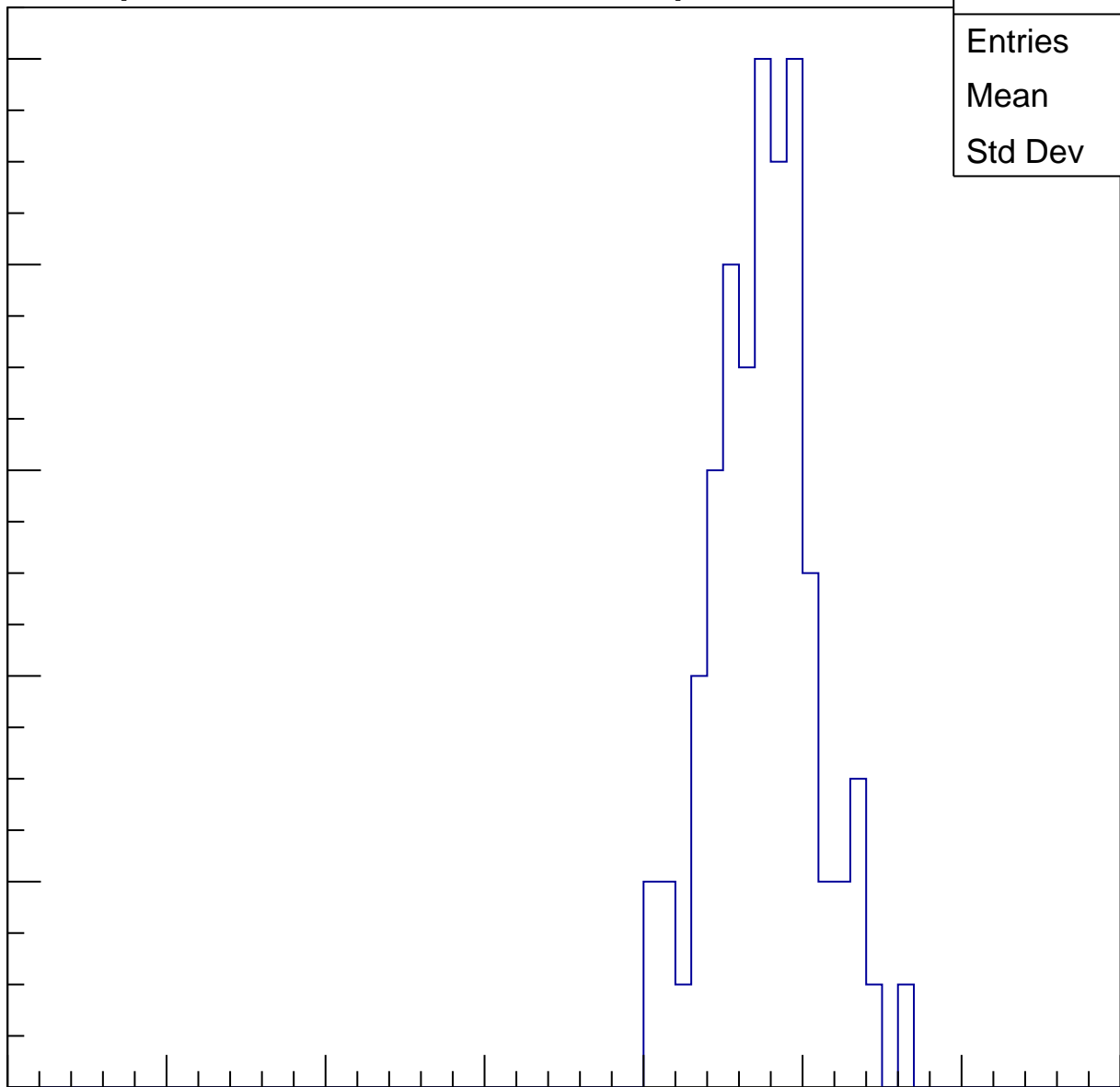
30

40

50

60

ampl

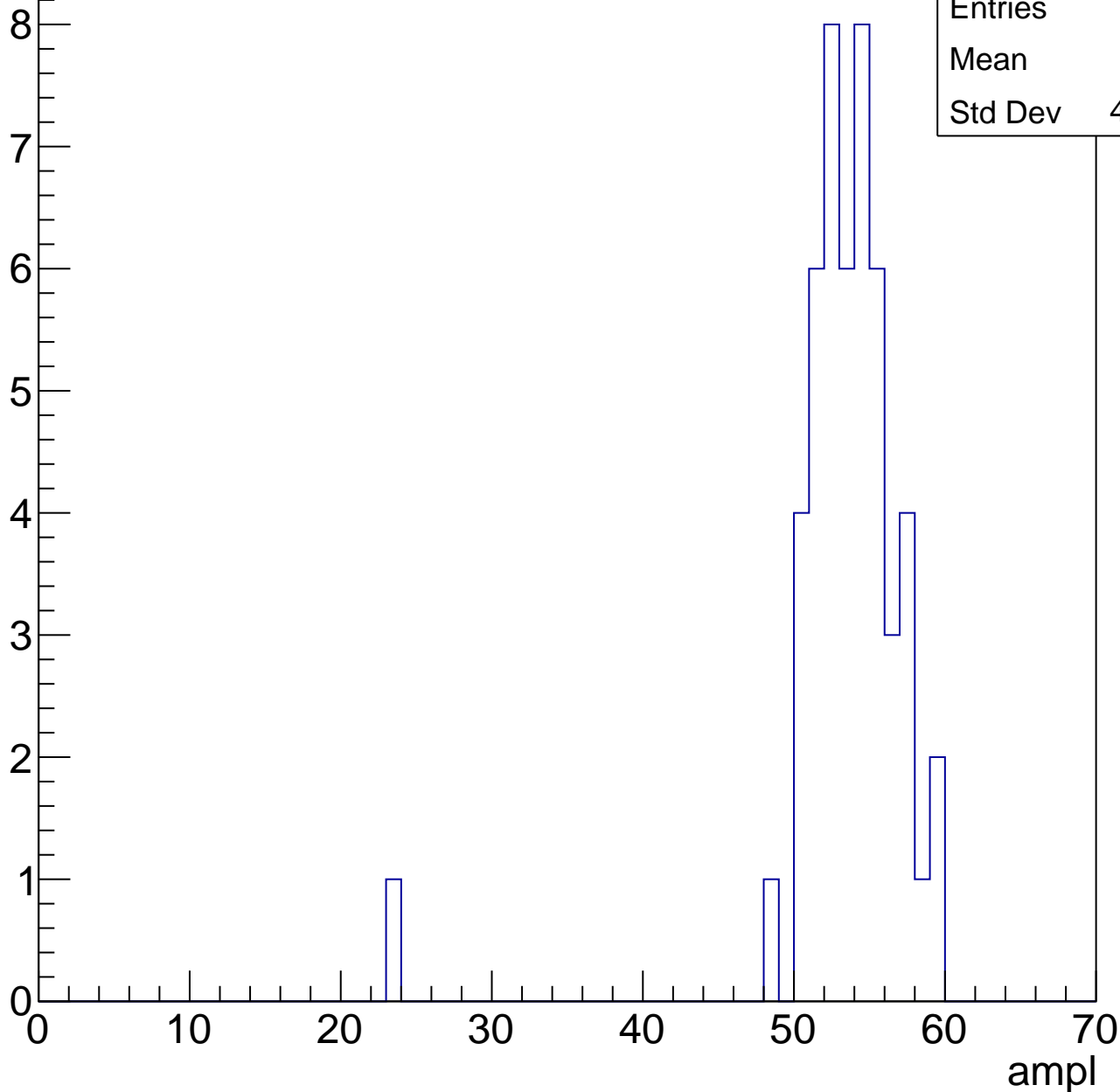


B1L103S, U9-ch106, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	52.9
Std Dev	4.924

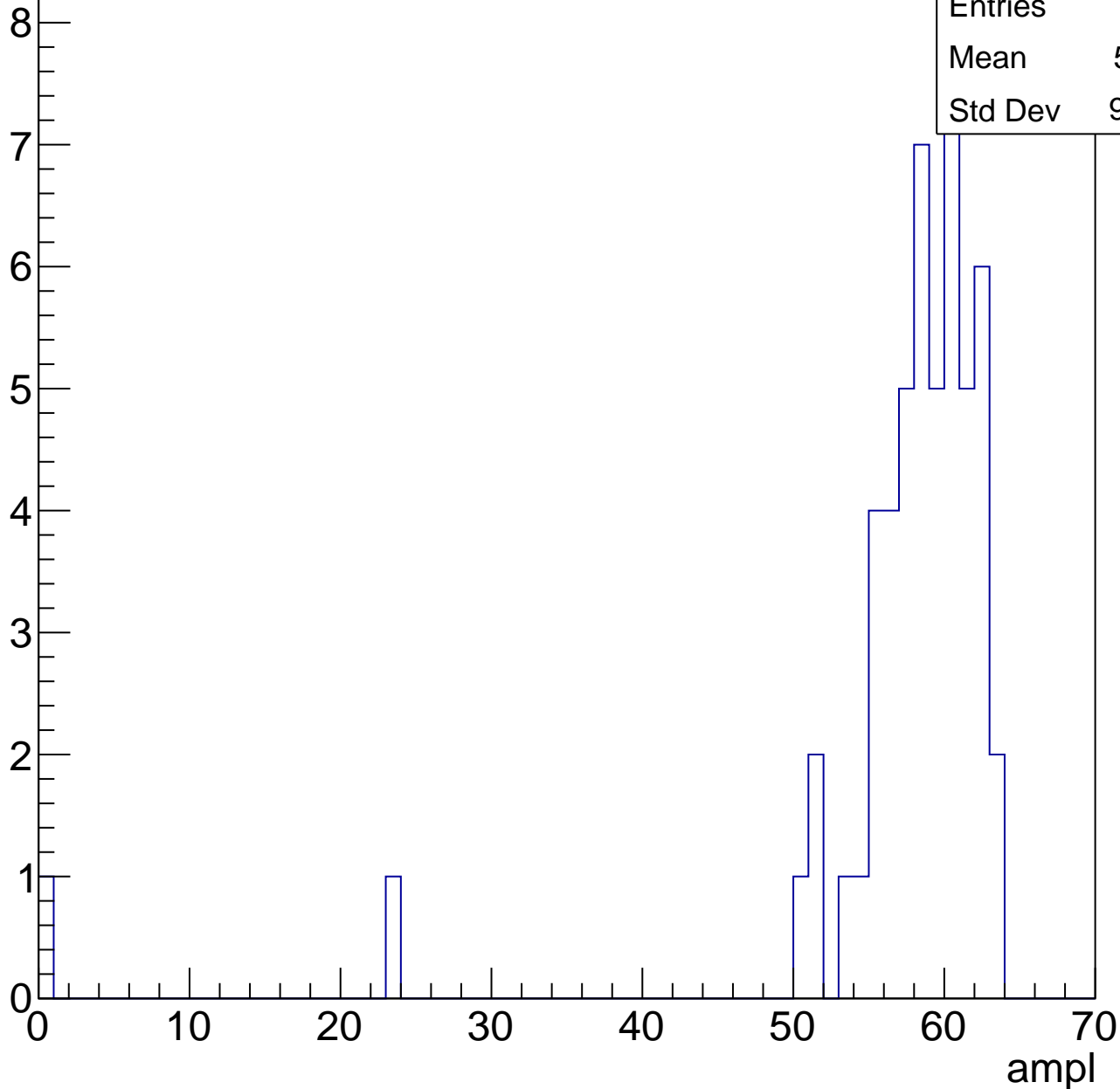


B1L103S, U9-ch106, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	56.51
Std Dev	9.673

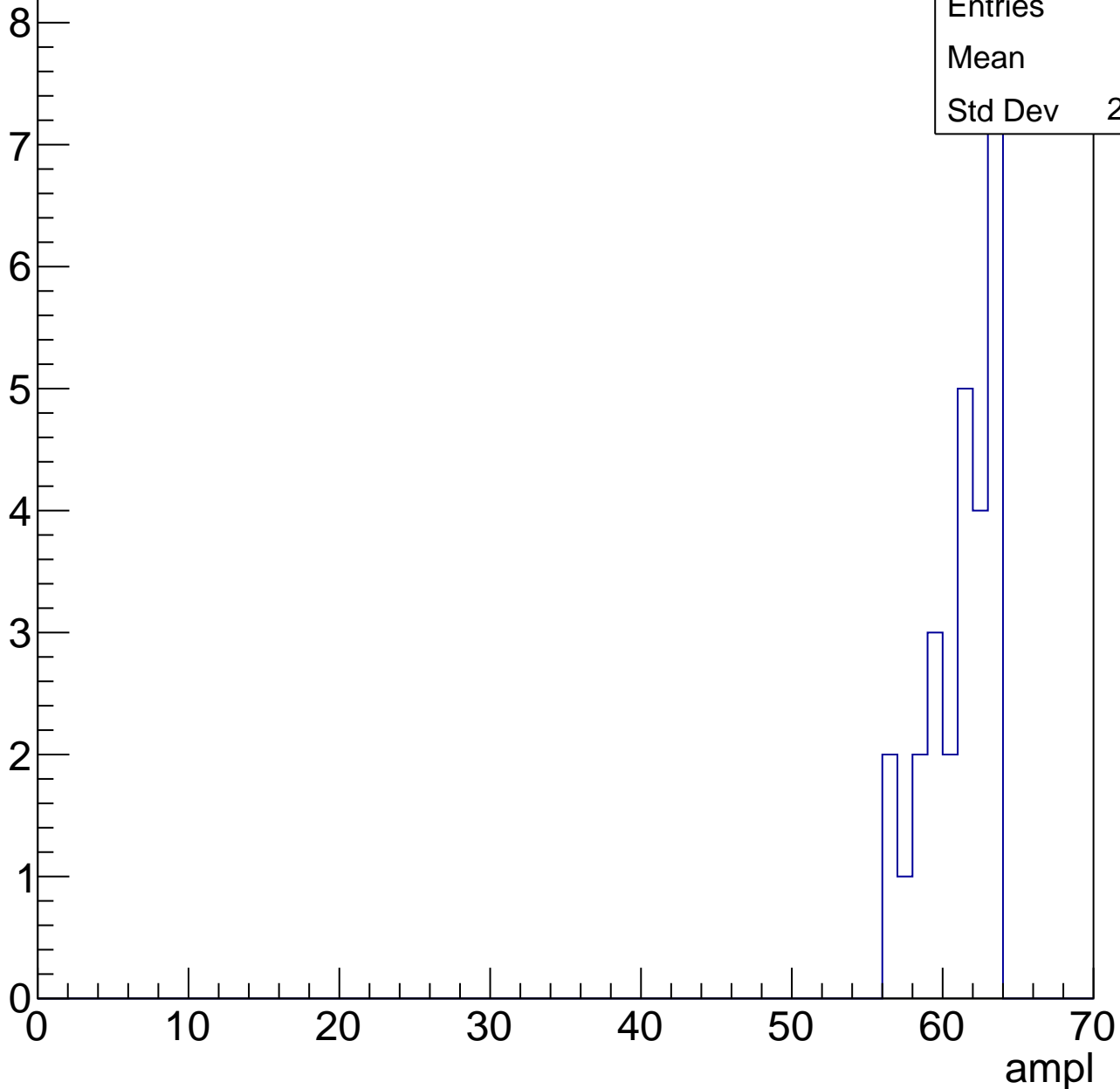


B1L103S, U9-ch106, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	27
Mean	60.7
Std Dev	2.208



B1L103S, U9-ch106, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

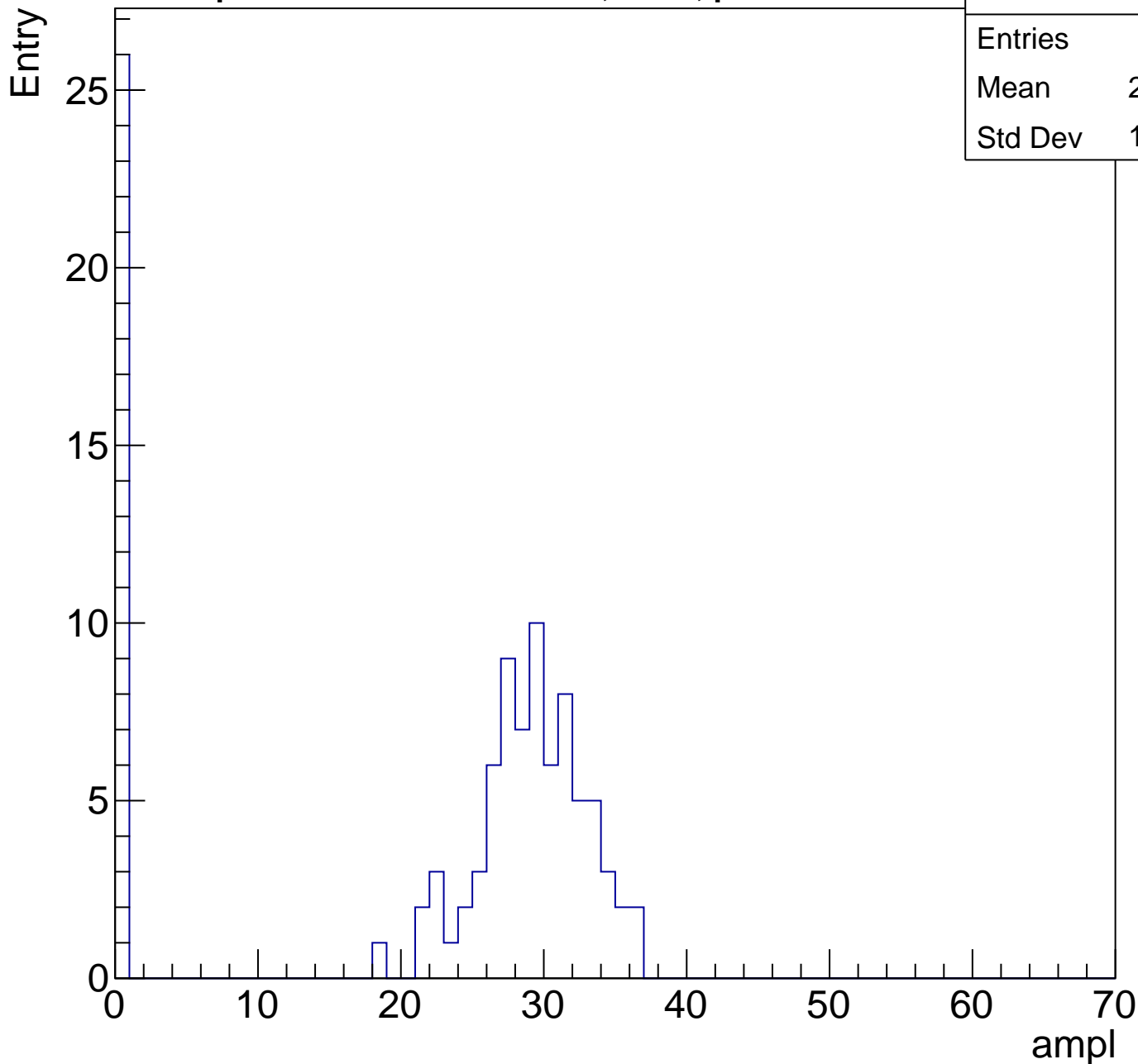
ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U9-ch107, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	101
Mean	21.33
Std Dev	12.96

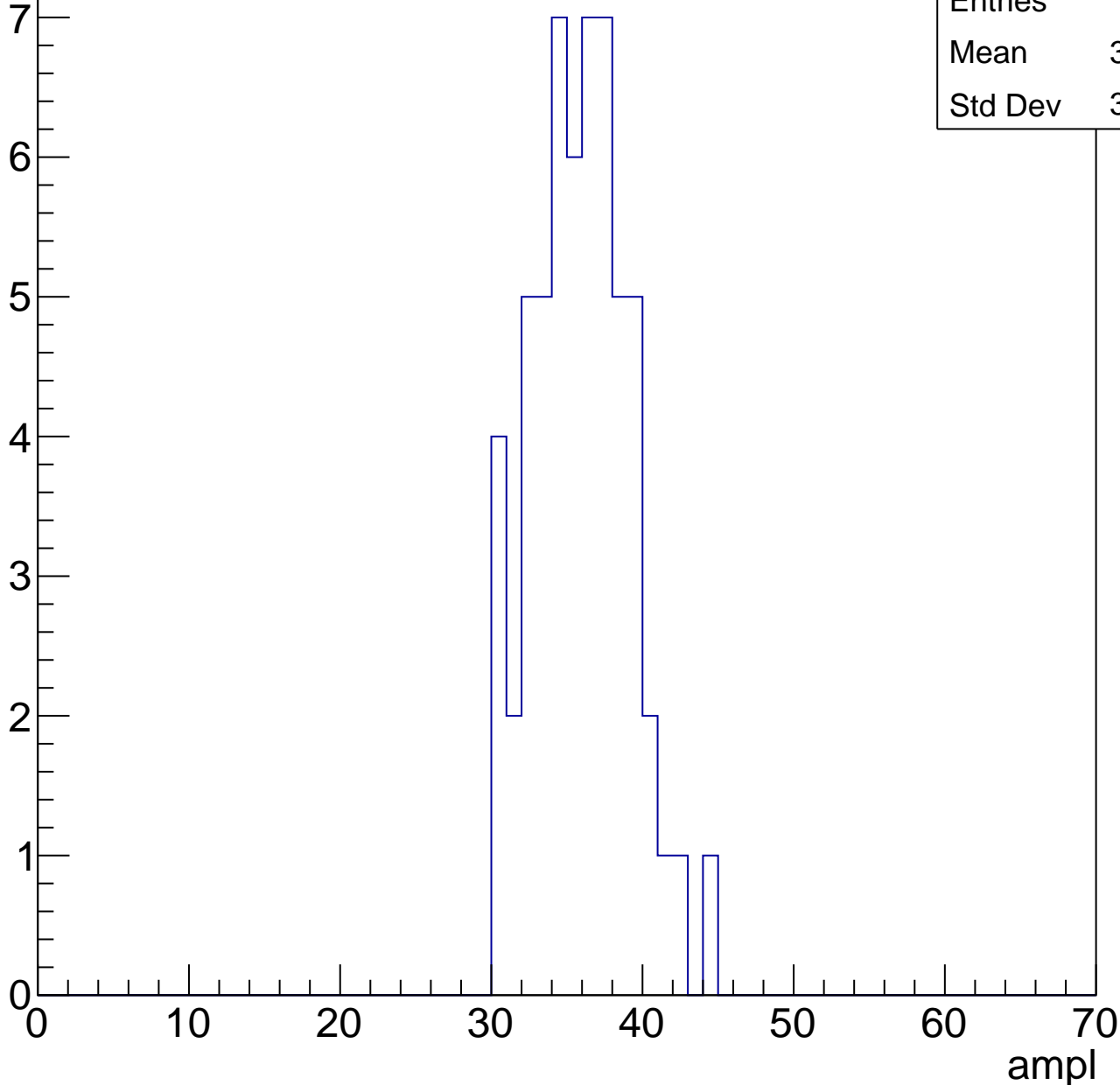


B1L103S, U9-ch107, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	35.48
Std Dev	3.125

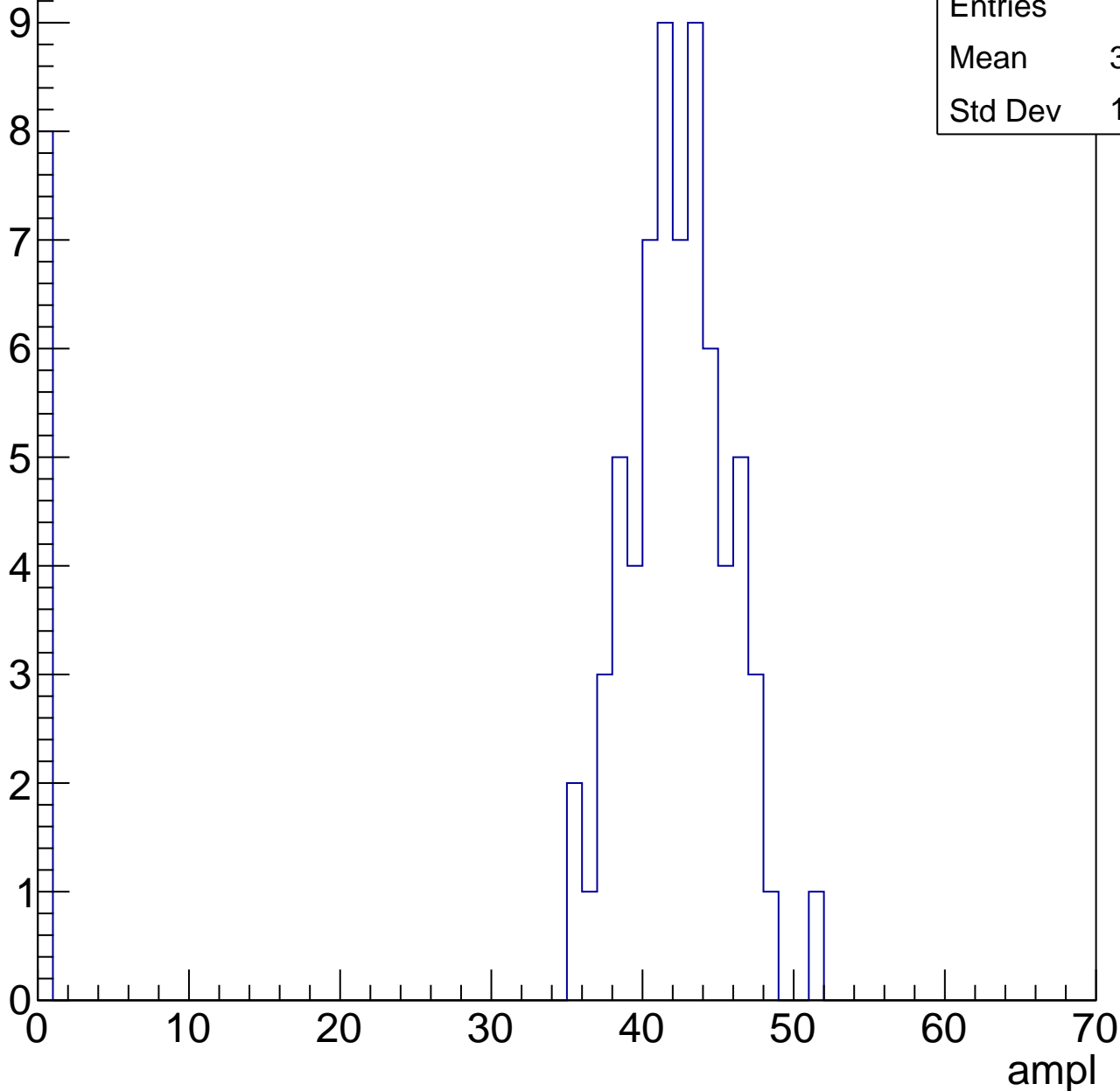


B1L103S, U9-ch107, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	37.43
Std Dev	13.29

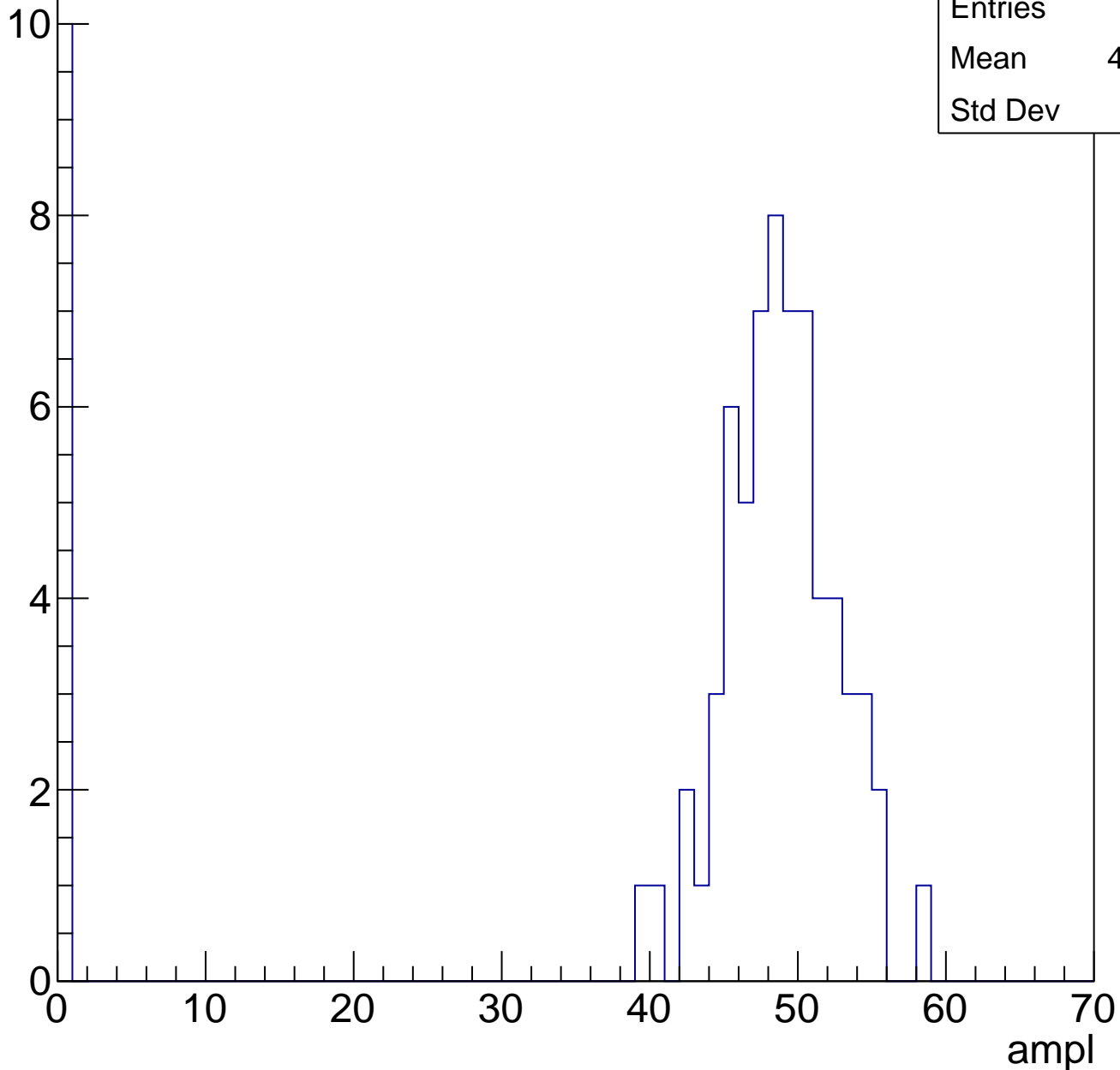


B1L103S, U9-ch107, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	41.93
Std Dev	16.8

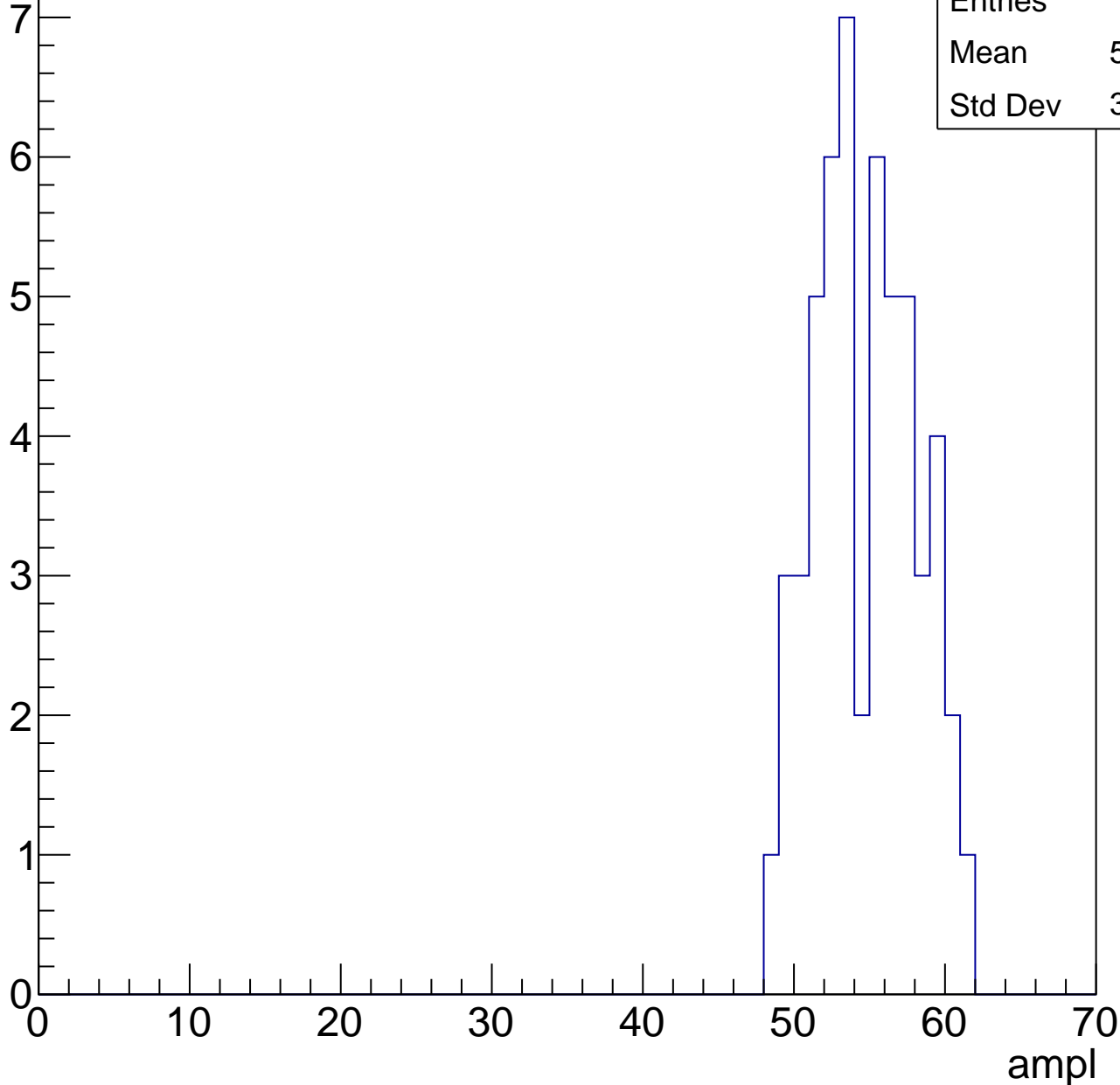
Entry



B1L103S, U9-ch107, adc4

calib_packv5_041523_1651.root, FC#0, port C2

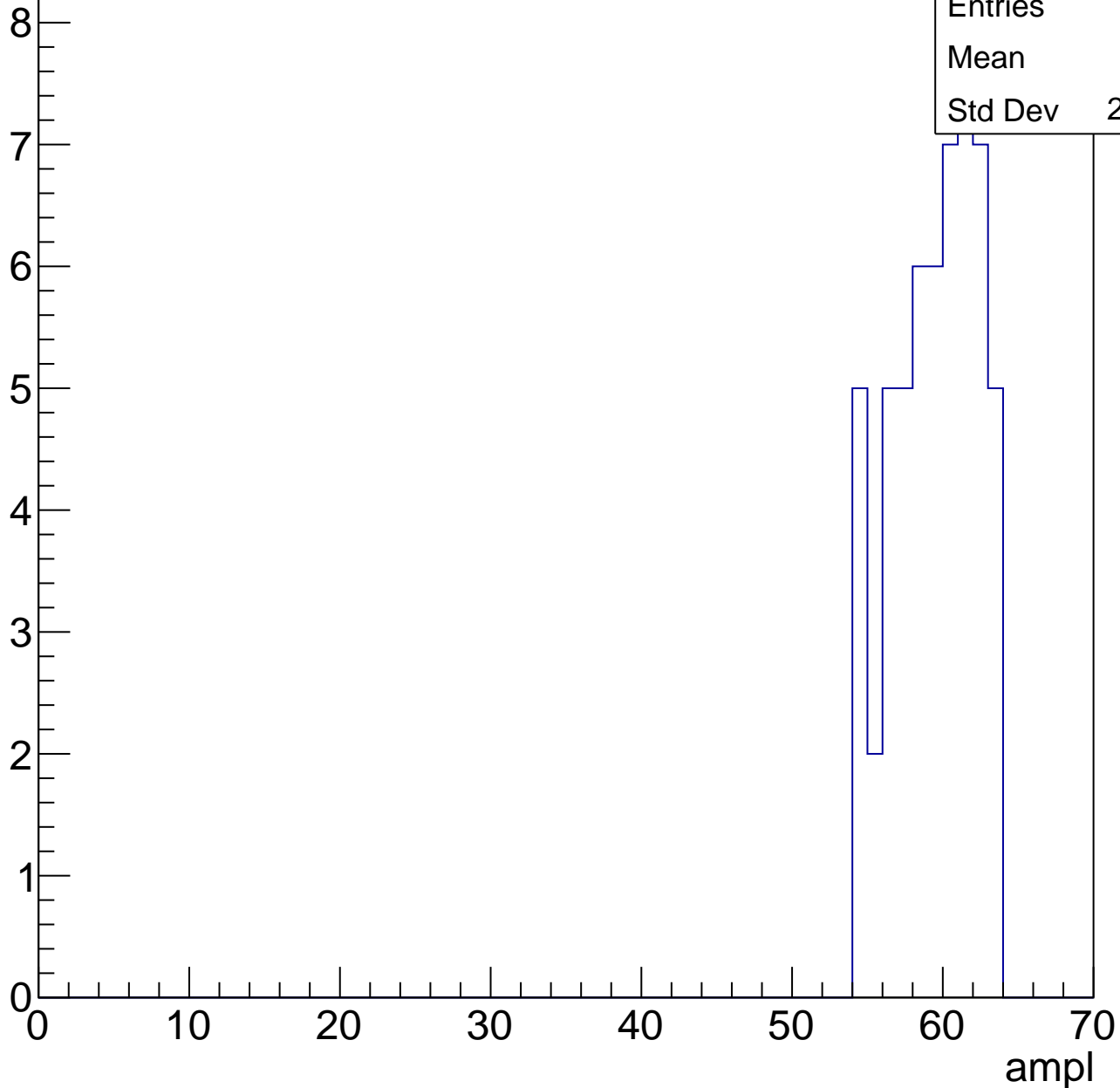
Entry



B1L103S, U9-ch107, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

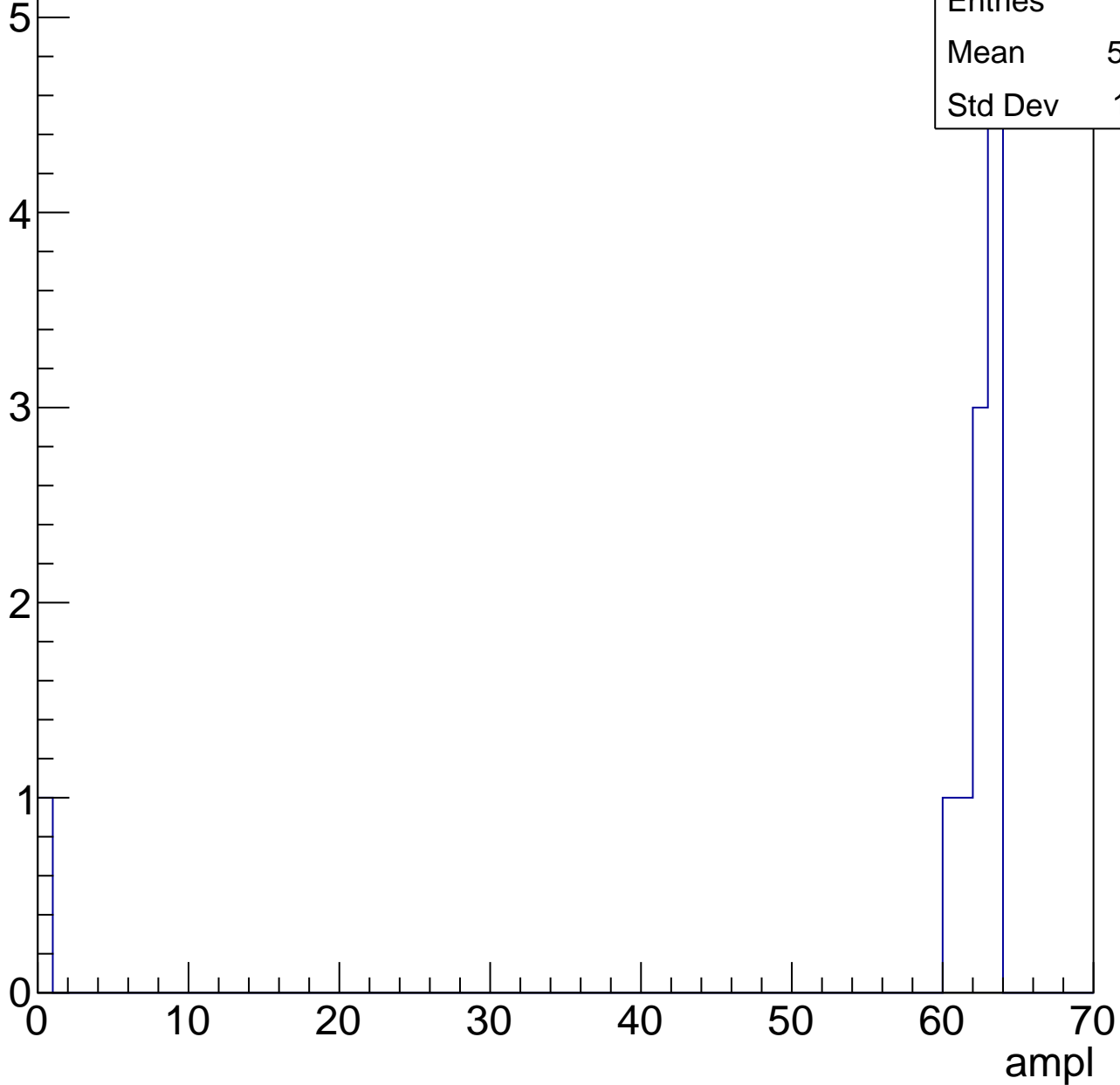


B1L103S, U9-ch107, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	11
Mean	56.55
Std Dev	17.91



B1L103S, U9-ch107, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U9-ch108, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	76
Mean	25.04
Std Dev	10.74

Entry

10

8

6

4

2

0

0

10

20

30

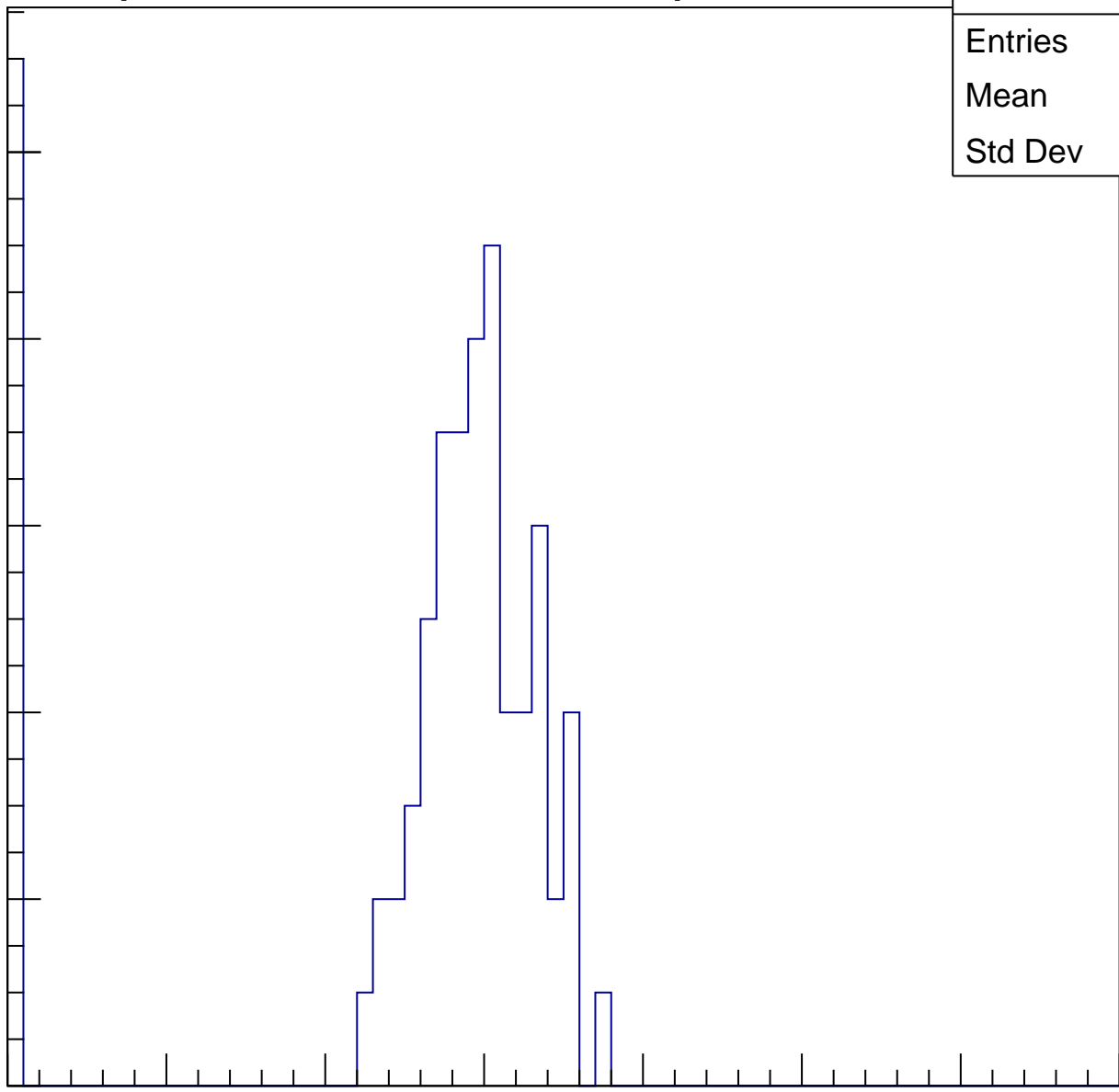
40

50

60

70

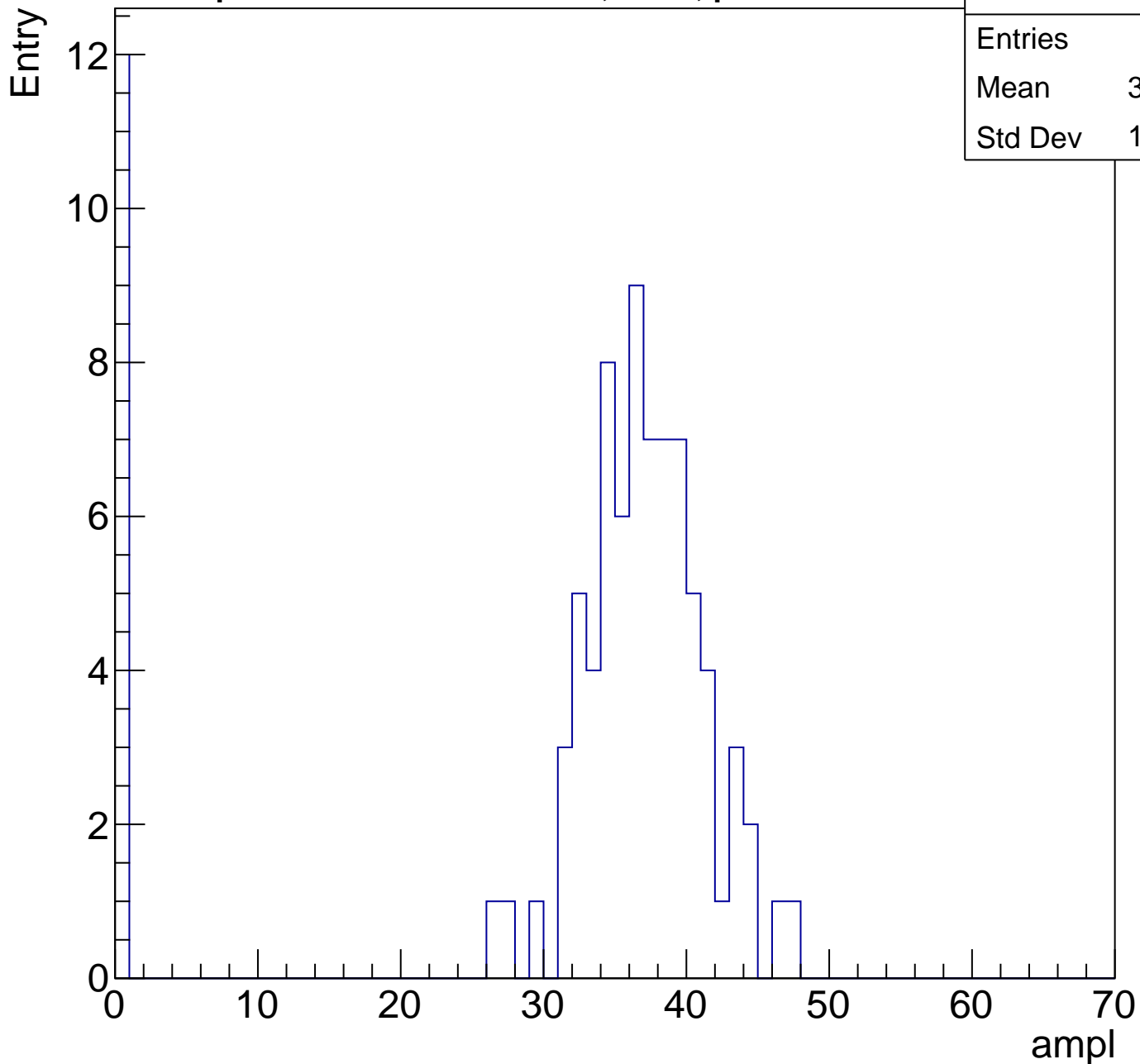
ampl



B1L103S, U9-ch108, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	88
Mean	31.67
Std Dev	13.13

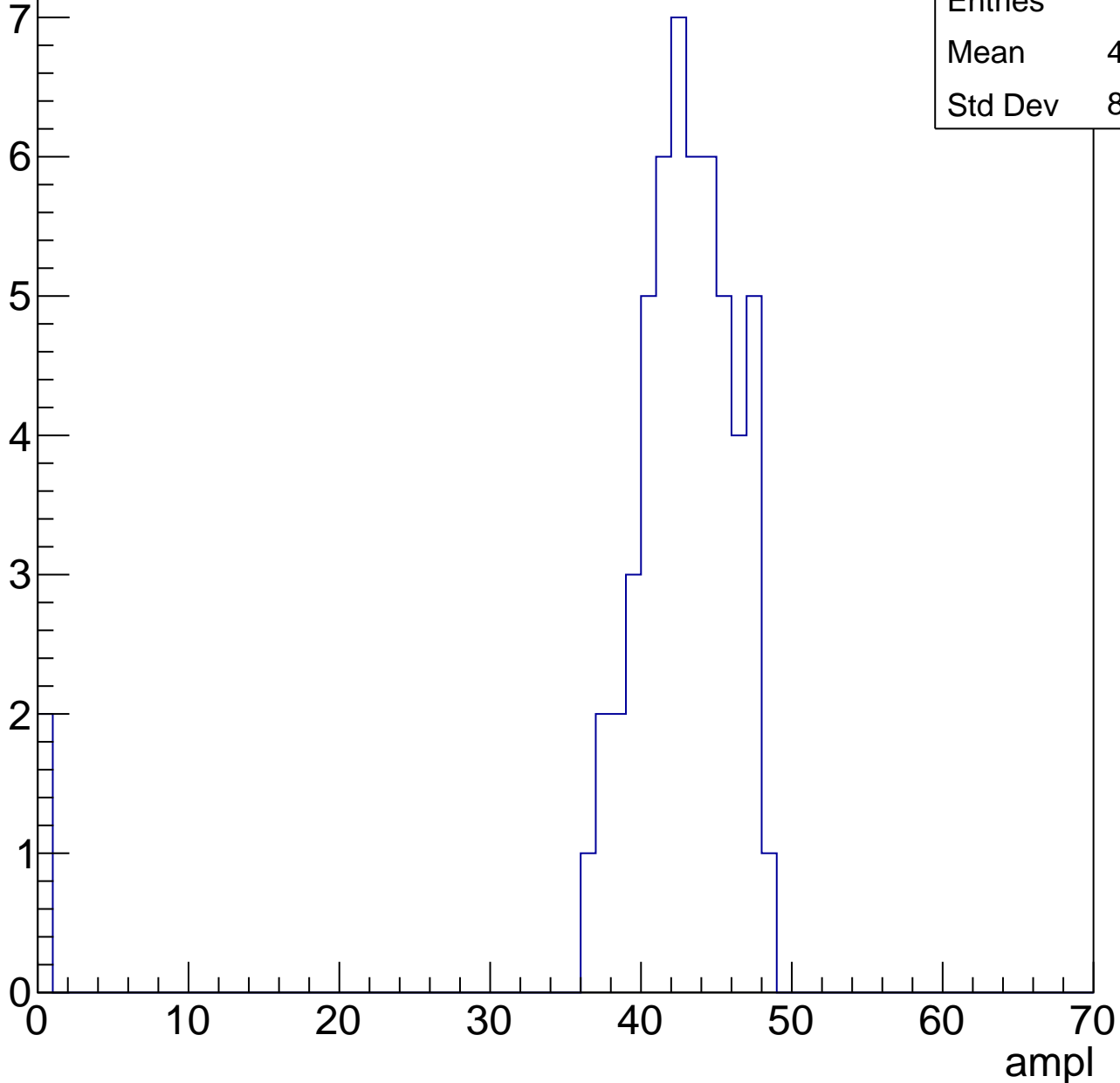


B1L103S, U9-ch108, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	41.04
Std Dev	8.472

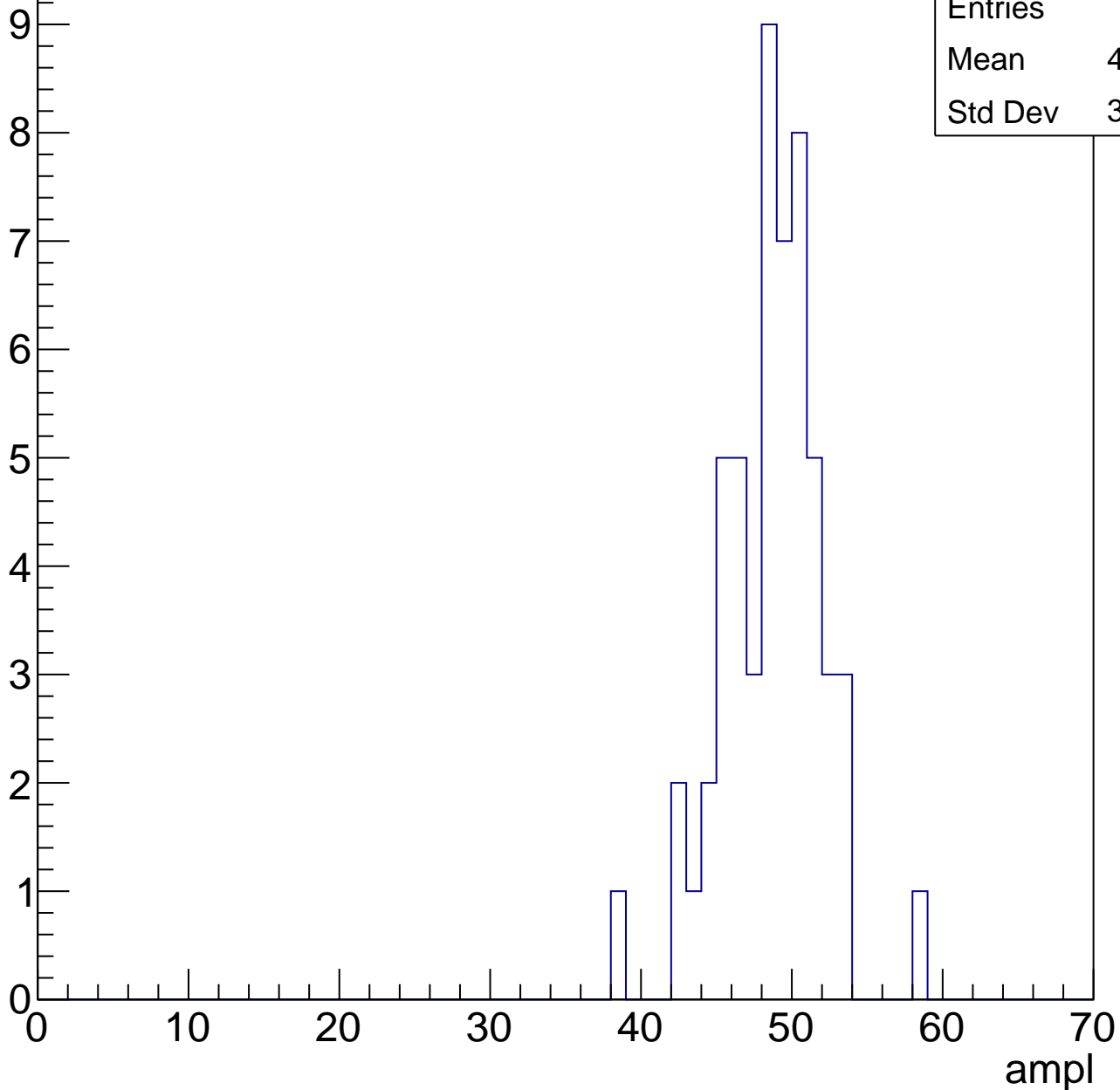


B1L103S, U9-ch108, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	48.22
Std Dev	3.307



B1L103S, U9-ch108, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	67
Mean	53.6
Std Dev	7.232

Entry

10

8

6

4

2

0

0

10

20

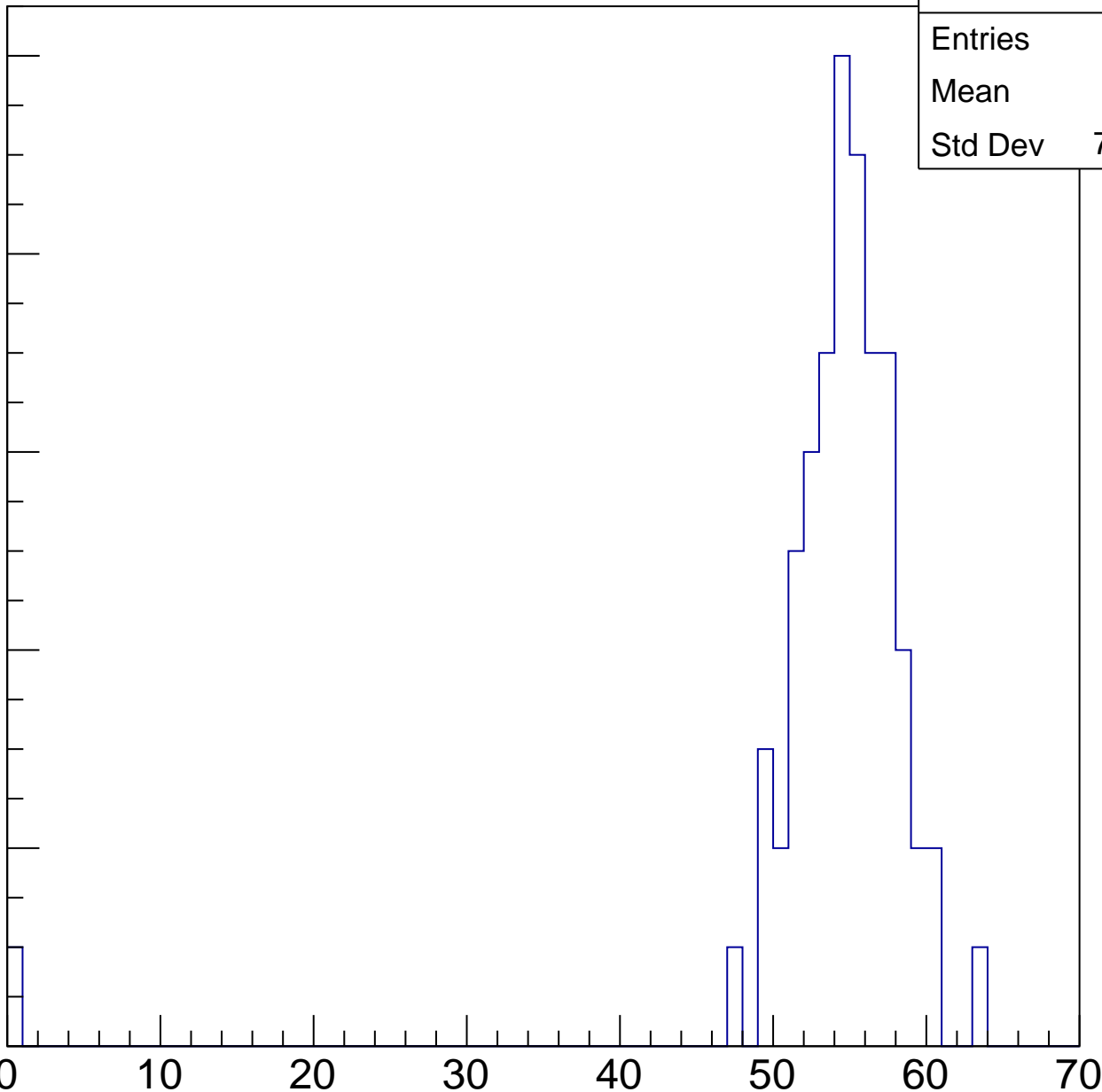
30

40

50

60

ampl



B1L103S, U9-ch108, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

7

6

5

4

3

2

1

0

Entries

44

Mean

59.52

Std Dev

2.35

ampl

0

10

20

30

40

50

60

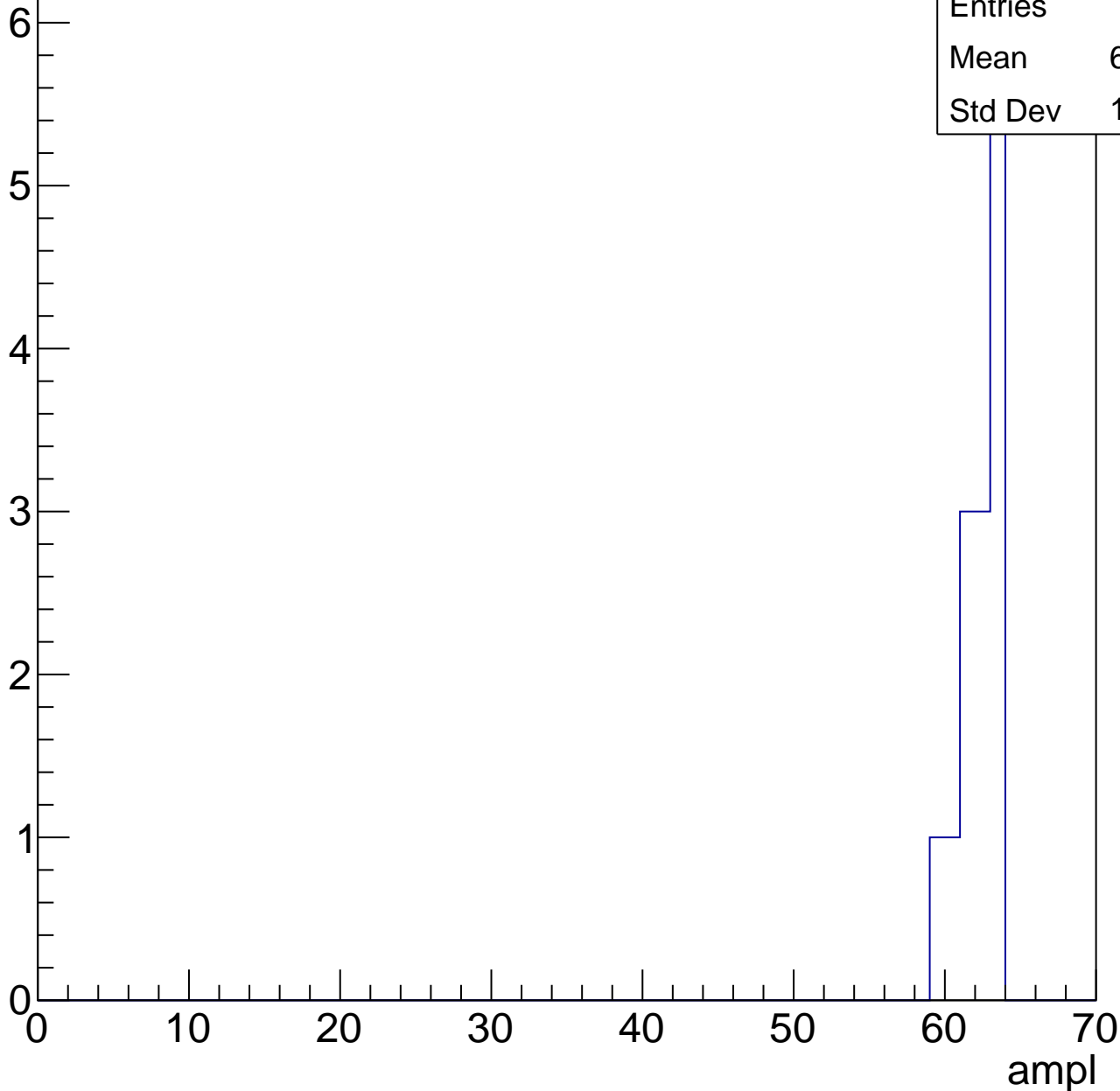
70

B1L103S, U9-ch108, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	14
Mean	61.86
Std Dev	1.245

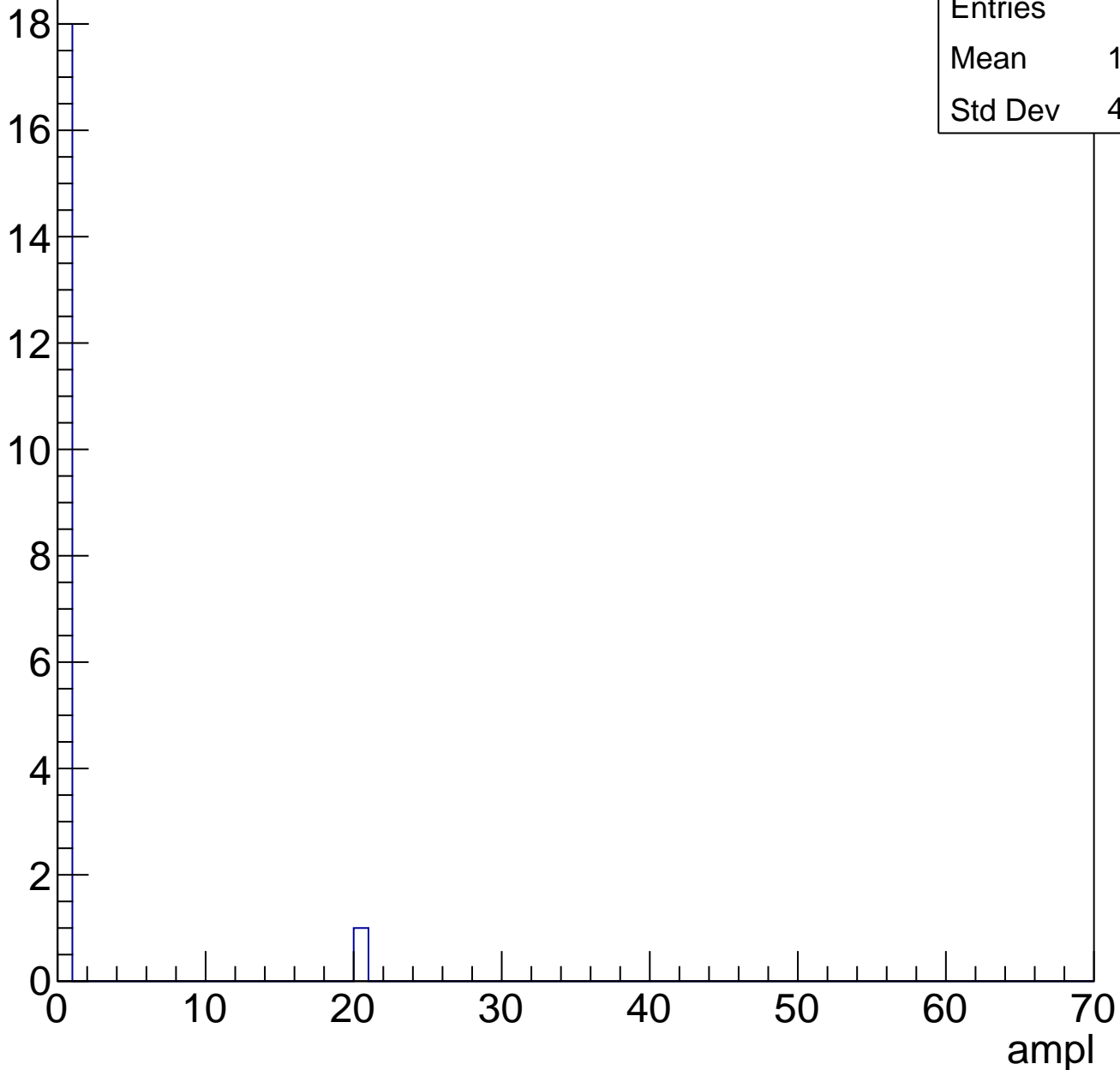


B1L103S, U9-ch108, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.053
Std Dev	4.466

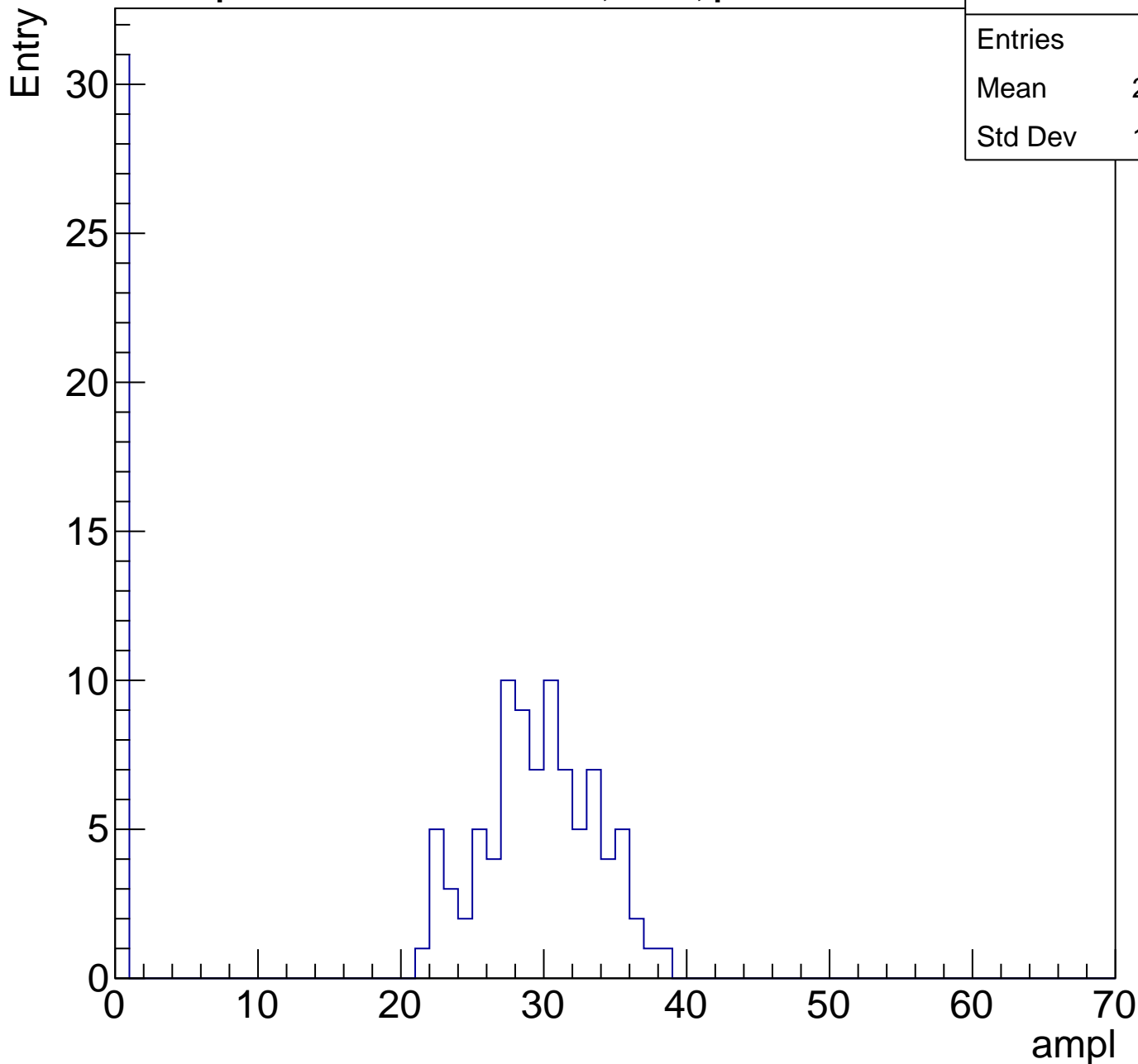
Entry



B1L103S, U9-ch109, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	119
Mean	21.58
Std Dev	13.24

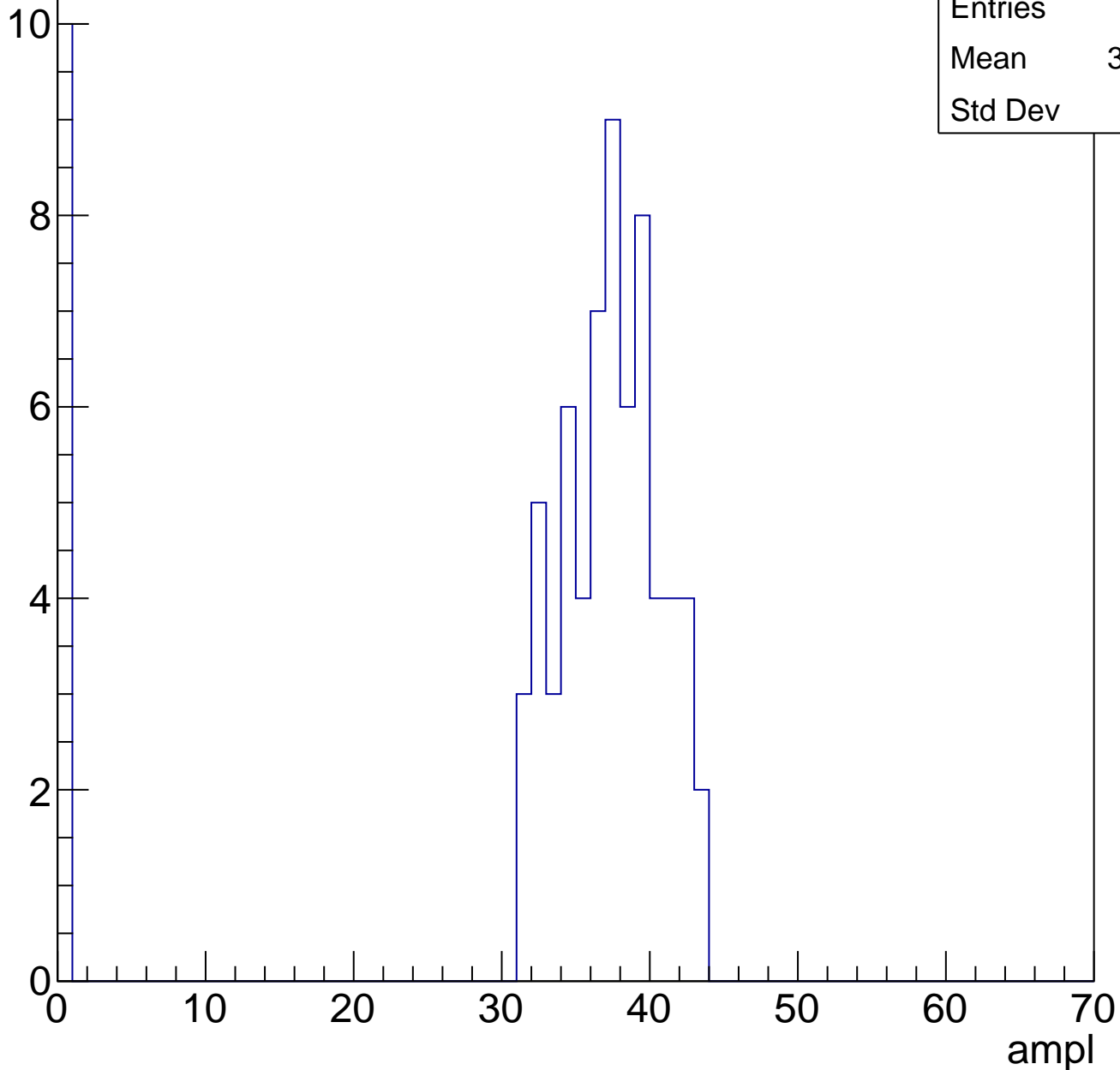


B1L103S, U9-ch109, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	31.99
Std Dev	12.9

Entry

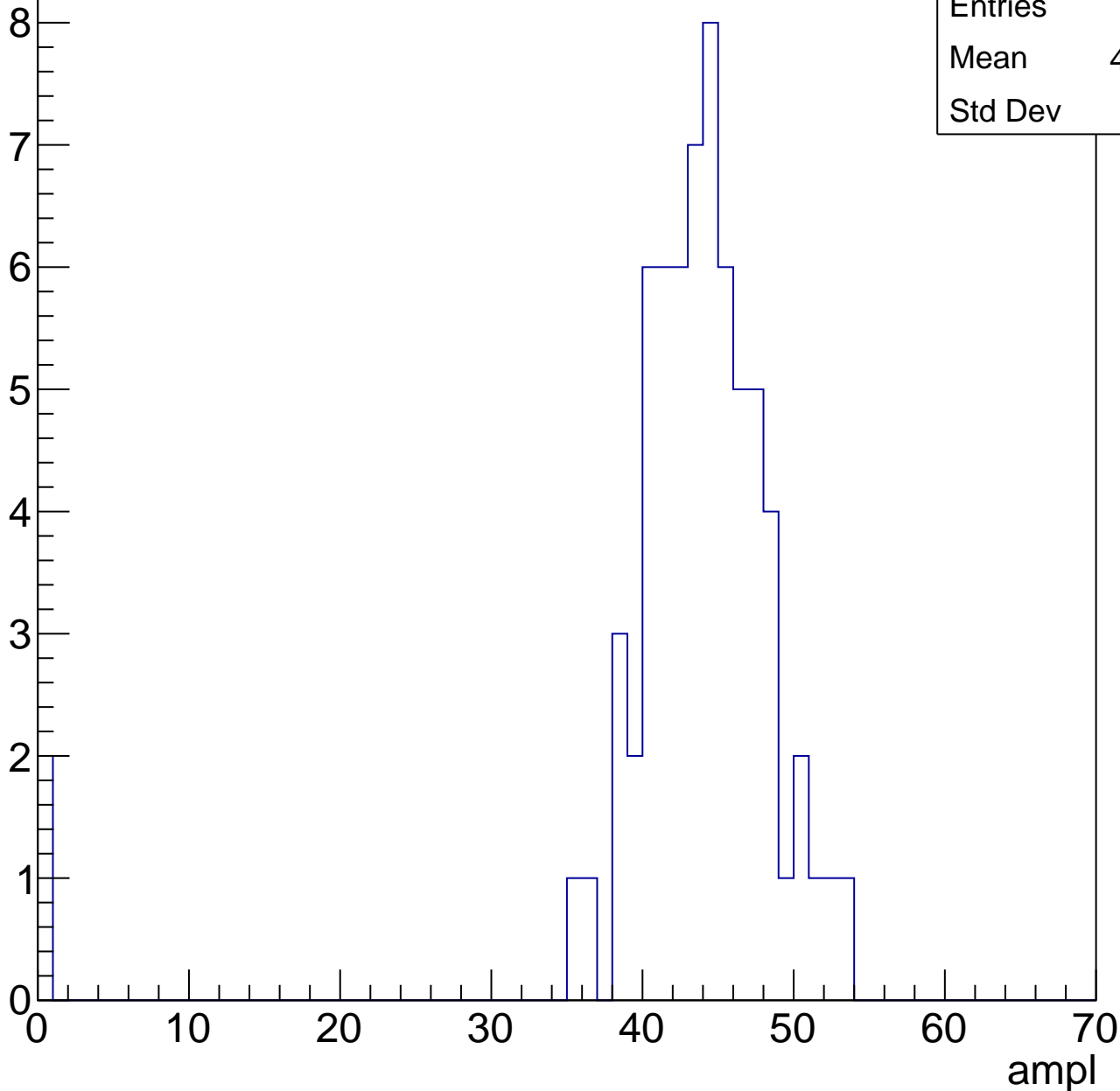


B1L103S, U9-ch109, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	42.44
Std Dev	8.24

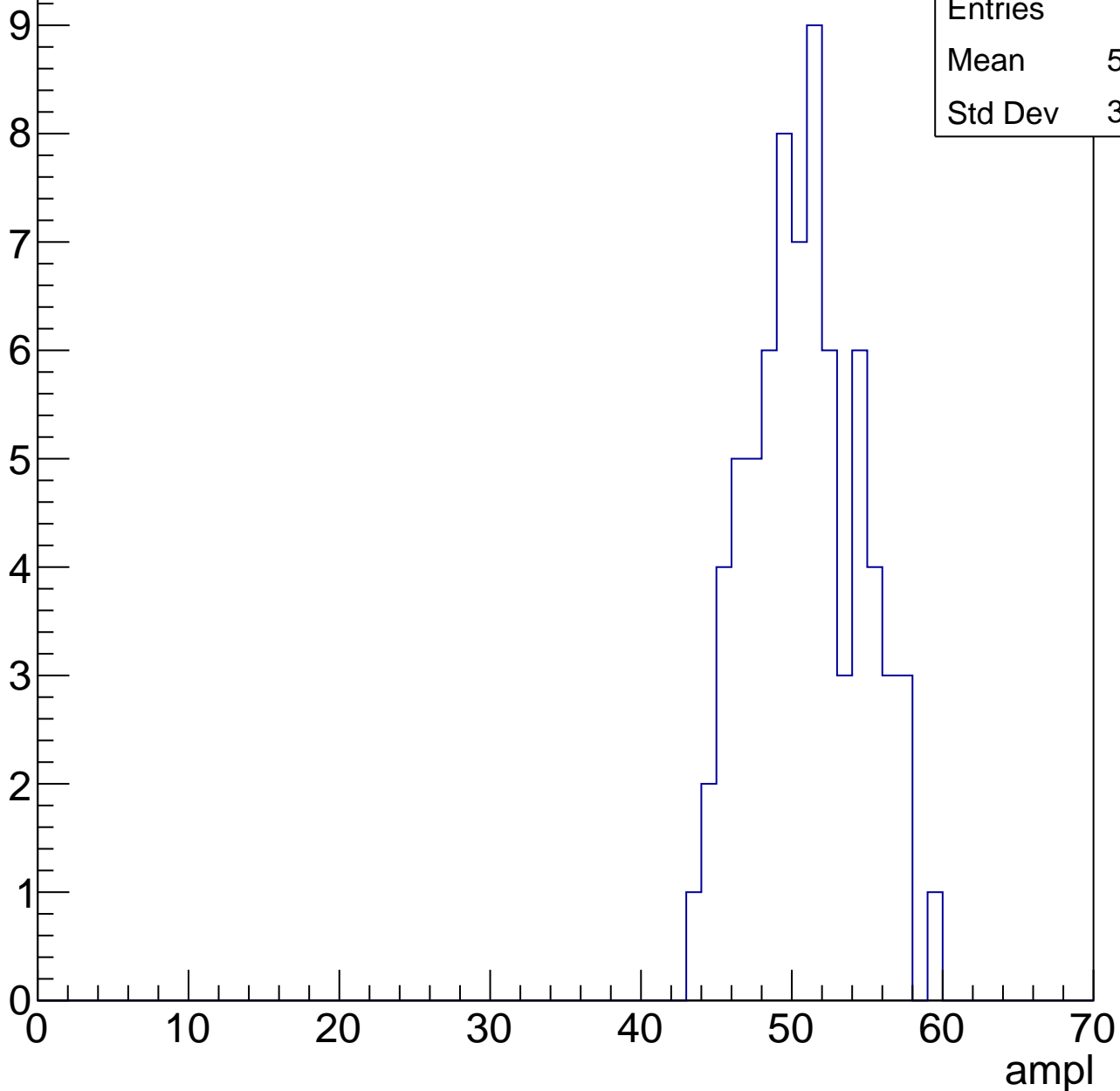


B1L103S, U9-ch109, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	50.38
Std Dev	3.625

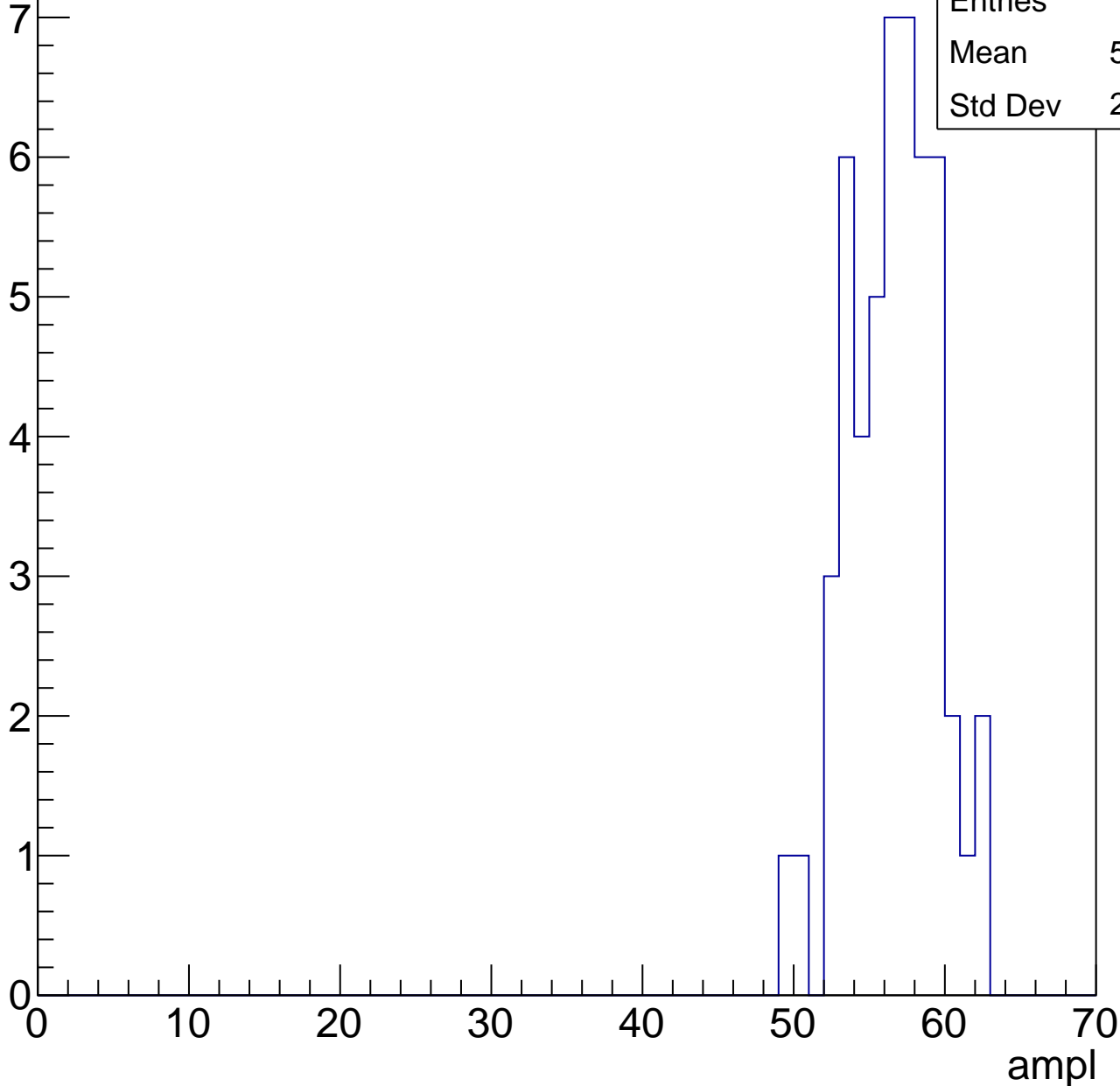


B1L103S, U9-ch109, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	56.12
Std Dev	2.874

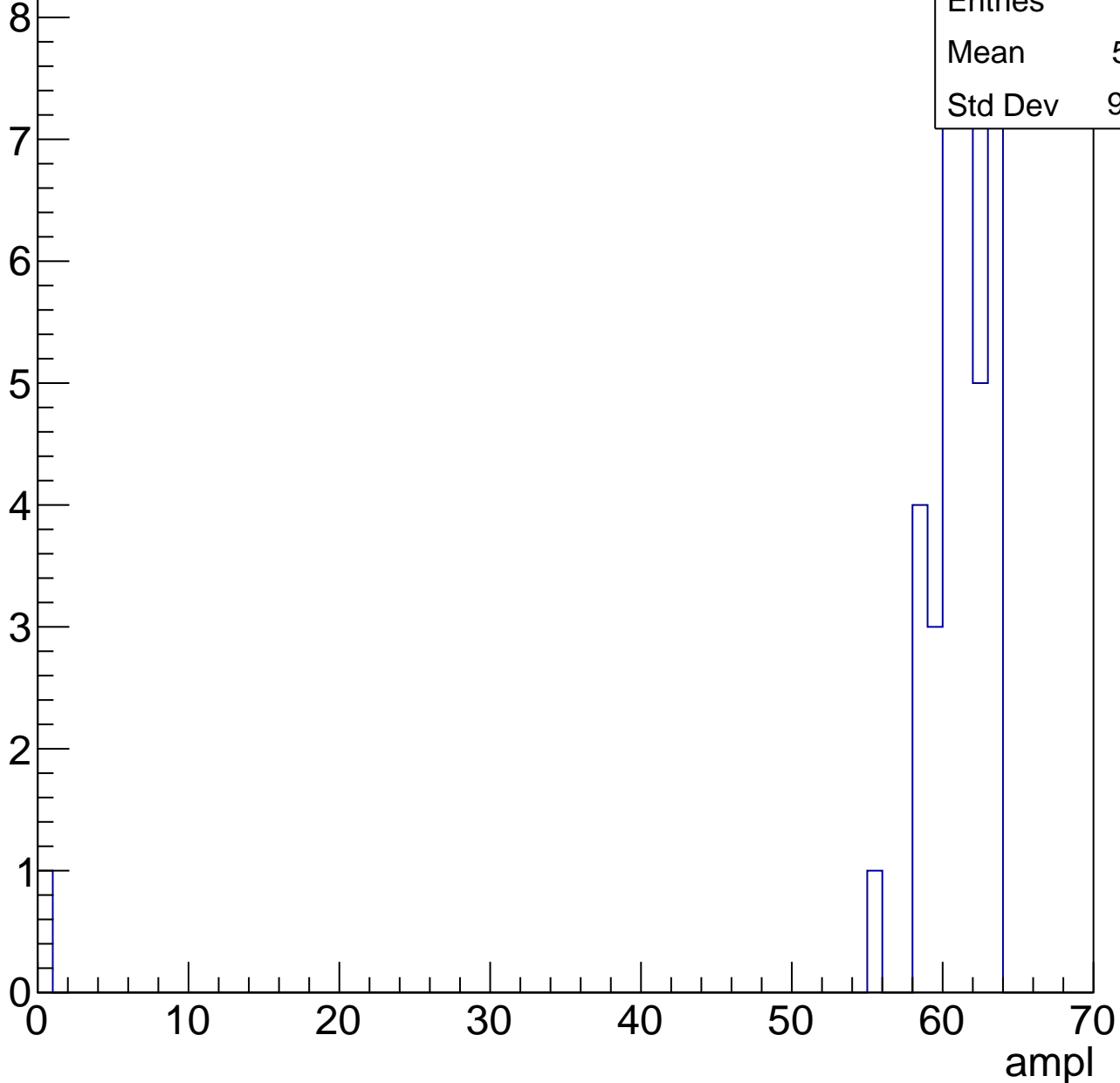


B1L103S, U9-ch109, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	38
Mean	59.11
Std Dev	9.886



B1L103S, U9-ch109, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

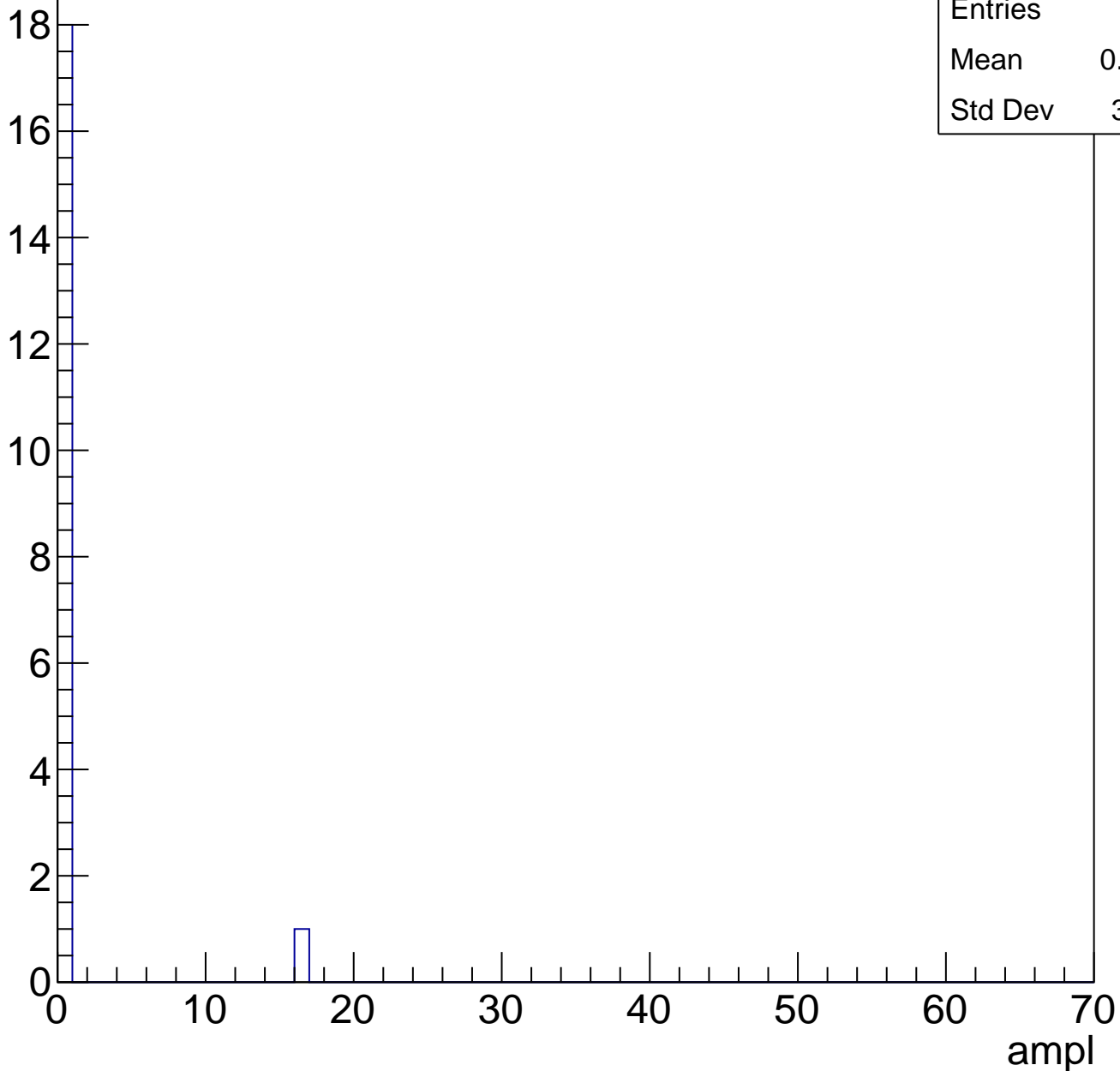


B1L103S, U9-ch109, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	0.8421
Std Dev	3.573

Entry

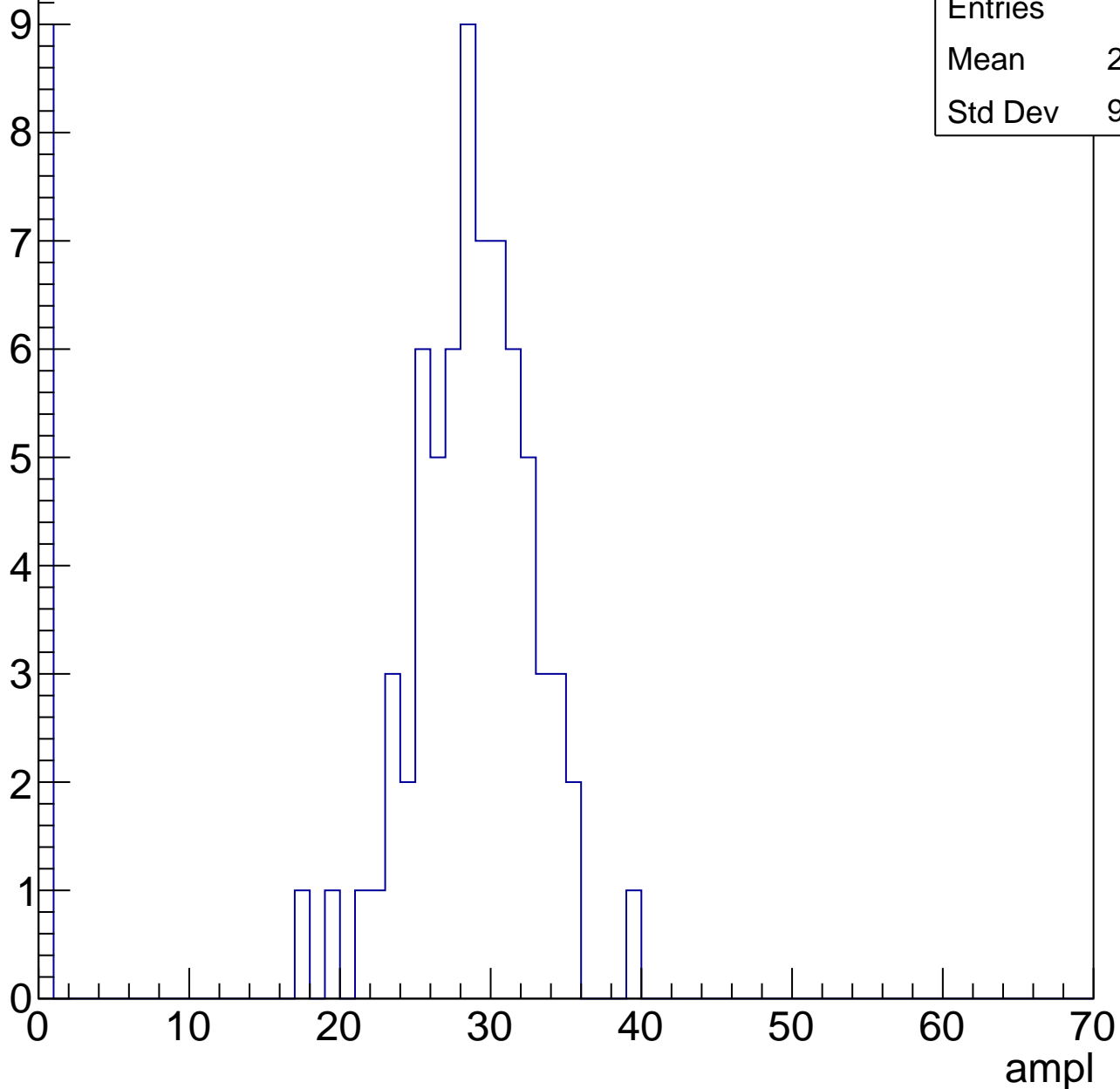


B1L103S, U9-ch110, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	25.12
Std Dev	9.774

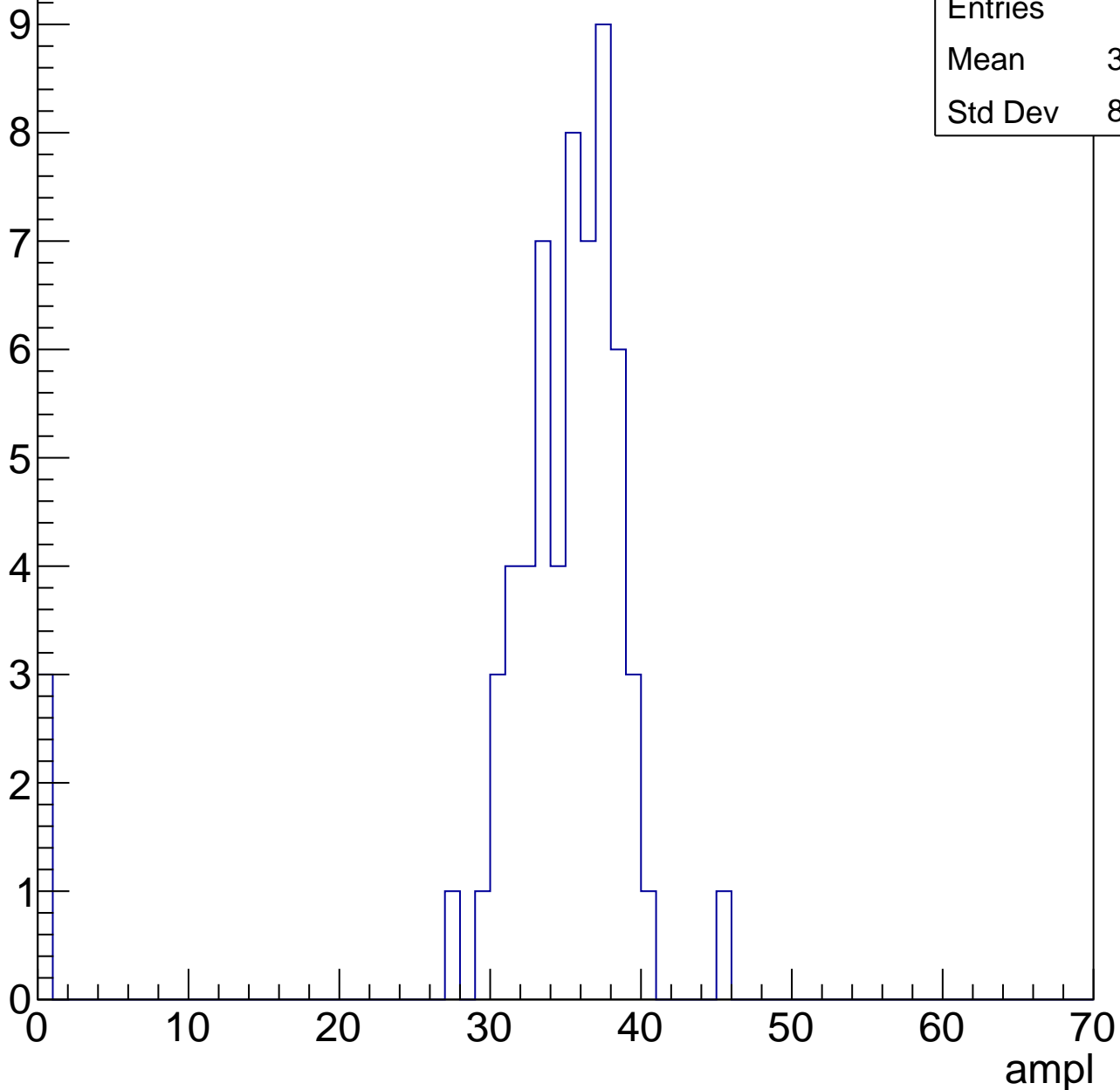


B1L103S, U9-ch110, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

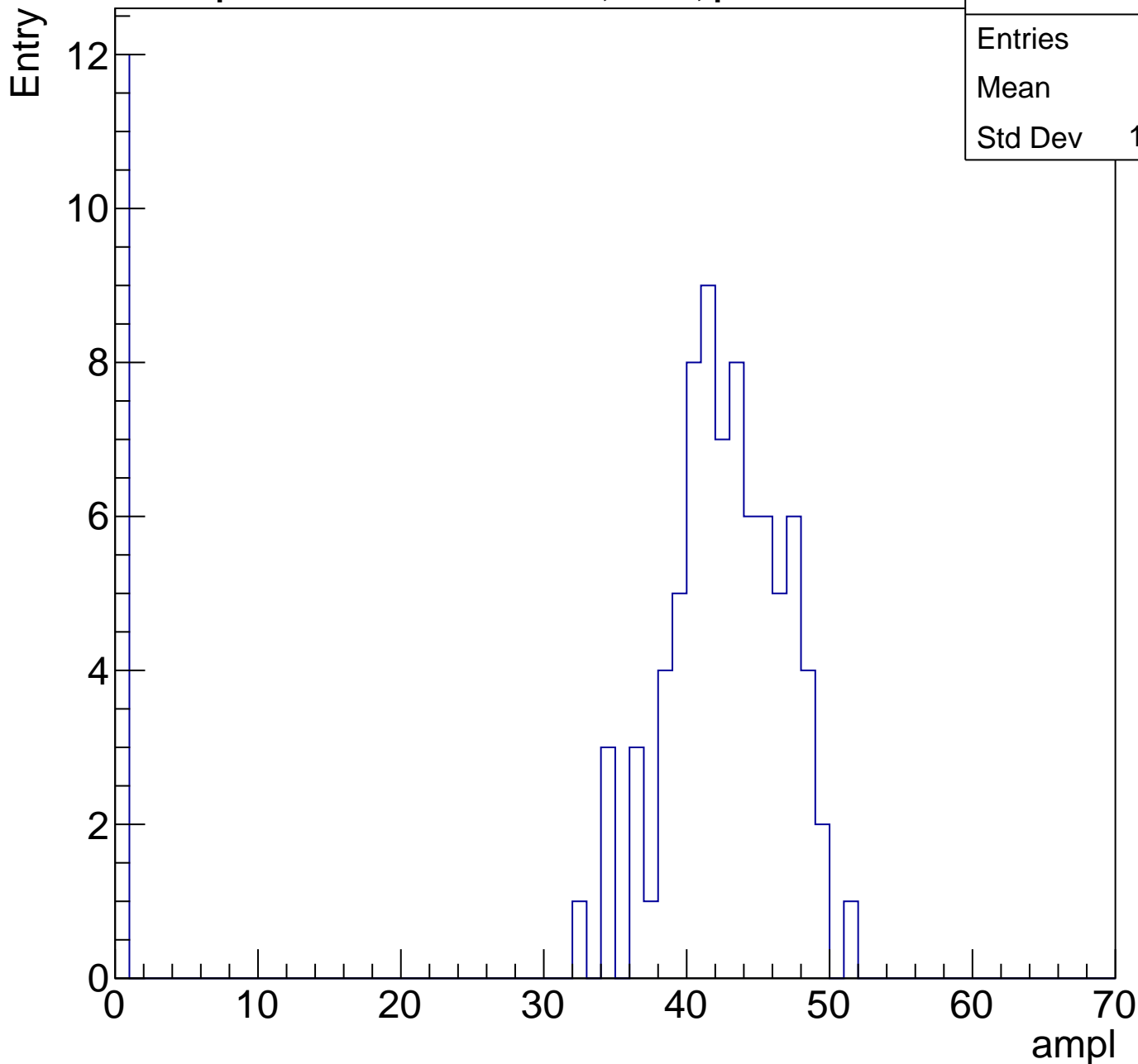
Entries	62
Mean	33.23
Std Dev	8.089



B1L103S, U9-ch110, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	91
Mean	36.7
Std Dev	14.76

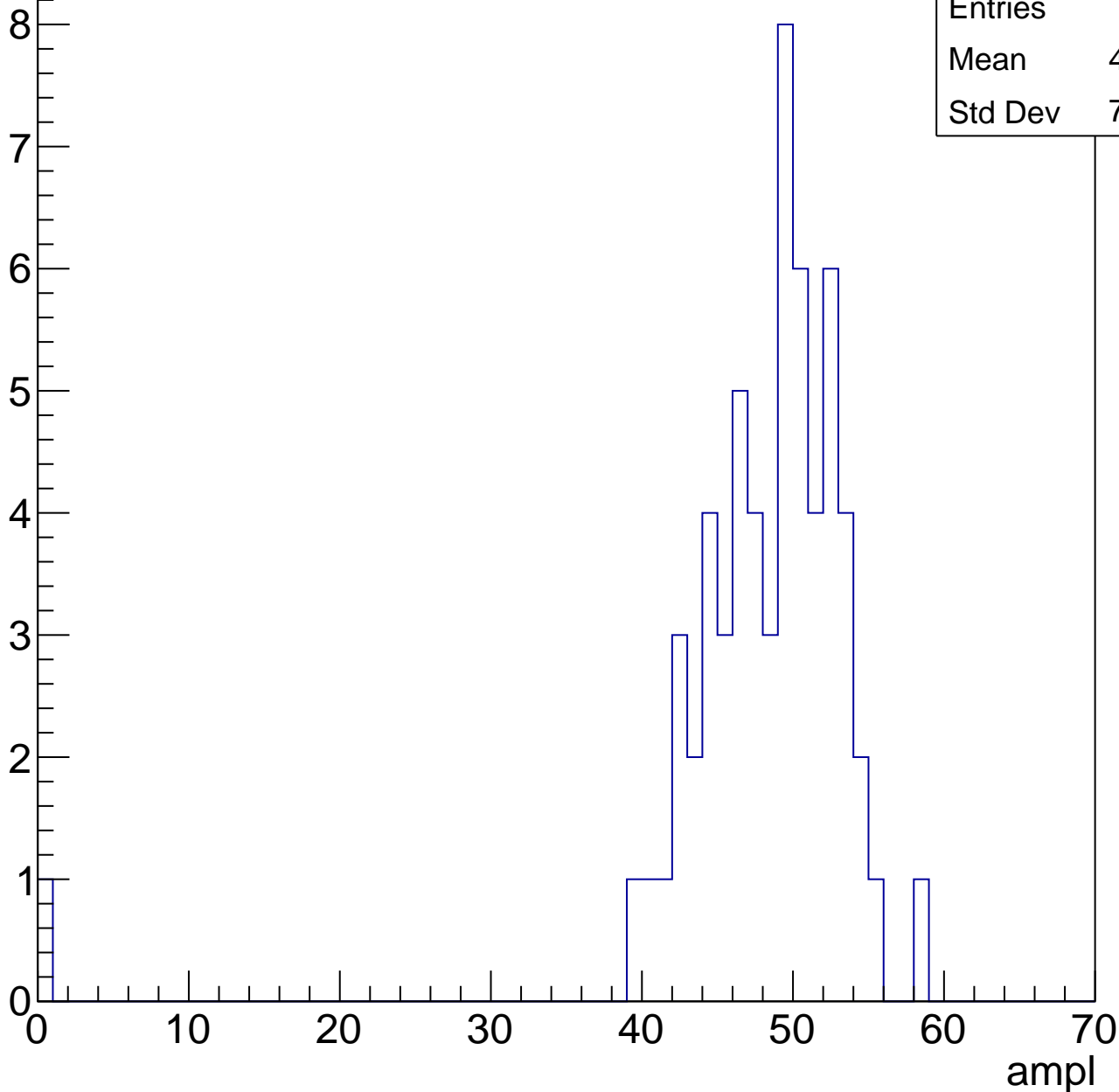


B1L103S, U9-ch110, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	47.43
Std Dev	7.345

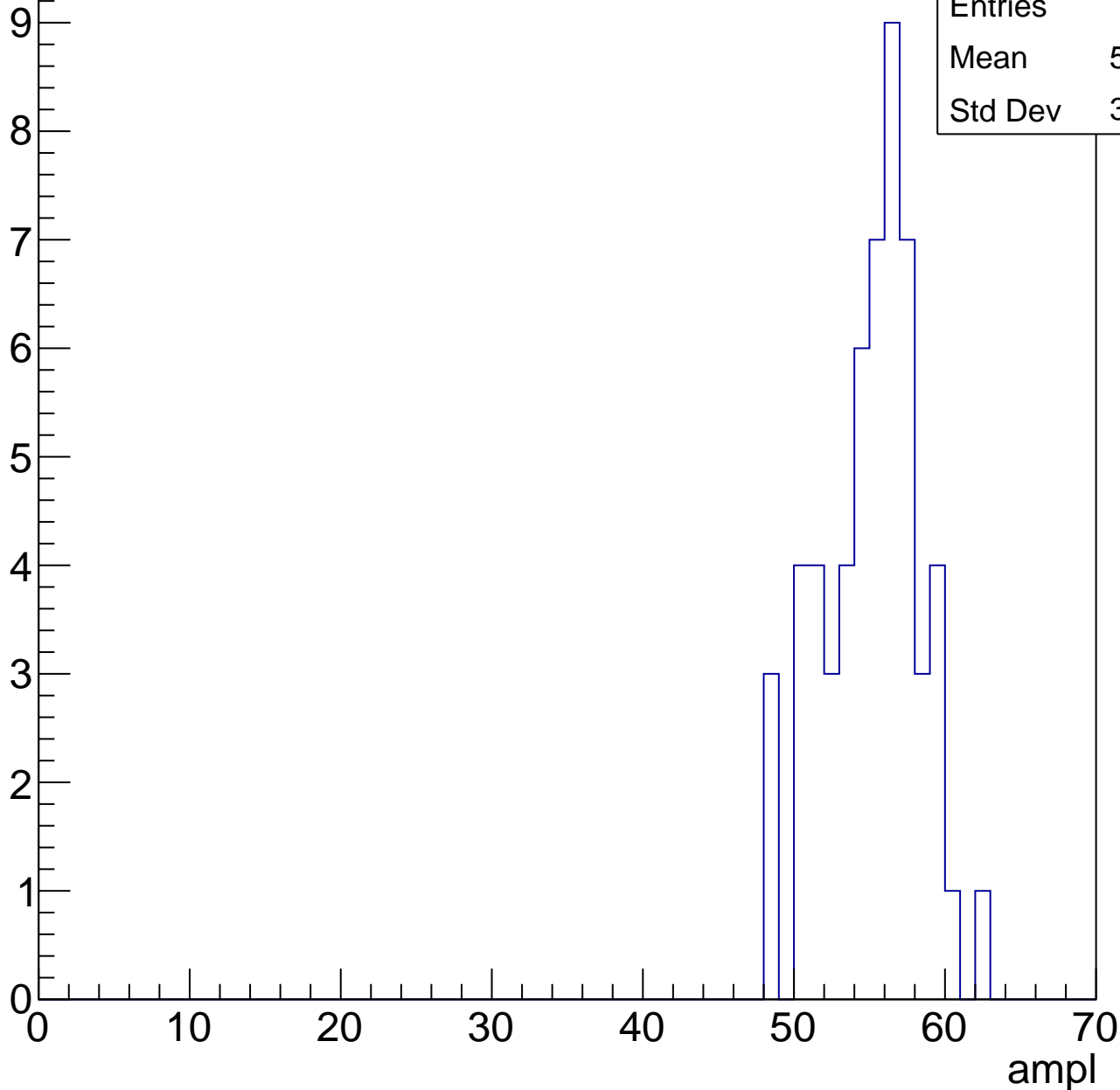


B1L103S, U9-ch110, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	54.64
Std Dev	3.148

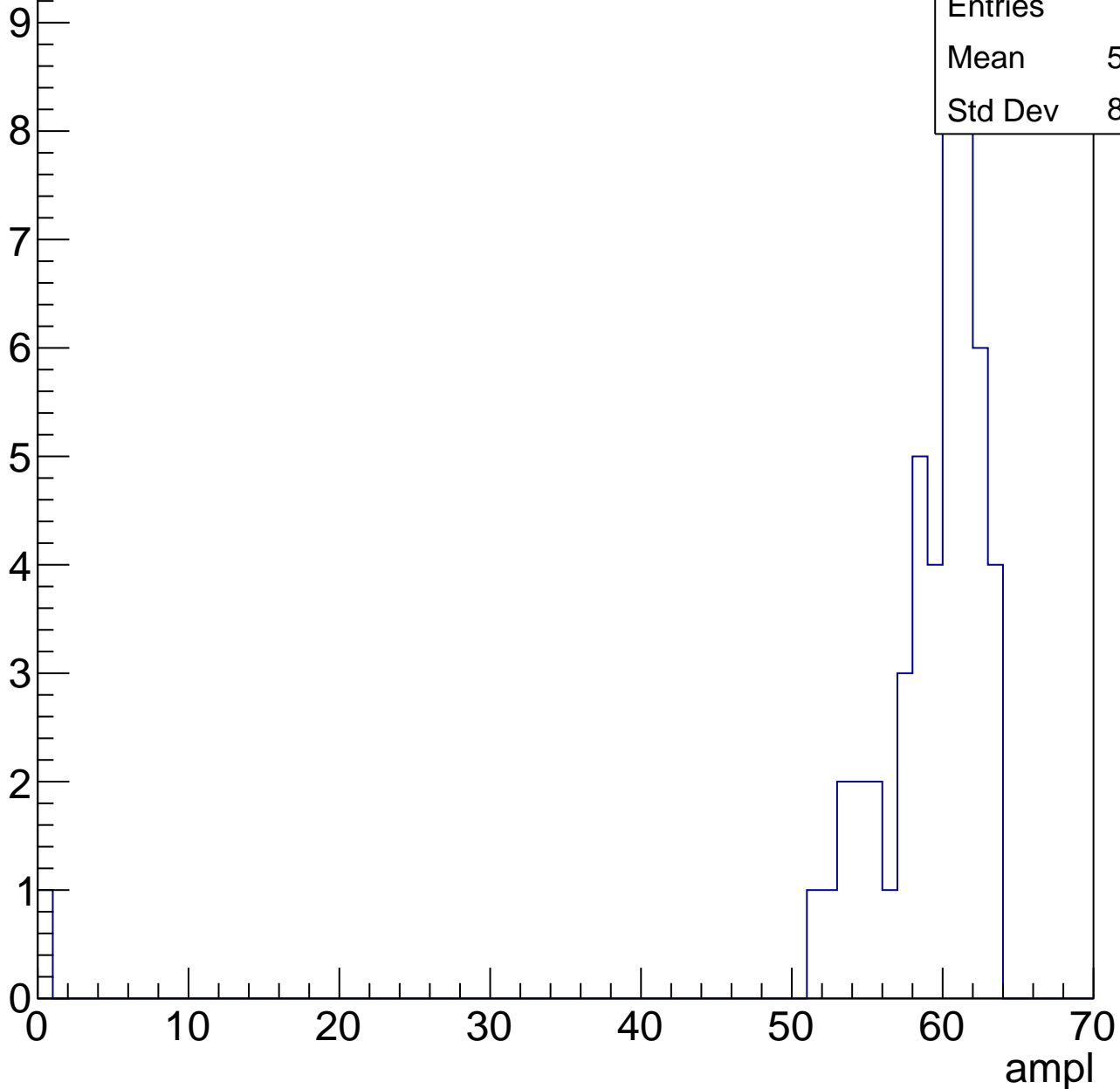


B1L103S, U9-ch110, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	57.82
Std Dev	8.884

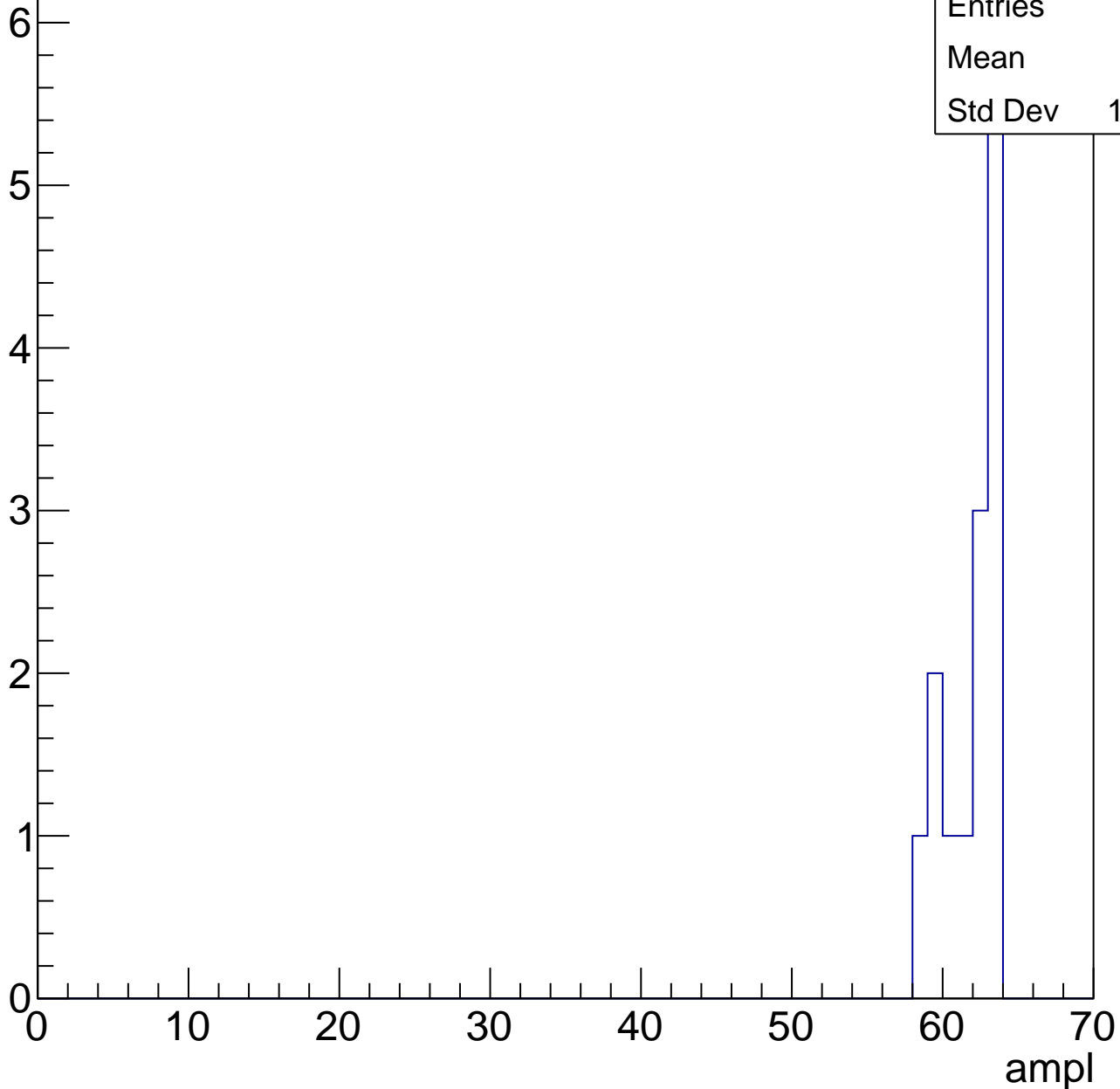


B1L103S, U9-ch110, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	14
Mean	61.5
Std Dev	1.722



B1L103S, U9-ch110, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

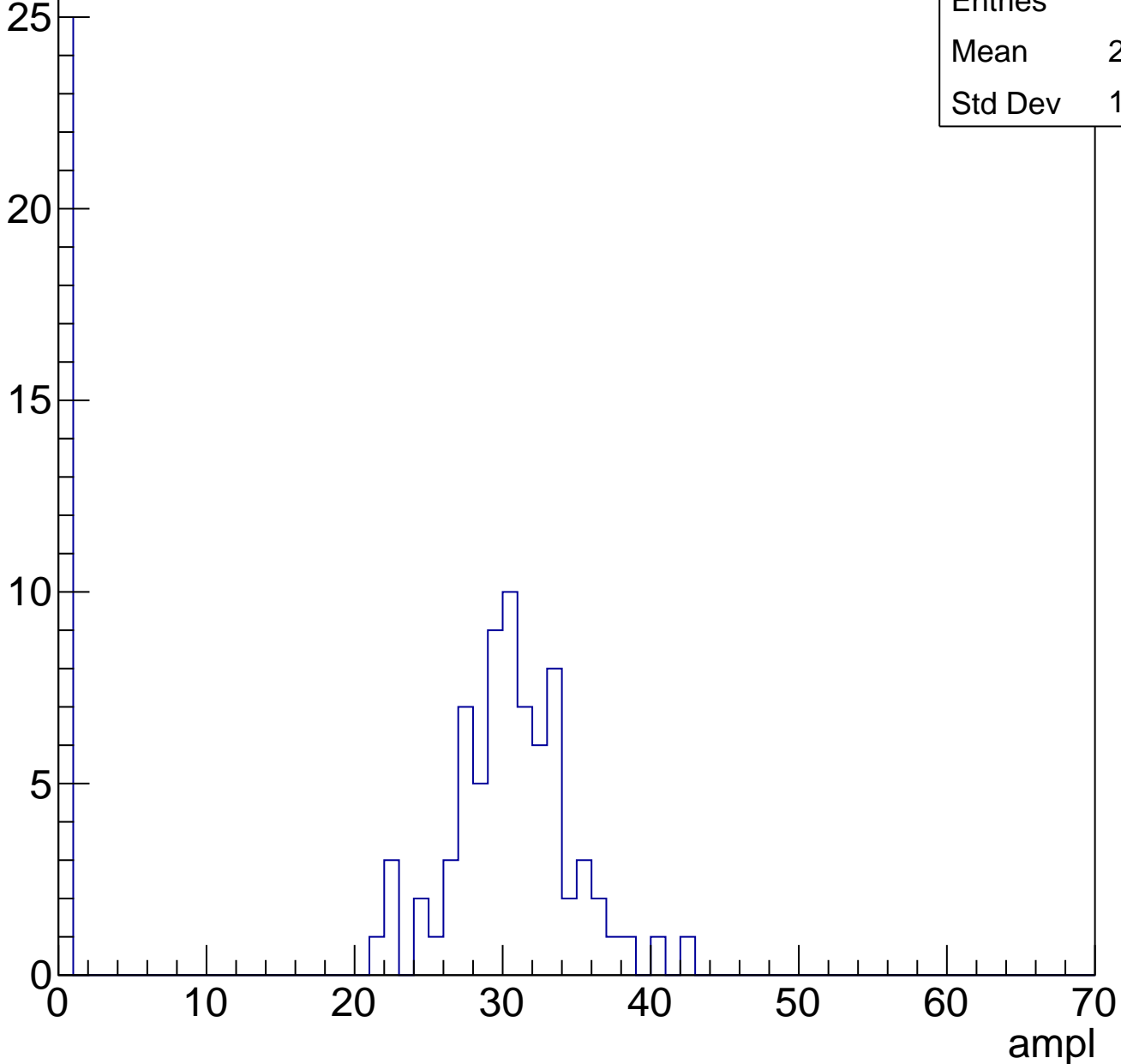
Entries	19
Mean	0
Std Dev	0

B1L103S, U9-ch111, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	98
Mean	22.48
Std Dev	13.59

Entry

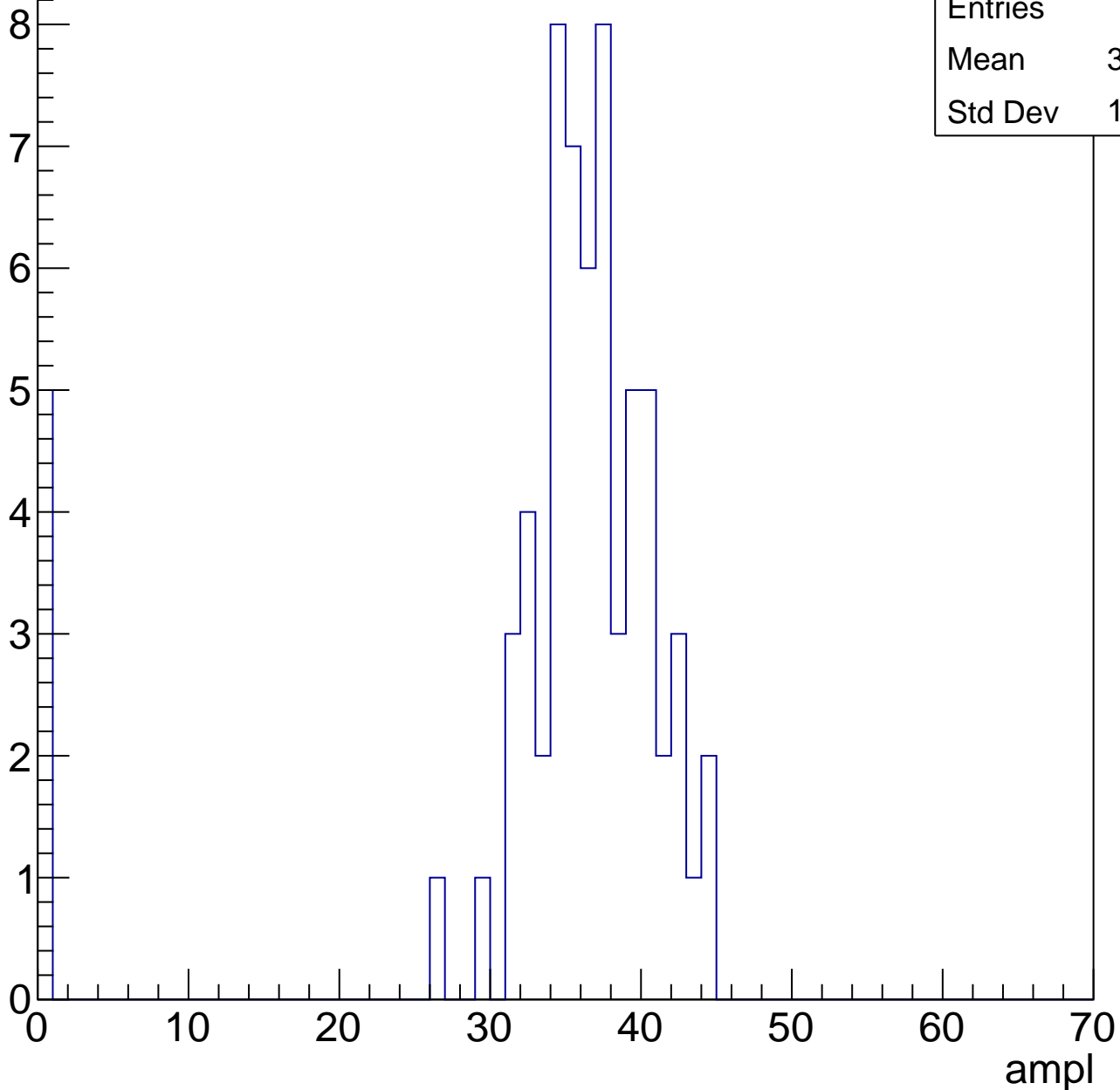


B1L103S, U9-ch111, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	33.62
Std Dev	10.25

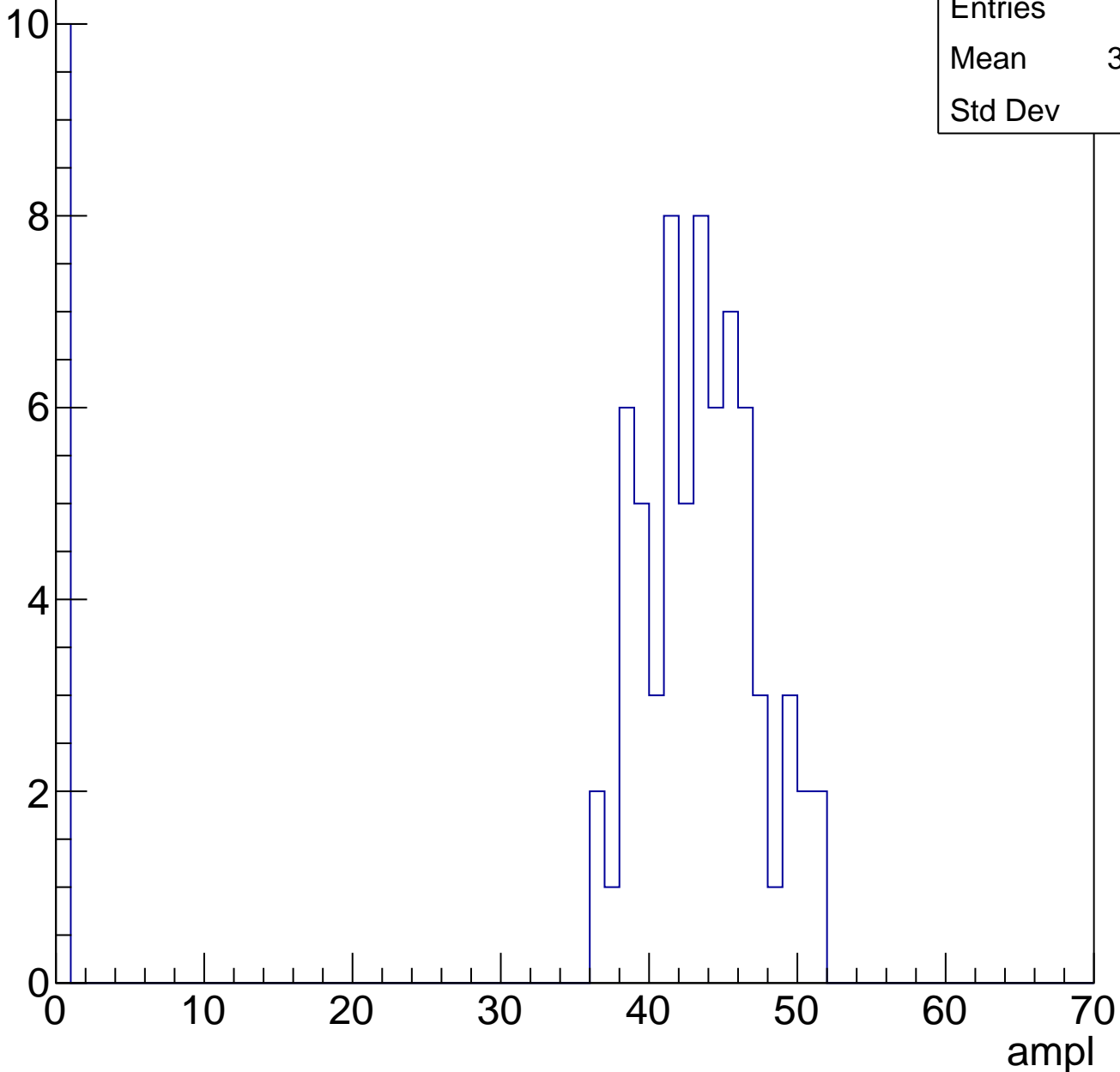


B1L103S, U9-ch111, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	78
Mean	37.53
Std Dev	14.8

Entry

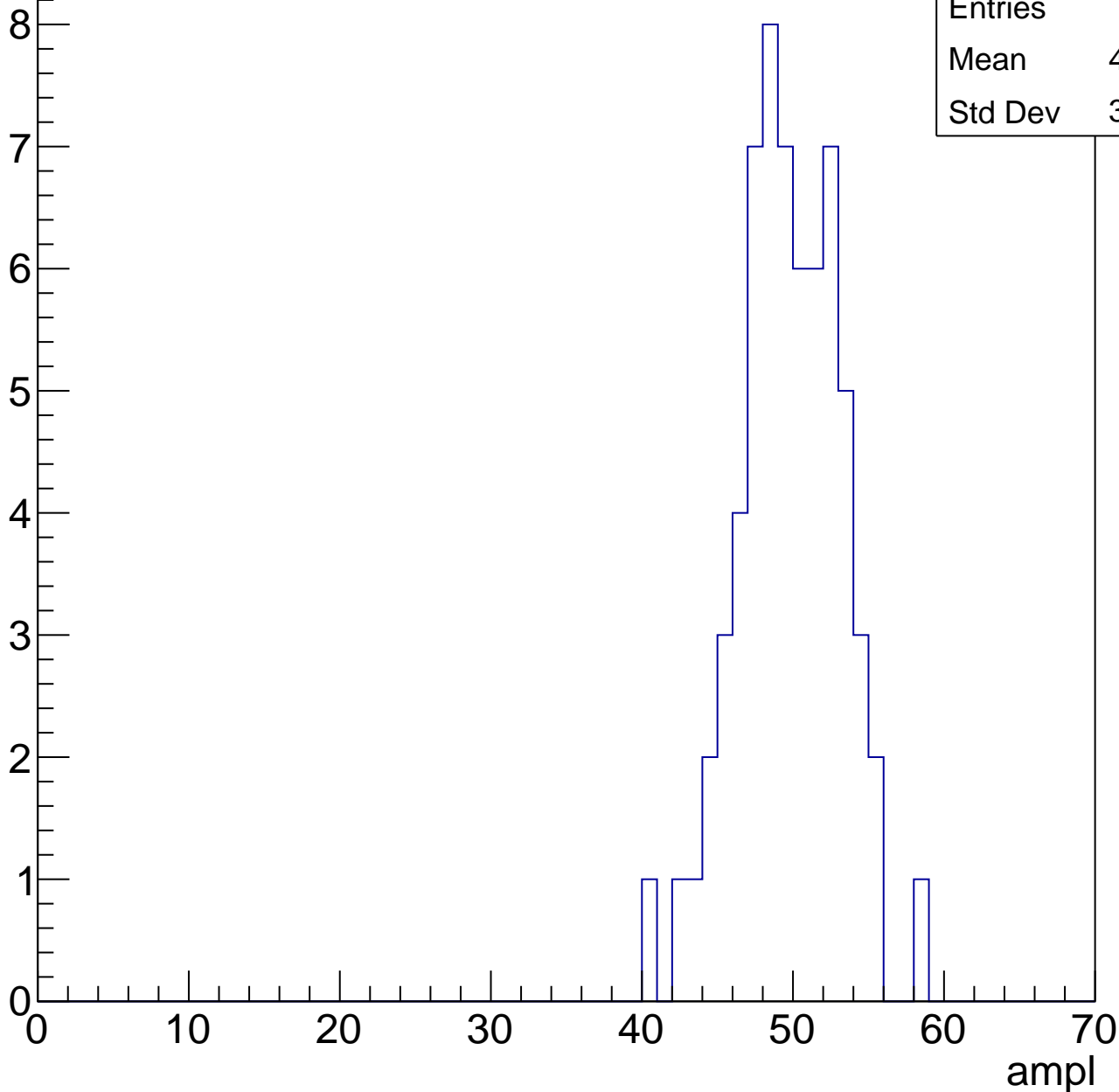


B1L103S, U9-ch111, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	49.27
Std Dev	3.383

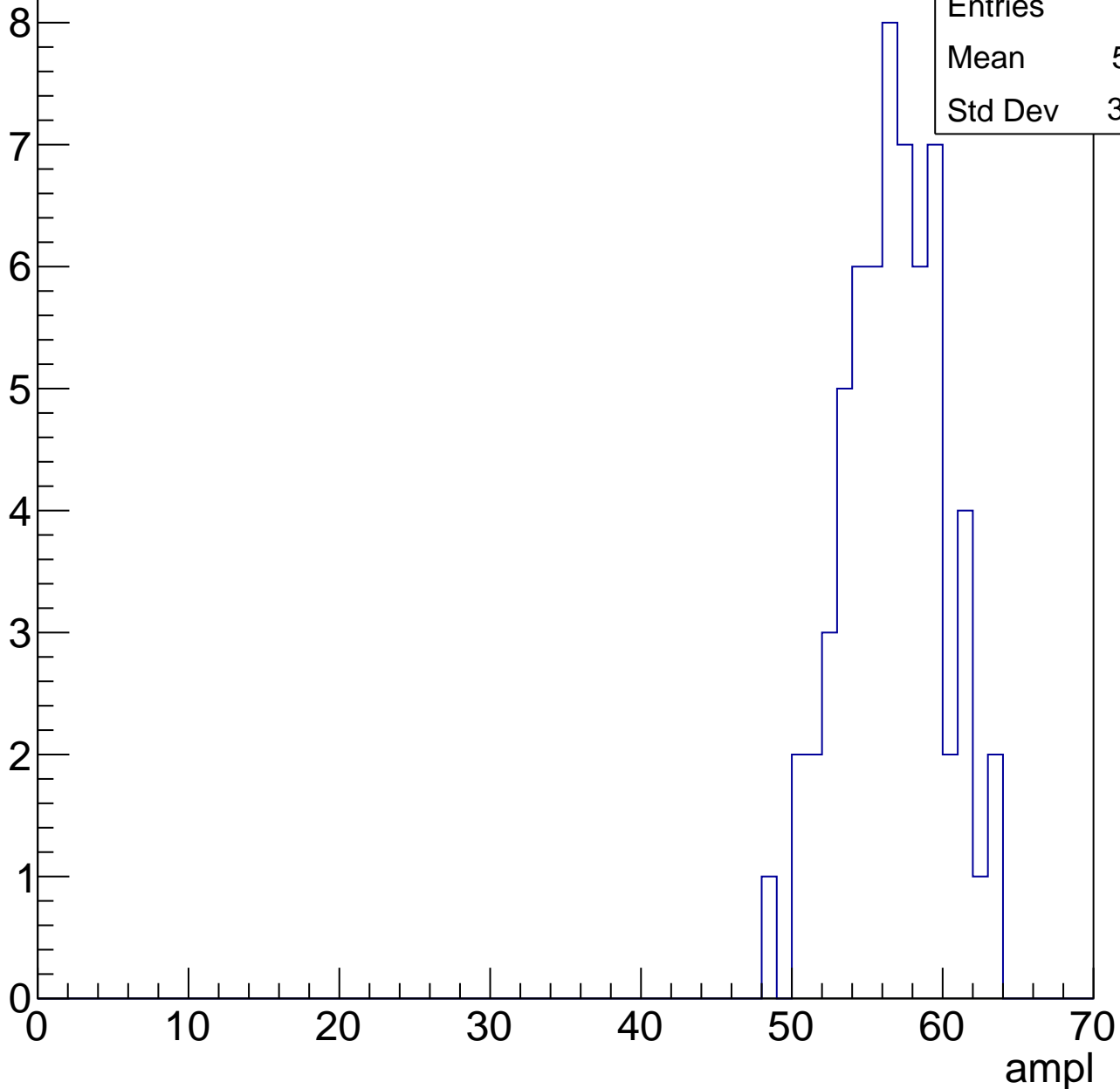


B1L103S, U9-ch111, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	56.21
Std Dev	3.278

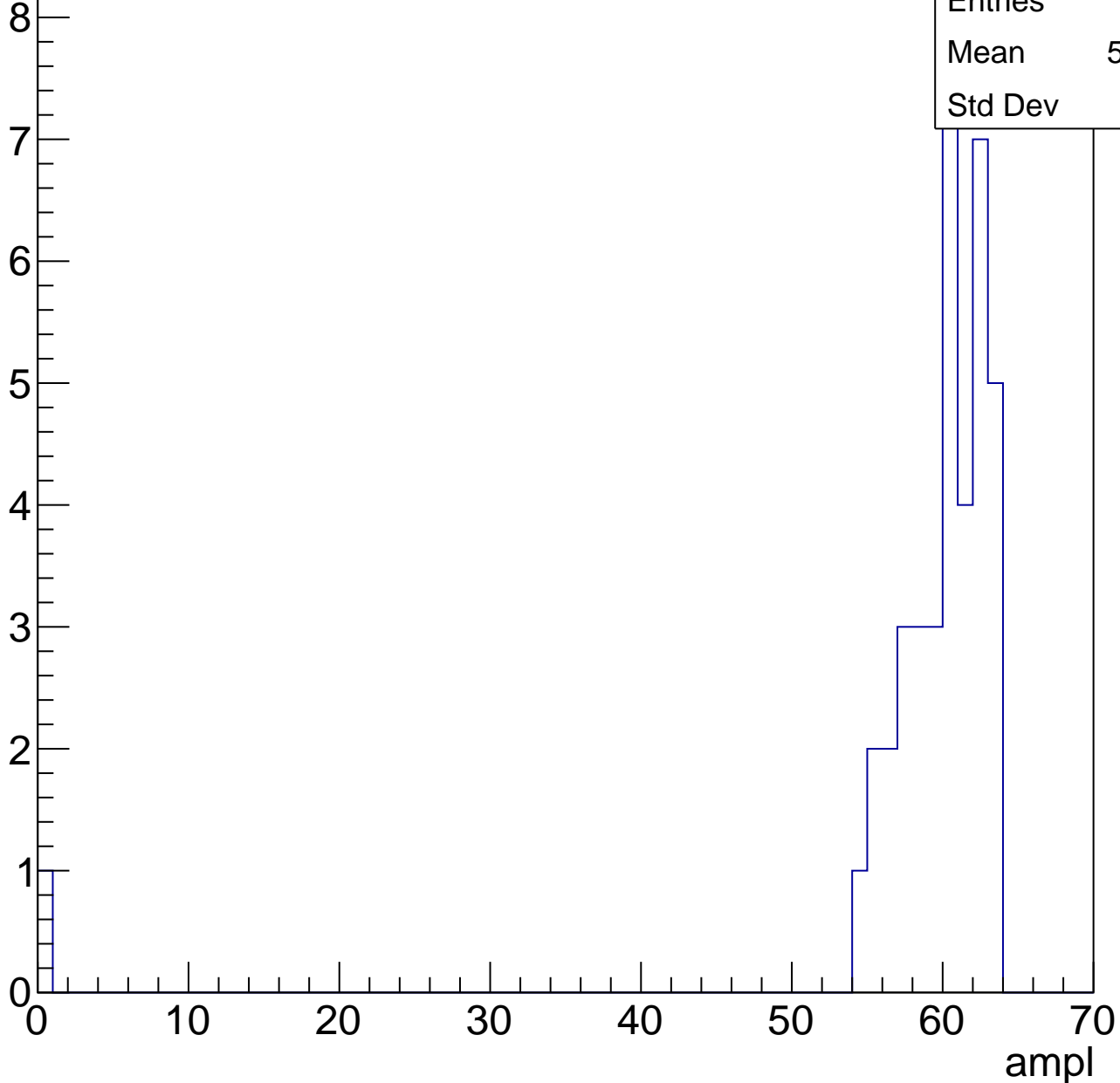


B1L103S, U9-ch111, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	58.23
Std Dev	9.76



B1L103S, U9-ch111, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch111, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

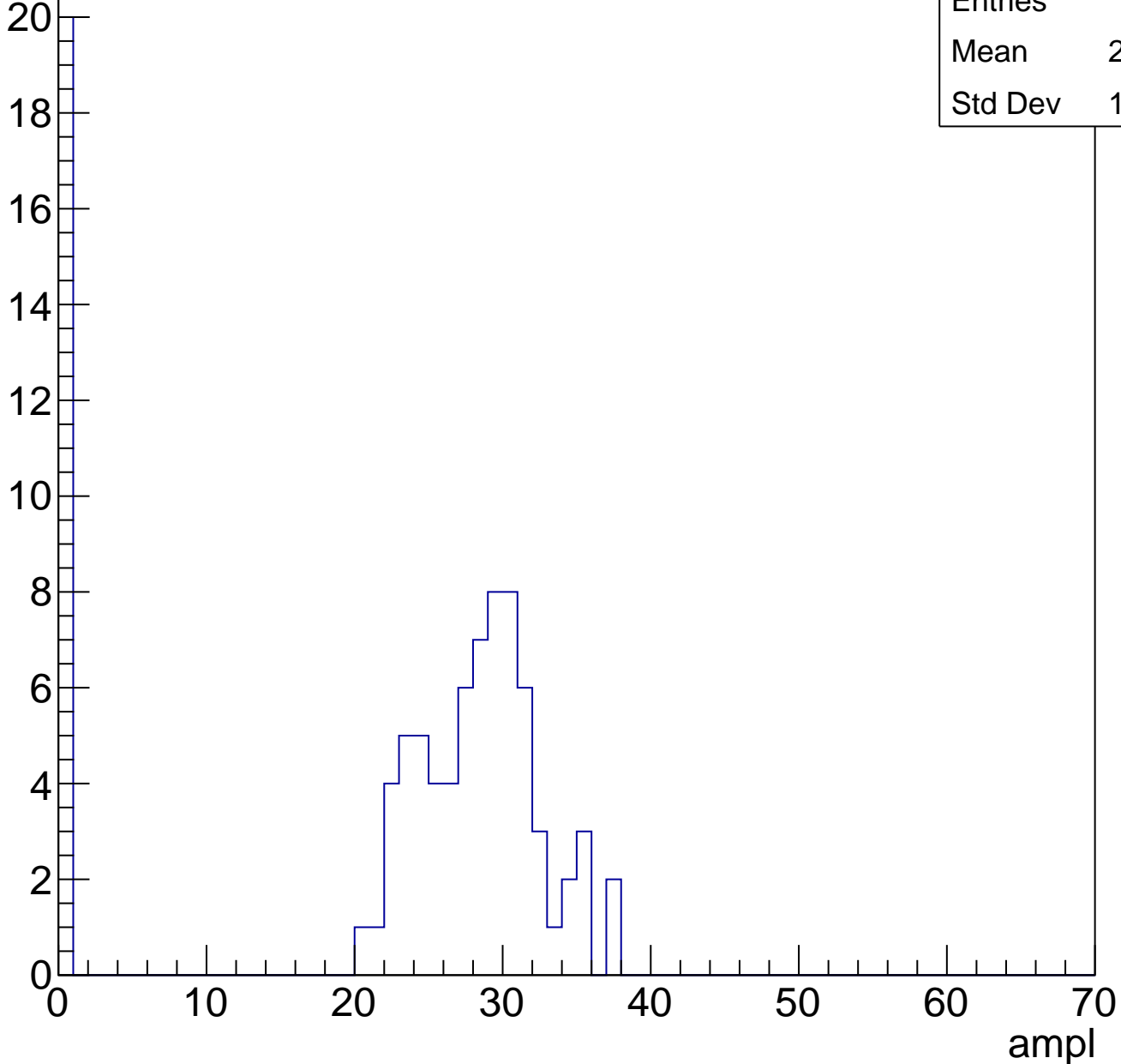


B1L103S, U9-ch112, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	90
Mean	21.78
Std Dev	12.14

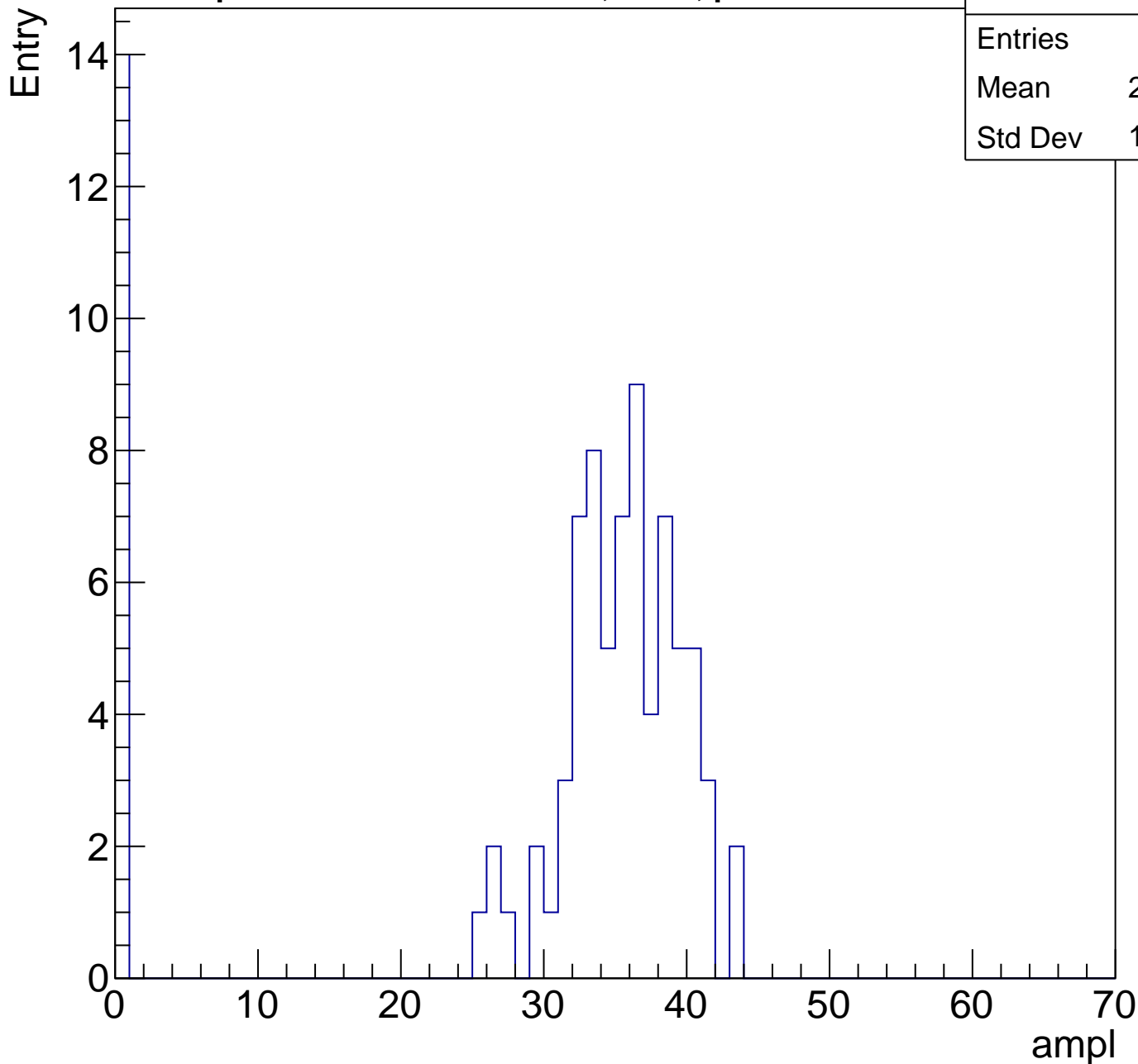
Entry



B1L103S, U9-ch112, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	86
Mean	29.42
Std Dev	13.46

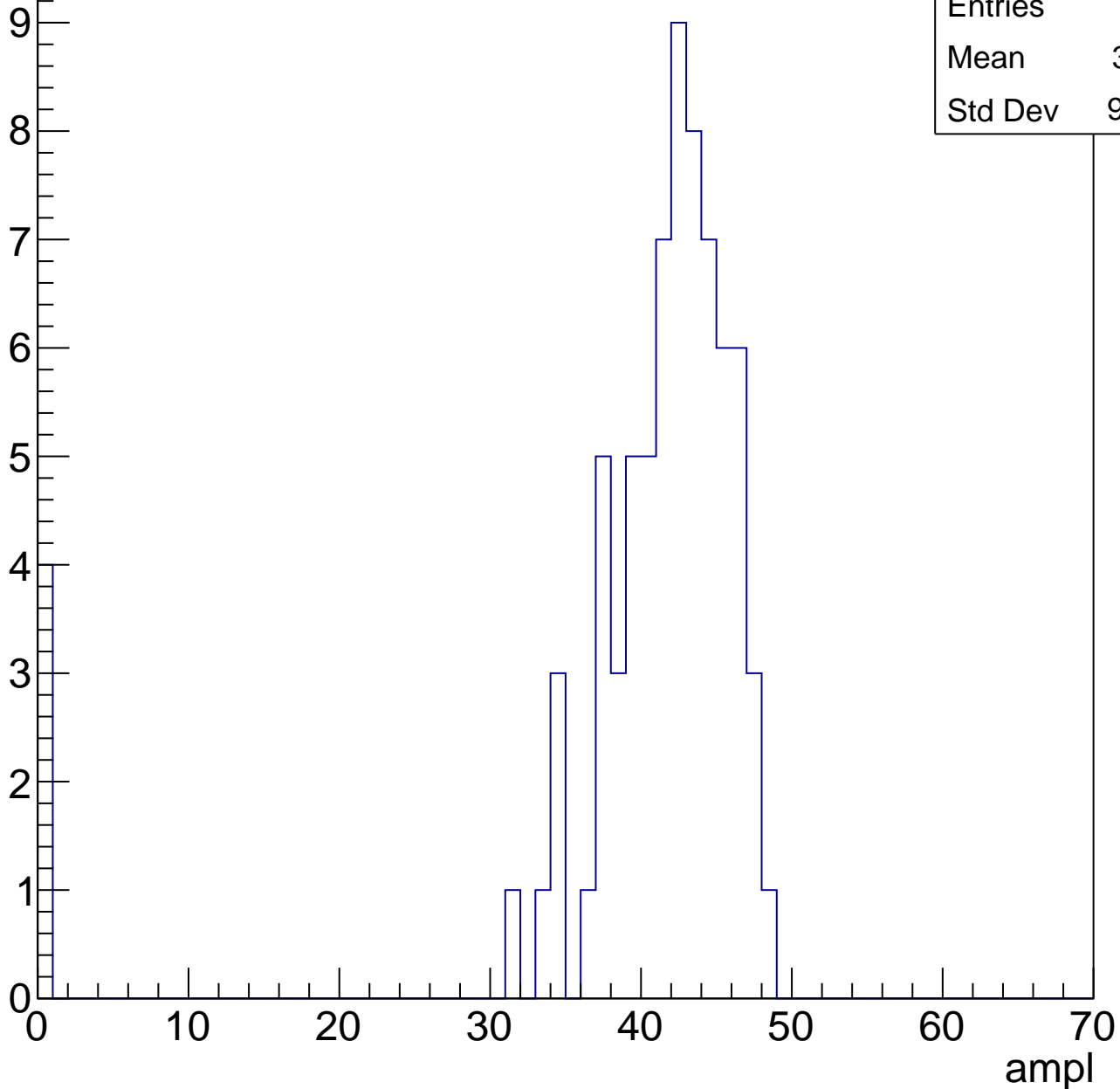


B1L103S, U9-ch112, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	39.31
Std Dev	9.989

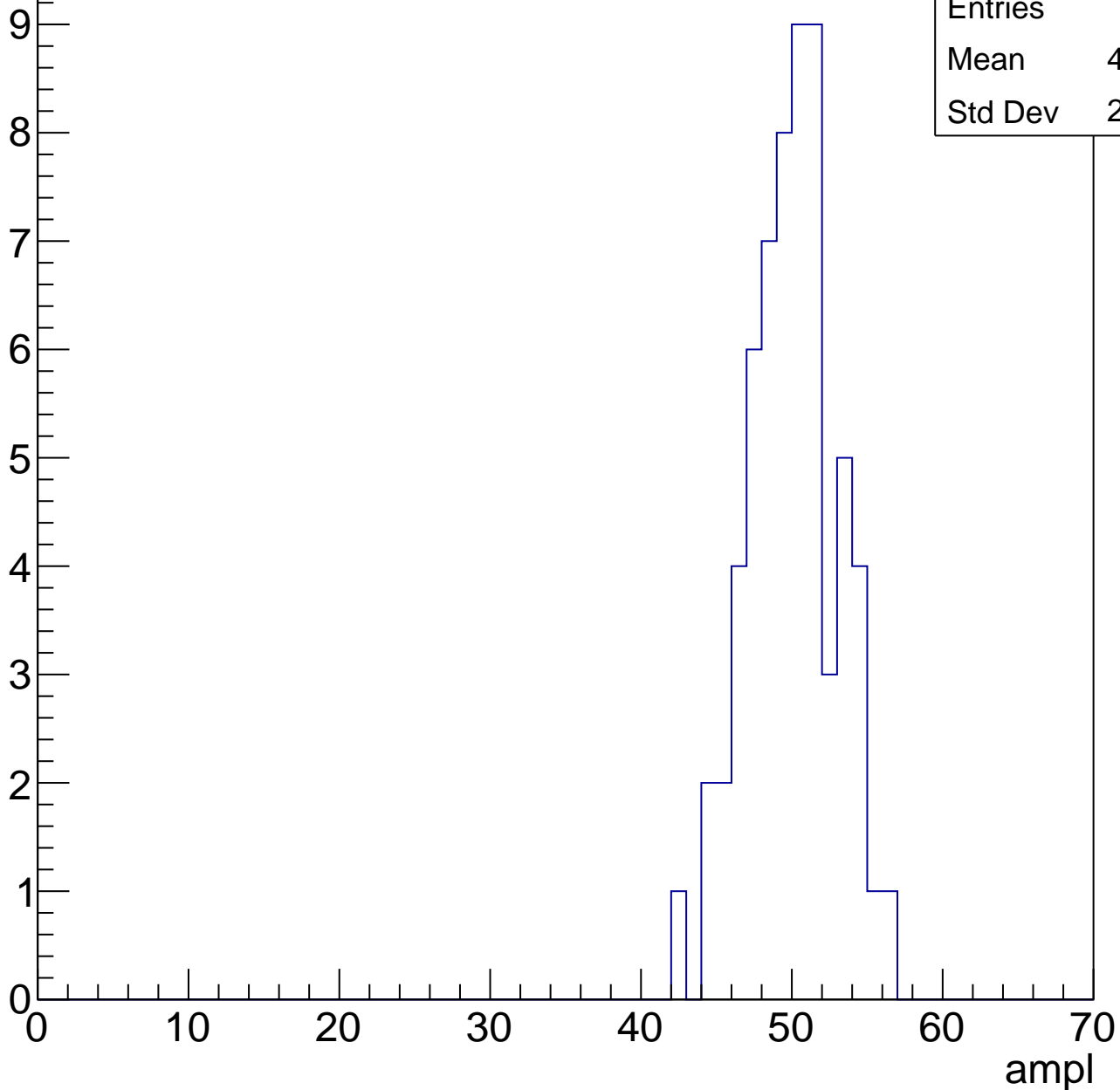


B1L103S, U9-ch112, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	49.53
Std Dev	2.889

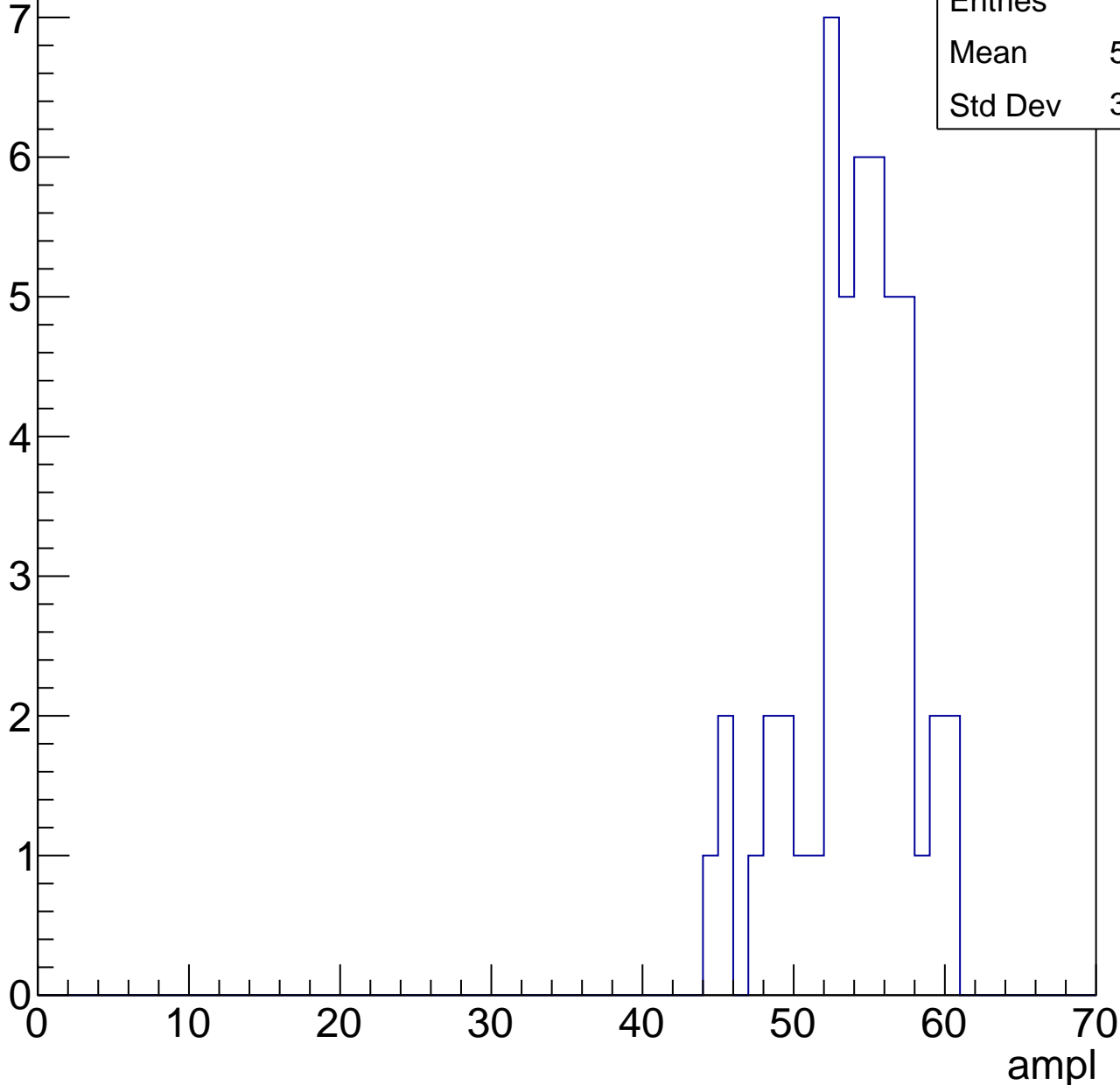


B1L103S, U9-ch112, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

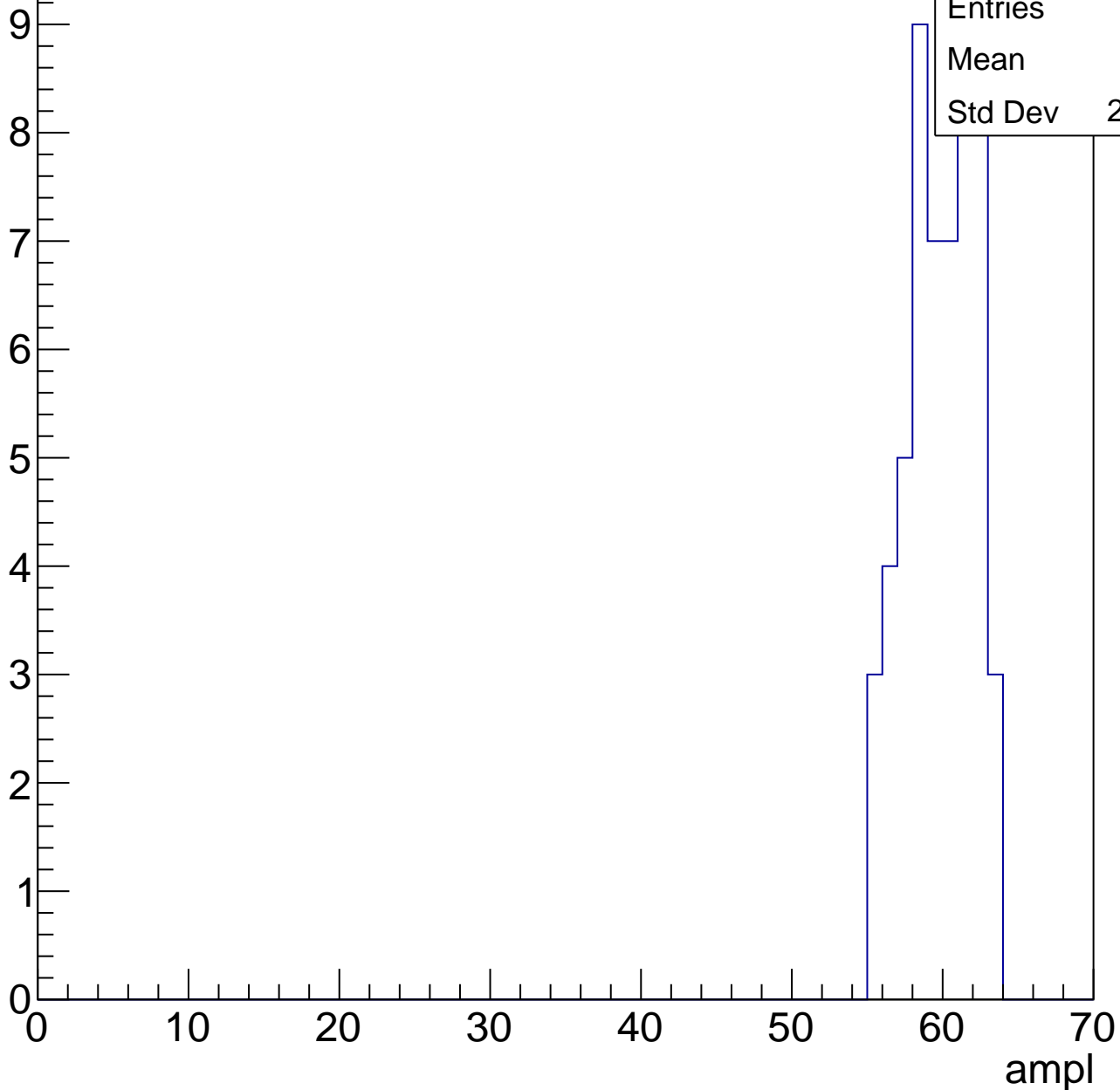
Entries	49
Mean	53.47
Std Dev	3.742



B1L103S, U9-ch112, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



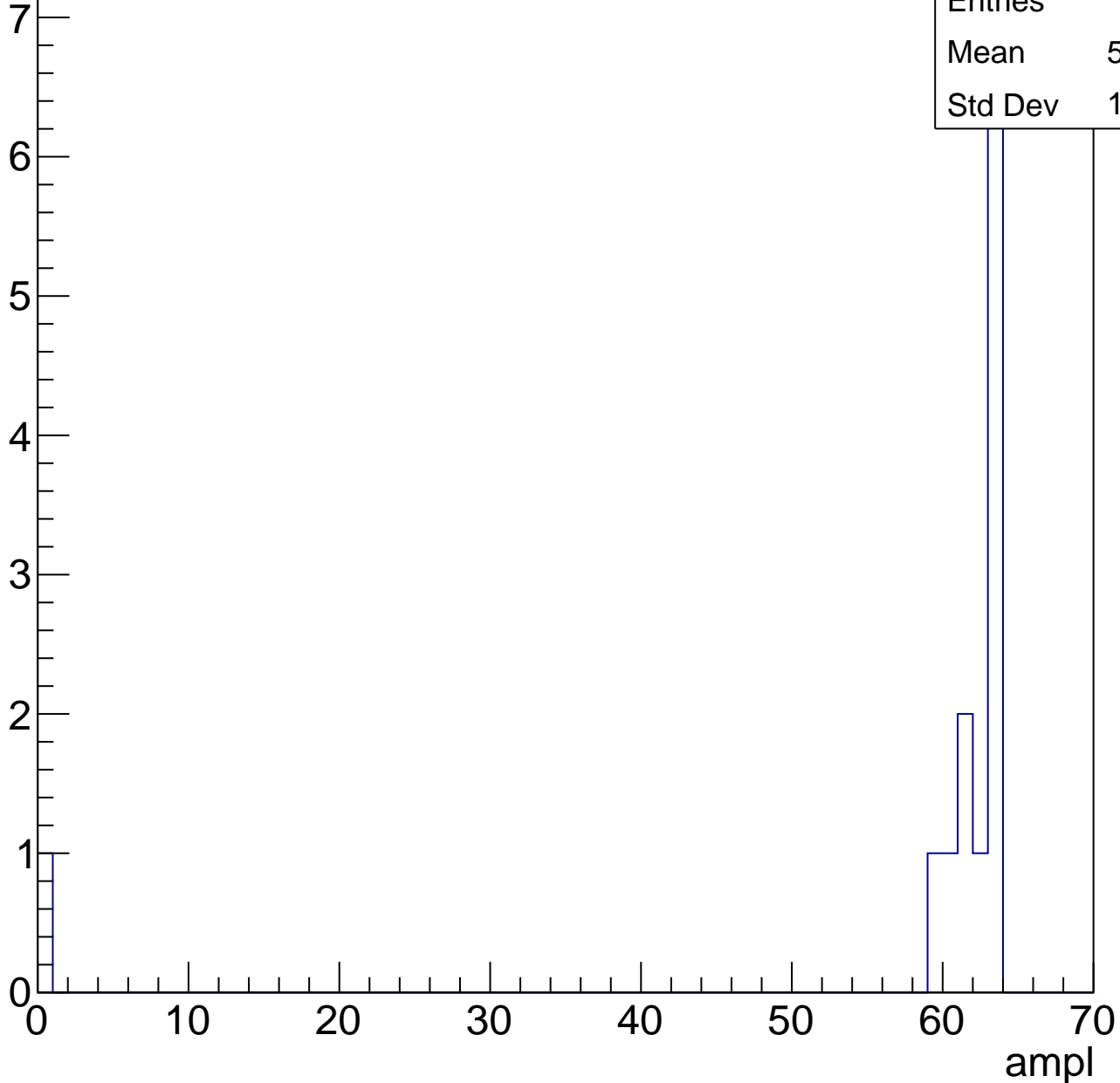
Entries	54
Mean	59.3
Std Dev	2.225

B1L103S, U9-ch112, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	13
Mean	57.23
Std Dev	16.57



B1L103S, U9-ch112, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51

Entry



B1L103S, U9-ch113, adc0

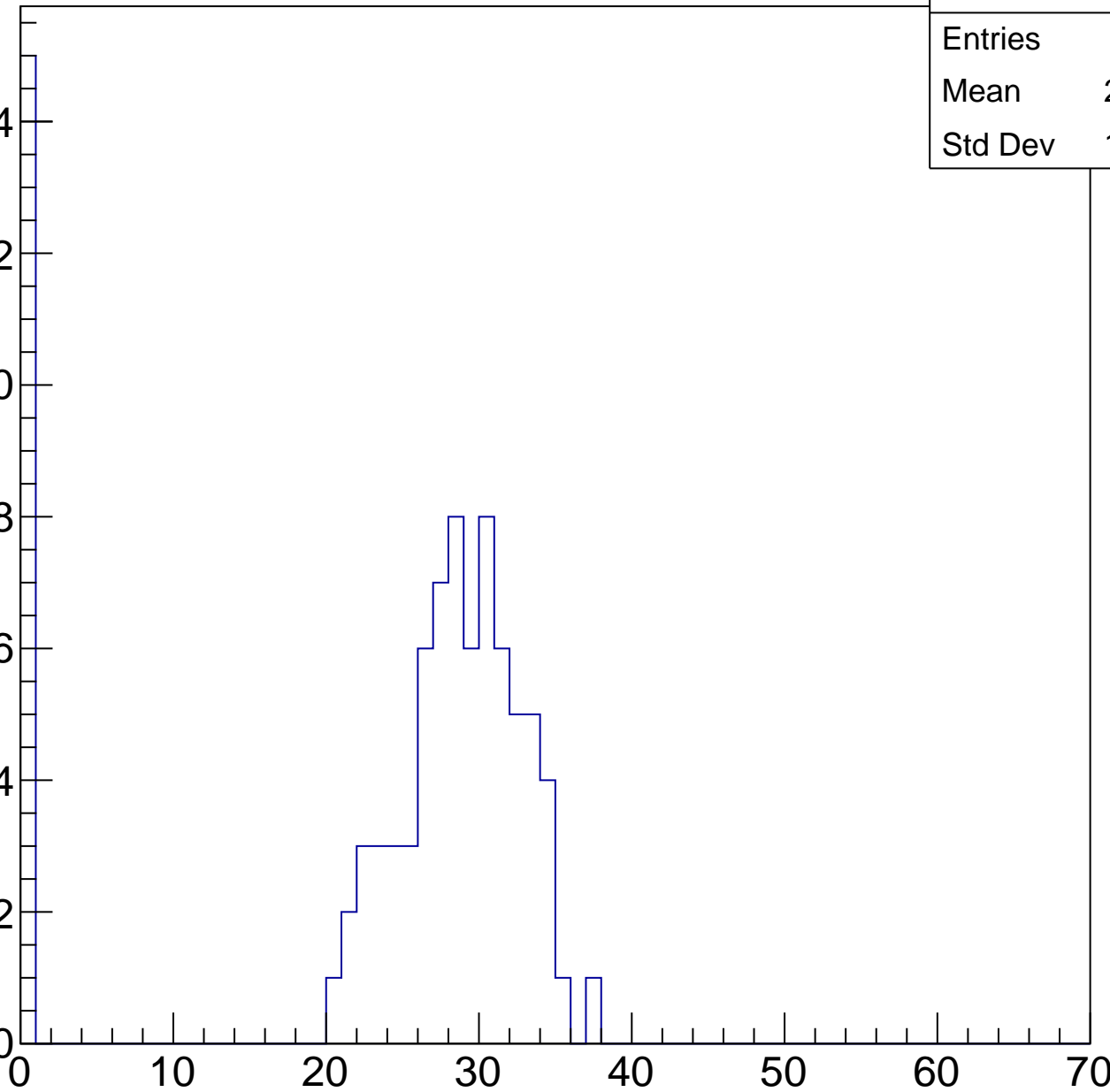
calib_packv5_041523_1651.root, FC#0, port C2

Entries	87
Mean	23.52
Std Dev	11.26

Entry

14
12
10
8
6
4
2
0

ampl

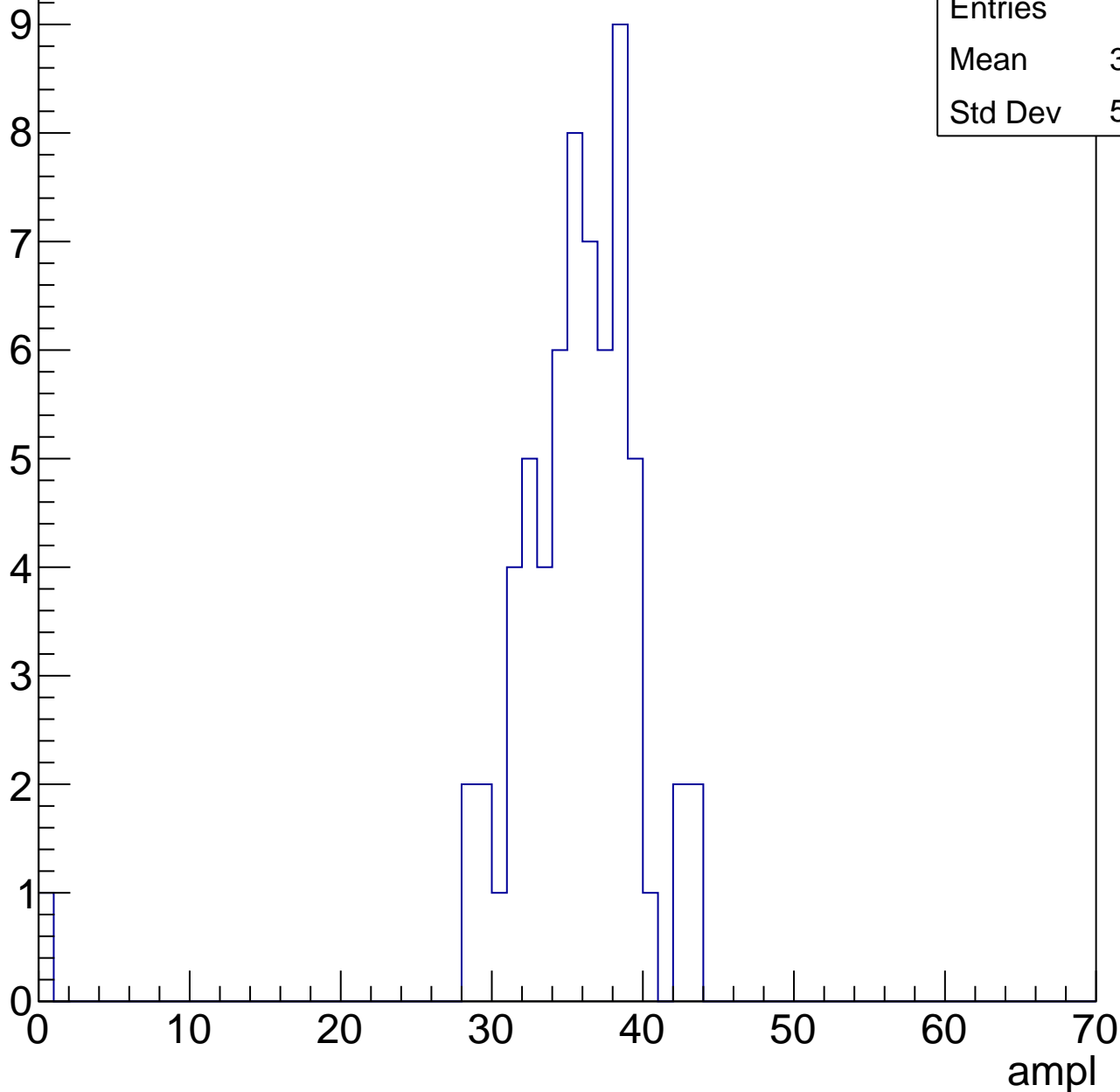


B1L103S, U9-ch113, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	34.85
Std Dev	5.537



B1L103S, U9-ch113, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	36.52
Std Dev	15.05

Entry

10

8

6

4

2

0

0

10

20

30

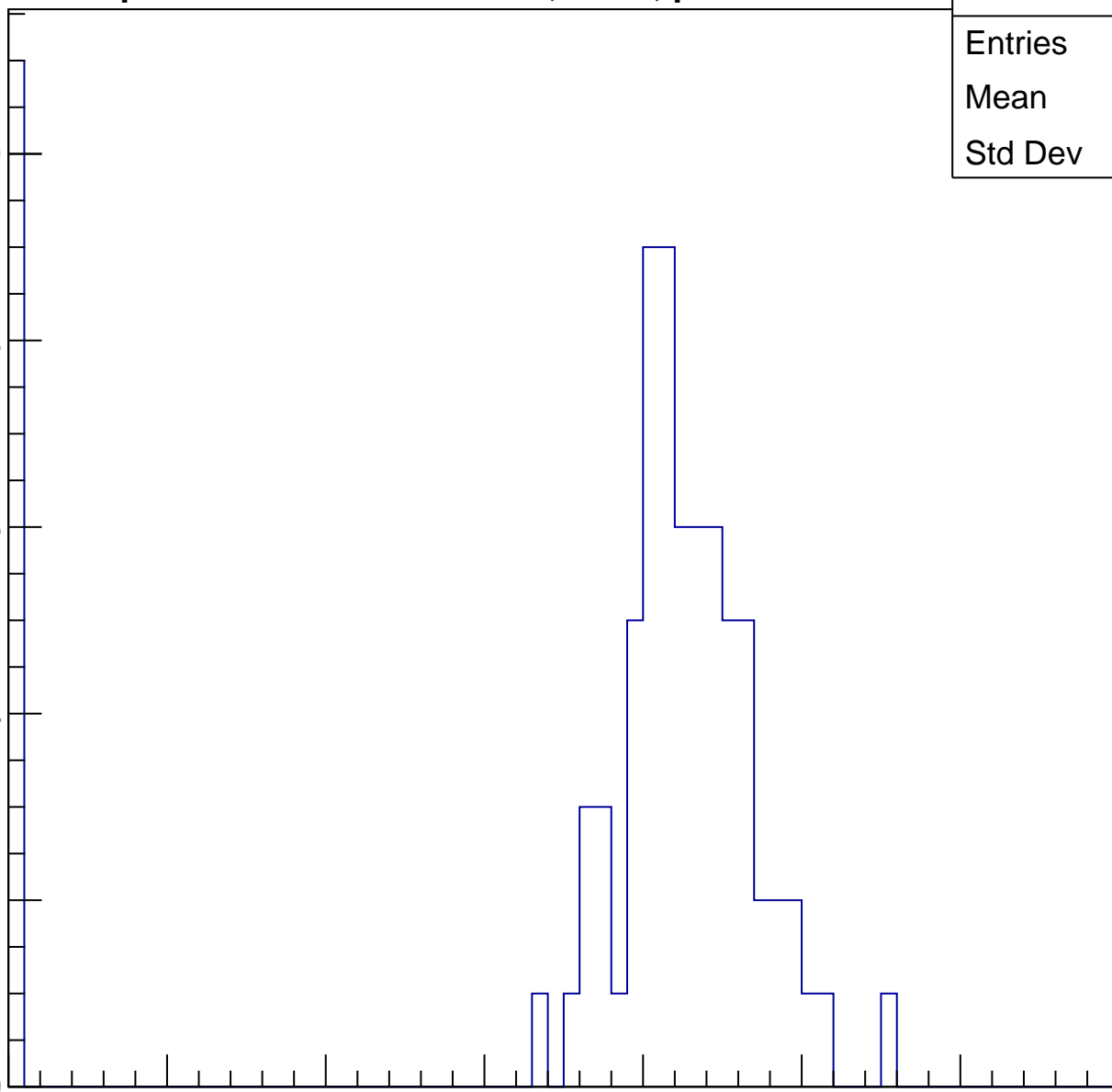
40

50

60

70

ampl

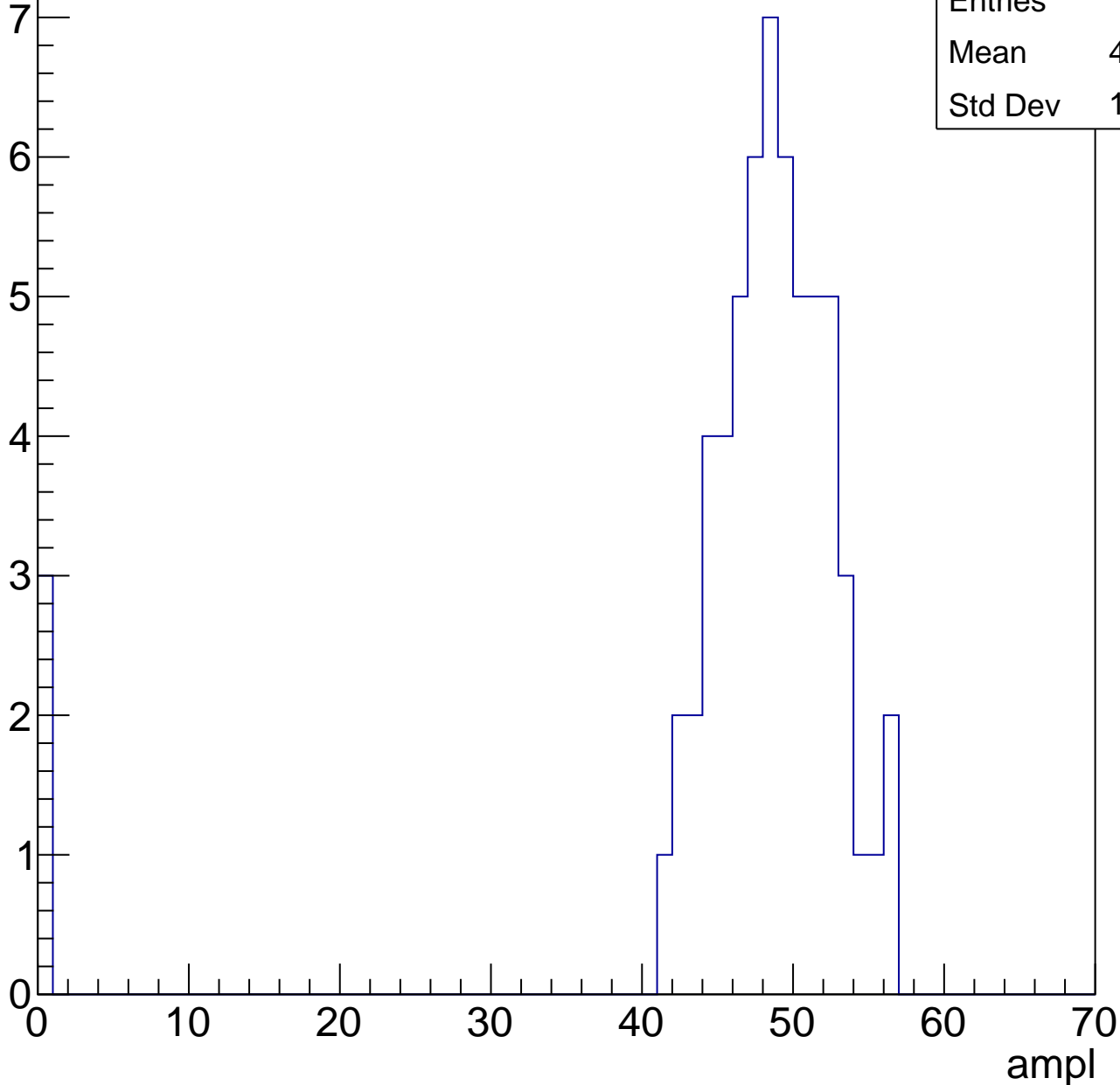


B1L103S, U9-ch113, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	46.03
Std Dev	10.93

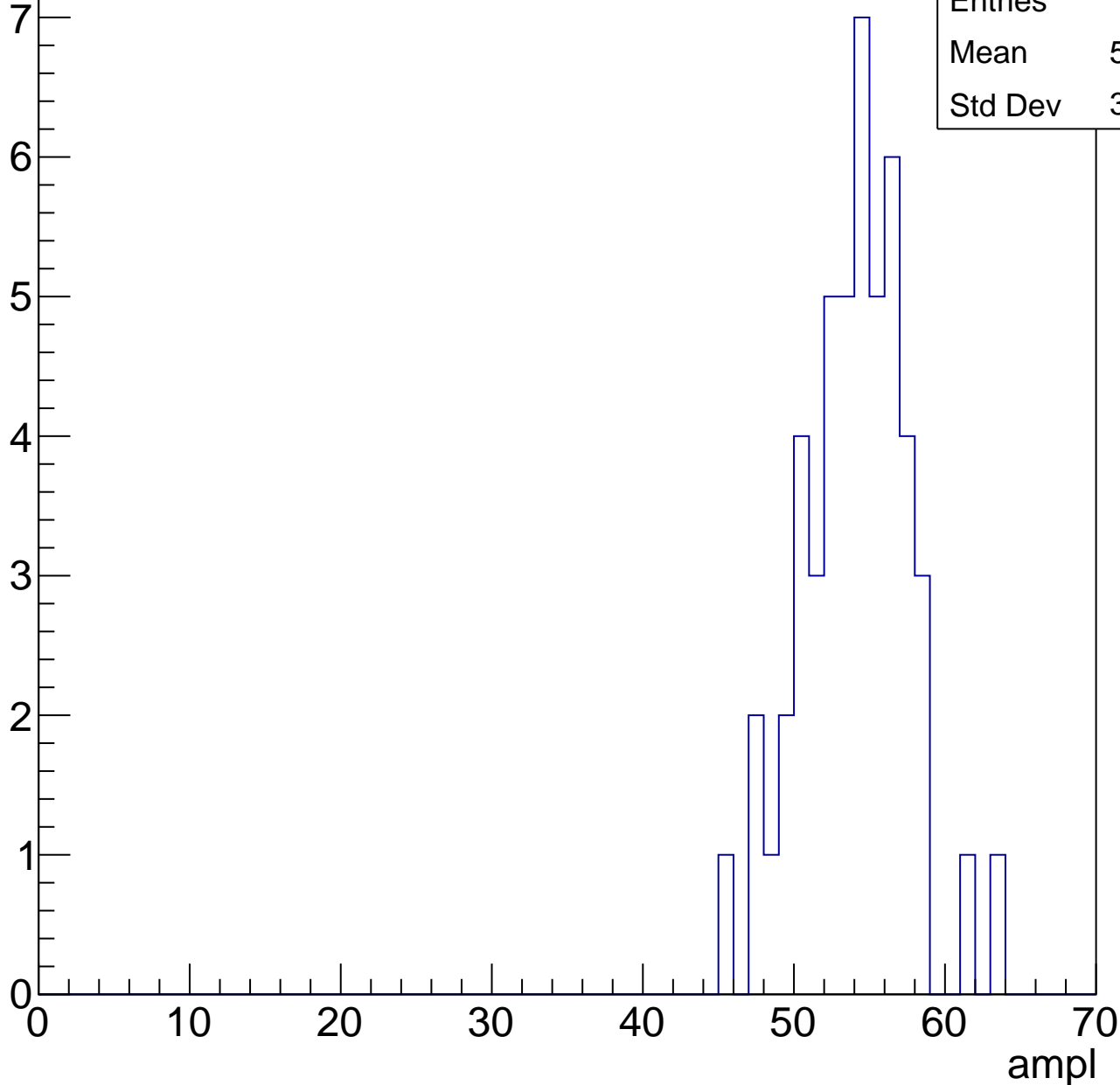


B1L103S, U9-ch113, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	53.56
Std Dev	3.505



B1L103S, U9-ch113, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entries	62
Mean	58.11
Std Dev	7.95

Entry

10

8

6

4

2

0

0

10

20

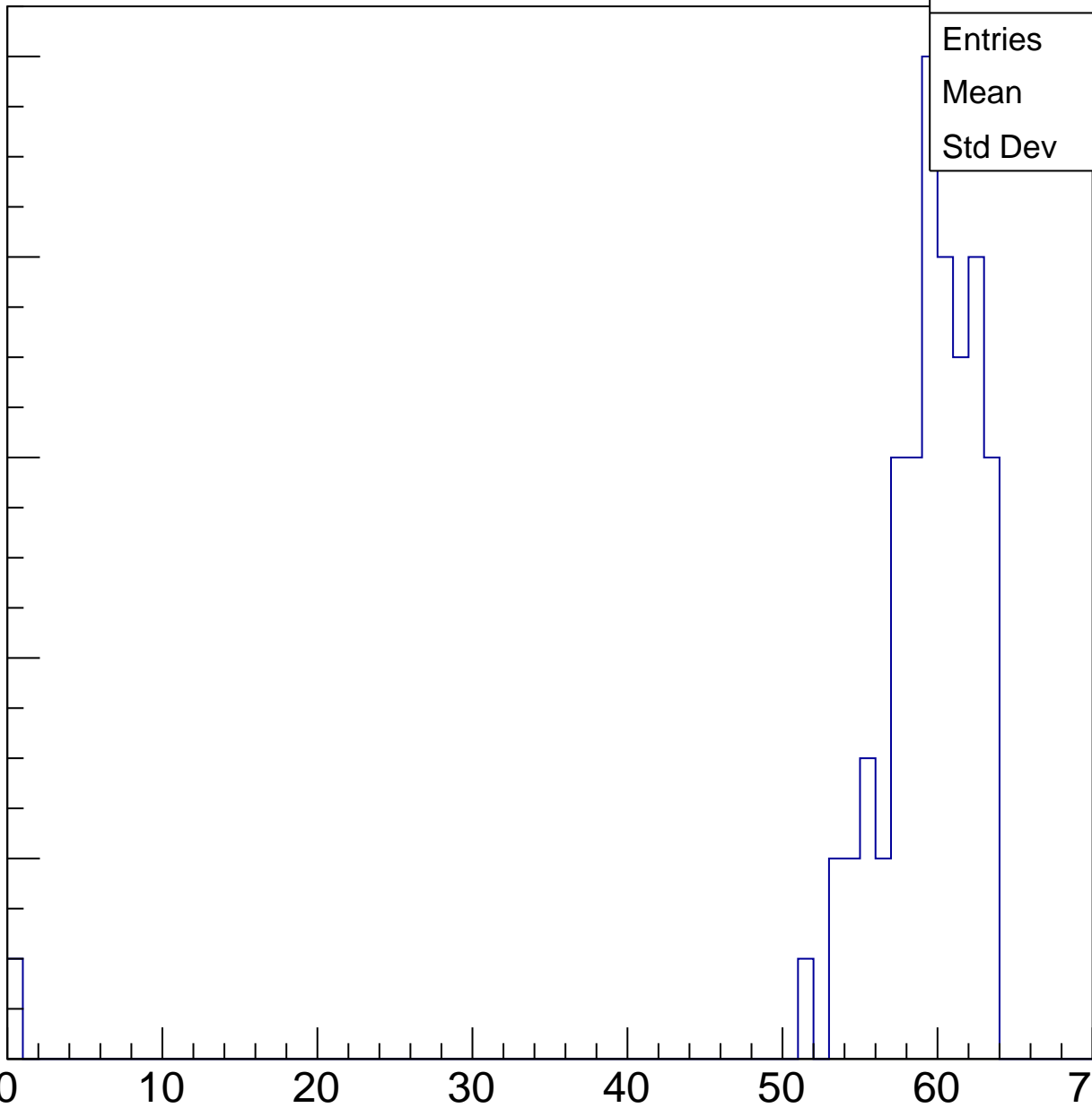
30

40

50

60

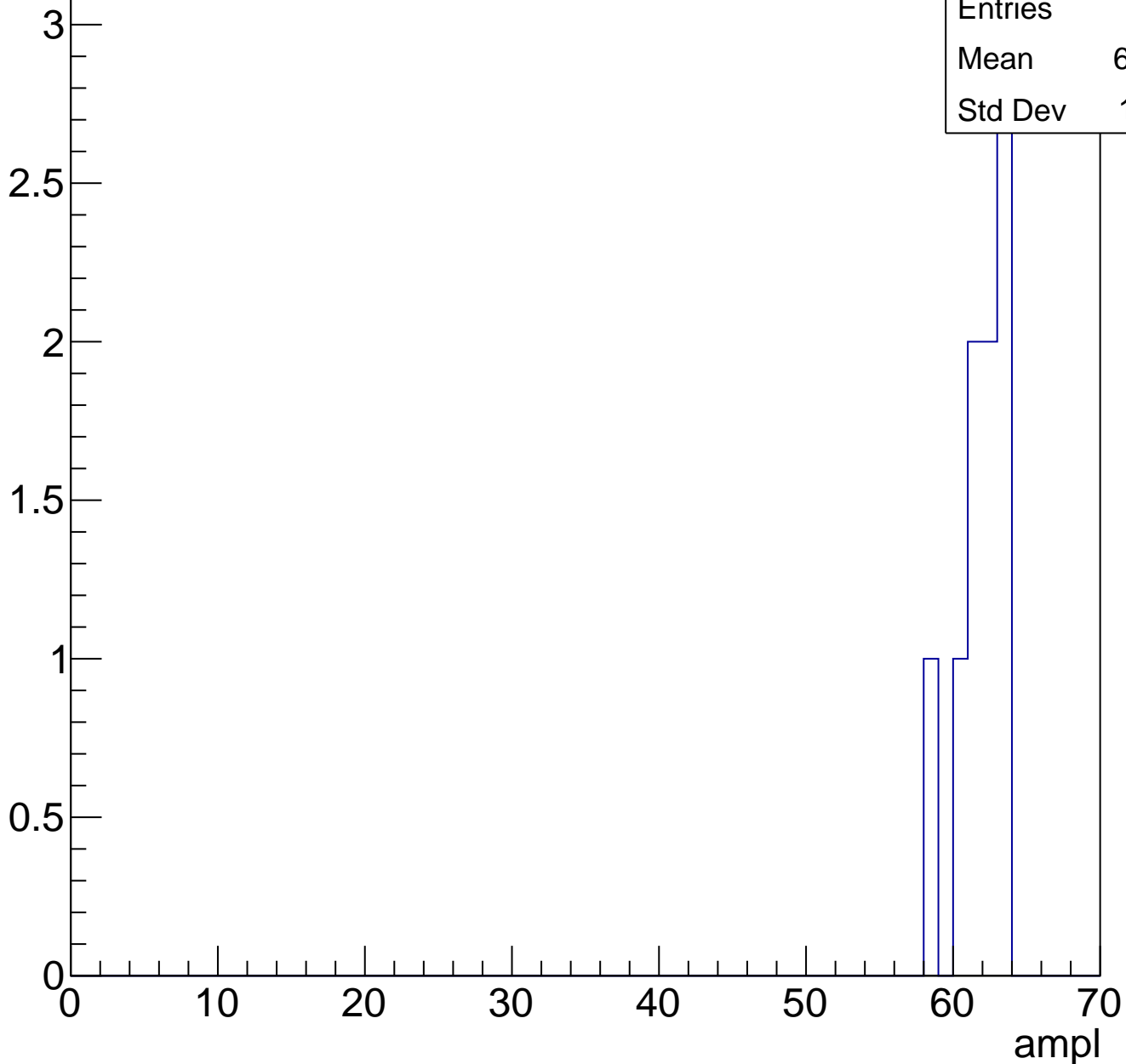
ampl



B1L103S, U9-ch113, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch113, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3
Std Dev	13.08

Entry



B1L103S, U9-ch114, adc0

calib_packv5_041523_1651.root, FC#0, port C2

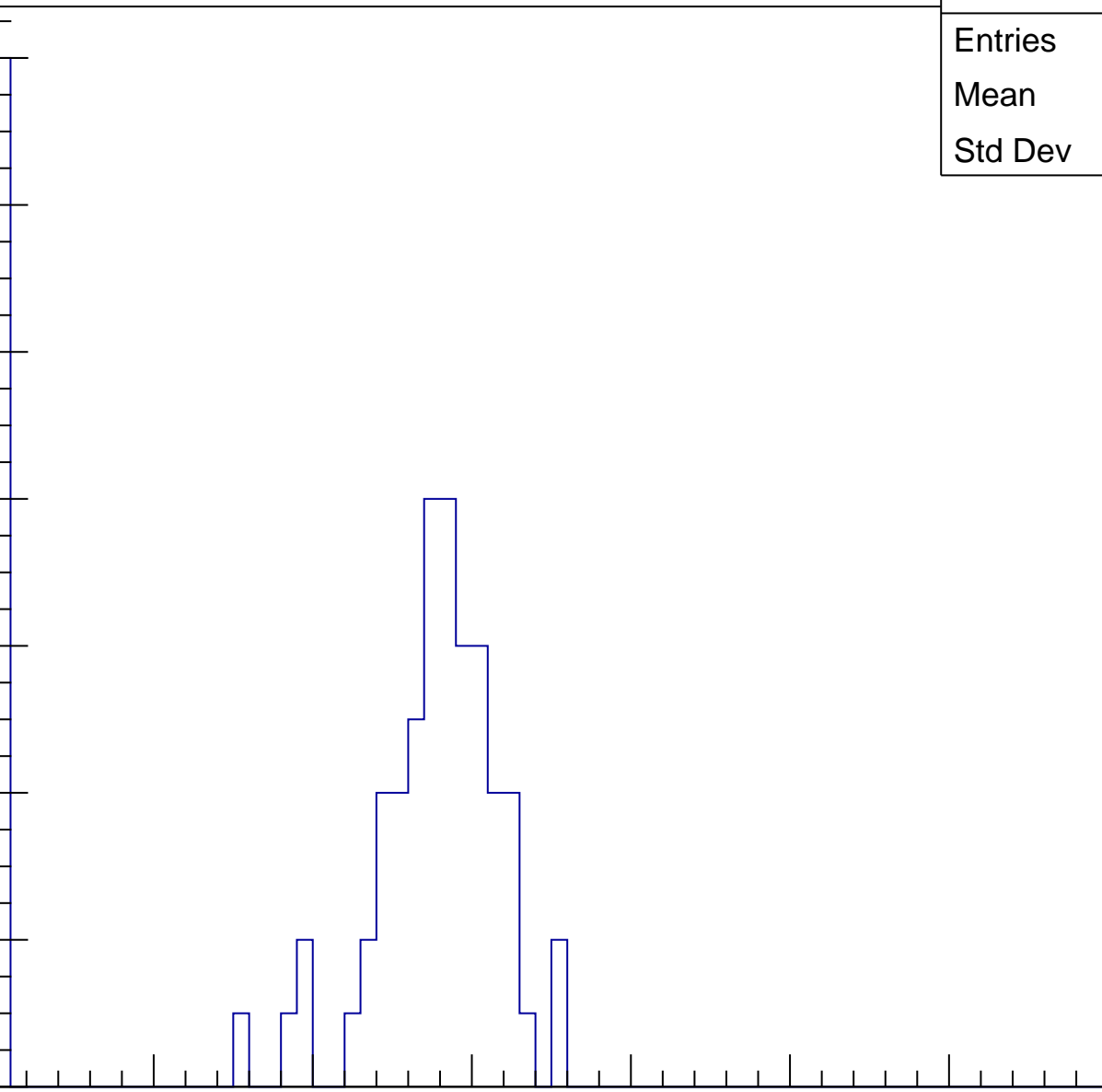
Entries	73
Mean	22.11
Std Dev	11.31

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl



B1L103S, U9-ch114, adc1

calib_packv5_041523_1651.root, FC#0, port C2

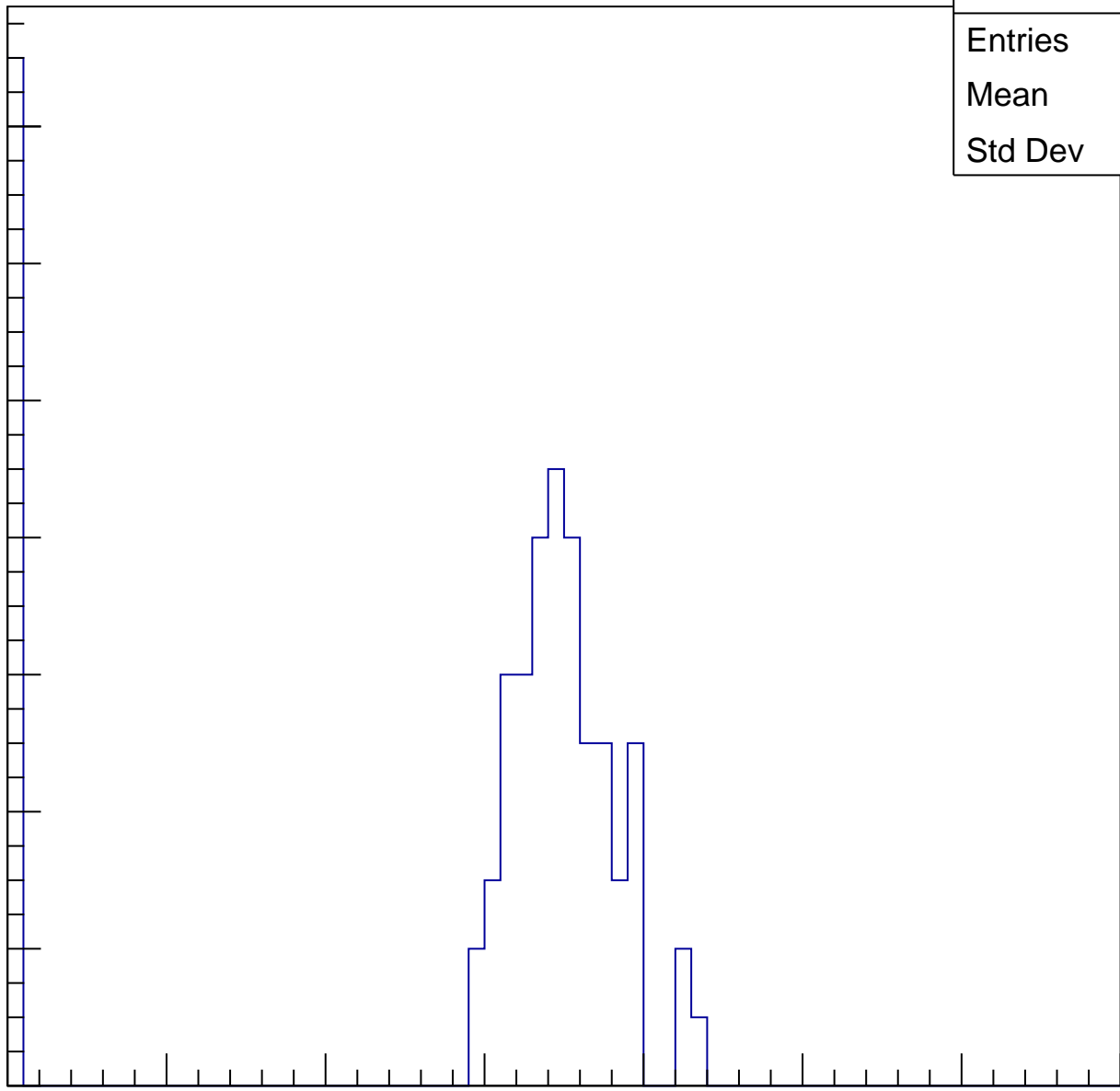
Entries	78
Mean	27.91
Std Dev	13.91

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

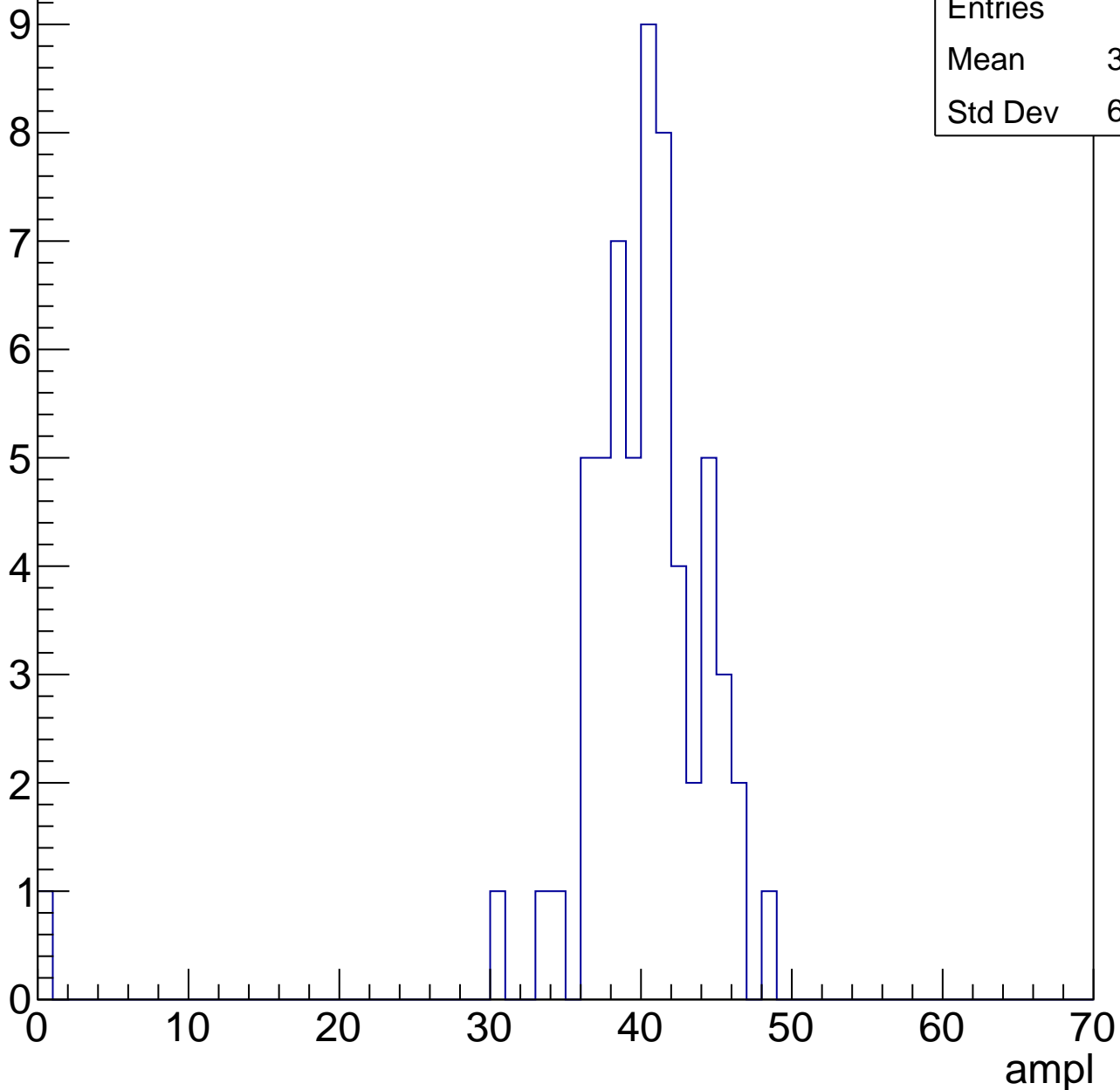


B1L103S, U9-ch114, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	39.33
Std Dev	6.123

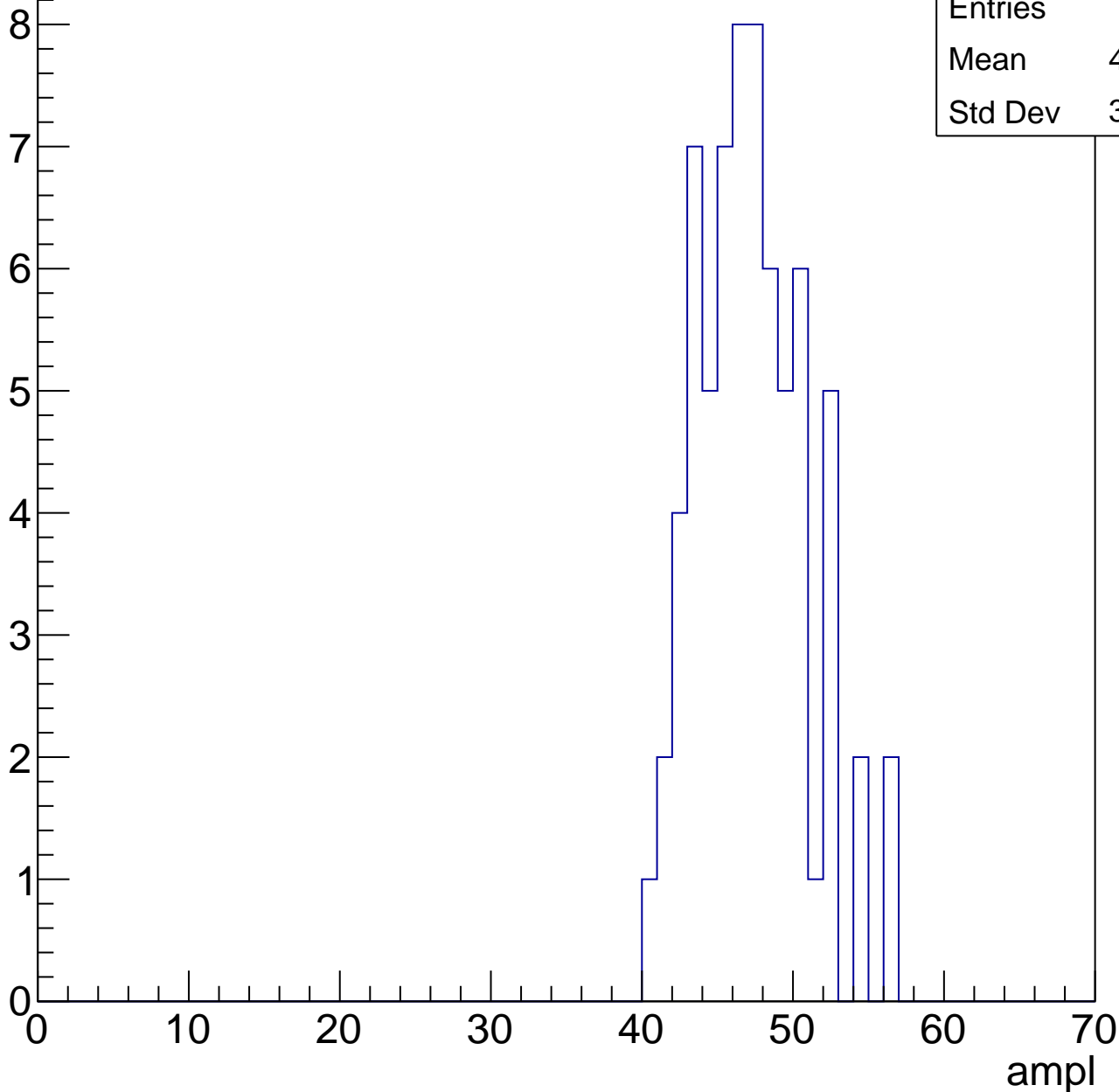


B1L103S, U9-ch114, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

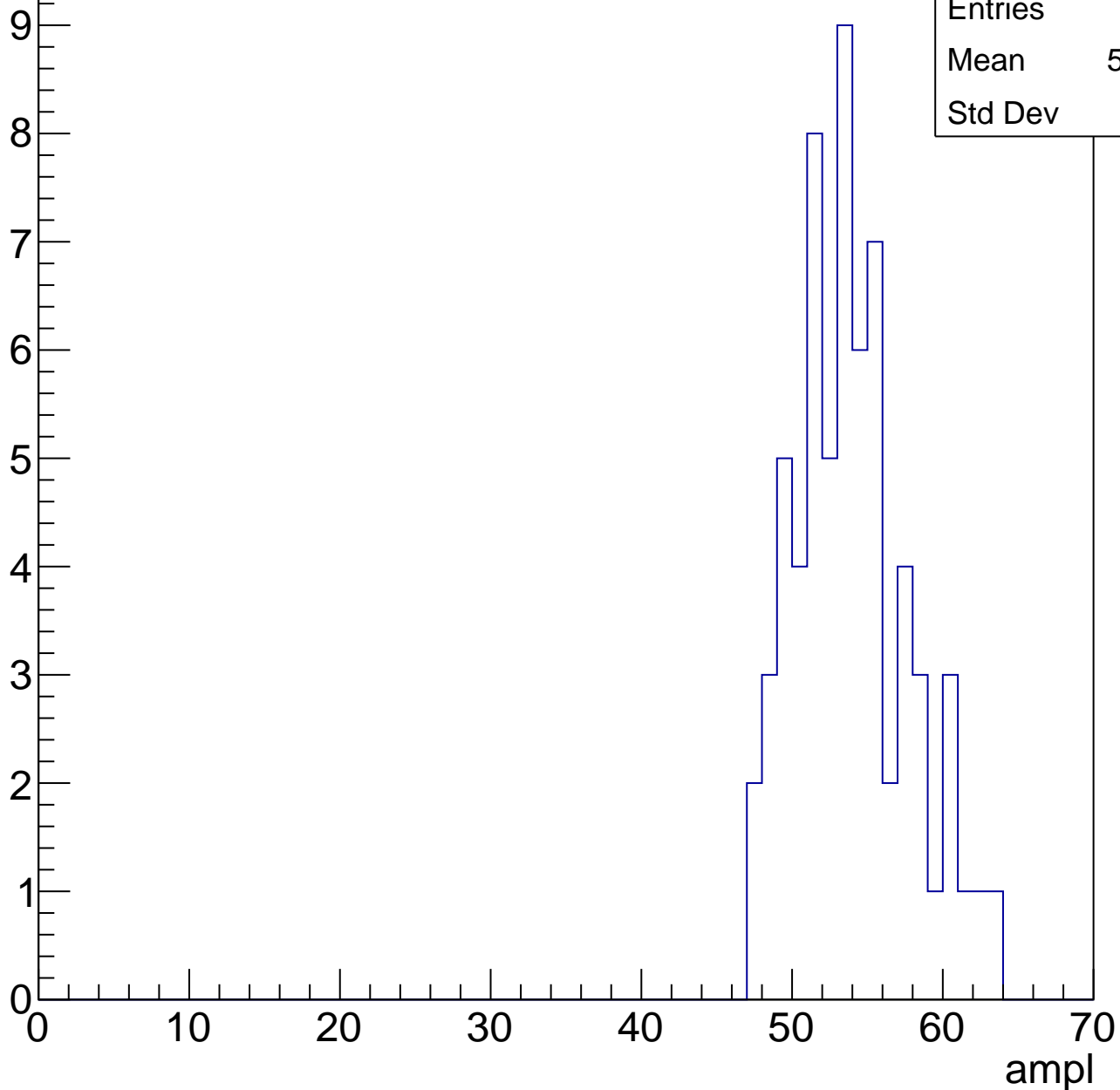
Entries	69
Mean	46.87
Std Dev	3.599



B1L103S, U9-ch114, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



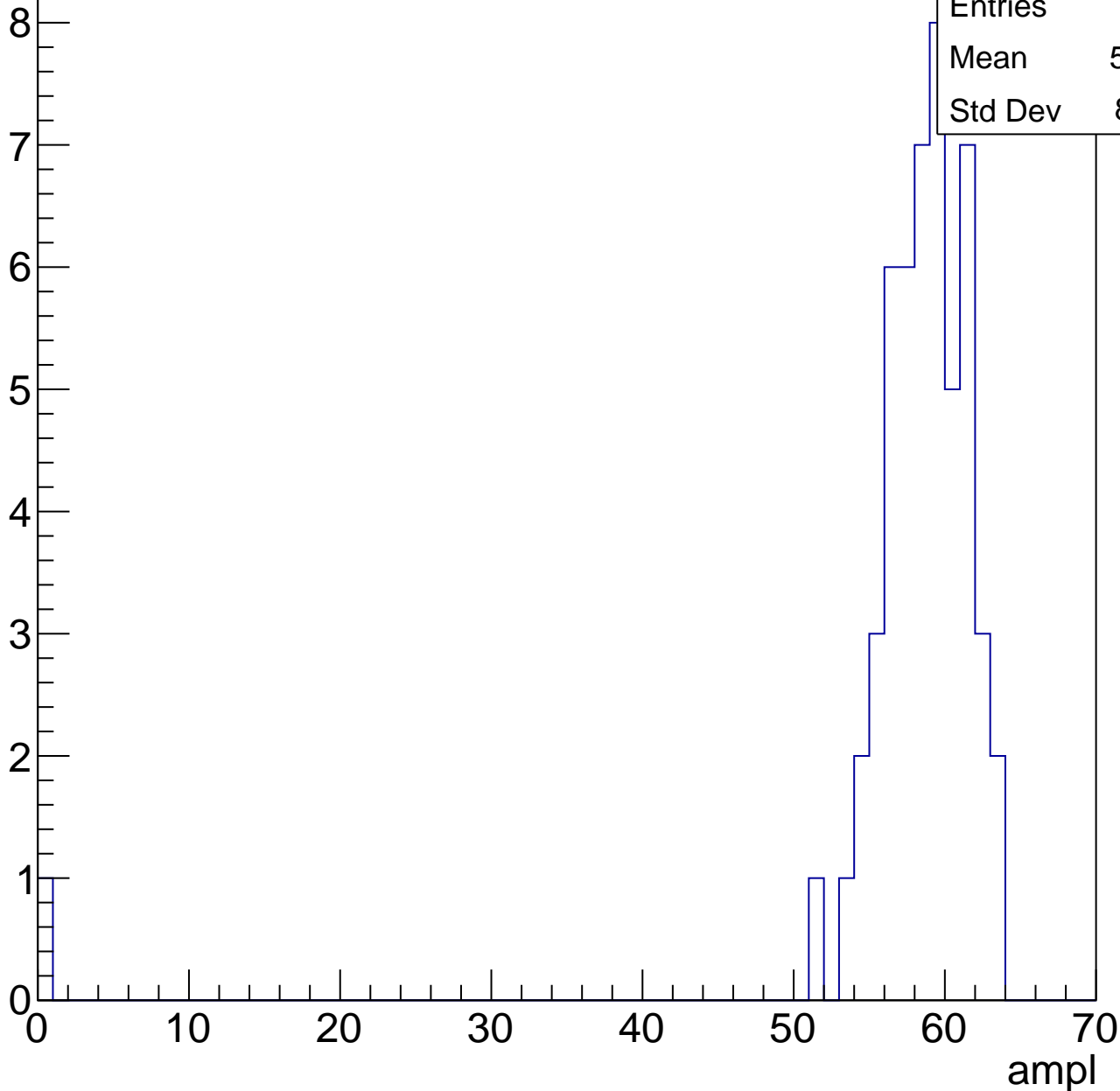
Entries	65
Mean	53.48
Std Dev	3.73

B1L103S, U9-ch114, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	57.15
Std Dev	8.411

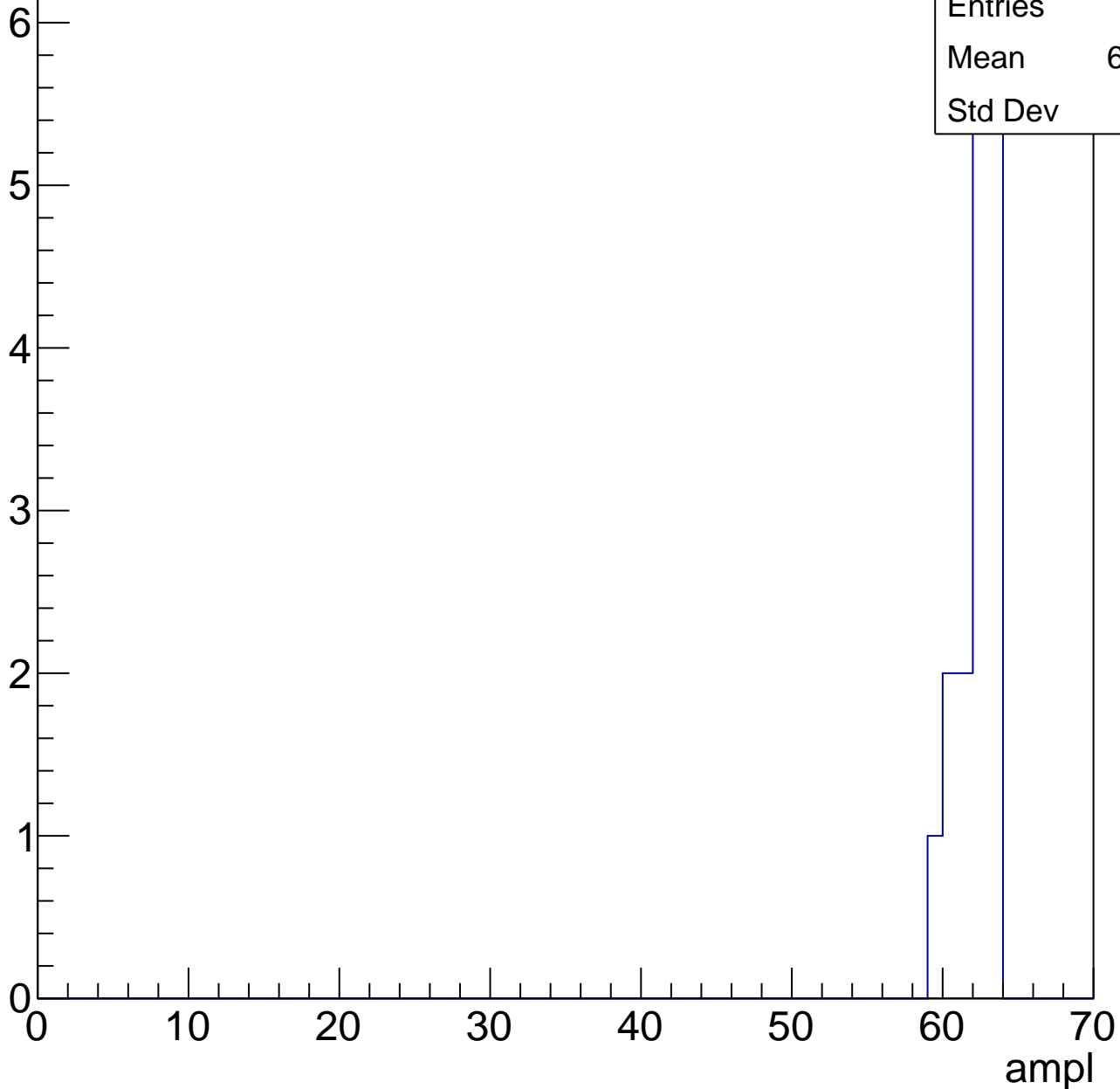


B1L103S, U9-ch114, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	17
Mean	61.82
Std Dev	1.2



B1L103S, U9-ch114, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry



B1L103S, U9-ch115, adc0

calib_packv5_041523_1651.root, FC#0, port C2

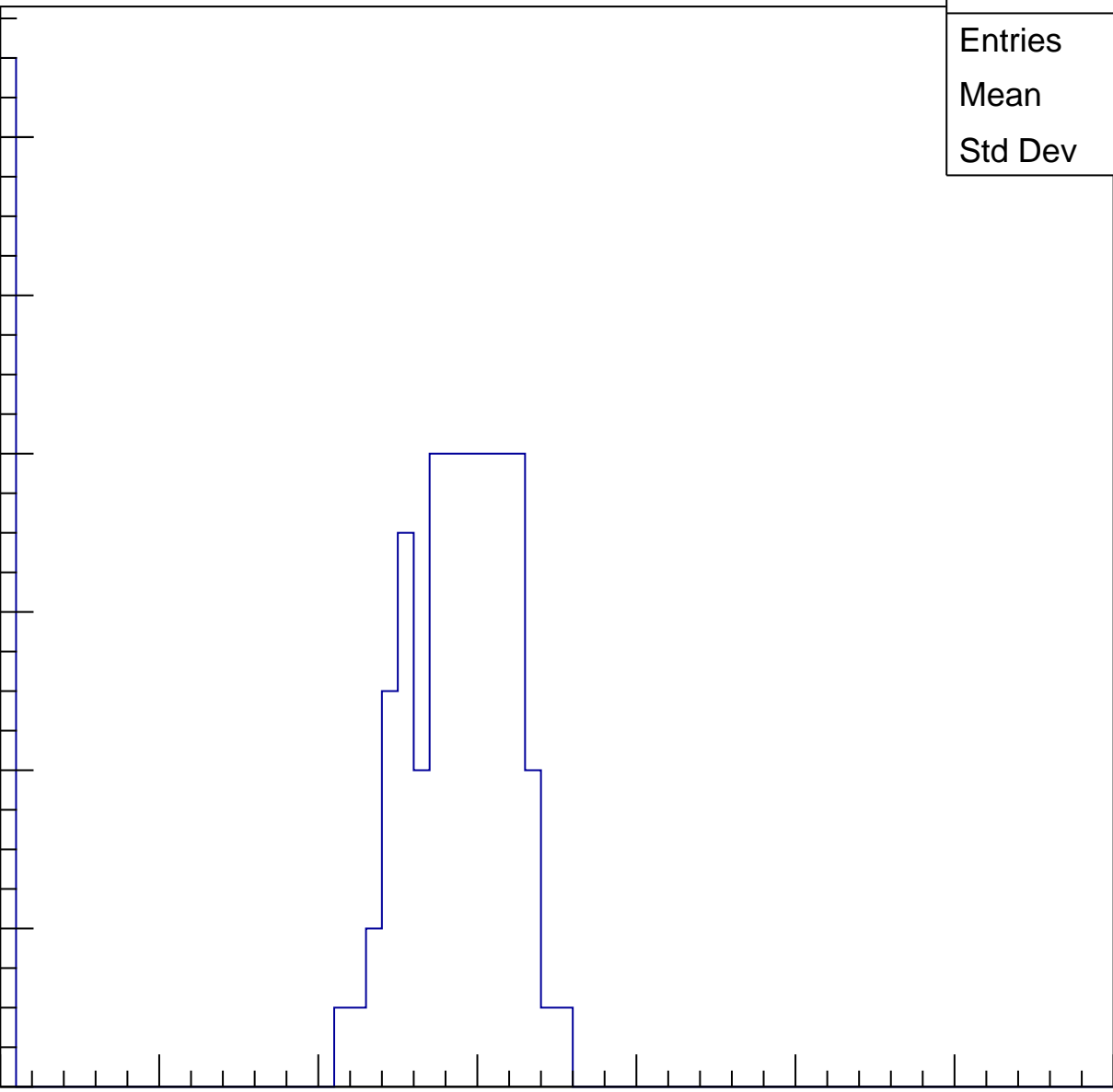
Entries	87
Mean	24.2
Std Dev	10.54

Entry

12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

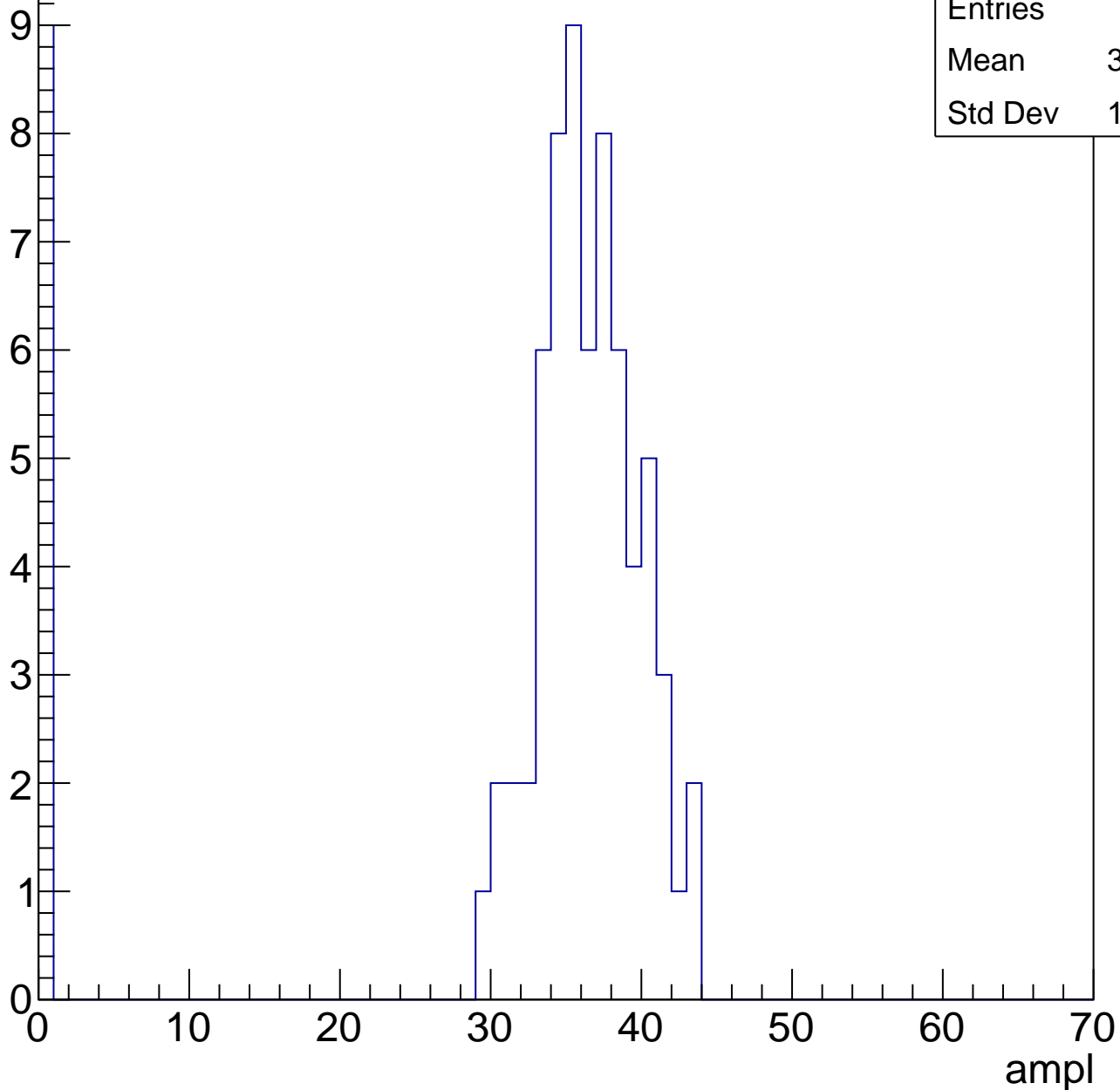
ampl



B1L103S, U9-ch115, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry



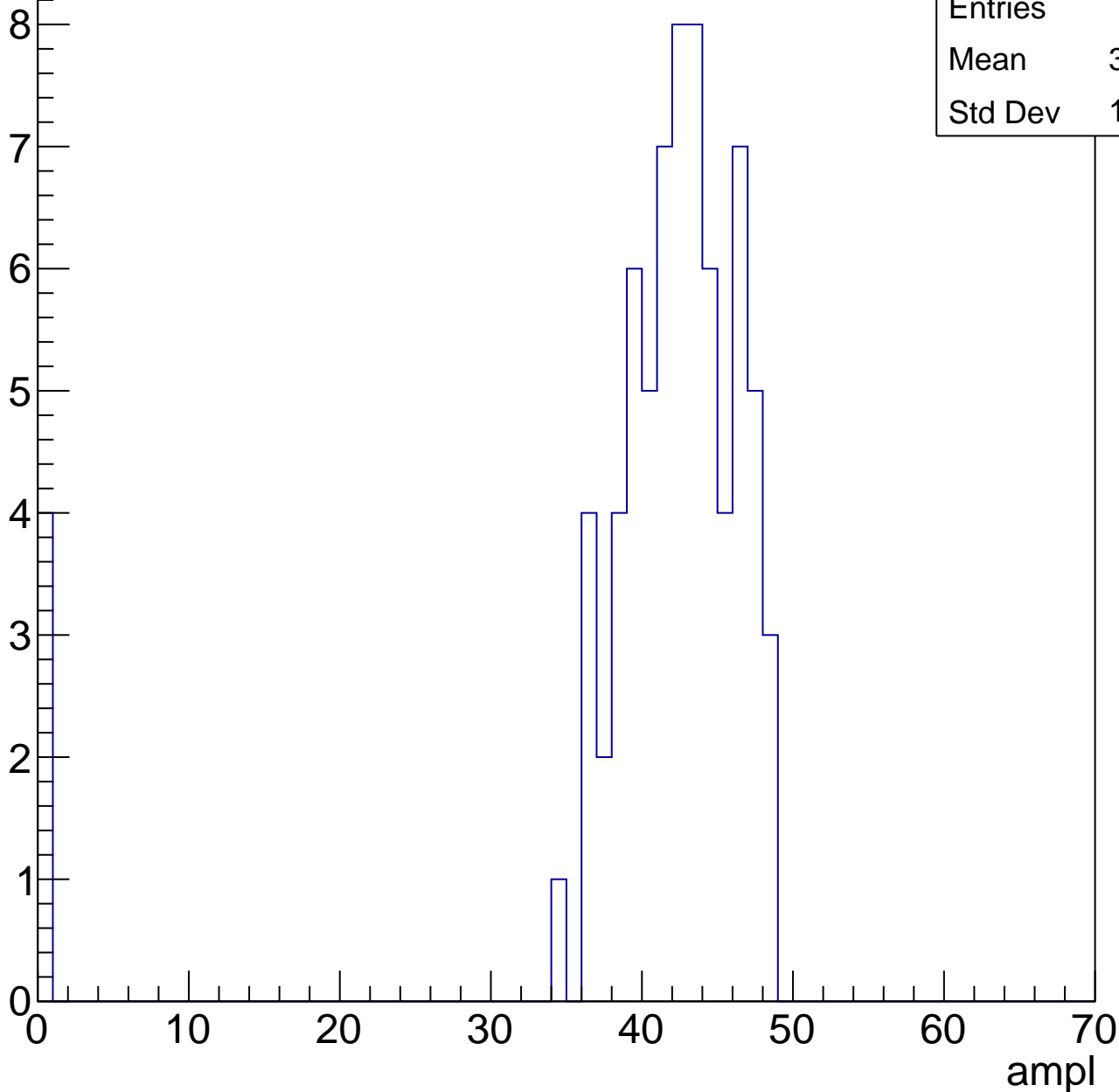
Entries	74
Mean	31.72
Std Dev	12.17

B1L103S, U9-ch115, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	39.86
Std Dev	10.09

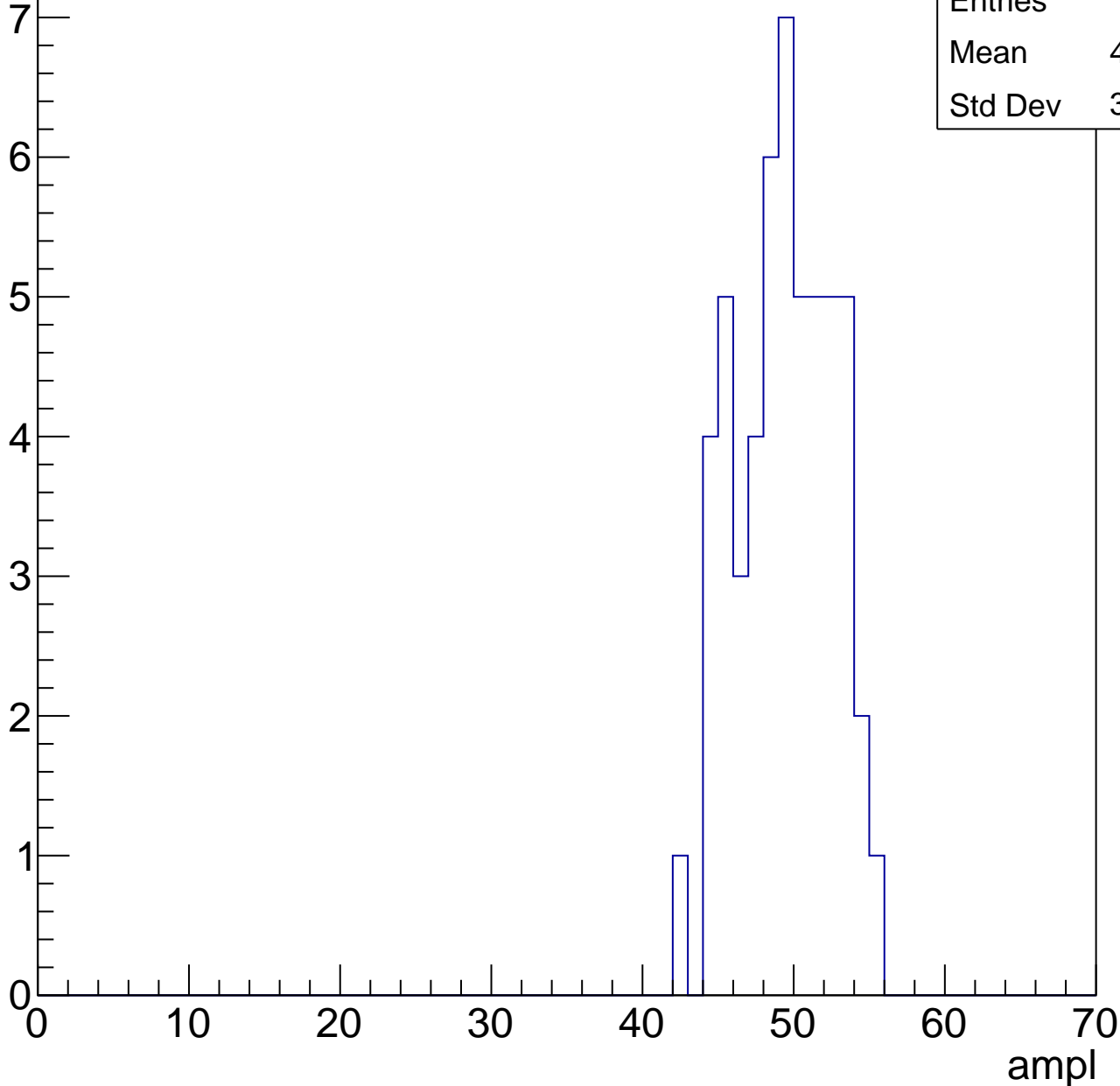


B1L103S, U9-ch115, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	48.92
Std Dev	3.113

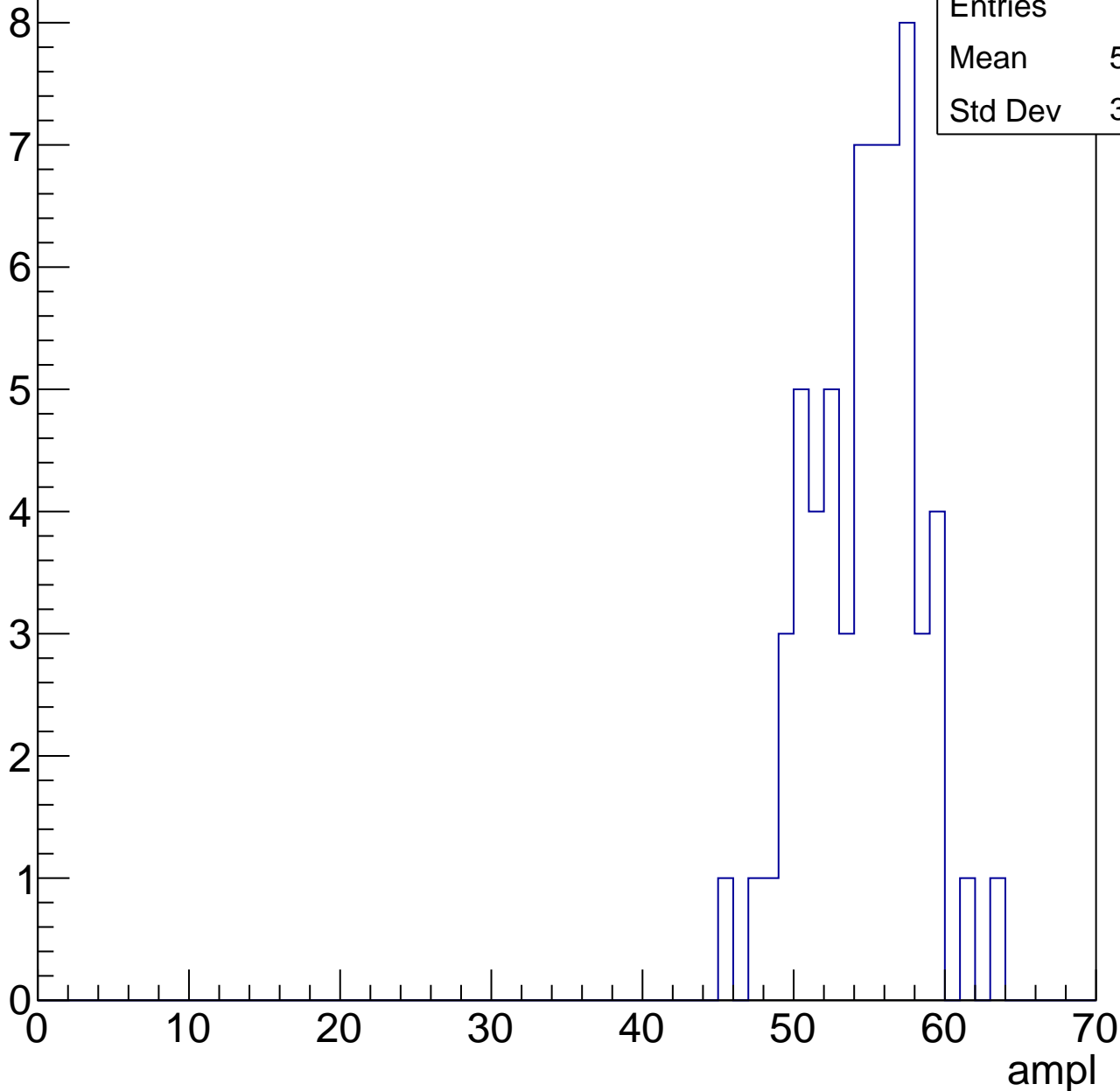


B1L103S, U9-ch115, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	54.18
Std Dev	3.537

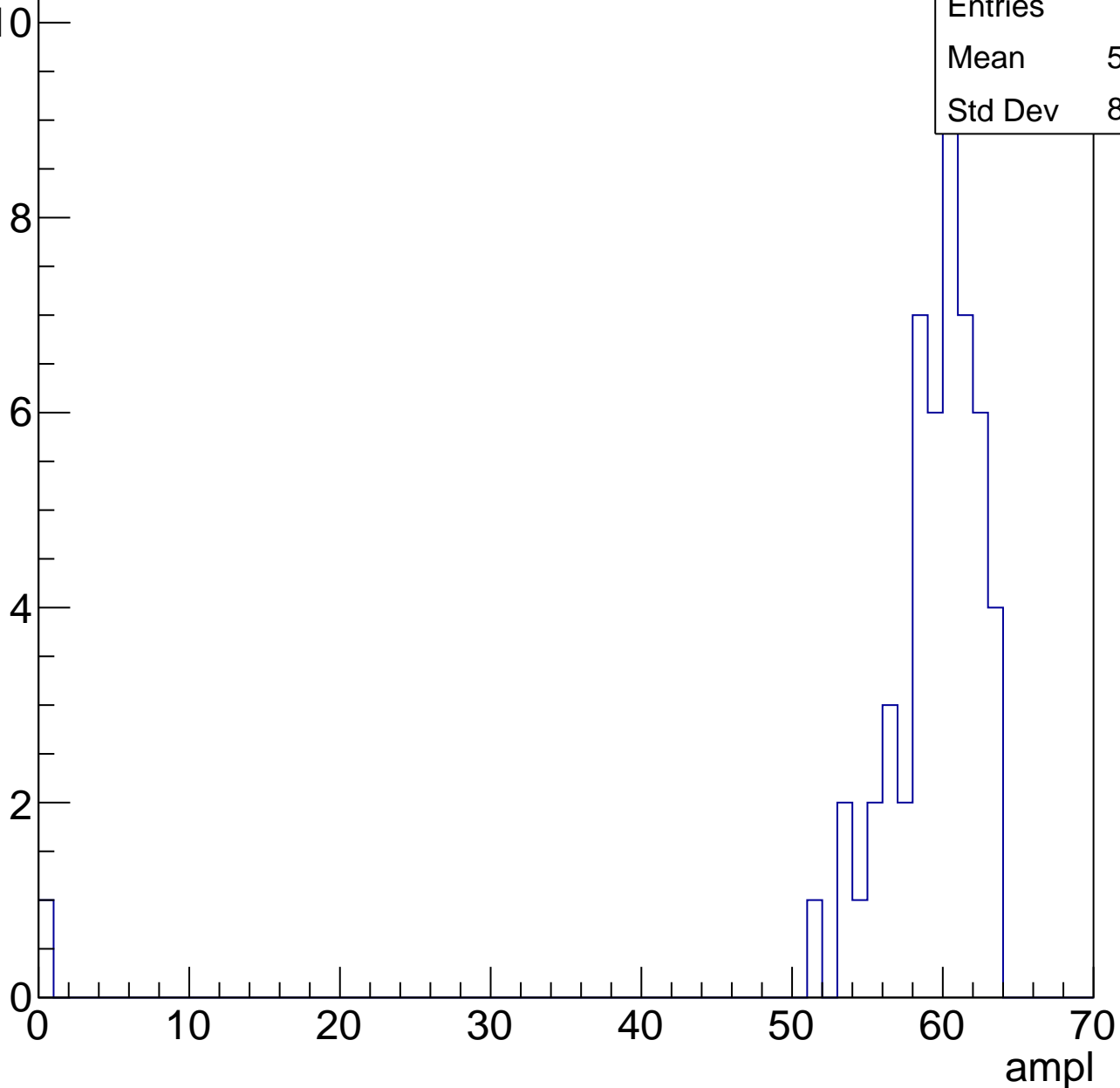


B1L103S, U9-ch115, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

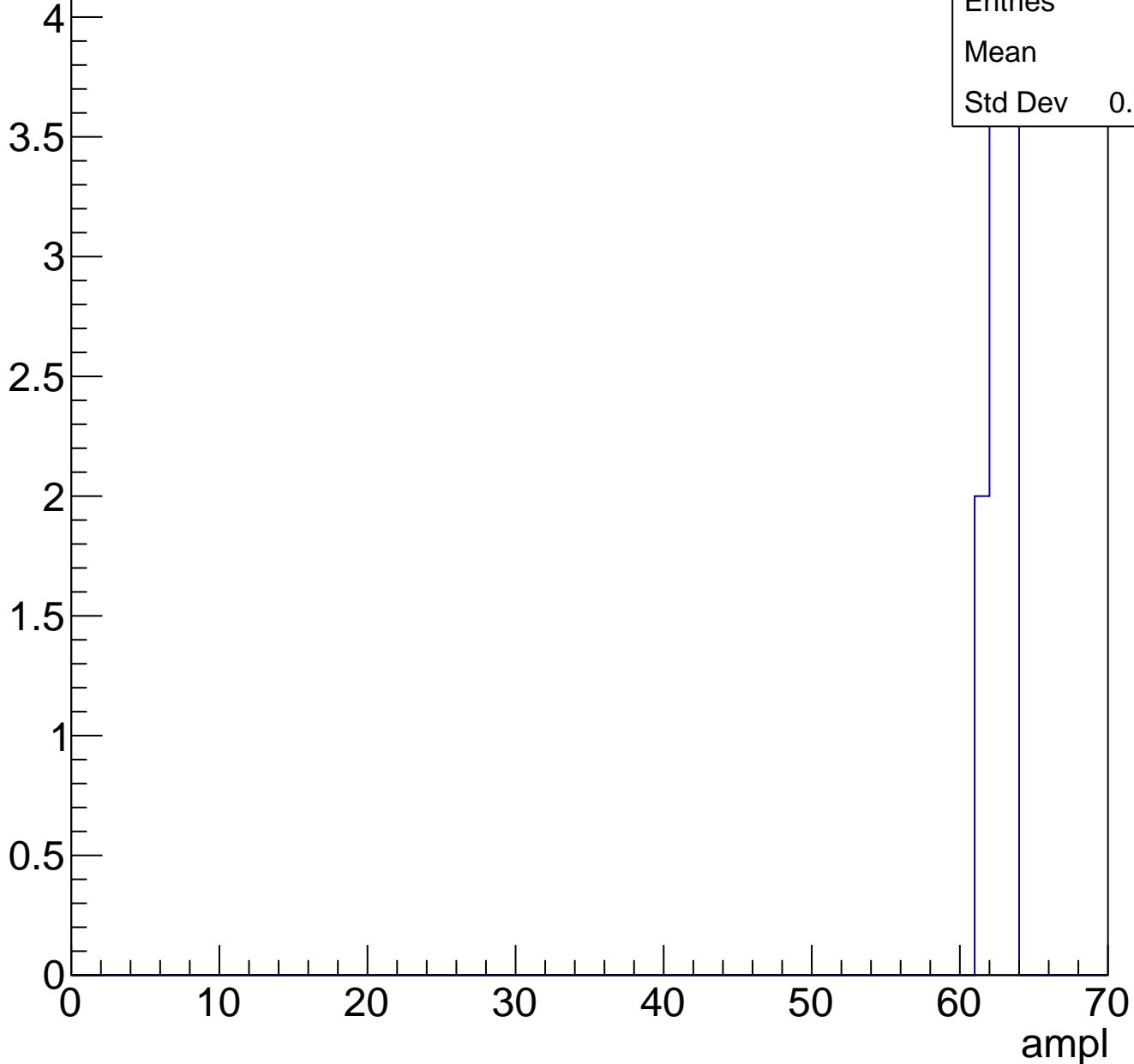
Entries	52
Mean	57.96
Std Dev	8.566



B1L103S, U9-ch115, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch115, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry

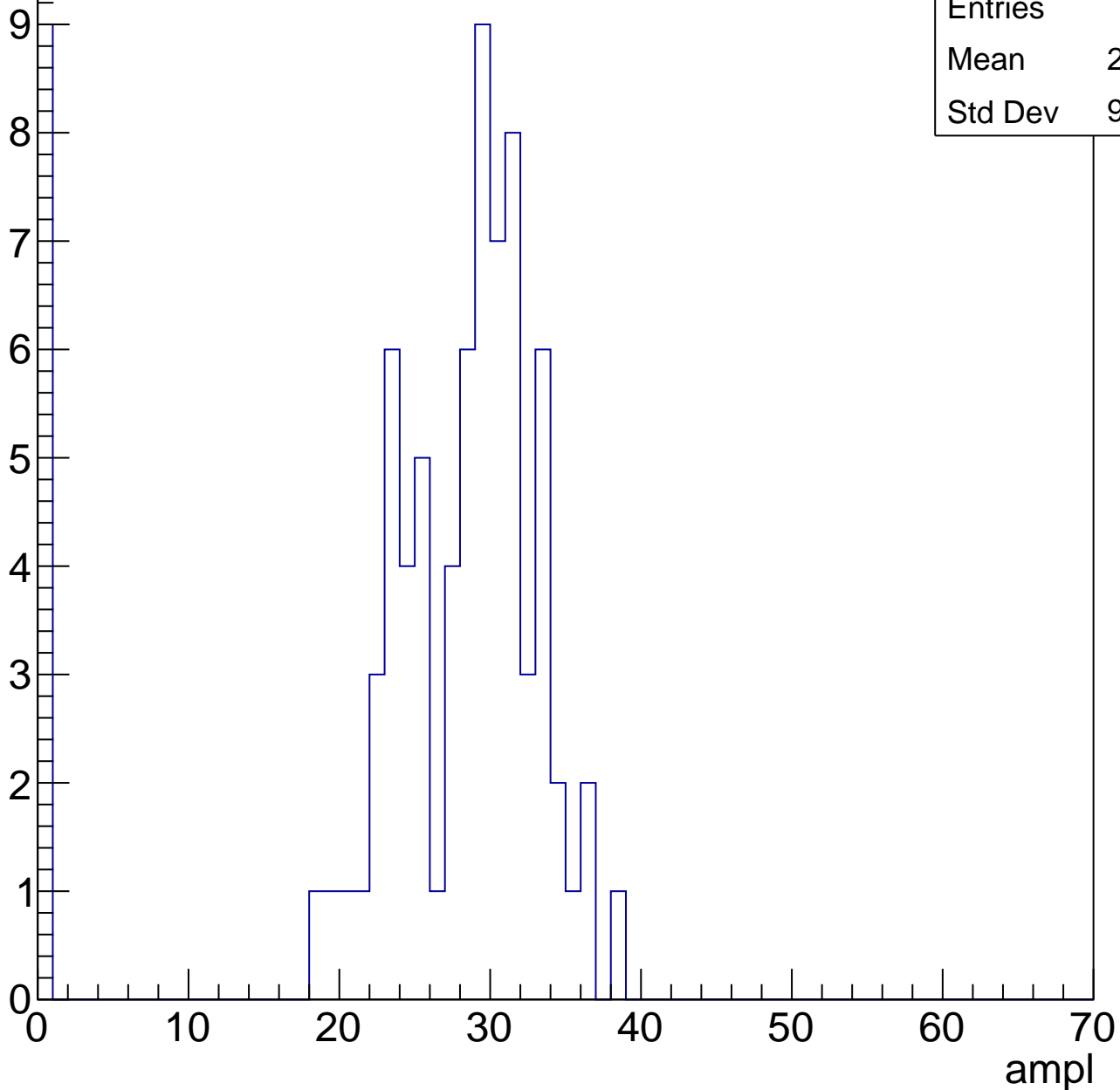


B1L103S, U9-ch116, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	81
Mean	25.07
Std Dev	9.742

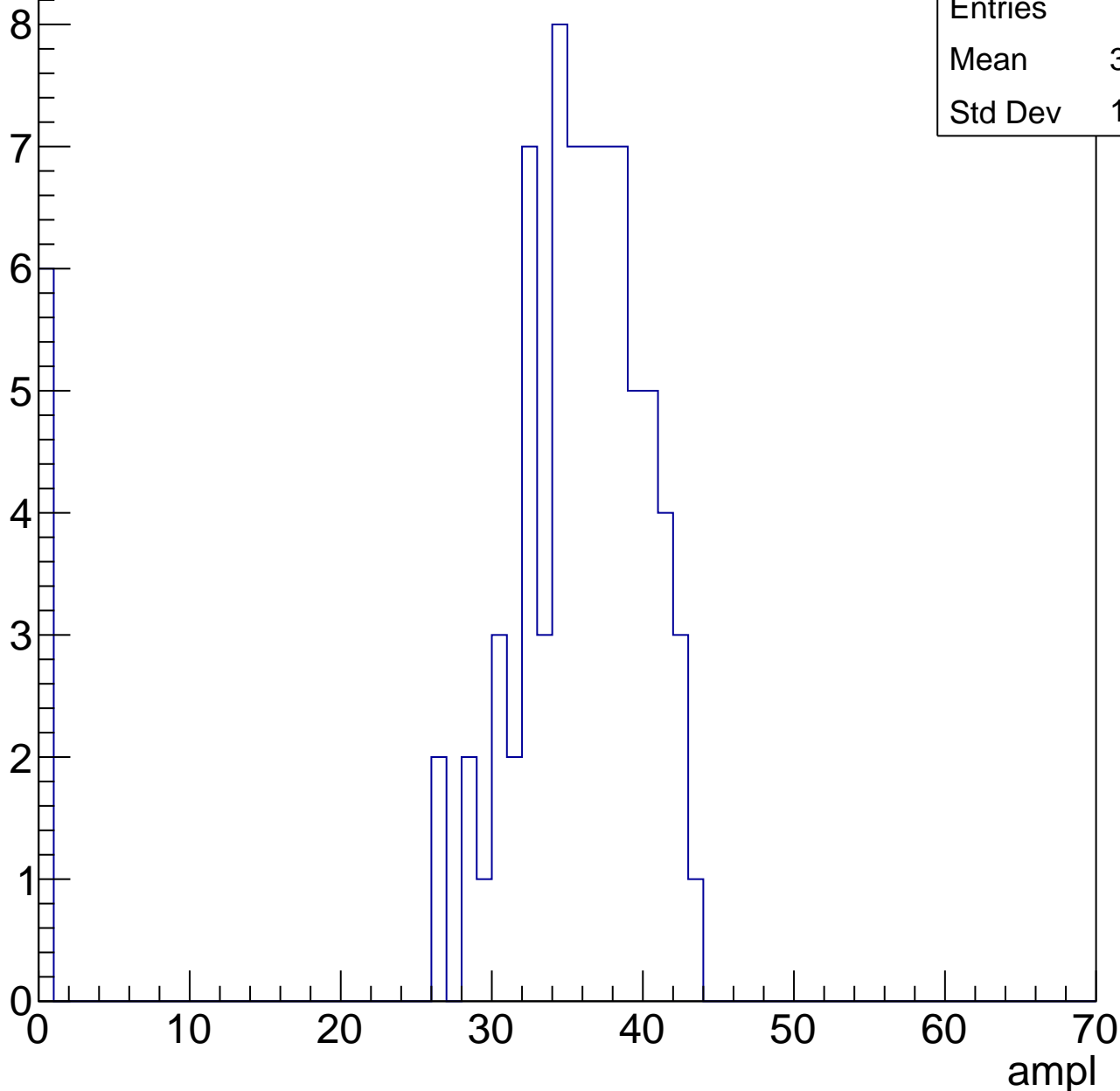


B1L103S, U9-ch116, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	80
Mean	32.92
Std Dev	10.09

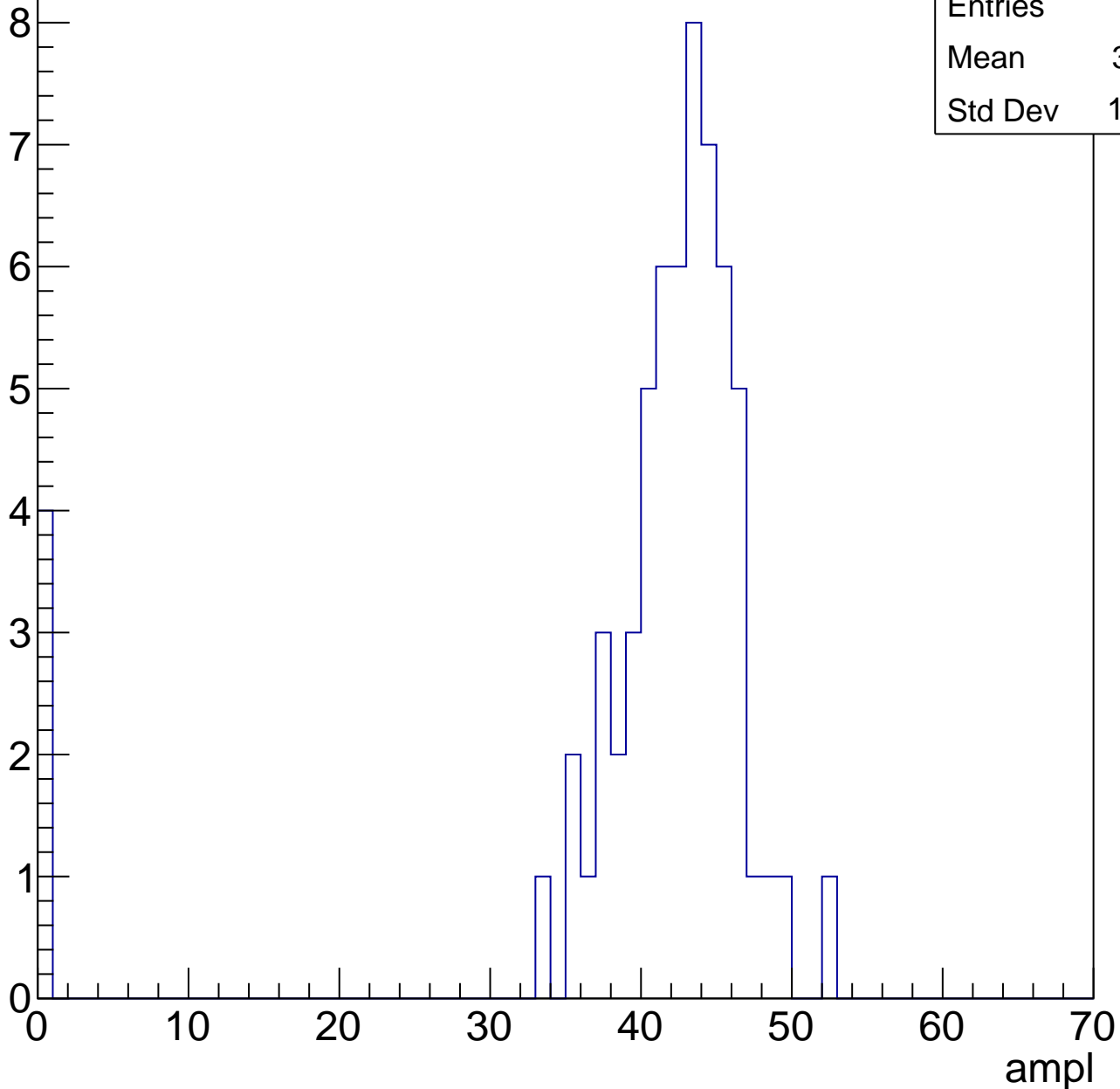


B1L103S, U9-ch116, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	39.51
Std Dev	10.85

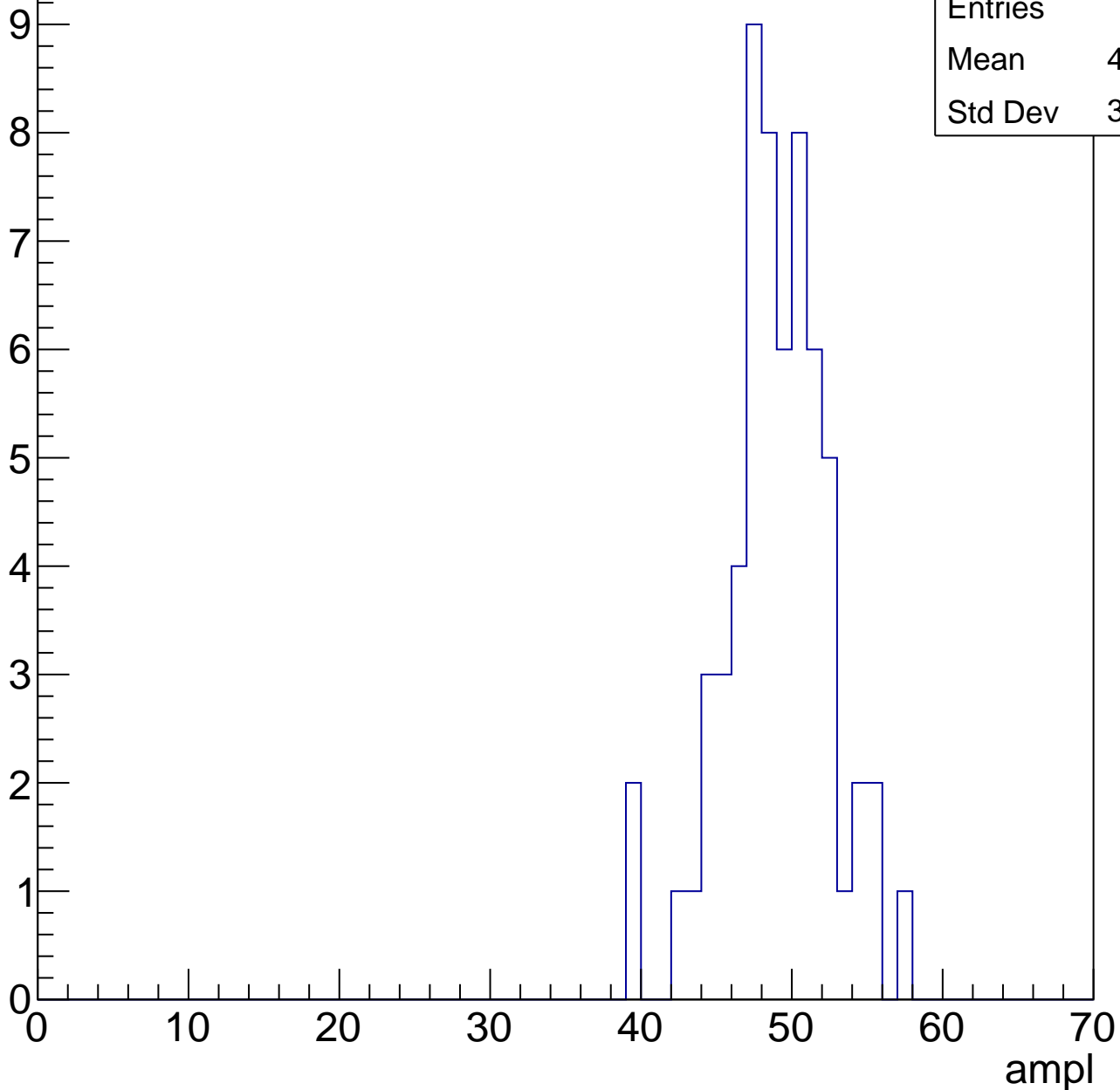


B1L103S, U9-ch116, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	48.53
Std Dev	3.486

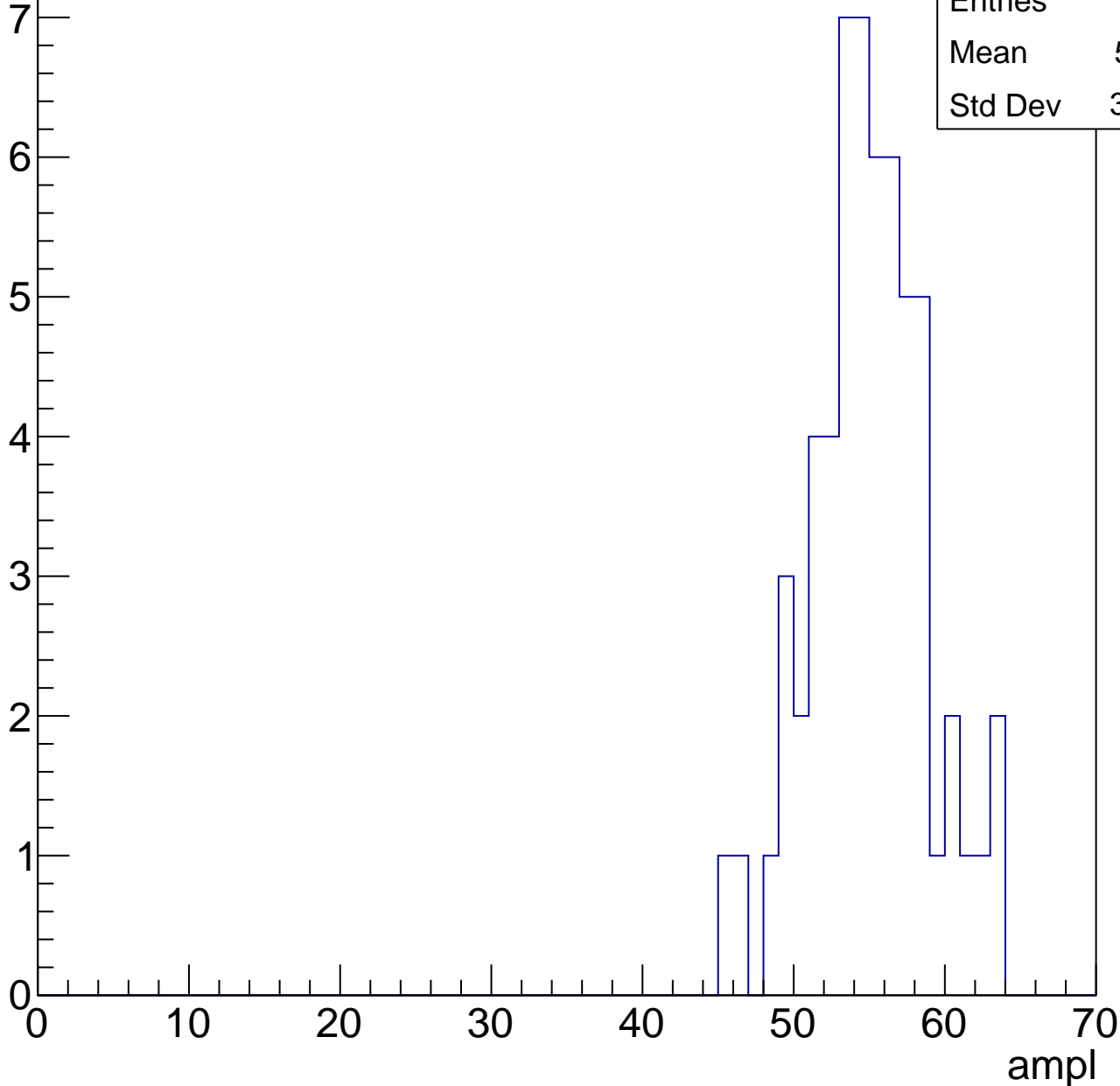


B1L103S, U9-ch116, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

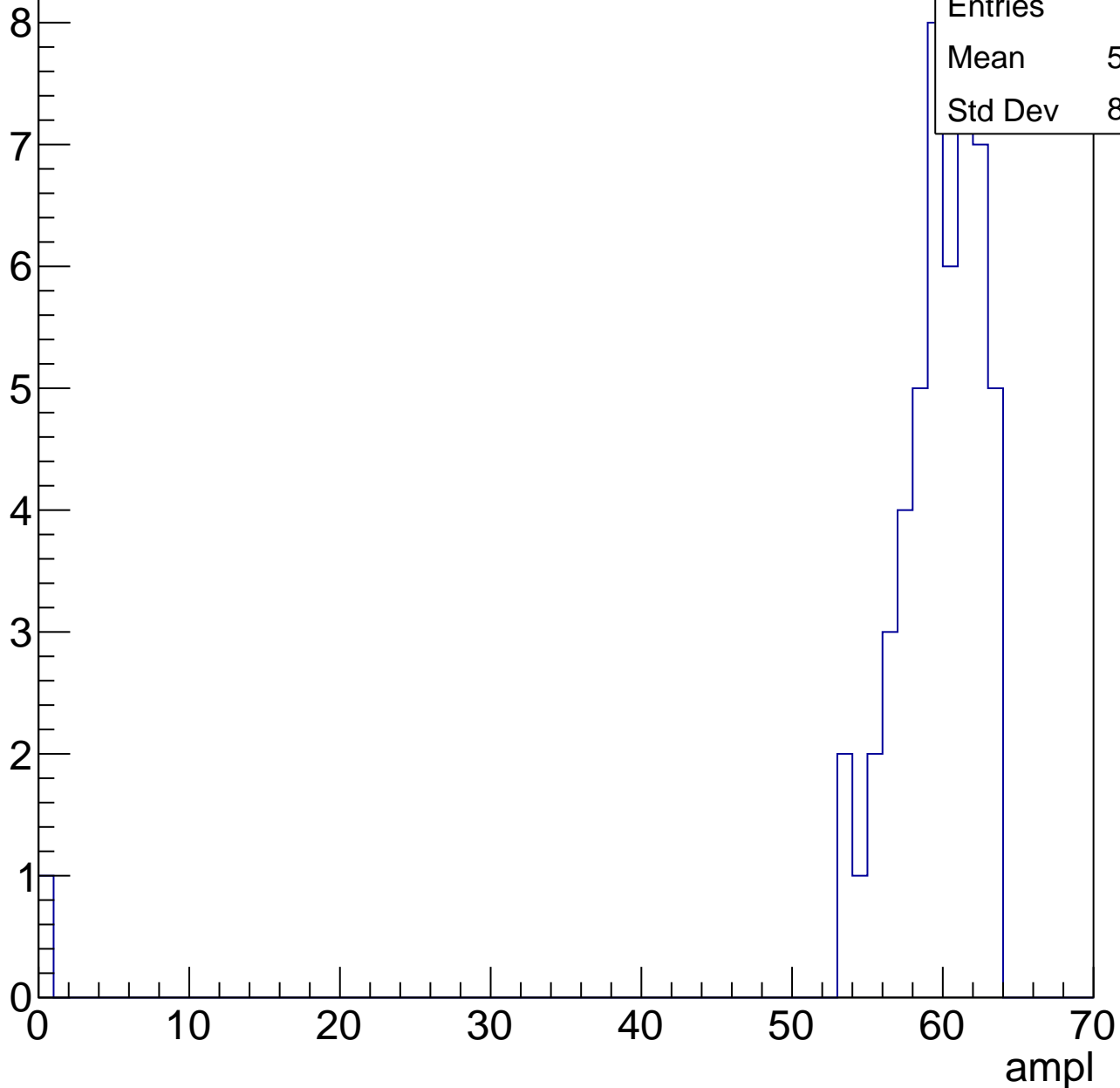
Entries	59
Mean	54.51
Std Dev	3.815



B1L103S, U9-ch116, adc5

calib_packv5_041523_1651.root, FC#0, port C2

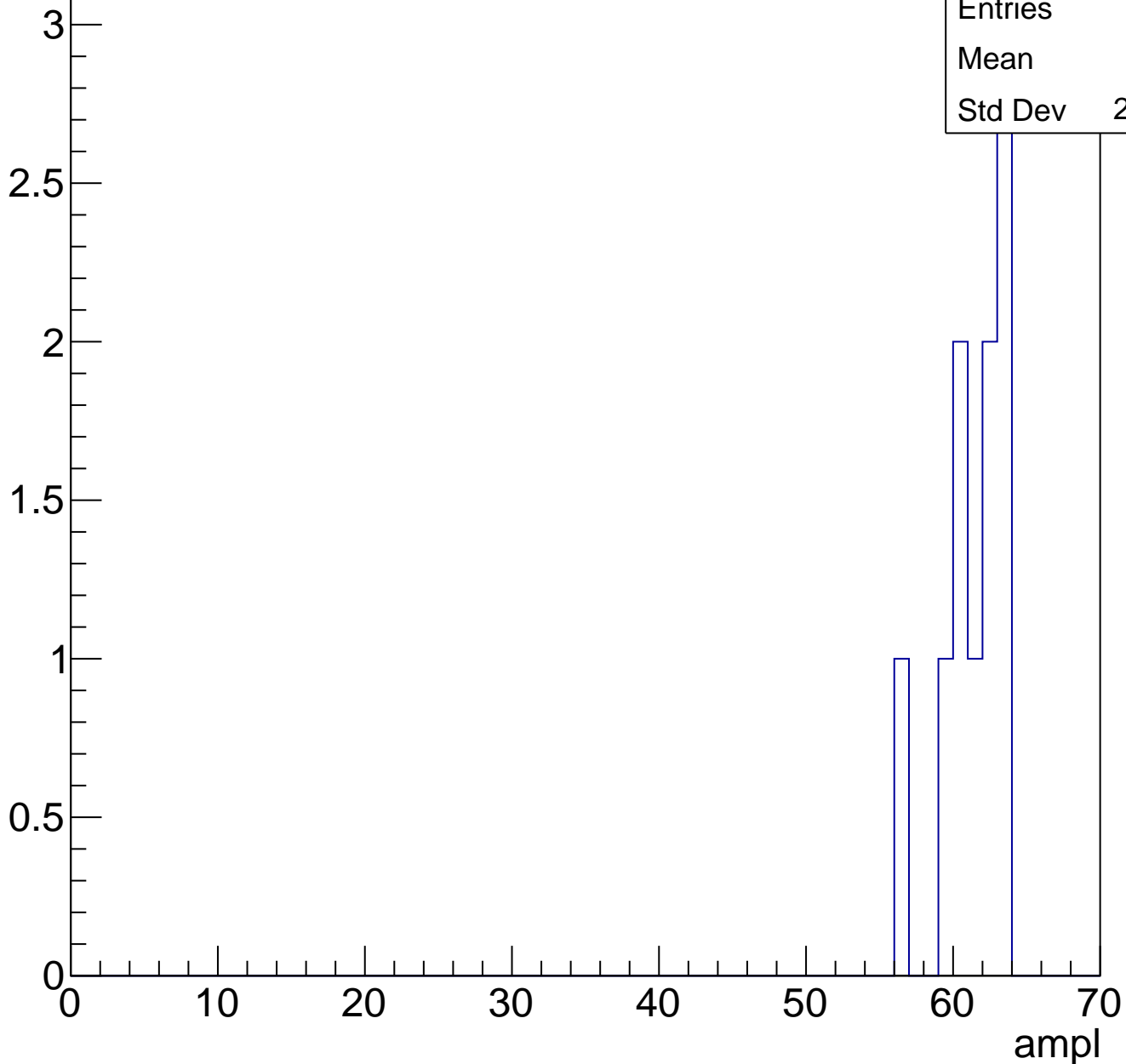
Entry



B1L103S, U9-ch116, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch116, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

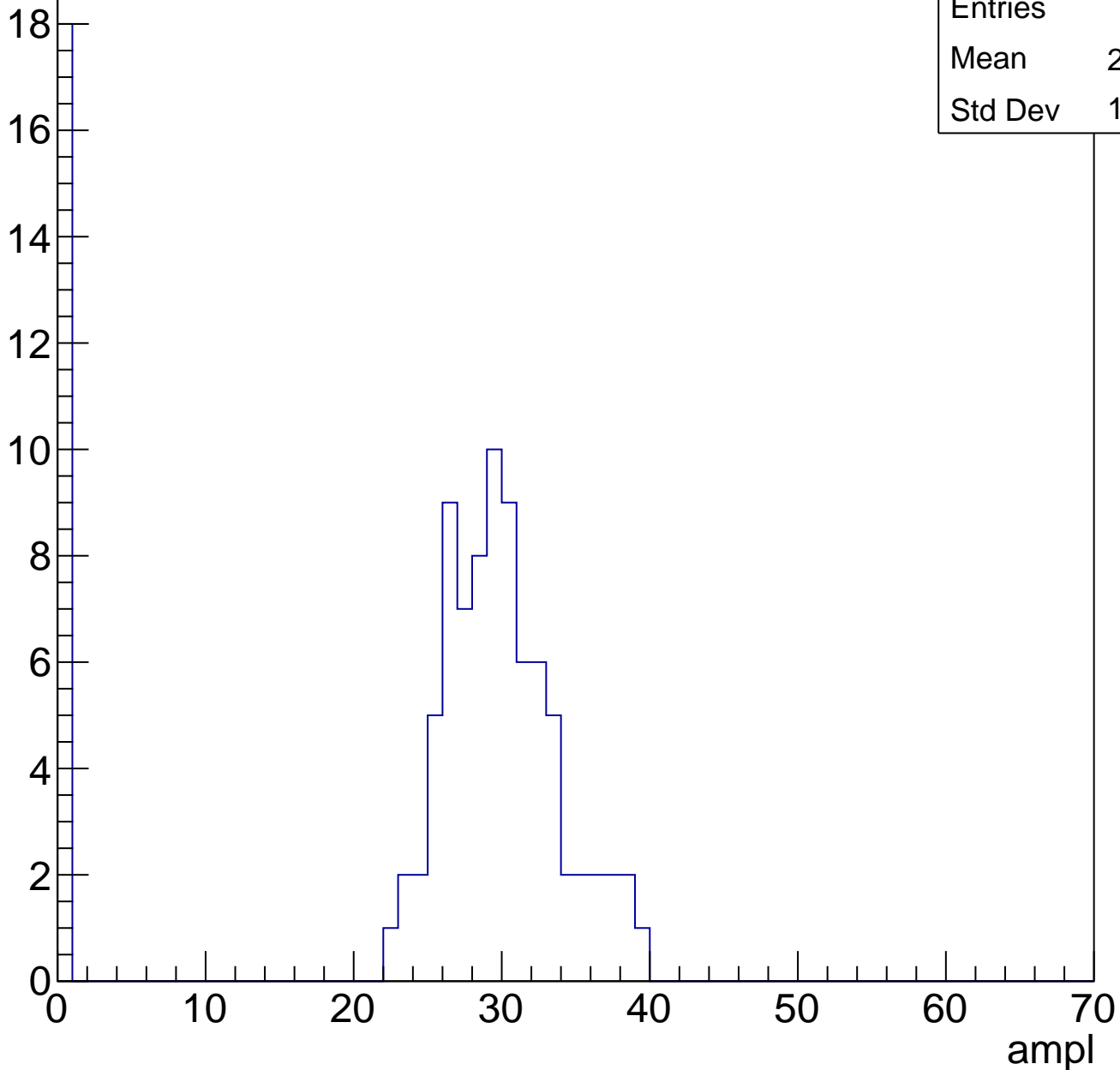


B1L103S, U9-ch117, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	99
Mean	24.14
Std Dev	11.87

Entry

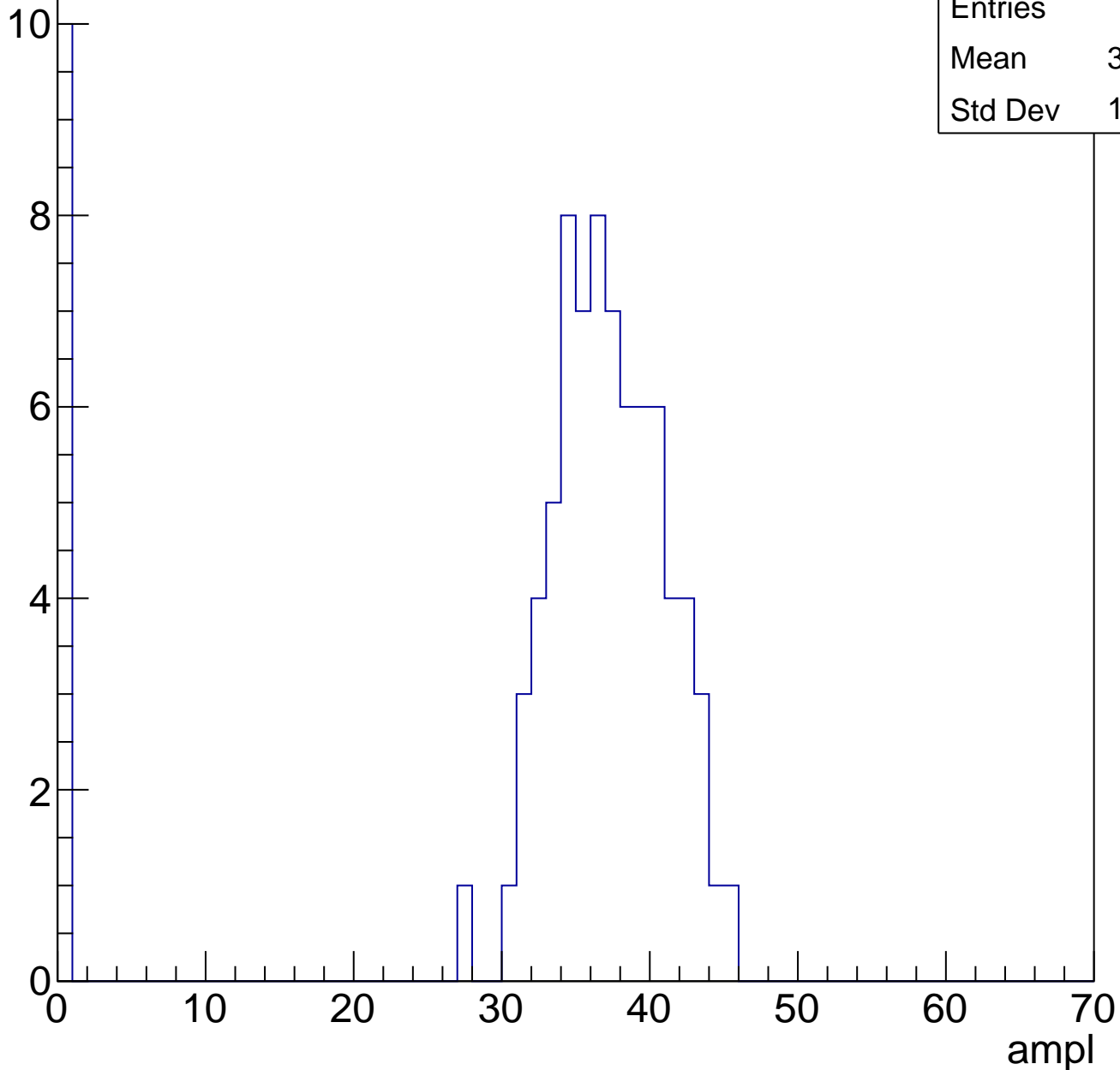


B1L103S, U9-ch117, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	85
Mean	32.46
Std Dev	12.34

Entry

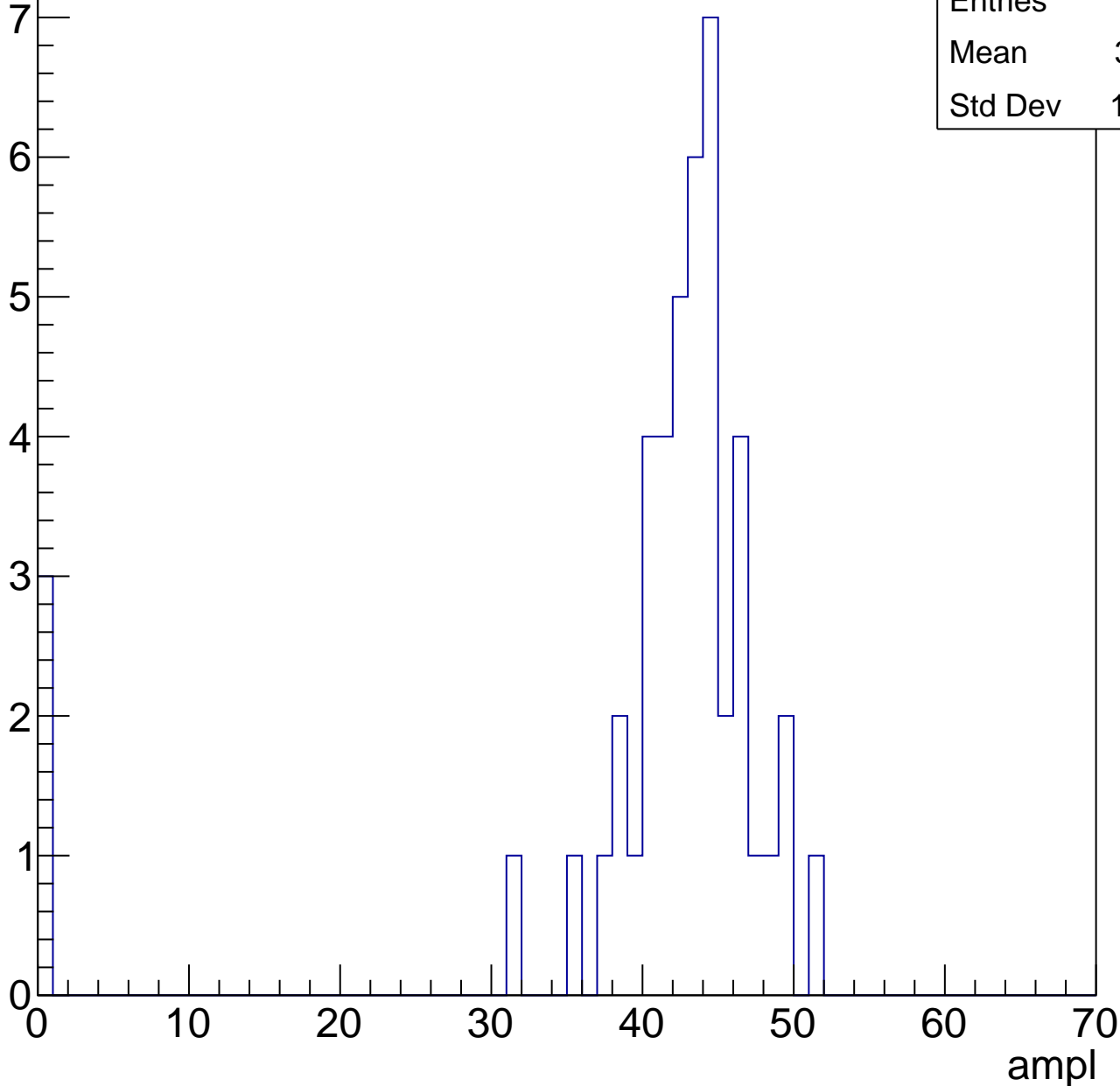


B1L103S, U9-ch117, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	46
Mean	39.91
Std Dev	11.14

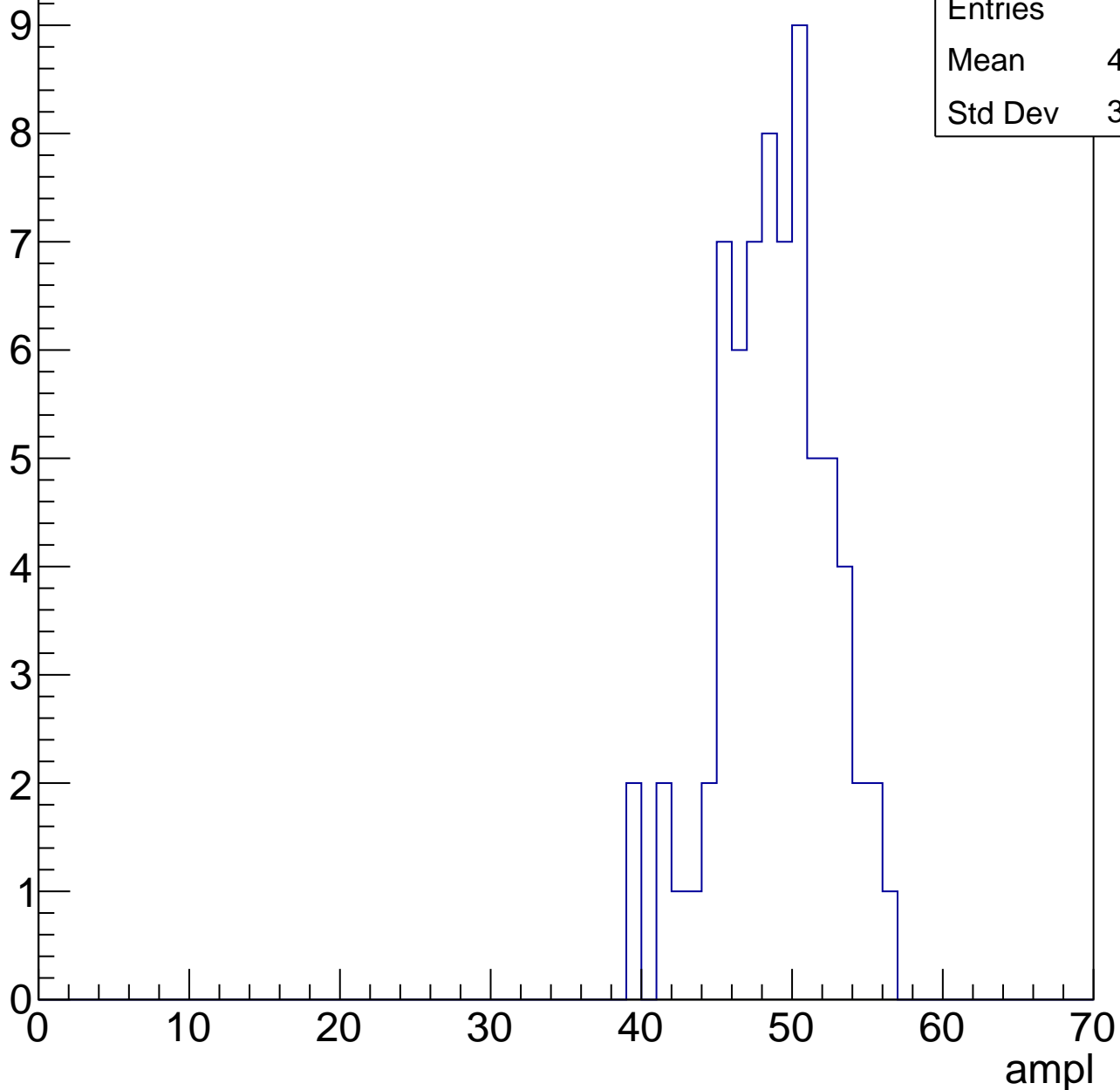


B1L103S, U9-ch117, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	48.32
Std Dev	3.642

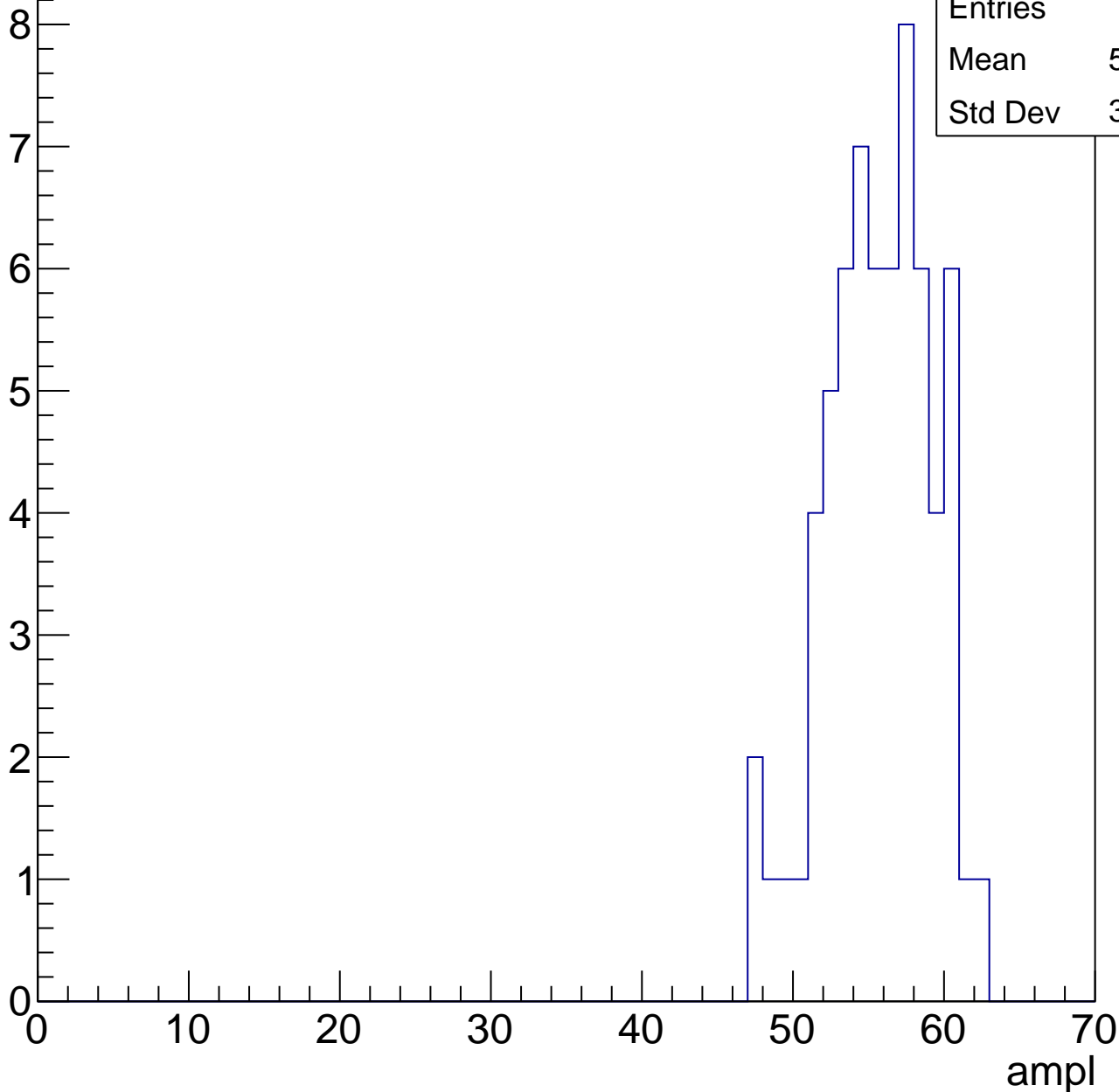


B1L103S, U9-ch117, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	55.23
Std Dev	3.432

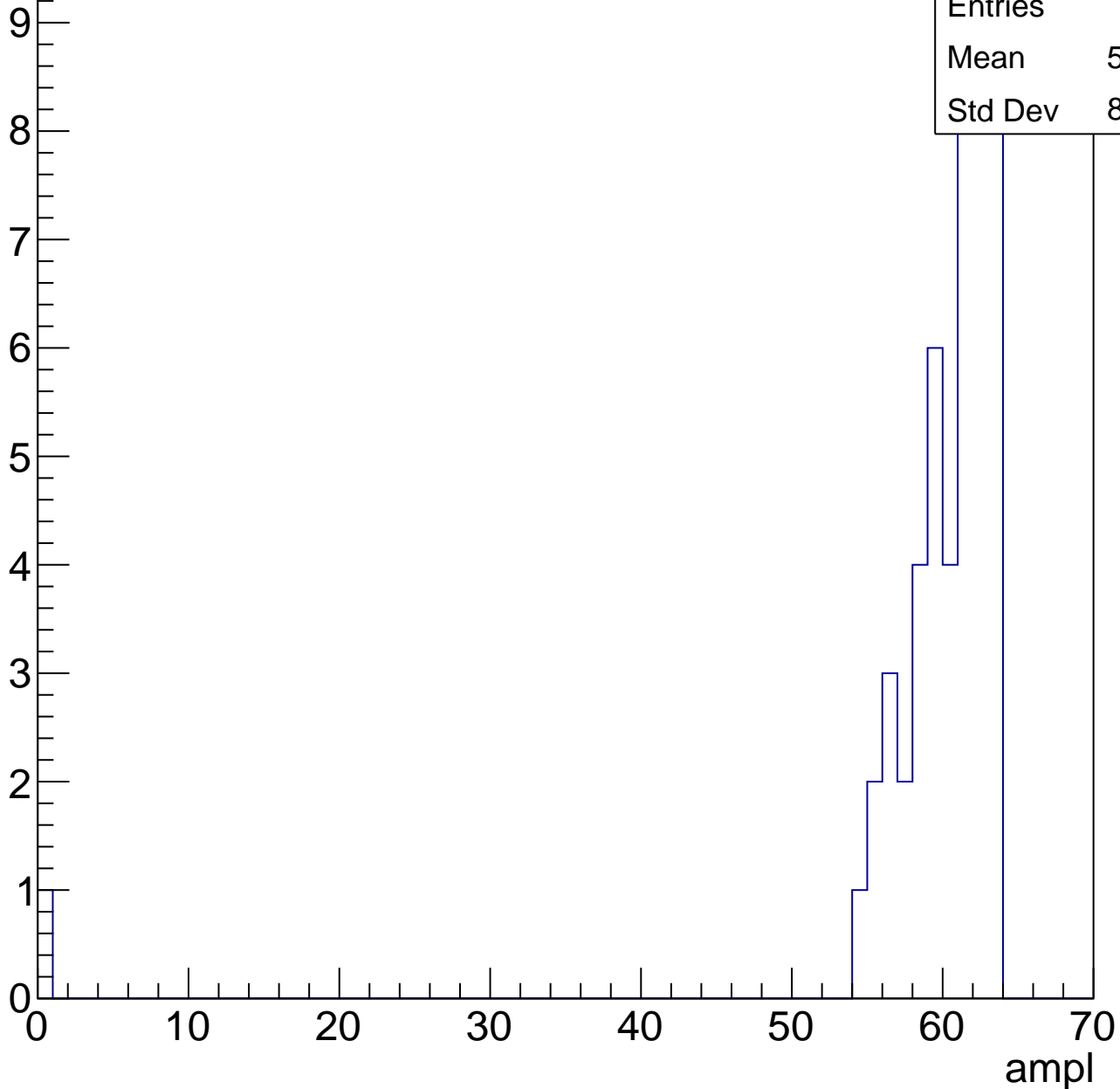


B1L103S, U9-ch117, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	58.88
Std Dev	8.849



B1L103S, U9-ch117, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	2
Mean	62
Std Dev	1

B1L103S, U9-ch117, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

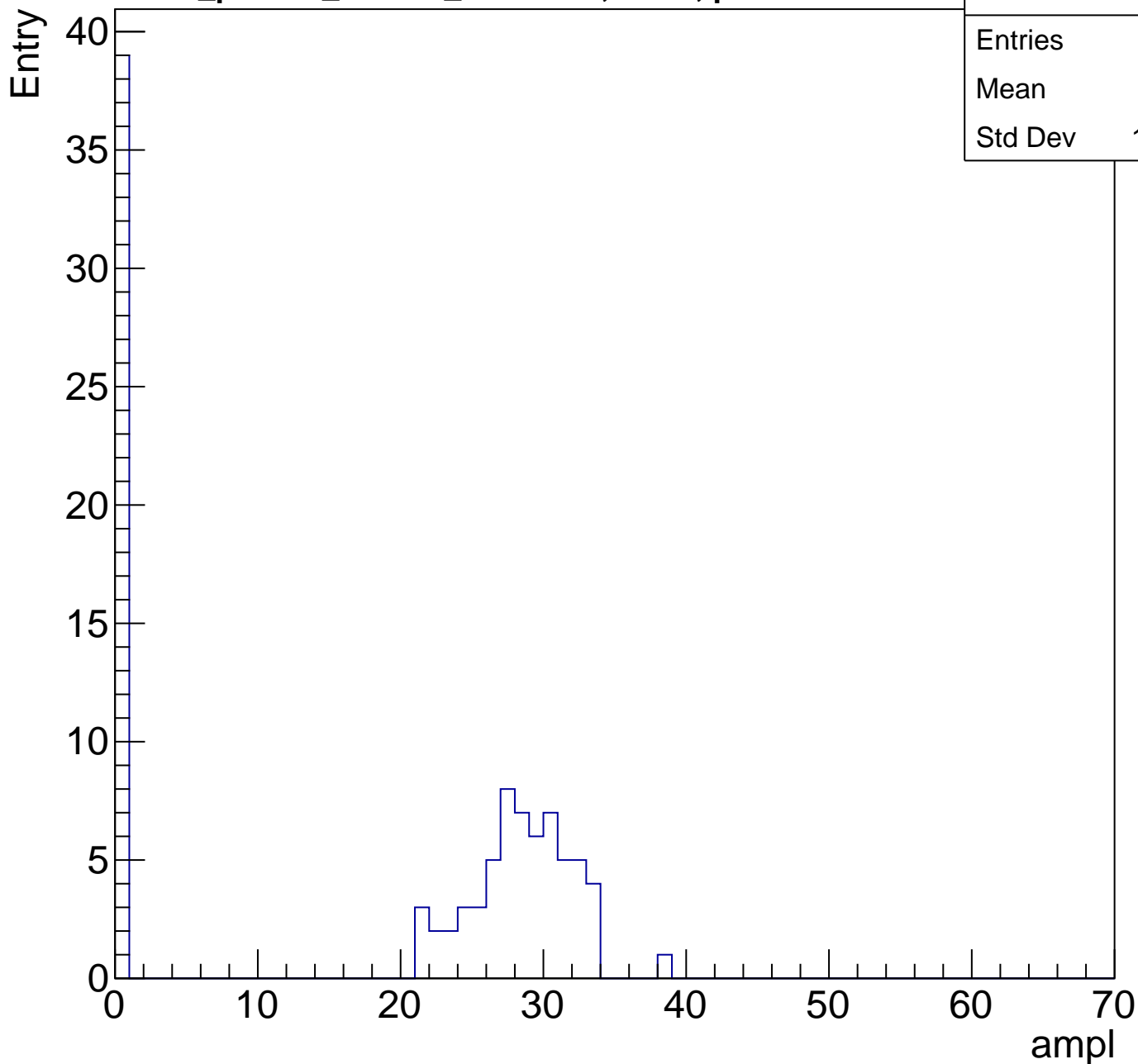
ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U9-ch118, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	100
Mean	17.11
Std Dev	13.95



B1L103S, U9-ch118, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	31.81
Std Dev	10.61

Entry

10
8
6
4
2
0

0

10

20

30

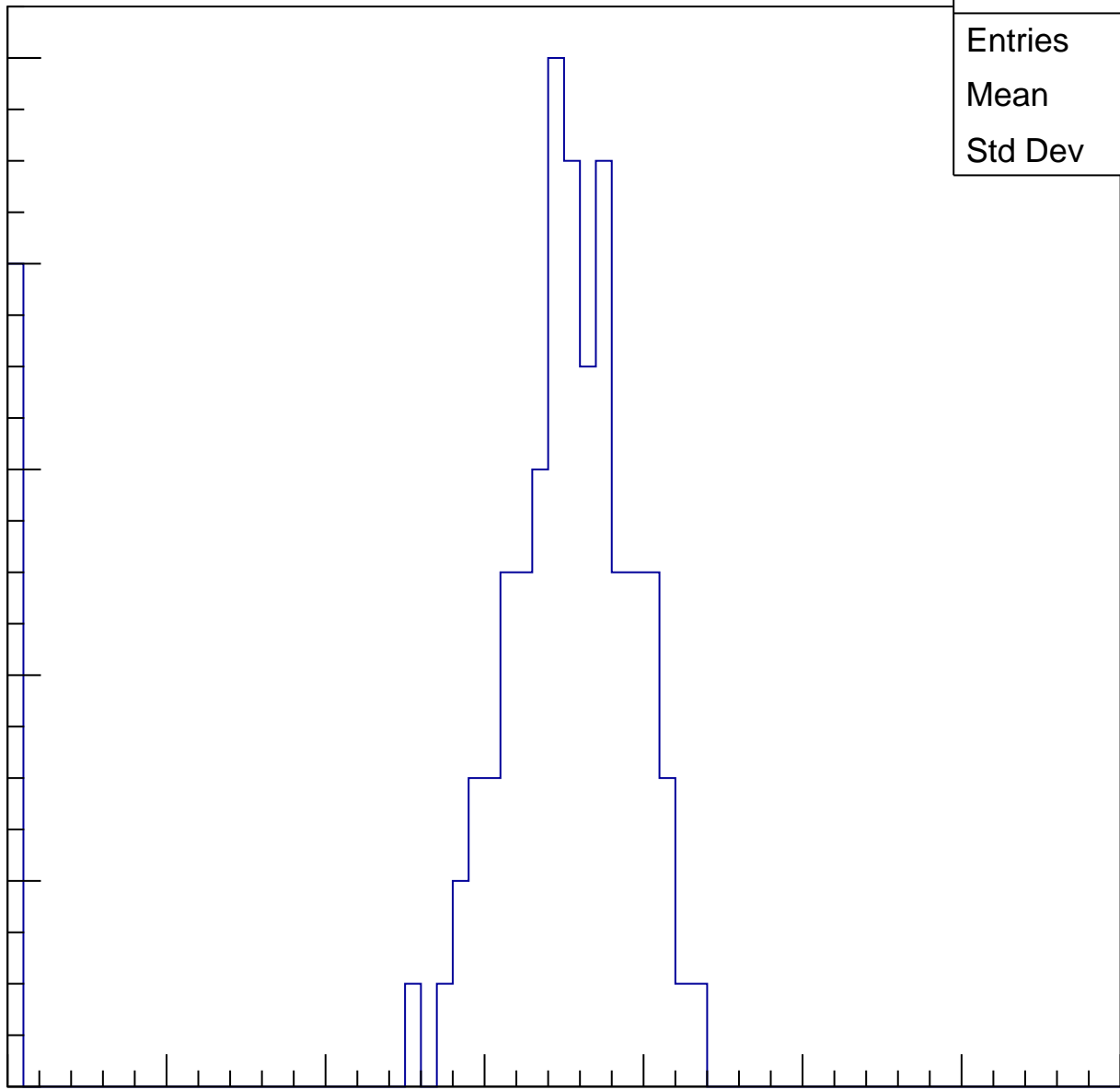
40

50

60

70

ampl

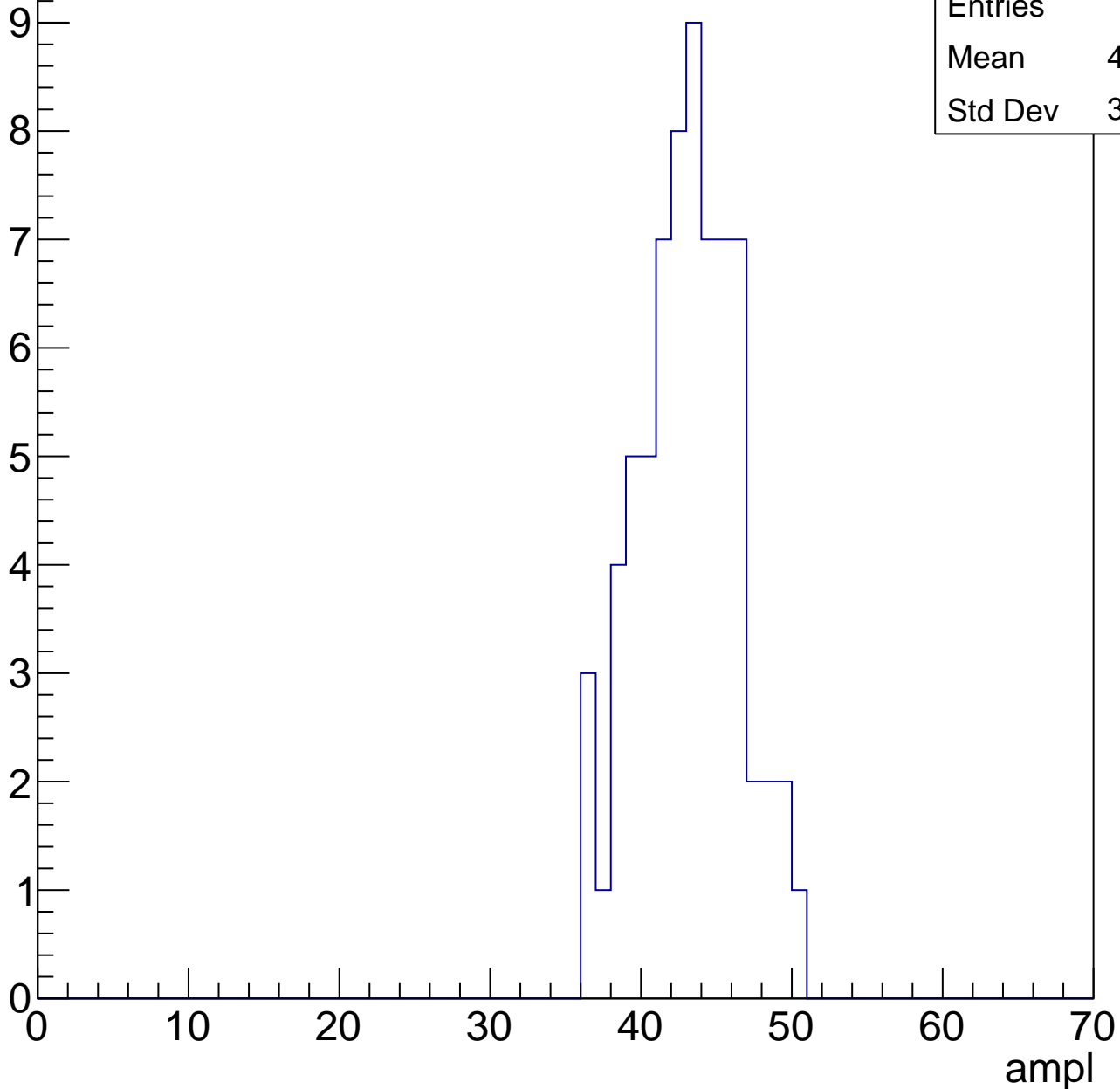


B1L103S, U9-ch118, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	42.64
Std Dev	3.243

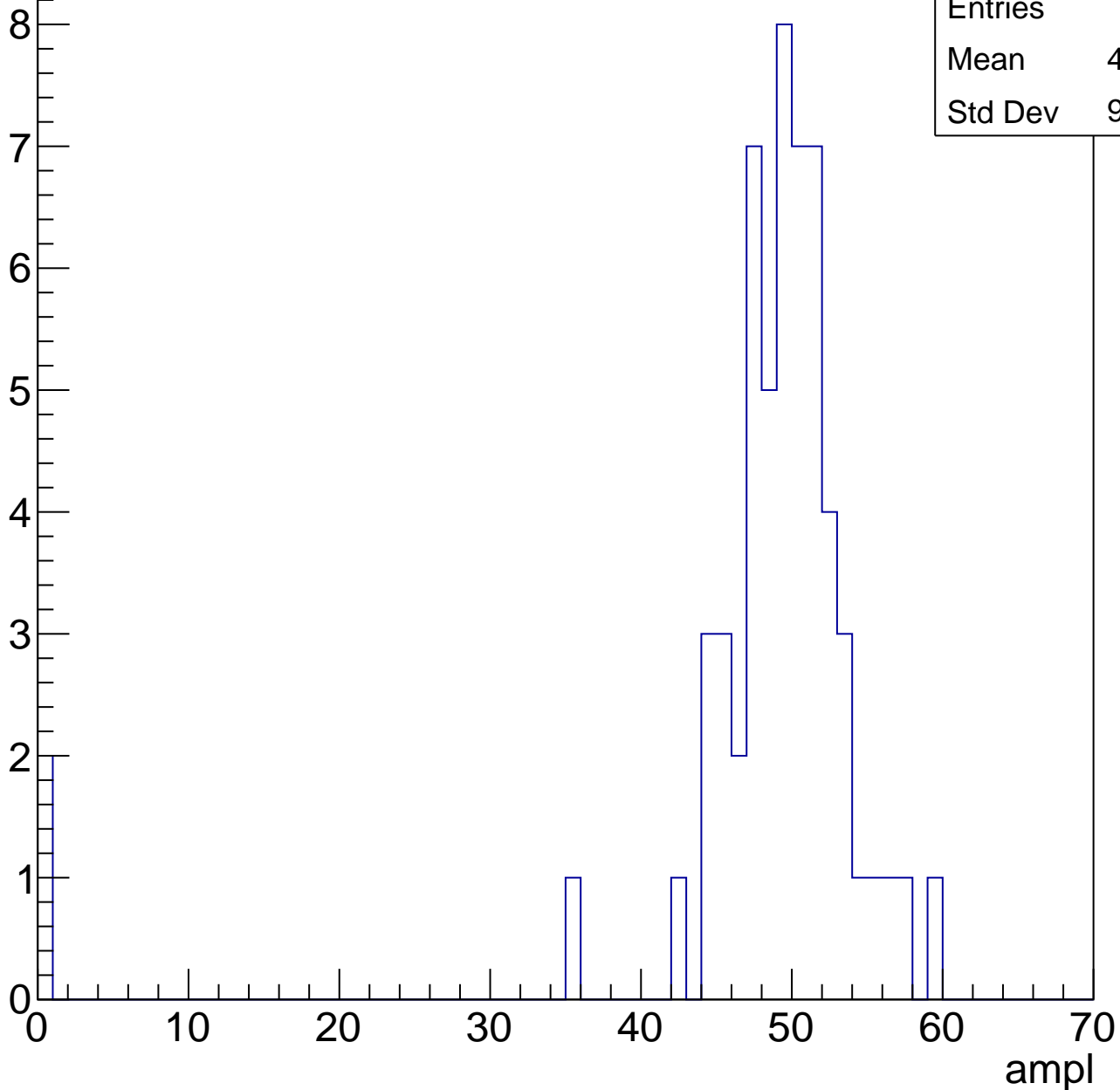


B1L103S, U9-ch118, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	47.45
Std Dev	9.715

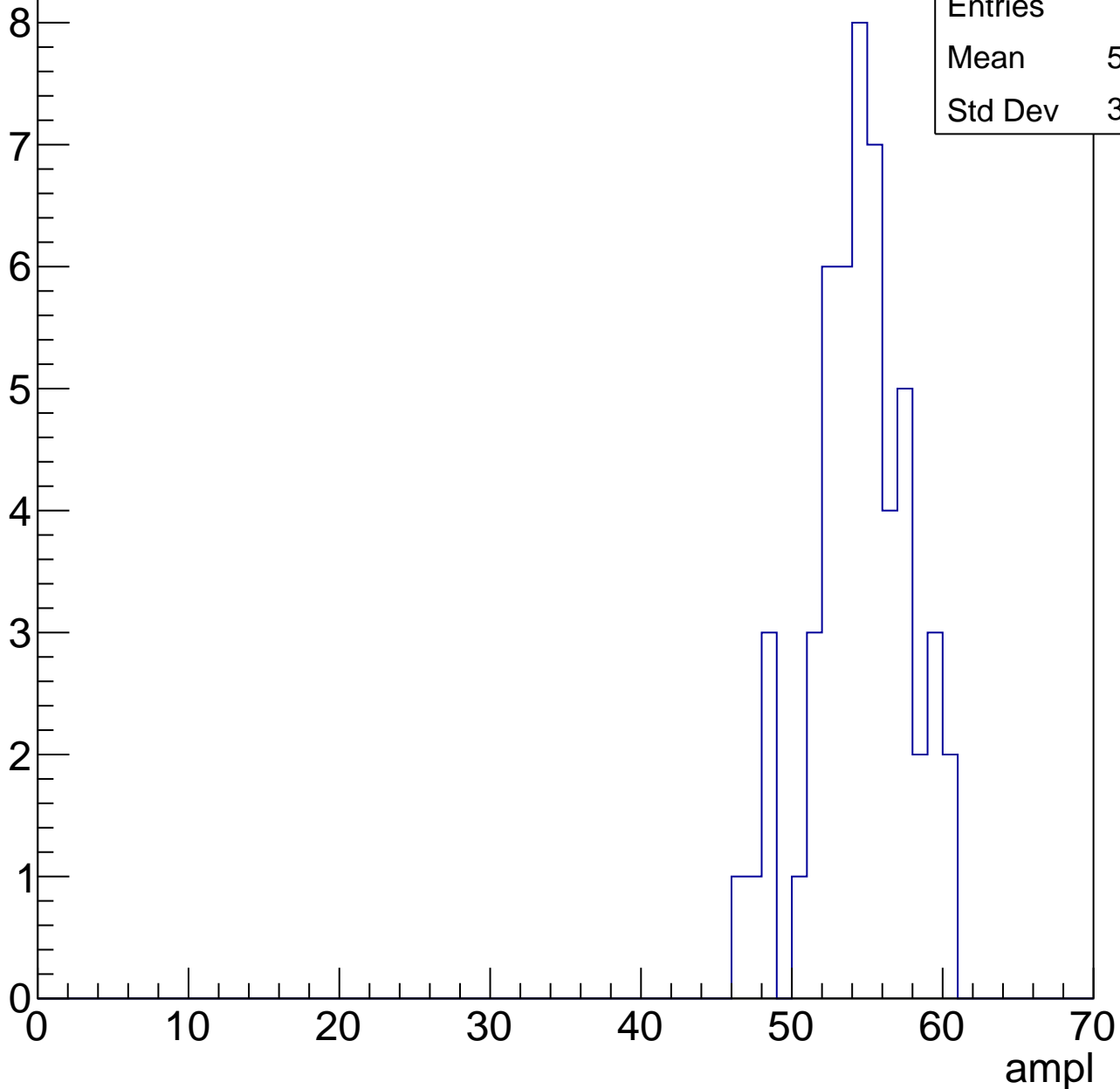


B1L103S, U9-ch118, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	54.02
Std Dev	3.225

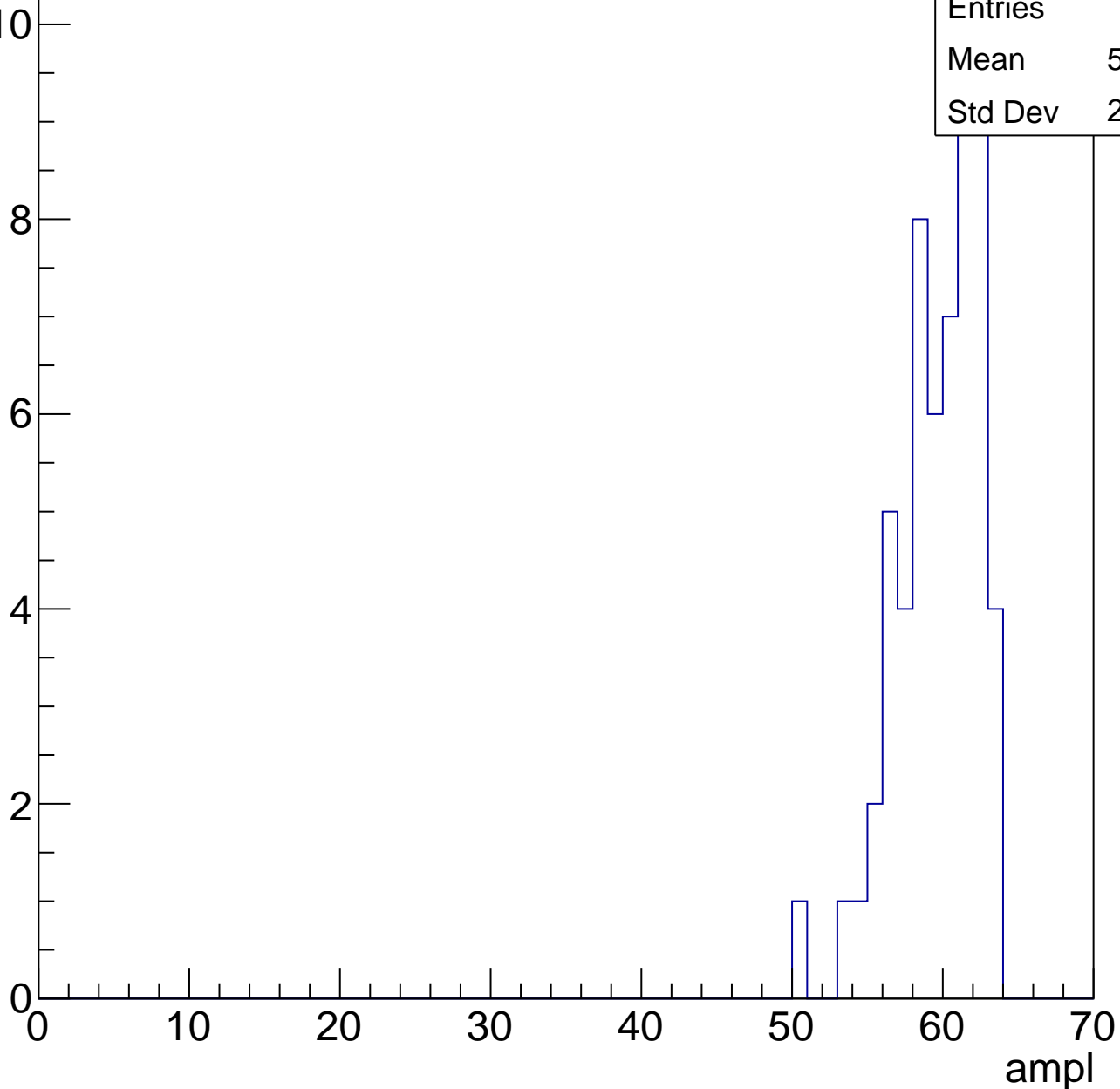


B1L103S, U9-ch118, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

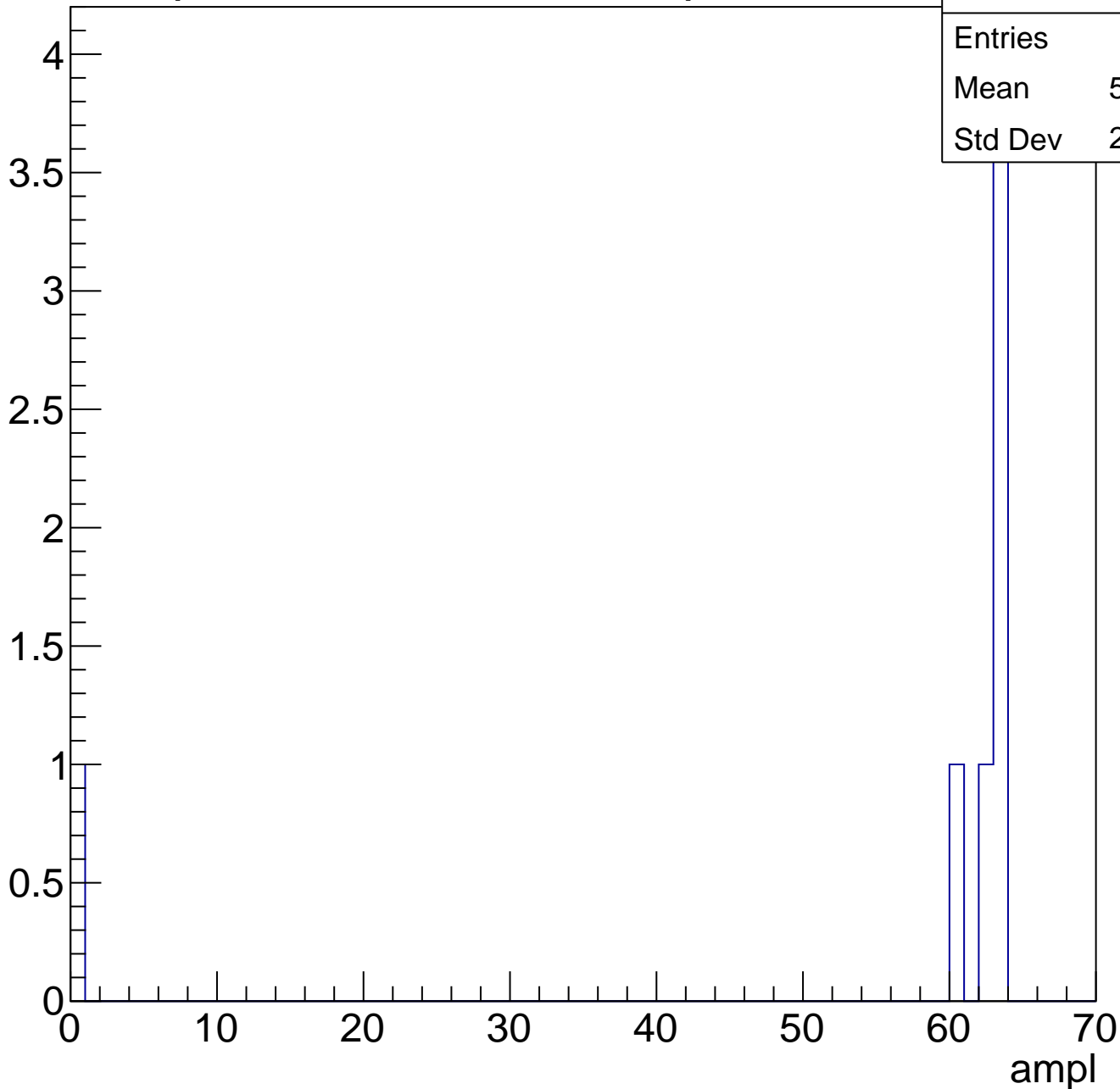
Entries	58
Mean	59.19
Std Dev	2.732



B1L103S, U9-ch118, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch118, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	6
Std Dev	18.49

Entry

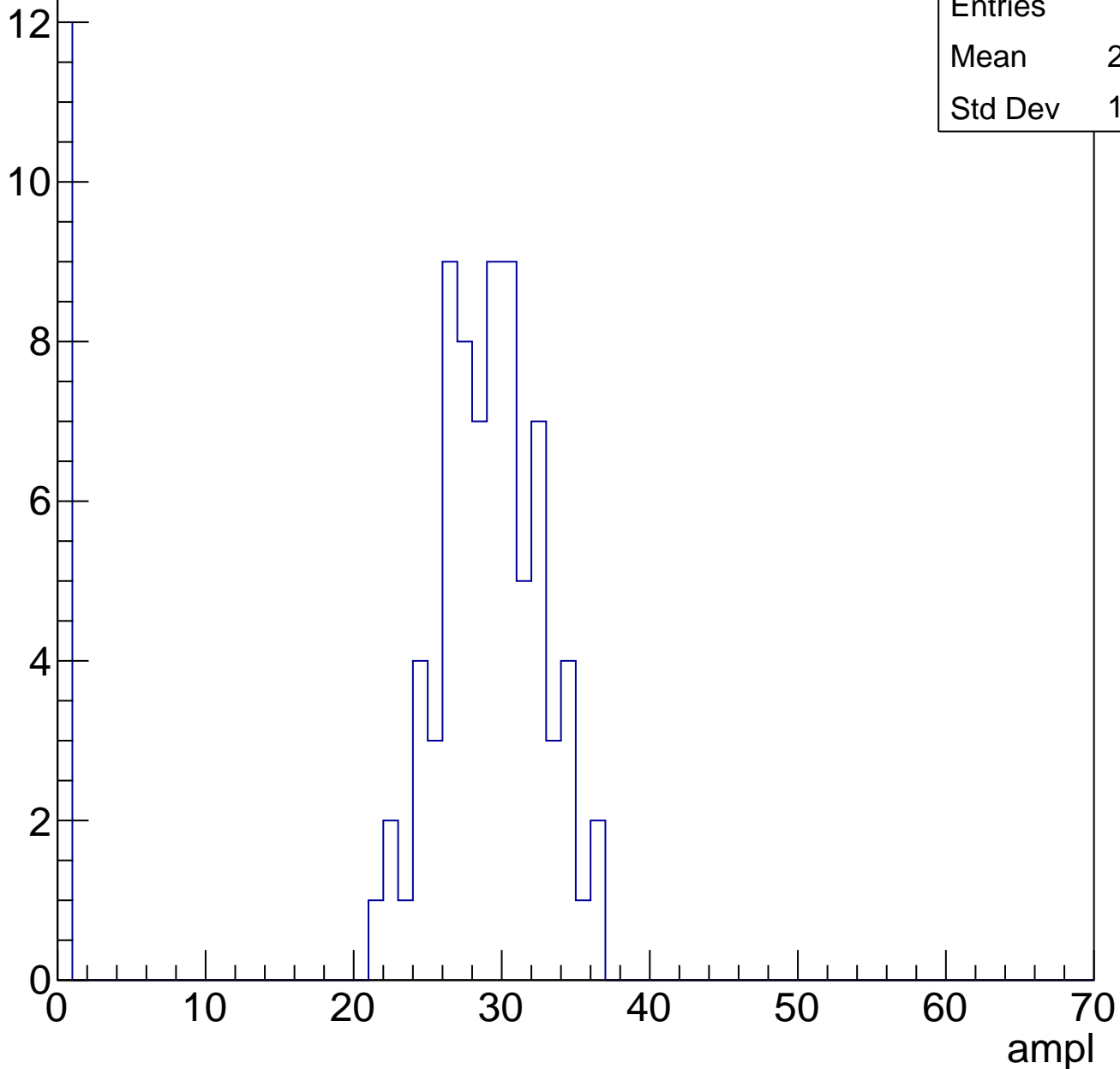


B1L103S, U9-ch119, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	87
Mean	24.79
Std Dev	10.39

Entry

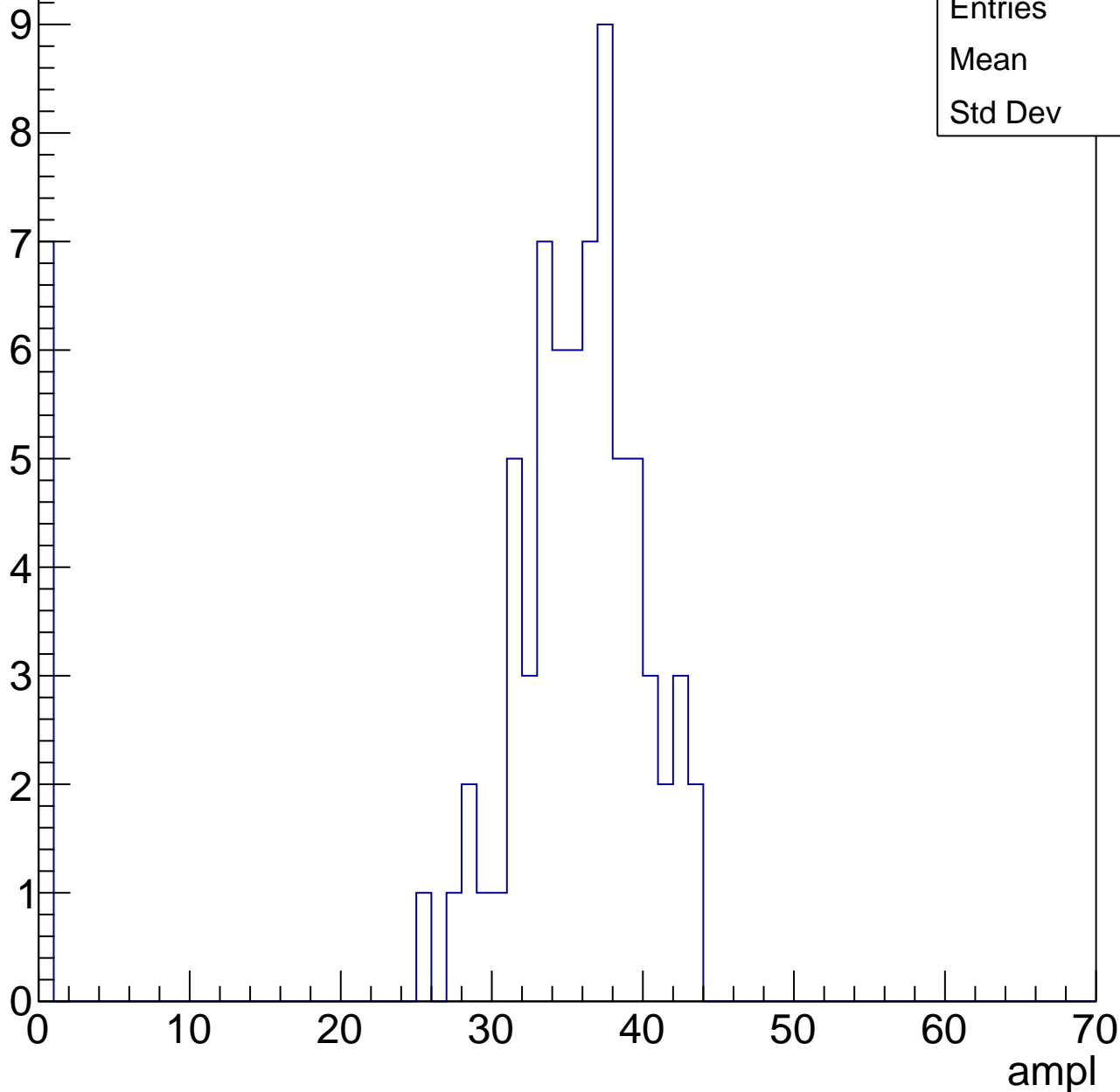


B1L103S, U9-ch119, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	32.2
Std Dev	10.9

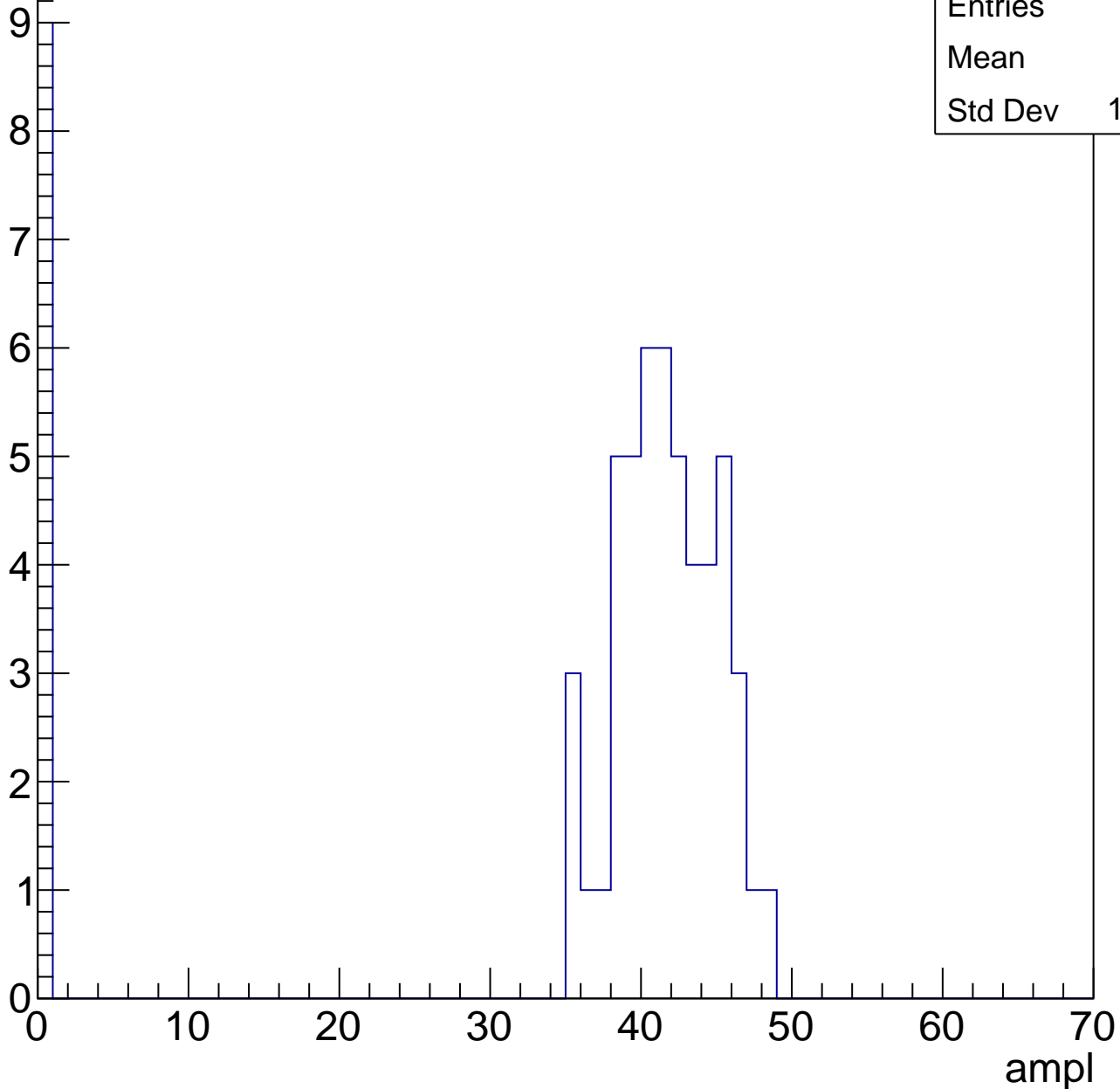


B1L103S, U9-ch119, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	35
Std Dev	15.14

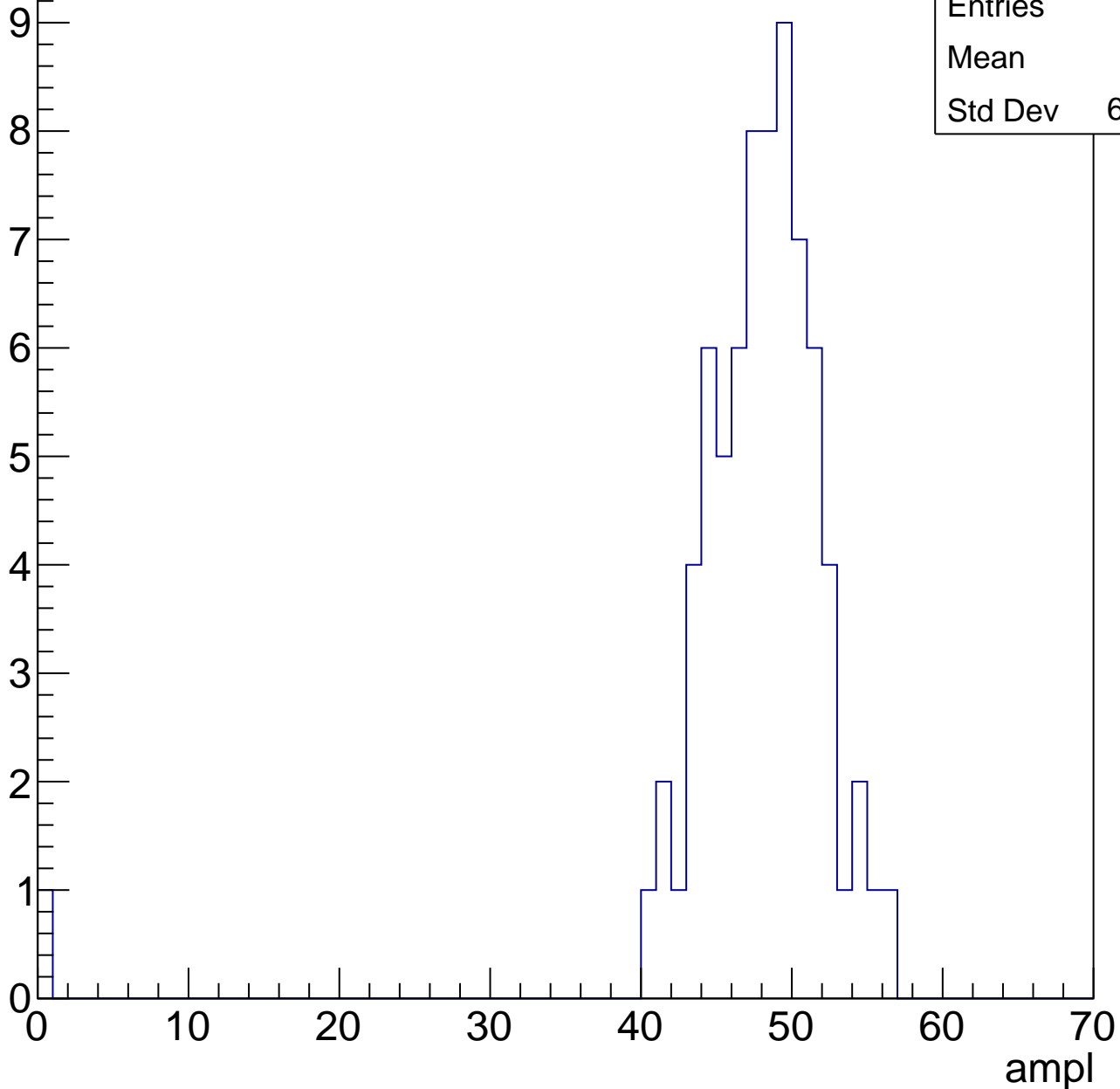


B1L103S, U9-ch119, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

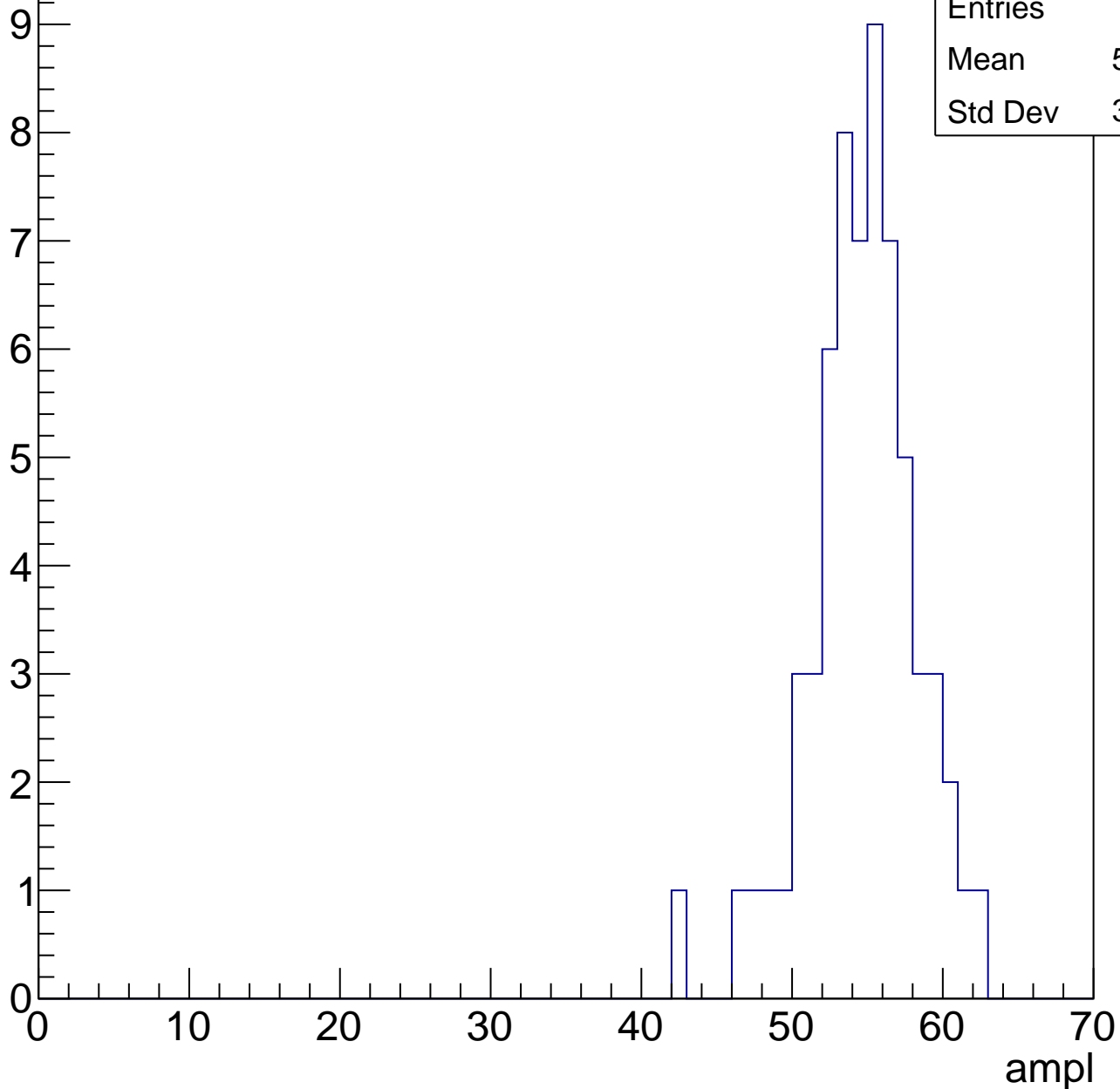
Entries	73
Mean	47.1
Std Dev	6.496



B1L103S, U9-ch119, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

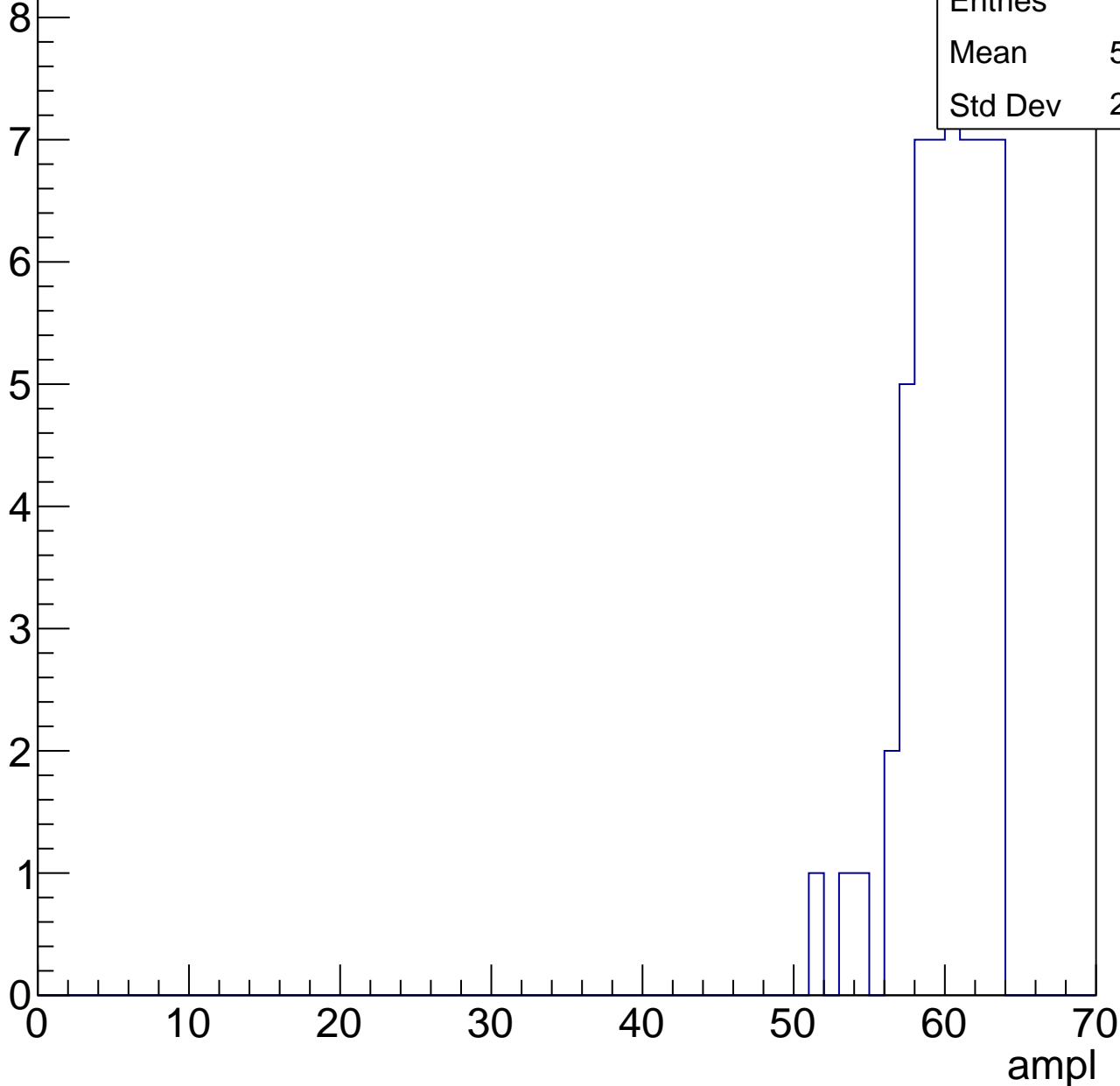


B1L103S, U9-ch119, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	59.55
Std Dev	2.625



B1L103S, U9-ch119, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch119, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

20
18
16
14
12
10
8
6
4
2
0

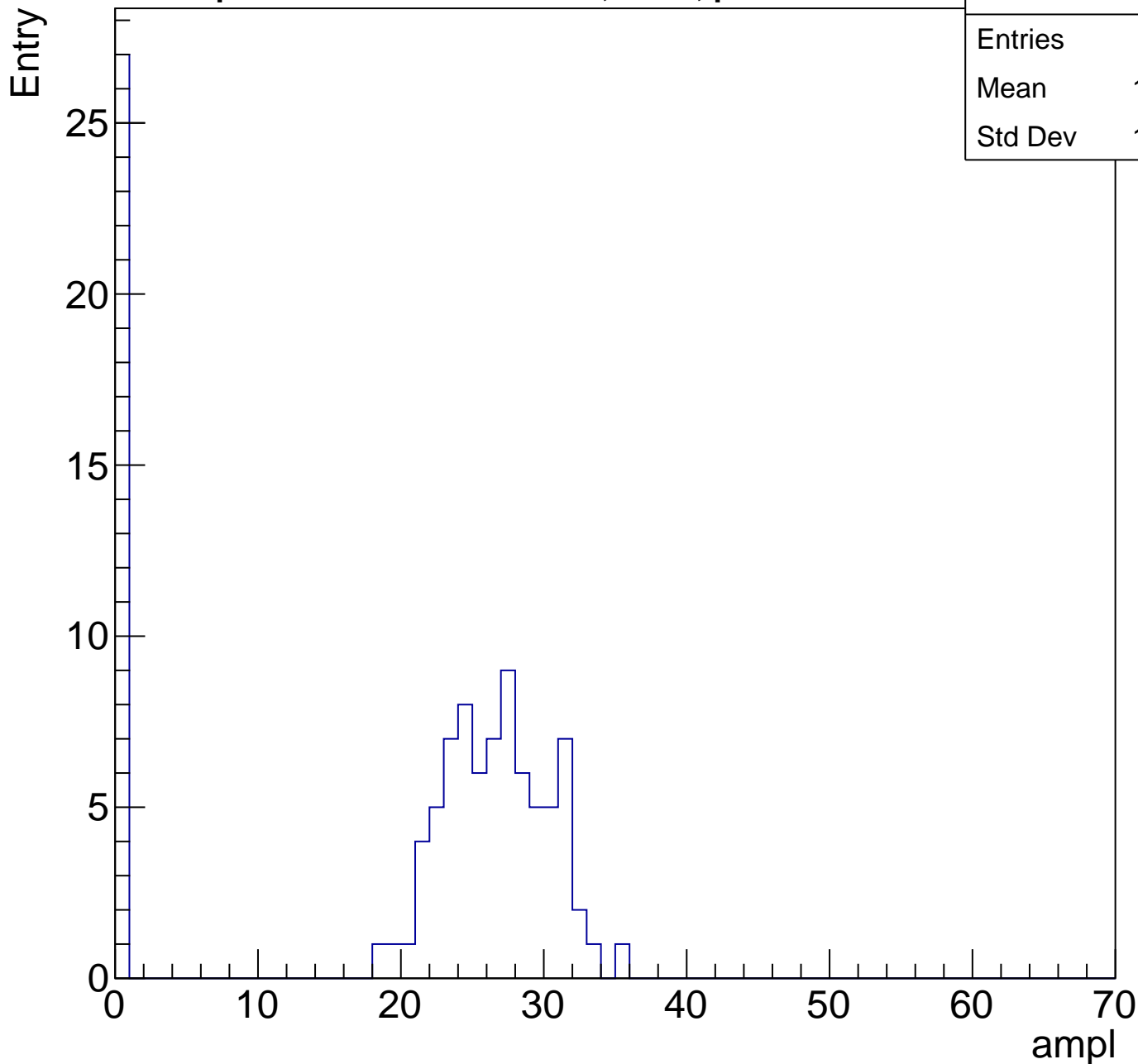
Entries	20
Mean	0
Std Dev	0

ampl

B1L103S, U9-ch120, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	103
Mean	19.33
Std Dev	11.92

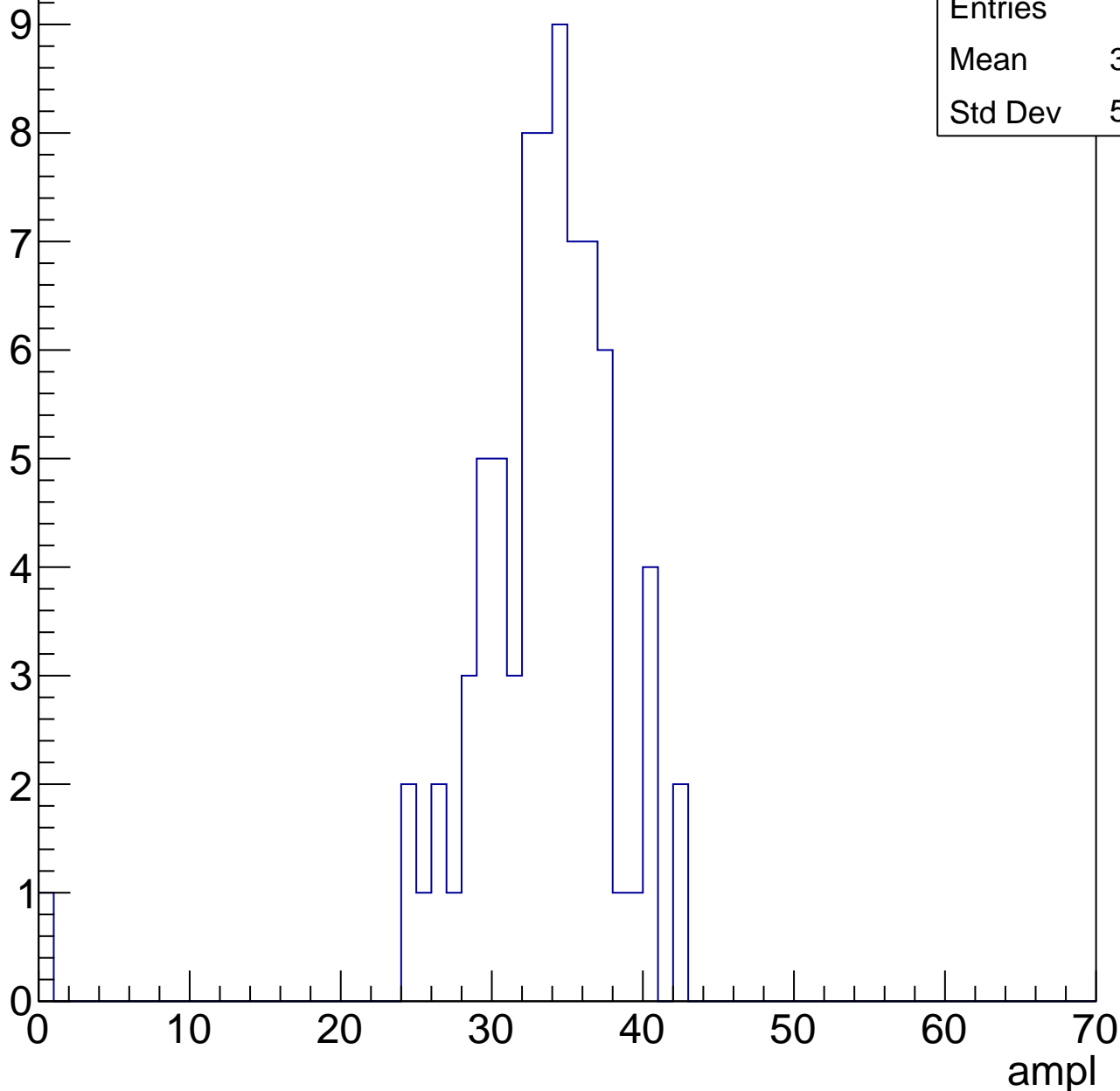


B1L103S, U9-ch120, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	32.76
Std Dev	5.477

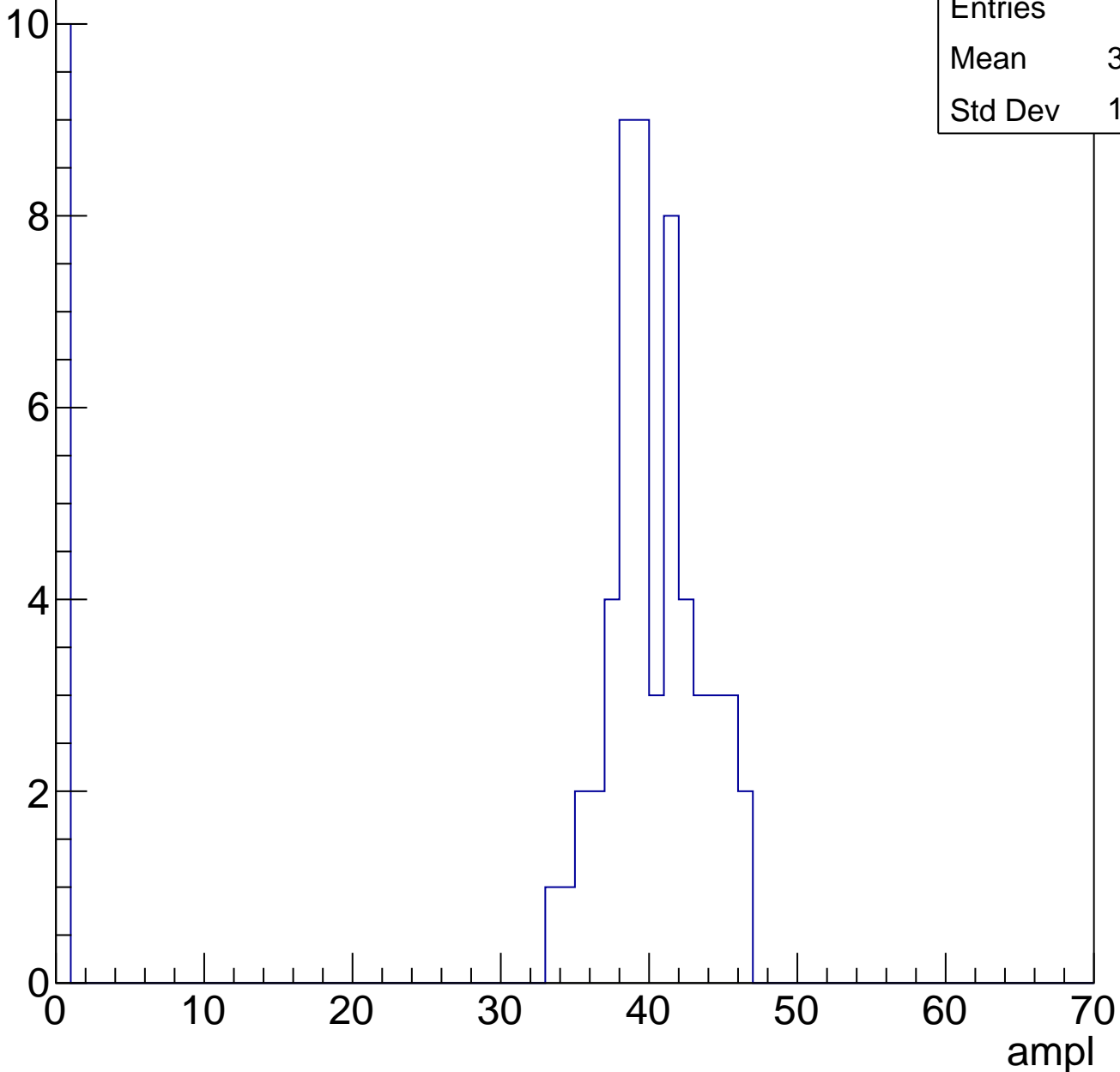


B1L103S, U9-ch120, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	64
Mean	33.66
Std Dev	14.75

Entry

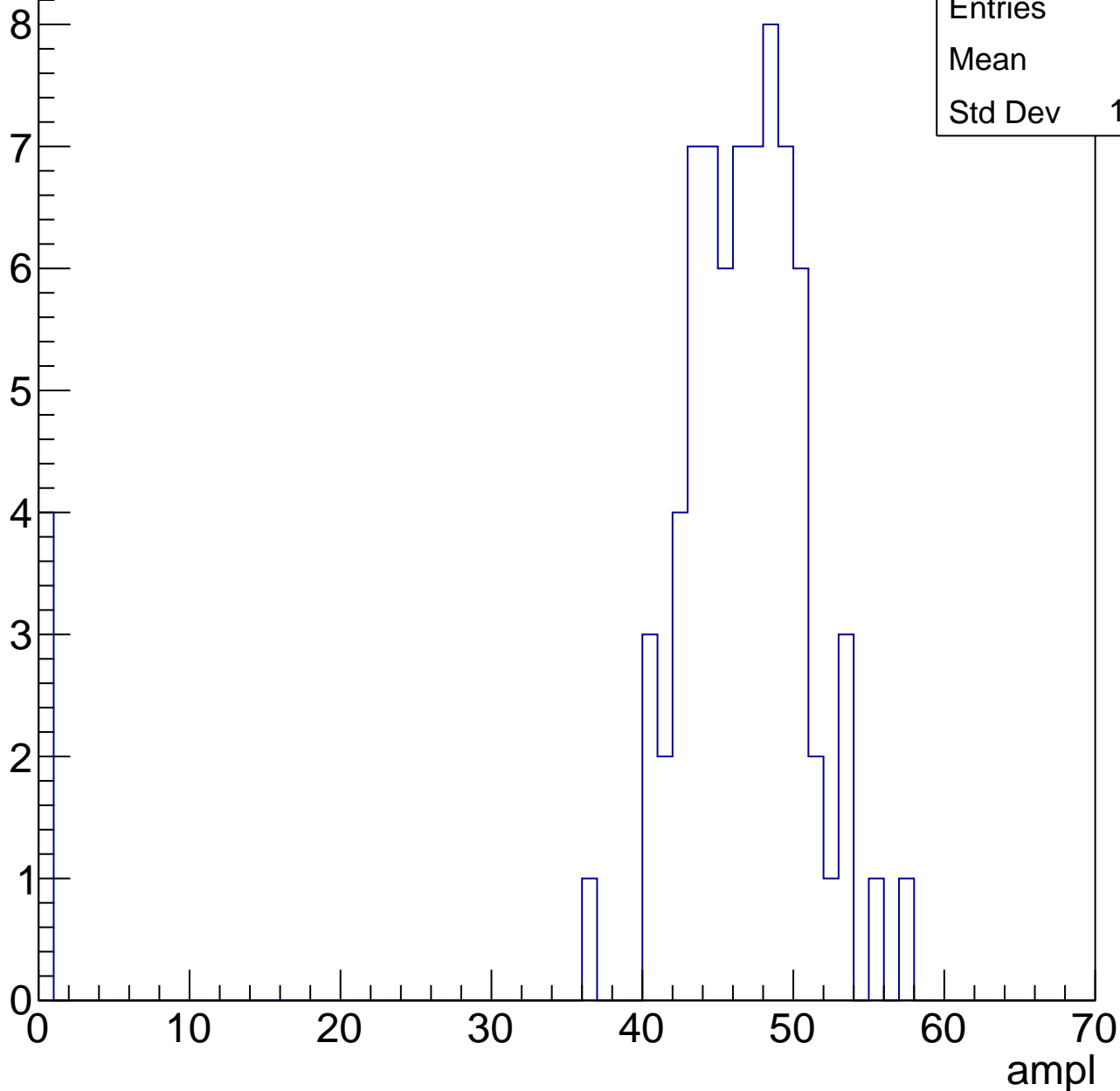


B1L103S, U9-ch120, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	44
Std Dev	10.94

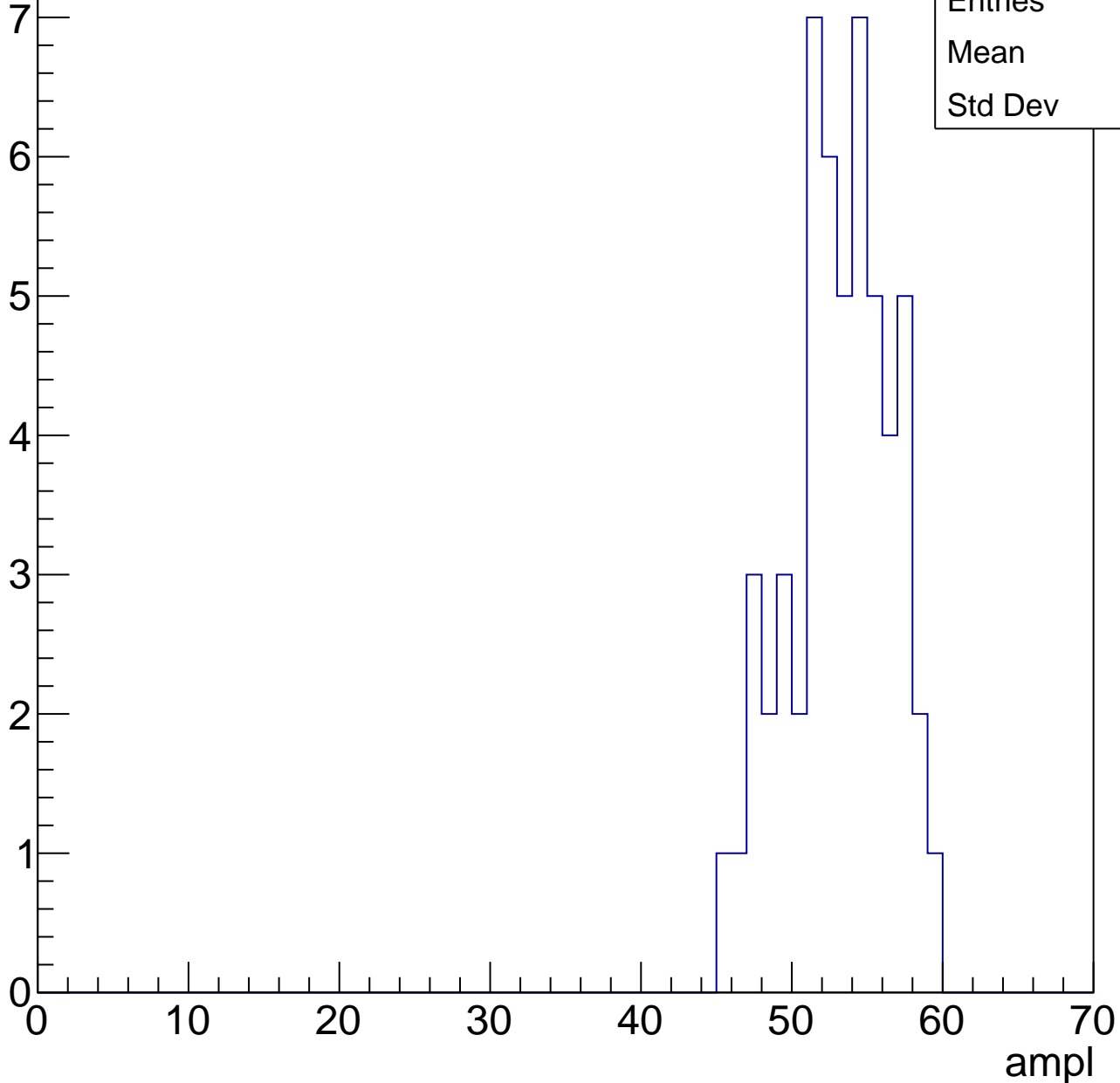


B1L103S, U9-ch120, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	52.7
Std Dev	3.32

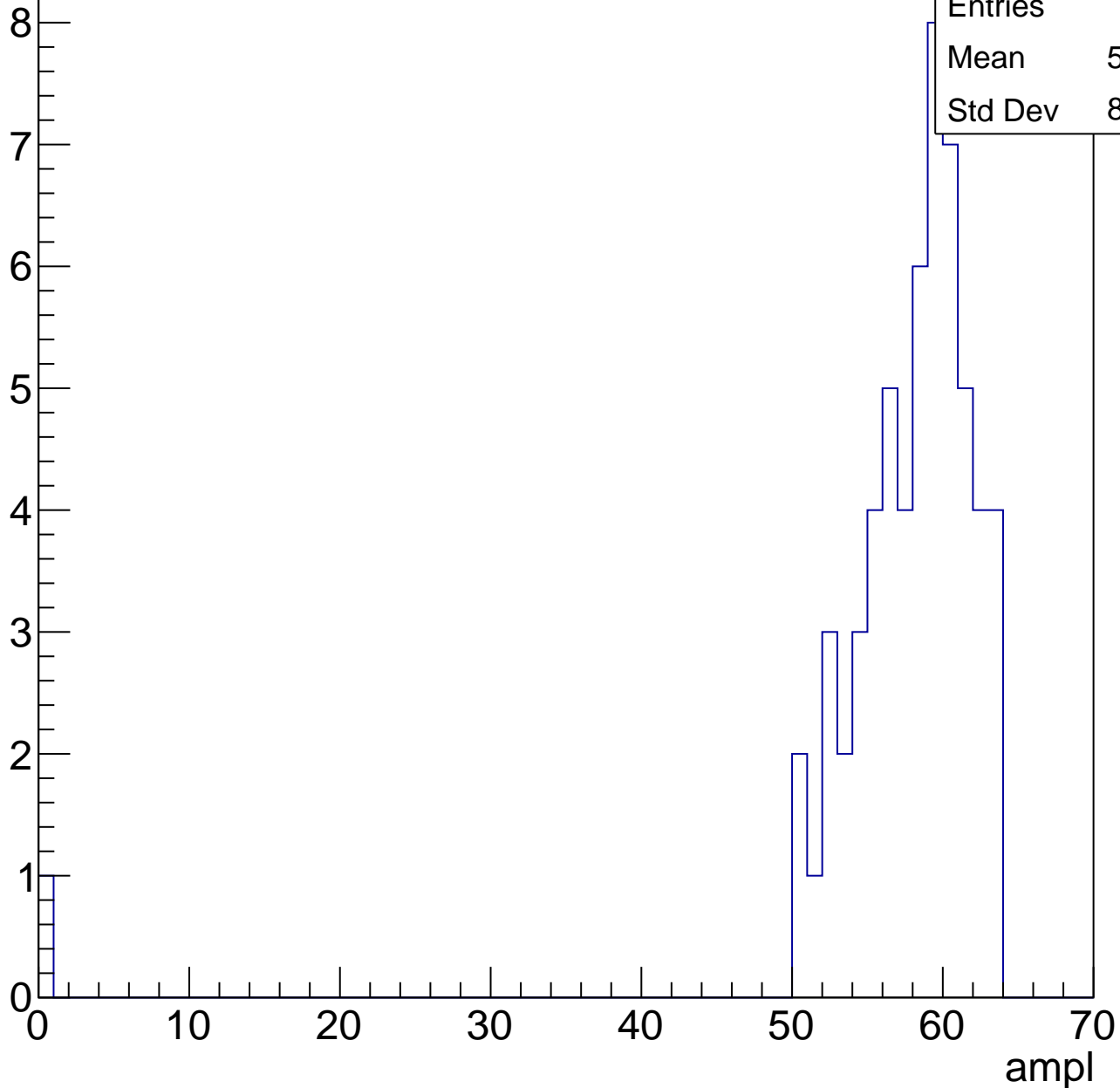


B1L103S, U9-ch120, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	56.75
Std Dev	8.192

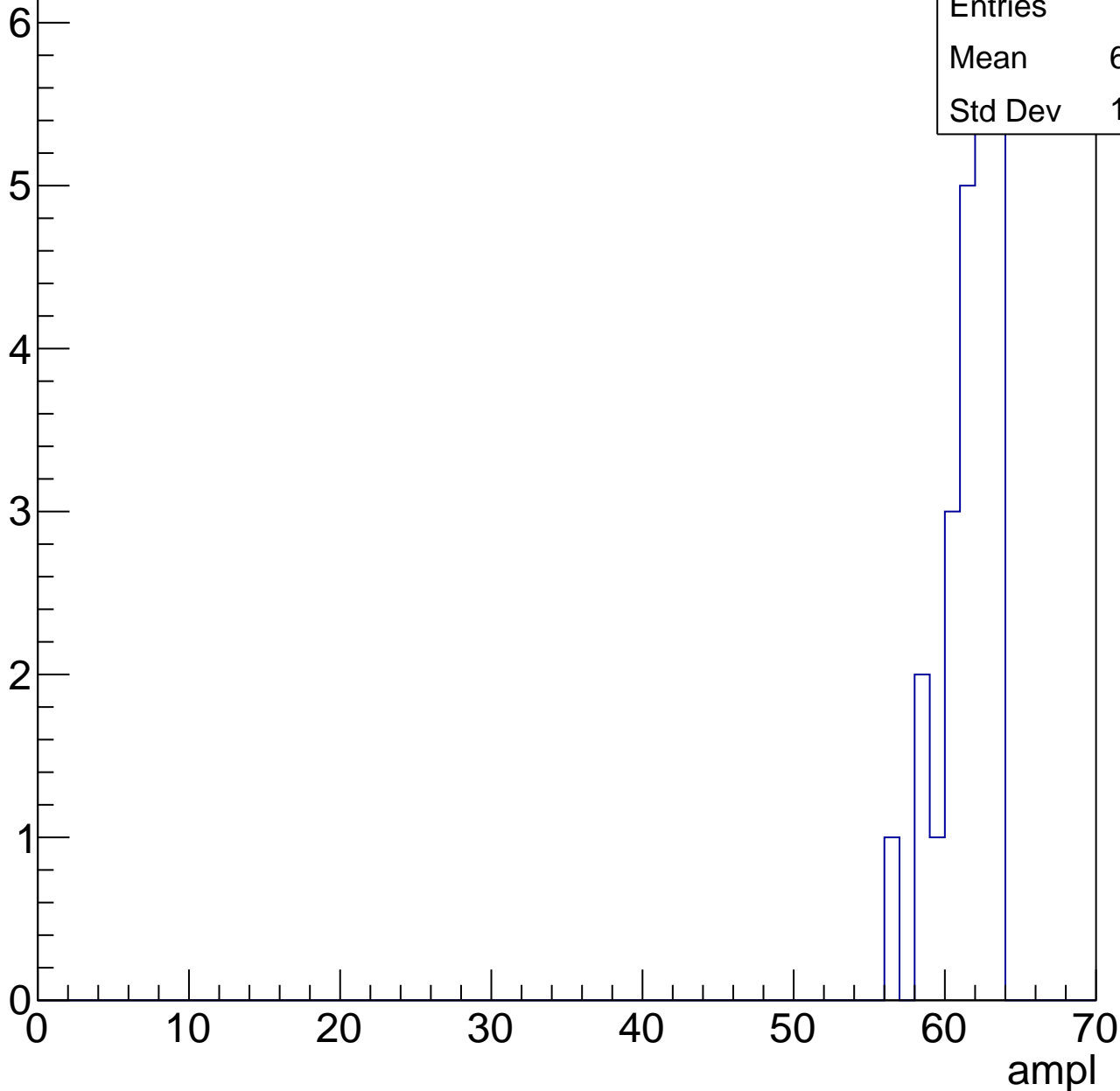


B1L103S, U9-ch120, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	24
Mean	61.08
Std Dev	1.824



B1L103S, U9-ch120, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U9-ch121, adc0

calib_packv5_041523_1651.root, FC#0, port C2

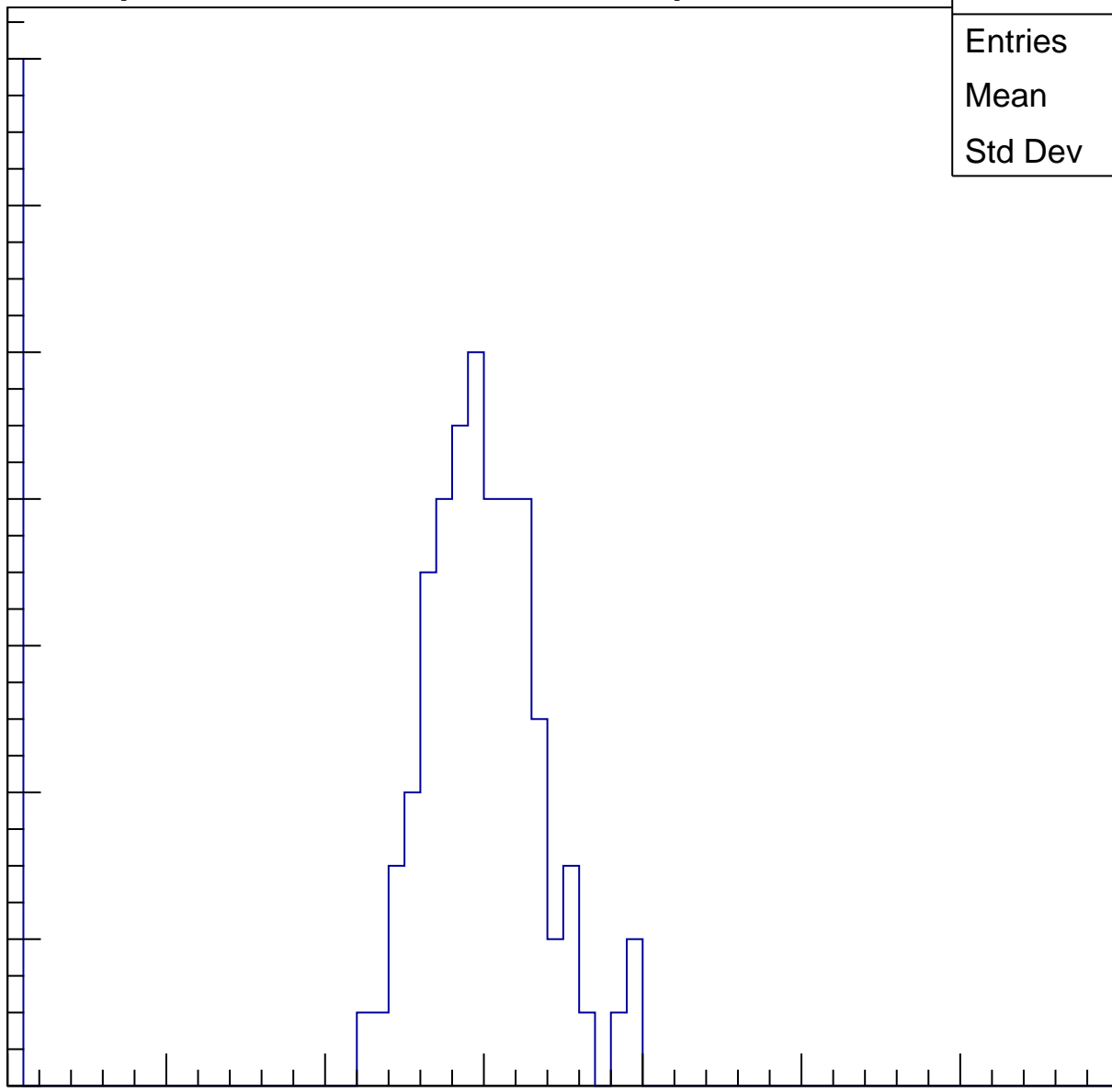
Entries	95
Mean	25.17
Std Dev	10.95

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

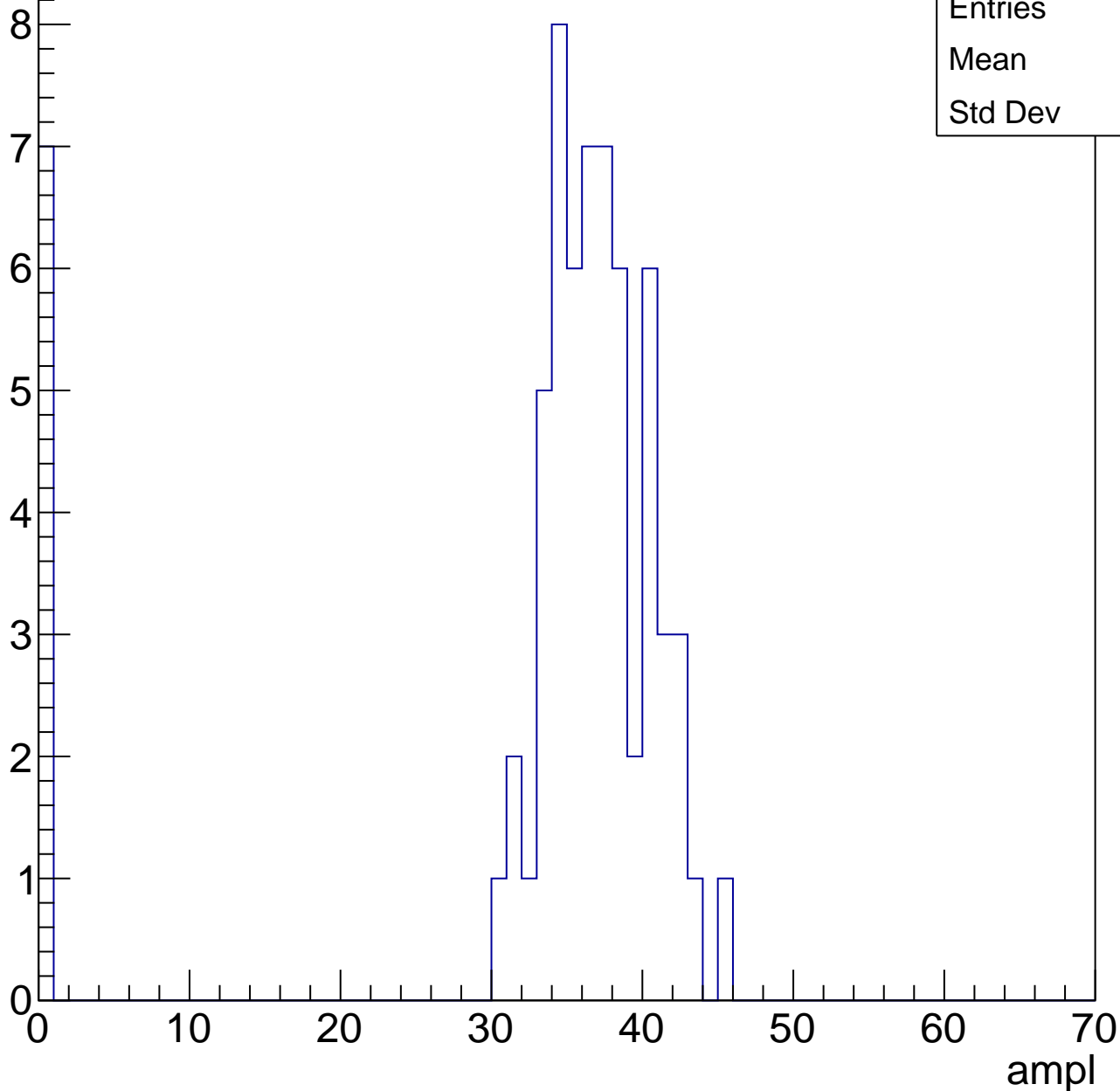


B1L103S, U9-ch121, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	32.8
Std Dev	11.7

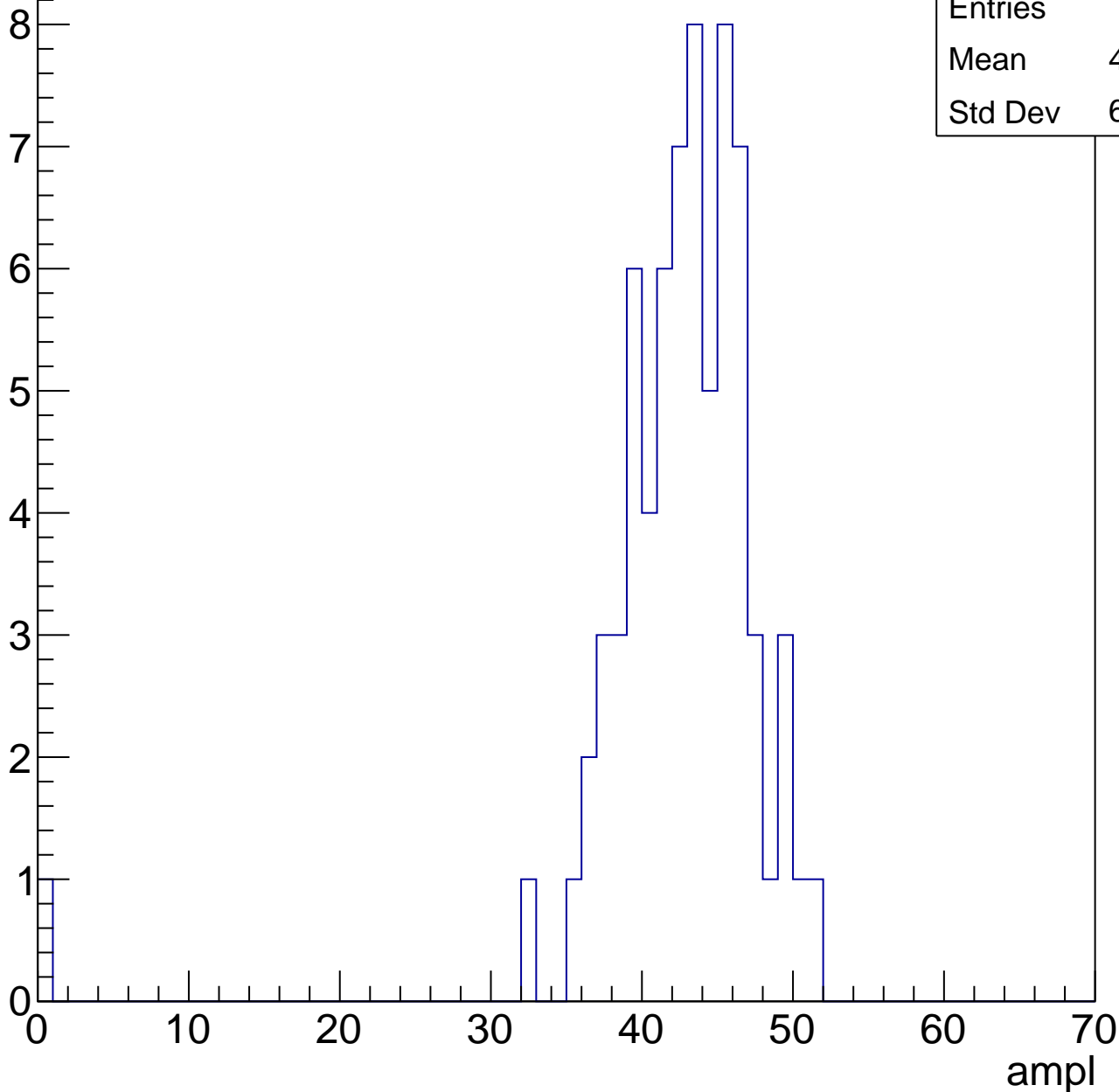


B1L103S, U9-ch121, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	41.99
Std Dev	6.279

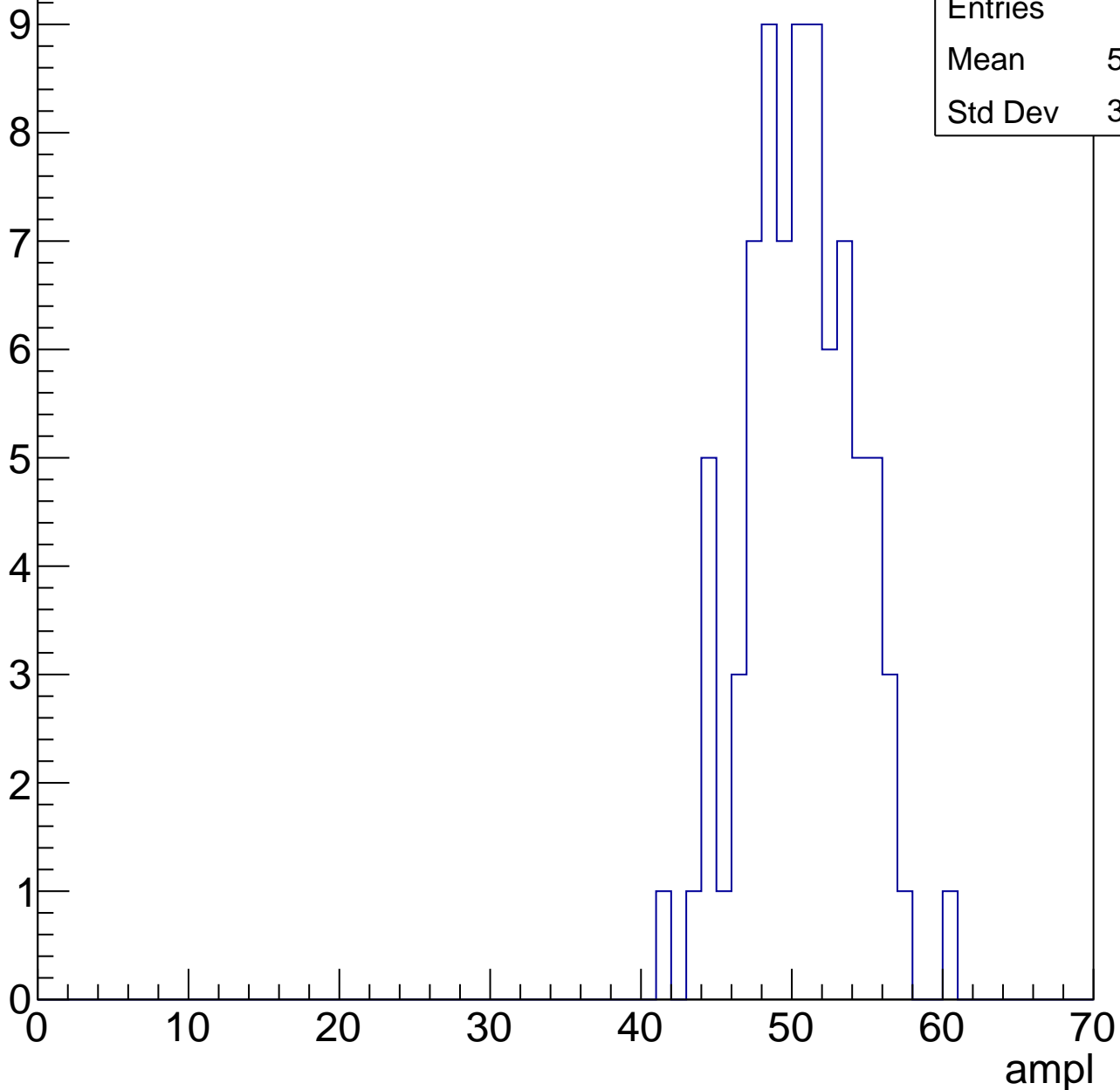


B1L103S, U9-ch121, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

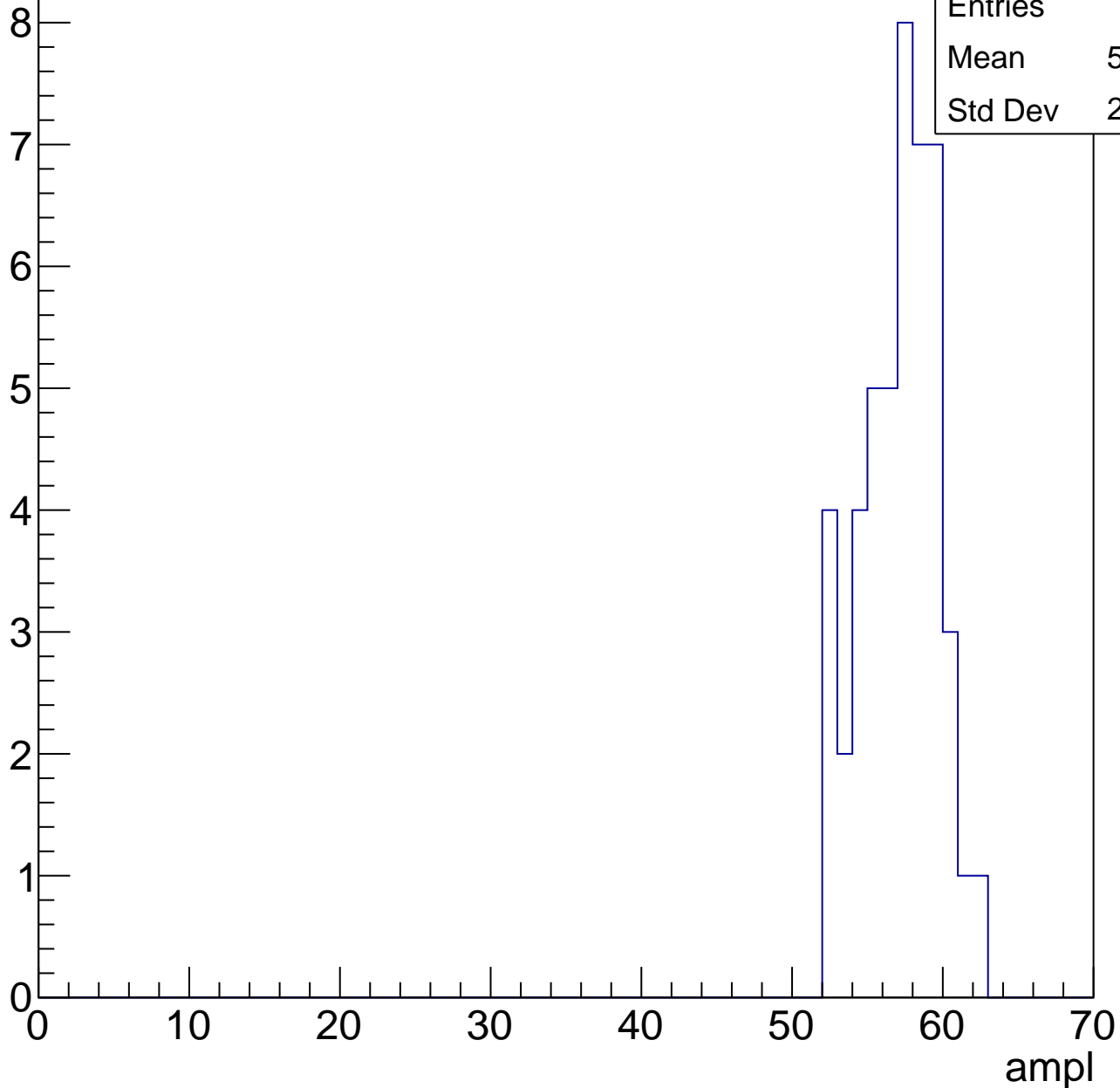
Entries	80
Mean	50.16
Std Dev	3.614



B1L103S, U9-ch121, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



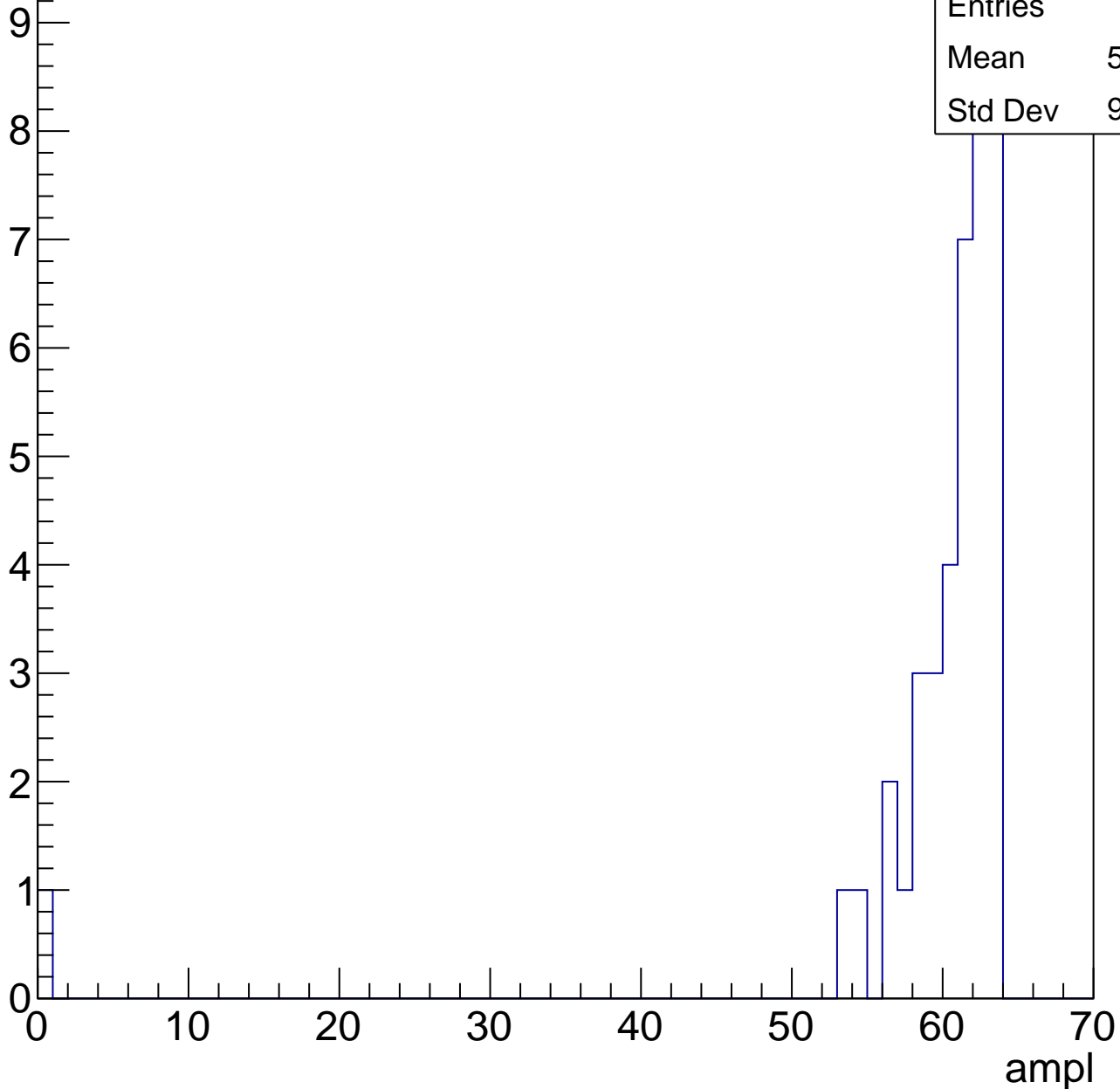
Entries	47
Mean	56.66
Std Dev	2.486

B1L103S, U9-ch121, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	58.92
Std Dev	9.766



B1L103S, U9-ch121, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	6
Mean	61.17
Std Dev	1.067

ampl

0 10 20 30 40 50 60 70

B1L103S, U9-ch121, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

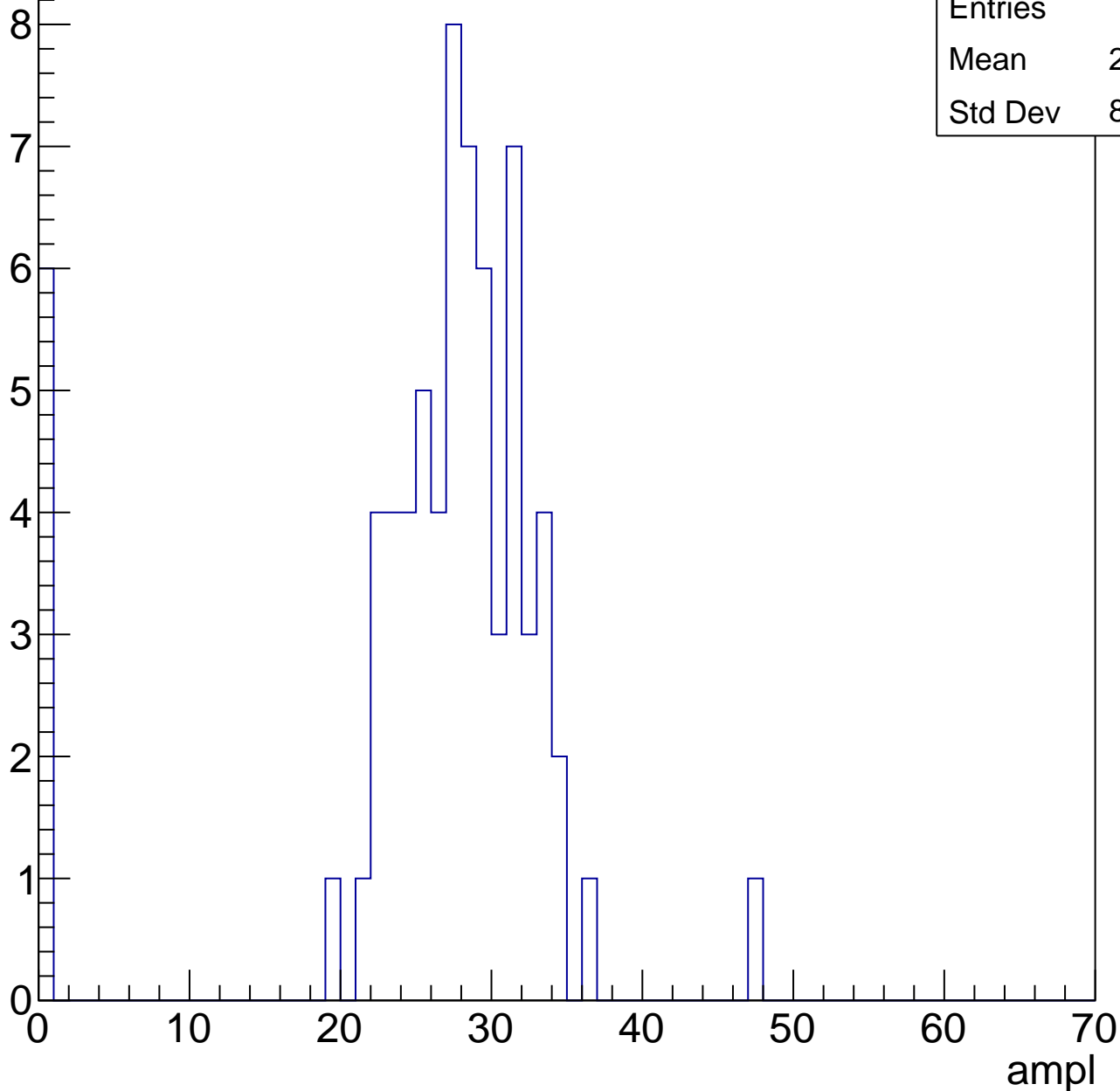
Entries	19
Mean	0
Std Dev	0

B1L103S, U9-ch122, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	25.59
Std Dev	8.822

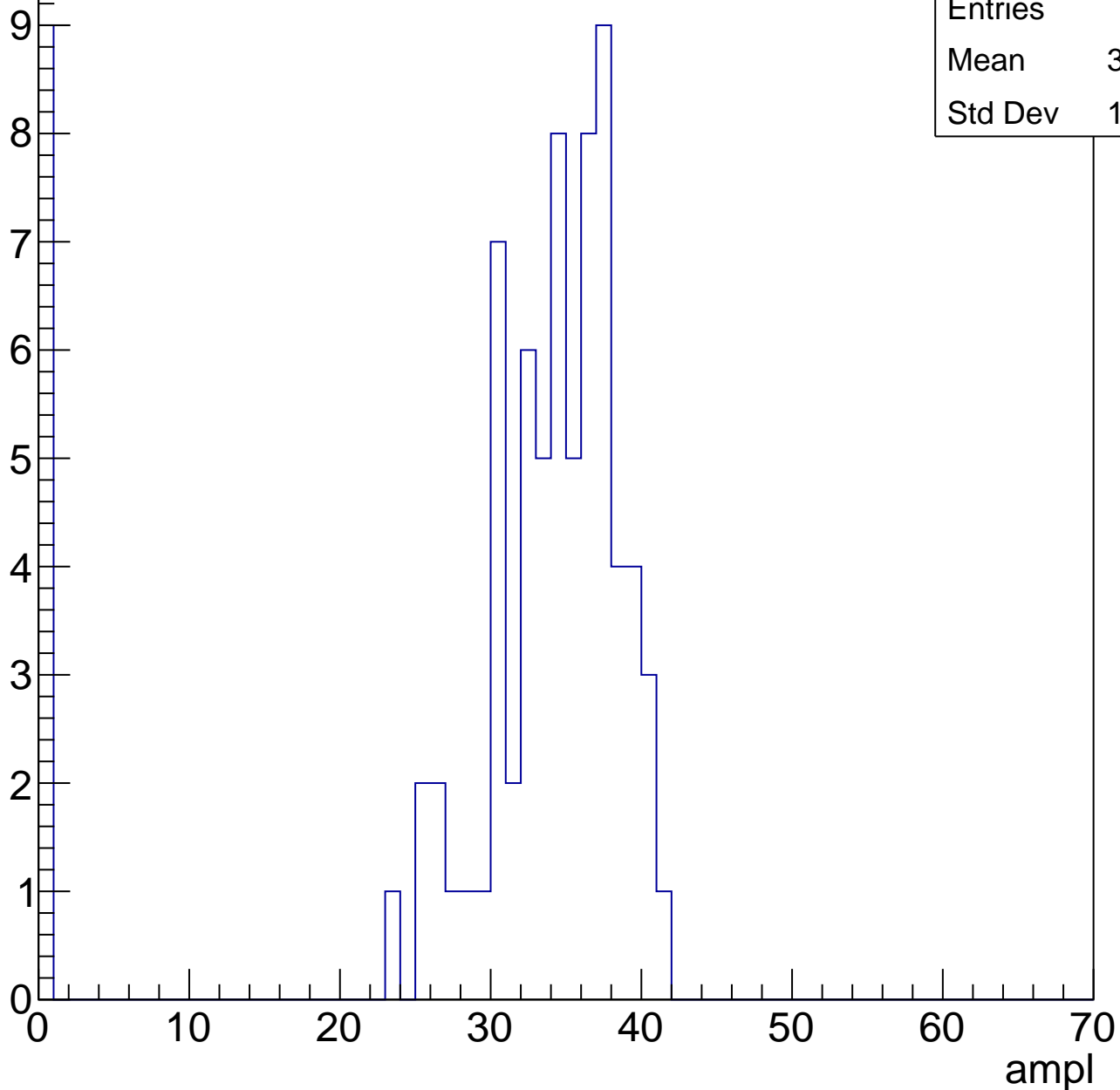


B1L103S, U9-ch122, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	79
Mean	30.06
Std Dev	11.42

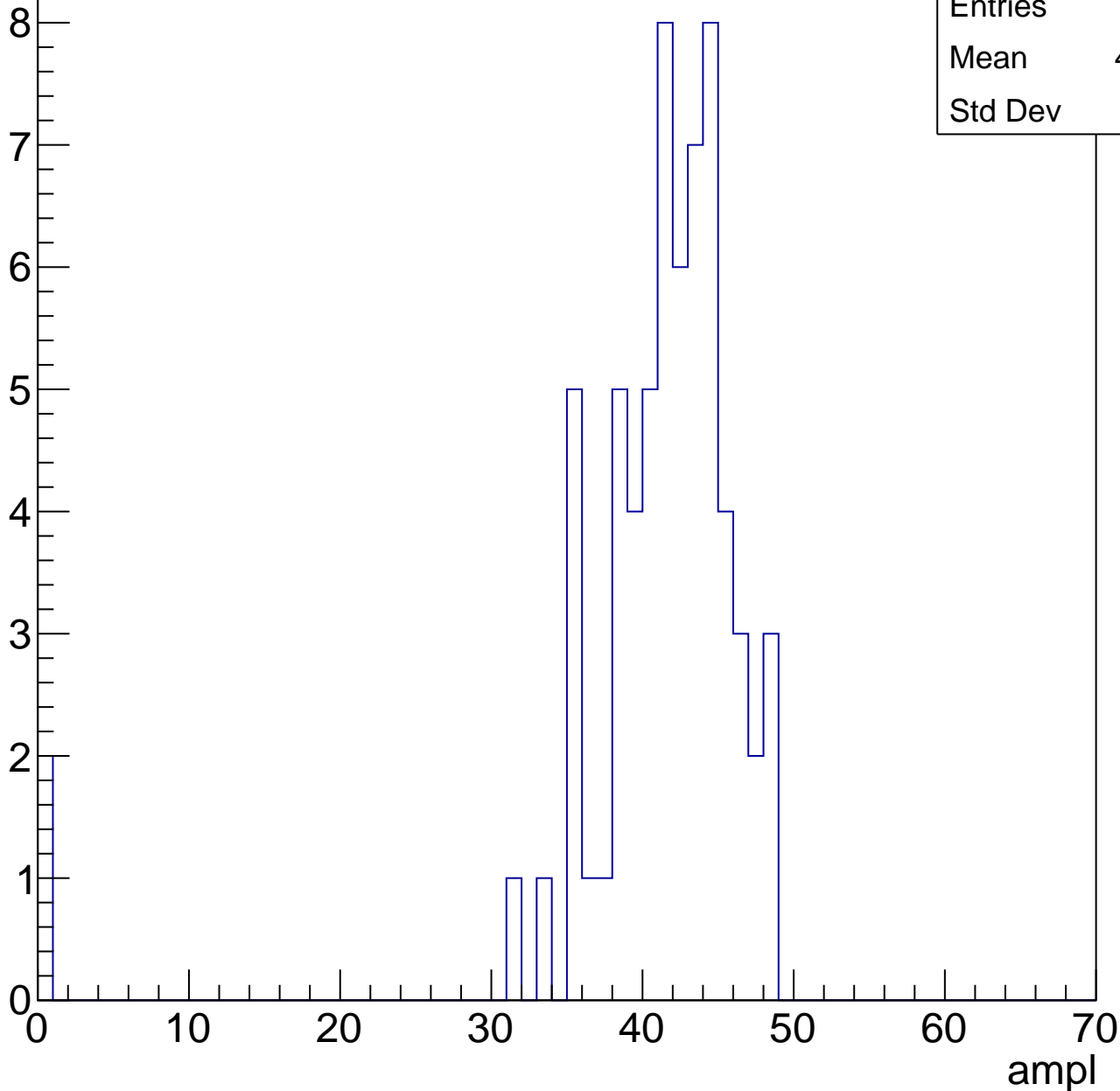


B1L103S, U9-ch122, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	40.11
Std Dev	8

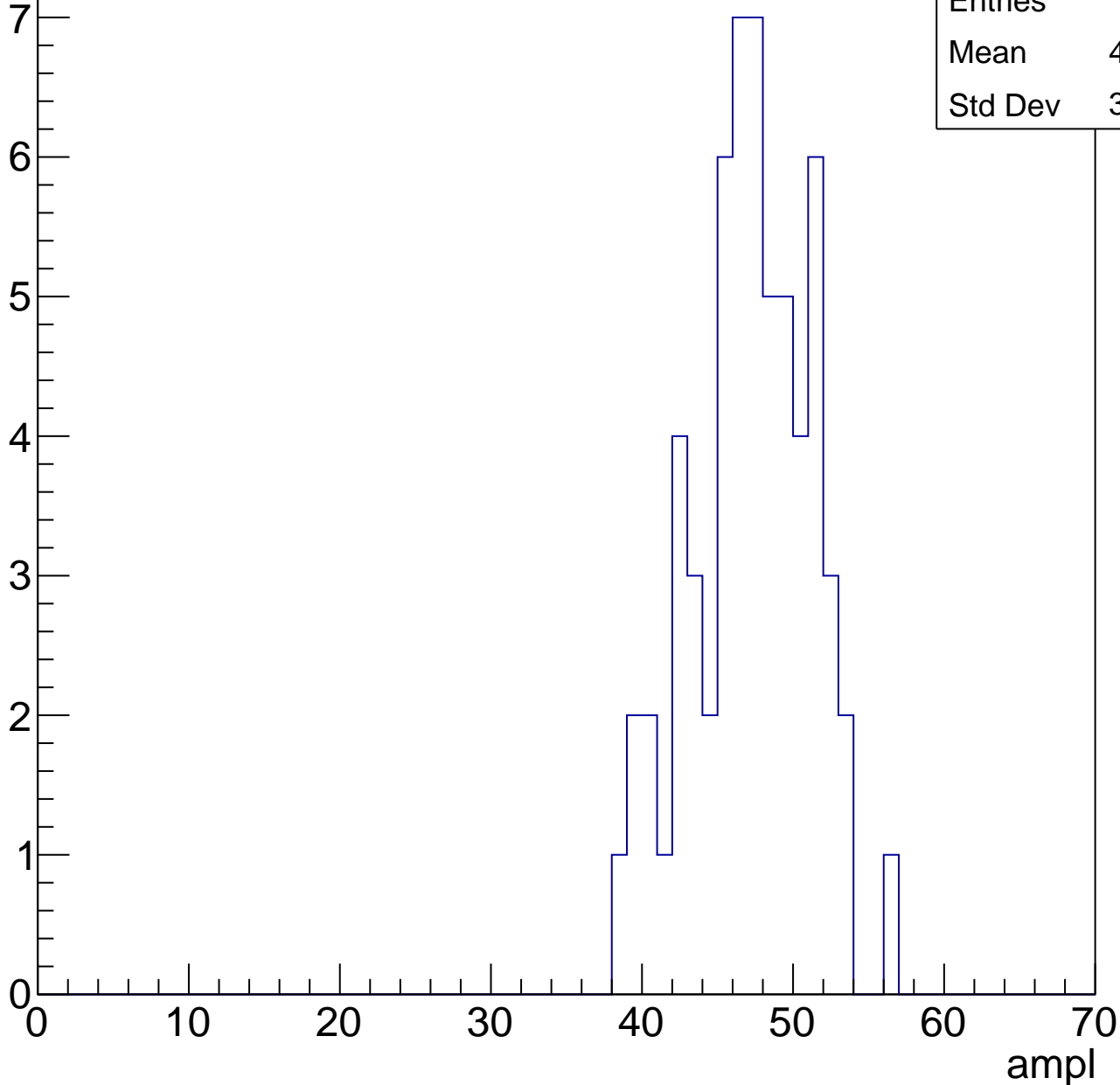


B1L103S, U9-ch122, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	46.75
Std Dev	3.886

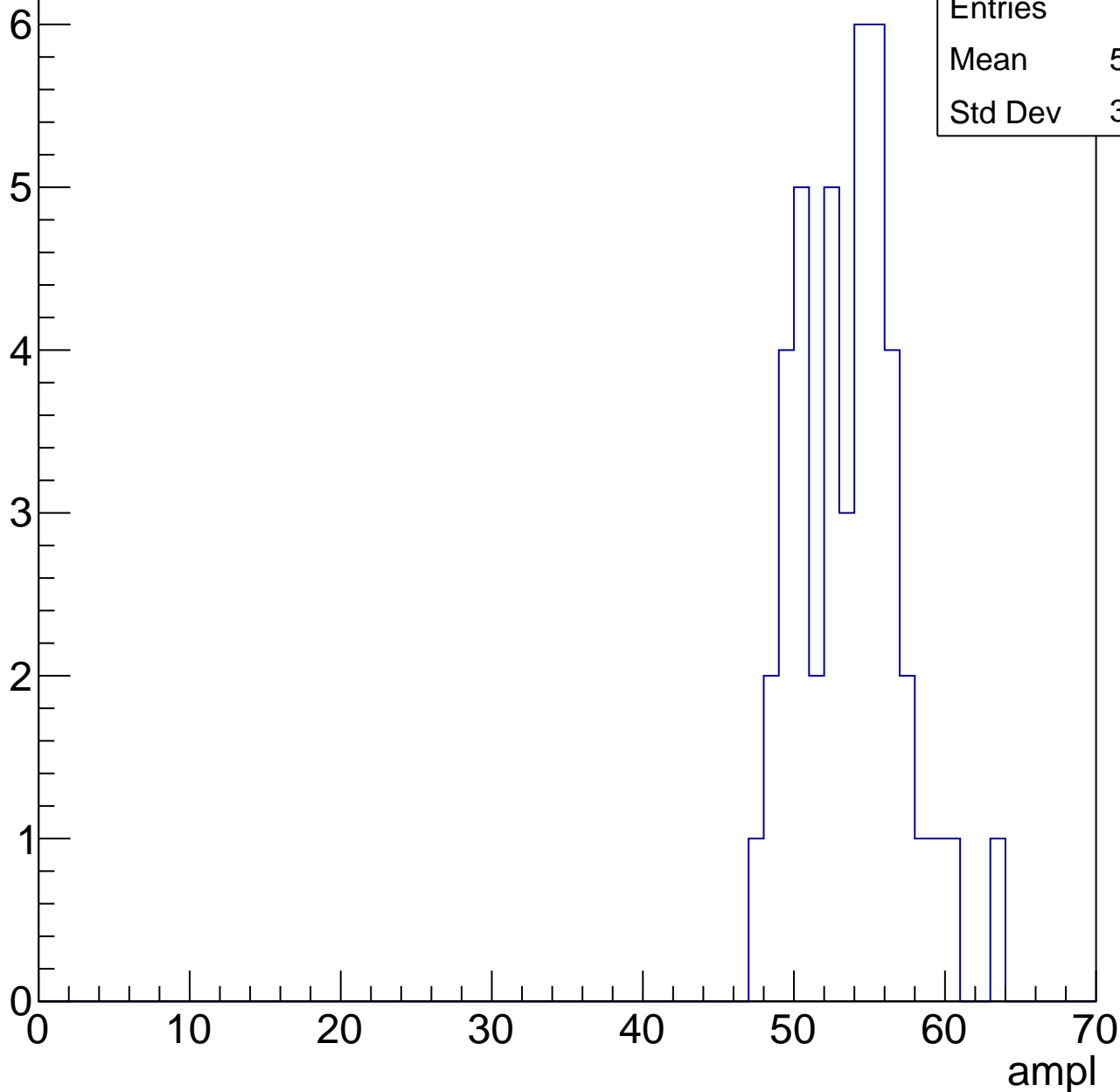


B1L103S, U9-ch122, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	44
Mean	53.23
Std Dev	3.417

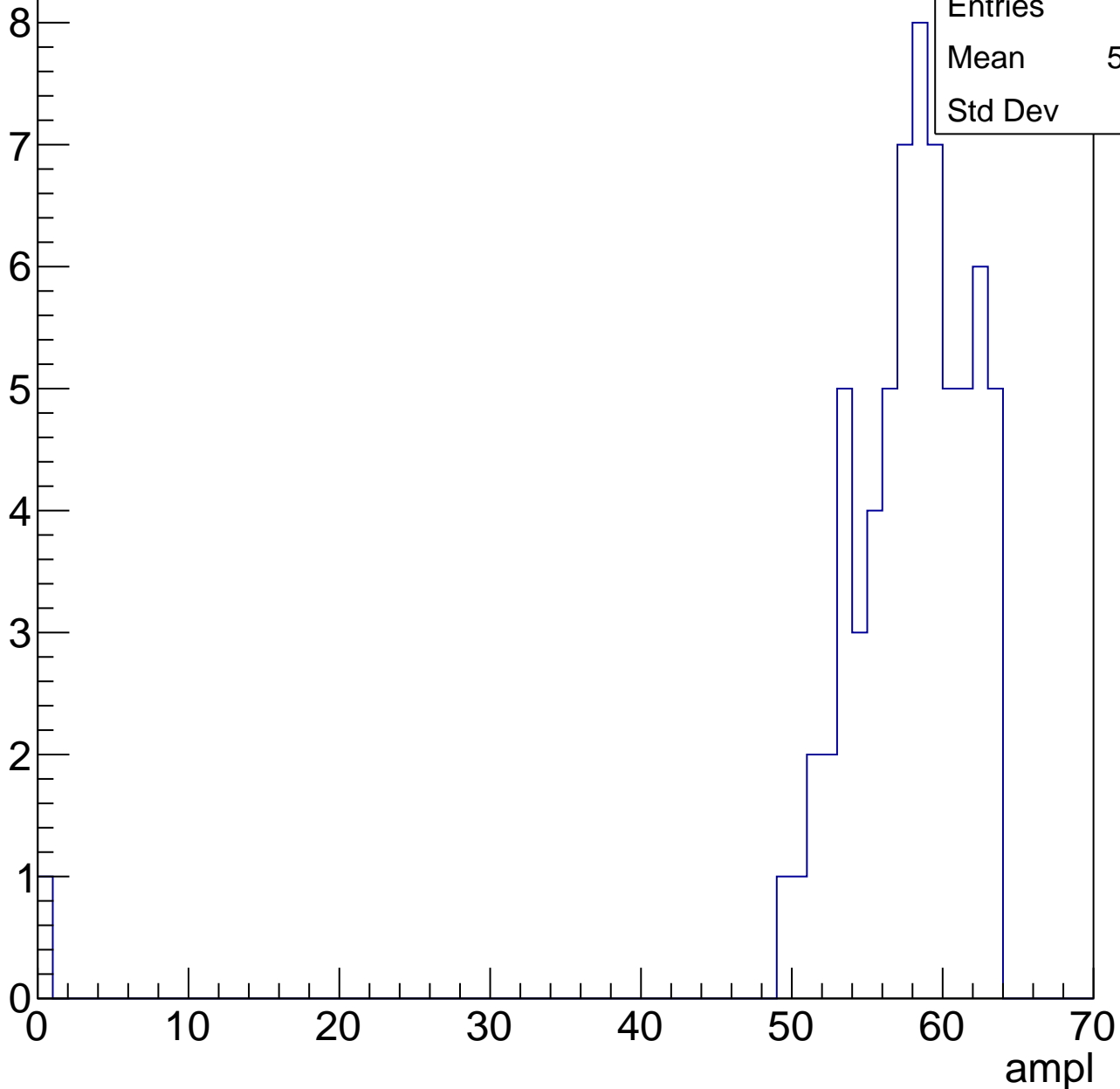


B1L103S, U9-ch122, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	56.72
Std Dev	7.82

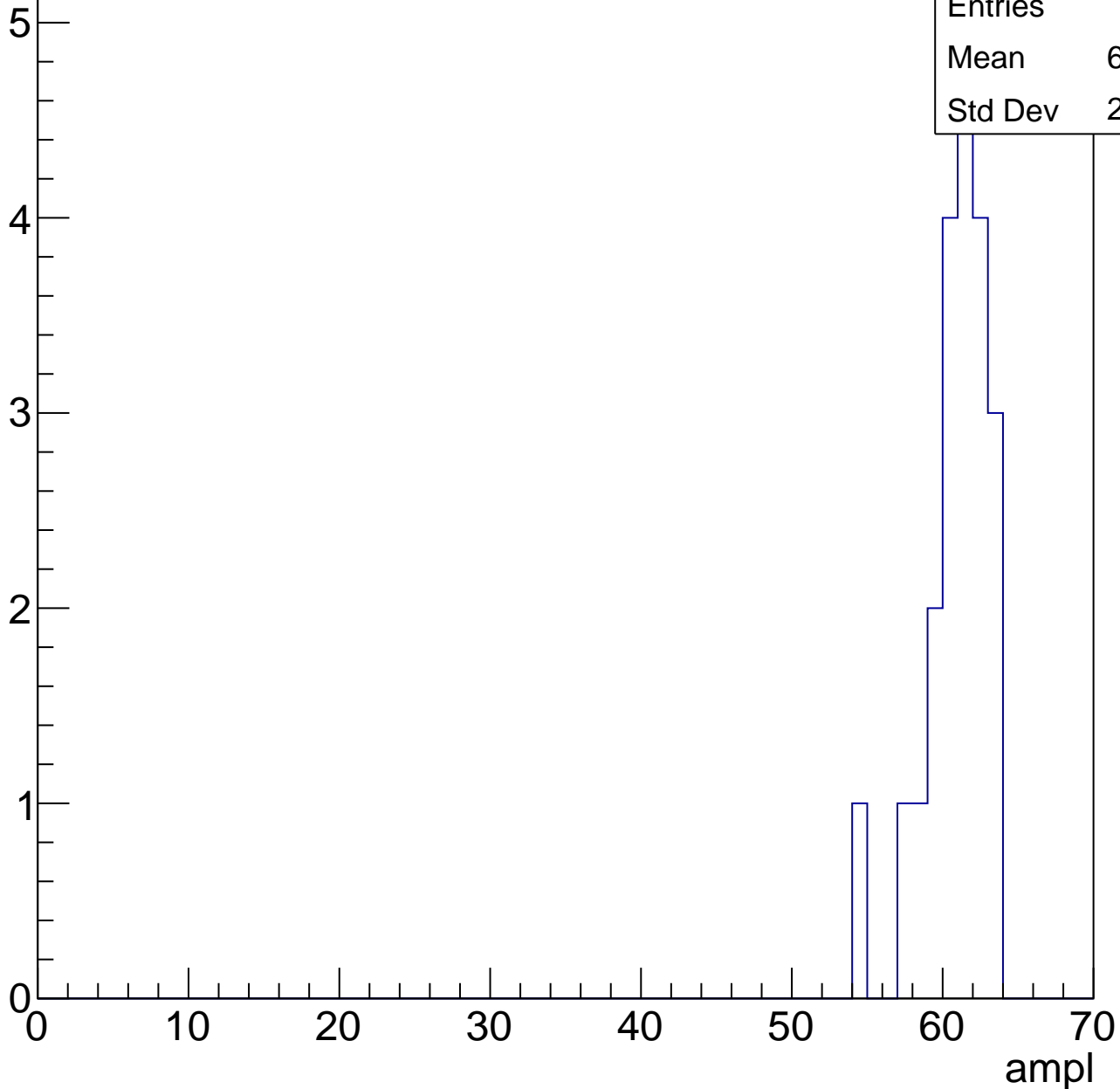


B1L103S, U9-ch122, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	21
Mean	60.43
Std Dev	2.129



B1L103S, U9-ch122, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry



B1L103S, U9-ch123, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	72
Mean	25.07
Std Dev	11.2

Entry

10

8

6

4

2

0

0

10

20

30

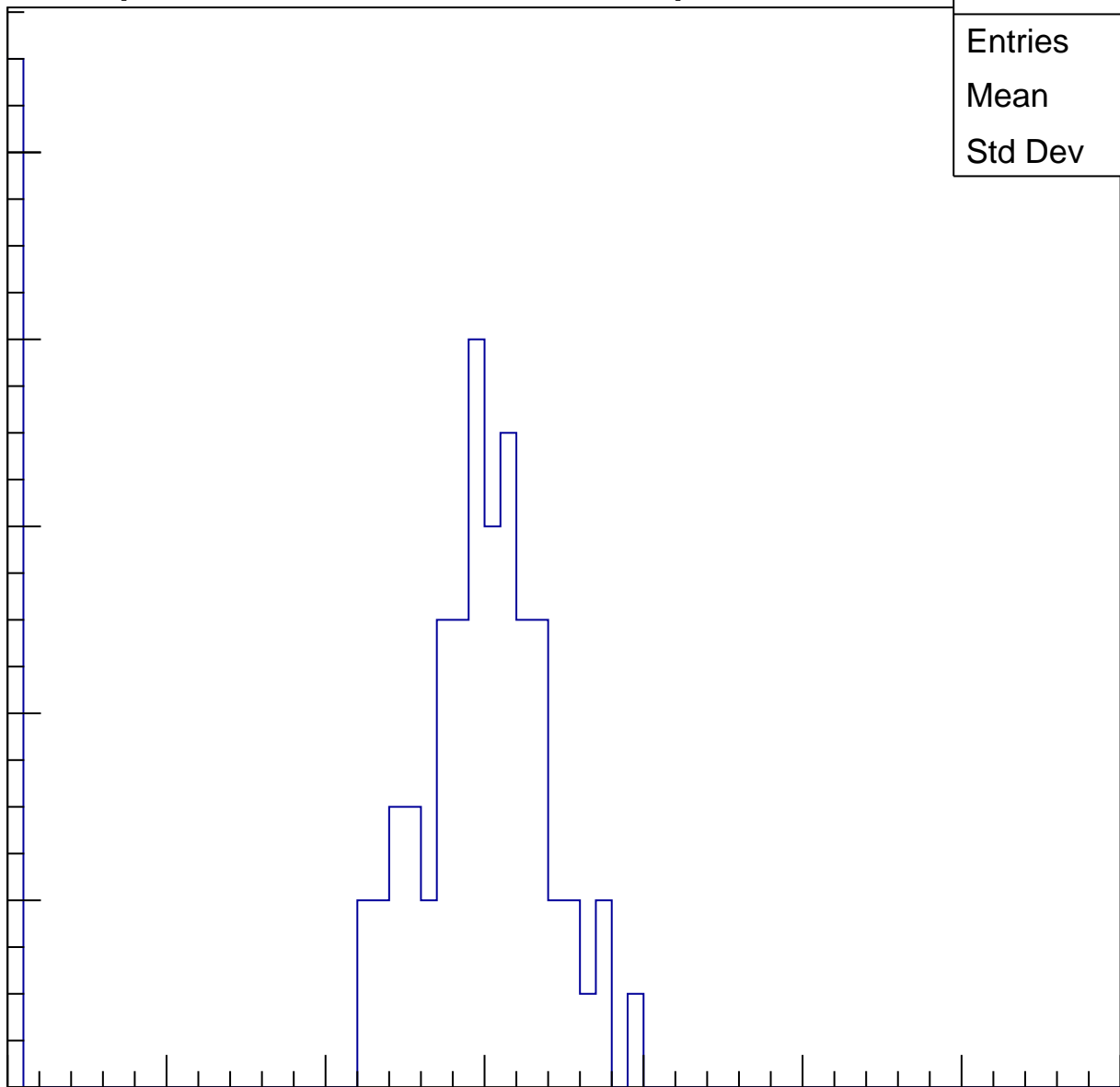
40

50

60

70

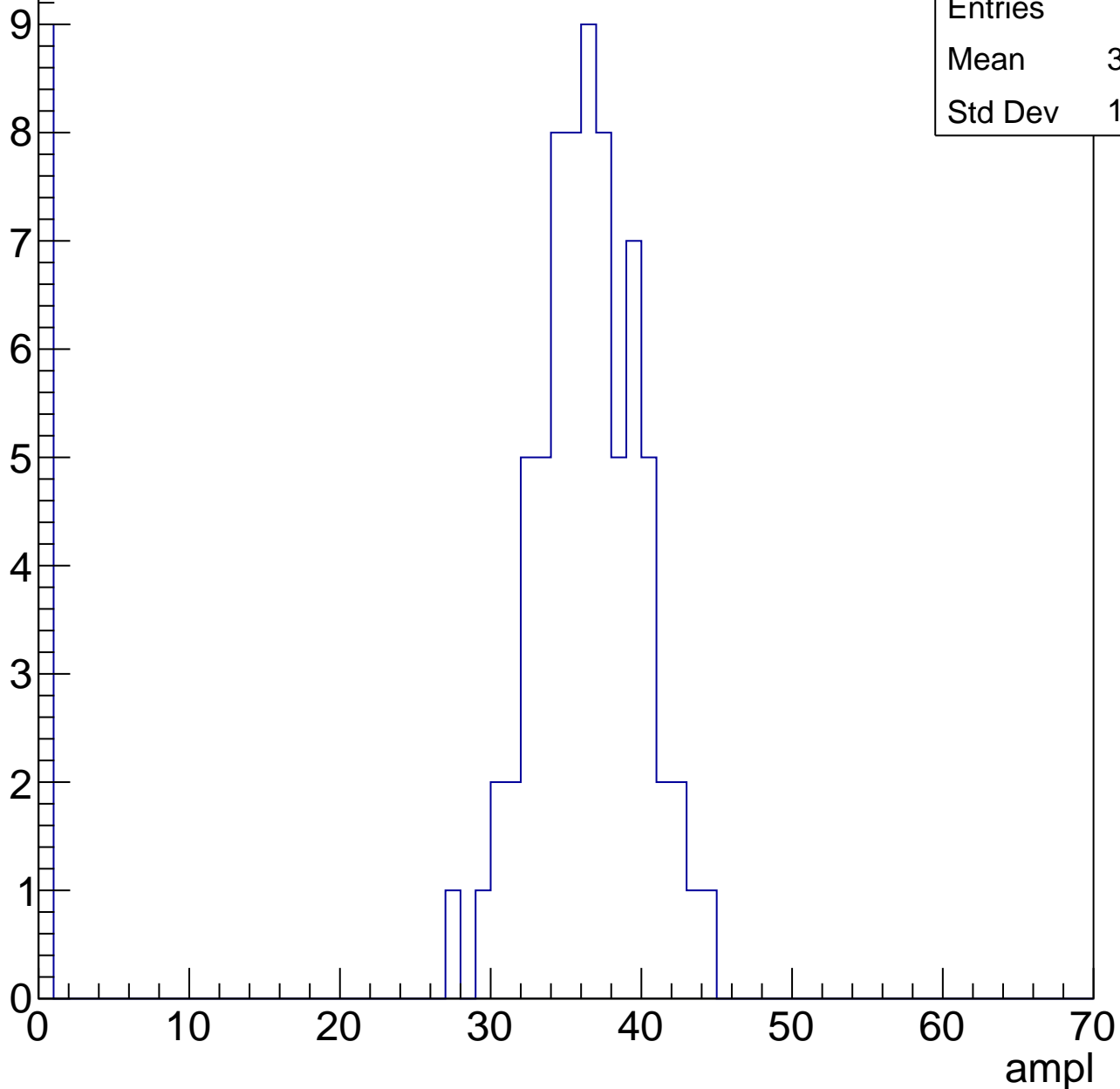
ampl



B1L103S, U9-ch123, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

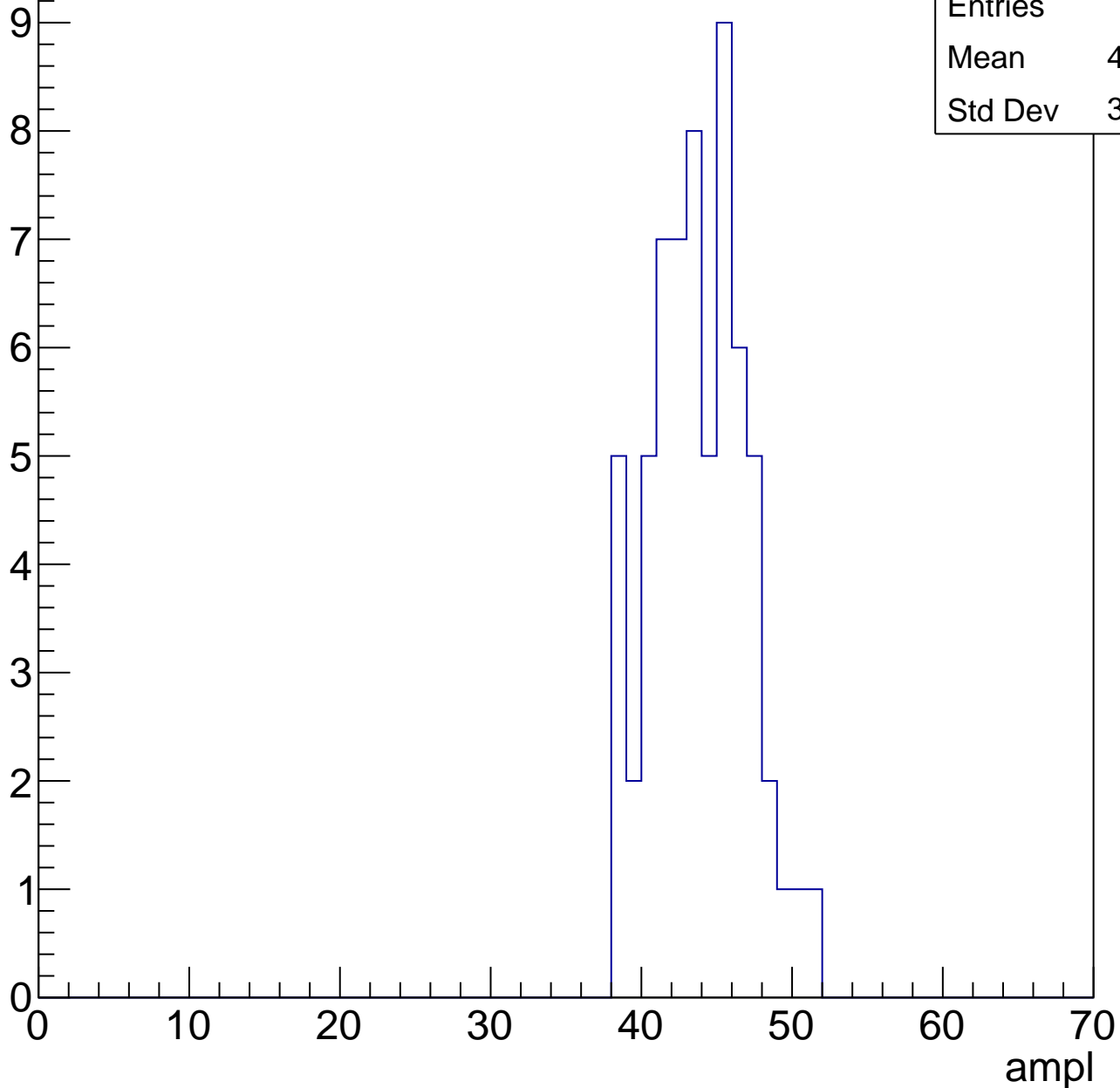


Entries	81
Mean	31.99
Std Dev	11.75

B1L103S, U9-ch123, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry



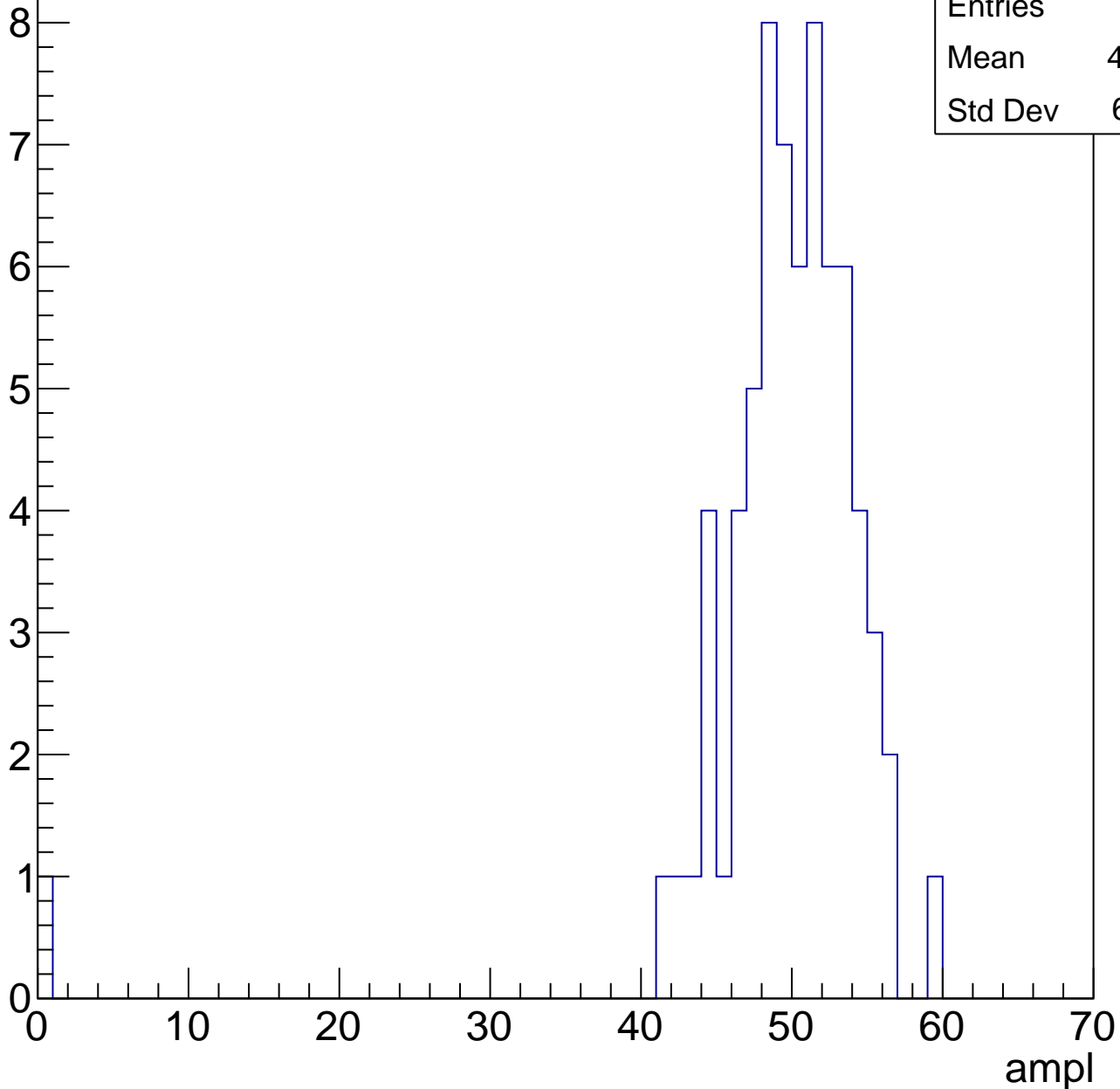
Entries	64
Mean	43.36
Std Dev	3.069

B1L103S, U9-ch123, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	49.03
Std Dev	6.941

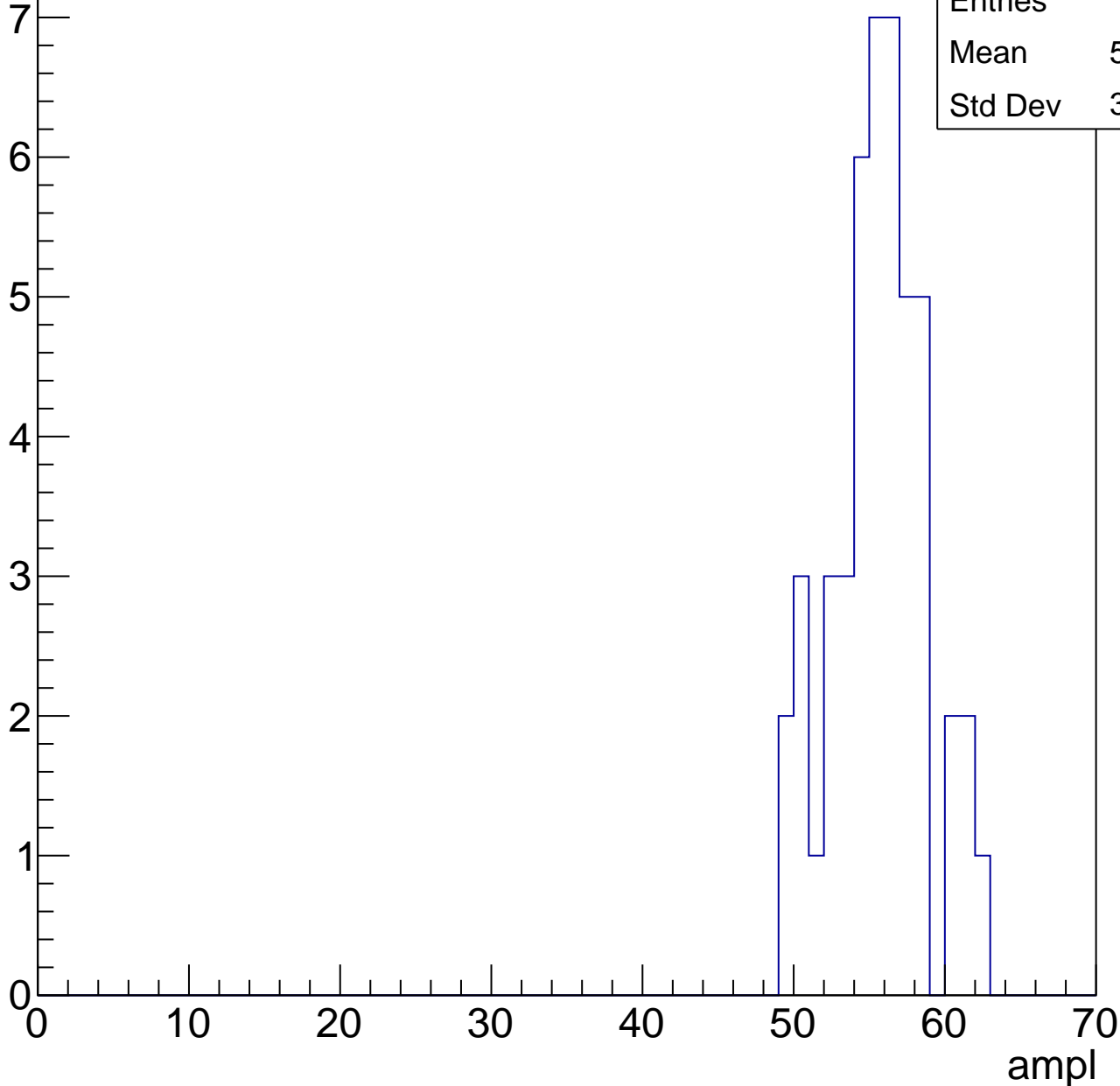


B1L103S, U9-ch123, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	47
Mean	55.19
Std Dev	3.092

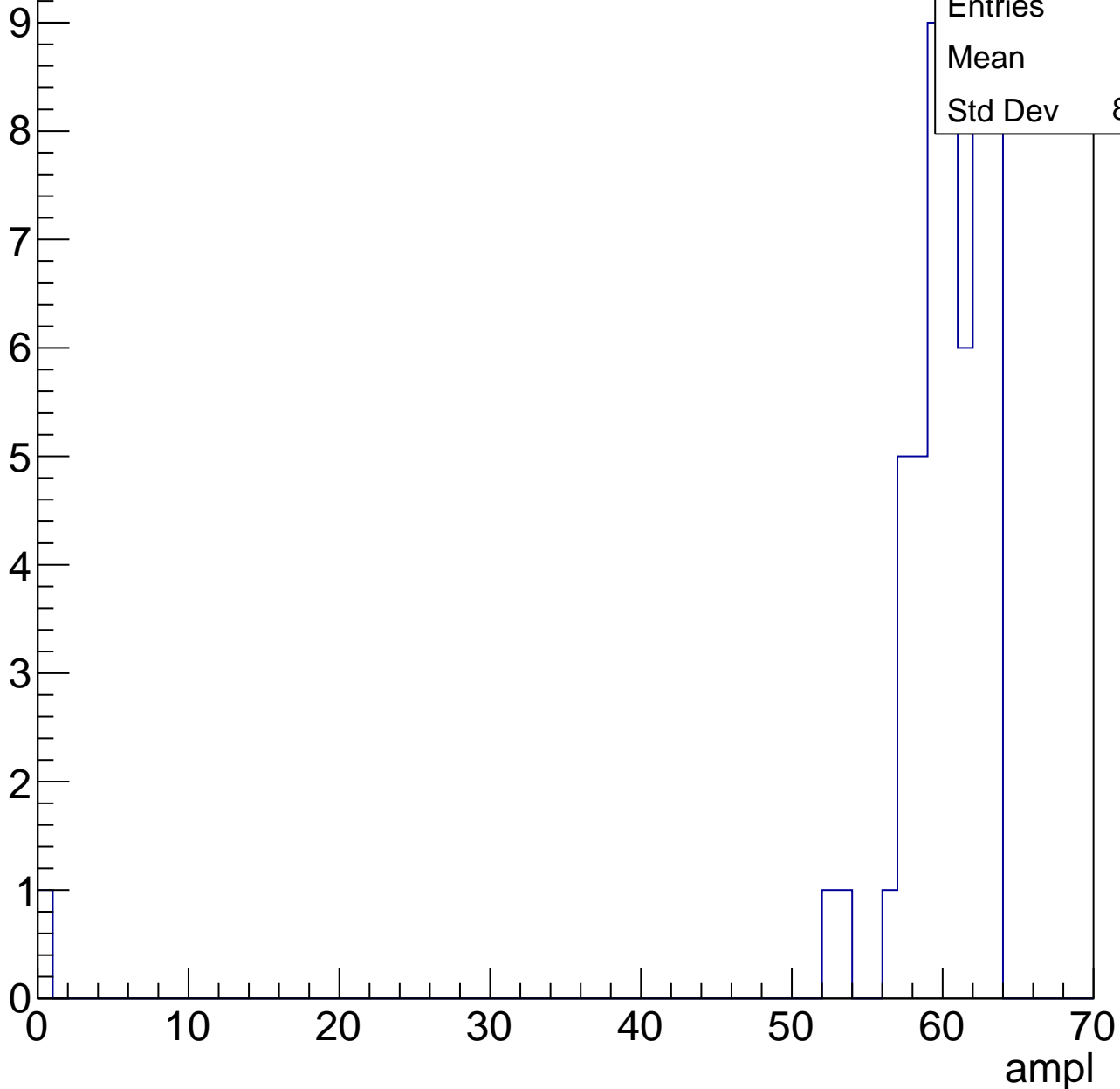


B1L103S, U9-ch123, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	58.8
Std Dev	8.431



B1L103S, U9-ch123, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

0 10 20 30 40 50 60 70

ampl

Entries	4
Mean	62
Std Dev	1

B1L103S, U9-ch123, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.053
Std Dev	4.466

Entry



B1L103S, U9-ch124, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	22.55
Std Dev	10.45

Entry

12

10

8

6

4

2

0

0

10

20

30

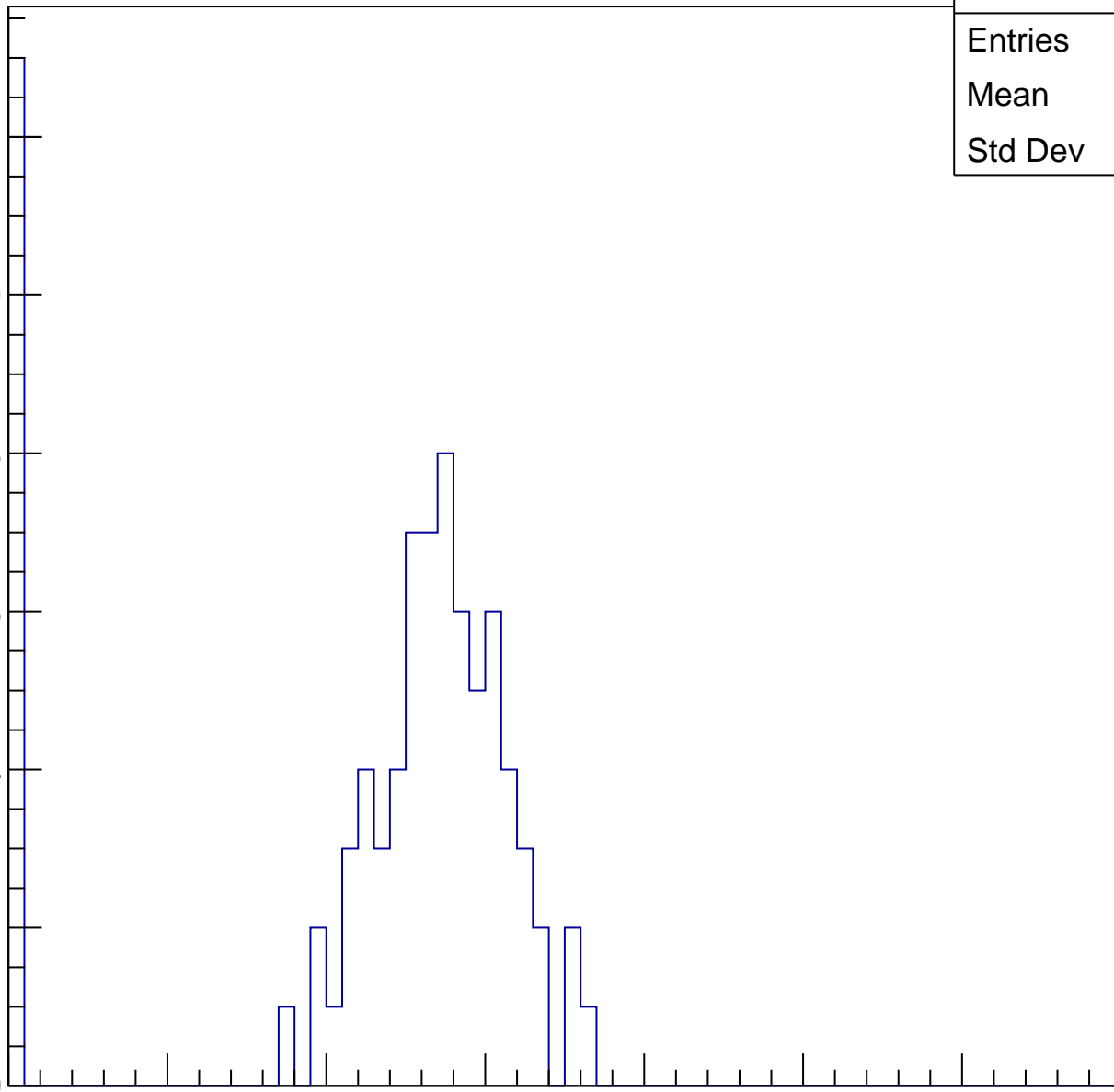
40

50

60

70

ampl

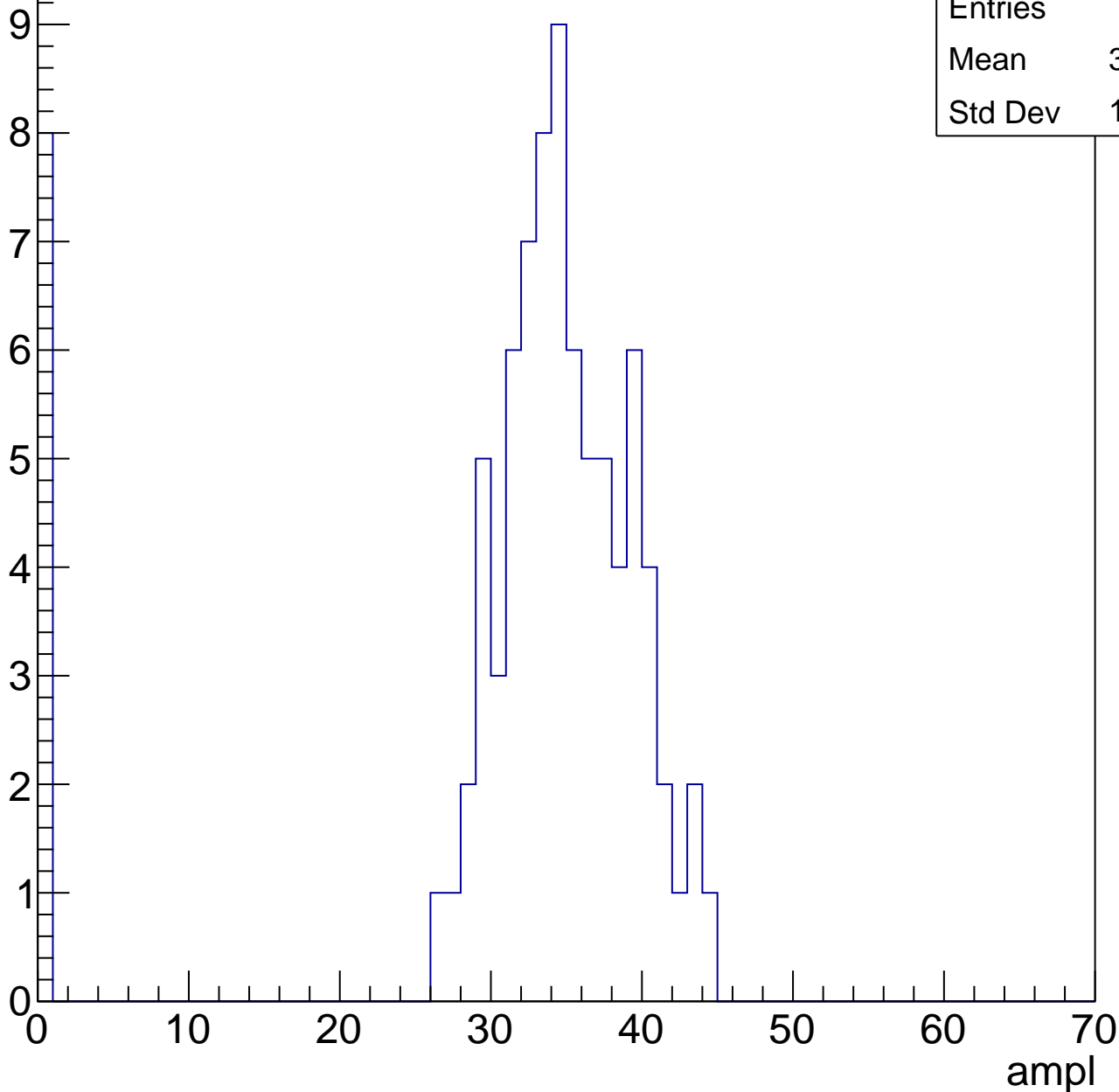


B1L103S, U9-ch124, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	86
Mean	31.38
Std Dev	10.76

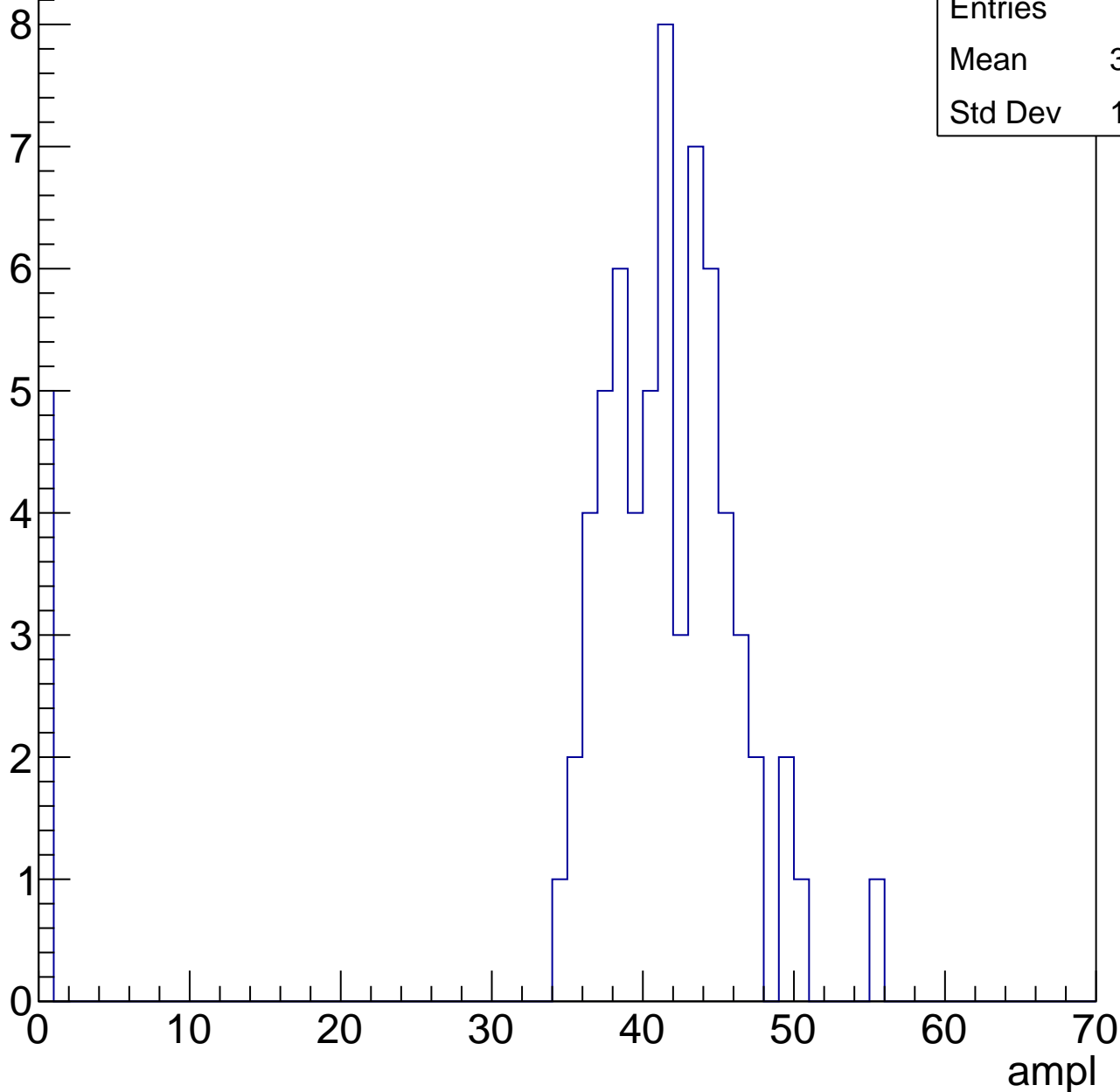


B1L103S, U9-ch124, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	38.42
Std Dev	11.44

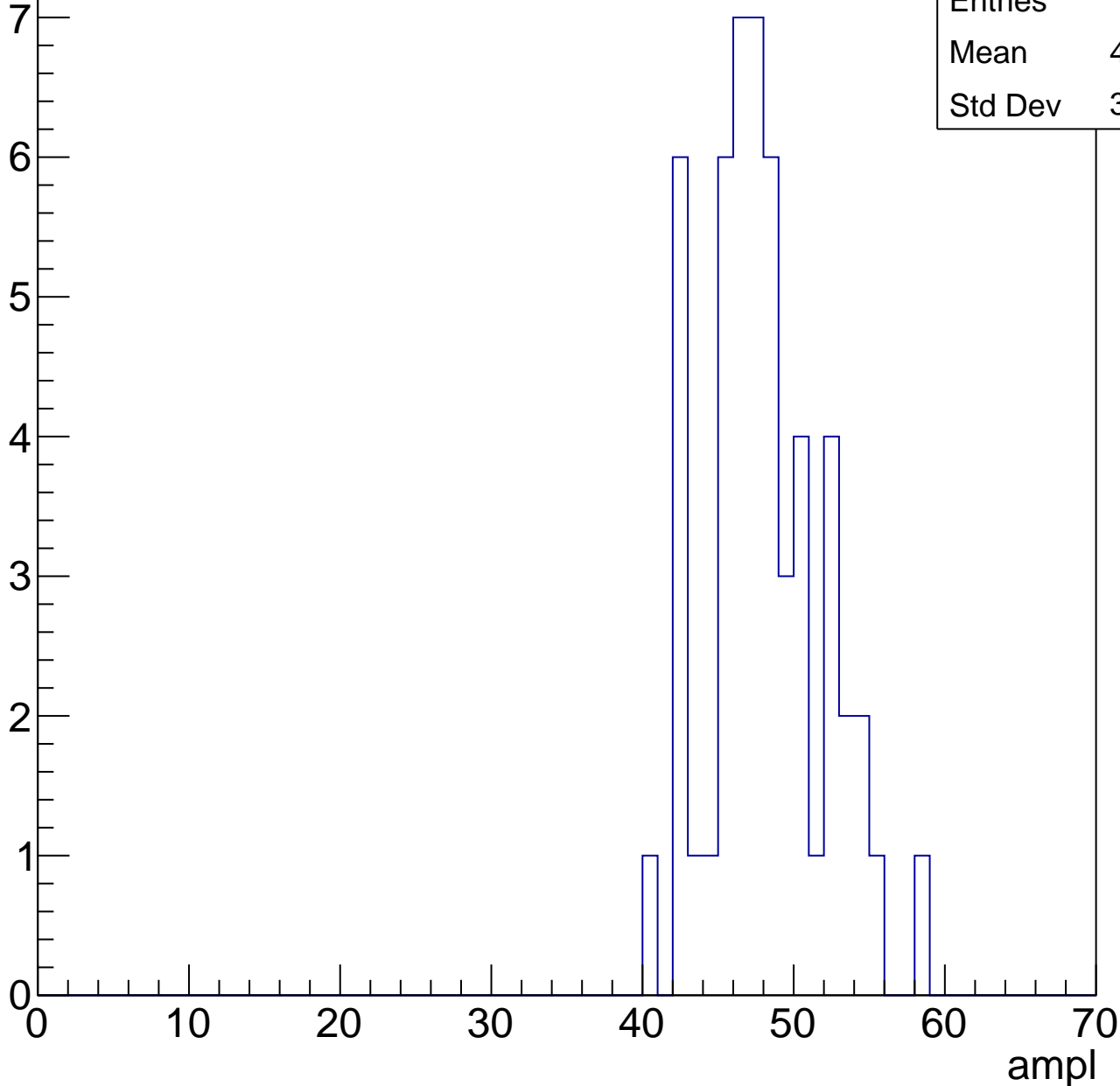


B1L103S, U9-ch124, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	47.57
Std Dev	3.794

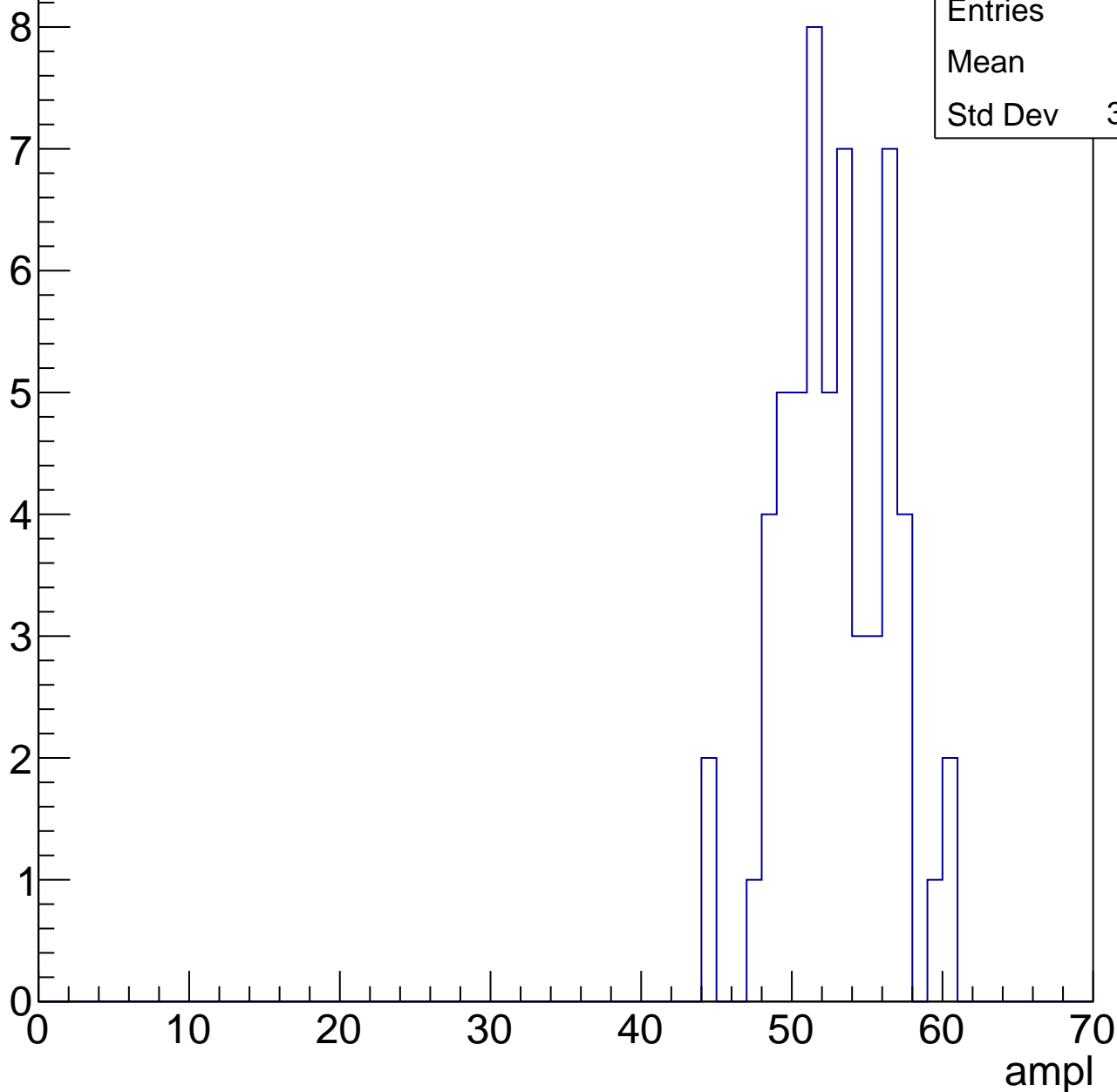


B1L103S, U9-ch124, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	52.4
Std Dev	3.544



B1L103S, U9-ch124, adc5

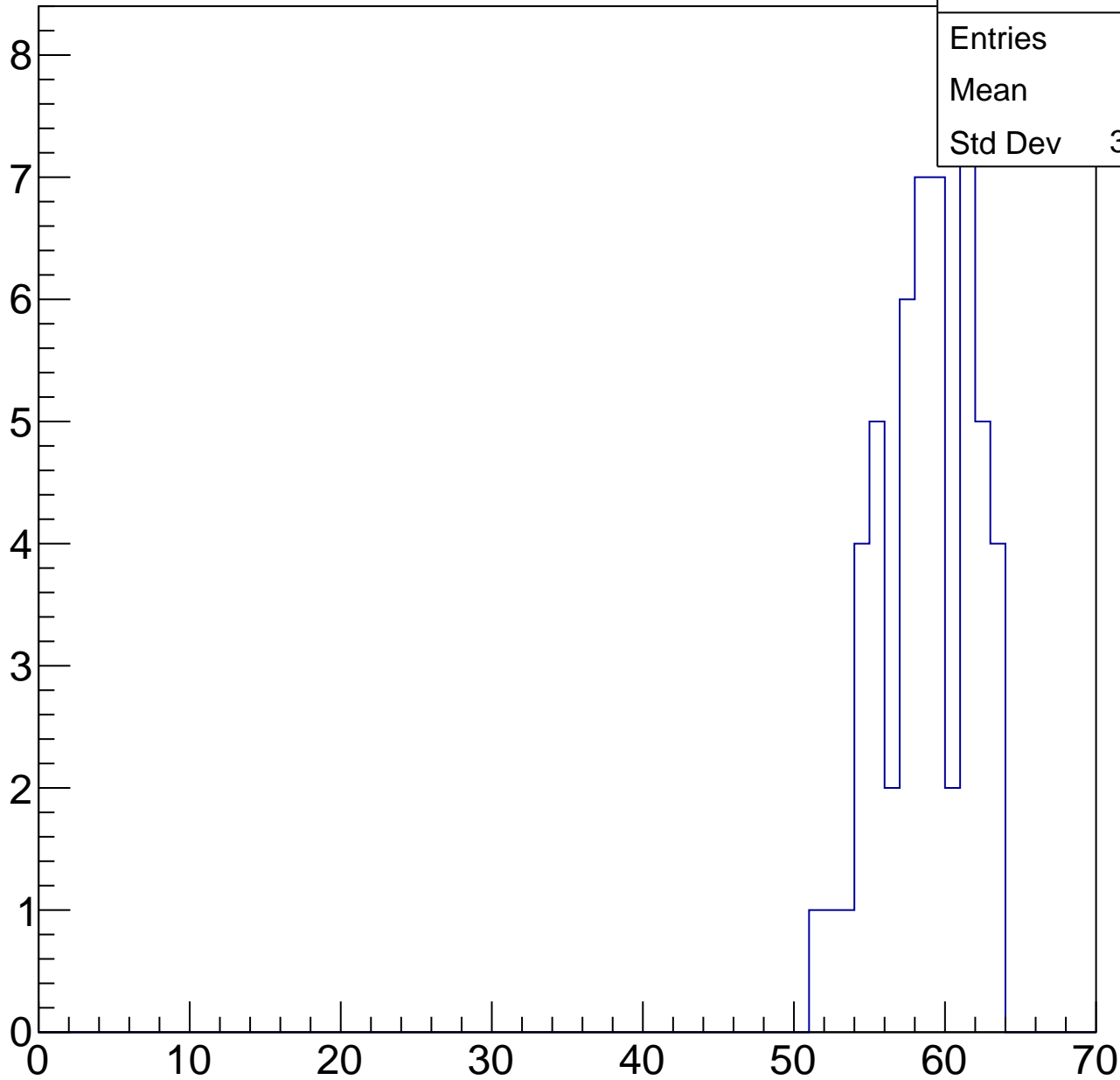
calib_packv5_041523_1651.root, FC#0, port C2

Entry

8
7
6
5
4
3
2
1
0

Entries	53
Mean	58.3
Std Dev	3.057

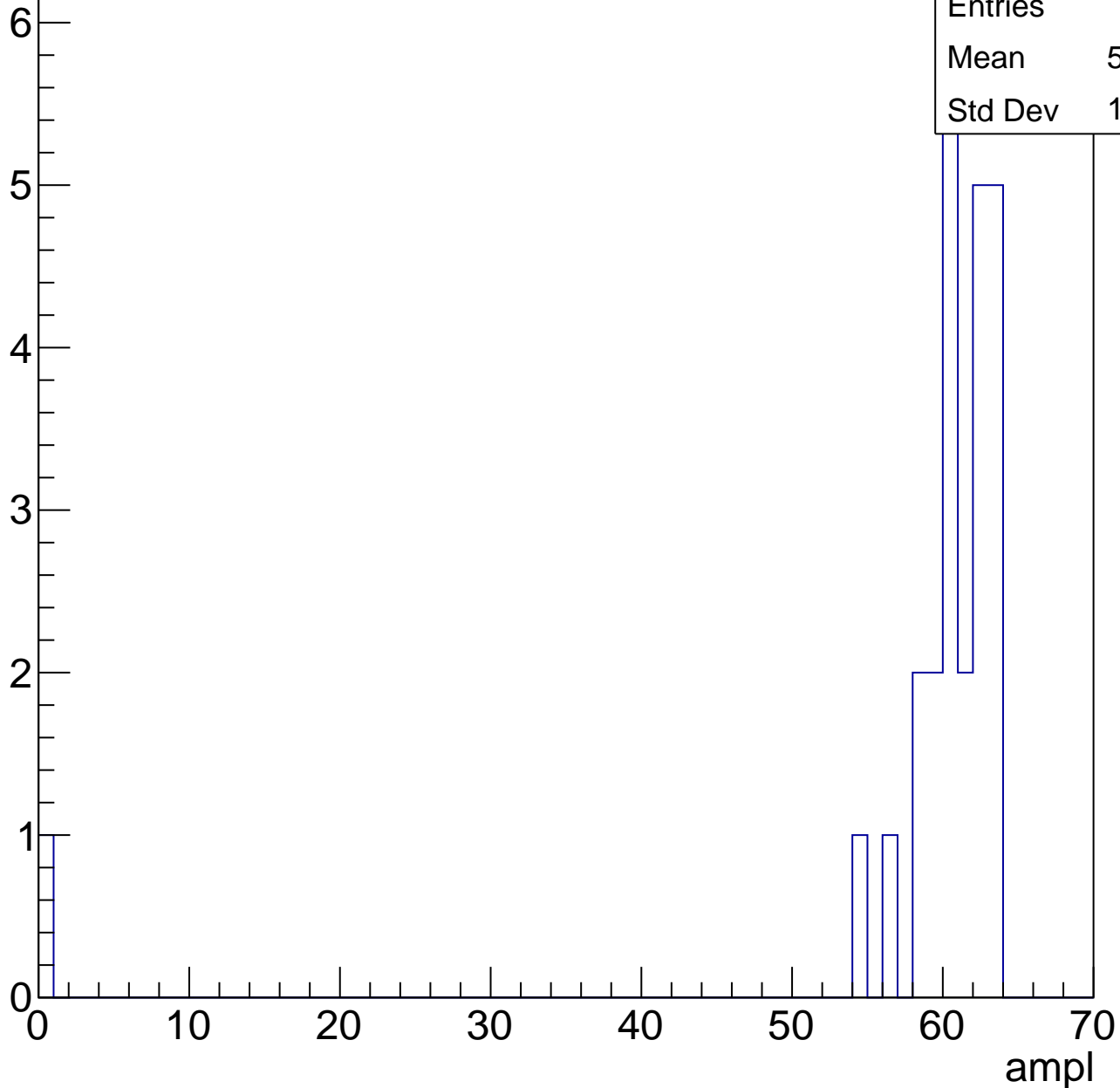
ampl



B1L103S, U9-ch124, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch124, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry



B1L103S, U9-ch125, adc0

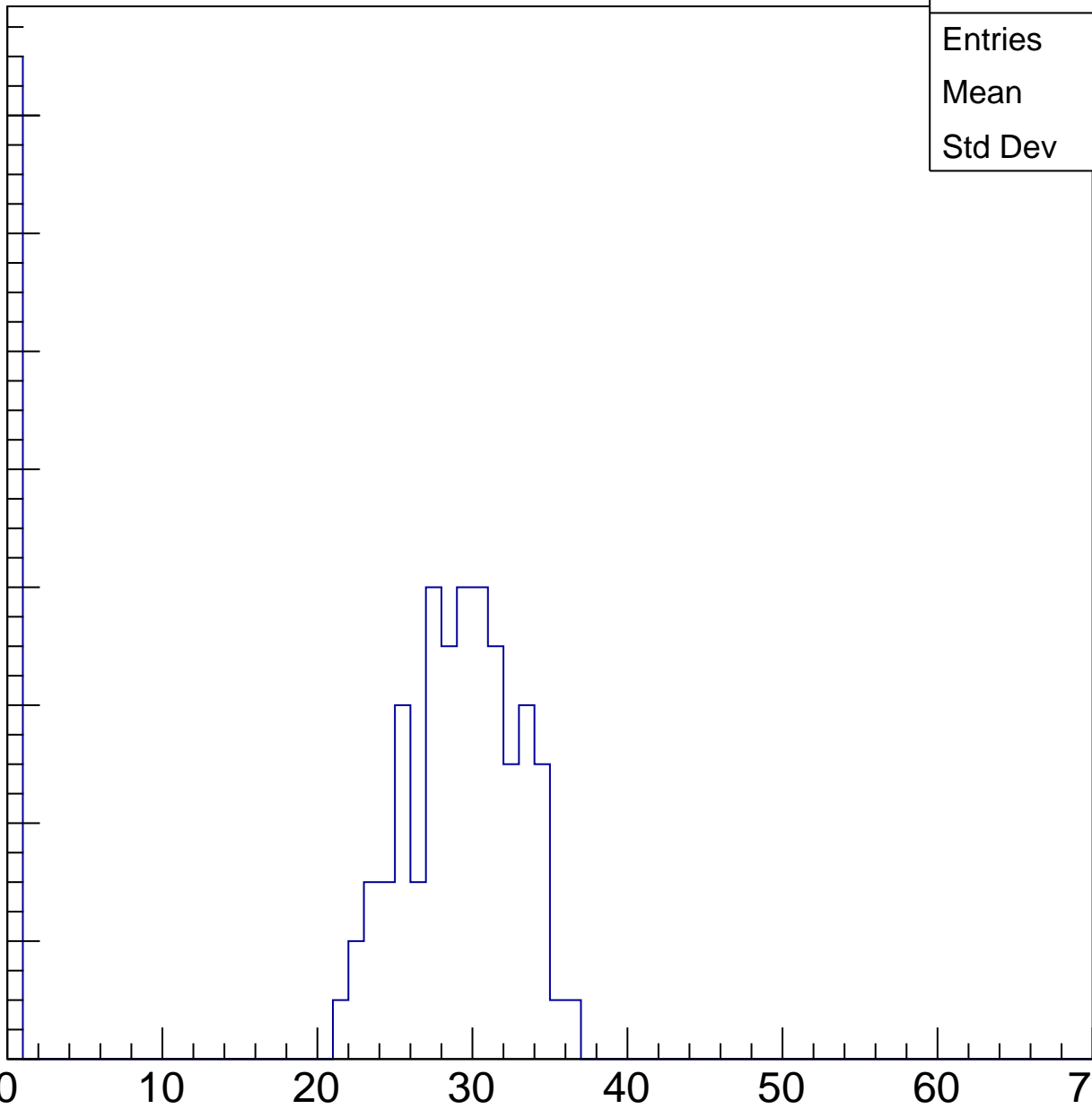
calib_packv5_041523_1651.root, FC#0, port C2

Entries	91
Mean	23.45
Std Dev	11.67

Entry

16
14
12
10
8
6
4
2
0

ampl

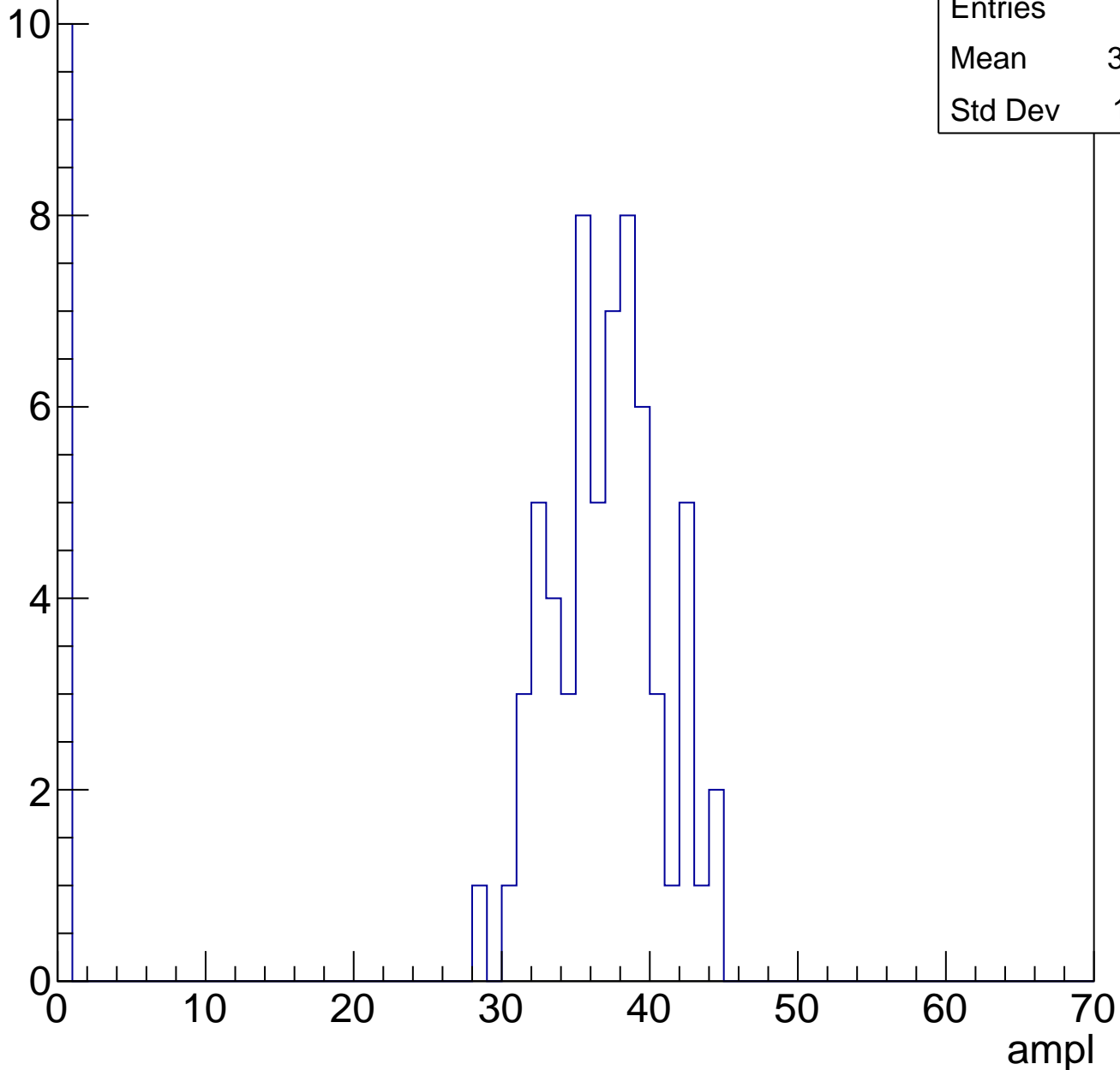


B1L103S, U9-ch125, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	73
Mean	31.56
Std Dev	13.01

Entry

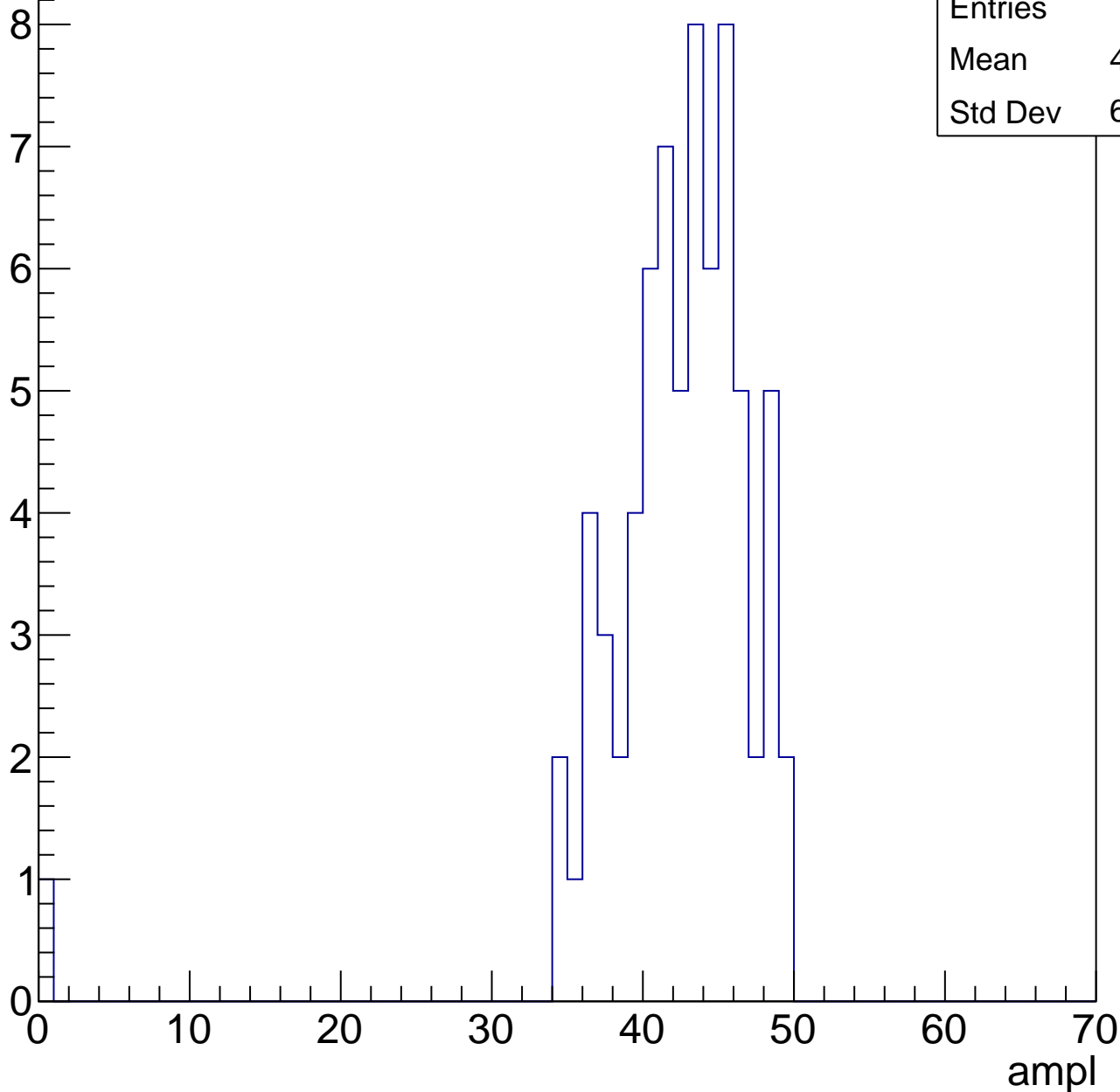


B1L103S, U9-ch125, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	41.65
Std Dev	6.237

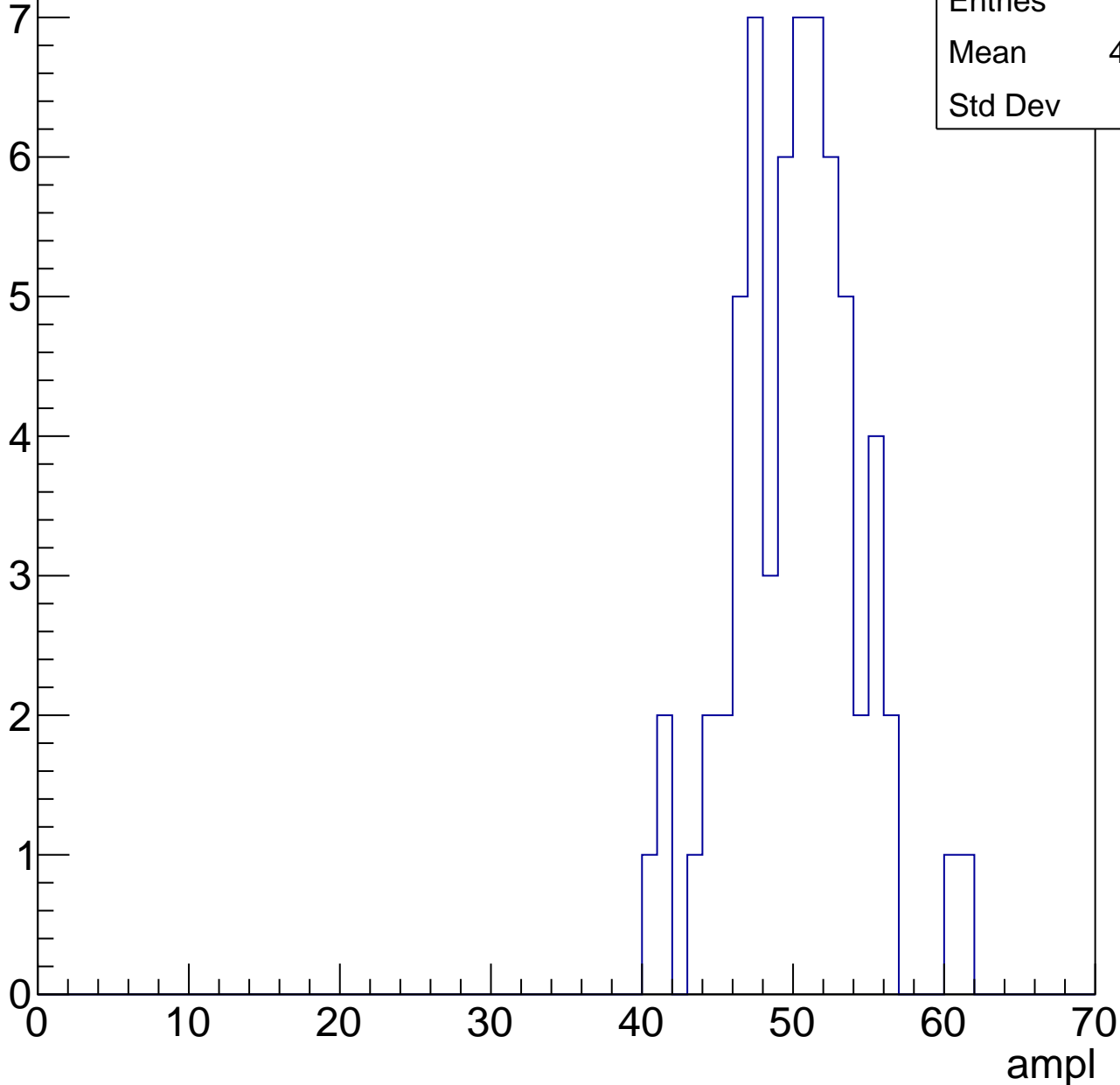


B1L103S, U9-ch125, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	49.77
Std Dev	4.13

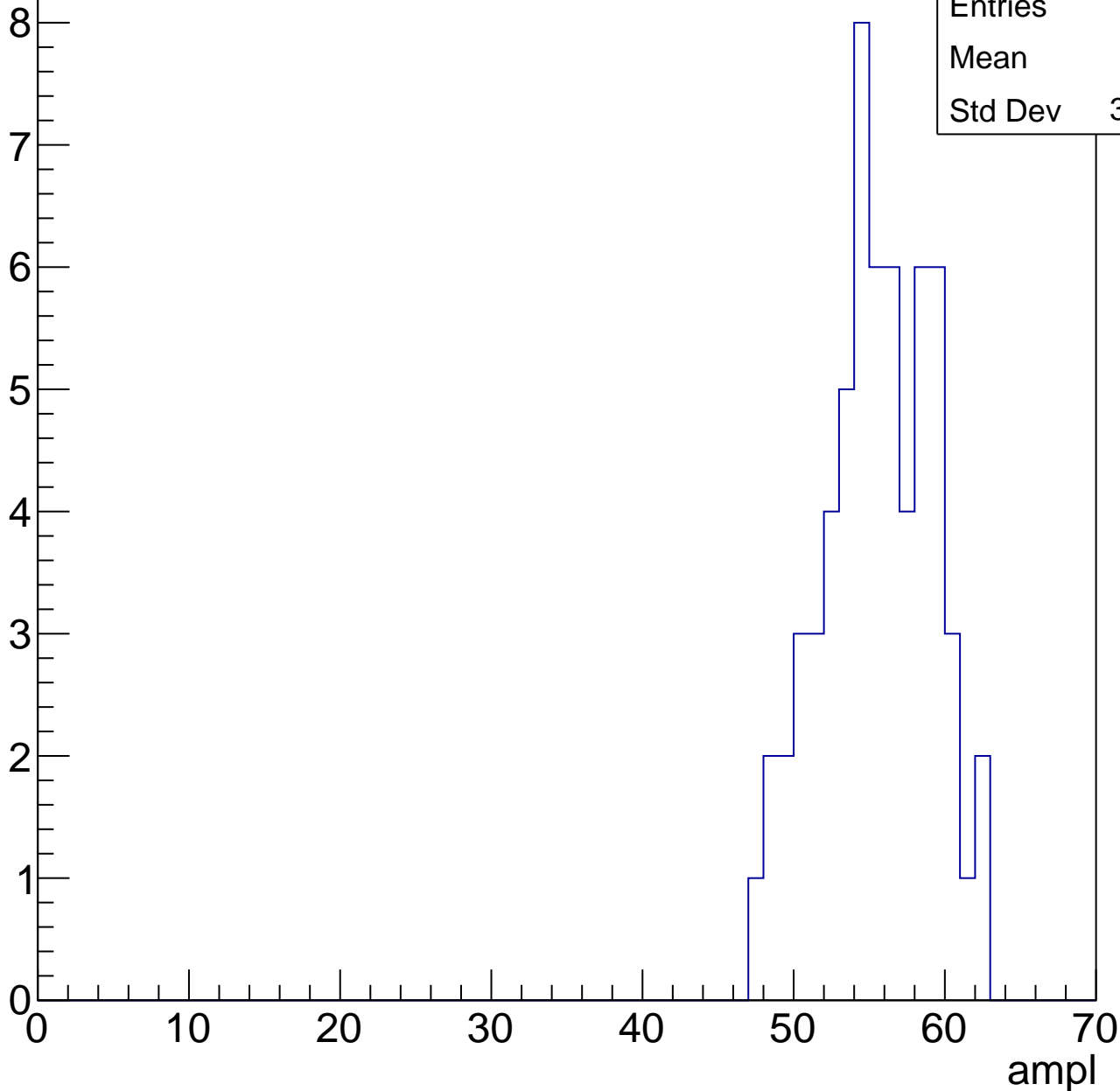


B1L103S, U9-ch125, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	55
Std Dev	3.597

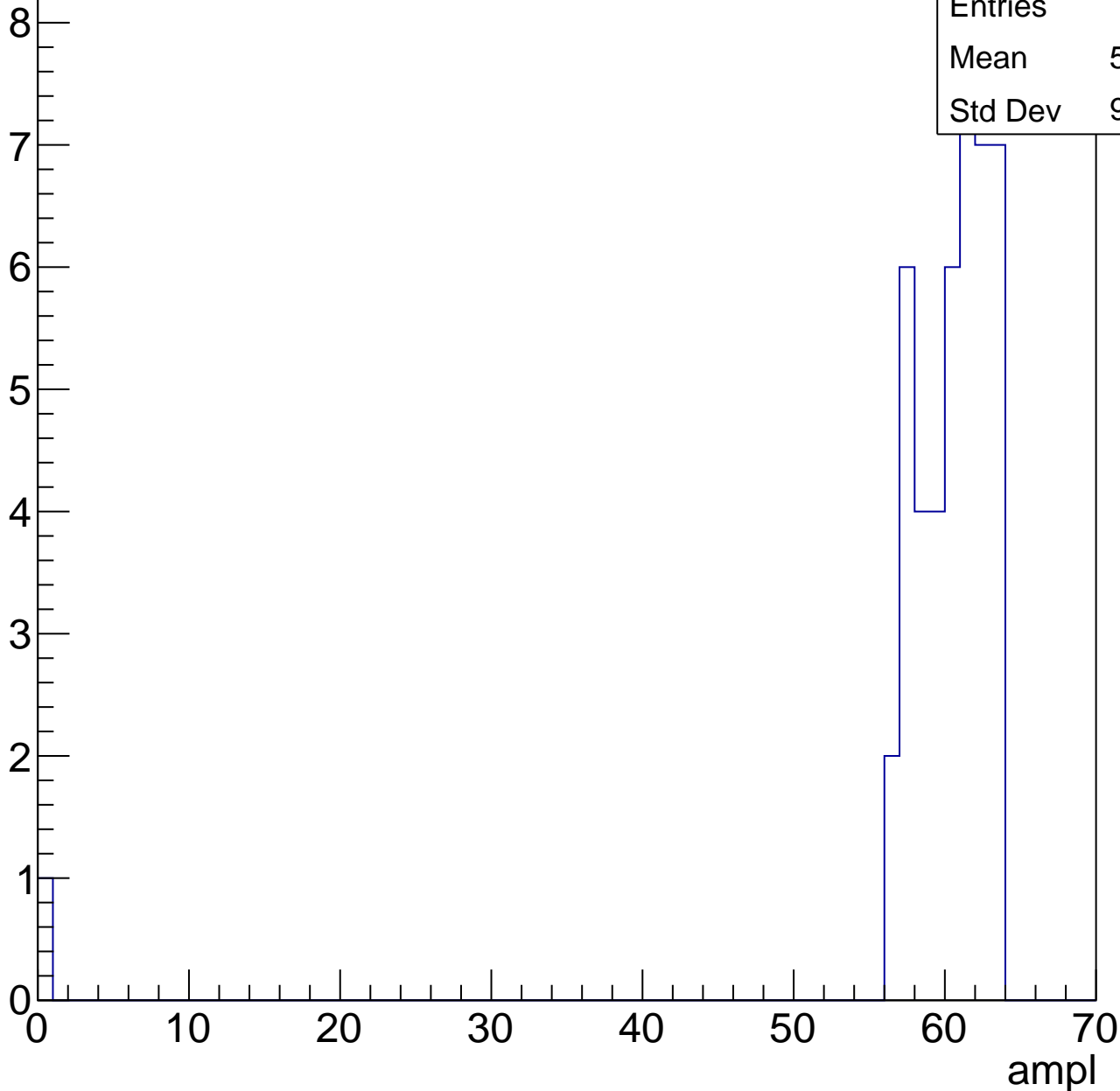


B1L103S, U9-ch125, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	45
Mean	58.78
Std Dev	9.114



B1L103S, U9-ch125, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U9-ch125, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry

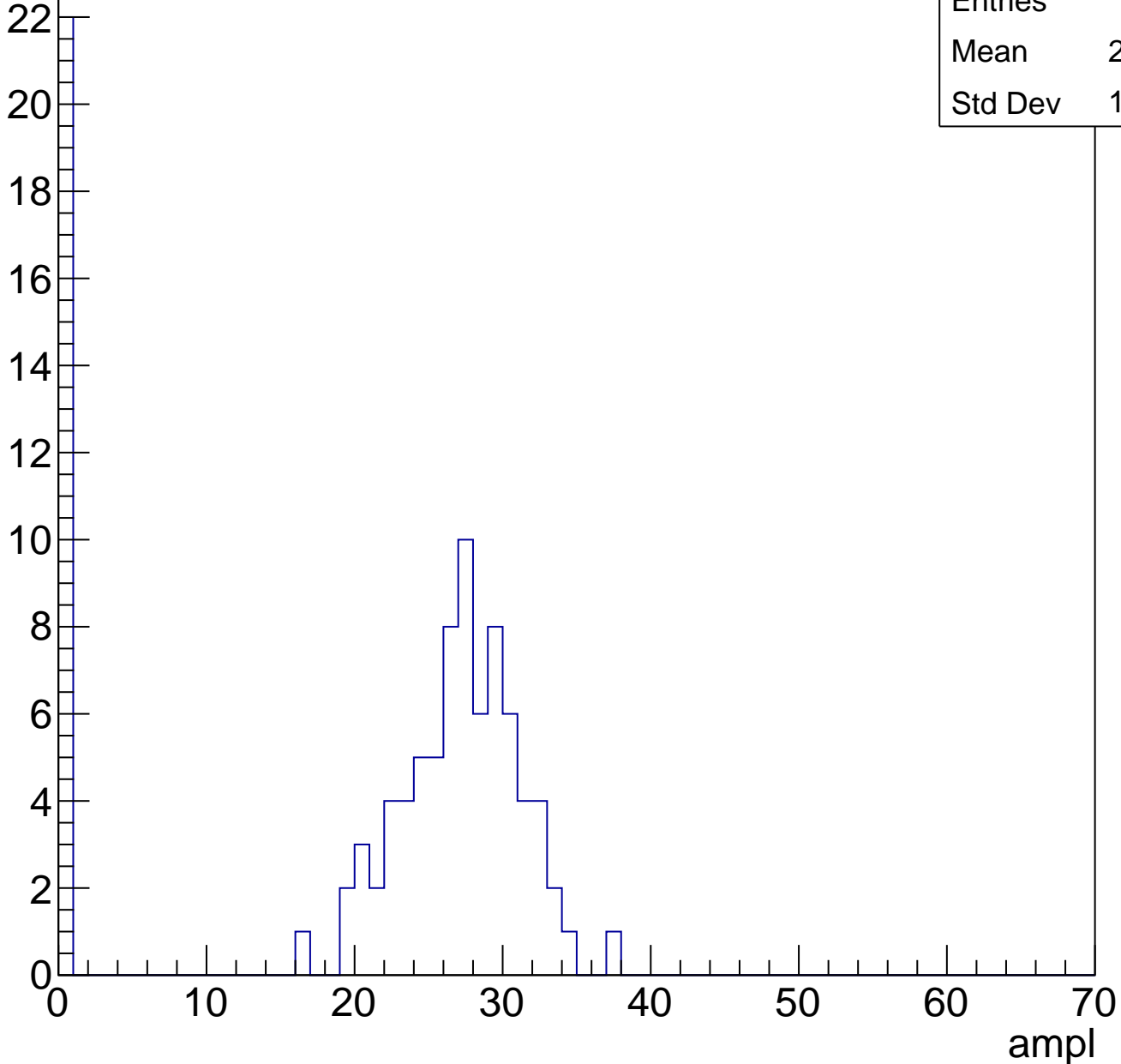


B1L103S, U9-ch126, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	98
Mean	20.69
Std Dev	11.66

Entry



B1L103S, U9-ch126, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	72
Mean	28.64
Std Dev	12.51

Entry

10

8

6

4

2

0

0

10

20

30

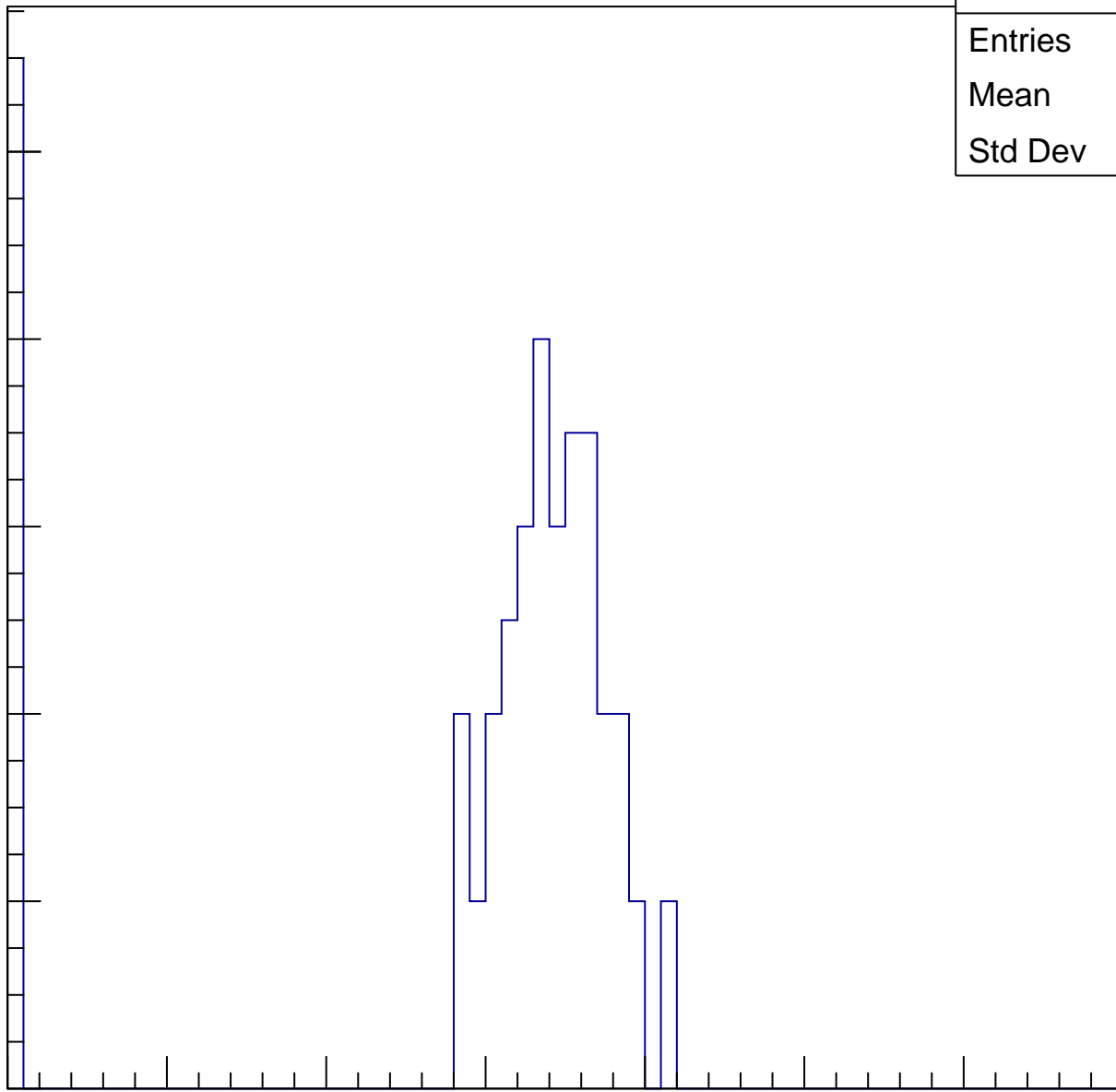
40

50

60

70

ampl



B1L103S, U9-ch126, adc2

calib_packv5_041523_1651.root, FC#0, port C2

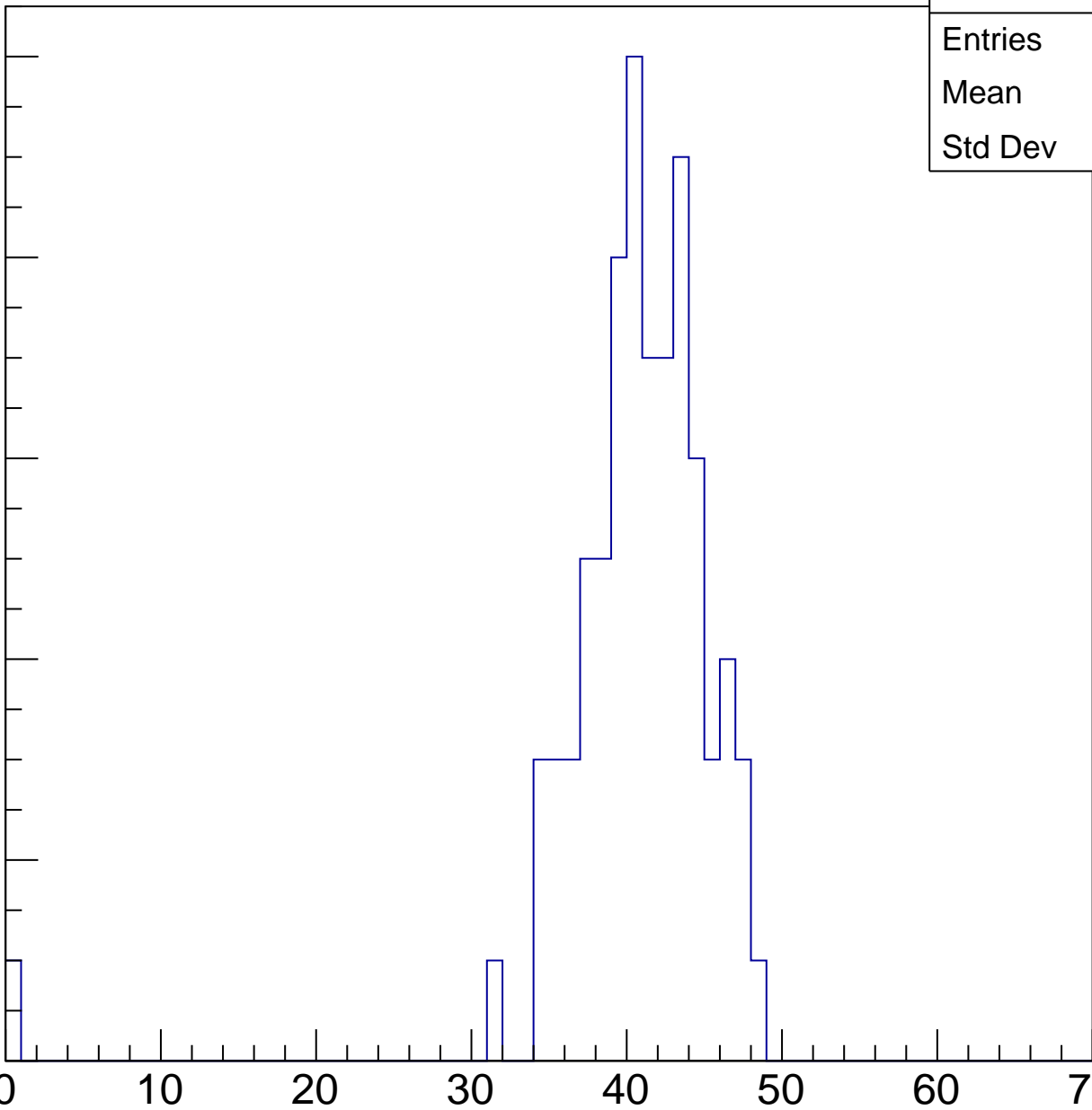
Entries	79
Mean	40.16
Std Dev	5.764

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

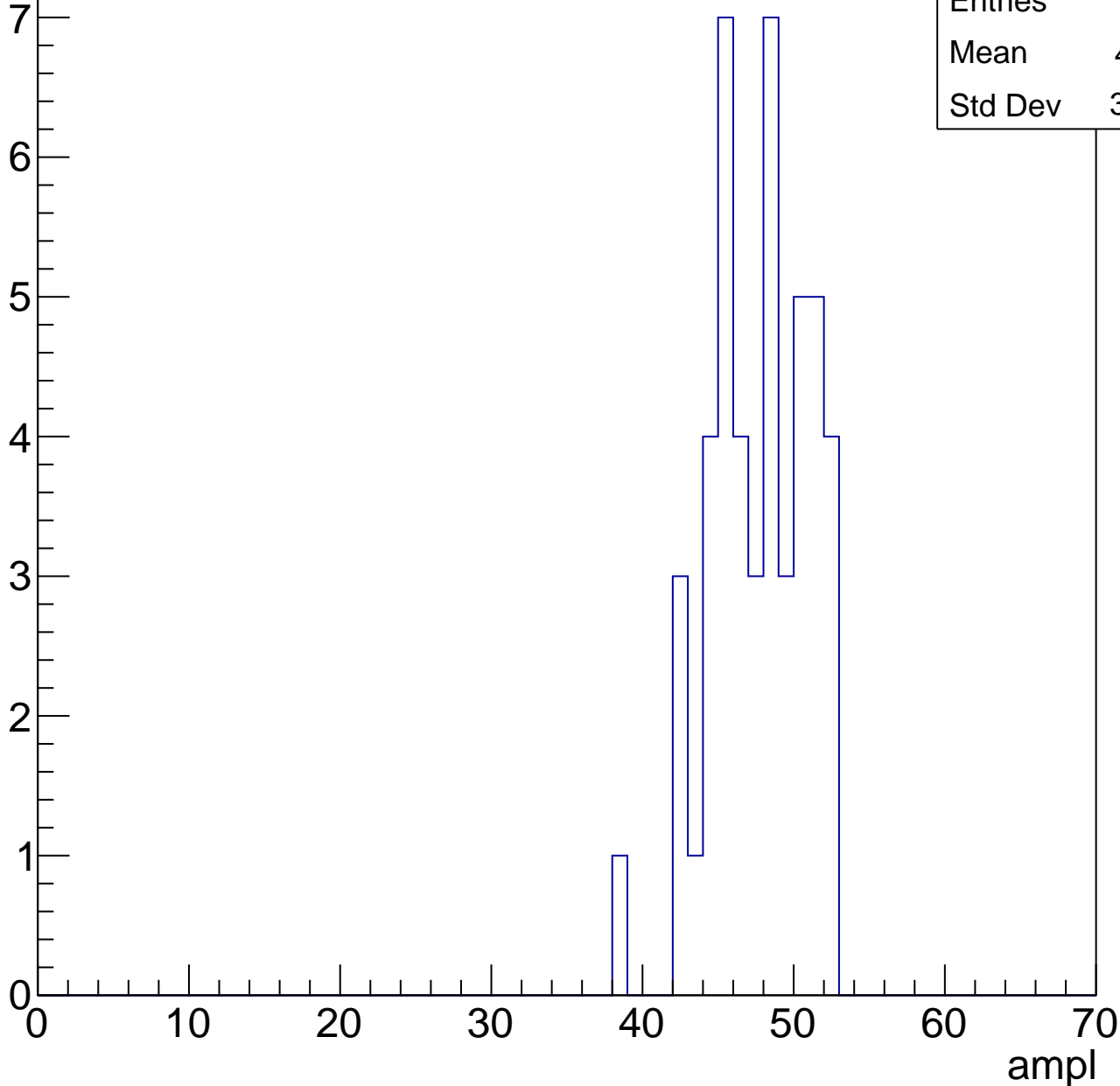


B1L103S, U9-ch126, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	47
Mean	47.21
Std Dev	3.202



B1L103S, U9-ch126, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	68
Mean	52.76
Std Dev	3.919

Entry

10

8

6

4

2

0

0

10

20

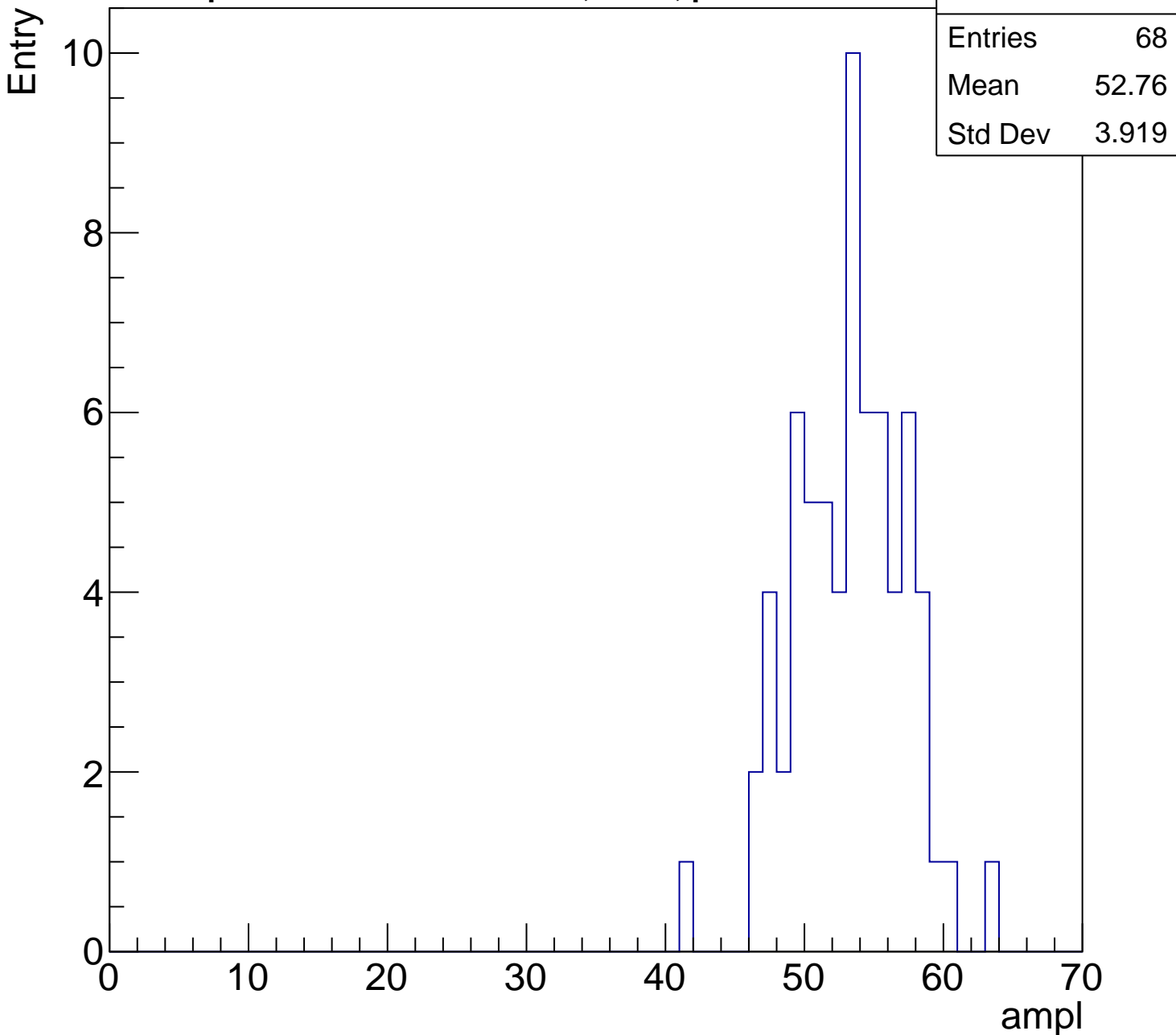
30

40

50

60

ampl

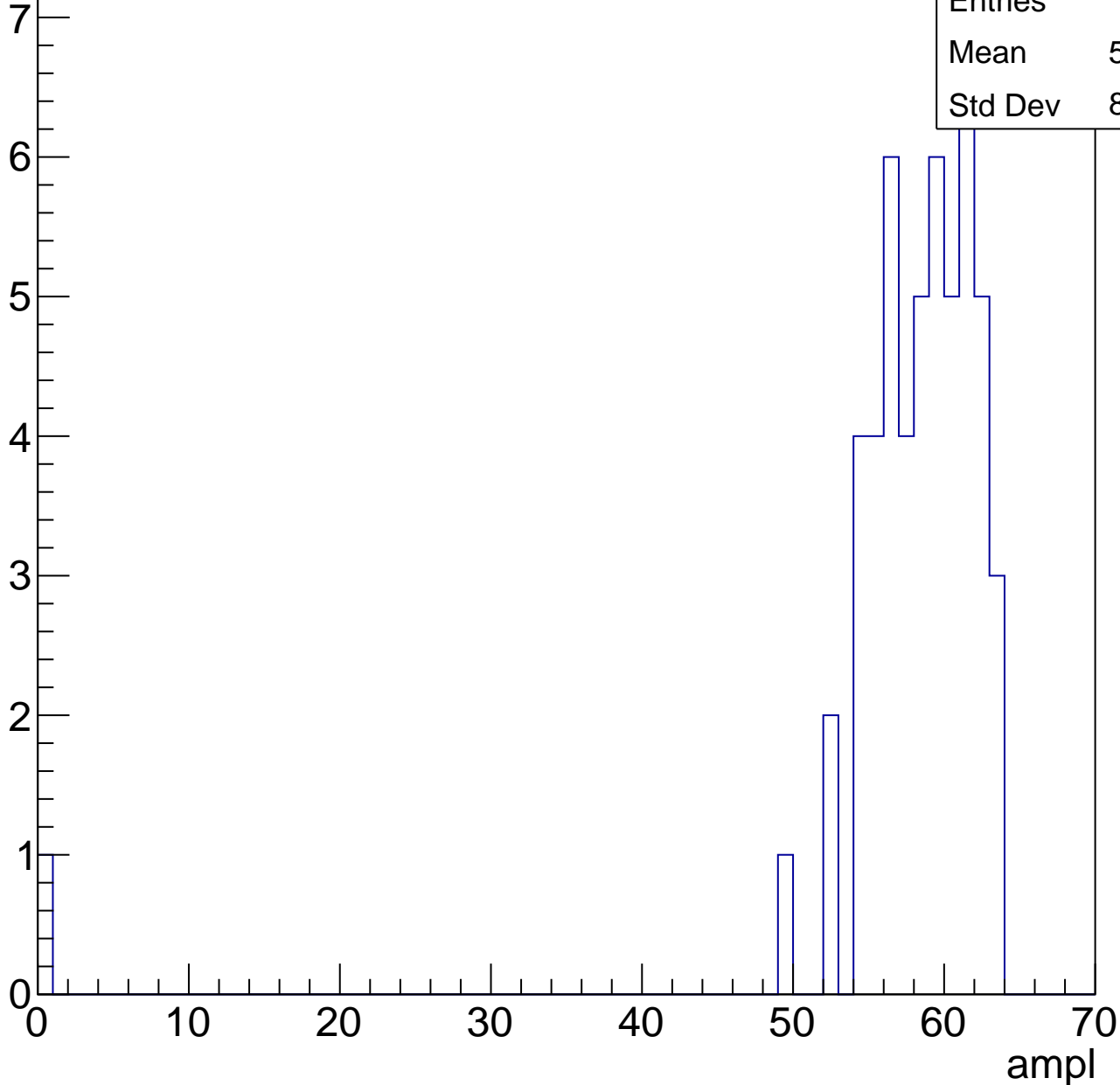


B1L103S, U9-ch126, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	57.04
Std Dev	8.512

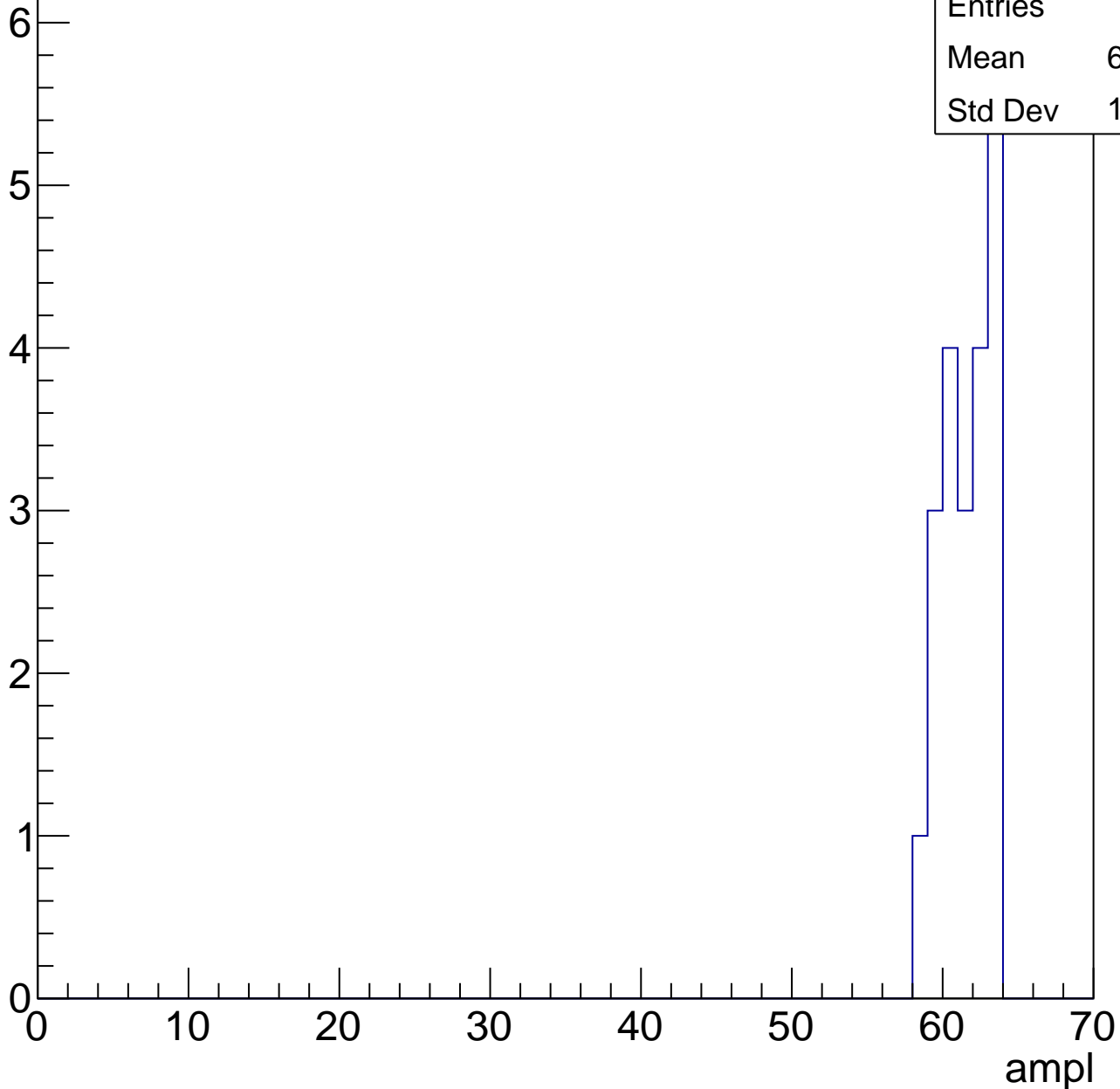


B1L103S, U9-ch126, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	21
Mean	61.14
Std Dev	1.582



B1L103S, U9-ch126, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51

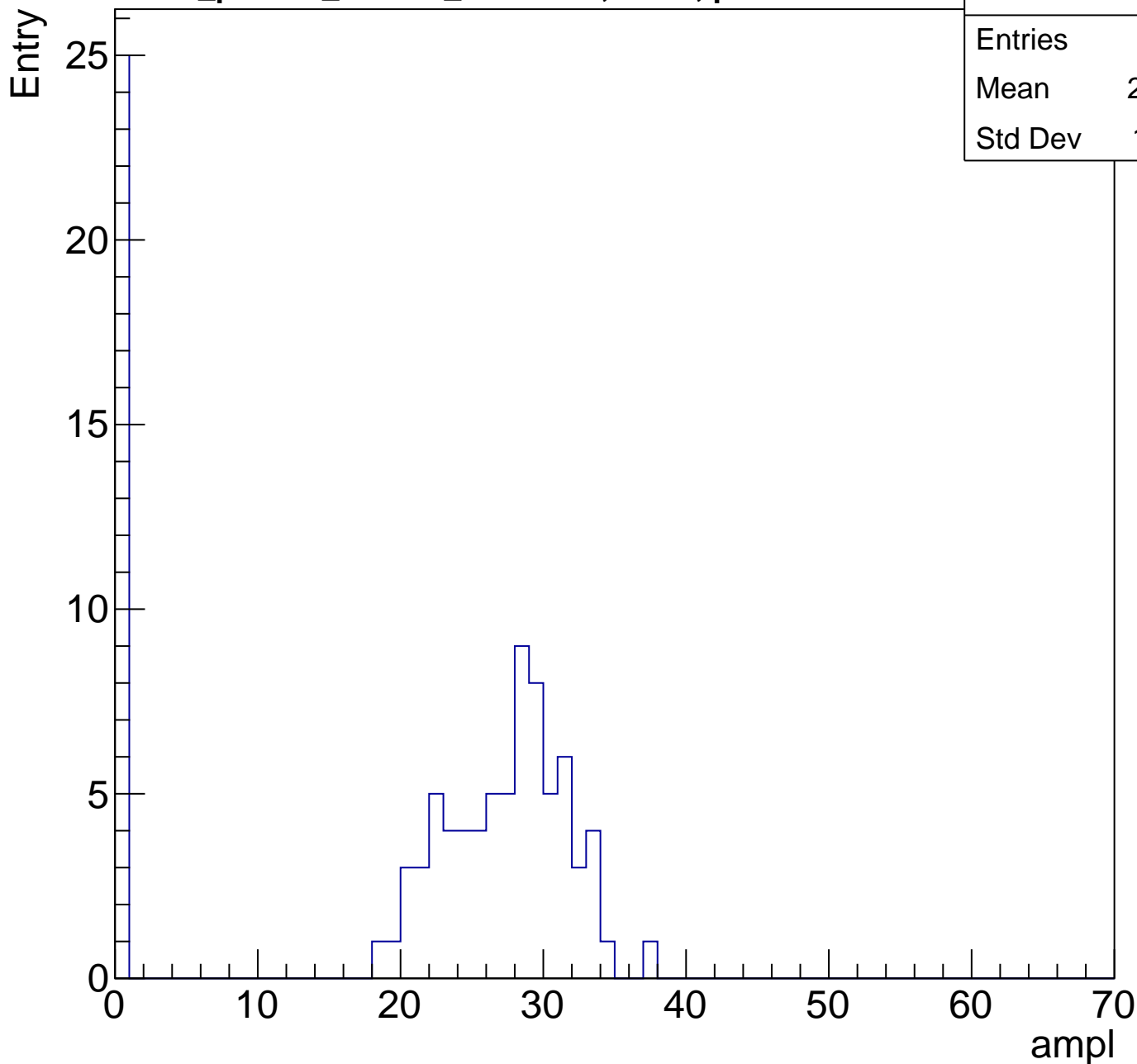
Entry



B1L103S, U9-ch127, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	97
Mean	20.02
Std Dev	12.31

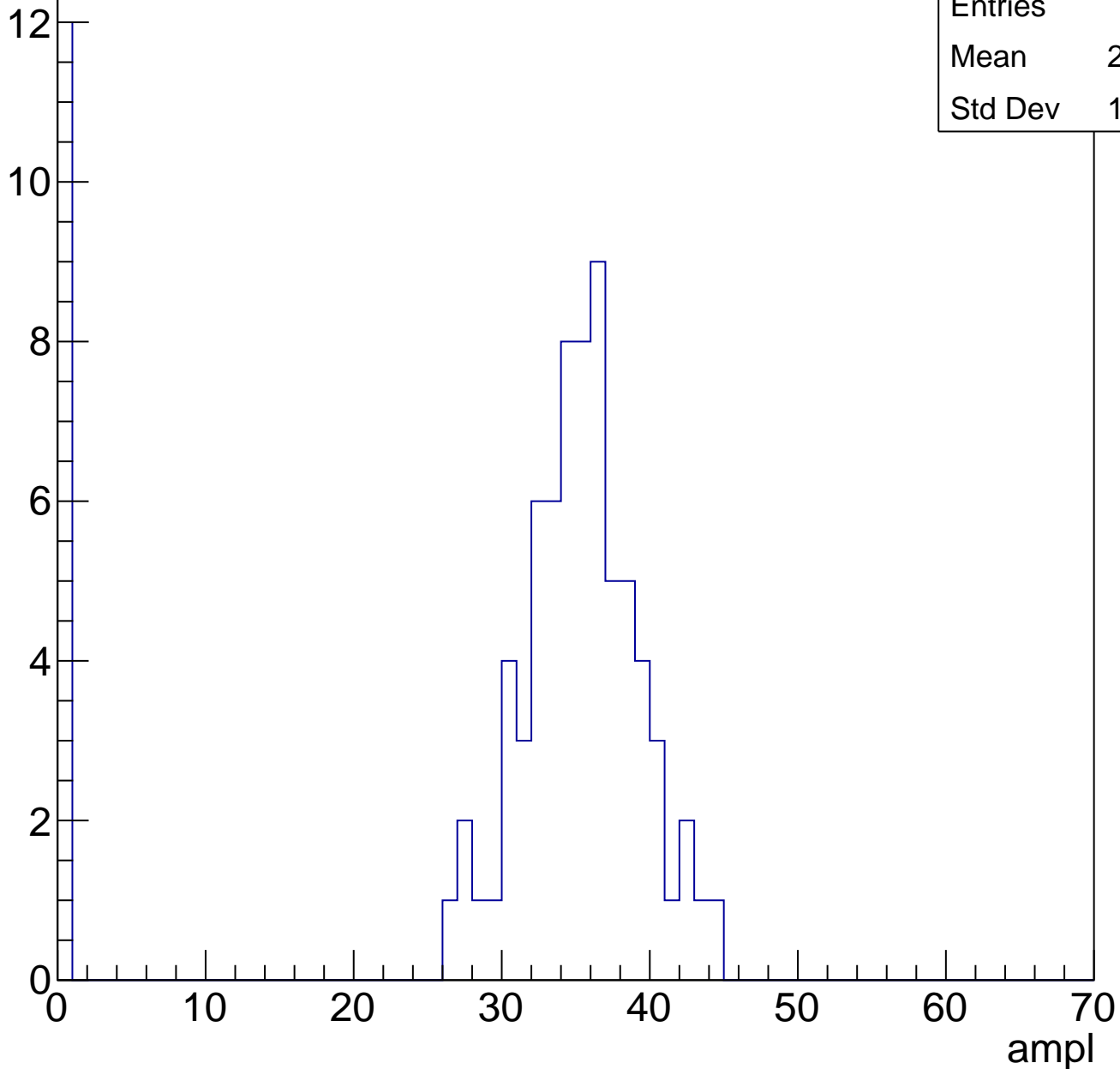


B1L103S, U9-ch127, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	83
Mean	29.87
Std Dev	12.77

Entry

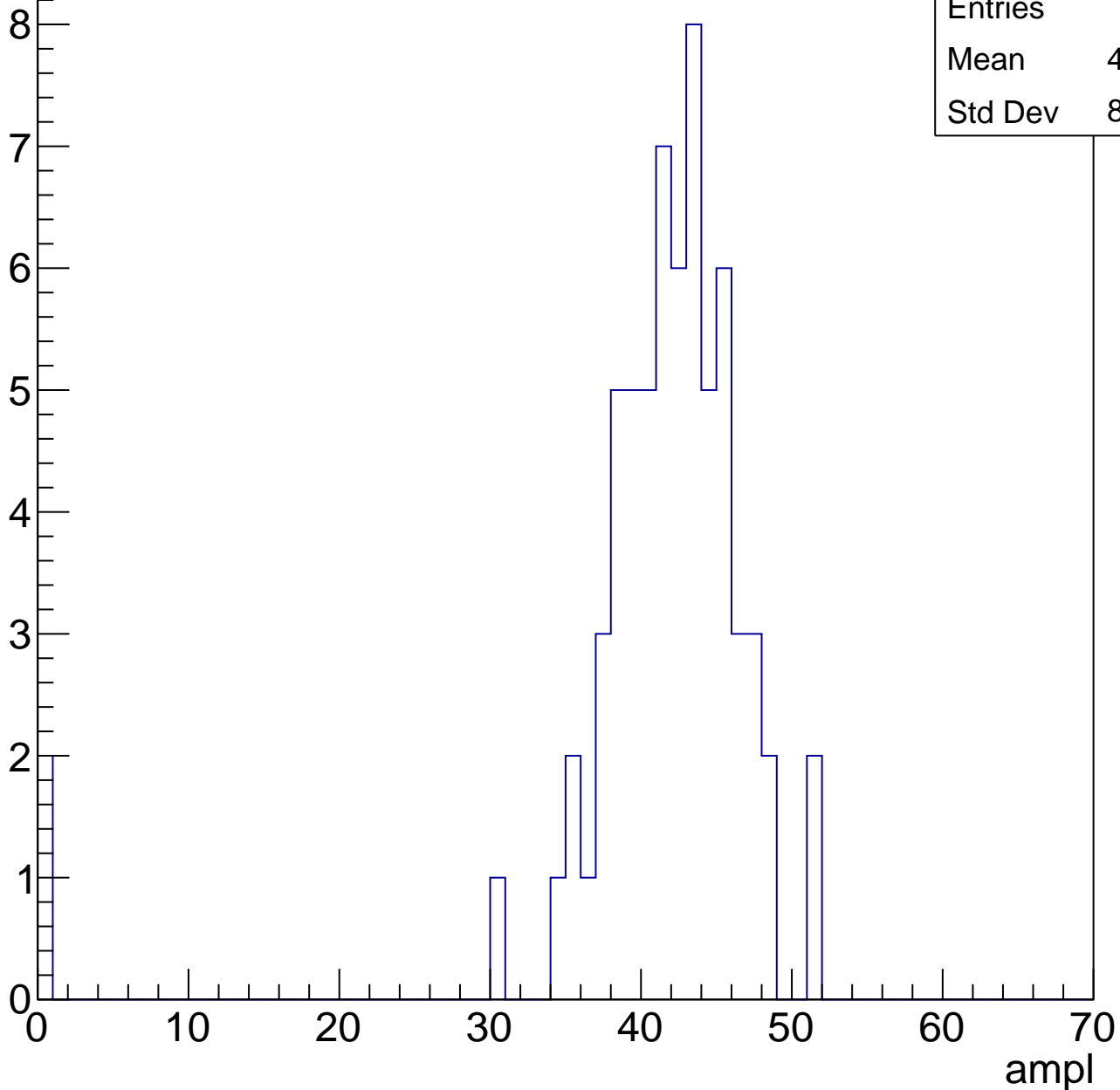


B1L103S, U9-ch127, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	40.54
Std Dev	8.097



B1L103S, U9-ch127, adc3

calib_packv5_041523_1651.root, FC#0, port C2

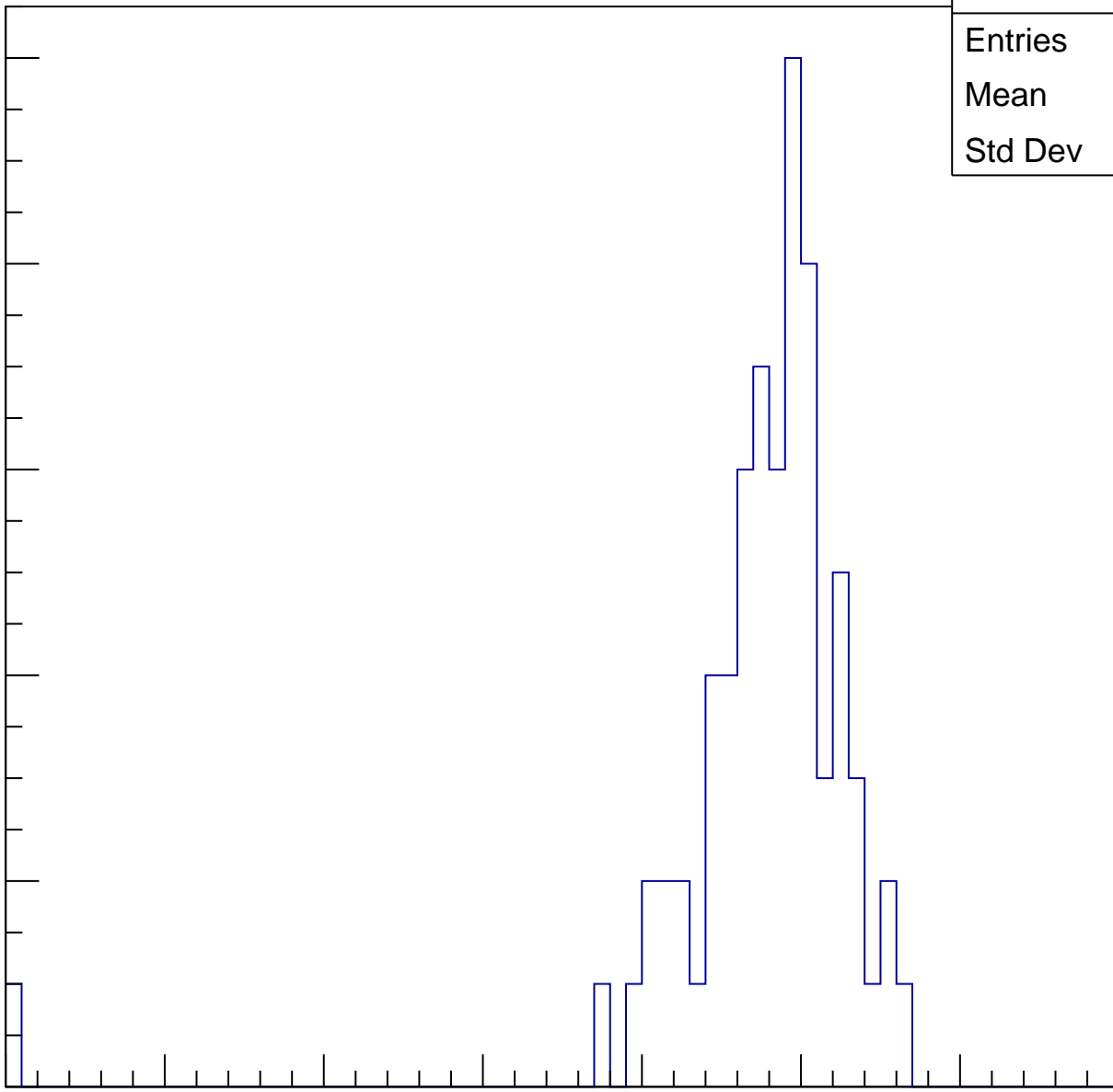
Entries	70
Mean	47.09
Std Dev	6.89

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

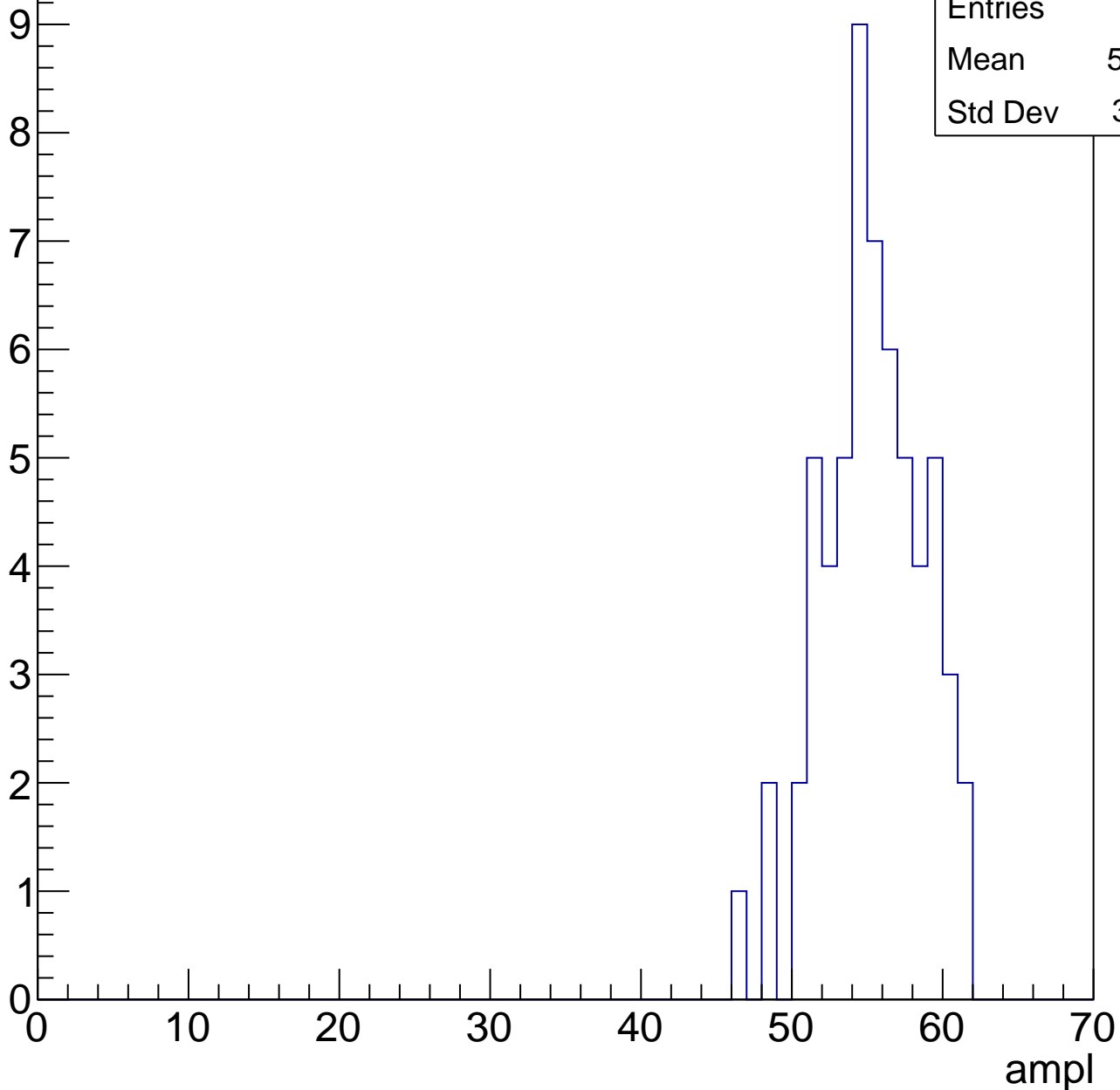


B1L103S, U9-ch127, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	54.85
Std Dev	3.321

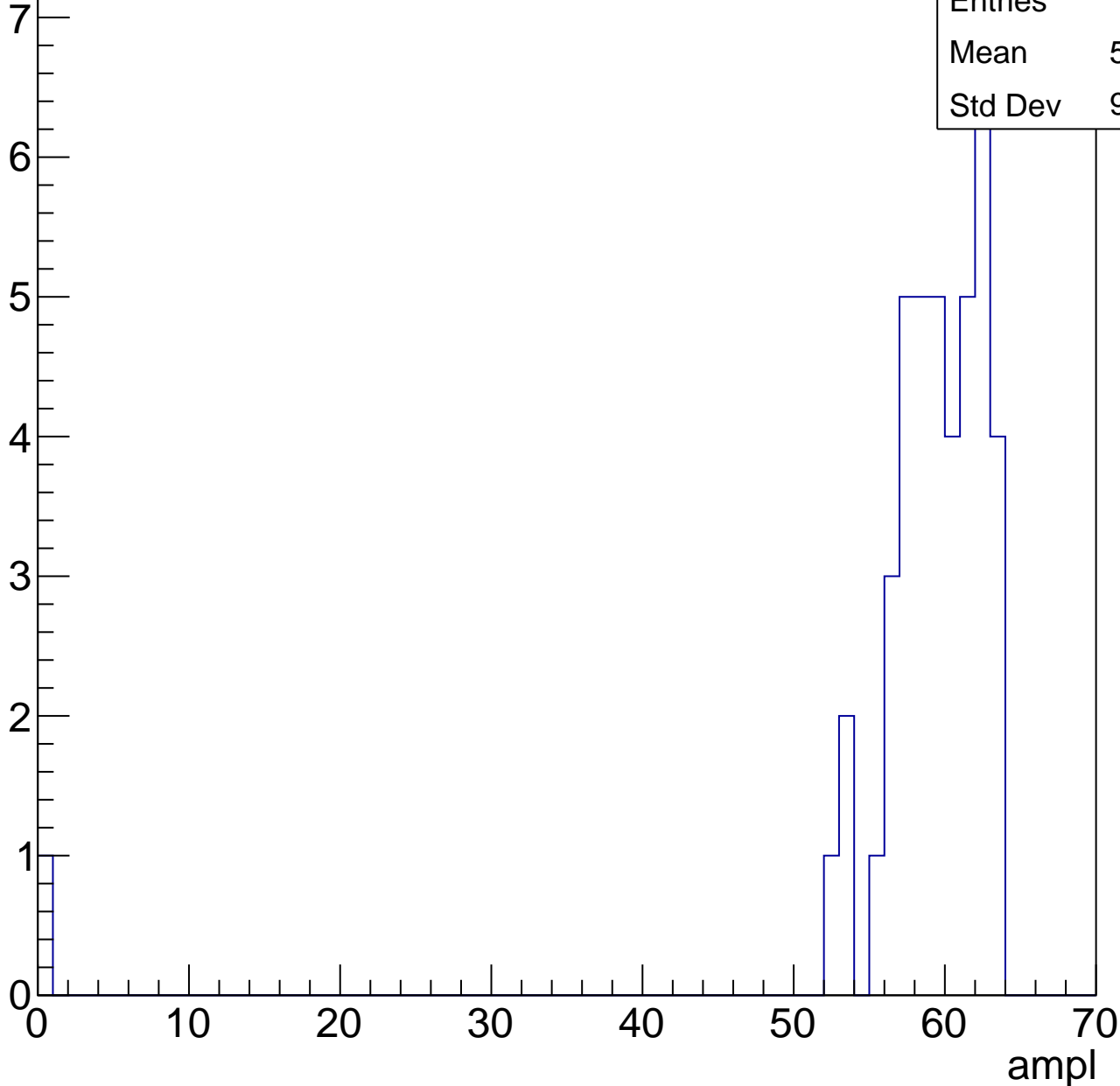


B1L103S, U9-ch127, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	43
Mean	57.72
Std Dev	9.339

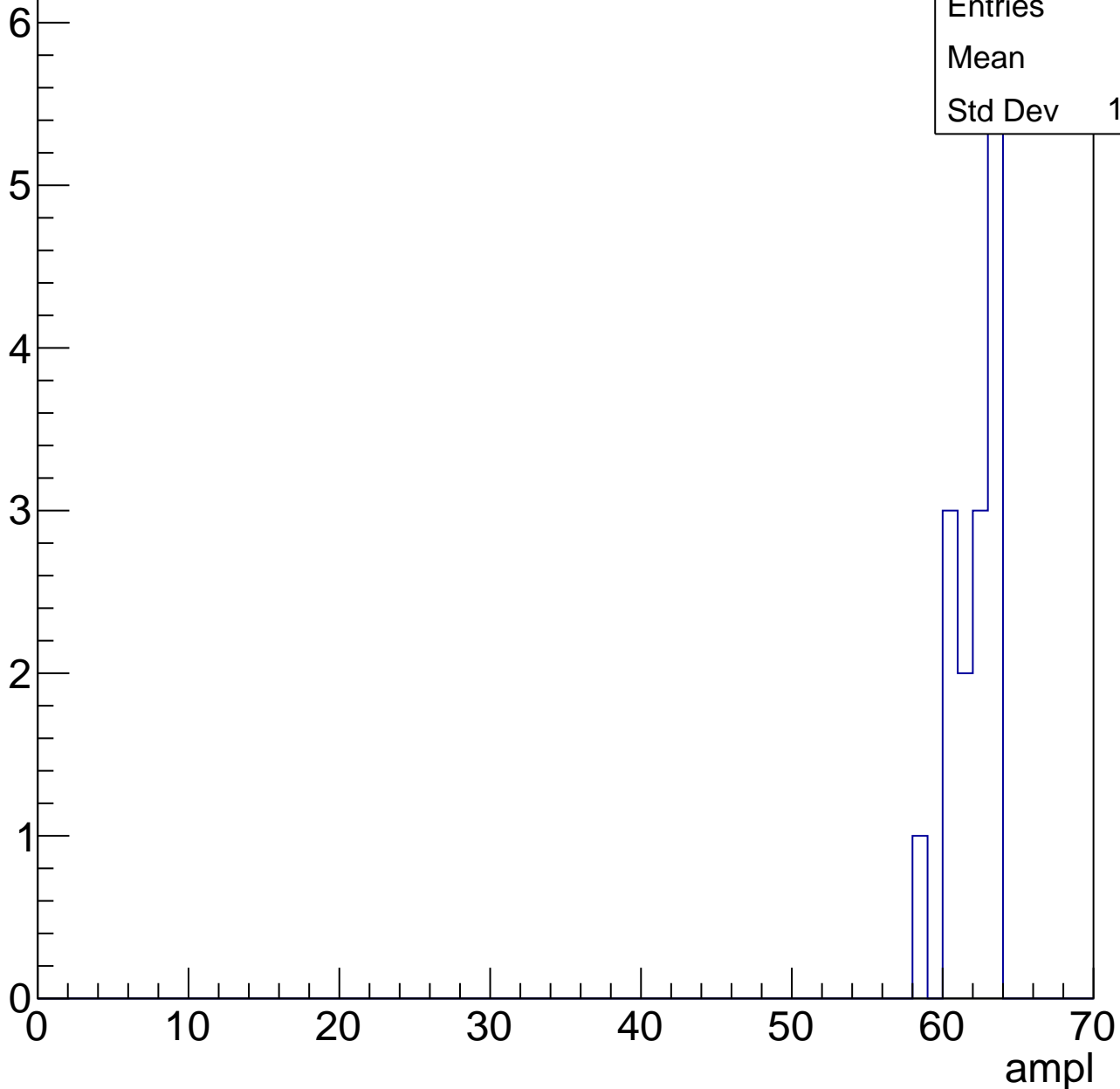


B1L103S, U9-ch127, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

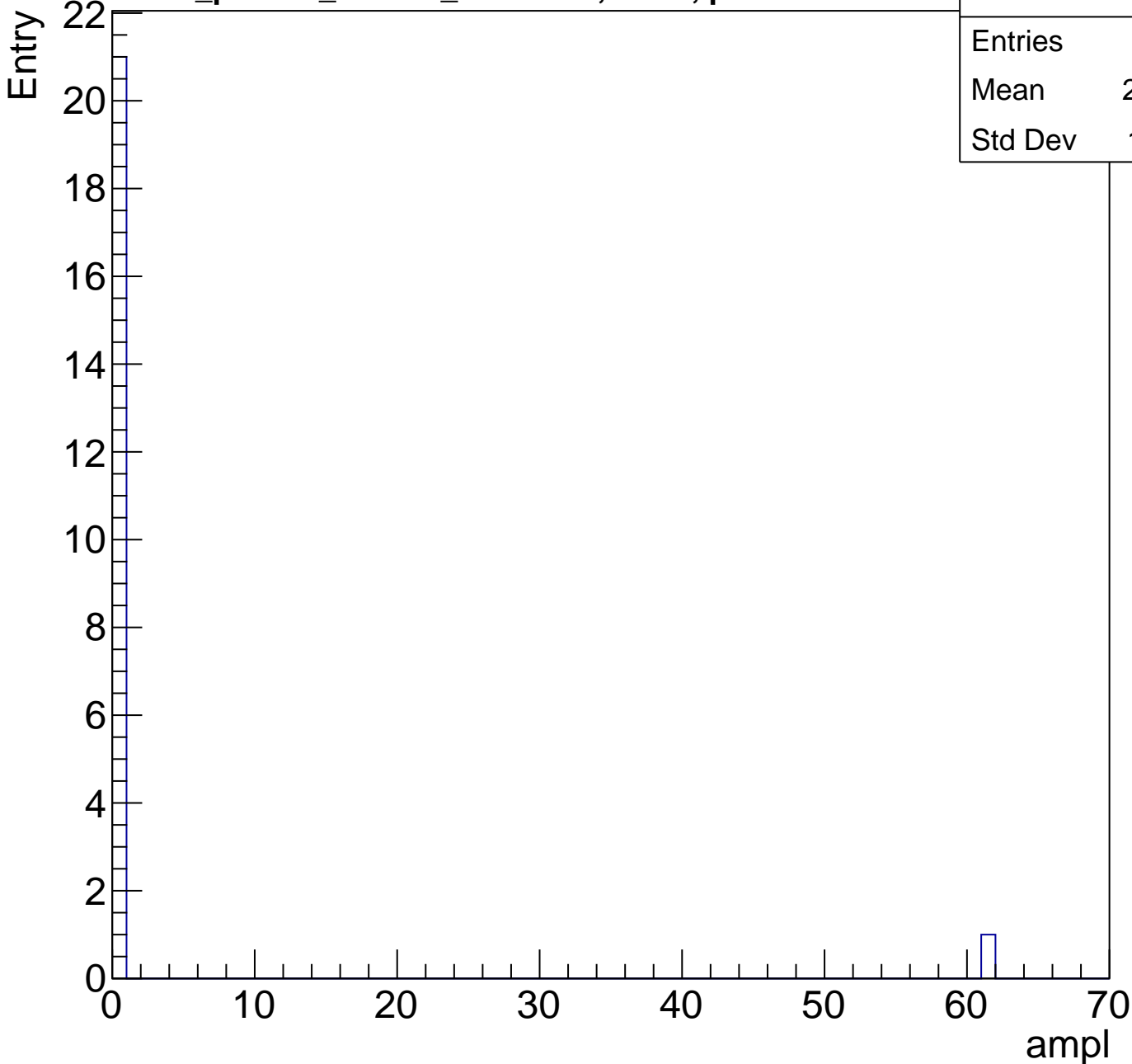
Entries	15
Mean	61.6
Std Dev	1.497



B1L103S, U9-ch127, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	22
Mean	2.773
Std Dev	12.71



B1L103S, U9-ch127, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	22
Mean	2.773
Std Dev	12.71

Entry

