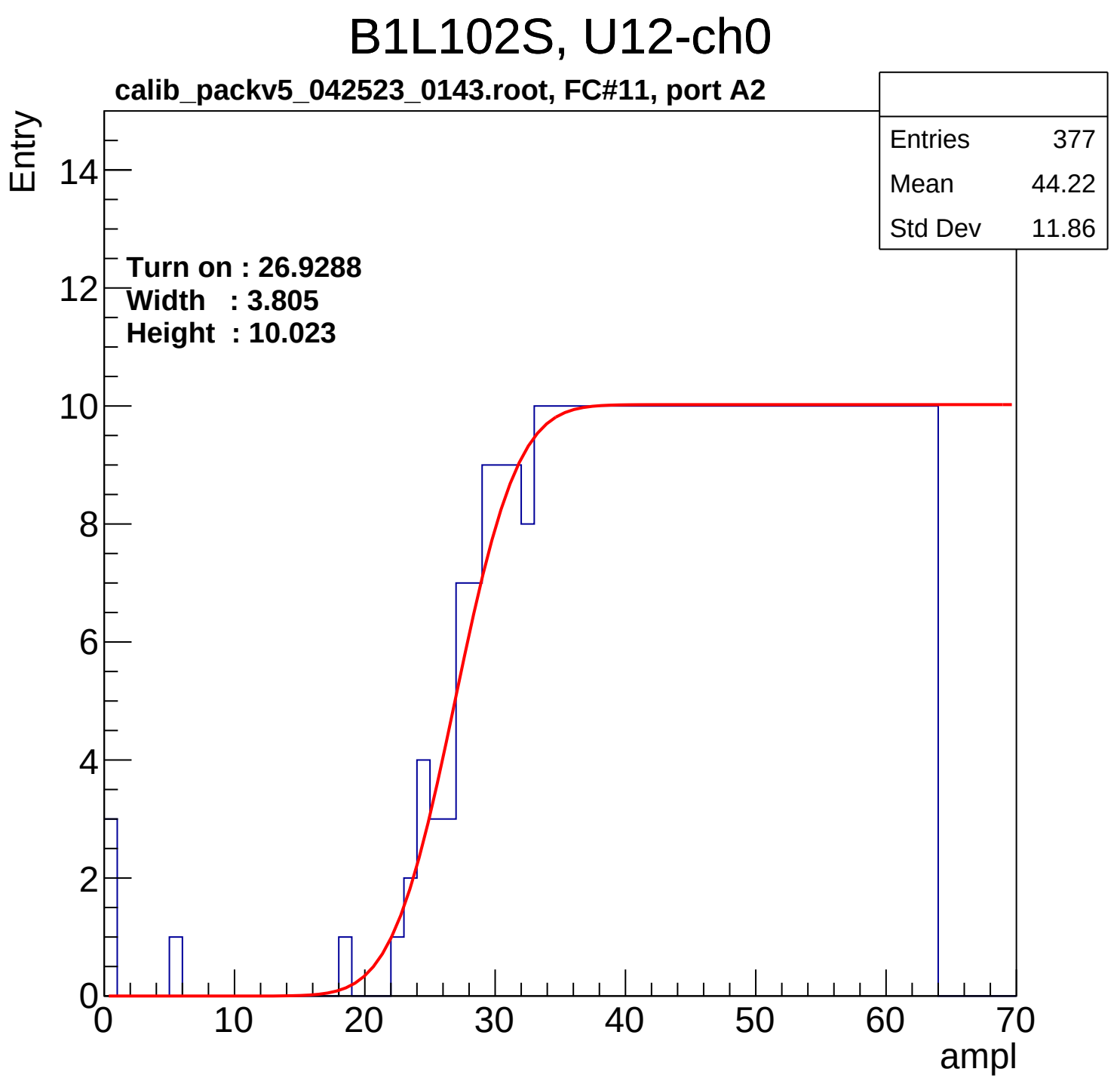
B1L102S, U12-ch0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.22
Std Dev 11.86
Turn on : 26.9288
Width : 3.805
Height : 10.023
Entry
ampl
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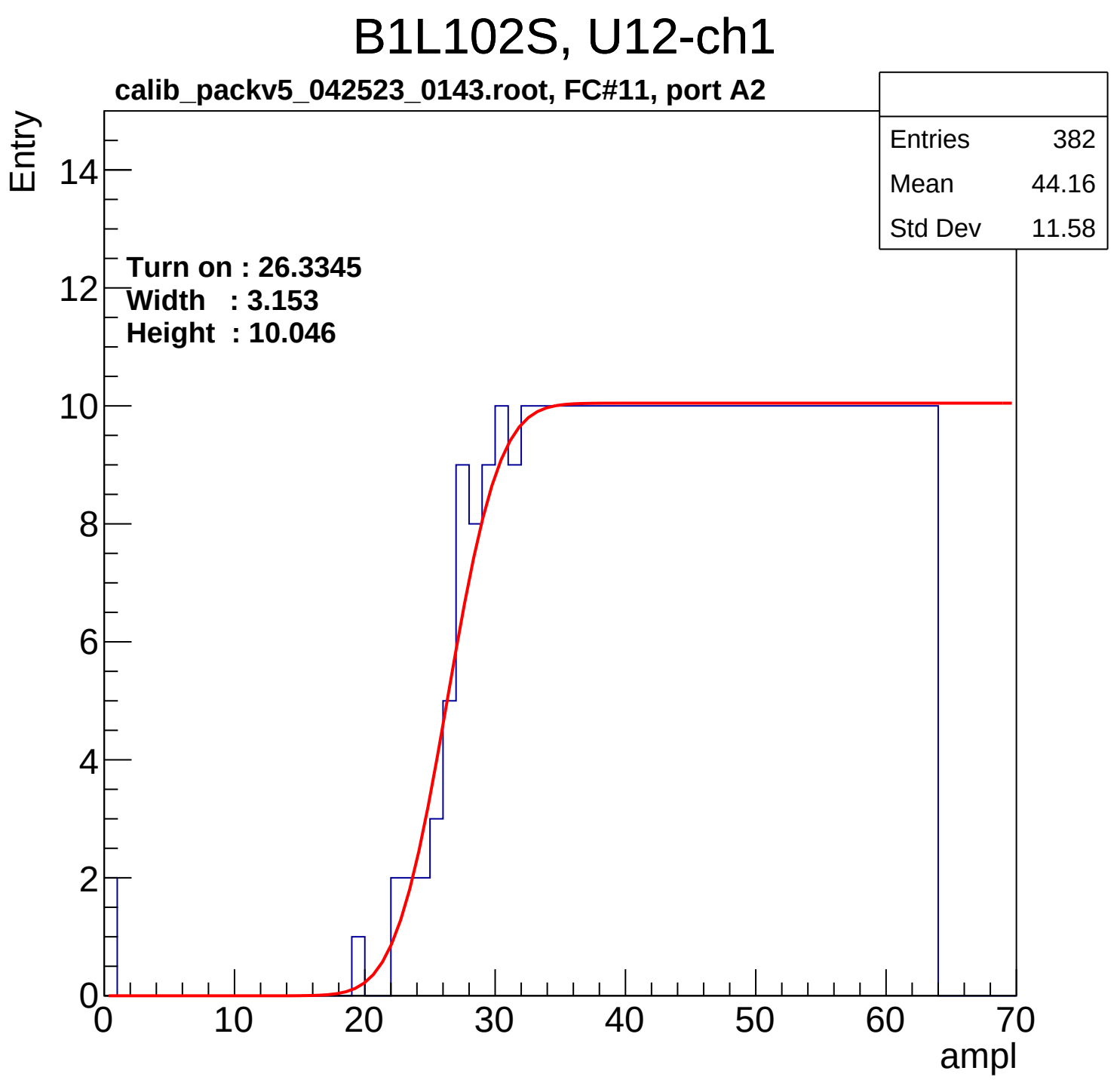
B1L102S, U12-ch1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.16
Std Dev 11.58
Turn on : 26.3345
Width : 3.153
Height : 10.046
Entry
ampl
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2
4
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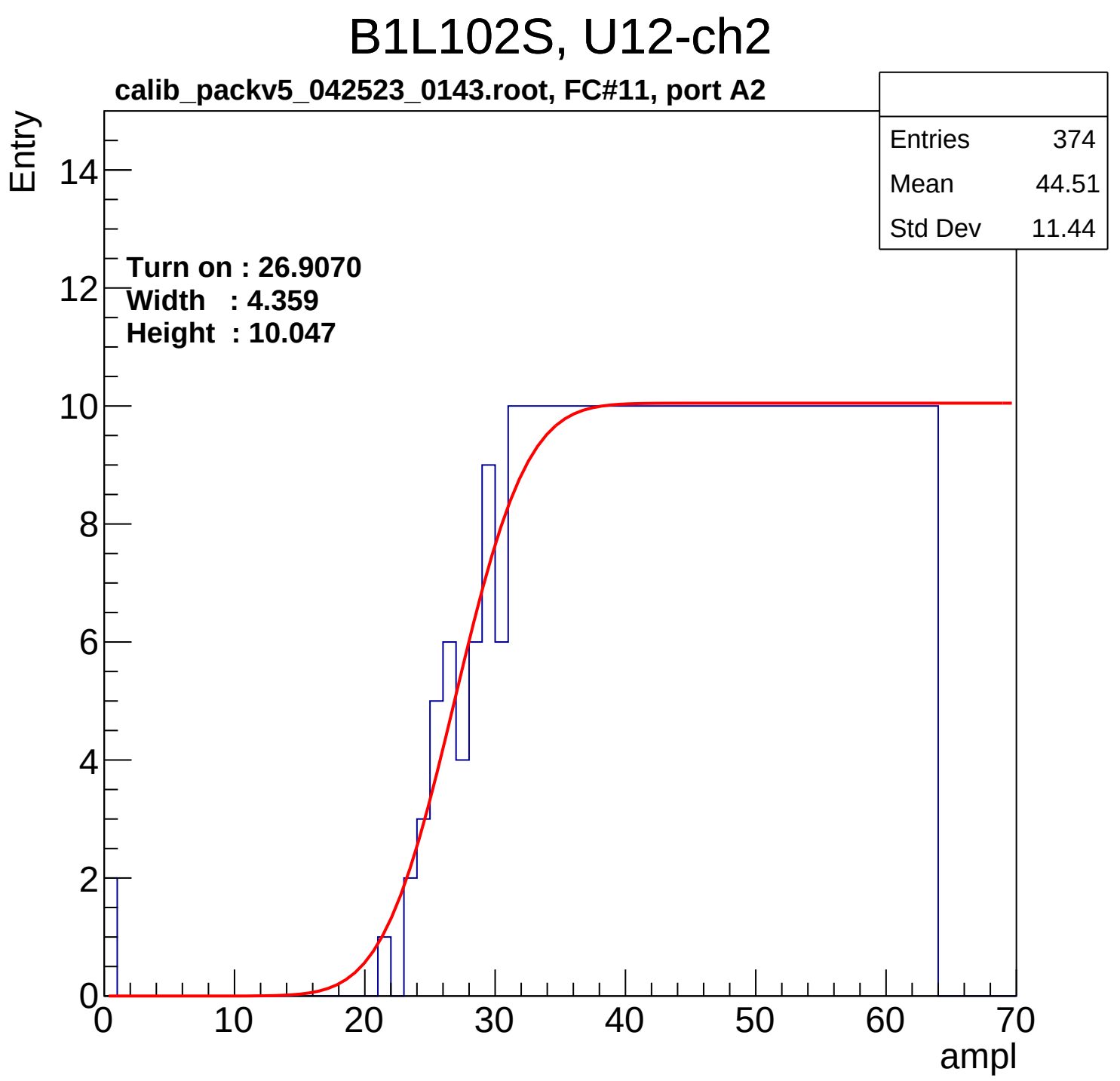
B1L102S, U12-ch2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.51
Std Dev 11.44
Turn on : 26.9070
Width : 4.359
Height : 10.047
Entry
ampl
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2
4
6
8
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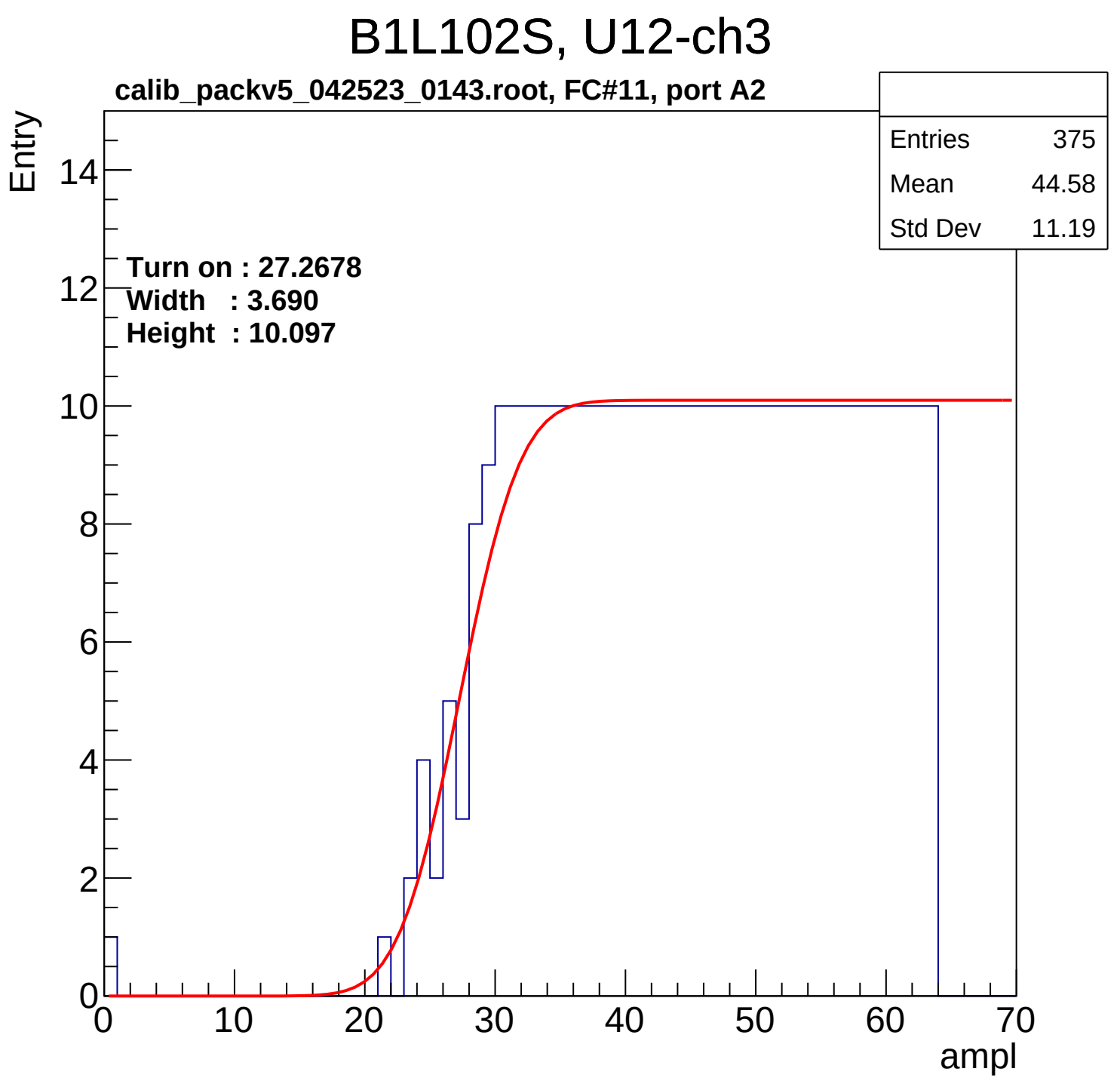
B1L102S, U12-ch3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 375
Mean 44.58
Std Dev 11.19
Turn on : 27.2678
Width : 3.690
Height : 10.097
Entry
ampl
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2
4
6
8
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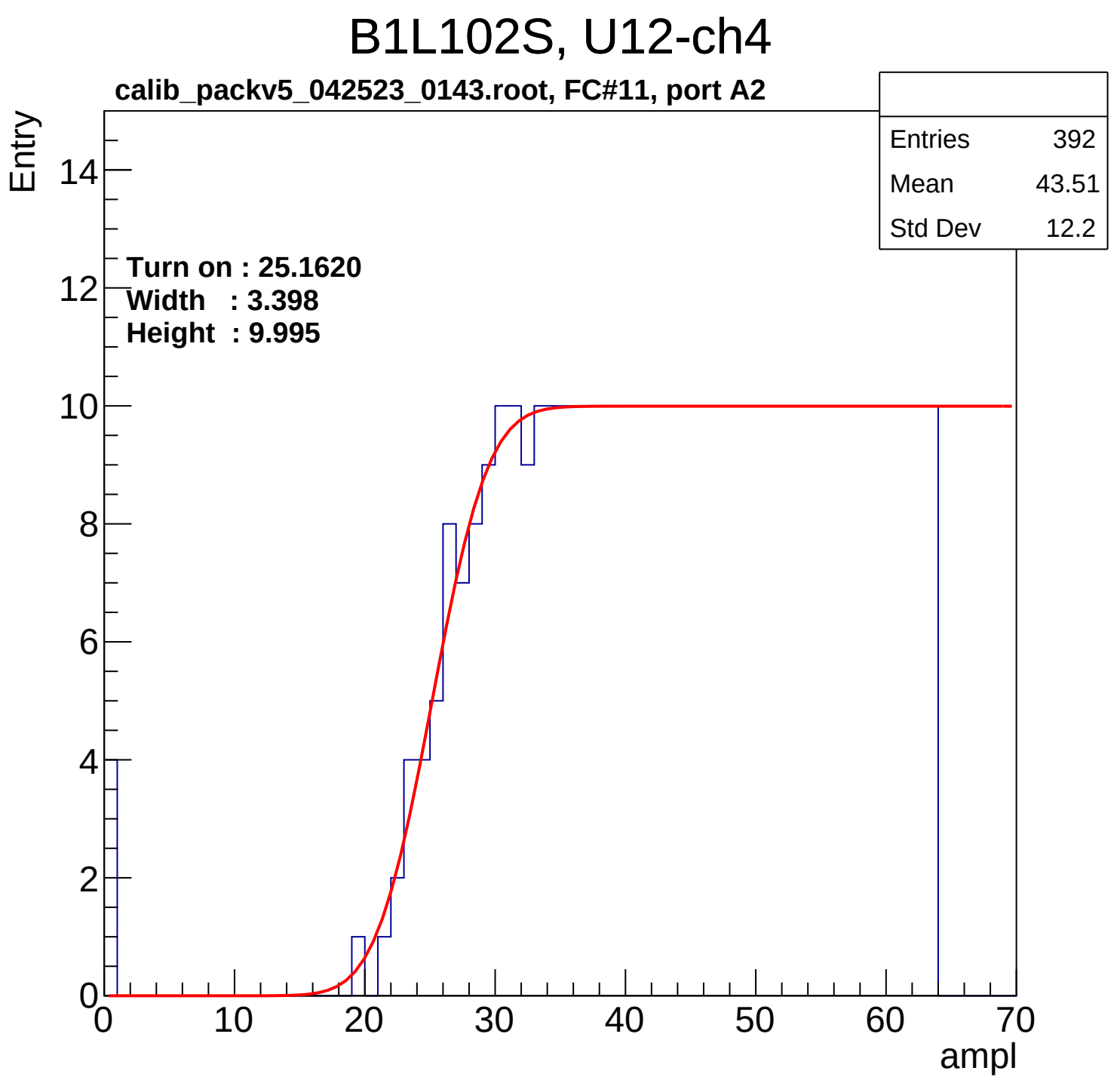
B1L102S, U12-ch4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.51
Std Dev 12.2
Turn on : 25.1620
Width : 3.398
Height : 9.995
Entry
ampl
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4
6
8
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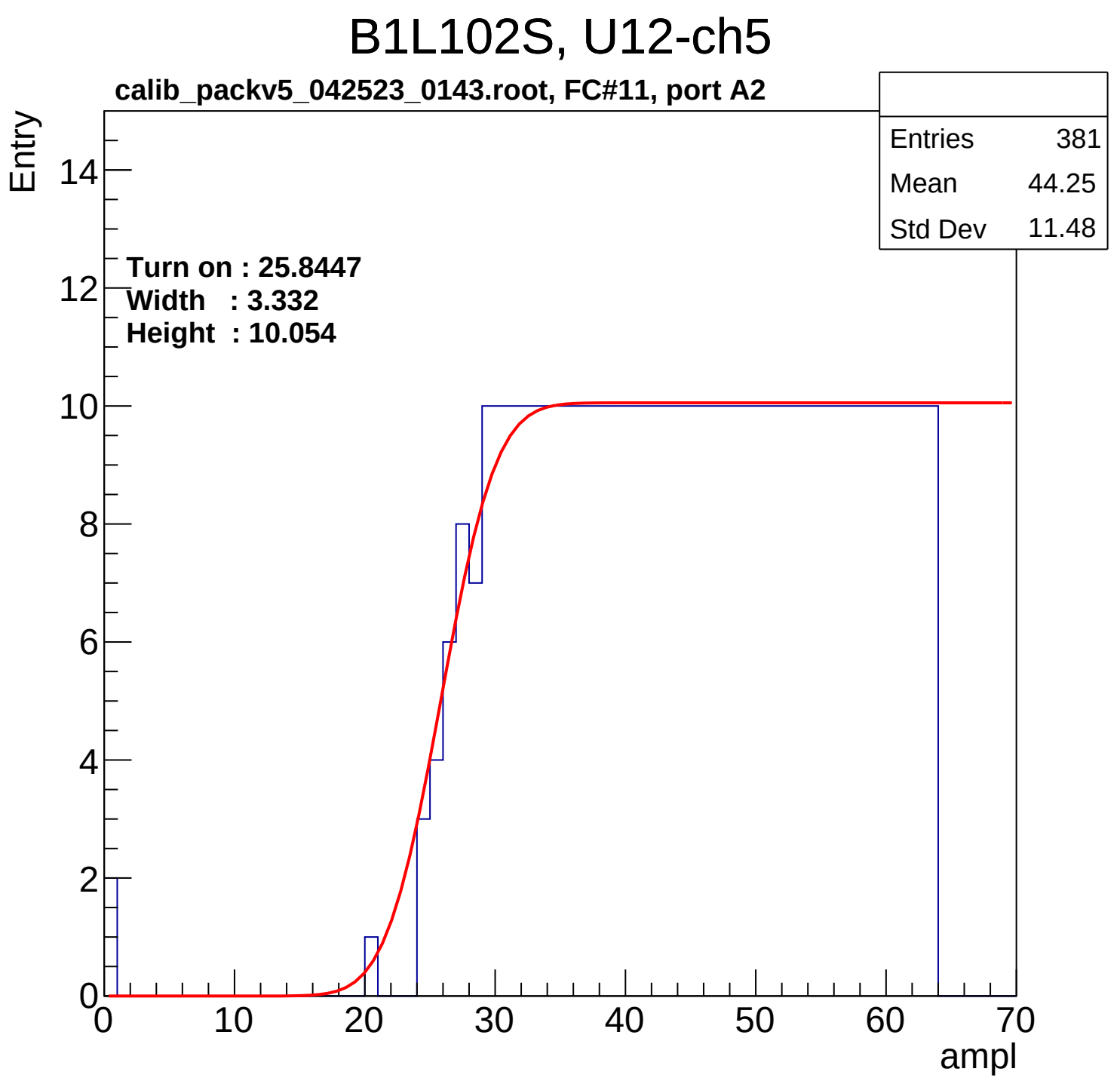
B1L102S, U12-ch5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.25
Std Dev 11.48
Turn on : 25.8447
Width : 3.332
Height : 10.054
Entry
ampl
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4
6
8
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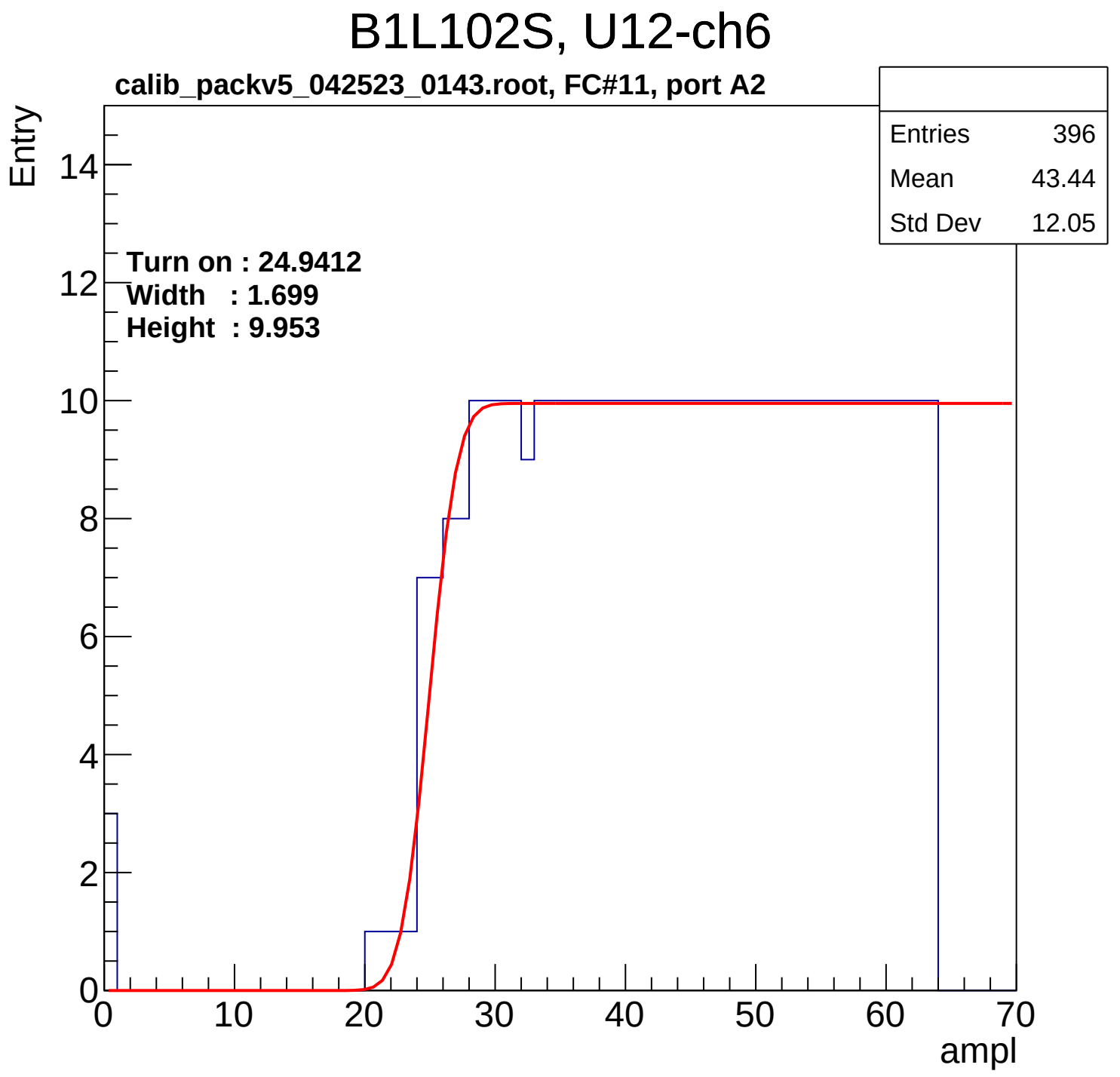
B1L102S, U12-ch6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.44
Std Dev 12.05
Turn on : 24.9412
Width : 1.699
Height : 9.953
Entry
ampl
0
2
4
6
8
10
12
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0
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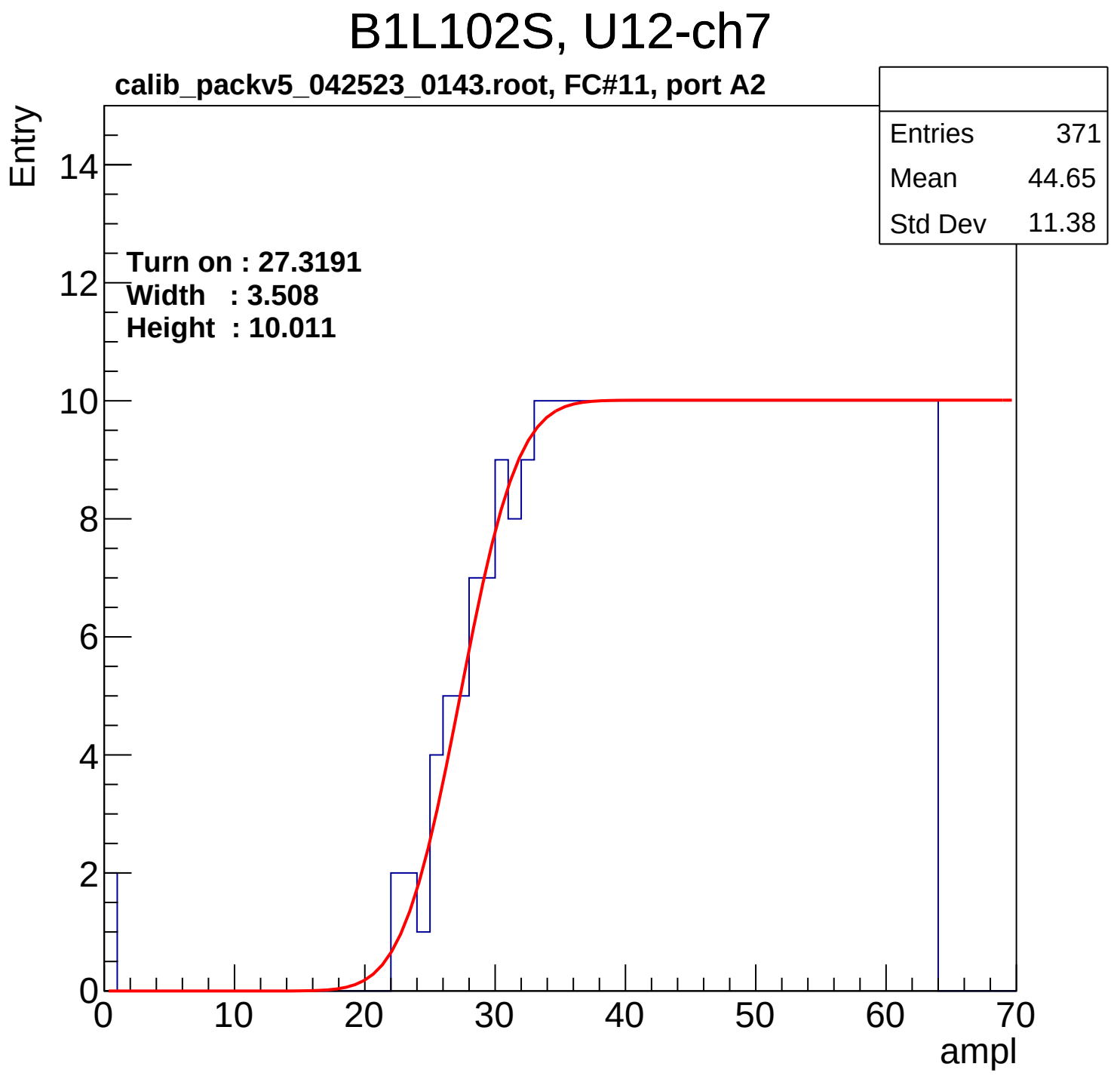
B1L102S, U12-ch7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 371
Mean 44.65
Std Dev 11.38
Turn on : 27.3191
Width : 3.508
Height : 10.011
Entry
ampl
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2
4
6
8
10
12
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0
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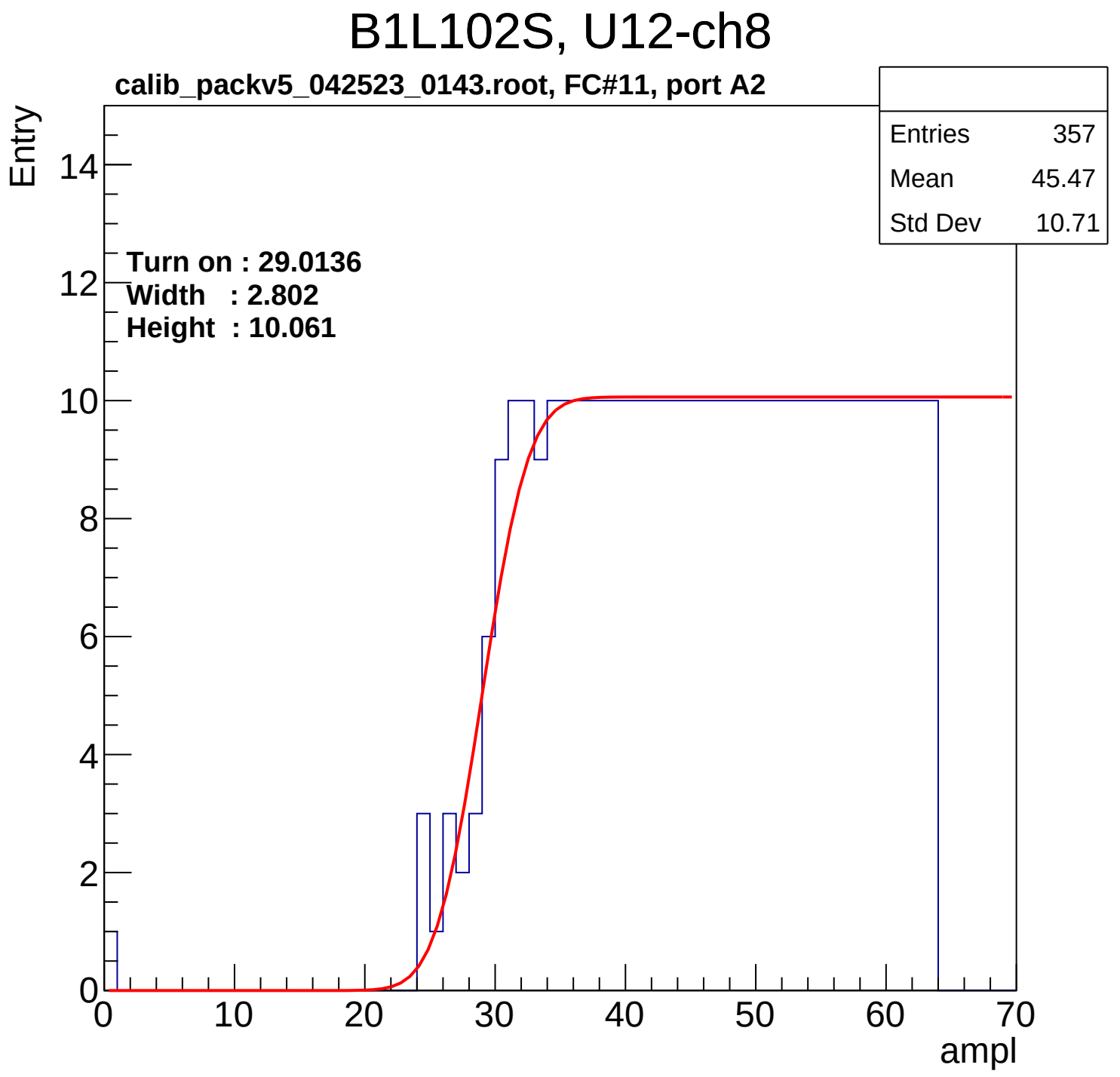
B1L102S, U12-ch8
calib_packv5_042523_0143.root, FC#11, port A2
Entries 357
Mean 45.47
Std Dev 10.71
Turn on : 29.0136
Width : 2.802
Height : 10.061
Entry
ampl
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2
4
6
8
10
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0
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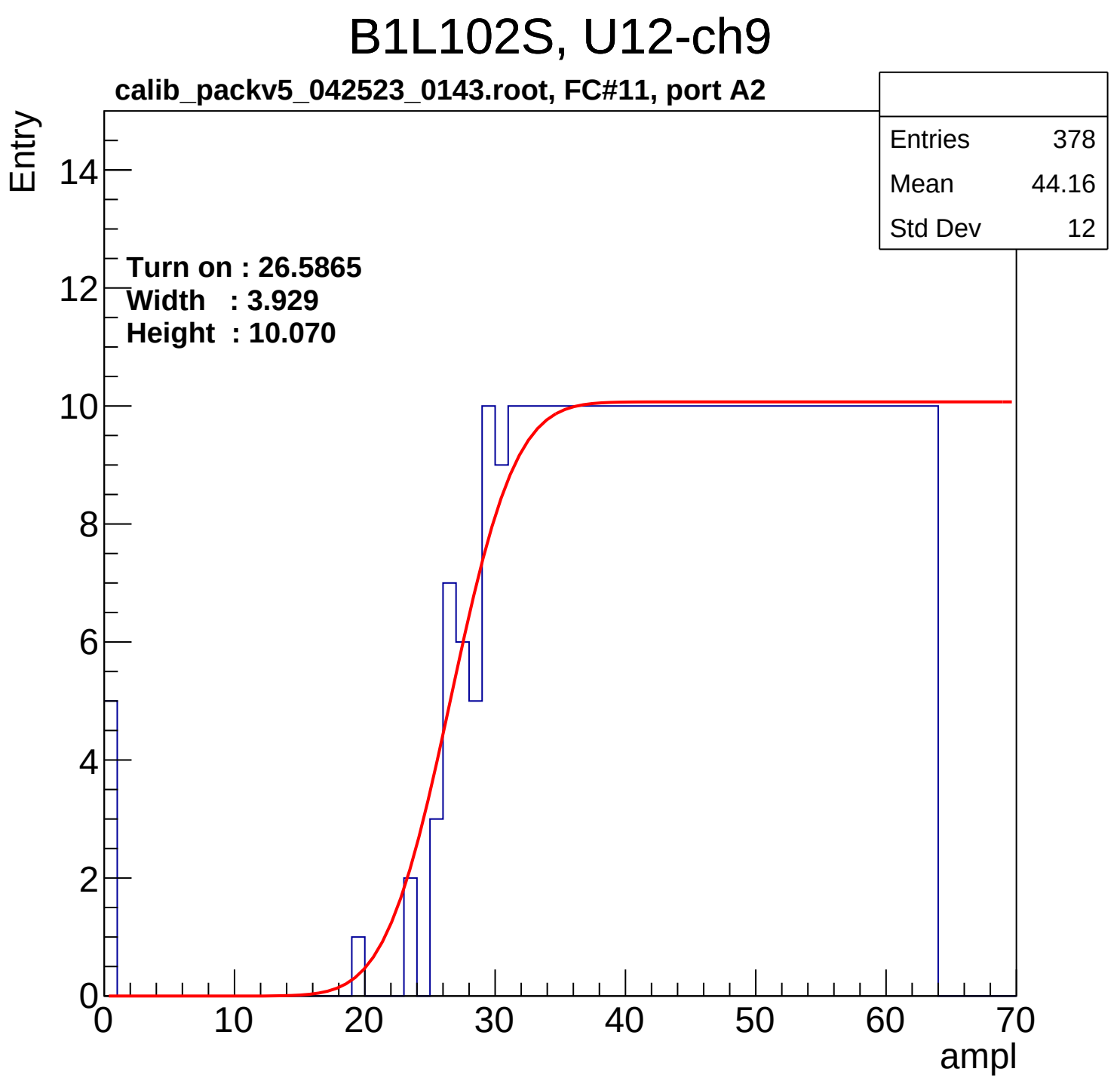
B1L102S, U12-ch9
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.16
Std Dev 12
Turn on : 26.5865
Width : 3.929
Height : 10.070
Entry
ampl
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2
4
6
8
10
12
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60
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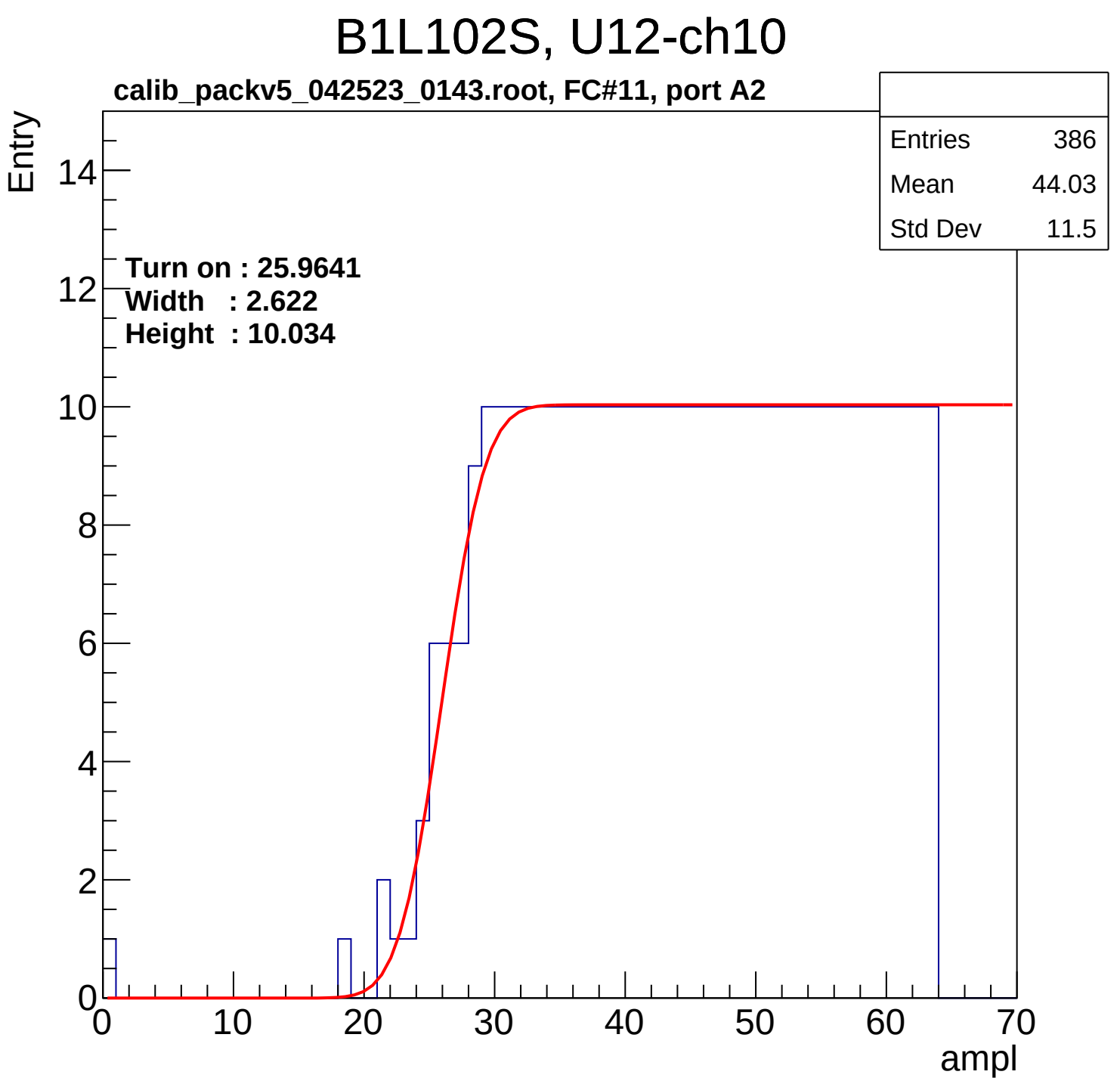
B1L102S, U12-ch10
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 44.03
Std Dev 11.5
Turn on : 25.9641
Width : 2.622
Height : 10.034
Entry
ampl
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4
6
8
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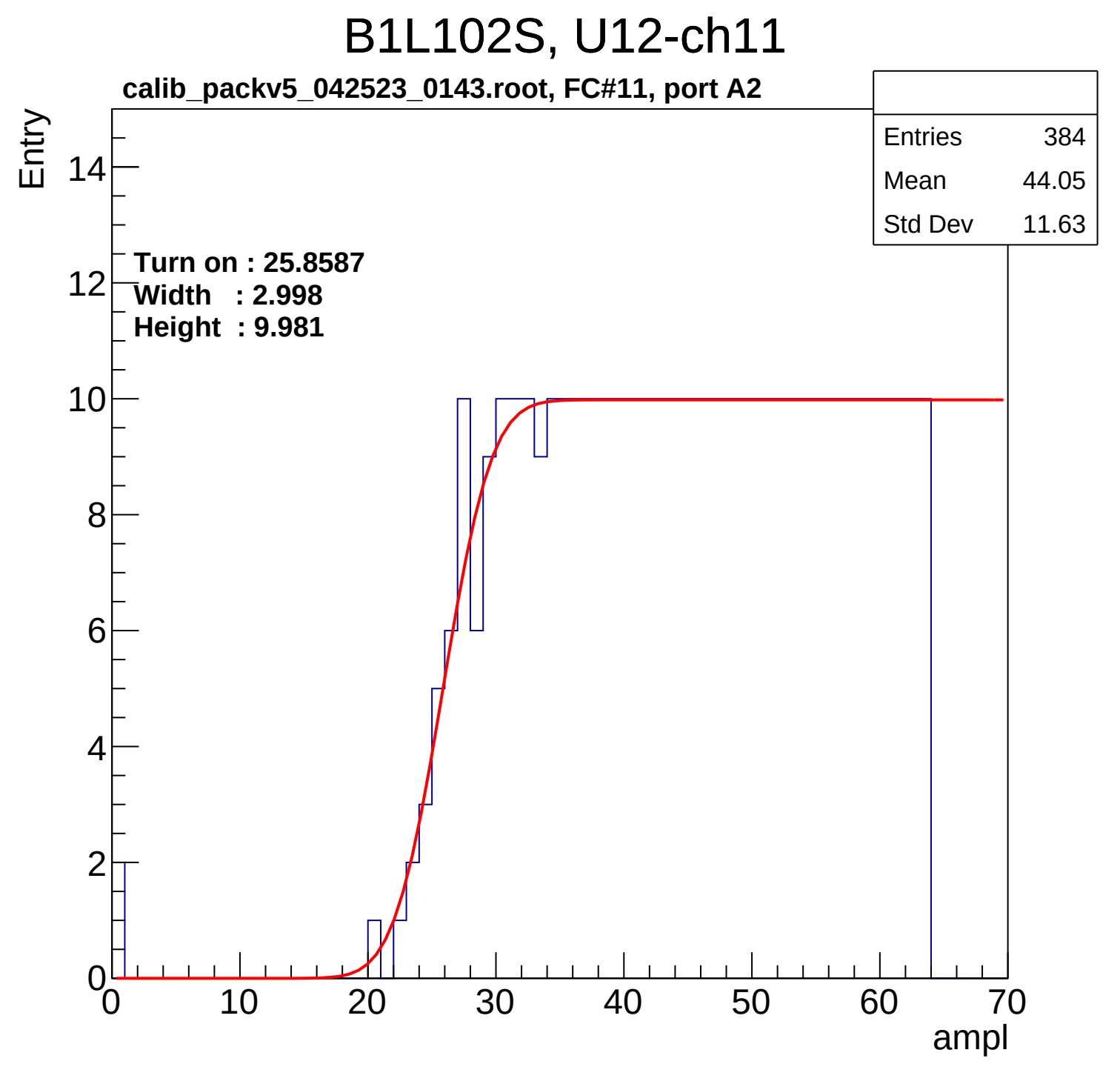
B1L102S, U12-ch11
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.05
Std Dev 11.63
Turn on : 25.8587
Width : 2.998
Height : 9.981
Entry
ampl
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6
8
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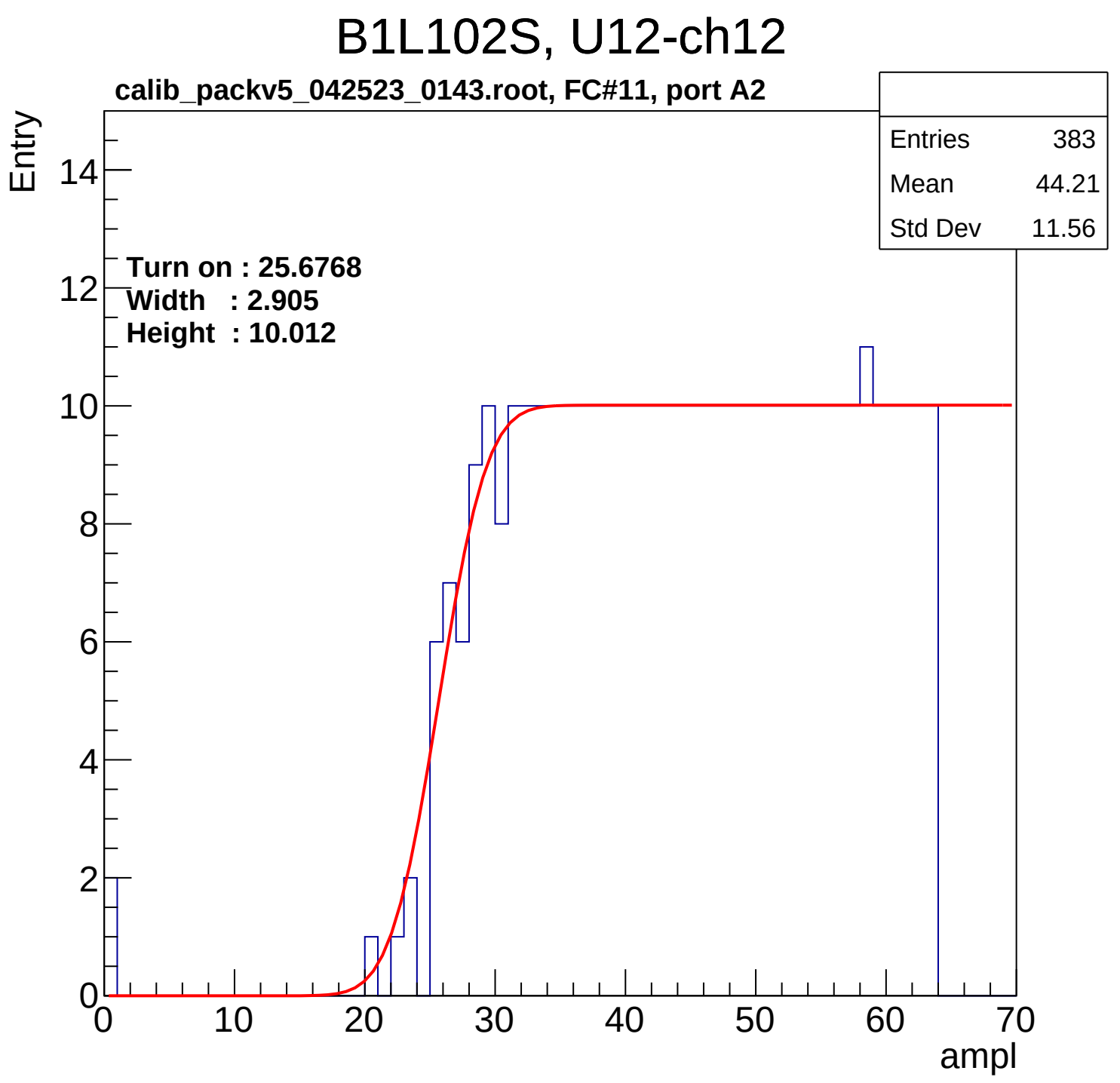
B1L102S, U12-ch12
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.21
Std Dev 11.56
Turn on : 25.6768
Width : 2.905
Height : 10.012
Entry
ampl
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2
4
6
8
10
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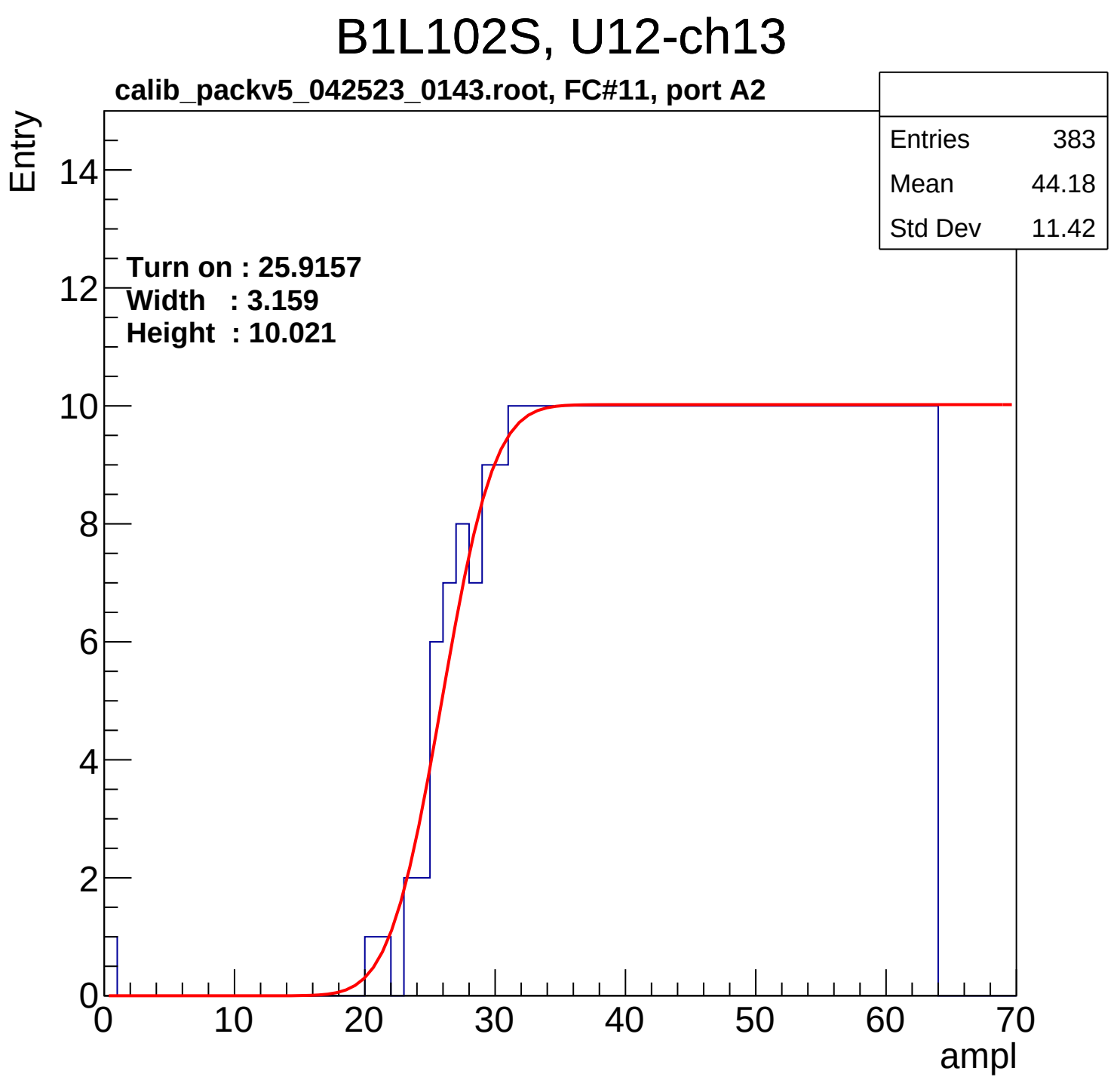
B1L102S, U12-ch13
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.18
Std Dev 11.42
Turn on : 25.9157
Width : 3.159
Height : 10.021
Entry
ampl
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4
6
8
10
12
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0
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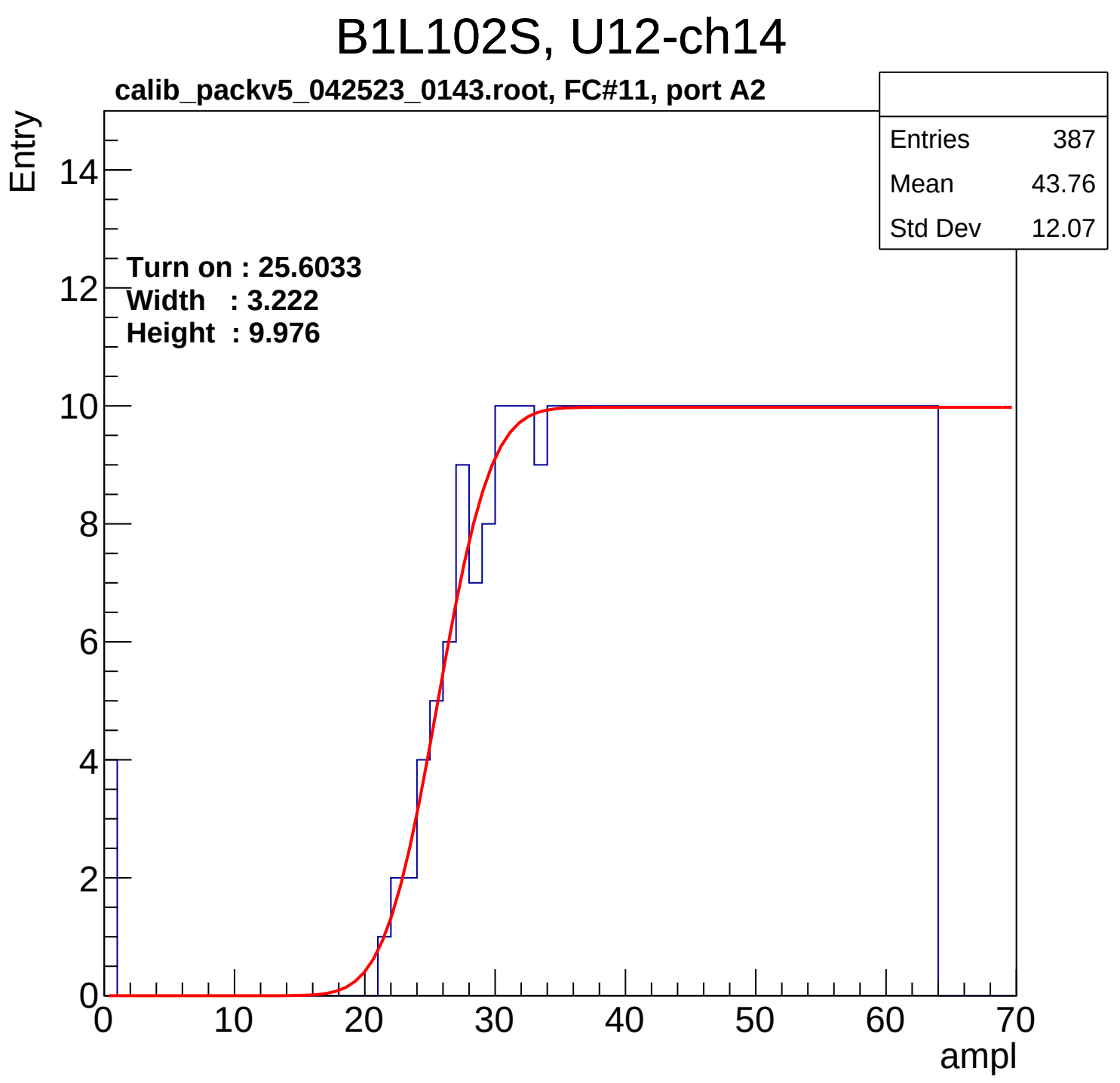
B1L102S, U12-ch14
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.76
Std Dev 12.07
Turn on : 25.6033
Width : 3.222
Height : 9.976
Entry
ampl
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6
8
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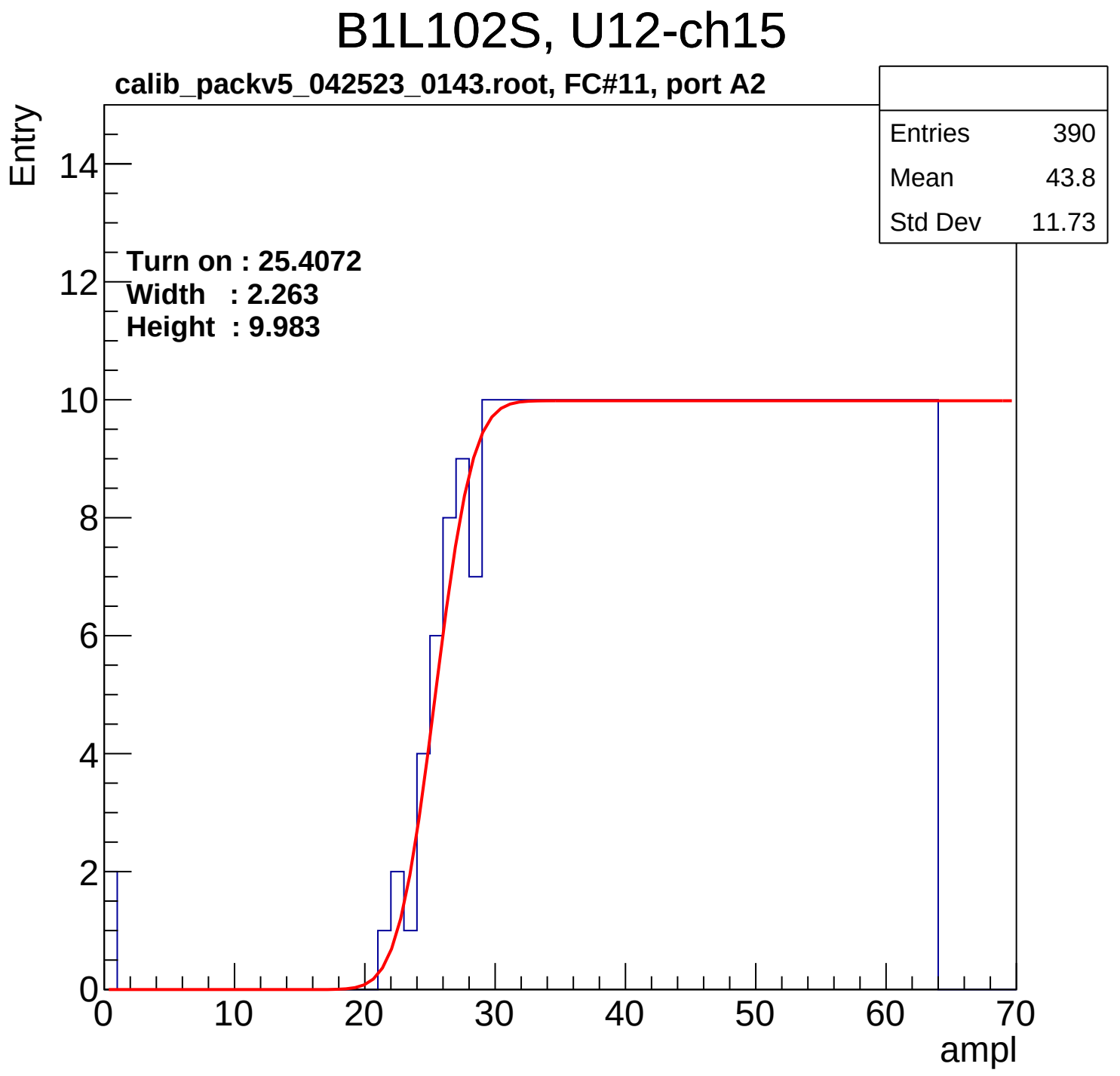
B1L102S, U12-ch15
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.8
Std Dev 11.73
Turn on : 25.4072
Width : 2.263
Height : 9.983
Entry
ampl
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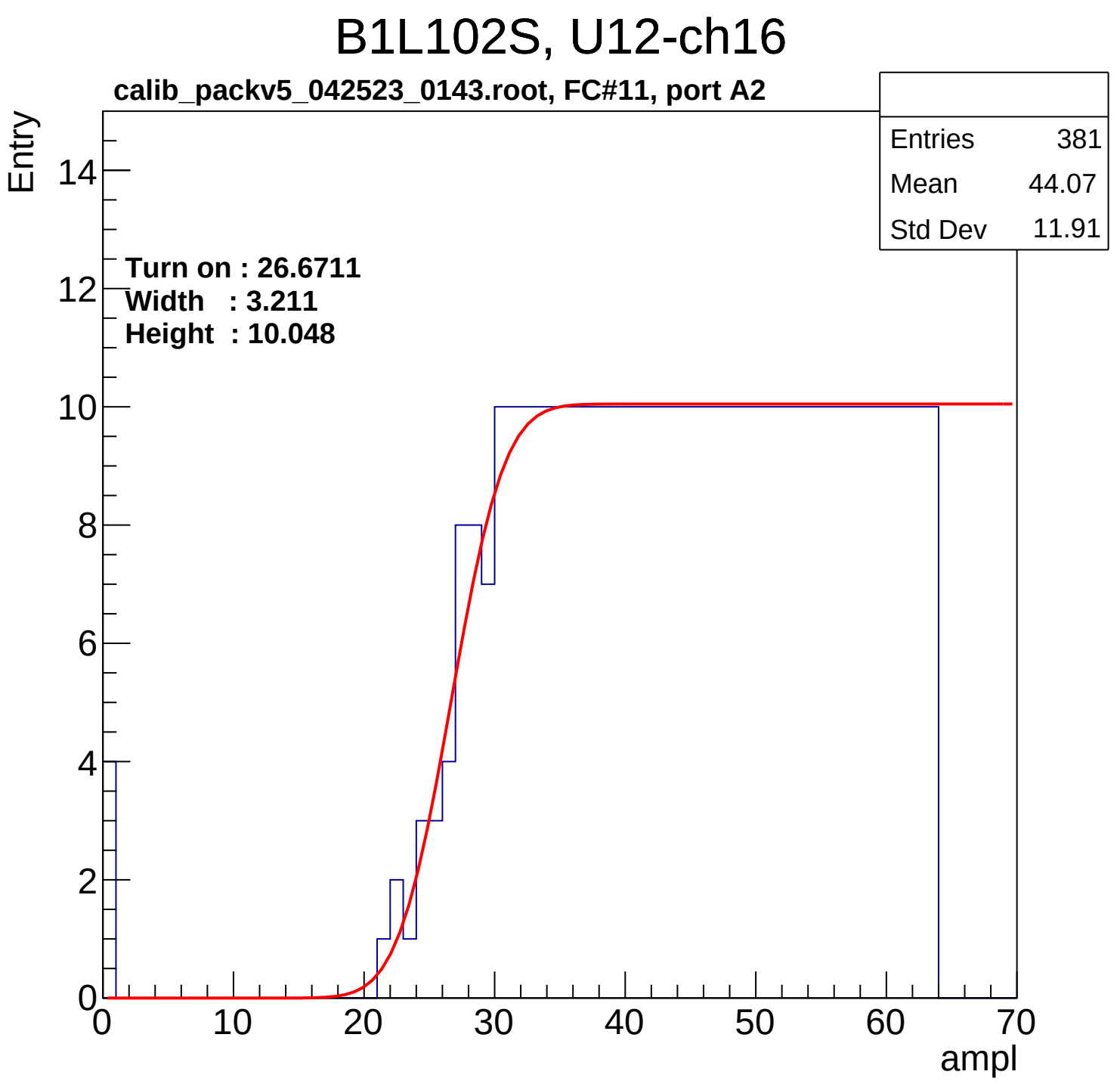
B1L102S, U12-ch16
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.07
Std Dev 11.91
Turn on : 26.6711
Width : 3.211
Height : 10.048
Entry
ampl
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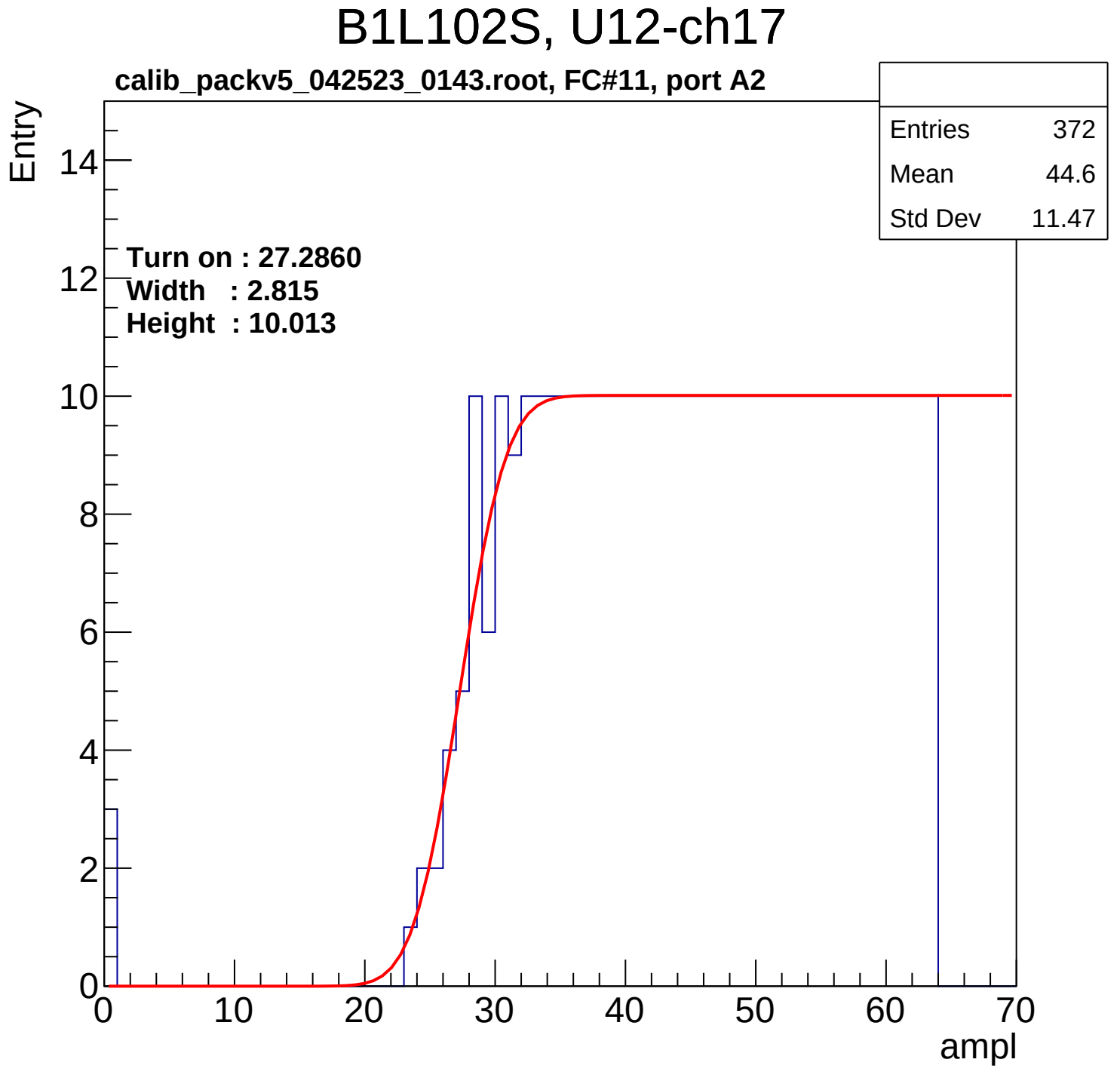
B1L102S, U12-ch17
calib_packv5_042523_0143.root, FC#11, port A2
Entries 372
Mean 44.6
Std Dev 11.47
Turn on : 27.2860
Width : 2.815
Height : 10.013
Entry
ampl
0
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8
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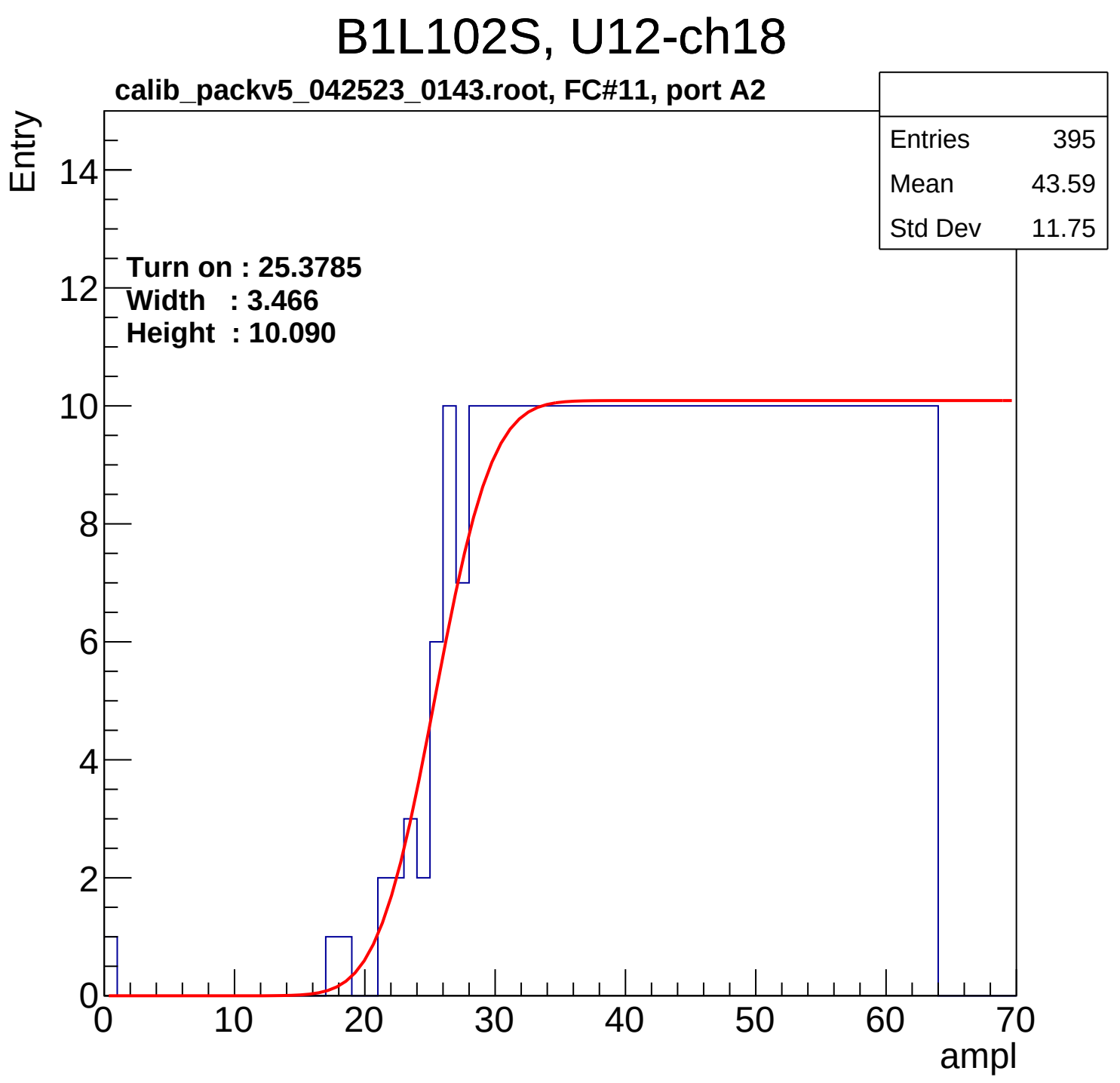
B1L102S, U12-ch18
calib_packv5_042523_0143.root, FC#11, port A2
Entries 395
Mean 43.59
Std Dev 11.75
Turn on : 25.3785
Width : 3.466
Height : 10.090
Entry
ampl
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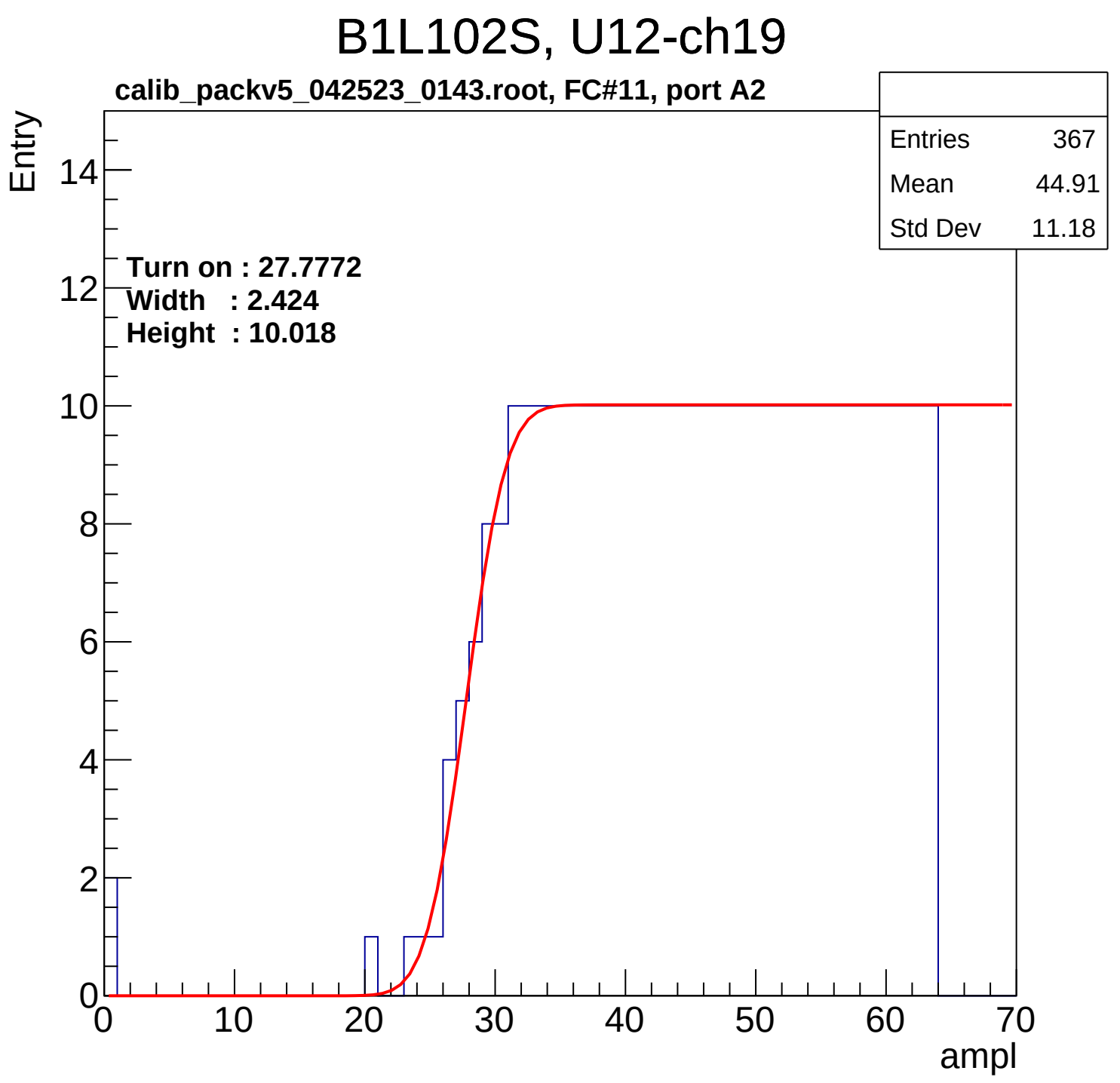
B1L102S, U12-ch19
calib_packv5_042523_0143.root, FC#11, port A2
Entries 367
Mean 44.91
Std Dev 11.18
Turn on : 27.7772
Width : 2.424
Height : 10.018
Entry
ampl
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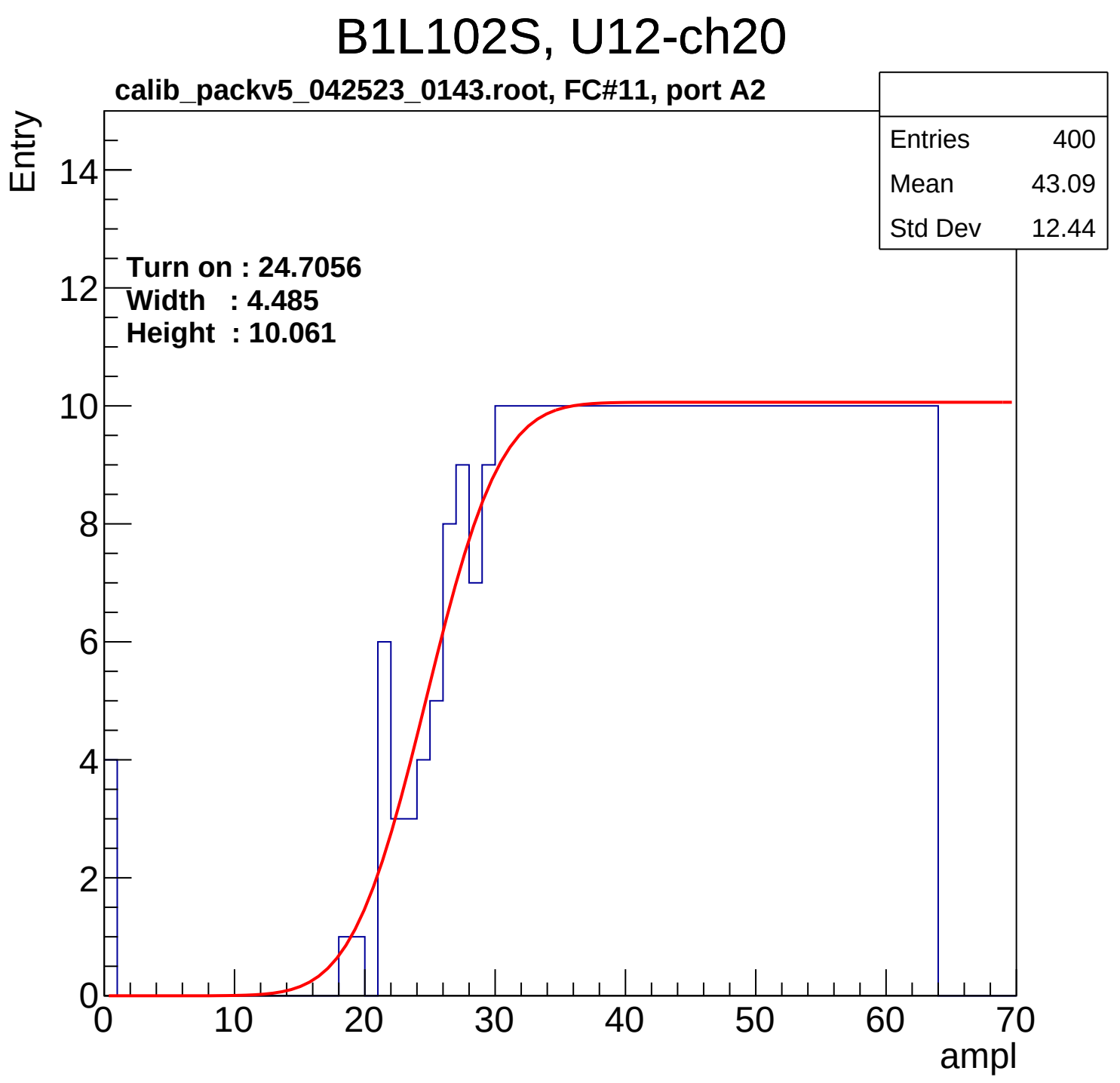
B1L102S, U12-ch20
calib_packv5_042523_0143.root, FC#11, port A2
Entries 400
Mean 43.09
Std Dev 12.44
Turn on : 24.7056
Width : 4.485
Height : 10.061
Entry
ampl
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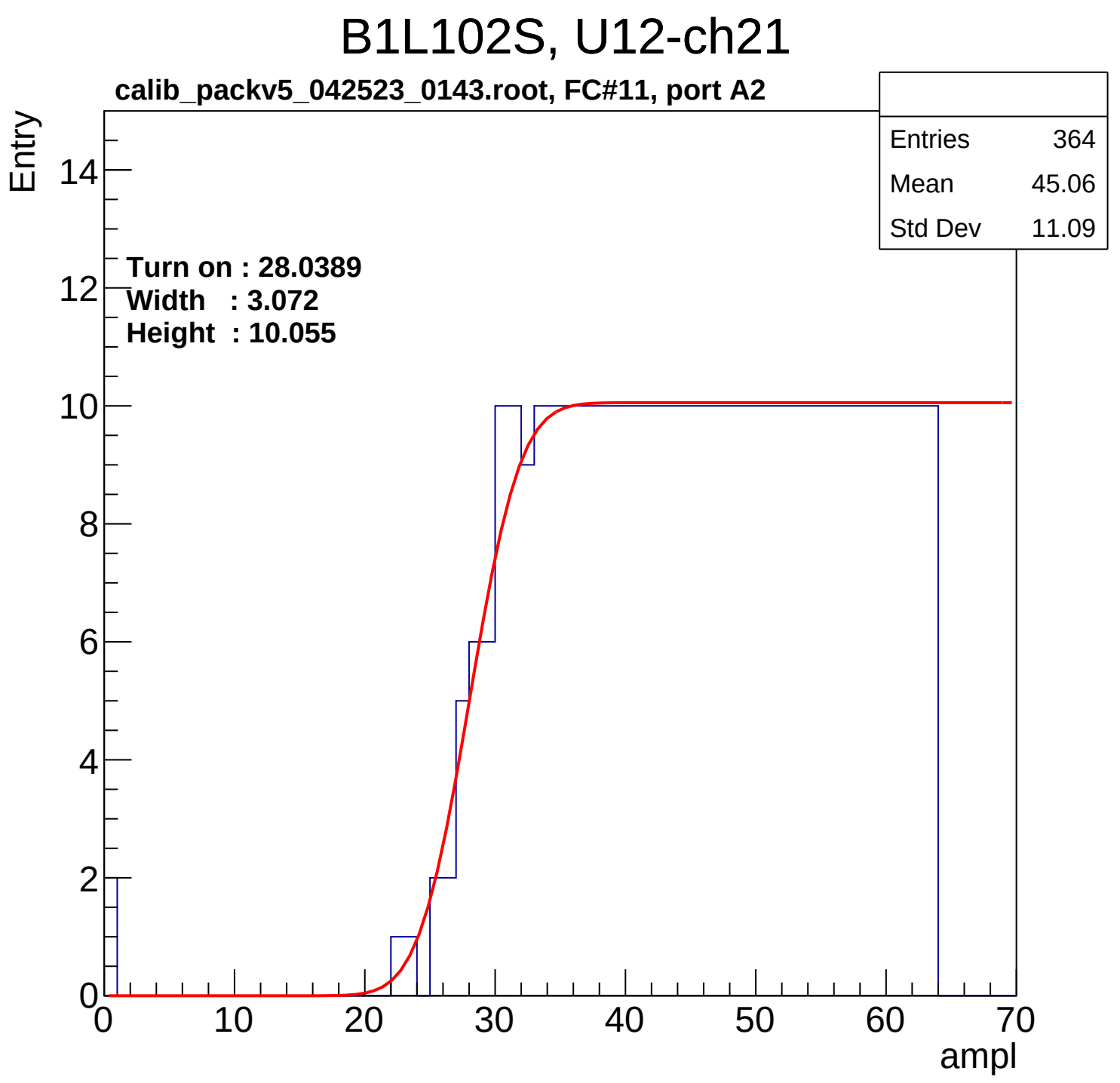
B1L102S, U12-ch21
calib_packv5_042523_0143.root, FC#11, port A2
Entries 364
Mean 45.06
Std Dev 11.09
Turn on : 28.0389
Width : 3.072
Height : 10.055
Entry
ampl
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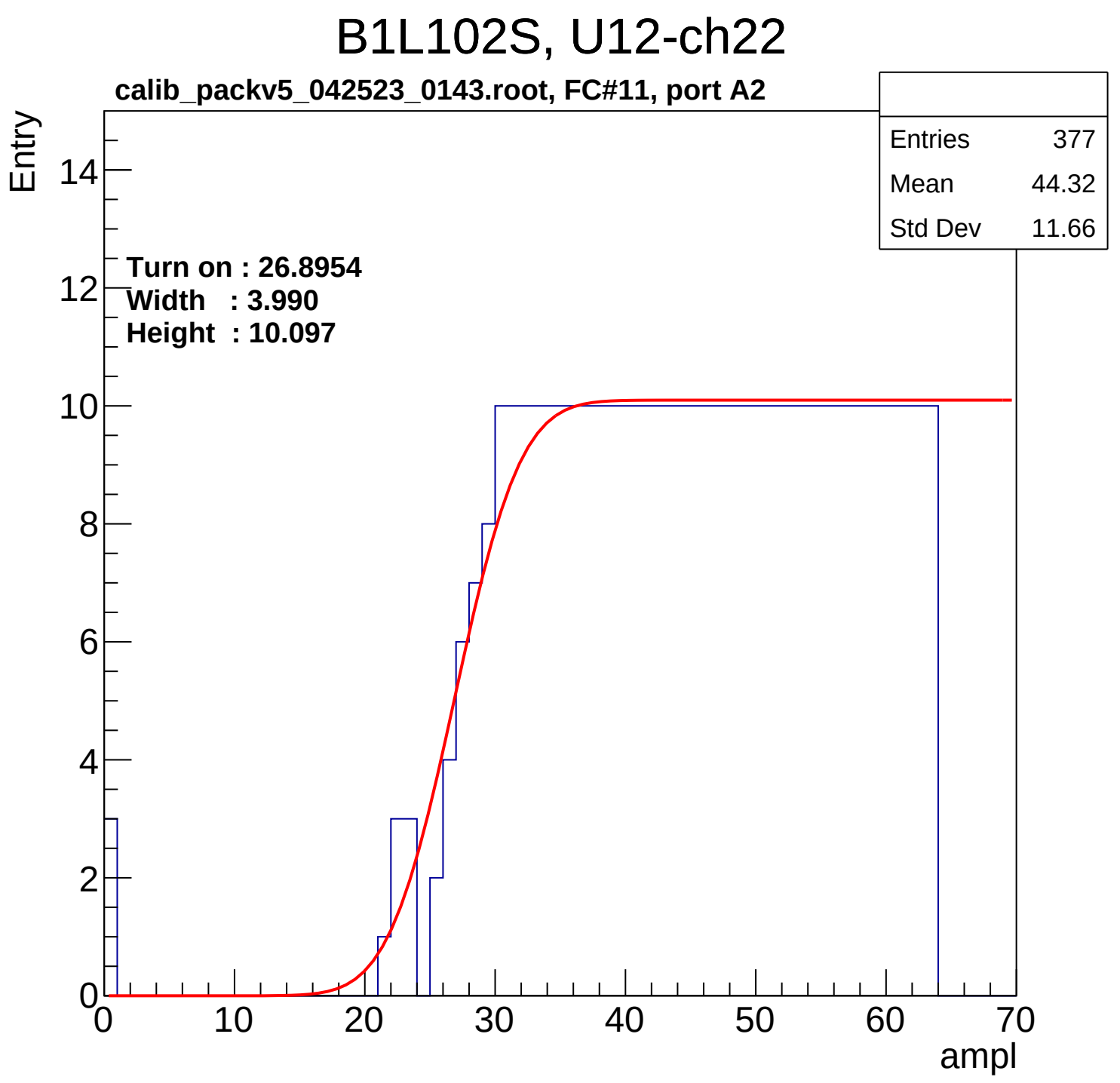
B1L102S, U12-ch22
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.32
Std Dev 11.66
Turn on : 26.8954
Width : 3.990
Height : 10.097
Entry
ampl
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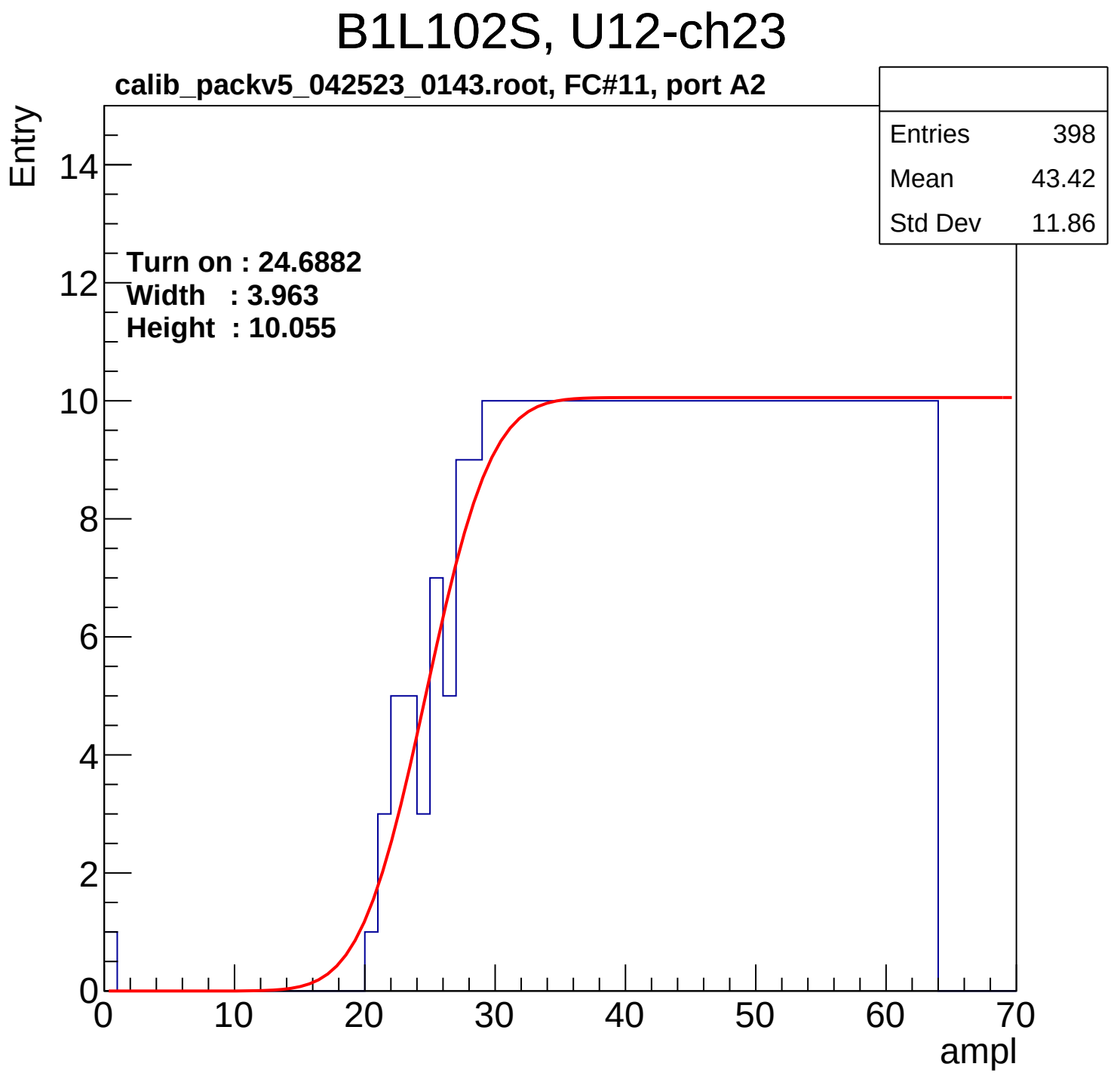
B1L102S, U12-ch23
calib_packv5_042523_0143.root, FC#11, port A2
Entries 398
Mean 43.42
Std Dev 11.86
Turn on : 24.6882
Width : 3.963
Height : 10.055
Entry
ampl
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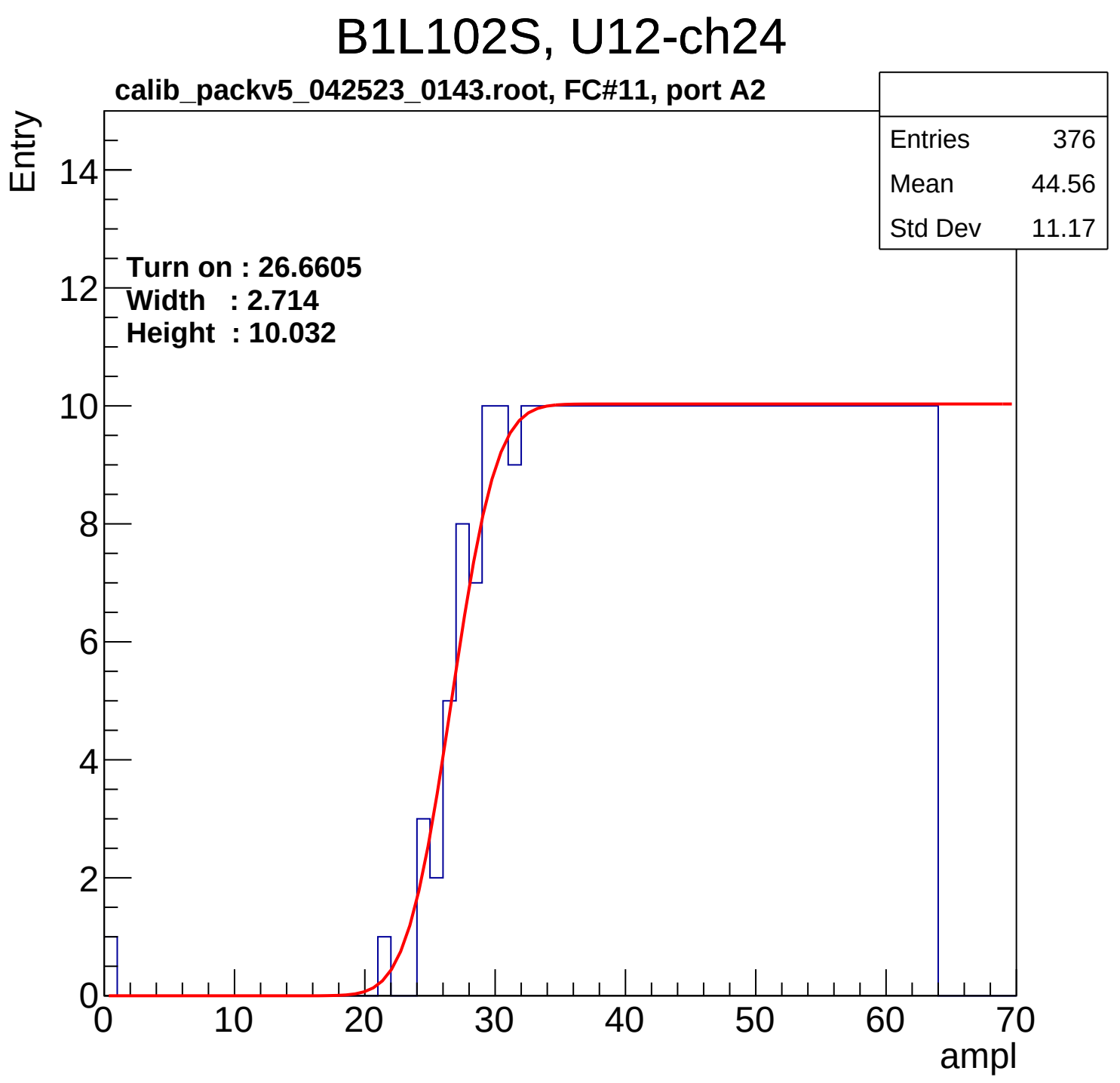
B1L102S, U12-ch24
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.56
Std Dev 11.17
Turn on : 26.6605
Width : 2.714
Height : 10.032
Entry
ampl
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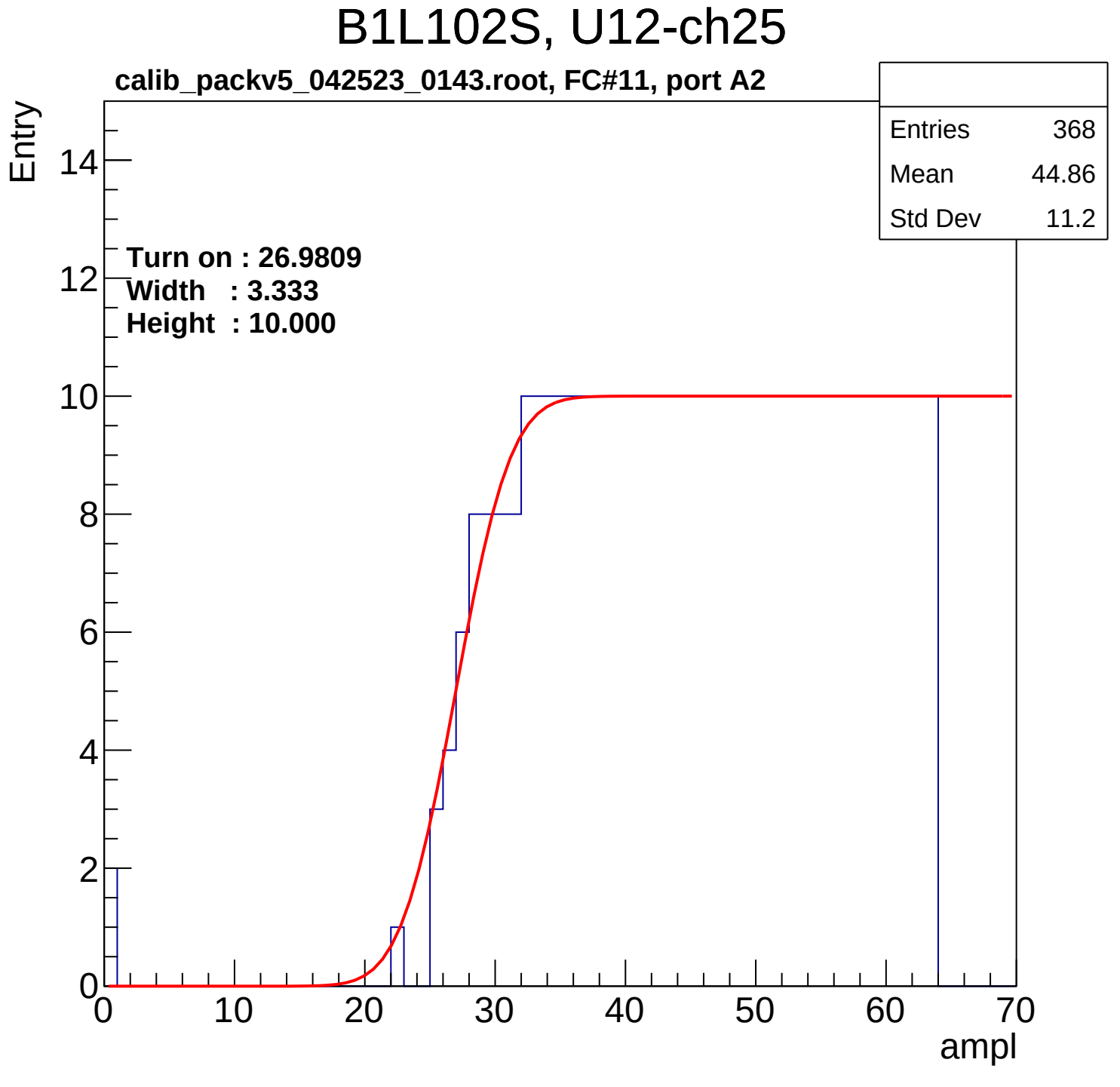
B1L102S, U12-ch25
calib_packv5_042523_0143.root, FC#11, port A2
Entries 368
Mean 44.86
Std Dev 11.2
Turn on : 26.9809
Width : 3.333
Height : 10.000
Entry
ampl
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6
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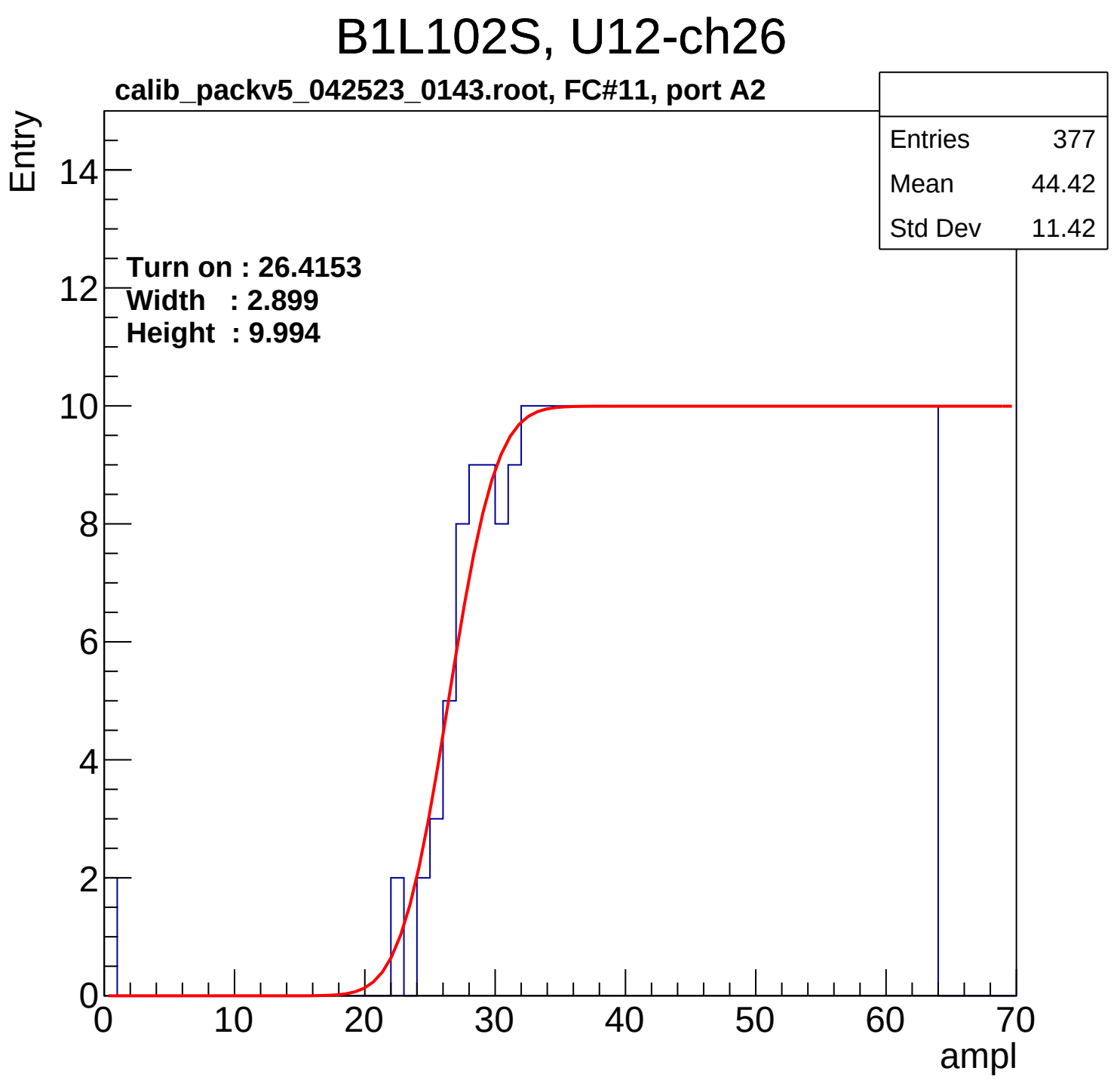
B1L102S, U12-ch26
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.42
Std Dev 11.42
Turn on : 26.4153
Width : 2.899
Height : 9.994
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ampl
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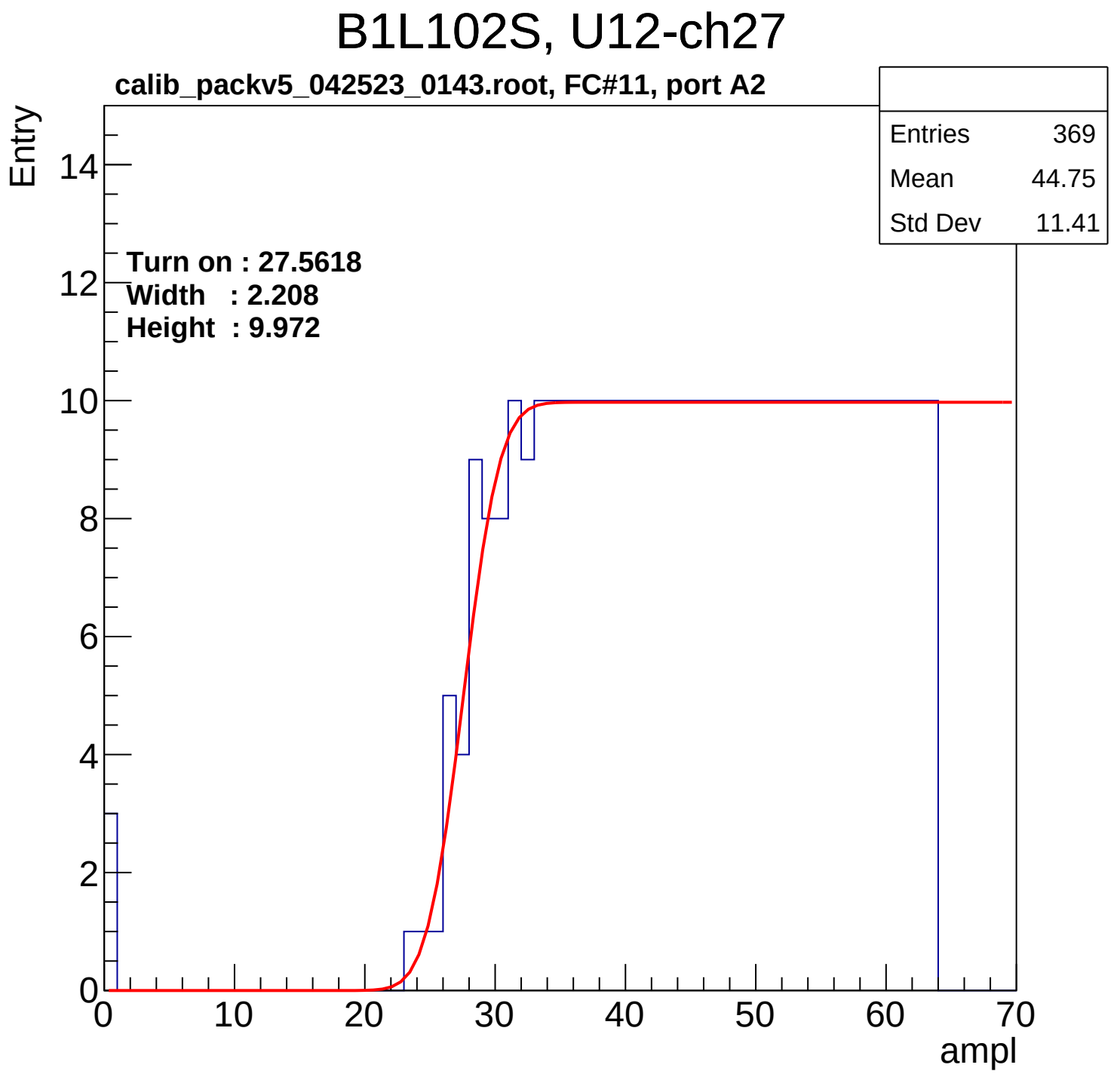
B1L102S, U12-ch27
calib_packv5_042523_0143.root, FC#11, port A2
Entries 369
Mean 44.75
Std Dev 11.41
Turn on : 27.5618
Width : 2.208
Height : 9.972
Entry
ampl
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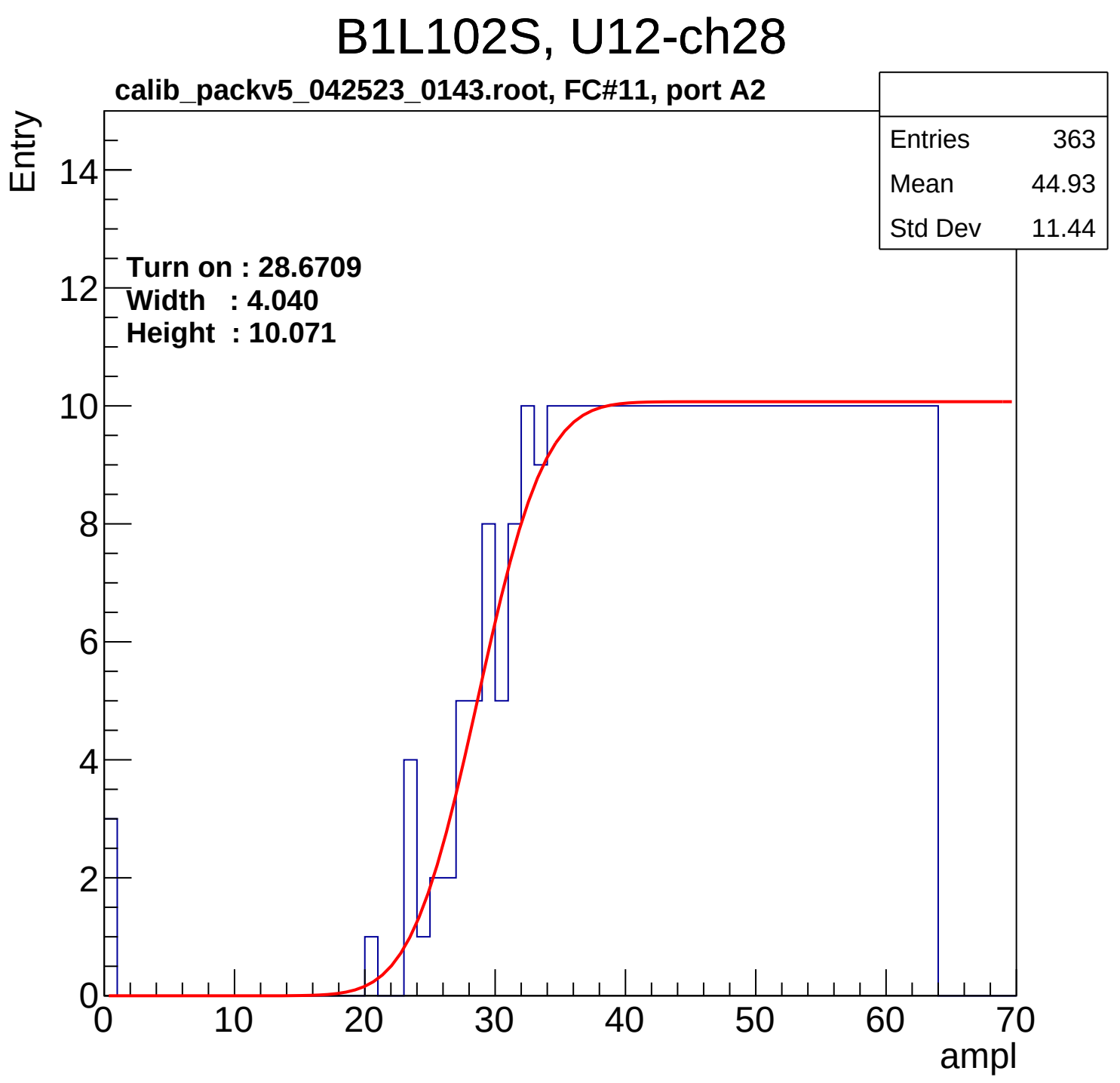
B1L102S, U12-ch28
calib_packv5_042523_0143.root, FC#11, port A2
Entries 363
Mean 44.93
Std Dev 11.44
Turn on : 28.6709
Width : 4.040
Height : 10.071
Entry
ampl
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4
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20
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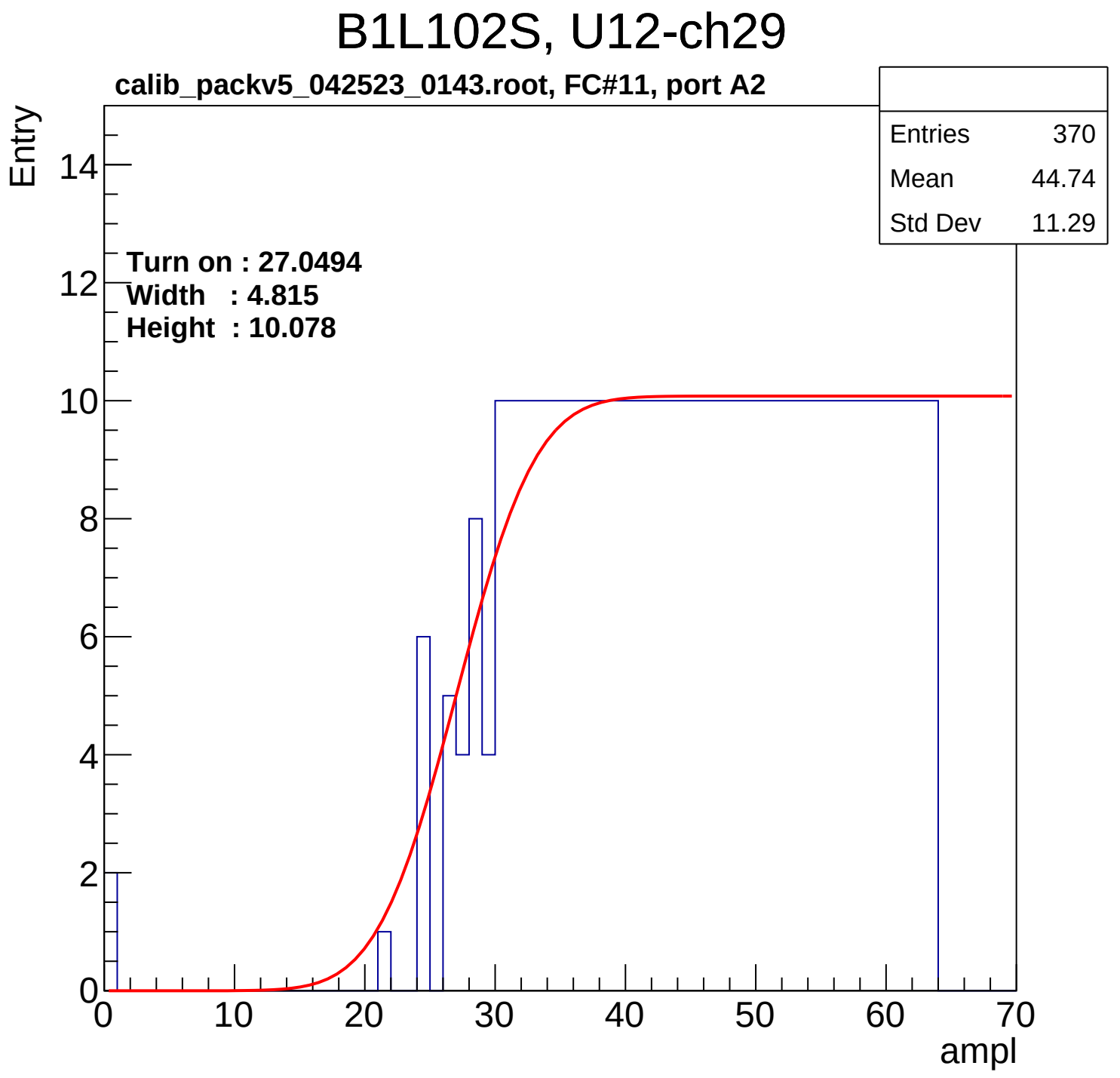
B1L102S, U12-ch29
calib_packv5_042523_0143.root, FC#11, port A2
Entries 370
Mean 44.74
Std Dev 11.29
Turn on : 27.0494
Width : 4.815
Height : 10.078
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ampl
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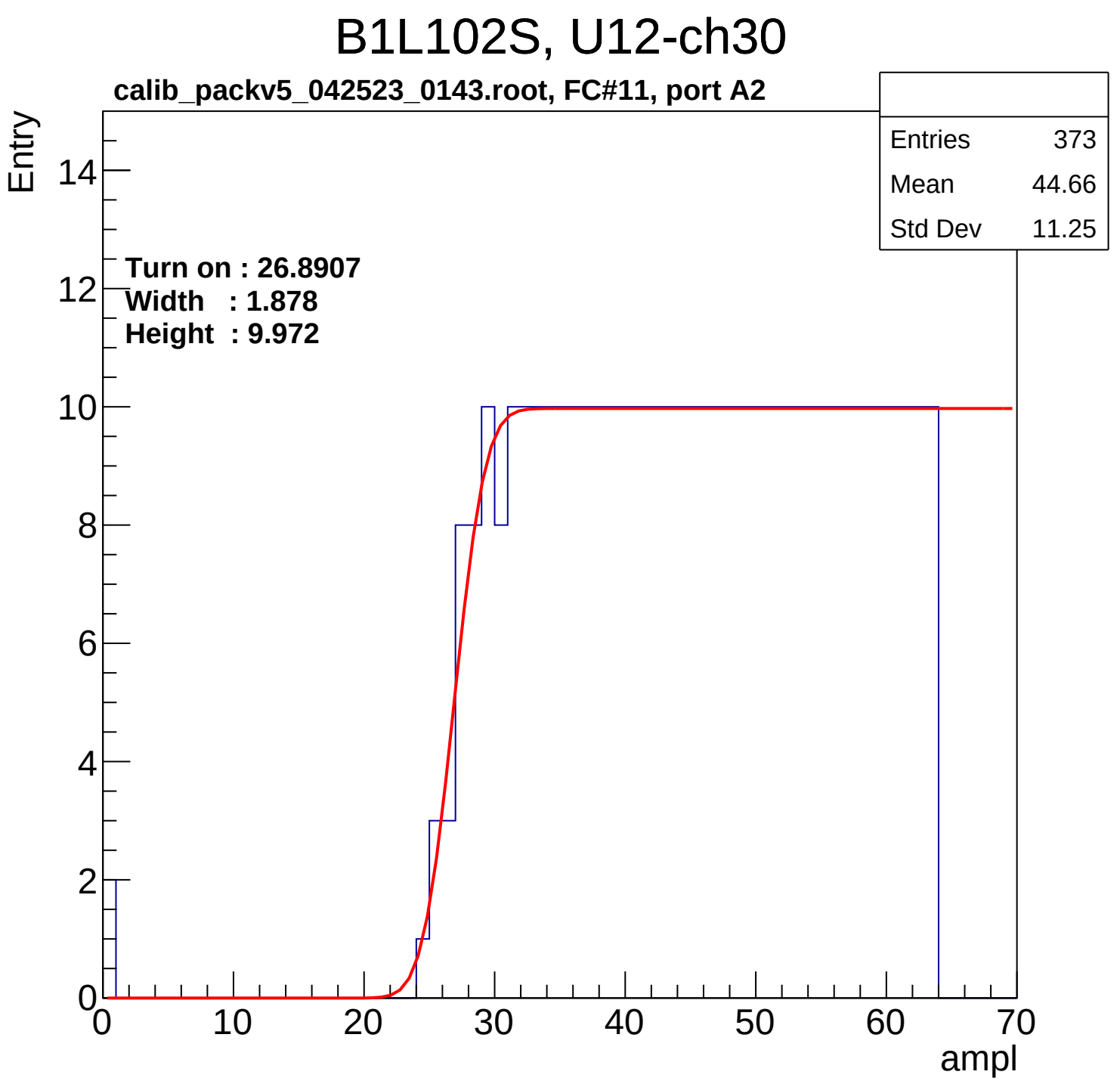
B1L102S, U12-ch30
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.66
Std Dev 11.25
Turn on : 26.8907
Width : 1.878
Height : 9.972
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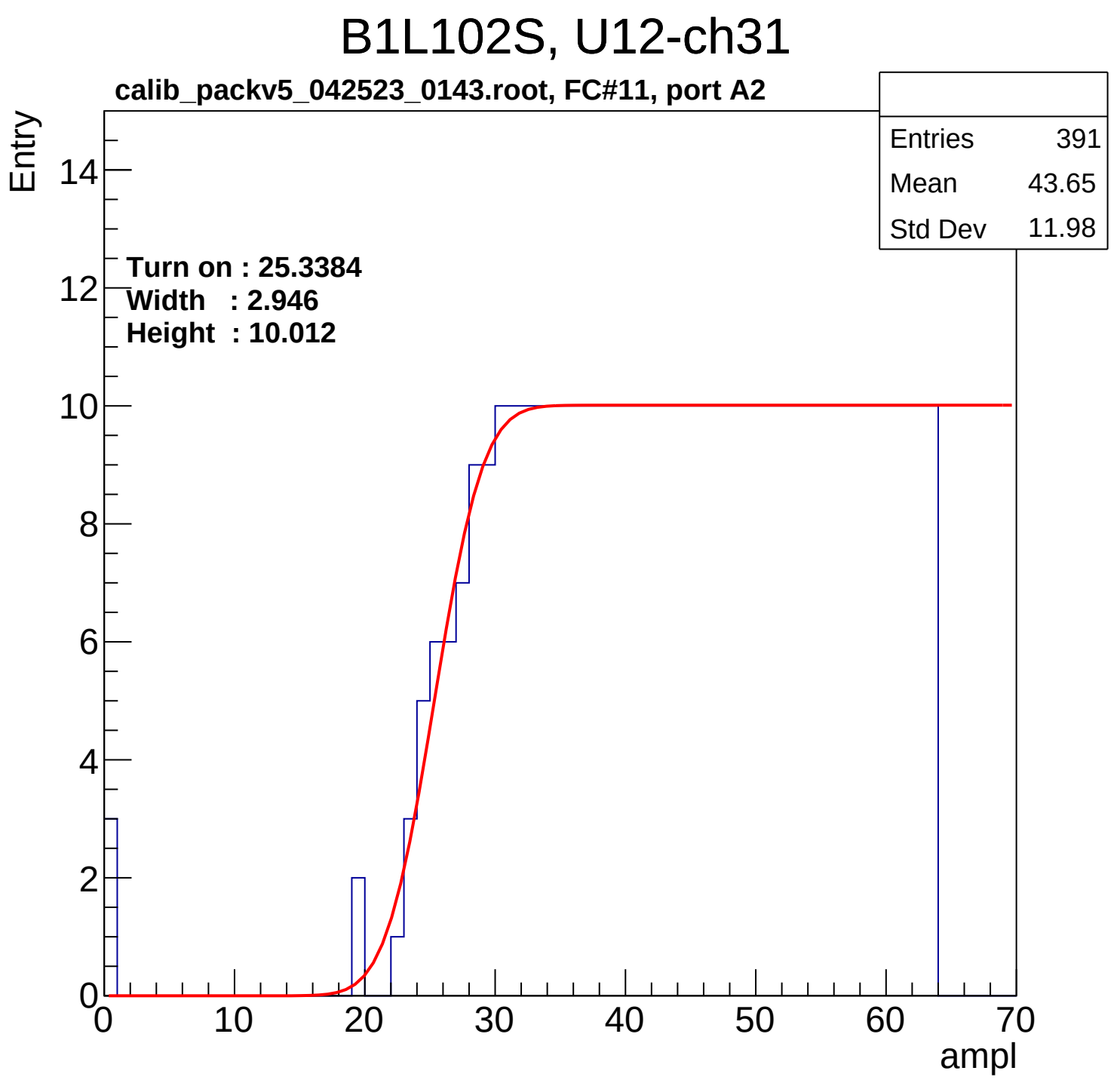
B1L102S, U12-ch31
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.65
Std Dev 11.98
Turn on : 25.3384
Width : 2.946
Height : 10.012
Entry
ampl
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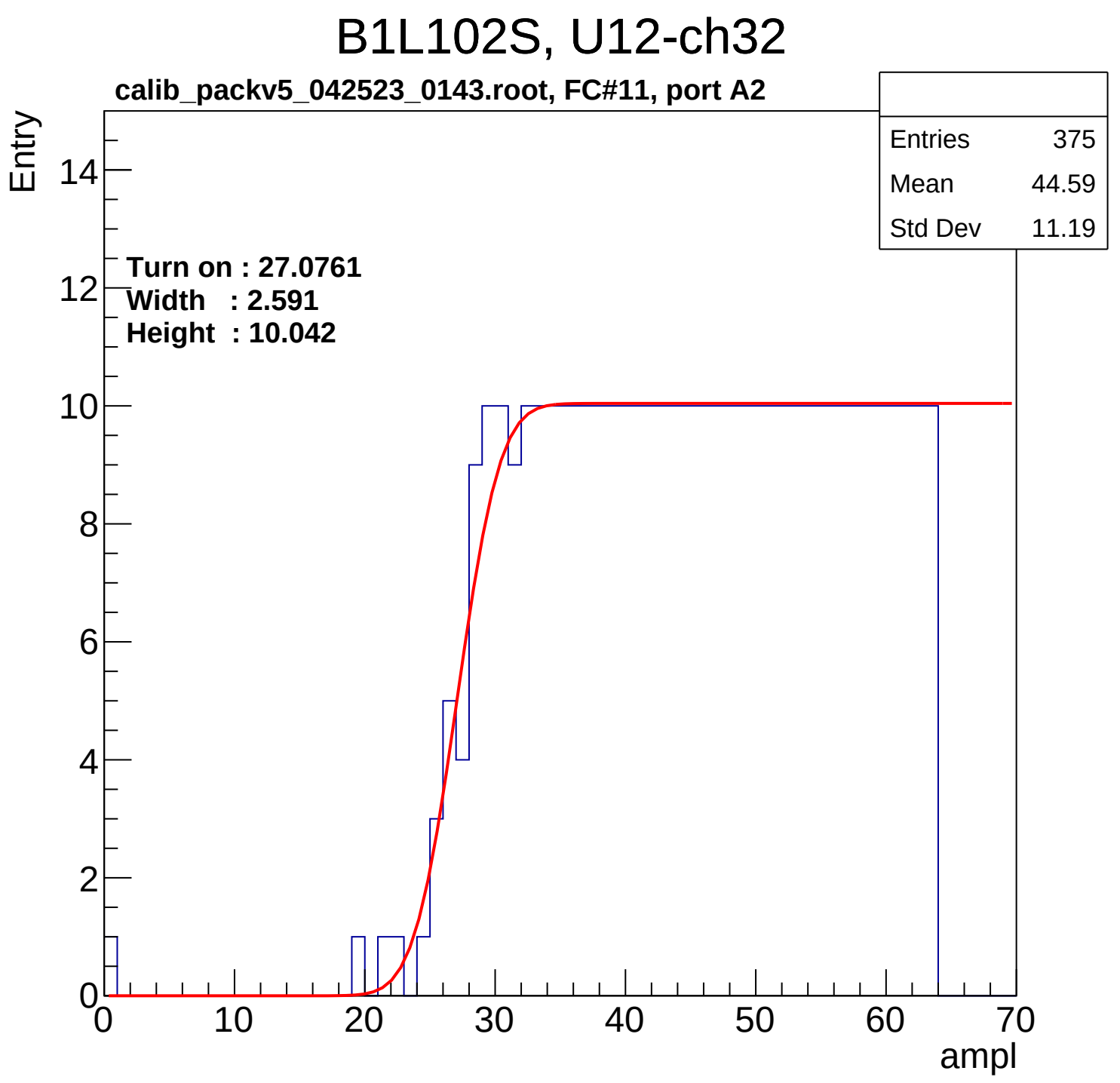
B1L102S, U12-ch32
calib_packv5_042523_0143.root, FC#11, port A2
Entries 375
Mean 44.59
Std Dev 11.19
Turn on : 27.0761
Width : 2.591
Height : 10.042
Entry
ampl
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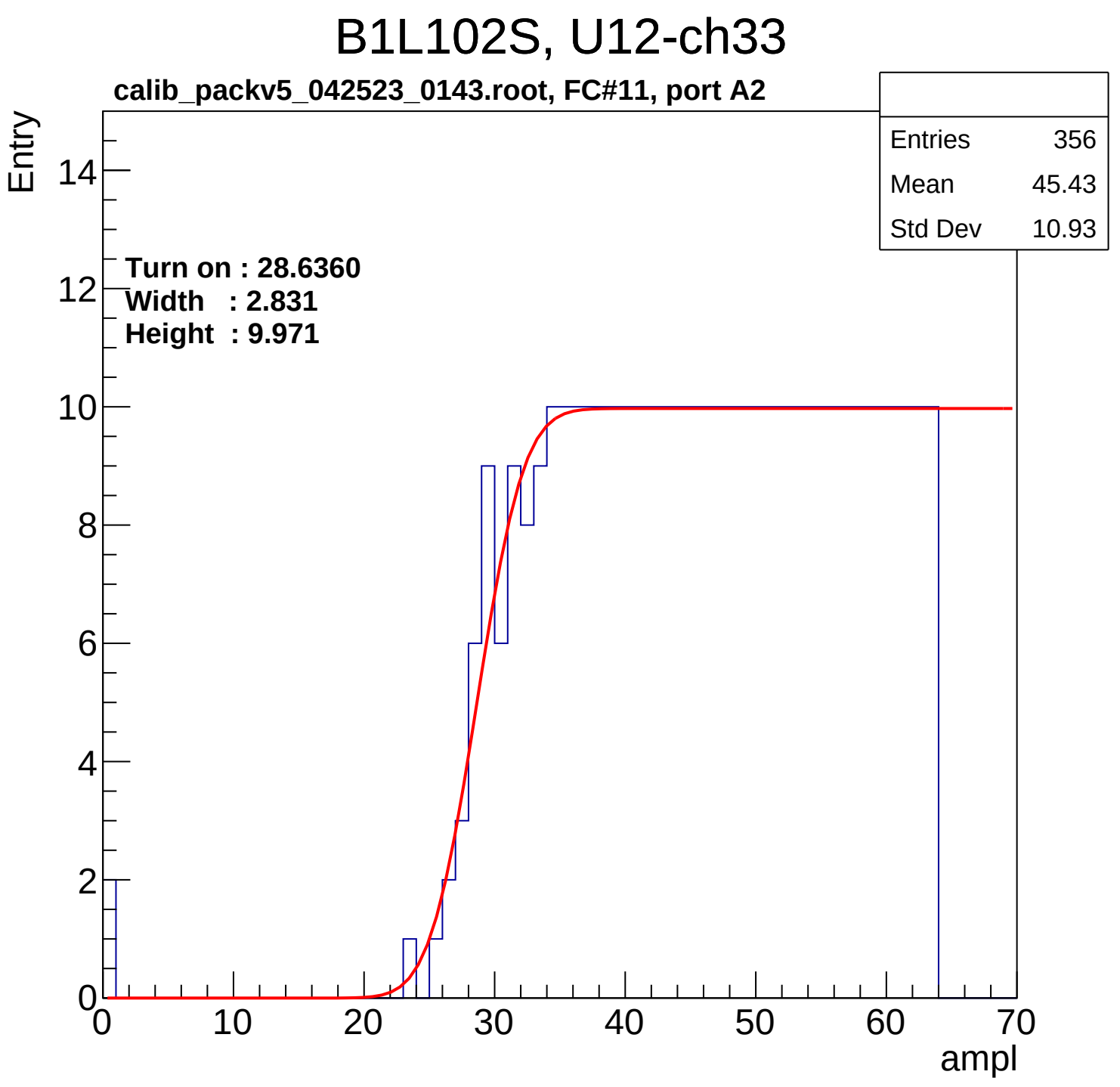
B1L102S, U12-ch33
calib_packv5_042523_0143.root, FC#11, port A2
Entries 356
Mean 45.43
Std Dev 10.93
Turn on : 28.6360
Width : 2.831
Height : 9.971
Entry
ampl
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2
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8
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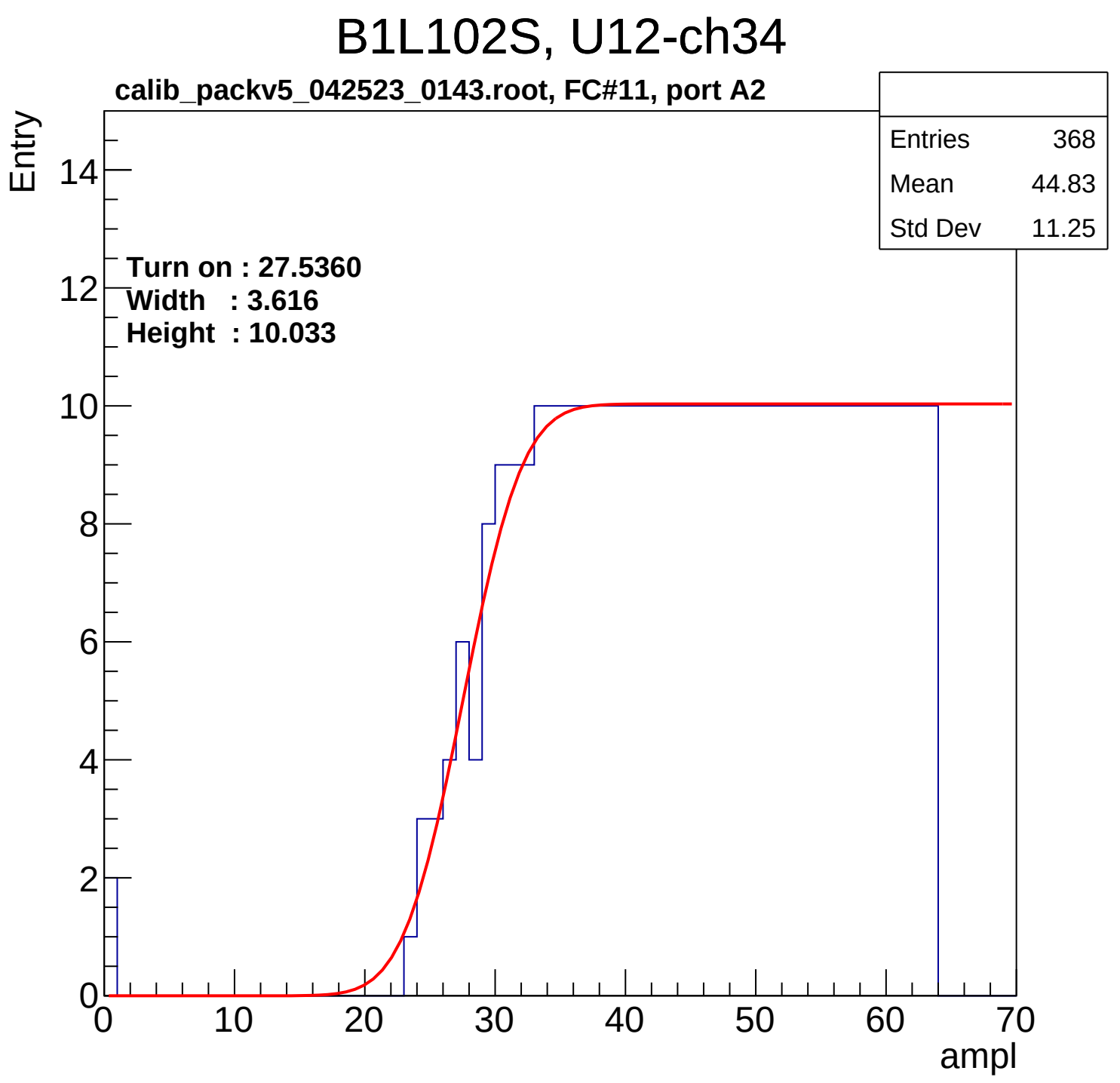
B1L102S, U12-ch34
calib_packv5_042523_0143.root, FC#11, port A2
Entries 368
Mean 44.83
Std Dev 11.25
Turn on : 27.5360
Width : 3.616
Height : 10.033
Entry
ampl
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4
6
8
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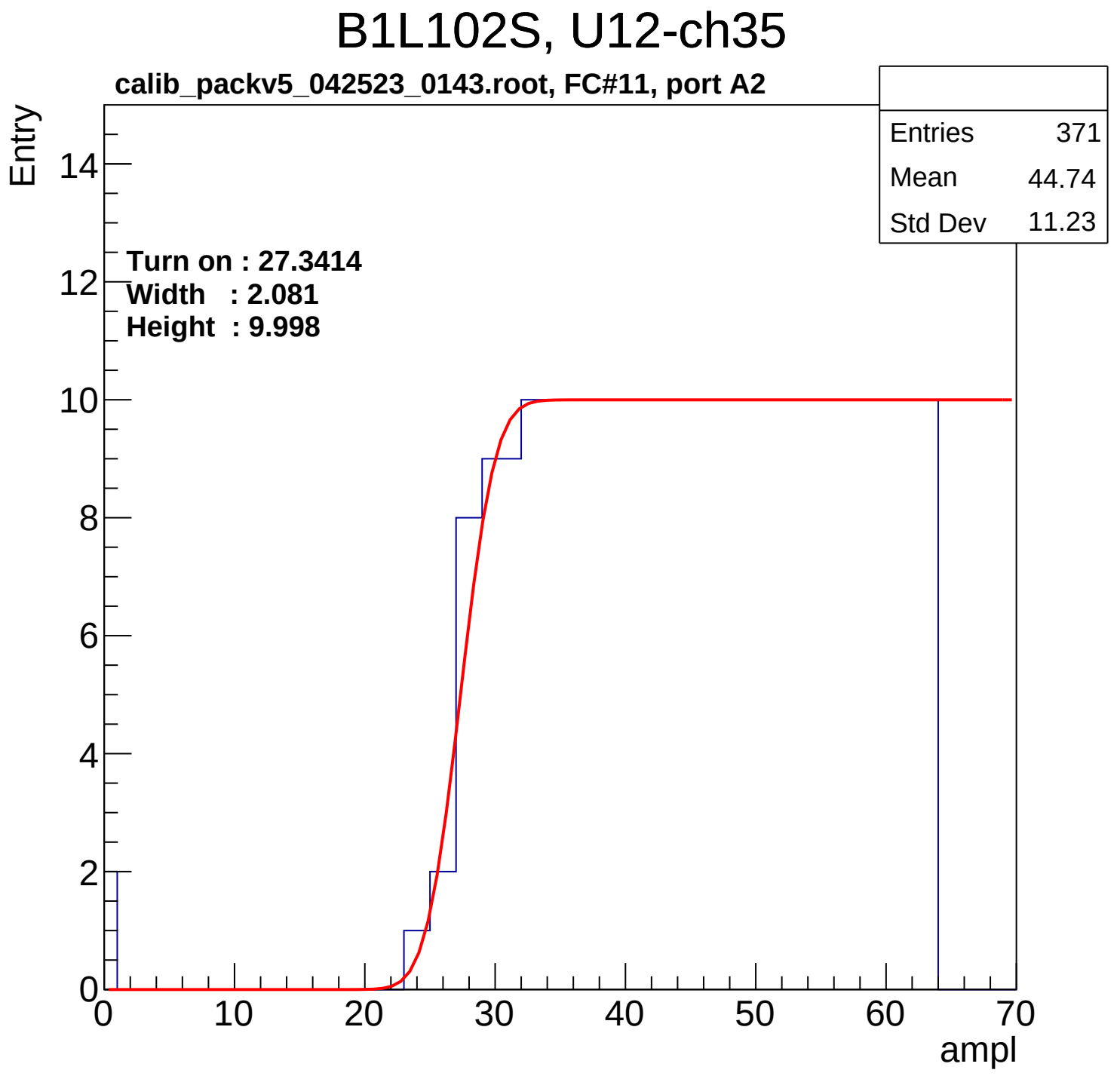
B1L102S, U12-ch35
calib_packv5_042523_0143.root, FC#11, port A2
Entries 371
Mean 44.74
Std Dev 11.23
Turn on : 27.3414
Width : 2.081
Height : 9.998
Entry
ampl
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6
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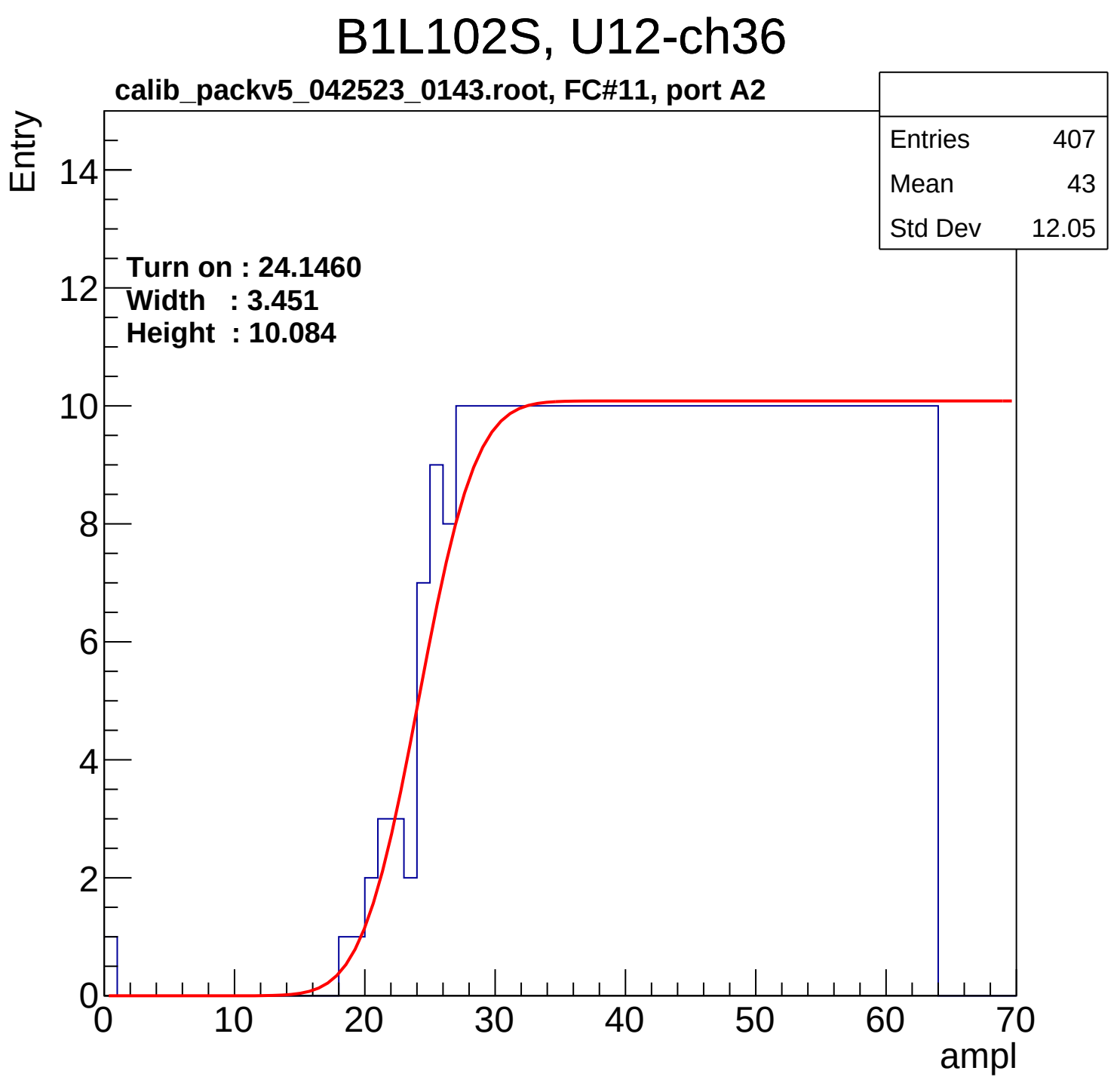
B1L102S, U12-ch36
calib_packv5_042523_0143.root, FC#11, port A2
Entries 407
Mean 43
Std Dev 12.05
Turn on : 24.1460
Width : 3.451
Height : 10.084
Entry
ampl
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2
4
6
8
10
12
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0
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60
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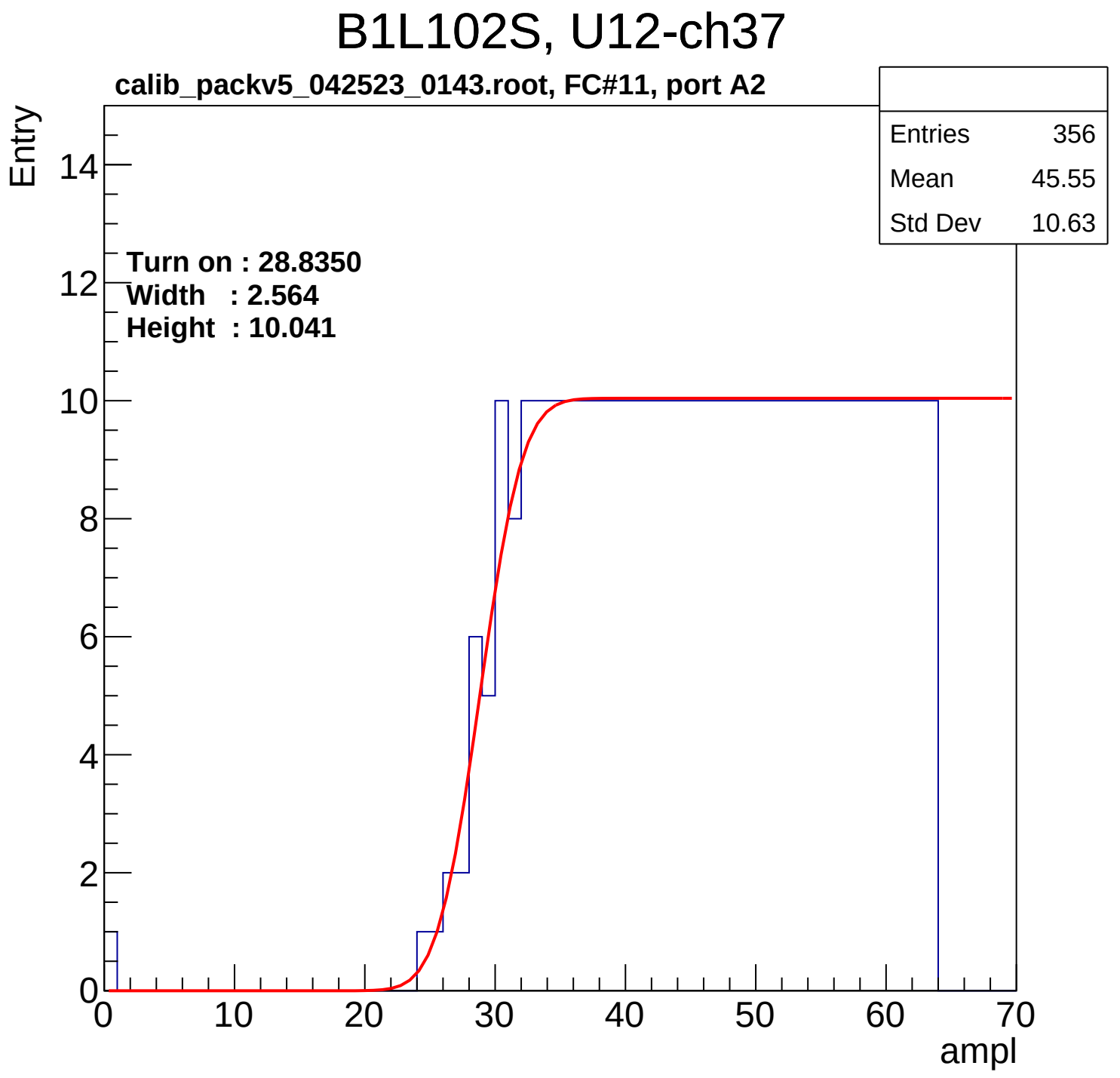
B1L102S, U12-ch37
calib_packv5_042523_0143.root, FC#11, port A2
Entries 356
Mean 45.55
Std Dev 10.63
Turn on : 28.8350
Width : 2.564
Height : 10.041
Entry
ampl
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6
8
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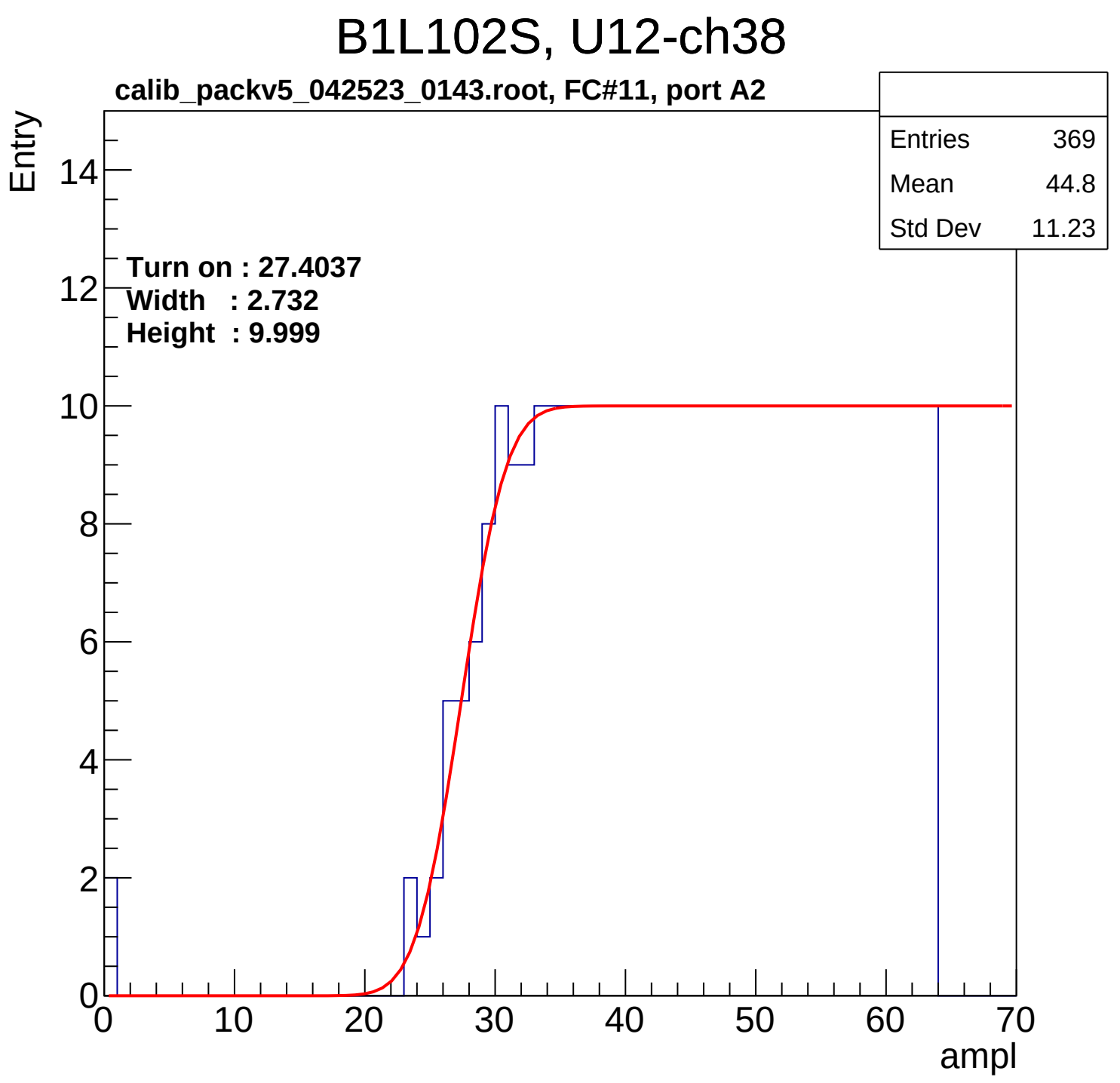
B1L102S, U12-ch38
calib_packv5_042523_0143.root, FC#11, port A2
Entries 369
Mean 44.8
Std Dev 11.23
Turn on : 27.4037
Width : 2.732
Height : 9.999
Entry
ampl
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6
8
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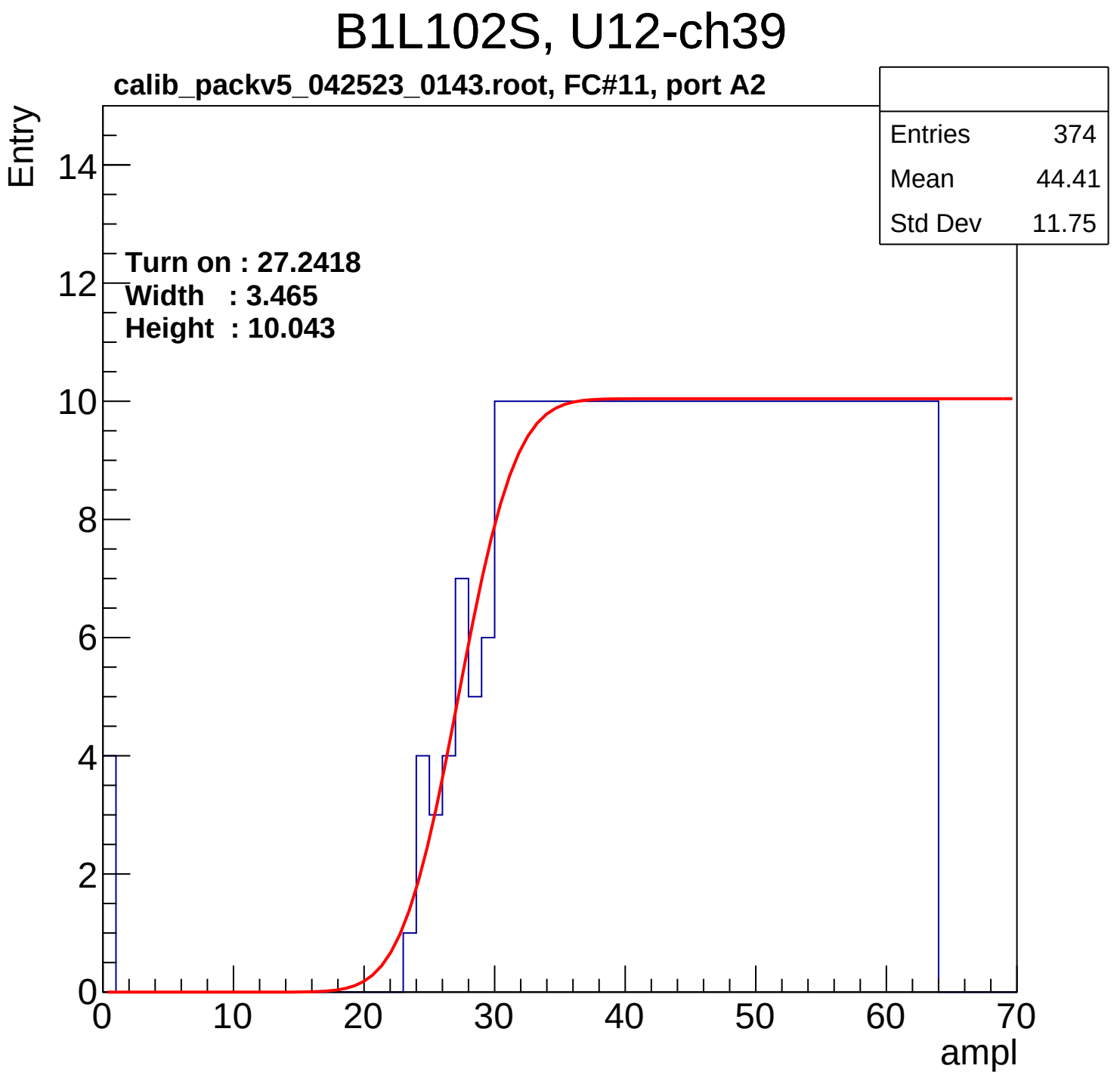
B1L102S, U12-ch39
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.41
Std Dev 11.75
Turn on : 27.2418
Width : 3.465
Height : 10.043
Entry
ampl
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8
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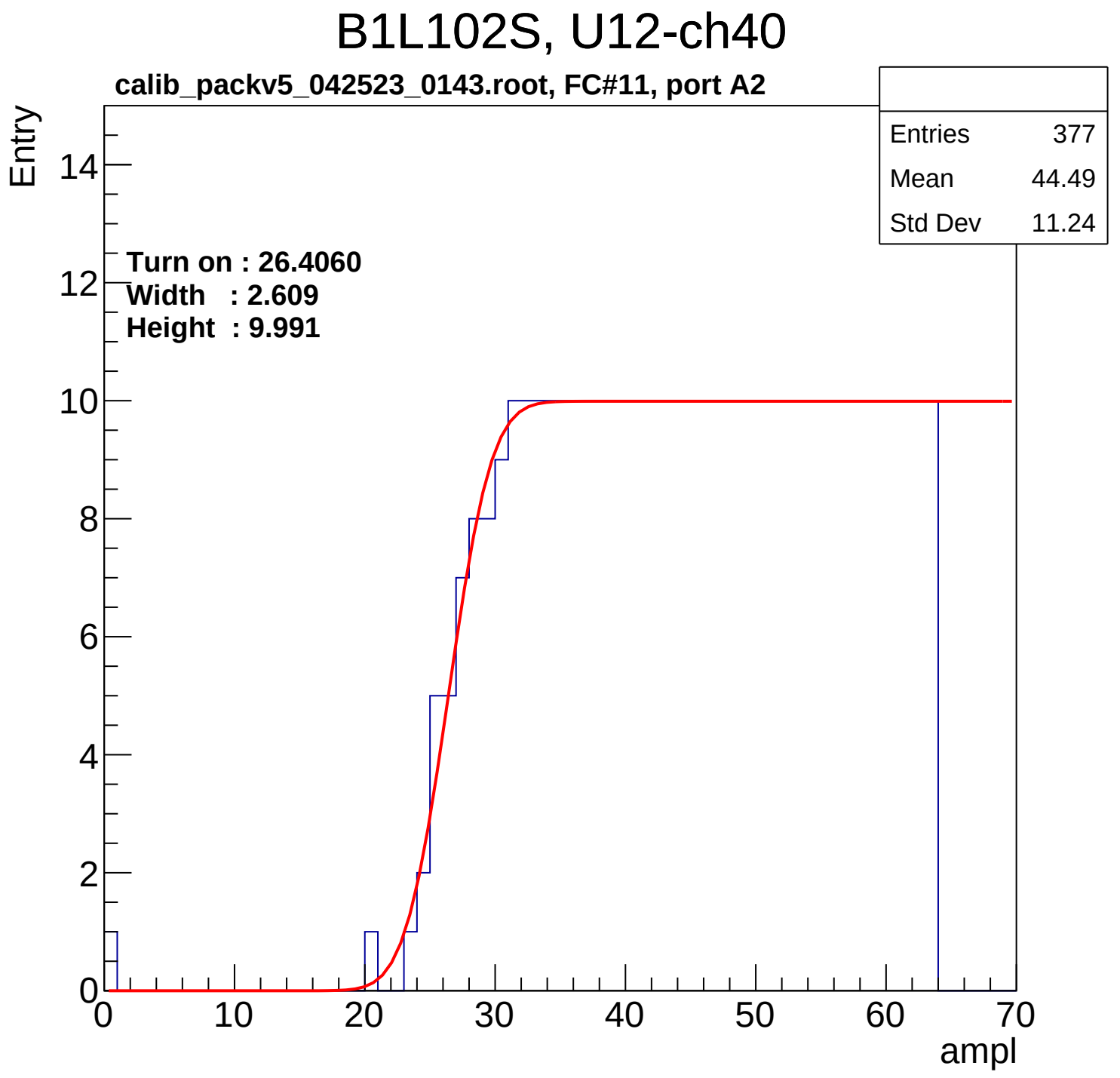
B1L102S, U12-ch40
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.49
Std Dev 11.24
Turn on : 26.4060
Width : 2.609
Height : 9.991
Entry
ampl
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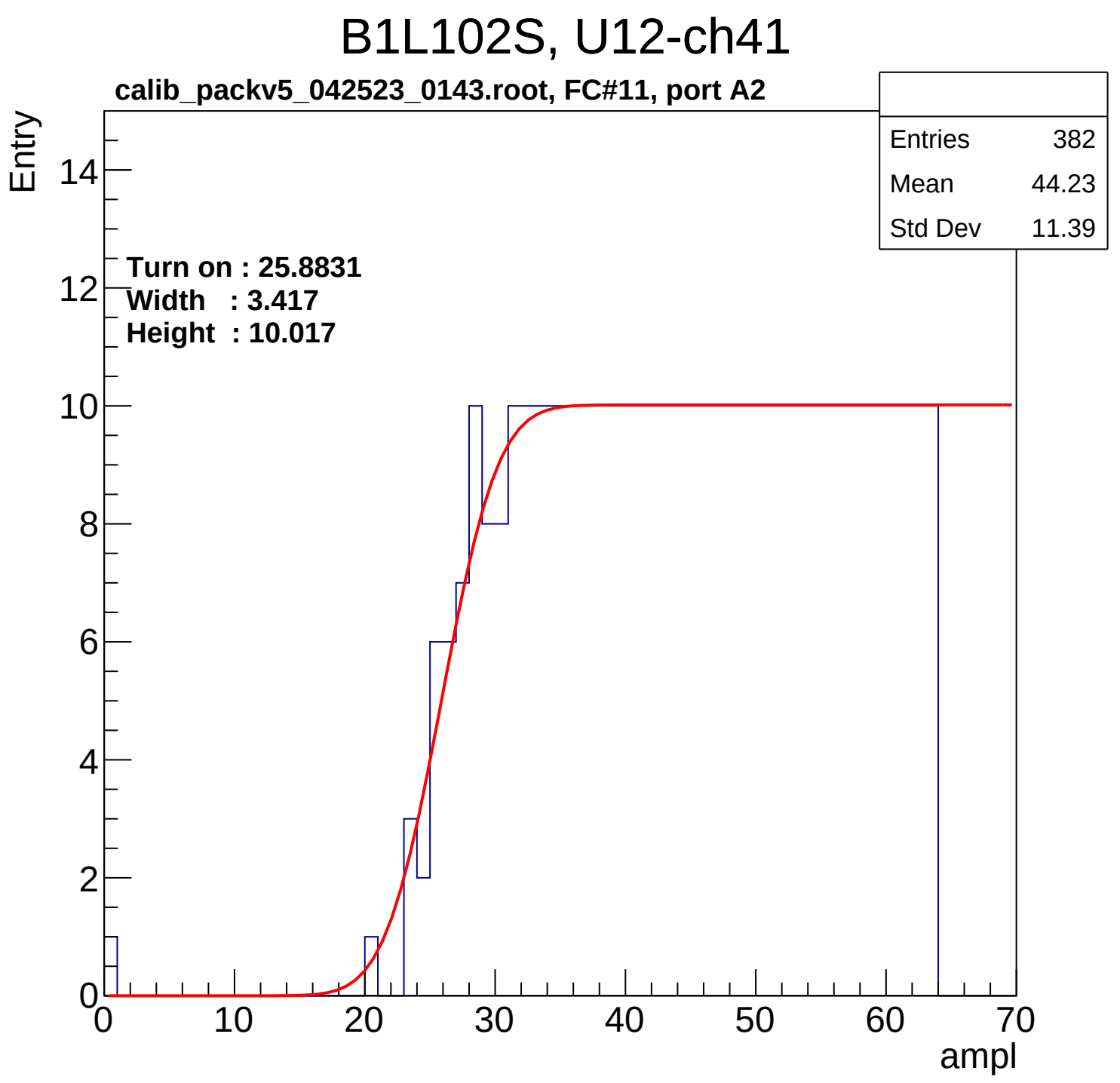
B1L102S, U12-ch41
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.23
Std Dev 11.39
Turn on : 25.8831
Width : 3.417
Height : 10.017
Entry
ampl
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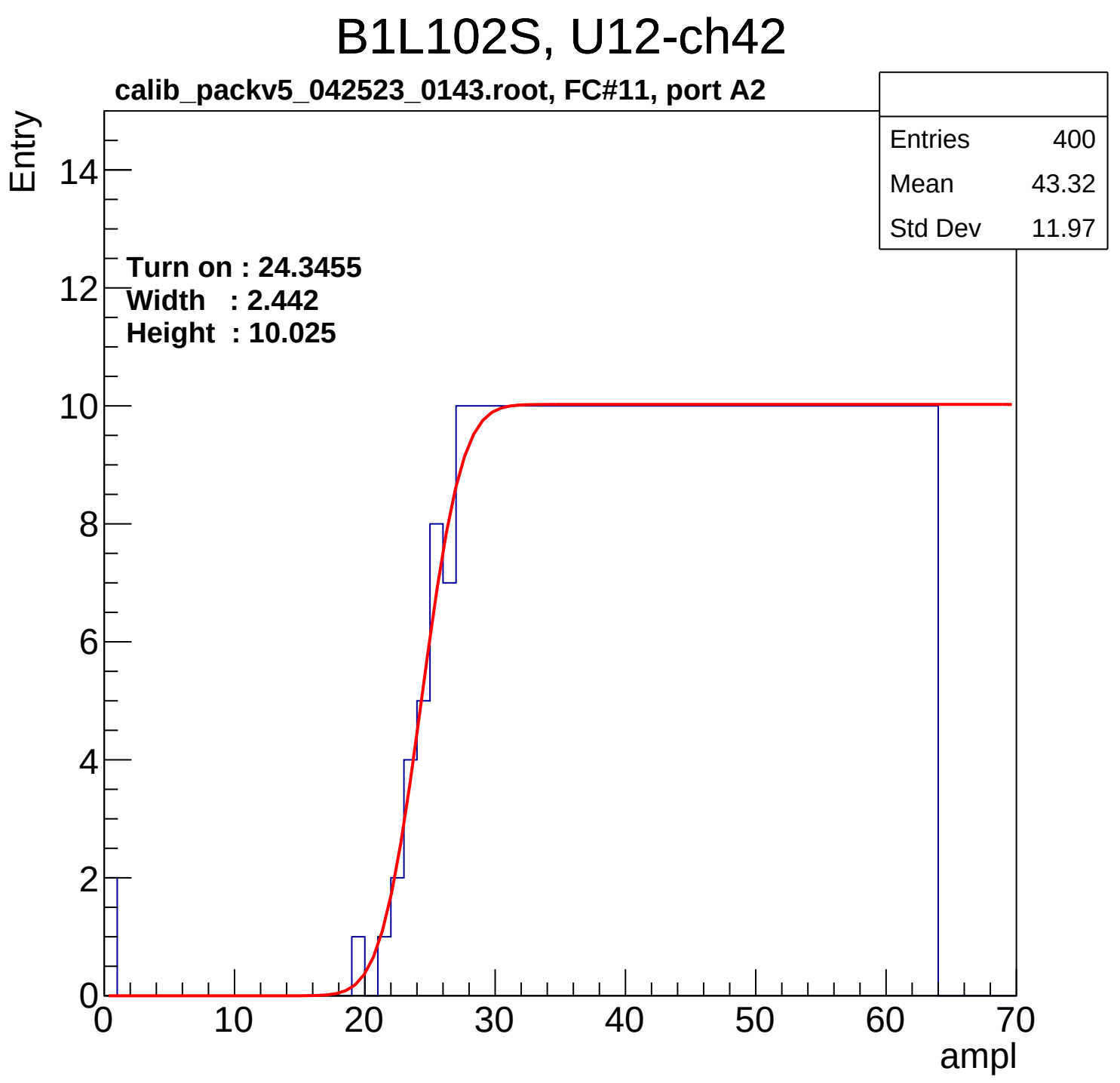
B1L102S, U12-ch42
calib_packv5_042523_0143.root, FC#11, port A2
Entries 400
Mean 43.32
Std Dev 11.97
Turn on : 24.3455
Width : 2.442
Height : 10.025
Entry
ampl
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6
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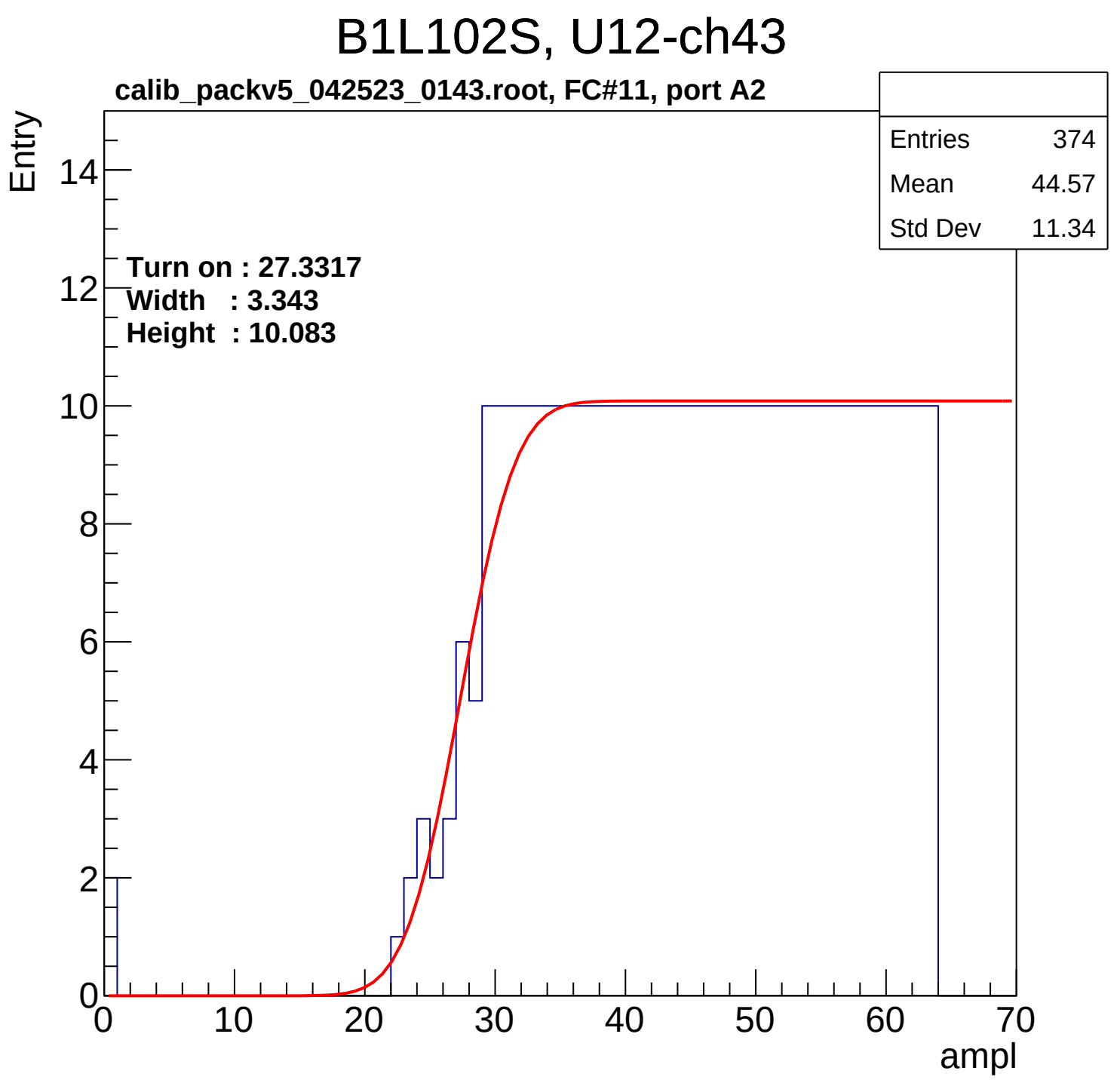
B1L102S, U12-ch43
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.57
Std Dev 11.34
Turn on : 27.3317
Width : 3.343
Height : 10.083
Entry
ampl
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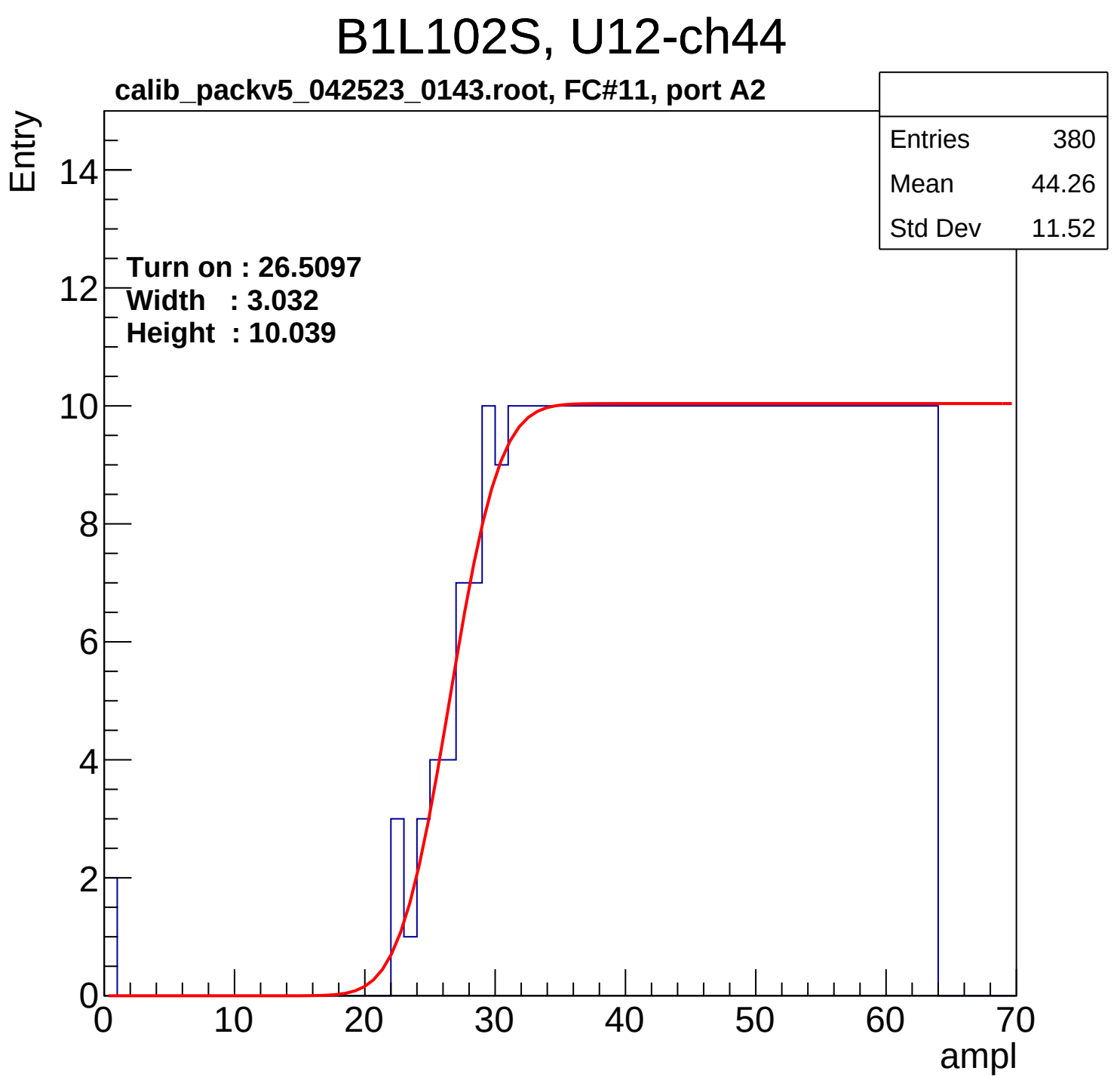
B1L102S, U12-ch44
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.26
Std Dev 11.52
Turn on : 26.5097
Width : 3.032
Height : 10.039
Entry
ampl
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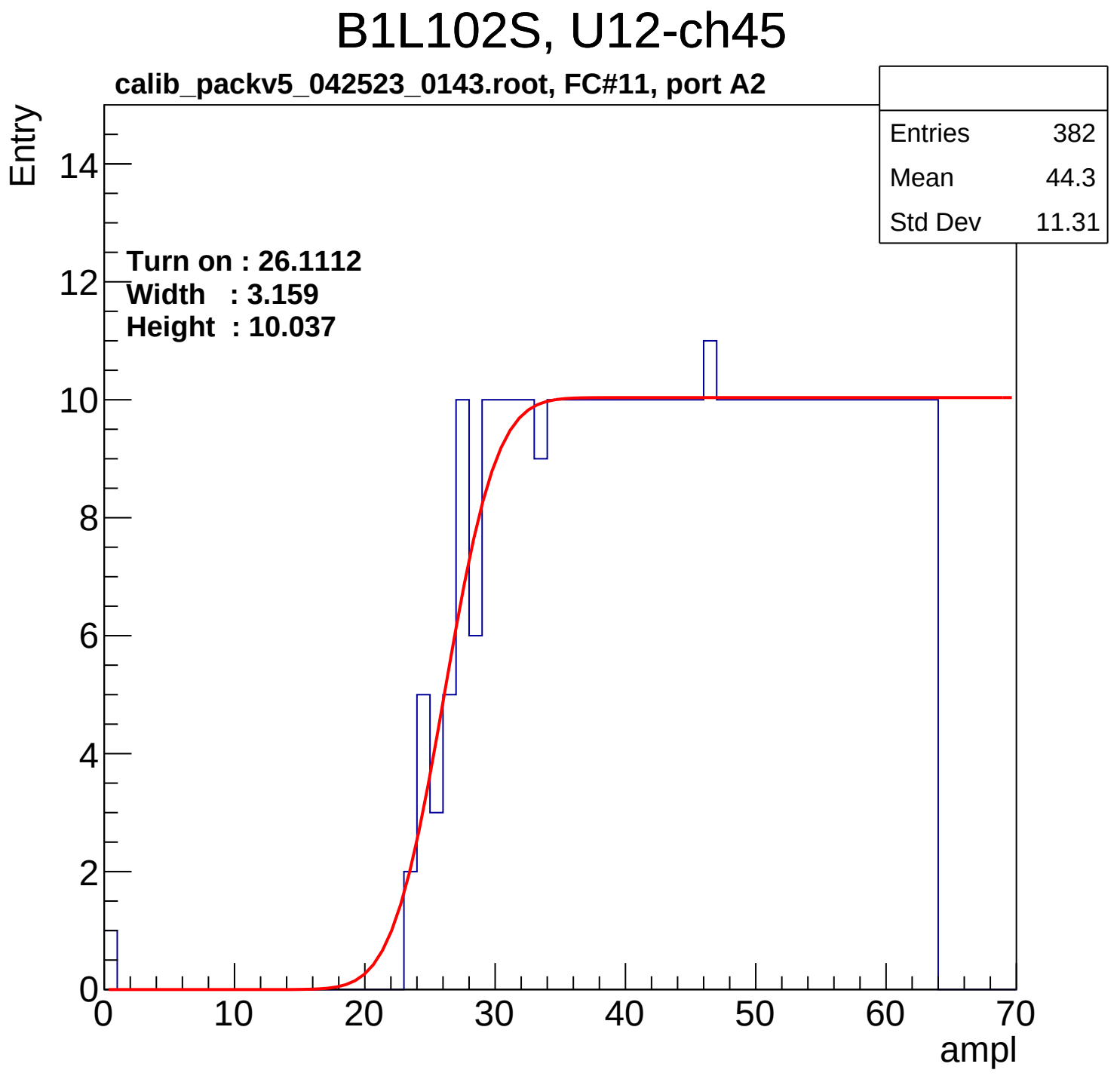
B1L102S, U12-ch45
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.3
Std Dev 11.31
Turn on : 26.1112
Width : 3.159
Height : 10.037
Entry
ampl
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6
8
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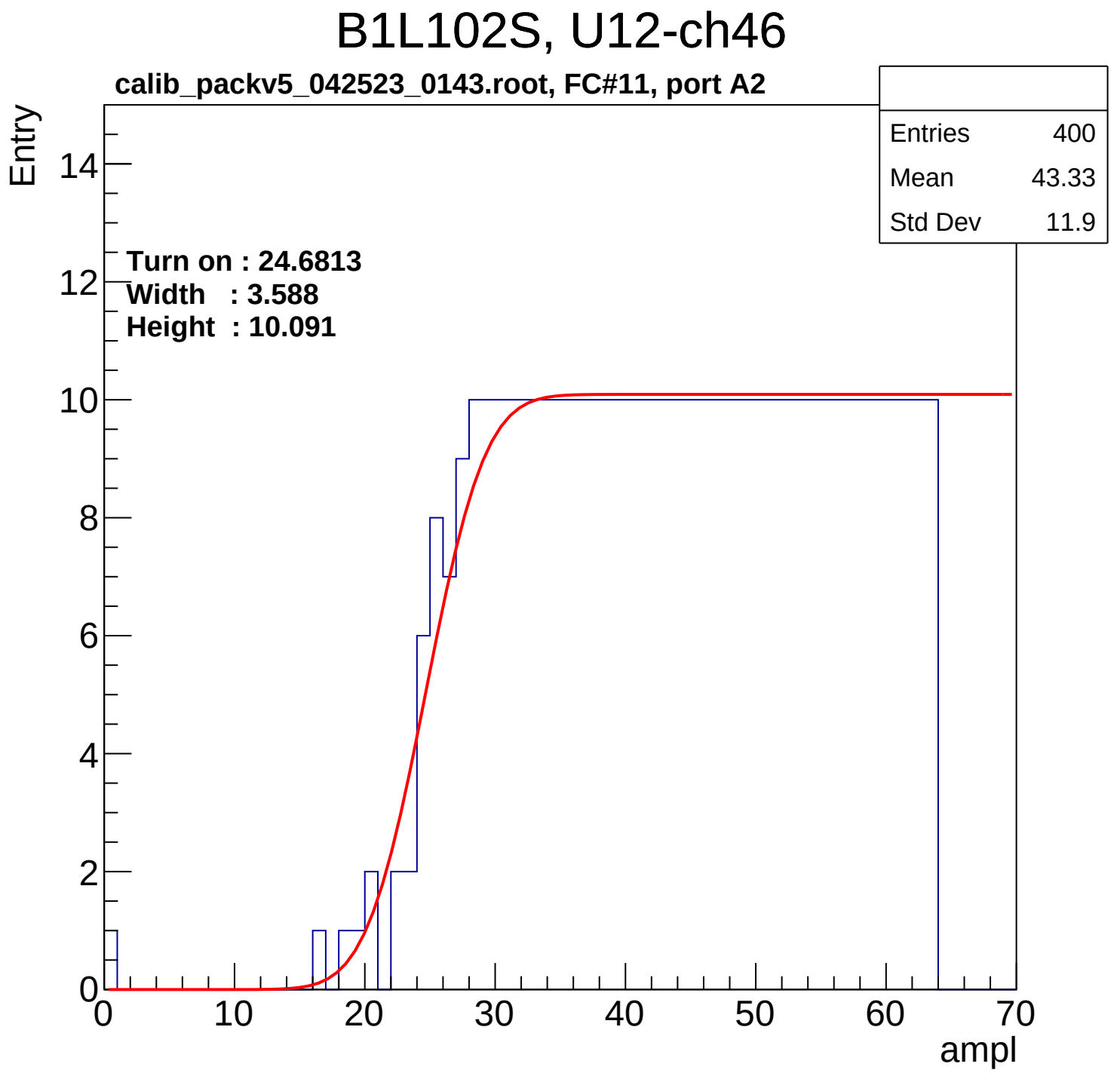
B1L102S, U12-ch46
calib_packv5_042523_0143.root, FC#11, port A2
Entries 400
Mean 43.33
Std Dev 11.9
Turn on : 24.6813
Width : 3.588
Height : 10.091
Entry
ampl
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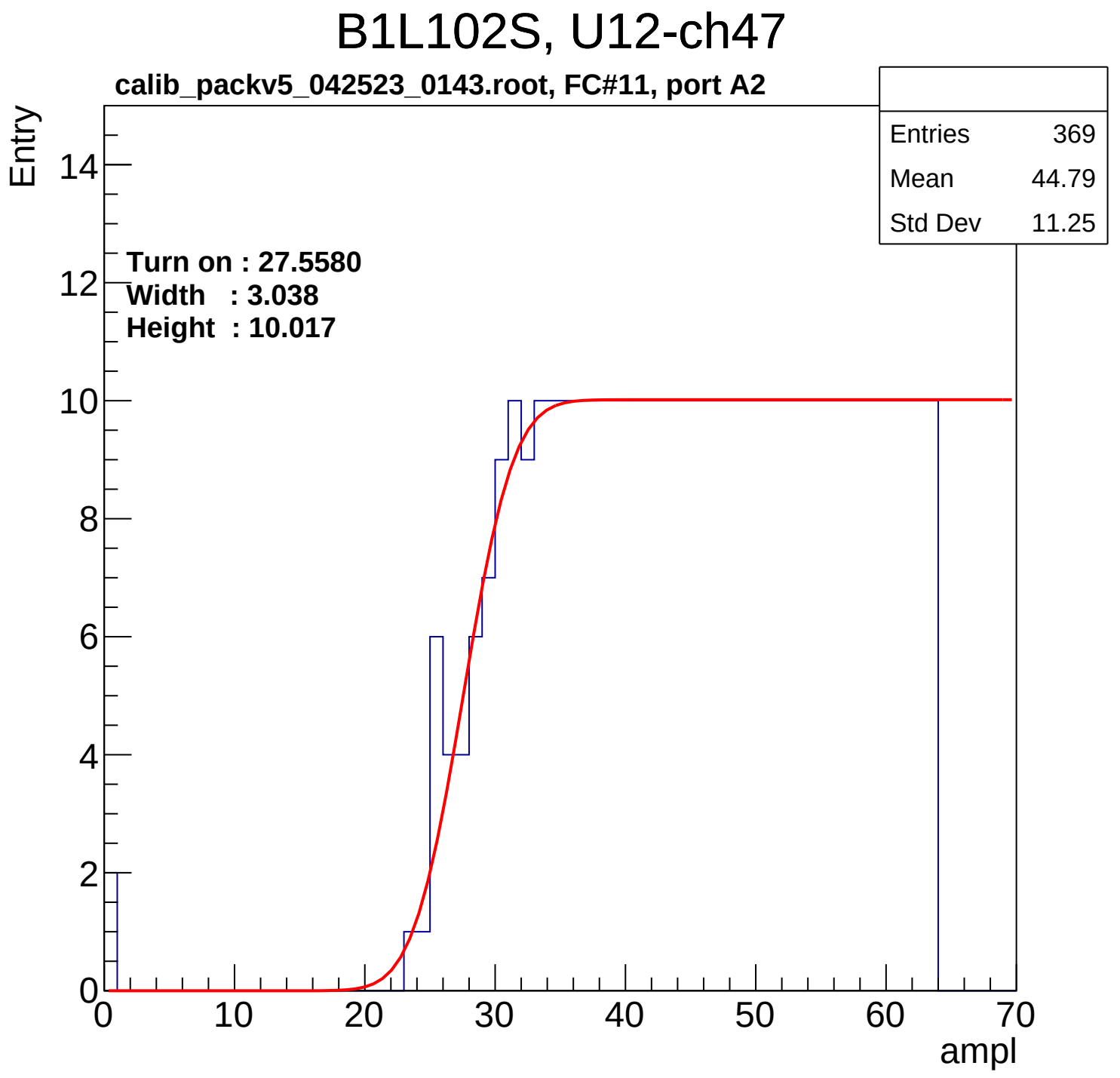
B1L102S, U12-ch47
calib_packv5_042523_0143.root, FC#11, port A2
Entries 369
Mean 44.79
Std Dev 11.25
Turn on : 27.5580
Width : 3.038
Height : 10.017
Entry
ampl
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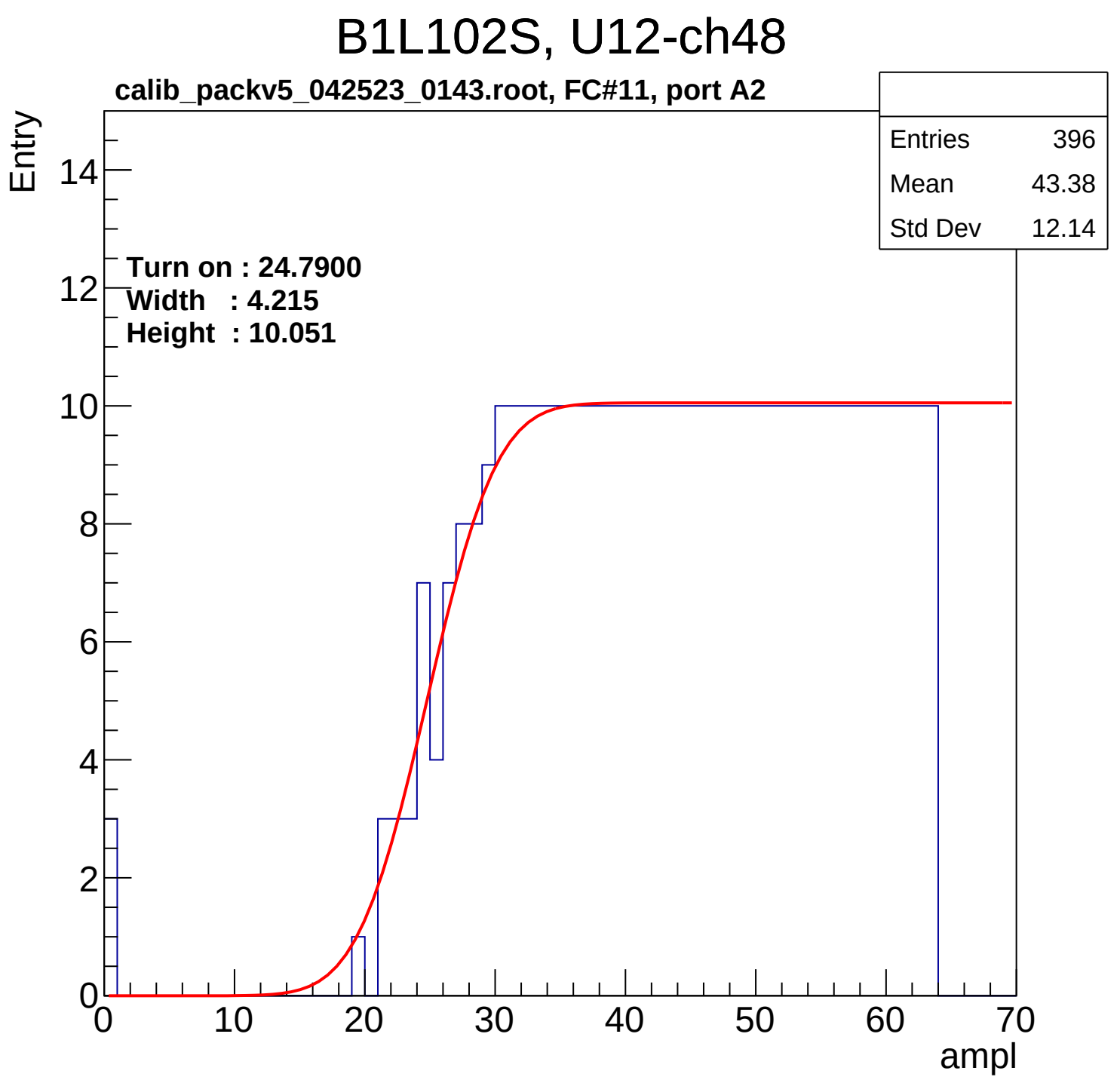
B1L102S, U12-ch48
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.38
Std Dev 12.14
Turn on : 24.7900
Width : 4.215
Height : 10.051
Entry
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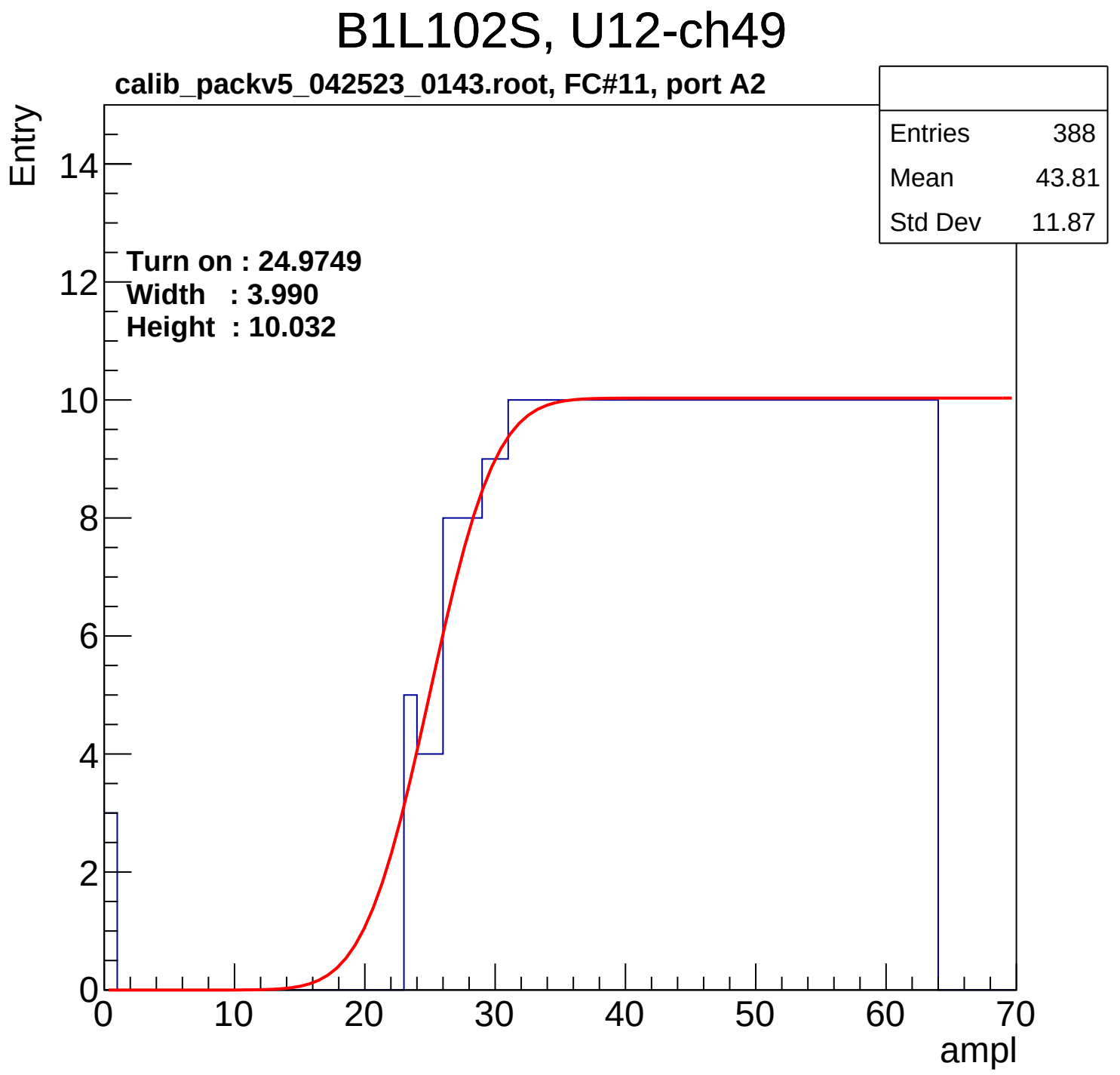
B1L102S, U12-ch49
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.81
Std Dev 11.87
Turn on : 24.9749
Width : 3.990
Height : 10.032
Entry
ampl
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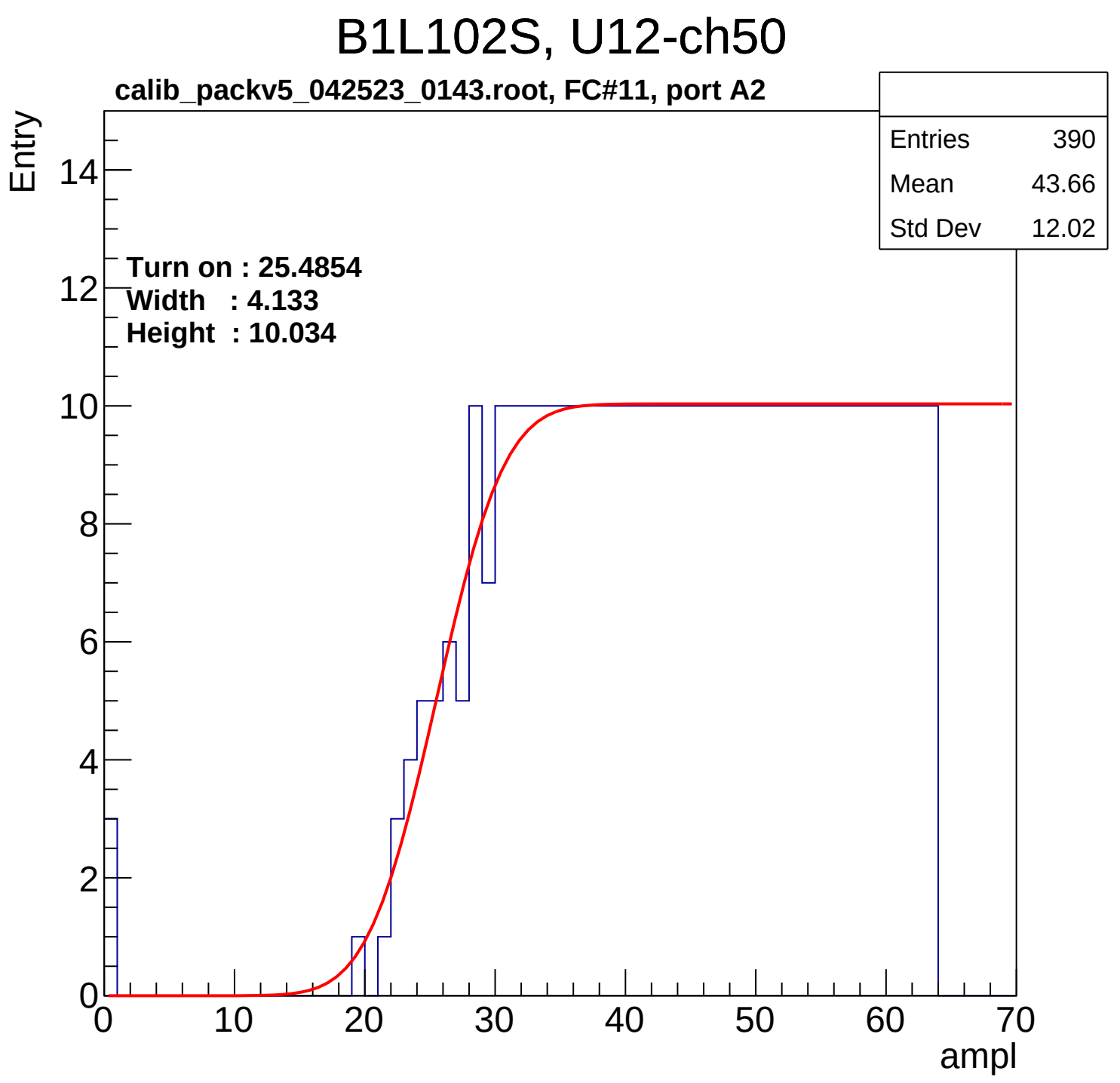
B1L102S, U12-ch50
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.66
Std Dev 12.02
Turn on : 25.4854
Width : 4.133
Height : 10.034
Entry
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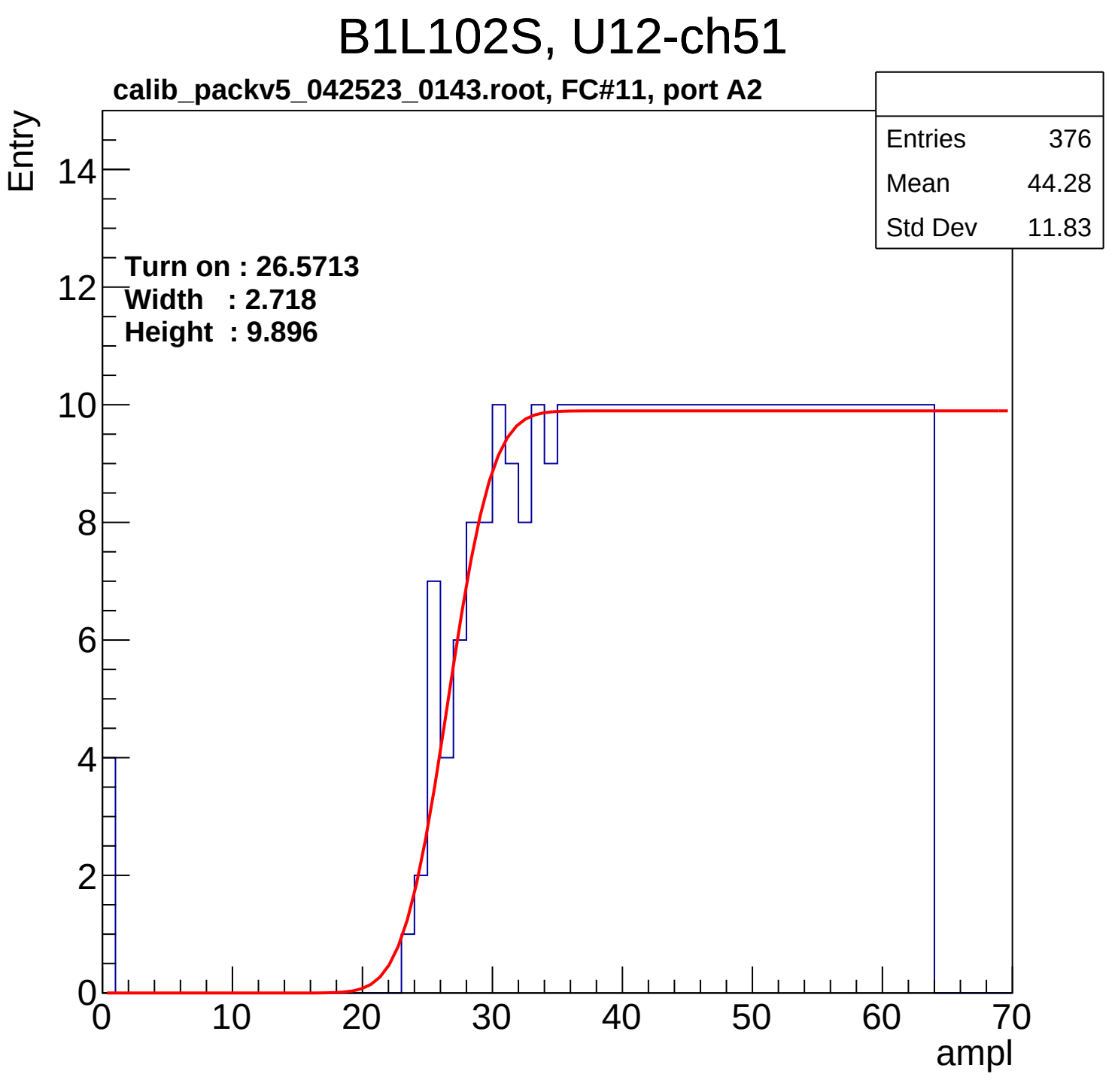
B1L102S, U12-ch51
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.28
Std Dev 11.83
Turn on : 26.5713
Width : 2.718
Height : 9.896
Entry
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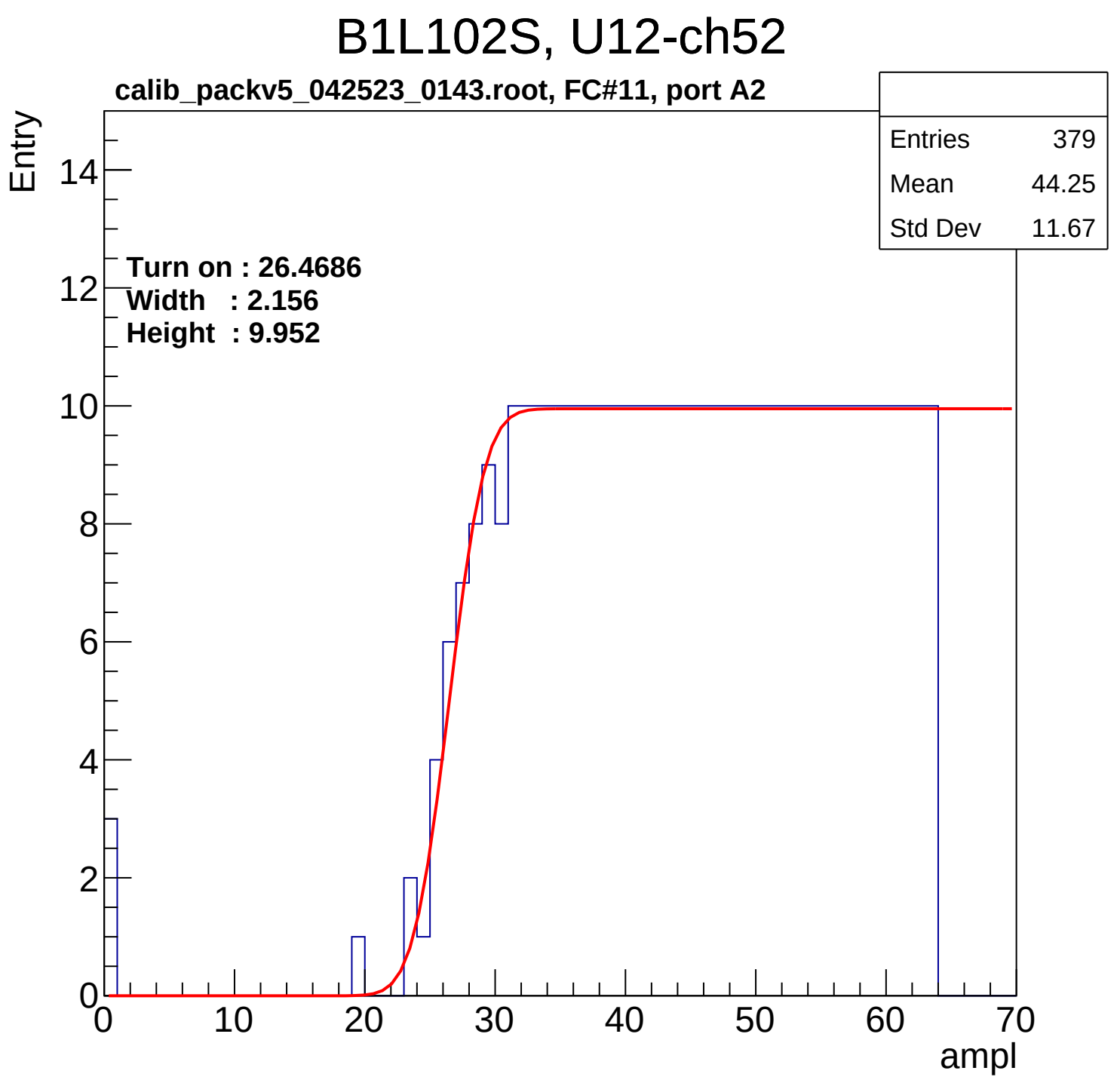
B1L102S, U12-ch52
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.25
Std Dev 11.67
Turn on : 26.4686
Width : 2.156
Height : 9.952
Entry
ampl
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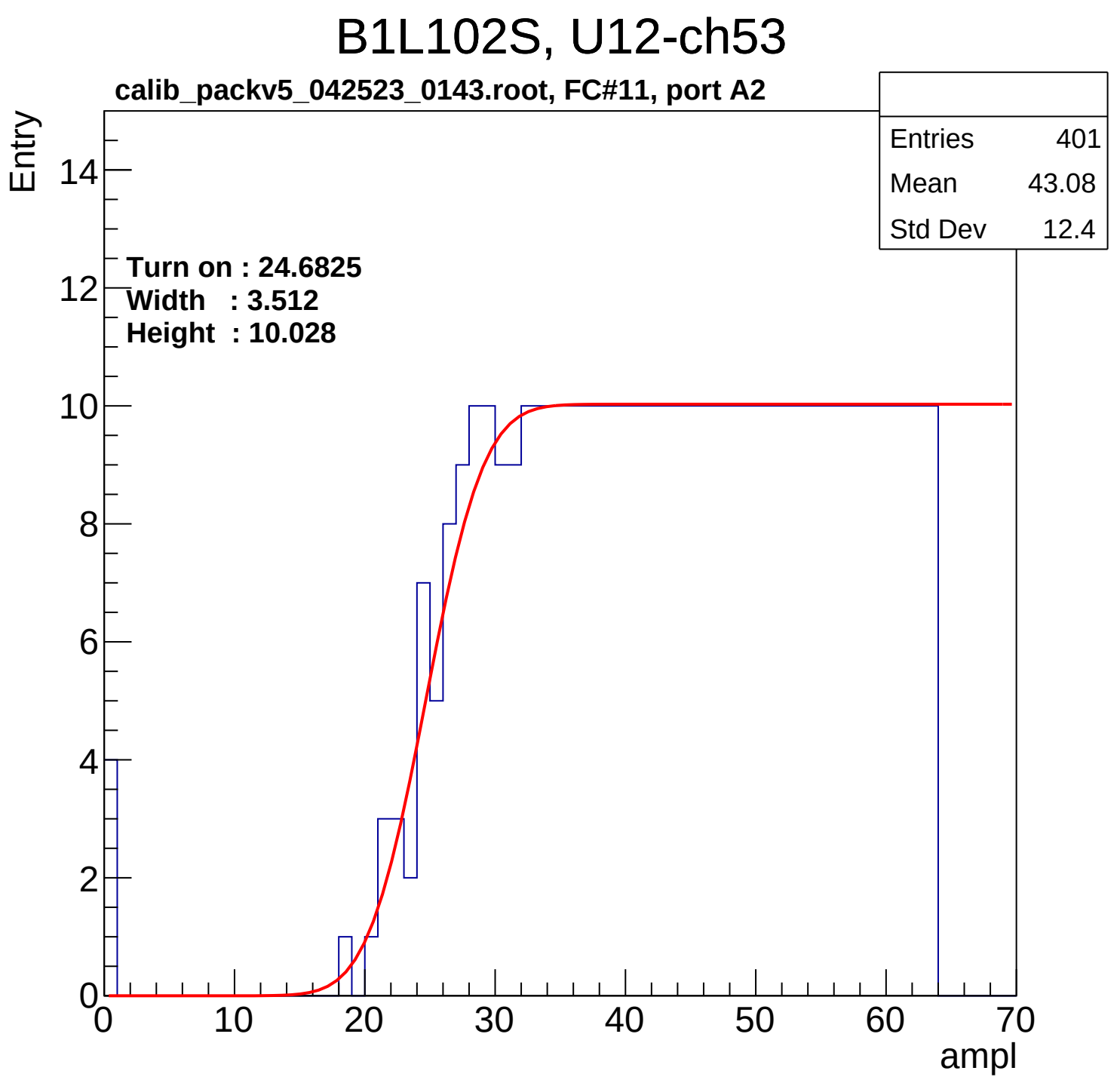
B1L102S, U12-ch53
calib_packv5_042523_0143.root, FC#11, port A2
Entries 401
Mean 43.08
Std Dev 12.4
Turn on : 24.6825
Width : 3.512
Height : 10.028
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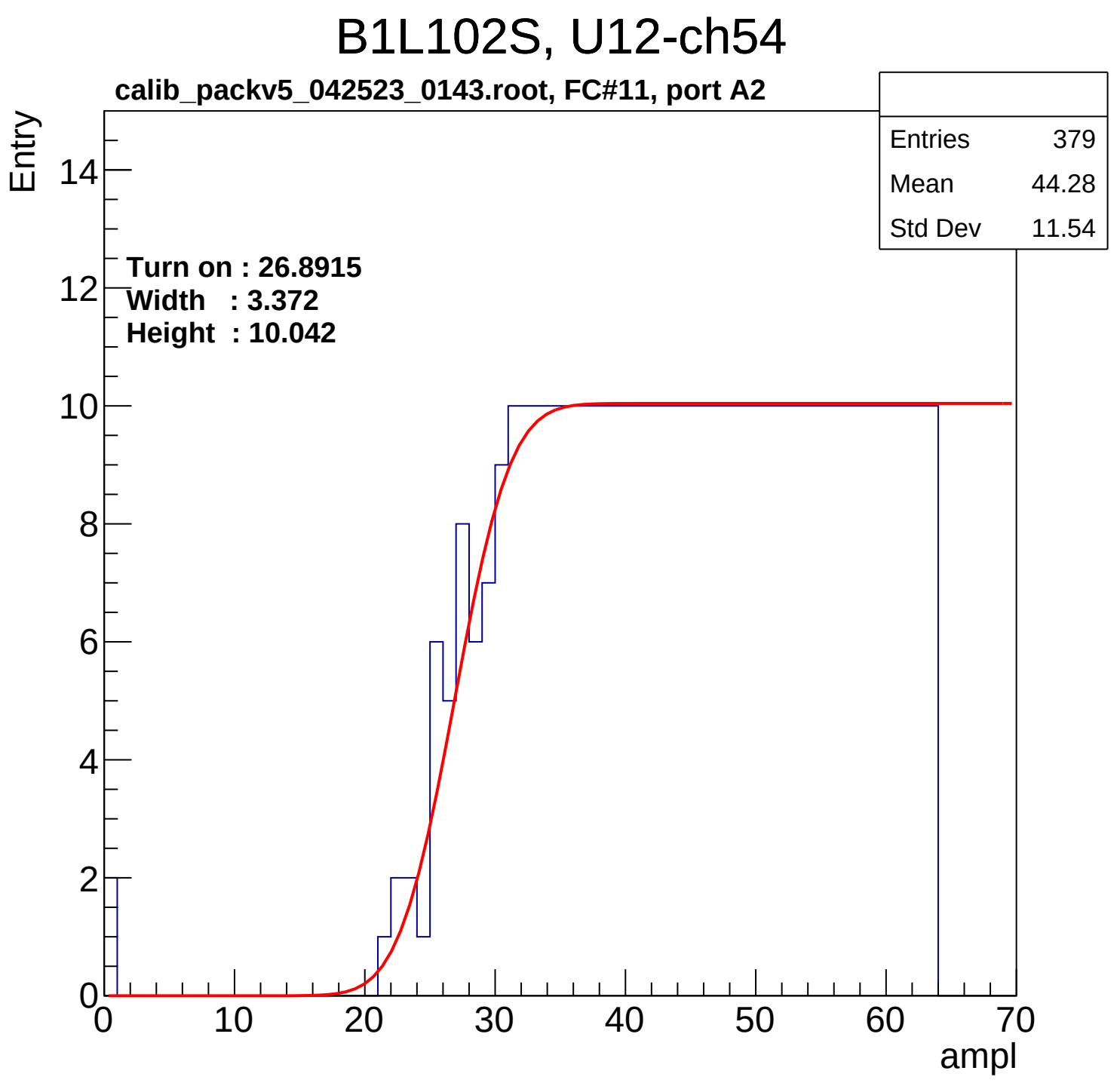
B1L102S, U12-ch54
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.28
Std Dev 11.54
Turn on : 26.8915
Width : 3.372
Height : 10.042
Entry
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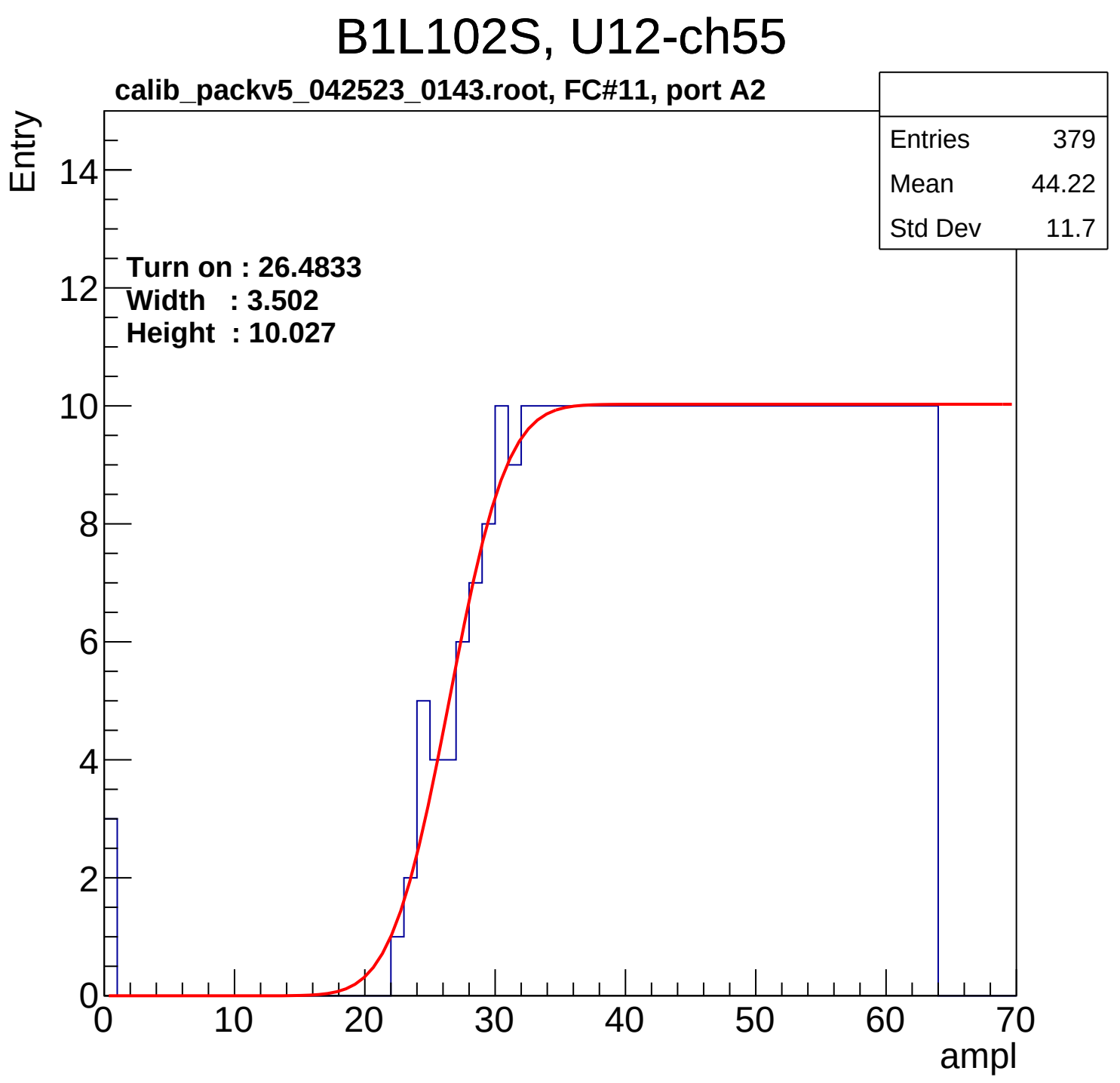
B1L102S, U12-ch55
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.22
Std Dev 11.7
Turn on : 26.4833
Width : 3.502
Height : 10.027
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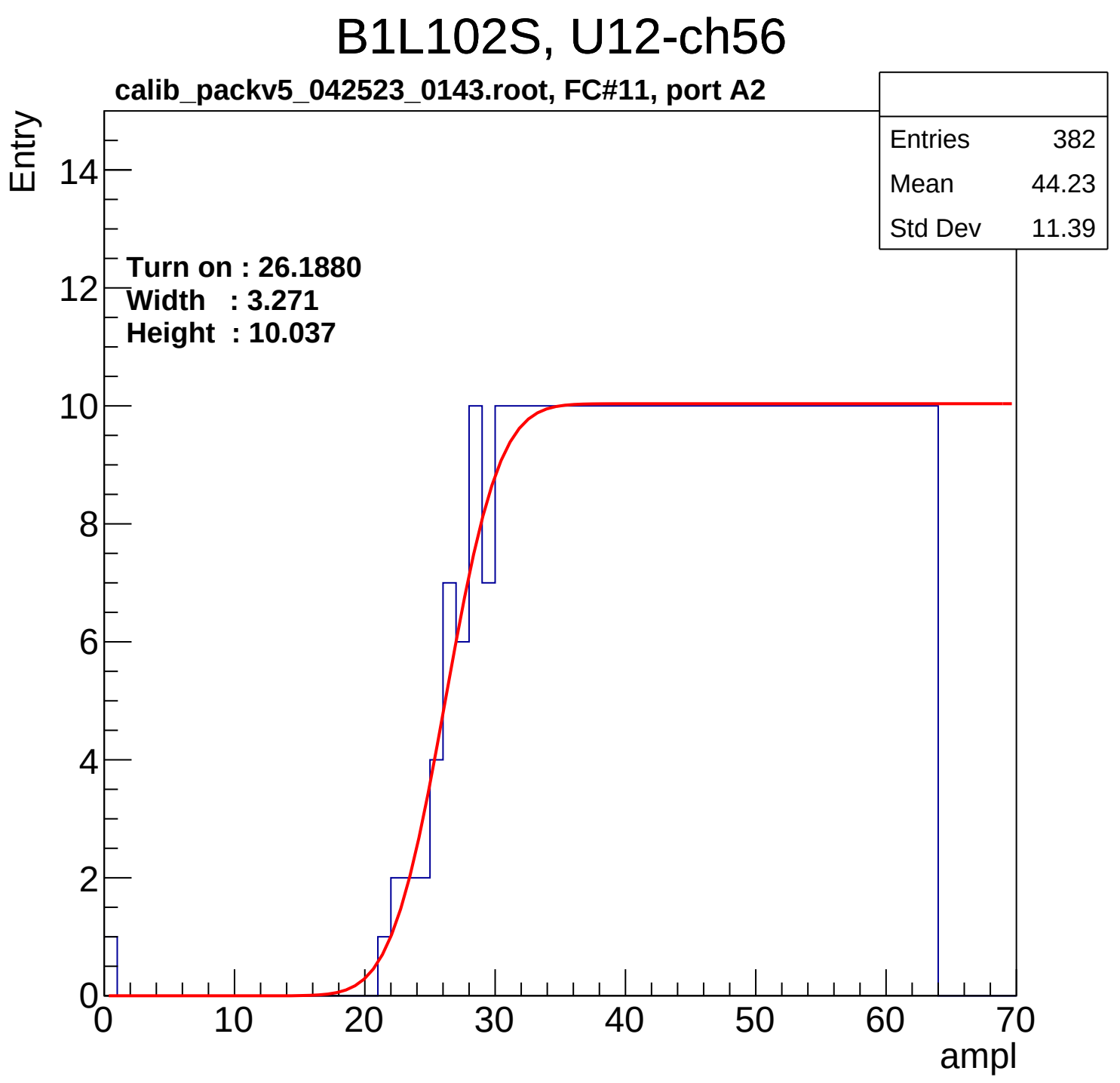
B1L102S, U12-ch56
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.23
Std Dev 11.39
Turn on : 26.1880
Width : 3.271
Height : 10.037
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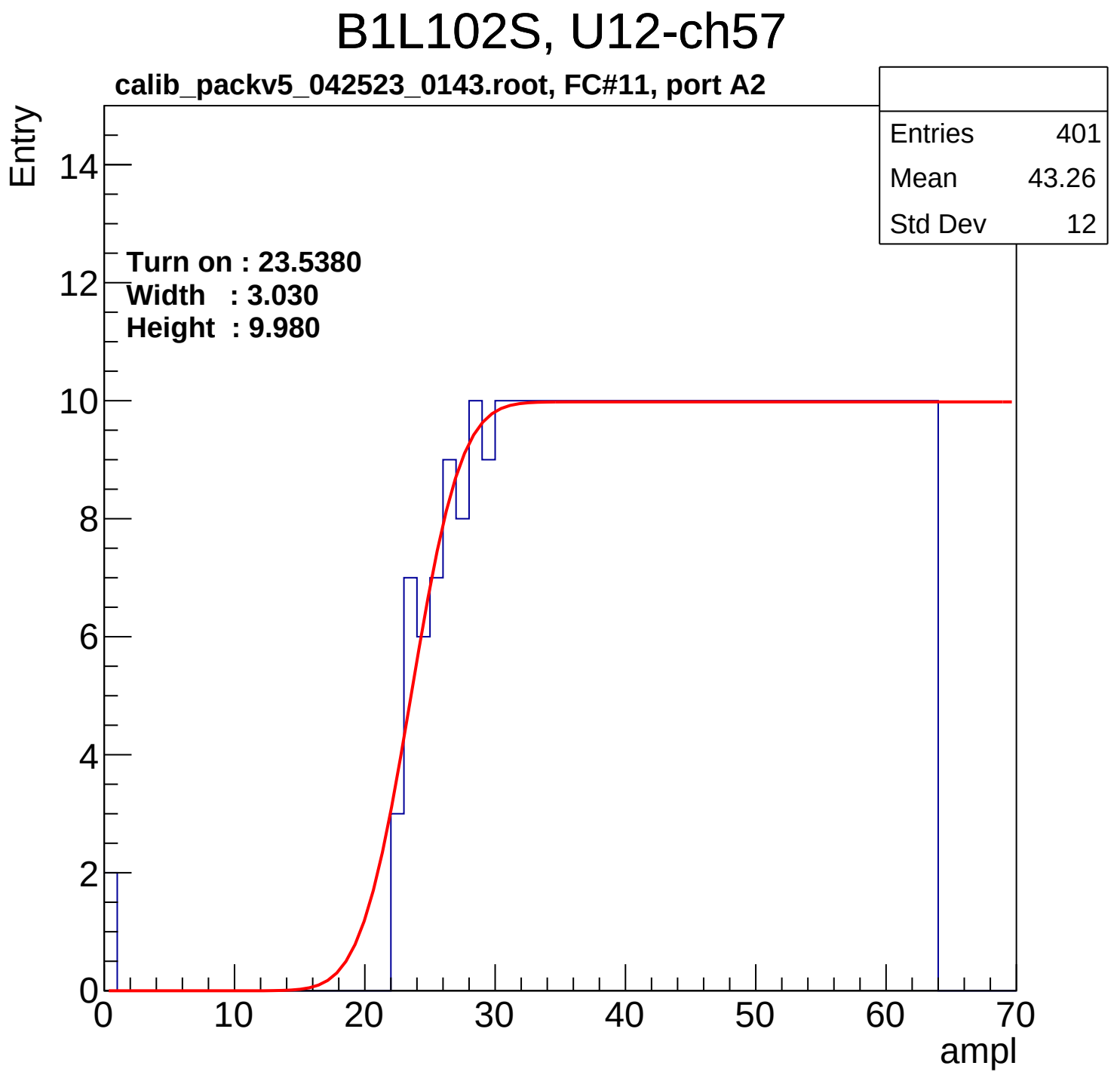
B1L102S, U12-ch57
calib_packv5_042523_0143.root, FC#11, port A2
Entries 401
Mean 43.26
Std Dev 12
Turn on : 23.5380
Width : 3.030
Height : 9.980
Entry
ampl
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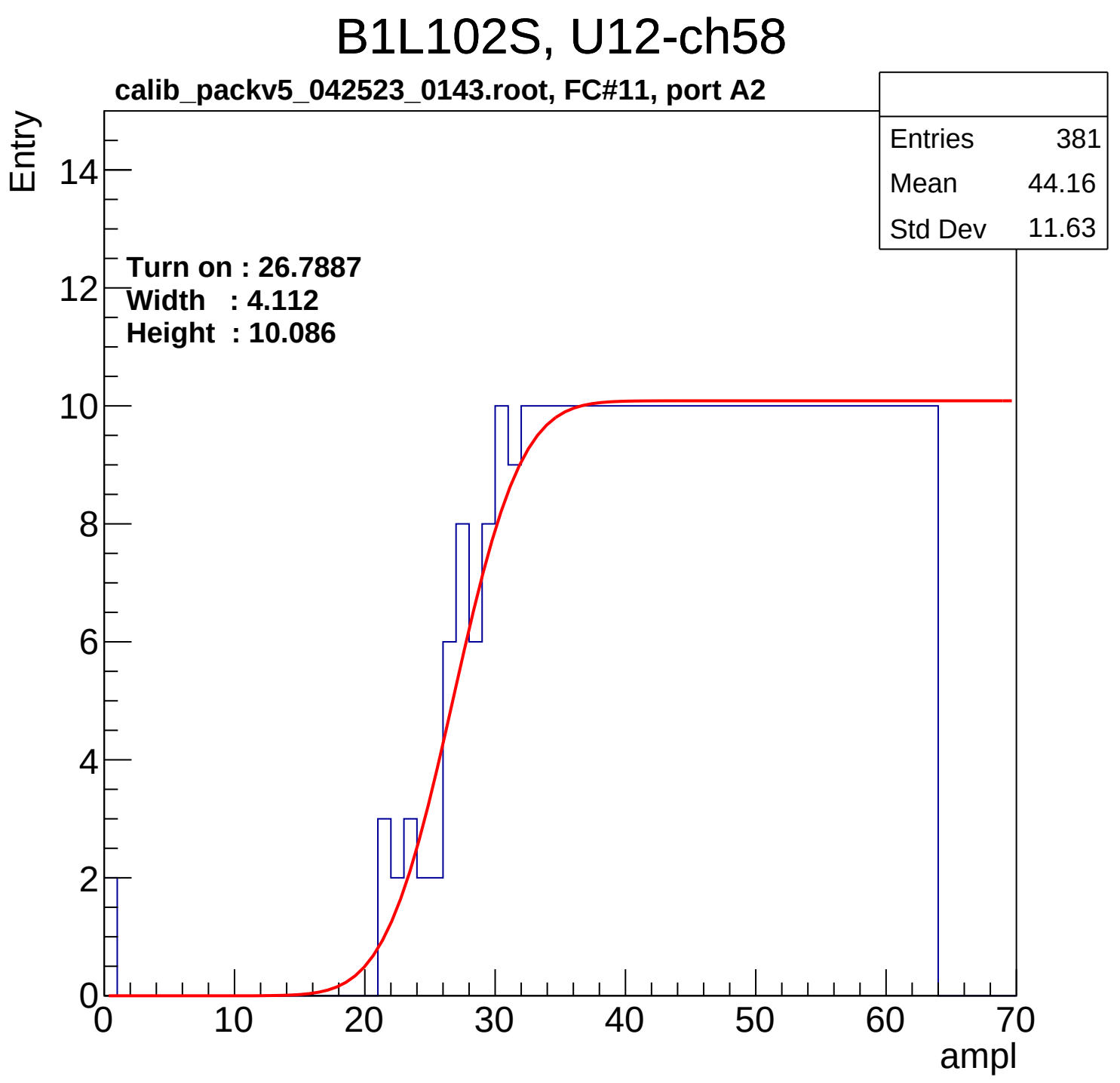
B1L102S, U12-ch58
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.16
Std Dev 11.63
Turn on : 26.7887
Width : 4.112
Height : 10.086
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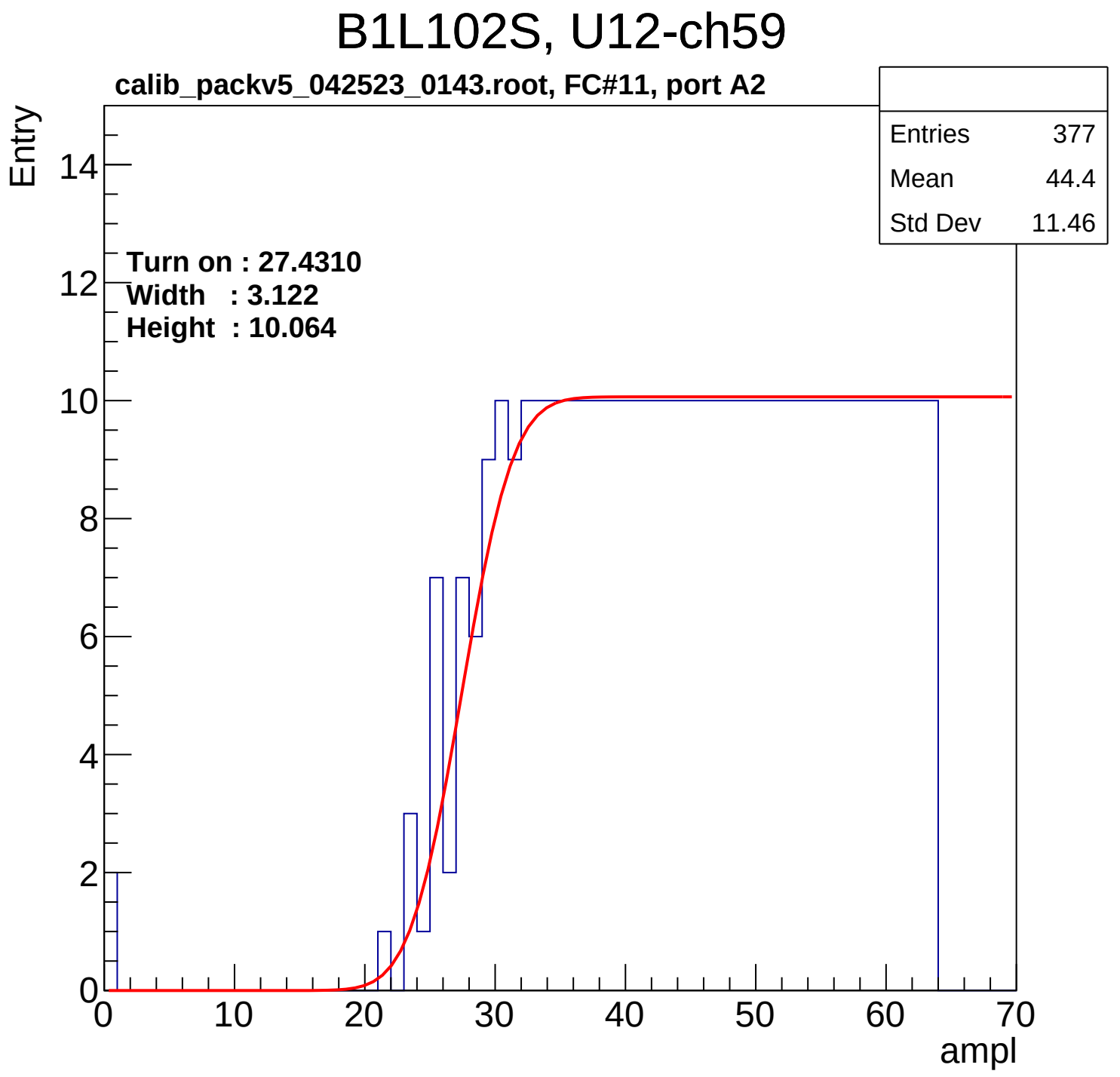
B1L102S, U12-ch59
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.4
Std Dev 11.46
Turn on : 27.4310
Width : 3.122
Height : 10.064
Entry
ampl
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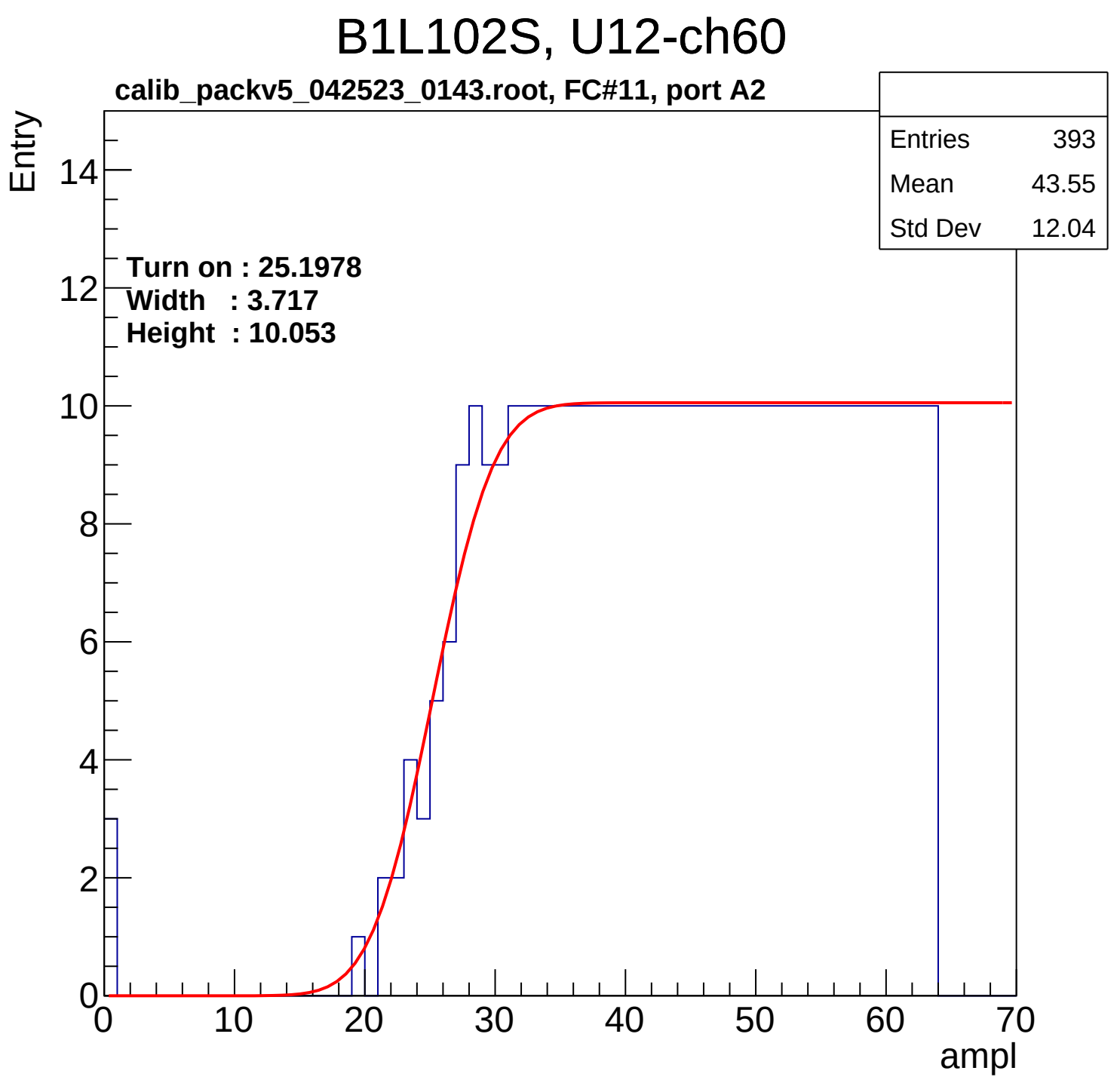
B1L102S, U12-ch60
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.55
Std Dev 12.04
Turn on : 25.1978
Width : 3.717
Height : 10.053
Entry
ampl
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2
4
6
8
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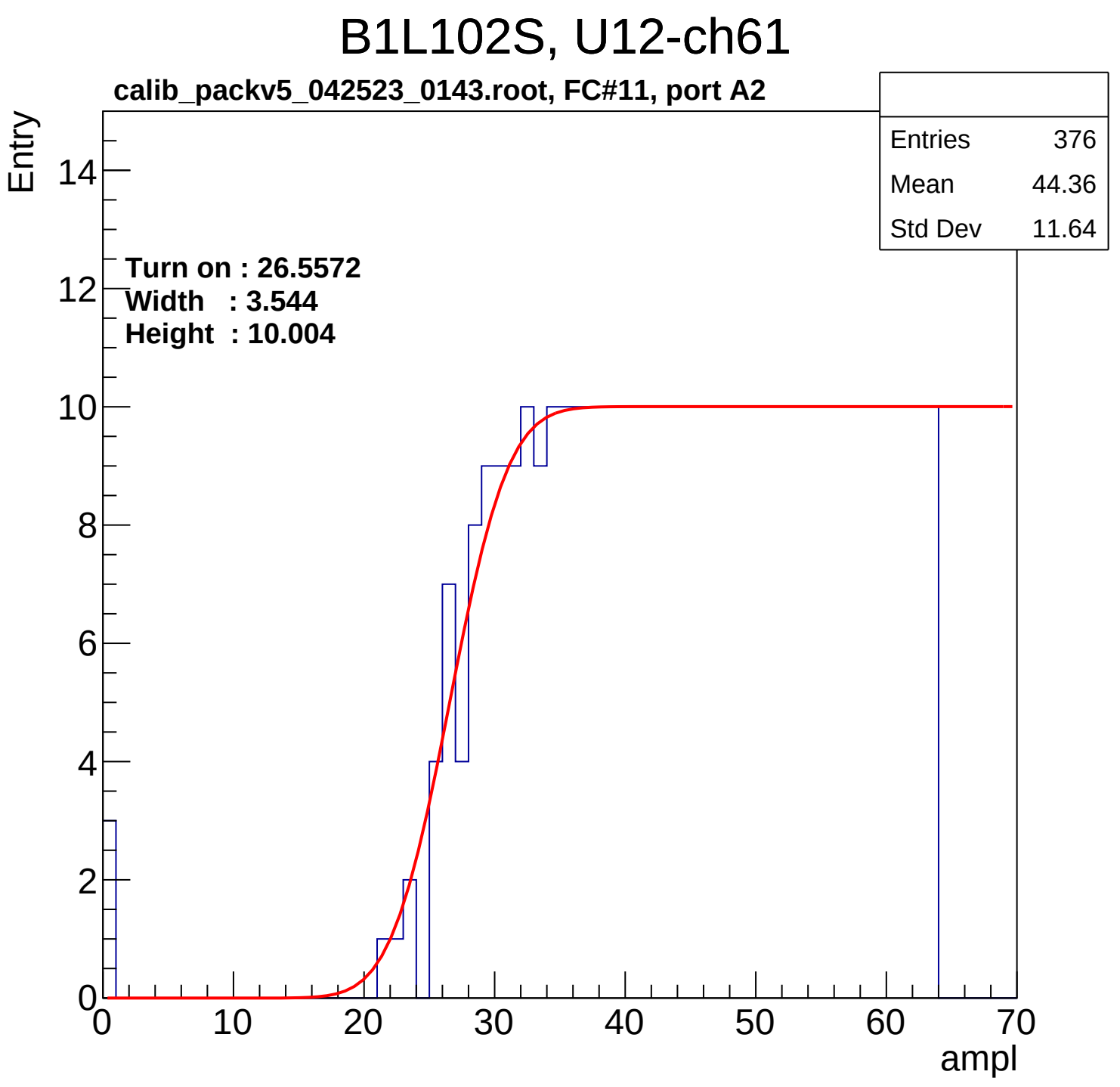
B1L102S, U12-ch61
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.36
Std Dev 11.64
Turn on : 26.5572
Width : 3.544
Height : 10.004
Entry
ampl
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2
4
6
8
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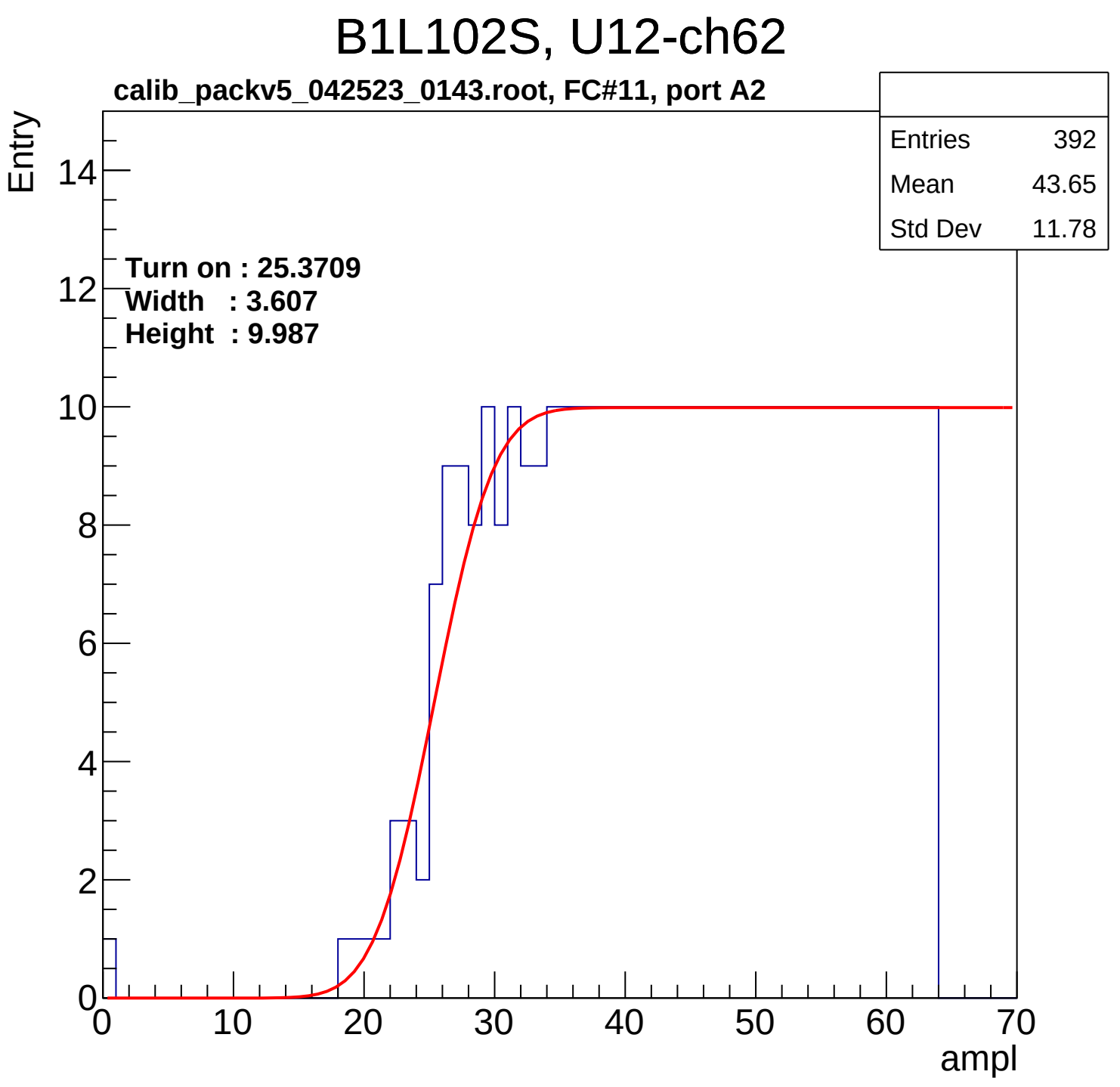
B1L102S, U12-ch62
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.65
Std Dev 11.78
Turn on : 25.3709
Width : 3.607
Height : 9.987
Entry
ampl
0
2
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6
8
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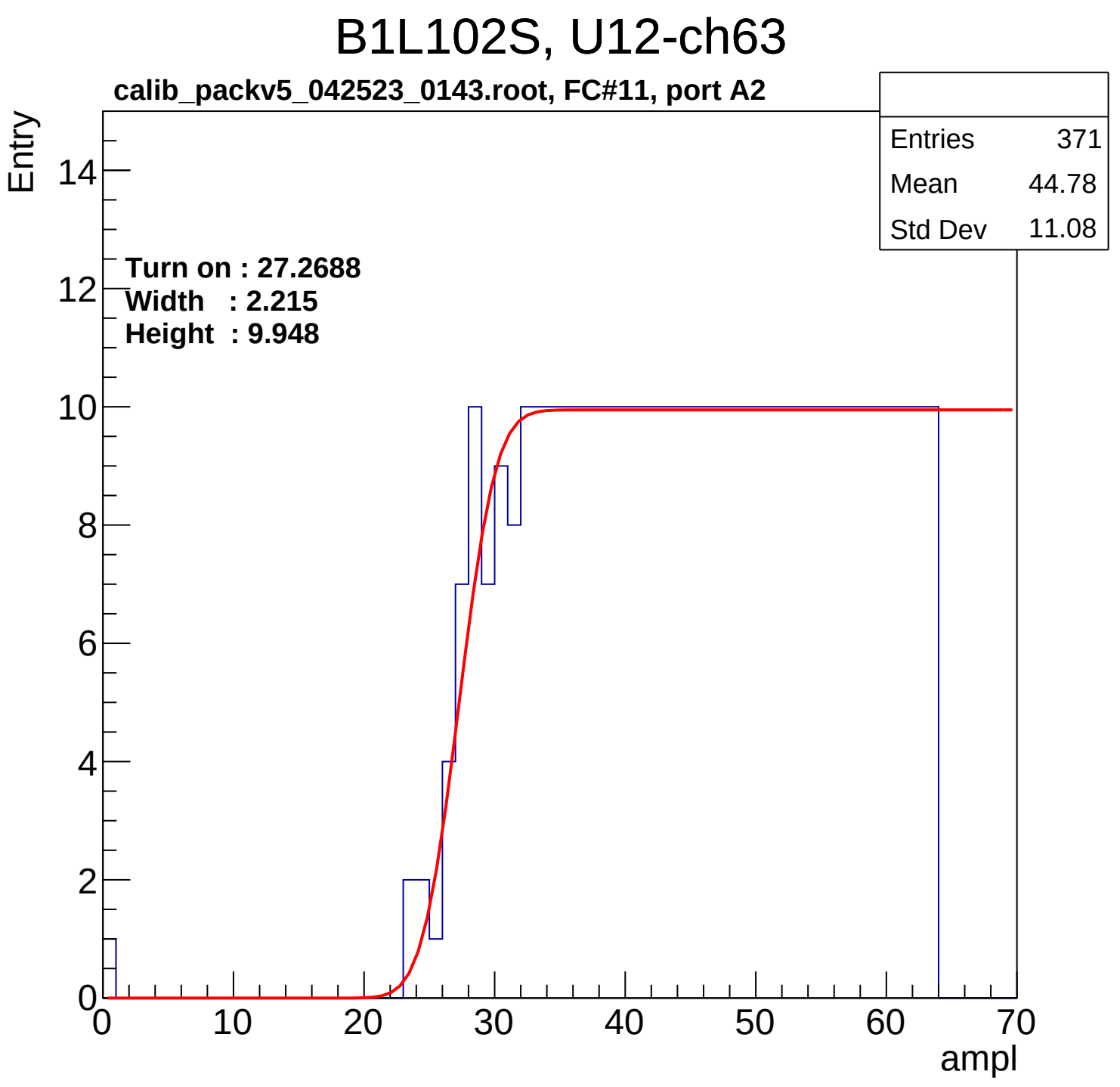
B1L102S, U12-ch63
calib_packv5_042523_0143.root, FC#11, port A2
Entries 371
Mean 44.78
Std Dev 11.08
Turn on : 27.2688
Width : 2.215
Height : 9.948
Entry
ampl
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2
4
6
8
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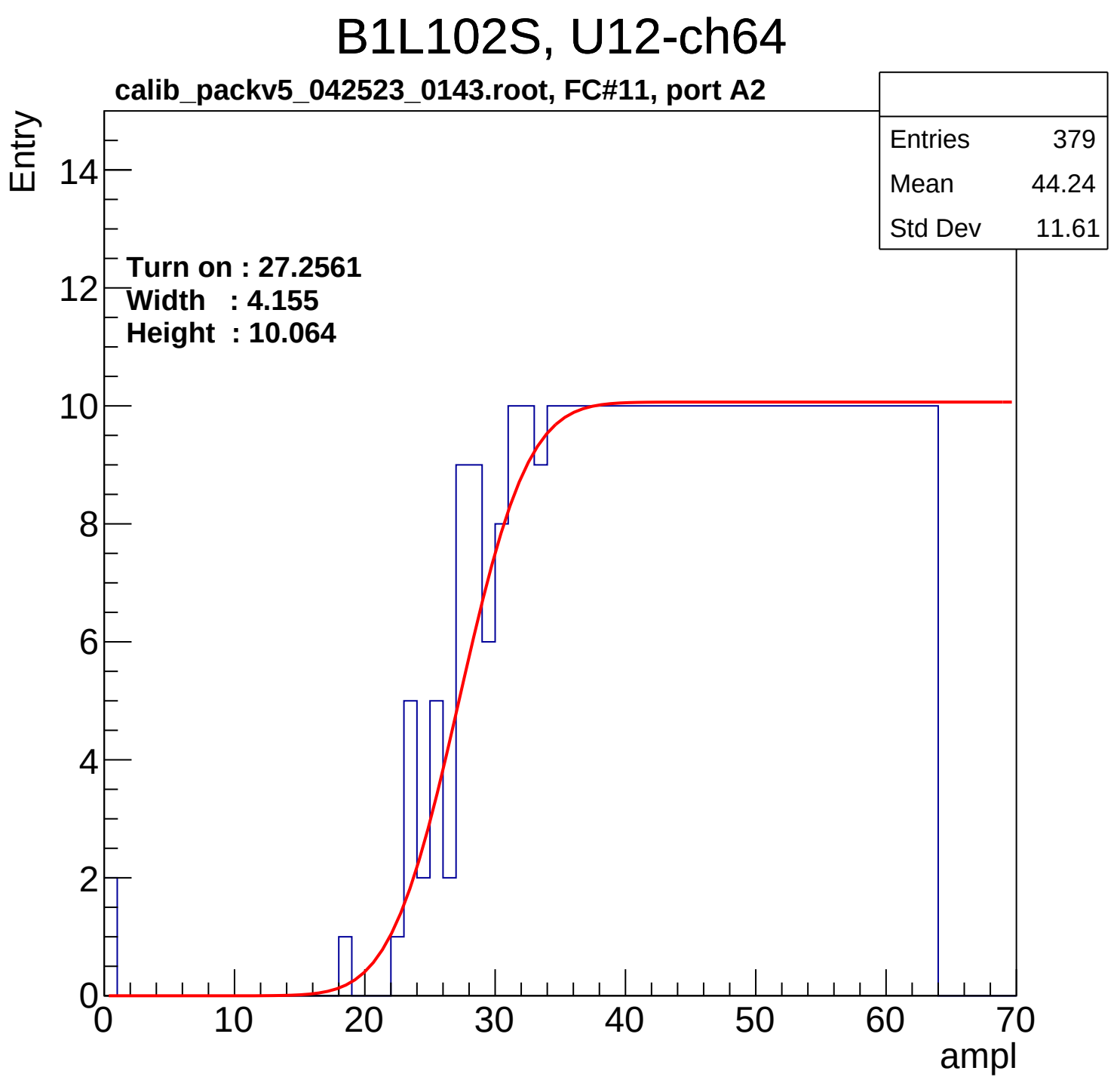
B1L102S, U12-ch64
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.24
Std Dev 11.61
Turn on : 27.2561
Width : 4.155
Height : 10.064
Entry
ampl
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8
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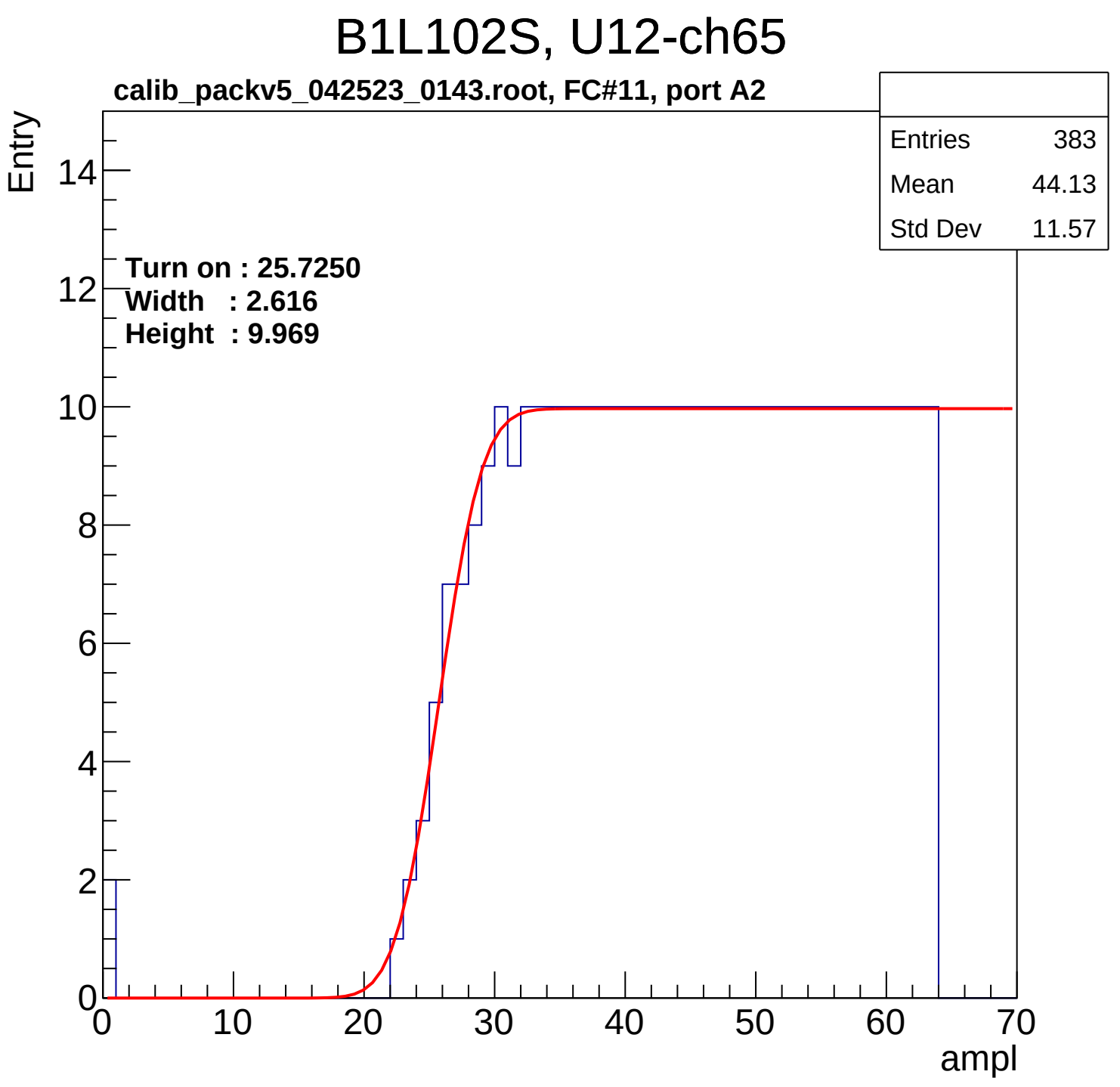
B1L102S, U12-ch65
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.13
Std Dev 11.57
Turn on : 25.7250
Width : 2.616
Height : 9.969
Entry
ampl
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2
4
6
8
10
12
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0
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60
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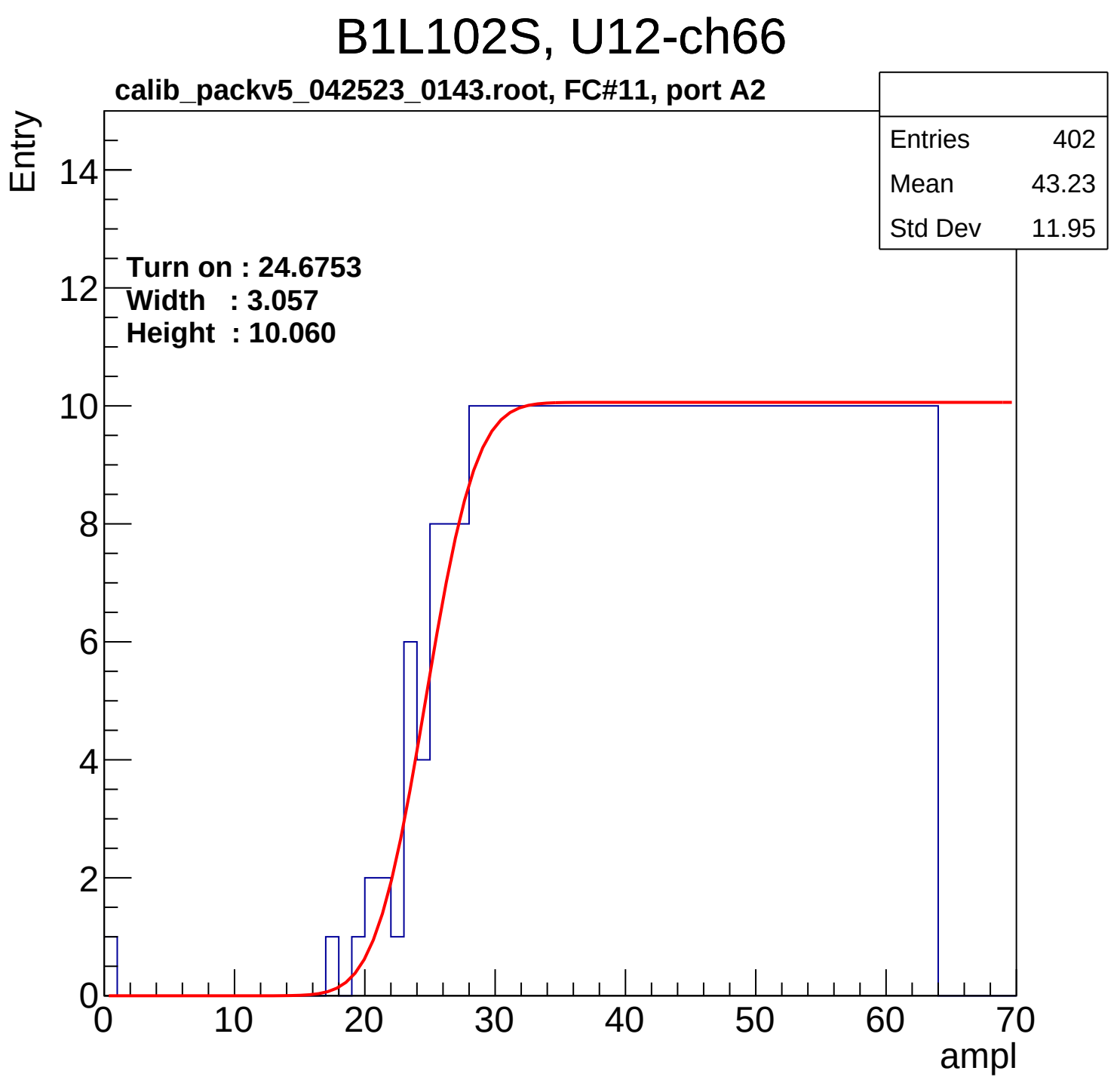
B1L102S, U12-ch66
calib_packv5_042523_0143.root, FC#11, port A2
Entries 402
Mean 43.23
Std Dev 11.95
Turn on : 24.6753
Width : 3.057
Height : 10.060
Entry
ampl
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8
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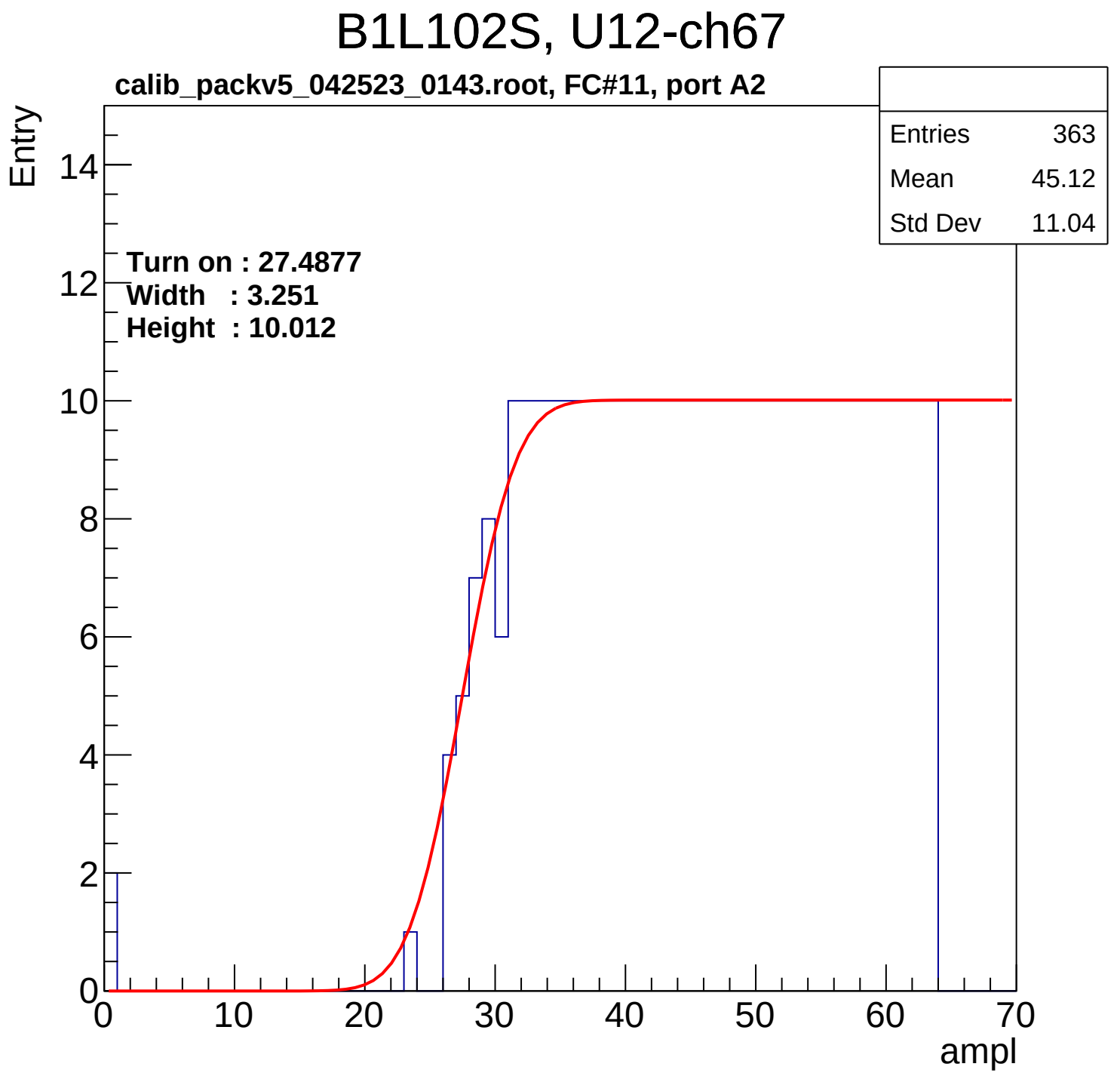
B1L102S, U12-ch67
calib_packv5_042523_0143.root, FC#11, port A2
Entries 363
Mean 45.12
Std Dev 11.04
Turn on : 27.4877
Width : 3.251
Height : 10.012
Entry
ampl
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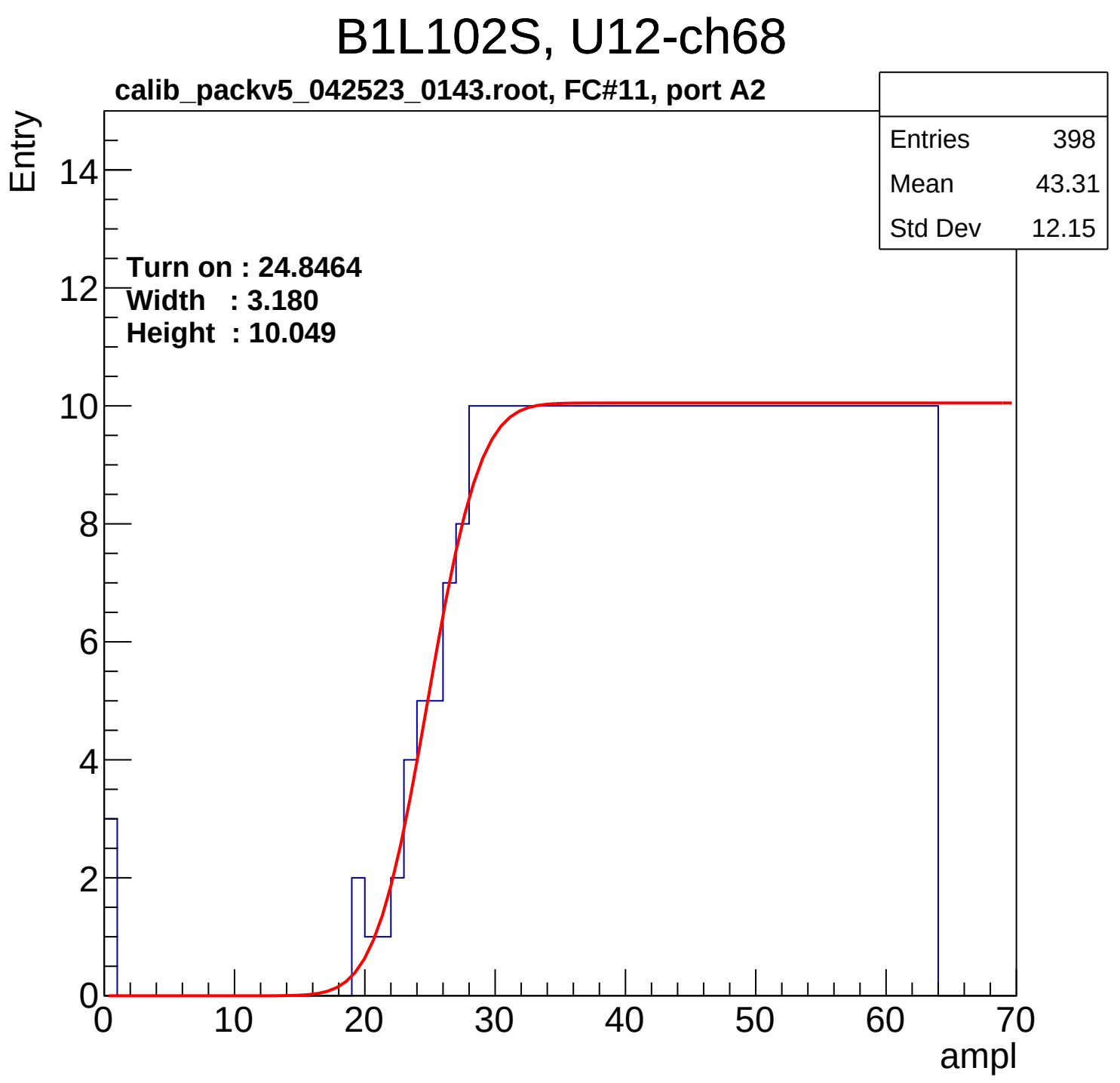
B1L102S, U12-ch68
calib_packv5_042523_0143.root, FC#11, port A2
Entries 398
Mean 43.31
Std Dev 12.15
Turn on : 24.8464
Width : 3.180
Height : 10.049
Entry
ampl
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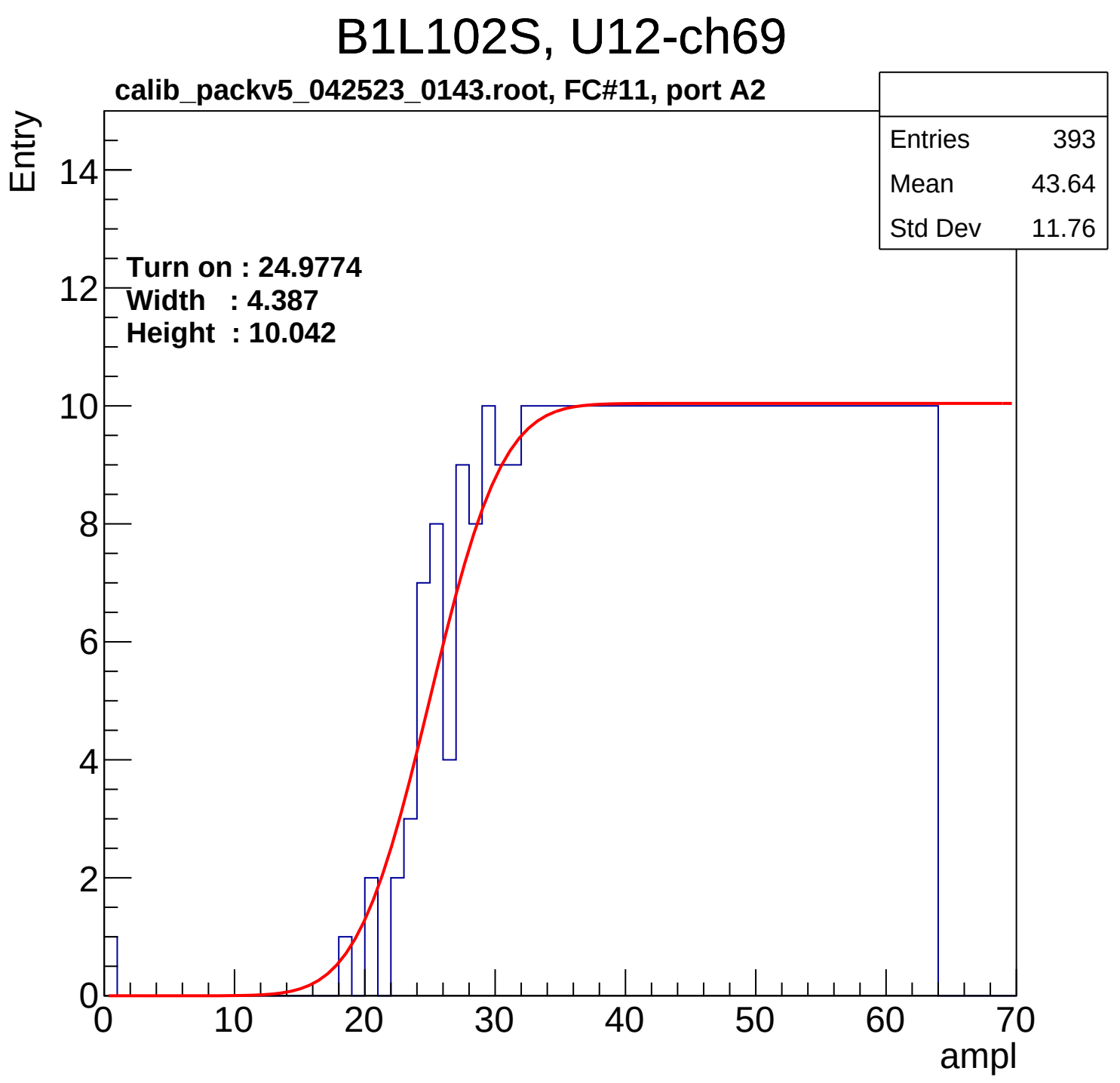
B1L102S, U12-ch69
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.64
Std Dev 11.76
Turn on : 24.9774
Width : 4.387
Height : 10.042
Entry
ampl
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4
6
8
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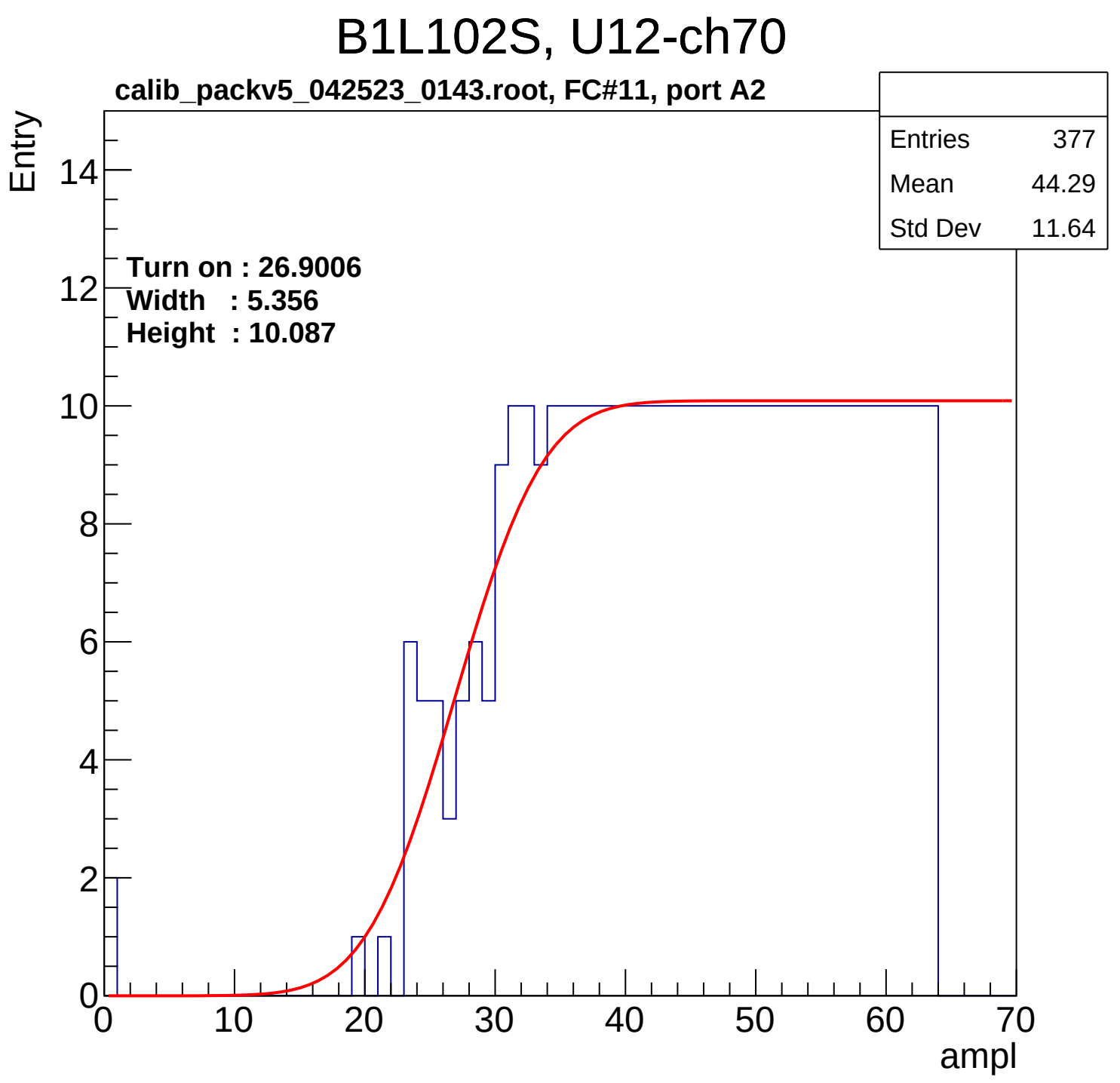
B1L102S, U12-ch70
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.29
Std Dev 11.64
Turn on : 26.9006
Width : 5.356
Height : 10.087
Entry
ampl
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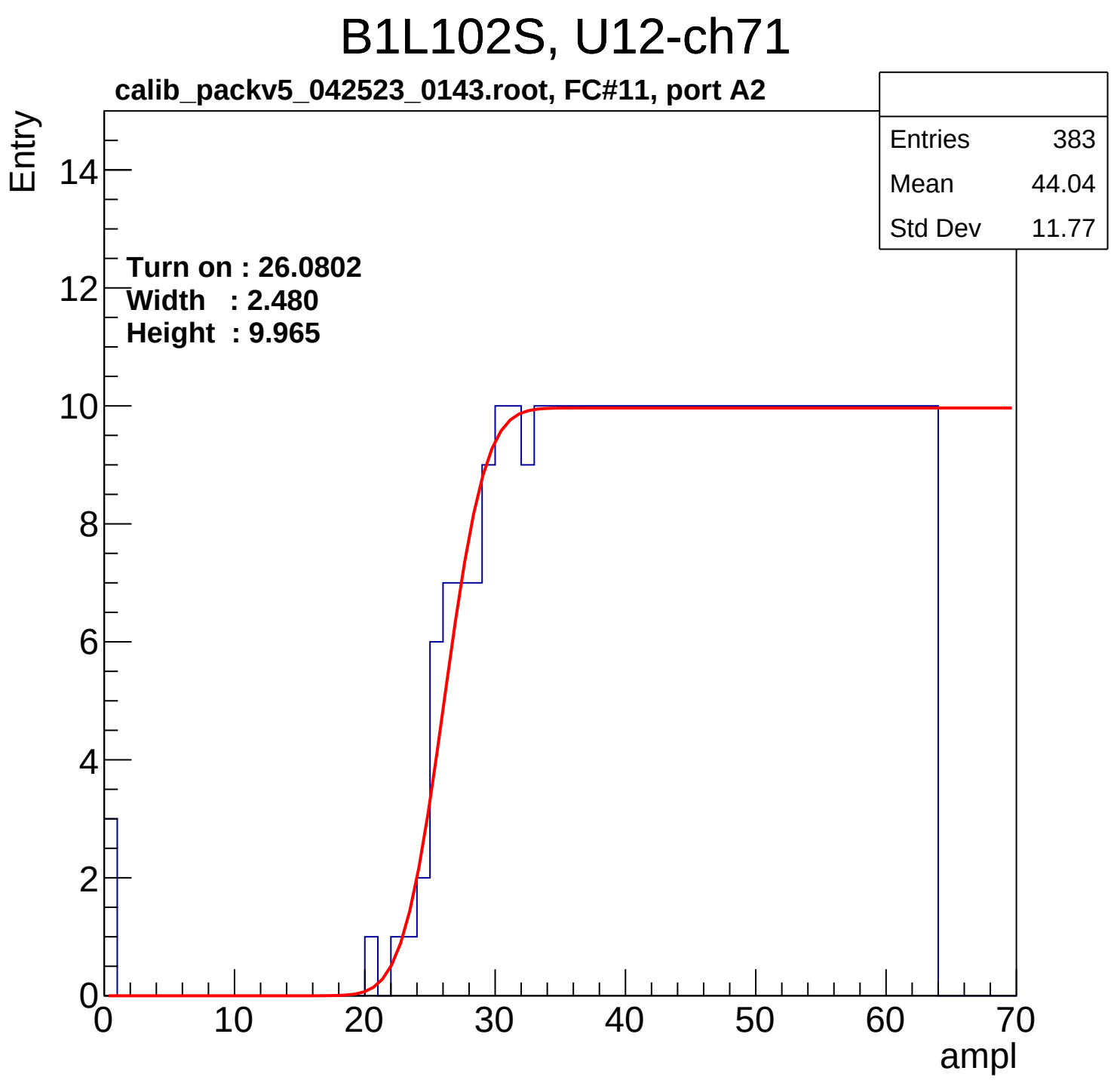
B1L102S, U12-ch71
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.04
Std Dev 11.77
Turn on : 26.0802
Width : 2.480
Height : 9.965
Entry
ampl
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6
8
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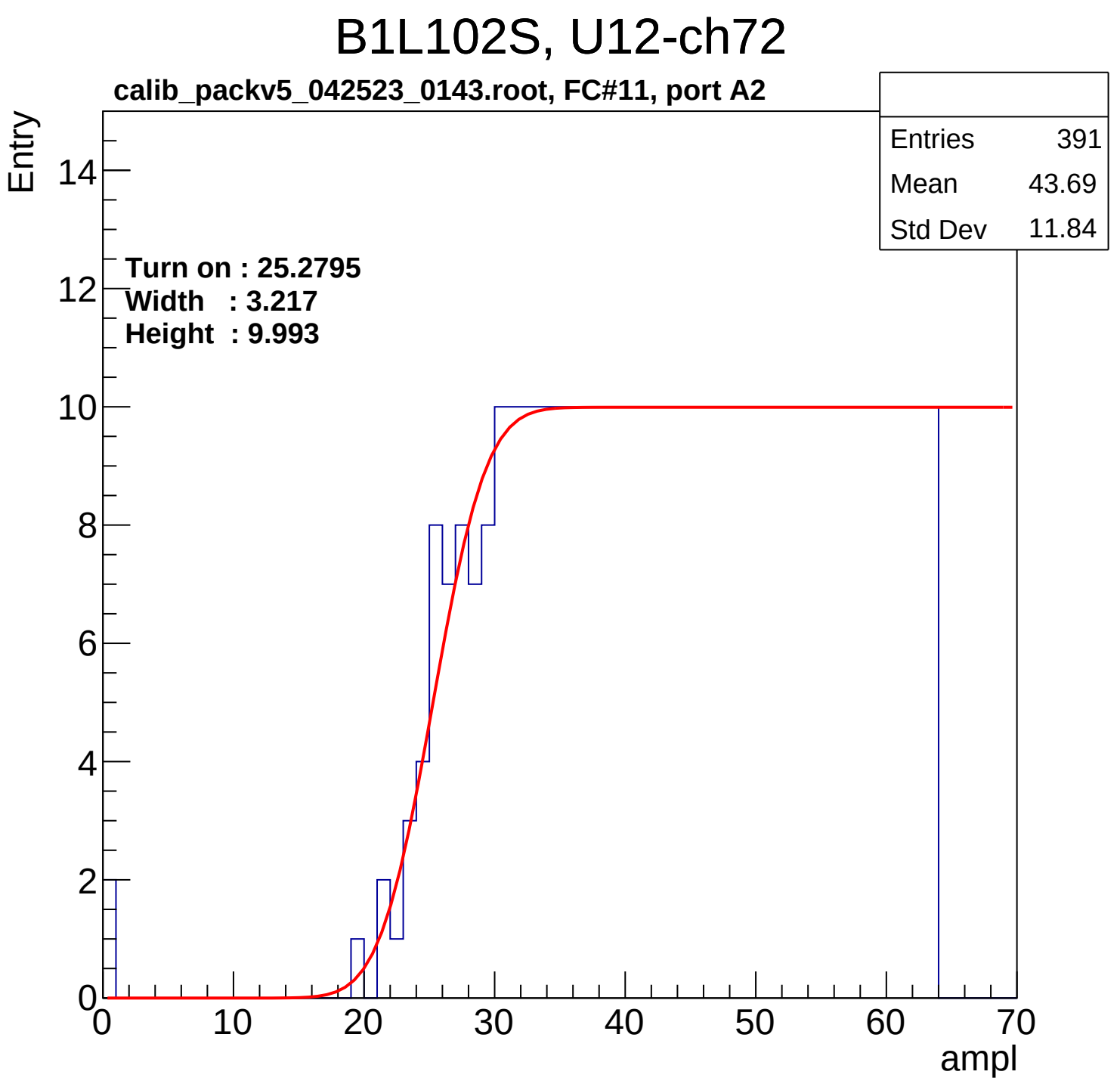
B1L102S, U12-ch72
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.69
Std Dev 11.84
Turn on : 25.2795
Width : 3.217
Height : 9.993
Entry
ampl
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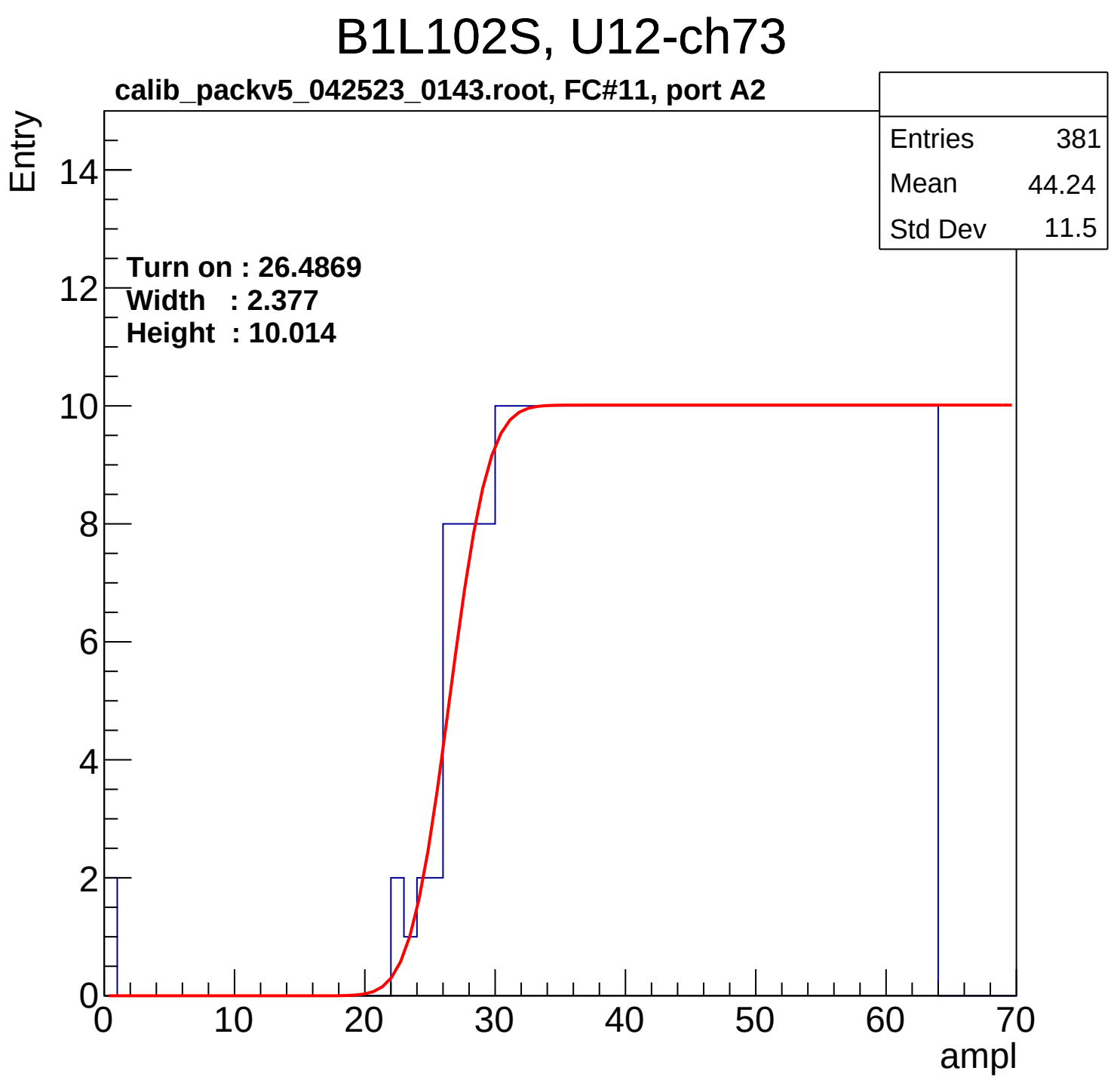
B1L102S, U12-ch73
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.24
Std Dev 11.5
Turn on : 26.4869
Width : 2.377
Height : 10.014
Entry
ampl
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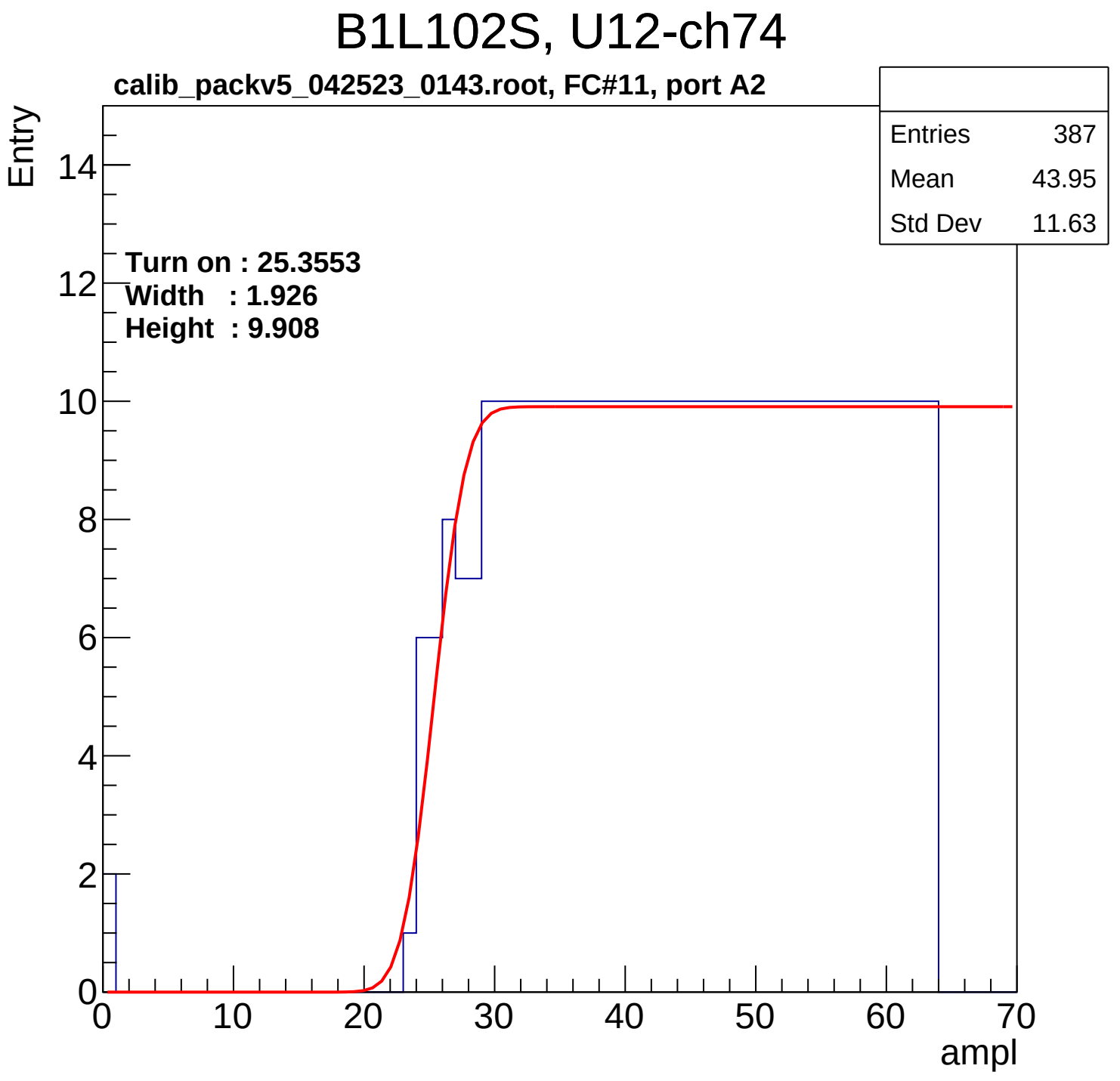
B1L102S, U12-ch74
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.95
Std Dev 11.63
Turn on : 25.3553
Width : 1.926
Height : 9.908
Entry
ampl
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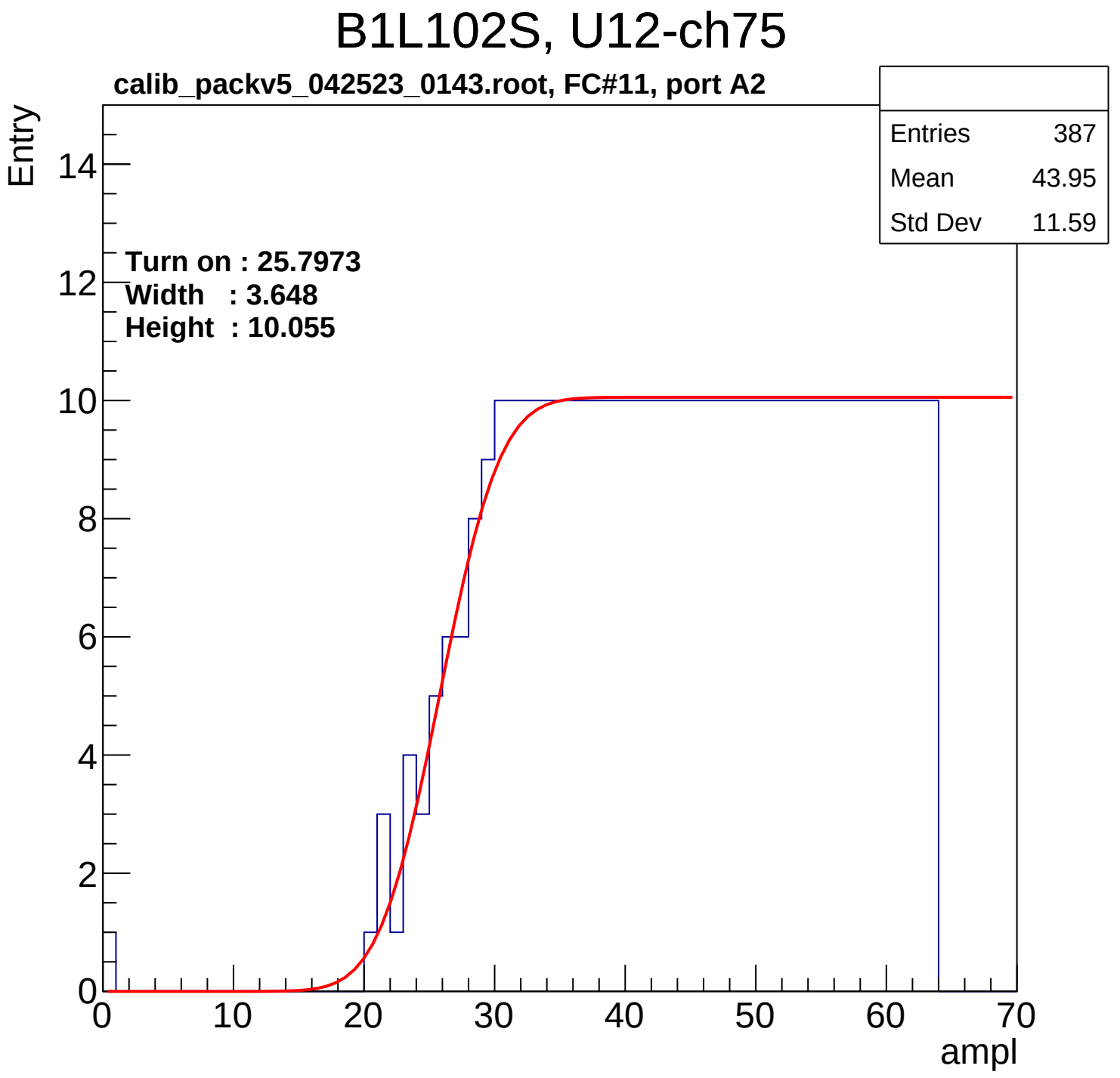
B1L102S, U12-ch75
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.95
Std Dev 11.59
Turn on : 25.7973
Width : 3.648
Height : 10.055
Entry
ampl
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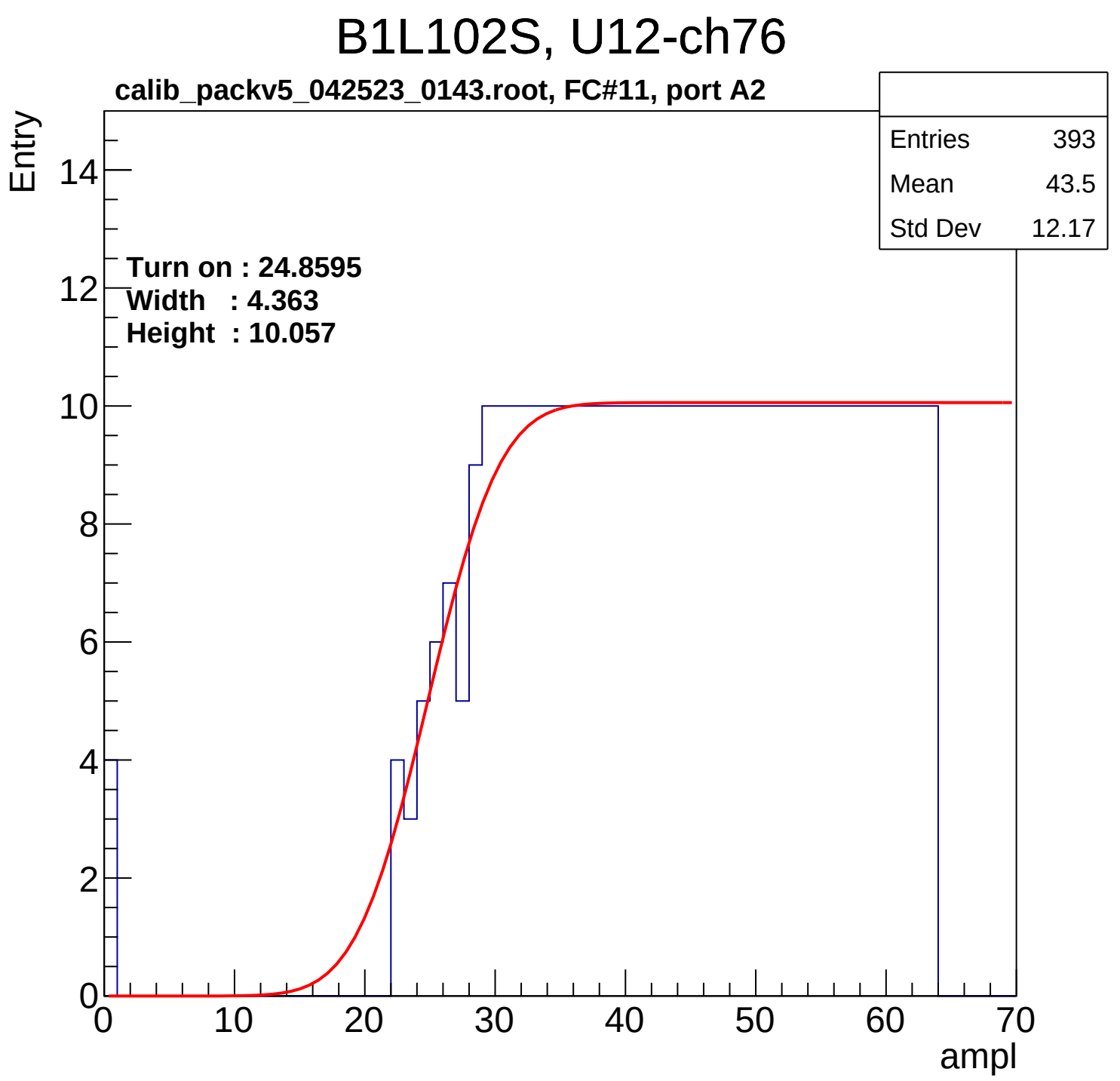
B1L102S, U12-ch76
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.5
Std Dev 12.17
Turn on : 24.8595
Width : 4.363
Height : 10.057
Entry
ampl
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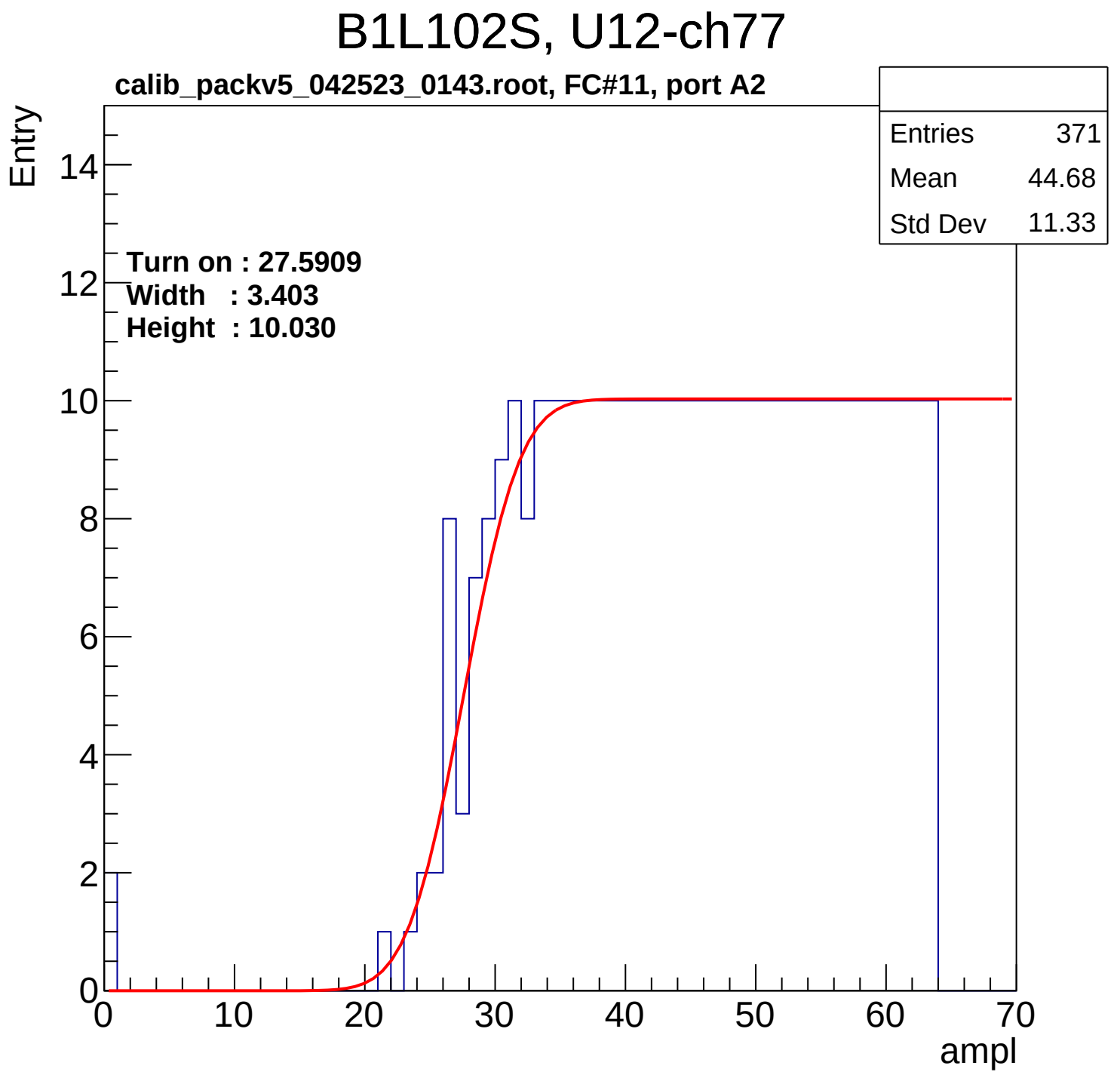
B1L102S, U12-ch77
calib_packv5_042523_0143.root, FC#11, port A2
Entries 371
Mean 44.68
Std Dev 11.33
Turn on : 27.5909
Width : 3.403
Height : 10.030
Entry
ampl
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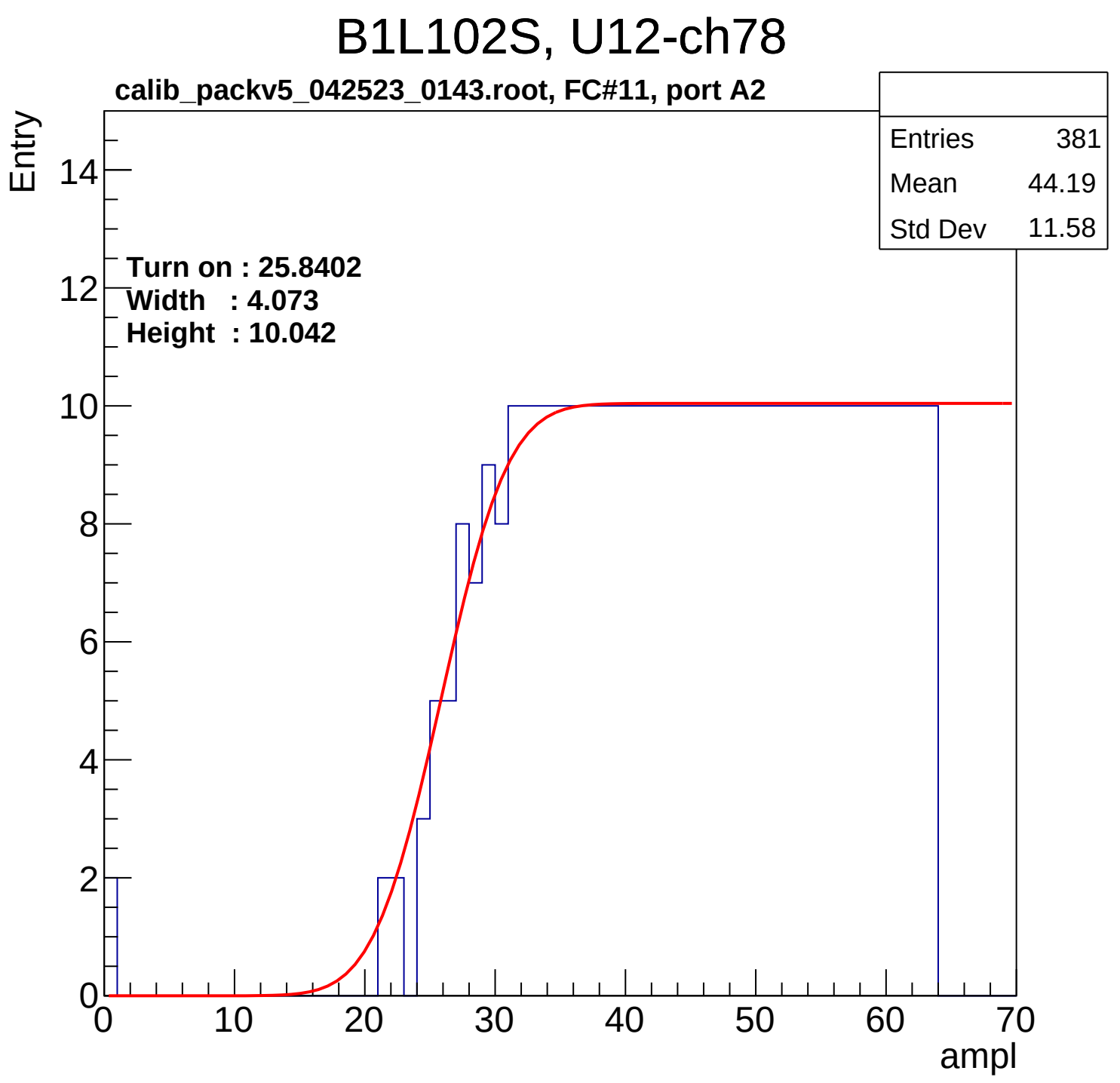
B1L102S, U12-ch78
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.19
Std Dev 11.58
Turn on : 25.8402
Width : 4.073
Height : 10.042
Entry
ampl
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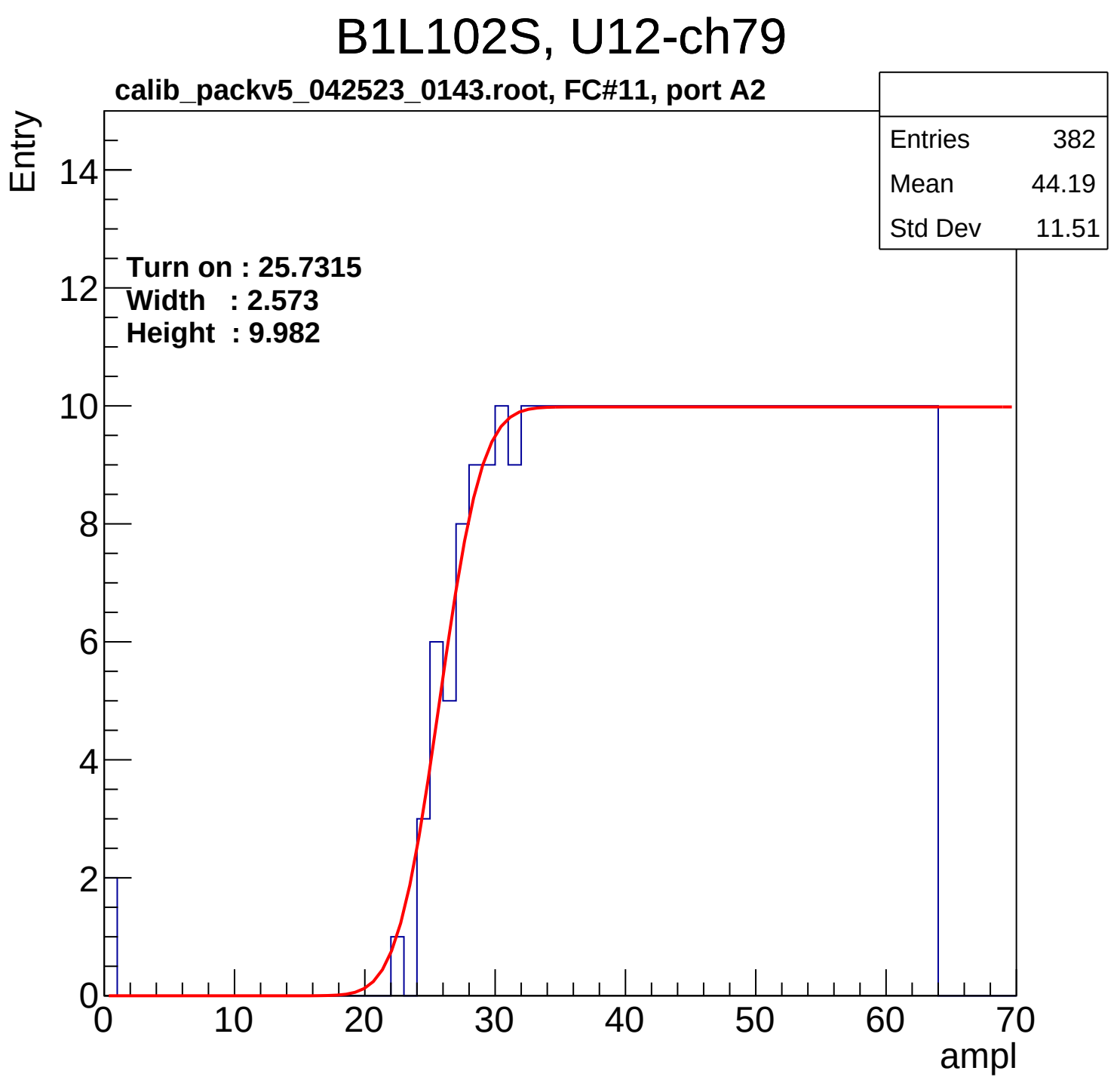
B1L102S, U12-ch79
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.19
Std Dev 11.51
Turn on : 25.7315
Width : 2.573
Height : 9.982
Entry
ampl
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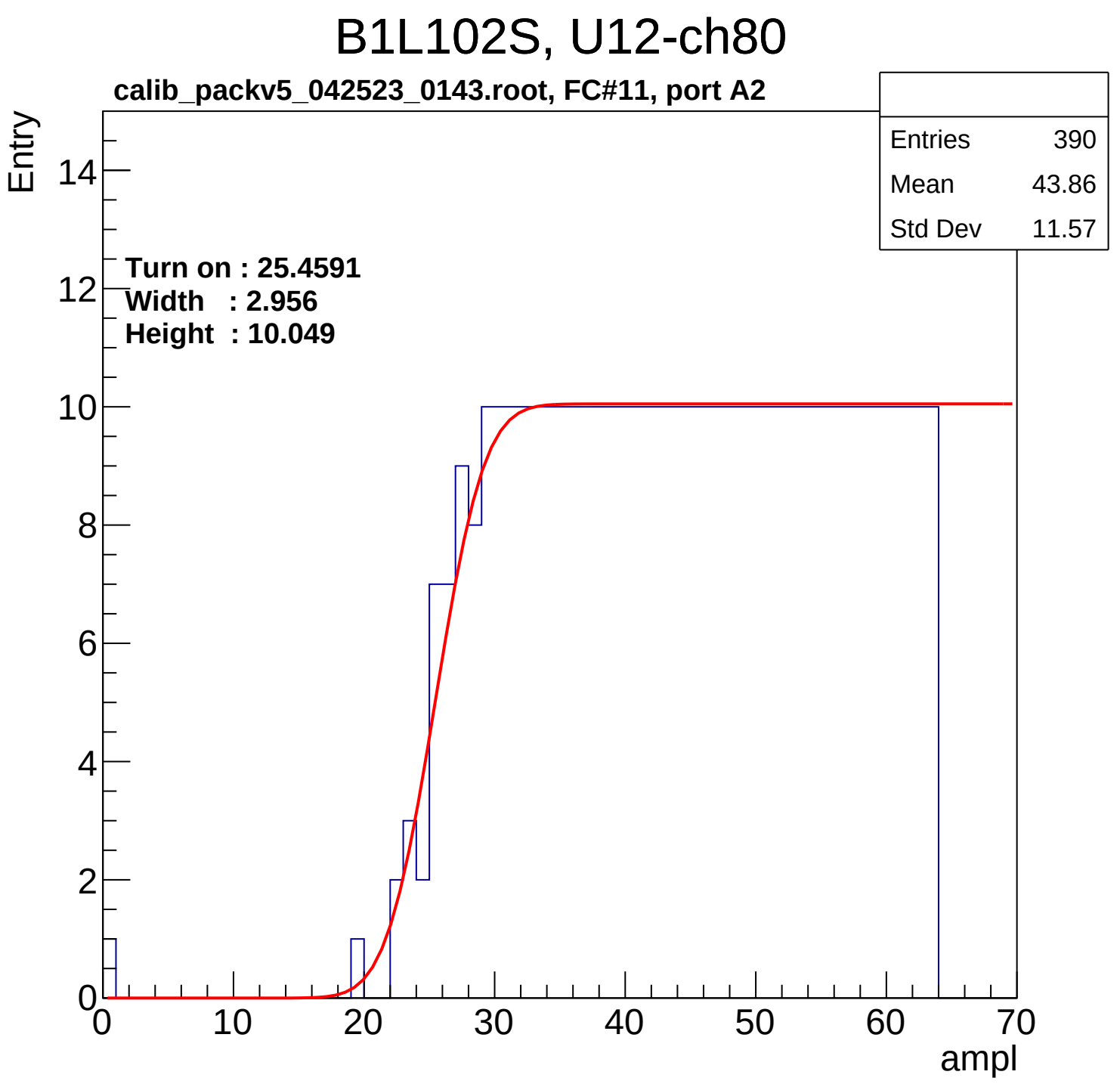
B1L102S, U12-ch80
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.86
Std Dev 11.57
Turn on : 25.4591
Width : 2.956
Height : 10.049
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ampl
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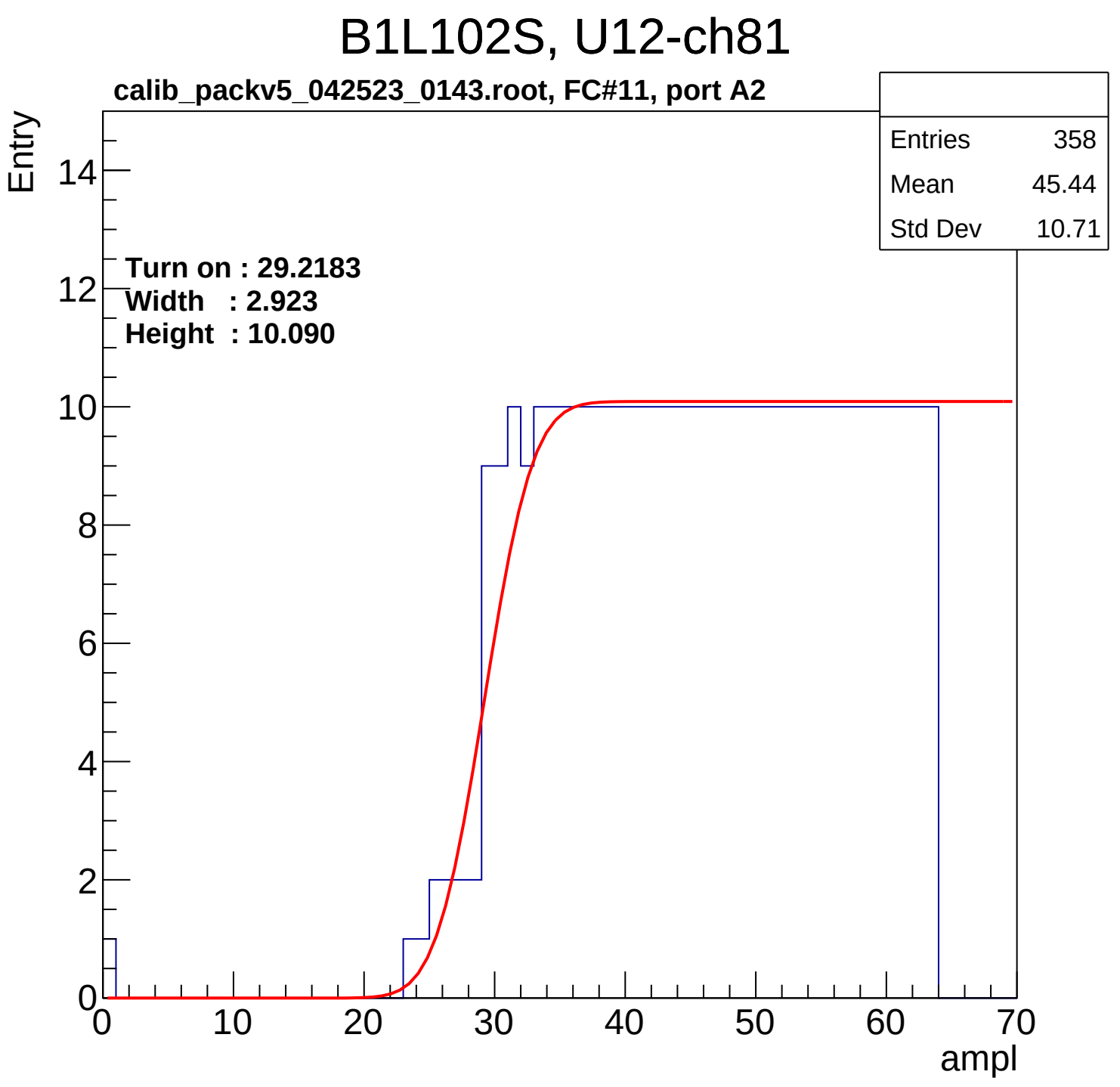
B1L102S, U12-ch81
calib_packv5_042523_0143.root, FC#11, port A2
Entries 358
Mean 45.44
Std Dev 10.71
Turn on : 29.2183
Width : 2.923
Height : 10.090
Entry
ampl
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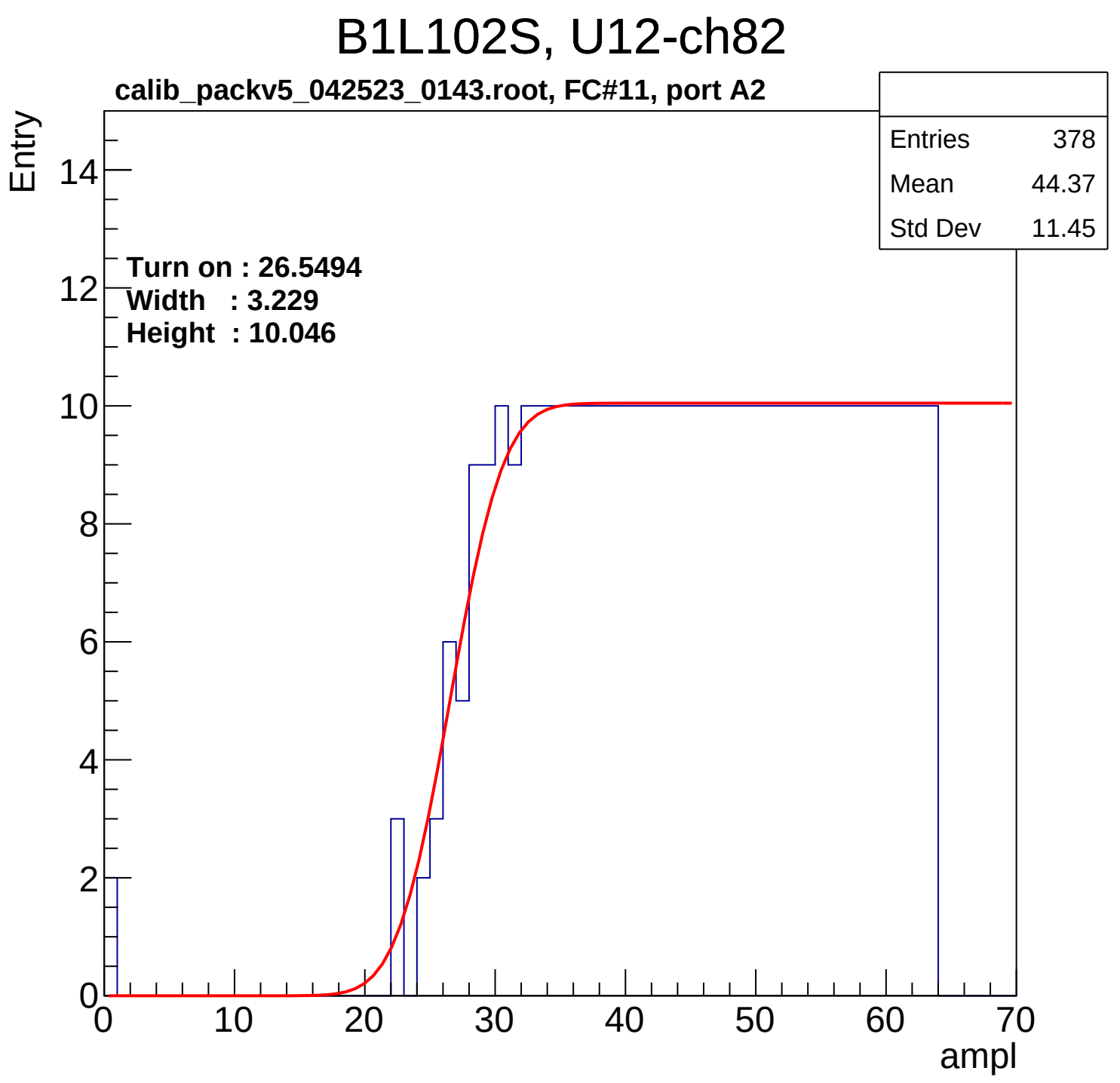
B1L102S, U12-ch82
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.37
Std Dev 11.45
Turn on : 26.5494
Width : 3.229
Height : 10.046
Entry
ampl
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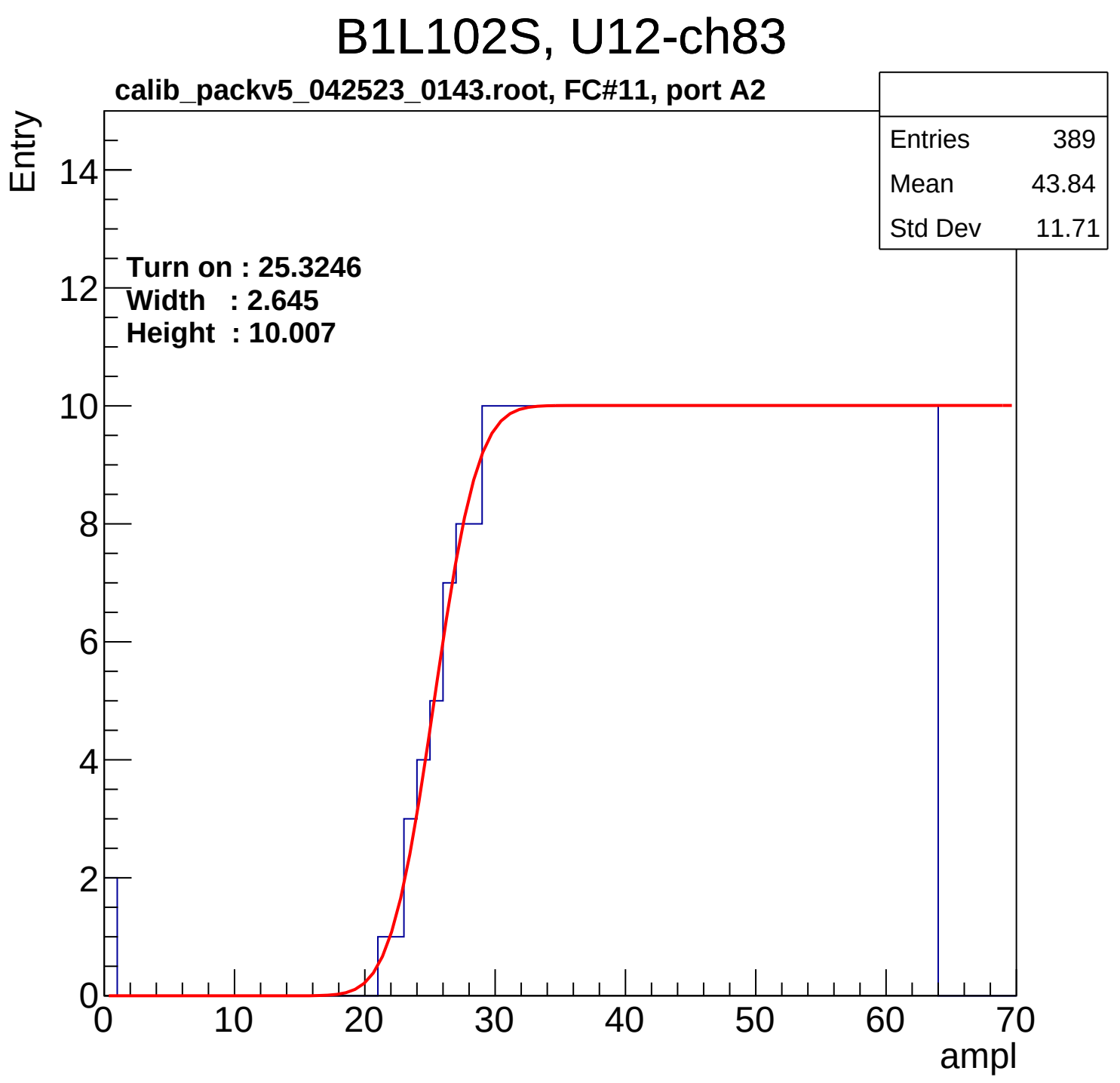
B1L102S, U12-ch83
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.84
Std Dev 11.71
Turn on : 25.3246
Width : 2.645
Height : 10.007
Entry
ampl
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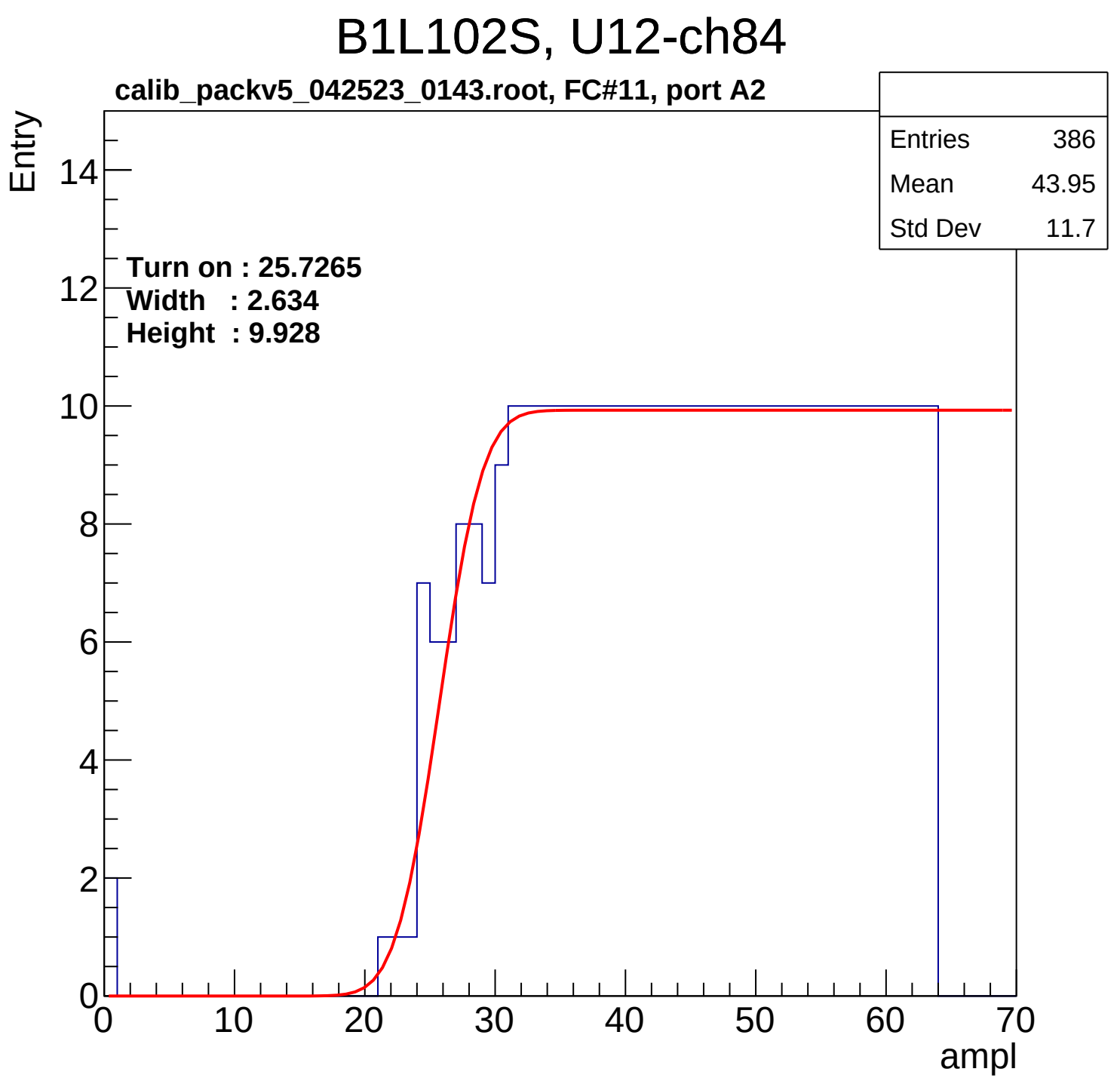
B1L102S, U12-ch84
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.95
Std Dev 11.7
Turn on : 25.7265
Width : 2.634
Height : 9.928
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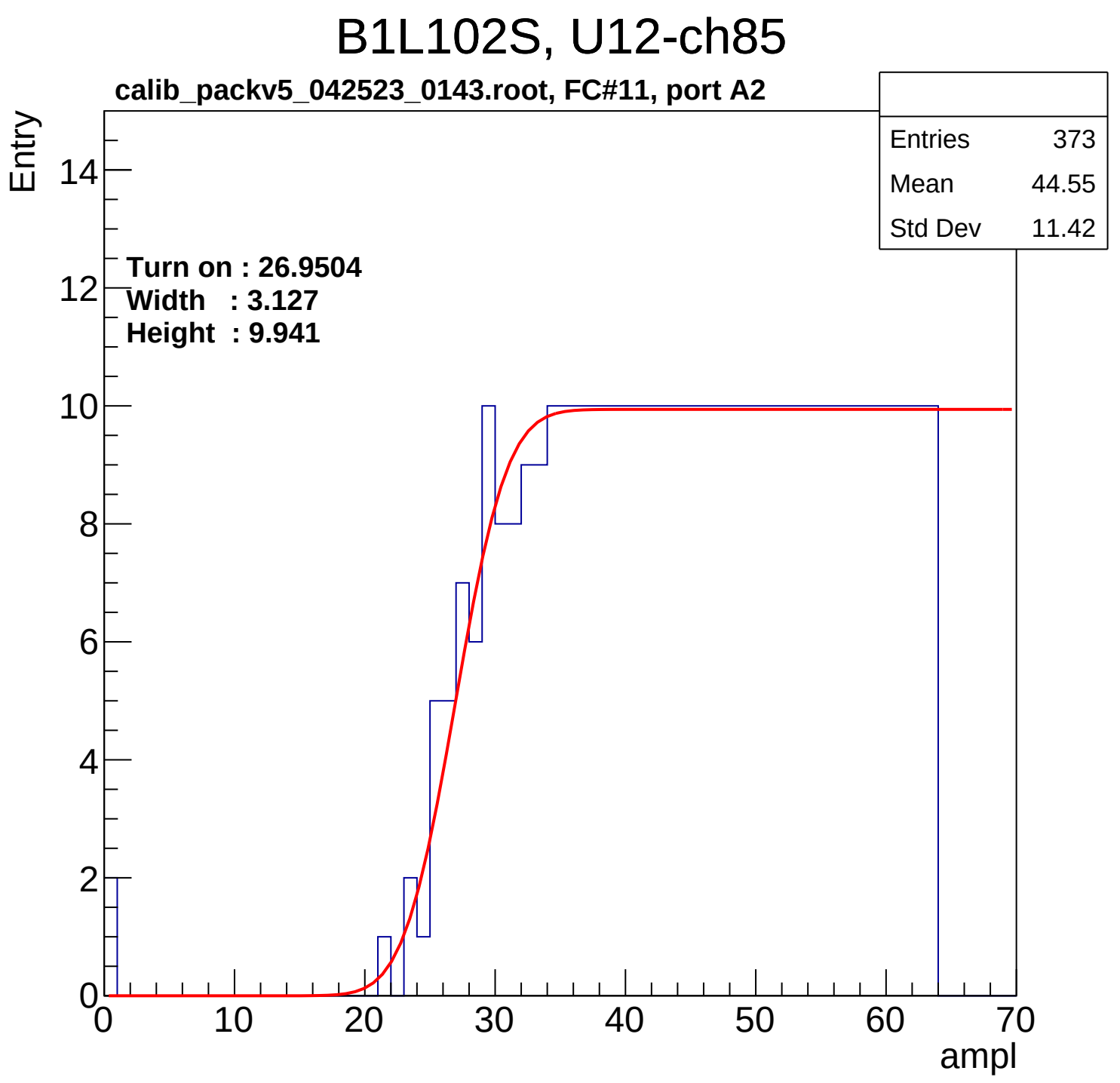
B1L102S, U12-ch85
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.55
Std Dev 11.42
Turn on : 26.9504
Width : 3.127
Height : 9.941
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ampl
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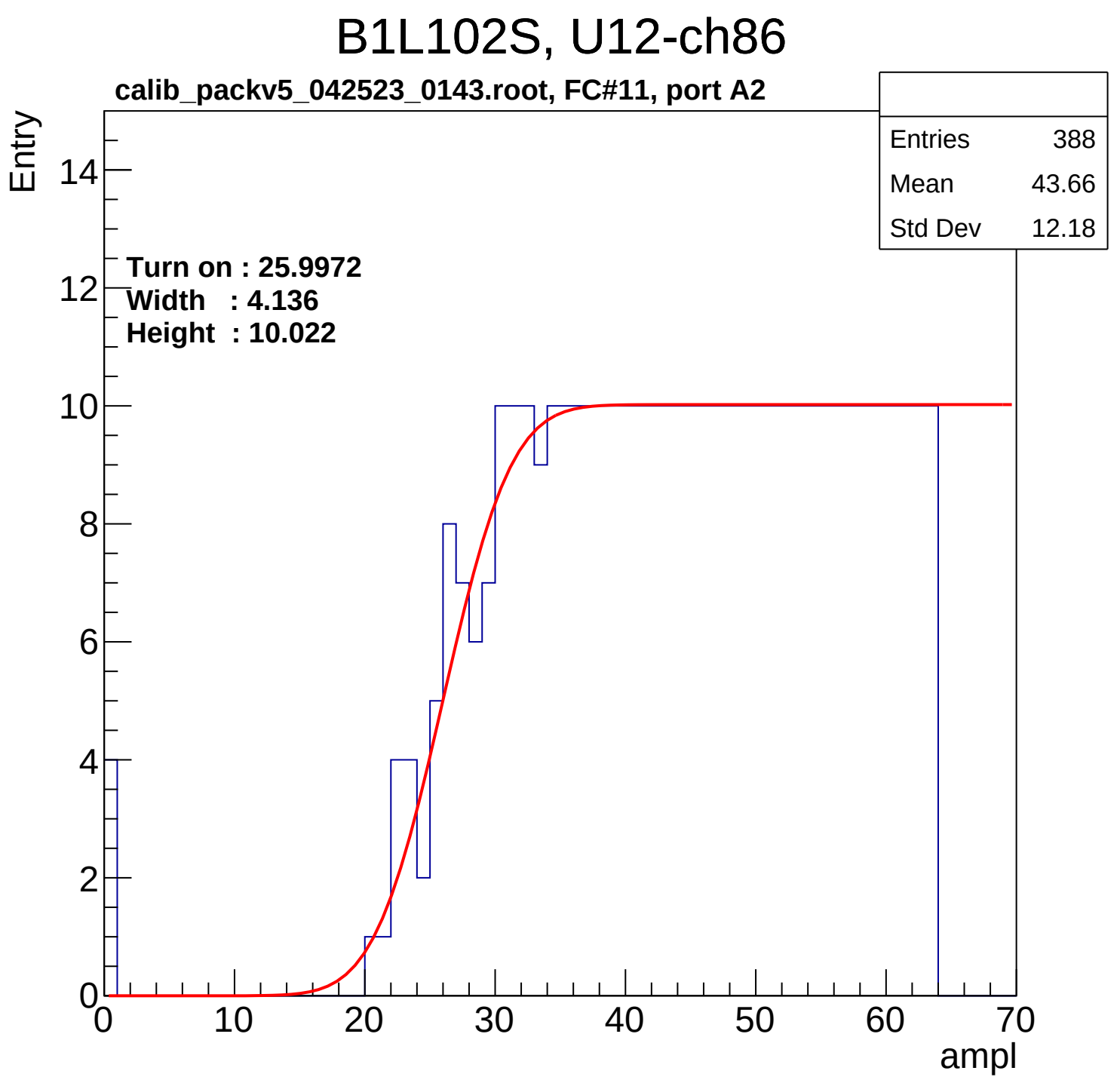
B1L102S, U12-ch86
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.66
Std Dev 12.18
Turn on : 25.9972
Width : 4.136
Height : 10.022
Entry
ampl
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6
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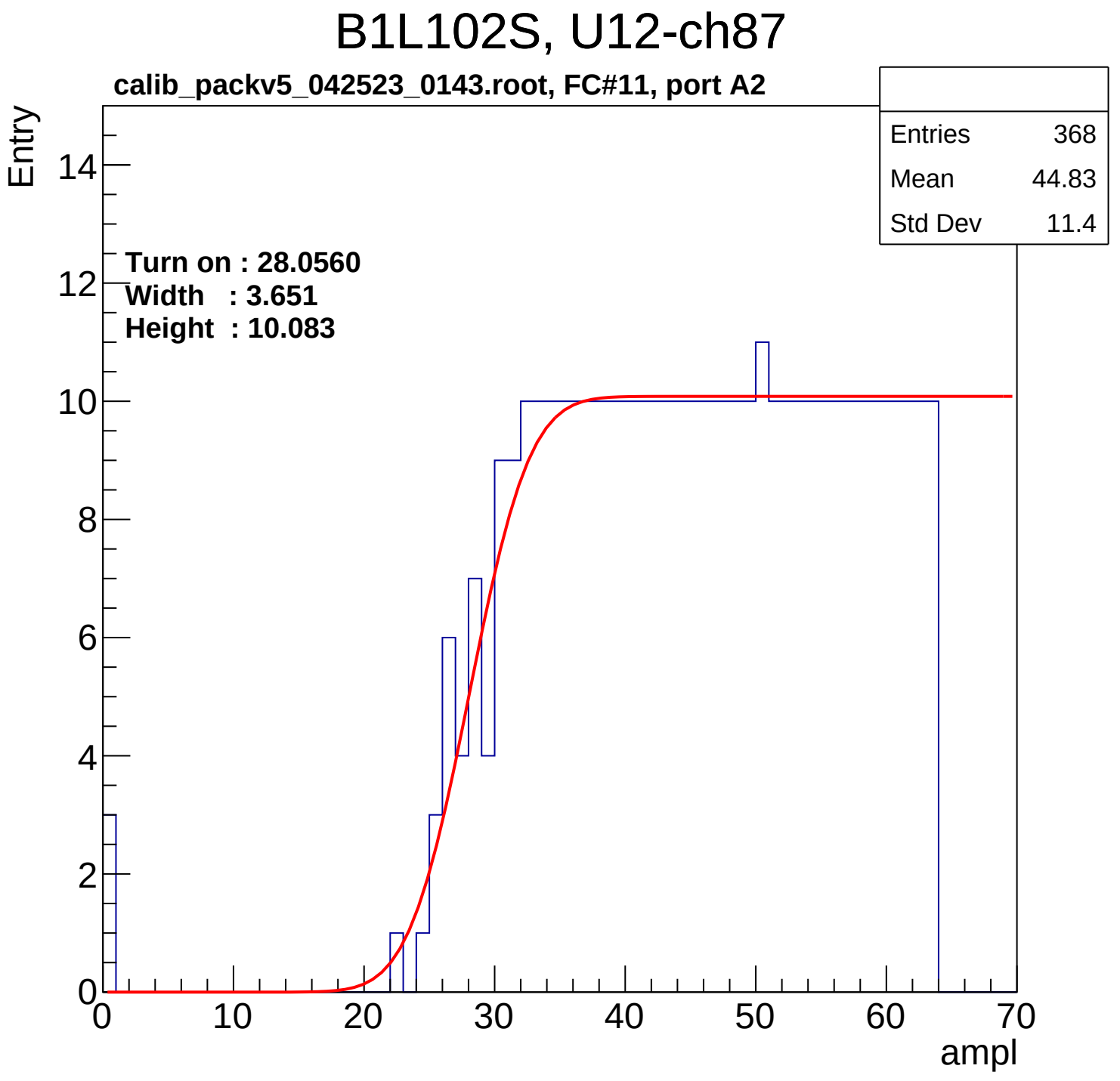
B1L102S, U12-ch87
calib_packv5_042523_0143.root, FC#11, port A2
Entries 368
Mean 44.83
Std Dev 11.4
Turn on : 28.0560
Width : 3.651
Height : 10.083
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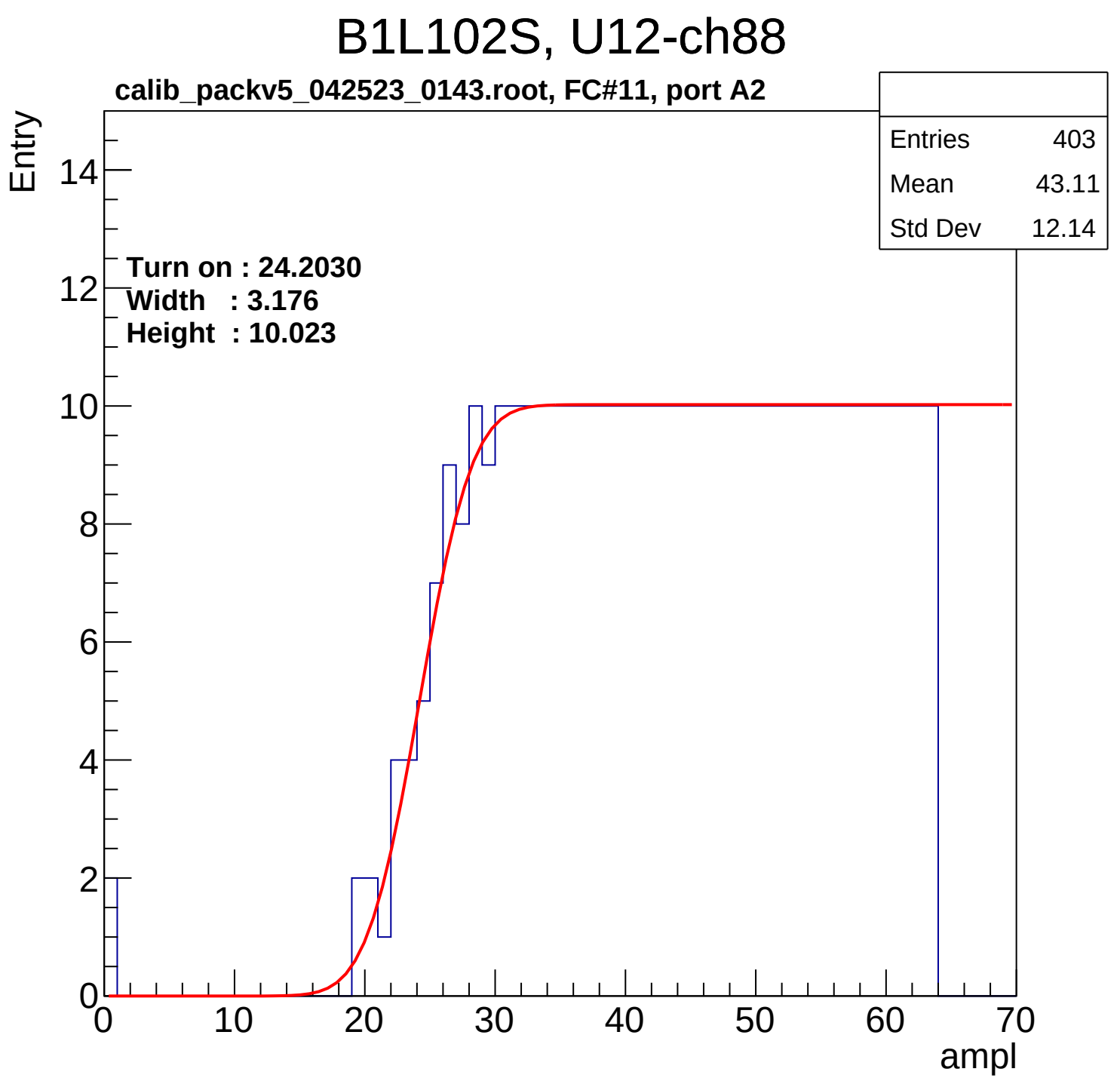
B1L102S, U12-ch88
calib_packv5_042523_0143.root, FC#11, port A2
Entries 403
Mean 43.11
Std Dev 12.14
Turn on : 24.2030
Width : 3.176
Height : 10.023
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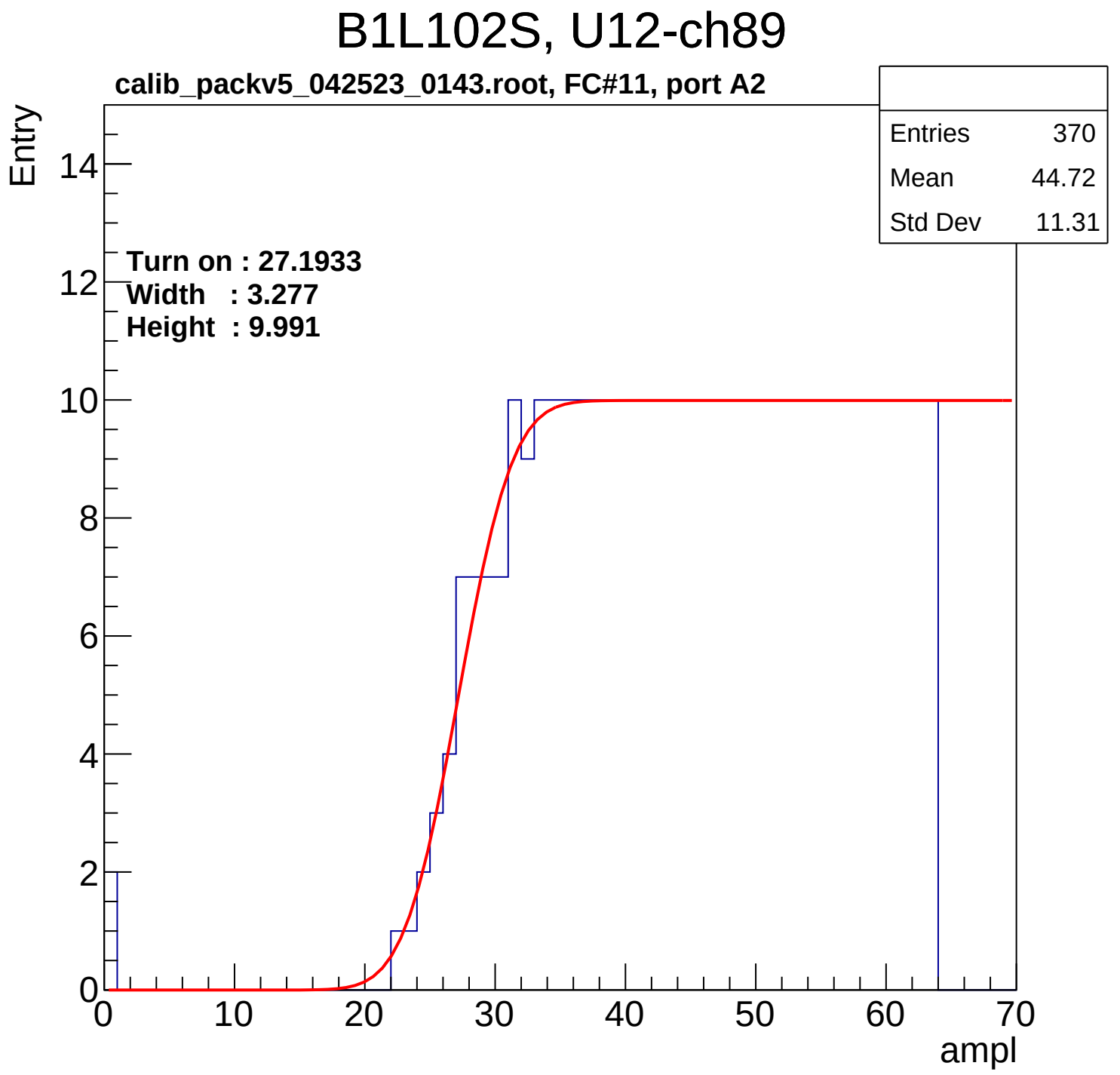
B1L102S, U12-ch89
calib_packv5_042523_0143.root, FC#11, port A2
Entries 370
Mean 44.72
Std Dev 11.31
Turn on : 27.1933
Width : 3.277
Height : 9.991
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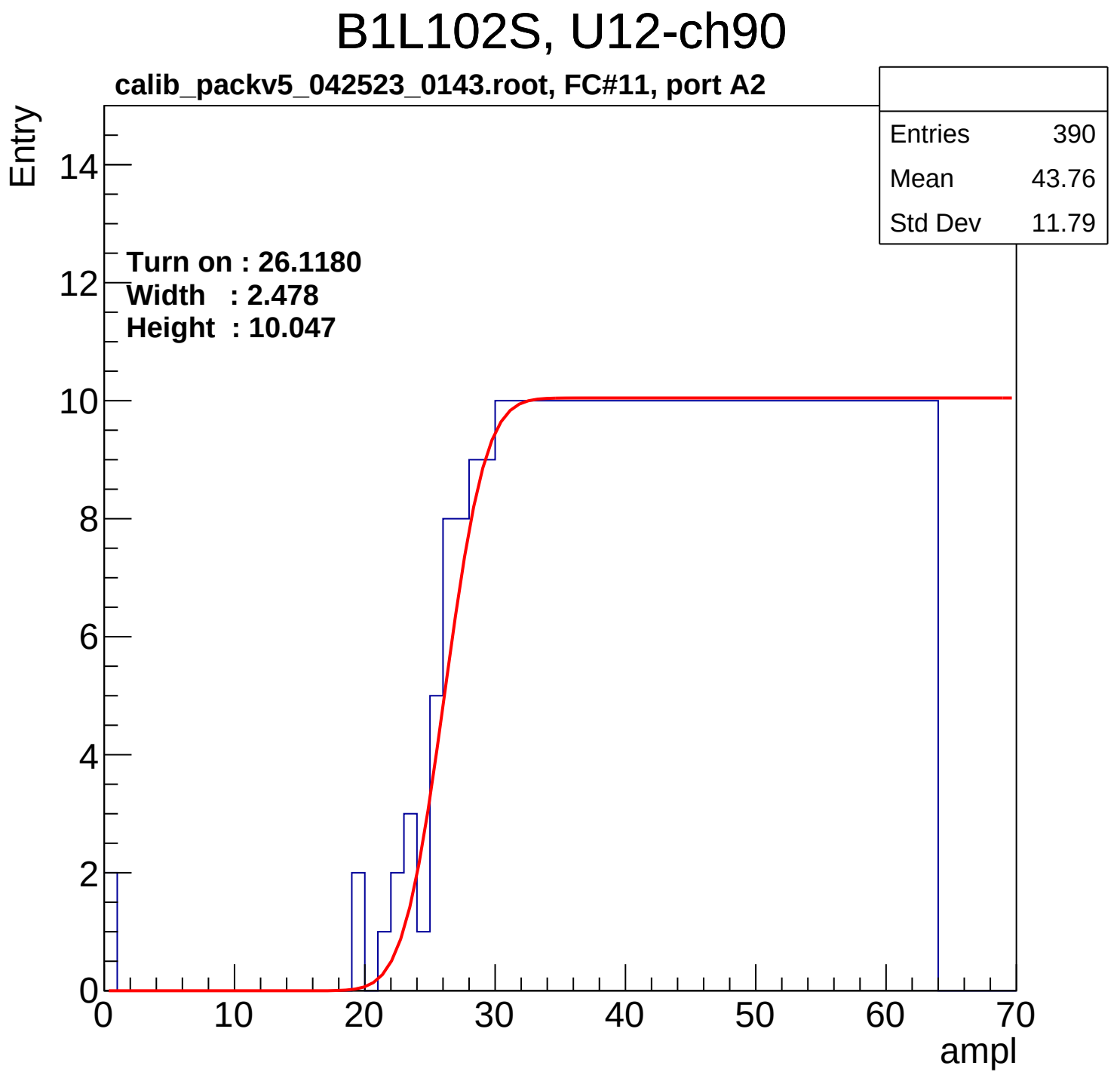
B1L102S, U12-ch90
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.76
Std Dev 11.79
Turn on : 26.1180
Width : 2.478
Height : 10.047
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ampl
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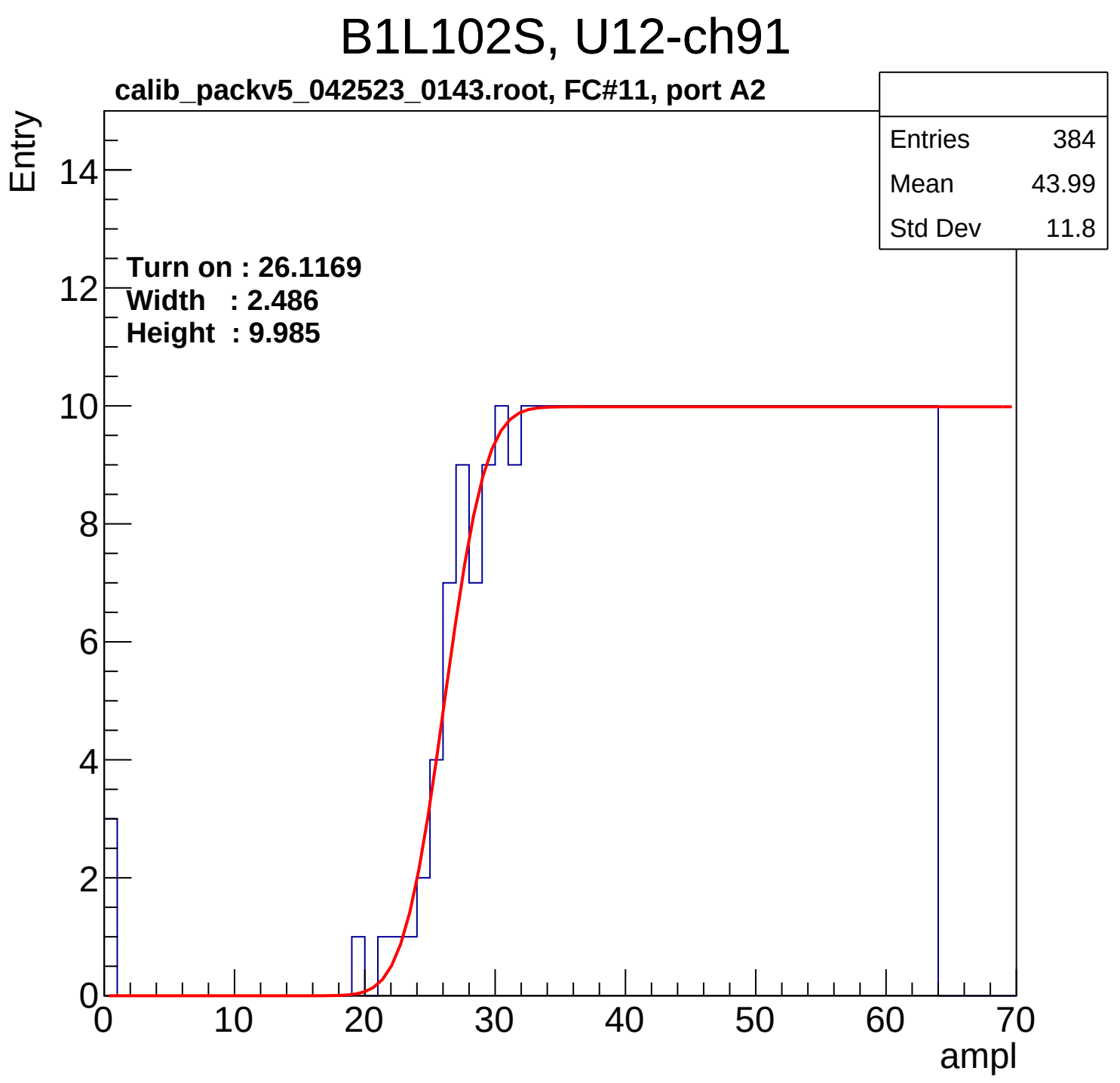
B1L102S, U12-ch91
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 43.99
Std Dev 11.8
Turn on : 26.1169
Width : 2.486
Height : 9.985
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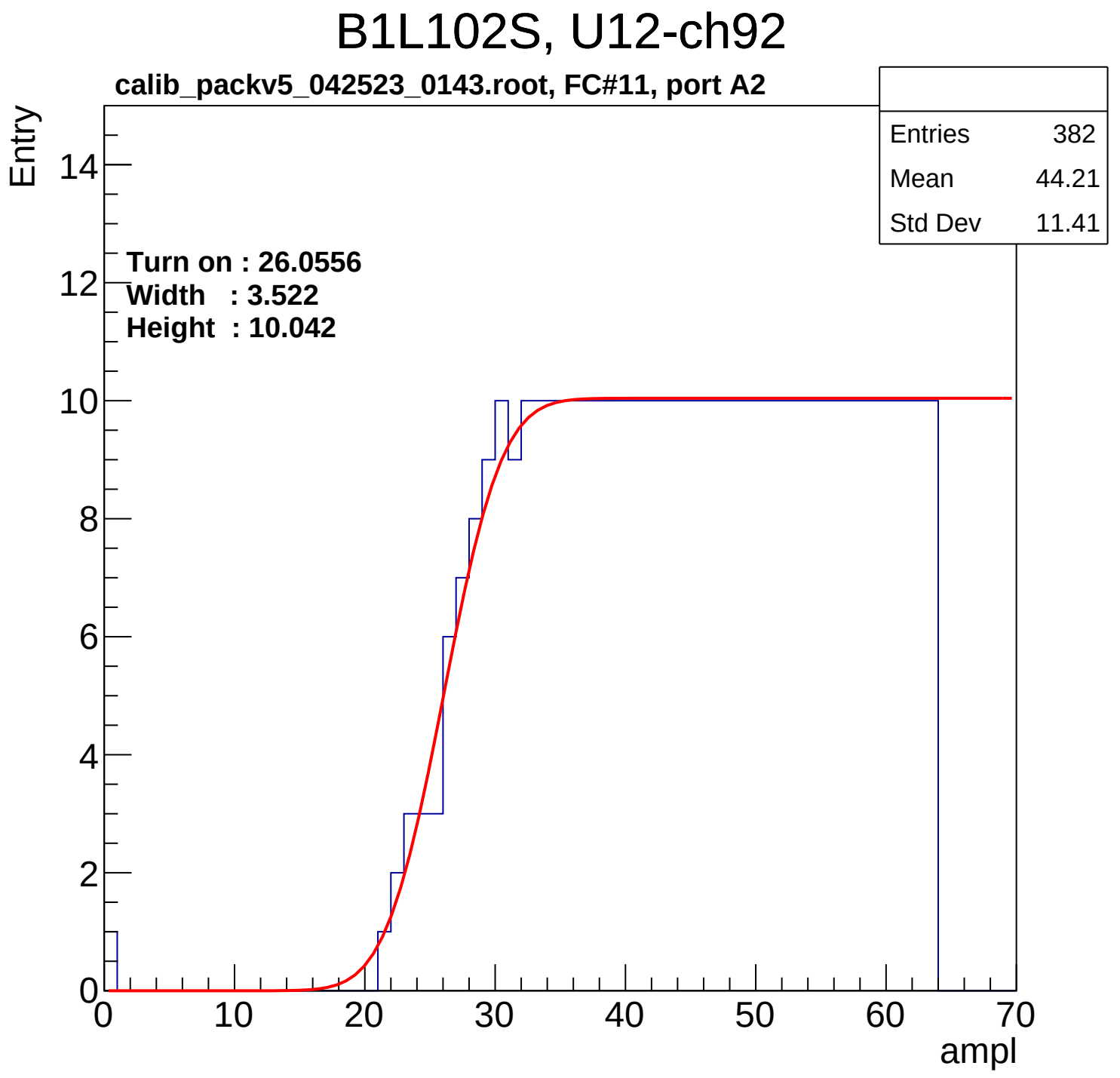
B1L102S, U12-ch92
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.21
Std Dev 11.41
Turn on : 26.0556
Width : 3.522
Height : 10.042
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ampl
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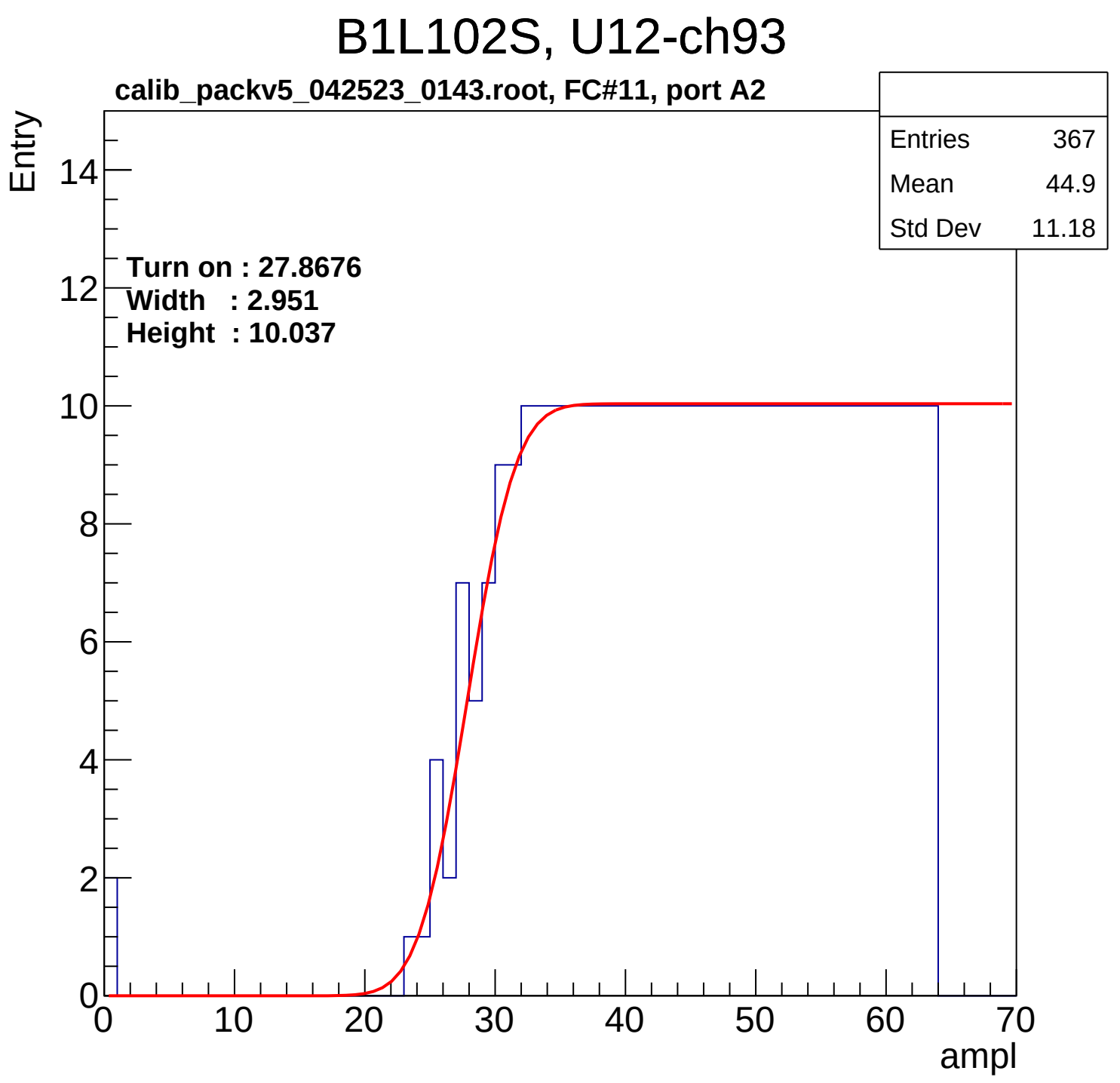
B1L102S, U12-ch93
calib_packv5_042523_0143.root, FC#11, port A2
Entries 367
Mean 44.9
Std Dev 11.18
Turn on : 27.8676
Width : 2.951
Height : 10.037
Entry
ampl
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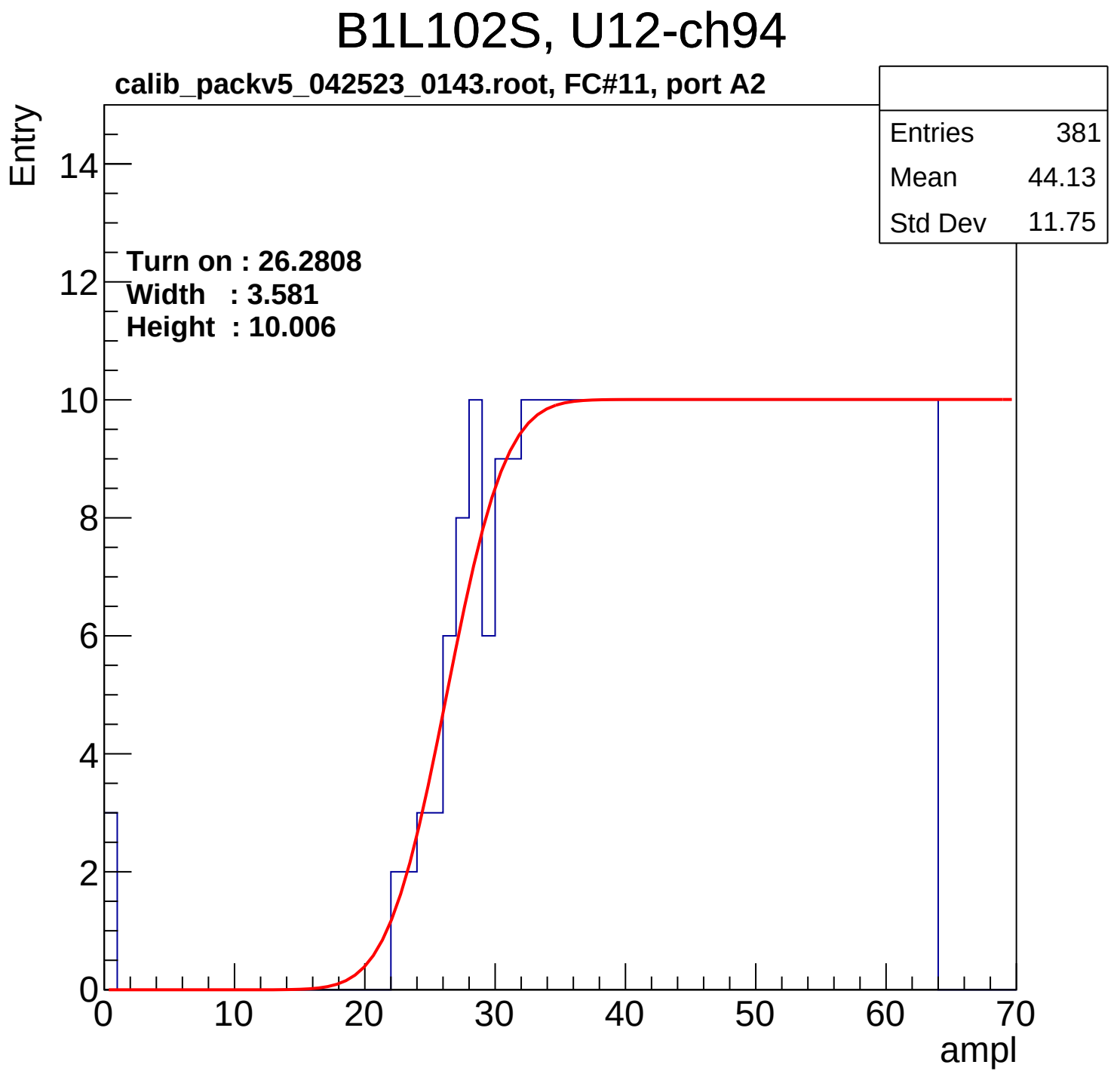
B1L102S, U12-ch94
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.13
Std Dev 11.75
Turn on : 26.2808
Width : 3.581
Height : 10.006
Entry
ampl
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6
8
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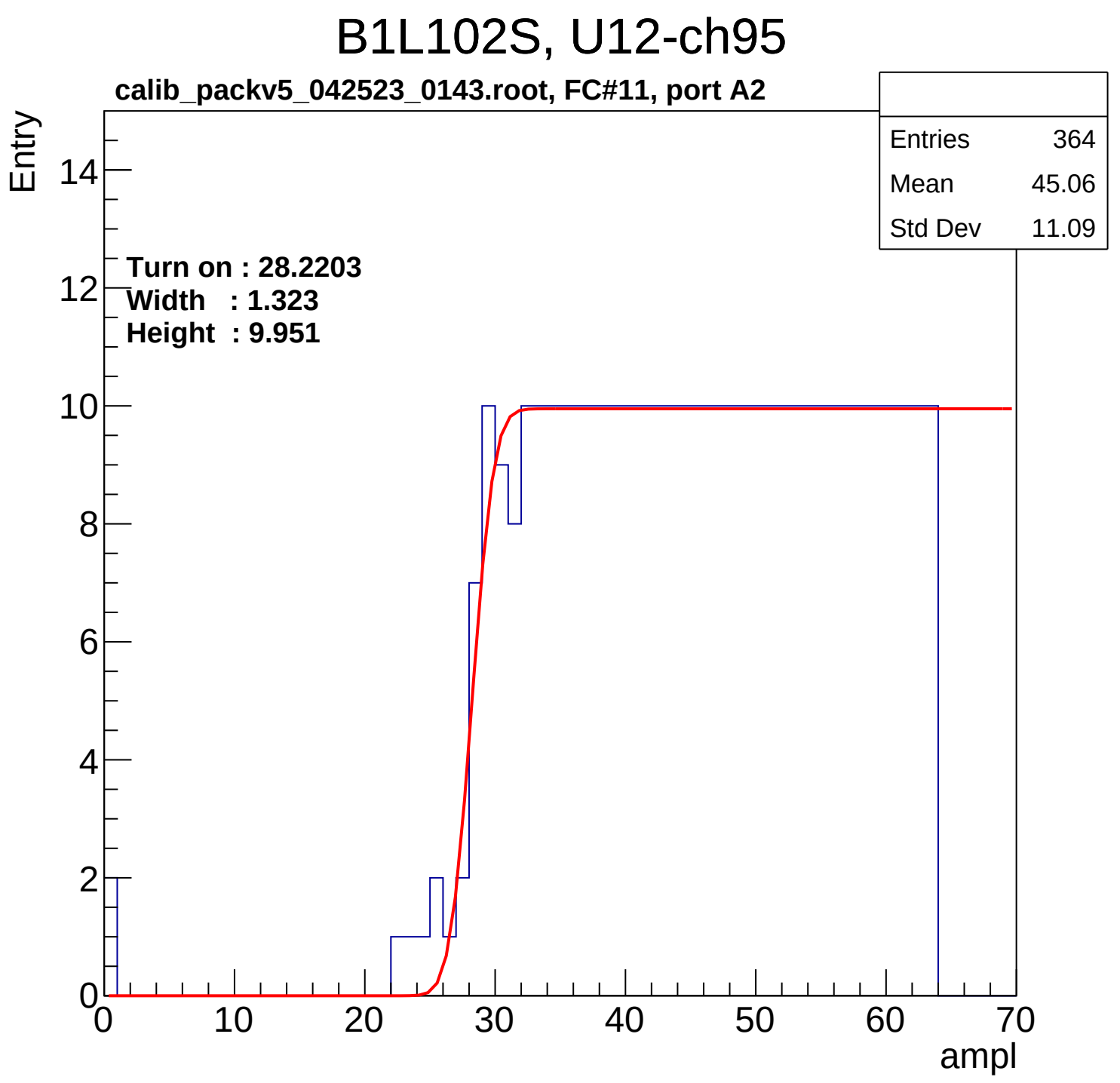
B1L102S, U12-ch95
calib_packv5_042523_0143.root, FC#11, port A2
Entries 364
Mean 45.06
Std Dev 11.09
Turn on : 28.2203
Width : 1.323
Height : 9.951
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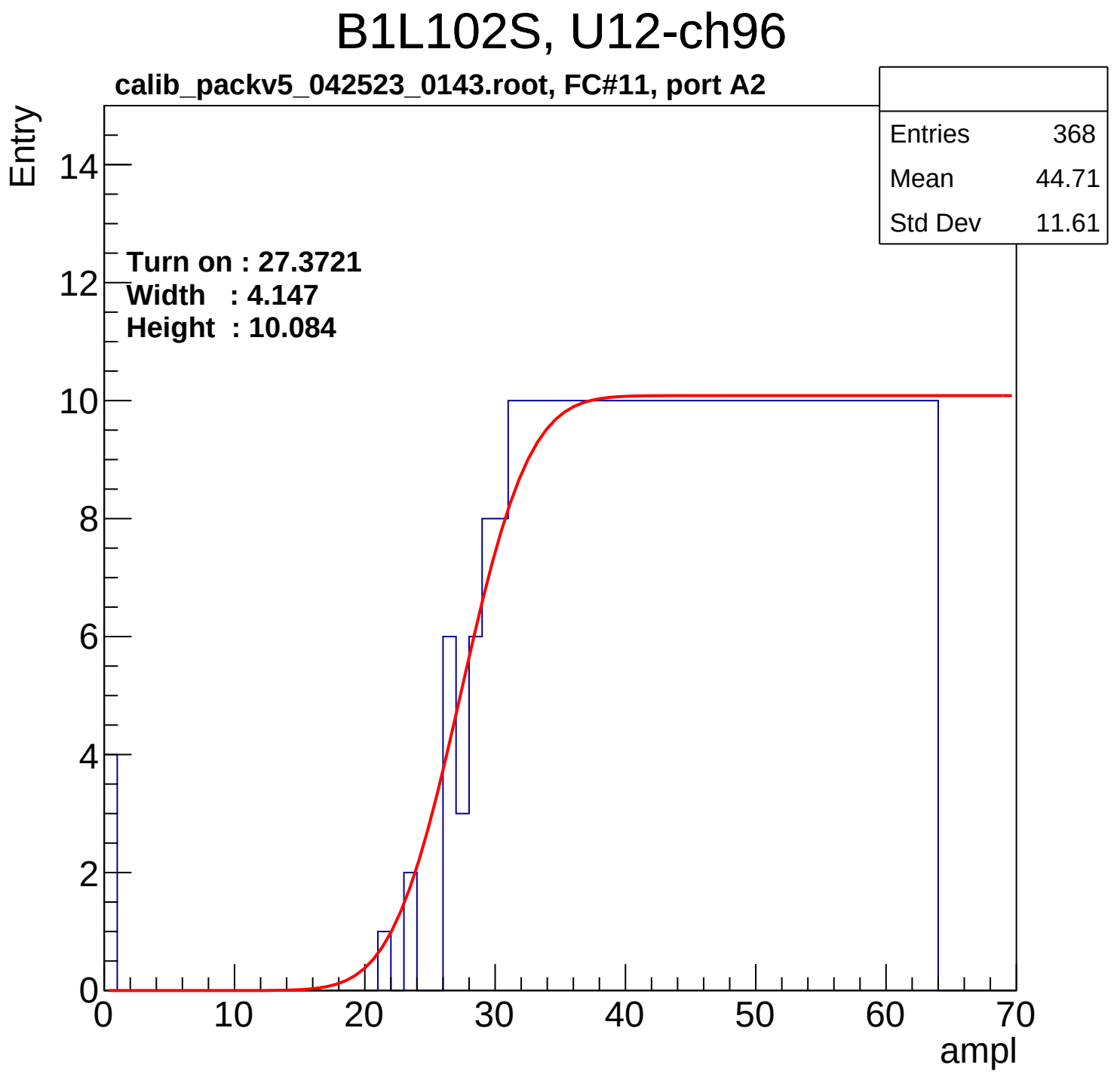
B1L102S, U12-ch96
calib_packv5_042523_0143.root, FC#11, port A2
Entries 368
Mean 44.71
Std Dev 11.61
Turn on : 27.3721
Width : 4.147
Height : 10.084
Entry
ampl
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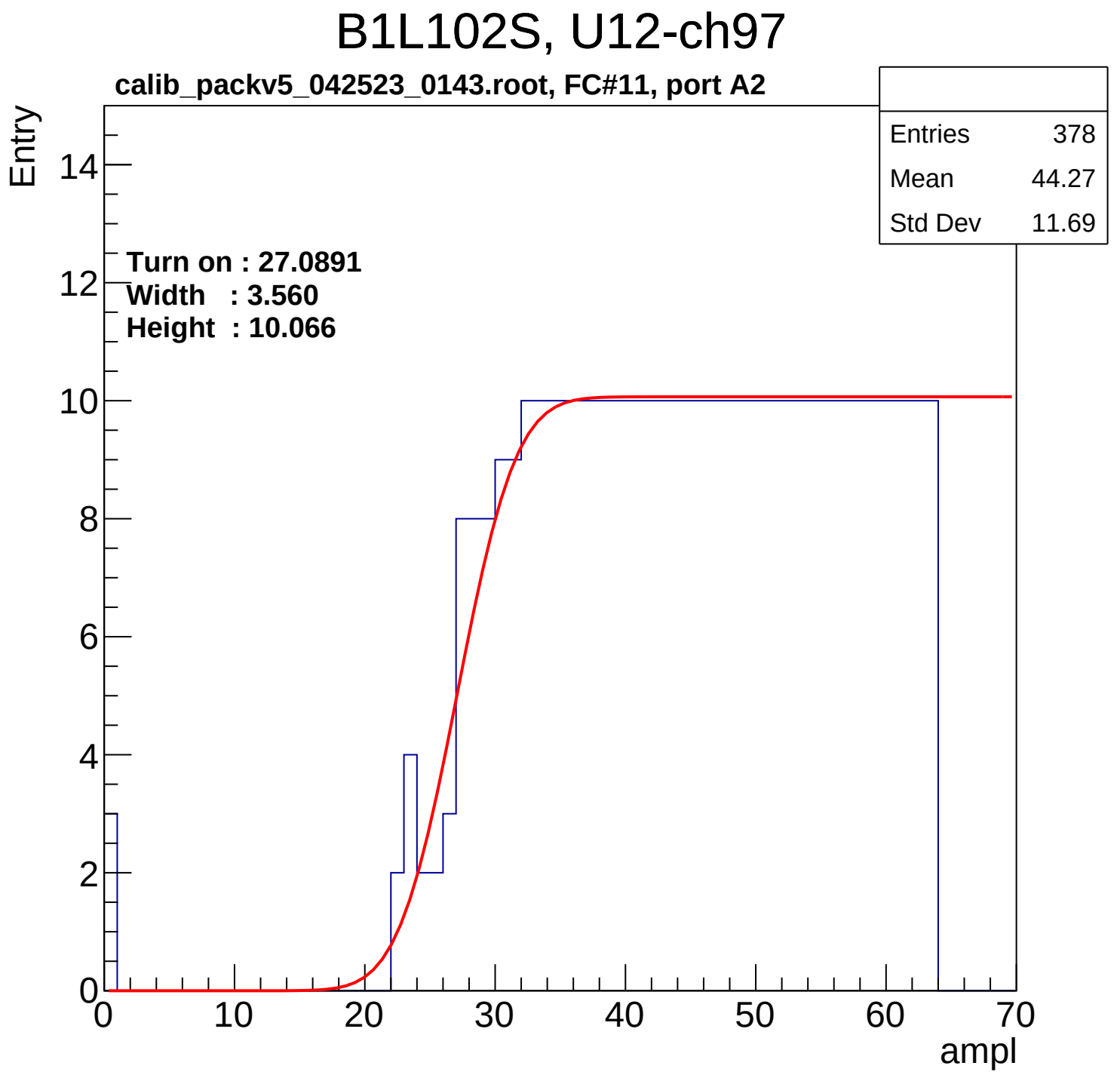
B1L102S, U12-ch97
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.27
Std Dev 11.69
Turn on : 27.0891
Width : 3.560
Height : 10.066
Entry
ampl
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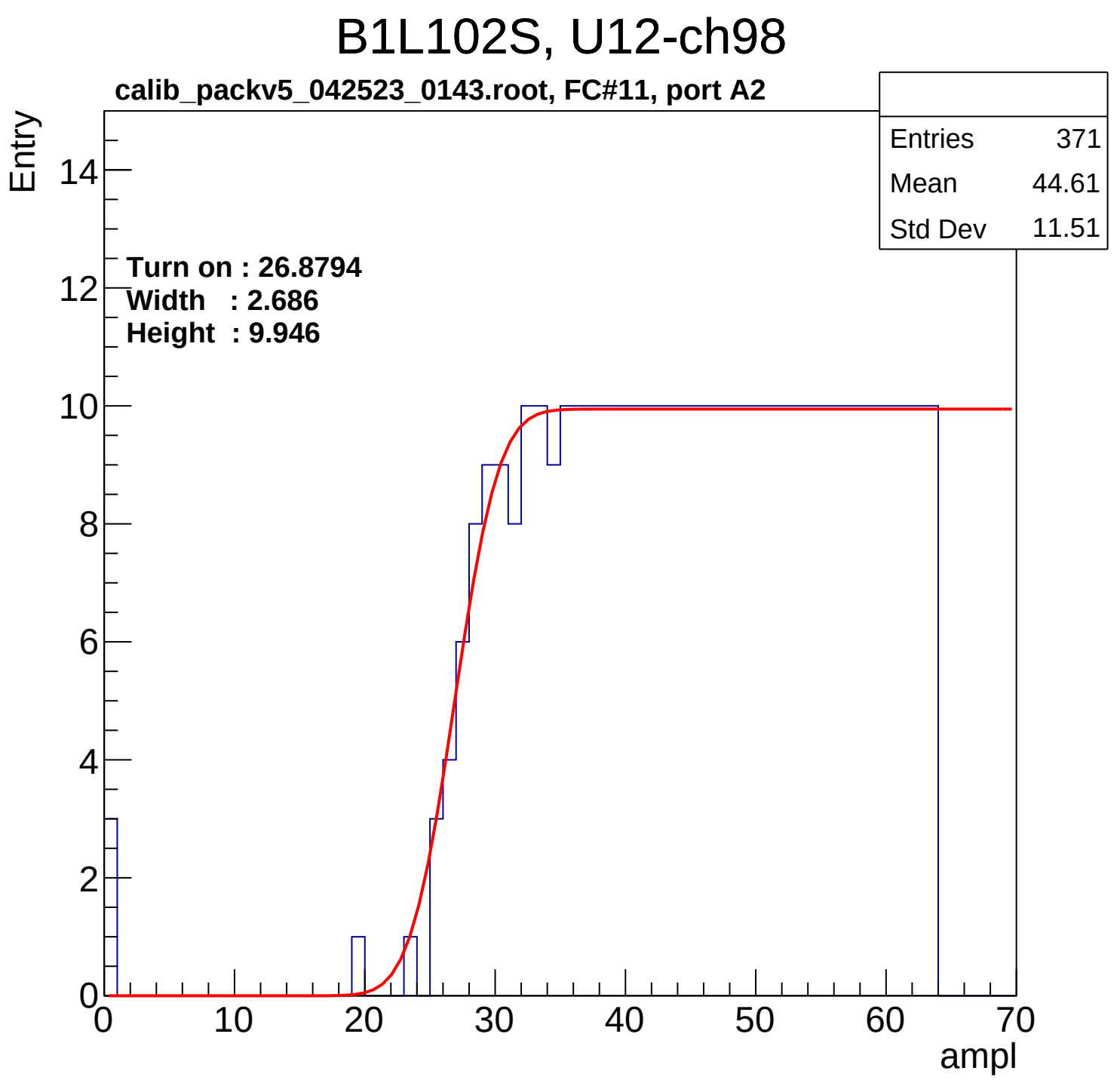
B1L102S, U12-ch98
calib_packv5_042523_0143.root, FC#11, port A2
Entries 371
Mean 44.61
Std Dev 11.51
Turn on : 26.8794
Width : 2.686
Height : 9.946
Entry
ampl
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8
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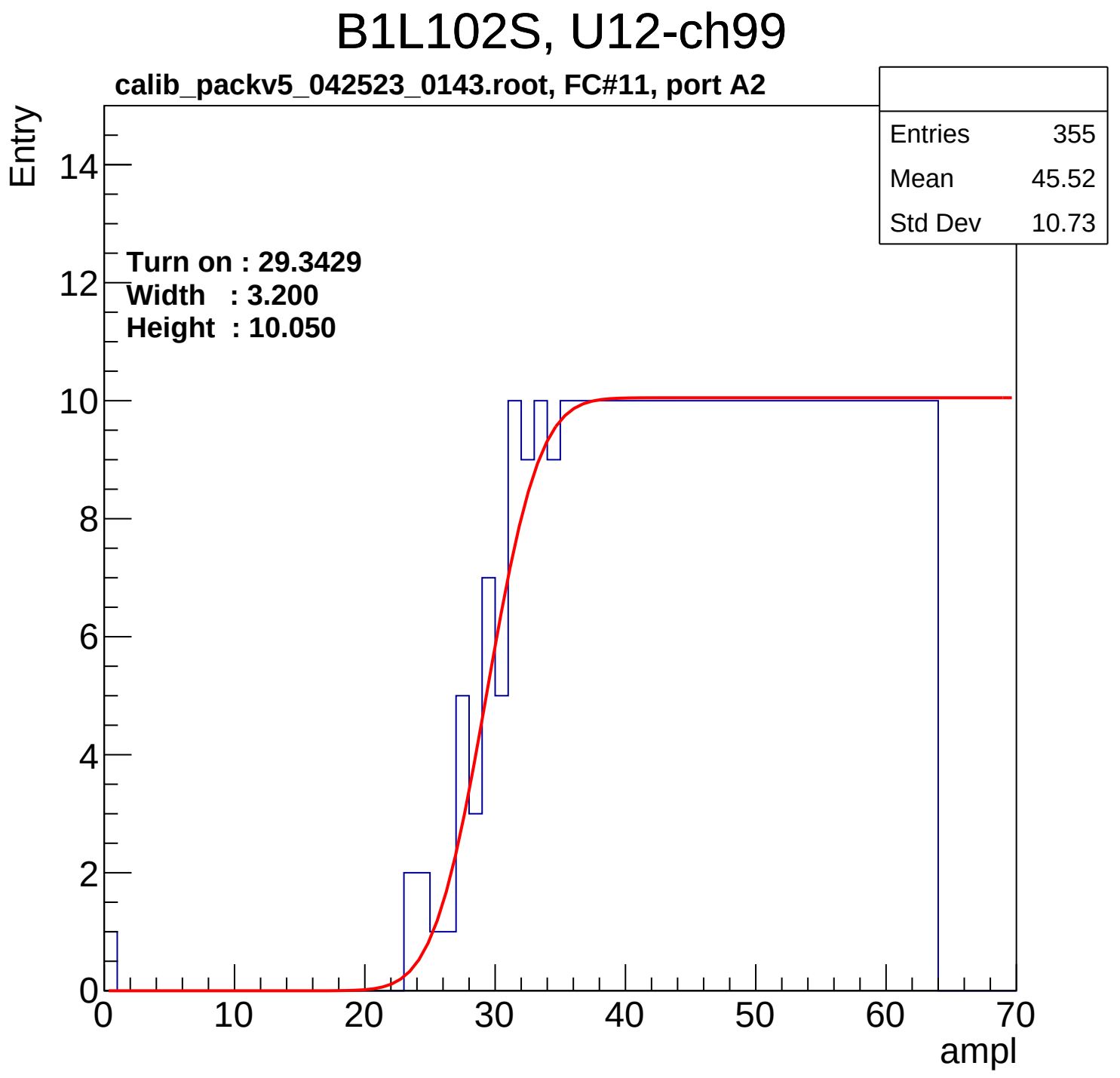
B1L102S, U12-ch99
calib_packv5_042523_0143.root, FC#11, port A2
Entries 355
Mean 45.52
Std Dev 10.73
Turn on : 29.3429
Width : 3.200
Height : 10.050
Entry
ampl
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6
8
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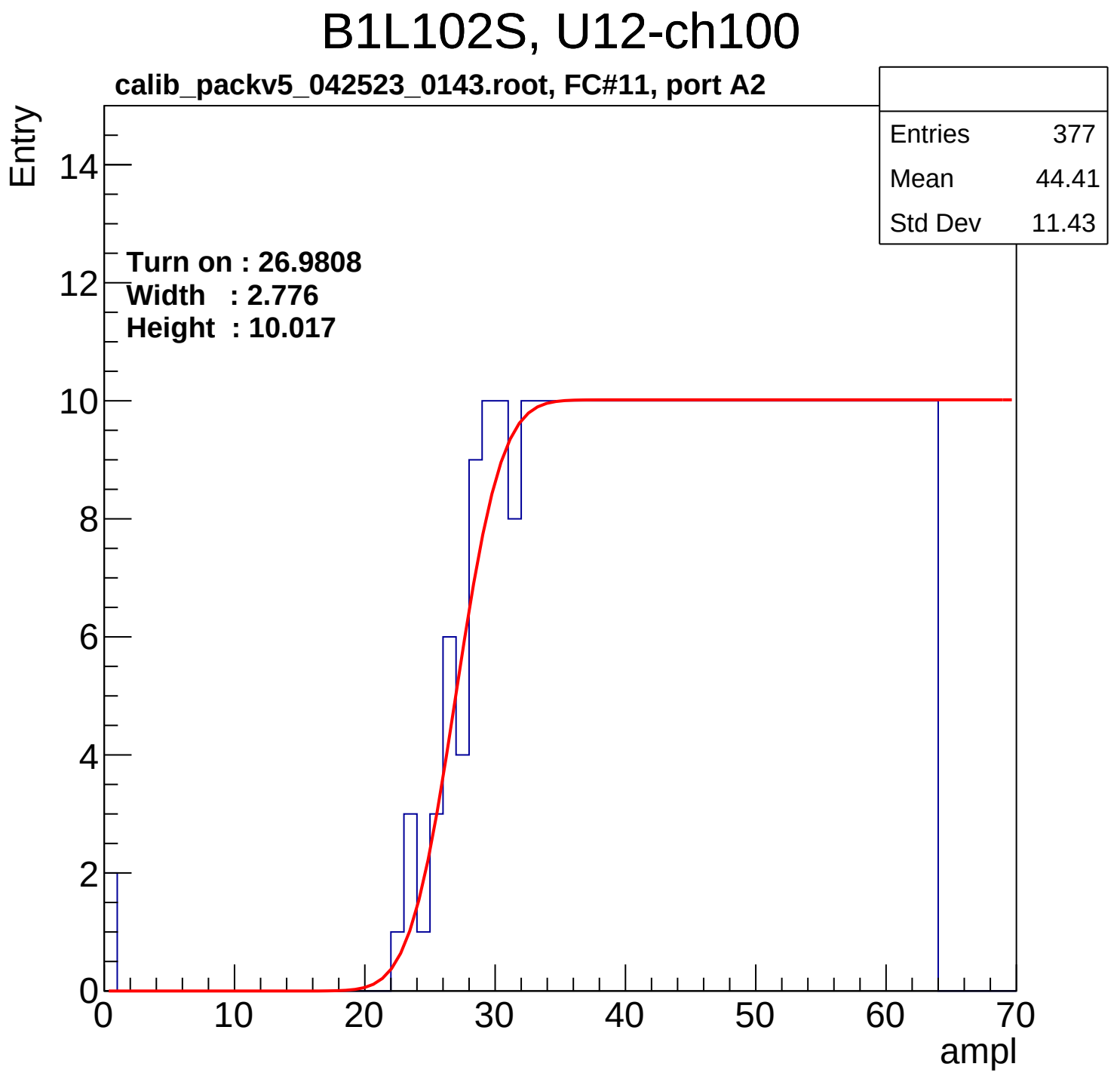
B1L102S, U12-ch100
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.41
Std Dev 11.43
Turn on : 26.9808
Width : 2.776
Height : 10.017
Entry
ampl
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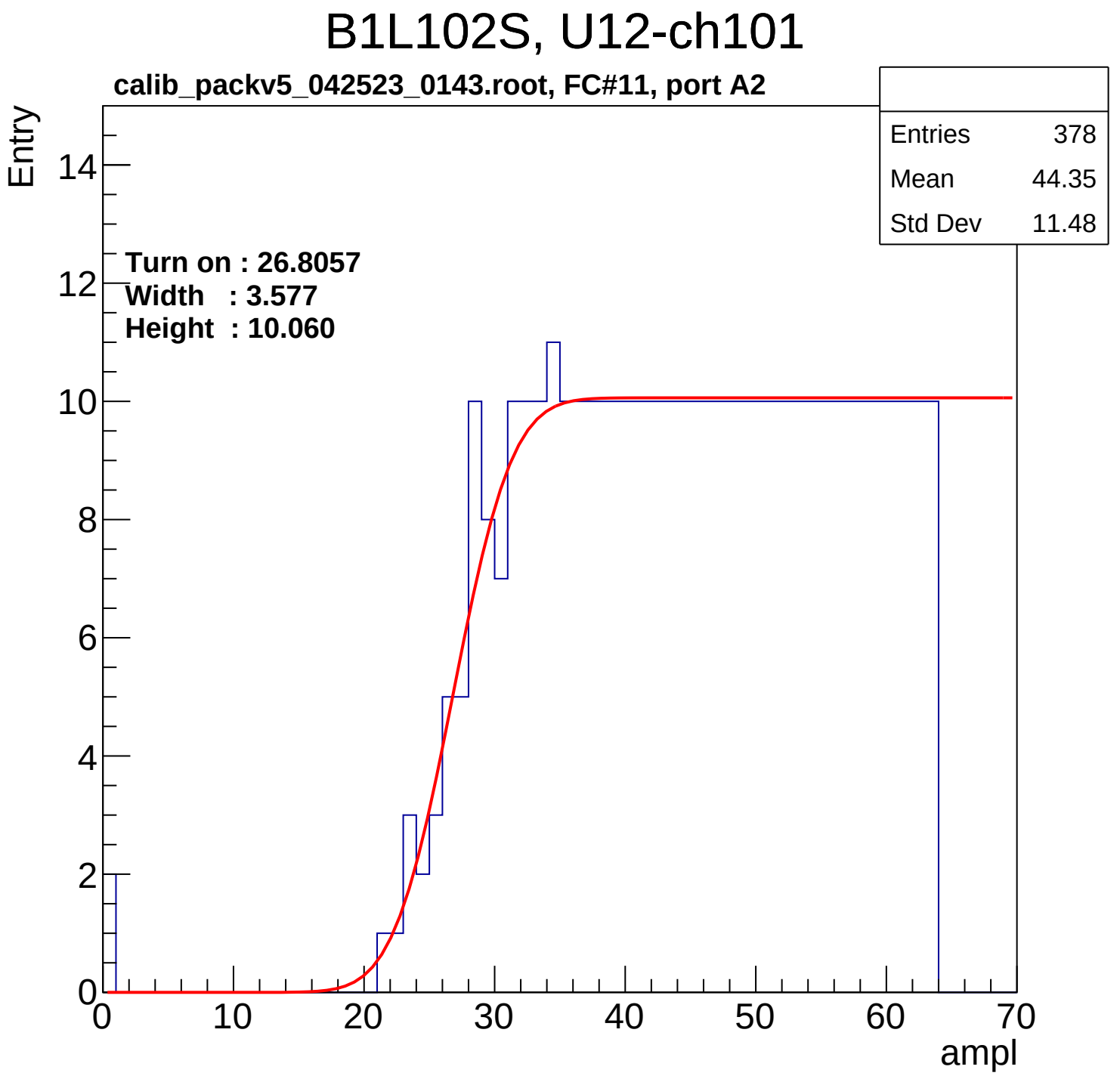
B1L102S, U12-ch101
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.35
Std Dev 11.48
Turn on : 26.8057
Width : 3.577
Height : 10.060
Entry
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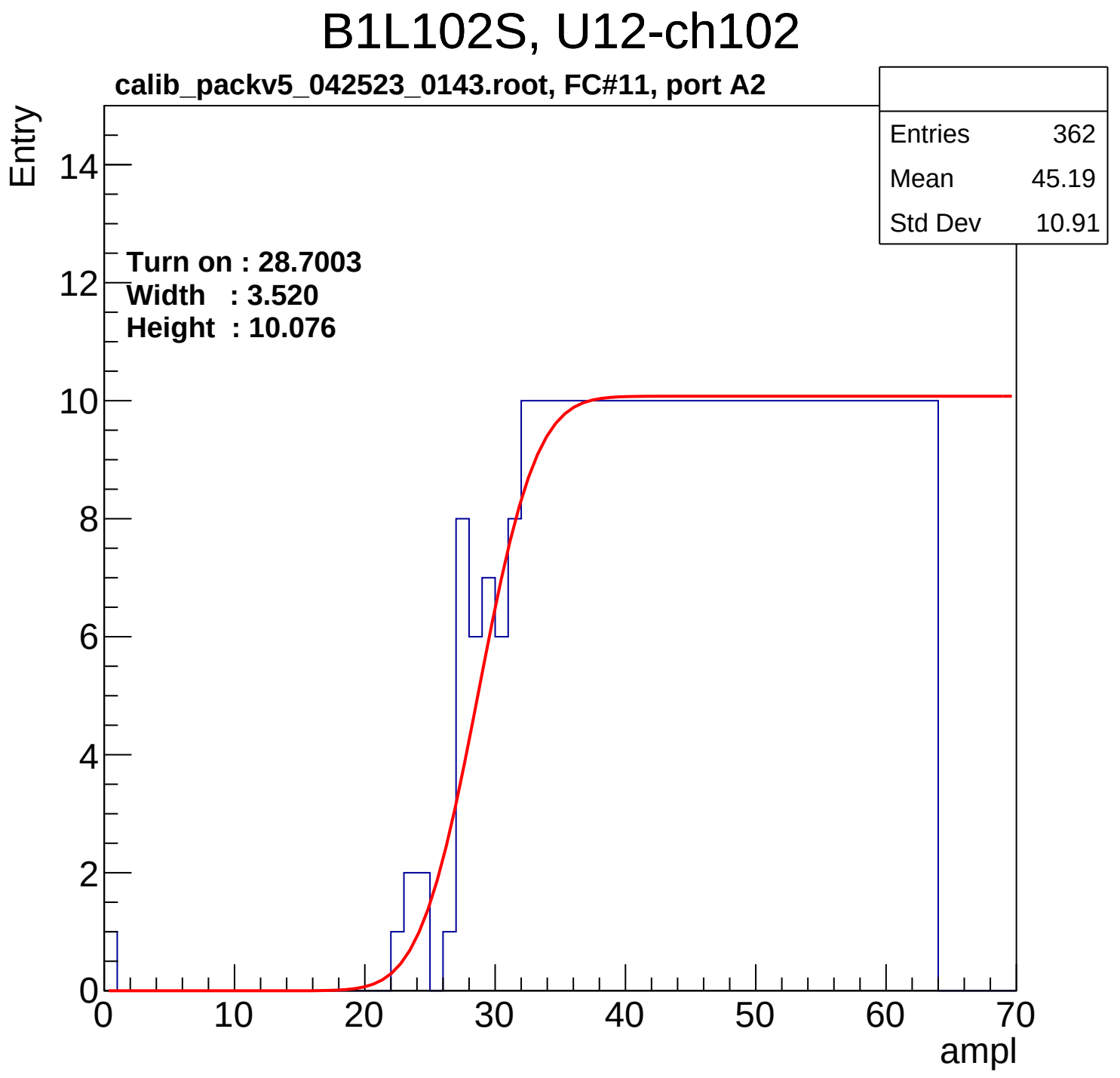
B1L102S, U12-ch102
calib_packv5_042523_0143.root, FC#11, port A2
Entries 362
Mean 45.19
Std Dev 10.91
Turn on : 28.7003
Width : 3.520
Height : 10.076
Entry
ampl
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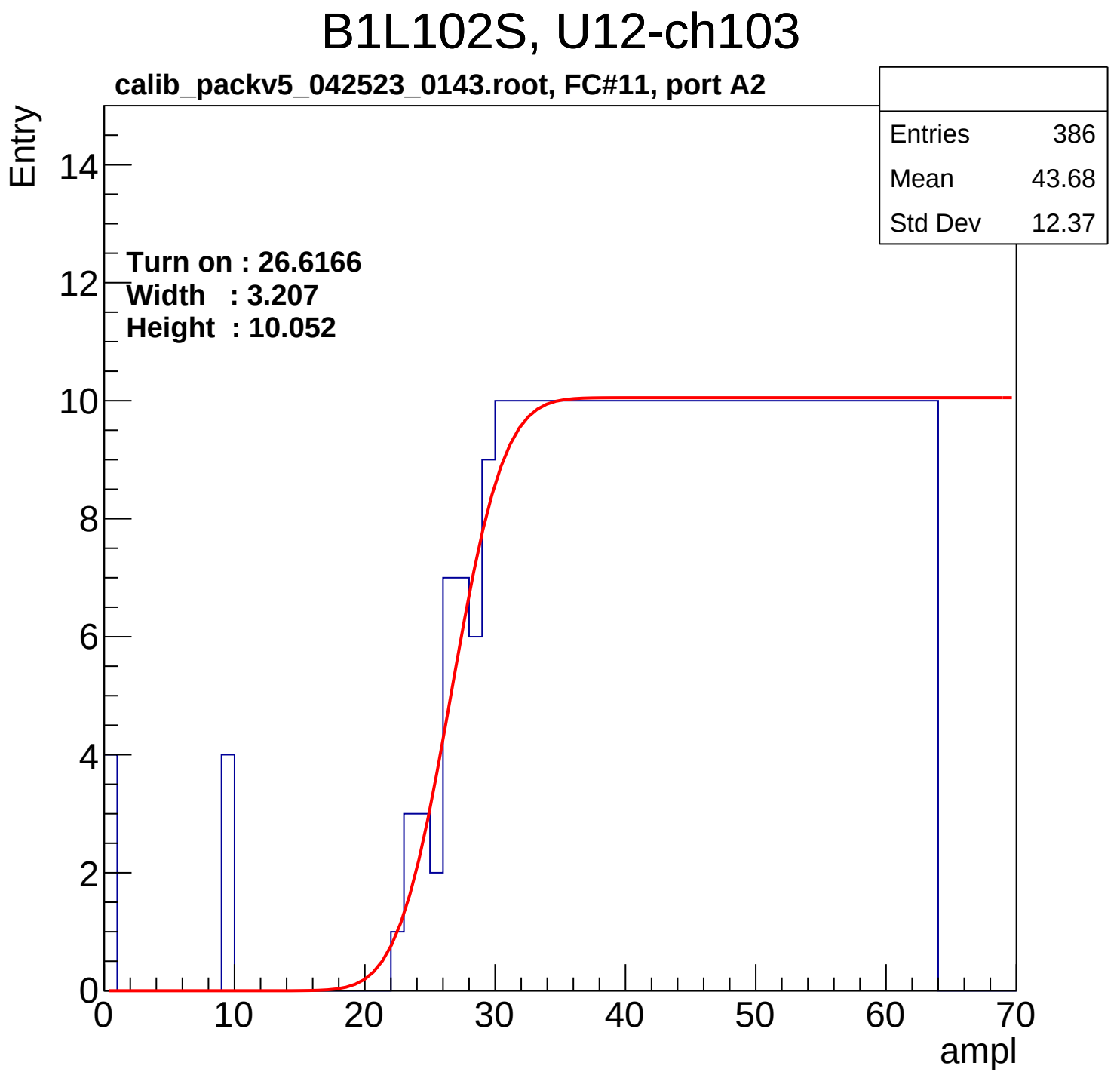
B1L102S, U12-ch103
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.68
Std Dev 12.37
Turn on : 26.6166
Width : 3.207
Height : 10.052
Entry
ampl
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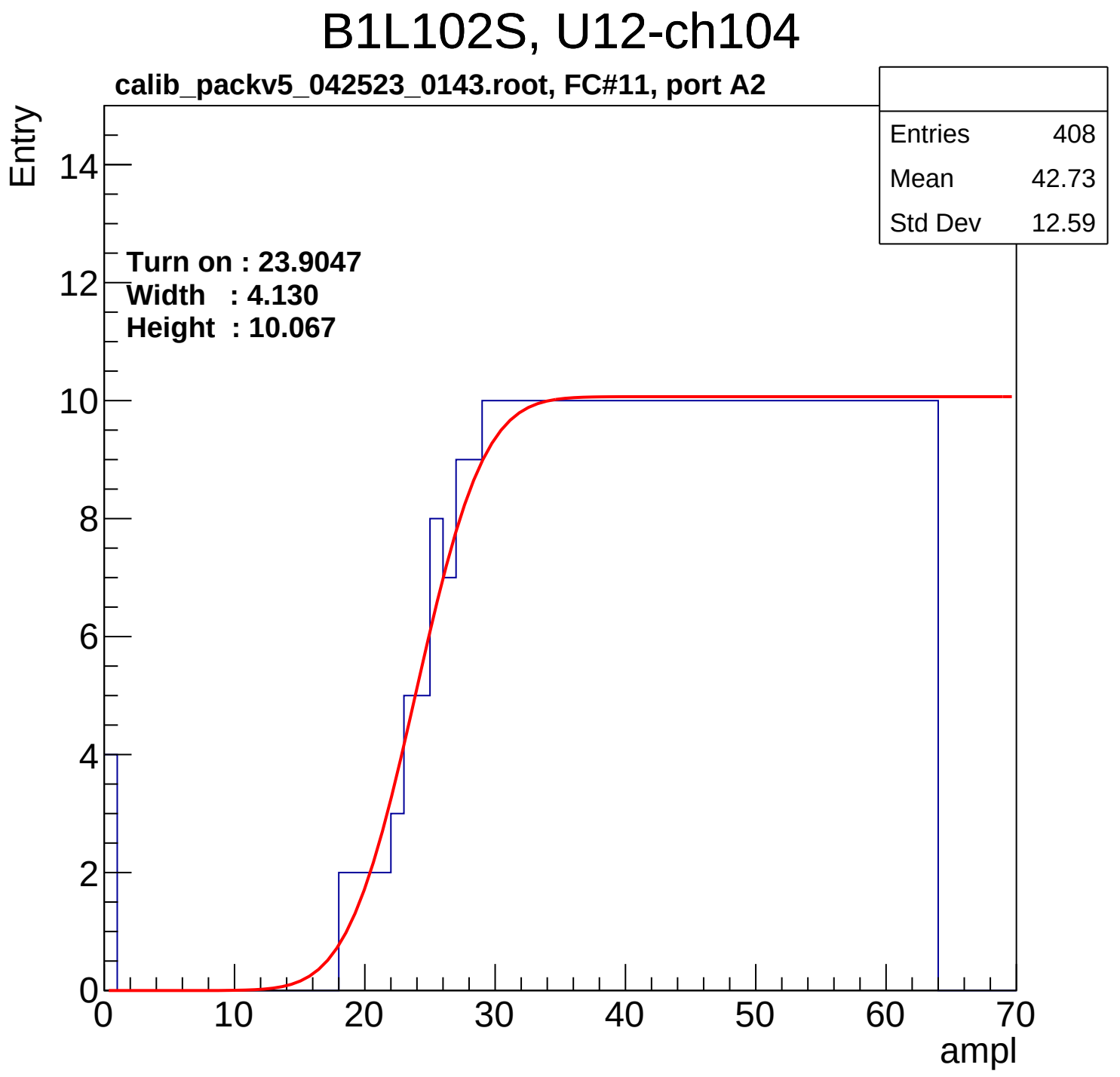
B1L102S, U12-ch104
calib_packv5_042523_0143.root, FC#11, port A2
Entries 408
Mean 42.73
Std Dev 12.59
Turn on : 23.9047
Width : 4.130
Height : 10.067
Entry
ampl
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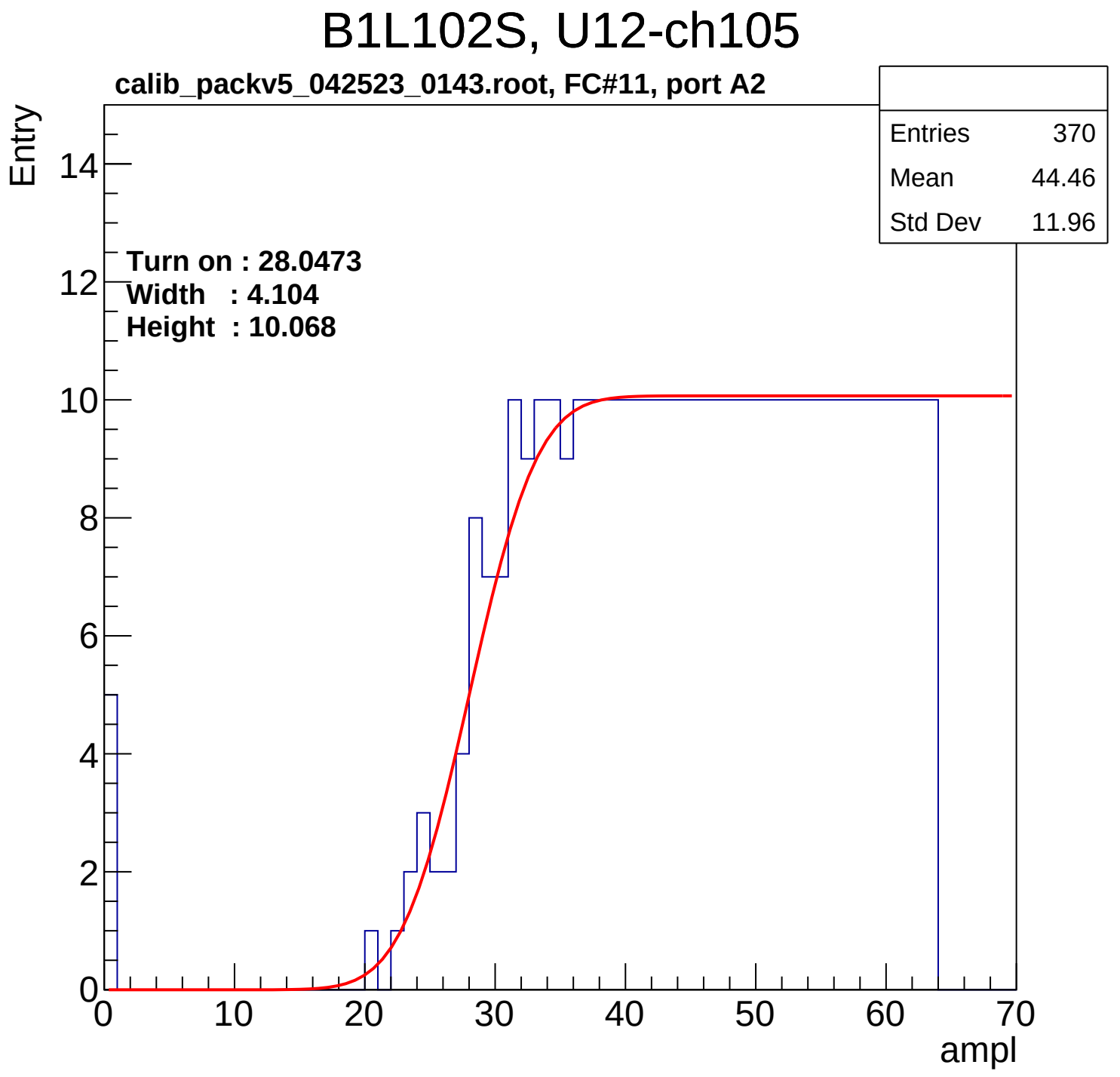
B1L102S, U12-ch105
calib_packv5_042523_0143.root, FC#11, port A2
Entries 370
Mean 44.46
Std Dev 11.96
Turn on : 28.0473
Width : 4.104
Height : 10.068
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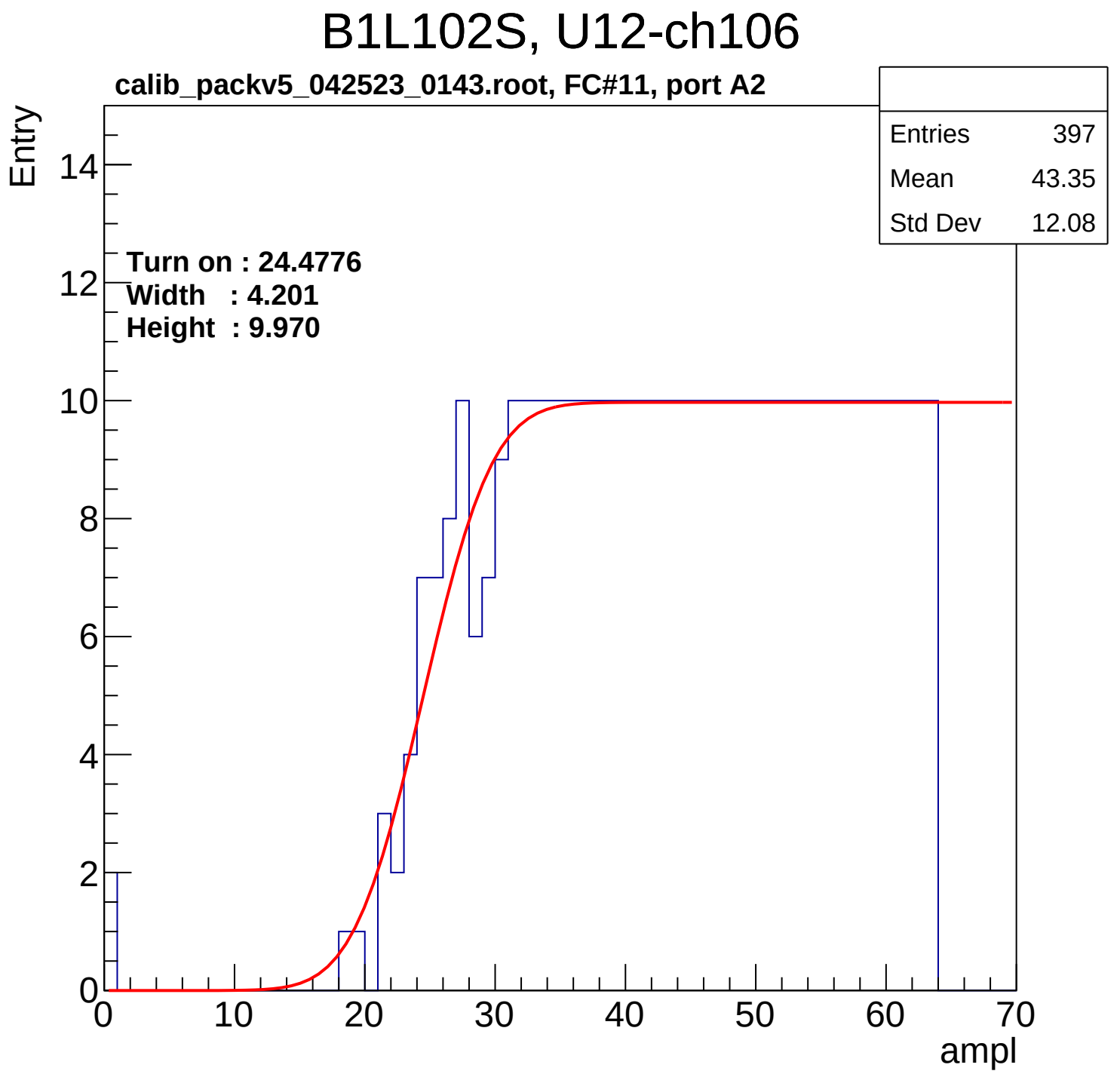
B1L102S, U12-ch106
calib_packv5_042523_0143.root, FC#11, port A2
Entries 397
Mean 43.35
Std Dev 12.08
Turn on : 24.4776
Width : 4.201
Height : 9.970
Entry
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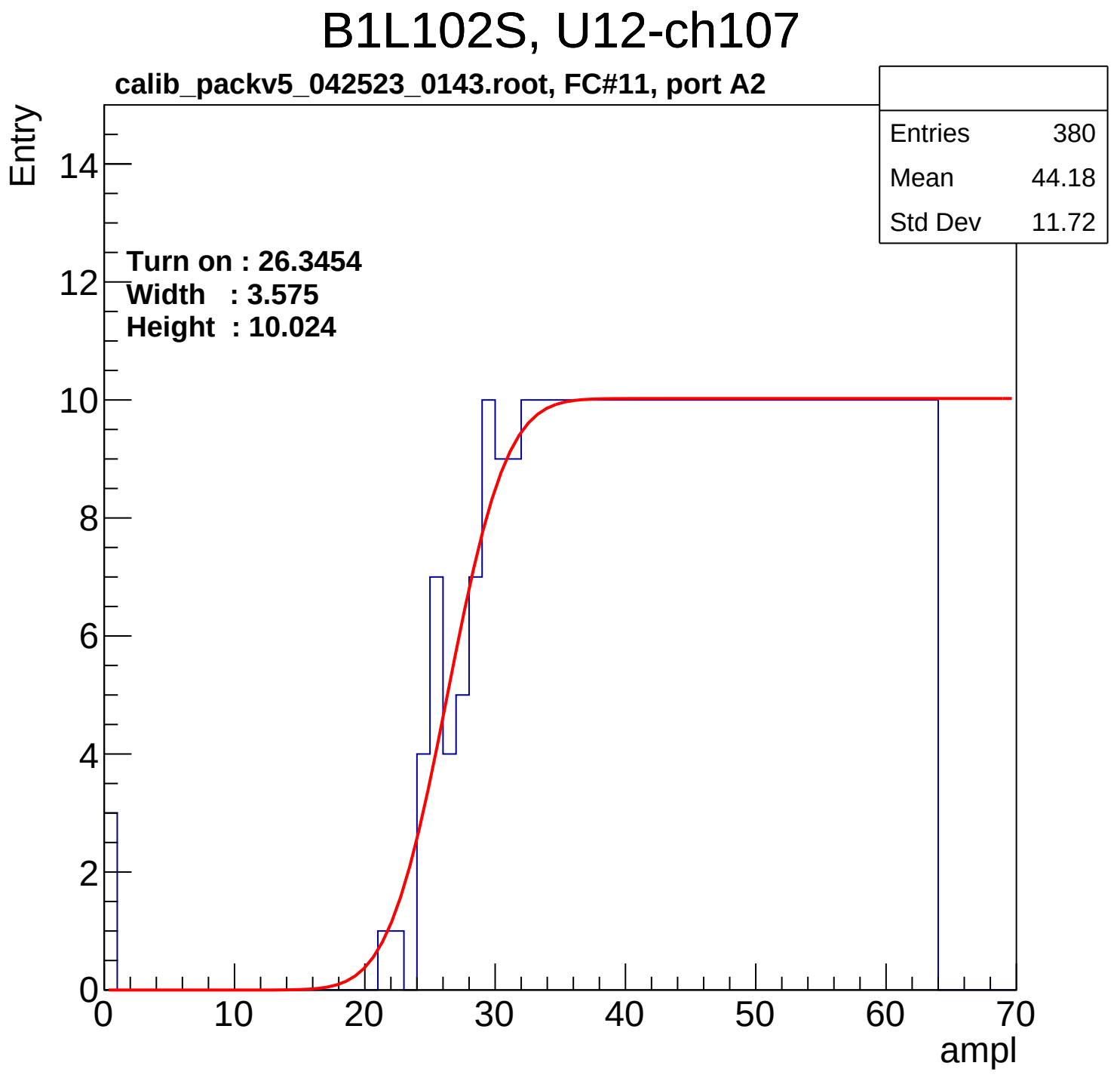
B1L102S, U12-ch107
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.18
Std Dev 11.72
Turn on : 26.3454
Width : 3.575
Height : 10.024
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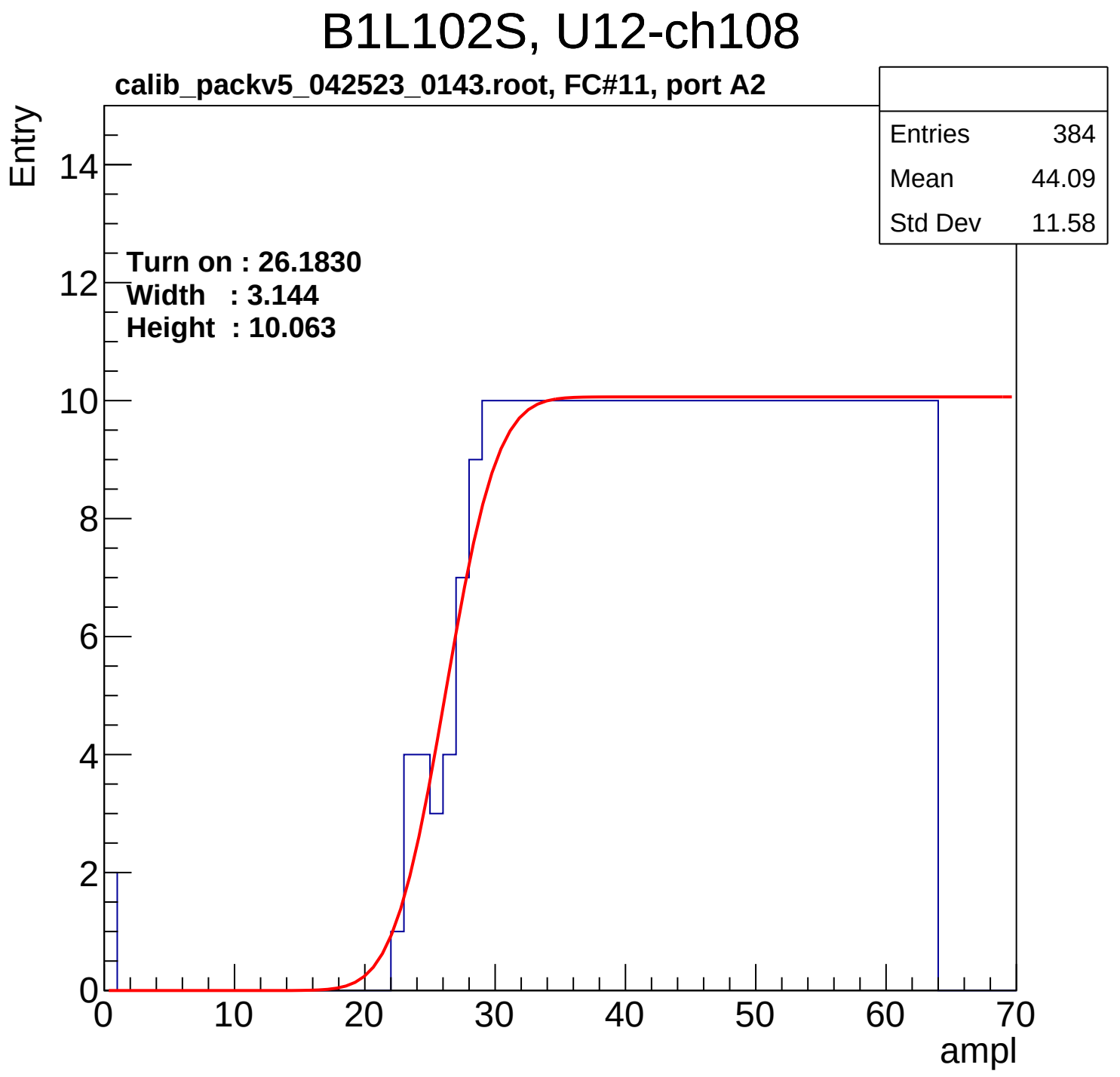
B1L102S, U12-ch108
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.09
Std Dev 11.58
Turn on : 26.1830
Width : 3.144
Height : 10.063
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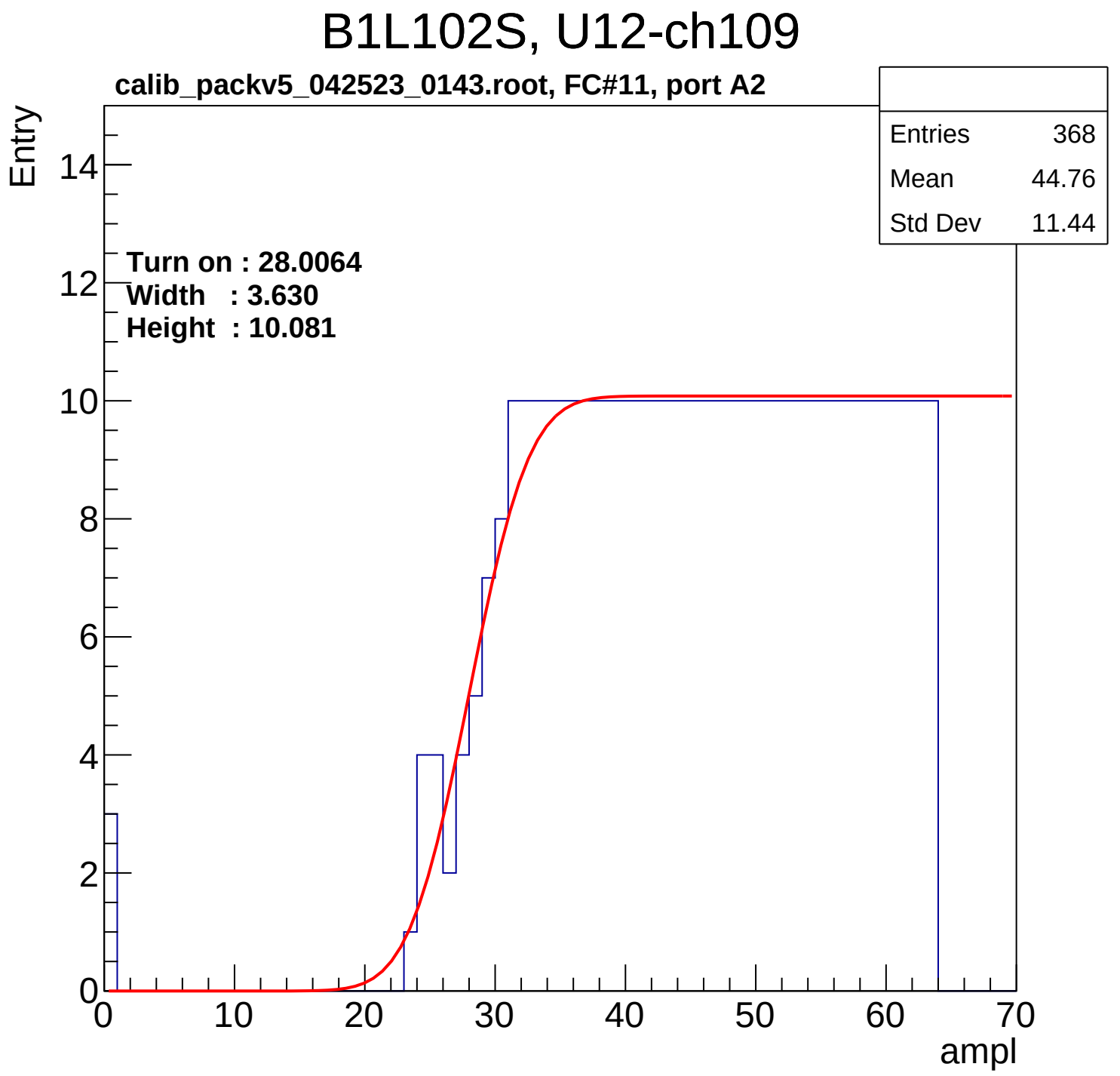
B1L102S, U12-ch109
calib_packv5_042523_0143.root, FC#11, port A2
Entries 368
Mean 44.76
Std Dev 11.44
Turn on : 28.0064
Width : 3.630
Height : 10.081
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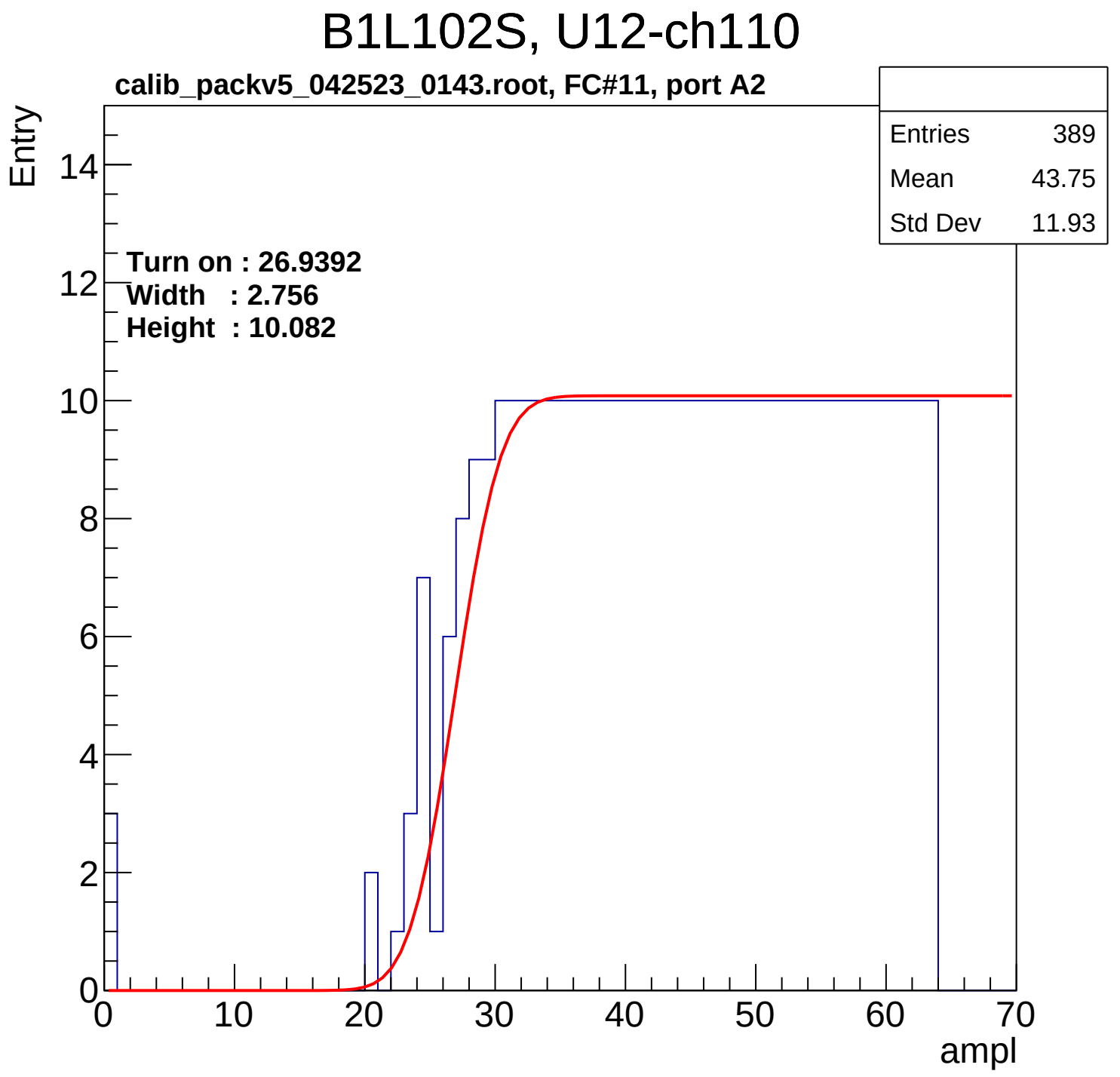
B1L102S, U12-ch110
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.75
Std Dev 11.93
Turn on : 26.9392
Width : 2.756
Height : 10.082
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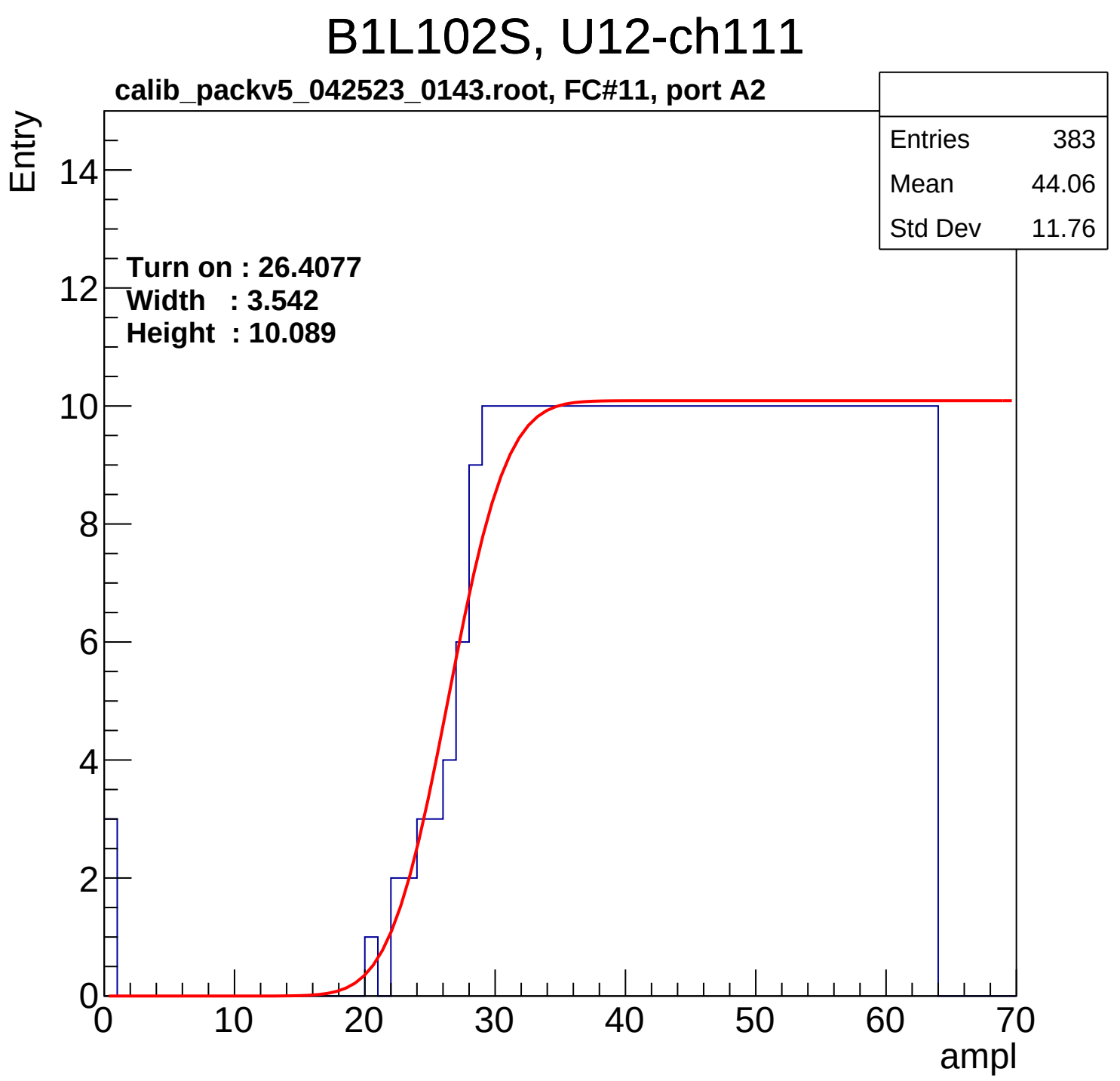
B1L102S, U12-ch111
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.06
Std Dev 11.76
Turn on : 26.4077
Width : 3.542
Height : 10.089
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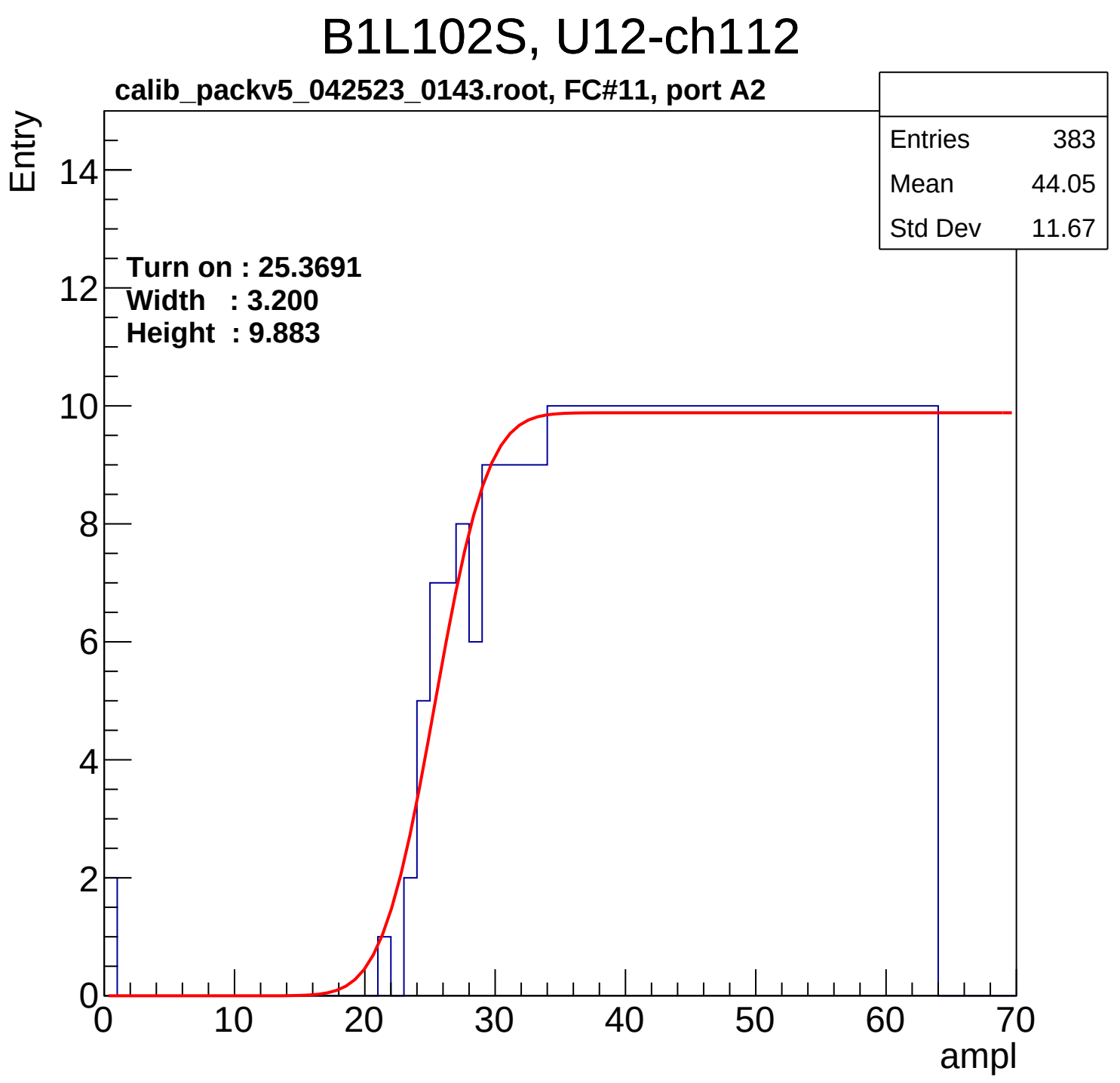
B1L102S, U12-ch112
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.05
Std Dev 11.67
Turn on : 25.3691
Width : 3.200
Height : 9.883
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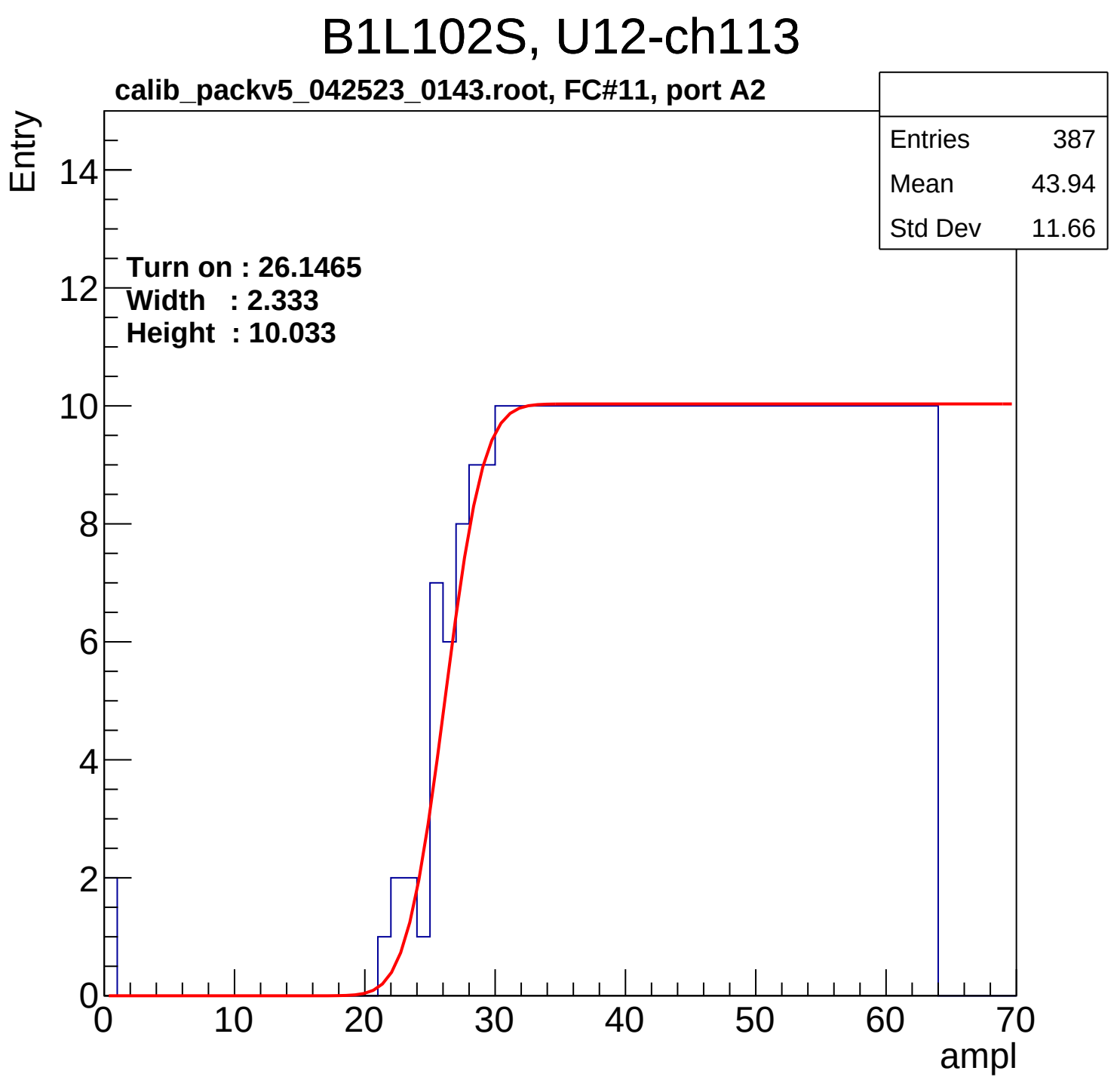
B1L102S, U12-ch113
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.94
Std Dev 11.66
Turn on : 26.1465
Width : 2.333
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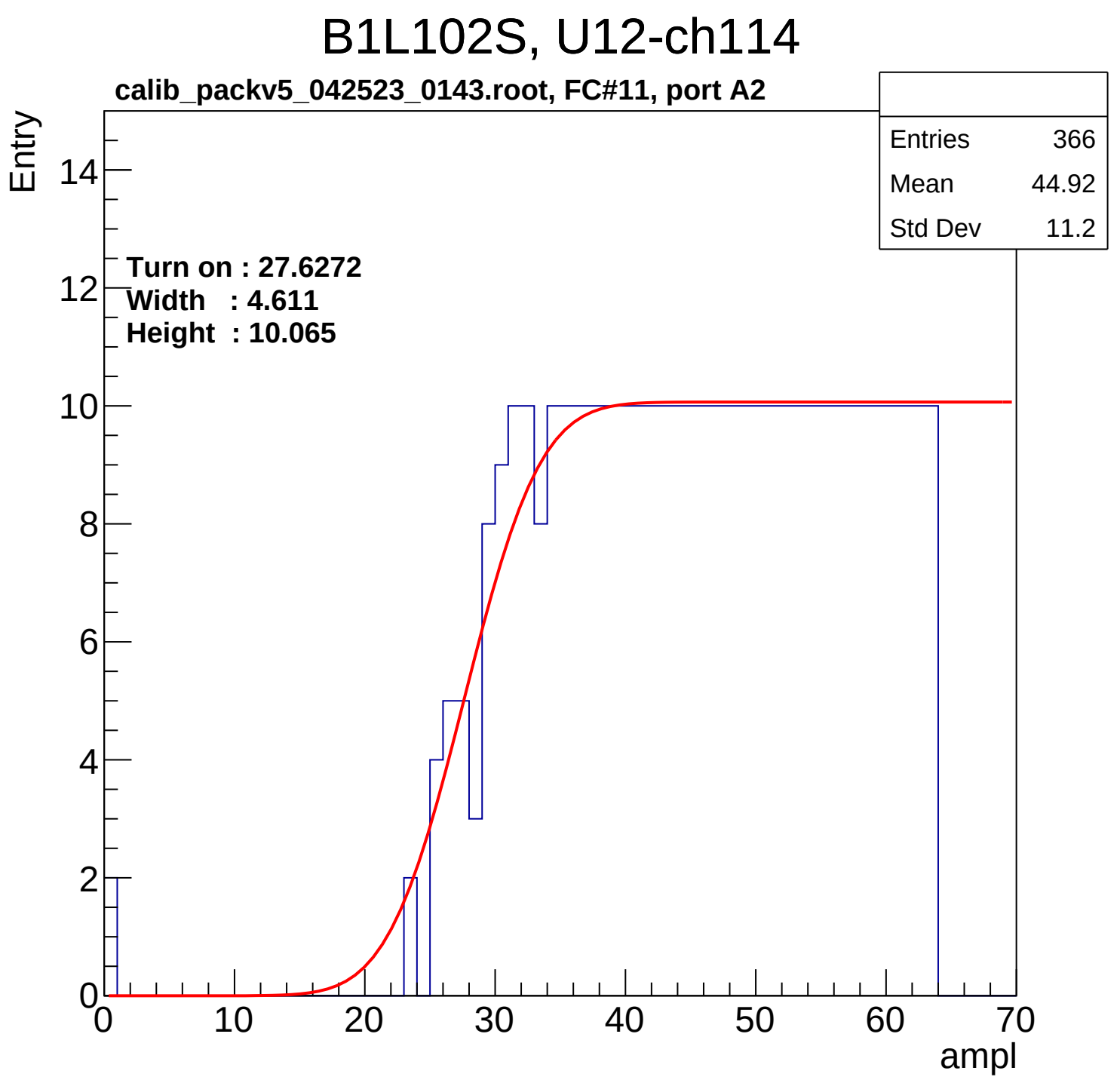
B1L102S, U12-ch114
calib_packv5_042523_0143.root, FC#11, port A2
Entries 366
Mean 44.92
Std Dev 11.2
Turn on : 27.6272
Width : 4.611
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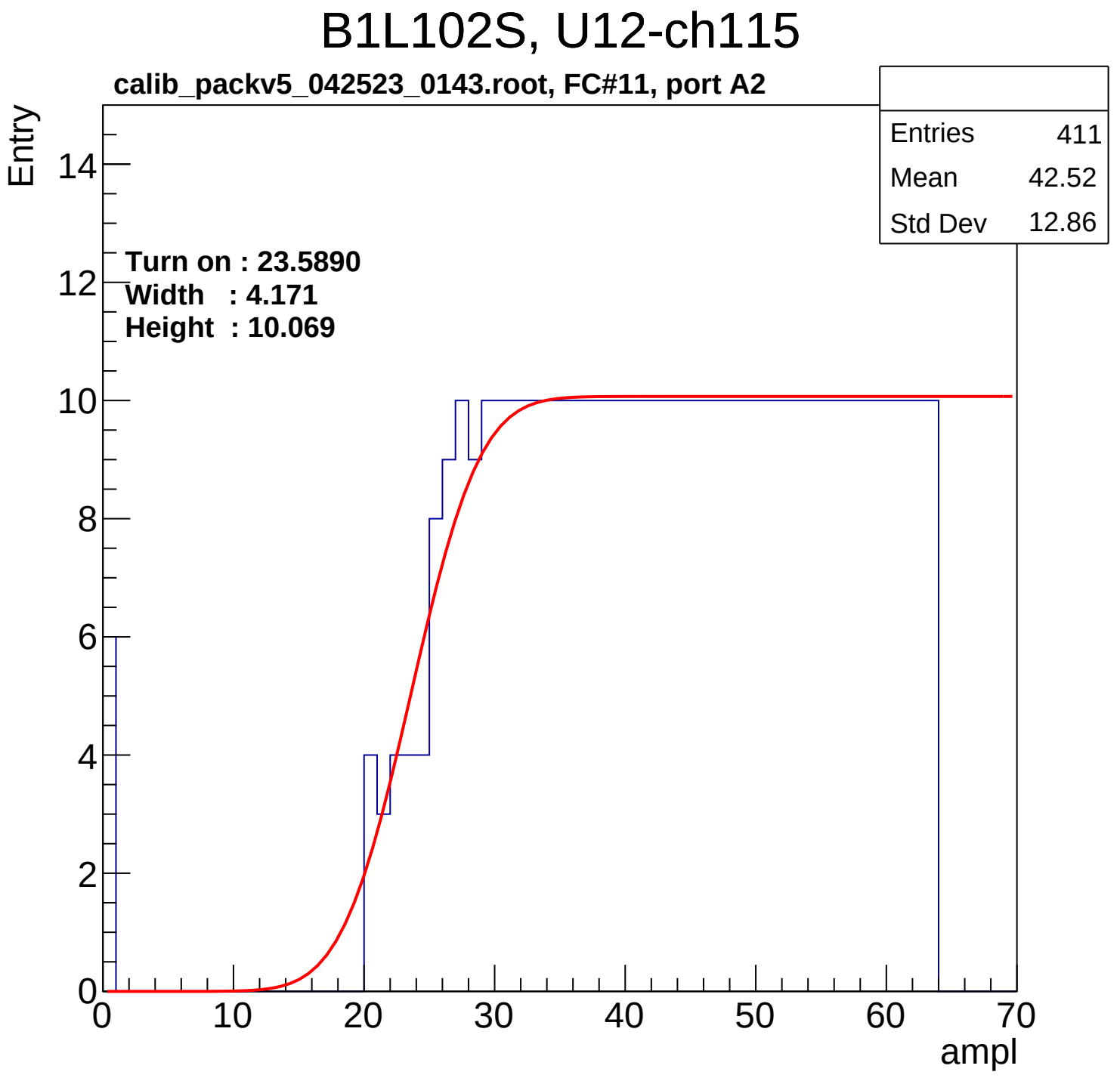
B1L102S, U12-ch115
calib_packv5_042523_0143.root, FC#11, port A2
Entries 411
Mean 42.52
Std Dev 12.86
Turn on : 23.5890
Width : 4.171
Height : 10.069
Entry
ampl
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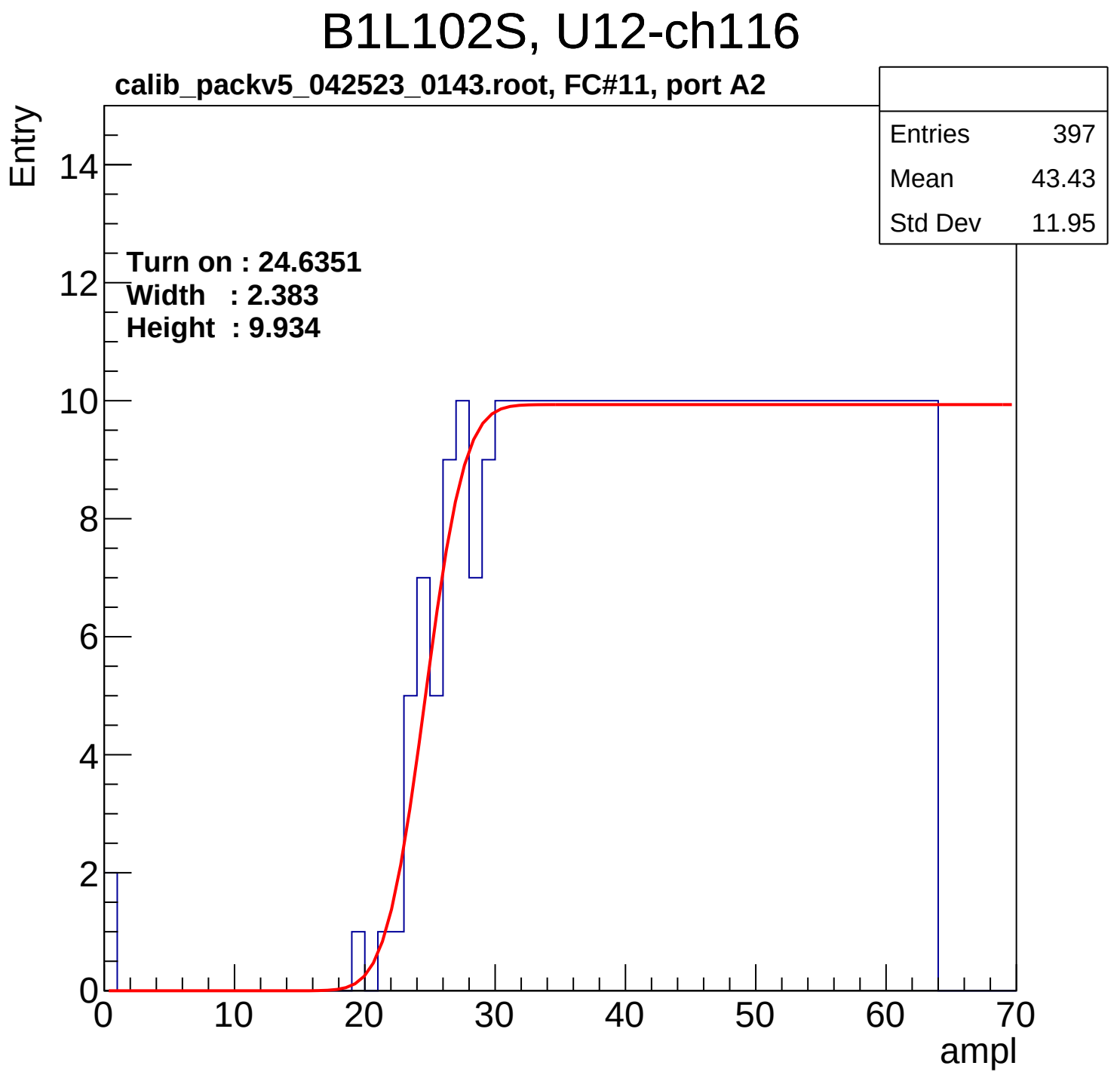
B1L102S, U12-ch116
calib_packv5_042523_0143.root, FC#11, port A2
Entries 397
Mean 43.43
Std Dev 11.95
Turn on : 24.6351
Width : 2.383
Height : 9.934
Entry
ampl
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2
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6
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10
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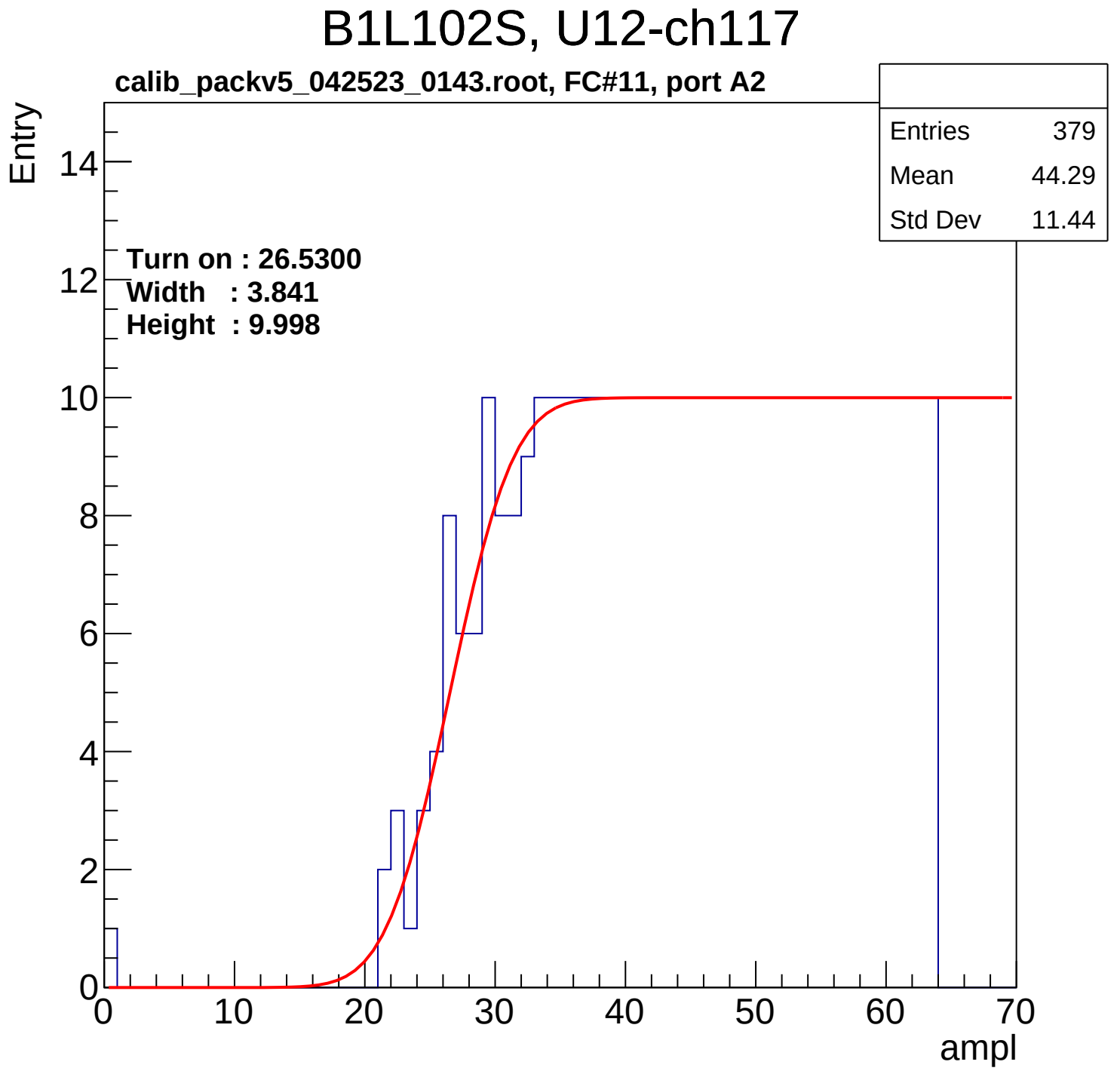
B1L102S, U12-ch117
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.29
Std Dev 11.44
Turn on : 26.5300
Width : 3.841
Height : 9.998
Entry
ampl
0
2
4
6
8
10
12
14
0
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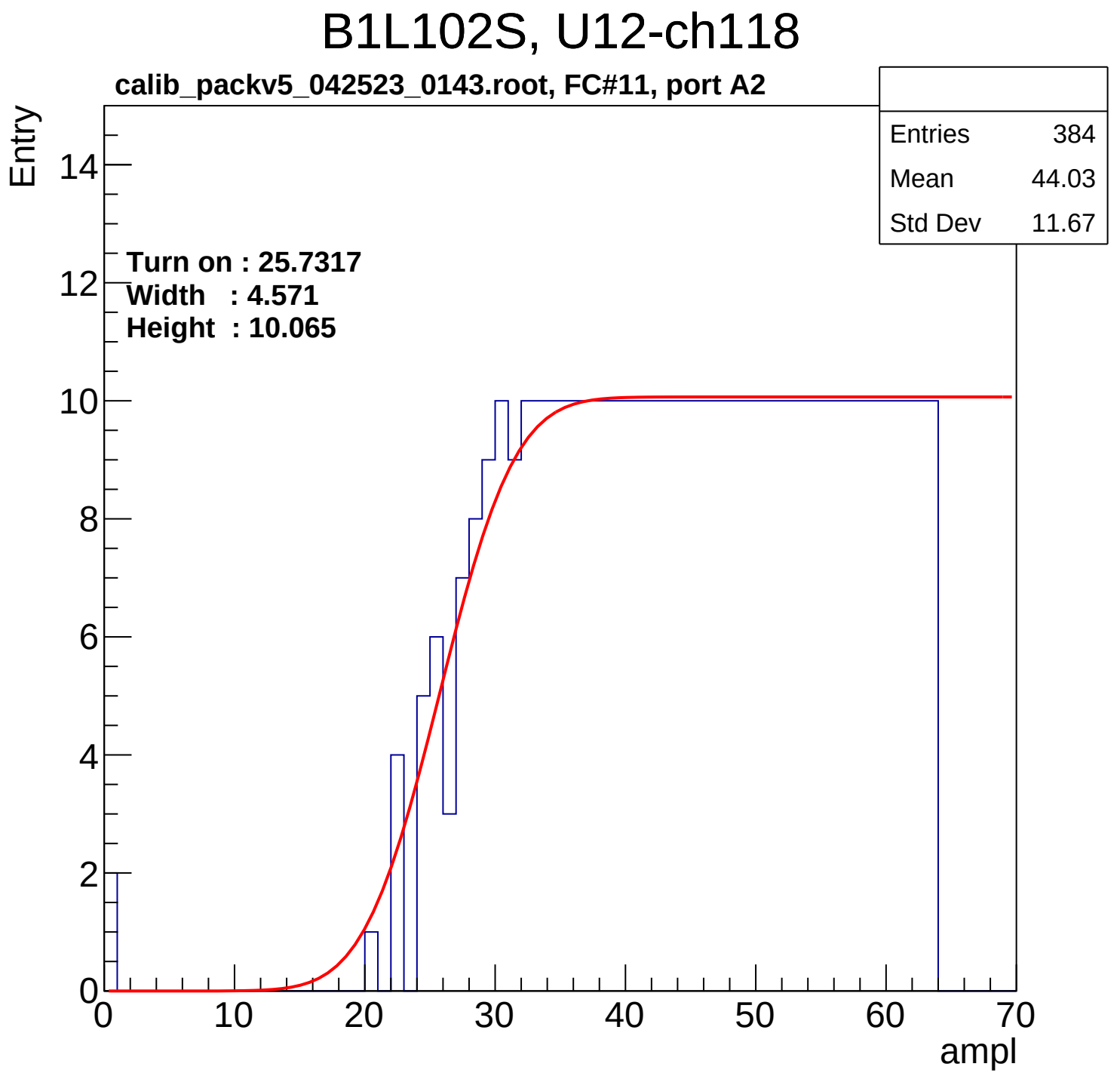
B1L102S, U12-ch118
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.03
Std Dev 11.67
Turn on : 25.7317
Width : 4.571
Height : 10.065
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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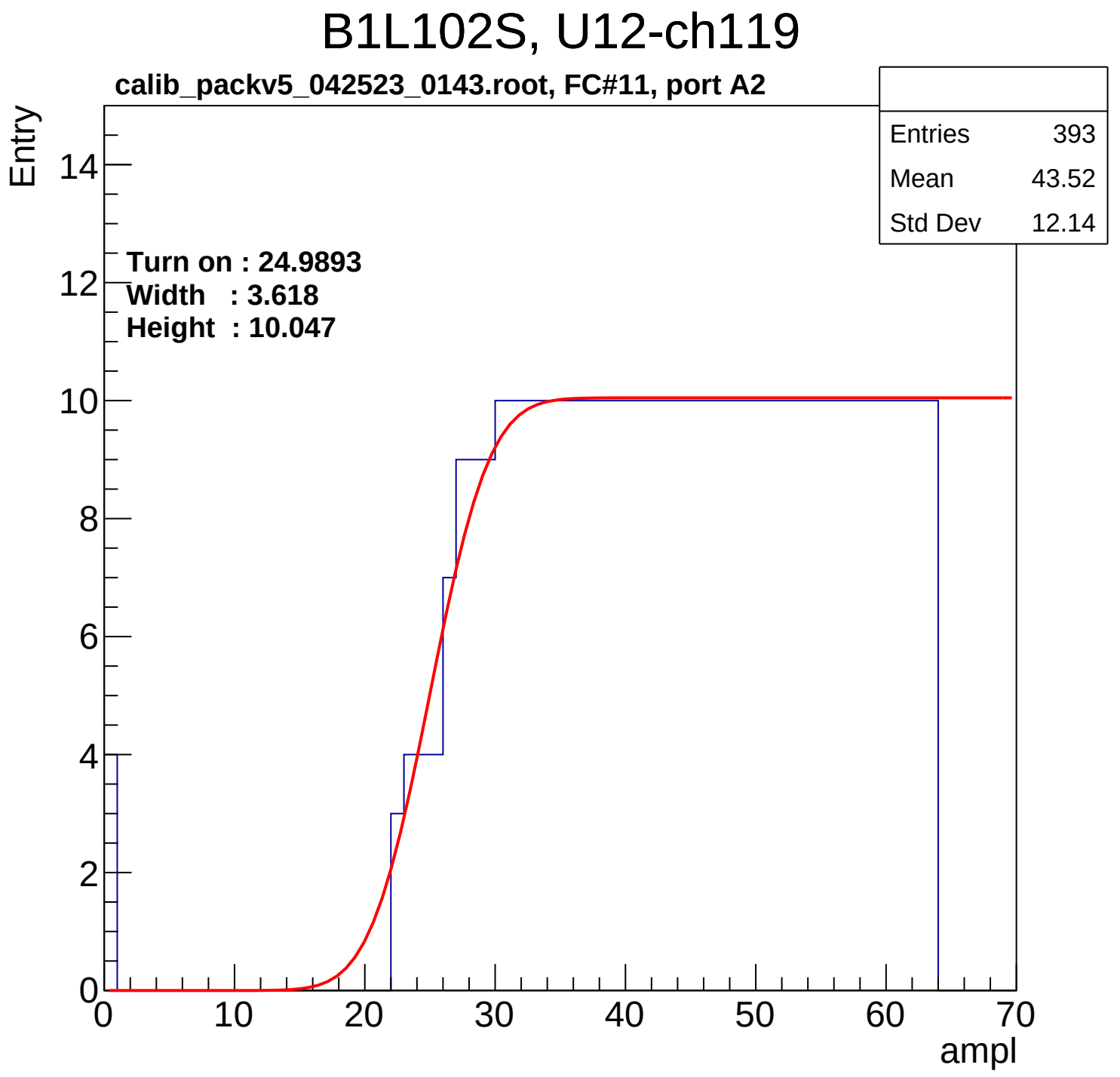
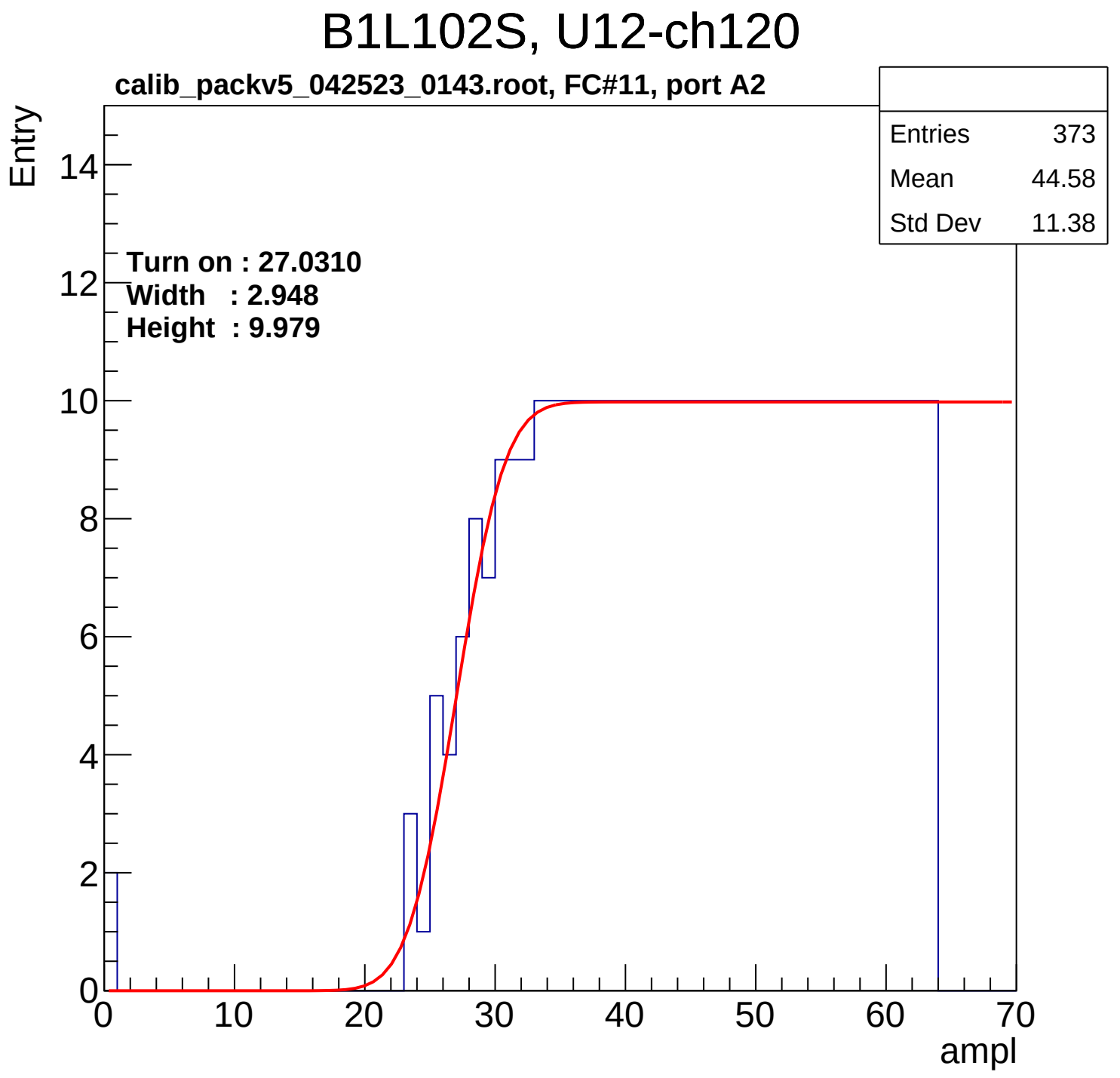

B1L102S, U12-ch119
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.52
Std Dev 12.14
Turn on : 24.9893
Width : 3.618
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U12-ch120
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.58
Std Dev 11.38
Turn on : 27.0310
Width : 2.948
Height : 9.979
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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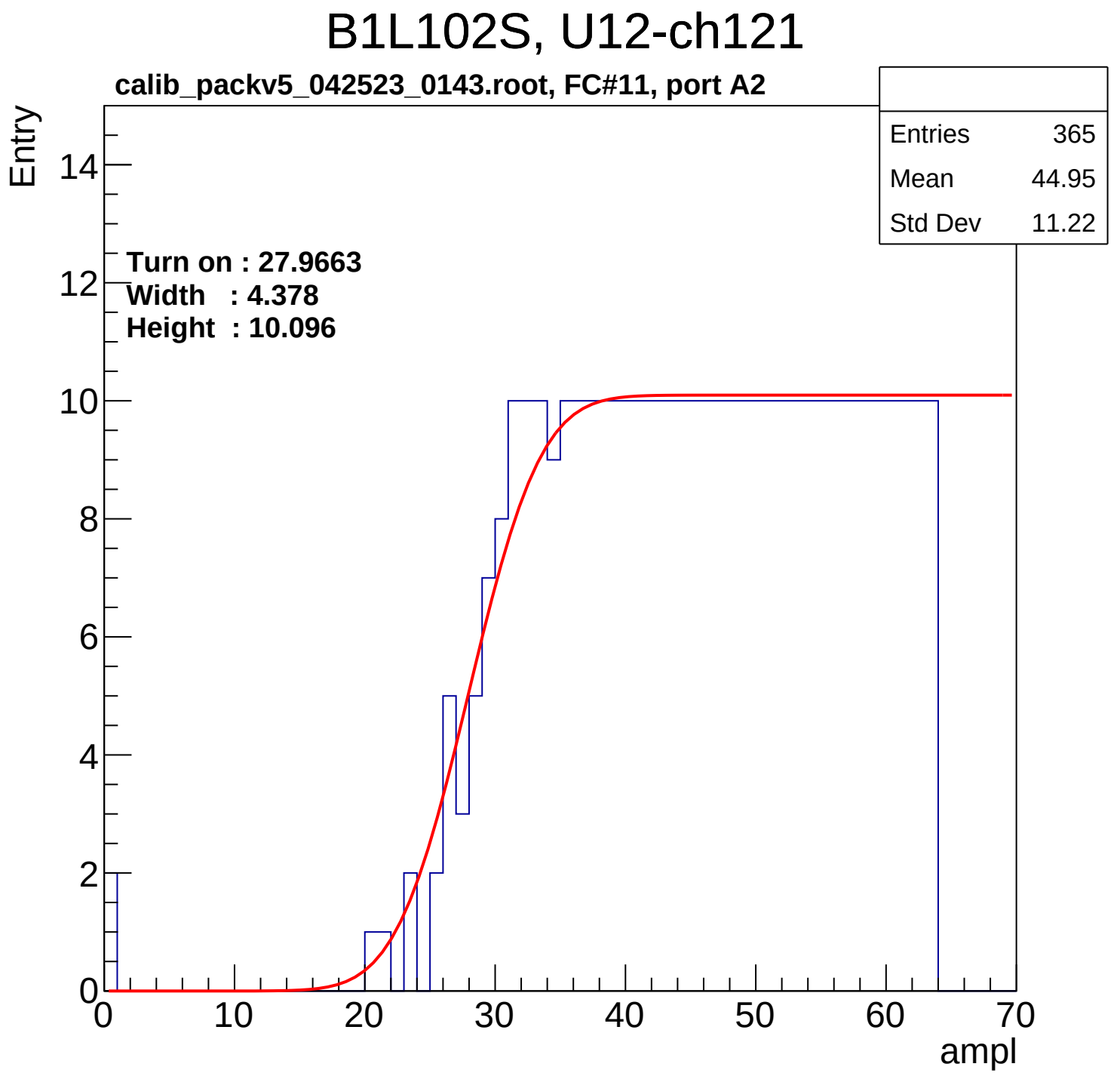
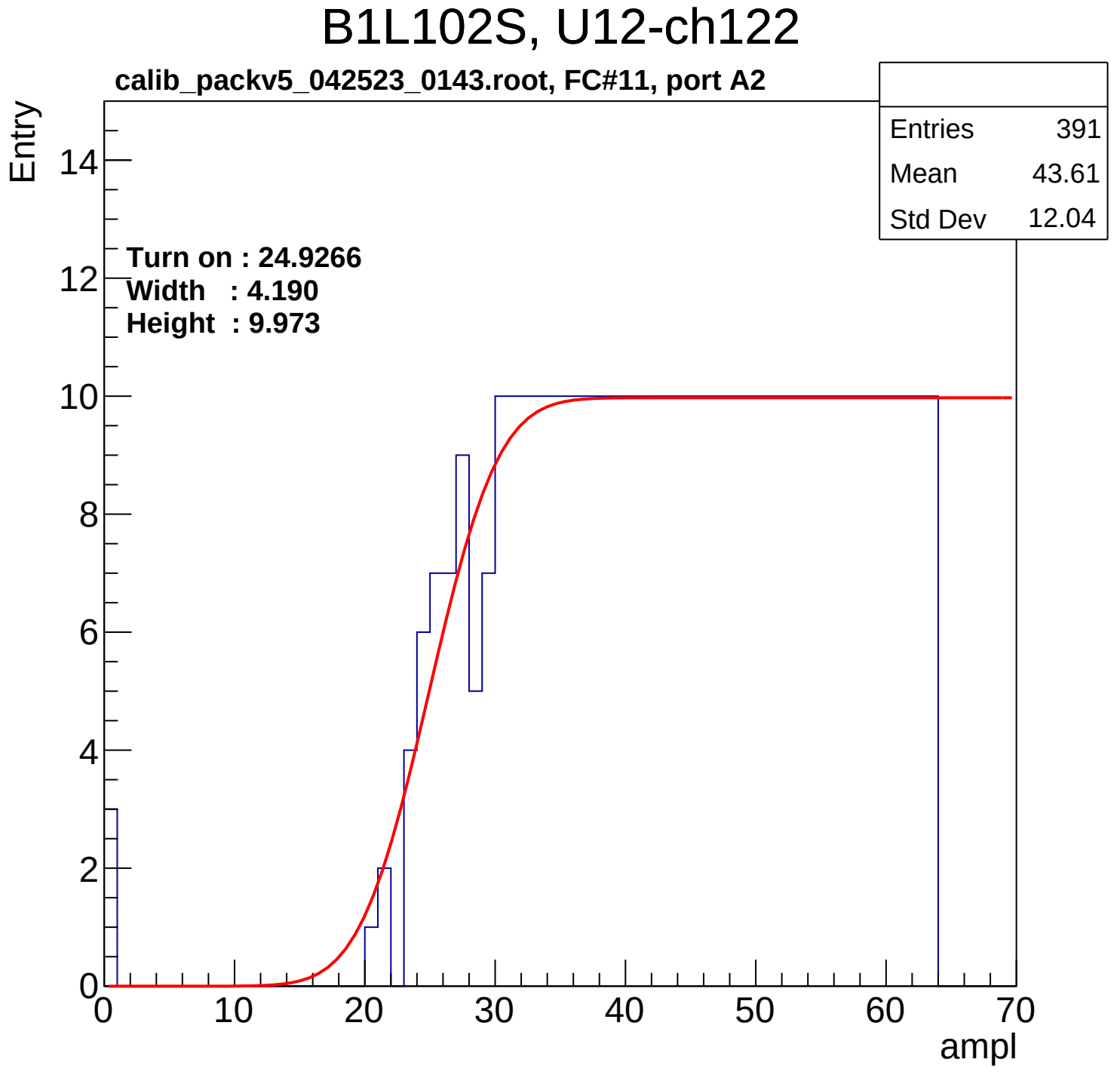

B1L102S, U12-ch121
calib_packv5_042523_0143.root, FC#11, port A2
Entries 365
Mean 44.95
Std Dev 11.22
Turn on : 27.9663
Width : 4.378
Height : 10.096
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U12-ch122
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.61
Std Dev 12.04
Turn on : 24.9266
Width : 4.190
Height : 9.973
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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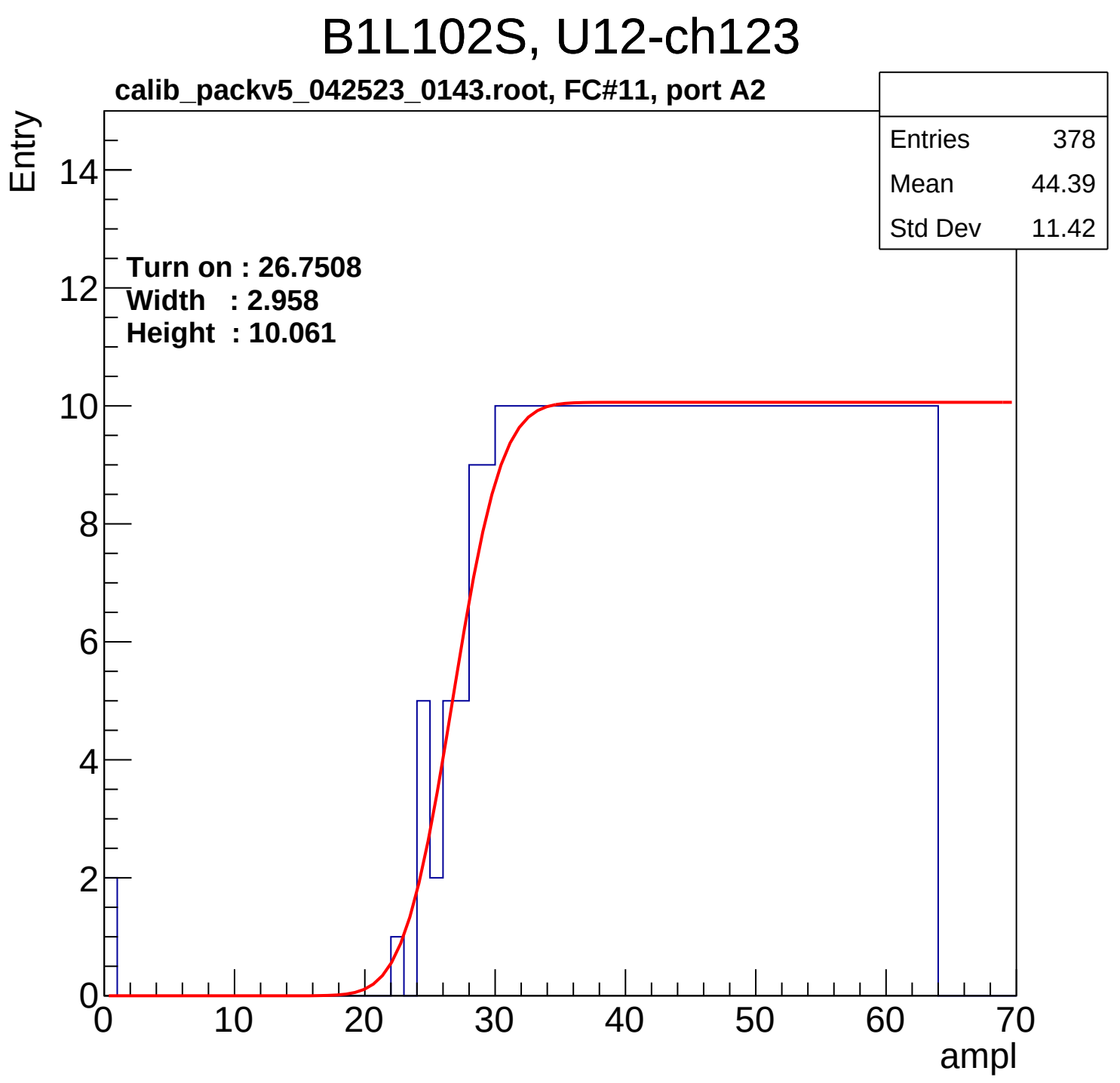
B1L102S, U12-ch123
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.39
Std Dev 11.42
Turn on : 26.7508
Width : 2.958
Height : 10.061
Entry
ampl
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2
4
6
8
10
12
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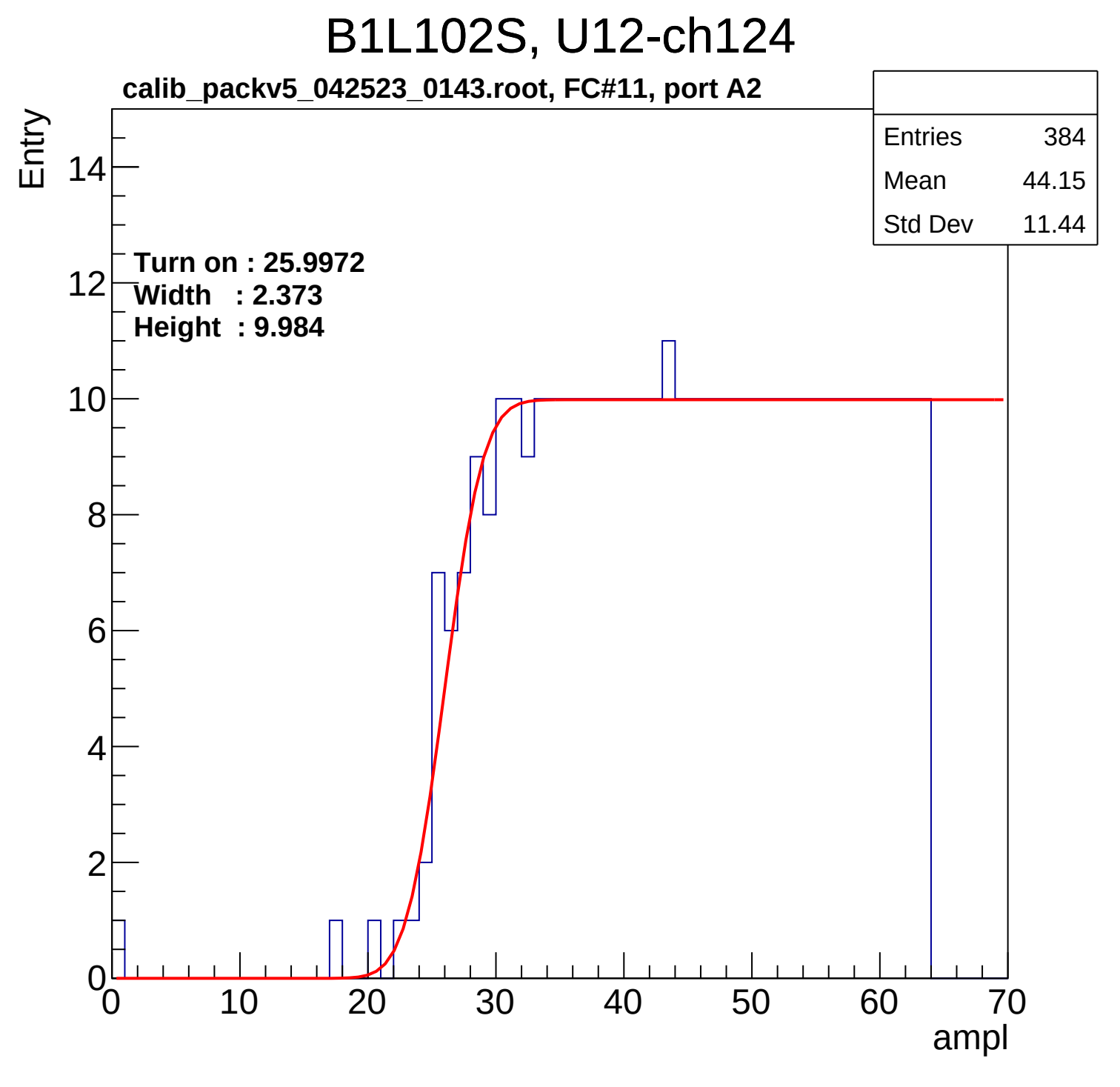
0
10
20
30
40
50
60
70


B1L102S, U12-ch124
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.15
Std Dev 11.44
Turn on : 25.9972
Width : 2.373
Height : 9.984
Entry
ampl
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4
6
8
10
12
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0
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20
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40
50
60
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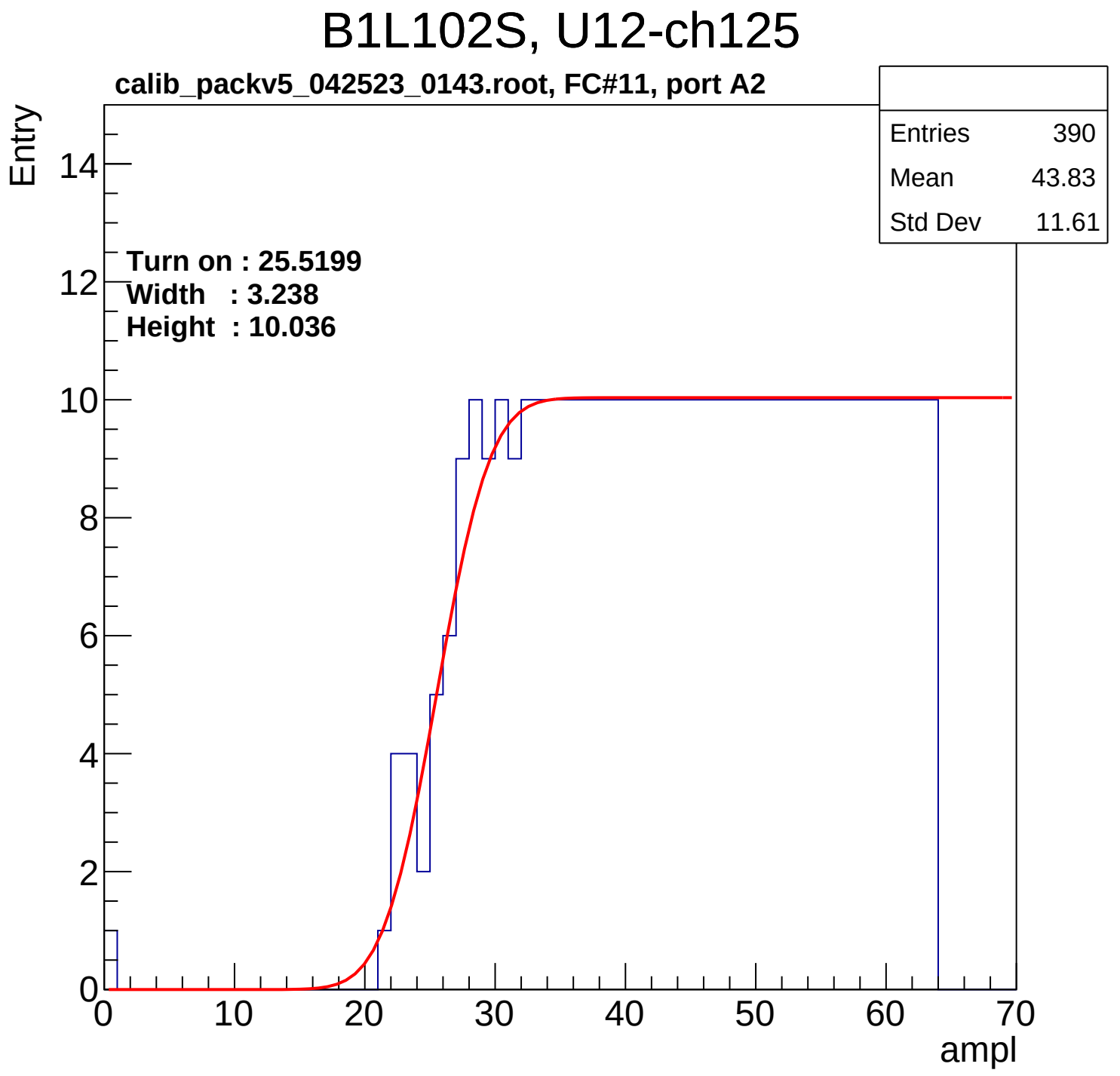
B1L102S, U12-ch125
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.83
Std Dev 11.61
Turn on : 25.5199
Width : 3.238
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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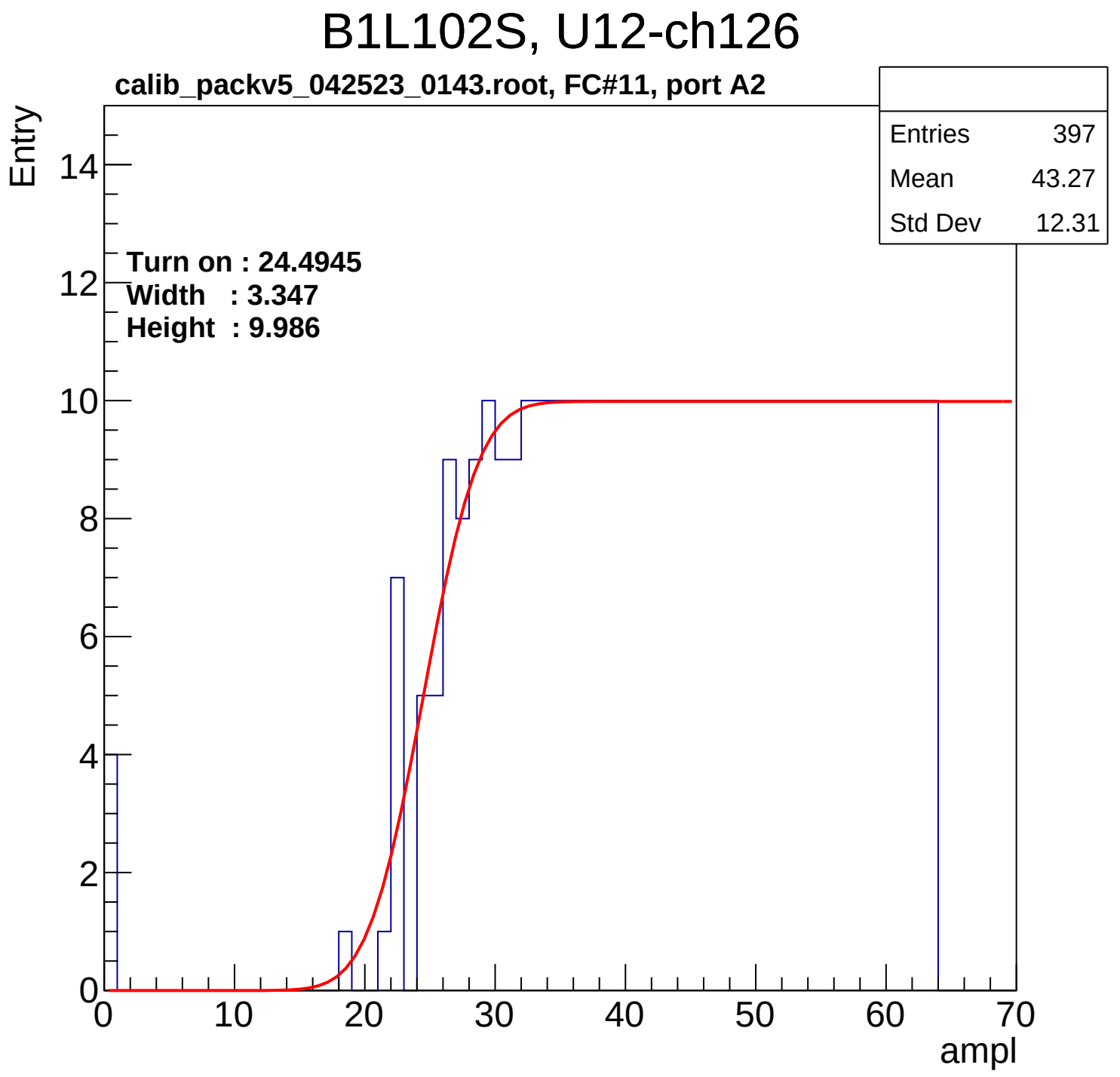
40
50
60
70


B1L102S, U12-ch126
calib_packv5_042523_0143.root, FC#11, port A2
Entries 397
Mean 43.27
Std Dev 12.31
Turn on : 24.4945
Width : 3.347
Height : 9.986
Entry
ampl
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2
4
6
8
10
12
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0
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40
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60
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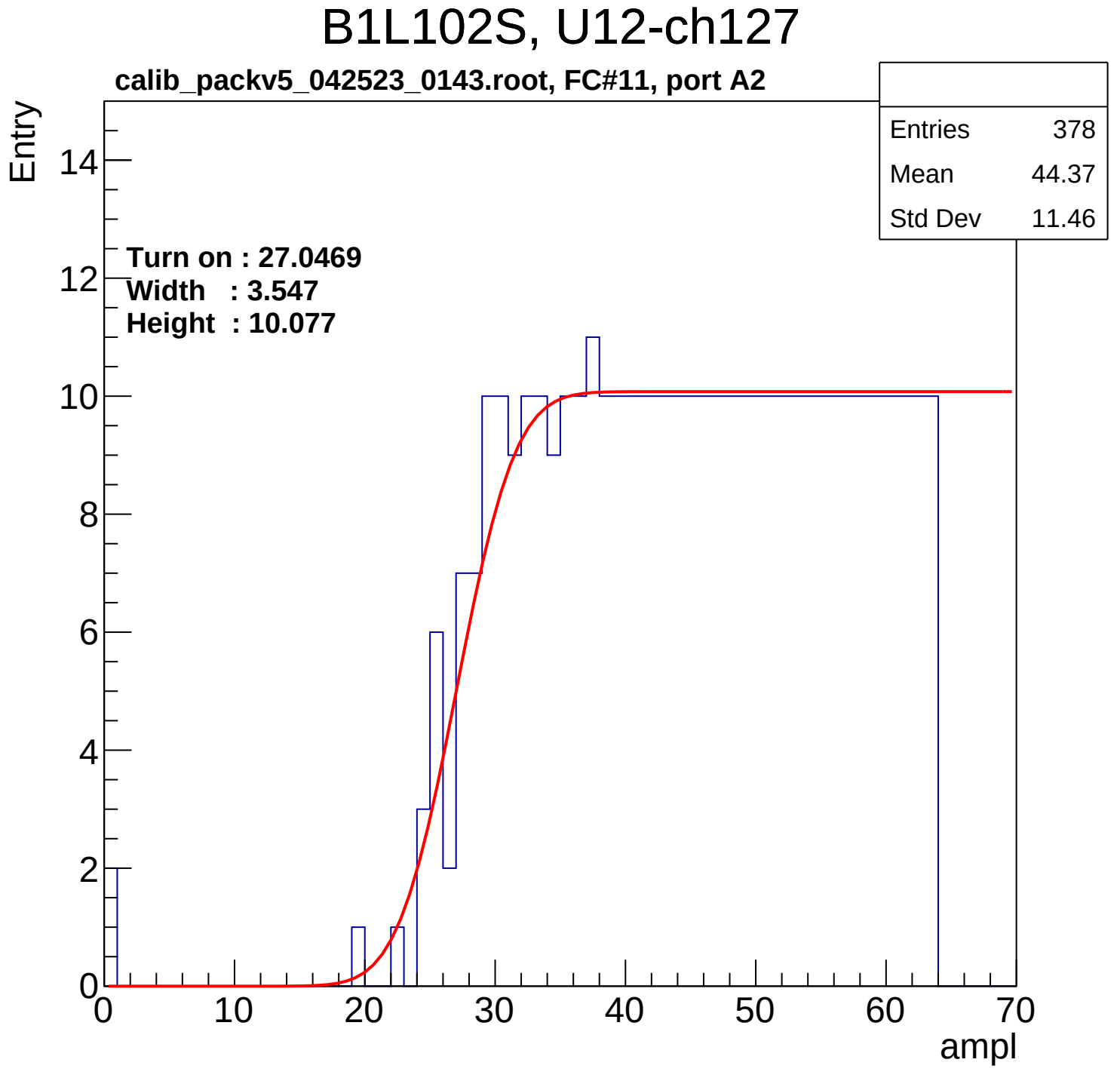
B1L102S, U12-ch127
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.37
Std Dev 11.46
Turn on : 27.0469
Width : 3.547
Height : 10.077
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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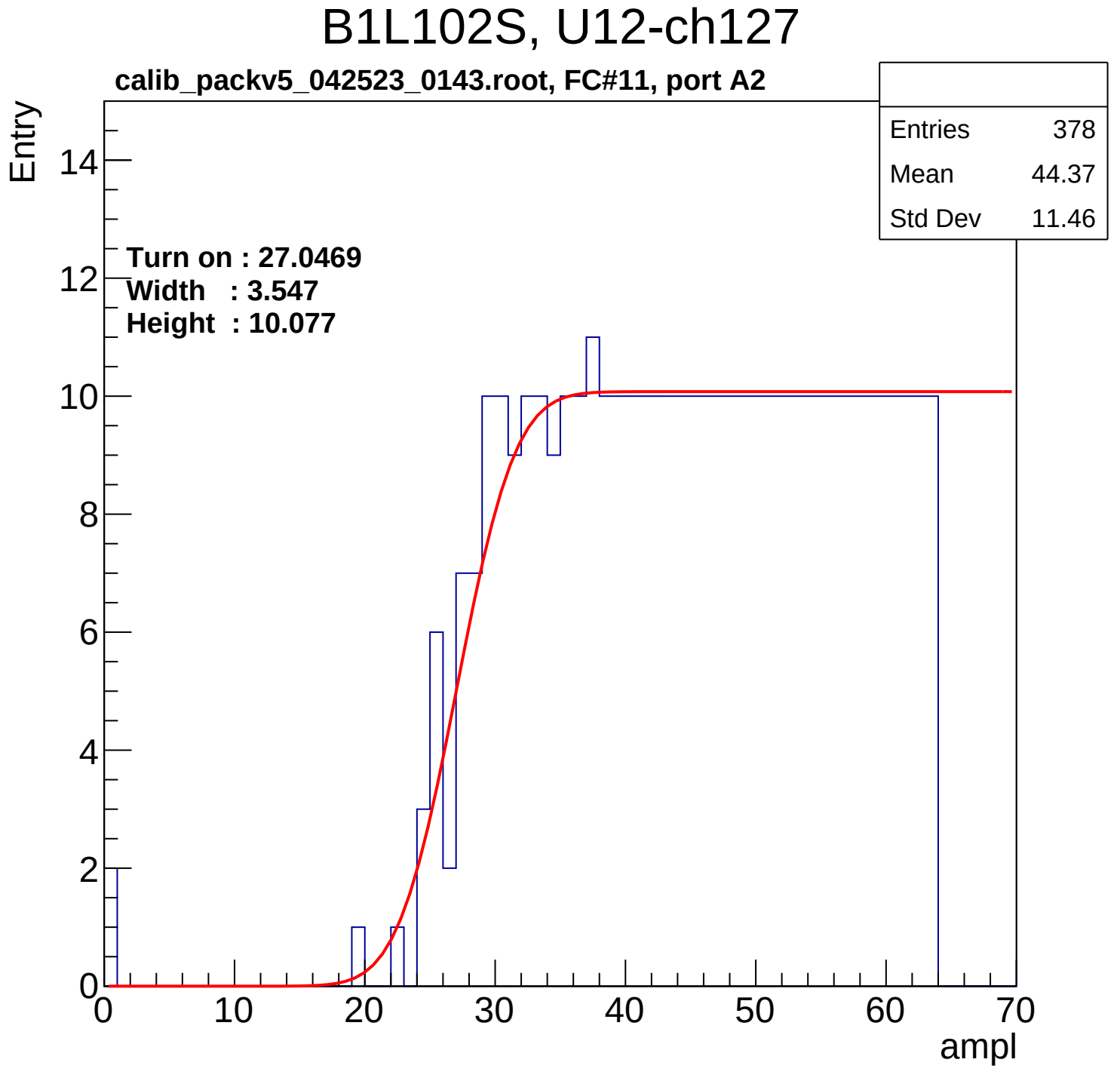
60
70


B1L102S, U12-ch127
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.37
Std Dev 11.46
Turn on : 27.0469
Width : 3.547
Height : 10.077
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70