

B1L103S, U19-ch0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	456
Mean	38.01
Std Dev	17.99

Turn on : 24.4477

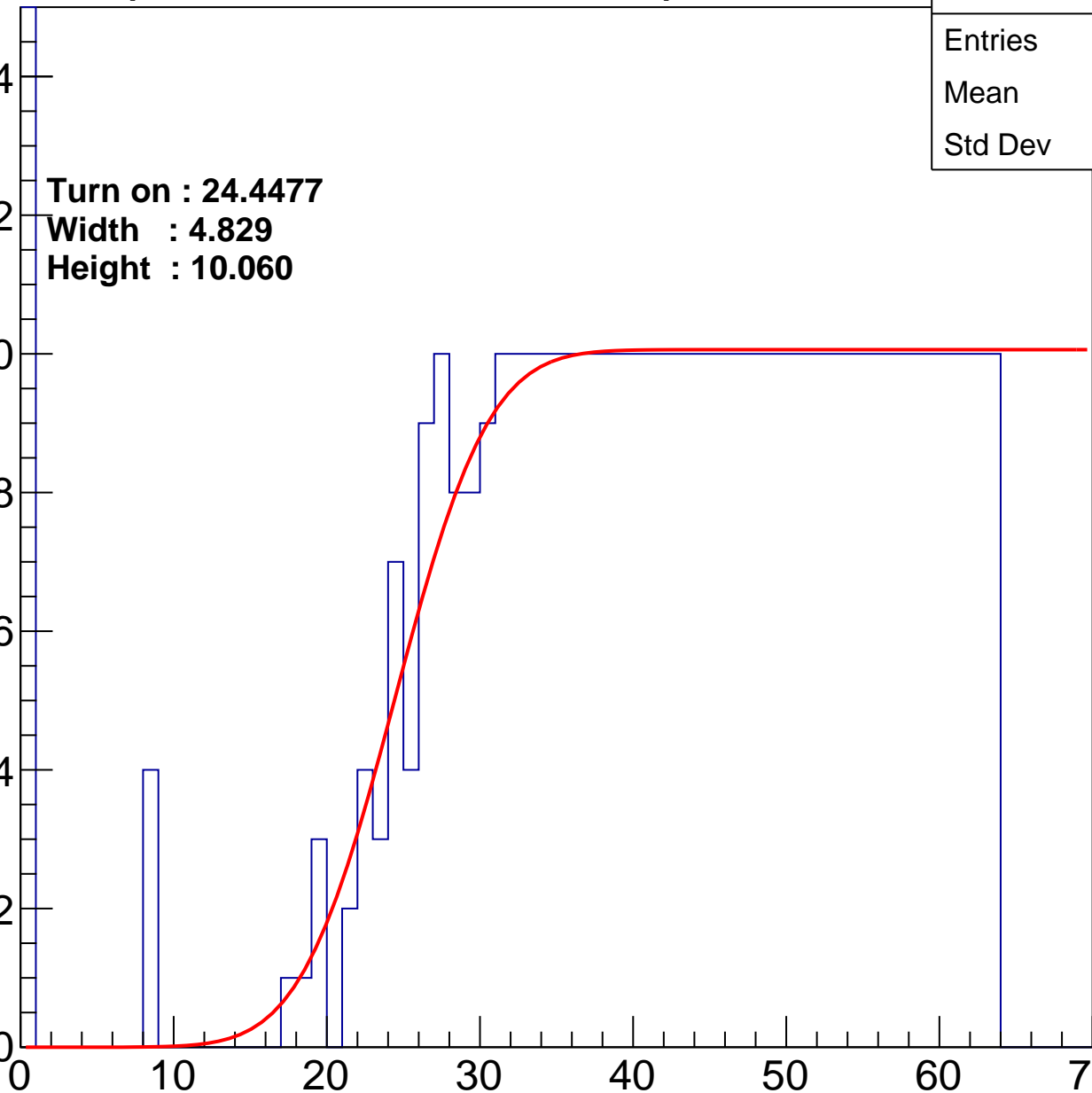
Width : 4.829

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	39.96
Std Dev	17.27

Turn on : 27.1262

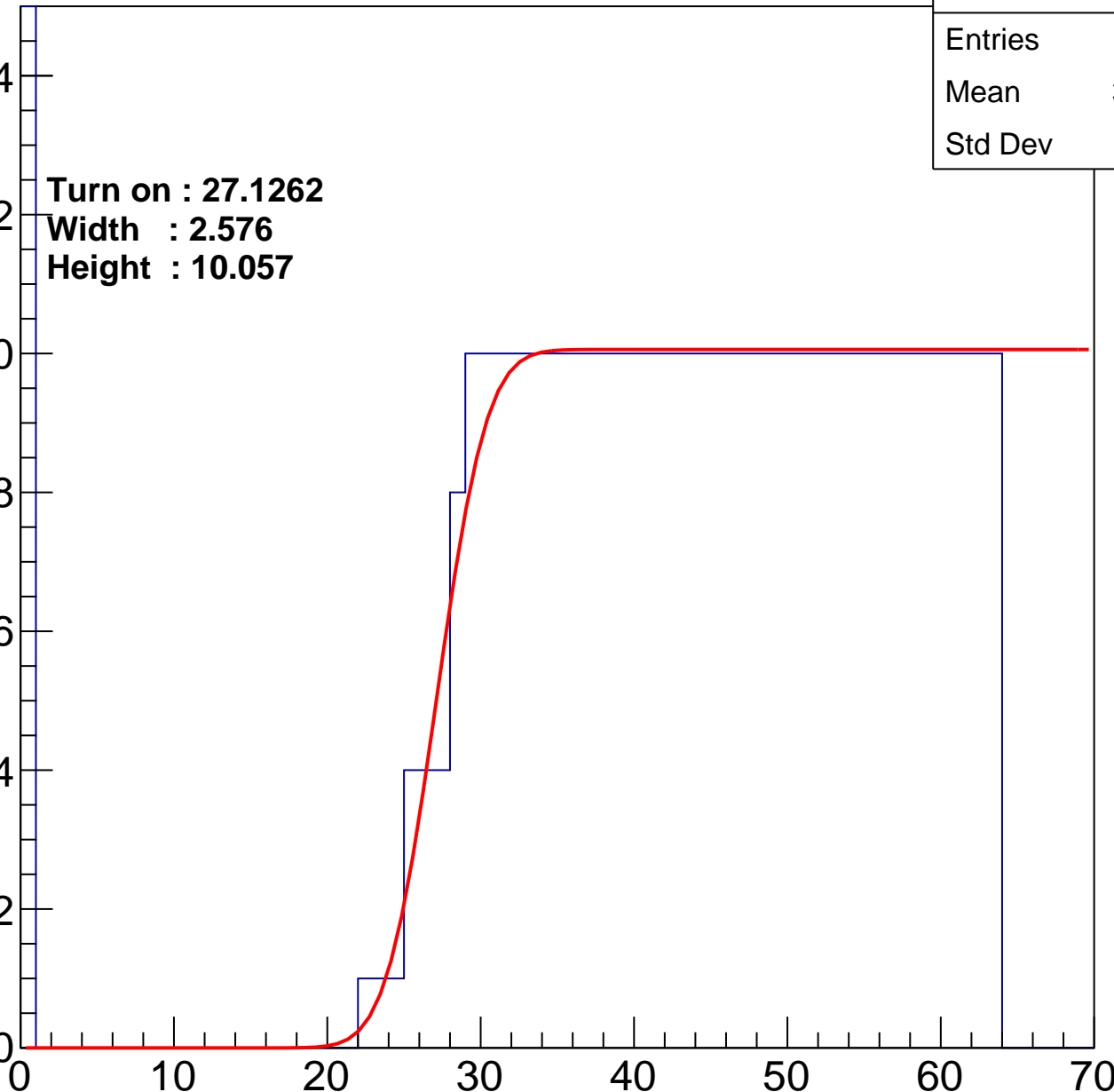
Width : 2.576

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	39.45
Std Dev	17.3

Turn on : 25.1463

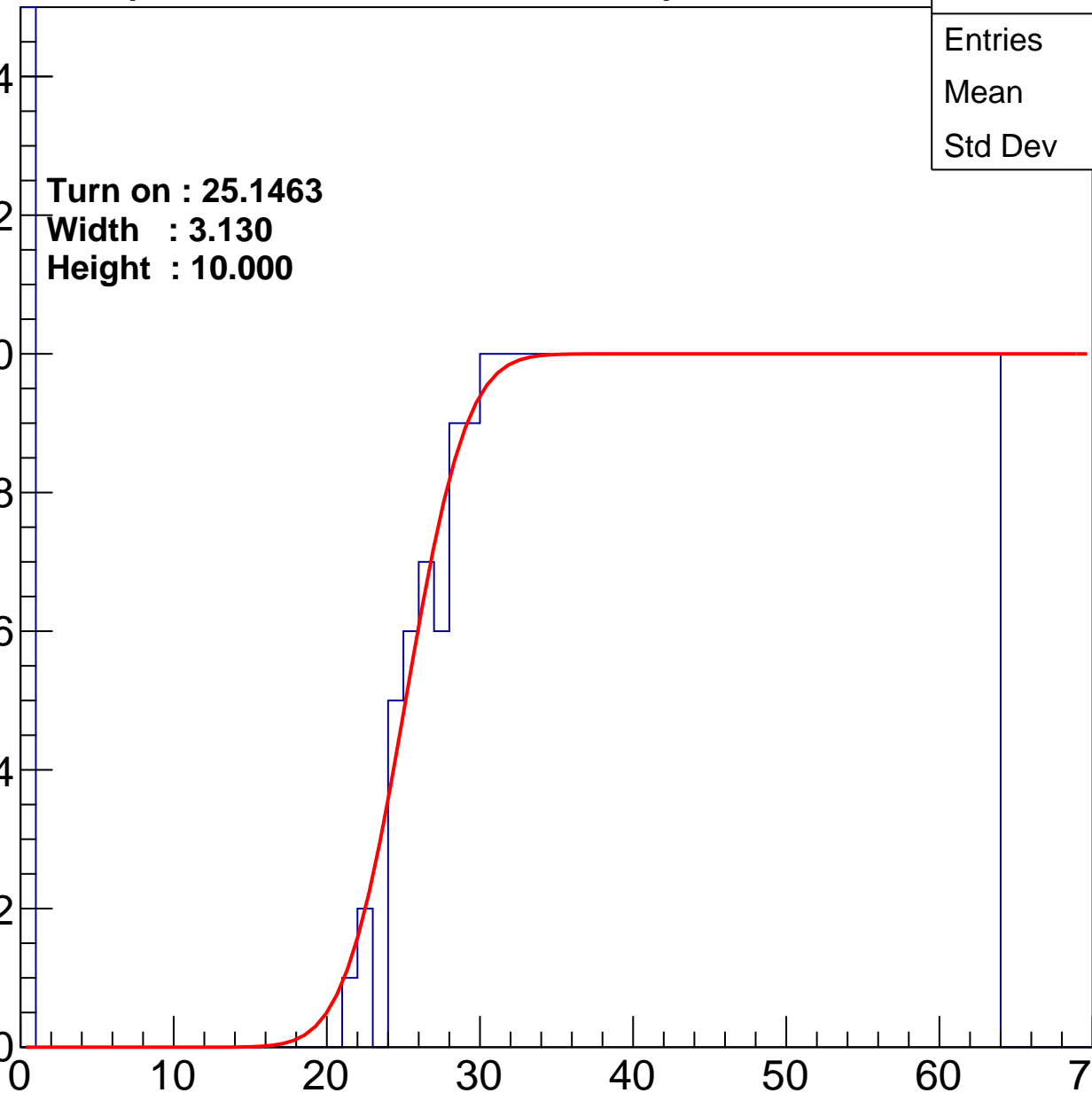
Width : 3.130

Height : 10.000

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	421
Mean	39.36
Std Dev	18

Turn on : 27.6874

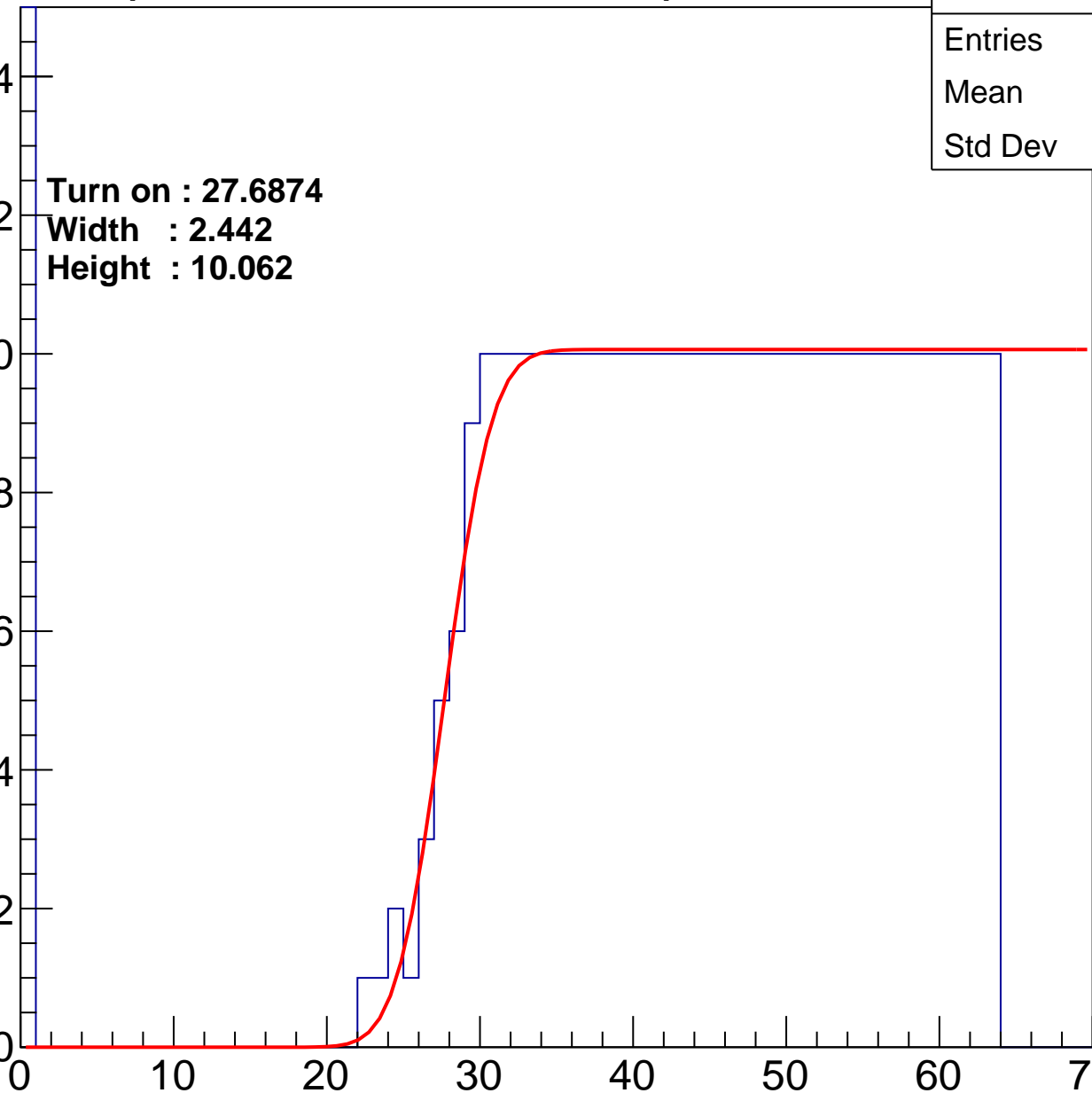
Width : 2.442

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	441
Mean	39.47
Std Dev	16.66

Turn on : 24.4213

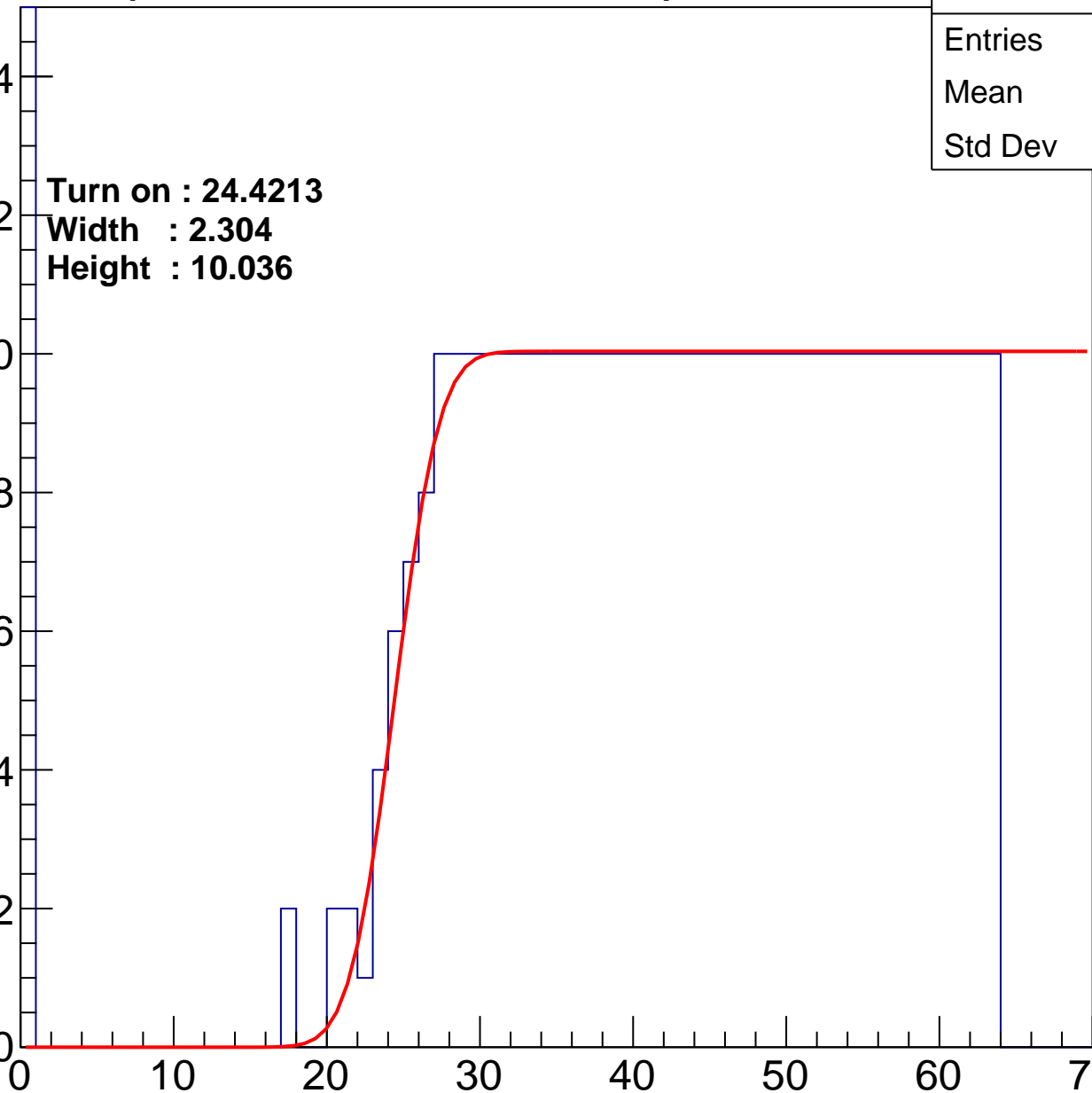
Width : 2.304

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch5

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	39.15
Std Dev	17.28

Turn on : 24.8600

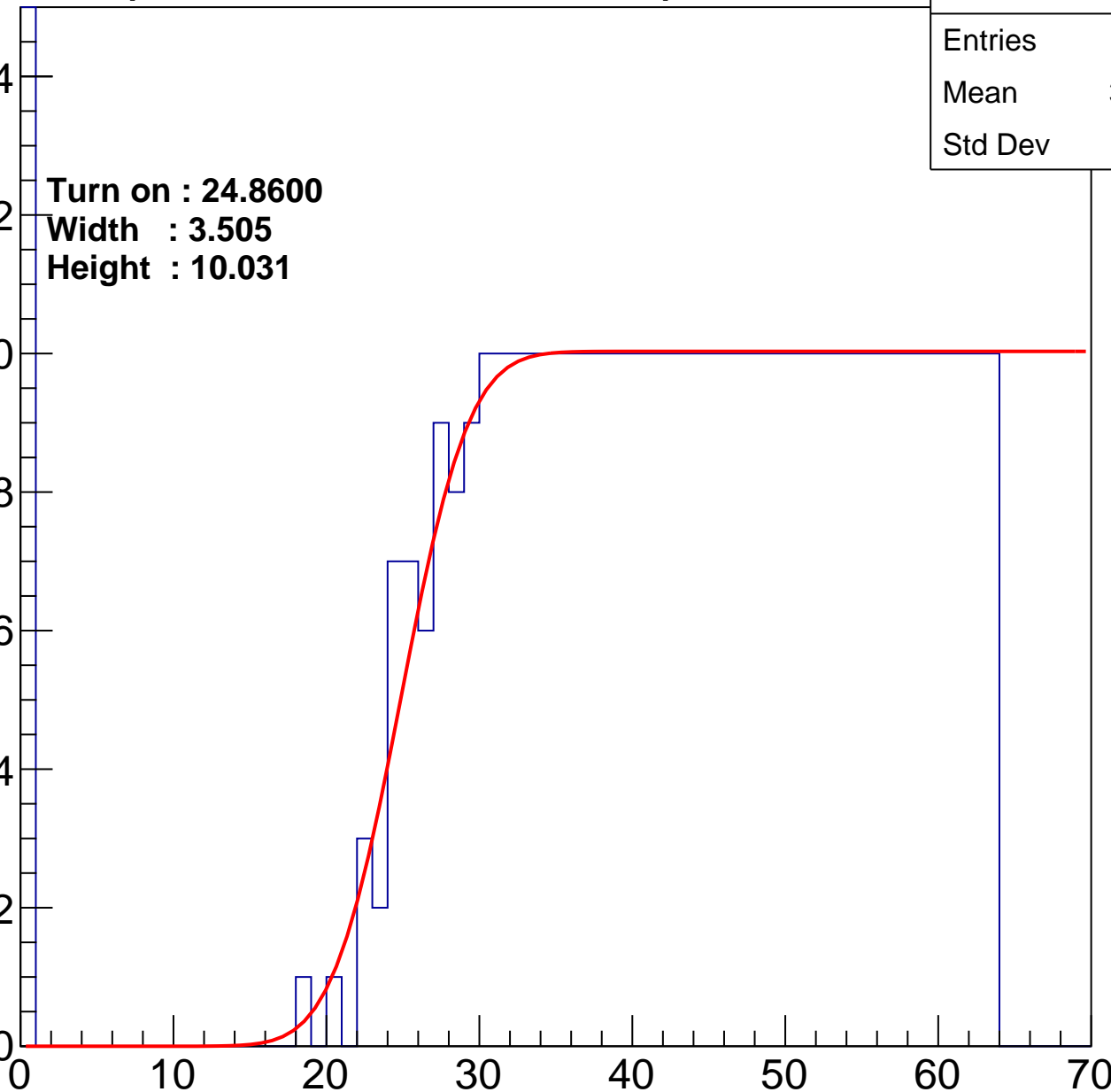
Width : 3.505

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch6

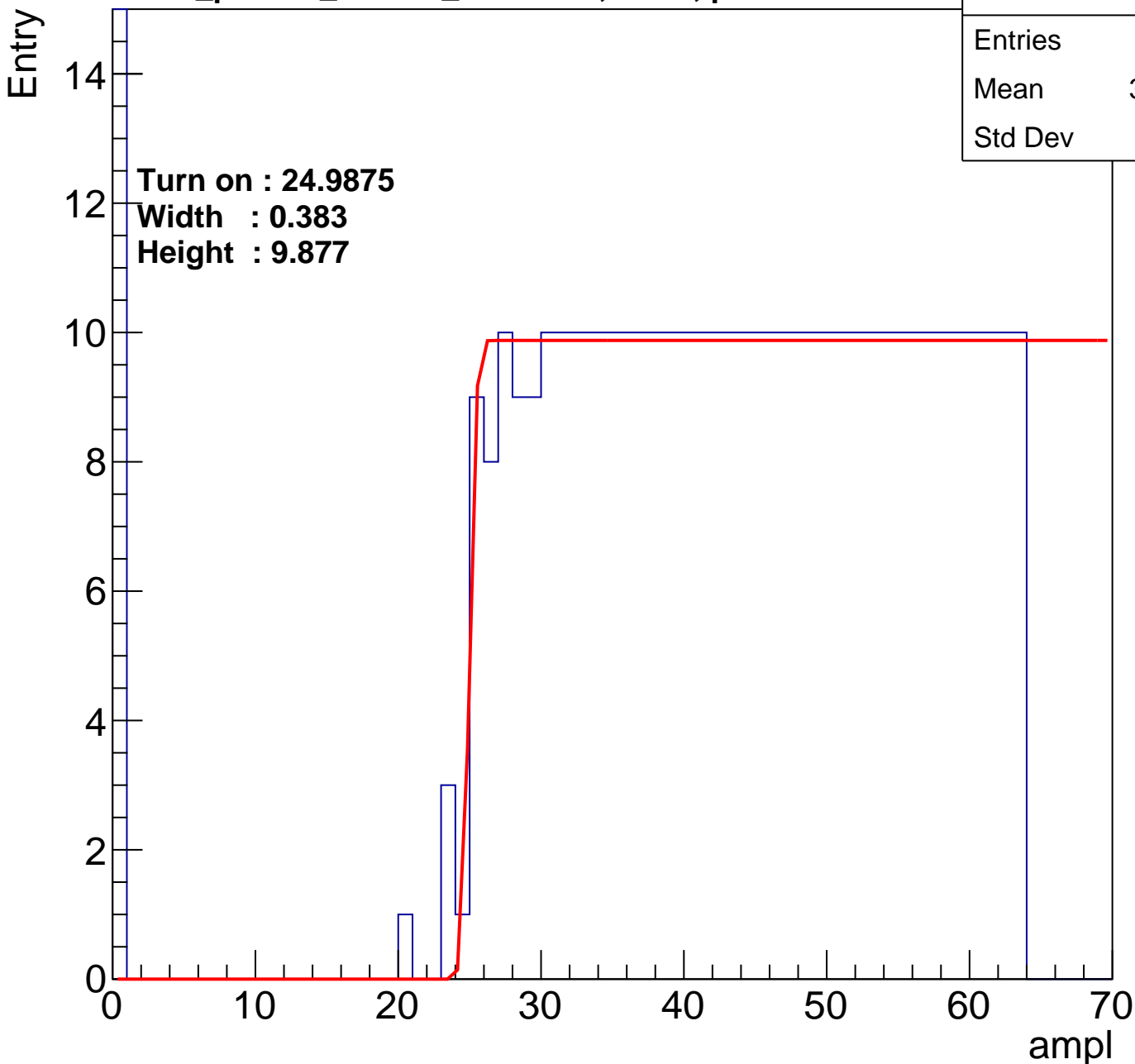
calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	39.13
Std Dev	17.41

Turn on : 24.9875

Width : 0.383

Height : 9.877



B1L103S, U19-ch7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	422
Mean	39.73
Std Dev	17.37

Turn on : 26.4727

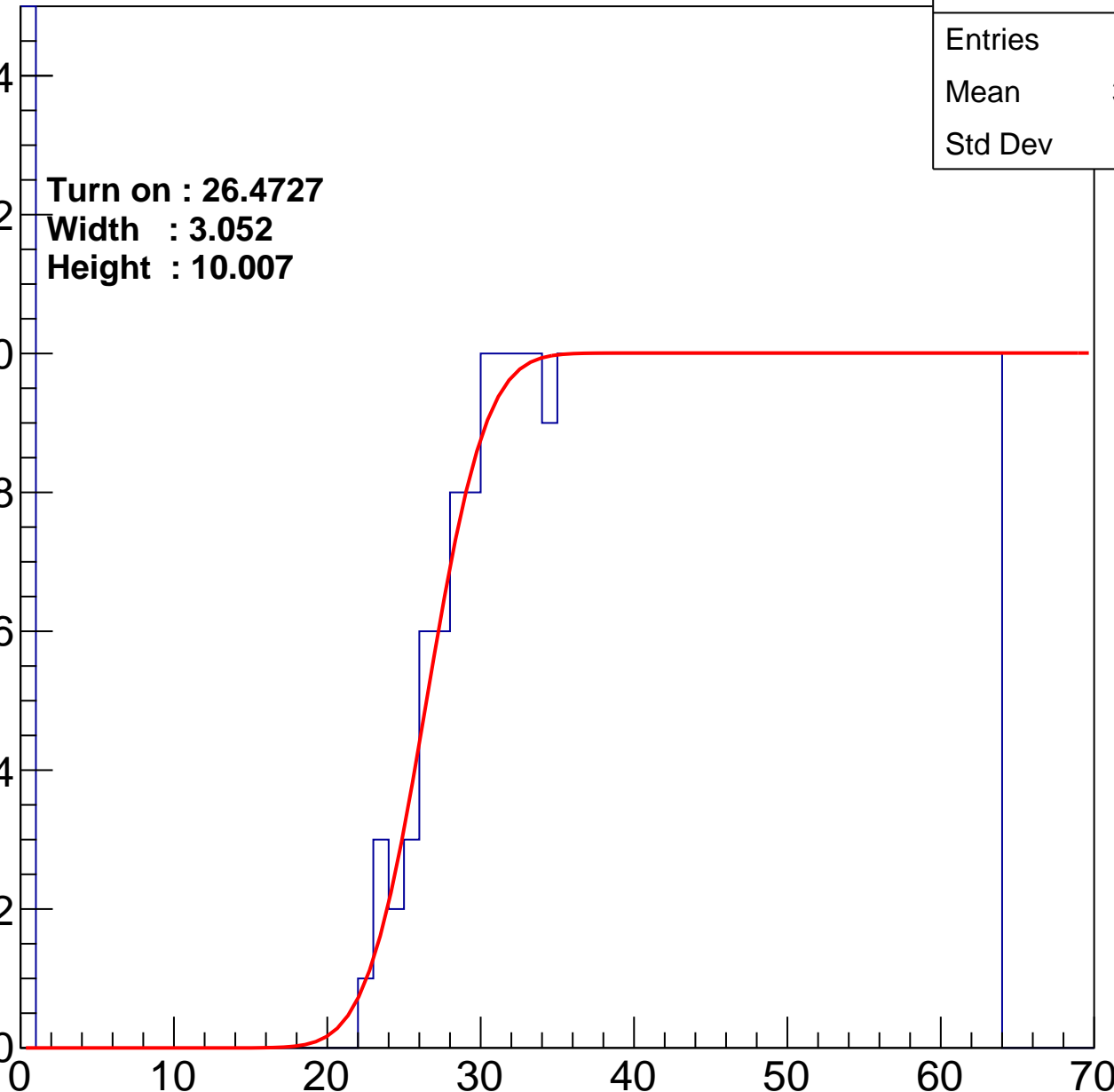
Width : 3.052

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch8

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	40.2
Std Dev	16.15

Turn on : 24.8564

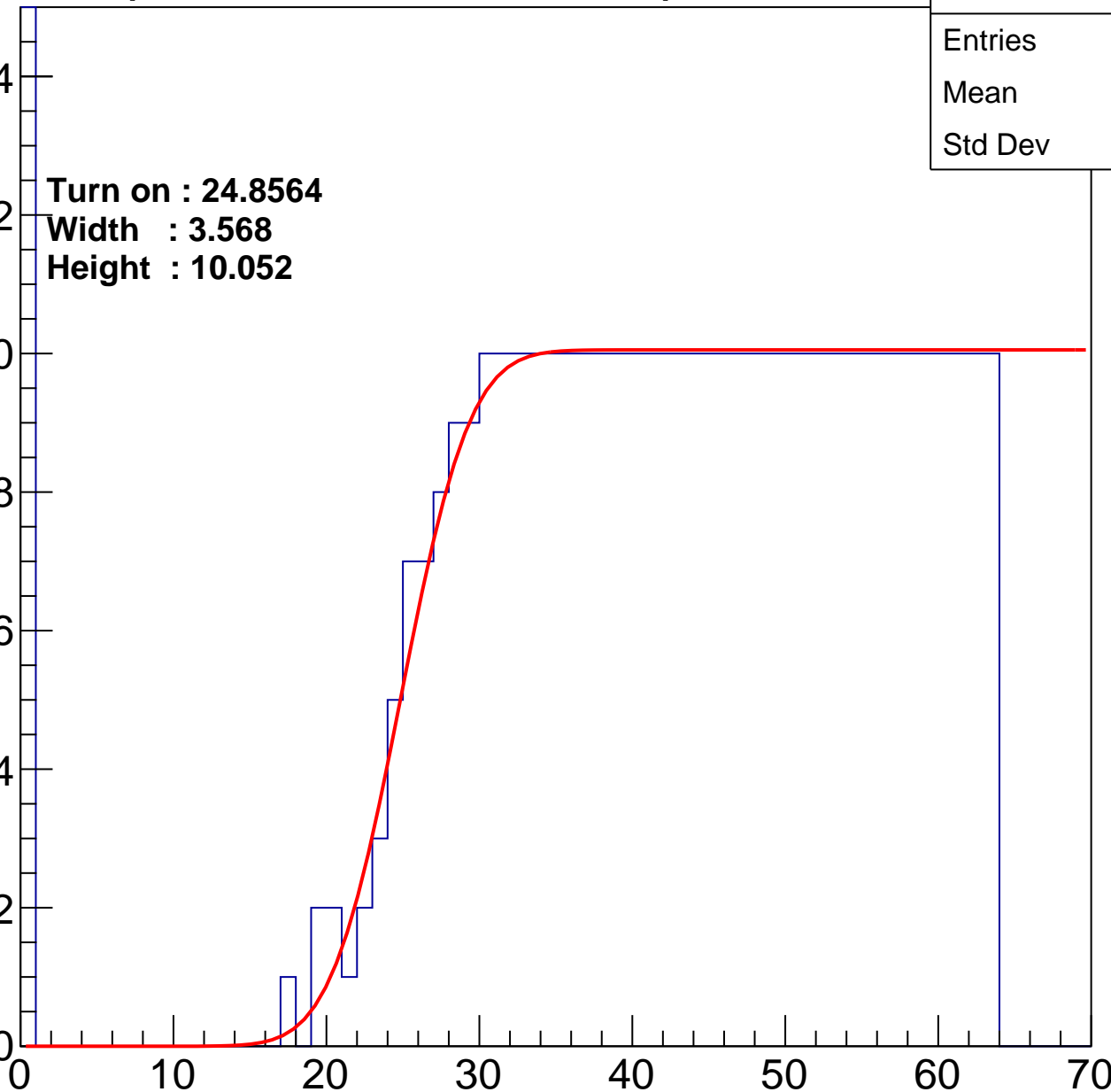
Width : 3.568

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch9

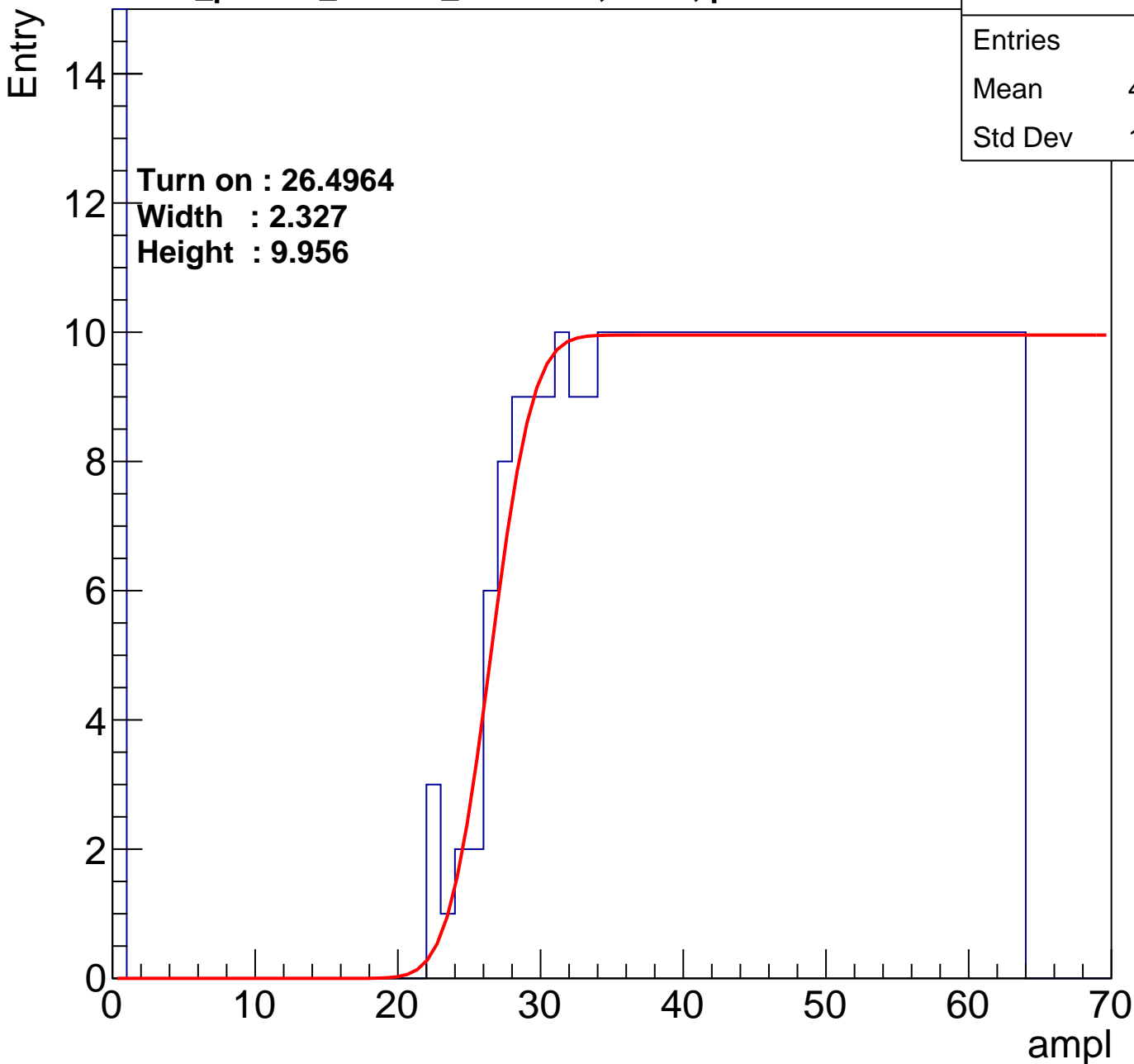
calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	40.16
Std Dev	16.92

Turn on : 26.4964

Width : 2.327

Height : 9.956



B1L103S, U19-ch10

calib_packv5_041523_1651.root, FC#0, port C2

Entries	415
Mean	39.98
Std Dev	17.4

Turn on : 27.2348

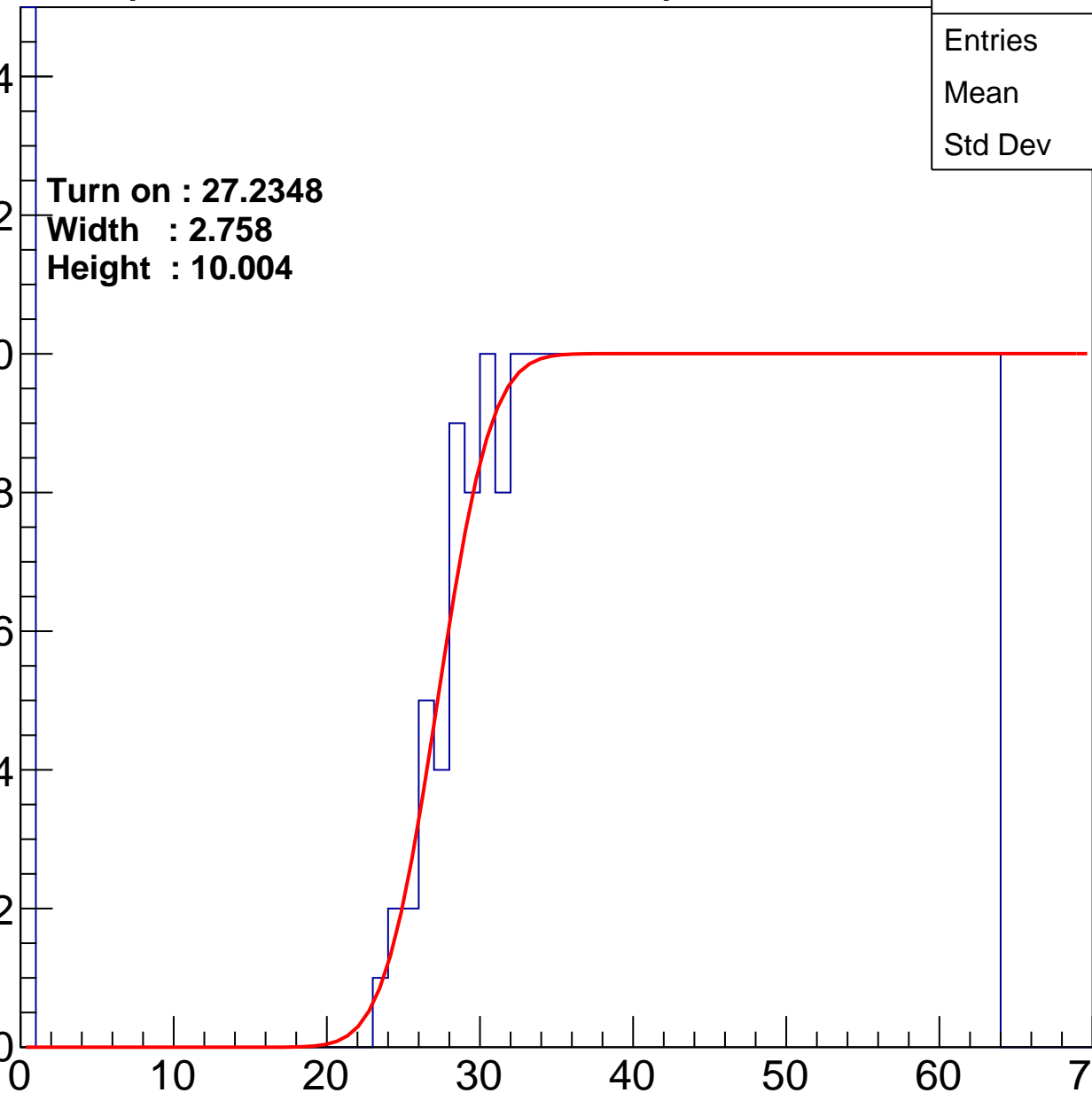
Width : 2.758

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch11

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	40.64
Std Dev	16.28

Turn on : 25.7815

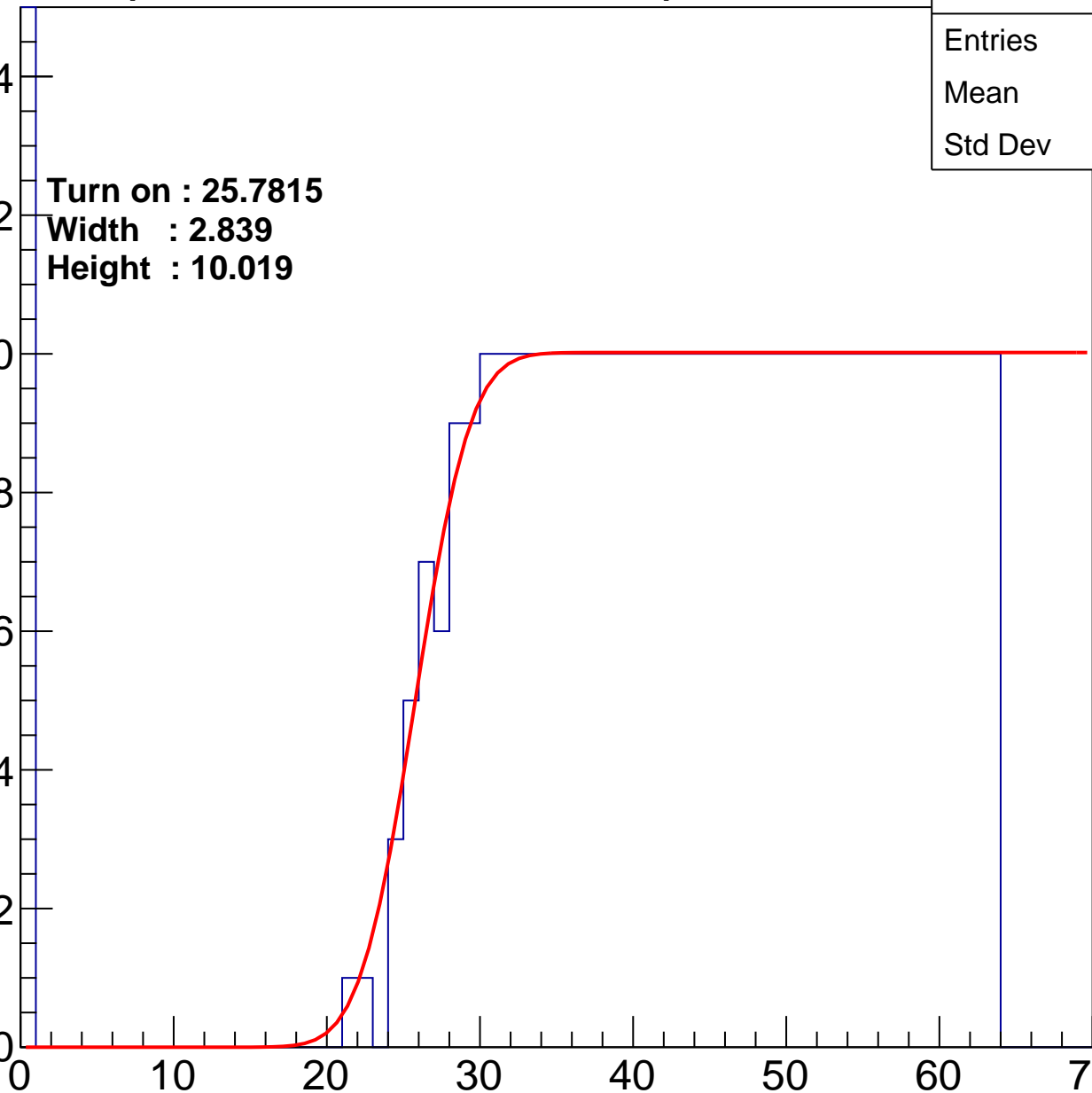
Width : 2.839

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch12

calib_packv5_041523_1651.root, FC#0, port C2

Entries	421
Mean	40.26
Std Dev	16.59

Turn on : 25.8460

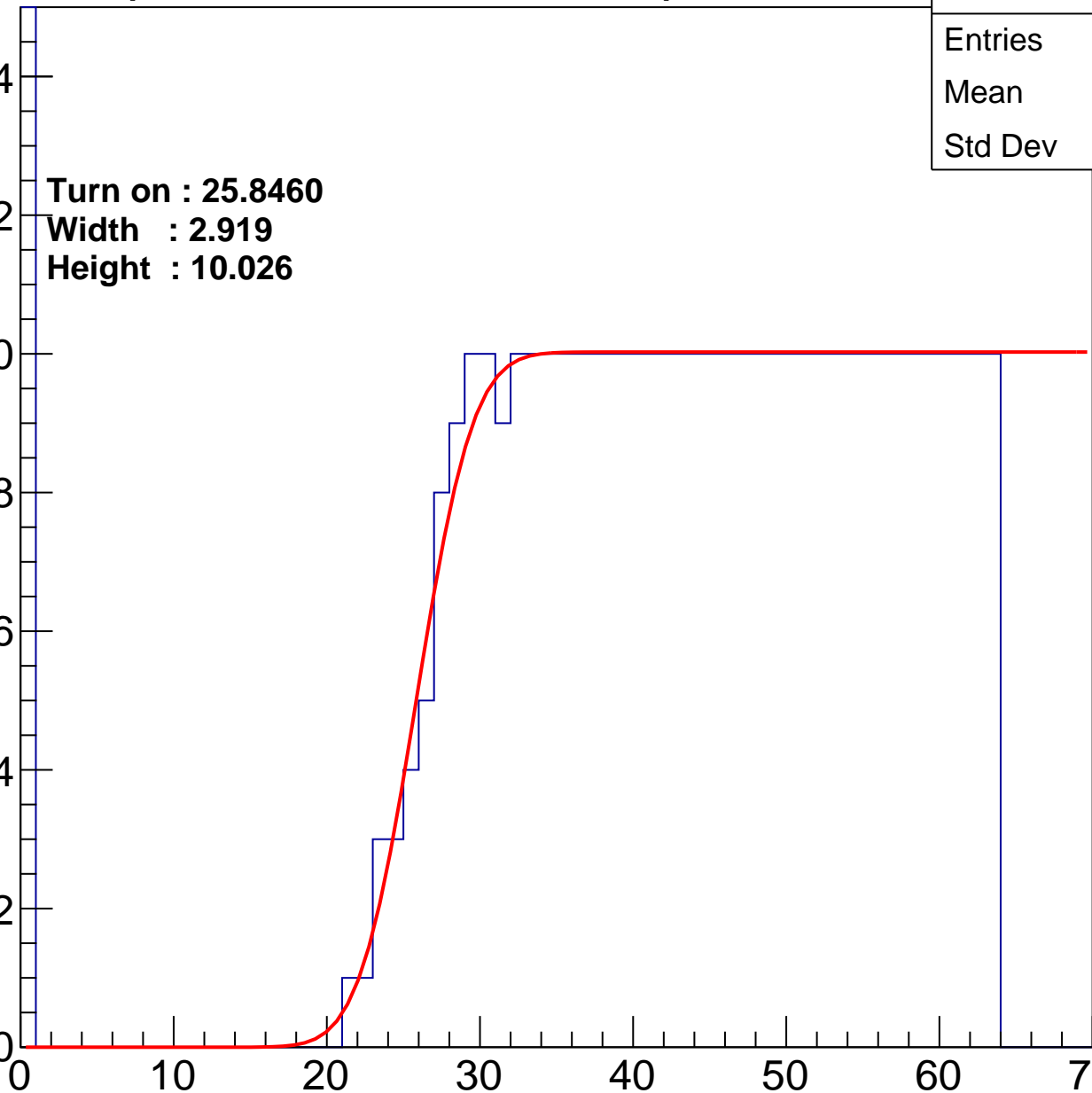
Width : 2.919

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch13

calib_packv5_041523_1651.root, FC#0, port C2

Entries	409
Mean	40.7
Std Dev	16.62

Turn on : 26.7501

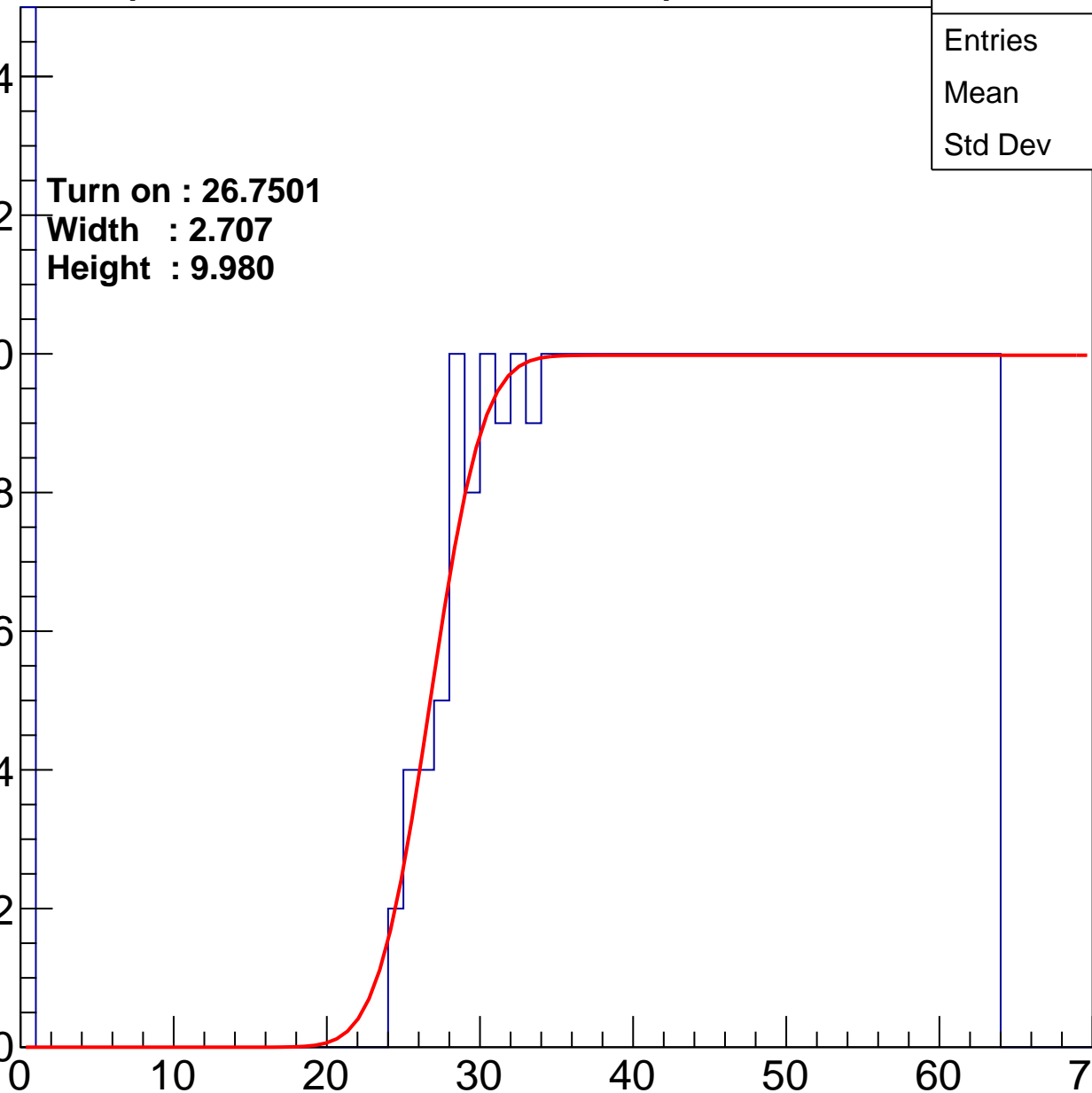
Width : 2.707

Height : 9.980

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch14

calib_packv5_041523_1651.root, FC#0, port C2

Entries	413
Mean	40.13
Std Dev	17.26

Turn on : 27.5594

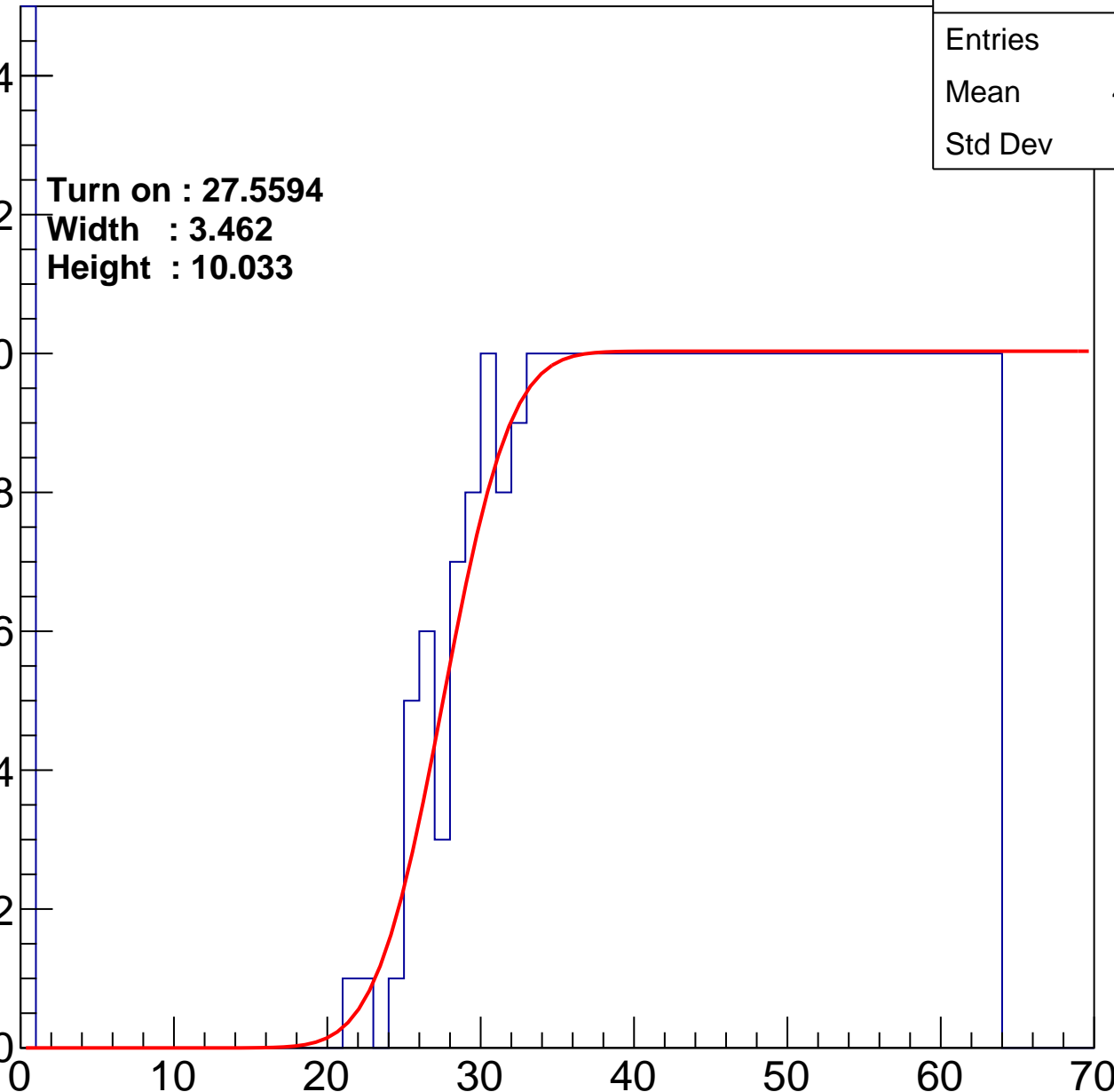
Width : 3.462

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch15

calib_packv5_041523_1651.root, FC#0, port C2

Entries	425
Mean	39.94
Std Dev	16.82

Turn on : 25.7881

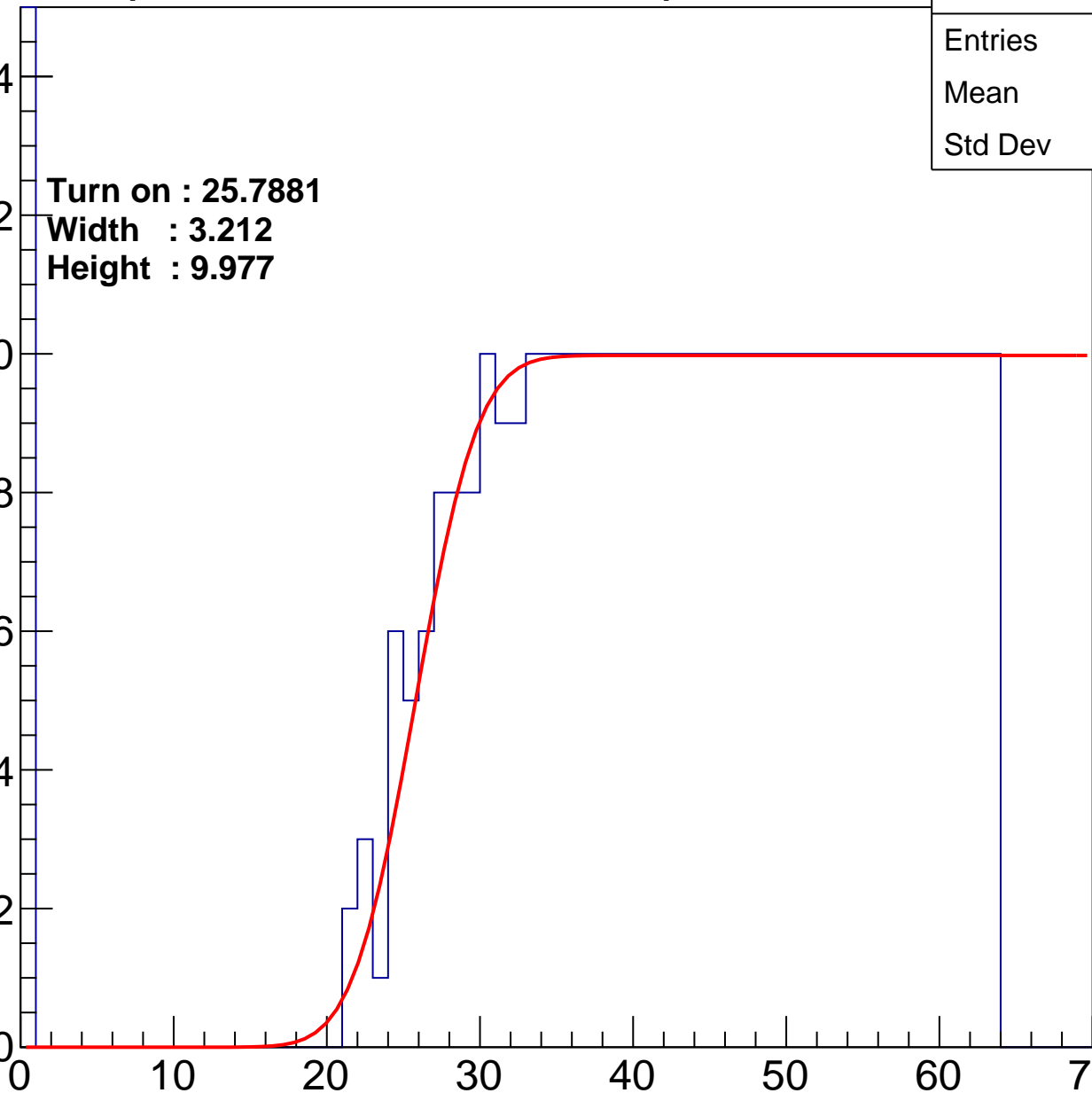
Width : 3.212

Height : 9.977

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch16

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.8
Std Dev	16.96

Turn on : 26.3878

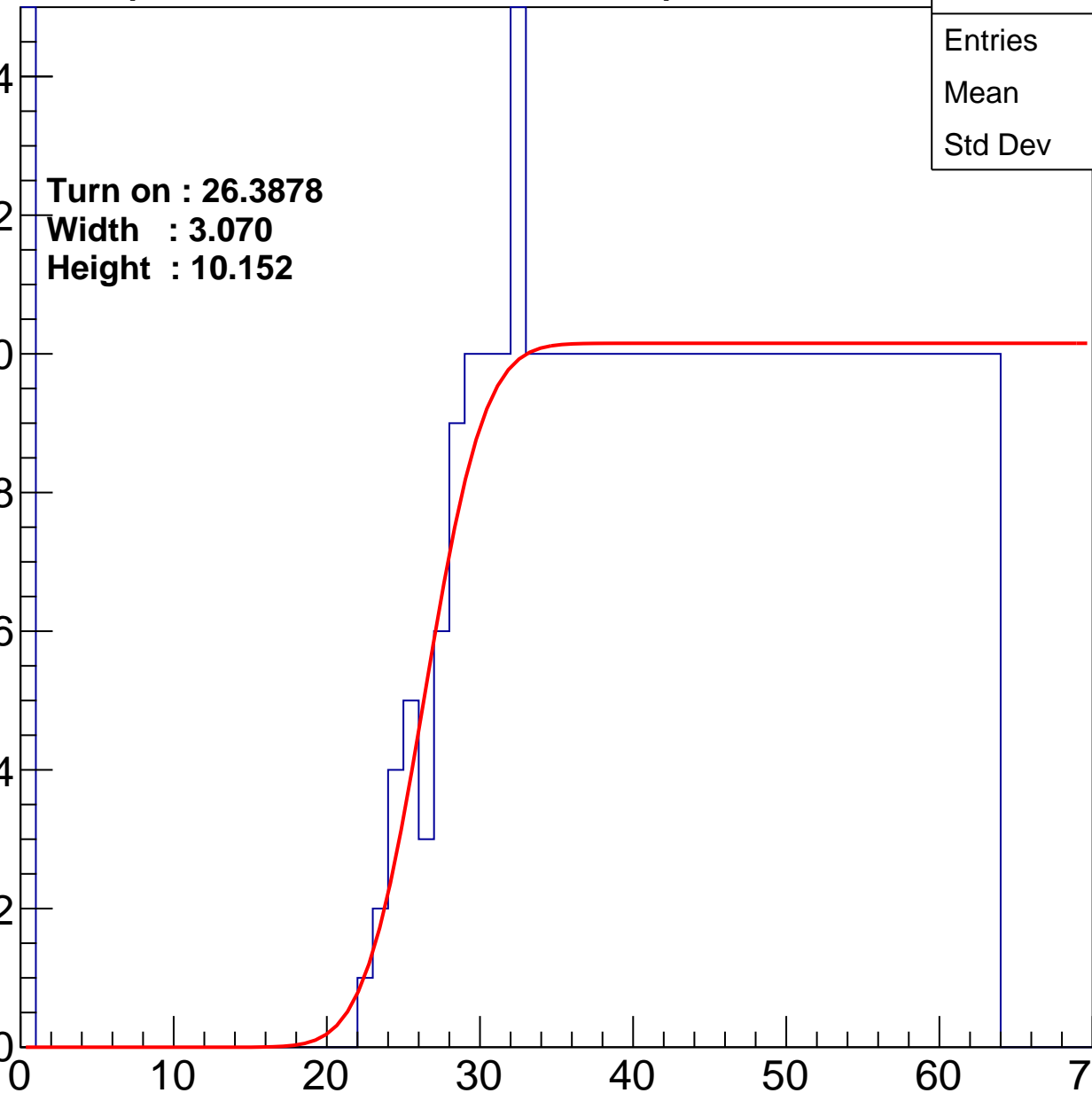
Width : 3.070

Height : 10.152

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch17

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.55
Std Dev	17.24

Turn on : 25.7437

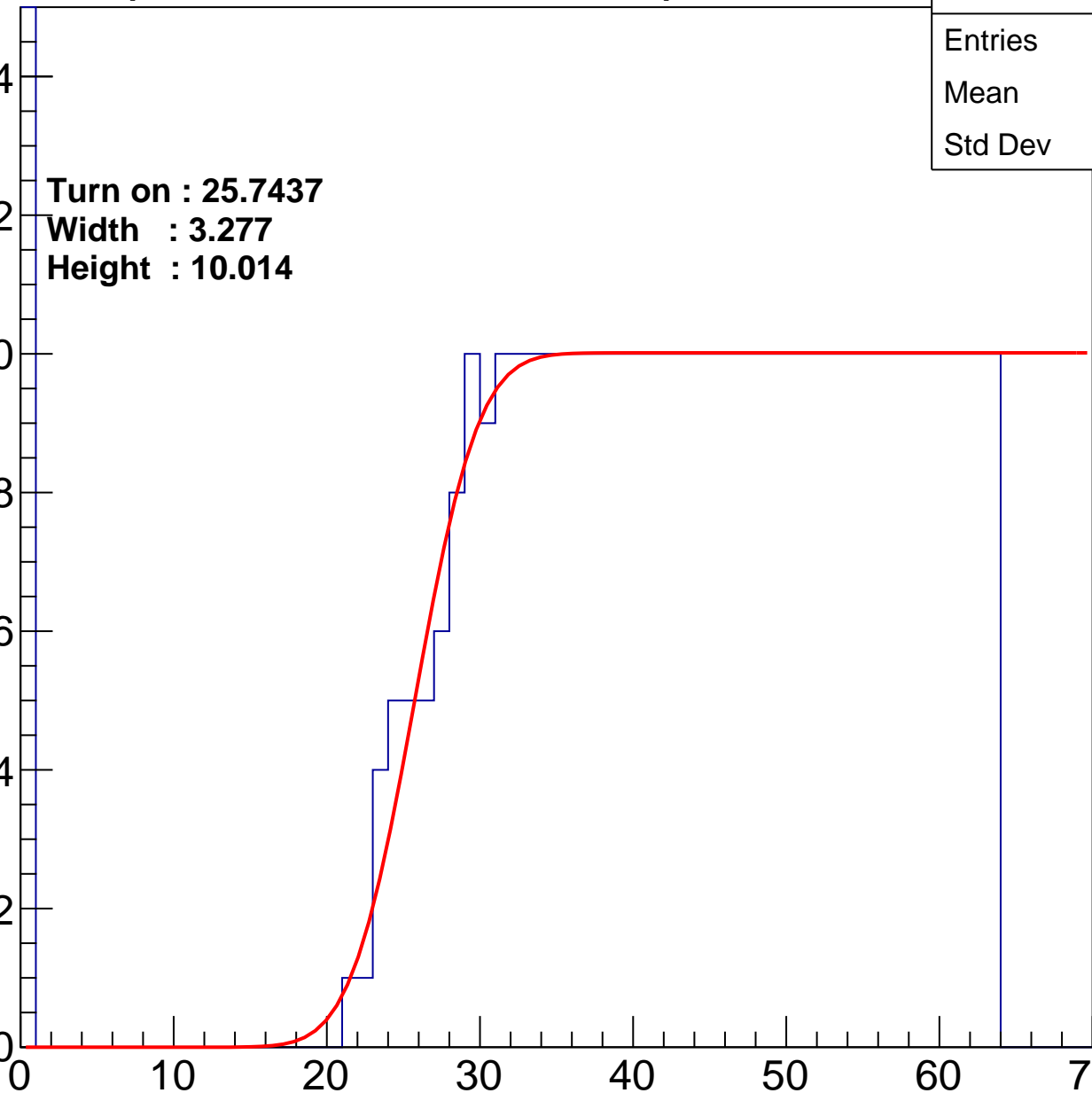
Width : 3.277

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch18

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	38.97
Std Dev	17.55

Turn on : 25.2304

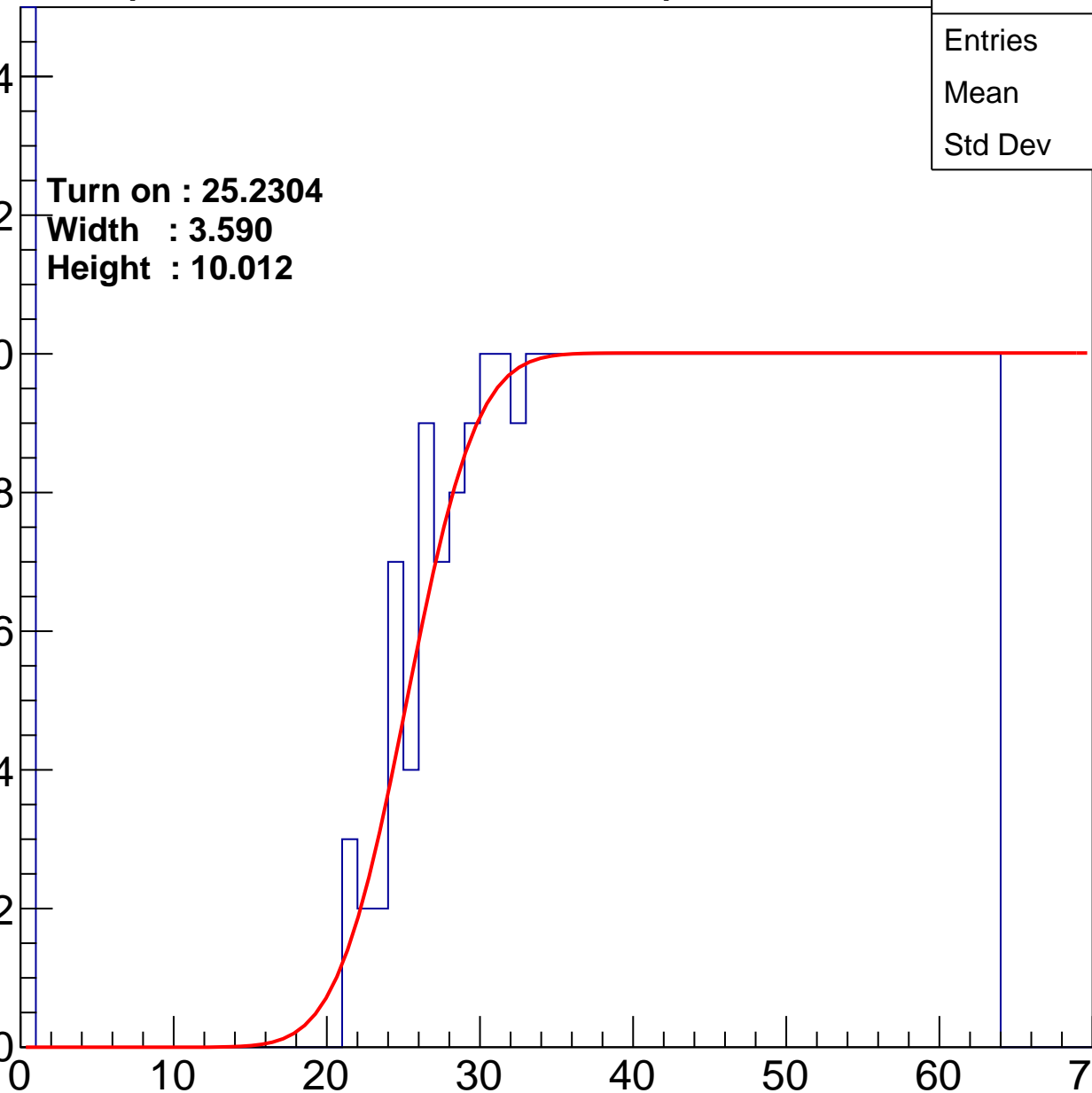
Width : 3.590

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch19

calib_packv5_041523_1651.root, FC#0, port C2

Entries	409
Mean	40.94
Std Dev	16.21

Turn on : 27.1916

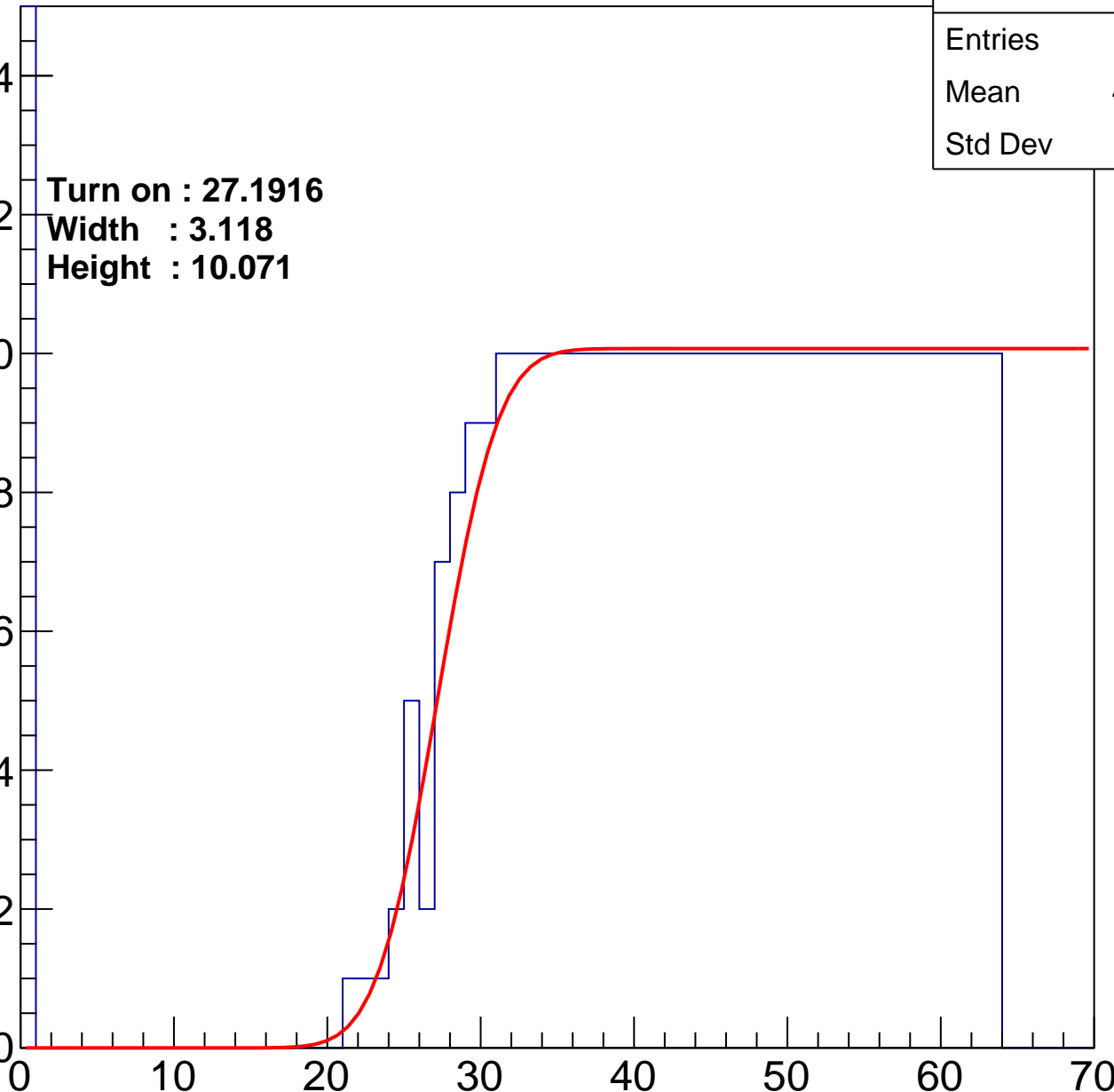
Width : 3.118

Height : 10.071

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch20

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.83
Std Dev	16.86

Turn on : 25.4352

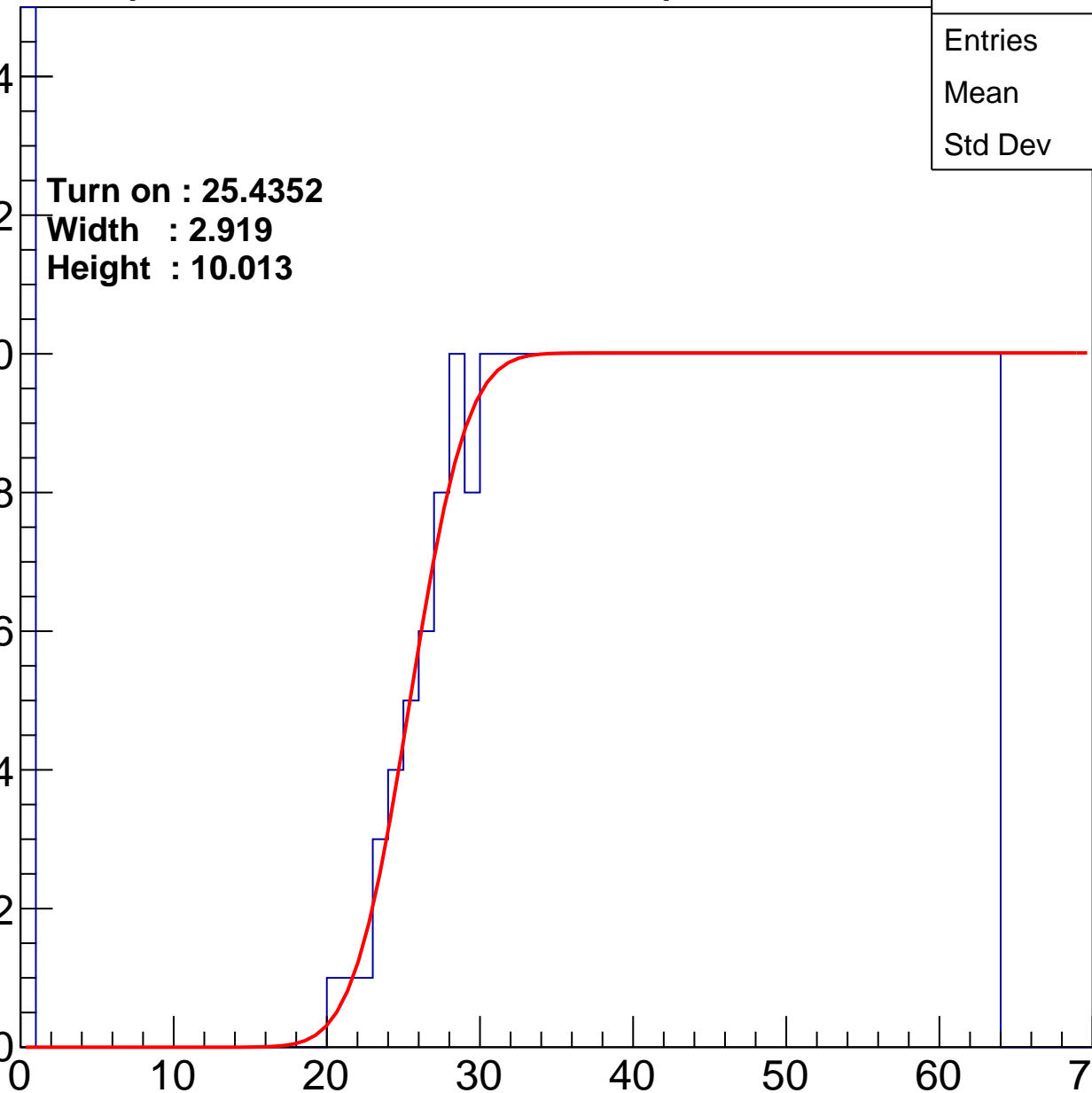
Width : 2.919

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch21

calib_packv5_041523_1651.root, FC#0, port C2

Entries	407
Mean	40.37
Std Dev	17.27

Turn on : 28.2304

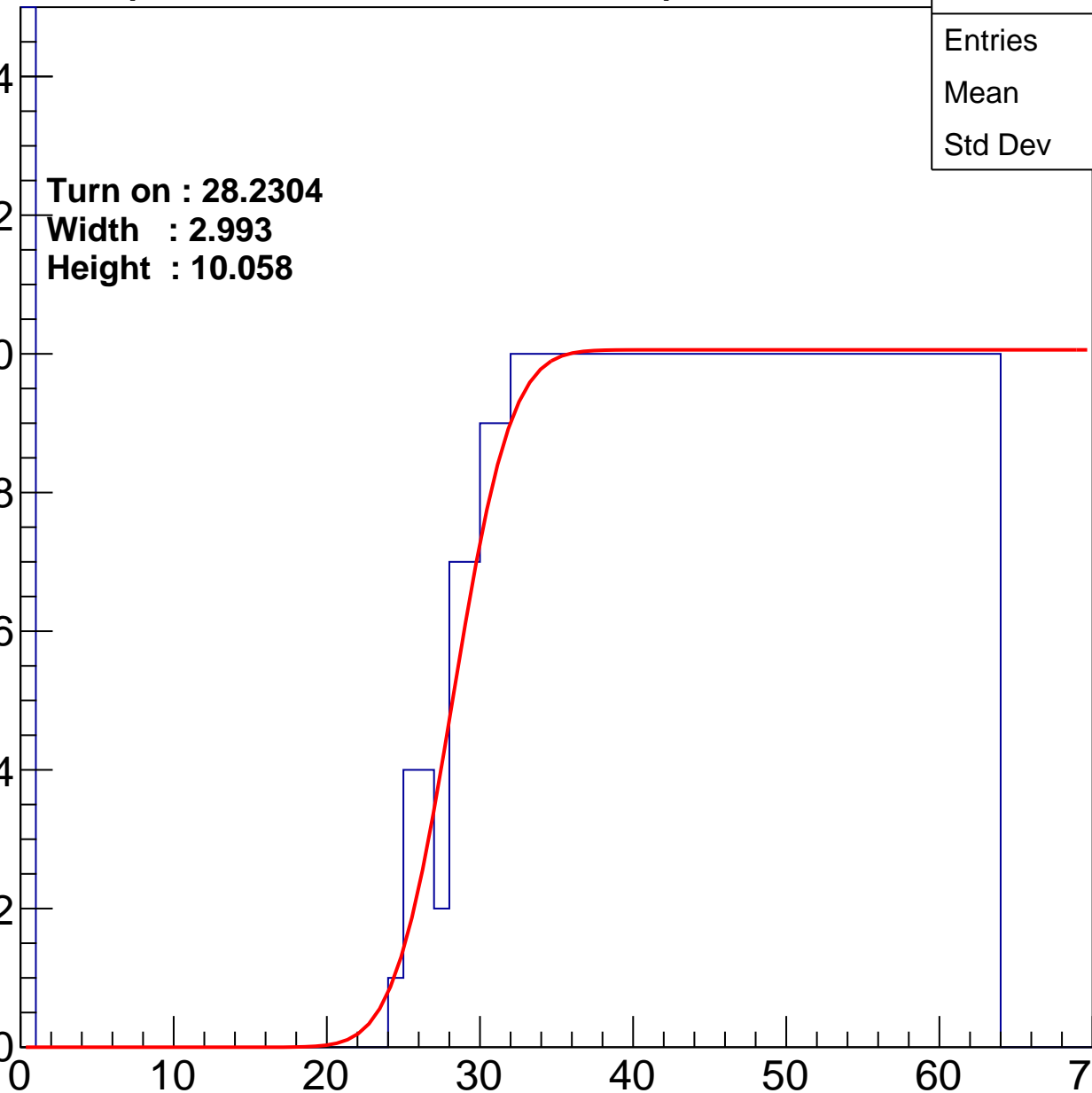
Width : 2.993

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch22

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	39.36
Std Dev	17.47

Turn on : 25.8540

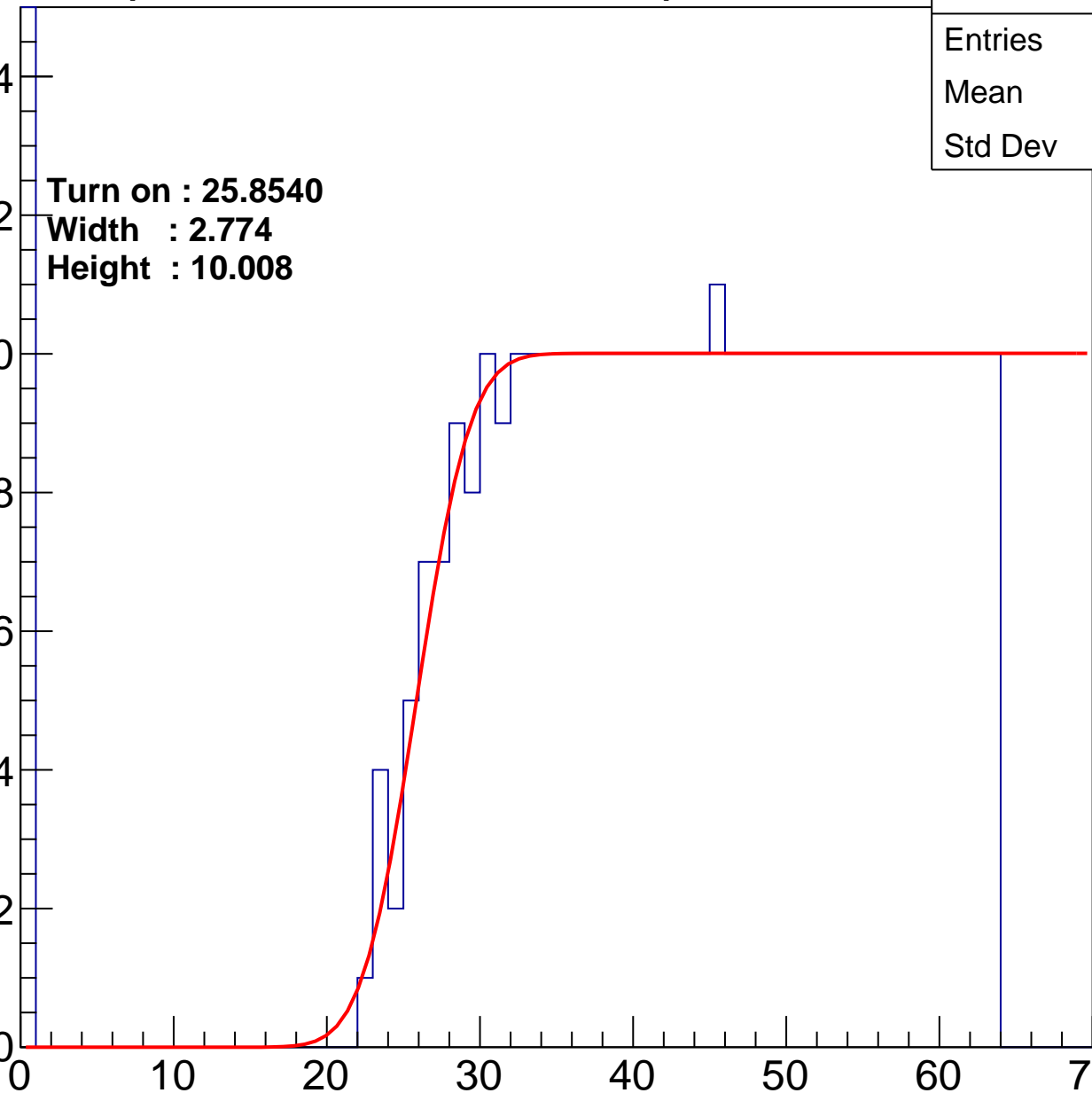
Width : 2.774

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch23

calib_packv5_041523_1651.root, FC#0, port C2

Entries	405
Mean	41.02
Std Dev	16.27

Turn on : 26.8796

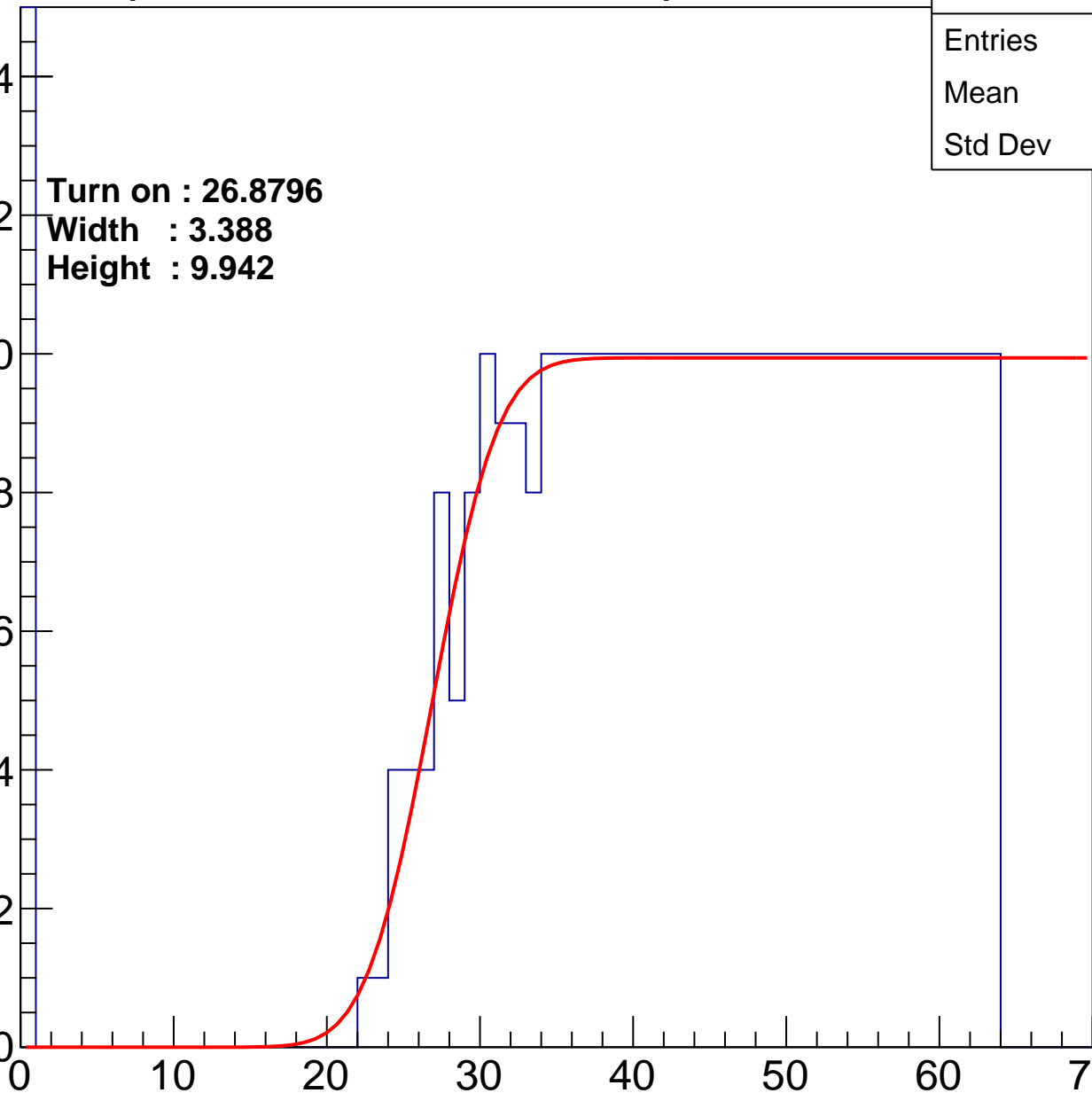
Width : 3.388

Height : 9.942

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch24

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	40.24
Std Dev	16.69

Turn on : 26.1438

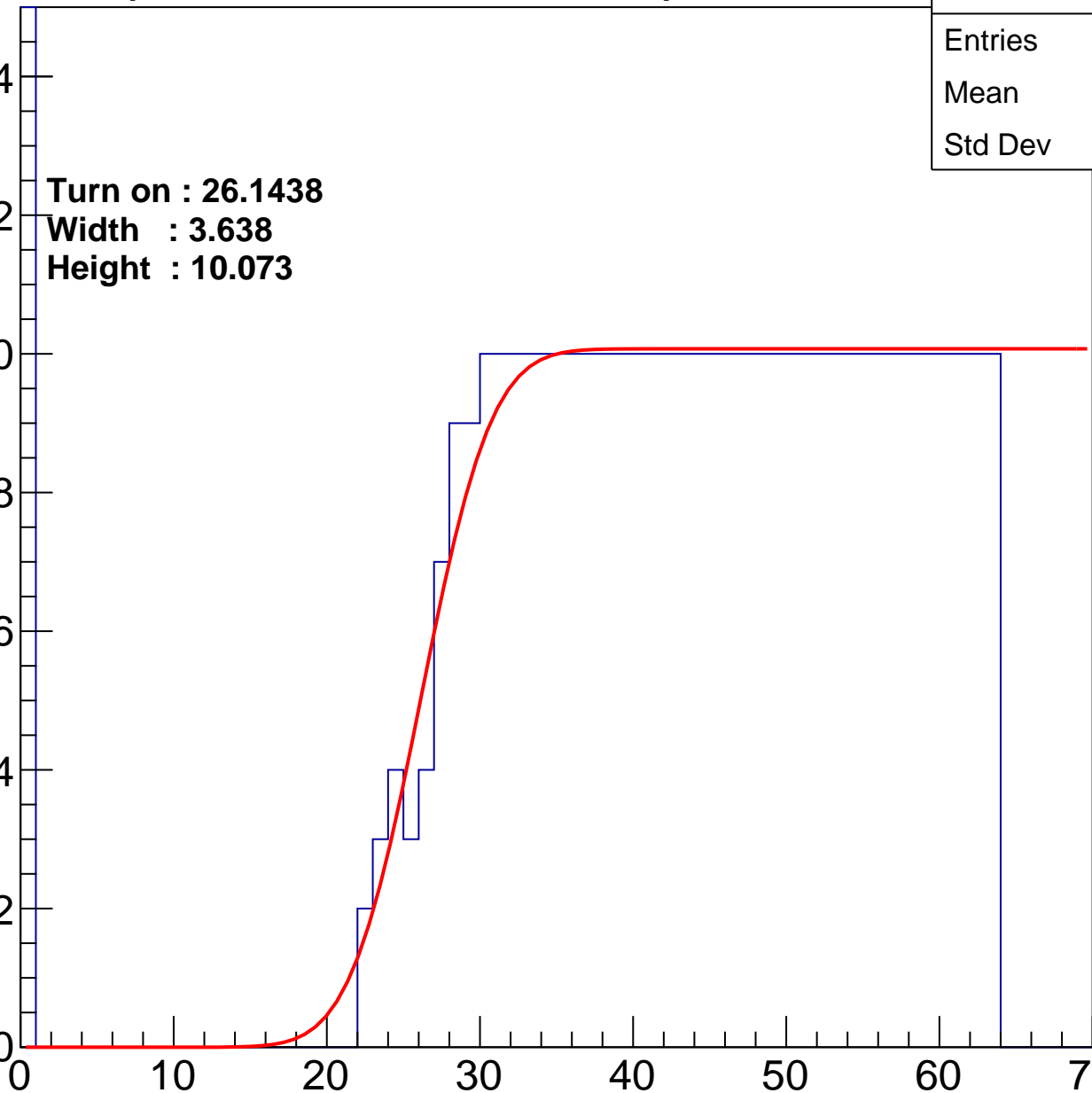
Width : 3.638

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch25

calib_packv5_041523_1651.root, FC#0, port C2

Entries	415
Mean	39.95
Std Dev	17.43

Turn on : 27.0023

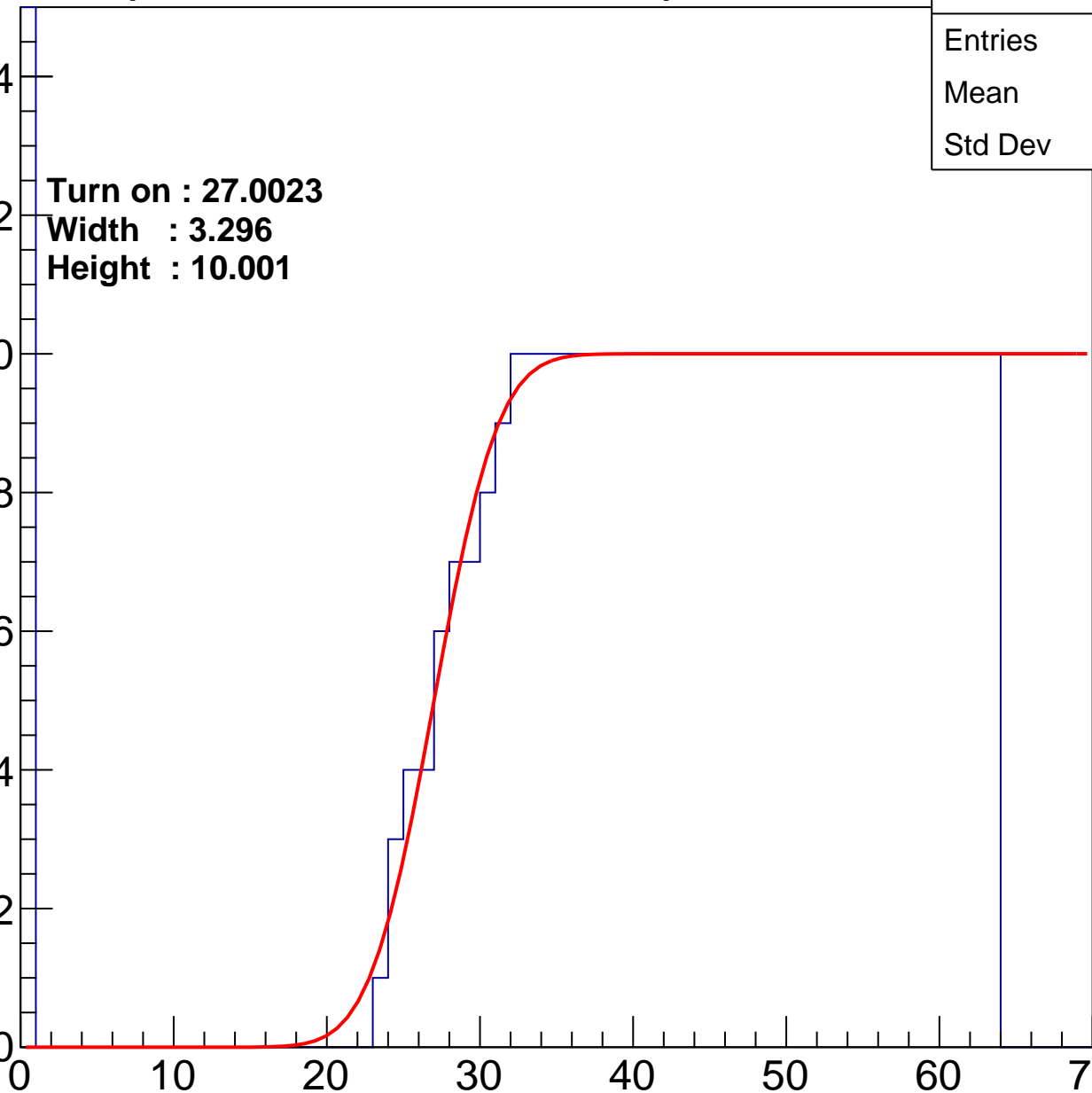
Width : 3.296

Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch26

calib_packv5_041523_1651.root, FC#0, port C2

Entries	415
Mean	40.38
Std Dev	16.74

Turn on : 26.7636

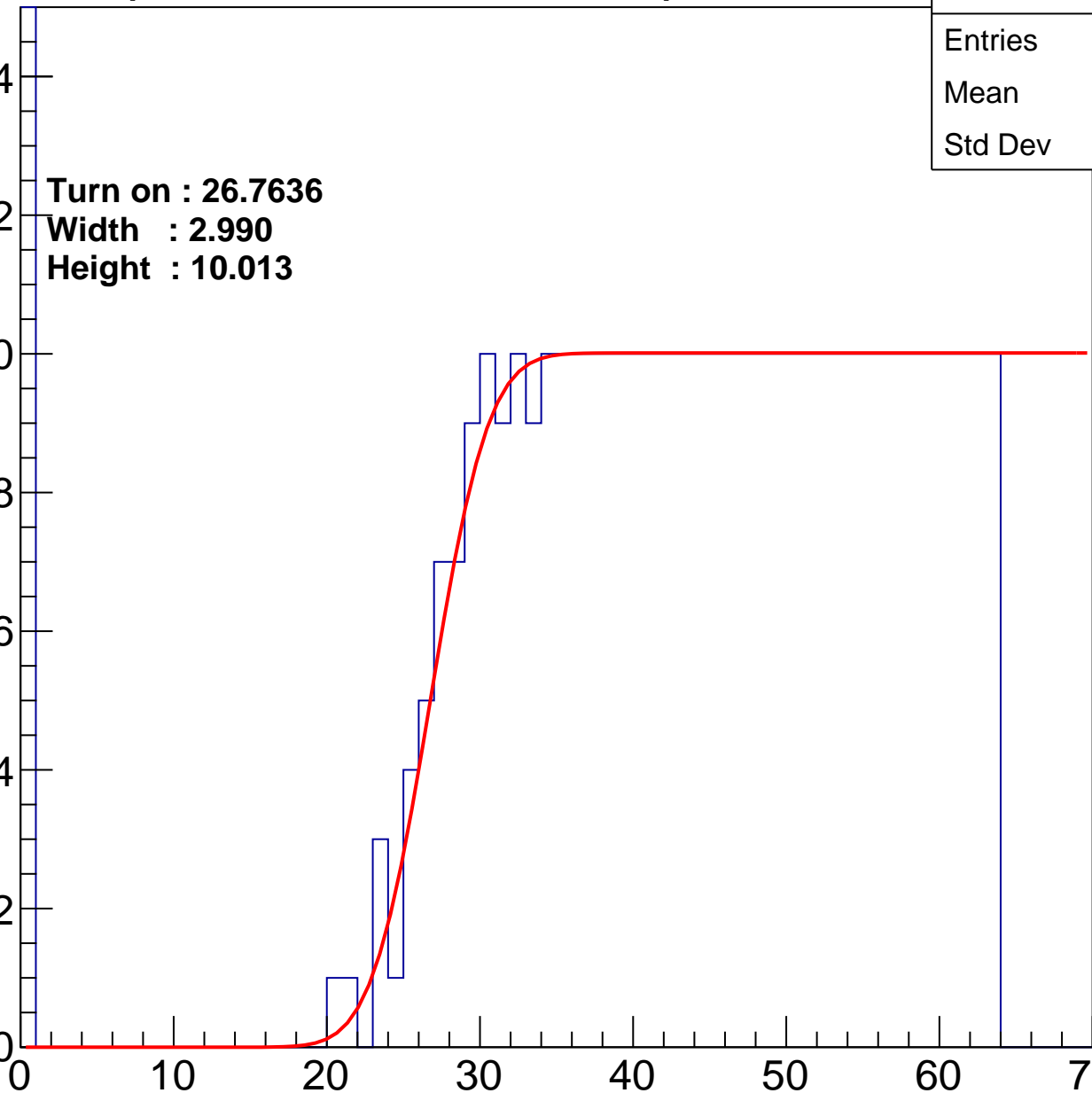
Width : 2.990

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch27

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	39.28
Std Dev	17.38

Turn on : 25.2937

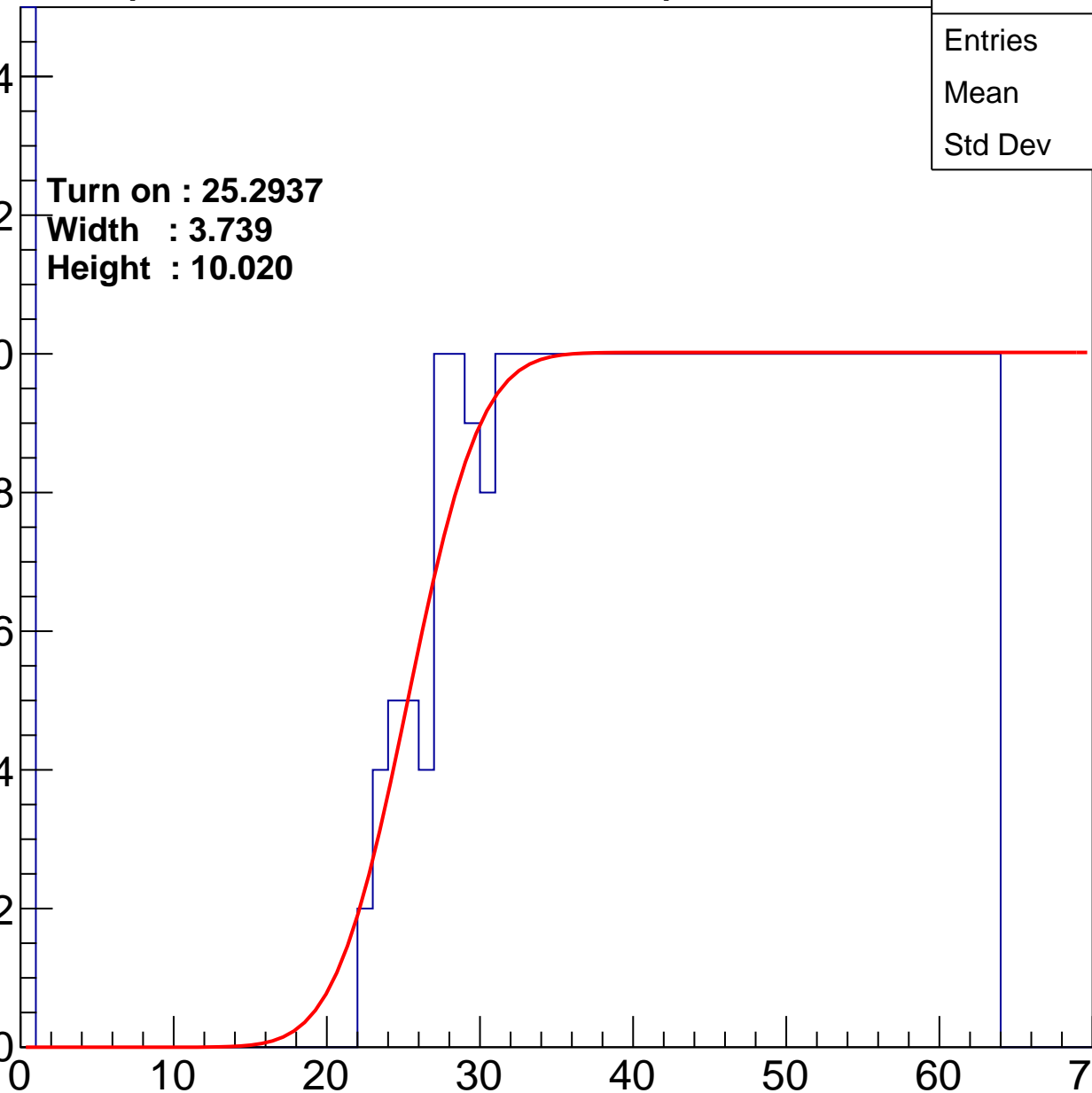
Width : 3.739

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch28

calib_packv5_041523_1651.root, FC#0, port C2

Entries	411
Mean	40.98
Std Dev	16

Turn on : 26.3669

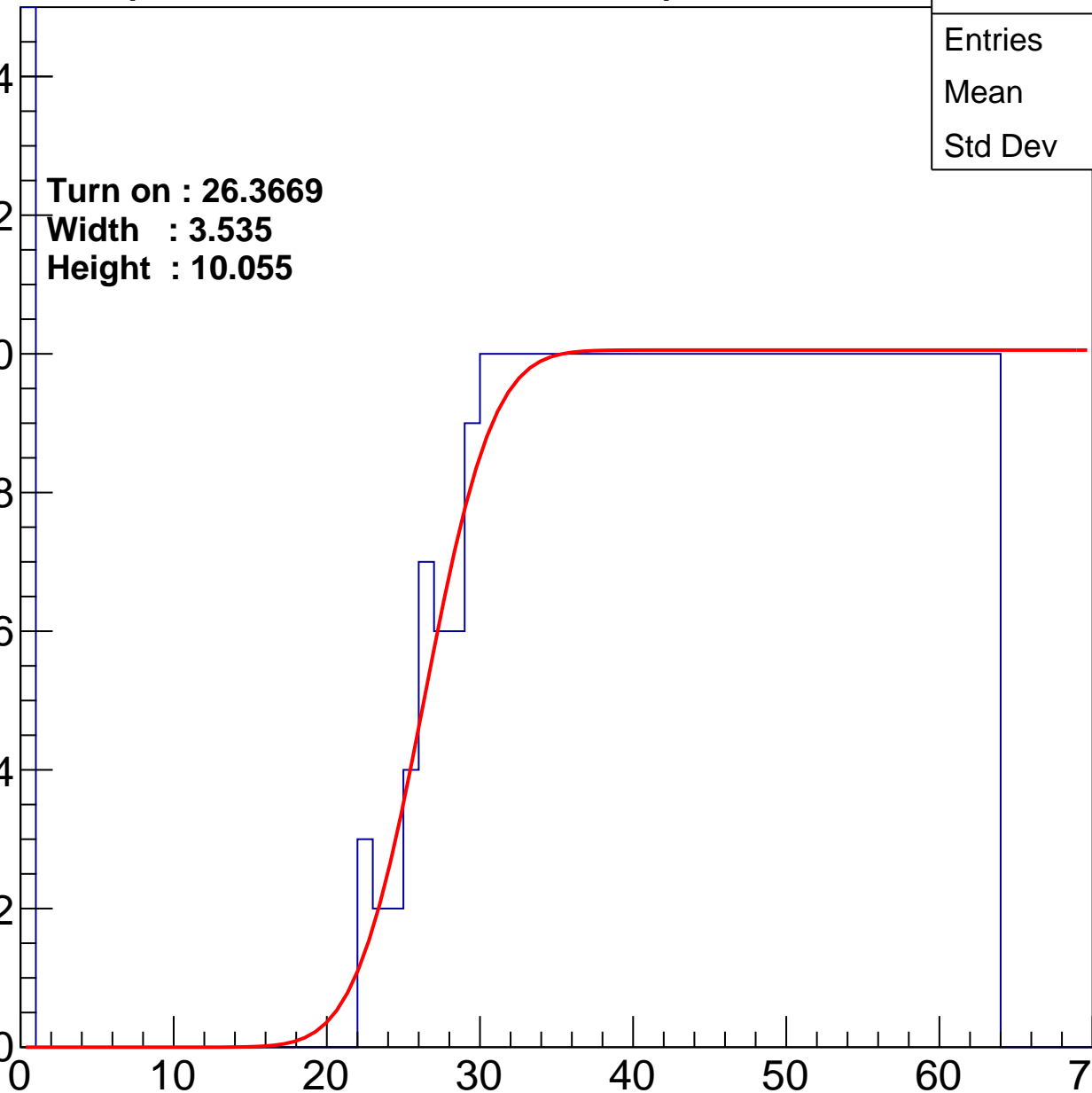
Width : 3.535

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch29

calib_packv5_041523_1651.root, FC#0, port C2

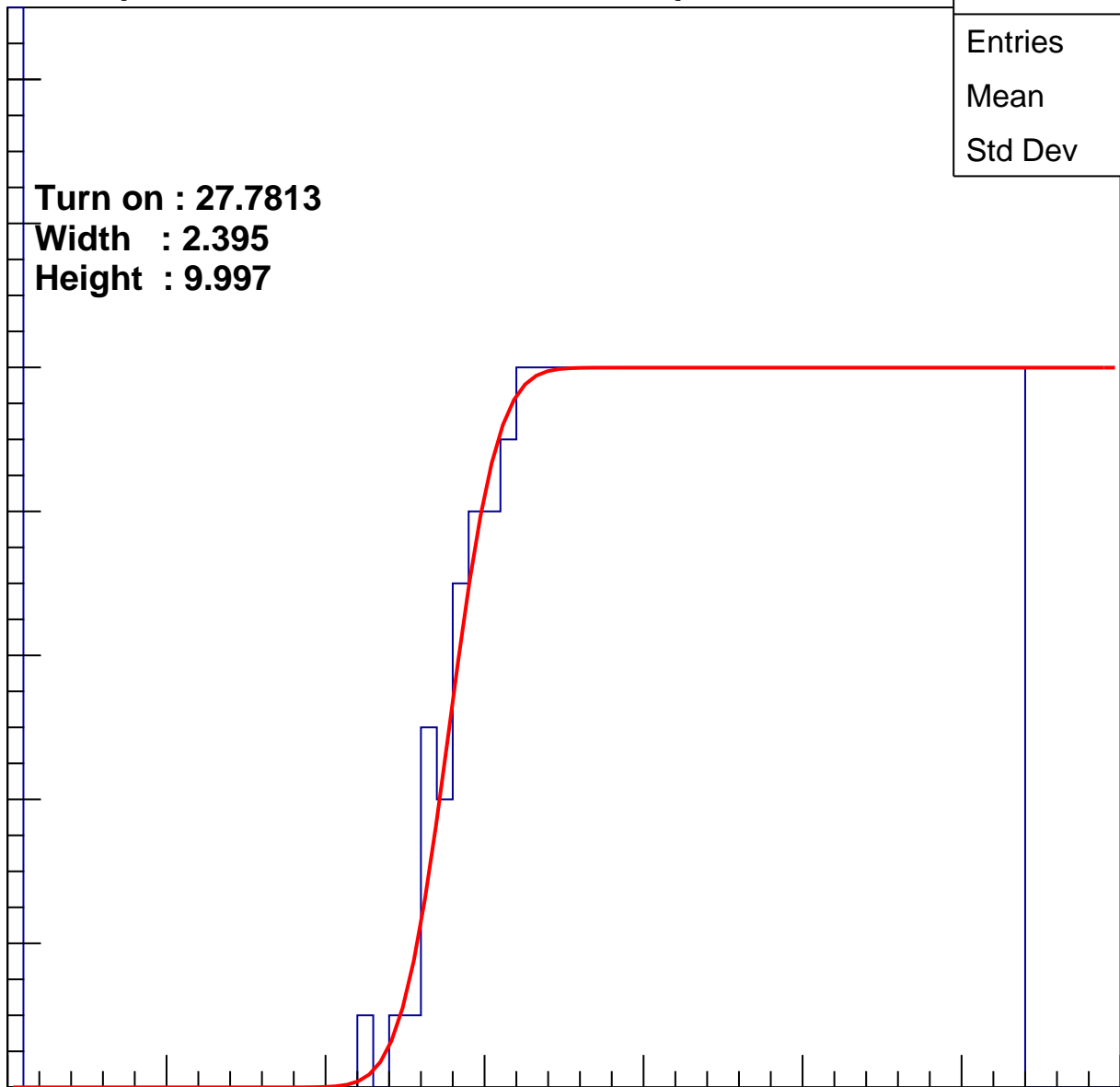
Entry

14
12
10
8
6
4
2
0

Turn on : 27.7813
Width : 2.395
Height : 9.997

Entries	395
Mean	41.66
Std Dev	15.89

ampl



B1L103S, U19-ch30

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	40.2
Std Dev	16.89

Turn on : 26.3073

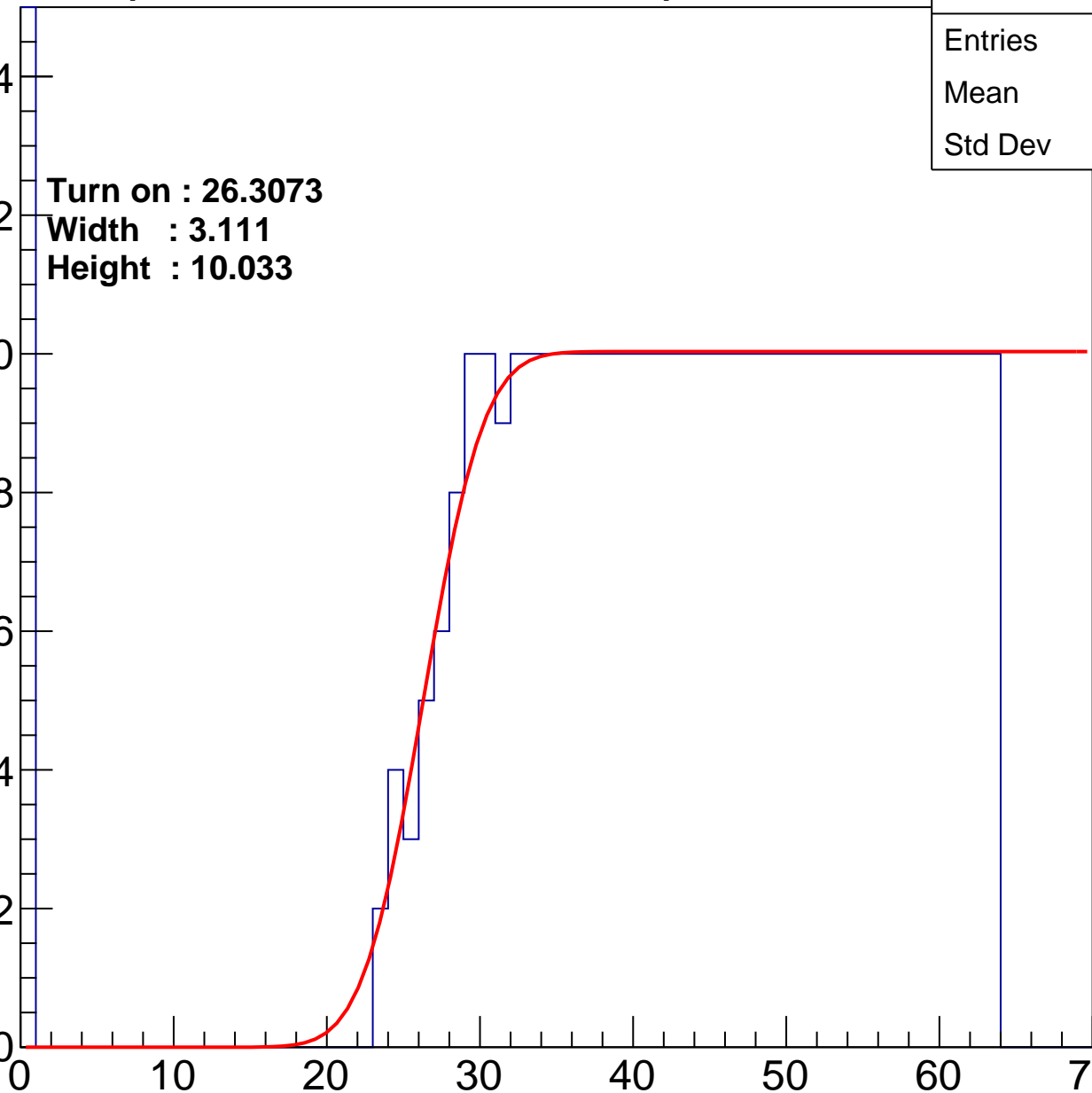
Width : 3.111

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch31

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	39.73
Std Dev	17.26

Turn on : 26.1639

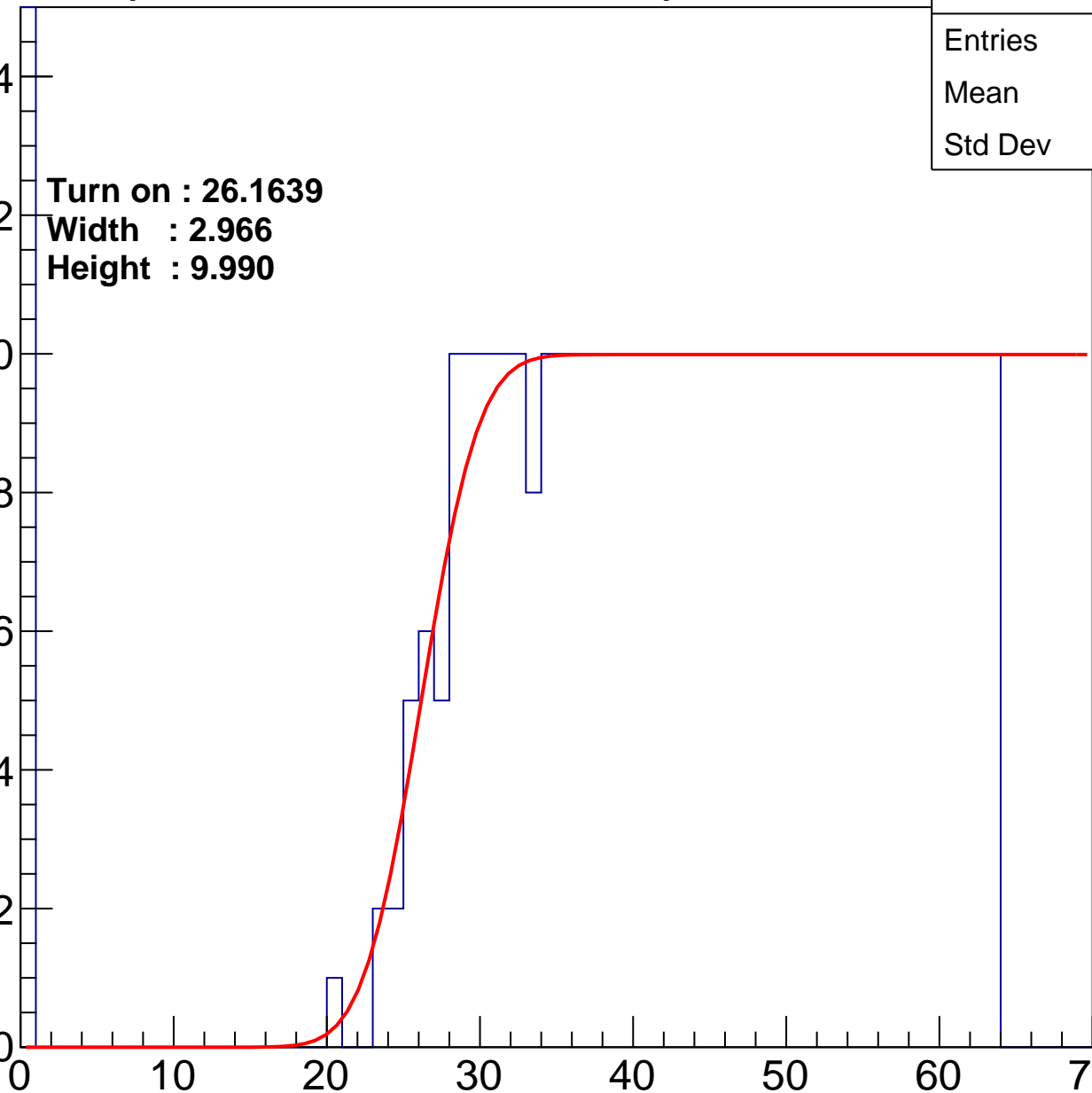
Width : 2.966

Height : 9.990

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch32

calib_packv5_041523_1651.root, FC#0, port C2

Entries	445
Mean	38.57
Std Dev	17.83

Turn on : 25.7722

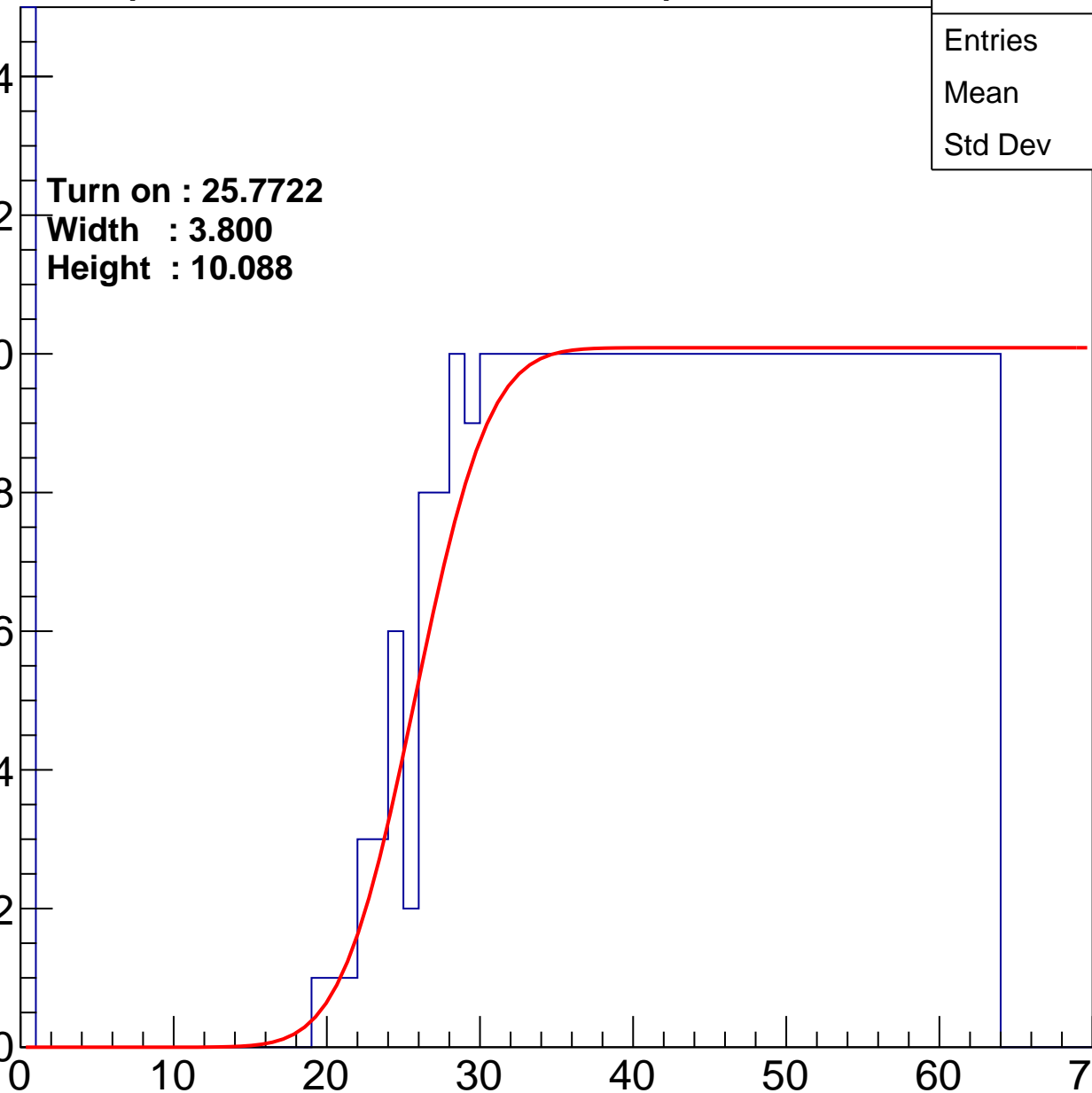
Width : 3.800

Height : 10.088

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch33

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	40.12
Std Dev	17.06

Turn on : 26.5182

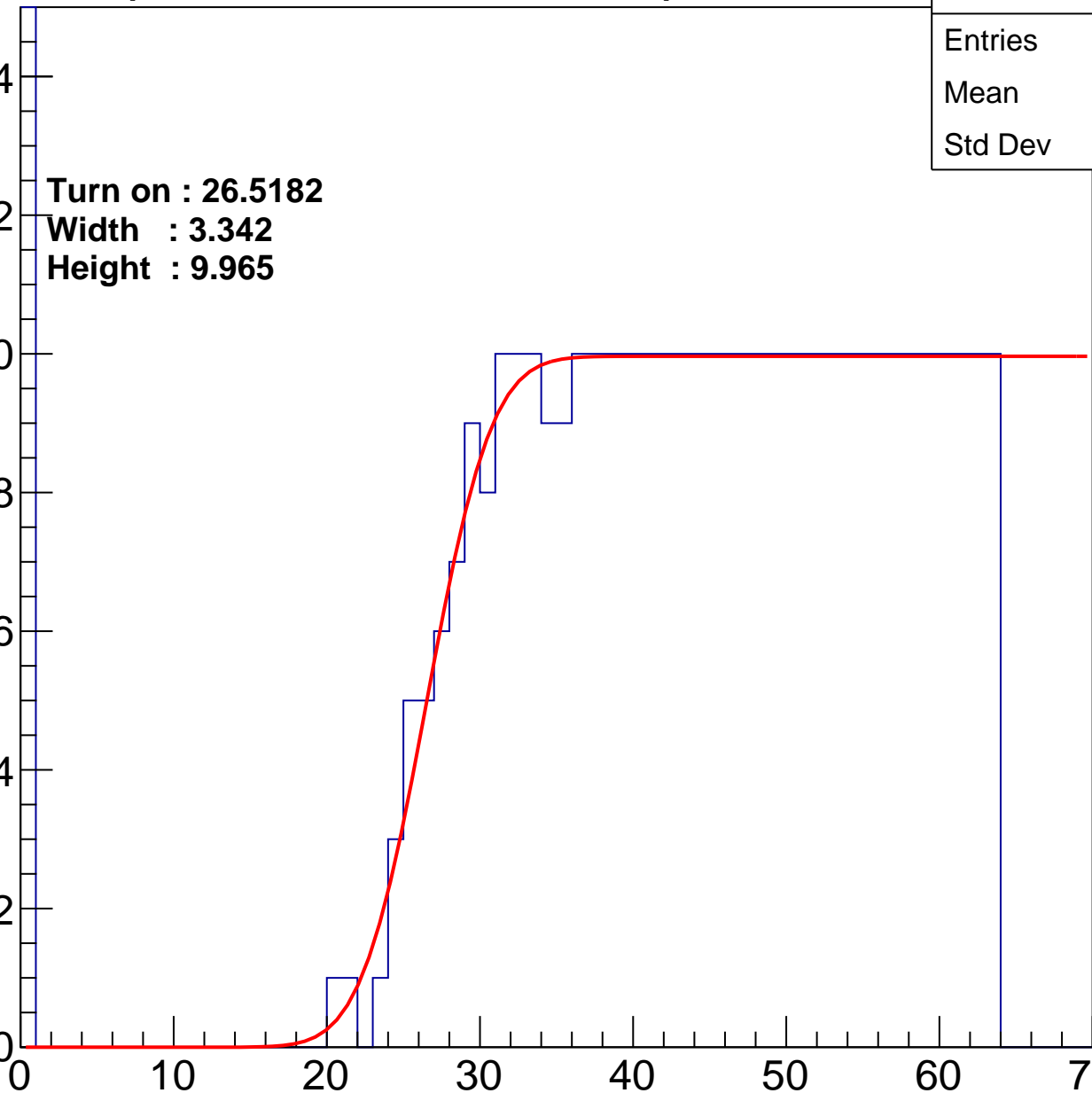
Width : 3.342

Height : 9.965

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch34

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	40.36
Std Dev	16.45

Turn on : 25.8449

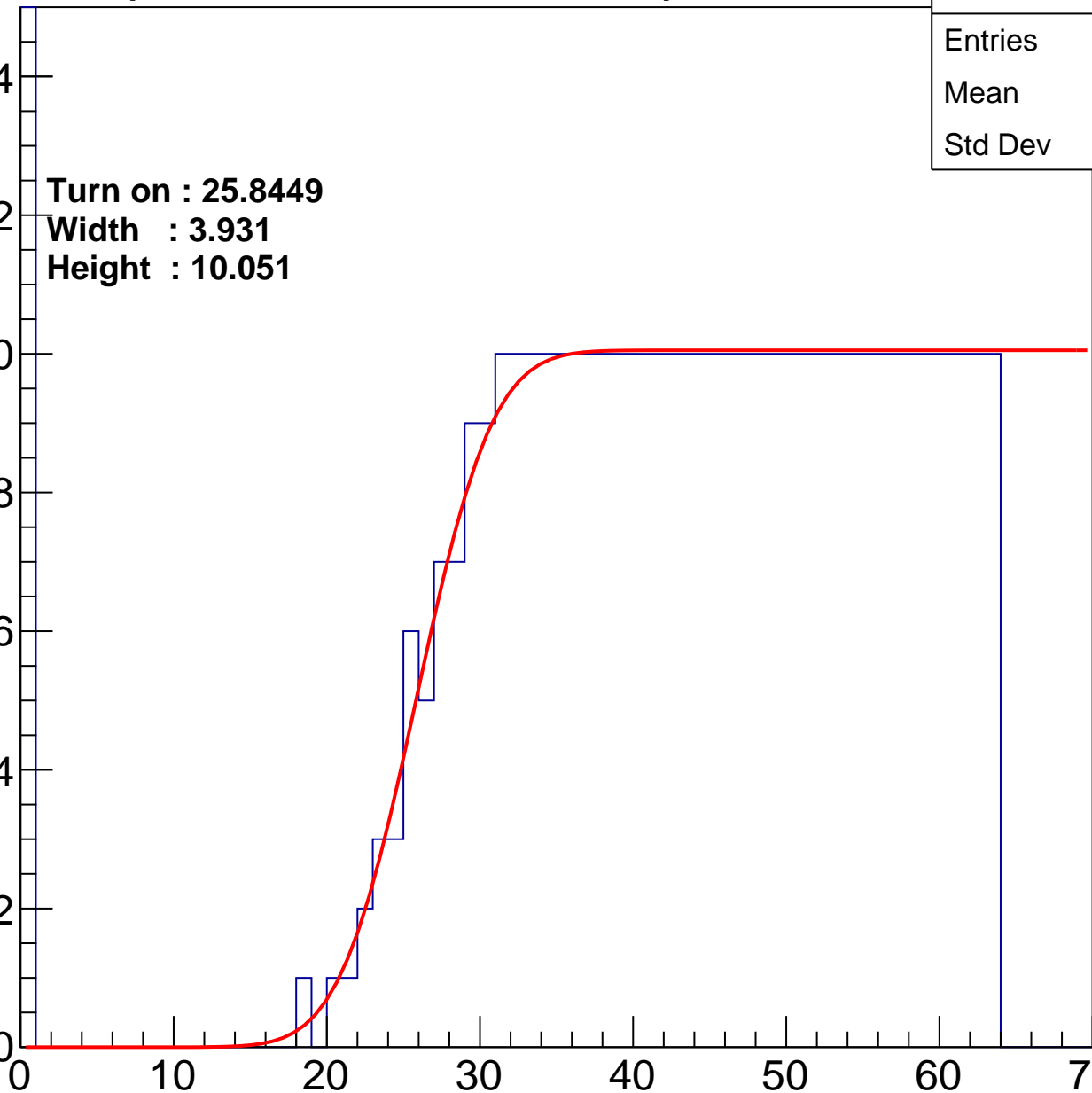
Width : 3.931

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch35

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	40.7
Std Dev	16.01

Turn on : 25.5831

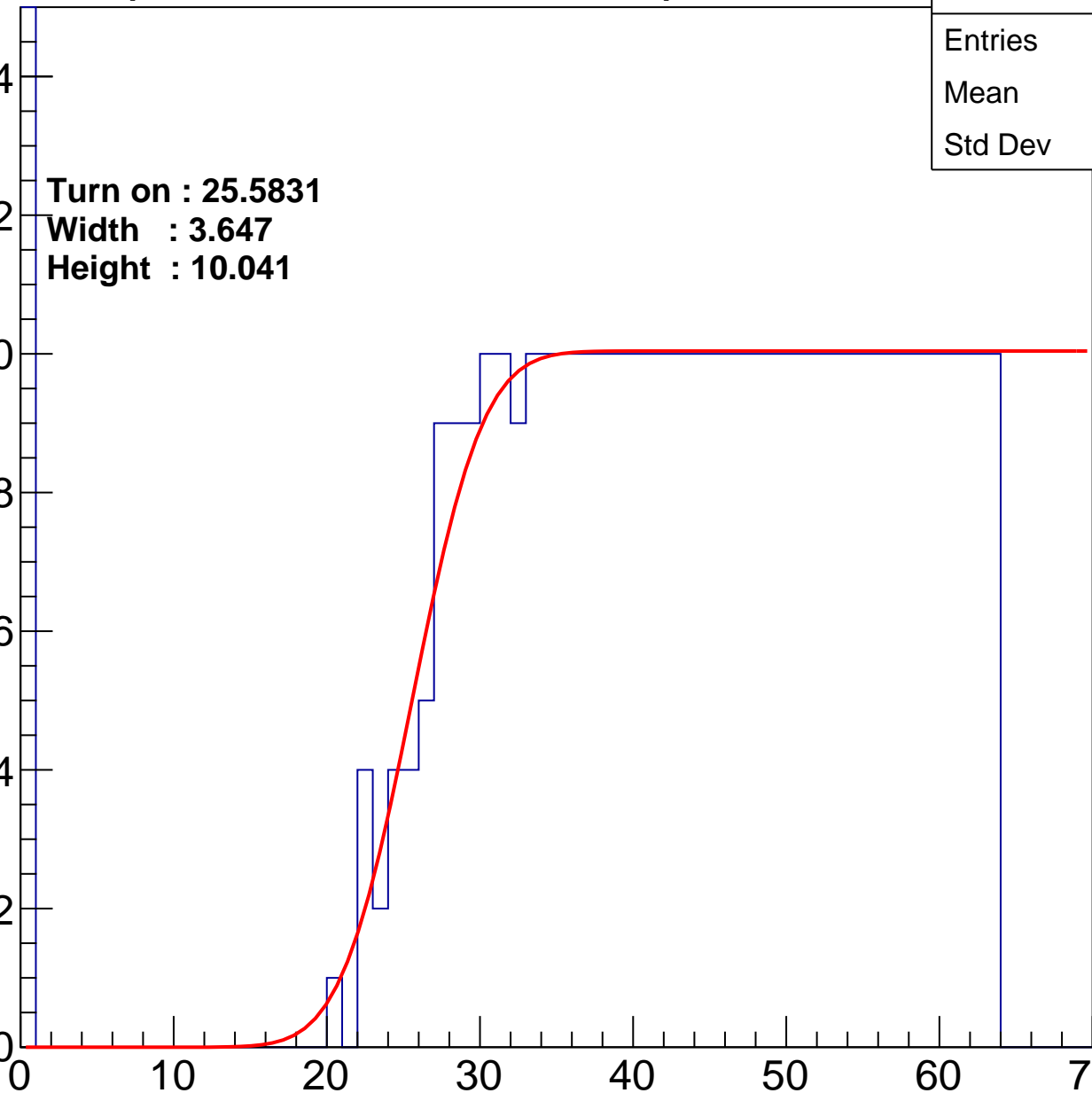
Width : 3.647

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch36

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	39.36
Std Dev	17.85

Turn on : 27.1529

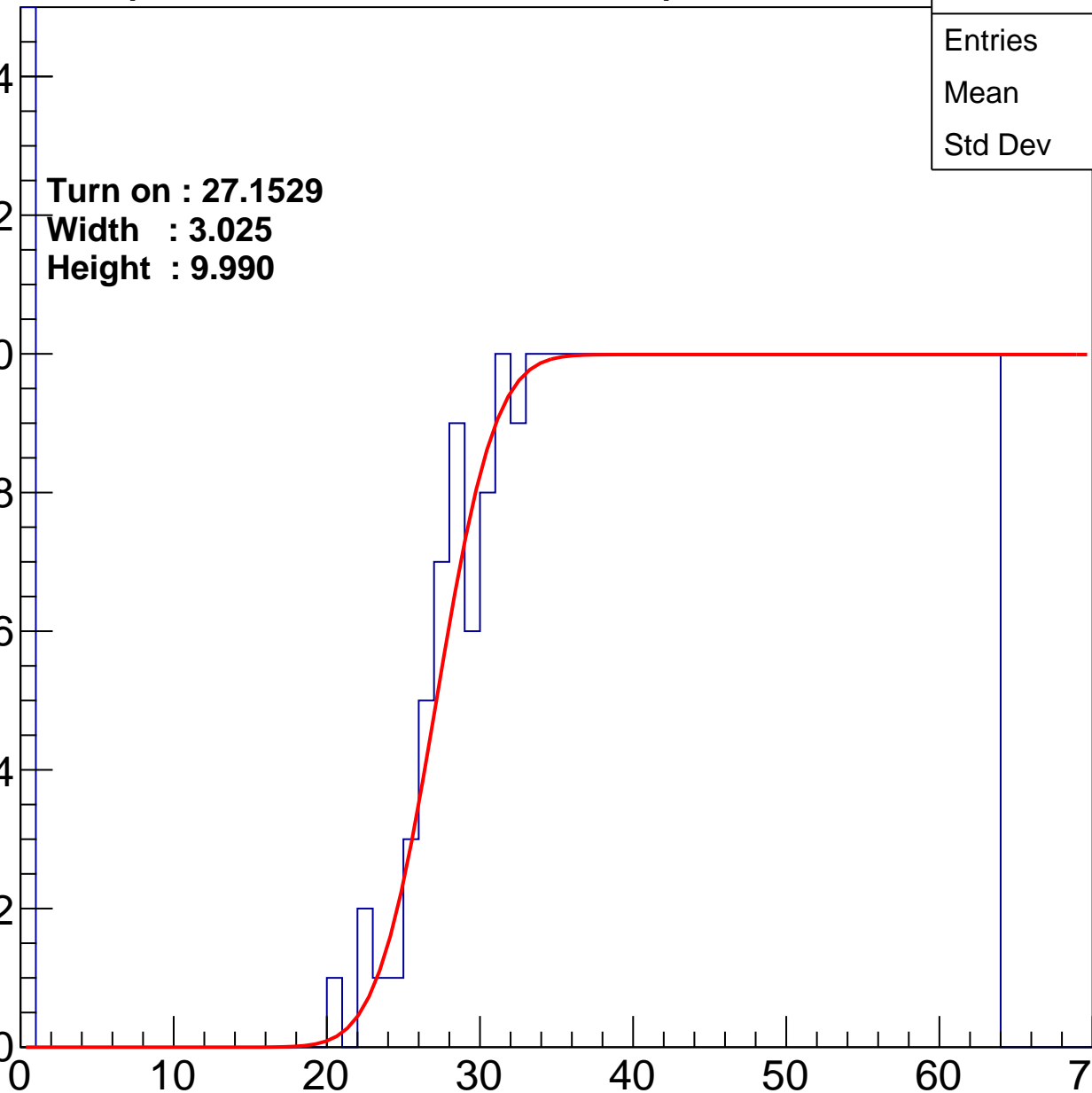
Width : 3.025

Height : 9.990

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch37

calib_packv5_041523_1651.root, FC#0, port C2

Entries	397
Mean	40.7
Std Dev	17.36

Turn on : 28.4979

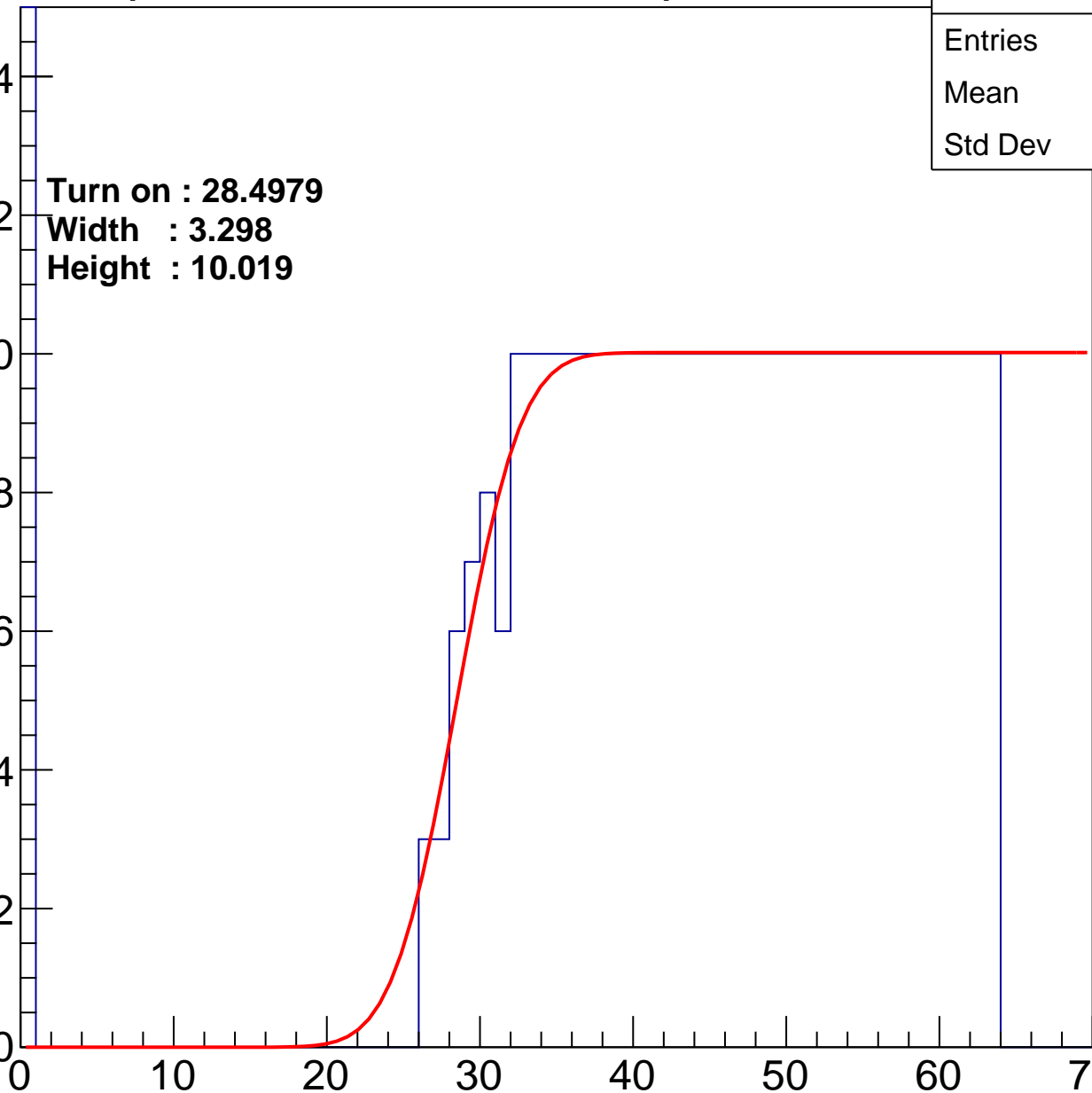
Width : 3.298

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch38

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	40.34
Std Dev	16.51

Turn on : 24.7659

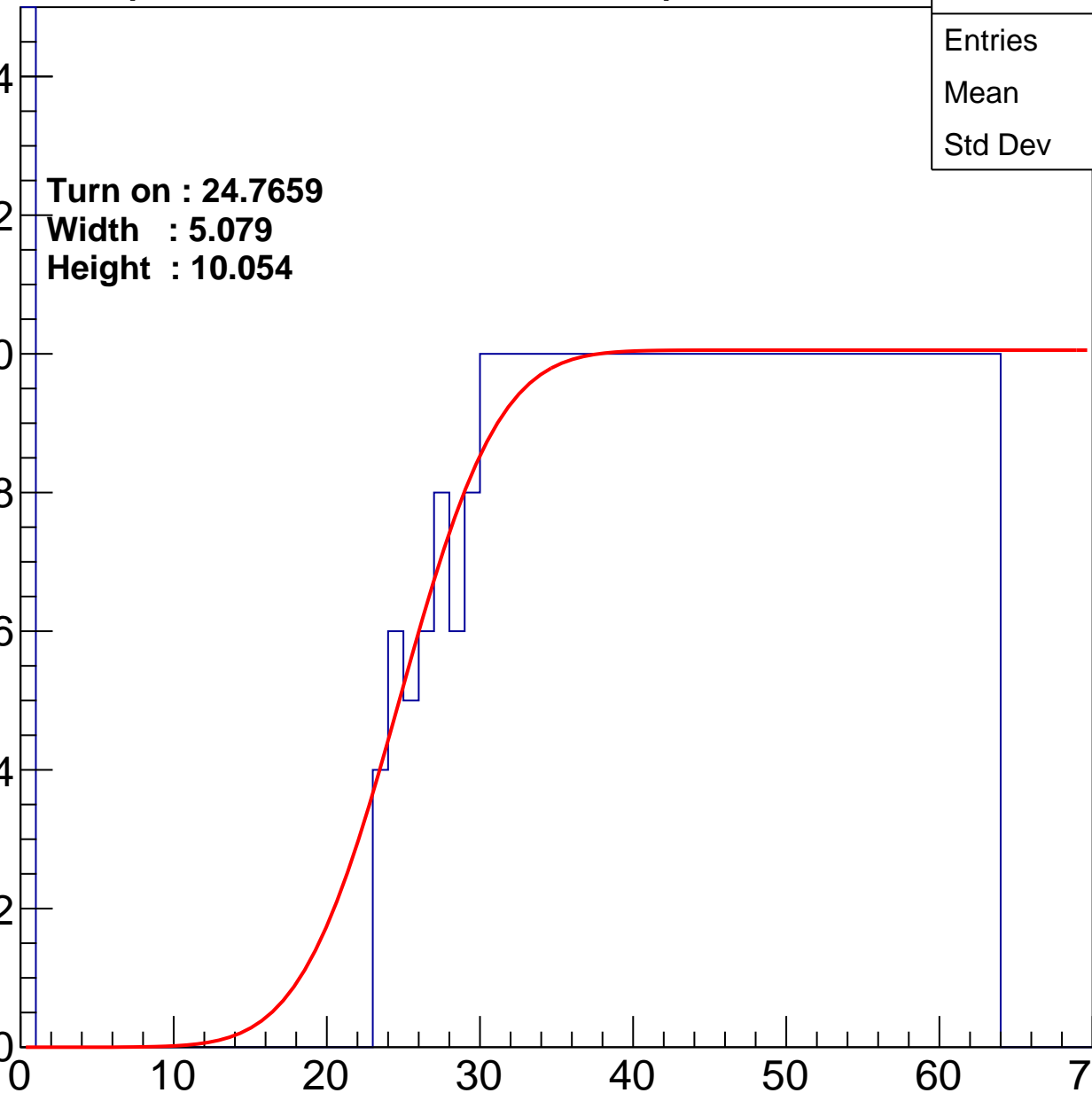
Width : 5.079

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch39

calib_packv5_041523_1651.root, FC#0, port C2

Entries	409
Mean	40.52
Std Dev	16.88

Turn on : 27.1727

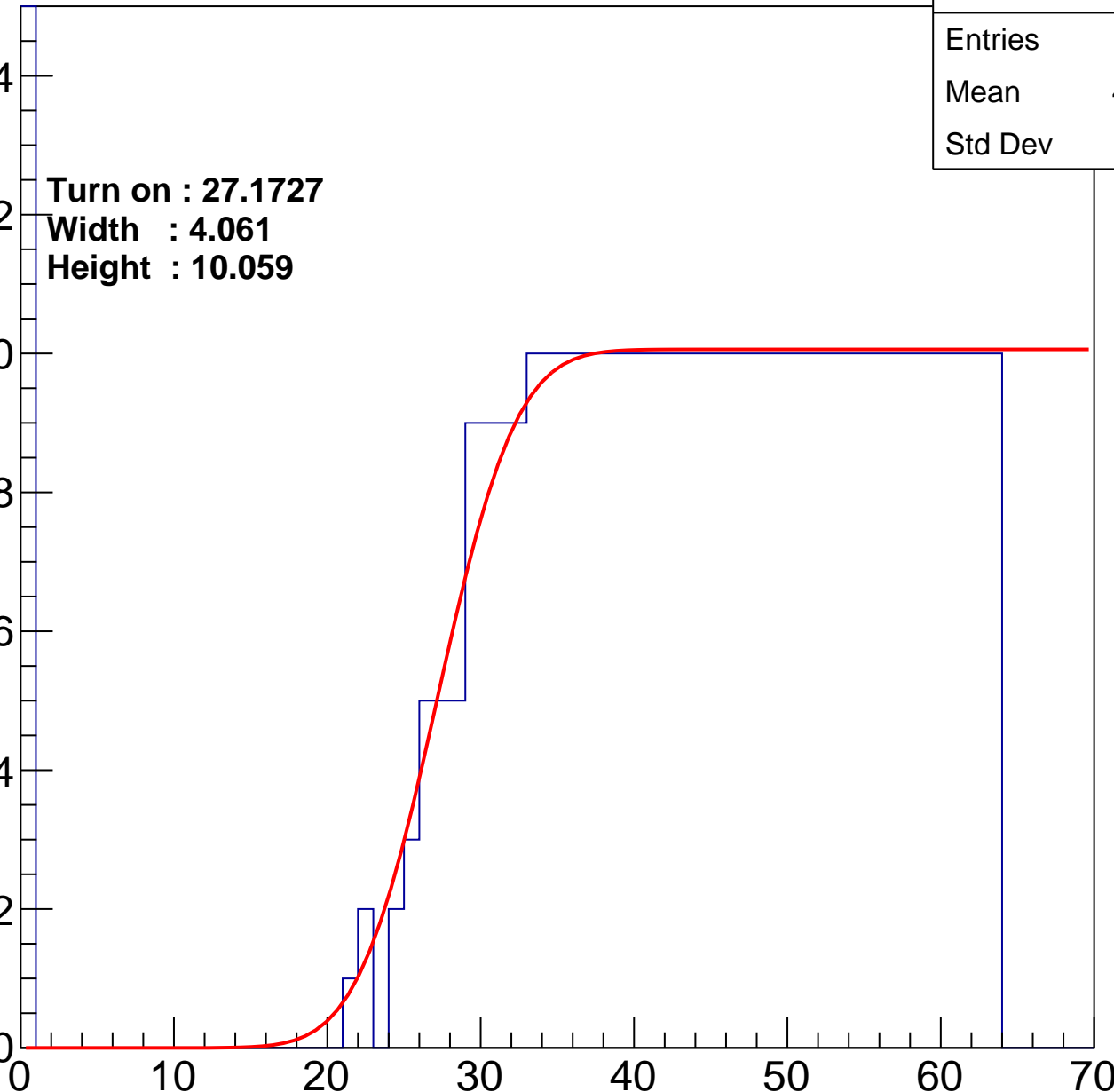
Width : 4.061

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch40

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	40.38
Std Dev	16.76

Turn on : 26.5335

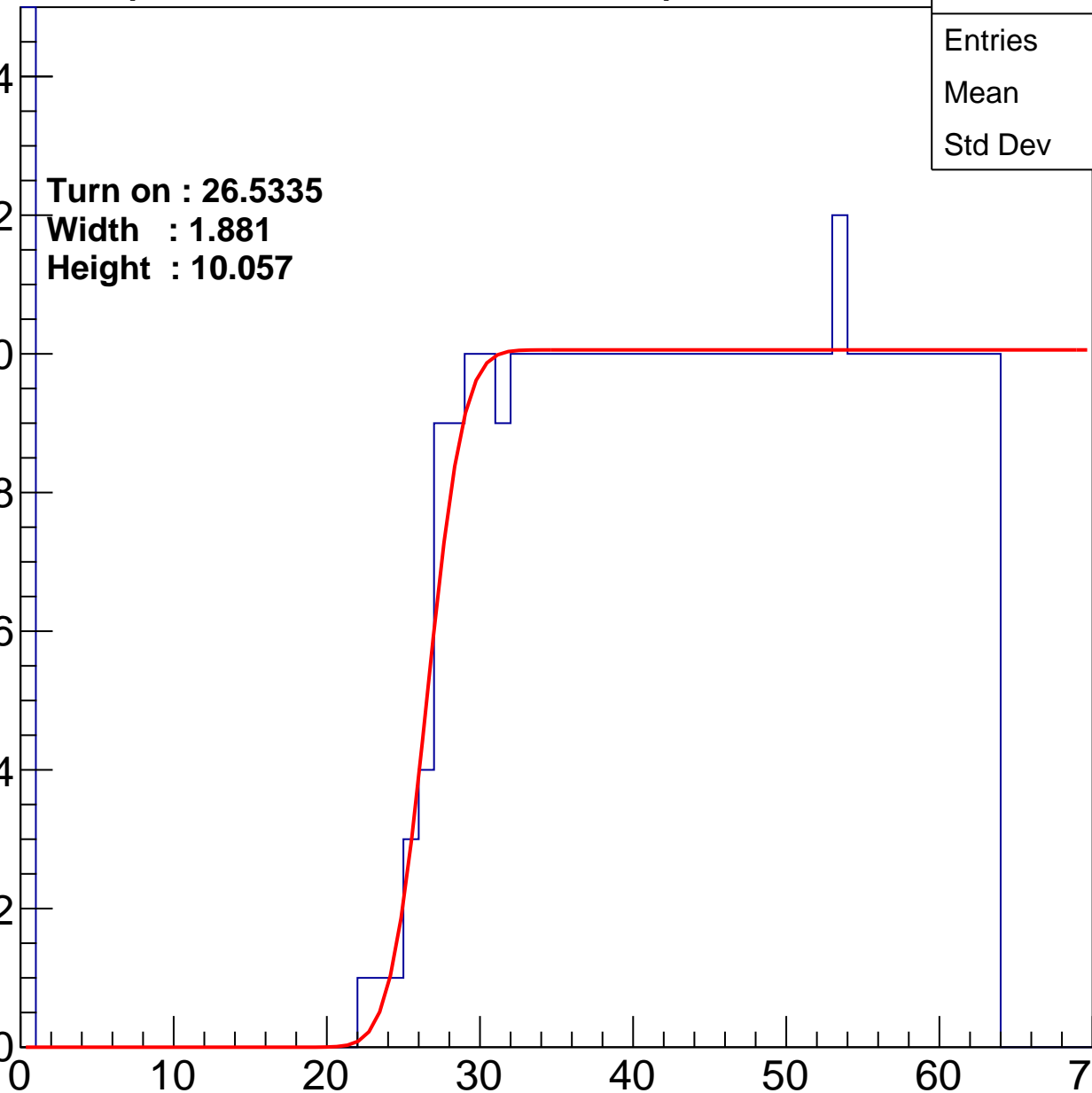
Width : 1.881

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch41

calib_packv5_041523_1651.root, FC#0, port C2

Entries	407
Mean	40.82
Std Dev	16.54

Turn on : 27.5182

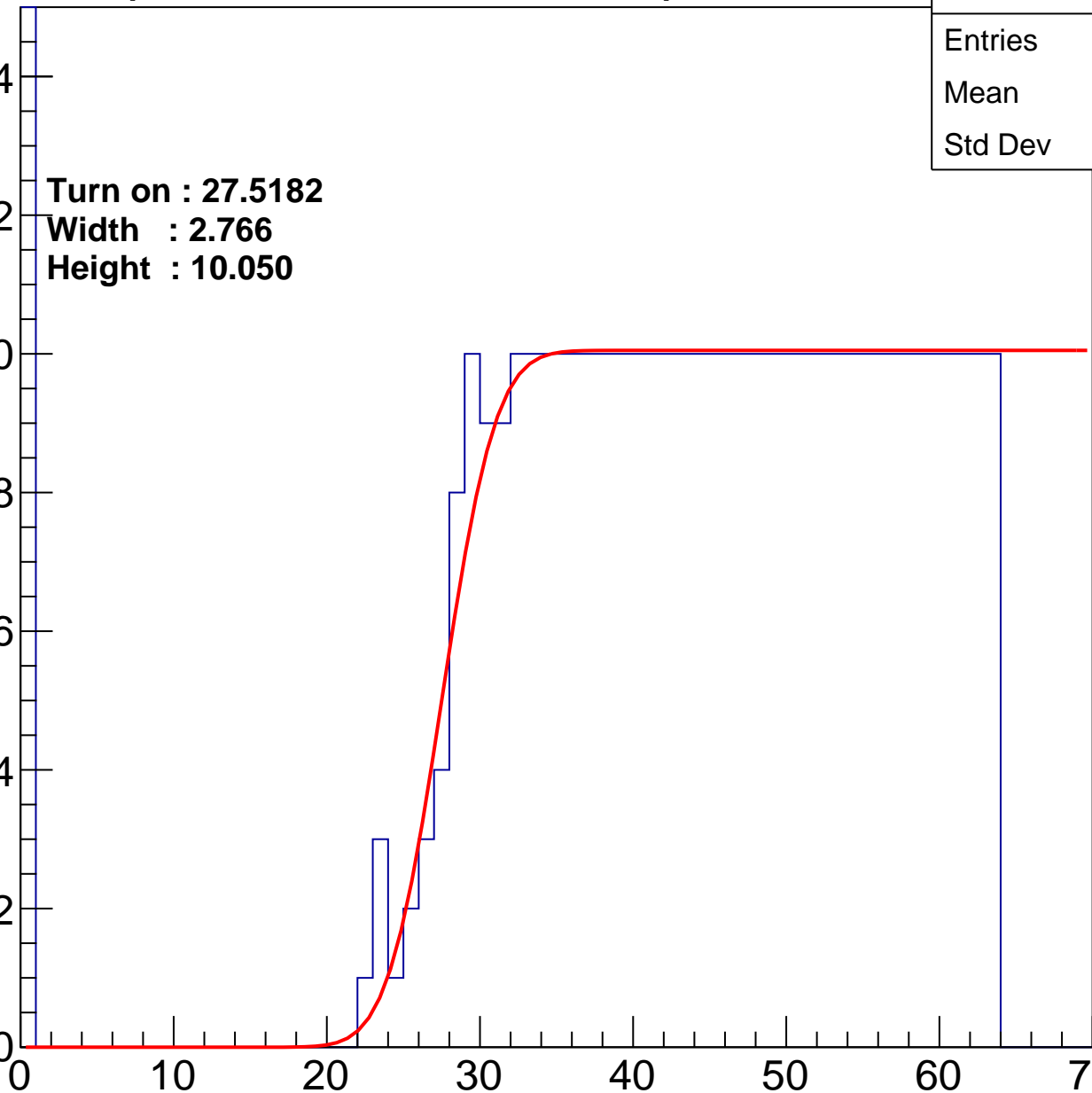
Width : 2.766

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch42

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	39.47
Std Dev	17.03

Turn on : 24.9623

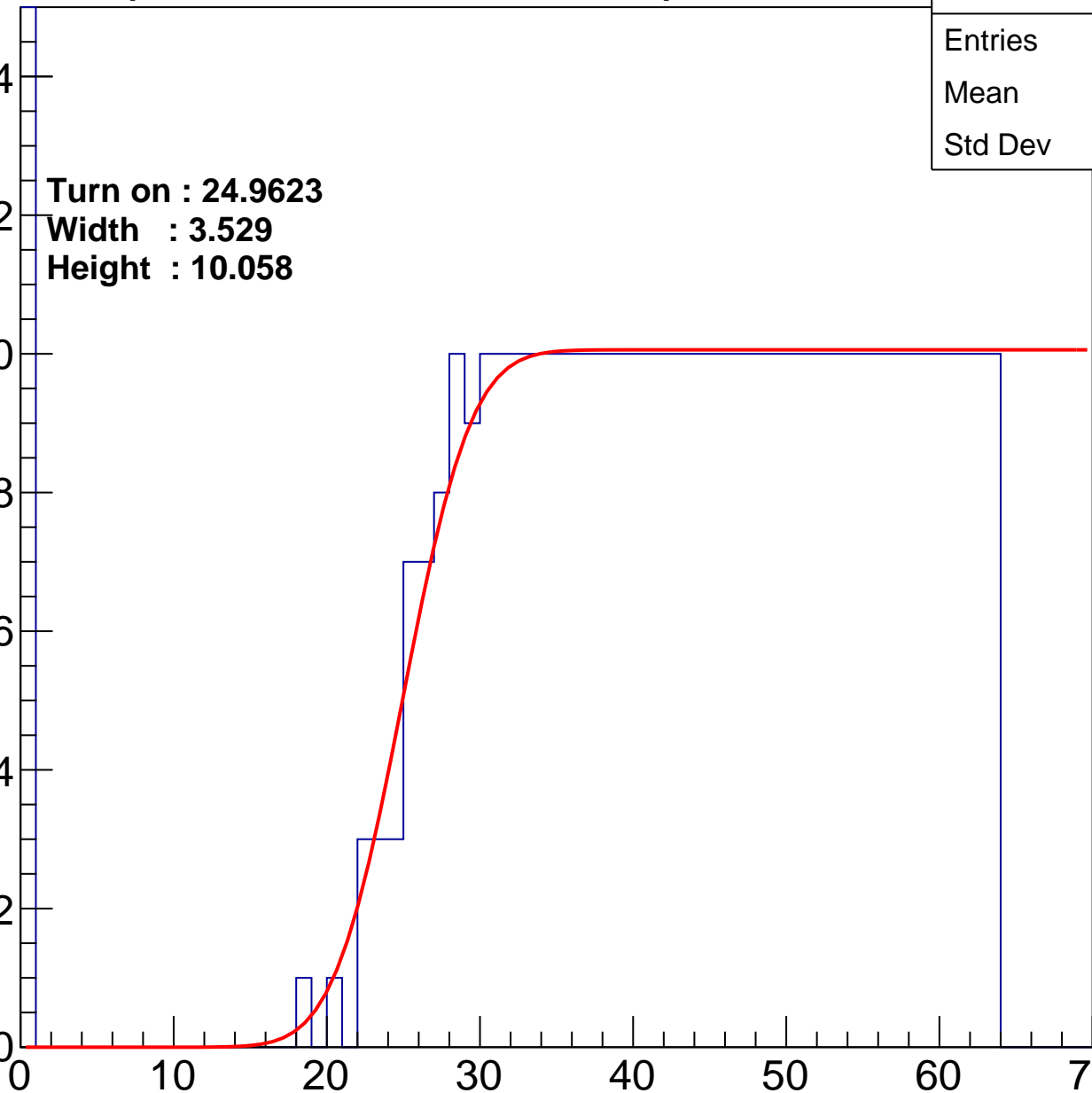
Width : 3.529

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch43

calib_packv5_041523_1651.root, FC#0, port C2

Entries	417
Mean	40.33
Std Dev	16.76

Turn on : 26.2286

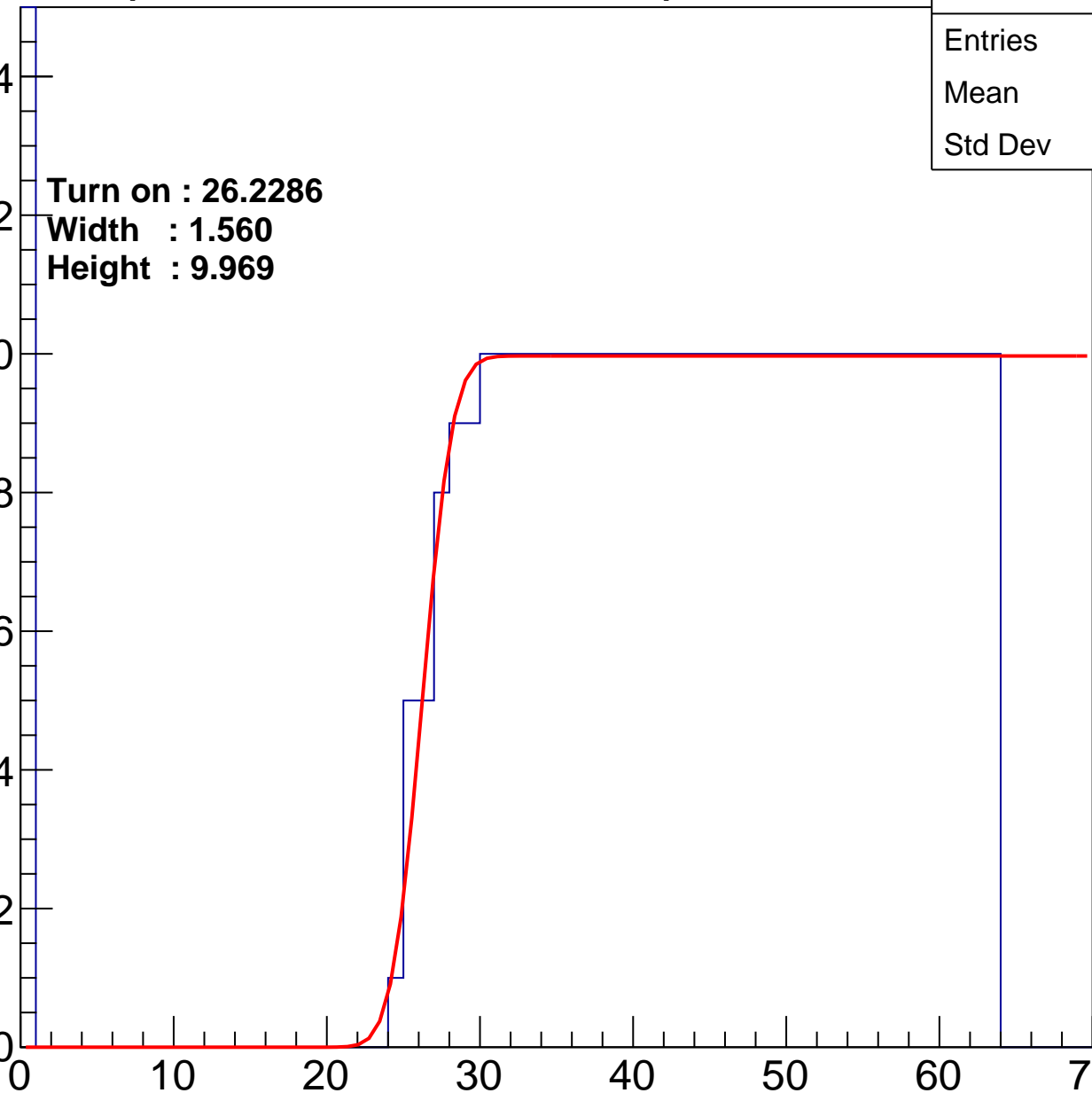
Width : 1.560

Height : 9.969

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch44

calib_packv5_041523_1651.root, FC#0, port C2

Entries	421
Mean	39.89
Std Dev	17.14

Turn on : 26.6595

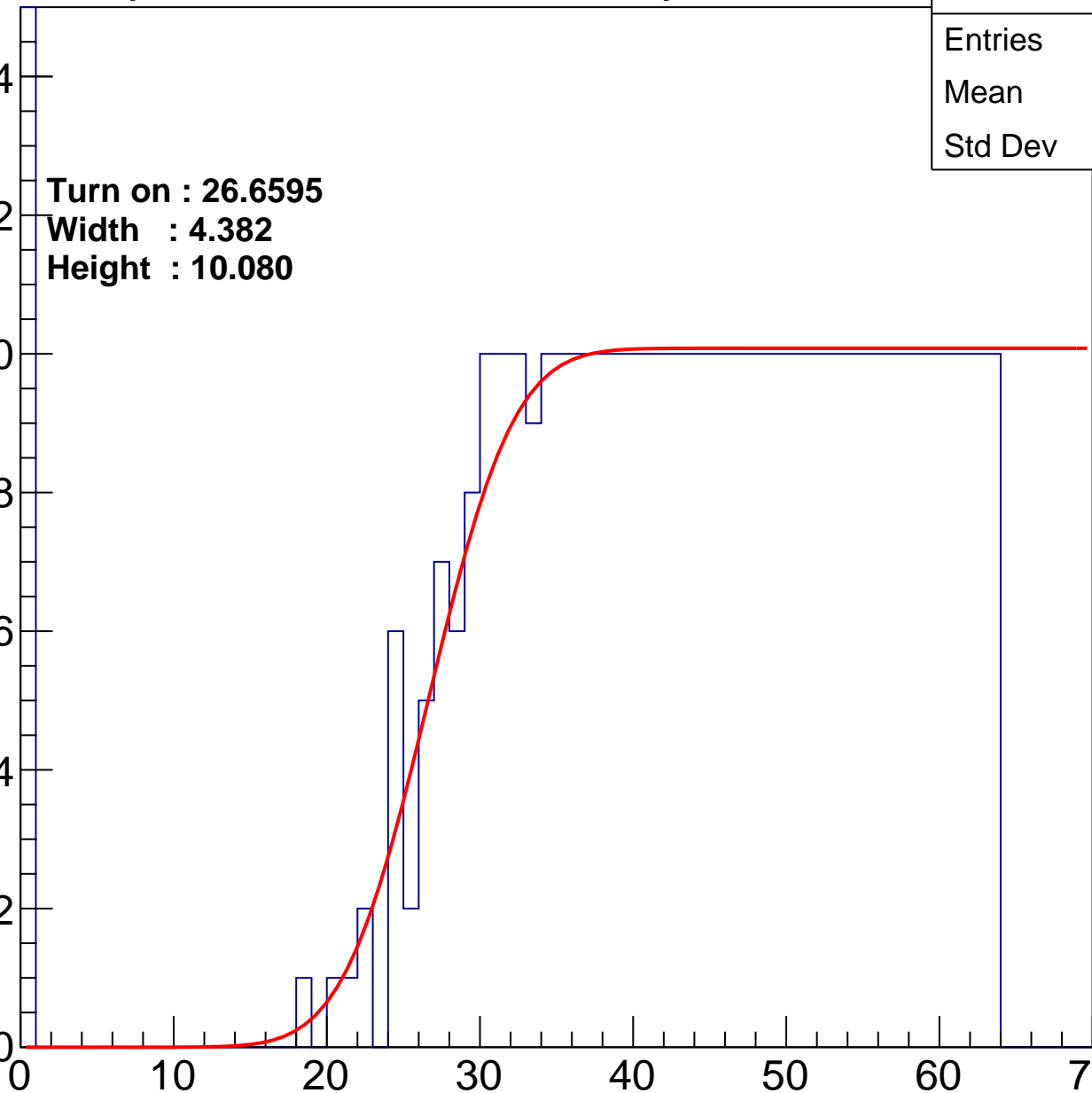
Width : 4.382

Height : 10.080

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch45

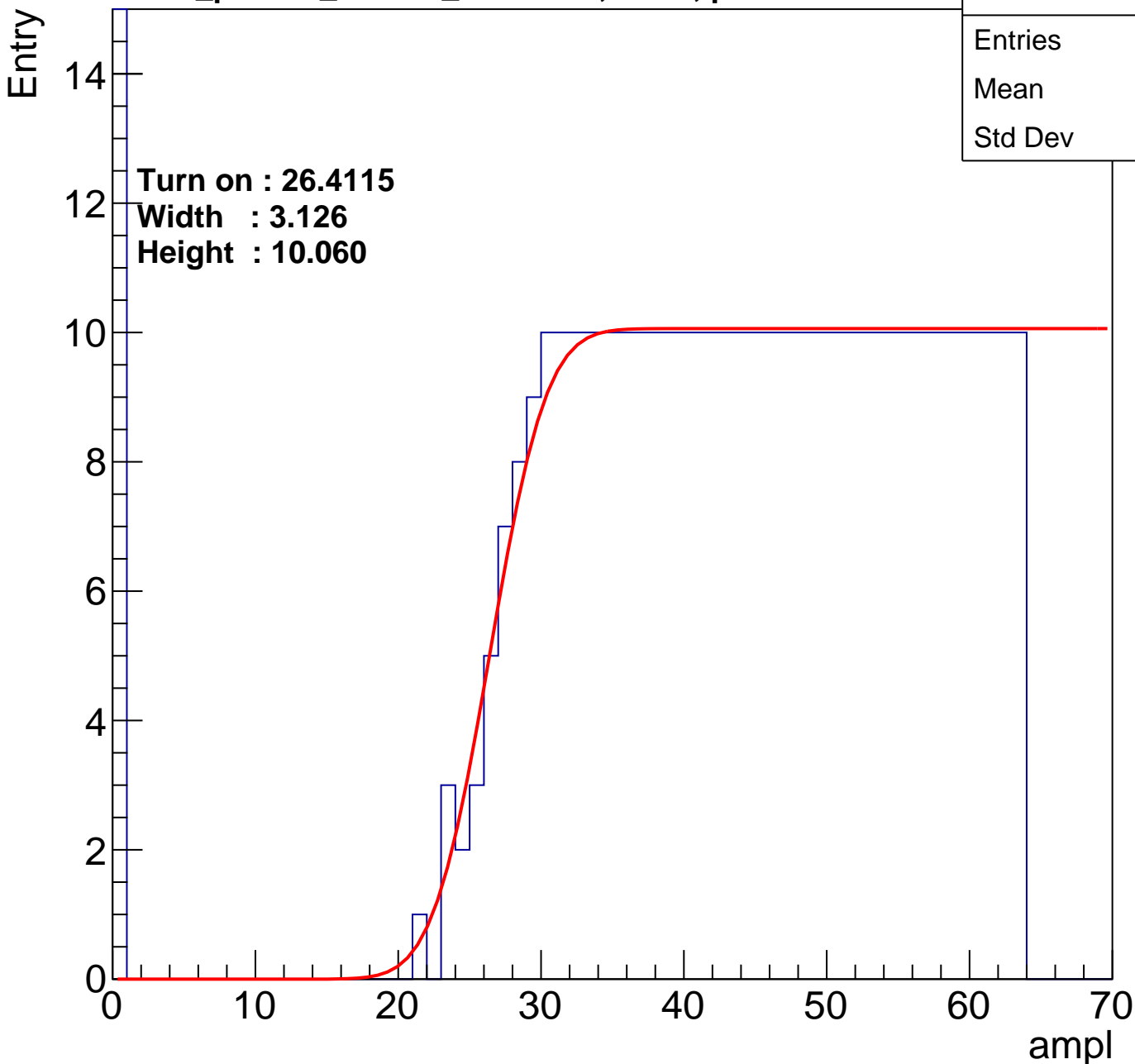
calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	39.5
Std Dev	17.51

Turn on : 26.4115

Width : 3.126

Height : 10.060



B1L103S, U19-ch46

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.19
Std Dev	17.78

Turn on : 26.5567

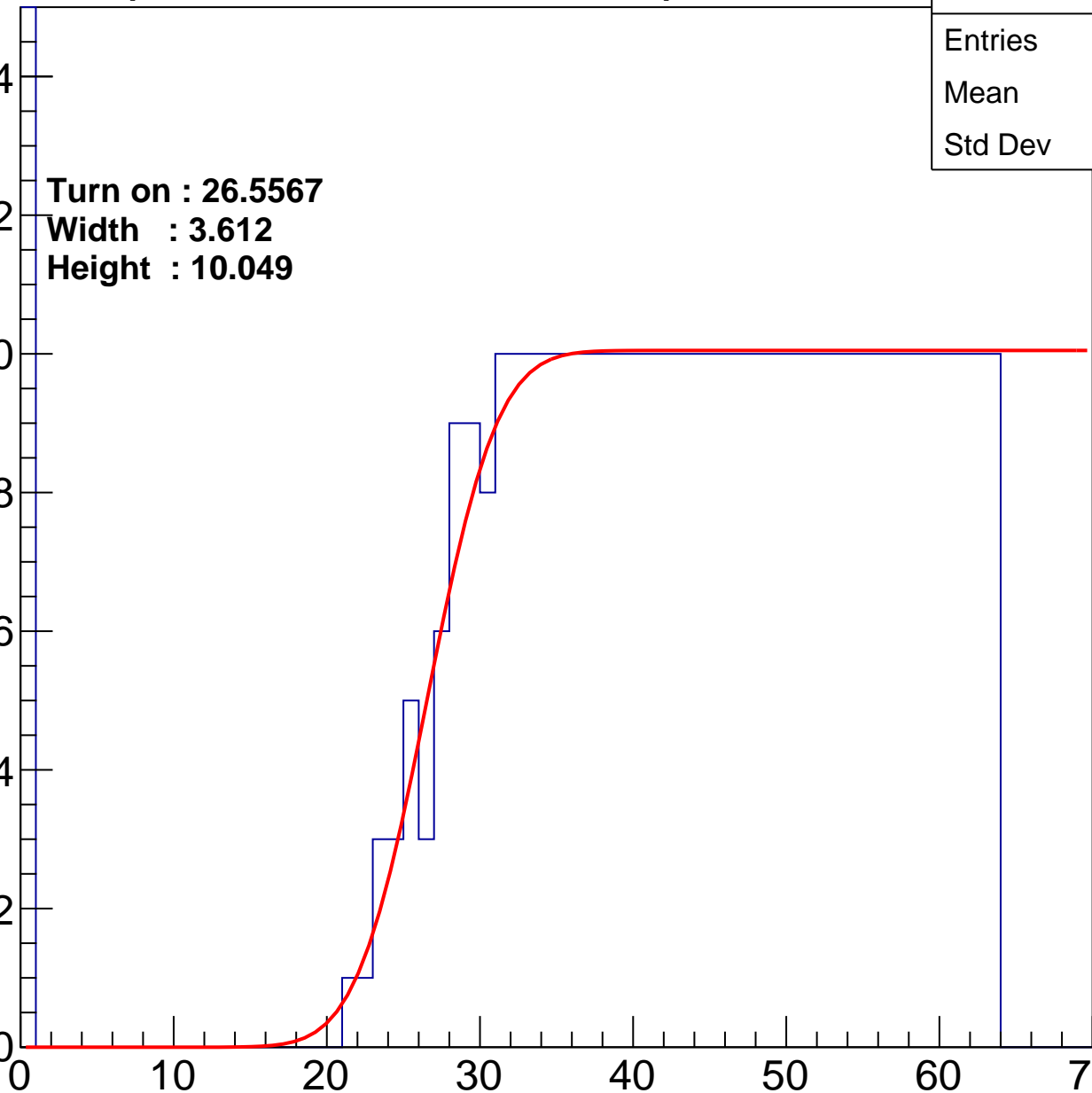
Width : 3.612

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch47

calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	39.36
Std Dev	17.3

Turn on : 25.3554

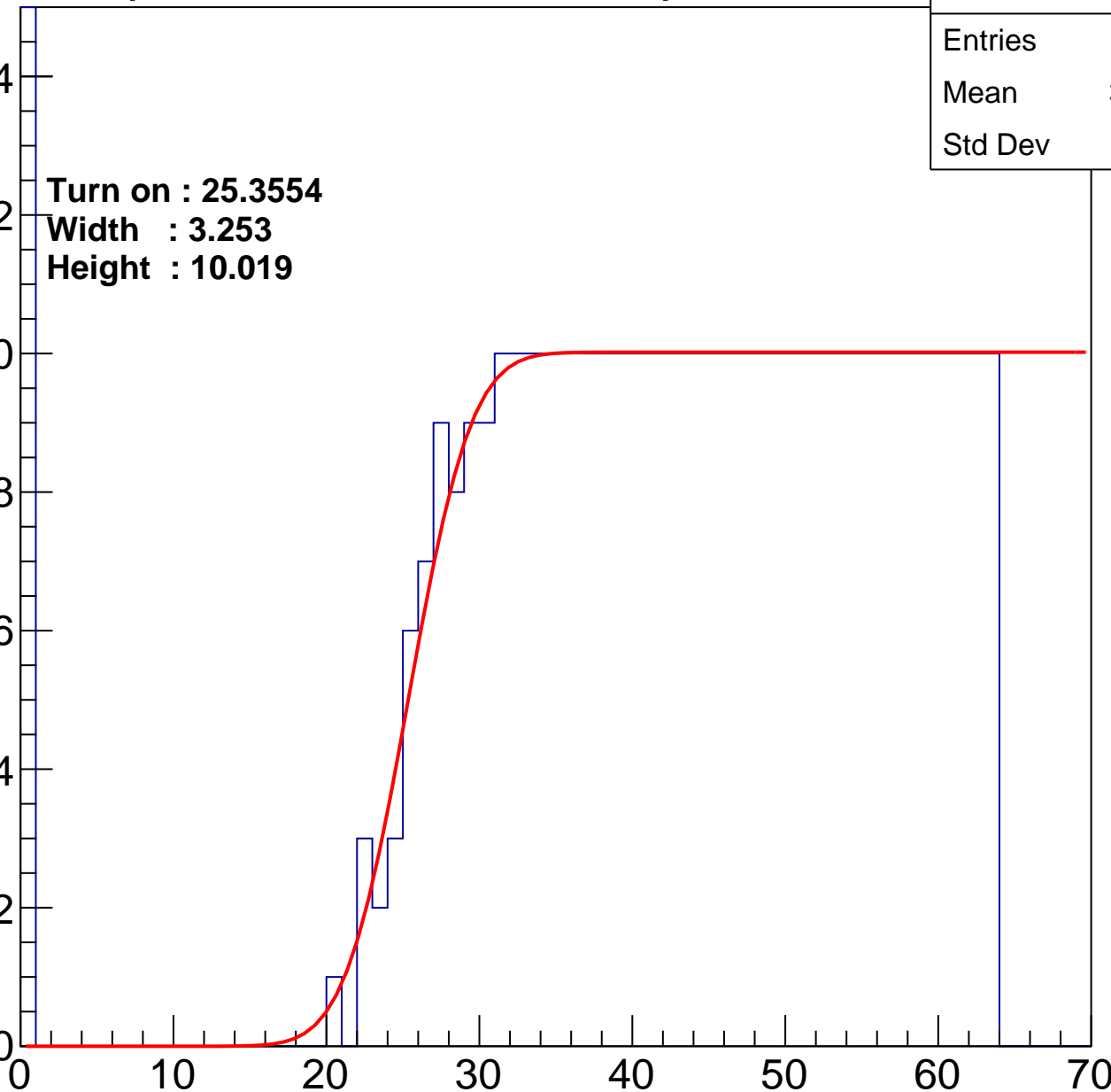
Width : 3.253

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch48

calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	39.62
Std Dev	16.88

Turn on : 25.0858

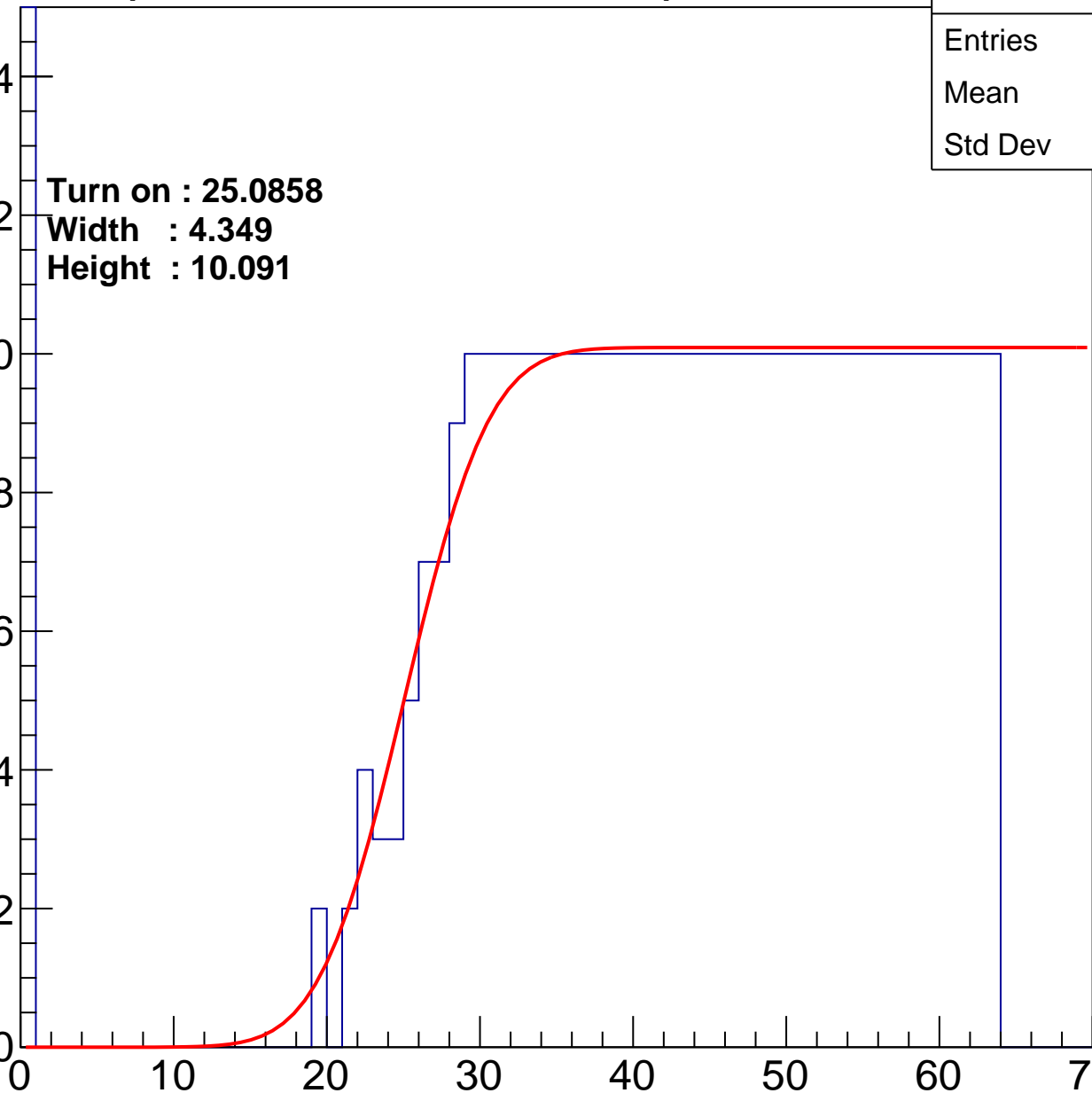
Width : 4.349

Height : 10.091

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch49

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	40.08
Std Dev	17

Turn on : 26.6609

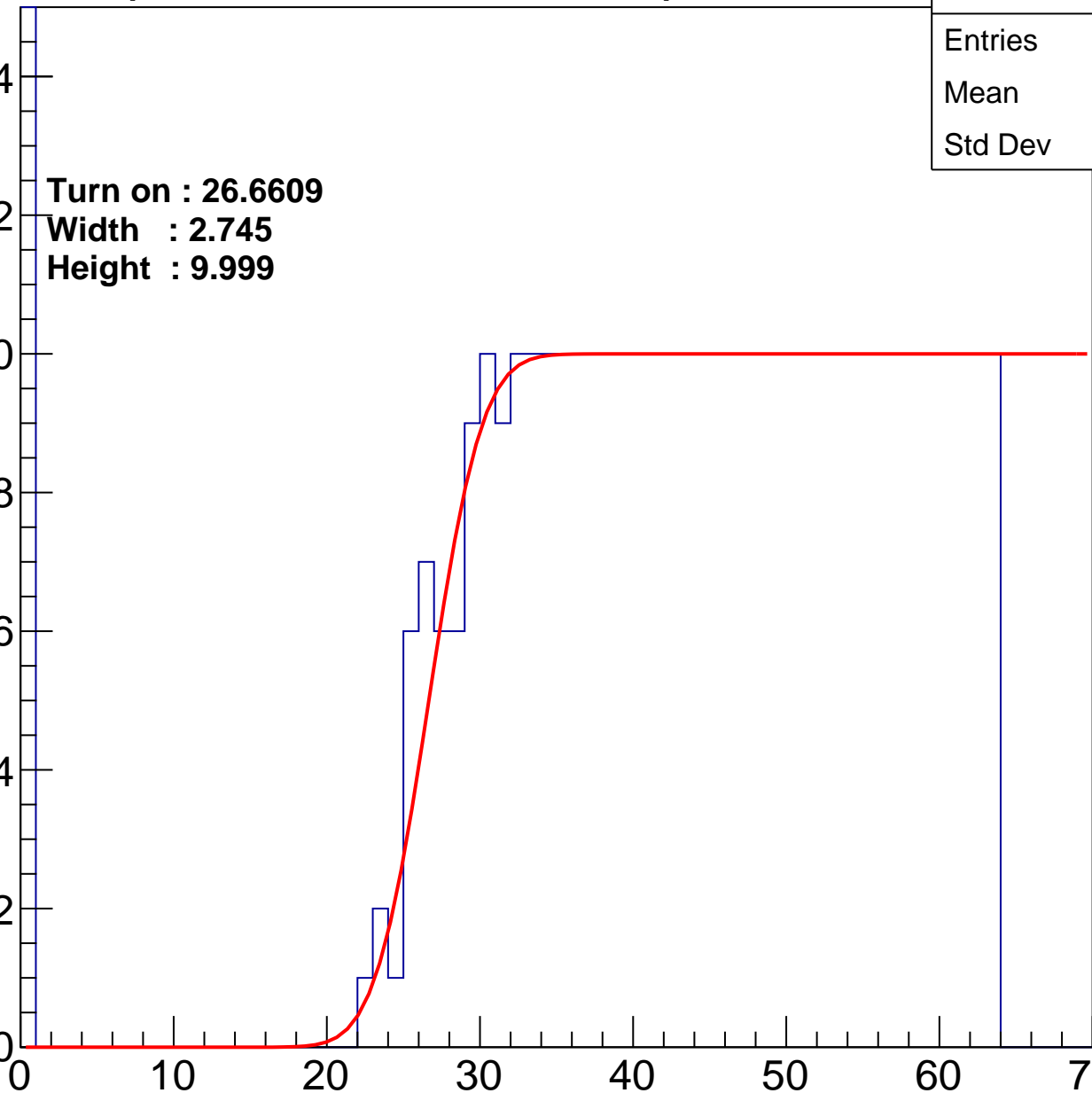
Width : 2.745

Height : 9.999

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch50

calib_packv5_041523_1651.root, FC#0, port C2

Entries	425
Mean	40.12
Std Dev	16.58

Turn on : 25.3438

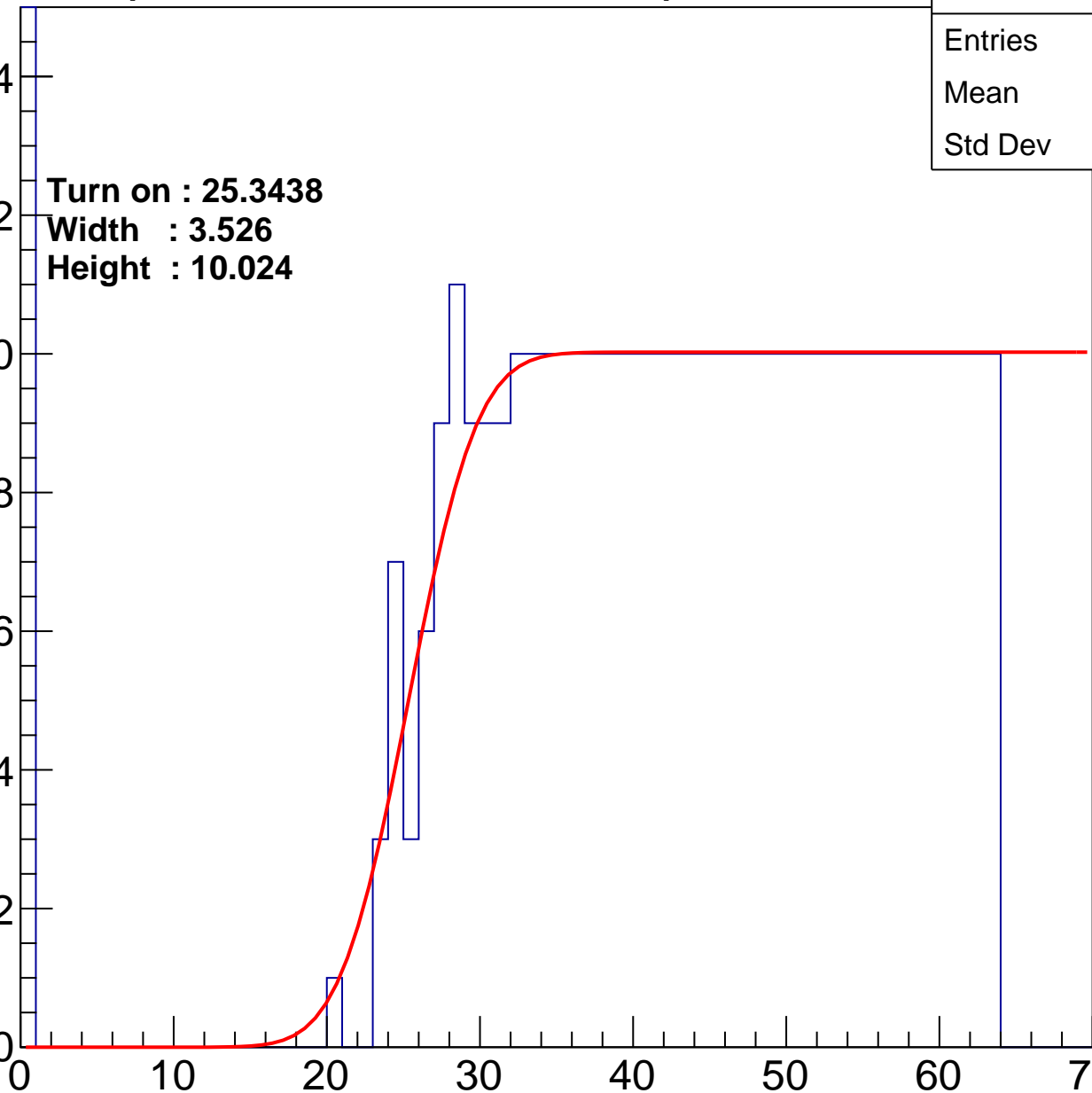
Width : 3.526

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch51

calib_packv5_041523_1651.root, FC#0, port C2

Entries	412
Mean	40.14
Std Dev	17.22

Turn on : 27.2380

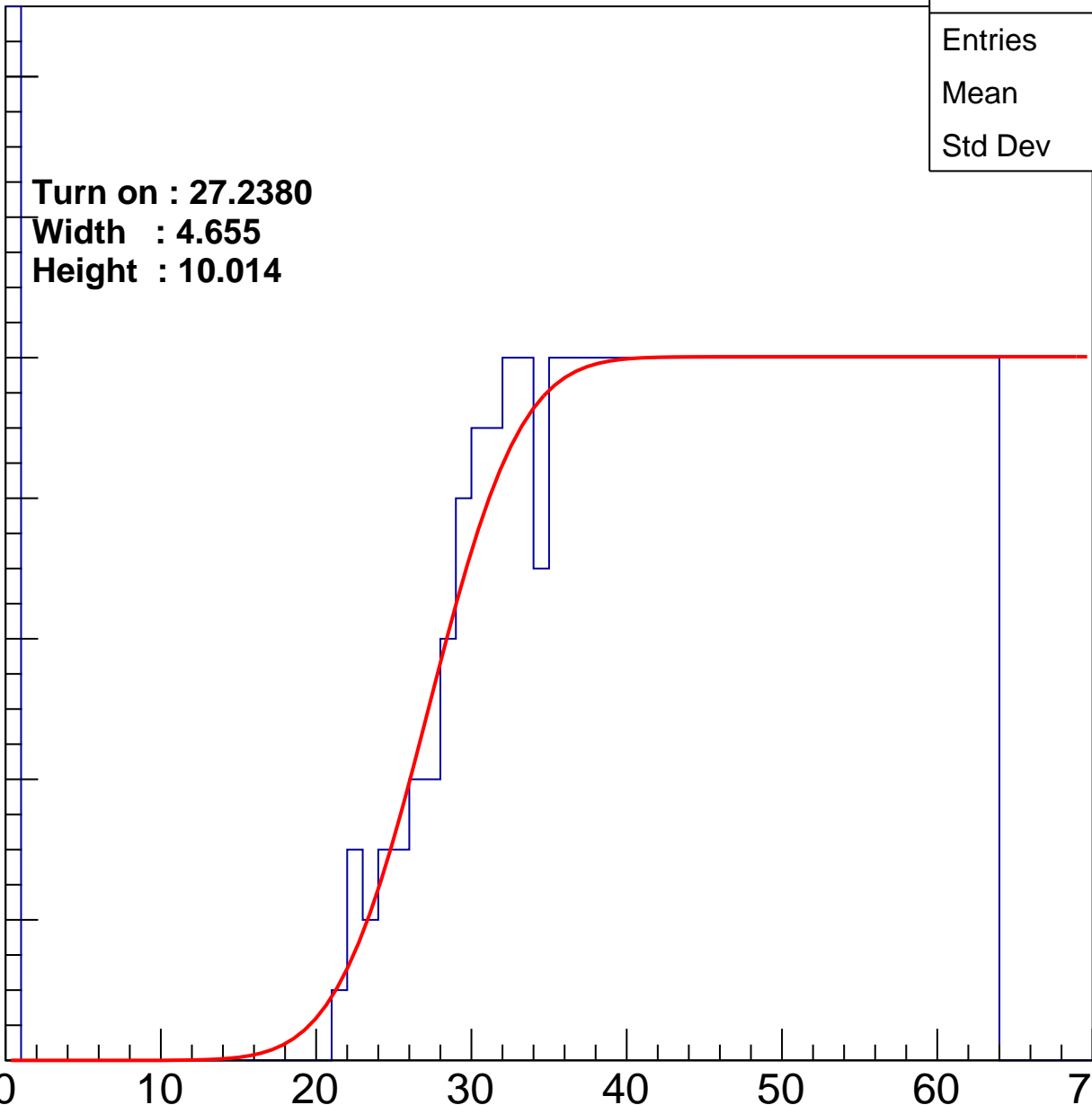
Width : 4.655

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch52

calib_packv5_041523_1651.root, FC#0, port C2

Entries	427
Mean	39.92
Std Dev	16.92

Turn on : 25.8207

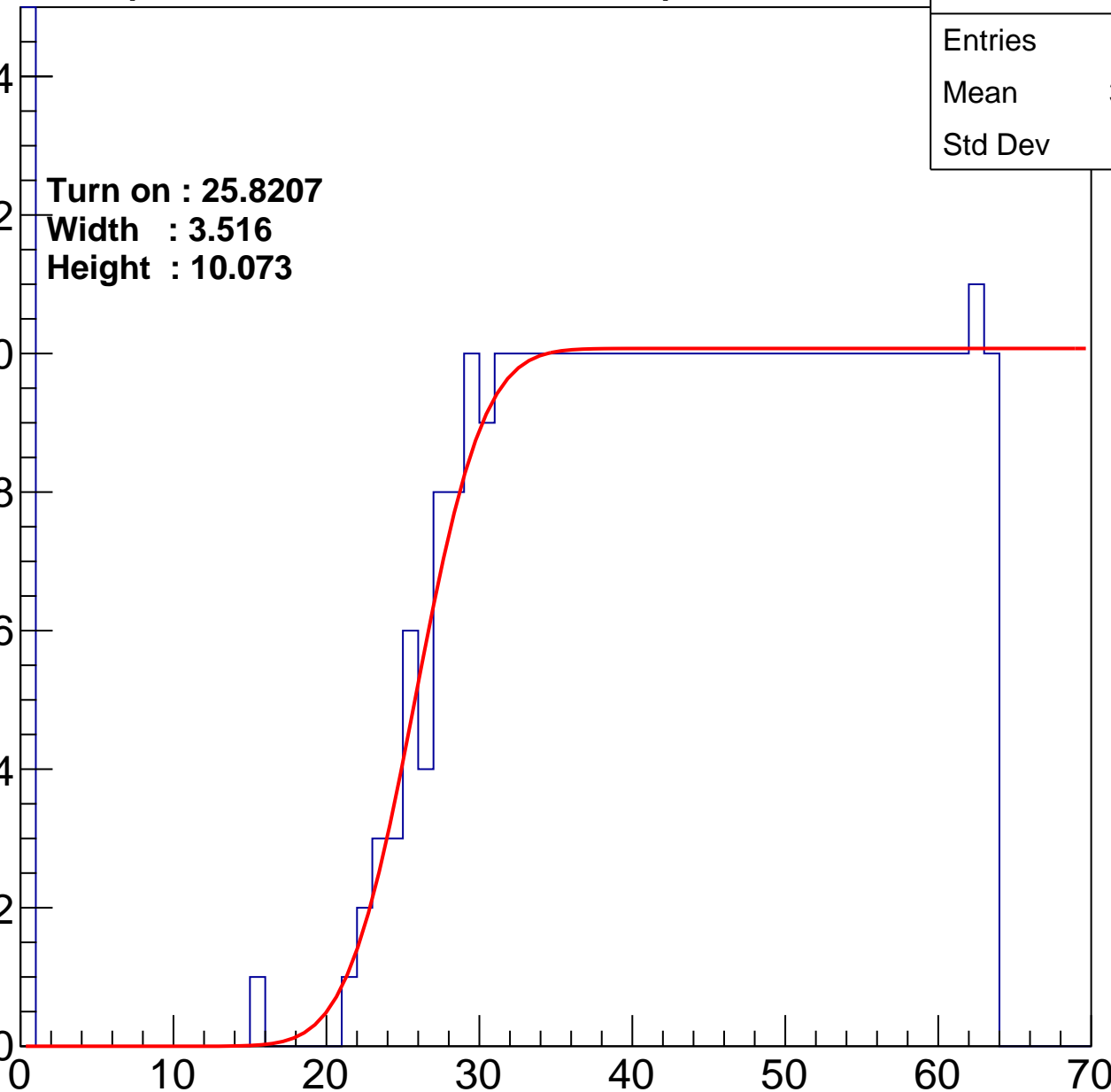
Width : 3.516

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch53

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.42
Std Dev	17.46

Turn on : 26.3575

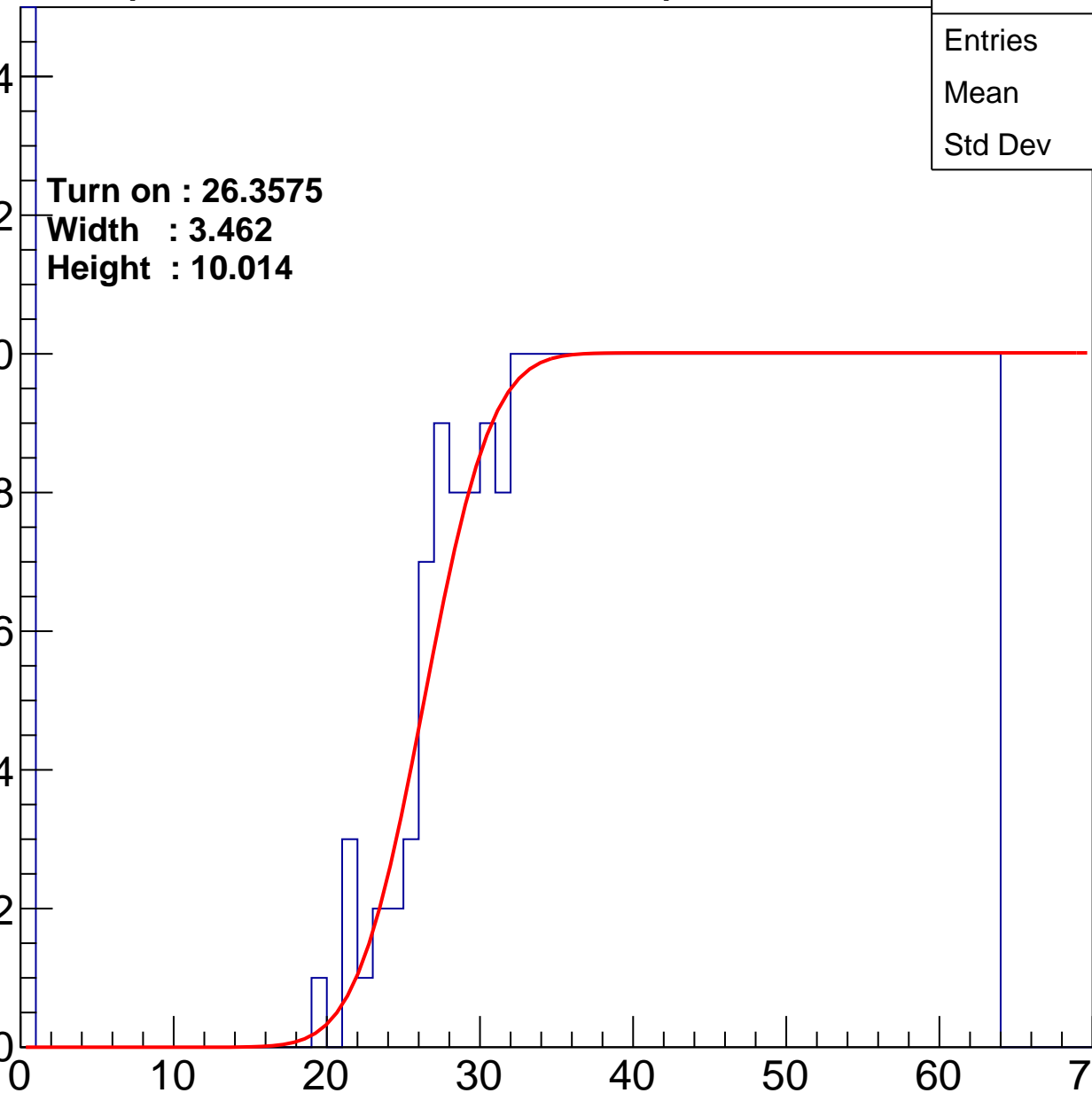
Width : 3.462

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch54

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	39.36
Std Dev	17.17

Turn on : 25.1713

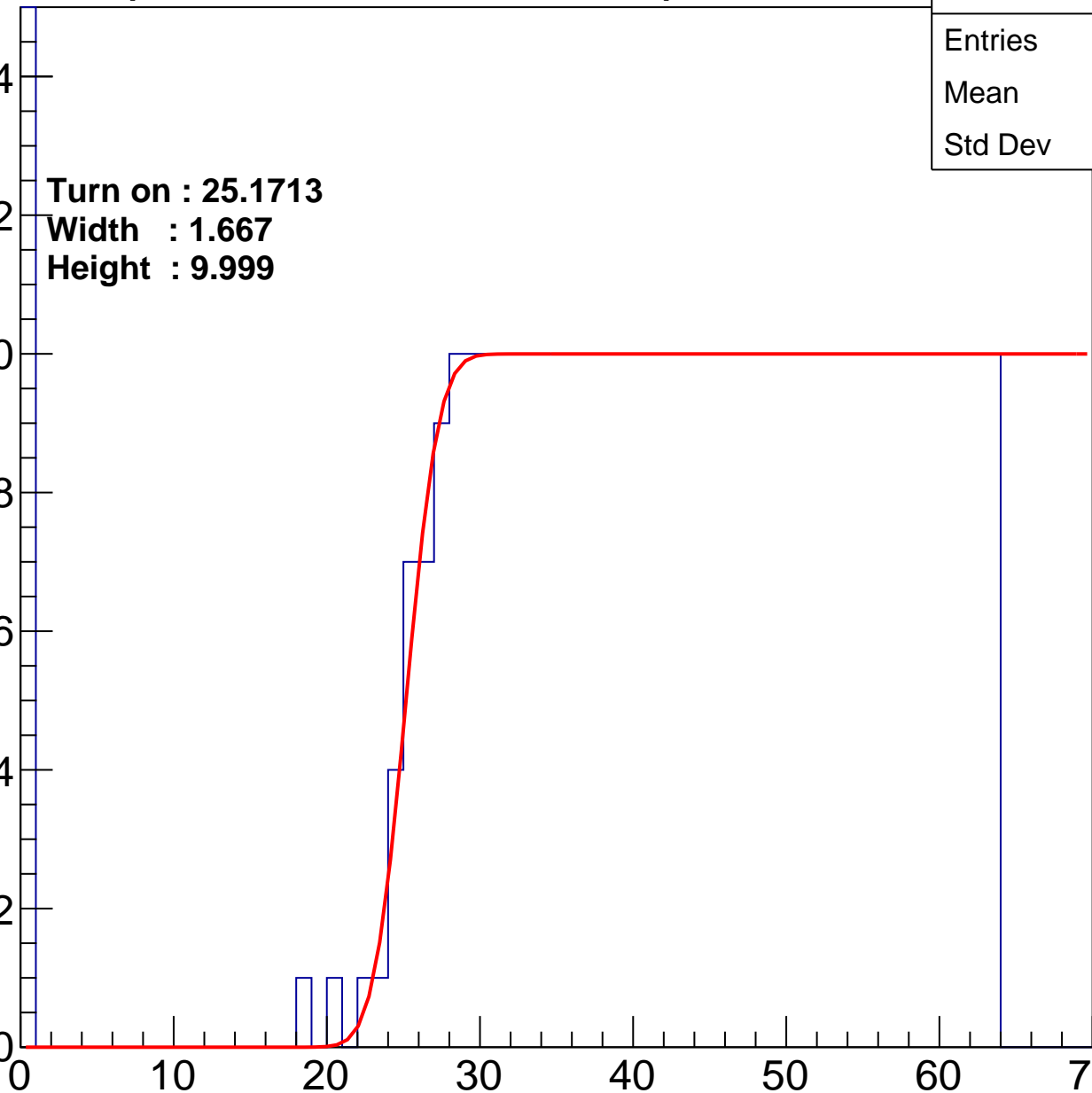
Width : 1.667

Height : 9.999

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch55

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	39.18
Std Dev	17.71

Turn on : 26.1327

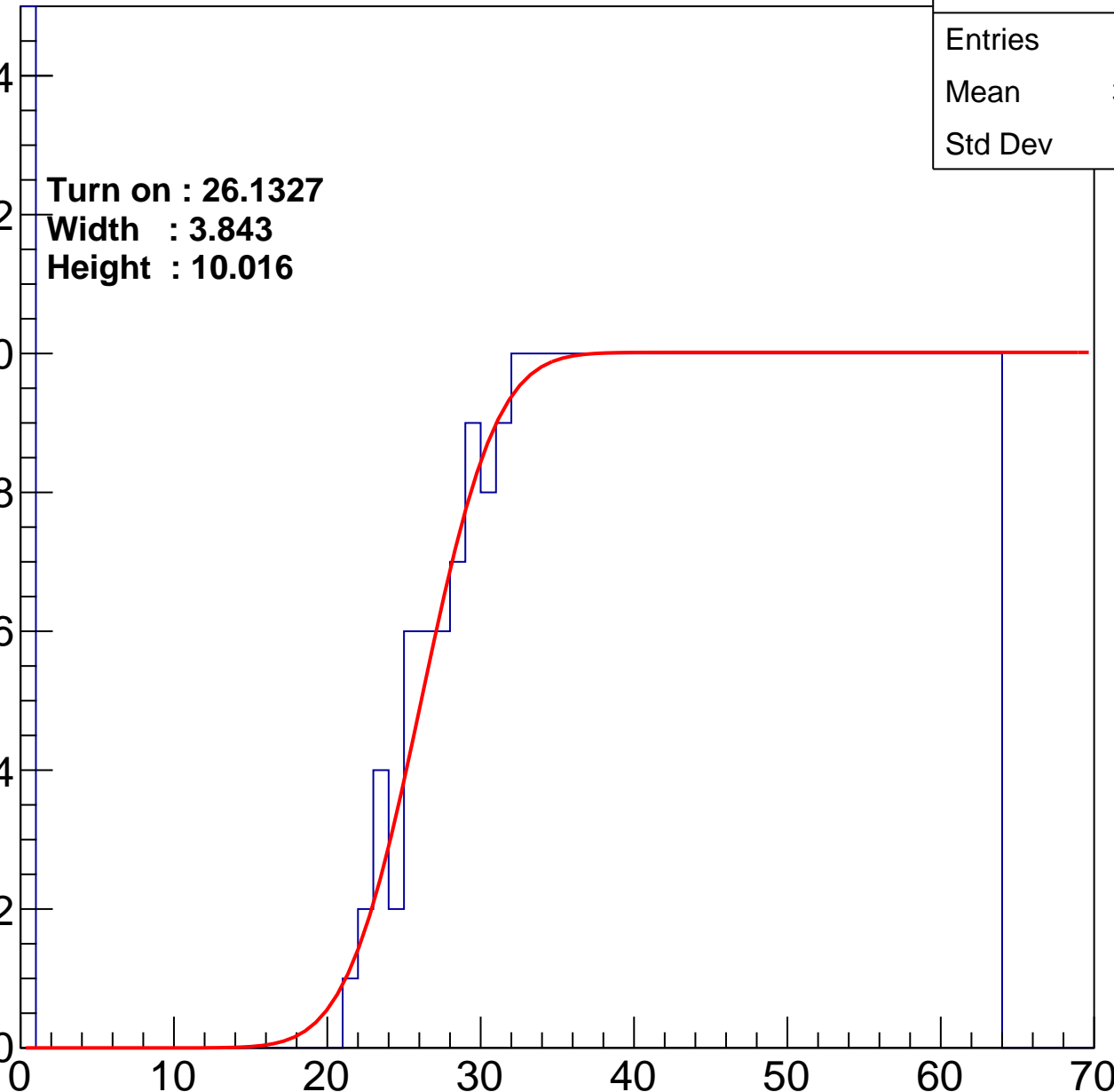
Width : 3.843

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch56

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	38.7
Std Dev	18.06

Turn on : 26.0878

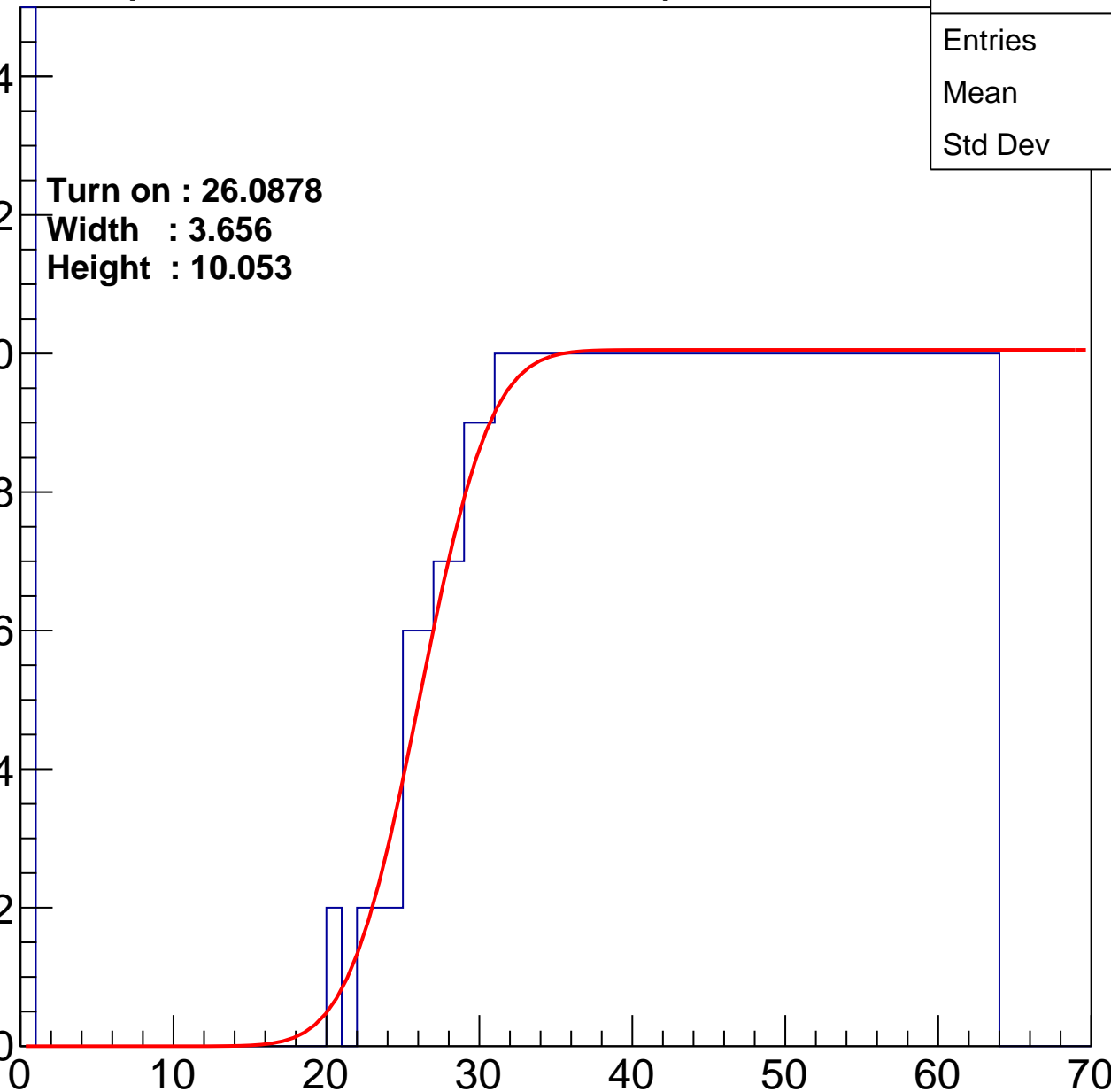
Width : 3.656

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch57

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	40.1
Std Dev	17.13

Turn on : 26.5676

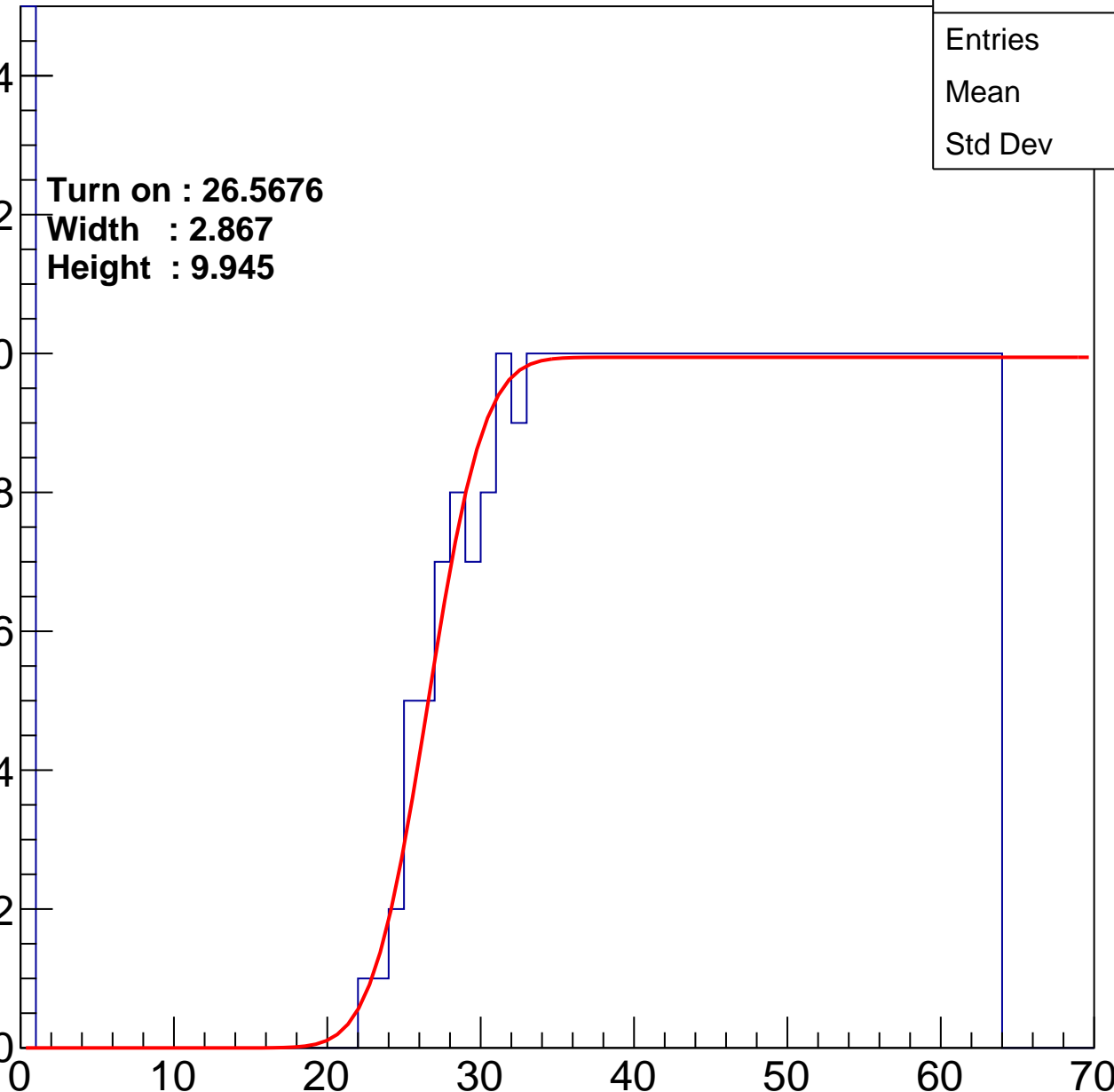
Width : 2.867

Height : 9.945

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch58

calib_packv5_041523_1651.root, FC#0, port C2

Entries	451
Mean	38.81
Std Dev	17.14

Turn on : 24.0756

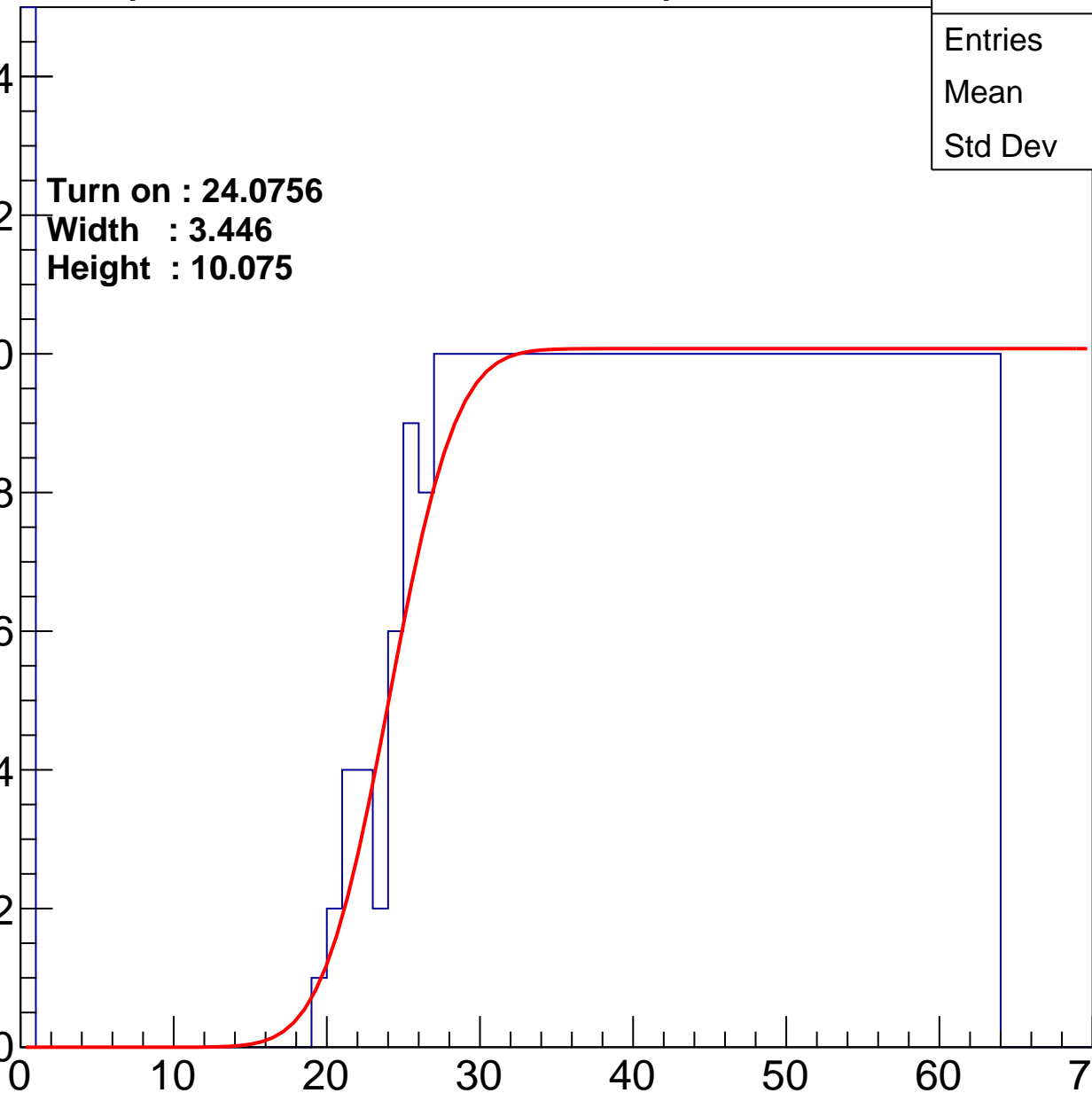
Width : 3.446

Height : 10.075

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch59

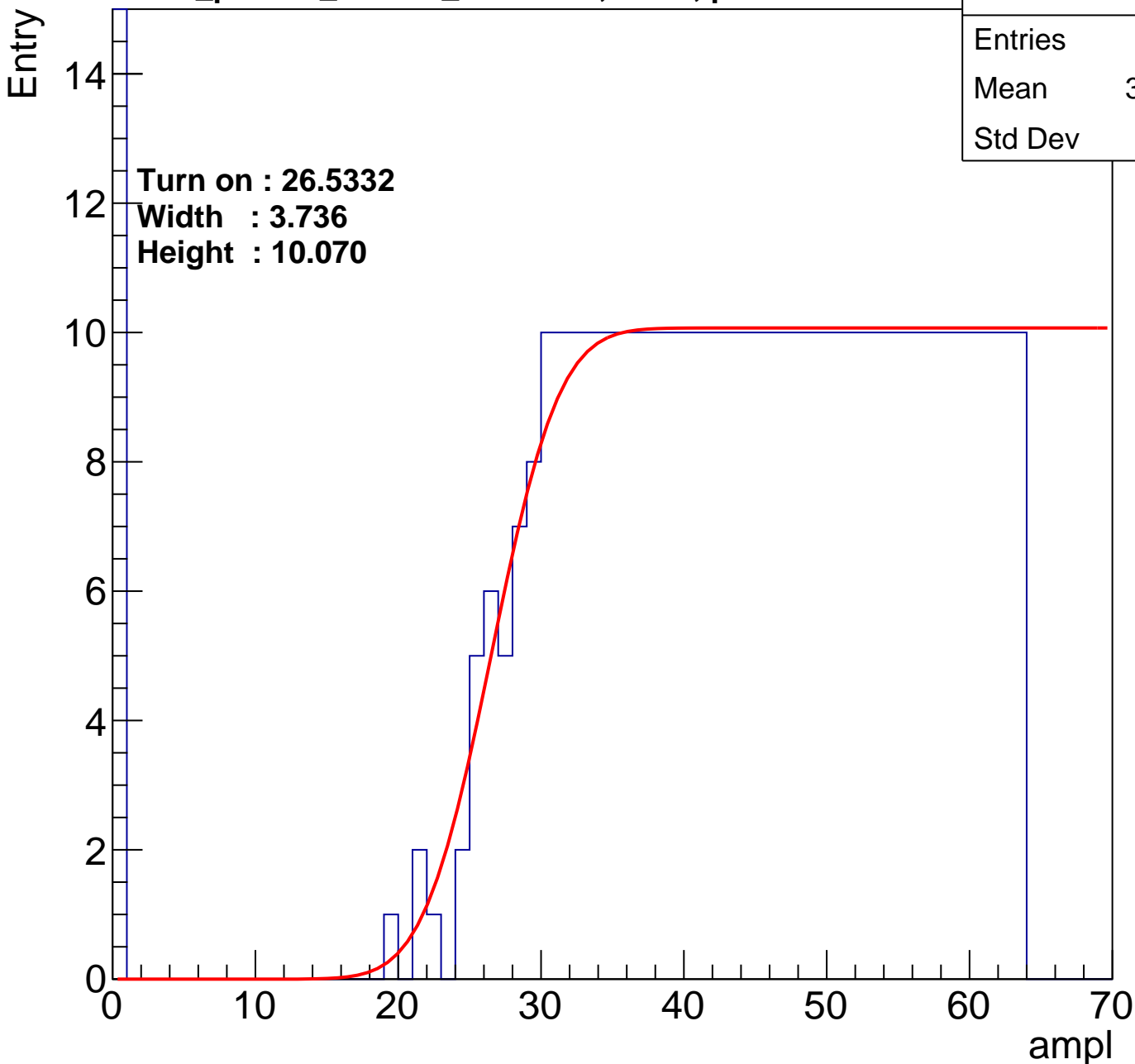
calib_packv5_041523_1651.root, FC#0, port C2

Entries	421
Mean	39.87
Std Dev	17.2

Turn on : 26.5332

Width : 3.736

Height : 10.070



B1L103S, U19-ch60

calib_packv5_041523_1651.root, FC#0, port C2

Entries	453
Mean	38.38
Std Dev	17.65

Turn on : 24.0142

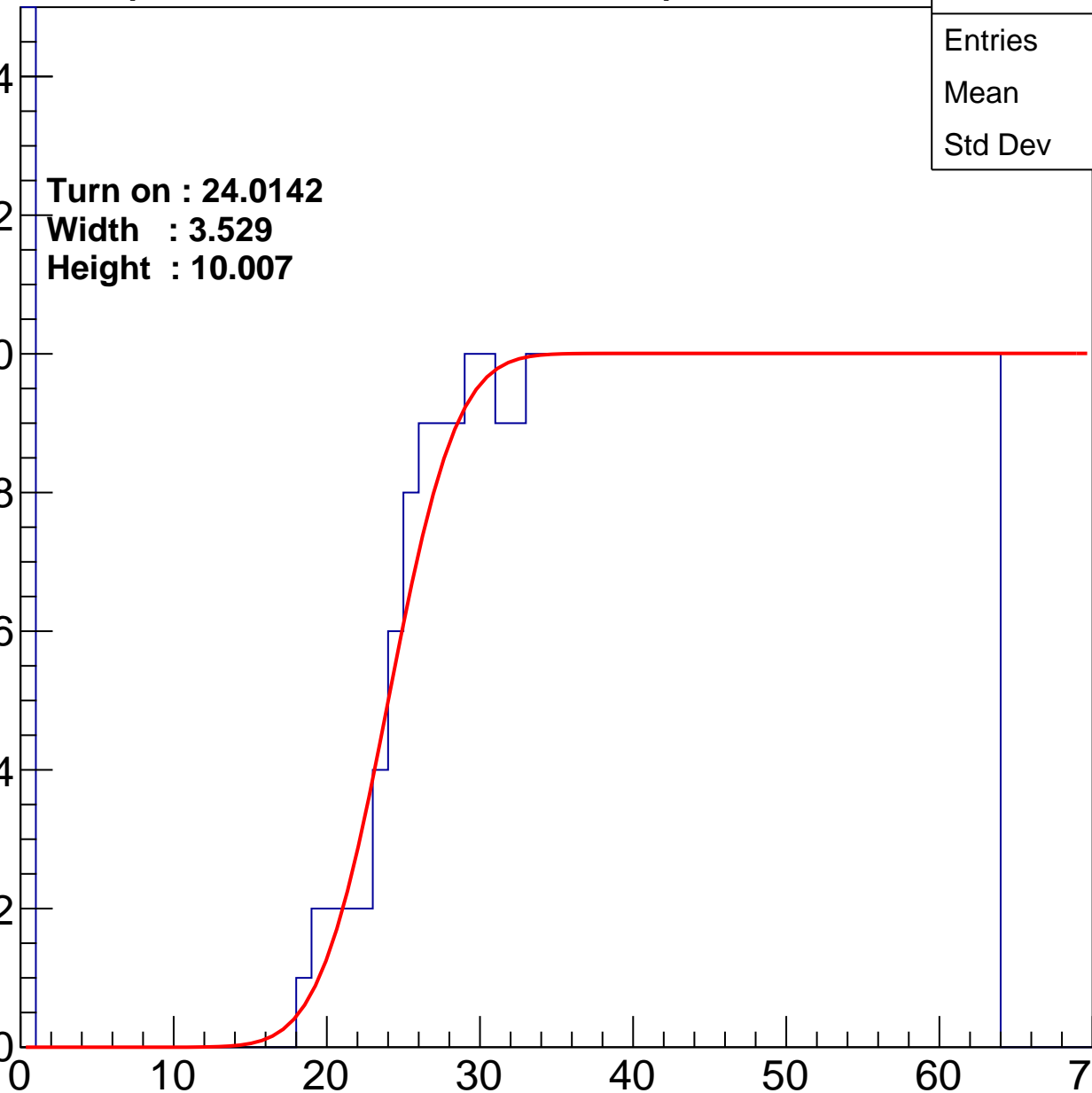
Width : 3.529

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch61

calib_packv5_041523_1651.root, FC#0, port C2

Entries	414
Mean	40.29
Std Dev	16.95

Turn on : 26.7844

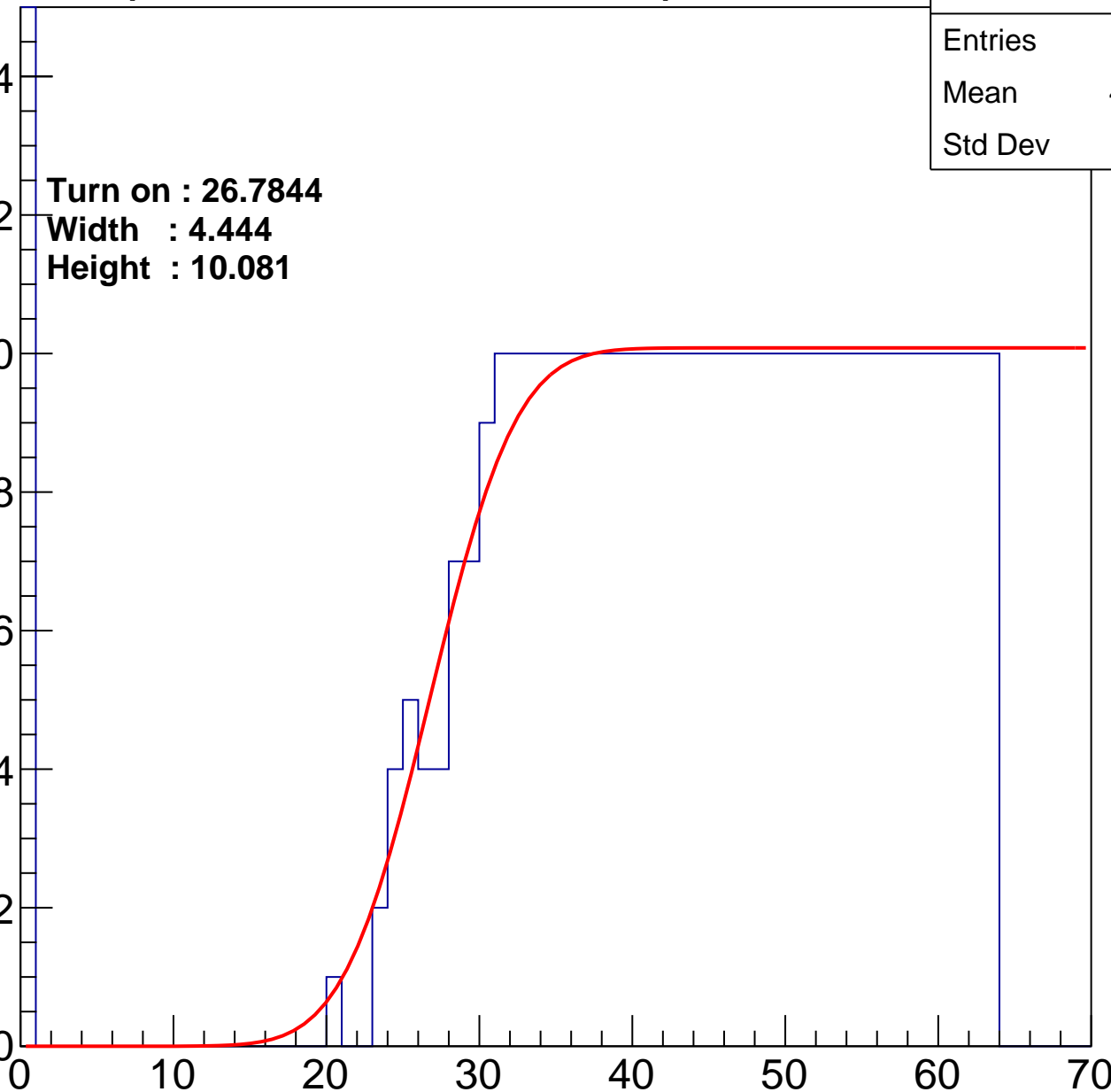
Width : 4.444

Height : 10.081

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch62

calib_packv5_041523_1651.root, FC#0, port C2

Entries	427
Mean	39.58
Std Dev	17.33

Turn on : 26.0070

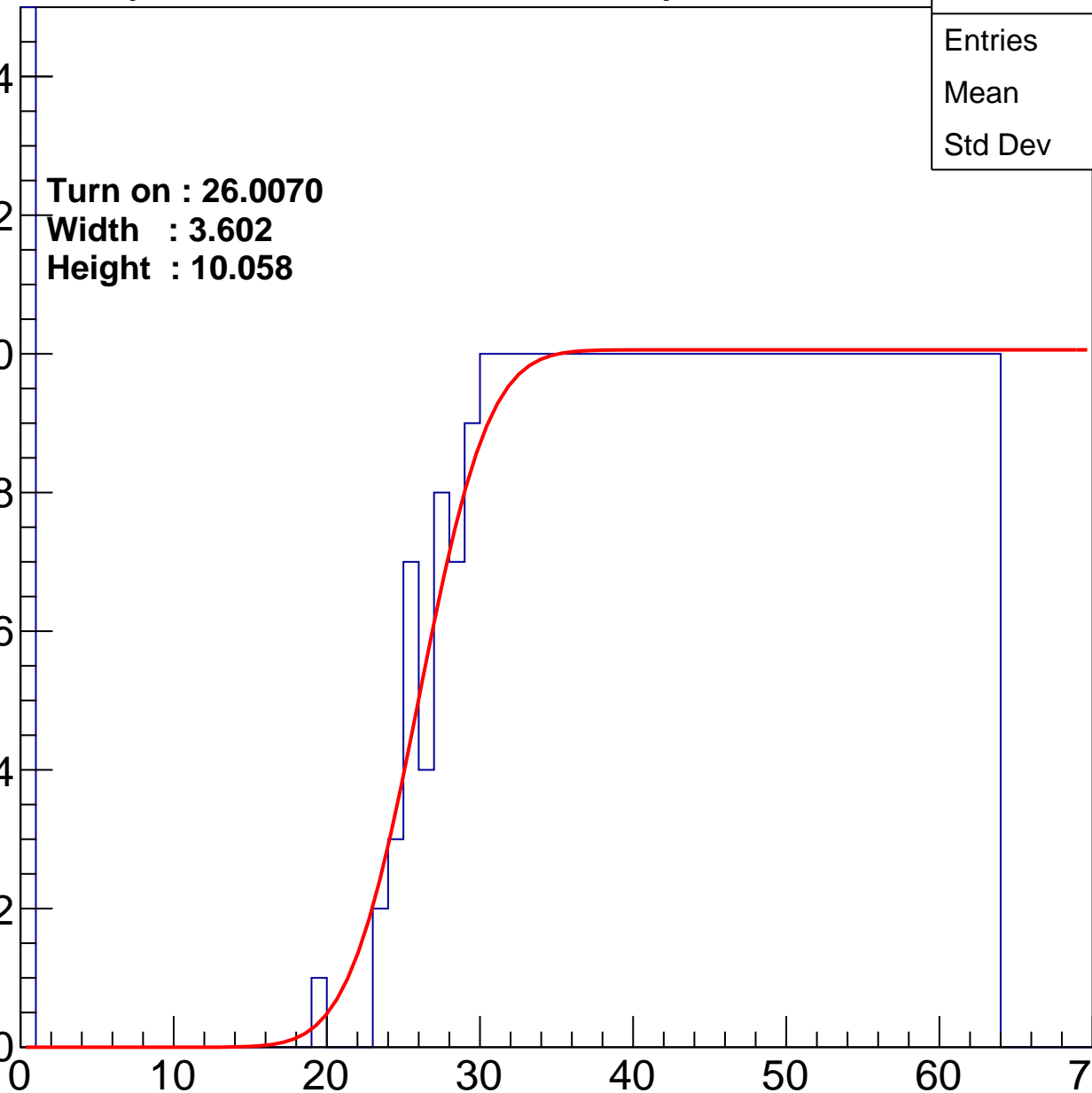
Width : 3.602

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch63

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	40.22
Std Dev	16.12

Turn on : 24.6801

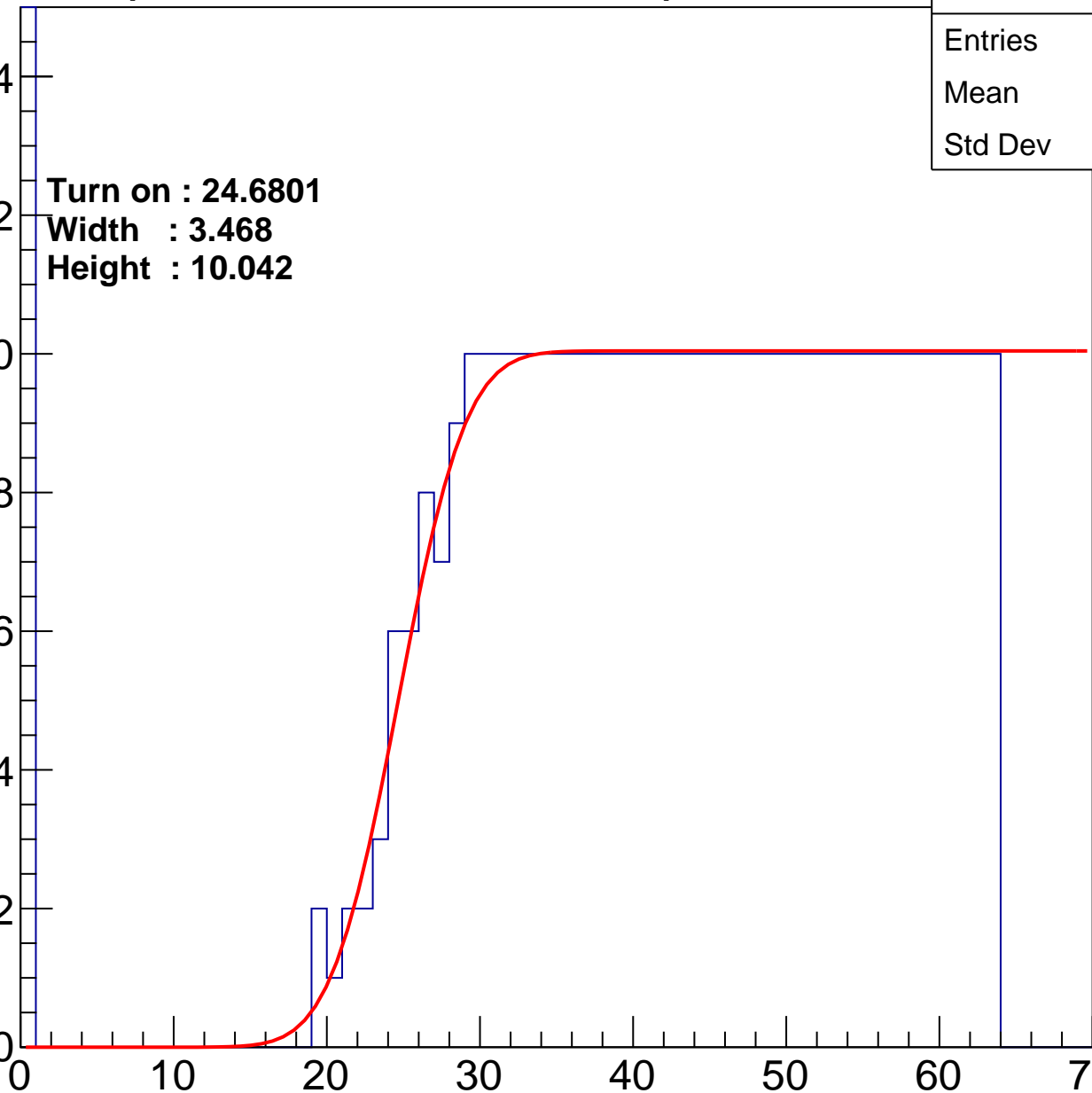
Width : 3.468

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch64

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	39.06
Std Dev	17.54

Turn on : 25.1550

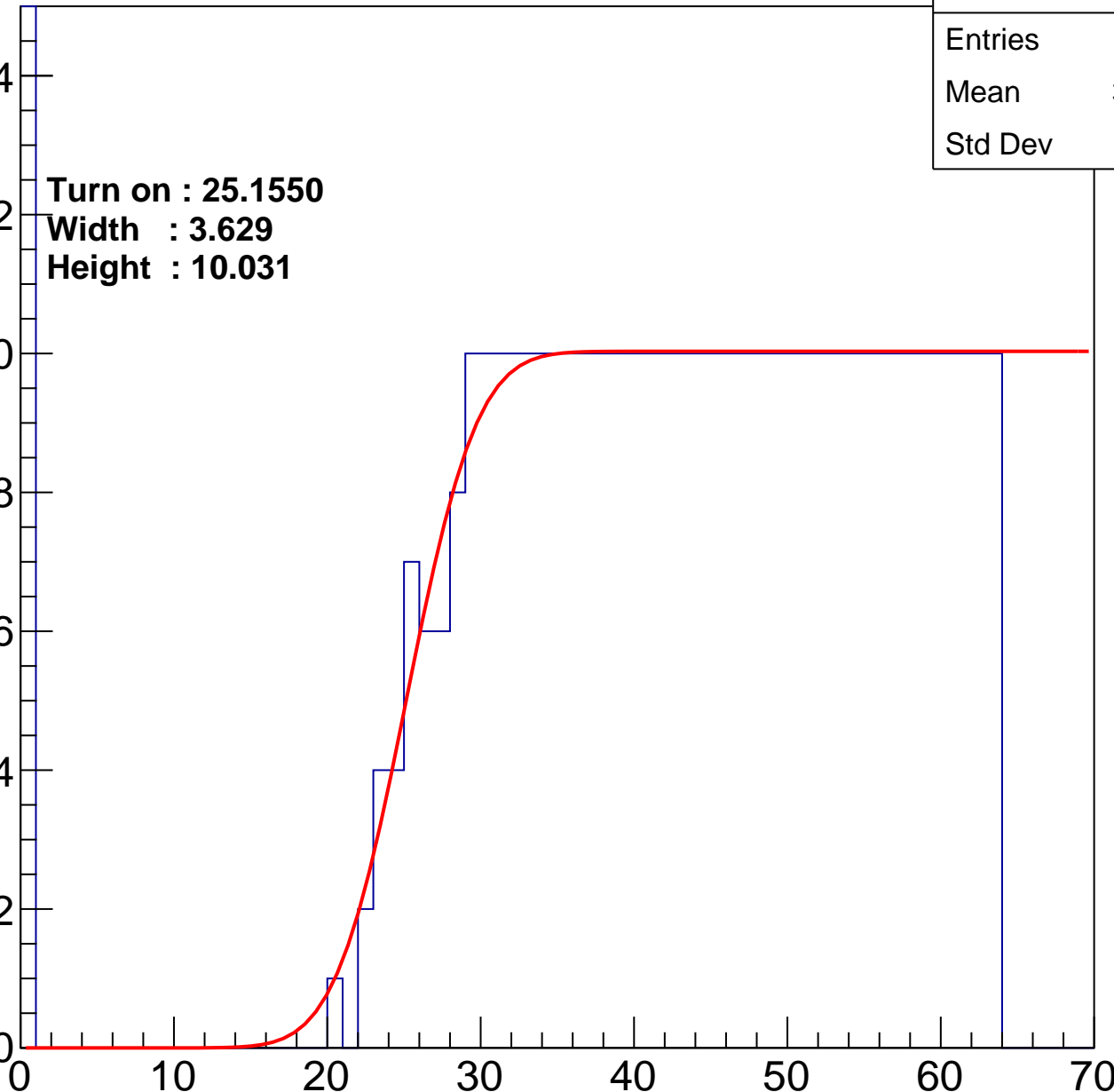
Width : 3.629

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch65

calib_packv5_041523_1651.root, FC#0, port C2

Entries	398
Mean	41.32
Std Dev	16.26

Turn on : 27.9183

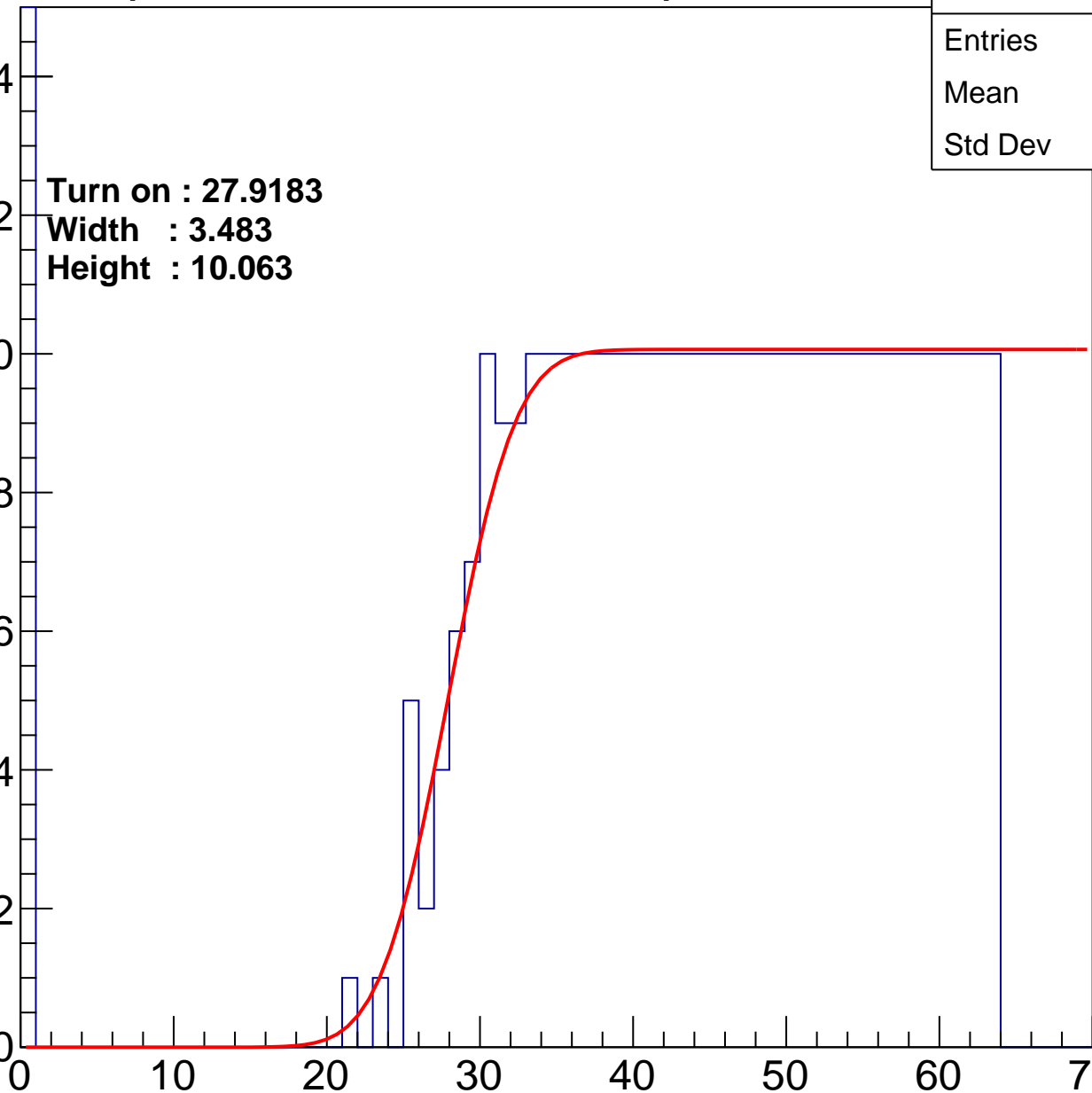
Width : 3.483

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch66

calib_packv5_041523_1651.root, FC#0, port C2

Entries	447
Mean	38.73
Std Dev	17.49

Turn on : 24.6307

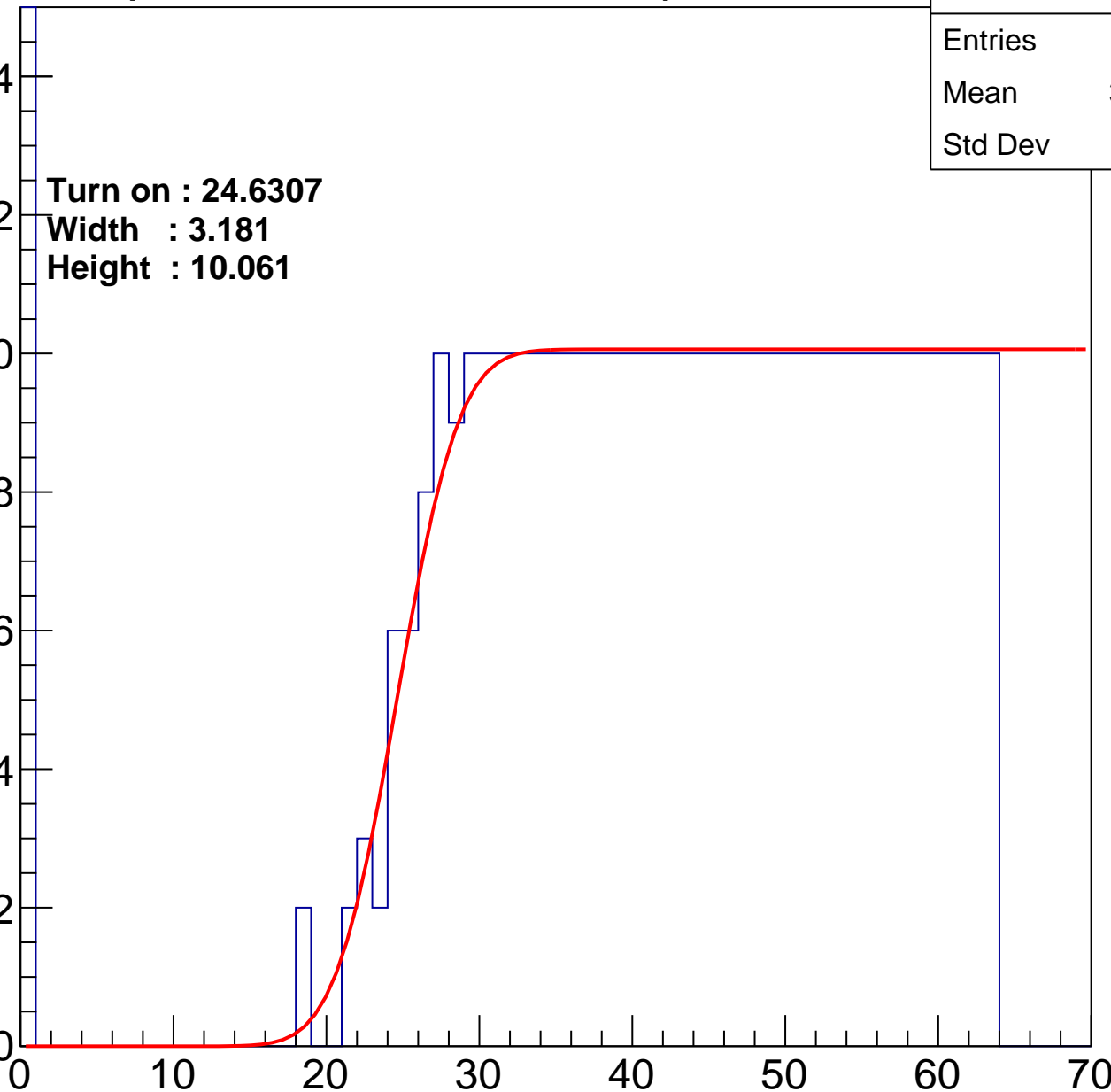
Width : 3.181

Height : 10.061

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch67

calib_packv5_041523_1651.root, FC#0, port C2

Entries	421
Mean	39.07
Std Dev	18.39

Turn on : 28.1051

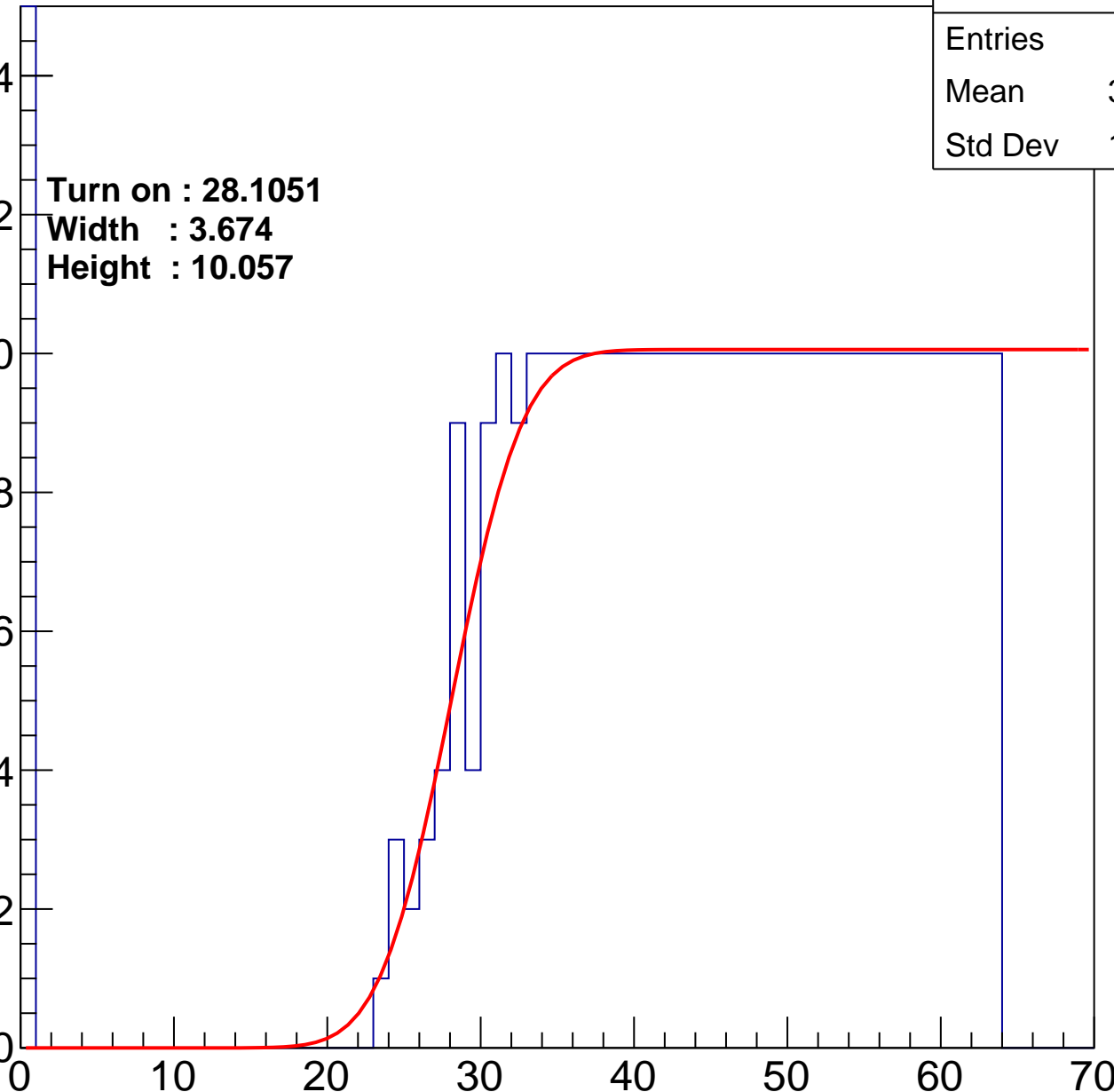
Width : 3.674

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch68

calib_packv5_041523_1651.root, FC#0, port C2

Entries	449
Mean	37.83
Std Dev	18.69

Turn on : 25.7362

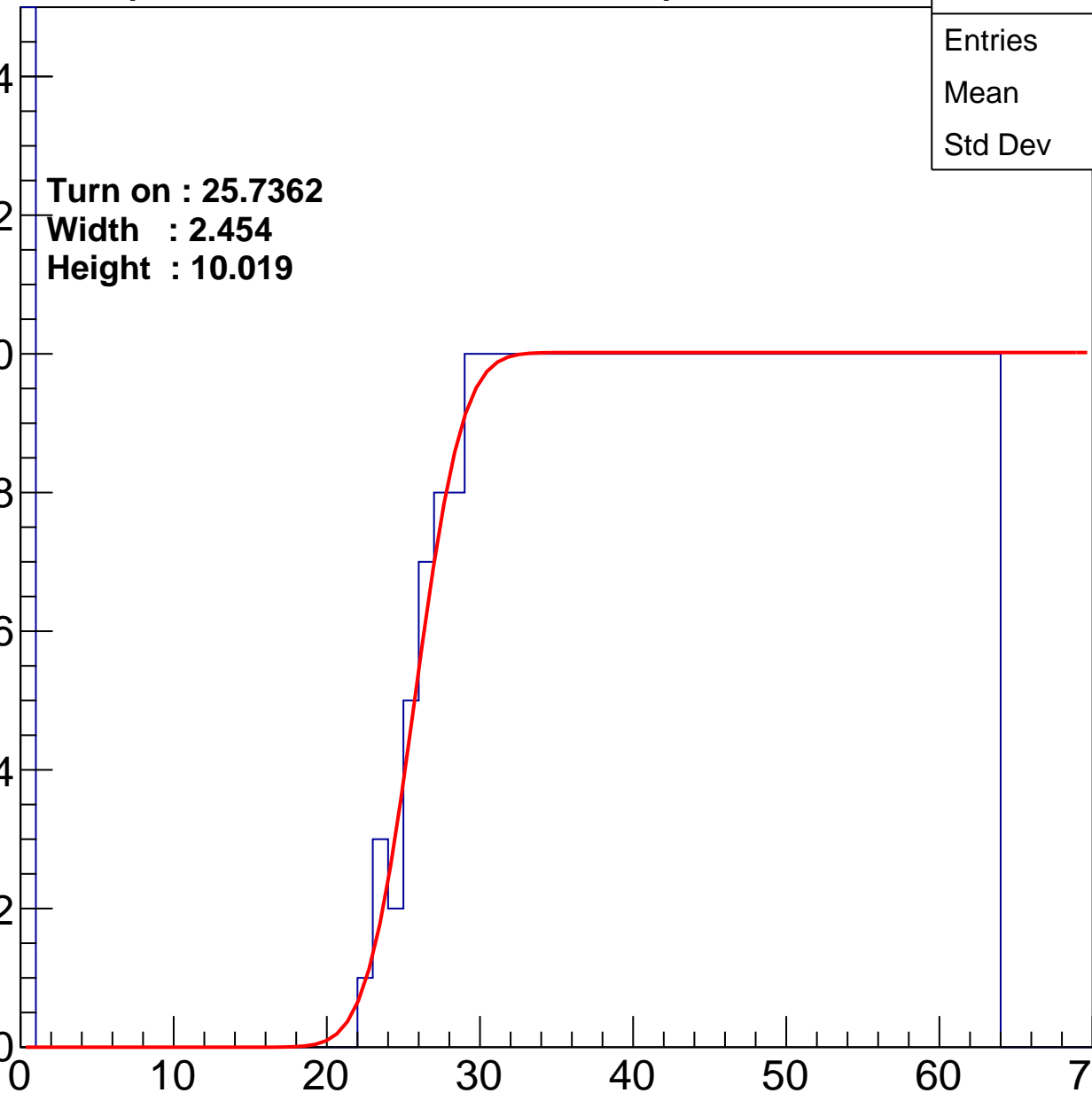
Width : 2.454

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch69

calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	39.64
Std Dev	16.85

Turn on : 24.7966

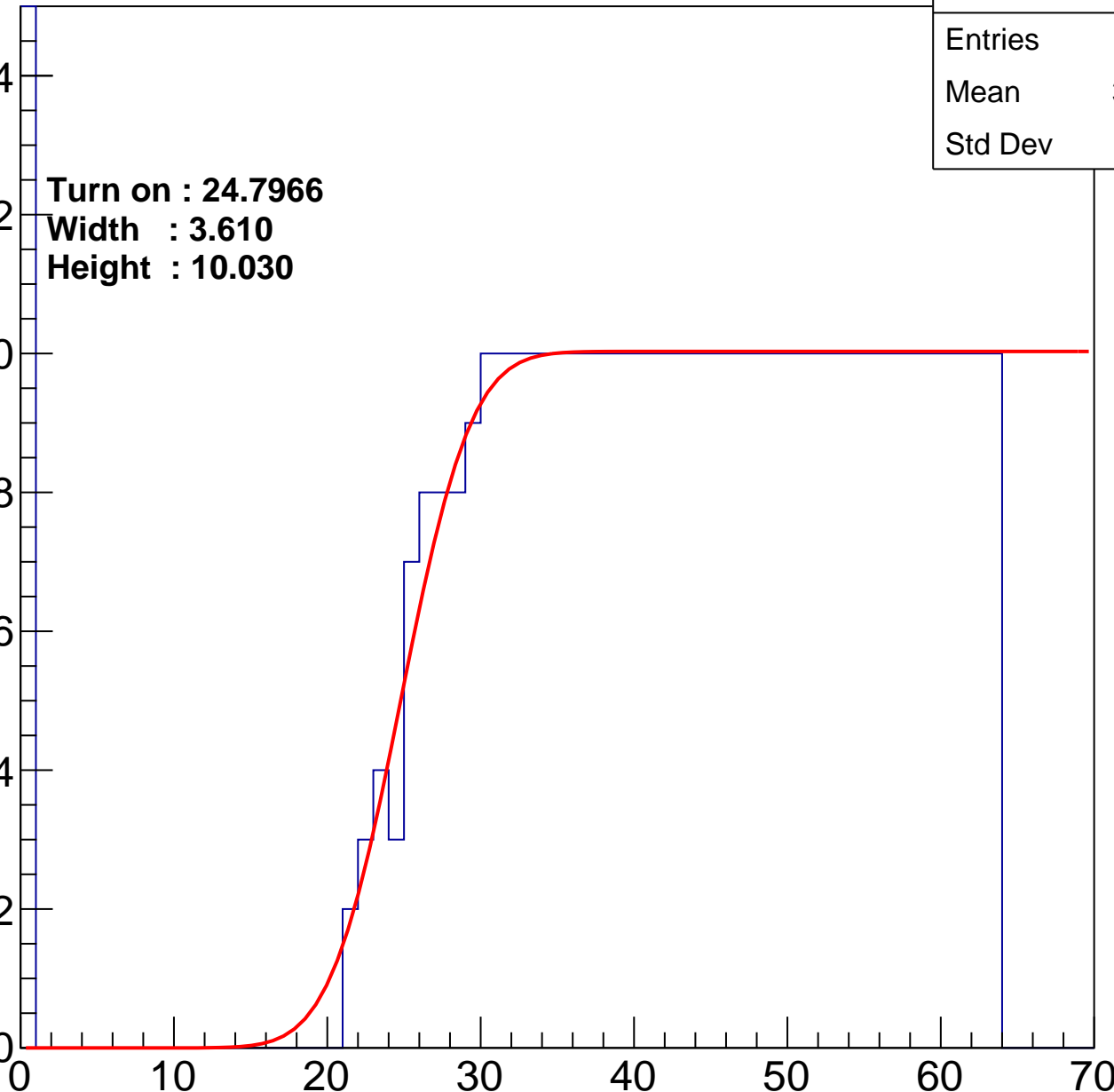
Width : 3.610

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch70

calib_packv5_041523_1651.root, FC#0, port C2

Entries	446
Mean	38.45
Std Dev	17.96

Turn on : 25.1257

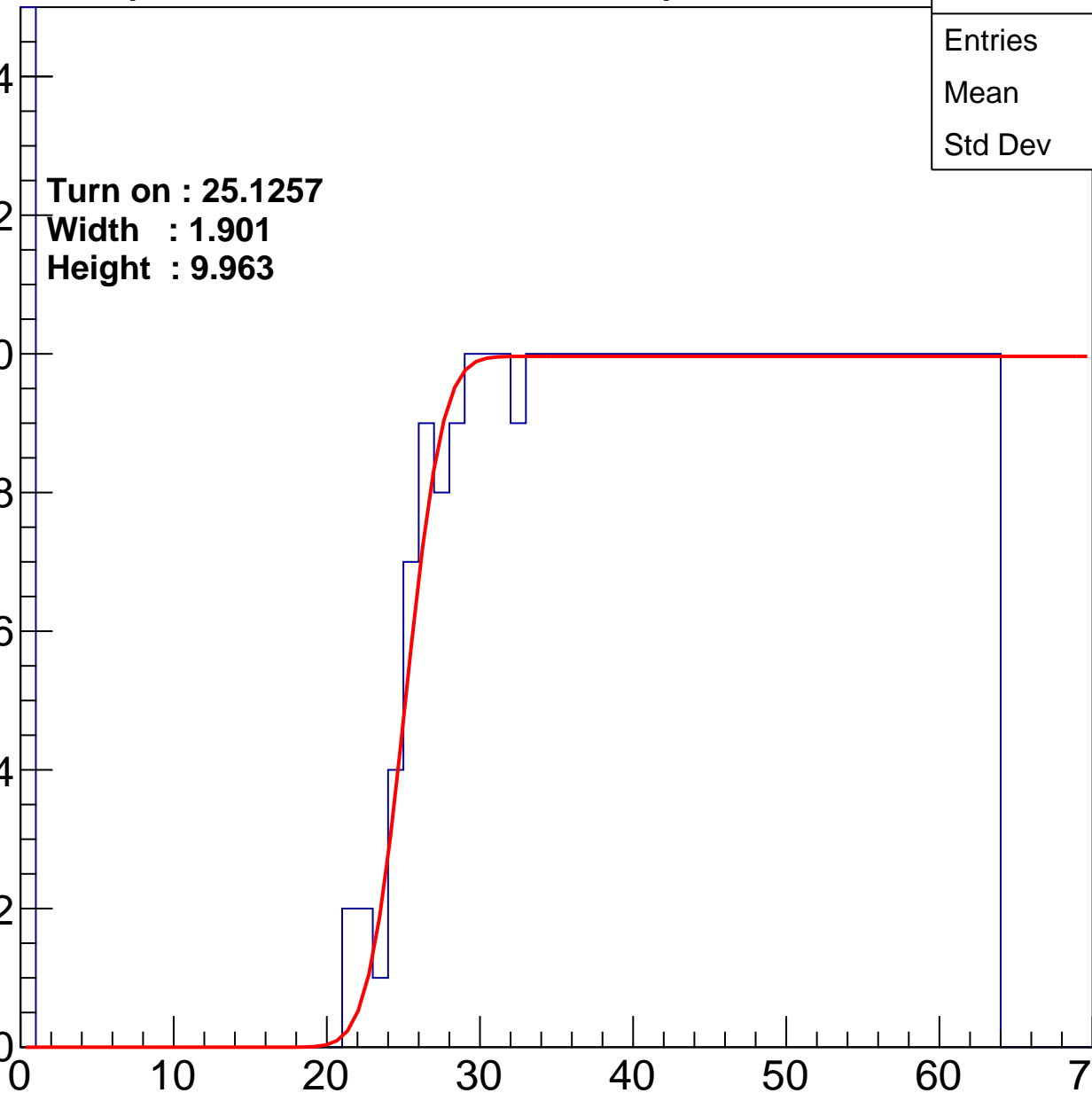
Width : 1.901

Height : 9.963

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch71

calib_packv5_041523_1651.root, FC#0, port C2

Entries	415
Mean	40.44
Std Dev	16.64

Turn on : 26.7403

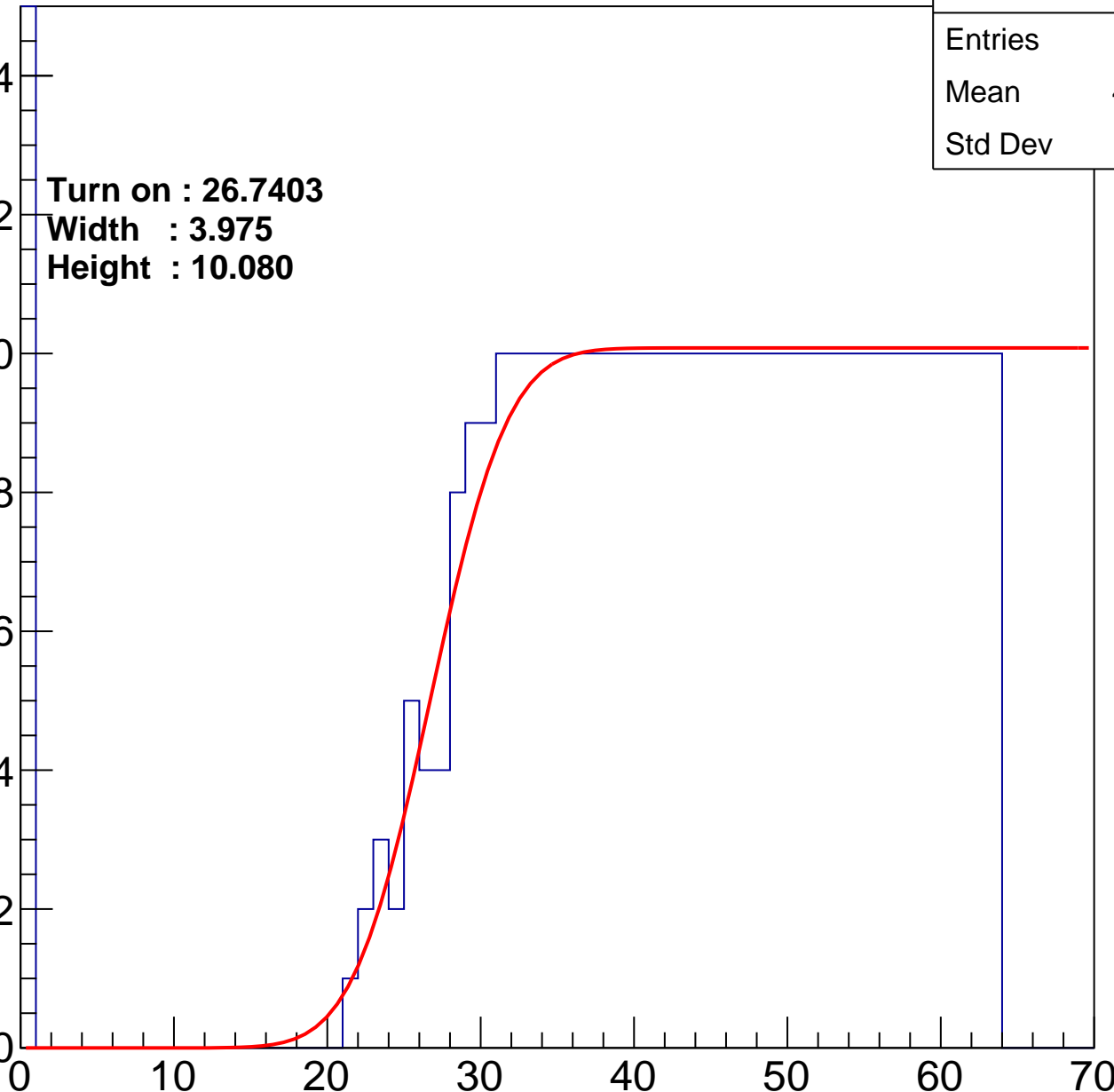
Width : 3.975

Height : 10.080

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch72

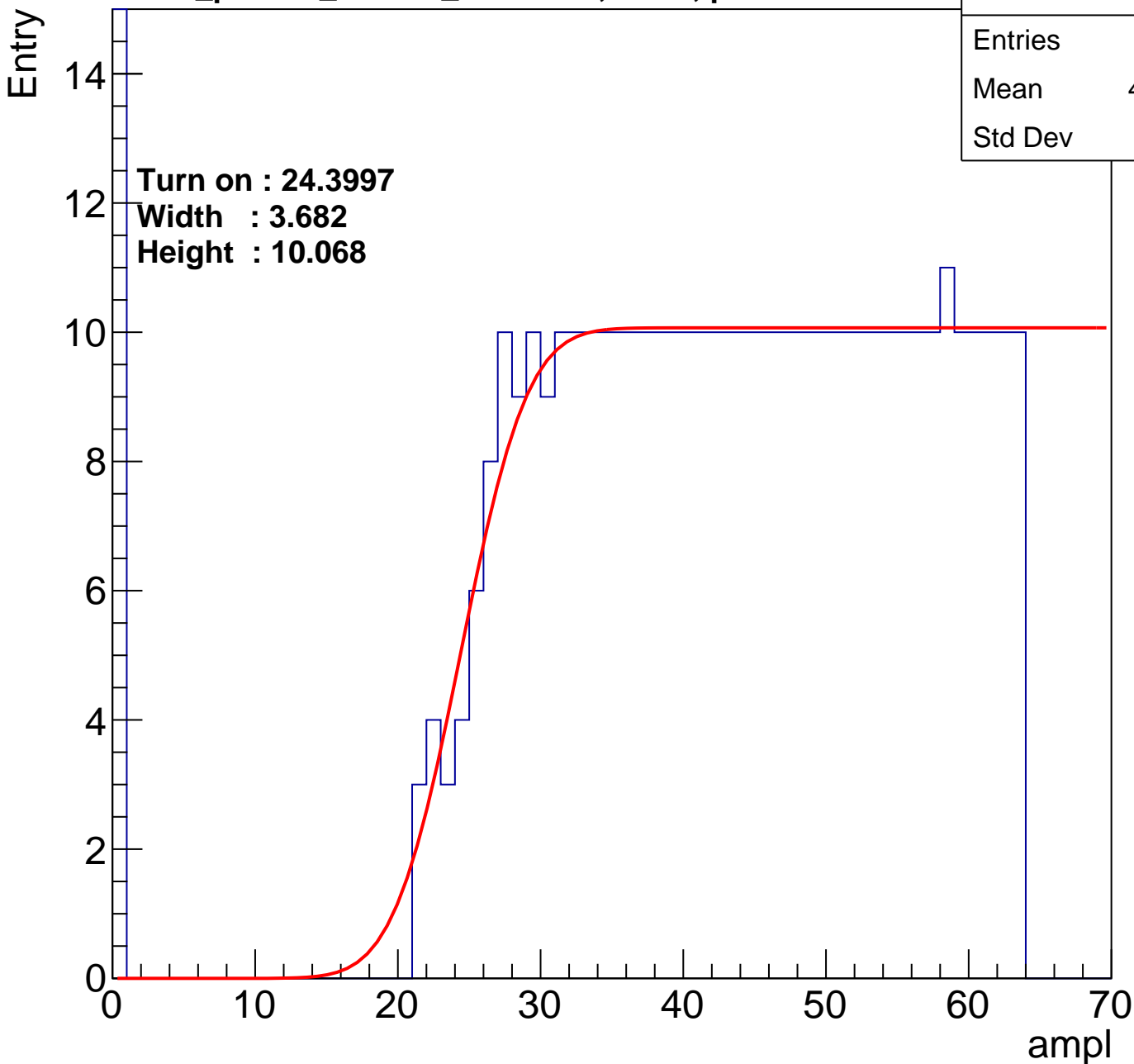
calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	40.38
Std Dev	16

Turn on : 24.3997

Width : 3.682

Height : 10.068



B1L103S, U19-ch73

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	38.9
Std Dev	18.2

Turn on : 27.1341

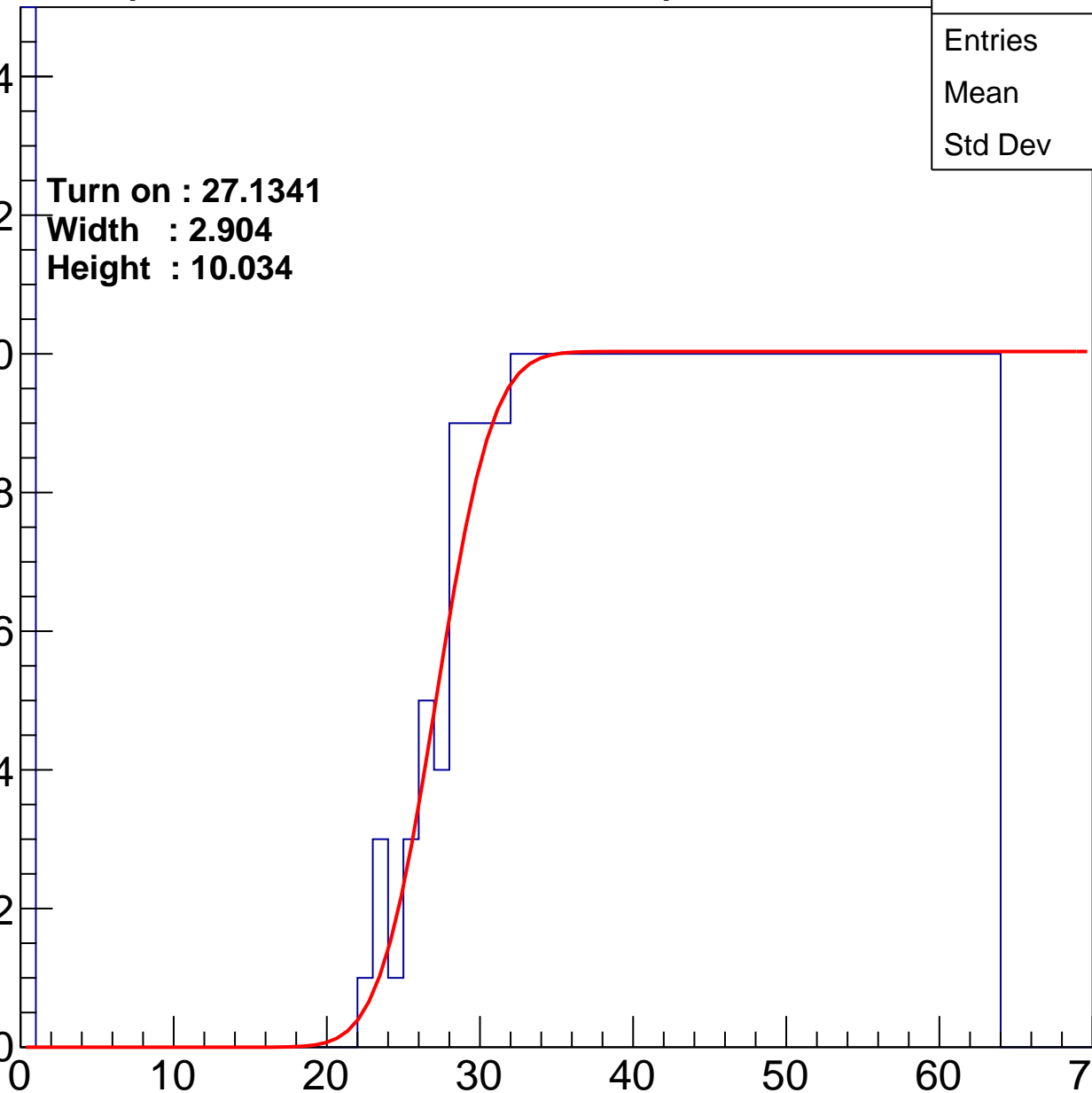
Width : 2.904

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch74

calib_packv5_041523_1651.root, FC#0, port C2

Entries	497
Mean	36.56
Std Dev	18.04

Turn on : 20.3180

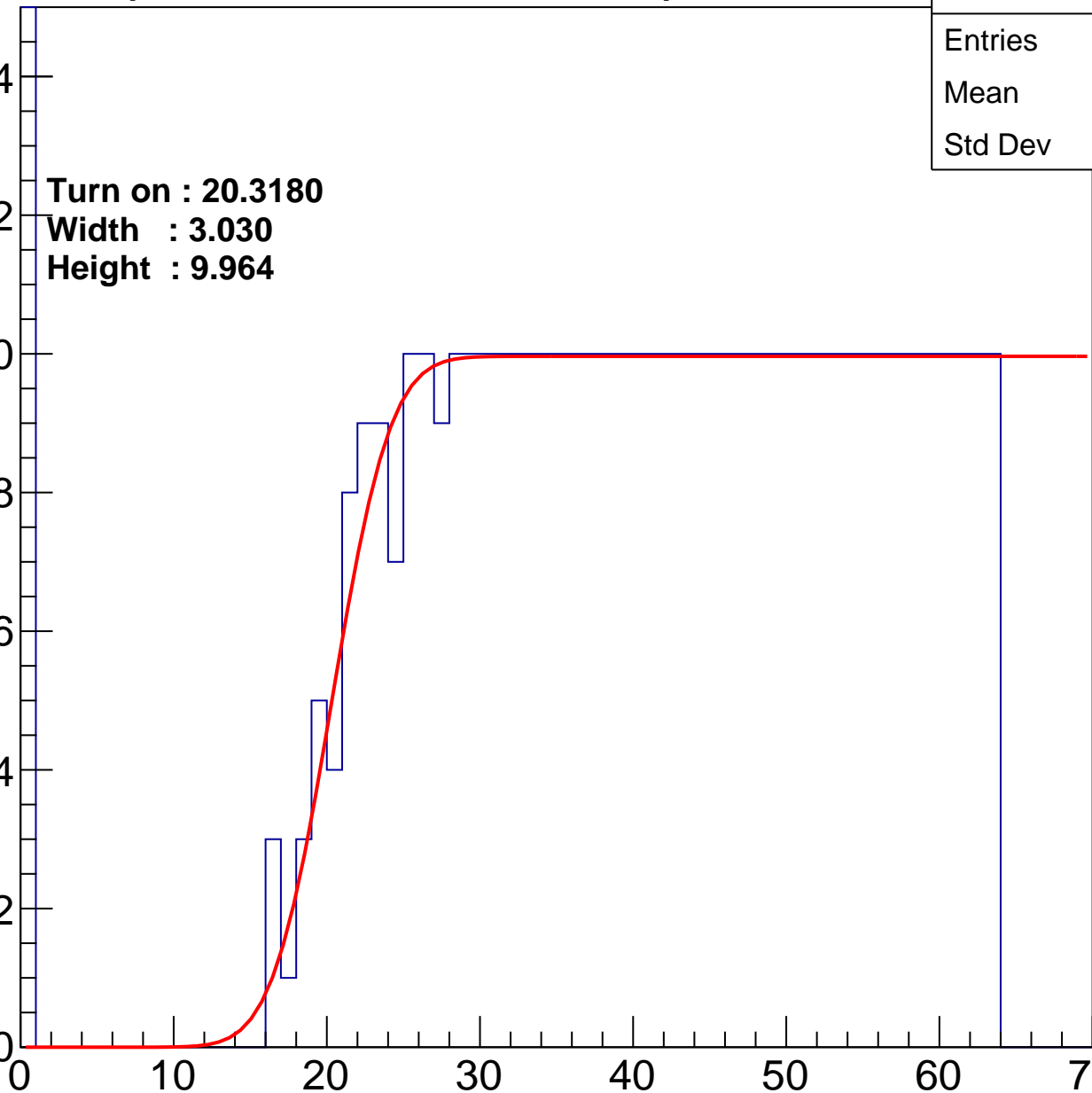
Width : 3.030

Height : 9.964

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch75

calib_packv5_041523_1651.root, FC#0, port C2

Entries	446
Mean	39.02
Std Dev	17.12

Turn on : 24.4279

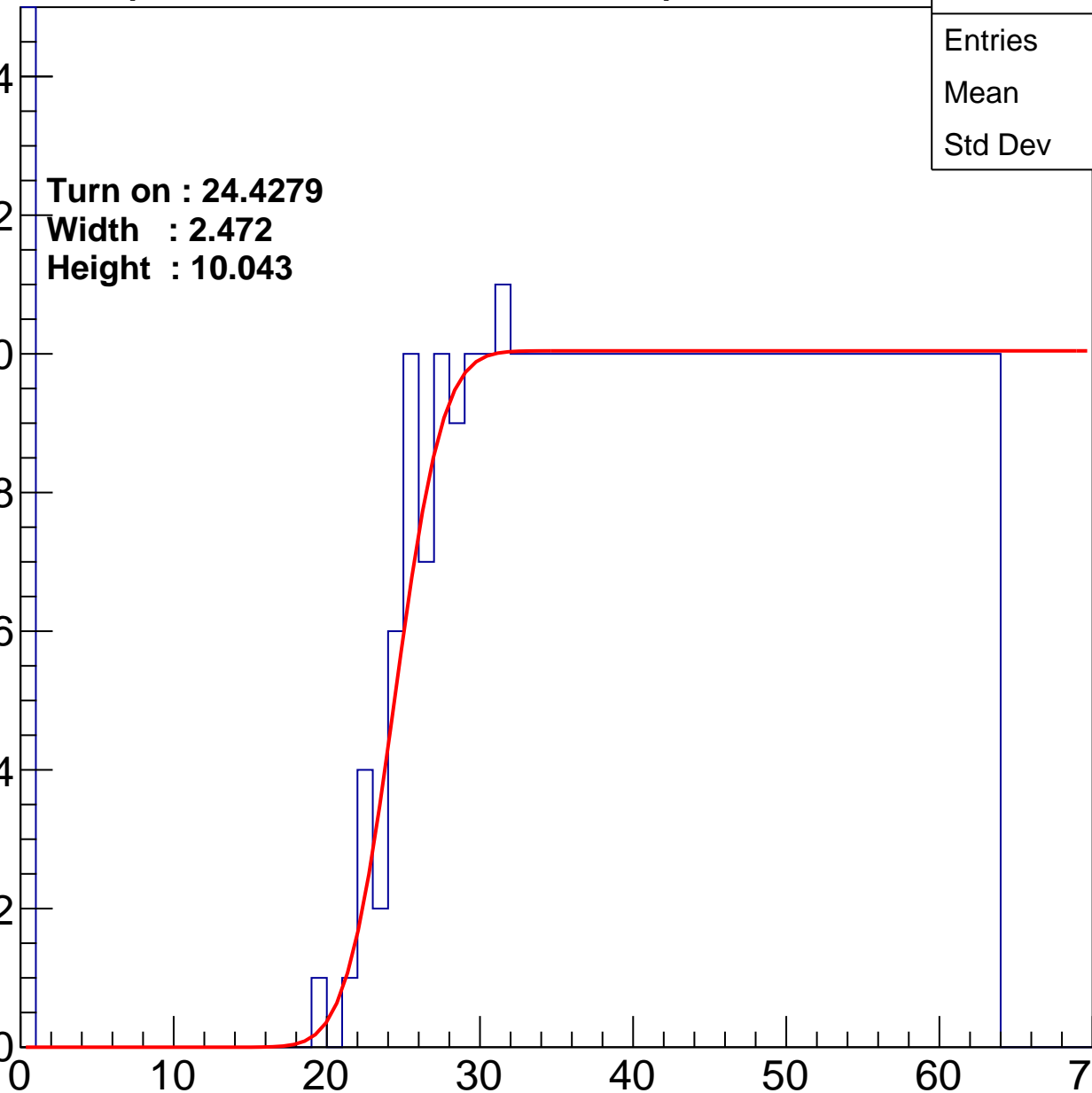
Width : 2.472

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch76

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	39.32
Std Dev	16.84

Turn on : 24.0803

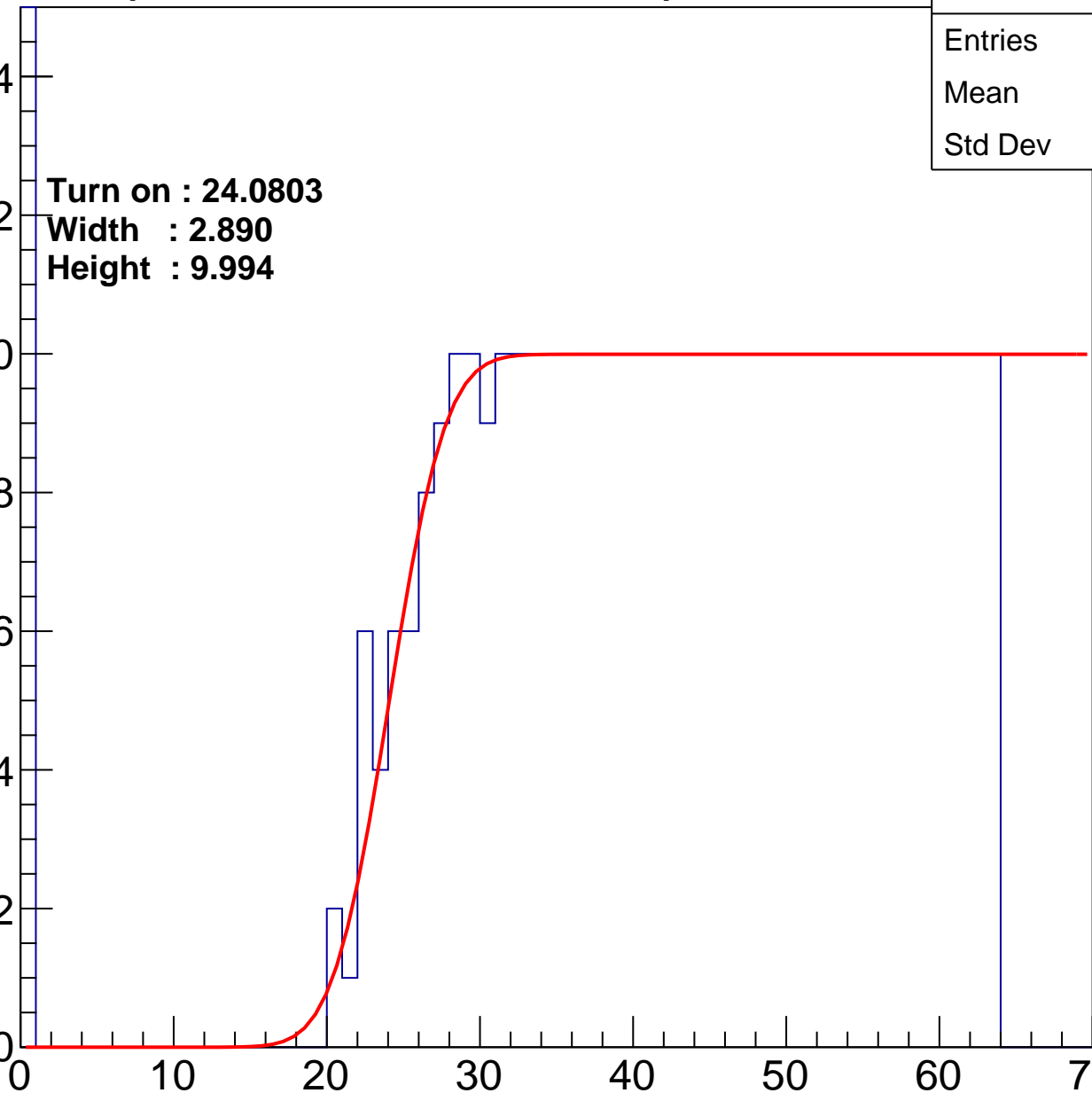
Width : 2.890

Height : 9.994

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch77

calib_packv5_041523_1651.root, FC#0, port C2

Entries	412
Mean	41.16
Std Dev	15.64

Turn on : 26.1636

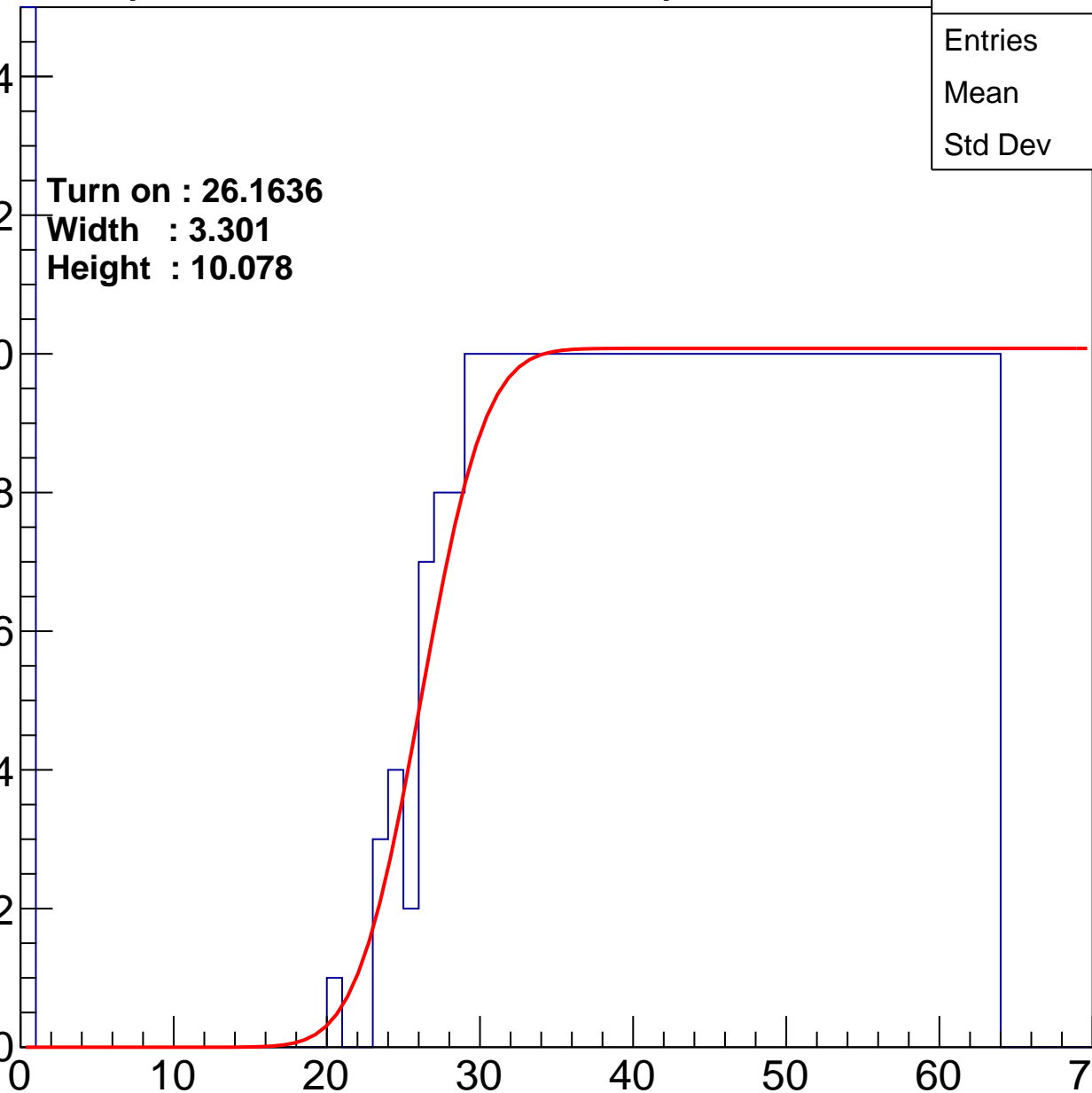
Width : 3.301

Height : 10.078

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch78

calib_packv5_041523_1651.root, FC#0, port C2

Entries	448
Mean	37.9
Std Dev	18.64

Turn on : 25.6795

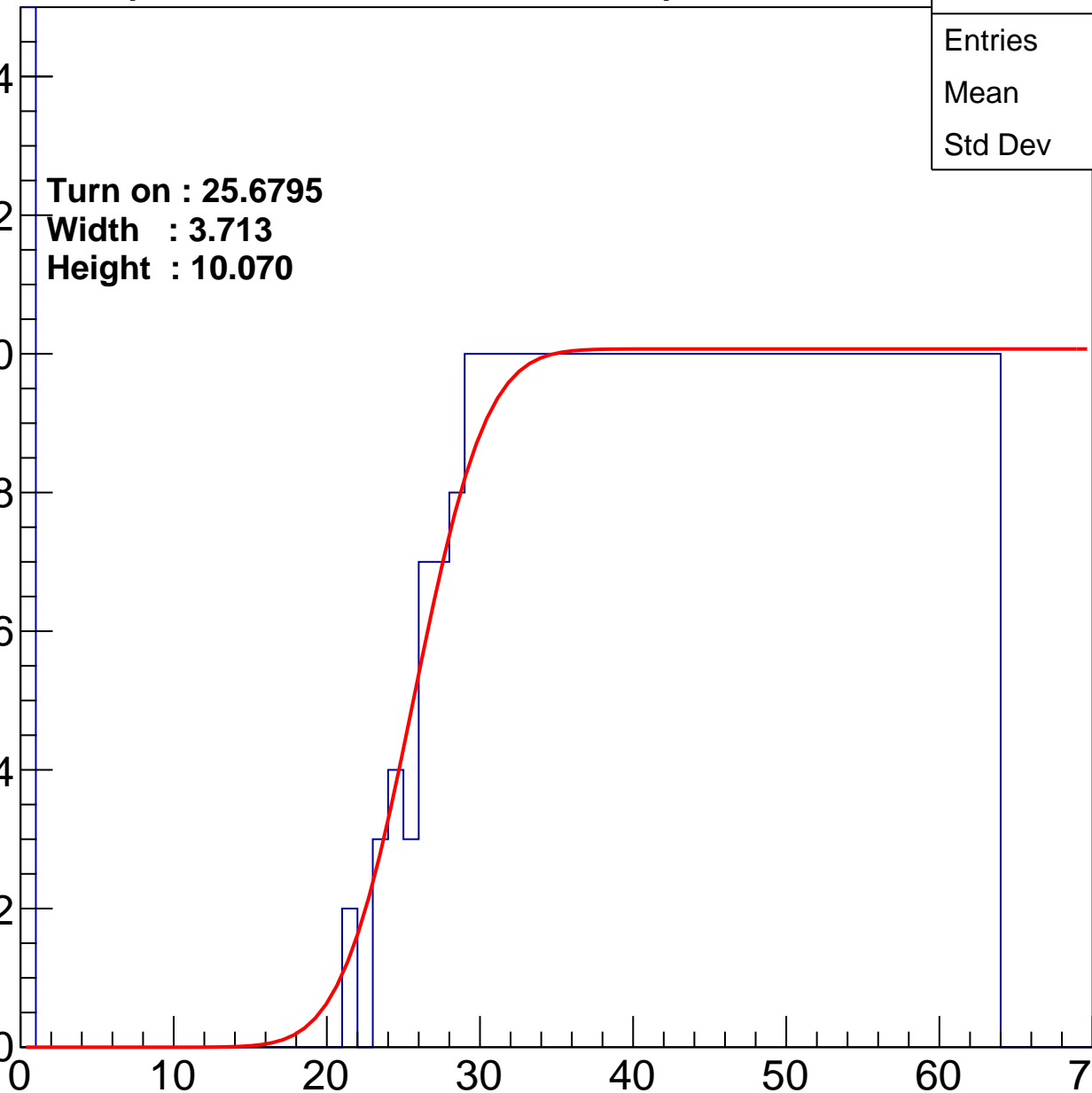
Width : 3.713

Height : 10.070

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch79

calib_packv5_041523_1651.root, FC#0, port C2

Entries	449
Mean	38.43
Std Dev	17.91

Turn on : 24.9020

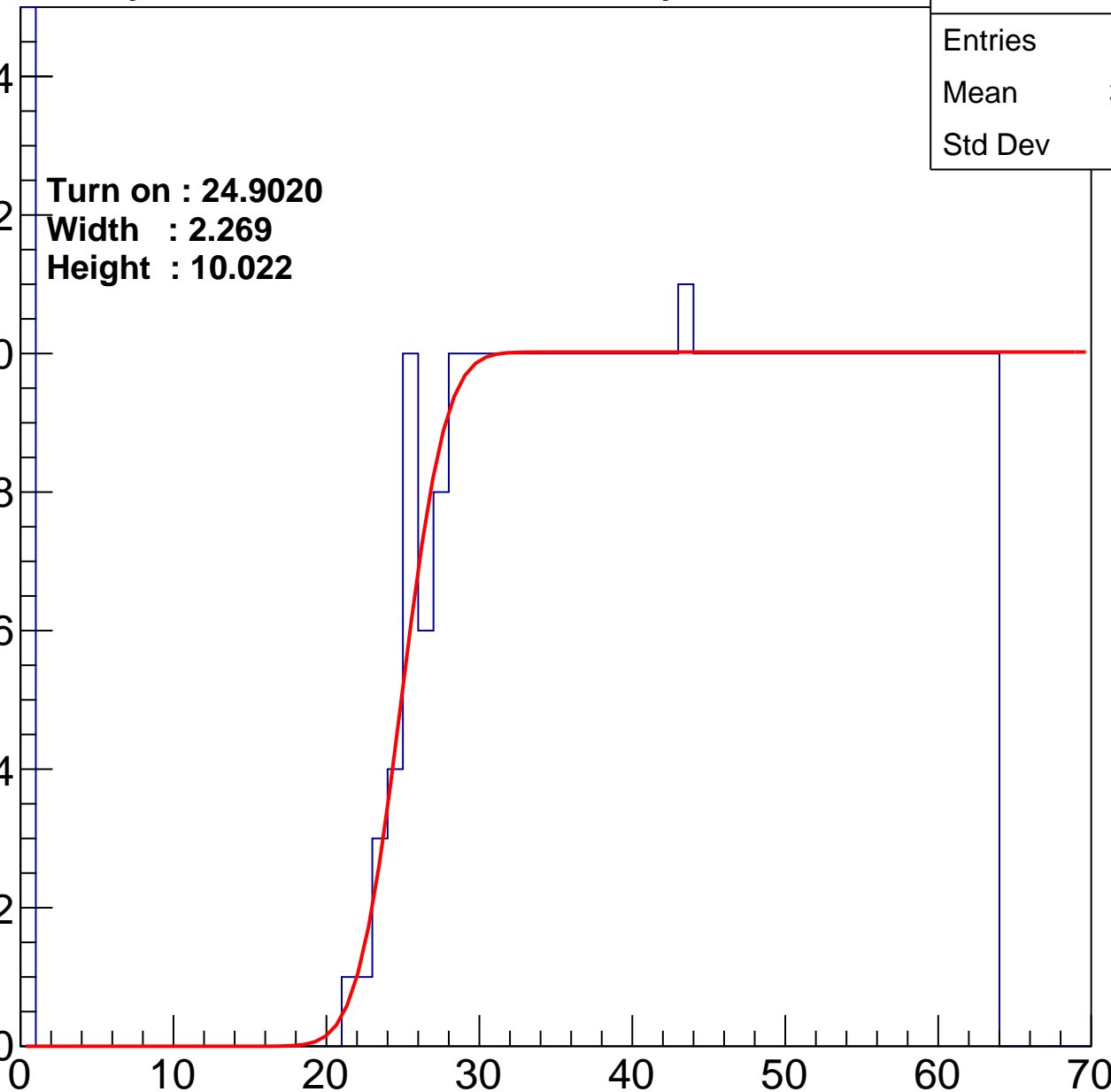
Width : 2.269

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch80

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	38.73
Std Dev	17.75

Turn on : 25.4841

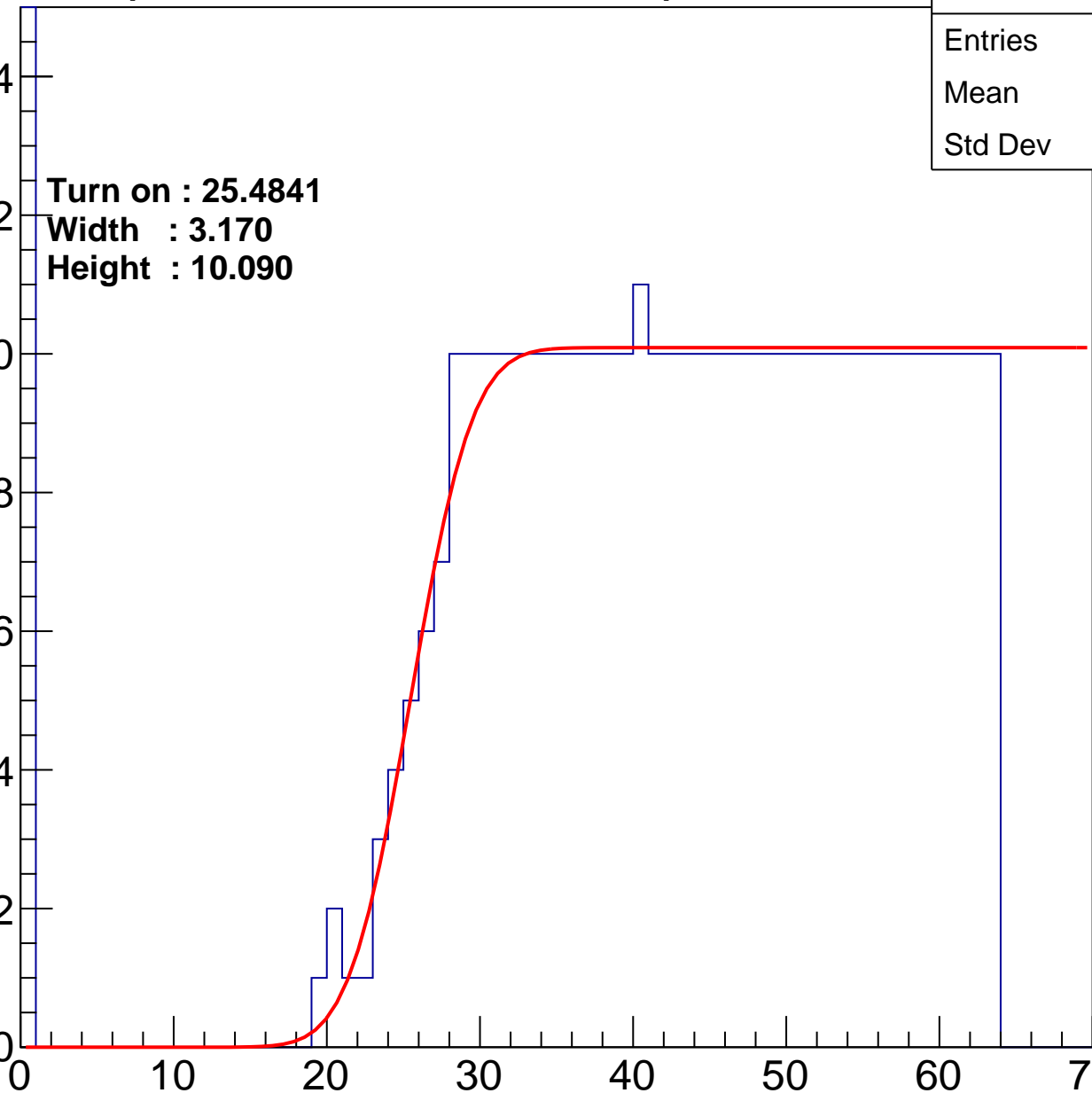
Width : 3.170

Height : 10.090

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch81

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	39.32
Std Dev	17.41

Turn on : 25.2506

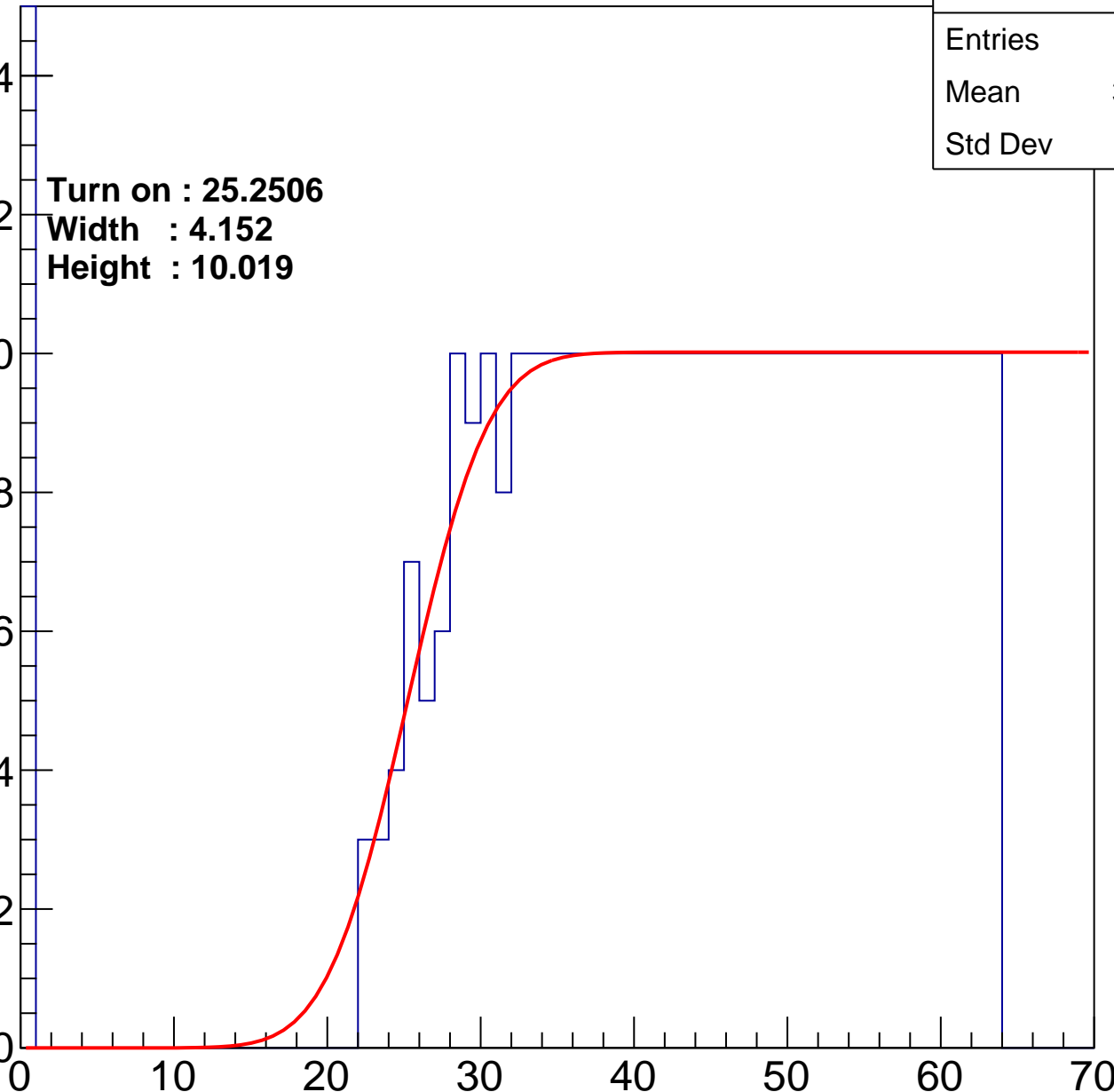
Width : 4.152

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch82

calib_packv5_041523_1651.root, FC#0, port C2

Entries	494
Mean	34.66
Std Dev	20.41

Turn on : 25.5305

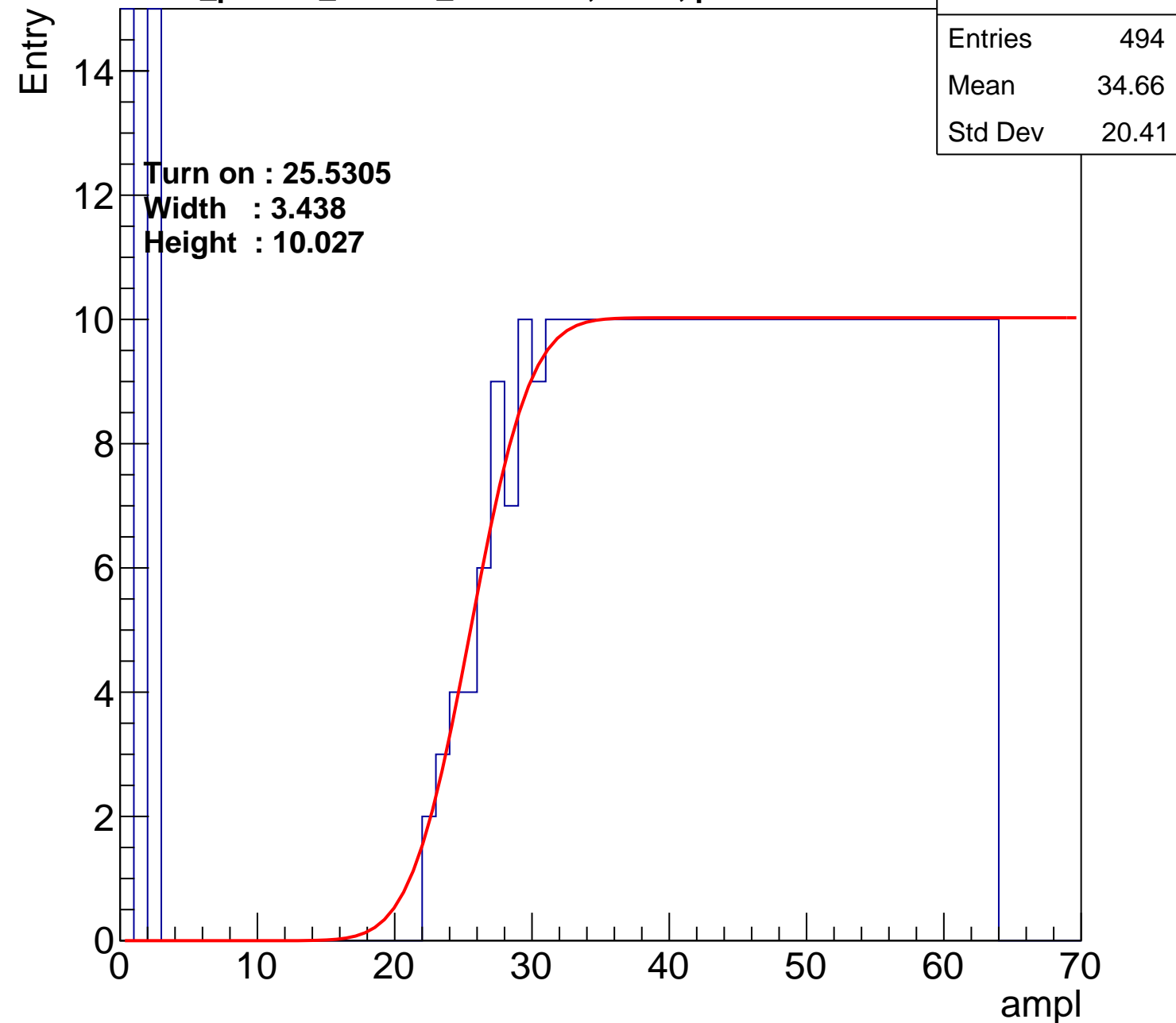
Width : 3.438

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch83

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	39.29
Std Dev	17.51

Turn on : 25.5845

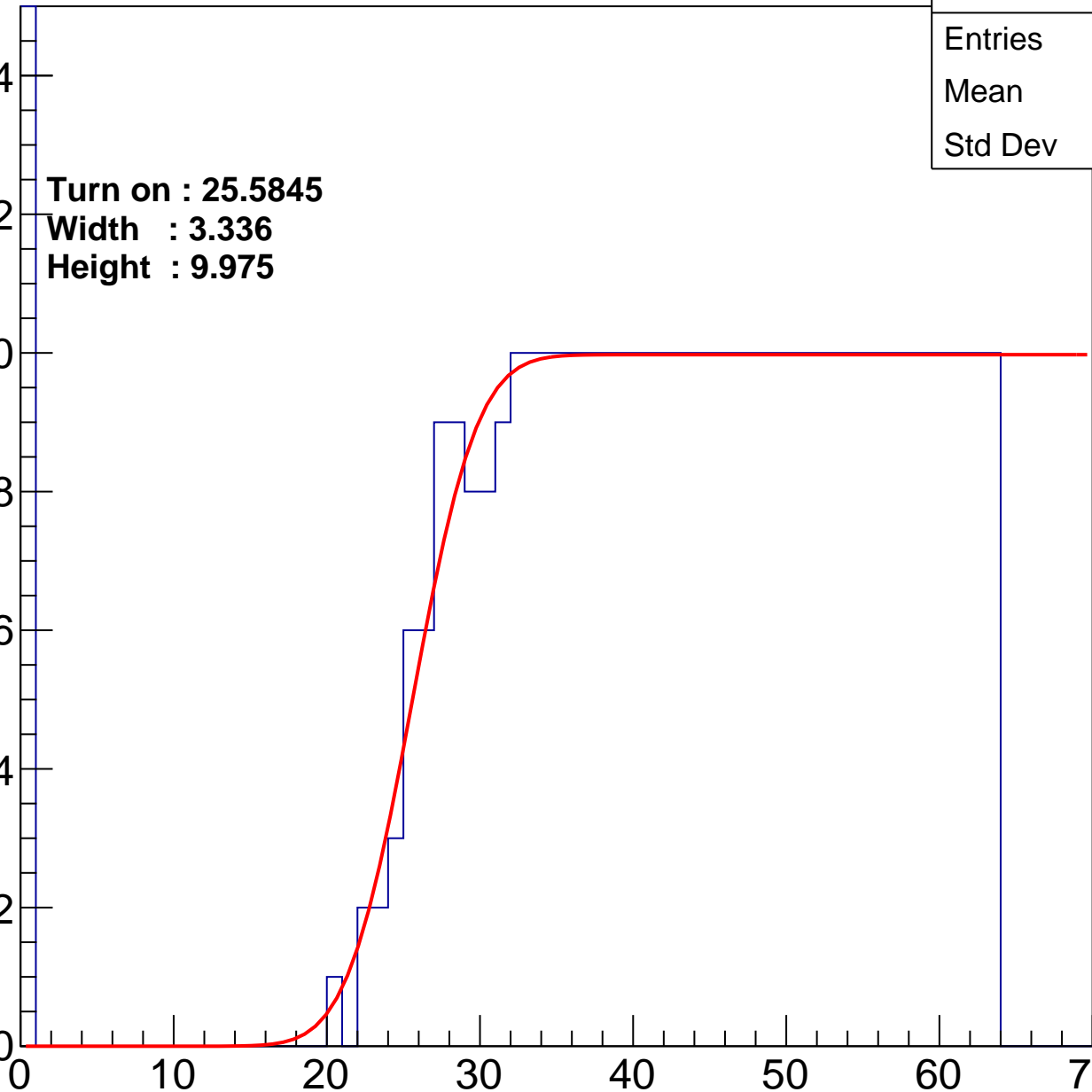
Width : 3.336

Height : 9.975

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch84

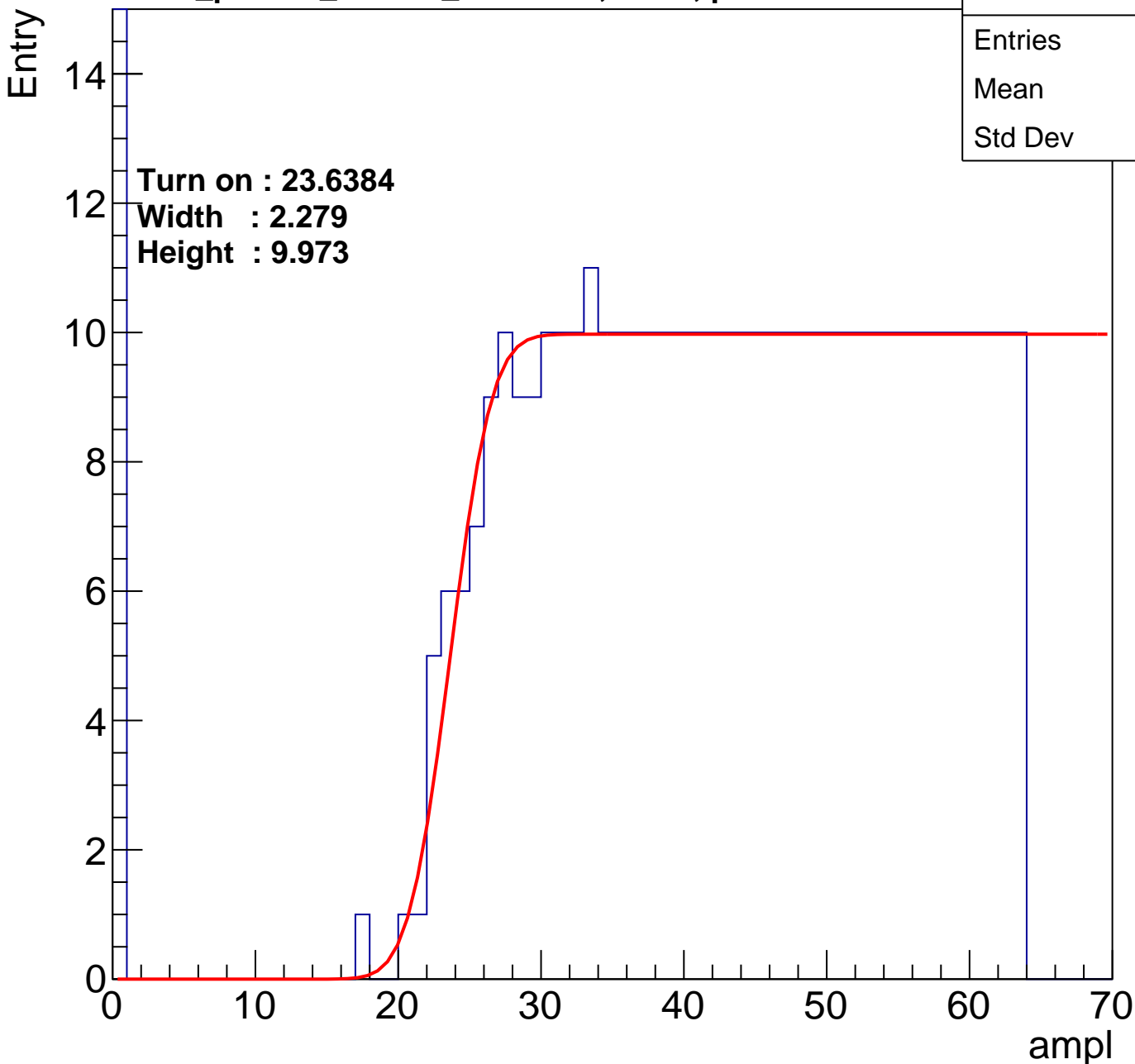
calib_packv5_041523_1651.root, FC#0, port C2

Entries	470
Mean	37.2
Std Dev	18.51

Turn on : 23.6384

Width : 2.279

Height : 9.973



B1L103S, U19-ch85

calib_packv5_041523_1651.root, FC#0, port C2

Entries	457
Mean	37.99
Std Dev	18.05

Turn on : 23.6727

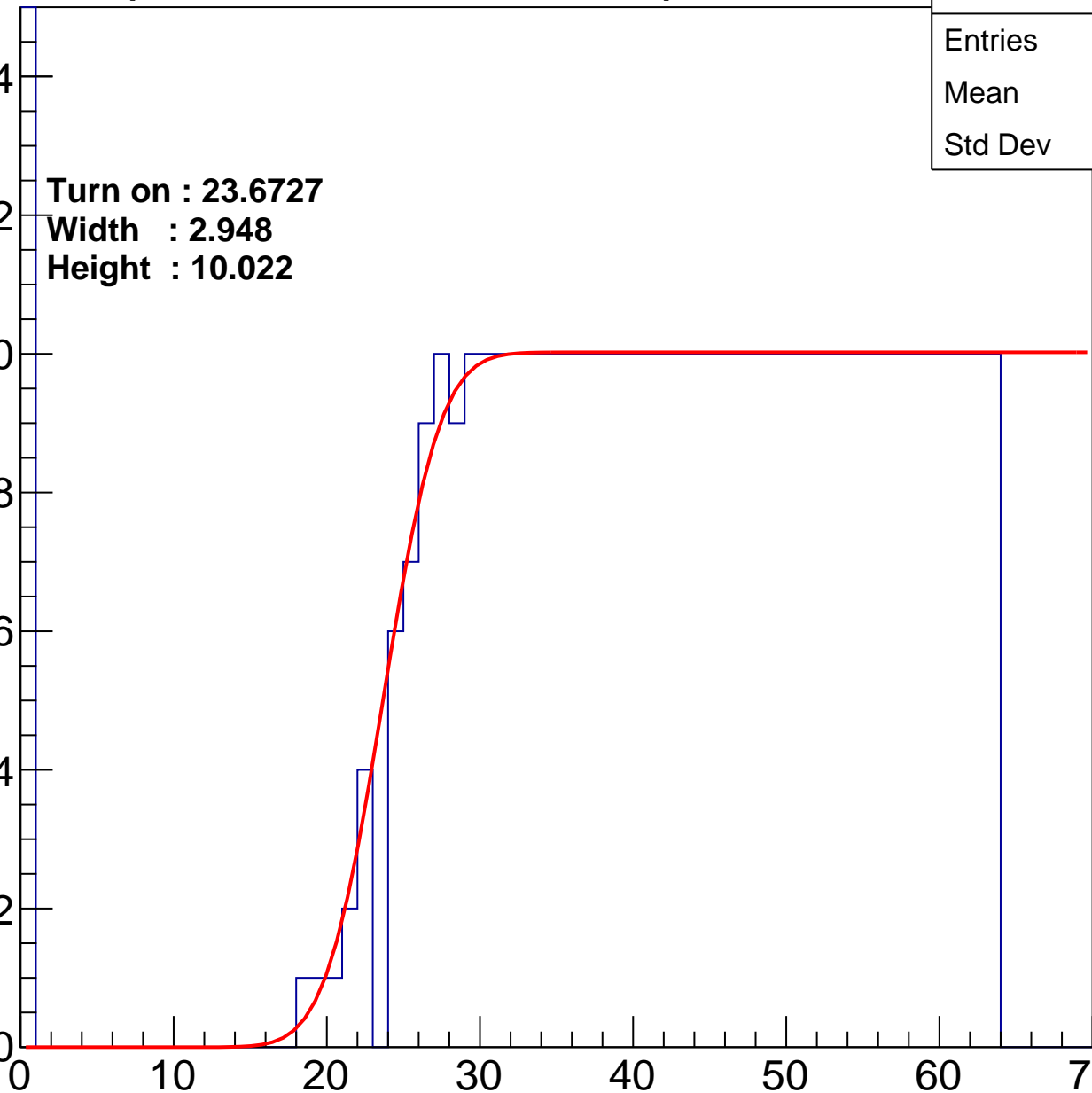
Width : 2.948

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch86

calib_packv5_041523_1651.root, FC#0, port C2

Entries	468
Mean	37.43
Std Dev	18.27

Turn on : 23.7254

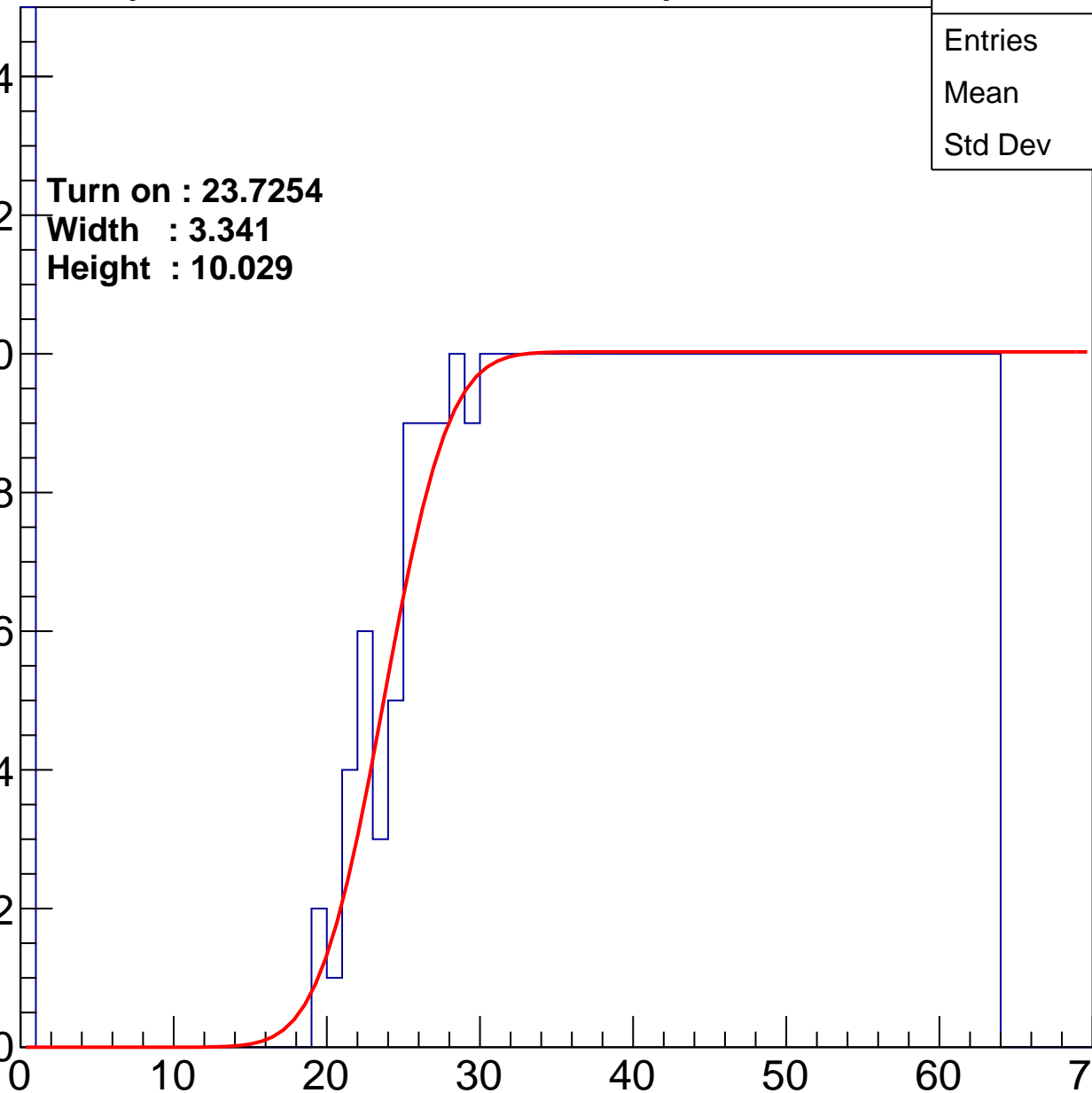
Width : 3.341

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch87

calib_packv5_041523_1651.root, FC#0, port C2

Entries	459
Mean	37.85
Std Dev	18.13

Turn on : 24.1876

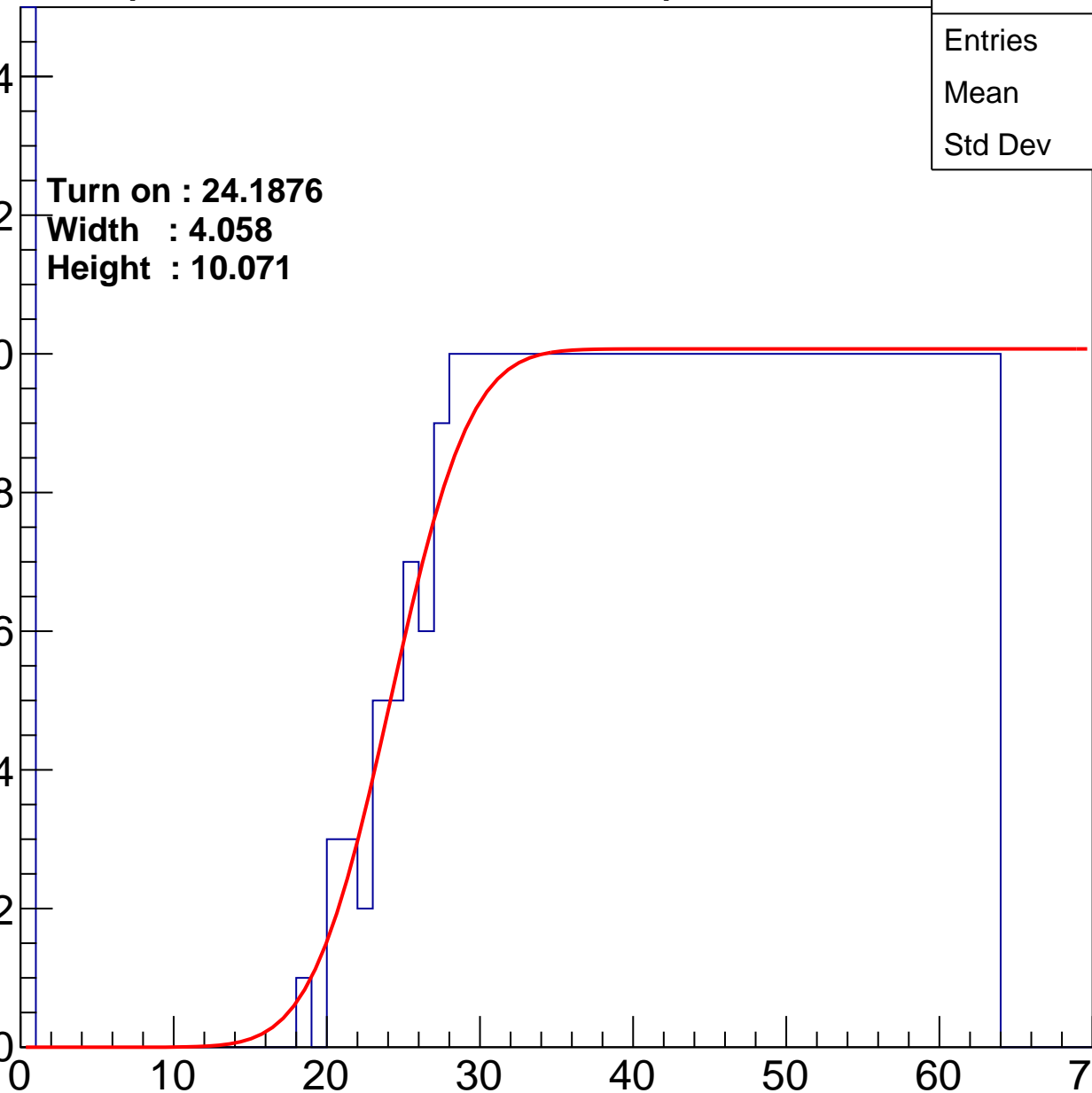
Width : 4.058

Height : 10.071

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch88

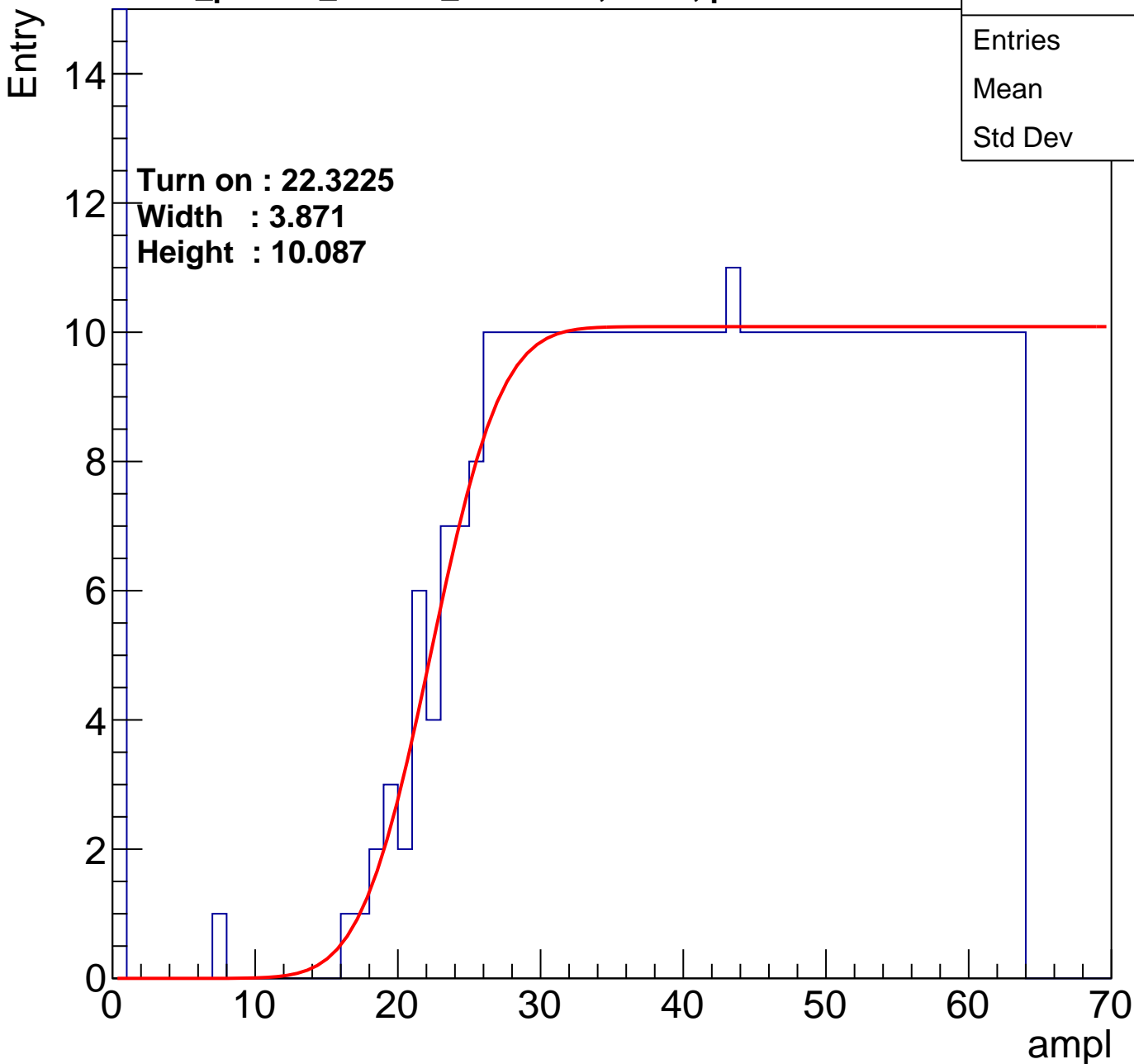
calib_packv5_041523_1651.root, FC#0, port C2

Entries	474
Mean	37.7
Std Dev	17.6

Turn on : 22.3225

Width : 3.871

Height : 10.087



B1L103S, U19-ch89

calib_packv5_041523_1651.root, FC#0, port C2

Entries	444
Mean	38.83
Std Dev	17.5

Turn on : 24.8620

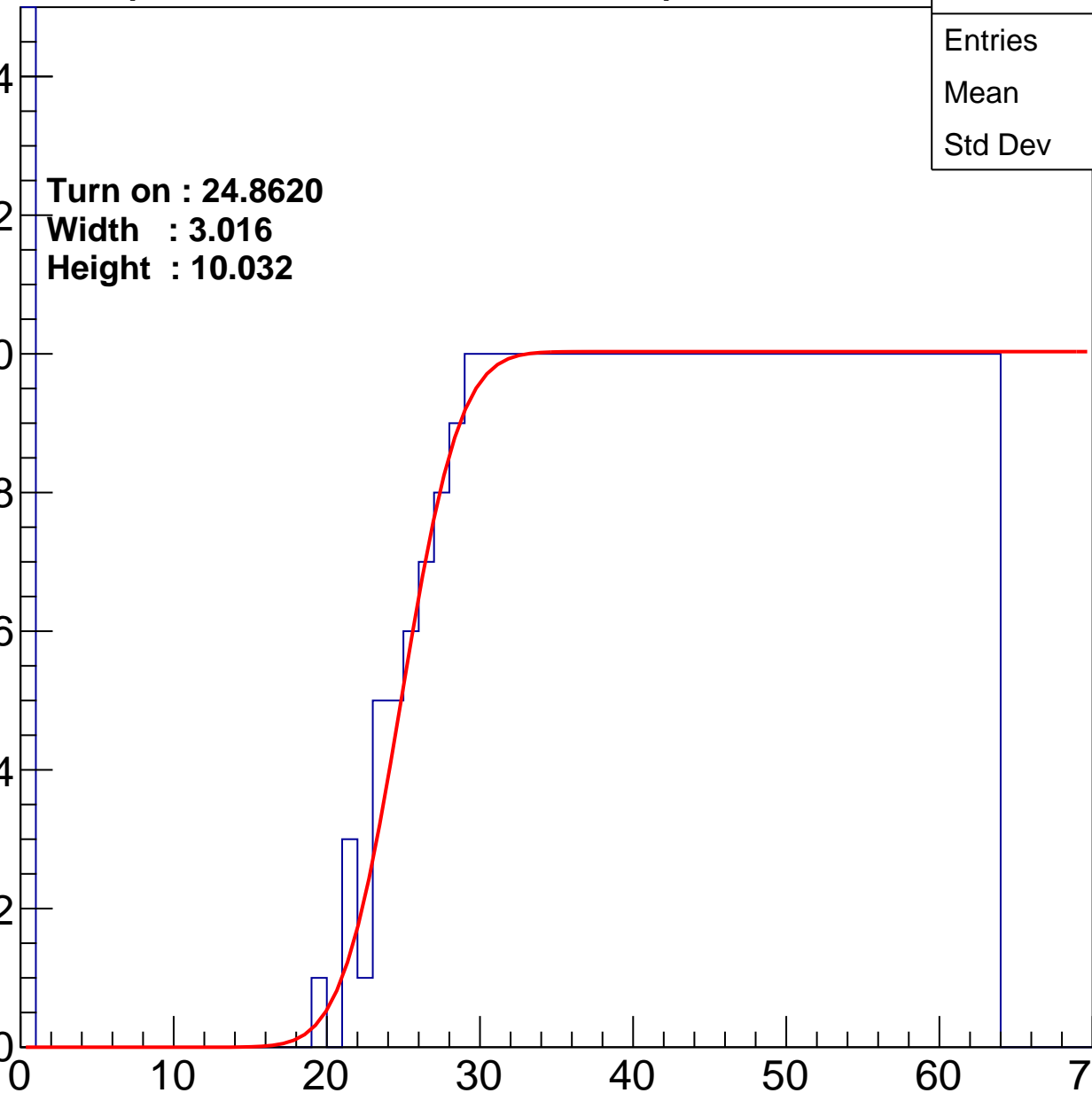
Width : 3.016

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch90

calib_packv5_041523_1651.root, FC#0, port C2

Entries	448
Mean	38.7
Std Dev	17.48

Turn on : 23.8240

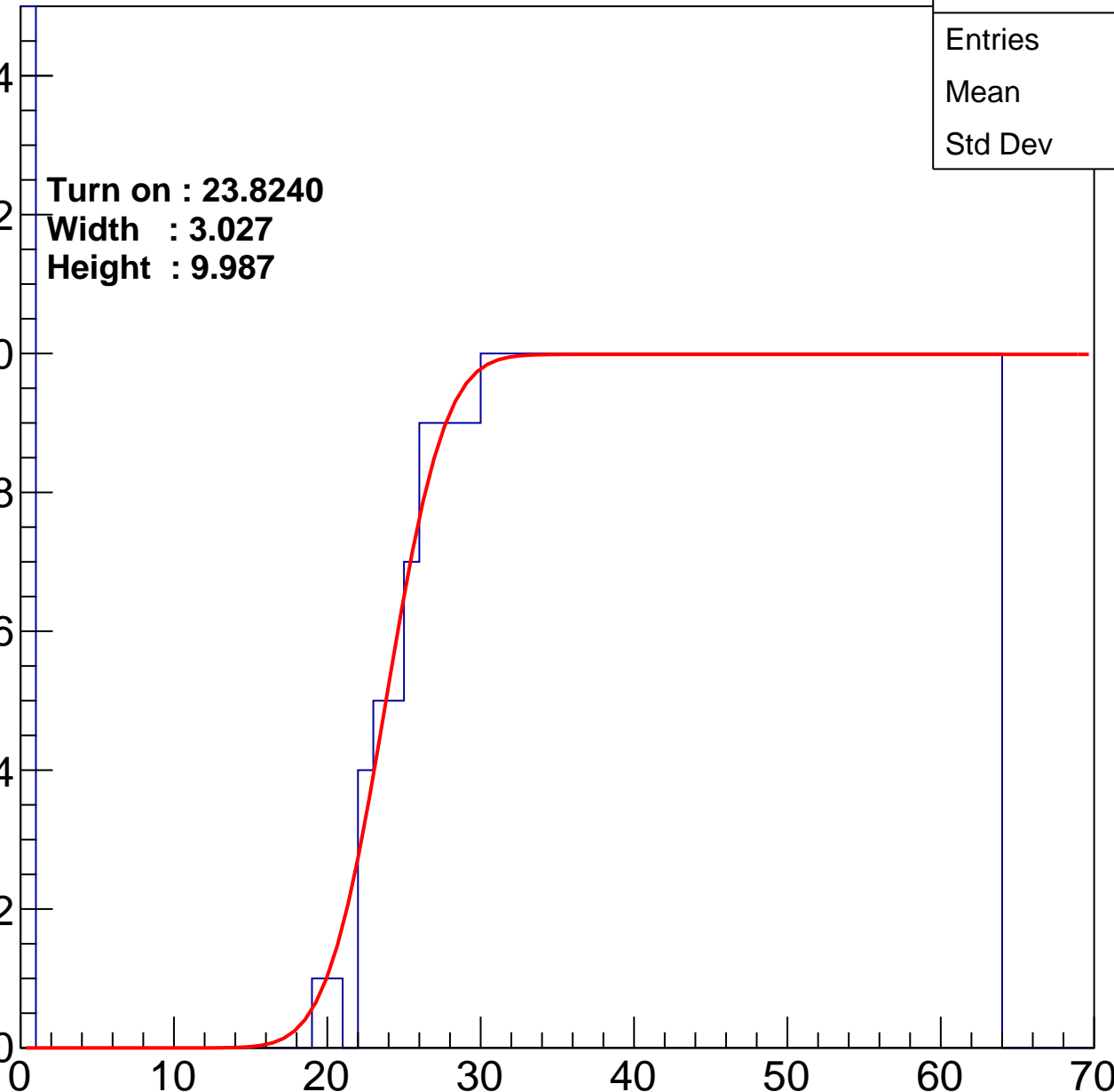
Width : 3.027

Height : 9.987

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch91

calib_packv5_041523_1651.root, FC#0, port C2

Entries	422
Mean	39.64
Std Dev	17.53

Turn on : 27.3043

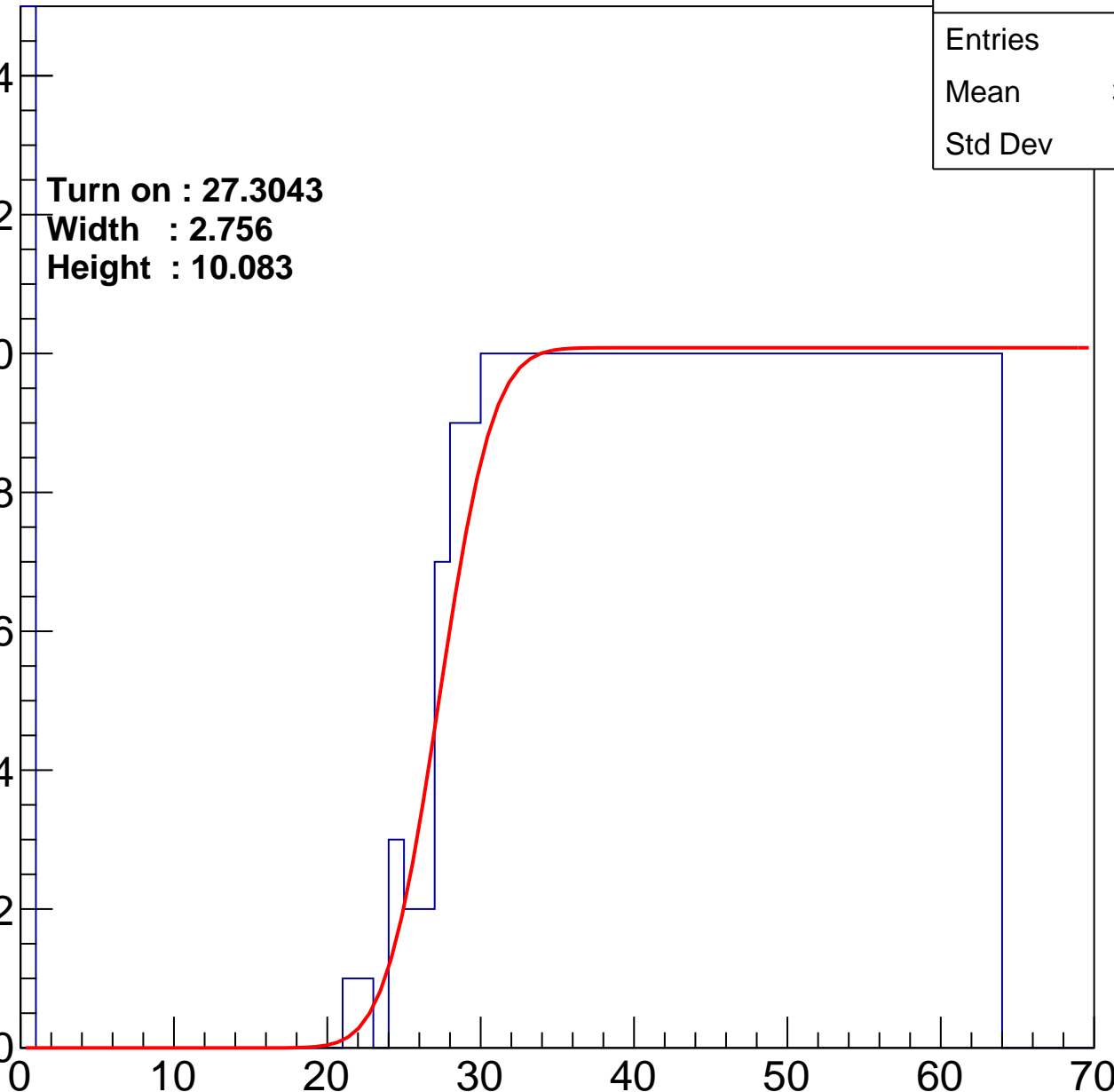
Width : 2.756

Height : 10.083

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch92

calib_packv5_041523_1651.root, FC#0, port C2

Entries	465
Mean	38.06
Std Dev	17.48

Turn on : 22.8159

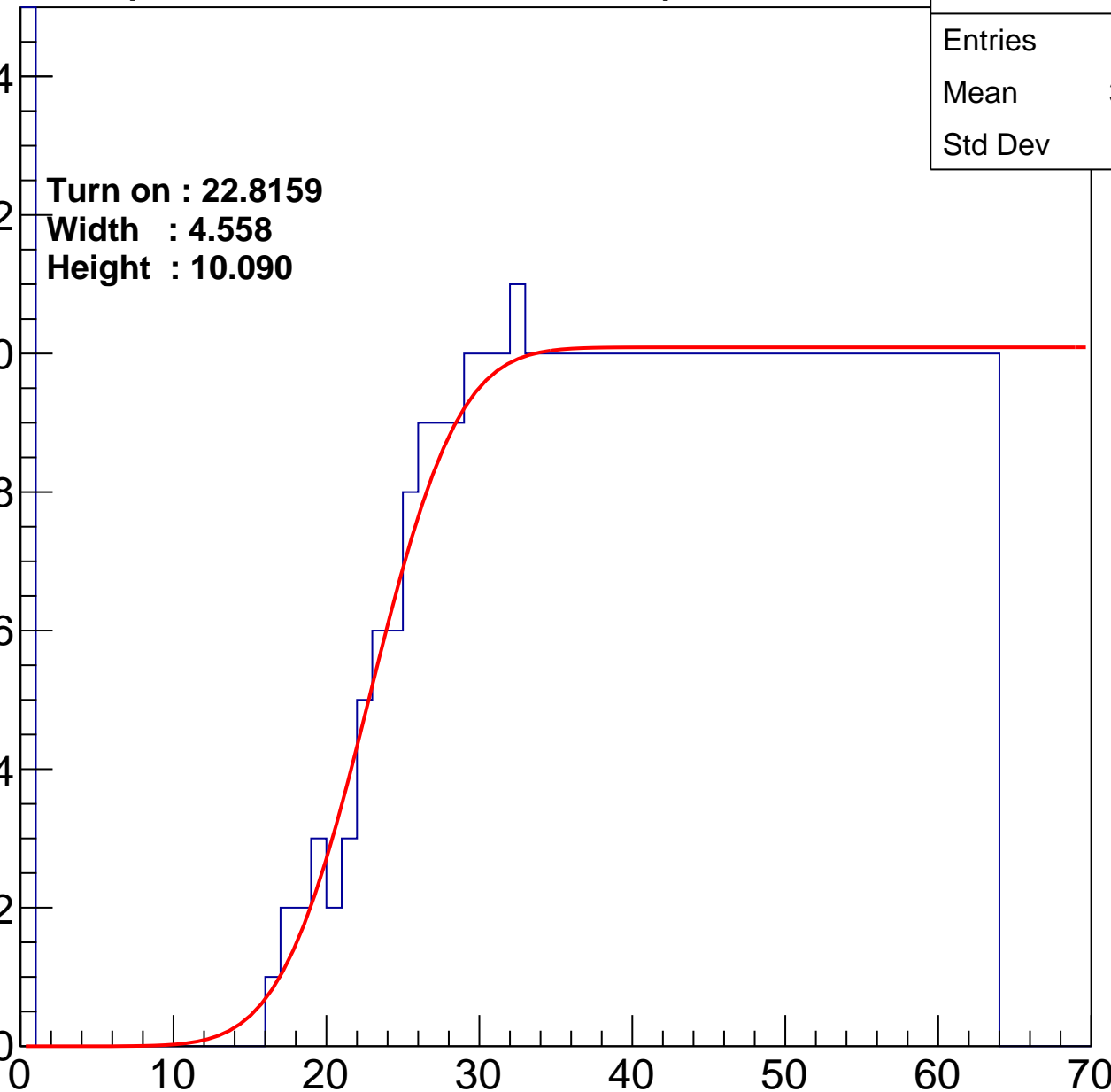
Width : 4.558

Height : 10.090

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch93

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.1
Std Dev	17.88

Turn on : 26.6027

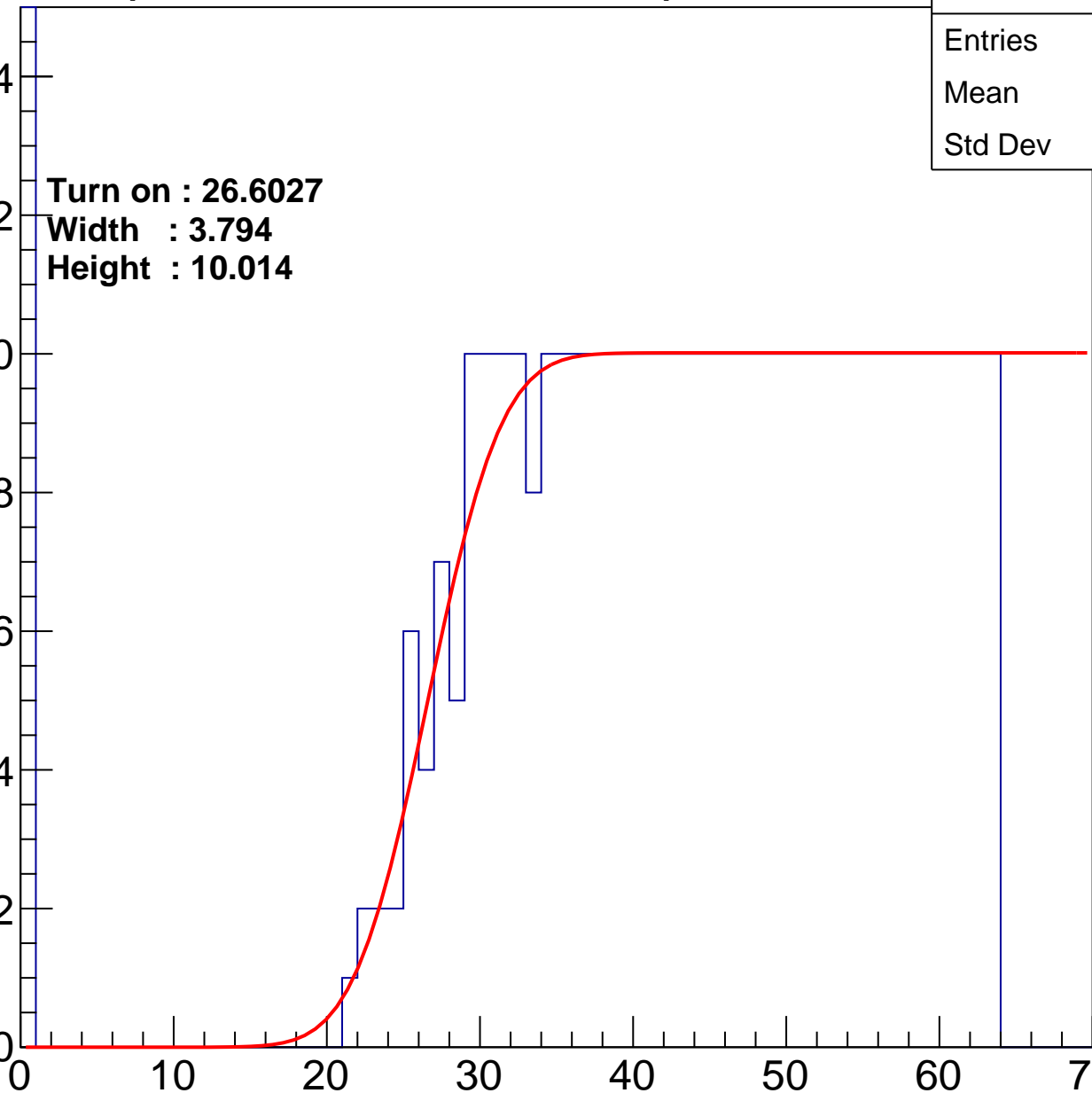
Width : 3.794

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch94

calib_packv5_041523_1651.root, FC#0, port C2

Entries	447
Mean	38.56
Std Dev	17.73

Turn on : 24.7438

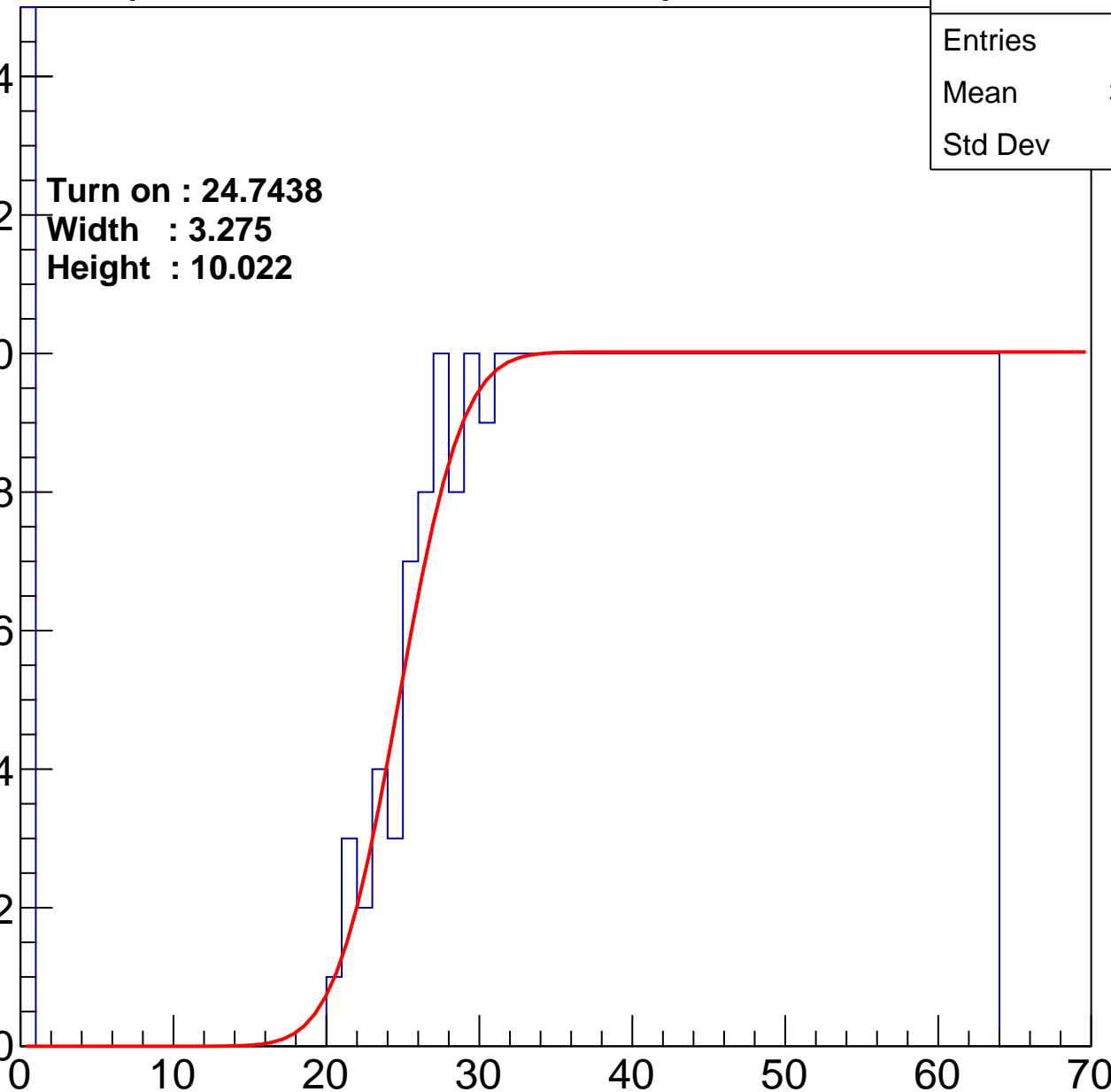
Width : 3.275

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch95

calib_packv5_041523_1651.root, FC#0, port C2

Entries	452
Mean	38.19
Std Dev	18.01

Turn on : 24.7184

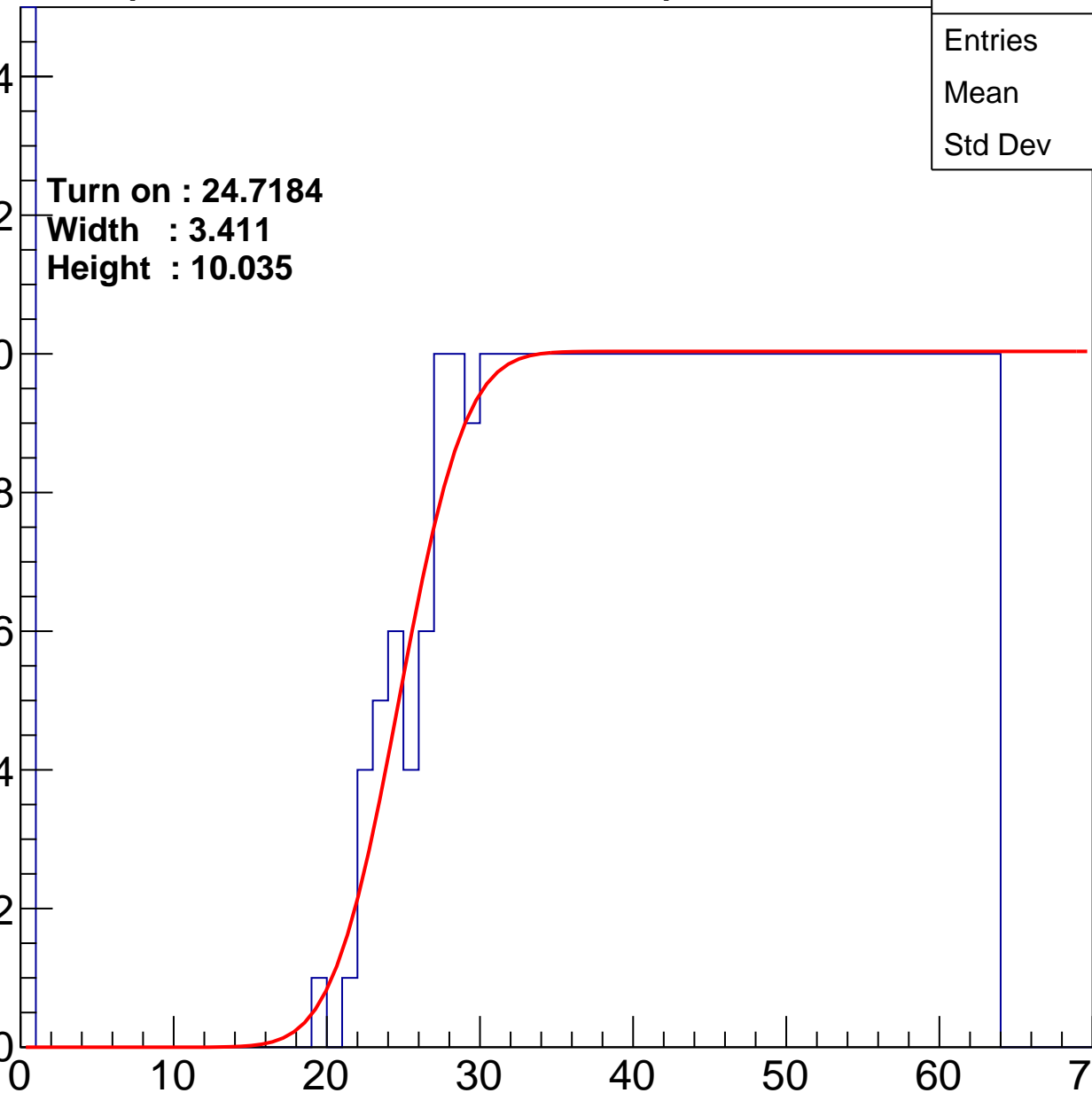
Width : 3.411

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch96

calib_packv5_041523_1651.root, FC#0, port C2

Entries	477
Mean	36.52
Std Dev	19.09

Turn on : 24.0970

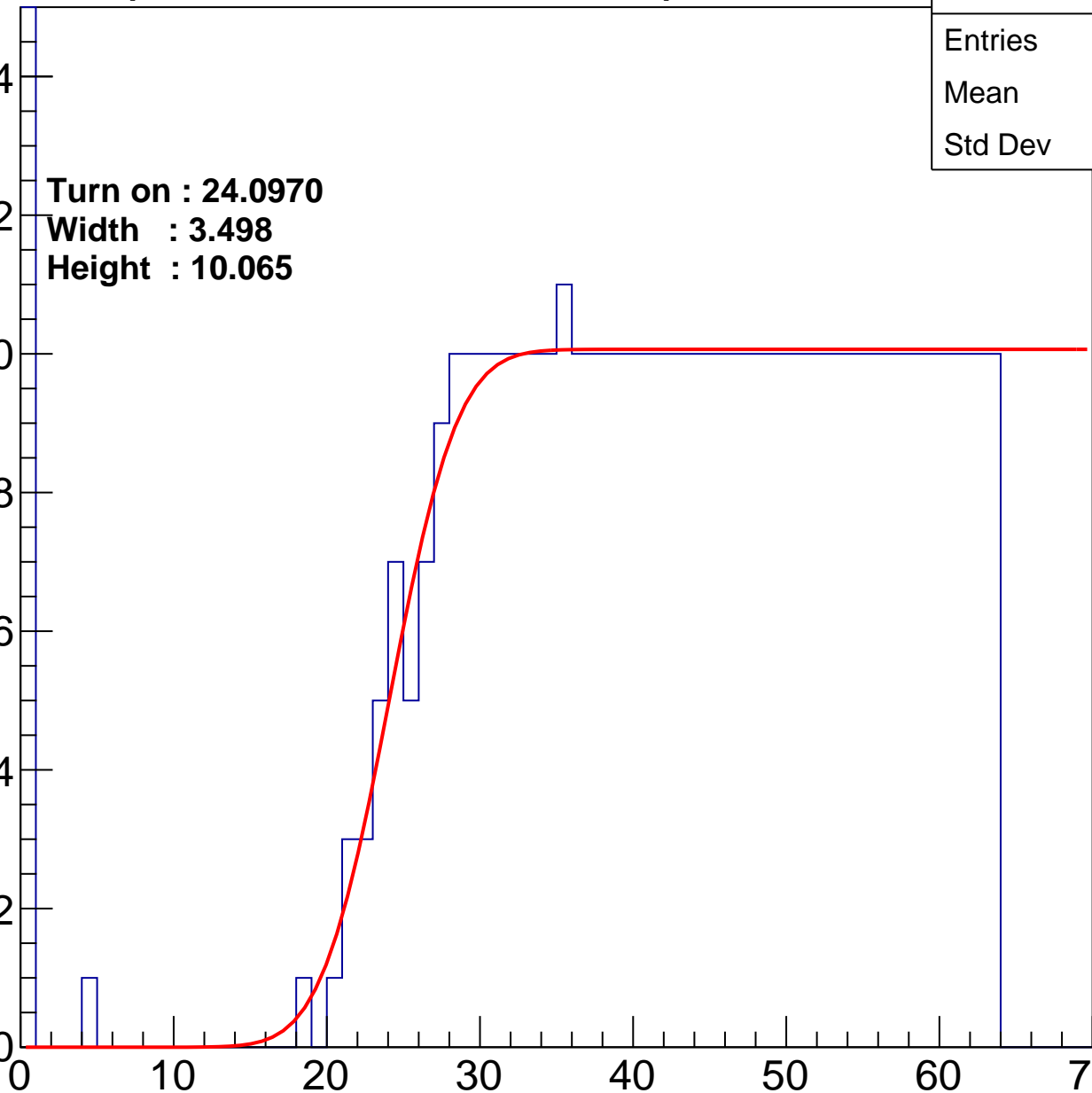
Width : 3.498

Height : 10.065

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch97

calib_packv5_041523_1651.root, FC#0, port C2

Entries	455
Mean	37.9
Std Dev	18.28

Turn on : 24.5431

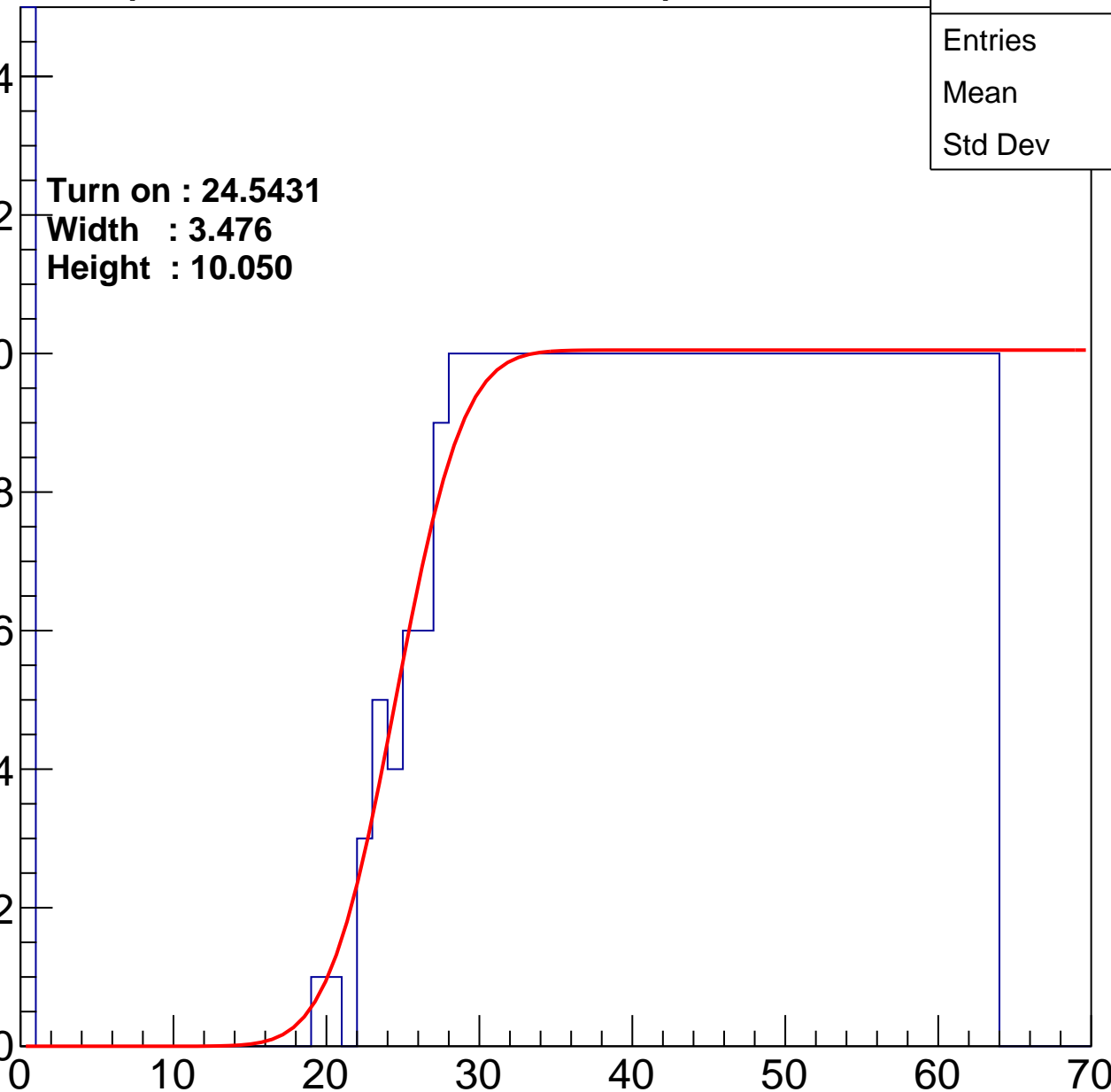
Width : 3.476

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch98

calib_packv5_041523_1651.root, FC#0, port C2

Entries	444
Mean	38.83
Std Dev	17.54

Turn on : 25.0185

Width : 1.386

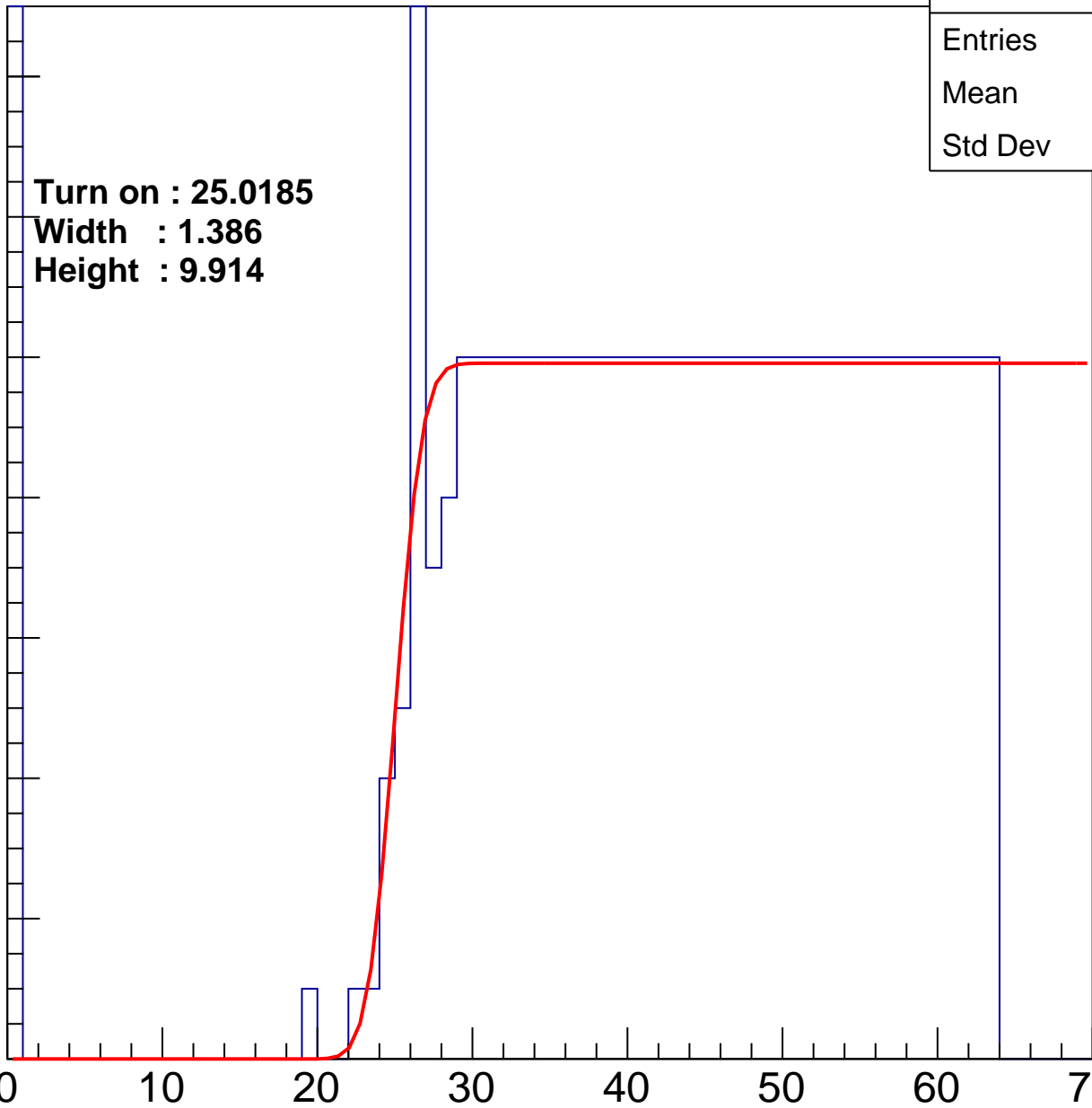
Height : 9.914

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U19-ch99

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	39.06
Std Dev	17.79

Turn on : 26.0807

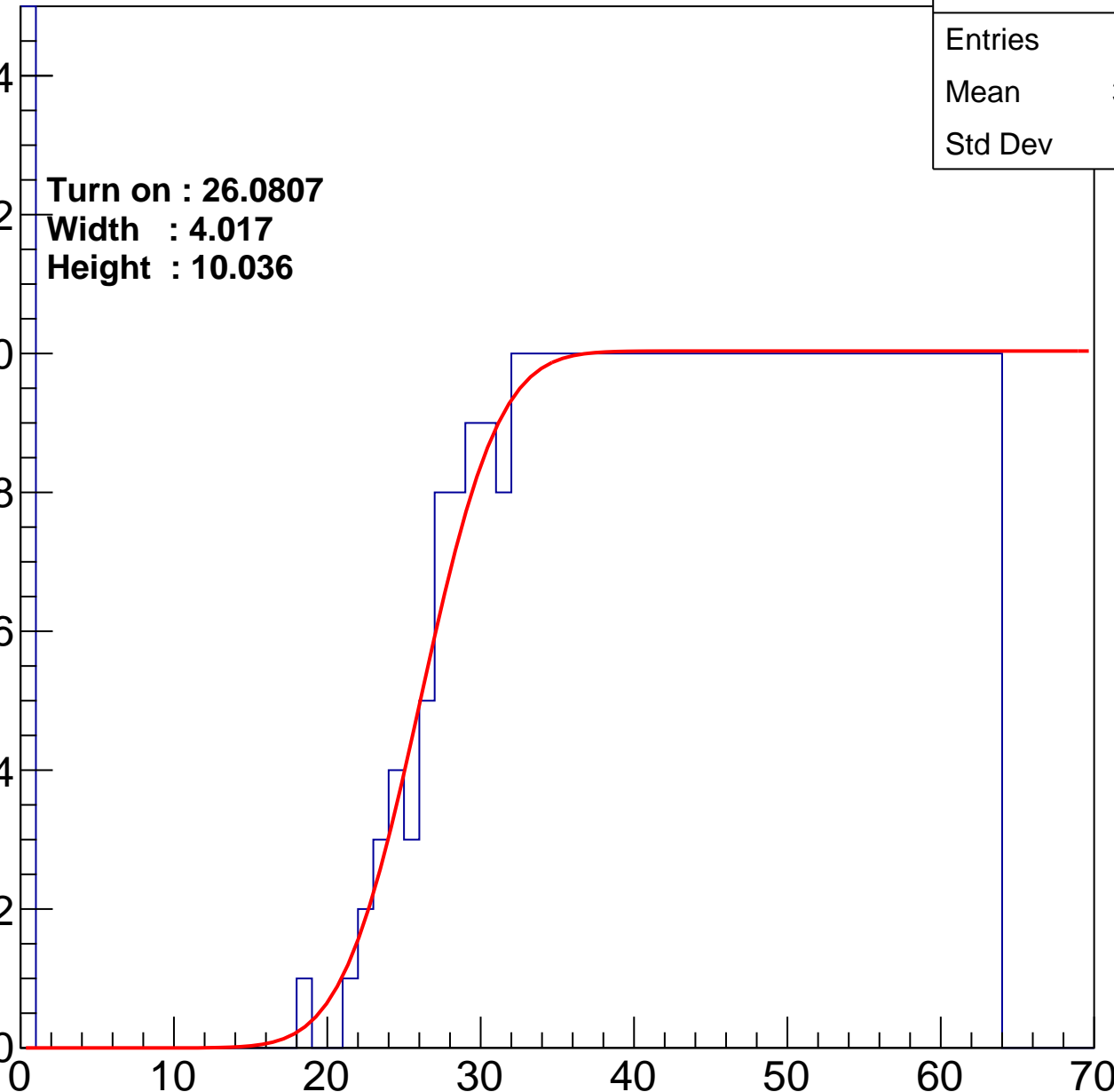
Width : 4.017

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch100

calib_packv5_041523_1651.root, FC#0, port C2

Entries	483
Mean	36.68
Std Dev	18.54

Turn on : 22.3619

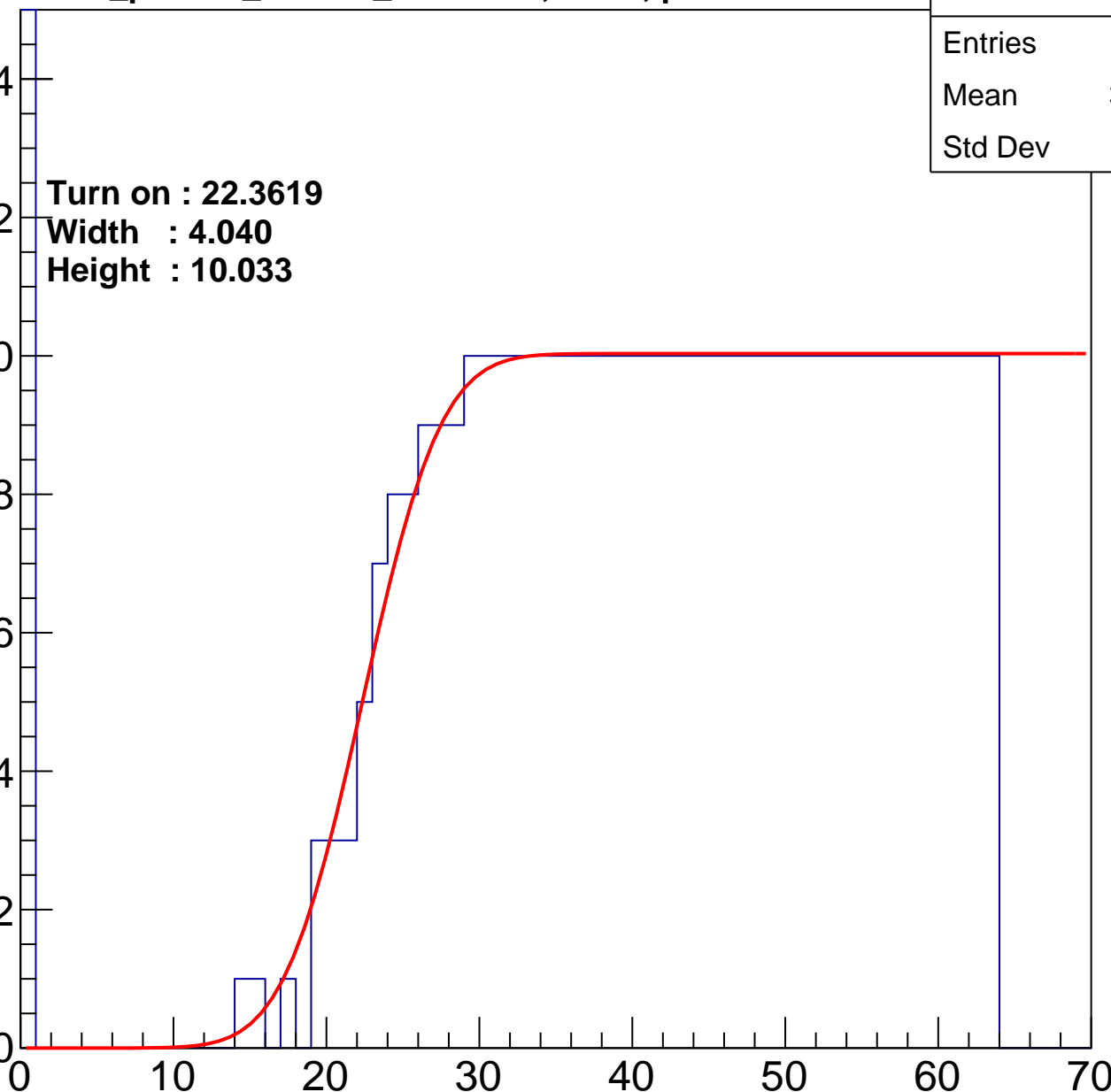
Width : 4.040

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch101

calib_packv5_041523_1651.root, FC#0, port C2

Entries	448
Mean	38.24
Std Dev	18.13

Turn on : 24.6359

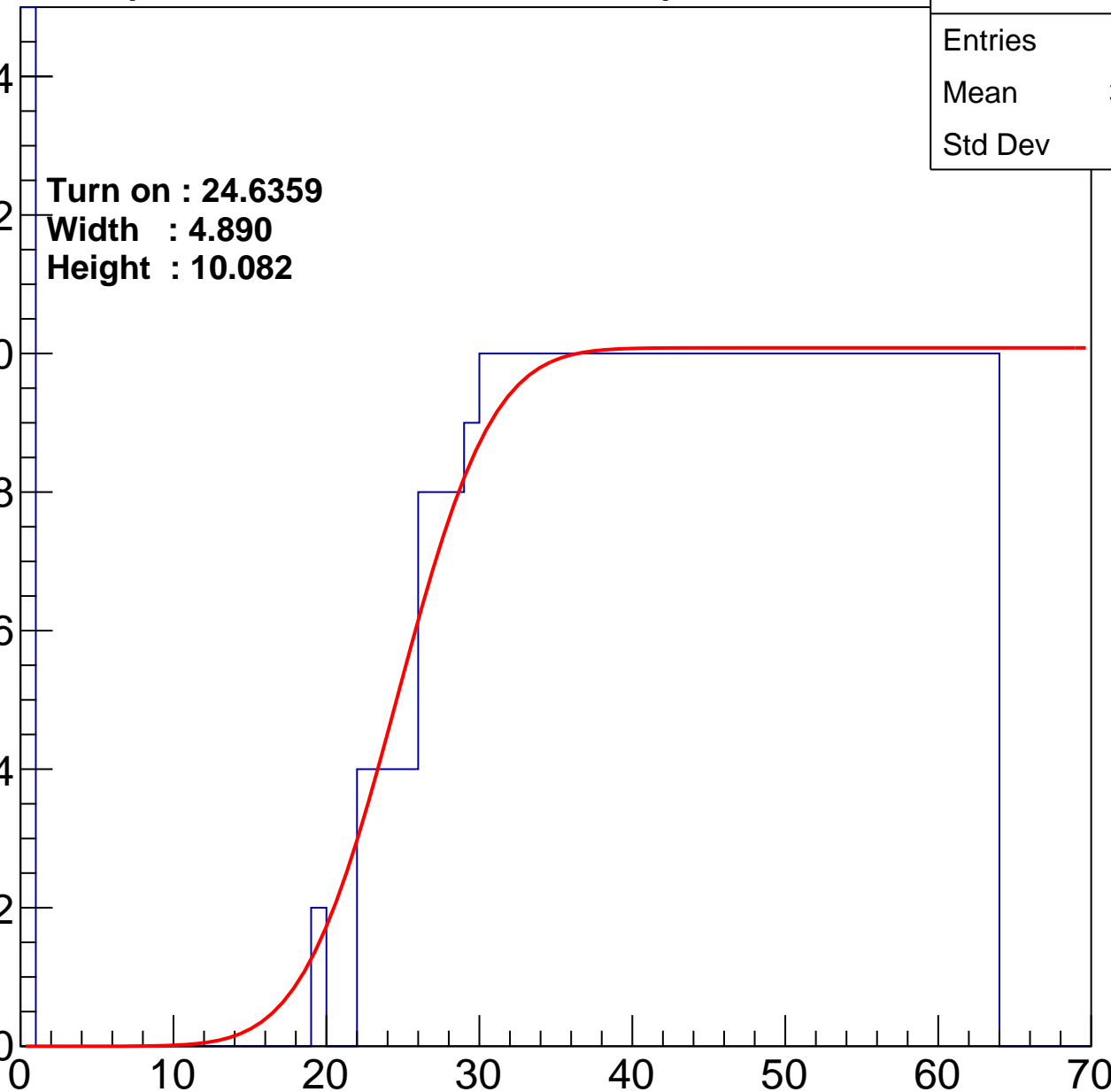
Width : 4.890

Height : 10.082

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch102

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	38.17
Std Dev	18.51

Turn on : 25.8670

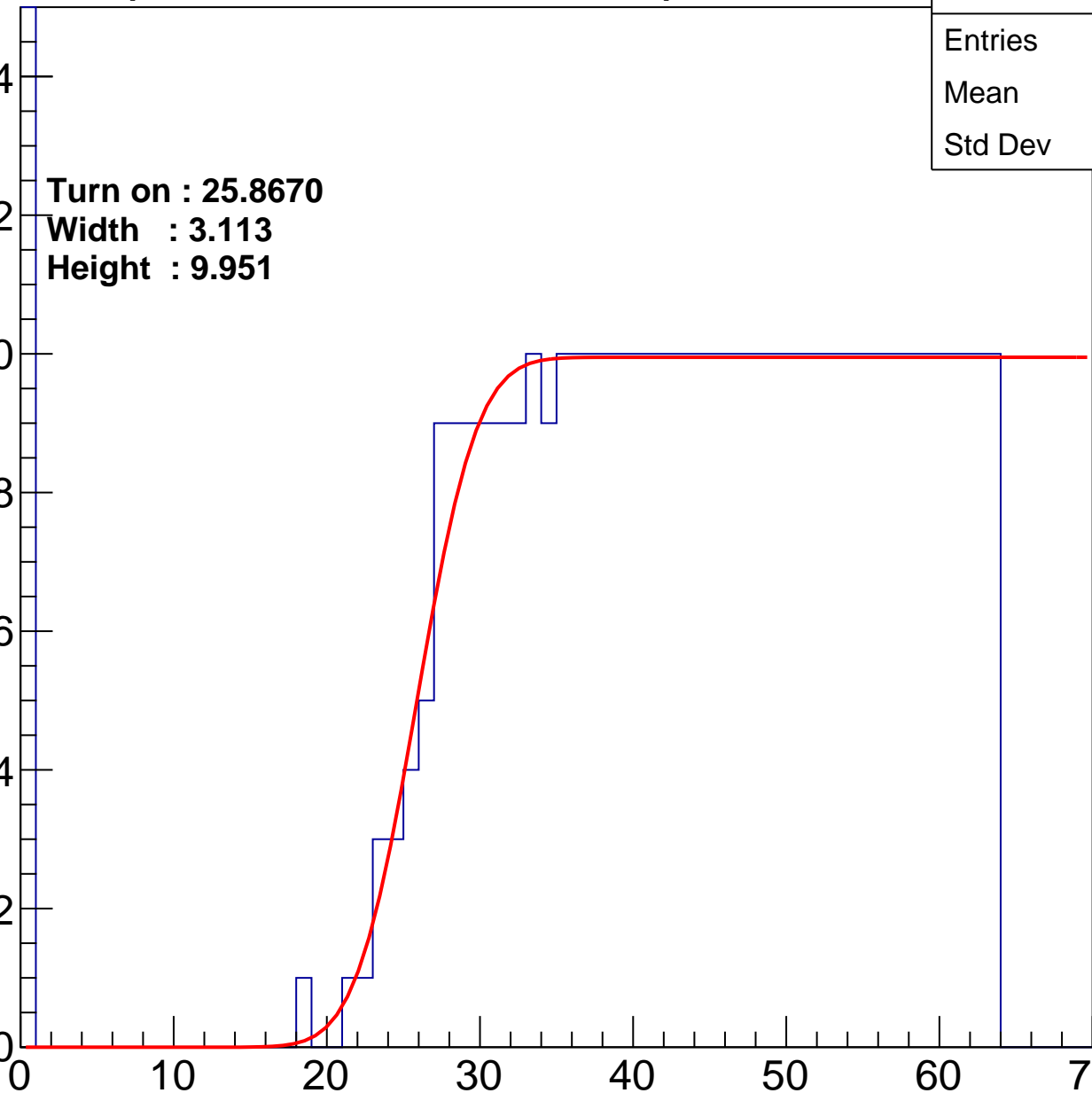
Width : 3.113

Height : 9.951

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch103

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	39.38
Std Dev	17.21

Turn on : 25.7177

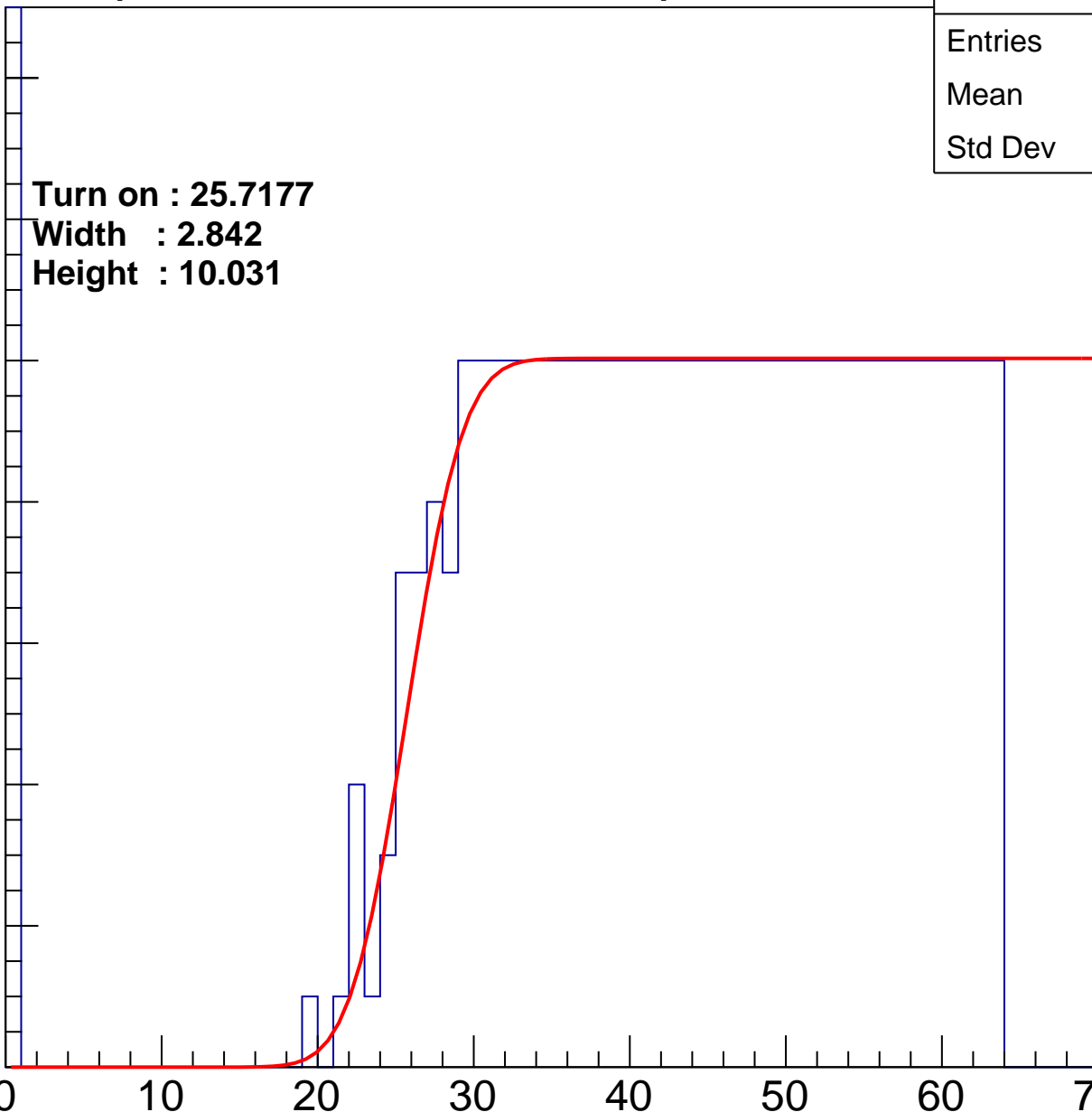
Width : 2.842

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch104

calib_packv5_041523_1651.root, FC#0, port C2

Entries	445
Mean	38.94
Std Dev	17.27

Turn on : 24.5247

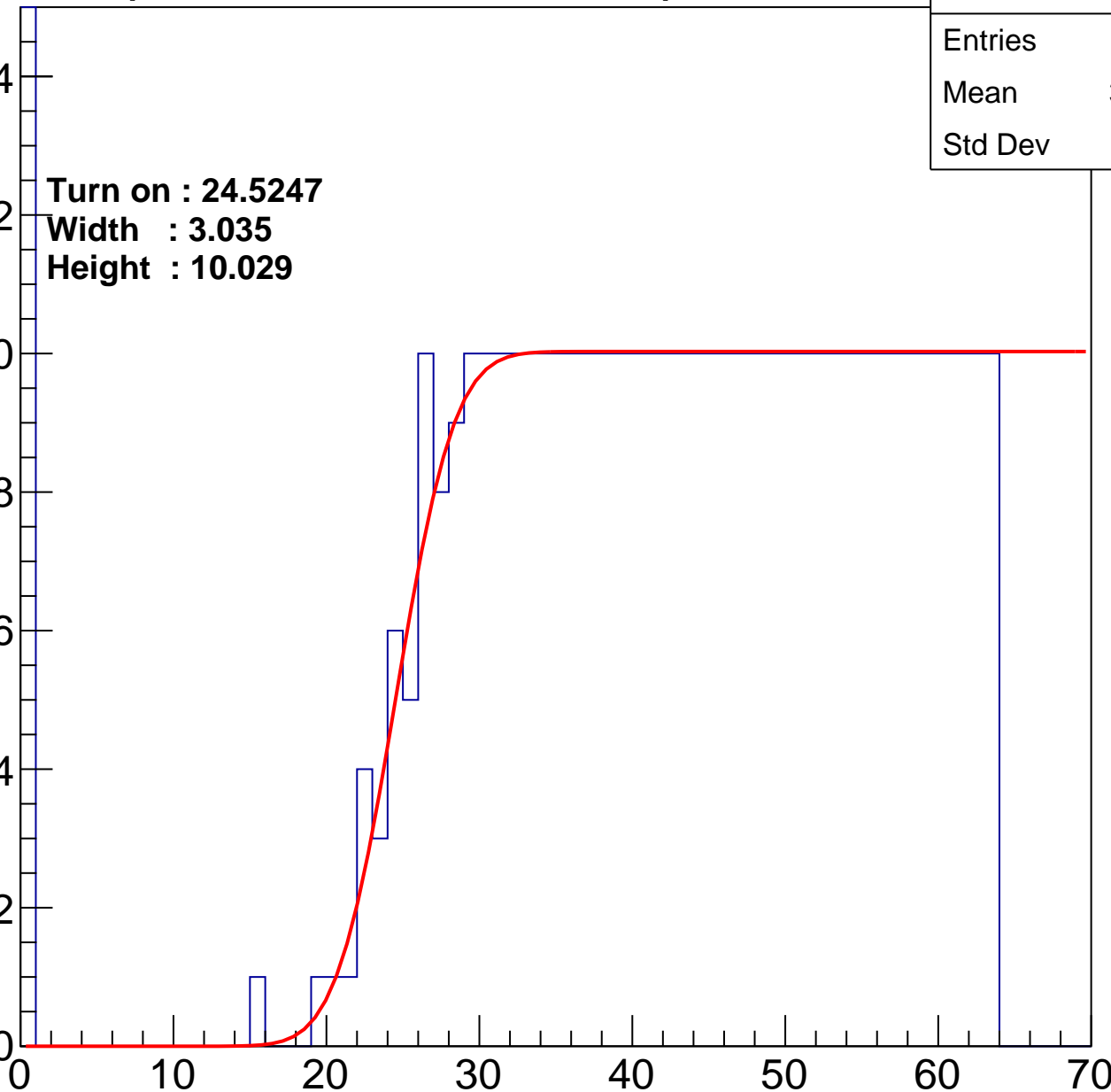
Width : 3.035

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch105

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	38.86
Std Dev	17.79

Turn on : 26.4423

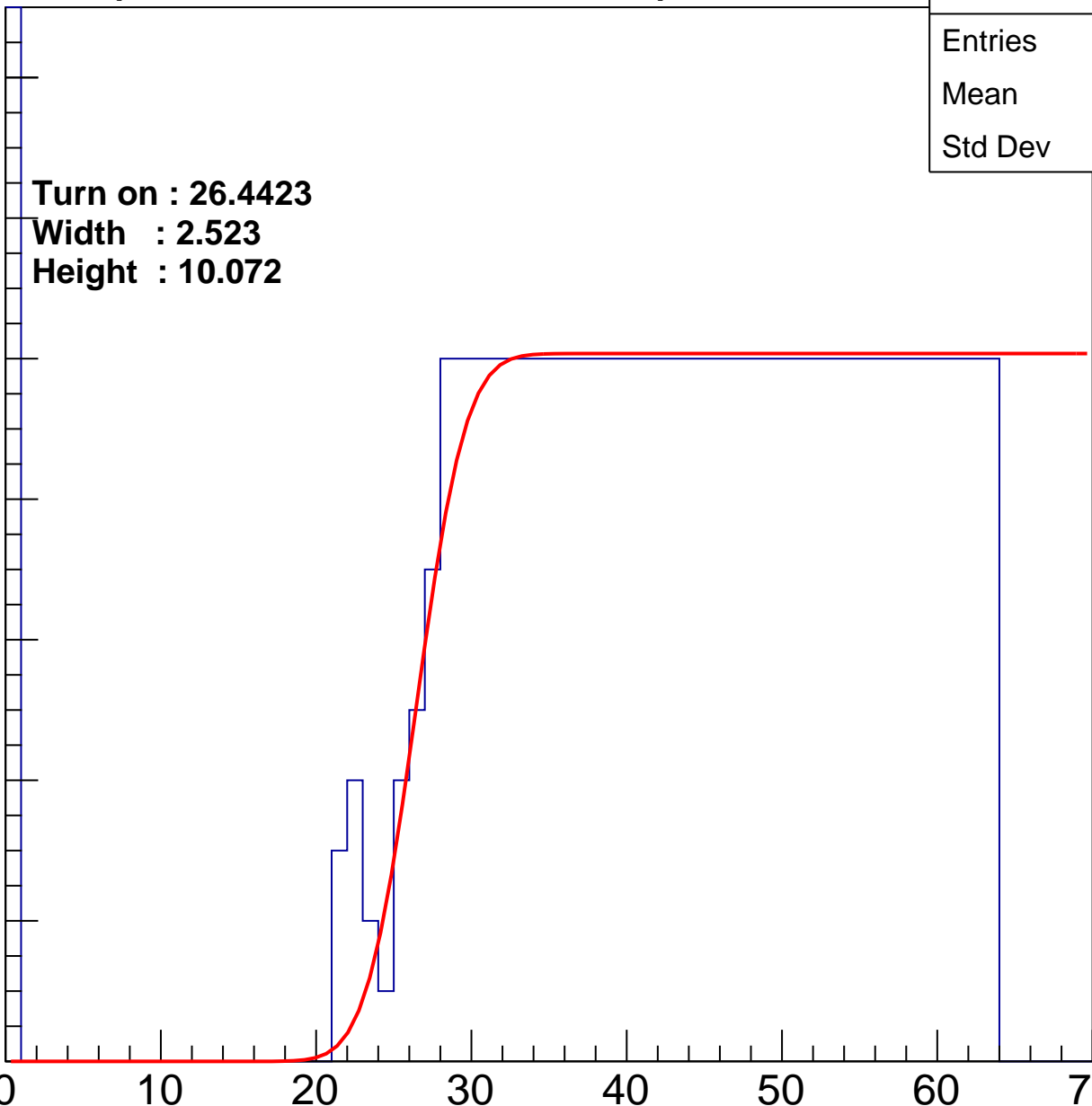
Width : 2.523

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch106

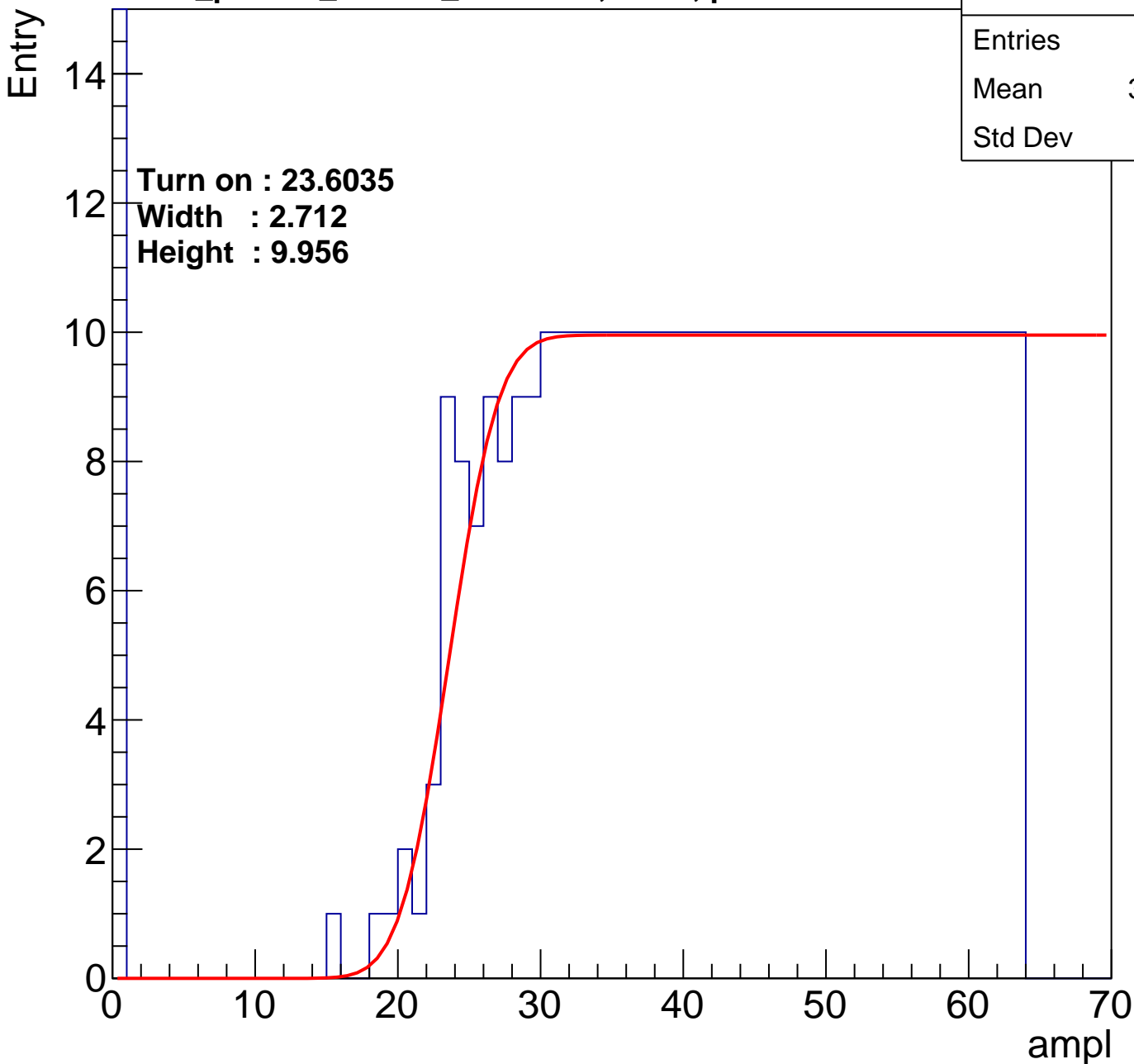
calib_packv5_041523_1651.root, FC#0, port C2

Entries	463
Mean	37.85
Std Dev	17.9

Turn on : 23.6035

Width : 2.712

Height : 9.956



B1L103S, U19-ch107

calib_packv5_041523_1651.root, FC#0, port C2

Entries	456
Mean	37.83
Std Dev	18.31

Turn on : 25.2339

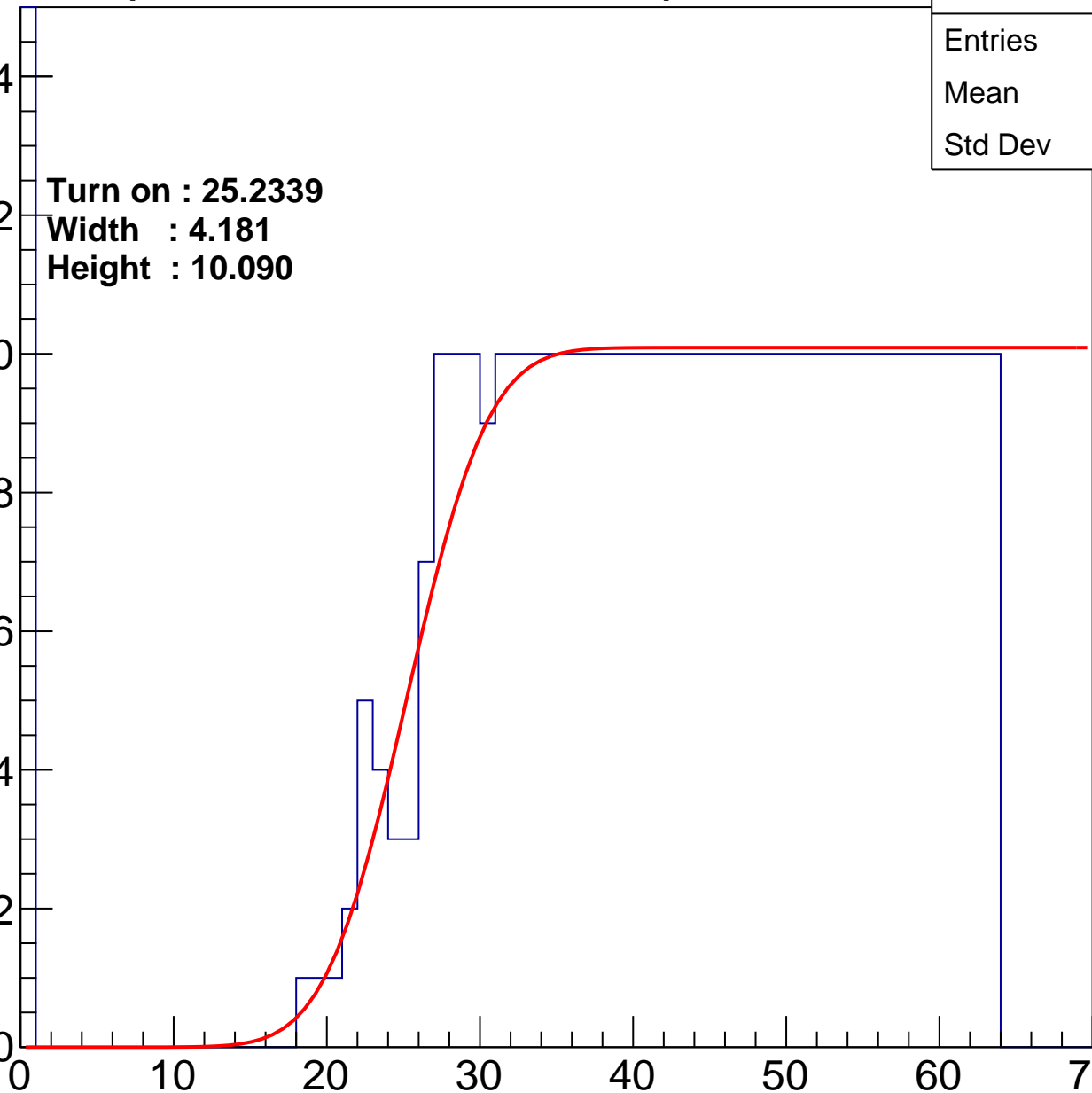
Width : 4.181

Height : 10.090

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch108

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.29
Std Dev	17.7

Turn on : 26.8529

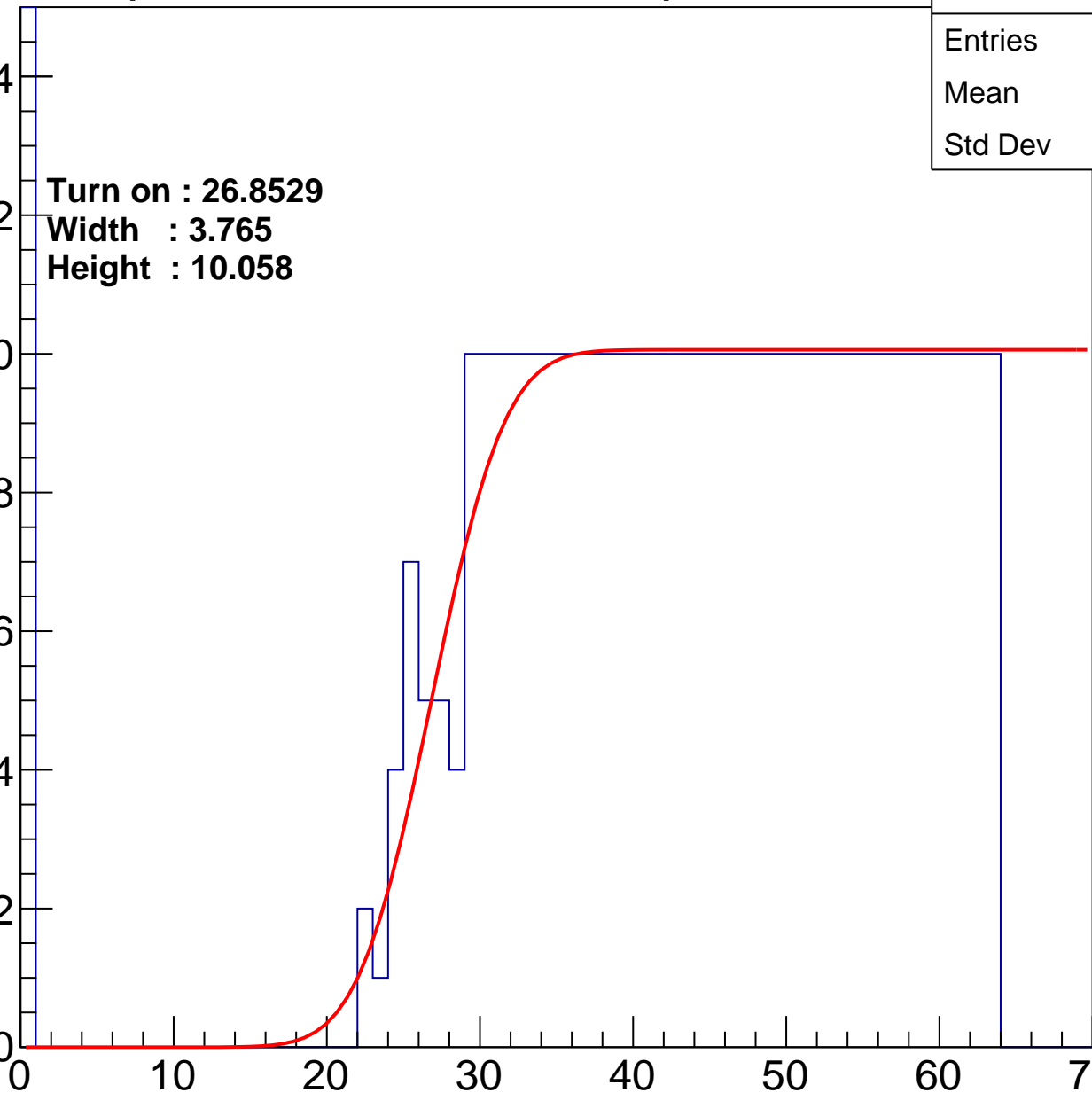
Width : 3.765

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch109

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	38.09
Std Dev	18.59

Turn on : 26.6136

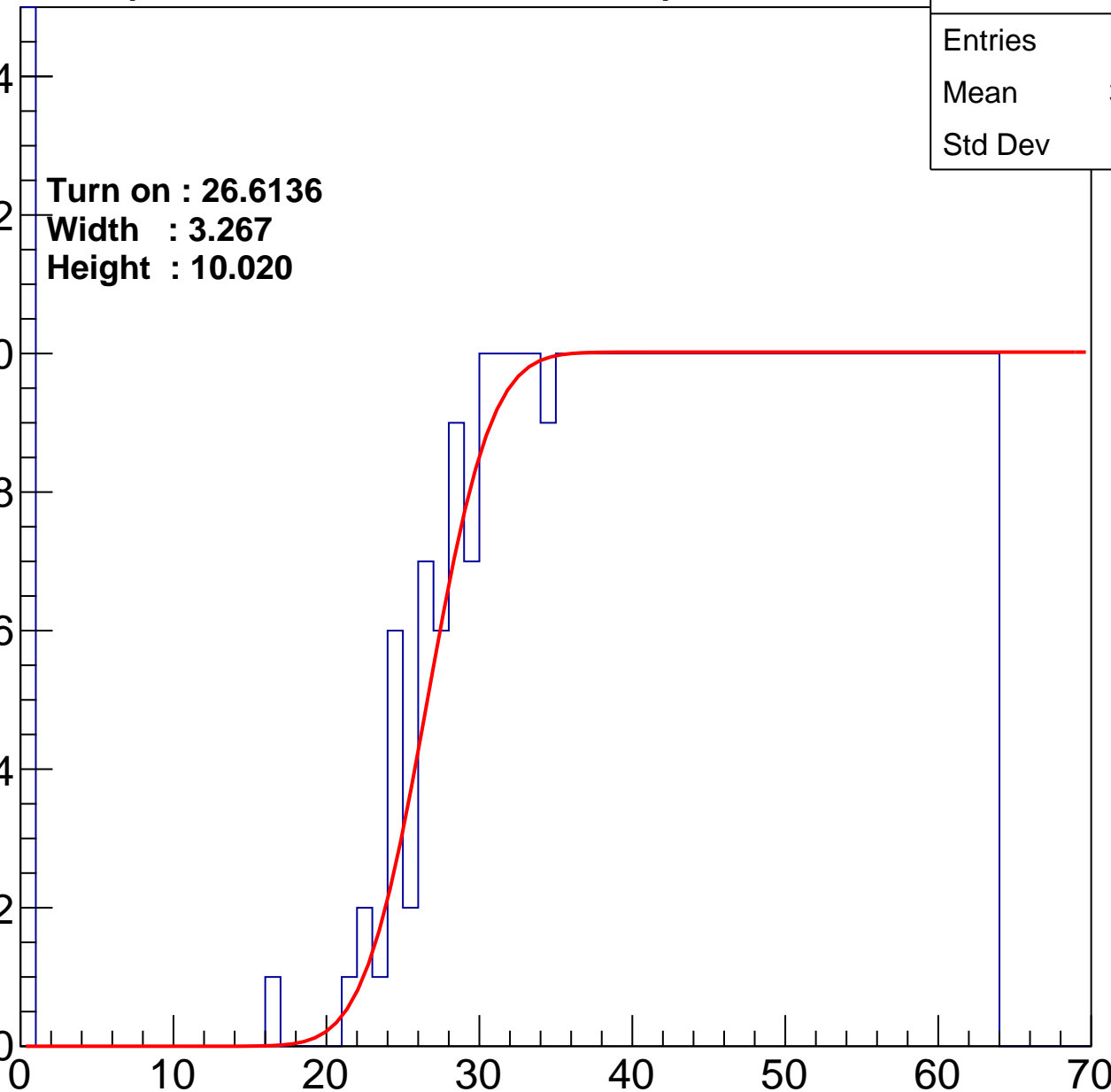
Width : 3.267

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch110

calib_packv5_041523_1651.root, FC#0, port C2

Entries	451
Mean	38.67
Std Dev	17.34

Turn on : 24.4652

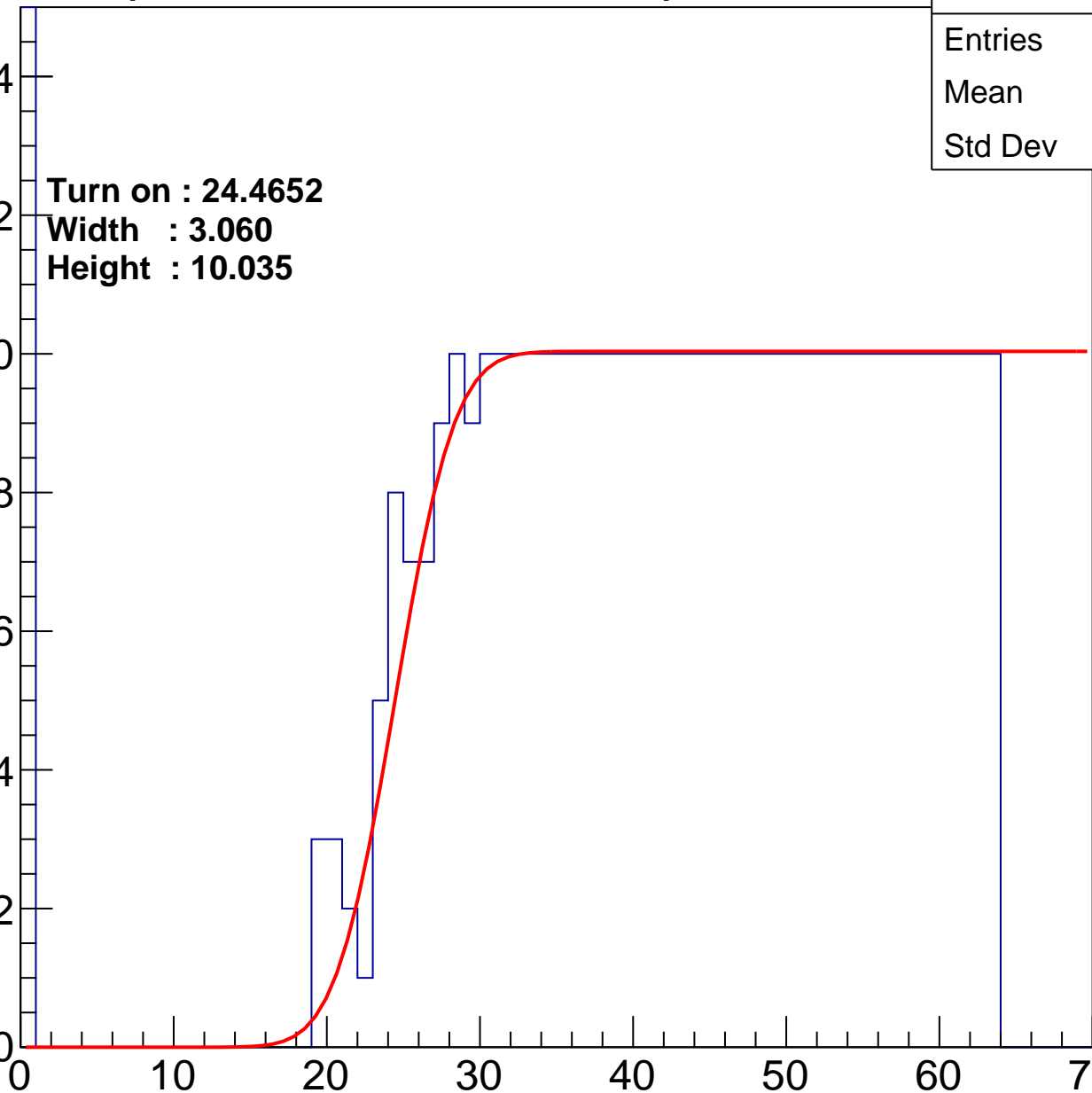
Width : 3.060

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch111

calib_packv5_041523_1651.root, FC#0, port C2

Entries	447
Mean	38.08
Std Dev	18.43

Turn on : 25.8145

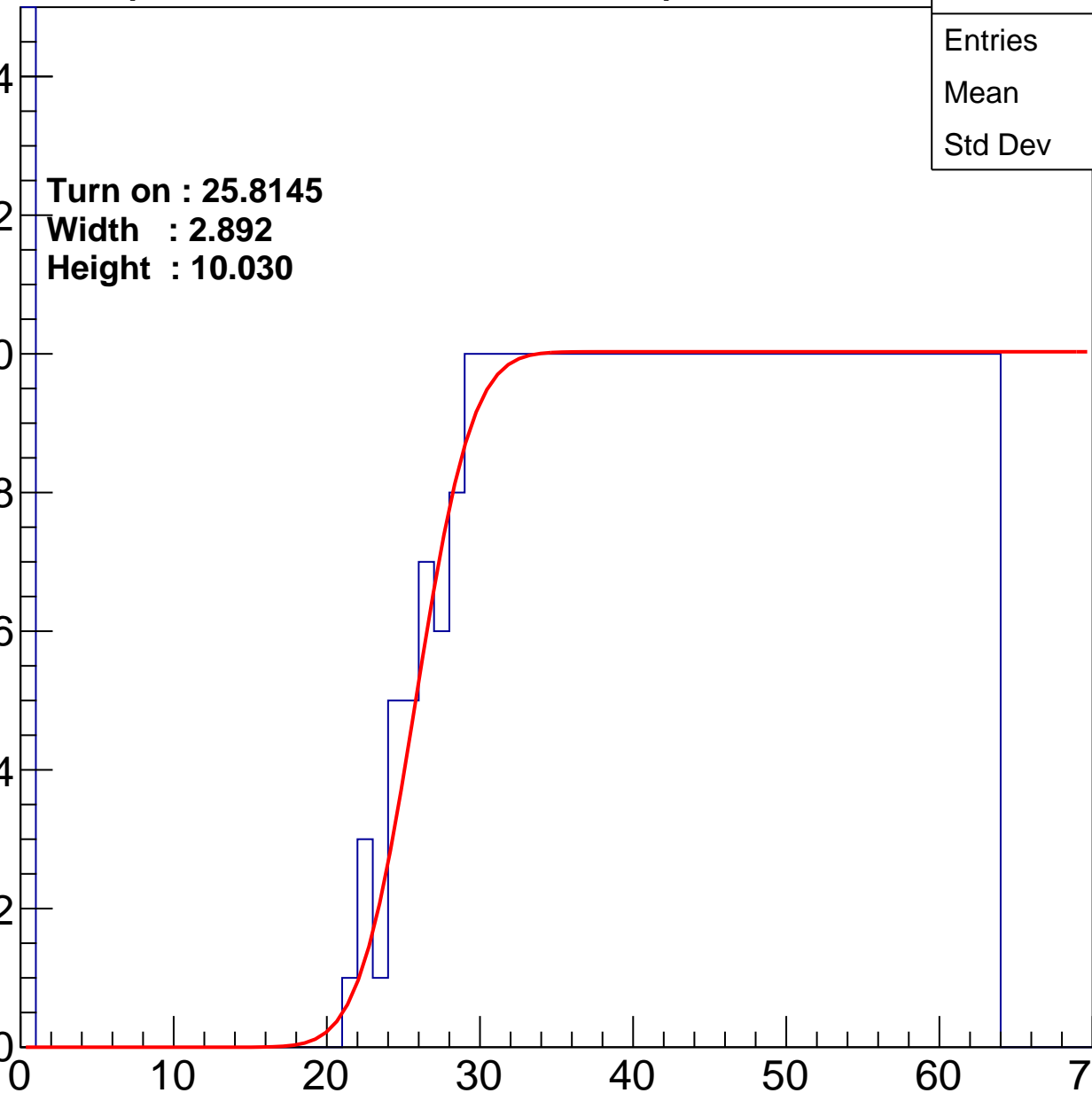
Width : 2.892

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch112

calib_packv5_041523_1651.root, FC#0, port C2

Entries	446
Mean	39.05
Std Dev	17.3

Turn on : 24.9462

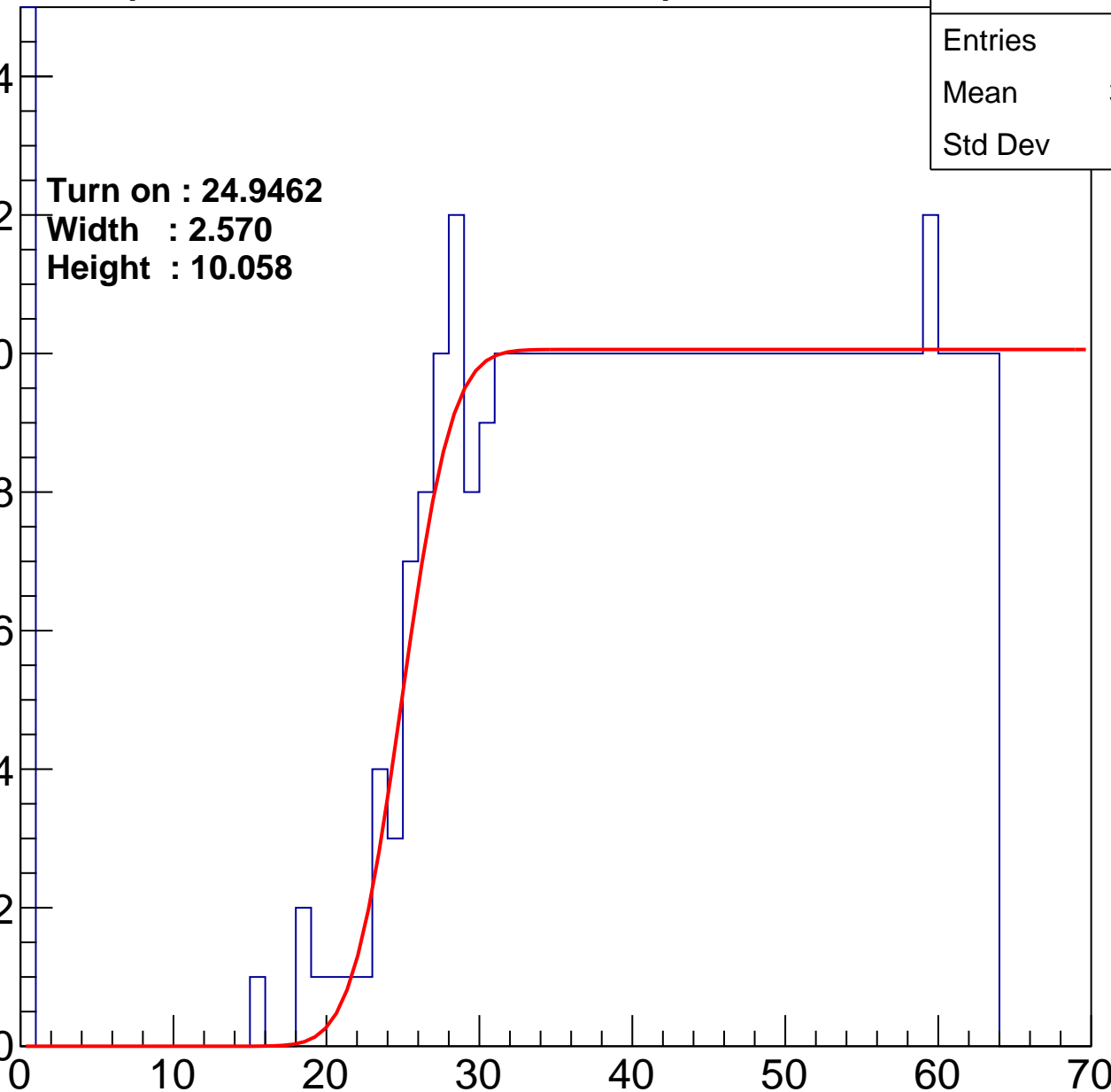
Width : 2.570

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch113

calib_packv5_041523_1651.root, FC#0, port C2

Entries	444
Mean	38.28
Std Dev	18.26

Turn on : 25.4011

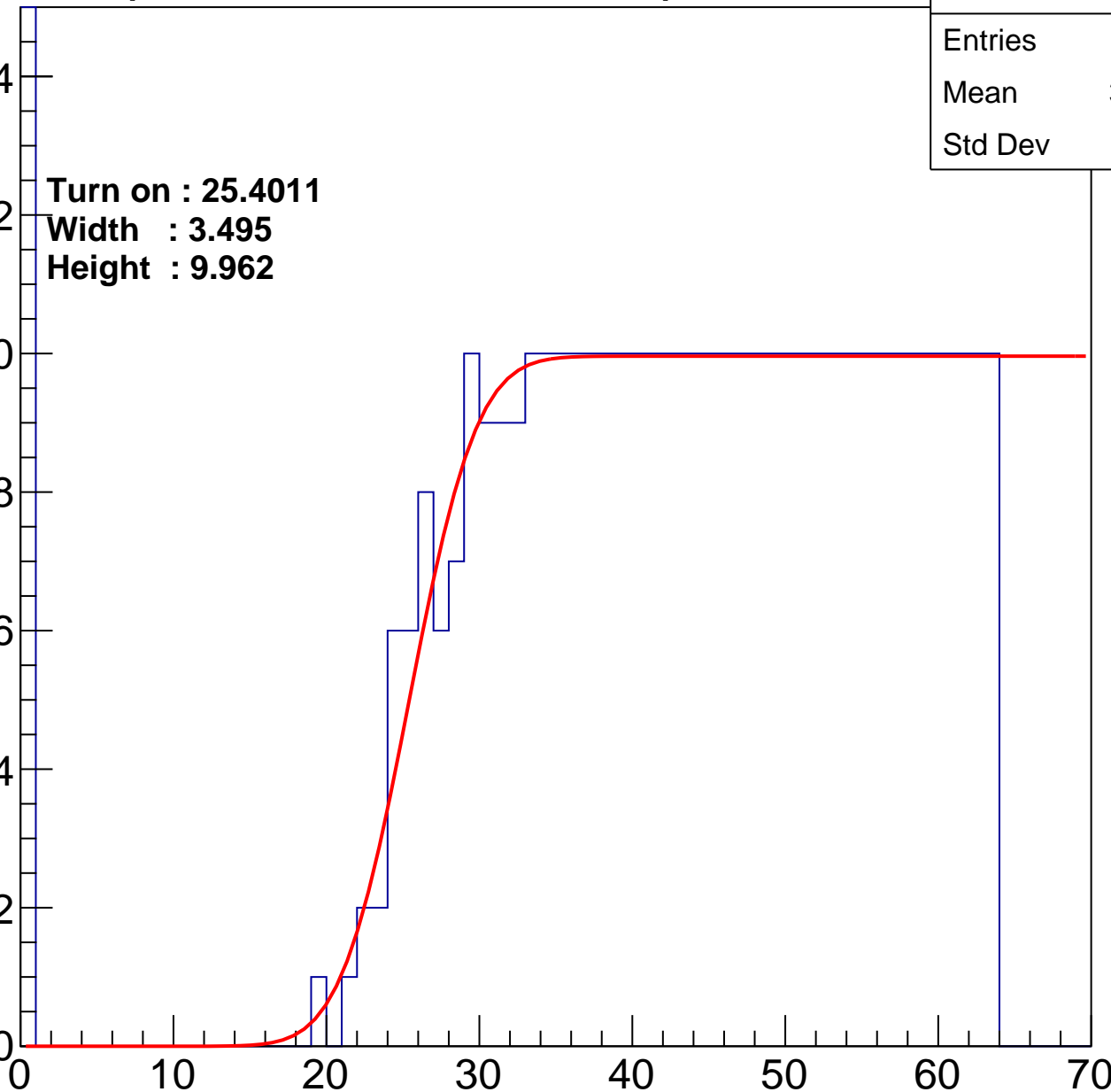
Width : 3.495

Height : 9.962

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch114

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	39.38
Std Dev	16.93

Turn on : 24.6401

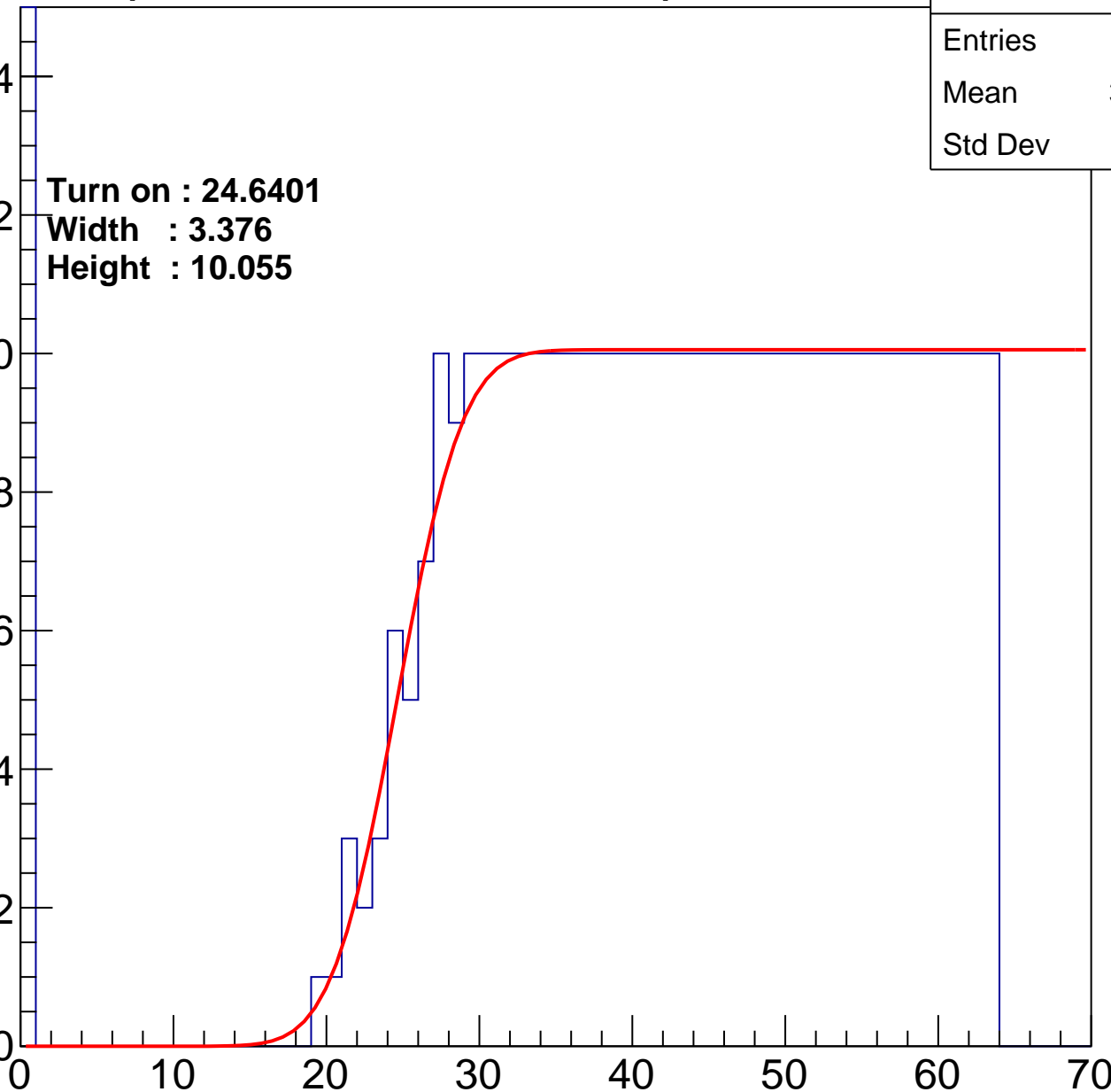
Width : 3.376

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch115

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	39.86
Std Dev	17.15

Turn on : 26.3338

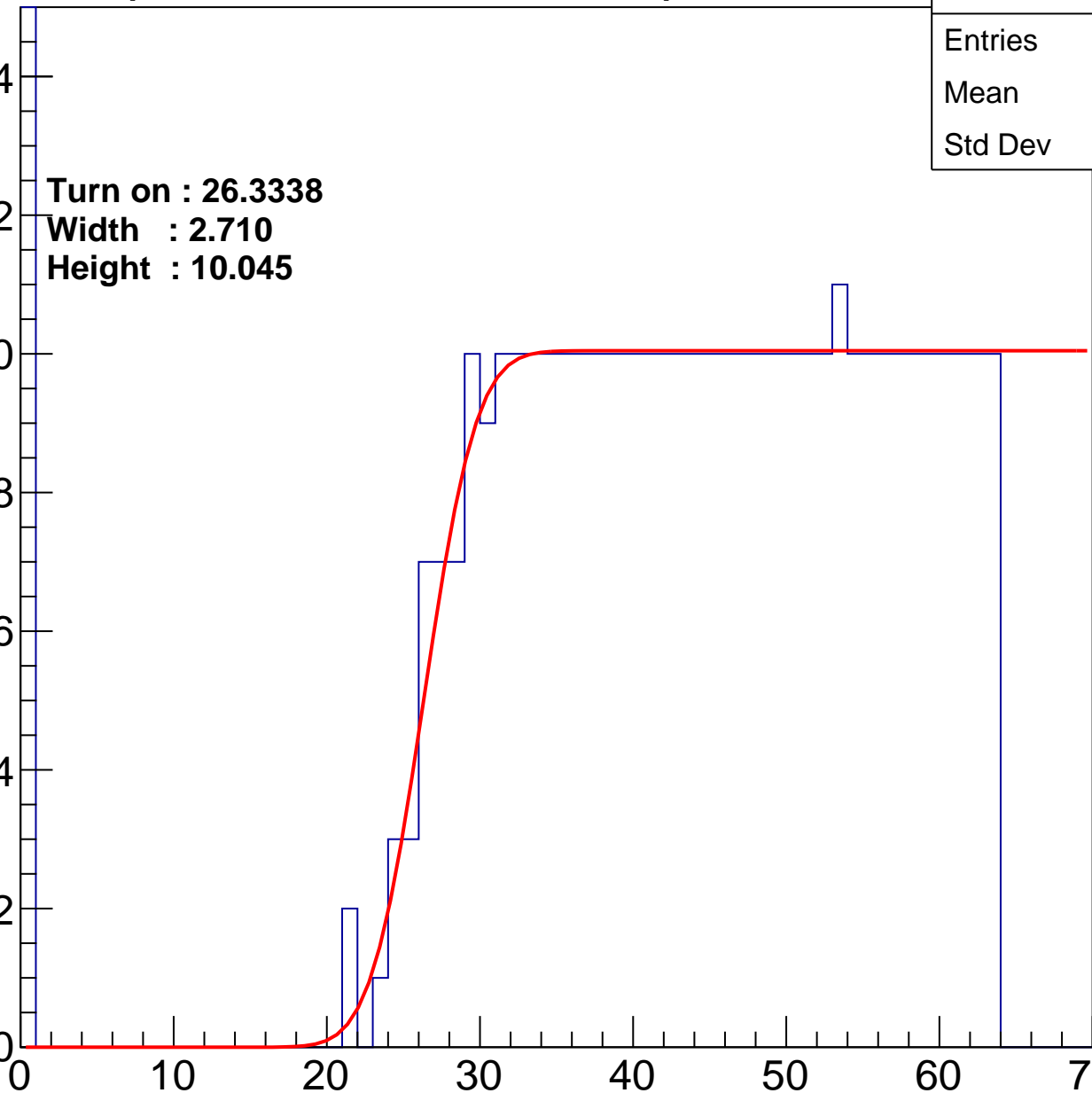
Width : 2.710

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch116

calib_packv5_041523_1651.root, FC#0, port C2

Entries	454
Mean	38.08
Std Dev	18.07

Turn on : 24.4599

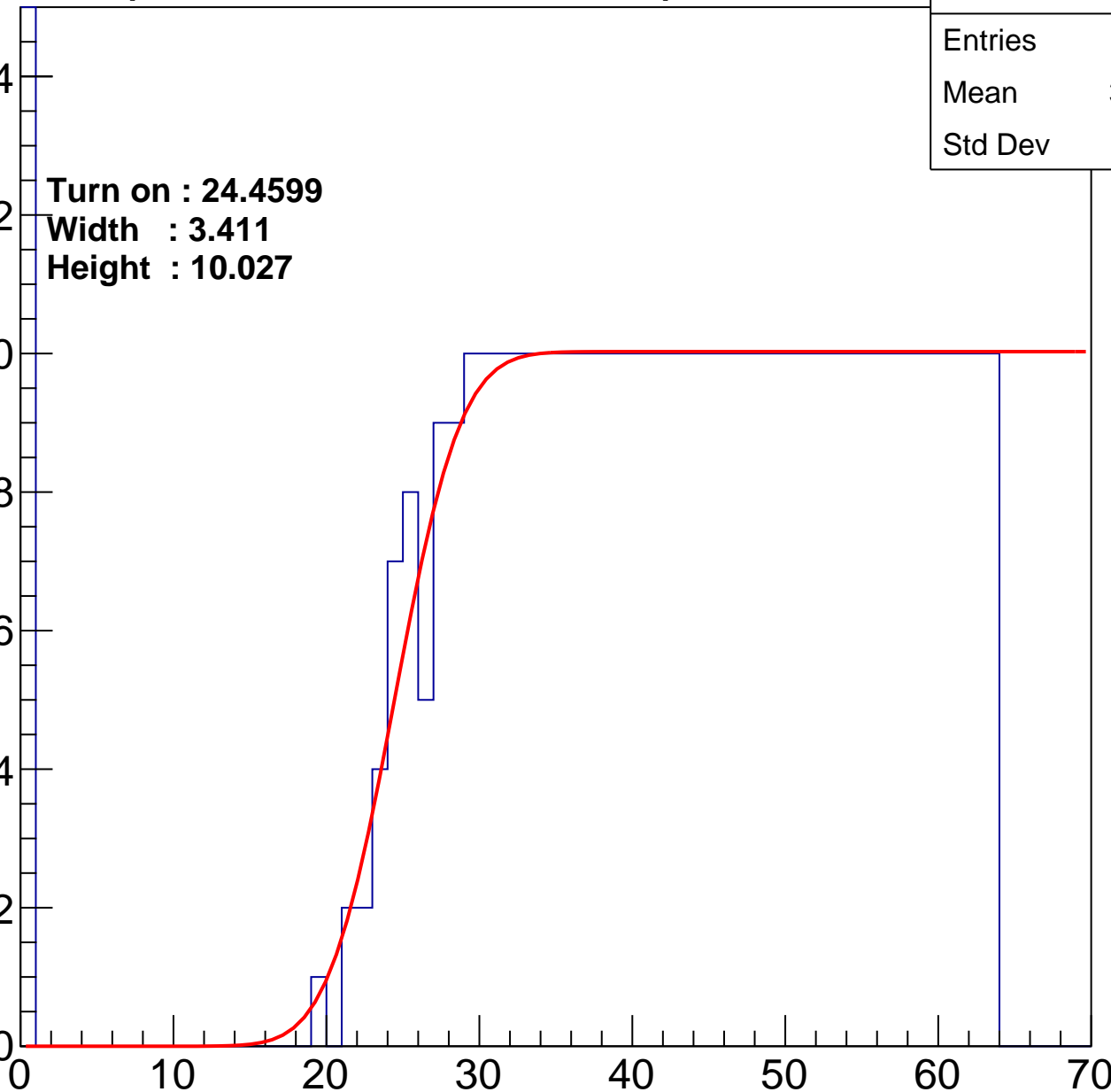
Width : 3.411

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch117

calib_packv5_041523_1651.root, FC#0, port C2

Entries	452
Mean	37.86
Std Dev	18.47

Turn on : 24.9936

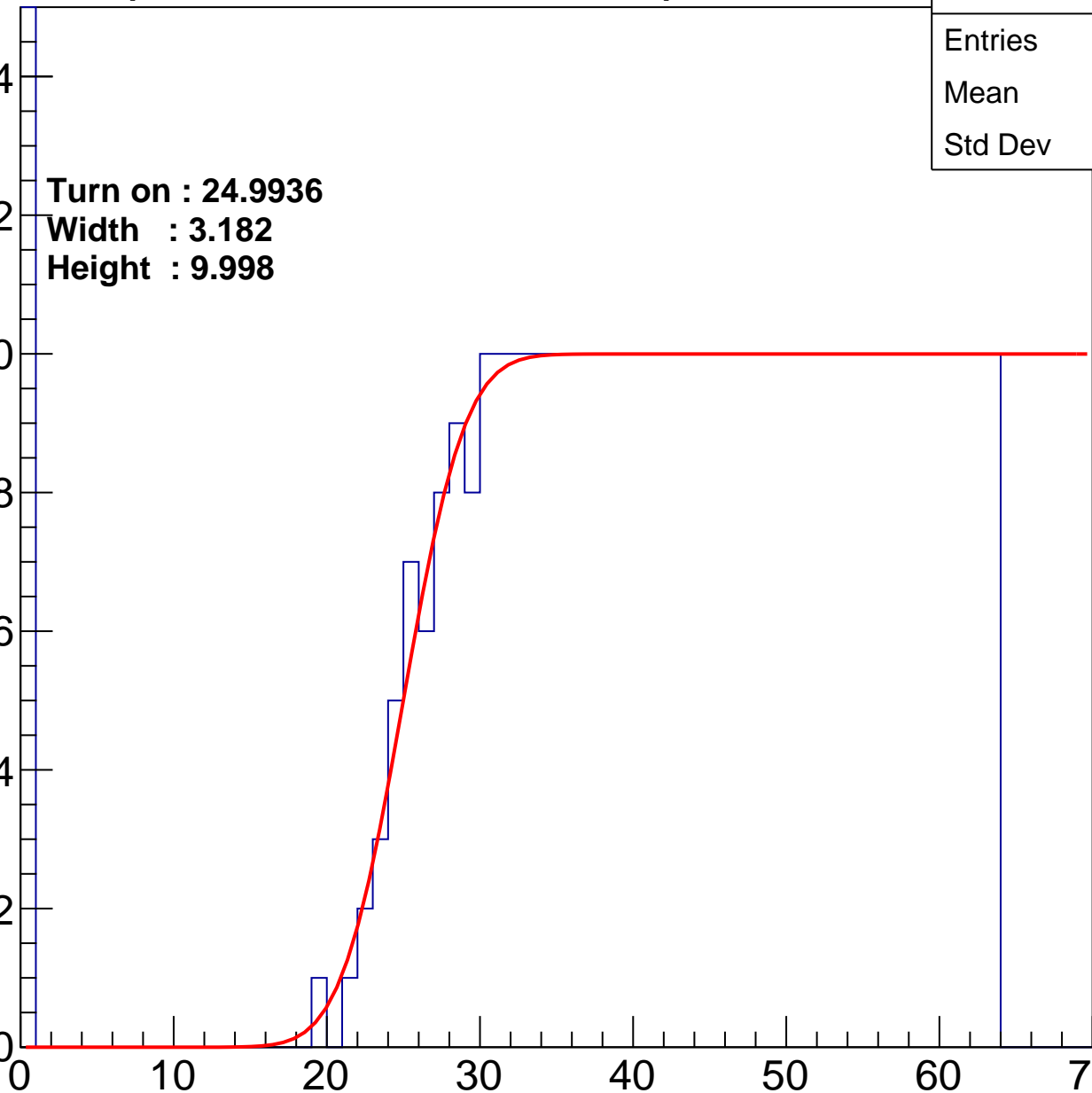
Width : 3.182

Height : 9.998

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch118

calib_packv5_041523_1651.root, FC#0, port C2

Entries	456
Mean	38.26
Std Dev	17.68

Turn on : 23.3738

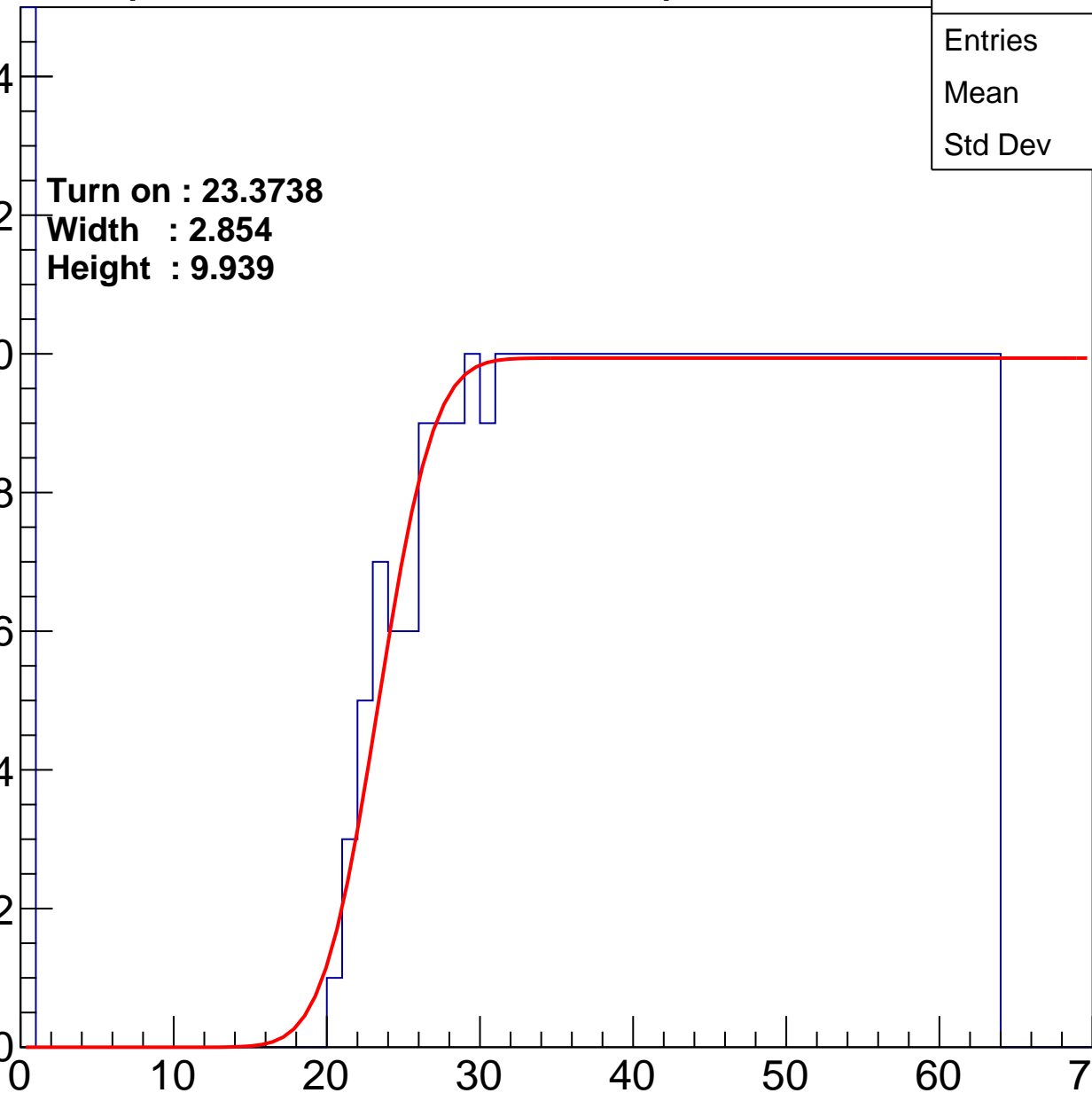
Width : 2.854

Height : 9.939

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch119

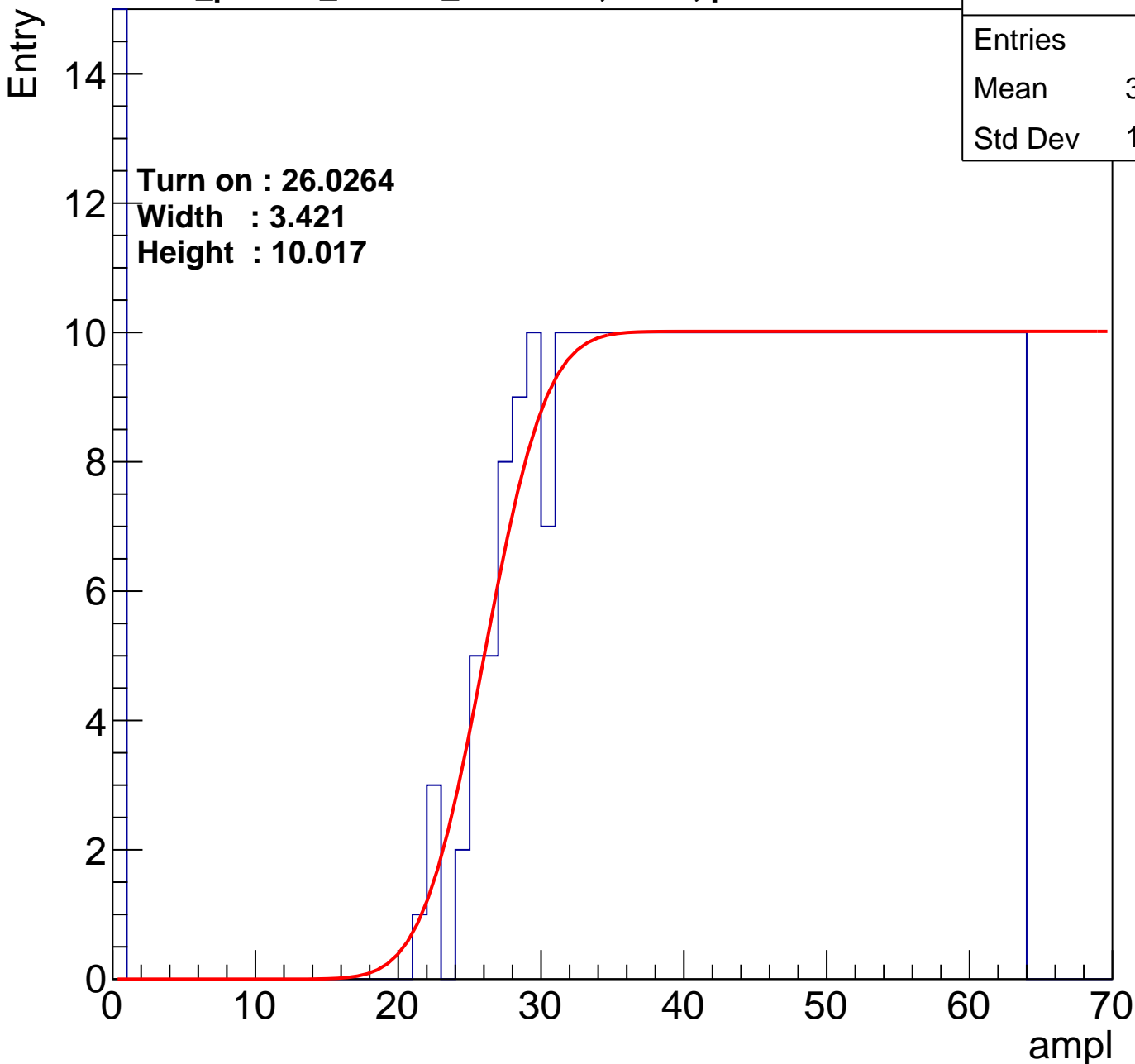
calib_packv5_041523_1651.root, FC#0, port C2

Entries	441
Mean	38.25
Std Dev	18.49

Turn on : 26.0264

Width : 3.421

Height : 10.017



B1L103S, U19-ch120

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	38.56
Std Dev	17.93

Turn on : 25.2802

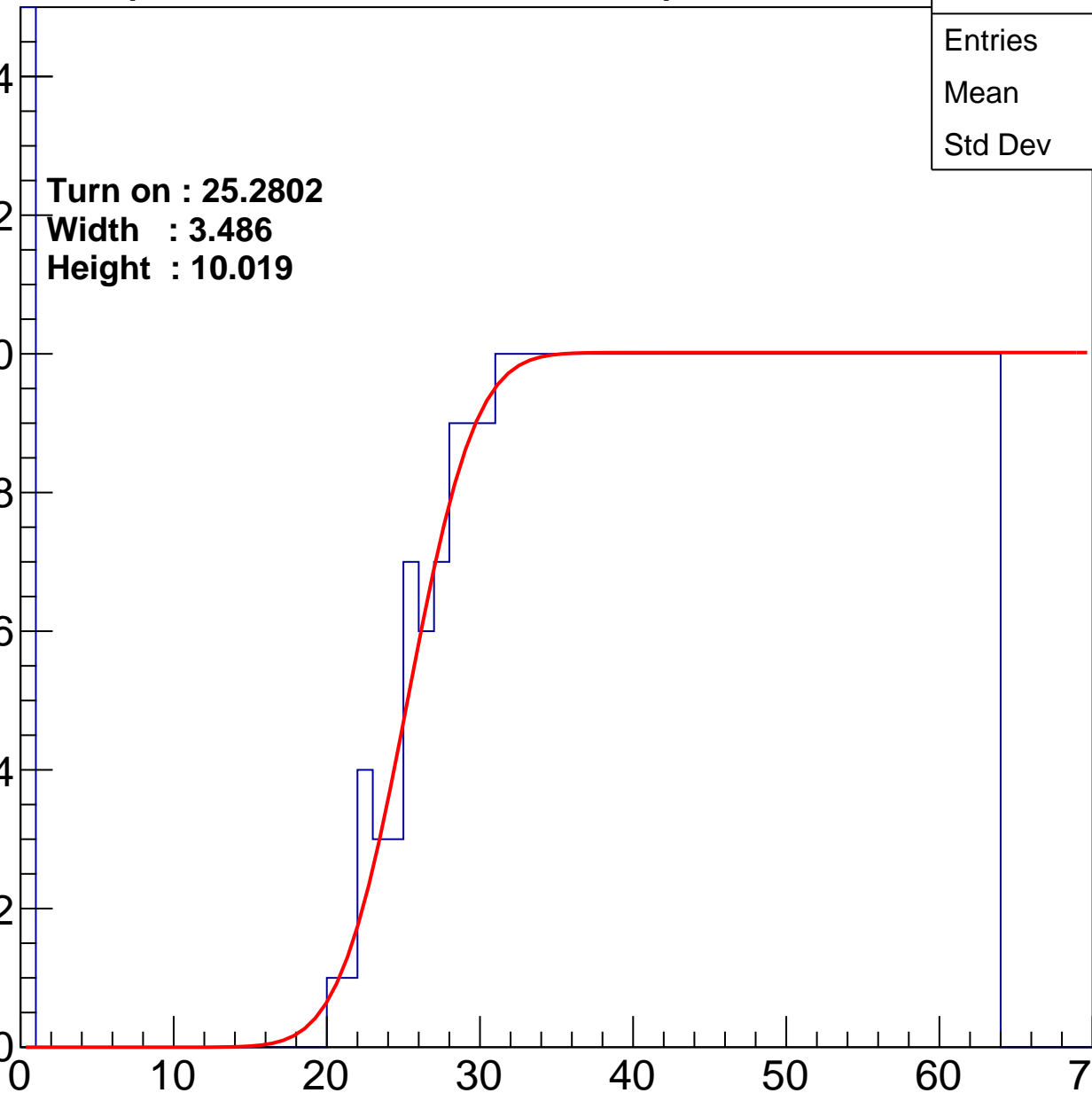
Width : 3.486

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch121

calib_packv5_041523_1651.root, FC#0, port C2

Entries	446
Mean	37.36
Std Dev	19.37

Turn on : 26.8001

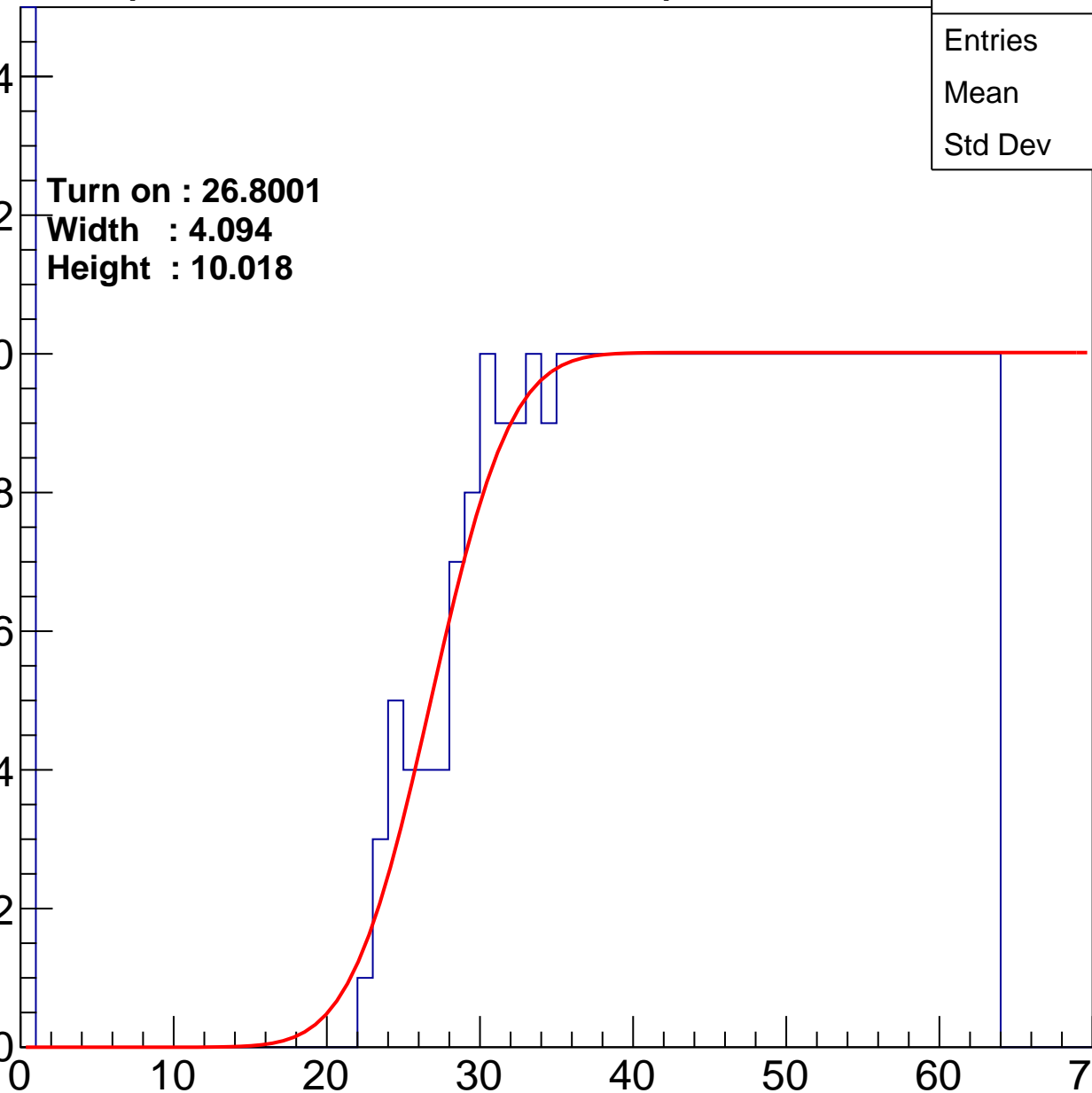
Width : 4.094

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch122

calib_packv5_041523_1651.root, FC#0, port C2

Entries	456
Mean	37.91
Std Dev	18.28

Turn on : 24.4476

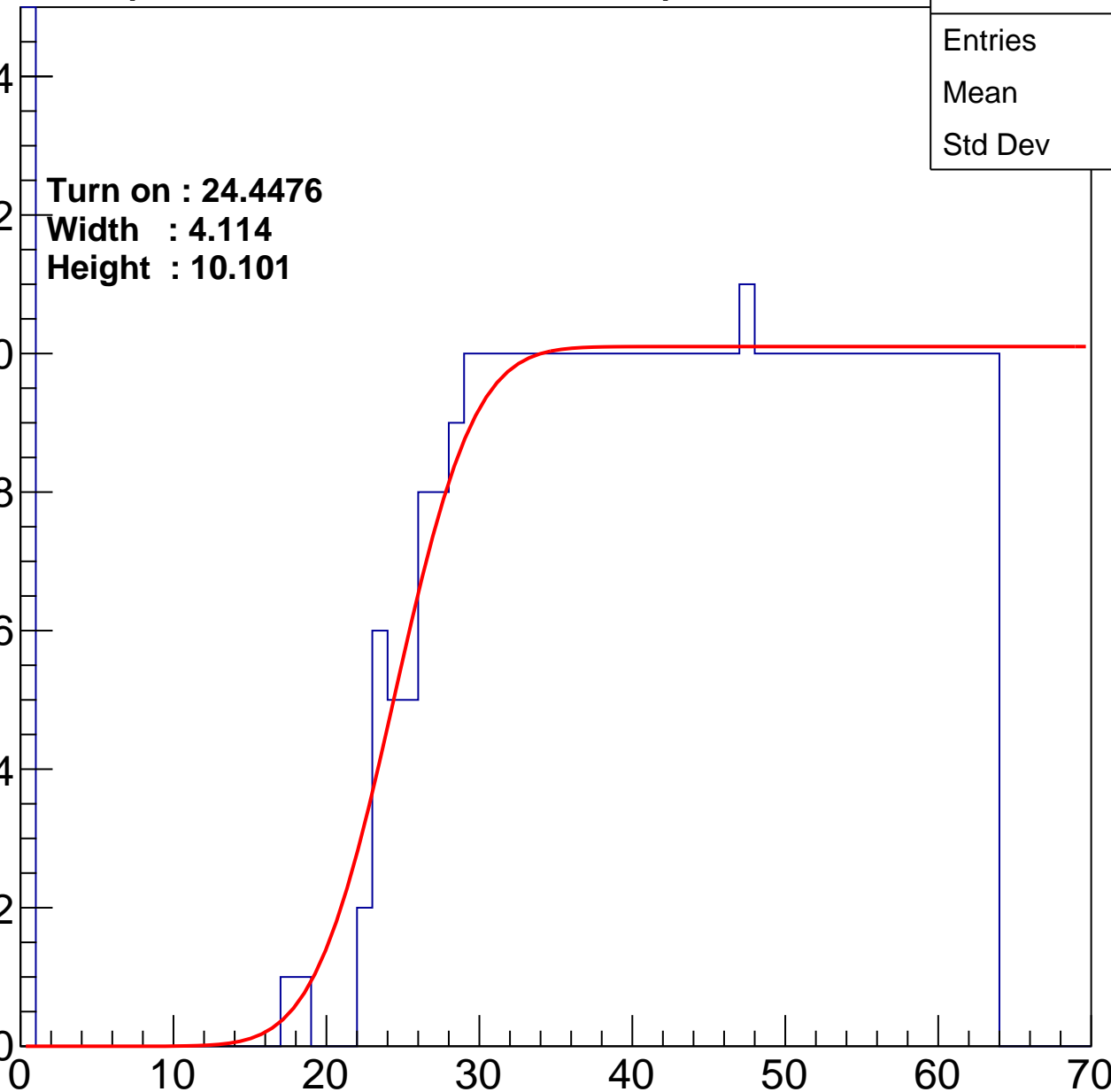
Width : 4.114

Height : 10.101

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch123

calib_packv5_041523_1651.root, FC#0, port C2

Entries	460
Mean	37.39
Std Dev	18.74

Turn on : 24.9463

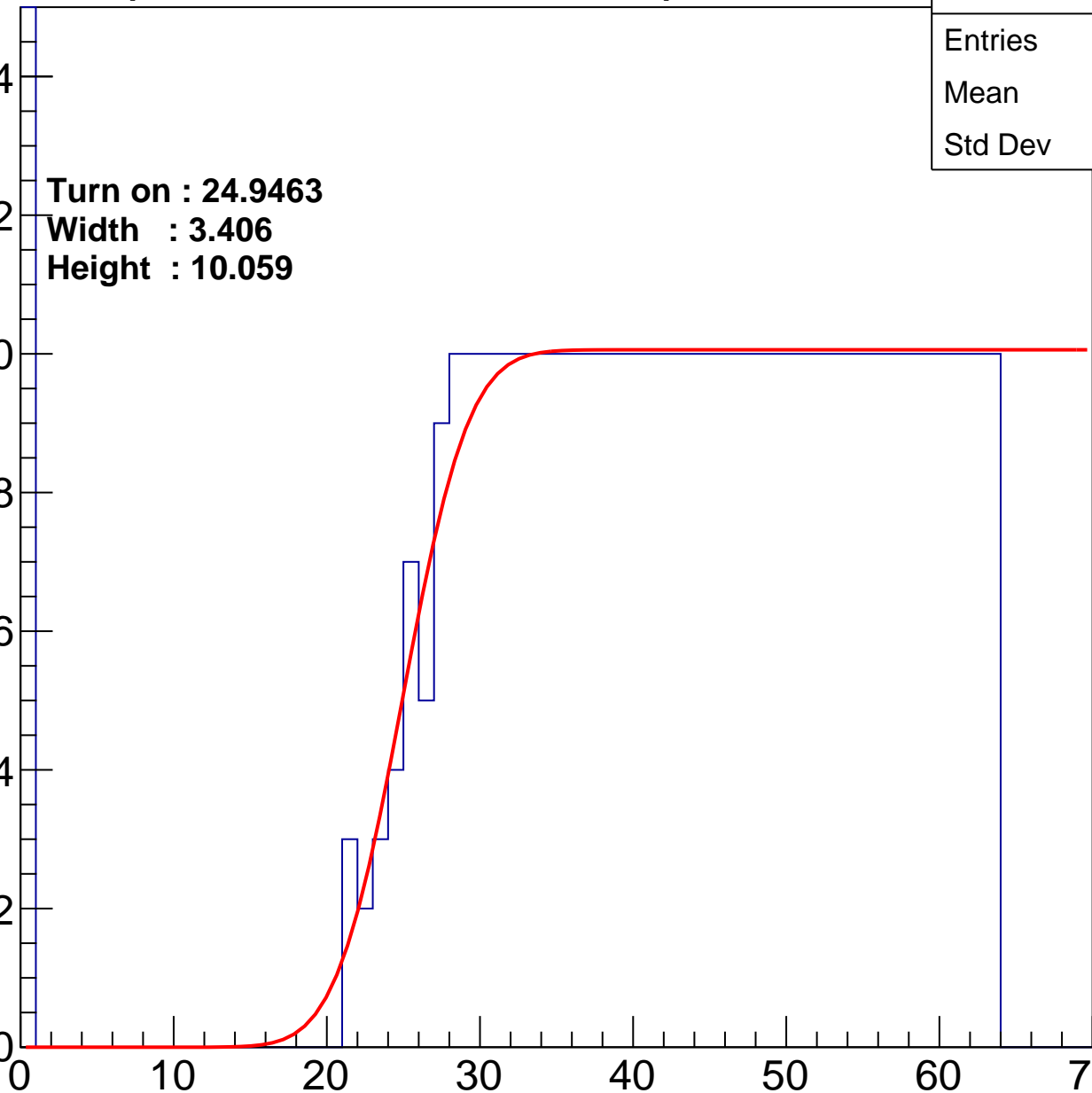
Width : 3.406

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch124

calib_packv5_041523_1651.root, FC#0, port C2

Entries	471
Mean	37.35
Std Dev	18.25

Turn on : 23.3063

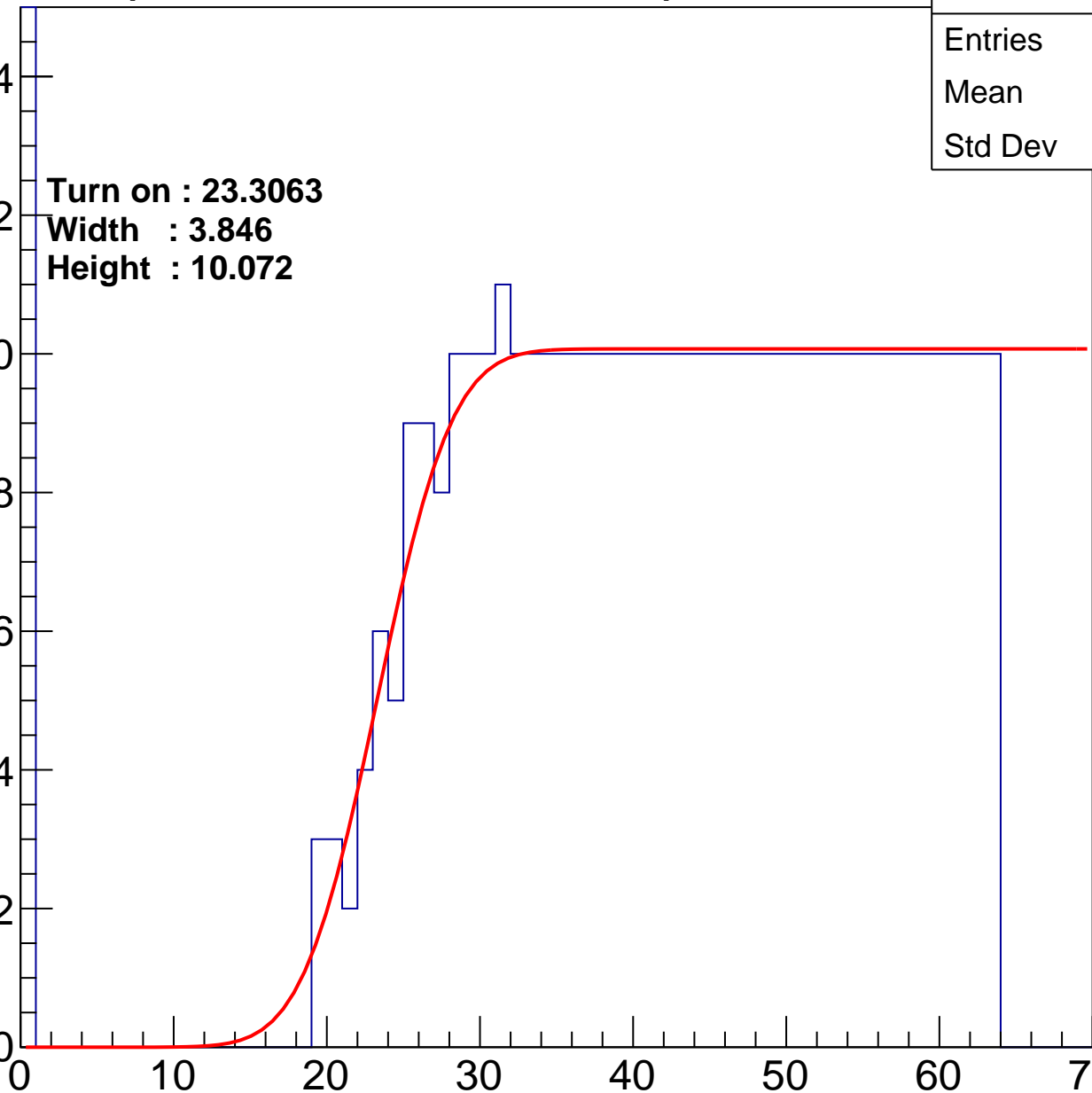
Width : 3.846

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch125

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	39.88
Std Dev	17.39

Turn on : 27.2534

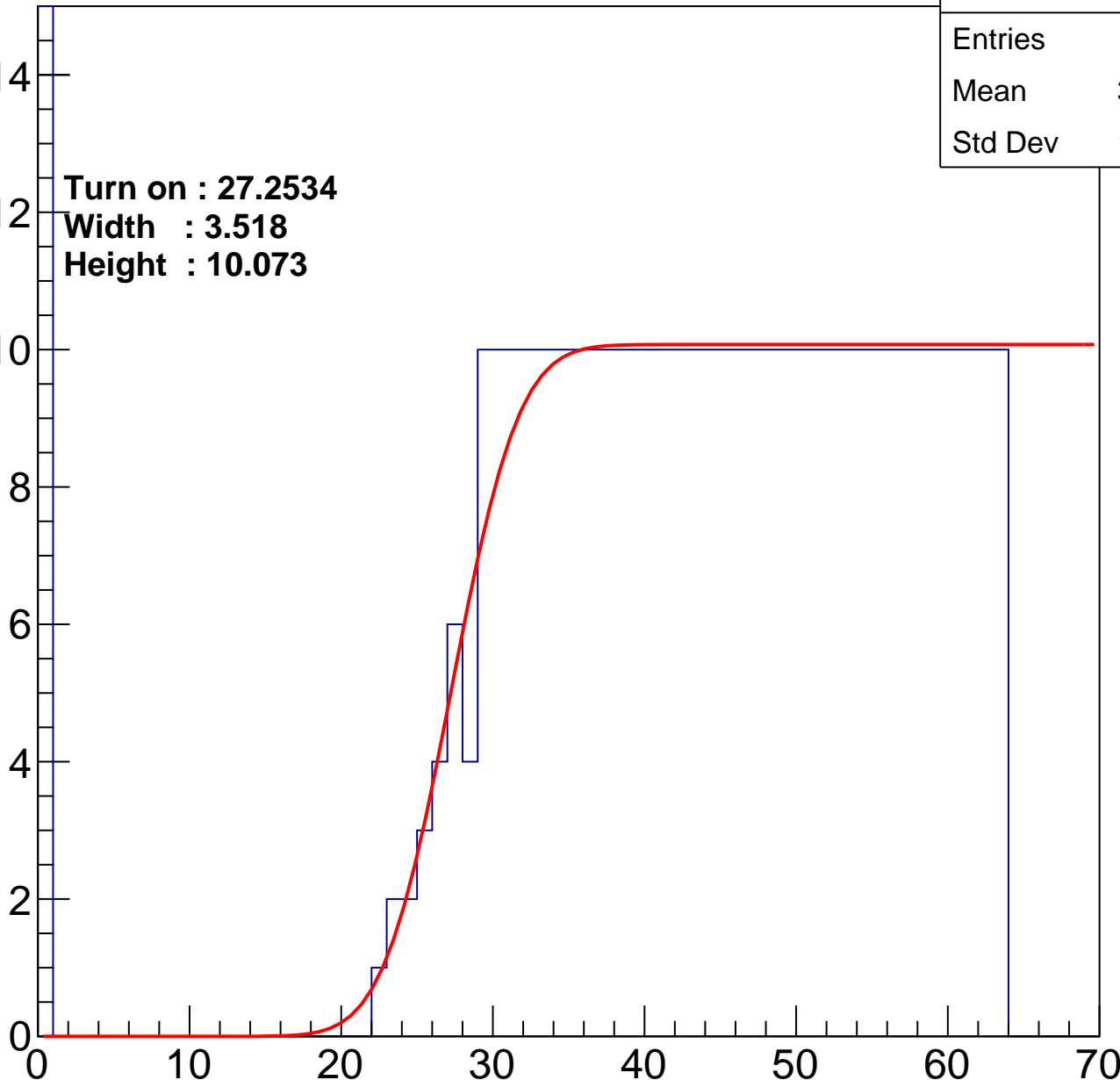
Width : 3.518

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch126

calib_packv5_041523_1651.root, FC#0, port C2

Entries	461
Mean	37.62
Std Dev	18.33

Turn on : 23.9708

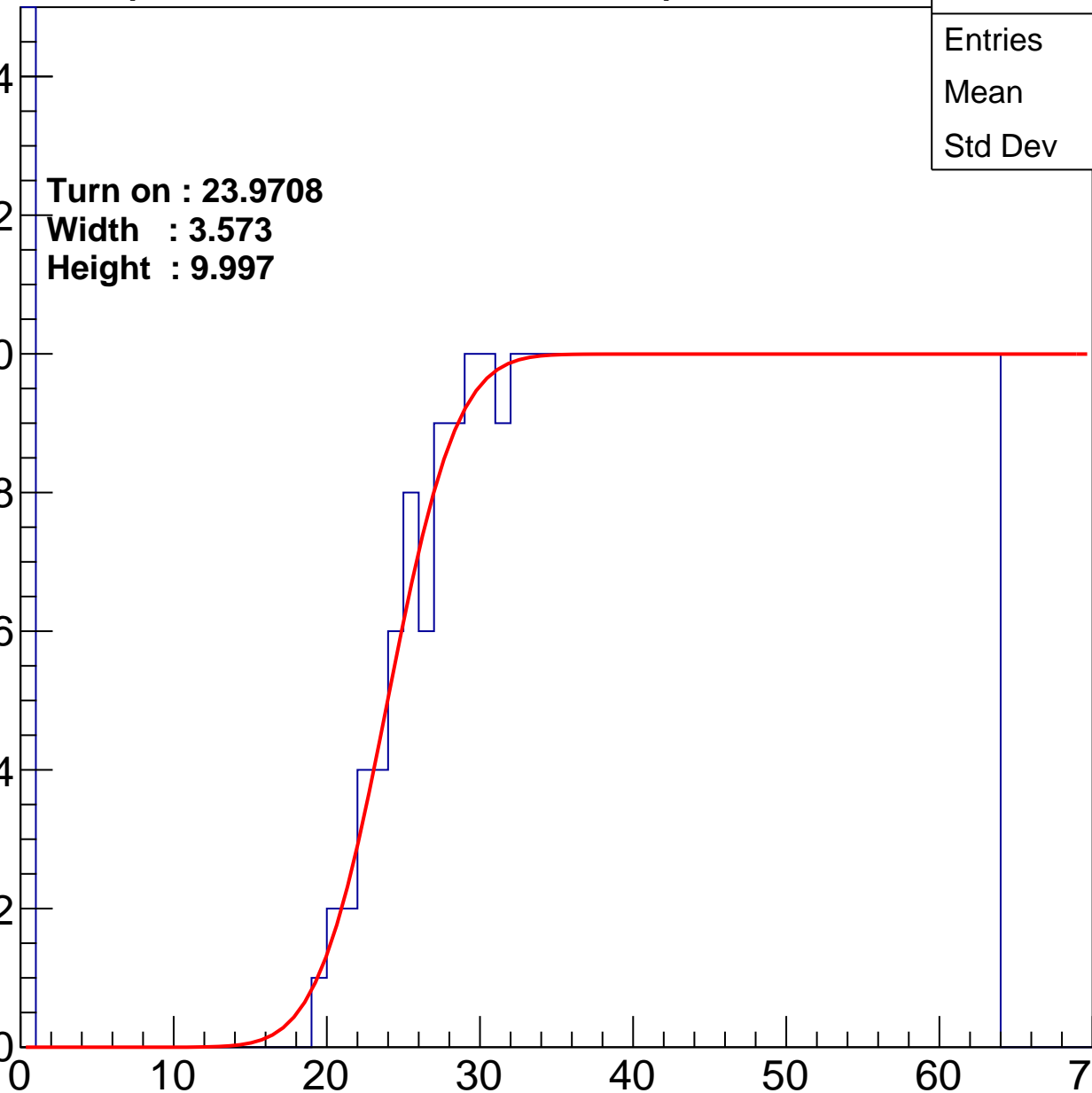
Width : 3.573

Height : 9.997

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch127

calib_packv5_041523_1651.root, FC#0, port C2

Entries	465
Mean	37.53
Std Dev	18.28

Turn on : 23.3330

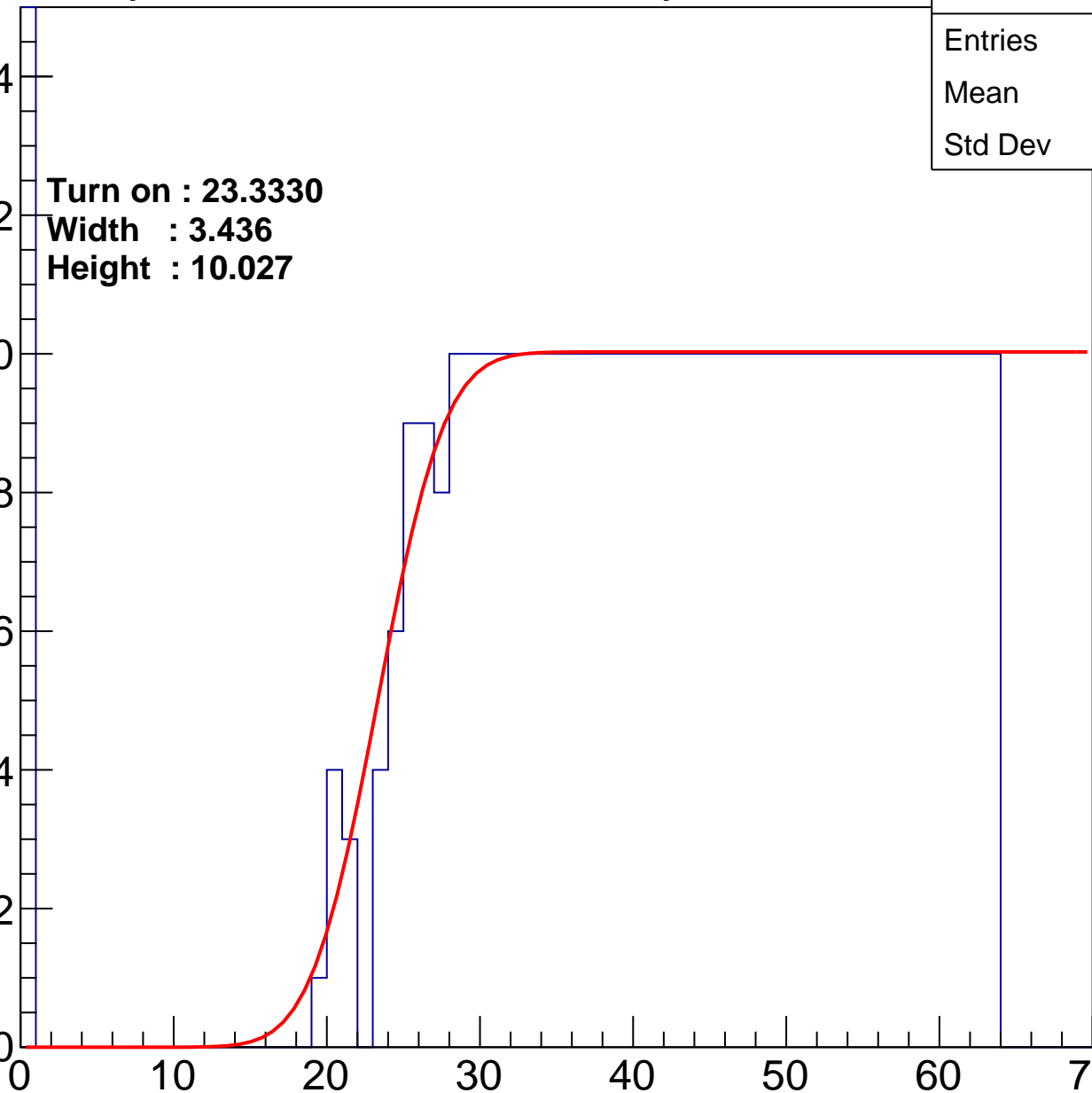
Width : 3.436

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U19-ch127

calib_packv5_041523_1651.root, FC#0, port C2

Entries	465
Mean	37.53
Std Dev	18.28

Turn on : 23.3330

Width : 3.436

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl

