

B1L102S, U1-ch0

calib_packv5_042523_0143.root, FC#11, port A2

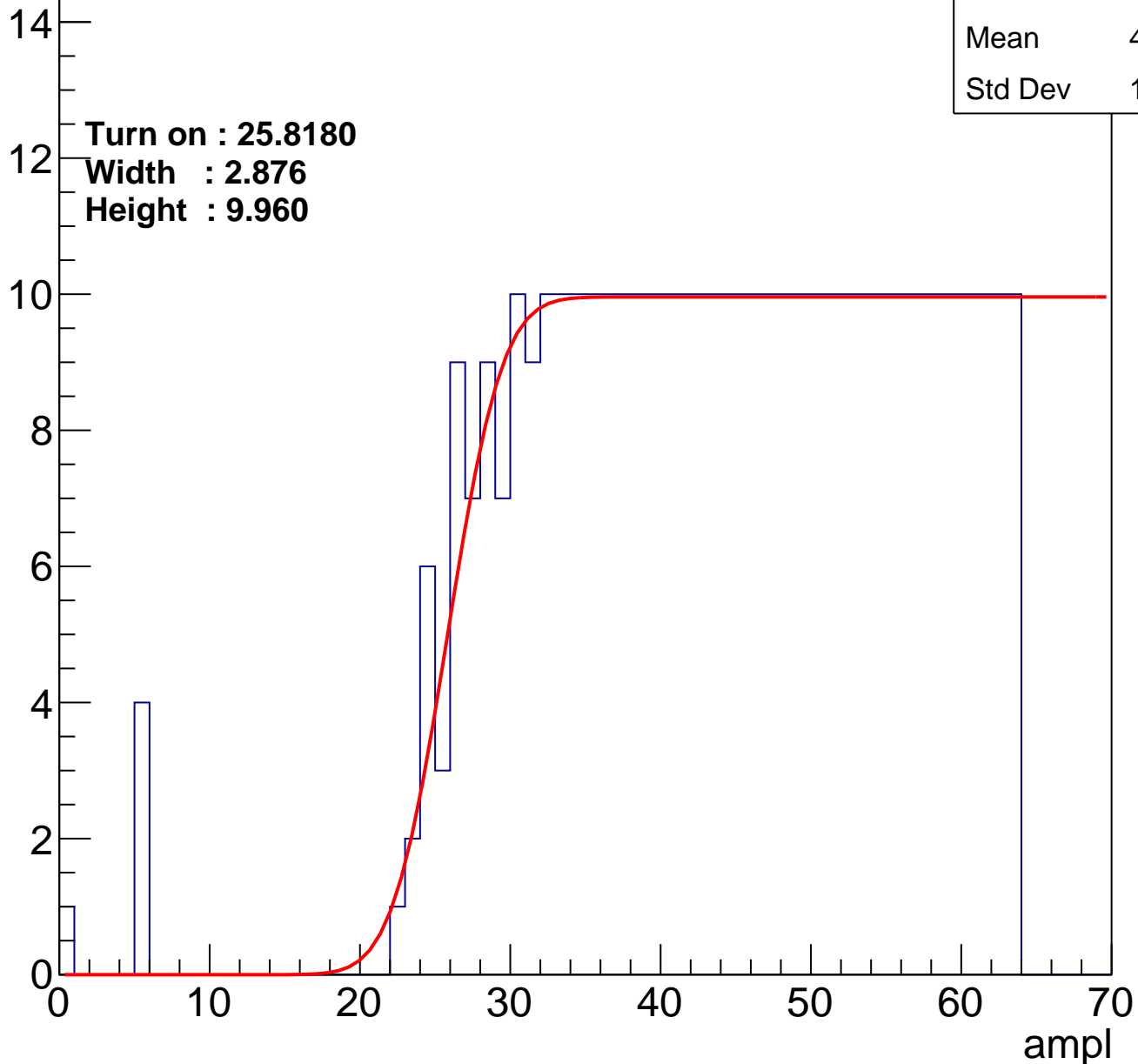
Entries	388
Mean	43.72
Std Dev	12.05

Turn on : 25.8180

Width : 2.876

Height : 9.960

Entry



B1L102S, U1-ch1

calib_packv5_042523_0143.root, FC#11, port A2

Entries	383
Mean	43.89
Std Dev	12.16

Turn on : 26.4361

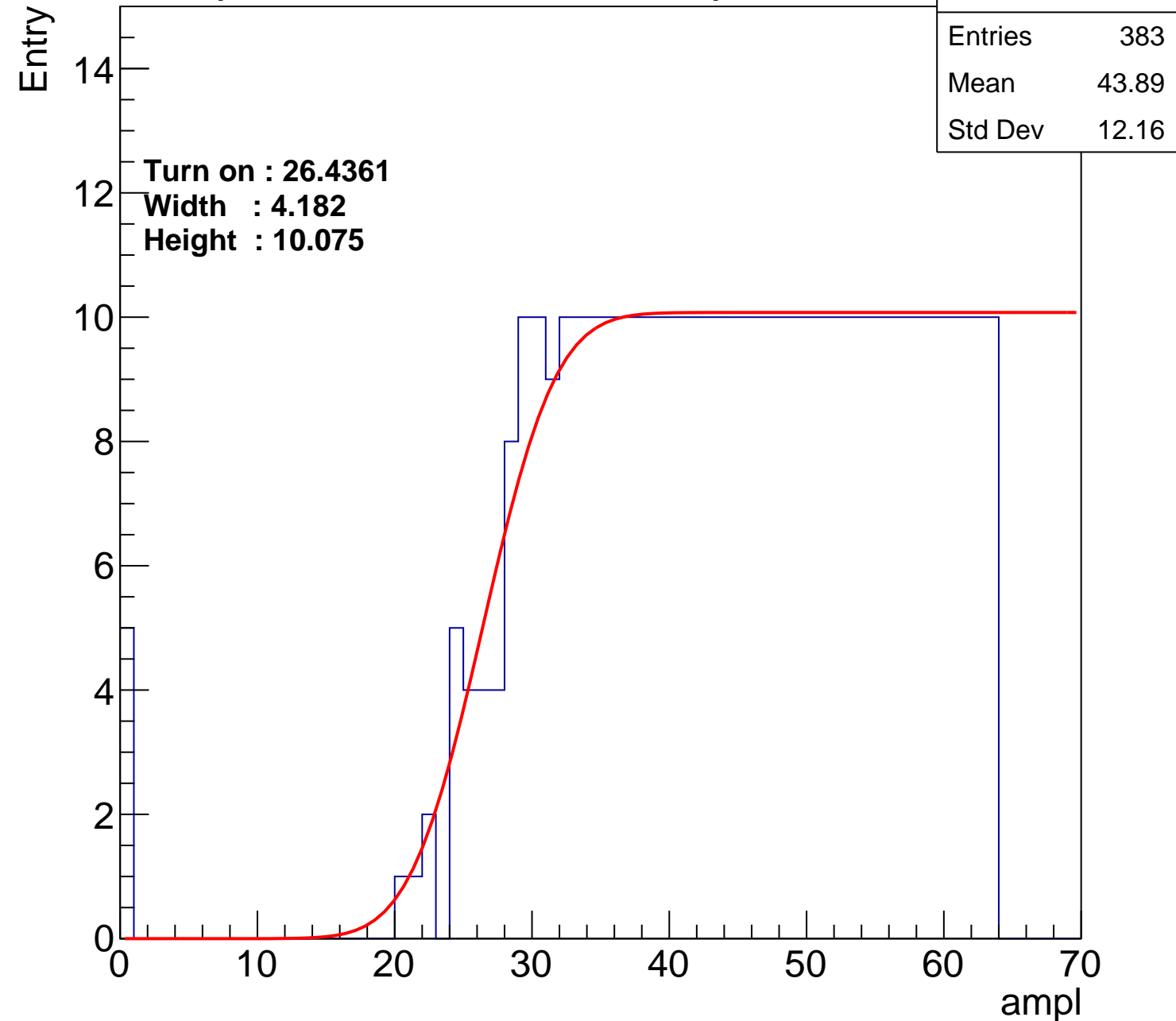
Width : 4.182

Height : 10.075

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch2

calib_packv5_042523_0143.root, FC#11, port A2

Entries	396
Mean	43.35
Std Dev	12.19

Turn on : 25.6374

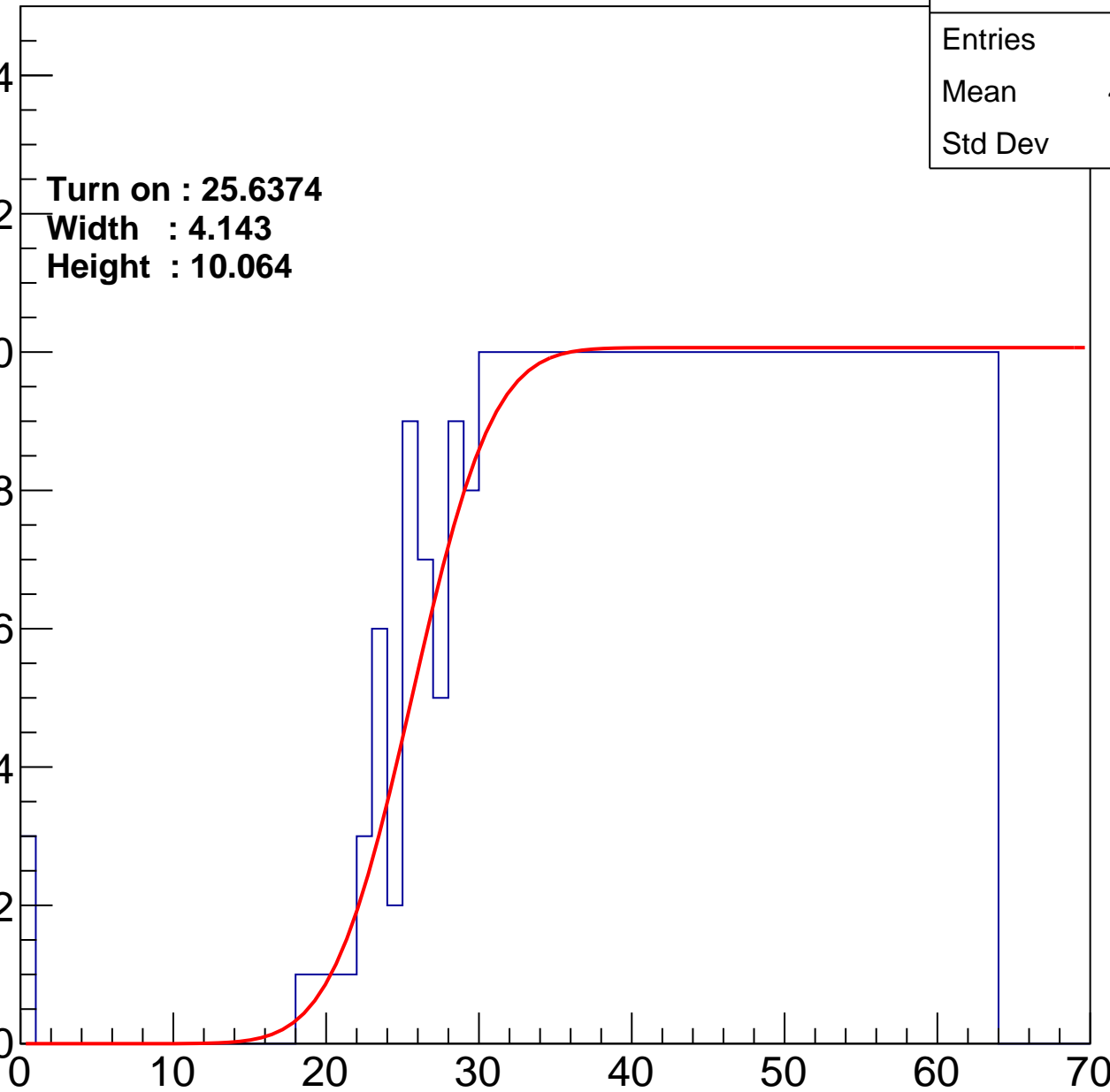
Width : 4.143

Height : 10.064

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch3

calib_packv5_042523_0143.root, FC#11, port A2

Entries	379
Mean	44.28
Std Dev	11.62

Turn on : 26.7134

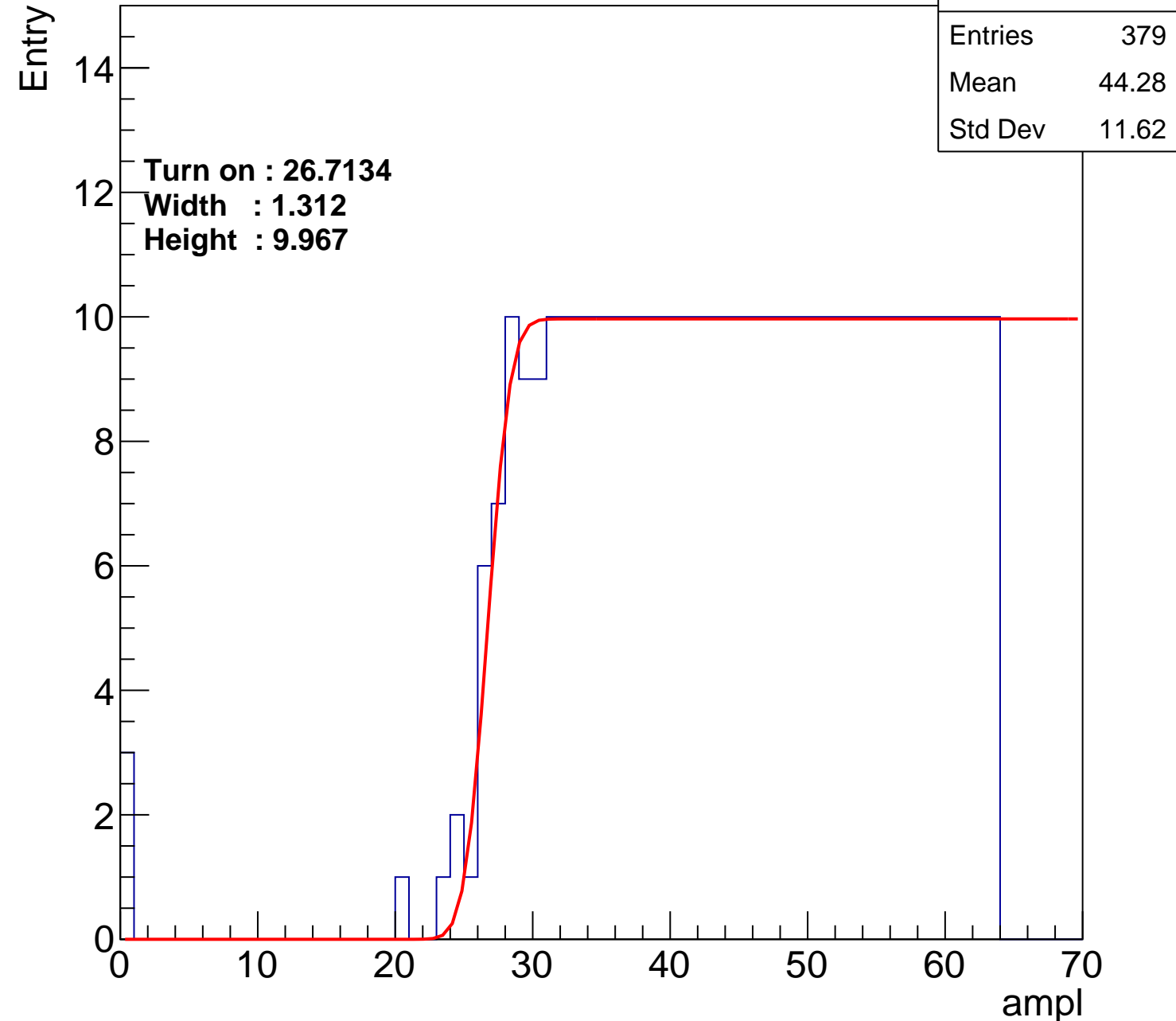
Width : 1.312

Height : 9.967

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch4

calib_packv5_042523_0143.root, FC#11, port A2

Entries	403
Mean	43.03
Std Dev	12.37

Turn on : 24.0752

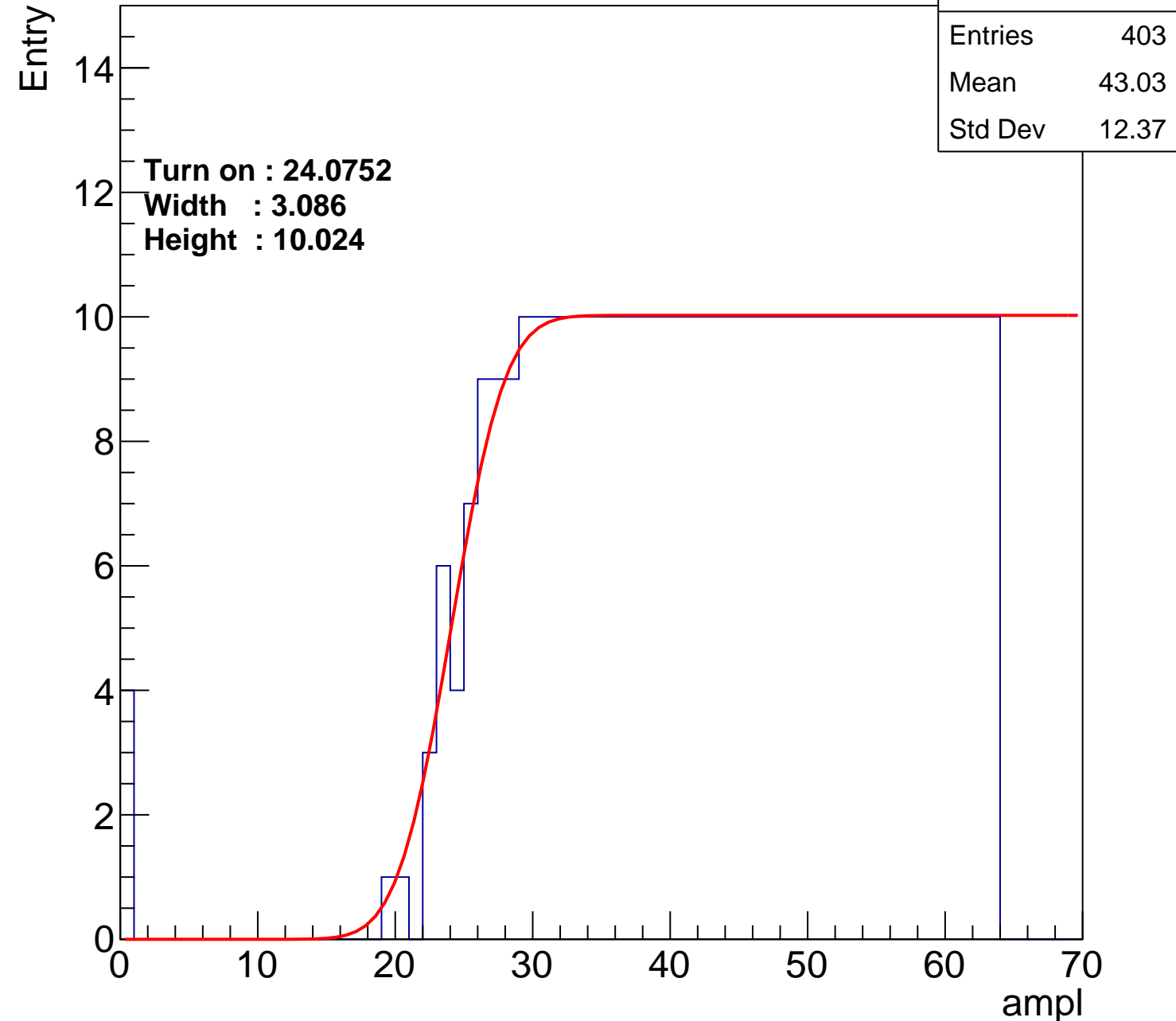
Width : 3.086

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch5

calib_packv5_042523_0143.root, FC#11, port A2

Entries	395
Mean	43.45
Std Dev	12.09

Turn on : 25.2609

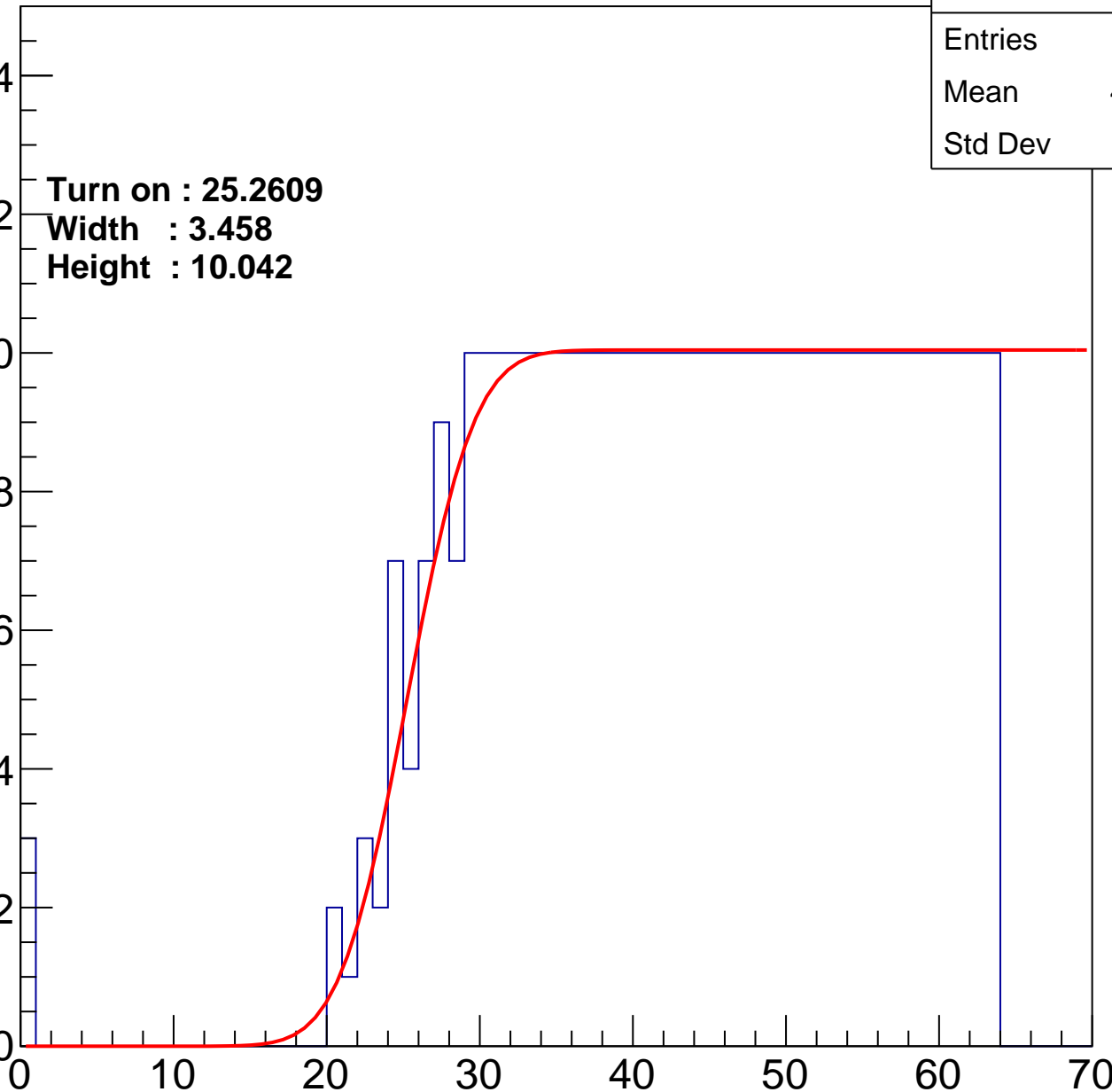
Width : 3.458

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch6

calib_packv5_042523_0143.root, FC#11, port A2

Entries	391
Mean	43.73
Std Dev	11.78

Turn on : 25.3879

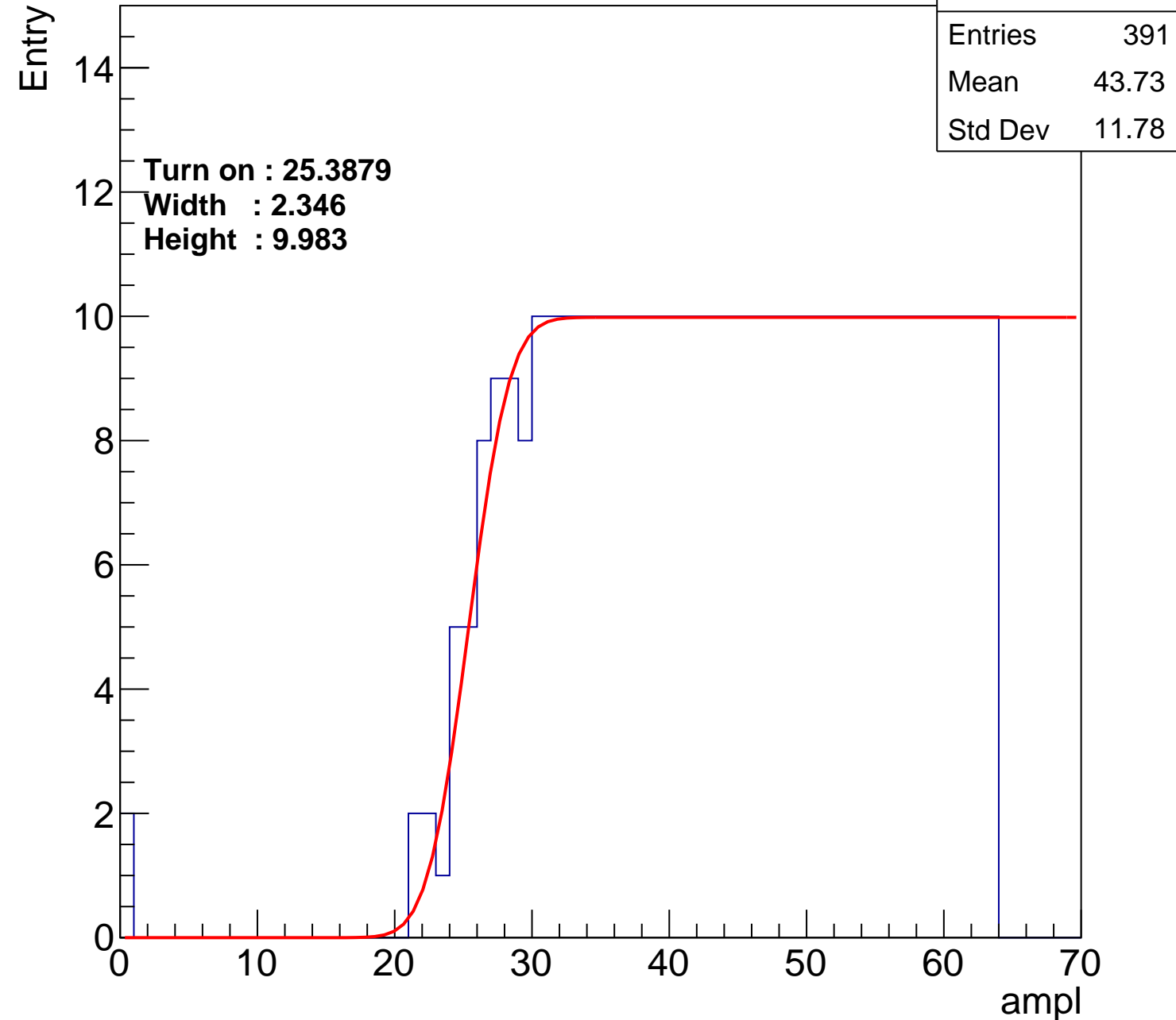
Width : 2.346

Height : 9.983

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch7

calib_packv5_042523_0143.root, FC#11, port A2

Entries	389
Mean	43.83
Std Dev	11.73

Turn on : 25.8685

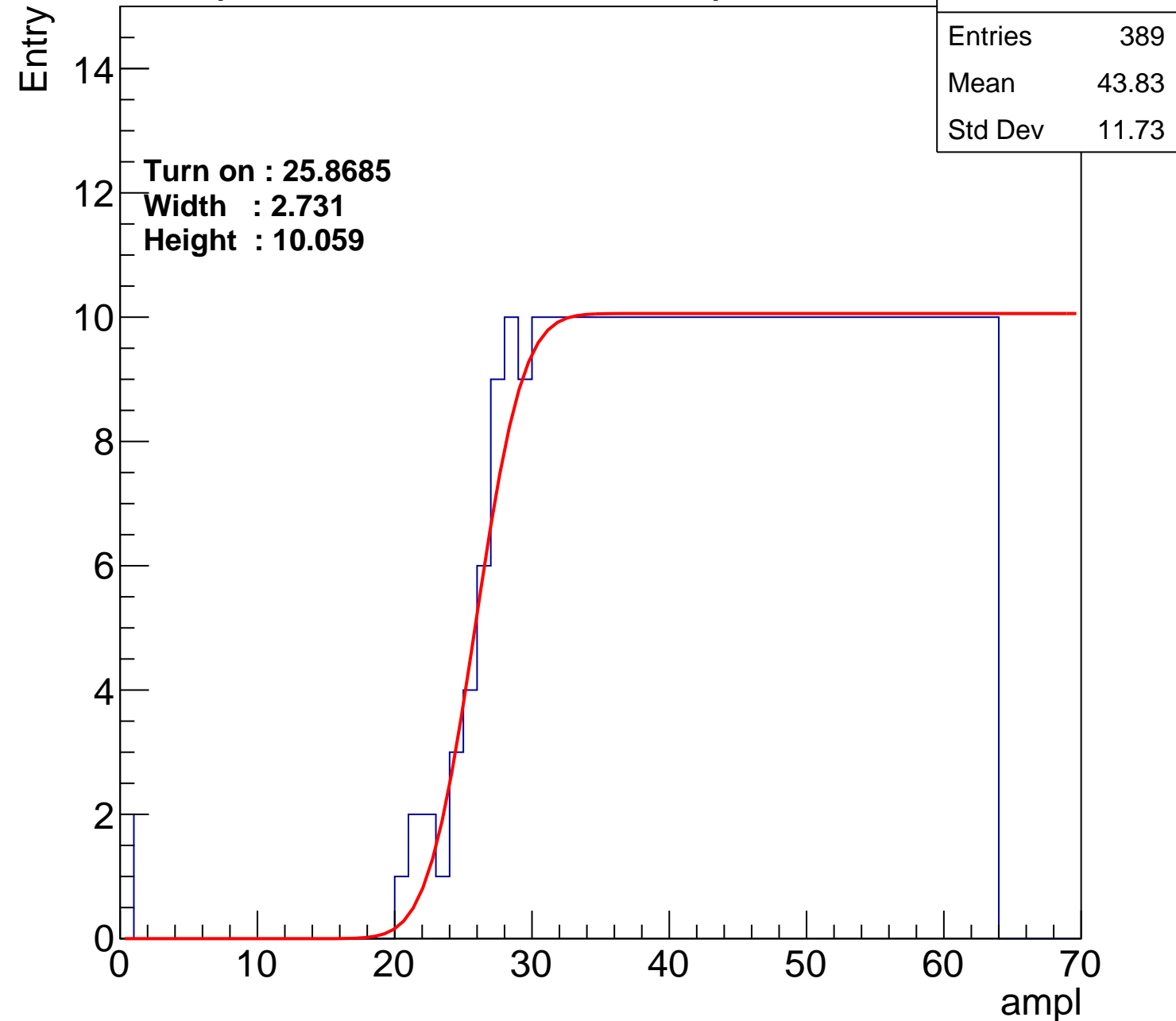
Width : 2.731

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch8

calib_packv5_042523_0143.root, FC#11, port A2

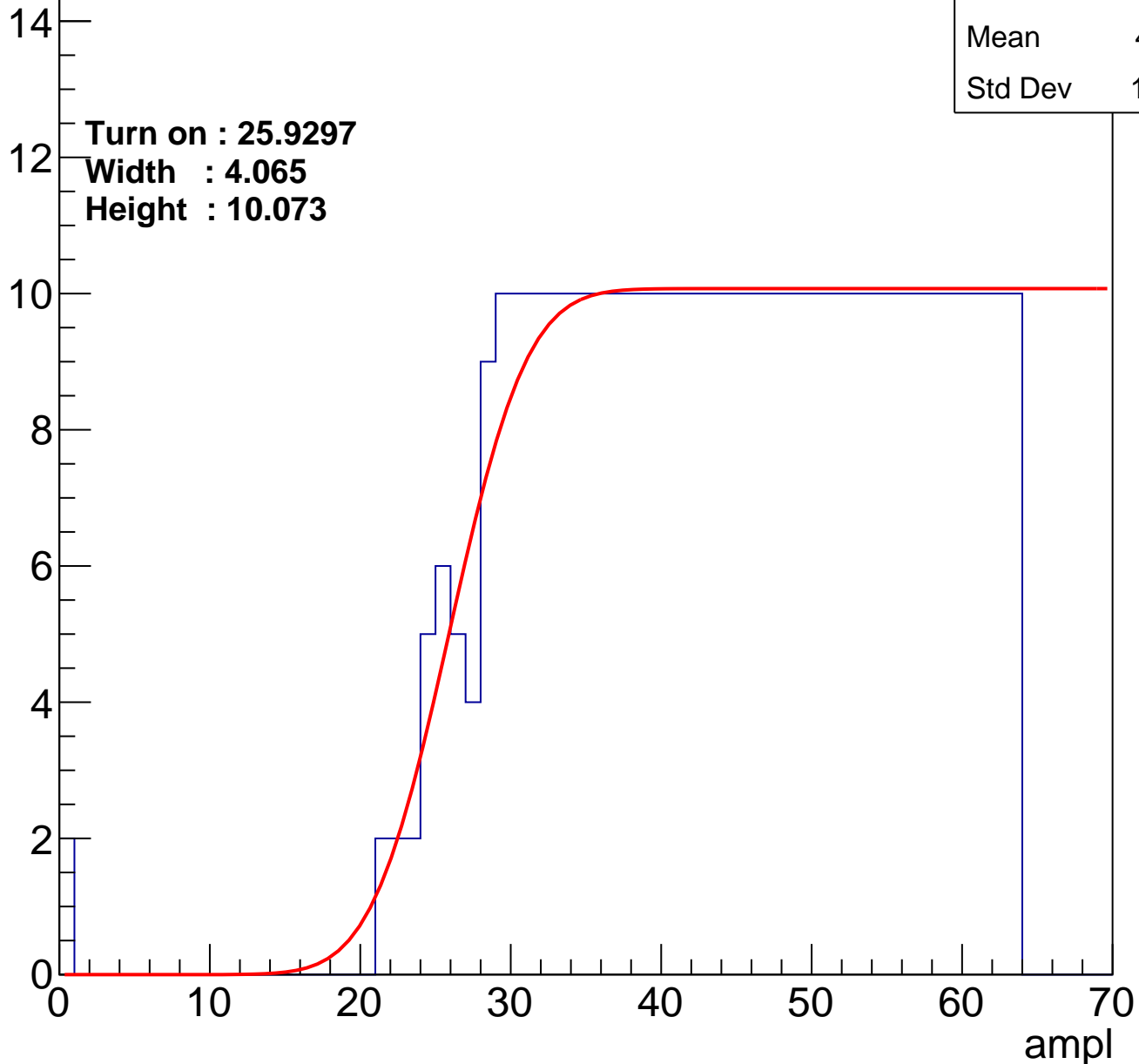
Entries	387
Mean	43.91
Std Dev	11.72

Turn on : 25.9297

Width : 4.065

Height : 10.073

Entry



B1L102S, U1-ch9

calib_packv5_042523_0143.root, FC#11, port A2

Entries	394
Mean	43.41
Std Dev	12.25

Turn on : 25.0155

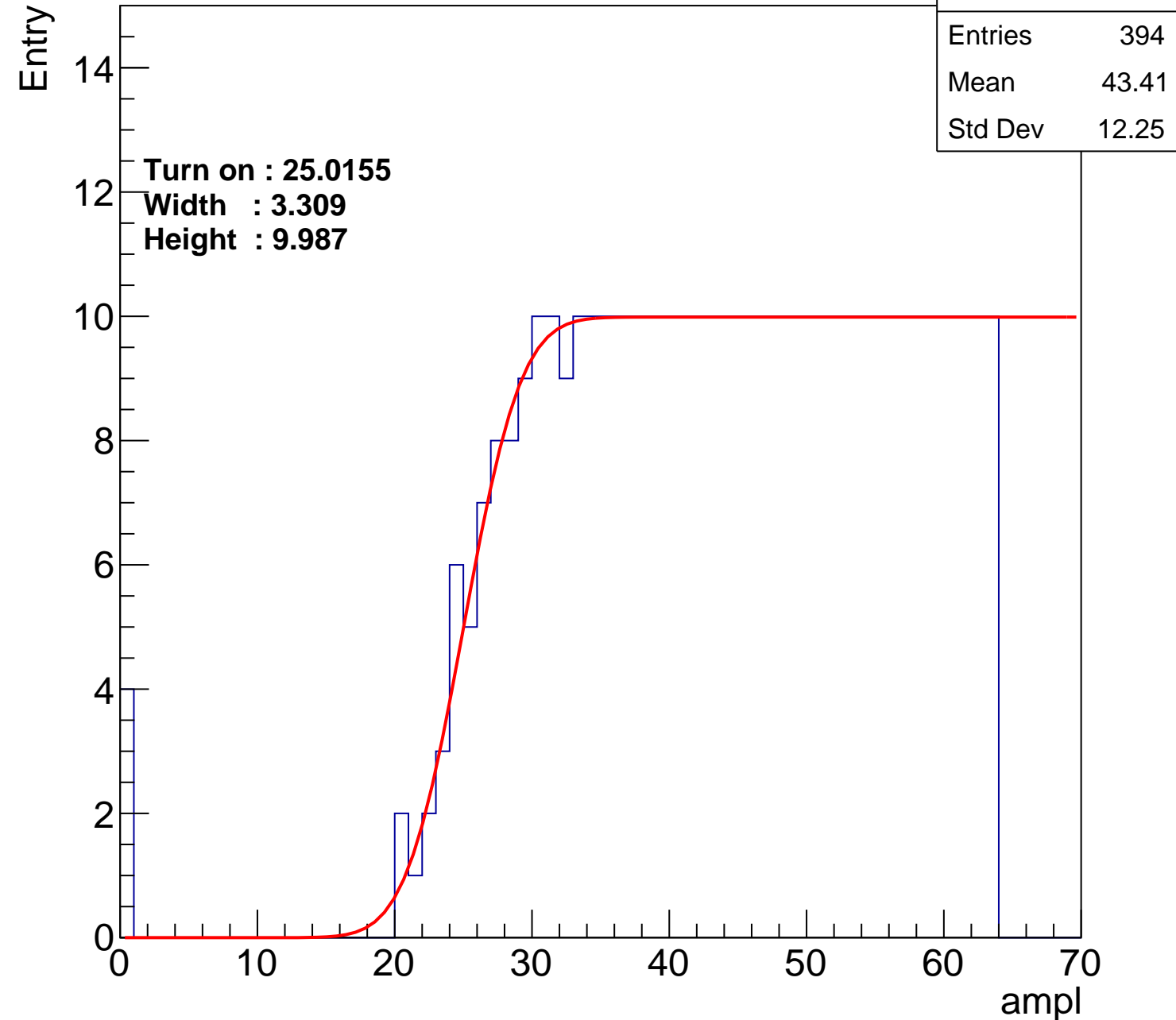
Width : 3.309

Height : 9.987

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch10

calib_packv5_042523_0143.root, FC#11, port A2

Entries	383
Mean	44.08
Std Dev	11.65

Turn on : 26.4679

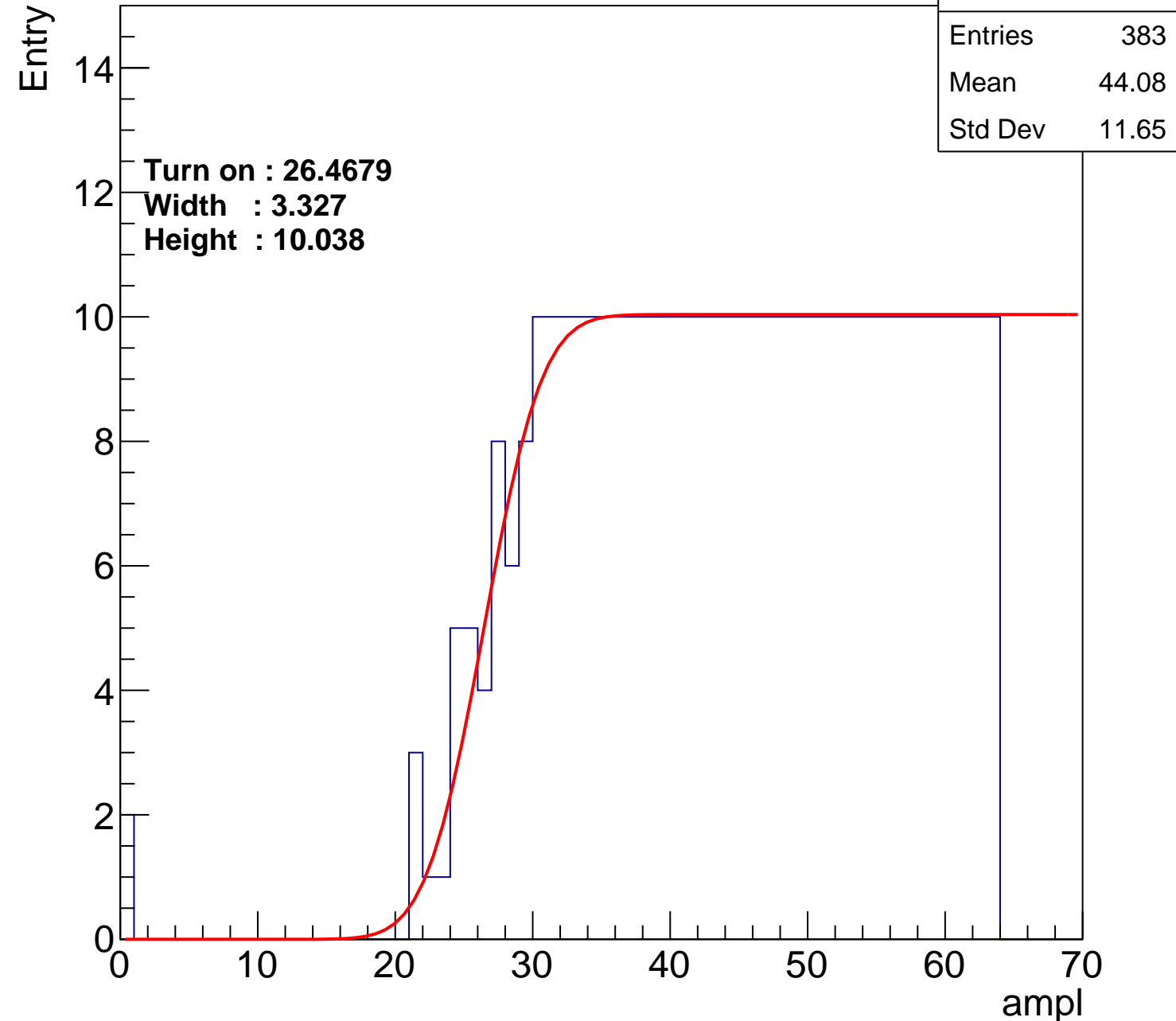
Width : 3.327

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch11

calib_packv5_042523_0143.root, FC#11, port A2

Entries	390
Mean	43.87
Std Dev	11.55

Turn on : 25.5455

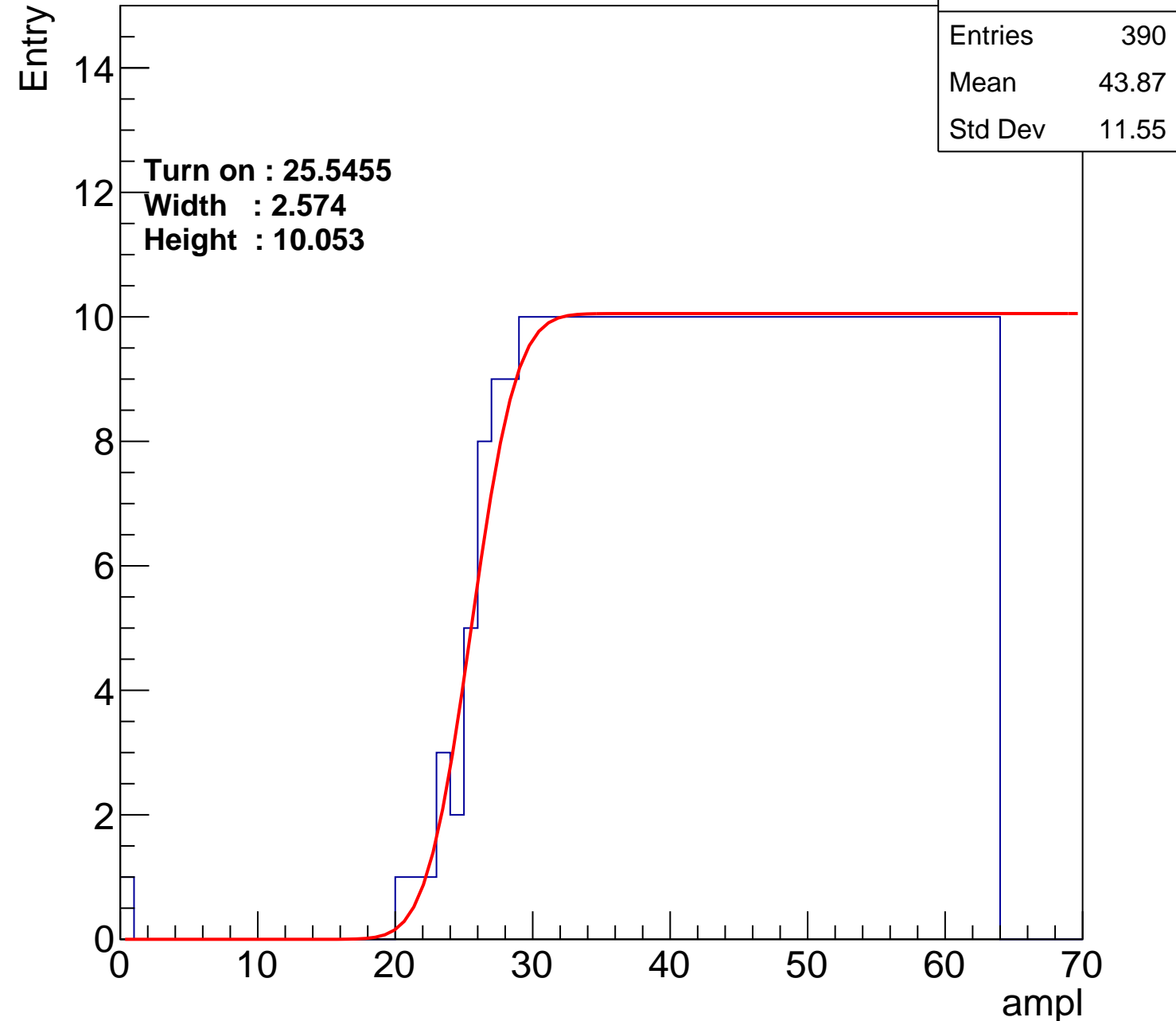
Width : 2.574

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch12

calib_packv5_042523_0143.root, FC#11, port A2

Entries	391
Mean	43.64
Std Dev	11.98

Turn on : 25.1456

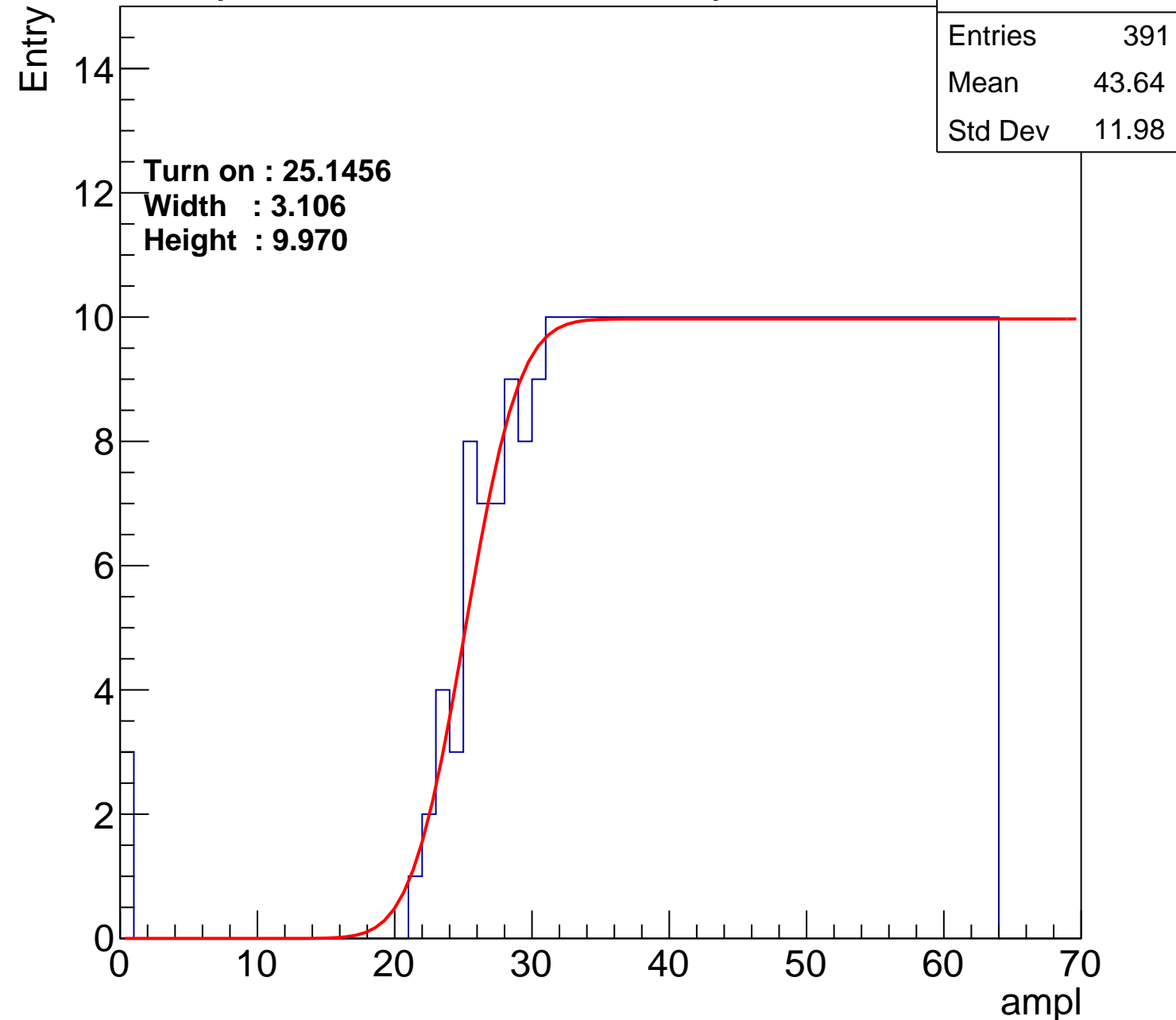
Width : 3.106

Height : 9.970

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch13

calib_packv5_042523_0143.root, FC#11, port A2

Entries	373
Mean	44.62
Std Dev	11.32

Turn on : 27.3204

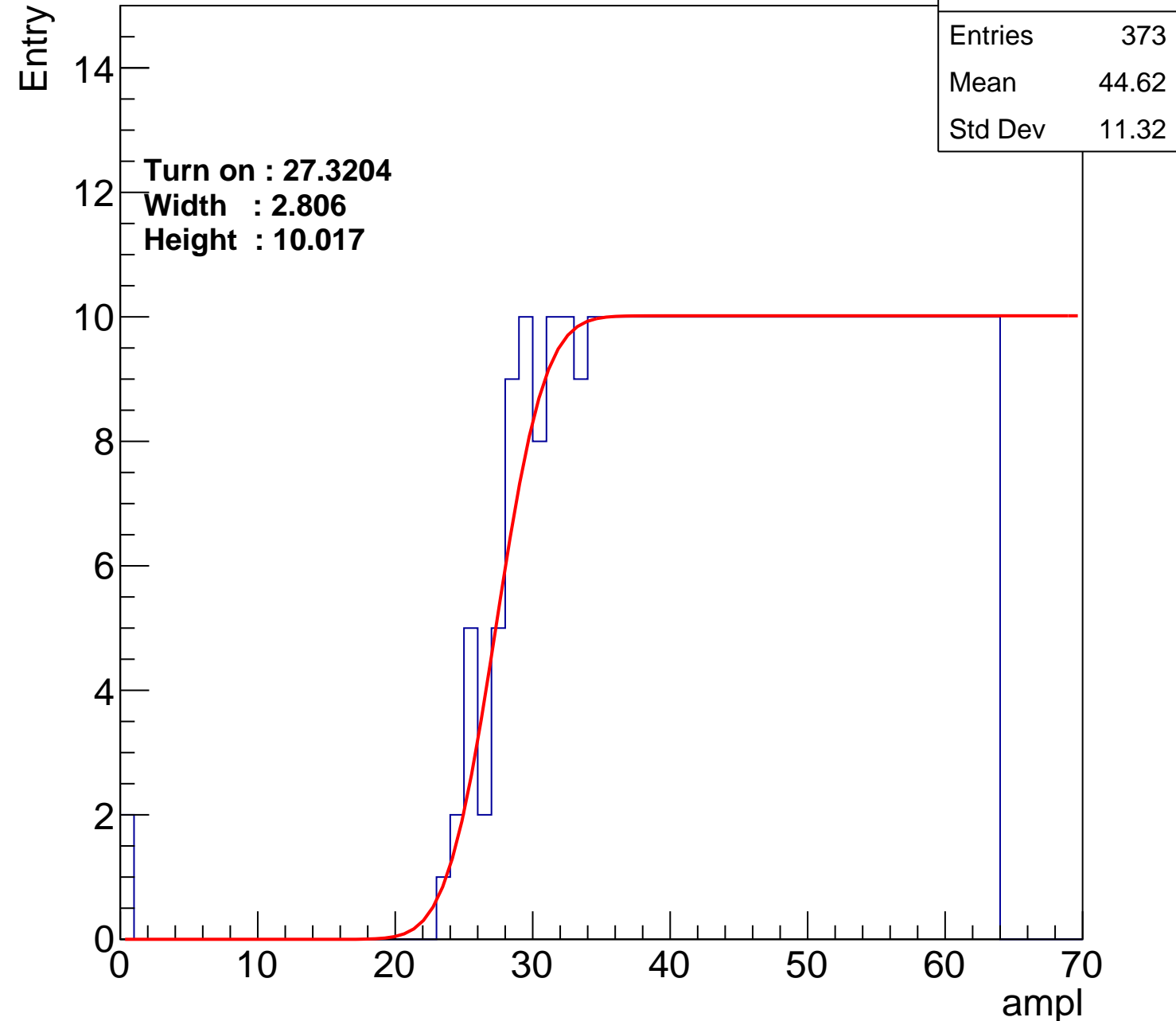
Width : 2.806

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch14

calib_packv5_042523_0143.root, FC#11, port A2

Entries	393
Mean	43.64
Std Dev	11.76

Turn on : 25.4057

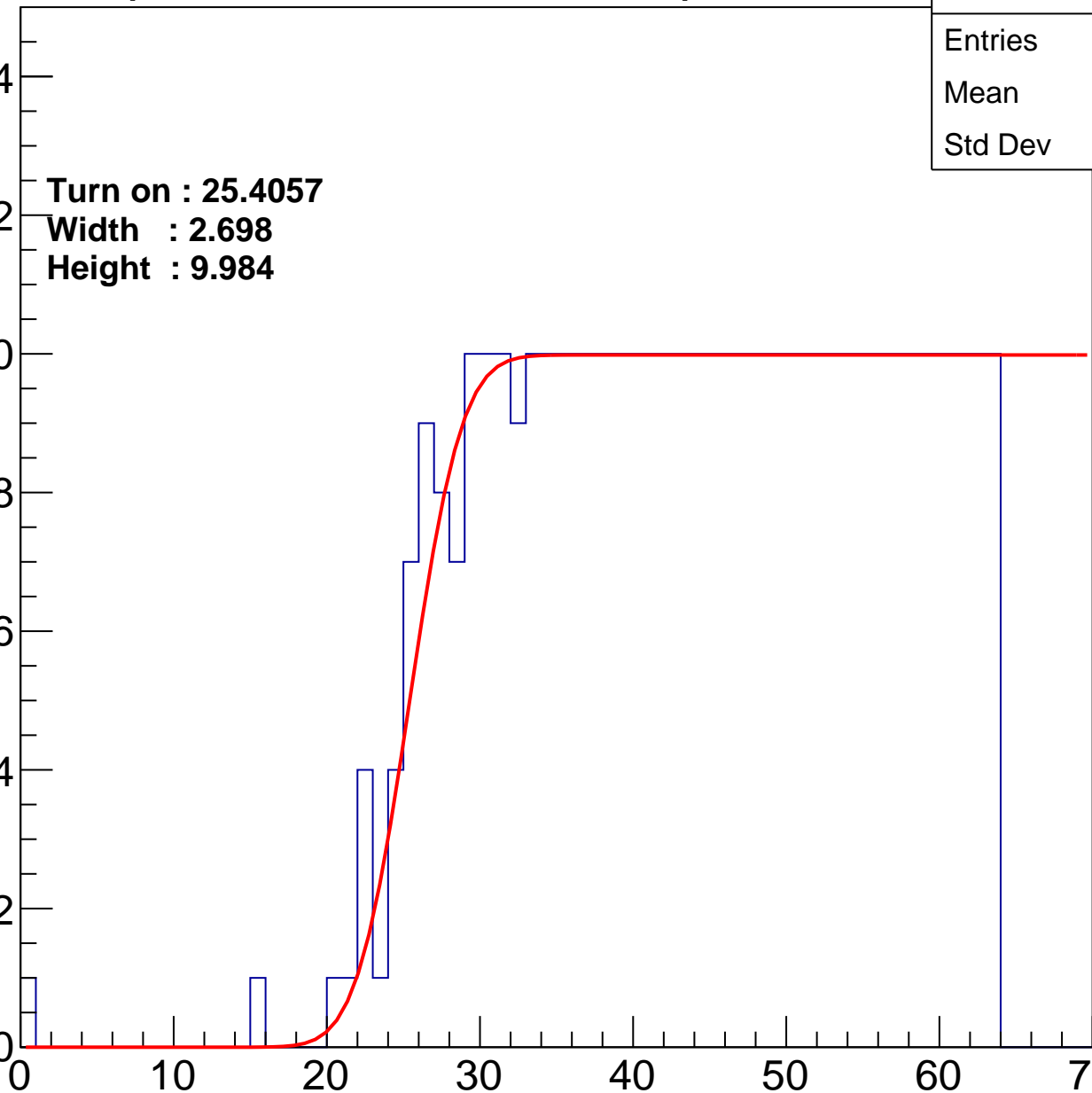
Width : 2.698

Height : 9.984

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch15

calib_packv5_042523_0143.root, FC#11, port A2

Entries	387
Mean	43.79
Std Dev	12.03

Turn on : 26.4780

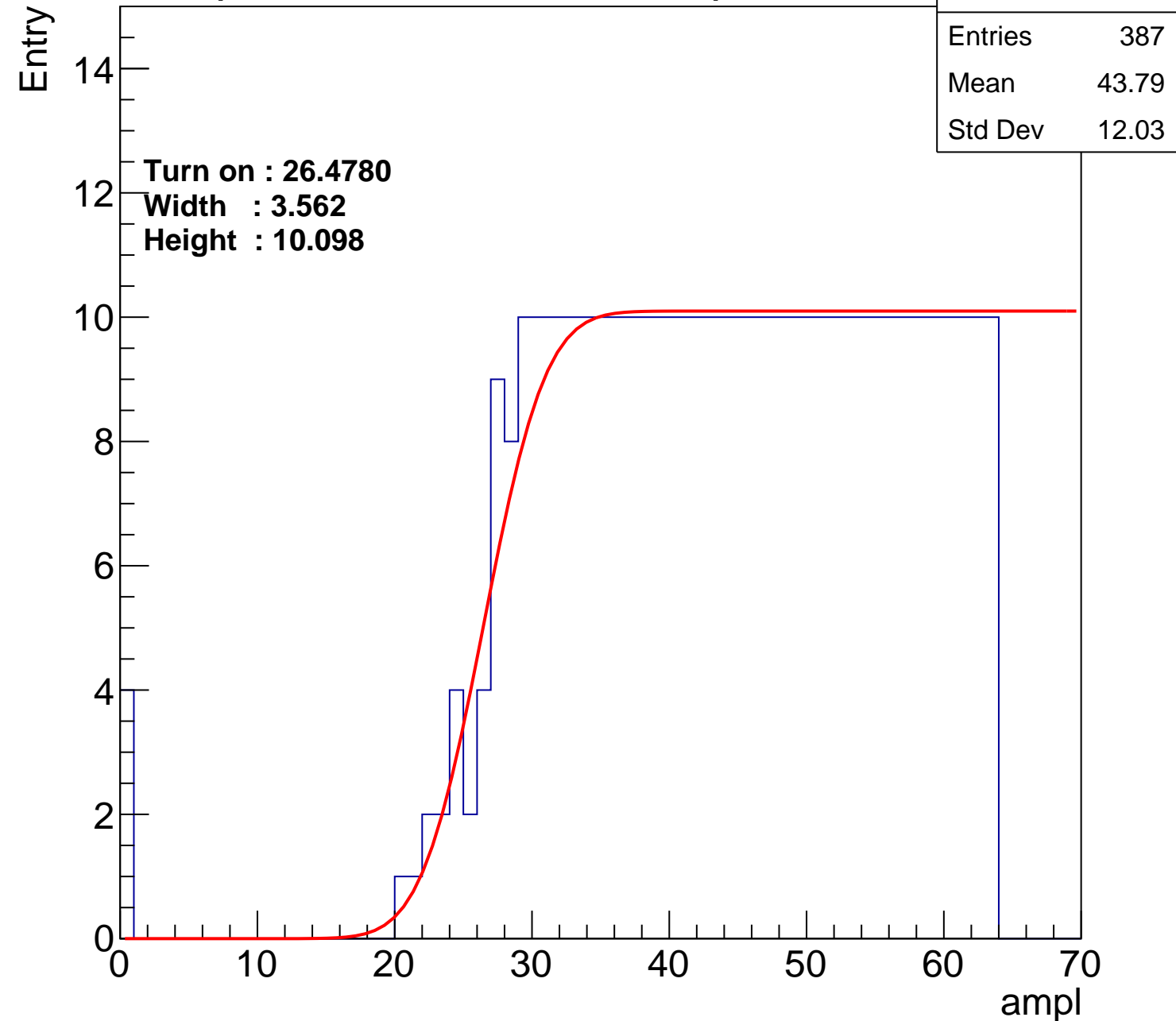
Width : 3.562

Height : 10.098

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch16

calib_packv5_042523_0143.root, FC#11, port A2

Entries	384
Mean	43.91
Std Dev	12

Turn on : 26.2195

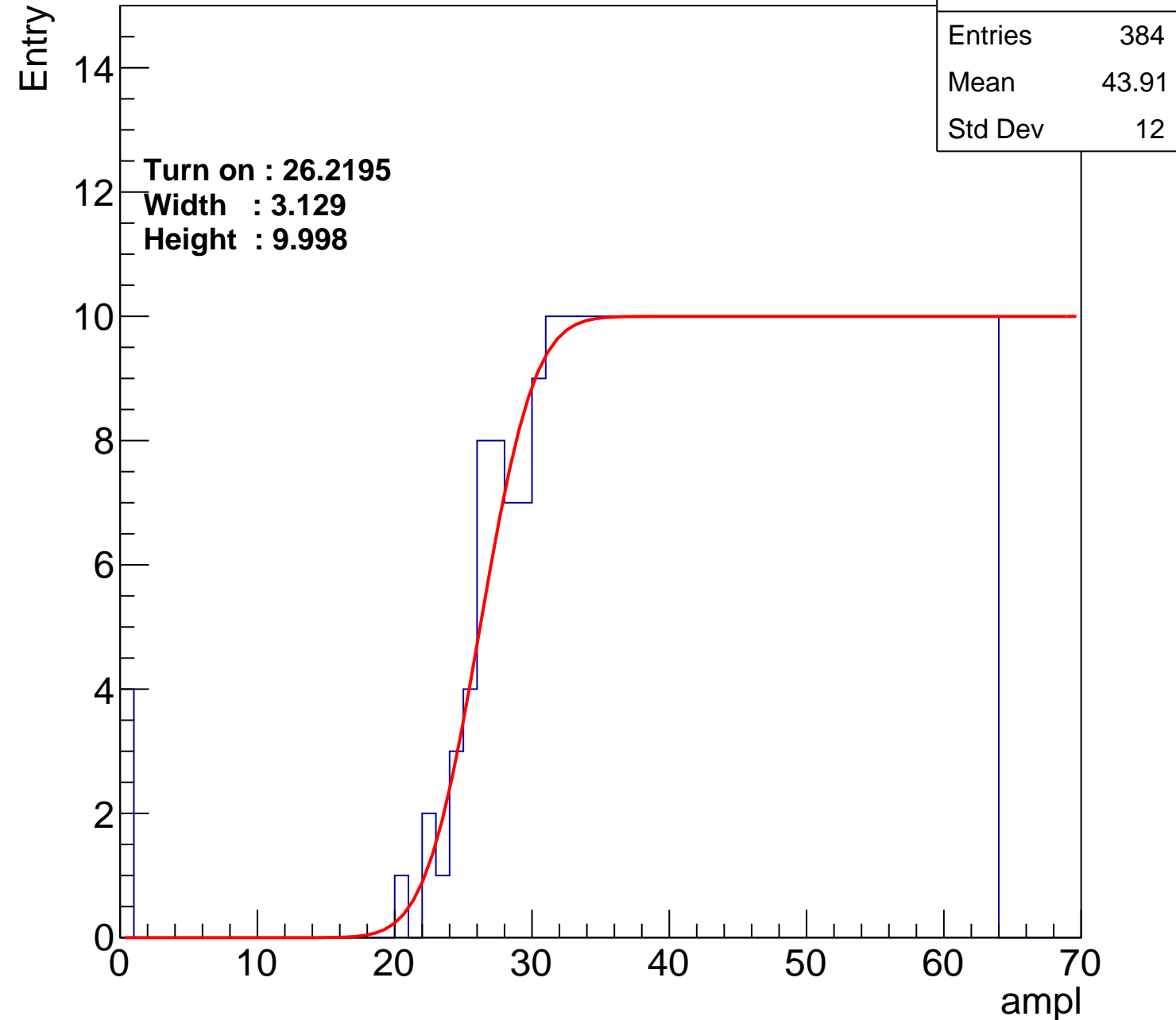
Width : 3.129

Height : 9.998

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch17

calib_packv5_042523_0143.root, FC#11, port A2

Entries	400
Mean	43.34
Std Dev	11.87

Turn on : 24.7523

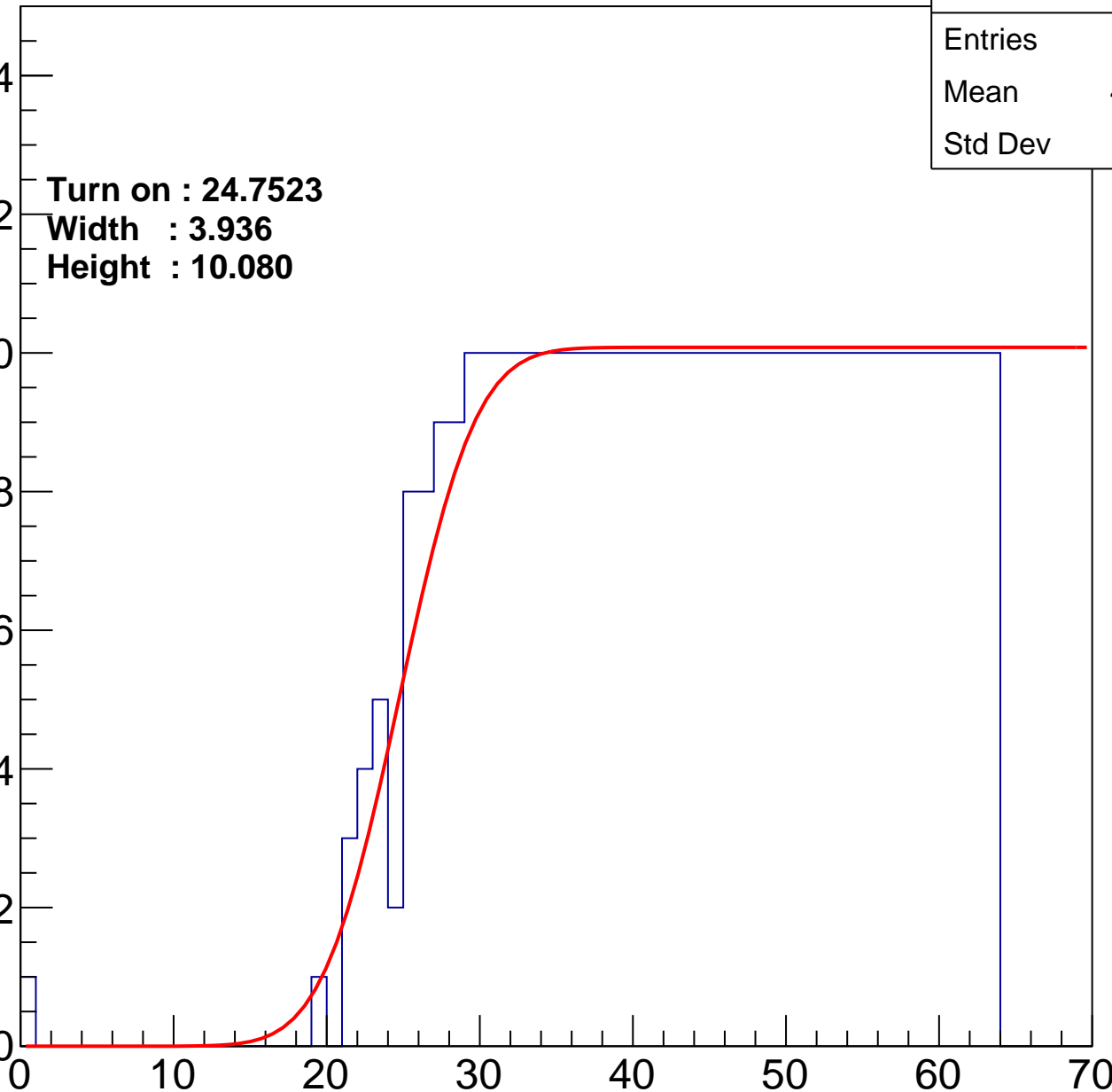
Width : 3.936

Height : 10.080

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch18

calib_packv5_042523_0143.root, FC#11, port A2

Entries	383
Mean	44.04
Std Dev	11.79

Turn on : 26.2827

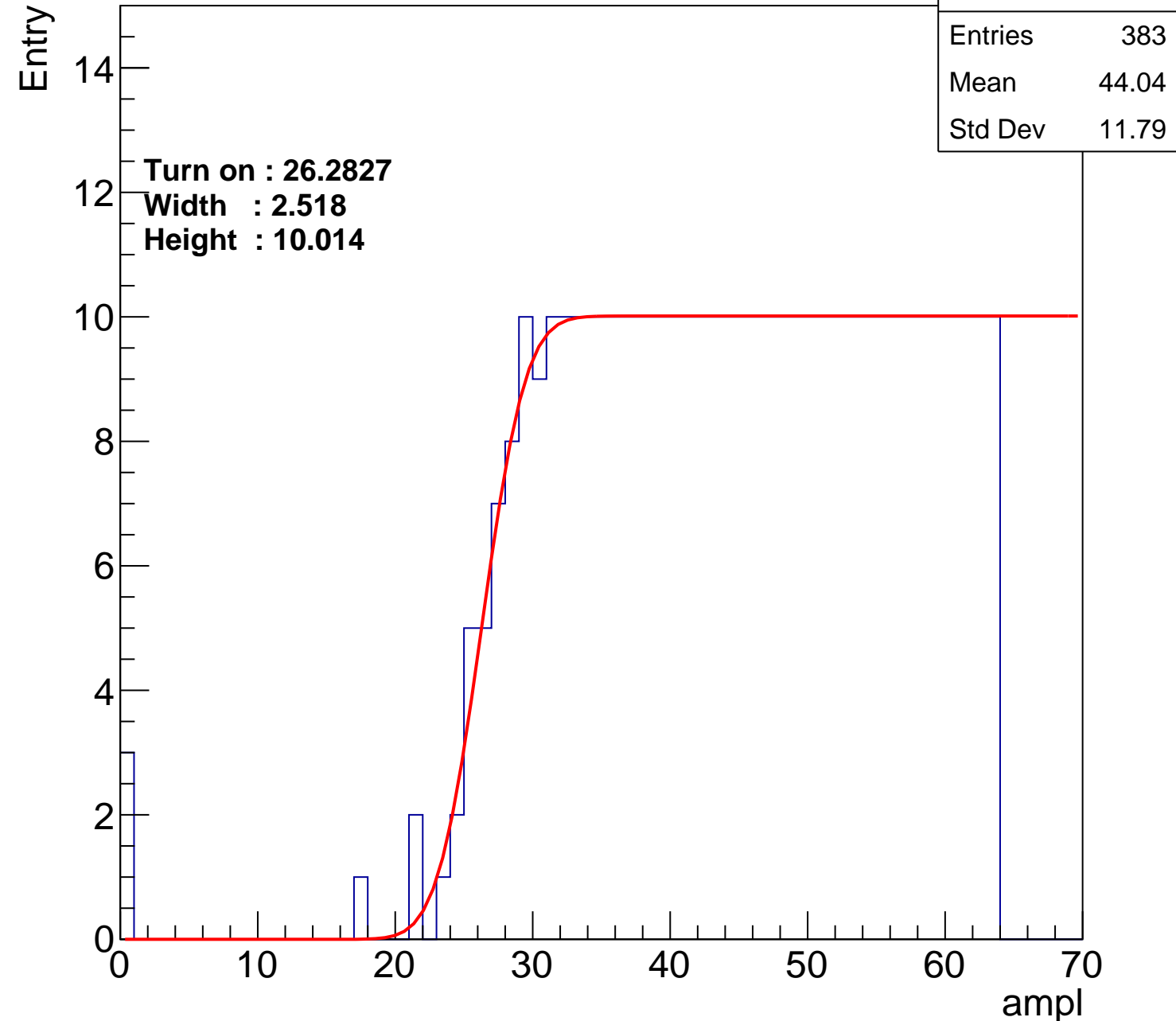
Width : 2.518

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch19

calib_packv5_042523_0143.root, FC#11, port A2

Entries	372
Mean	44.58
Std Dev	11.52

Turn on : 27.7015

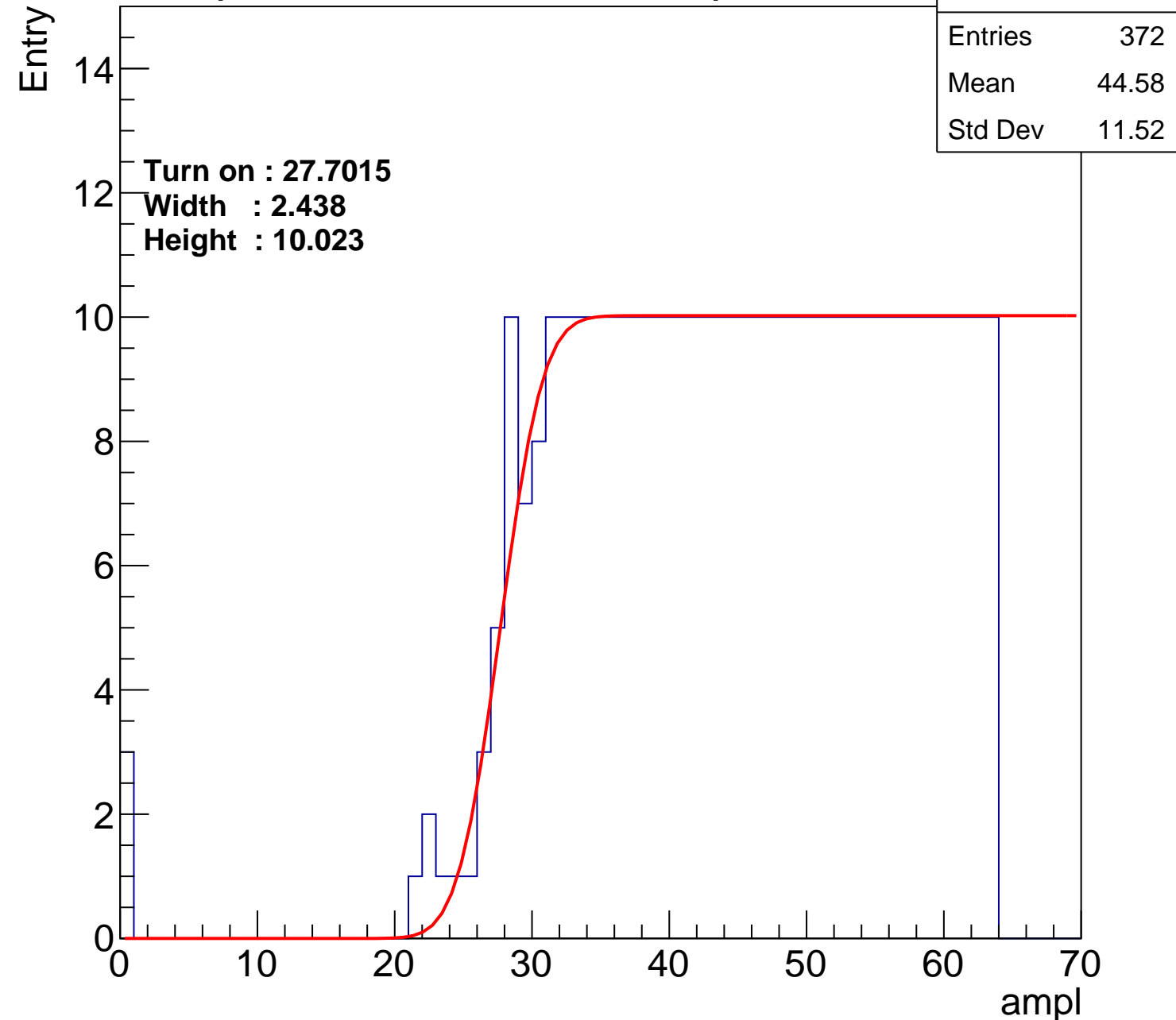
Width : 2.438

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch20

calib_packv5_042523_0143.root, FC#11, port A2

Entries	400
Mean	43.27
Std Dev	12.04

Turn on : 24.4245

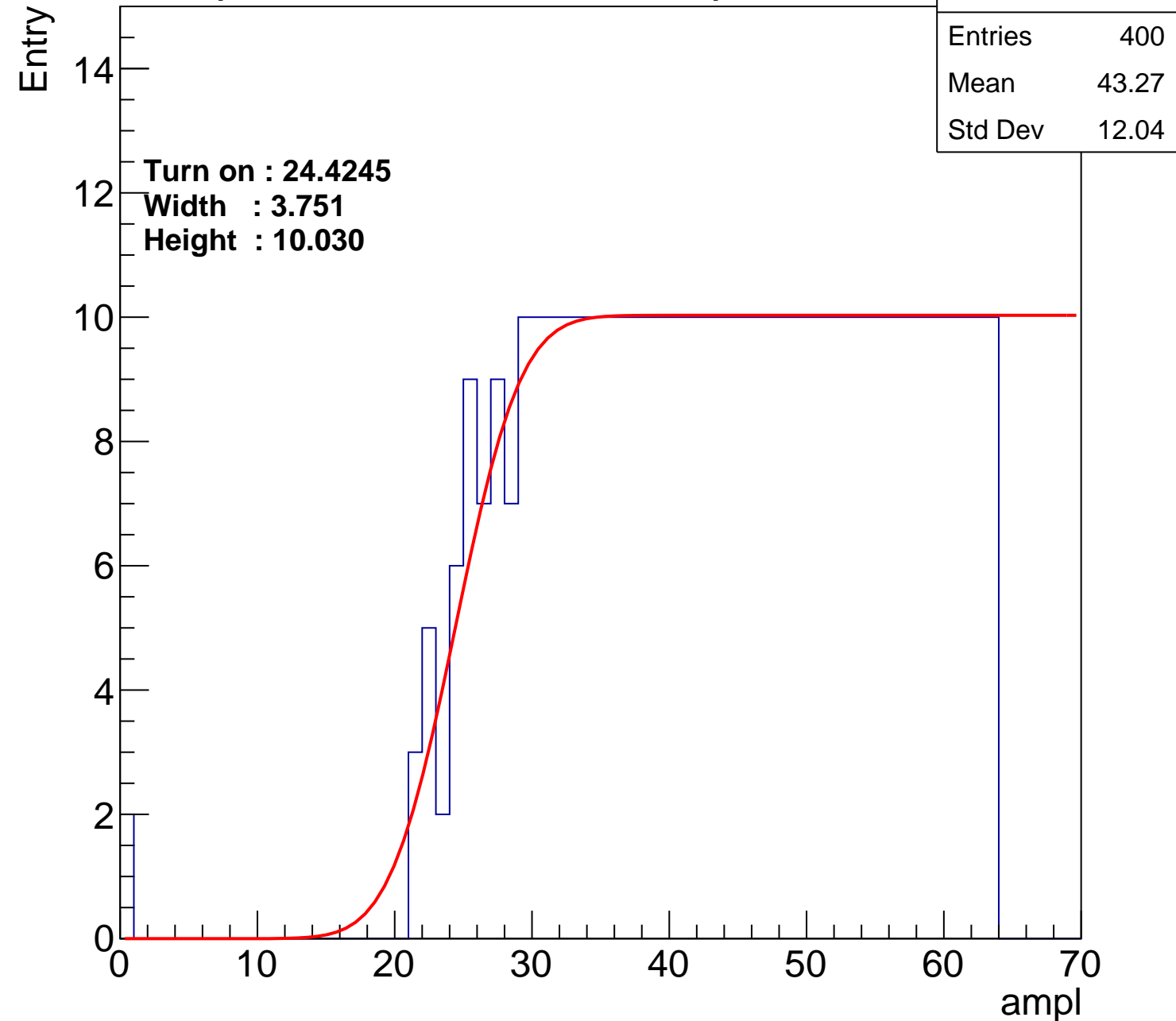
Width : 3.751

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch21

calib_packv5_042523_0143.root, FC#11, port A2

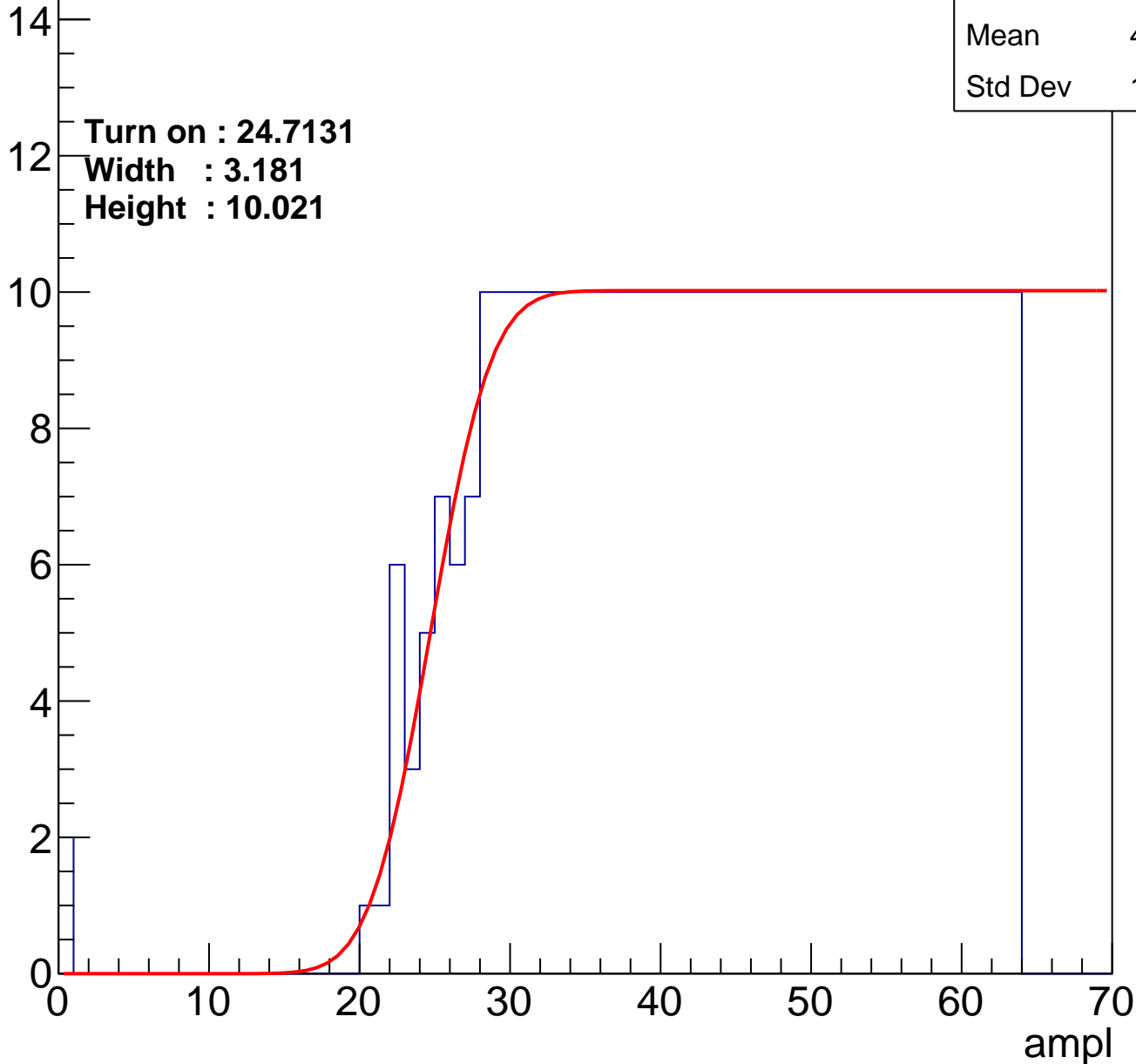
Entries	398
Mean	43.37
Std Dev	11.99

Turn on : 24.7131

Width : 3.181

Height : 10.021

Entry



B1L102S, U1-ch22

calib_packv5_042523_0143.root, FC#11, port A2

Entries	358
Mean	45.37
Std Dev	10.82

Turn on : 28.9375

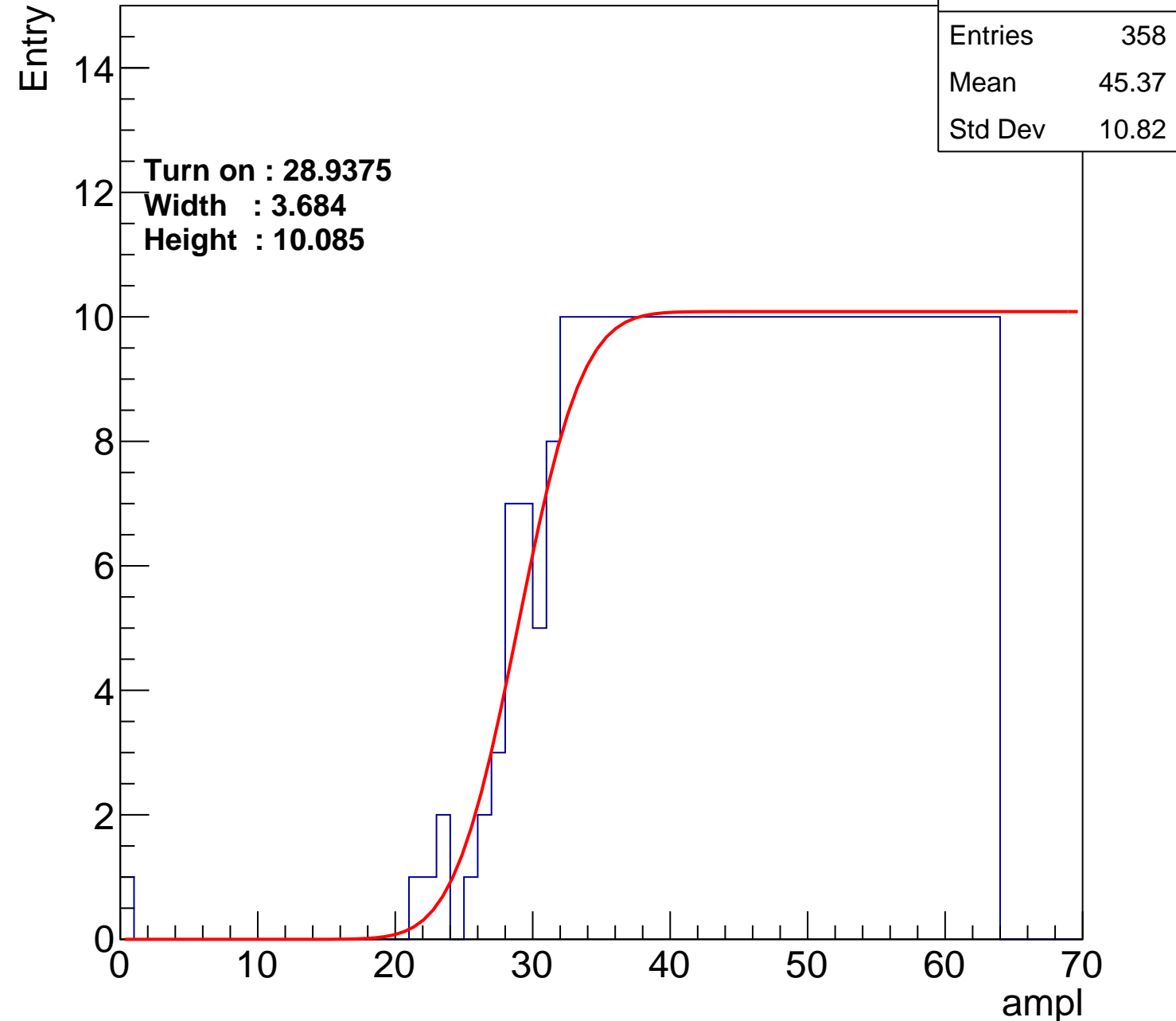
Width : 3.684

Height : 10.085

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch23

calib_packv5_042523_0143.root, FC#11, port A2

Entries	378
Mean	44.39
Std Dev	11.33

Turn on : 26.3394

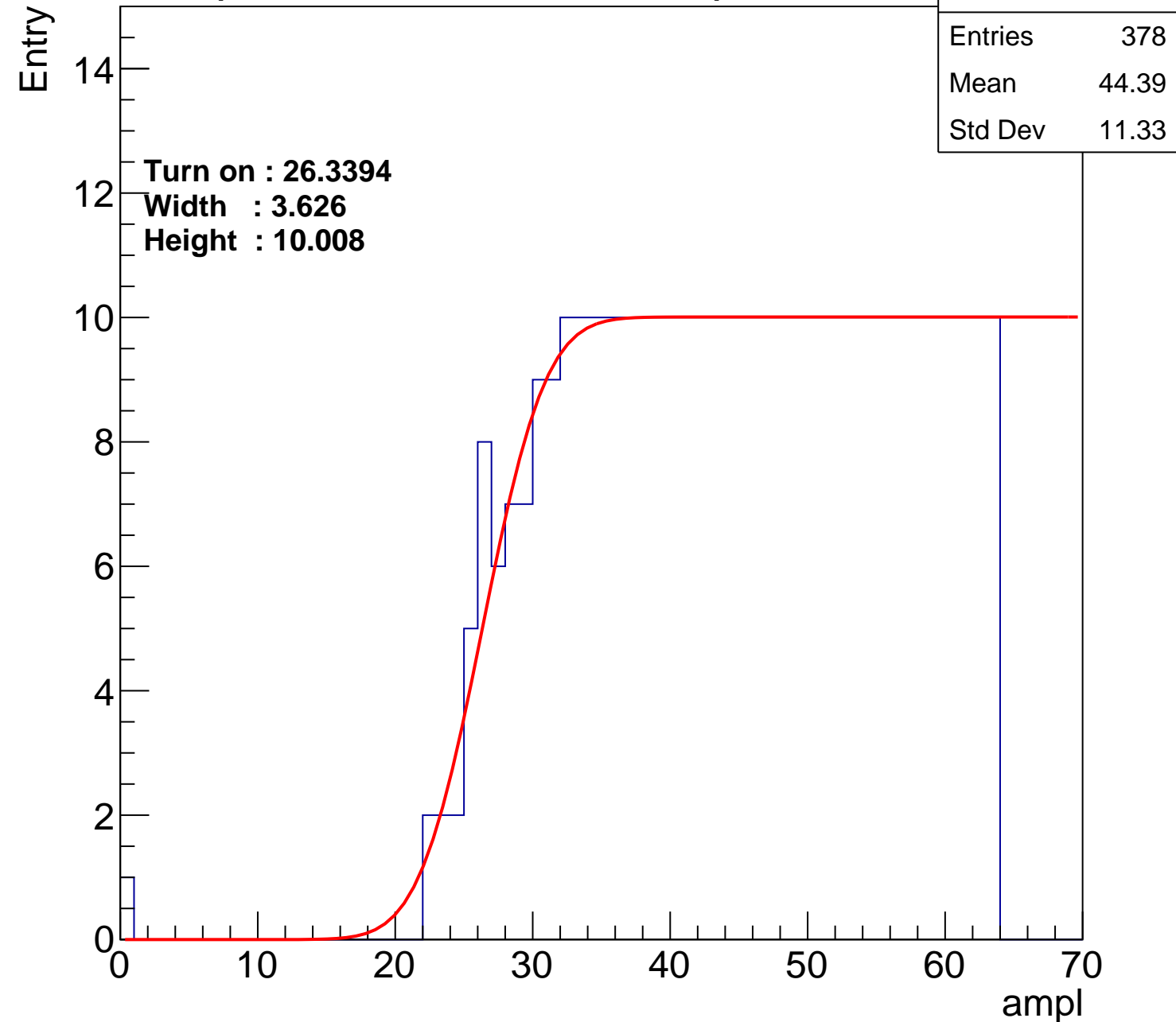
Width : 3.626

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch24

calib_packv5_042523_0143.root, FC#11, port A2

Entries	402
Mean	42.92
Std Dev	12.72

Turn on : 24.6902

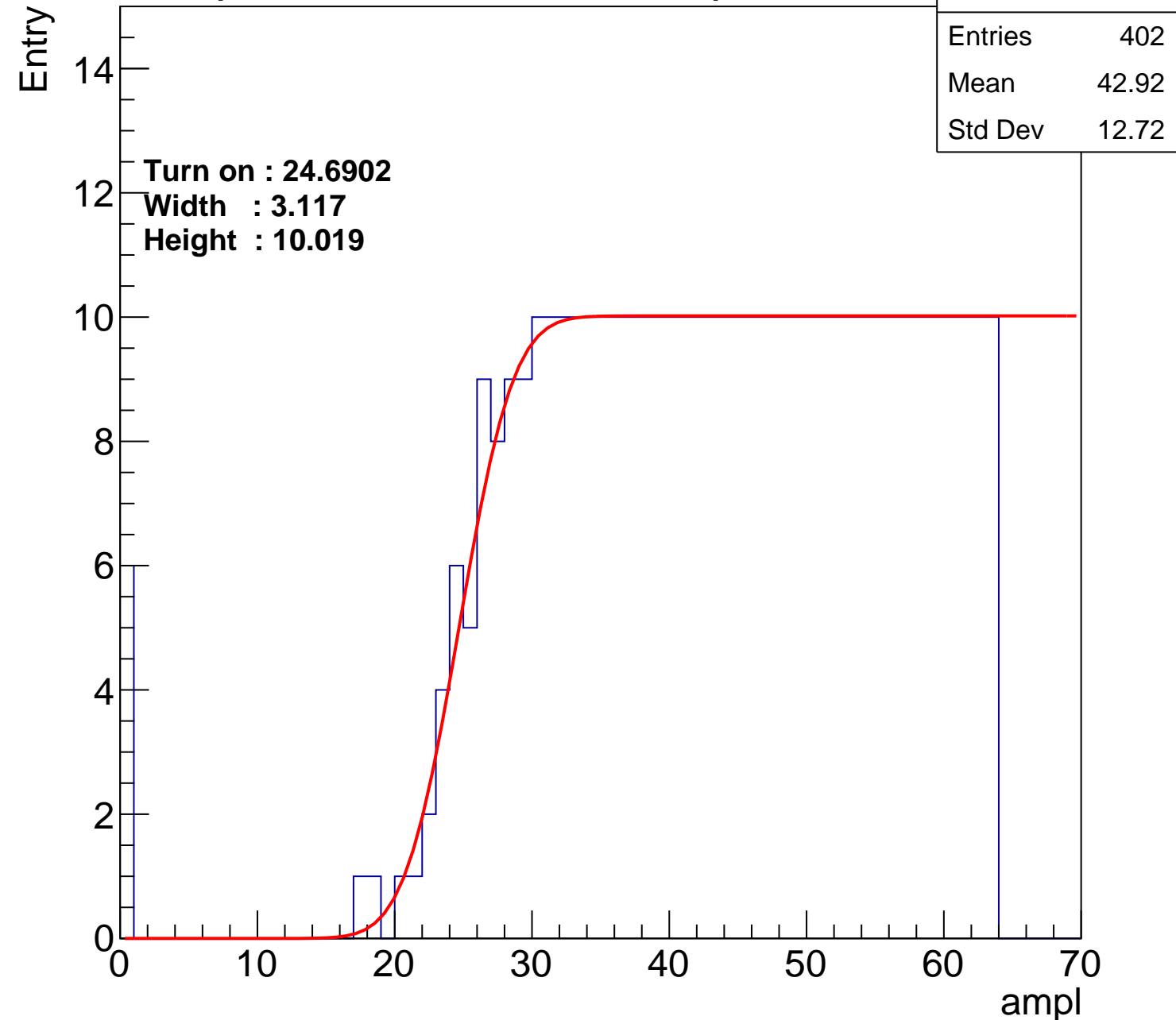
Width : 3.117

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch25

calib_packv5_042523_0143.root, FC#11, port A2

Entries	392
Mean	43.48
Std Dev	12.33

Turn on : 25.8044

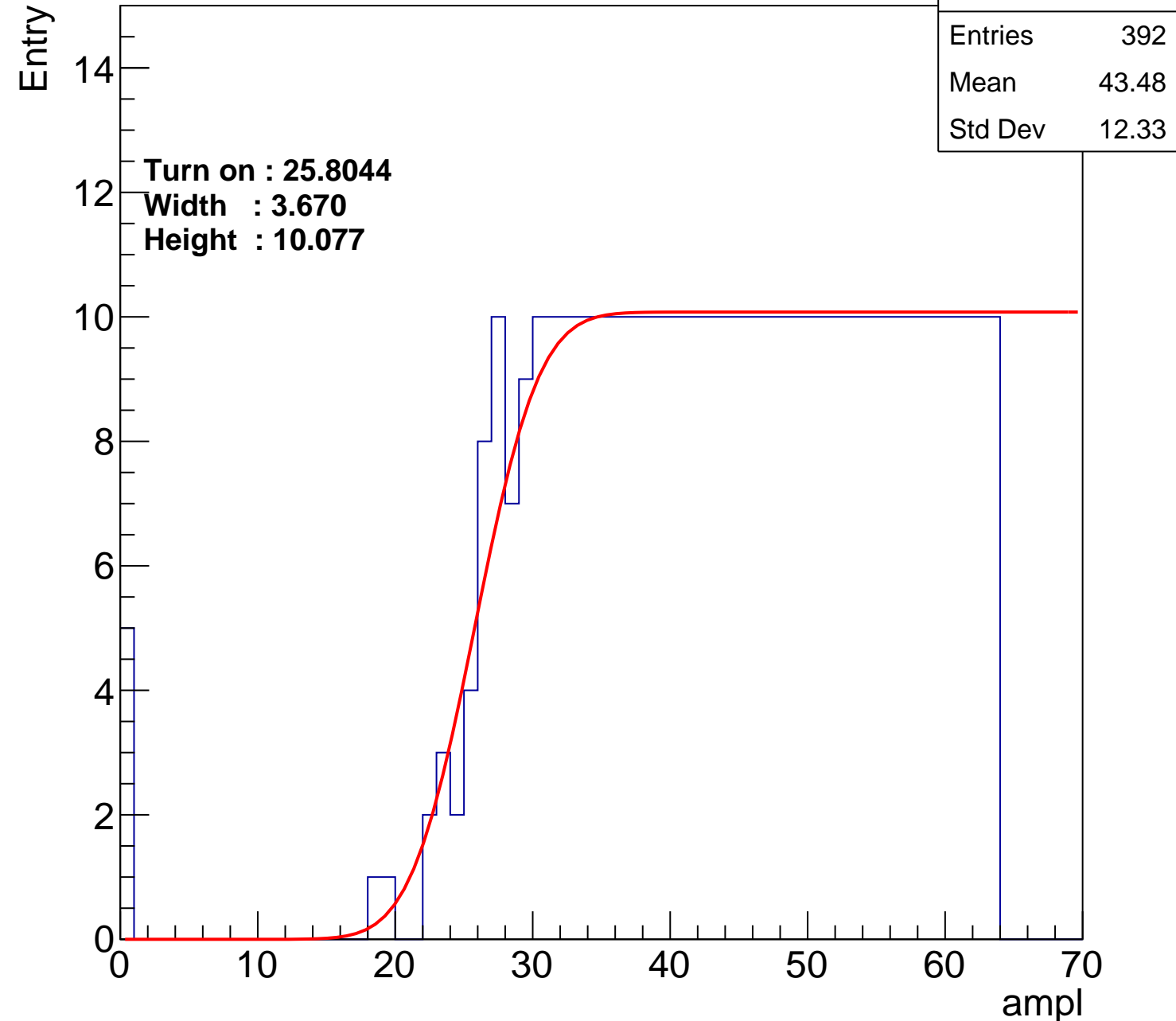
Width : 3.670

Height : 10.077

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch26

calib_packv5_042523_0143.root, FC#11, port A2

Entries	406
Mean	42.84
Std Dev	12.52

Turn on : 24.1471

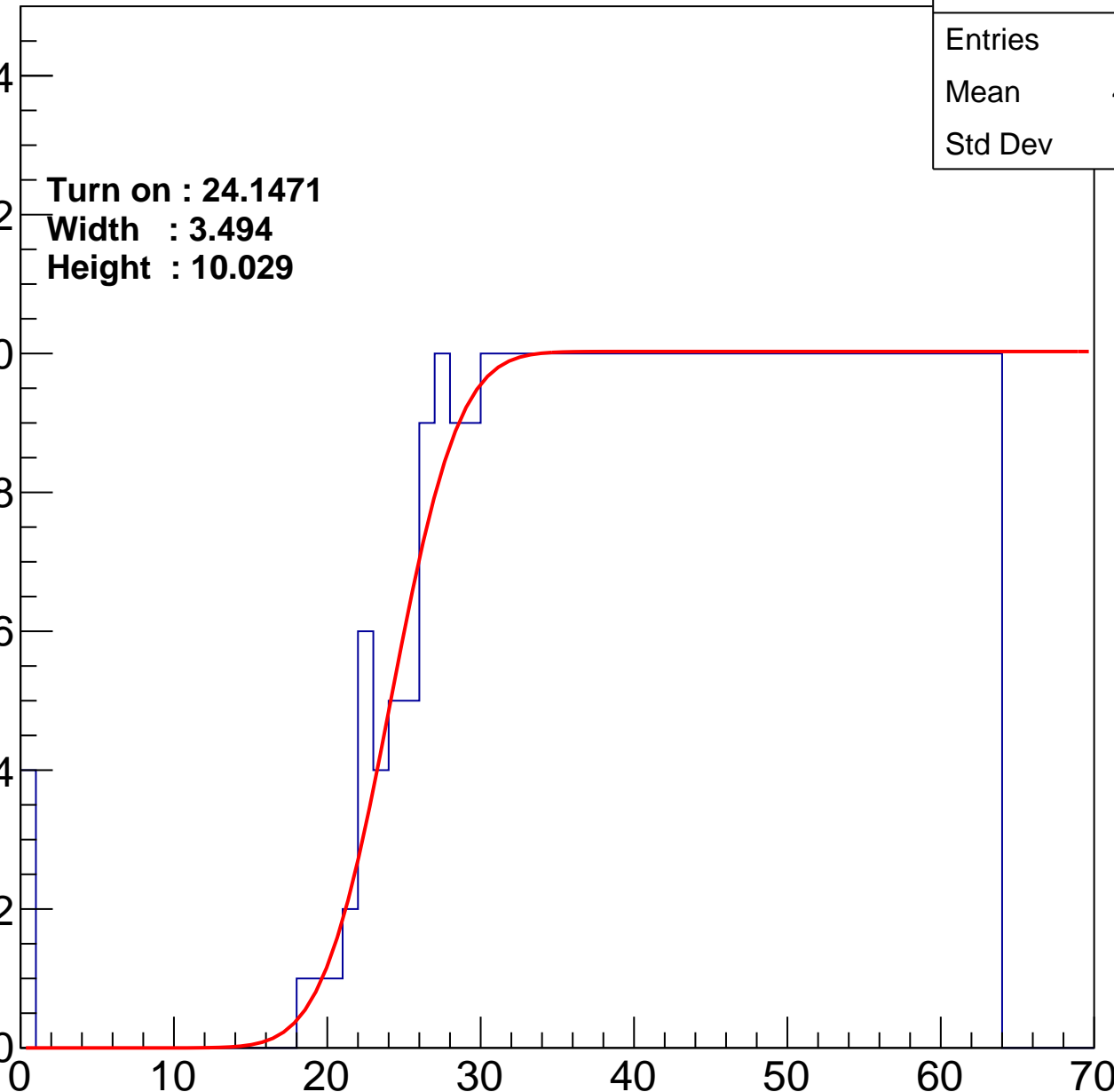
Width : 3.494

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch27

calib_packv5_042523_0143.root, FC#11, port A2

Entries	382
Mean	44.22
Std Dev	11.4

Turn on : 25.4776

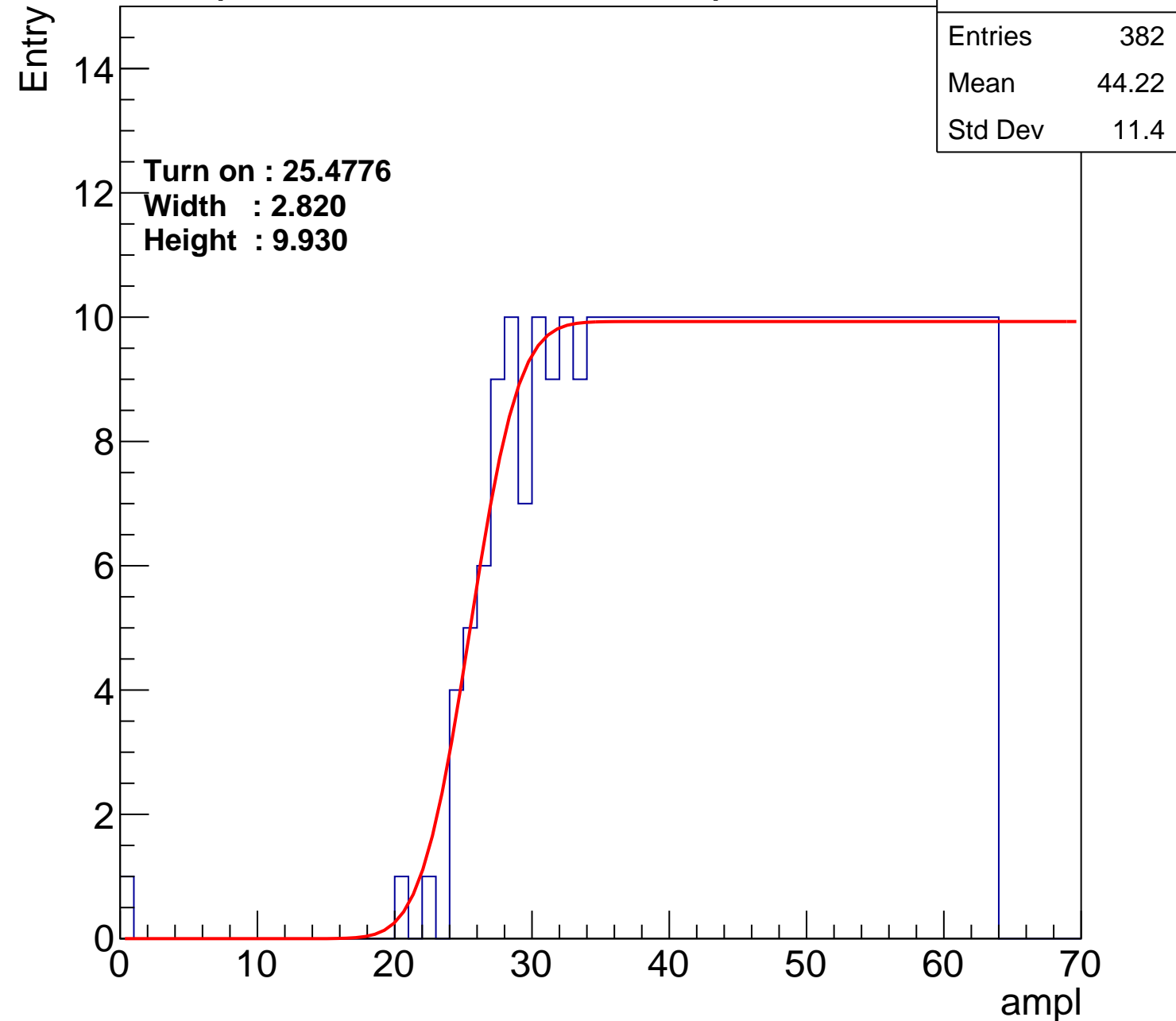
Width : 2.820

Height : 9.930

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch28

calib_packv5_042523_0143.root, FC#11, port A2

Entries	391
Mean	43.64
Std Dev	11.99

Turn on : 25.2858

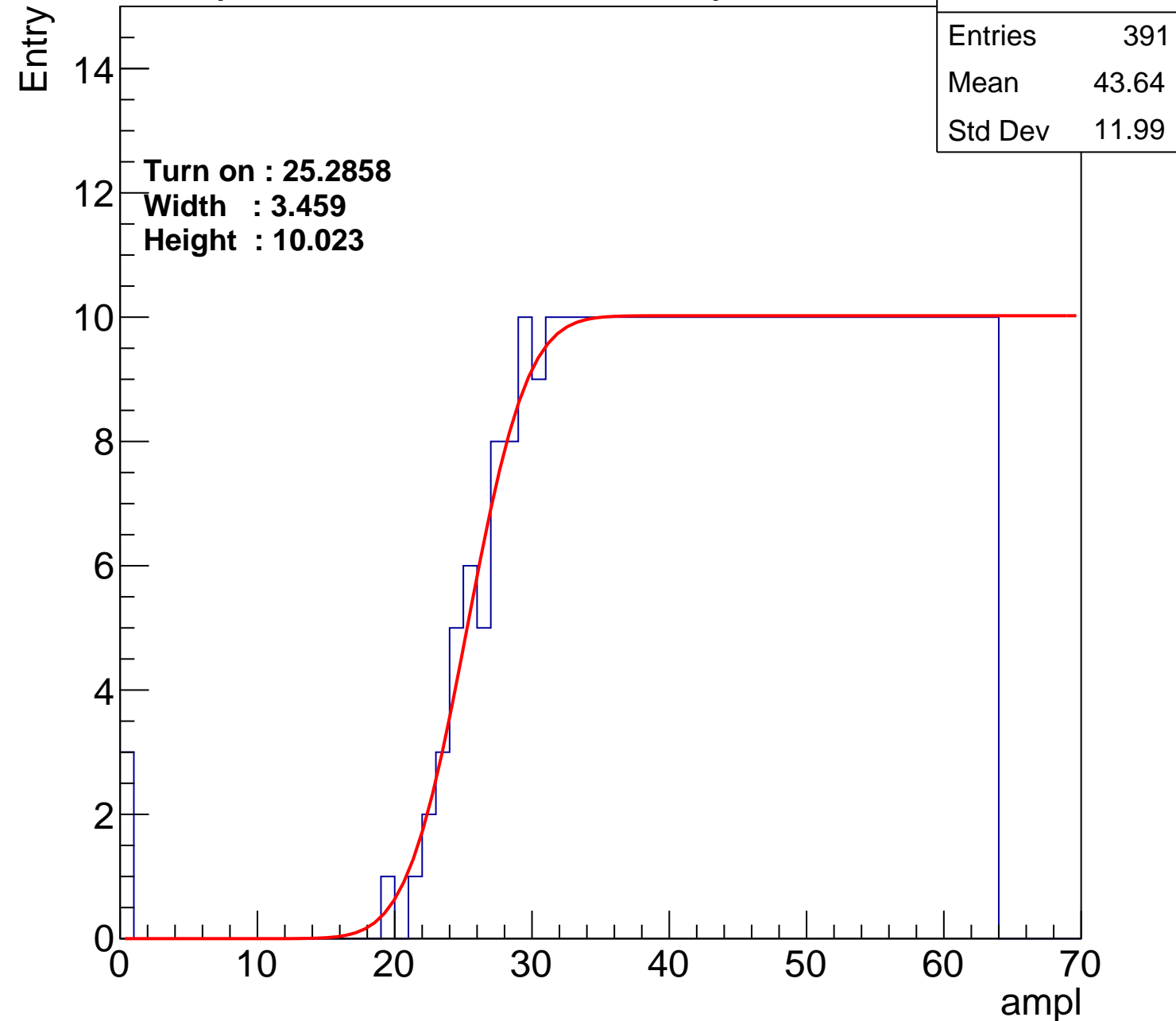
Width : 3.459

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch29

calib_packv5_042523_0143.root, FC#11, port A2

Entries	413
Mean	42.49
Std Dev	12.75

Turn on : 23.3558

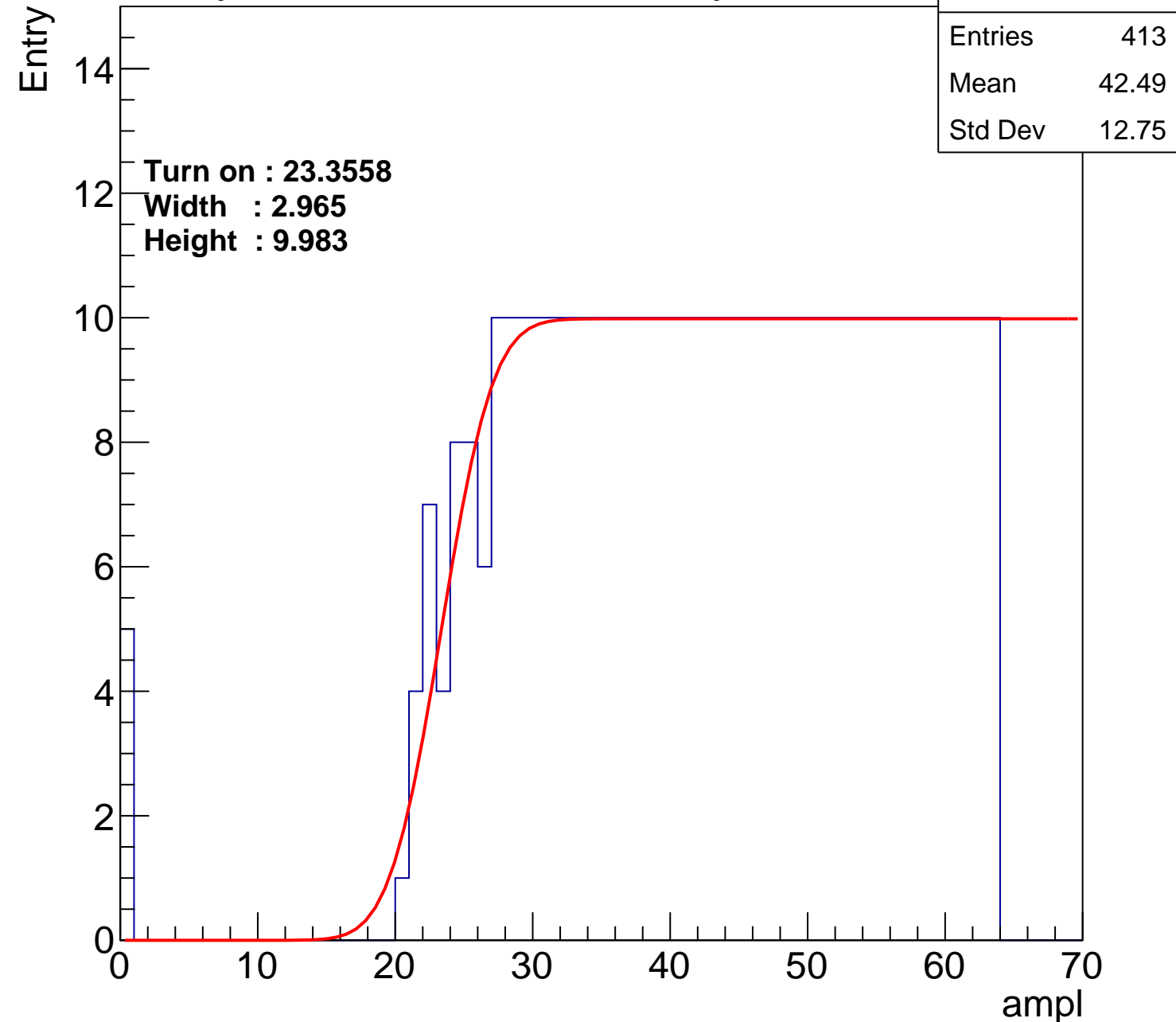
Width : 2.965

Height : 9.983

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch30

calib_packv5_042523_0143.root, FC#11, port A2

Entries	374
Mean	44.59
Std Dev	11.24

Turn on : 27.1188

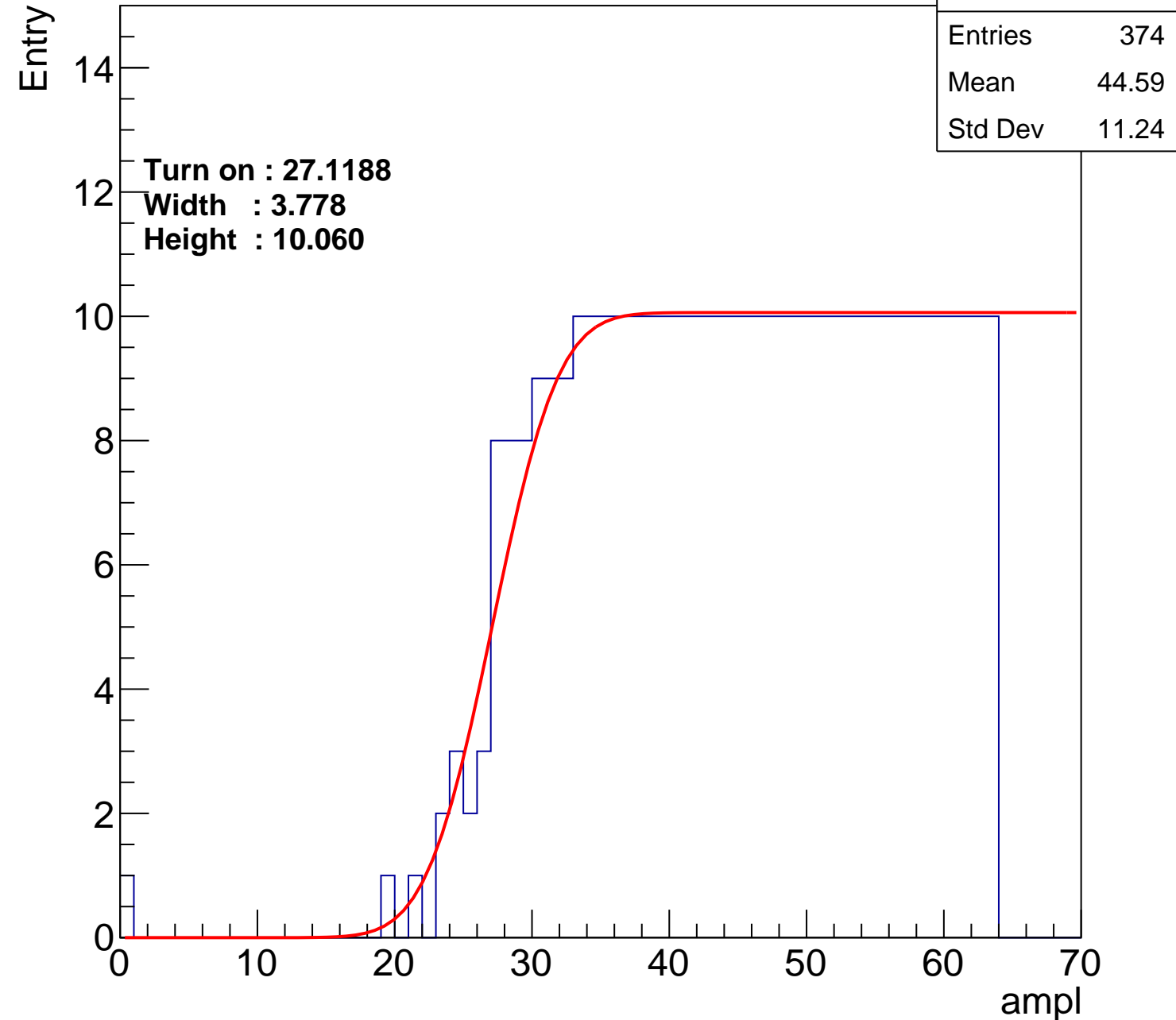
Width : 3.778

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch31

calib_packv5_042523_0143.root, FC#11, port A2

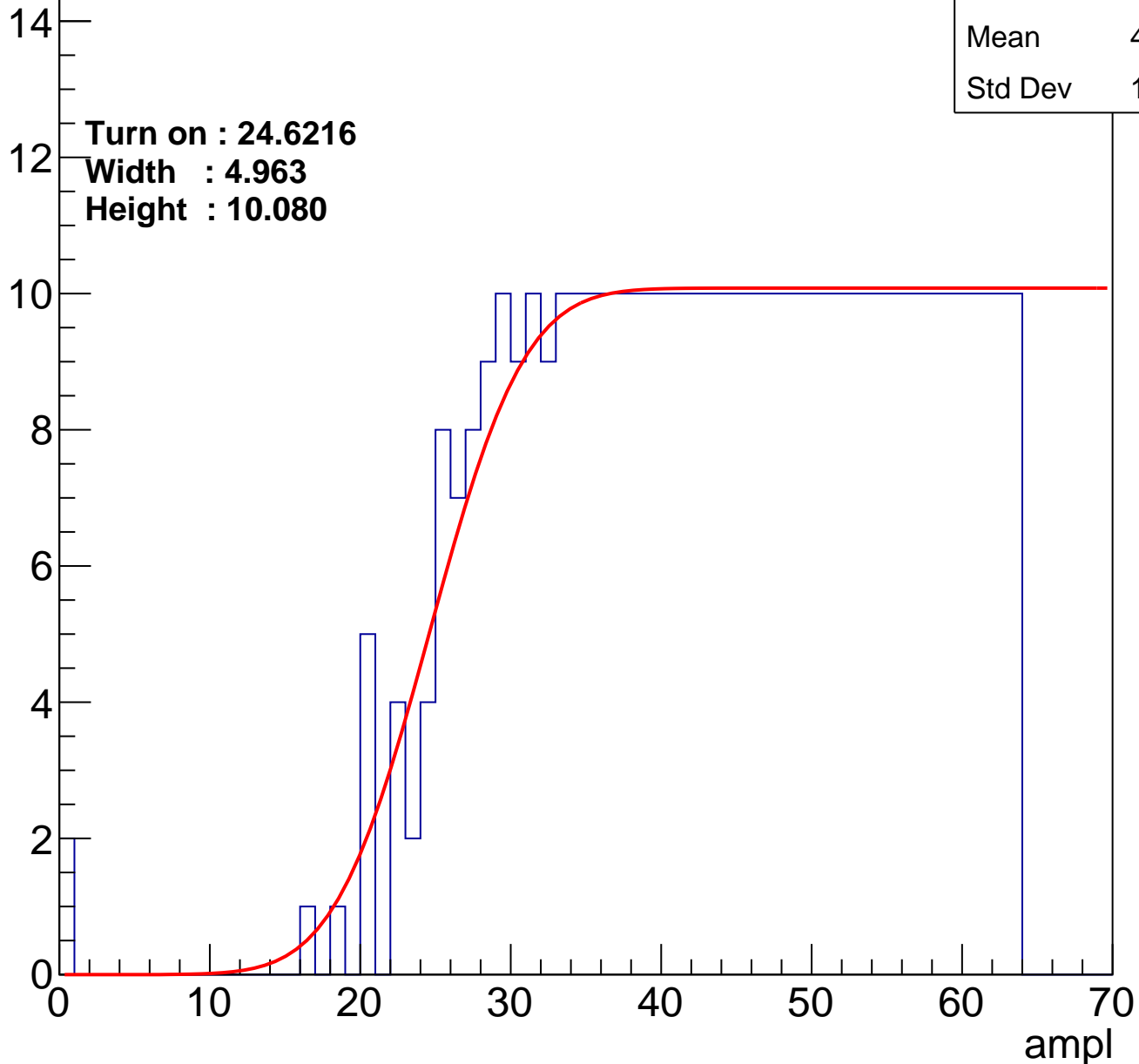
Entries	399
Mean	43.24
Std Dev	12.15

Turn on : 24.6216

Width : 4.963

Height : 10.080

Entry



B1L102S, U1-ch32

calib_packv5_042523_0143.root, FC#11, port A2

Entries	411
Mean	42.73
Std Dev	12.33

Turn on : 23.3041

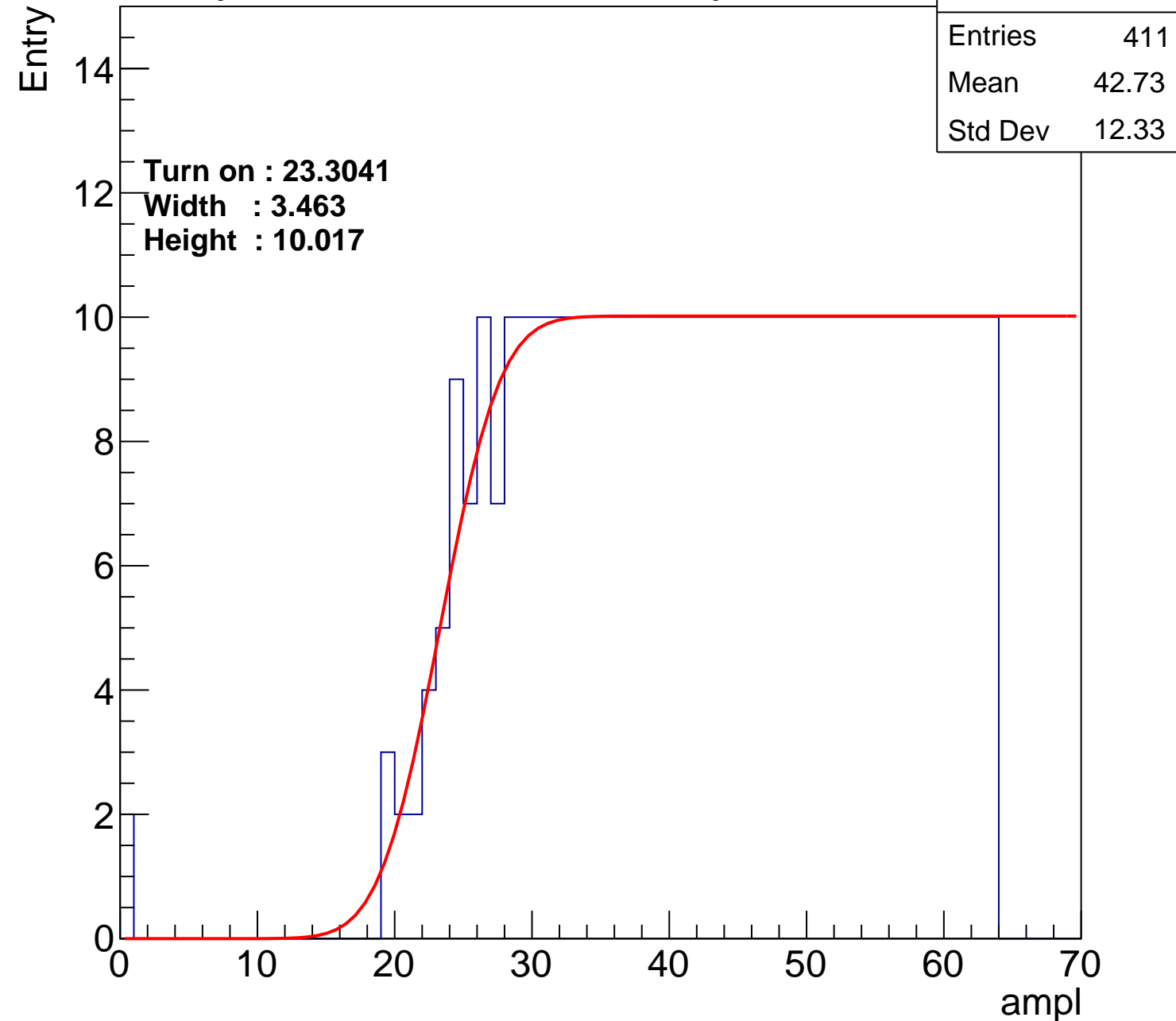
Width : 3.463

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch33

calib_packv5_042523_0143.root, FC#11, port A2

Entries	381
Mean	44.18
Std Dev	11.6

Turn on : 26.4478

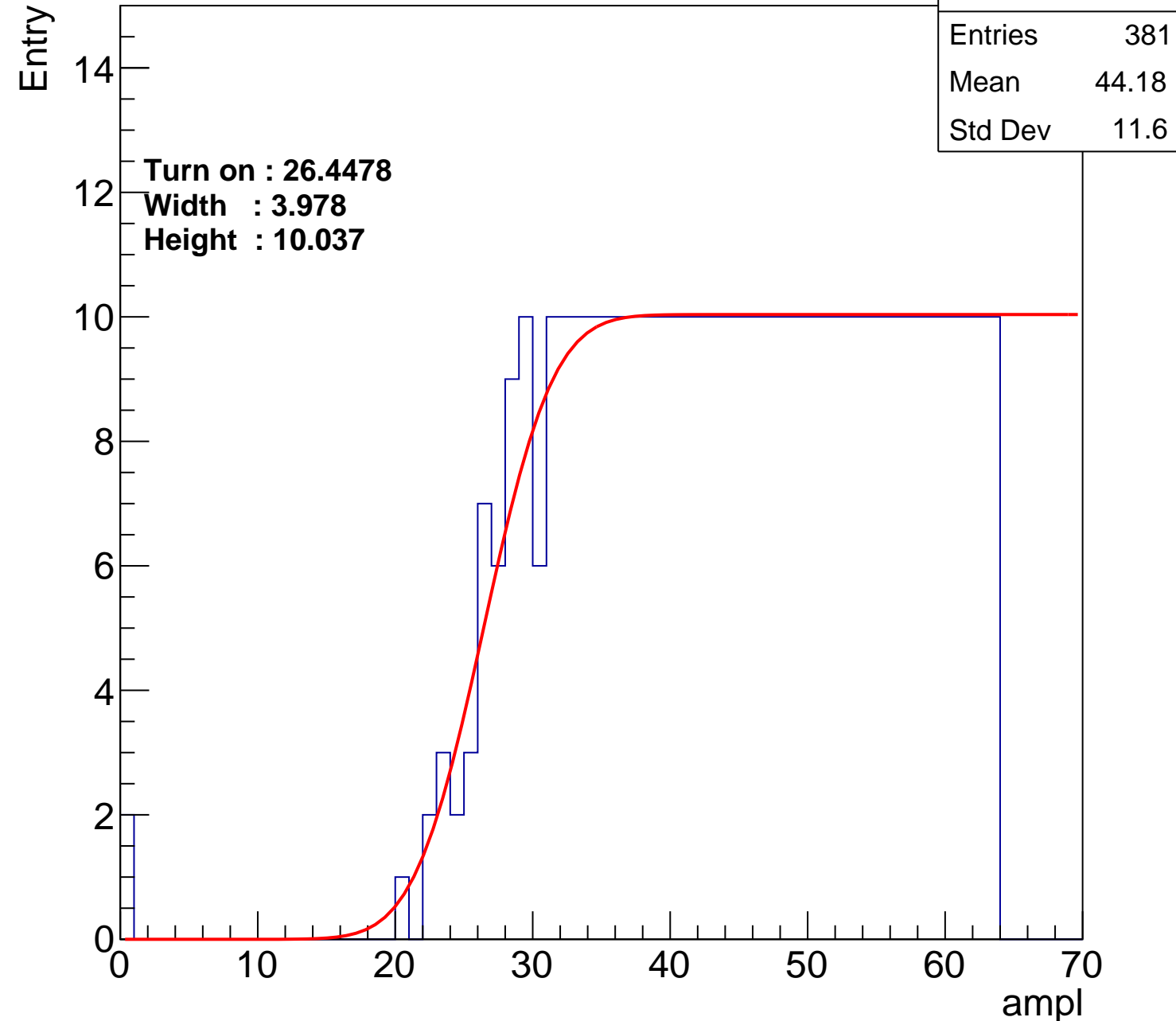
Width : 3.978

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch34

calib_packv5_042523_0143.root, FC#11, port A2

Entries	397
Mean	43.42
Std Dev	11.97

Turn on : 24.7293

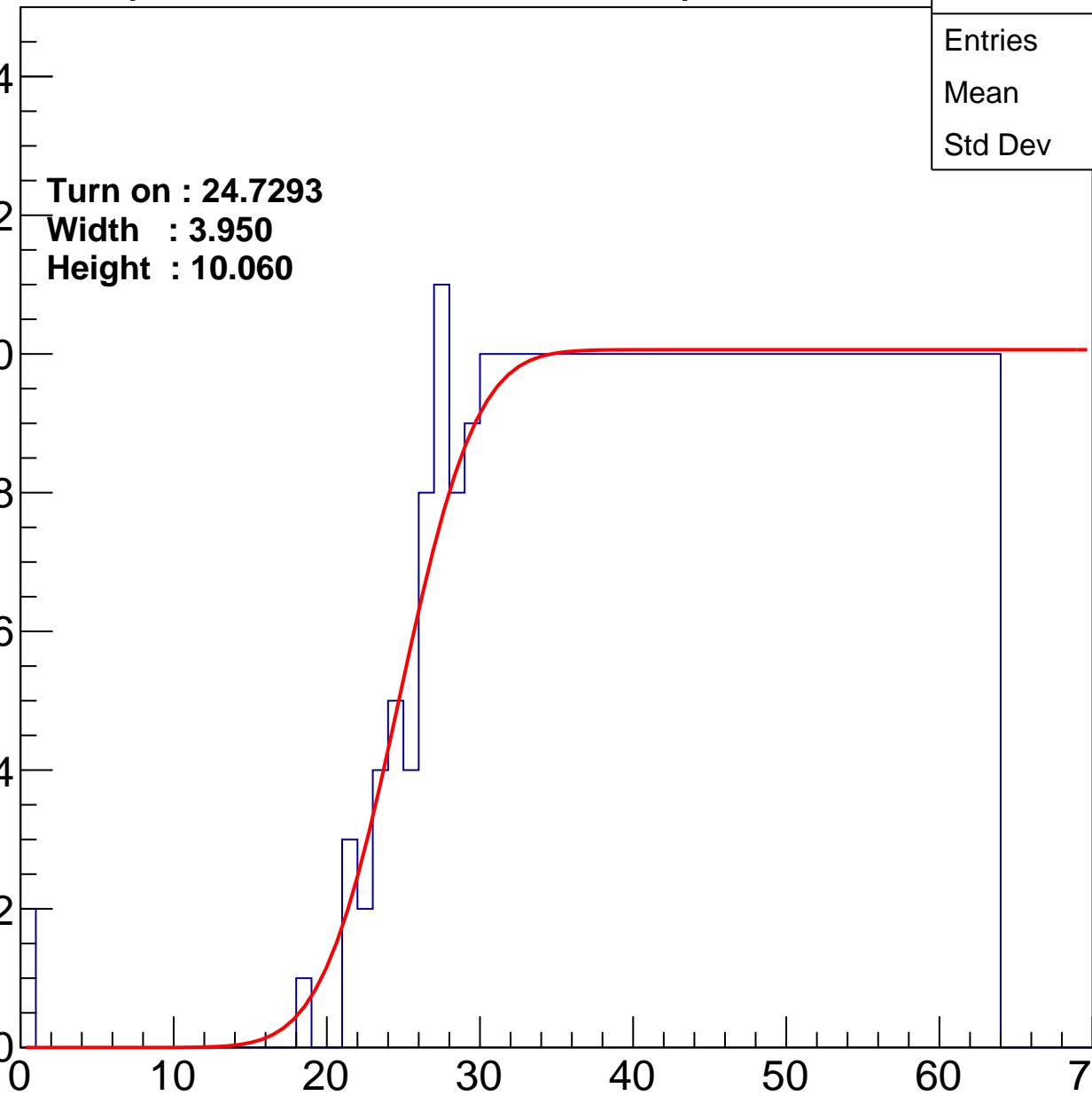
Width : 3.950

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch35

calib_packv5_042523_0143.root, FC#11, port A2

Entries	374
Mean	44.66
Std Dev	11.11

Turn on : 26.7280

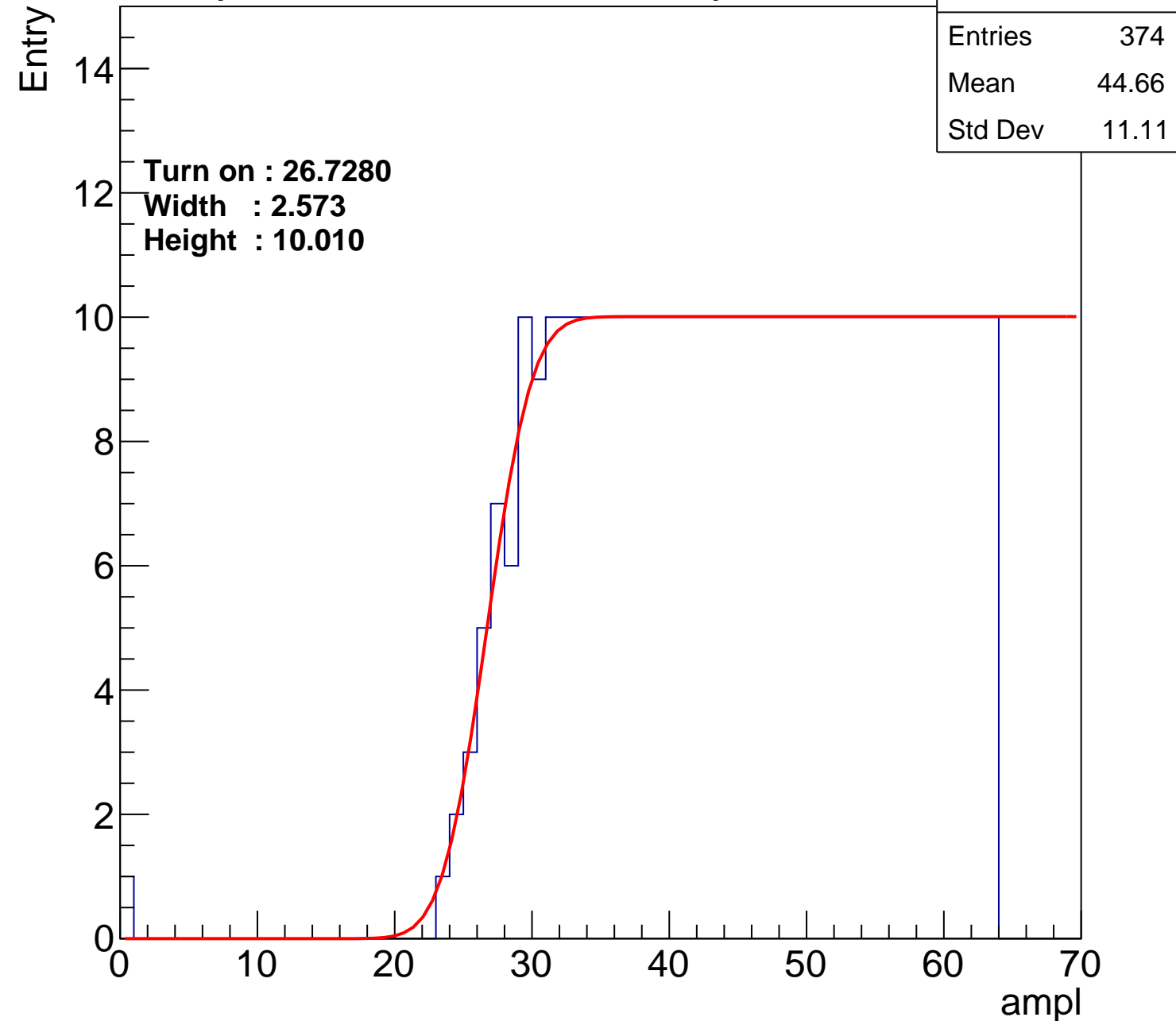
Width : 2.573

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch36

calib_packv5_042523_0143.root, FC#11, port A2

Entries	394
Mean	43.57
Std Dev	11.89

Turn on : 25.0370

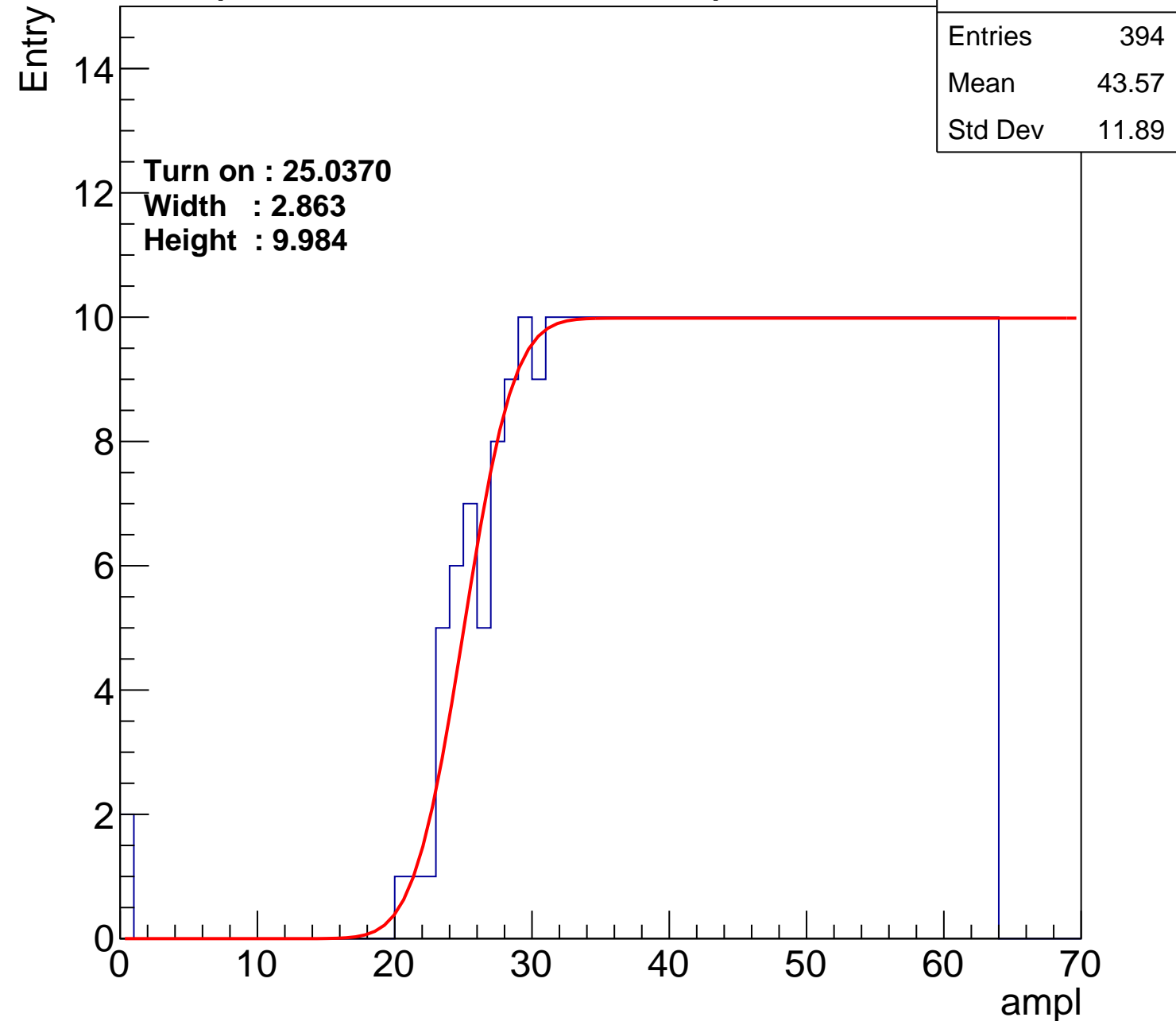
Width : 2.863

Height : 9.984

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch37

calib_packv5_042523_0143.root, FC#11, port A2

Entries	390
Mean	43.84
Std Dev	11.59

Turn on : 24.9226

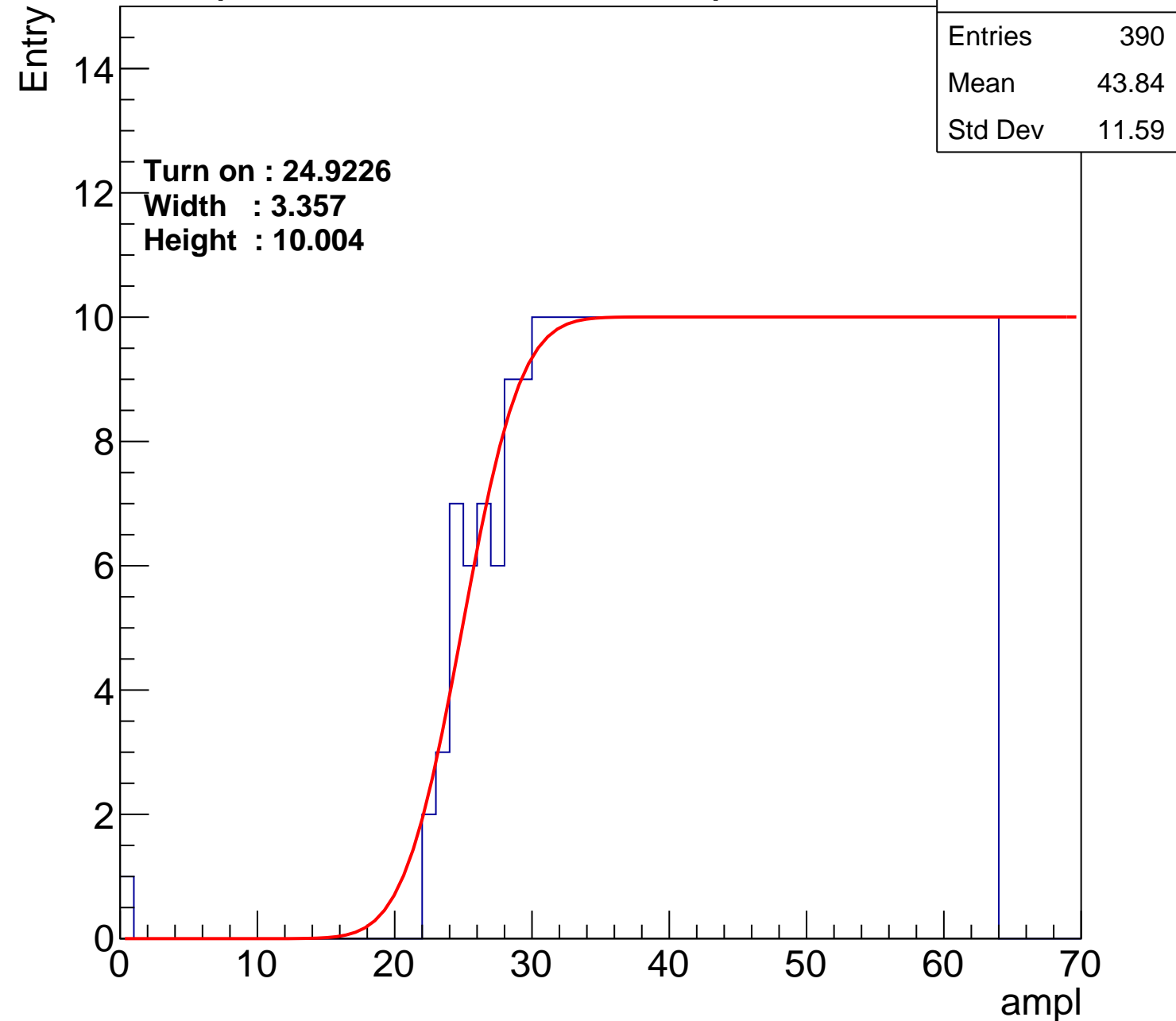
Width : 3.357

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch38

calib_packv5_042523_0143.root, FC#11, port A2

Entries	396
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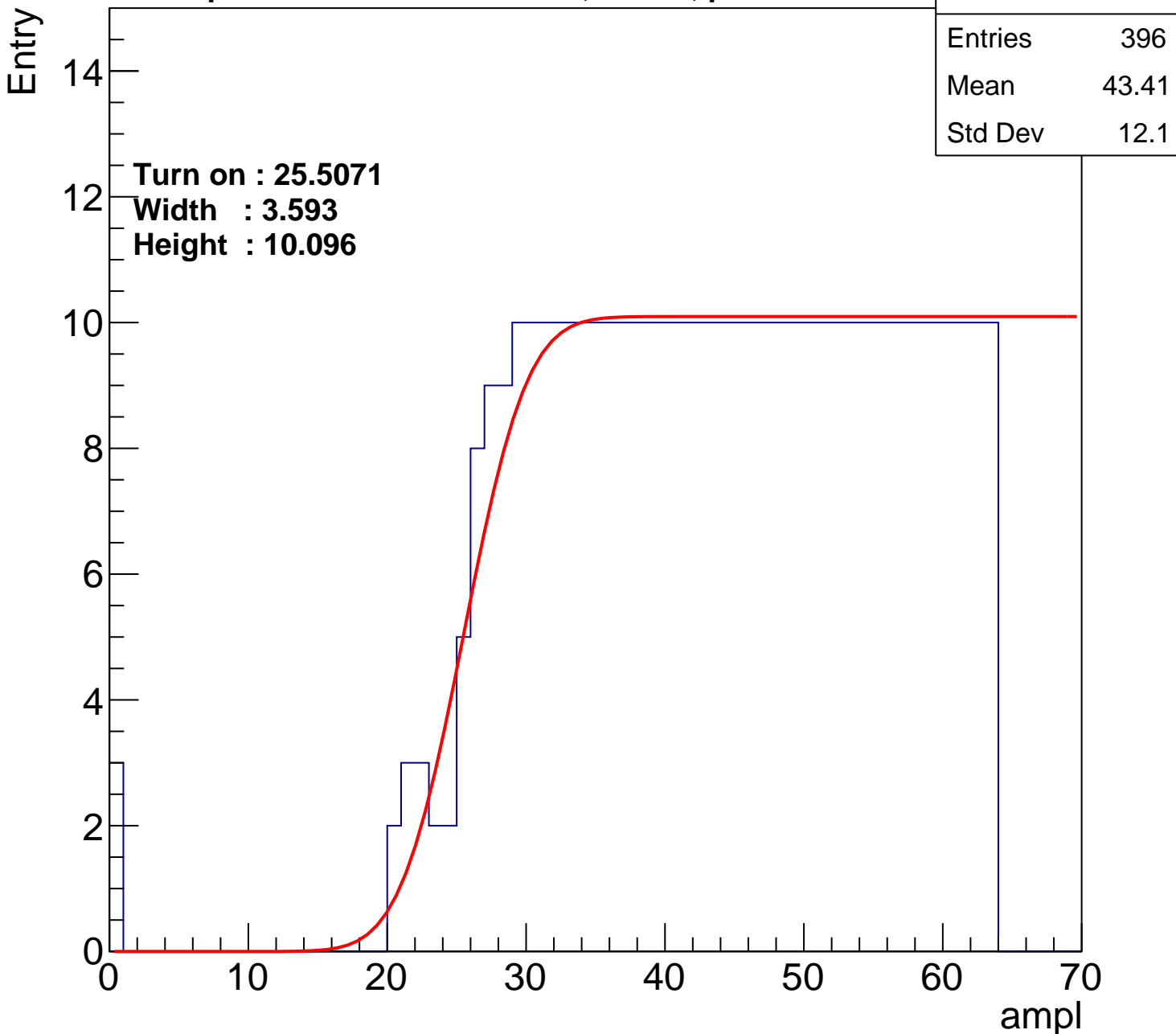
Mean	43.41
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Std Dev	12.1
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Turn on : 25.5071

Width : 3.593

Height : 10.096



B1L102S, U1-ch39

calib_packv5_042523_0143.root, FC#11, port A2

Entries	385
Mean	43.92
Std Dev	11.86

Turn on : 25.5926

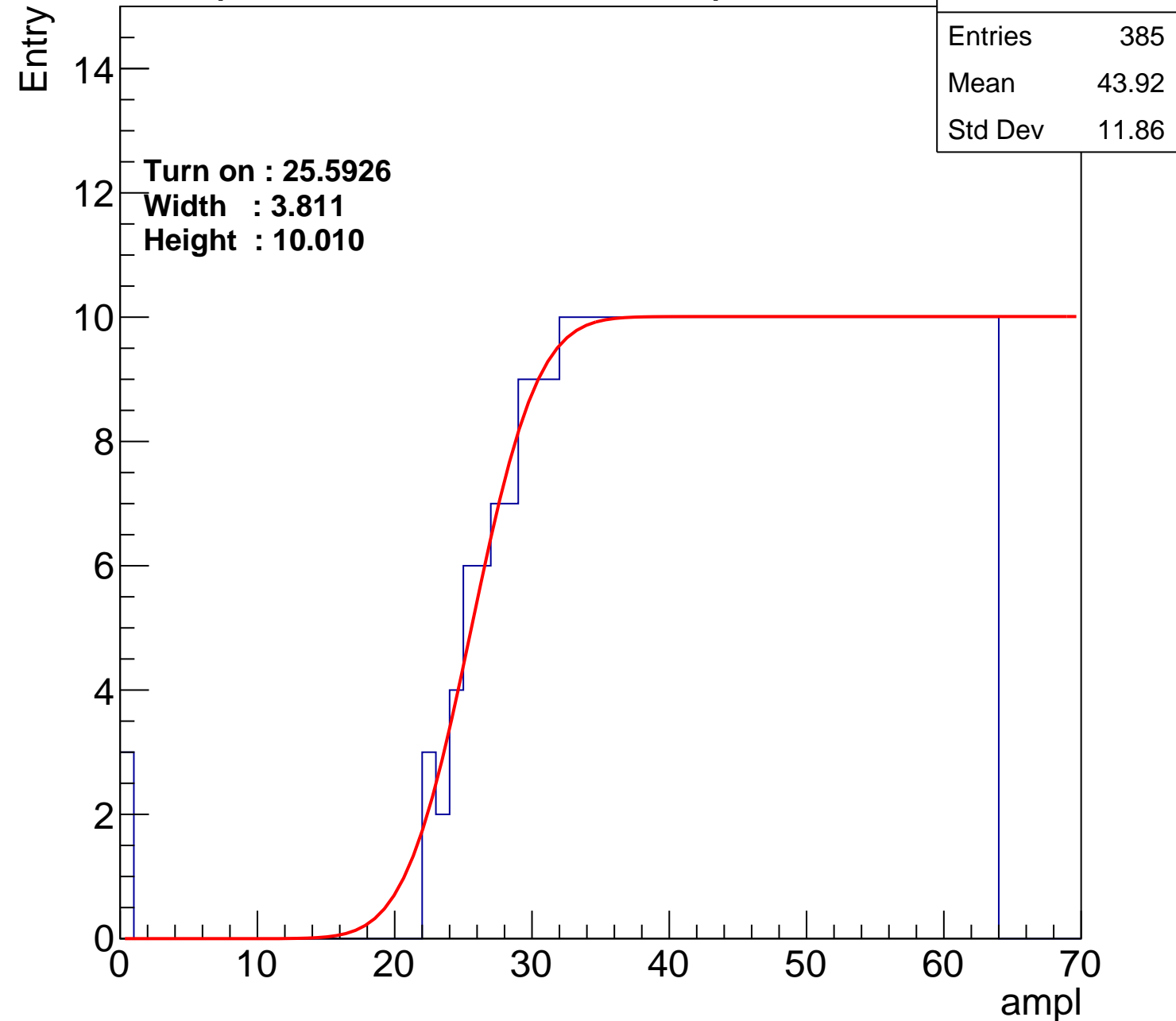
Width : 3.811

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch40

calib_packv5_042523_0143.root, FC#11, port A2

Entries	383
Mean	43.96
Std Dev	11.98

Turn on : 25.2576

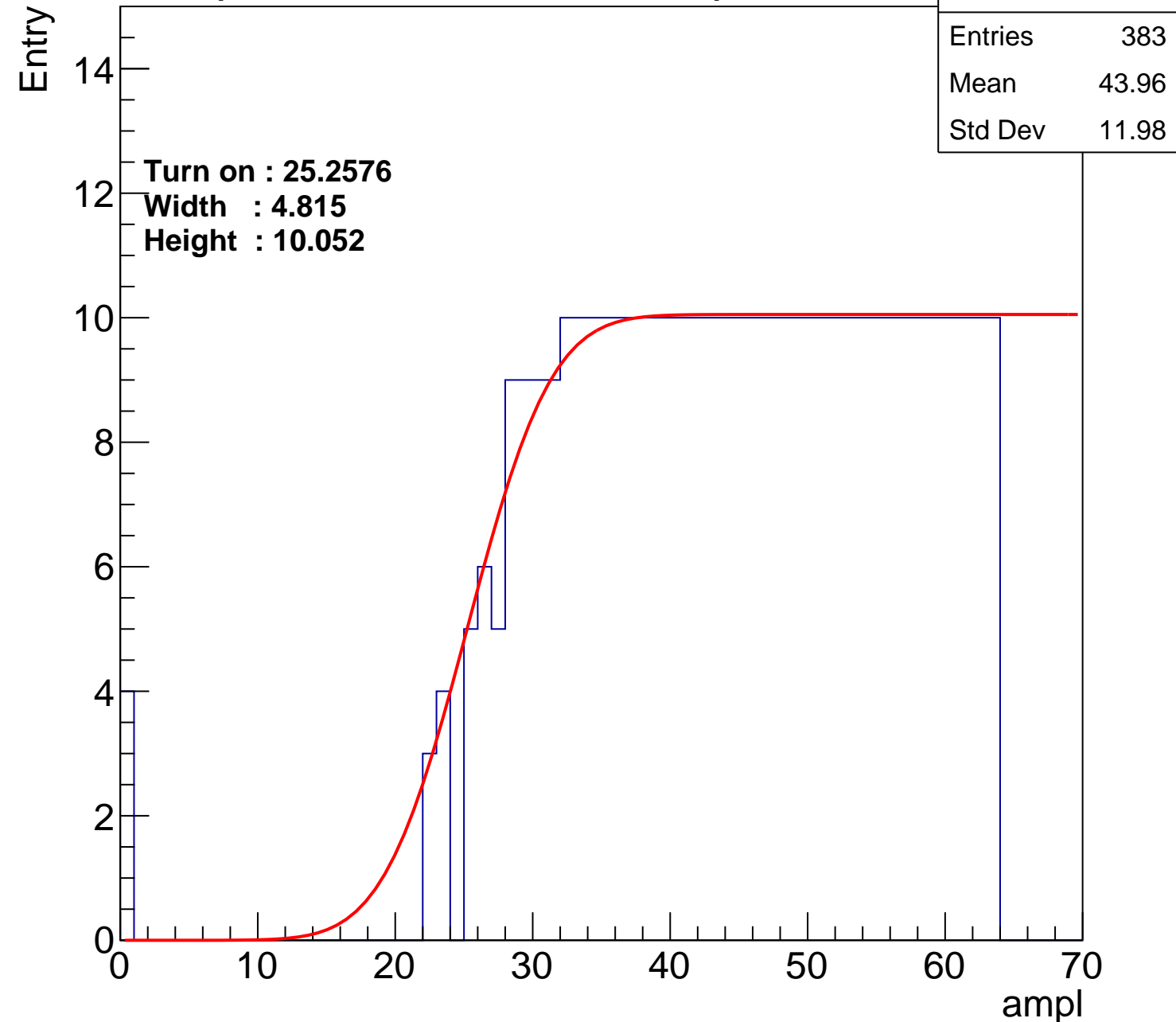
Width : 4.815

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch41

calib_packv5_042523_0143.root, FC#11, port A2

Entries	388
Mean	43.95
Std Dev	11.53

Turn on : 25.3549

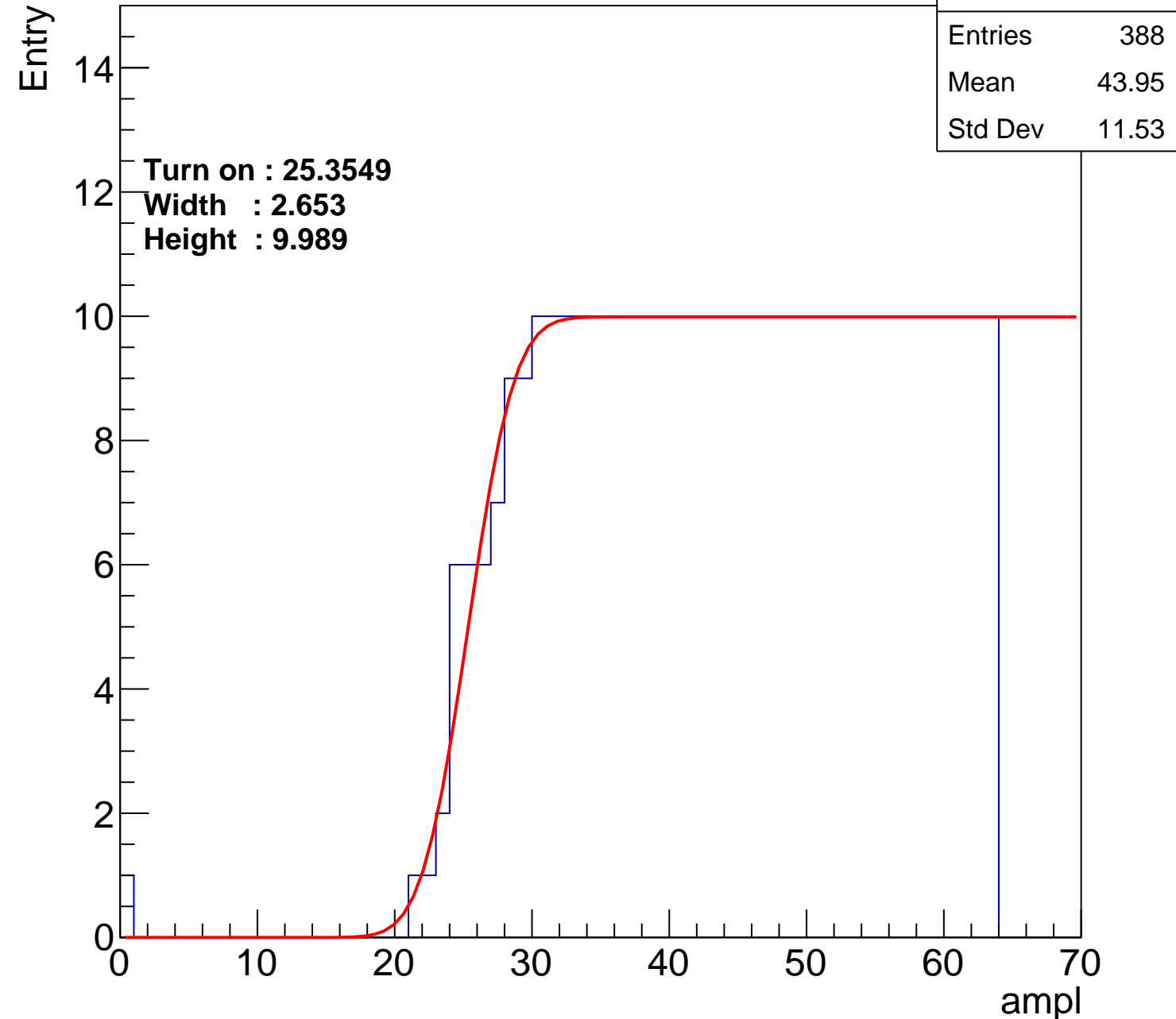
Width : 2.653

Height : 9.989

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch42

calib_packv5_042523_0143.root, FC#11, port A2

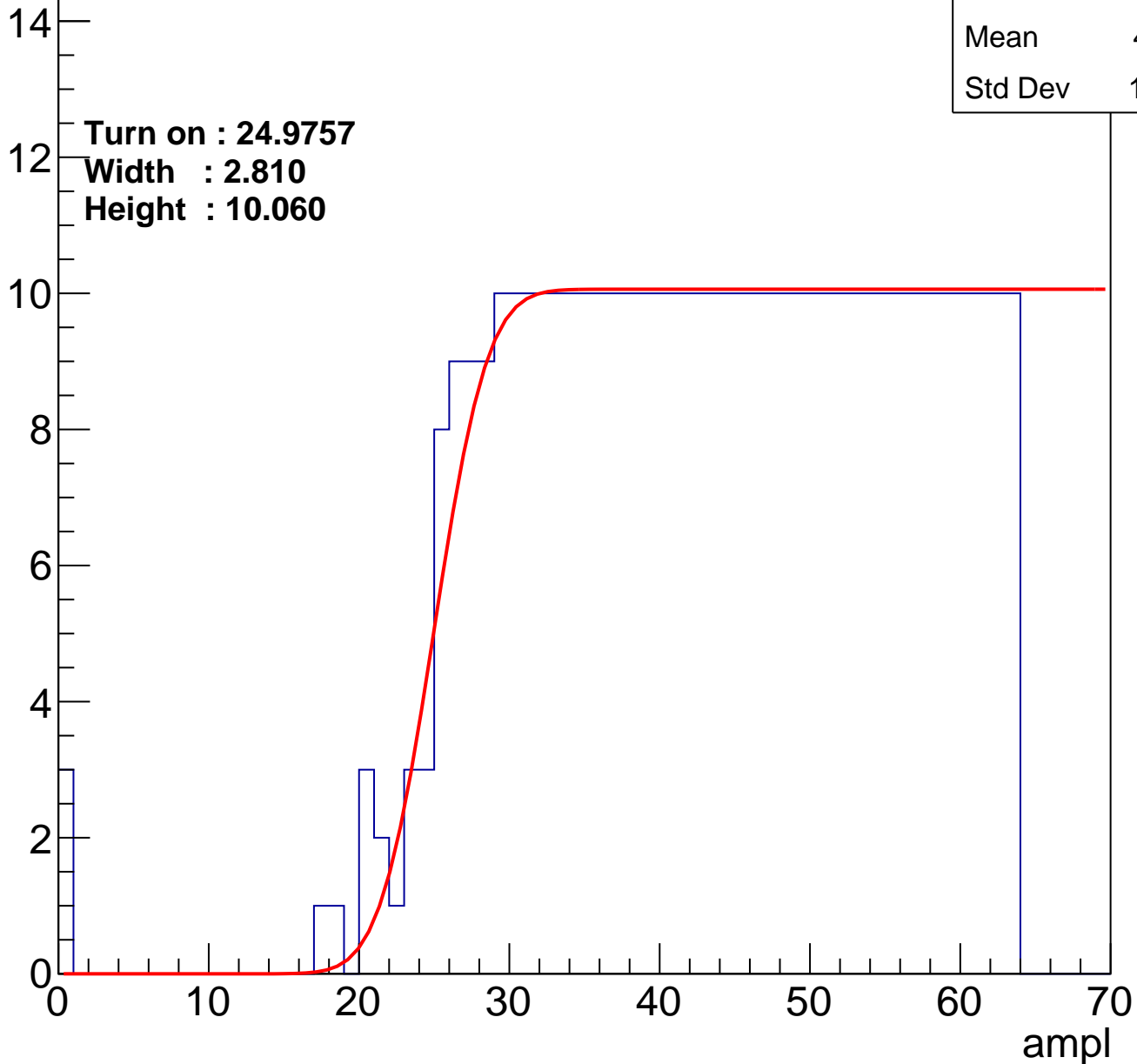
Entries	402
Mean	43.11
Std Dev	12.27

Turn on : 24.9757

Width : 2.810

Height : 10.060

Entry



B1L102S, U1-ch43

calib_packv5_042523_0143.root, FC#11, port A2

Entries	397
Mean	43.37
Std Dev	12.11

Turn on : 24.8736

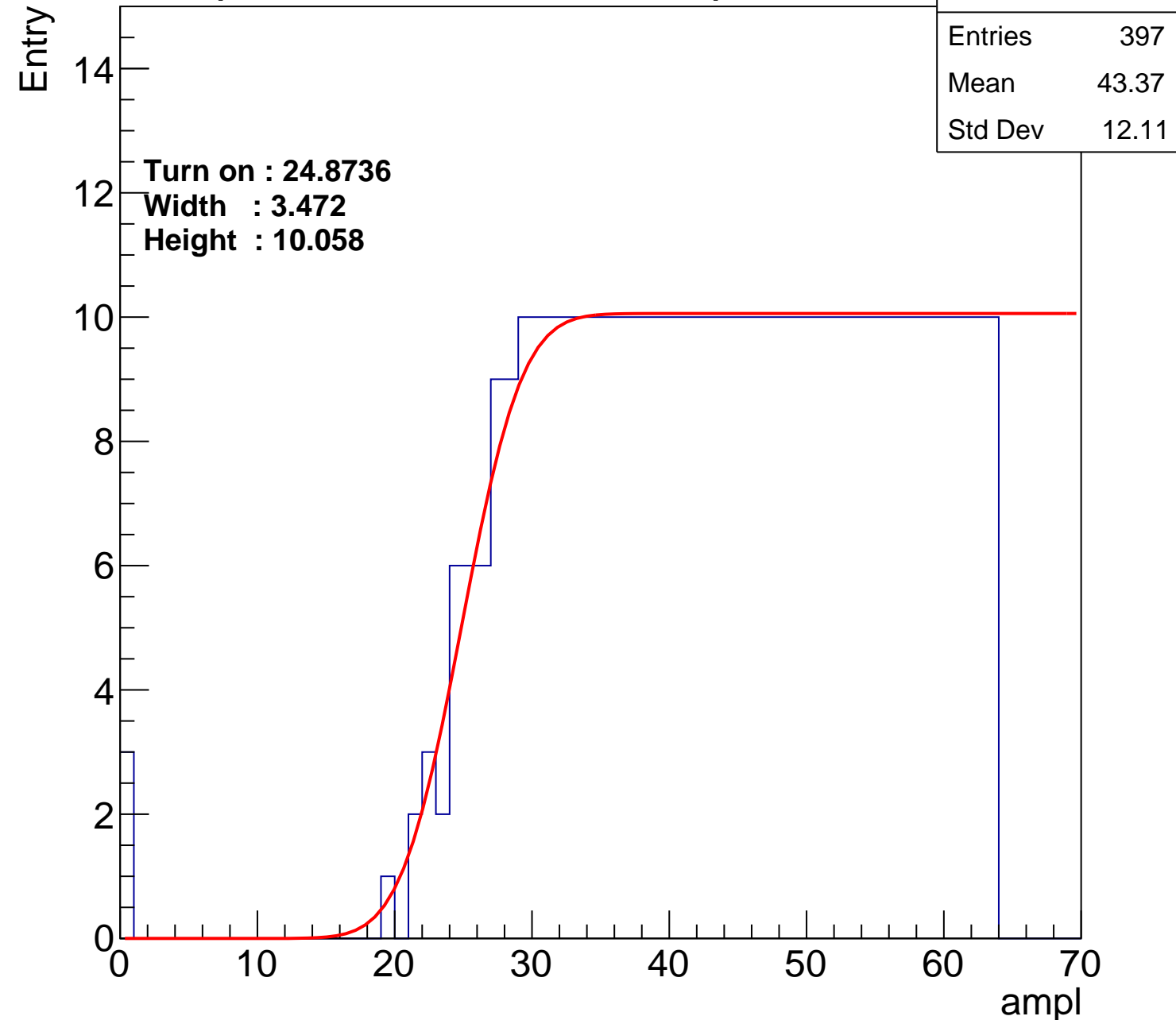
Width : 3.472

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch44

calib_packv5_042523_0143.root, FC#11, port A2

Entries	388
Mean	43.82
Std Dev	11.8

Turn on : 25.8171

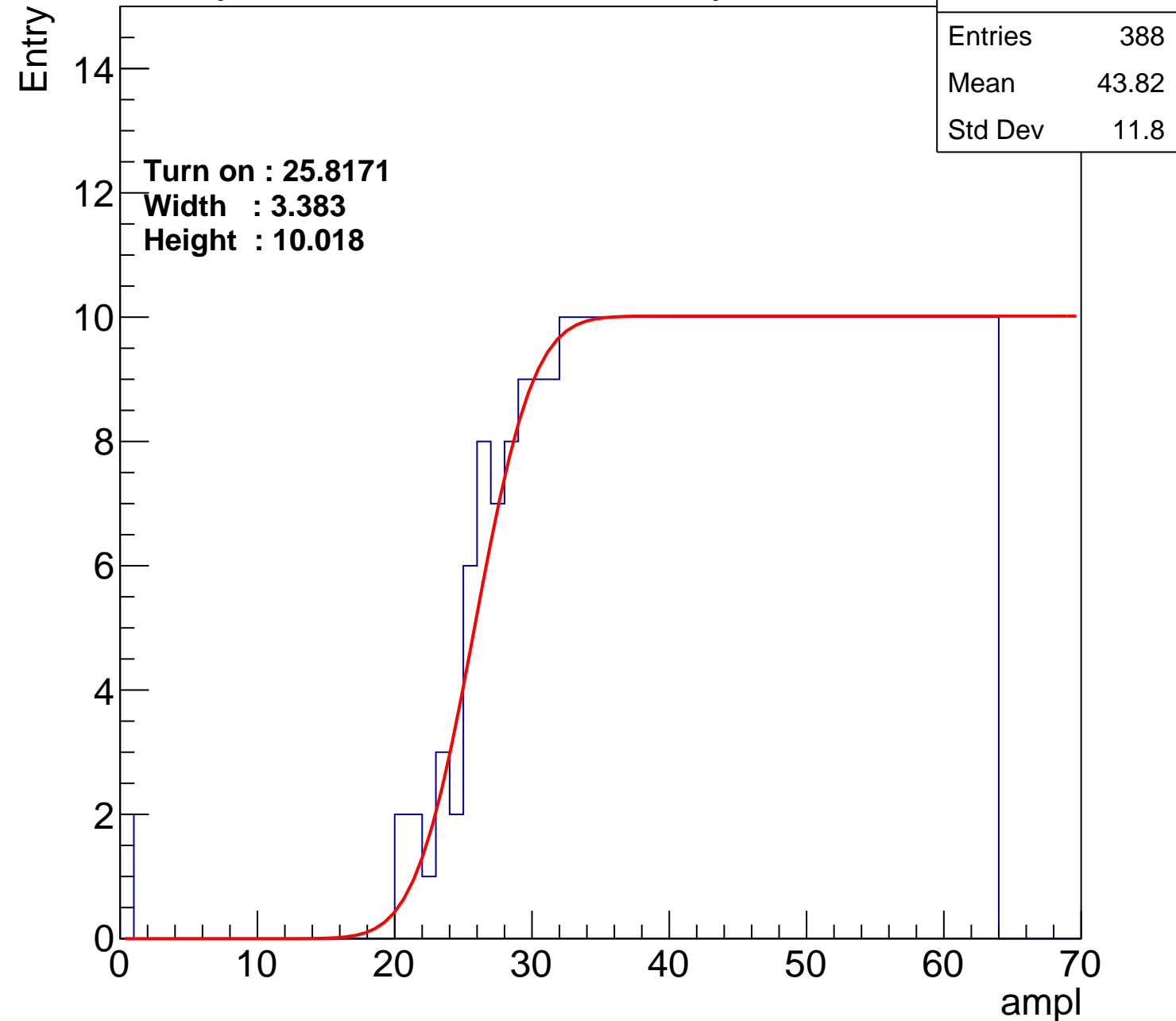
Width : 3.383

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch45

calib_packv5_042523_0143.root, FC#11, port A2

Entries	395
Mean	43.49
Std Dev	12.02

Turn on : 24.8459

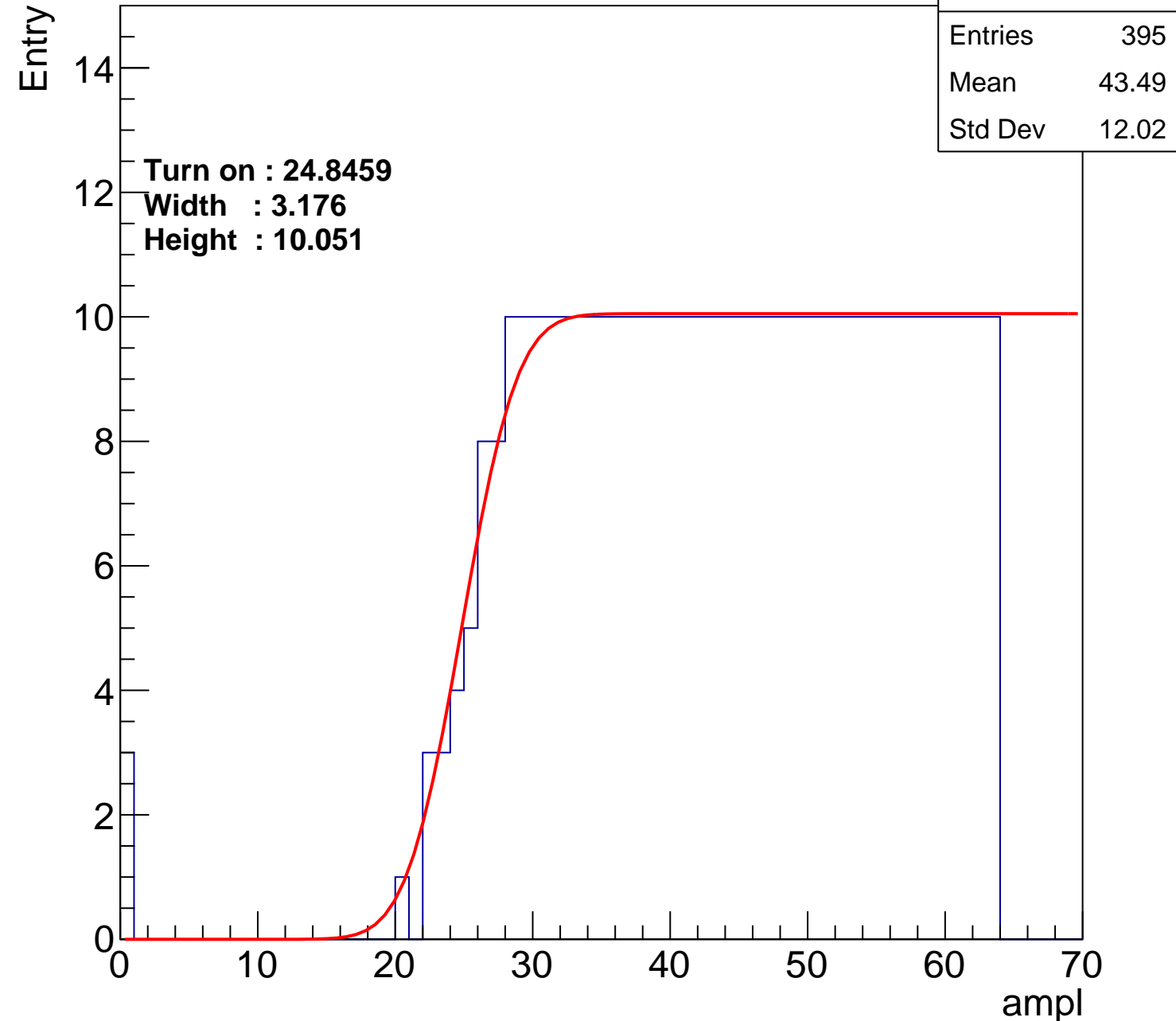
Width : 3.176

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch46

calib_packv5_042523_0143.root, FC#11, port A2

Entries	394
Mean	43.45
Std Dev	12.19

Turn on : 25.7639

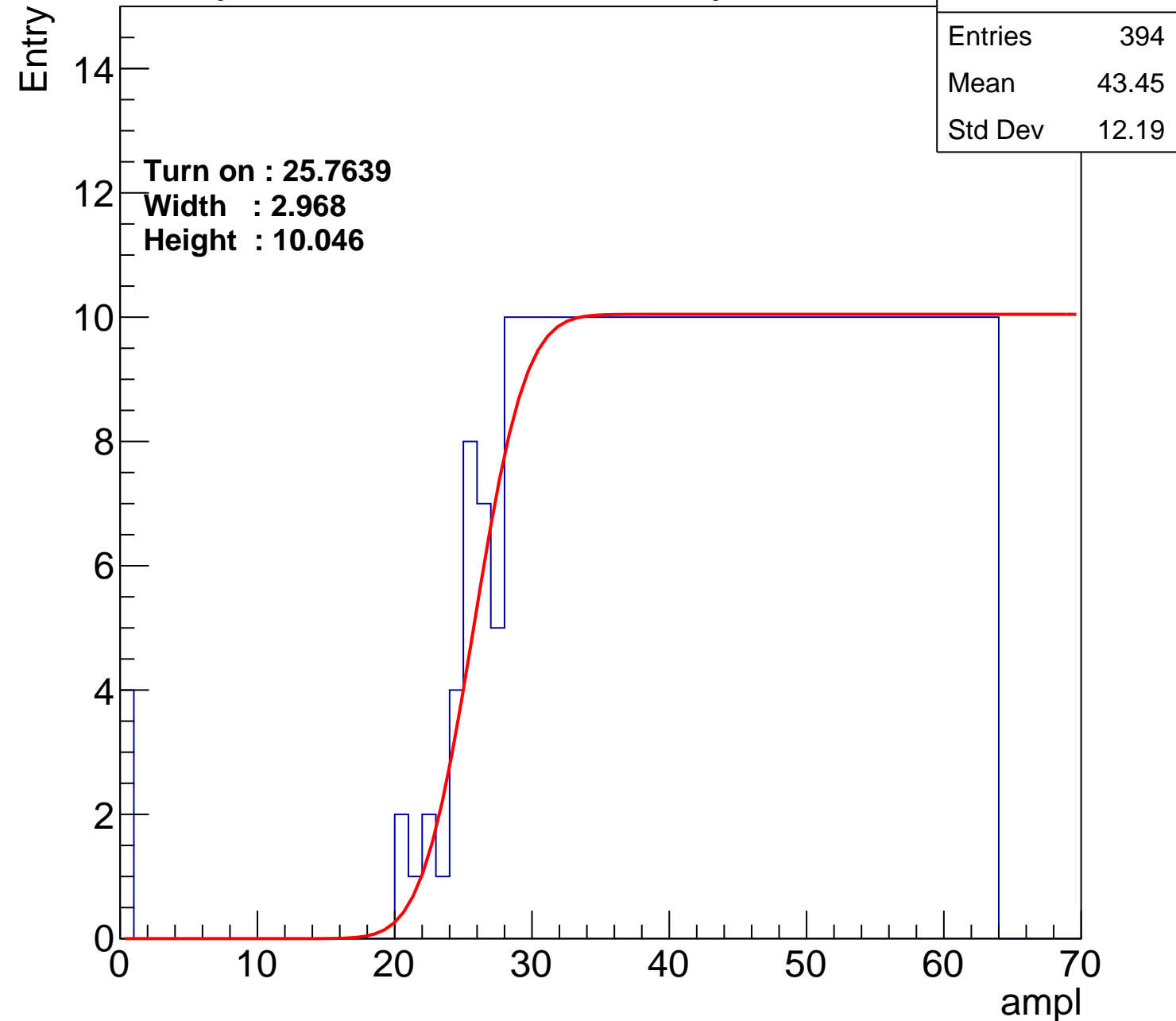
Width : 2.968

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch47

calib_packv5_042523_0143.root, FC#11, port A2

Entries	376
Mean	44.4
Std Dev	11.58

Turn on : 26.4640

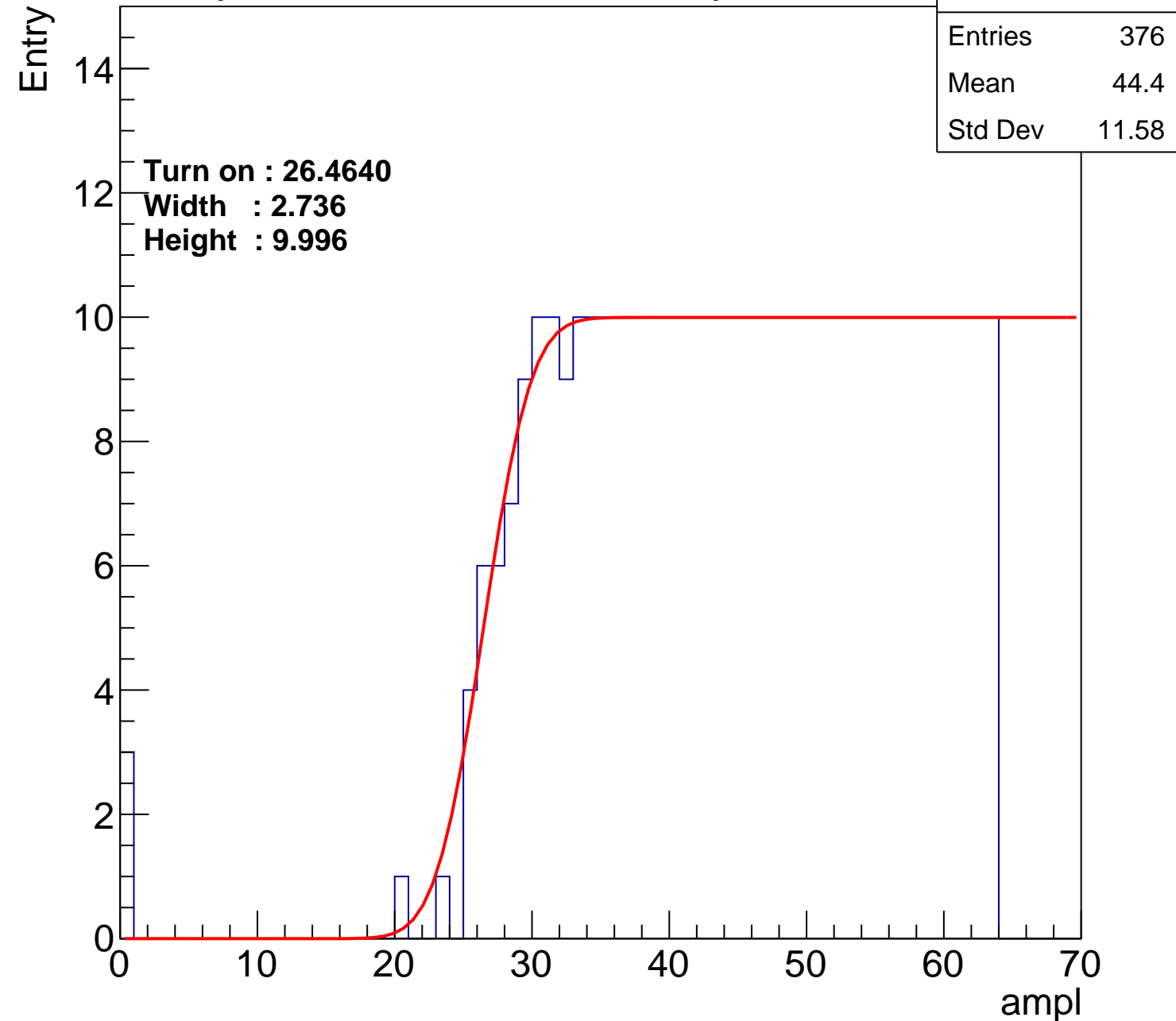
Width : 2.736

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch48

calib_packv5_042523_0143.root, FC#11, port A2

Entries	399
Mean	43.19
Std Dev	12.33

Turn on : 24.7463

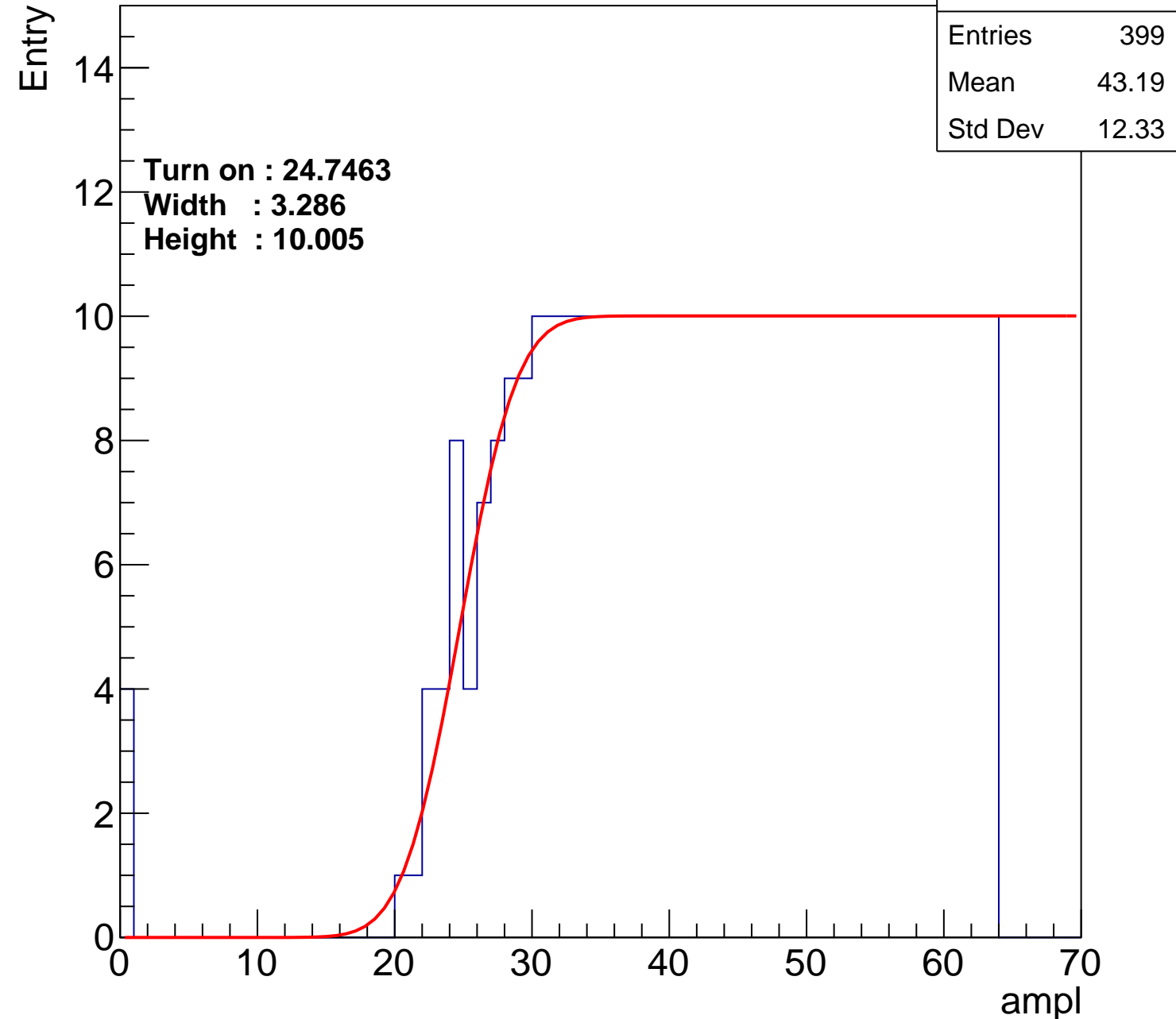
Width : 3.286

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch49

calib_packv5_042523_0143.root, FC#11, port A2

Entries	363
Mean	45.02
Std Dev	11.29

Turn on : 28.2714

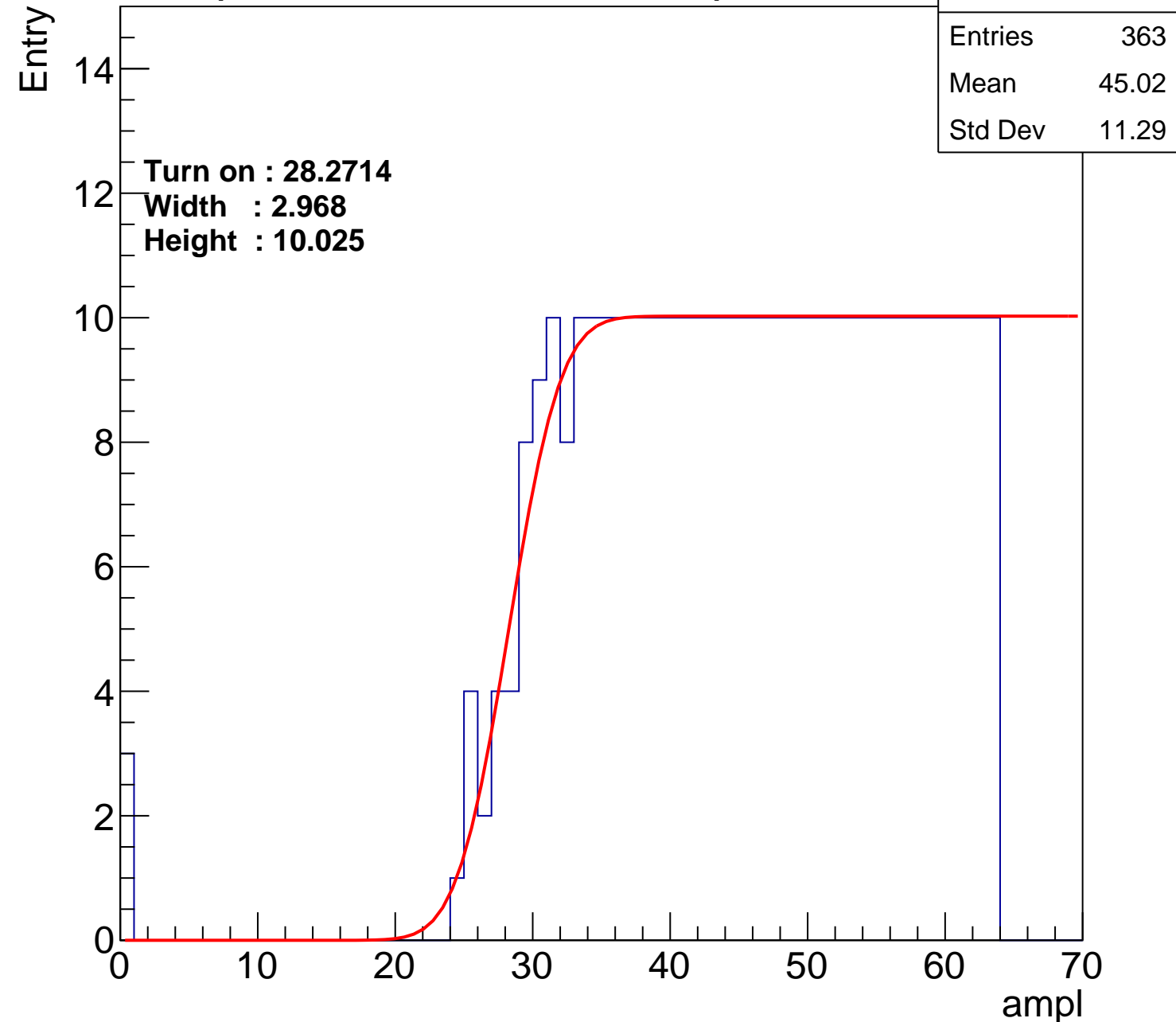
Width : 2.968

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch50

calib_packv5_042523_0143.root, FC#11, port A2

Entries	377
Mean	44.46
Std Dev	11.28

Turn on : 26.5741

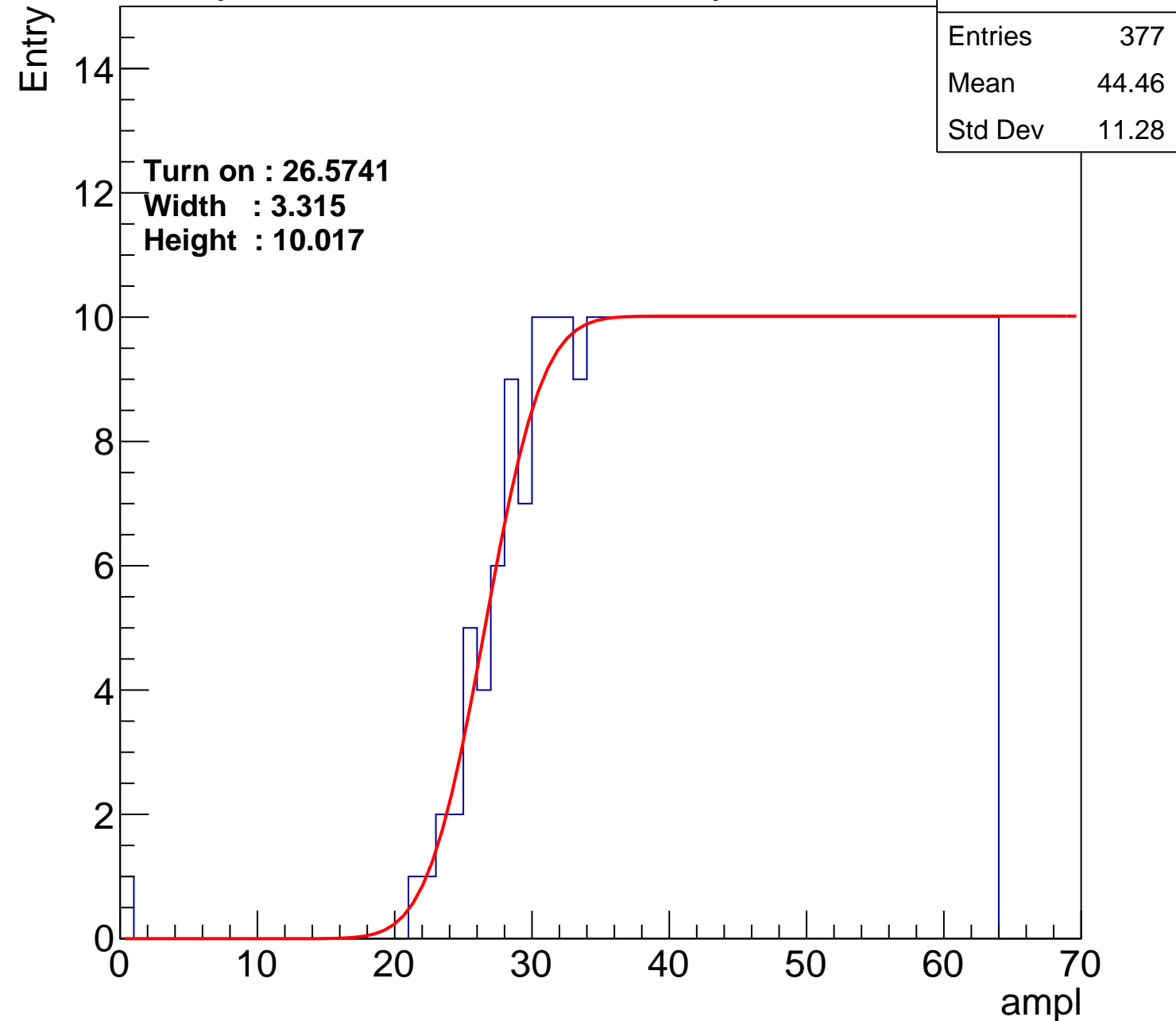
Width : 3.315

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch51

calib_packv5_042523_0143.root, FC#11, port A2

Entries	398
Mean	43.39
Std Dev	11.96

Turn on : 24.1479

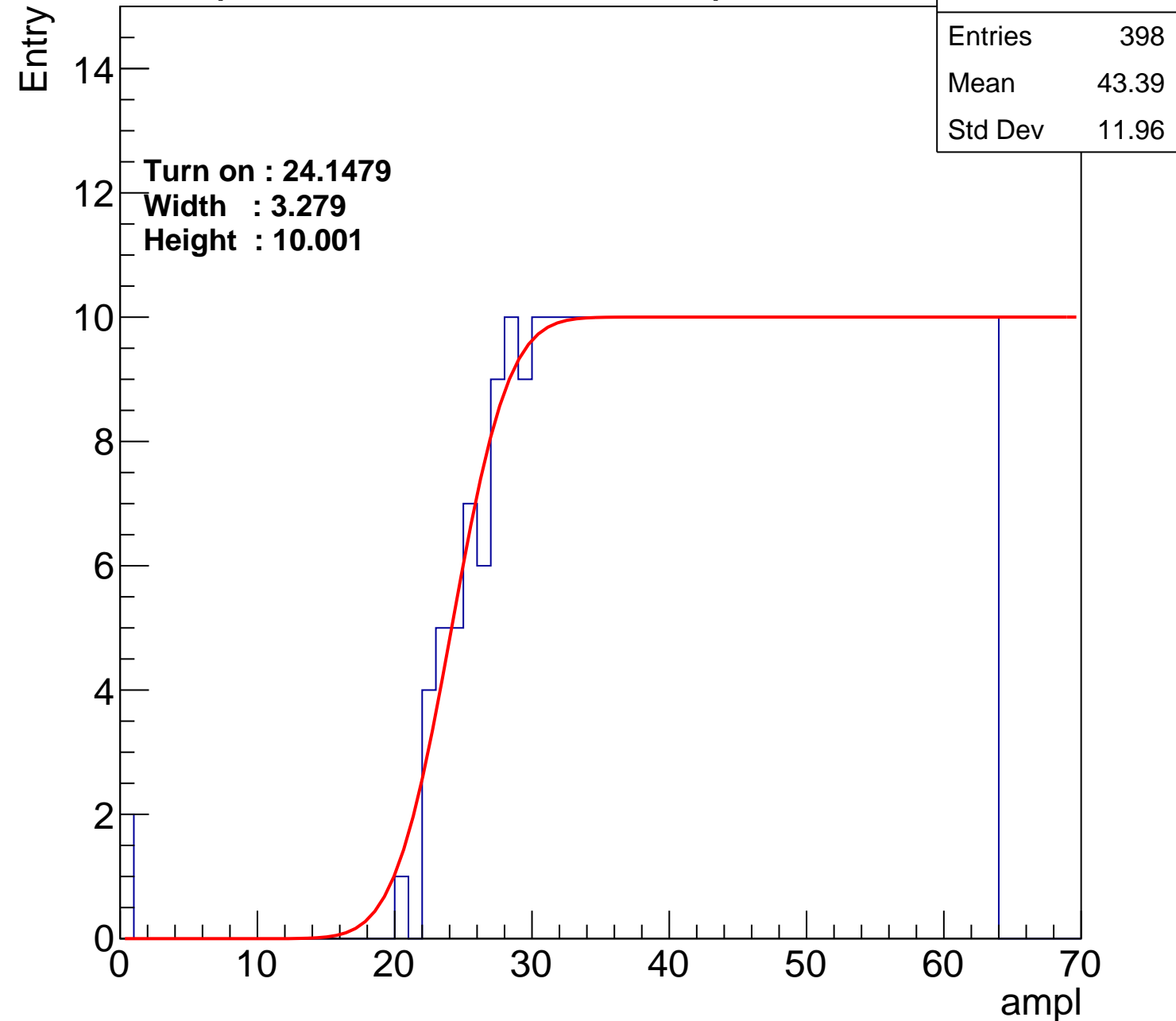
Width : 3.279

Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch52

calib_packv5_042523_0143.root, FC#11, port A2

Entries	398
Mean	43.31
Std Dev	12.16

Turn on : 24.8792

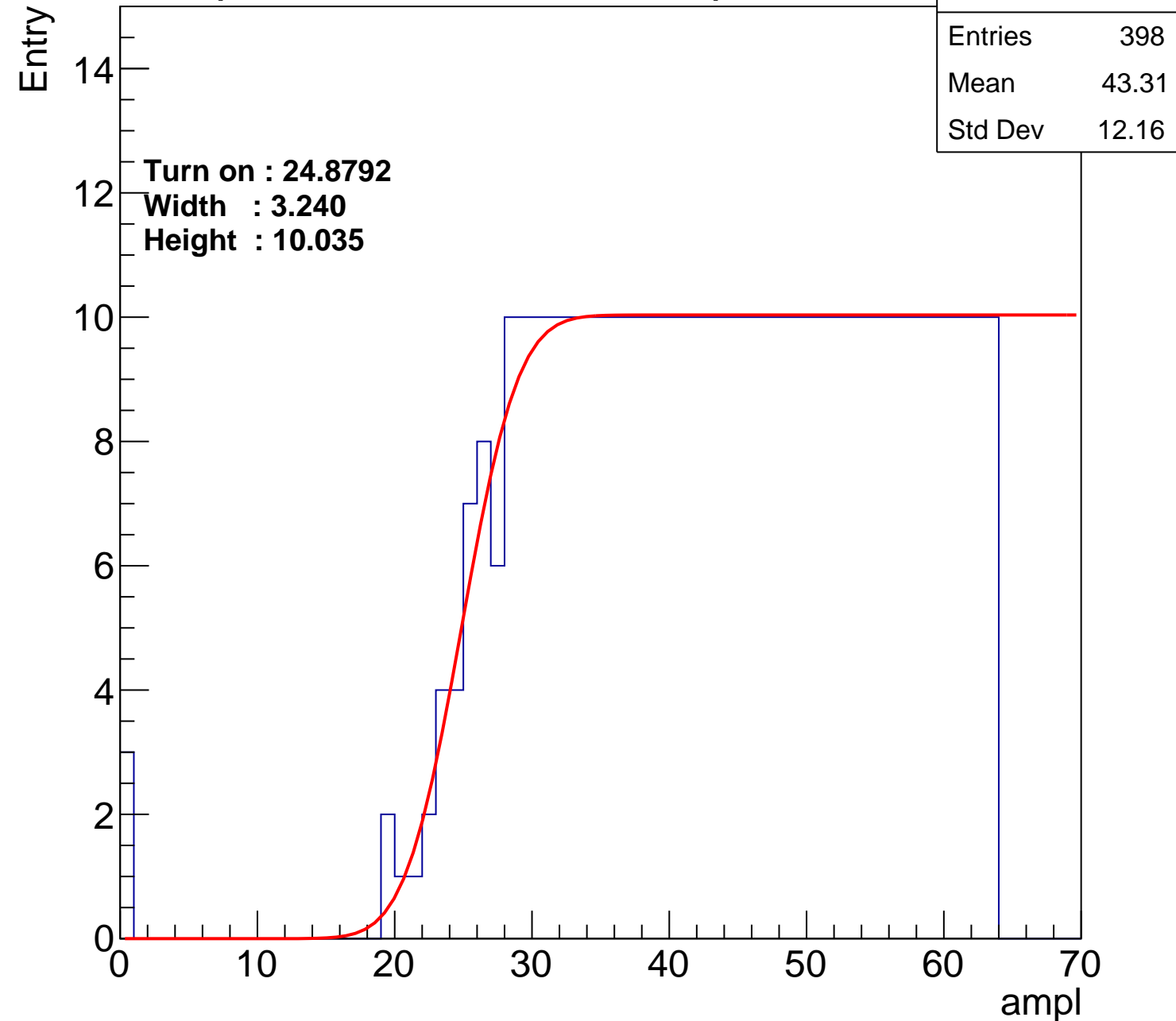
Width : 3.240

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch53

calib_packv5_042523_0143.root, FC#11, port A2

Entries	395
Mean	43.55
Std Dev	11.81

Turn on : 25.5642

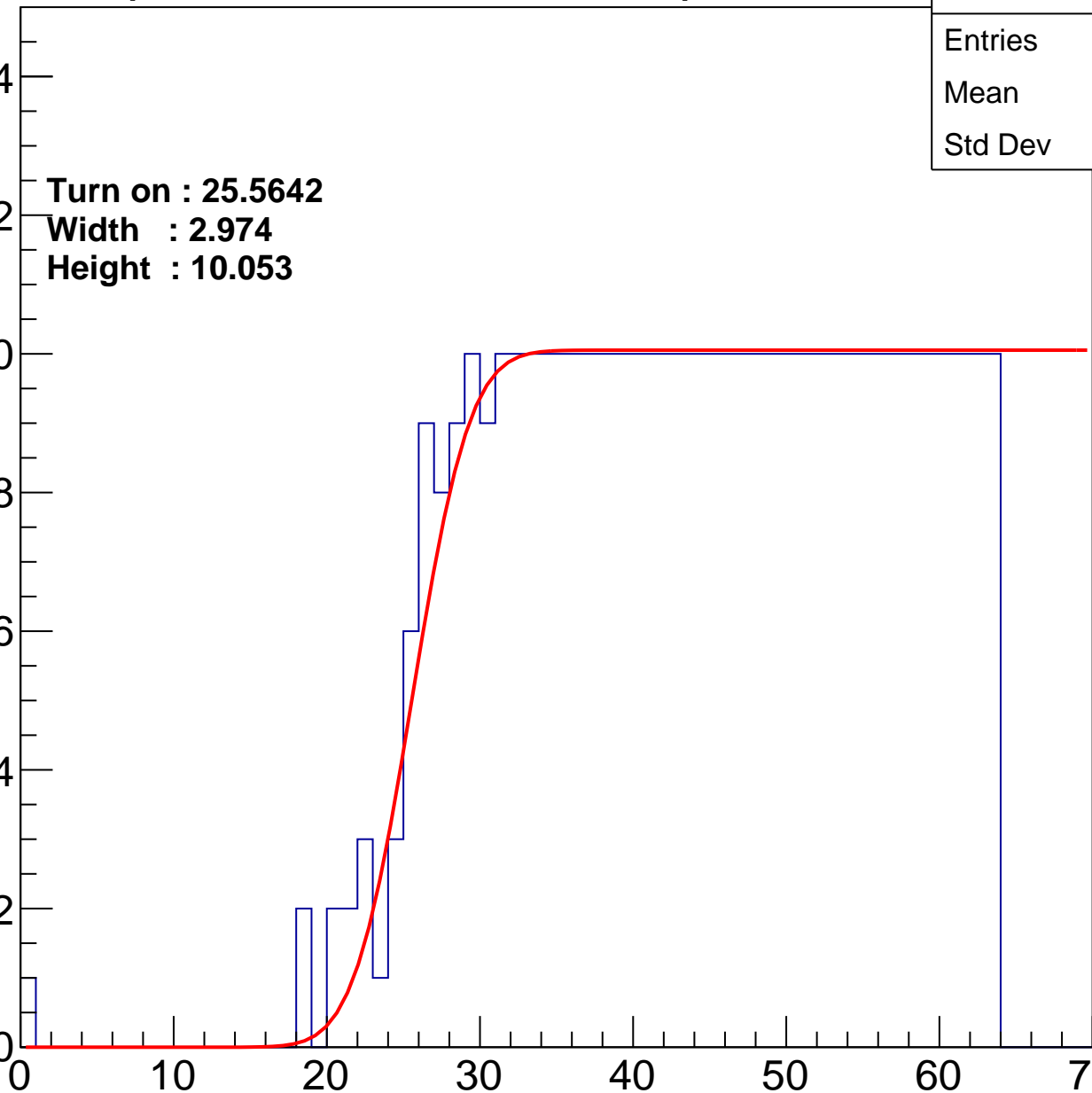
Width : 2.974

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch54

calib_packv5_042523_0143.root, FC#11, port A2

Entries	384
Mean	43.98
Std Dev	11.81

Turn on : 25.9904

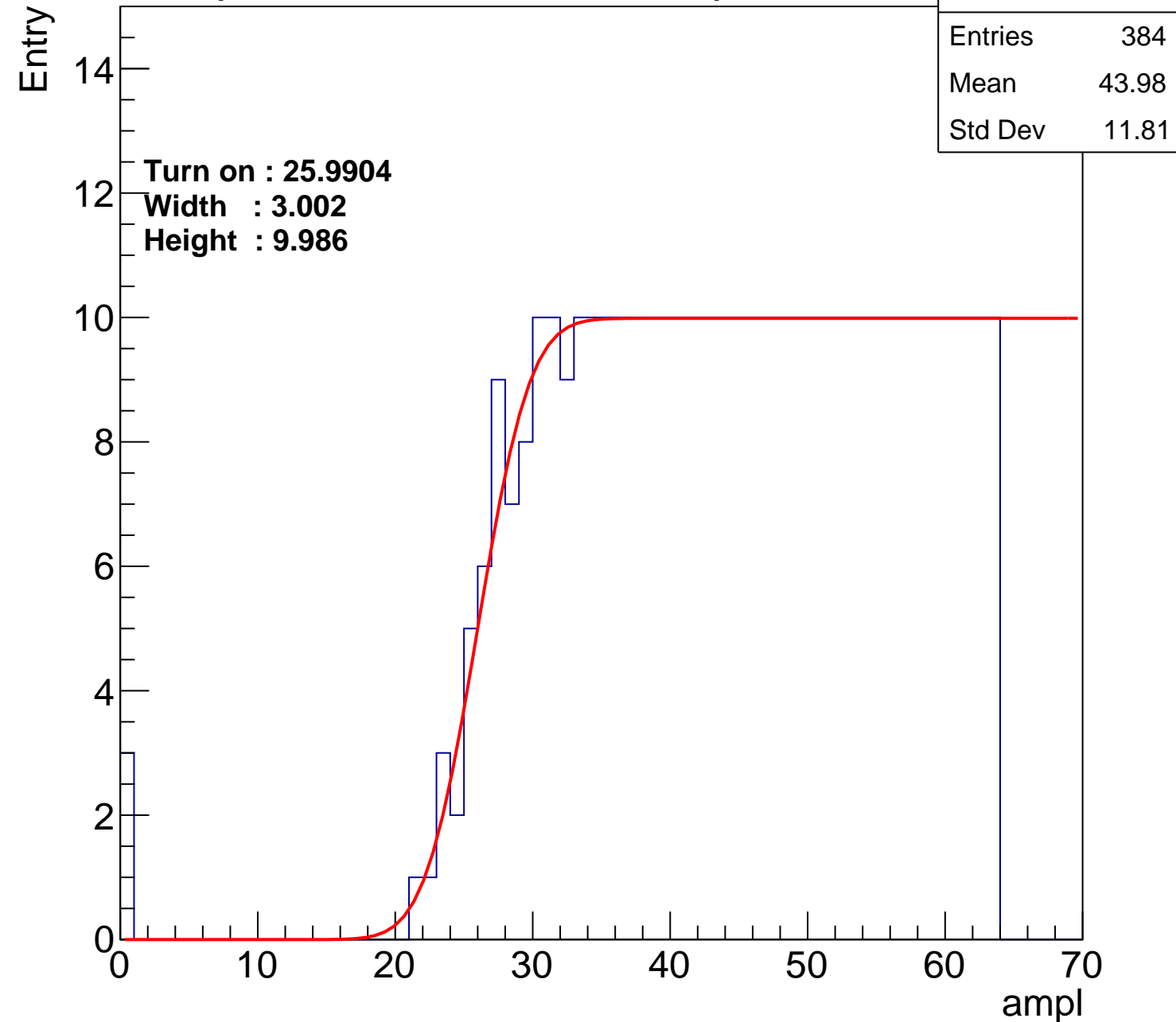
Width : 3.002

Height : 9.986

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch55

calib_packv5_042523_0143.root, FC#11, port A2

Entries	395
Mean	43.54
Std Dev	11.82

Turn on : 25.5315

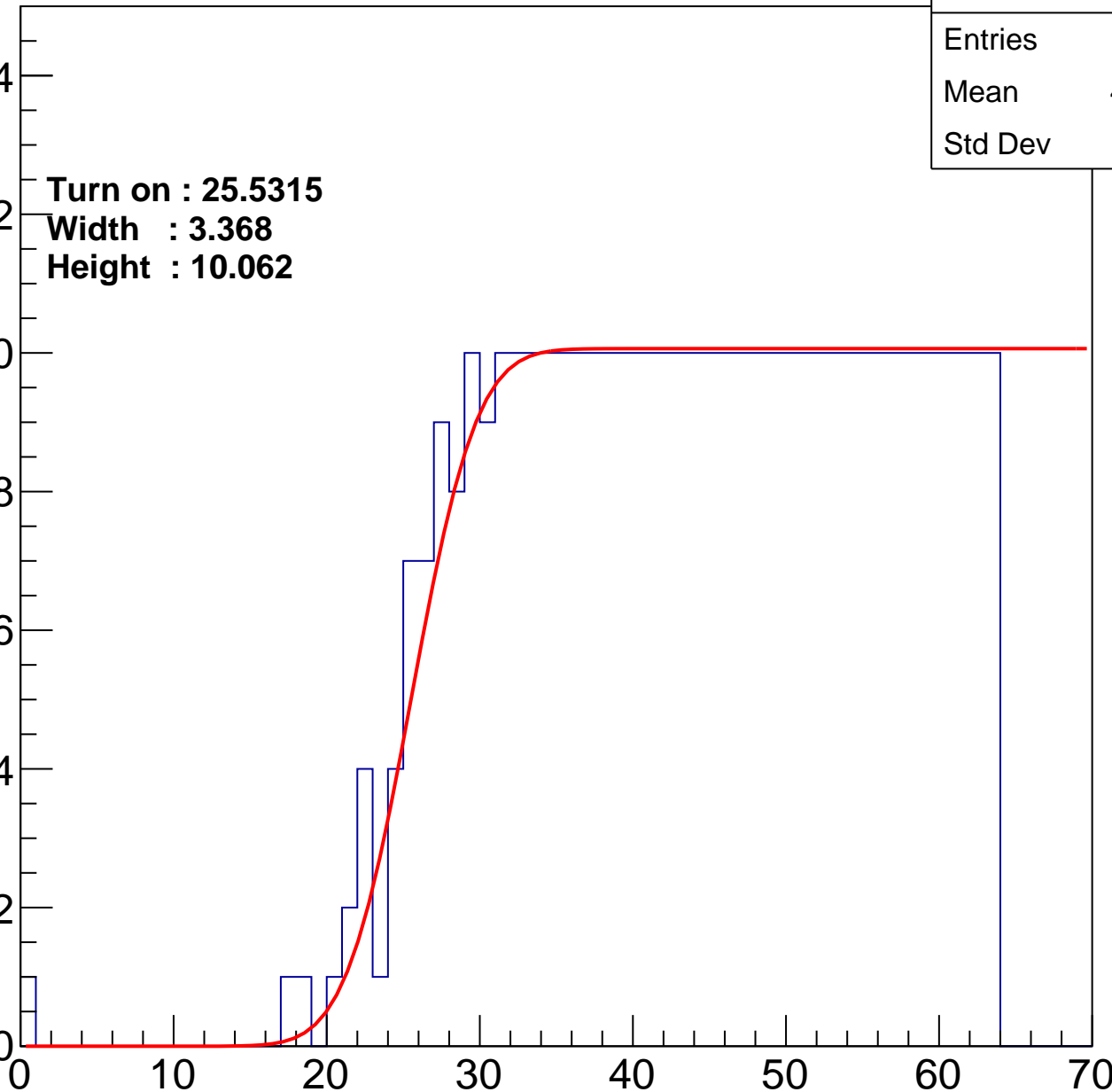
Width : 3.368

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch56

calib_packv5_042523_0143.root, FC#11, port A2

Entries	389
Mean	43.81
Std Dev	11.77

Turn on : 26.1594

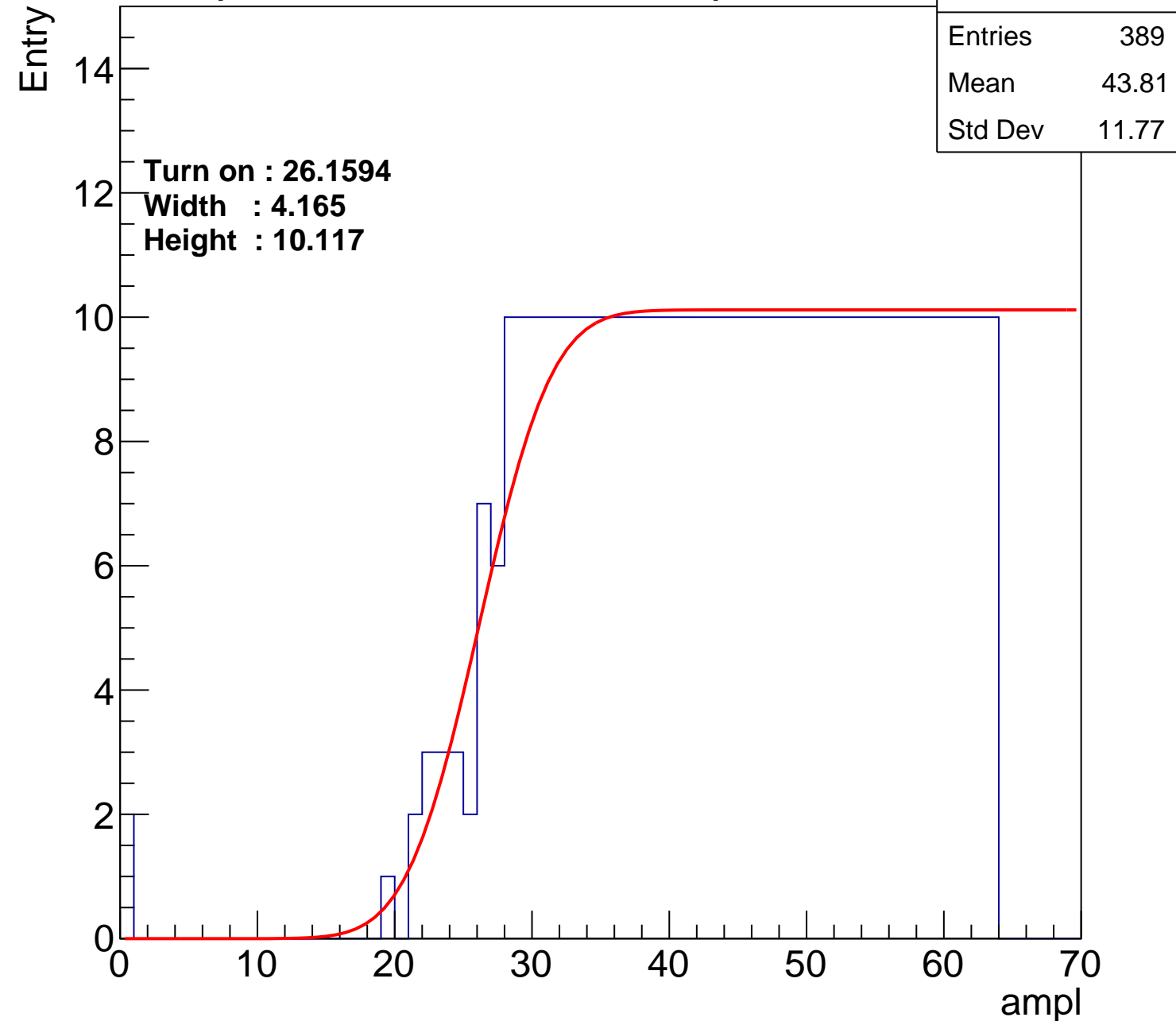
Width : 4.165

Height : 10.117

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch57

calib_packv5_042523_0143.root, FC#11, port A2

Entries	390
Mean	43.78
Std Dev	11.75

Turn on : 25.4457

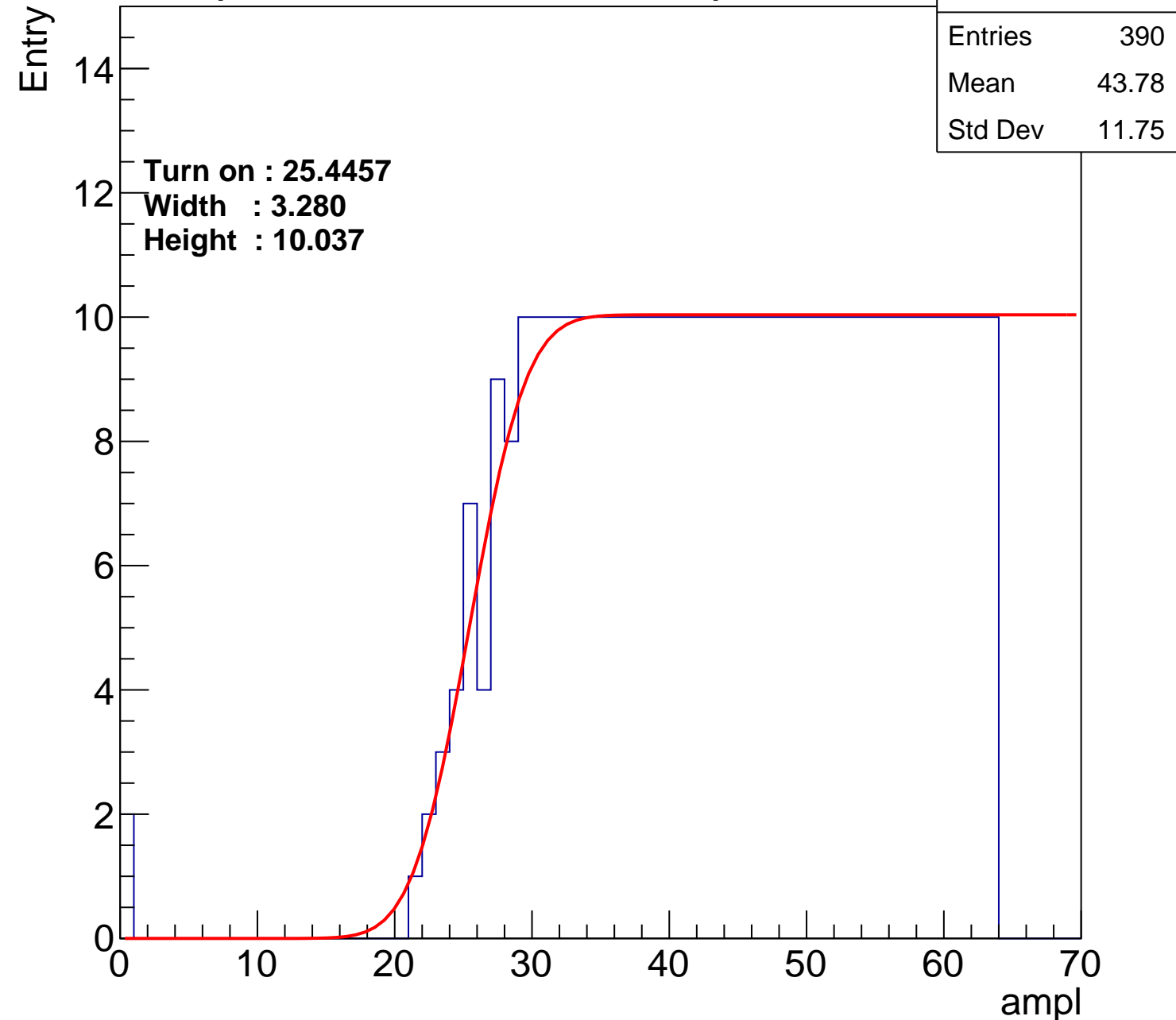
Width : 3.280

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch58

calib_packv5_042523_0143.root, FC#11, port A2

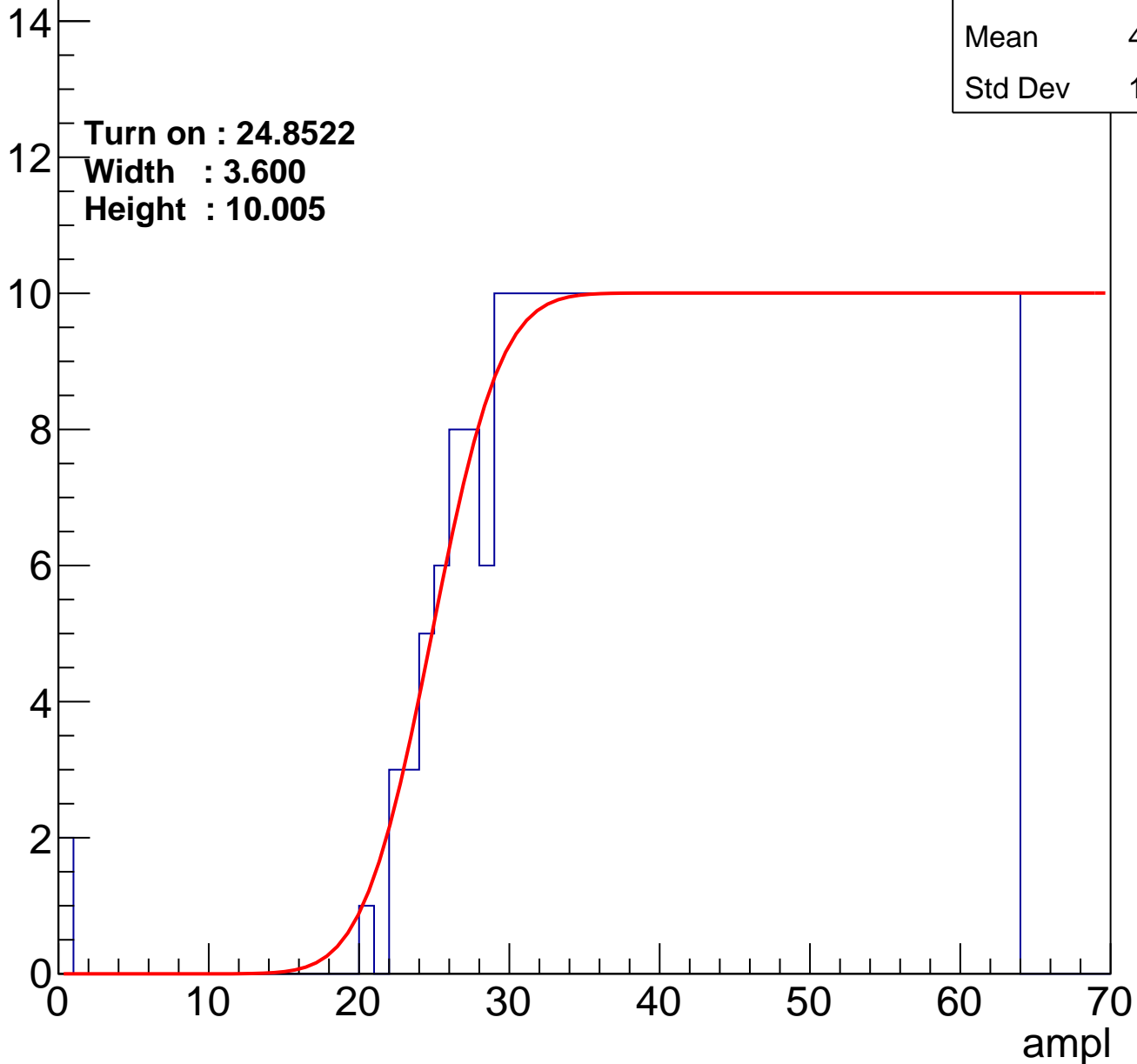
Entries	392
Mean	43.67
Std Dev	11.83

Turn on : 24.8522

Width : 3.600

Height : 10.005

Entry



B1L102S, U1-ch59

calib_packv5_042523_0143.root, FC#11, port A2

Entries	400
Mean	43.29
Std Dev	12.01

Turn on : 24.3966

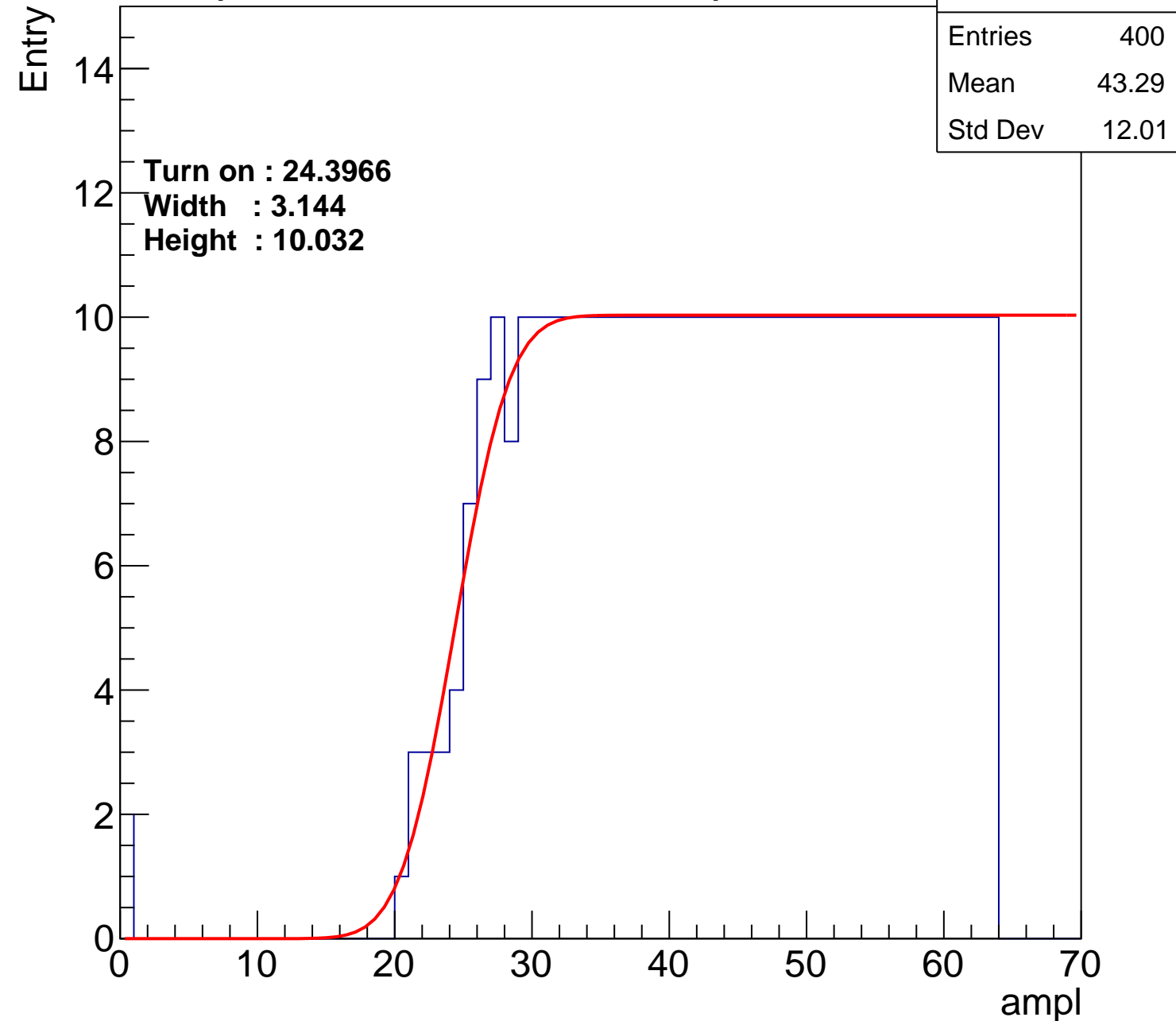
Width : 3.144

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch60

calib_packv5_042523_0143.root, FC#11, port A2

Entries	395
Mean	43.39
Std Dev	12.24

Turn on : 25.0436

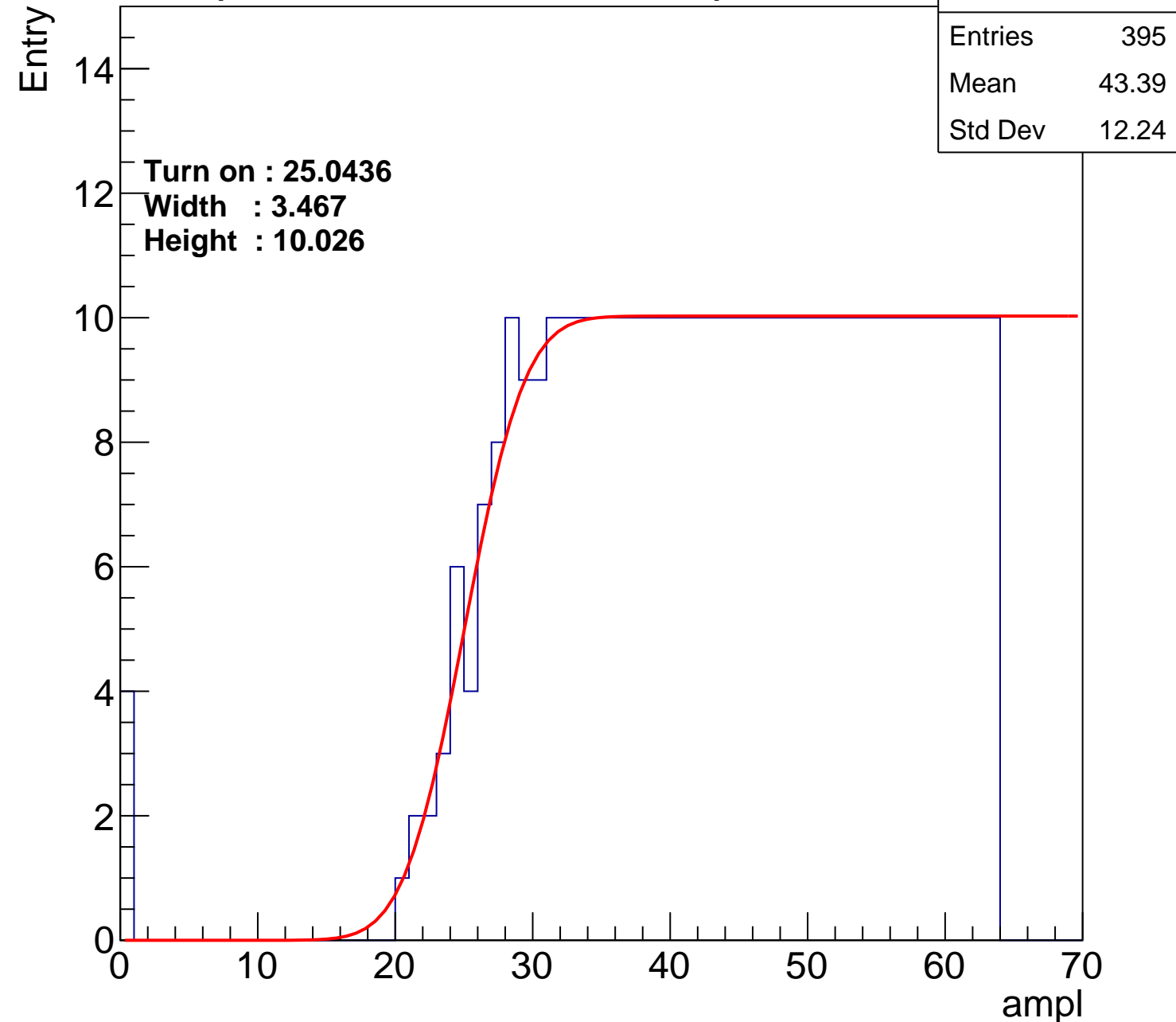
Width : 3.467

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch61

calib_packv5_042523_0143.root, FC#11, port A2

Entries	358
Mean	45.34
Std Dev	10.97

Turn on : 28.5092

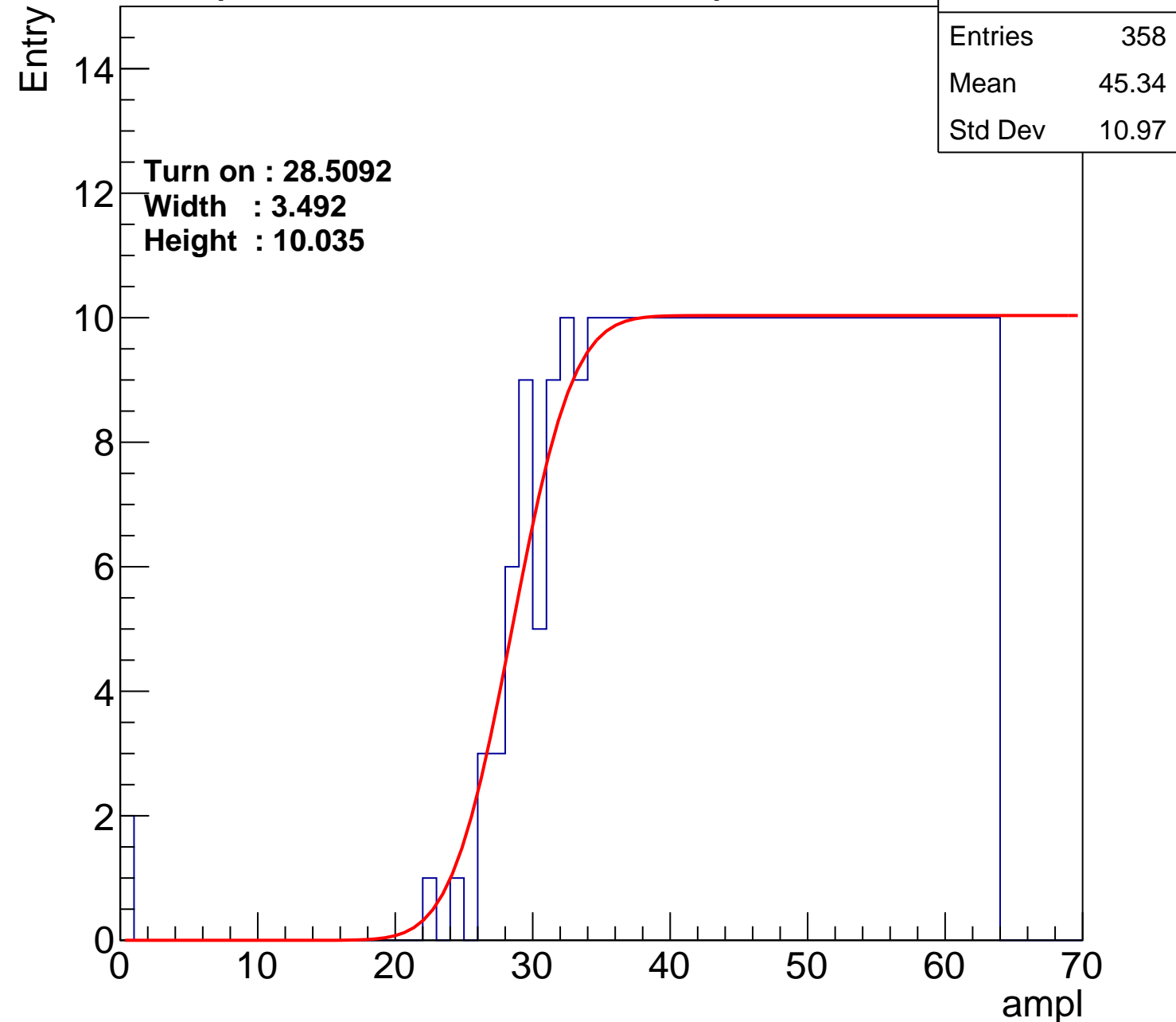
Width : 3.492

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch62

calib_packv5_042523_0143.root, FC#11, port A2

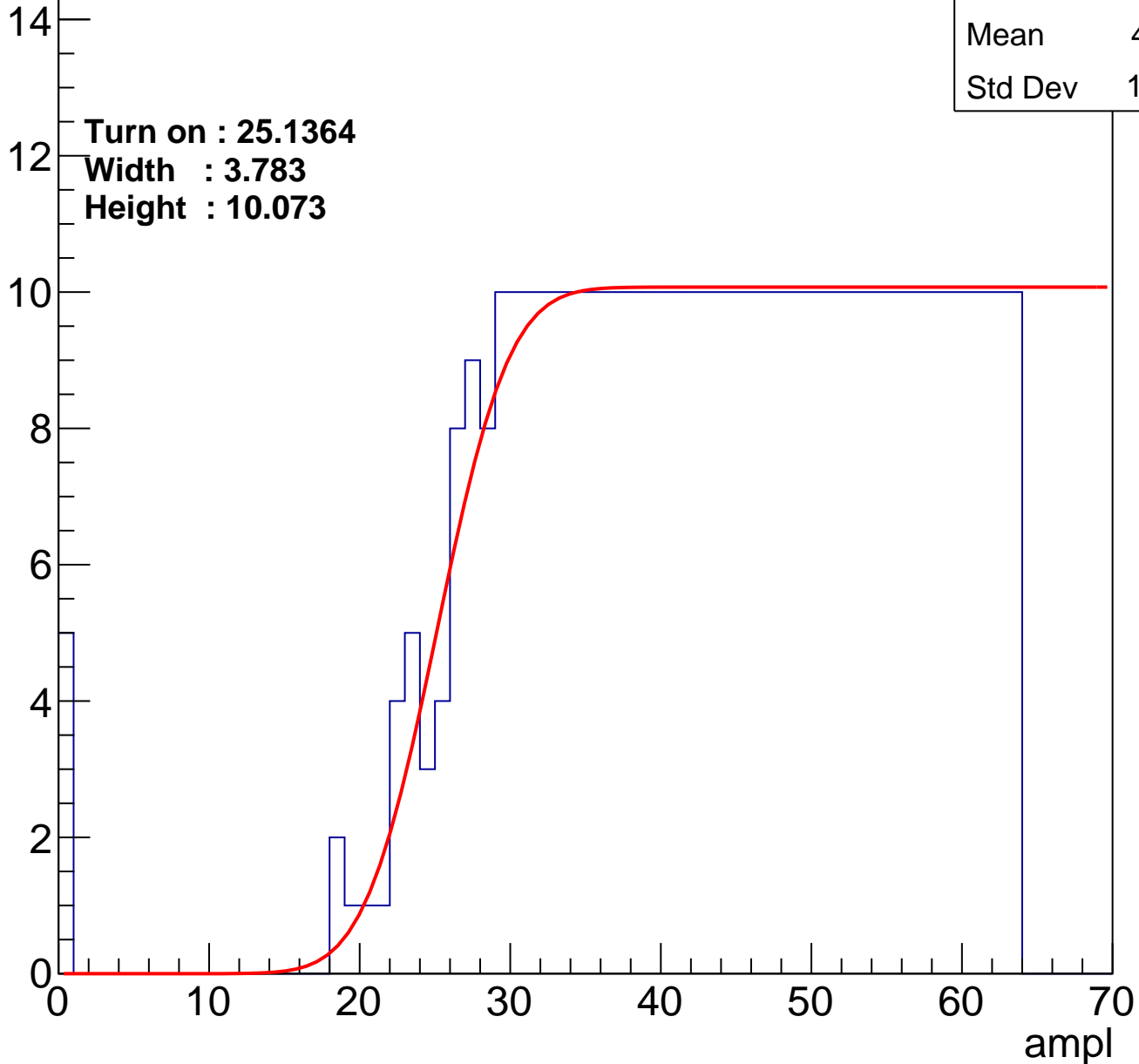
Entries	401
Mean	43.01
Std Dev	12.58

Turn on : 25.1364

Width : 3.783

Height : 10.073

Entry



B1L102S, U1-ch63

calib_packv5_042523_0143.root, FC#11, port A2

Entries	378
Mean	44.42
Std Dev	11.29

Turn on : 27.3018

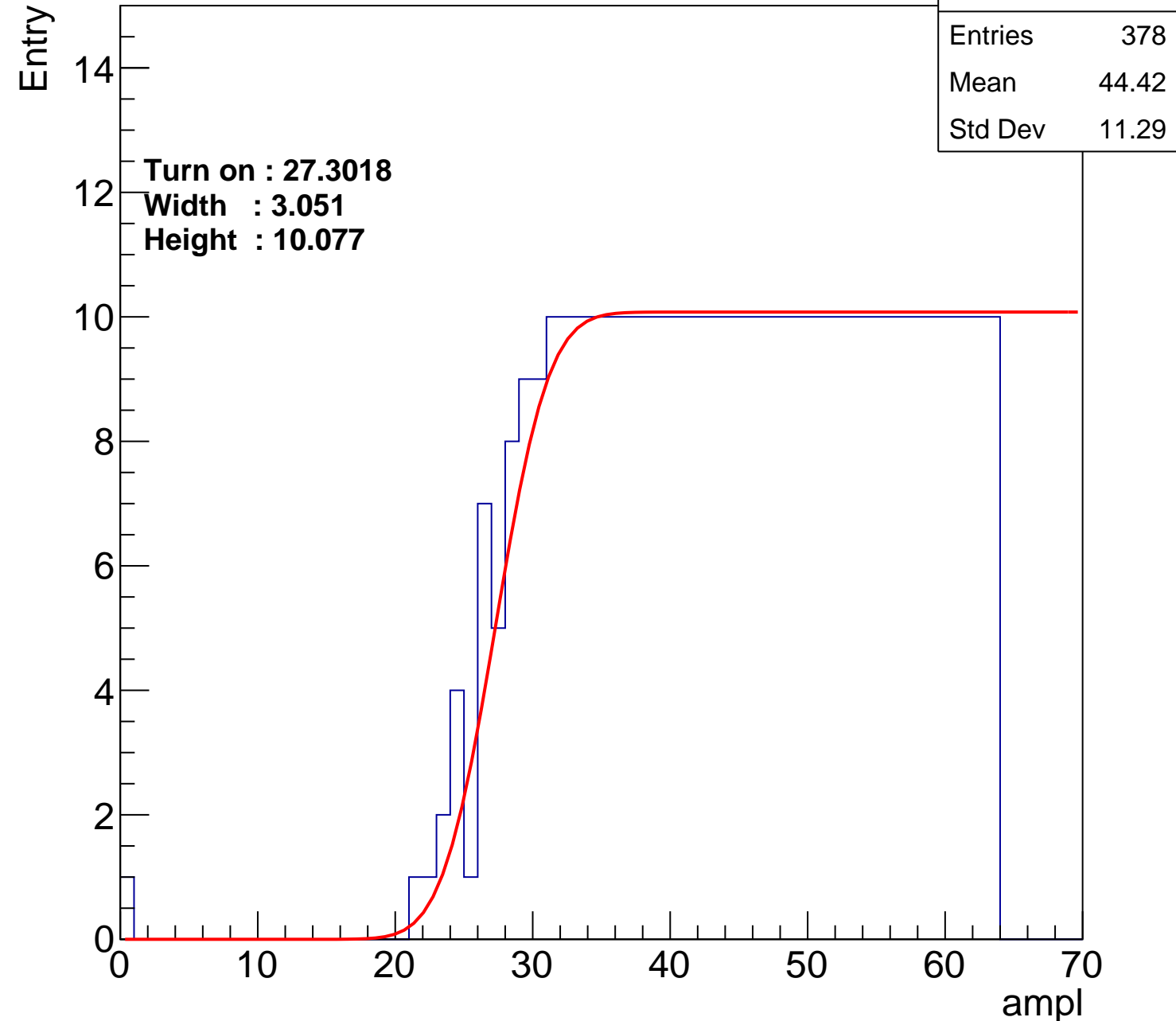
Width : 3.051

Height : 10.077

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch64

calib_packv5_042523_0143.root, FC#11, port A2

Entries	401
Mean	42.91
Std Dev	12.83

Turn on : 25.3578

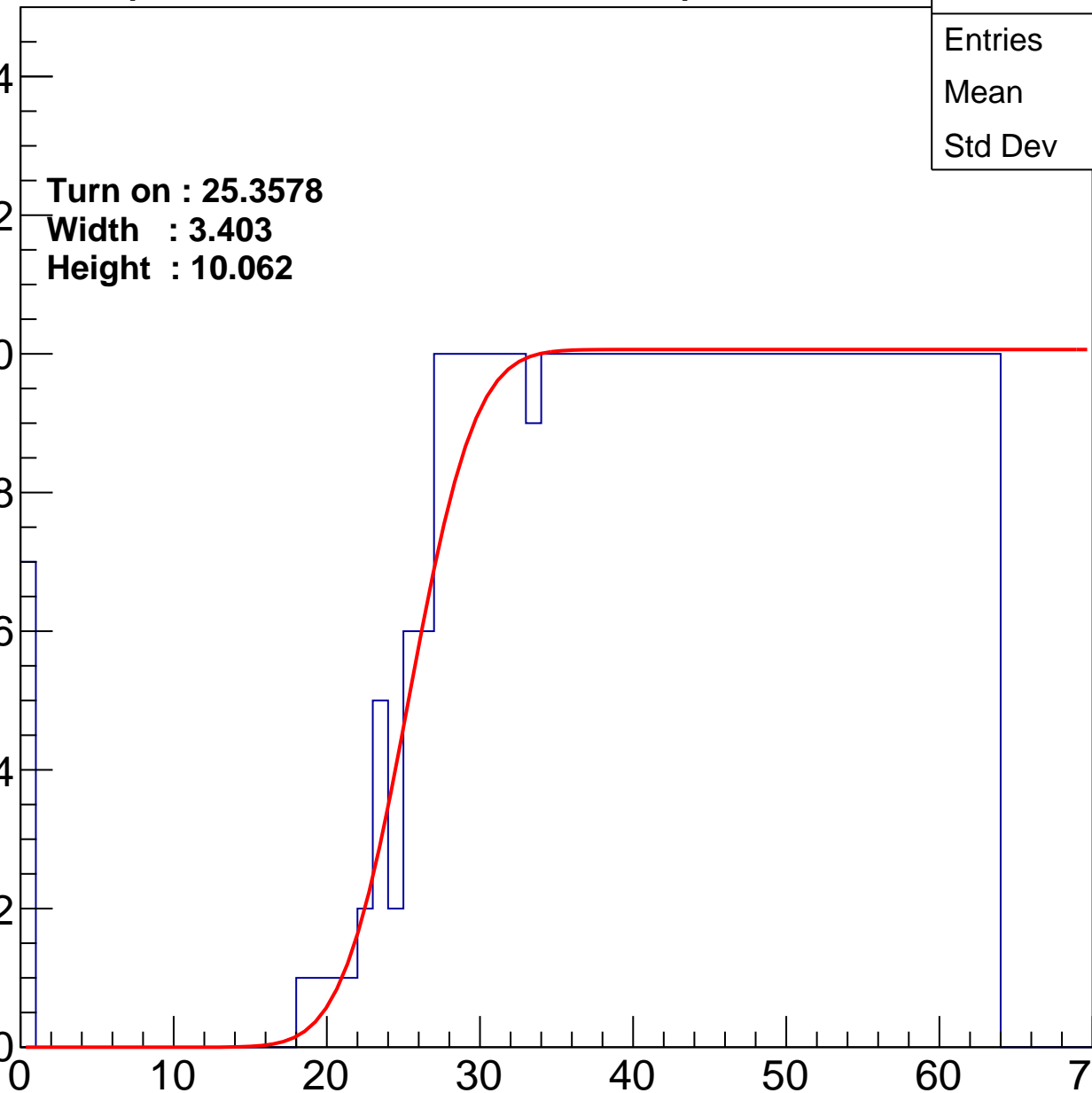
Width : 3.403

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch65

calib_packv5_042523_0143.root, FC#11, port A2

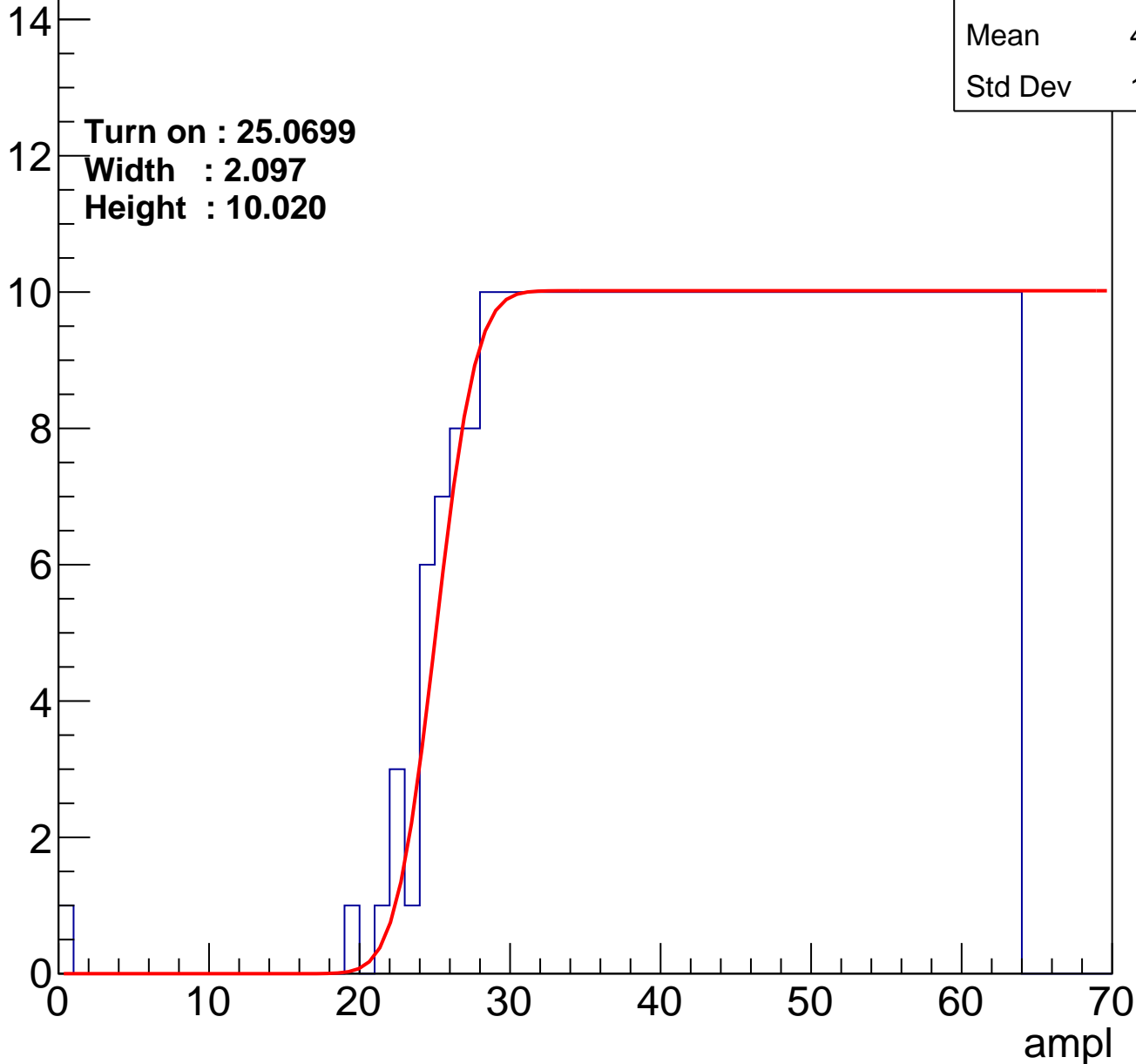
Entries	396
Mean	43.57
Std Dev	11.72

Turn on : 25.0699

Width : 2.097

Height : 10.020

Entry



B1L102S, U1-ch66

calib_packv5_042523_0143.root, FC#11, port A2

Entries	413
Mean	42.5
Std Dev	12.7

Turn on : 23.7571

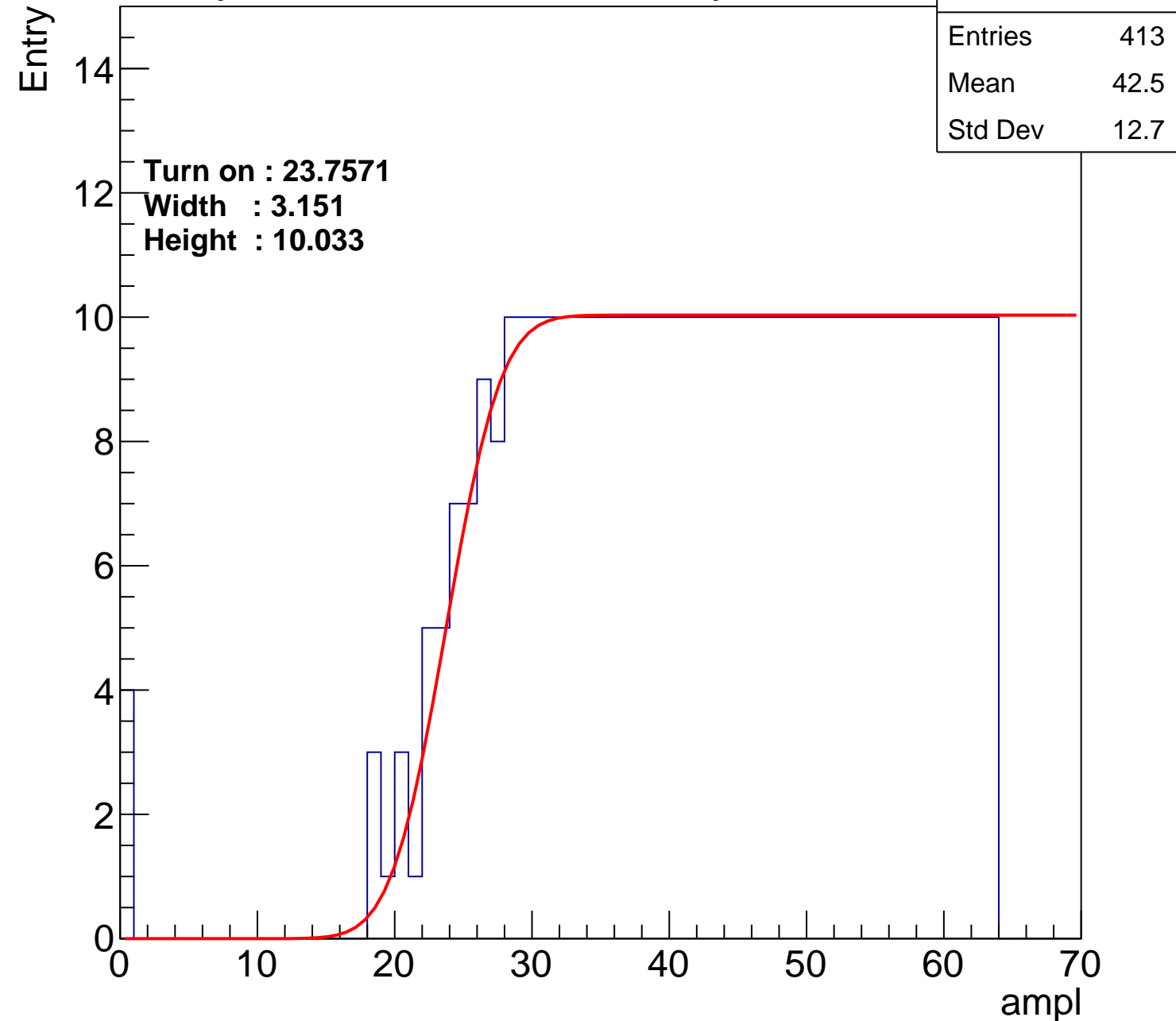
Width : 3.151

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch67

calib_packv5_042523_0143.root, FC#11, port A2

Entries	375
Mean	44.36
Std Dev	11.78

Turn on : 26.8447

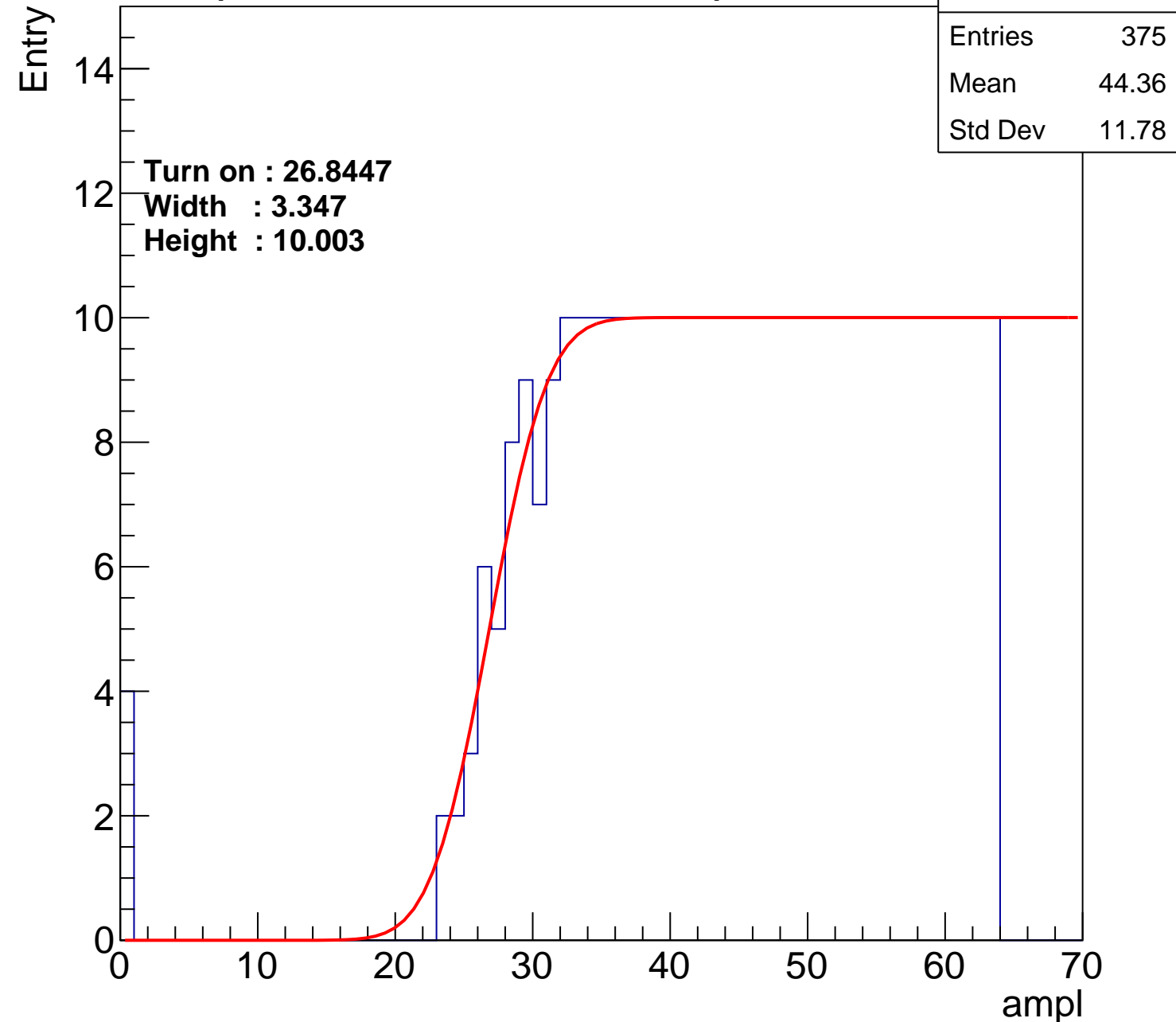
Width : 3.347

Height : 10.003

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch68

calib_packv5_042523_0143.root, FC#11, port A2

Entries	380
Mean	44.16
Std Dev	11.68

Turn on : 26.6156

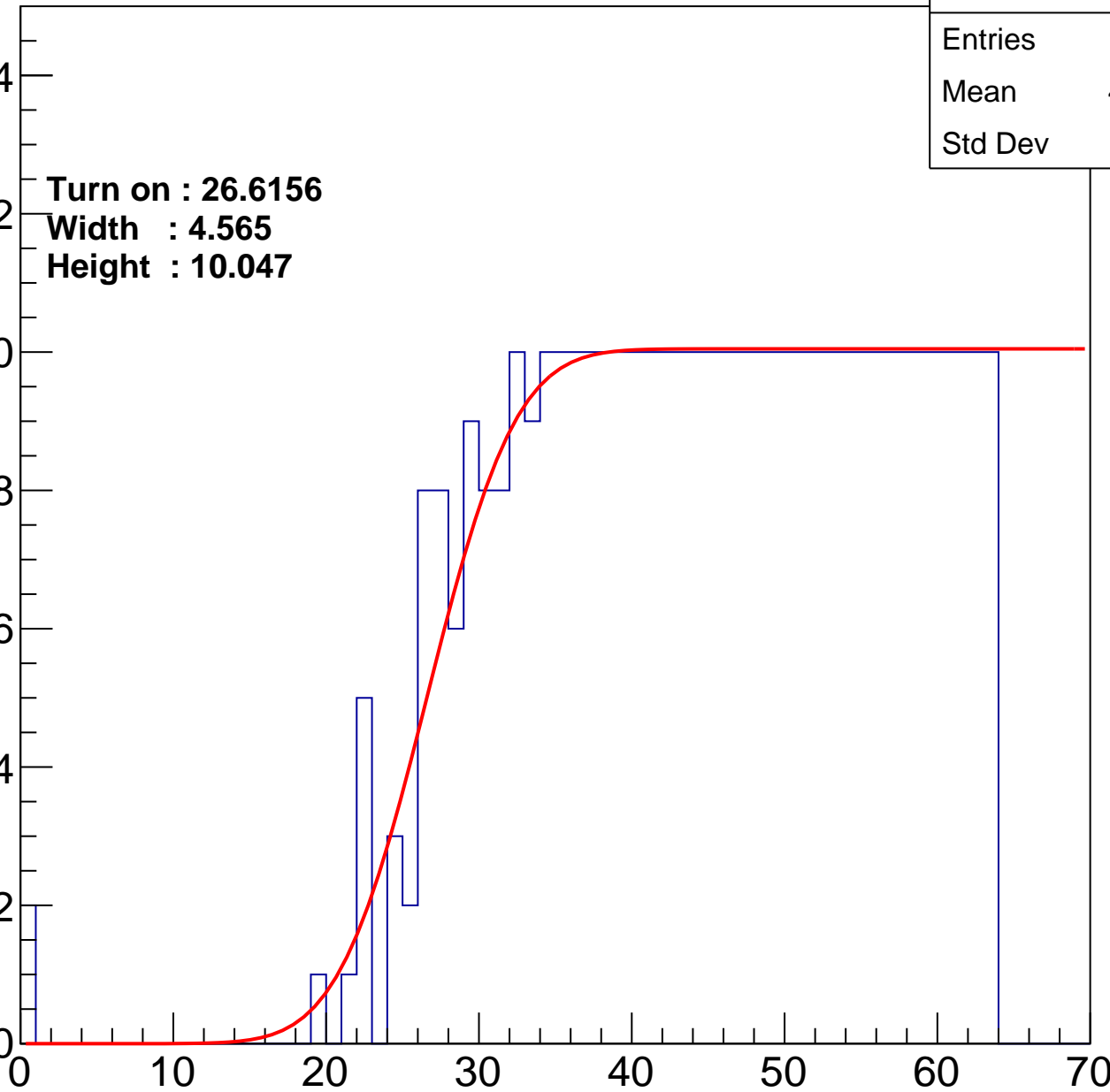
Width : 4.565

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch69

calib_packv5_042523_0143.root, FC#11, port A2

Entries	406
Mean	42.93
Std Dev	12.32

Turn on : 23.6329

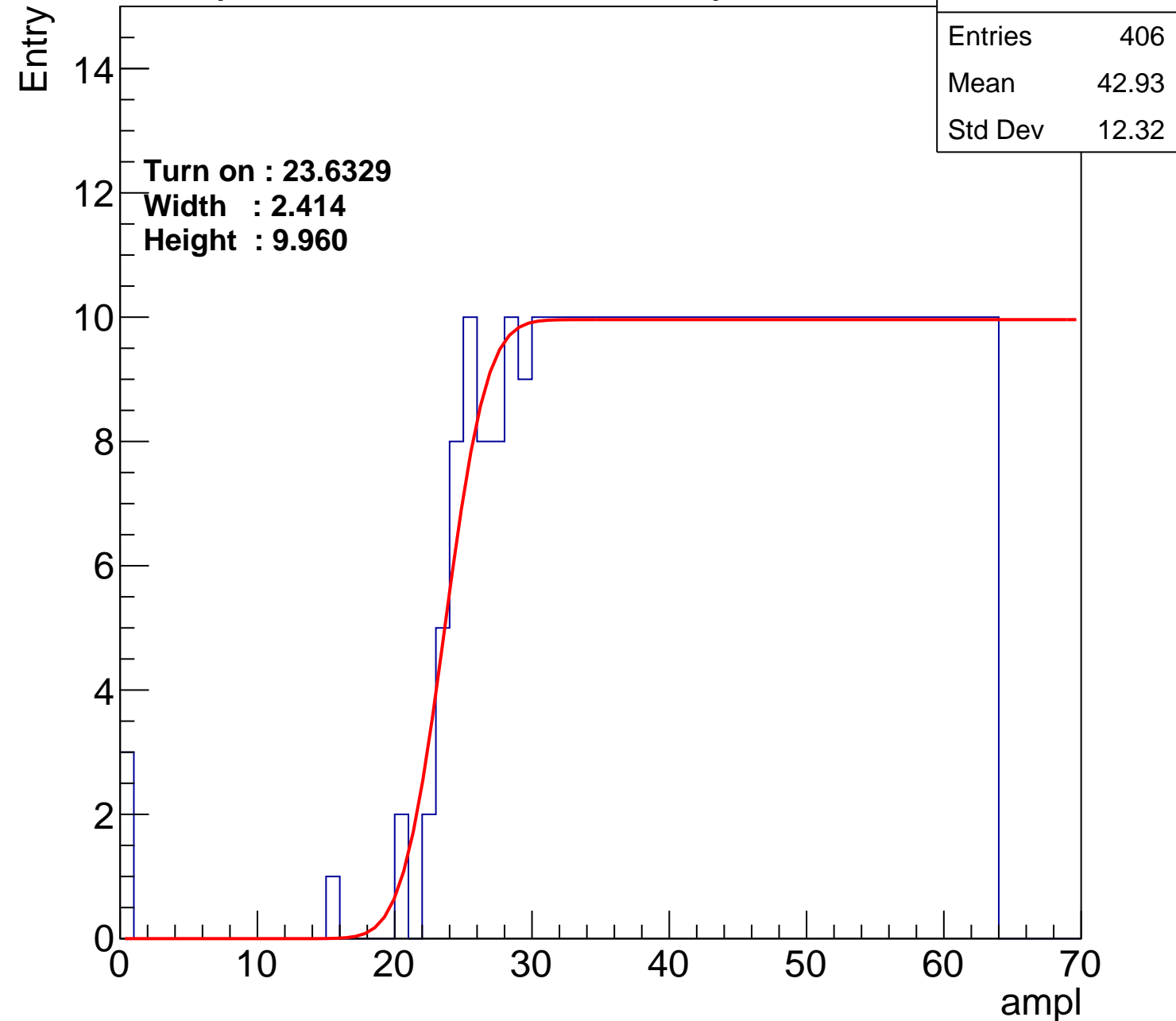
Width : 2.414

Height : 9.960

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch70

calib_packv5_042523_0143.root, FC#11, port A2

Entries	383
Mean	44.13
Std Dev	11.57

Turn on : 25.8519

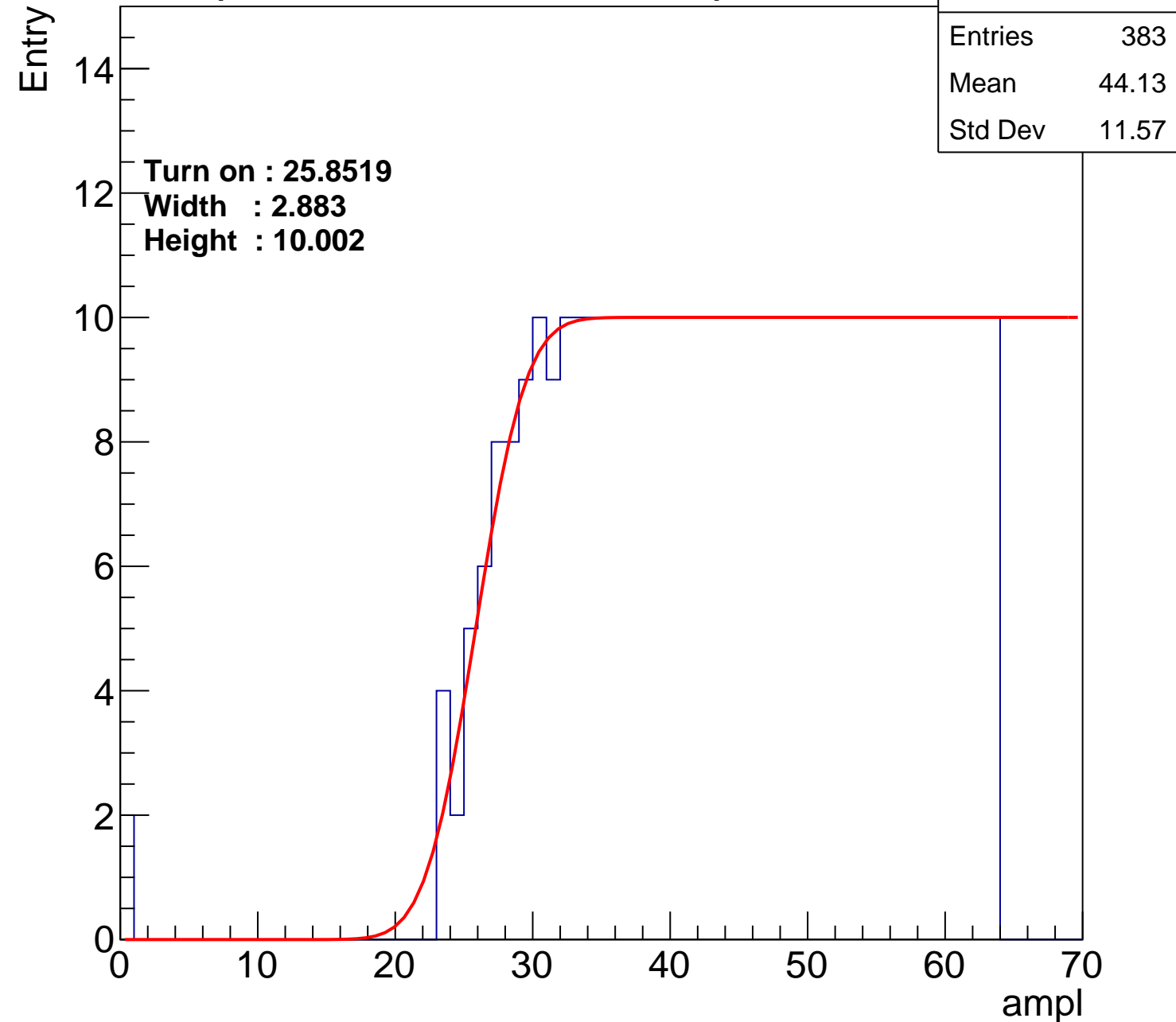
Width : 2.883

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch71

calib_packv5_042523_0143.root, FC#11, port A2

Entries	389
Mean	43.84
Std Dev	11.72

Turn on : 25.4509

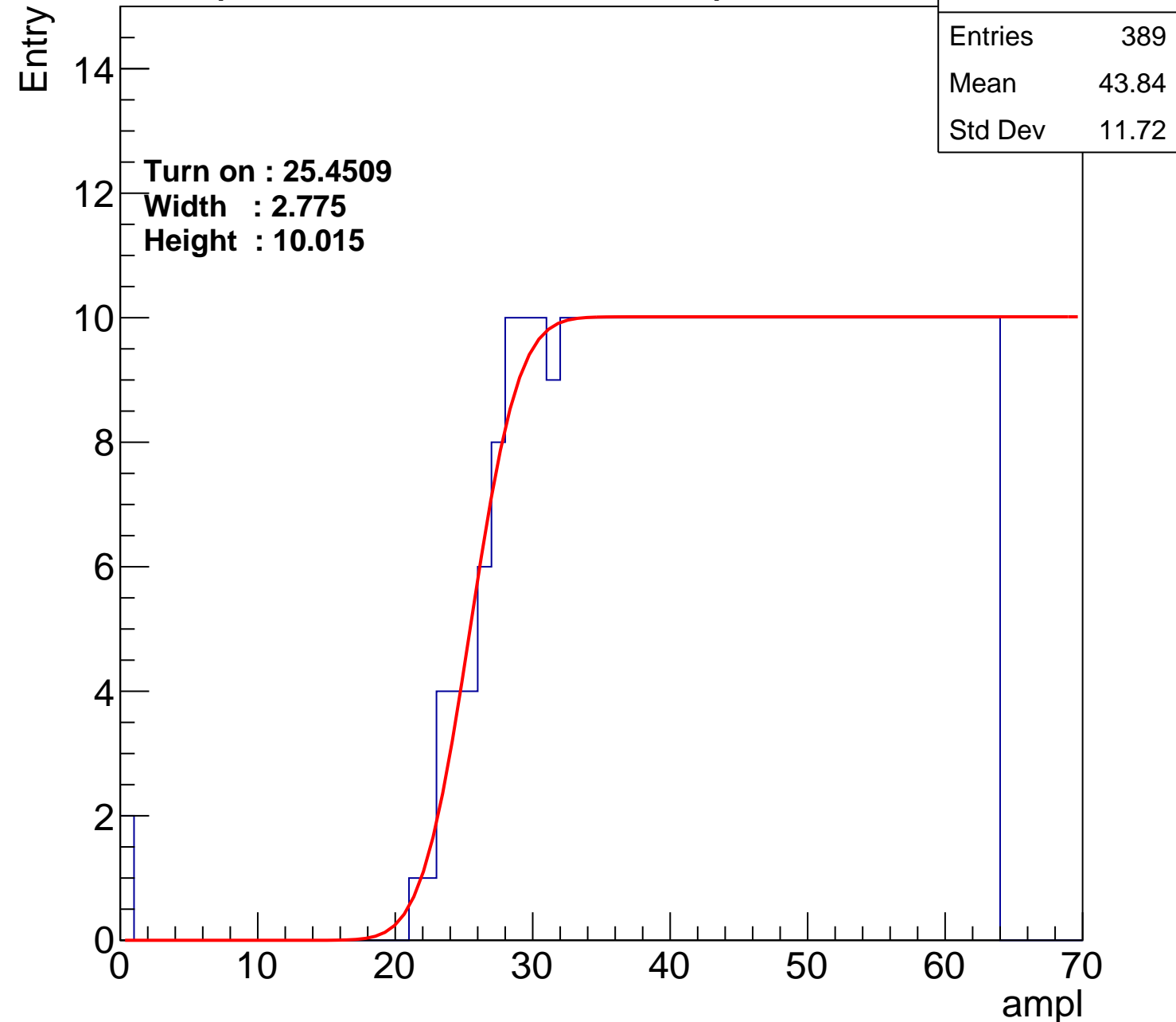
Width : 2.775

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch72

calib_packv5_042523_0143.root, FC#11, port A2

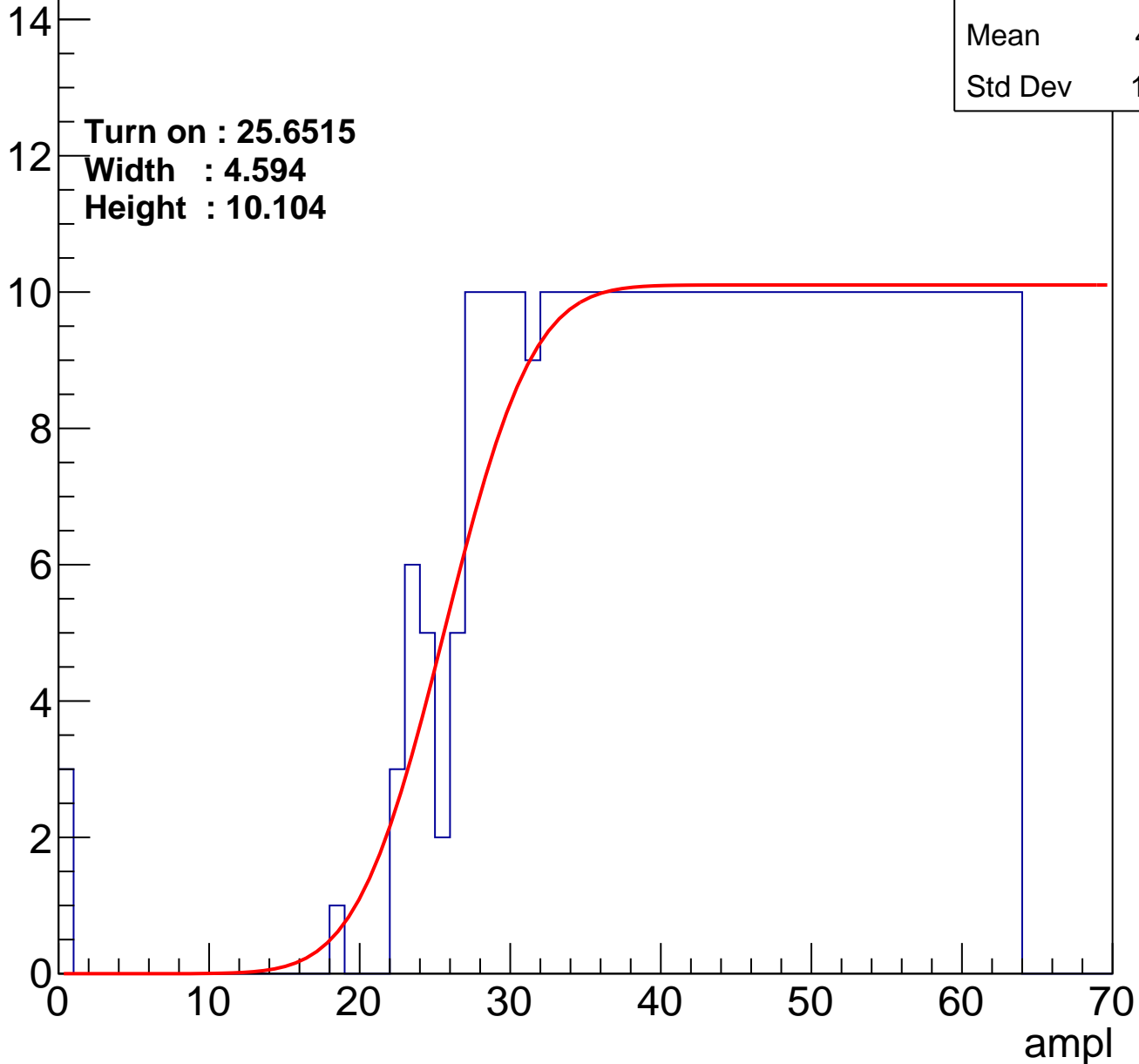
Entries	394
Mean	43.51
Std Dev	12.05

Turn on : 25.6515

Width : 4.594

Height : 10.104

Entry



B1L102S, U1-ch73

calib_packv5_042523_0143.root, FC#11, port A2

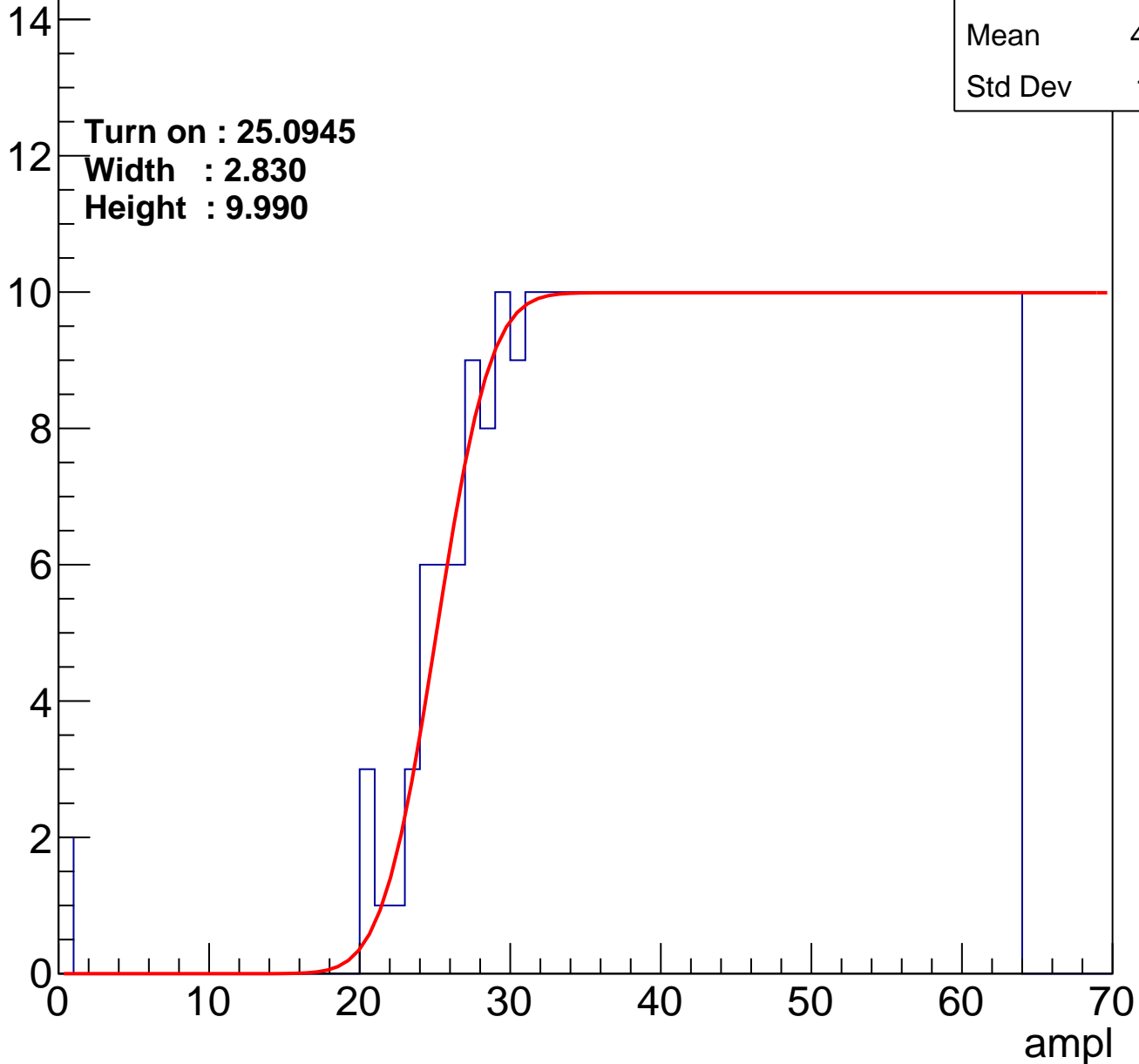
Entries	394
Mean	43.55
Std Dev	11.91

Turn on : 25.0945

Width : 2.830

Height : 9.990

Entry



B1L102S, U1-ch74

calib_packv5_042523_0143.root, FC#11, port A2

Entries	405
Mean	42.87
Std Dev	12.51

Turn on : 23.5467

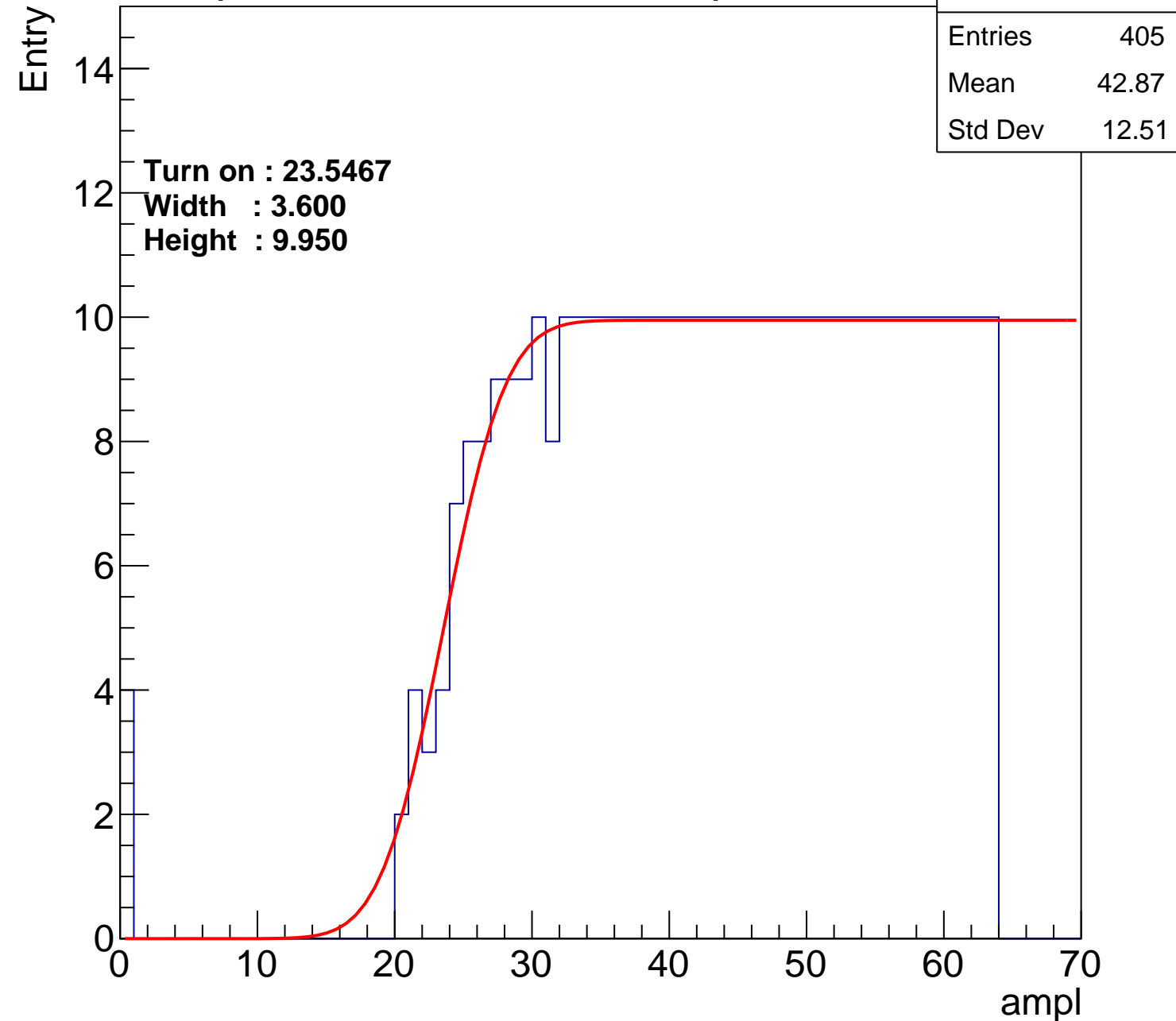
Width : 3.600

Height : 9.950

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch75

calib_packv5_042523_0143.root, FC#11, port A2

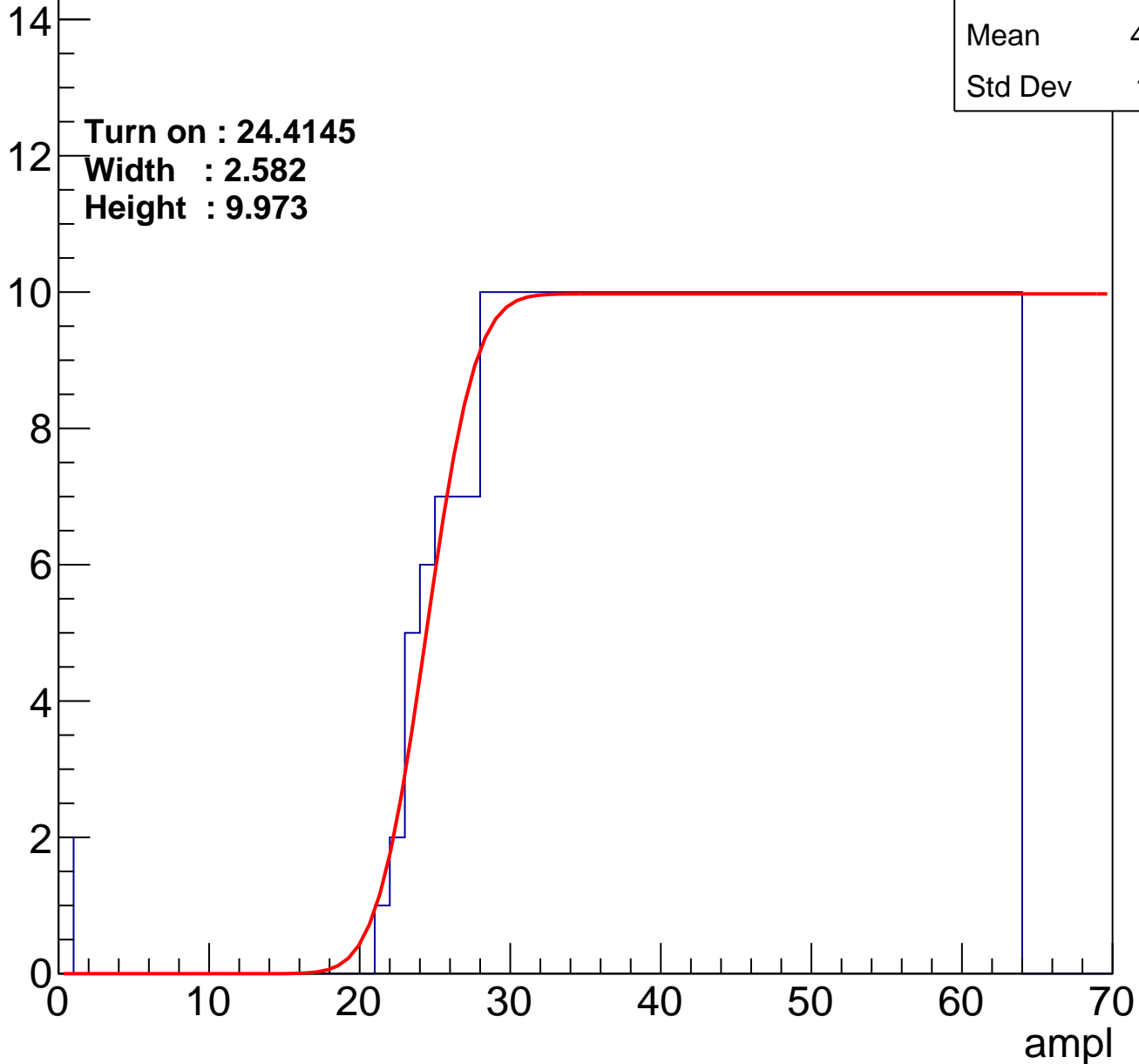
Entries	397
Mean	43.45
Std Dev	11.91

Turn on : 24.4145

Width : 2.582

Height : 9.973

Entry



B1L102S, U1-ch76

calib_packv5_042523_0143.root, FC#11, port A2

Entries	378
Mean	44.32
Std Dev	11.61

Turn on : 26.4014

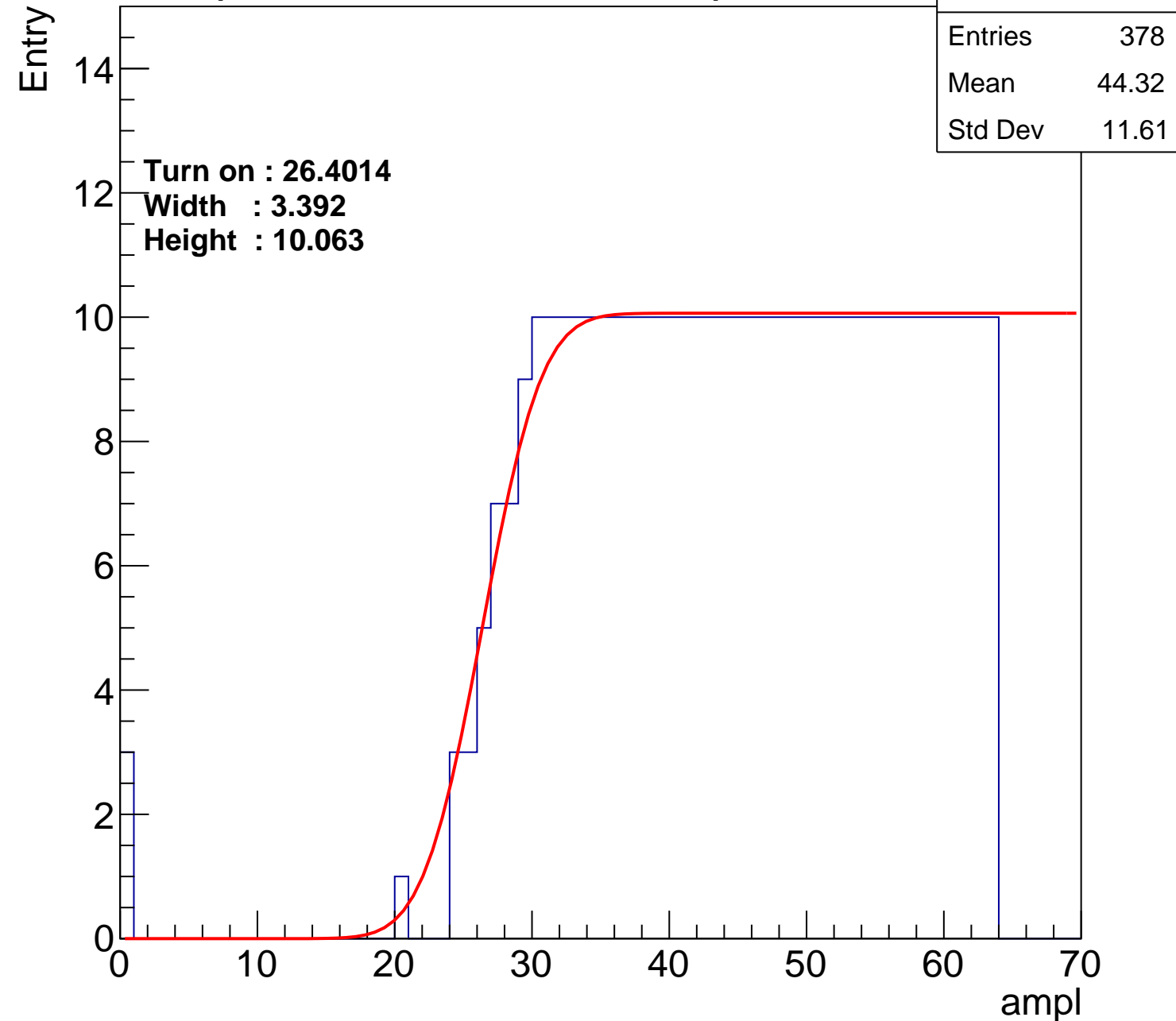
Width : 3.392

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch77

calib_packv5_042523_0143.root, FC#11, port A2

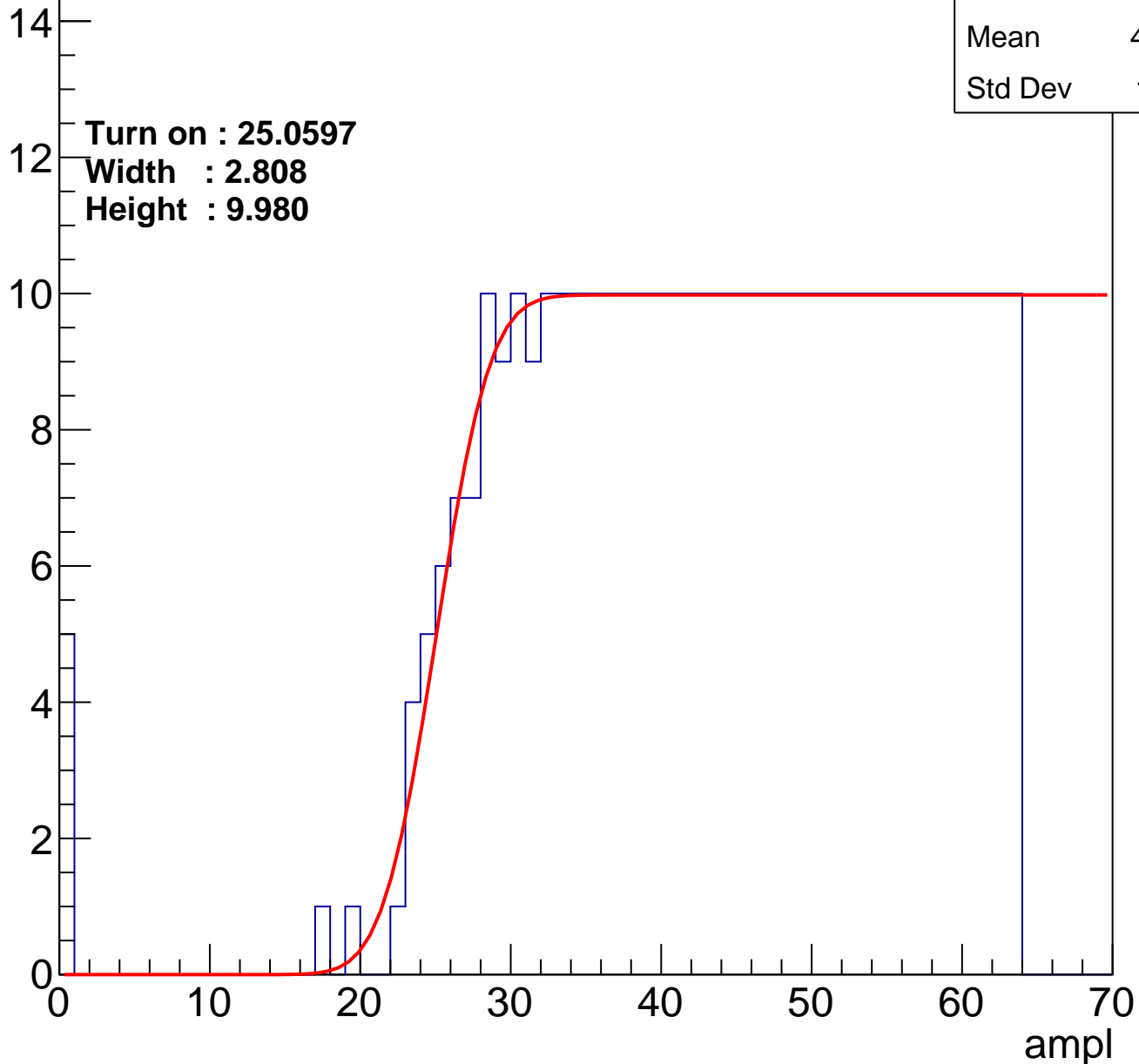
Entries	395
Mean	43.32
Std Dev	12.41

Turn on : 25.0597

Width : 2.808

Height : 9.980

Entry



B1L102S, U1-ch78

calib_packv5_042523_0143.root, FC#11, port A2

Entries	381
Mean	44.12
Std Dev	11.77

Turn on : 26.1301

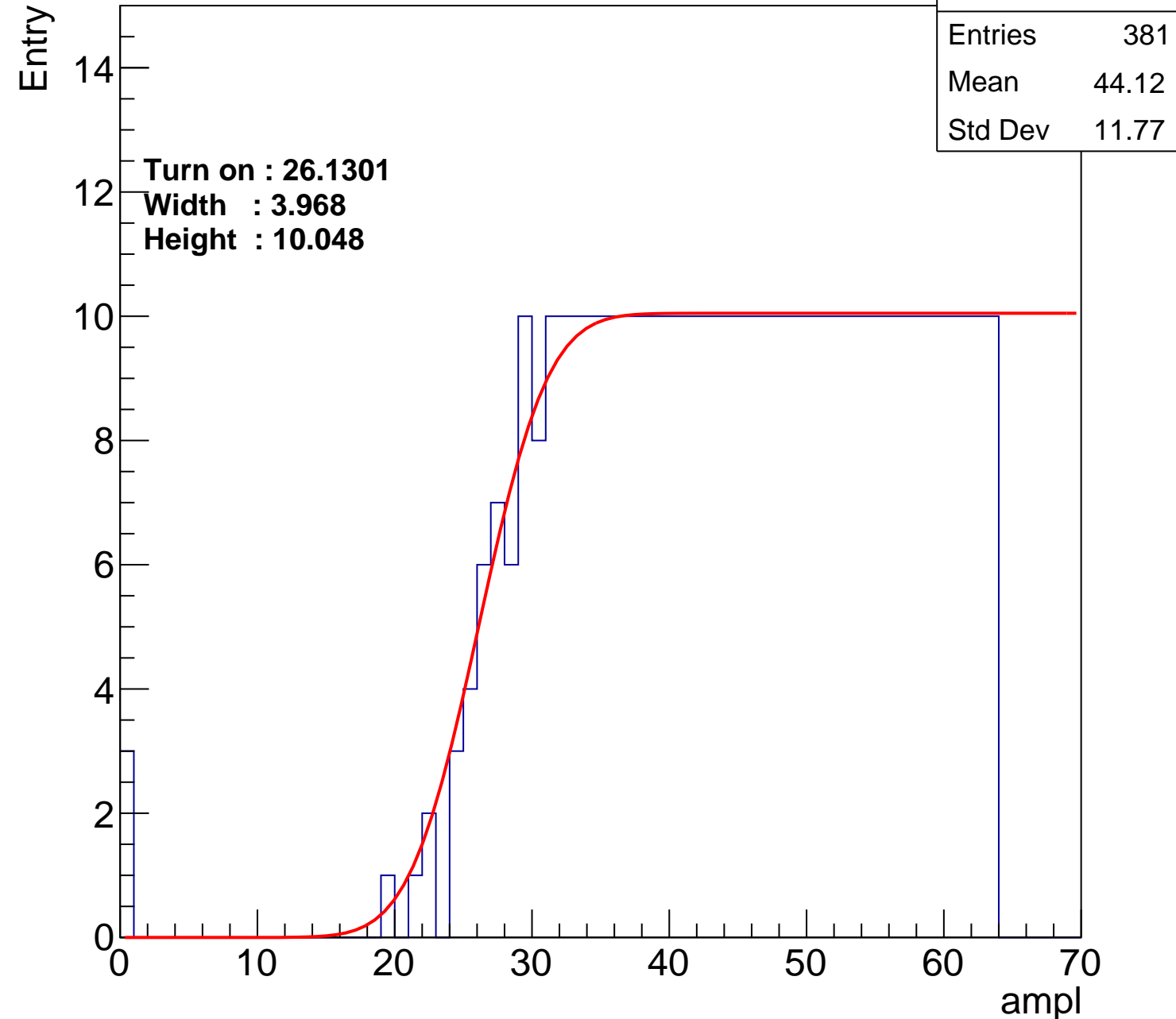
Width : 3.968

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch79

calib_packv5_042523_0143.root, FC#11, port A2

Entries	390
Mean	43.85
Std Dev	11.57

Turn on : 25.4649

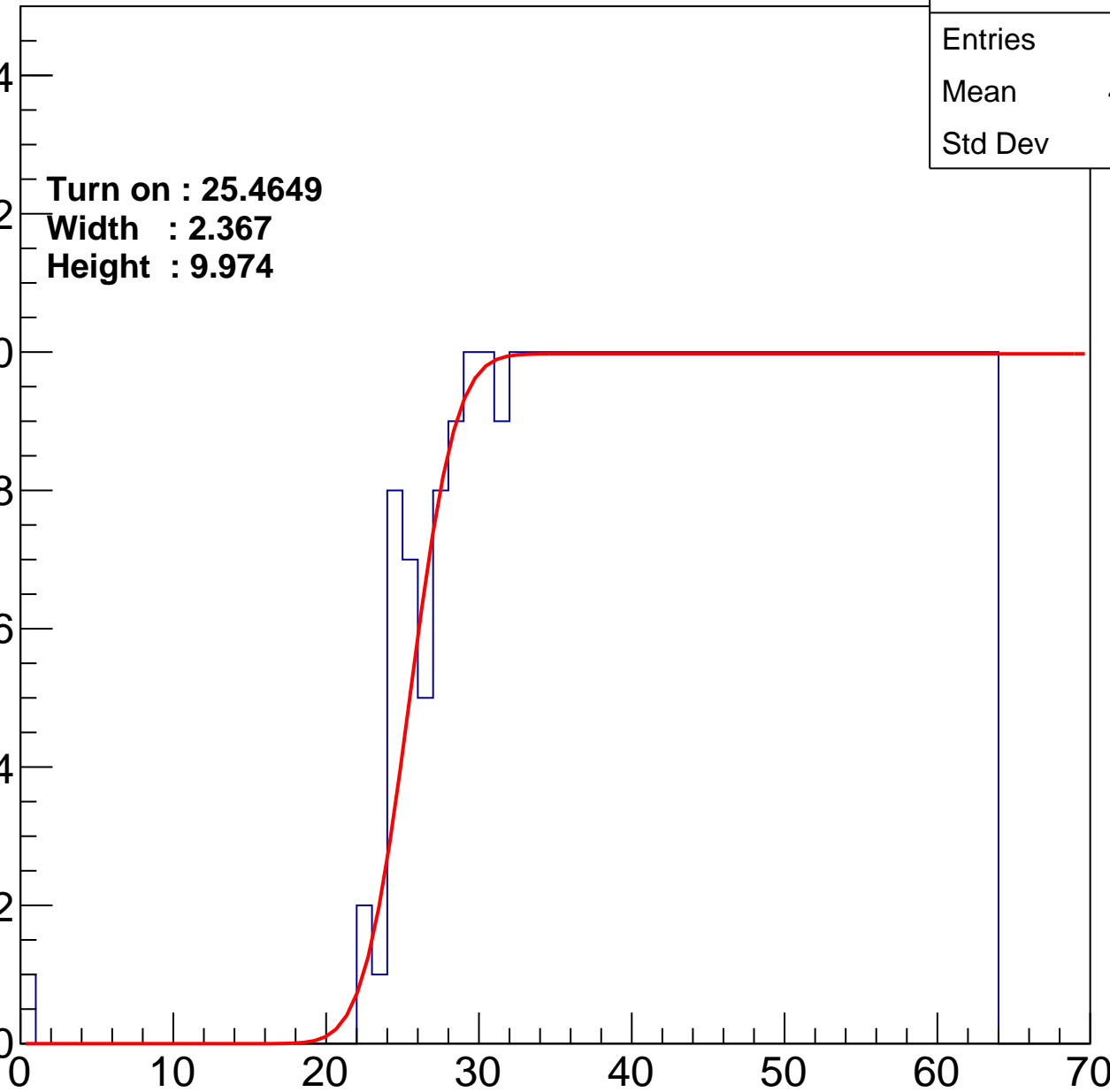
Width : 2.367

Height : 9.974

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch80

calib_packv5_042523_0143.root, FC#11, port A2

Entries	406
Mean	42.88
Std Dev	12.47

Turn on : 24.2888

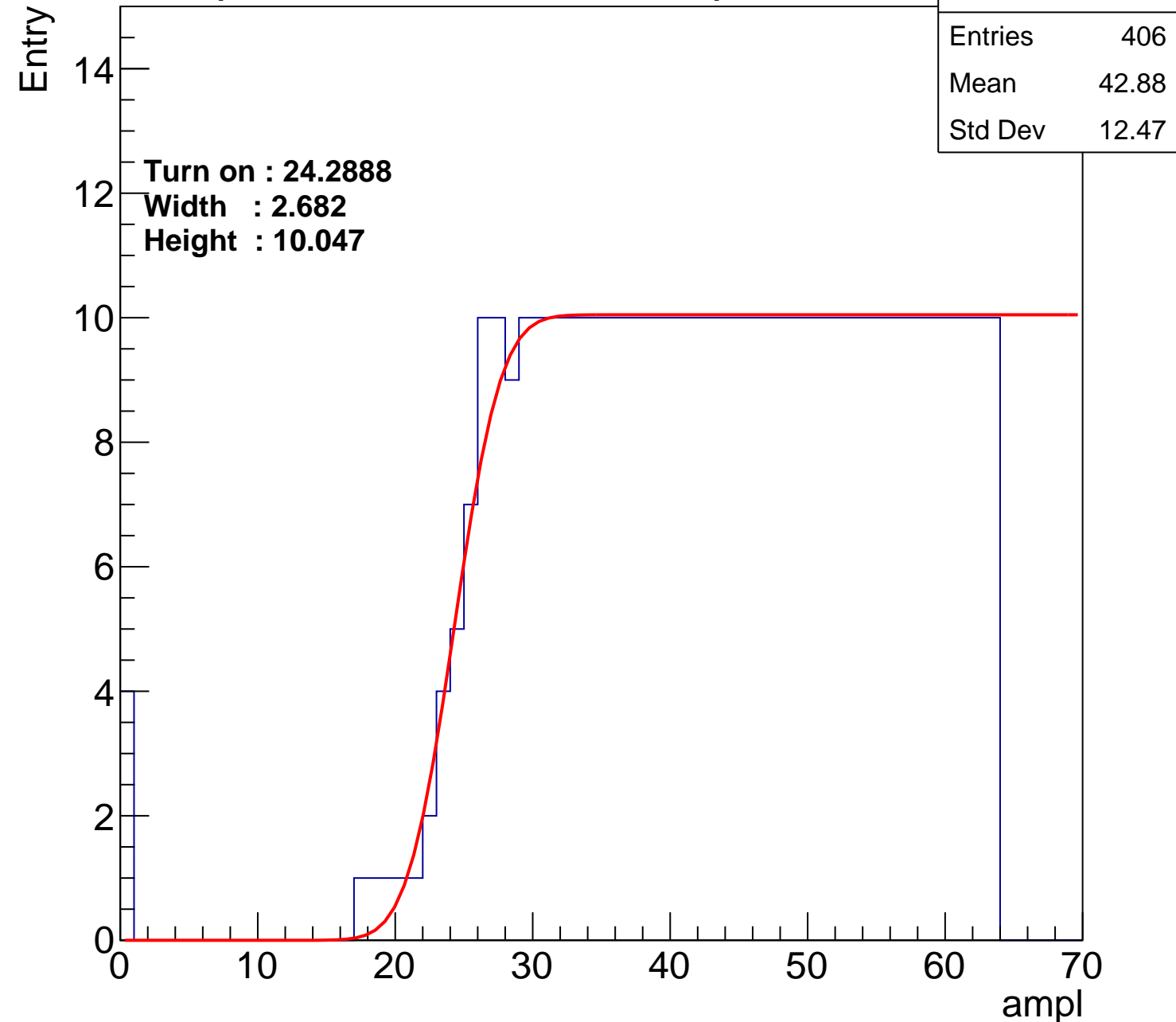
Width : 2.682

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch81

calib_packv5_042523_0143.root, FC#11, port A2

Entries	389
Mean	43.72
Std Dev	11.96

Turn on : 25.3384

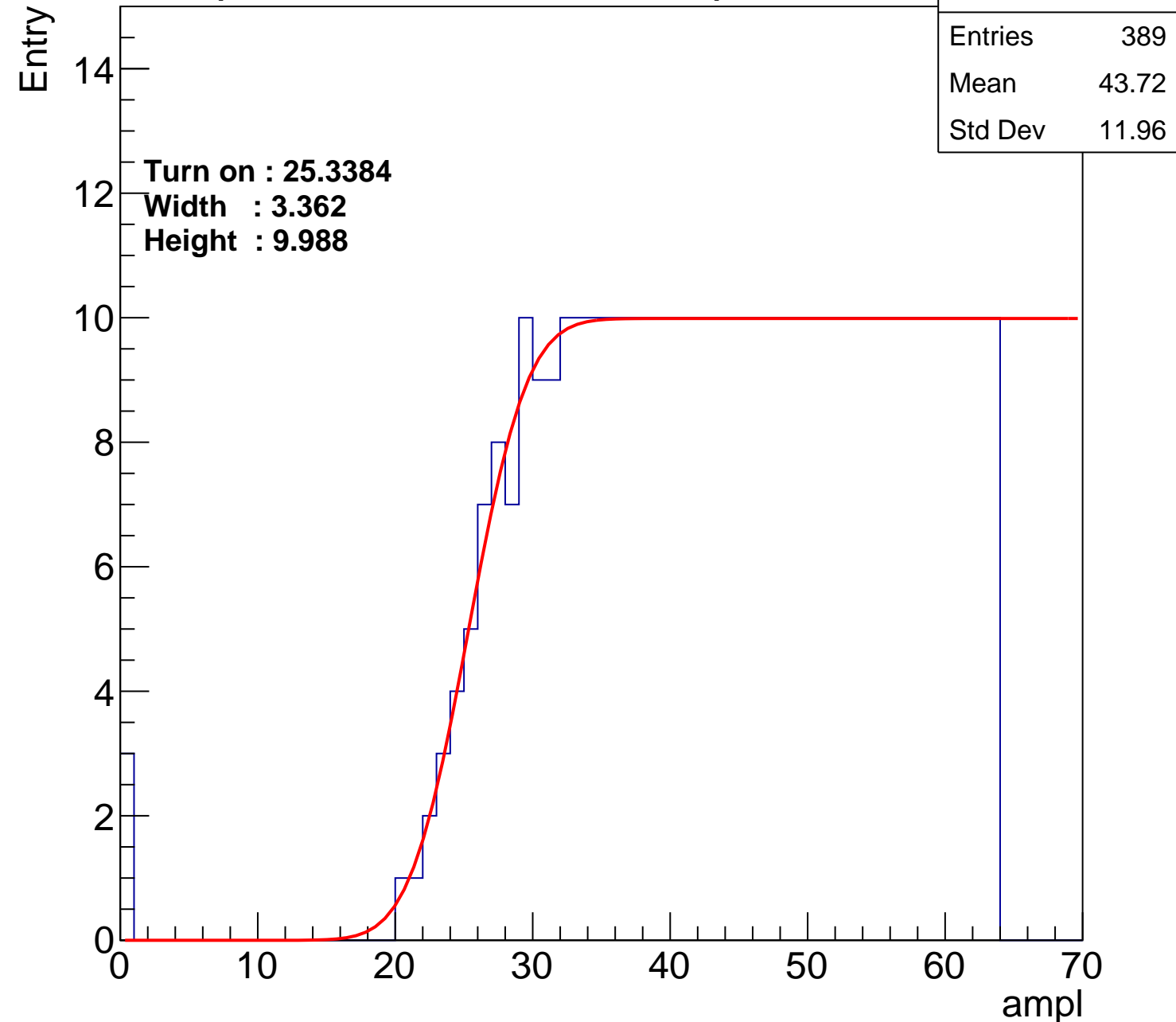
Width : 3.362

Height : 9.988

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch82

calib_packv5_042523_0143.root, FC#11, port A2

Entries	395
Mean	43.4
Std Dev	12.21

Turn on : 24.8906

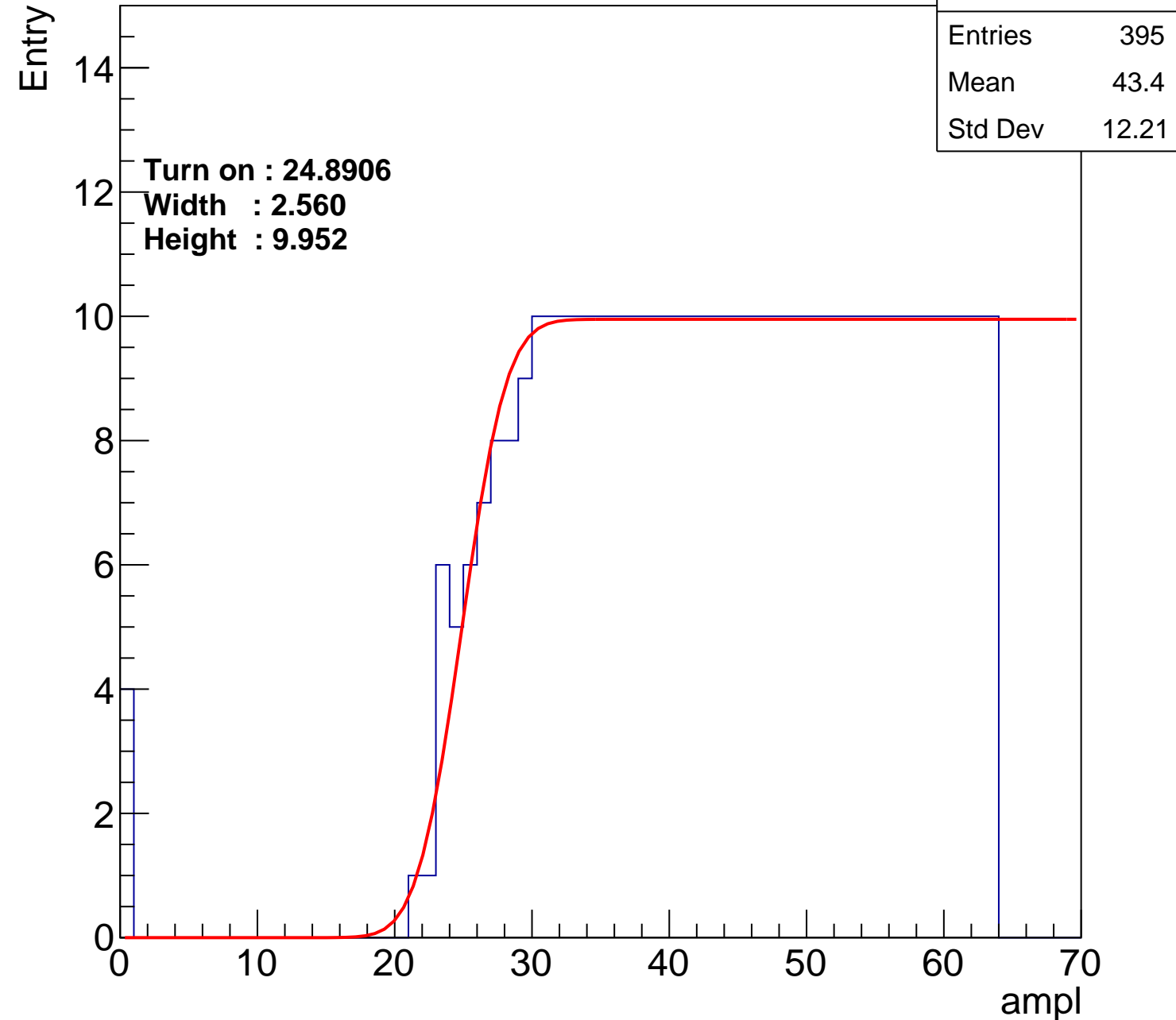
Width : 2.560

Height : 9.952

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch83

calib_packv5_042523_0143.root, FC#11, port A2

Entries	378
Mean	44.35
Std Dev	11.49

Turn on : 27.2249

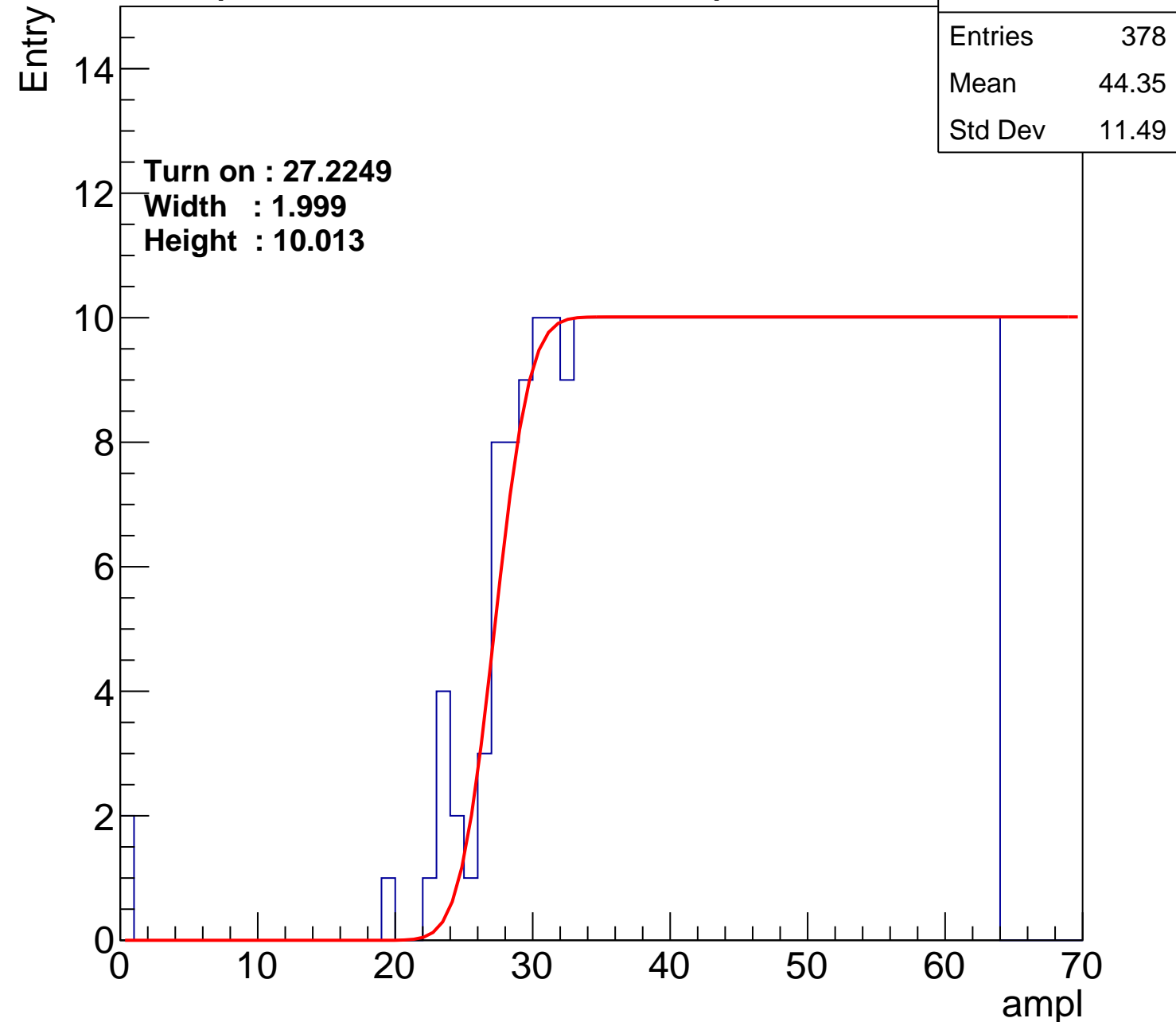
Width : 1.999

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch84

calib_packv5_042523_0143.root, FC#11, port A2

Entries	394
Mean	43.53
Std Dev	11.95

Turn on : 25.3177

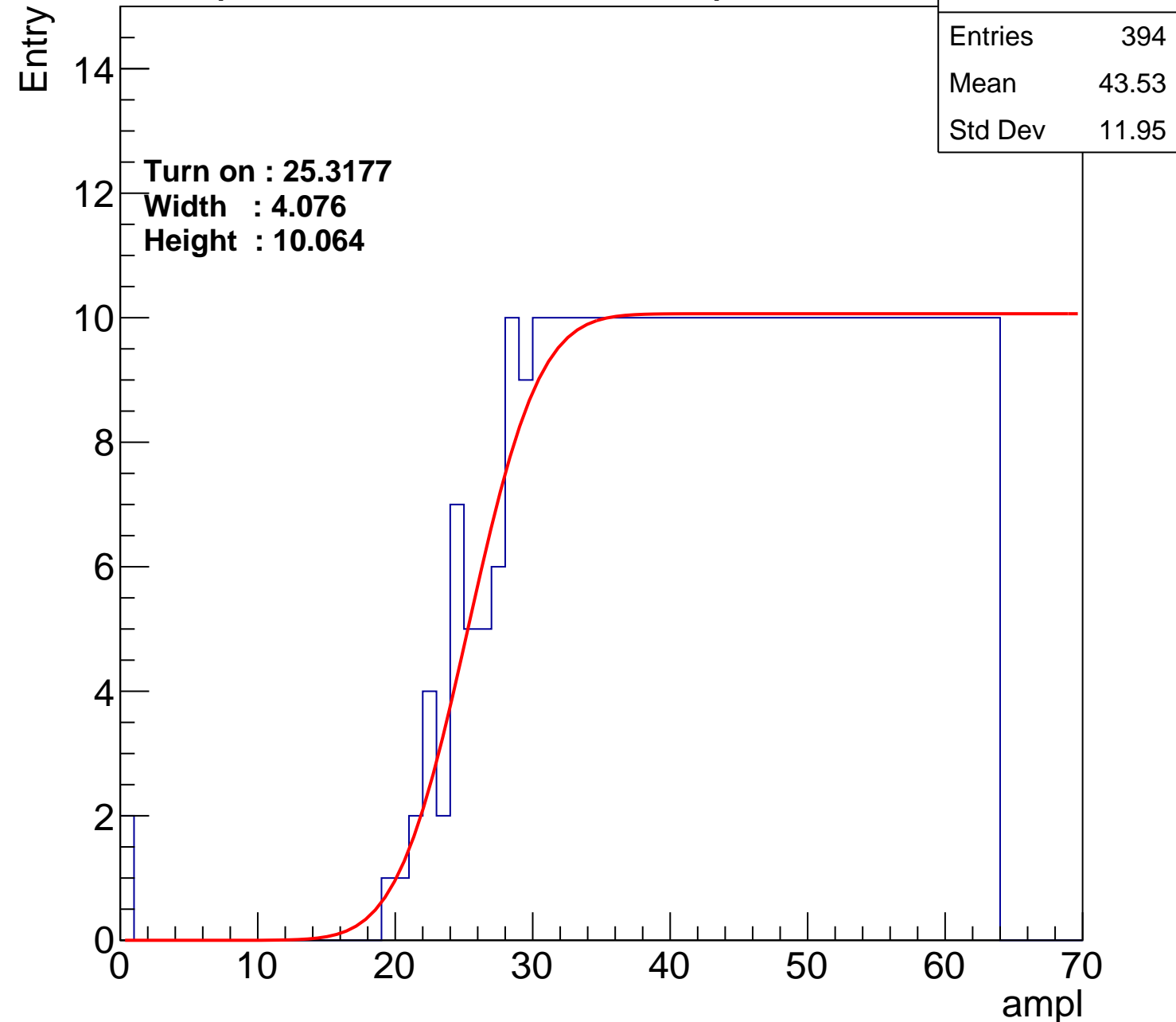
Width : 4.076

Height : 10.064

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch85

calib_packv5_042523_0143.root, FC#11, port A2

Entries	376
Mean	44.12
Std Dev	12.23

Turn on : 26.9977

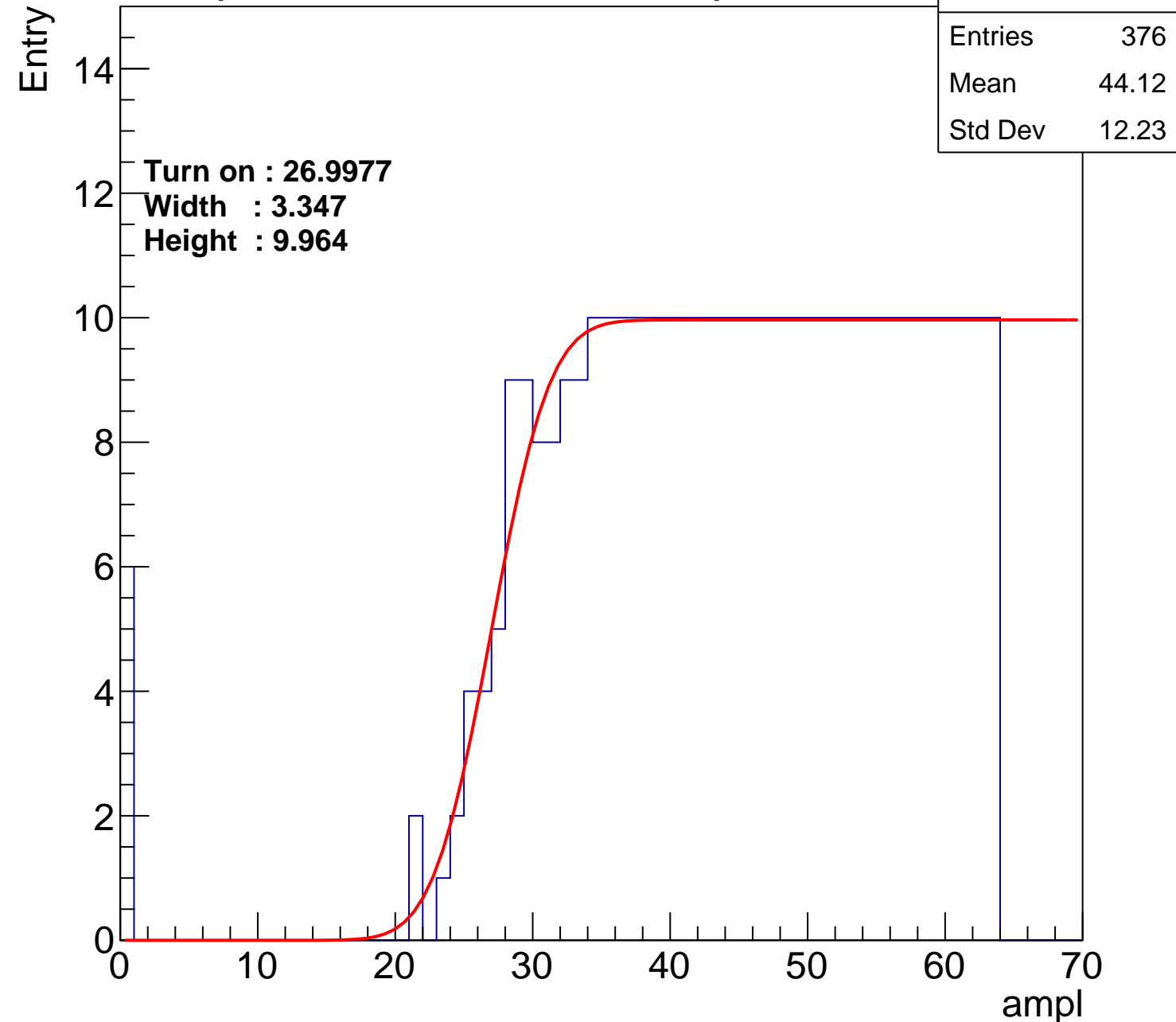
Width : 3.347

Height : 9.964

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch86

calib_packv5_042523_0143.root, FC#11, port A2

Entries	396
Mean	43.43
Std Dev	12

Turn on : 25.5019

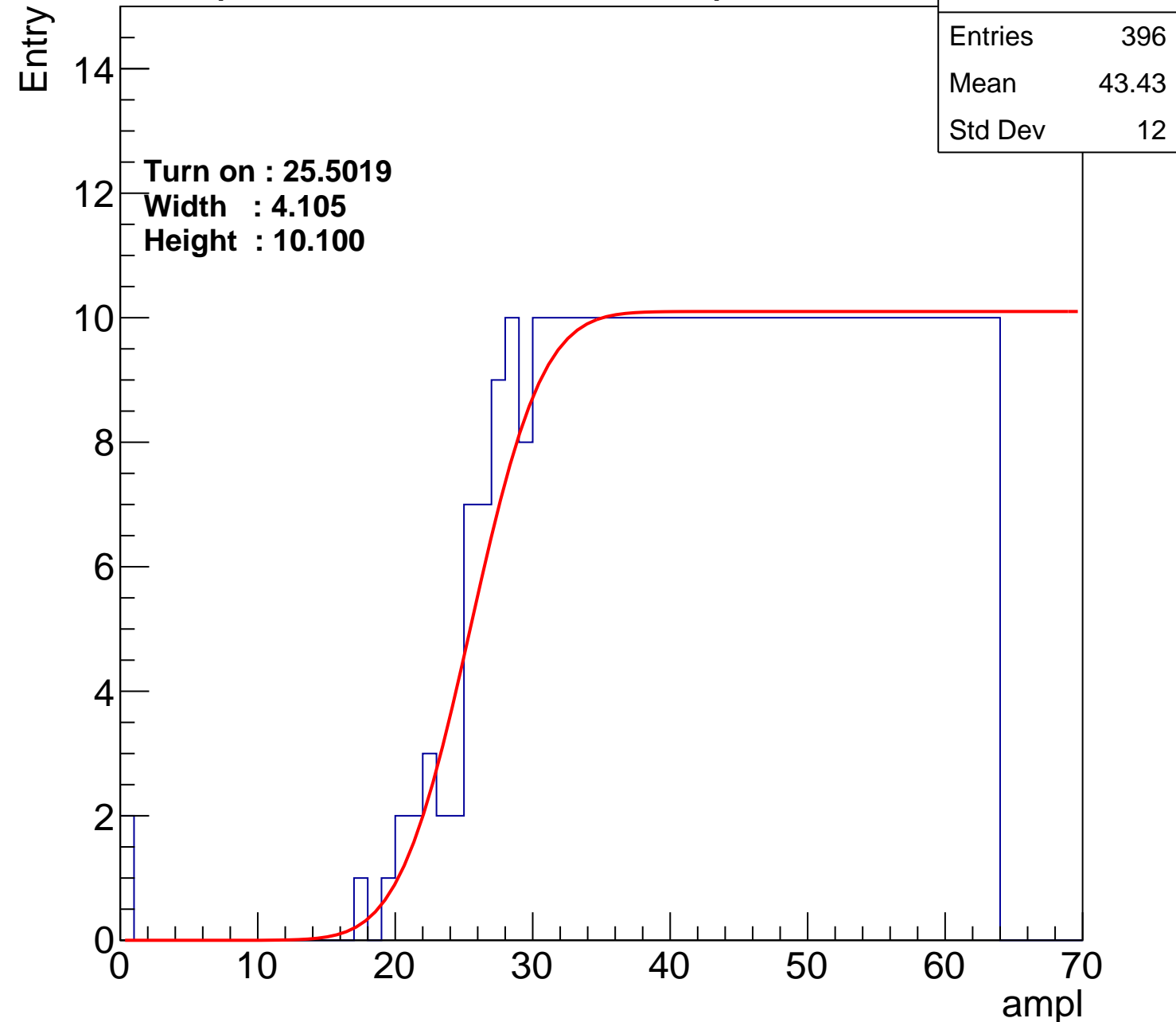
Width : 4.105

Height : 10.100

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch87

calib_packv5_042523_0143.root, FC#11, port A2

Entries	374
Mean	44.45
Std Dev	11.83

Turn on : 27.6046

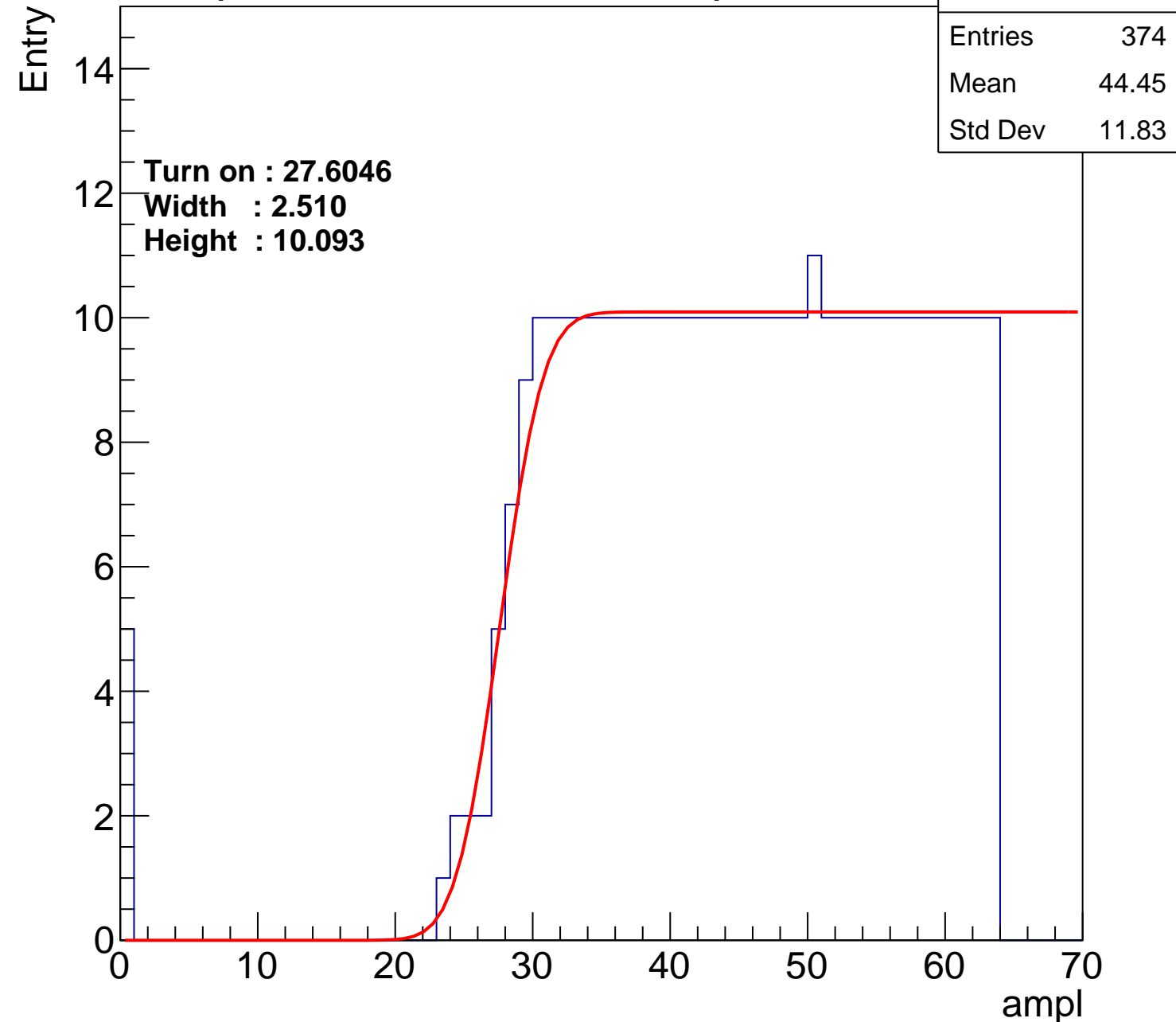
Width : 2.510

Height : 10.093

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch88

calib_packv5_042523_0143.root, FC#11, port A2

Entries	395
Mean	43.55
Std Dev	11.8

Turn on : 24.4997

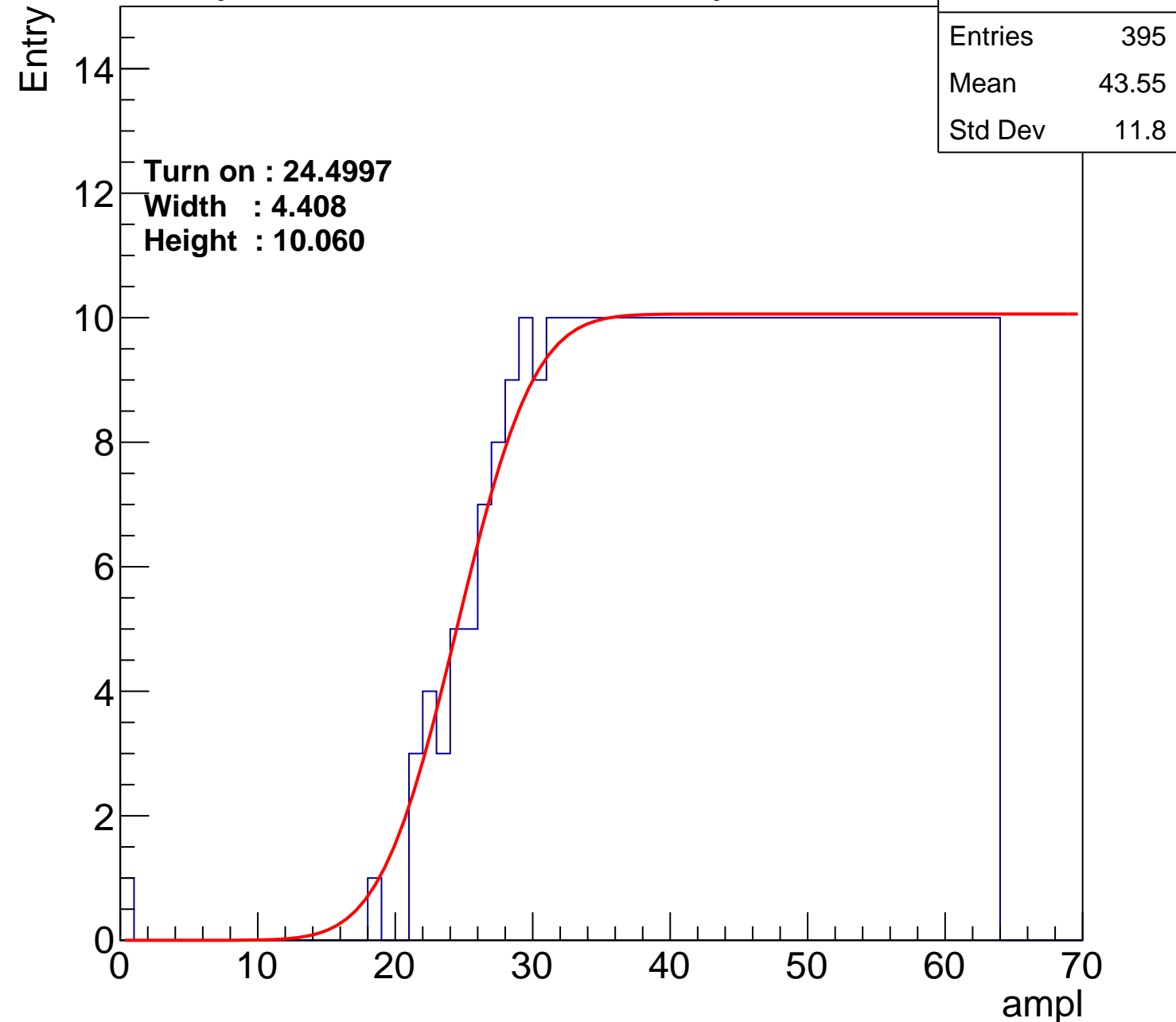
Width : 4.408

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch89

calib_packv5_042523_0143.root, FC#11, port A2

Entries	386
Mean	44.01
Std Dev	11.61

Turn on : 25.8939

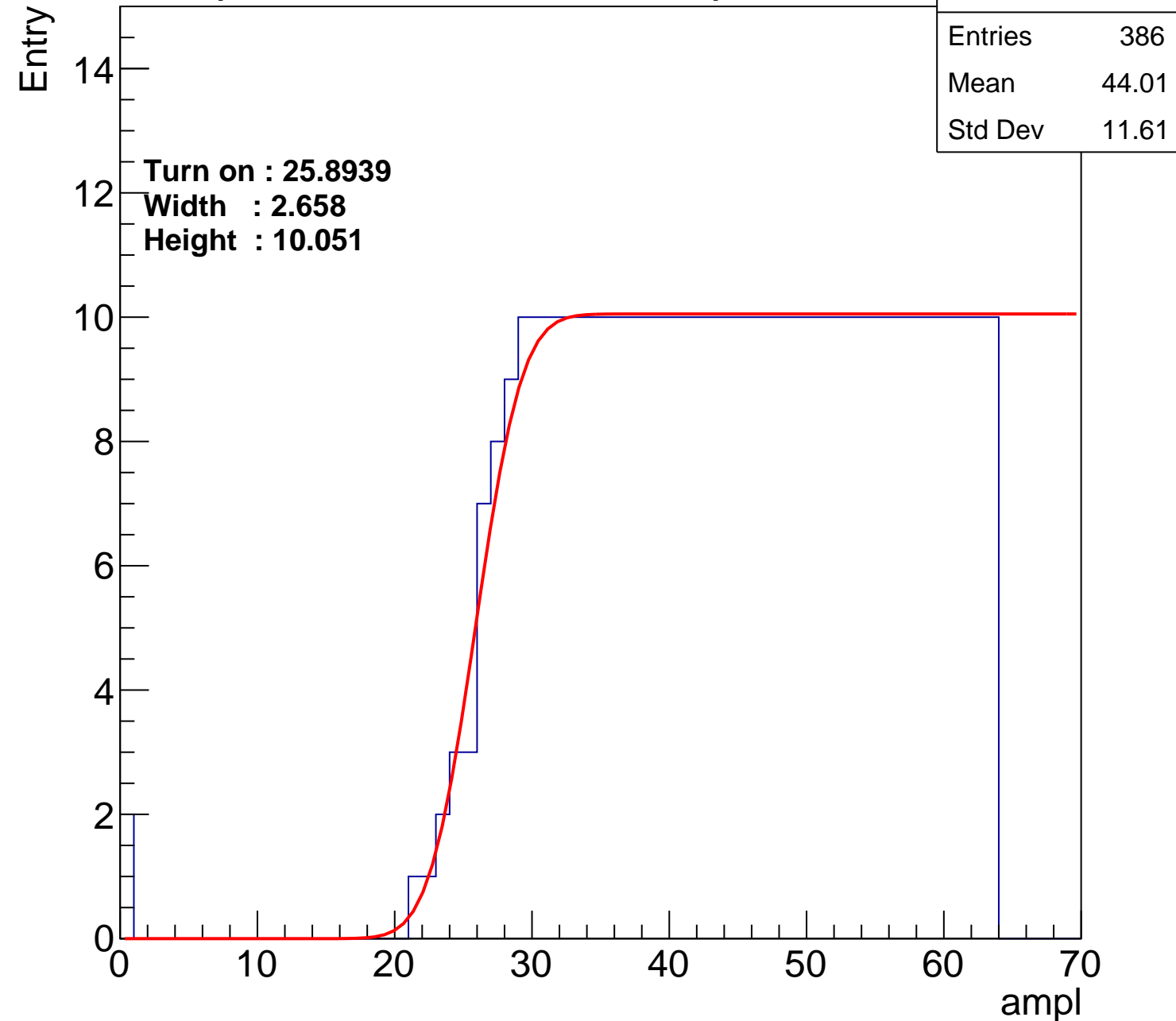
Width : 2.658

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch90

calib_packv5_042523_0143.root, FC#11, port A2

Entries	373
Mean	44.69
Std Dev	11.13

Turn on : 27.3938

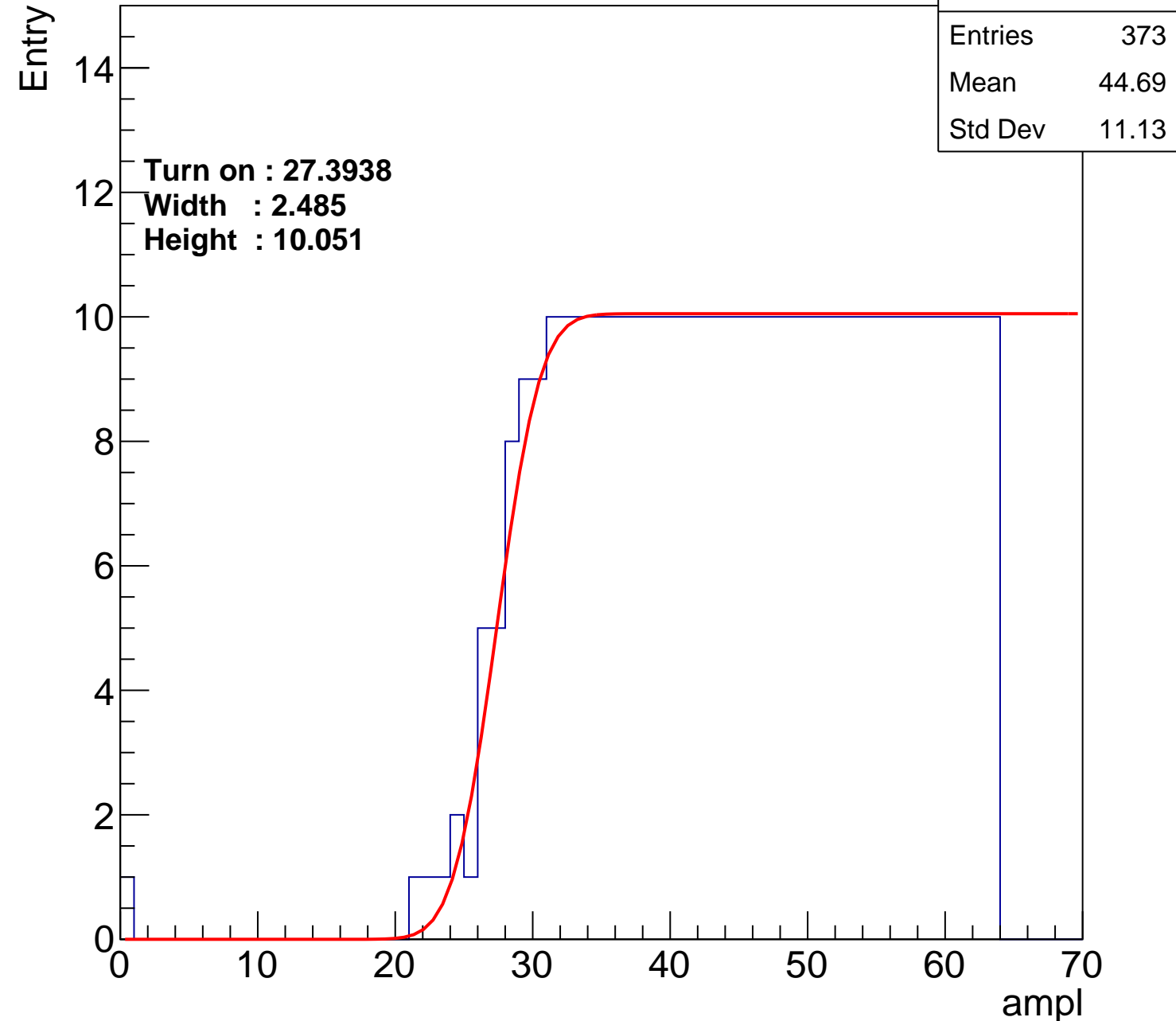
Width : 2.485

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch91

calib_packv5_042523_0143.root, FC#11, port A2

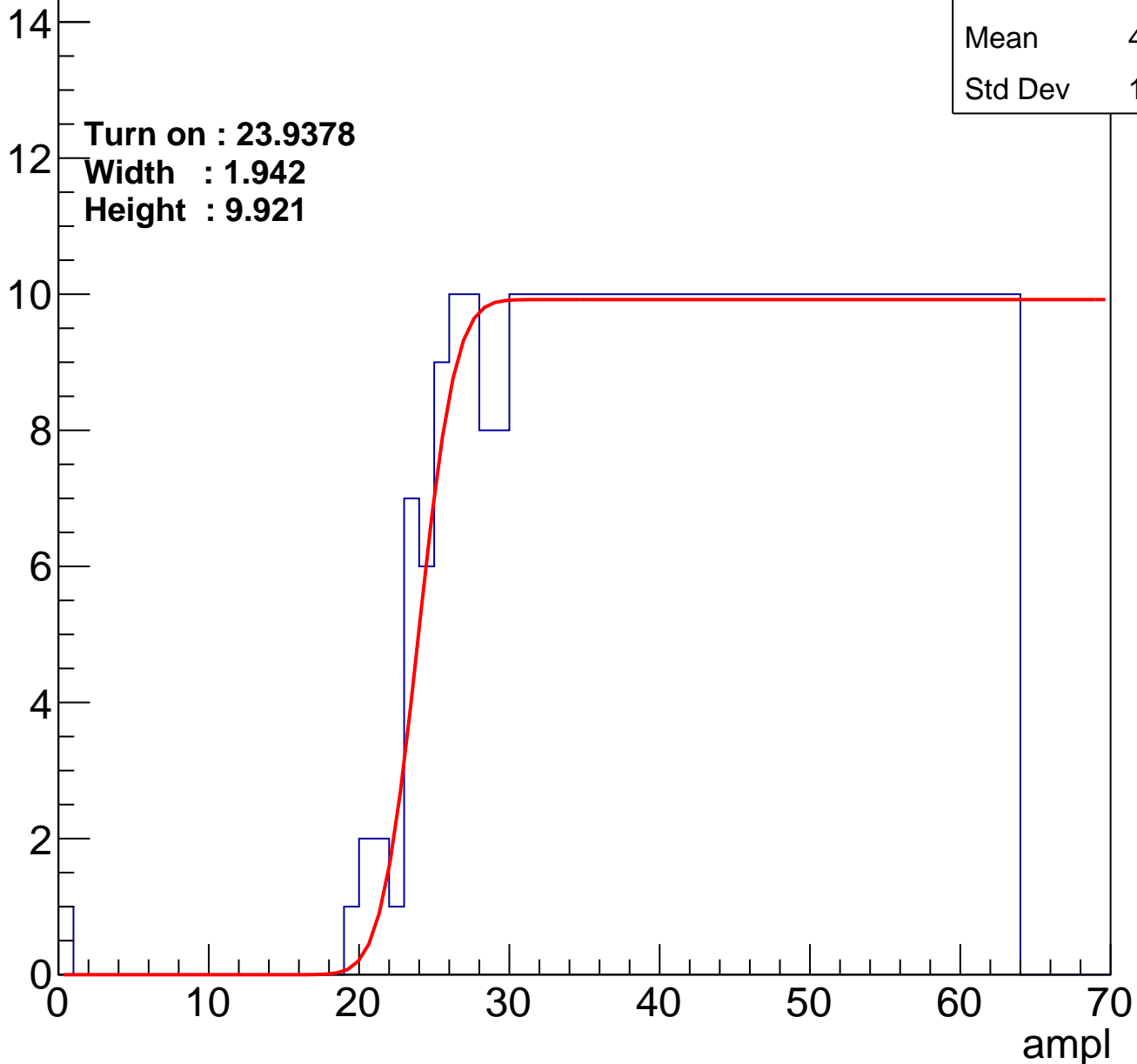
Entries	405
Mean	43.08
Std Dev	12.02

Turn on : 23.9378

Width : 1.942

Height : 9.921

Entry



B1L102S, U1-ch92

calib_packv5_042523_0143.root, FC#11, port A2

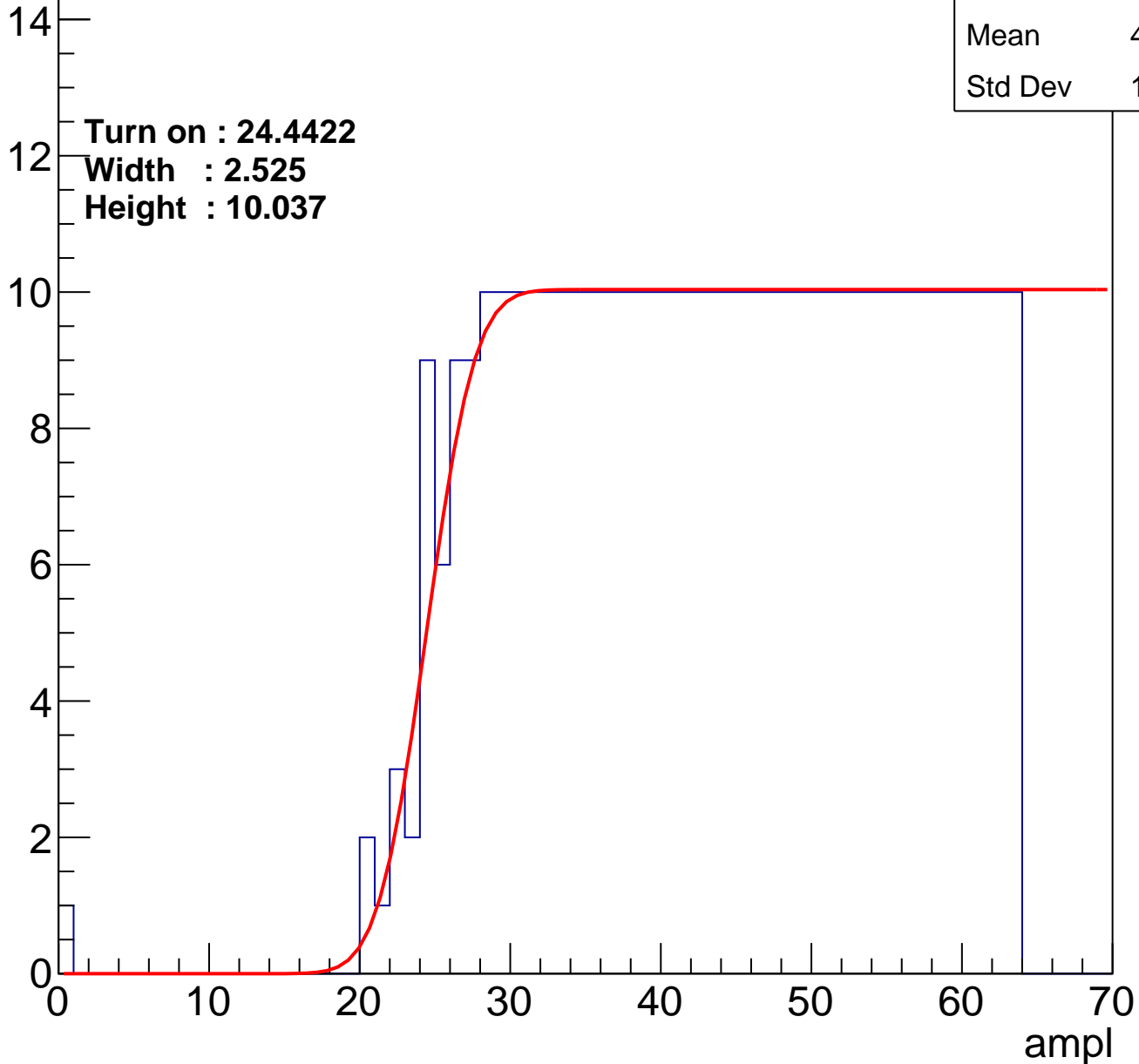
Entries	402
Mean	43.27
Std Dev	11.87

Turn on : 24.4422

Width : 2.525

Height : 10.037

Entry



B1L102S, U1-ch93

calib_packv5_042523_0143.root, FC#11, port A2

Entries	385
Mean	43.95
Std Dev	11.82

Turn on : 26.4744

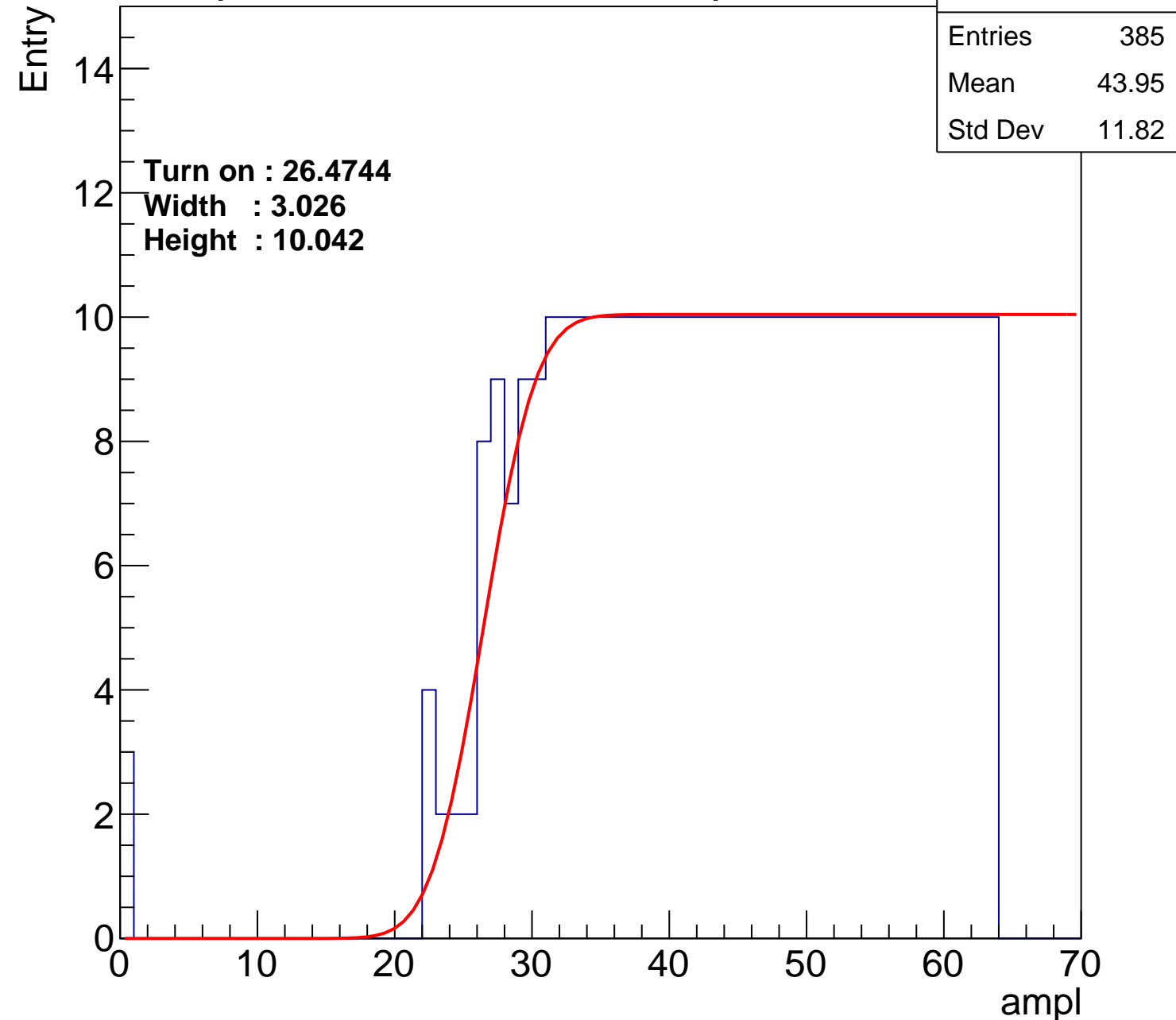
Width : 3.026

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch94

calib_packv5_042523_0143.root, FC#11, port A2

Entries	399
Mean	43.26
Std Dev	12.16

Turn on : 23.9352

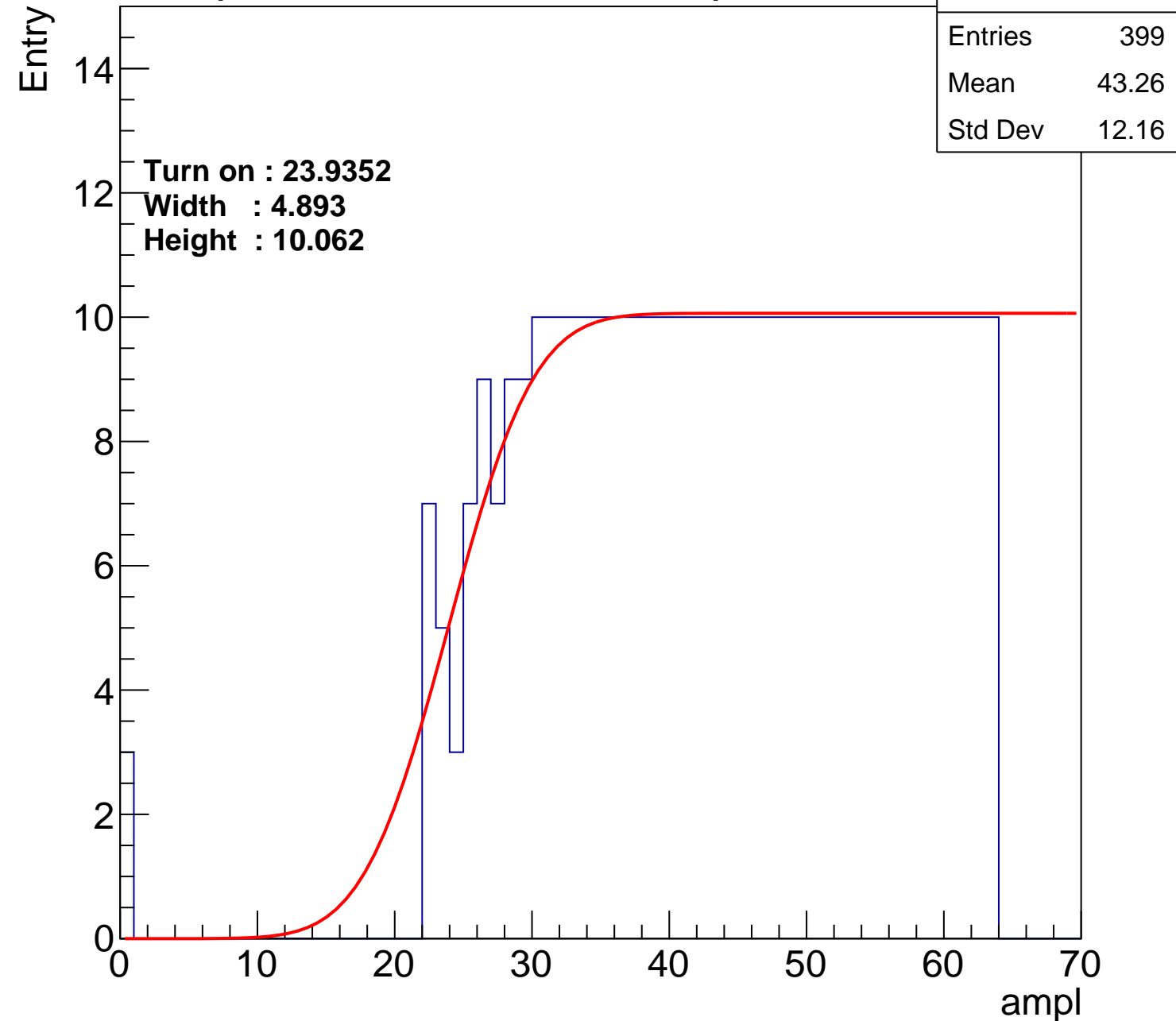
Width : 4.893

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch95

calib_packv5_042523_0143.root, FC#11, port A2

Entries	377
Mean	44.46
Std Dev	11.35

Turn on : 26.7280

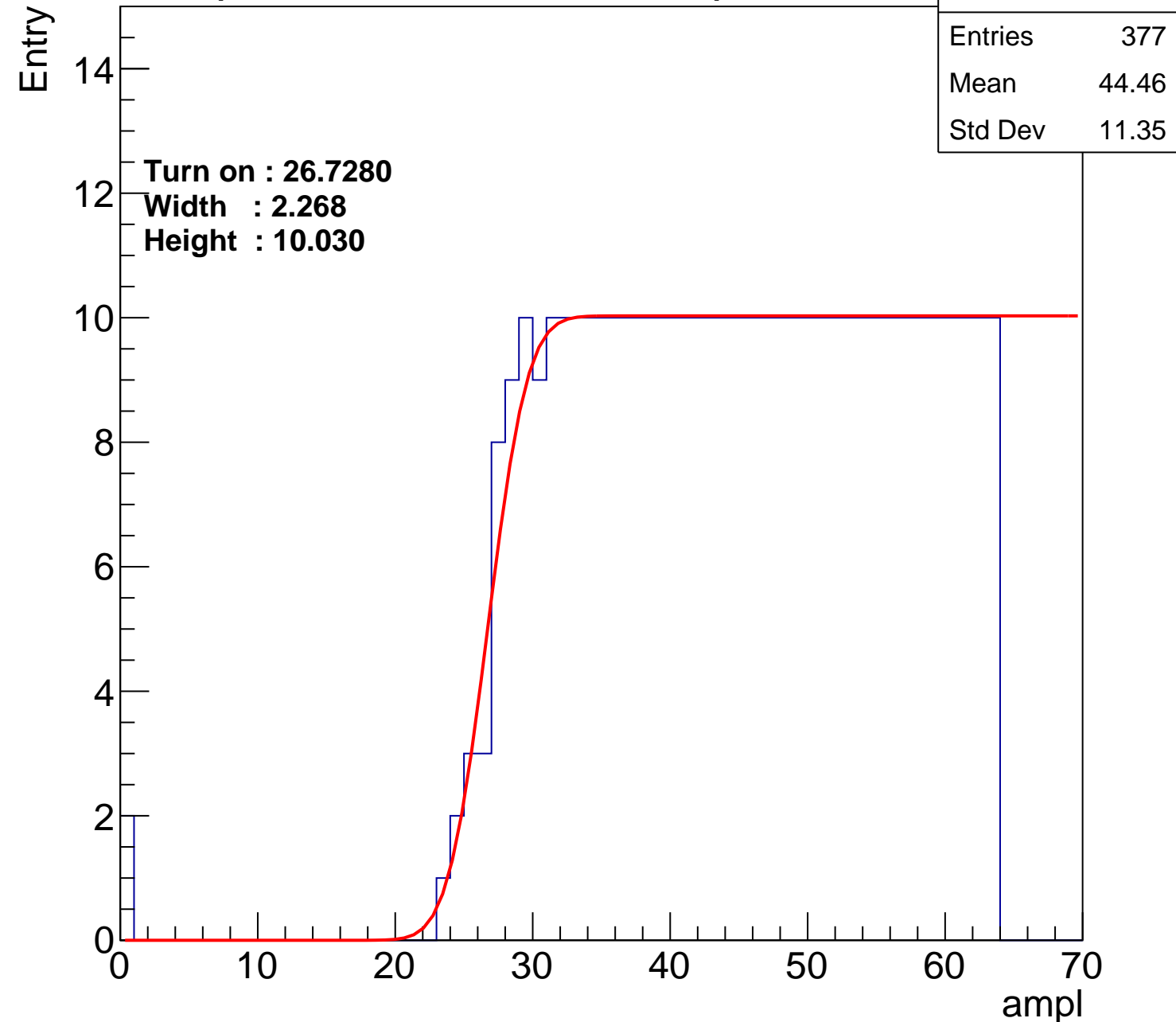
Width : 2.268

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch96

calib_packv5_042523_0143.root, FC#11, port A2

Entries	385
Mean	44.1
Std Dev	11.43

Turn on : 25.1623

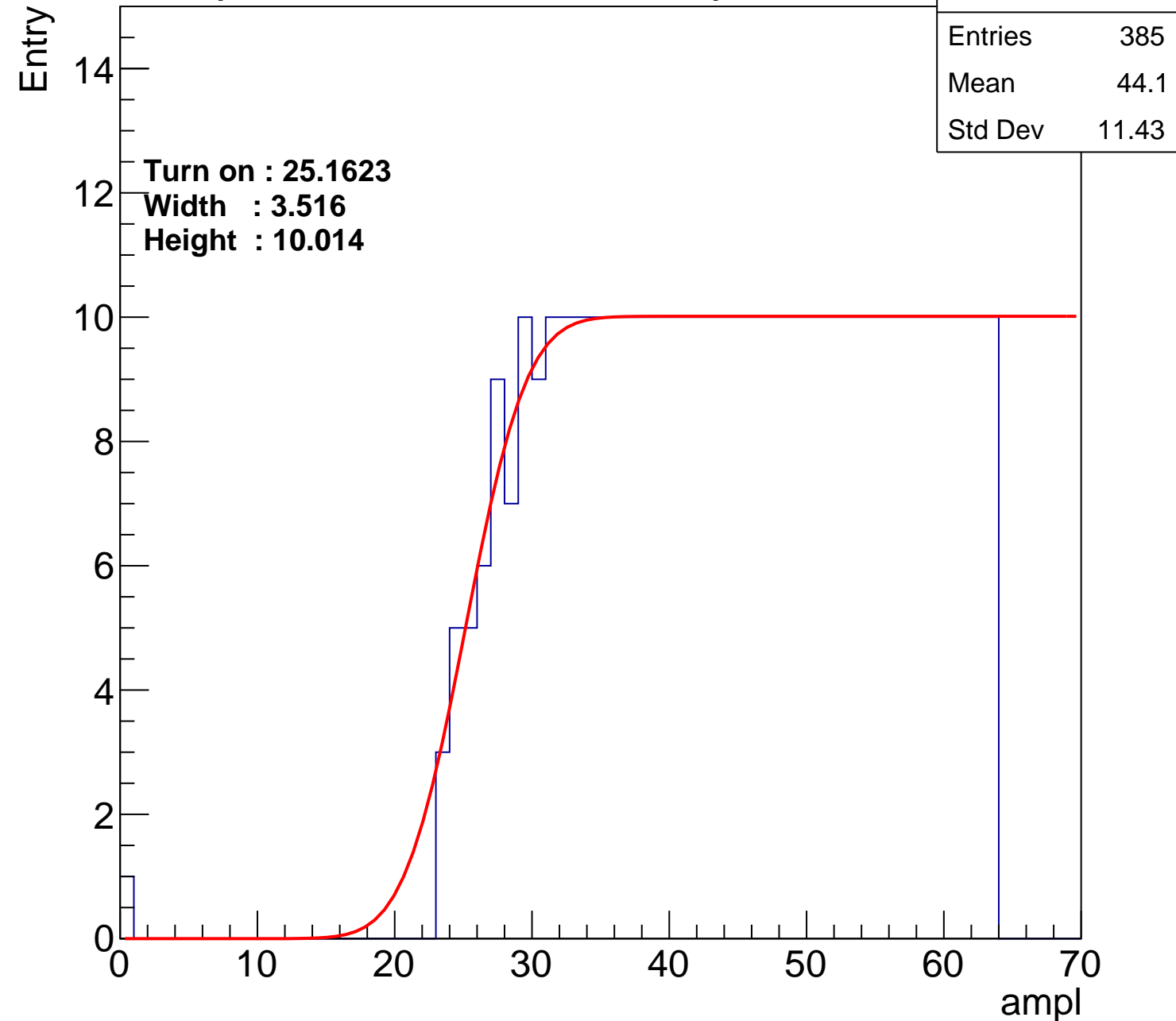
Width : 3.516

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch97

calib_packv5_042523_0143.root, FC#11, port A2

Entries	369
Mean	44.66
Std Dev	11.62

Turn on : 28.1777

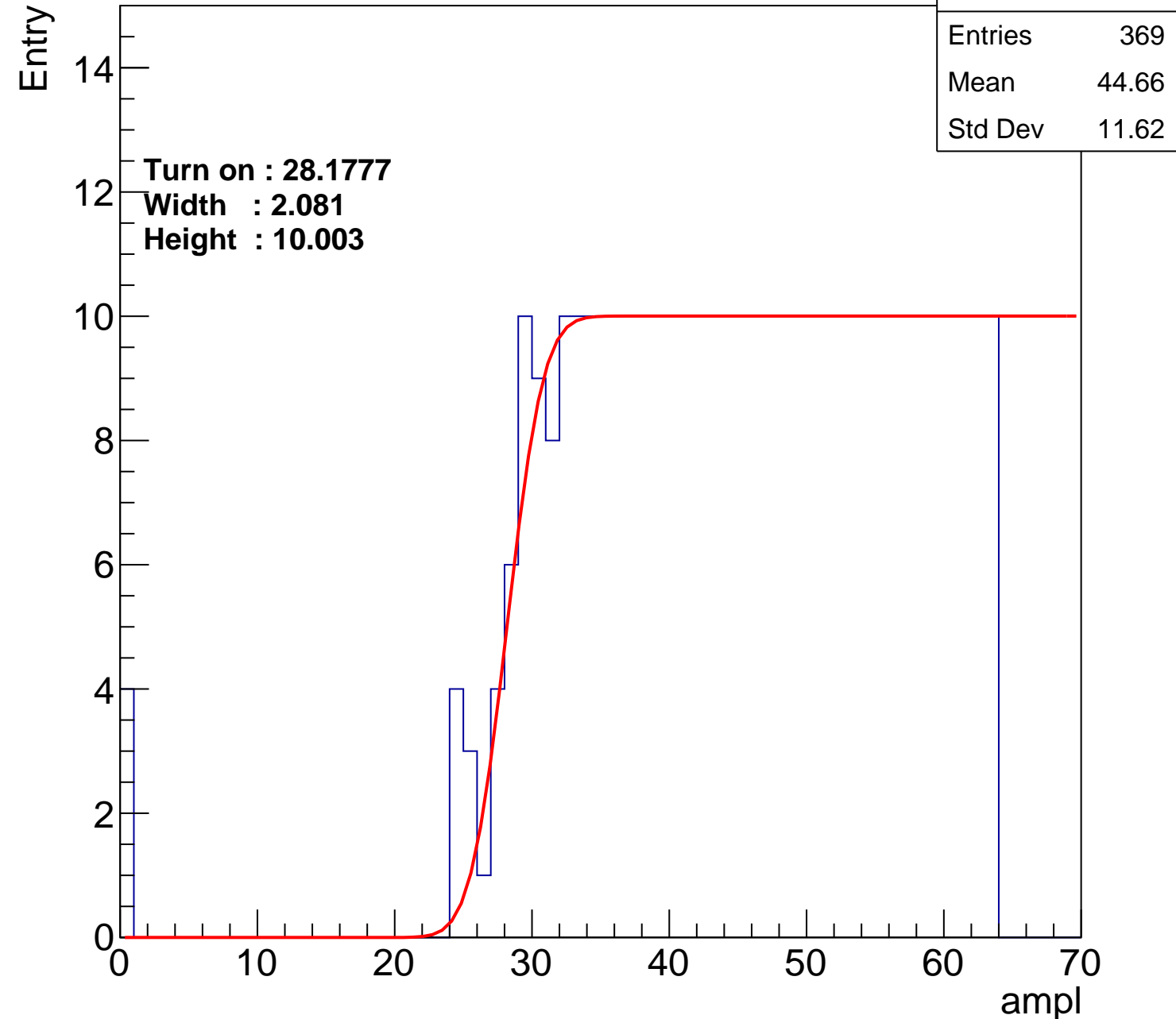
Width : 2.081

Height : 10.003

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch98

calib_packv5_042523_0143.root, FC#11, port A2

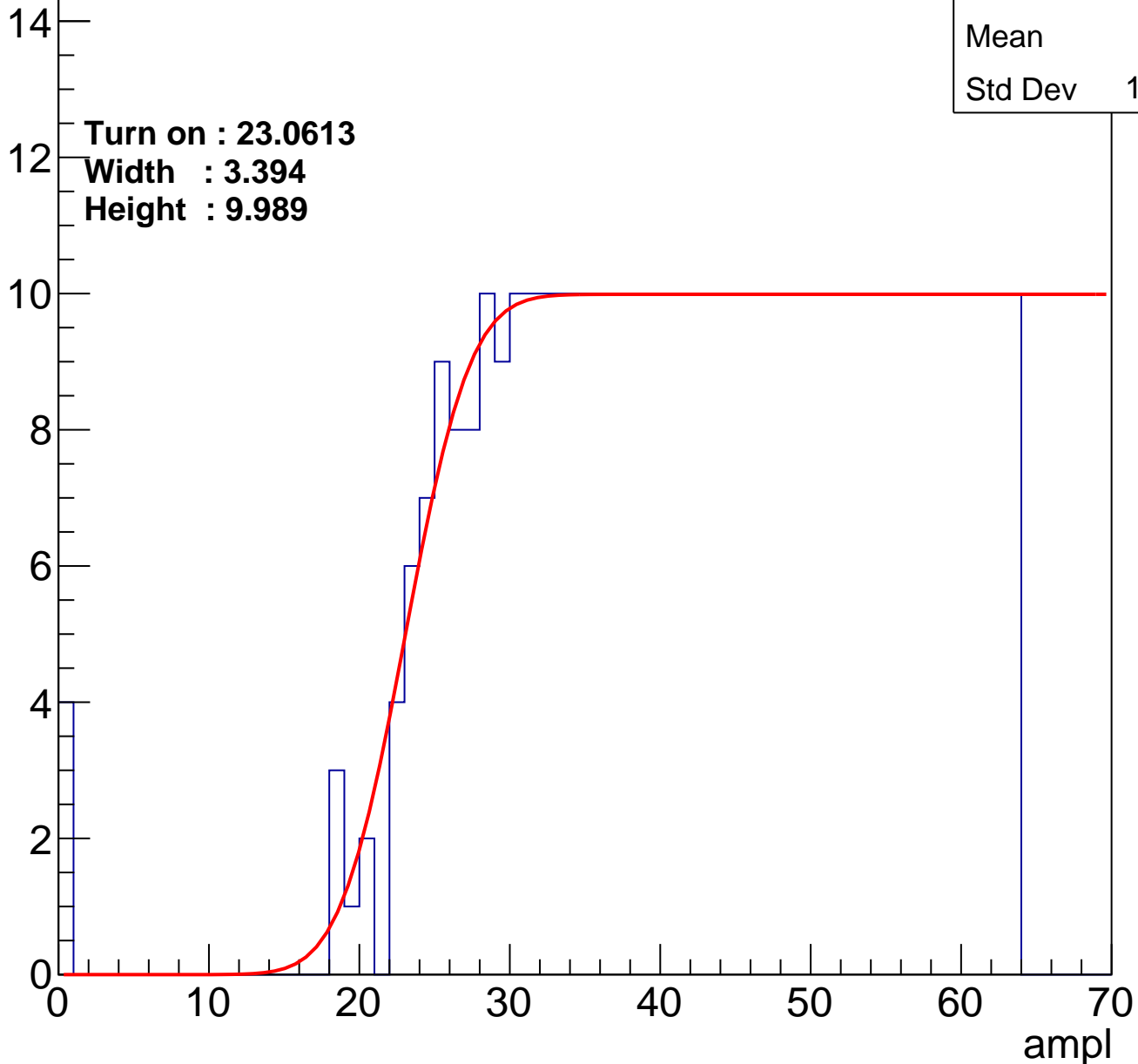
Entries	411
Mean	42.6
Std Dev	12.64

Turn on : 23.0613

Width : 3.394

Height : 9.989

Entry



B1L102S, U1-ch99

calib_packv5_042523_0143.root, FC#11, port A2

Entries	384
Mean	44.11
Std Dev	11.55

Turn on : 25.8026

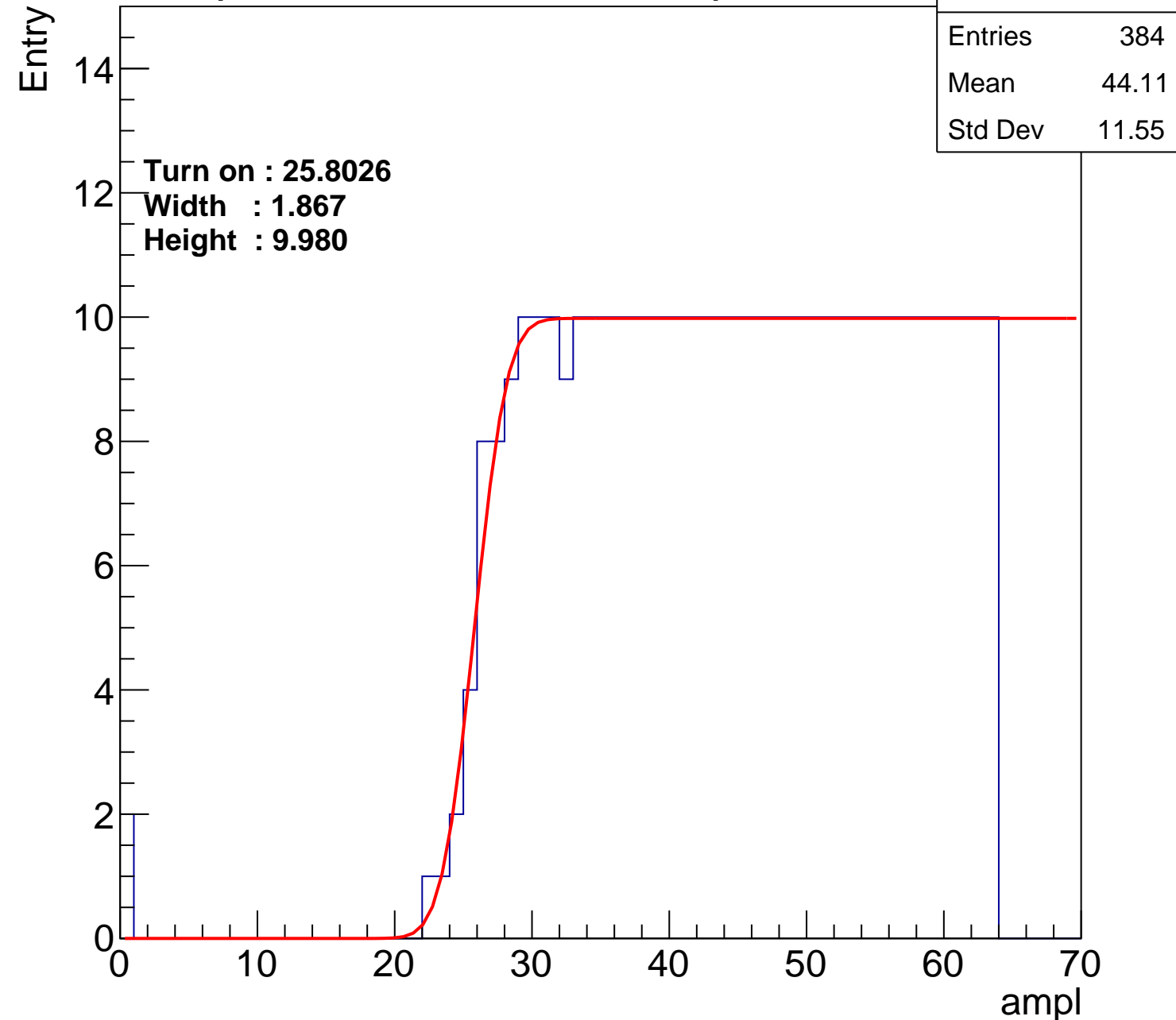
Width : 1.867

Height : 9.980

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch100

calib_packv5_042523_0143.root, FC#11, port A2

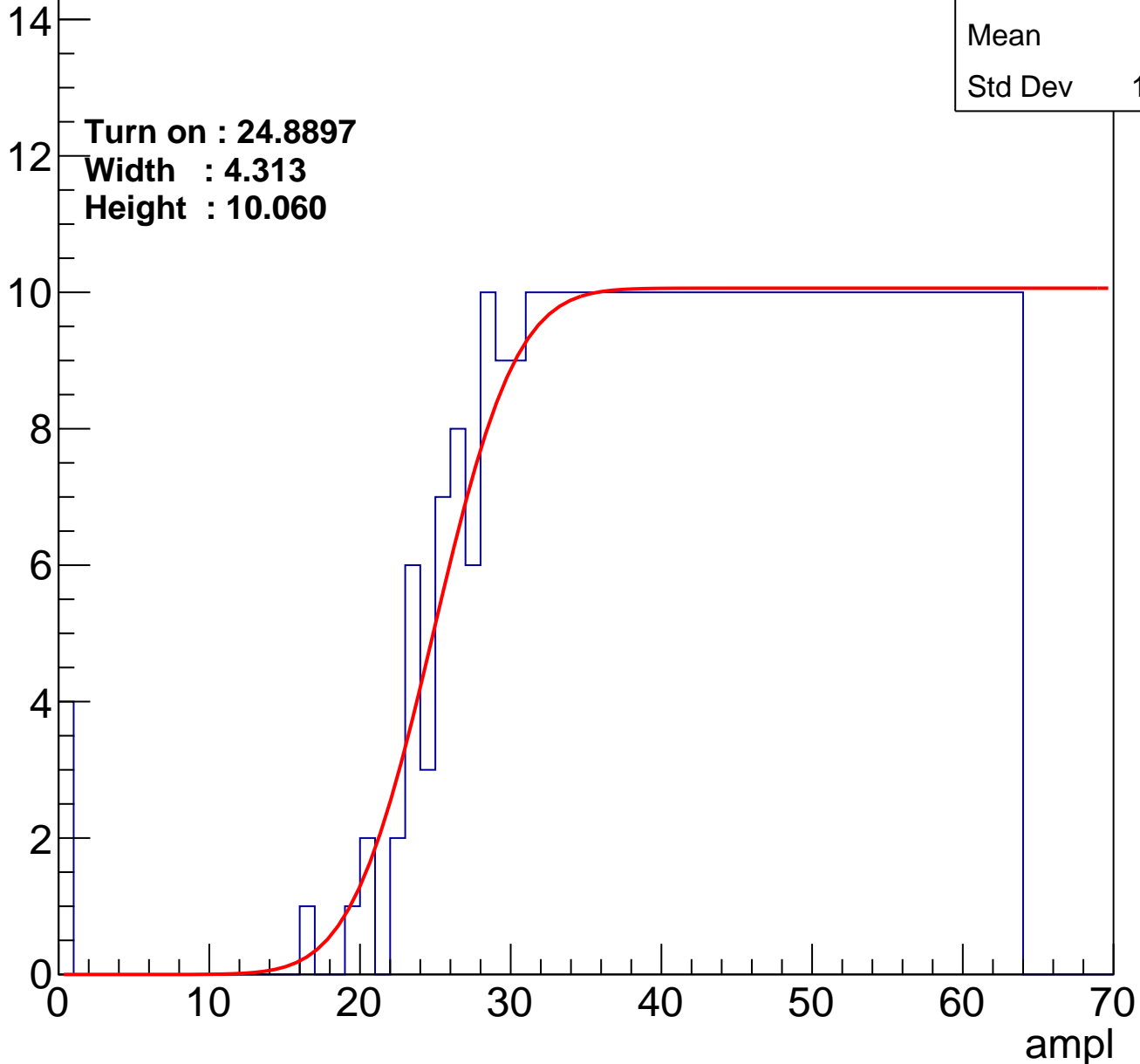
Entries	398
Mean	43.2
Std Dev	12.38

Turn on : 24.8897

Width : 4.313

Height : 10.060

Entry



B1L102S, U1-ch101

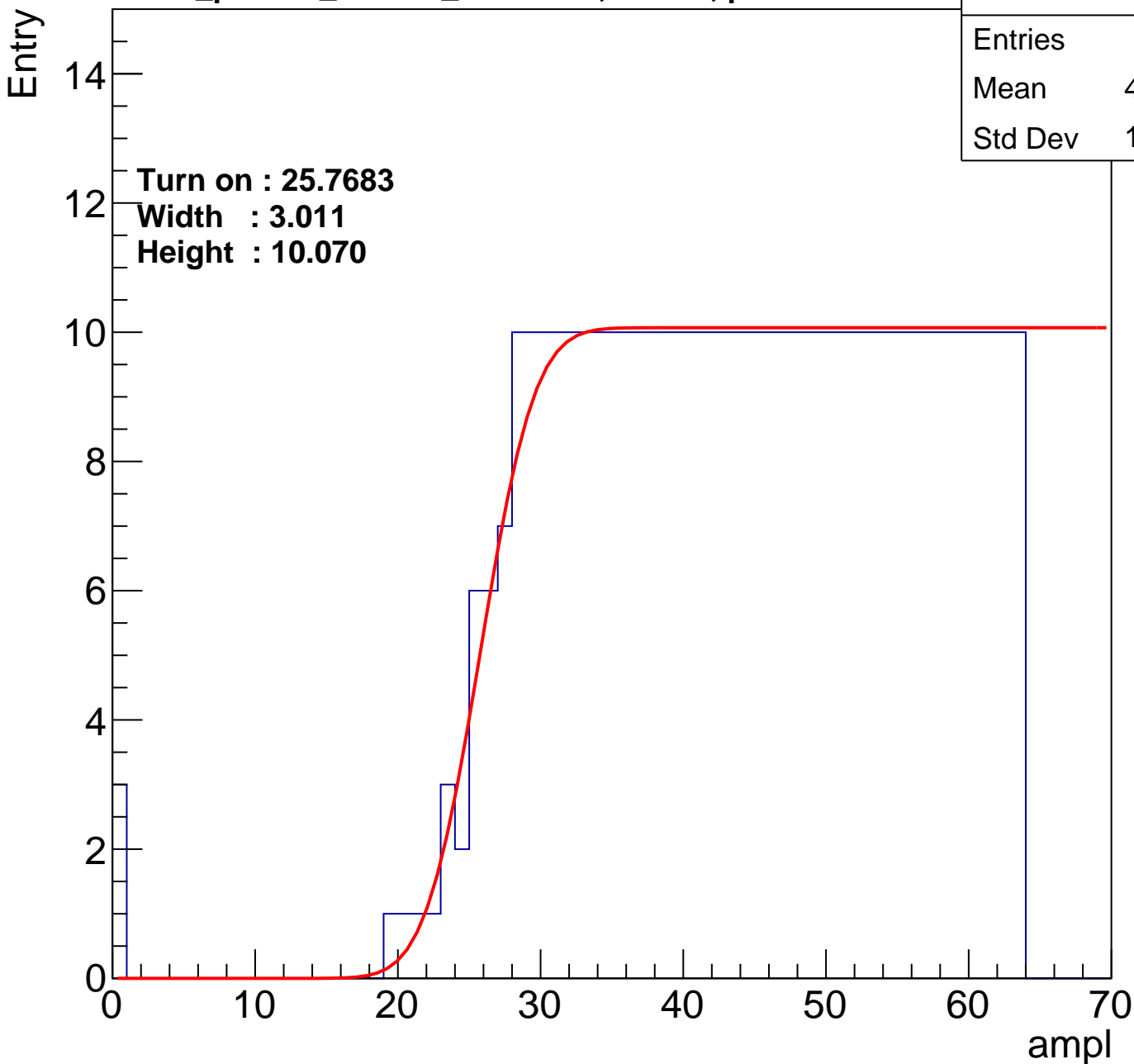
calib_packv5_042523_0143.root, FC#11, port A2

Entries	391
Mean	43.67
Std Dev	11.96

Turn on : 25.7683

Width : 3.011

Height : 10.070



B1L102S, U1-ch102

calib_packv5_042523_0143.root, FC#11, port A2

Entries	387
Mean	43.97
Std Dev	11.54

Turn on : 25.7532

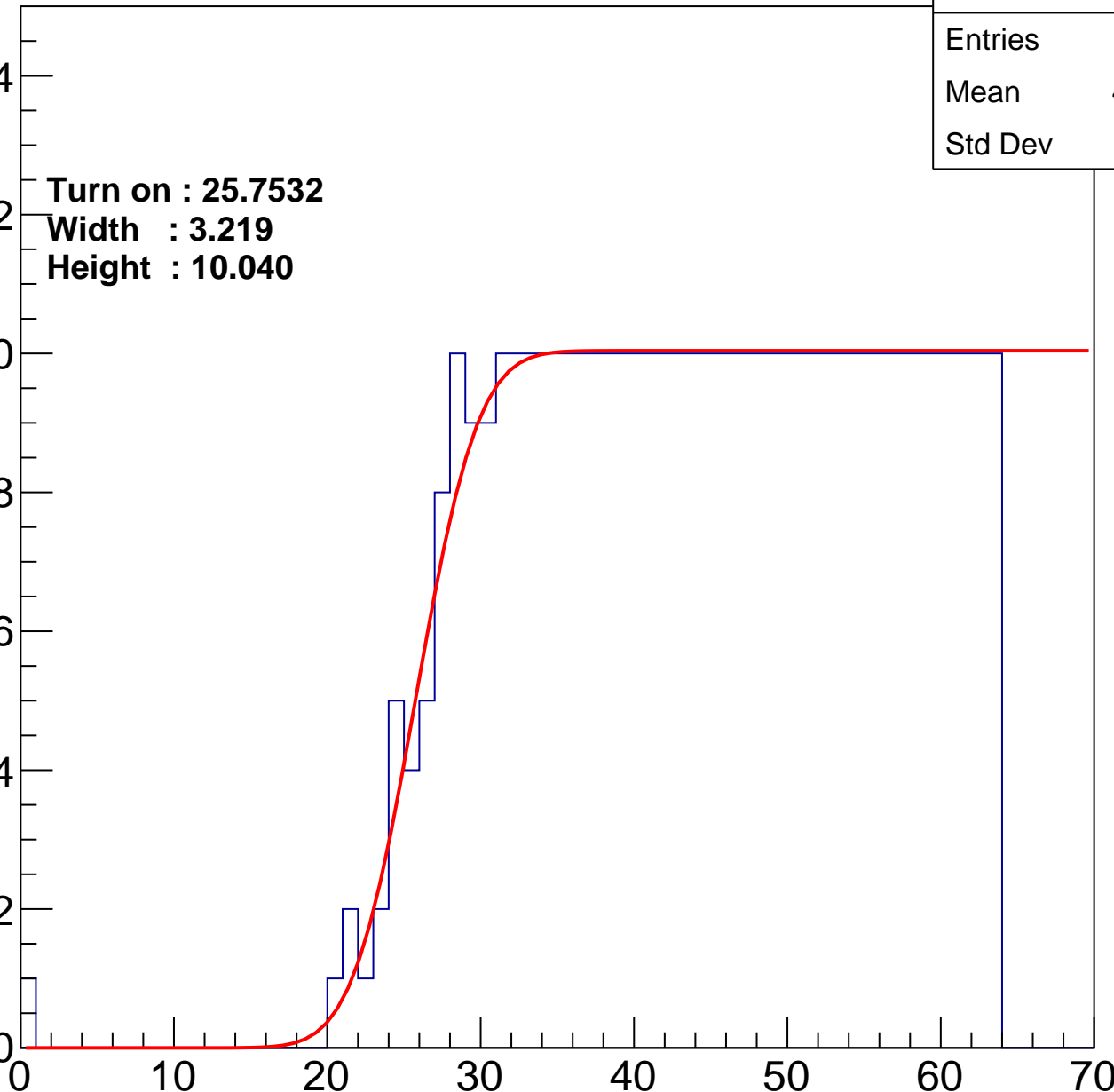
Width : 3.219

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch103

calib_packv5_042523_0143.root, FC#11, port A2

Entries	369
Mean	44.78
Std Dev	11.27

Turn on : 27.6136

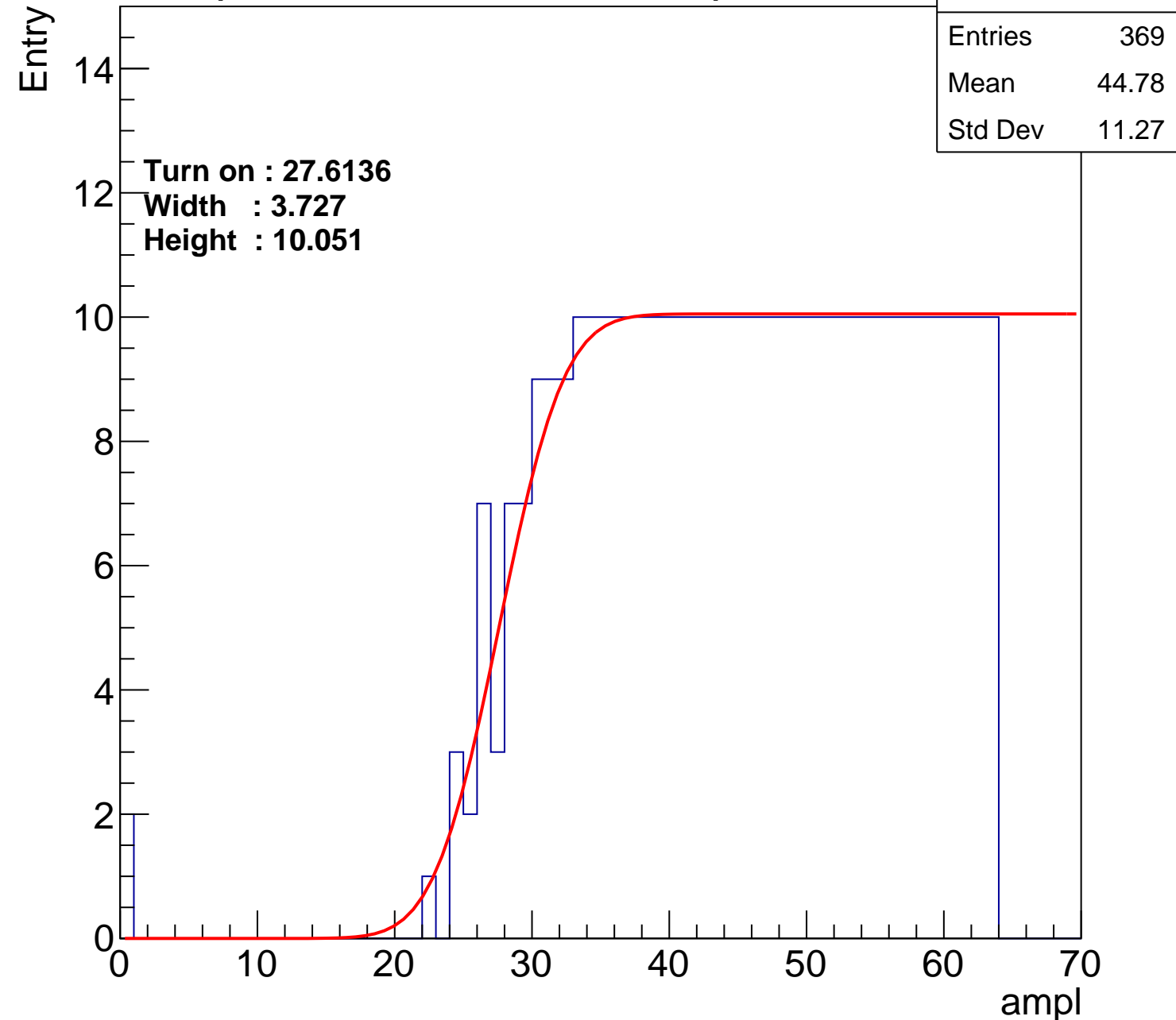
Width : 3.727

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch104

calib_packv5_042523_0143.root, FC#11, port A2

Entries	411
Mean	42.77
Std Dev	12.27

Turn on : 23.3896

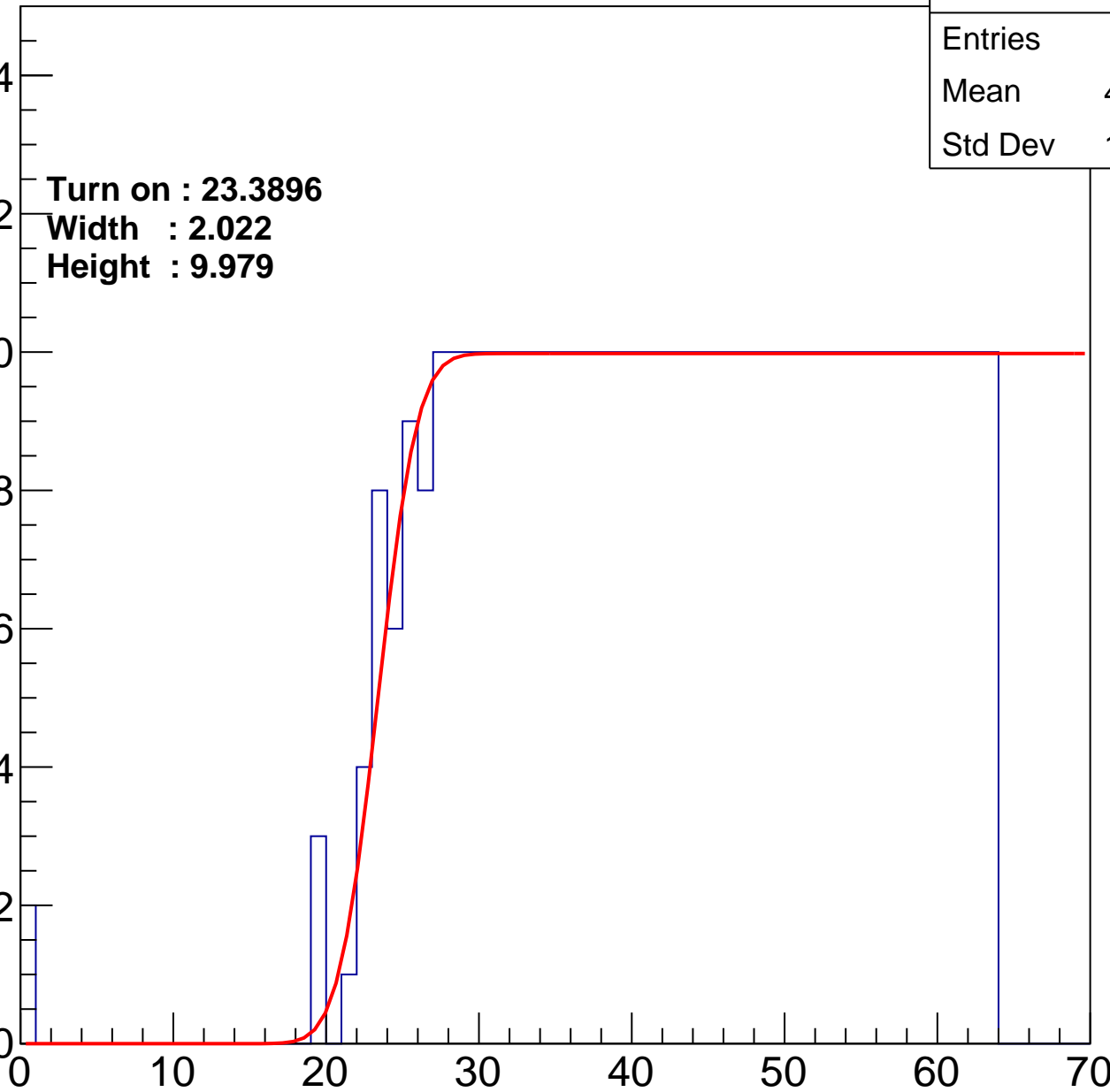
Width : 2.022

Height : 9.979

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch105

calib_packv5_042523_0143.root, FC#11, port A2

Entries	382
Mean	44.1
Std Dev	11.73

Turn on : 25.9355

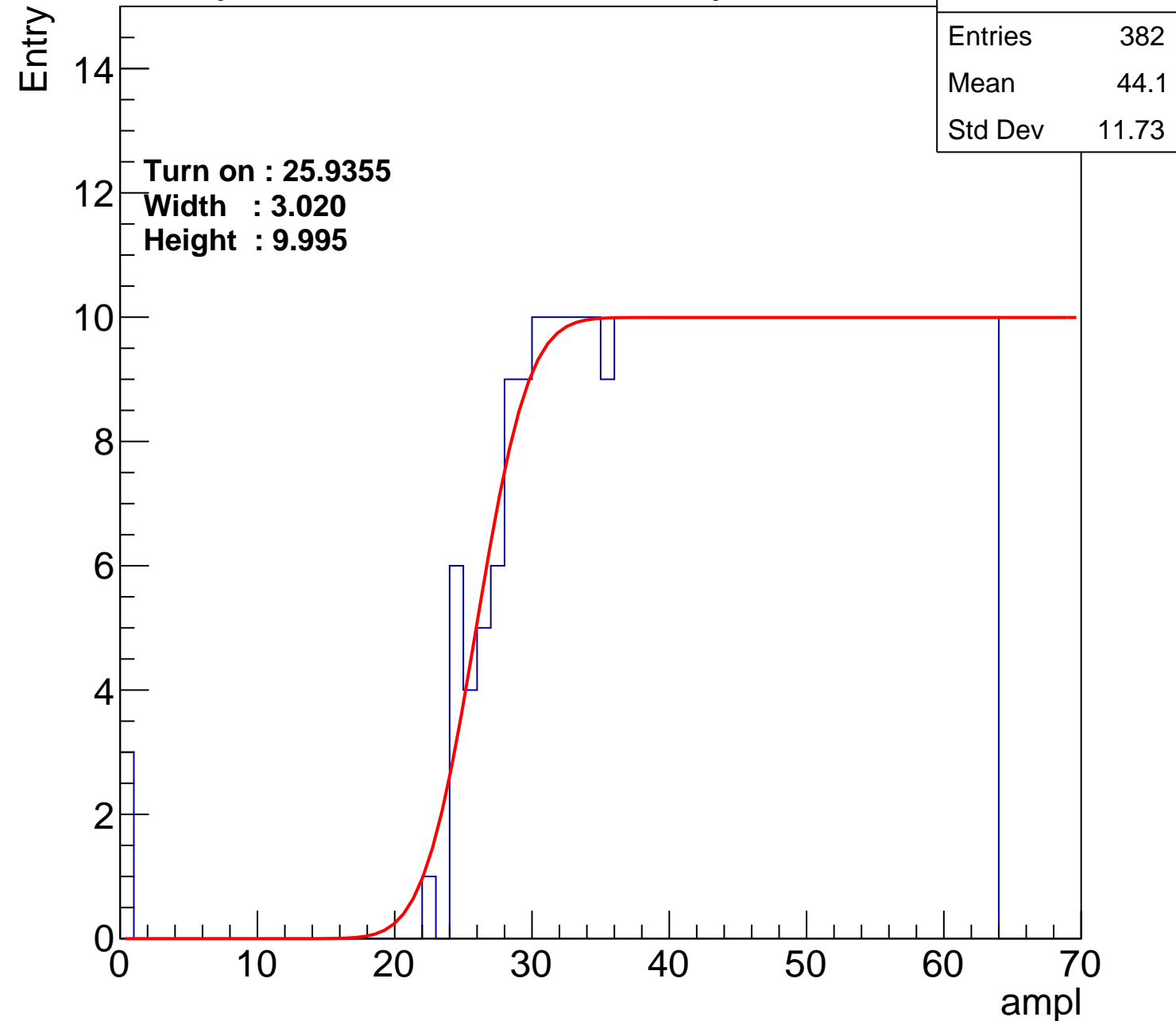
Width : 3.020

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch106

calib_packv5_042523_0143.root, FC#11, port A2

Entries	374
Mean	44.52
Std Dev	11.42

Turn on : 26.8740

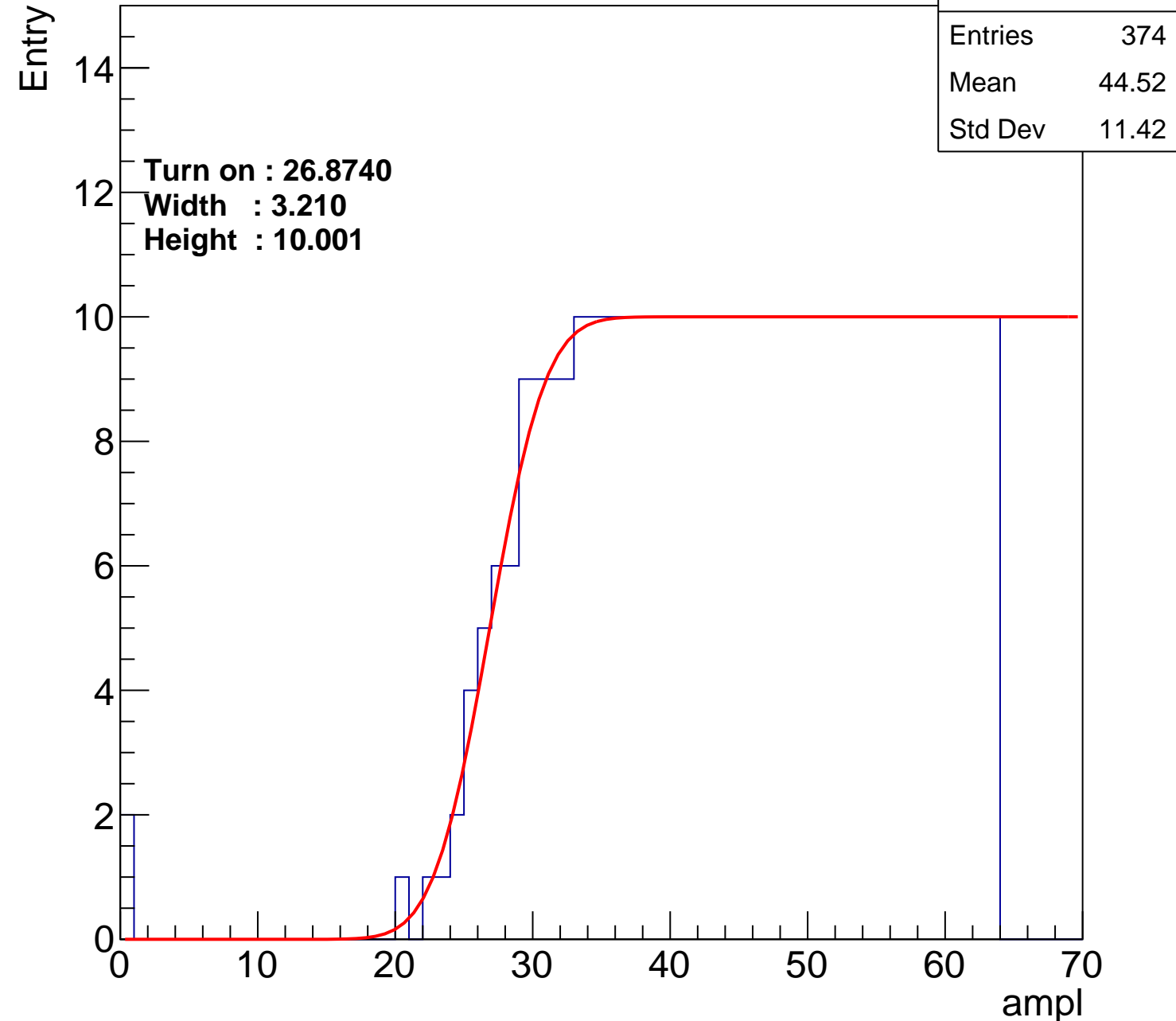
Width : 3.210

Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch107

calib_packv5_042523_0143.root, FC#11, port A2

Entries	398
Mean	43.15
Std Dev	12.57

Turn on : 24.9285

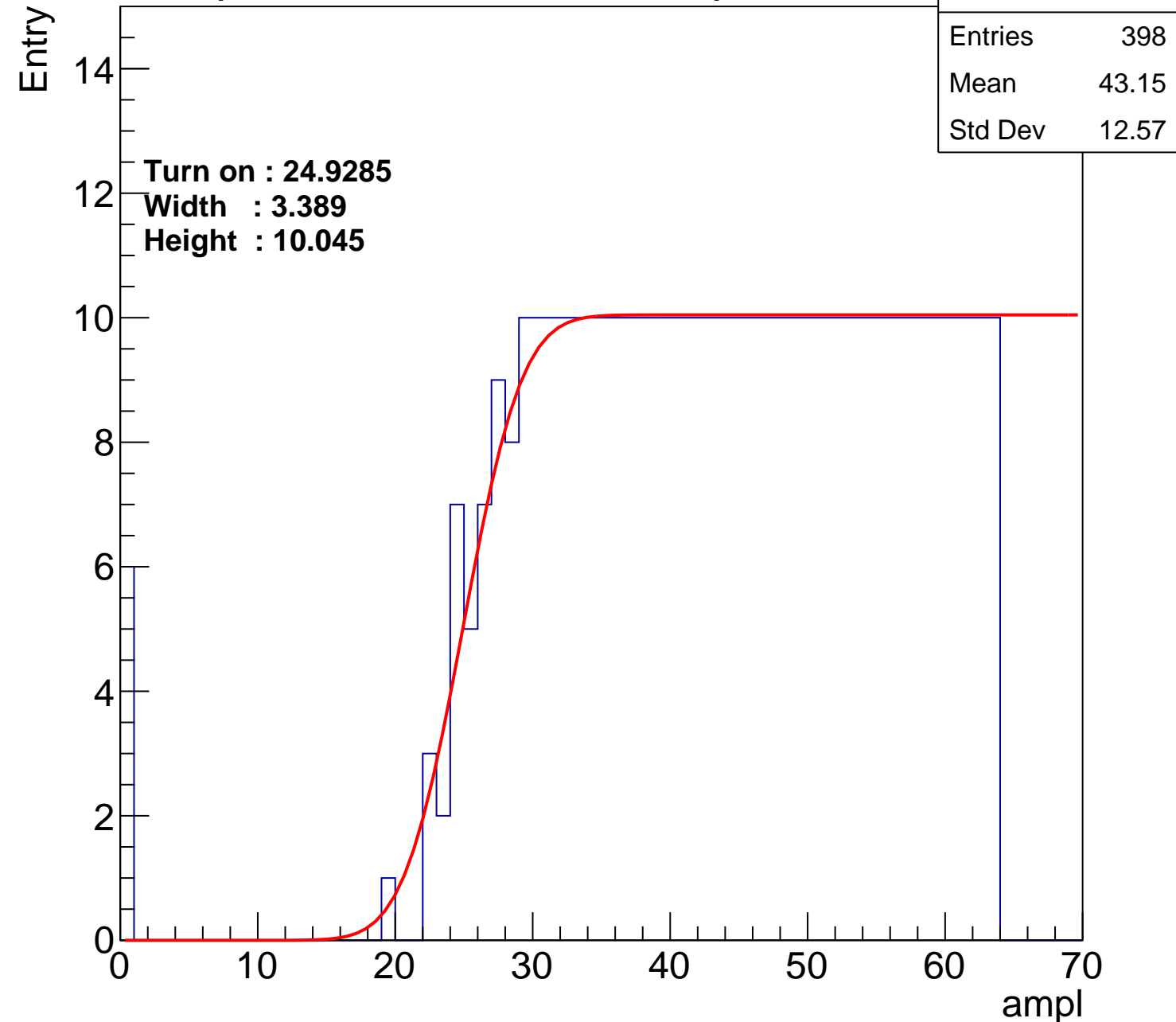
Width : 3.389

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch108

calib_packv5_042523_0143.root, FC#11, port A2

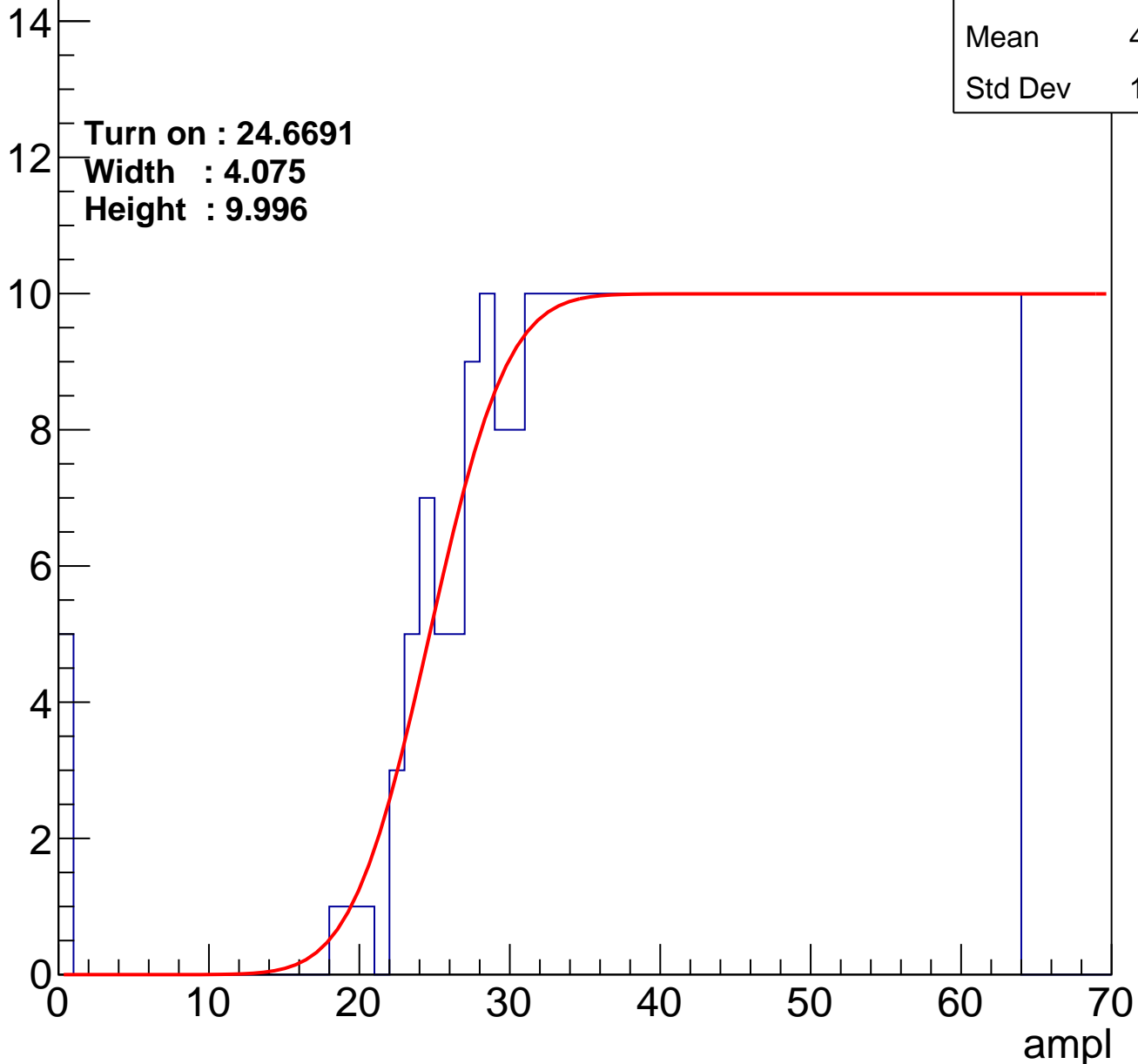
Entries	398
Mean	43.13
Std Dev	12.54

Turn on : 24.6691

Width : 4.075

Height : 9.996

Entry



B1L102S, U1-ch109

calib_packv5_042523_0143.root, FC#11, port A2

Entries	398
Mean	43.24
Std Dev	12.25

Turn on : 24.7199

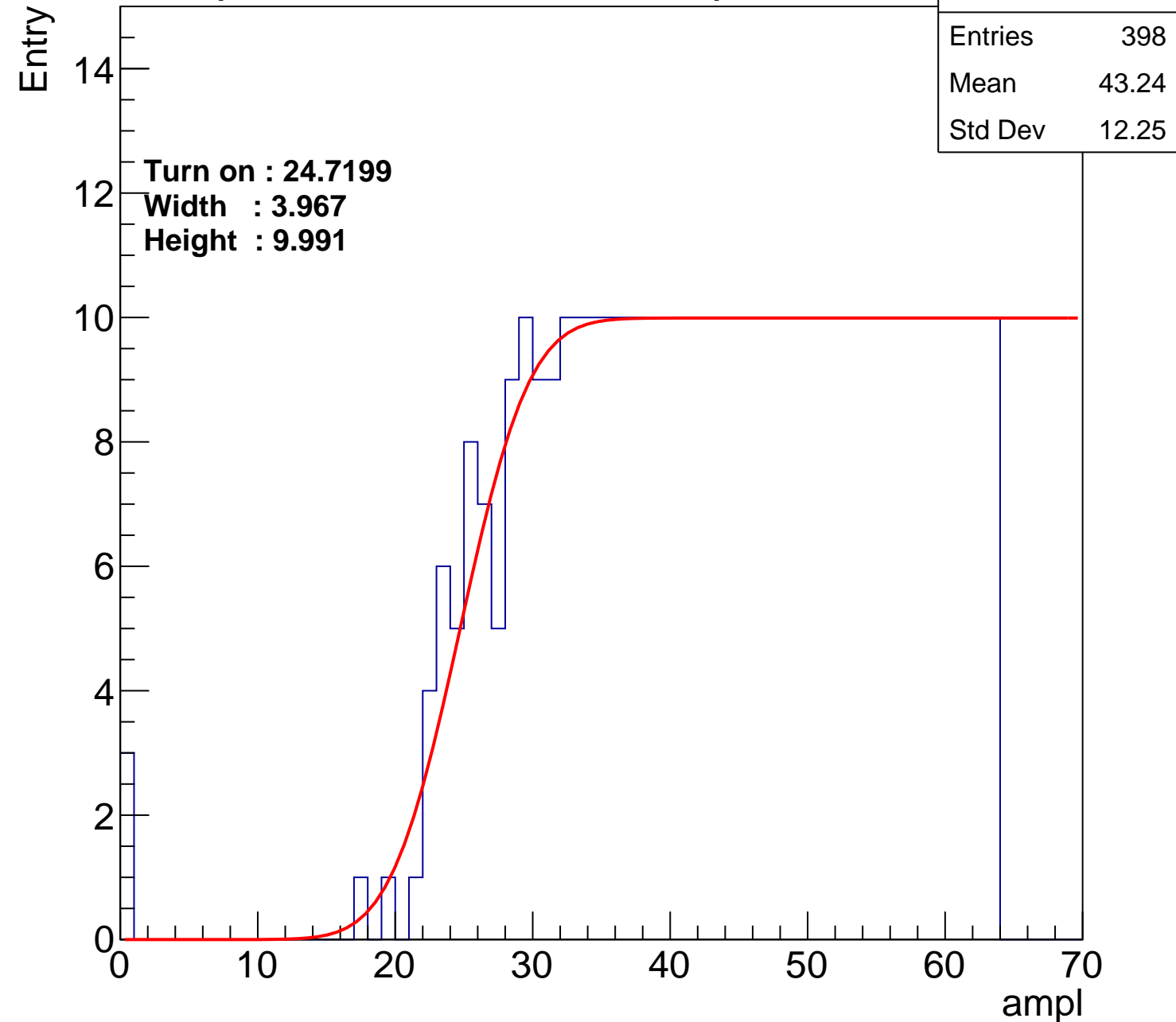
Width : 3.967

Height : 9.991

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch110

calib_packv5_042523_0143.root, FC#11, port A2

Entries	395
Mean	43.45
Std Dev	12.07

Turn on : 24.8477

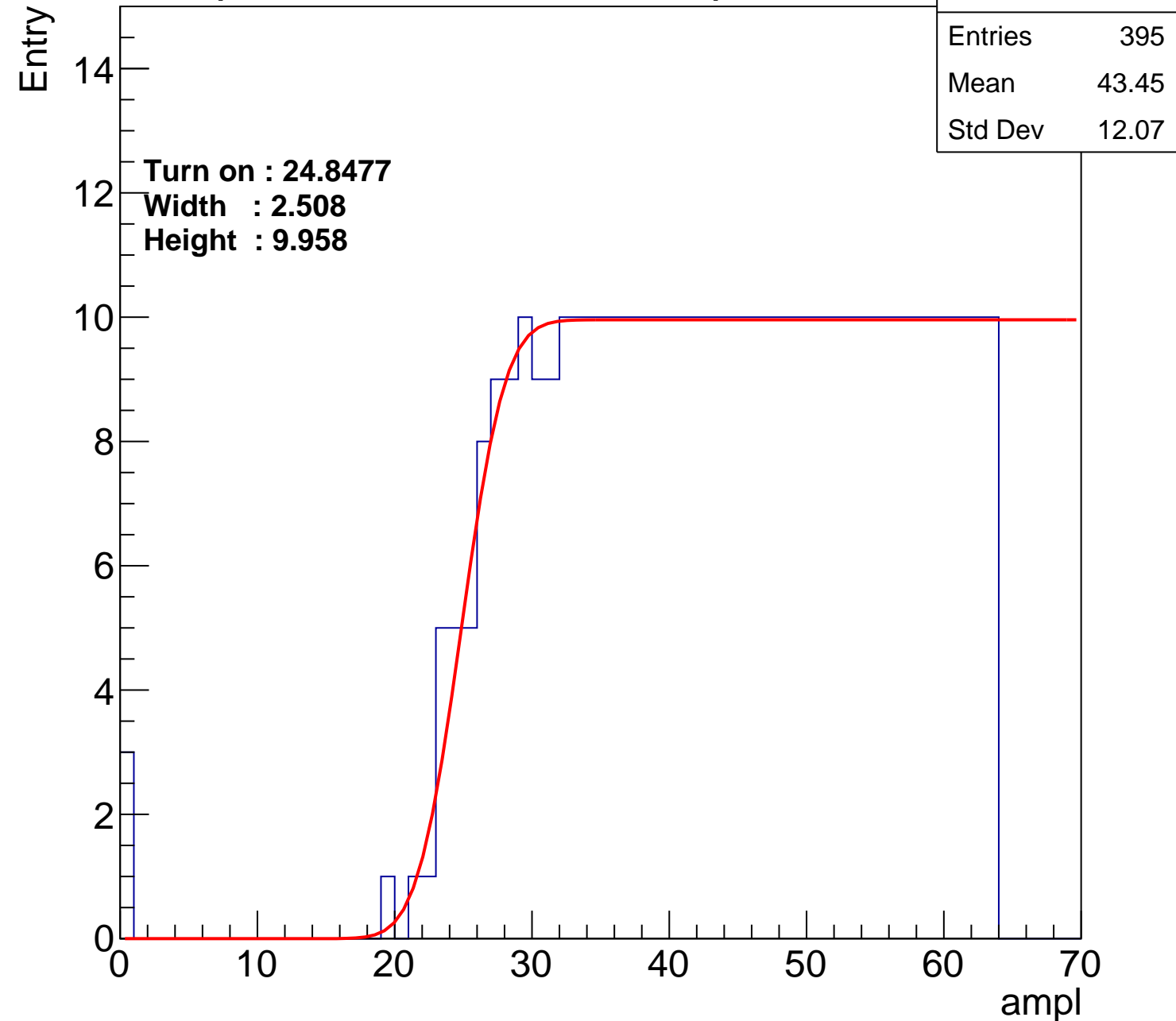
Width : 2.508

Height : 9.958

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch111

calib_packv5_042523_0143.root, FC#11, port A2

Entries	399
Mean	43.15
Std Dev	12.46

Turn on : 25.0279

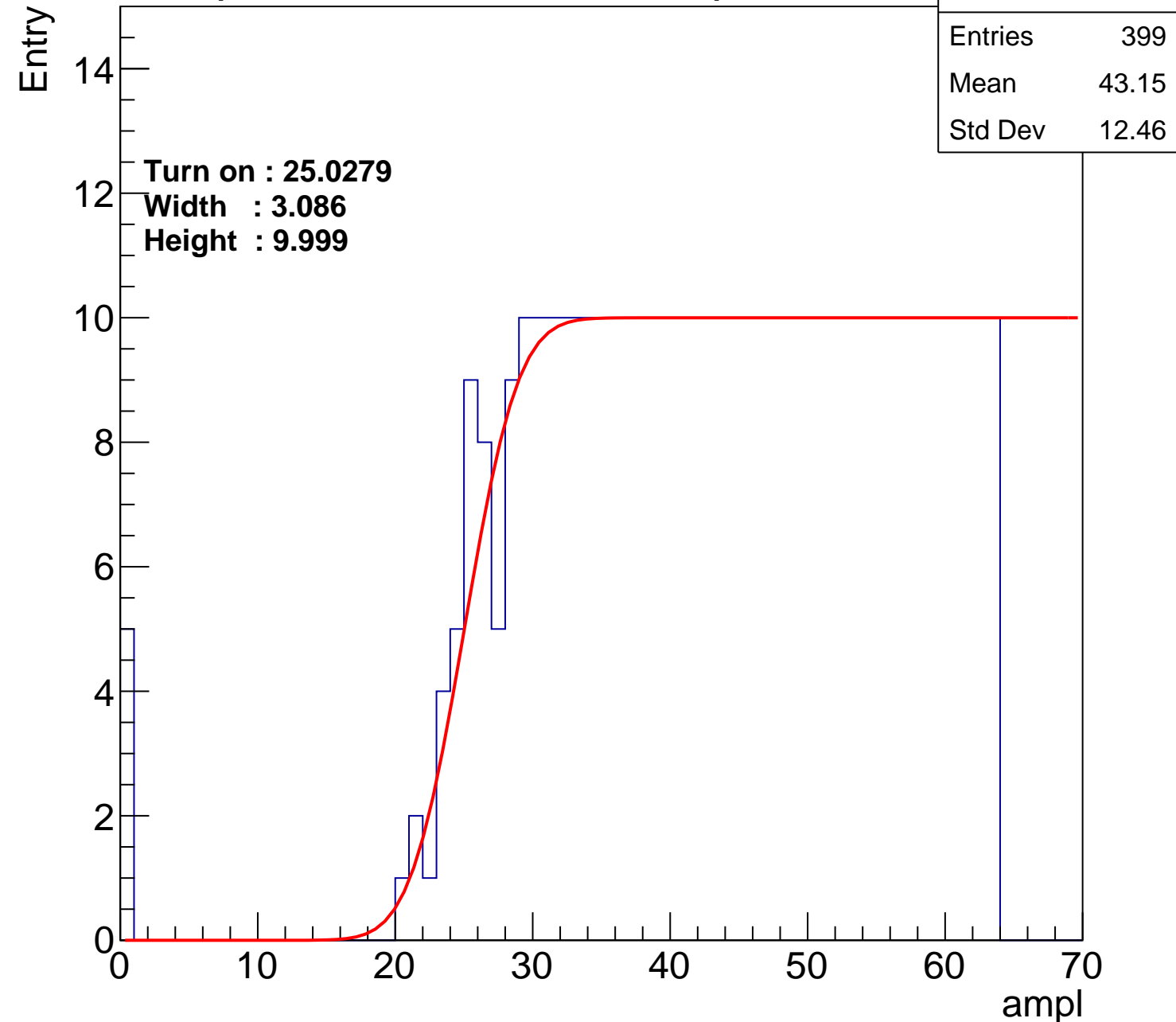
Width : 3.086

Height : 9.999

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch112

calib_packv5_042523_0143.root, FC#11, port A2

Entries	389
Mean	43.67
Std Dev	12.11

Turn on : 25.8202

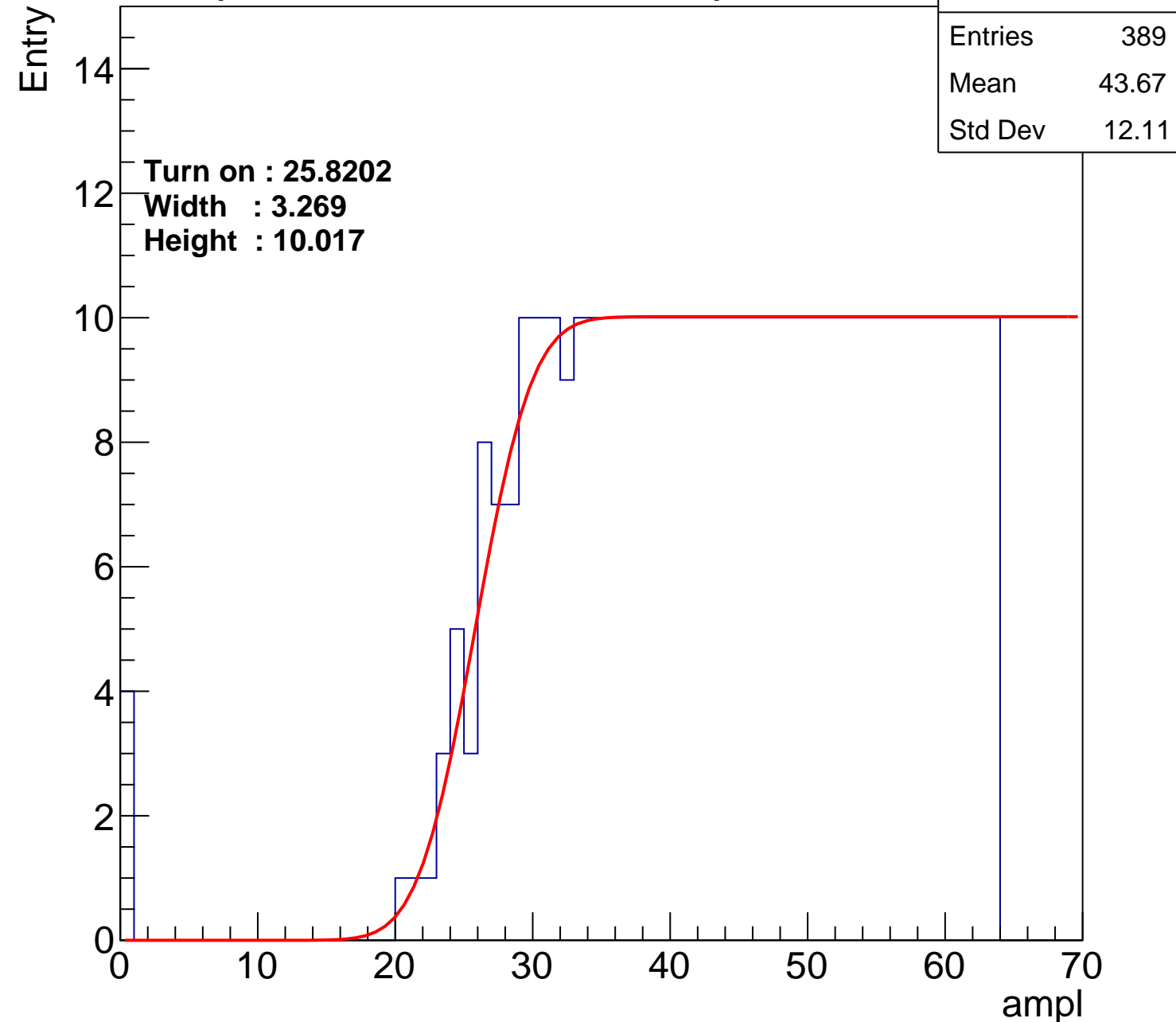
Width : 3.269

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch113

calib_packv5_042523_0143.root, FC#11, port A2

Entries	385
Mean	44.06
Std Dev	11.5

Turn on : 25.8772

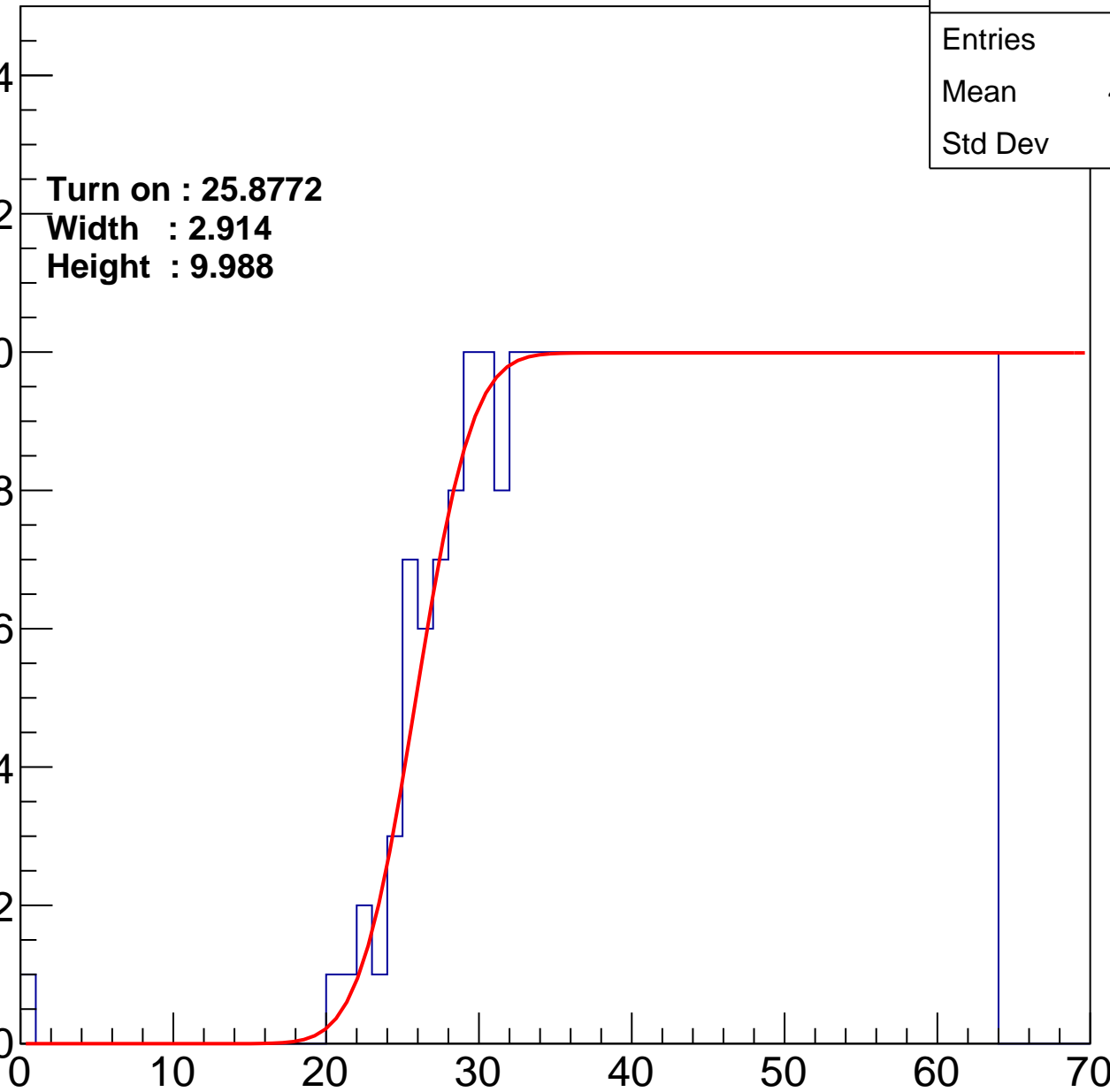
Width : 2.914

Height : 9.988

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch114

calib_packv5_042523_0143.root, FC#11, port A2

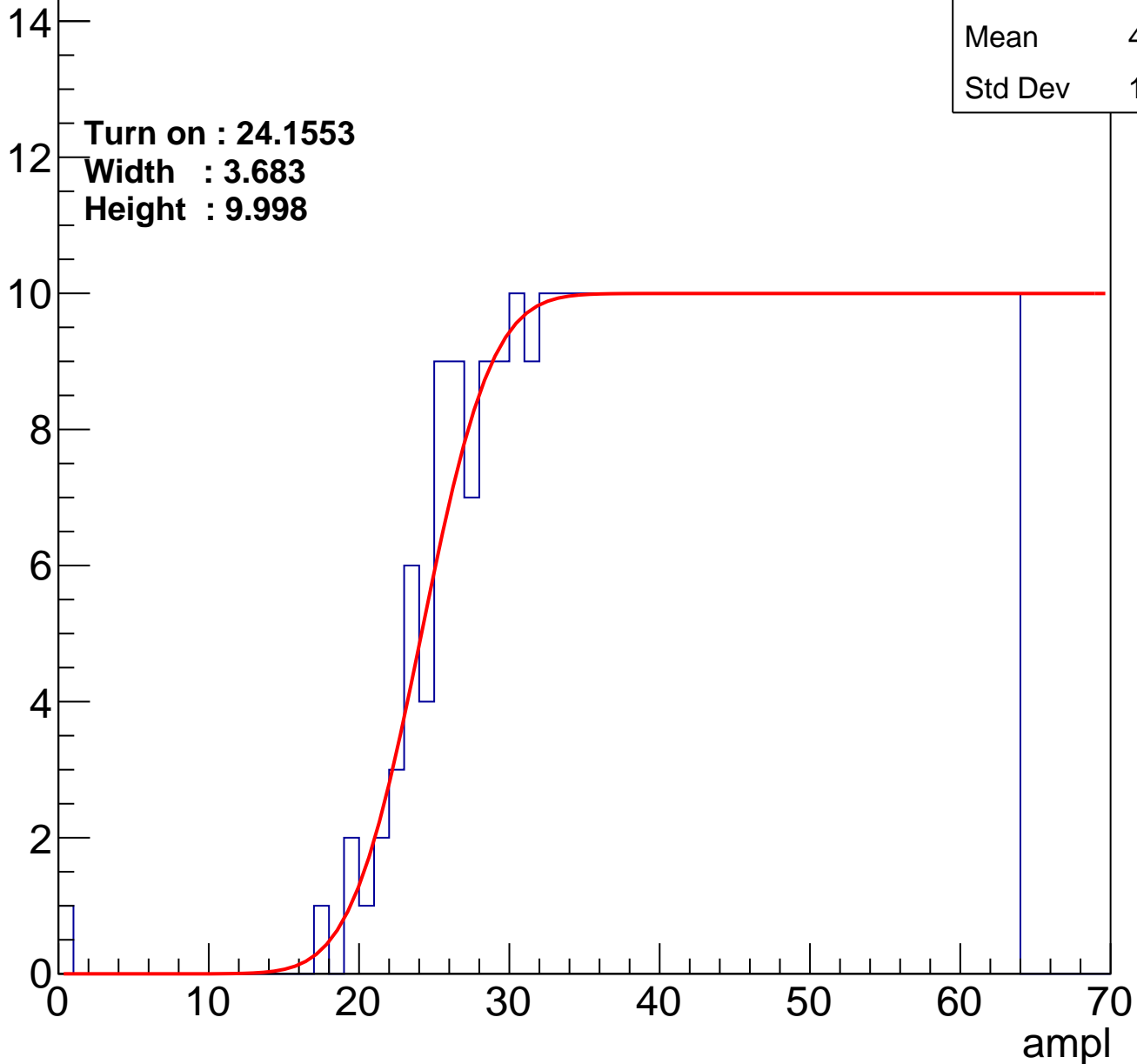
Entries	402
Mean	43.18
Std Dev	12.03

Turn on : 24.1553

Width : 3.683

Height : 9.998

Entry



B1L102S, U1-ch115

calib_packv5_042523_0143.root, FC#11, port A2

Entries	392
Mean	43.53
Std Dev	12.18

Turn on : 25.0361

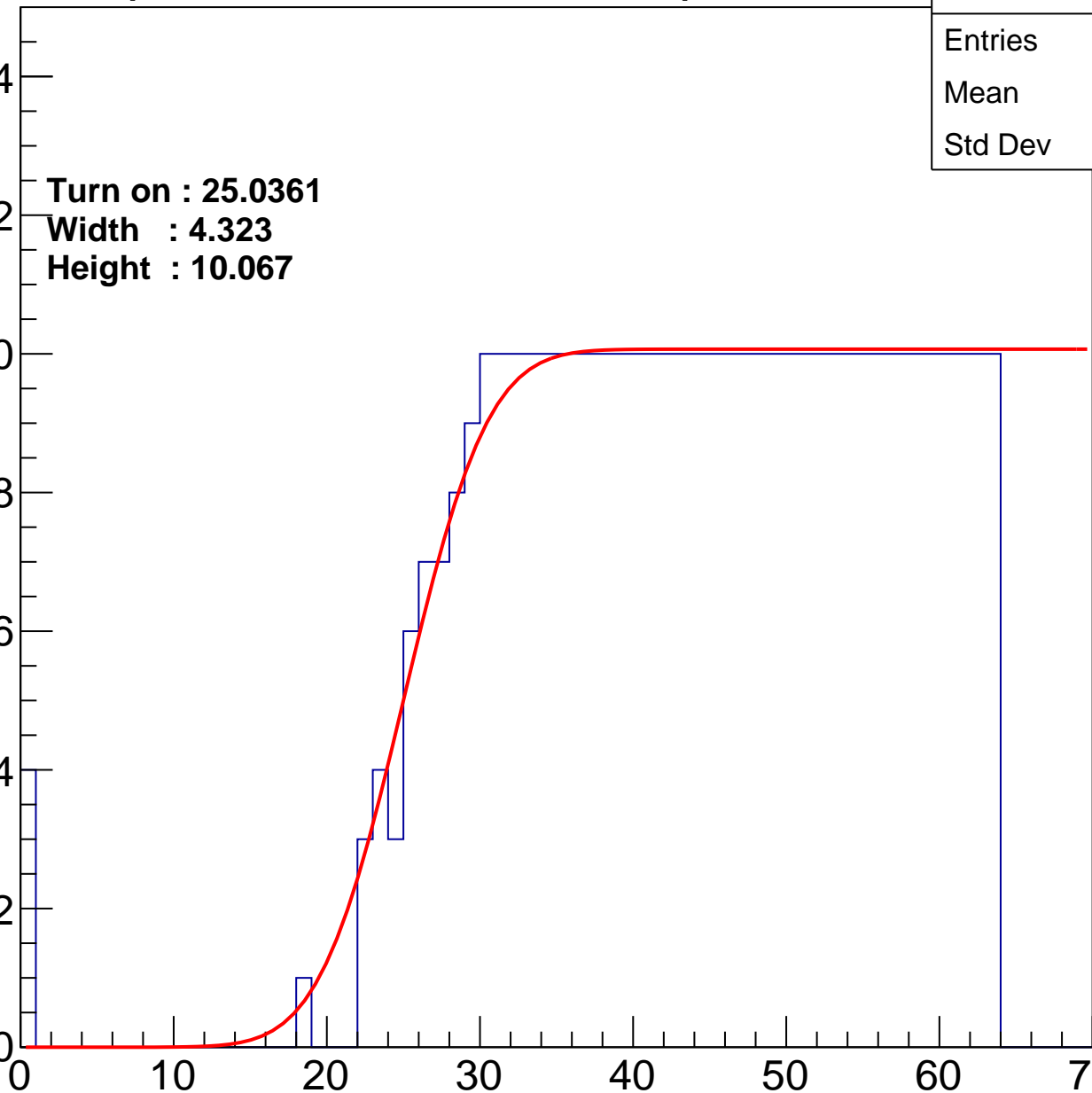
Width : 4.323

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch116

calib_packv5_042523_0143.root, FC#11, port A2

Entries	383
Mean	43.98
Std Dev	11.89

Turn on : 26.6190

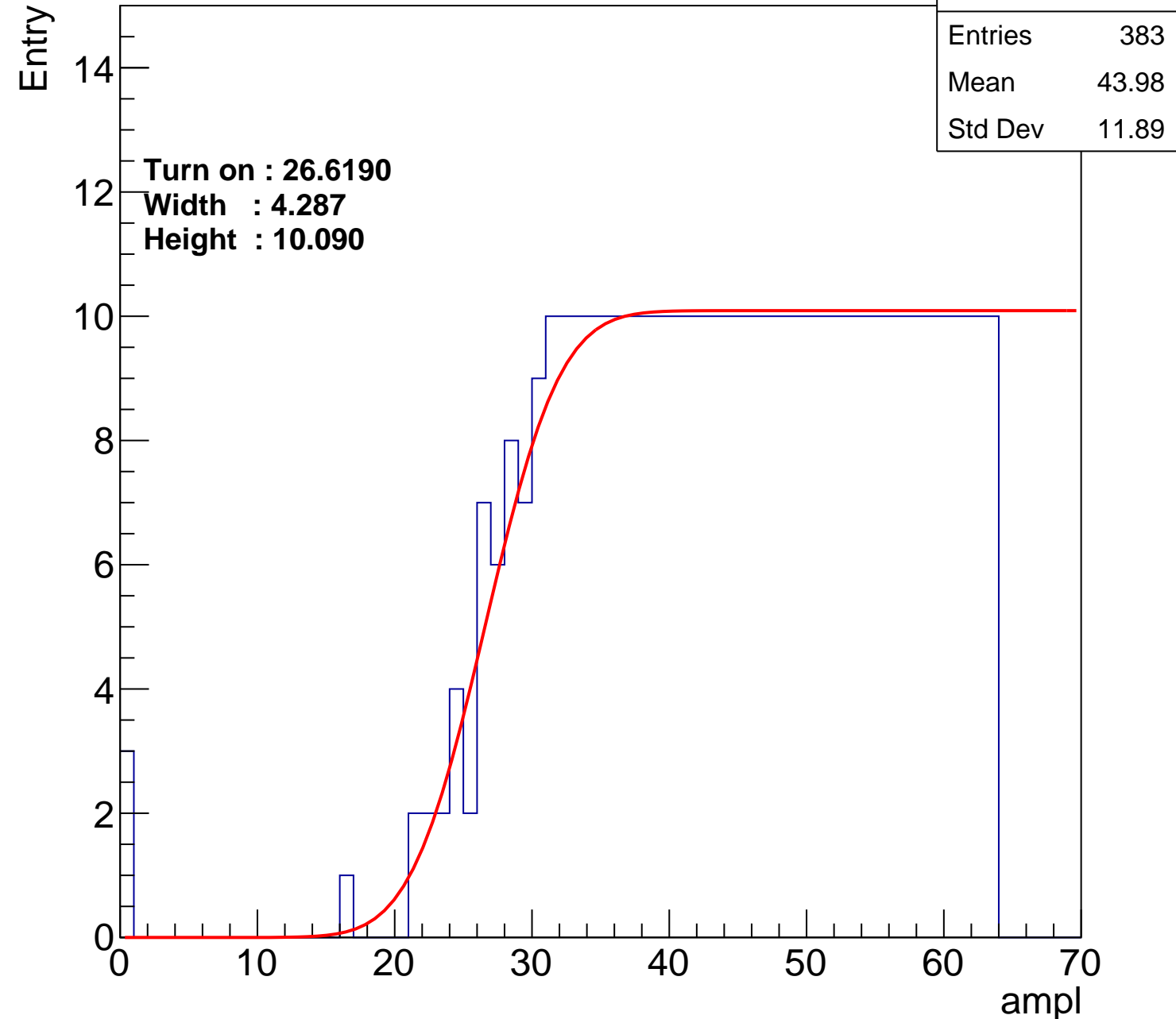
Width : 4.287

Height : 10.090

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch117

calib_packv5_042523_0143.root, FC#11, port A2

Entries	389
Mean	43.84
Std Dev	11.66

Turn on : 25.6535

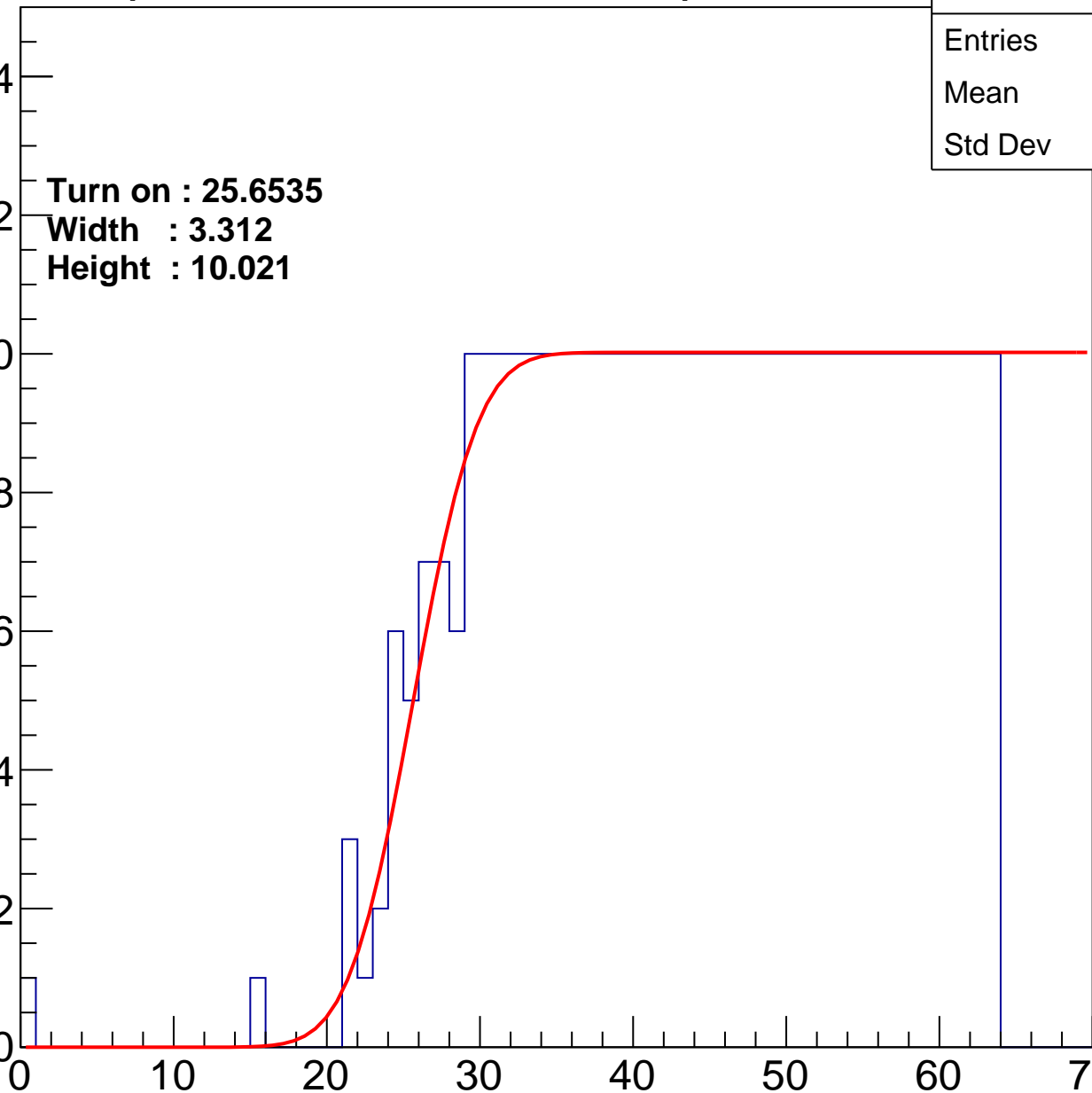
Width : 3.312

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch118

calib_packv5_042523_0143.root, FC#11, port A2

Entries	405
Mean	42.94
Std Dev	12.36

Turn on : 24.3921

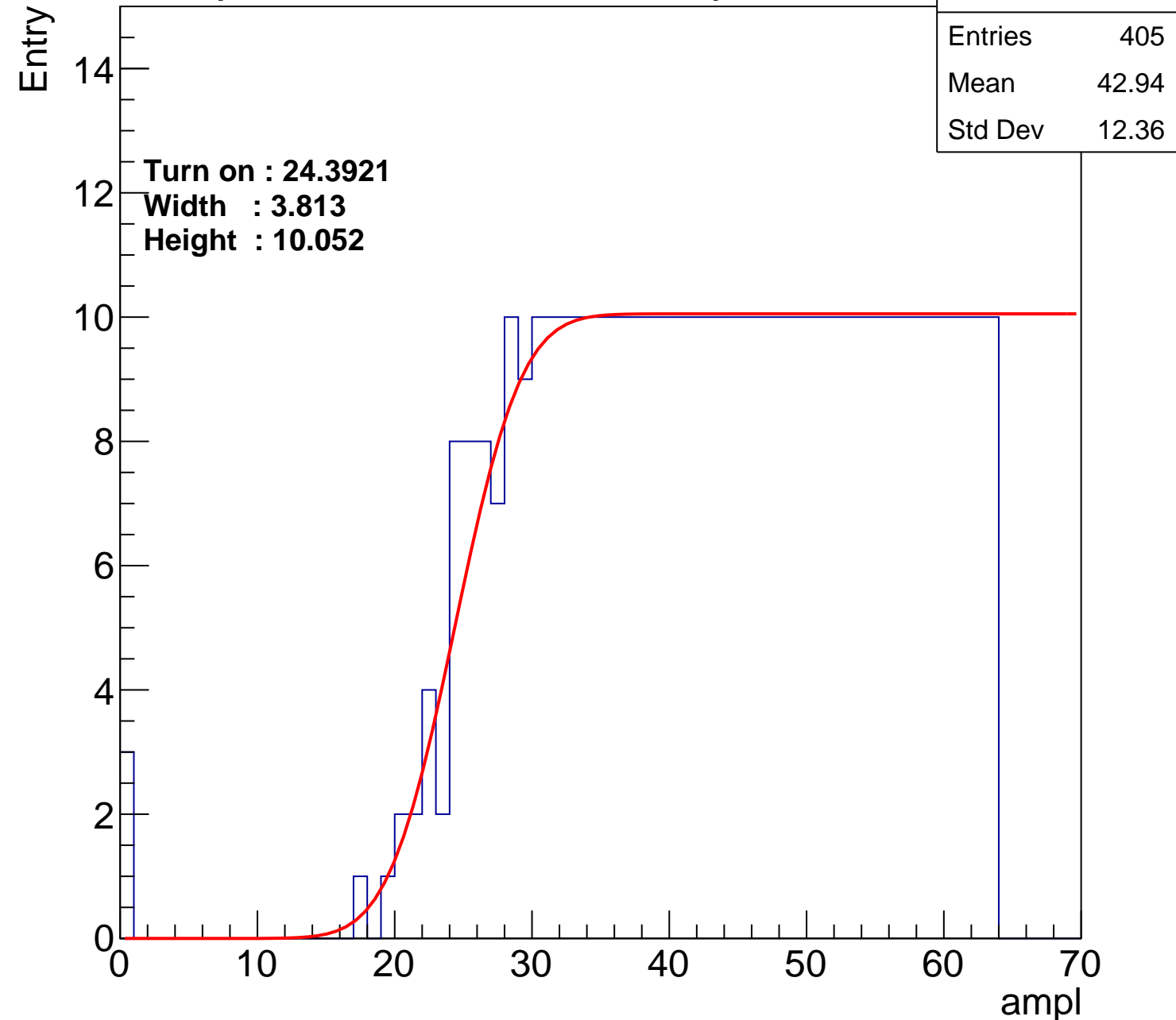
Width : 3.813

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch119

calib_packv5_042523_0143.root, FC#11, port A2

Entries	370
Mean	44.5
Std Dev	11.9

Turn on : 27.5283

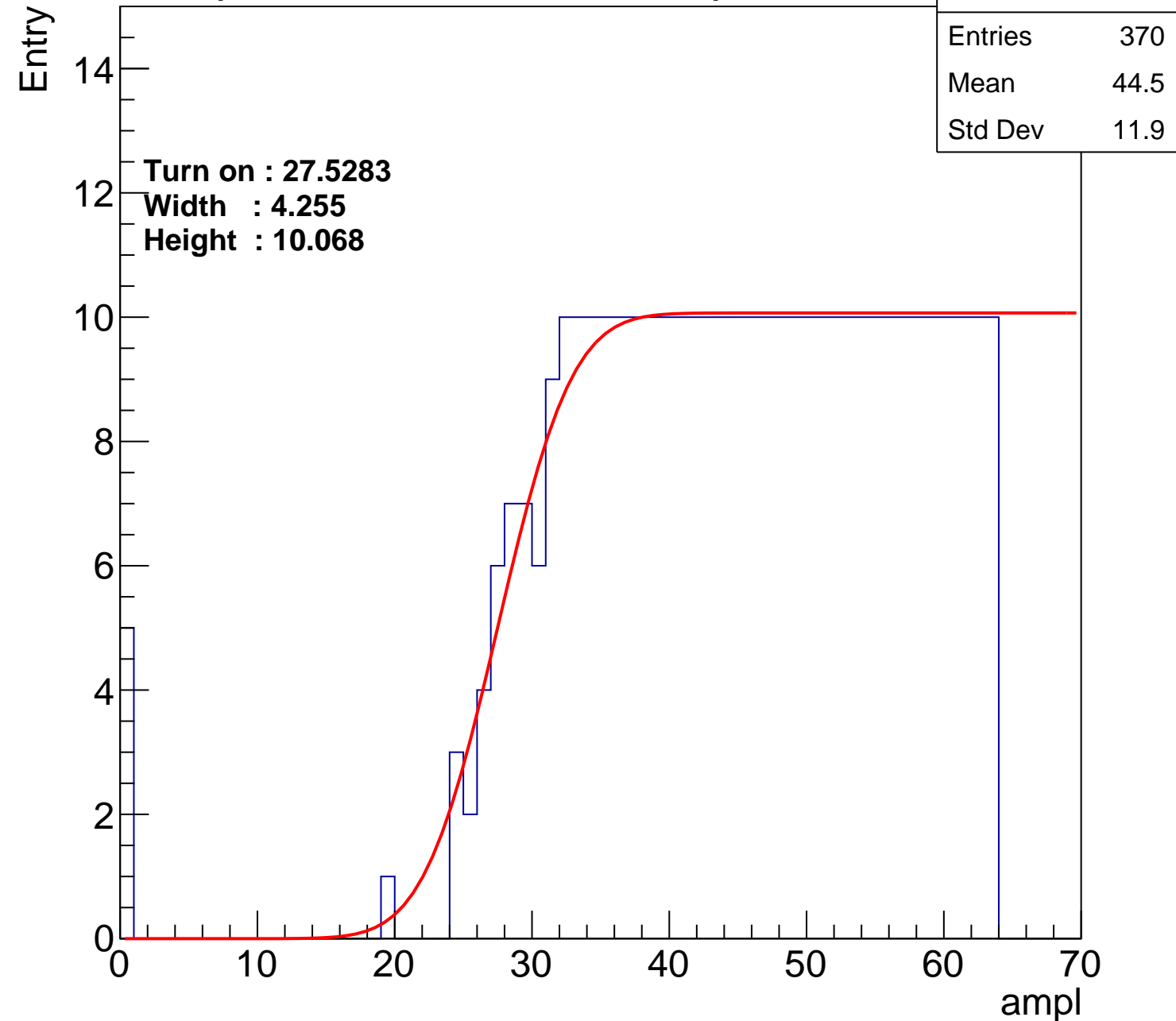
Width : 4.255

Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch120

calib_packv5_042523_0143.root, FC#11, port A2

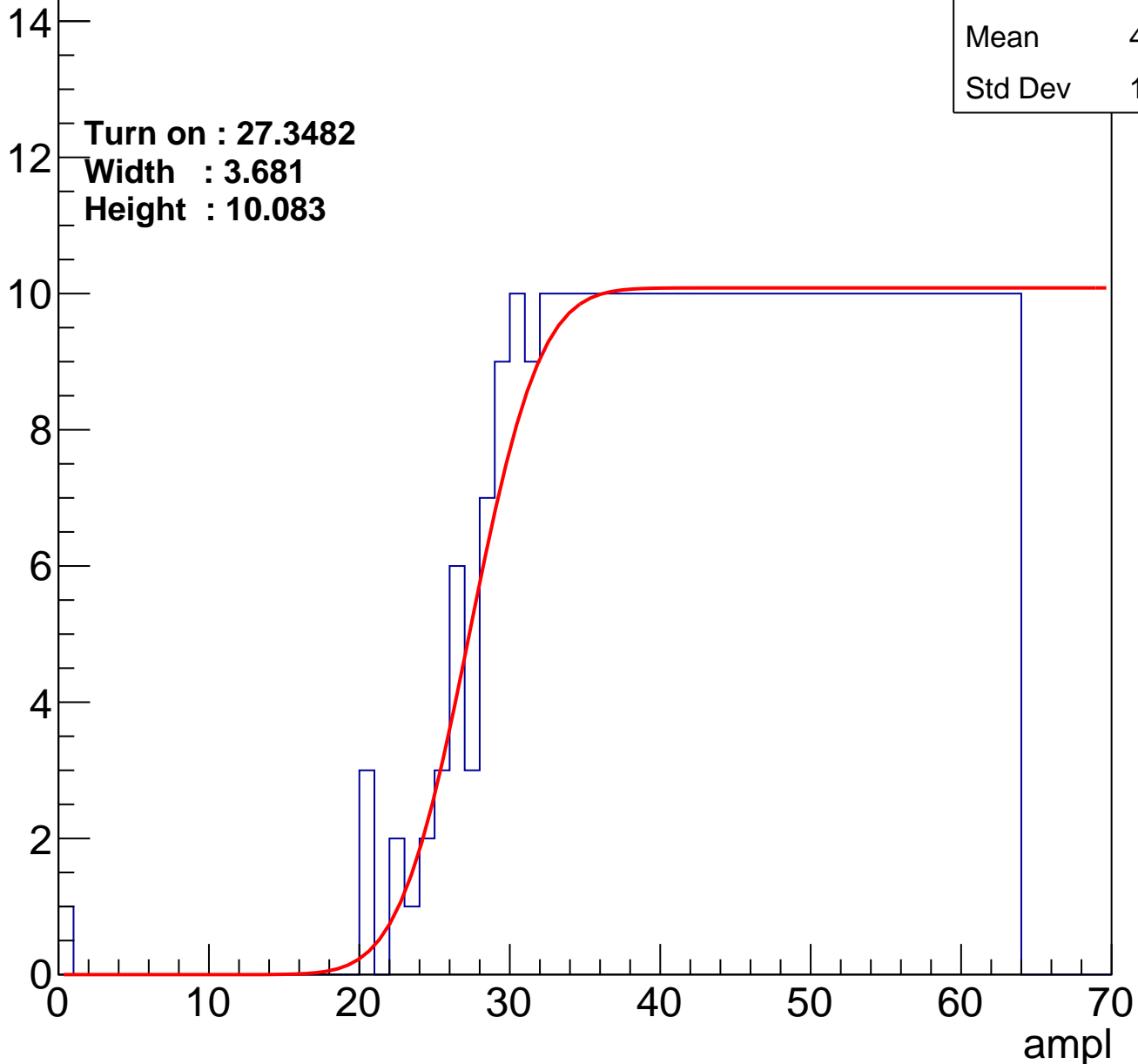
Entries	376
Mean	44.48
Std Dev	11.32

Turn on : 27.3482

Width : 3.681

Height : 10.083

Entry



B1L102S, U1-ch121

calib_packv5_042523_0143.root, FC#11, port A2

Entries	400
Mean	43.17
Std Dev	12.31

Turn on : 23.9664

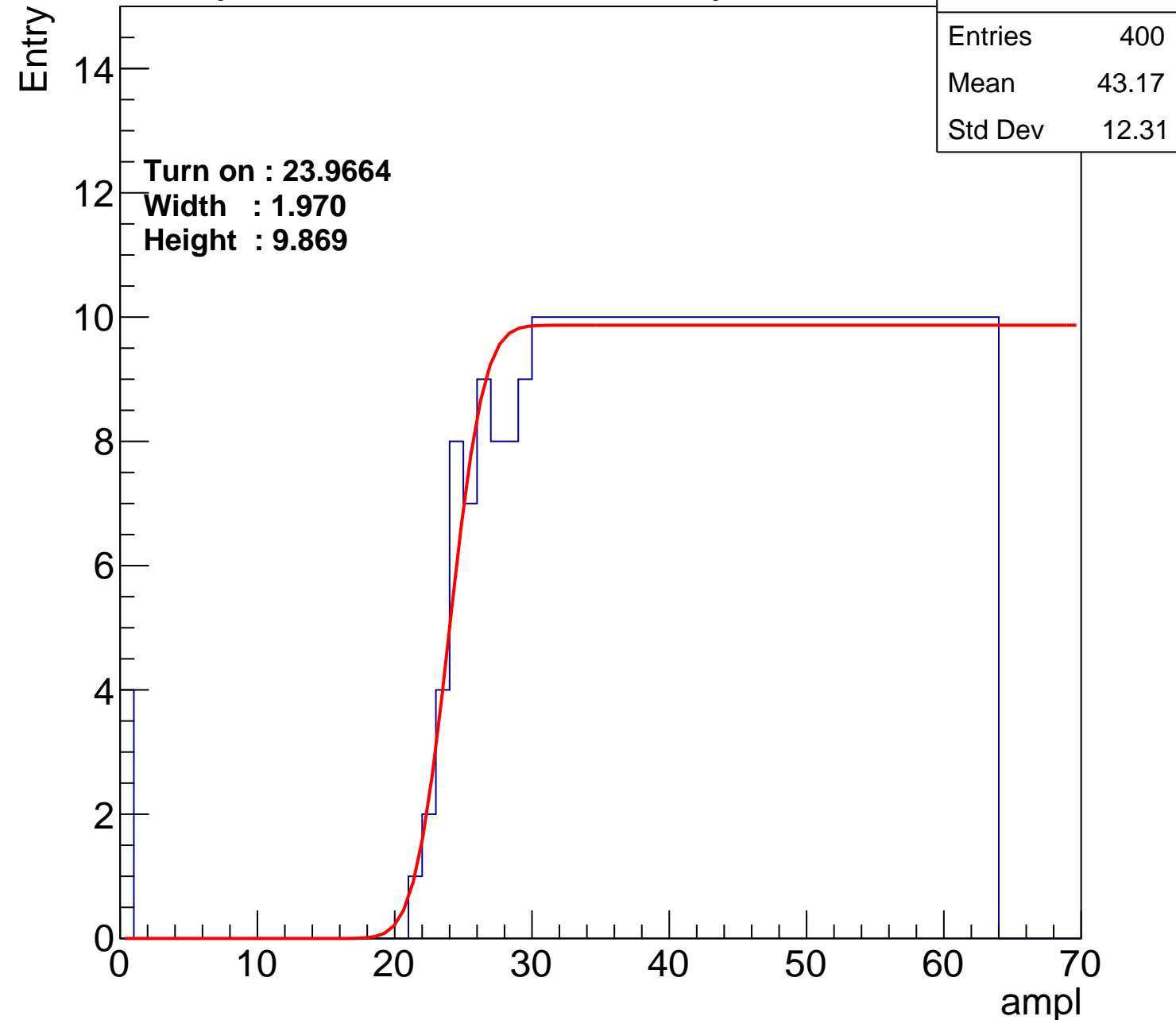
Width : 1.970

Height : 9.869

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch122

calib_packv5_042523_0143.root, FC#11, port A2

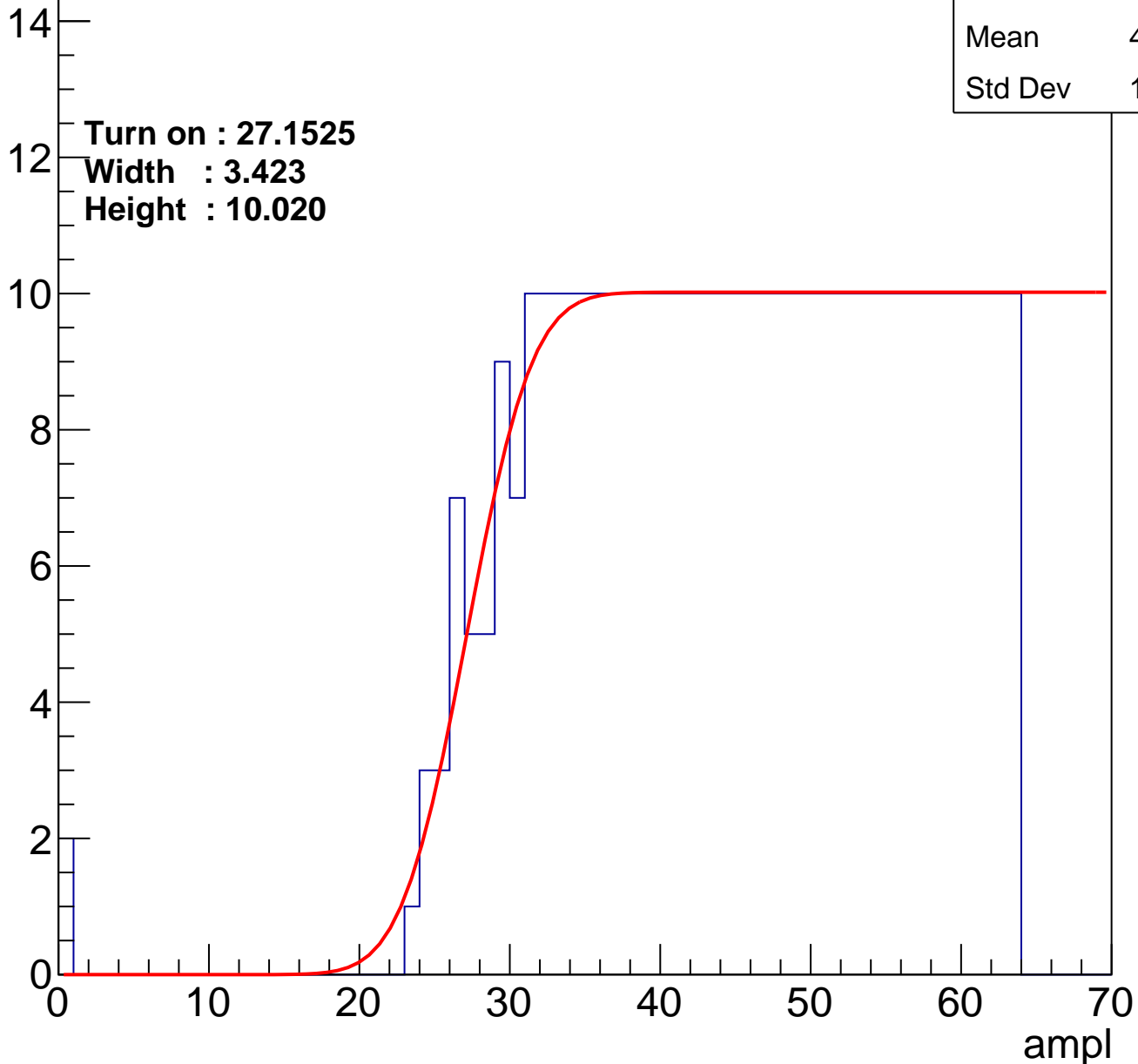
Entries	372
Mean	44.65
Std Dev	11.33

Turn on : 27.1525

Width : 3.423

Height : 10.020

Entry



B1L102S, U1-ch123

calib_packv5_042523_0143.root, FC#11, port A2

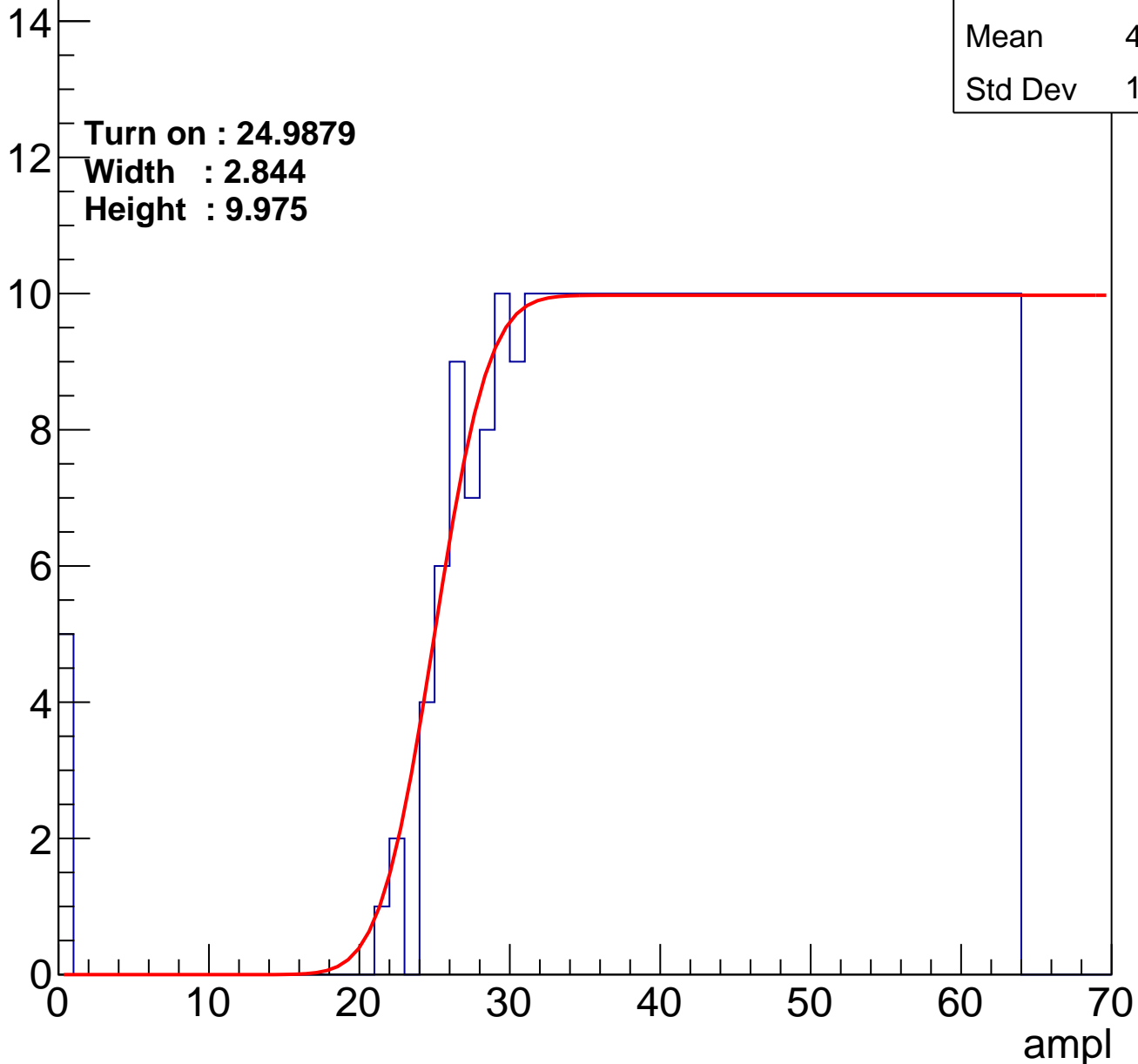
Entries	391
Mean	43.55
Std Dev	12.26

Turn on : 24.9879

Width : 2.844

Height : 9.975

Entry



B1L102S, U1-ch124

calib_packv5_042523_0143.root, FC#11, port A2

Entries	389
Mean	43.68
Std Dev	12.03

Turn on : 25.2816

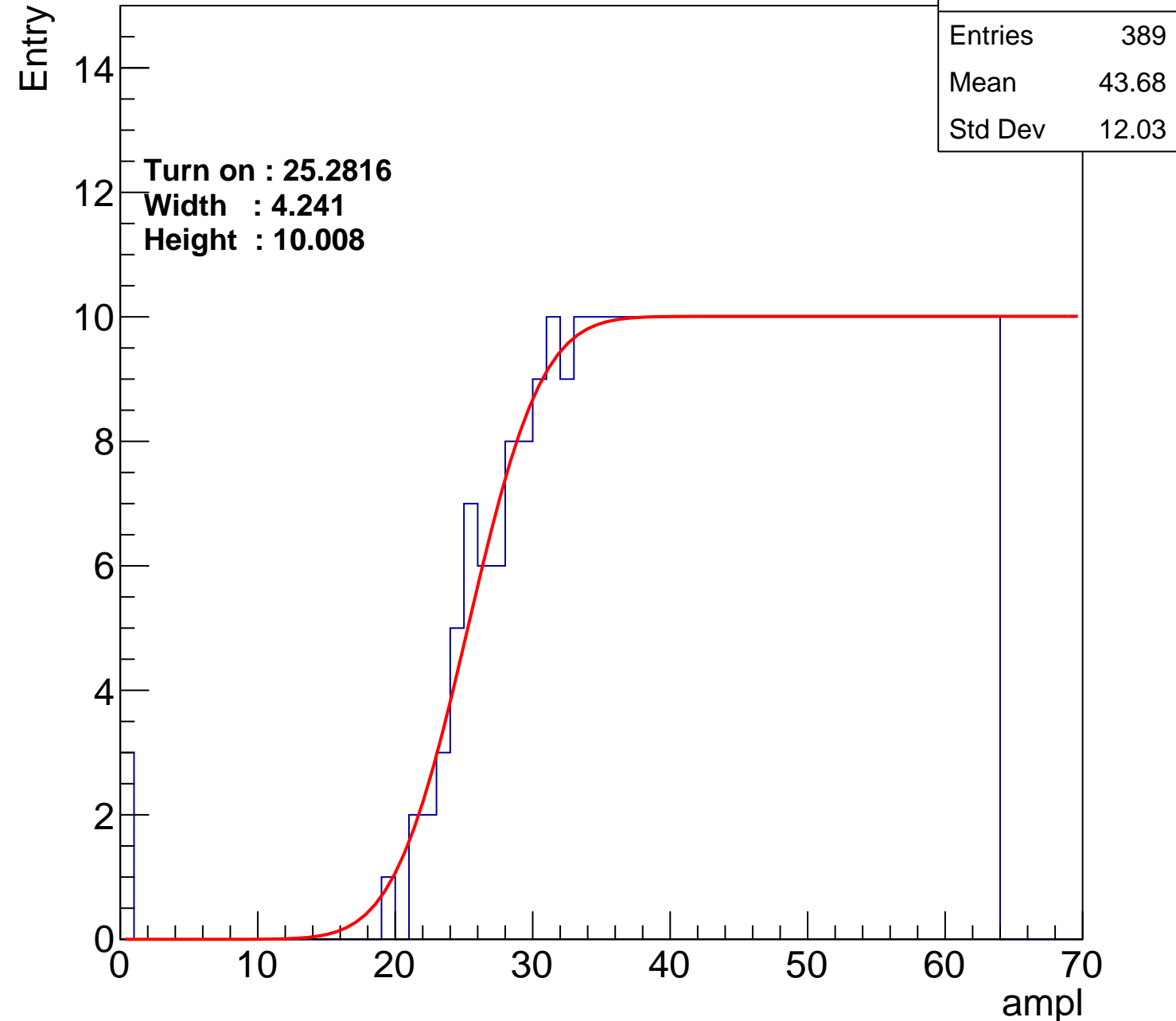
Width : 4.241

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch125

calib_packv5_042523_0143.root, FC#11, port A2

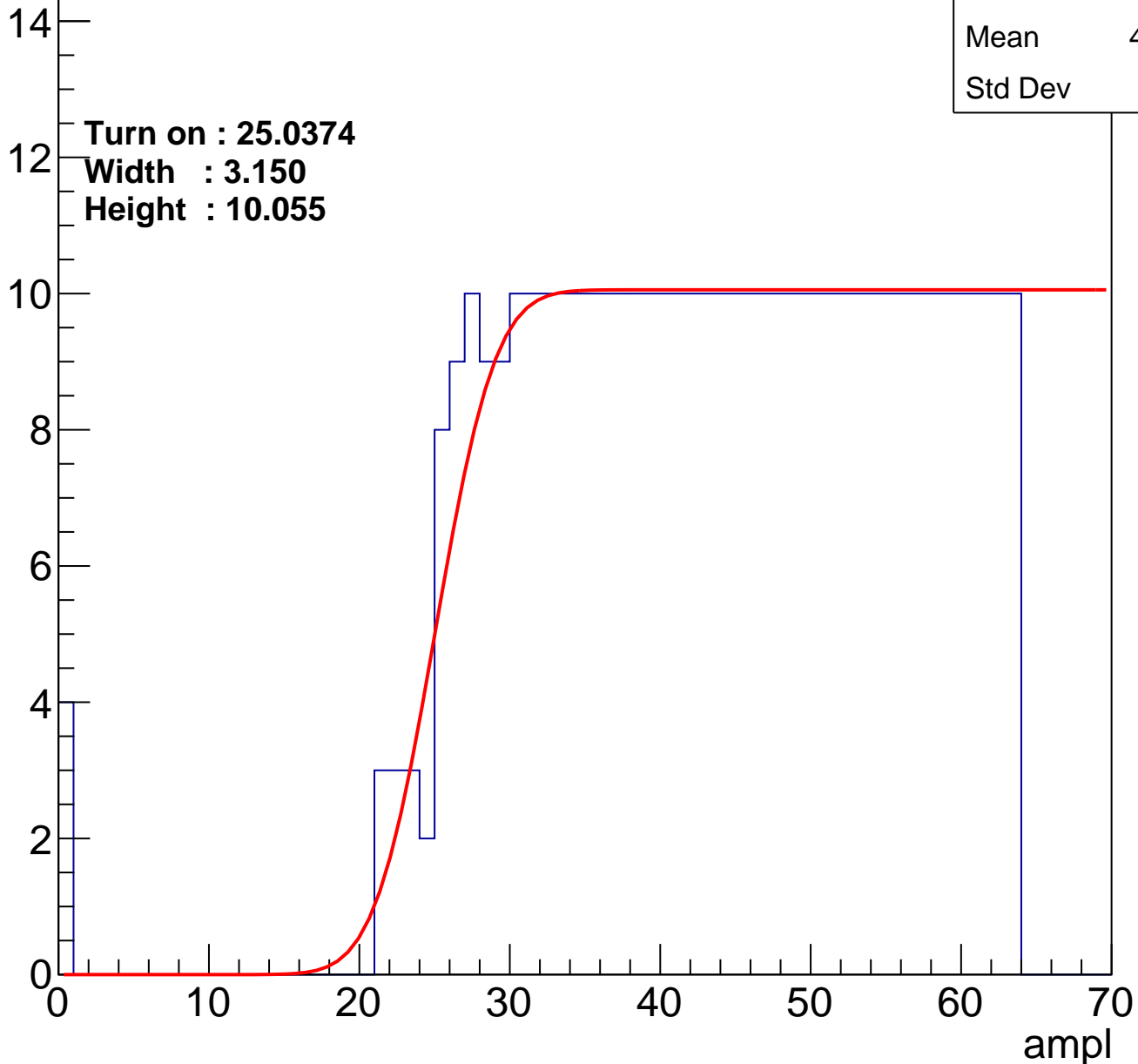
Entries	400
Mean	43.18
Std Dev	12.3

Turn on : 25.0374

Width : 3.150

Height : 10.055

Entry



B1L102S, U1-ch126

calib_packv5_042523_0143.root, FC#11, port A2

Entries	391
Mean	43.58
Std Dev	12.22

Turn on : 25.6185

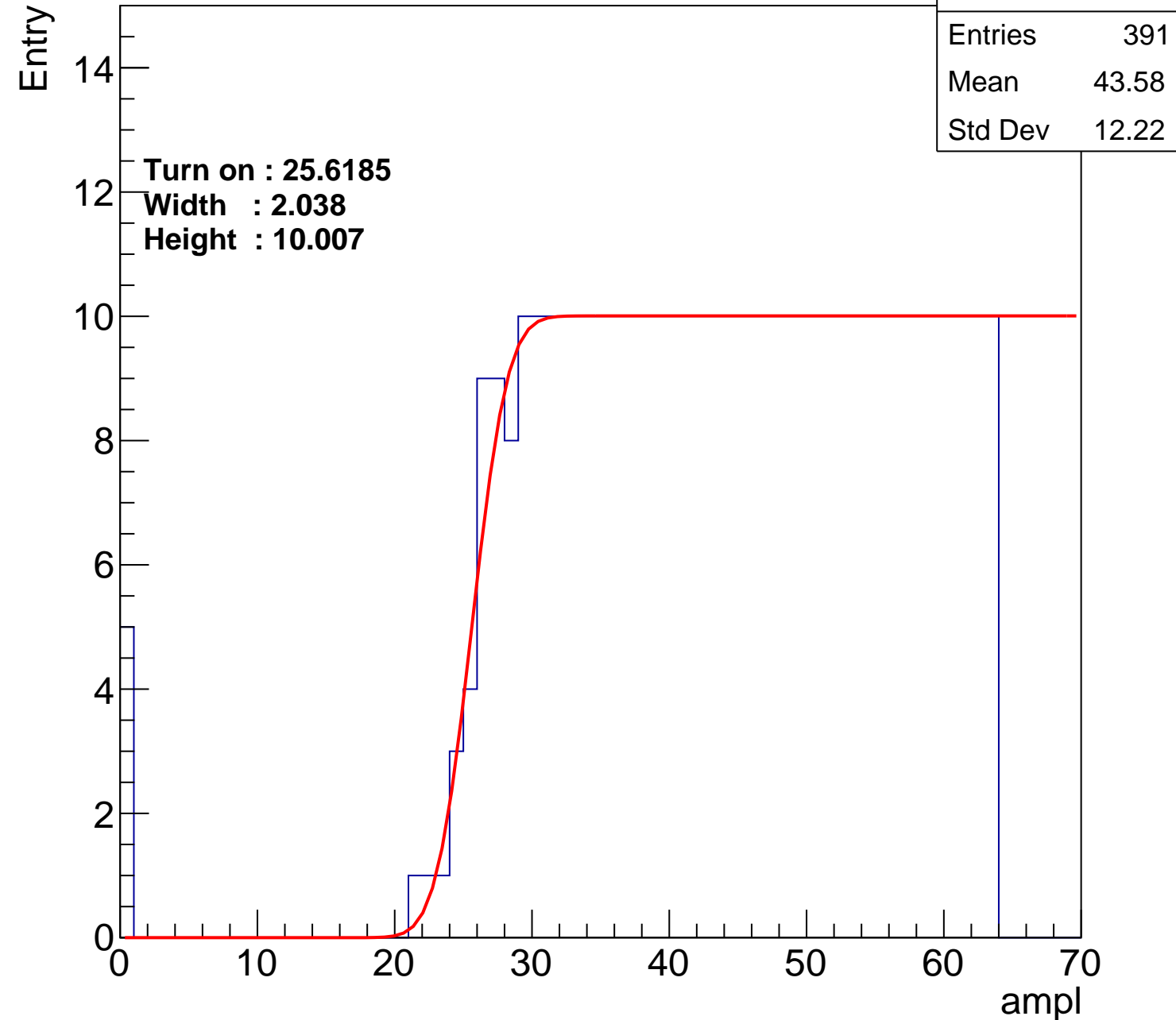
Width : 2.038

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch127

calib_packv5_042523_0143.root, FC#11, port A2

Entries	372
Mean	44.58
Std Dev	11.52

Turn on : 27.7947

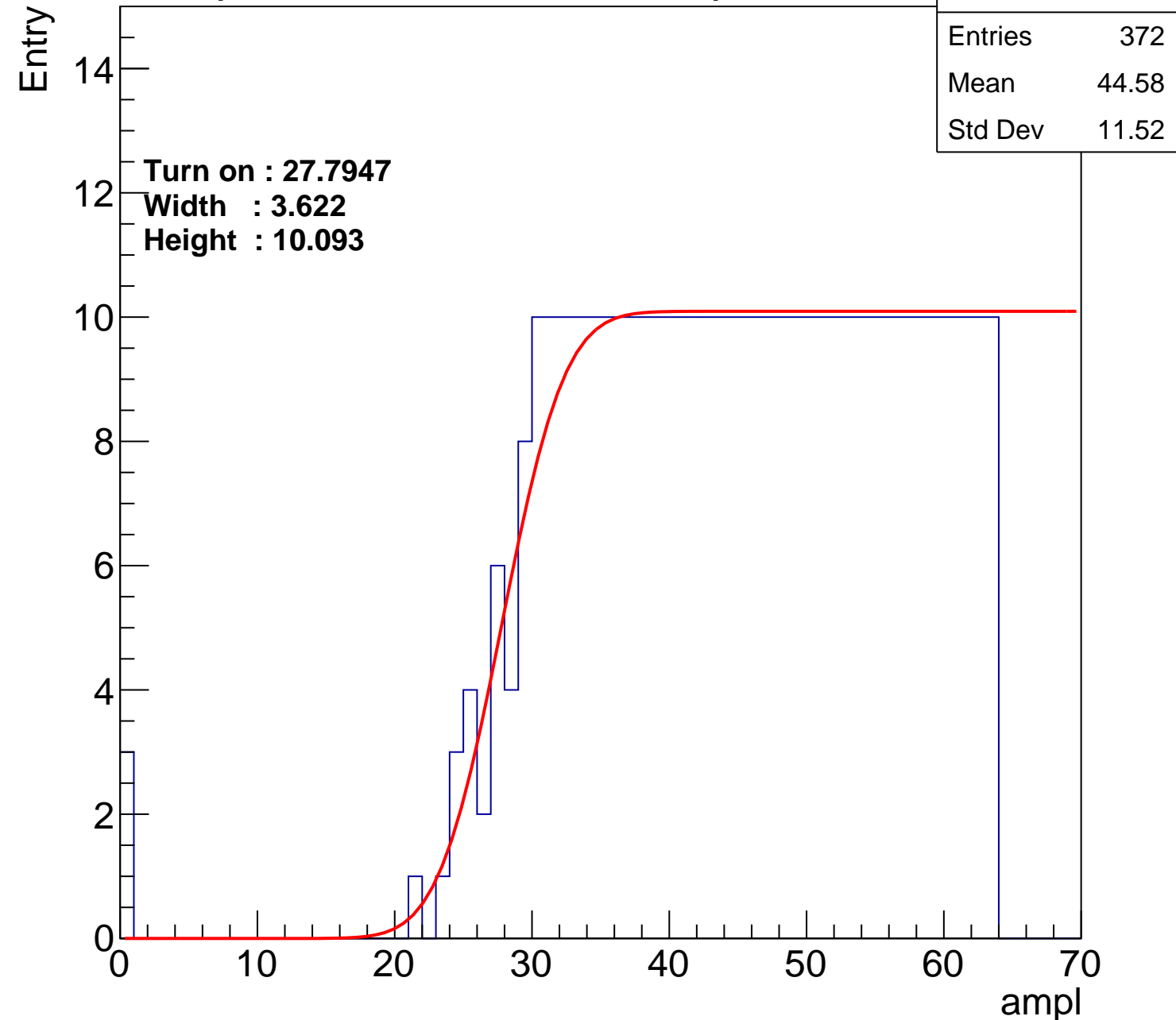
Width : 3.622

Height : 10.093

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U1-ch127

calib_packv5_042523_0143.root, FC#11, port A2

Entries	372
Mean	44.58
Std Dev	11.52

Turn on : 27.7947

Width : 3.622

Height : 10.093

Entry

14
12
10
8
6
4
2
0

ampl

