

B1L101S, U10-ch0

calib_packv5_042523_0143.root, FC#0, port D2

Entries	392
Mean	43.56
Std Dev	12.07

Turn on : 25.3185

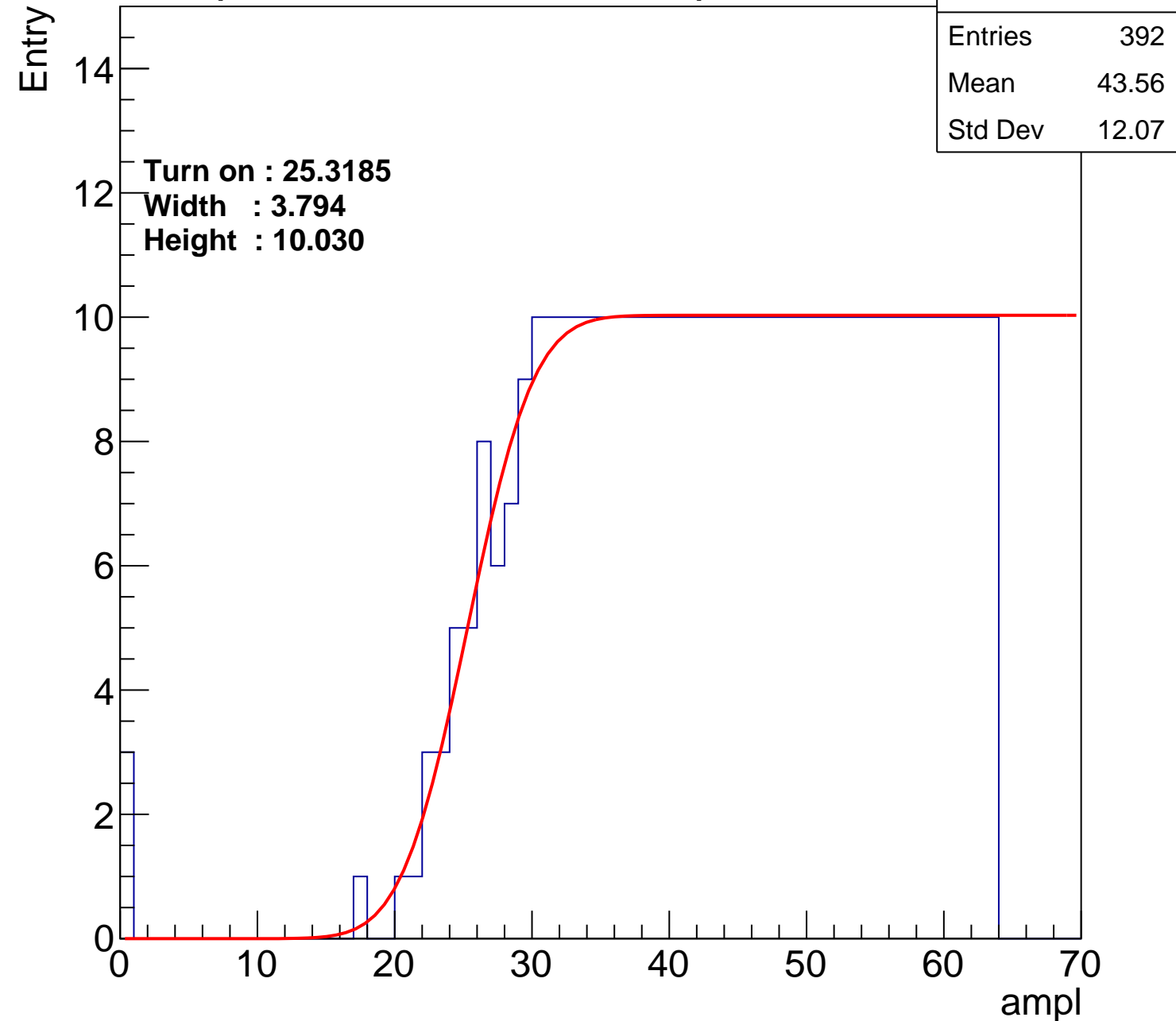
Width : 3.794

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch1

calib_packv5_042523_0143.root, FC#0, port D2

Entries	349
Mean	45.6
Std Dev	11.24

Turn on : 29.8672

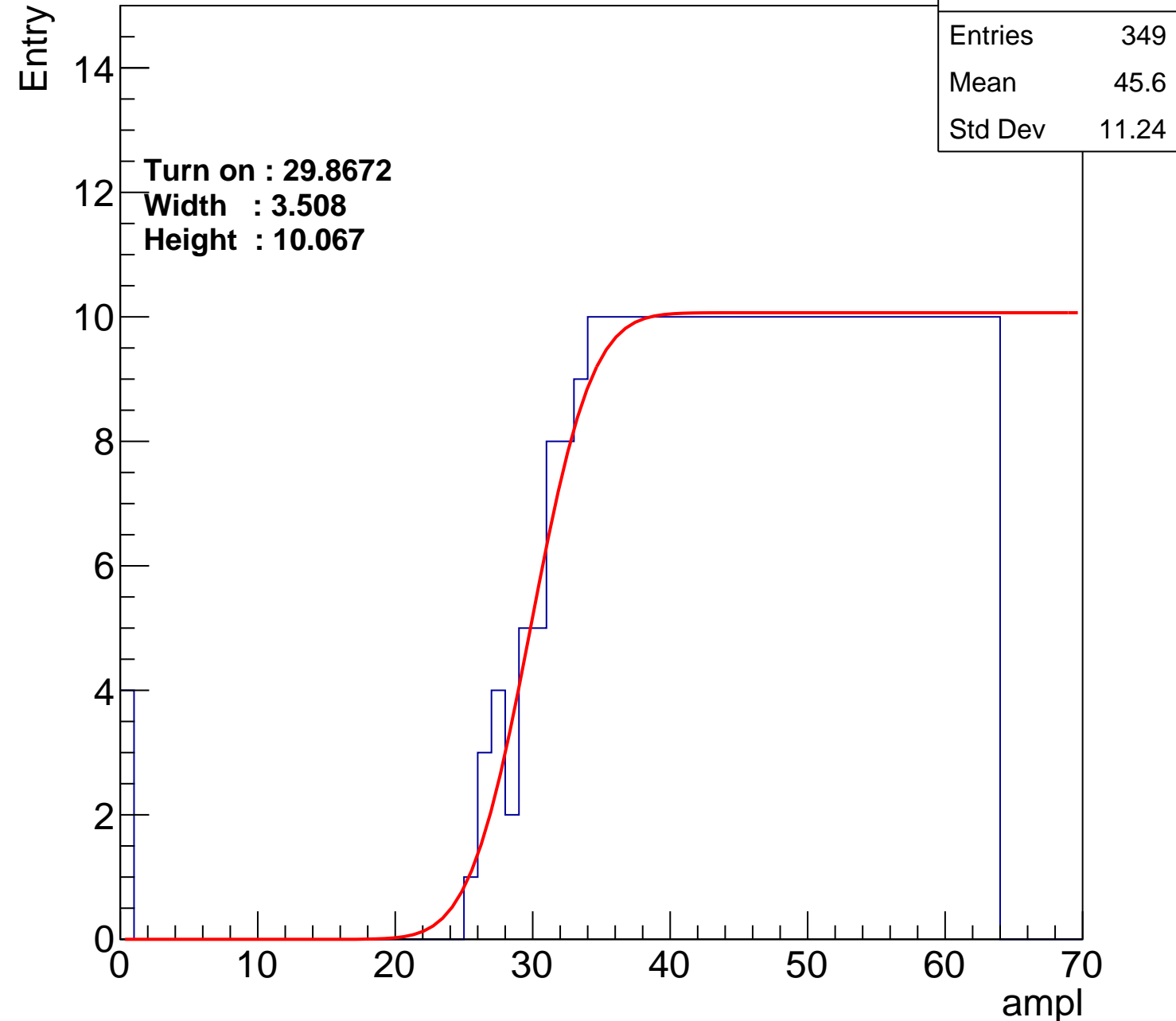
Width : 3.508

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch2

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.44
Std Dev	11.39

Turn on : 26.5714

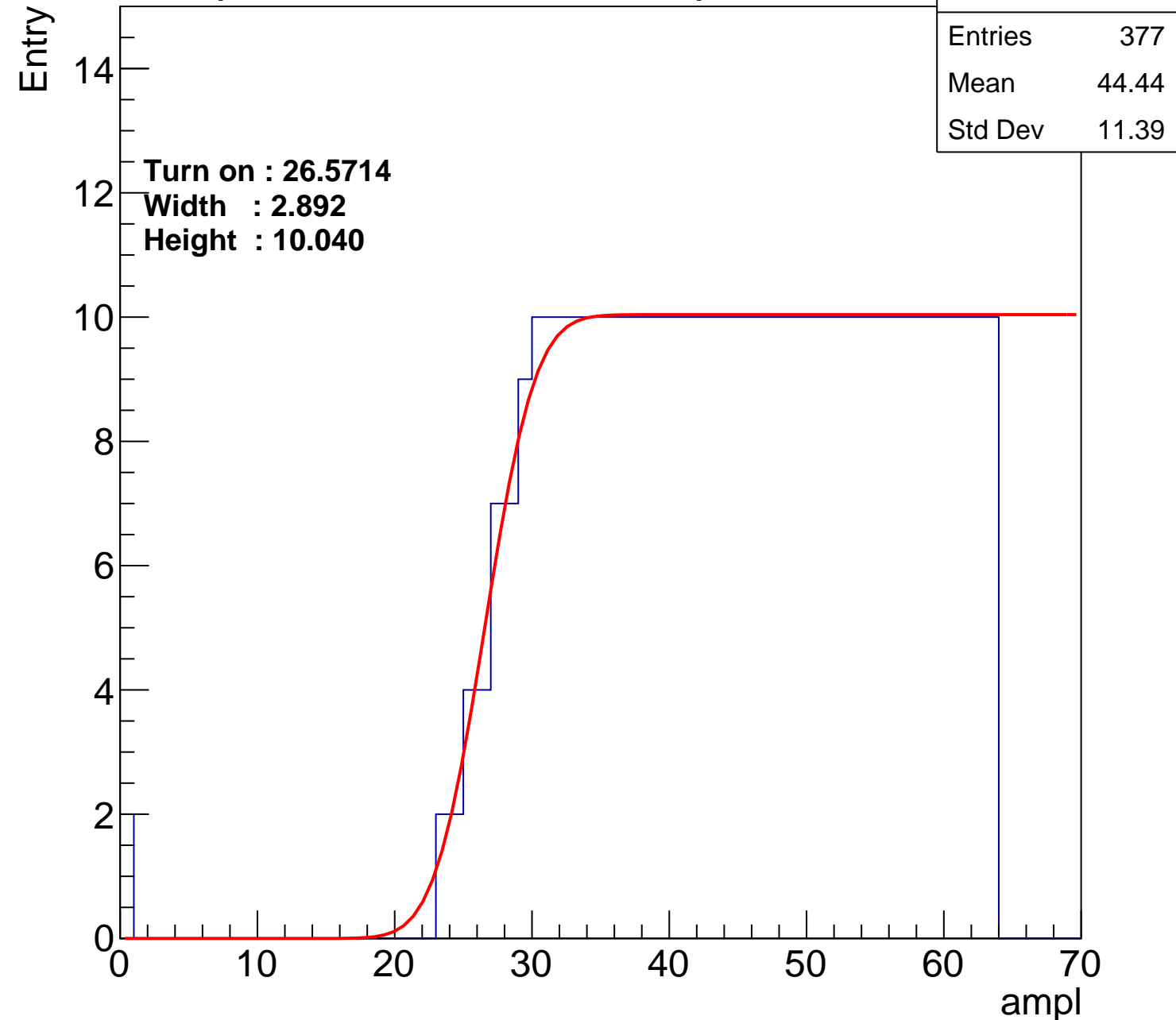
Width : 2.892

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch3

calib_packv5_042523_0143.root, FC#0, port D2

Entries	362
Mean	45.14
Std Dev	11.07

Turn on : 27.9257

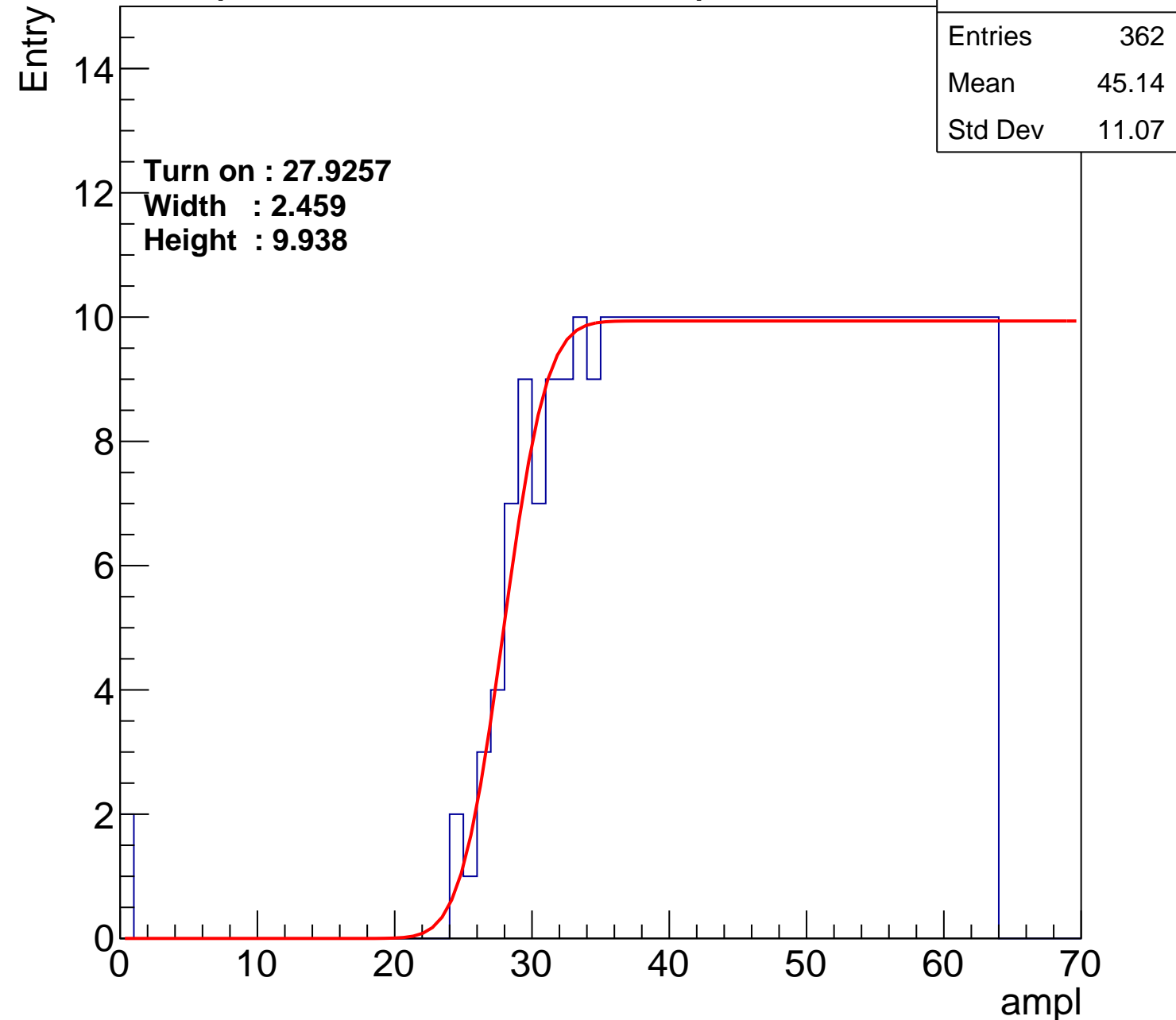
Width : 2.459

Height : 9.938

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch4

calib_packv5_042523_0143.root, FC#0, port D2

Entries	365
Mean	44.93
Std Dev	11.34

Turn on : 27.8825

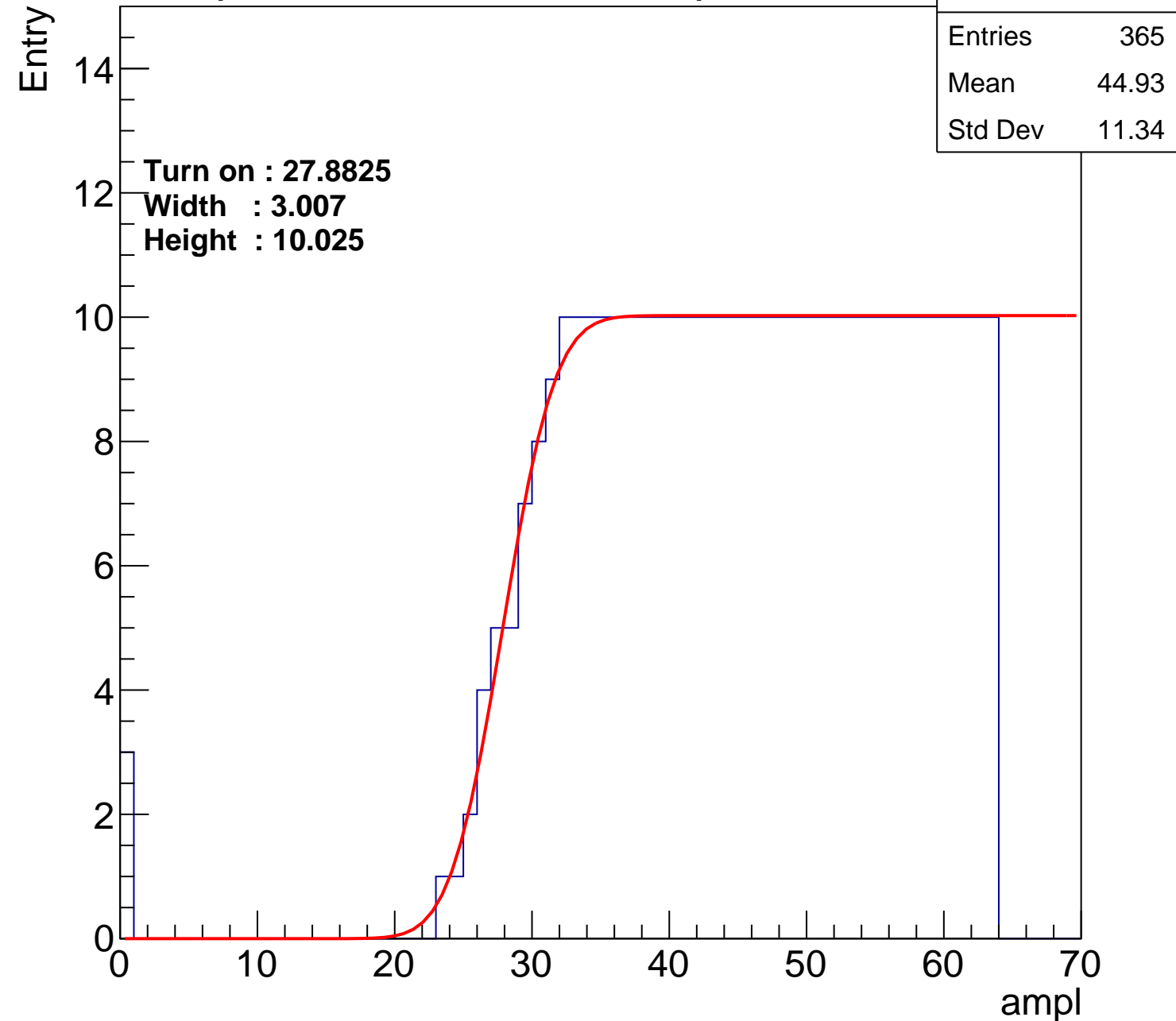
Width : 3.007

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch5

calib_packv5_042523_0143.root, FC#0, port D2

Entries	360
Mean	45.21
Std Dev	11.06

Turn on : 27.5616

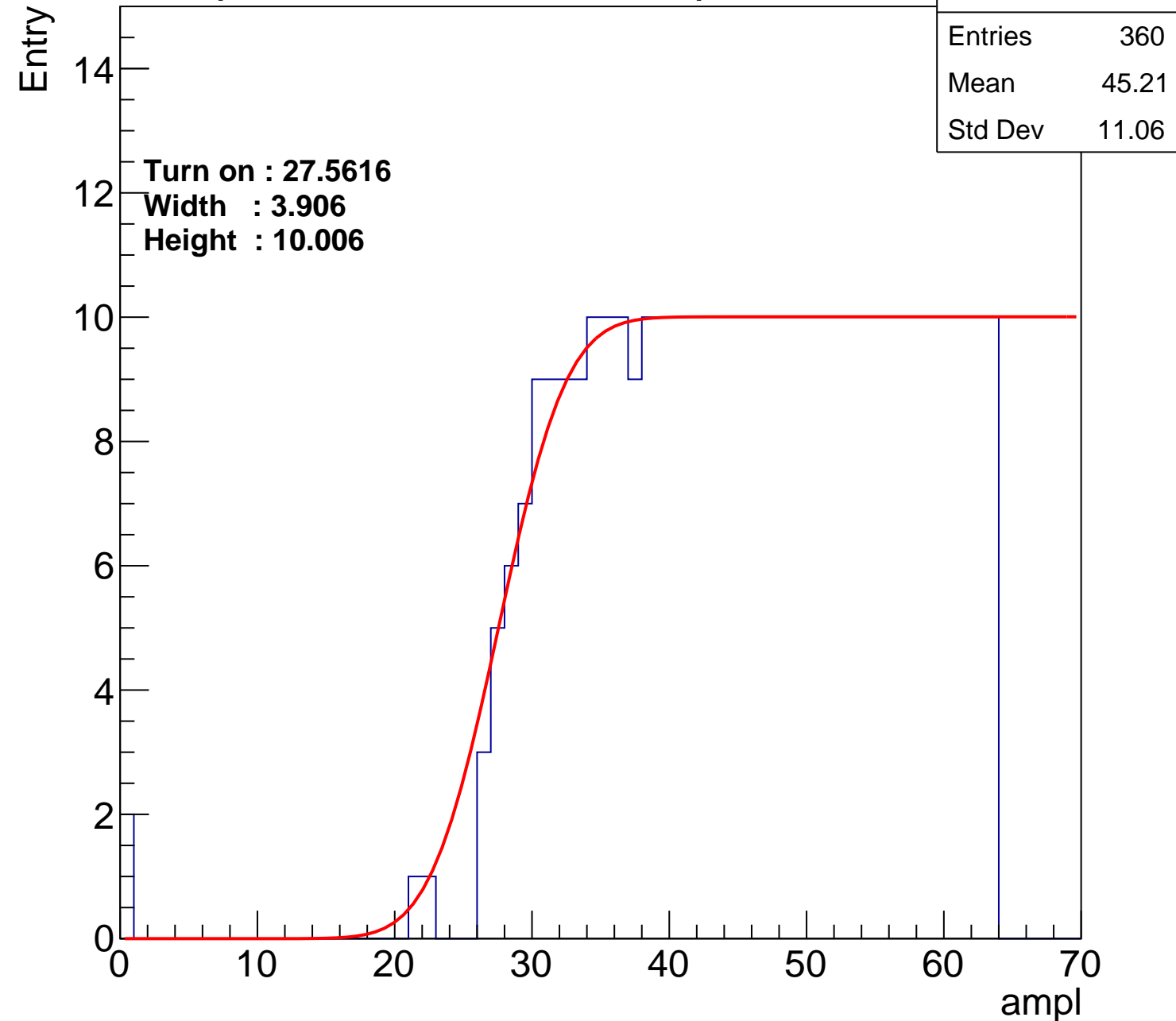
Width : 3.906

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch6

calib_packv5_042523_0143.root, FC#0, port D2

Entries	394
Mean	43.35
Std Dev	12.47

Turn on : 24.9800

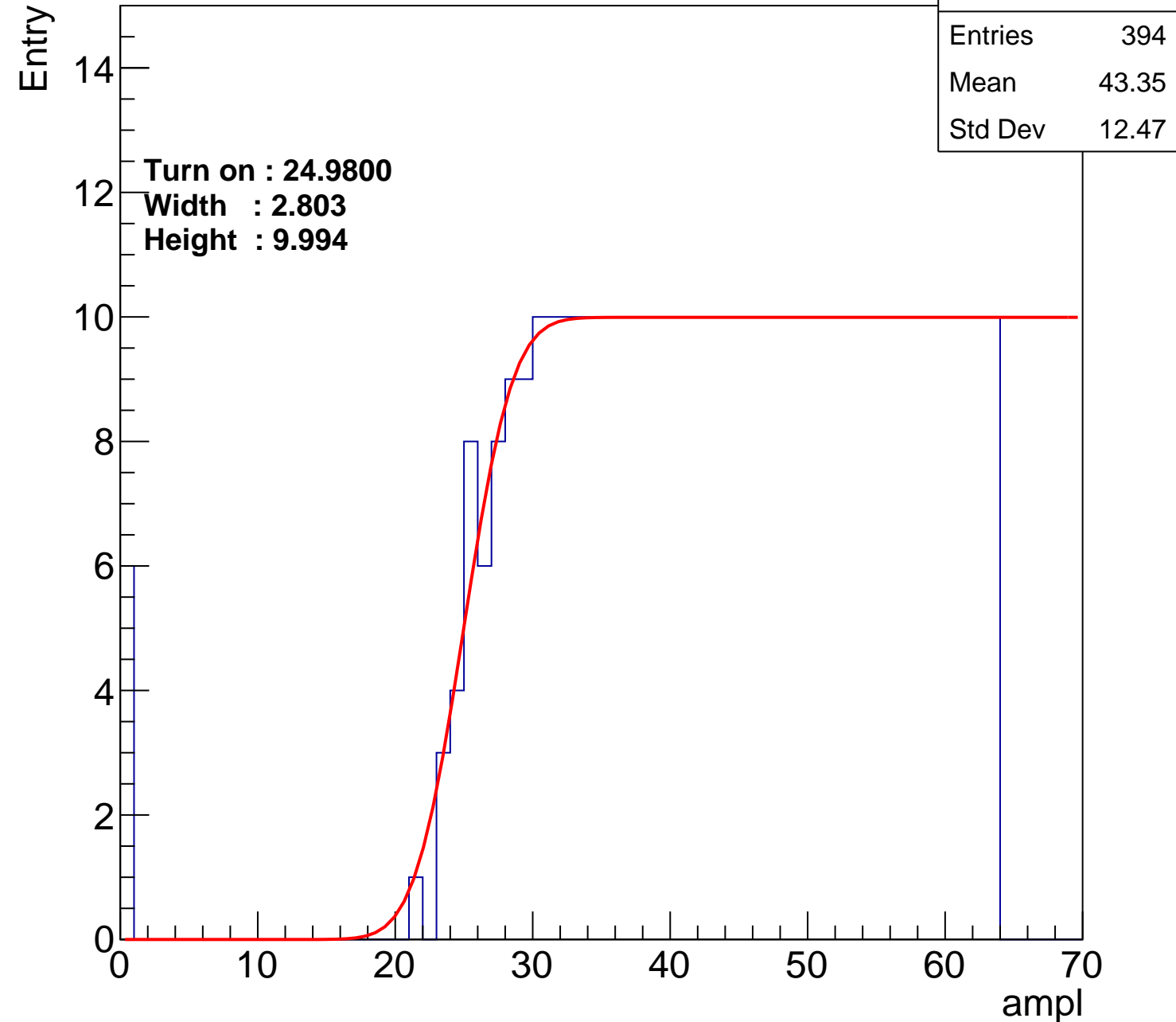
Width : 2.803

Height : 9.994

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch7

calib_packv5_042523_0143.root, FC#0, port D2

Entries	353
Mean	45.63
Std Dev	10.66

Turn on : 28.9311

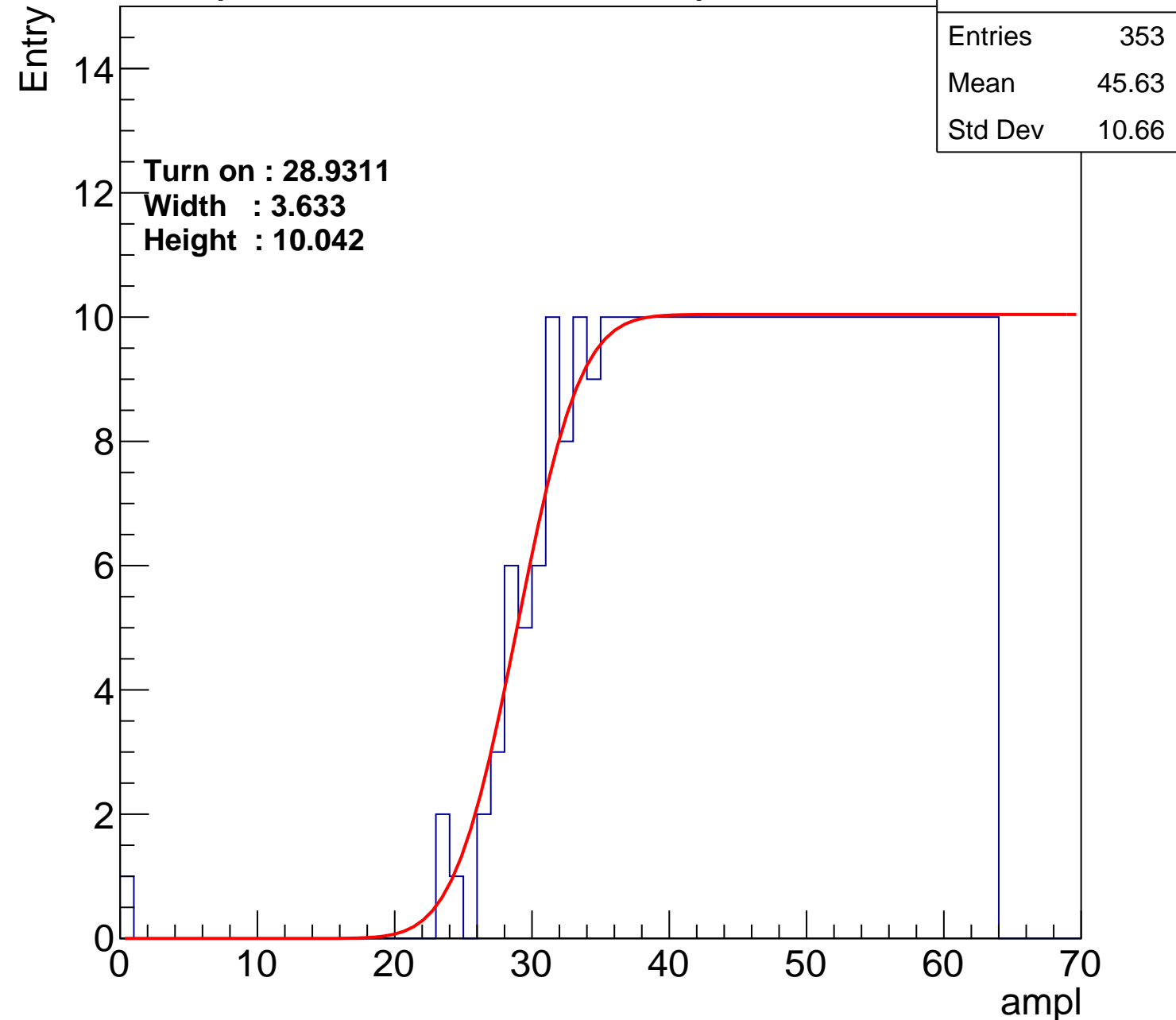
Width : 3.633

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch8

calib_packv5_042523_0143.root, FC#0, port D2

Entries	369
Mean	44.8
Std Dev	11.23

Turn on : 27.0596

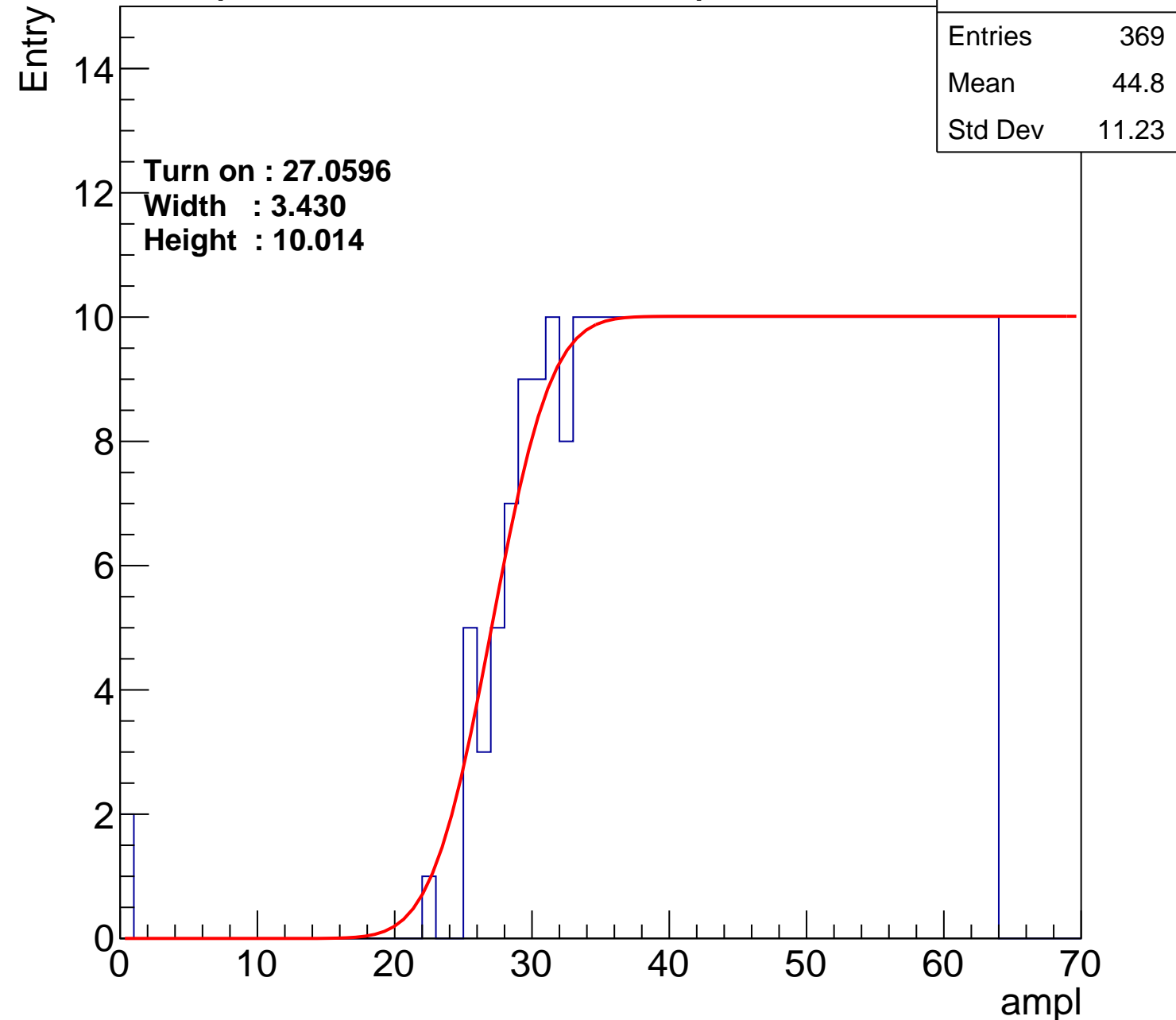
Width : 3.430

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch9

calib_packv5_042523_0143.root, FC#0, port D2

Entries	383
Mean	44.04
Std Dev	11.86

Turn on : 26.4058

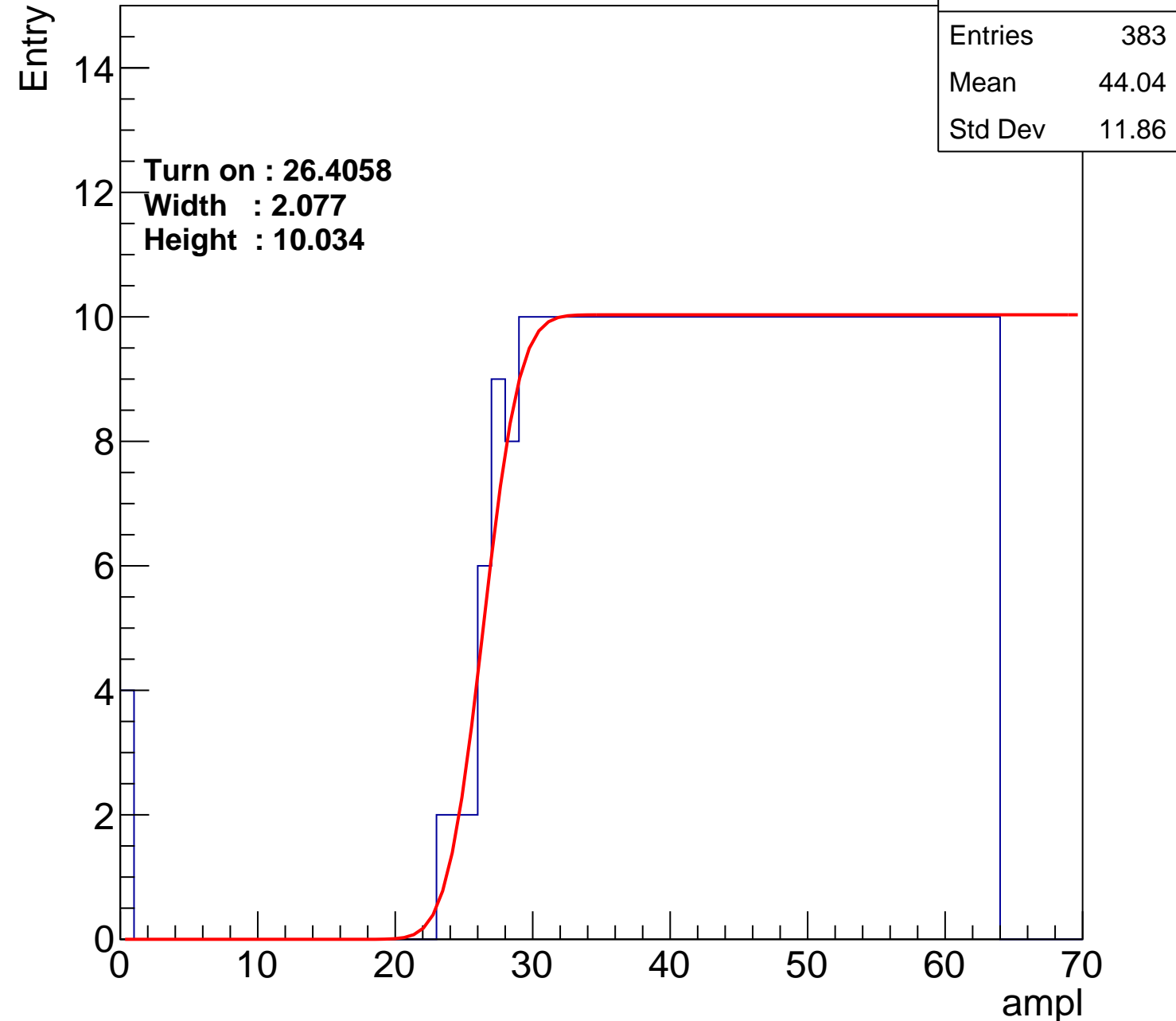
Width : 2.077

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch10

calib_packv5_042523_0143.root, FC#0, port D2

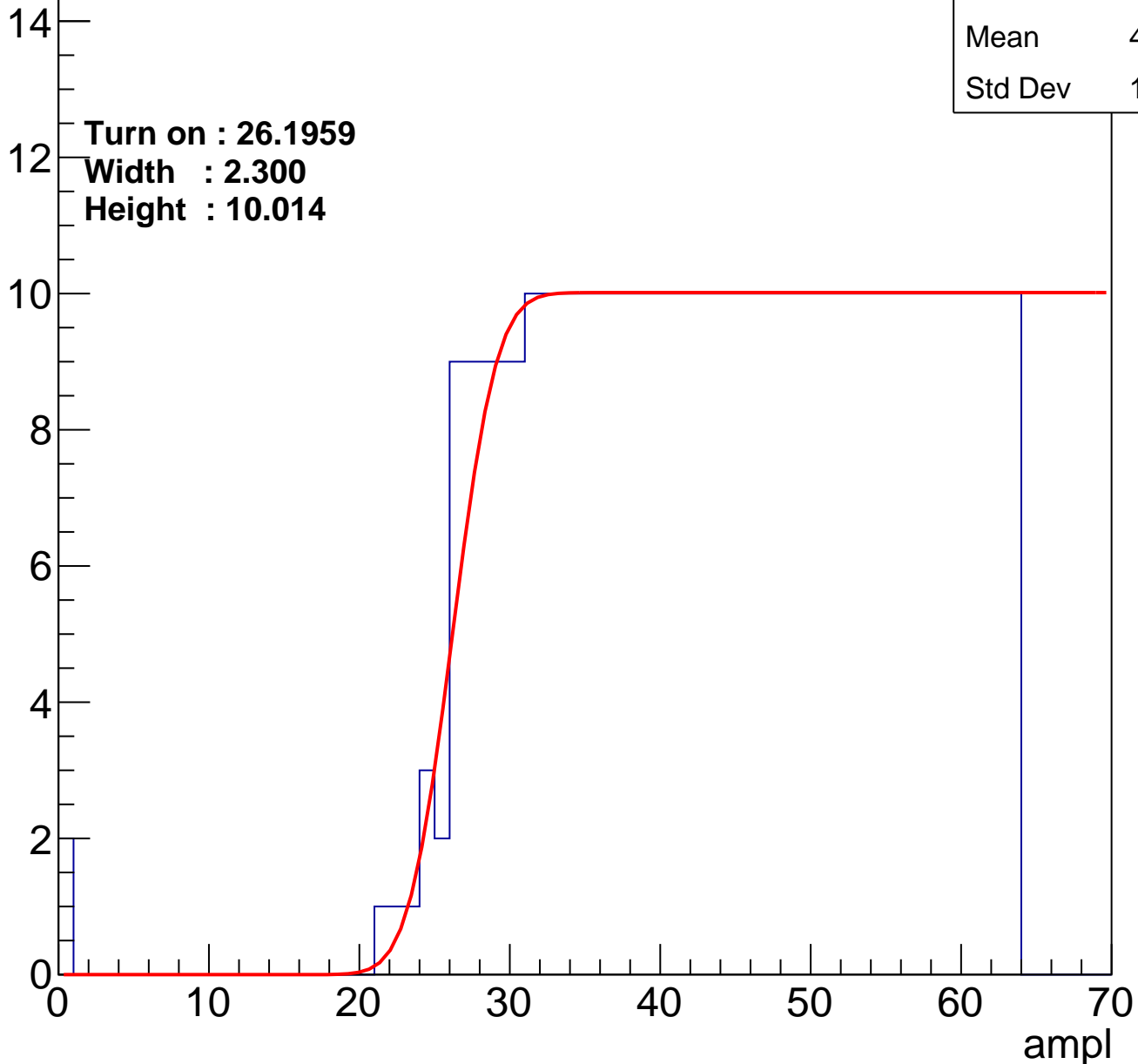
Entries	385
Mean	44.05
Std Dev	11.59

Turn on : 26.1959

Width : 2.300

Height : 10.014

Entry



B1L101S, U10-ch11

calib_packv5_042523_0143.root, FC#0, port D2

Entries	392
Mean	43.68
Std Dev	11.82

Turn on : 25.5827

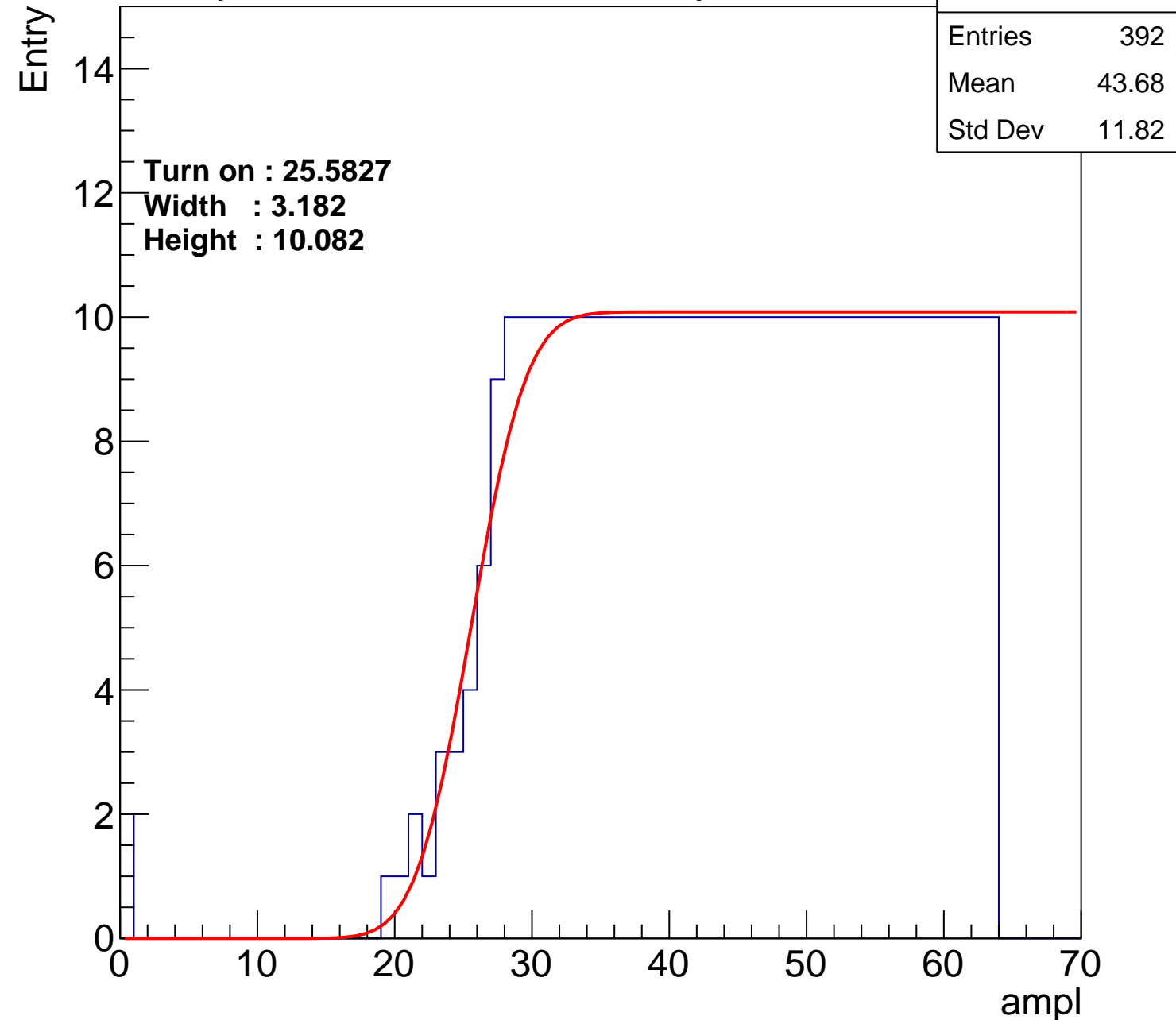
Width : 3.182

Height : 10.082

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch12

calib_packv5_042523_0143.root, FC#0, port D2

Entries	378
Mean	44.32
Std Dev	11.53

Turn on : 27.1510

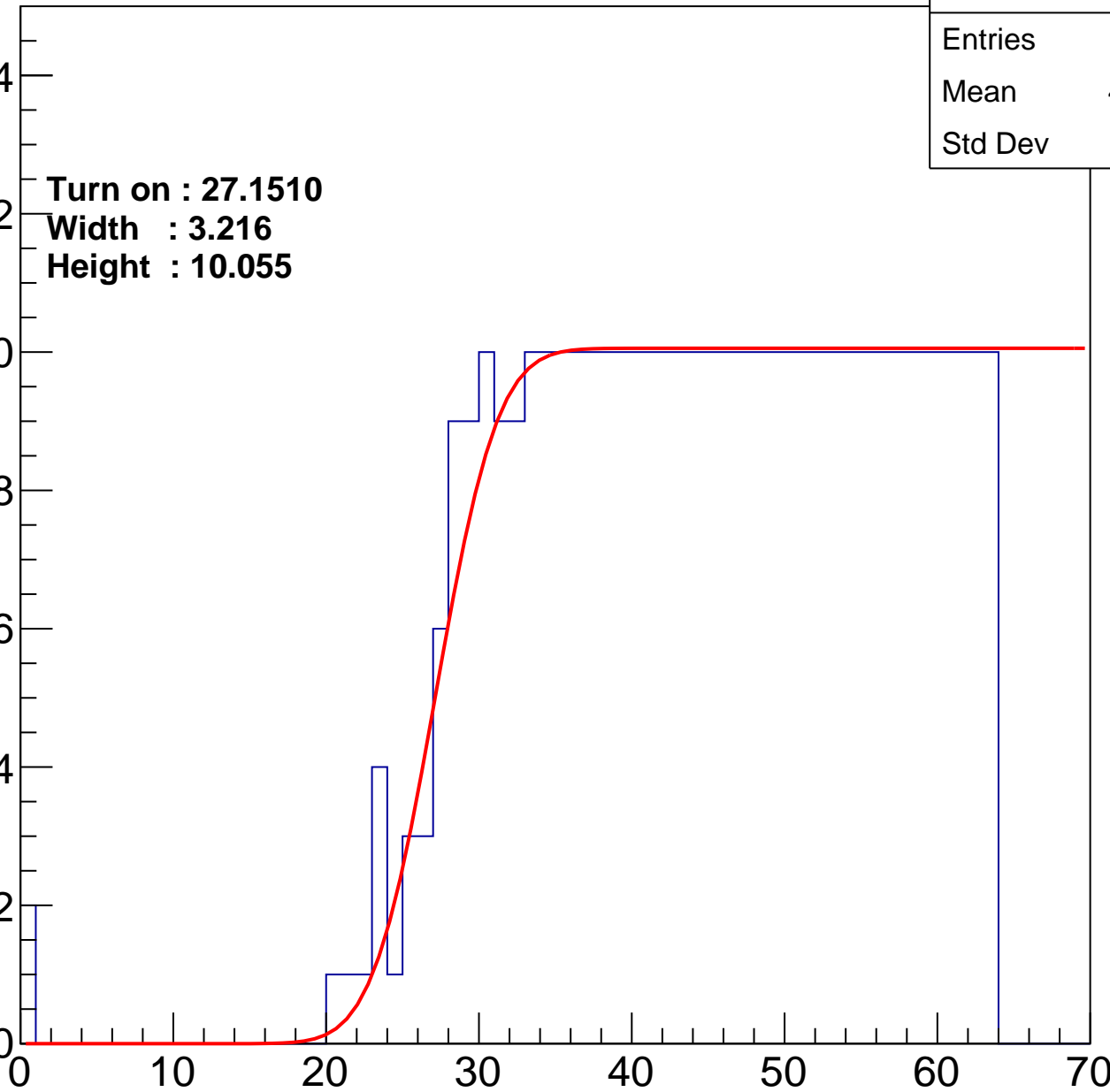
Width : 3.216

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch13

calib_packv5_042523_0143.root, FC#0, port D2

Entries	353
Mean	45.37
Std Dev	11.37

Turn on : 29.3698

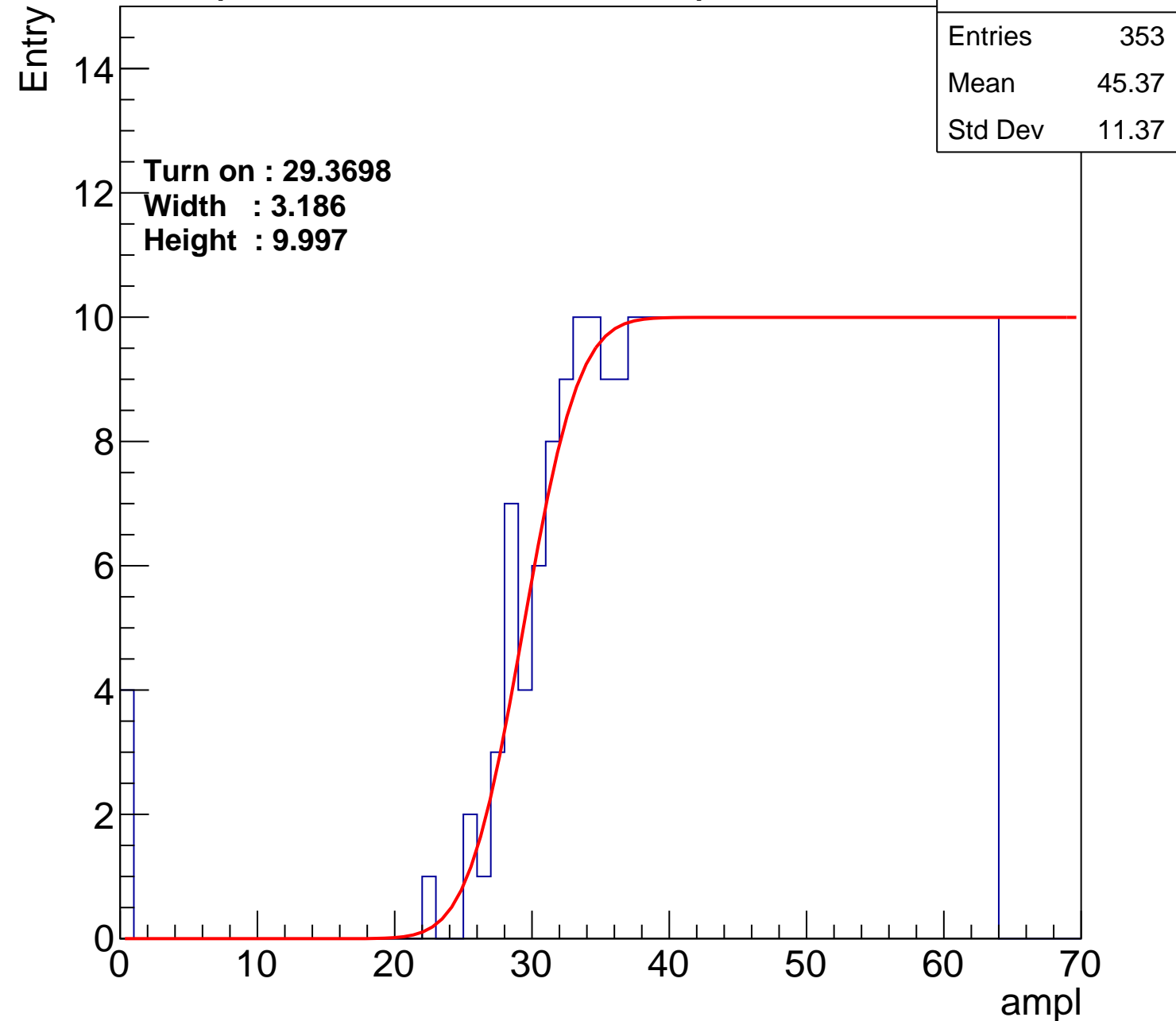
Width : 3.186

Height : 9.997

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch14

calib_packv5_042523_0143.root, FC#0, port D2

Entries	363
Mean	45.01
Std Dev	11.31

Turn on : 27.8292

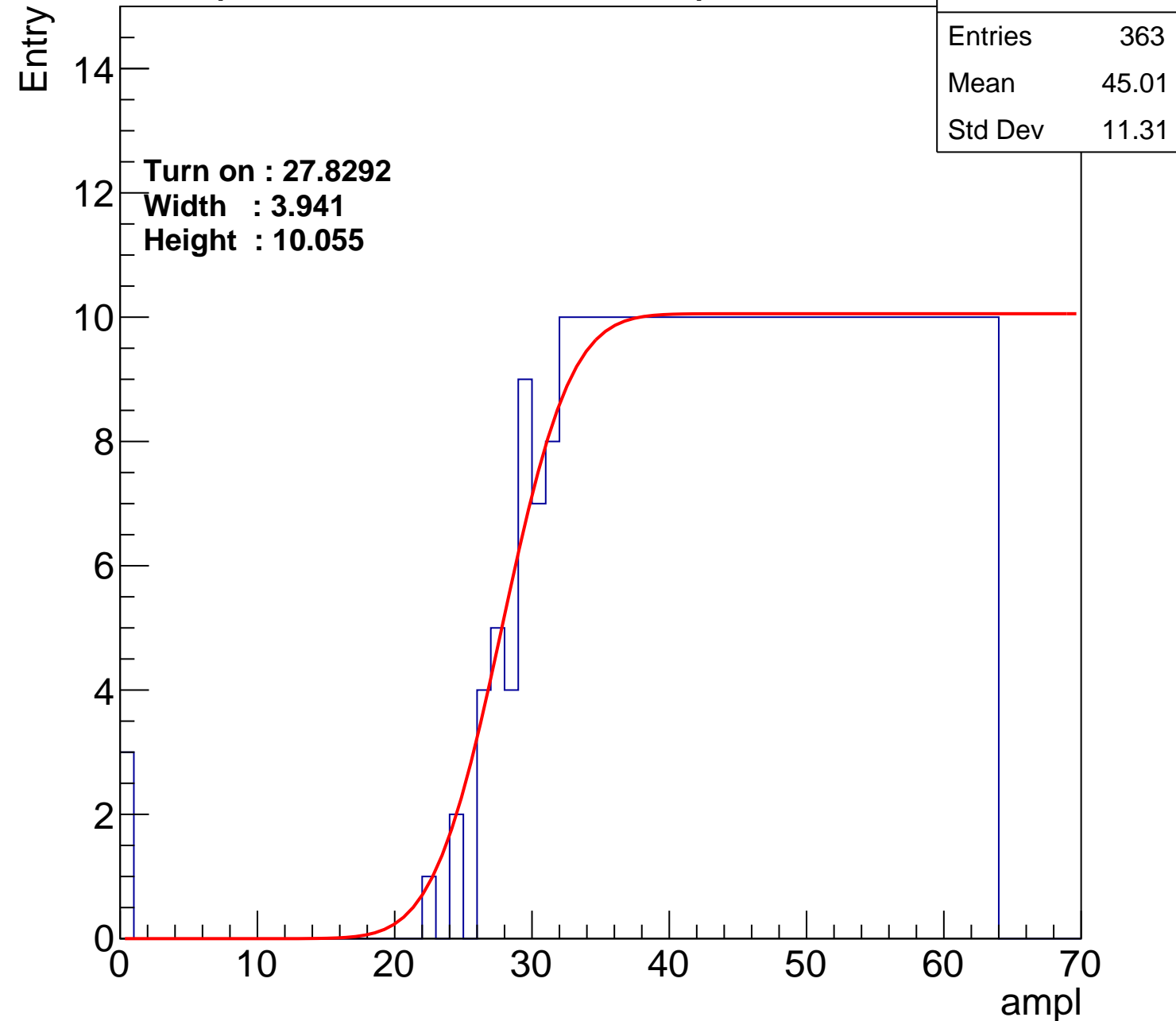
Width : 3.941

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch15

calib_packv5_042523_0143.root, FC#0, port D2

Entries	365
Mean	45.12
Std Dev	10.85

Turn on : 27.5425

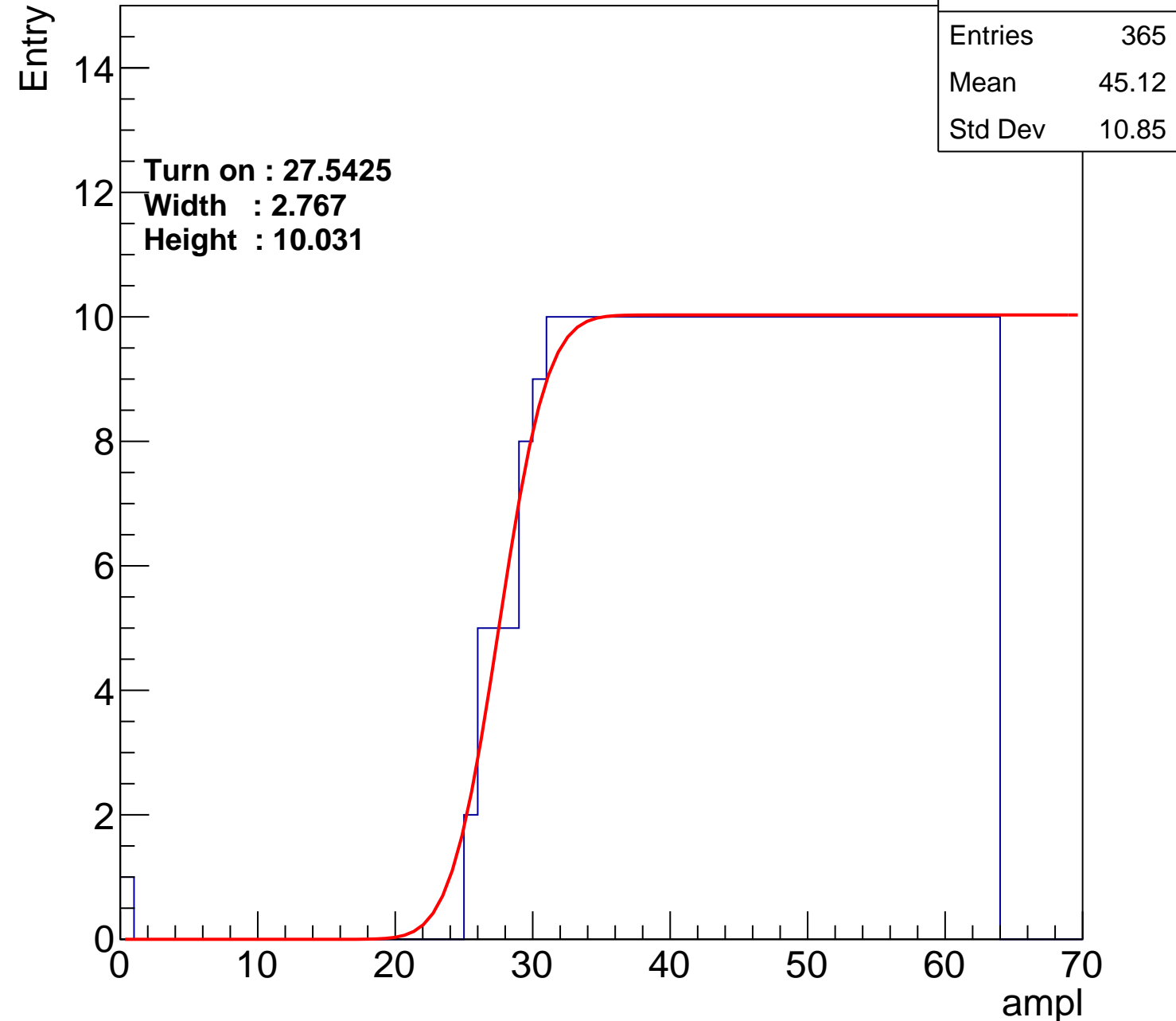
Width : 2.767

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch16

calib_packv5_042523_0143.root, FC#0, port D2

Entries	390
Mean	43.65
Std Dev	12.1

Turn on : 25.9107

Width : 3.161

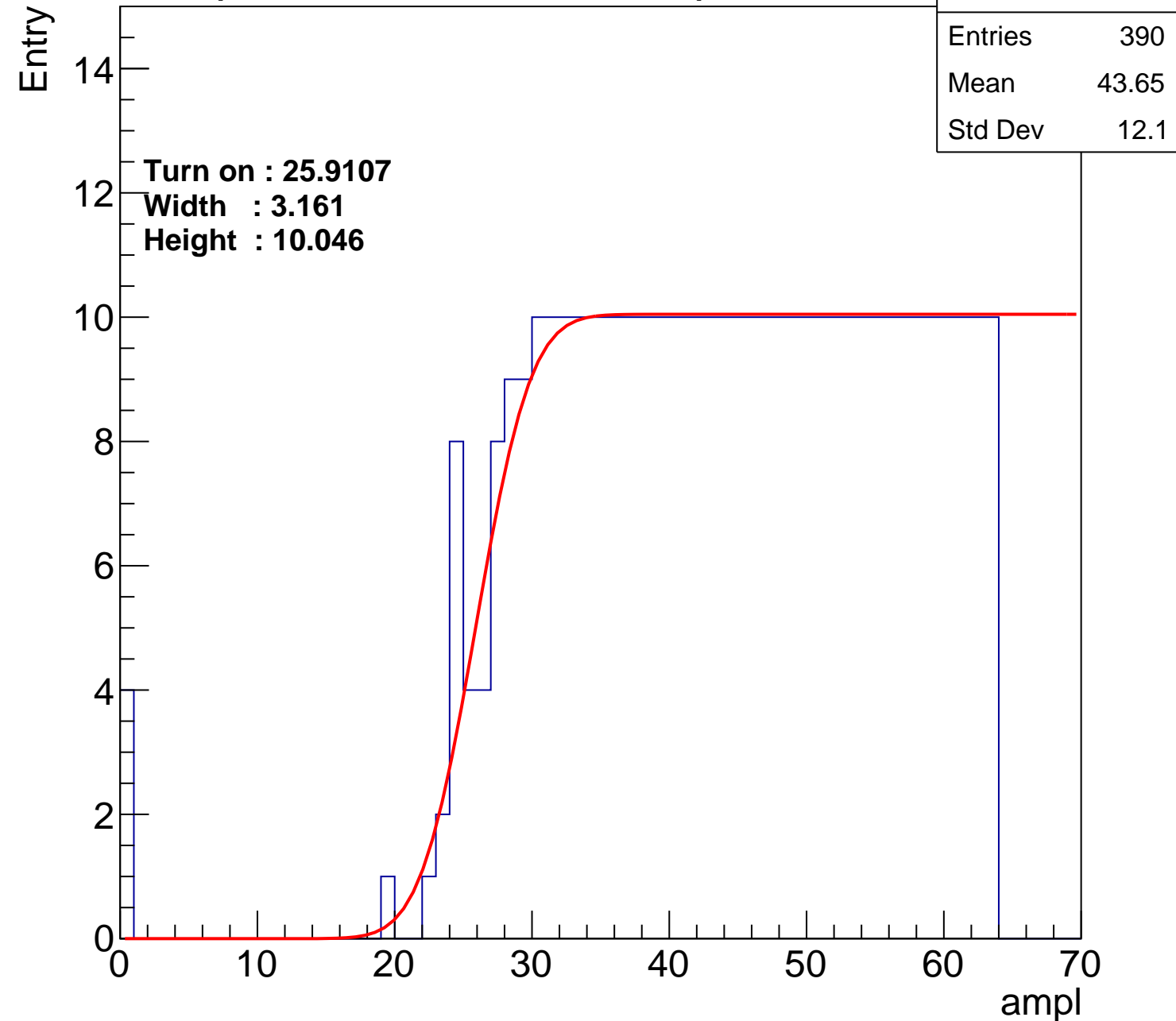
Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L101S, U10-ch17

calib_packv5_042523_0143.root, FC#0, port D2

Entries	380
Mean	44.3
Std Dev	11.46

Turn on : 26.4724

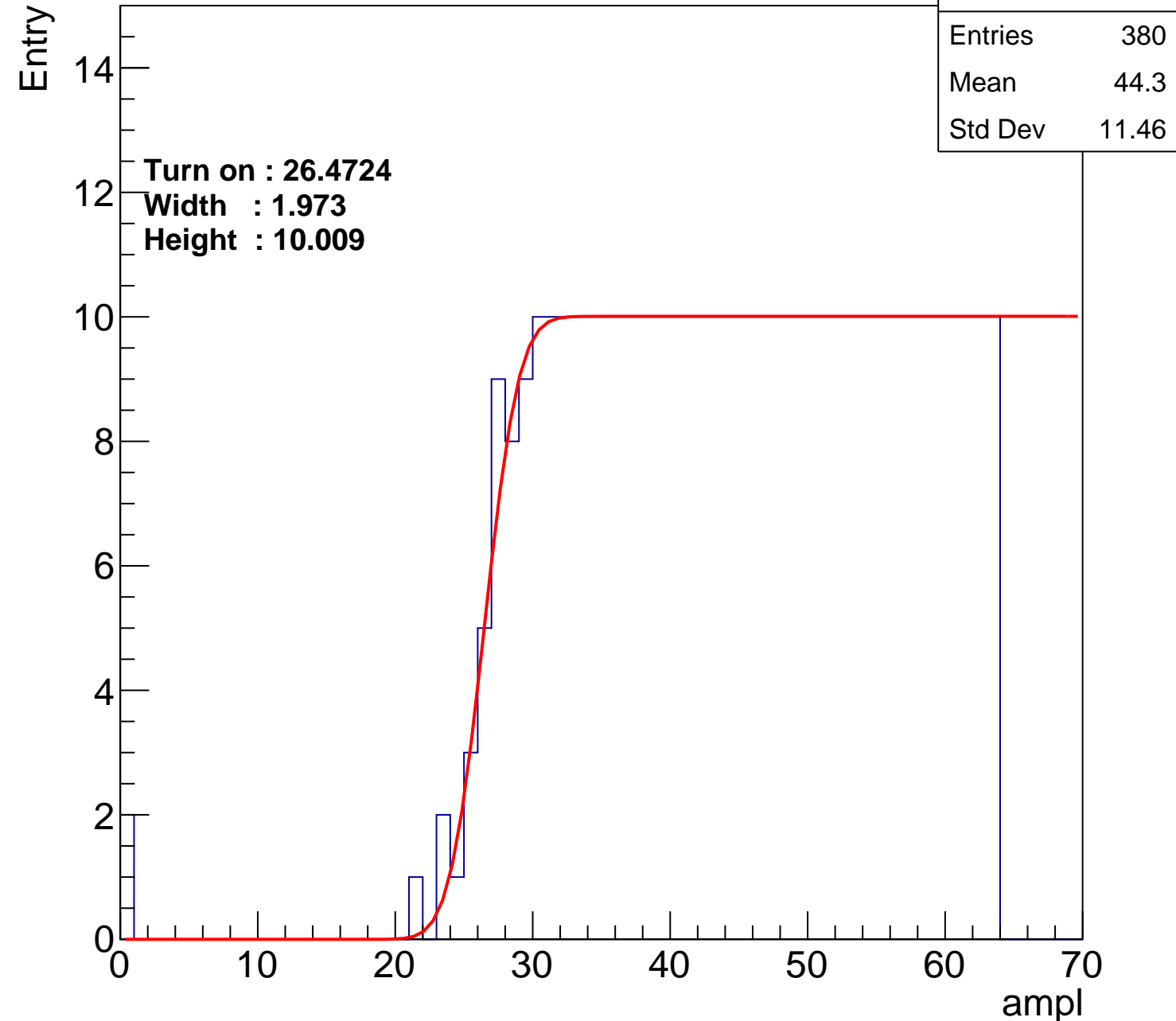
Width : 1.973

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch18

calib_packv5_042523_0143.root, FC#0, port D2

Entries	395
Mean	43.36
Std Dev	12.34

Turn on : 25.0891

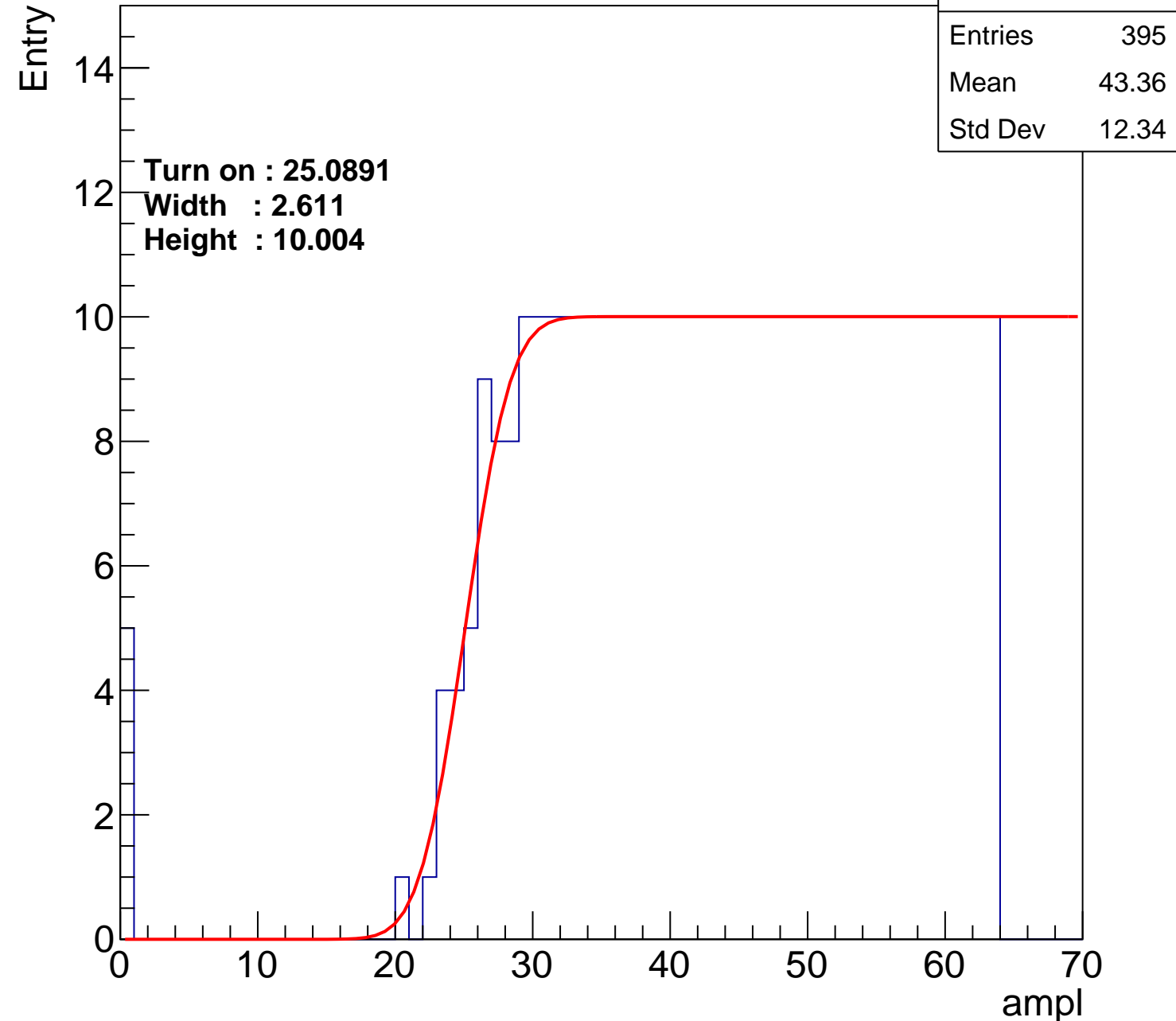
Width : 2.611

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch19

calib_packv5_042523_0143.root, FC#0, port D2

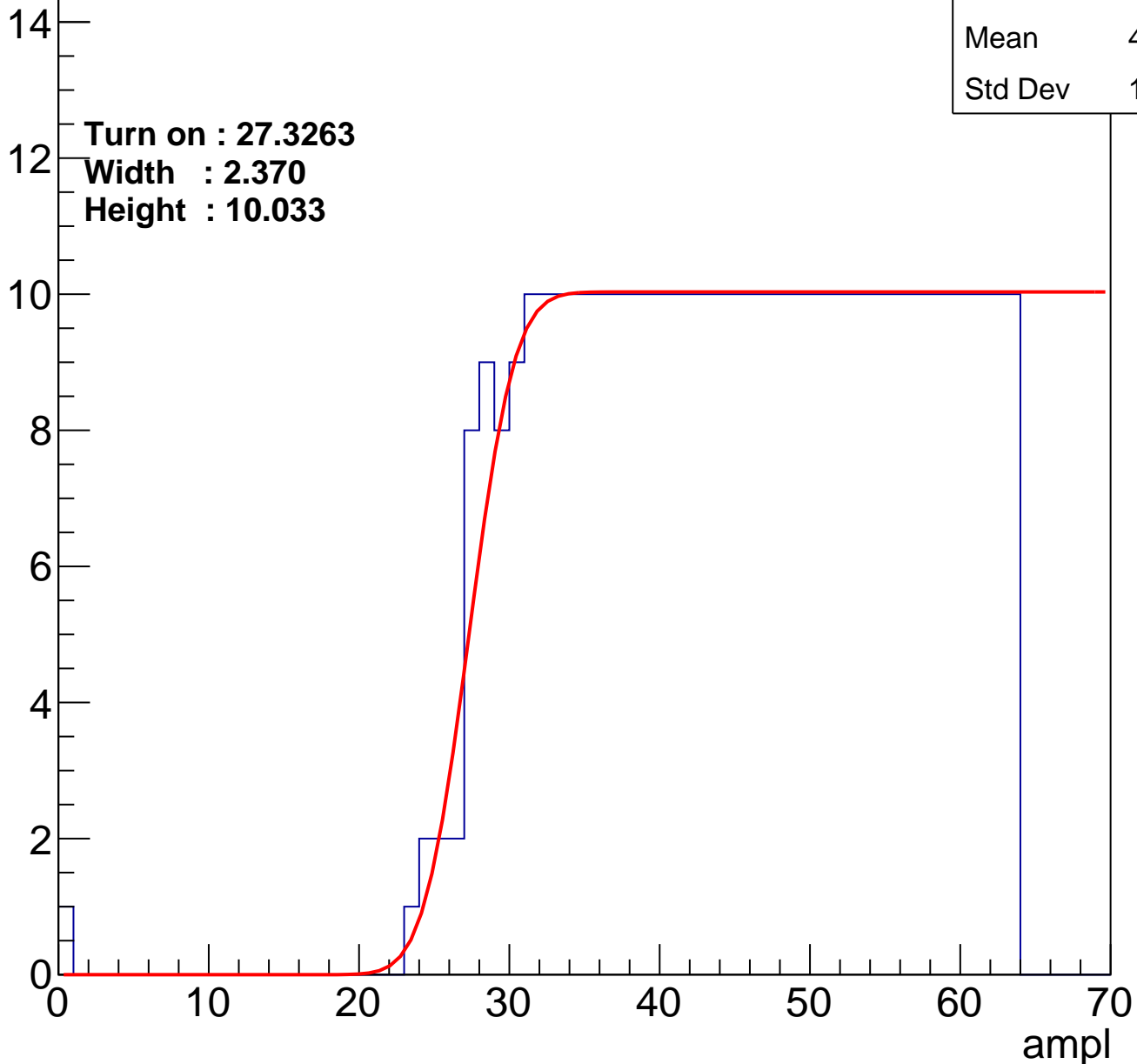
Entries	372
Mean	44.77
Std Dev	11.05

Turn on : 27.3263

Width : 2.370

Height : 10.033

Entry



B1L101S, U10-ch20

calib_packv5_042523_0143.root, FC#0, port D2

Entries	359
Mean	45.22
Std Dev	11.2

Turn on : 28.4730

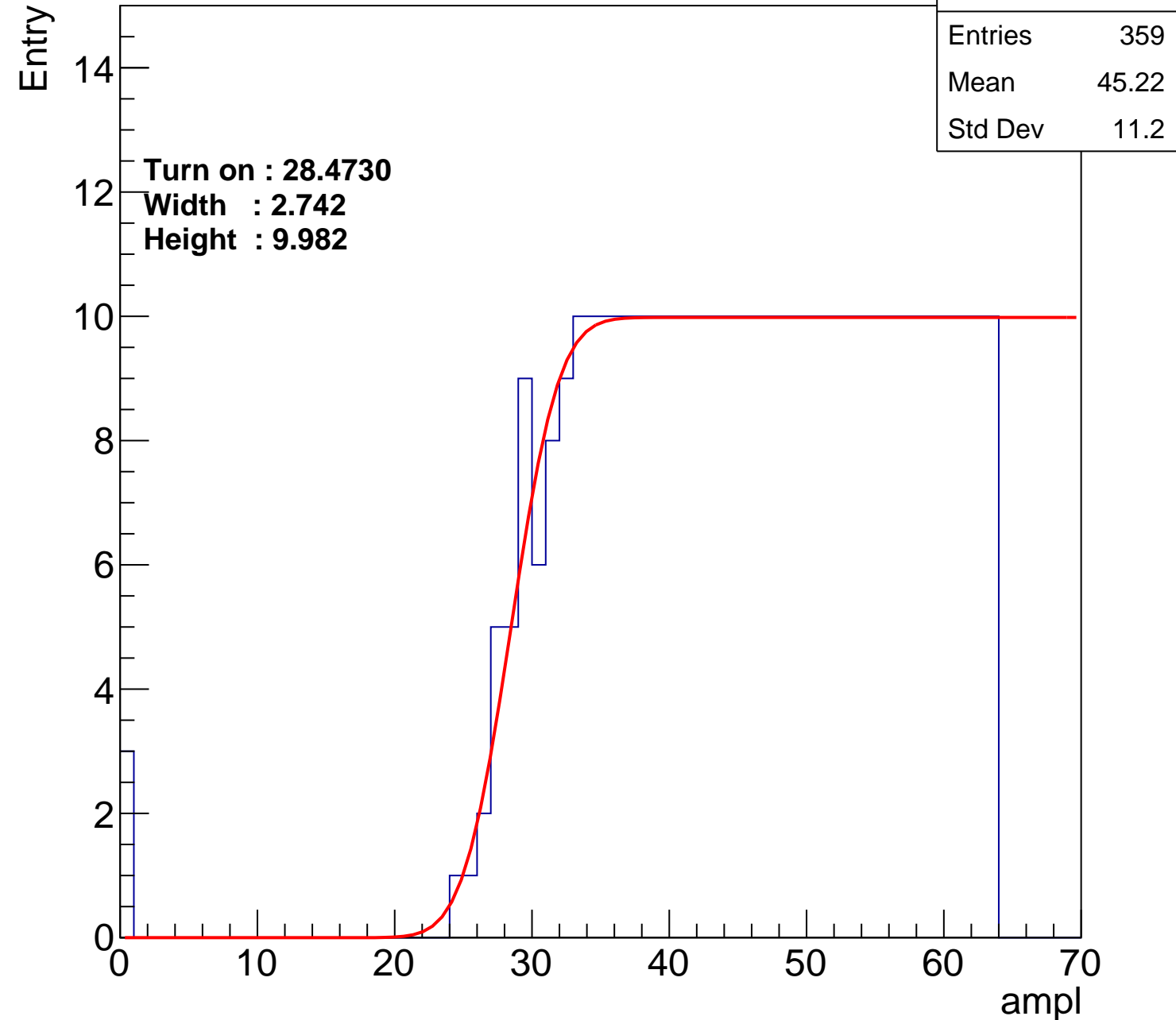
Width : 2.742

Height : 9.982

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch21

calib_packv5_042523_0143.root, FC#0, port D2

Entries	359
Mean	45.29
Std Dev	10.99

Turn on : 28.1168

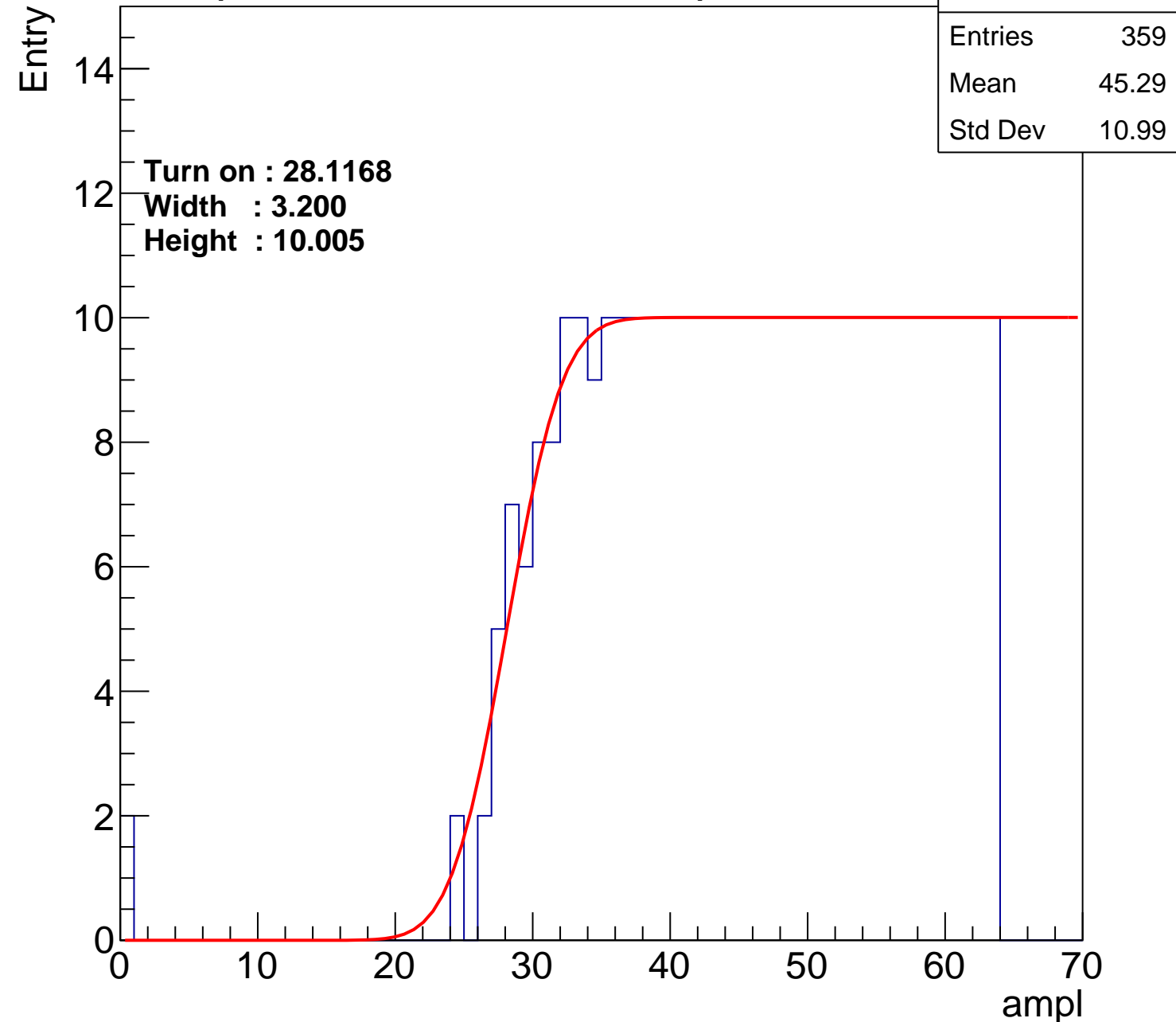
Width : 3.200

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch22

calib_packv5_042523_0143.root, FC#0, port D2

Entries	379
Mean	44.14
Std Dev	11.92

Turn on : 27.0534

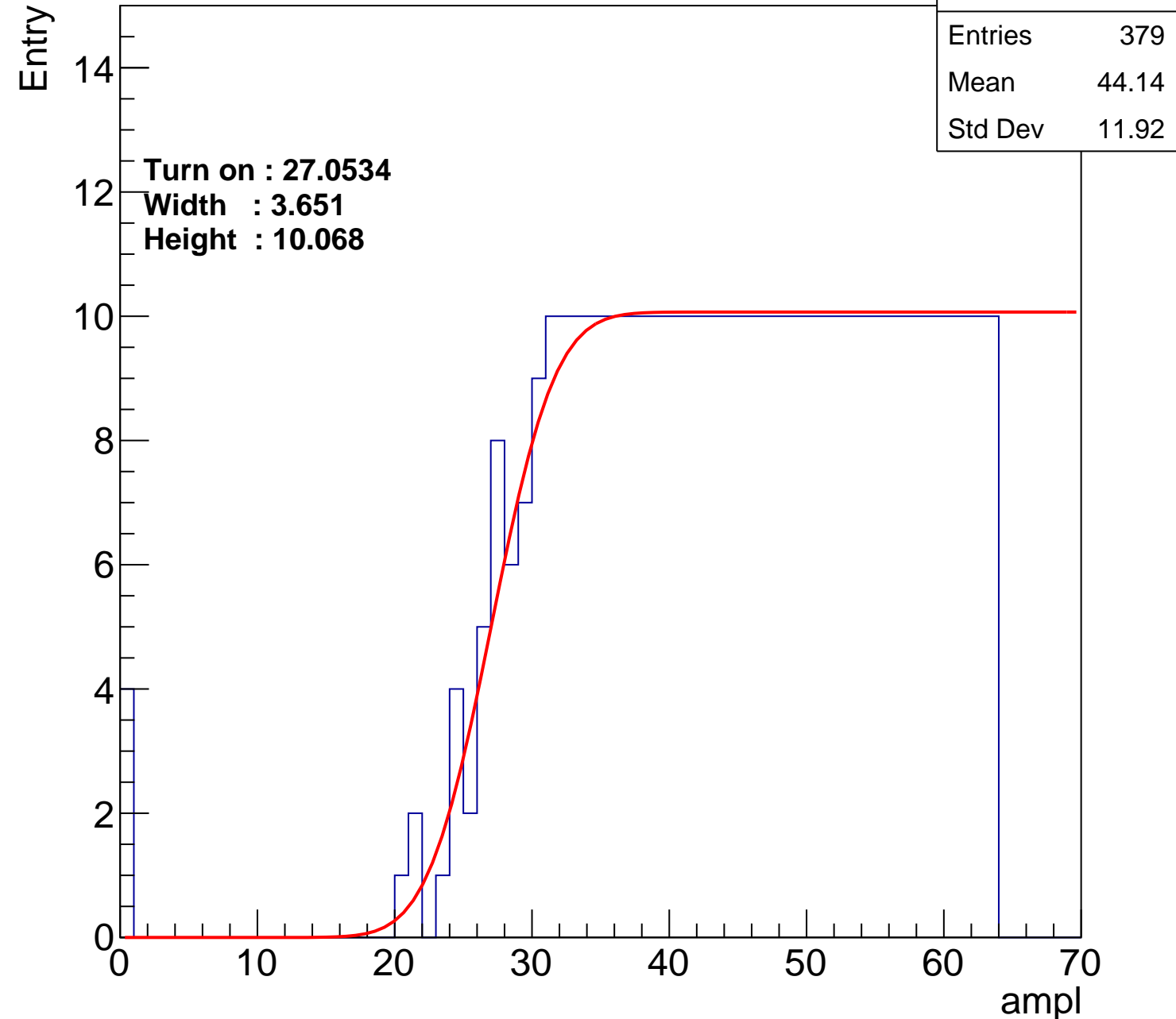
Width : 3.651

Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch23

calib_packv5_042523_0143.root, FC#0, port D2

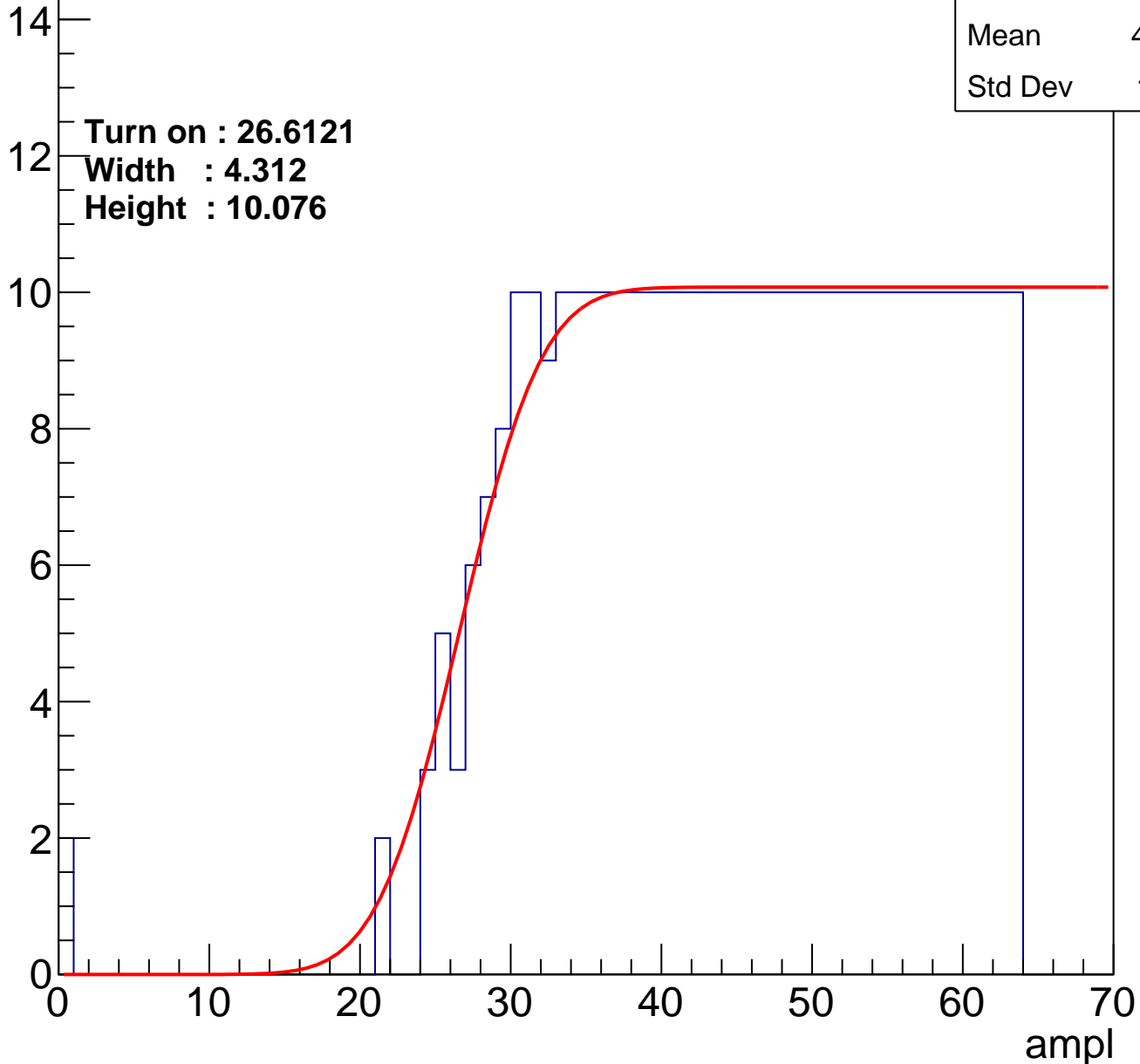
Entries	375
Mean	44.49
Std Dev	11.41

Turn on : 26.6121

Width : 4.312

Height : 10.076

Entry



B1L101S, U10-ch24

calib_packv5_042523_0143.root, FC#0, port D2

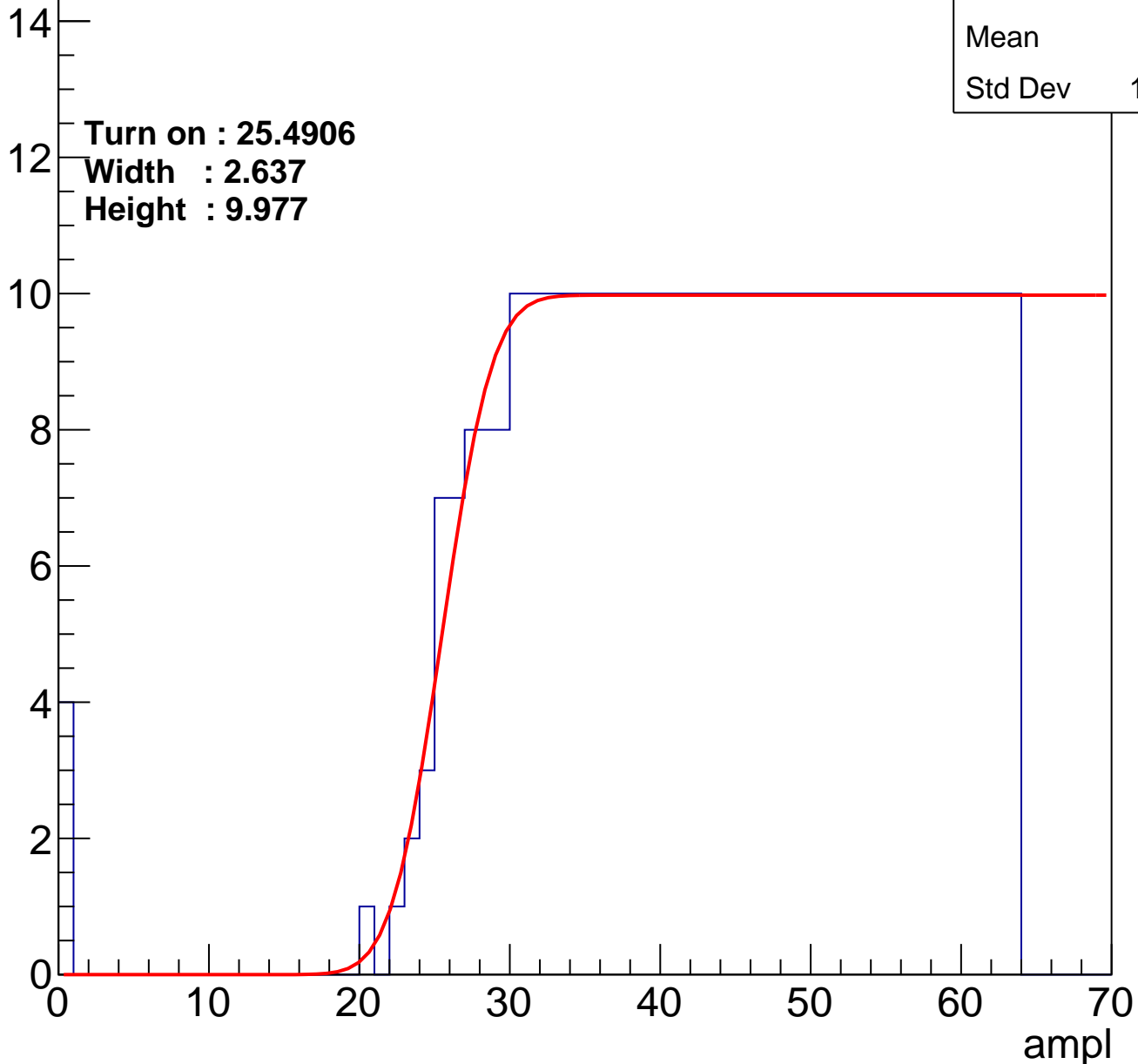
Entries	389
Mean	43.7
Std Dev	12.07

Turn on : 25.4906

Width : 2.637

Height : 9.977

Entry



B1L101S, U10-ch25

calib_packv5_042523_0143.root, FC#0, port D2

Entries	367
Mean	44.99
Std Dev	10.95

Turn on : 28.0916

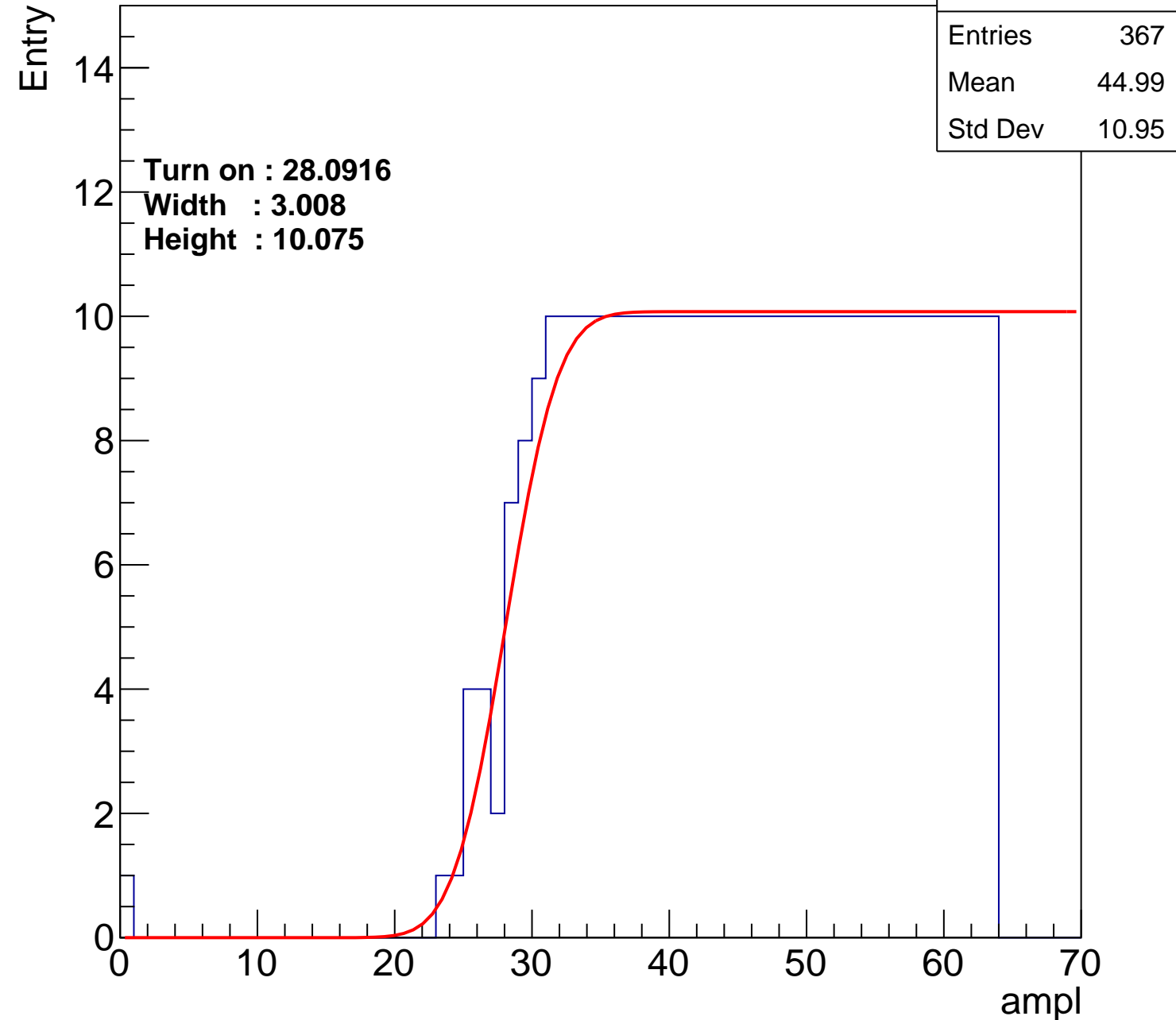
Width : 3.008

Height : 10.075

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch26

calib_packv5_042523_0143.root, FC#0, port D2

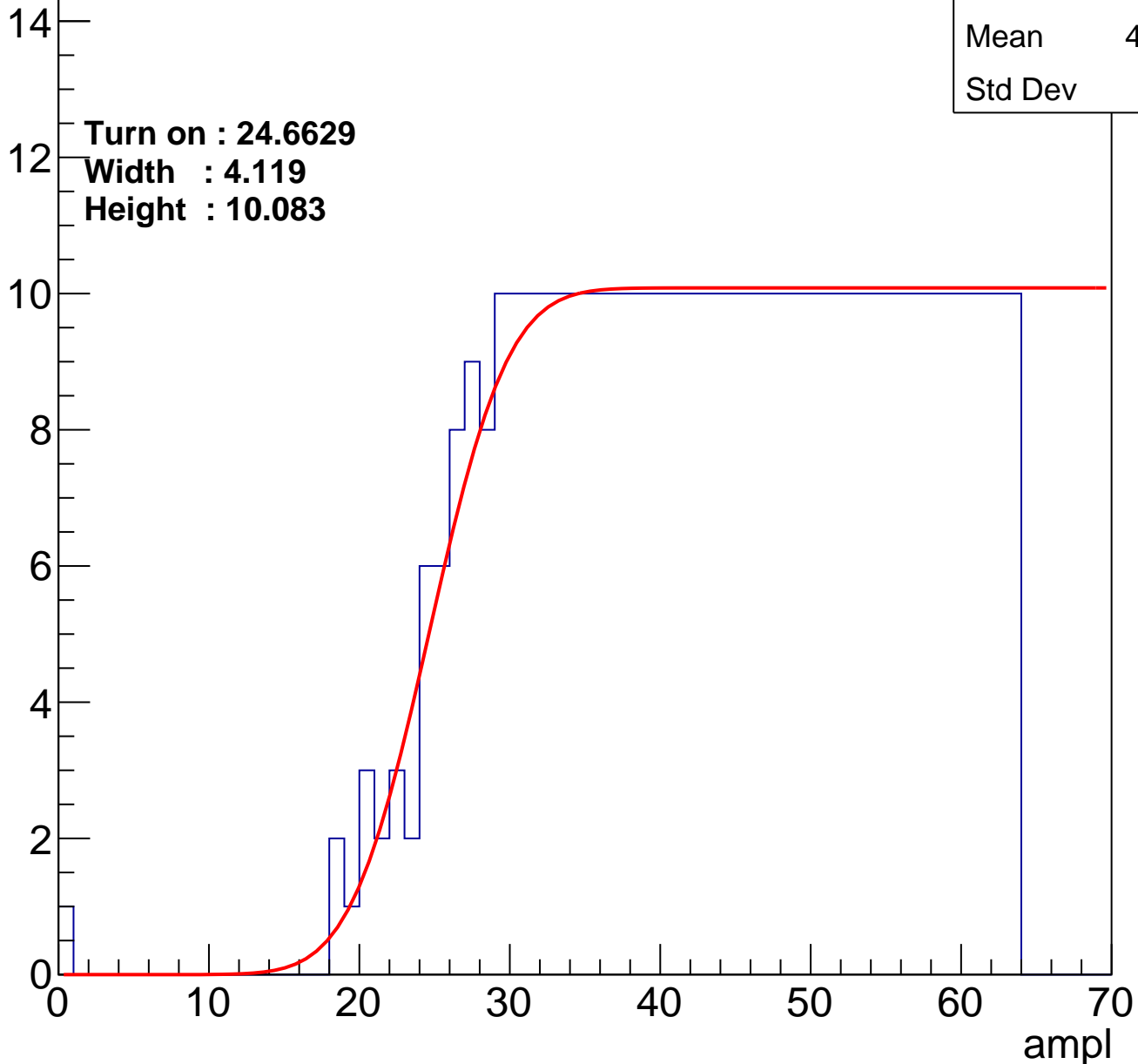
Entries	401
Mean	43.24
Std Dev	12

Turn on : 24.6629

Width : 4.119

Height : 10.083

Entry



B1L101S, U10-ch27

calib_packv5_042523_0143.root, FC#0, port D2

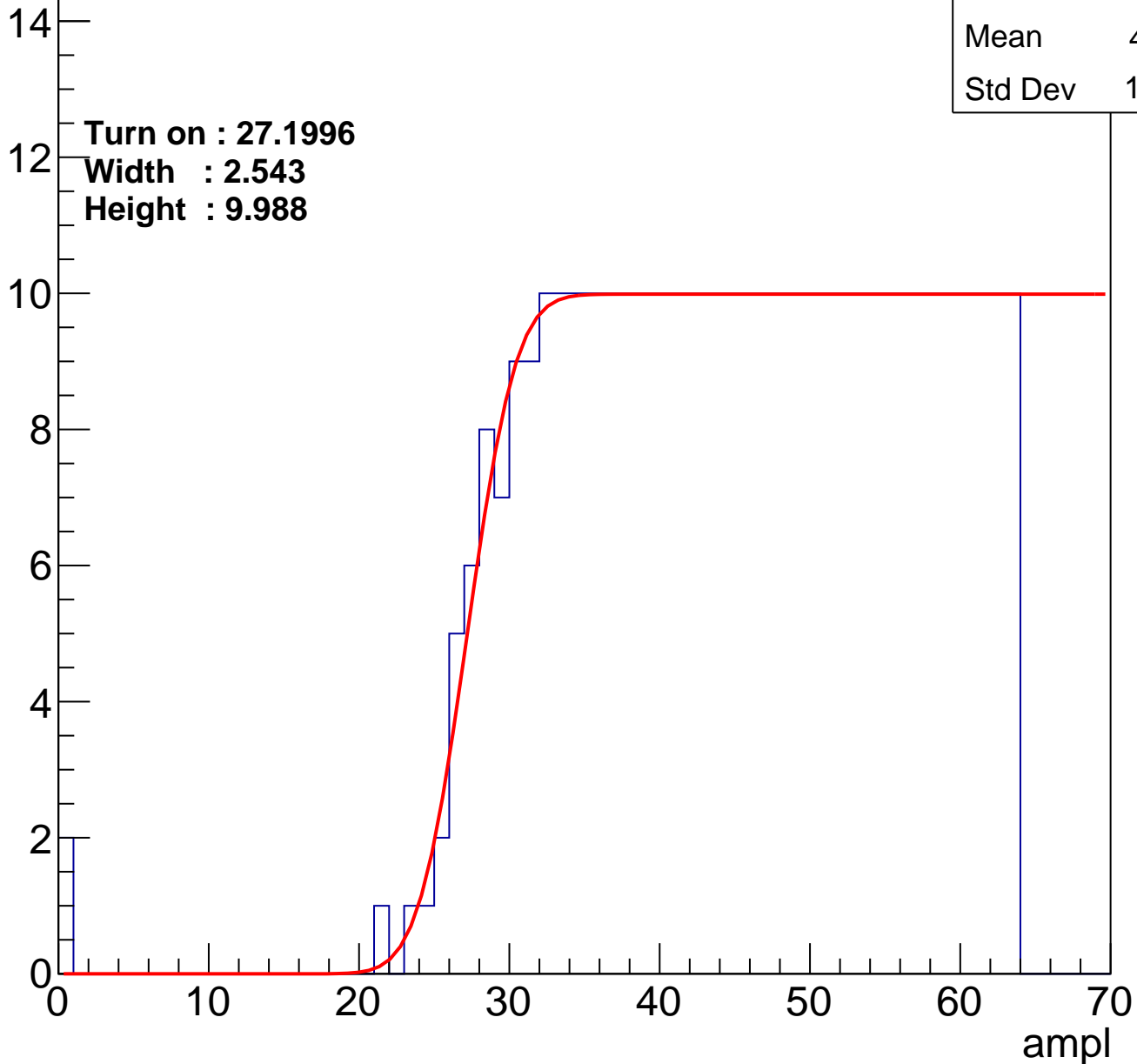
Entries	371
Mean	44.71
Std Dev	11.28

Turn on : 27.1996

Width : 2.543

Height : 9.988

Entry



B1L101S, U10-ch28

calib_packv5_042523_0143.root, FC#0, port D2

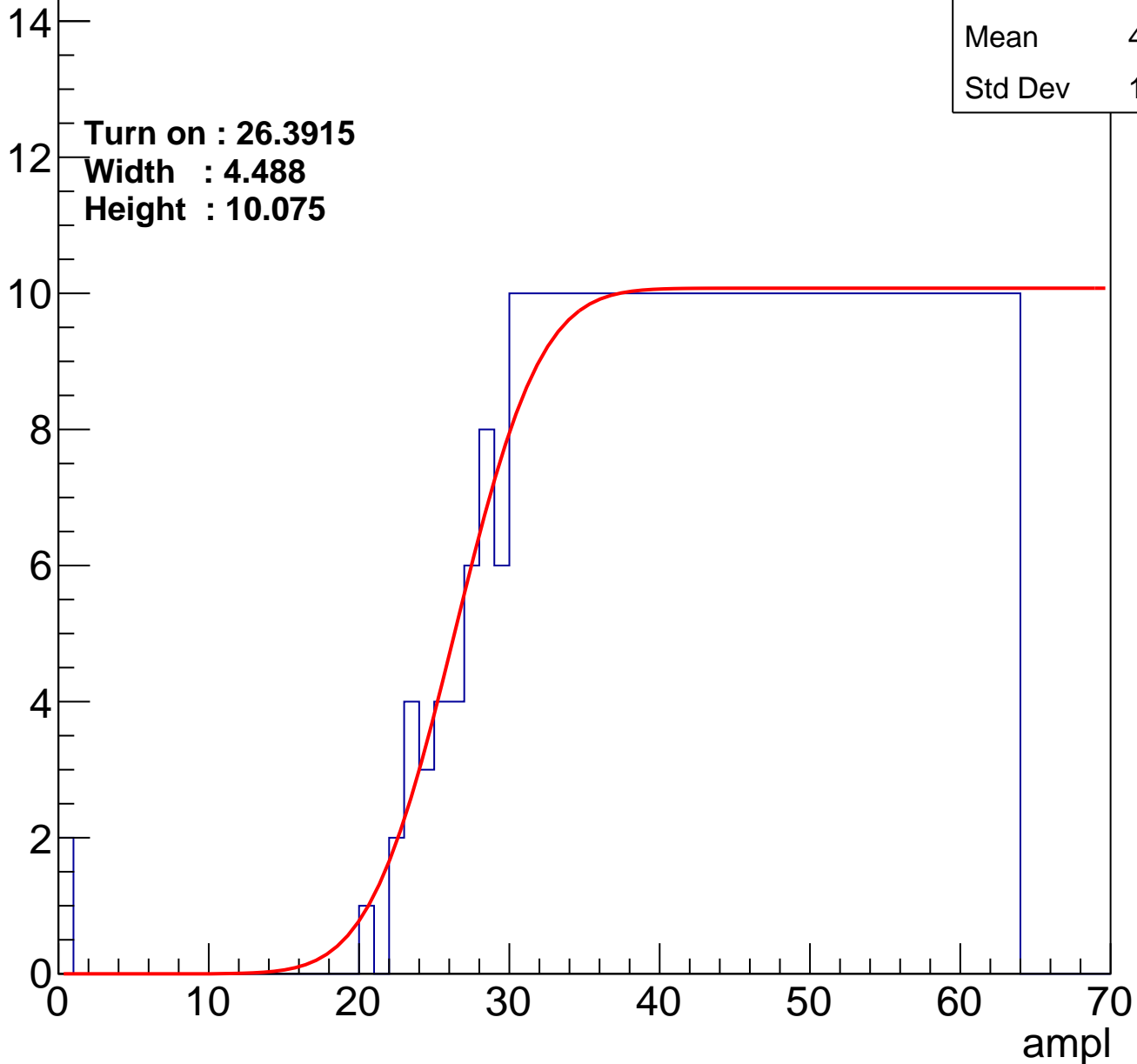
Entries	380
Mean	44.22
Std Dev	11.59

Turn on : 26.3915

Width : 4.488

Height : 10.075

Entry



B1L101S, U10-ch29

calib_packv5_042523_0143.root, FC#0, port D2

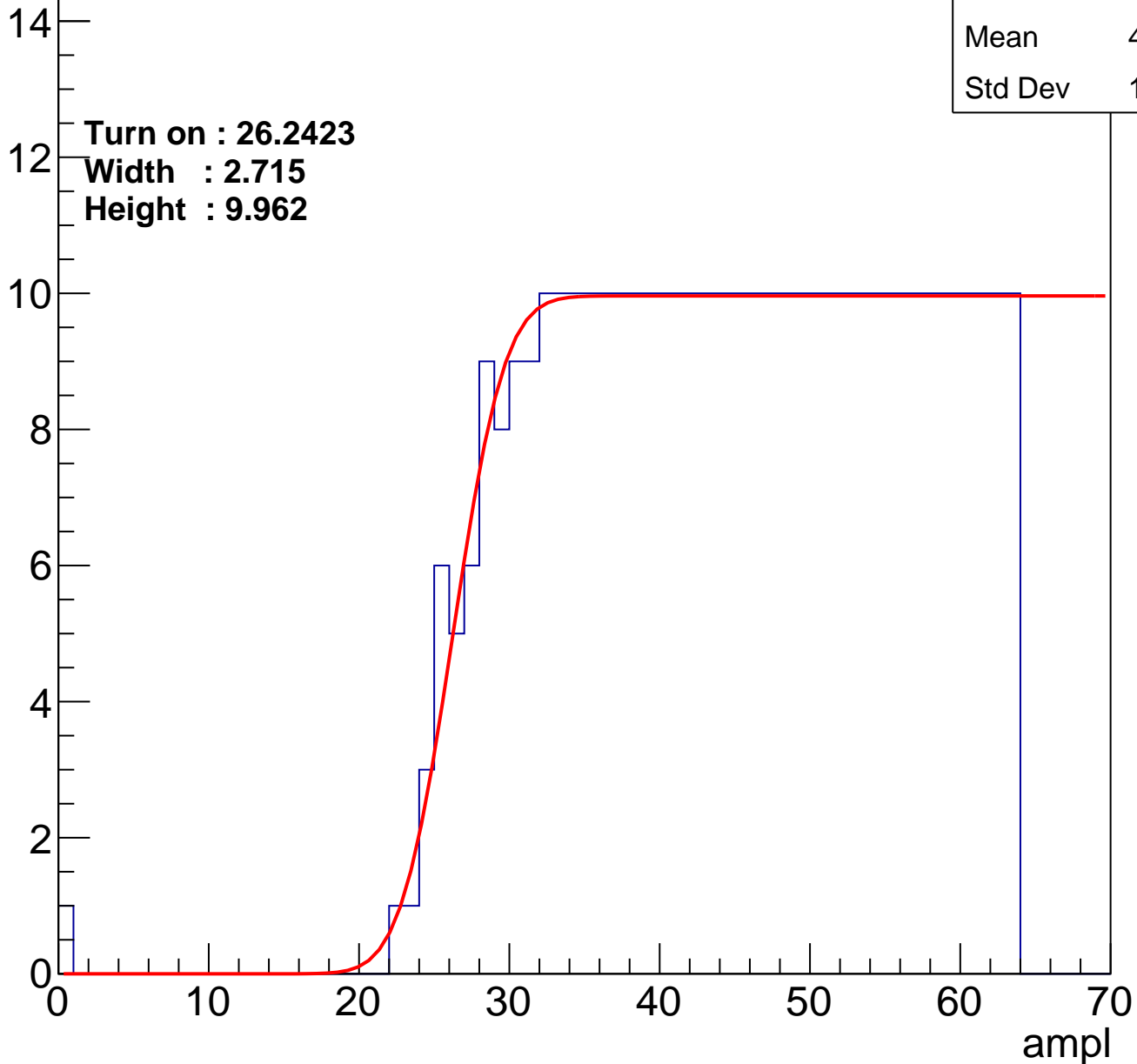
Entries	378
Mean	44.42
Std Dev	11.28

Turn on : 26.2423

Width : 2.715

Height : 9.962

Entry



B1L101S, U10-ch30

calib_packv5_042523_0143.root, FC#0, port D2

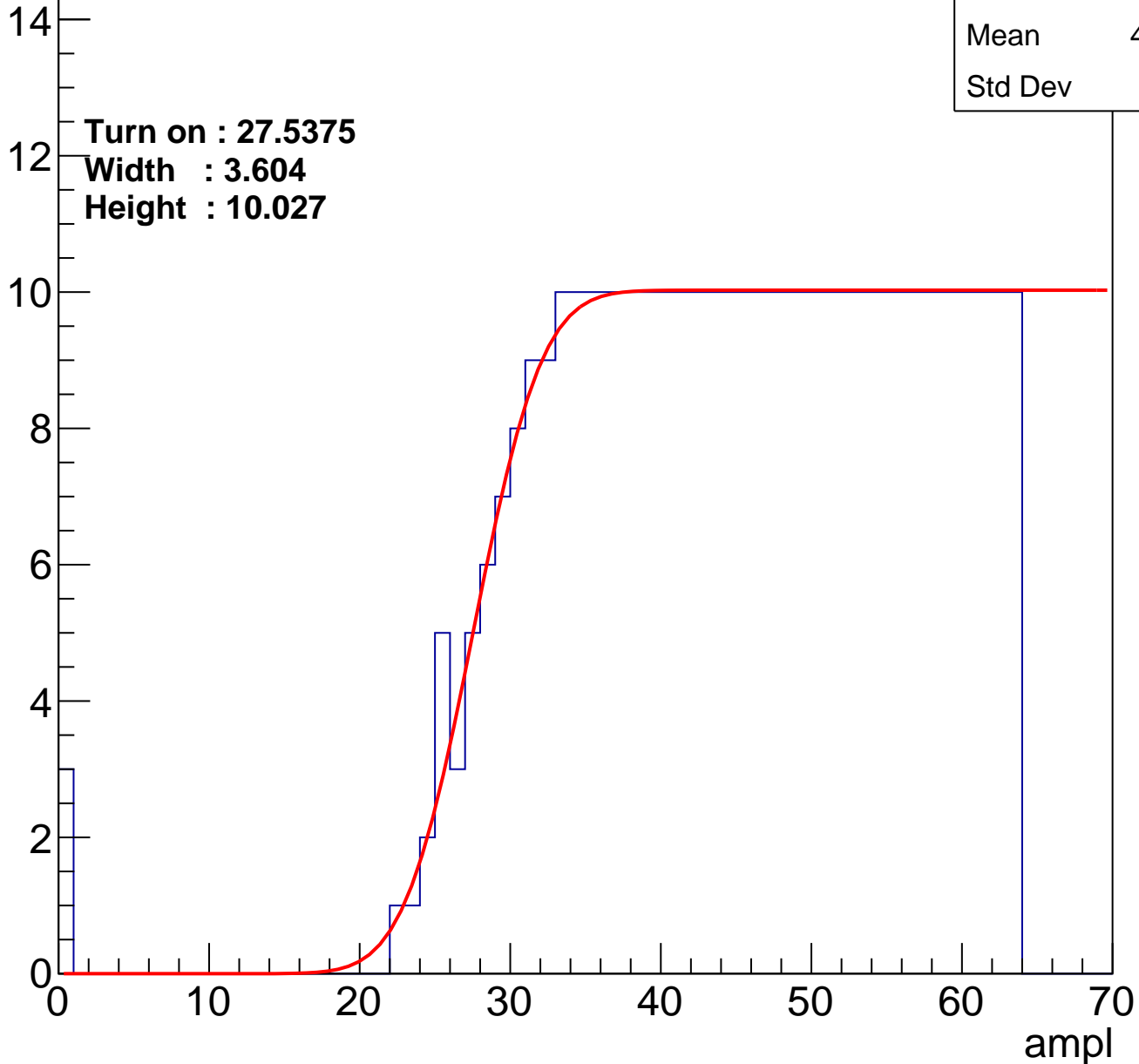
Entries	369
Mean	44.69
Std Dev	11.5

Turn on : 27.5375

Width : 3.604

Height : 10.027

Entry



B1L101S, U10-ch31

calib_packv5_042523_0143.root, FC#0, port D2

Entries	365
Mean	44.94
Std Dev	11.32

Turn on : 28.1660

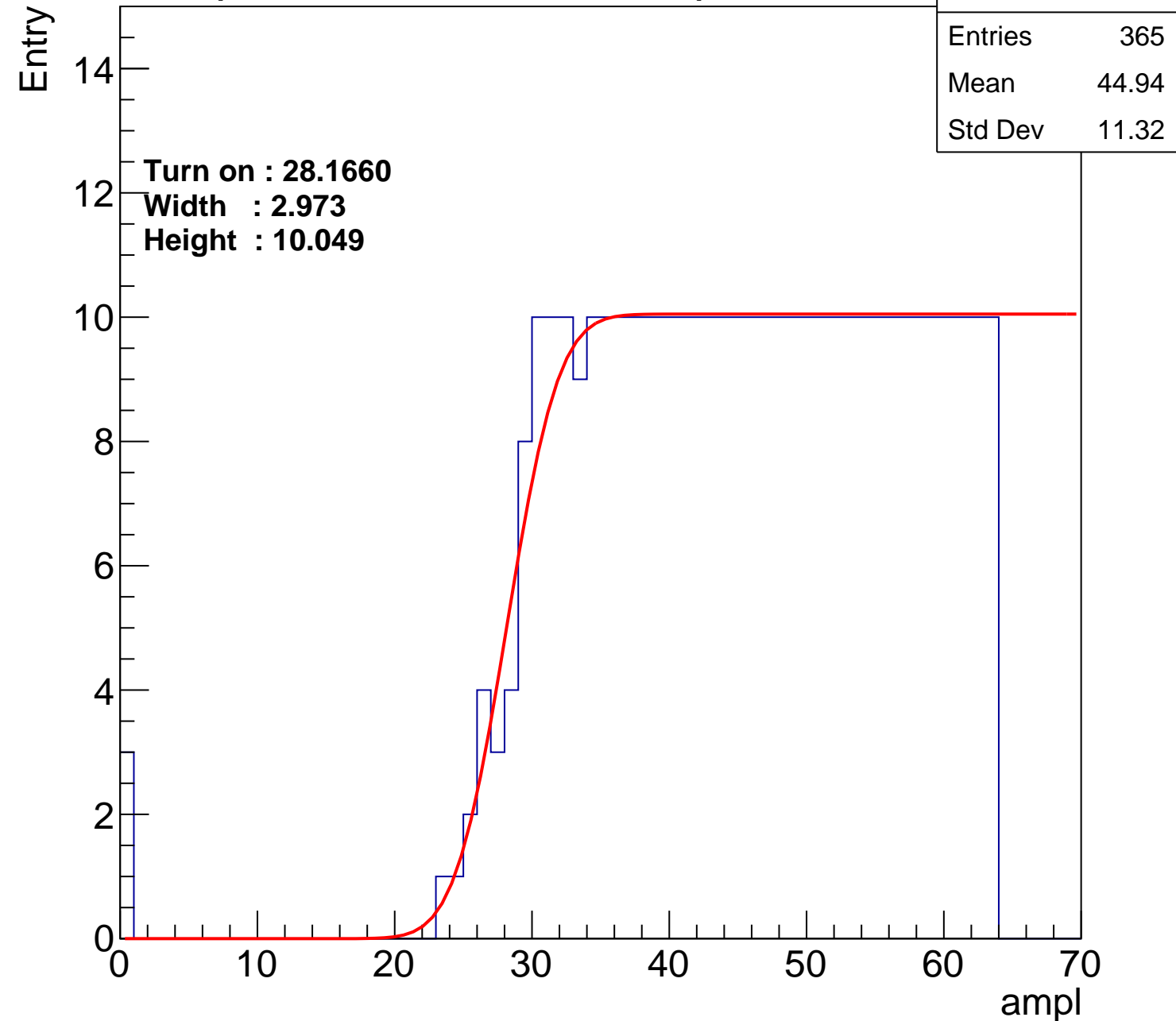
Width : 2.973

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch32

calib_packv5_042523_0143.root, FC#0, port D2

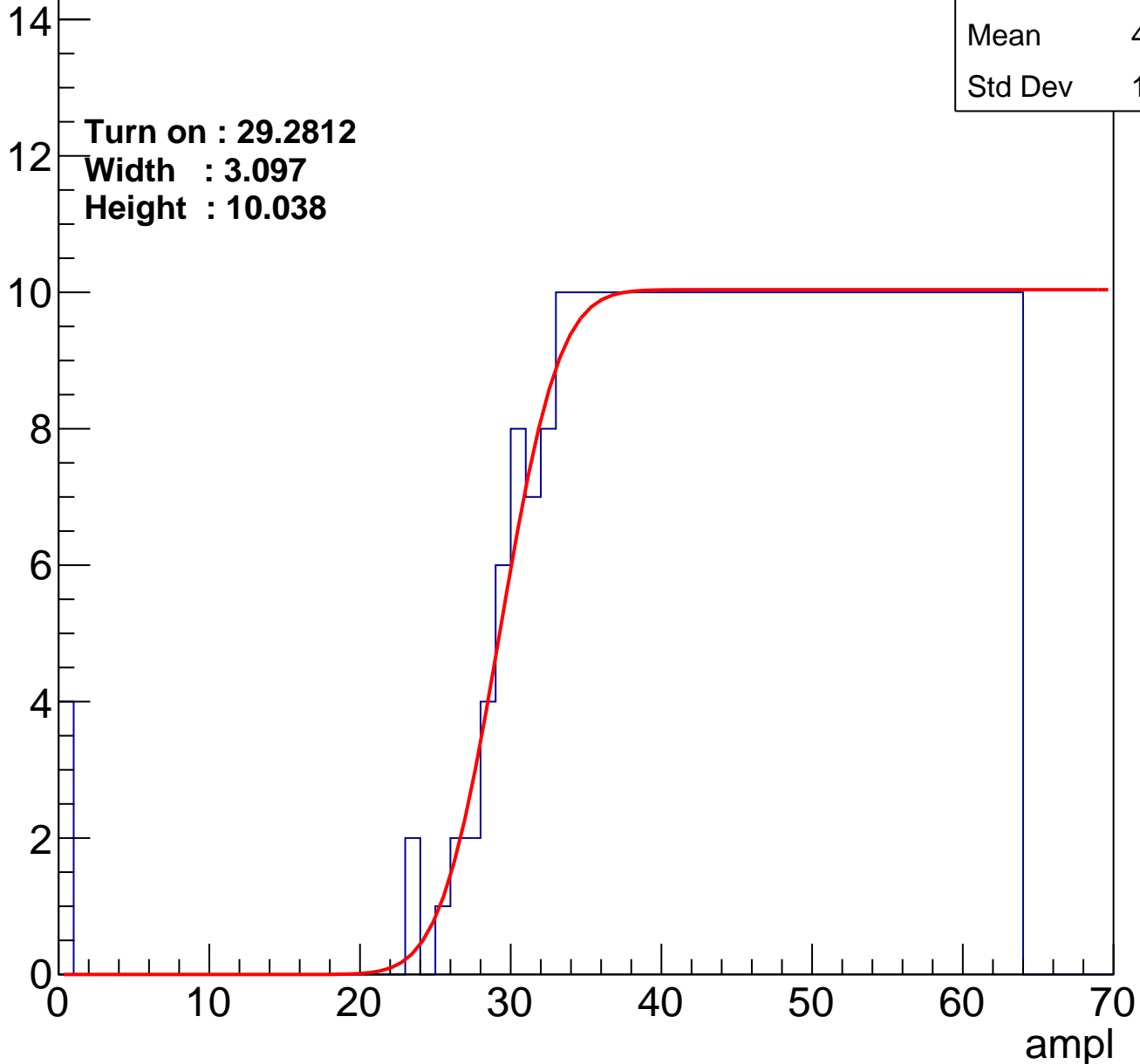
Entries	354
Mean	45.36
Std Dev	11.35

Turn on : 29.2812

Width : 3.097

Height : 10.038

Entry



B1L101S, U10-ch33

calib_packv5_042523_0143.root, FC#0, port D2

Entries	365
Mean	44.93
Std Dev	11.34

Turn on : 28.1355

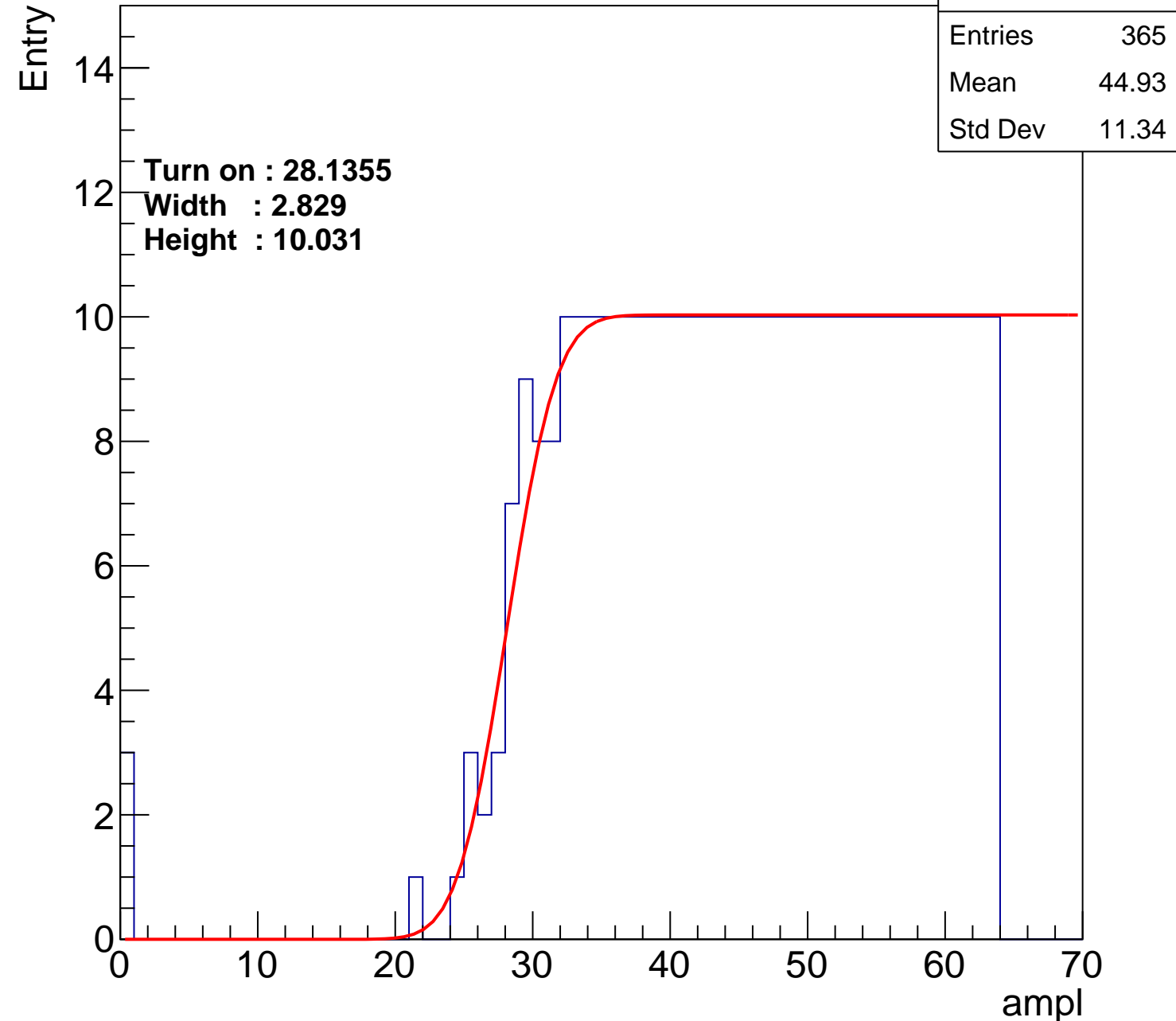
Width : 2.829

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch34

calib_packv5_042523_0143.root, FC#0, port D2

Entries	370
Mean	44.86
Std Dev	10.99

Turn on : 26.9415

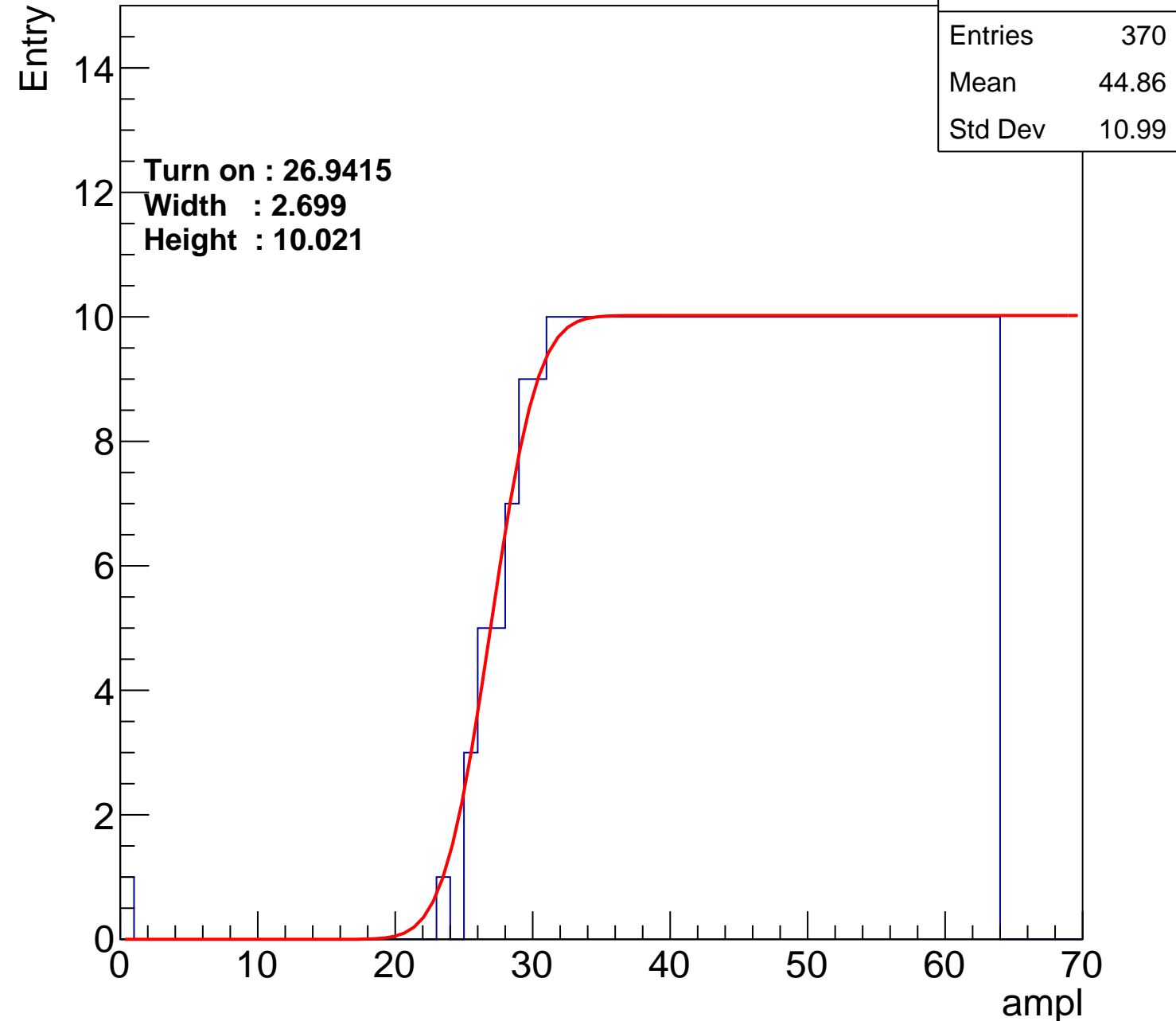
Width : 2.699

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch35

calib_packv5_042523_0143.root, FC#0, port D2

Entries	363
Mean	45.22
Std Dev	10.98

Turn on : 28.3048

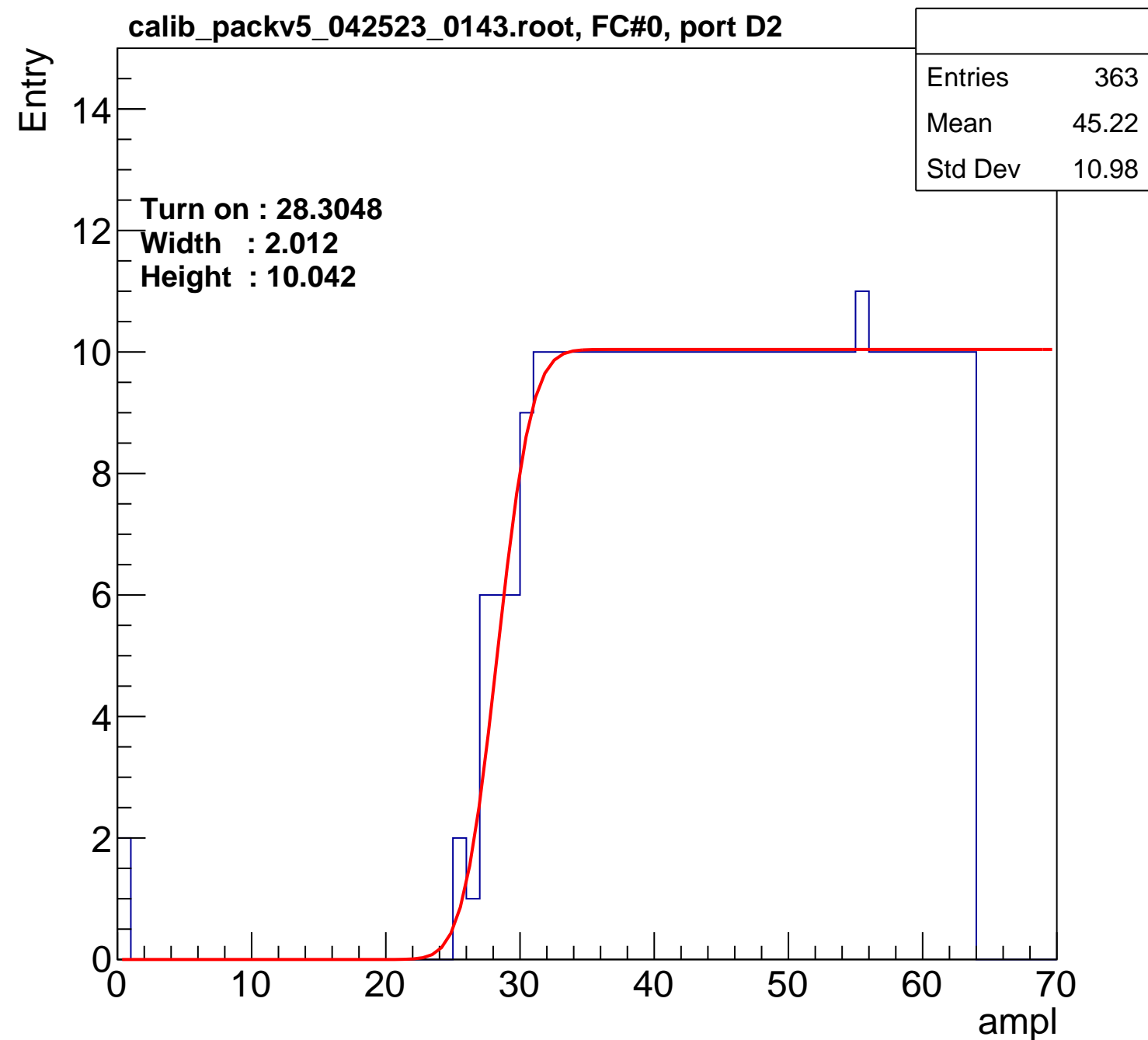
Width : 2.012

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch36

calib_packv5_042523_0143.root, FC#0, port D2

Entries	370
Mean	44.59
Std Dev	11.69

Turn on : 28.1541

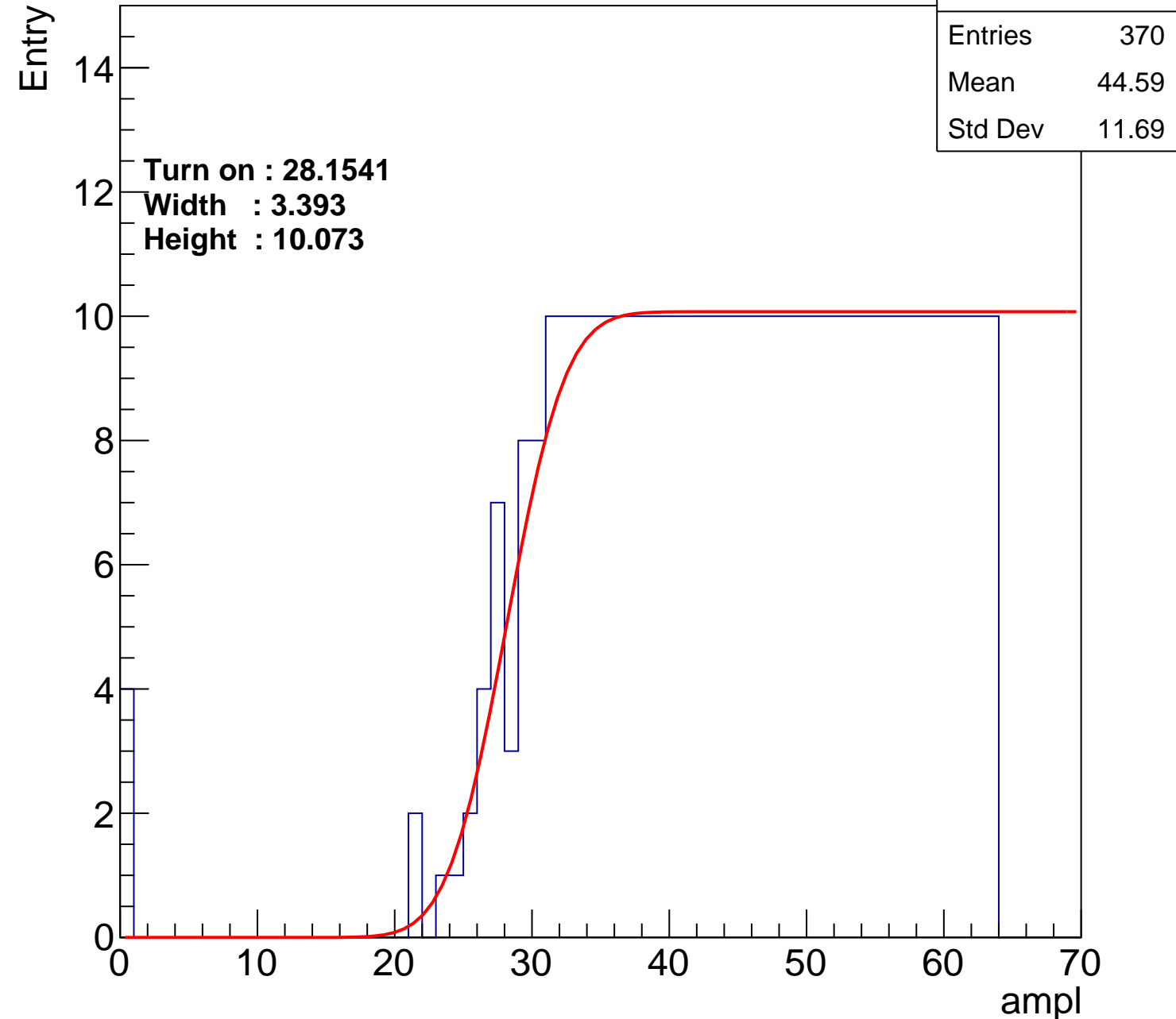
Width : 3.393

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch37

calib_packv5_042523_0143.root, FC#0, port D2

Entries	365
Mean	44.99
Std Dev	11.16

Turn on : 28.0436

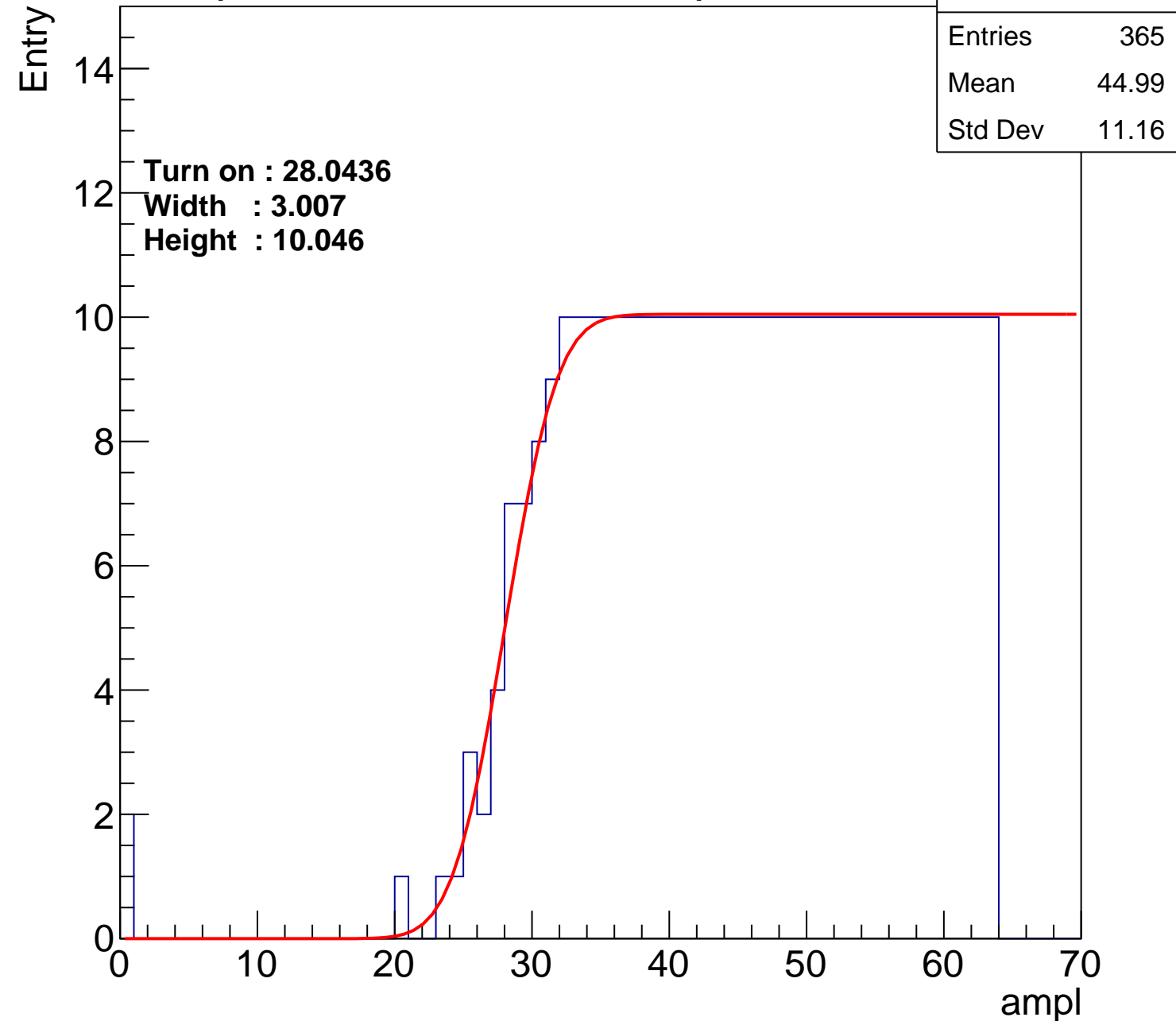
Width : 3.007

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch38

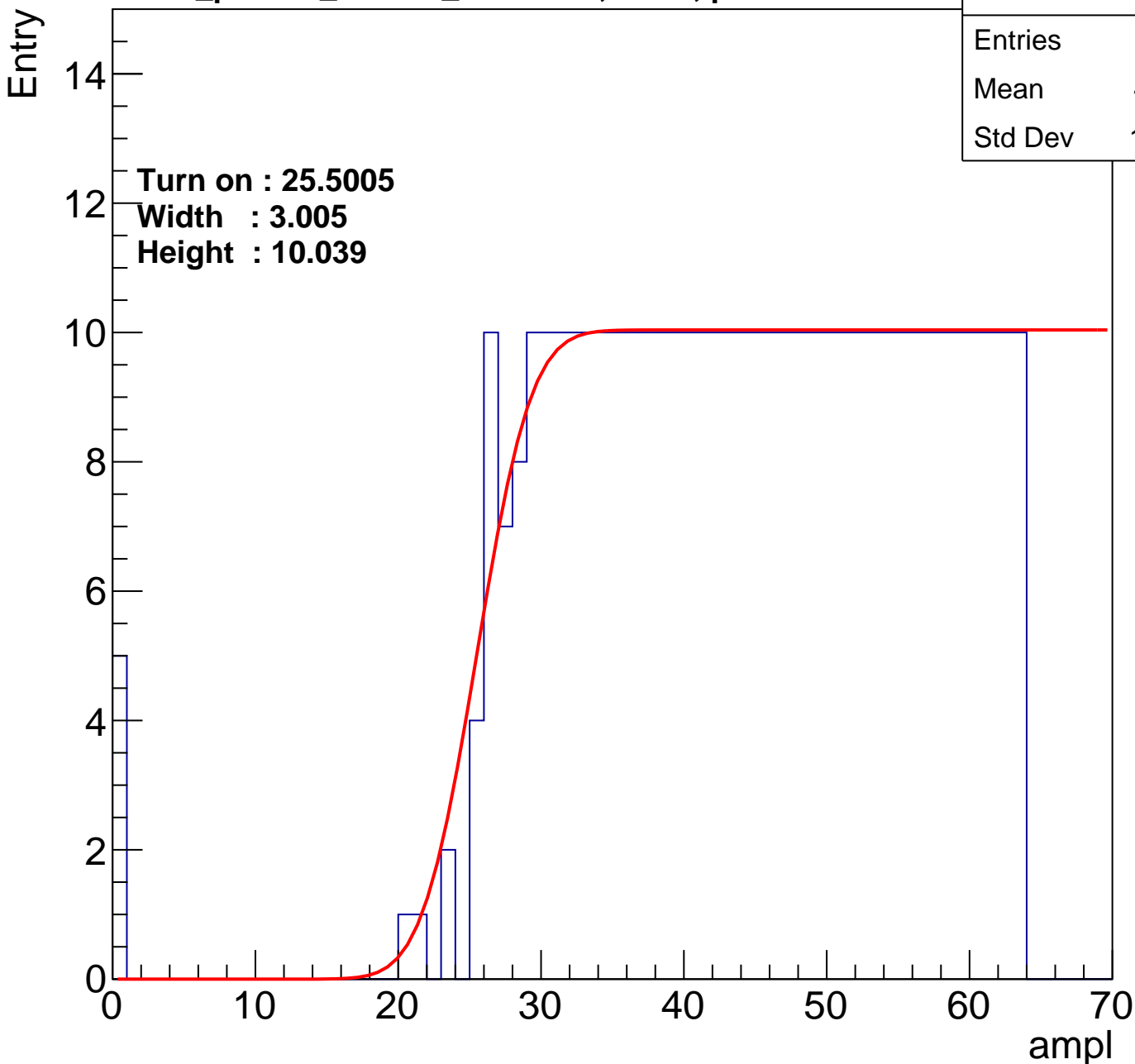
calib_packv5_042523_0143.root, FC#0, port D2

Entries	388
Mean	43.71
Std Dev	12.17

Turn on : 25.5005

Width : 3.005

Height : 10.039



B1L101S, U10-ch39

calib_packv5_042523_0143.root, FC#0, port D2

Entries	365
Mean	44.98
Std Dev	11.17

Turn on : 27.7948

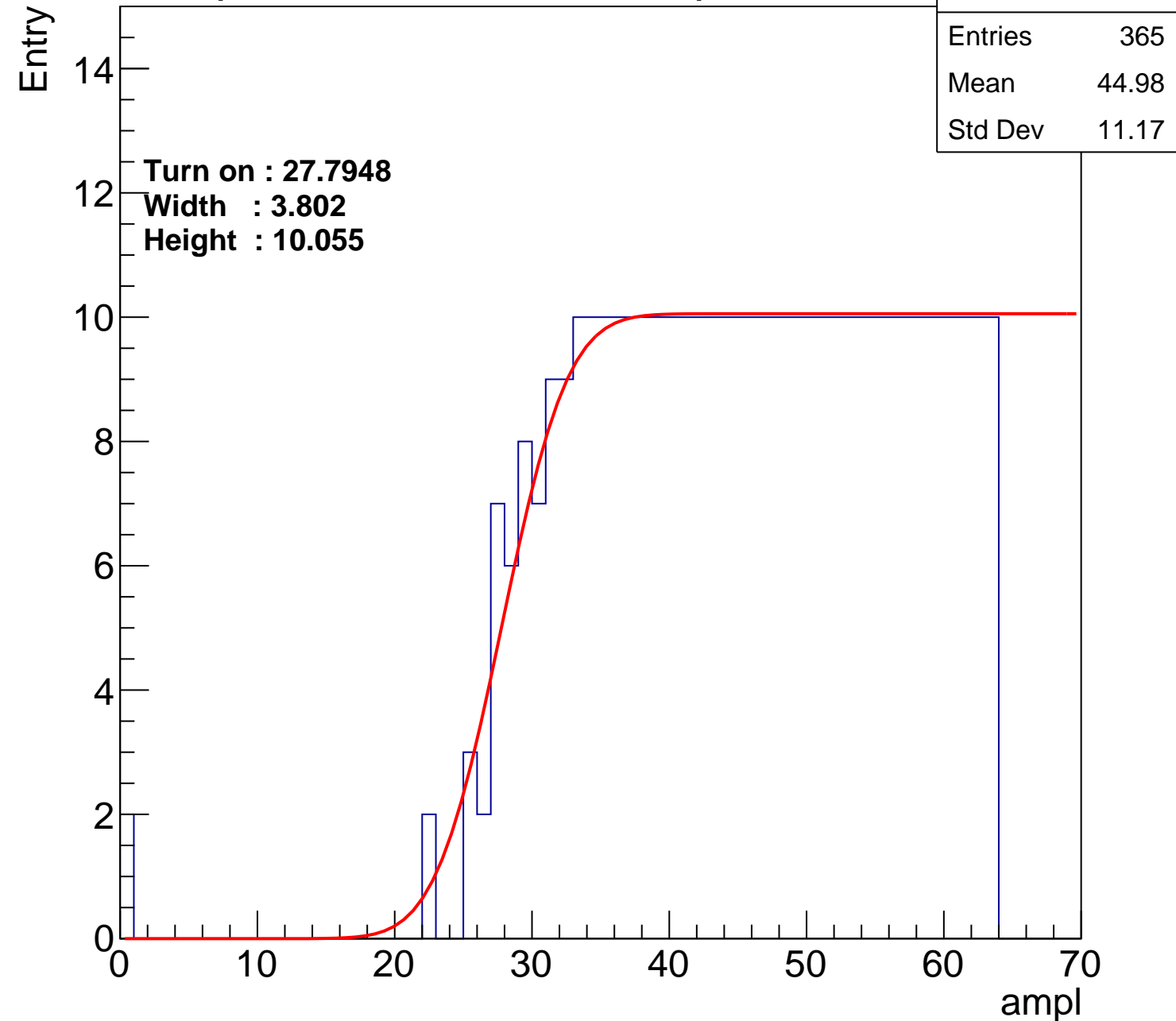
Width : 3.802

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch40

calib_packv5_042523_0143.root, FC#0, port D2

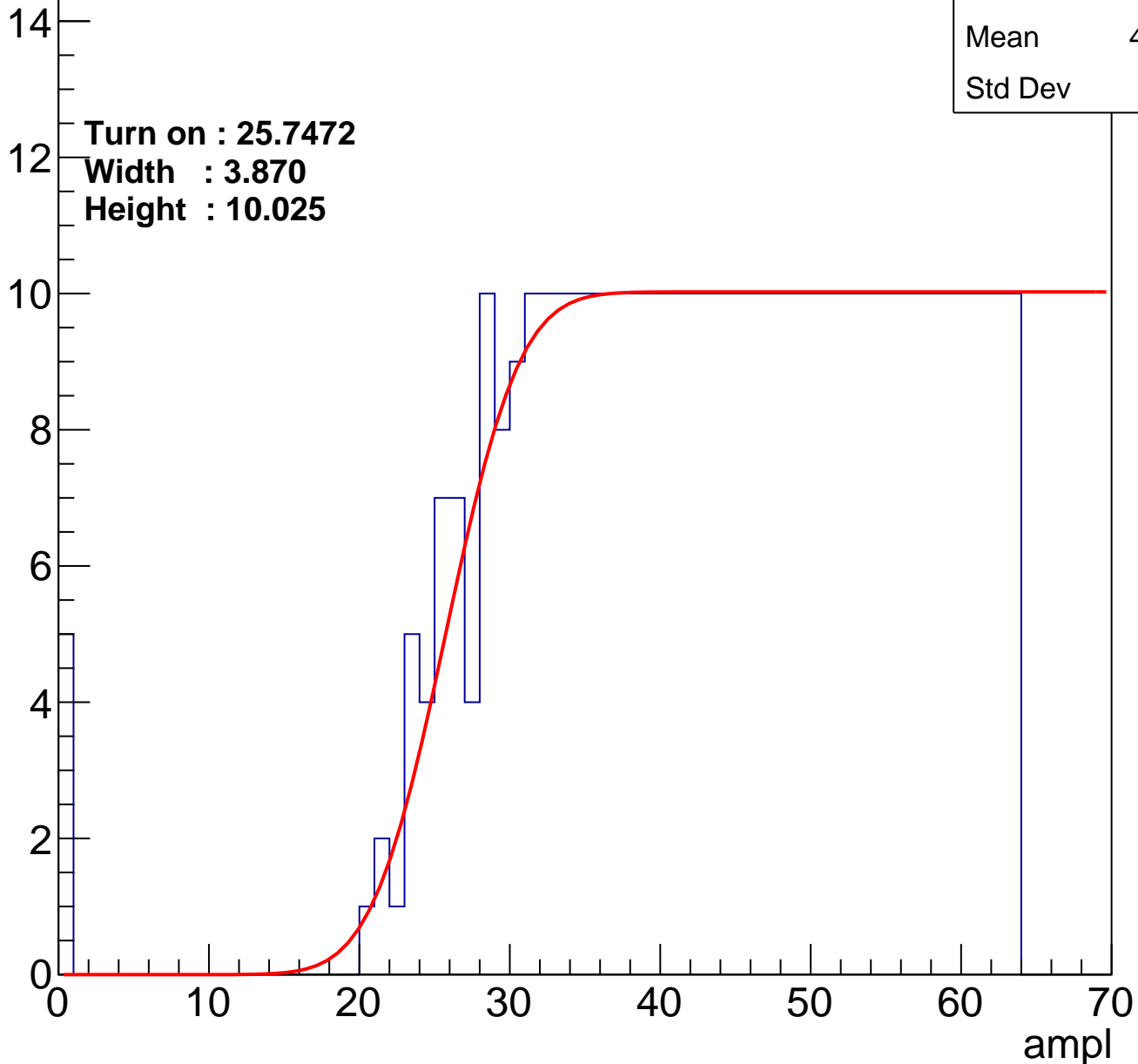
Entries	393
Mean	43.39
Std Dev	12.4

Turn on : 25.7472

Width : 3.870

Height : 10.025

Entry



B1L101S, U10-ch41

calib_packv5_042523_0143.root, FC#0, port D2

Entries	393
Mean	43.61
Std Dev	11.93

Turn on : 24.4422

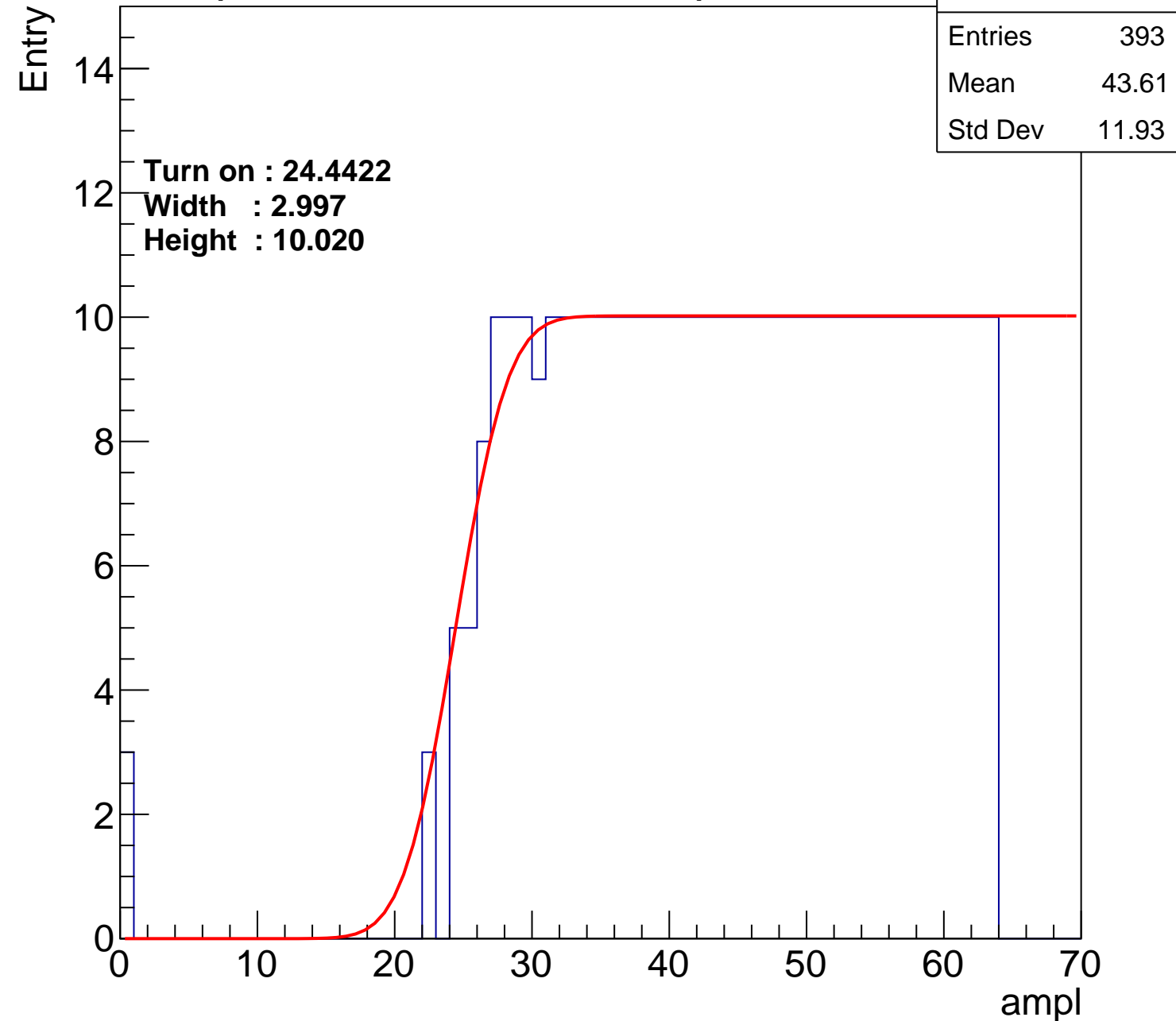
Width : 2.997

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch42

calib_packv5_042523_0143.root, FC#0, port D2

Entries	371
Mean	44.76
Std Dev	11.11

Turn on : 27.1985

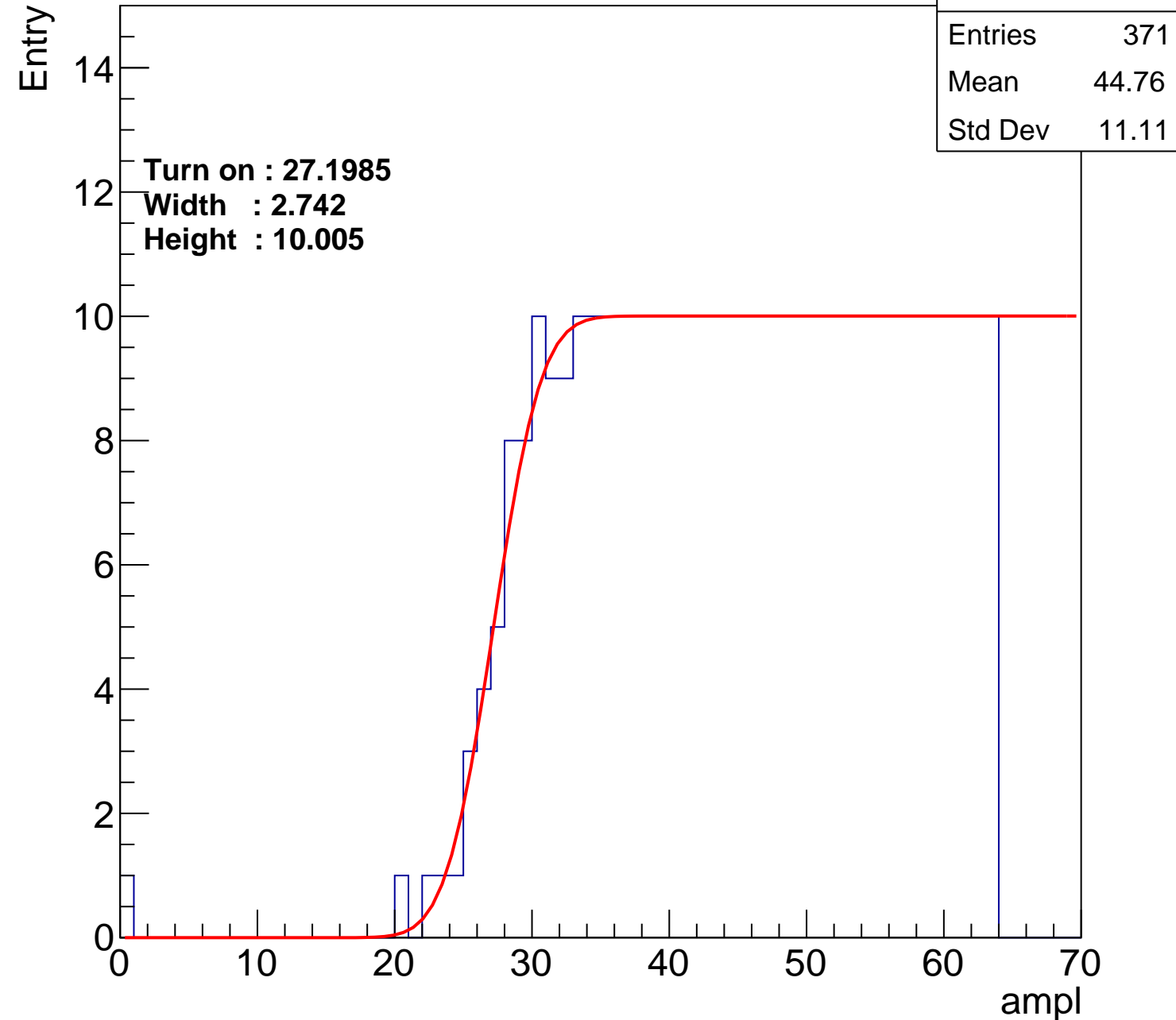
Width : 2.742

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch43

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.57
Std Dev	11.2

Turn on : 26.8636

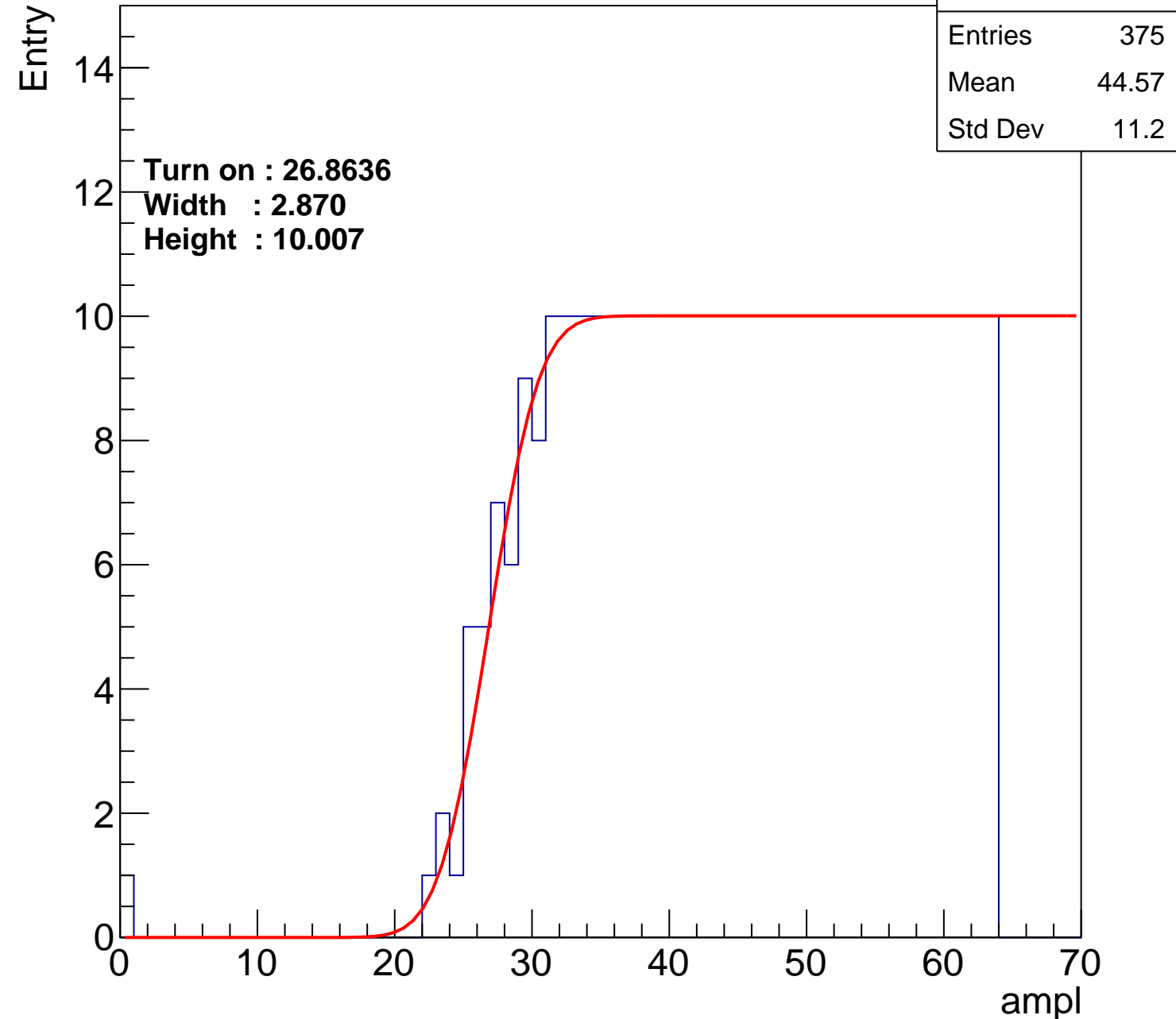
Width : 2.870

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch44

calib_packv5_042523_0143.root, FC#0, port D2

Entries	383
Mean	44.05
Std Dev	11.76

Turn on : 26.1510

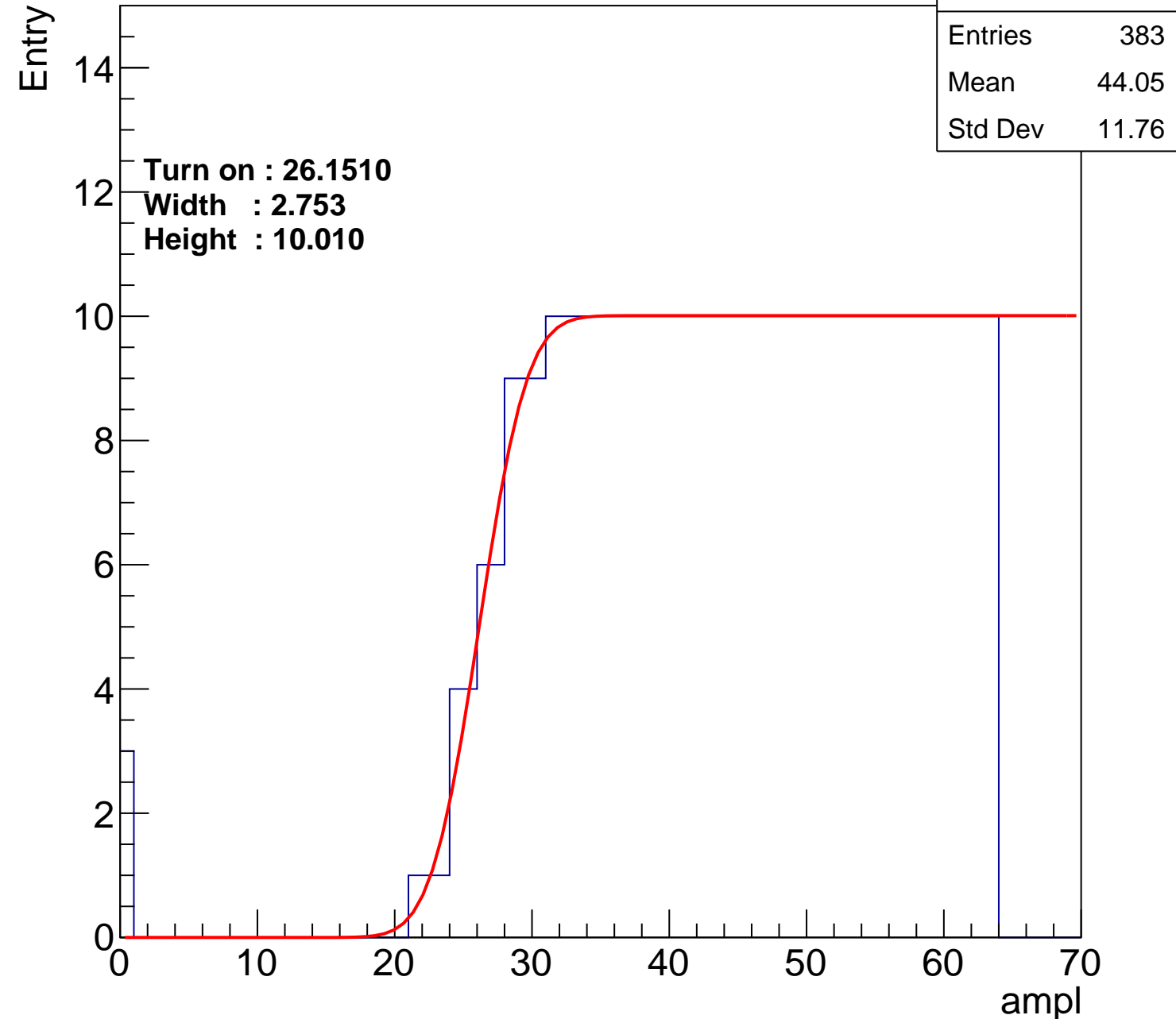
Width : 2.753

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch45

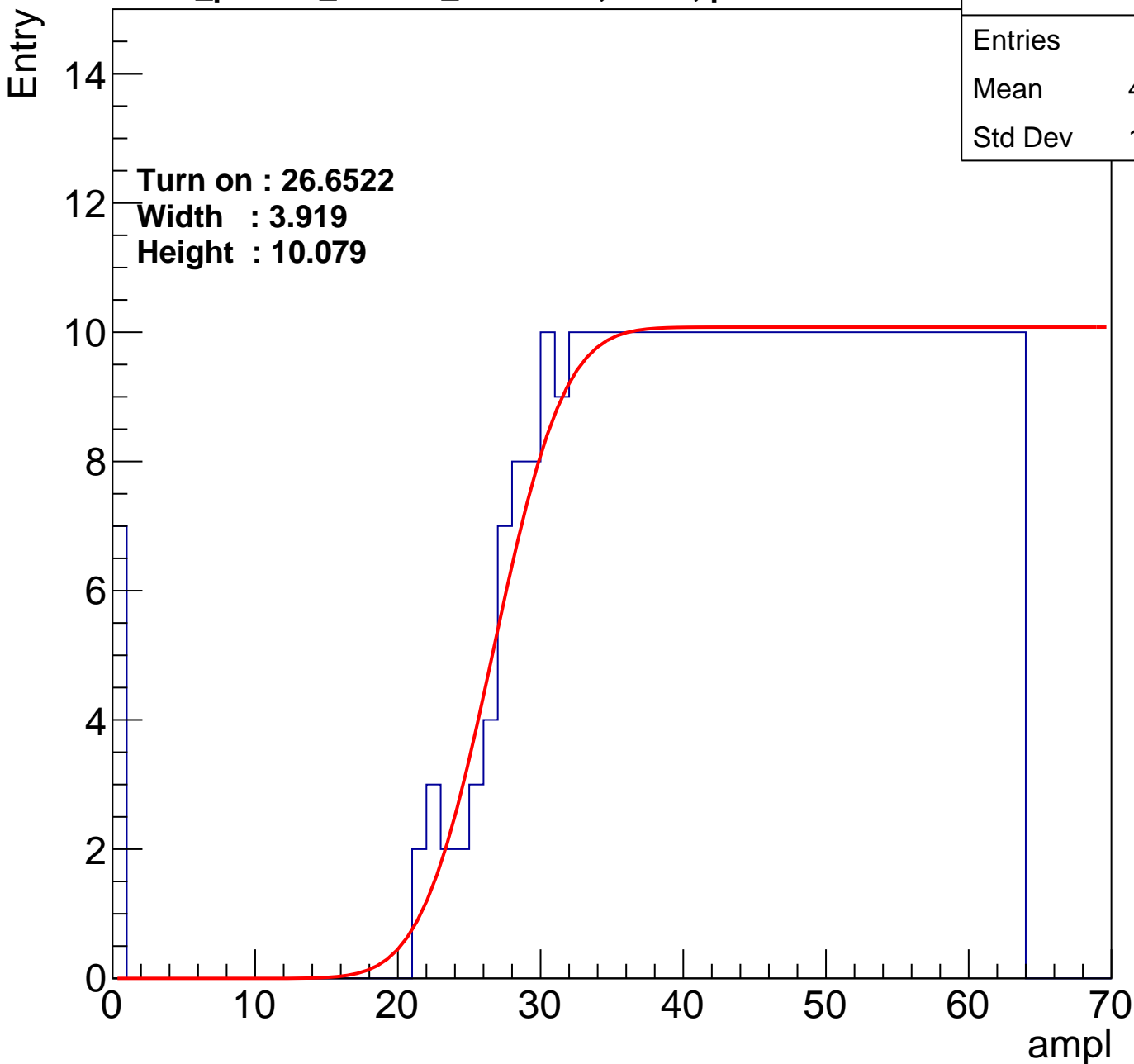
calib_packv5_042523_0143.root, FC#0, port D2

Entries	385
Mean	43.65
Std Dev	12.55

Turn on : 26.6522

Width : 3.919

Height : 10.079



B1L101S, U10-ch46

calib_packv5_042523_0143.root, FC#0, port D2

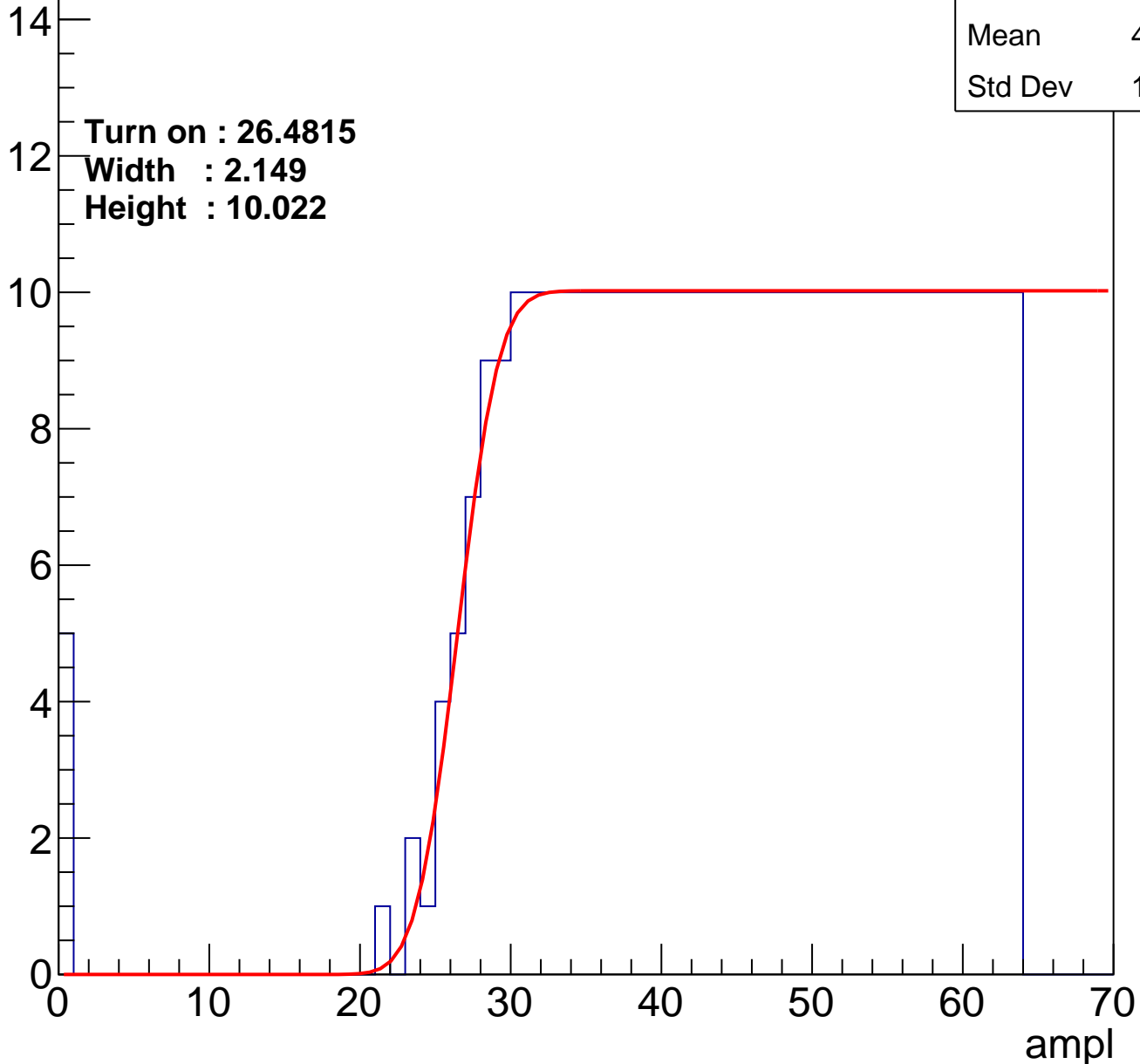
Entries	383
Mean	43.95
Std Dev	12.07

Turn on : 26.4815

Width : 2.149

Height : 10.022

Entry



B1L101S, U10-ch47

calib_packv5_042523_0143.root, FC#0, port D2

Entries	368
Mean	44.88
Std Dev	11.07

Turn on : 27.4022

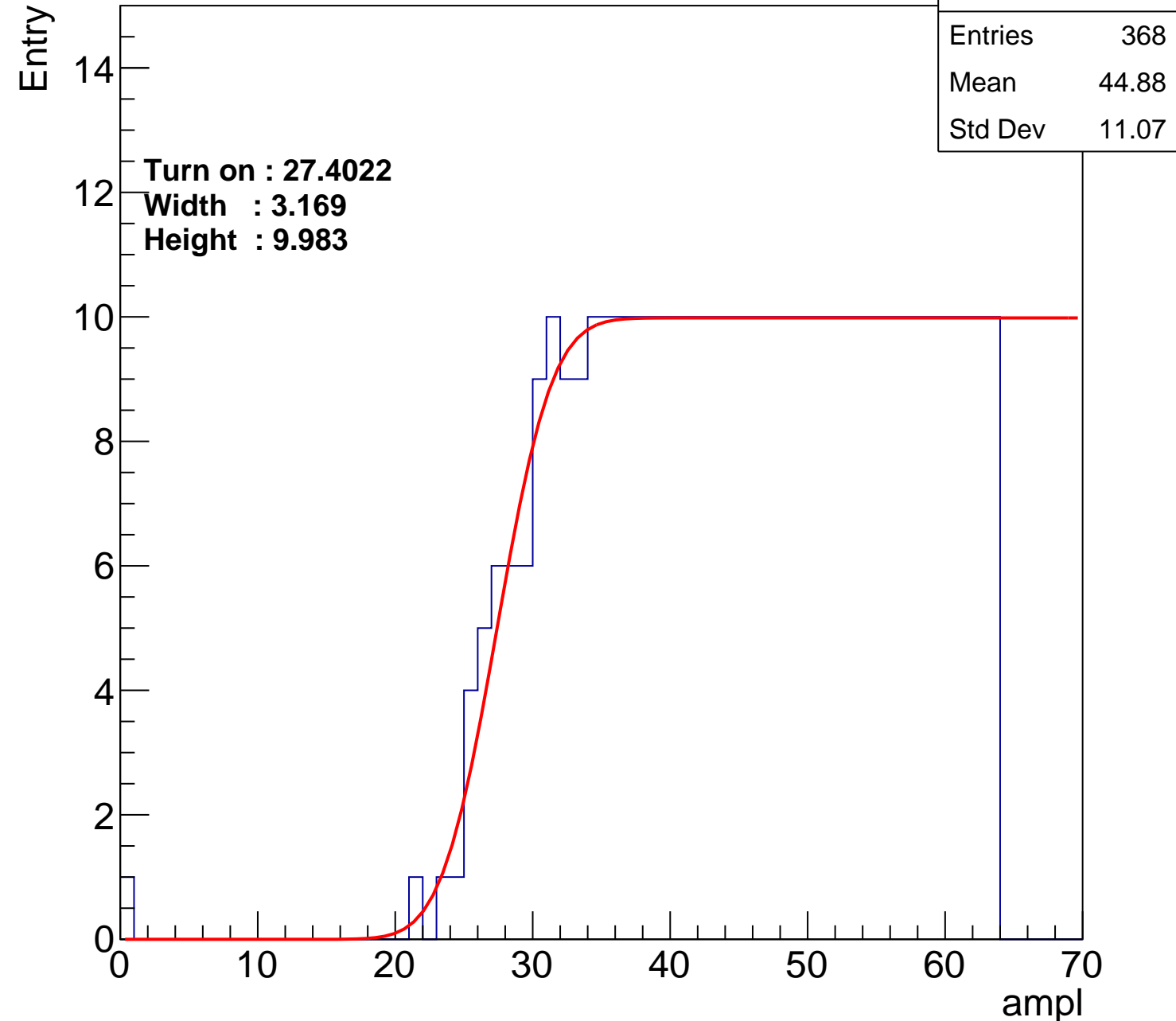
Width : 3.169

Height : 9.983

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch48

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.57
Std Dev	11.34

Turn on : 26.7564

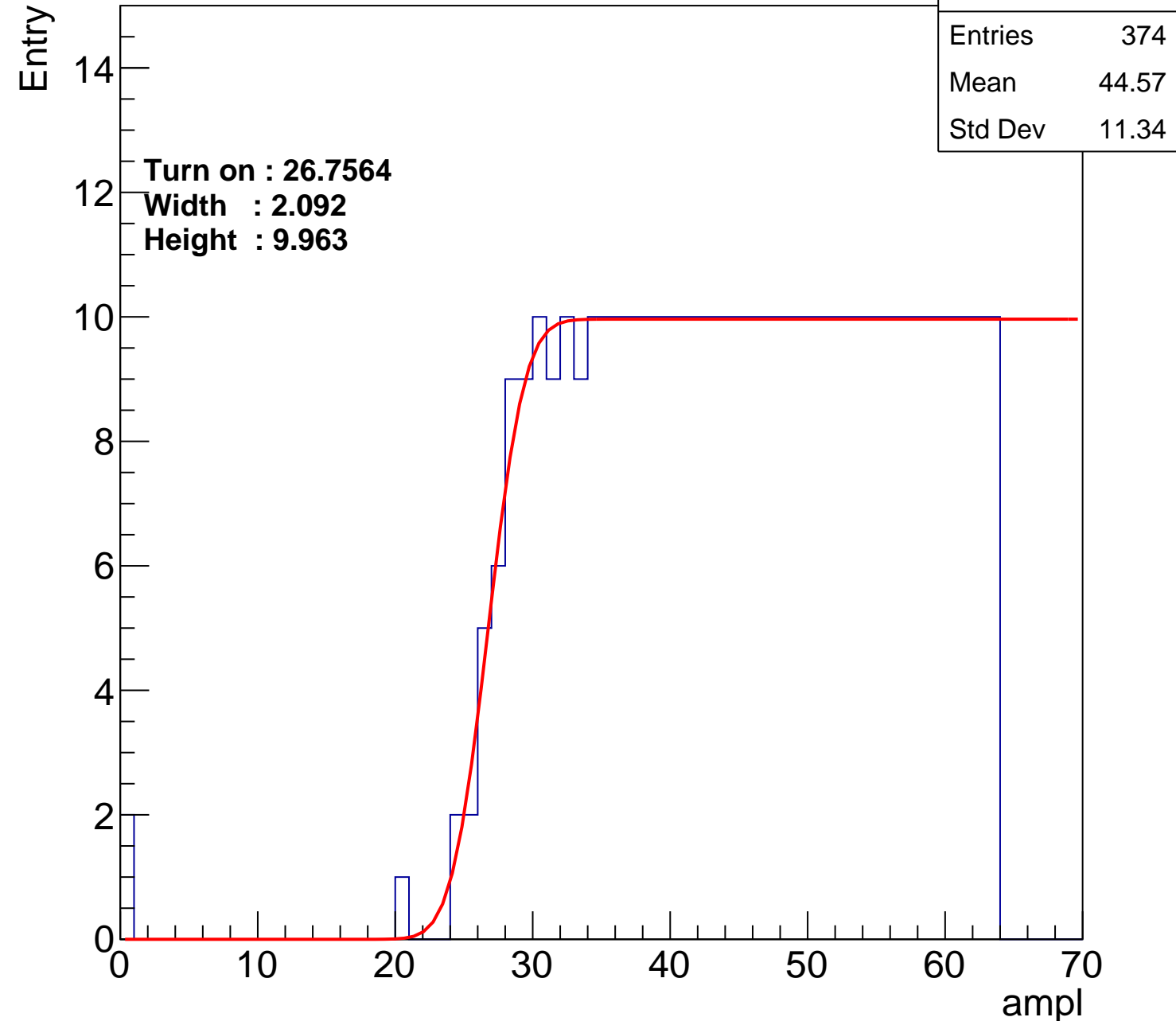
Width : 2.092

Height : 9.963

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch49

calib_packv5_042523_0143.root, FC#0, port D2

Entries	364
Mean	44.8
Std Dev	11.75

Turn on : 28.2813

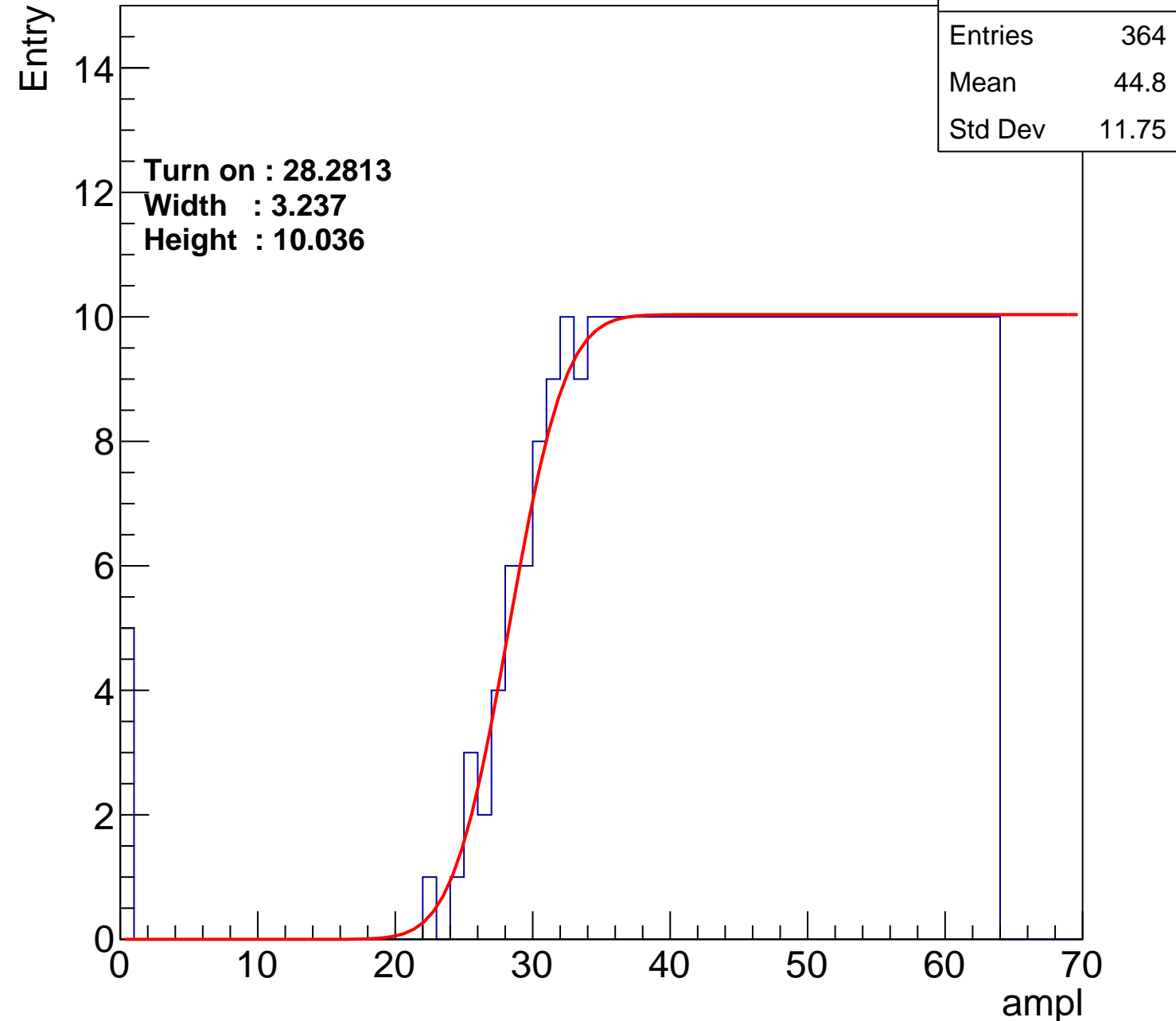
Width : 3.237

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch50

calib_packv5_042523_0143.root, FC#0, port D2

Entries	384
Mean	44.01
Std Dev	11.71

Turn on : 26.4924

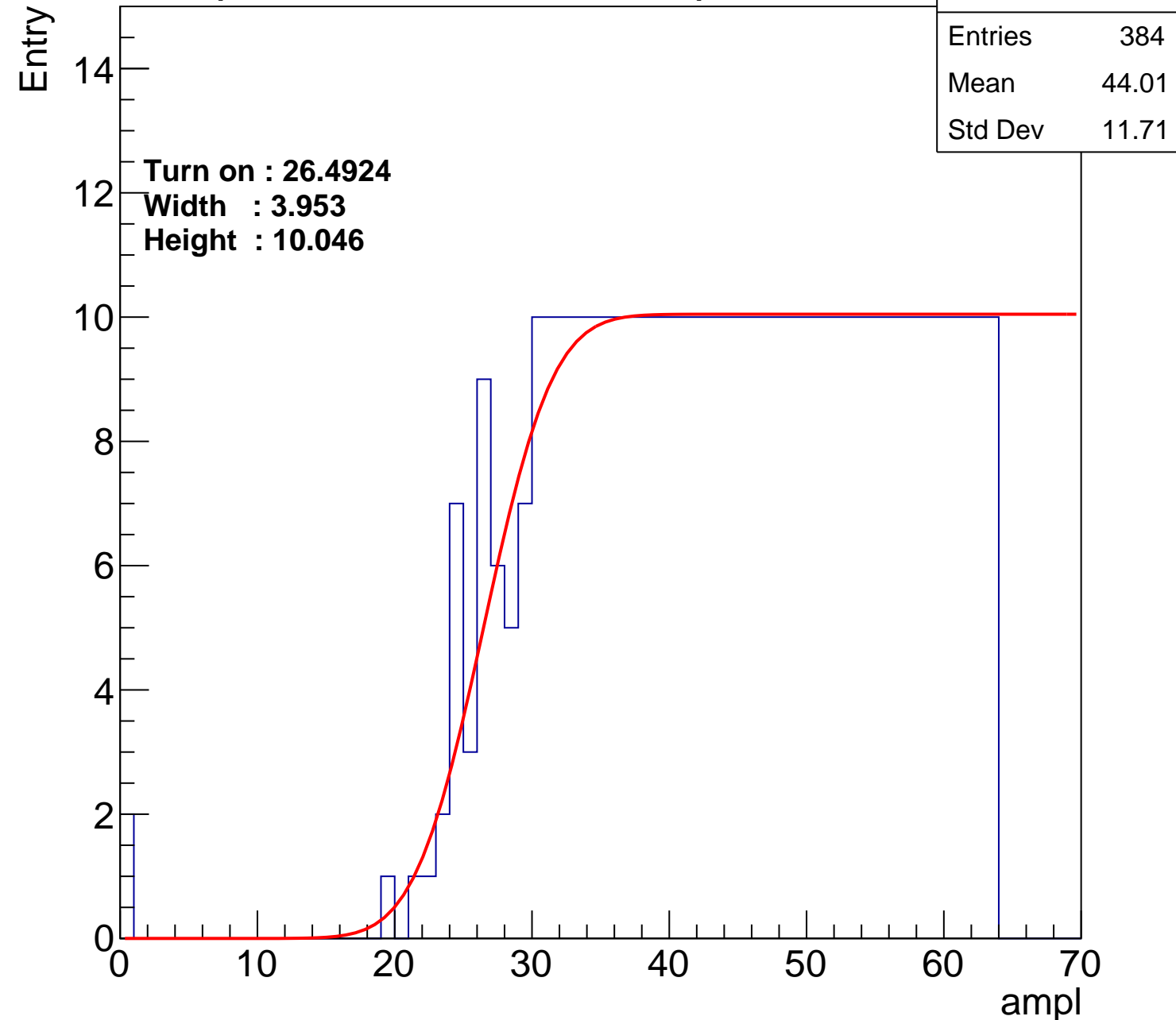
Width : 3.953

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch51

calib_packv5_042523_0143.root, FC#0, port D2

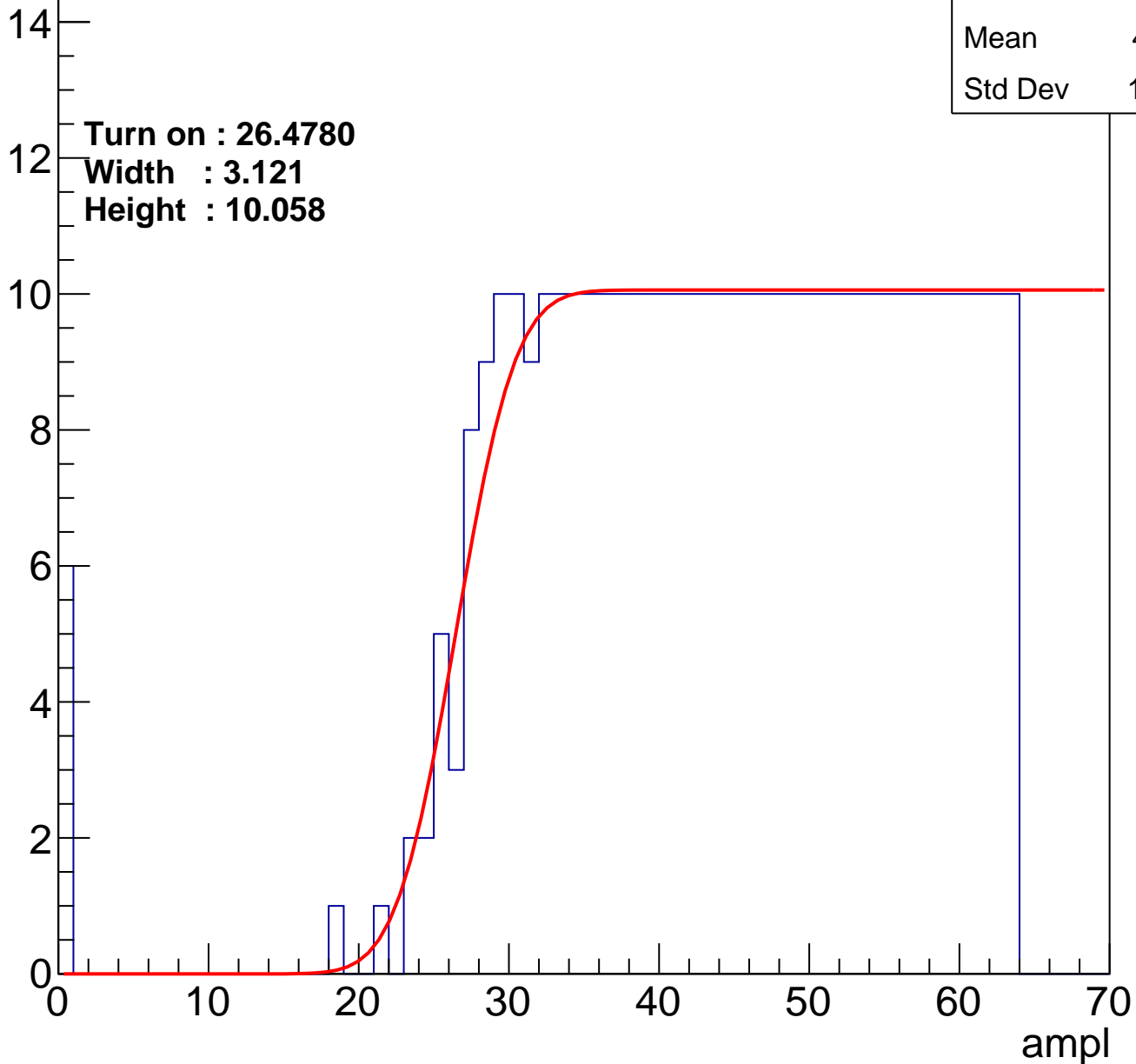
Entries	386
Mean	43.71
Std Dev	12.34

Turn on : 26.4780

Width : 3.121

Height : 10.058

Entry



B1L101S, U10-ch52

calib_packv5_042523_0143.root, FC#0, port D2

Entries	383
Mean	43.75
Std Dev	12.5

Turn on : 26.4712

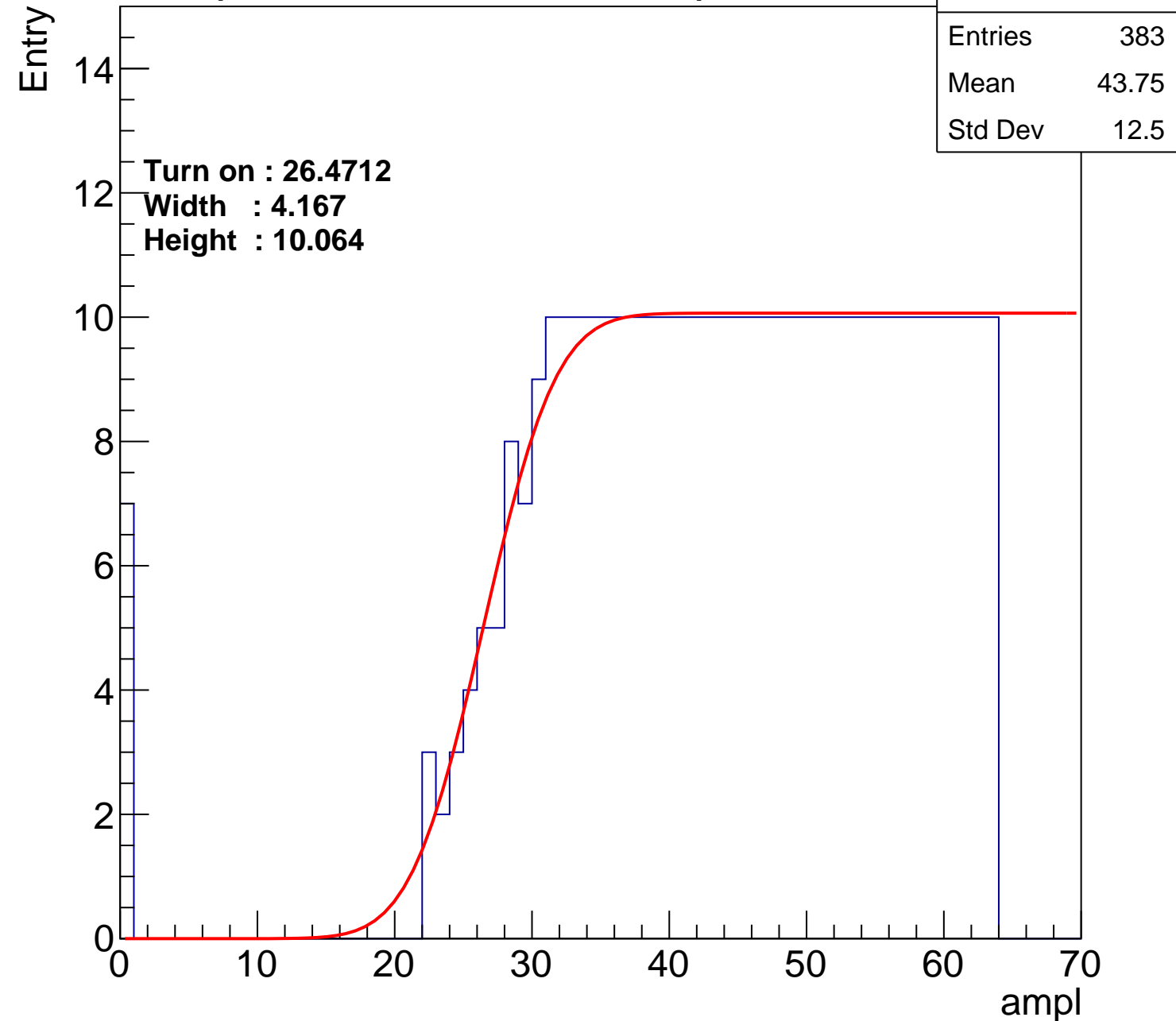
Width : 4.167

Height : 10.064

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch53

calib_packv5_042523_0143.root, FC#0, port D2

Entries	369
Mean	44.9
Std Dev	10.99

Turn on : 27.0417

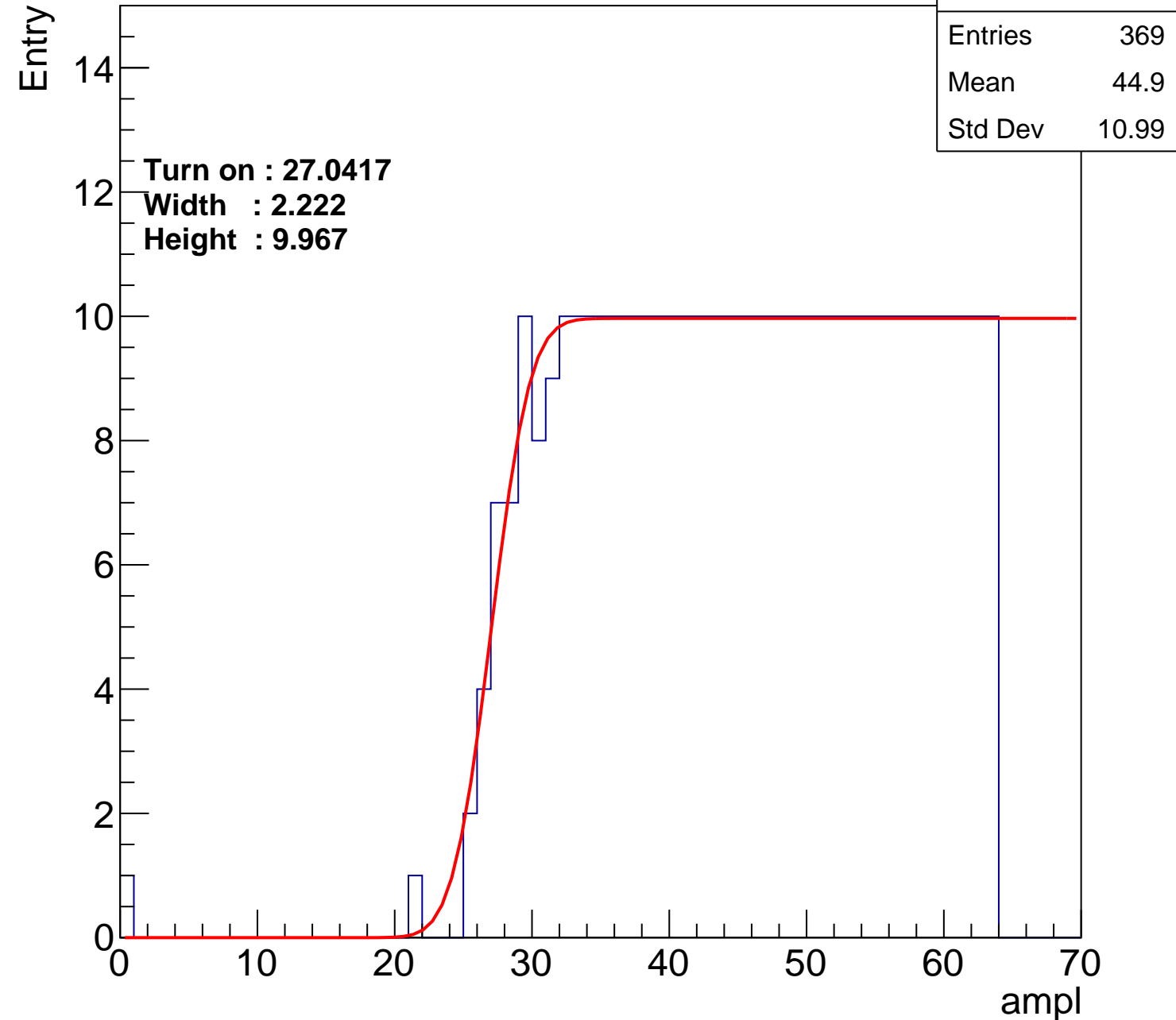
Width : 2.222

Height : 9.967

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch54

calib_packv5_042523_0143.root, FC#0, port D2

Entries	385
Mean	43.97
Std Dev	11.72

Turn on : 25.7085

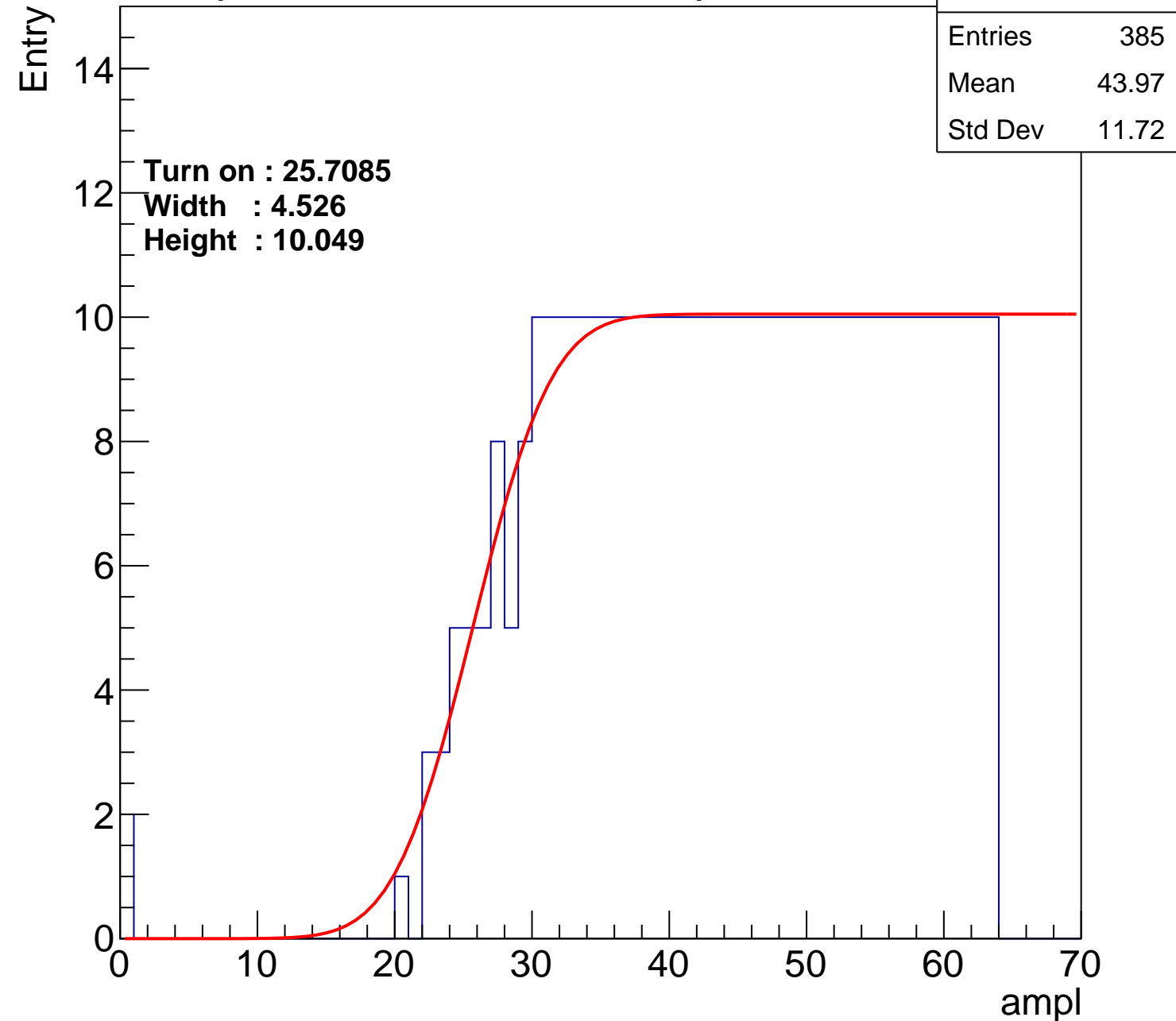
Width : 4.526

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch55

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.55
Std Dev	11.18

Turn on : 26.4138

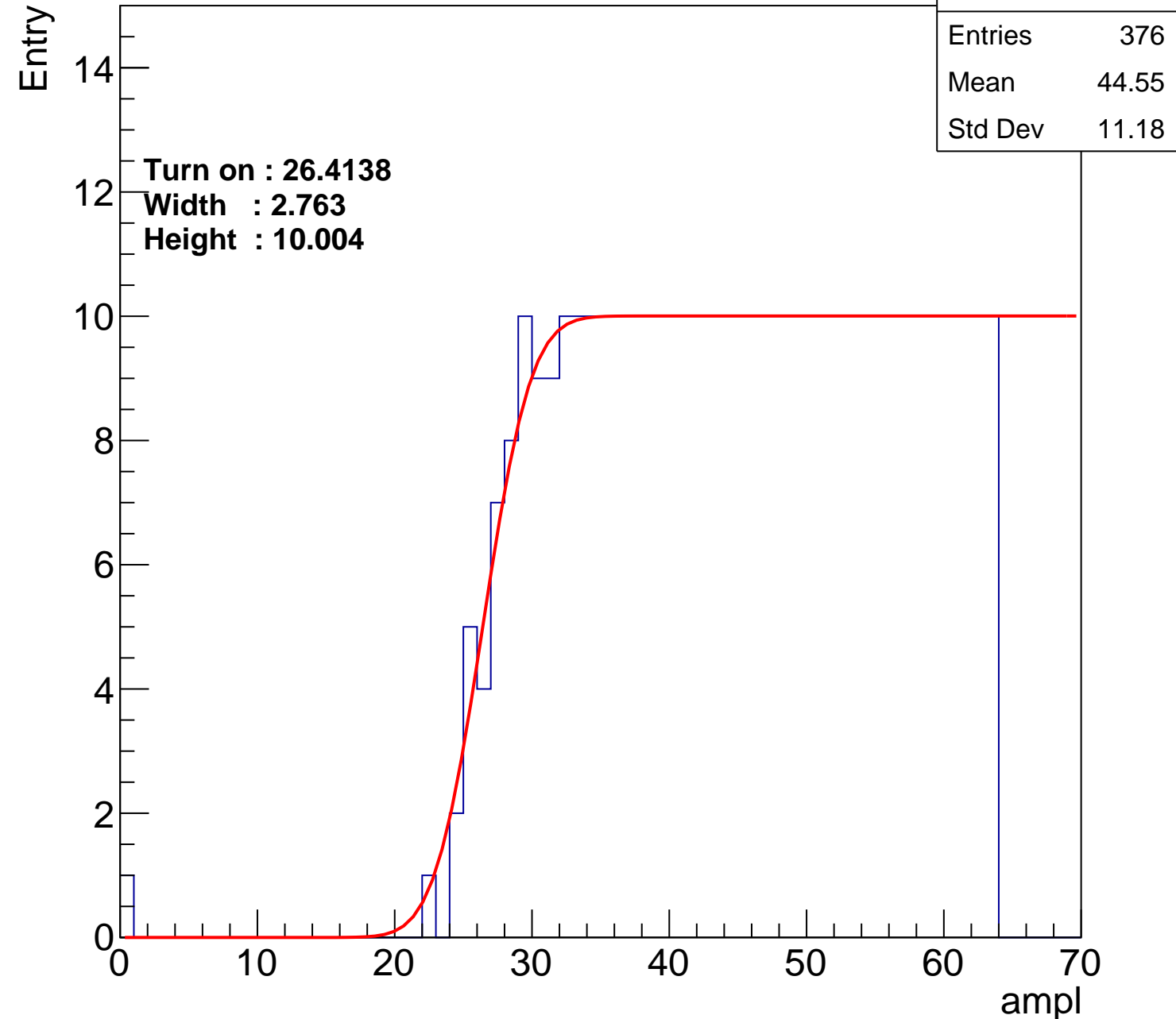
Width : 2.763

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch56

calib_packv5_042523_0143.root, FC#0, port D2

Entries	378
Mean	44.27
Std Dev	11.7

Turn on : 26.8607

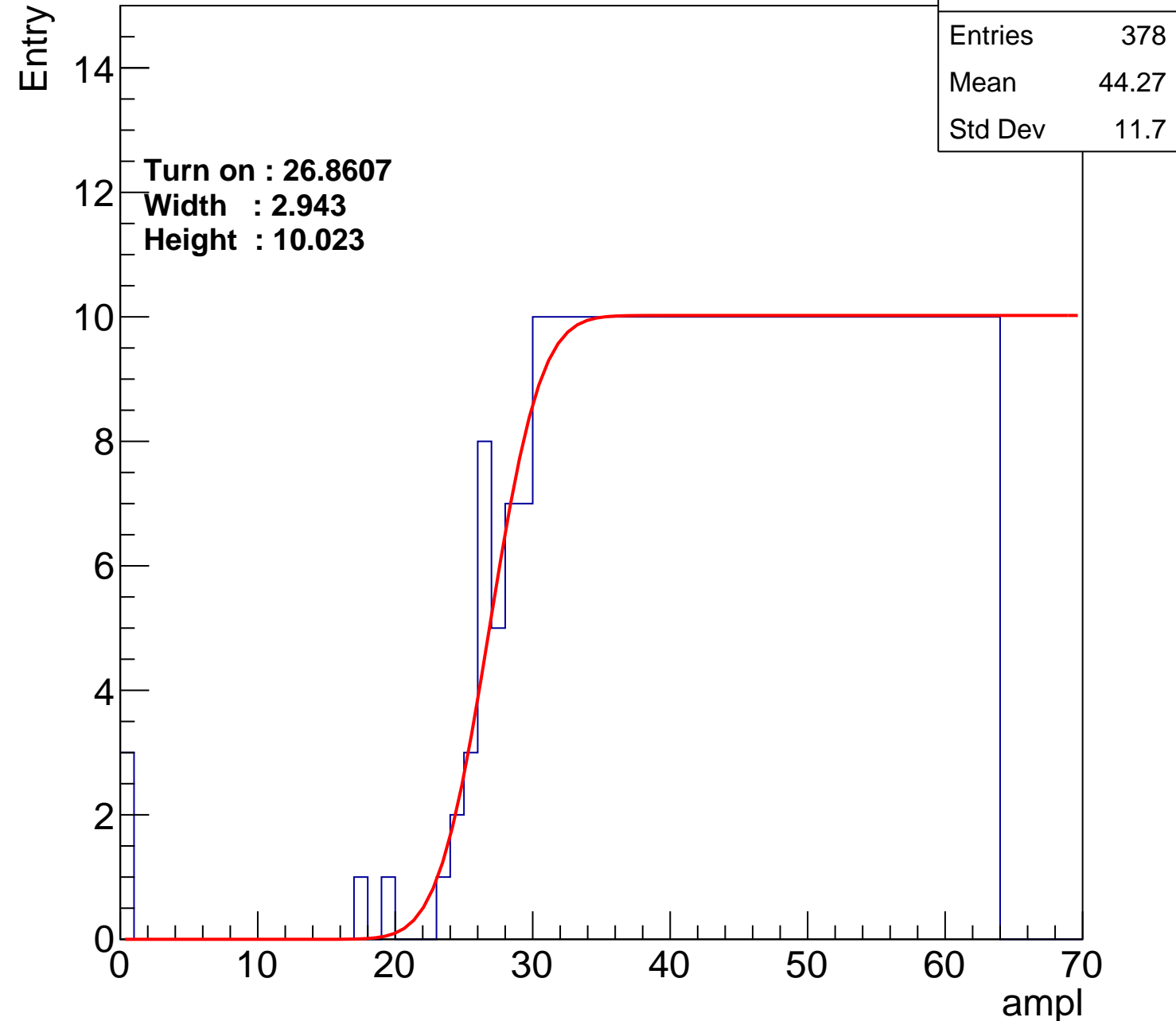
Width : 2.943

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch57

calib_packv5_042523_0143.root, FC#0, port D2

Entries	384
Mean	43.99
Std Dev	11.81

Turn on : 26.0737

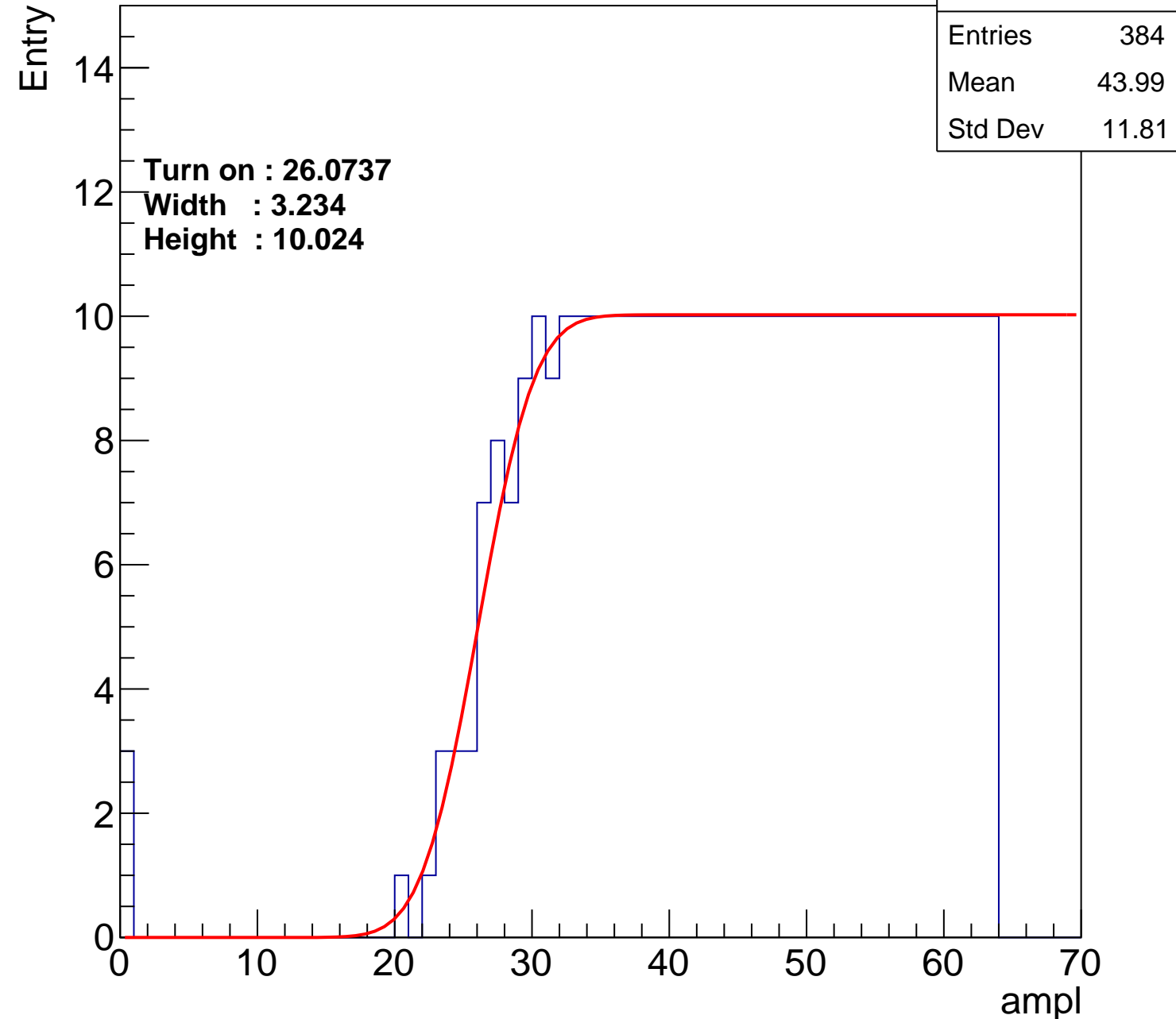
Width : 3.234

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch58

calib_packv5_042523_0143.root, FC#0, port D2

Entries	366
Mean	45.03
Std Dev	10.93

Turn on : 27.6398

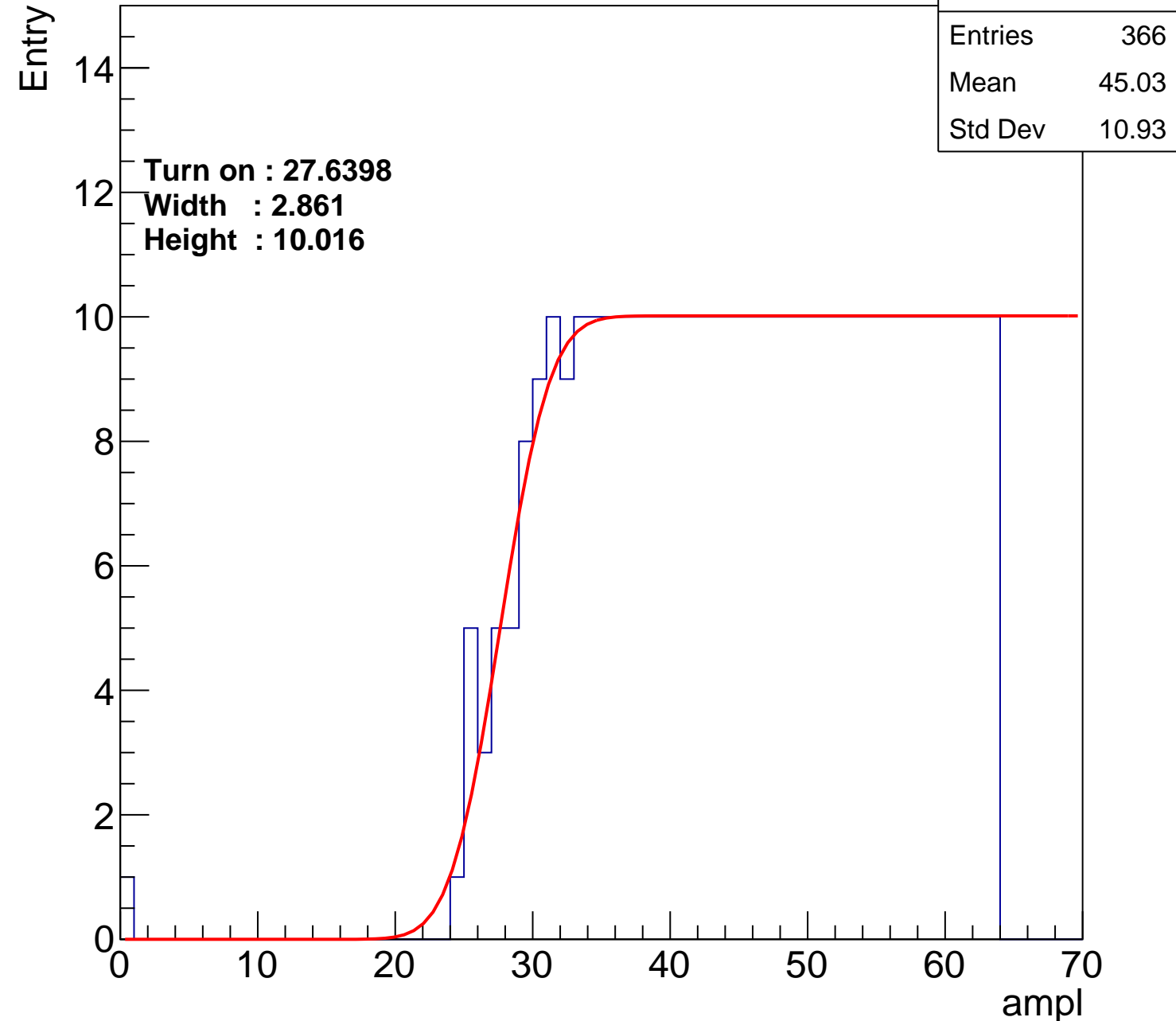
Width : 2.861

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch59

calib_packv5_042523_0143.root, FC#0, port D2

Entries	363
Mean	45.08
Std Dev	11.2

Turn on : 27.7639

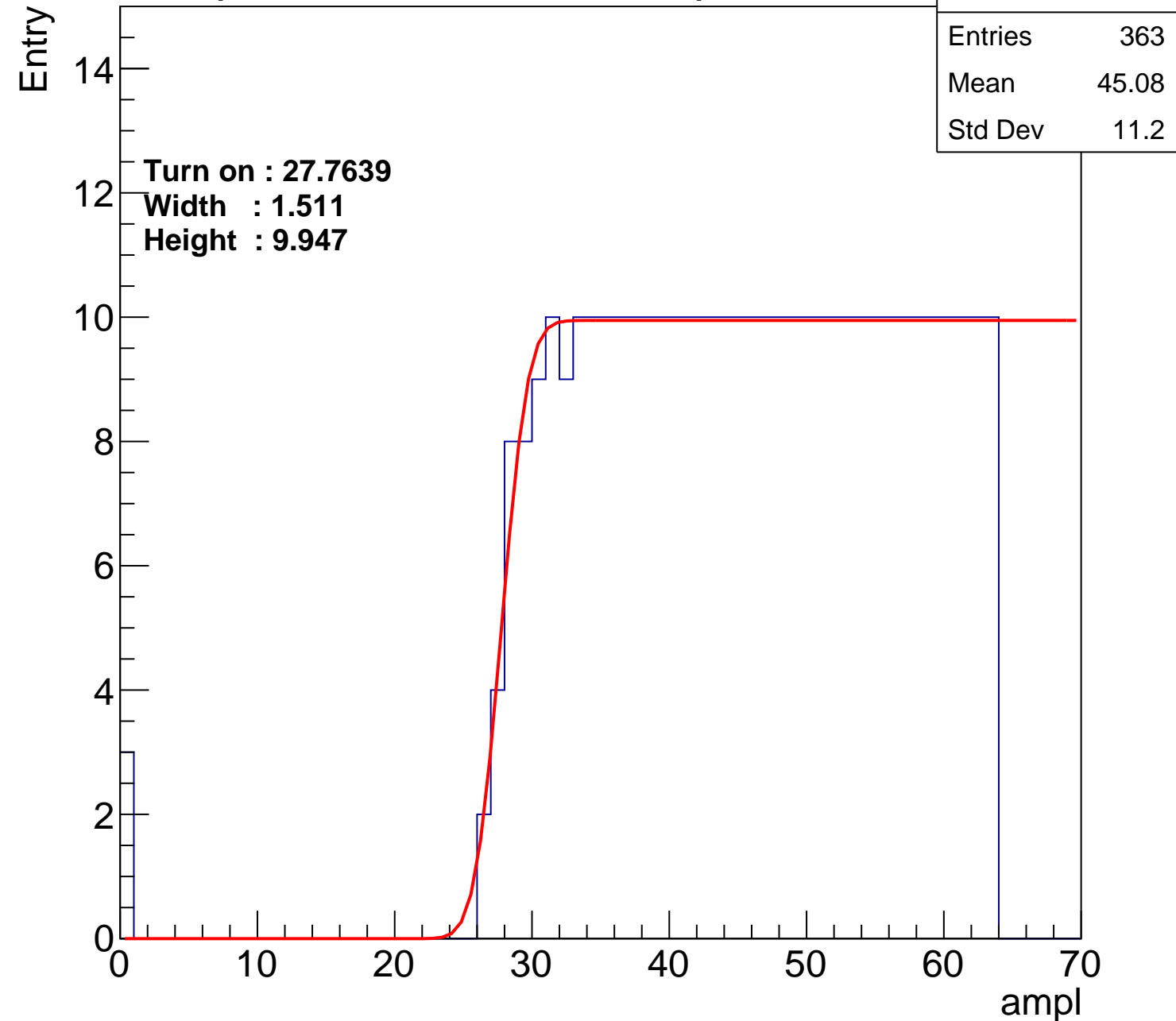
Width : 1.511

Height : 9.947

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch60

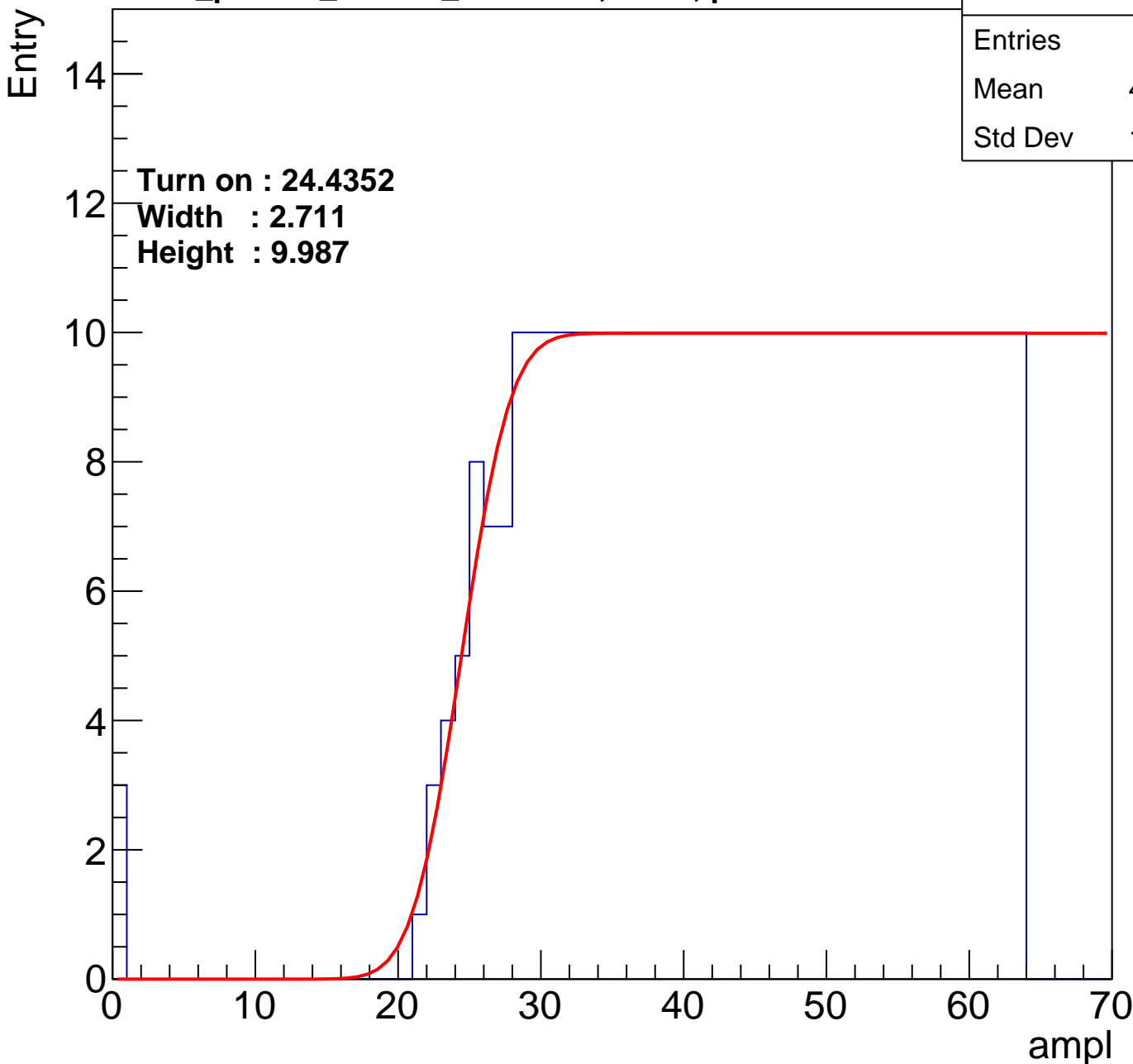
calib_packv5_042523_0143.root, FC#0, port D2

Entries	398
Mean	43.34
Std Dev	12.09

Turn on : 24.4352

Width : 2.711

Height : 9.987



B1L101S, U10-ch61

calib_packv5_042523_0143.root, FC#0, port D2

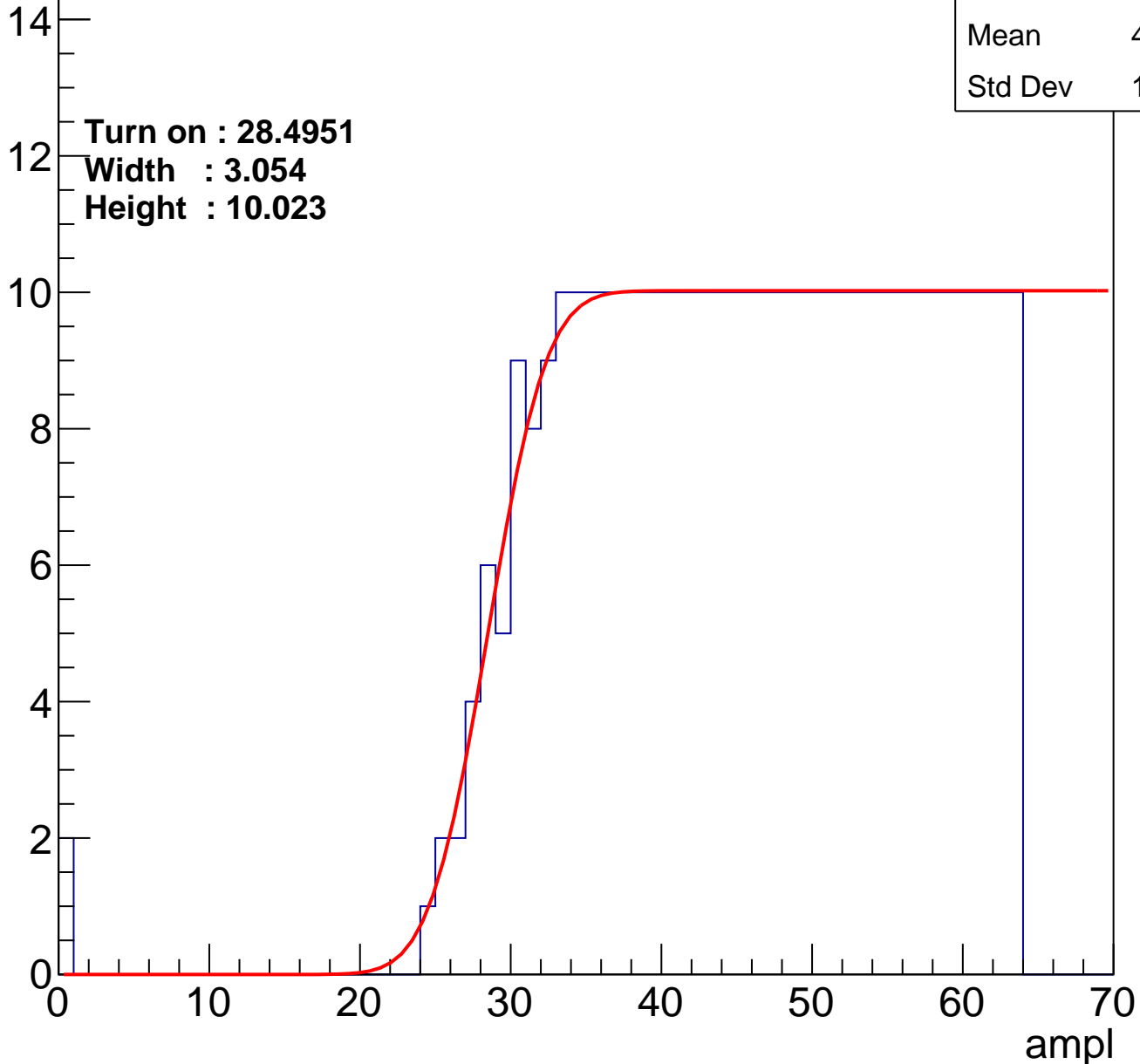
Entries	358
Mean	45.34
Std Dev	10.96

Turn on : 28.4951

Width : 3.054

Height : 10.023

Entry



B1L101S, U10-ch62

calib_packv5_042523_0143.root, FC#0, port D2

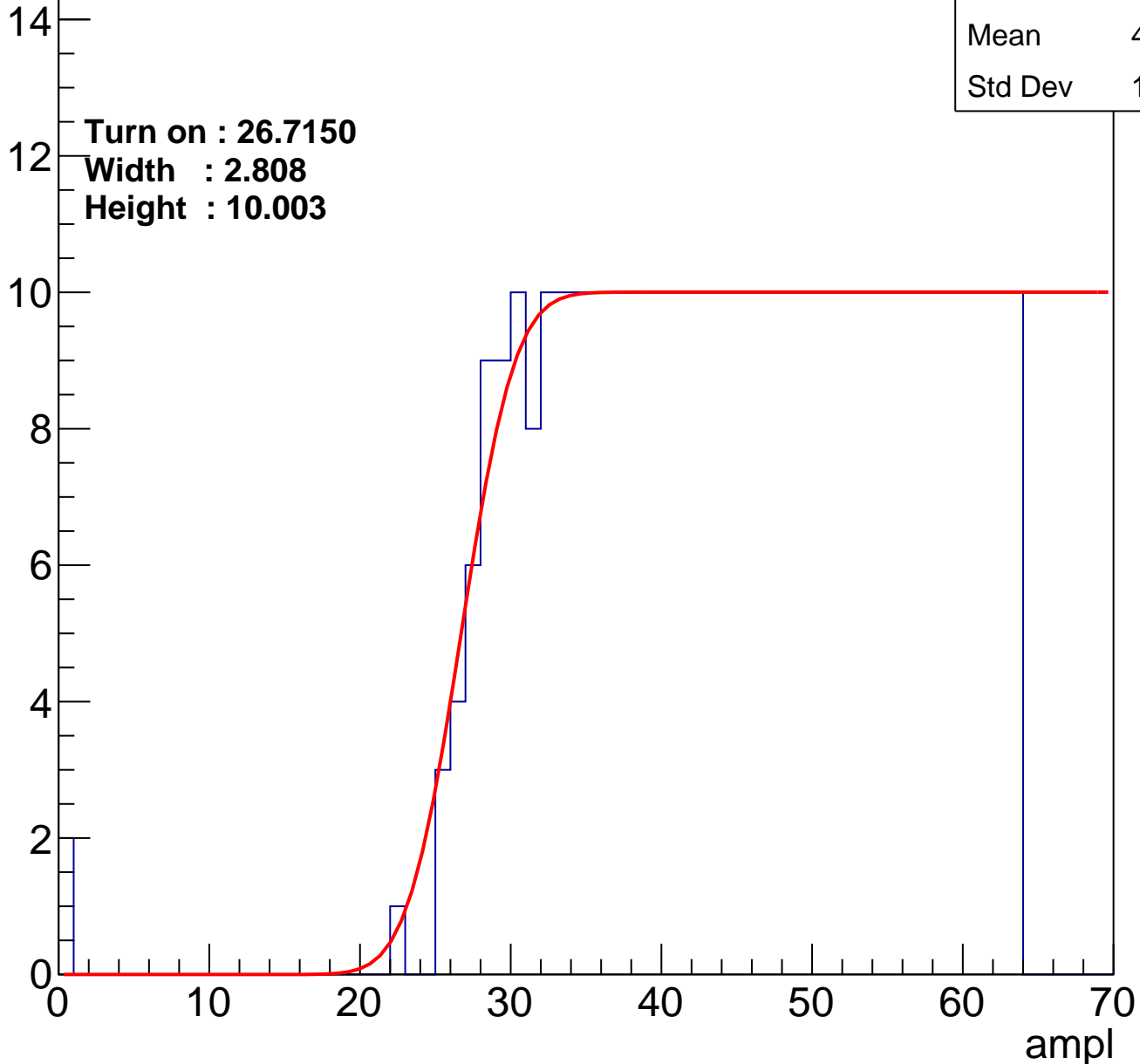
Entries	372
Mean	44.69
Std Dev	11.26

Turn on : 26.7150

Width : 2.808

Height : 10.003

Entry



B1L101S, U10-ch63

calib_packv5_042523_0143.root, FC#0, port D2

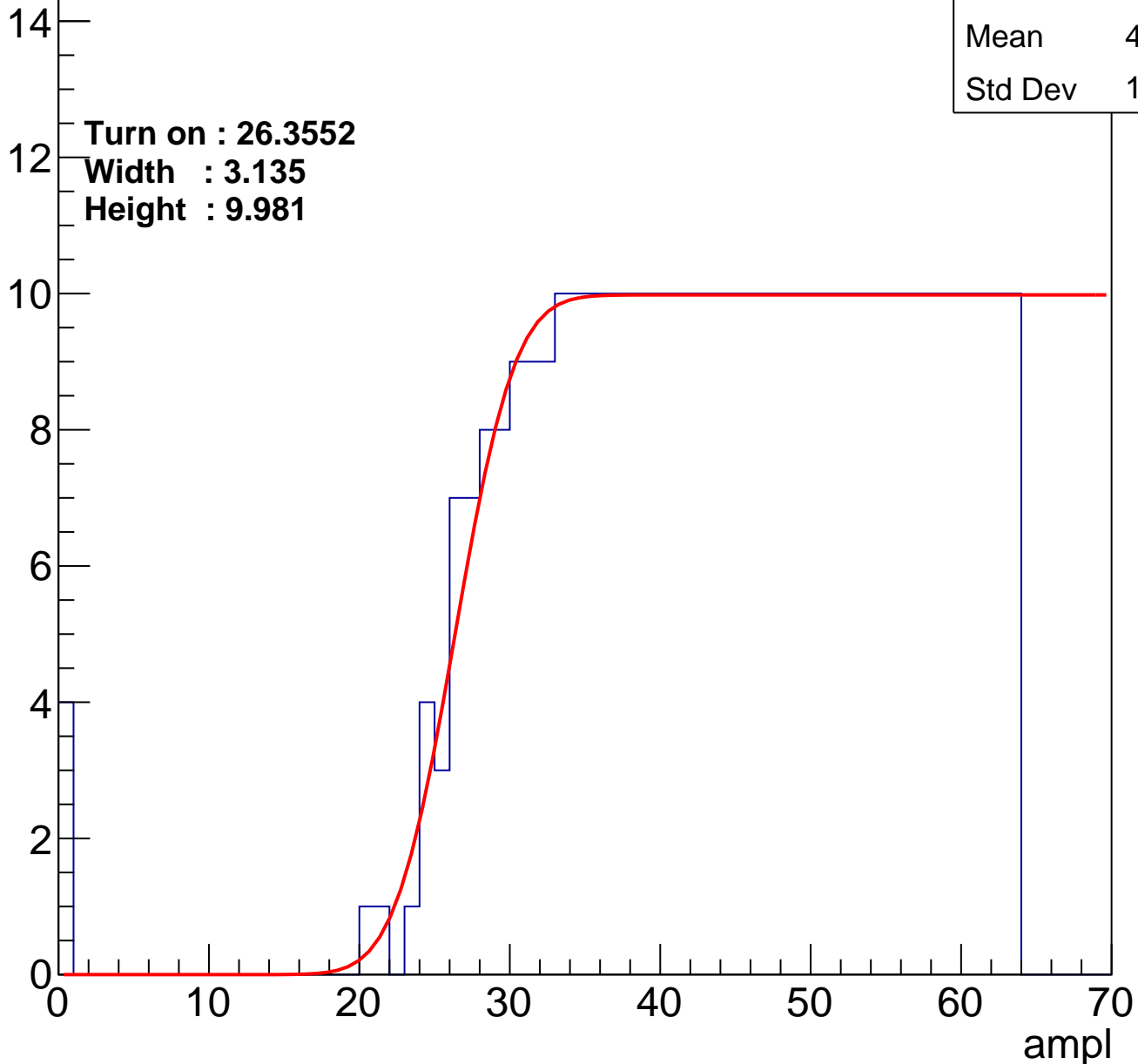
Entries	381
Mean	44.04
Std Dev	11.95

Turn on : 26.3552

Width : 3.135

Height : 9.981

Entry



B1L101S, U10-ch64

calib_packv5_042523_0143.root, FC#0, port D2

Entries	380
Mean	44.38
Std Dev	11.25

Turn on : 26.3564

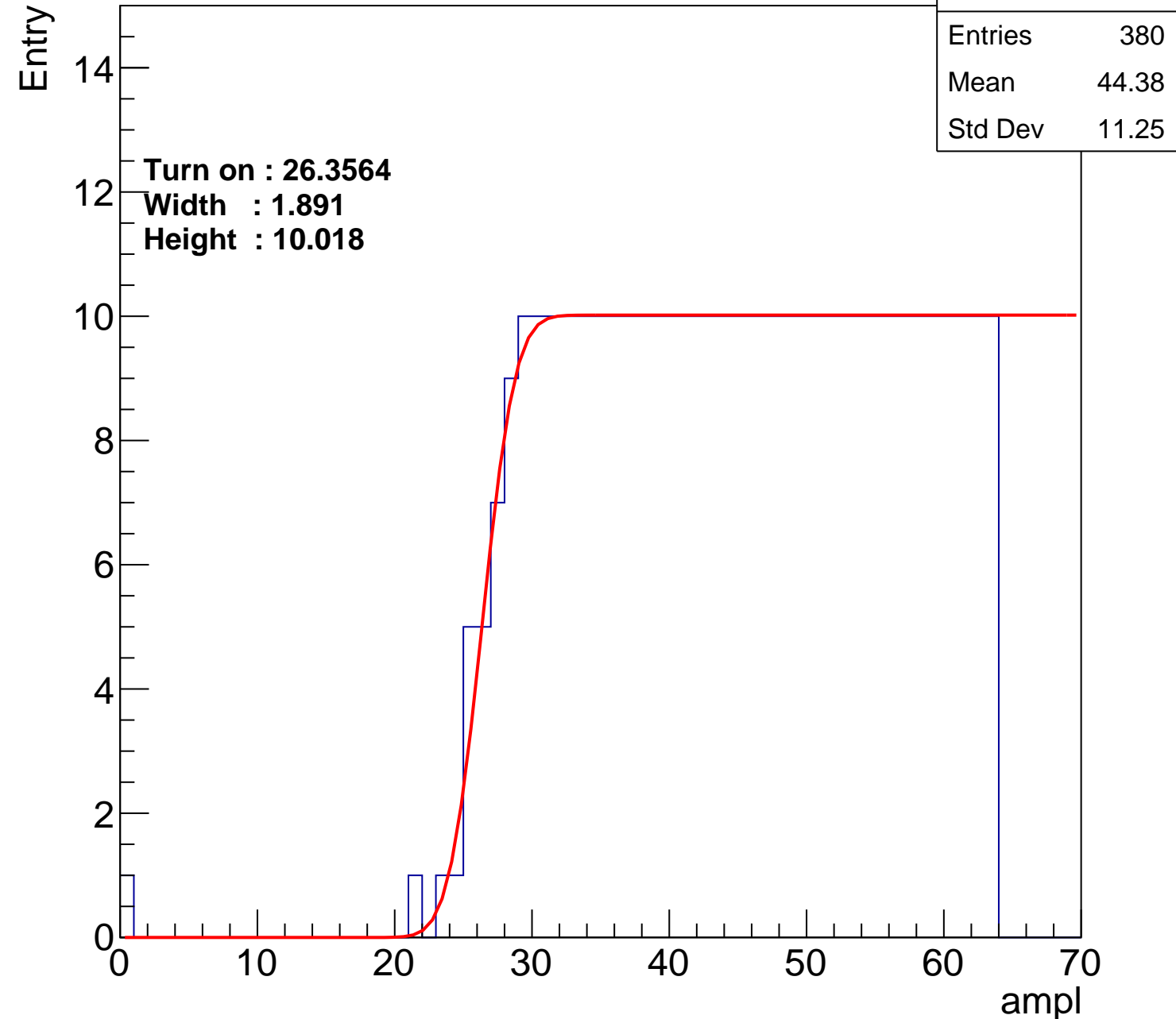
Width : 1.891

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch65

calib_packv5_042523_0143.root, FC#0, port D2

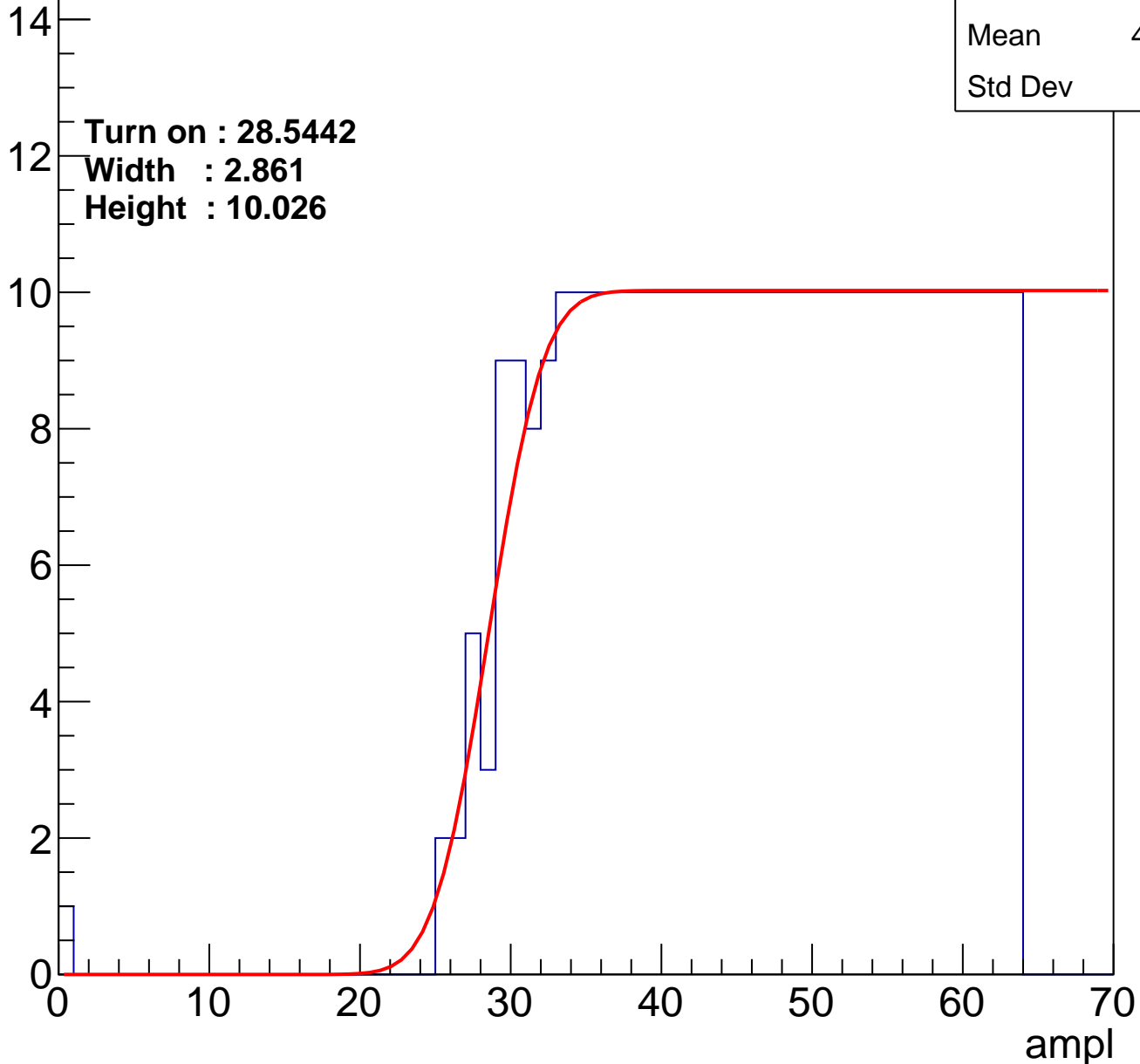
Entries	358
Mean	45.44
Std Dev	10.7

Turn on : 28.5442

Width : 2.861

Height : 10.026

Entry



B1L101S, U10-ch66

calib_packv5_042523_0143.root, FC#0, port D2

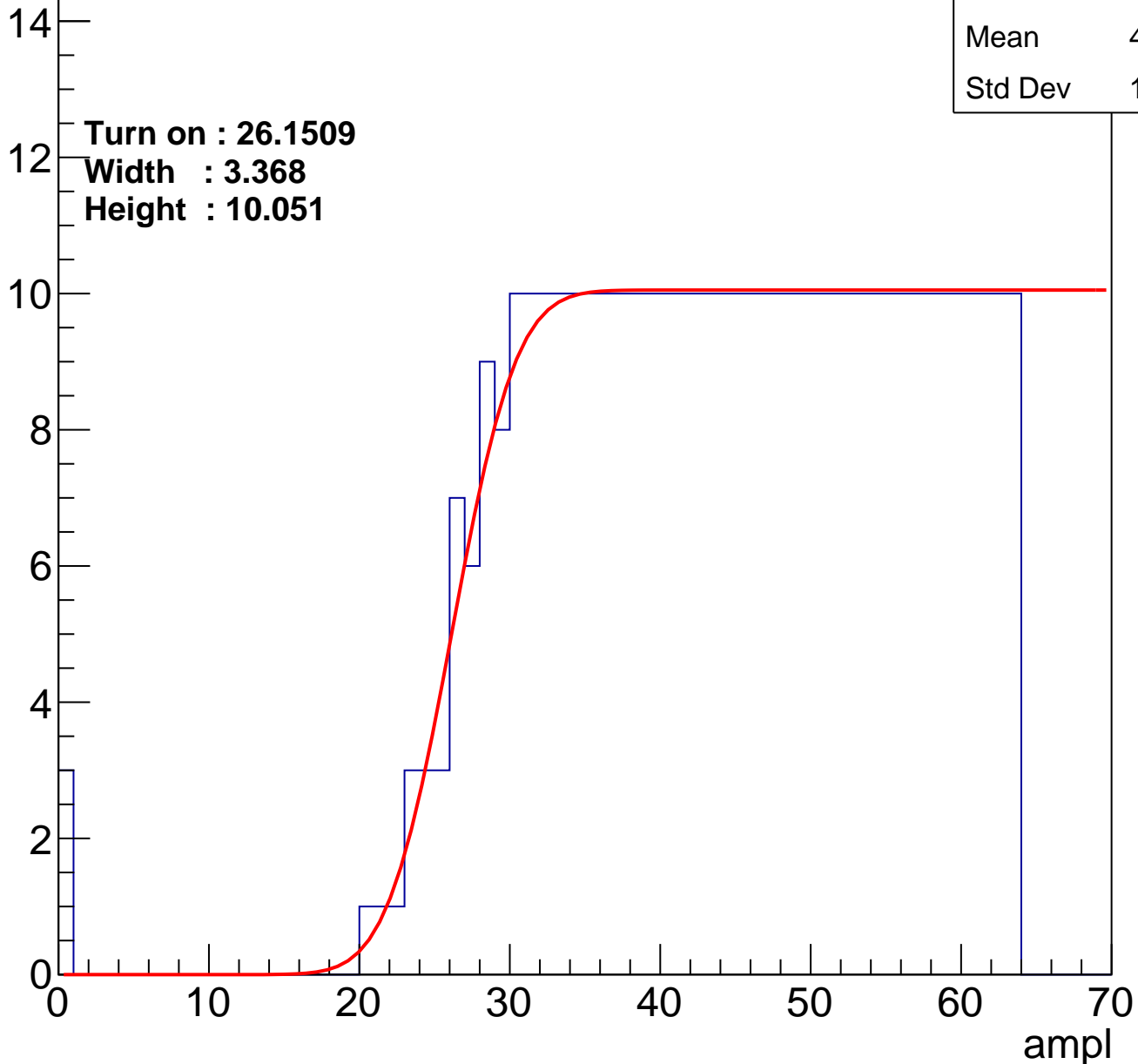
Entries	385
Mean	43.94
Std Dev	11.84

Turn on : 26.1509

Width : 3.368

Height : 10.051

Entry



B1L101S, U10-ch67

calib_packv5_042523_0143.root, FC#0, port D2

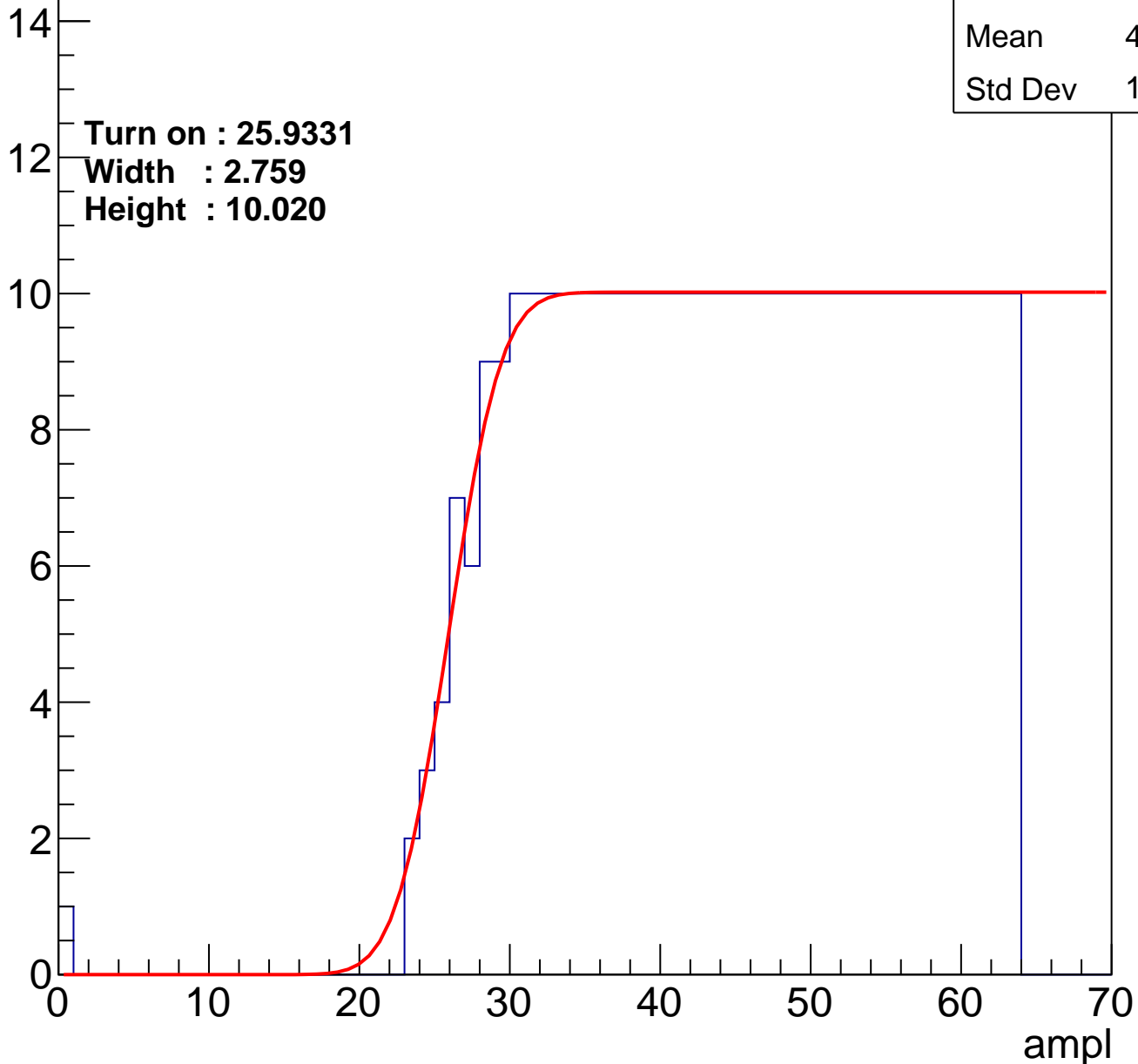
Entries	381
Mean	44.32
Std Dev	11.29

Turn on : 25.9331

Width : 2.759

Height : 10.020

Entry



B1L101S, U10-ch68

calib_packv5_042523_0143.root, FC#0, port D2

Entries	383
Mean	44.1
Std Dev	11.63

Turn on : 26.1944

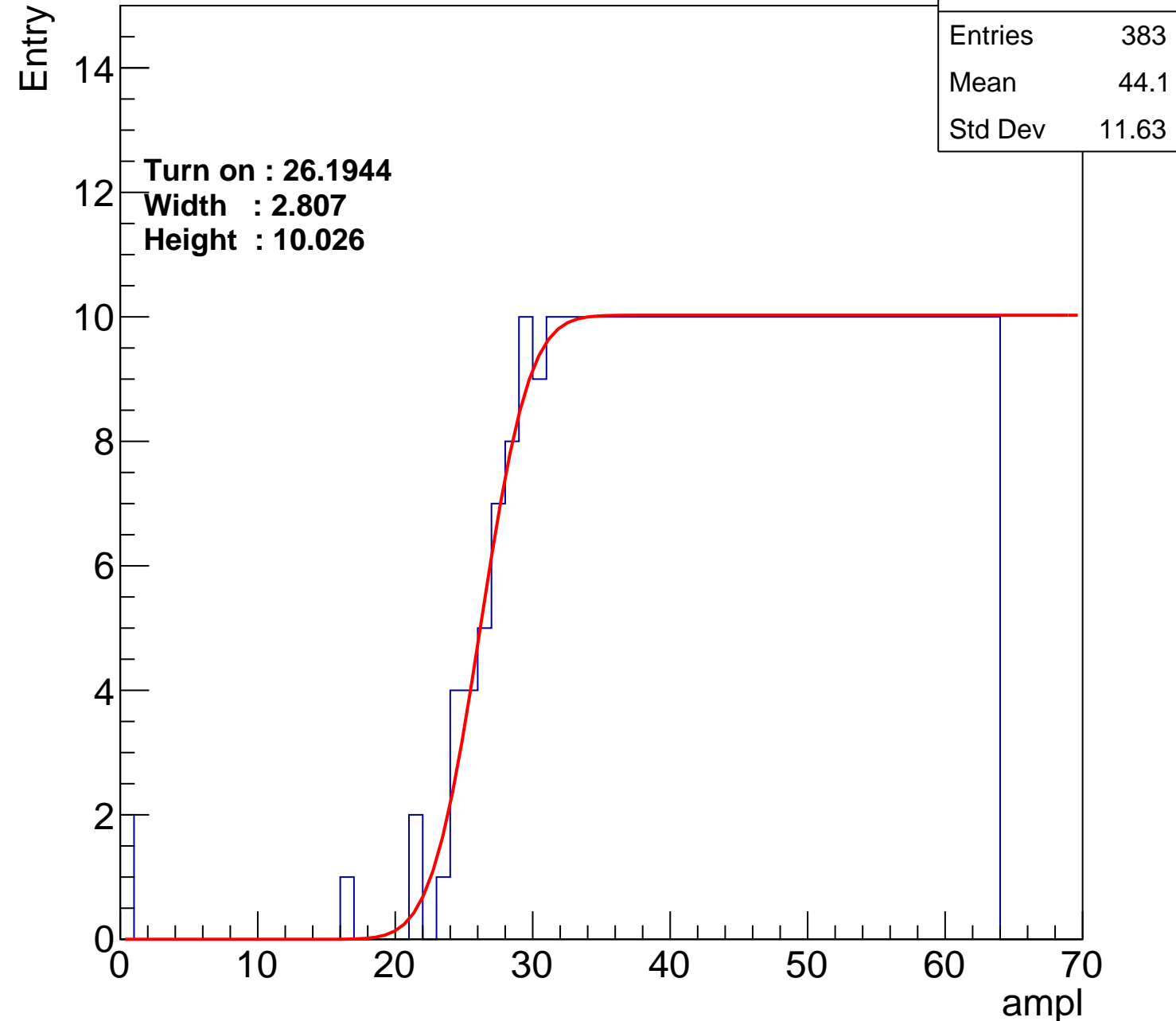
Width : 2.807

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch69

calib_packv5_042523_0143.root, FC#0, port D2

Entries	371
Mean	44.74
Std Dev	11.24

Turn on : 27.3892

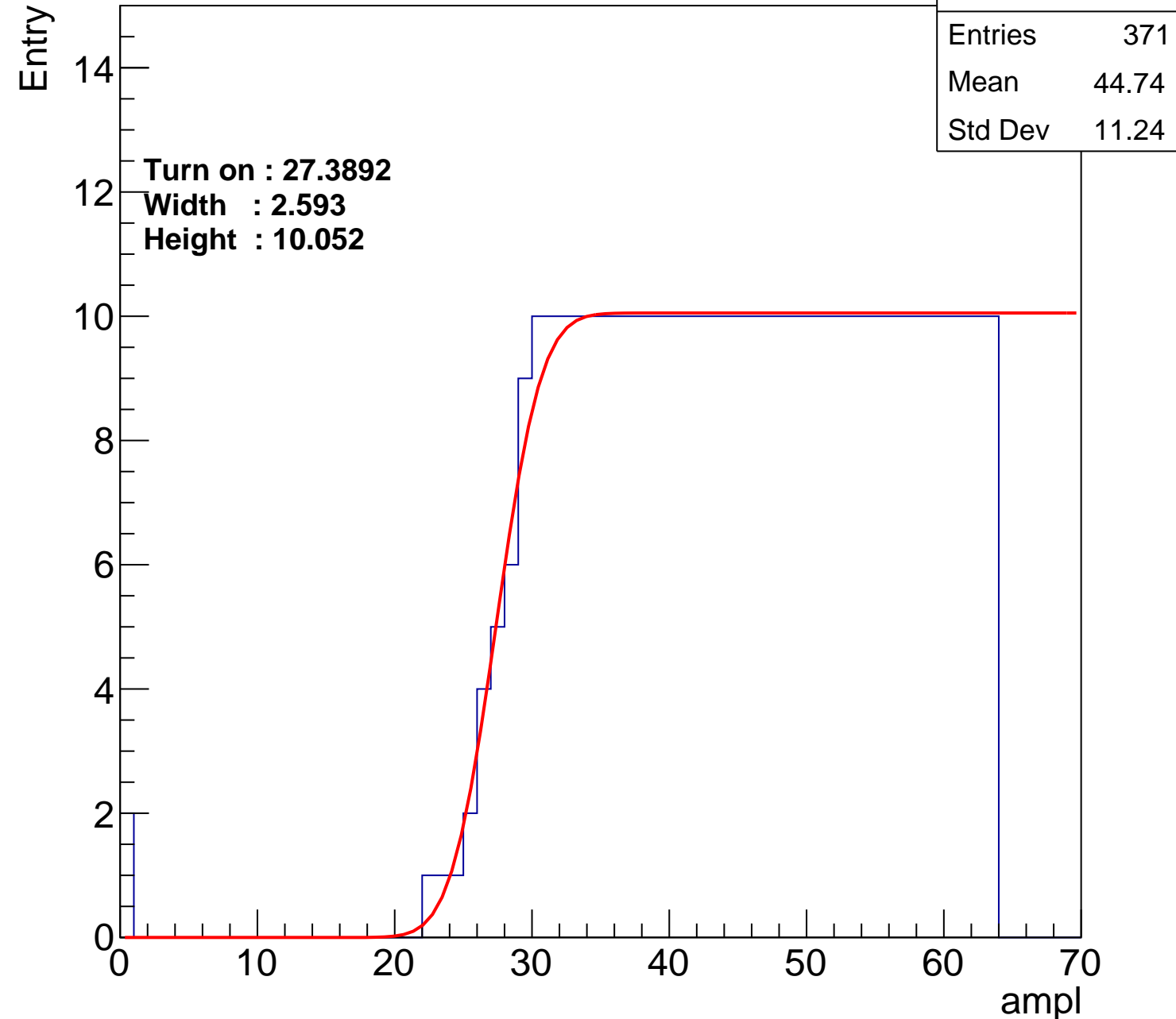
Width : 2.593

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch70

calib_packv5_042523_0143.root, FC#0, port D2

Entries	382
Mean	44.09
Std Dev	11.76

Turn on : 26.4500

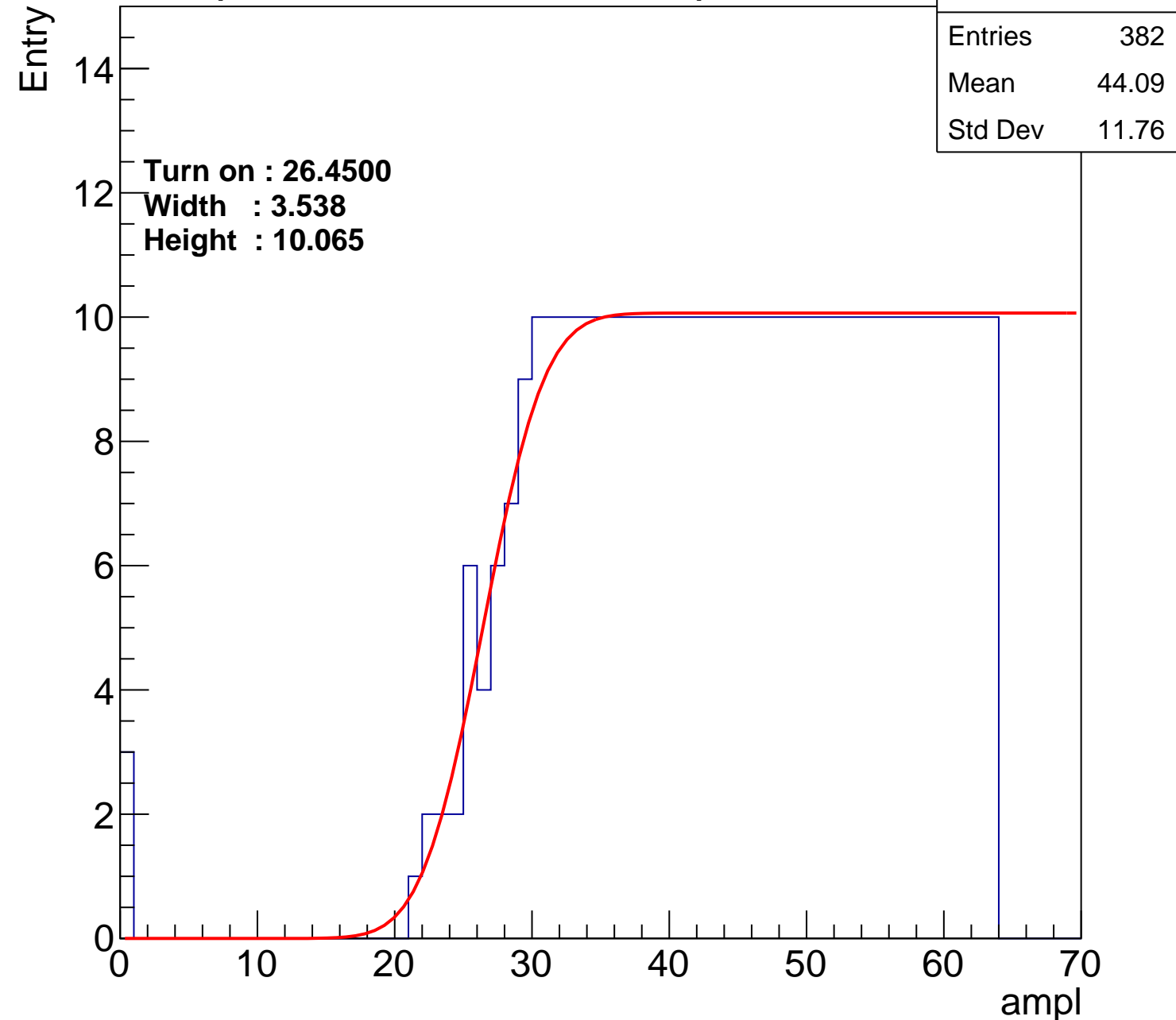
Width : 3.538

Height : 10.065

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch71

calib_packv5_042523_0143.root, FC#0, port D2

Entries	368
Mean	44.85
Std Dev	11.21

Turn on : 27.7460

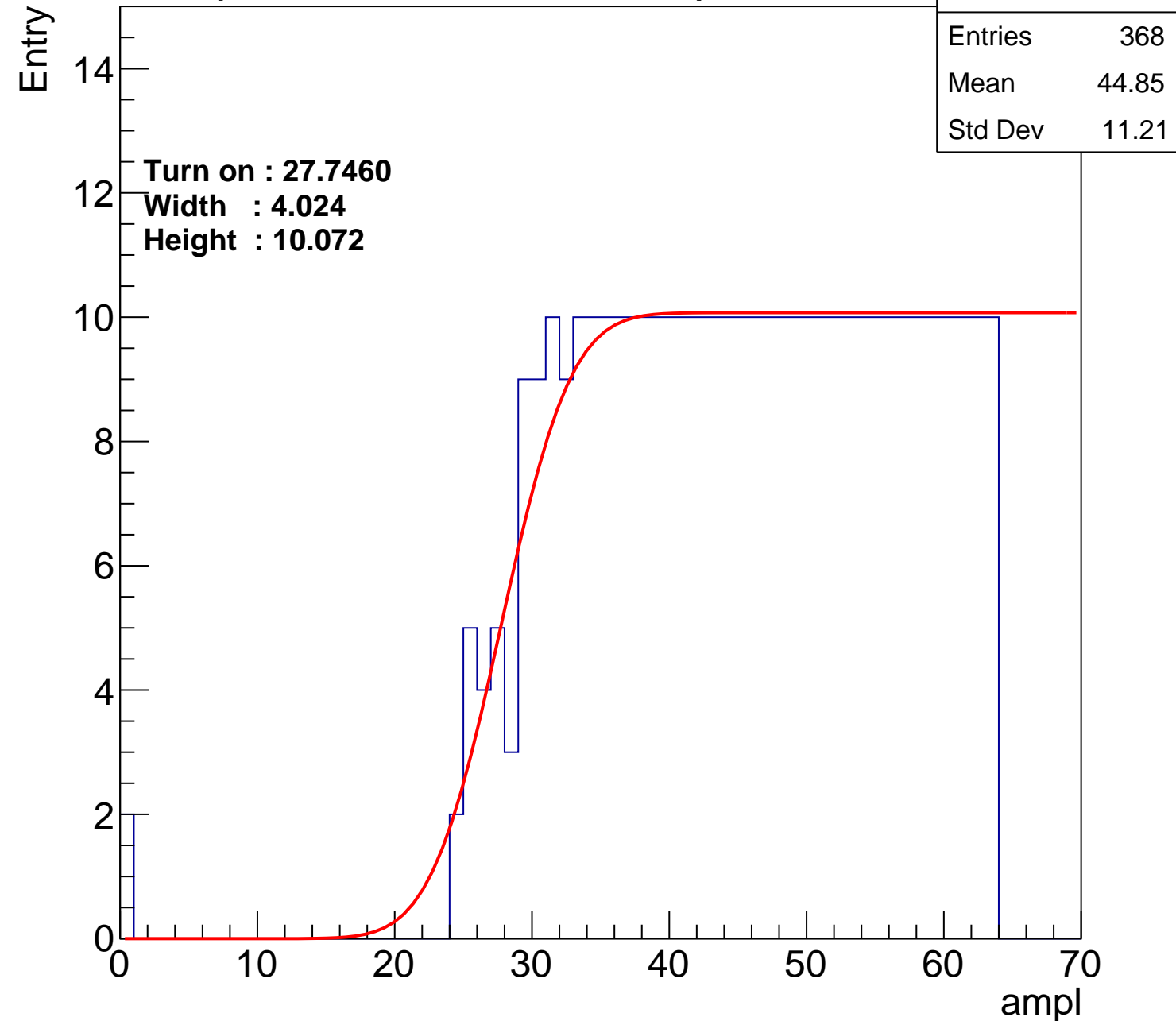
Width : 4.024

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch72

calib_packv5_042523_0143.root, FC#0, port D2

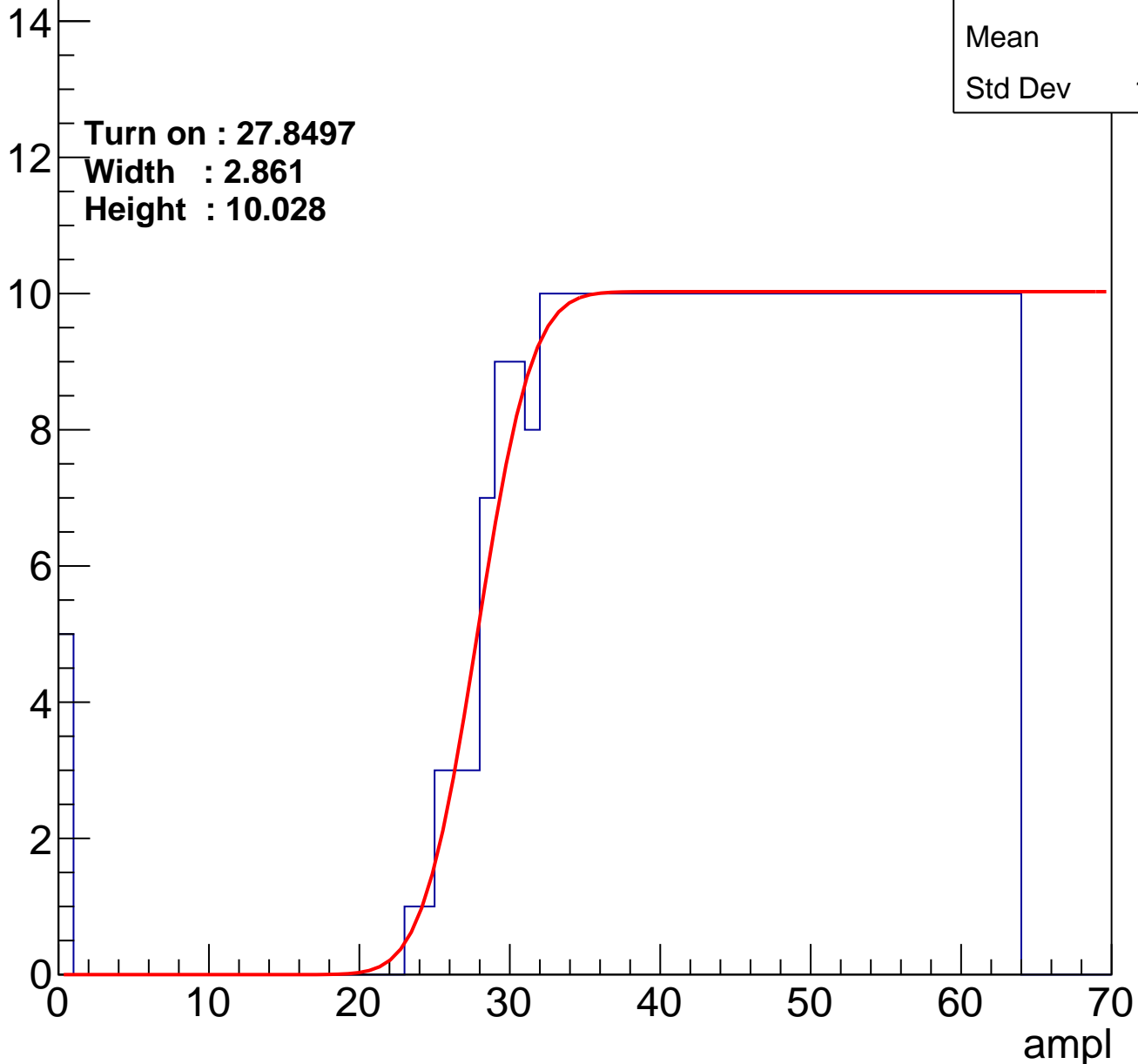
Entries	369
Mean	44.6
Std Dev	11.81

Turn on : 27.8497

Width : 2.861

Height : 10.028

Entry



B1L101S, U10-ch73

calib_packv5_042523_0143.root, FC#0, port D2

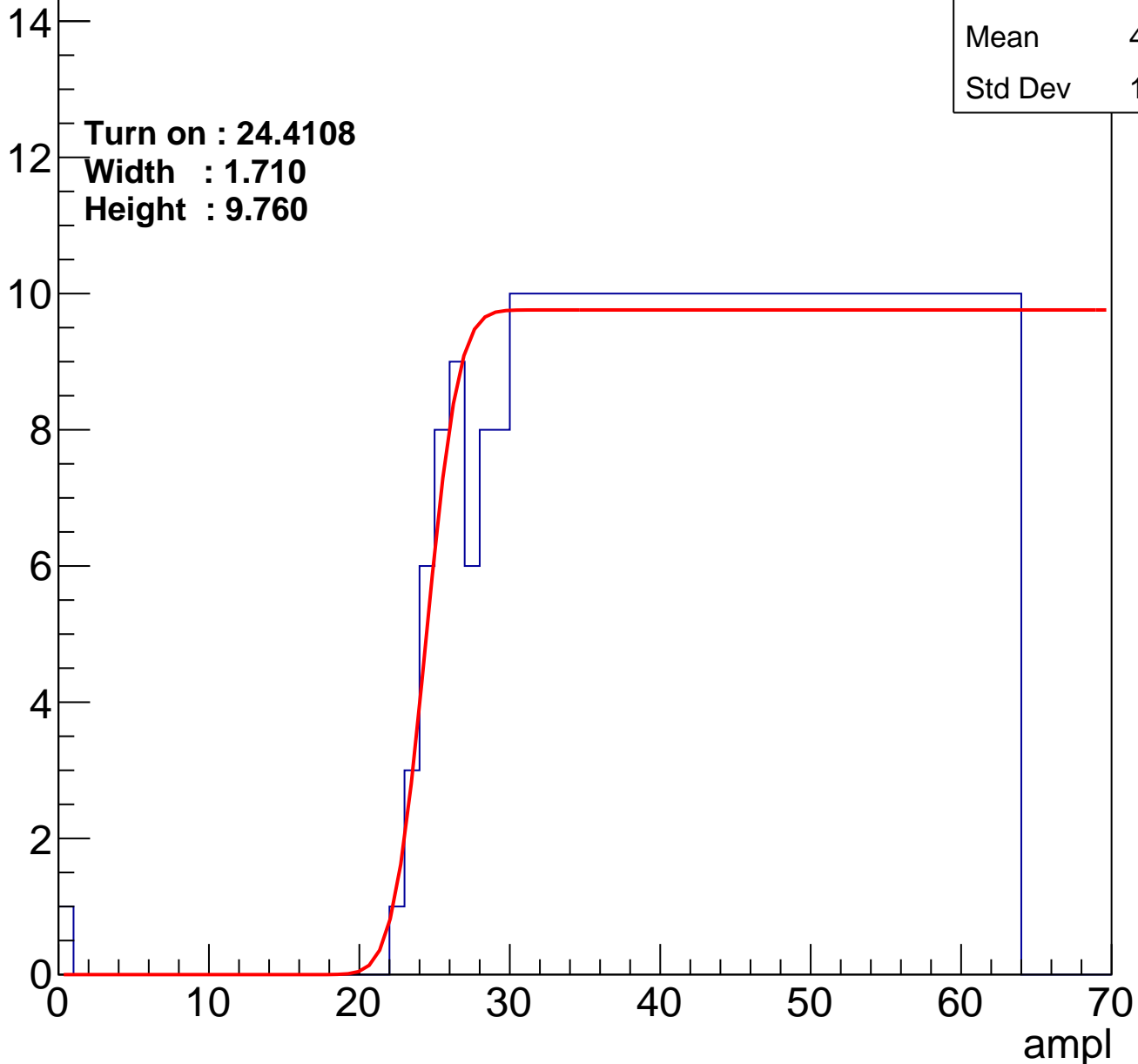
Entries	390
Mean	43.84
Std Dev	11.59

Turn on : 24.4108

Width : 1.710

Height : 9.760

Entry



B1L101S, U10-ch74

calib_packv5_042523_0143.root, FC#0, port D2

Entries	381
Mean	44.06
Std Dev	11.93

Turn on : 26.5069

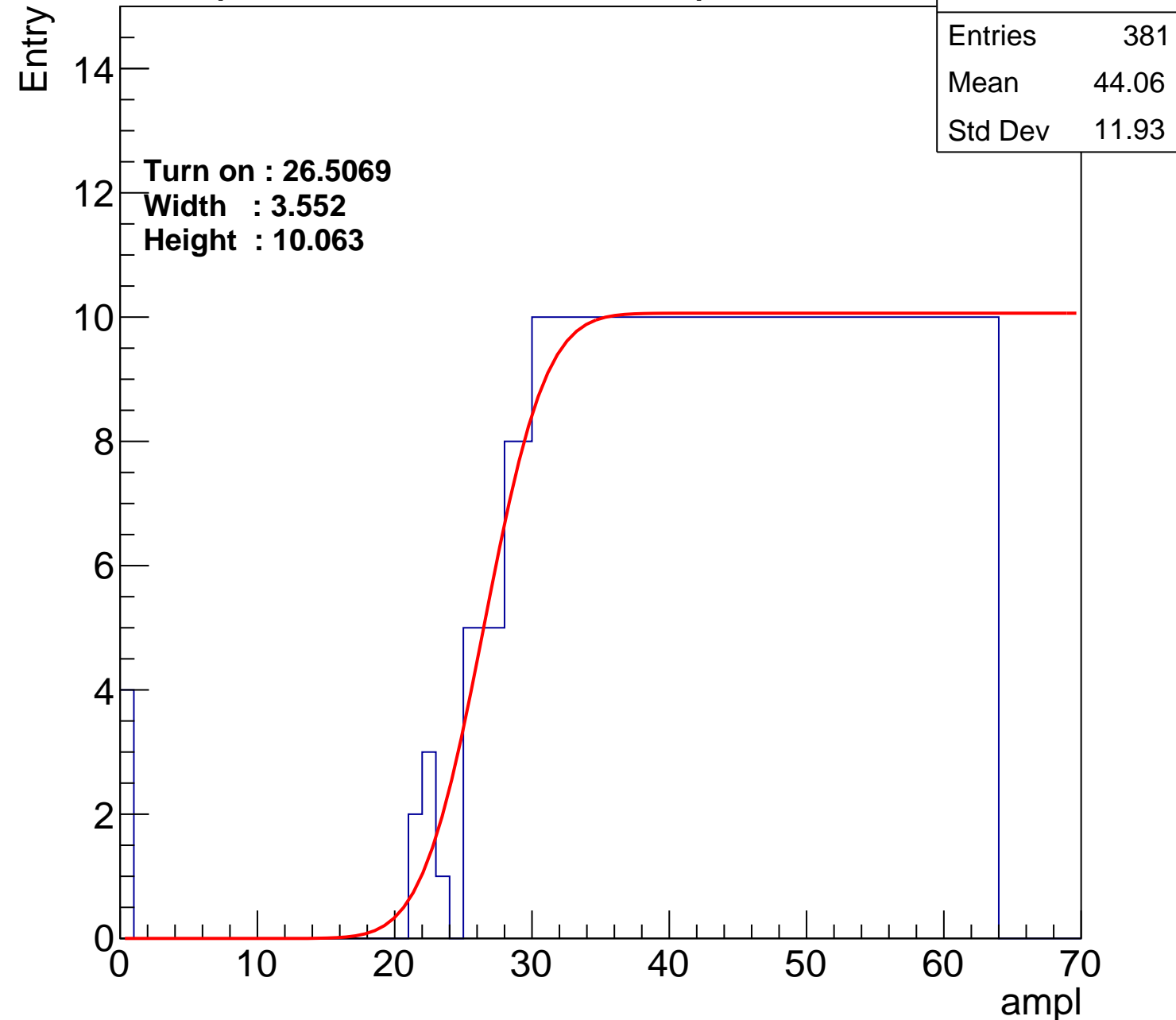
Width : 3.552

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch75

calib_packv5_042523_0143.root, FC#0, port D2

Entries	384
Mean	44.02
Std Dev	11.76

Turn on : 26.1069

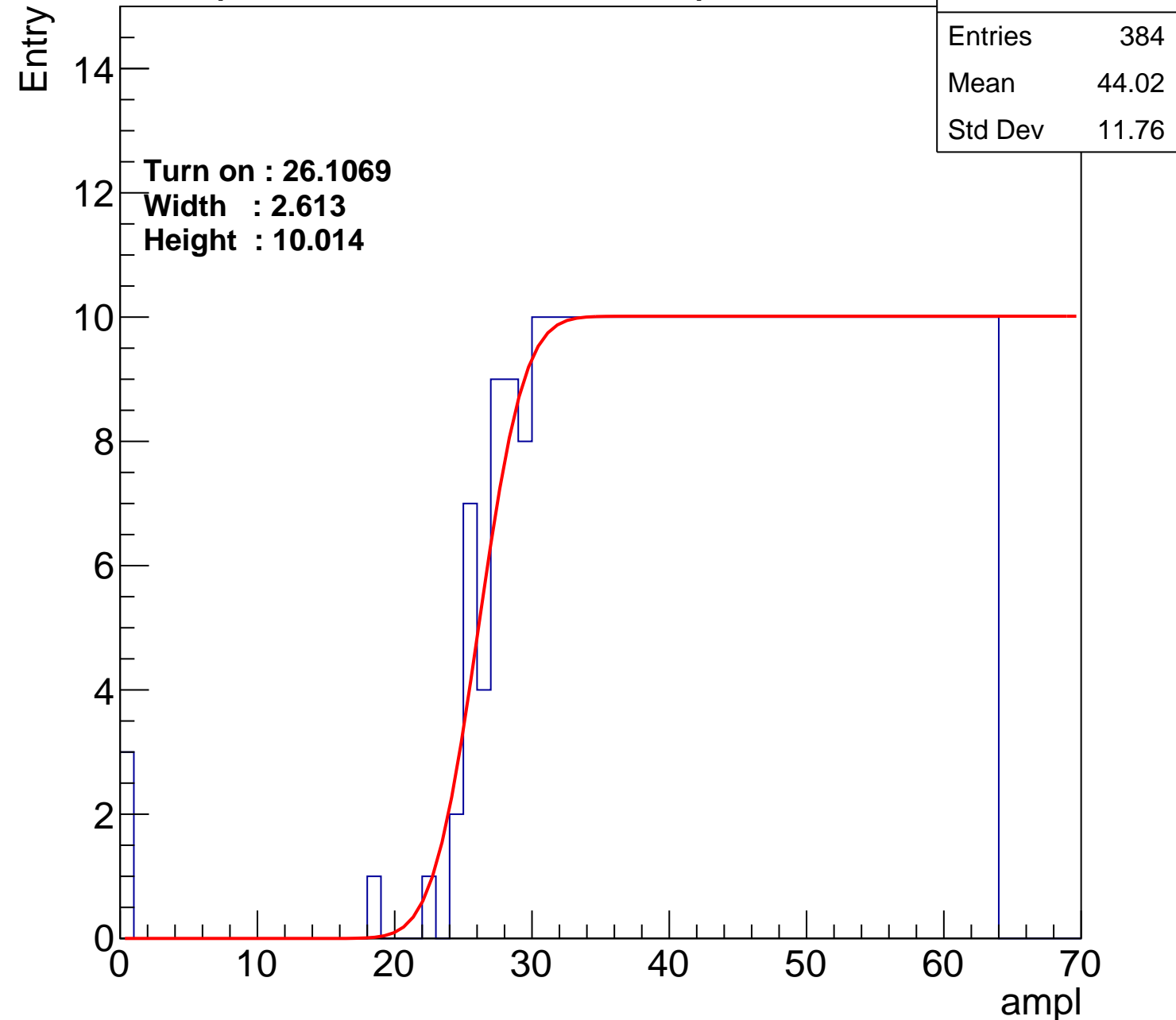
Width : 2.613

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch76

calib_packv5_042523_0143.root, FC#0, port D2

Entries	364
Mean	44.97
Std Dev	11.33

Turn on : 28.4820

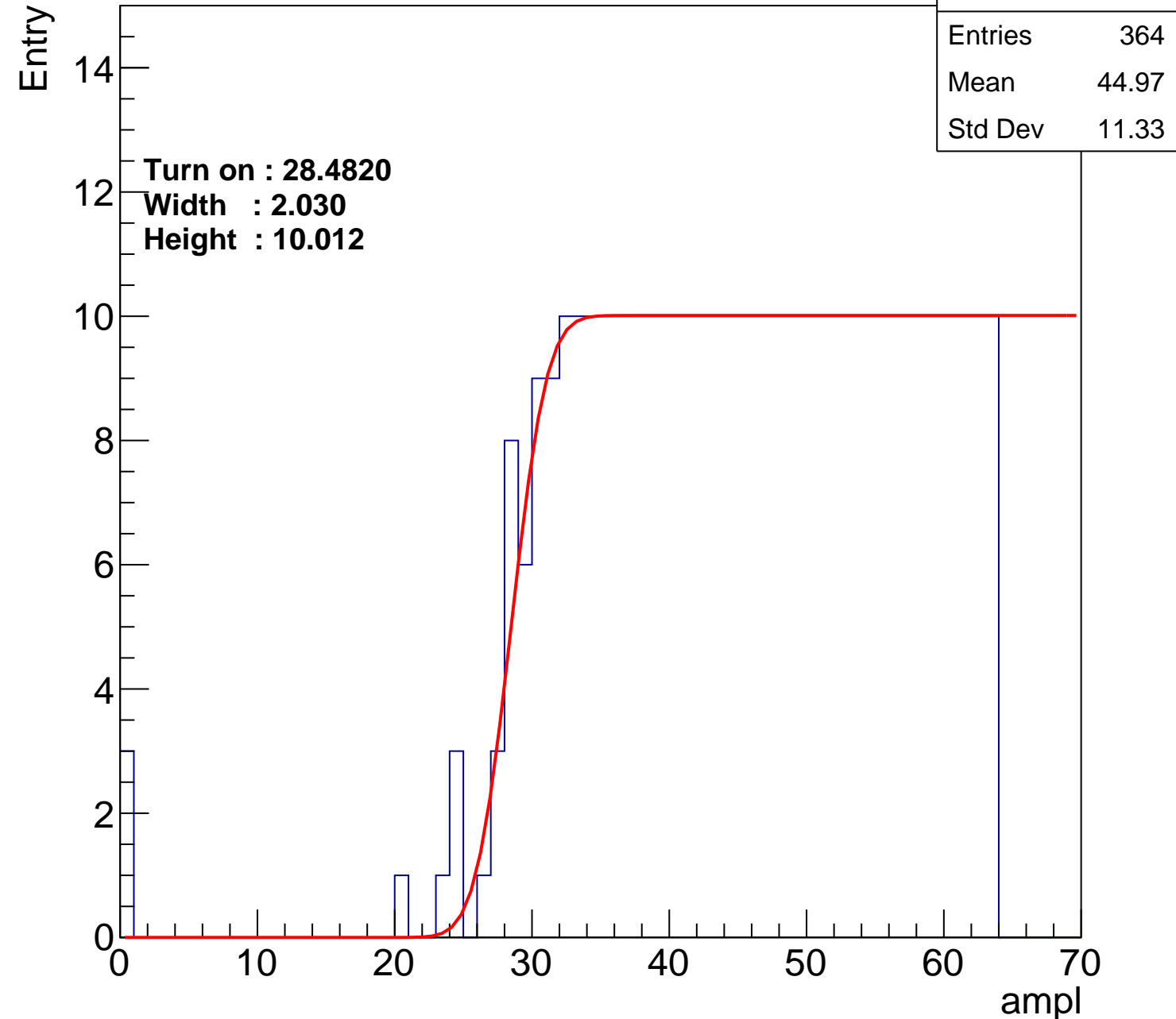
Width : 2.030

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch77

calib_packv5_042523_0143.root, FC#0, port D2

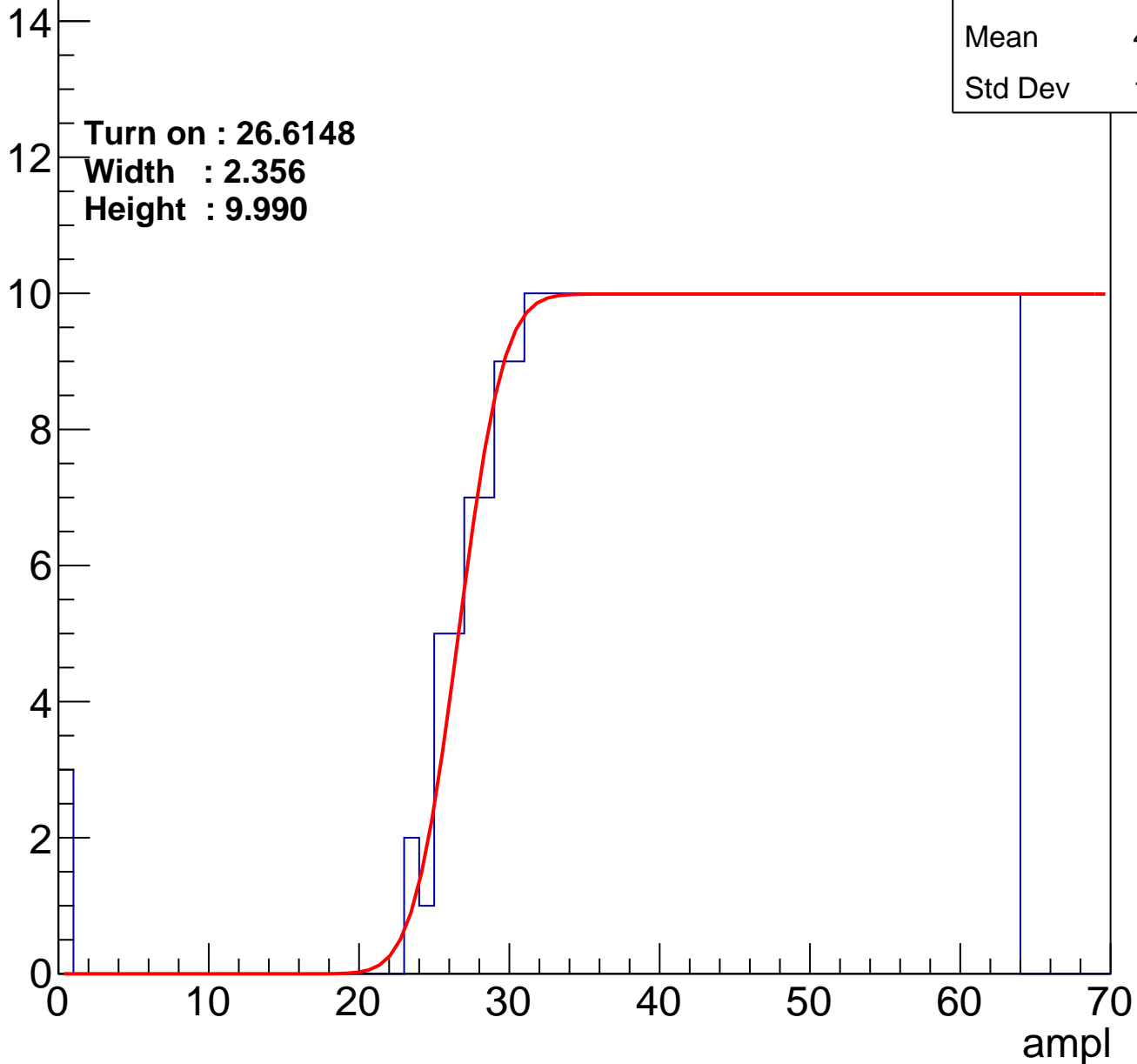
Entries	378
Mean	44.31
Std Dev	11.61

Turn on : 26.6148

Width : 2.356

Height : 9.990

Entry



B1L101S, U10-ch78

calib_packv5_042523_0143.root, FC#0, port D2

Entries	373
Mean	44.69
Std Dev	11.12

Turn on : 27.1092

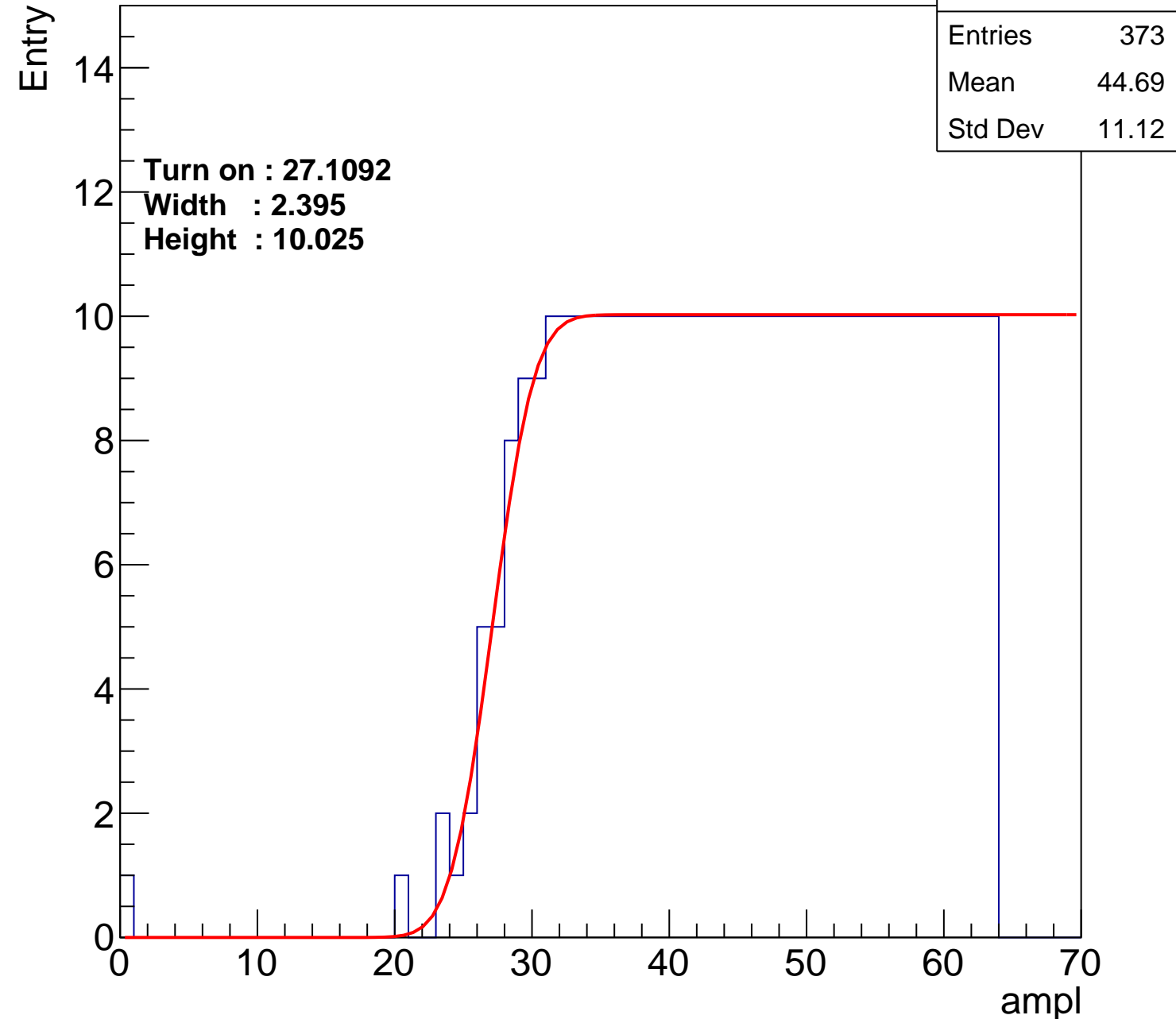
Width : 2.395

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch79

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.32
Std Dev	11.79

Turn on : 27.1627

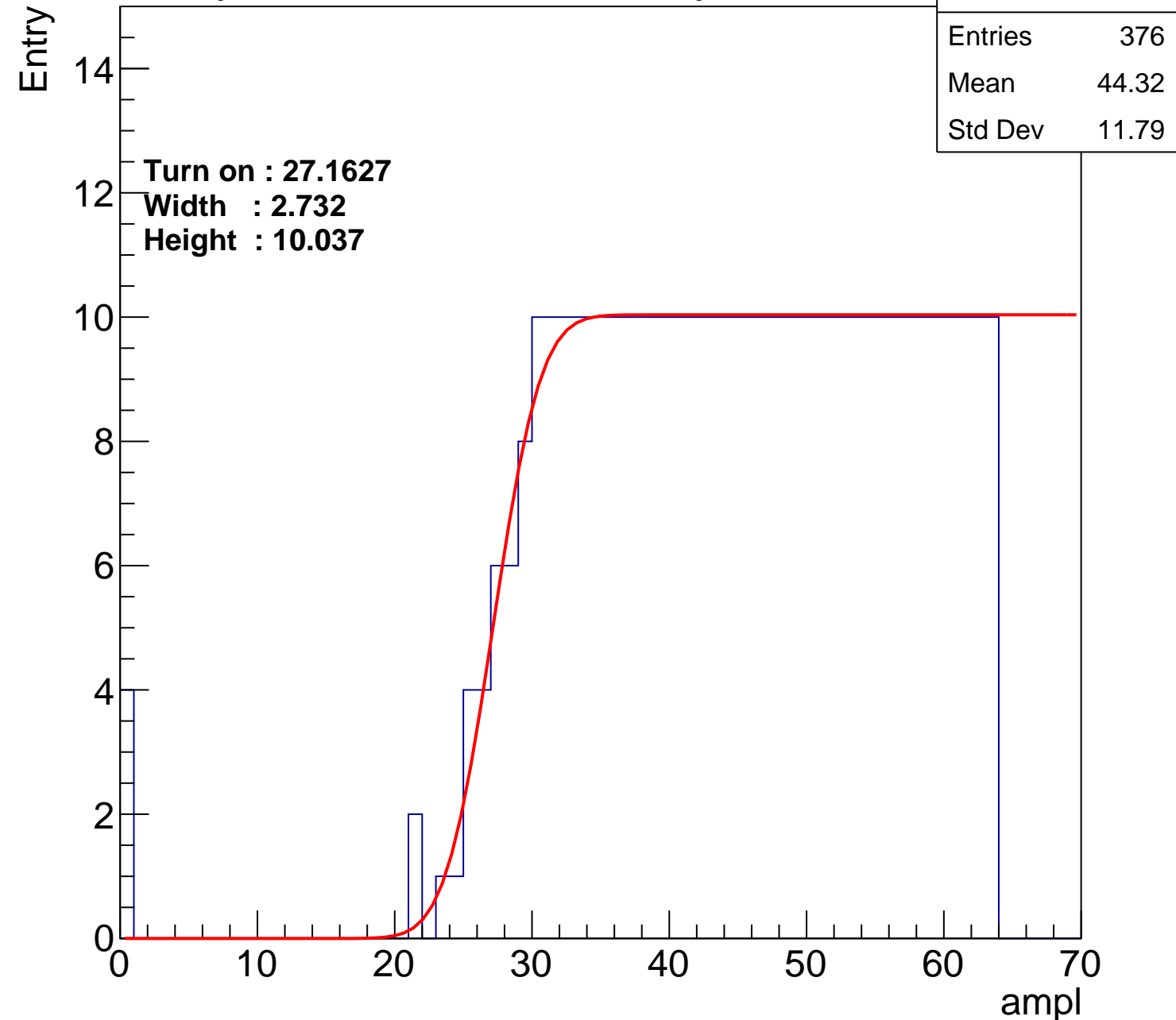
Width : 2.732

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch80

calib_packv5_042523_0143.root, FC#0, port D2

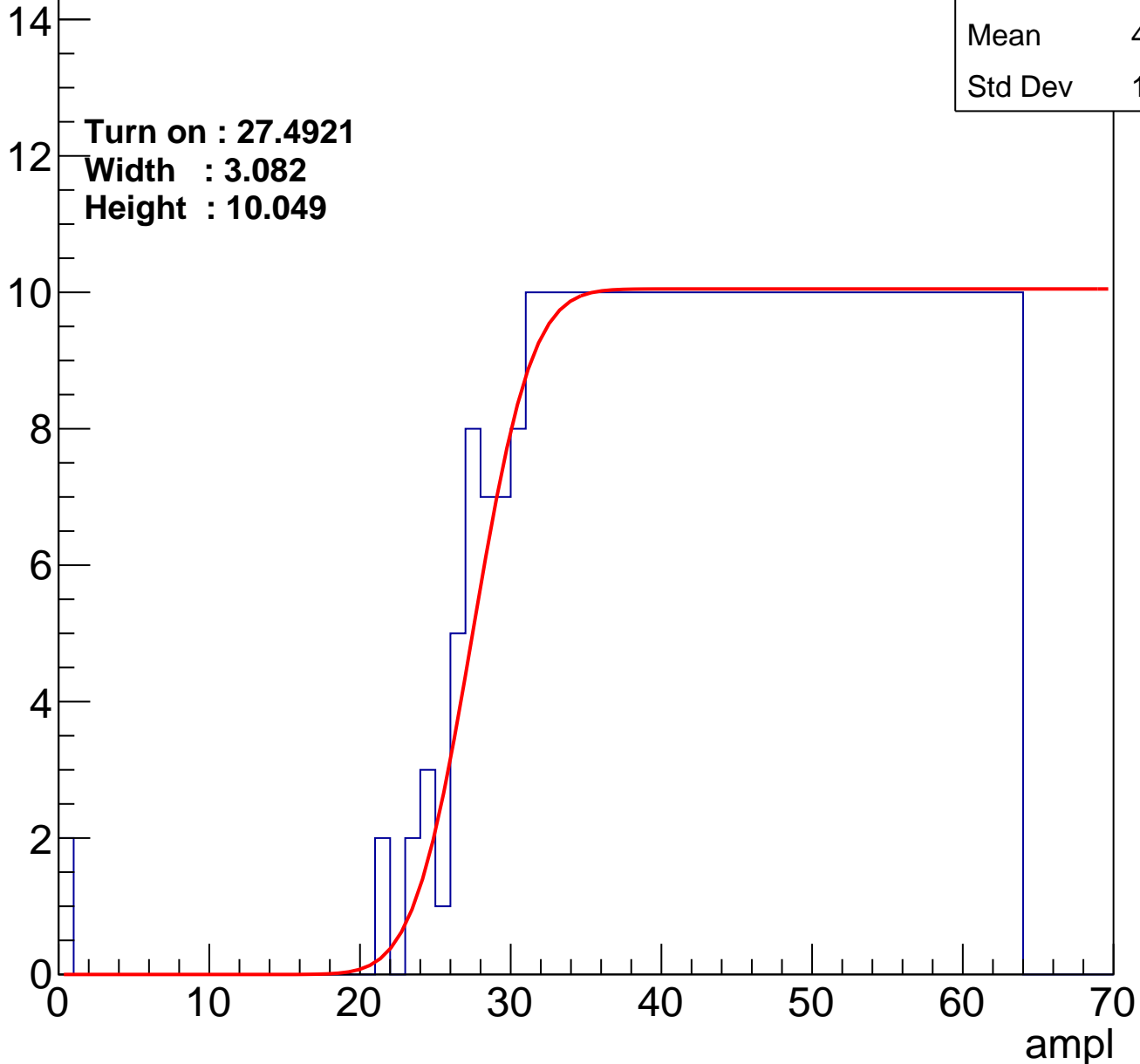
Entries	375
Mean	44.48
Std Dev	11.44

Turn on : 27.4921

Width : 3.082

Height : 10.049

Entry



B1L101S, U10-ch81

calib_packv5_042523_0143.root, FC#0, port D2

Entries	381
Mean	44.17
Std Dev	11.68

Turn on : 26.0255

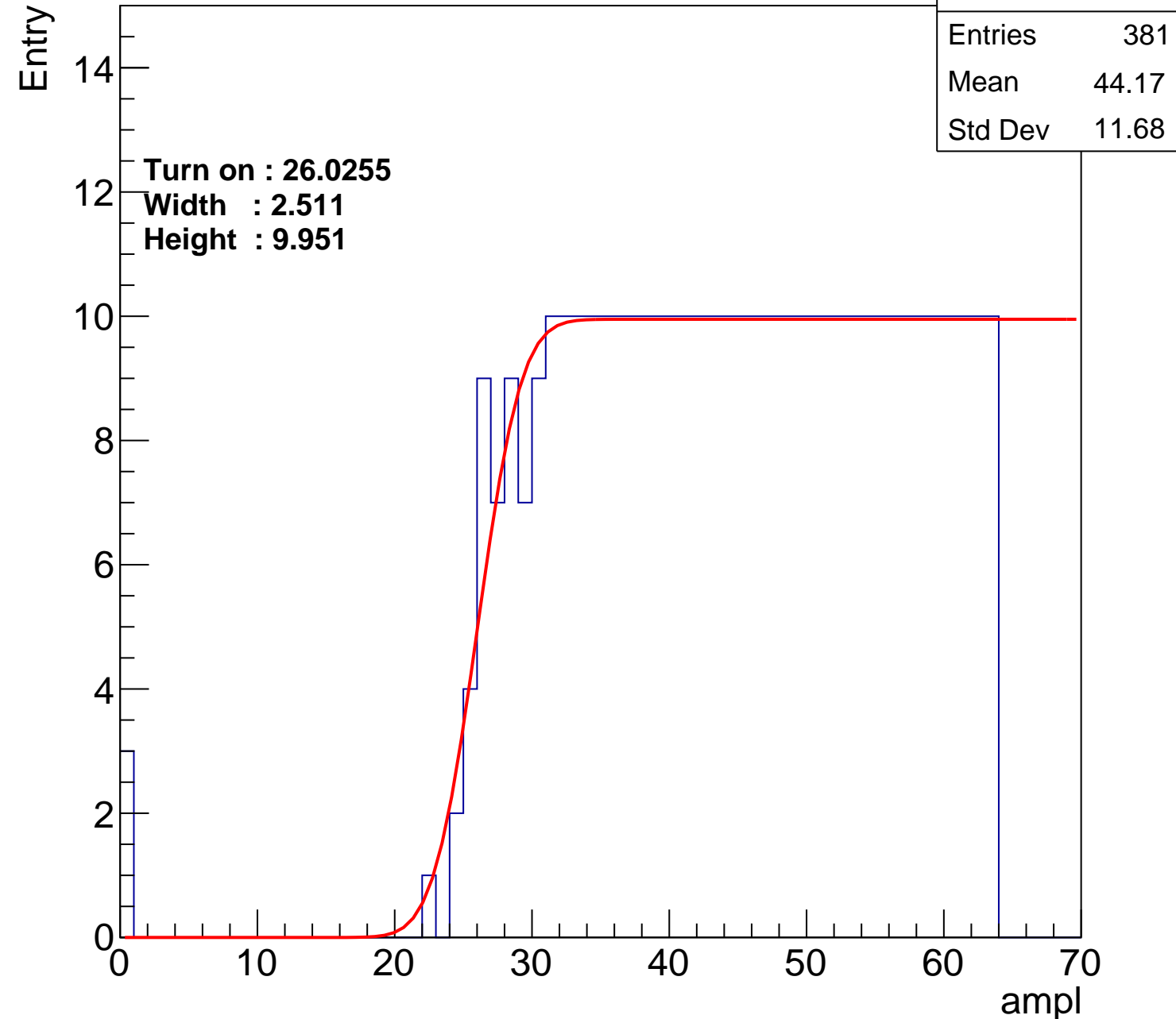
Width : 2.511

Height : 9.951

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch82

calib_packv5_042523_0143.root, FC#0, port D2

Entries	378
Mean	44.16
Std Dev	12

Turn on : 26.9420

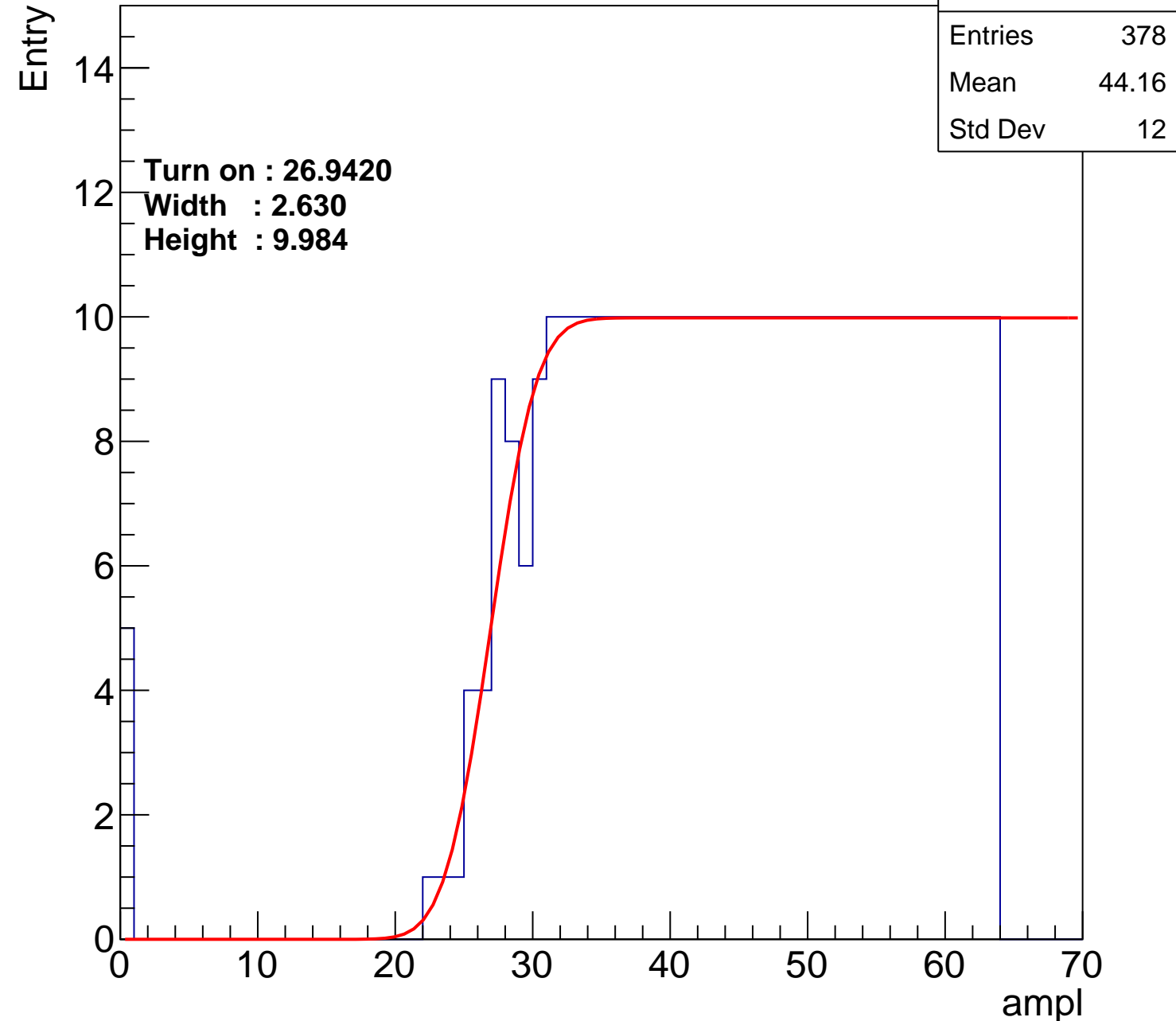
Width : 2.630

Height : 9.984

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch83

calib_packv5_042523_0143.root, FC#0, port D2

Entries	379
Mean	44.32
Std Dev	11.47

Turn on : 26.6984

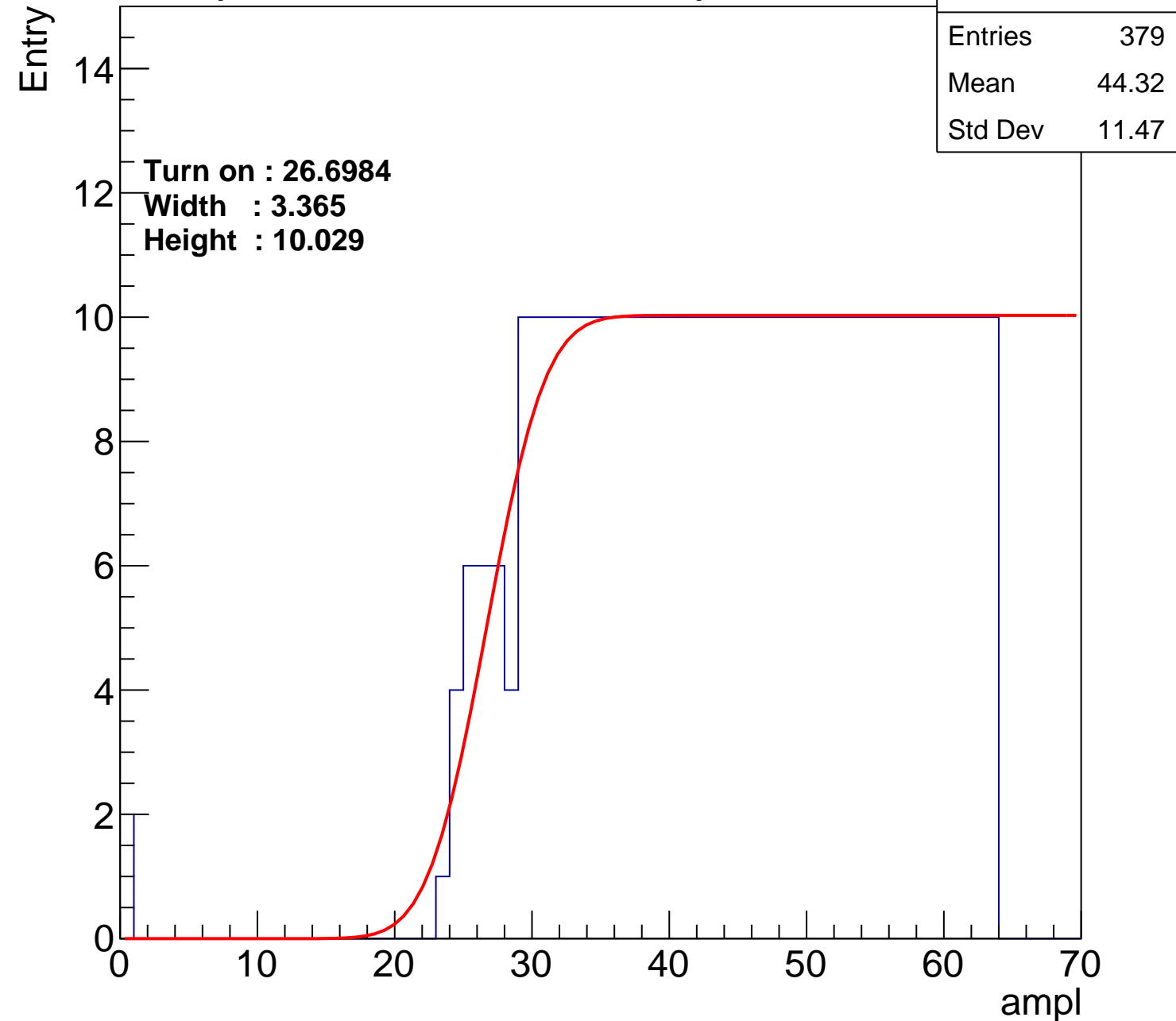
Width : 3.365

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch84

calib_packv5_042523_0143.root, FC#0, port D2

Entries	388
Mean	43.75
Std Dev	12.05

Turn on : 25.9190

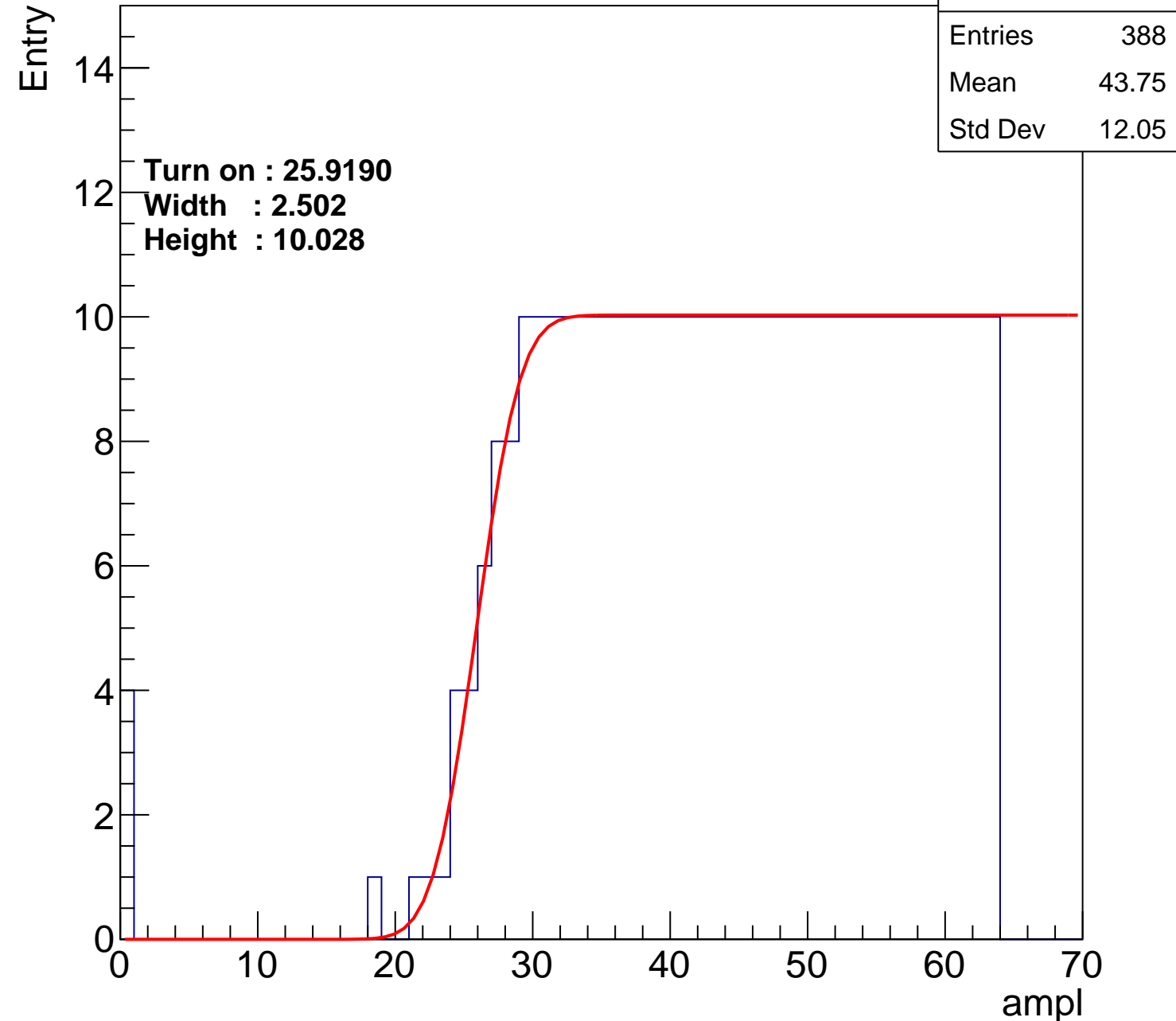
Width : 2.502

Height : 10.028

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch85

calib_packv5_042523_0143.root, FC#0, port D2

Entries	383
Mean	43.77
Std Dev	12.46

Turn on : 26.1153

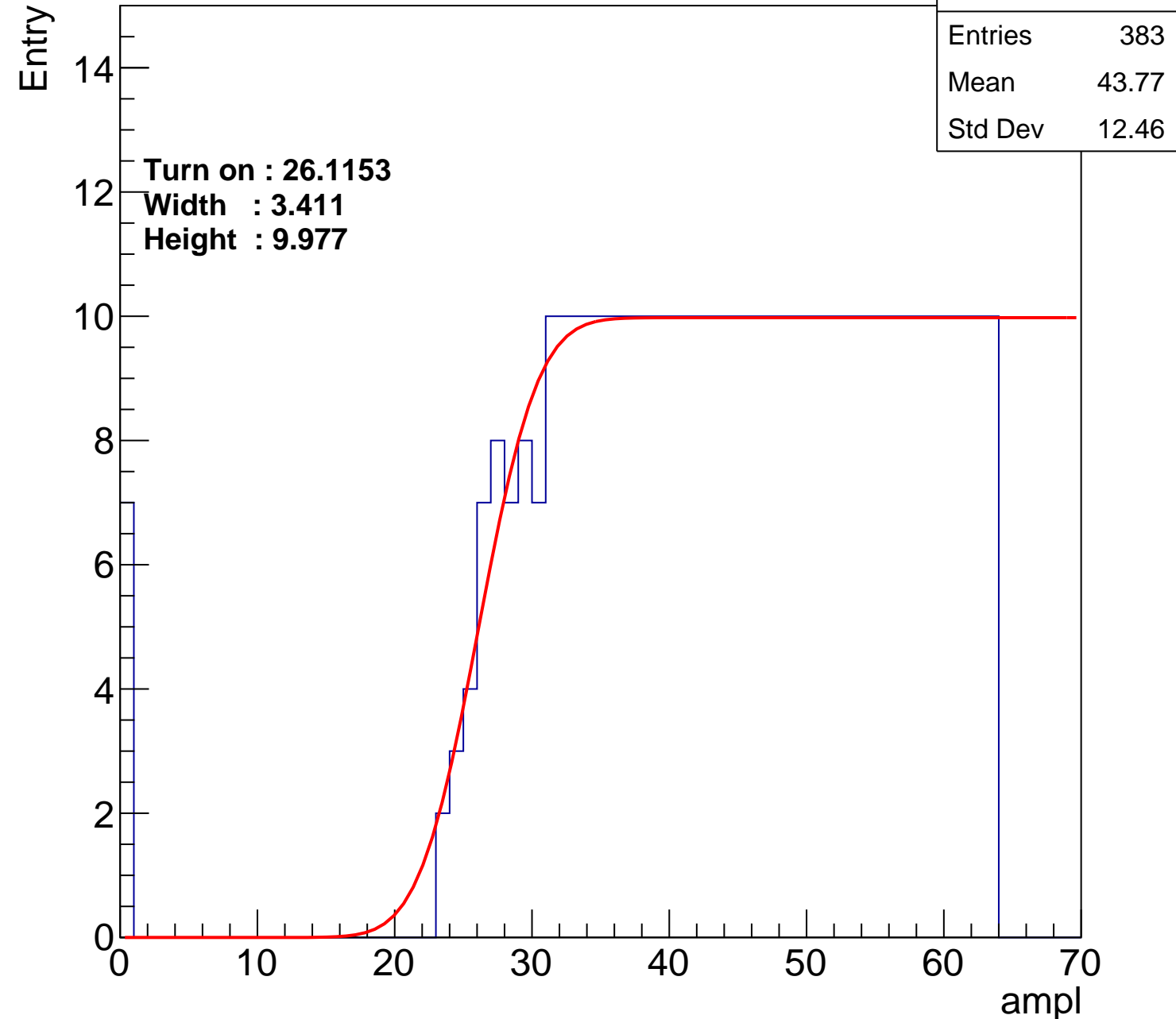
Width : 3.411

Height : 9.977

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch86

calib_packv5_042523_0143.root, FC#0, port D2

Entries	389
Mean	43.56
Std Dev	12.48

Turn on : 26.2706

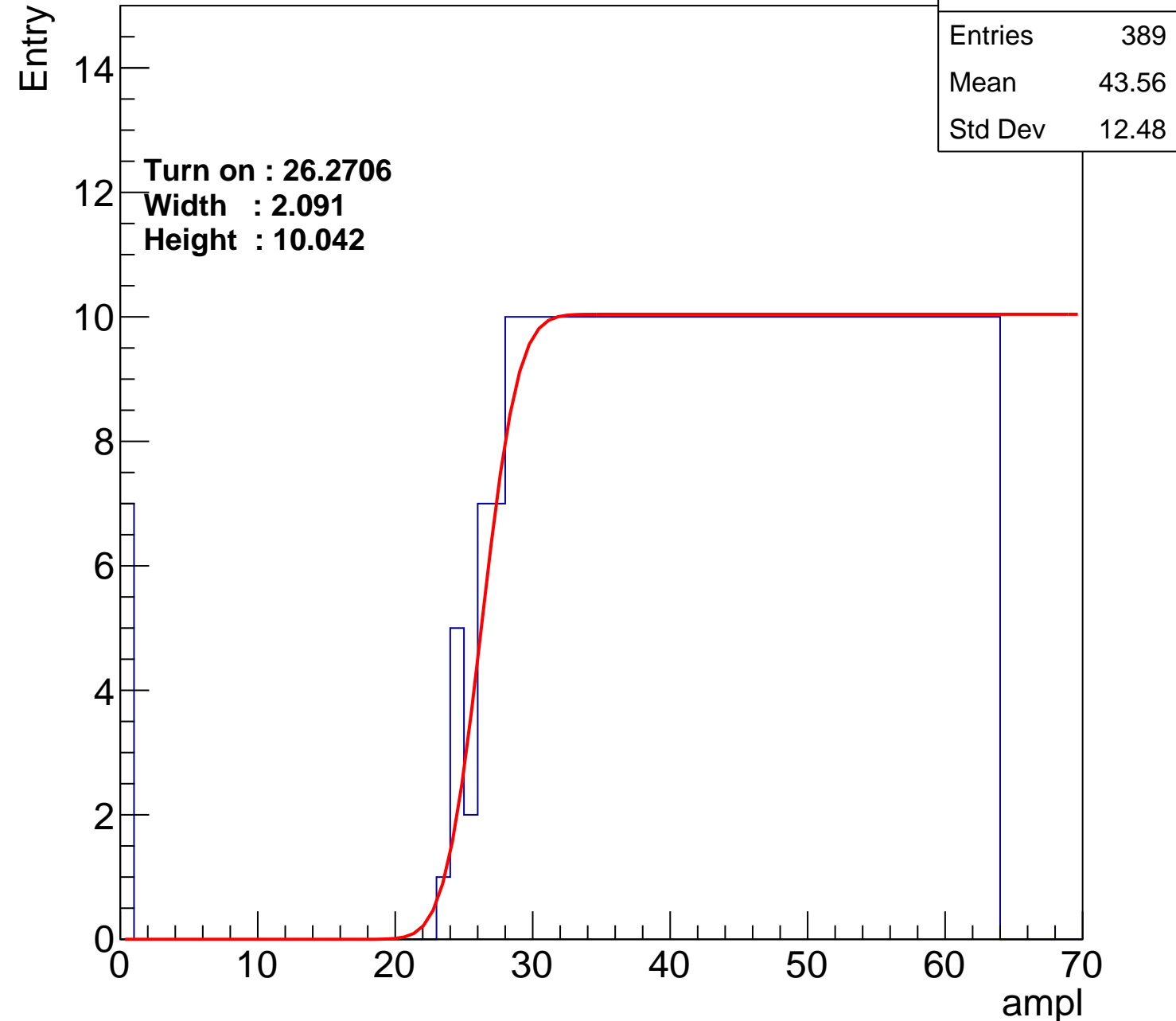
Width : 2.091

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch87

calib_packv5_042523_0143.root, FC#0, port D2

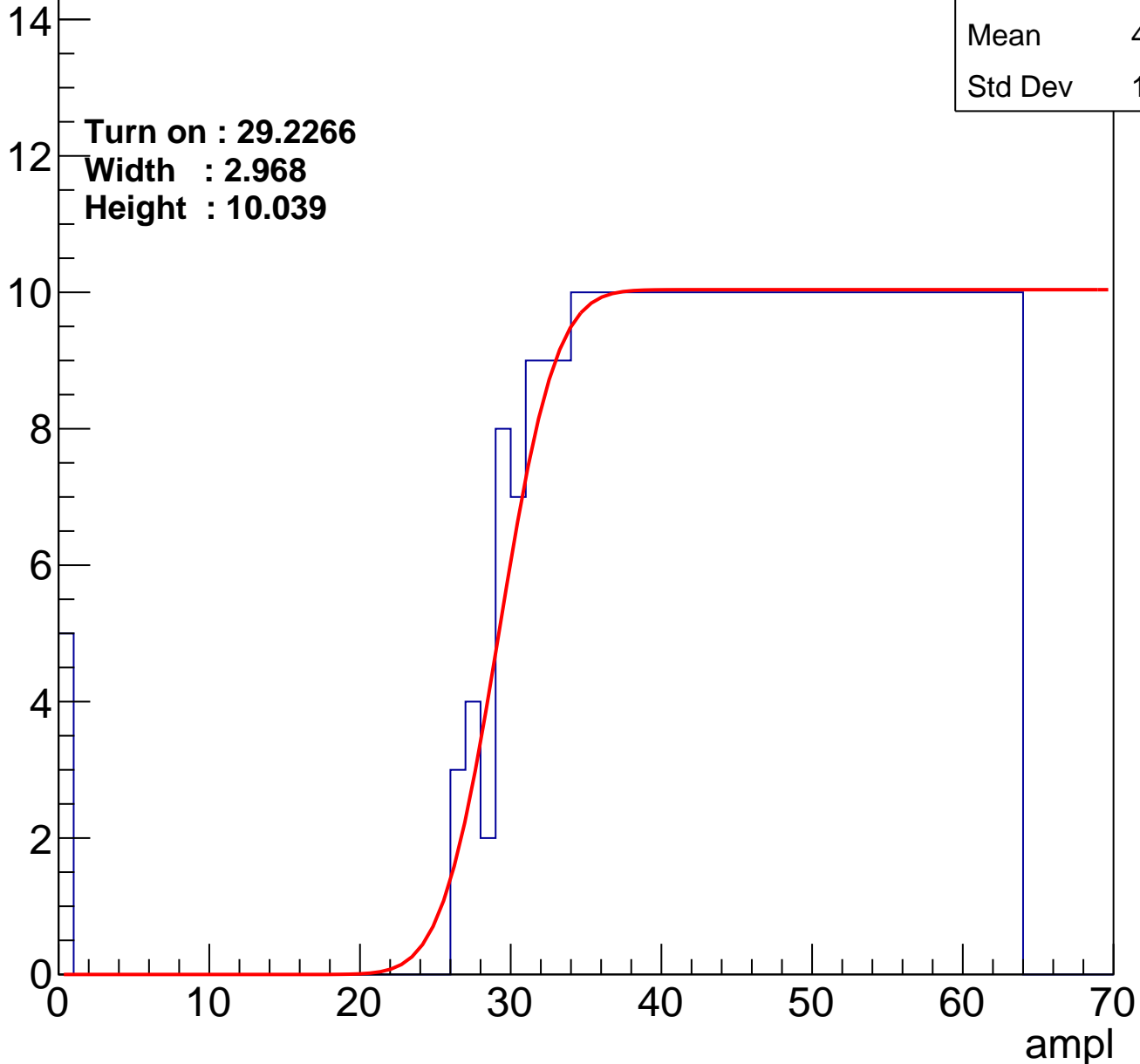
Entries	356
Mean	45.22
Std Dev	11.54

Turn on : 29.2266

Width : 2.968

Height : 10.039

Entry



B1L101S, U10-ch88

calib_packv5_042523_0143.root, FC#0, port D2

Entries	385
Mean	43.79
Std Dev	12.2

Turn on : 26.2157

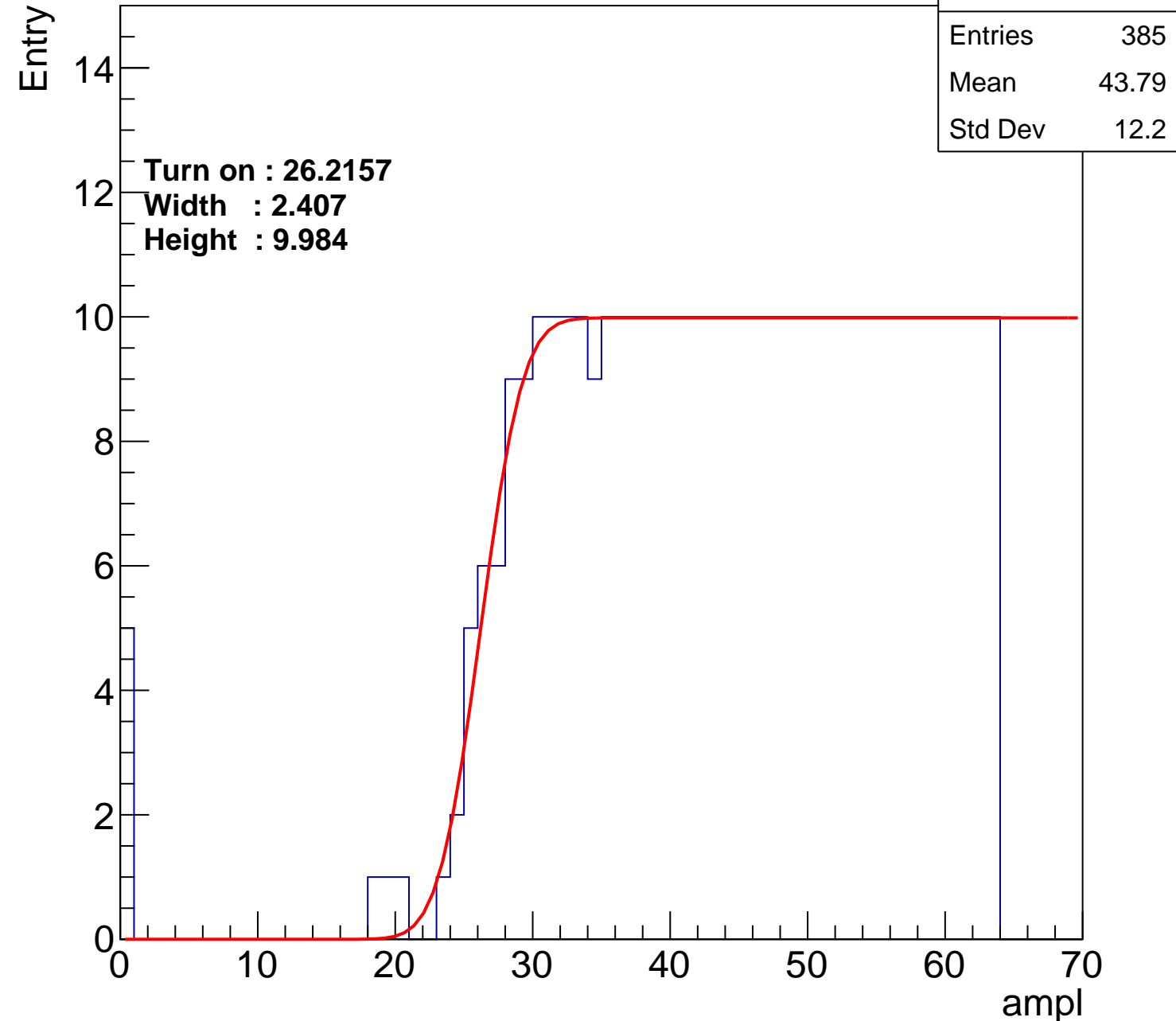
Width : 2.407

Height : 9.984

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch89

calib_packv5_042523_0143.root, FC#0, port D2

Entries	371
Mean	44.56
Std Dev	11.68

Turn on : 27.4481

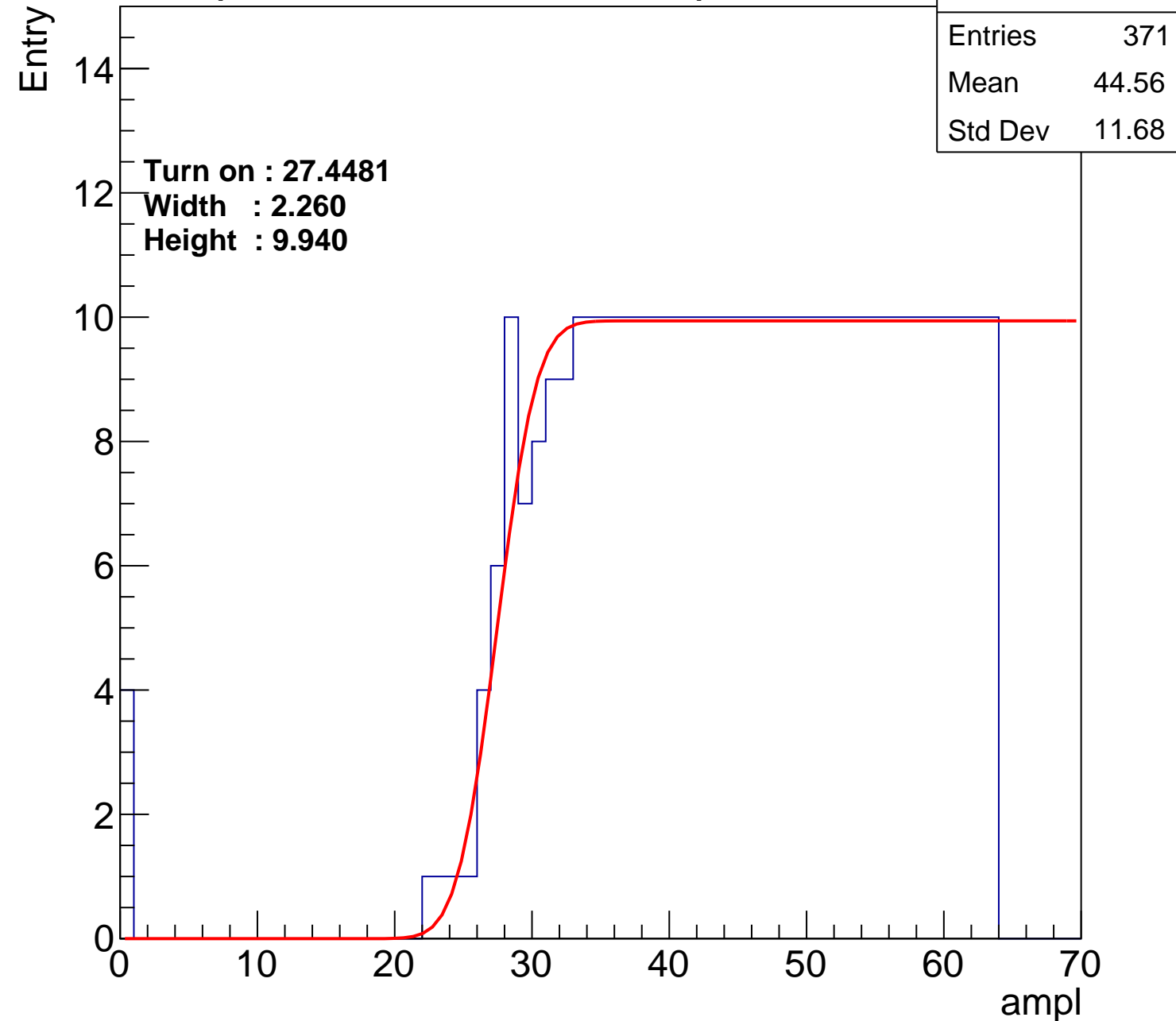
Width : 2.260

Height : 9.940

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch90

calib_packv5_042523_0143.root, FC#0, port D2

Entries	397
Mean	43.33
Std Dev	12.16

Turn on : 25.0166

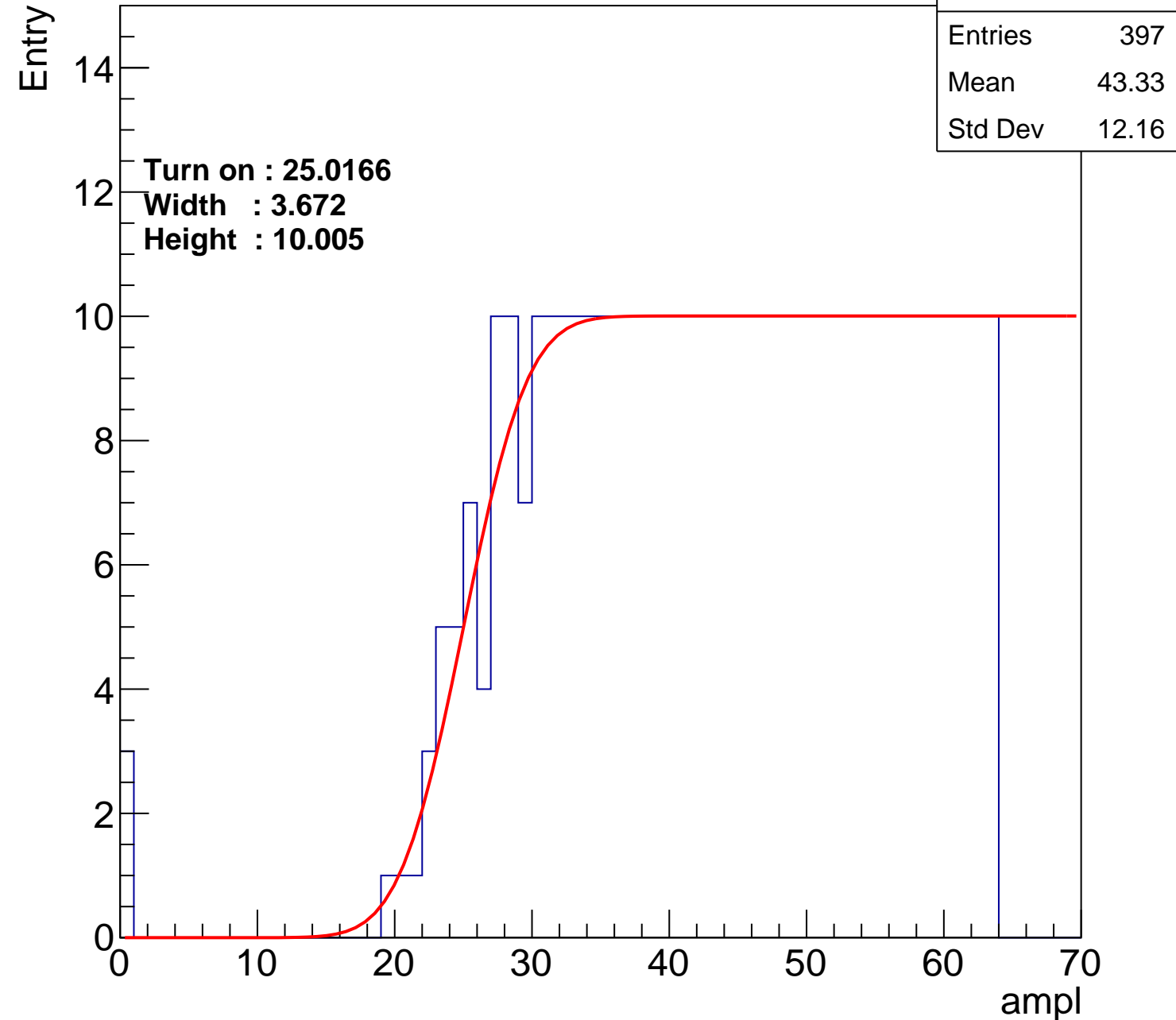
Width : 3.672

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch91

calib_packv5_042523_0143.root, FC#0, port D2

Entries	362
Mean	45.24
Std Dev	10.81

Turn on : 28.4786

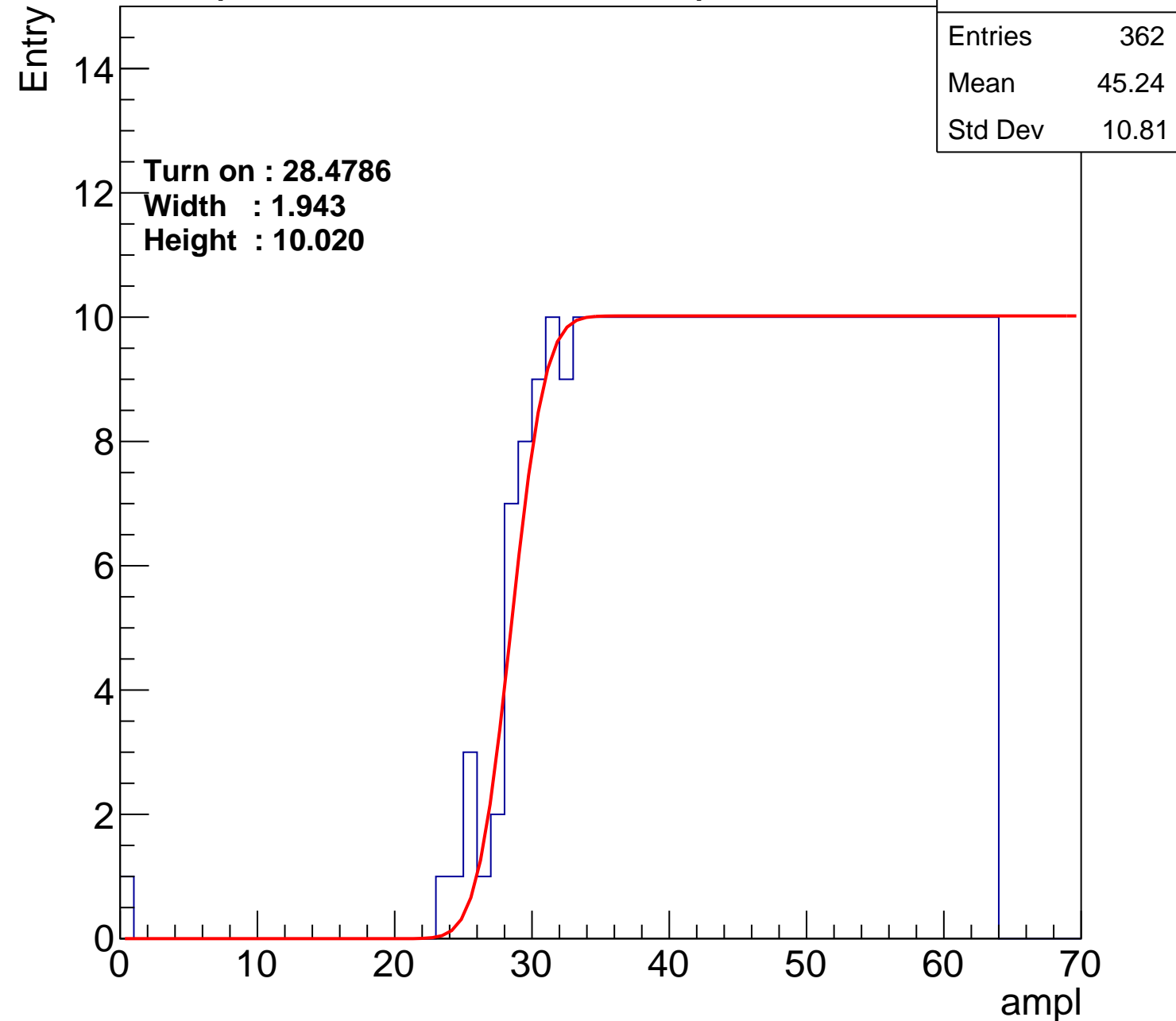
Width : 1.943

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch92

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.42
Std Dev	11.62

Turn on : 27.7477

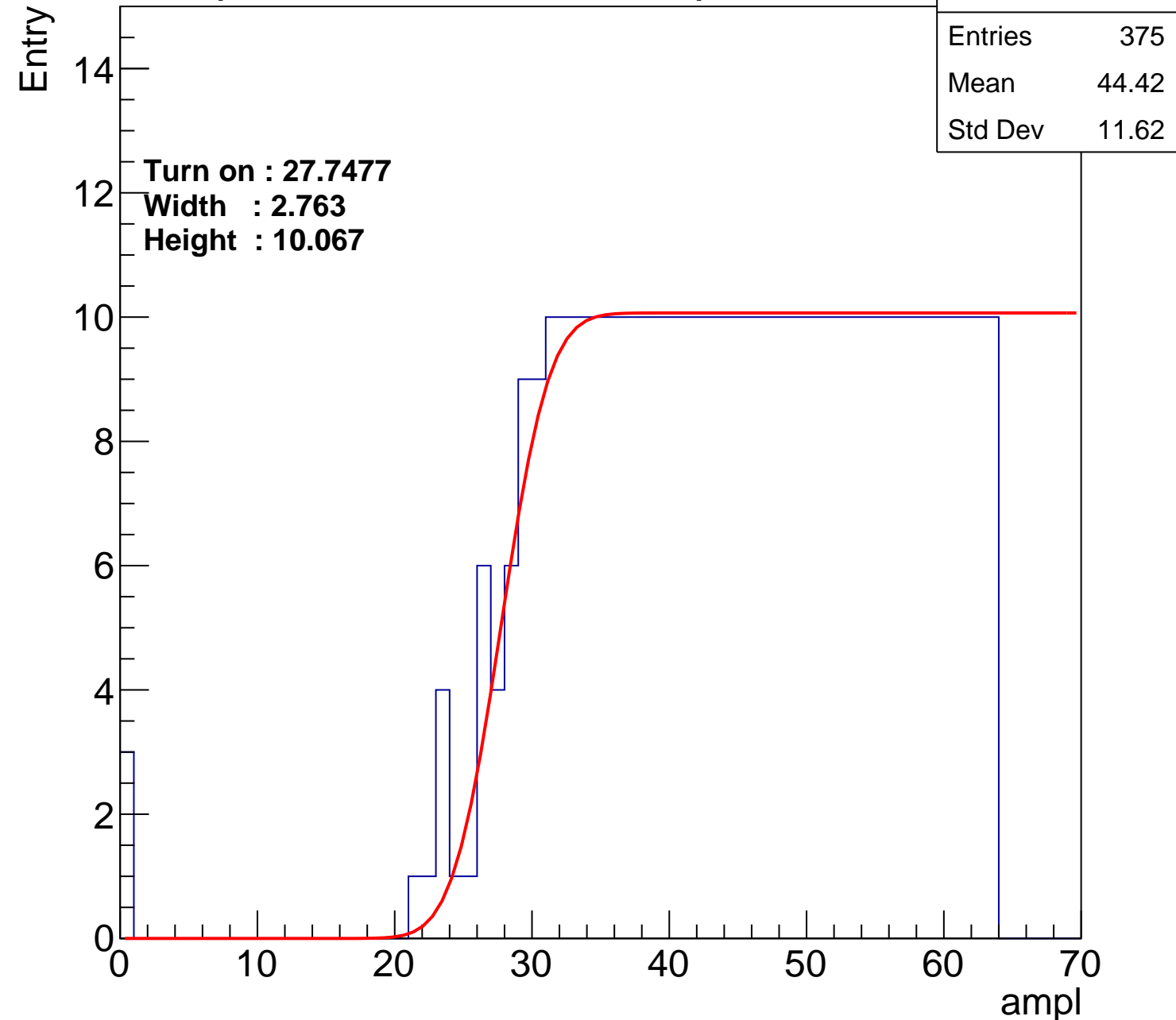
Width : 2.763

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch93

calib_packv5_042523_0143.root, FC#0, port D2

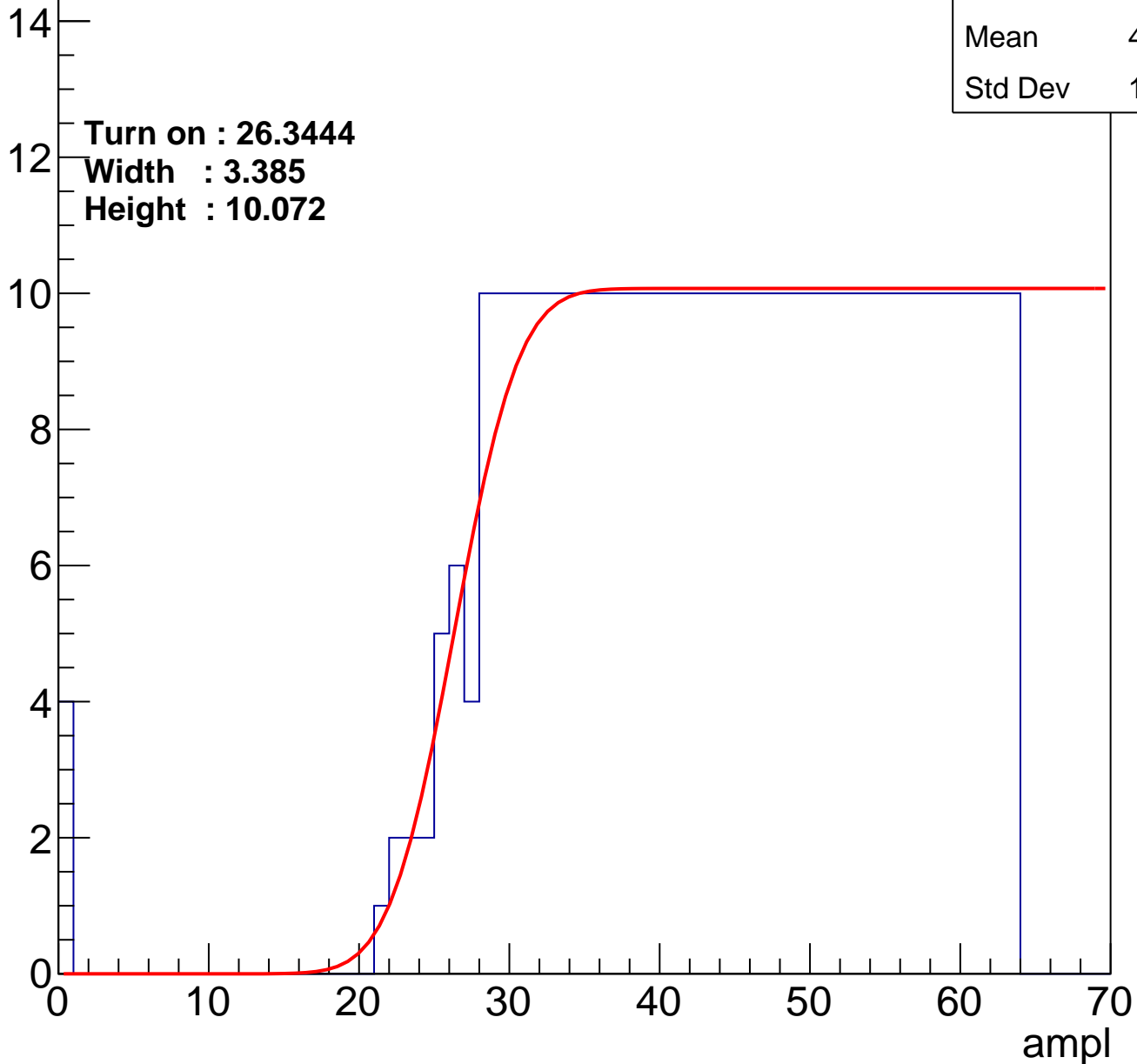
Entries	386
Mean	43.85
Std Dev	11.99

Turn on : 26.3444

Width : 3.385

Height : 10.072

Entry



B1L101S, U10-ch94

calib_packv5_042523_0143.root, FC#0, port D2

Entries	365
Mean	45.02
Std Dev	11.11

Turn on : 27.9802

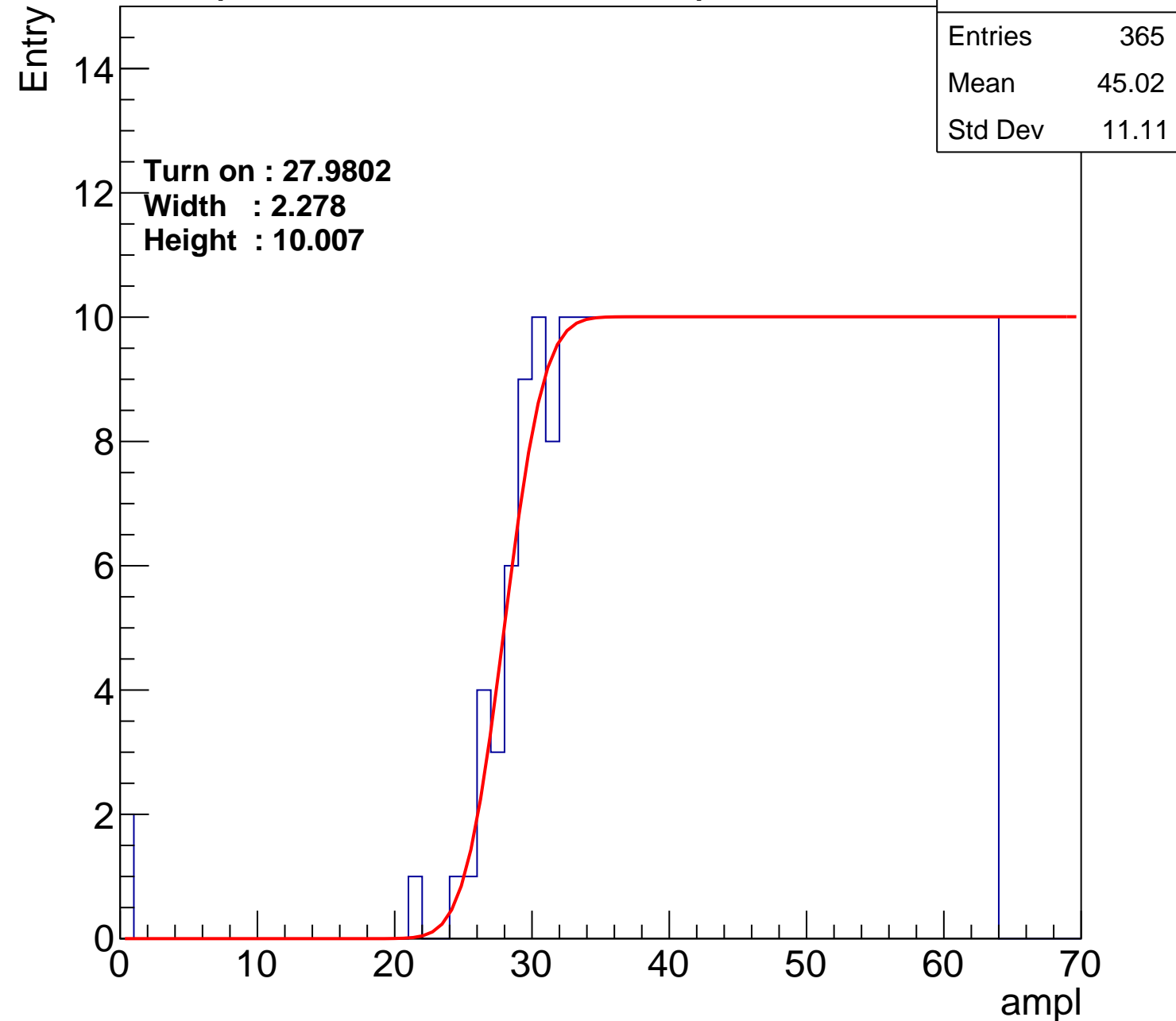
Width : 2.278

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch95

calib_packv5_042523_0143.root, FC#0, port D2

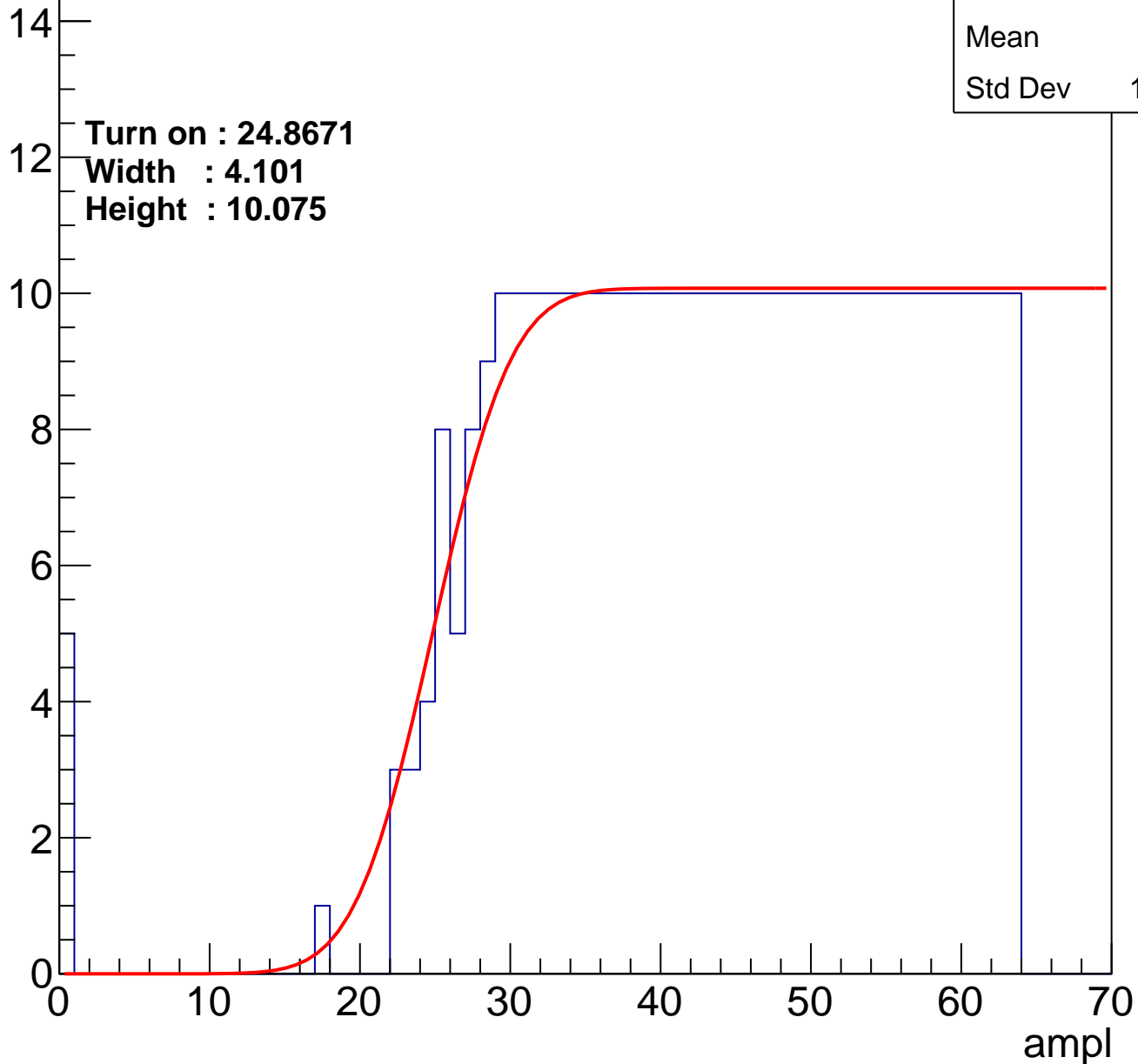
Entries	396
Mean	43.3
Std Dev	12.39

Turn on : 24.8671

Width : 4.101

Height : 10.075

Entry



B1L101S, U10-ch96

calib_packv5_042523_0143.root, FC#0, port D2

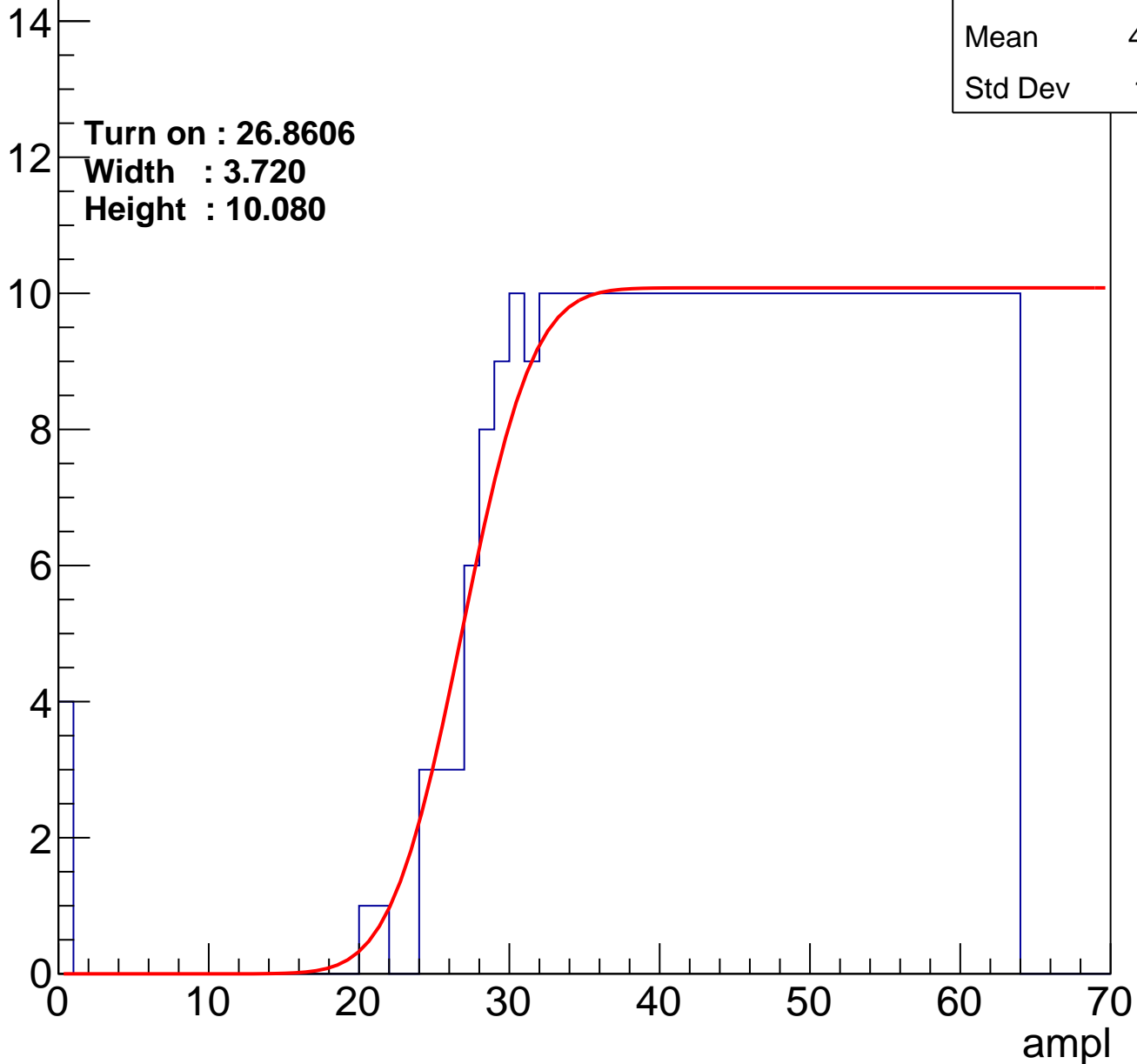
Entries	377
Mean	44.28
Std Dev	11.81

Turn on : 26.8606

Width : 3.720

Height : 10.080

Entry



B1L101S, U10-ch97

calib_packv5_042523_0143.root, FC#0, port D2

Entries	351
Mean	45.65
Std Dev	10.84

Turn on : 28.8372

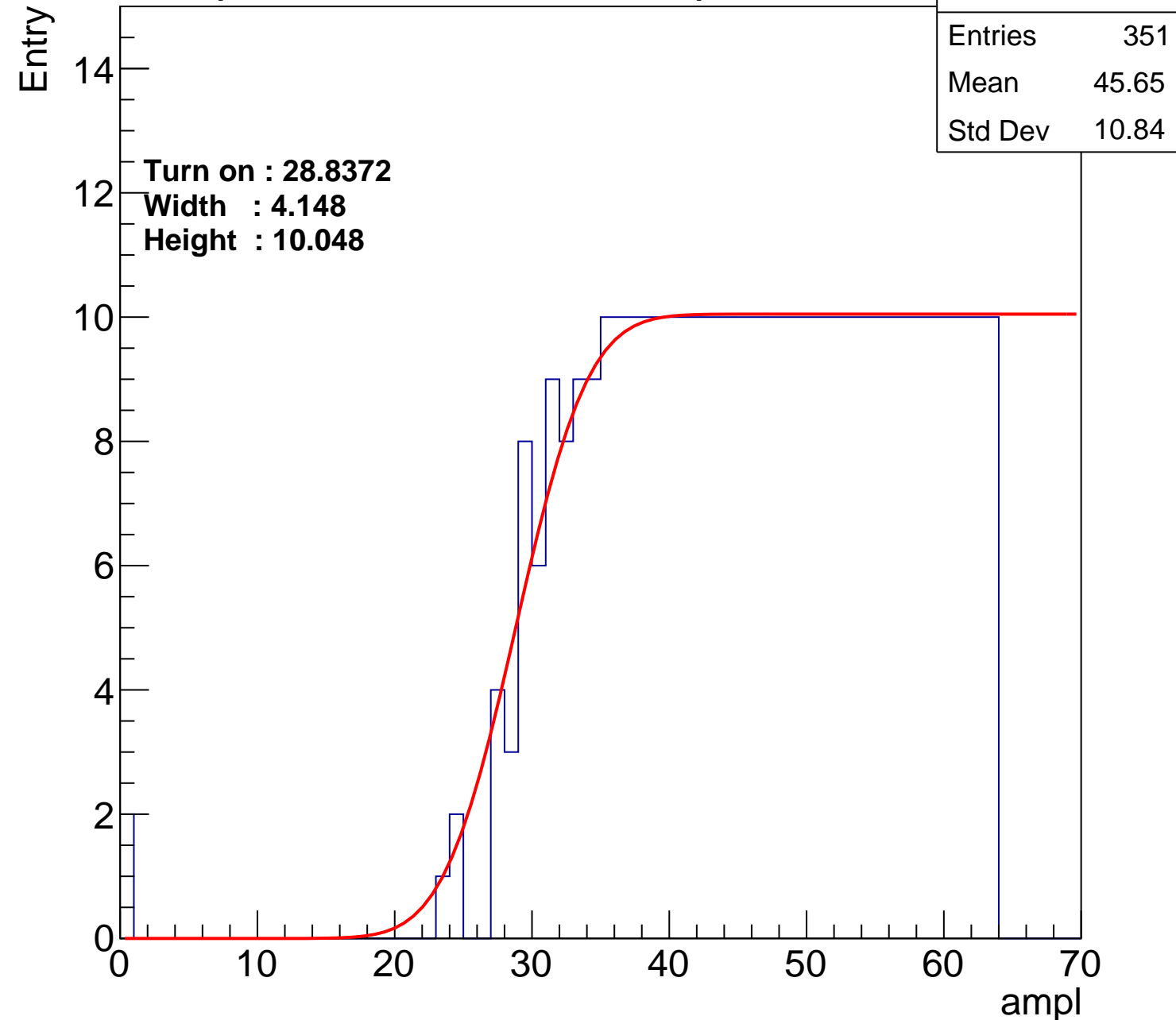
Width : 4.148

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch98

calib_packv5_042523_0143.root, FC#0, port D2

Entries	391
Mean	43.62
Std Dev	12.03

Turn on : 25.4671

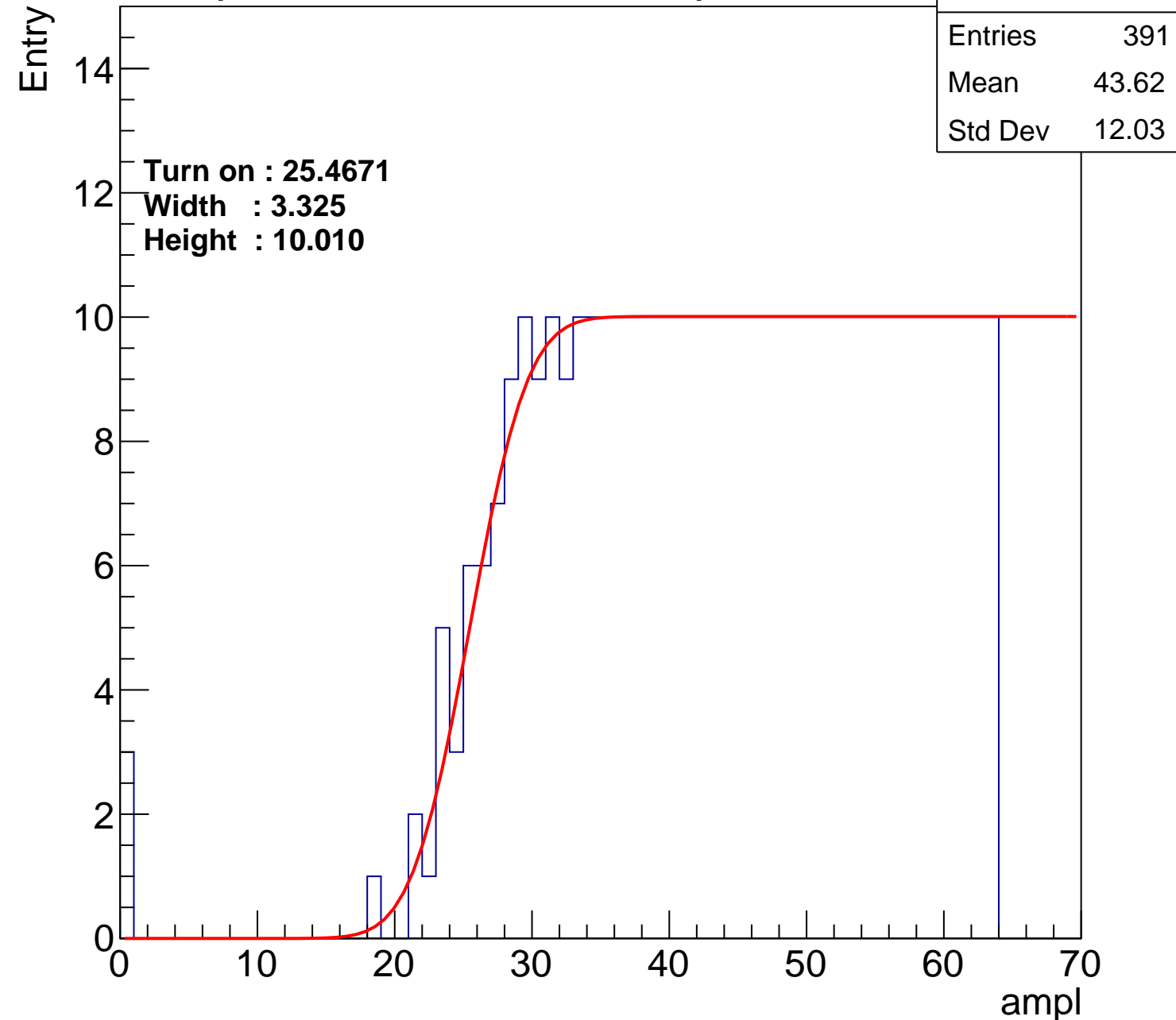
Width : 3.325

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch99

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.41
Std Dev	11.48

Turn on : 26.7240

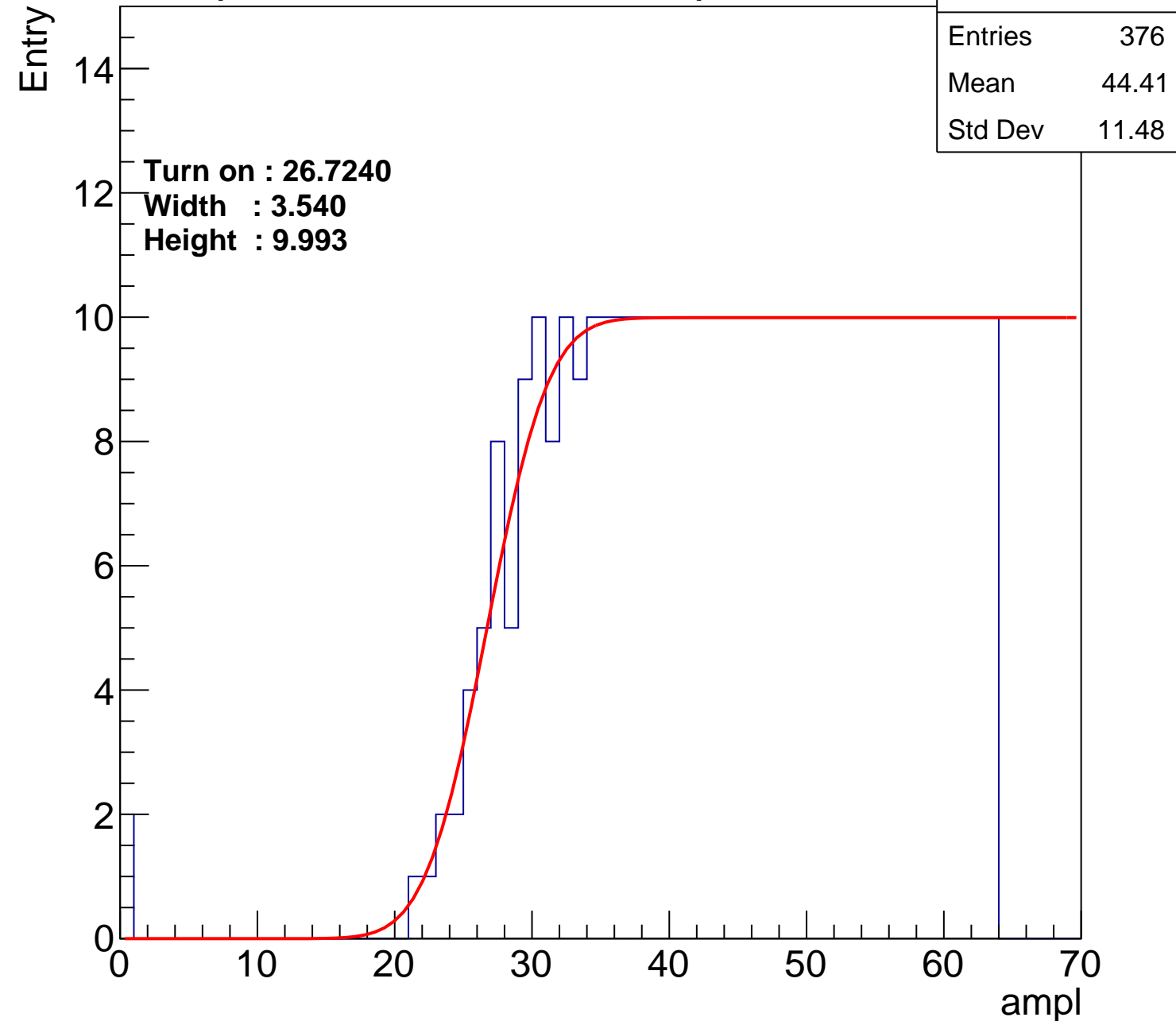
Width : 3.540

Height : 9.993

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch100

calib_packv5_042523_0143.root, FC#0, port D2

Entries	373
Mean	44.56
Std Dev	11.49

Turn on : 27.1680

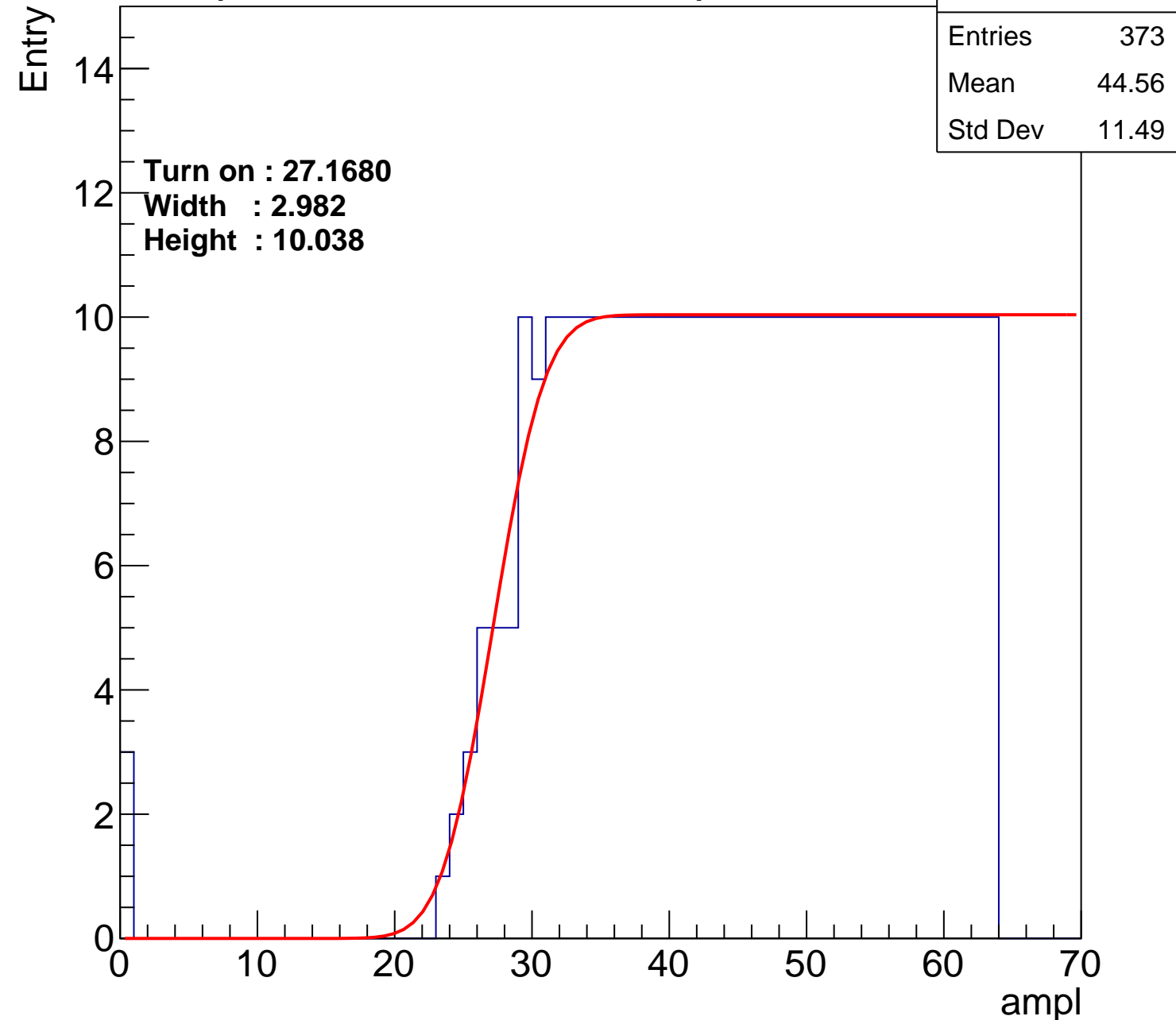
Width : 2.982

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch101

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.49
Std Dev	11.28

Turn on : 27.4274

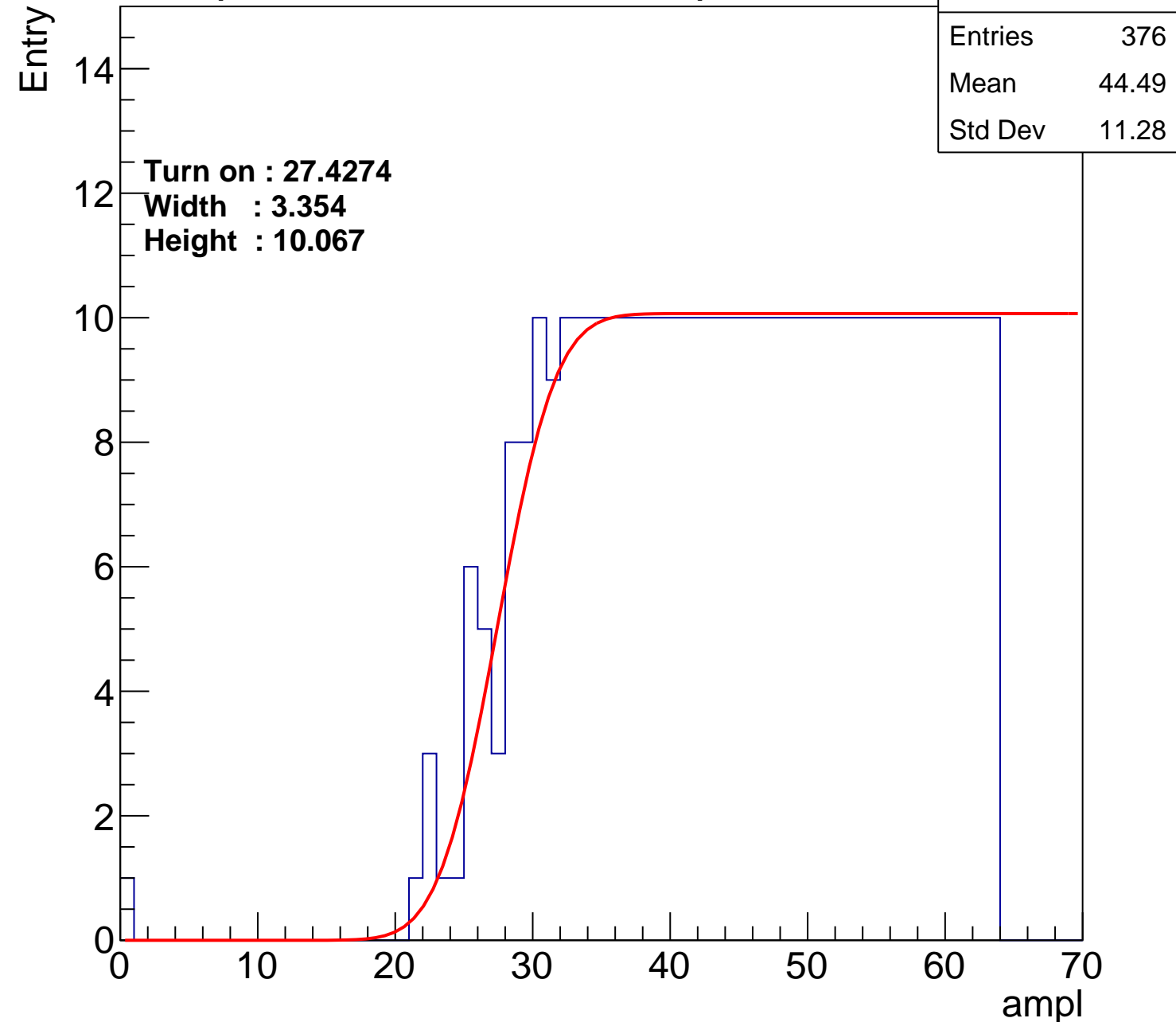
Width : 3.354

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch102

calib_packv5_042523_0143.root, FC#0, port D2

Entries	370
Mean	44.74
Std Dev	11.2

Turn on : 27.4119

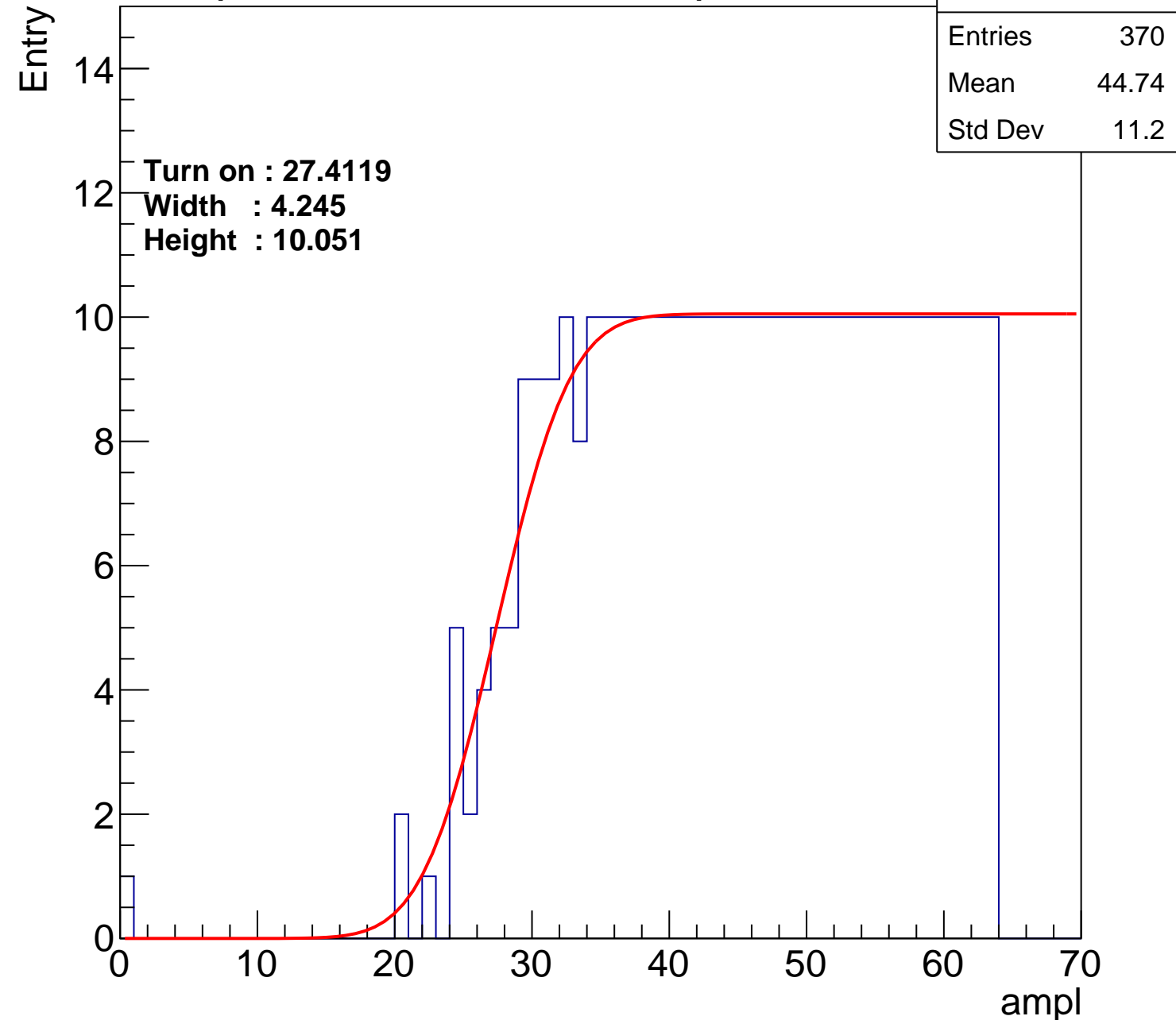
Width : 4.245

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch103

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.38
Std Dev	11.62

Turn on : 26.7104

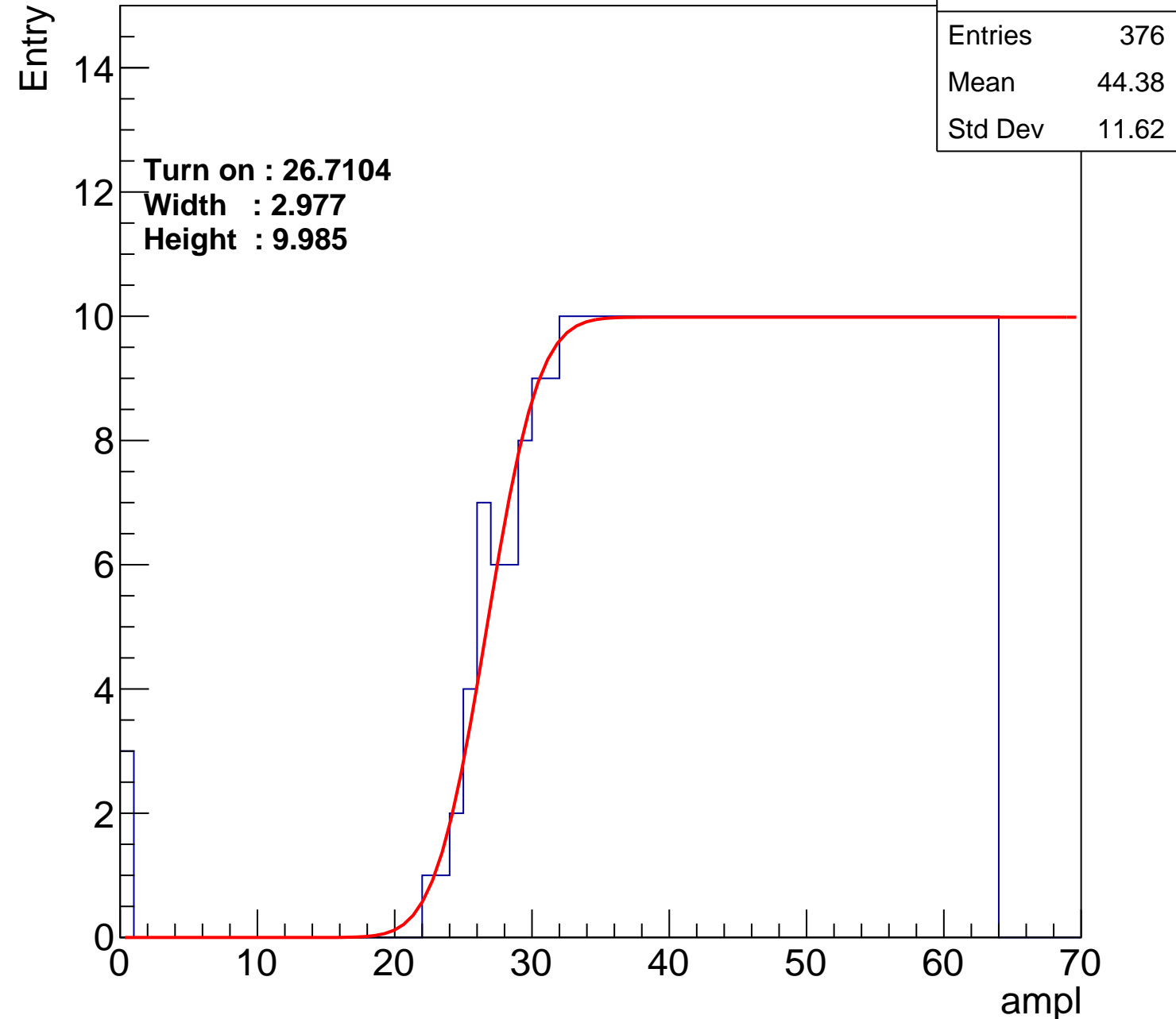
Width : 2.977

Height : 9.985

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch104

calib_packv5_042523_0143.root, FC#0, port D2

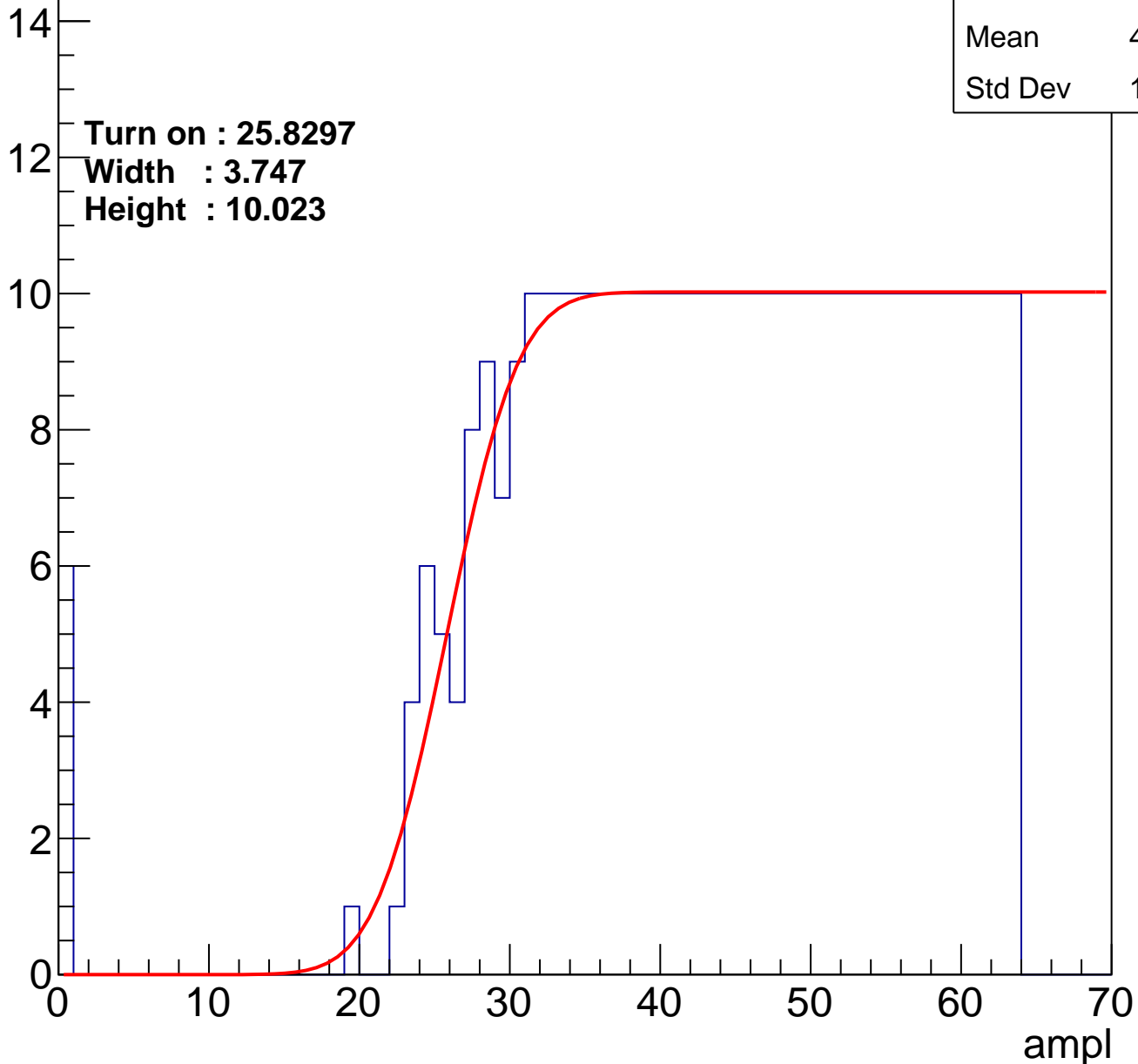
Entries	390
Mean	43.48
Std Dev	12.48

Turn on : 25.8297

Width : 3.747

Height : 10.023

Entry



B1L101S, U10-ch105

calib_packv5_042523_0143.root, FC#0, port D2

Entries	360
Mean	45.3
Std Dev	10.82

Turn on : 28.1579

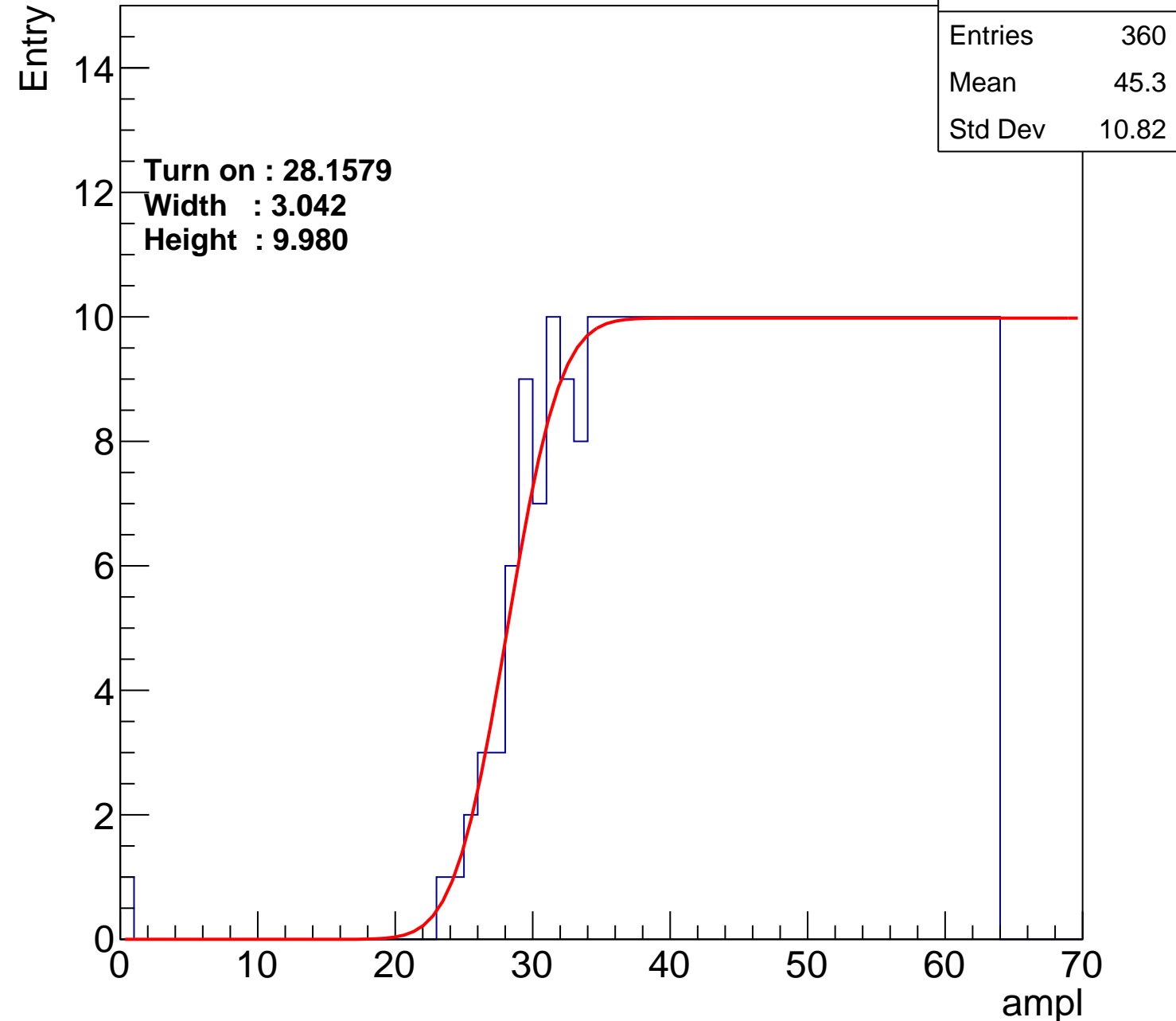
Width : 3.042

Height : 9.980

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch106

calib_packv5_042523_0143.root, FC#0, port D2

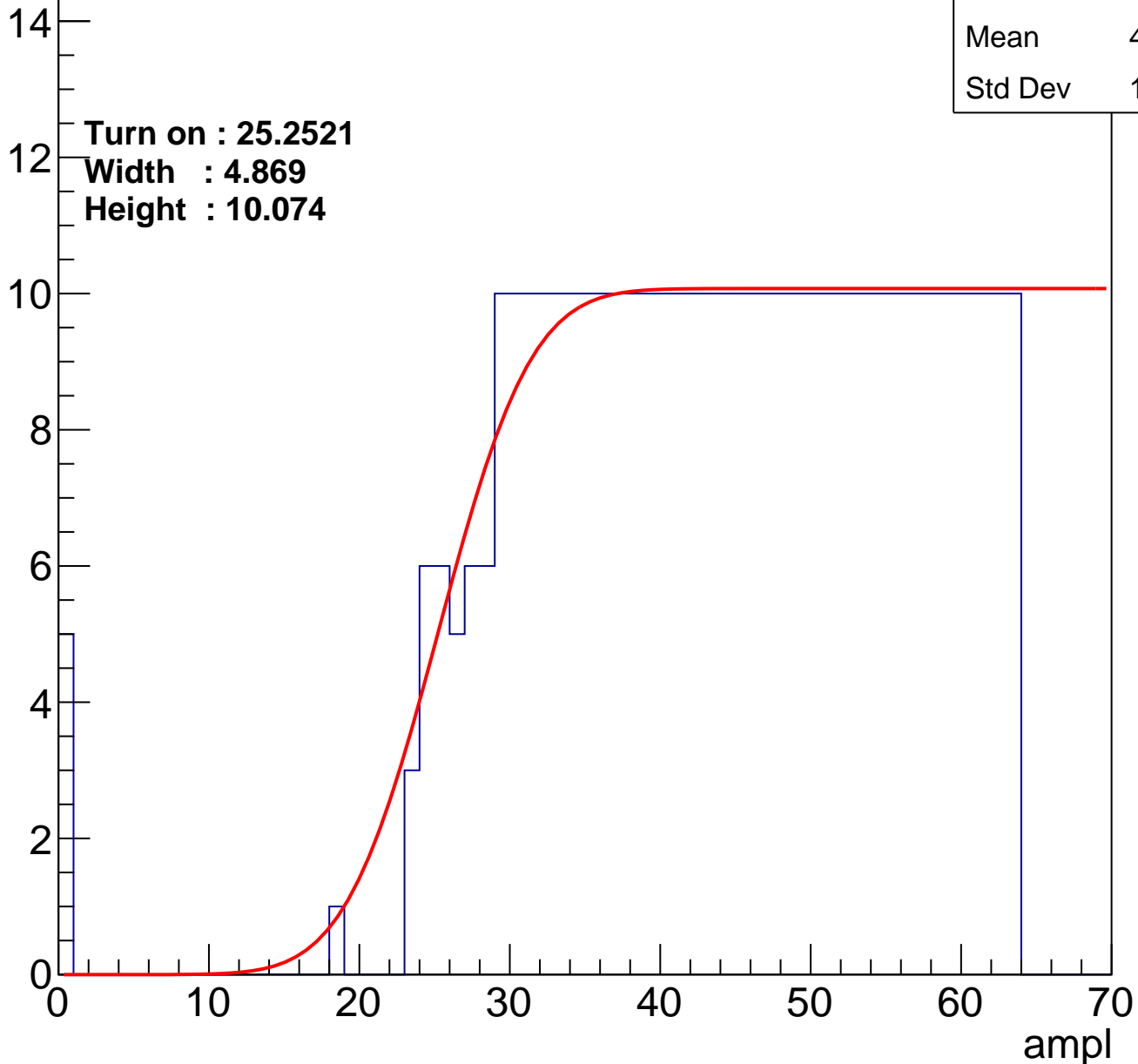
Entries	388
Mean	43.66
Std Dev	12.25

Turn on : 25.2521

Width : 4.869

Height : 10.074

Entry



B1L101S, U10-ch107

calib_packv5_042523_0143.root, FC#0, port D2

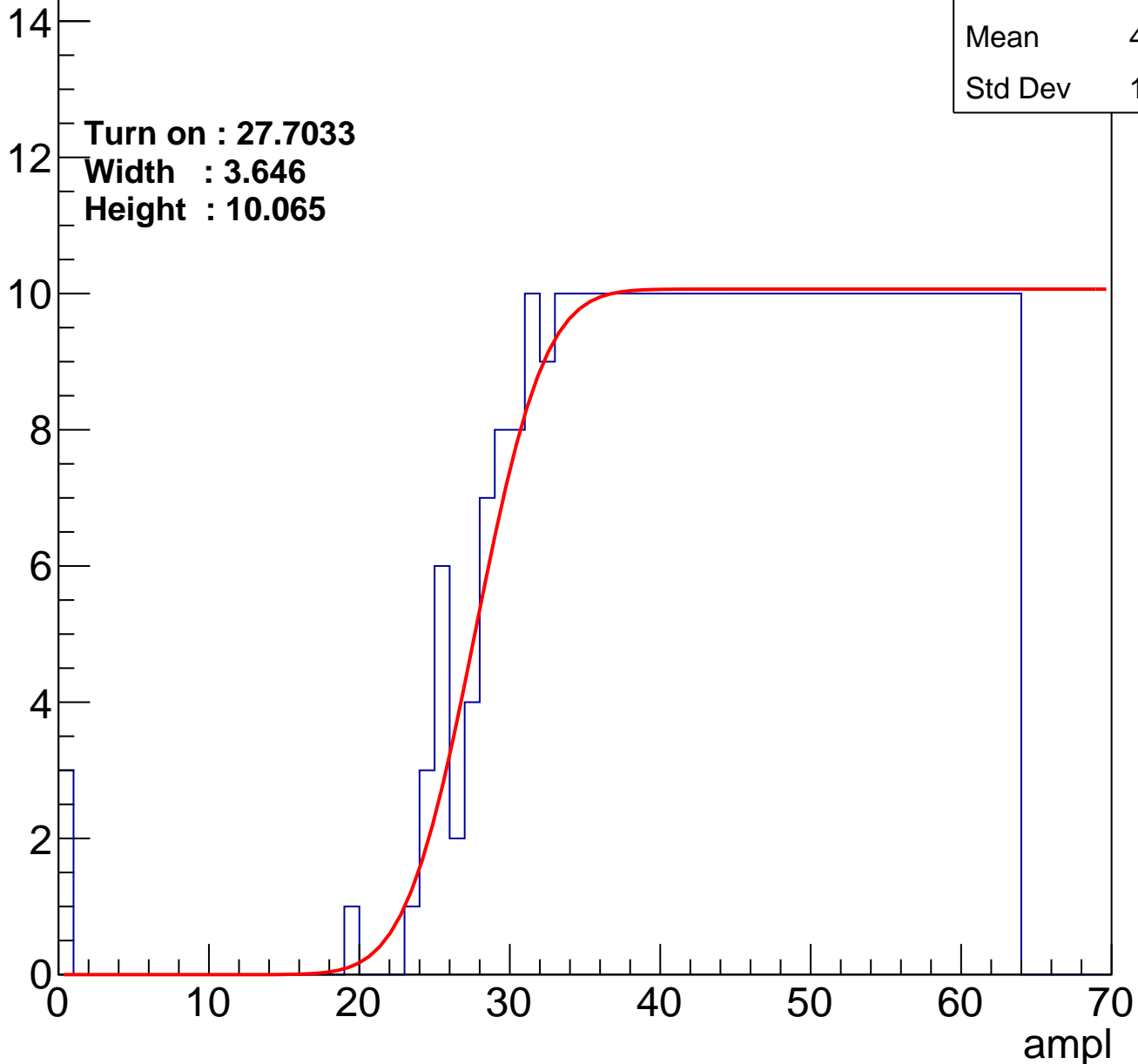
Entries	372
Mean	44.54
Std Dev	11.57

Turn on : 27.7033

Width : 3.646

Height : 10.065

Entry



B1L101S, U10-ch108

calib_packv5_042523_0143.root, FC#0, port D2

Entries	380
Mean	43.98
Std Dev	12.25

Turn on : 26.5795

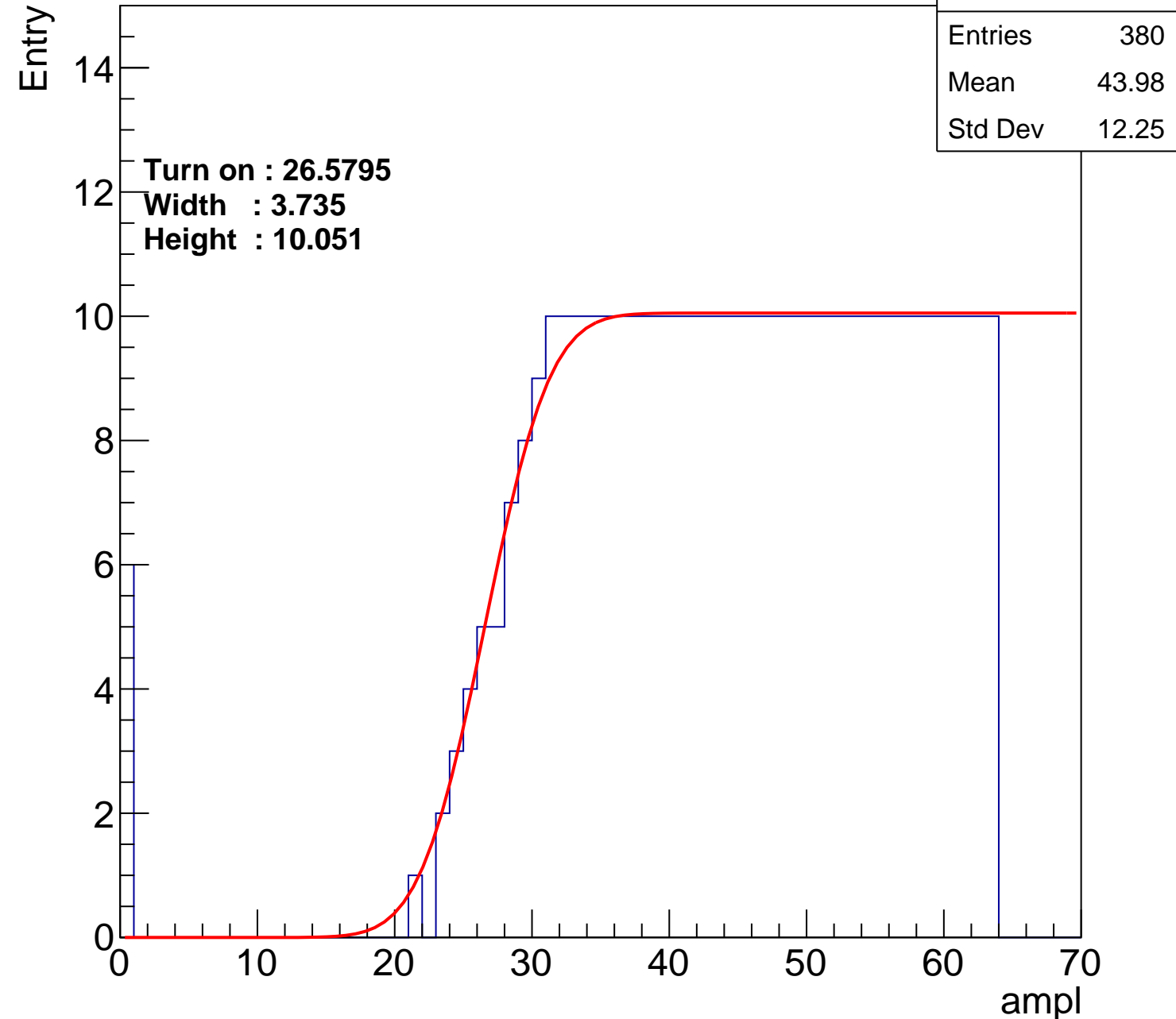
Width : 3.735

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch109

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.48
Std Dev	11.43

Turn on : 26.8168

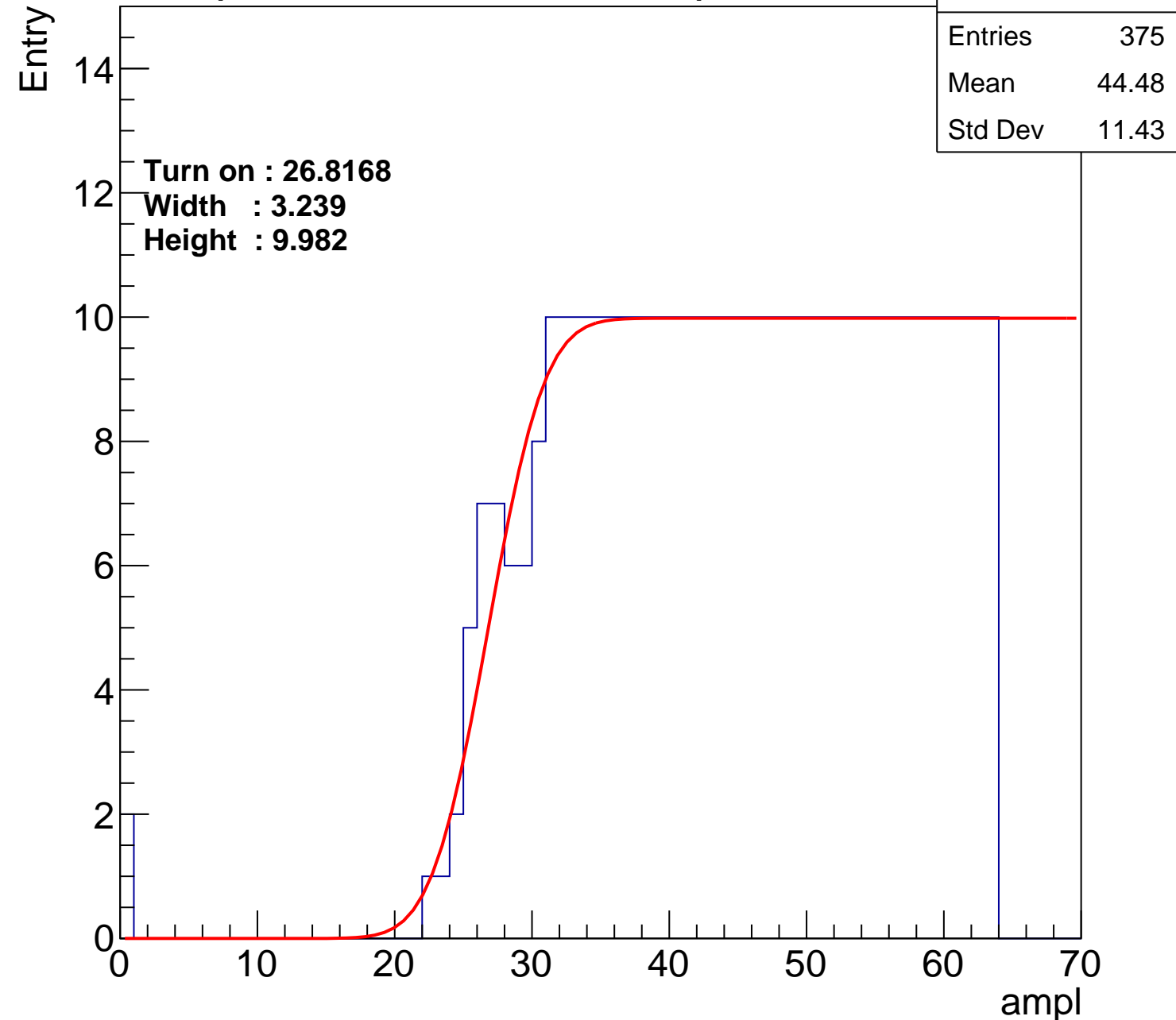
Width : 3.239

Height : 9.982

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch110

calib_packv5_042523_0143.root, FC#0, port D2

Entries	381
Mean	44.25
Std Dev	11.4

Turn on : 26.2609

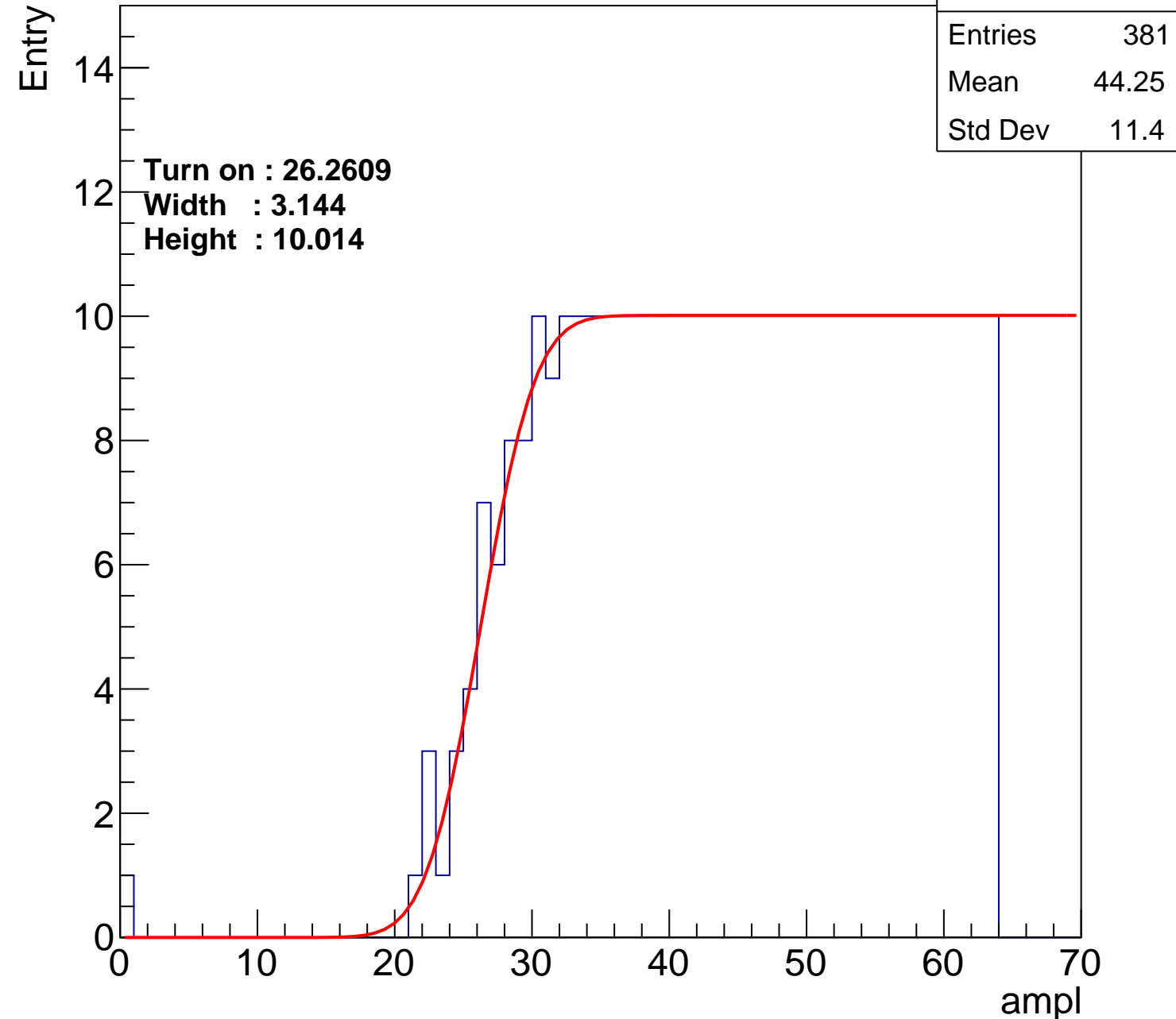
Width : 3.144

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch111

calib_packv5_042523_0143.root, FC#0, port D2

Entries	373
Mean	44.47
Std Dev	11.7

Turn on : 26.6673

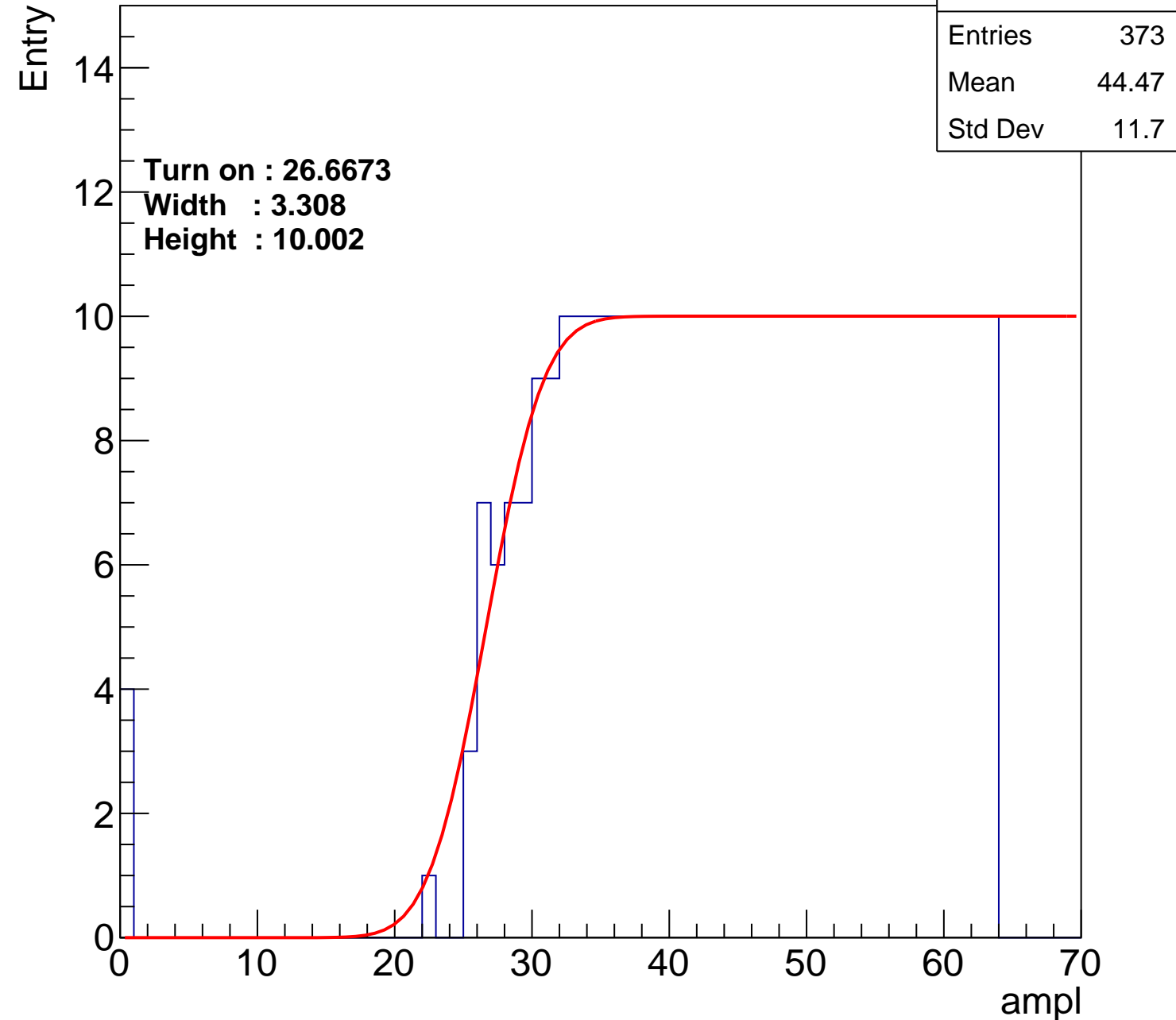
Width : 3.308

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch112

calib_packv5_042523_0143.root, FC#0, port D2

Entries	360
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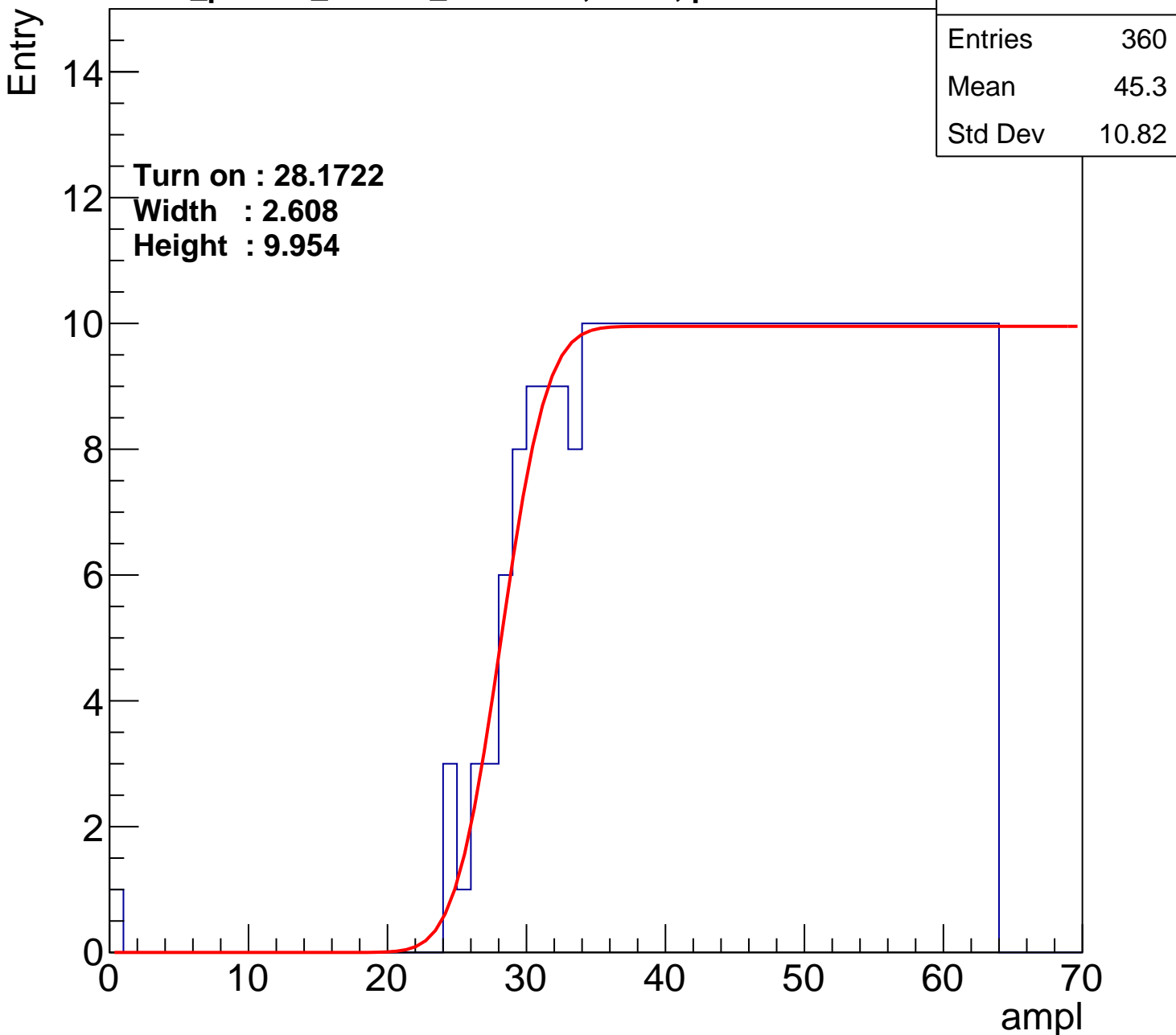
Mean	45.3
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Std Dev	10.82
---------	-------

Turn on : 28.1722

Width : 2.608

Height : 9.954



B1L101S, U10-ch113

calib_packv5_042523_0143.root, FC#0, port D2

Entries	381
Mean	44.15
Std Dev	11.72

Turn on : 26.4190

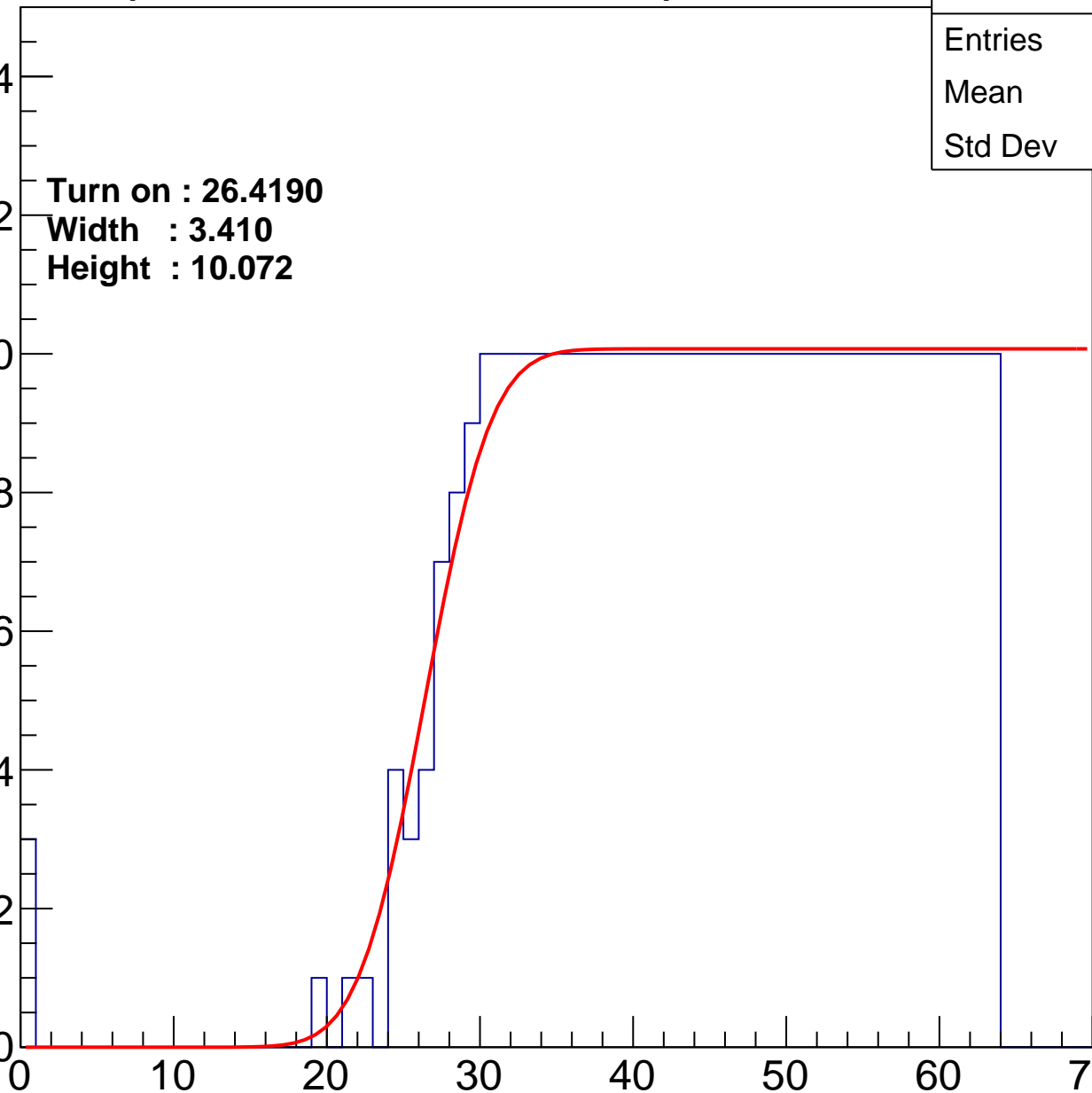
Width : 3.410

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch114

calib_packv5_042523_0143.root, FC#0, port D2

Entries	384
Mean	44.02
Std Dev	11.77

Turn on : 25.6461

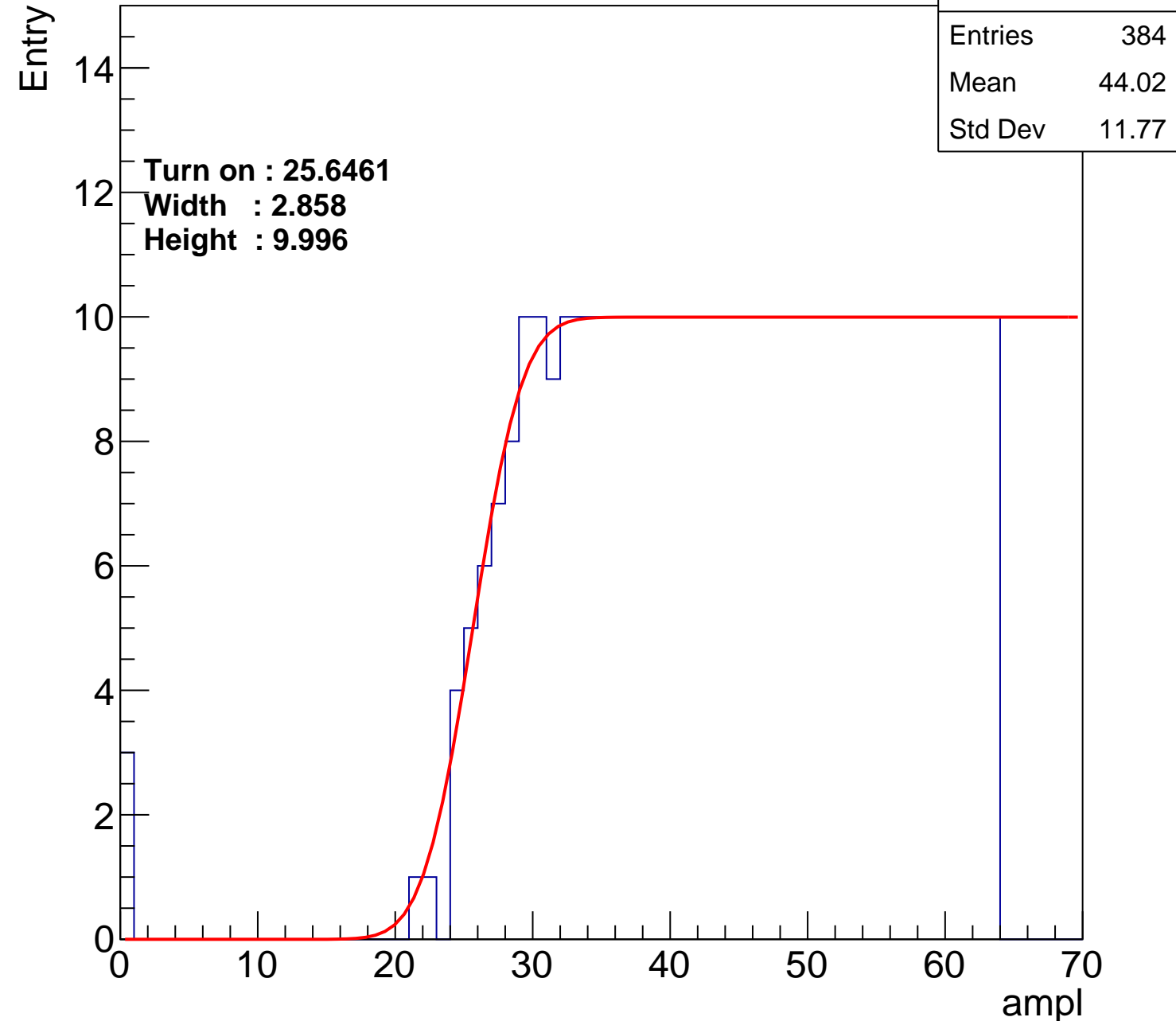
Width : 2.858

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch115

calib_packv5_042523_0143.root, FC#0, port D2

Entries	371
Mean	44.46
Std Dev	11.9

Turn on : 27.3226

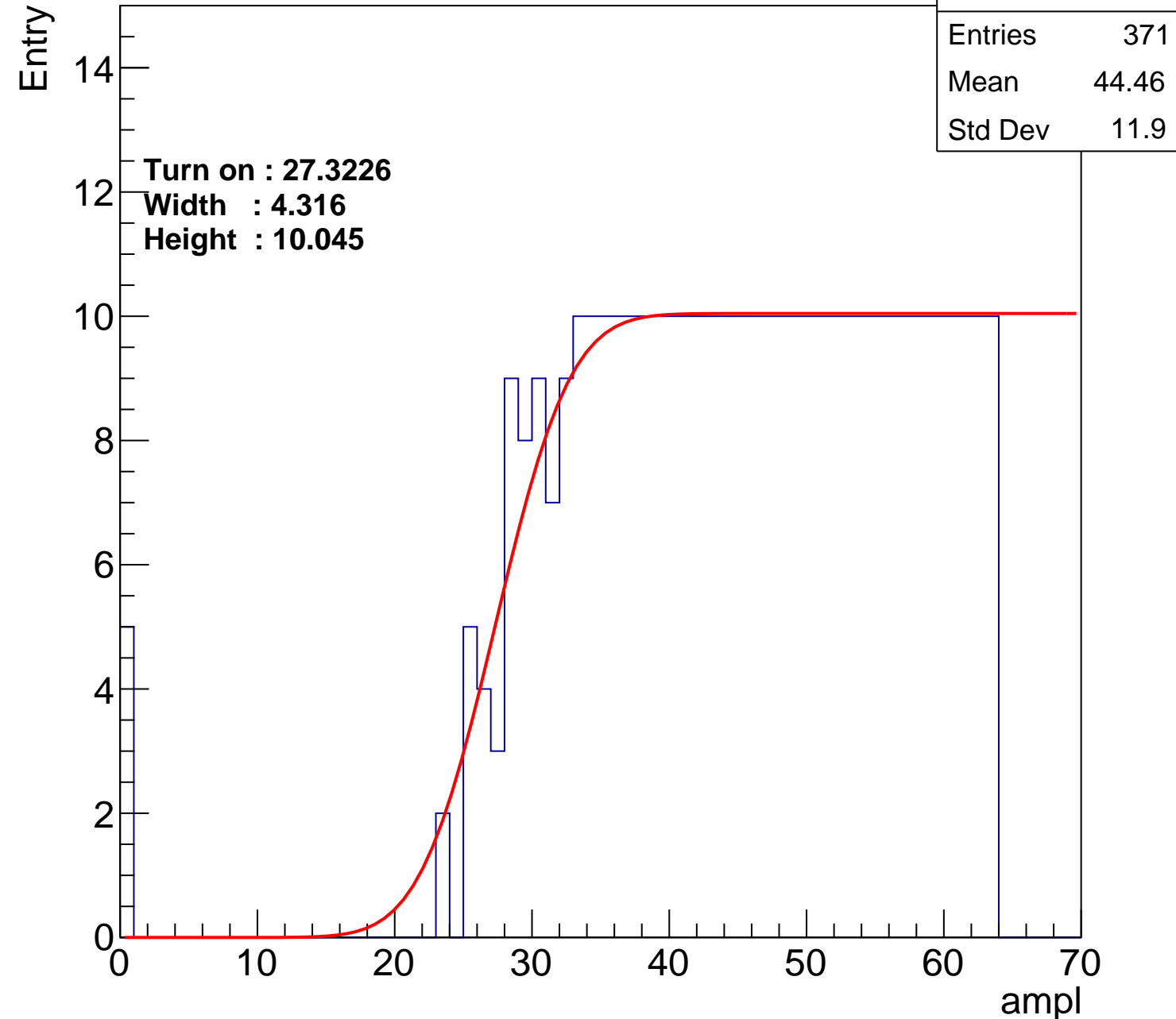
Width : 4.316

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch116

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.23
Std Dev	11.87

Turn on : 27.2032

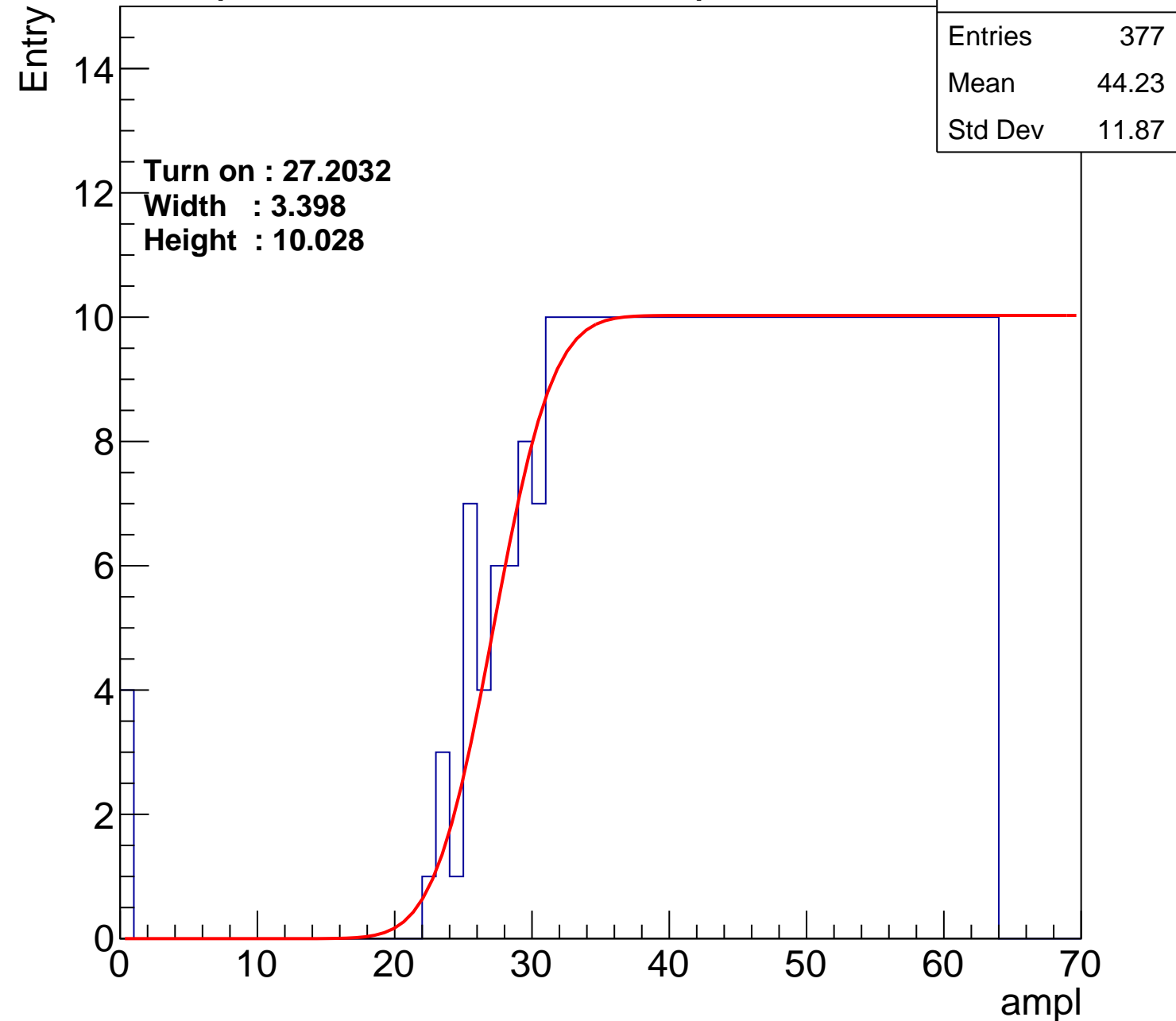
Width : 3.398

Height : 10.028

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch117

calib_packv5_042523_0143.root, FC#0, port D2

Entries	371
Mean	44.84
Std Dev	11.04

Turn on : 27.5094

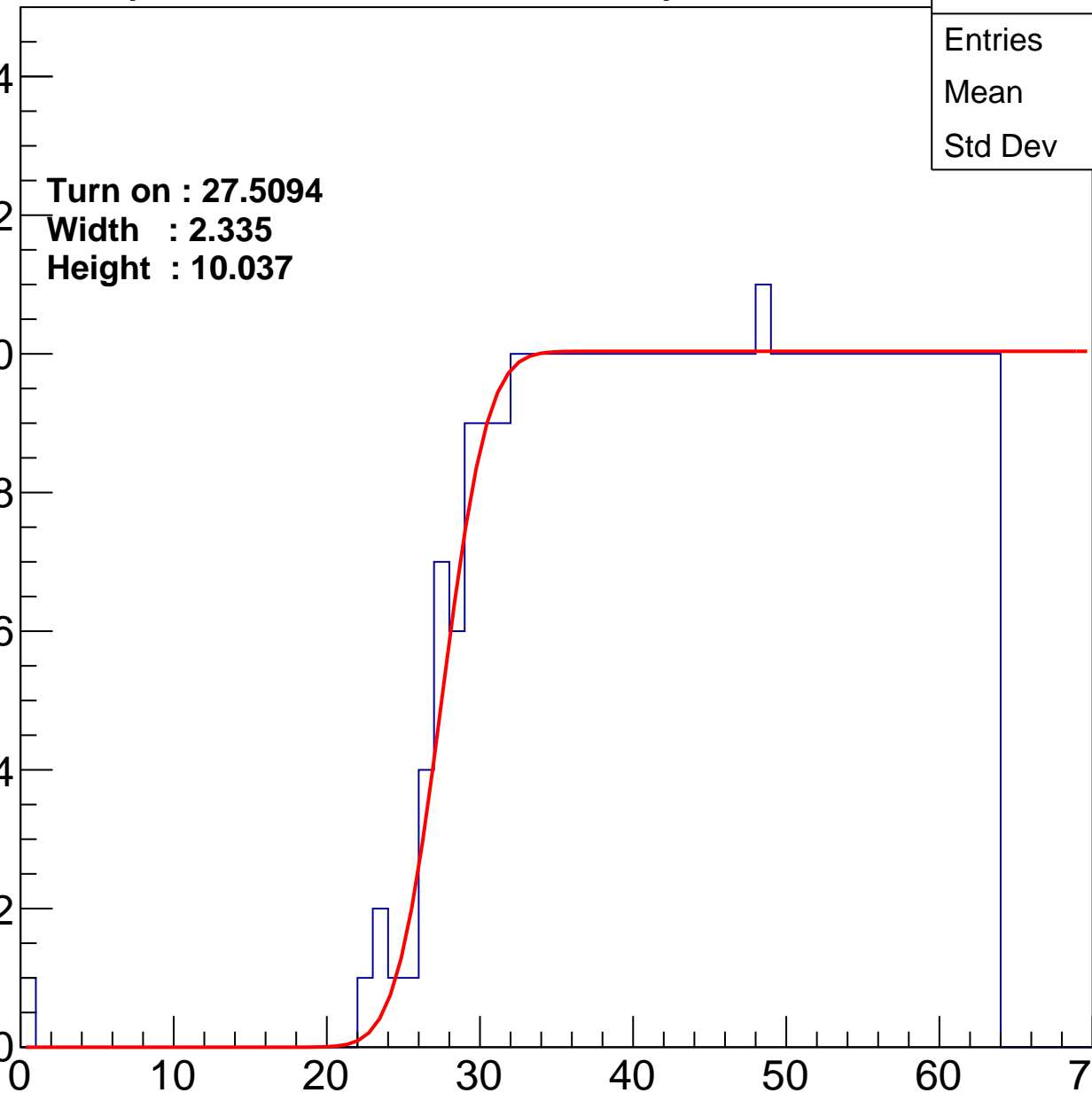
Width : 2.335

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch118

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.6
Std Dev	11.16

Turn on : 26.9256

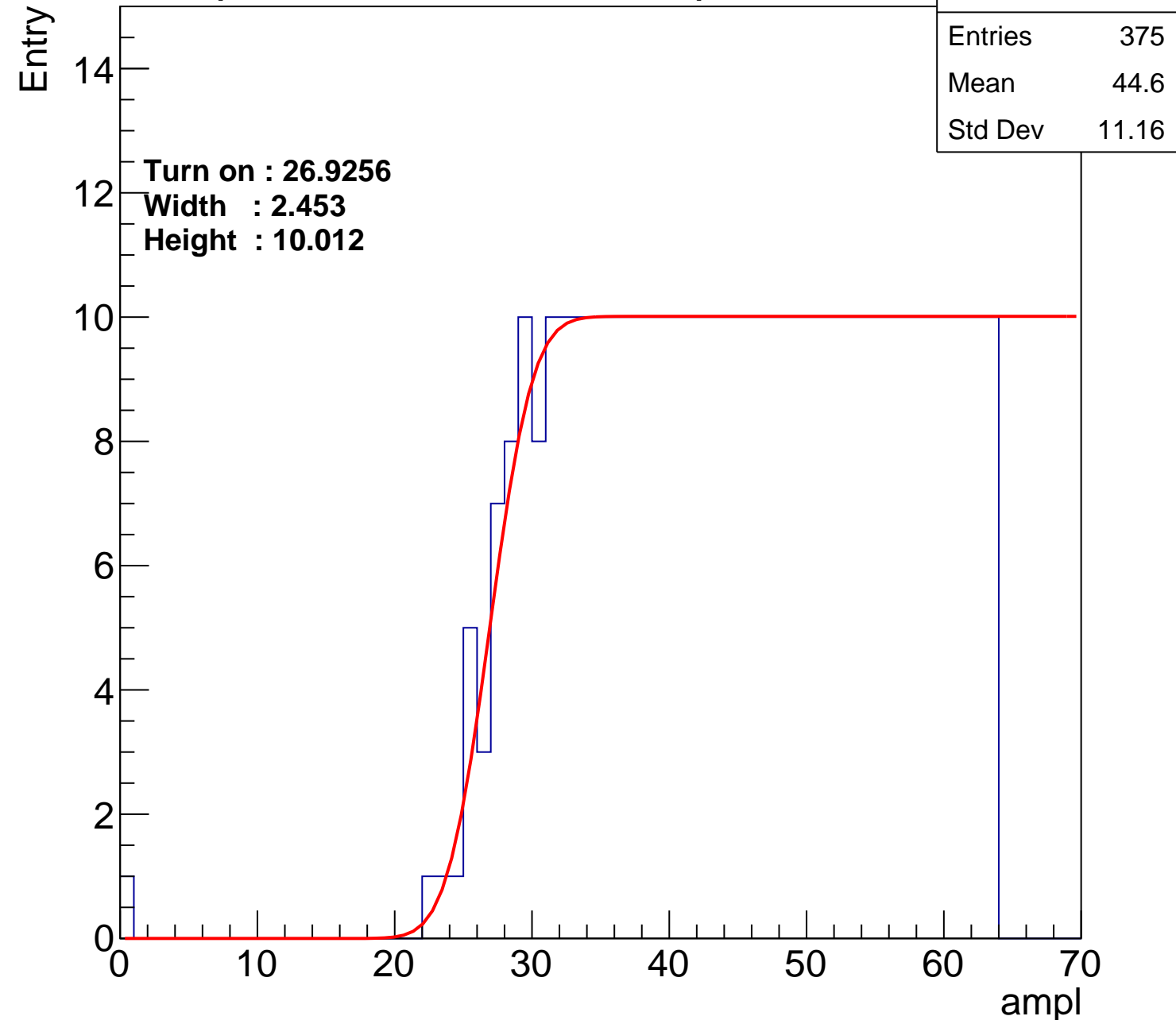
Width : 2.453

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch119

calib_packv5_042523_0143.root, FC#0, port D2

Entries	398
Mean	43.35
Std Dev	12.03

Turn on : 24.7654

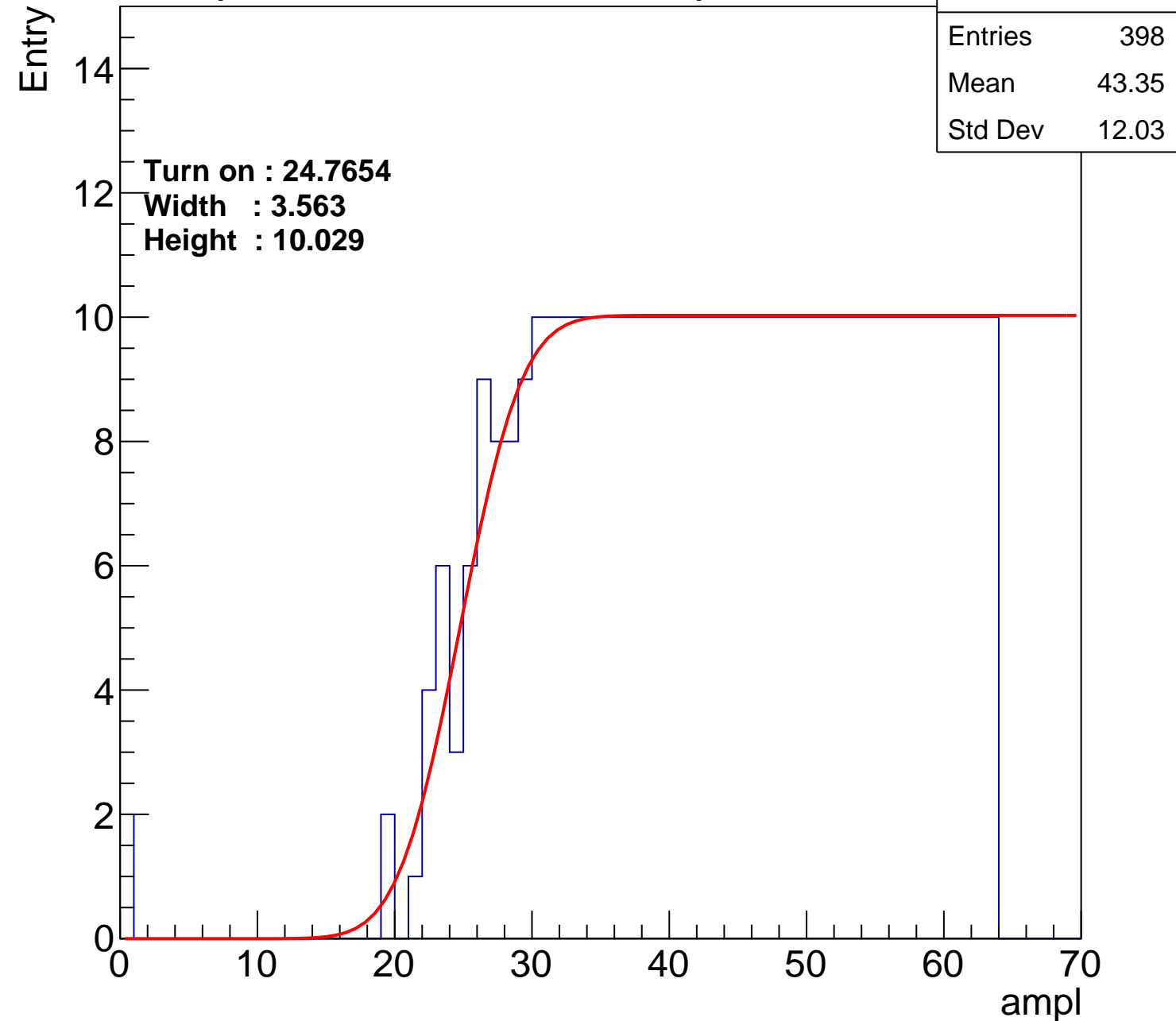
Width : 3.563

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch120

calib_packv5_042523_0143.root, FC#0, port D2

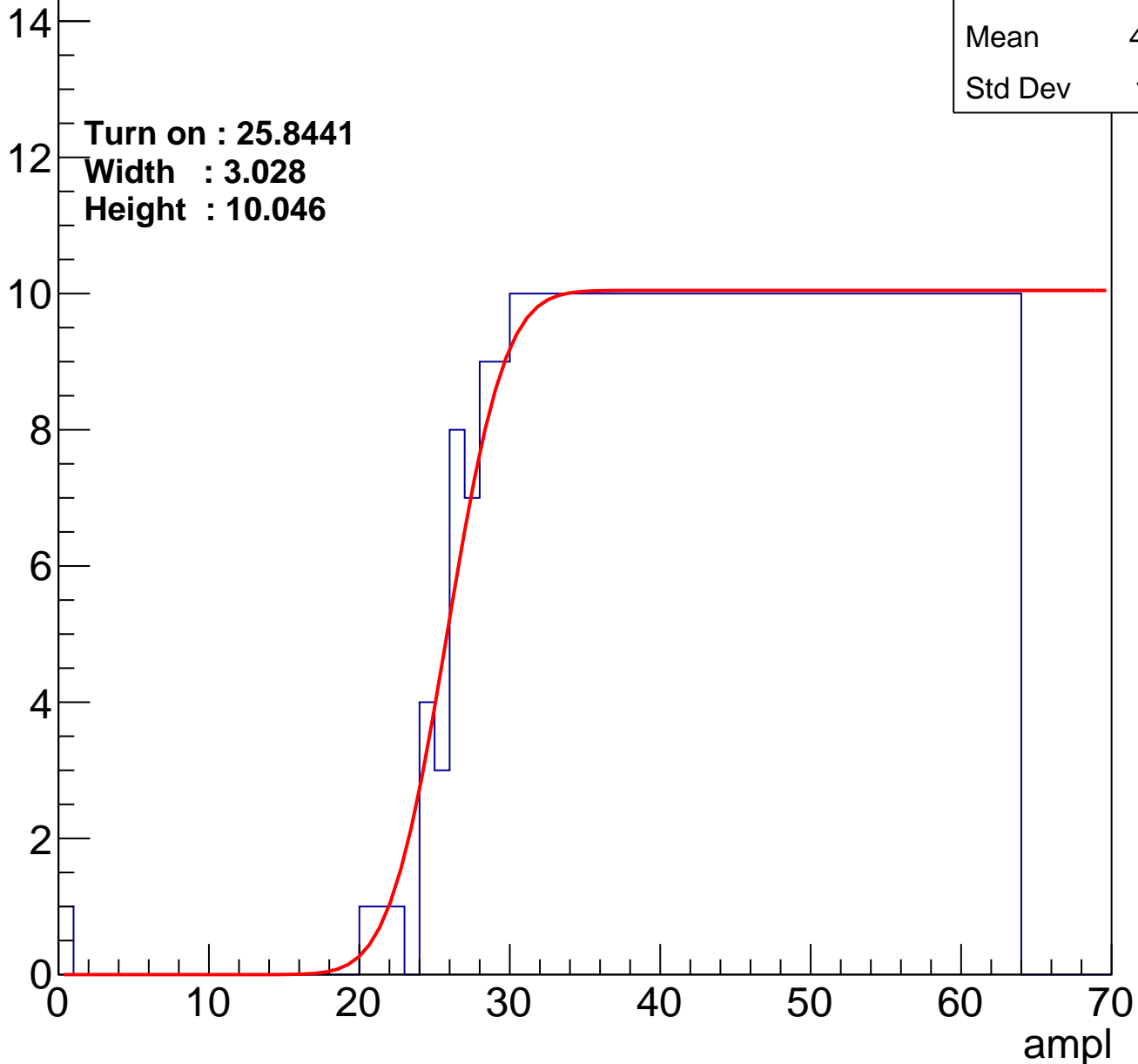
Entries	384
Mean	44.15
Std Dev	11.41

Turn on : 25.8441

Width : 3.028

Height : 10.046

Entry



B1L101S, U10-ch121

calib_packv5_042523_0143.root, FC#0, port D2

Entries	363
Mean	44.9
Std Dev	11.57

Turn on : 28.0641

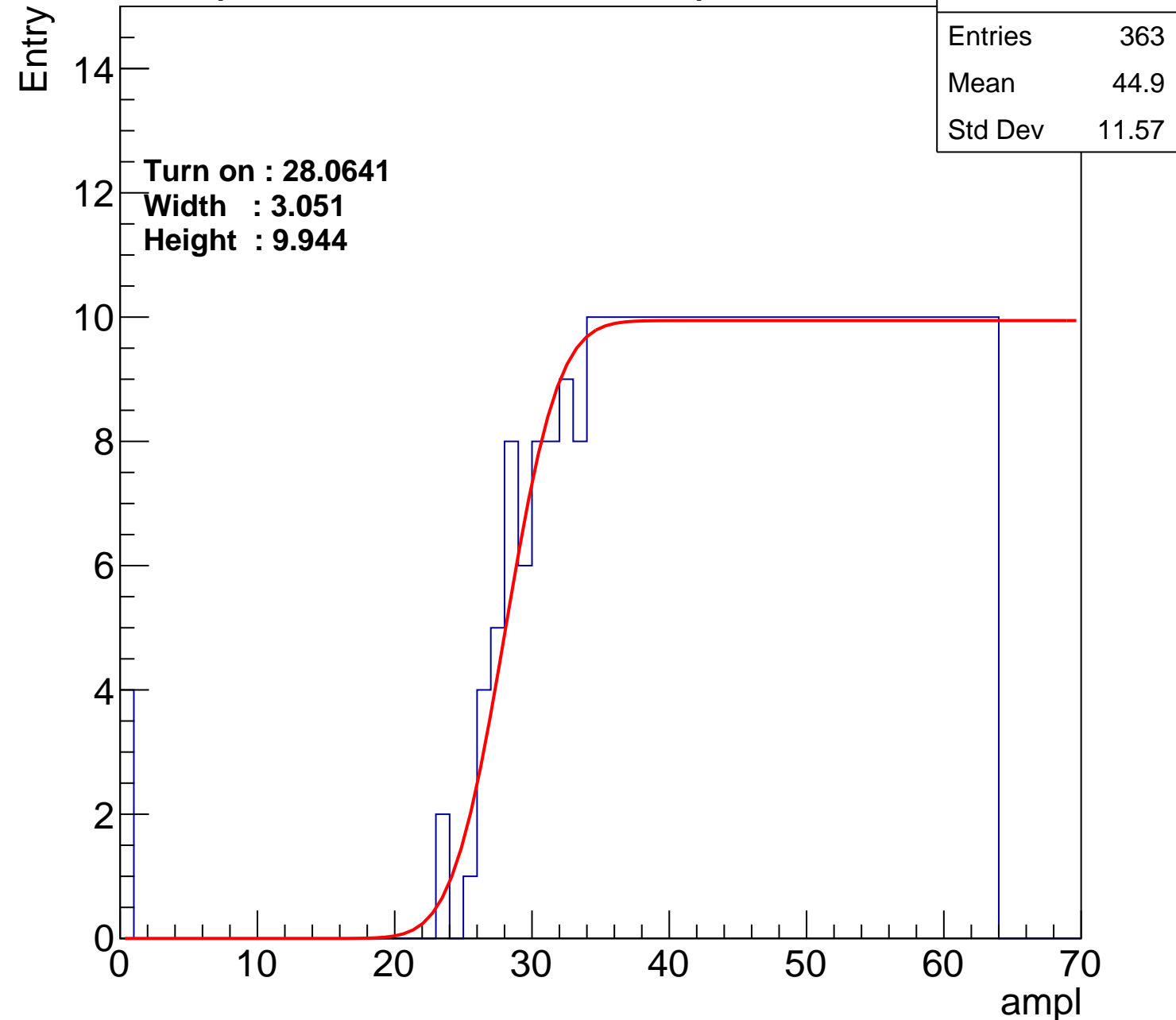
Width : 3.051

Height : 9.944

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch122

calib_packv5_042523_0143.root, FC#0, port D2

Entries	361
Mean	45.02
Std Dev	11.5

Turn on : 28.1491

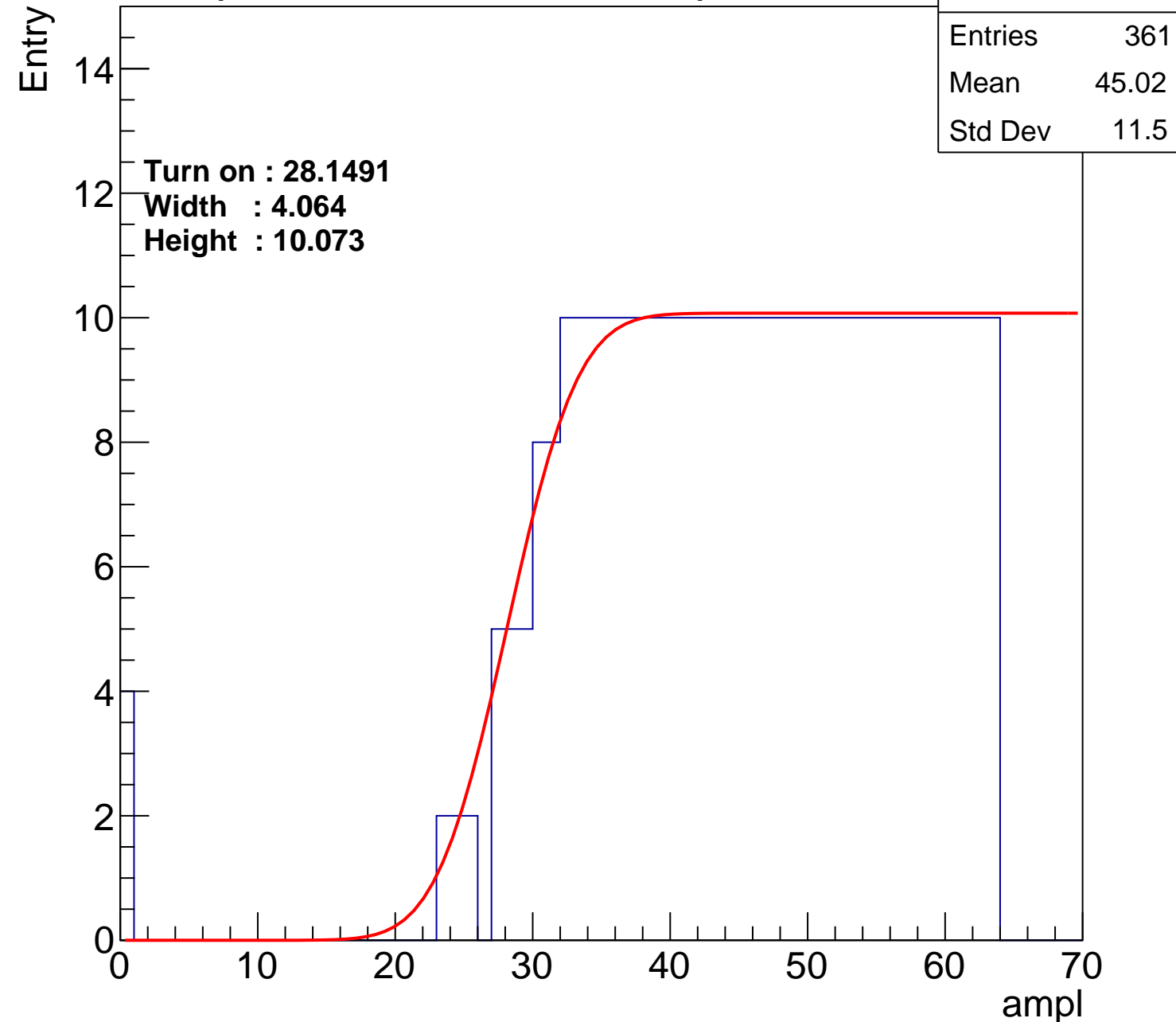
Width : 4.064

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch123

calib_packv5_042523_0143.root, FC#0, port D2

Entries	355
Mean	45.45
Std Dev	10.96

Turn on : 28.9753

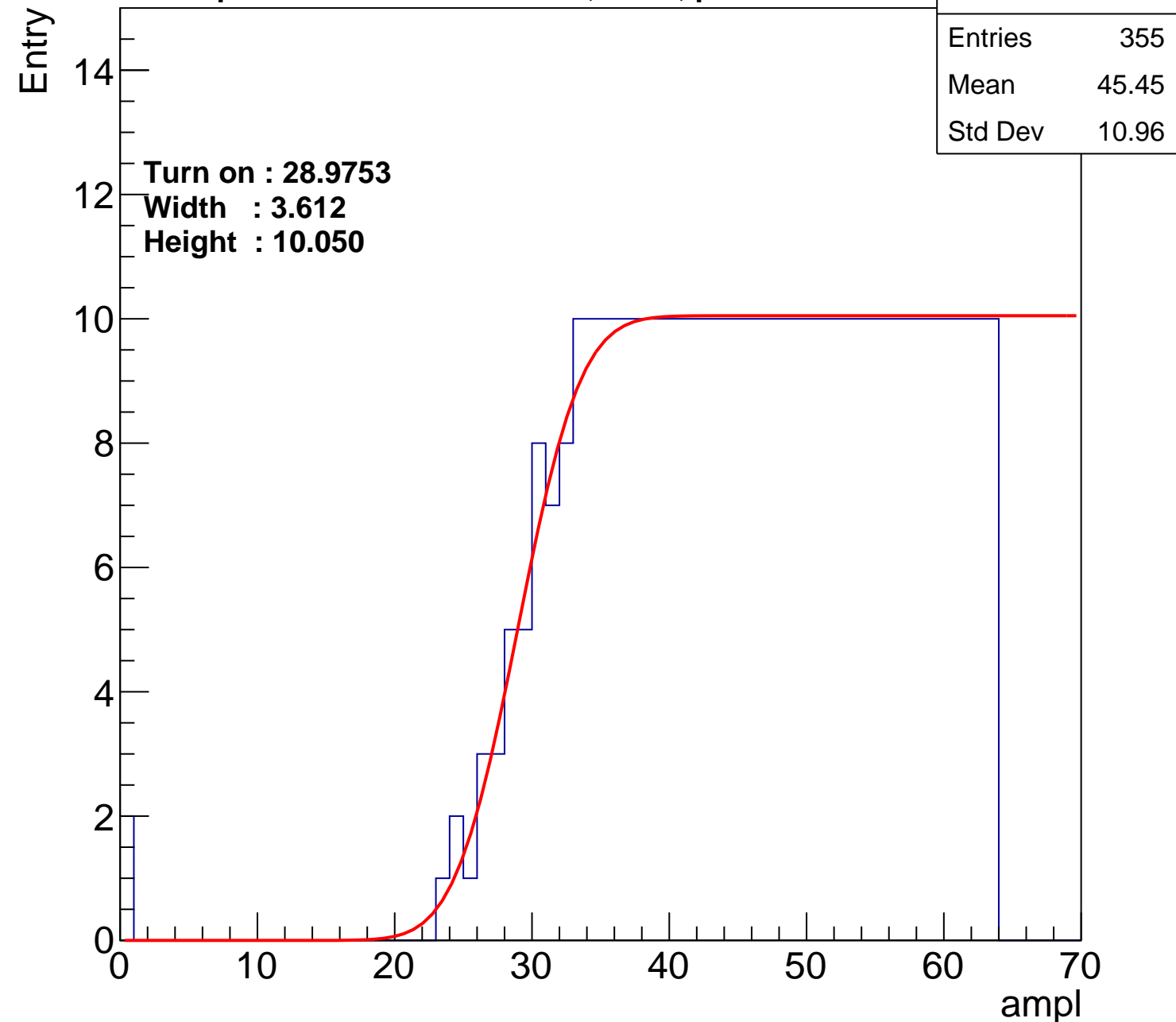
Width : 3.612

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch124

calib_packv5_042523_0143.root, FC#0, port D2

Entries	384
Mean	44.04
Std Dev	11.66

Turn on : 25.8326

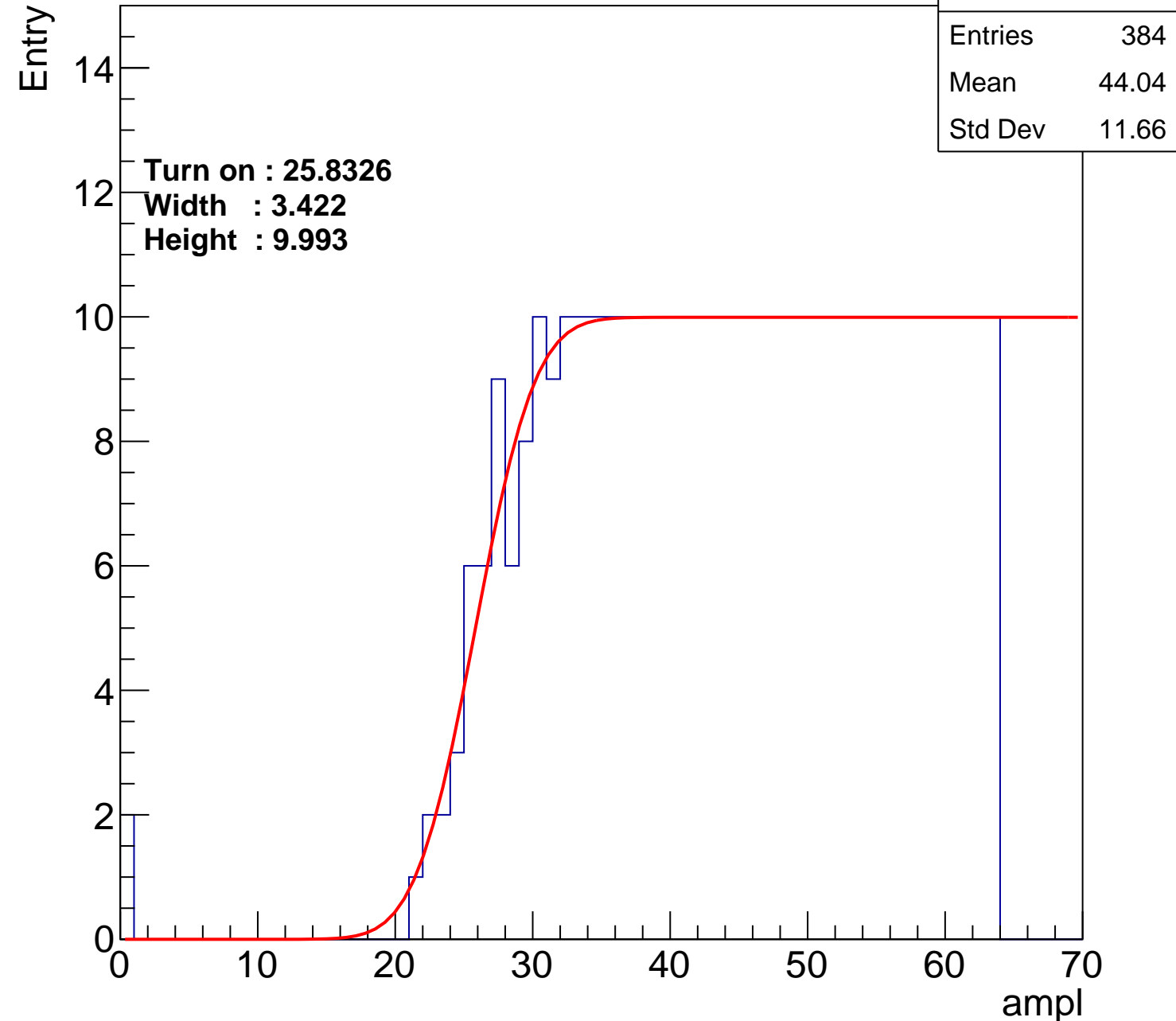
Width : 3.422

Height : 9.993

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch125

calib_packv5_042523_0143.root, FC#0, port D2

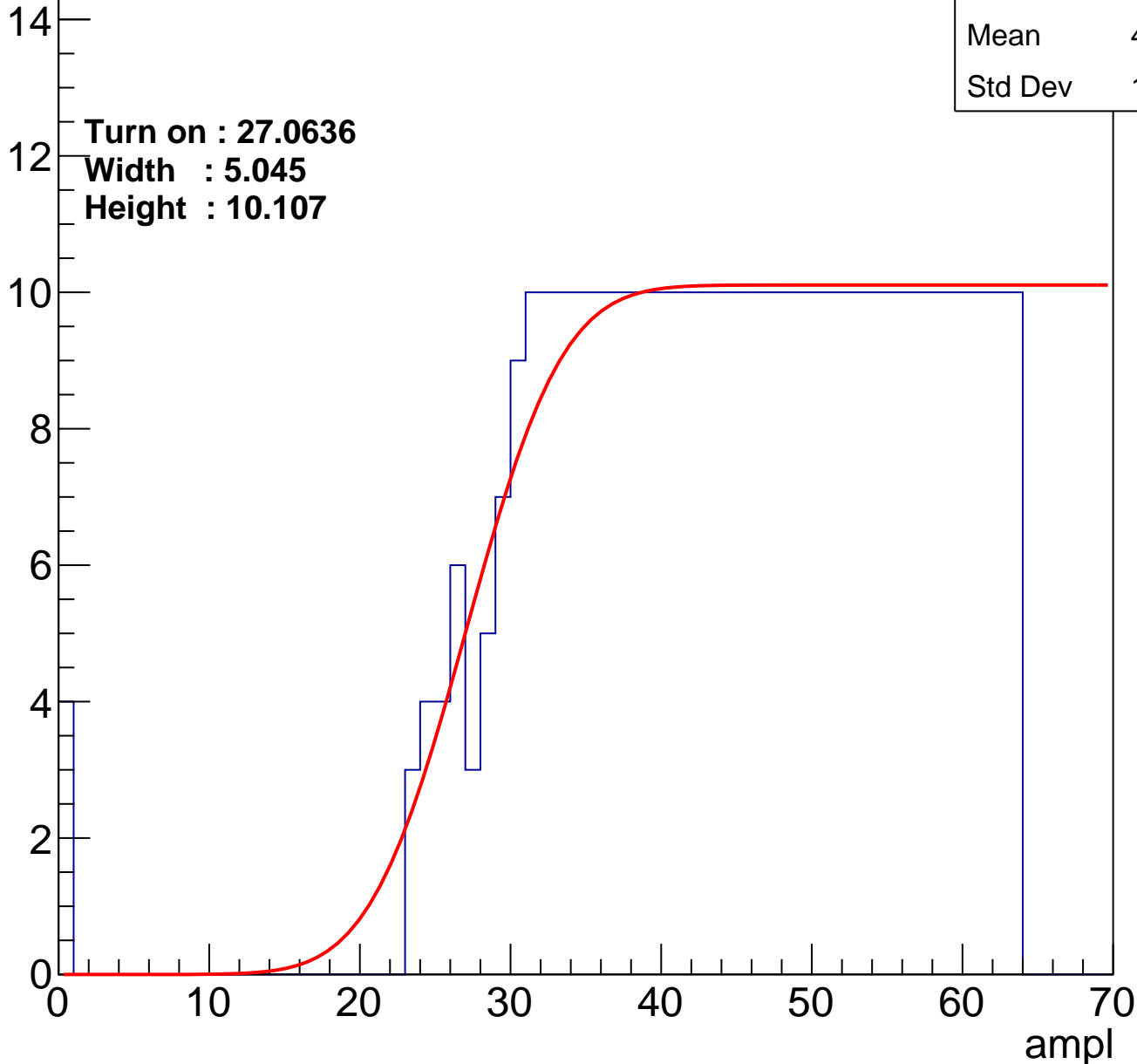
Entries	375
Mean	44.33
Std Dev	11.82

Turn on : 27.0636

Width : 5.045

Height : 10.107

Entry



B1L101S, U10-ch126

calib_packv5_042523_0143.root, FC#0, port D2

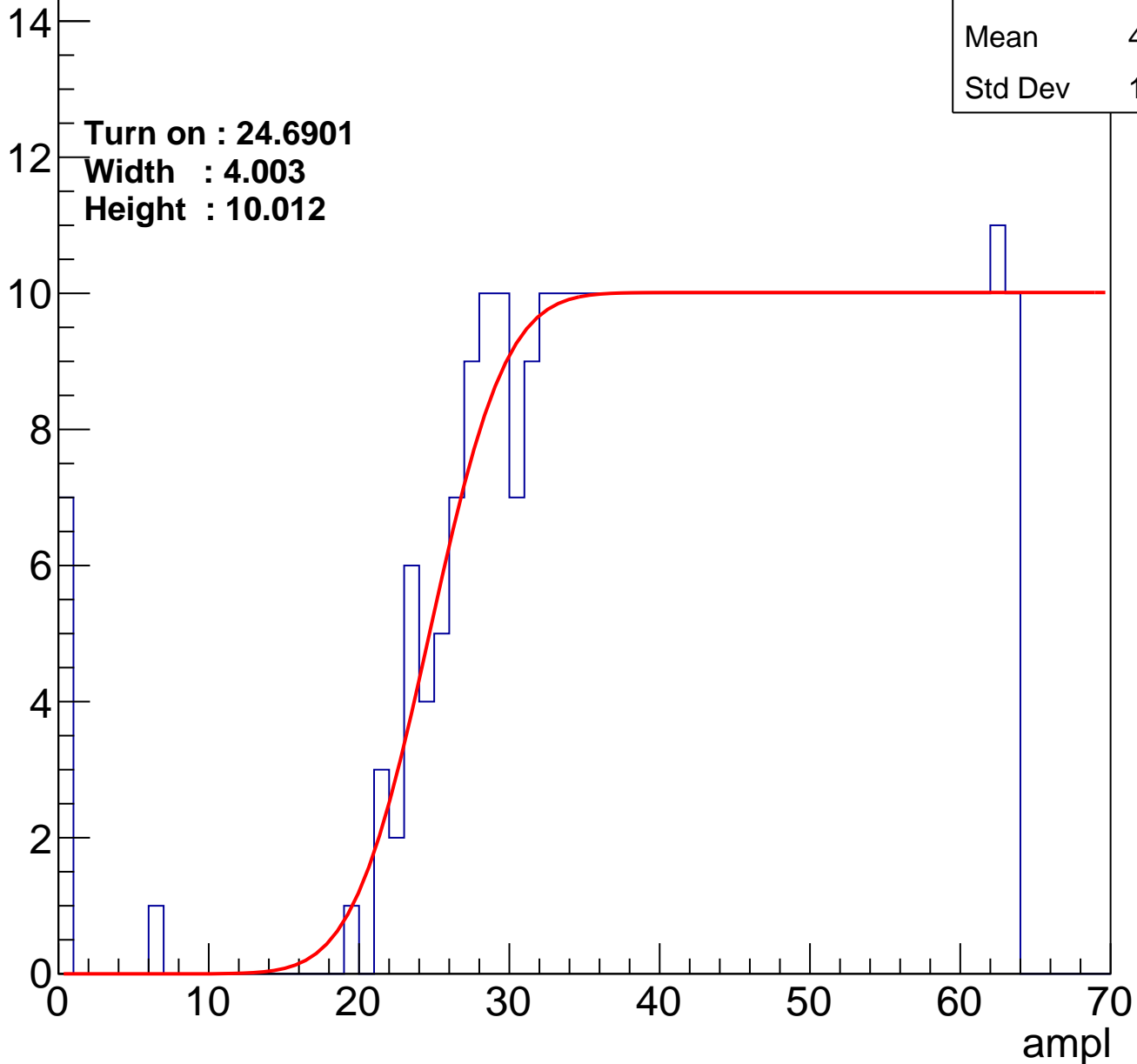
Entries	402
Mean	42.88
Std Dev	12.99

Turn on : 24.6901

Width : 4.003

Height : 10.012

Entry



B1L101S, U10-ch127

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.29
Std Dev	11.71

Turn on : 27.4578

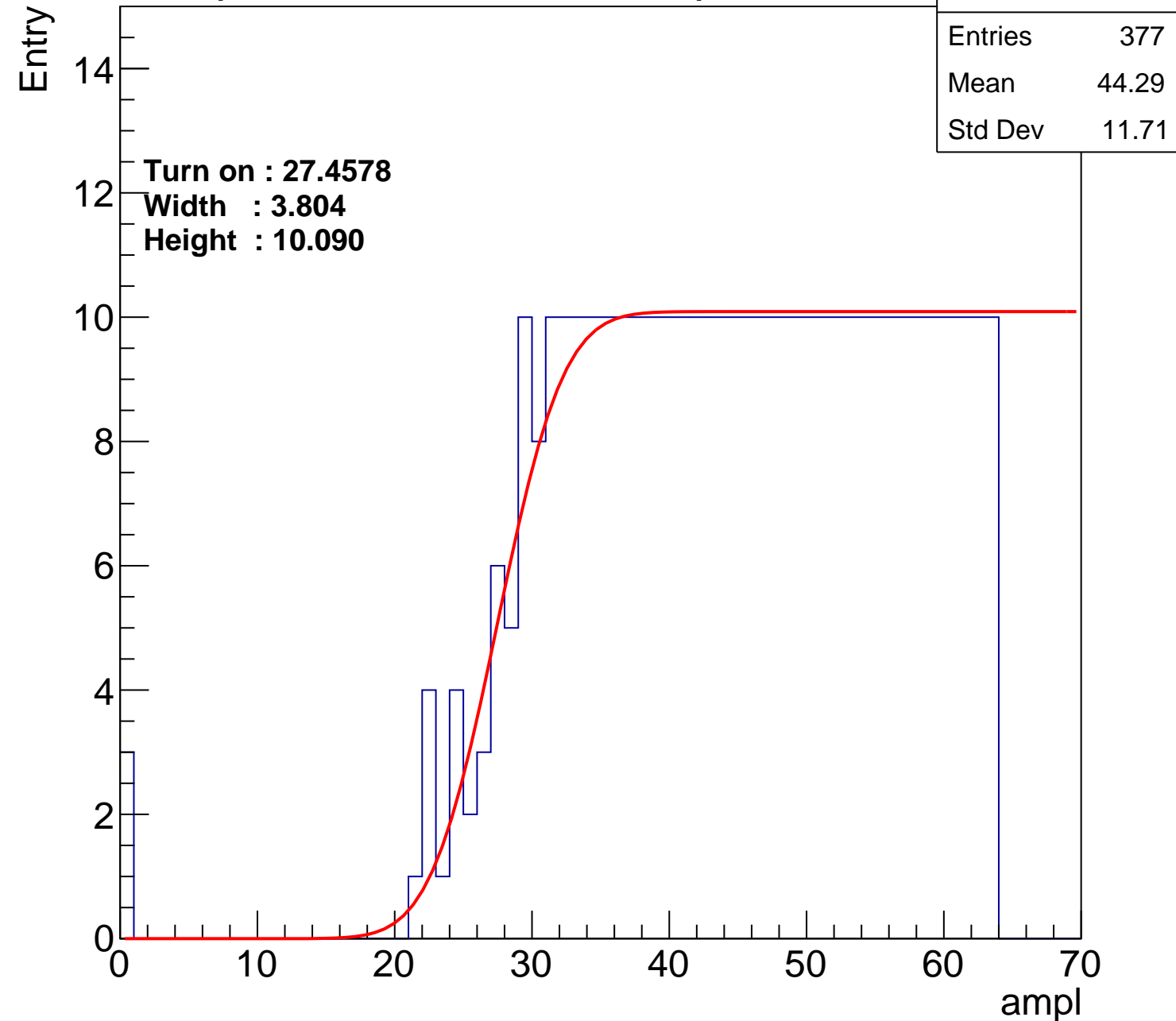
Width : 3.804

Height : 10.090

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U10-ch127

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.29
Std Dev	11.71

Turn on : 27.4578

Width : 3.804

Height : 10.090

Entry

14
12
10
8
6
4
2
0

ampl

