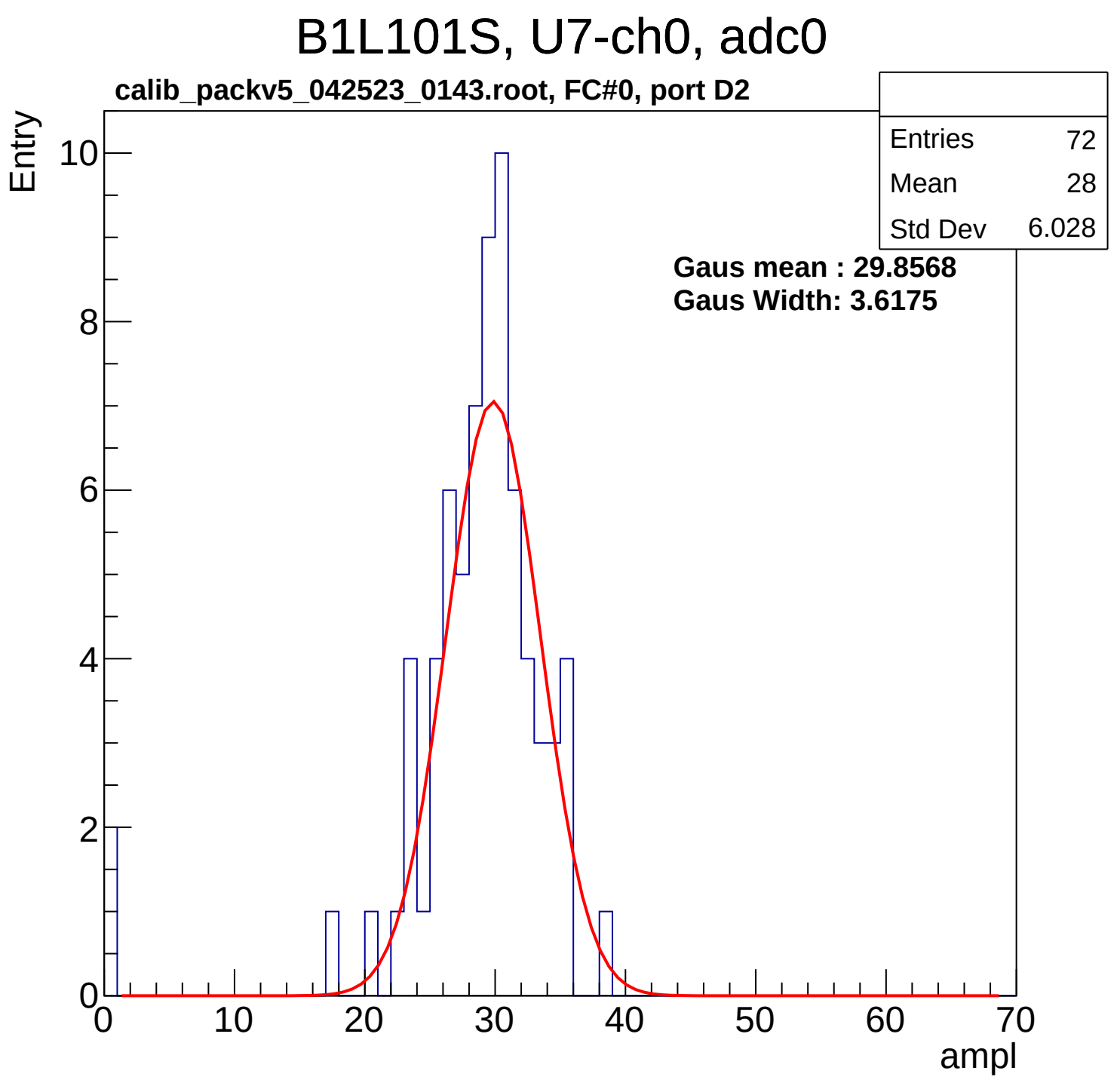
B1L101S, U7-ch0, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 28
Std Dev 6.028
Gaus mean : 29.8568
Gaus Width: 3.6175
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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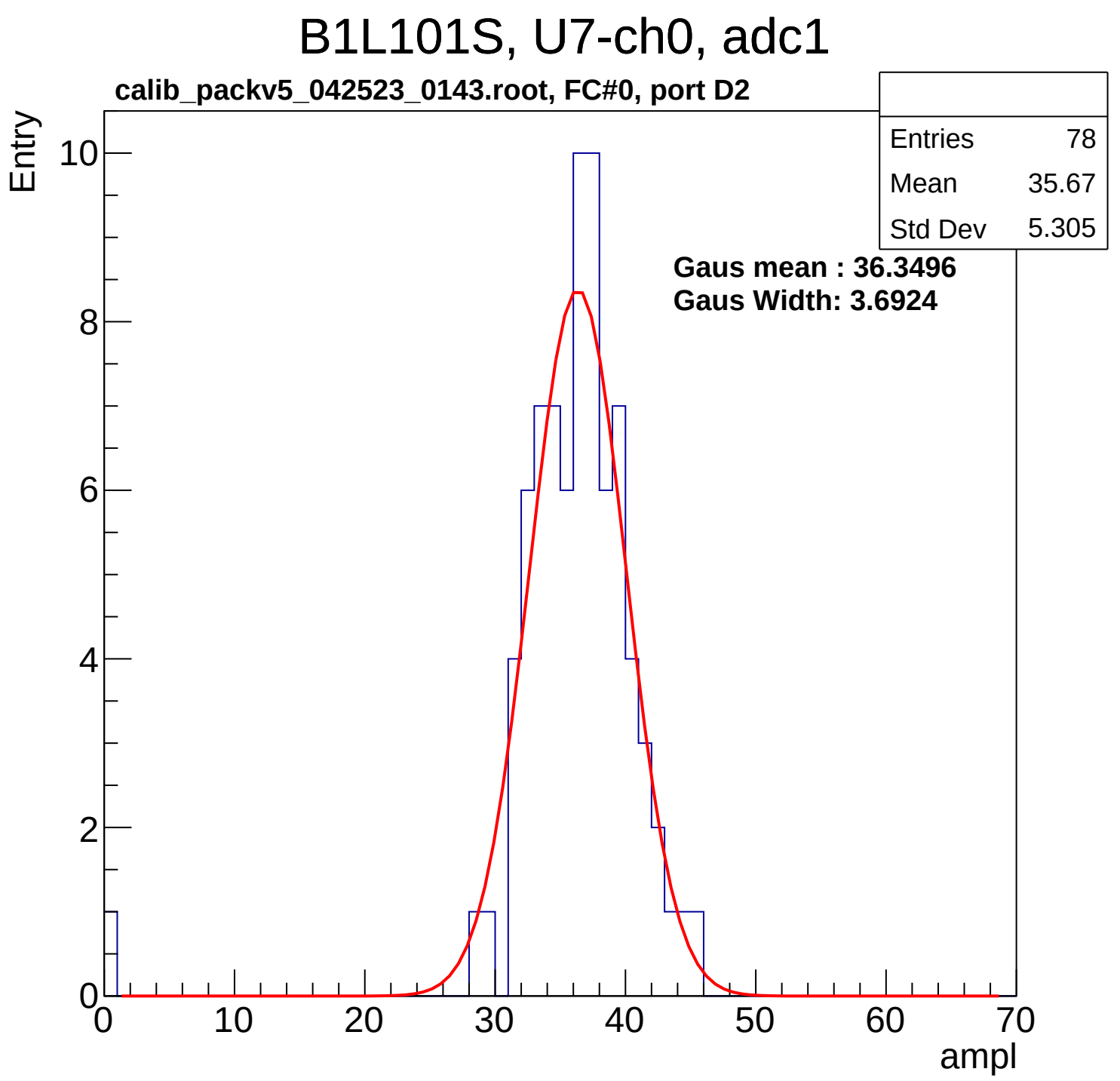
B1L101S, U7-ch0, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 35.67
Std Dev 5.305
Gaus mean : 36.3496
Gaus Width: 3.6924
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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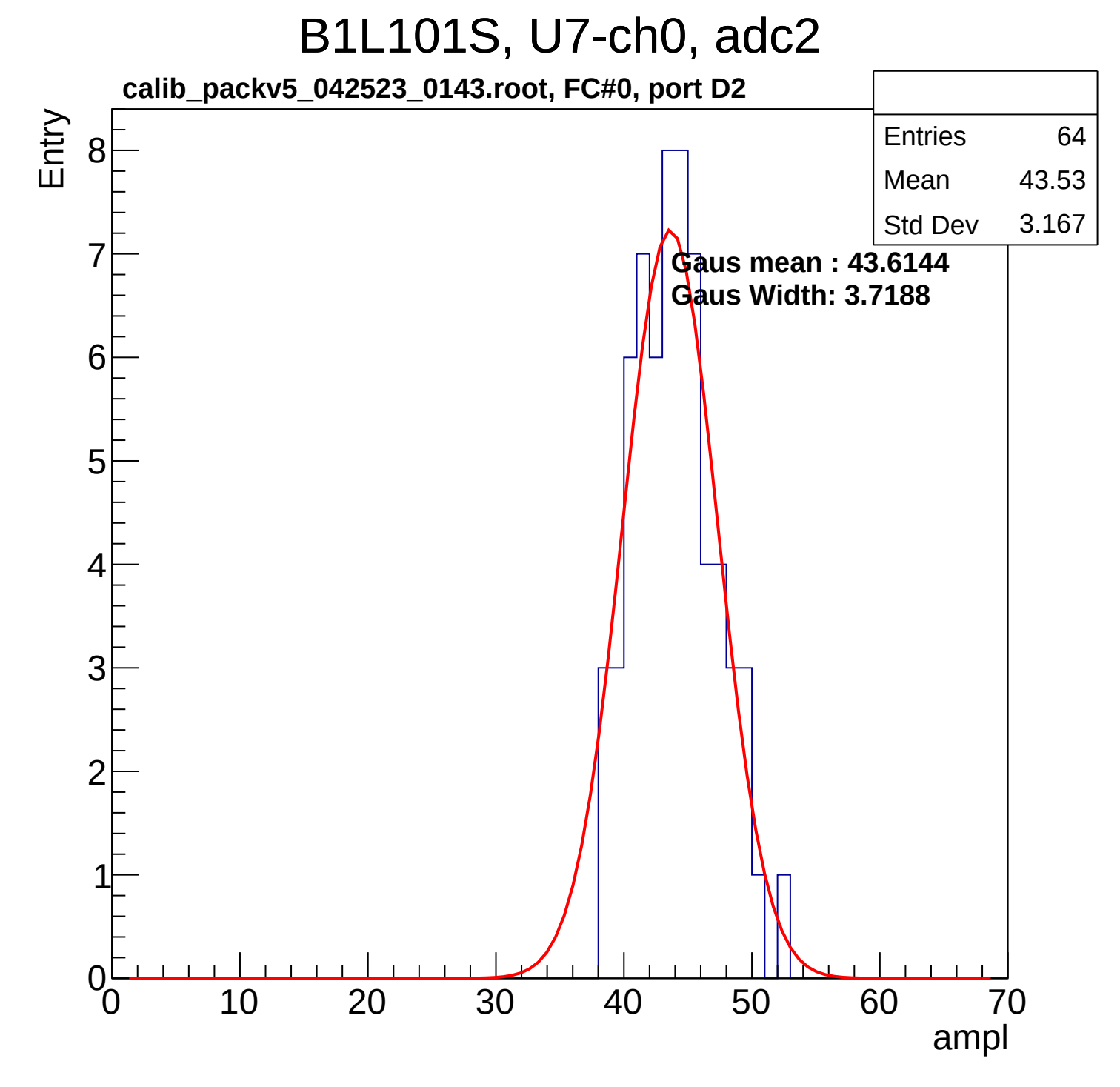
B1L101S, U7-ch0, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 43.53
Std Dev 3.167
Gaus mean : 43.6144
Gaus Width: 3.7188
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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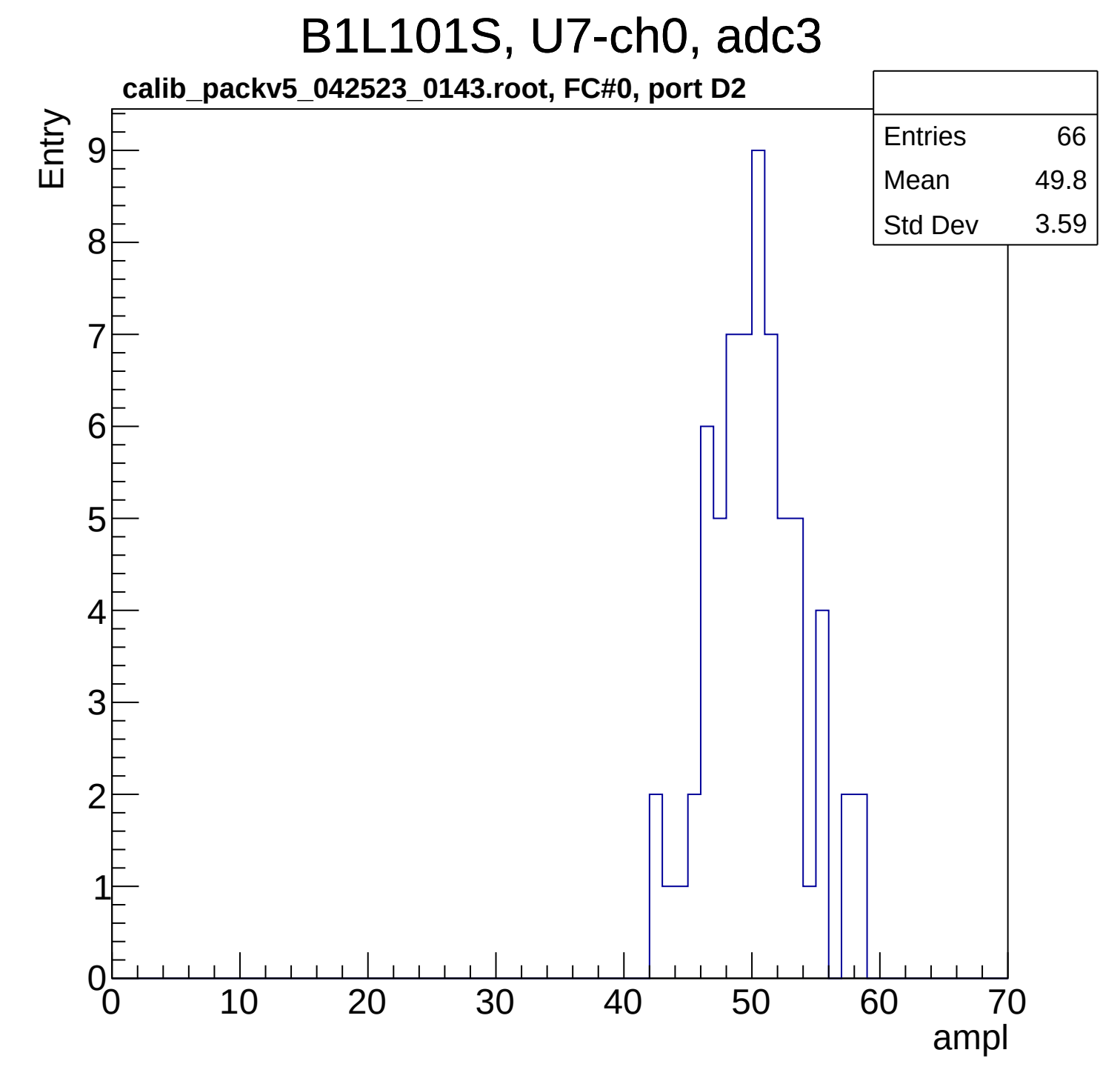
B1L101S, U7-ch0, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 49.8
Std Dev 3.59
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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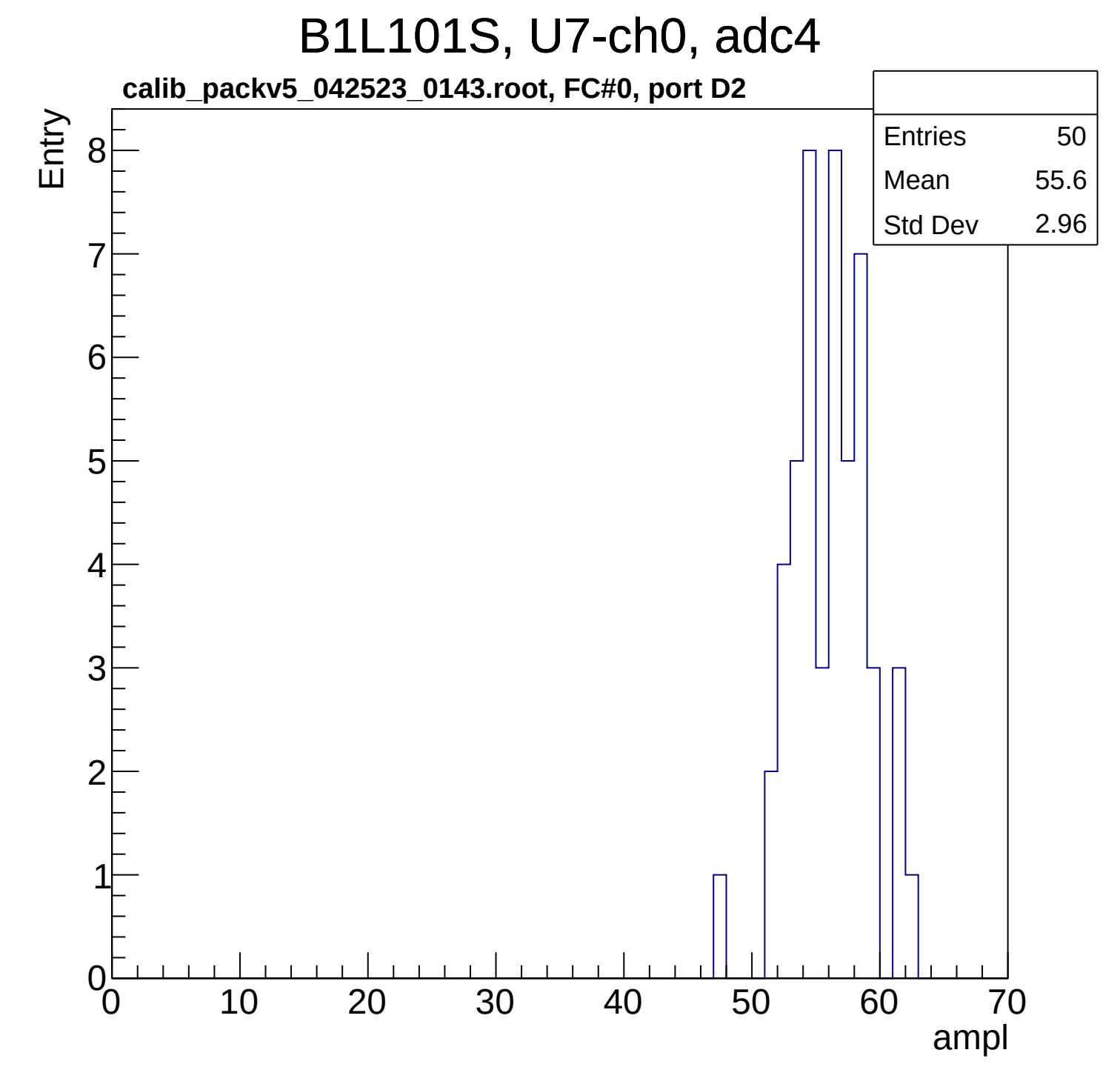
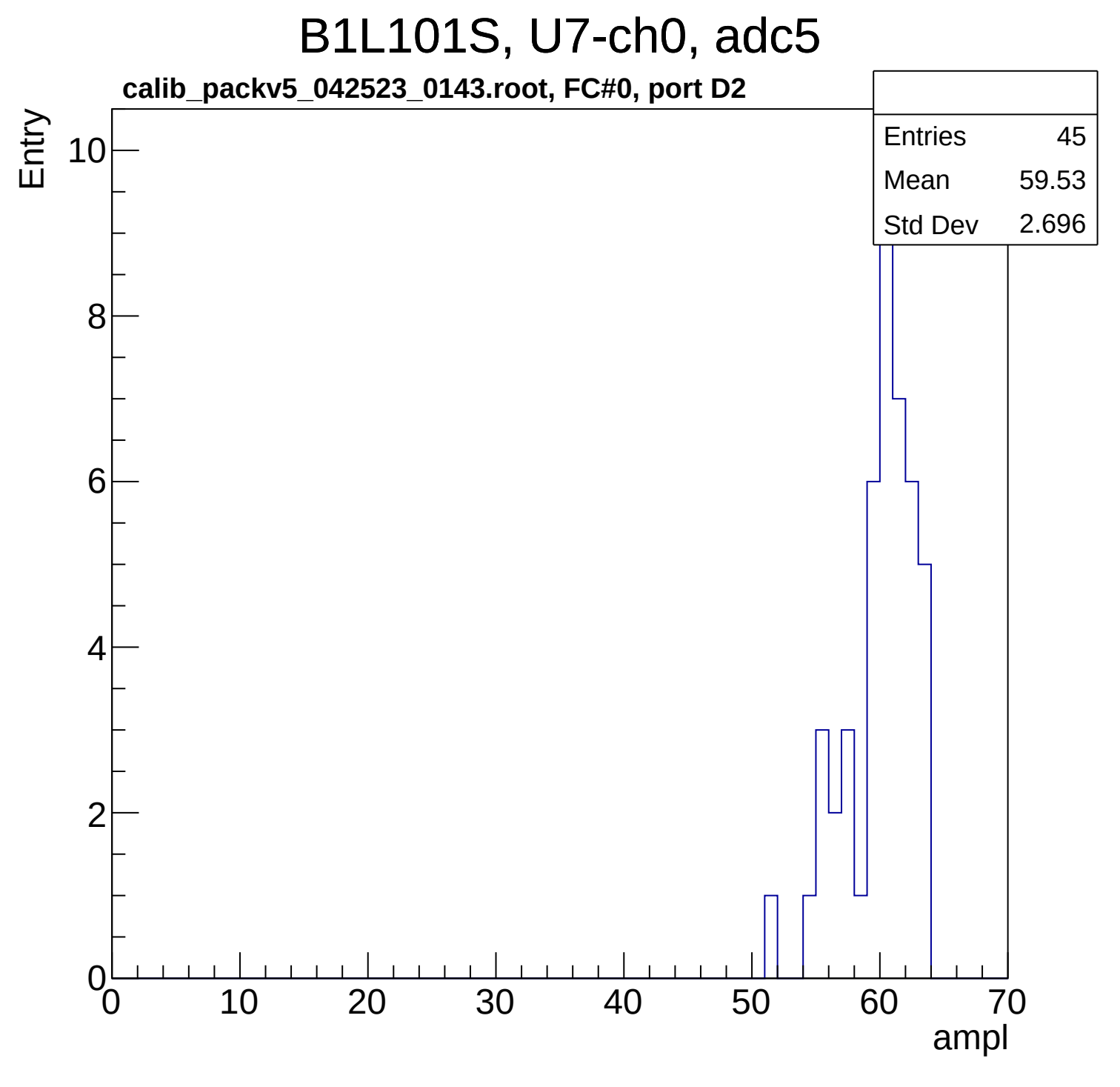

B1L101S, U7-ch0, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 55.6
Std Dev 2.96
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch0, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 59.53
Std Dev 2.696
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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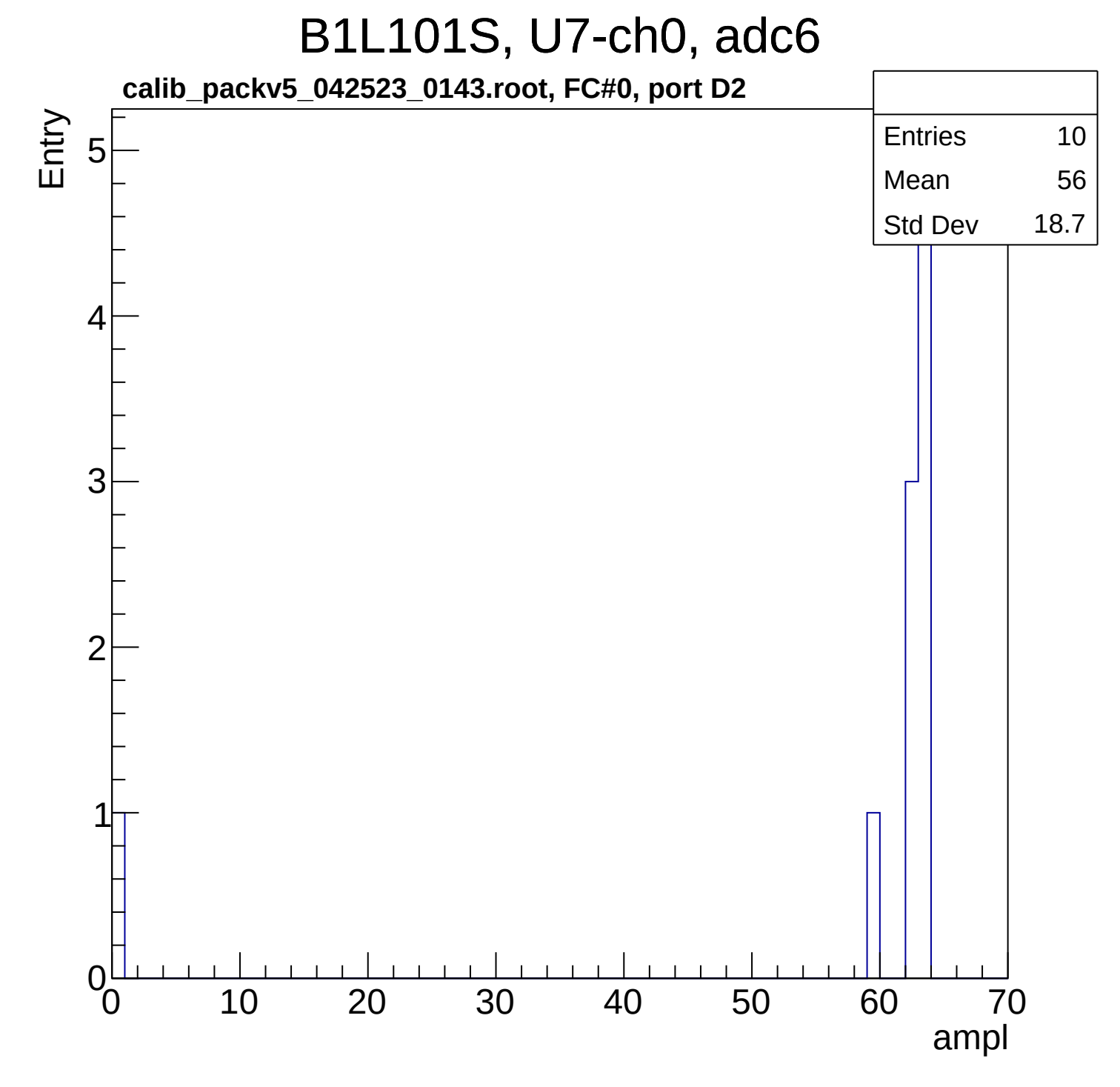
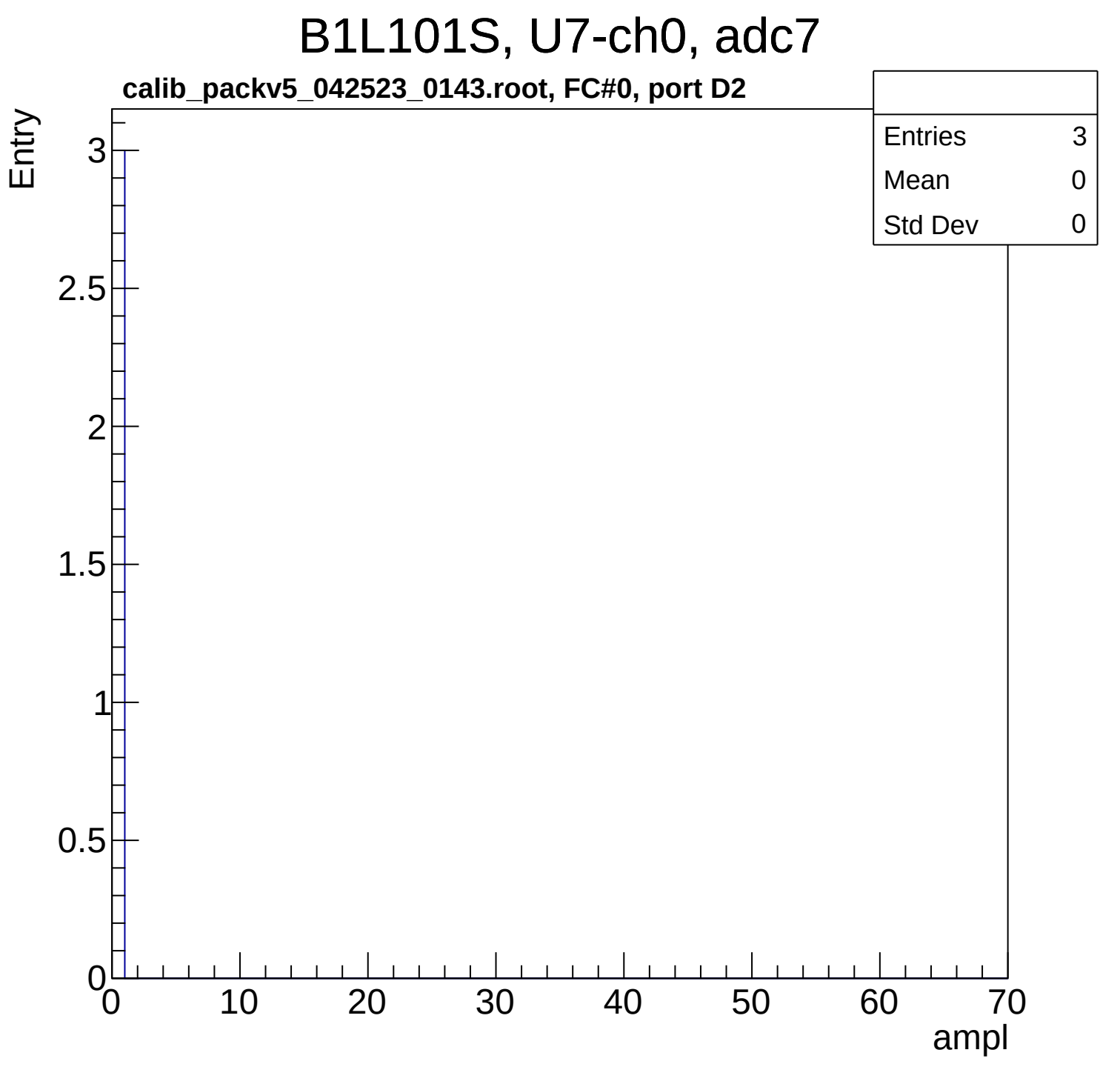
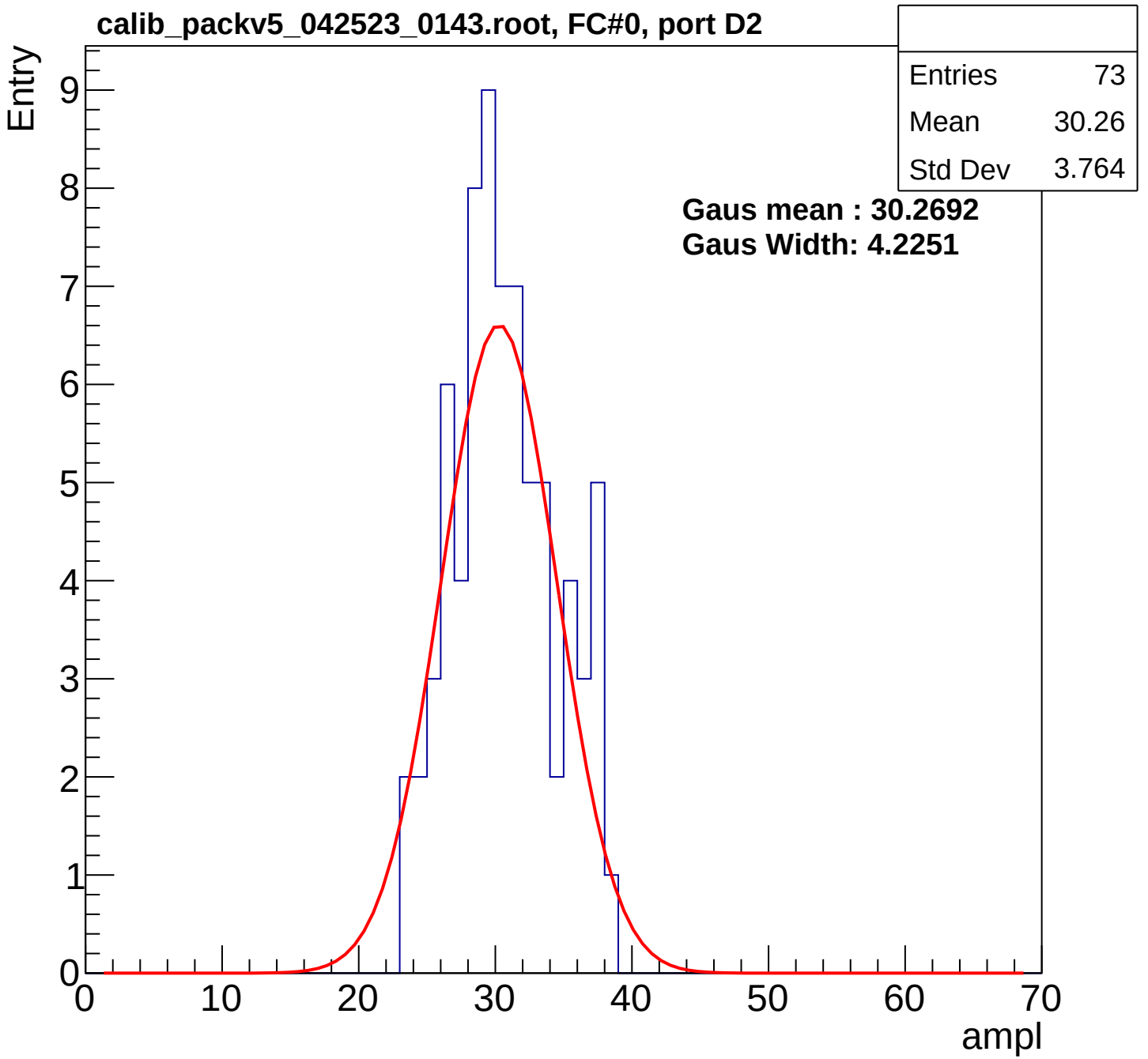
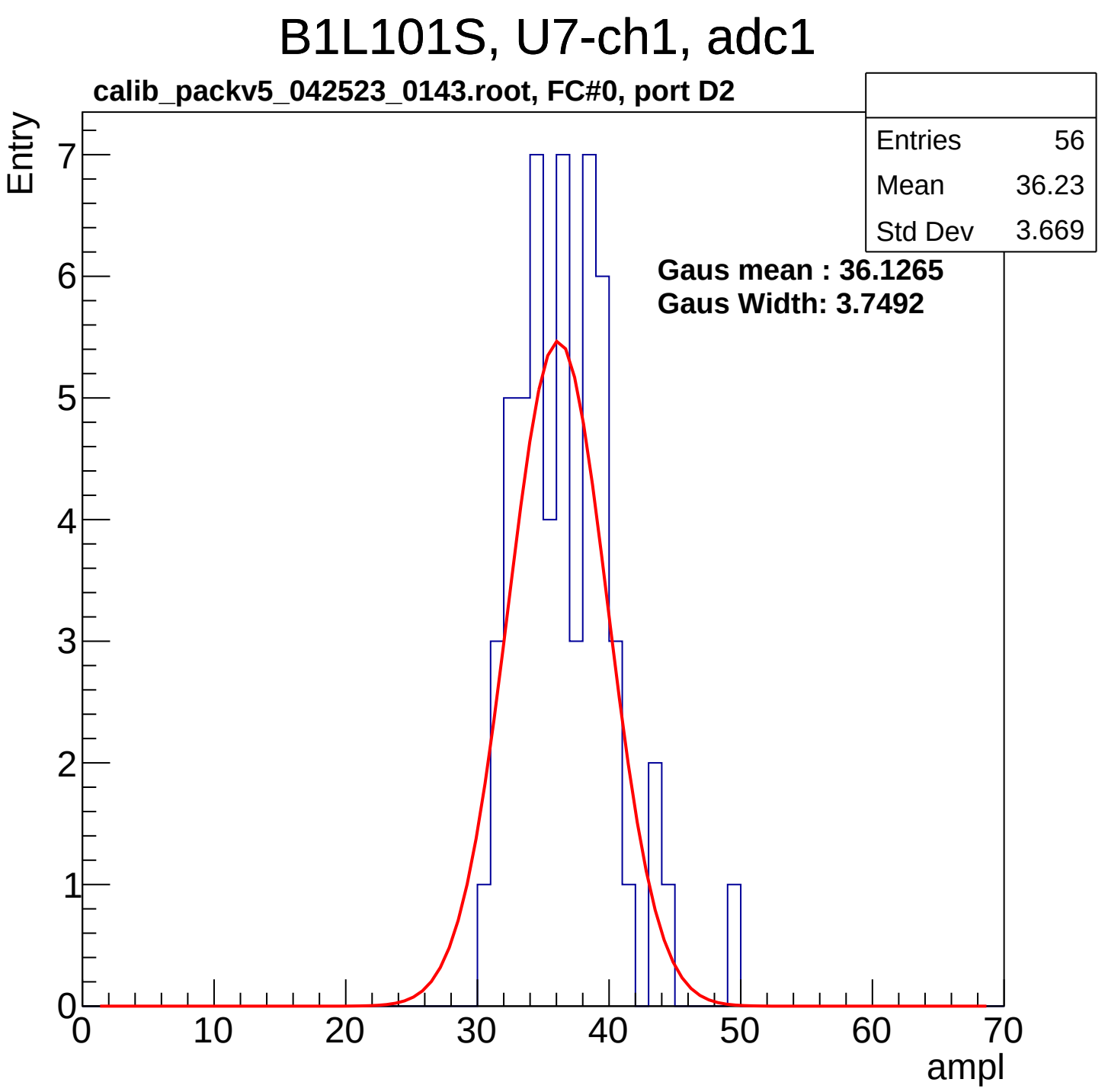
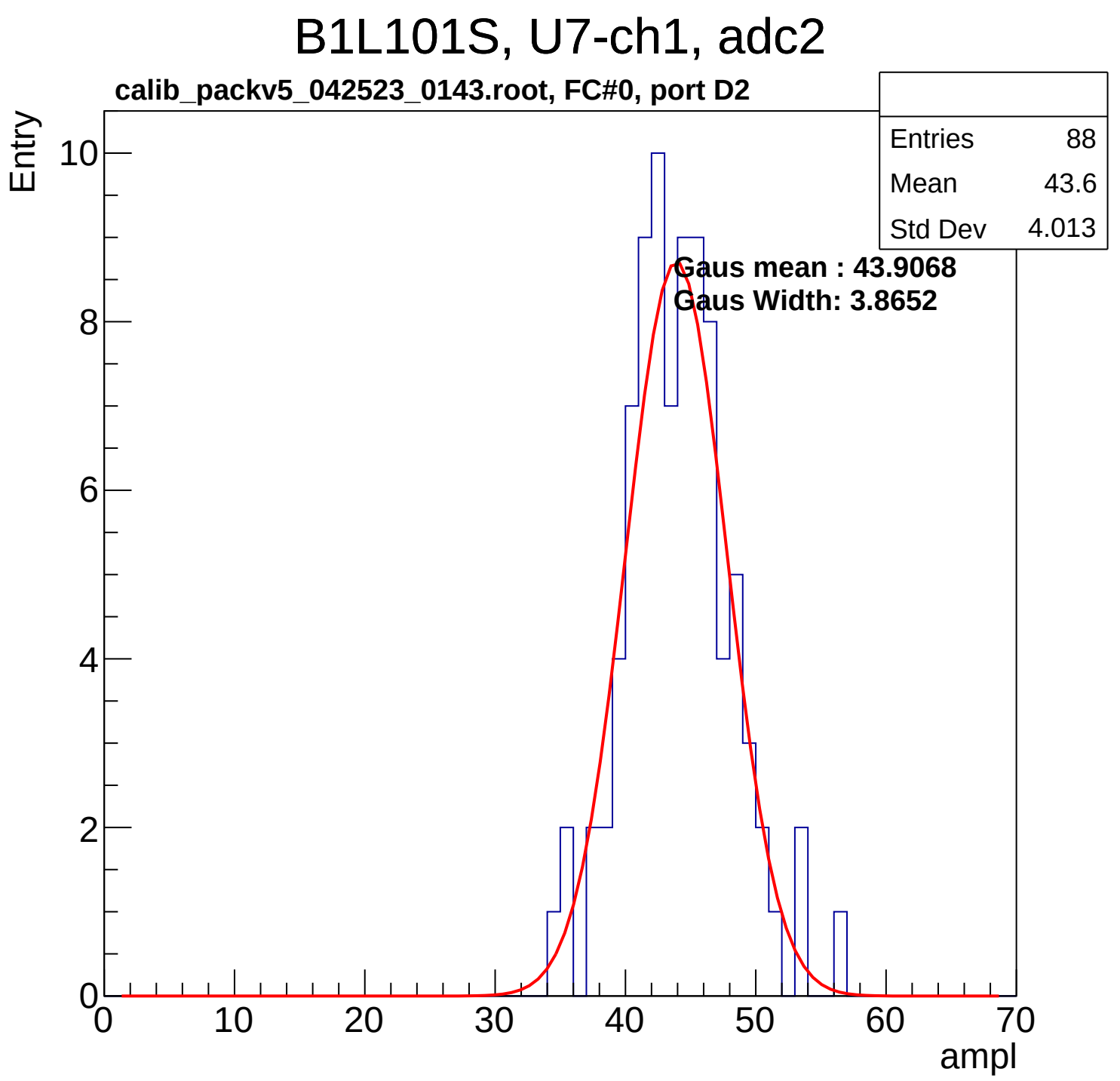
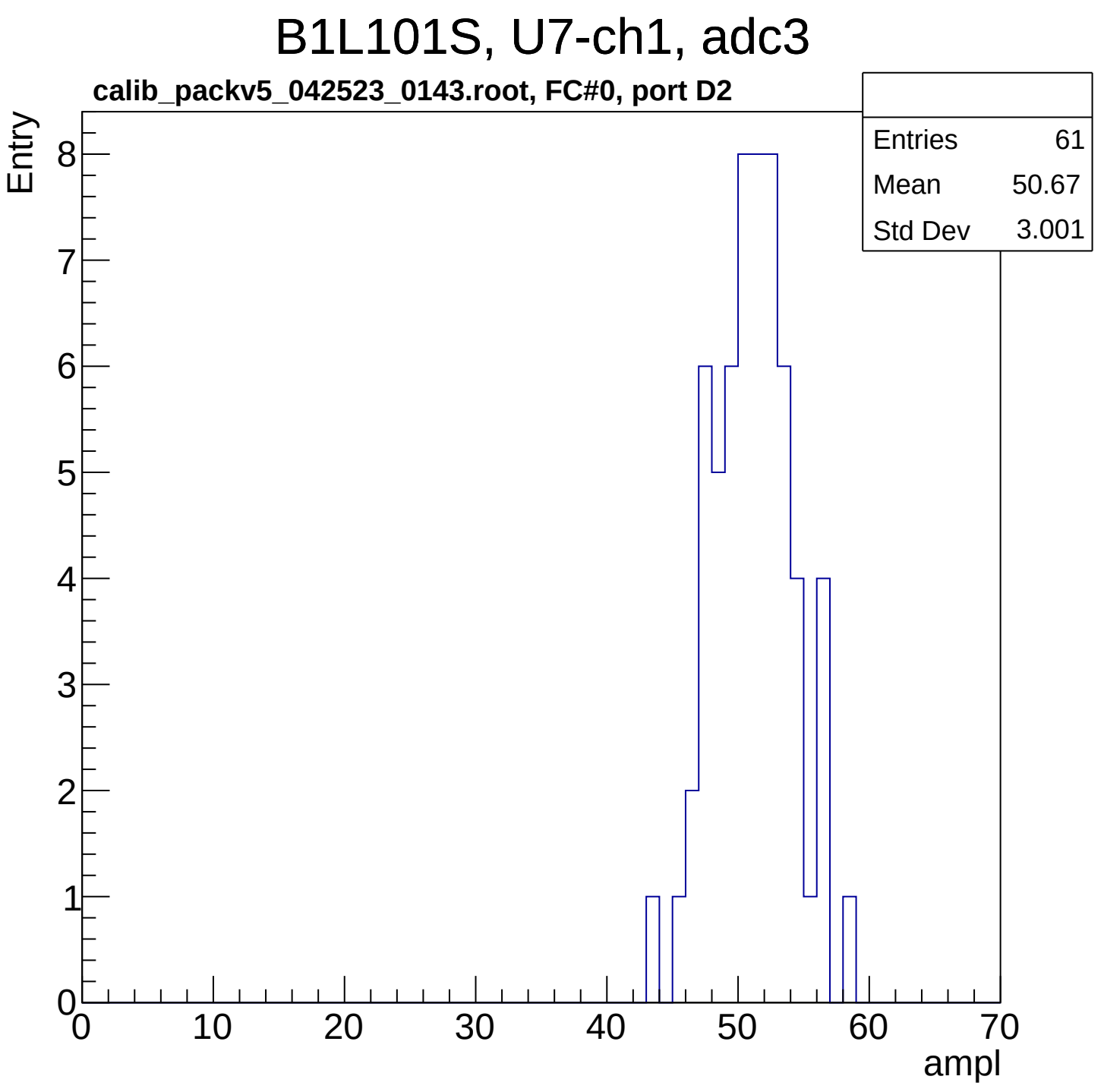

B1L101S, U7-ch0, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 56
Std Dev 18.7
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

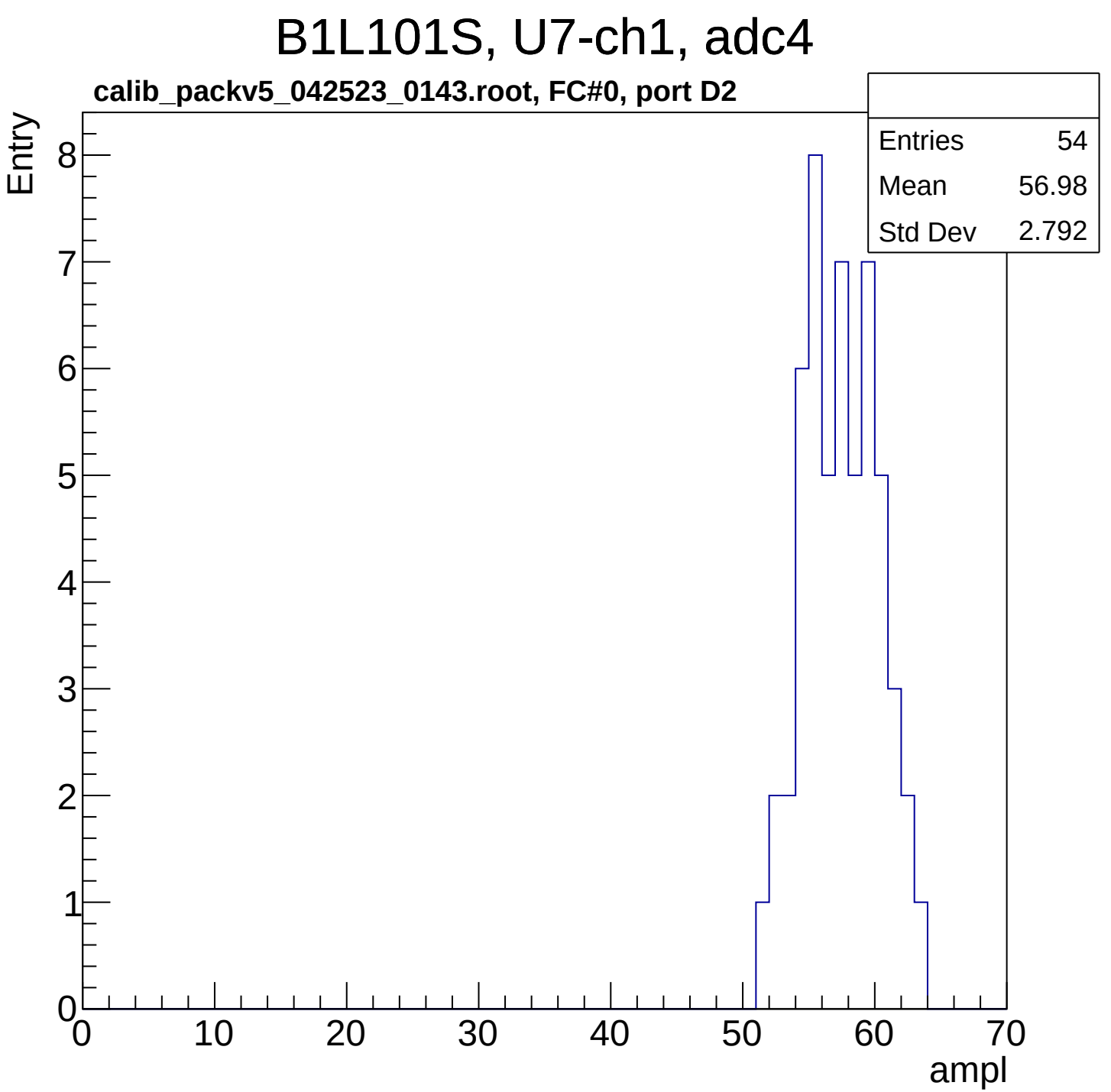

B1L101S, U7-ch0, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 0
Std Dev 0
Entry
3
2.5
2
1.5
1
0.5
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch1, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 30.26
Std Dev 3.764
Gaus mean : 30.2692
Gaus Width: 4.2251
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch1, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 36.23
Std Dev 3.669
Gaus mean : 36.1265
Gaus Width: 3.7492
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U7-ch1, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 88
Mean 43.6
Std Dev 4.013
Gaus mean : 43.9068
Gaus Width: 3.8652
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch1, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 50.67
Std Dev 3.001
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch1, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 56.98
Std Dev 2.792
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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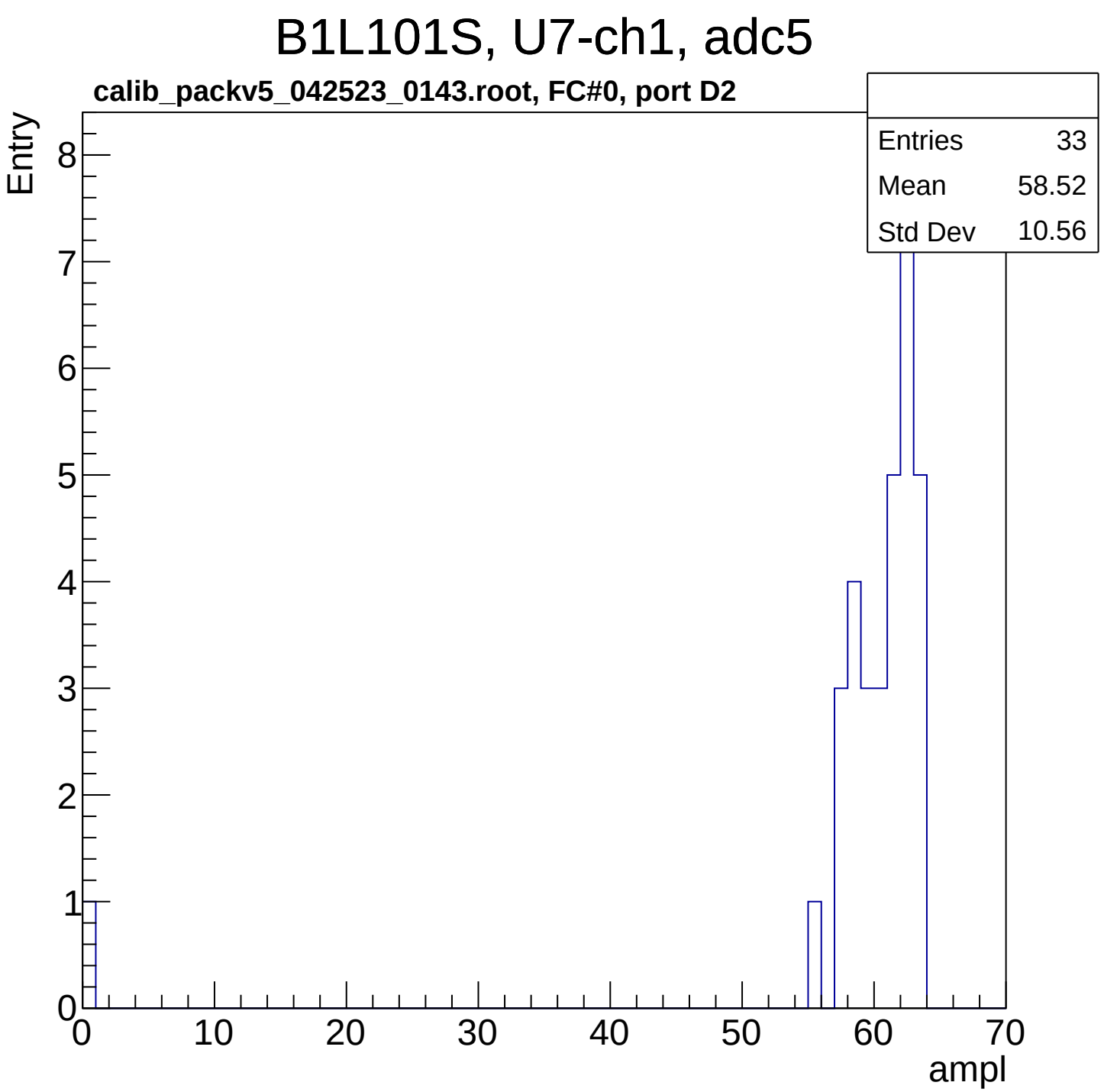
B1L101S, U7-ch1, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 33
Mean 58.52
Std Dev 10.56
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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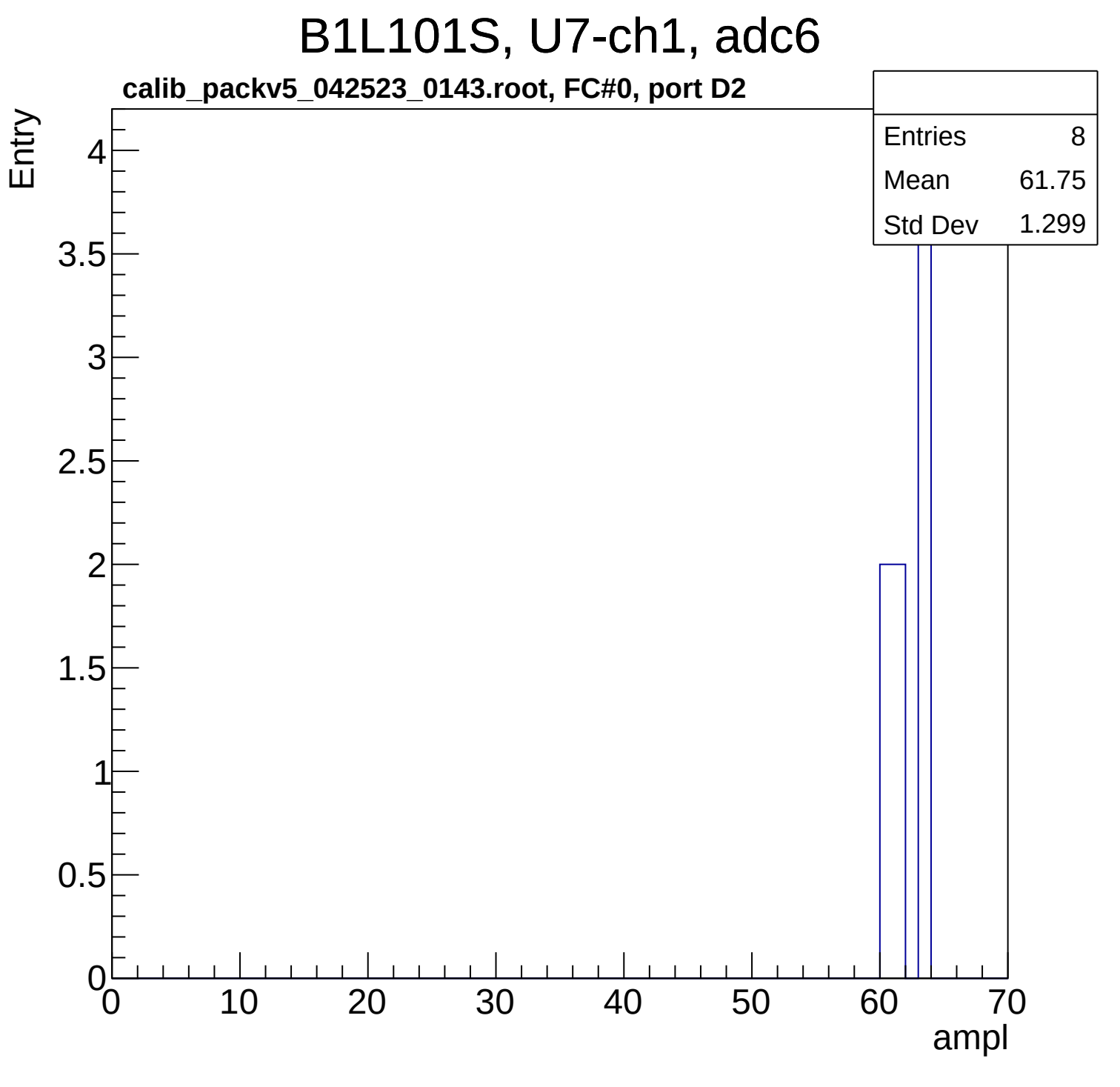
B1L101S, U7-ch1, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 61.75
Std Dev 1.299
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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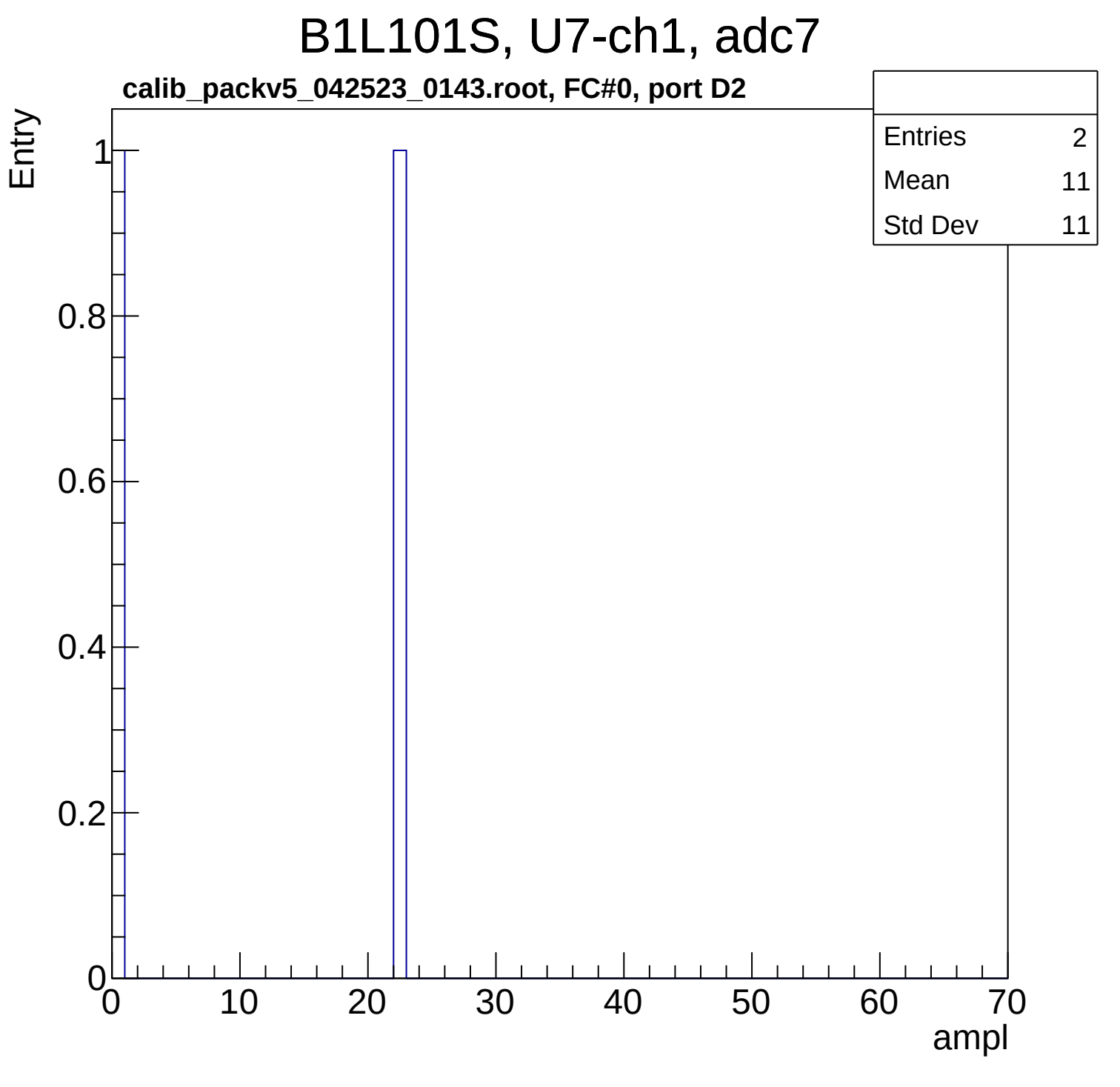
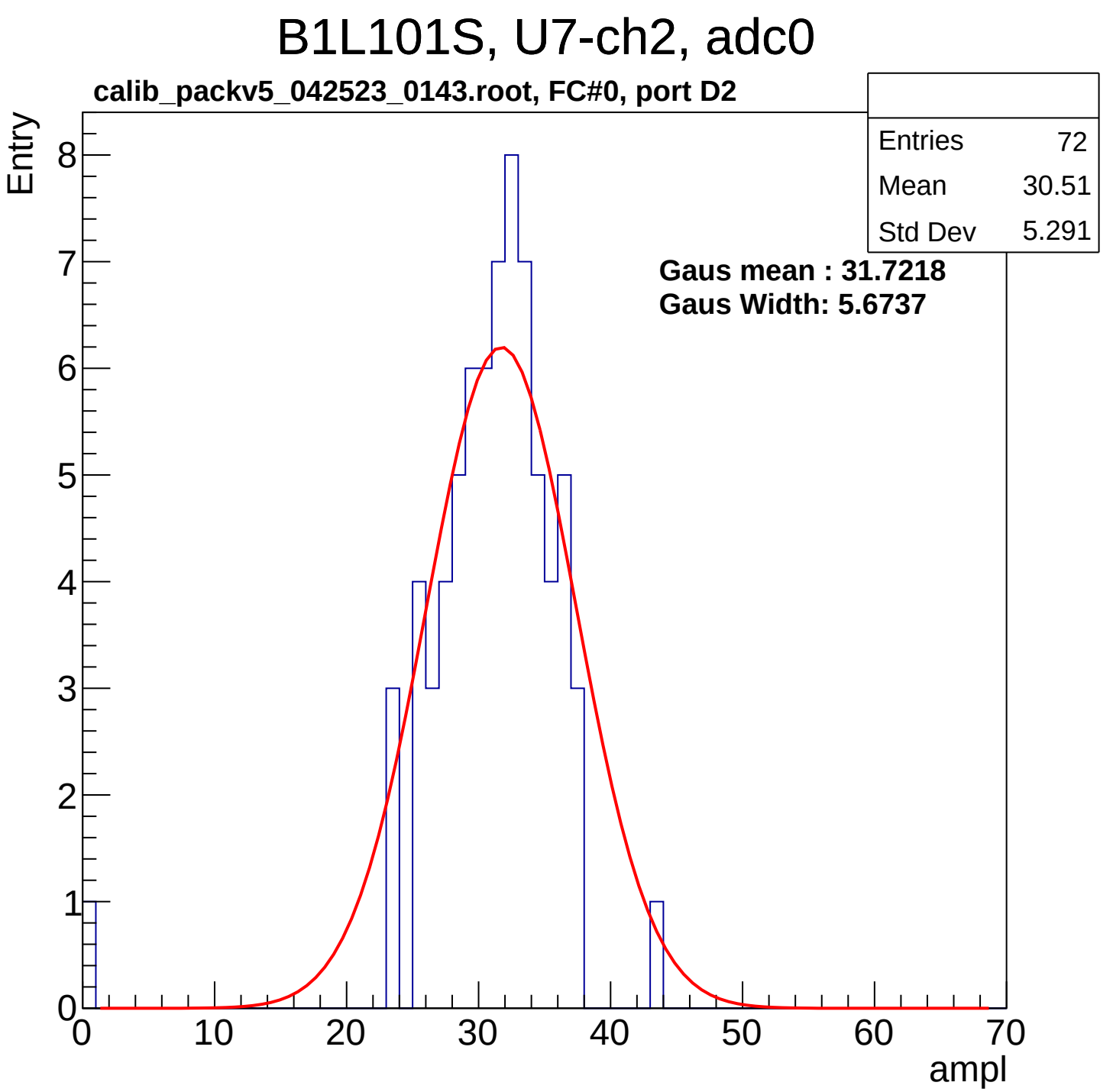

B1L101S, U7-ch1, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 11
Std Dev 11
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch2, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 30.51
Std Dev 5.291
Gaus mean : 31.7218
Gaus Width: 5.6737
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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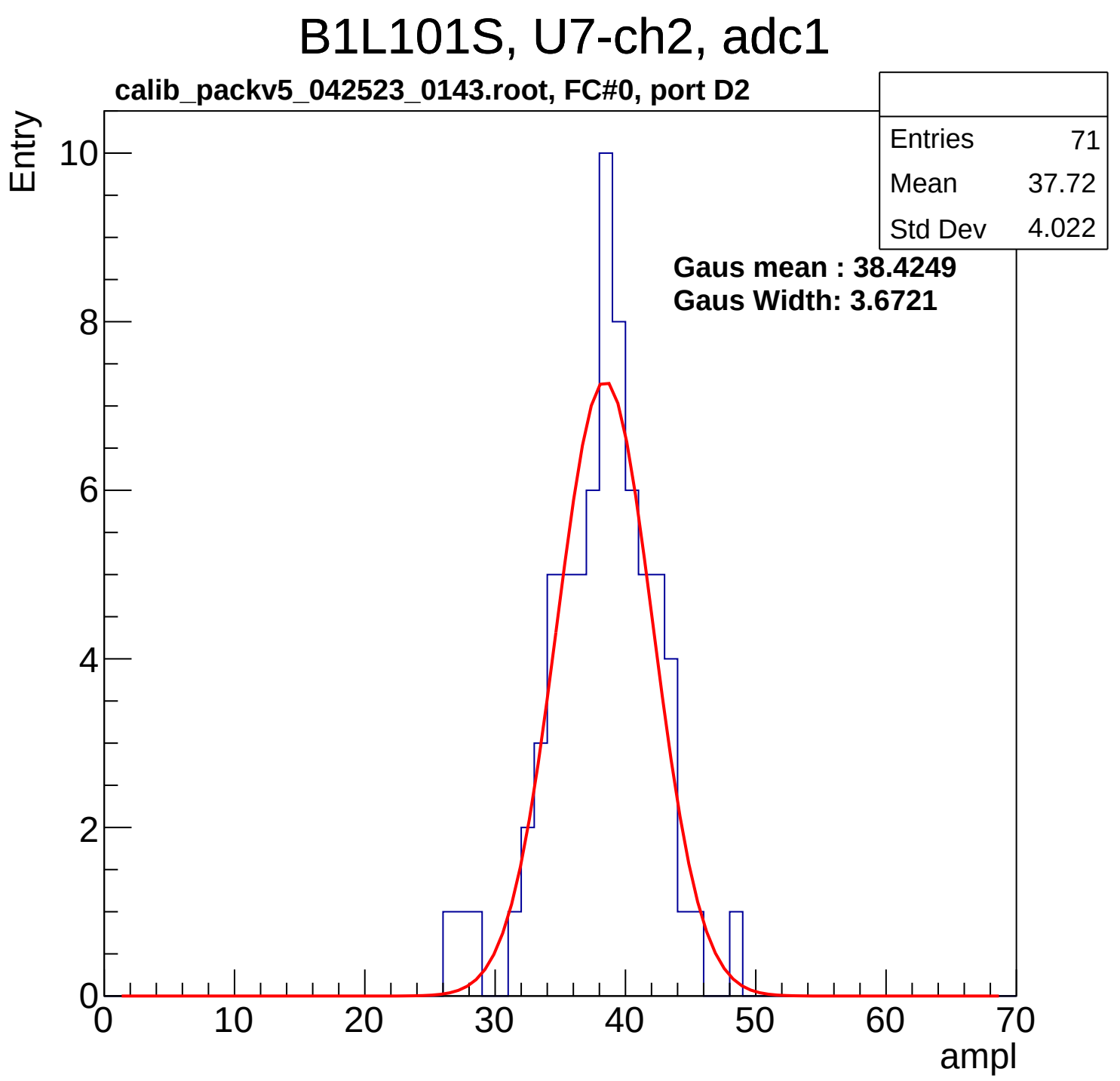
B1L101S, U7-ch2, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 37.72
Std Dev 4.022
Gaus mean : 38.4249
Gaus Width: 3.6721
Entry
ampl
0
2
4
6
8
10
0
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20
30
40
50
60
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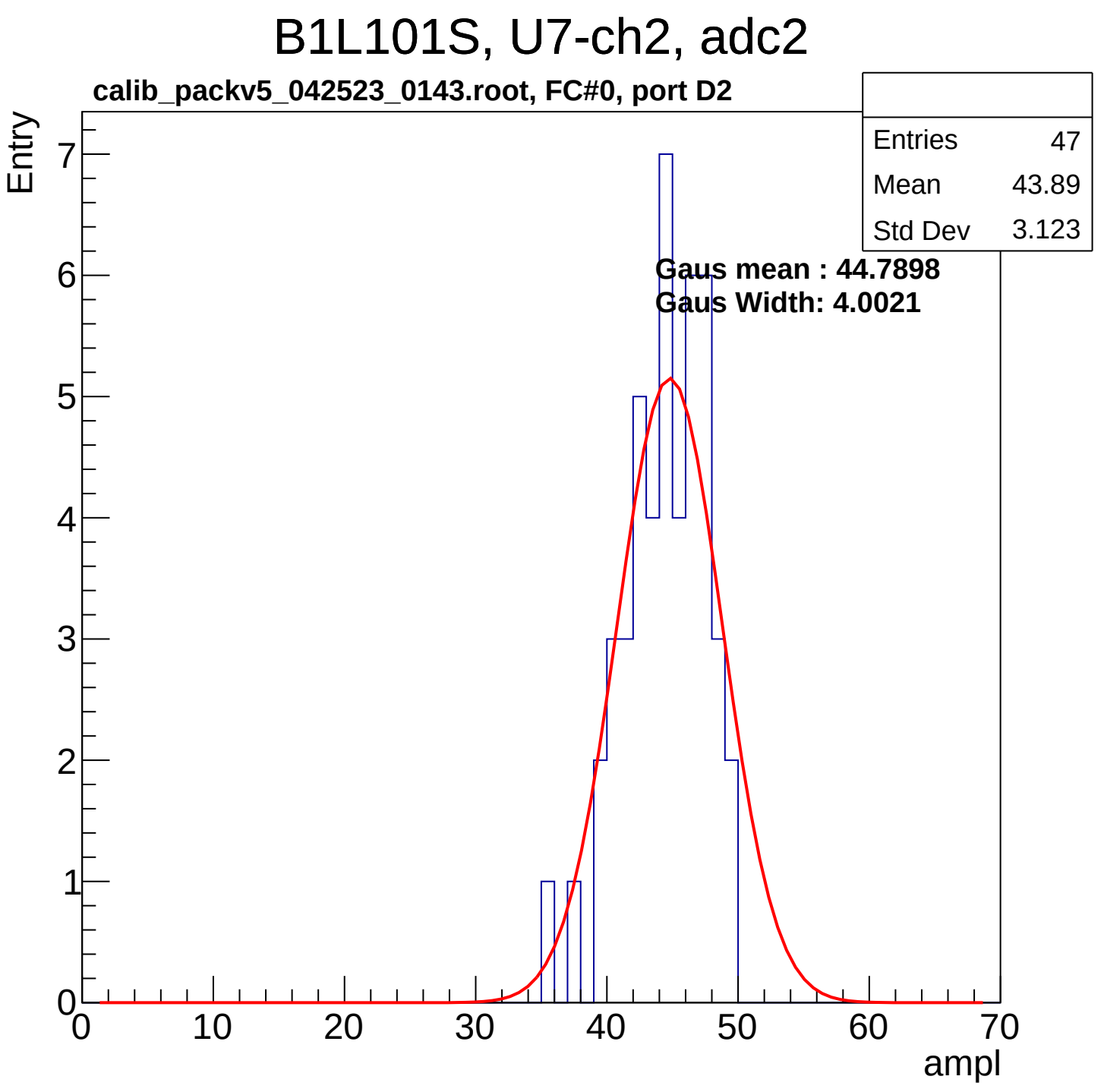
B1L101S, U7-ch2, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 43.89
Std Dev 3.123
Gaus mean : 44.7898
Gaus Width: 4.0021
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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60
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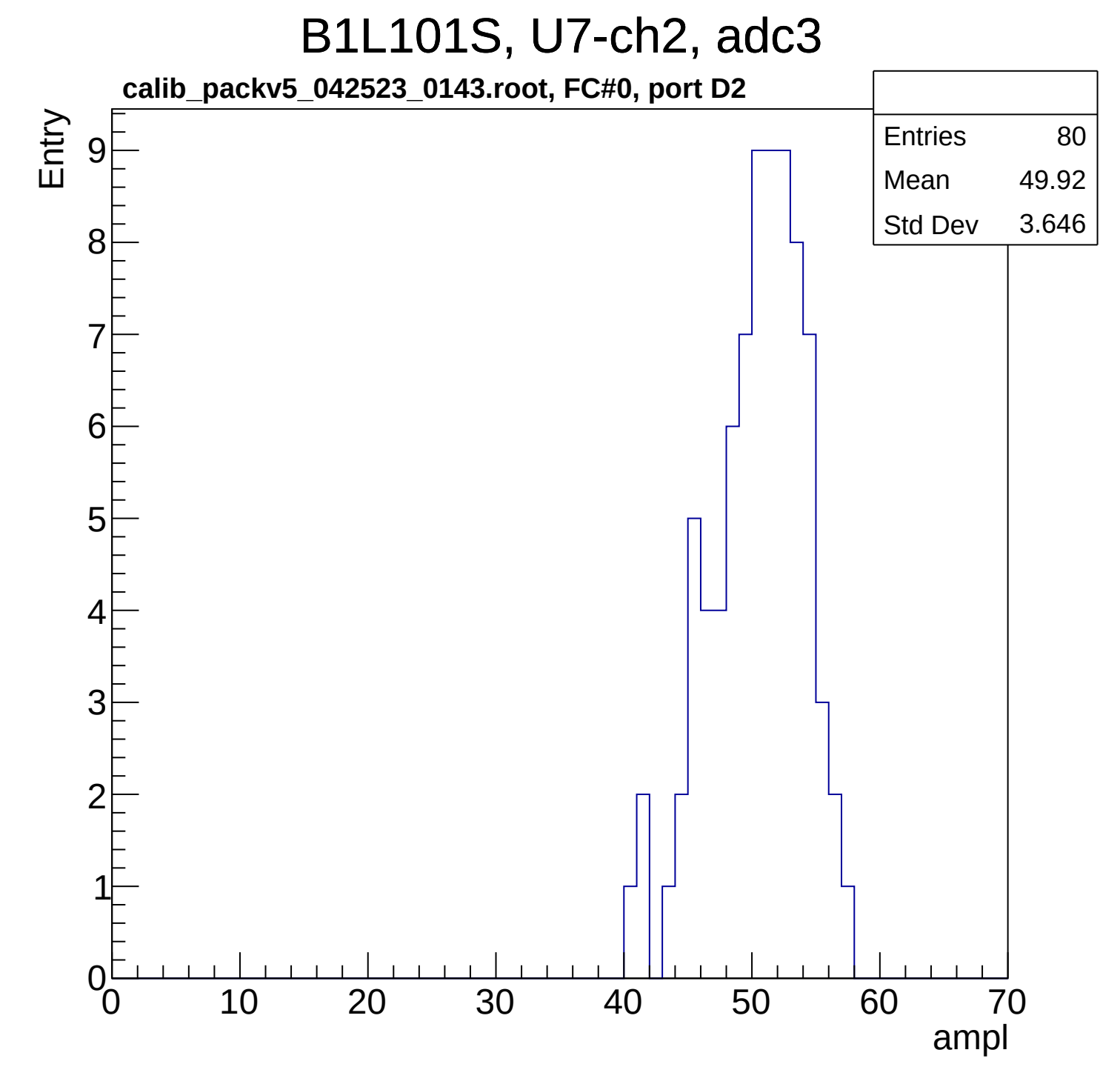
B1L101S, U7-ch2, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 80
Mean 49.92
Std Dev 3.646
Entry
ampl
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4
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6
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8
9
0
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60
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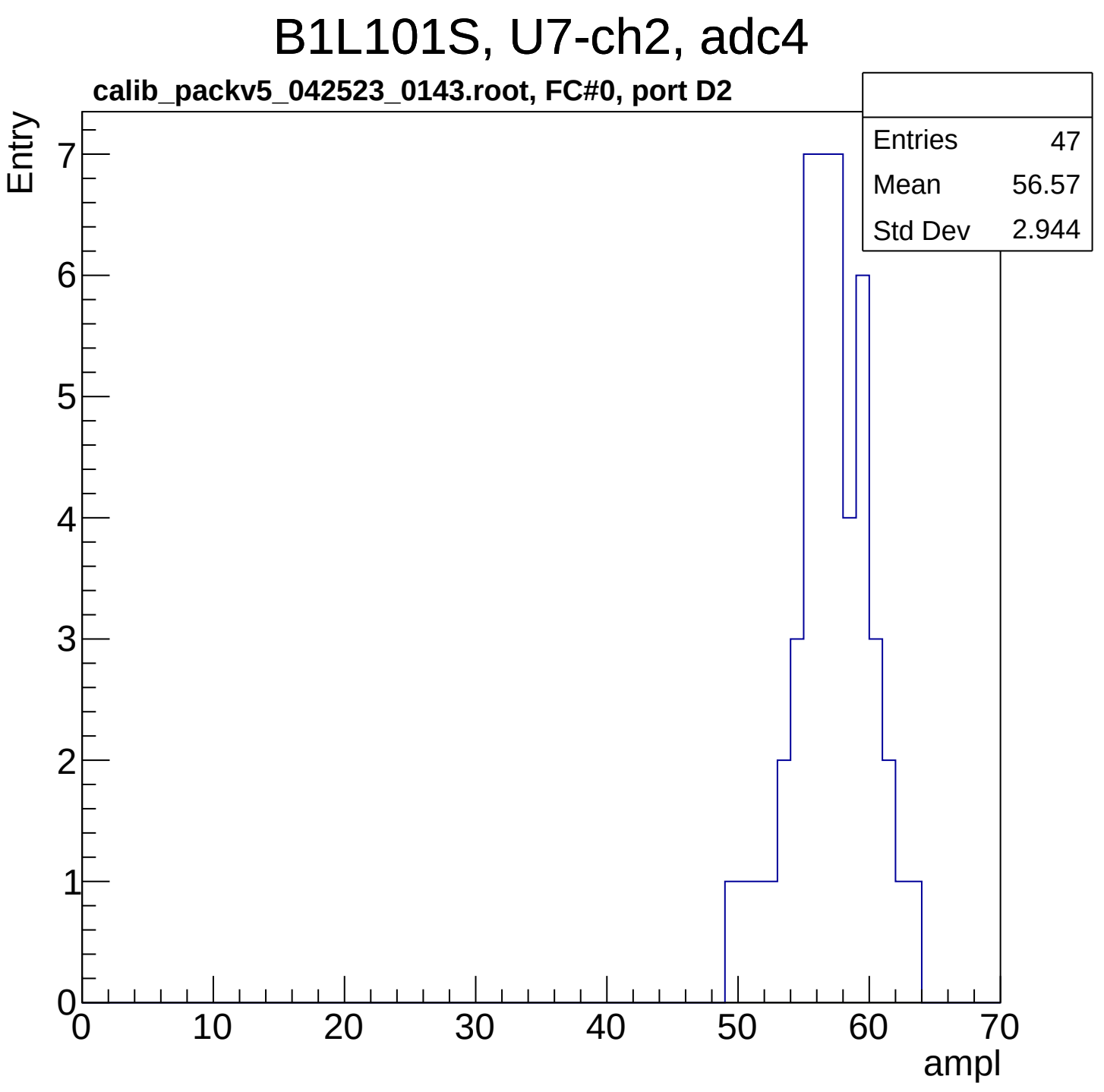
B1L101S, U7-ch2, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 56.57
Std Dev 2.944
Entry
ampl
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3
4
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6
7
0
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20
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40
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60
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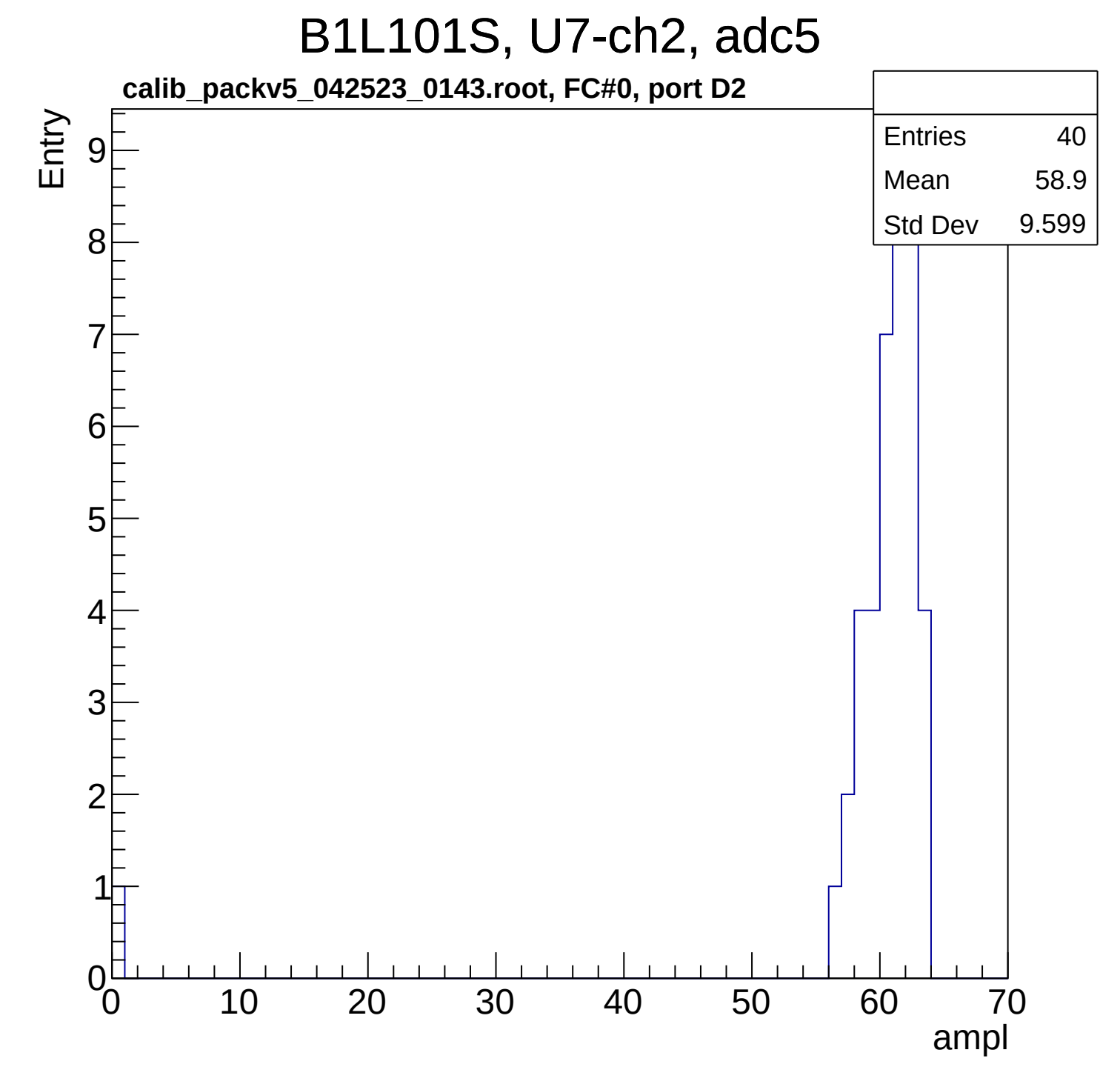
B1L101S, U7-ch2, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 40
Mean 58.9
Std Dev 9.599
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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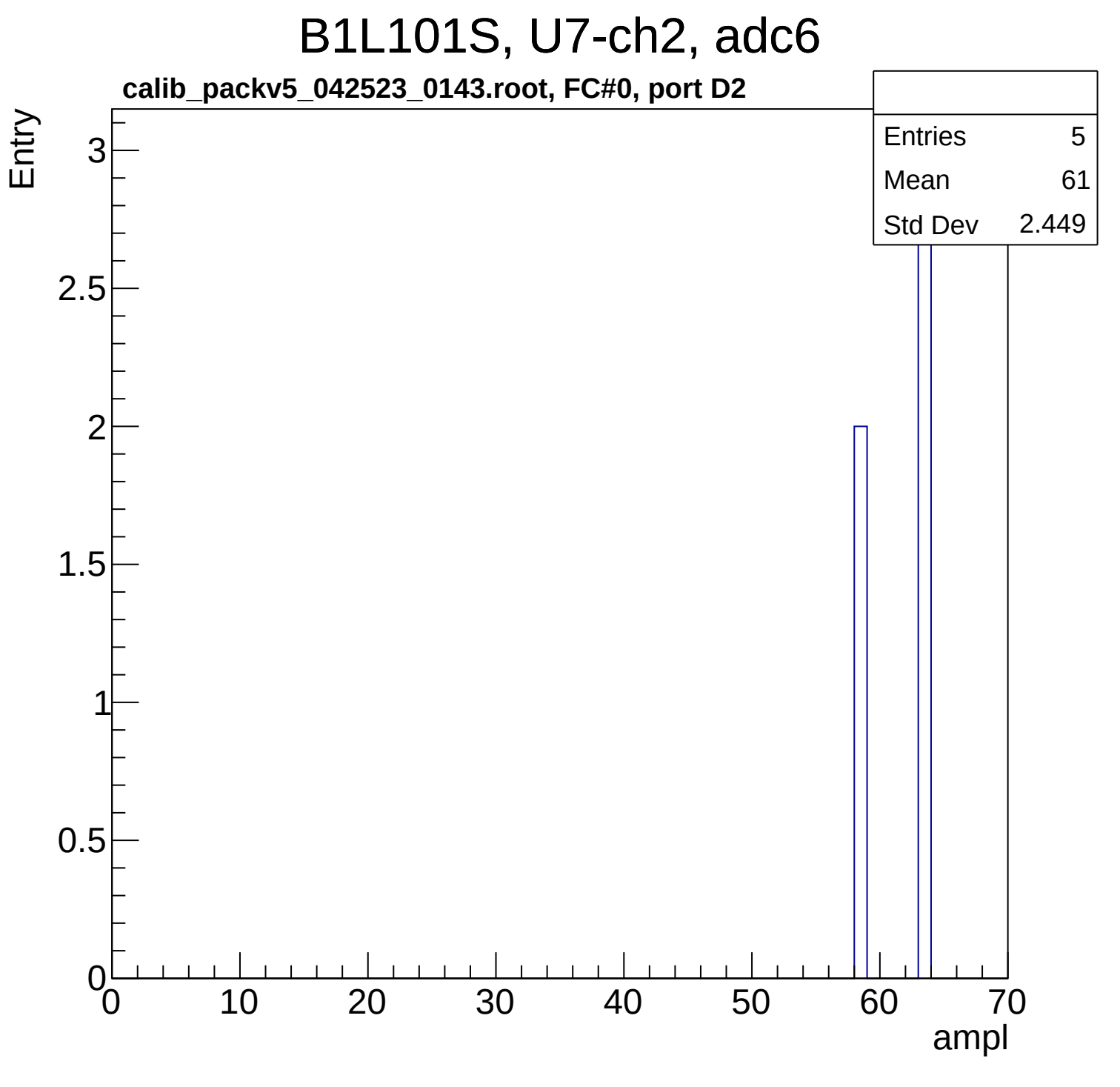
B1L101S, U7-ch2, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 61
Std Dev 2.449
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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40
50
60
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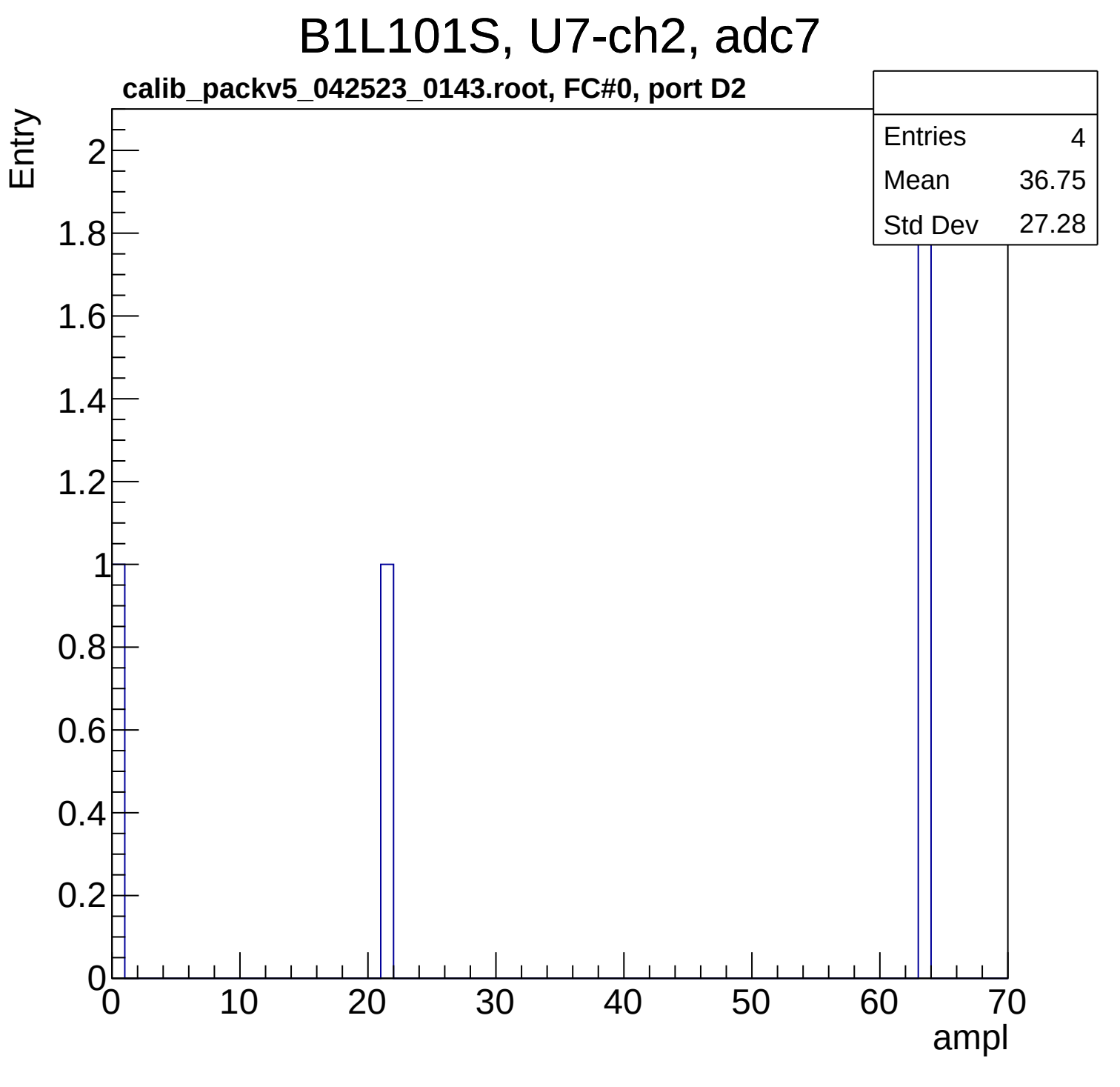
B1L101S, U7-ch2, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 36.75
Std Dev 27.28
Entry
ampl
0
0.2
0.4
0.6
0.8
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1.2
1.4
1.6
1.8
2
0
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20
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40
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60
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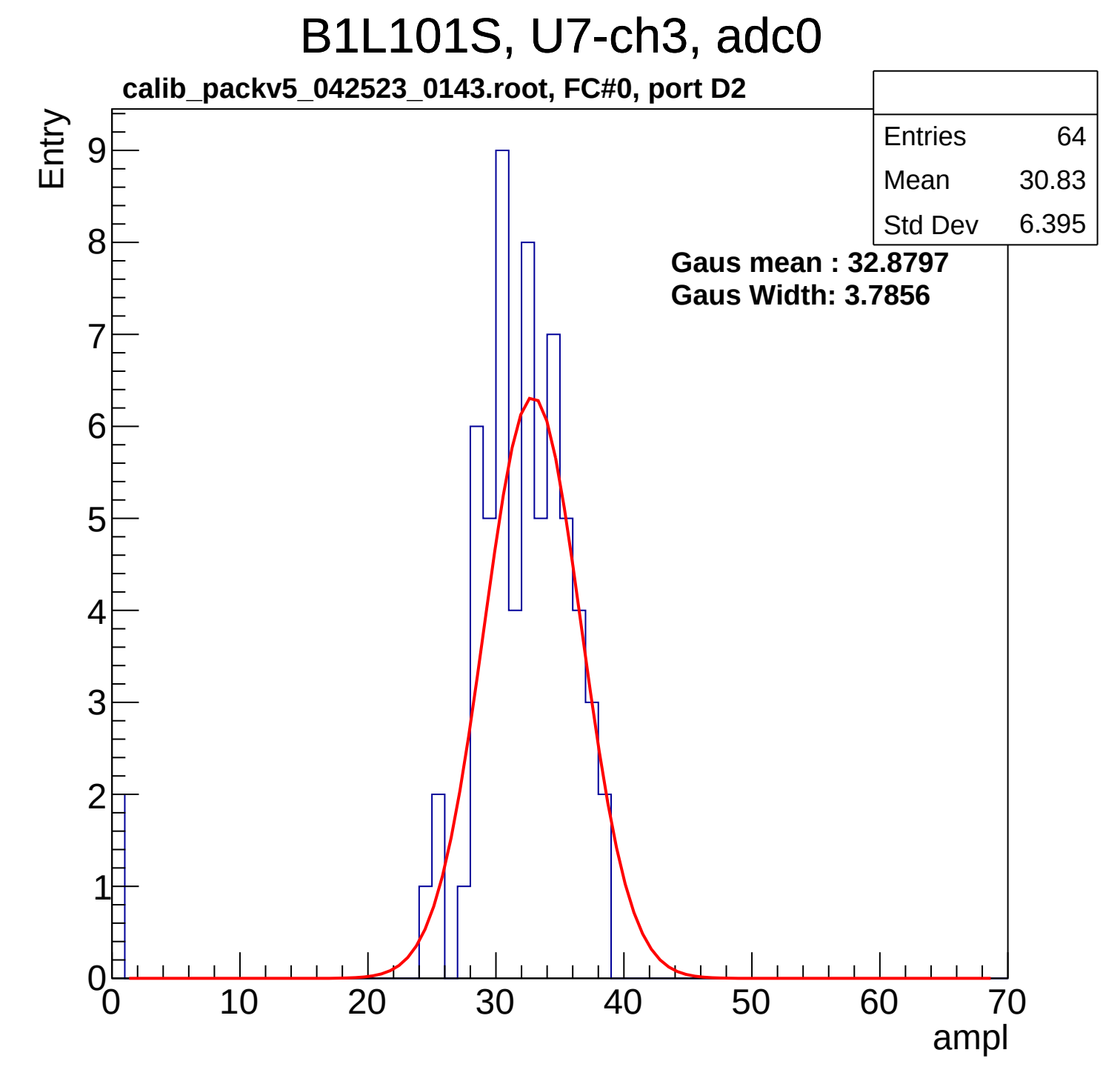
B1L101S, U7-ch3, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 30.83
Std Dev 6.395
Gaus mean : 32.8797
Gaus Width: 3.7856
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
50
60
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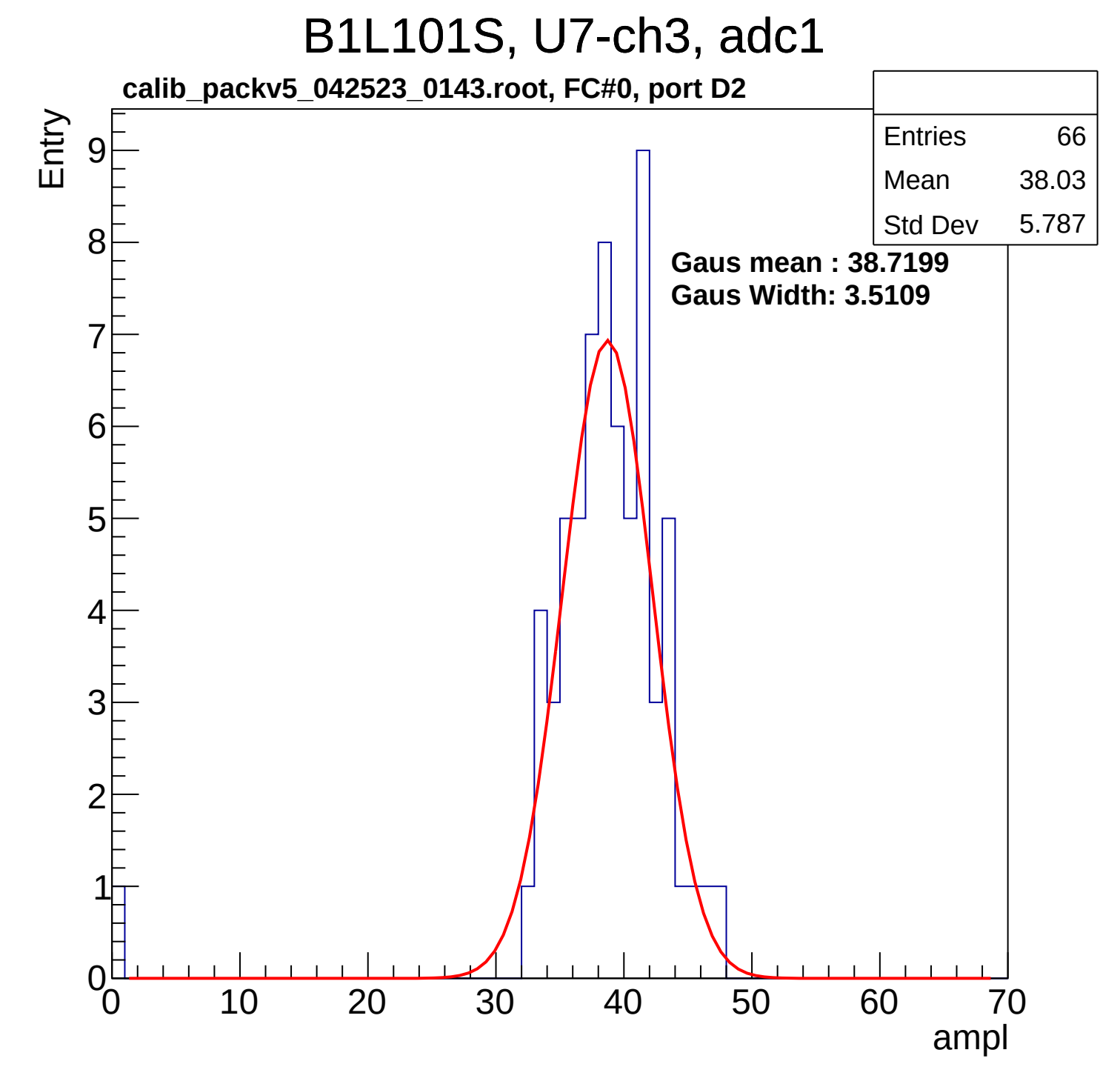
B1L101S, U7-ch3, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 38.03
Std Dev 5.787
Gaus mean : 38.7199
Gaus Width: 3.5109
Entry
ampl
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10
20
30
40
50
60
70
1
2
3
4
5
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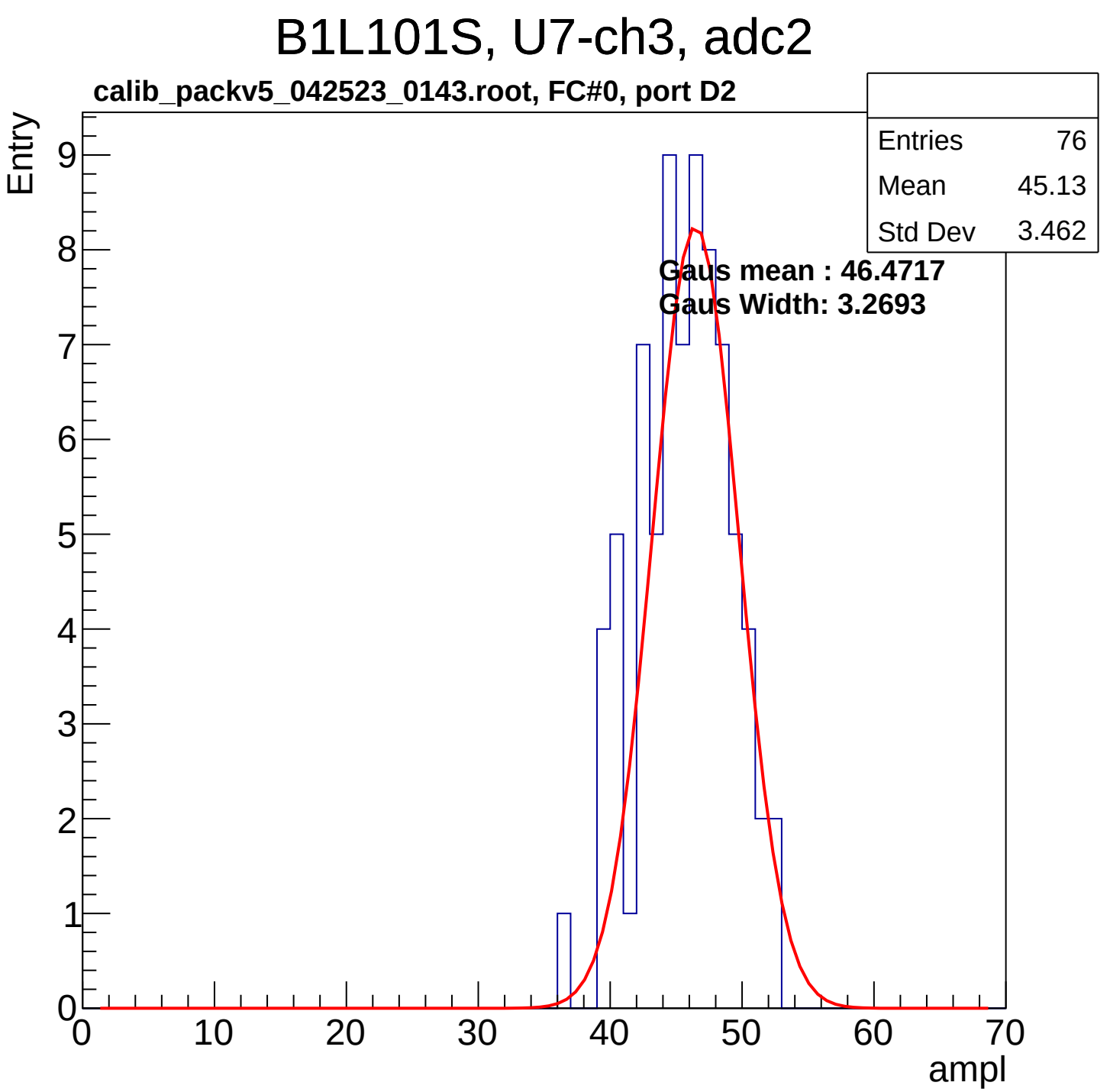
7
8
9


B1L101S, U7-ch3, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 45.13
Std Dev 3.462
Gaus mean : 46.4717
Gaus Width: 3.2693
Entry
ampl
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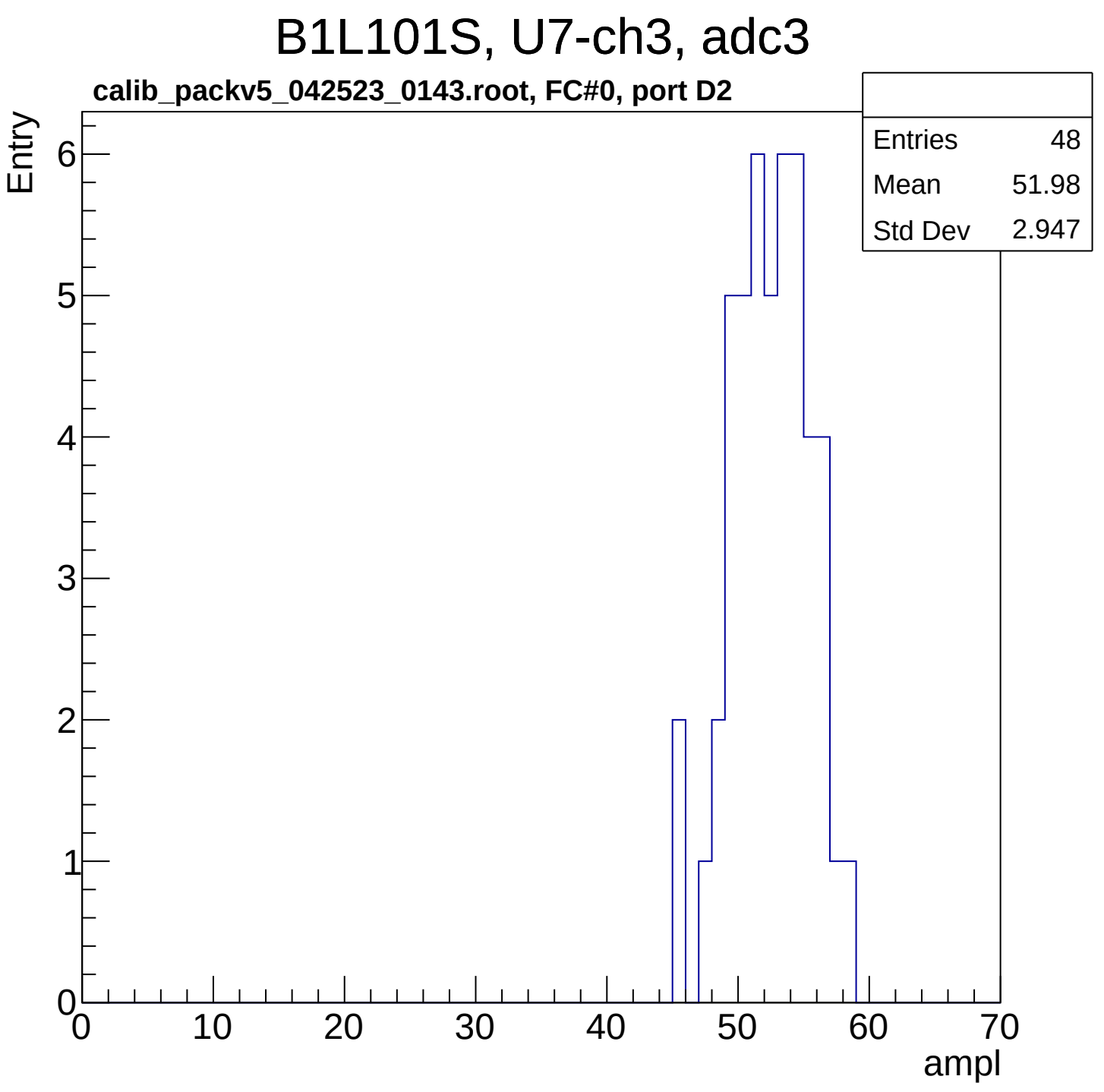
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L101S, U7-ch3, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 51.98
Std Dev 2.947
Entry
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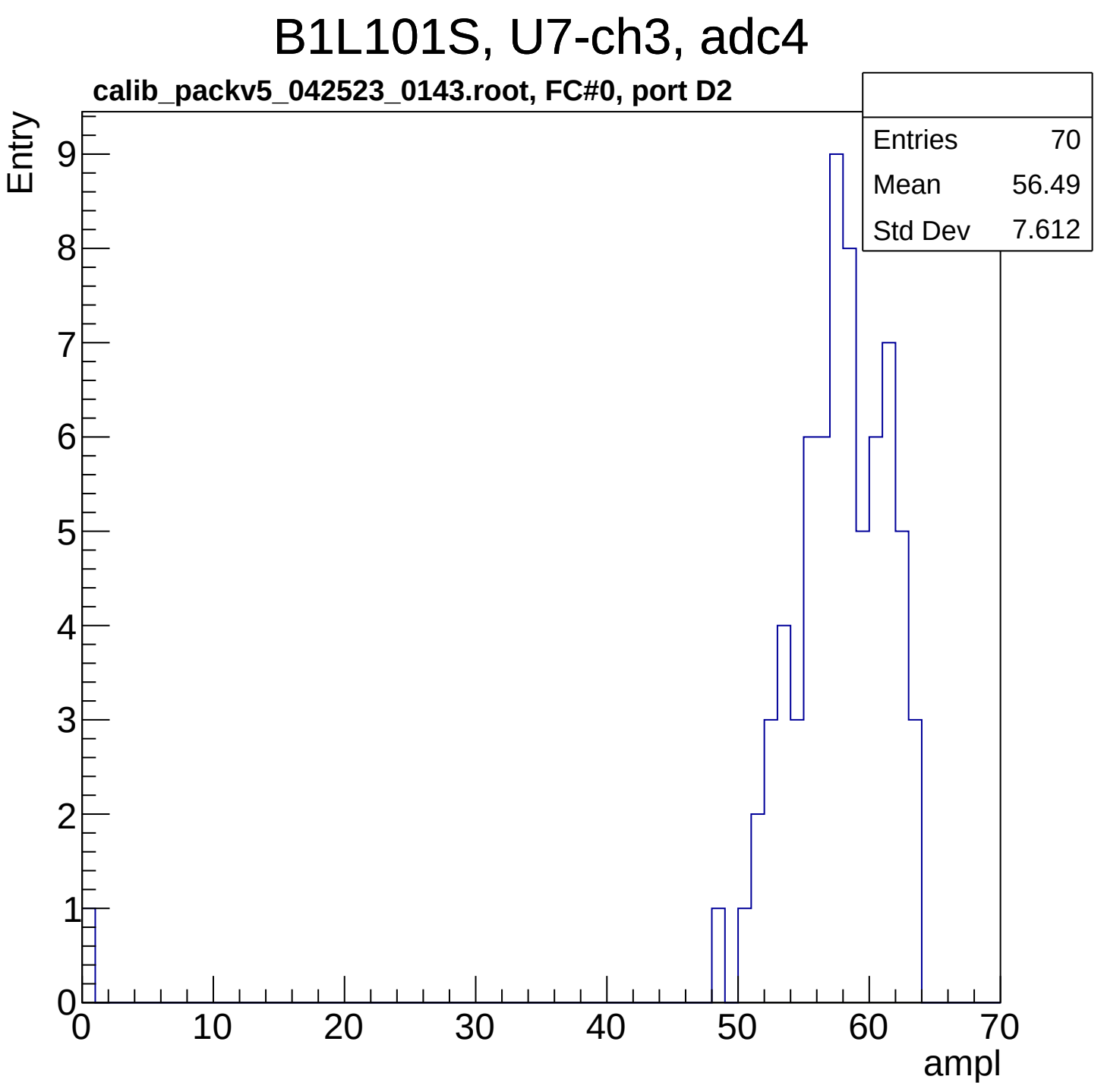
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch3, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 56.49
Std Dev 7.612
Entry
ampl
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2
3
4
5
6
7
8
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0
10
20
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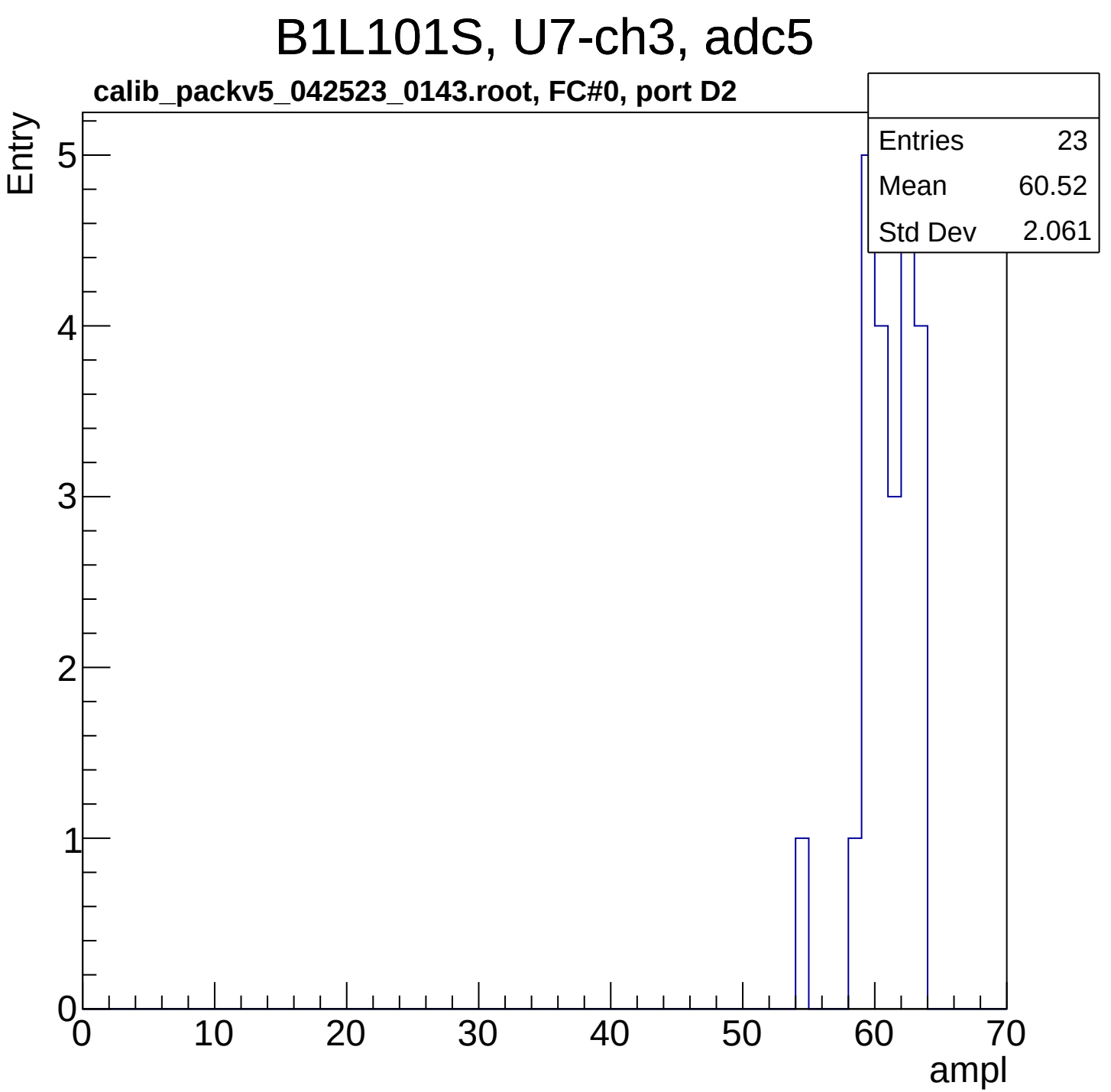
40
50
60
70


B1L101S, U7-ch3, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 23
Mean 60.52
Std Dev 2.061
Entry
ampl
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1
2
3
4
5
0
10
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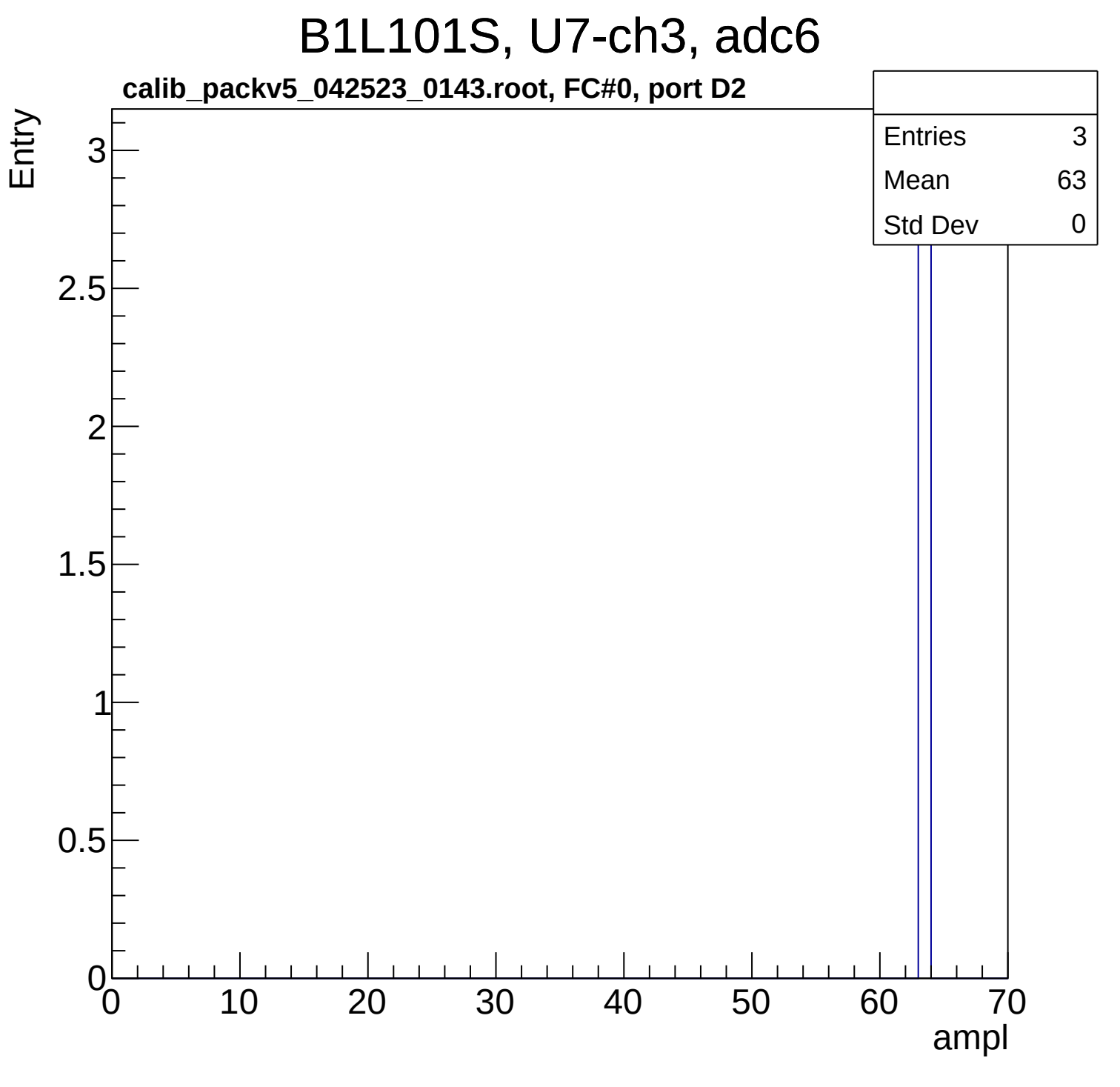
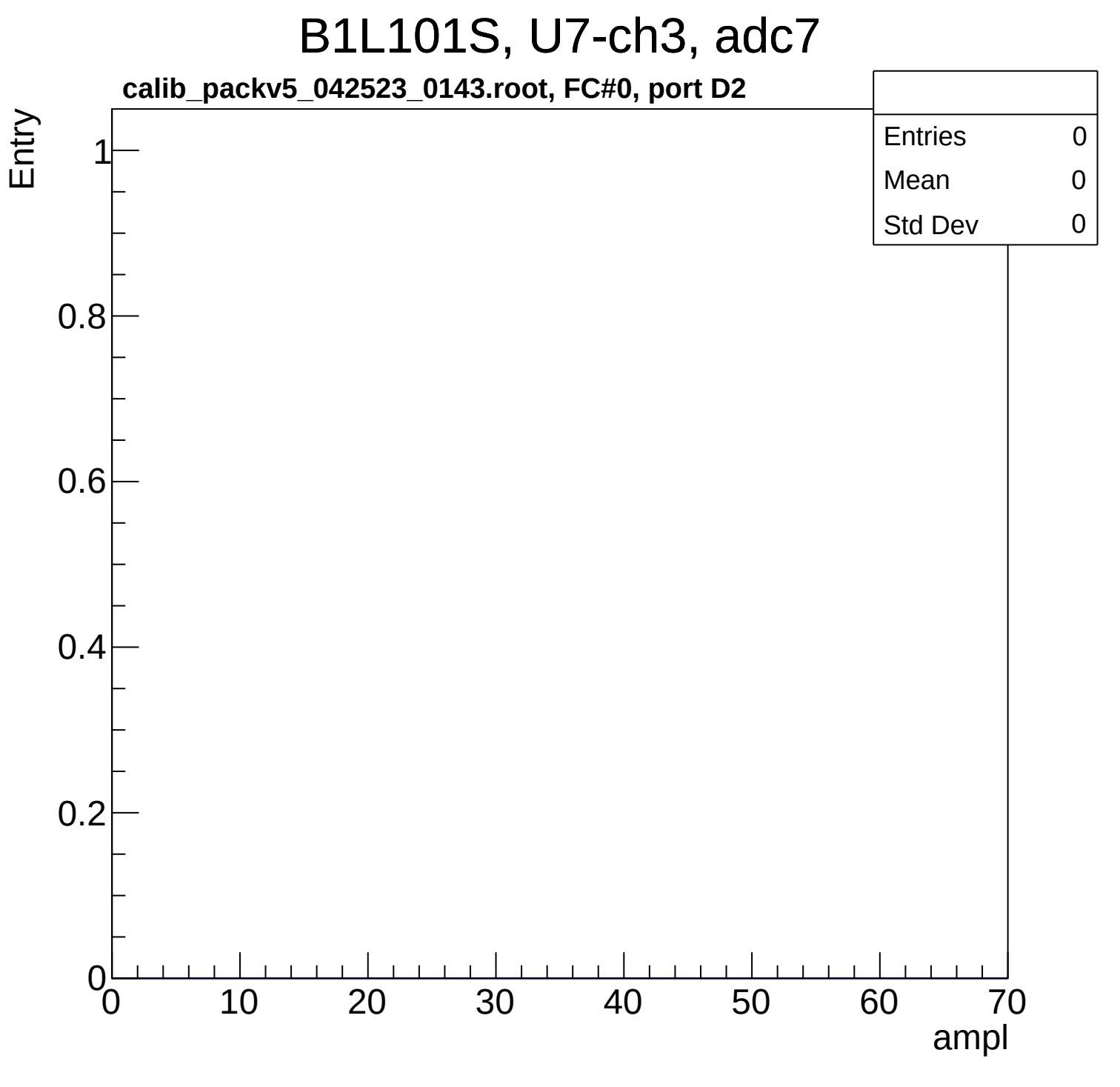
30
40
50
60
70


B1L101S, U7-ch3, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 63
Std Dev 0
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U7-ch3, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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0.6
0.4
0.2
0
0
10
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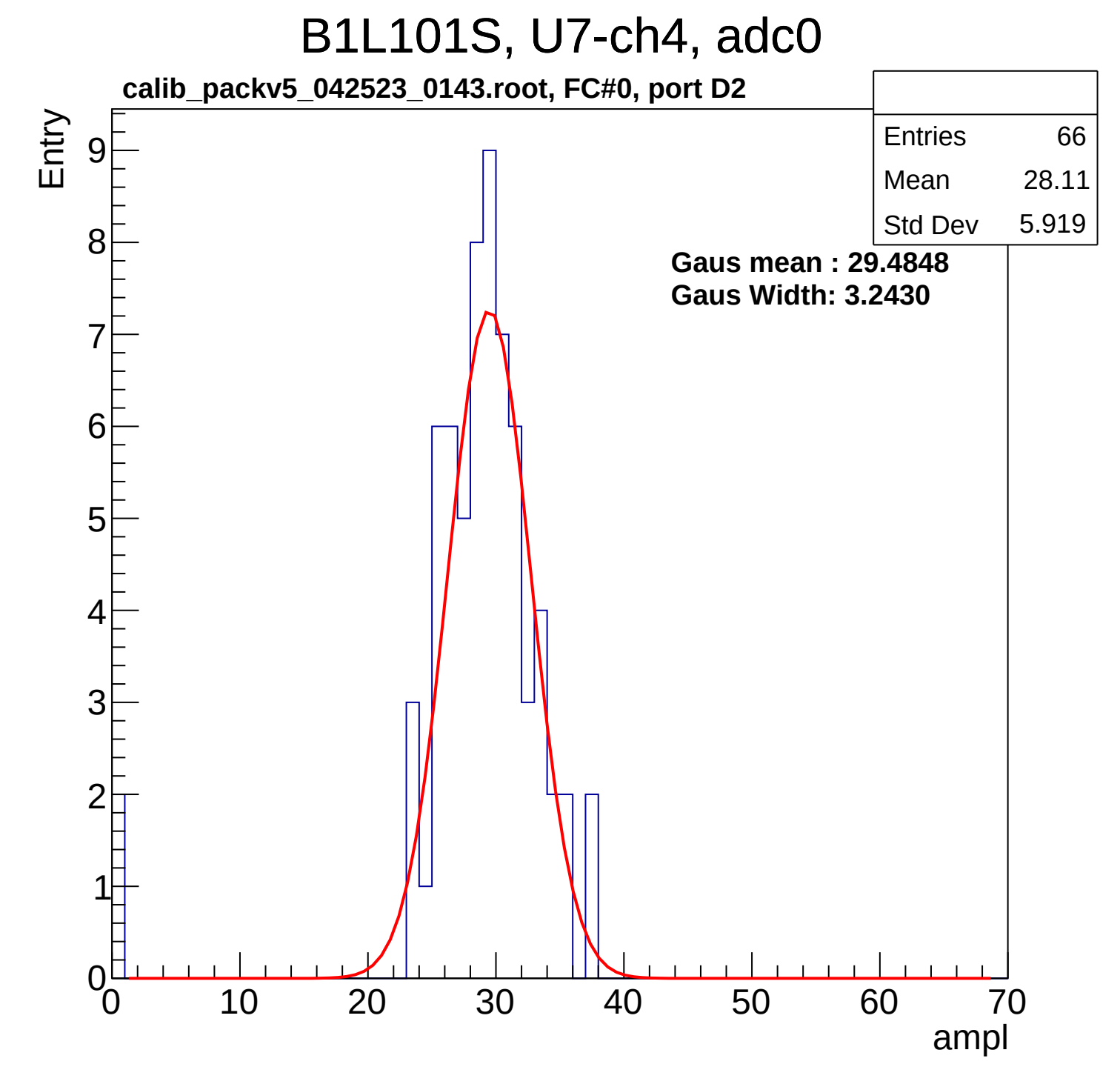
60
70
ampl


B1L101S, U7-ch4, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 28.11
Std Dev 5.919
Gaus mean : 29.4848
Gaus Width: 3.2430
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
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40
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60
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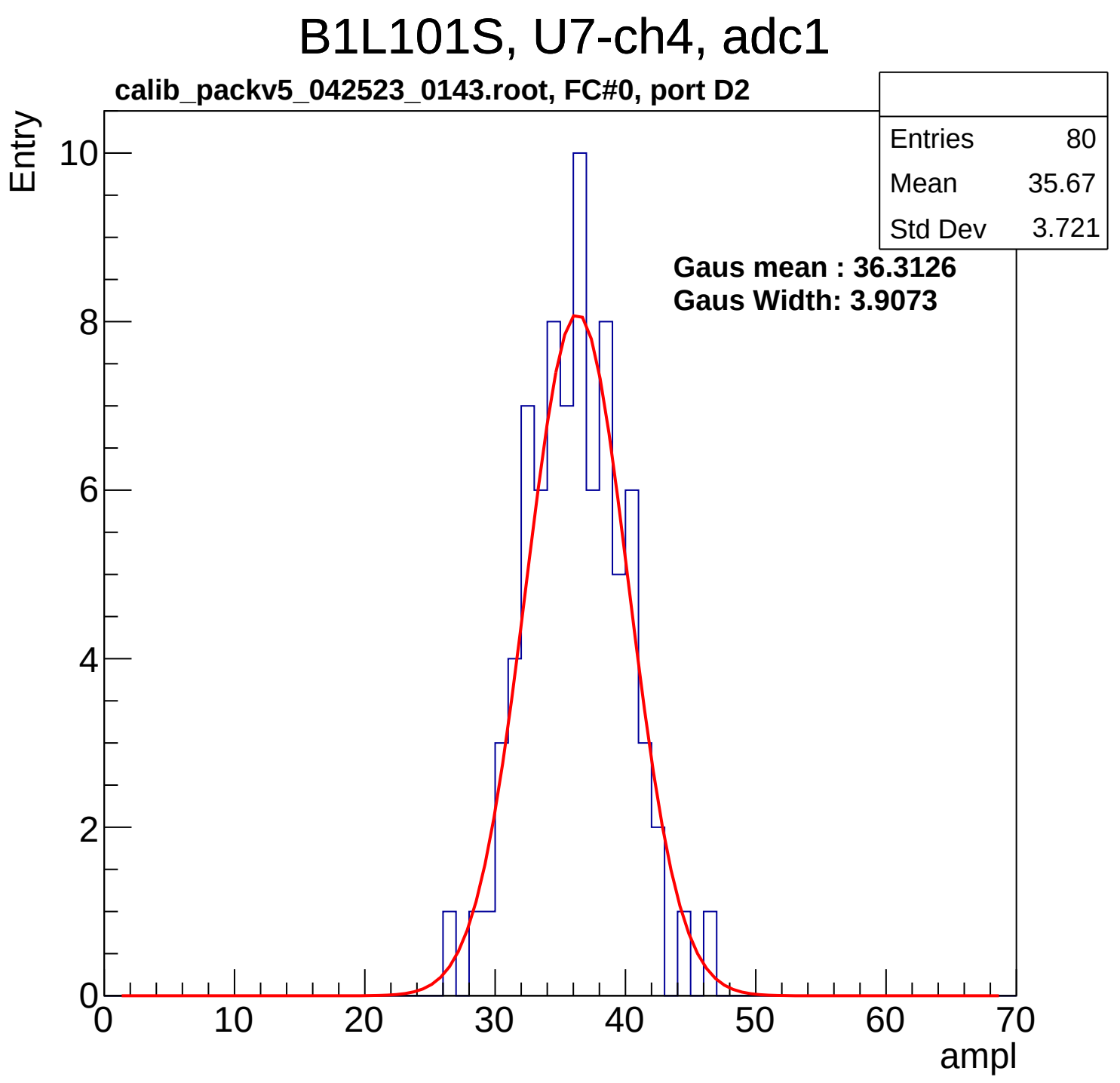
B1L101S, U7-ch4, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 80
Mean 35.67
Std Dev 3.721
Gaus mean : 36.3126
Gaus Width: 3.9073
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
50
60
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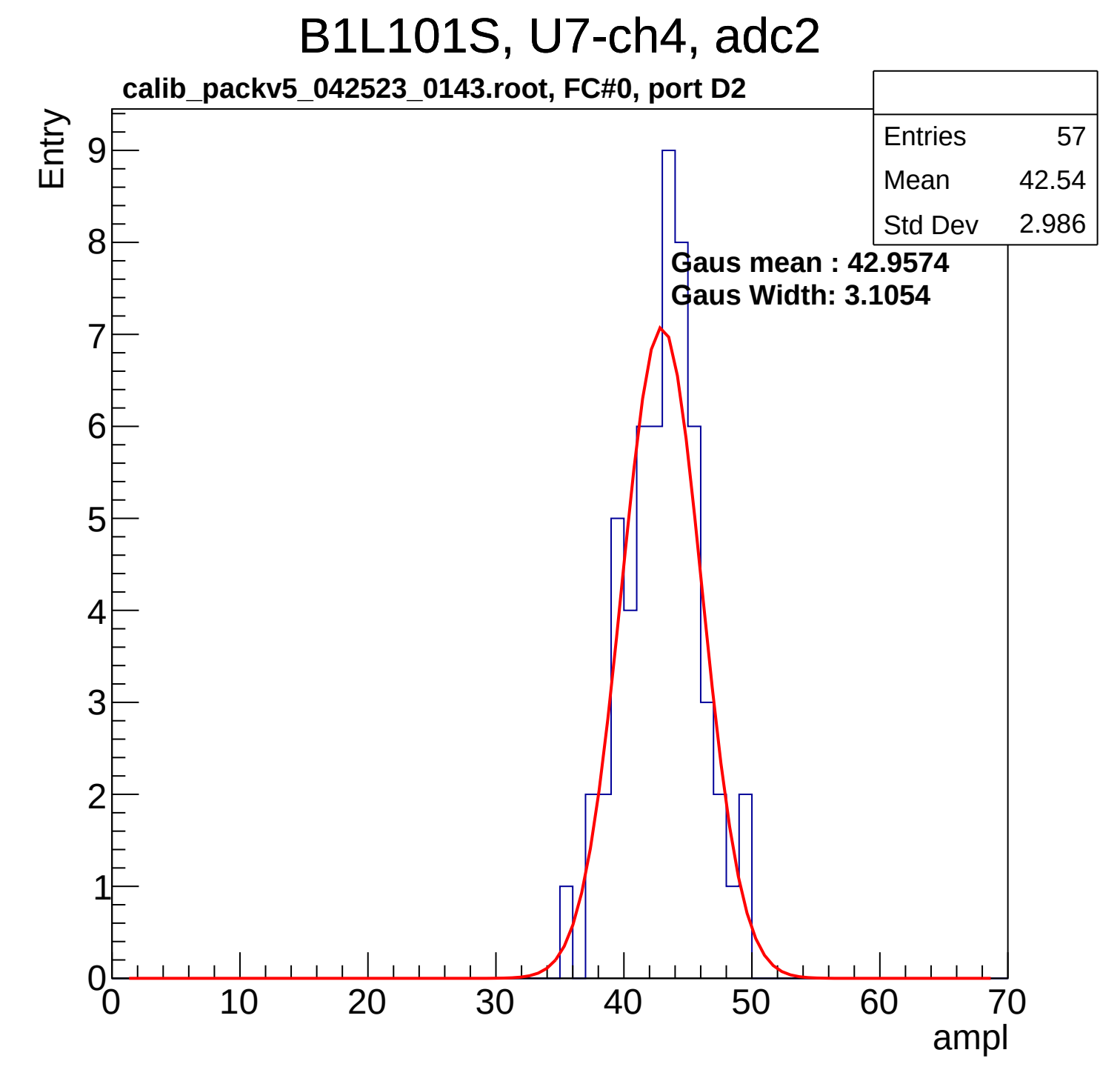
B1L101S, U7-ch4, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 42.54
Std Dev 2.986
Gaus mean : 42.9574
Gaus Width: 3.1054
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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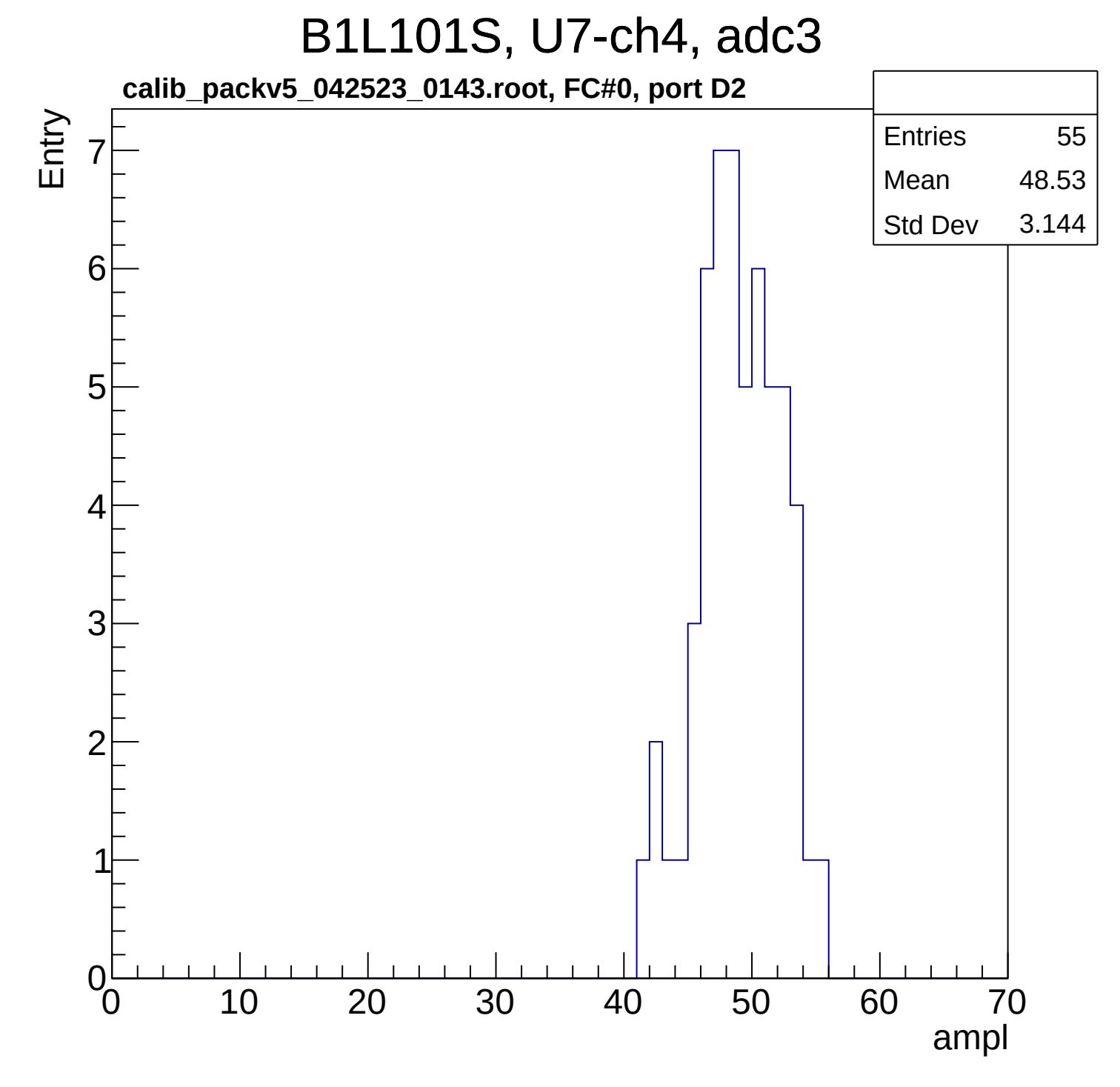
B1L101S, U7-ch4, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 48.53
Std Dev 3.144
Entry
ampl
0
1
2
3
4
5
6
7
0
10
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40
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60
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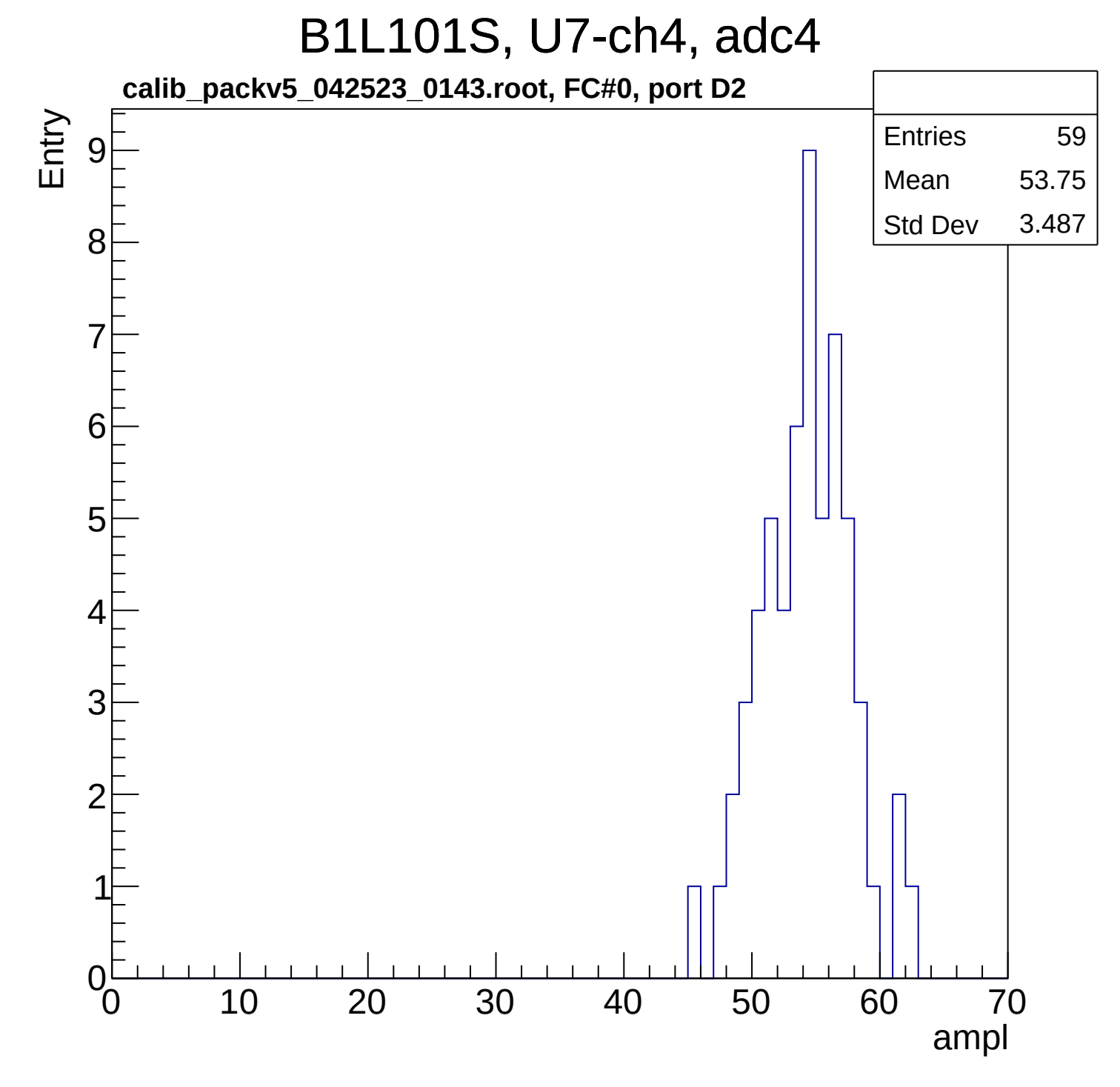
B1L101S, U7-ch4, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 53.75
Std Dev 3.487
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
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60
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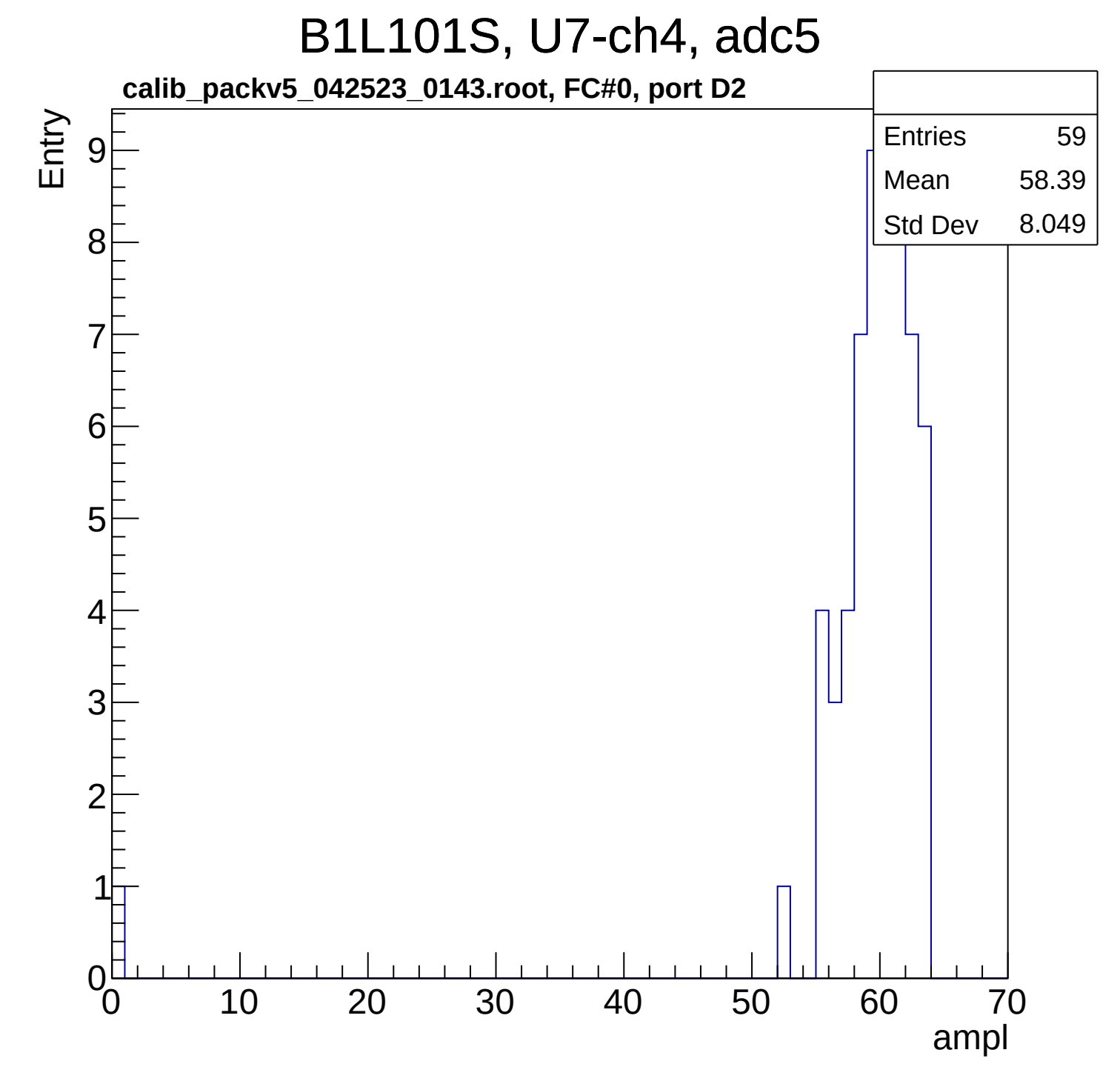
B1L101S, U7-ch4, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 58.39
Std Dev 8.049
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
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60
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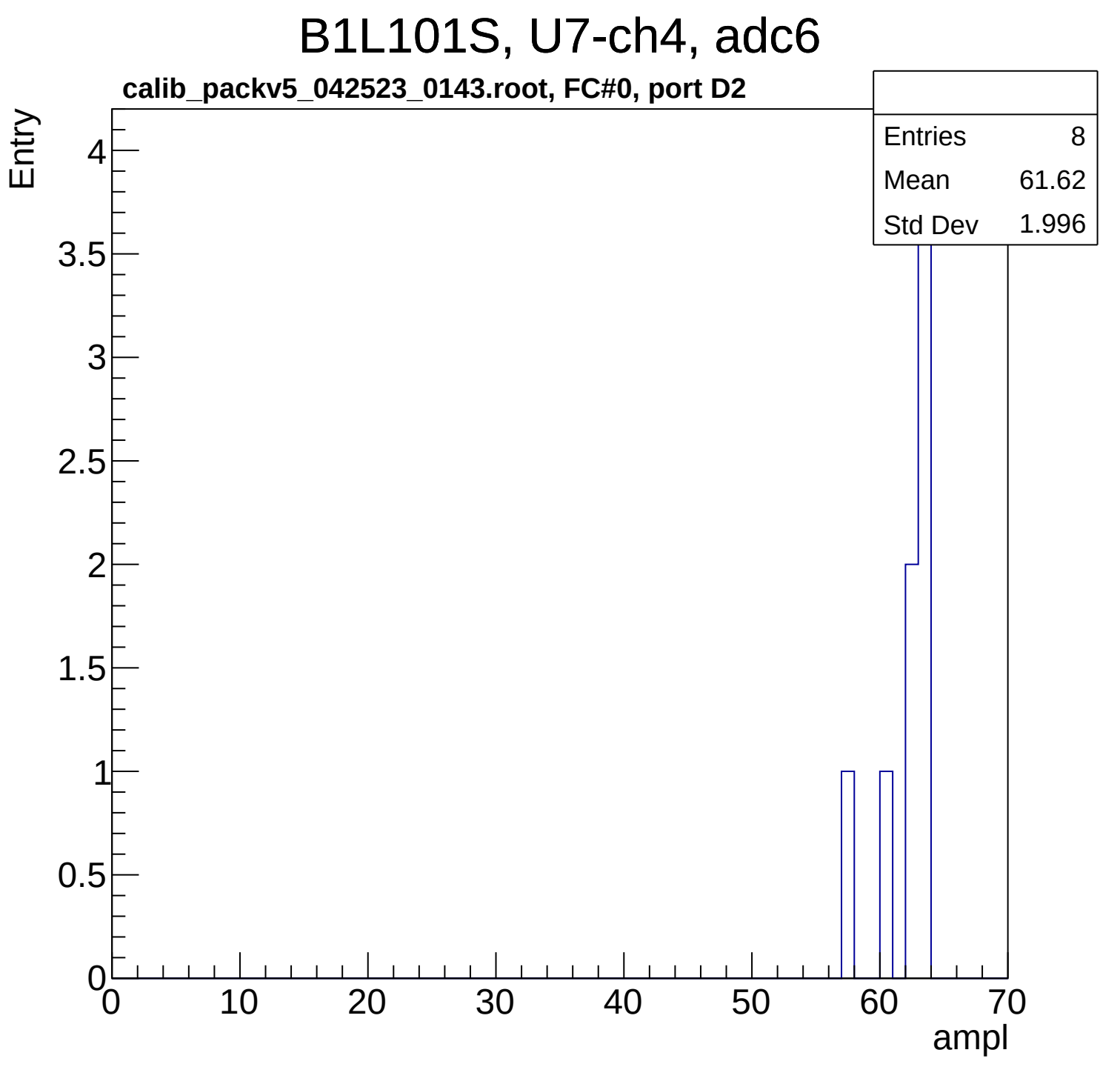
B1L101S, U7-ch4, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 61.62
Std Dev 1.996
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
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60
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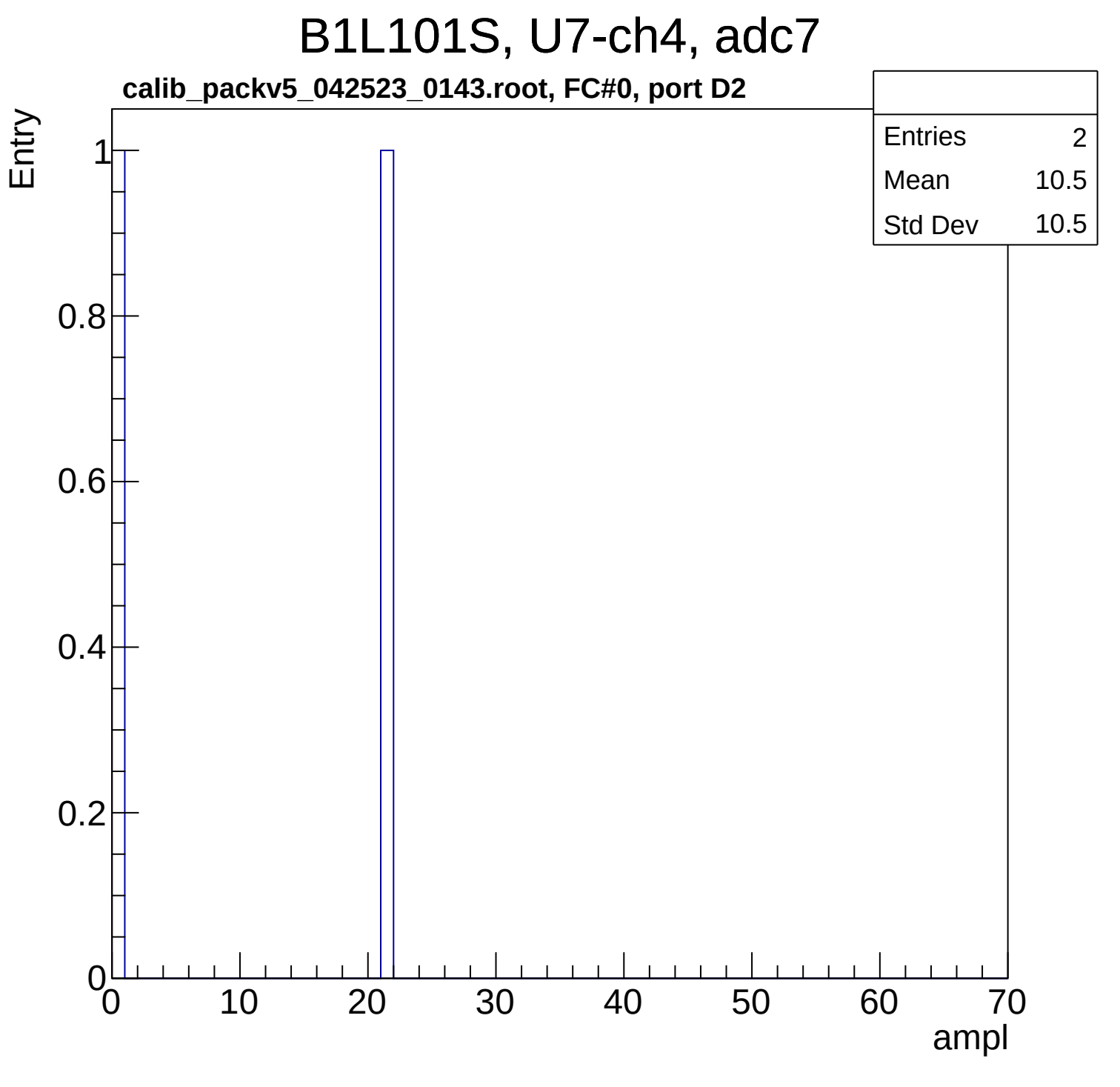
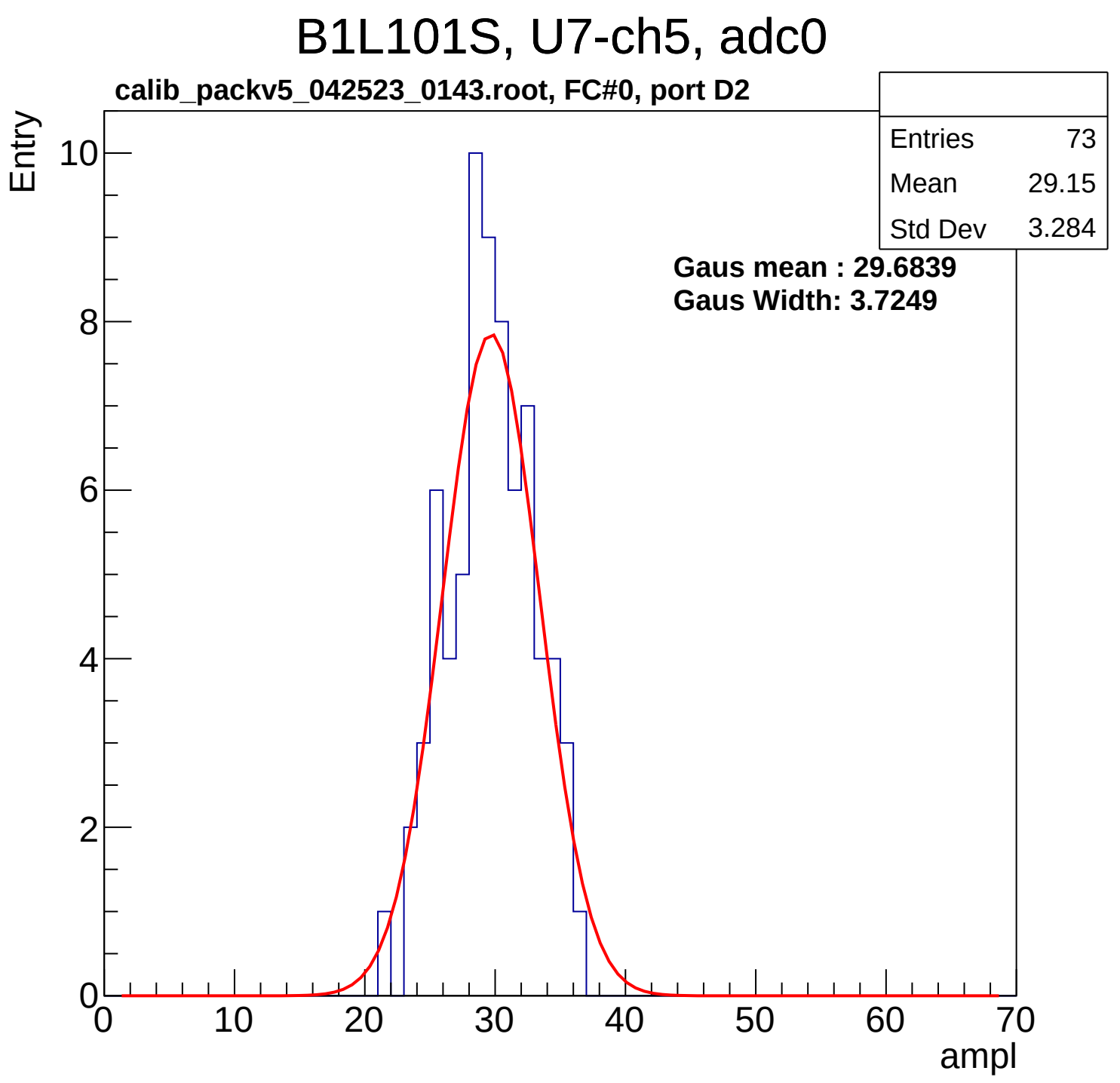
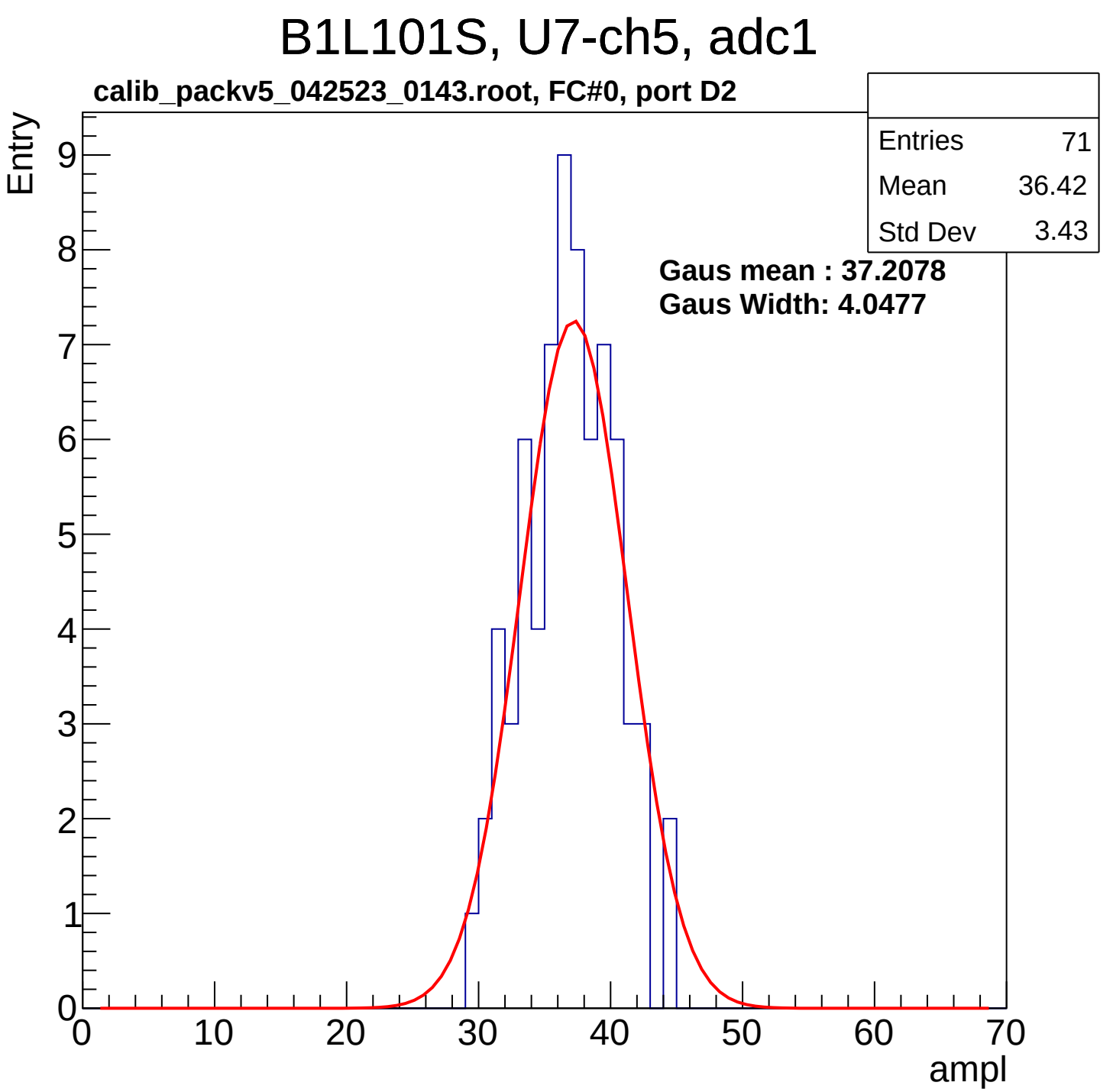

B1L101S, U7-ch4, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 10.5
Std Dev 10.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch5, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 29.15
Std Dev 3.284
Gaus mean : 29.6839
Gaus Width: 3.7249
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch5, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 36.42
Std Dev 3.43
Gaus mean : 37.2078
Gaus Width: 4.0477
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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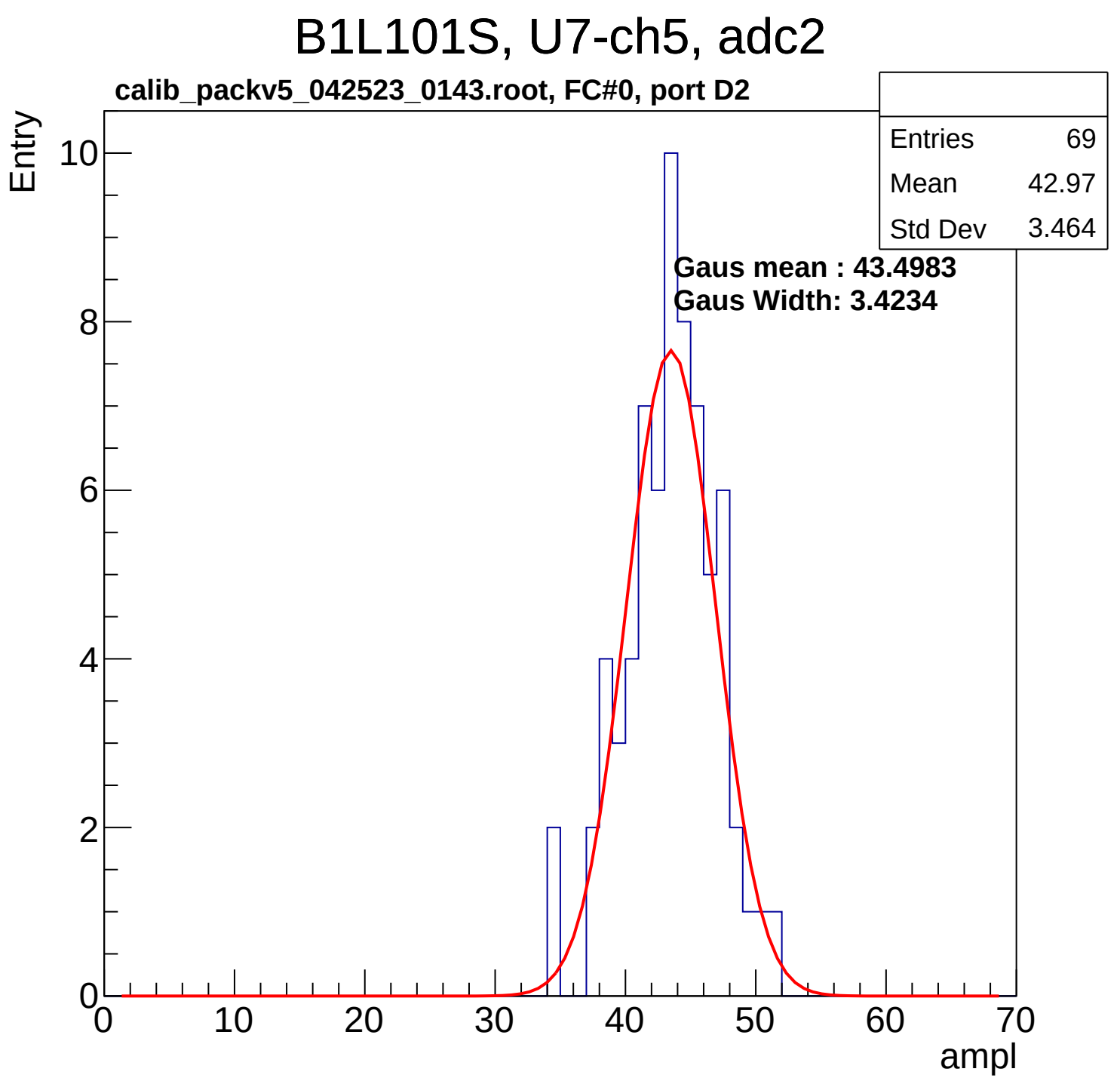
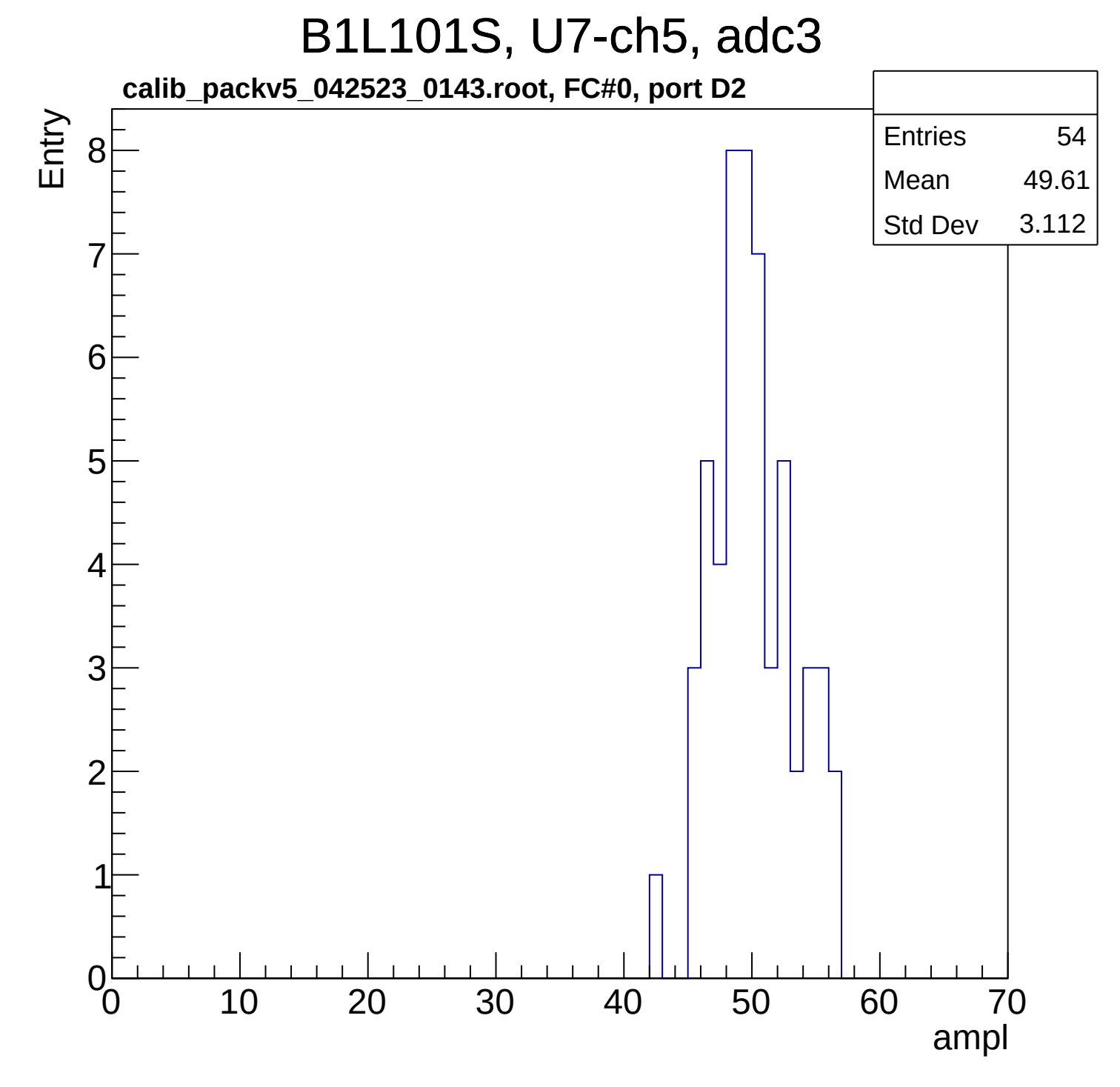

B1L101S, U7-ch5, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 42.97
Std Dev 3.464
Gaus mean : 43.4983
Gaus Width: 3.4234
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch5, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 49.61
Std Dev 3.112
Entry
ampl
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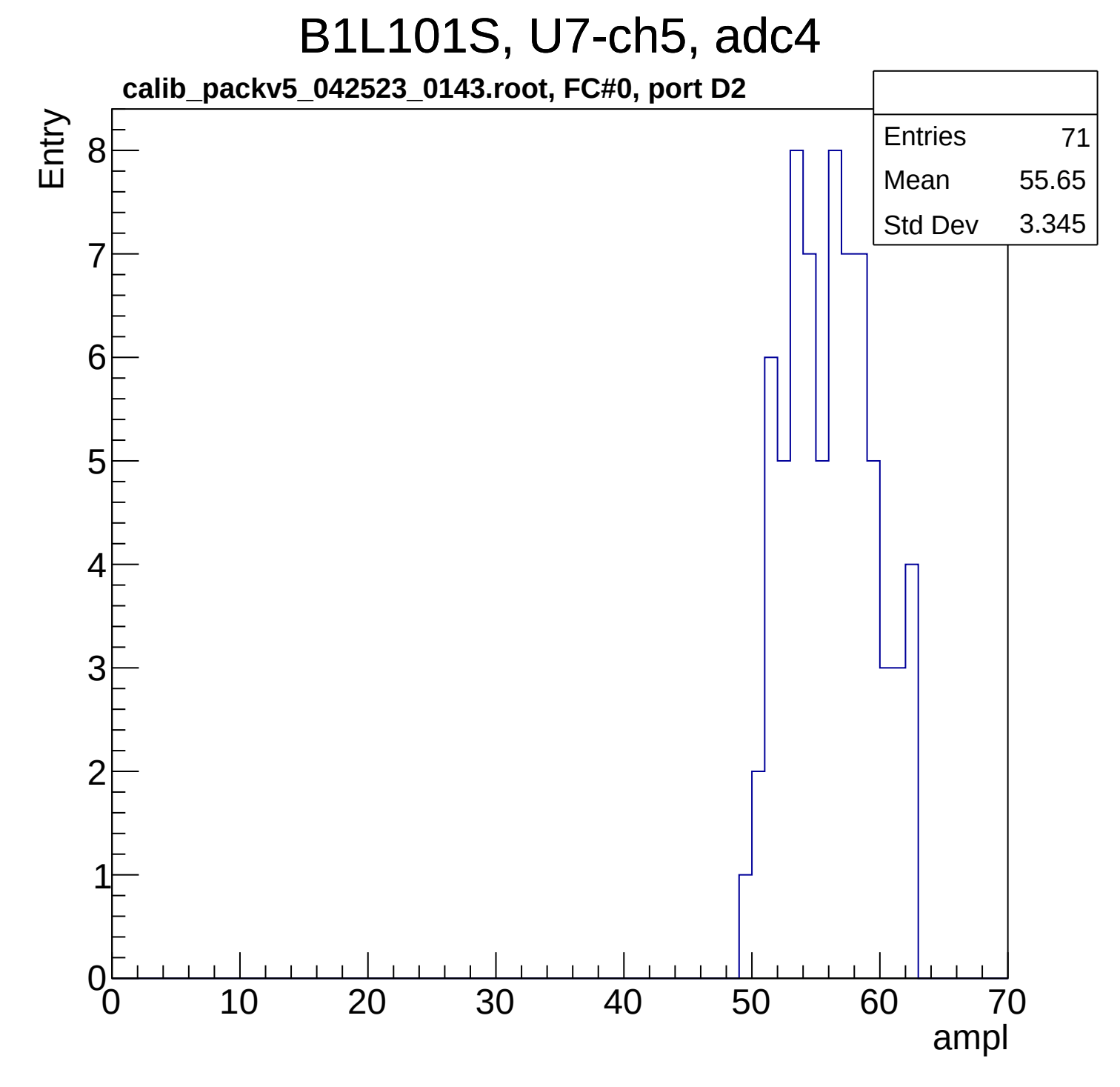
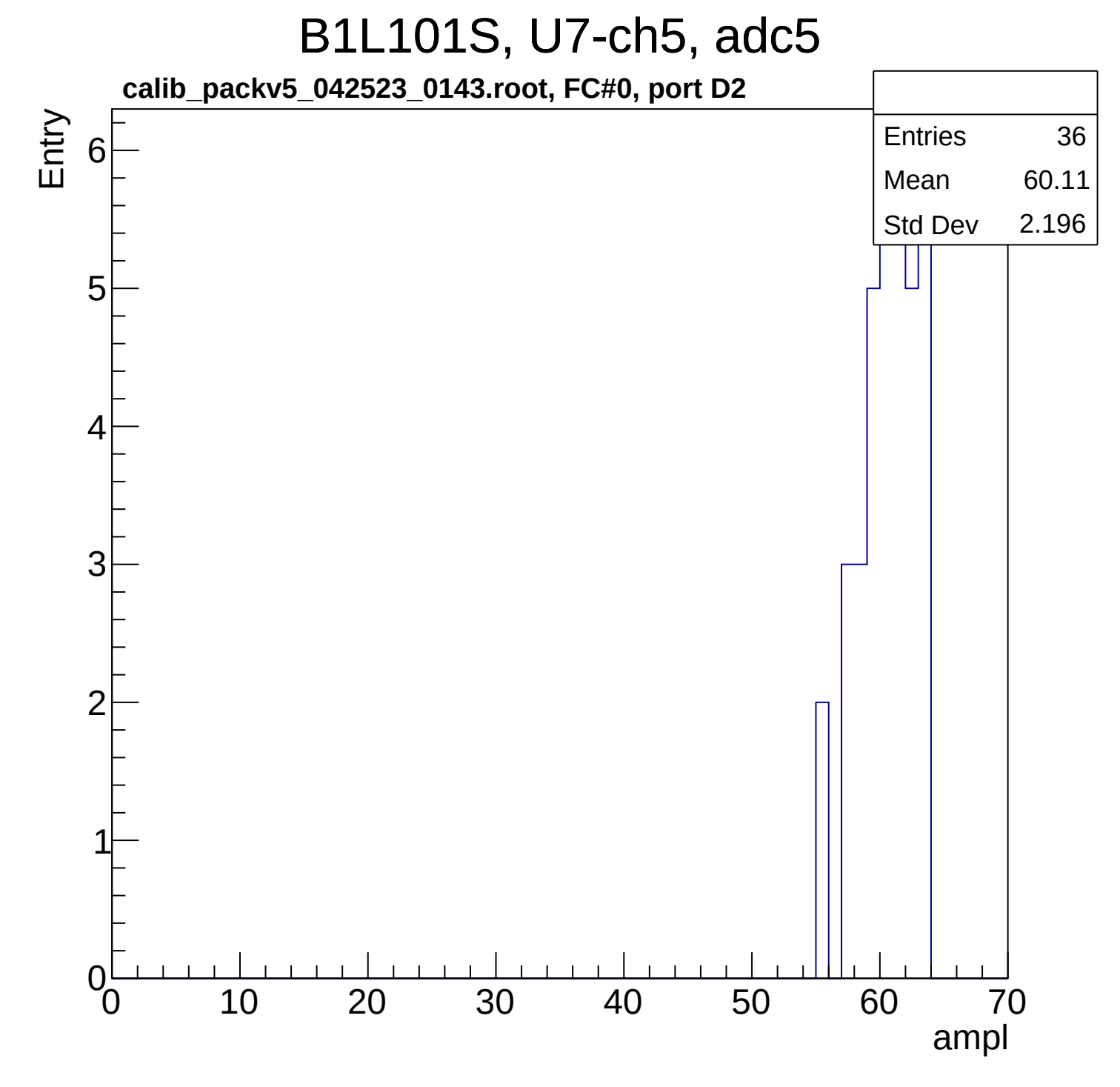
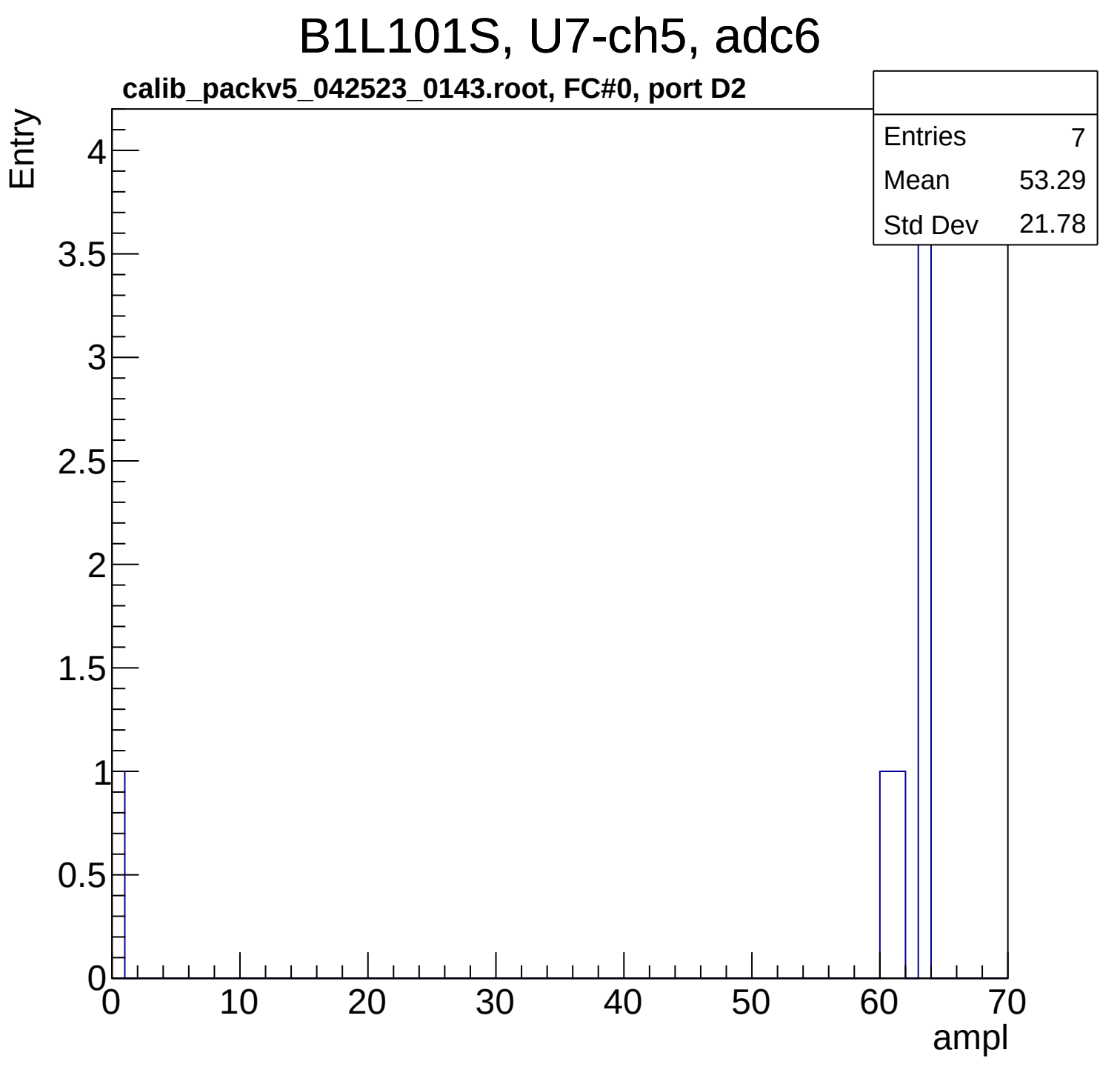
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch5, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 55.65
Std Dev 3.345
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch5, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 36
Mean 60.11
Std Dev 2.196
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch5, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 53.29
Std Dev 21.78
Entry
ampl
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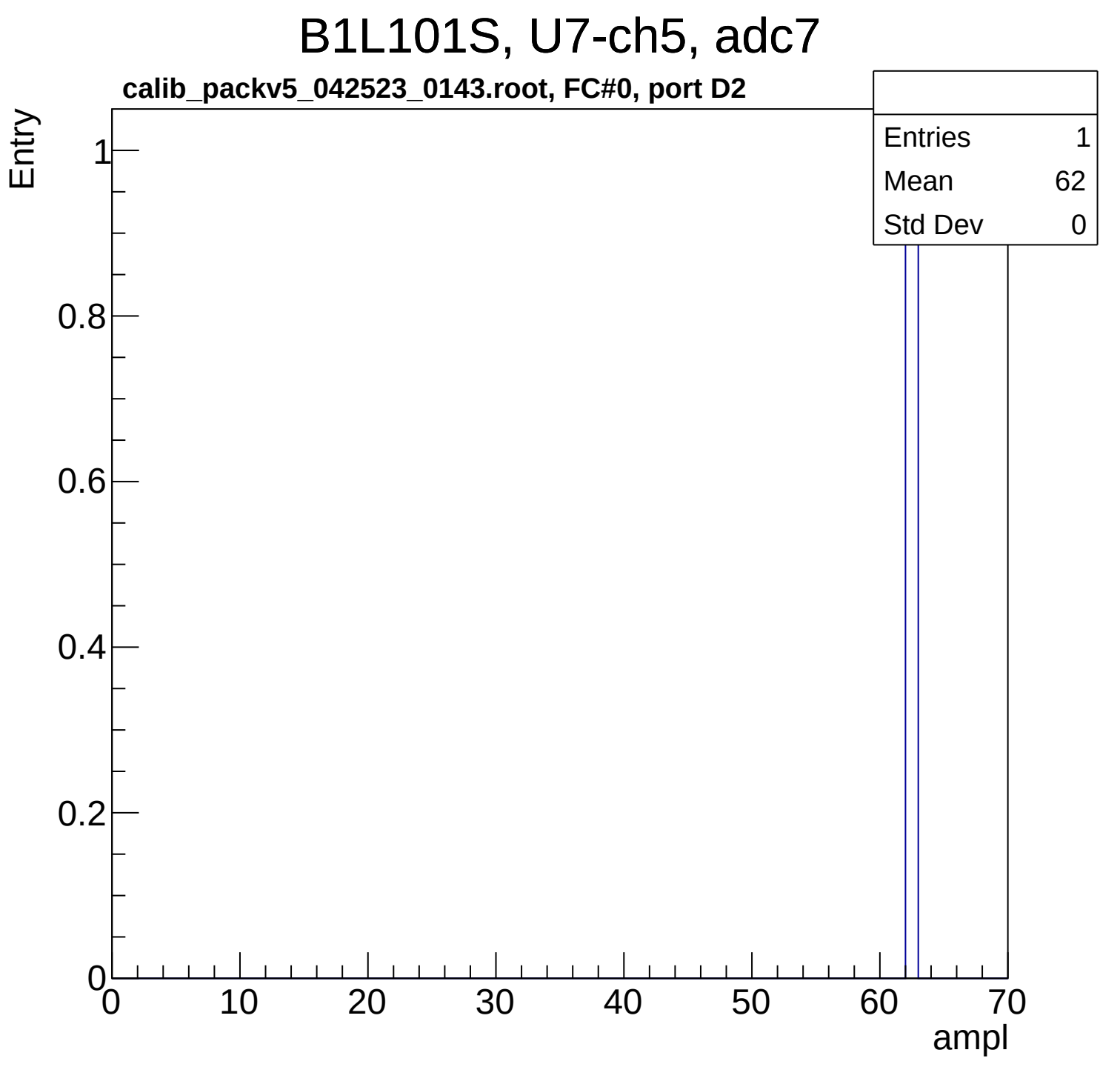
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L101S, U7-ch5, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 62
Std Dev 0
Entry
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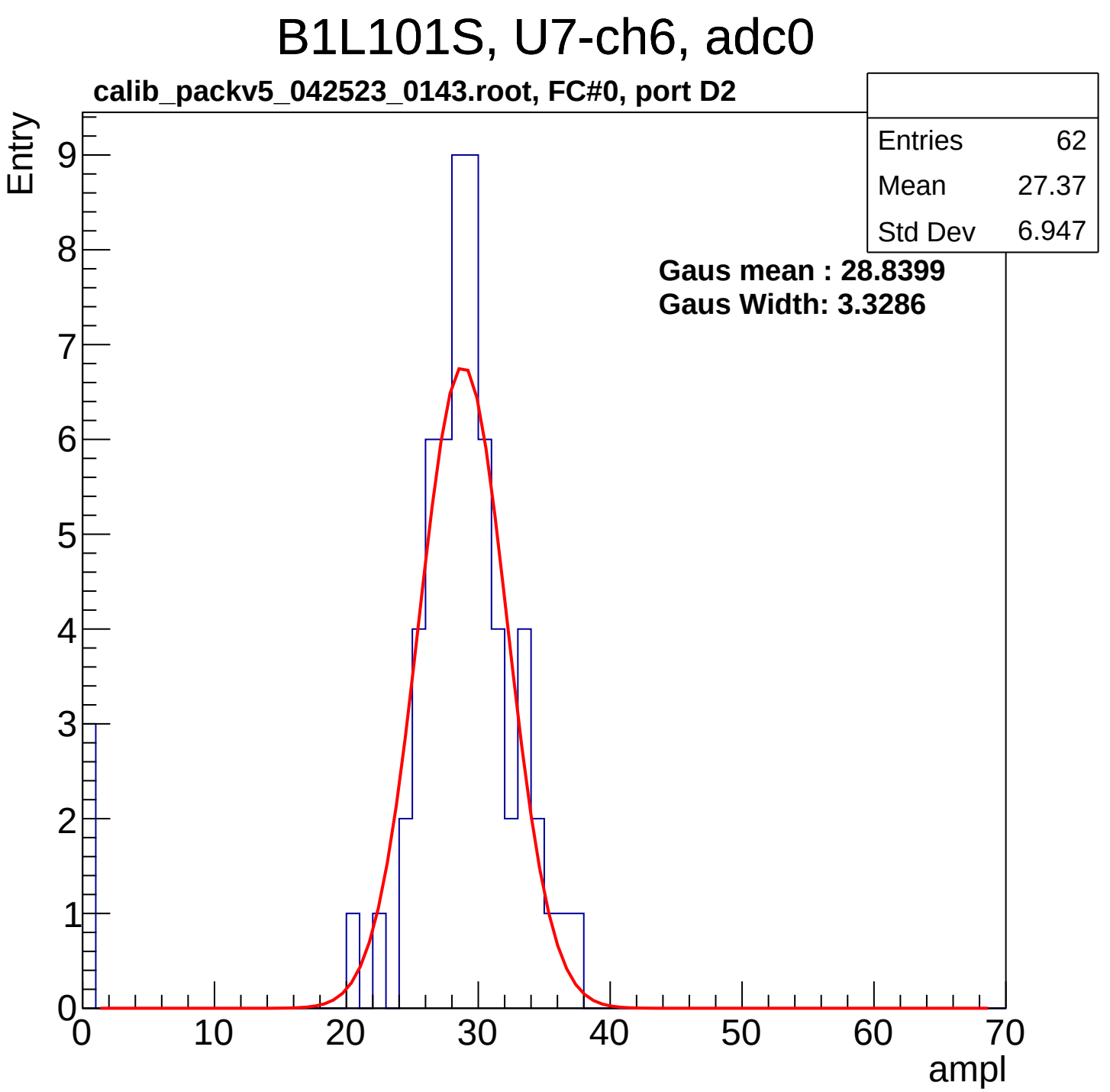
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch6, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 27.37
Std Dev 6.947
Gaus mean : 28.8399
Gaus Width: 3.3286
Entry
ampl
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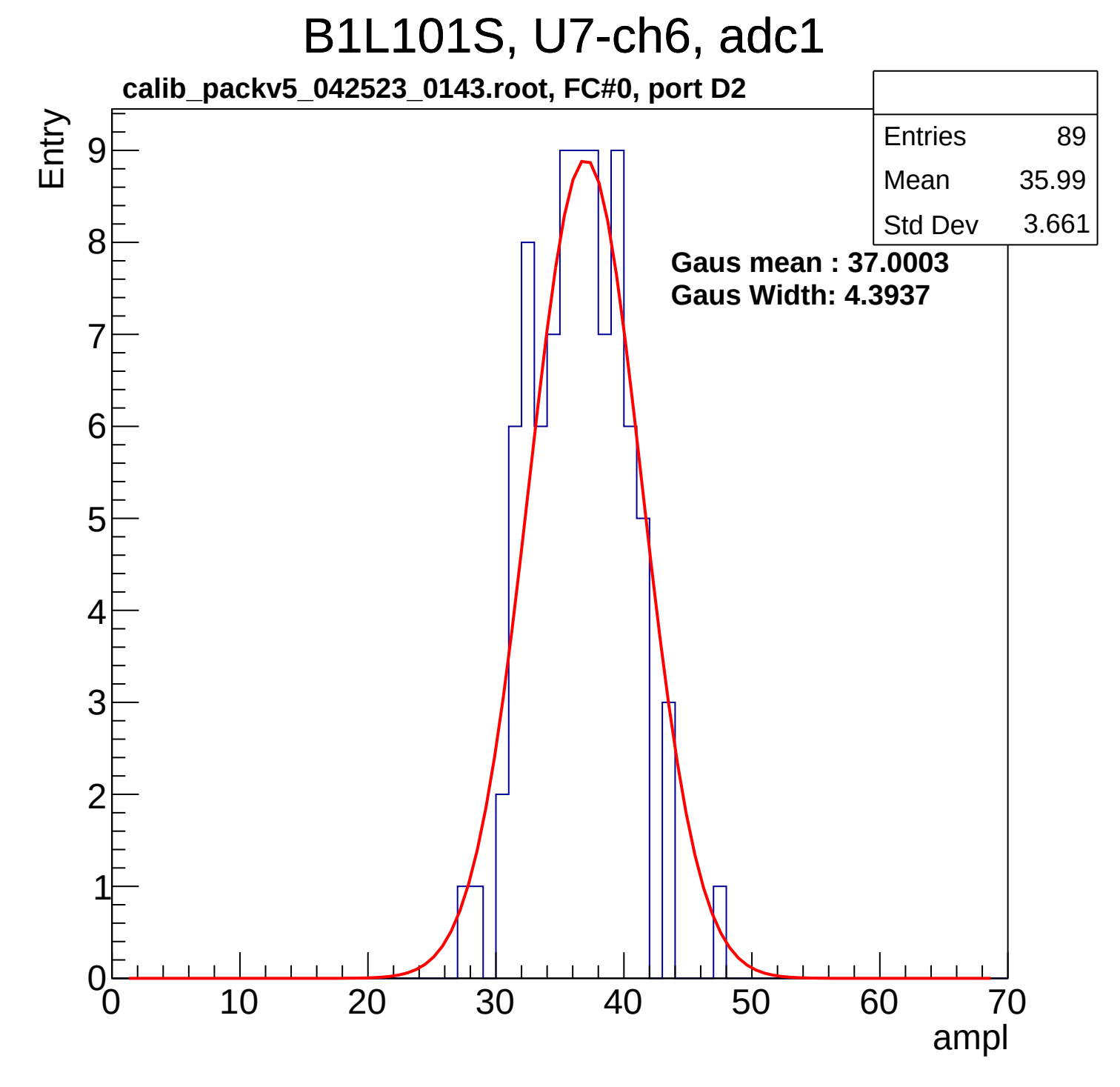
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L101S, U7-ch6, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 89
Mean 35.99
Std Dev 3.661
Gaus mean : 37.0003
Gaus Width: 4.3937
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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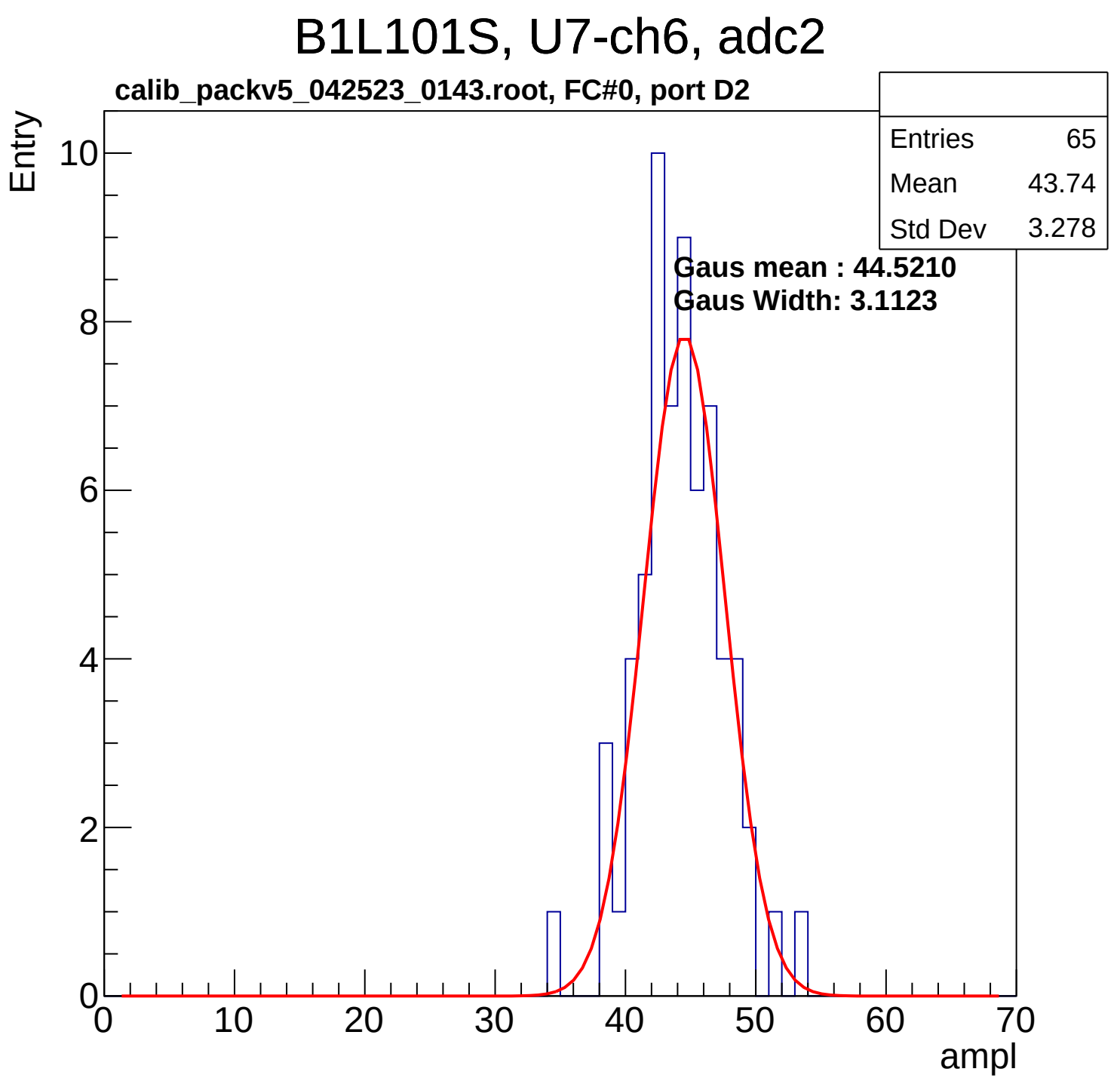
B1L101S, U7-ch6, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 43.74
Std Dev 3.278
Gaus mean : 44.5210
Gaus Width: 3.1123
Entry
ampl
0
2
4
6
8
10
0
10
20
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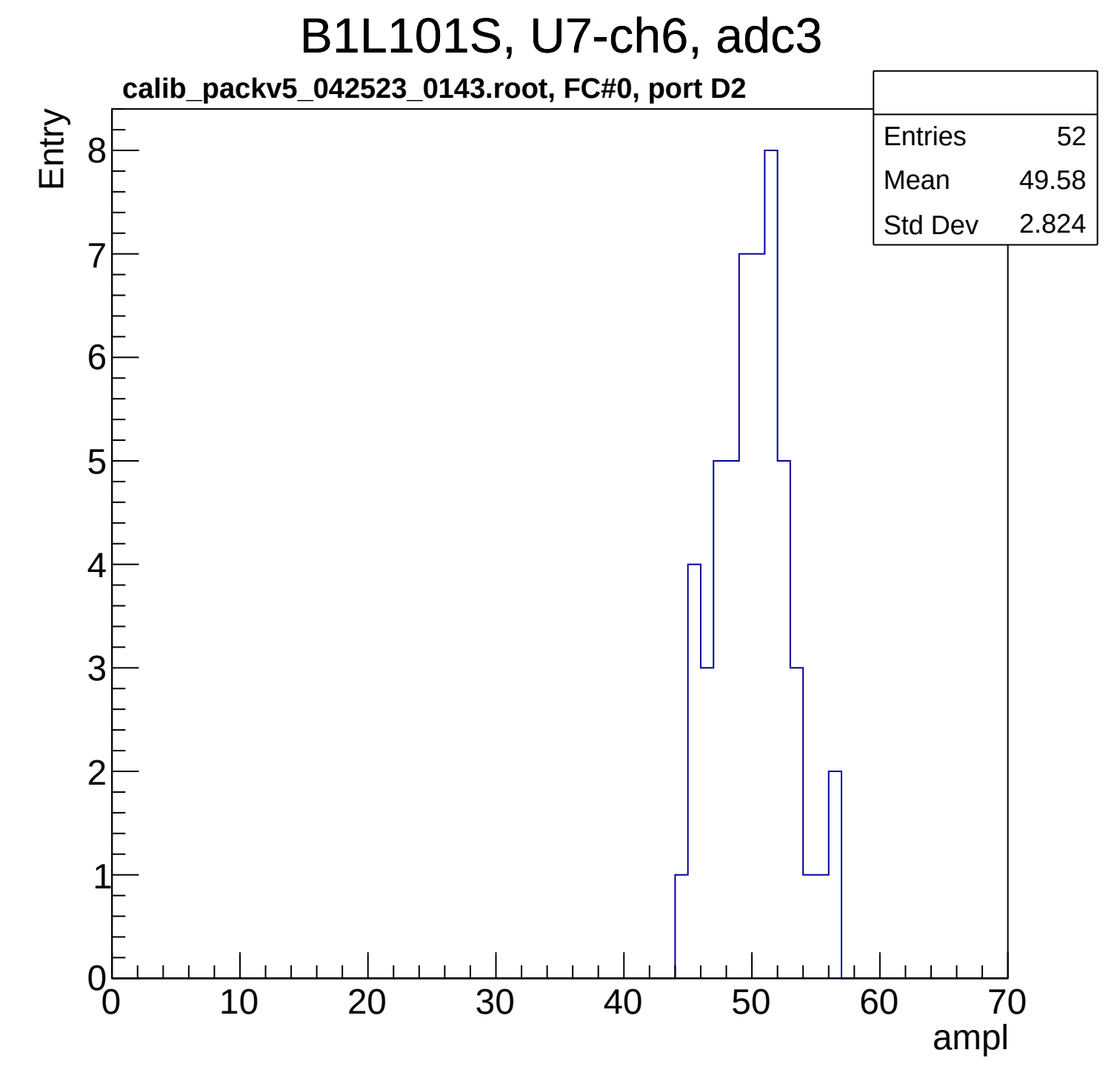
40
50
60
70


B1L101S, U7-ch6, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 49.58
Std Dev 2.824
Entry
ampl
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1
2
3
4
5
6
7
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0
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40
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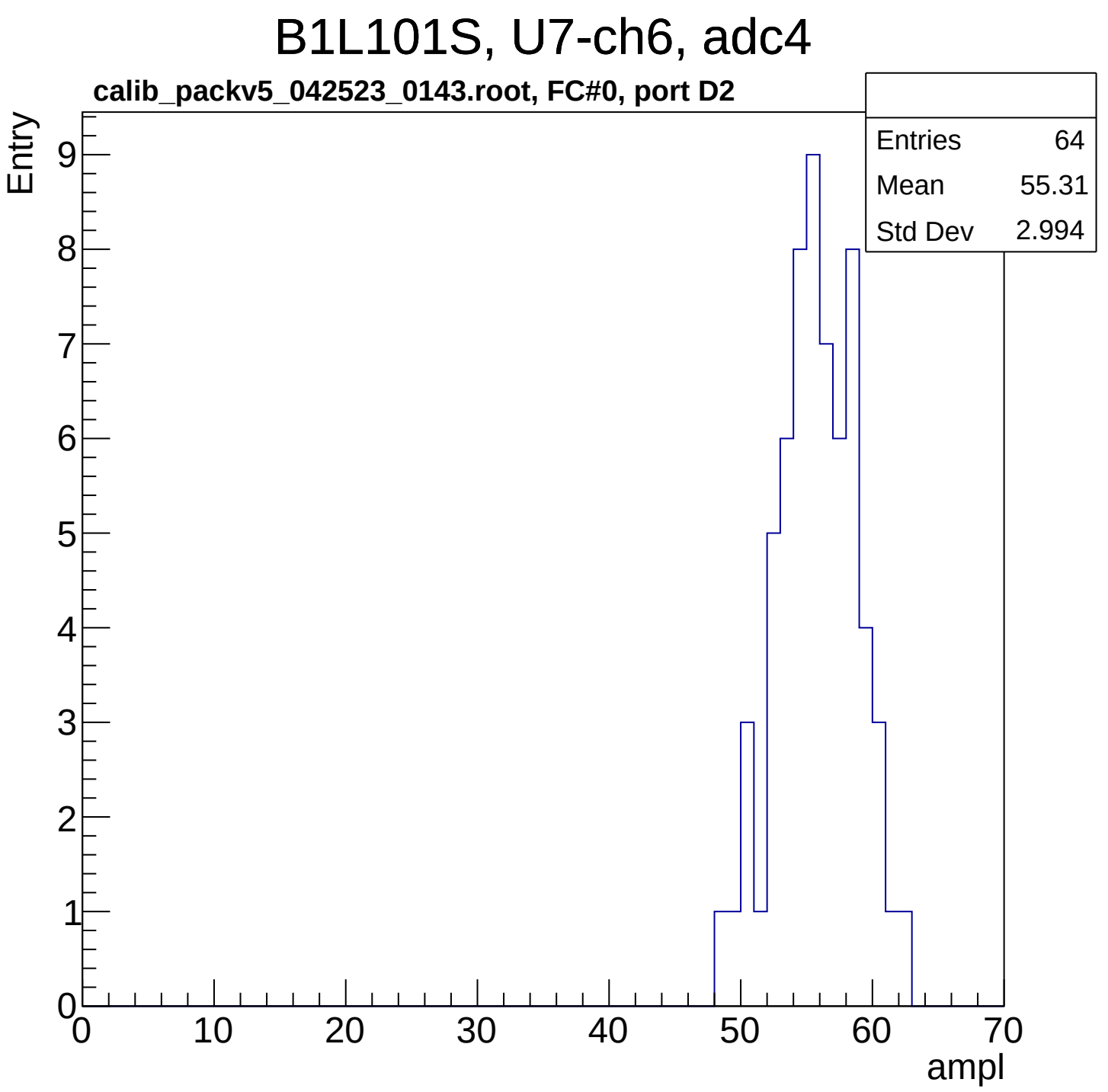
60
70


B1L101S, U7-ch6, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 55.31
Std Dev 2.994
Entry
ampl
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6
7
8
9
0
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60
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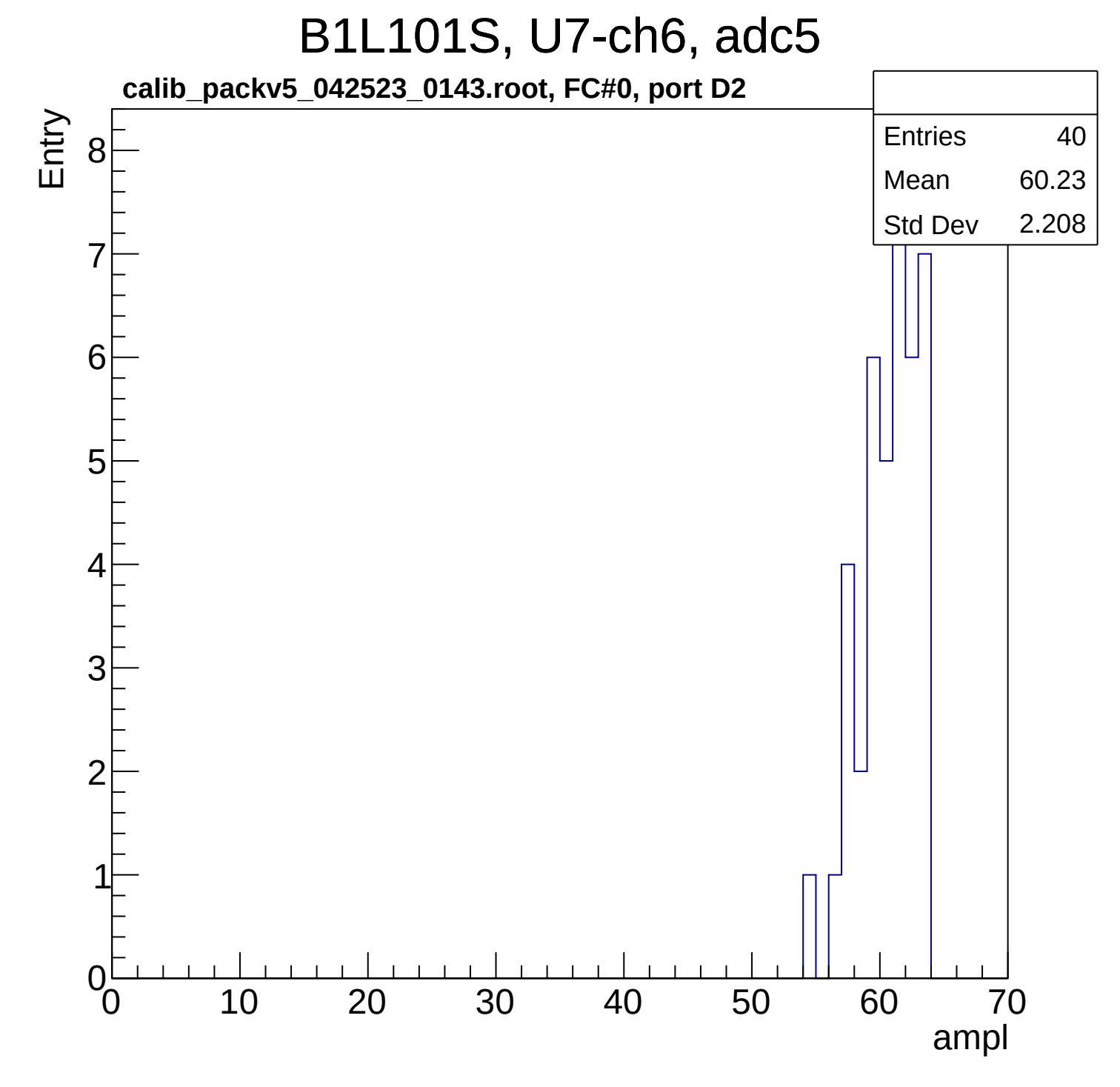
B1L101S, U7-ch6, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 40
Mean 60.23
Std Dev 2.208
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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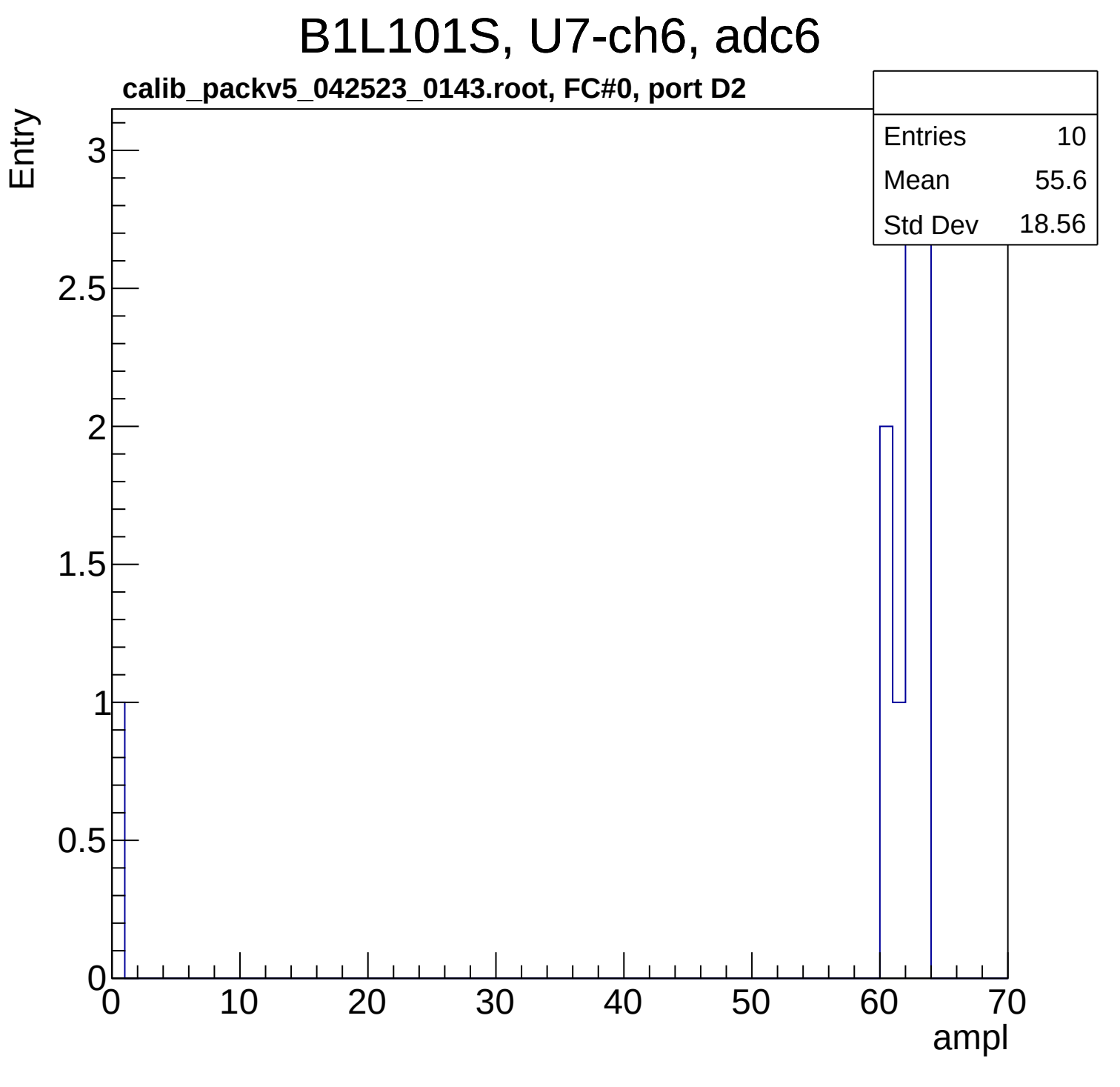
40
50
60
70


B1L101S, U7-ch6, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 55.6
Std Dev 18.56
Entry
ampl
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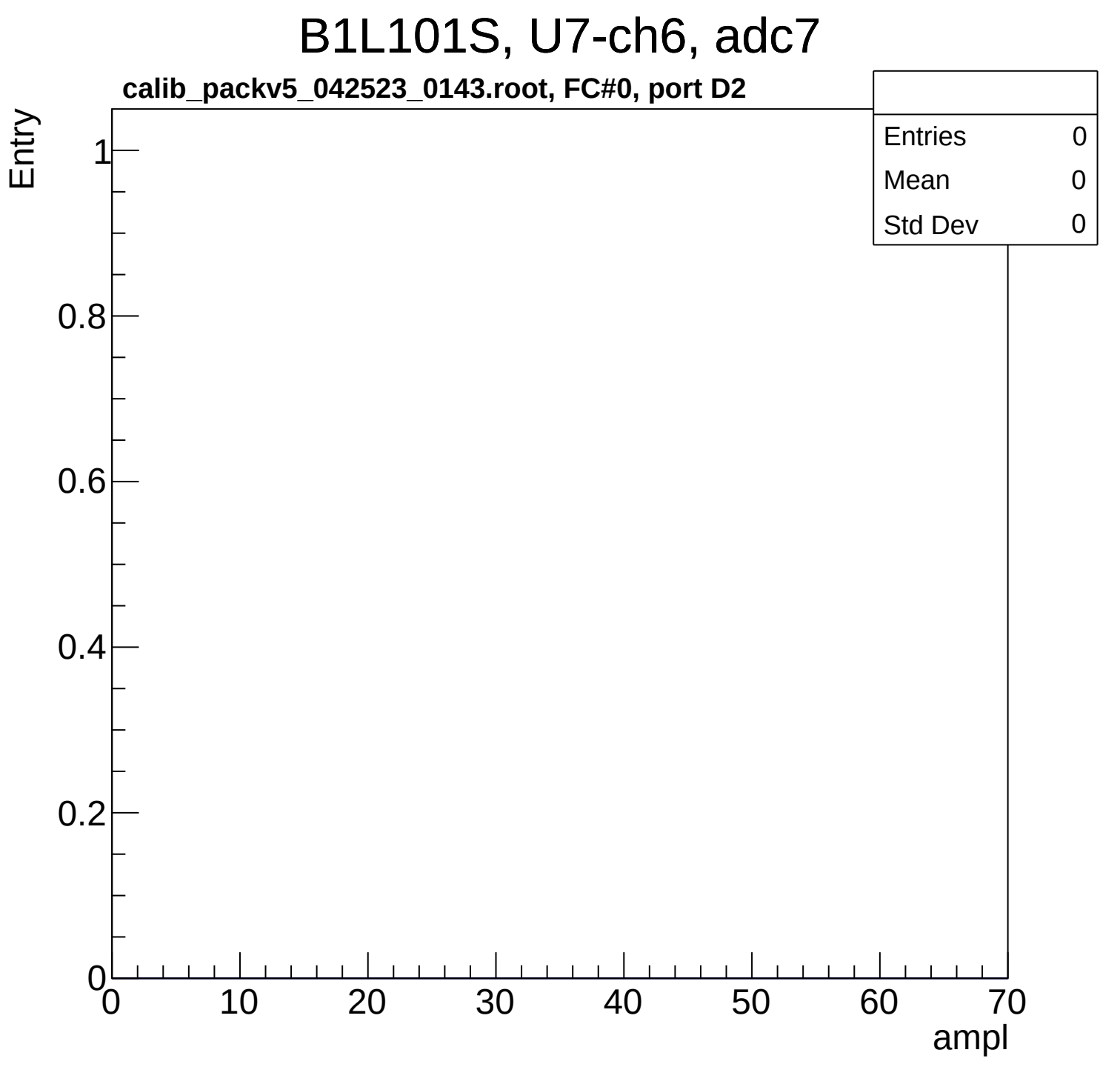
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U7-ch6, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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0.6
0.4
0.2
0
0
10
20
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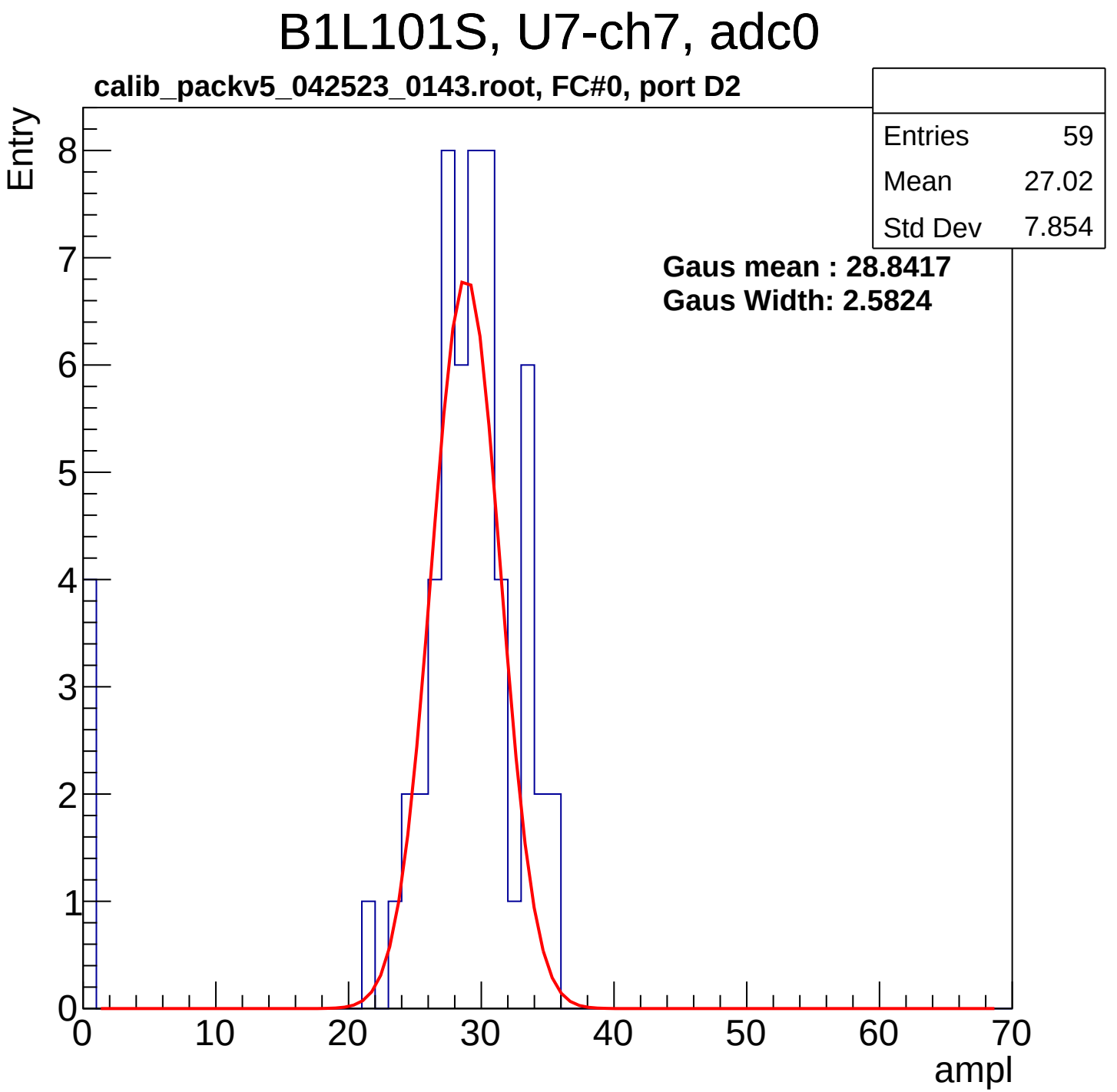
50
60
70
ampl


B1L101S, U7-ch7, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 27.02
Std Dev 7.854
Gaus mean : 28.8417
Gaus Width: 2.5824
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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60
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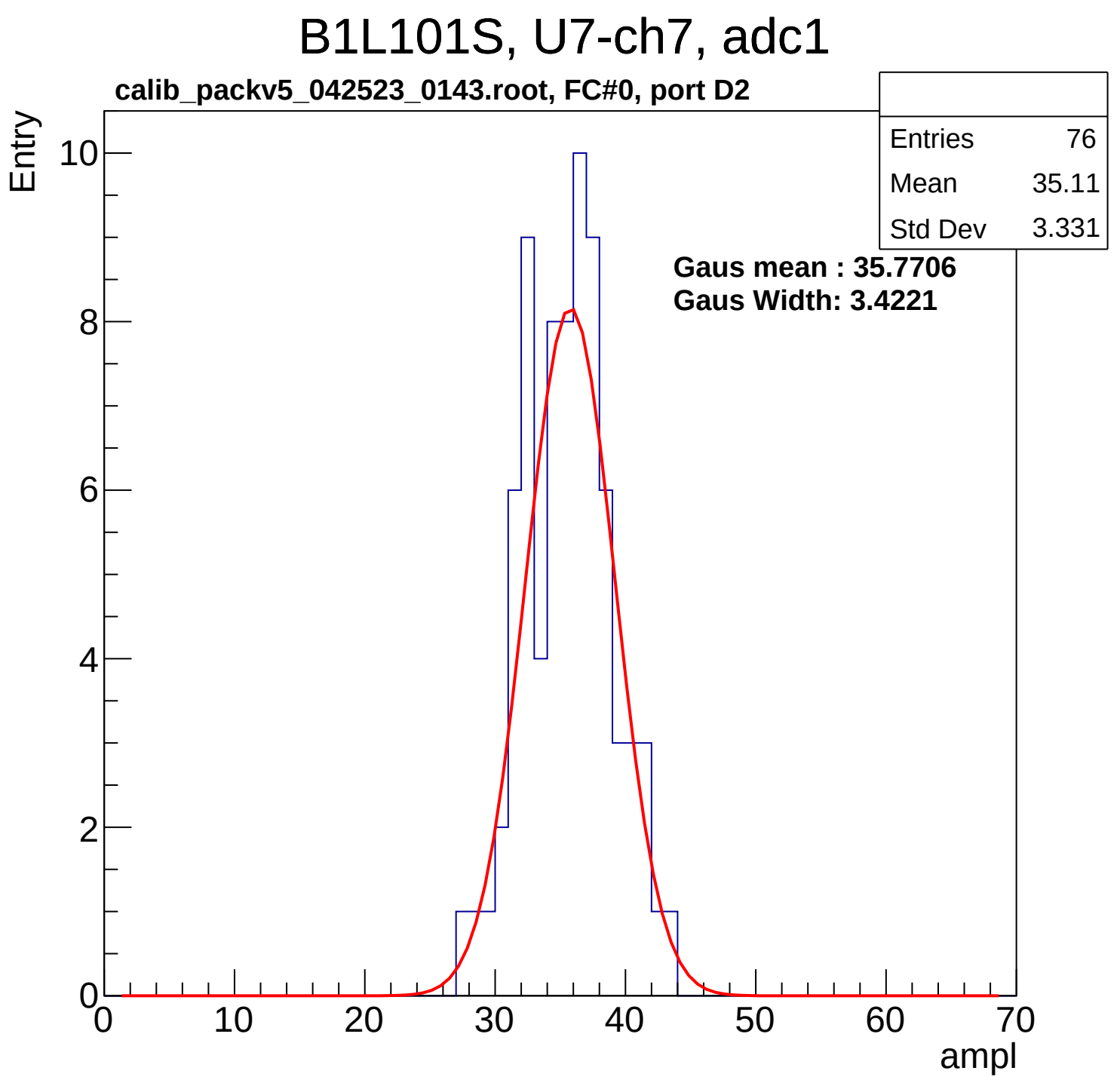
B1L101S, U7-ch7, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 35.11
Std Dev 3.331
Gaus mean : 35.7706
Gaus Width: 3.4221
Entry
ampl
0
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4
6
8
10
0
10
20
30
40
50
60
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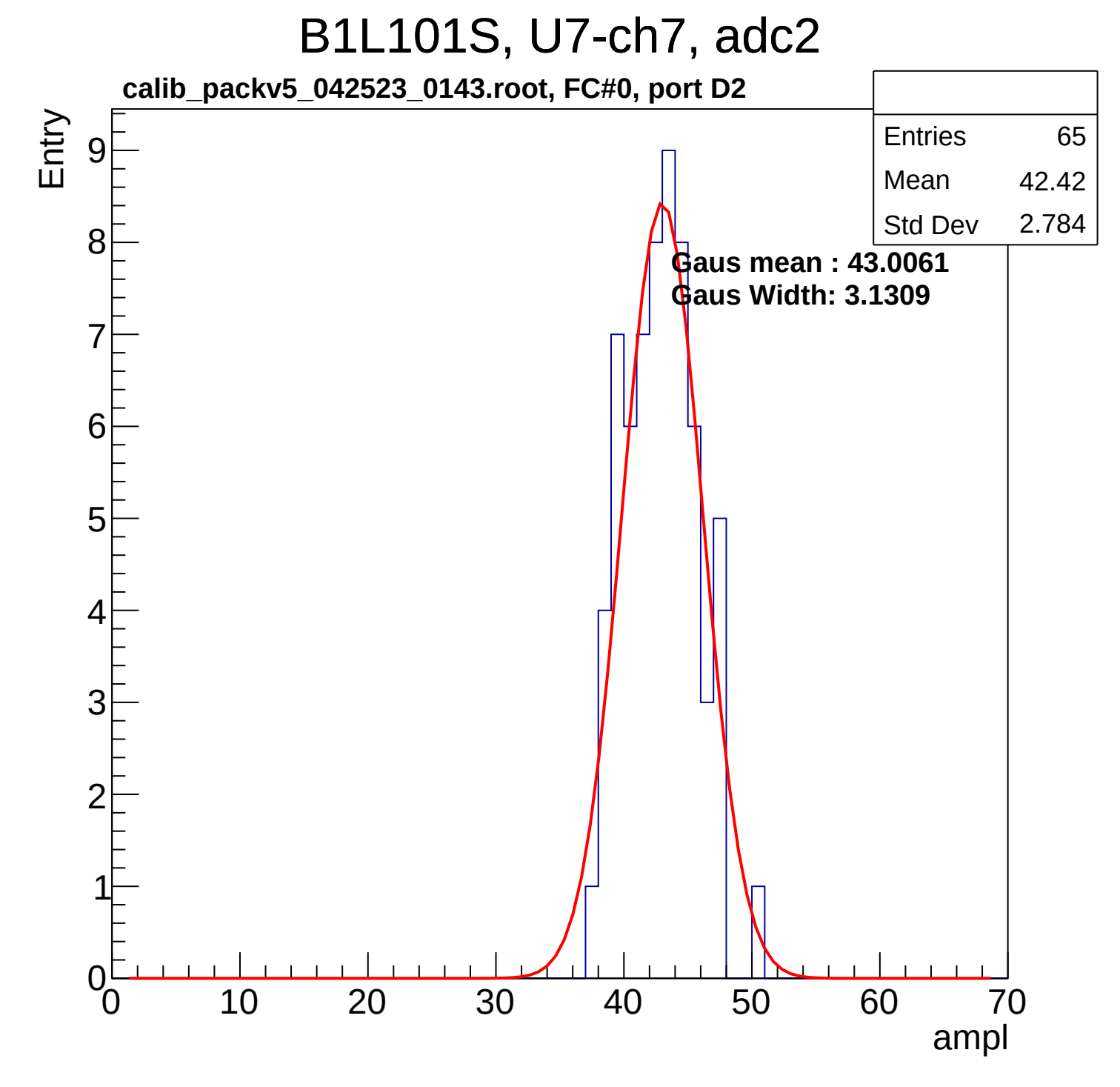
B1L101S, U7-ch7, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 42.42
Std Dev 2.784
Gaus mean : 43.0061
Gaus Width: 3.1309
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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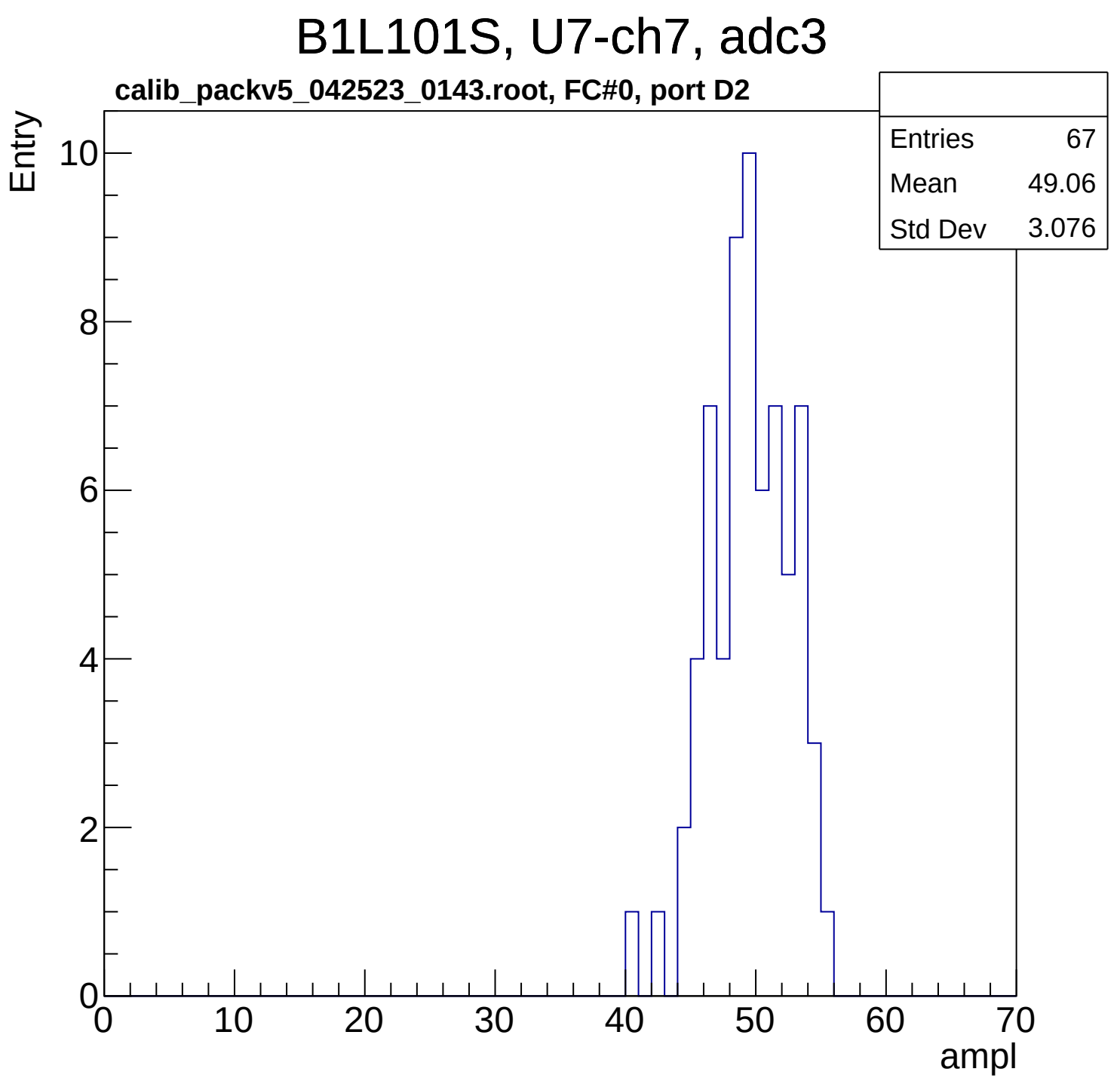
B1L101S, U7-ch7, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 49.06
Std Dev 3.076
Entry
ampl
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4
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60
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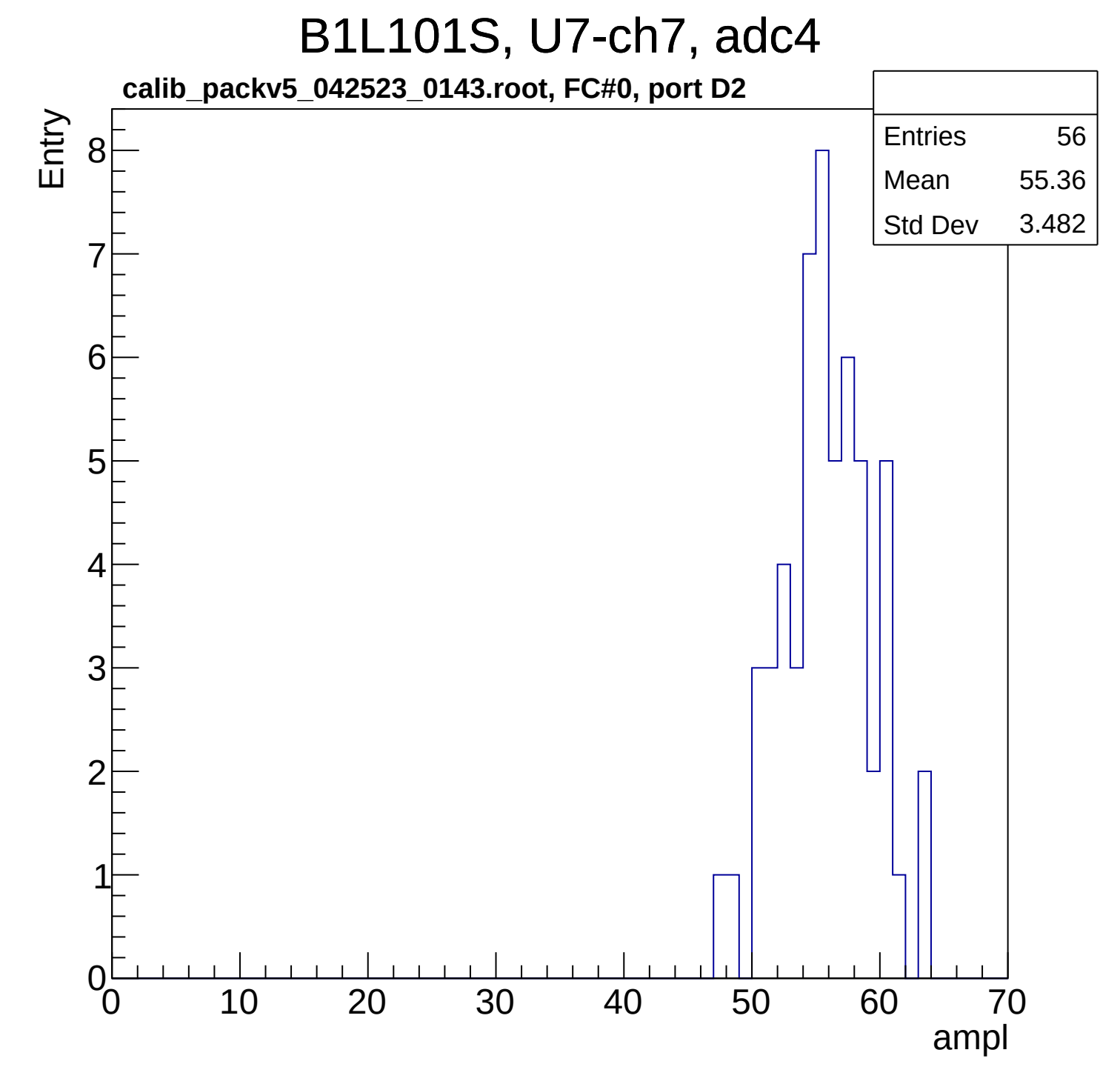
B1L101S, U7-ch7, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 55.36
Std Dev 3.482
Entry
ampl
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3
4
5
6
7
8
0
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20
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40
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60
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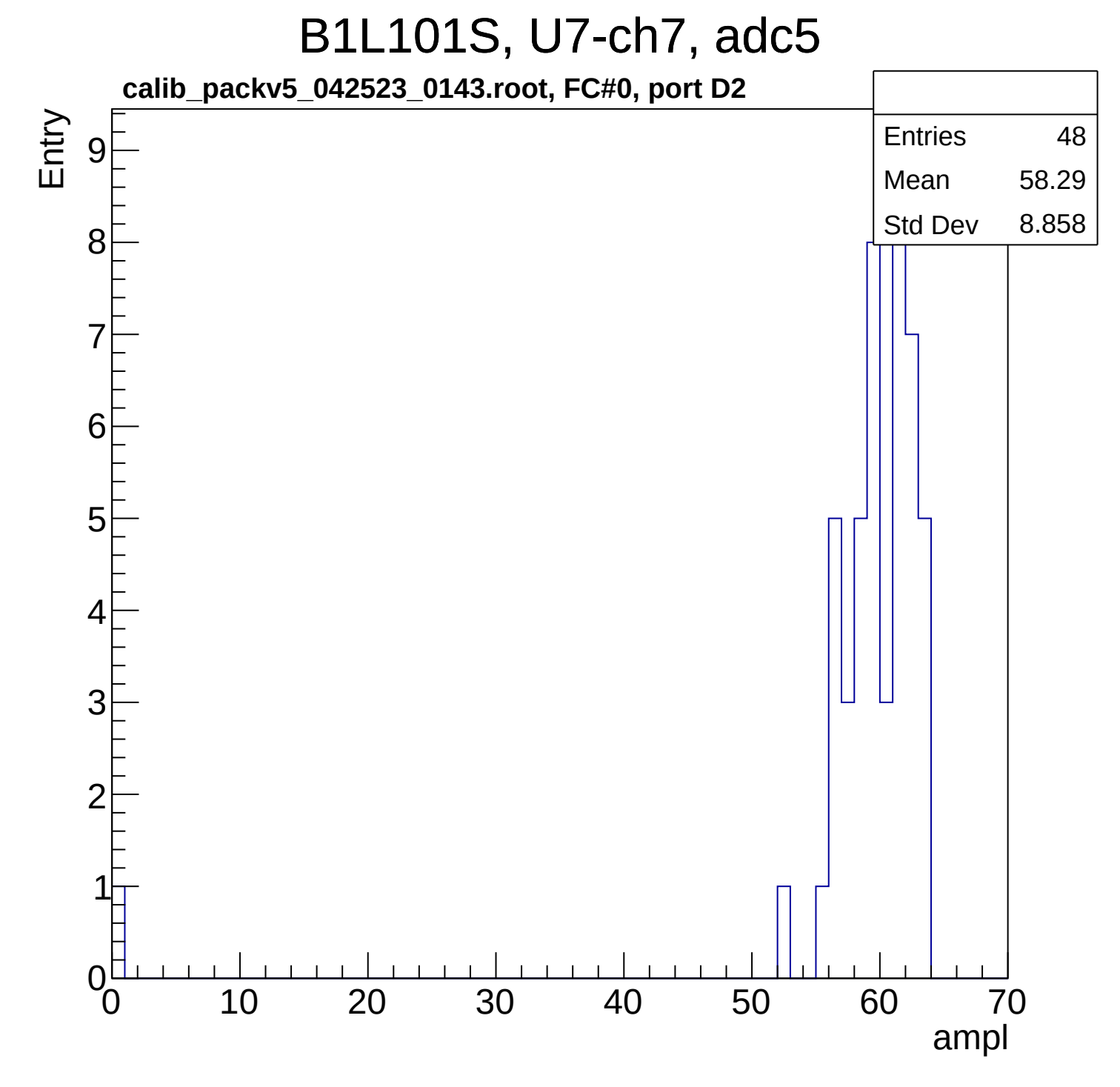
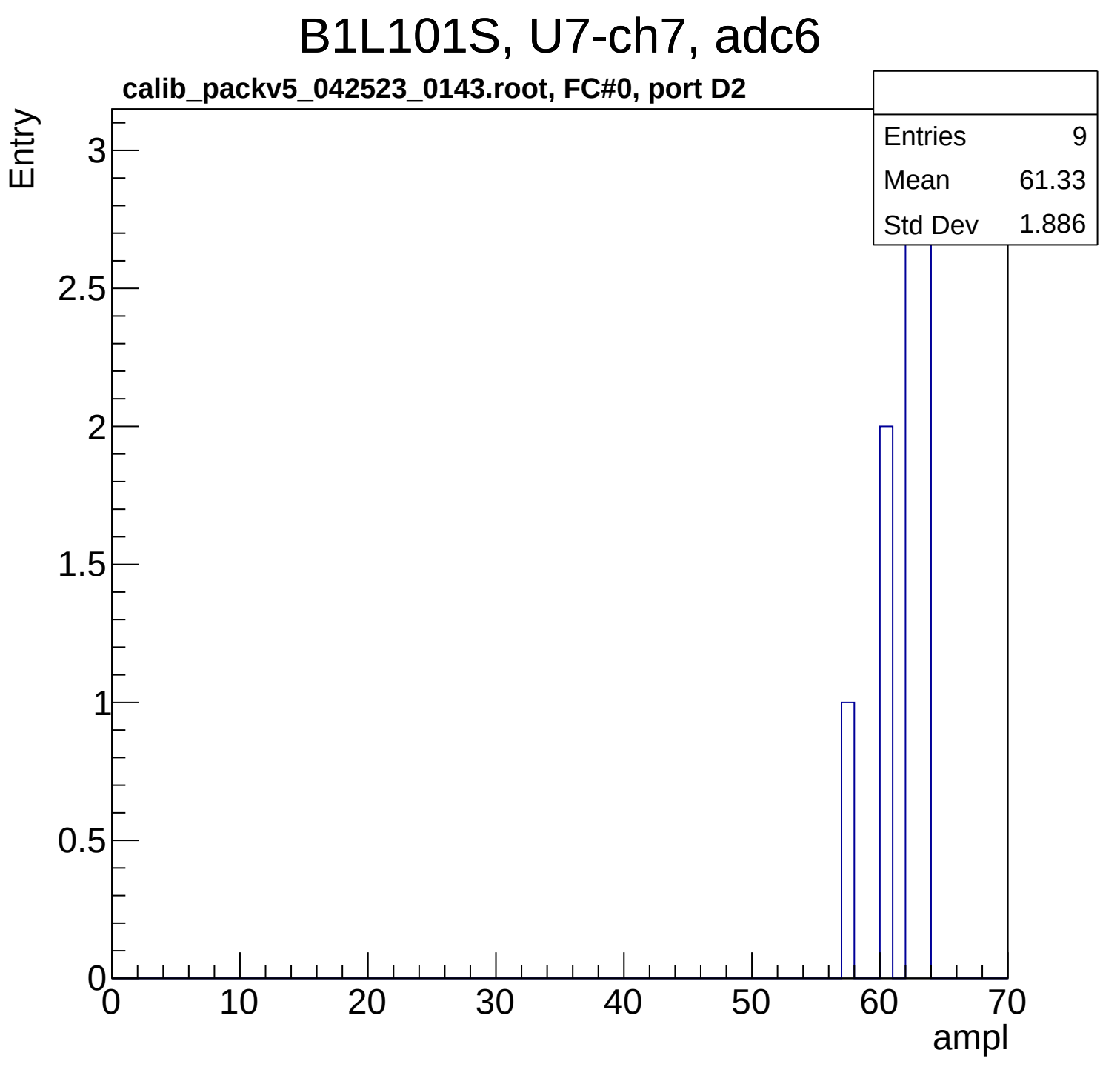

B1L101S, U7-ch7, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 58.29
Std Dev 8.858
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch7, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 61.33
Std Dev 1.886
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
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40
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60
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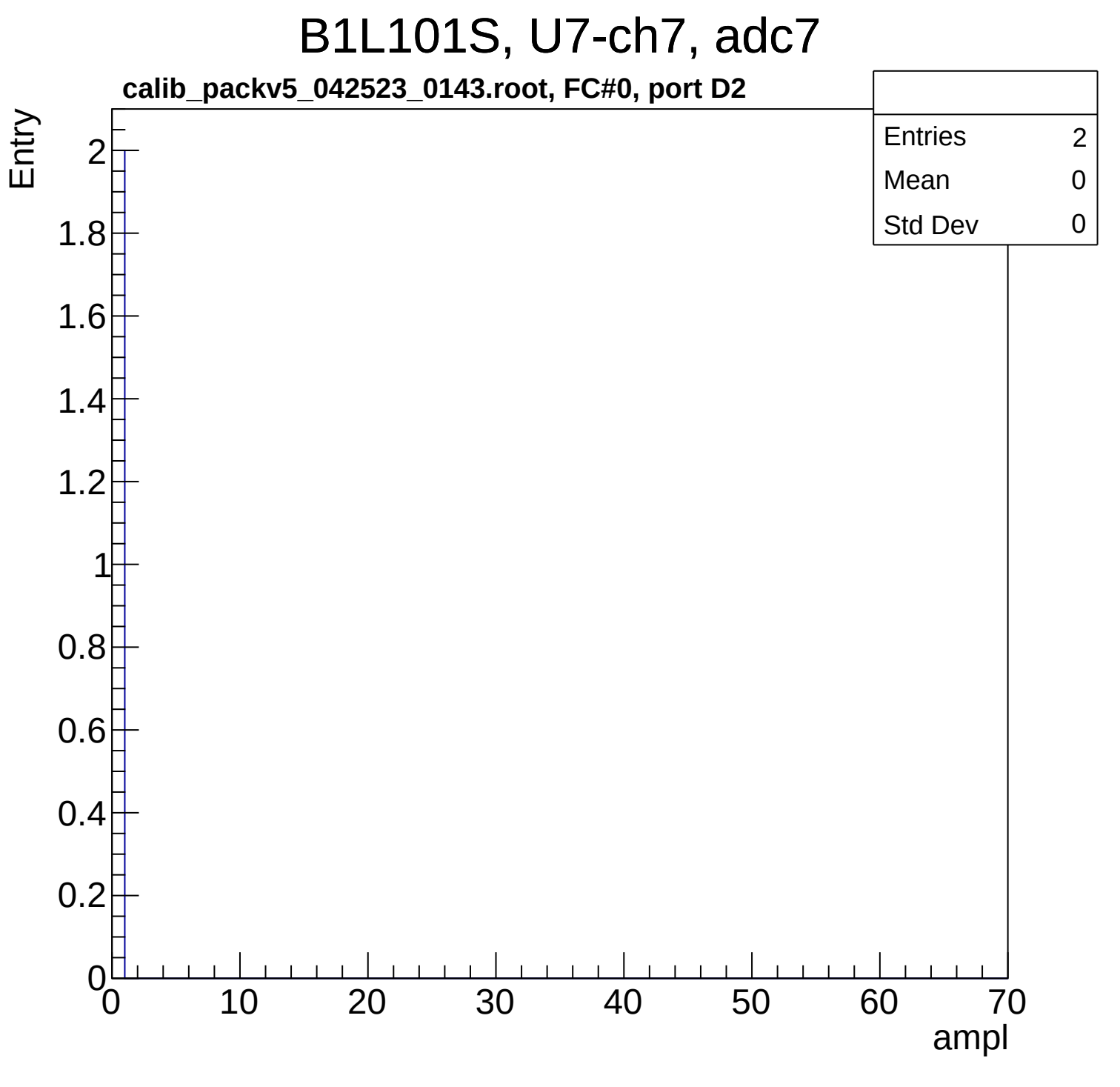
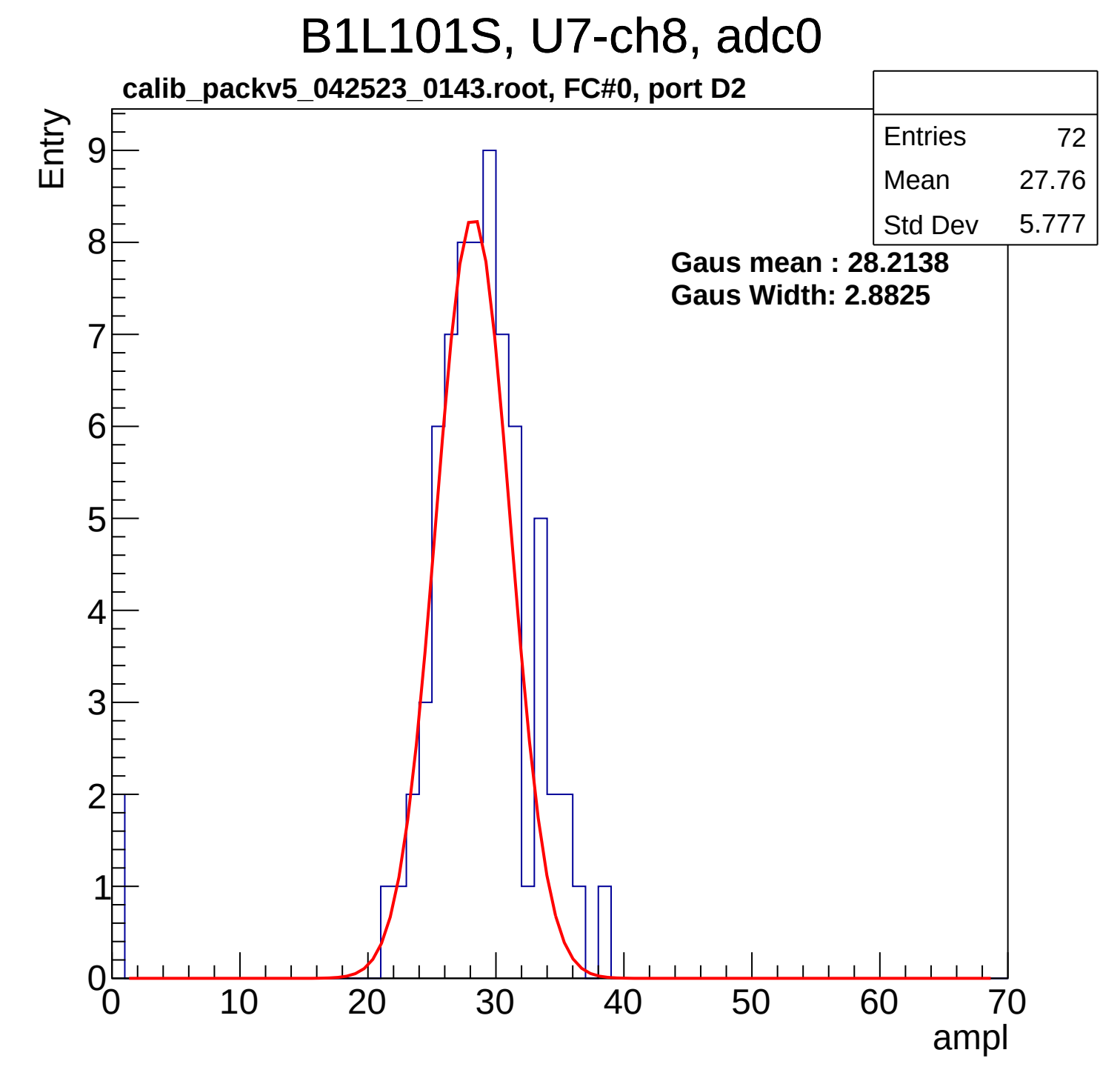
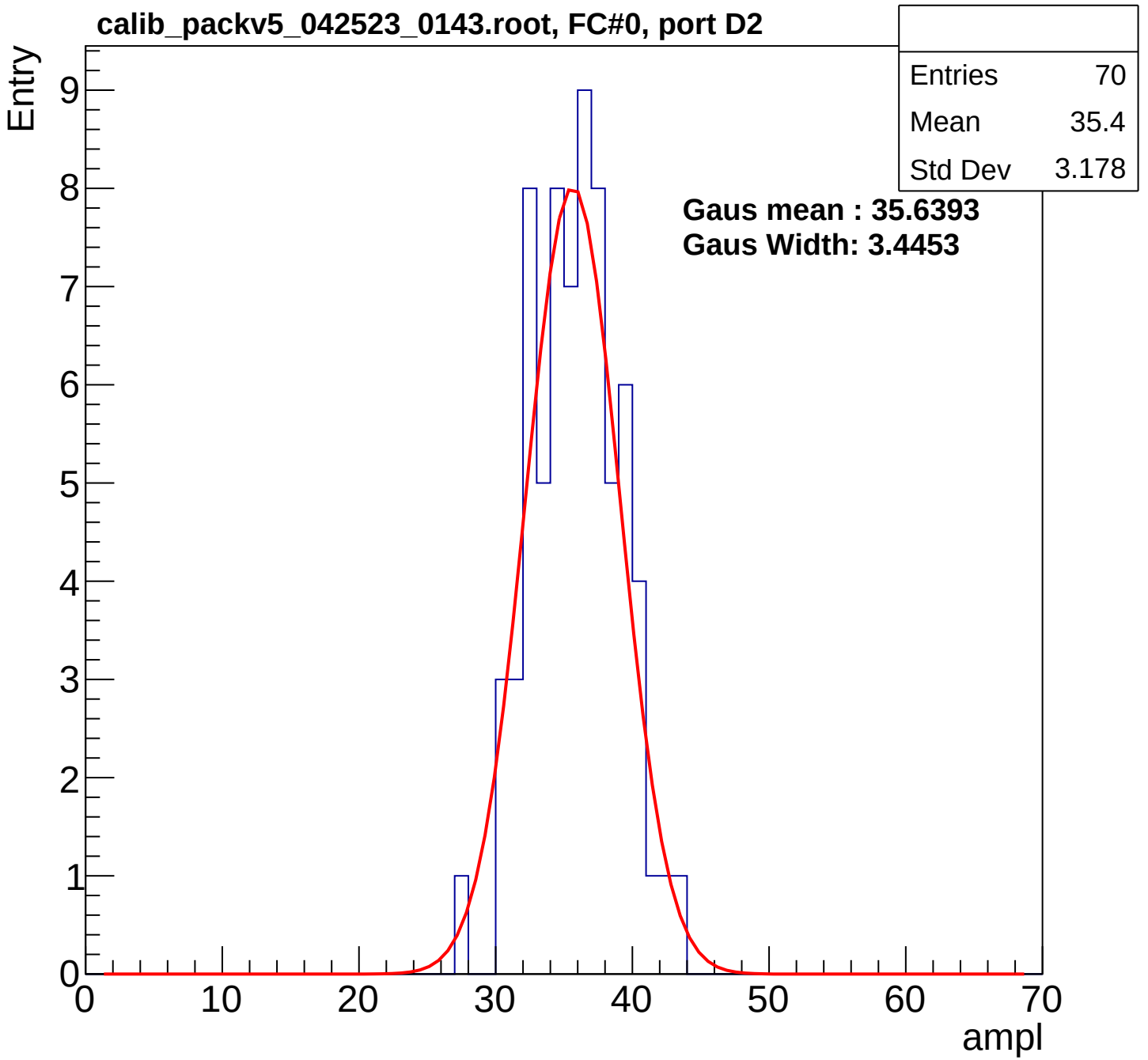
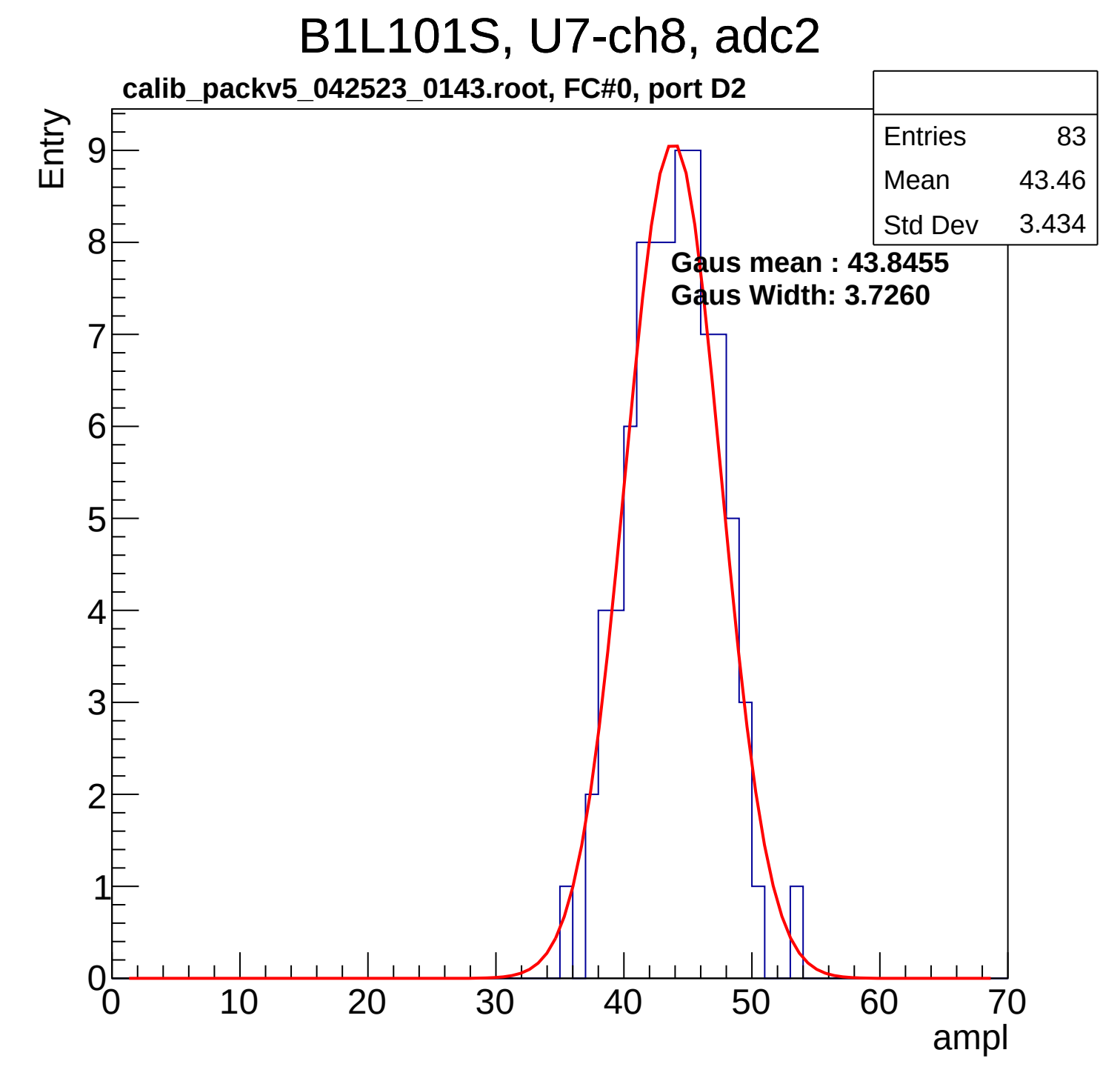
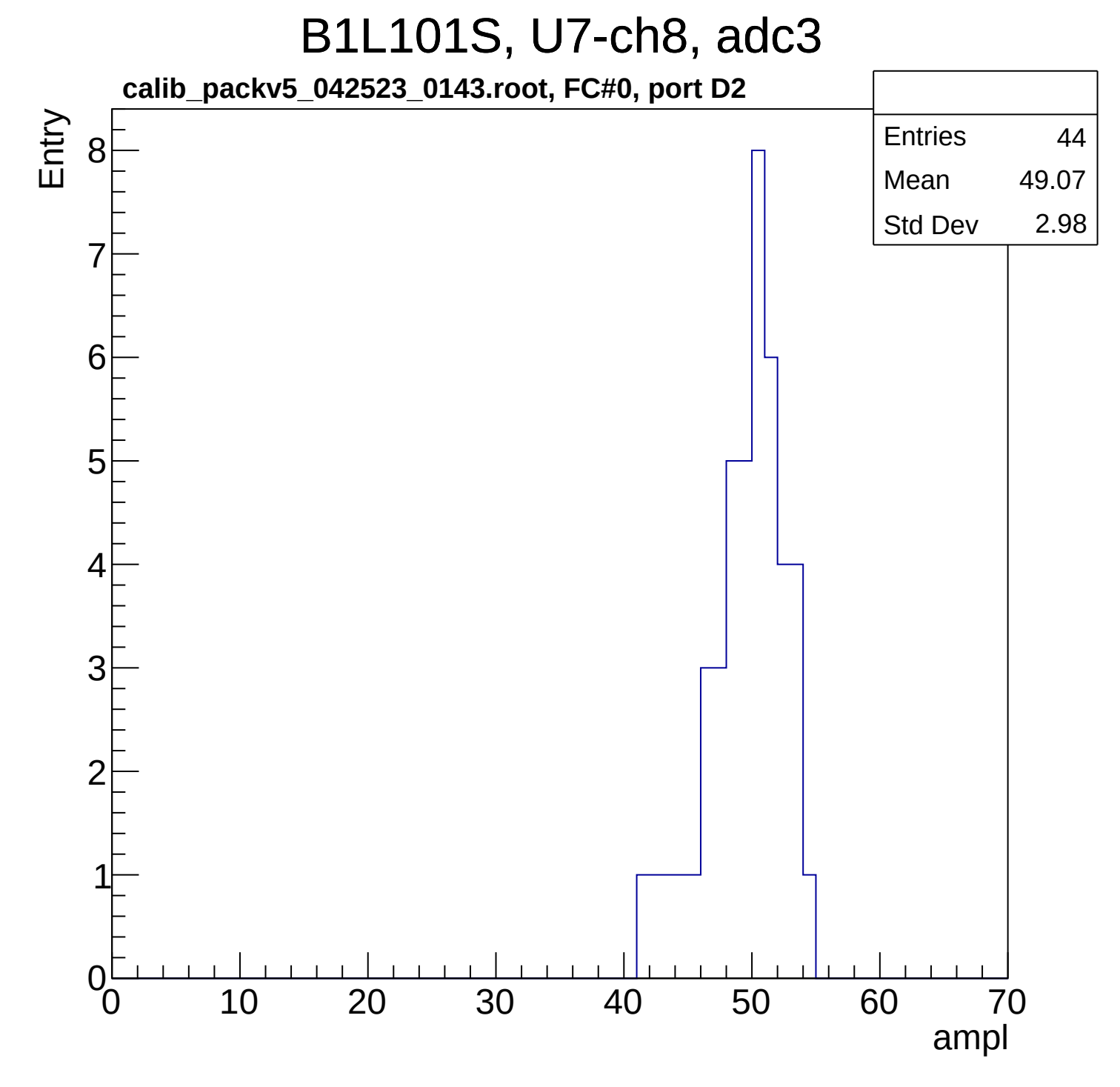

B1L101S, U7-ch7, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch8, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 27.76
Std Dev 5.777
Gaus mean : 28.2138
Gaus Width: 2.8825
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch8, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 35.4
Std Dev 3.178
Gaus mean : 35.6393
Gaus Width: 3.4453
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch8, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 83
Mean 43.46
Std Dev 3.434
Gaus mean : 43.8455
Gaus Width: 3.7260
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L101S, U7-ch8, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 44
Mean 49.07
Std Dev 2.98
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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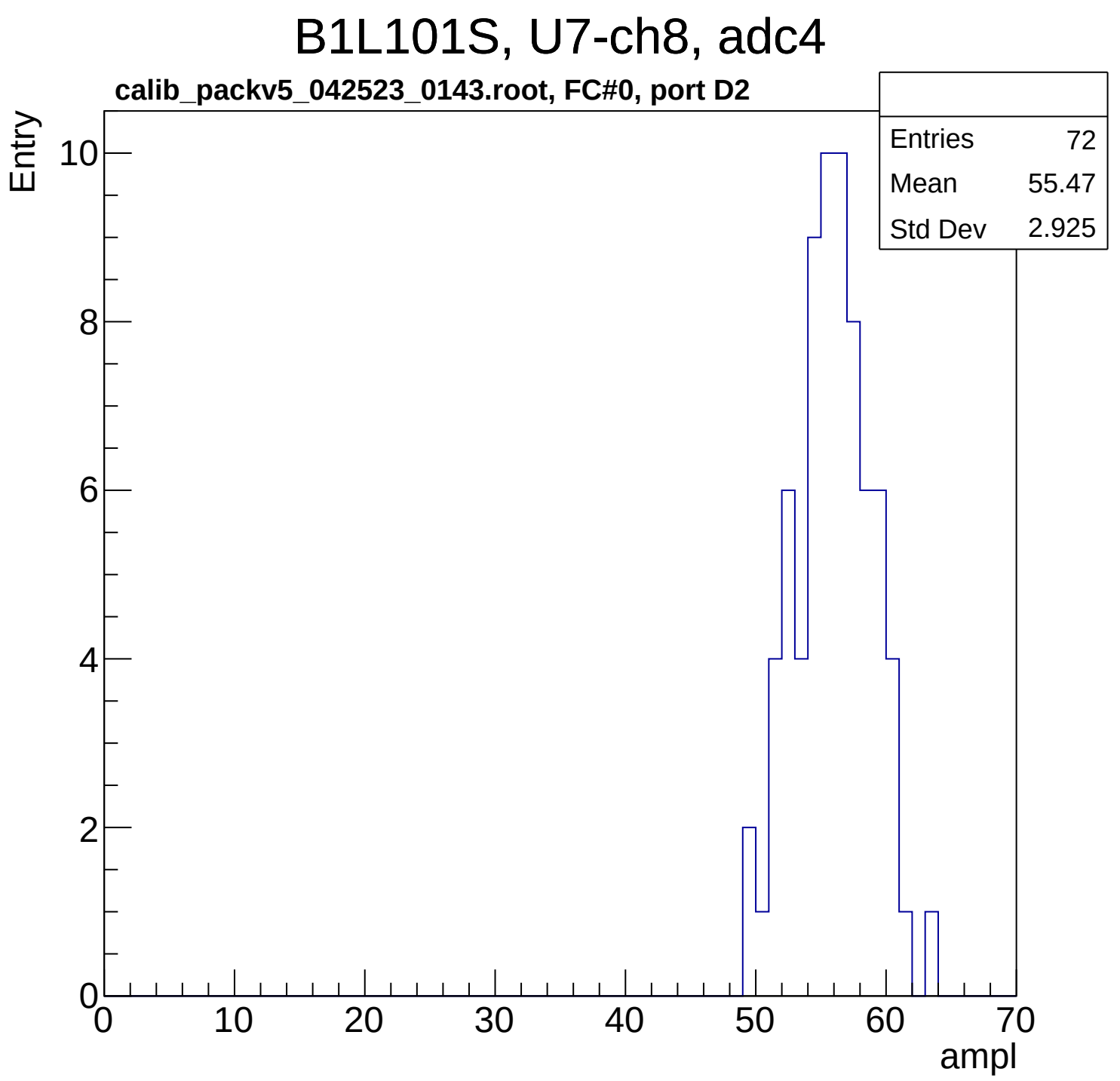
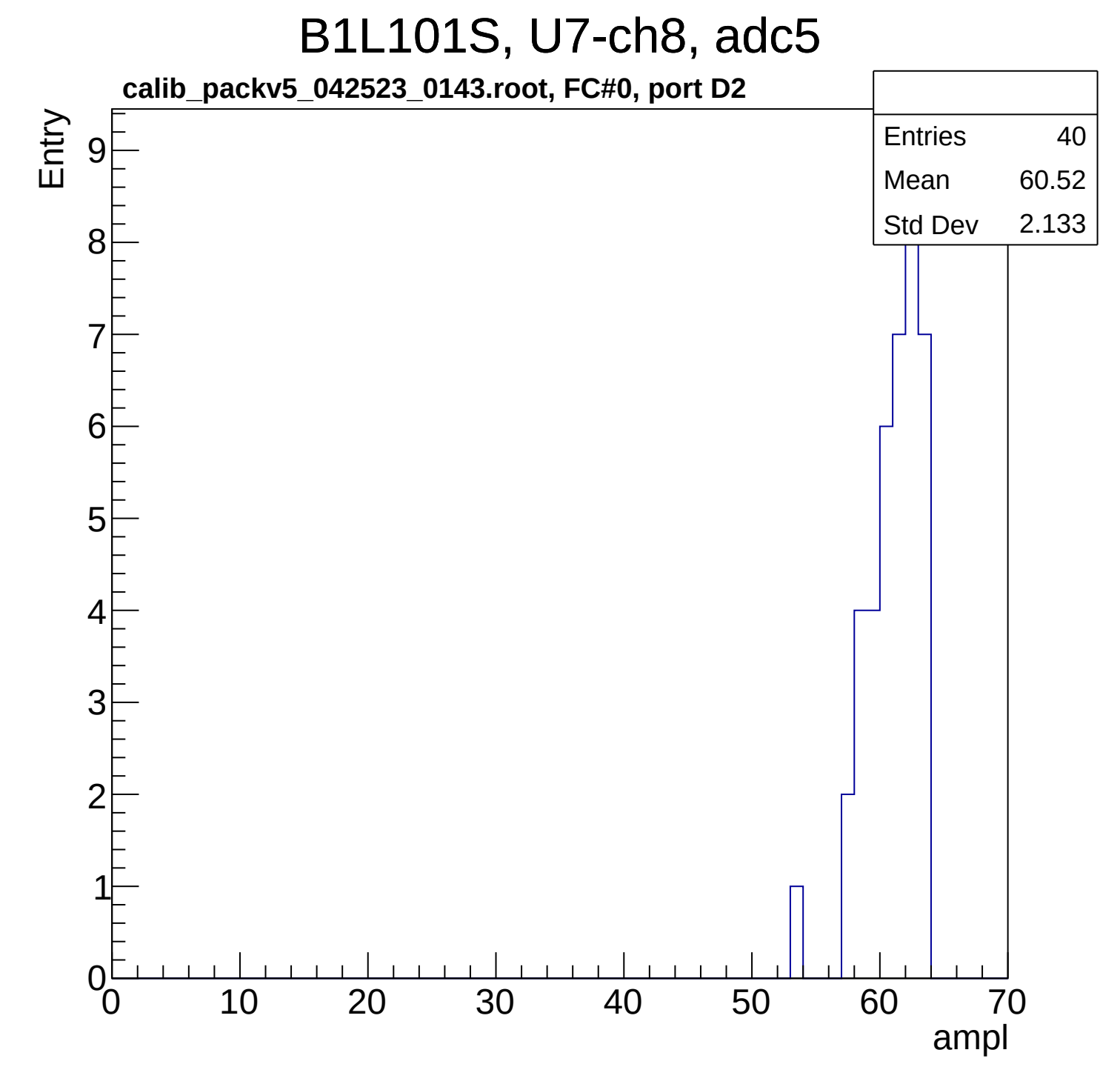

B1L101S, U7-ch8, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 55.47
Std Dev 2.925
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch8, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 40
Mean 60.52
Std Dev 2.133
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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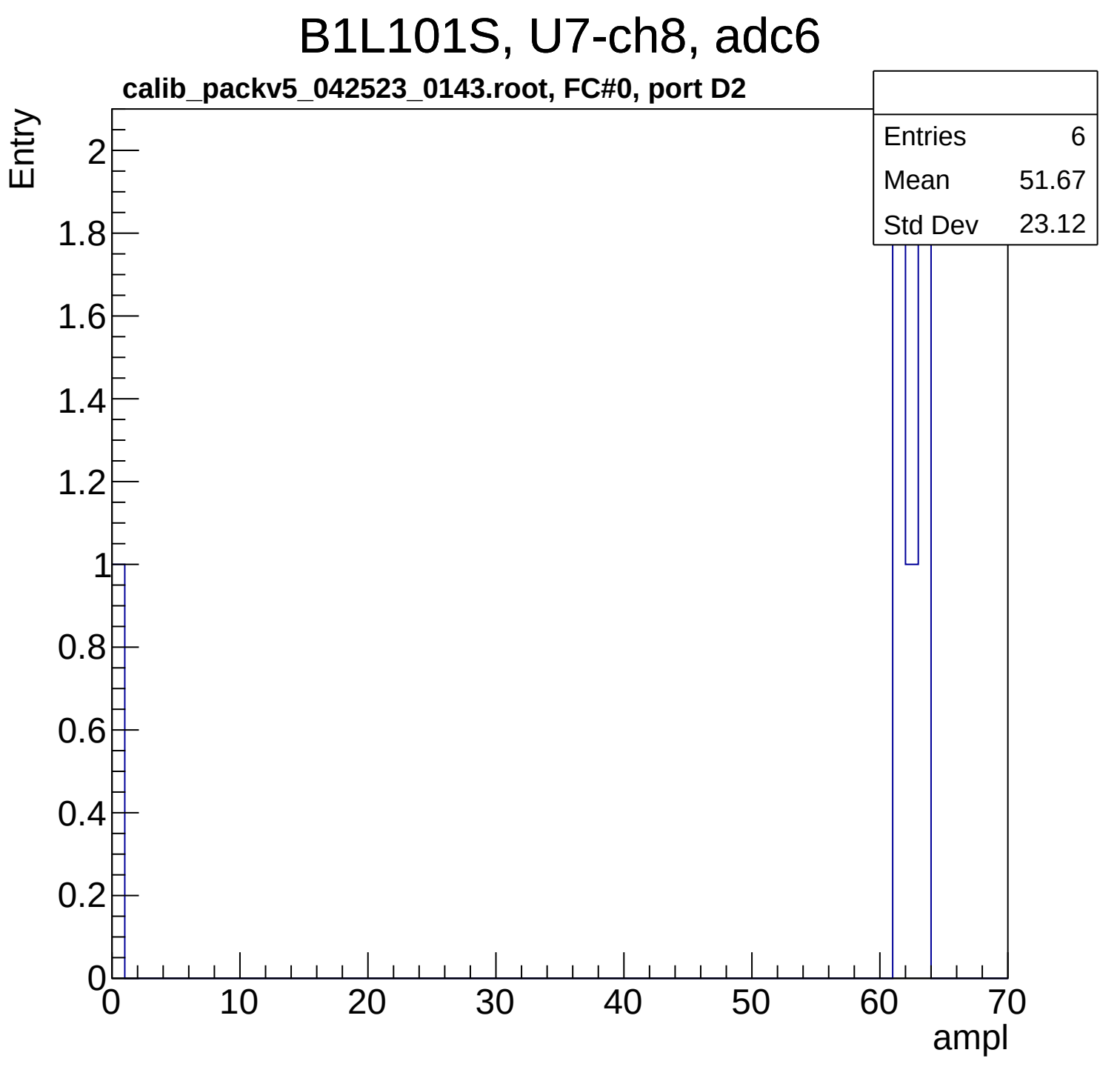
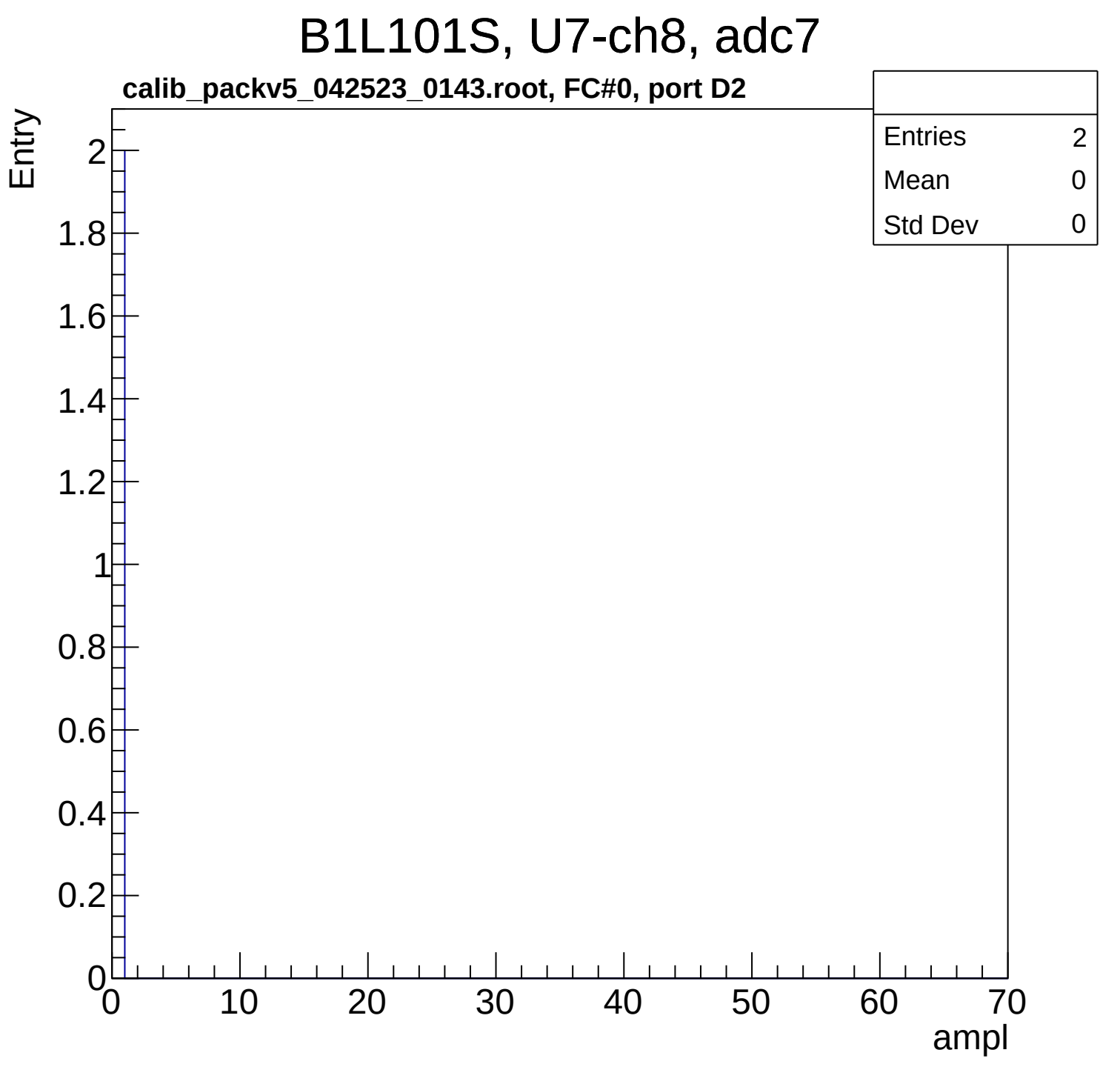
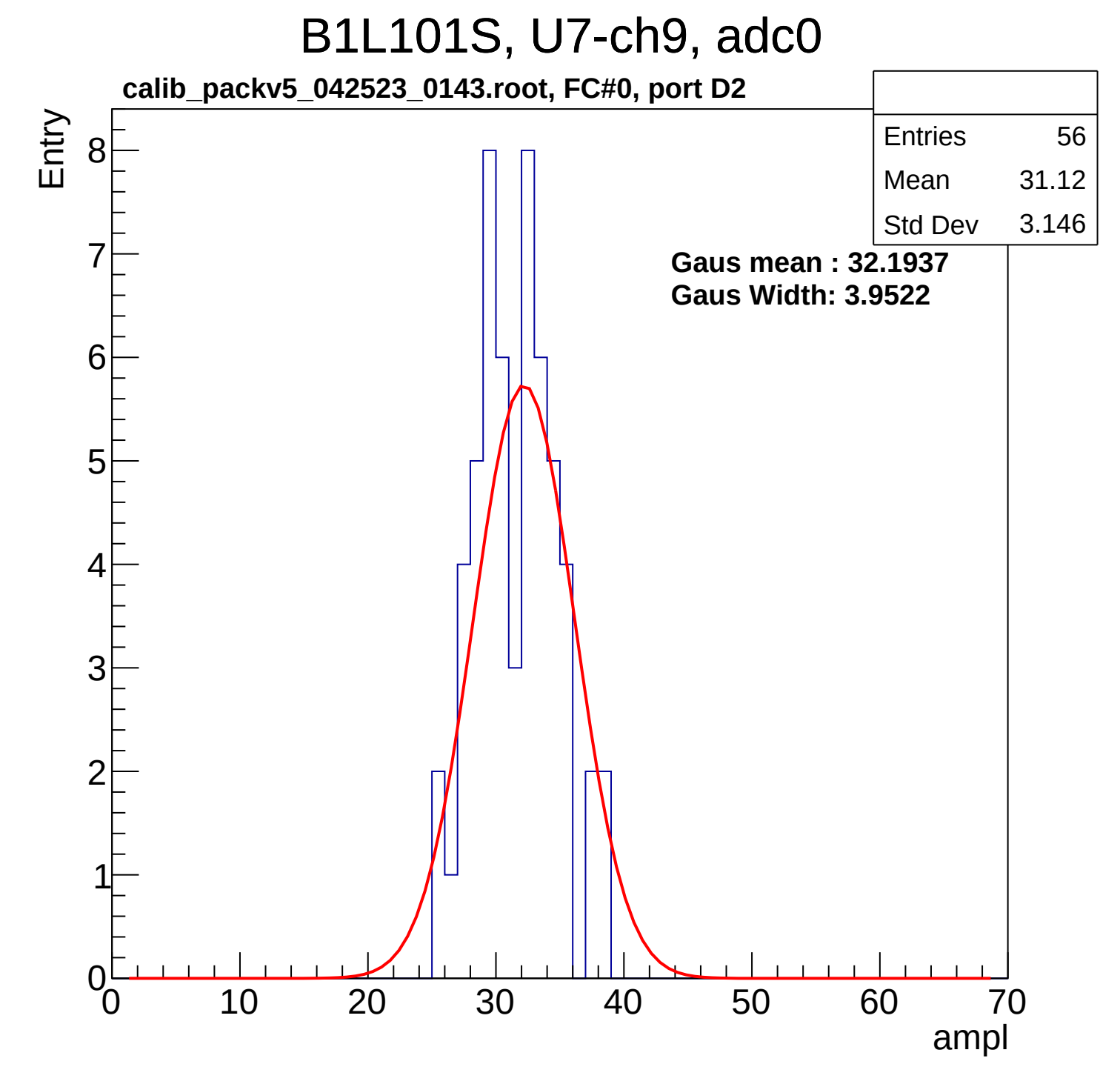

B1L101S, U7-ch8, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 51.67
Std Dev 23.12
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U7-ch8, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch9, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 31.12
Std Dev 3.146
Gaus mean : 32.1937
Gaus Width: 3.9522
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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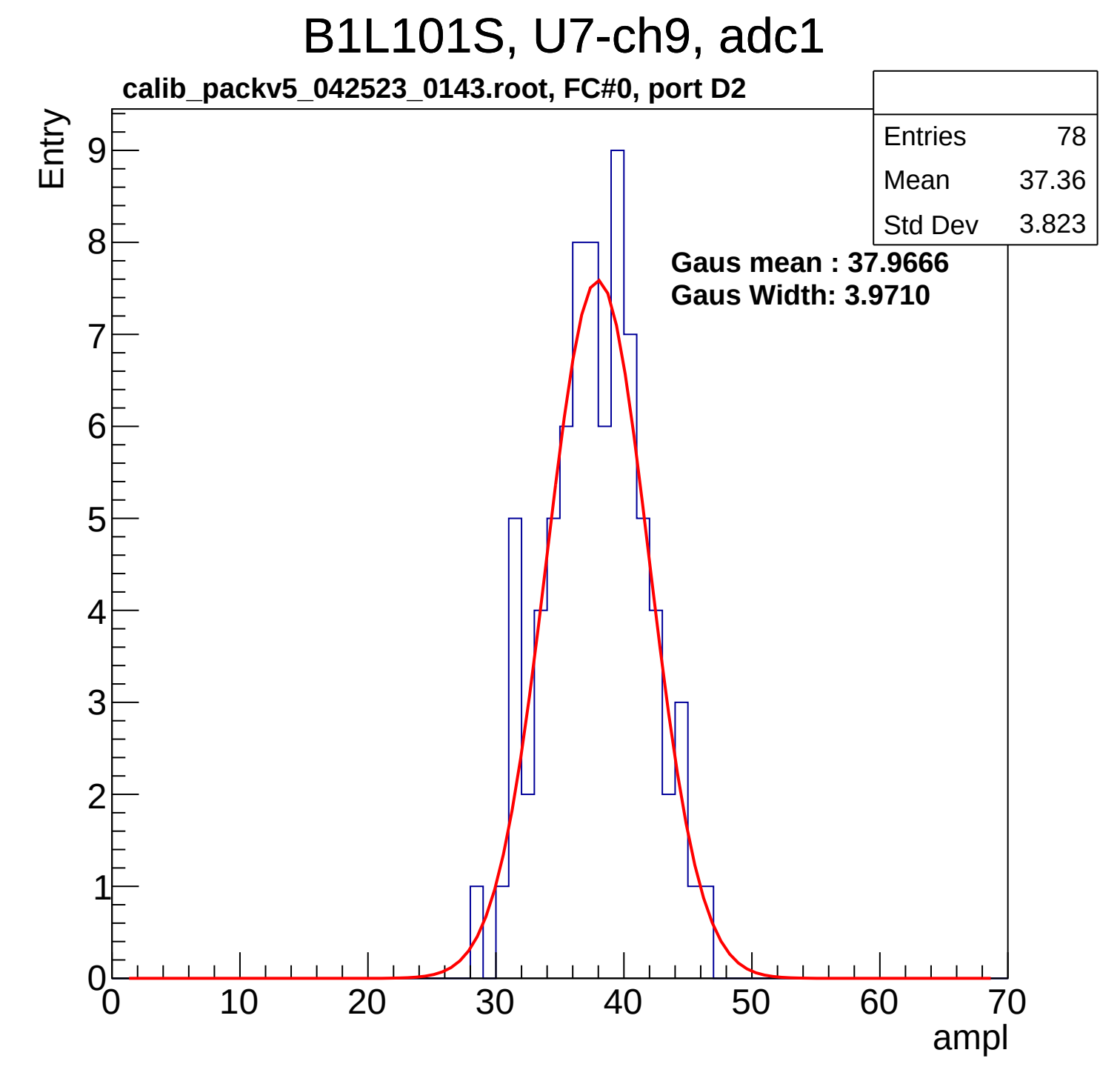
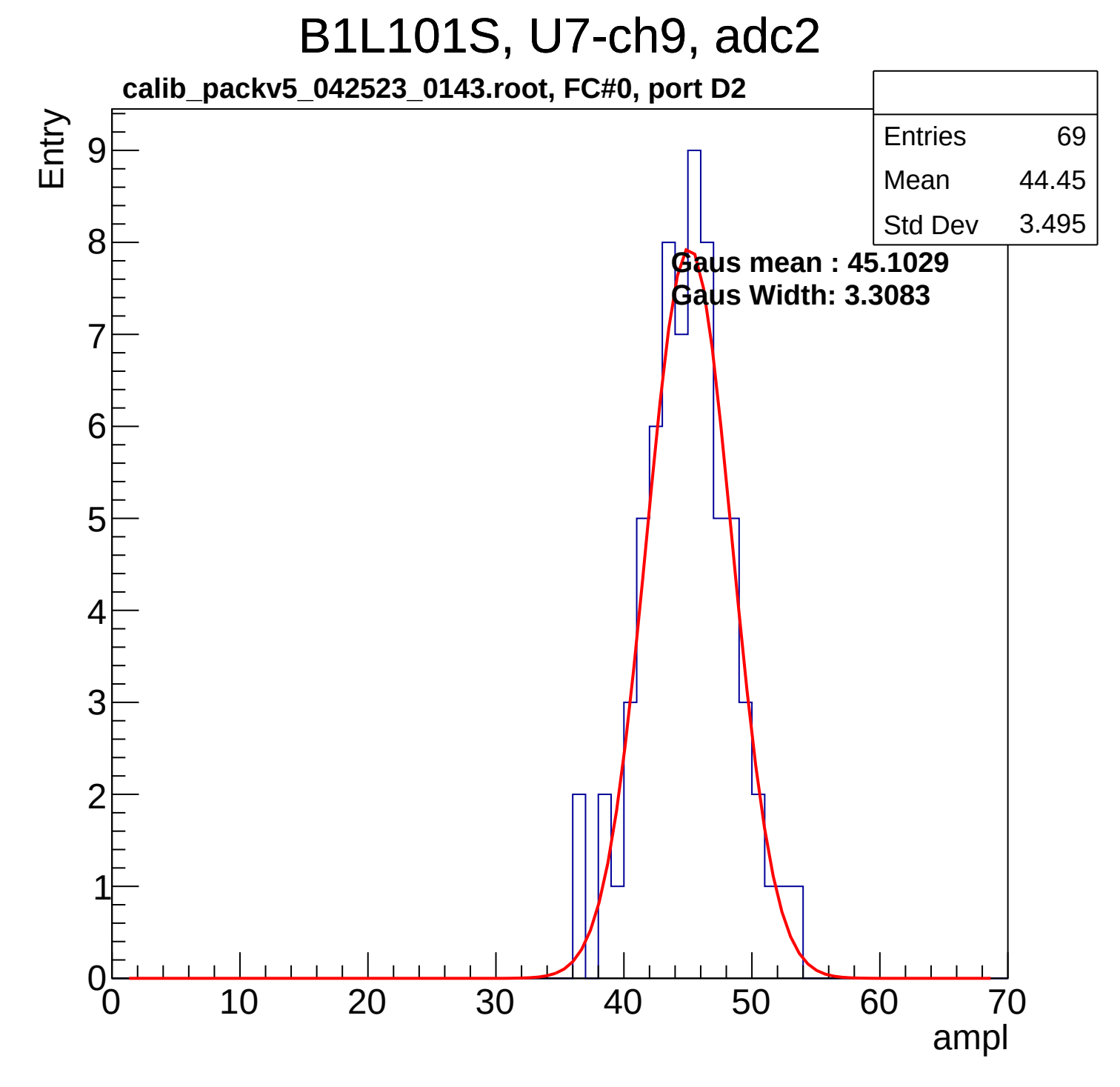

B1L101S, U7-ch9, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 37.36
Std Dev 3.823
Gaus mean : 37.9666
Gaus Width: 3.9710
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch9, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 44.45
Std Dev 3.495
Gaus mean : 45.1029
Gaus Width: 3.3083
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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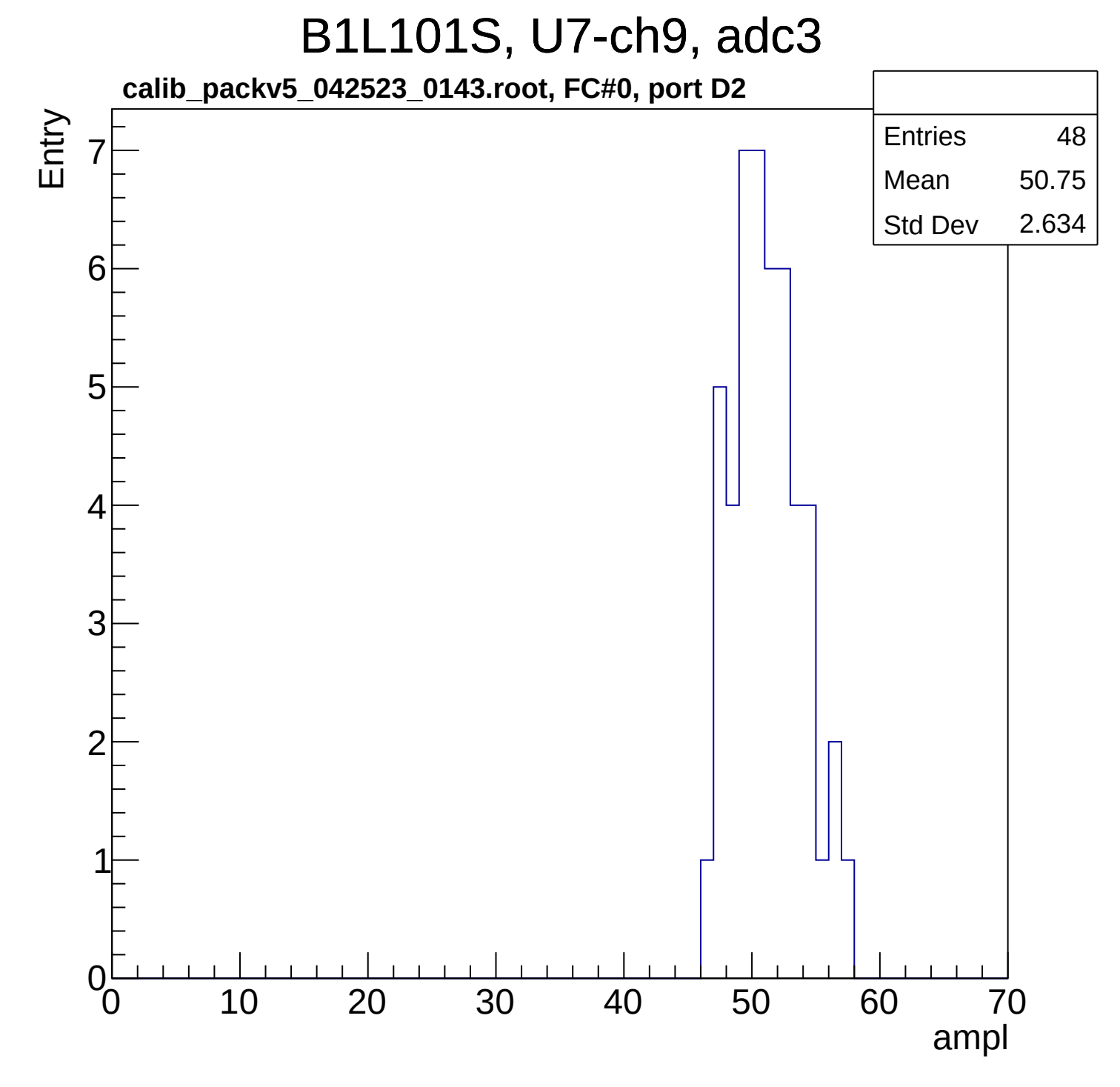
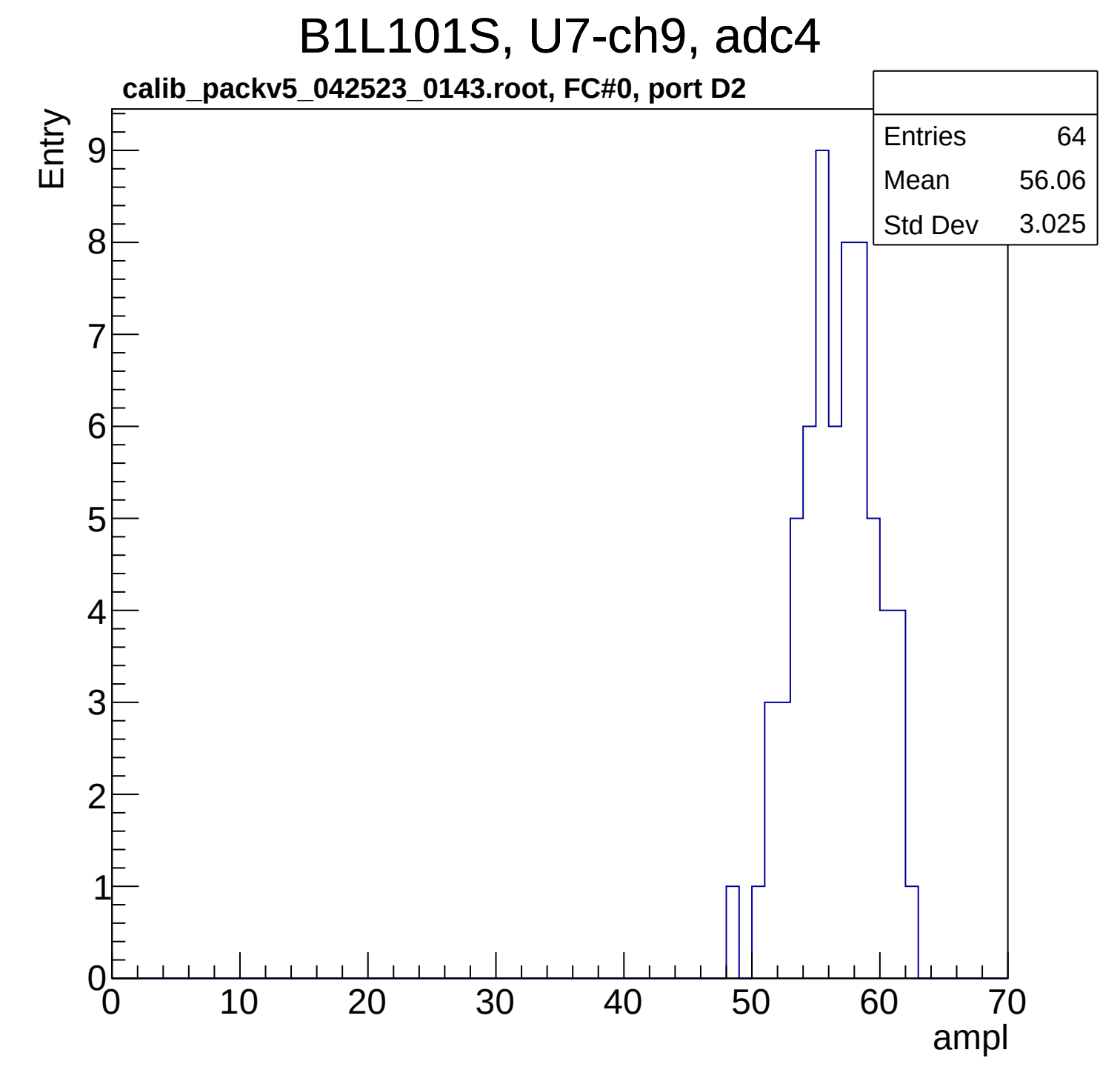

B1L101S, U7-ch9, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 50.75
Std Dev 2.634
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U7-ch9, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 56.06
Std Dev 3.025
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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60
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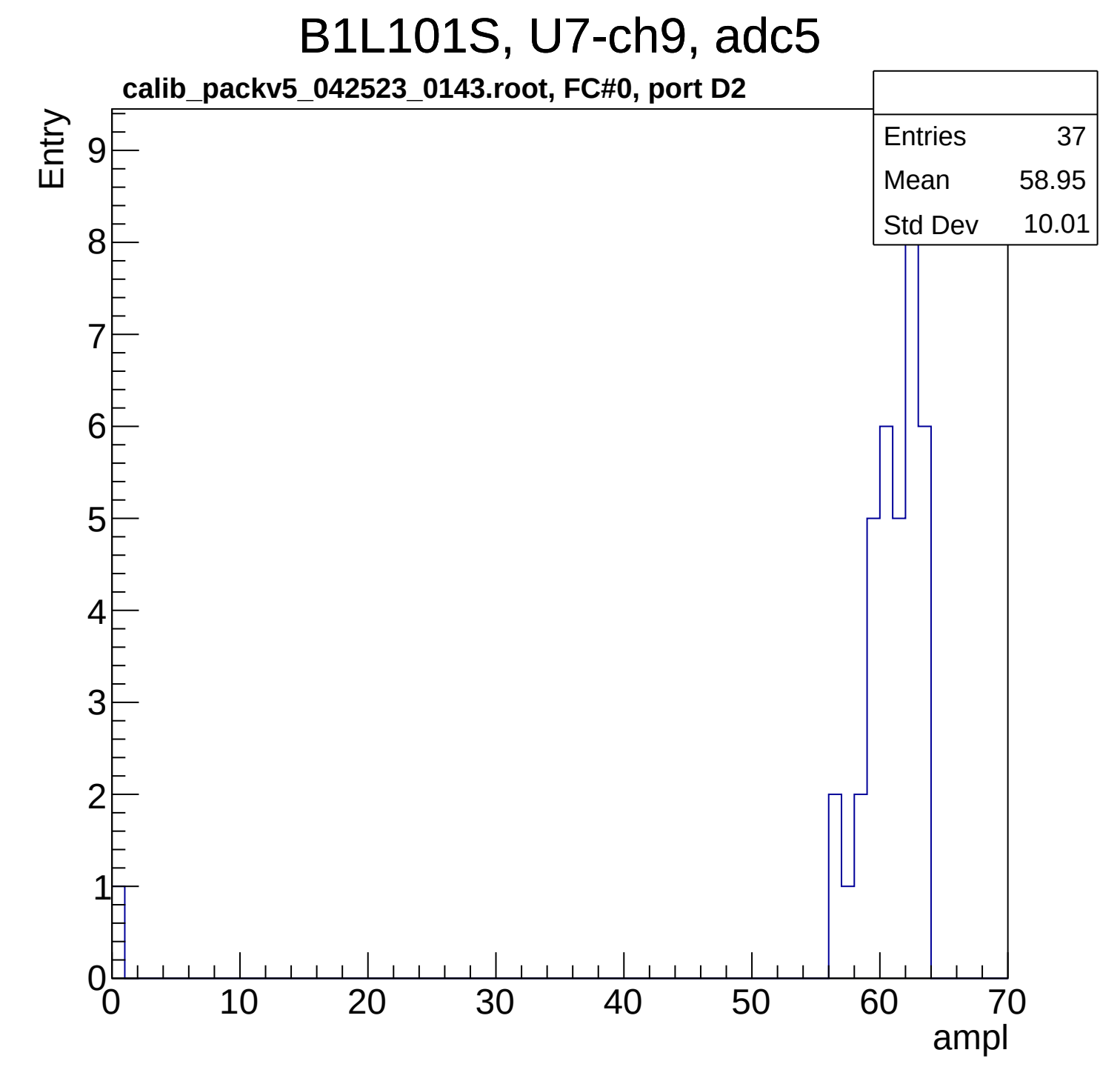
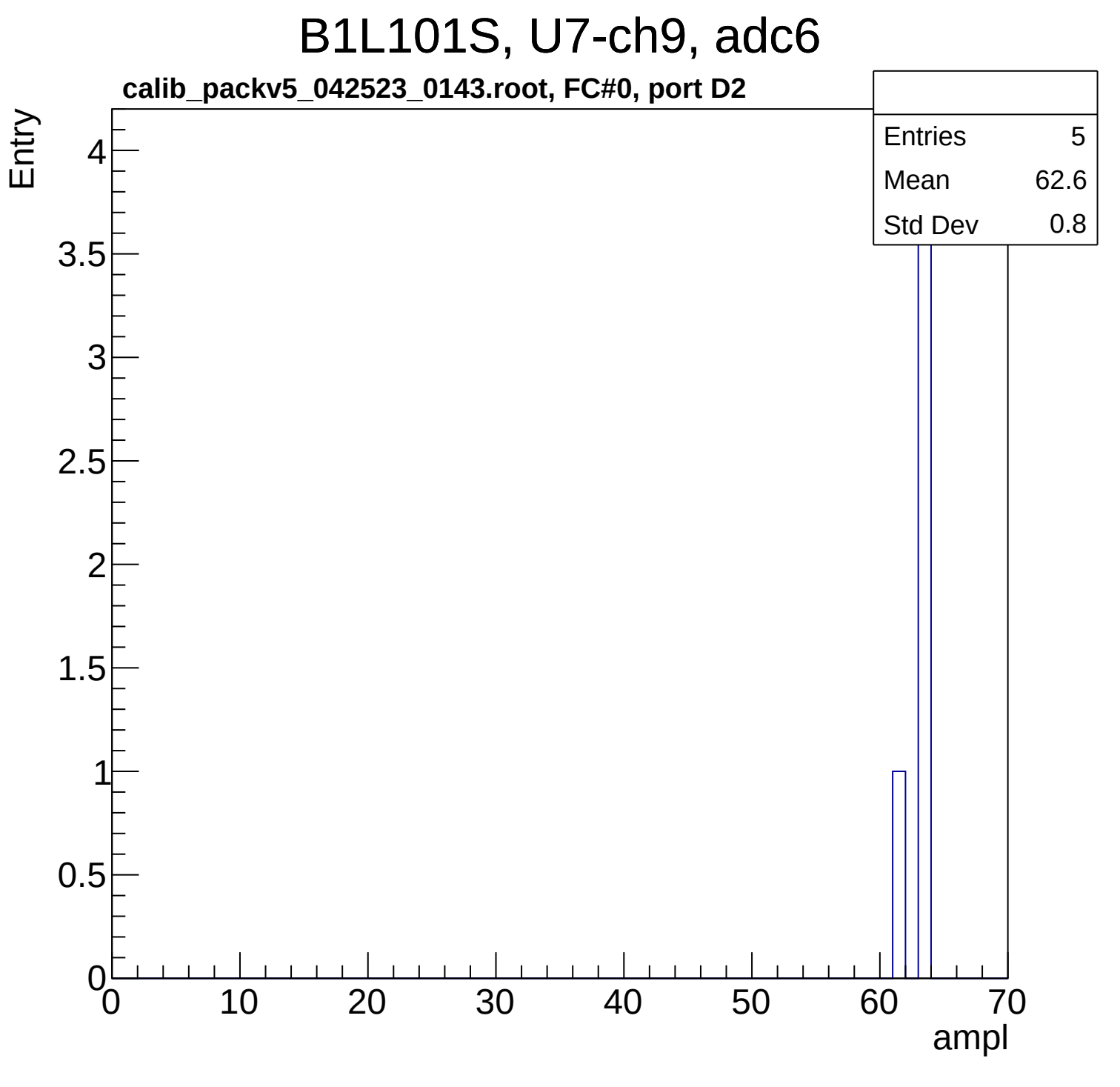
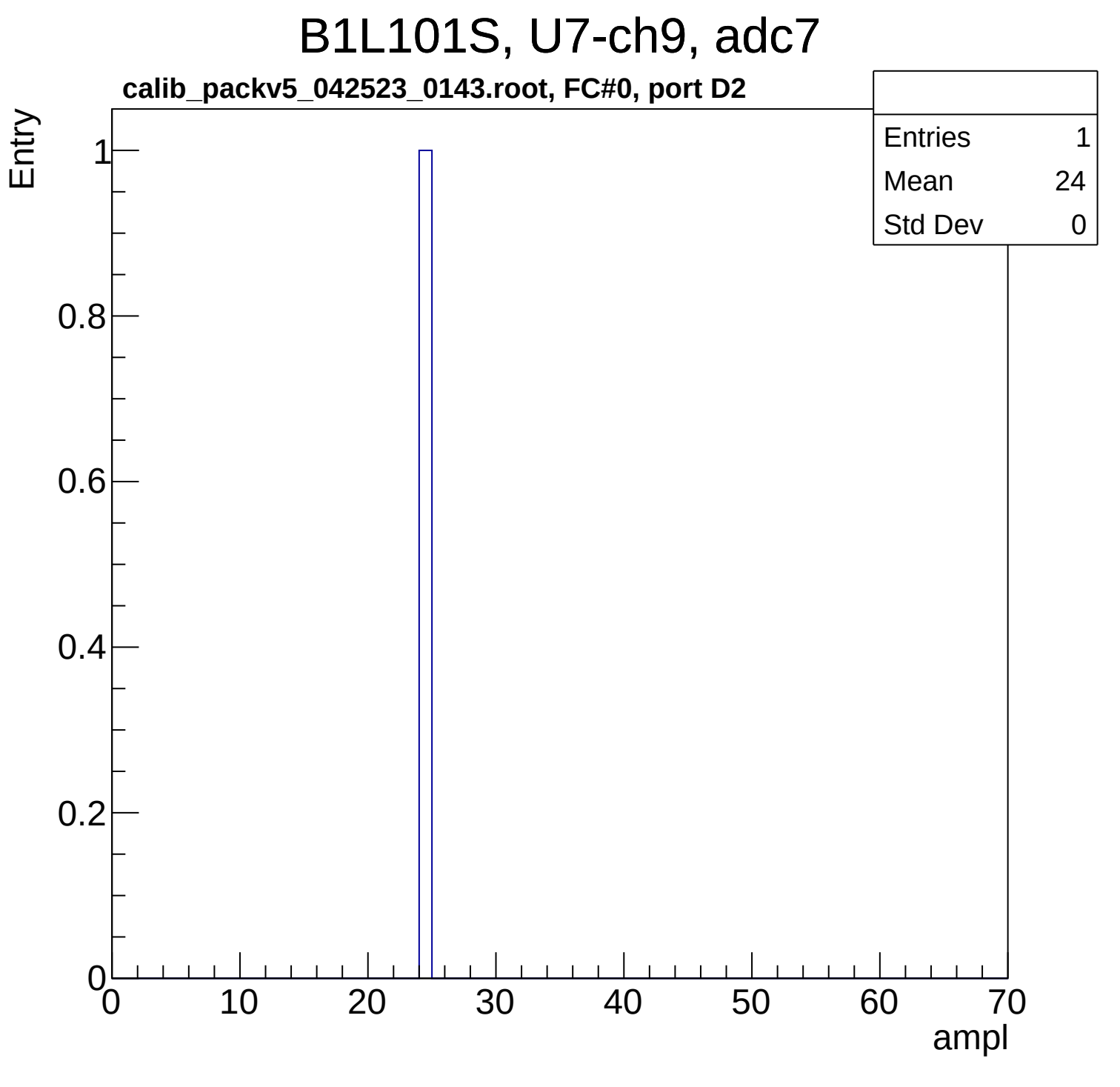
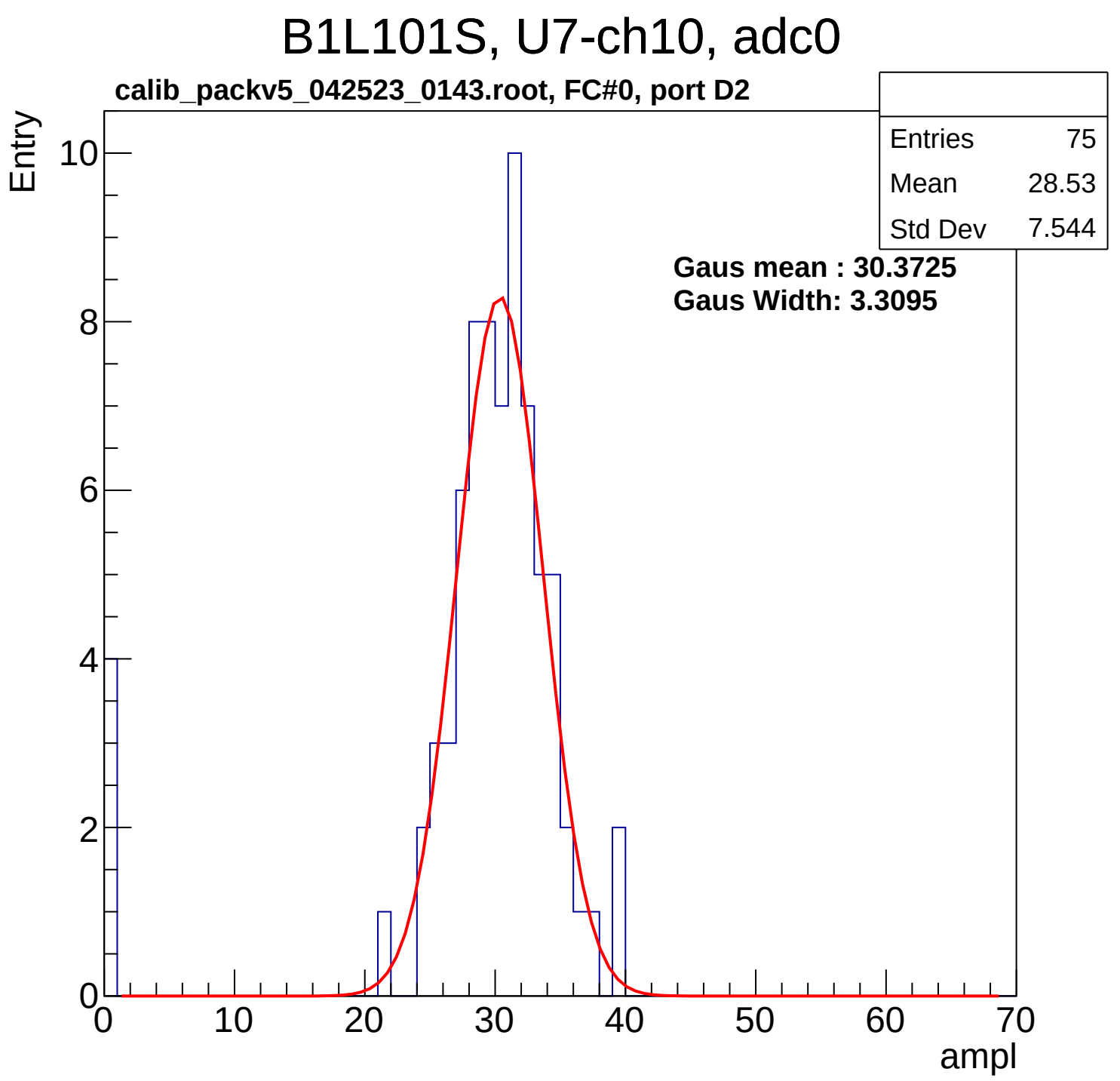
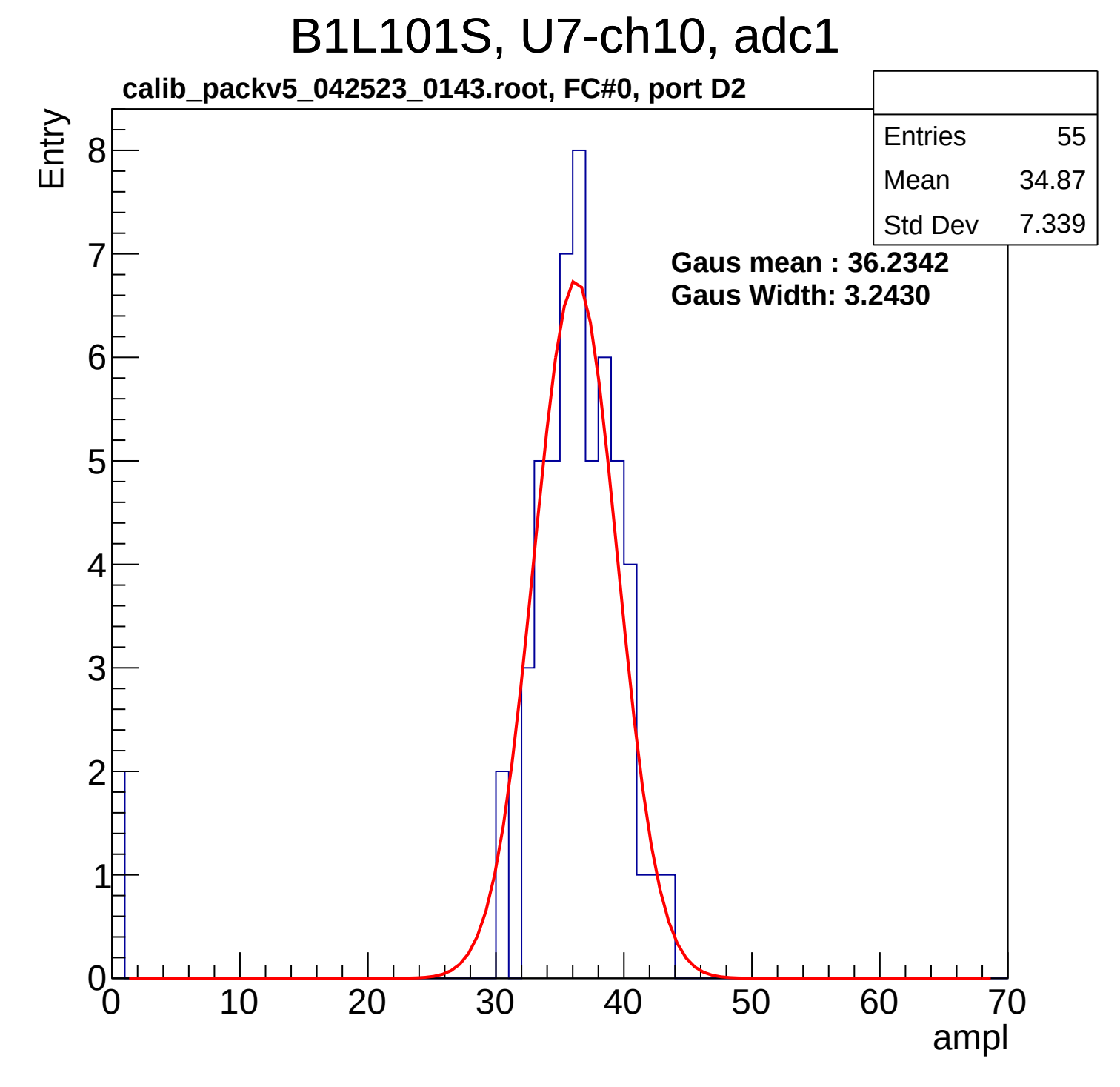

B1L101S, U7-ch9, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 37
Mean 58.95
Std Dev 10.01
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch9, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 62.6
Std Dev 0.8
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L101S, U7-ch9, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 24
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch10, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 28.53
Std Dev 7.544
Gaus mean : 30.3725
Gaus Width: 3.3095
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch10, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 34.87
Std Dev 7.339
Gaus mean : 36.2342
Gaus Width: 3.2430
Entry
ampl
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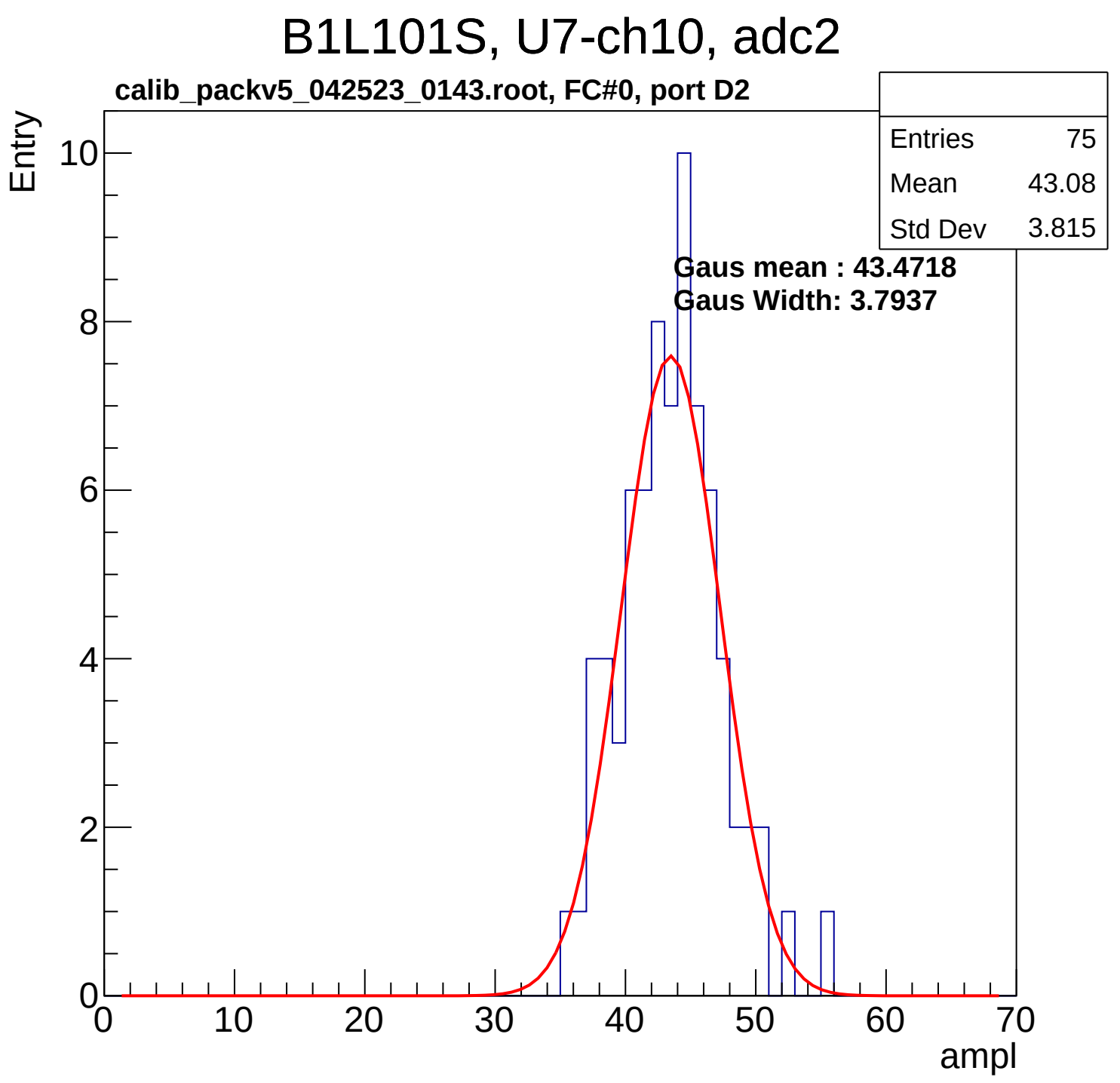
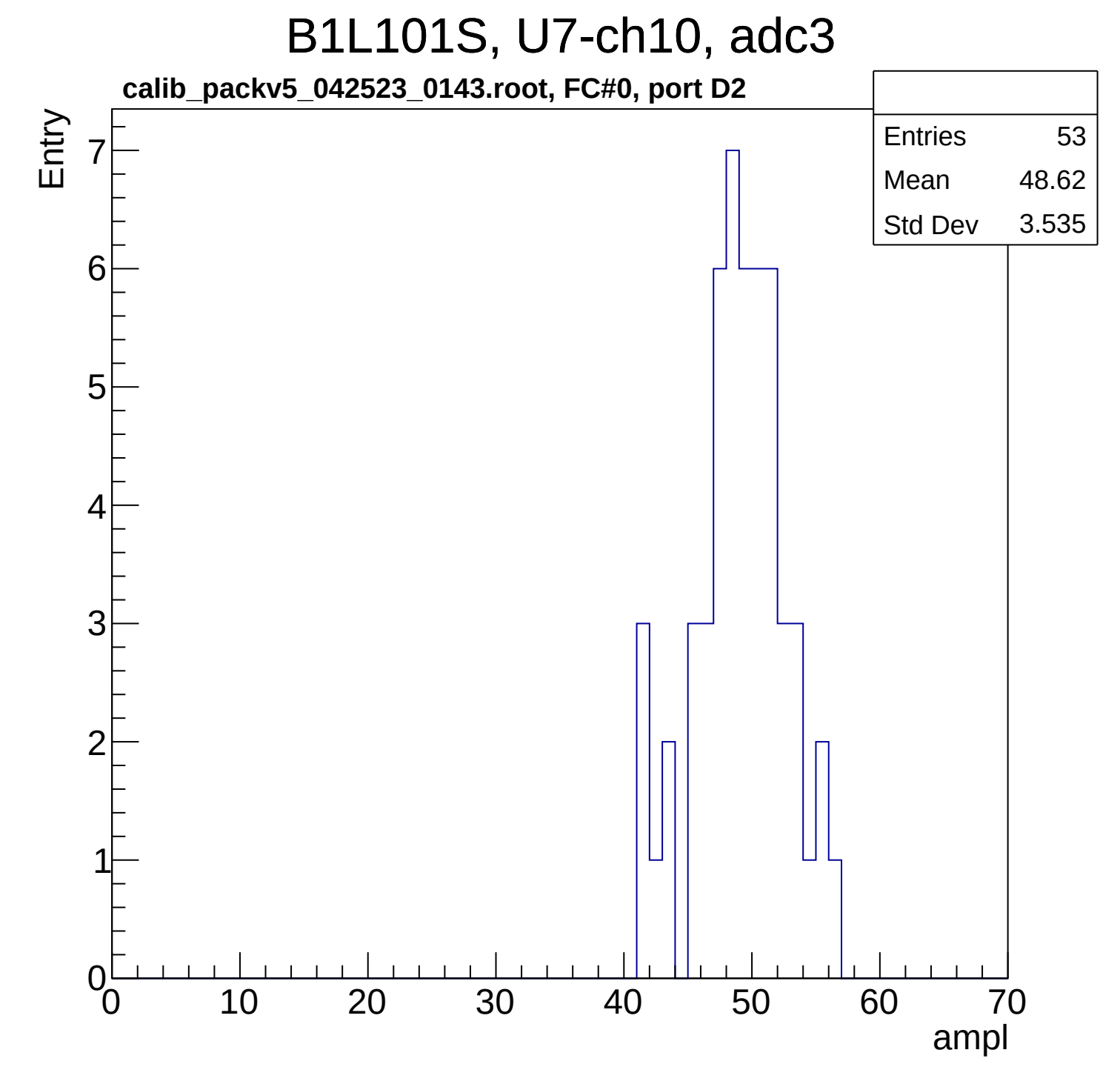
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch10, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 43.08
Std Dev 3.815
Gaus mean : 43.4718
Gaus Width: 3.7937
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch10, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 48.62
Std Dev 3.535
Entry
ampl
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1
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3
4
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6
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0
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50
60
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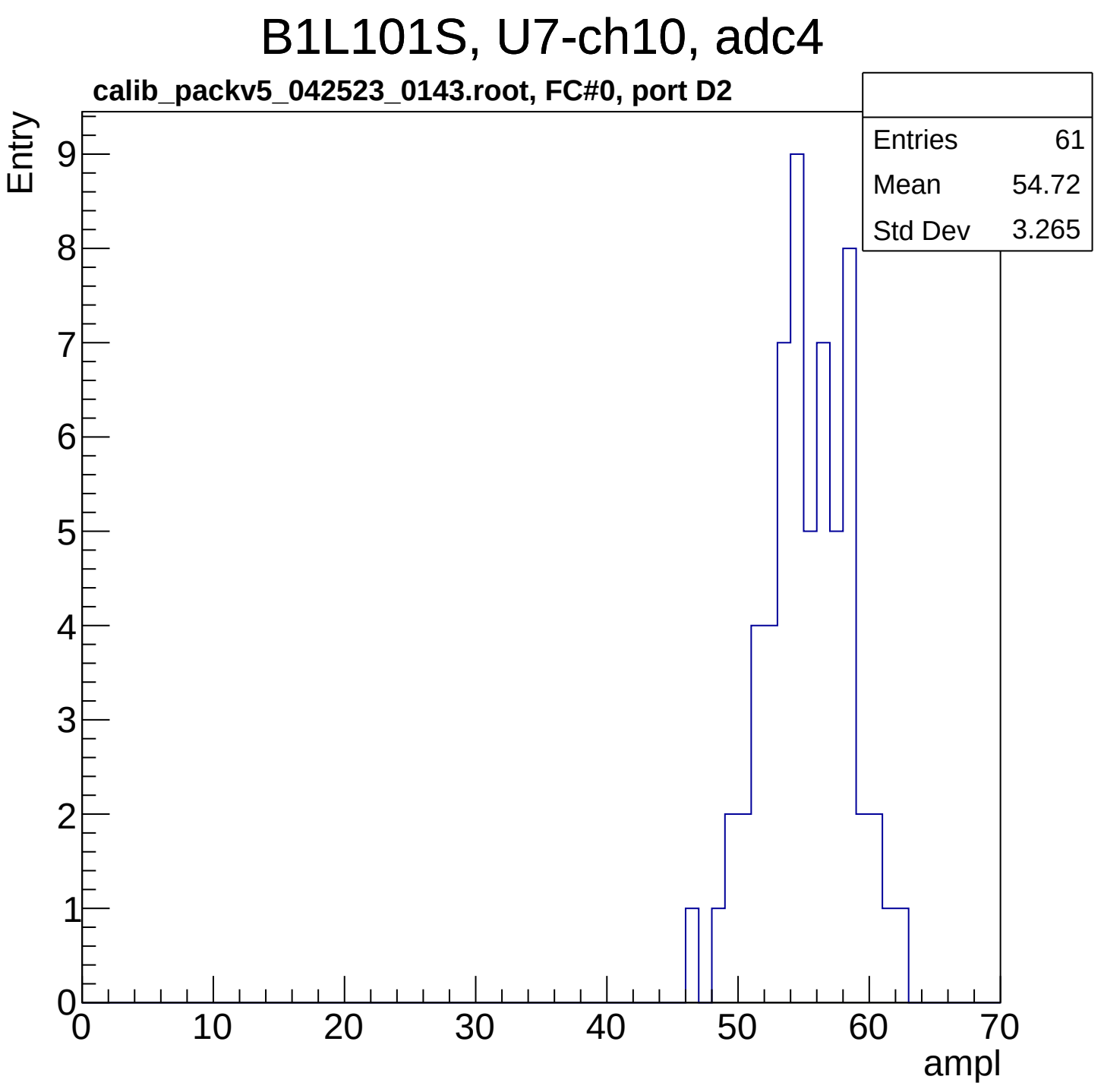
B1L101S, U7-ch10, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 54.72
Std Dev 3.265
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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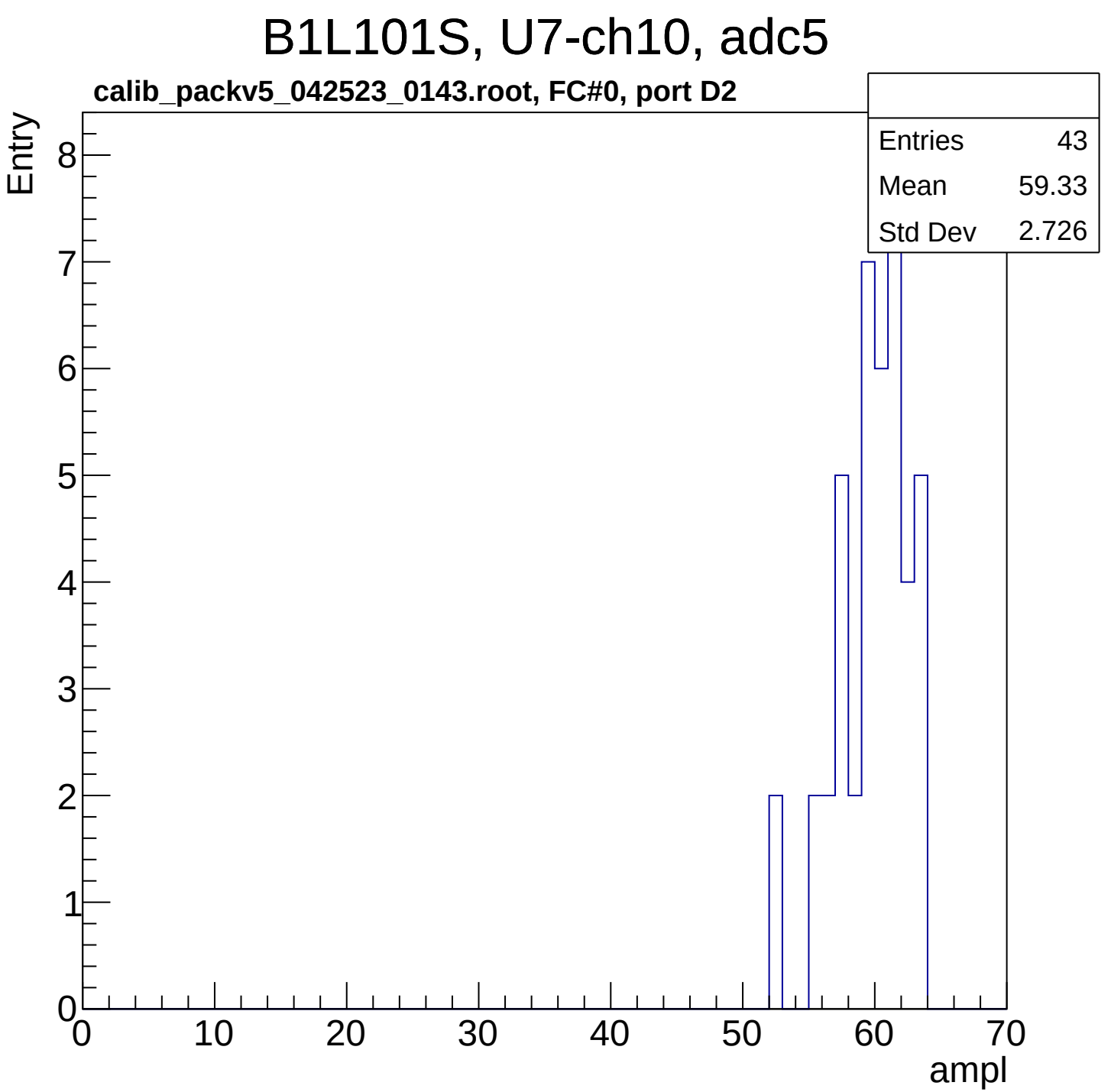
B1L101S, U7-ch10, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 43
Mean 59.33
Std Dev 2.726
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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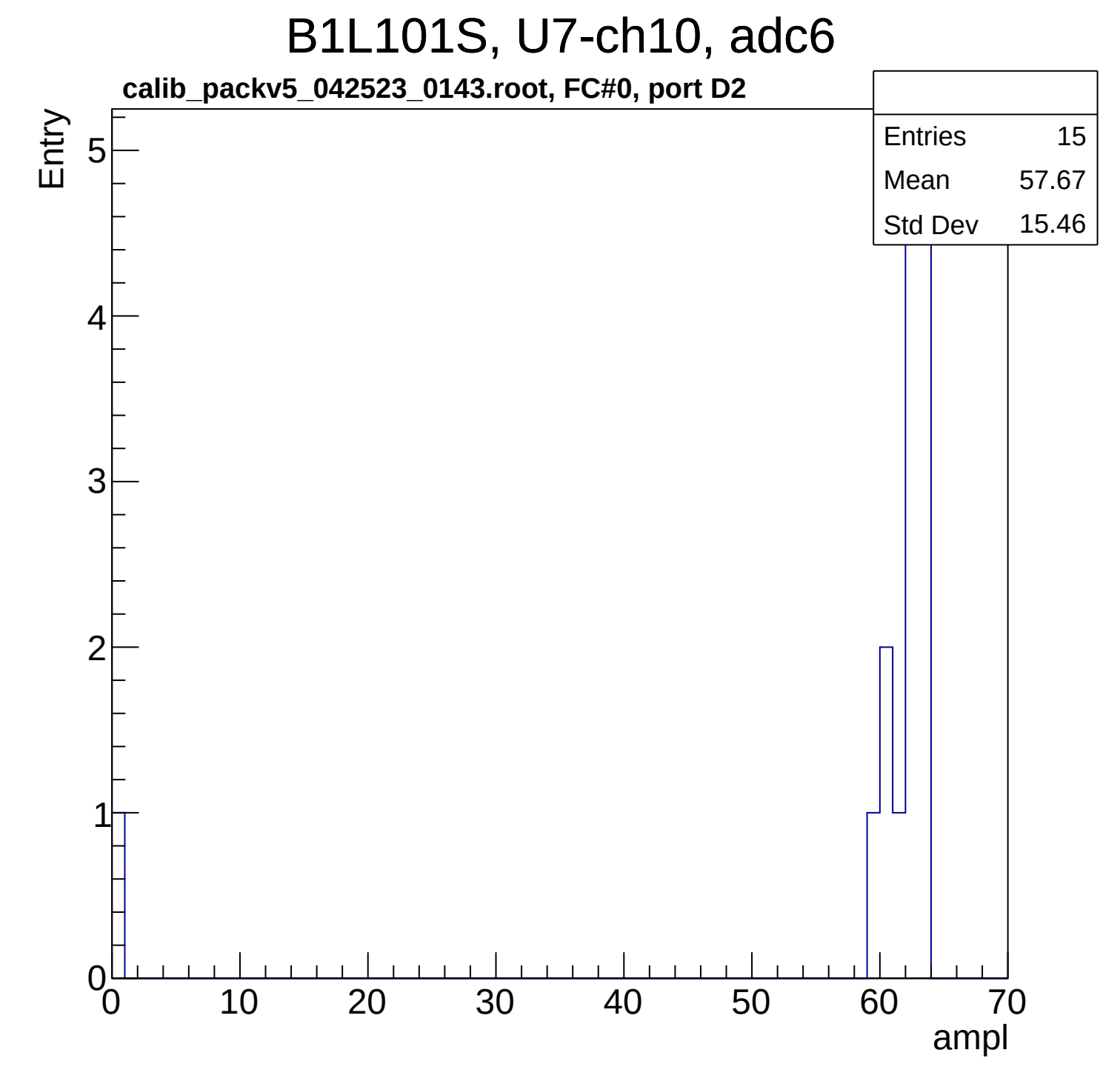
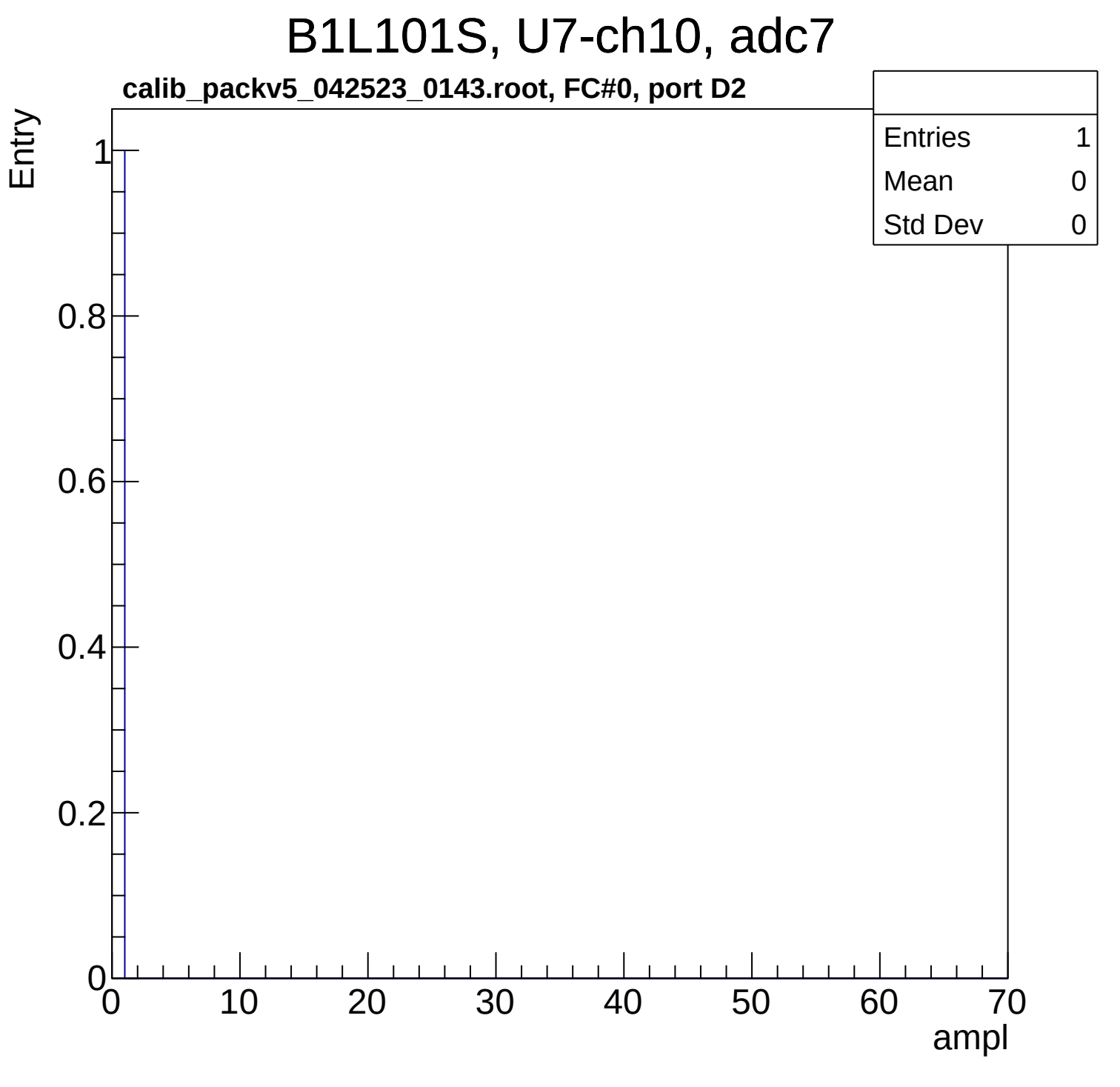

B1L101S, U7-ch10, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 15
Mean 57.67
Std Dev 15.46
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch10, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
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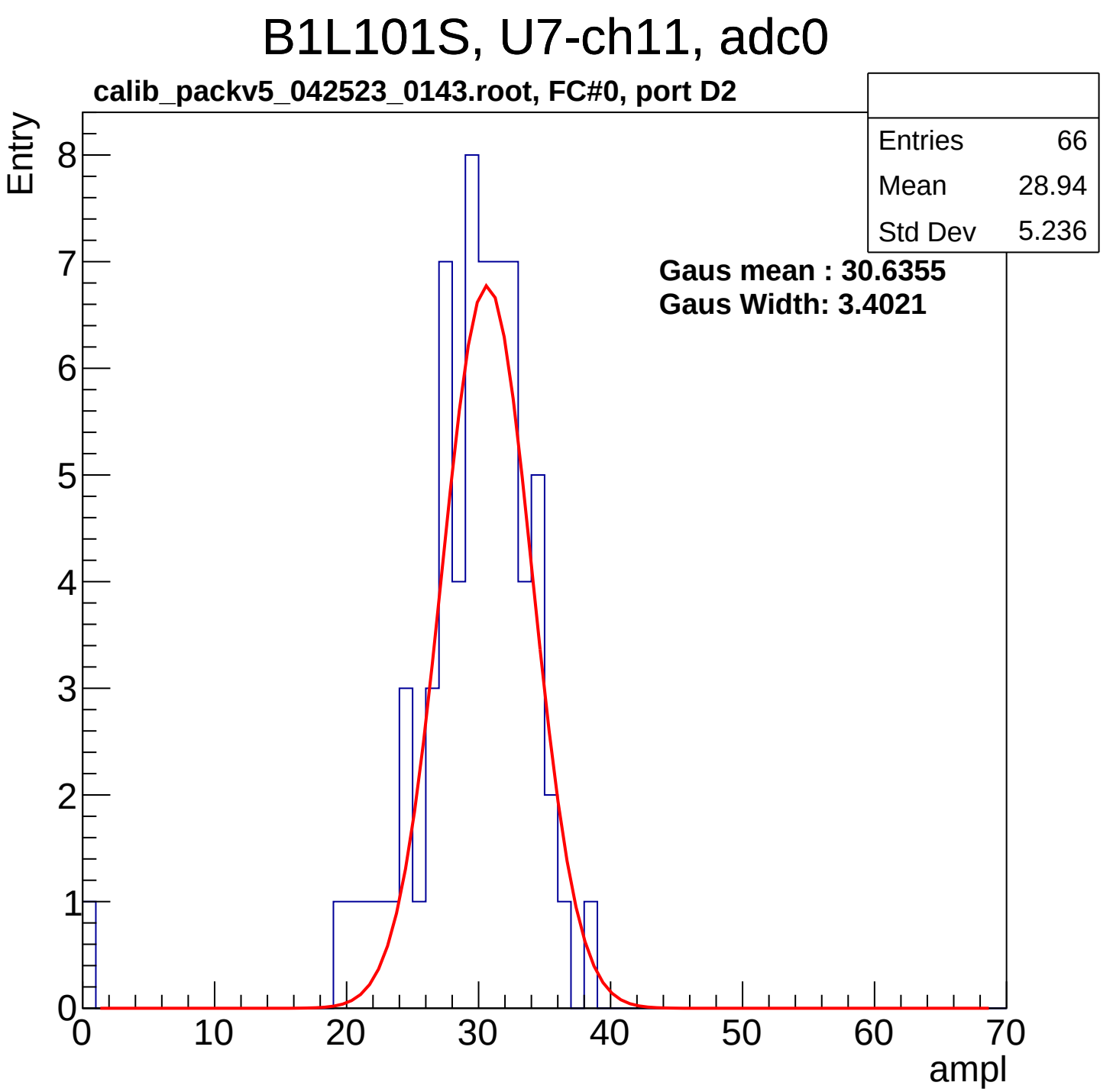
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch11, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 28.94
Std Dev 5.236
Gaus mean : 30.6355
Gaus Width: 3.4021
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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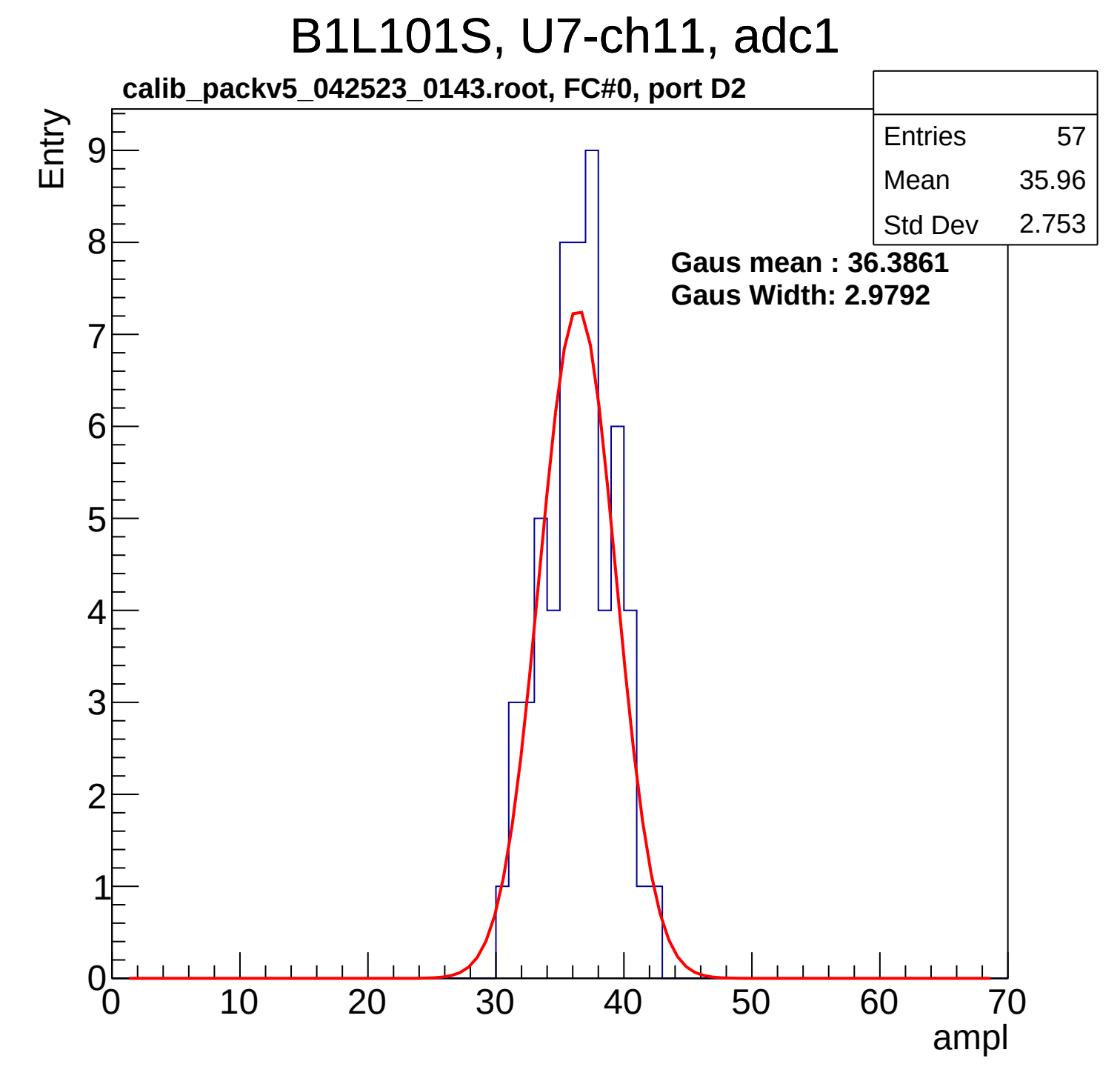
40
50
60
70


B1L101S, U7-ch11, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 35.96
Std Dev 2.753
Gaus mean : 36.3861
Gaus Width: 2.9792
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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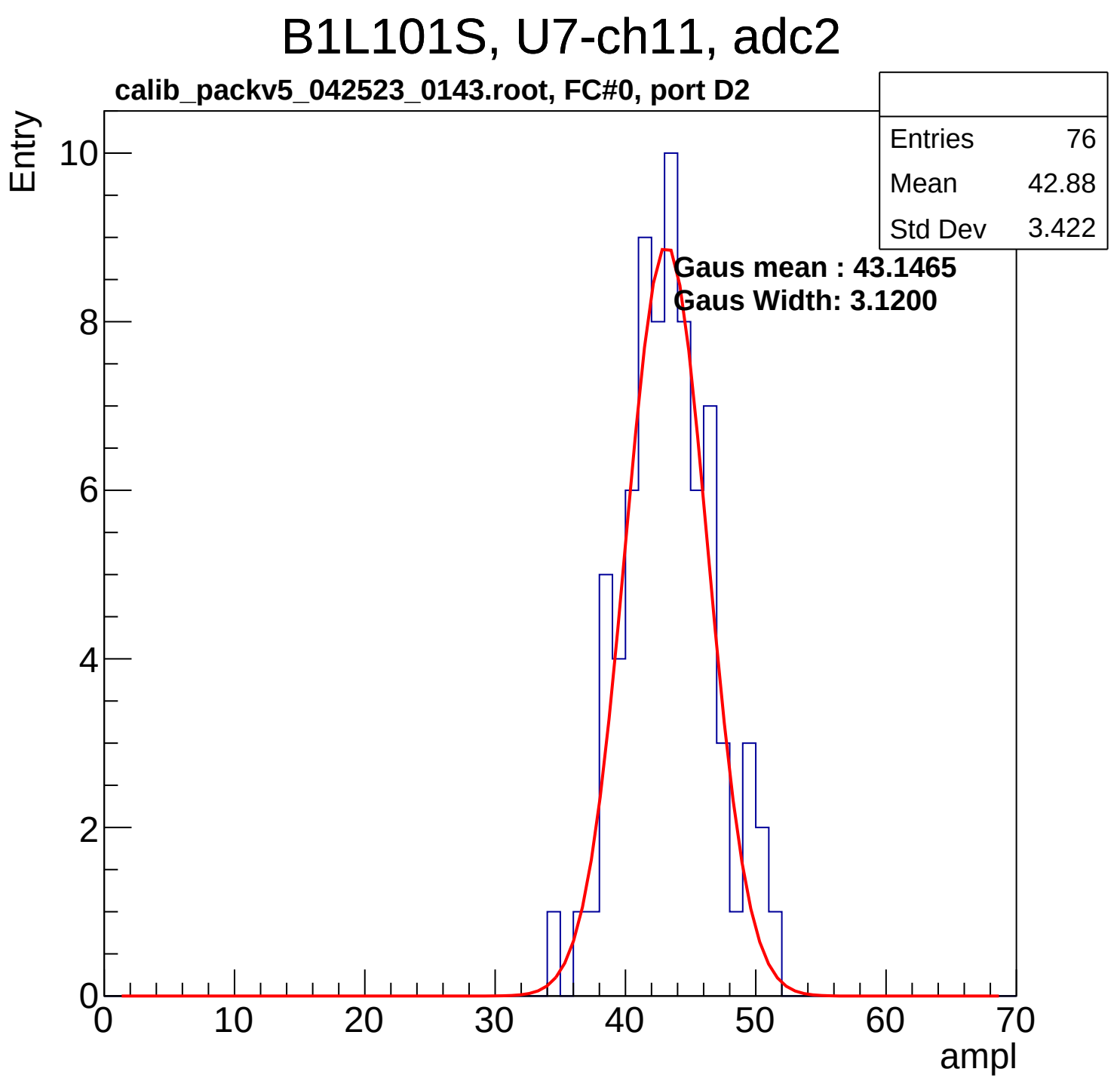
B1L101S, U7-ch11, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 42.88
Std Dev 3.422
Gaus mean : 43.1465
Gaus Width: 3.1200
Entry
ampl
0
2
4
6
8
10
0
10
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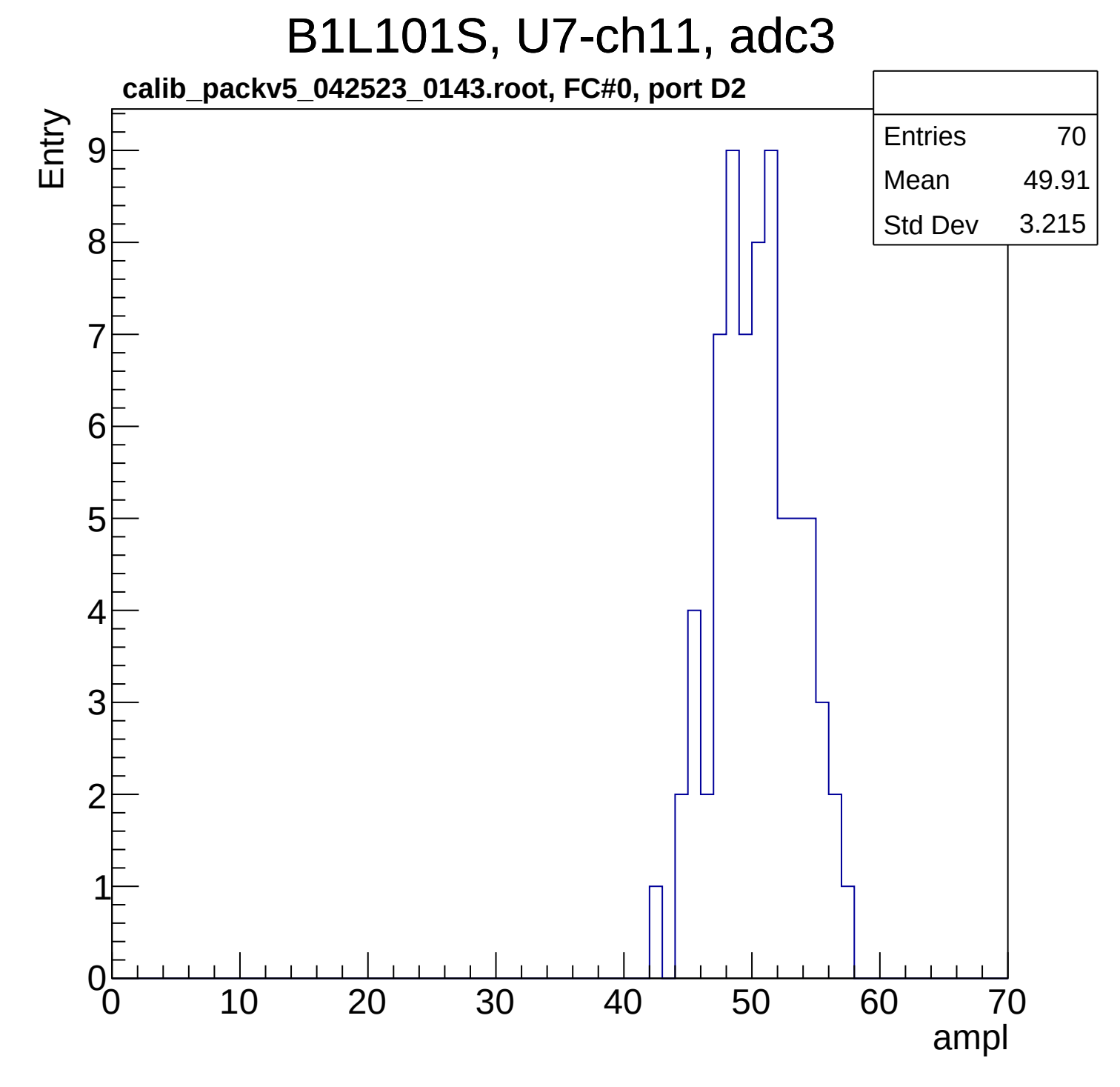
40
50
60
70


B1L101S, U7-ch11, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 49.91
Std Dev 3.215
Entry
ampl
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3
4
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6
7
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0
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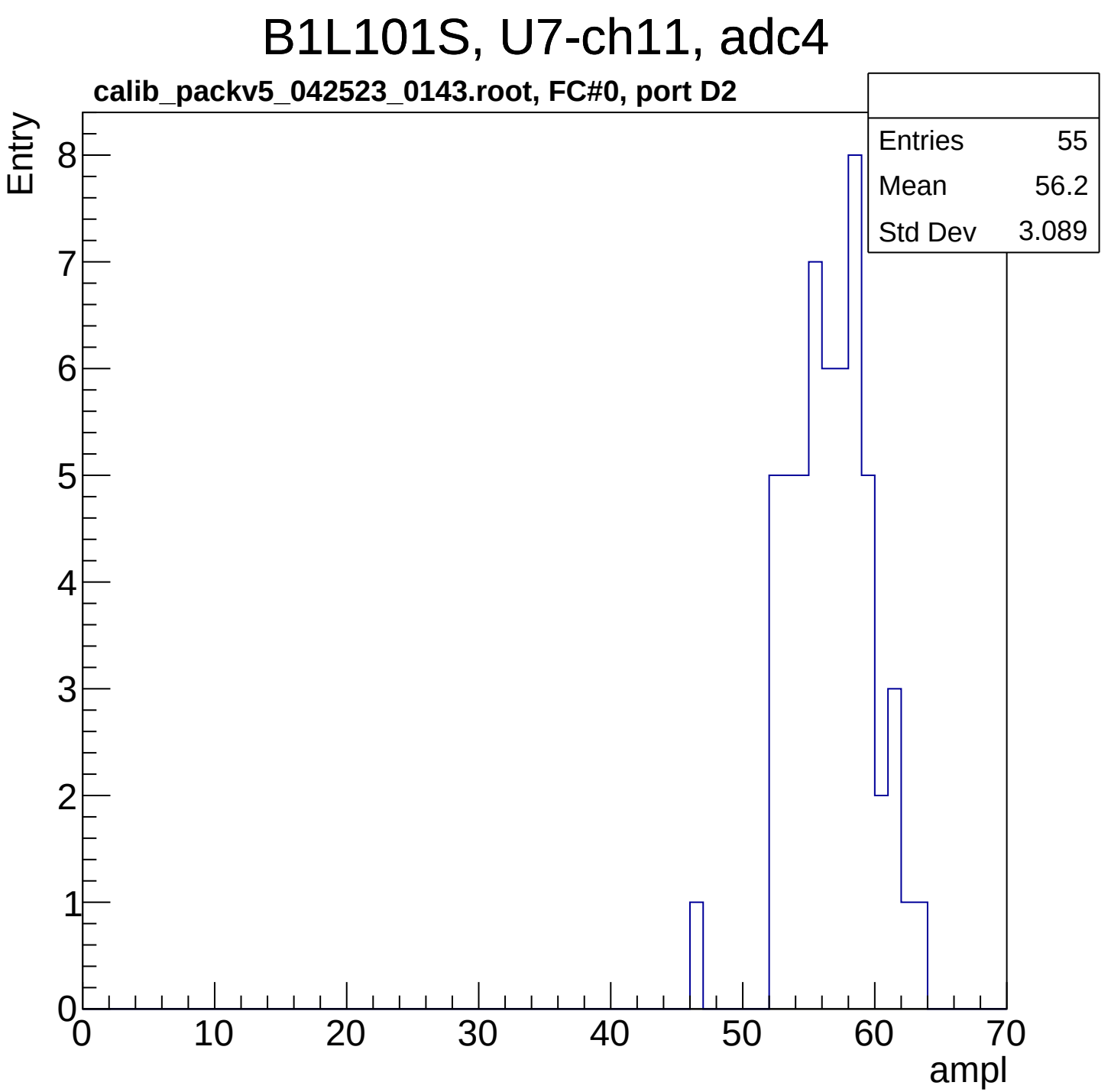
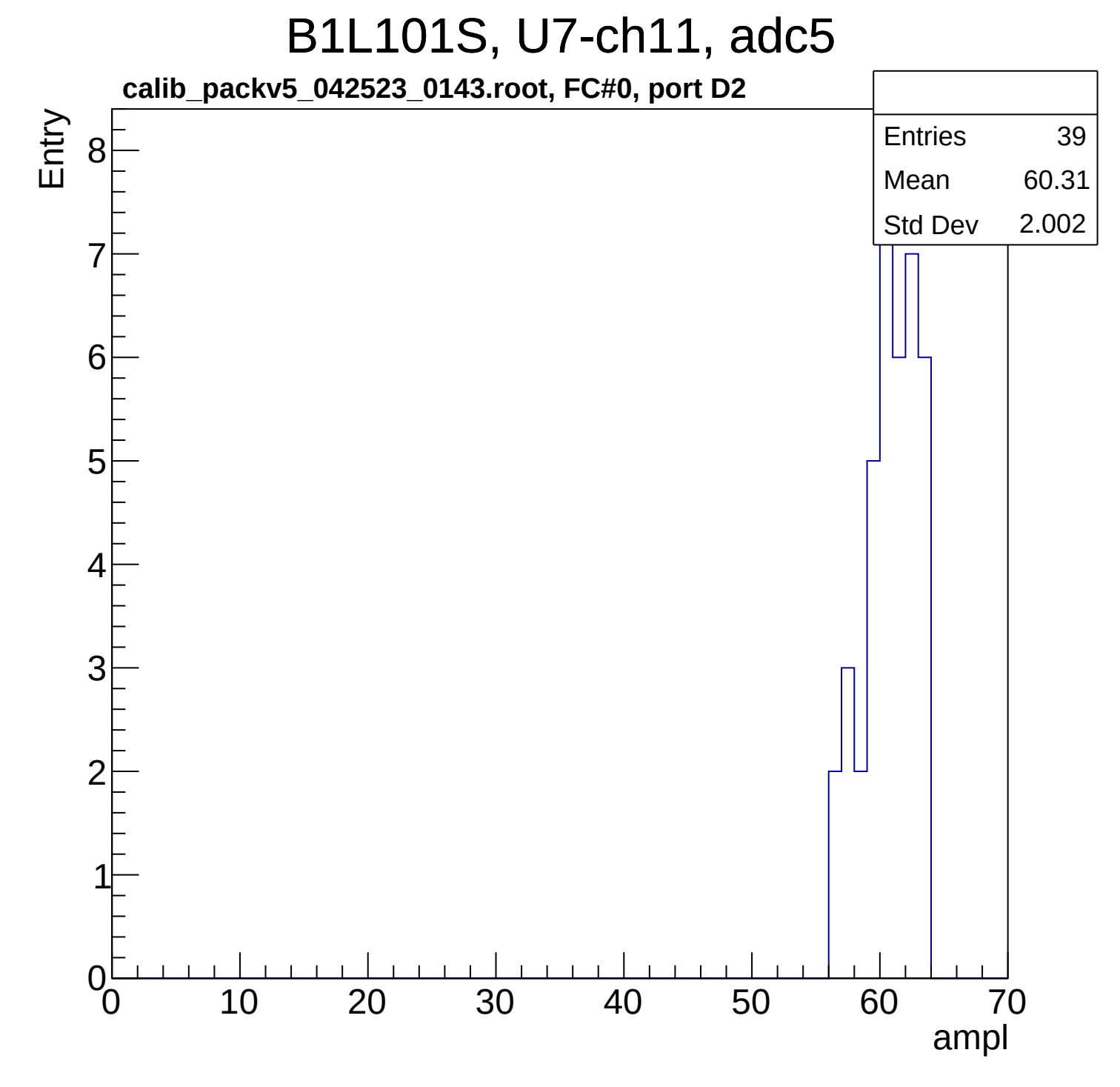

B1L101S, U7-ch11, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 56.2
Std Dev 3.089
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch11, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 39
Mean 60.31
Std Dev 2.002
Entry
ampl
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1
2
3
4
5
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7
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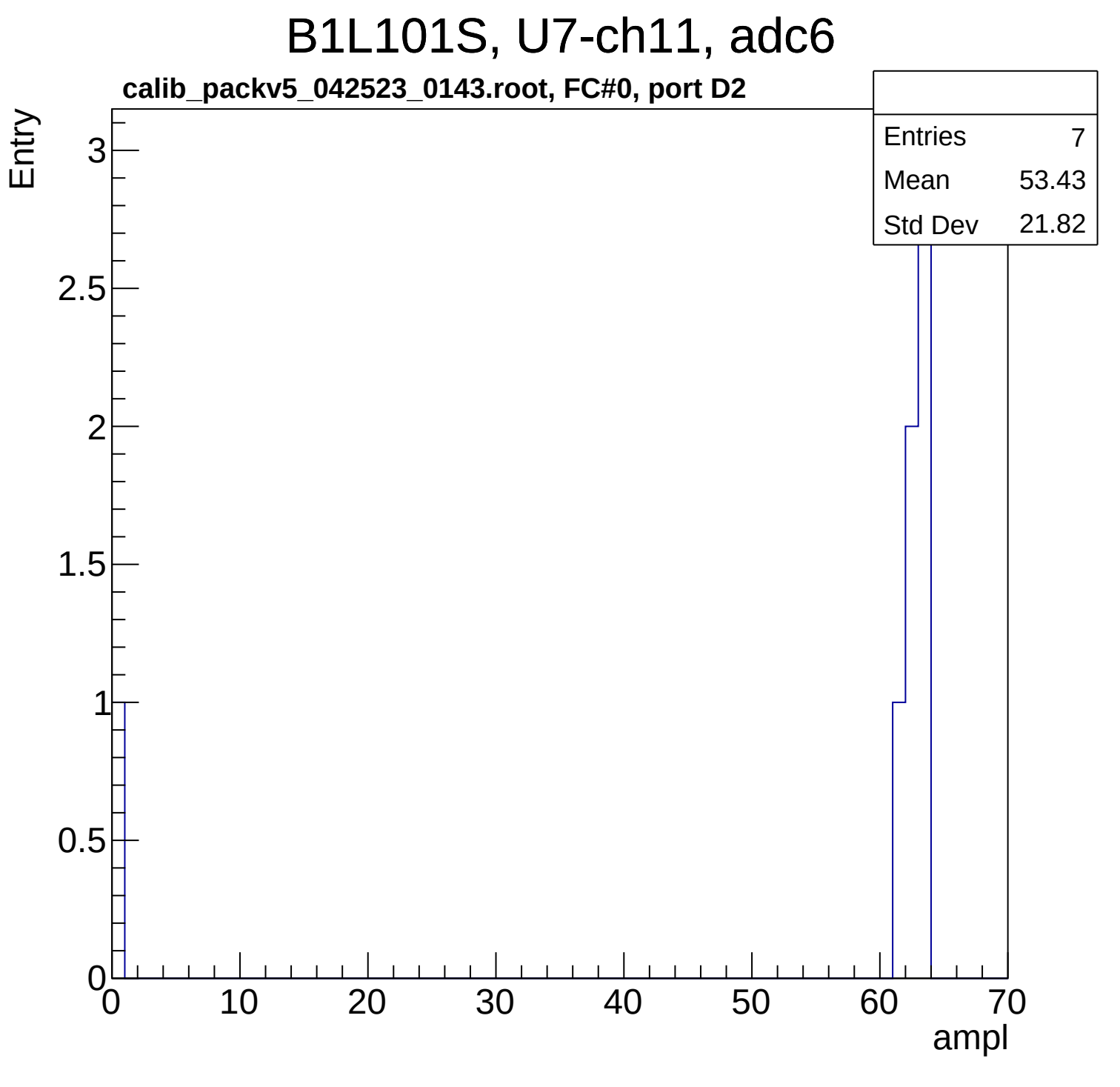
B1L101S, U7-ch11, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 53.43
Std Dev 21.82
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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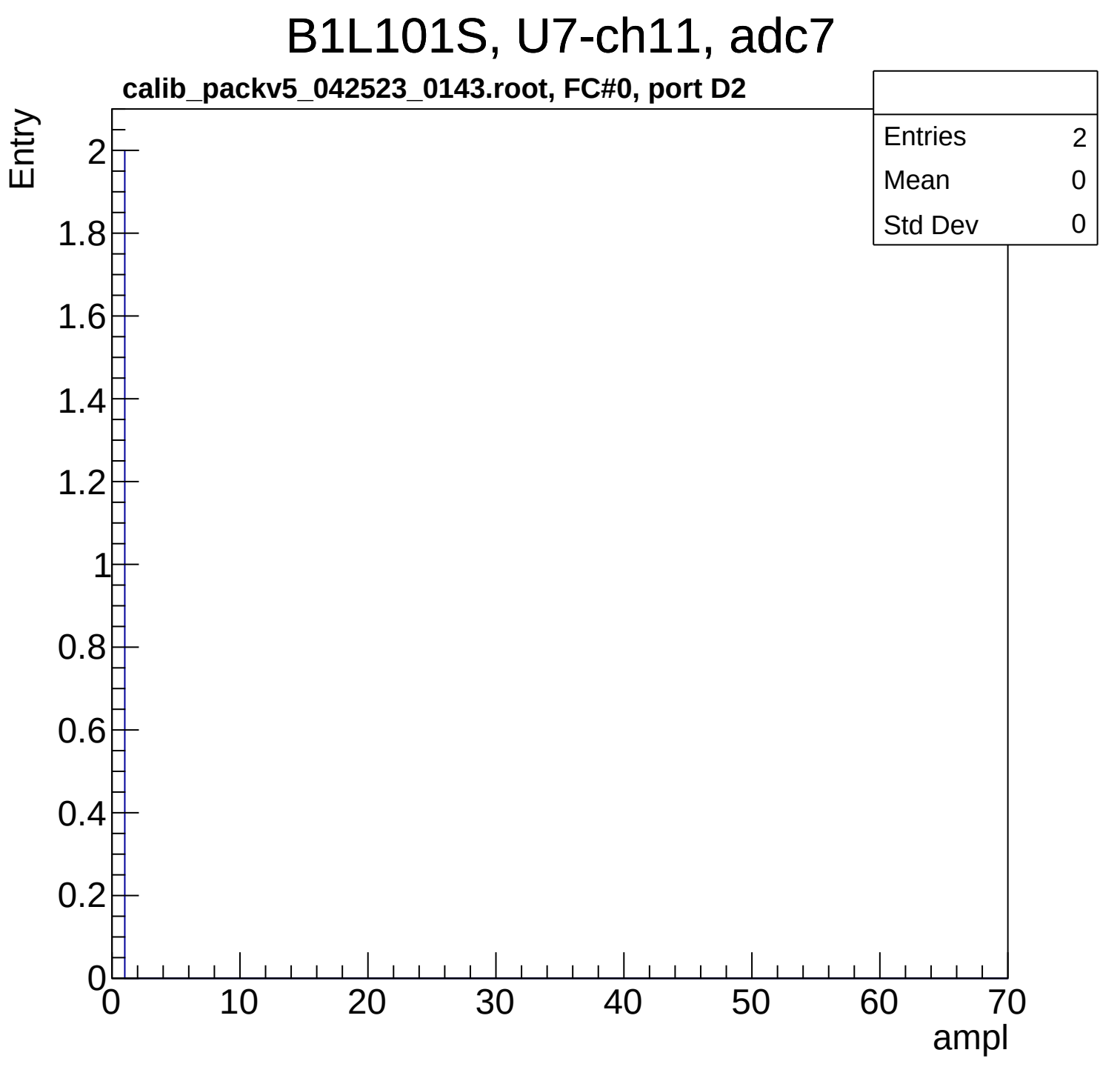
B1L101S, U7-ch11, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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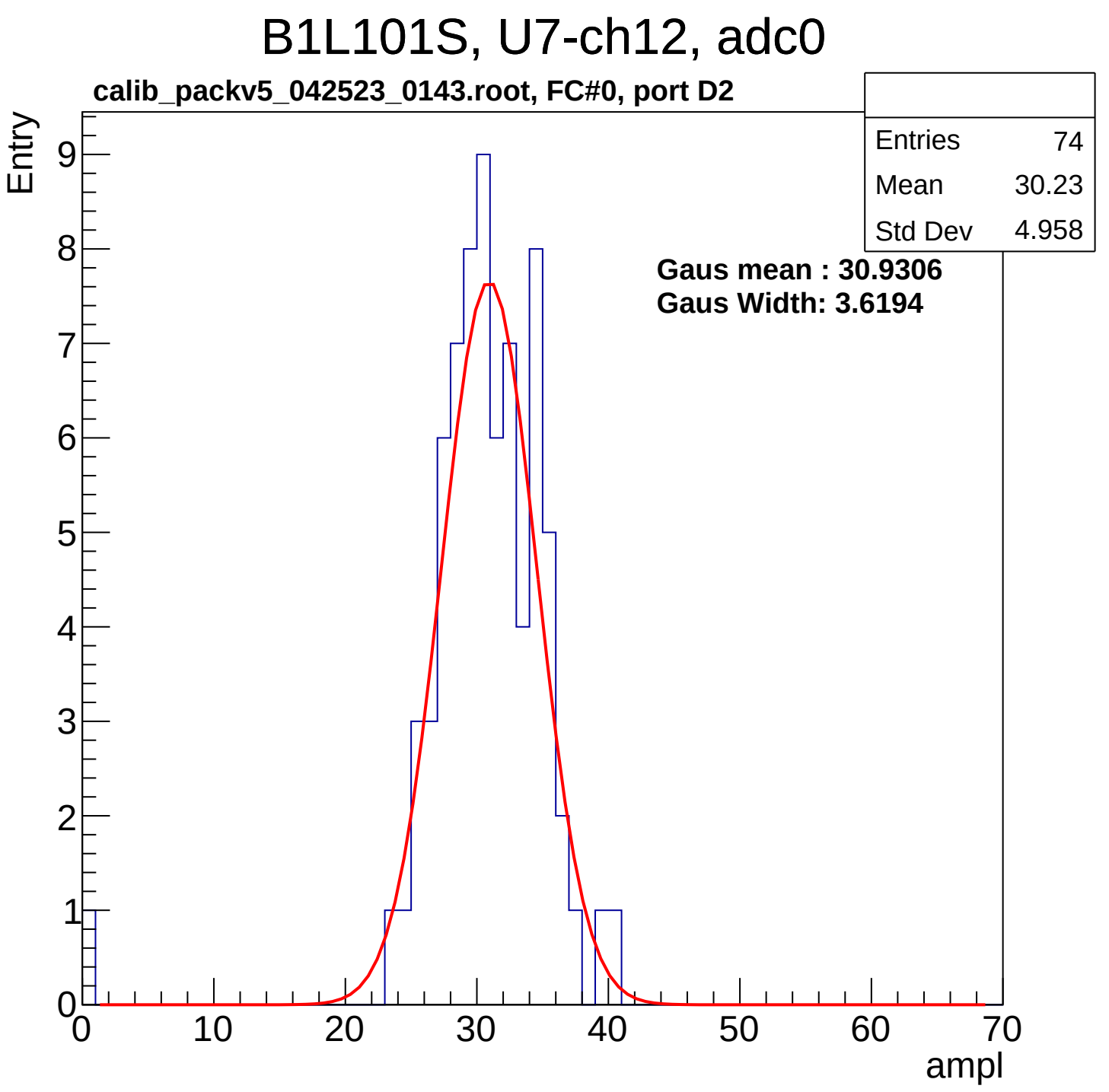
B1L101S, U7-ch12, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 30.23
Std Dev 4.958
Gaus mean : 30.9306
Gaus Width: 3.6194
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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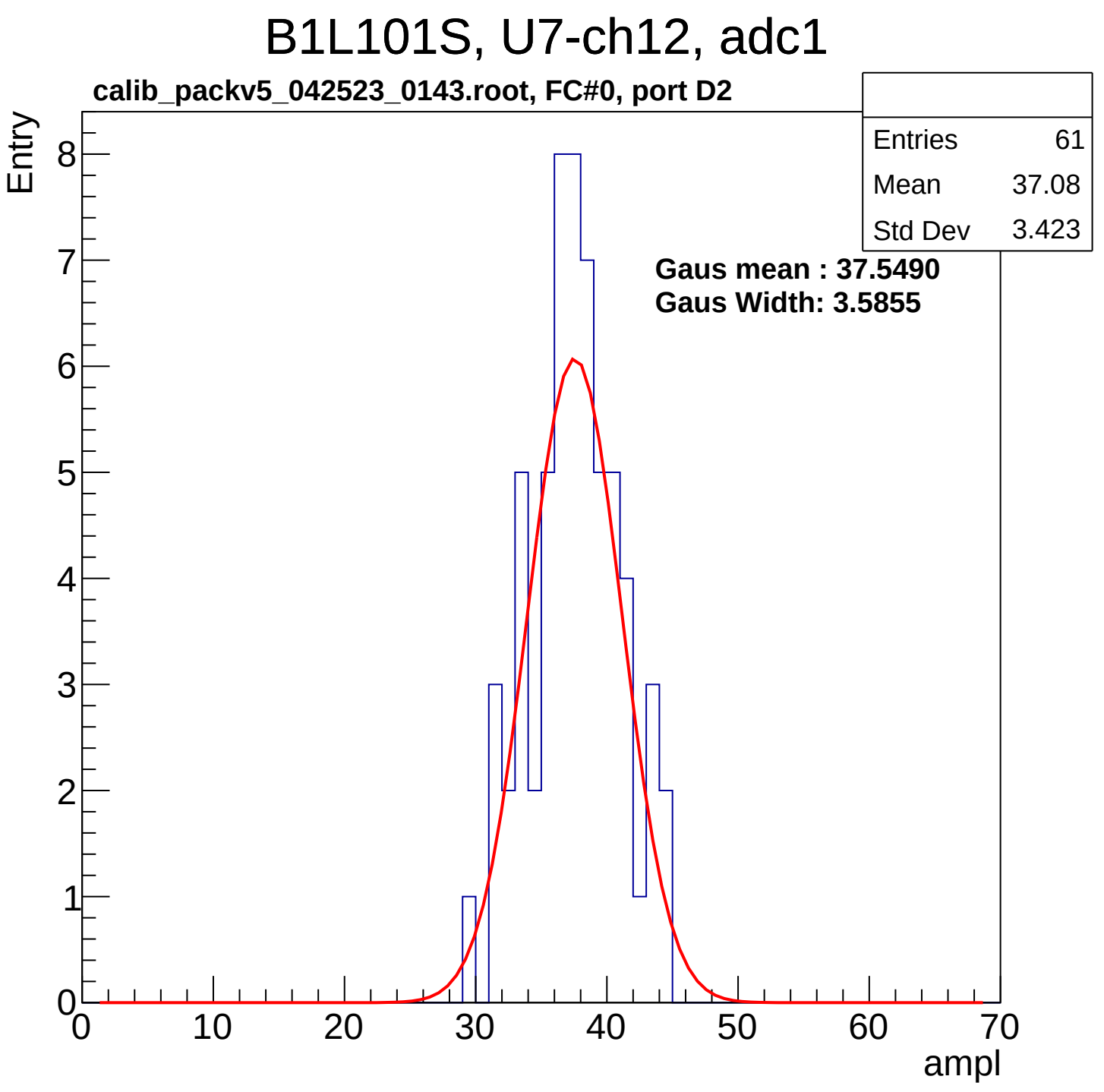
B1L101S, U7-ch12, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 37.08
Std Dev 3.423
Gaus mean : 37.5490
Gaus Width: 3.5855
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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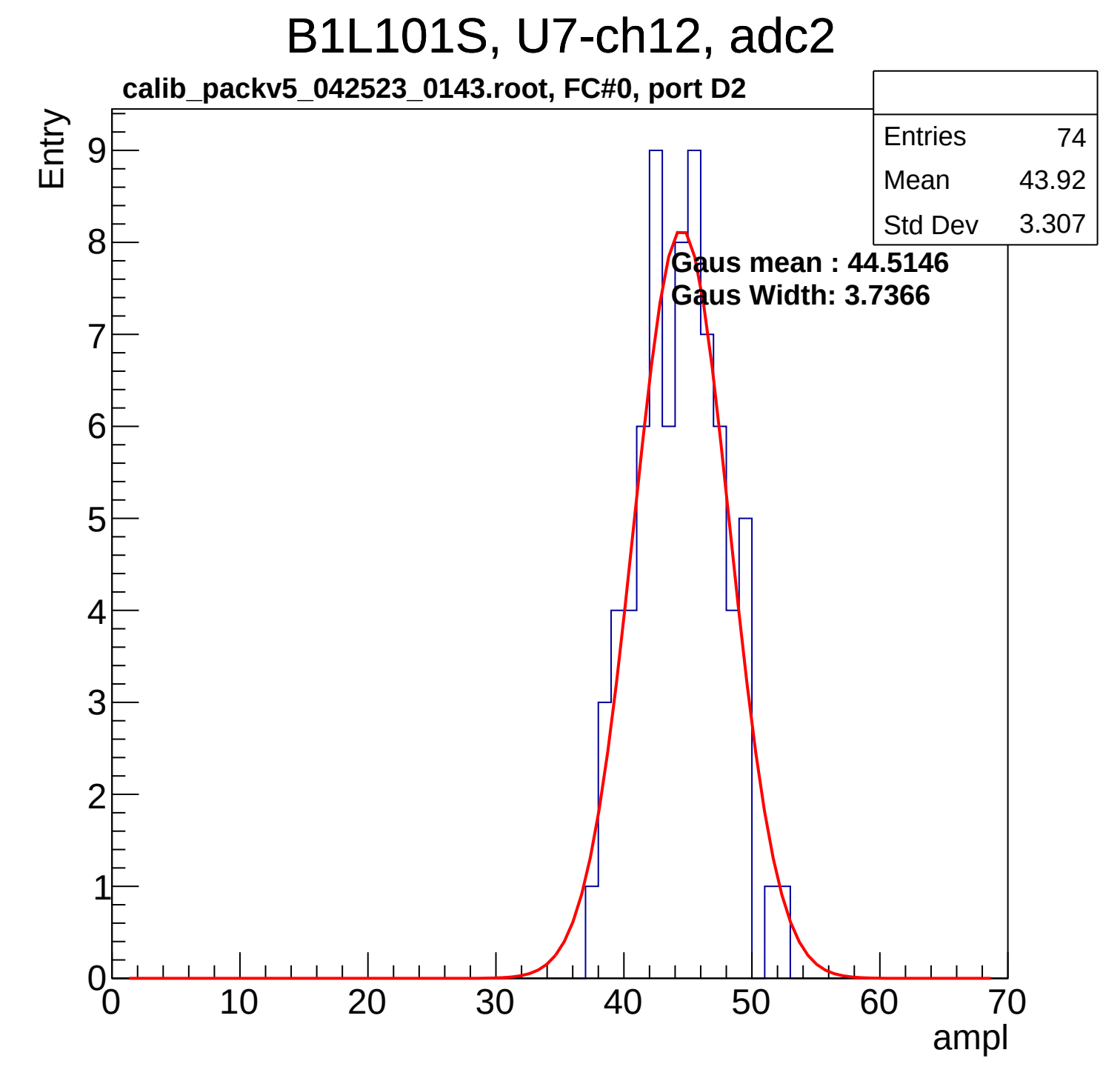
B1L101S, U7-ch12, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 43.92
Std Dev 3.307
Gaus mean : 44.5146
Gaus Width: 3.7366
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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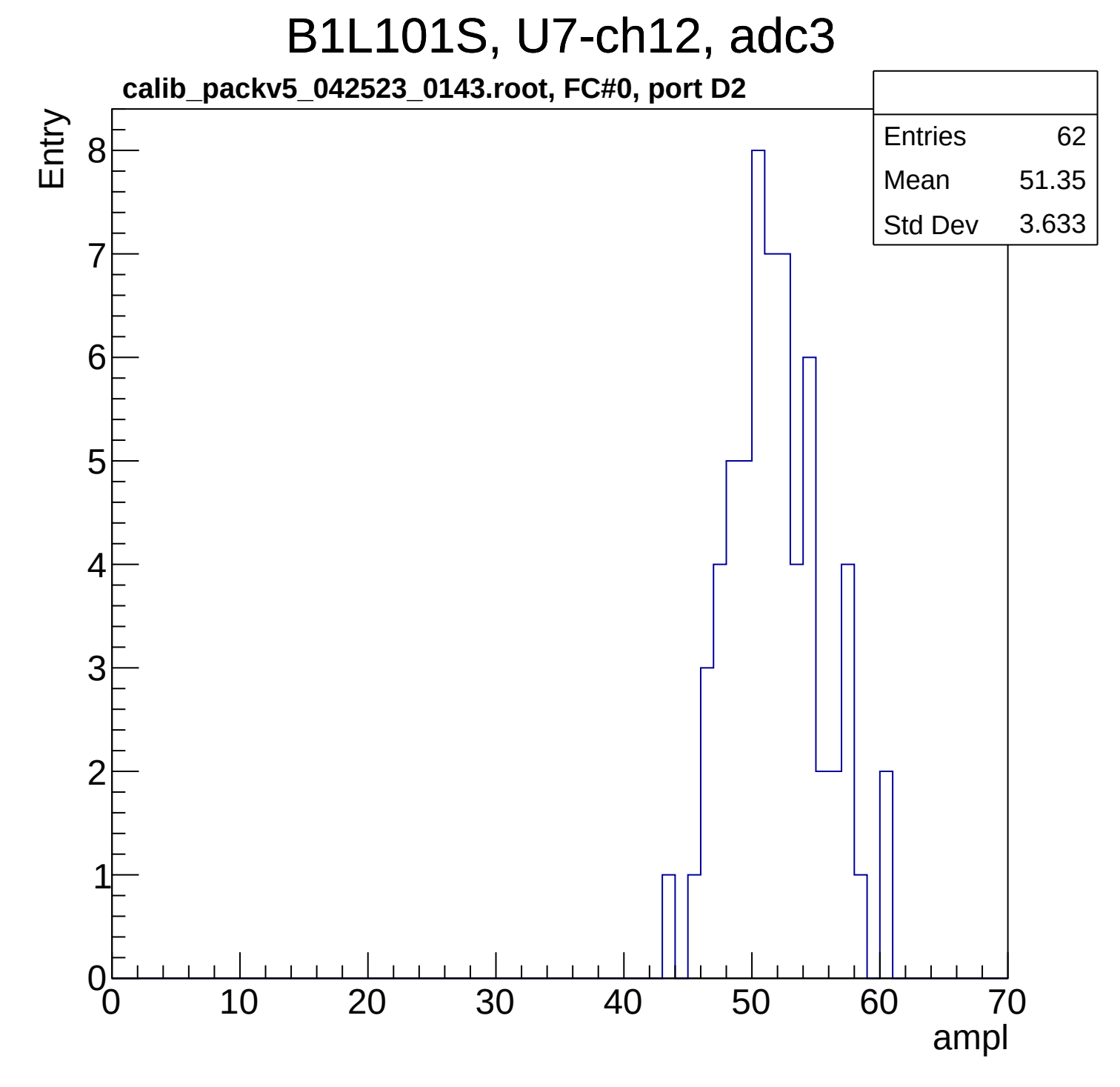
B1L101S, U7-ch12, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 51.35
Std Dev 3.633
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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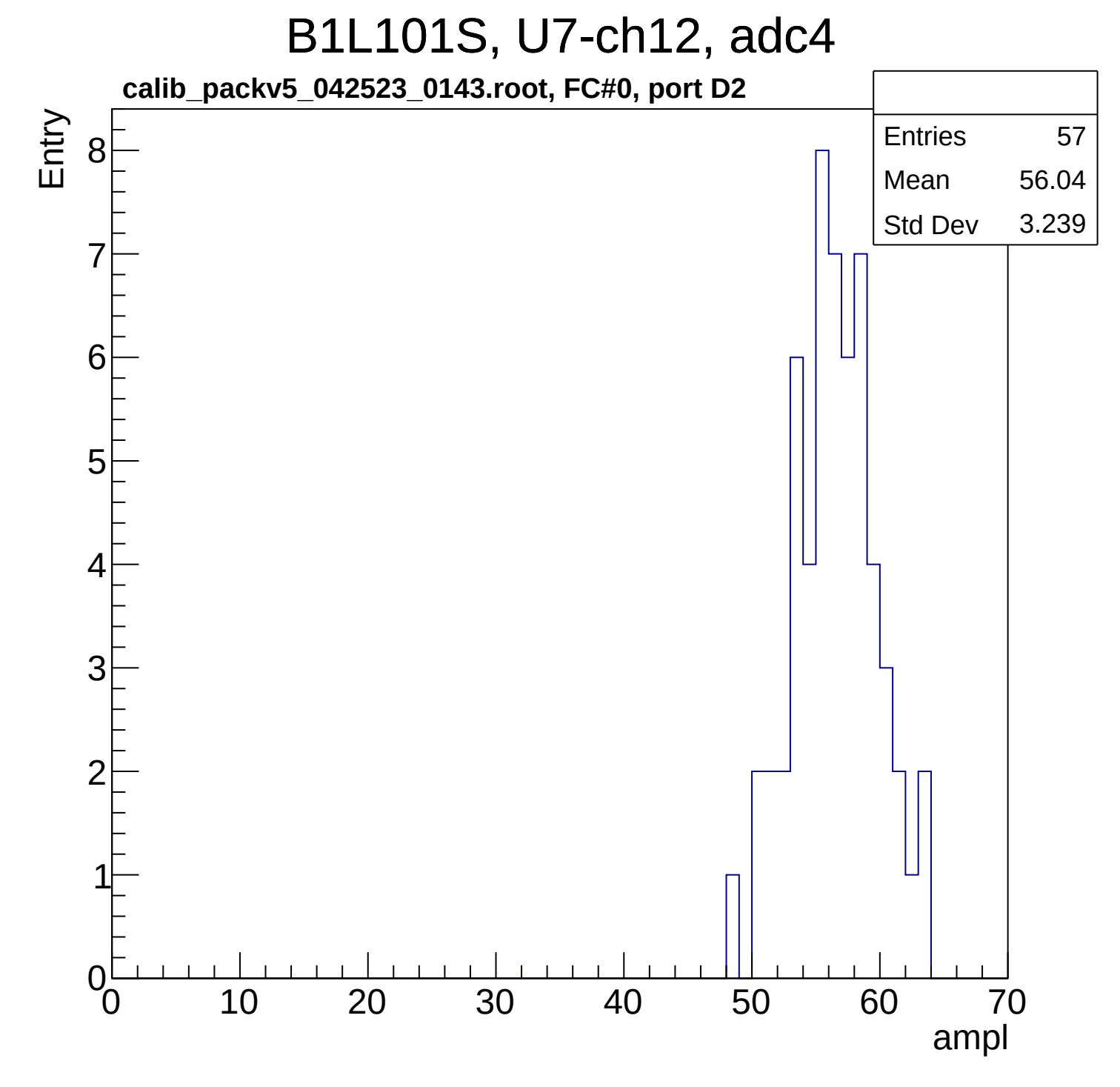
B1L101S, U7-ch12, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 56.04
Std Dev 3.239
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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40
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60
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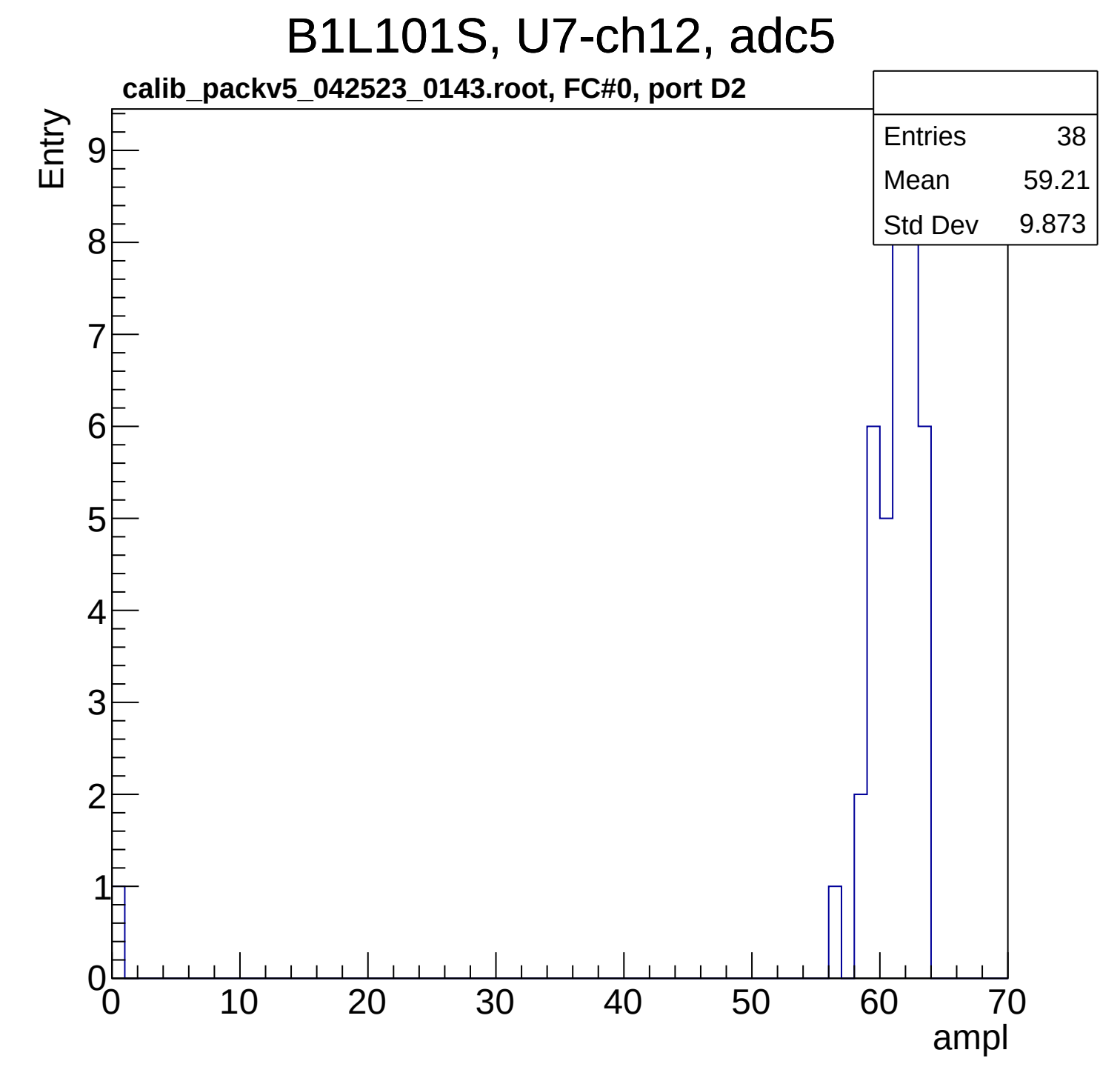
B1L101S, U7-ch12, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 38
Mean 59.21
Std Dev 9.873
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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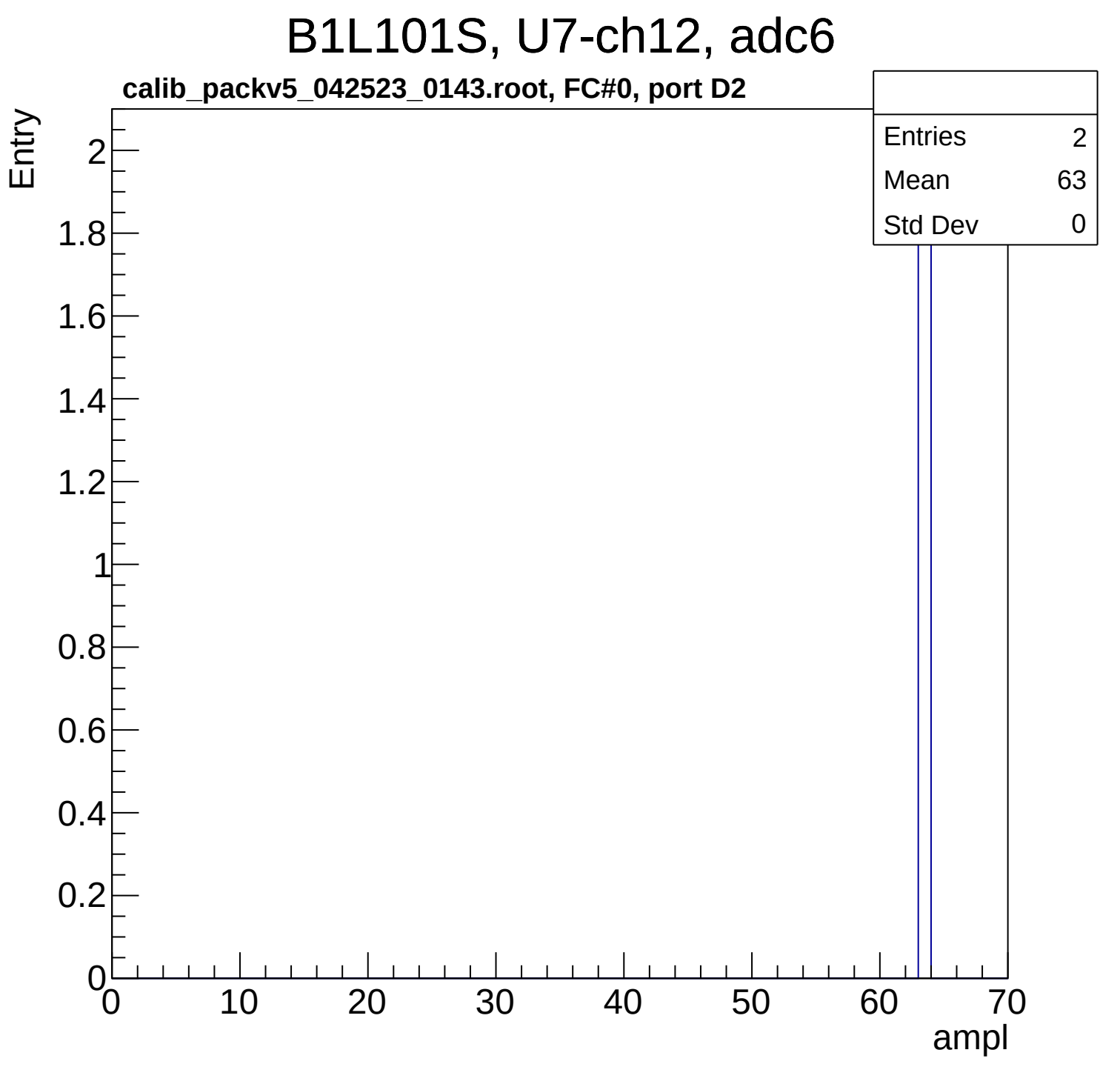
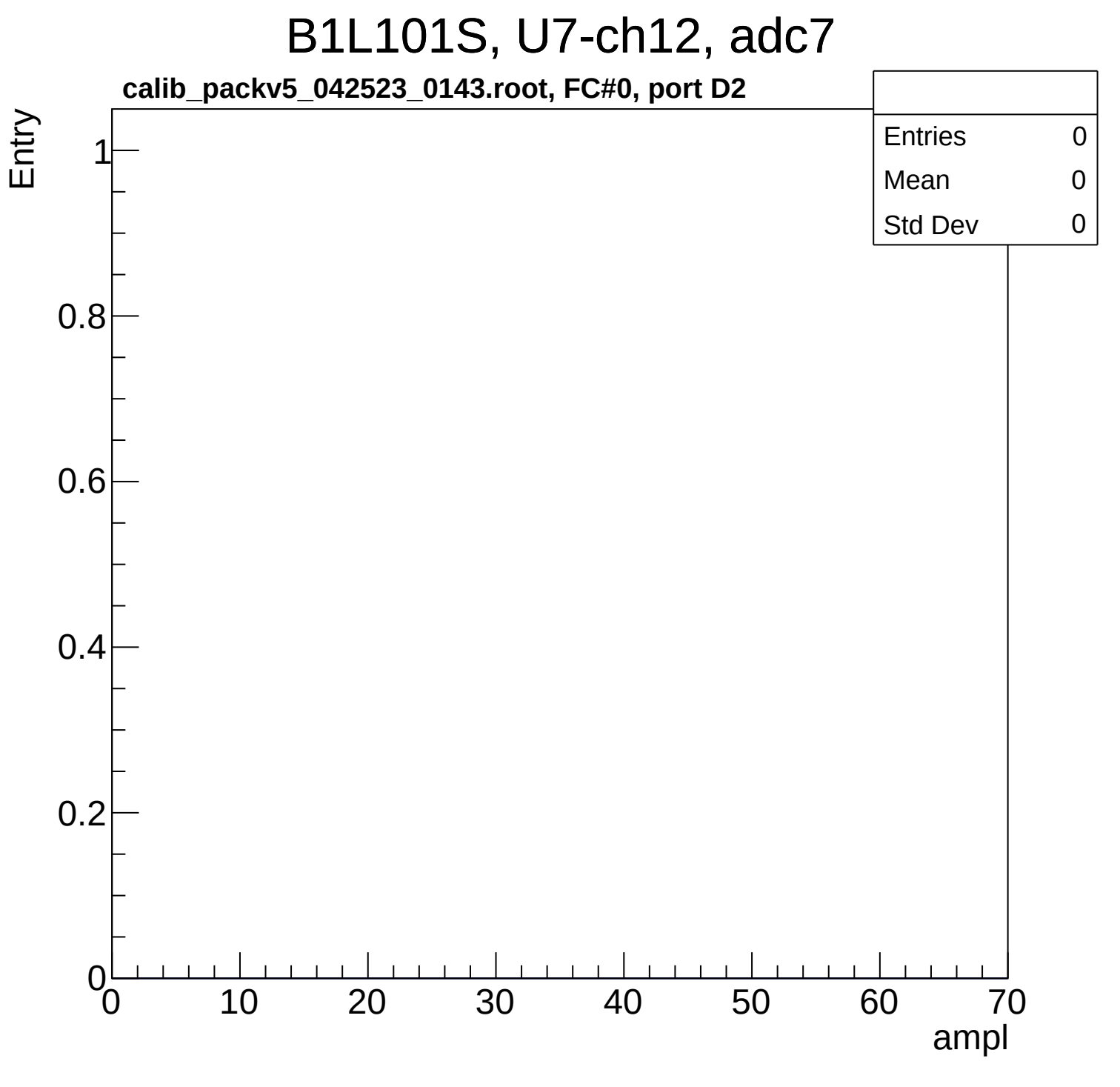
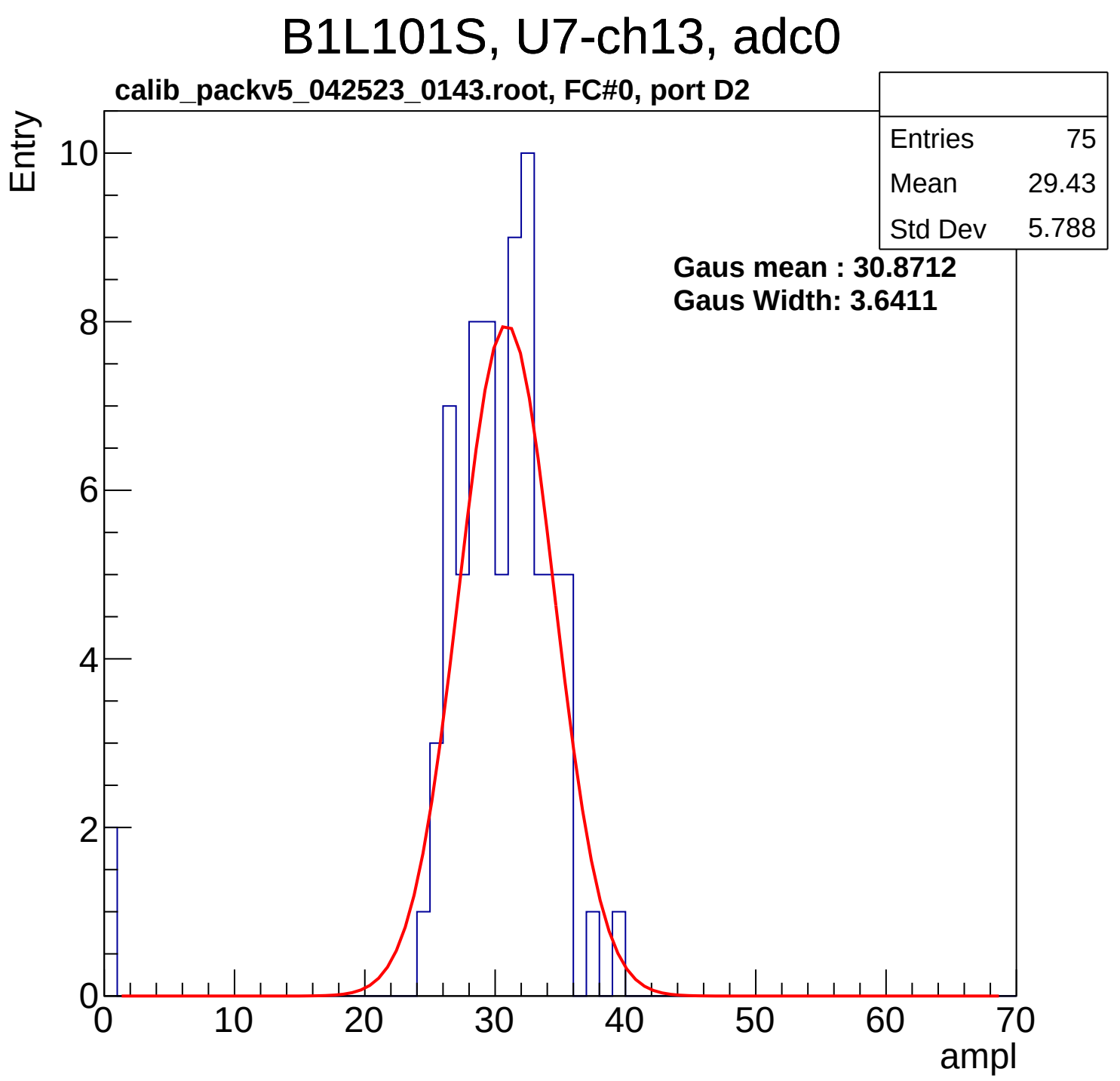

B1L101S, U7-ch12, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U7-ch12, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch13, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 29.43
Std Dev 5.788
Gaus mean : 30.8712
Gaus Width: 3.6411
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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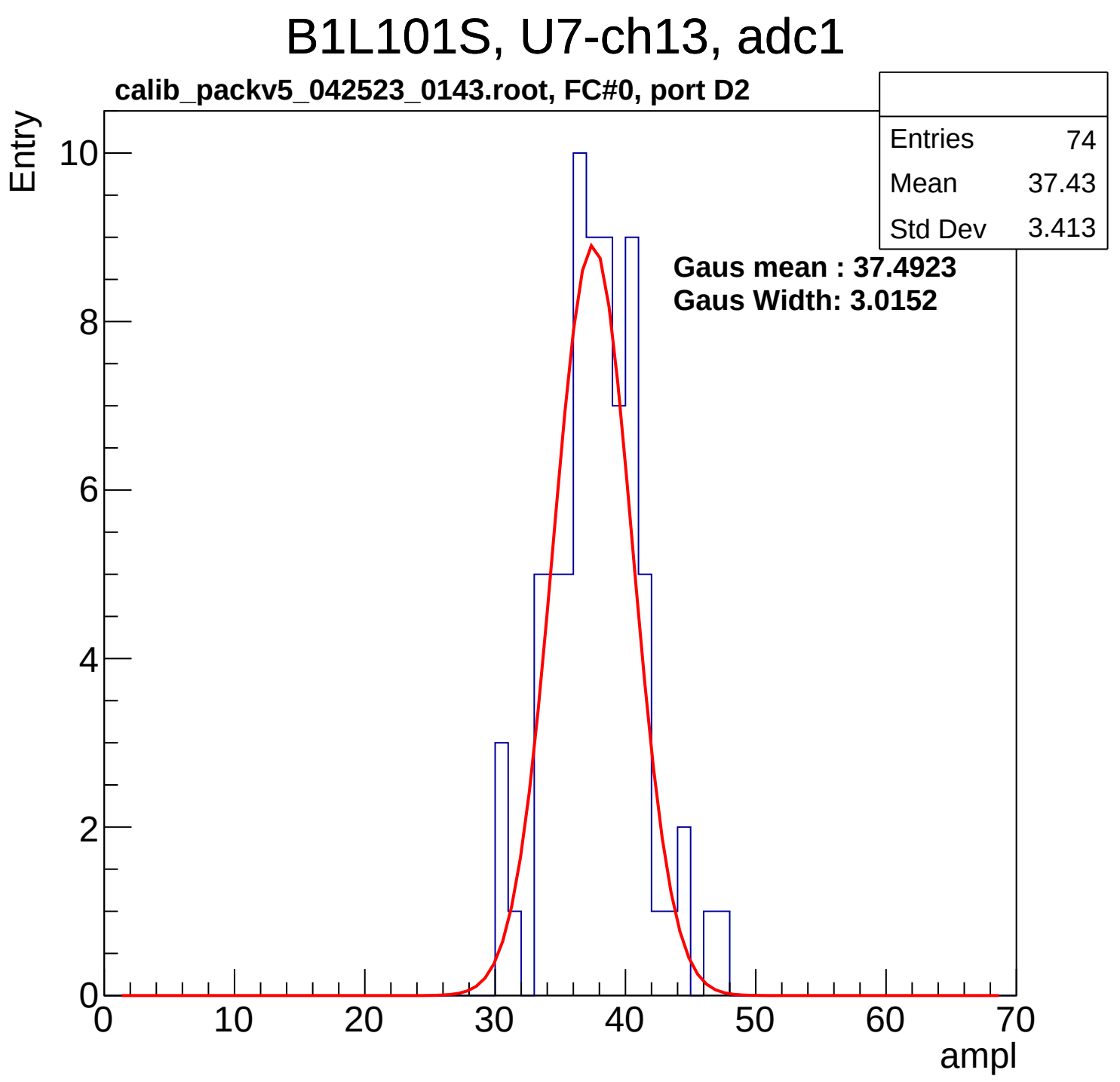
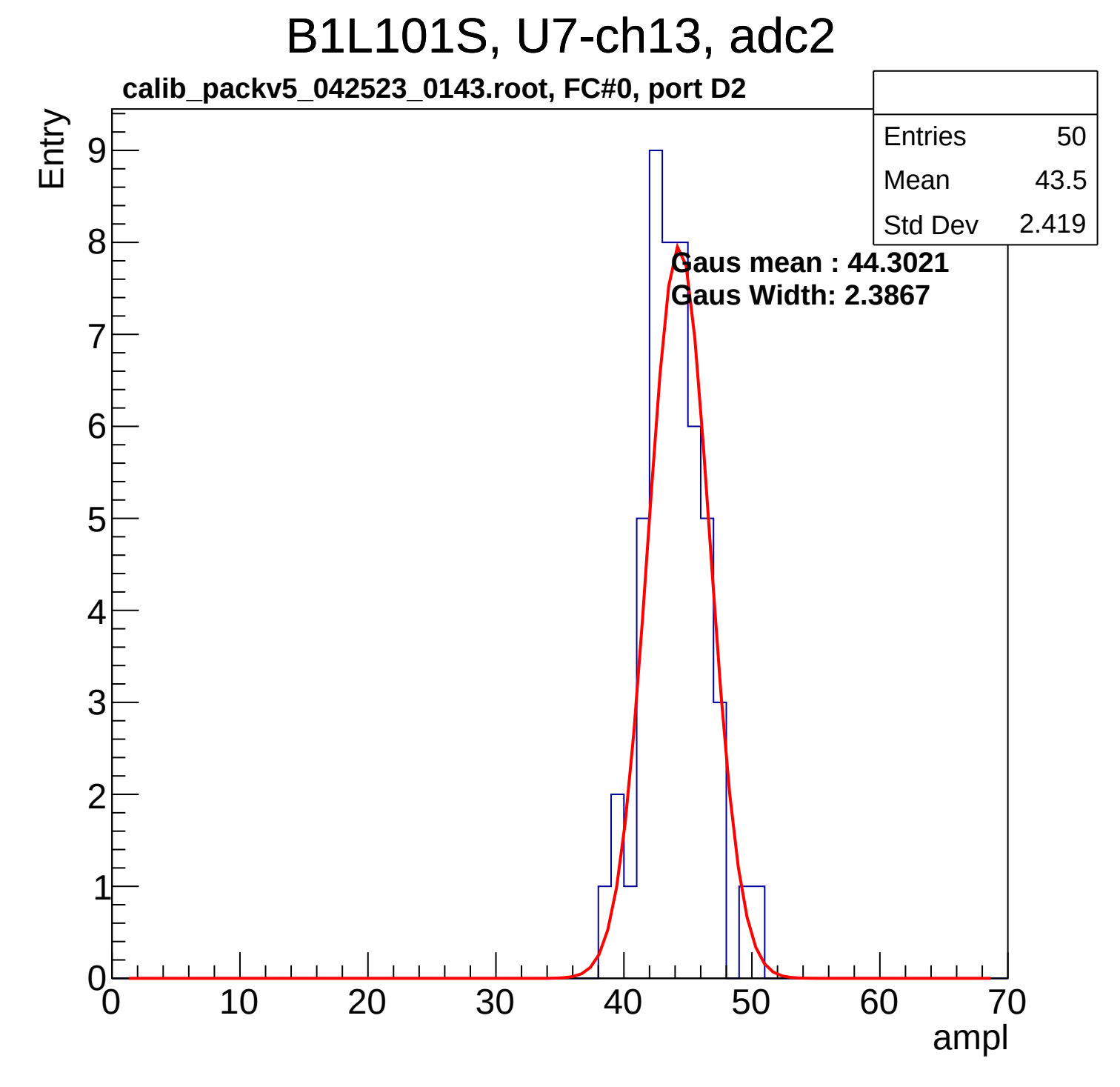

B1L101S, U7-ch13, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 37.43
Std Dev 3.413
Gaus mean : 37.4923
Gaus Width: 3.0152
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch13, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 43.5
Std Dev 2.419
Gaus mean : 44.3021
Gaus Width: 2.3867
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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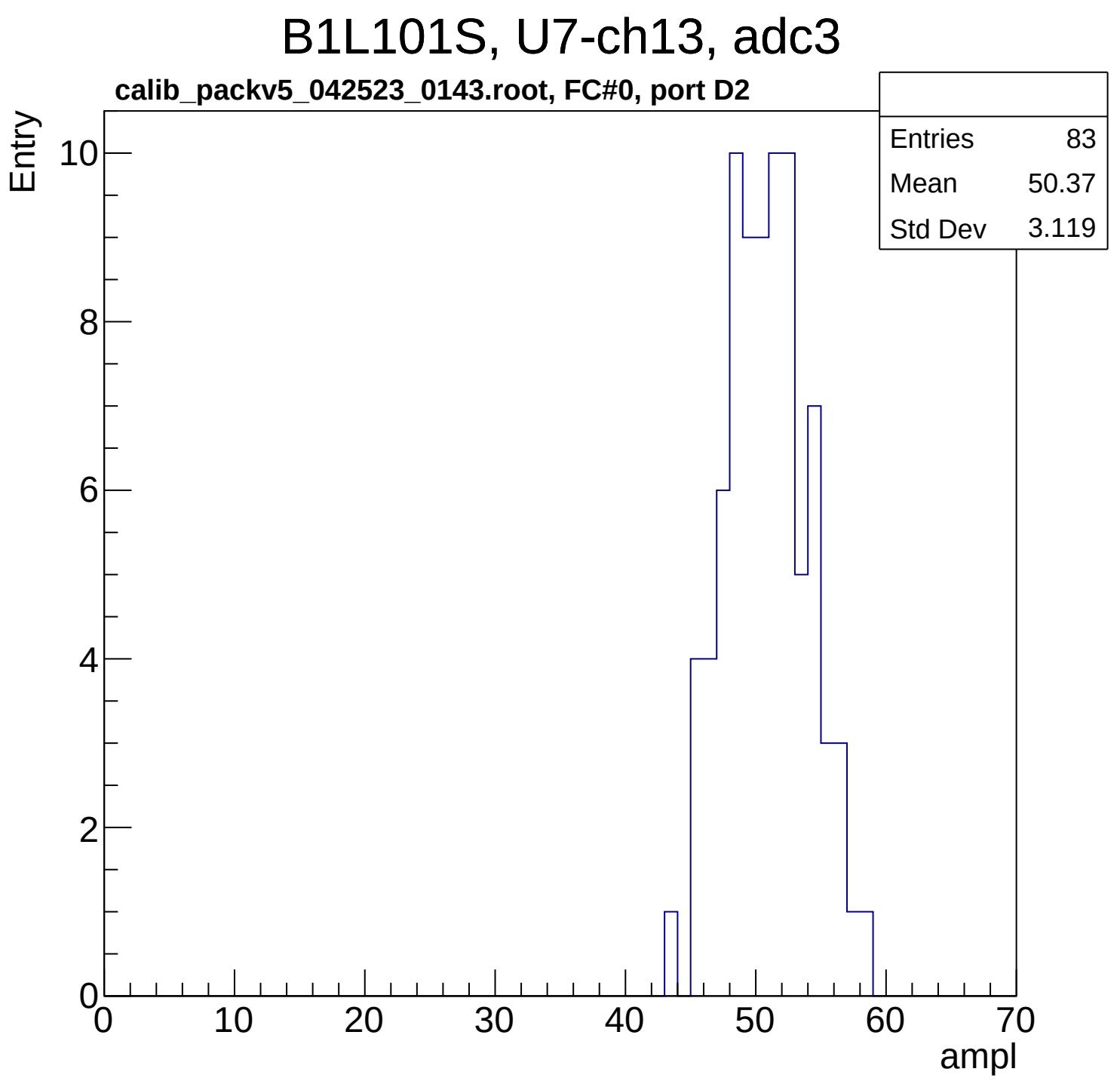
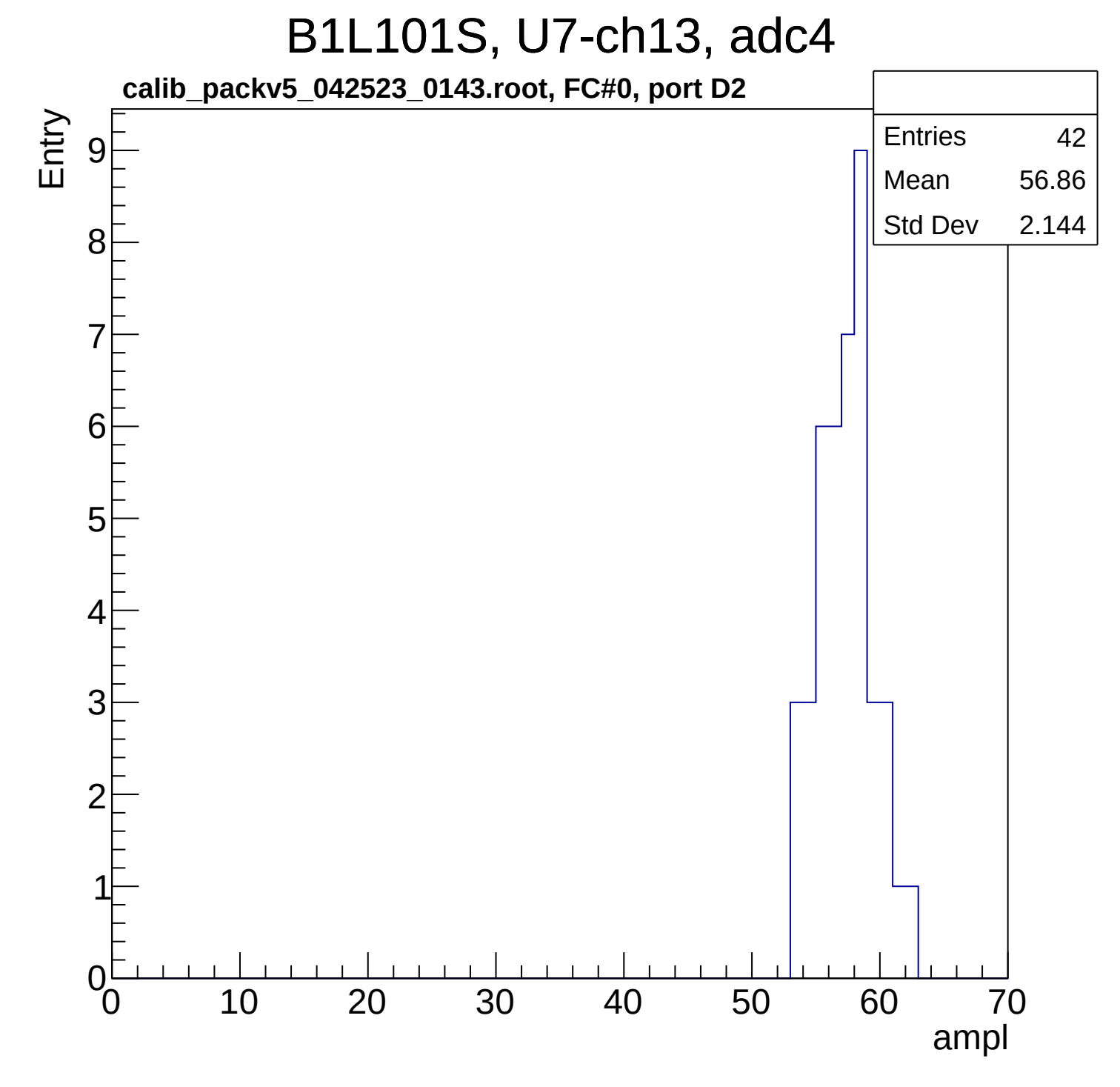
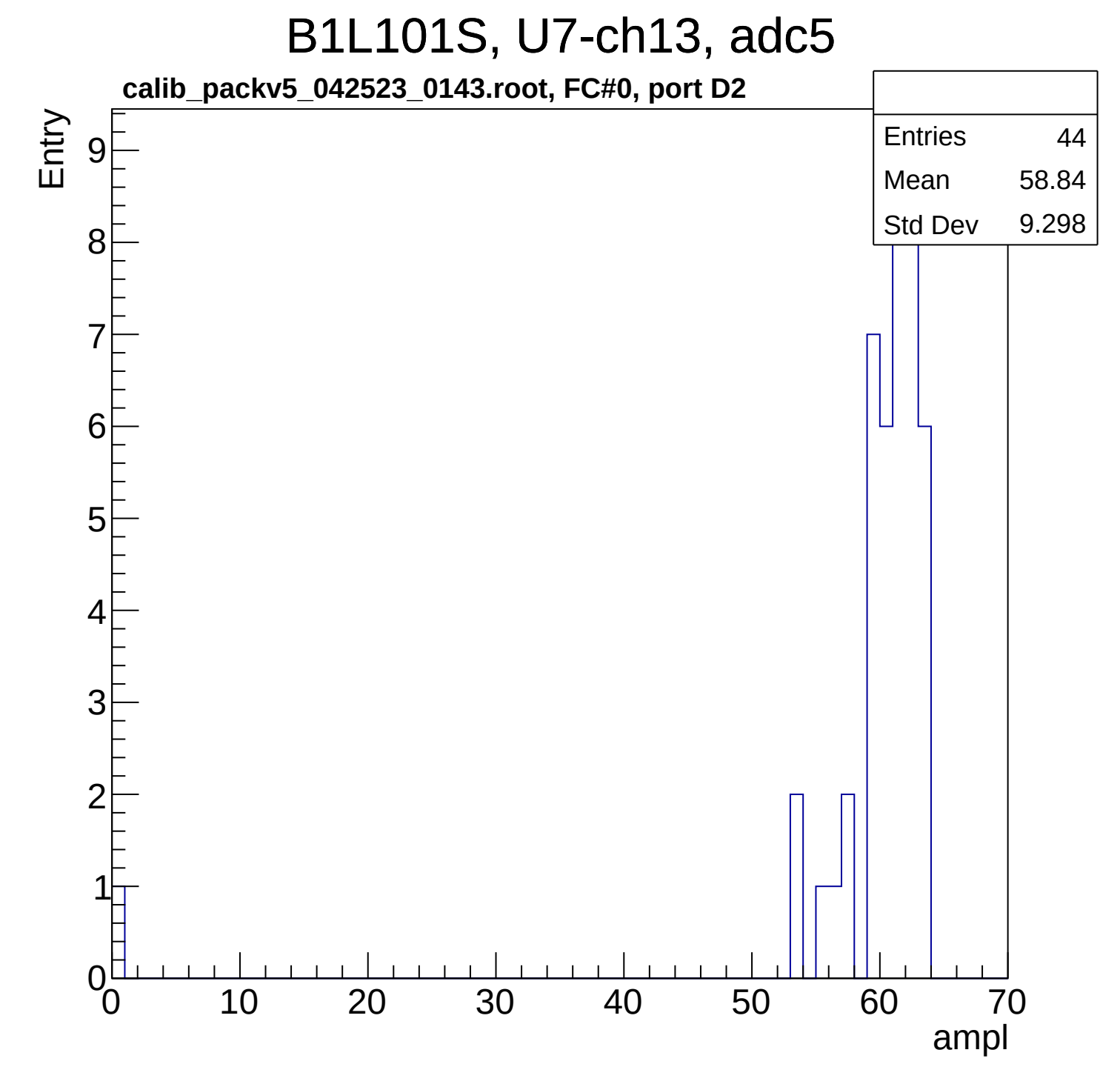

B1L101S, U7-ch13, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 83
Mean 50.37
Std Dev 3.119
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch13, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 56.86
Std Dev 2.144
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch13, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 44
Mean 58.84
Std Dev 9.298
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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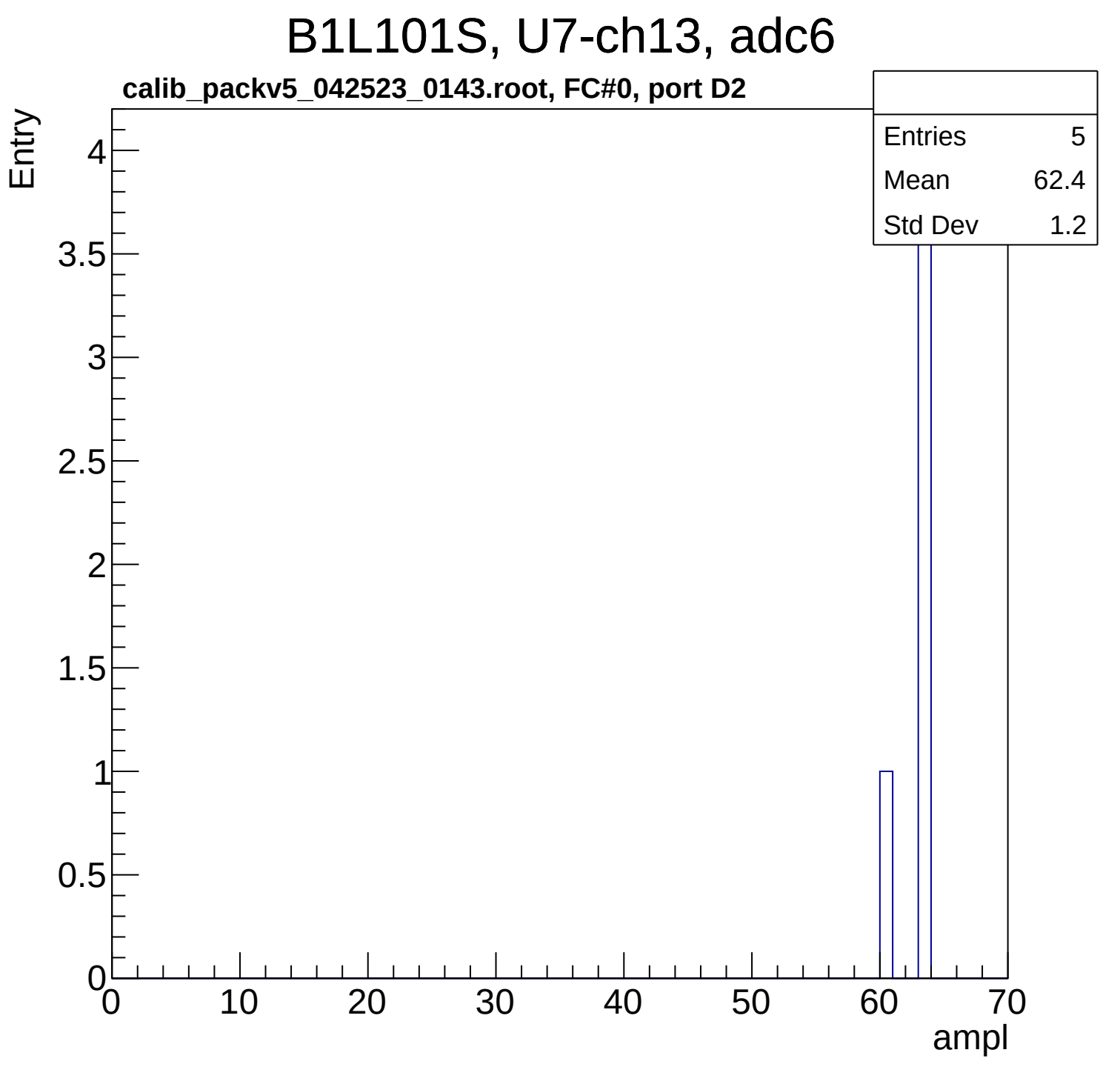
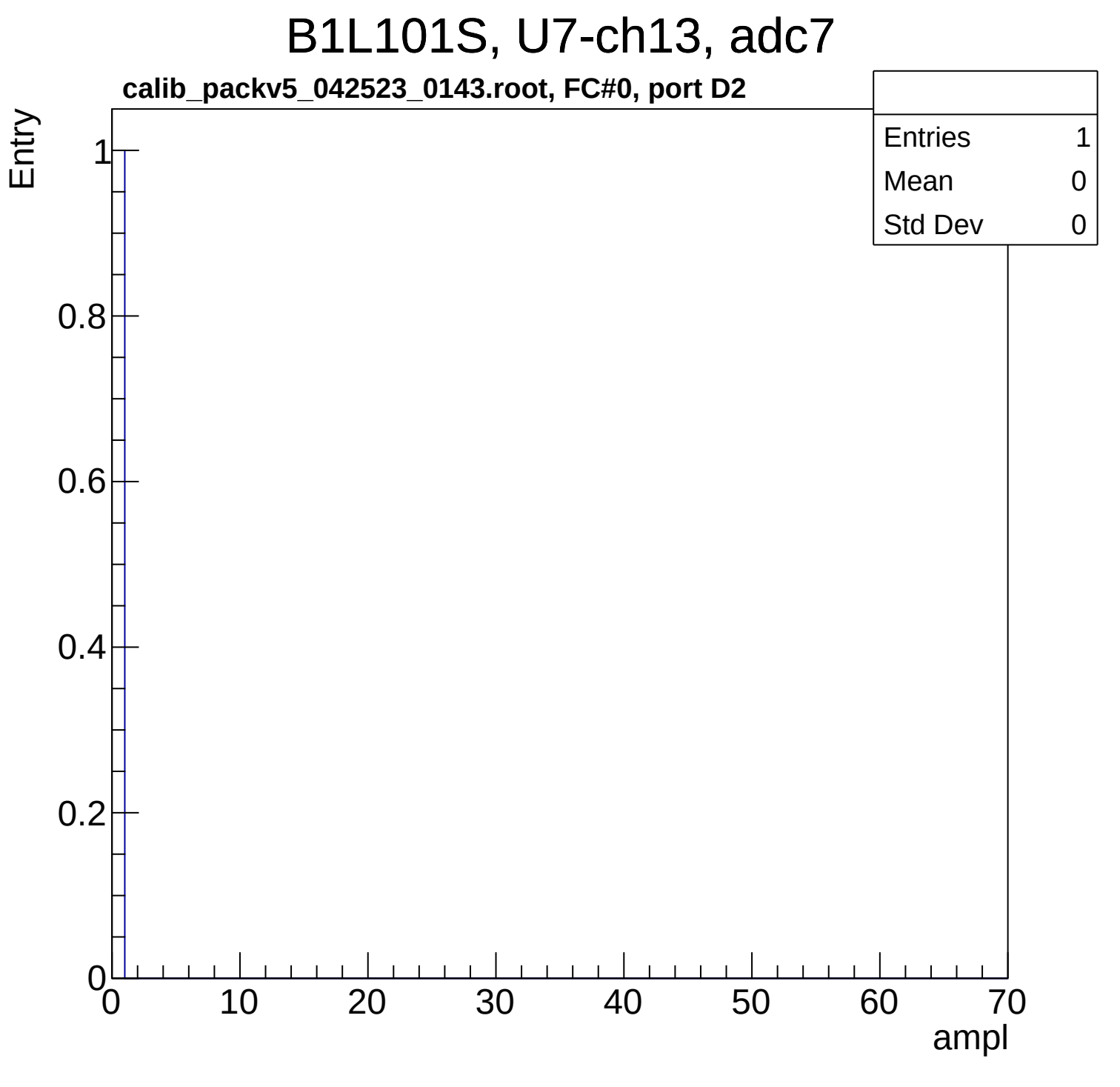
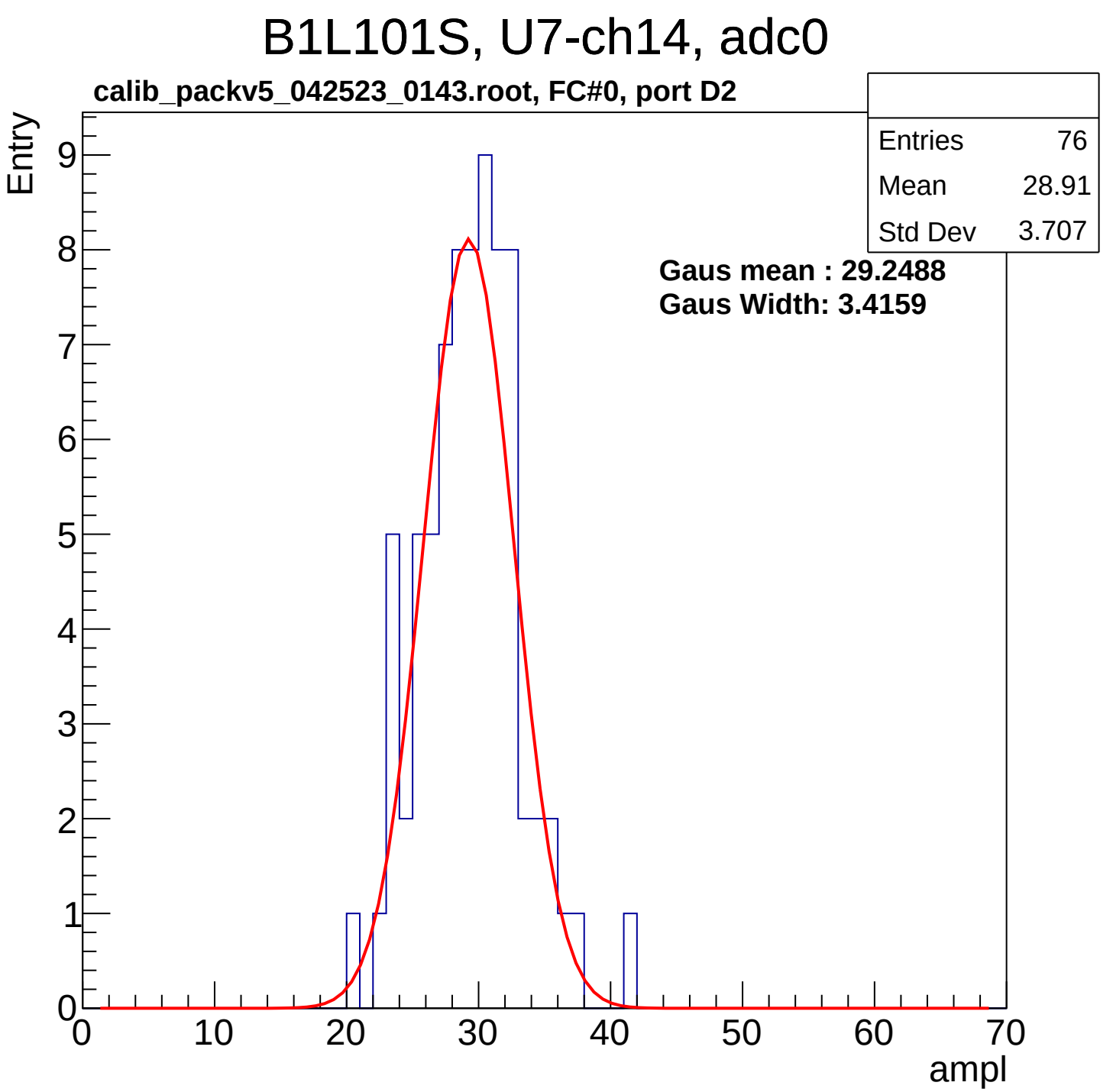

B1L101S, U7-ch13, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 62.4
Std Dev 1.2
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L101S, U7-ch13, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch14, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 28.91
Std Dev 3.707
Gaus mean : 29.2488
Gaus Width: 3.4159
Entry
ampl
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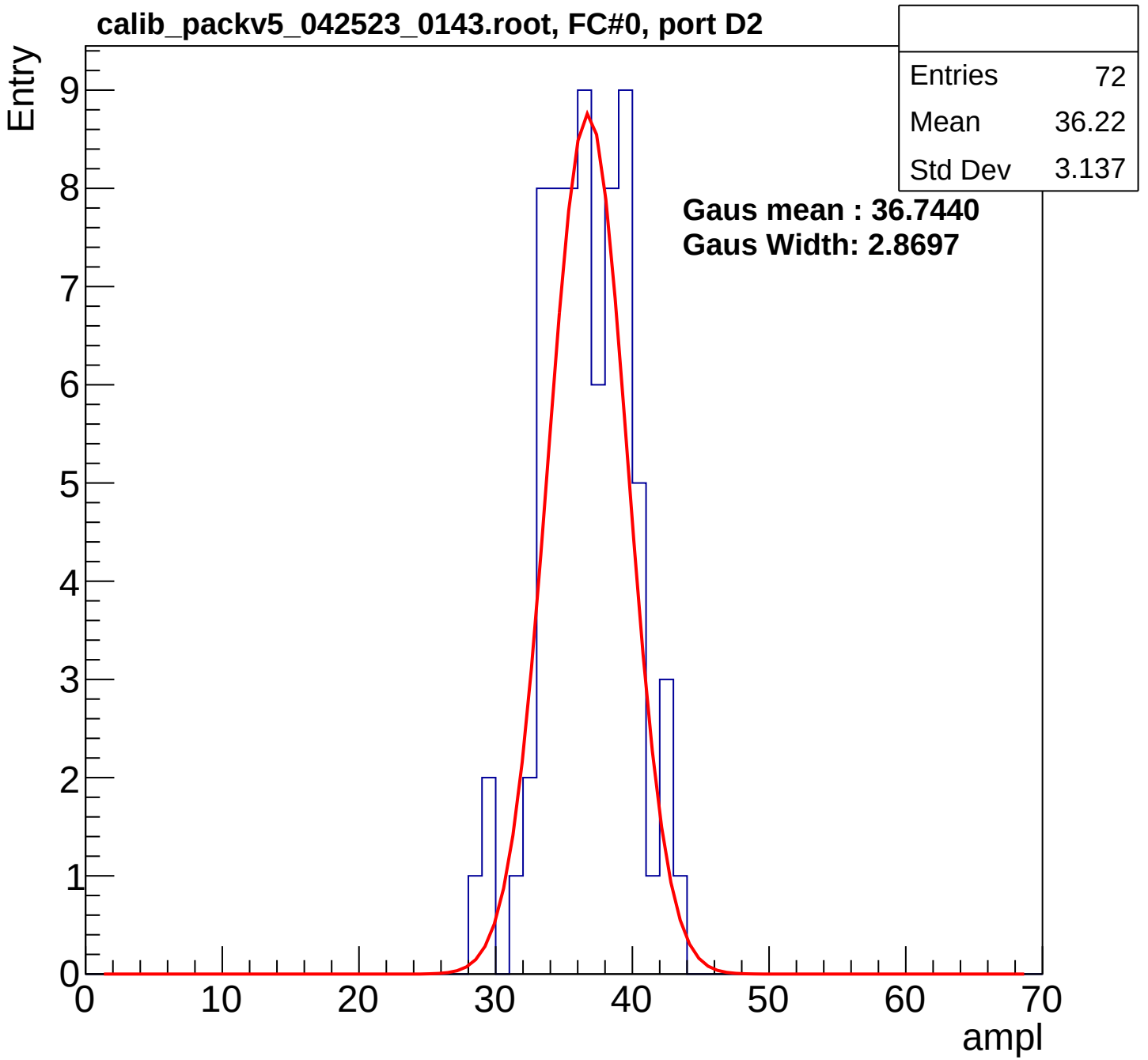
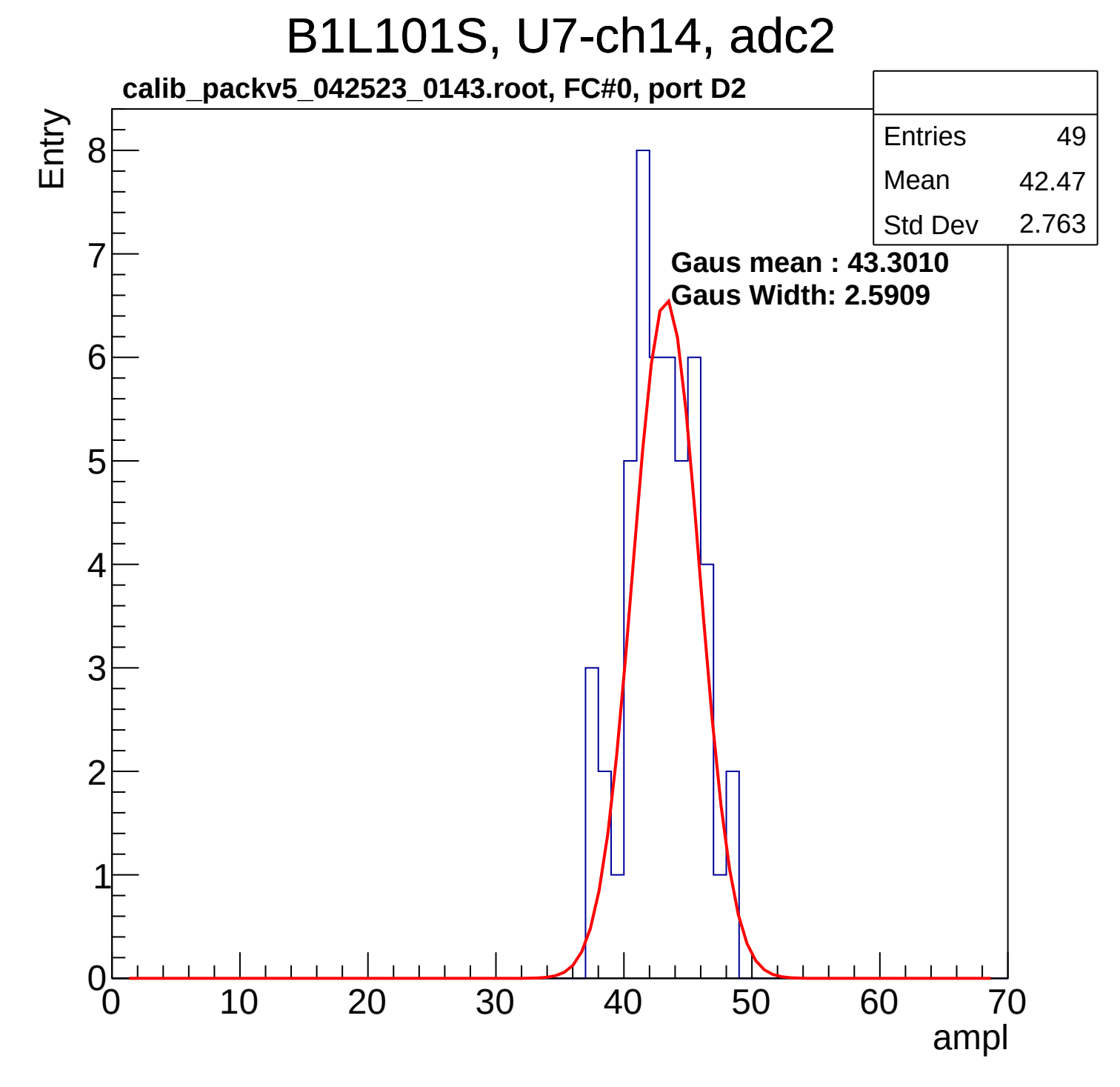
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch14, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 36.22
Std Dev 3.137
Gaus mean : 36.7440
Gaus Width: 2.8697
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch14, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 42.47
Std Dev 2.763
Gaus mean : 43.3010
Gaus Width: 2.5909
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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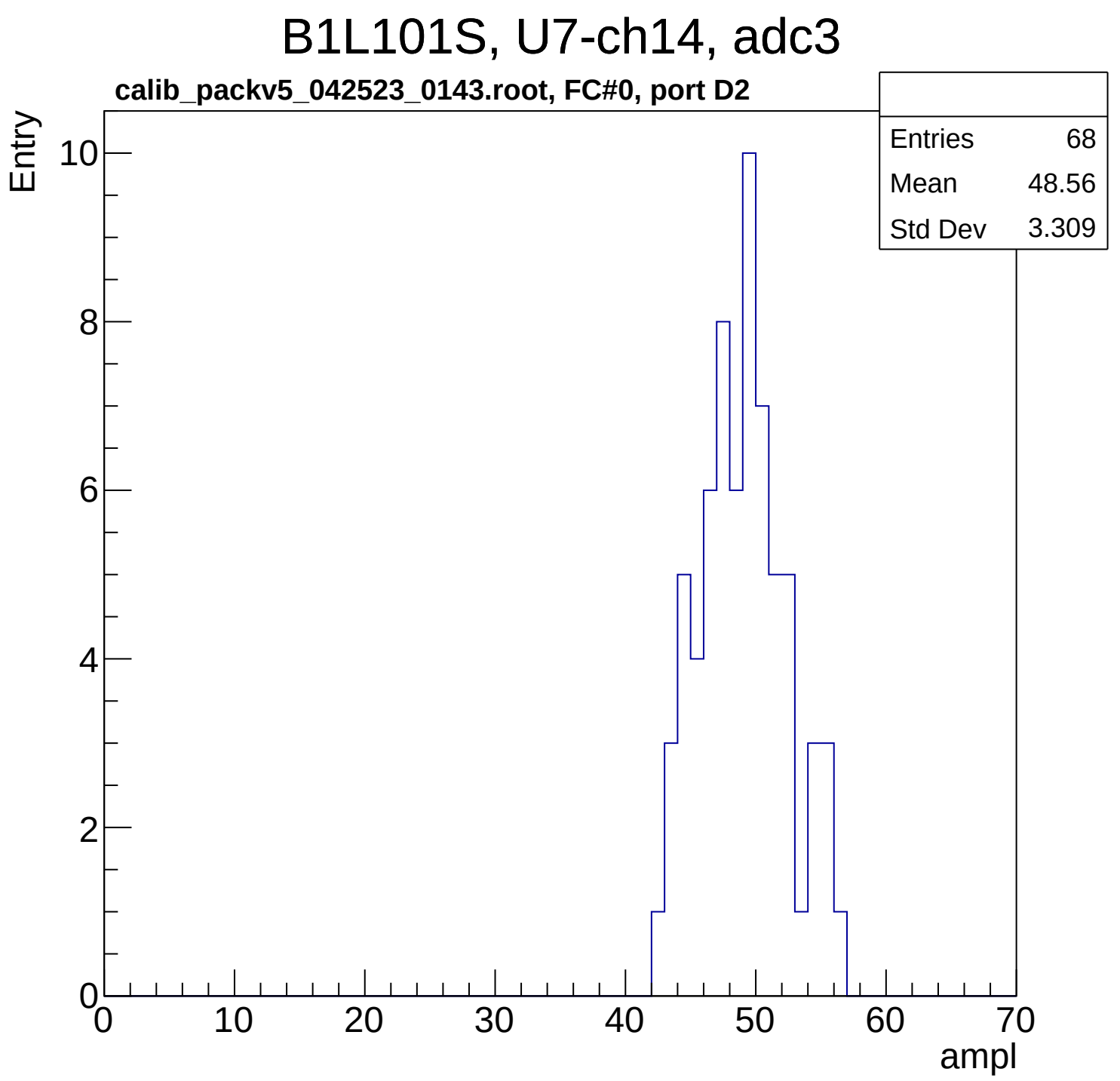
B1L101S, U7-ch14, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 48.56
Std Dev 3.309
Entry
ampl
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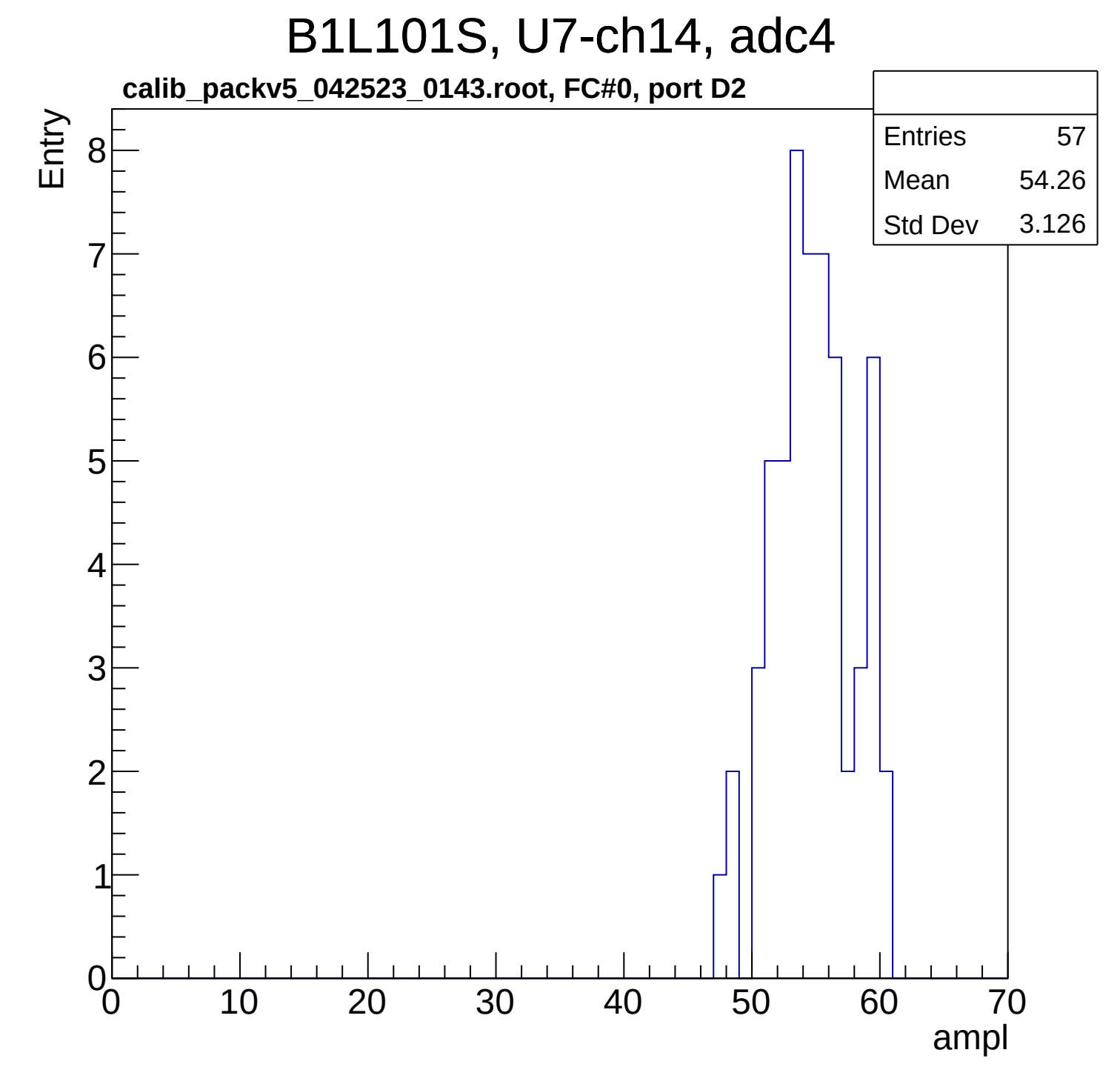
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch14, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 54.26
Std Dev 3.126
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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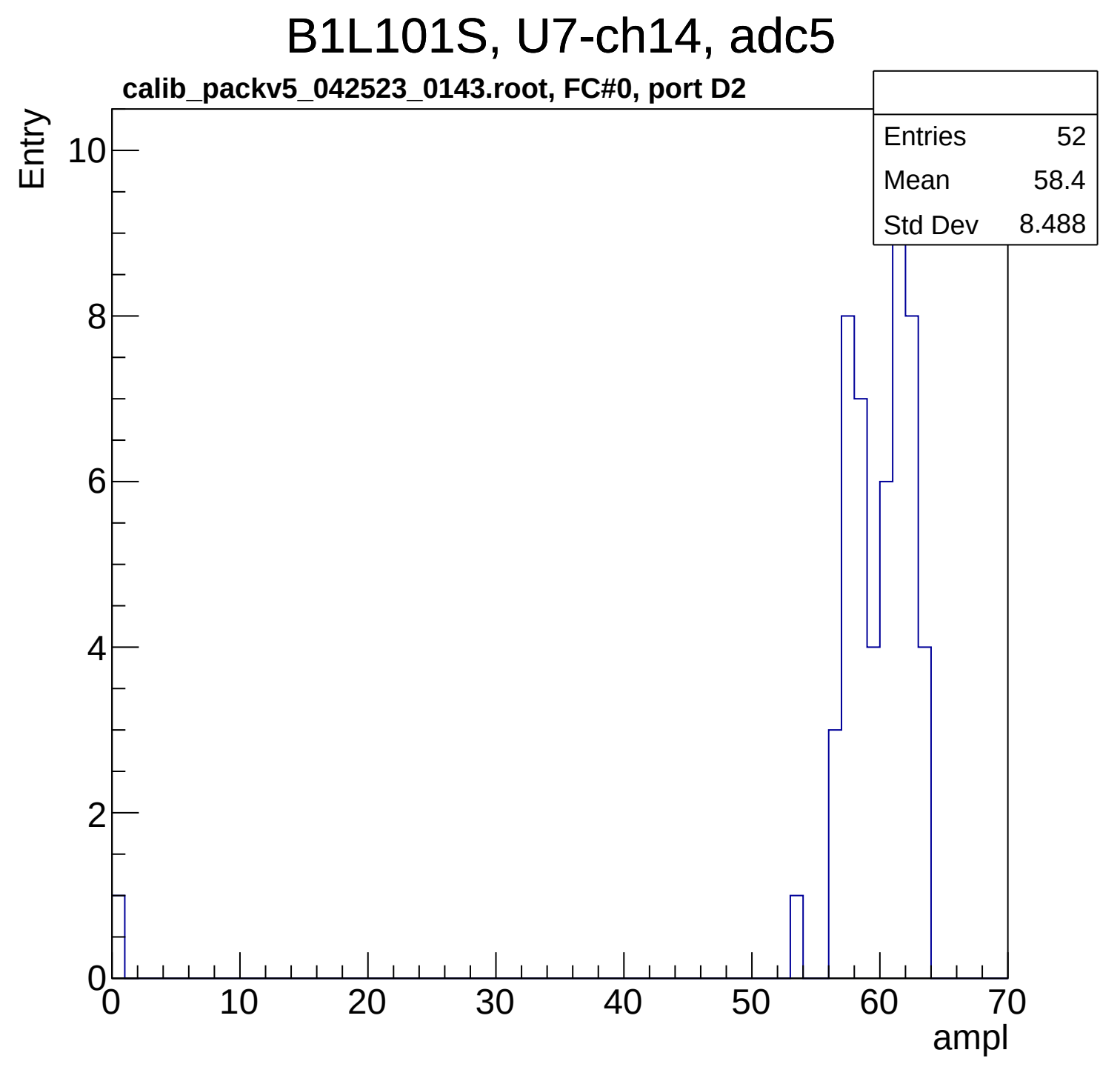
B1L101S, U7-ch14, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 58.4
Std Dev 8.488
Entry
ampl
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2
4
6
8
10
0
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20
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40
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60
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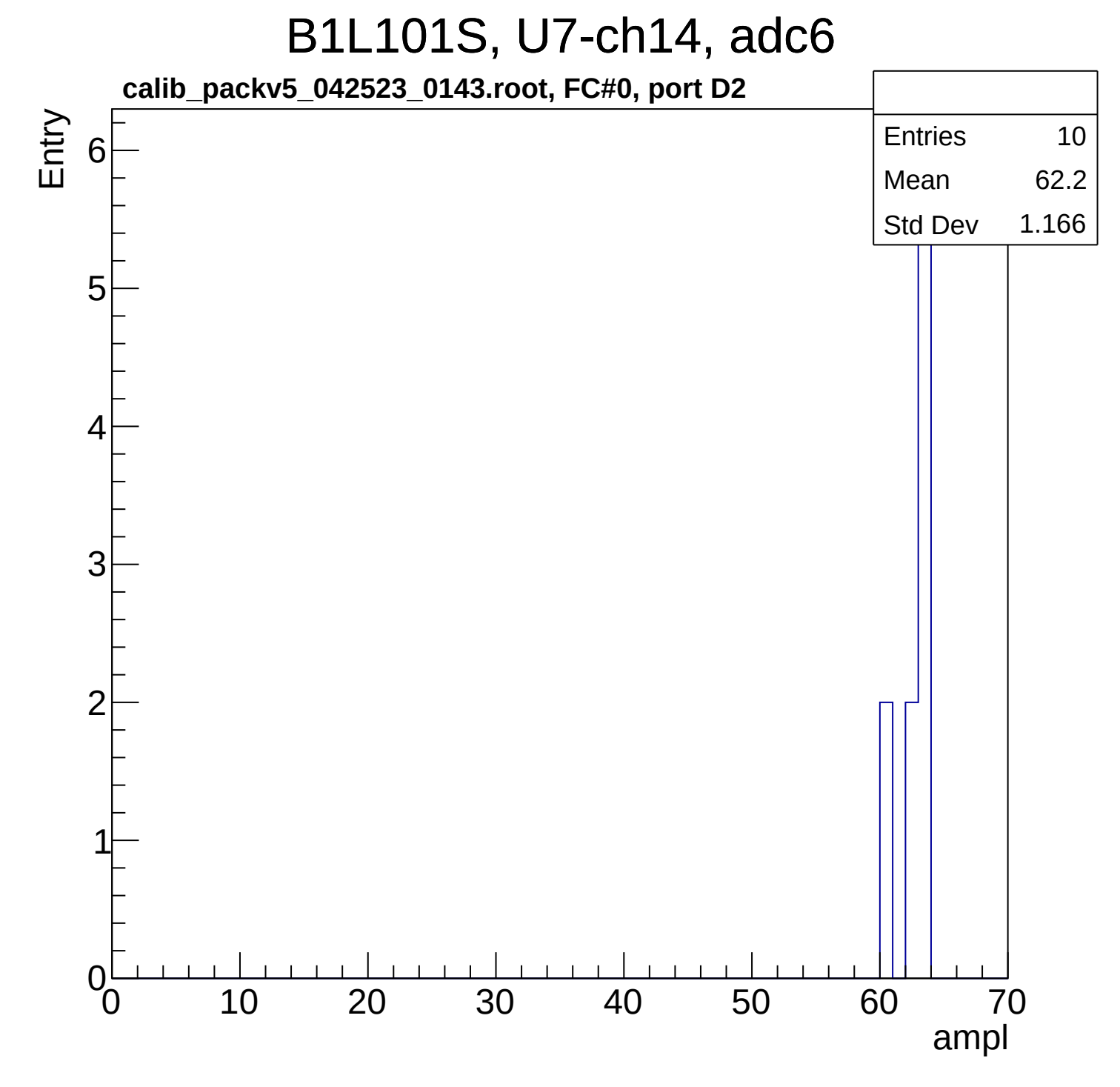
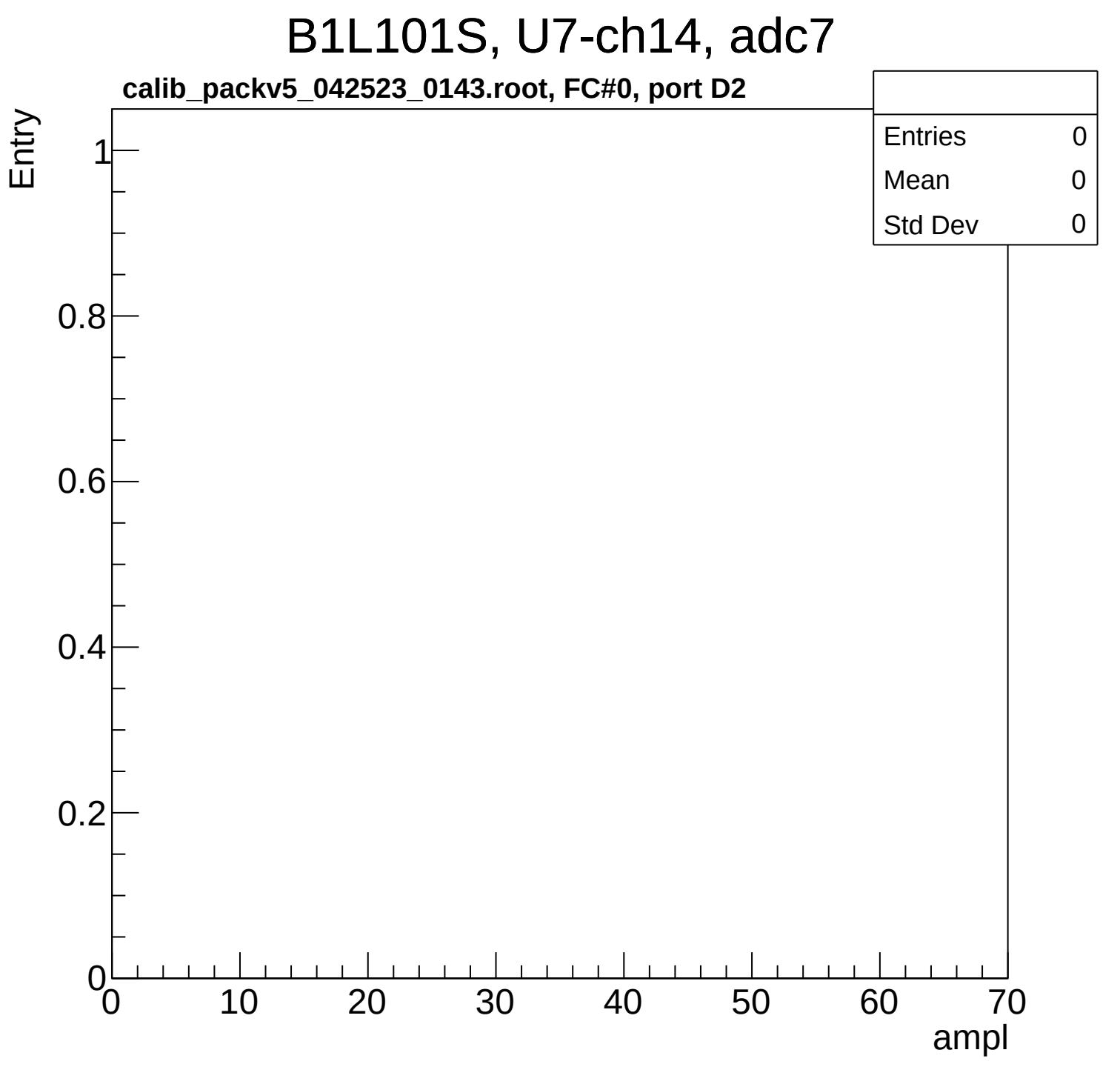

B1L101S, U7-ch14, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 62.2
Std Dev 1.166
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L101S, U7-ch14, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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0.6
0.4
0.2
0
0
10
20
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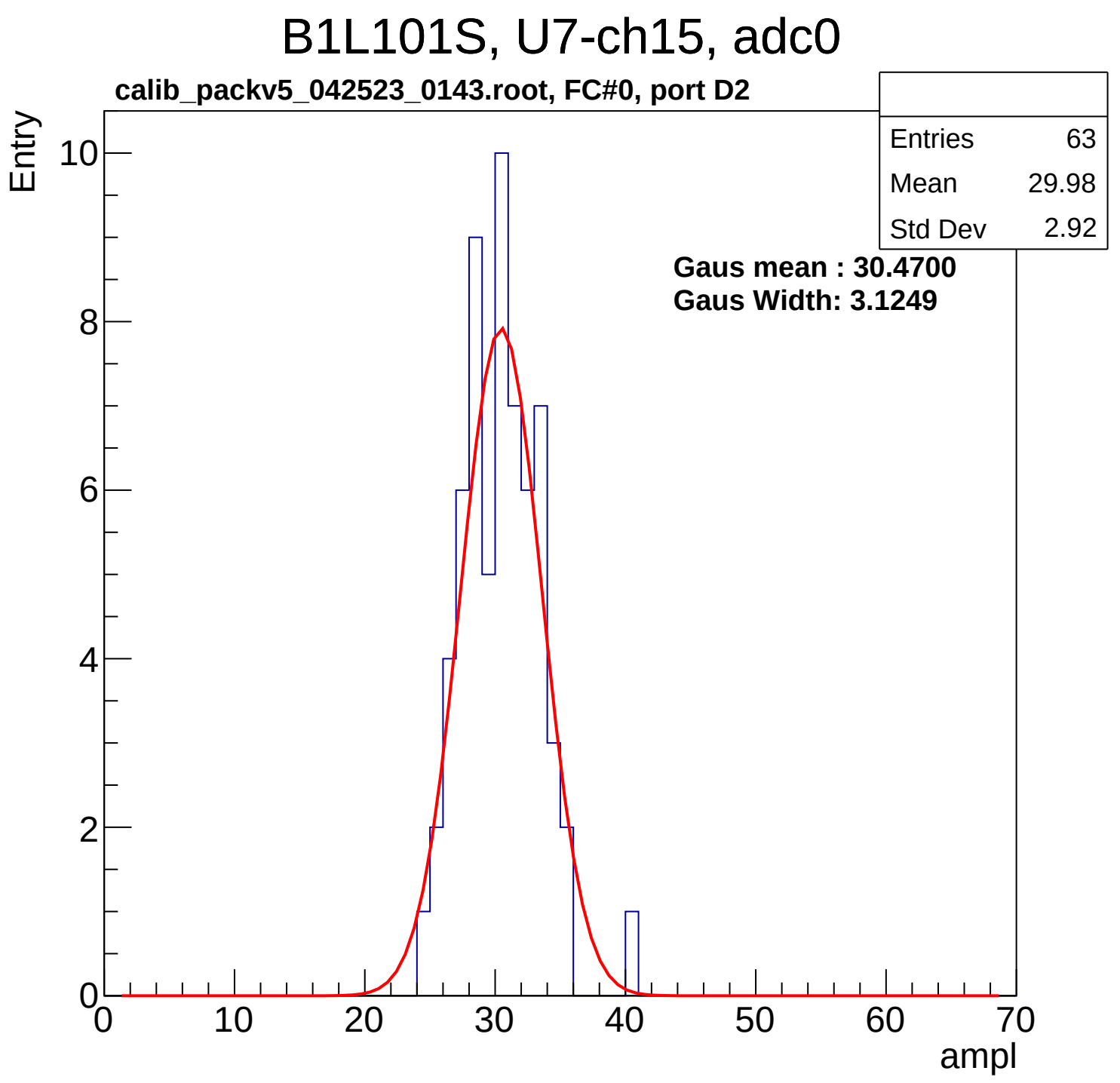
40
50
60
70
ampl


B1L101S, U7-ch15, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 29.98
Std Dev 2.92
Gaus mean : 30.4700
Gaus Width: 3.1249
Entry
ampl
0
2
4
6
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0
10
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60
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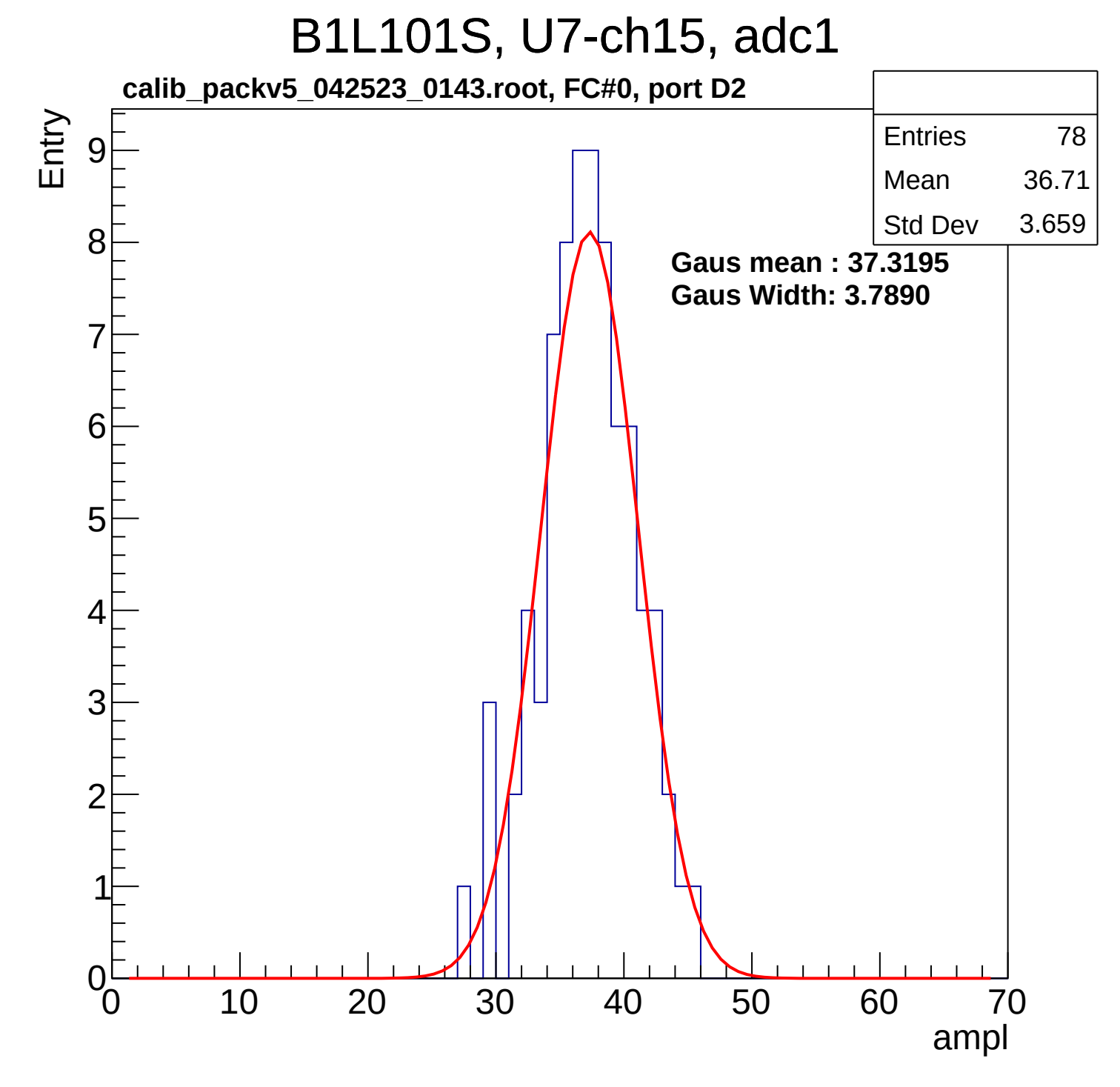
B1L101S, U7-ch15, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 36.71
Std Dev 3.659
Gaus mean : 37.3195
Gaus Width: 3.7890
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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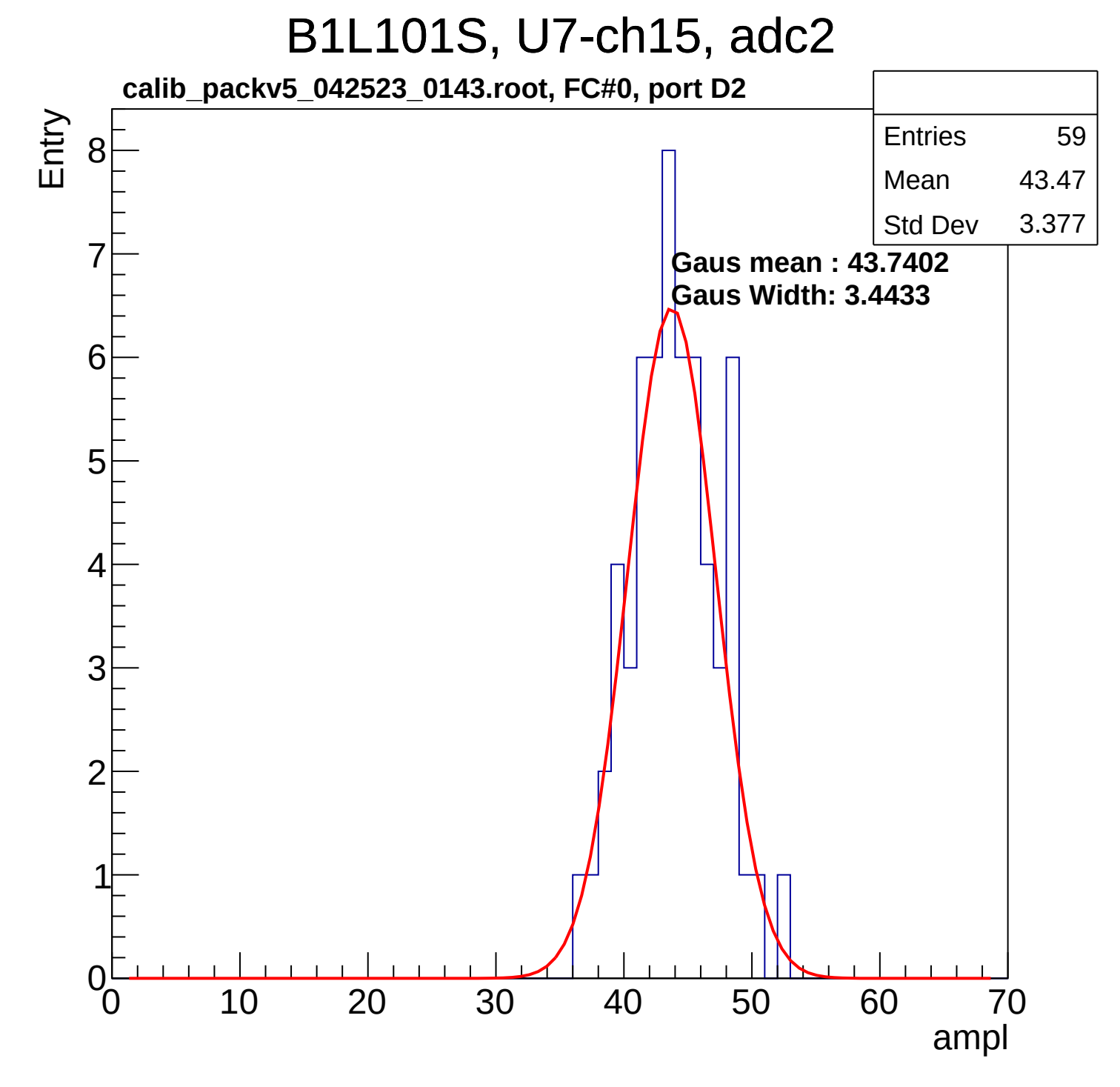
B1L101S, U7-ch15, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 43.47
Std Dev 3.377
Gaus mean : 43.7402
Gaus Width: 3.4433
Entry
ampl
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1
2
3
4
5
6
7
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0
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40
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60
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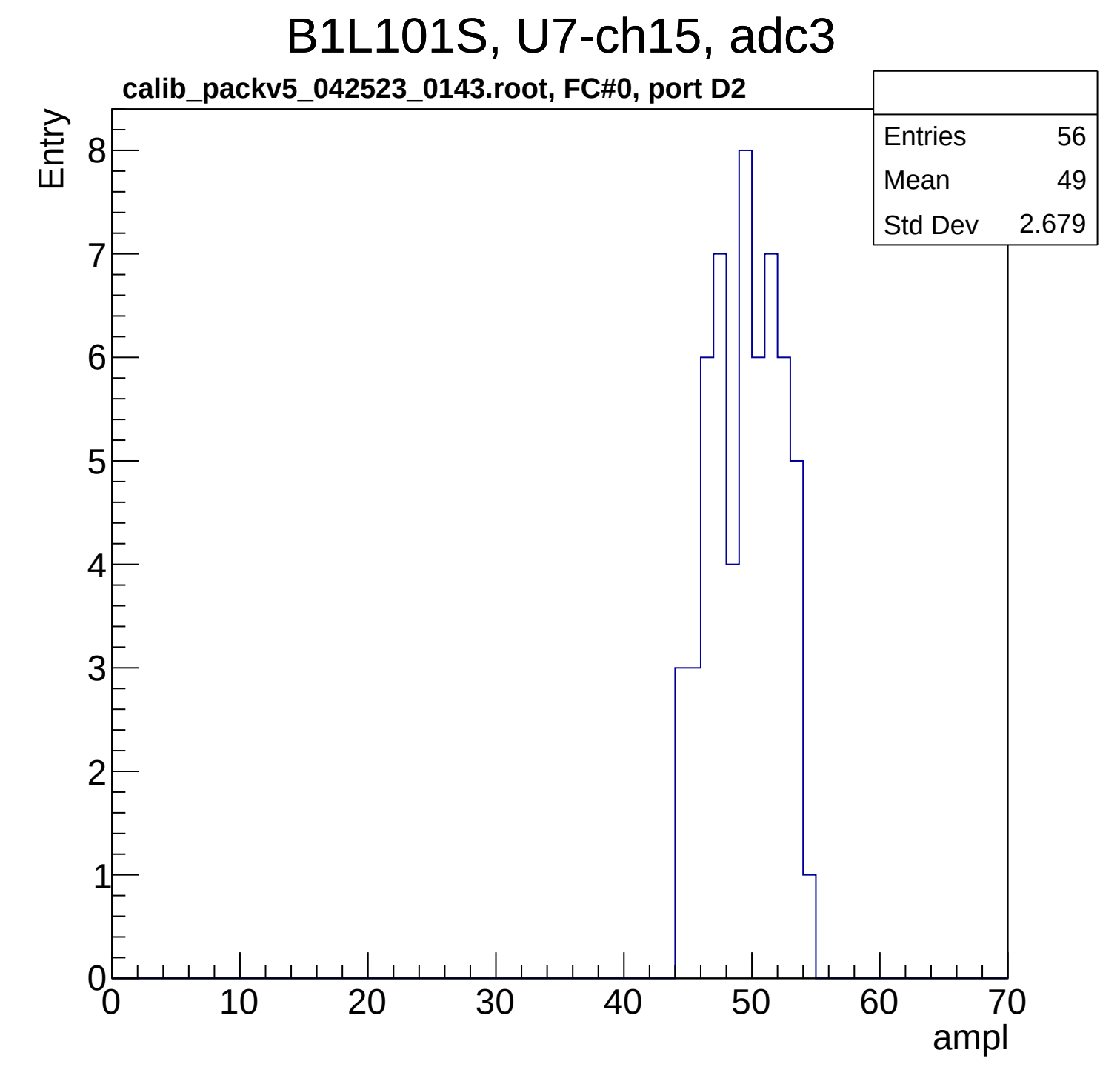
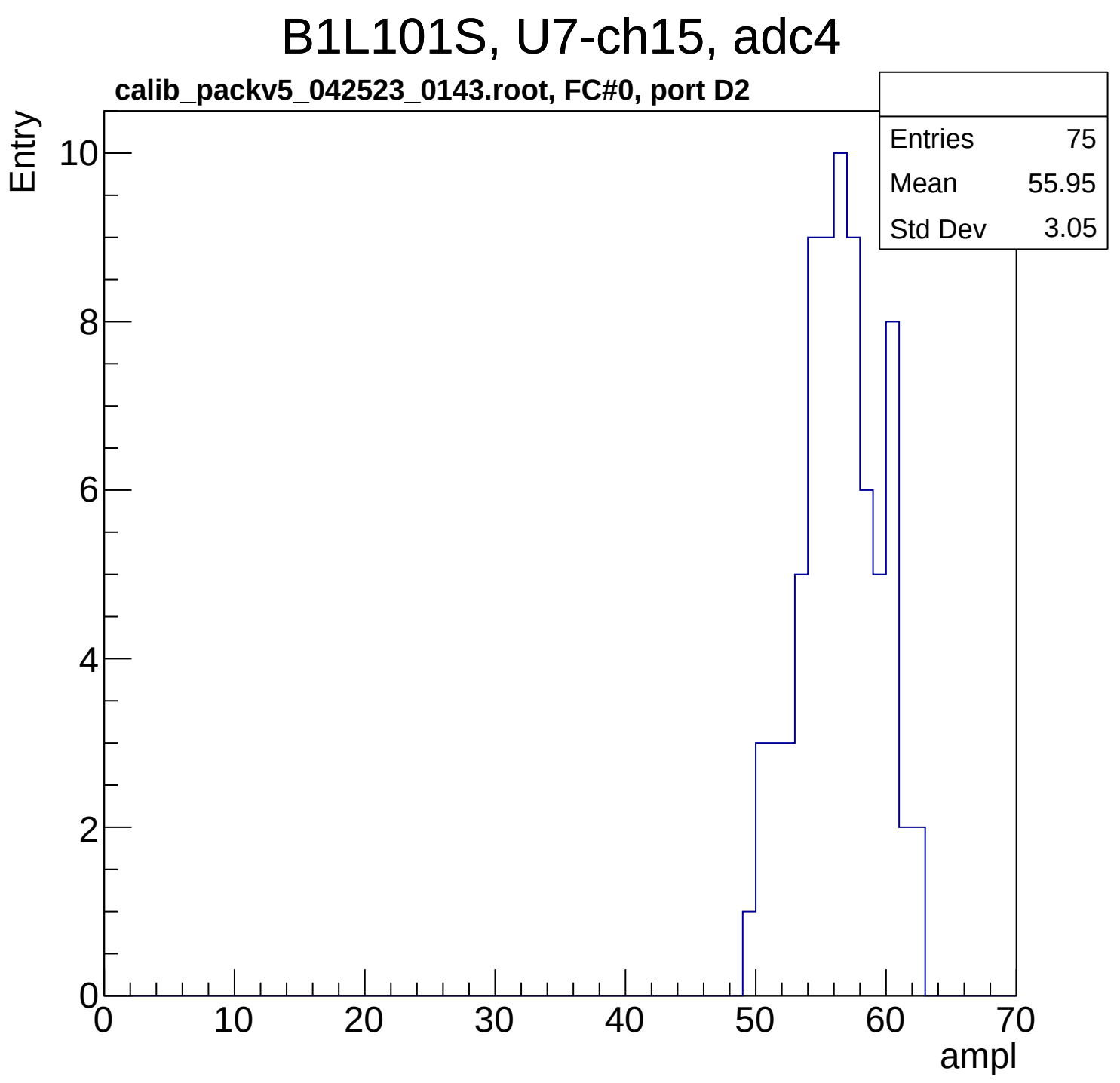
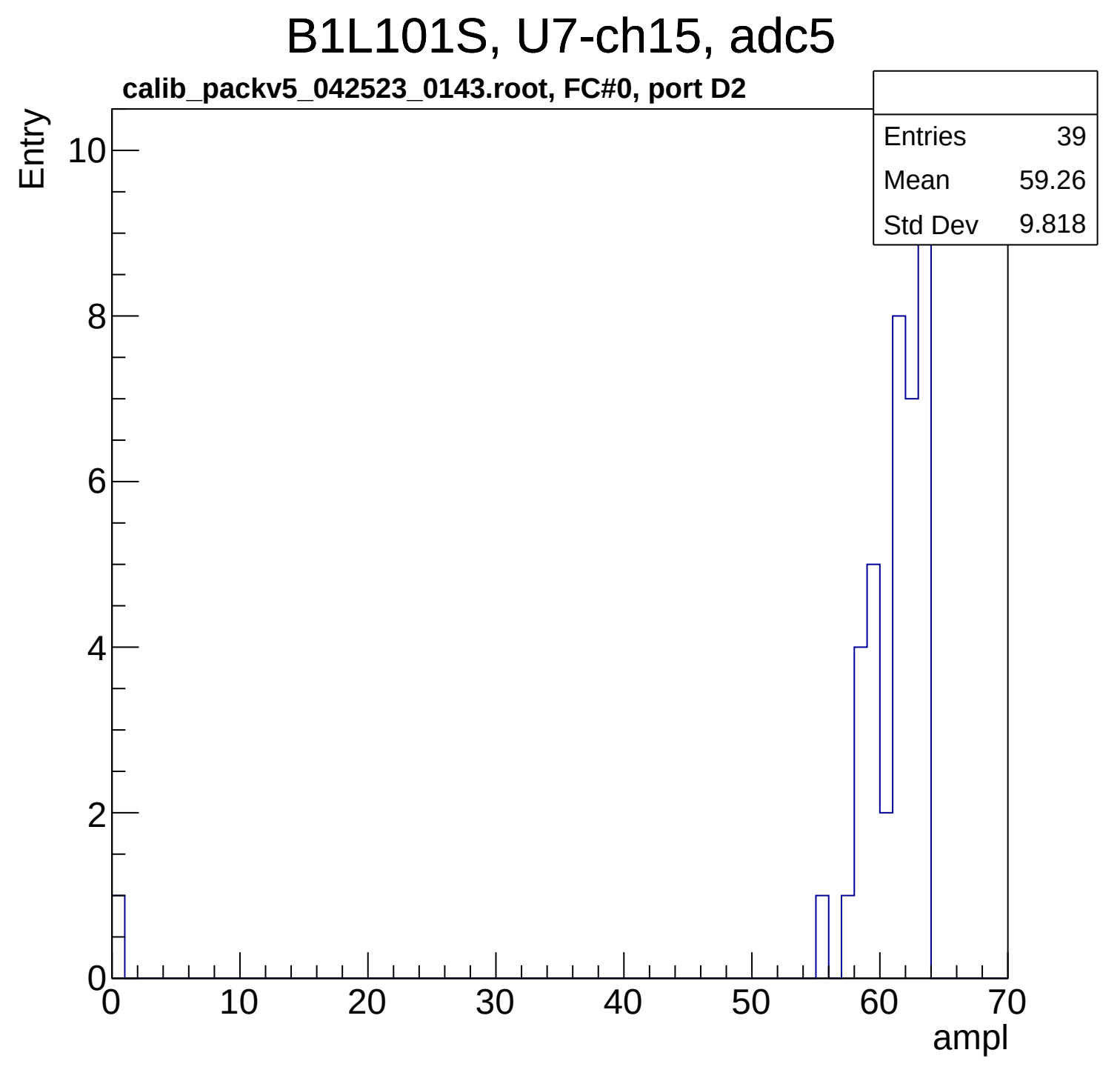

B1L101S, U7-ch15, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 49
Std Dev 2.679
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch15, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 55.95
Std Dev 3.05
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch15, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 39
Mean 59.26
Std Dev 9.818
Entry
ampl
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2
4
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8
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0
10
20
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40
50
60
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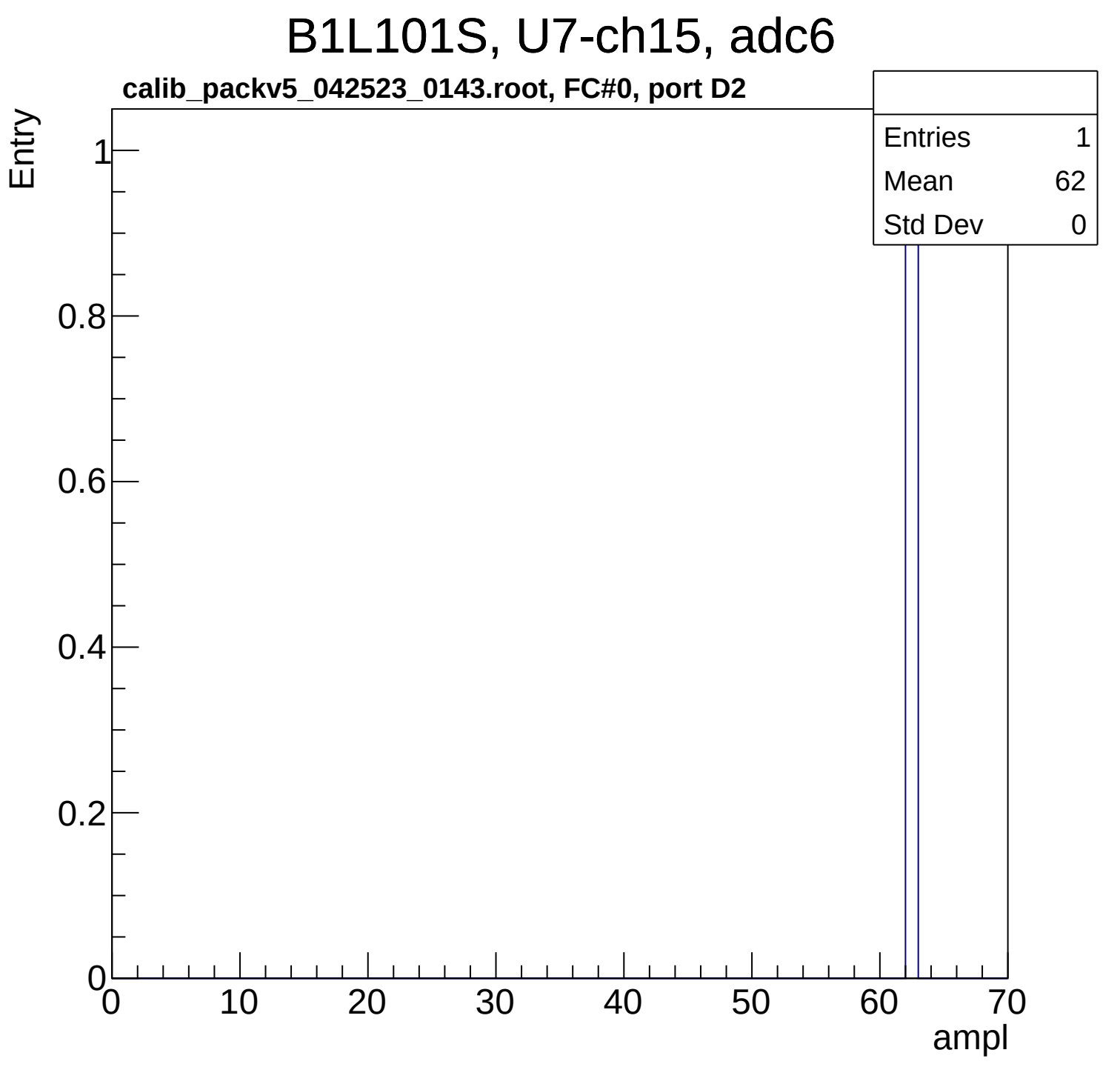
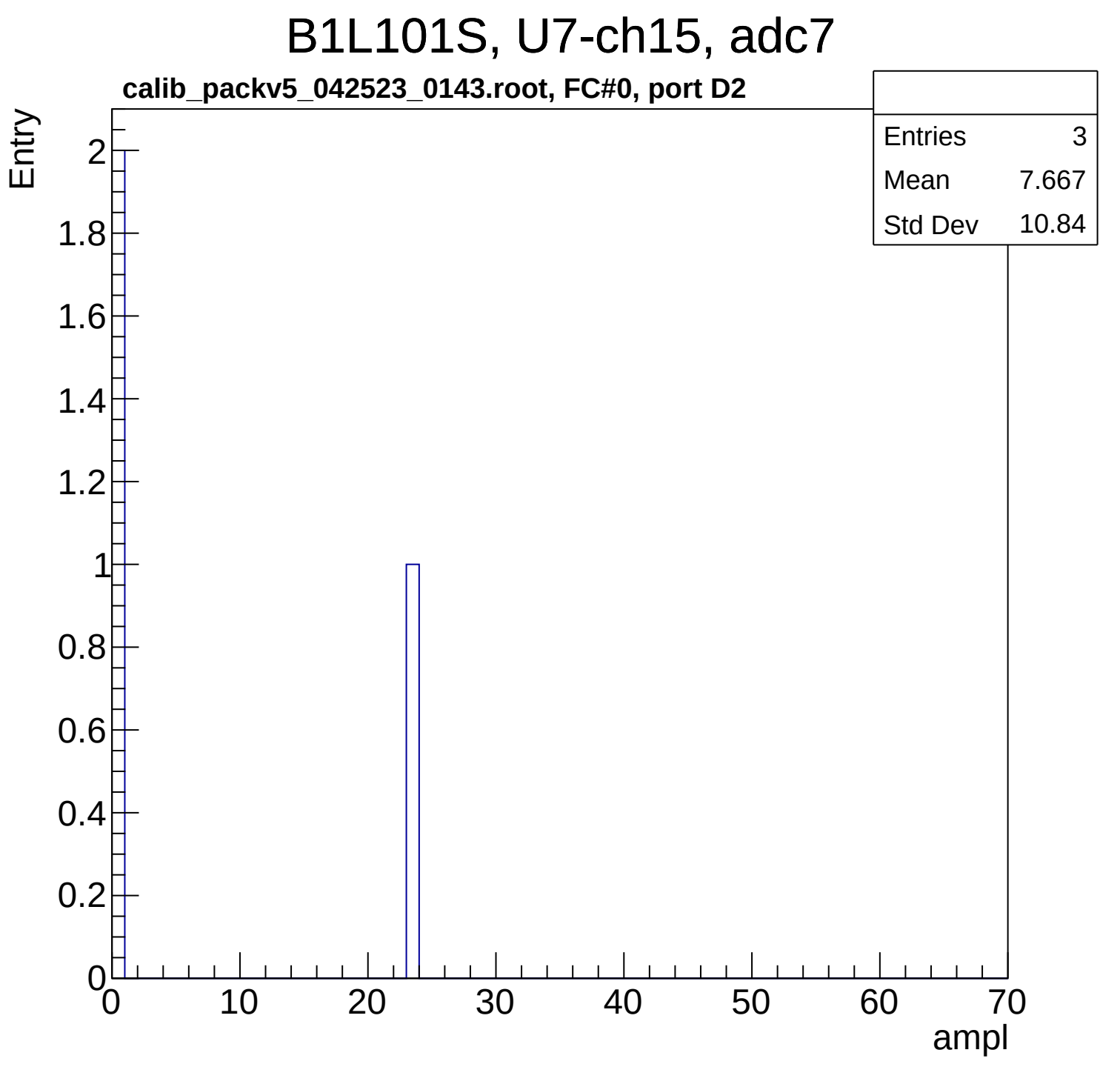
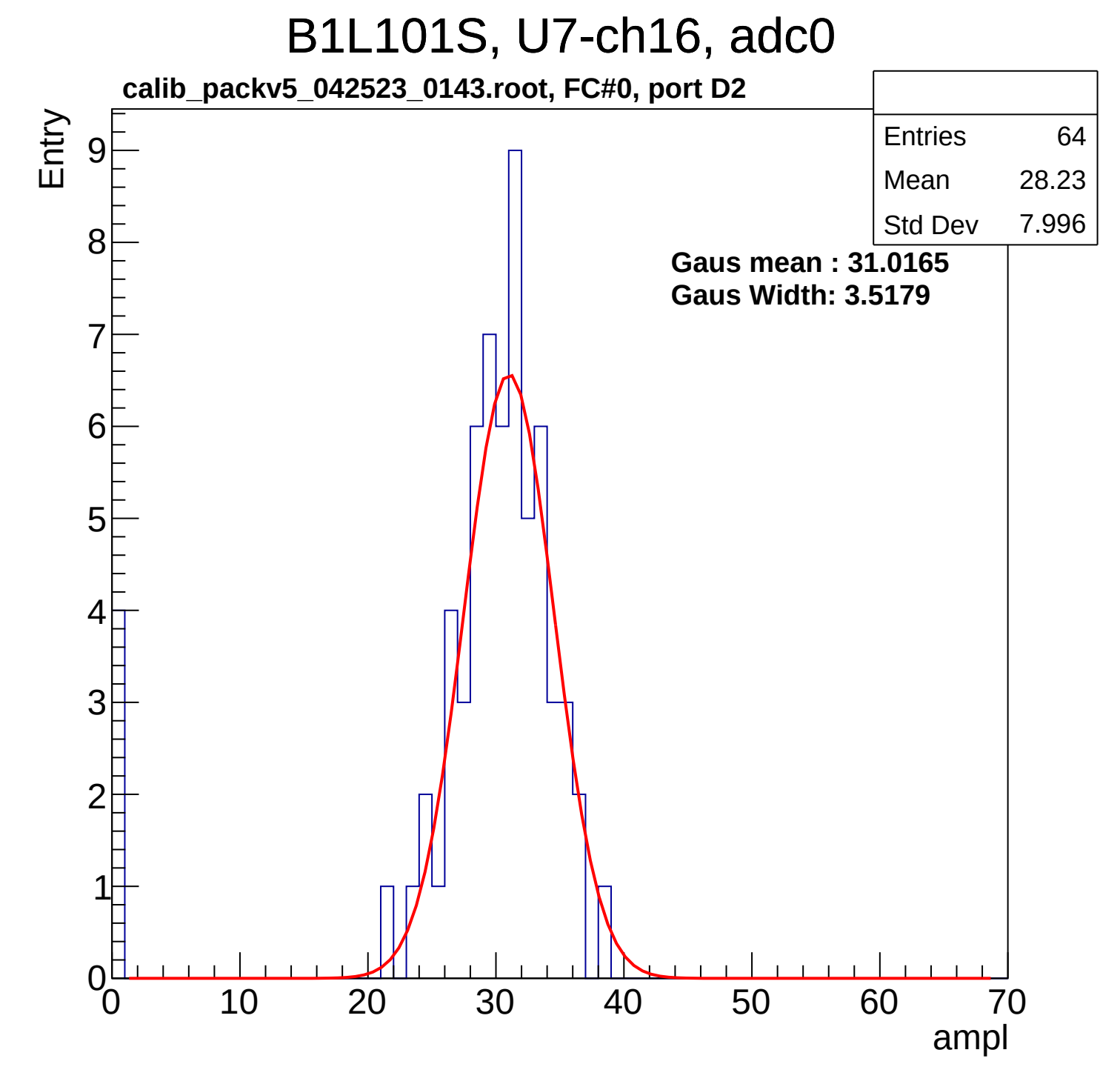
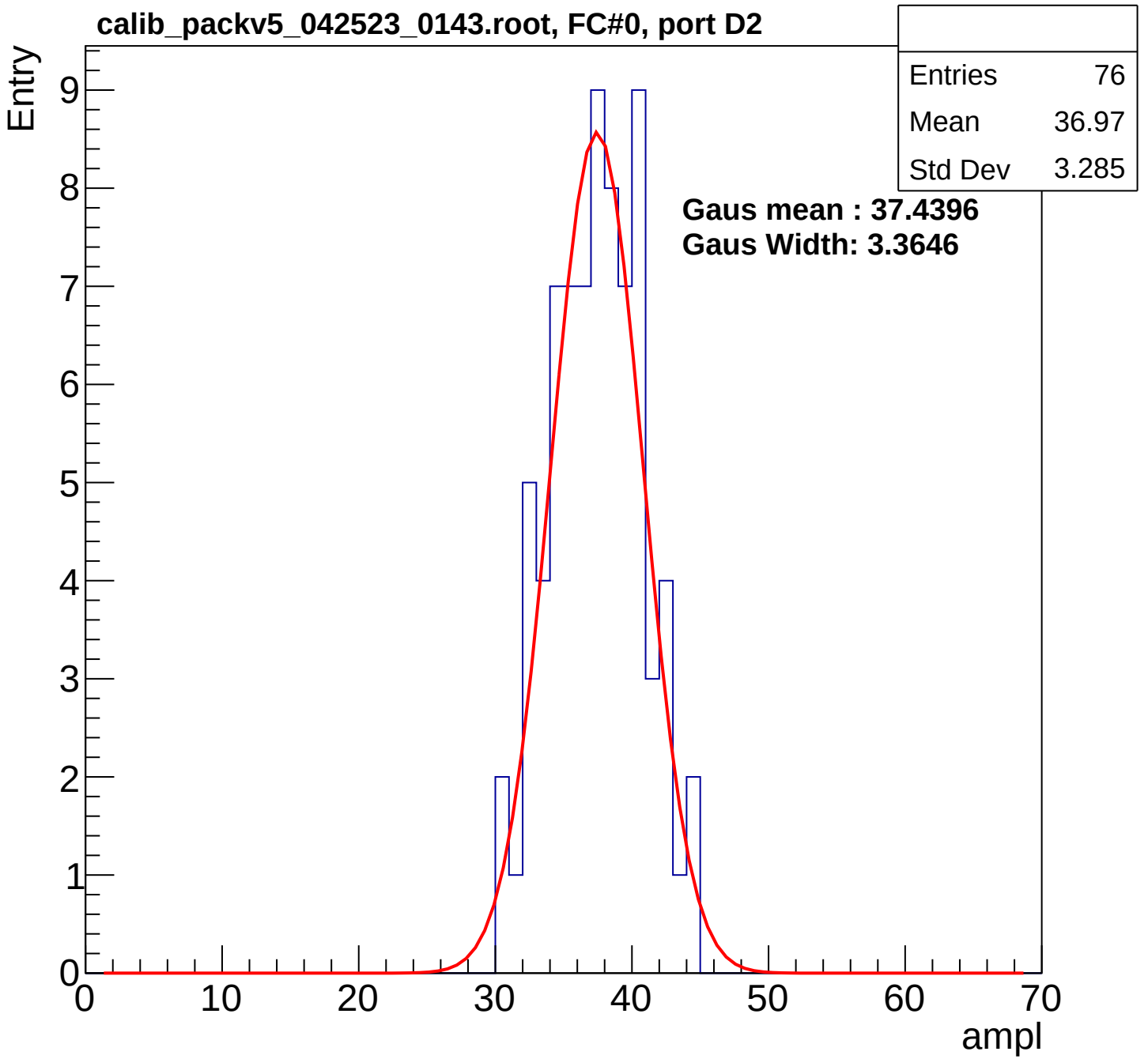
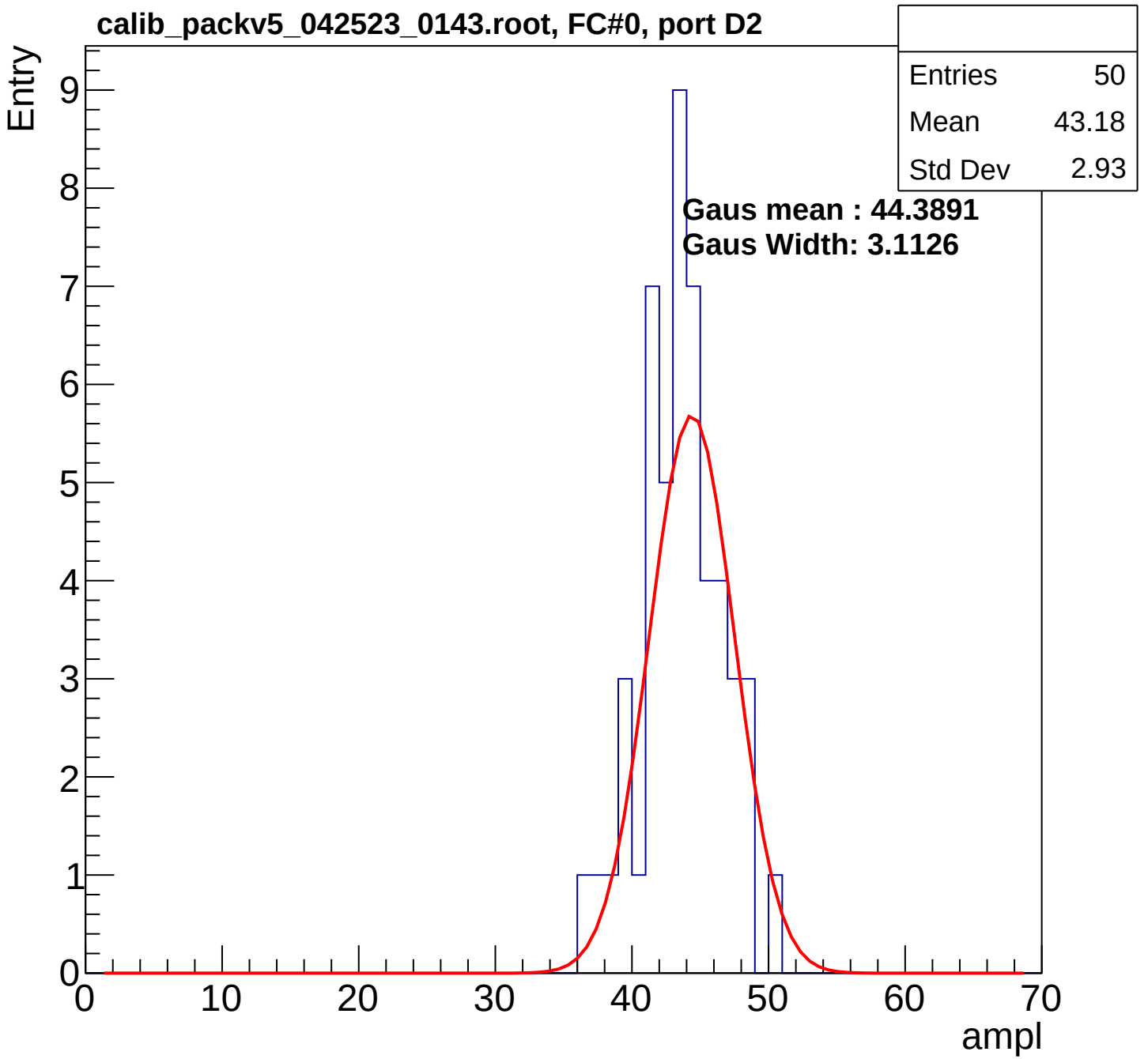
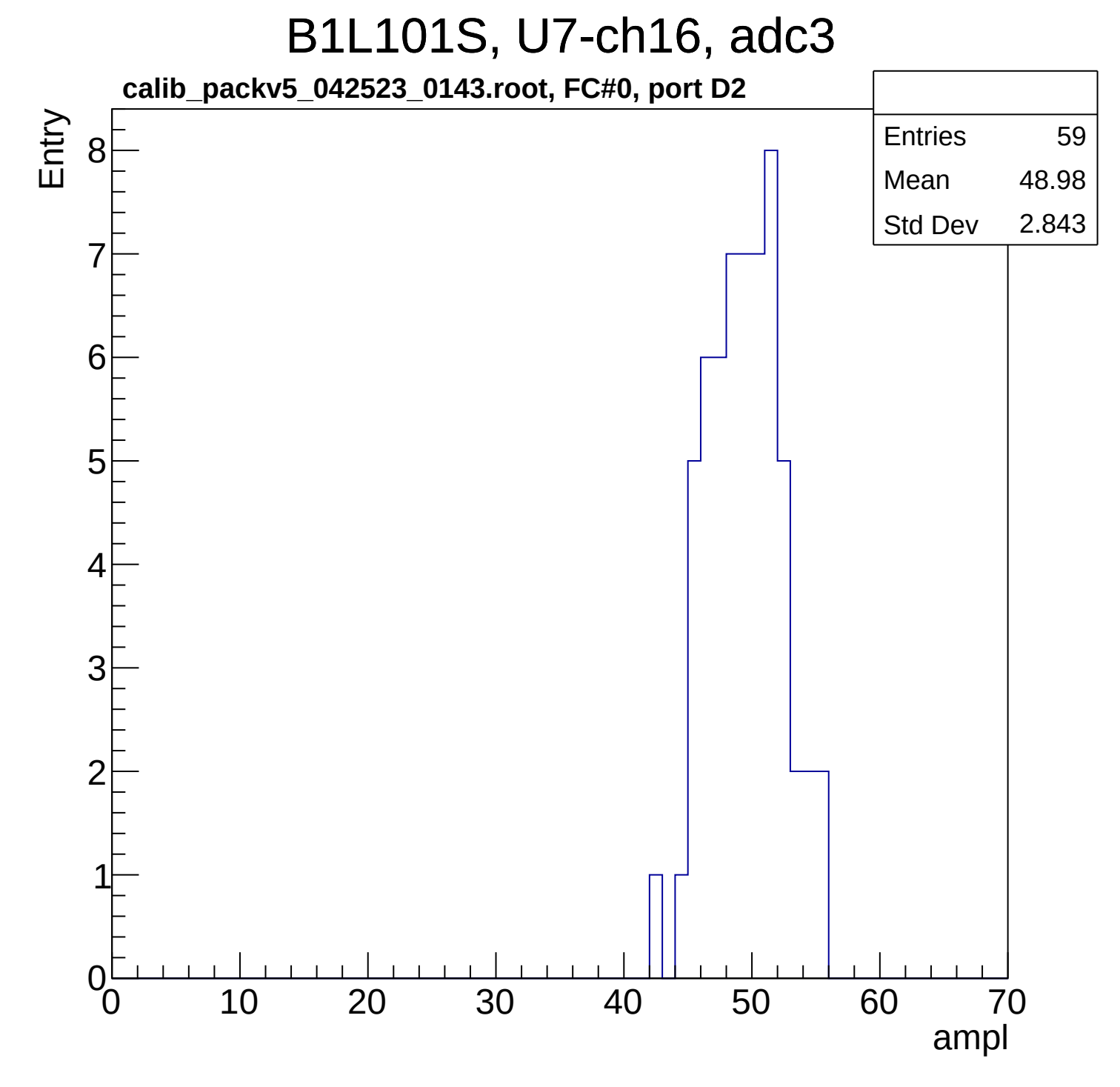

B1L101S, U7-ch15, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

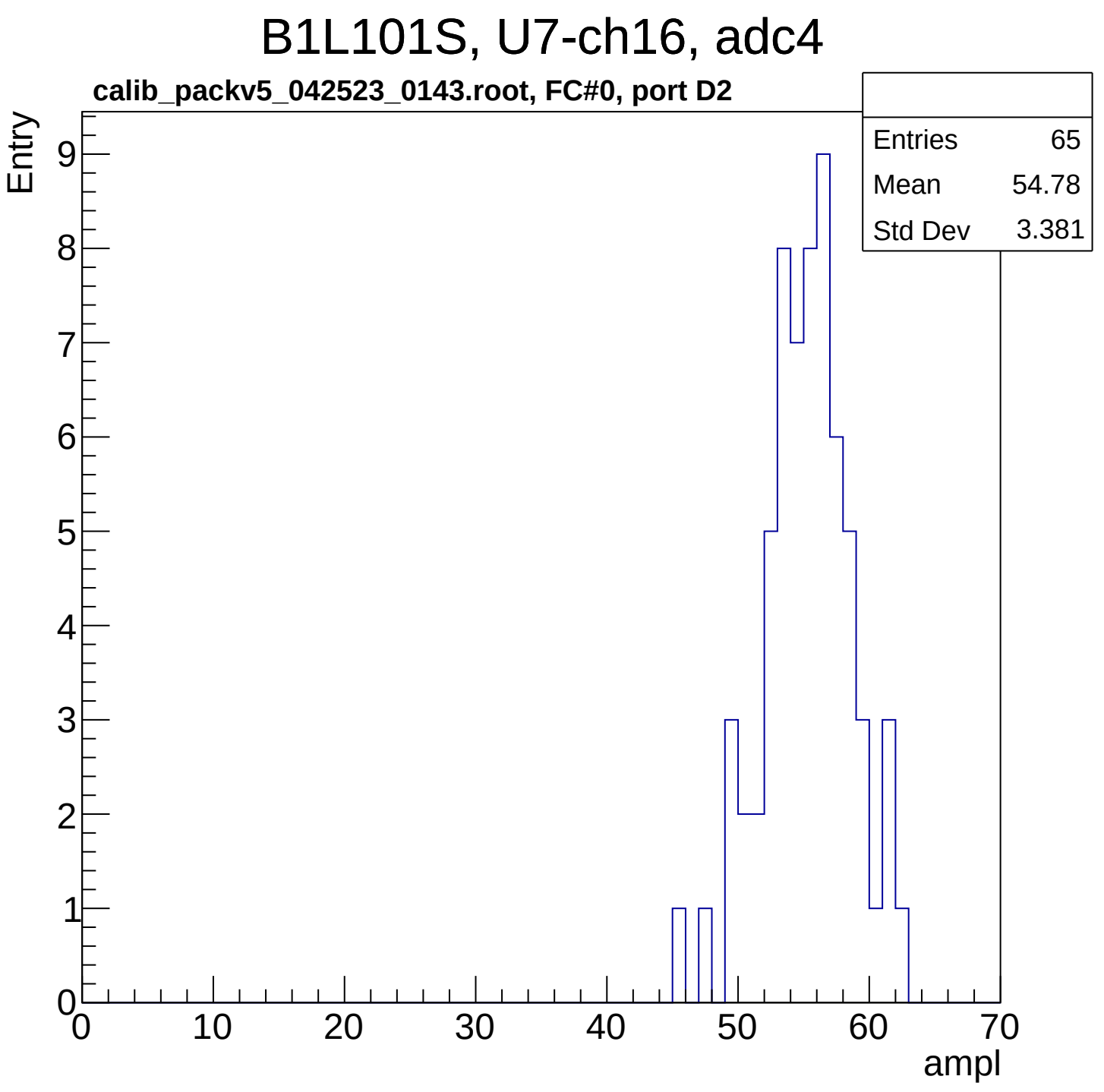

B1L101S, U7-ch15, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 7.667
Std Dev 10.84
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U7-ch16, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 28.23
Std Dev 7.996
Gaus mean : 31.0165
Gaus Width: 3.5179
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch16, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 36.97
Std Dev 3.285
Gaus mean : 37.4396
Gaus Width: 3.3646
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L101S, U7-ch16, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 43.18
Std Dev 2.93
Gaus mean : 44.3891
Gaus Width: 3.1126
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch16, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 48.98
Std Dev 2.843
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch16, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 54.78
Std Dev 3.381
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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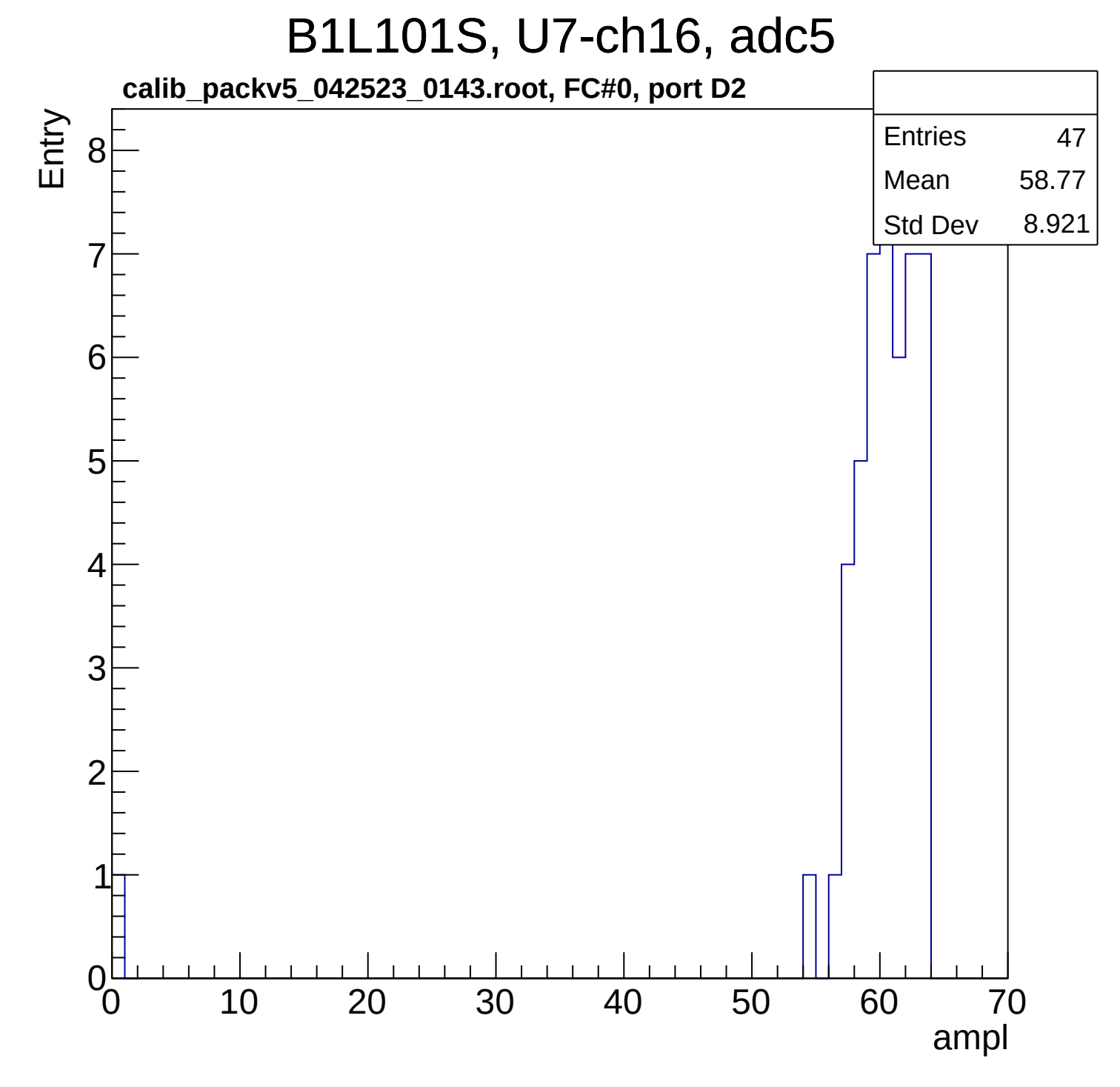
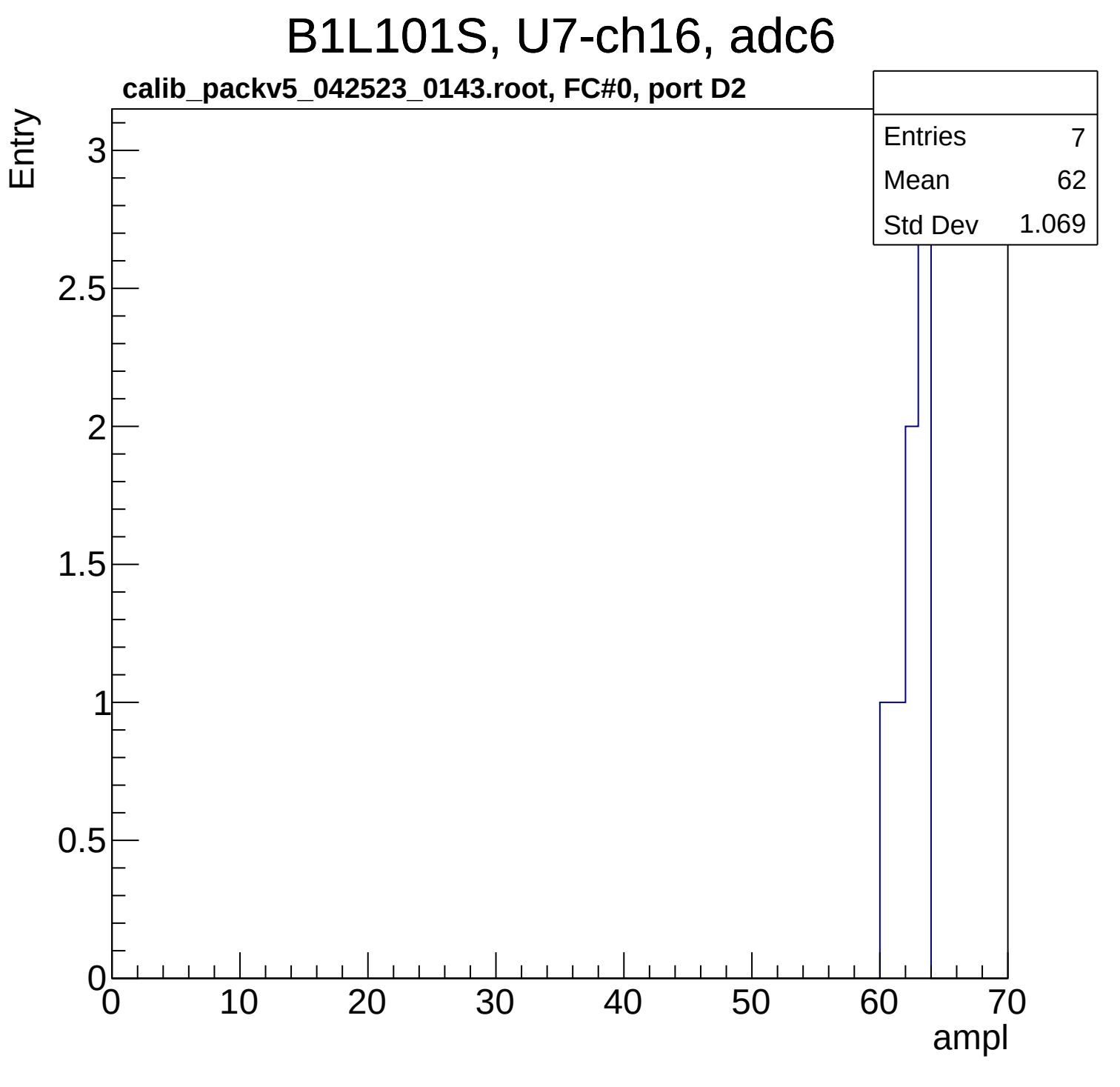

B1L101S, U7-ch16, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 58.77
Std Dev 8.921
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch16, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 62
Std Dev 1.069
Entry
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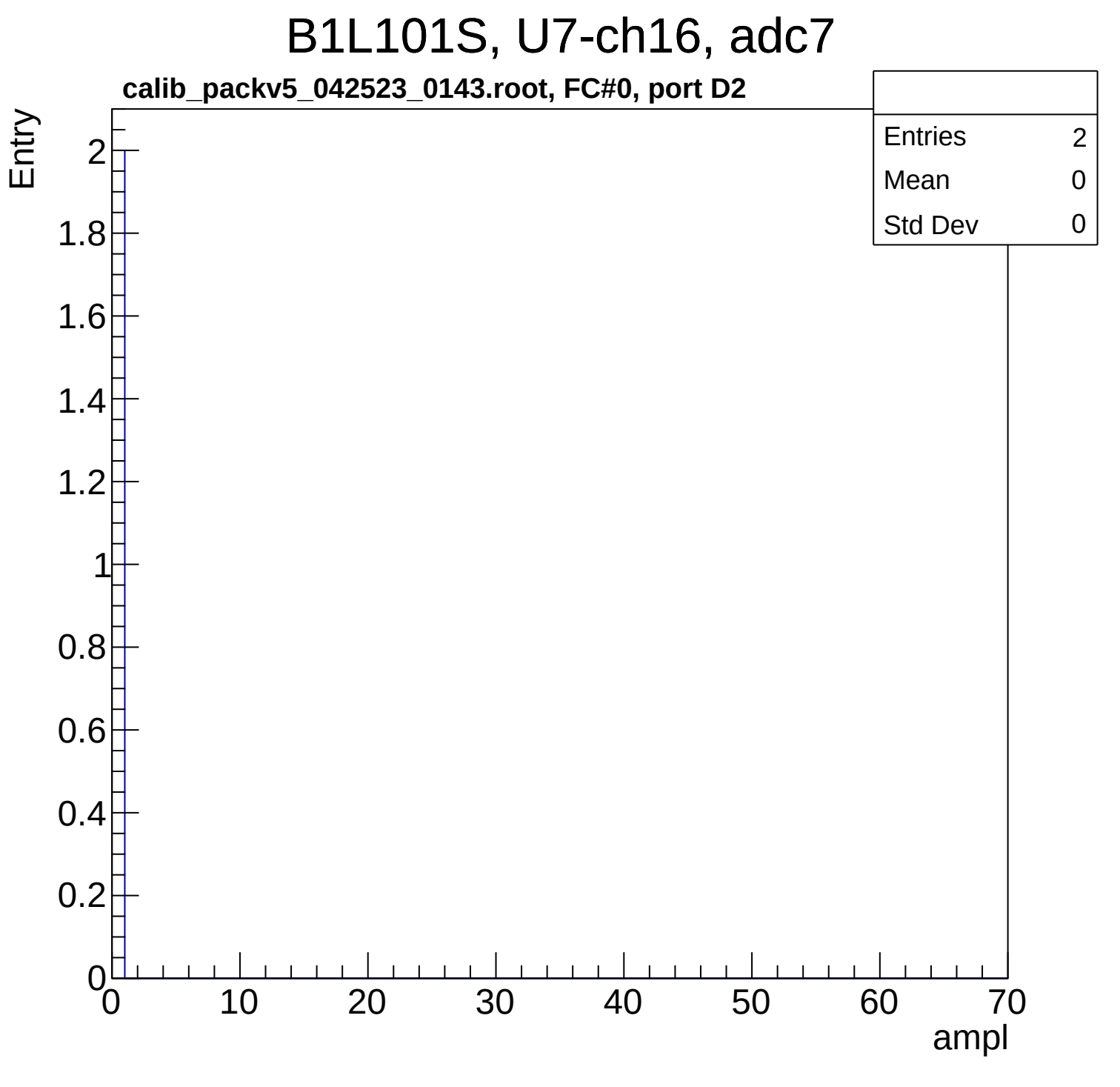
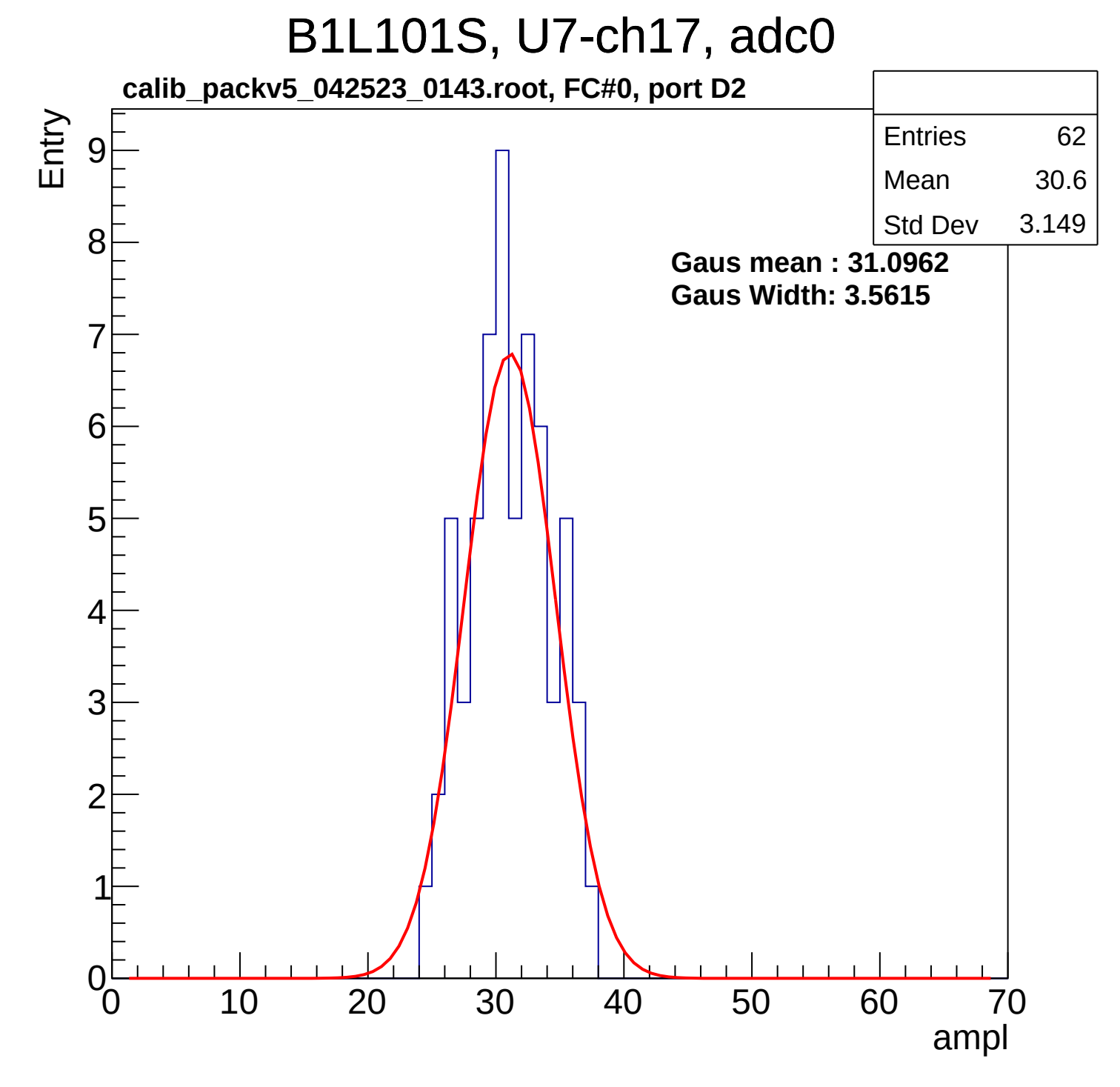
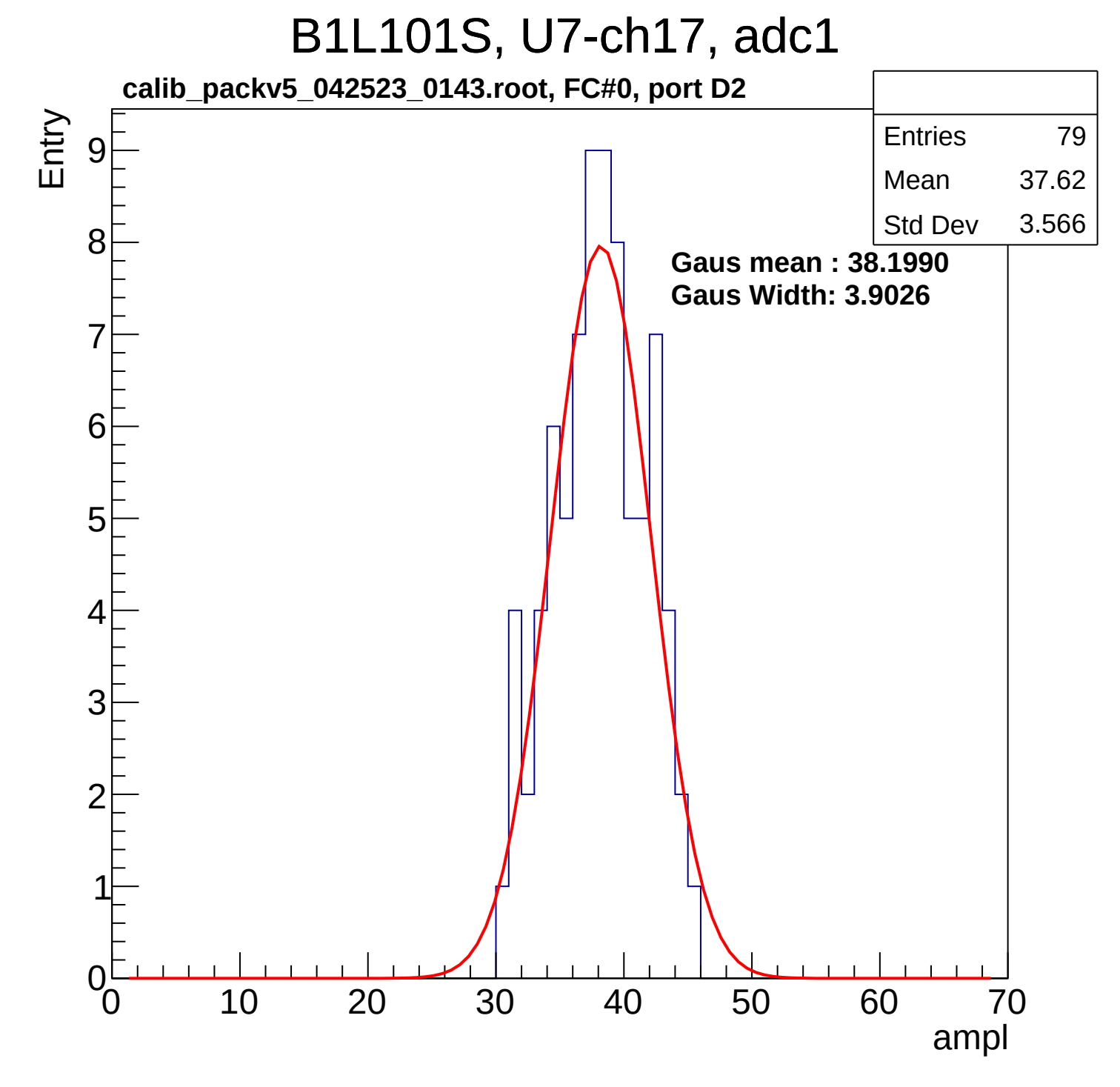
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch16, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U7-ch17, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 30.6
Std Dev 3.149
Gaus mean : 31.0962
Gaus Width: 3.5615
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch17, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 37.62
Std Dev 3.566
Gaus mean : 38.1990
Gaus Width: 3.9026
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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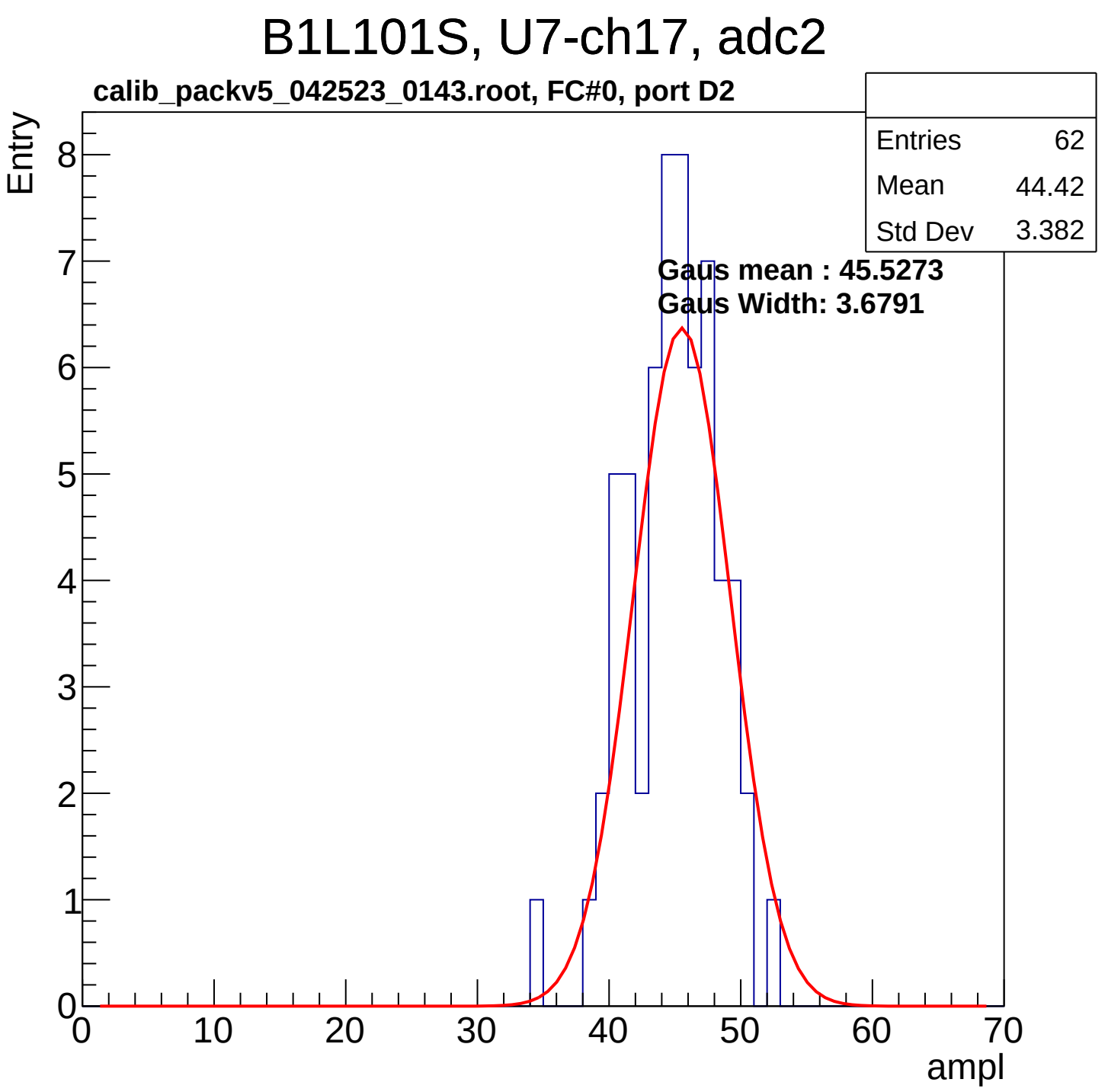
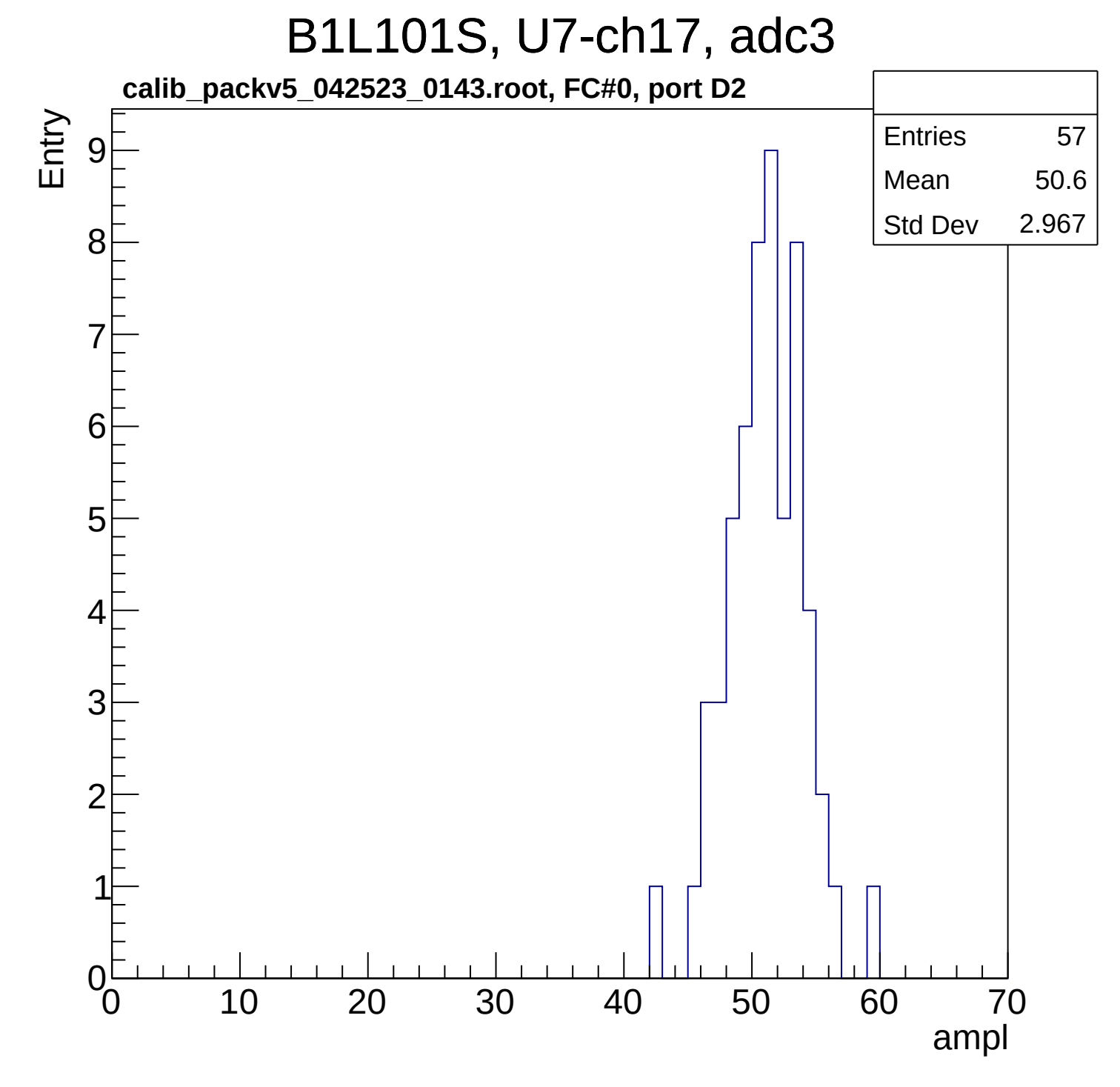

B1L101S, U7-ch17, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 44.42
Std Dev 3.382
Gaus mean : 45.5273
Gaus Width: 3.6791
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch17, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 50.6
Std Dev 2.967
Entry
ampl
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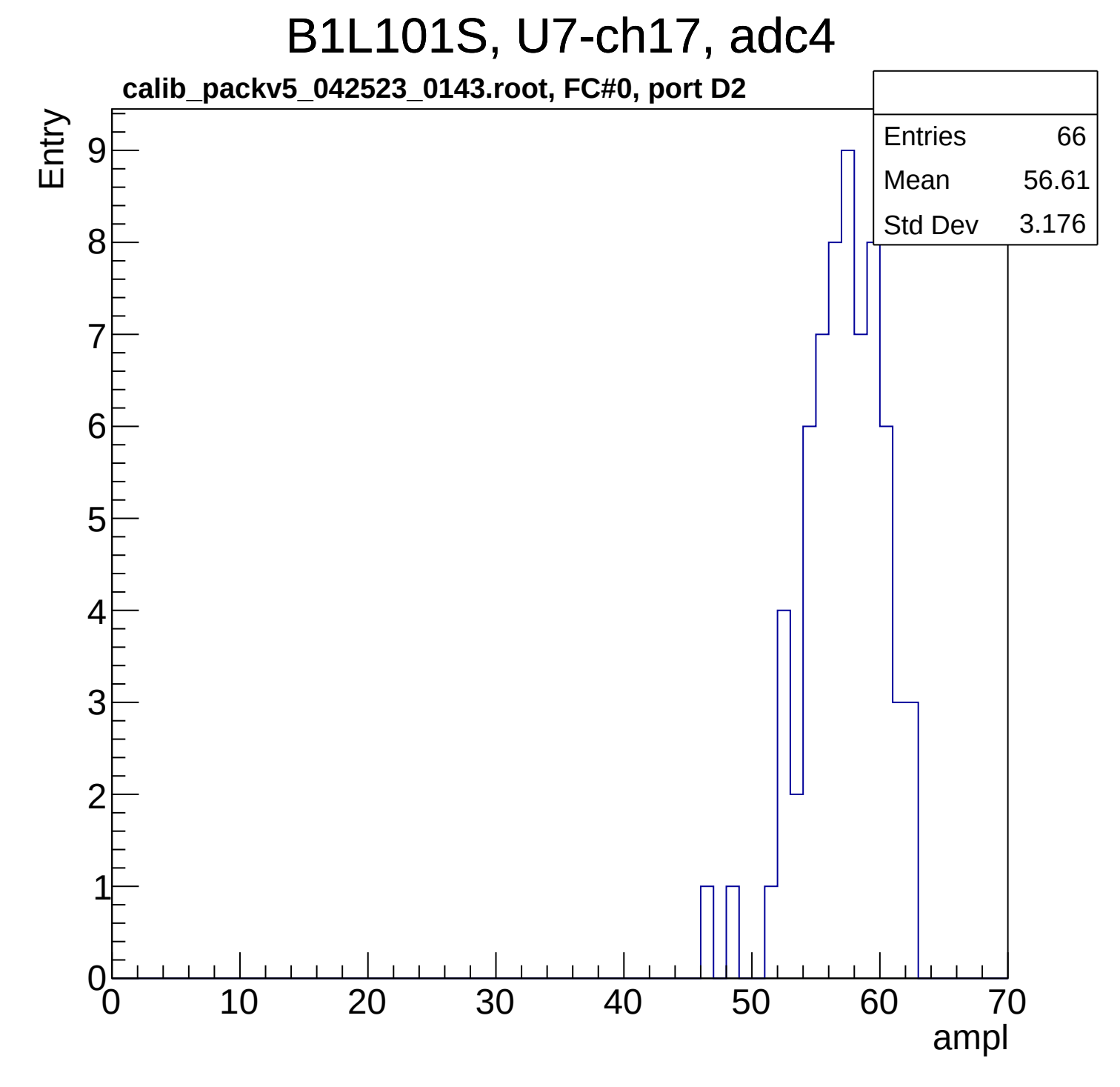
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch17, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 56.61
Std Dev 3.176
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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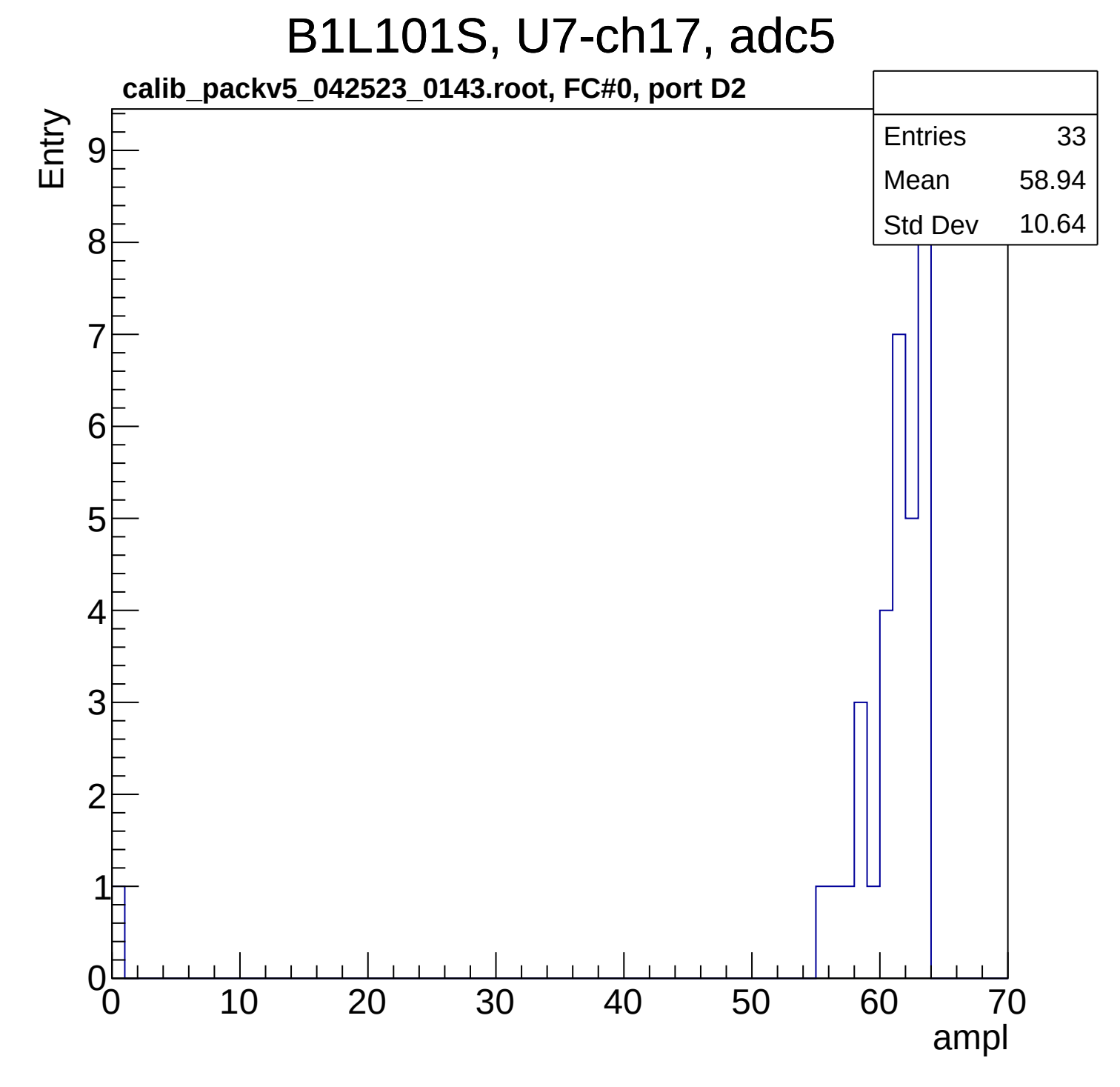
60
70


B1L101S, U7-ch17, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 33
Mean 58.94
Std Dev 10.64
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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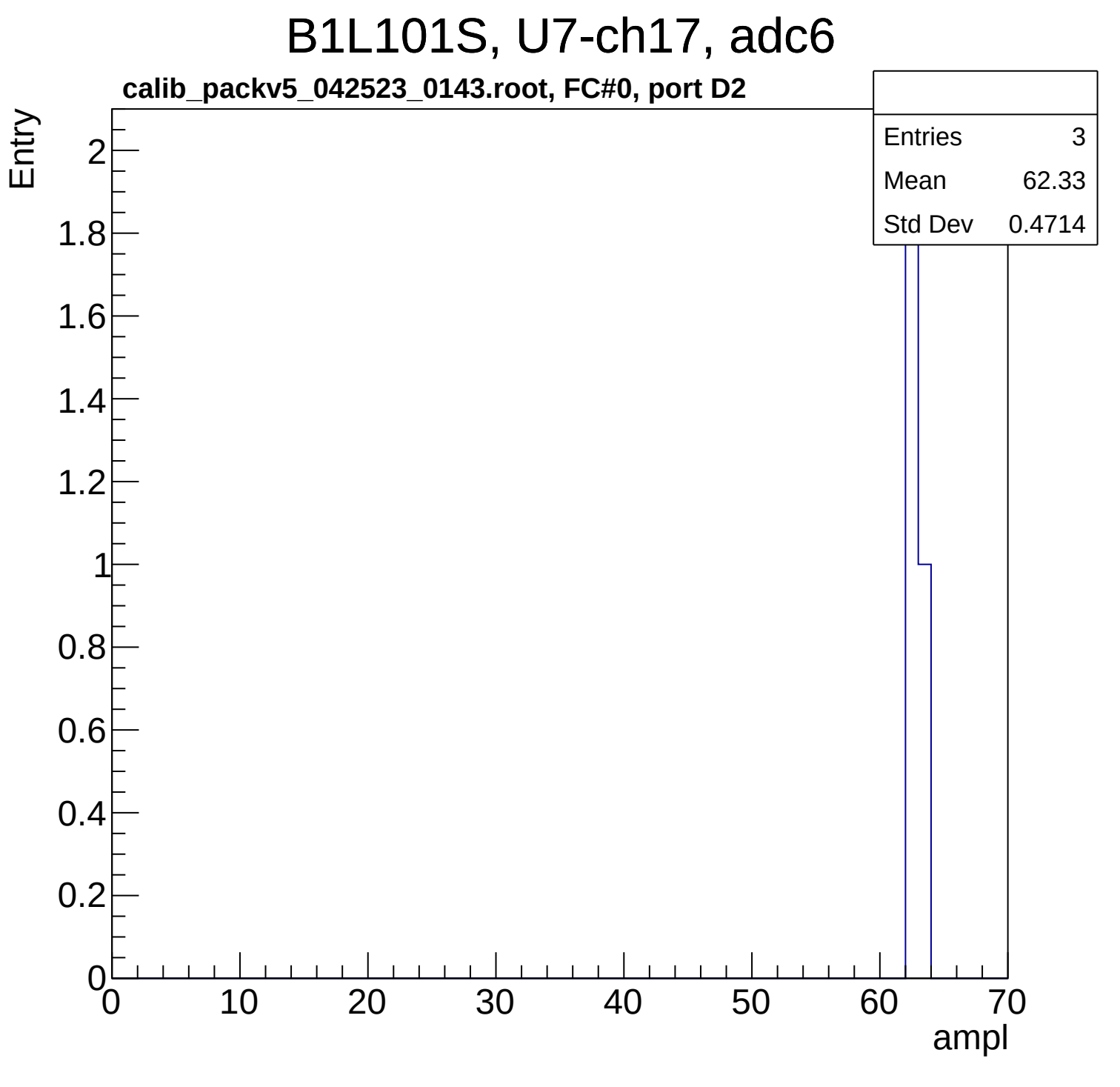
20
30
40
50
60
70


B1L101S, U7-ch17, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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60
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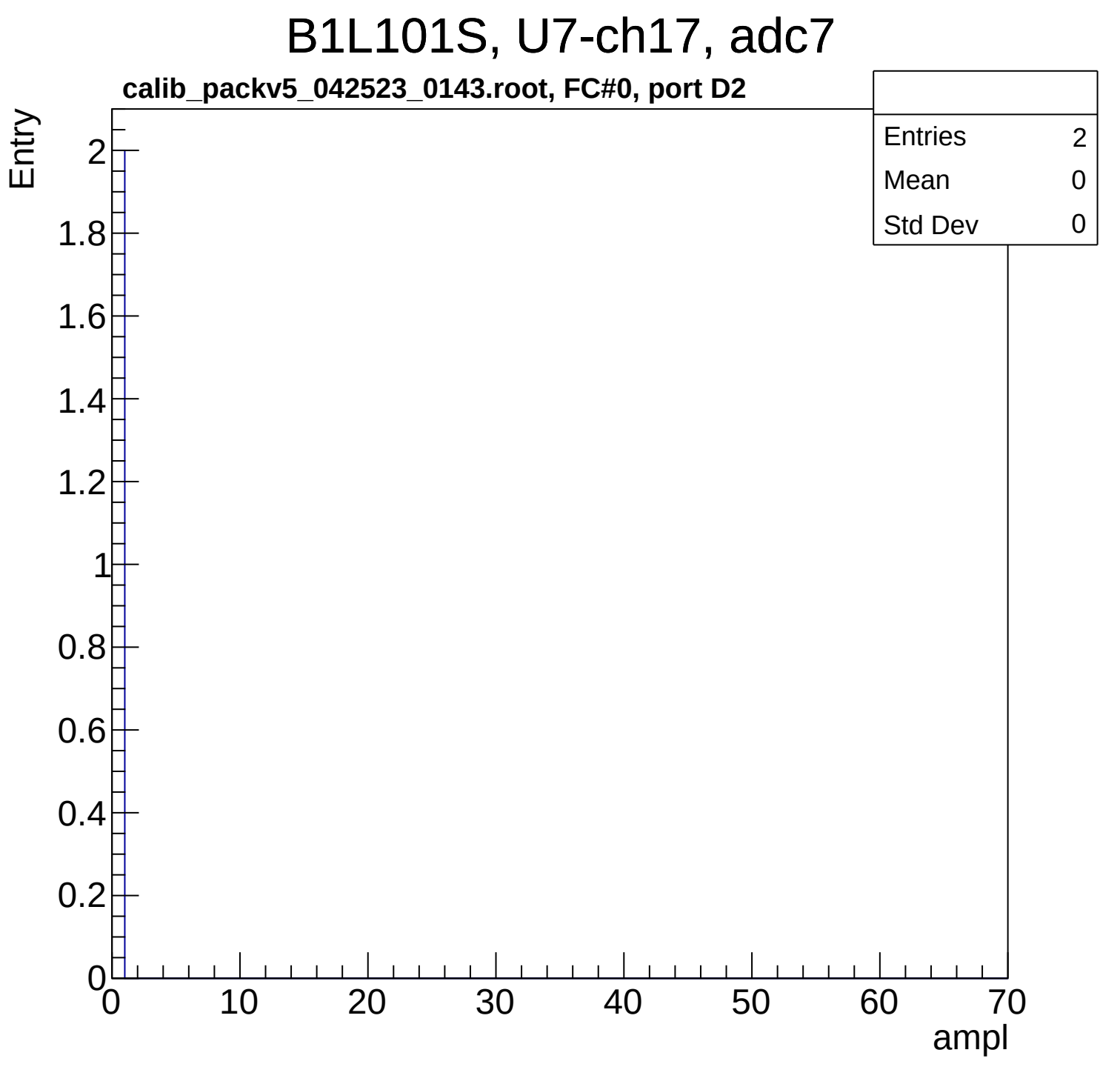
B1L101S, U7-ch17, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
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30
40
50
60
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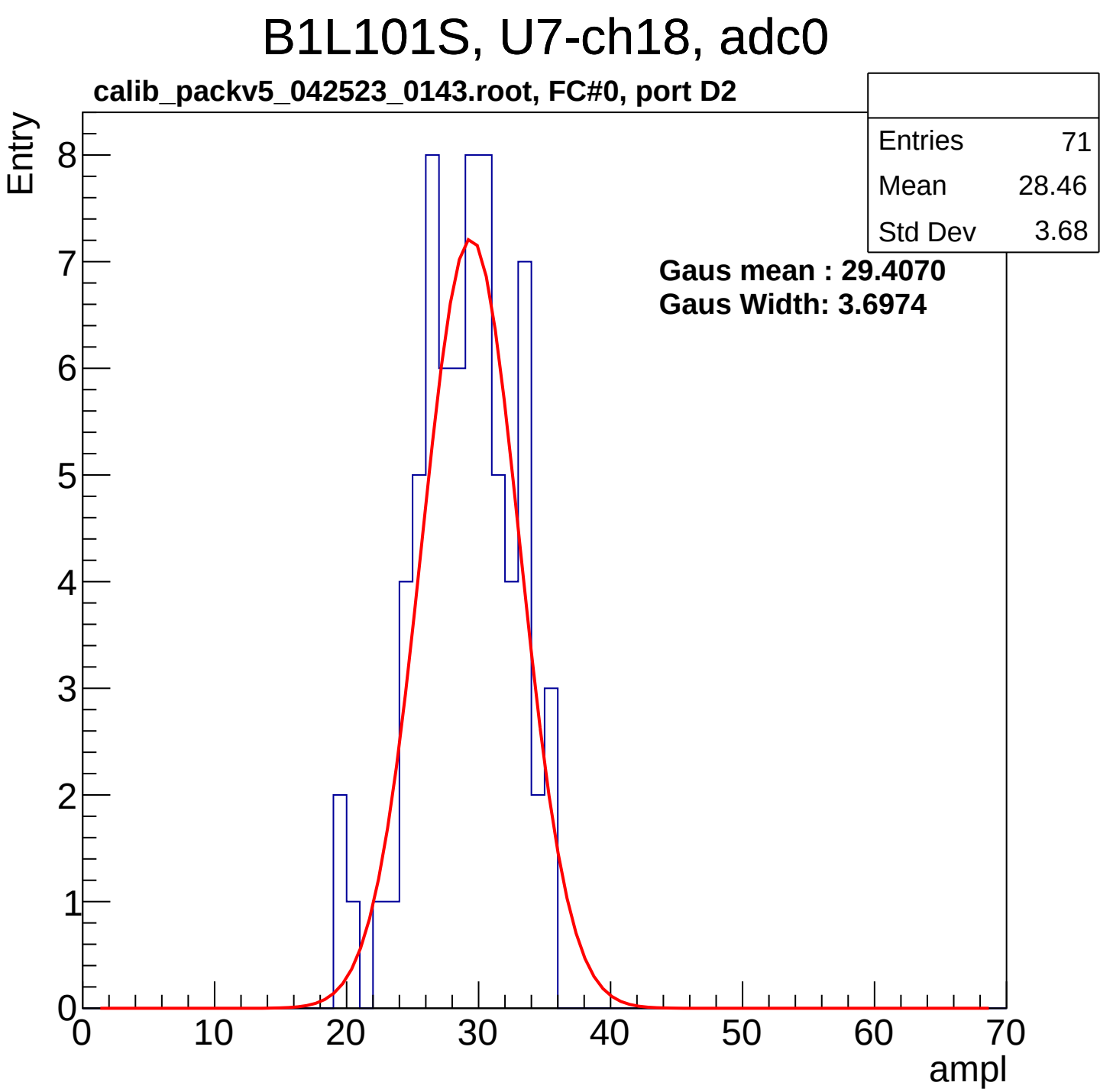
B1L101S, U7-ch18, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 28.46
Std Dev 3.68
Gaus mean : 29.4070
Gaus Width: 3.6974
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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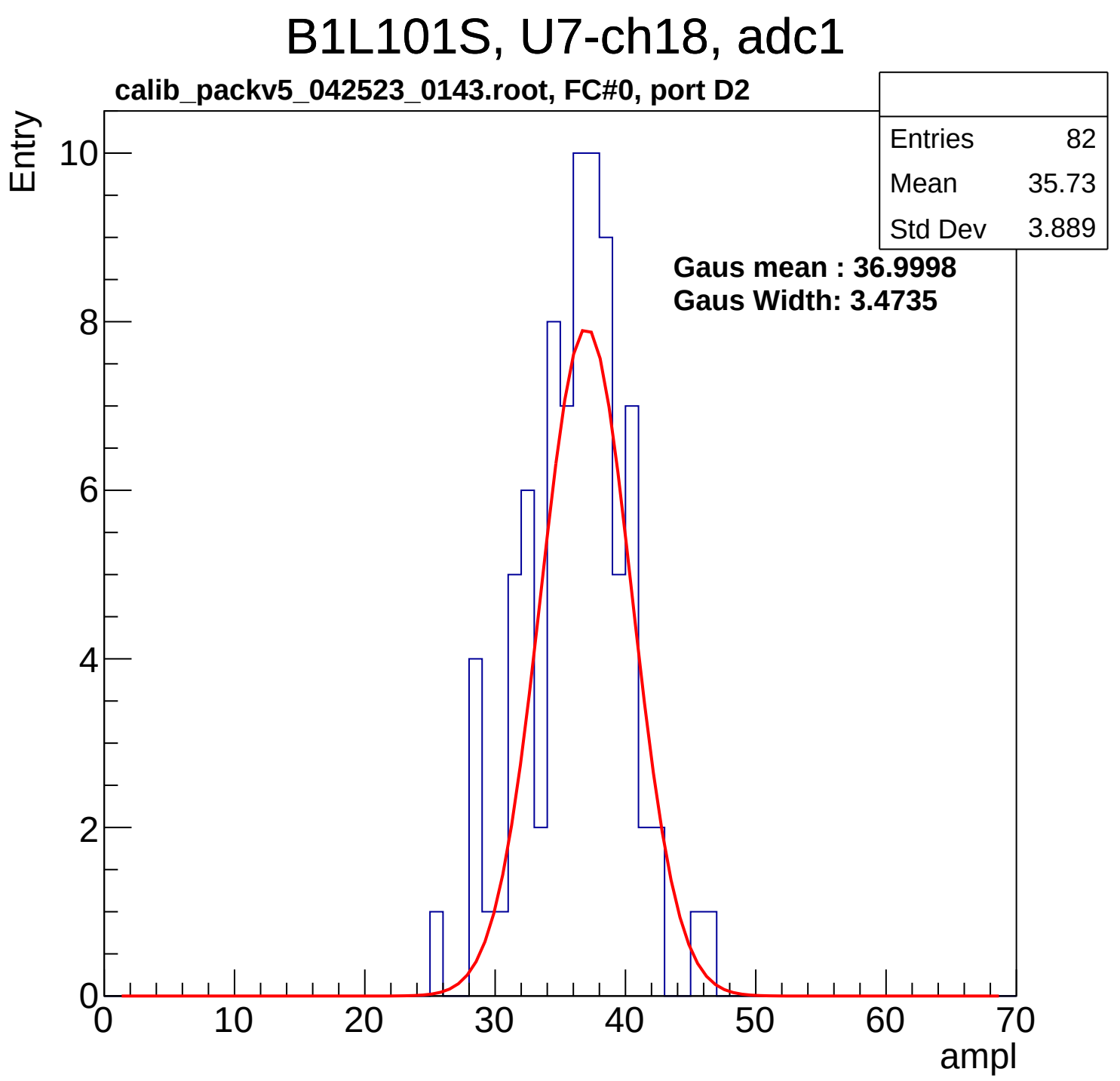
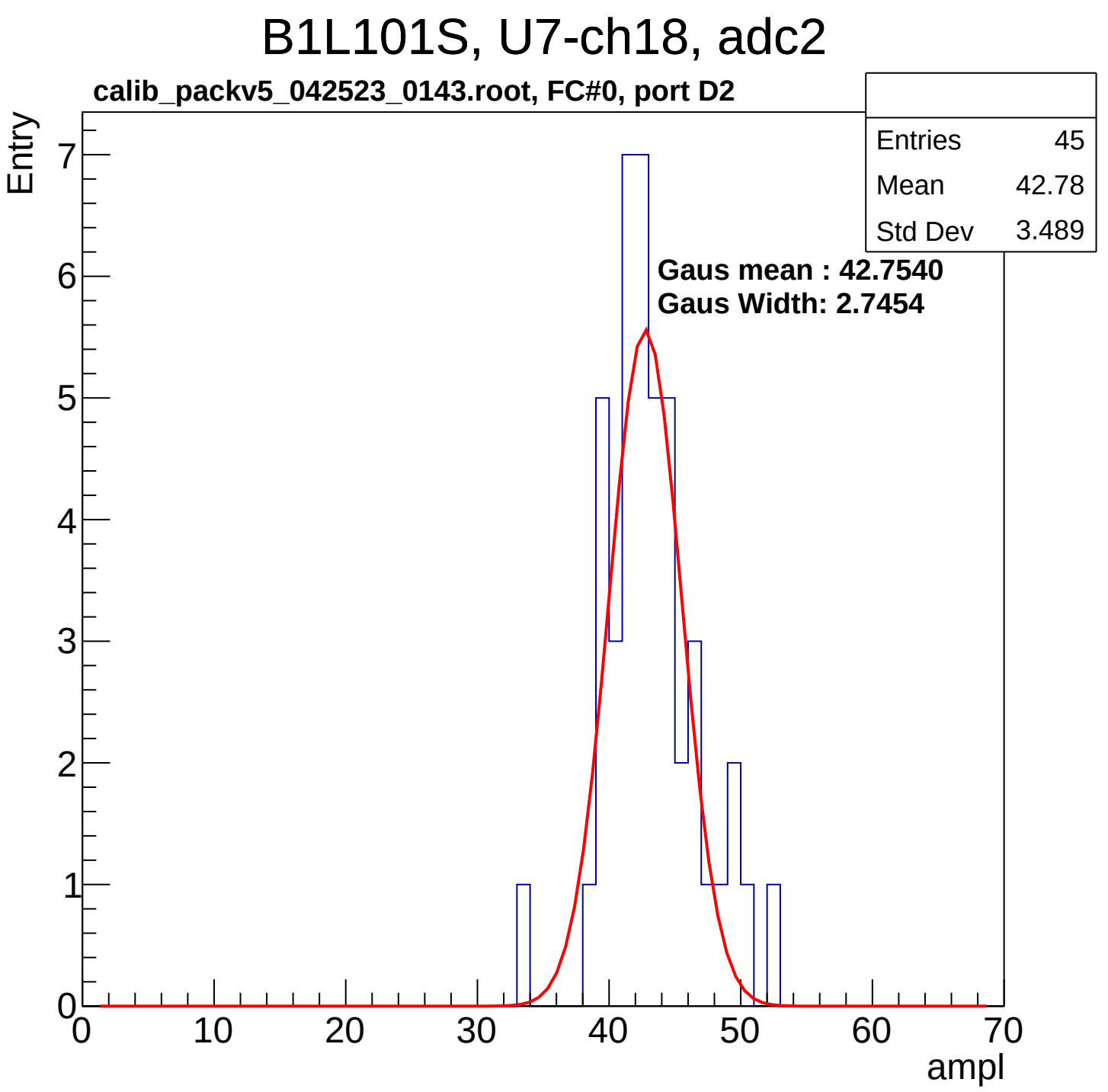
40
50
60
70


B1L101S, U7-ch18, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 82
Mean 35.73
Std Dev 3.889
Gaus mean : 36.9998
Gaus Width: 3.4735
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch18, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 42.78
Std Dev 3.489
Gaus mean : 42.7540
Gaus Width: 2.7454
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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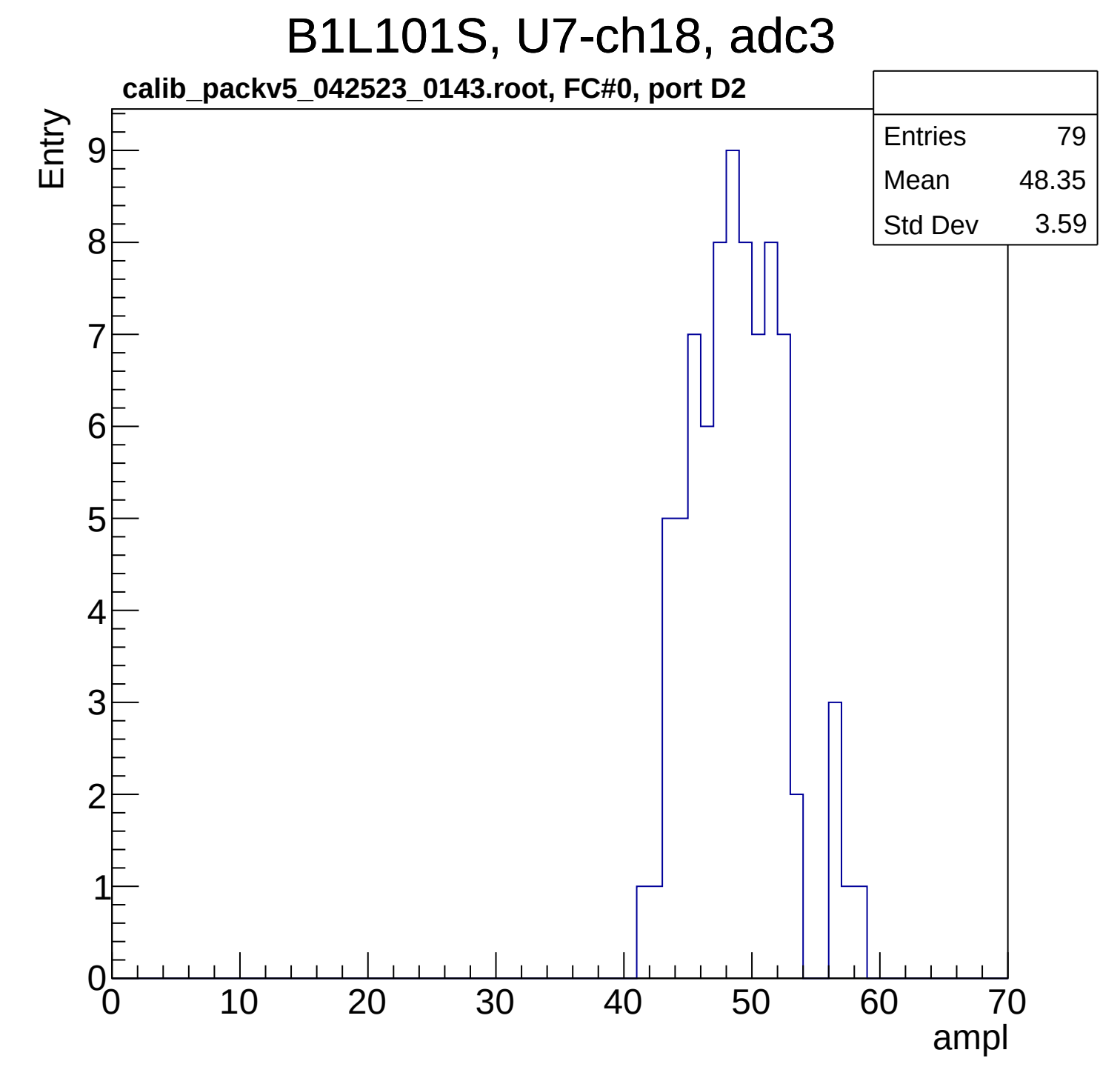
B1L101S, U7-ch18, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 48.35
Std Dev 3.59
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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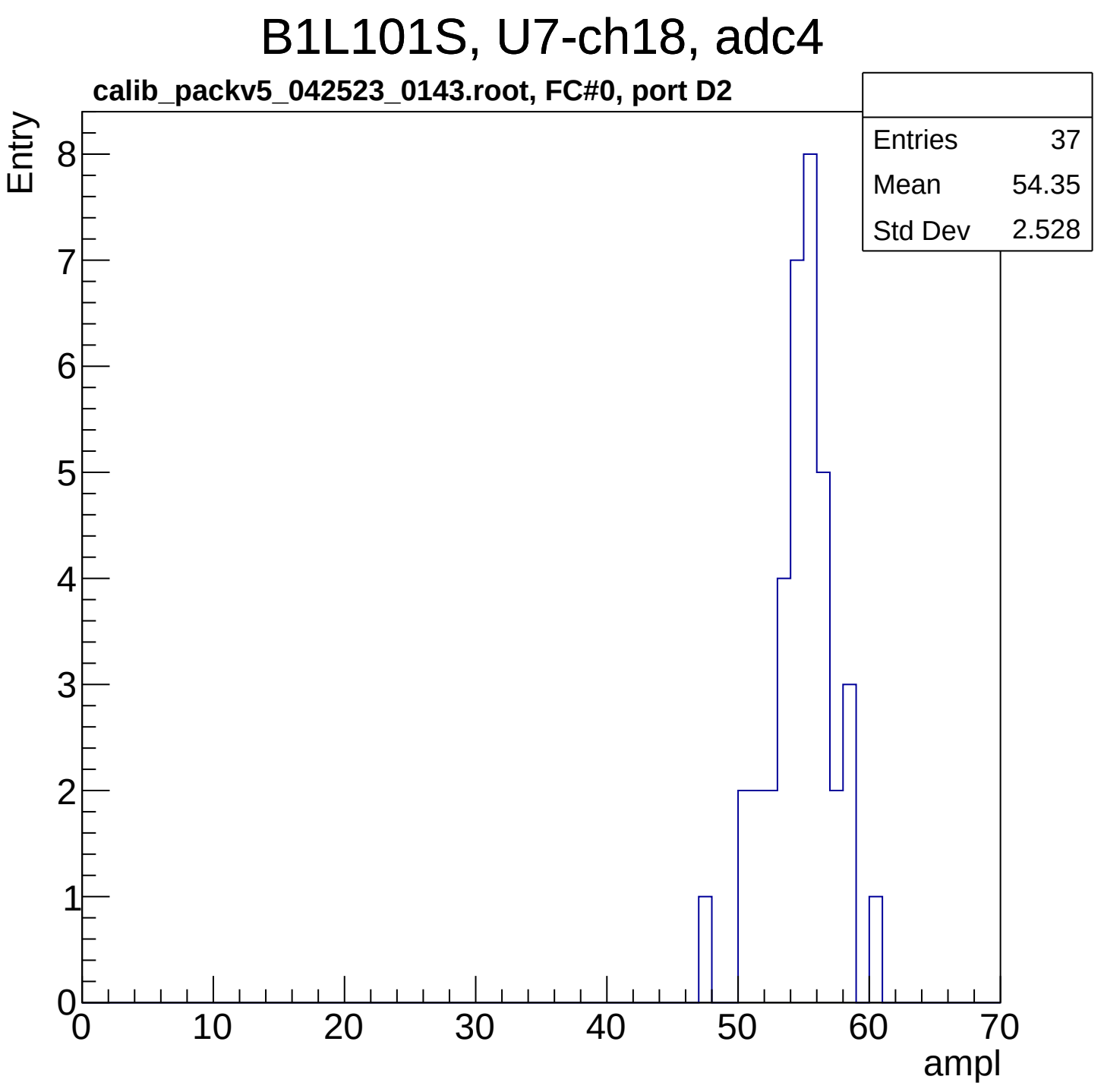
B1L101S, U7-ch18, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 37
Mean 54.35
Std Dev 2.528
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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40
50
60
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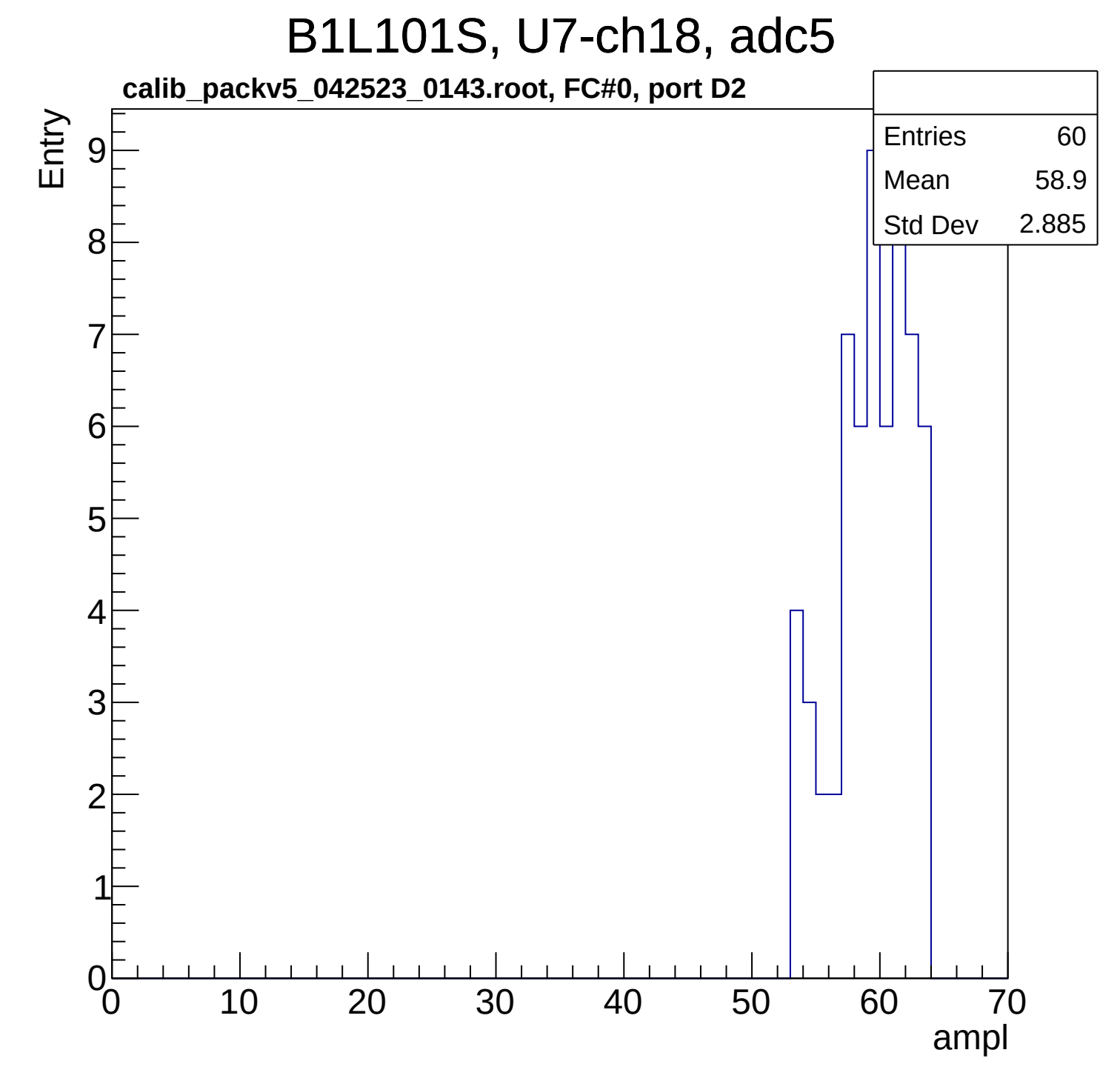
B1L101S, U7-ch18, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 58.9
Std Dev 2.885
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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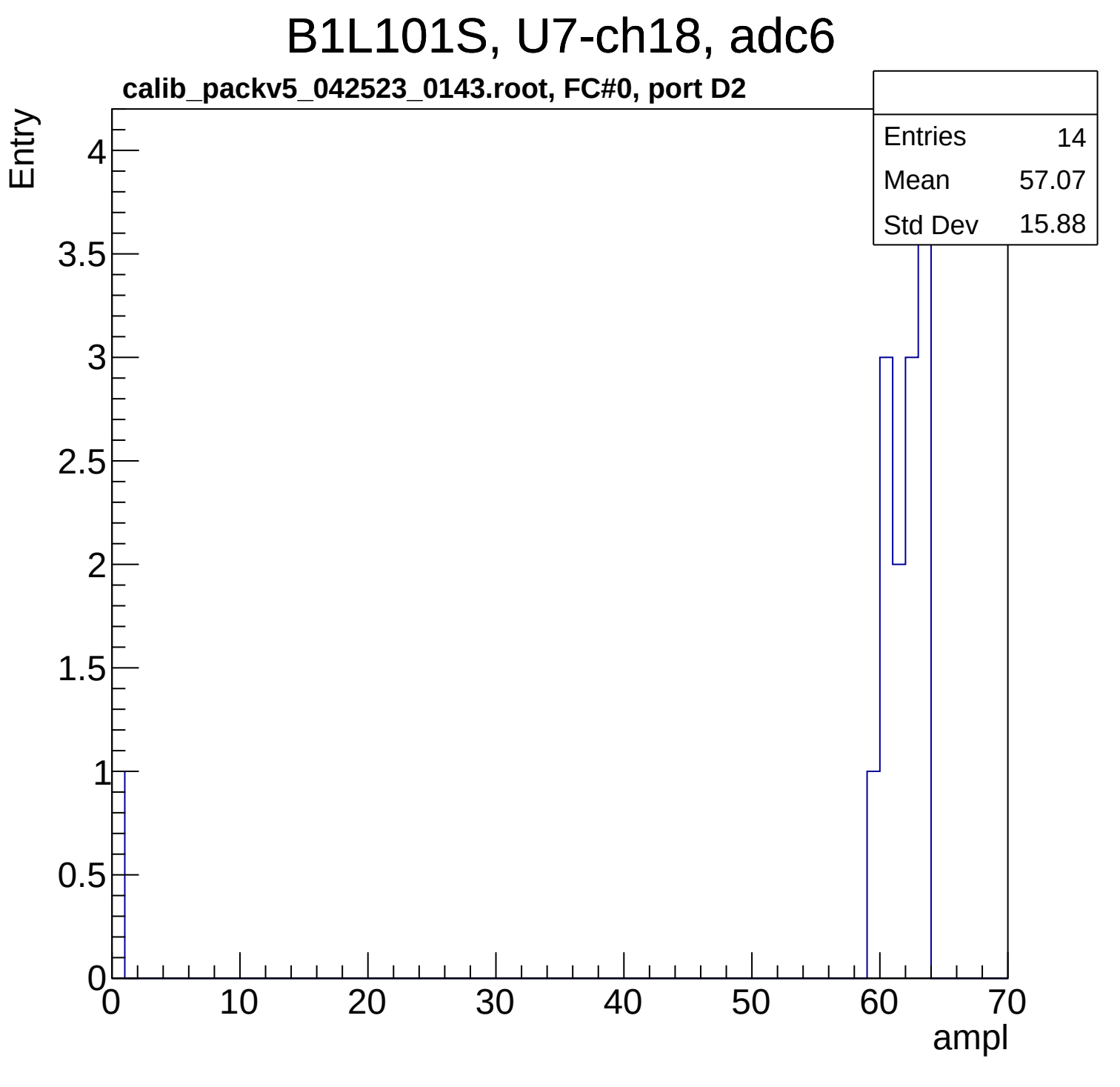
B1L101S, U7-ch18, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 14
Mean 57.07
Std Dev 15.88
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
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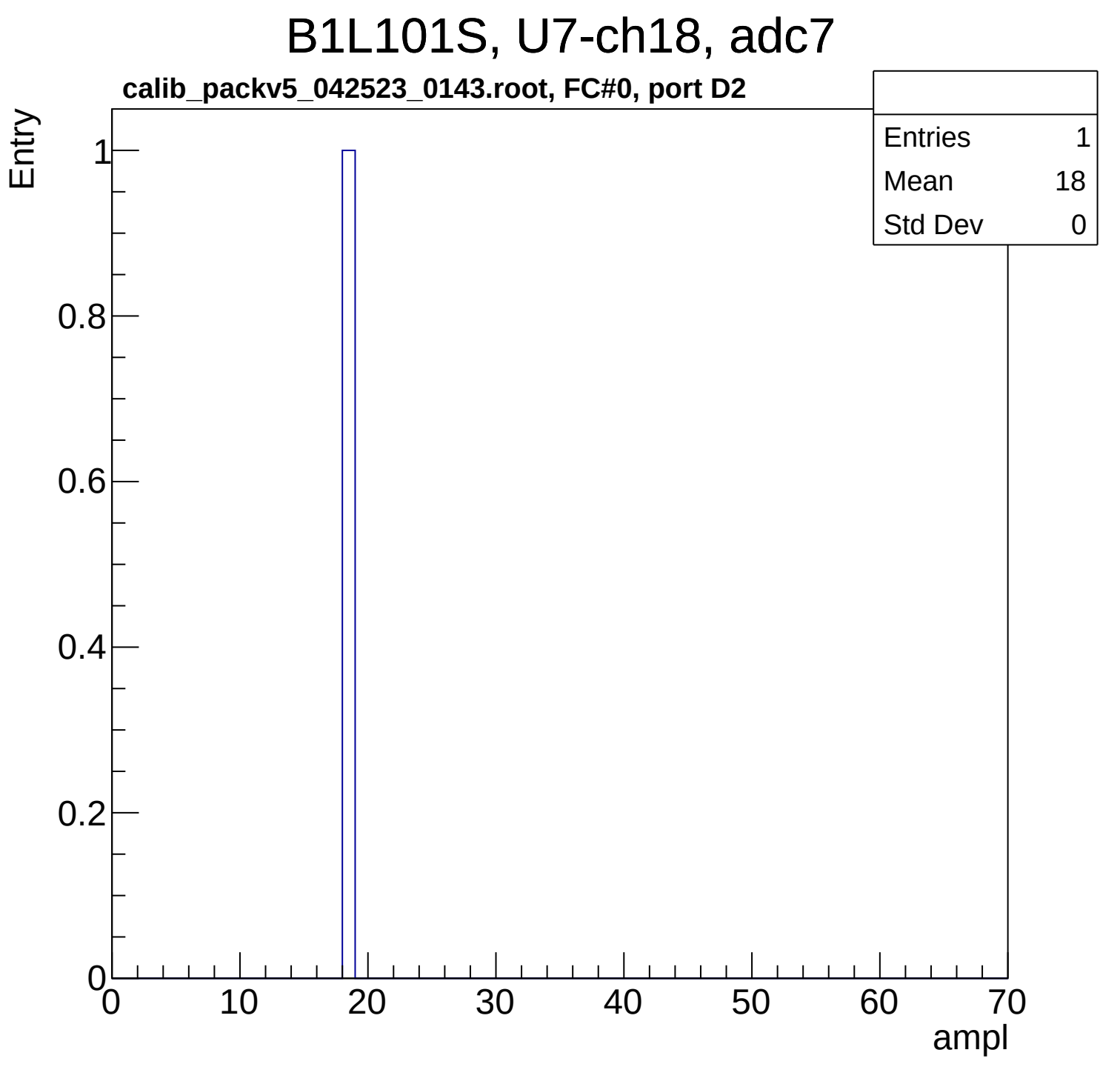
30
40
50
60
70


B1L101S, U7-ch18, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 18
Std Dev 0
Entry
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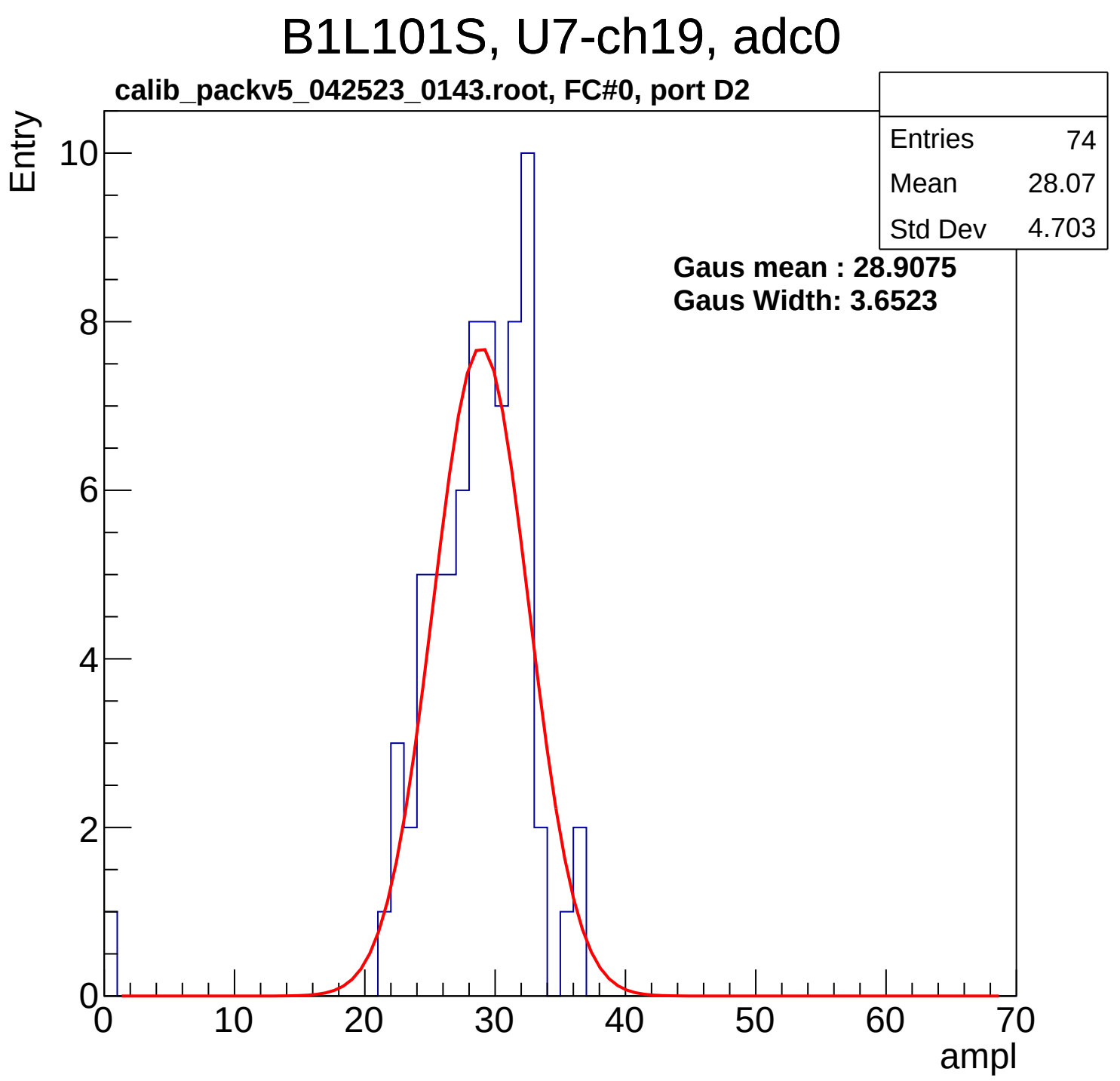
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch19, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 28.07
Std Dev 4.703
Gaus mean : 28.9075
Gaus Width: 3.6523
Entry
ampl
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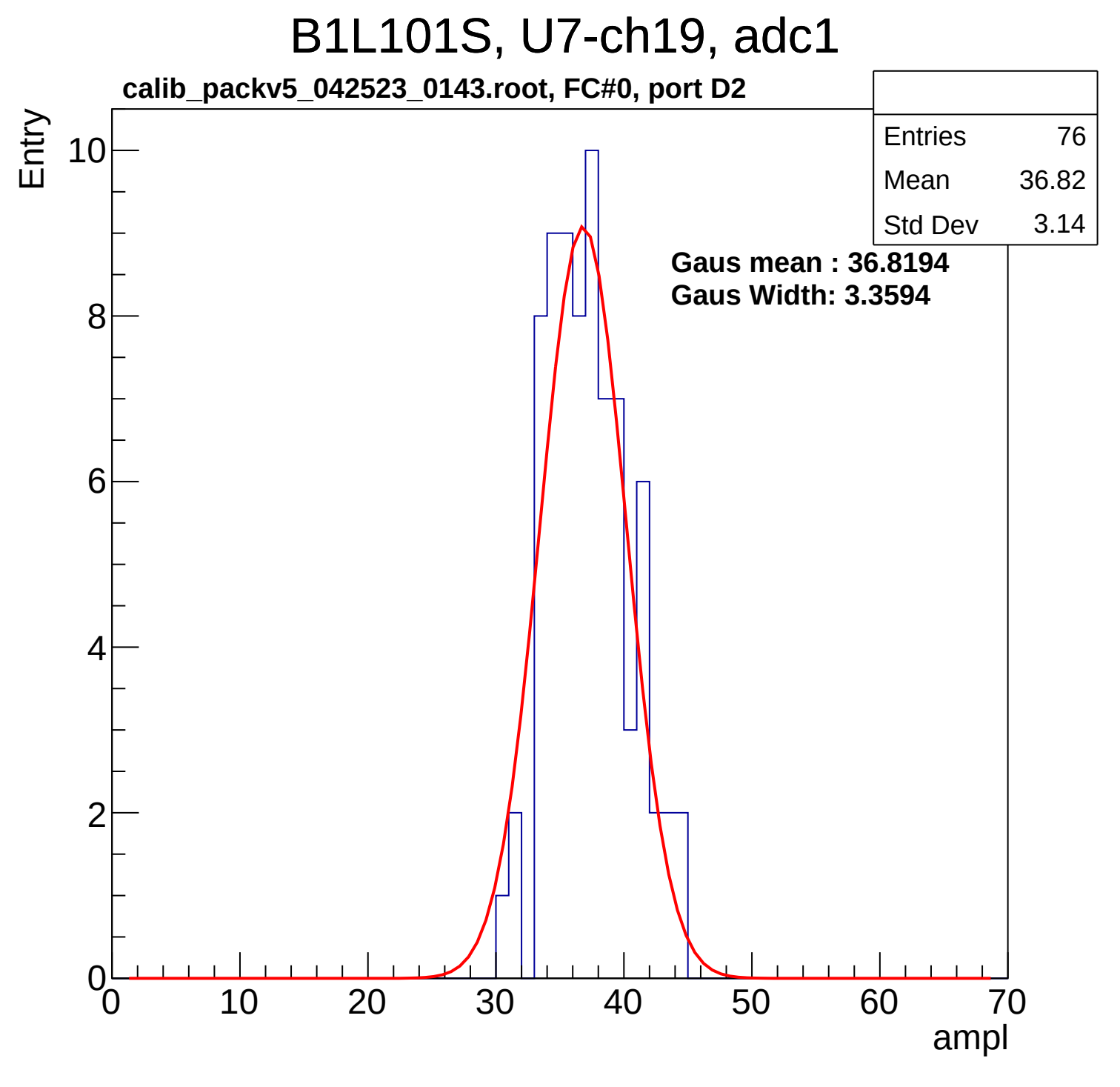
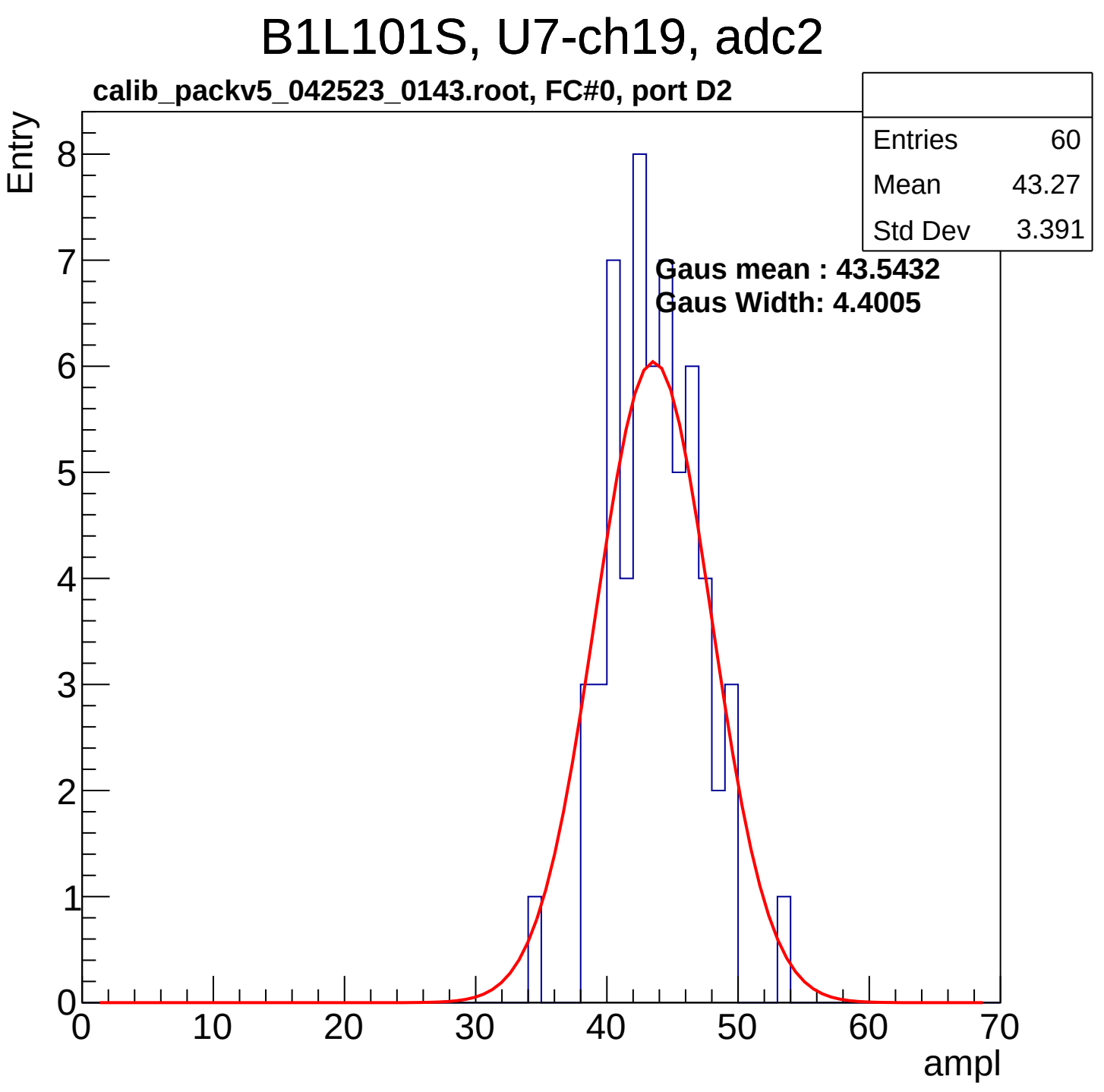
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch19, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 36.82
Std Dev 3.14
Gaus mean : 36.8194
Gaus Width: 3.3594
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch19, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 43.27
Std Dev 3.391
Gaus mean : 43.5432
Gaus Width: 4.4005
Entry
ampl
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1
2
3
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5
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0
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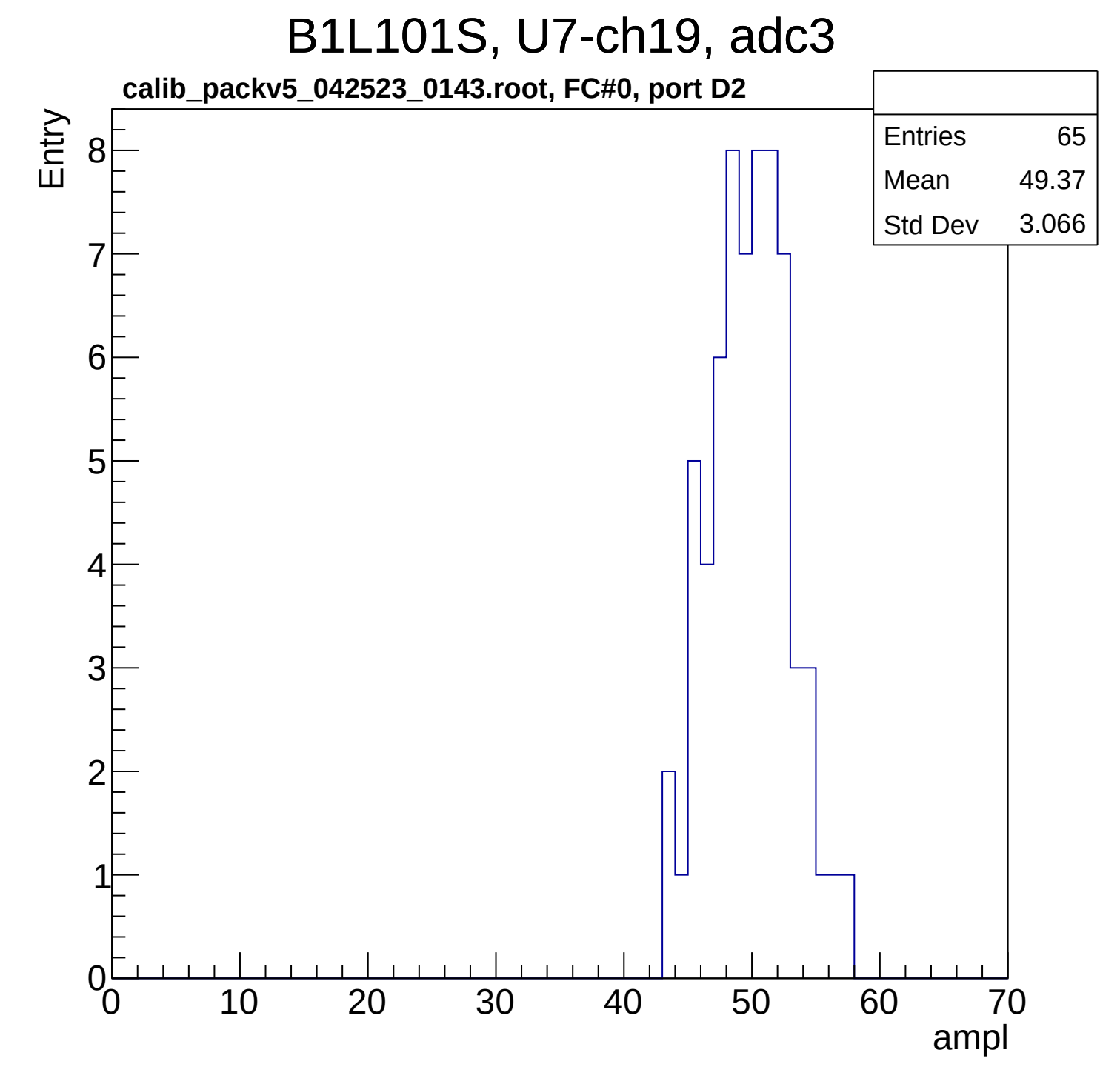
B1L101S, U7-ch19, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 49.37
Std Dev 3.066
Entry
ampl
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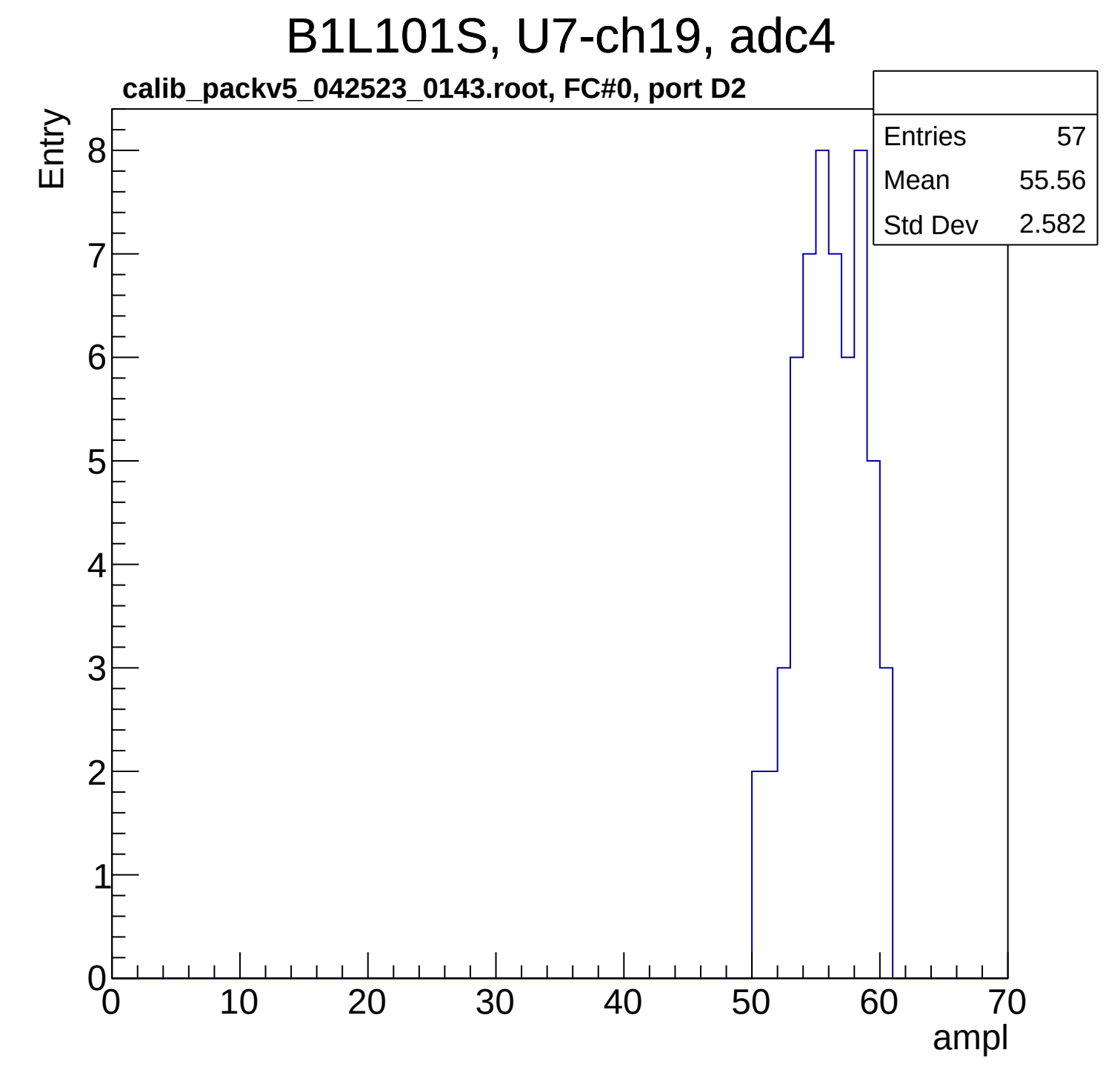
B1L101S, U7-ch19, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 55.56
Std Dev 2.582
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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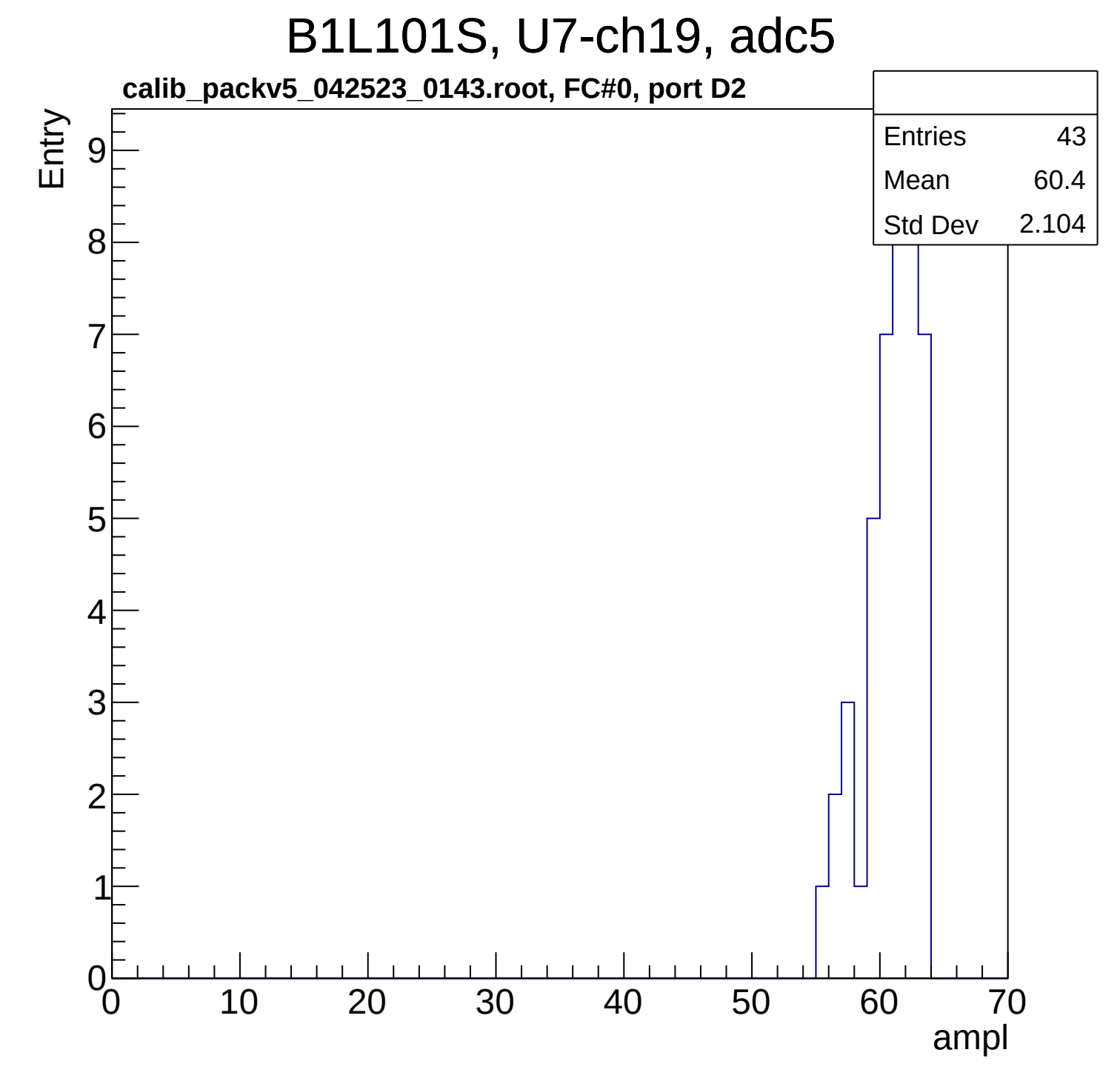
B1L101S, U7-ch19, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 43
Mean 60.4
Std Dev 2.104
Entry
ampl
0
1
2
3
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5
6
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0
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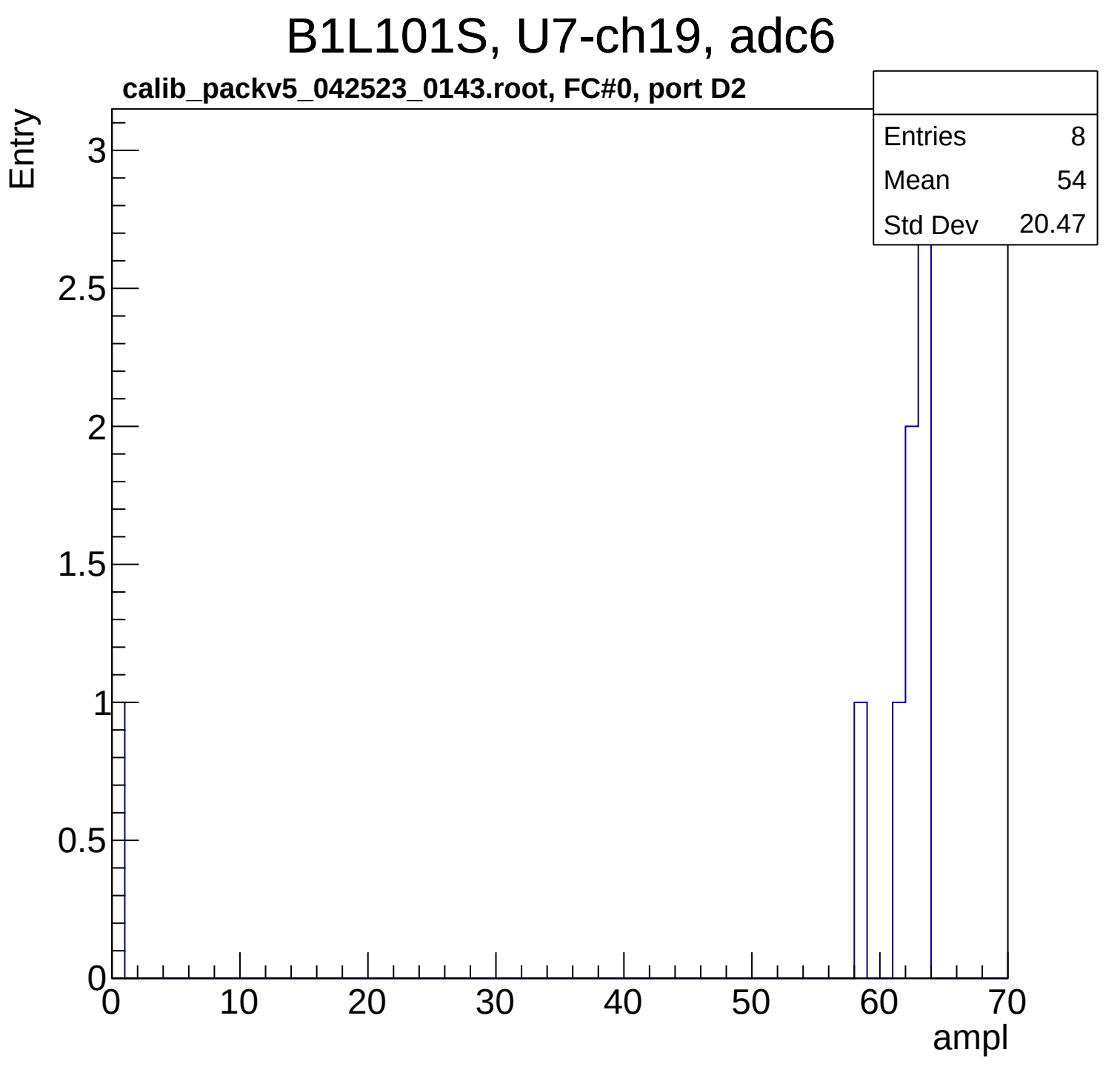
B1L101S, U7-ch19, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 54
Std Dev 20.47
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
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40
50
60
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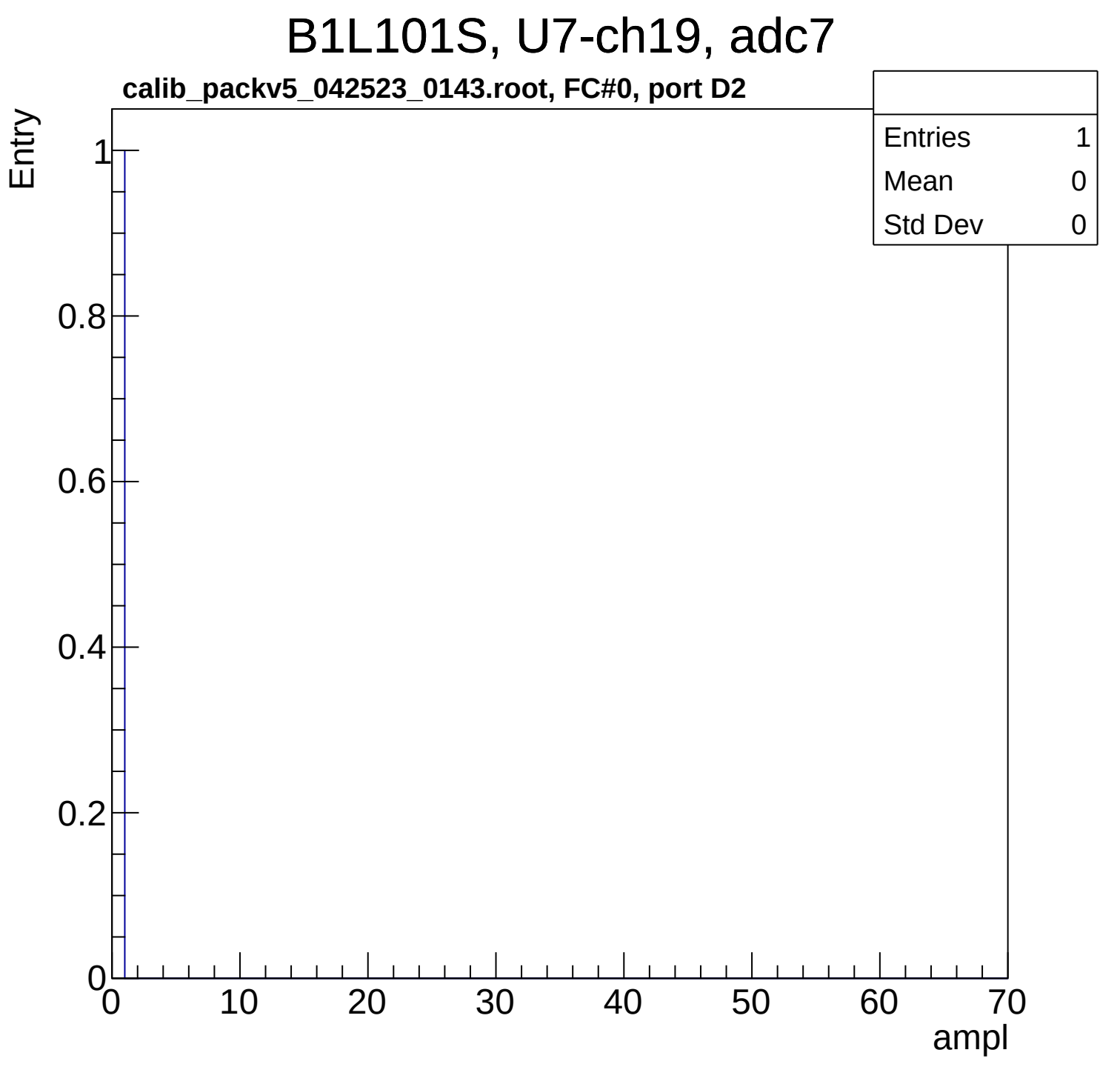
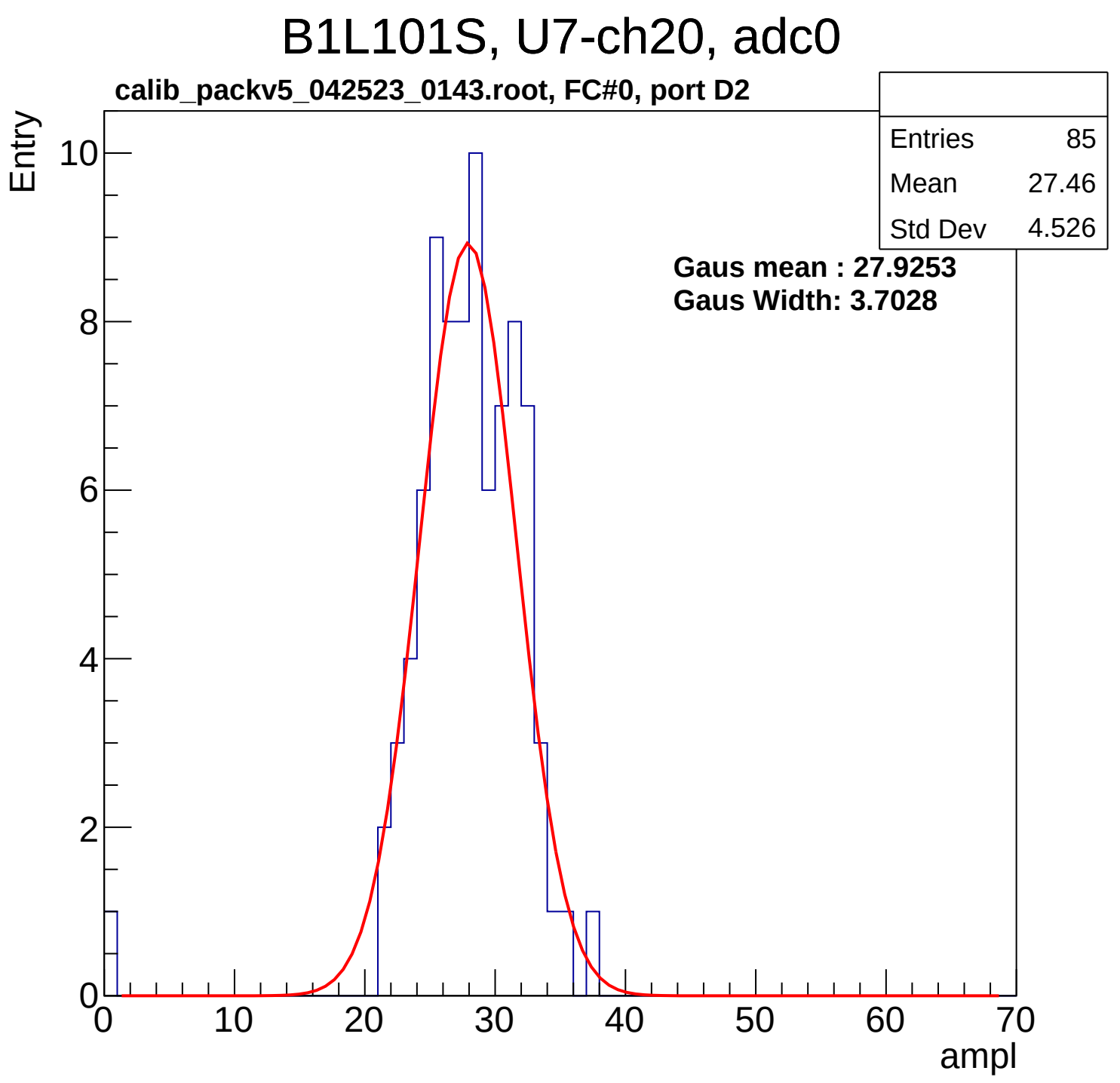
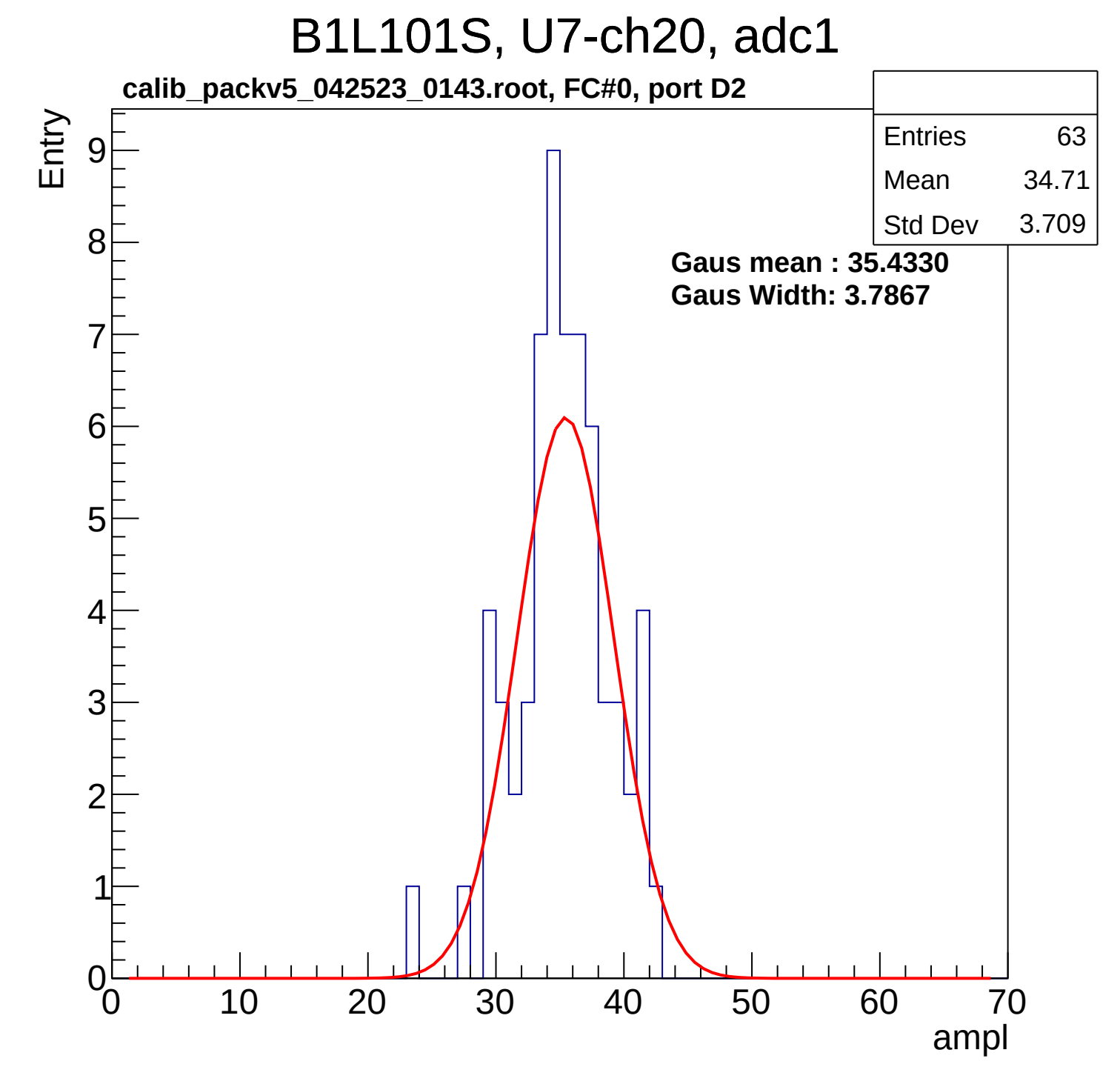

B1L101S, U7-ch19, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch20, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 85
Mean 27.46
Std Dev 4.526
Gaus mean : 27.9253
Gaus Width: 3.7028
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch20, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 34.71
Std Dev 3.709
Gaus mean : 35.4330
Gaus Width: 3.7867
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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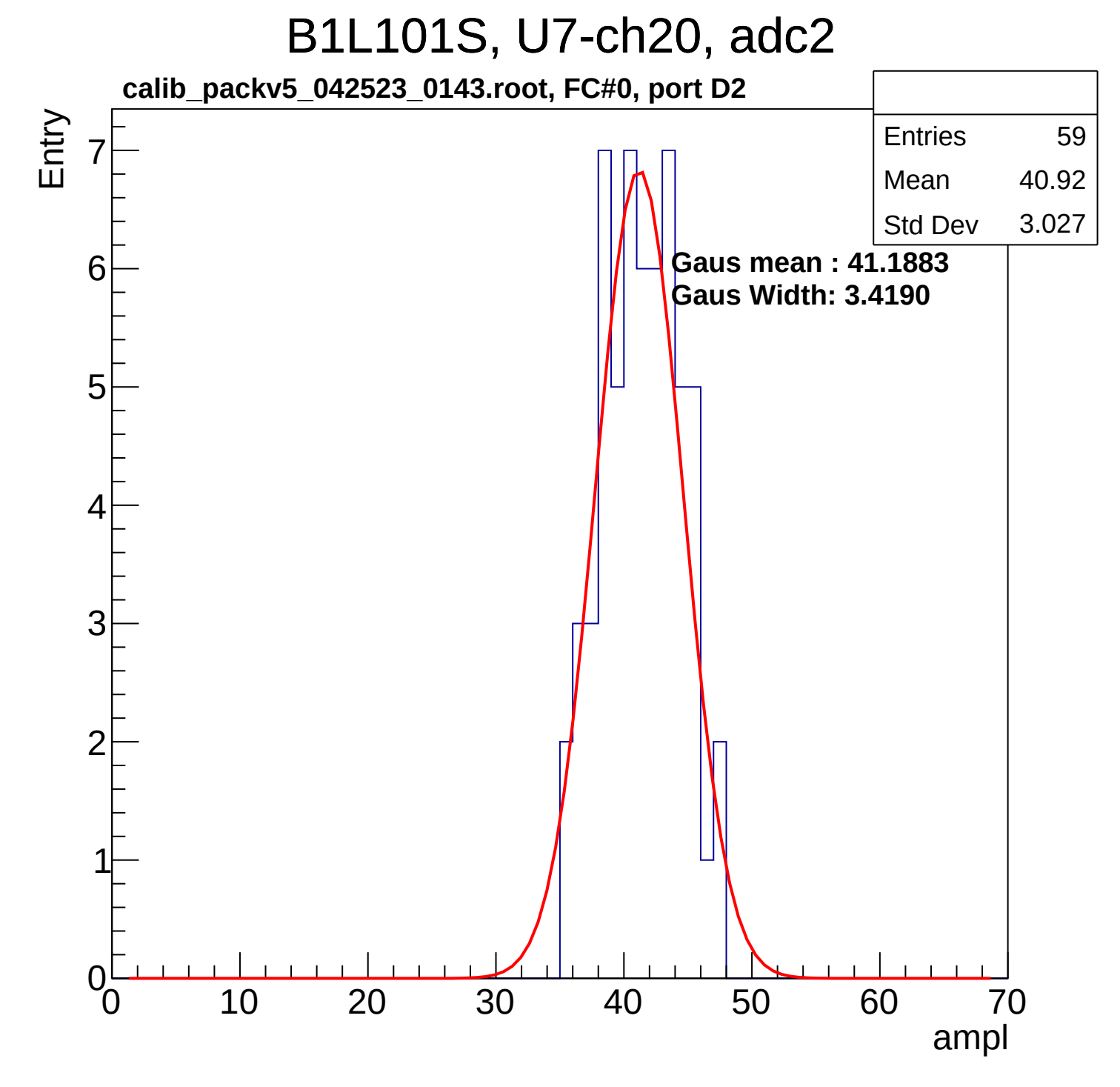
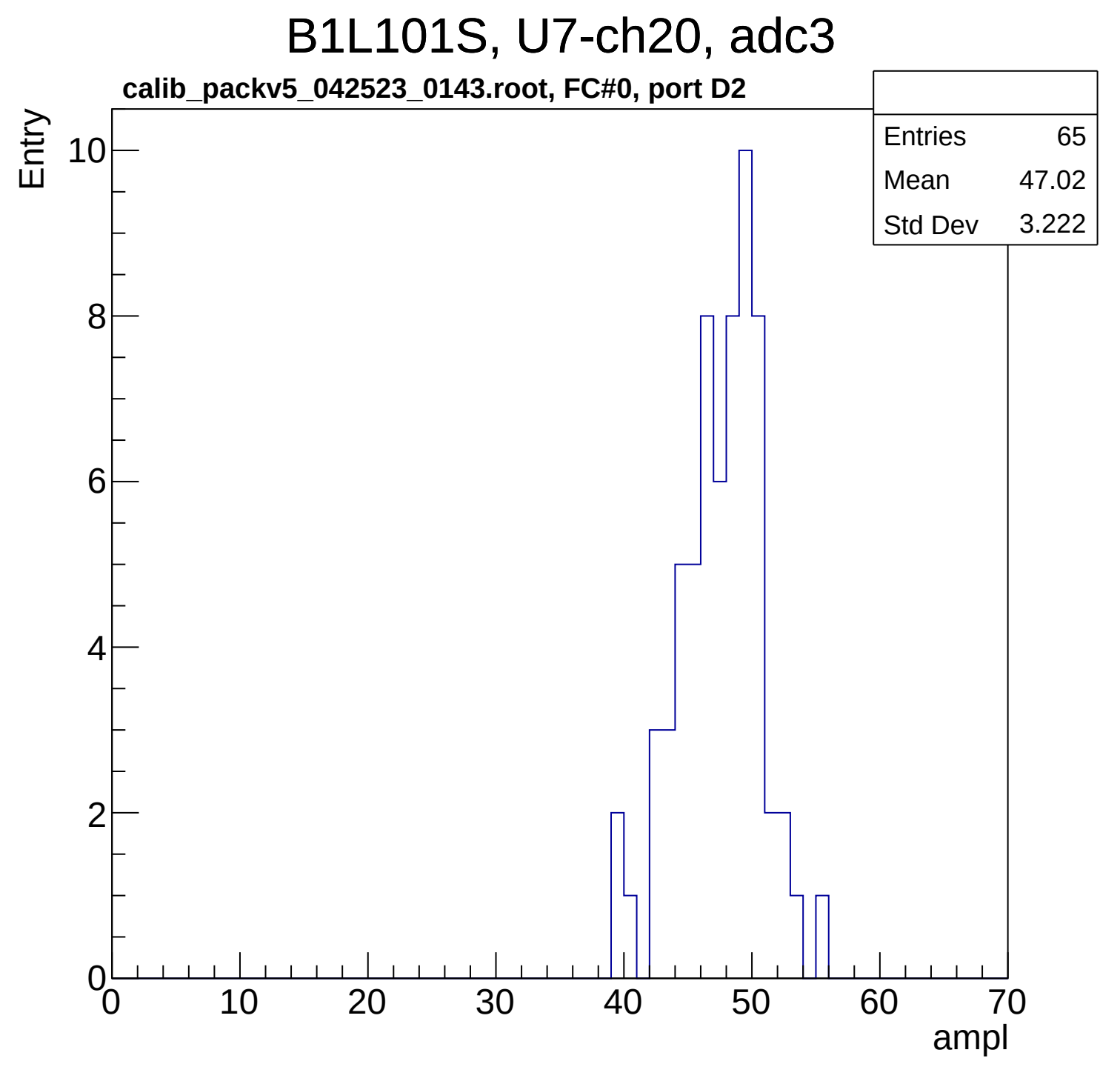
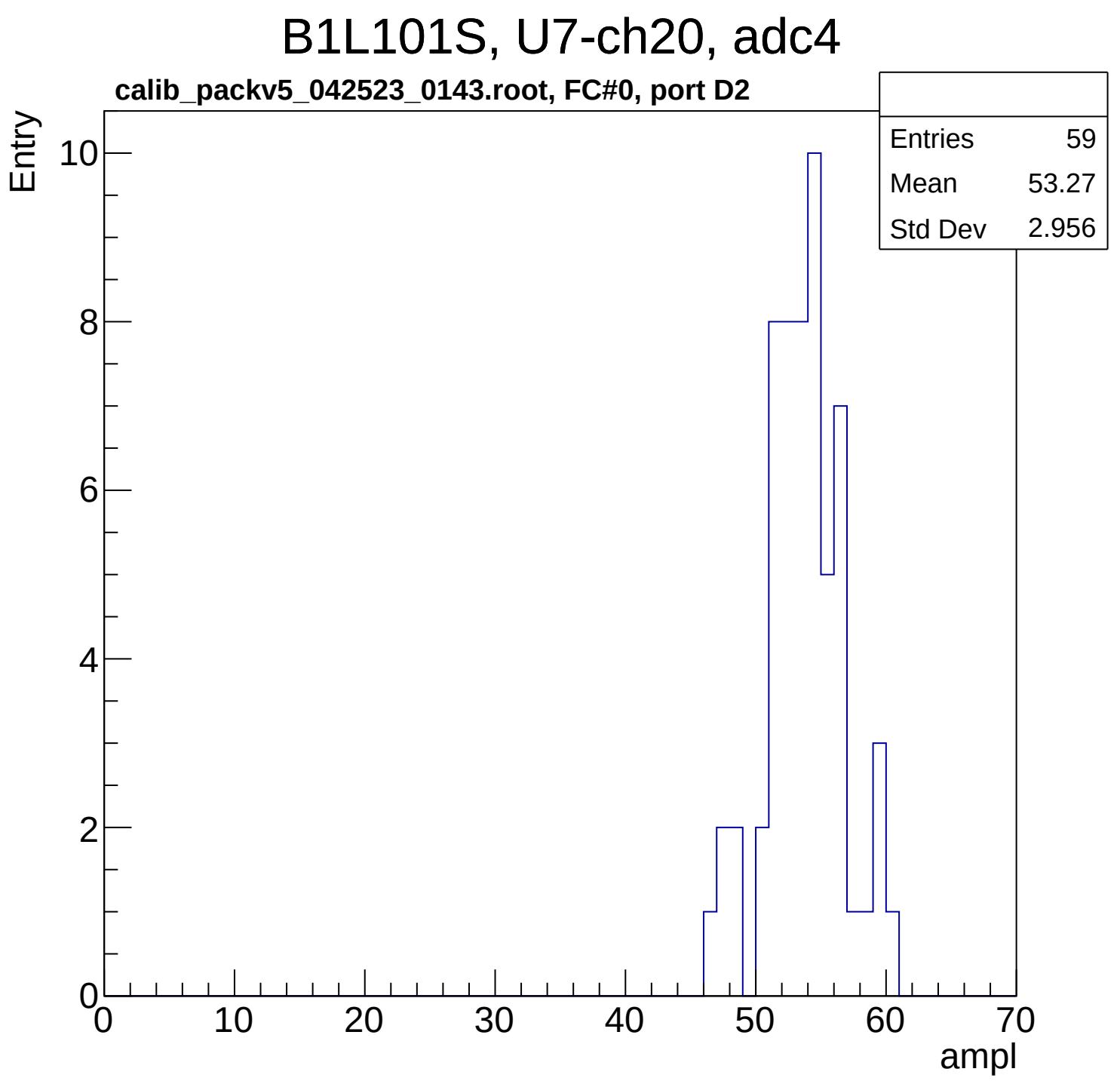

B1L101S, U7-ch20, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 40.92
Std Dev 3.027
Gaus mean : 41.1883
Gaus Width: 3.4190
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U7-ch20, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 47.02
Std Dev 3.222
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch20, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 53.27
Std Dev 2.956
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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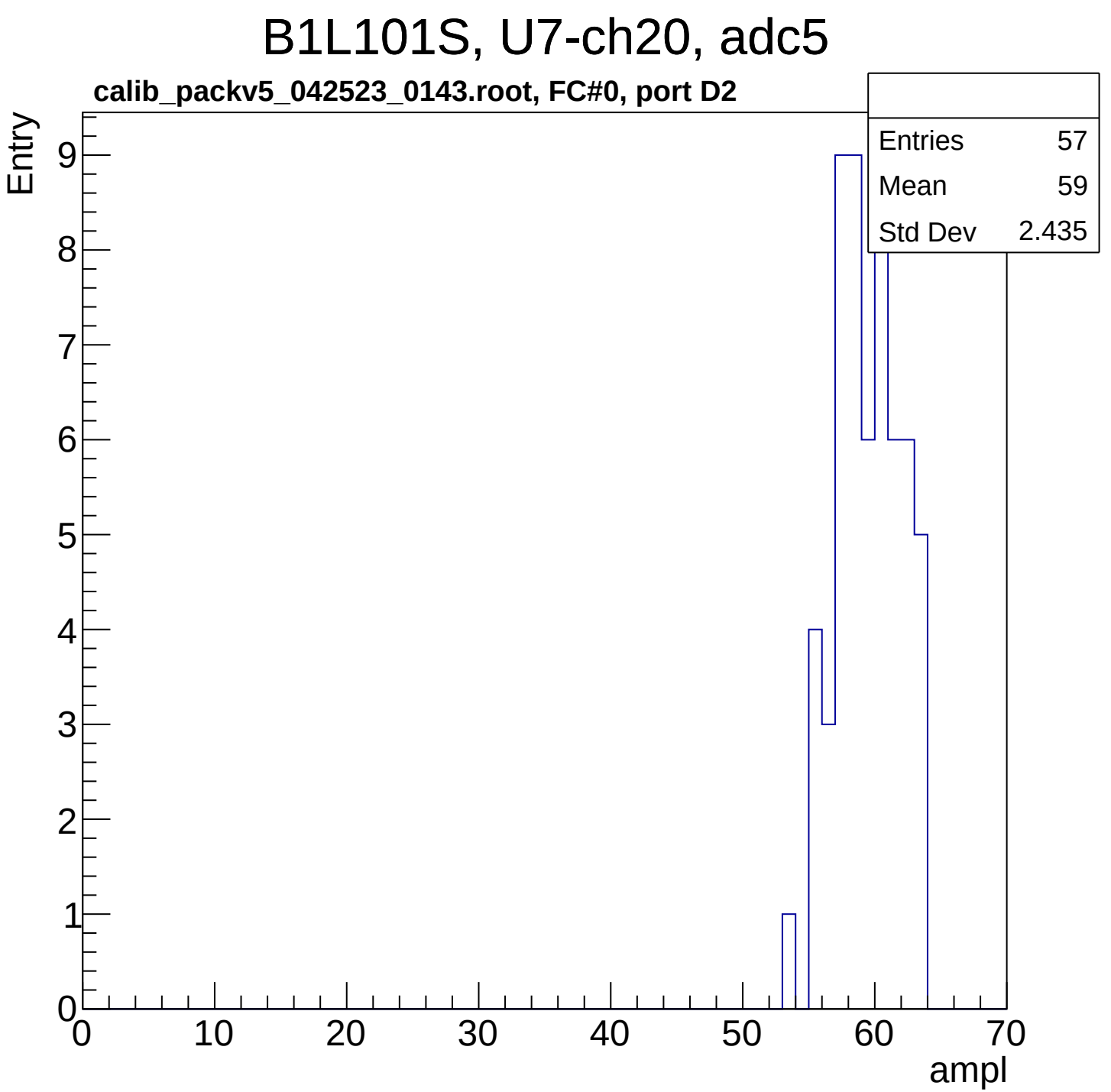
B1L101S, U7-ch20, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 59
Std Dev 2.435
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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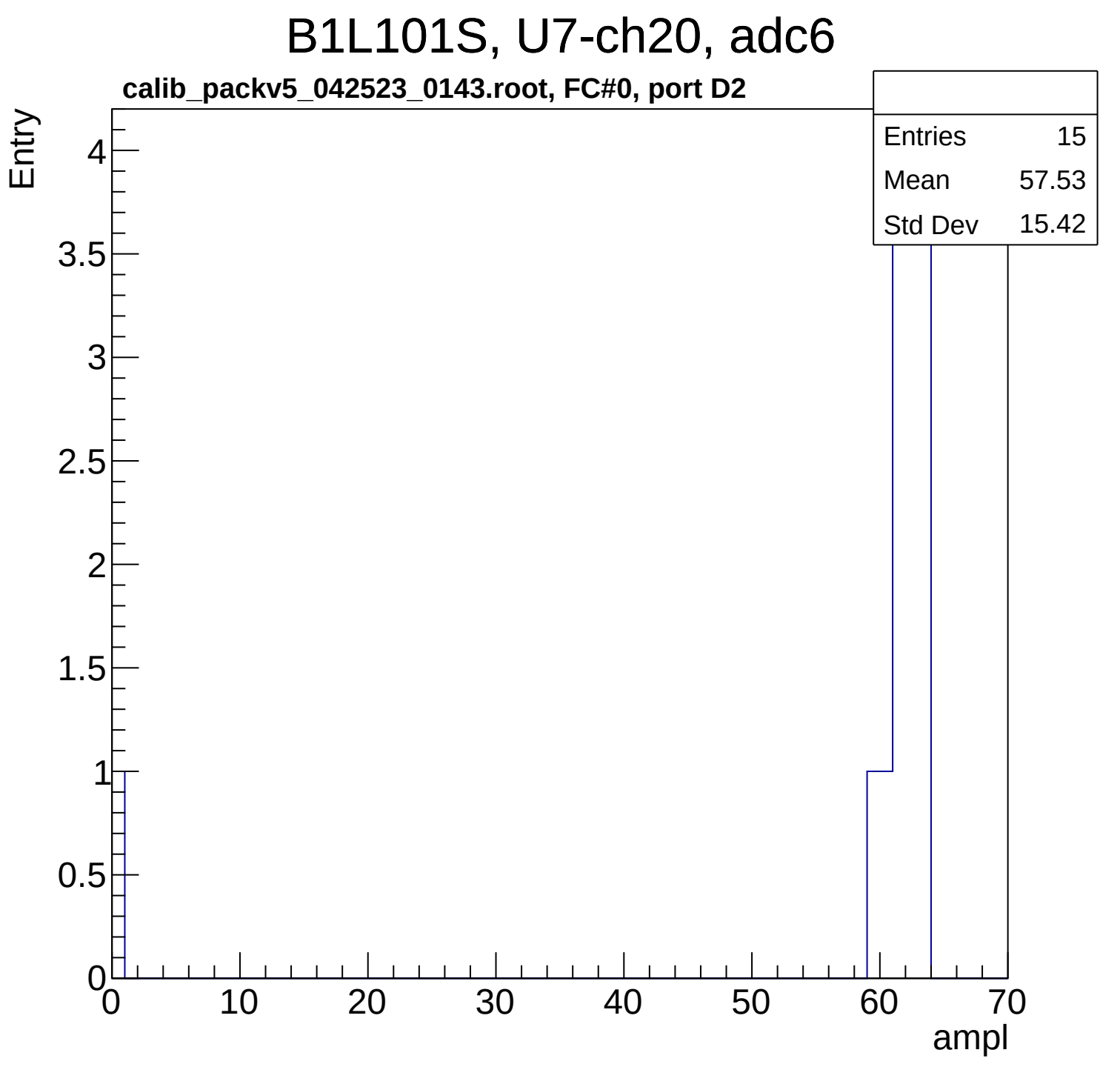
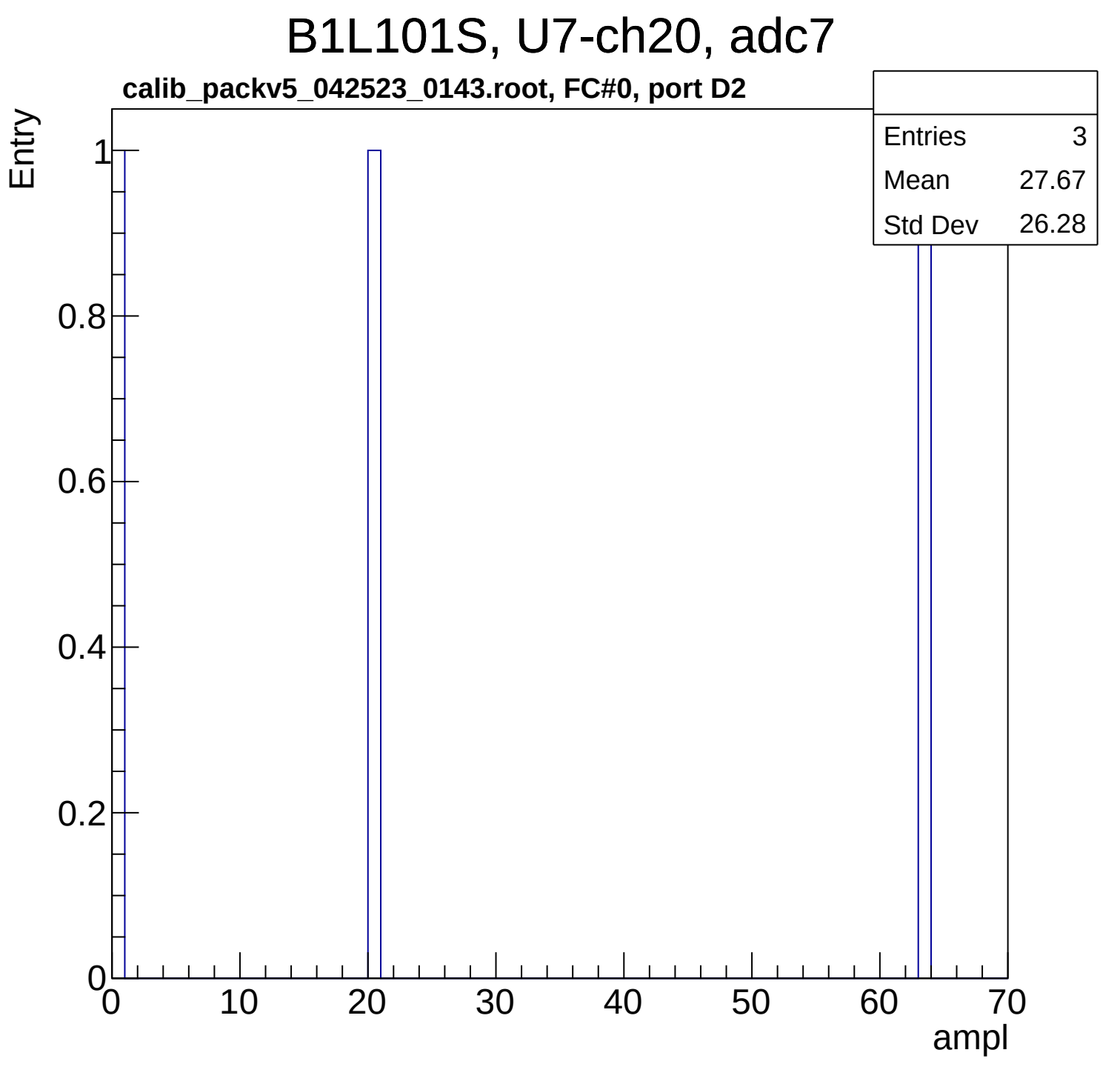
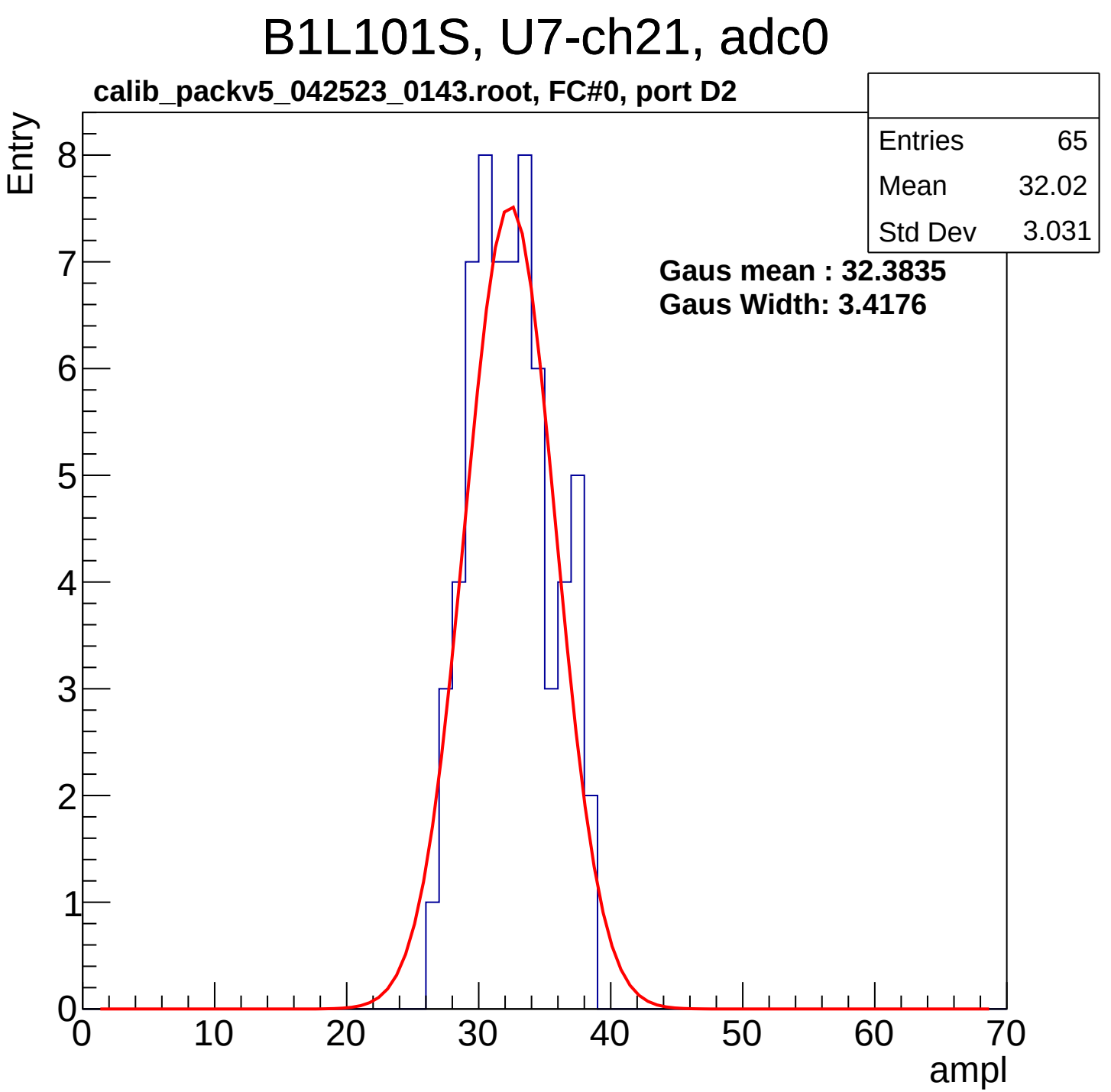
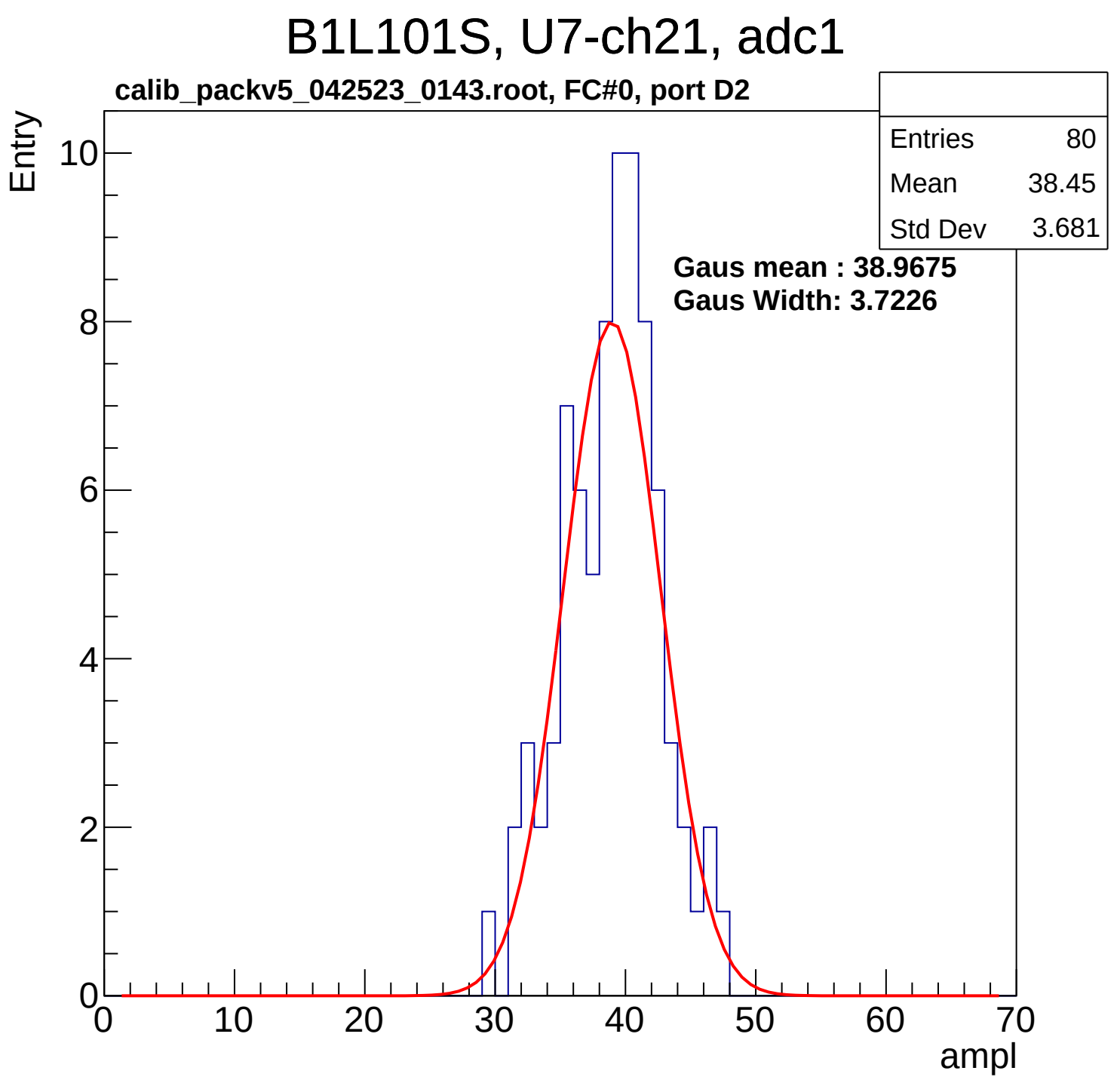
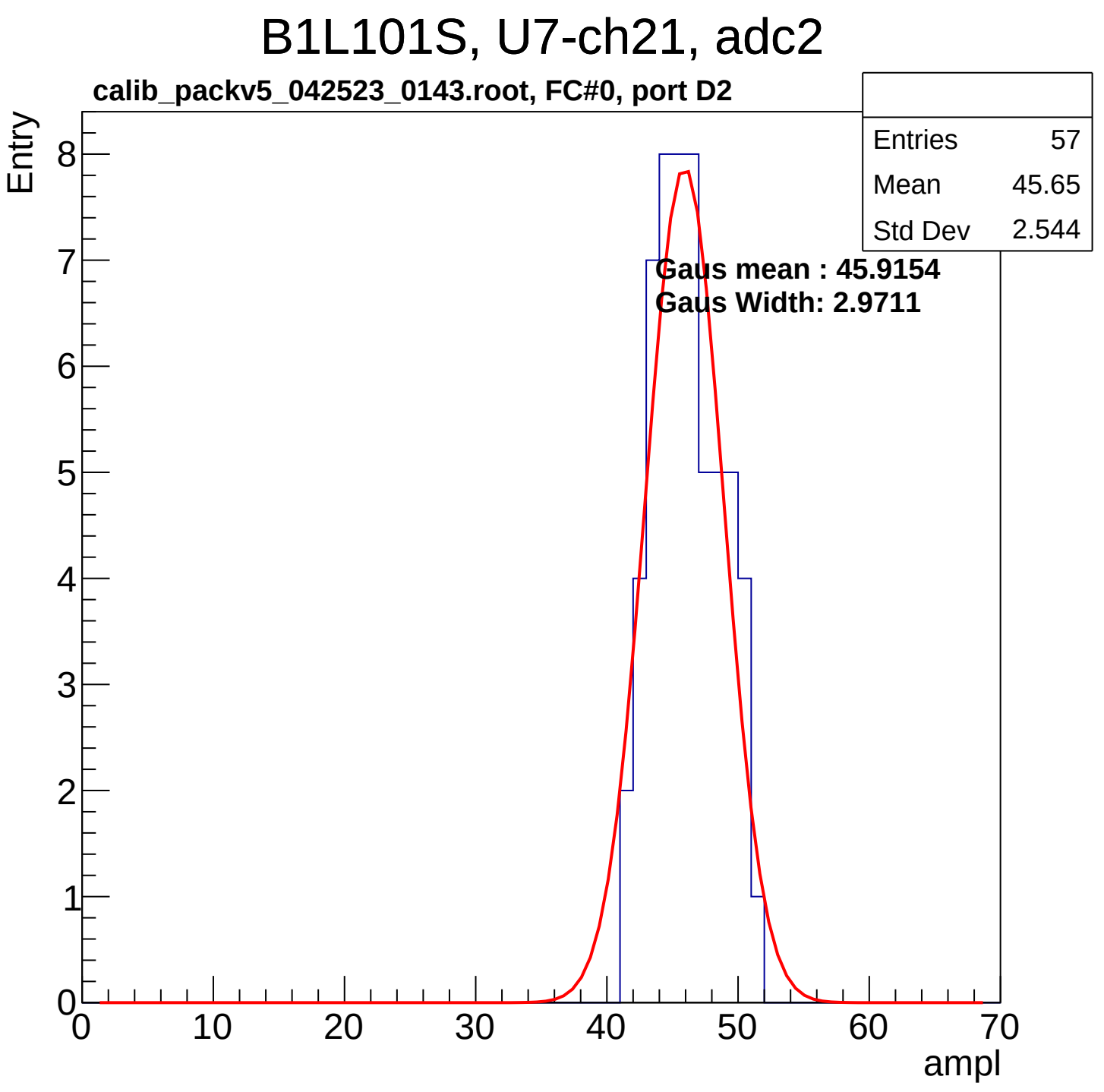
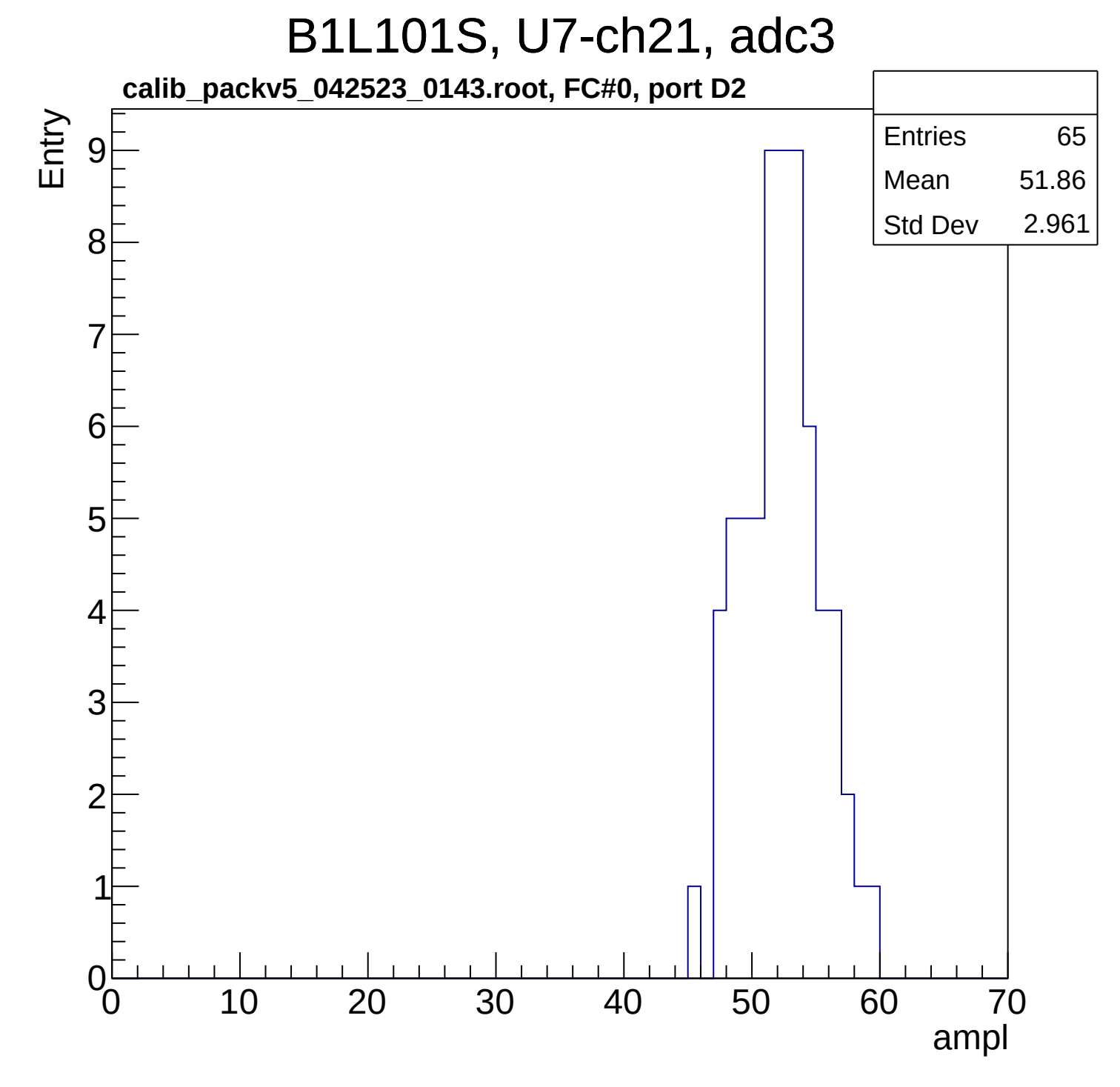

B1L101S, U7-ch20, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 15
Mean 57.53
Std Dev 15.42
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

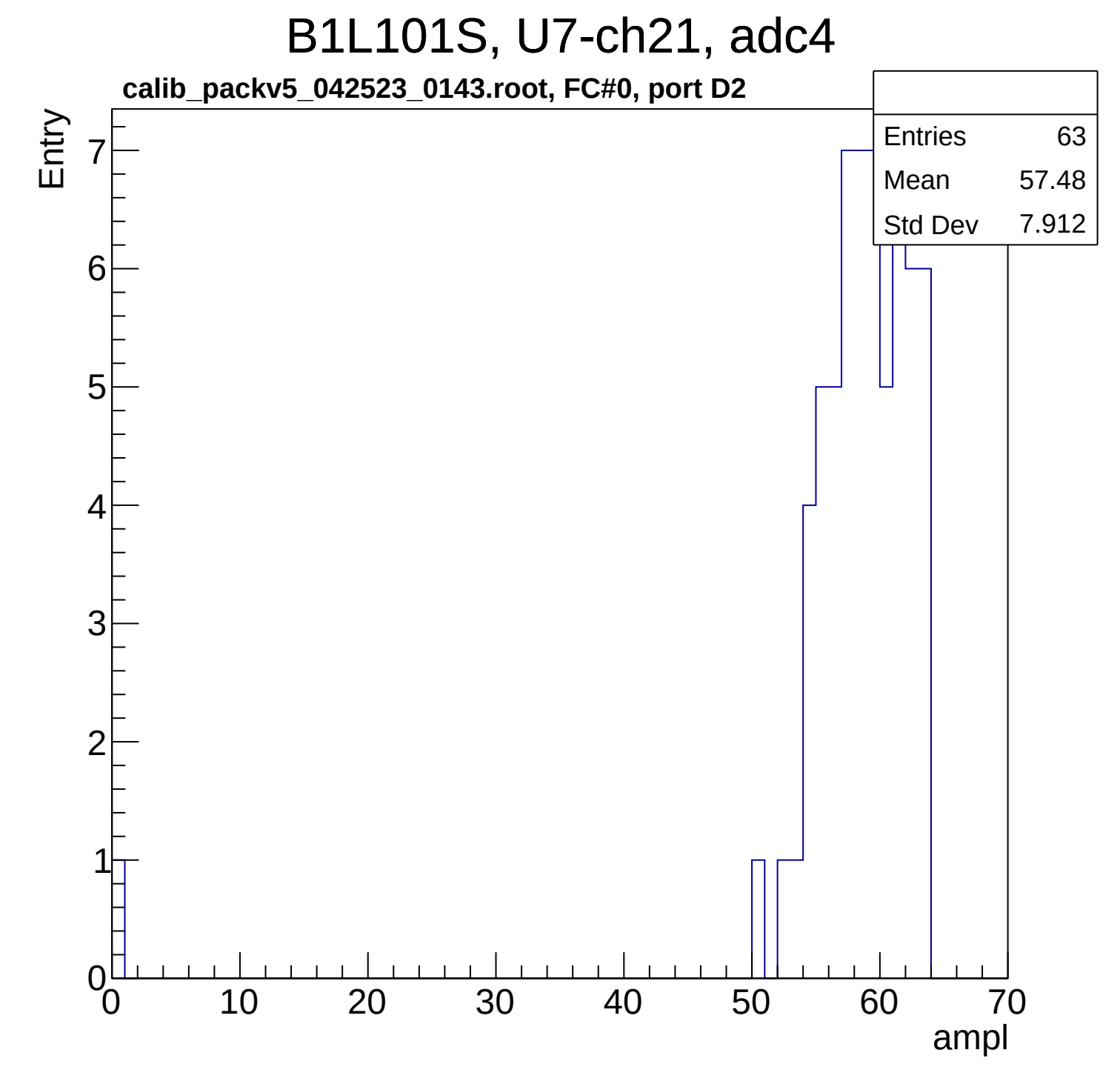

B1L101S, U7-ch20, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 27.67
Std Dev 26.28
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

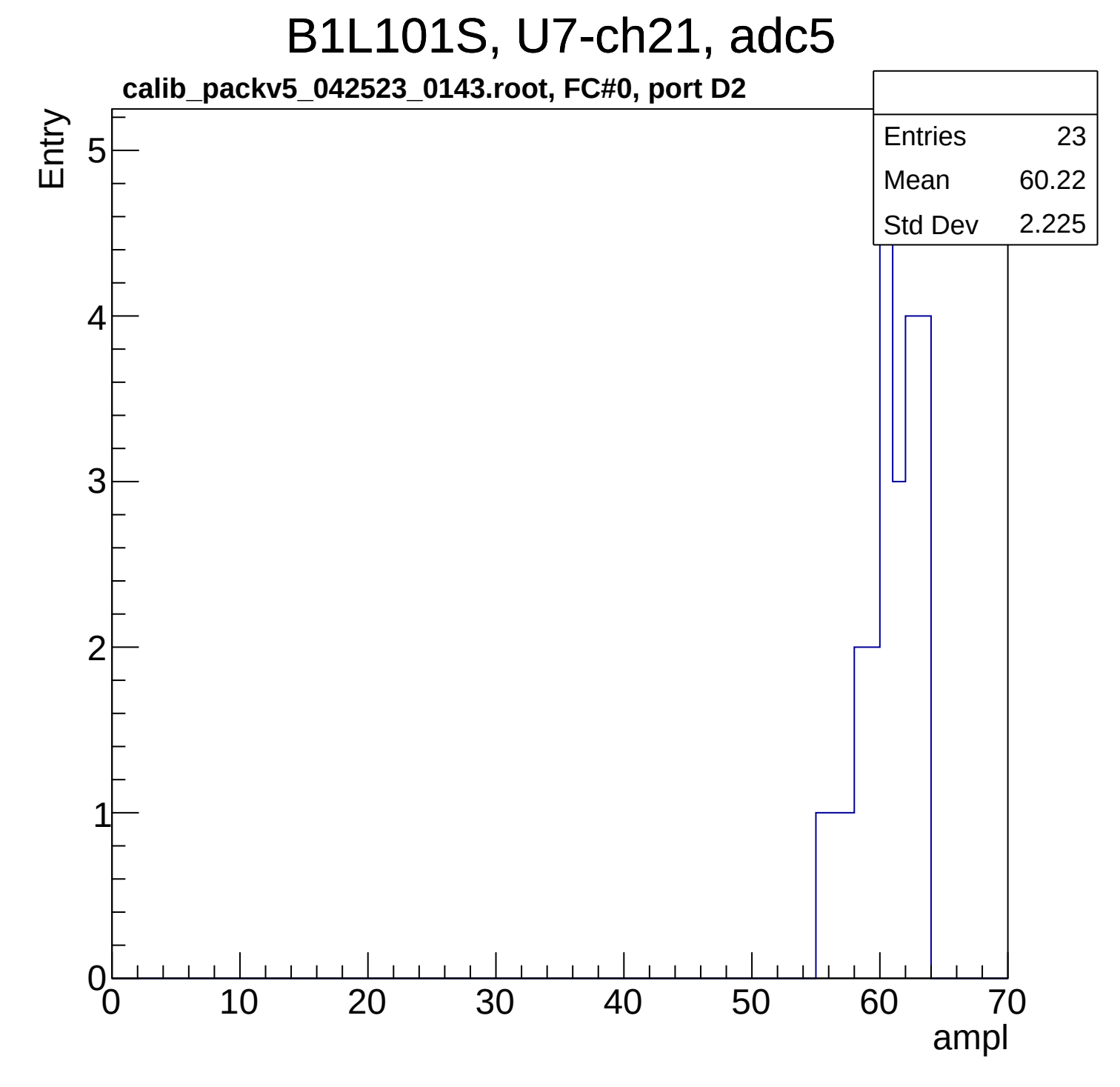

B1L101S, U7-ch21, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 32.02
Std Dev 3.031
Gaus mean : 32.3835
Gaus Width: 3.4176
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

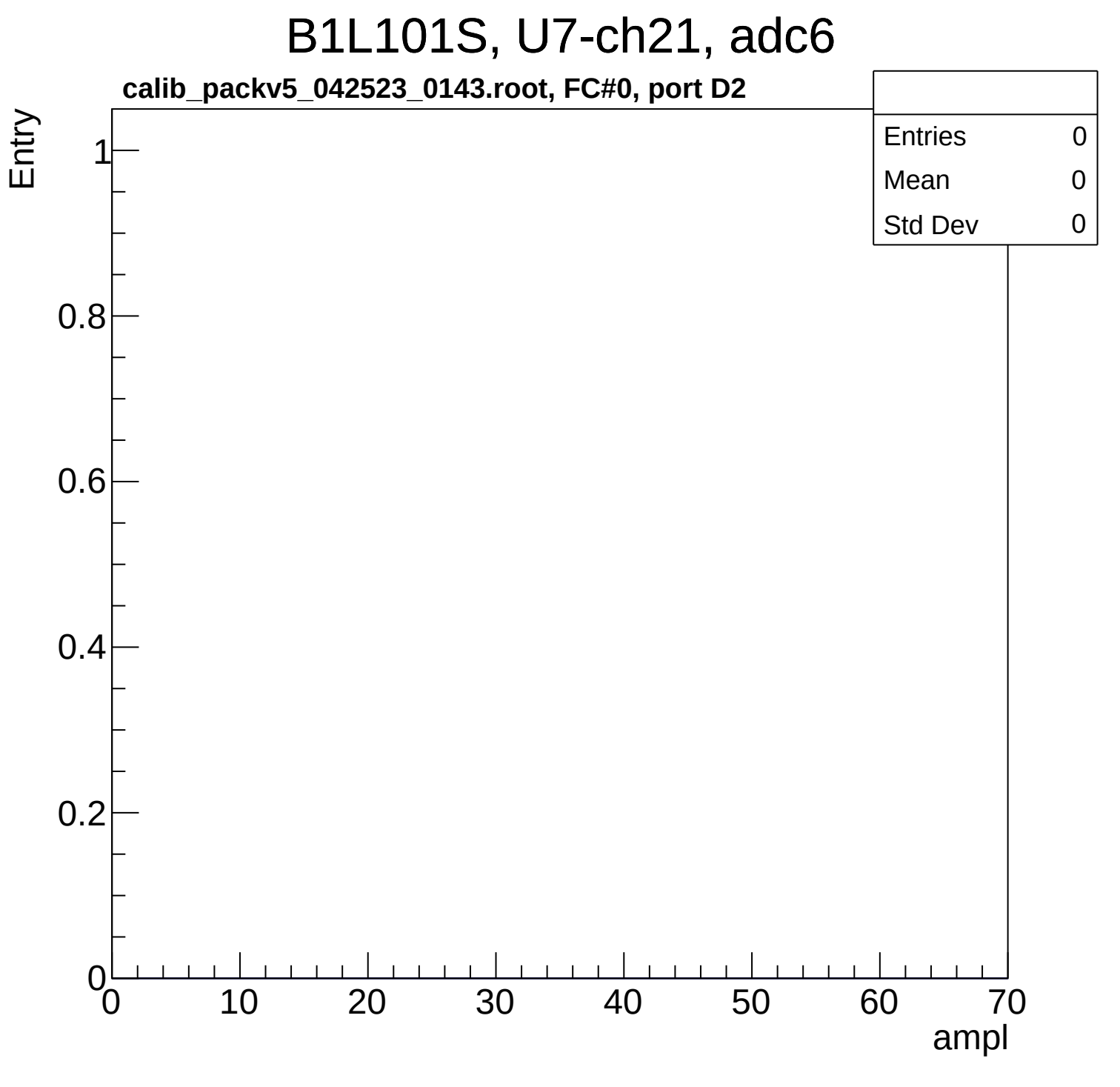

B1L101S, U7-ch21, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 80
Mean 38.45
Std Dev 3.681
Gaus mean : 38.9675
Gaus Width: 3.7226
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch21, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 45.65
Std Dev 2.544
Gaus mean : 45.9154
Gaus Width: 2.9711
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch21, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 51.86
Std Dev 2.961
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch21, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 57.48
Std Dev 7.912
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U7-ch21, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 23
Mean 60.22
Std Dev 2.225
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch21, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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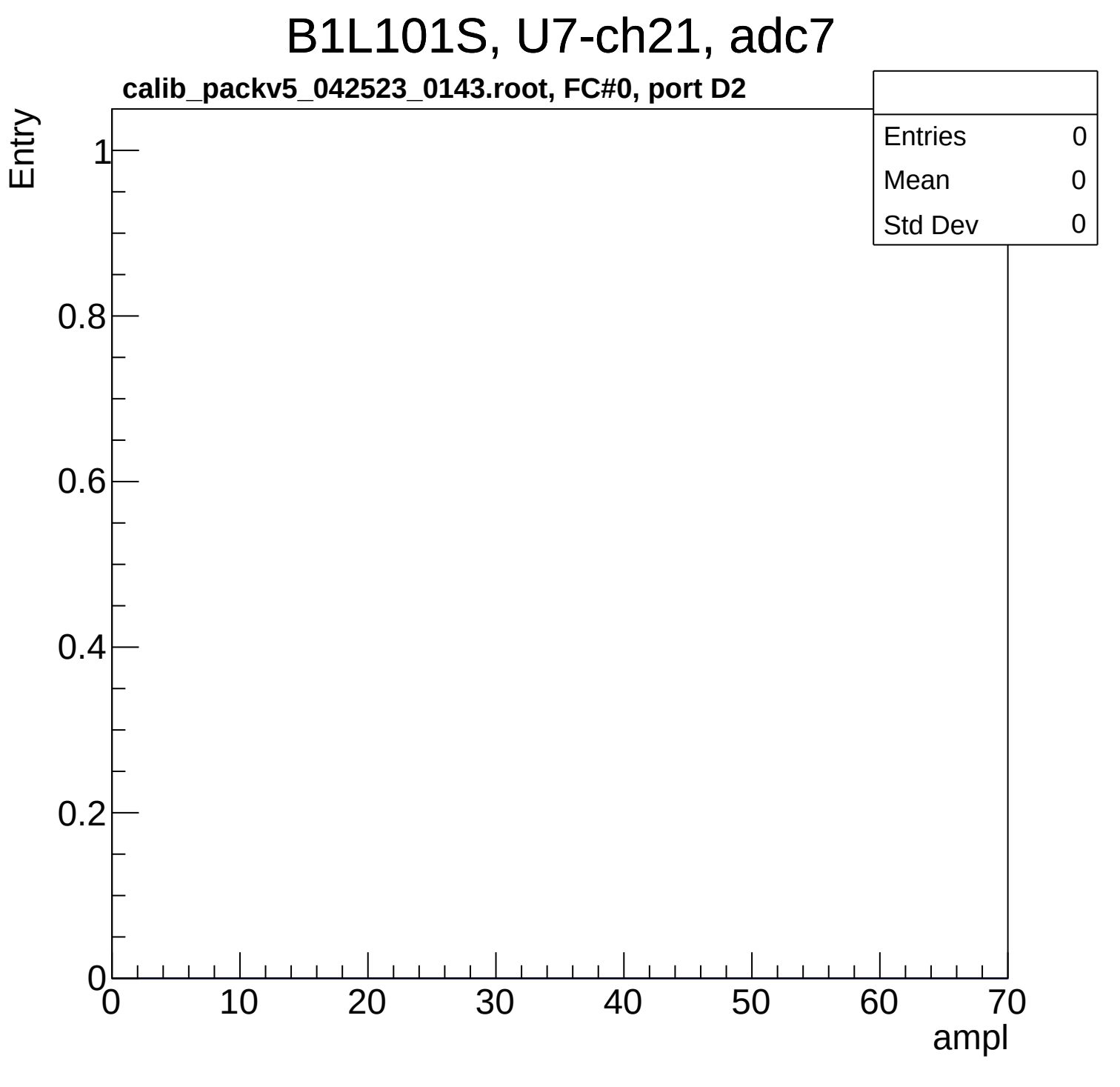
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch21, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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0.6
0.4
0.2
0
0
10
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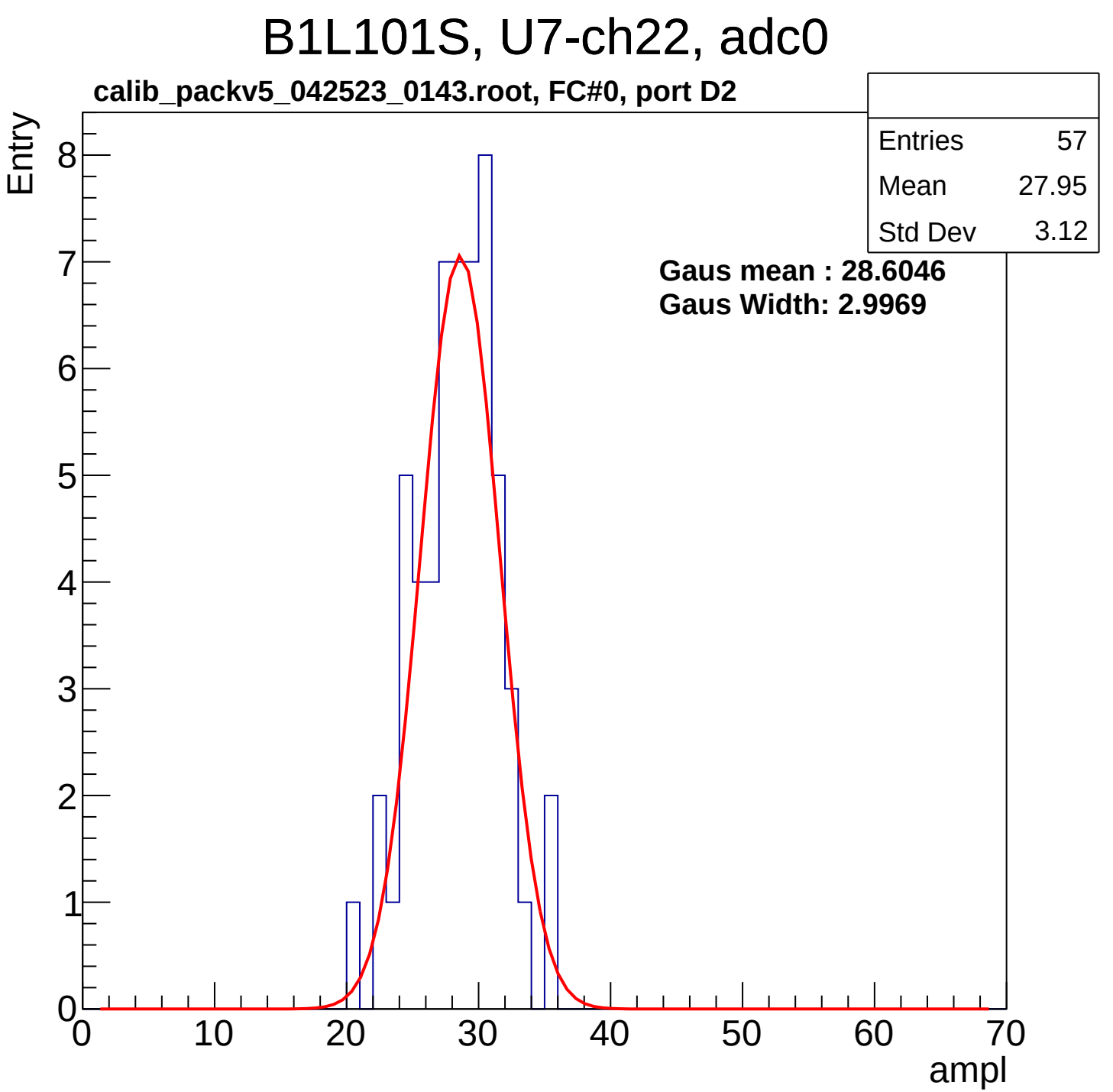
50
60
70
ampl


B1L101S, U7-ch22, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 27.95
Std Dev 3.12
Gaus mean : 28.6046
Gaus Width: 2.9969
Entry
ampl
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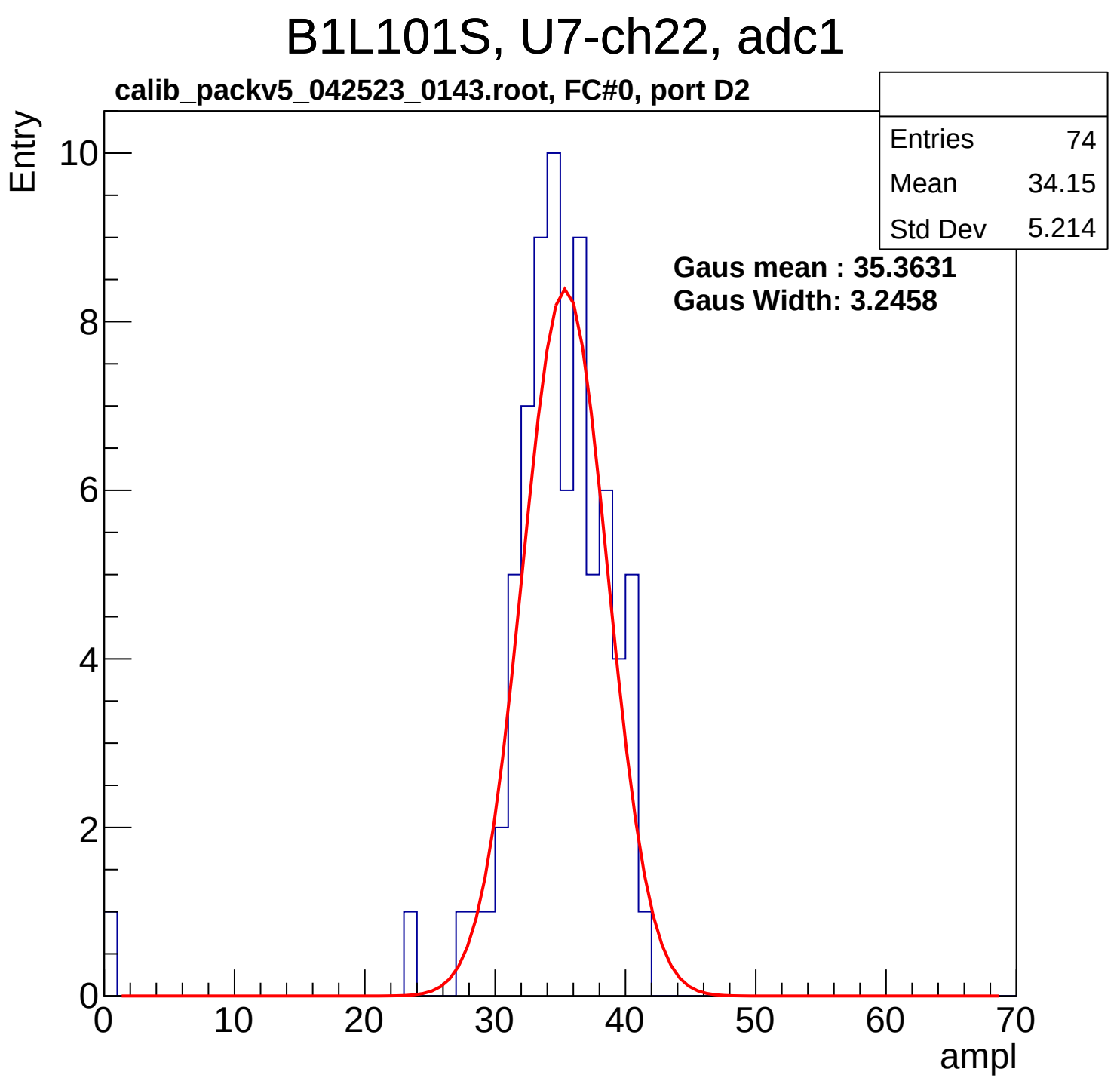
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch22, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 34.15
Std Dev 5.214
Gaus mean : 35.3631
Gaus Width: 3.2458
Entry
ampl
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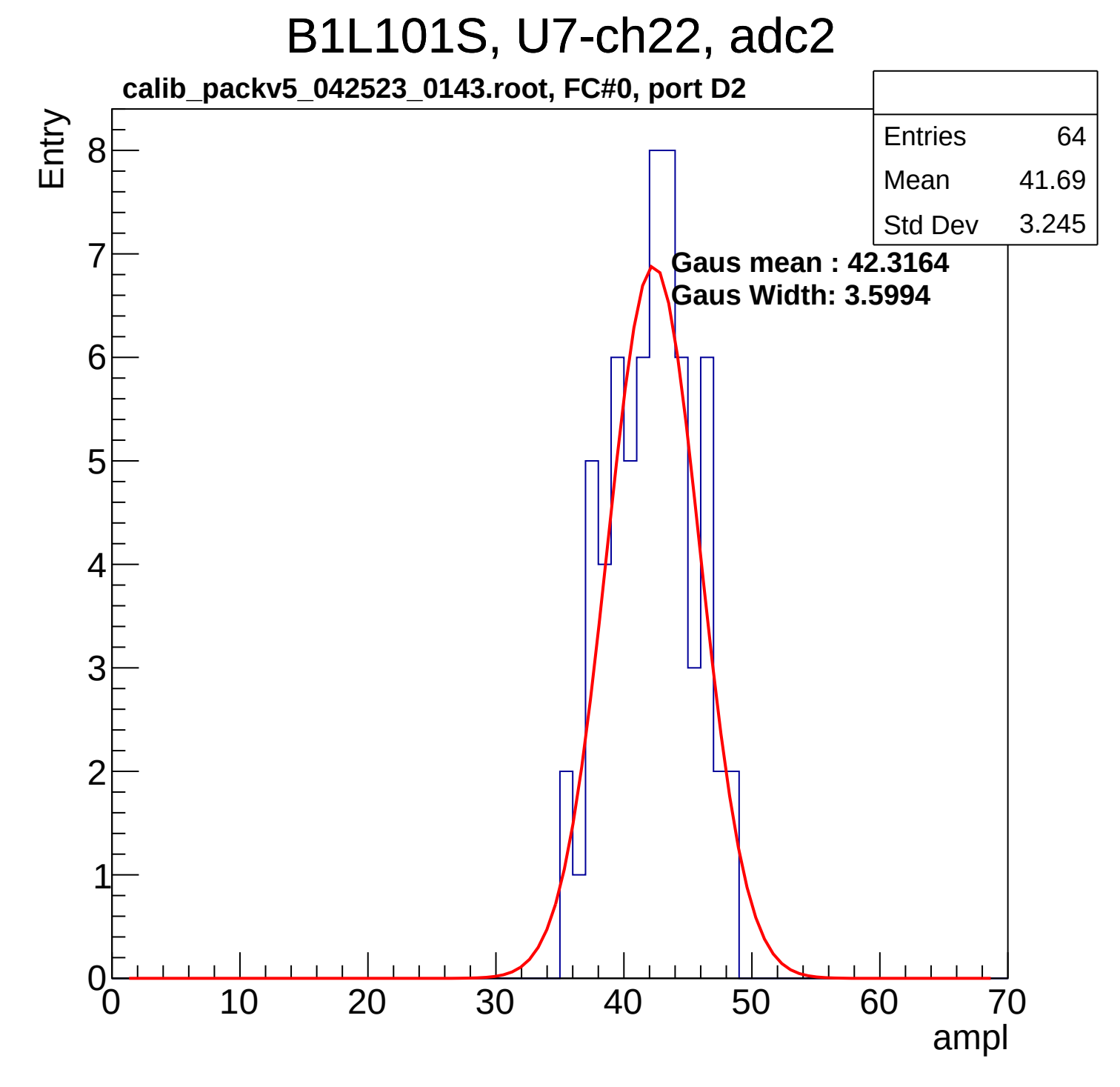
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch22, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 41.69
Std Dev 3.245
Gaus mean : 42.3164
Gaus Width: 3.5994
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
50
60
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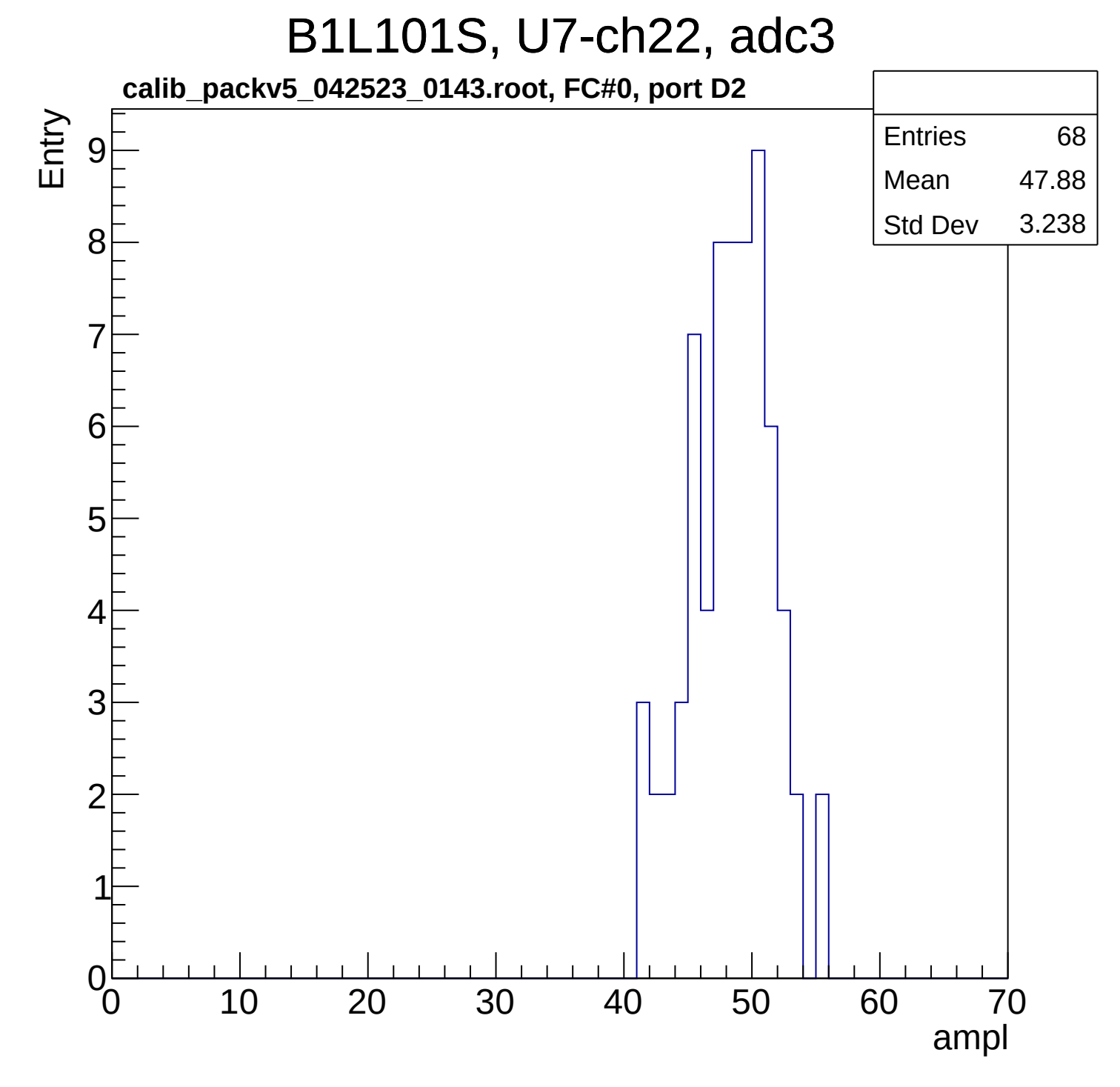
B1L101S, U7-ch22, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 47.88
Std Dev 3.238
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
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40
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60
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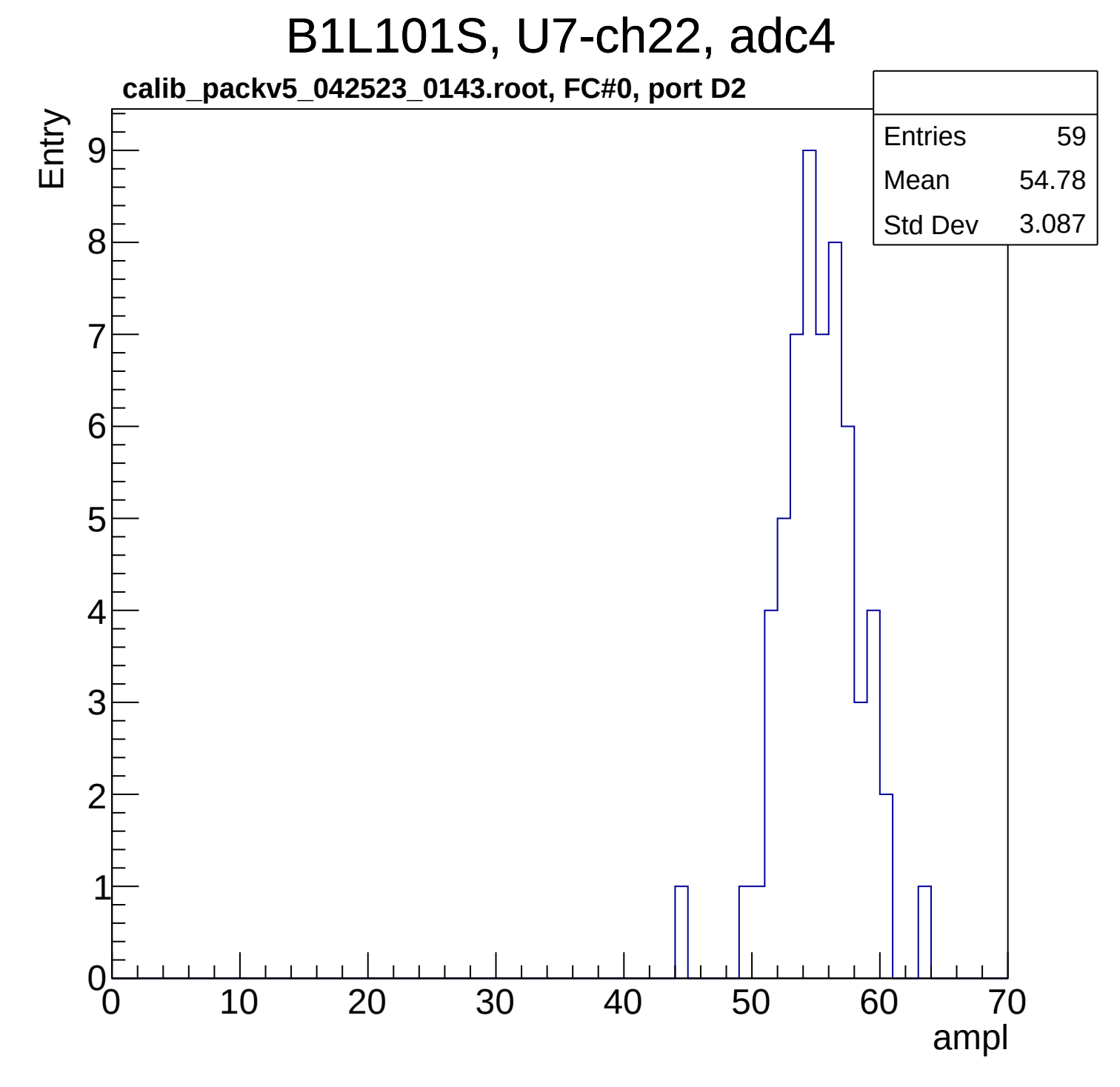
B1L101S, U7-ch22, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 54.78
Std Dev 3.087
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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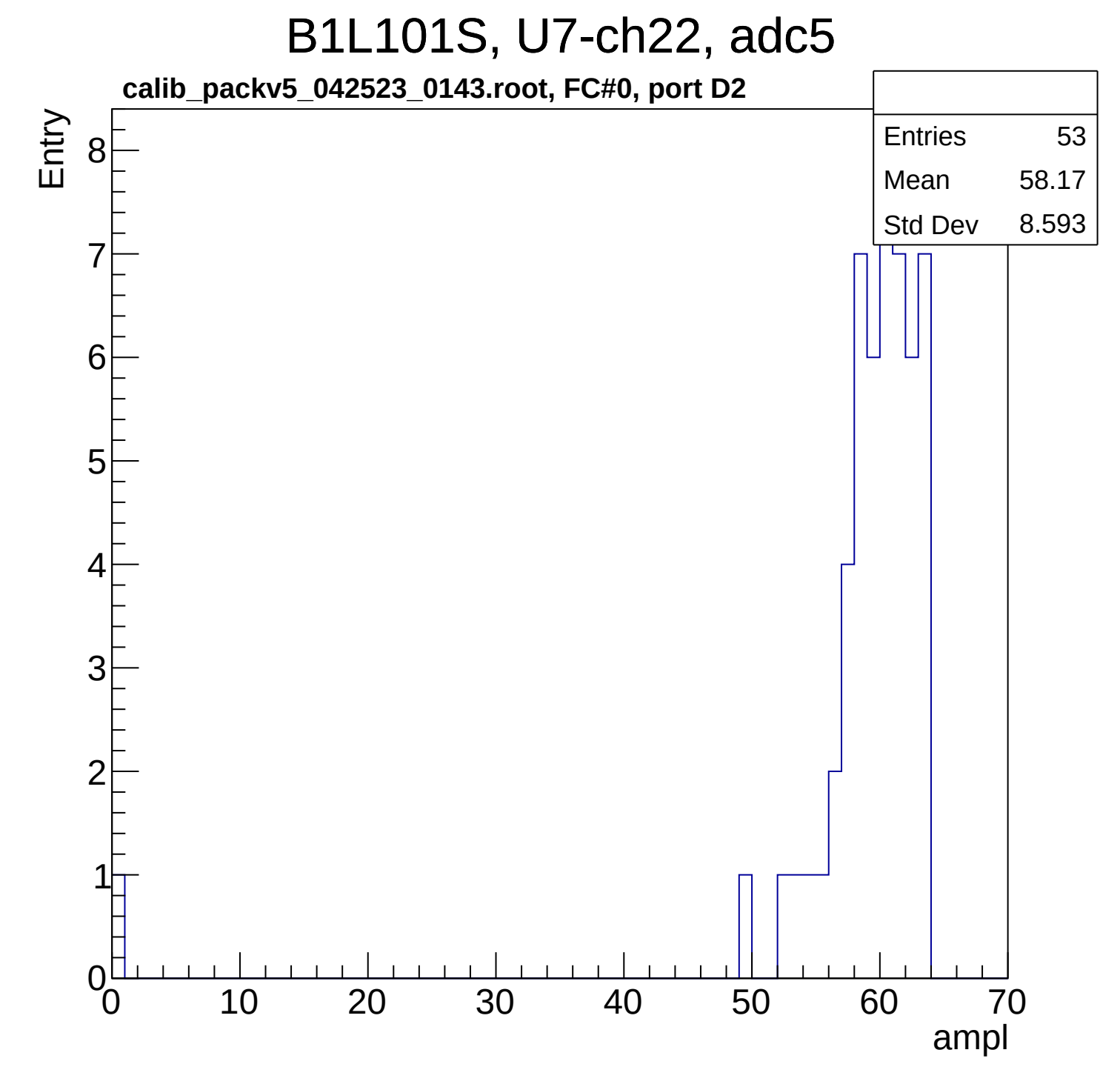
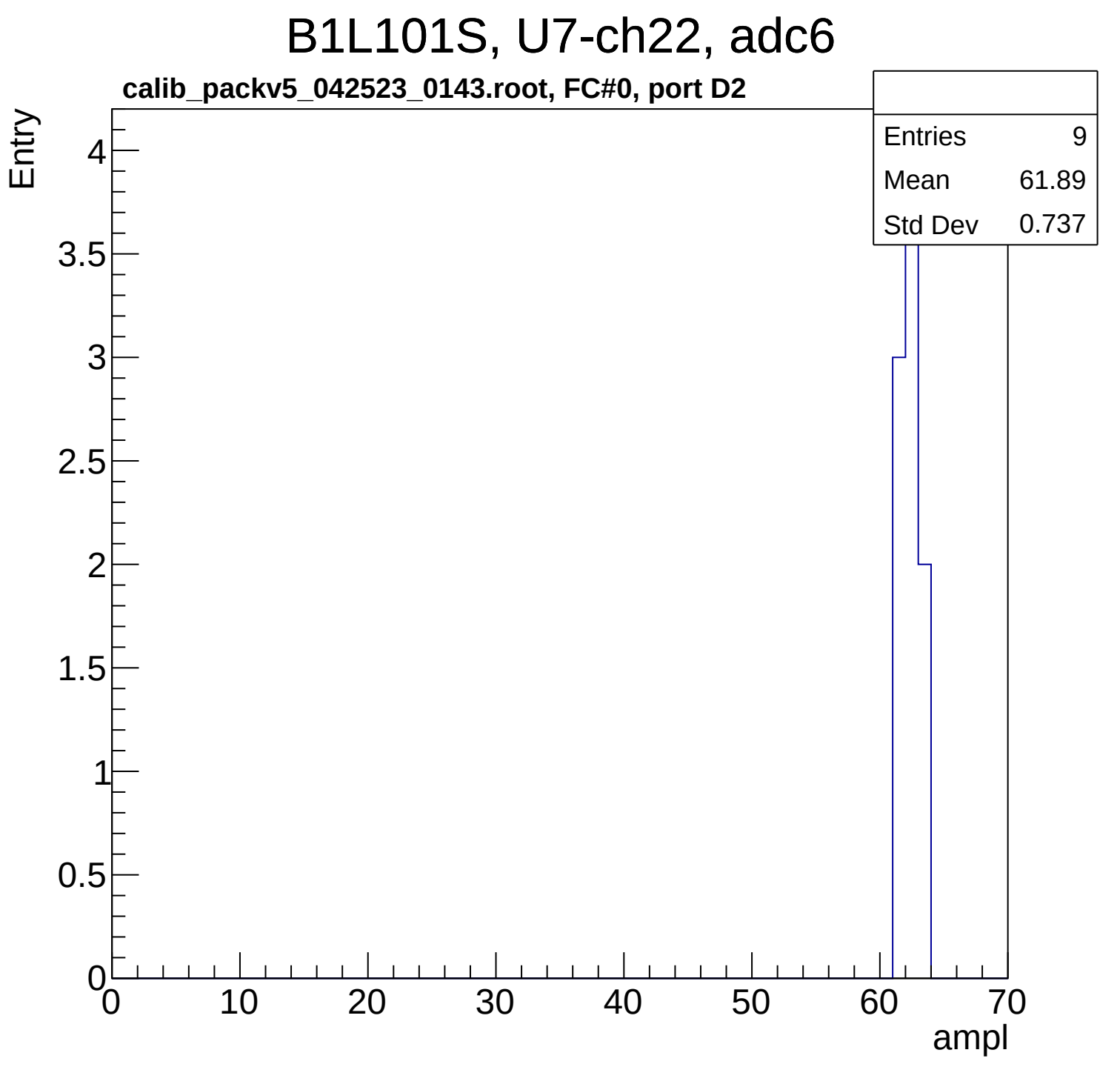

B1L101S, U7-ch22, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 58.17
Std Dev 8.593
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch22, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 61.89
Std Dev 0.737
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
10
20
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40
50
60
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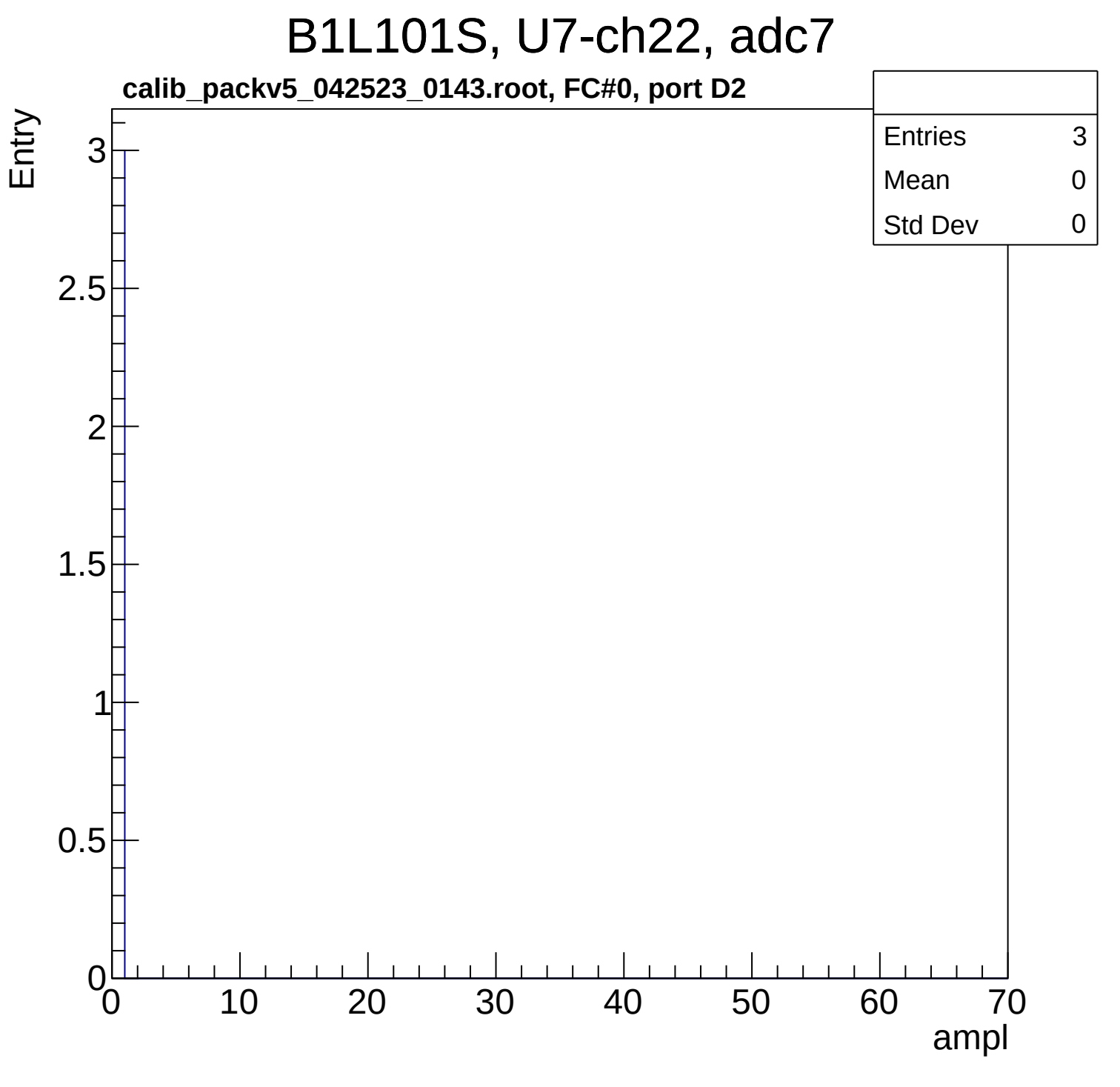
B1L101S, U7-ch22, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 0
Std Dev 0
Entry
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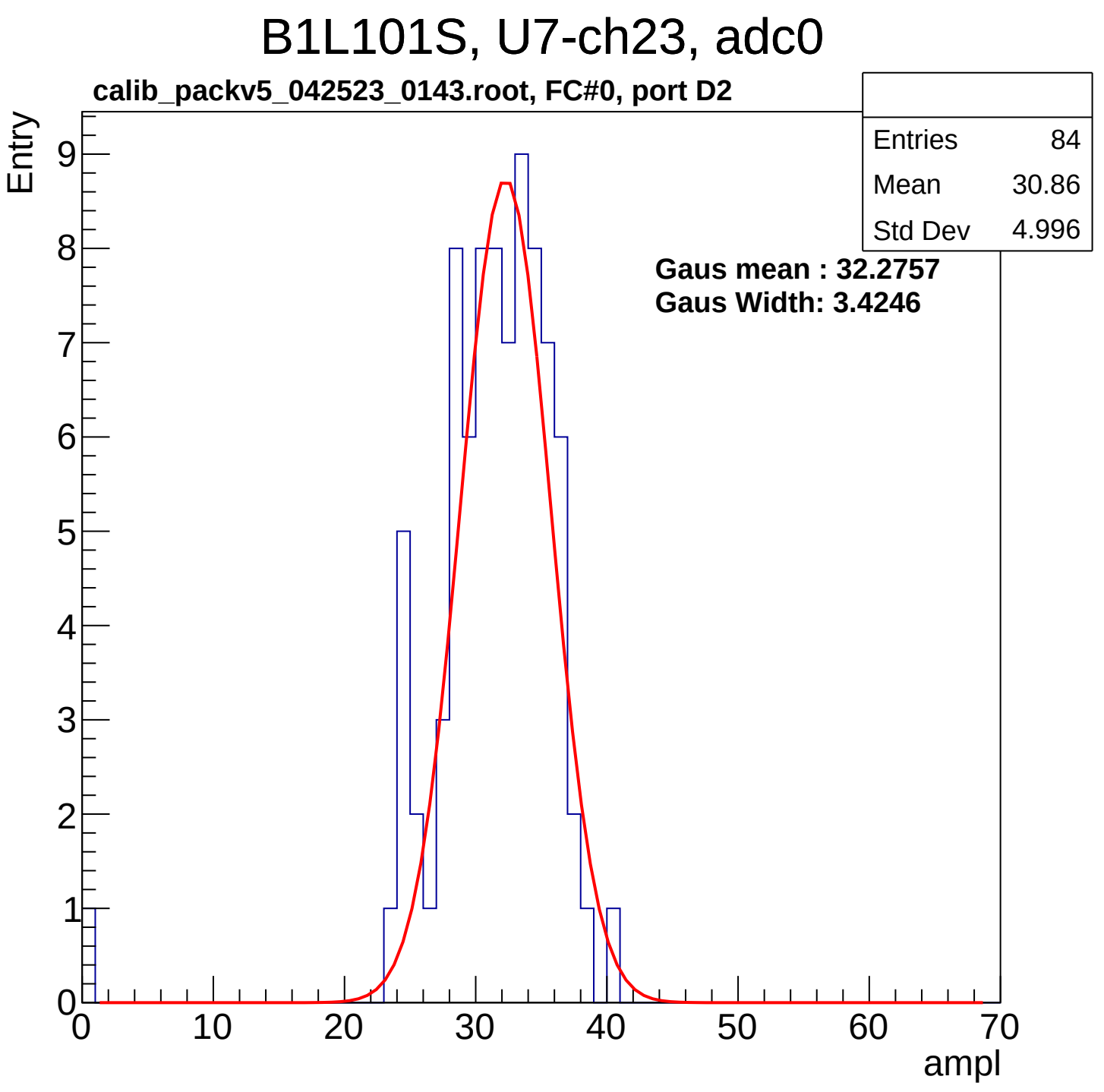
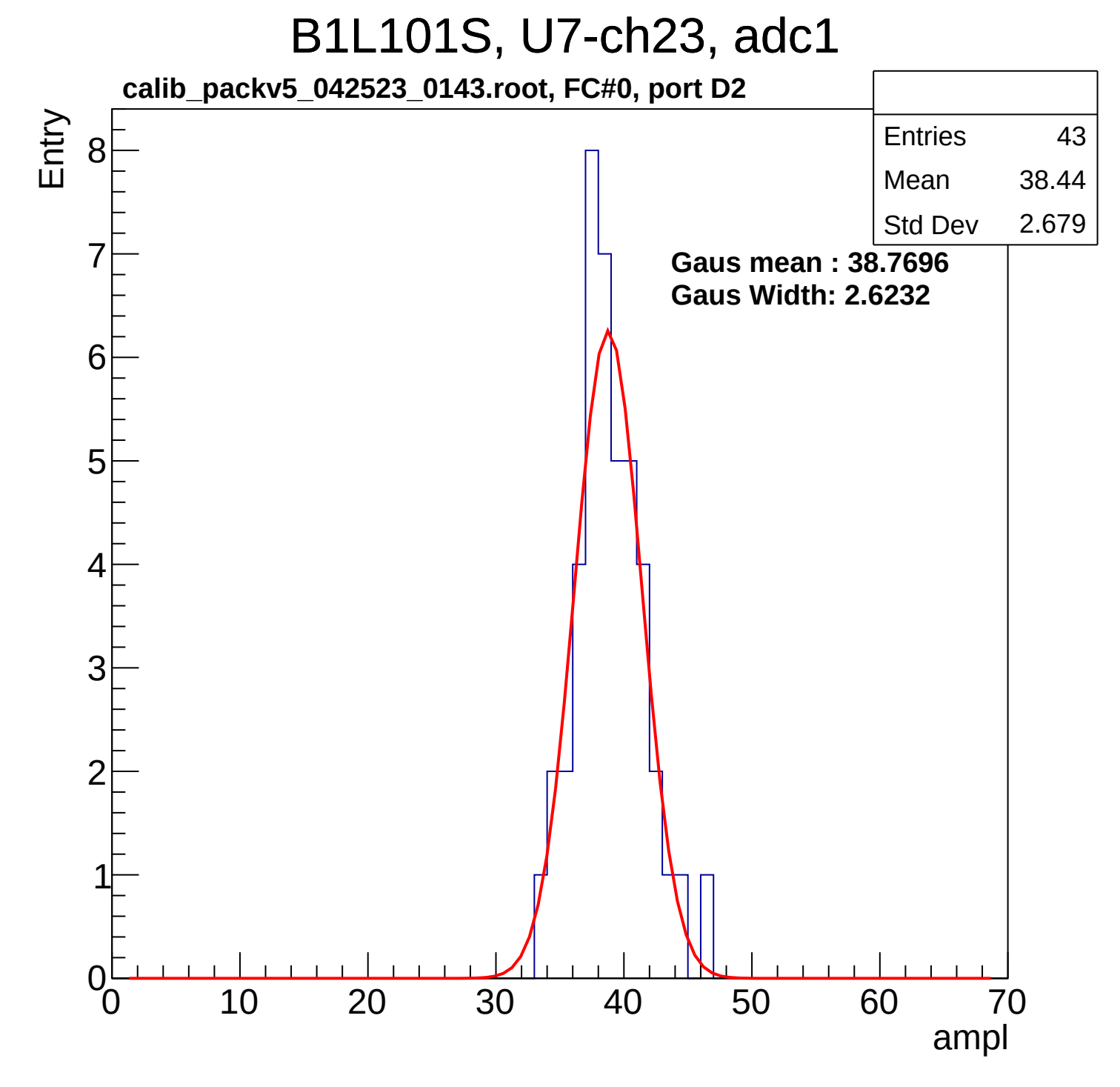
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch23, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 84
Mean 30.86
Std Dev 4.996
Gaus mean : 32.2757
Gaus Width: 3.4246
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch23, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 43
Mean 38.44
Std Dev 2.679
Gaus mean : 38.7696
Gaus Width: 2.6232
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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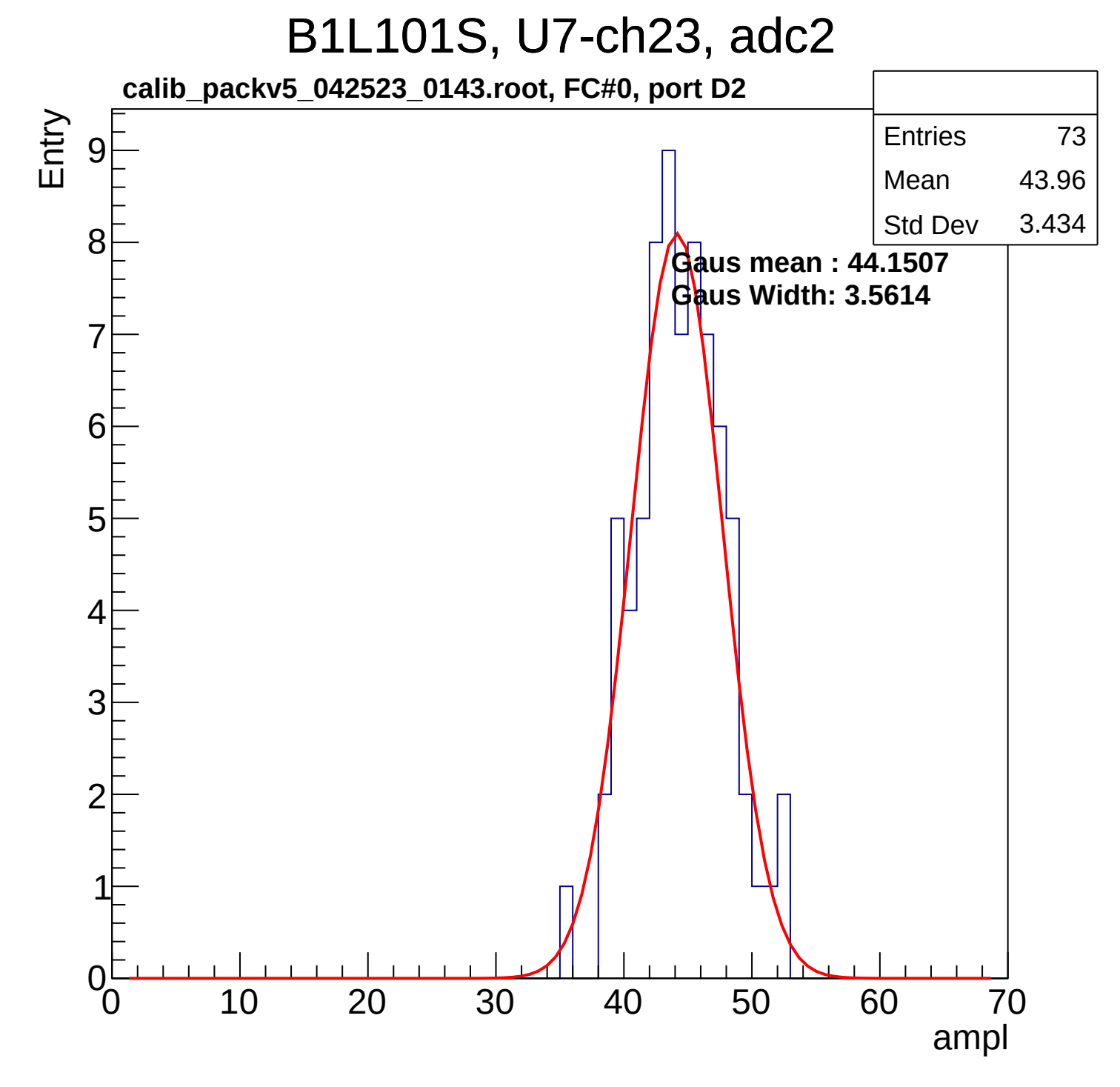
B1L101S, U7-ch23, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 43.96
Std Dev 3.434
Gaus mean : 44.1507
Gaus Width: 3.5614
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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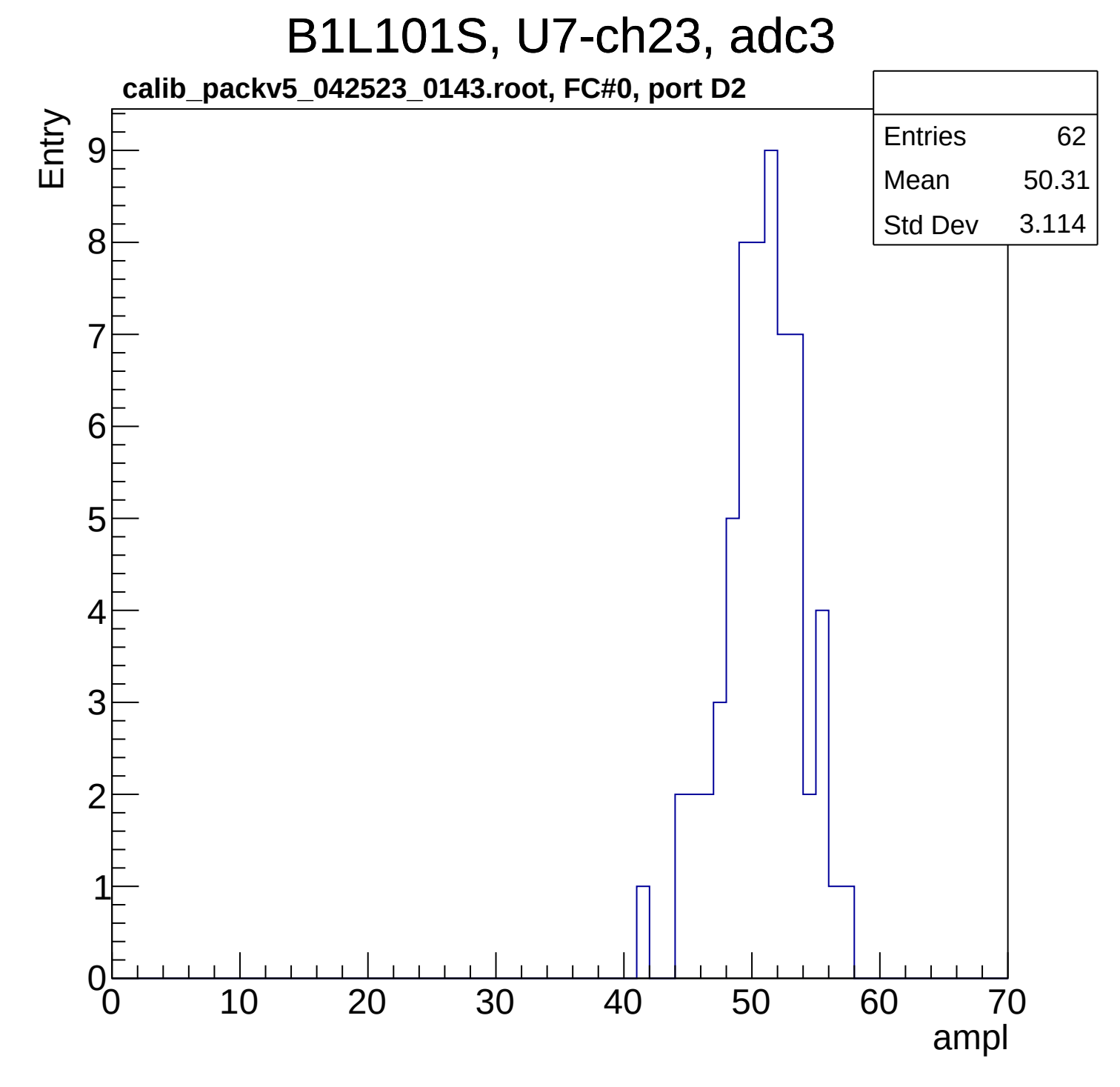
B1L101S, U7-ch23, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 50.31
Std Dev 3.114
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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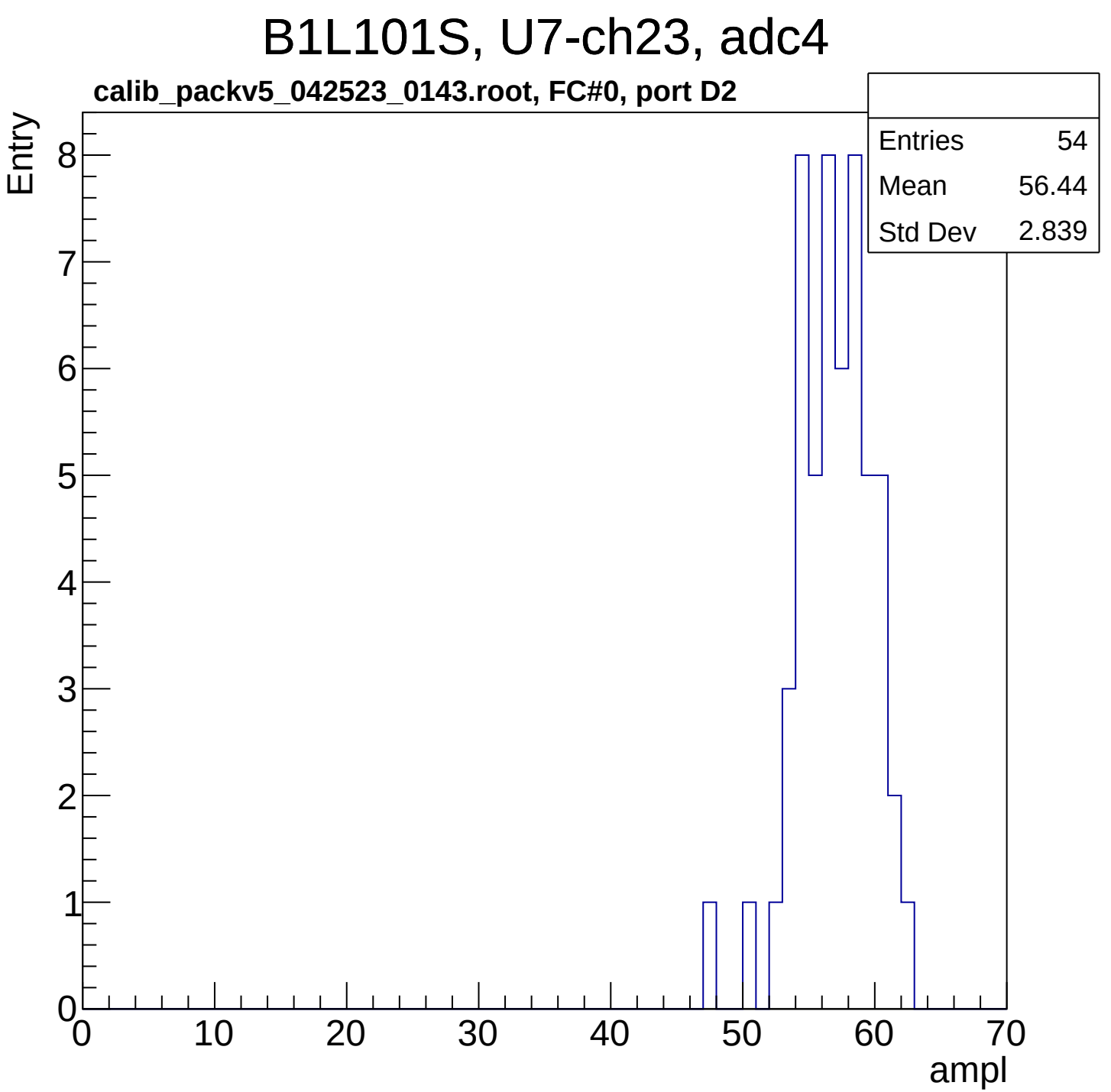
B1L101S, U7-ch23, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 56.44
Std Dev 2.839
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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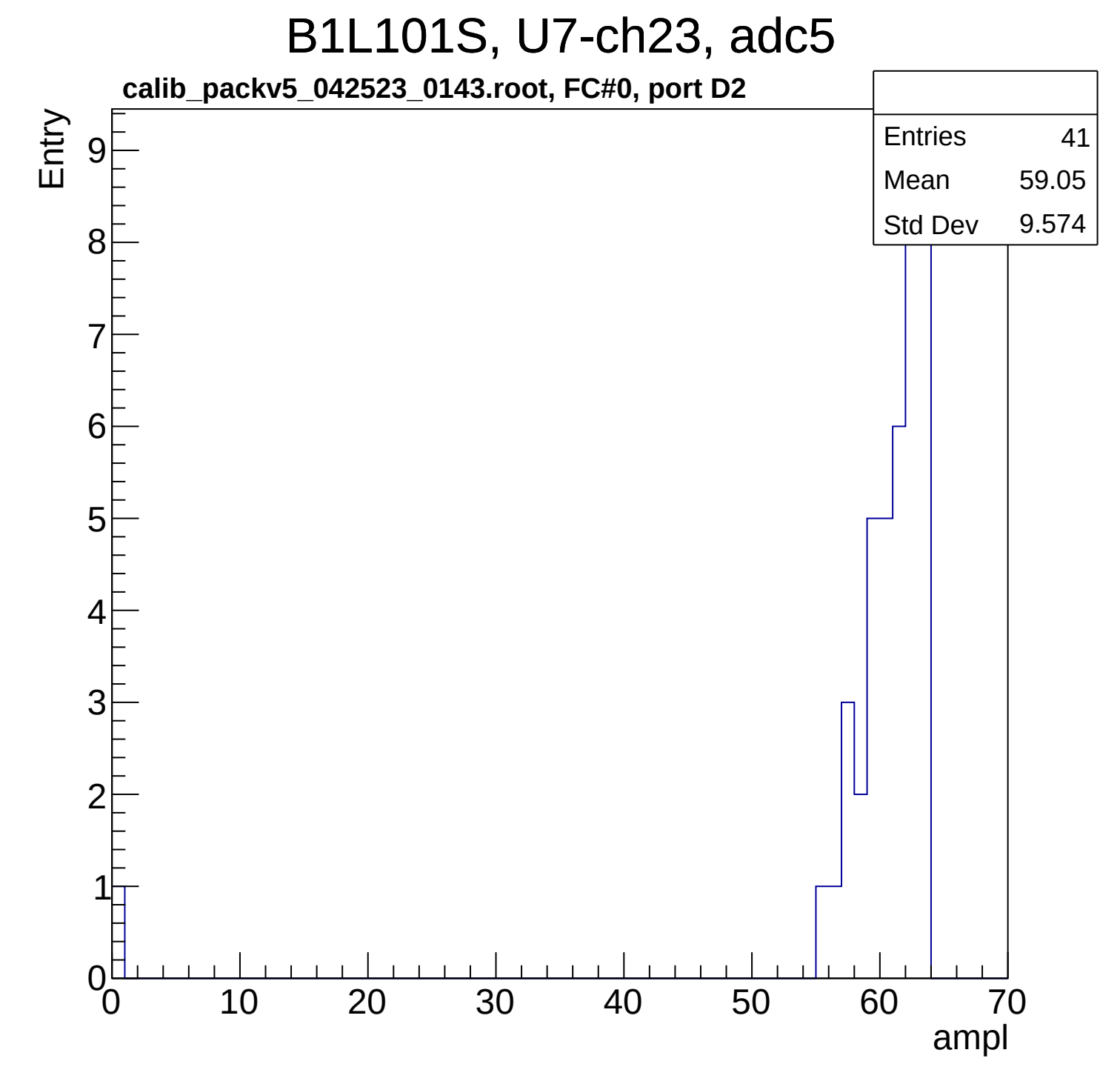
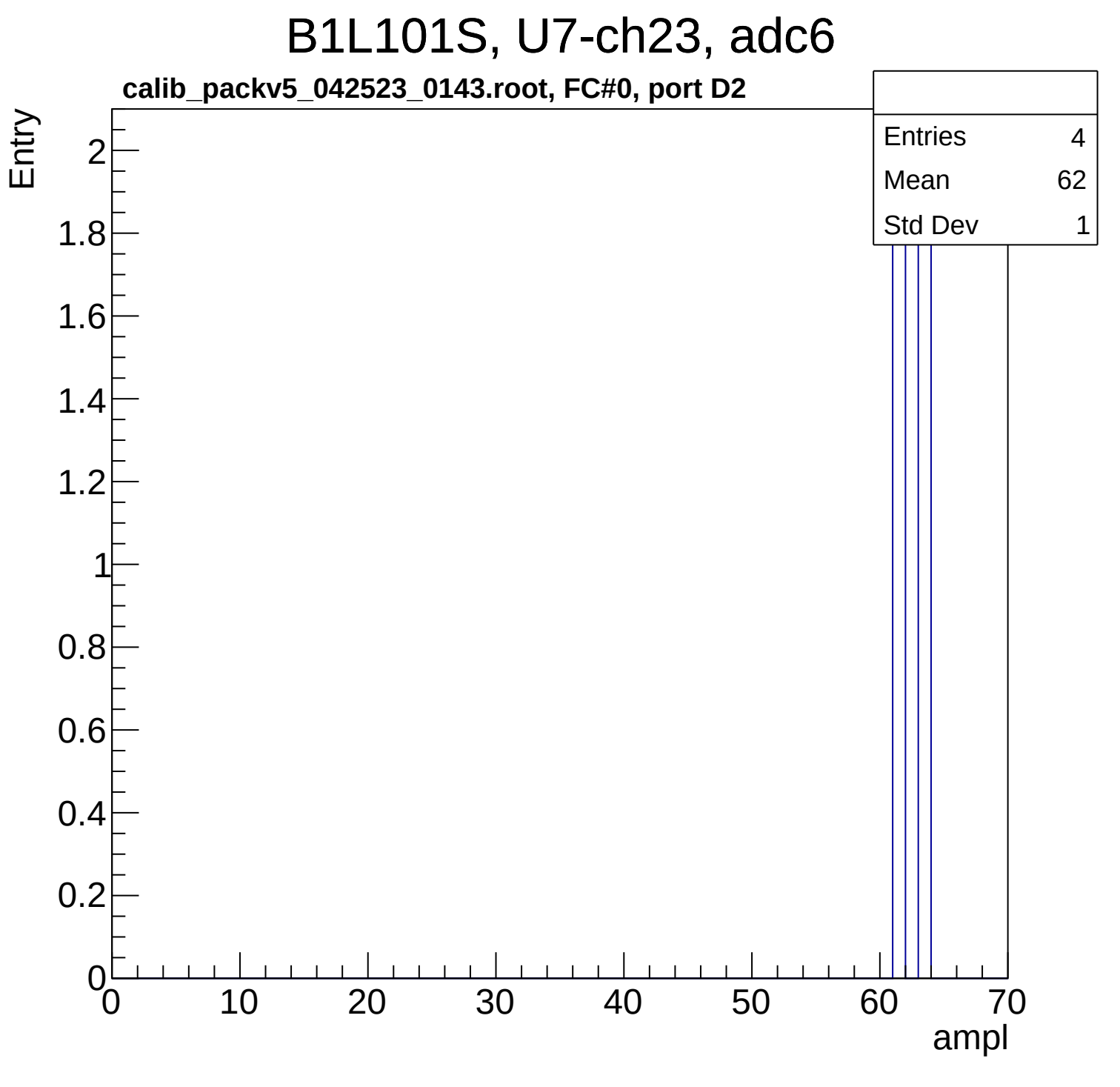
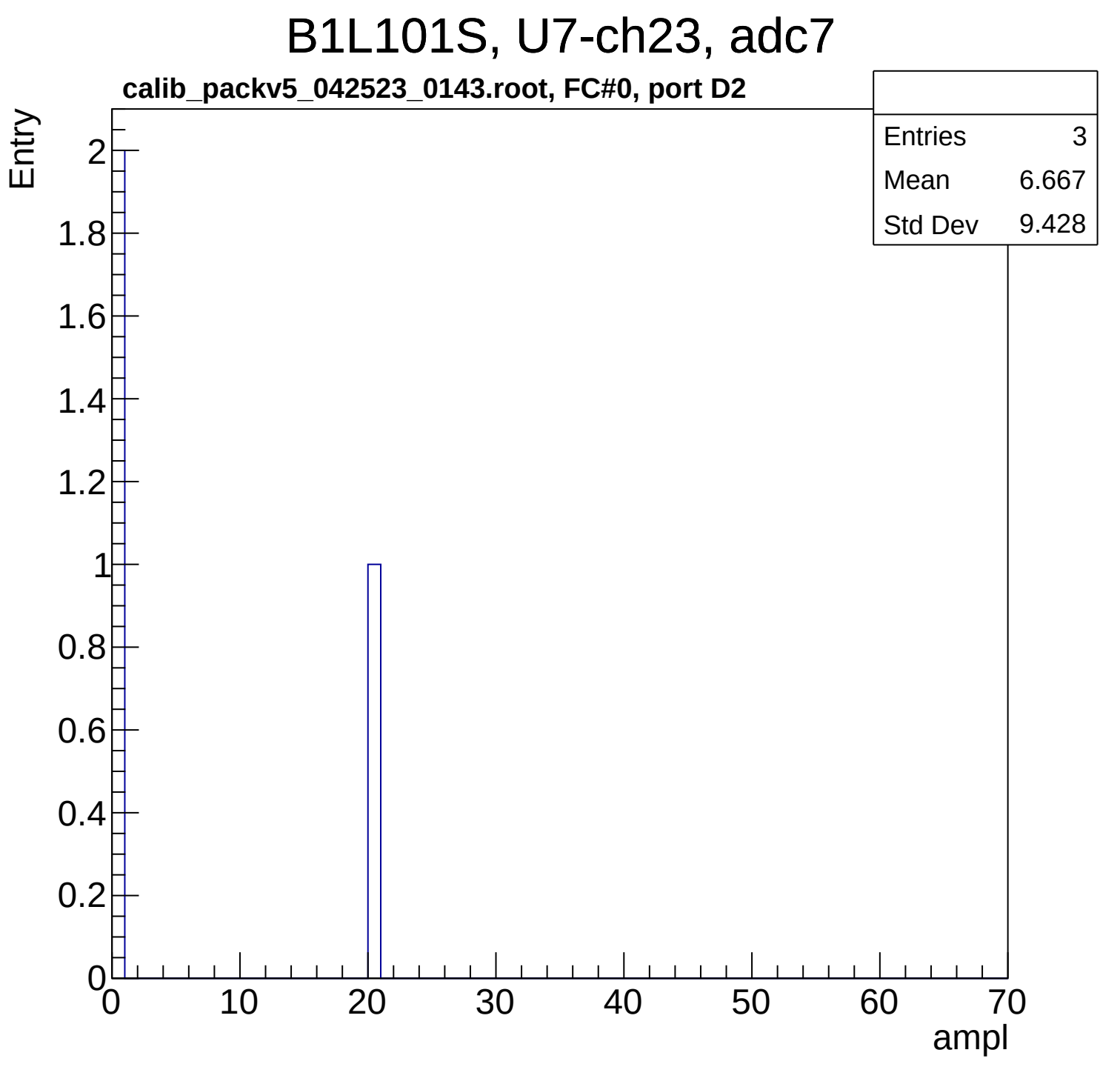
40
50
60
70


B1L101S, U7-ch23, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 41
Mean 59.05
Std Dev 9.574
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch23, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 62
Std Dev 1
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U7-ch23, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 6.667
Std Dev 9.428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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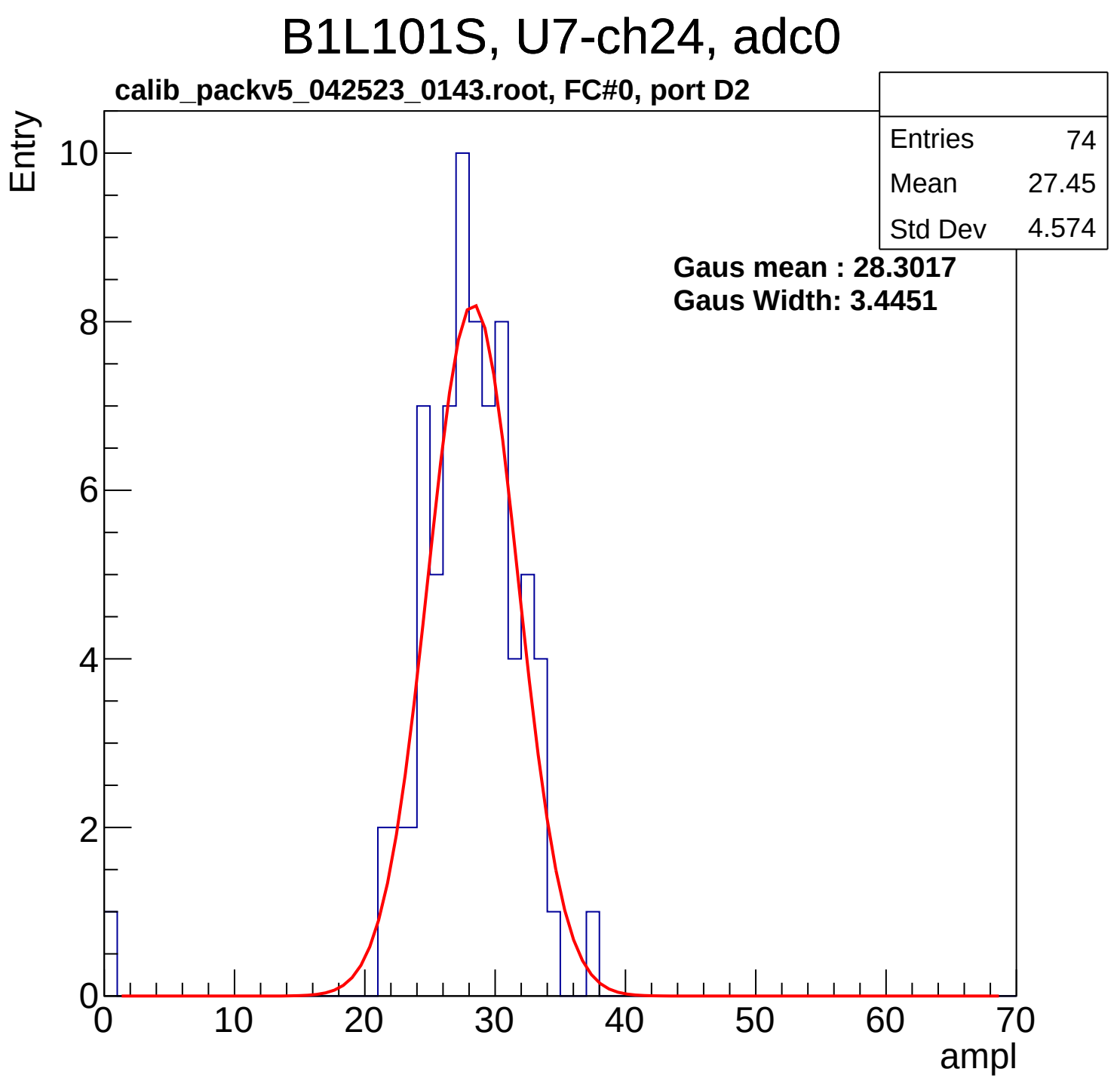
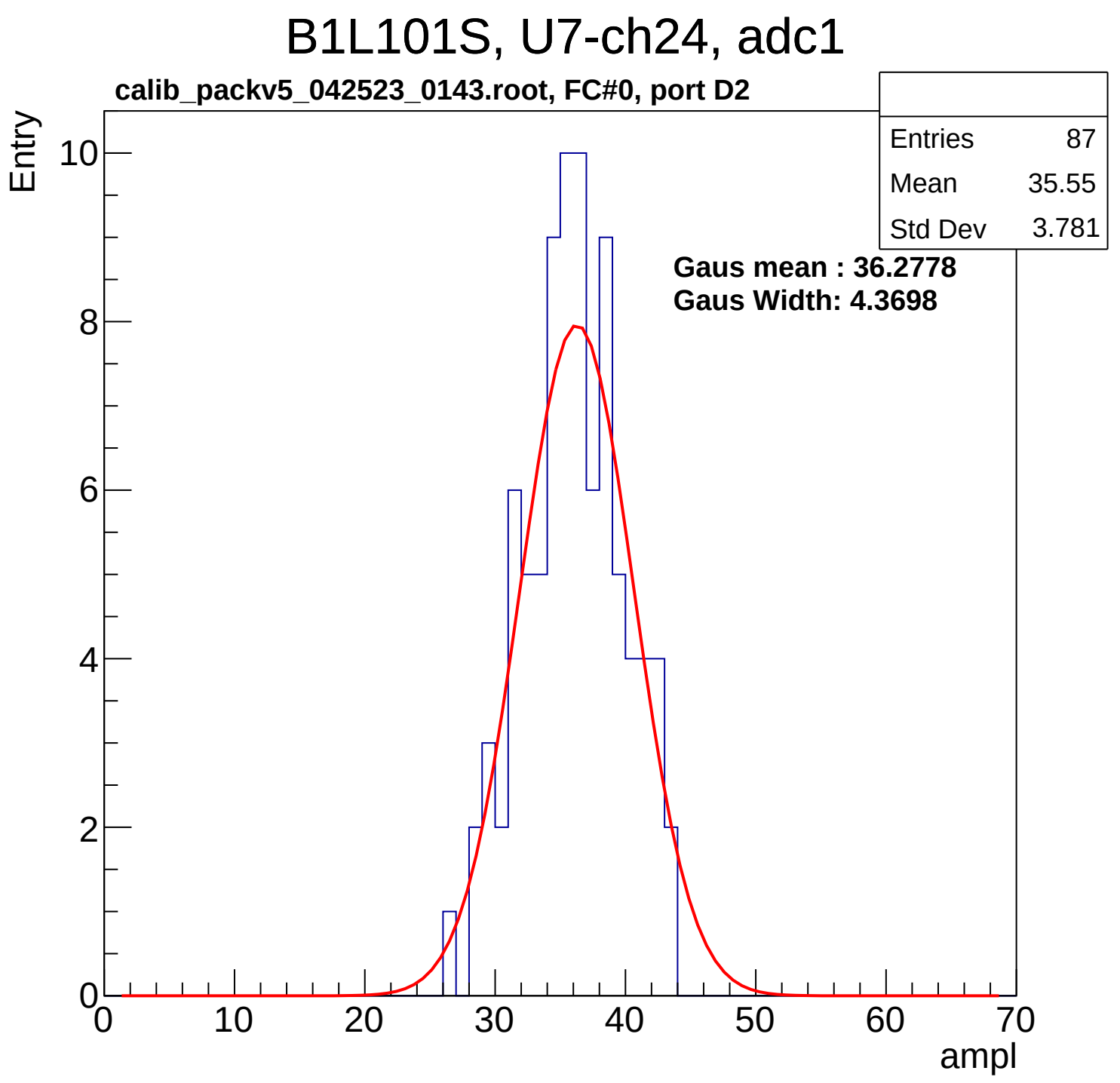
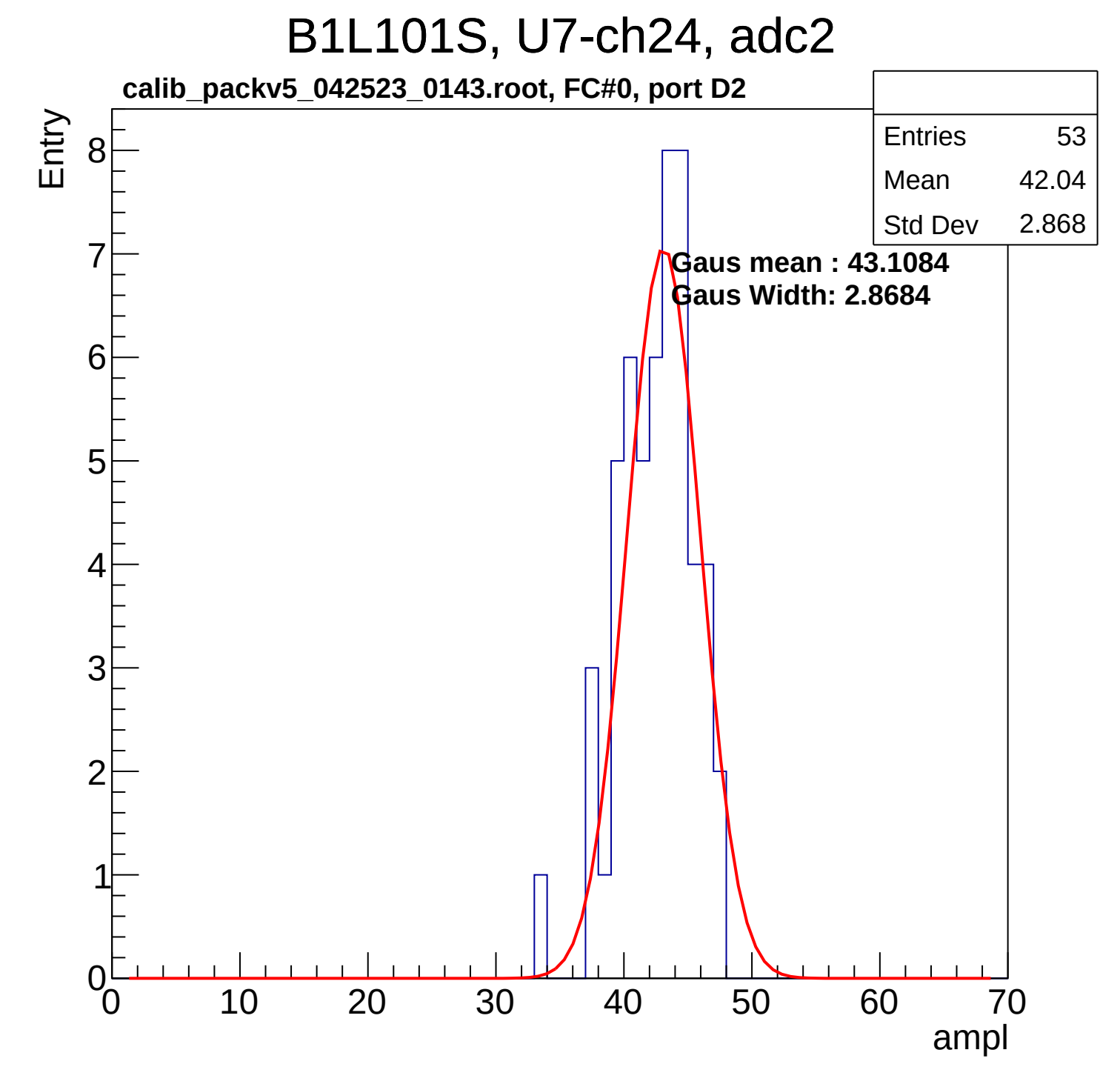
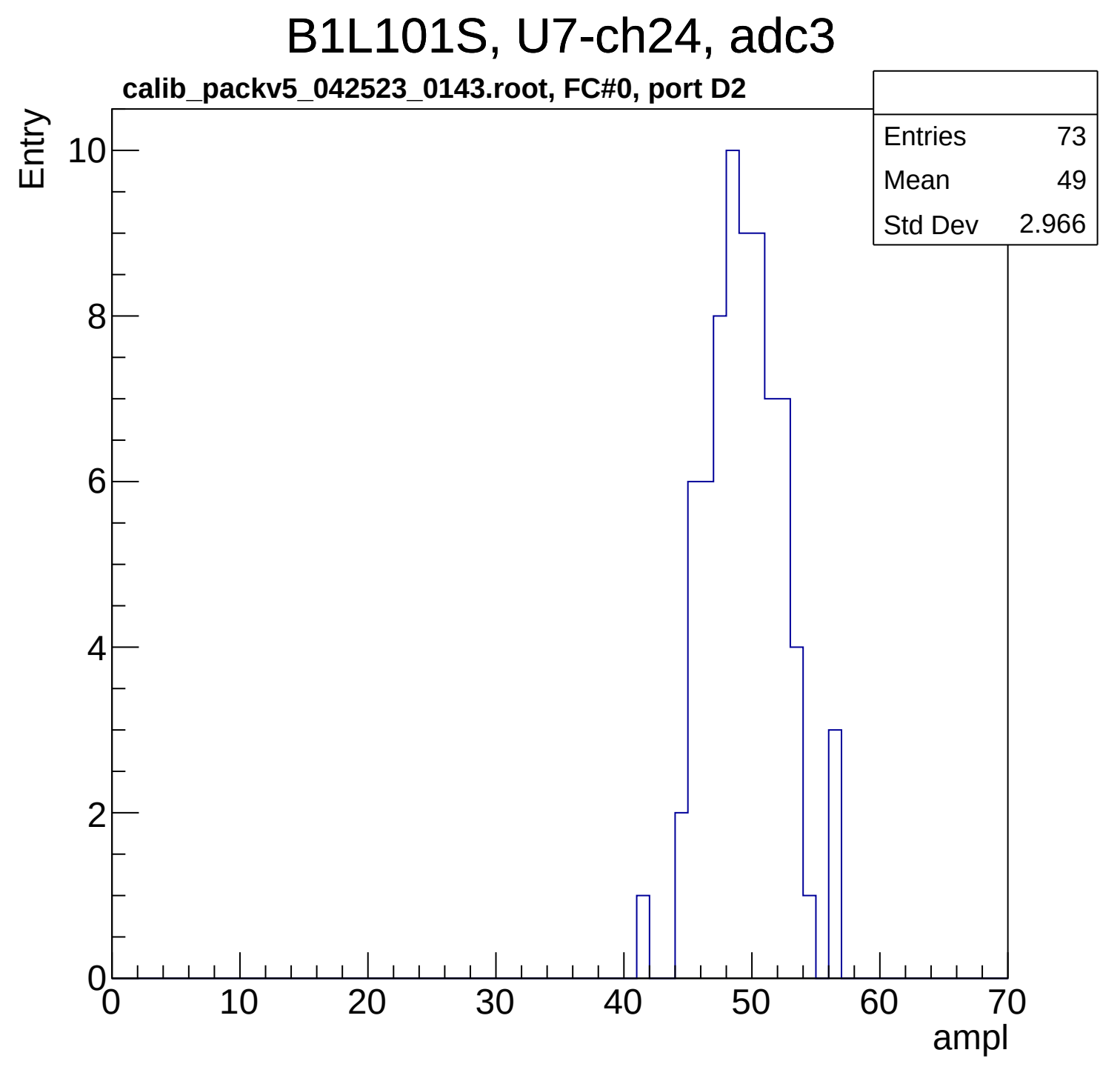
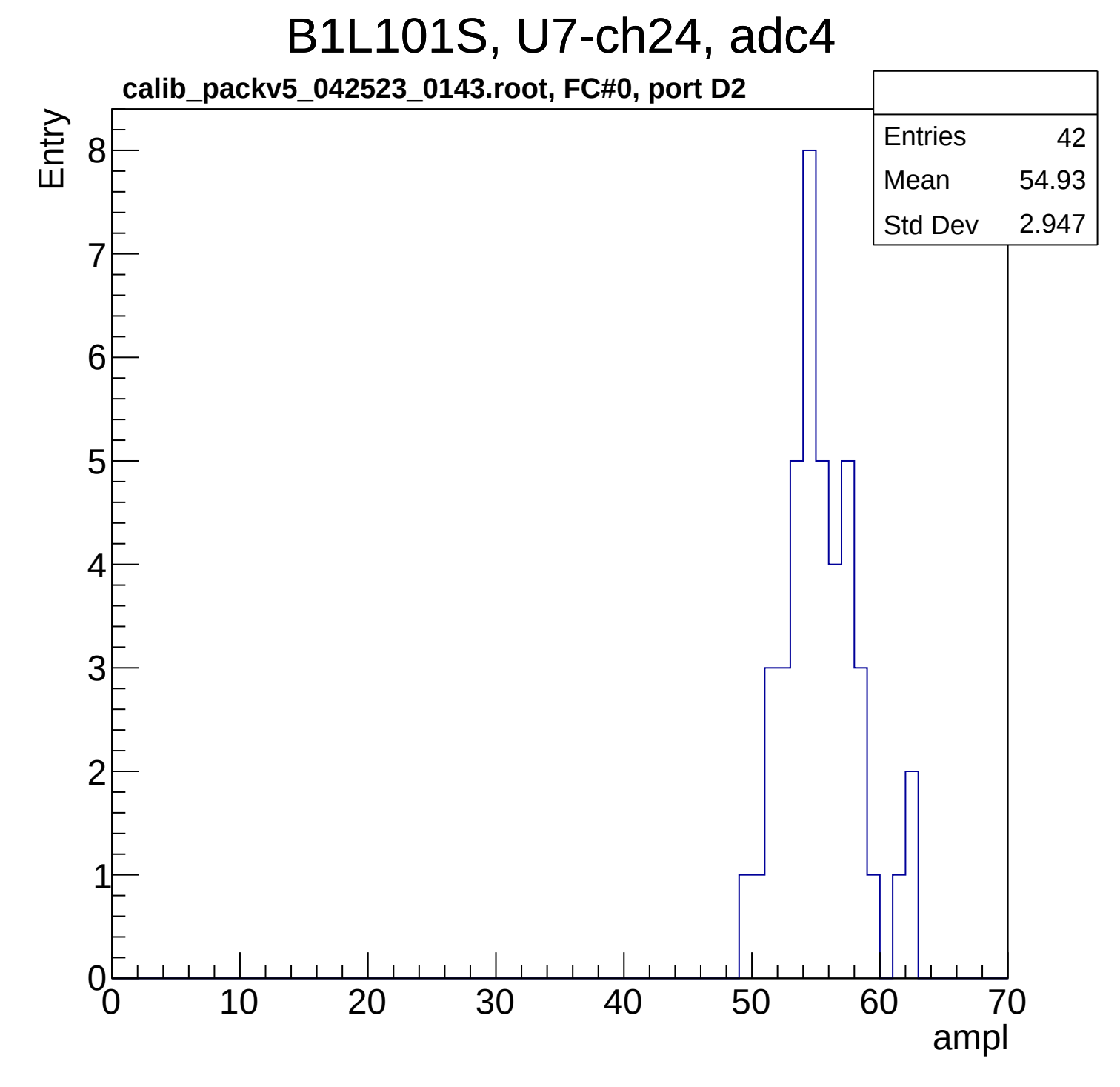
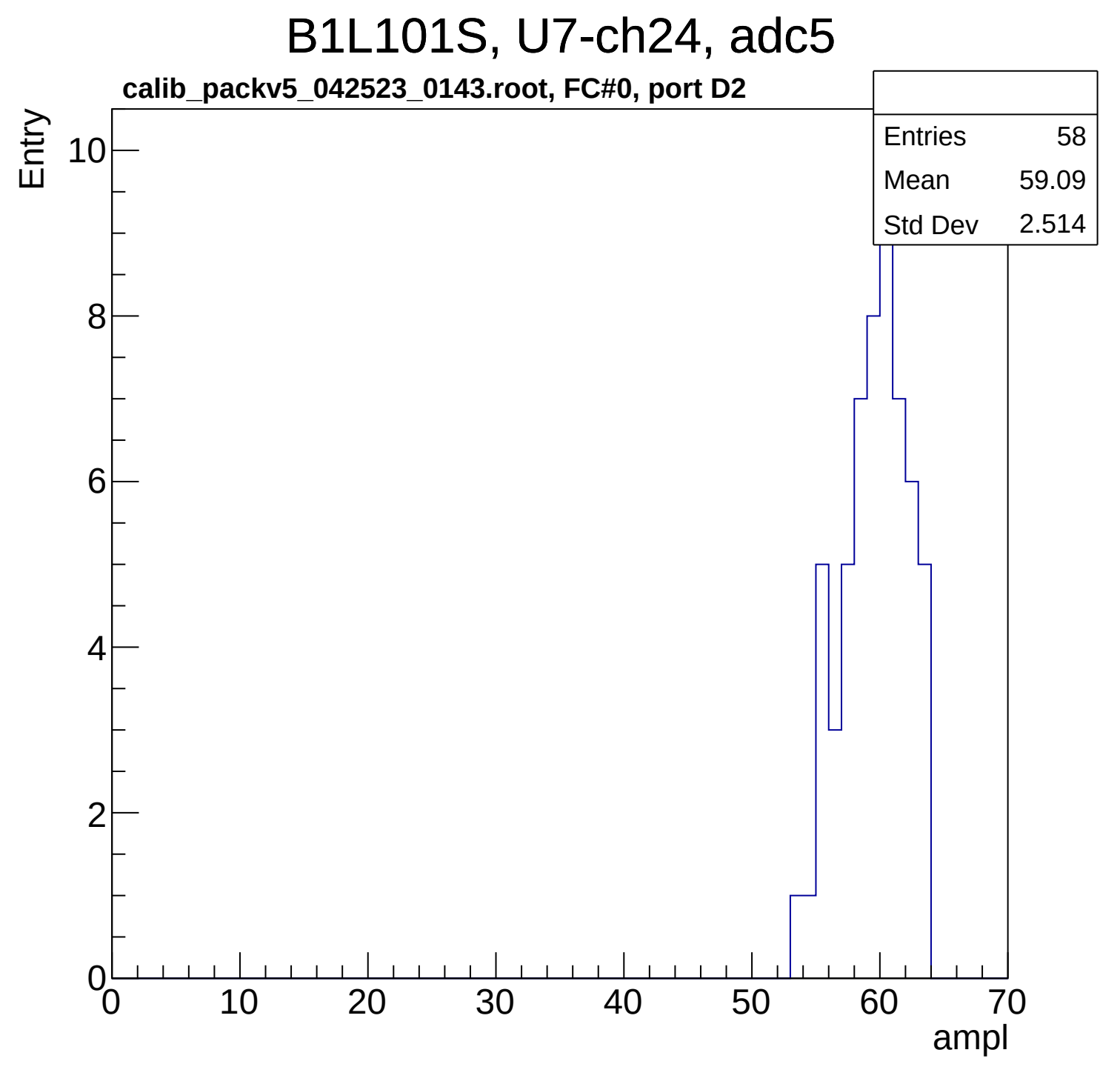

B1L101S, U7-ch24, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 27.45
Std Dev 4.574
Gaus mean : 28.3017
Gaus Width: 3.4451
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

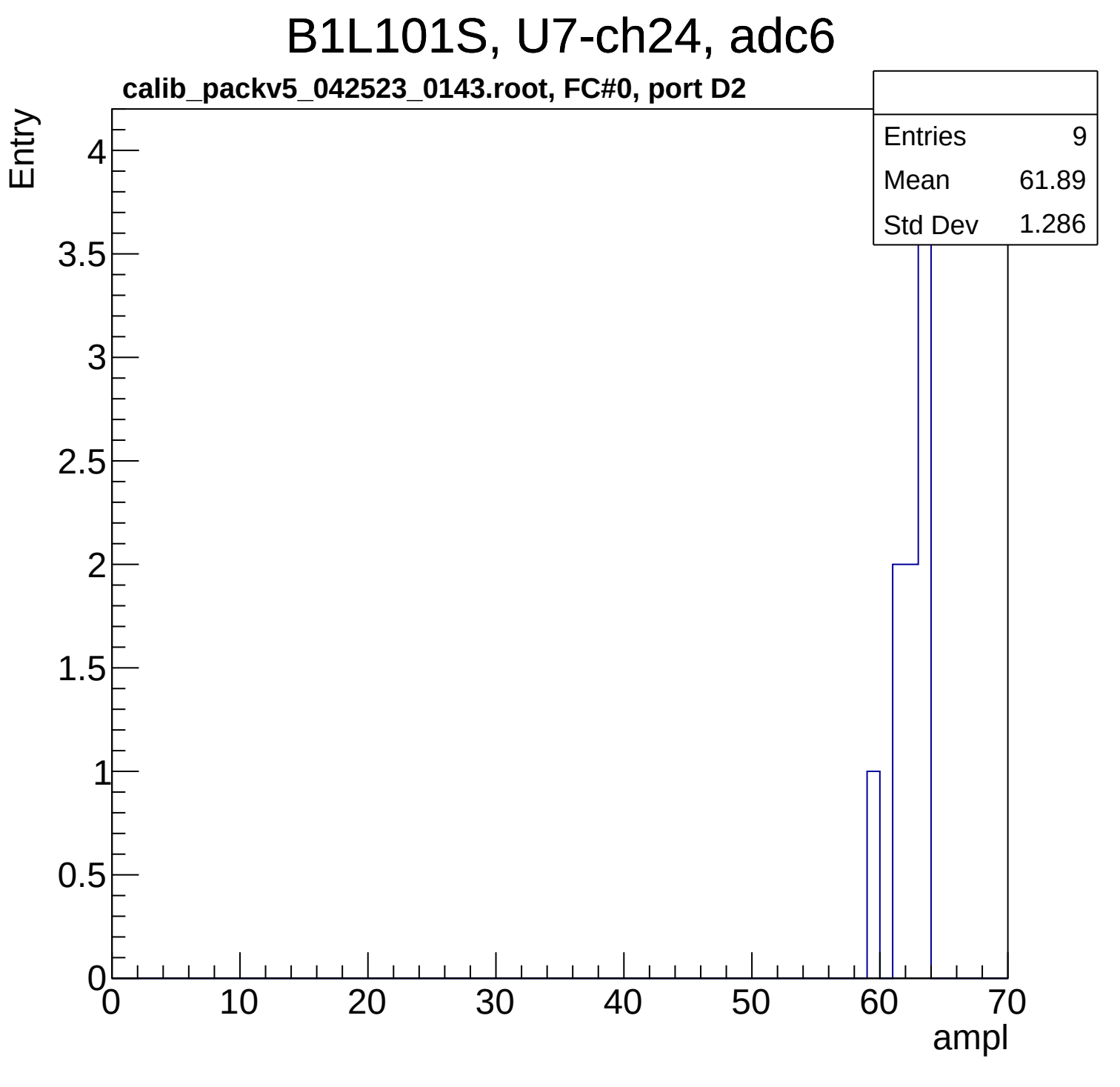

B1L101S, U7-ch24, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 87
Mean 35.55
Std Dev 3.781
Gaus mean : 36.2778
Gaus Width: 4.3698
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch24, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 42.04
Std Dev 2.868
Gaus mean : 43.1084
Gaus Width: 2.8684
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch24, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 49
Std Dev 2.966
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch24, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 54.93
Std Dev 2.947
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch24, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 59.09
Std Dev 2.514
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch24, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 61.89
Std Dev 1.286
Entry
ampl
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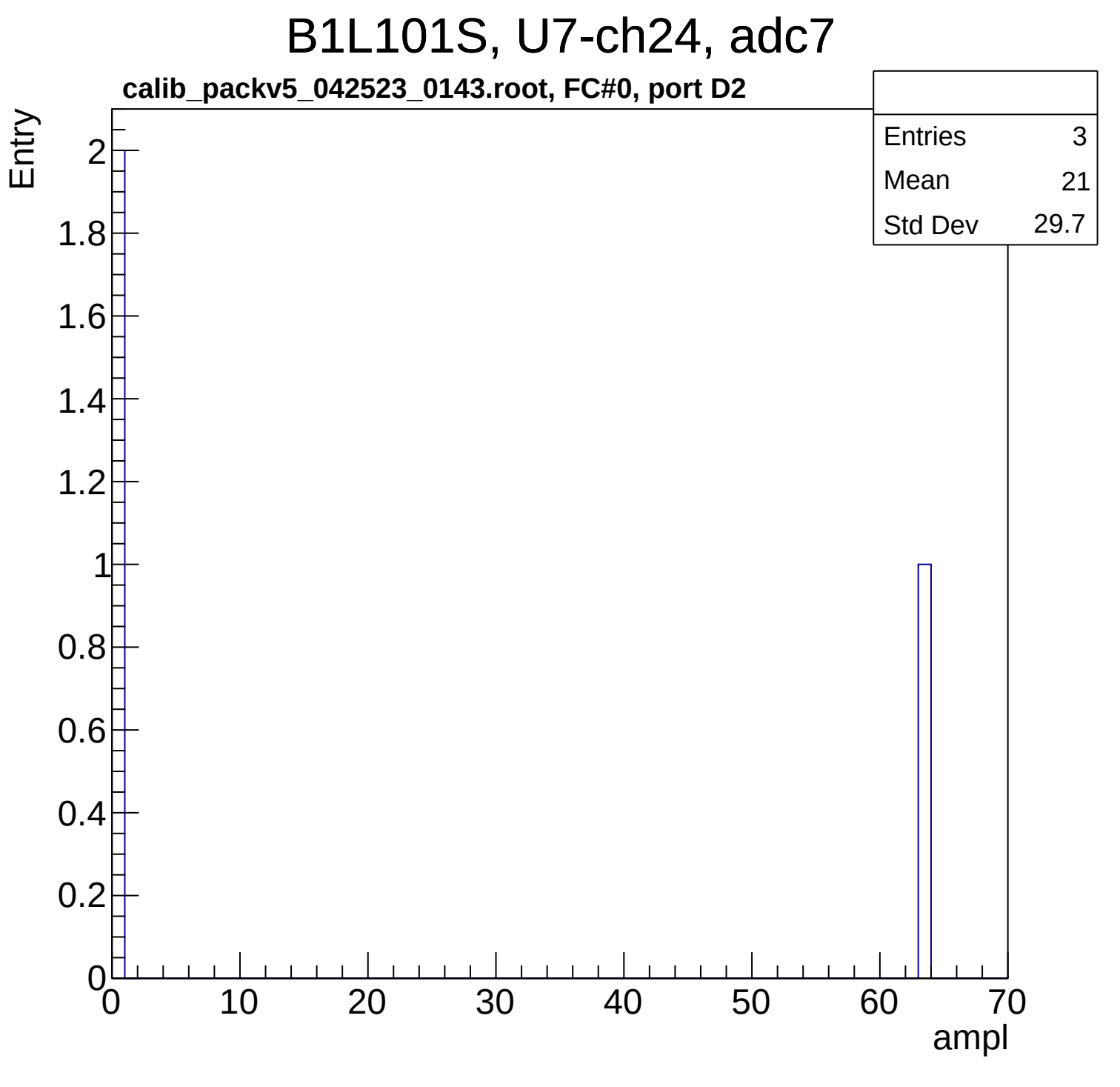
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L101S, U7-ch24, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 21
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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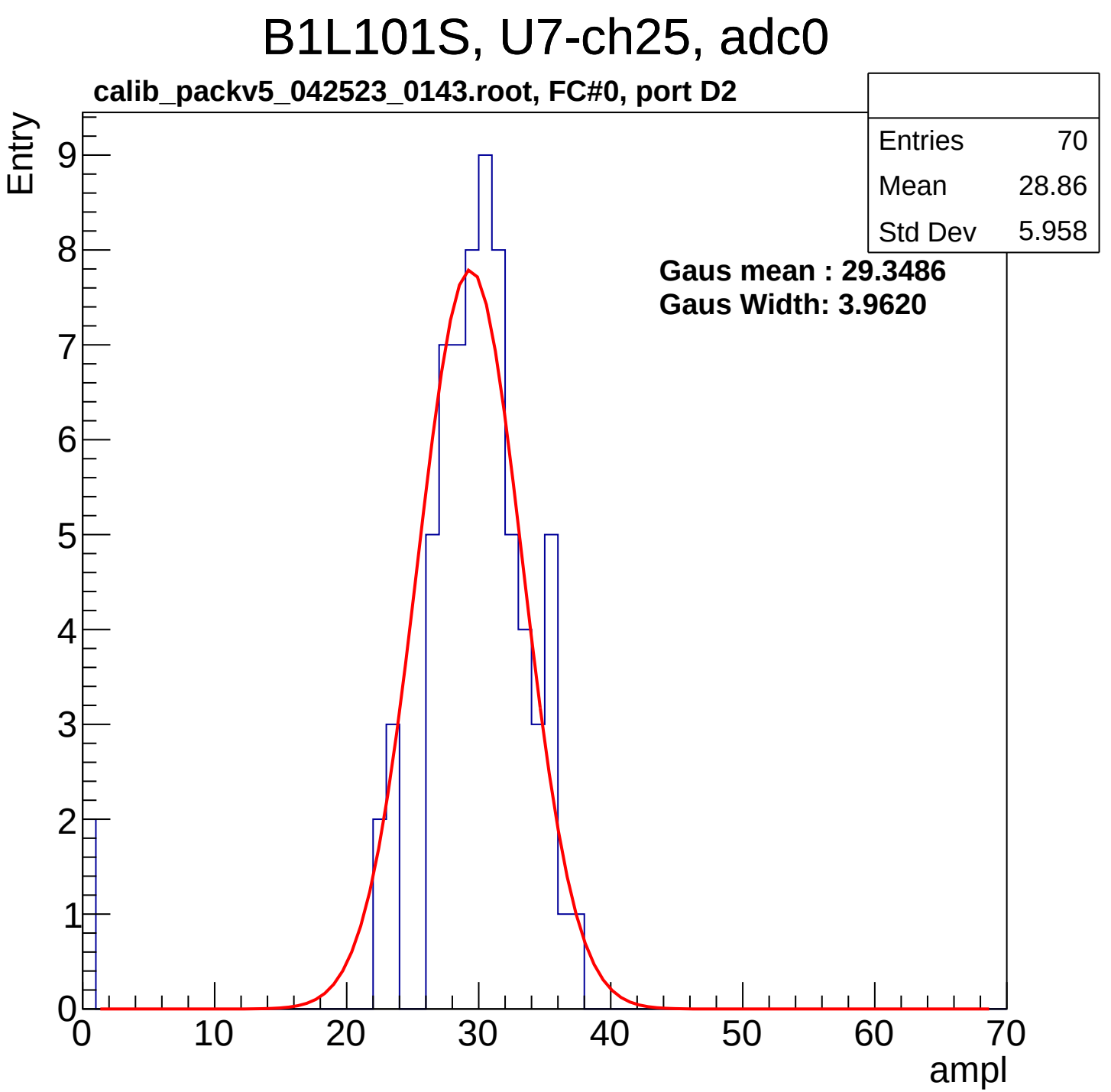
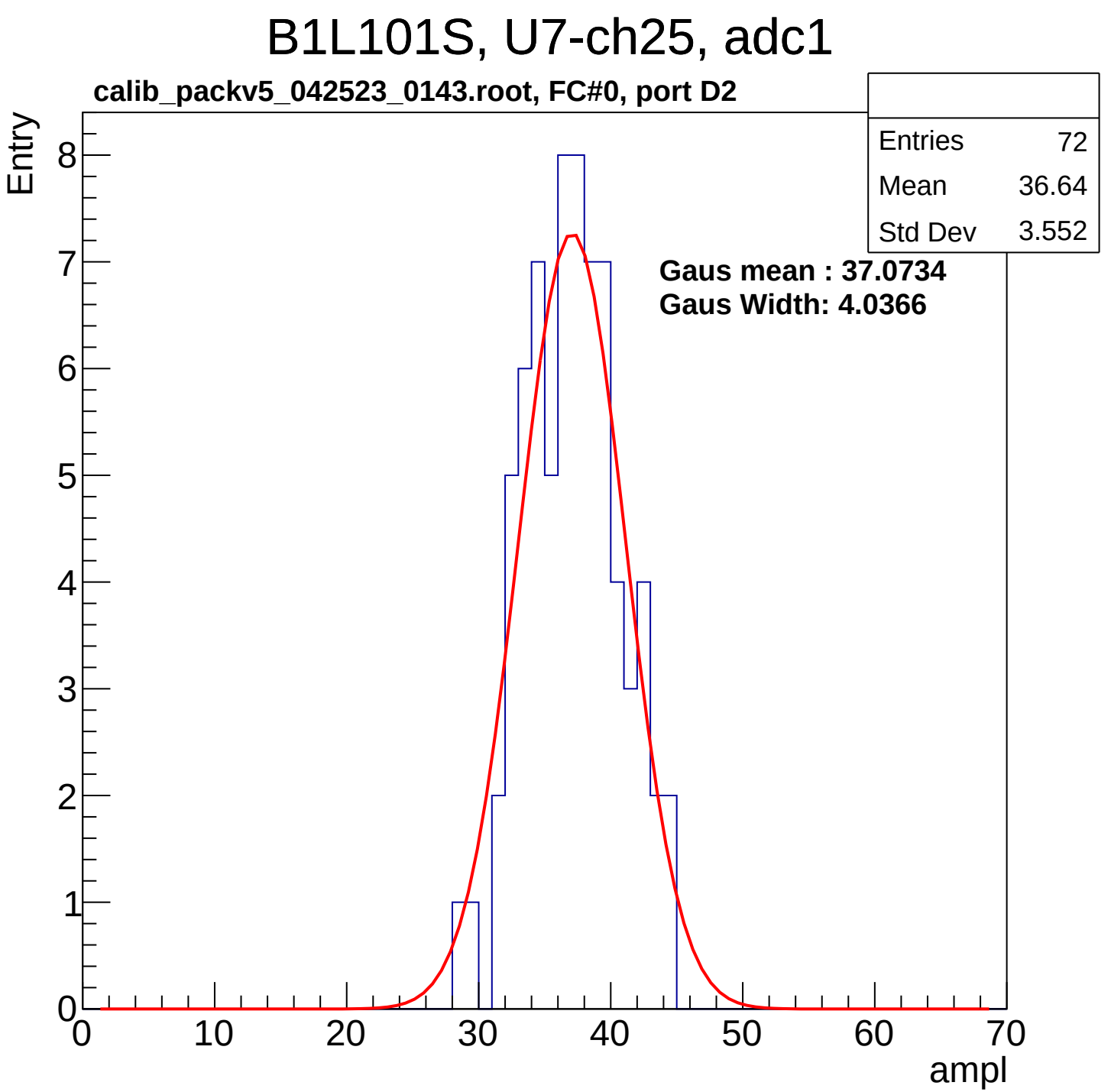
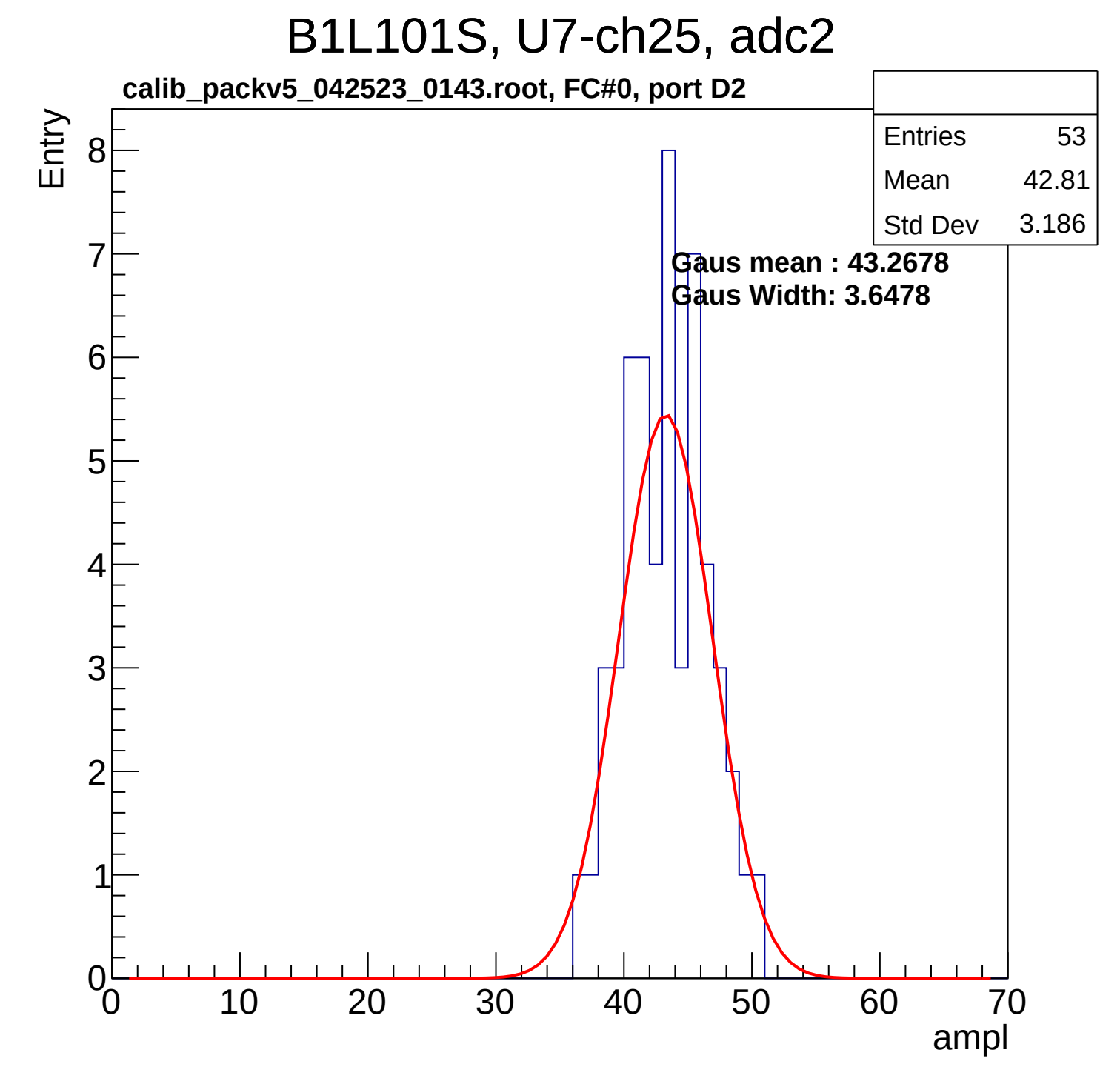

B1L101S, U7-ch25, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 28.86
Std Dev 5.958
Gaus mean : 29.3486
Gaus Width: 3.9620
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch25, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 36.64
Std Dev 3.552
Gaus mean : 37.0734
Gaus Width: 4.0366
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch25, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 42.81
Std Dev 3.186
Gaus mean : 43.2678
Gaus Width: 3.6478
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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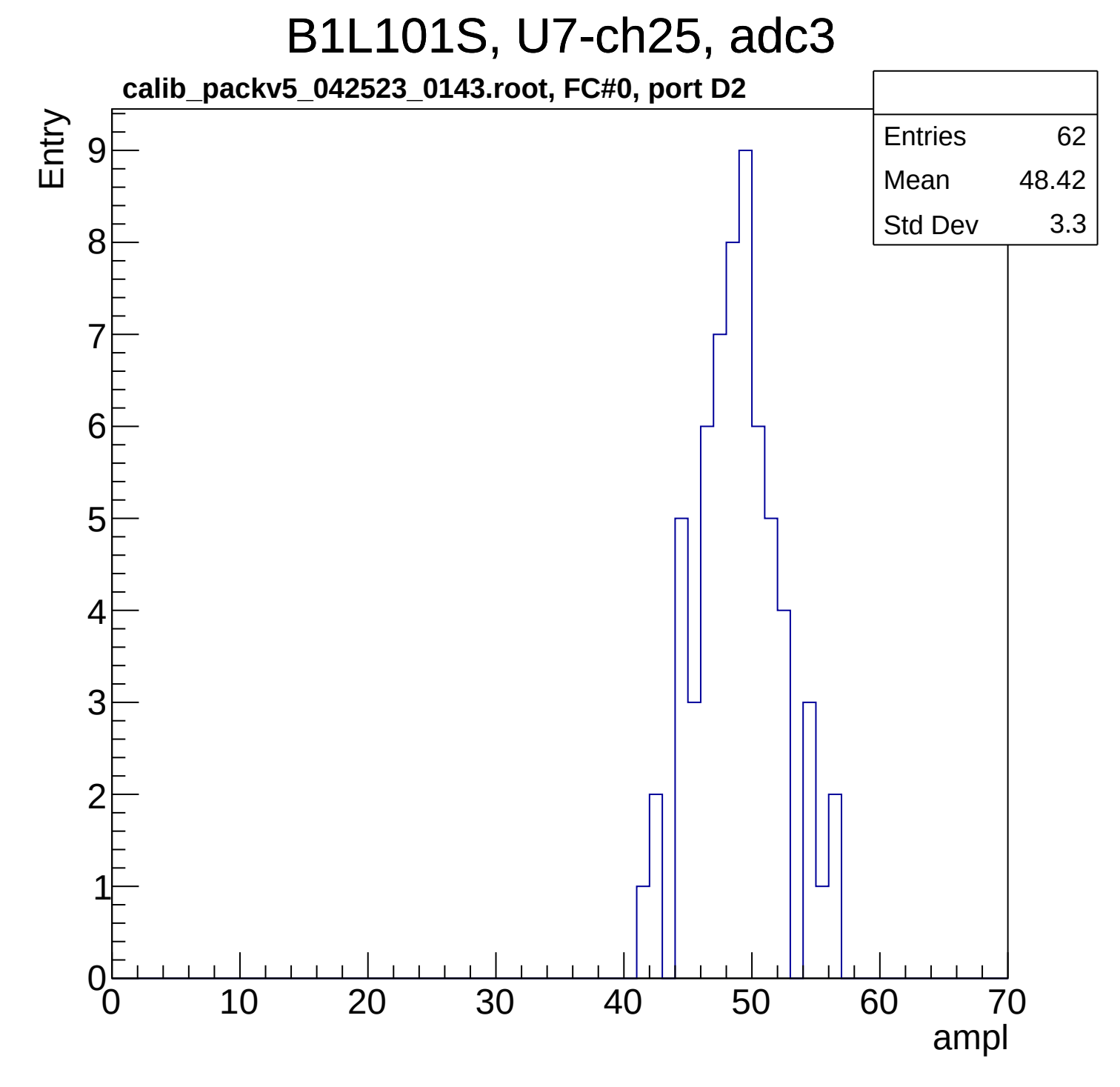
B1L101S, U7-ch25, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 48.42
Std Dev 3.3
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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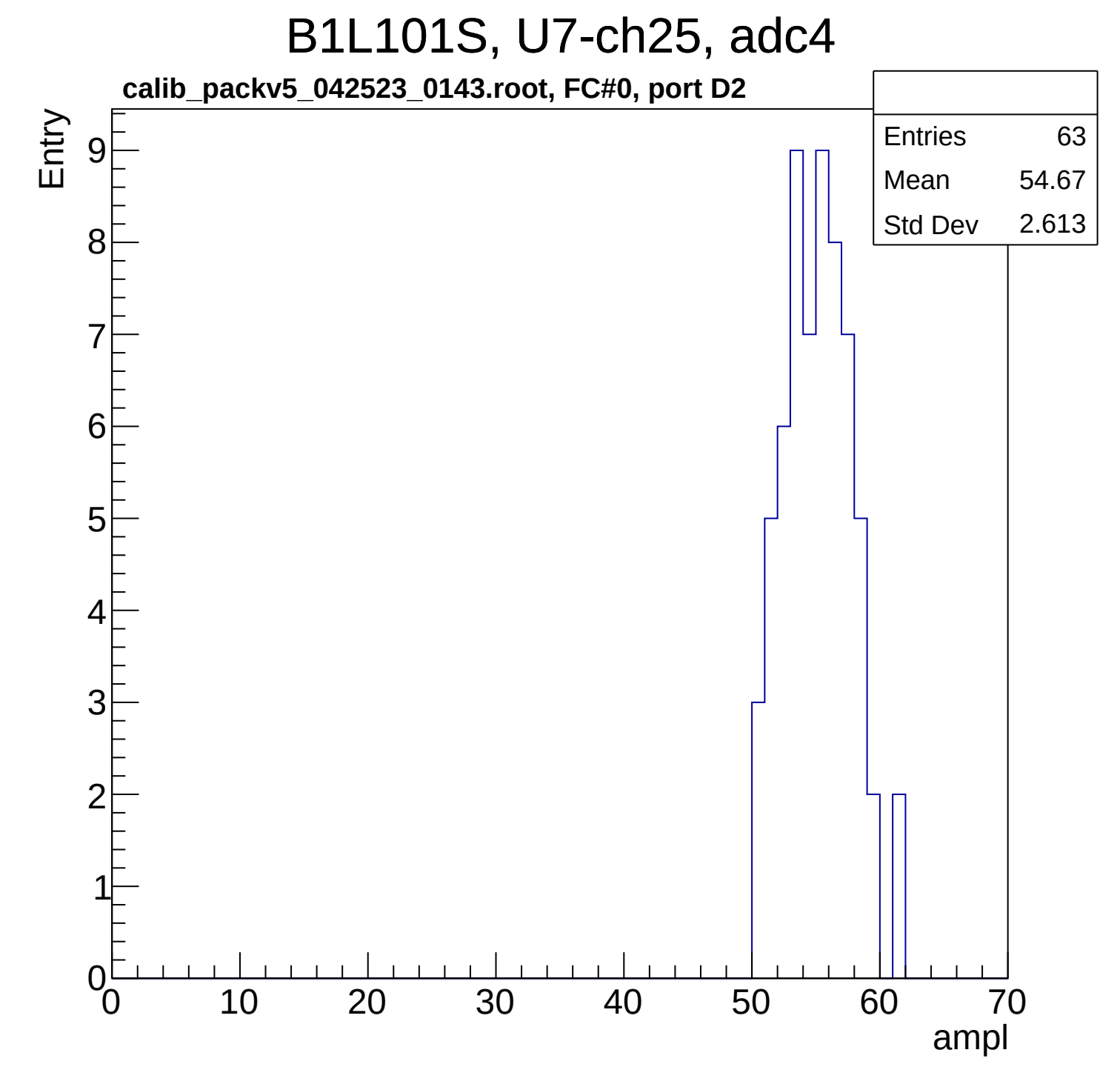
B1L101S, U7-ch25, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 54.67
Std Dev 2.613
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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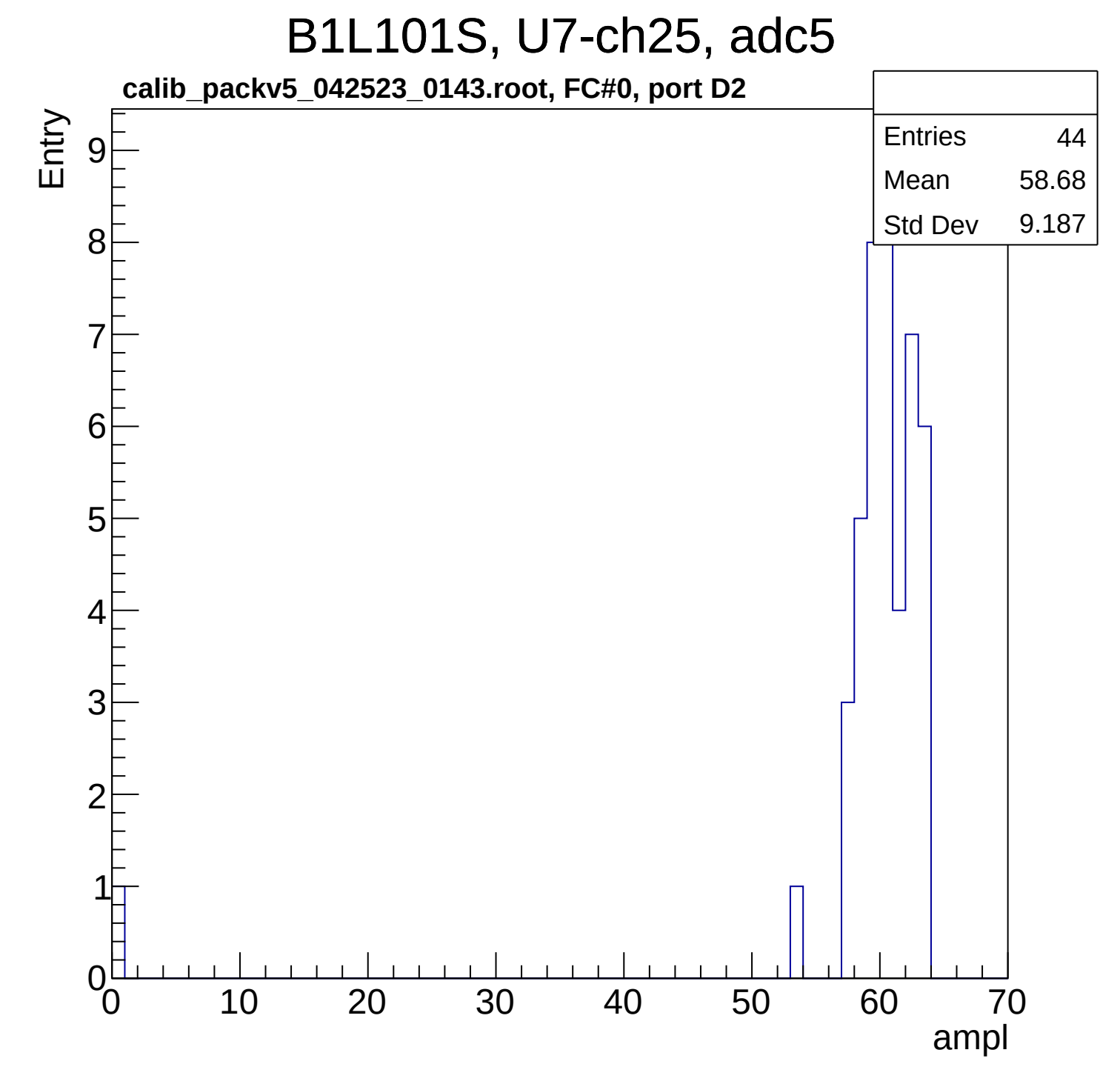
60
70


B1L101S, U7-ch25, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 44
Mean 58.68
Std Dev 9.187
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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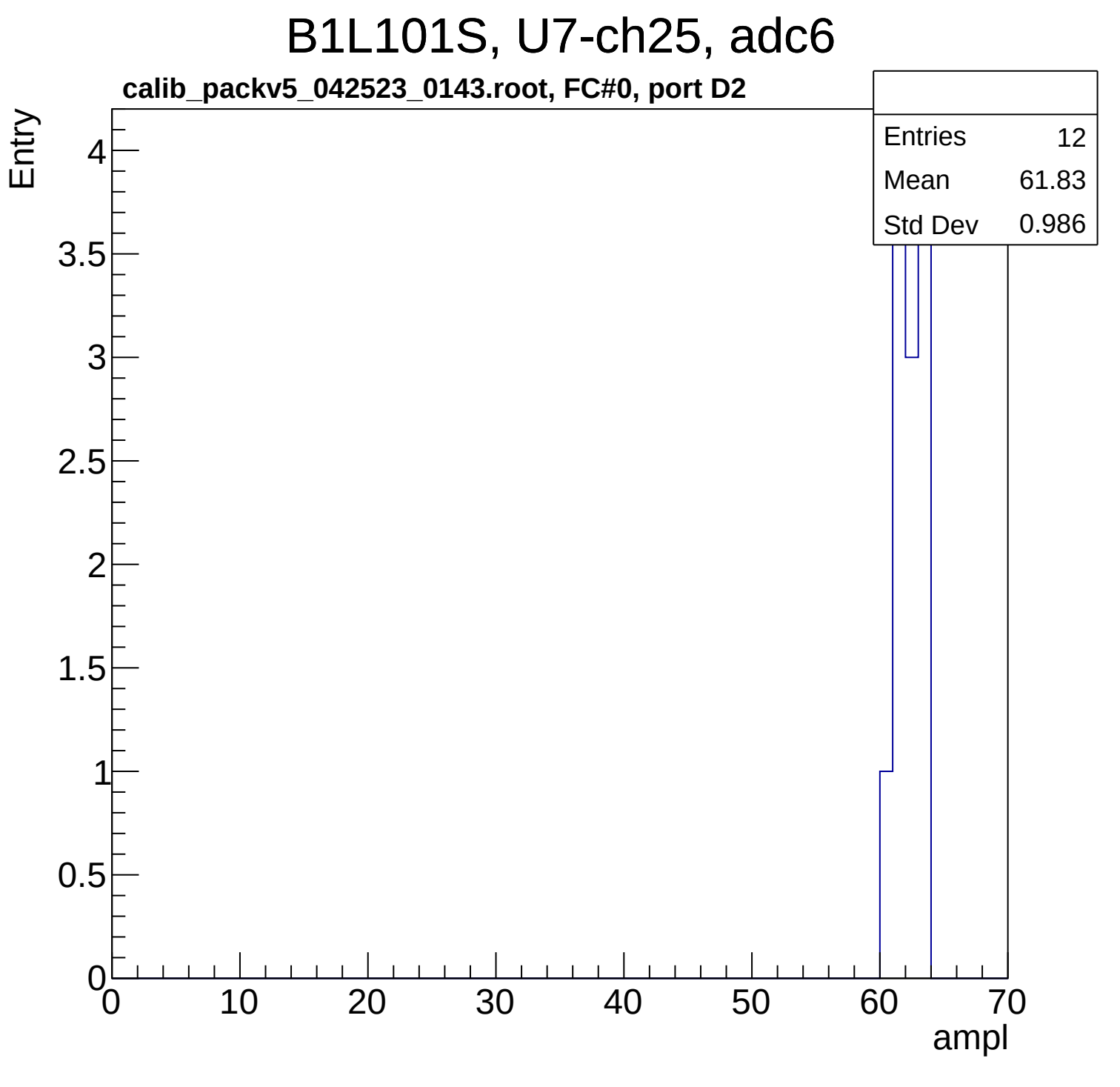
B1L101S, U7-ch25, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 12
Mean 61.83
Std Dev 0.986
Entry
ampl
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1
1.5
2
2.5
3
3.5
4
0
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40
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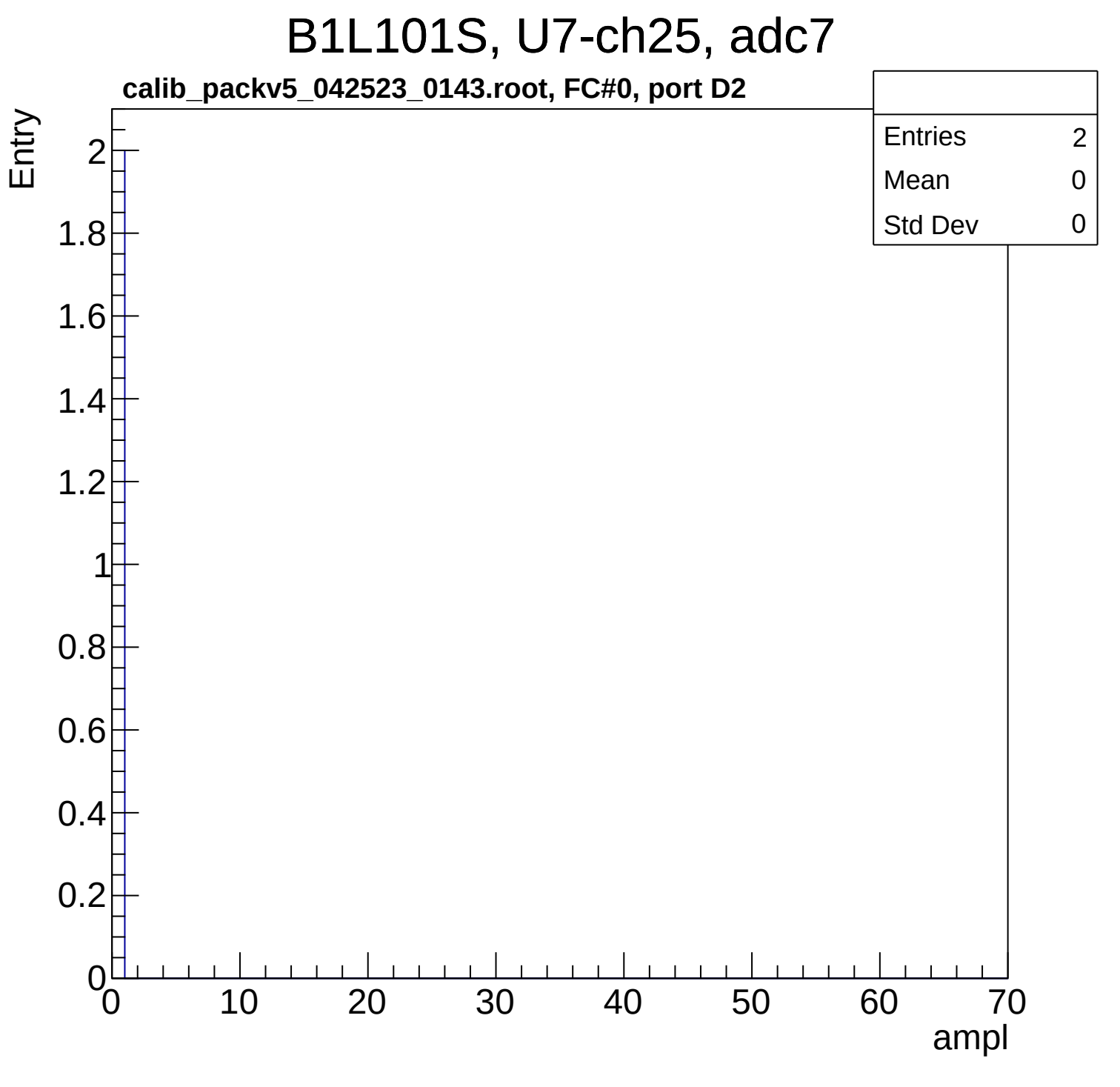
60
70


B1L101S, U7-ch25, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
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1
1.2
1.4
1.6
1.8
2
0
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20
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60
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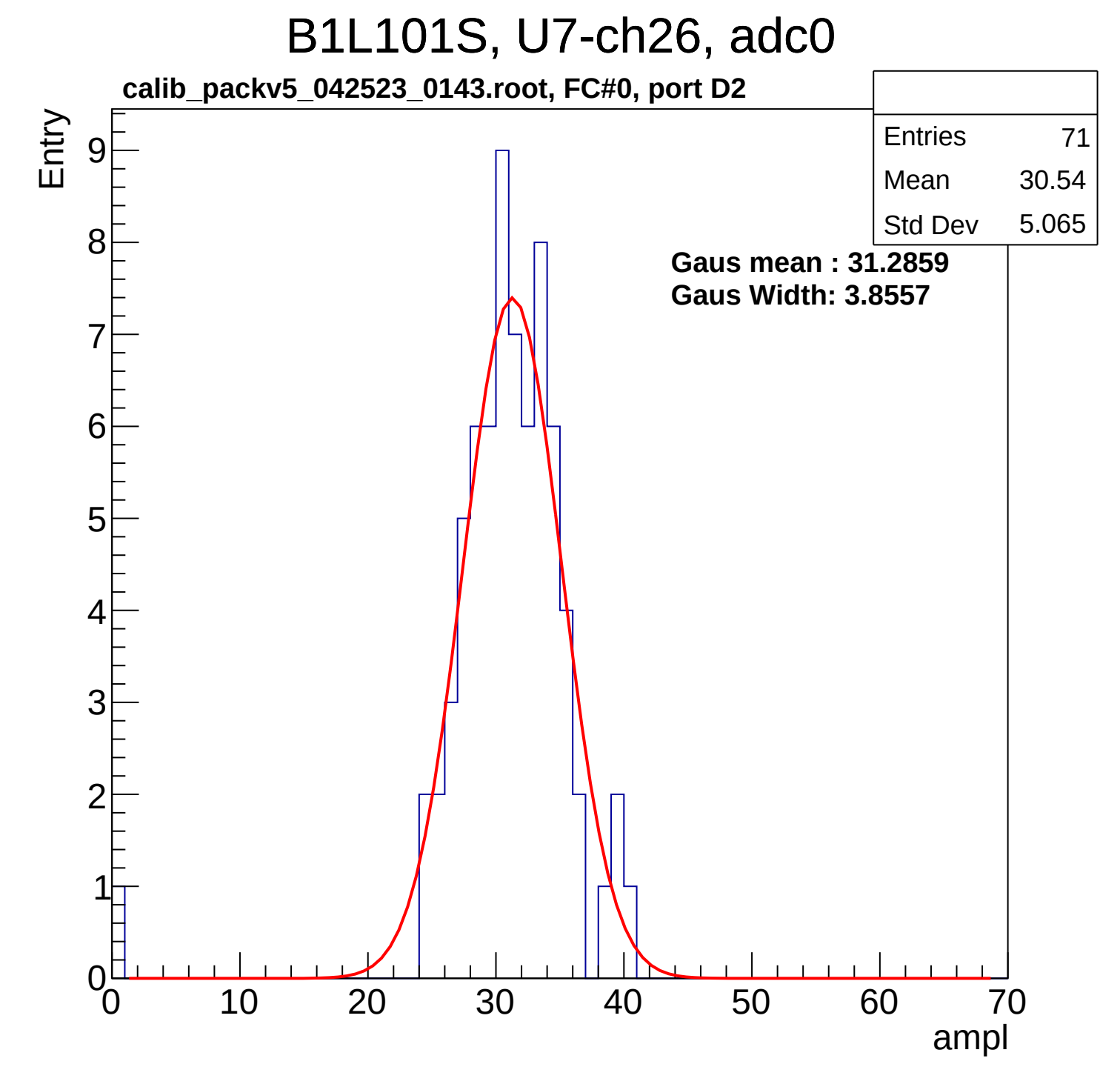
B1L101S, U7-ch26, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 30.54
Std Dev 5.065
Gaus mean : 31.2859
Gaus Width: 3.8557
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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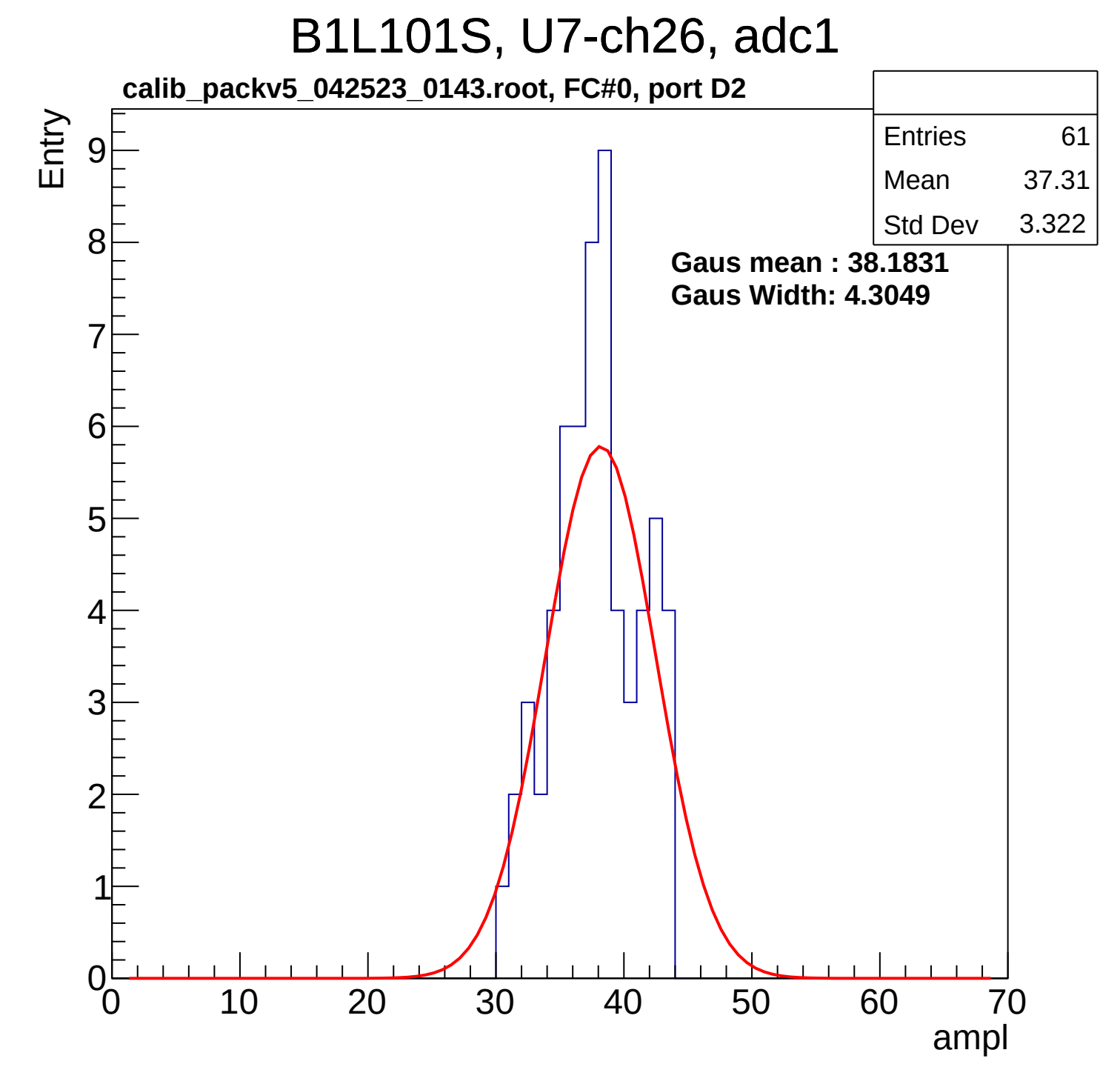
B1L101S, U7-ch26, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 37.31
Std Dev 3.322
Gaus mean : 38.1831
Gaus Width: 4.3049
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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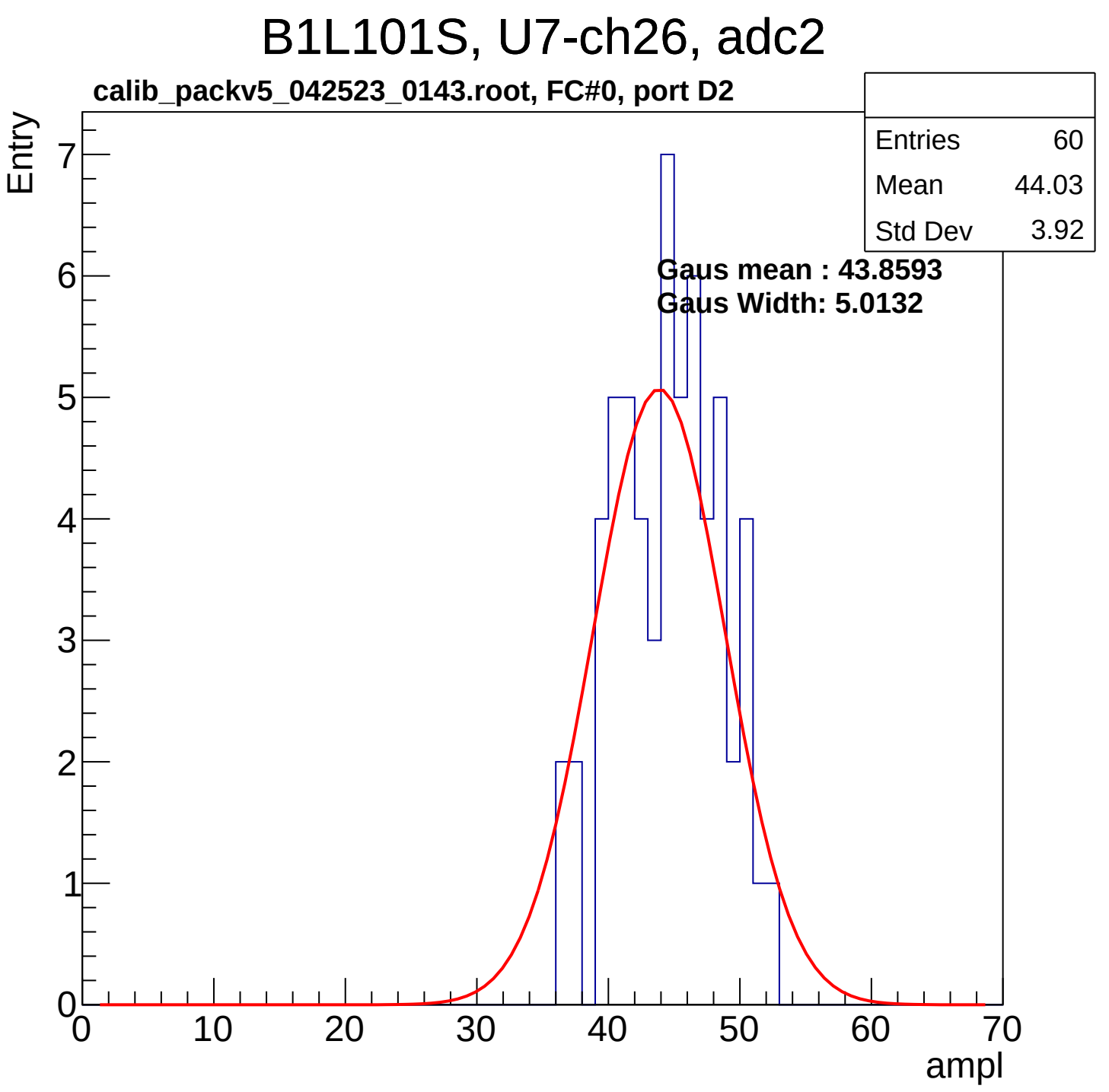
B1L101S, U7-ch26, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 44.03
Std Dev 3.92
Gaus mean : 43.8593
Gaus Width: 5.0132
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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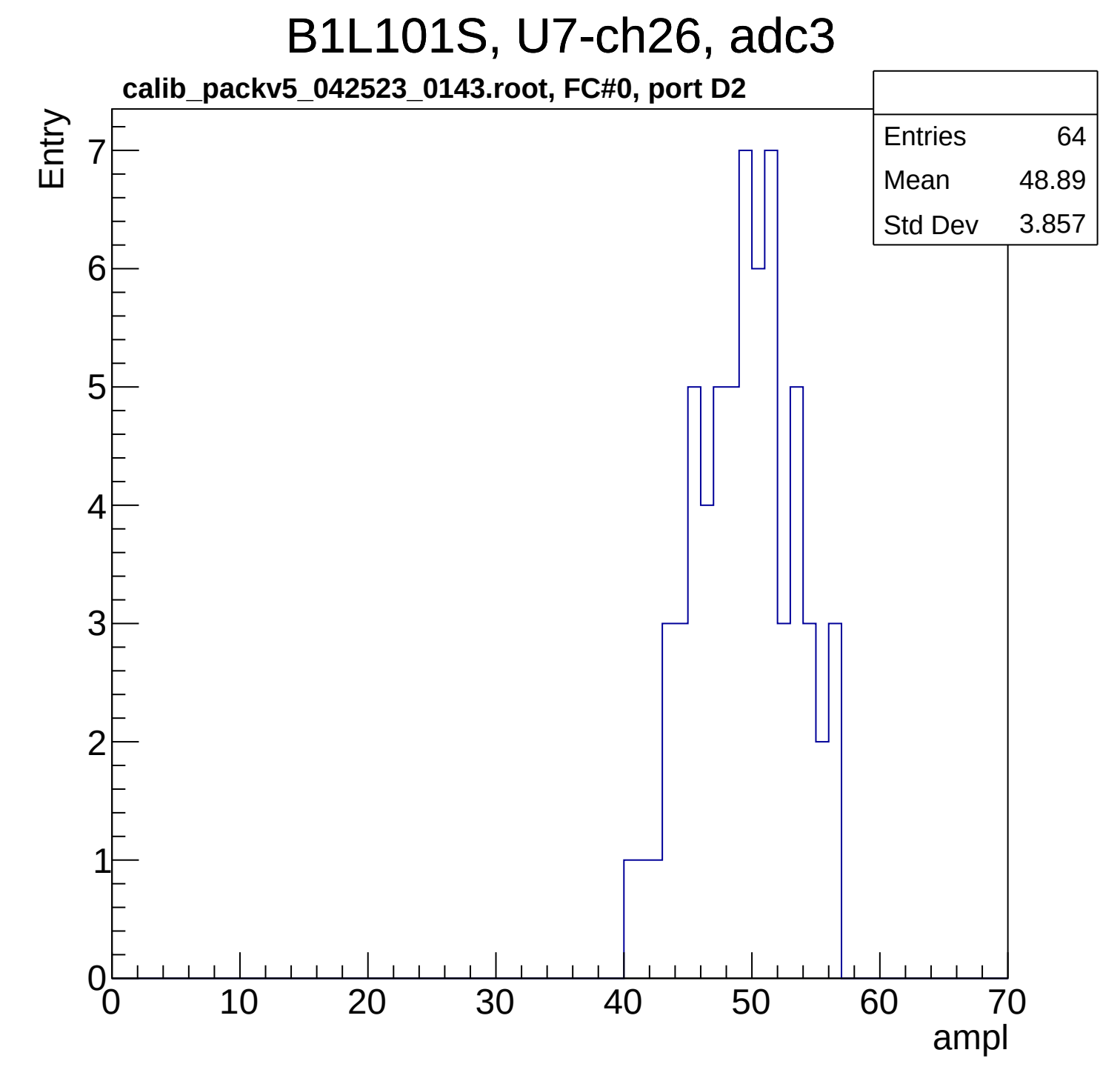
B1L101S, U7-ch26, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 48.89
Std Dev 3.857
Entry
ampl
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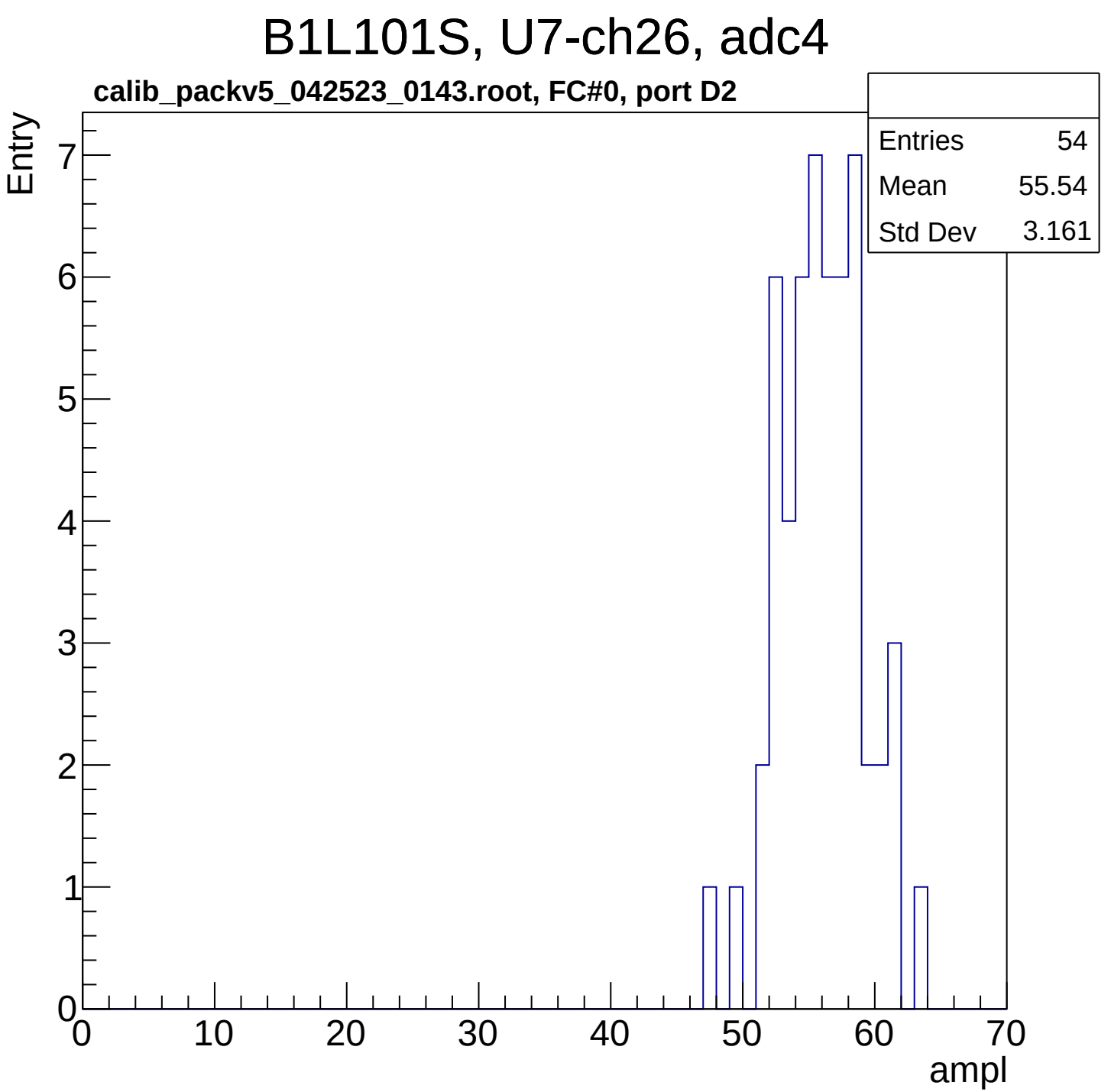
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U7-ch26, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 55.54
Std Dev 3.161
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
50
60
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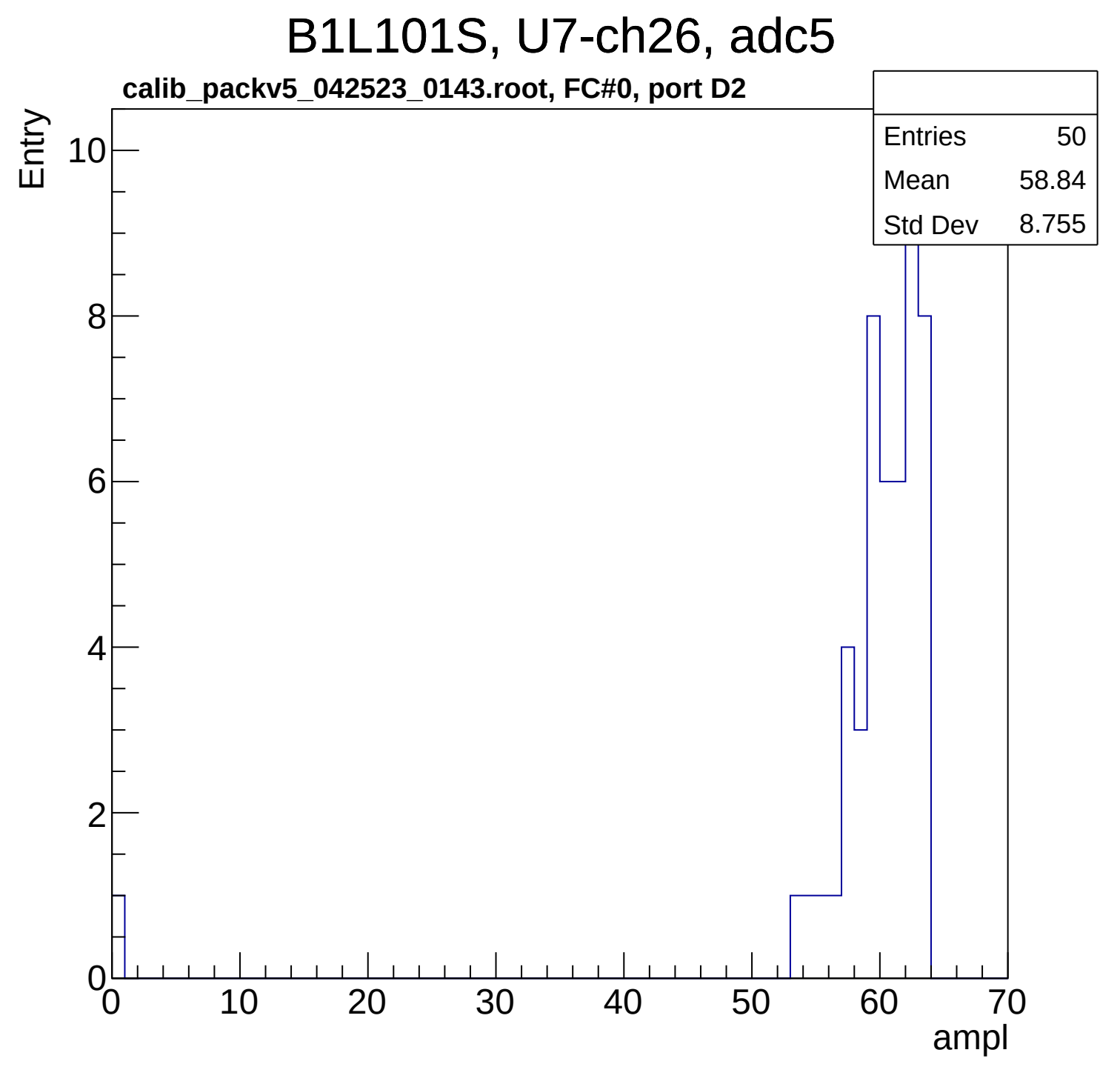
B1L101S, U7-ch26, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 58.84
Std Dev 8.755
Entry
ampl
0
2
4
6
8
10
0
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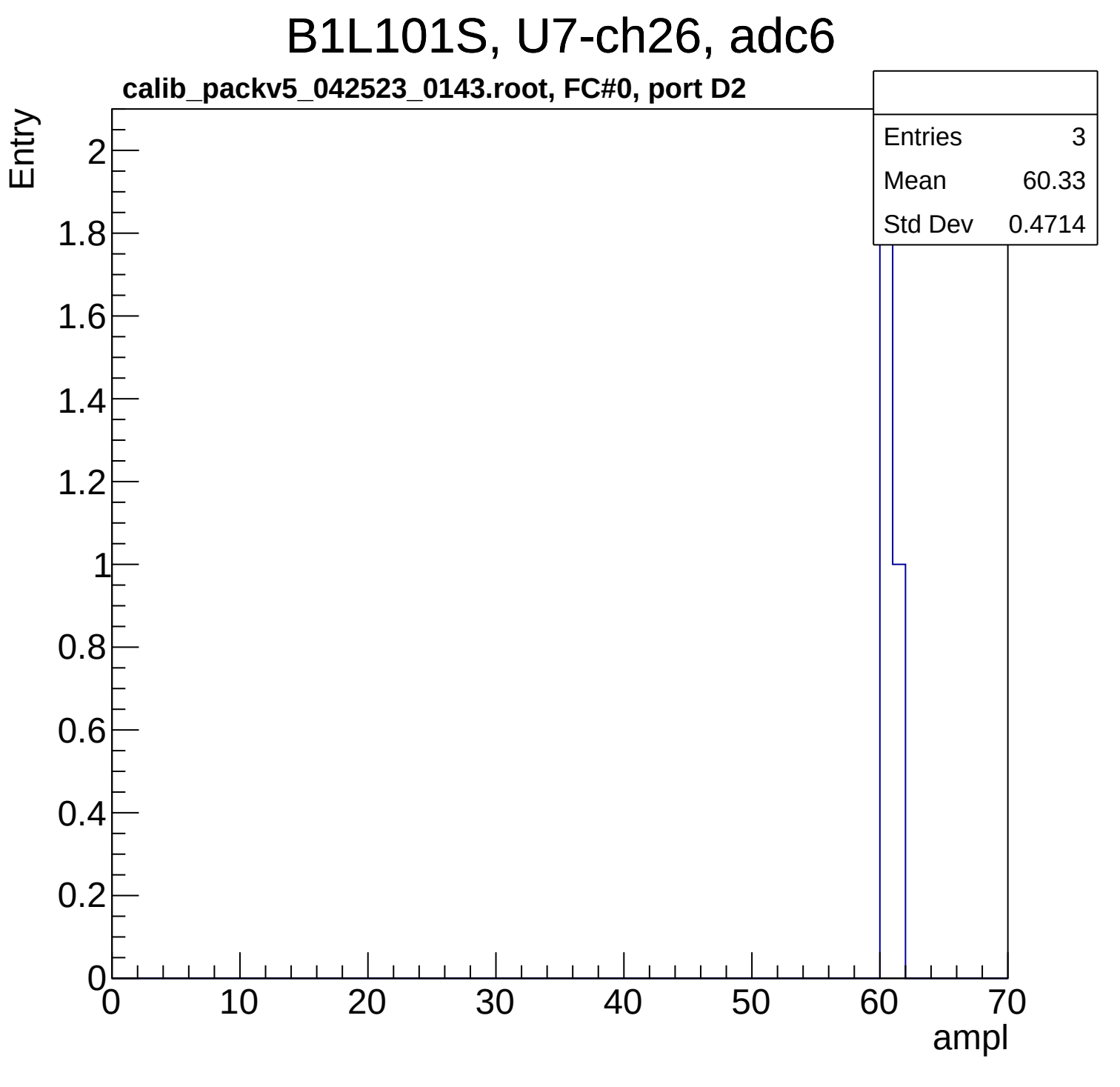
20
30
40
50
60
70


B1L101S, U7-ch26, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 60.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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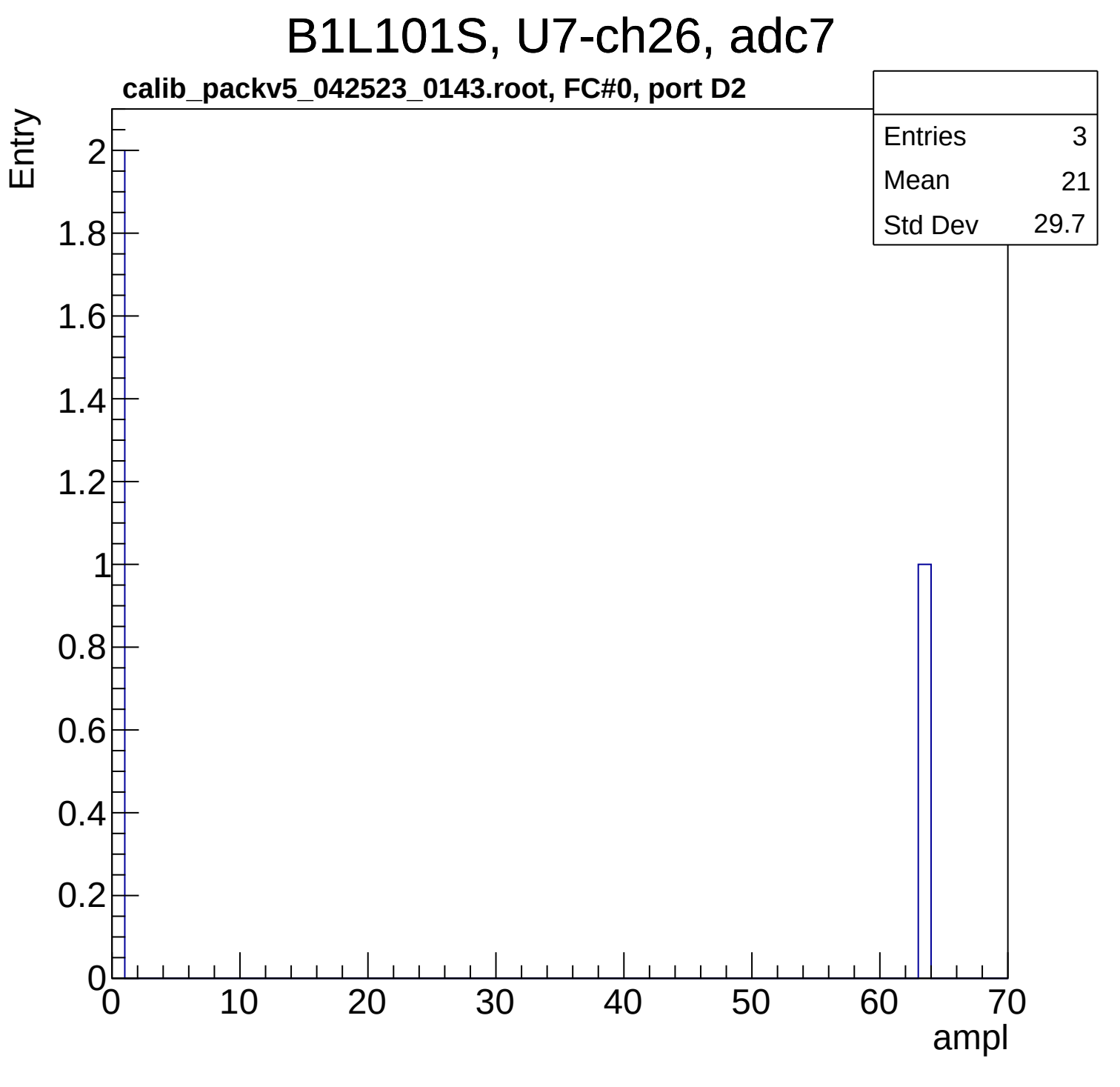
40
50
60
70


B1L101S, U7-ch26, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 21
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
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60
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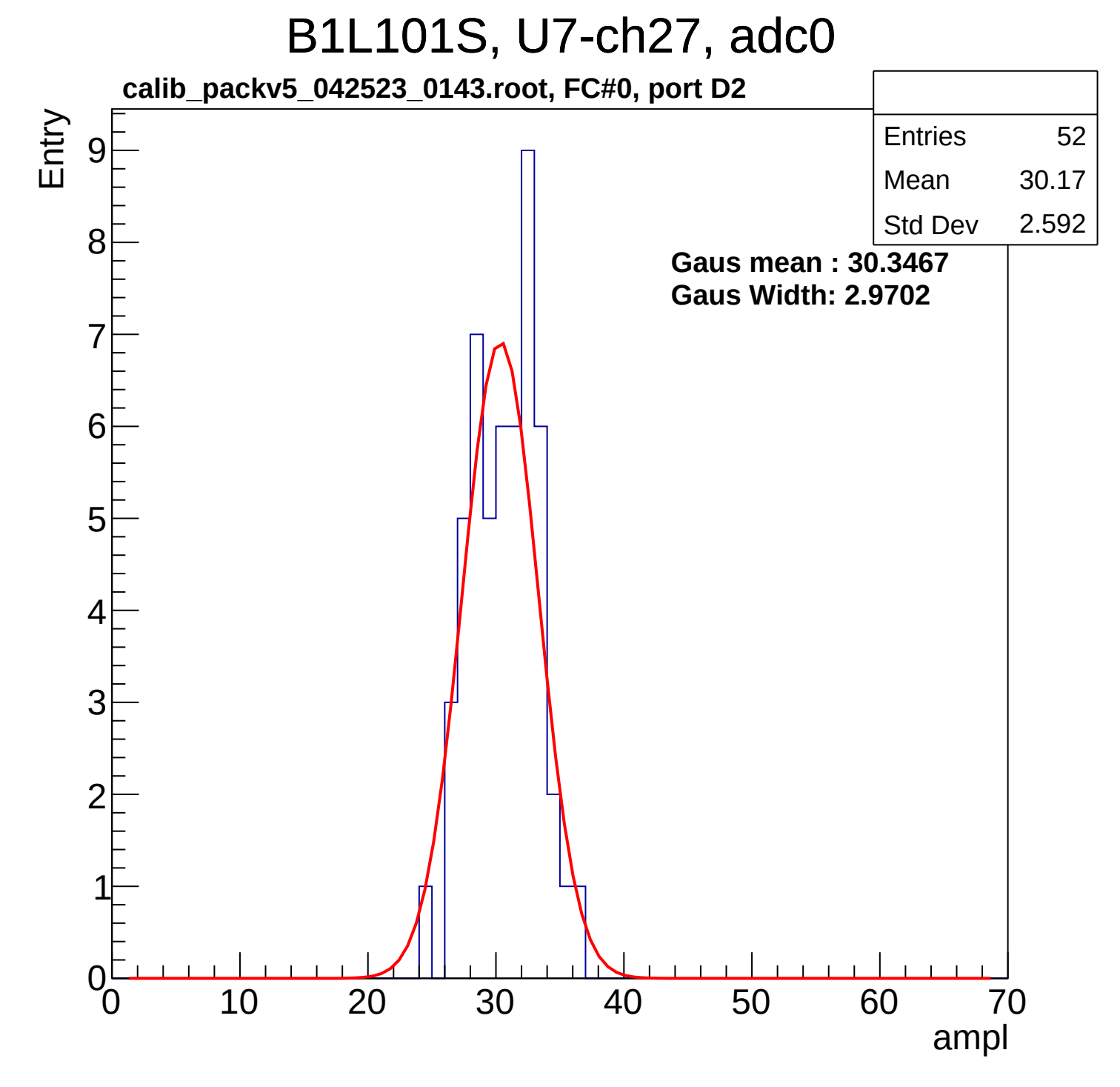
B1L101S, U7-ch27, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 30.17
Std Dev 2.592
Gaus mean : 30.3467
Gaus Width: 2.9702
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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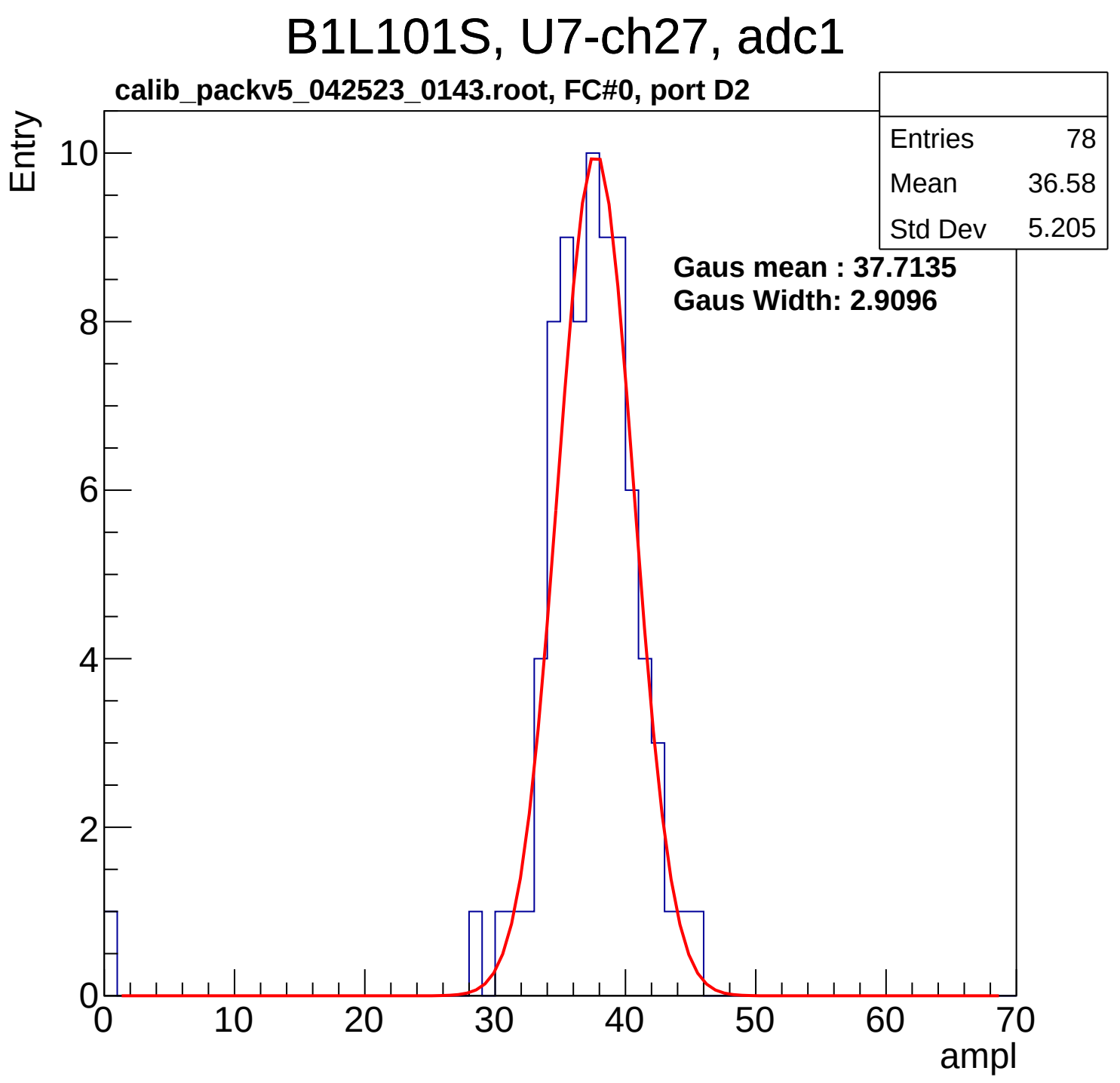
B1L101S, U7-ch27, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 36.58
Std Dev 5.205
Gaus mean : 37.7135
Gaus Width: 2.9096
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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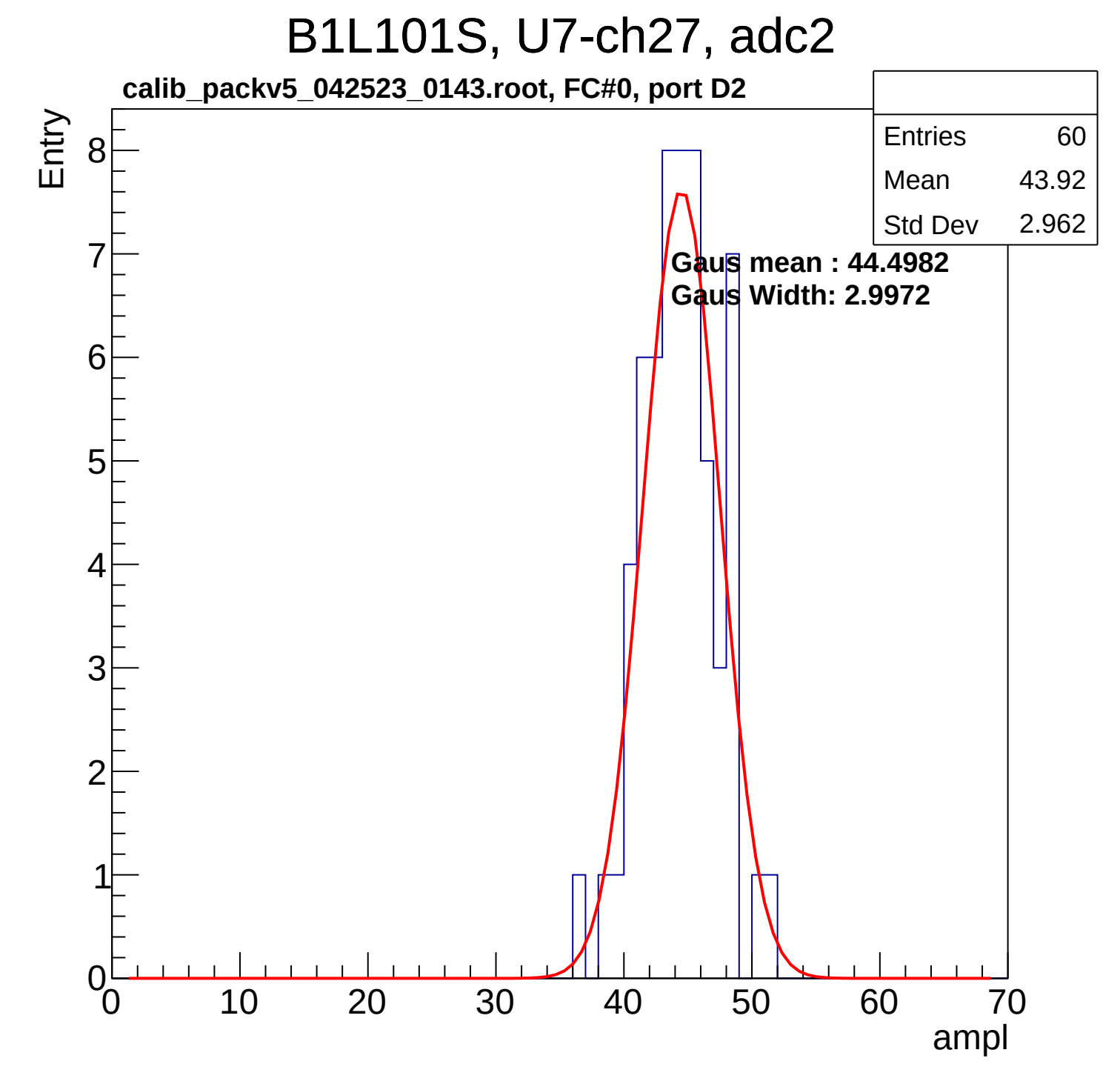
B1L101S, U7-ch27, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 43.92
Std Dev 2.962
Gaus mean : 44.4982
Gaus Width: 2.9972
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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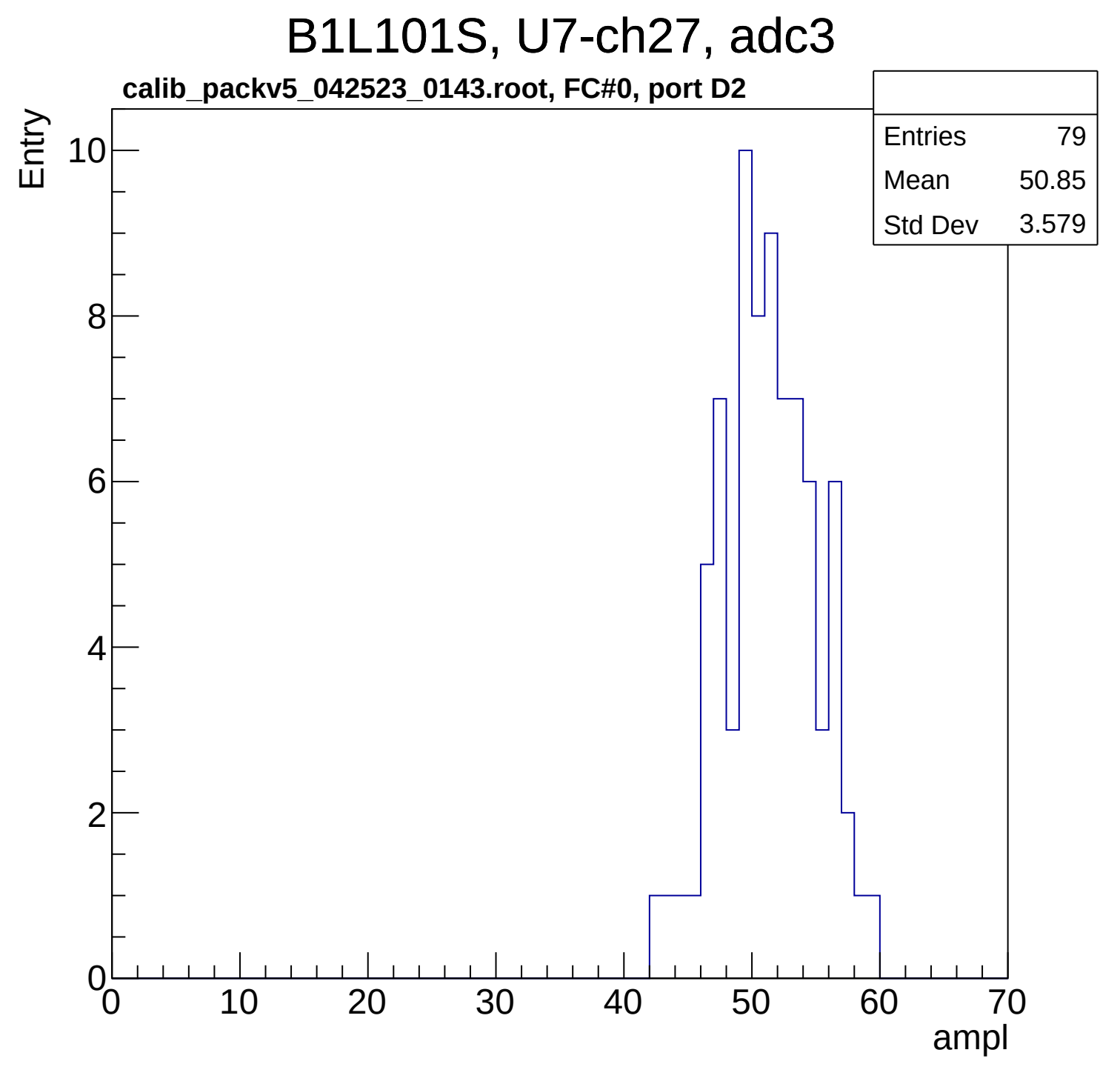
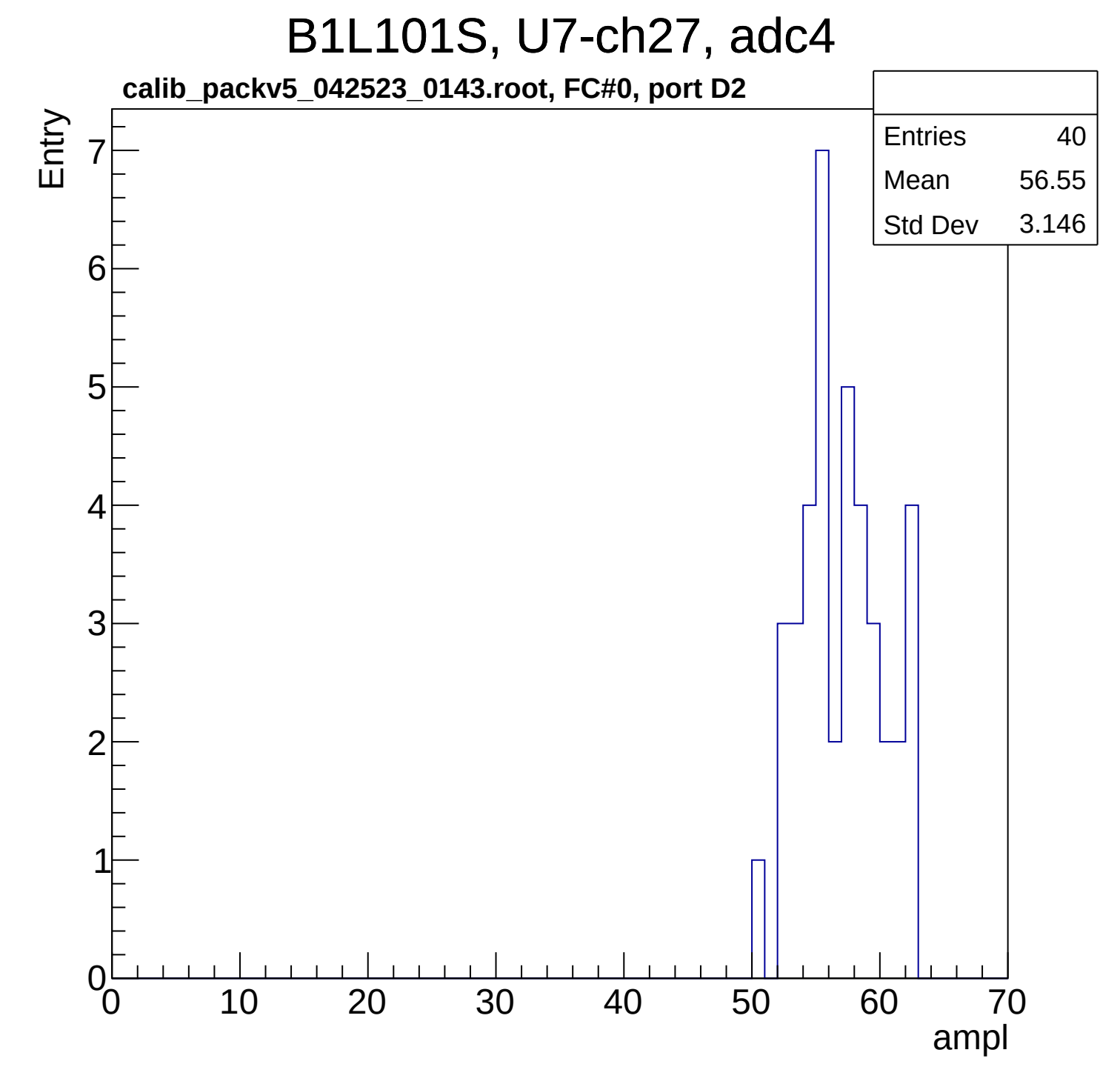

B1L101S, U7-ch27, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 50.85
Std Dev 3.579
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch27, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 40
Mean 56.55
Std Dev 3.146
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
50
60
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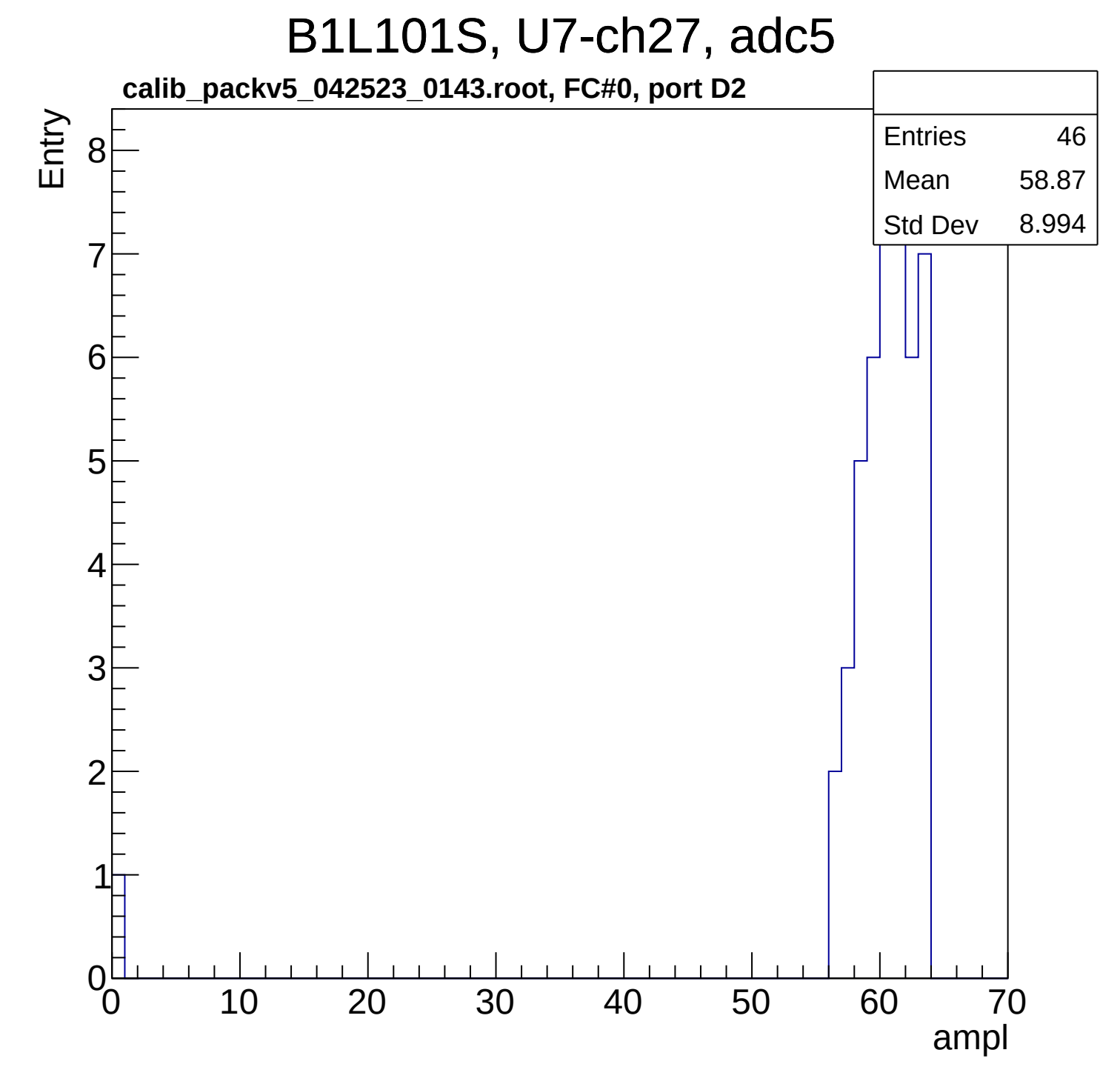
B1L101S, U7-ch27, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 58.87
Std Dev 8.994
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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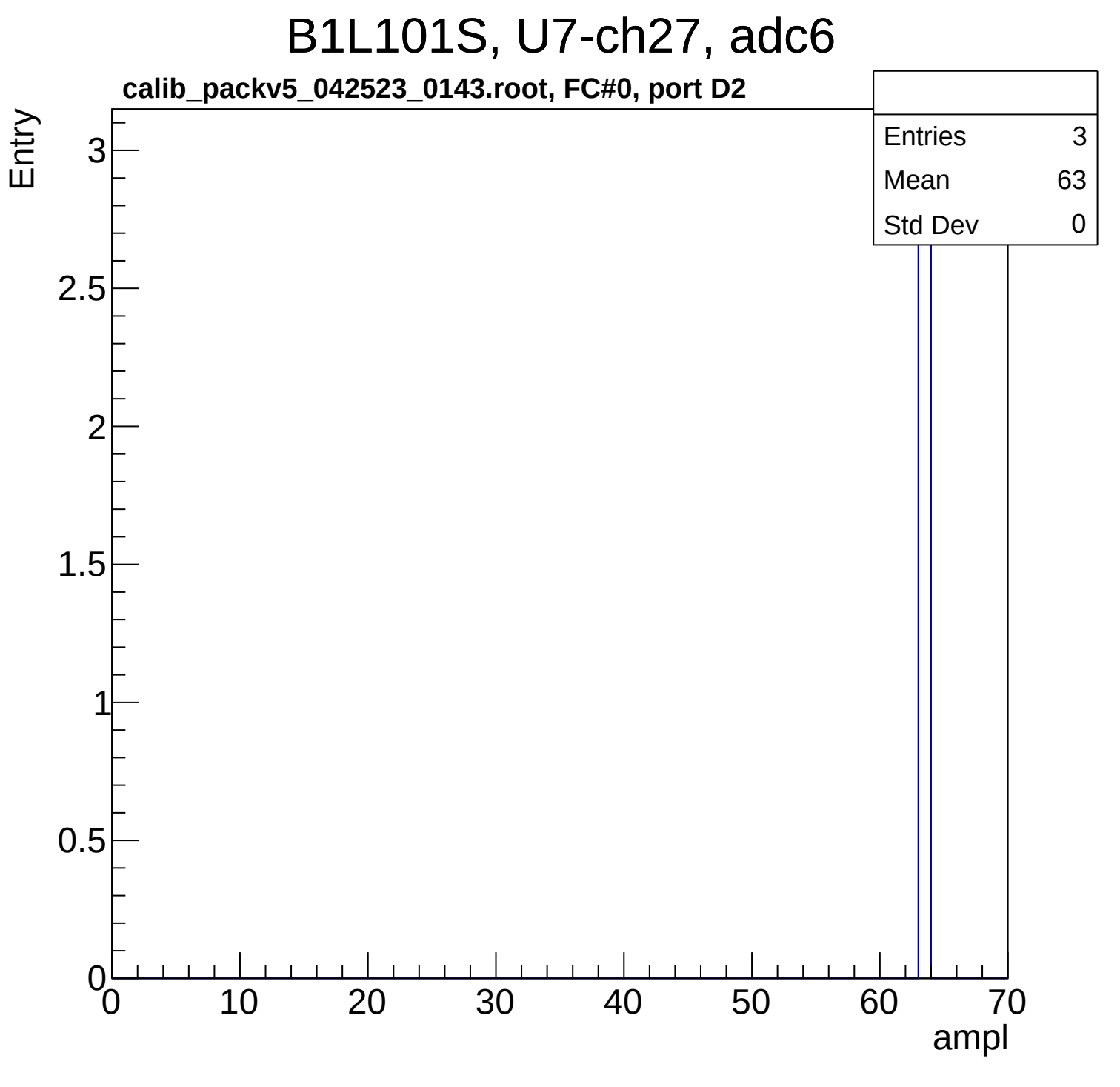
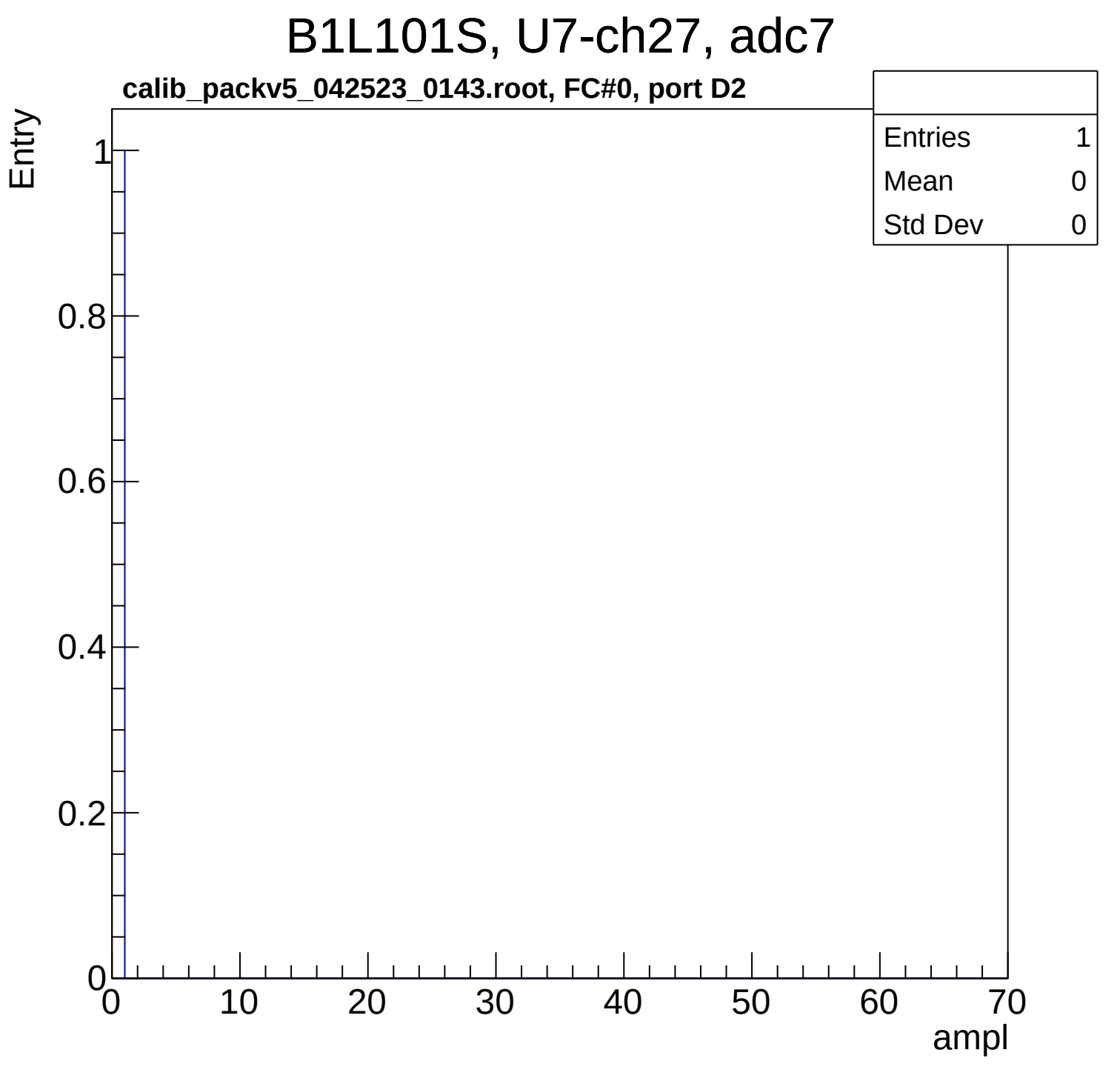
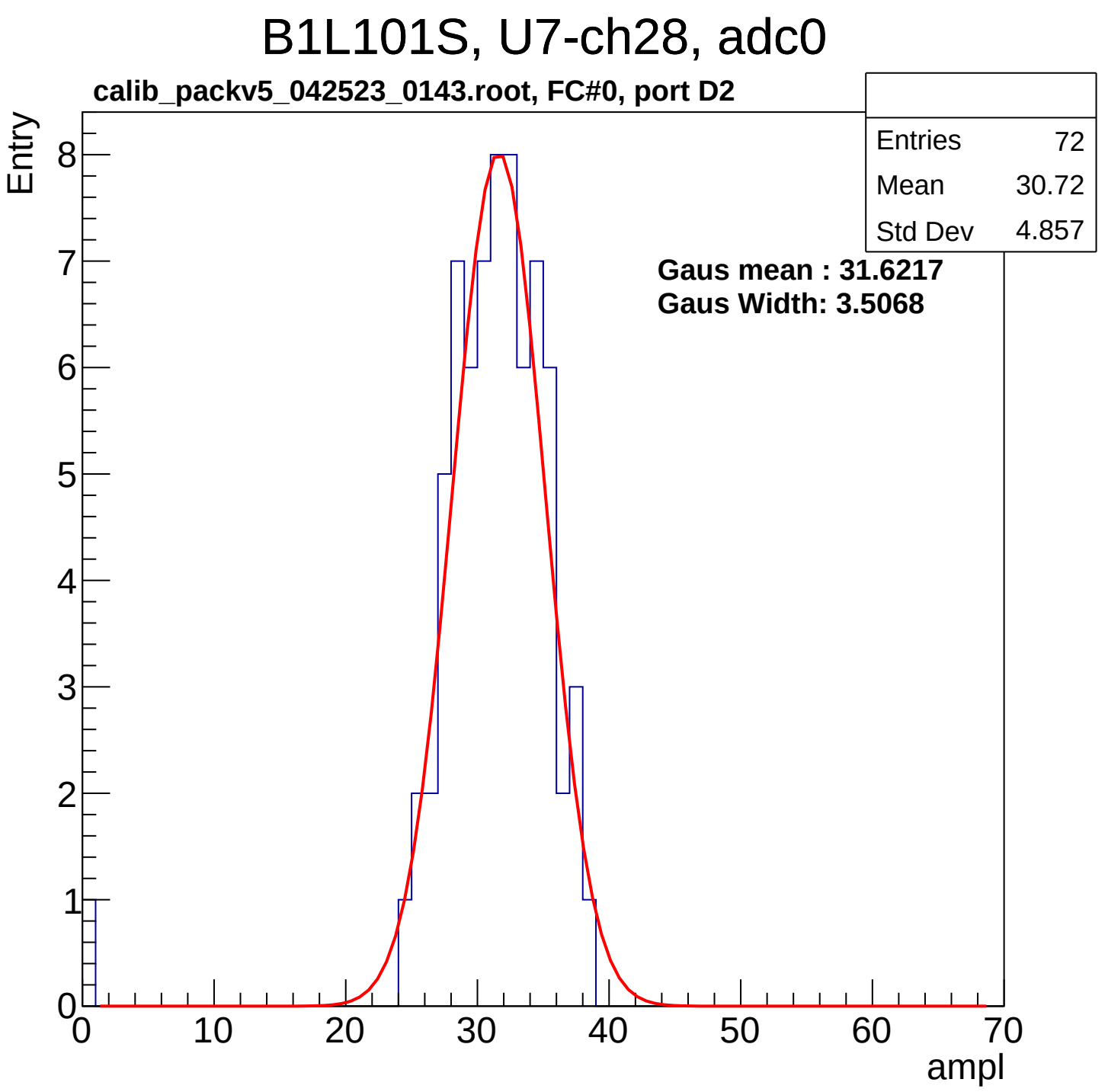
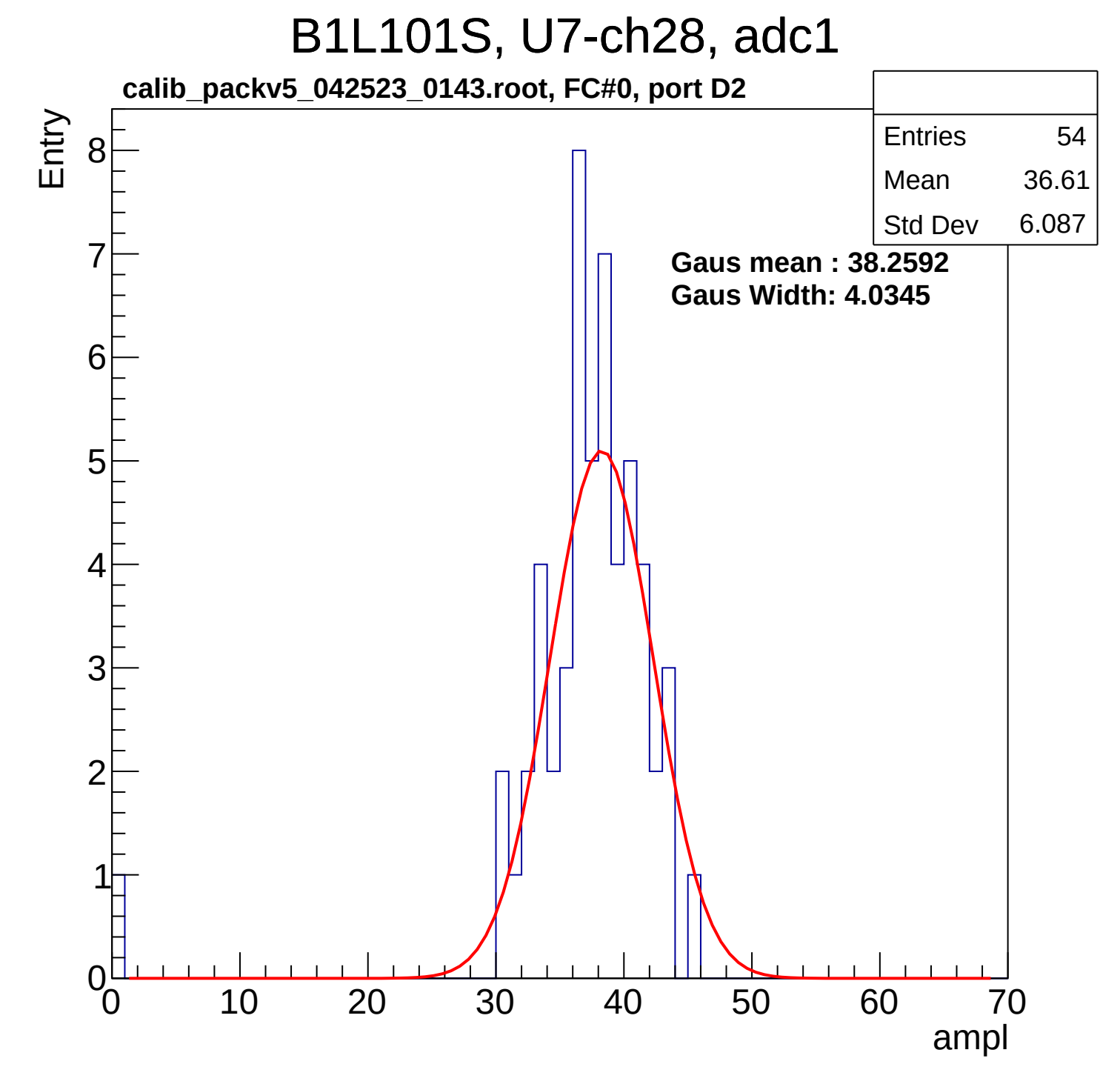
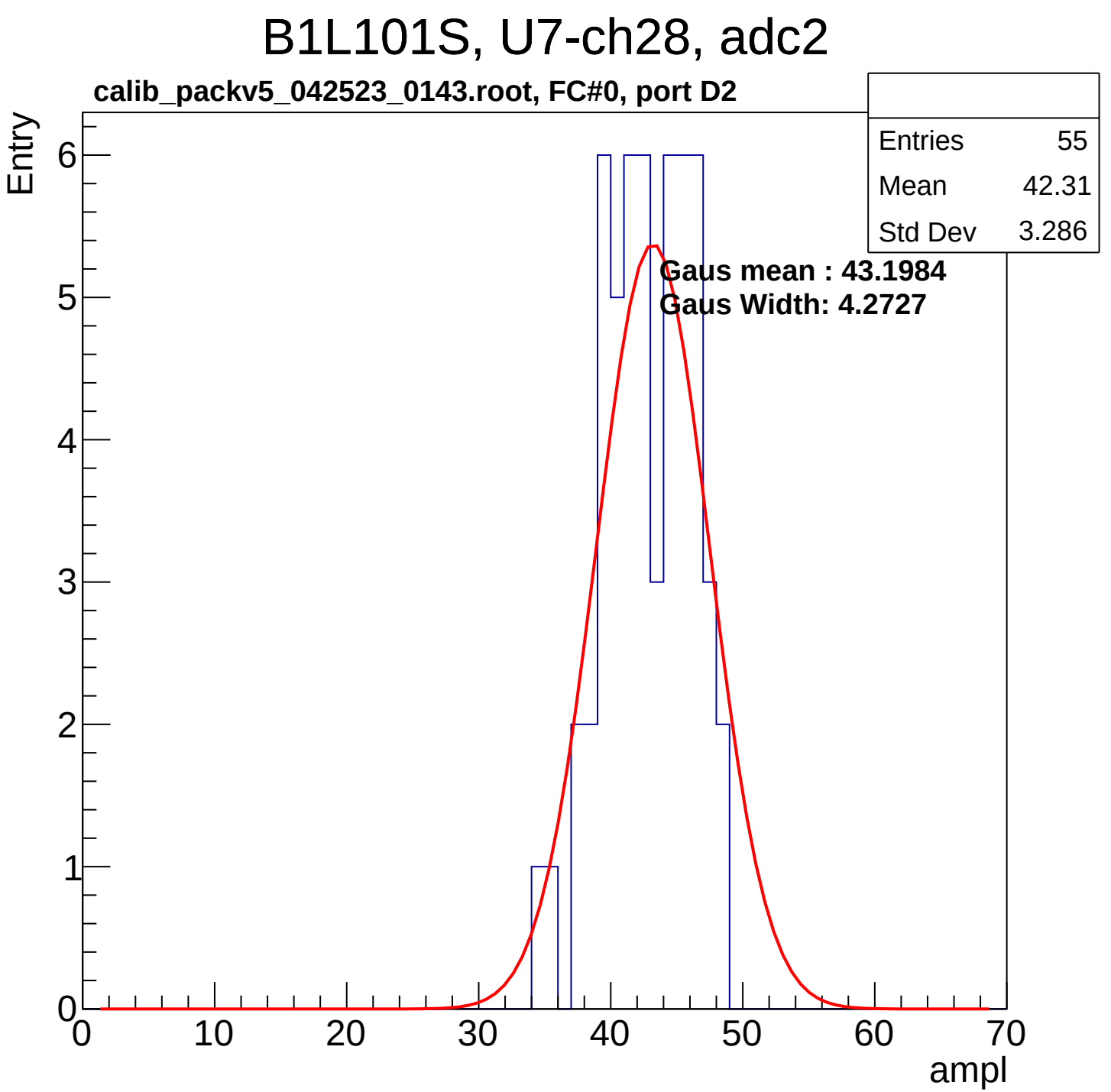
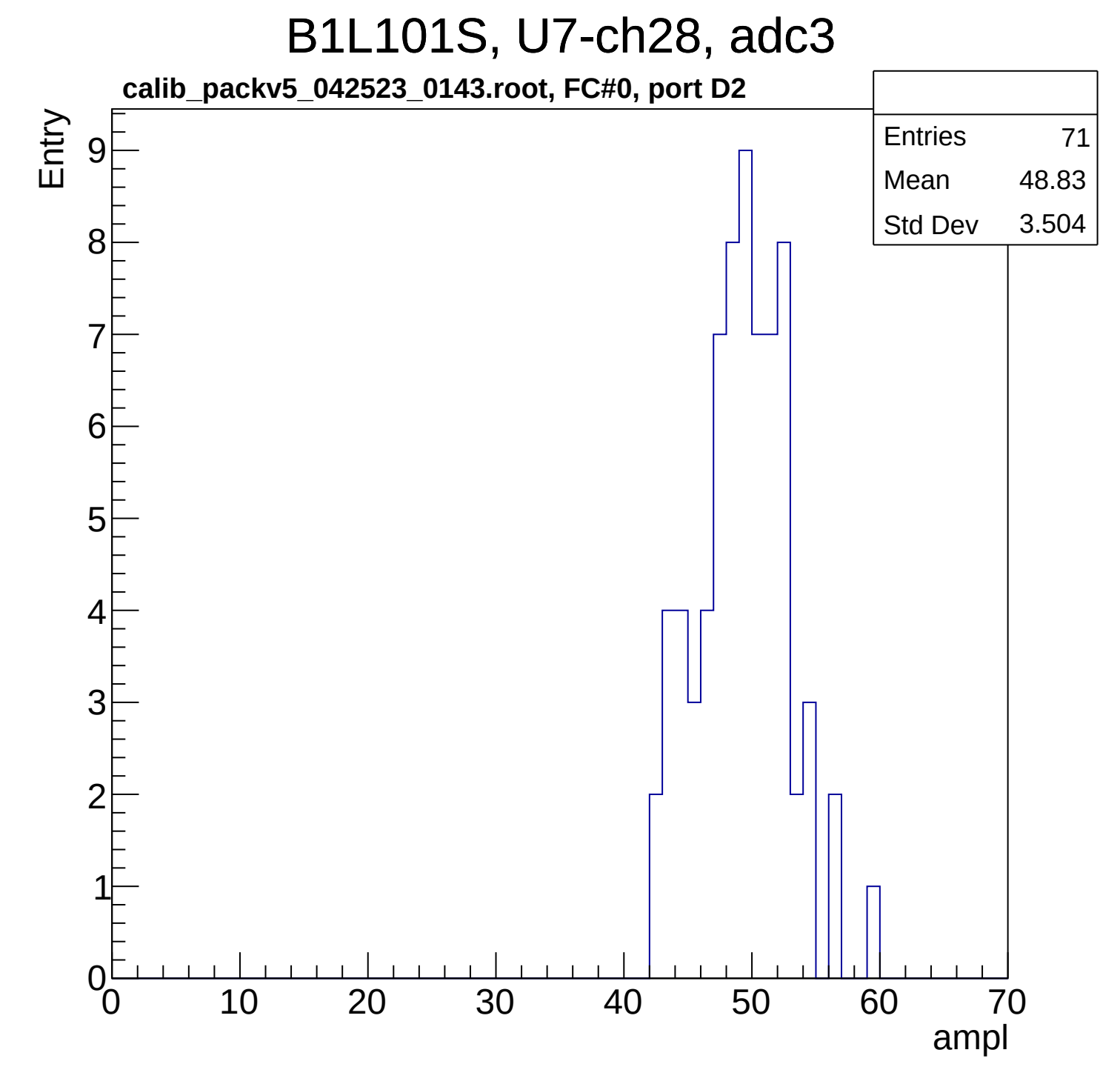

B1L101S, U7-ch27, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 63
Std Dev 0
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch27, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch28, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 30.72
Std Dev 4.857
Gaus mean : 31.6217
Gaus Width: 3.5068
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch28, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 36.61
Std Dev 6.087
Gaus mean : 38.2592
Gaus Width: 4.0345
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch28, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 42.31
Std Dev 3.286
Gaus mean : 43.1984
Gaus Width: 4.2727
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L101S, U7-ch28, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 48.83
Std Dev 3.504
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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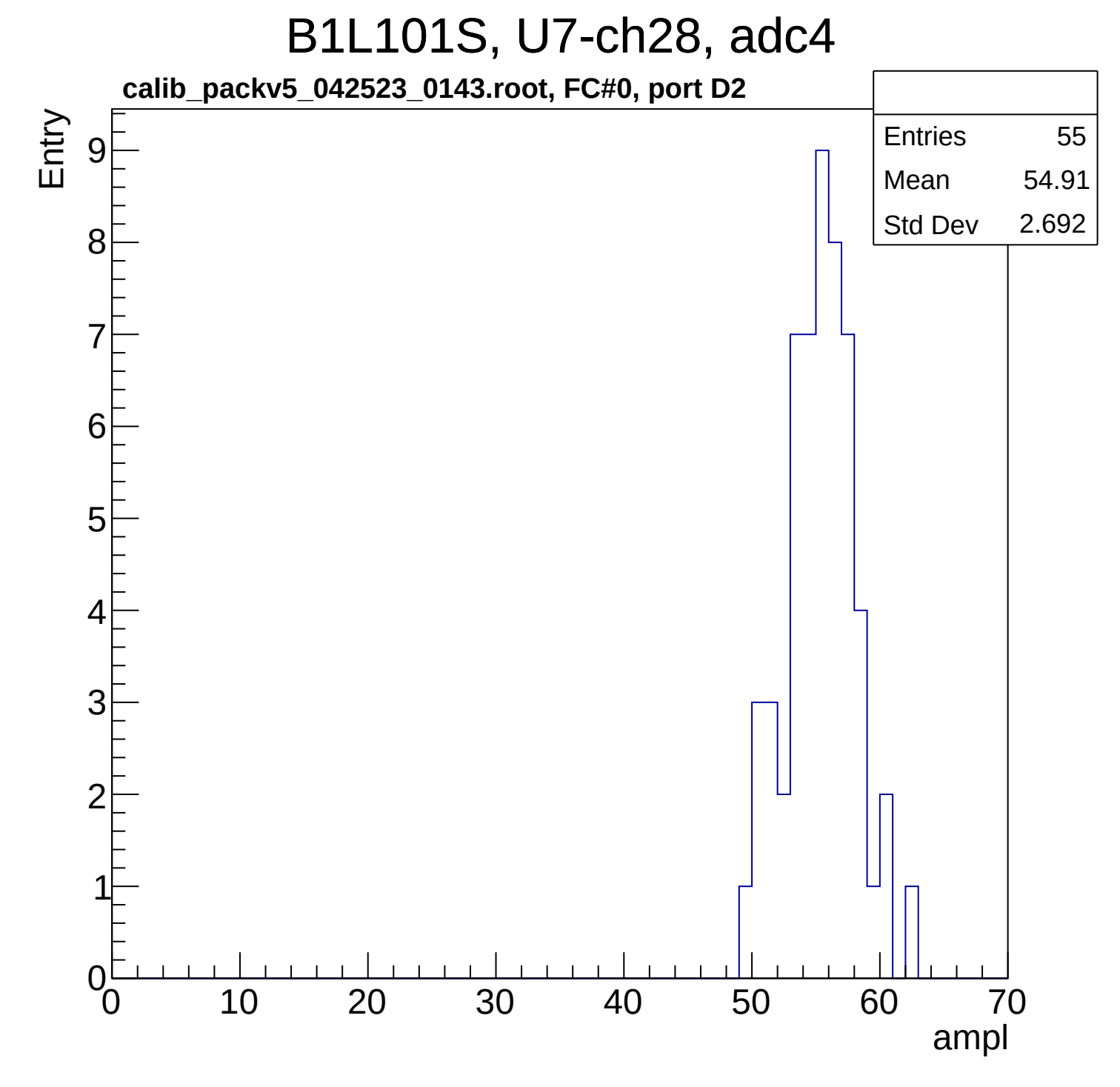
B1L101S, U7-ch28, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 54.91
Std Dev 2.692
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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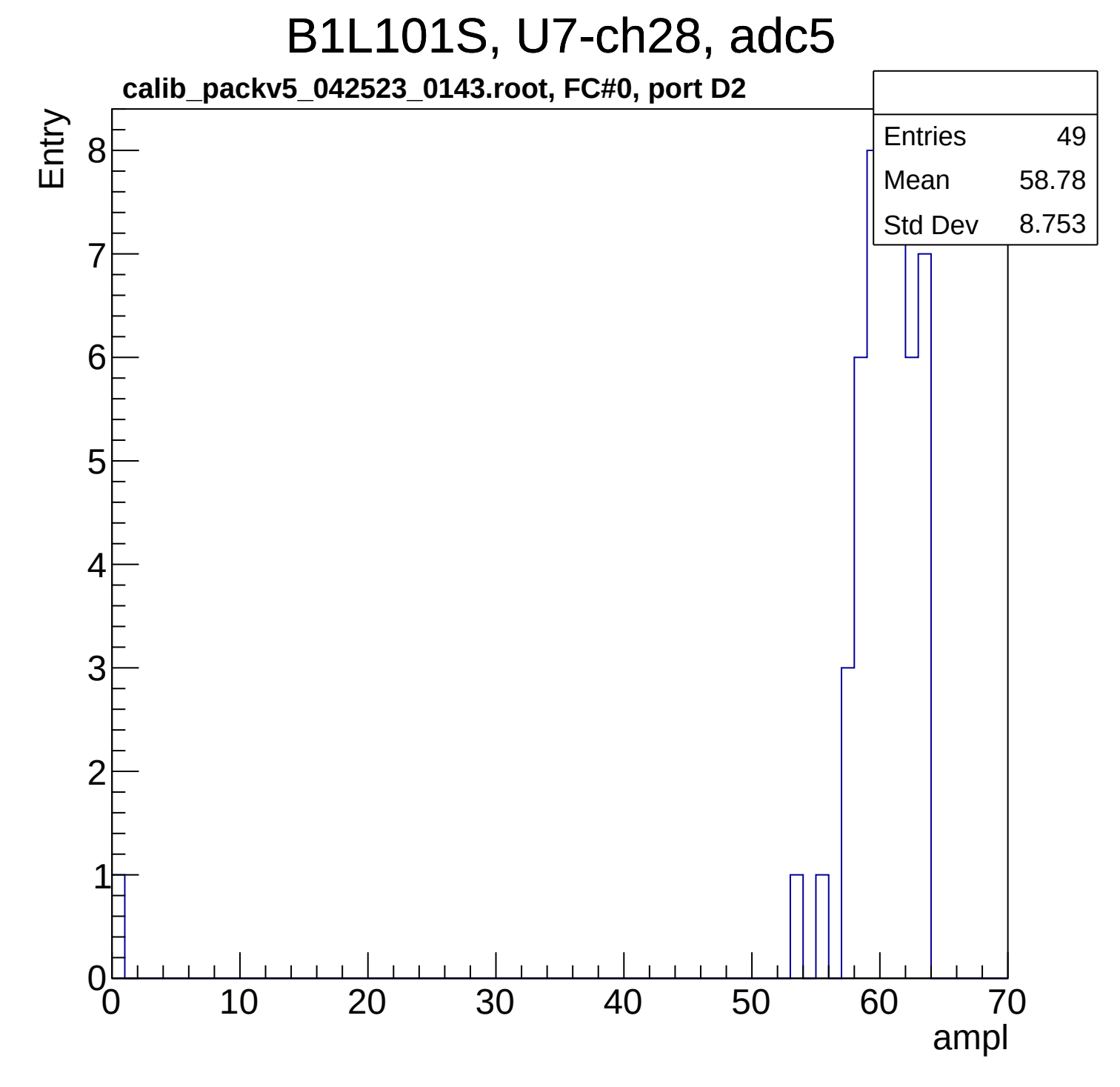
B1L101S, U7-ch28, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 58.78
Std Dev 8.753
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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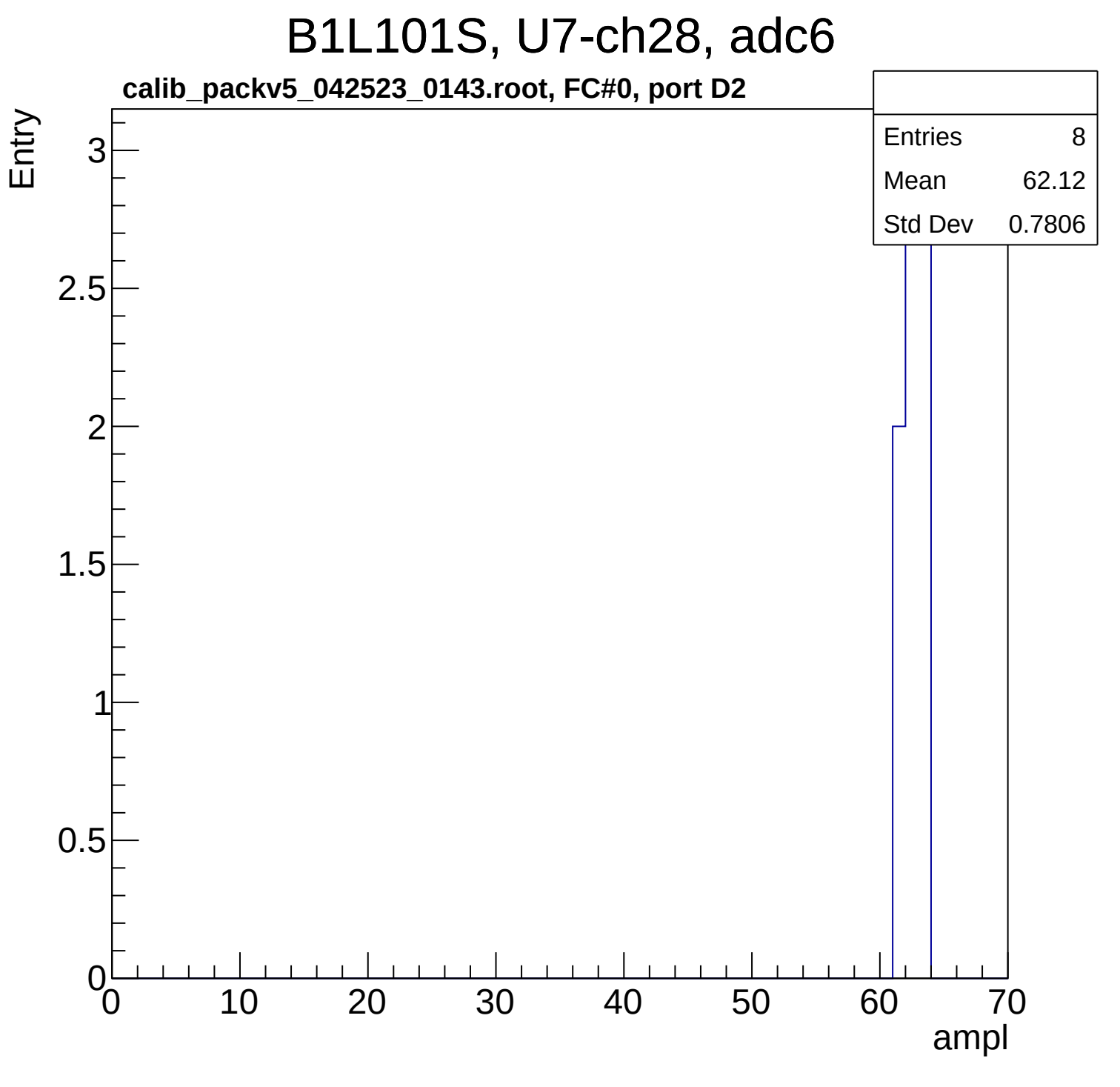
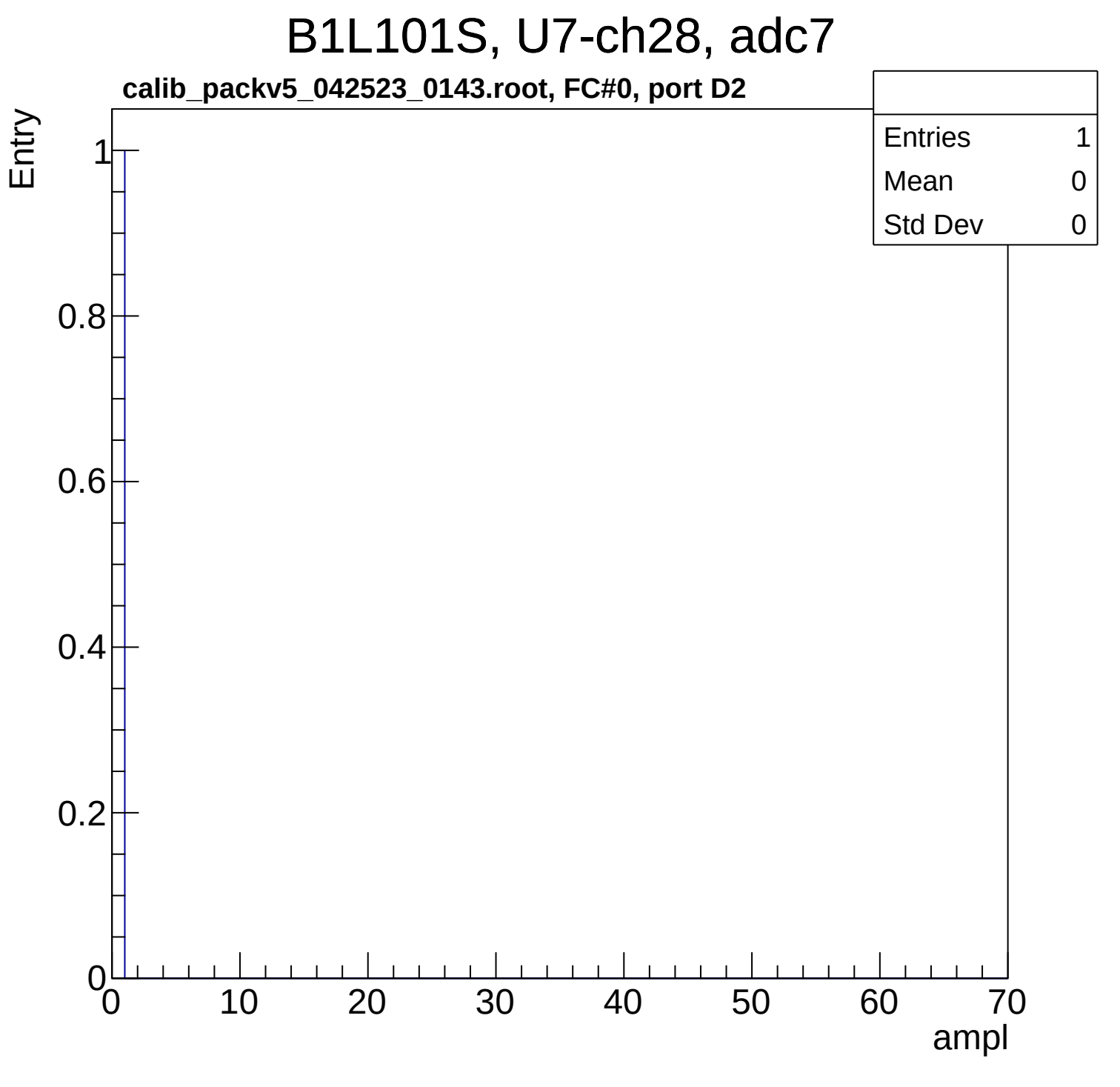
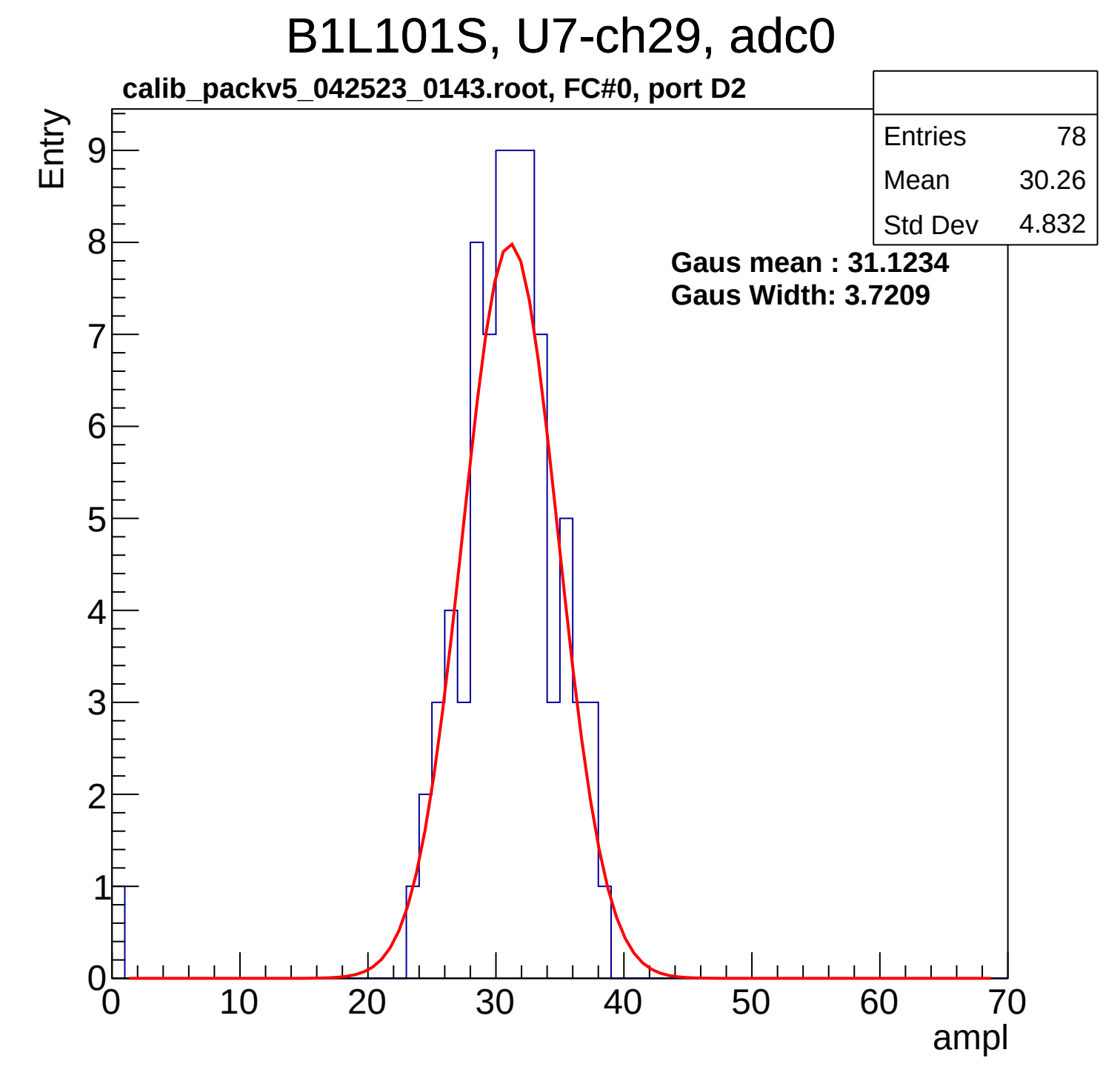

B1L101S, U7-ch28, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 62.12
Std Dev 0.7806
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch28, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch29, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 30.26
Std Dev 4.832
Gaus mean : 31.1234
Gaus Width: 3.7209
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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40
50
60
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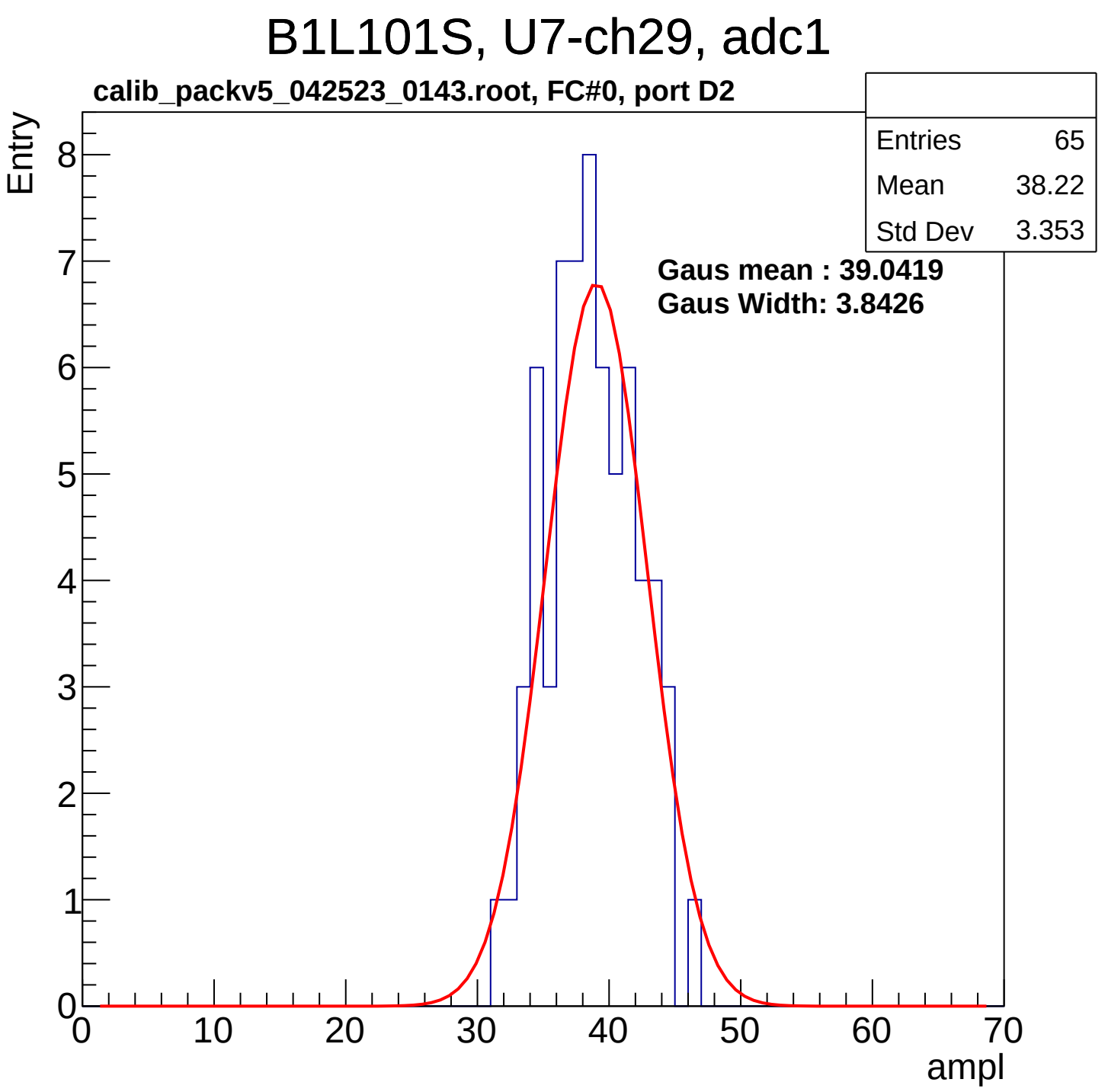
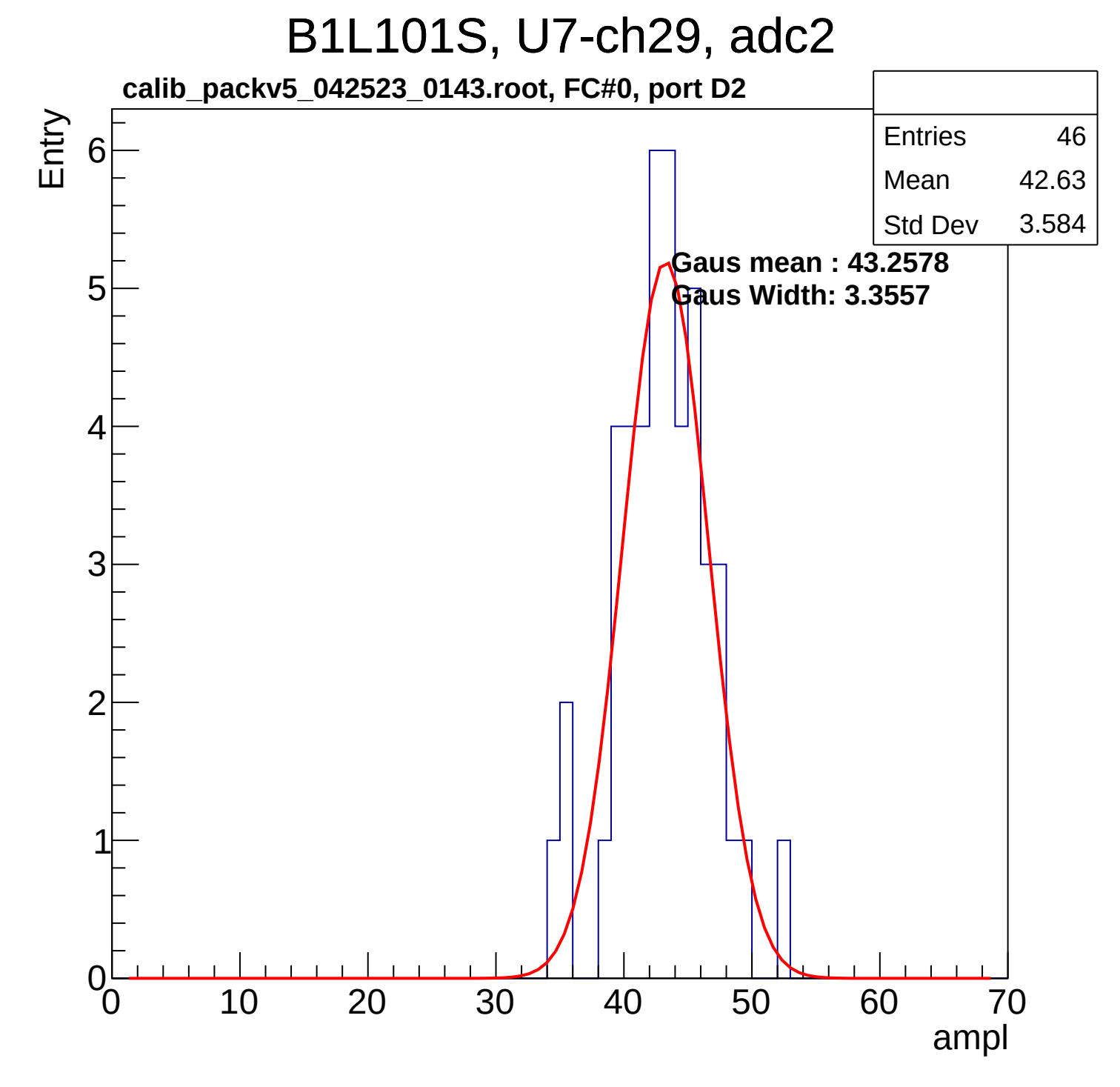

B1L101S, U7-ch29, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 38.22
Std Dev 3.353
Gaus mean : 39.0419
Gaus Width: 3.8426
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch29, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 42.63
Std Dev 3.584
Gaus mean : 43.2578
Gaus Width: 3.3557
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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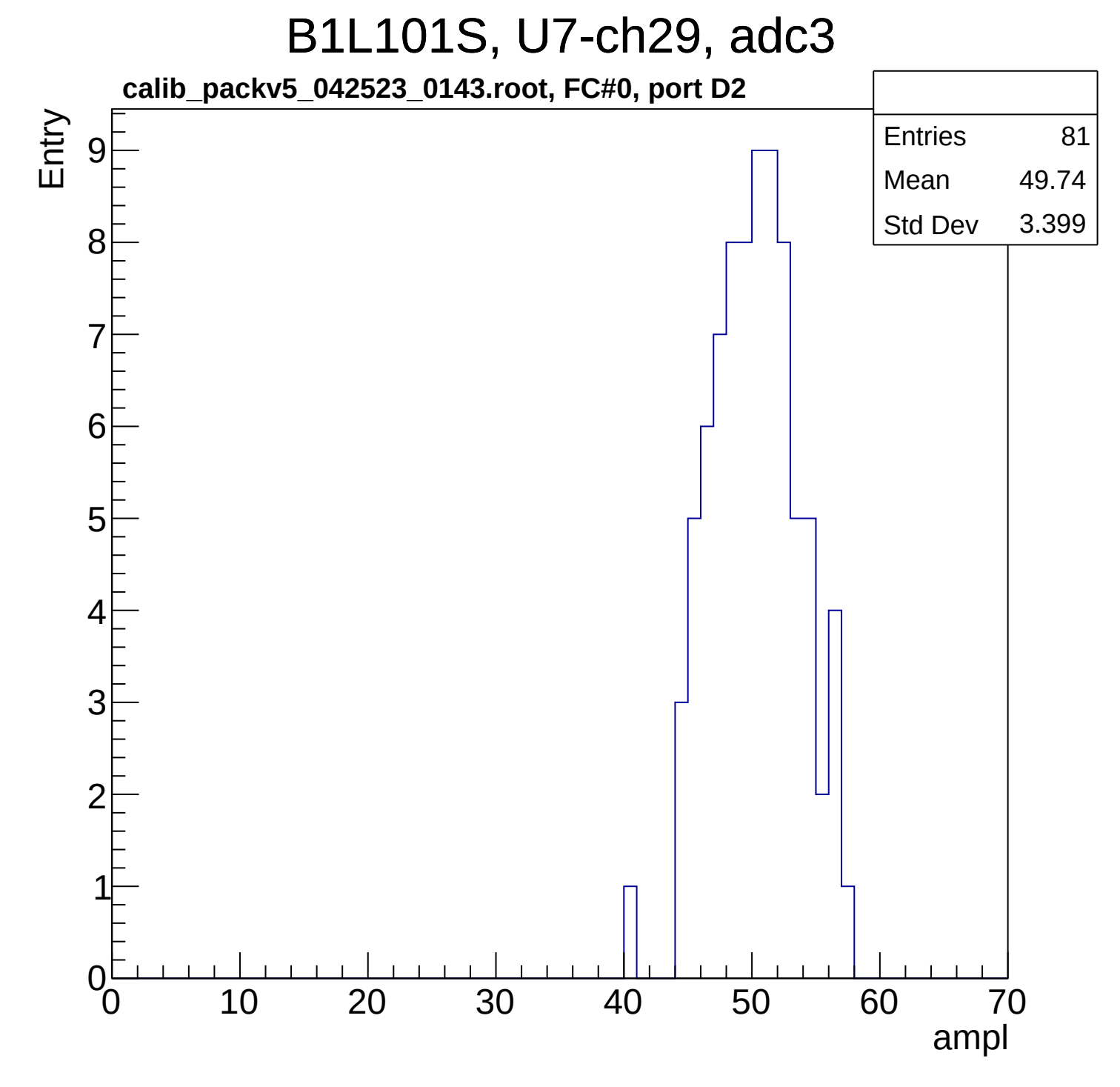
B1L101S, U7-ch29, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 81
Mean 49.74
Std Dev 3.399
Entry
ampl
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3
4
5
6
7
8
9
0
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60
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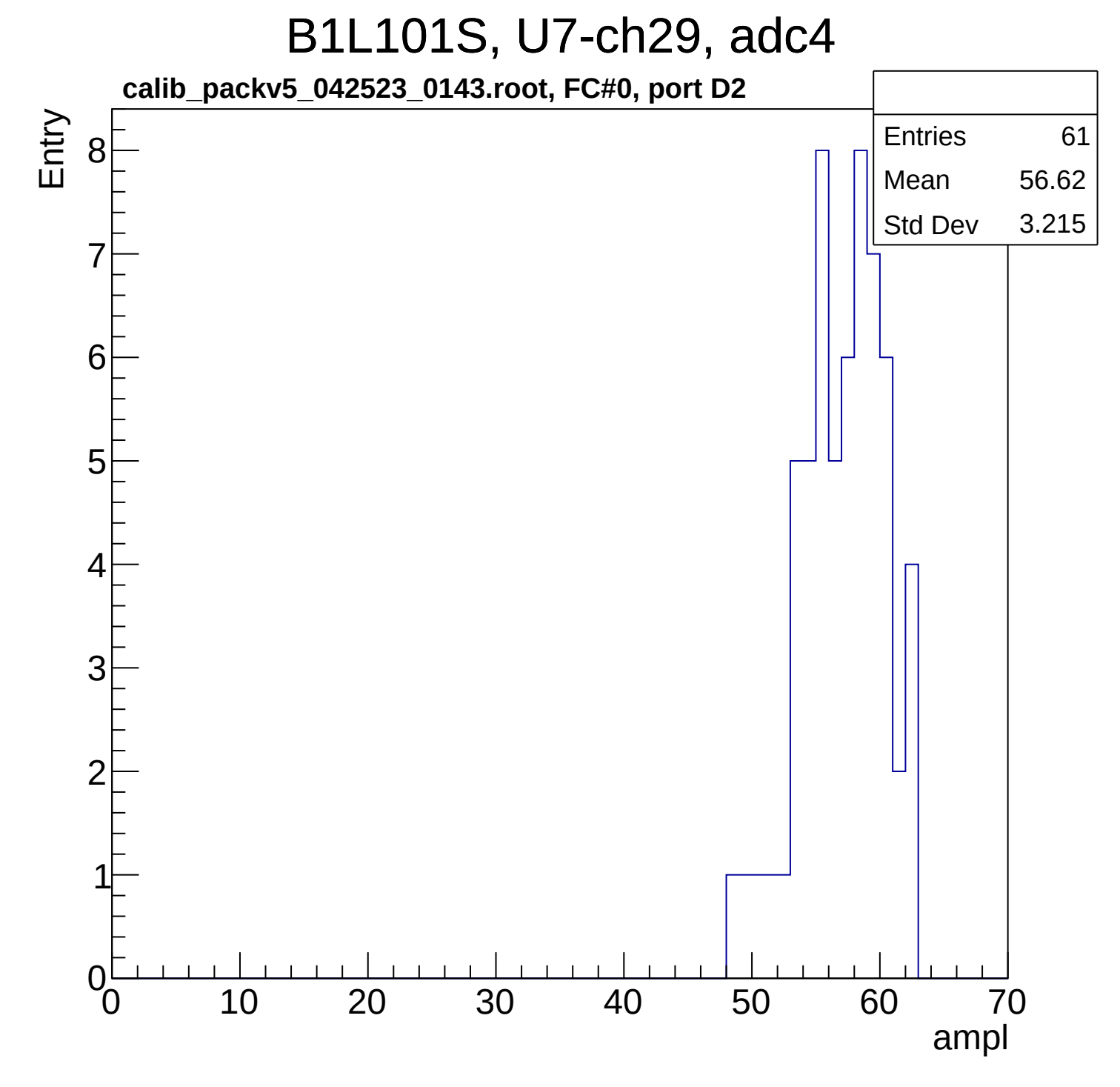
B1L101S, U7-ch29, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 56.62
Std Dev 3.215
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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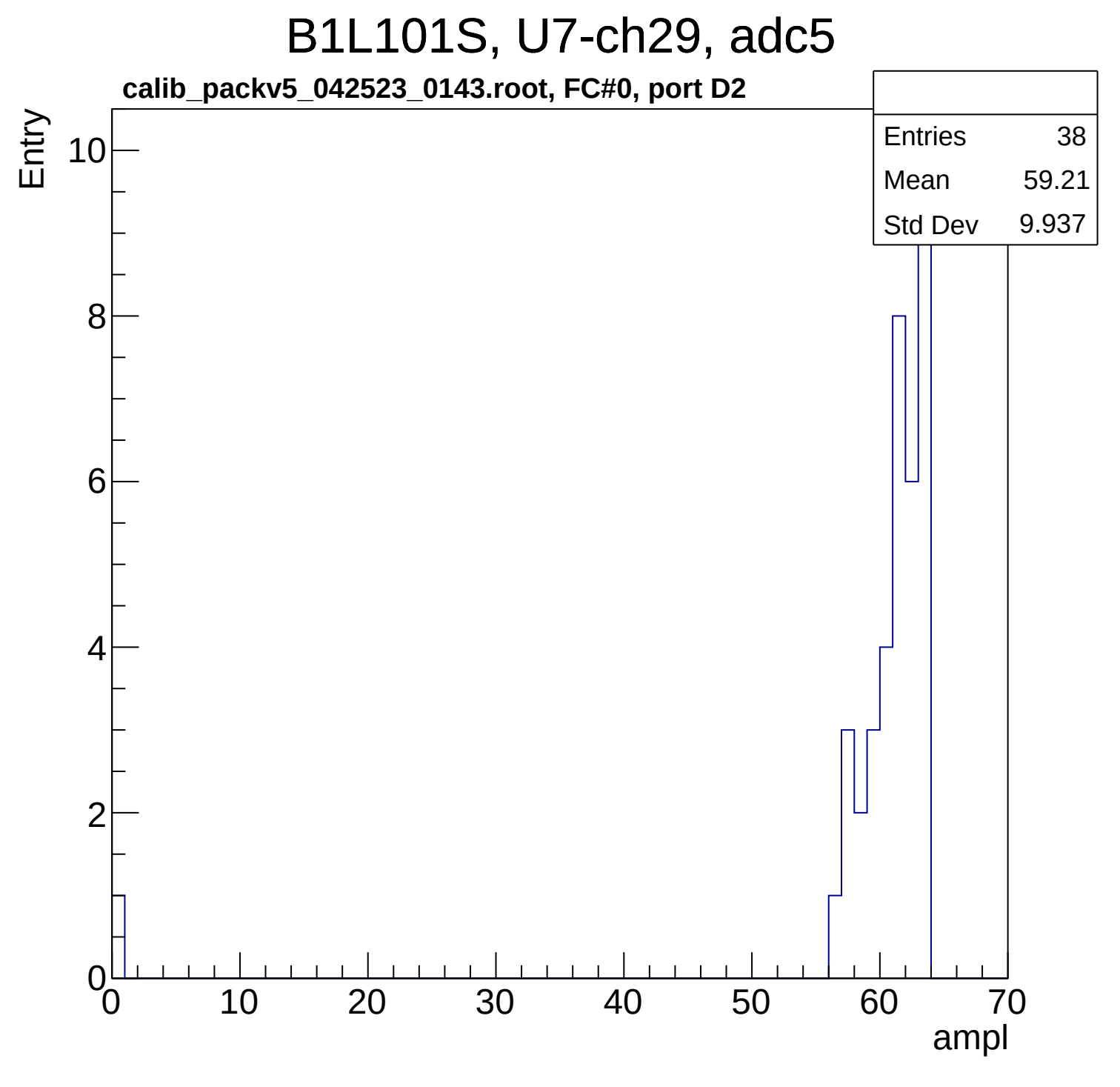
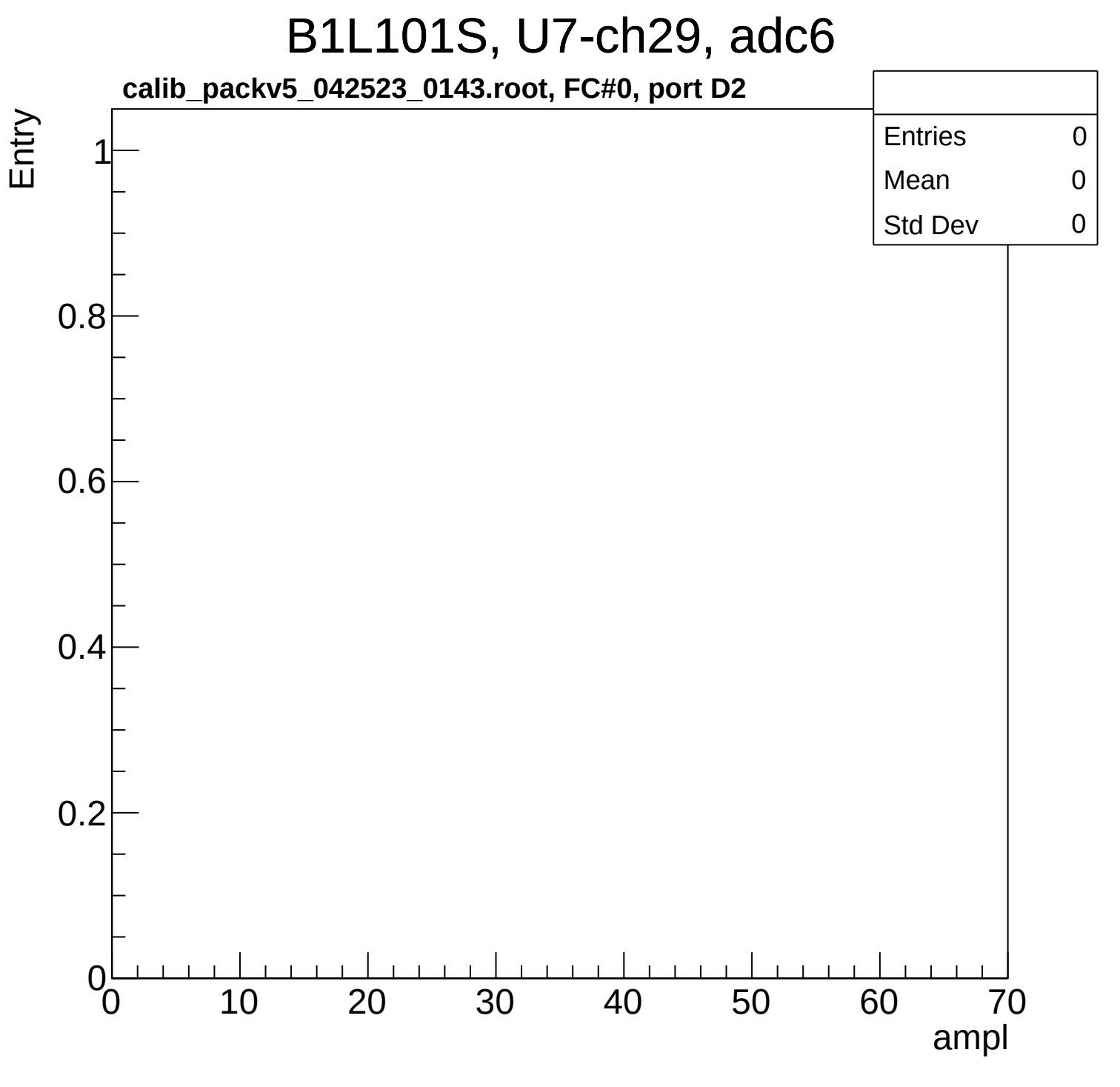

B1L101S, U7-ch29, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 38
Mean 59.21
Std Dev 9.937
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch29, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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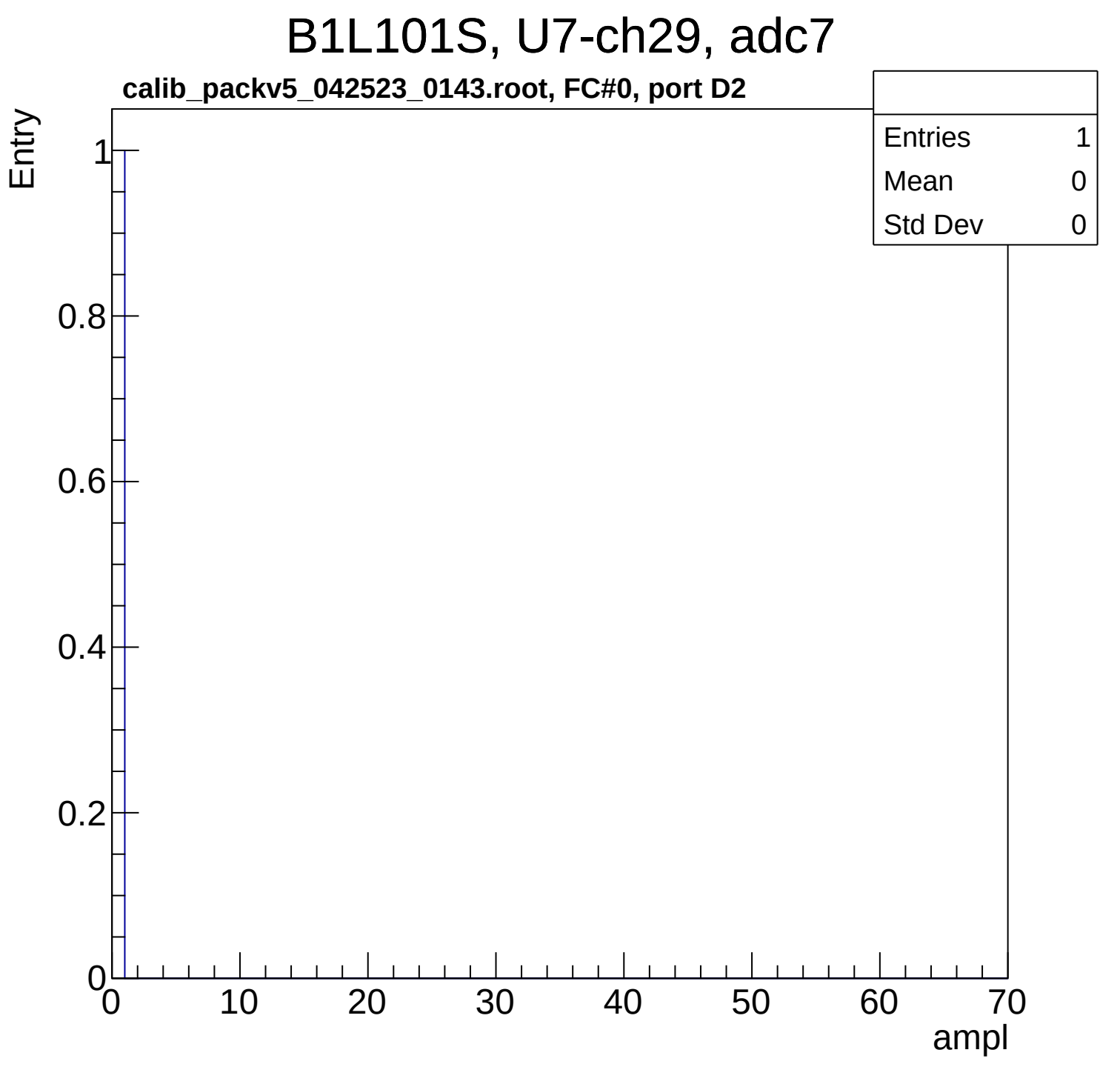
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch29, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
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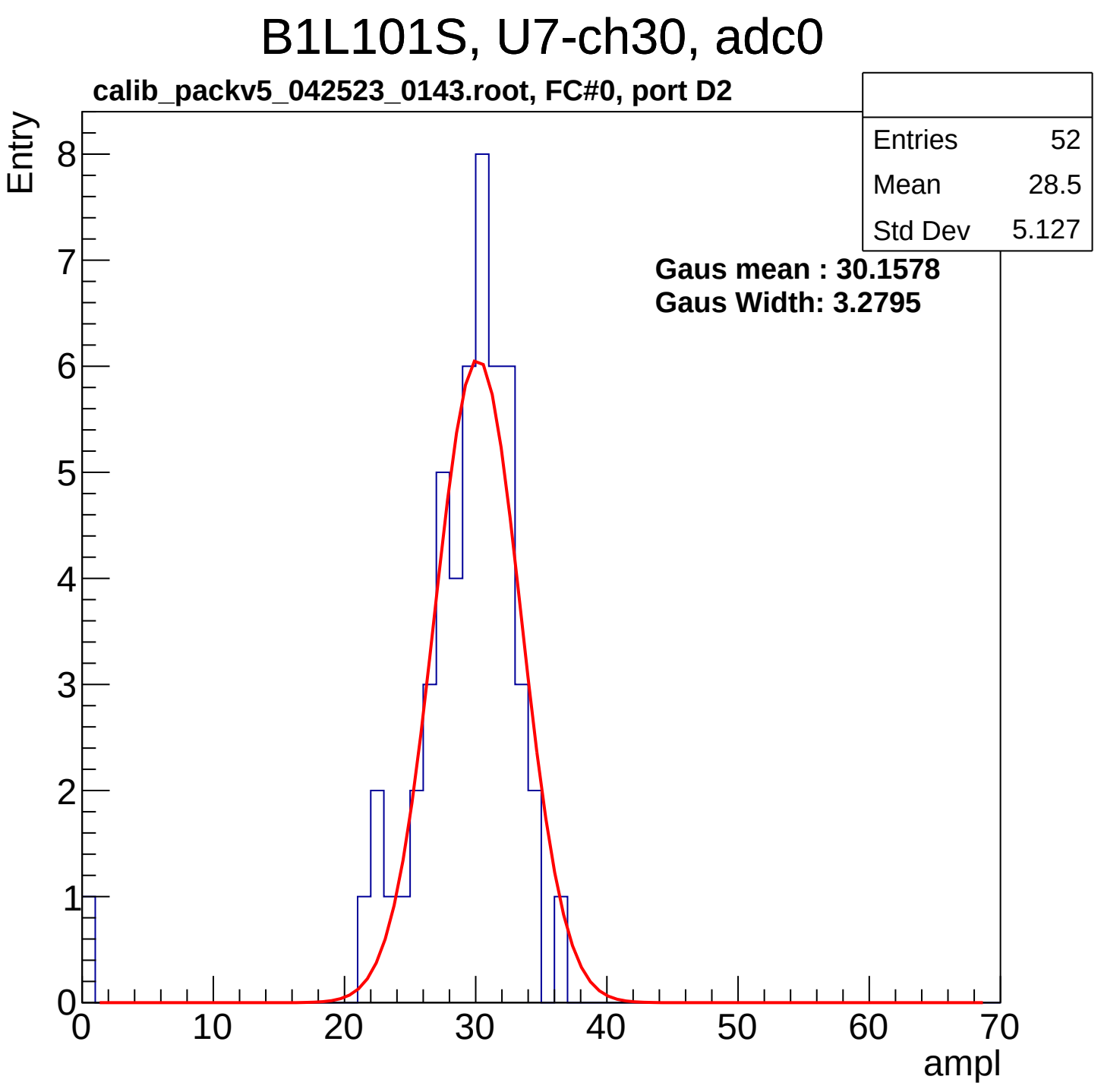
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch30, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 28.5
Std Dev 5.127
Gaus mean : 30.1578
Gaus Width: 3.2795
Entry
ampl
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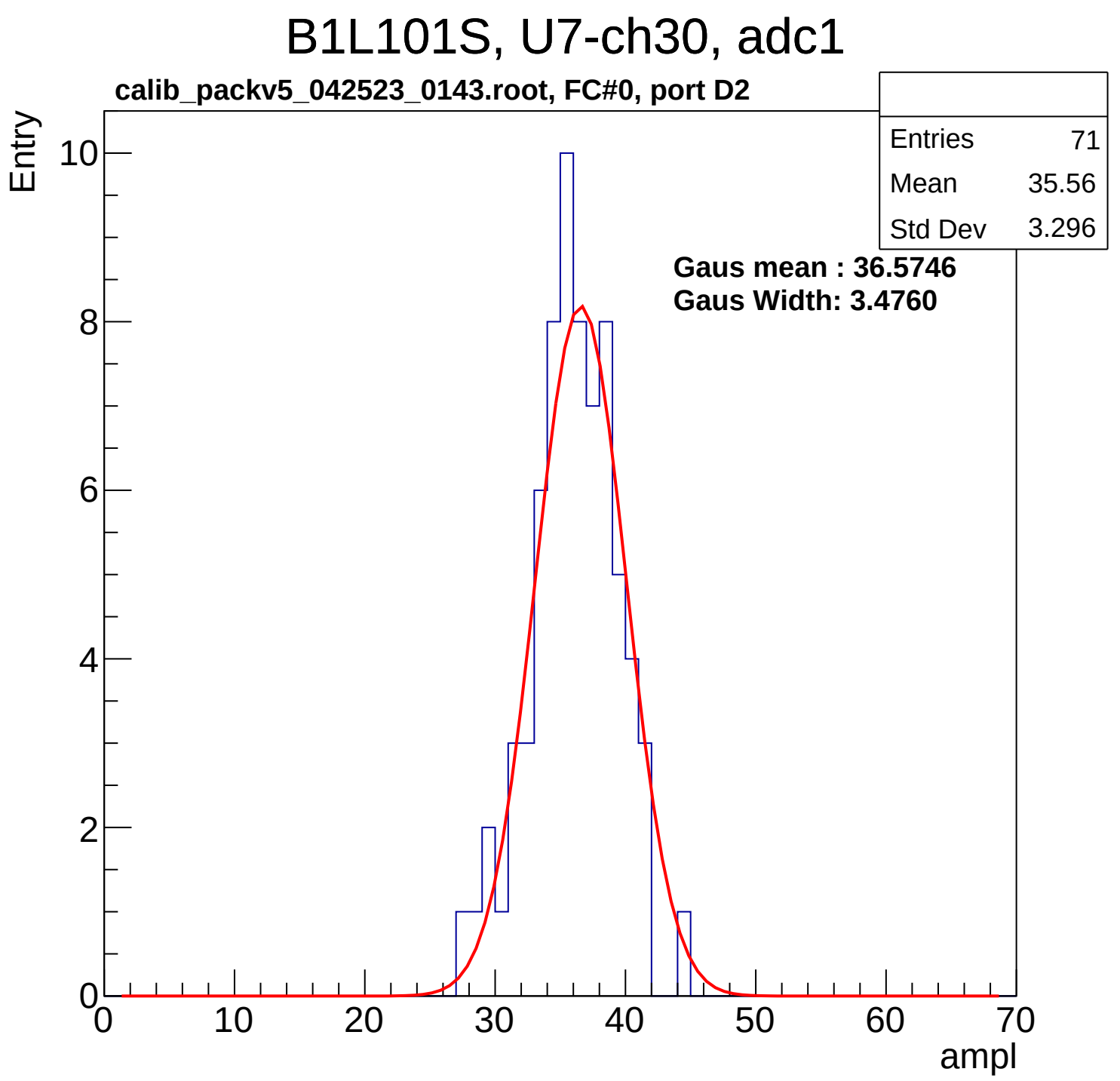
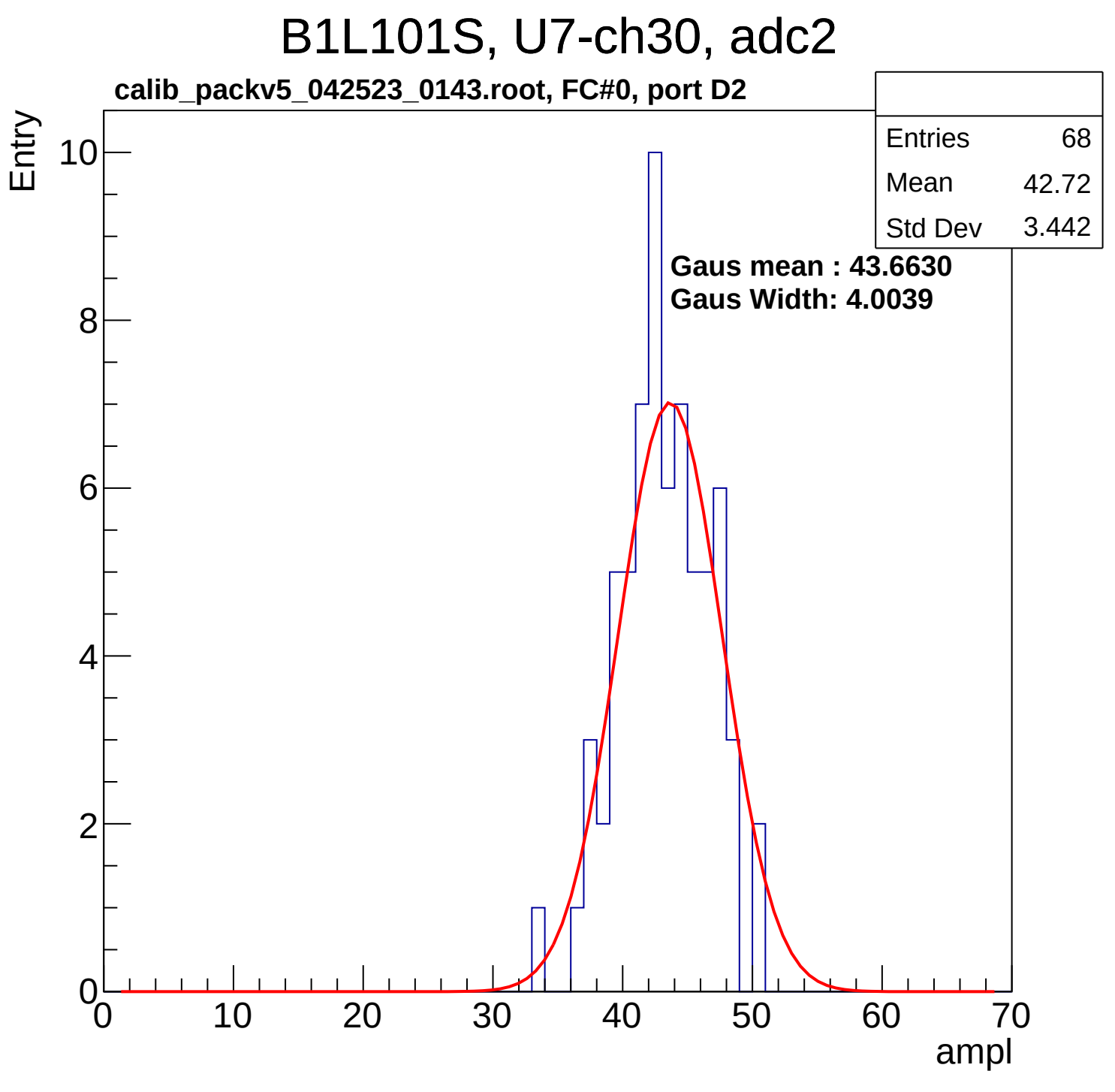
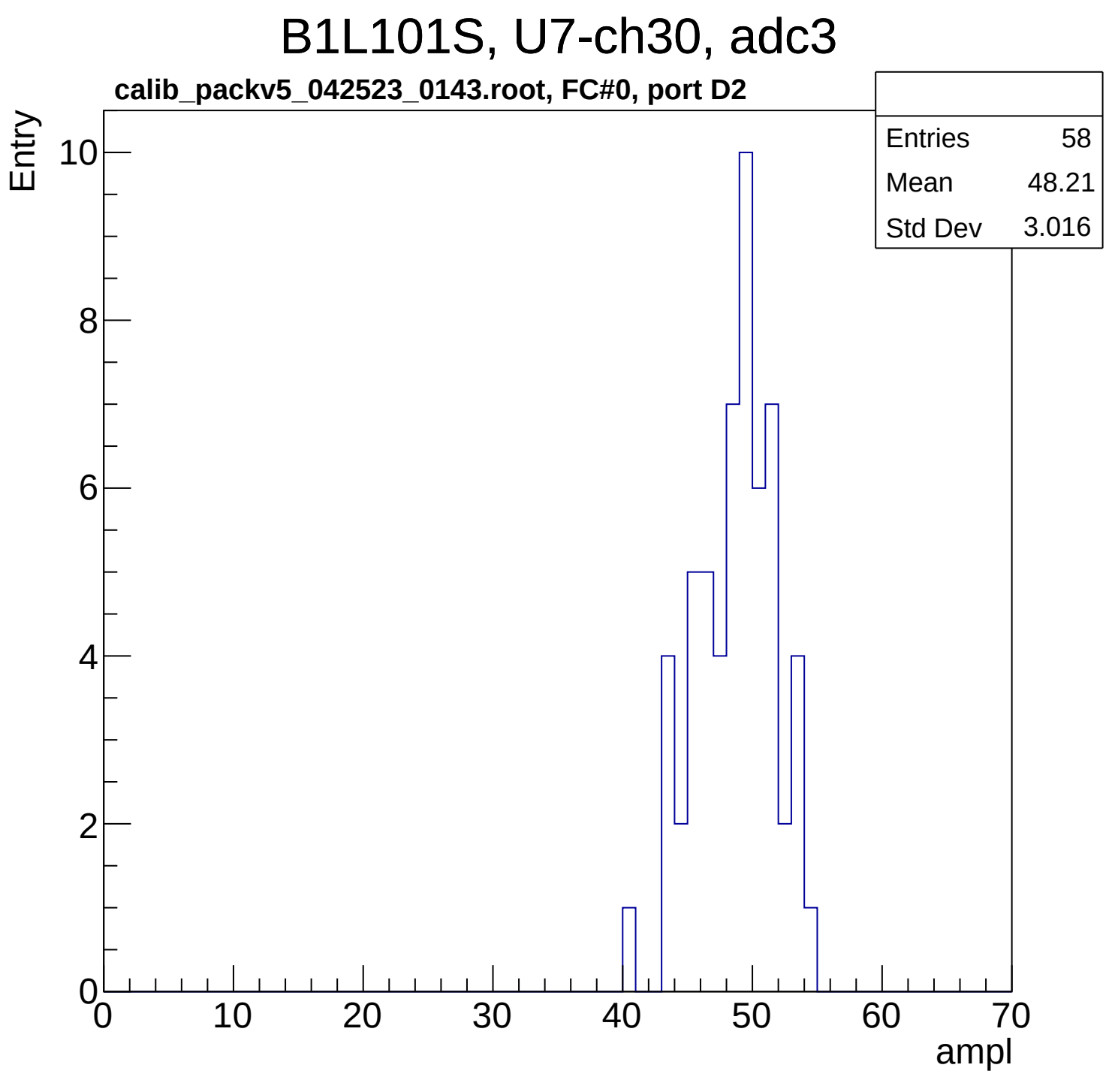
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch30, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 35.56
Std Dev 3.296
Gaus mean : 36.5746
Gaus Width: 3.4760
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch30, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 42.72
Std Dev 3.442
Gaus mean : 43.6630
Gaus Width: 4.0039
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch30, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 48.21
Std Dev 3.016
Entry
ampl
0
2
4
6
8
10
0
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20
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40
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60
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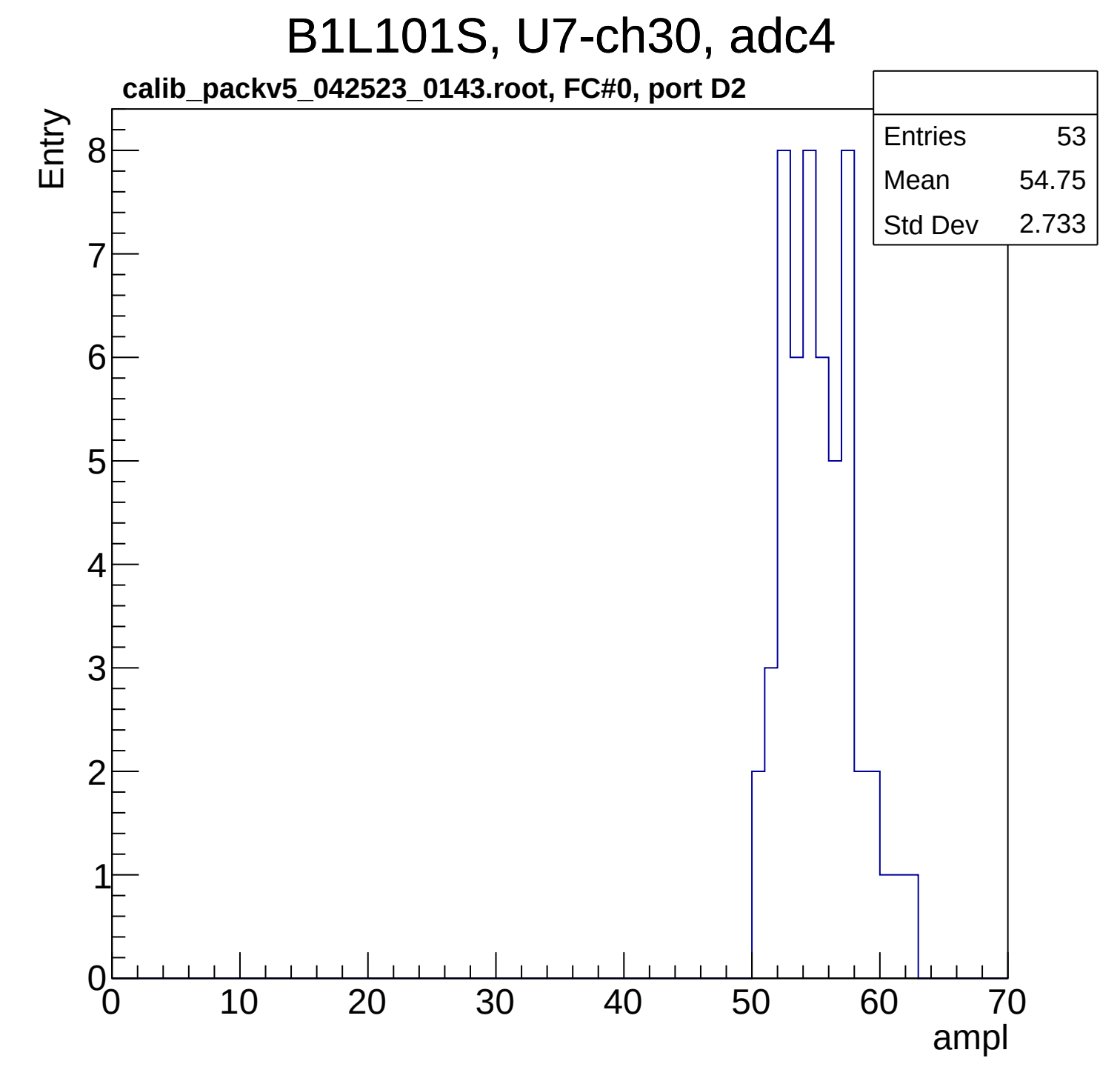
B1L101S, U7-ch30, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 54.75
Std Dev 2.733
Entry
ampl
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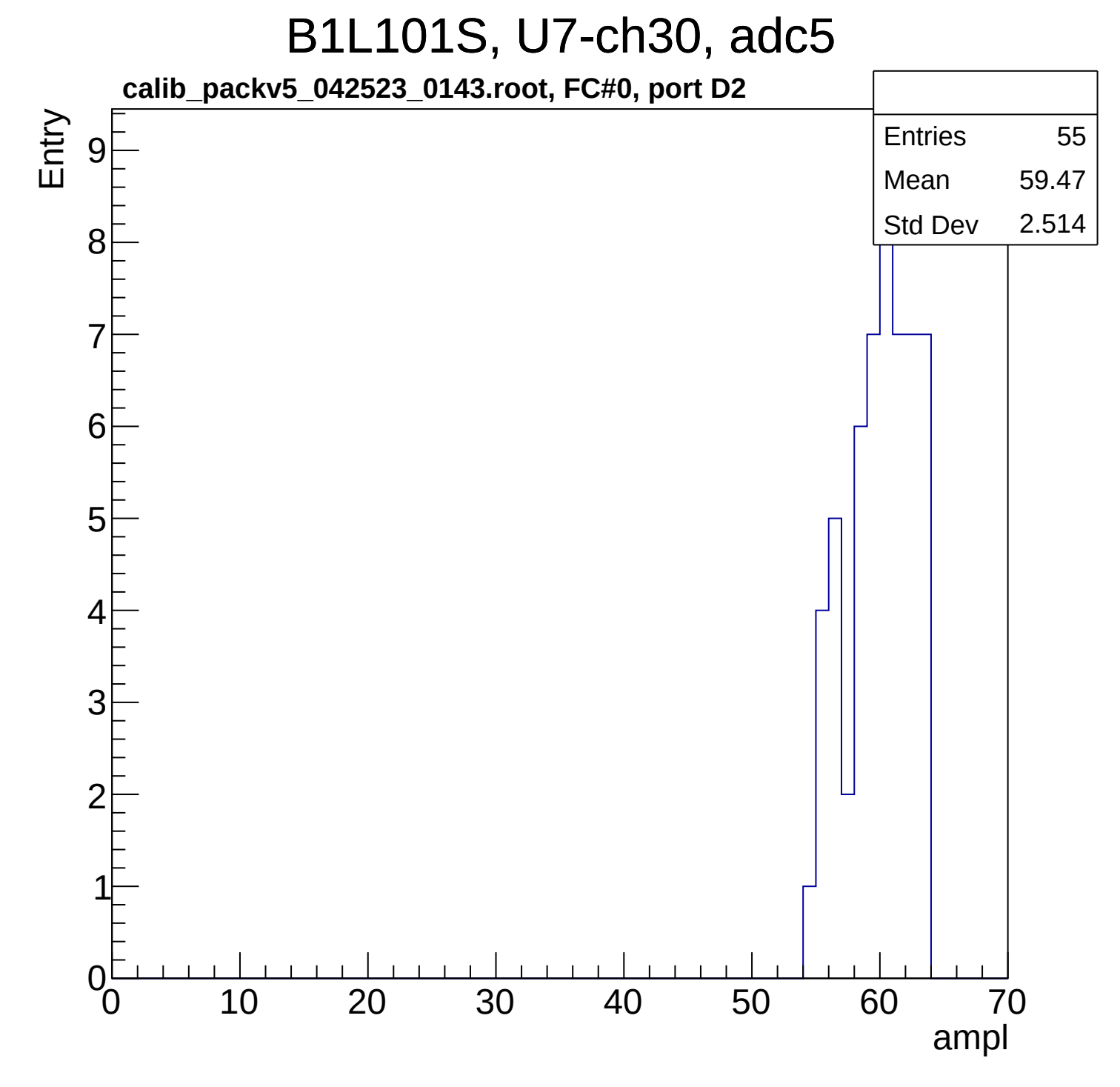
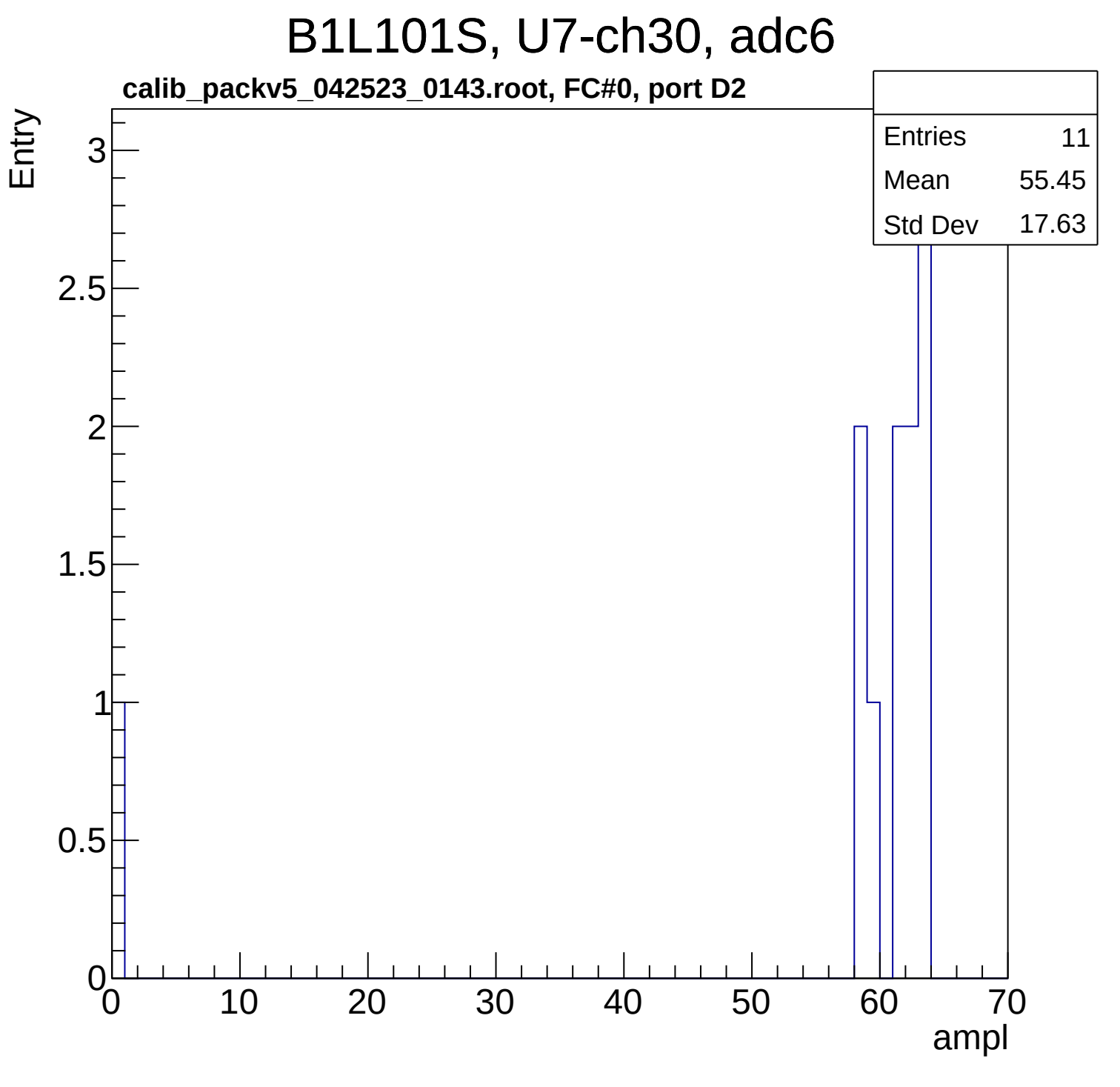
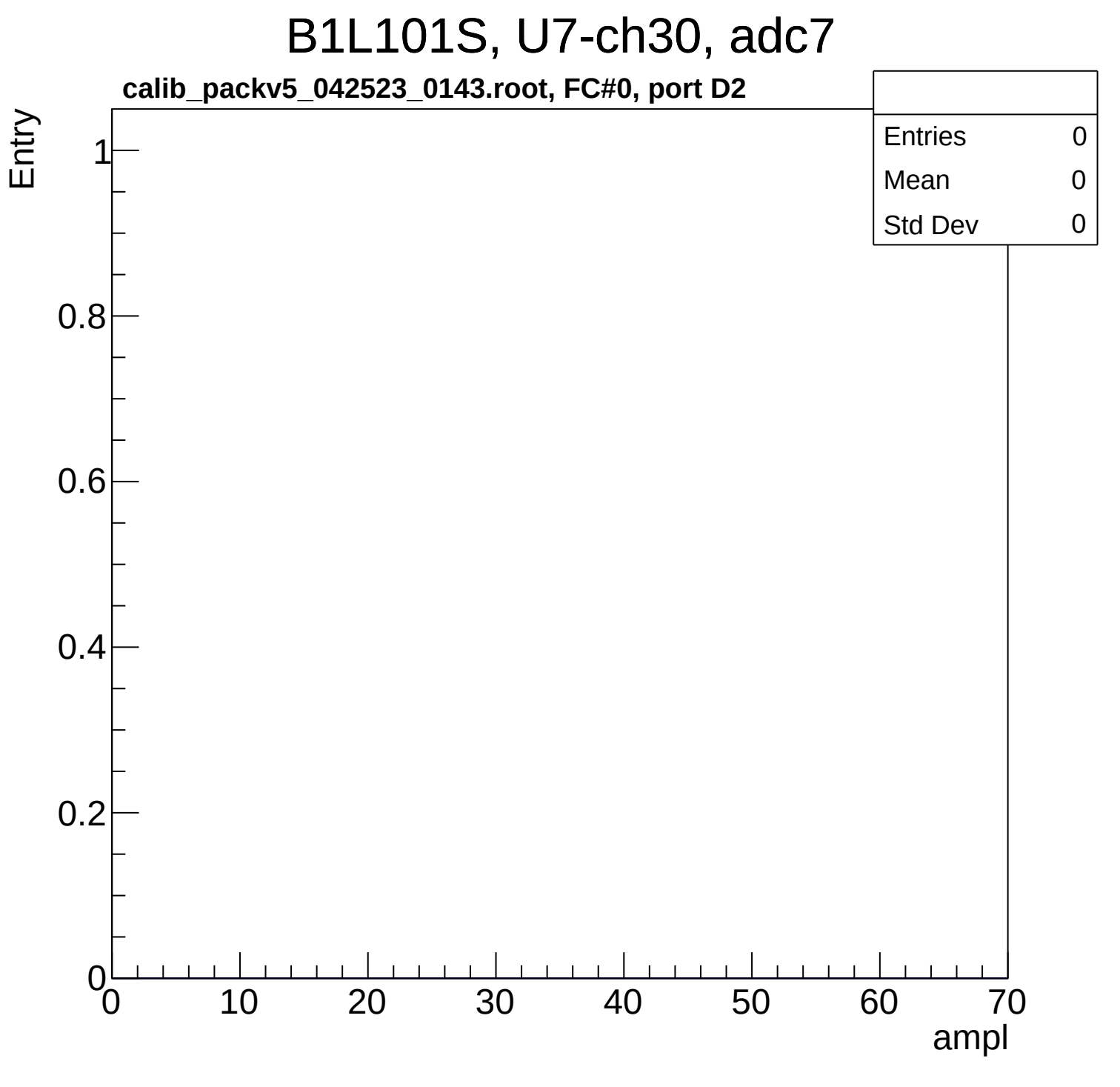
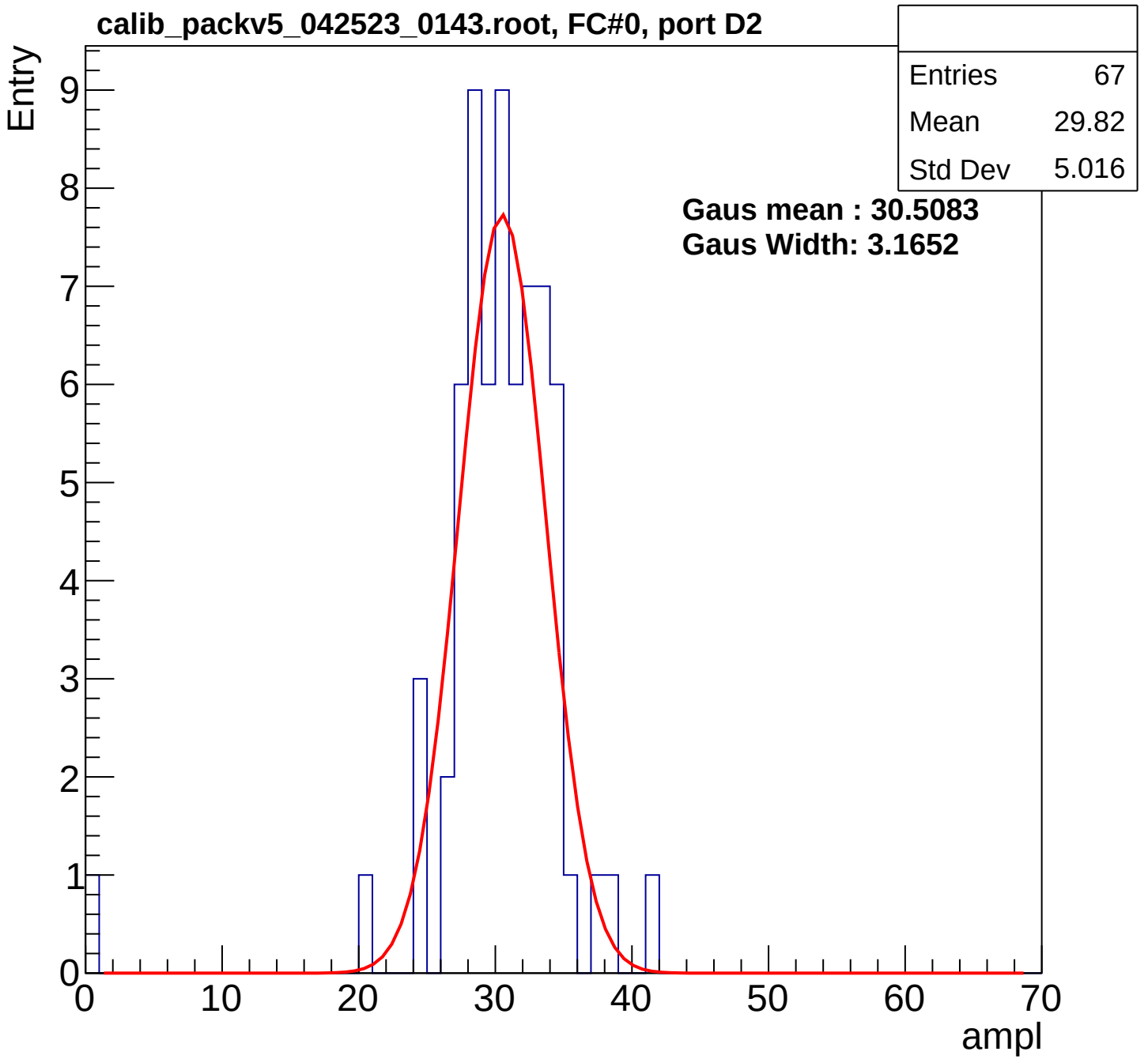
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch30, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 59.47
Std Dev 2.514
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch30, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 11
Mean 55.45
Std Dev 17.63
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U7-ch30, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch31, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 29.82
Std Dev 5.016
Gaus mean : 30.5083
Gaus Width: 3.1652
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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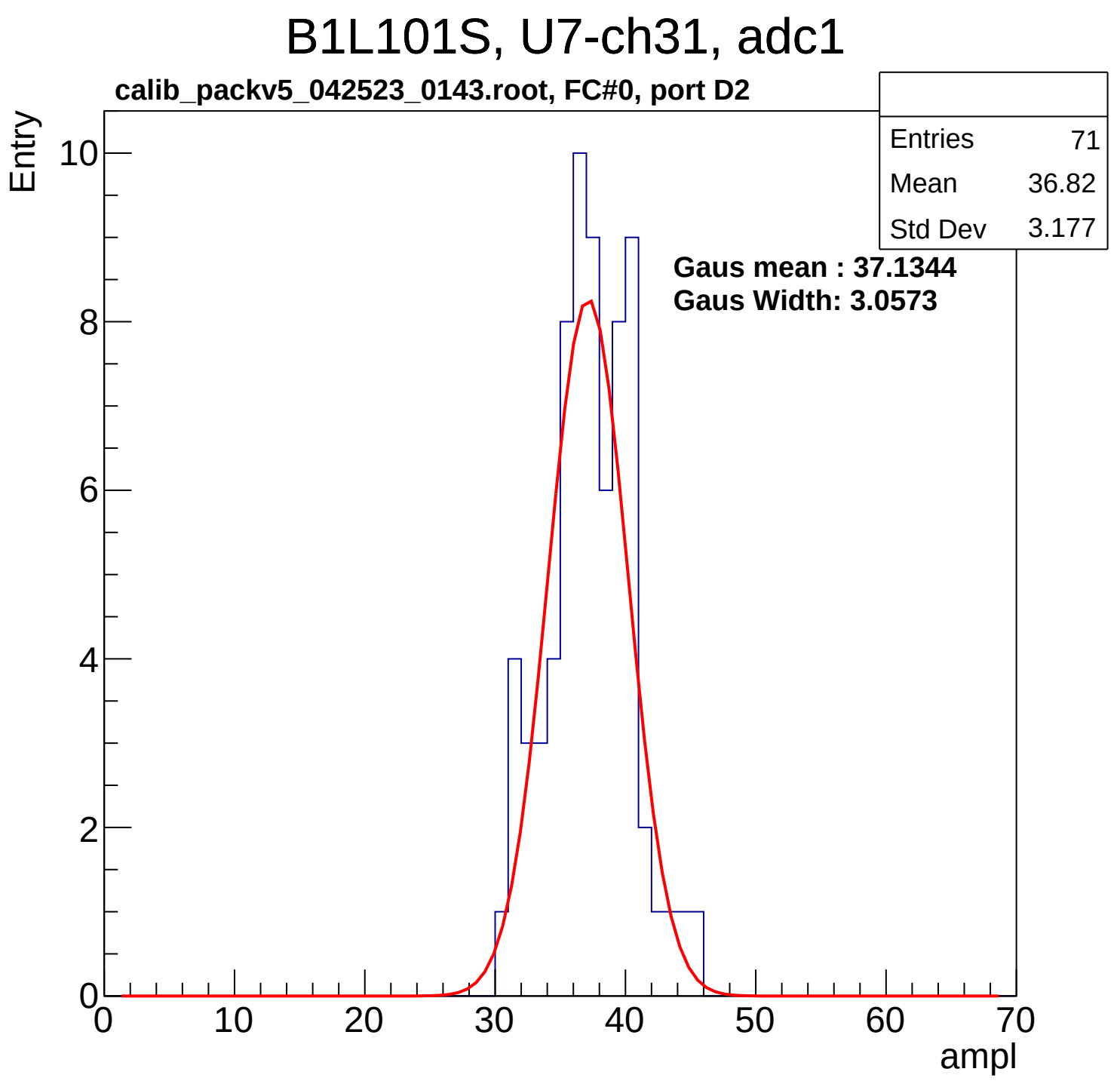
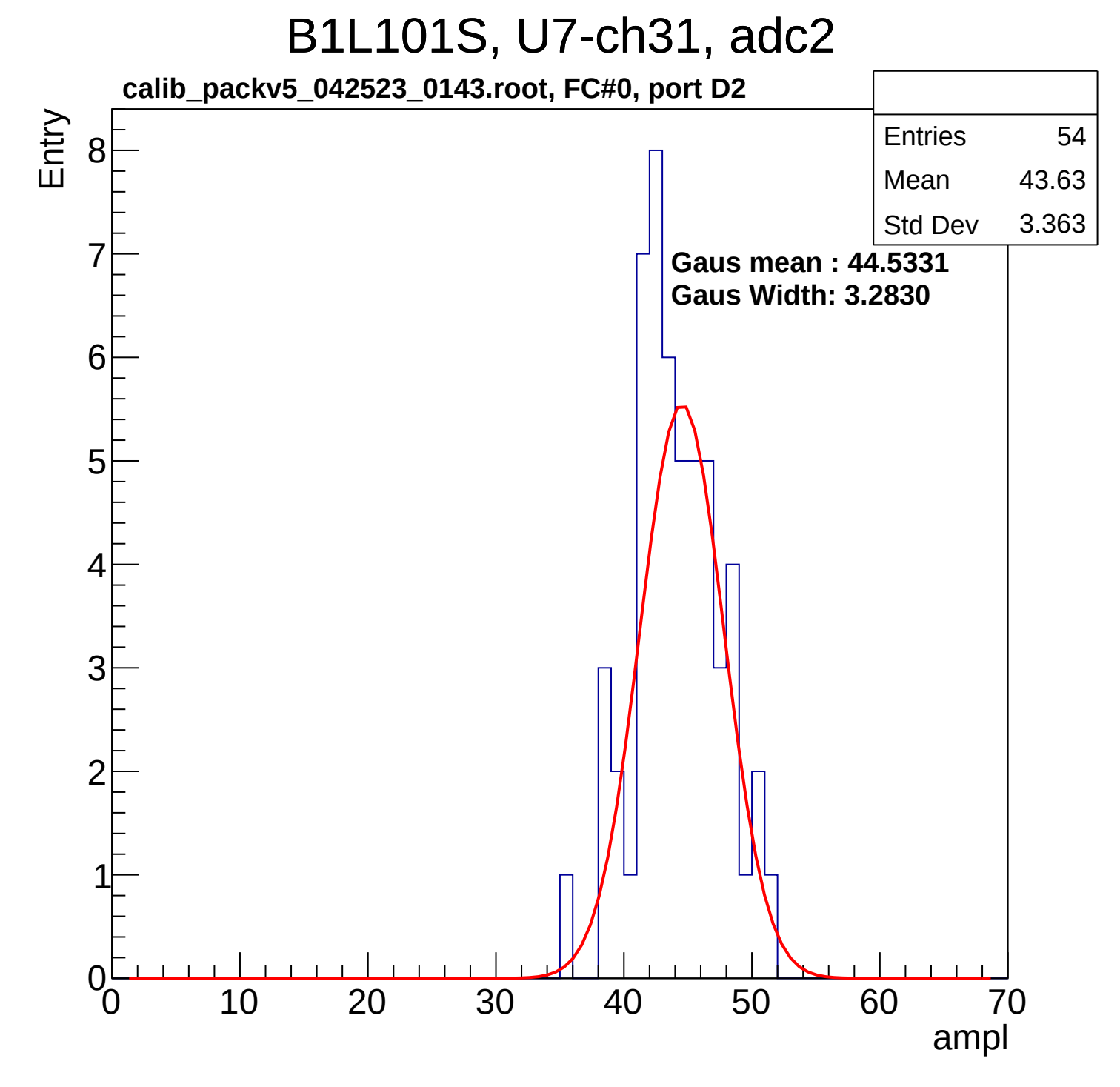

B1L101S, U7-ch31, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 36.82
Std Dev 3.177
Gaus mean : 37.1344
Gaus Width: 3.0573
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch31, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 43.63
Std Dev 3.363
Gaus mean : 44.5331
Gaus Width: 3.2830
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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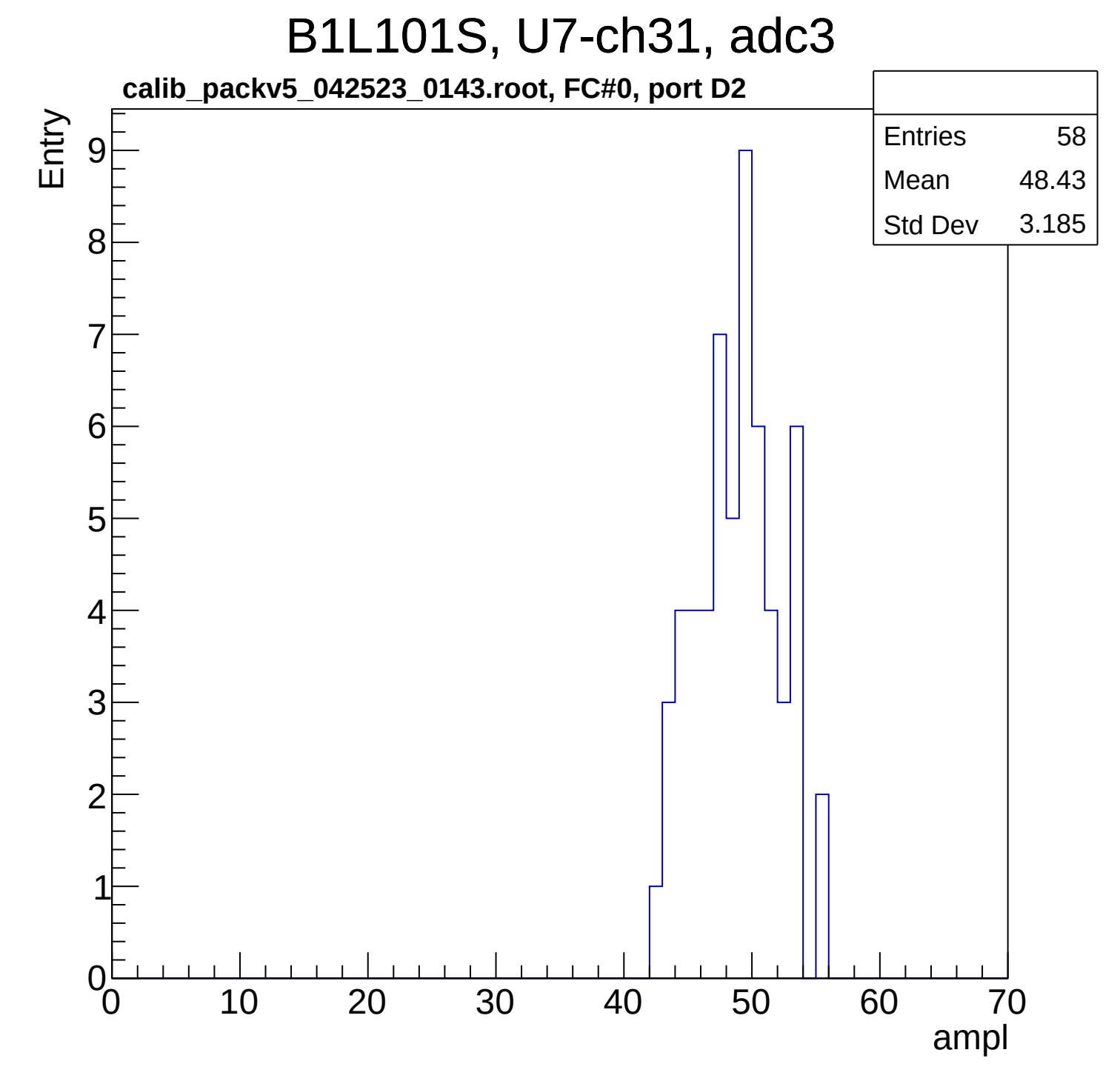
B1L101S, U7-ch31, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 48.43
Std Dev 3.185
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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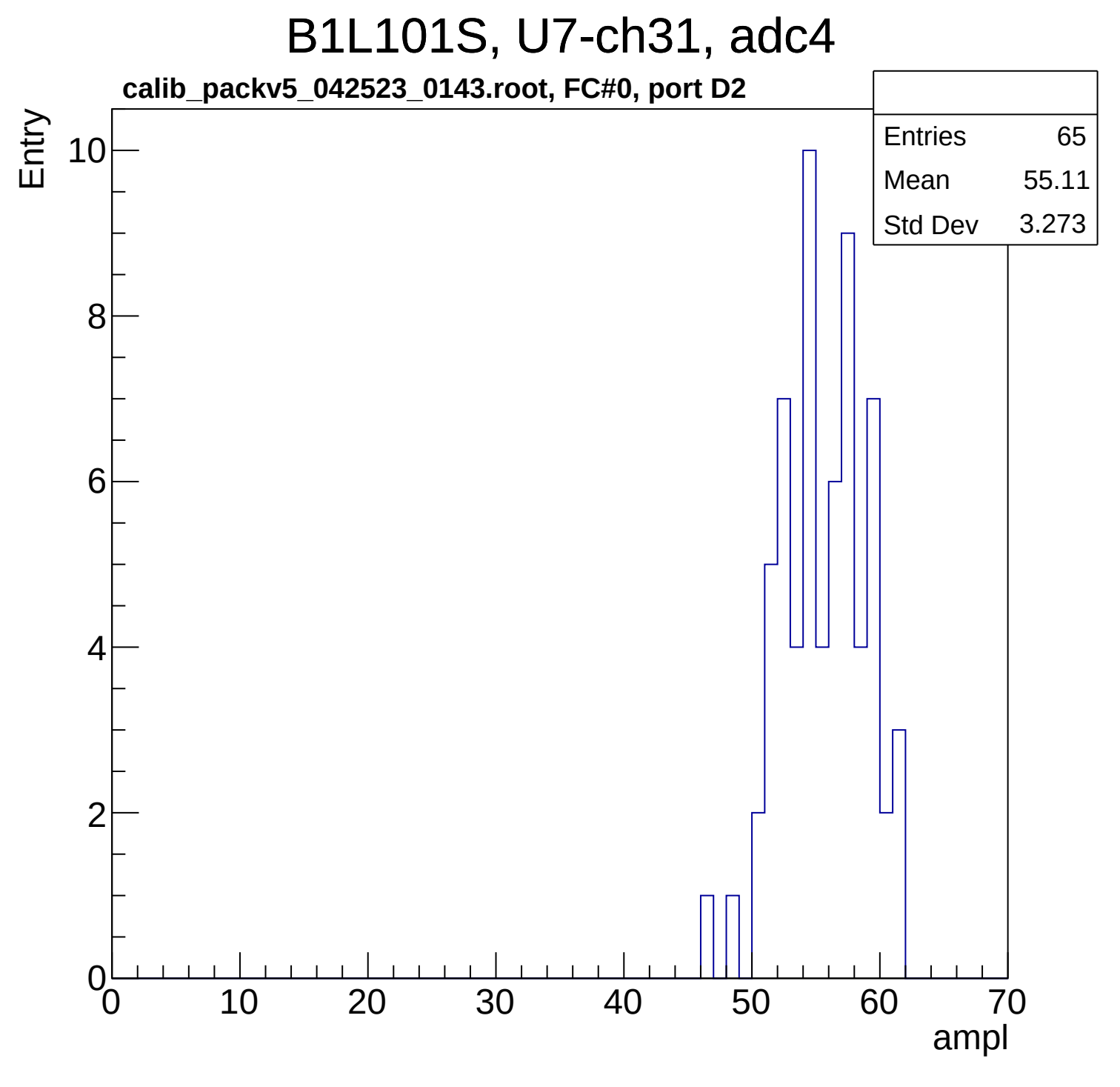
B1L101S, U7-ch31, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 55.11
Std Dev 3.273
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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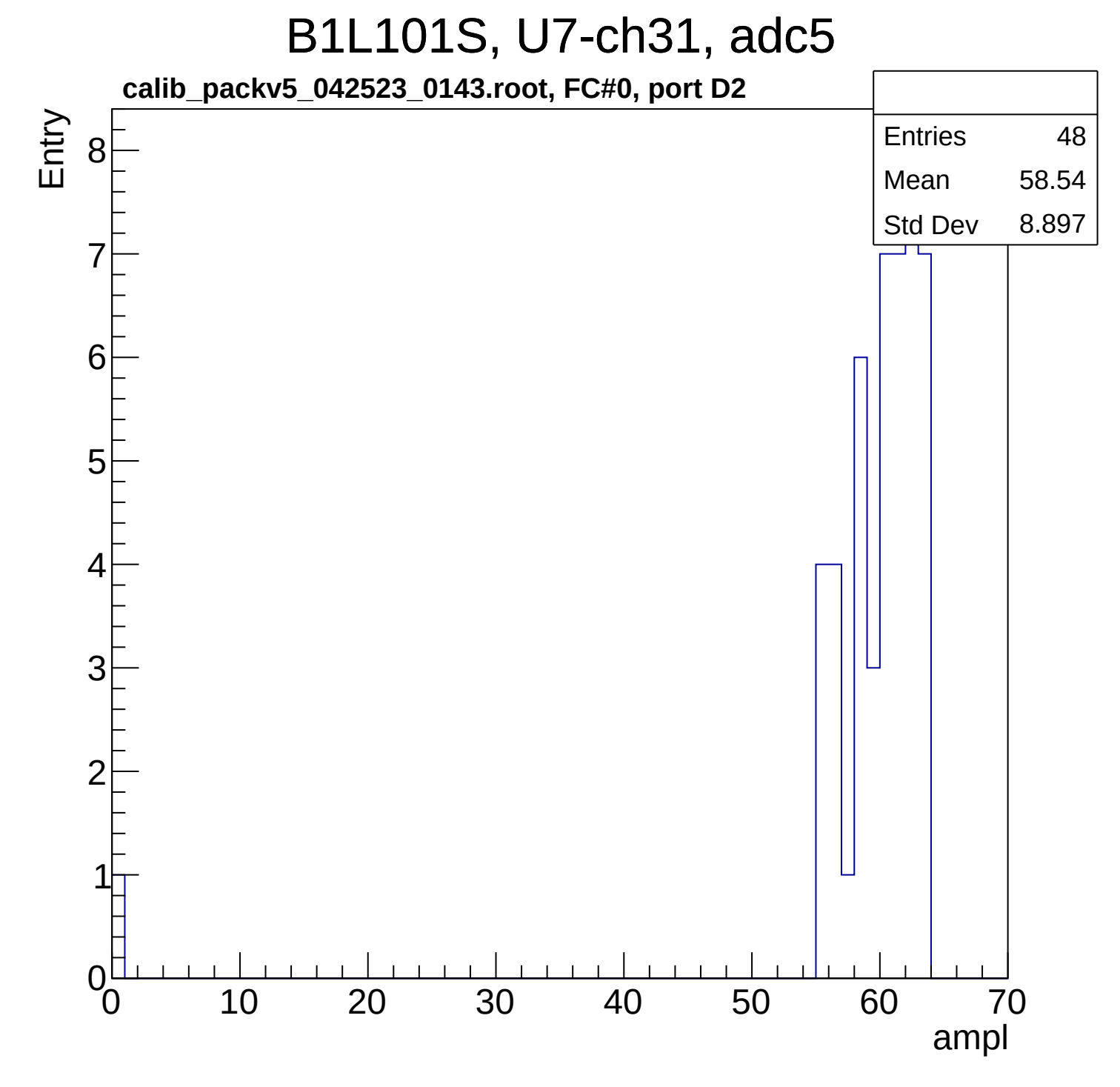
B1L101S, U7-ch31, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 58.54
Std Dev 8.897
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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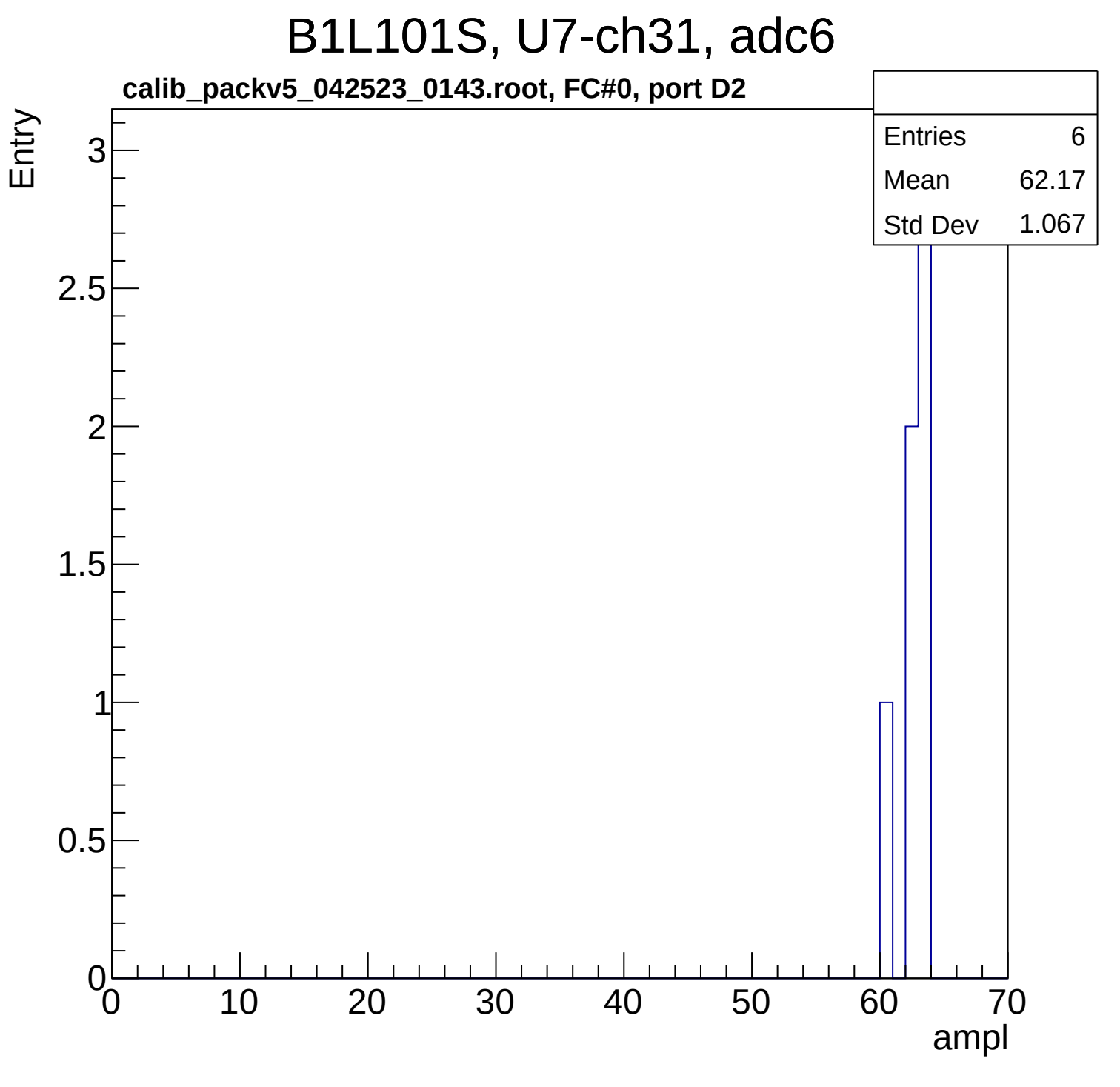
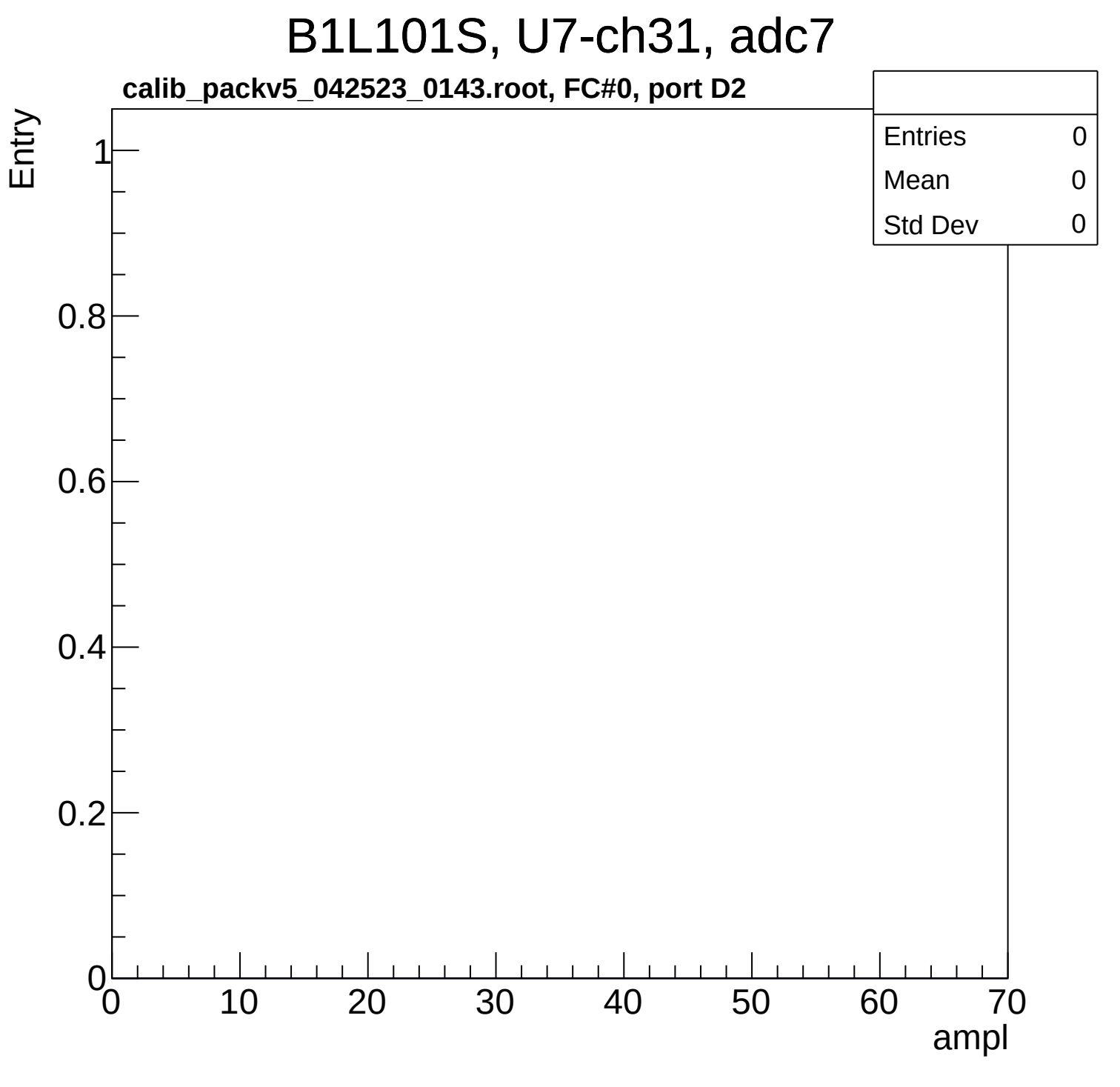
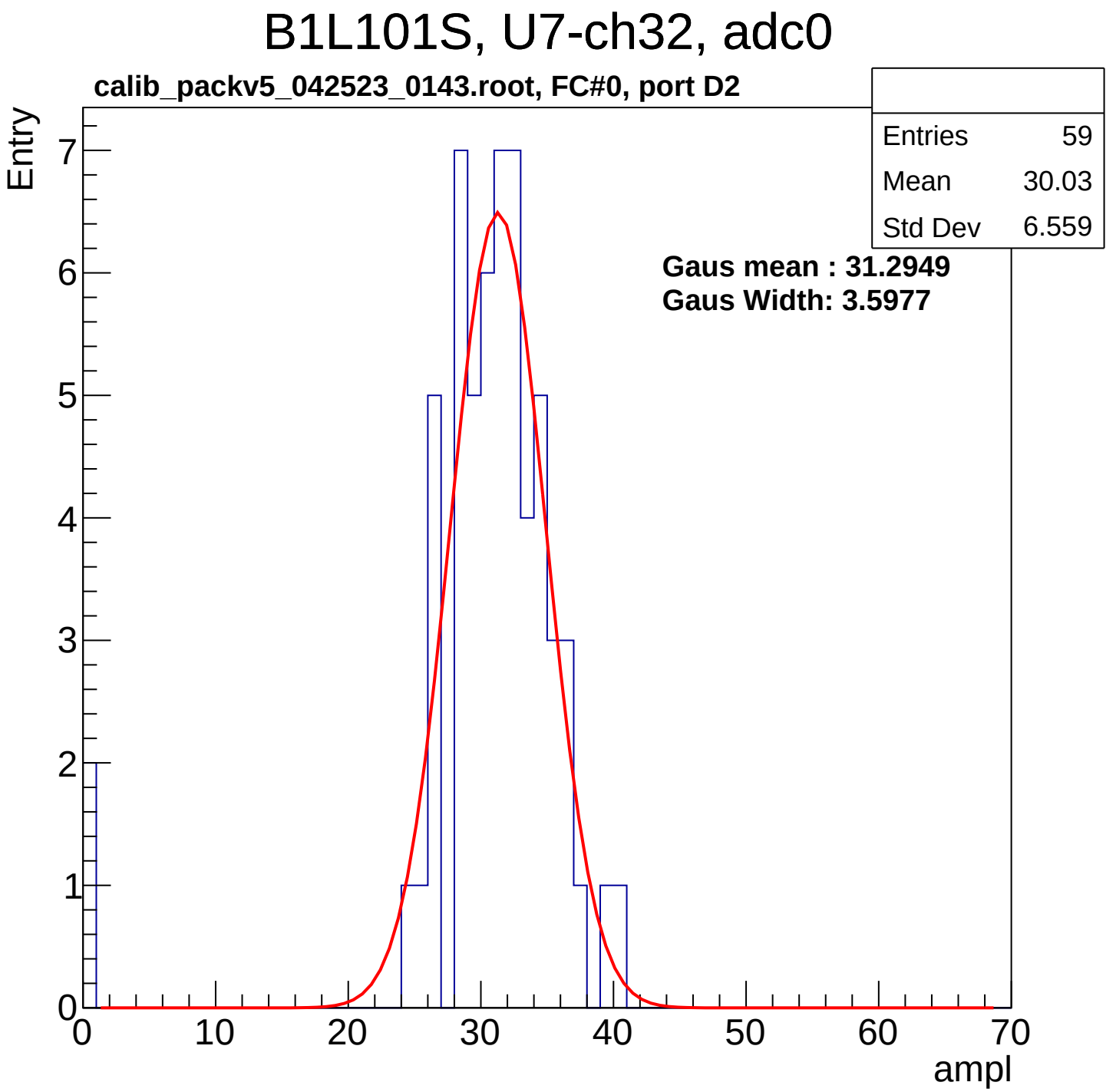
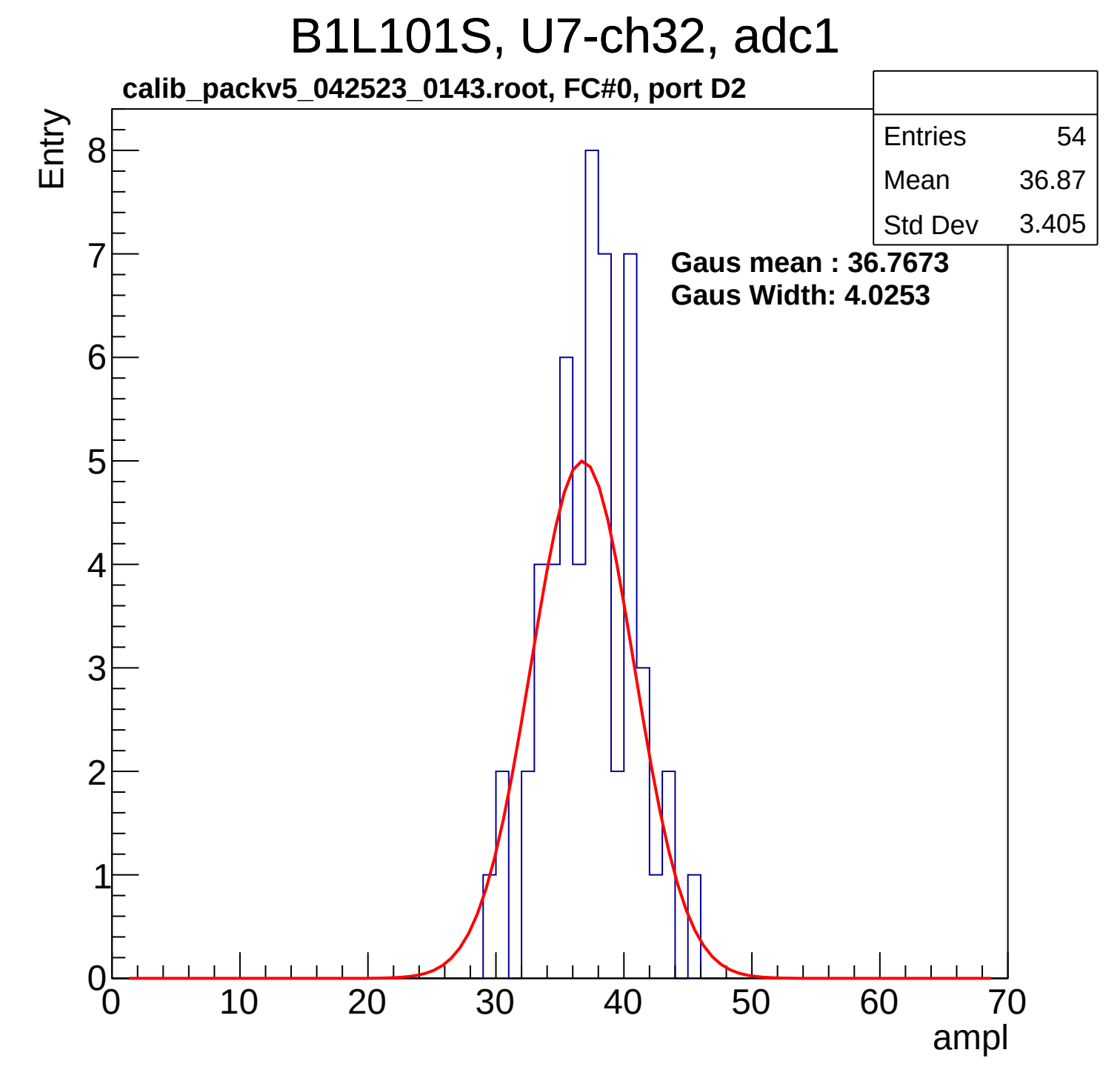

B1L101S, U7-ch31, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 62.17
Std Dev 1.067
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U7-ch31, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch32, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 30.03
Std Dev 6.559
Gaus mean : 31.2949
Gaus Width: 3.5977
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U7-ch32, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 36.87
Std Dev 3.405
Gaus mean : 36.7673
Gaus Width: 4.0253
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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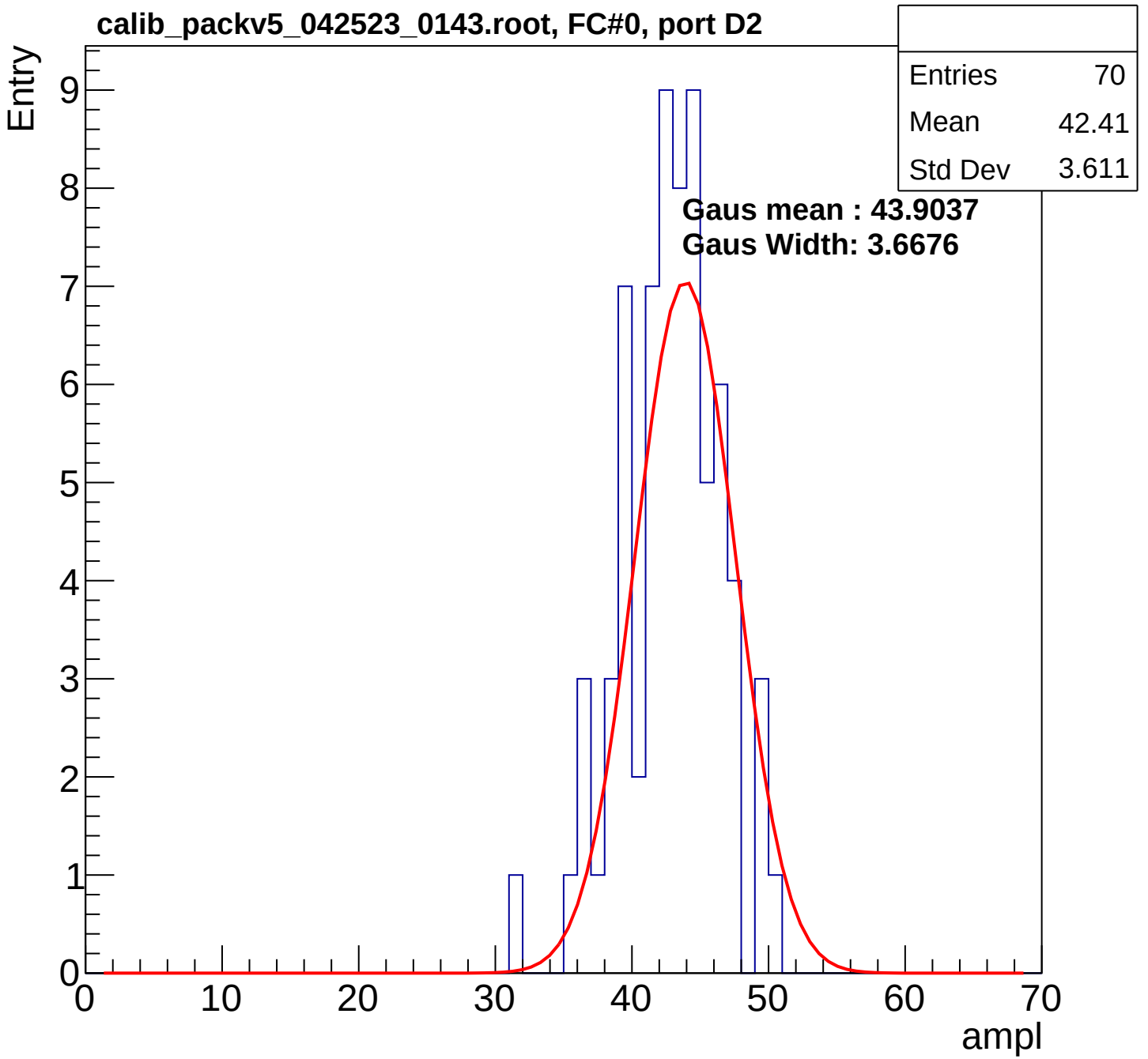
B1L101S, U7-ch32, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 42.41
Std Dev 3.611
Gaus mean : 43.9037
Gaus Width: 3.6676
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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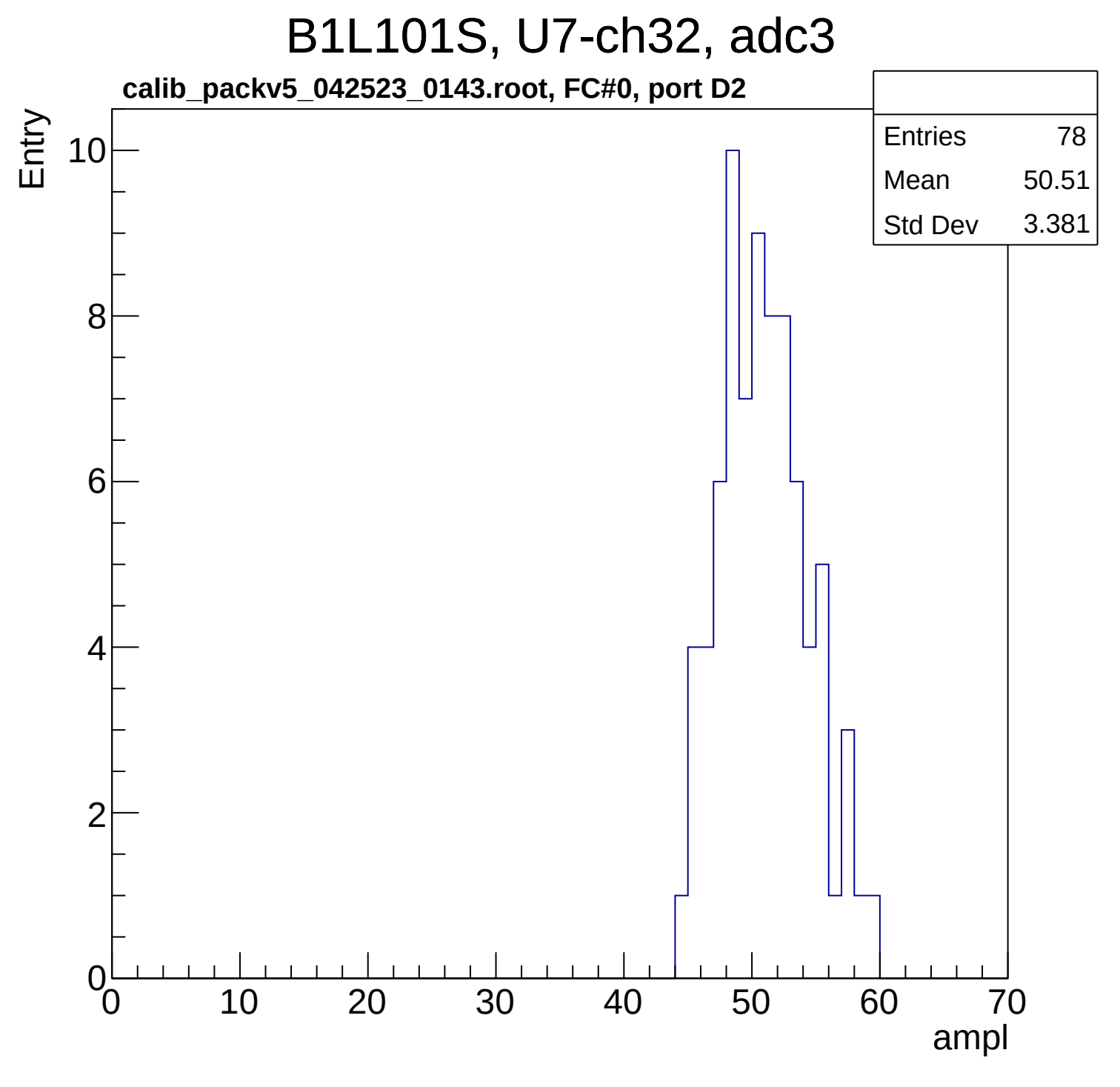
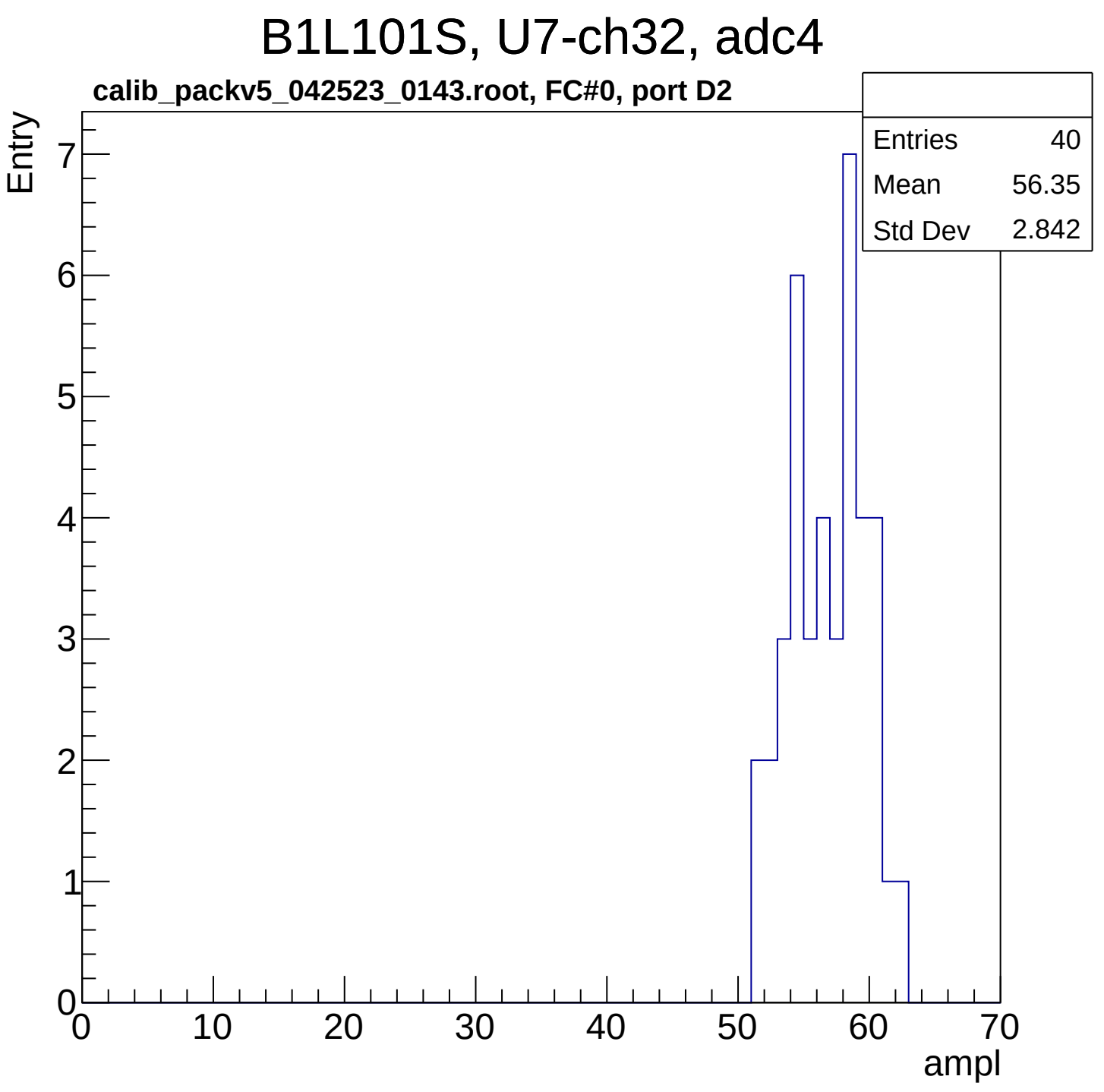
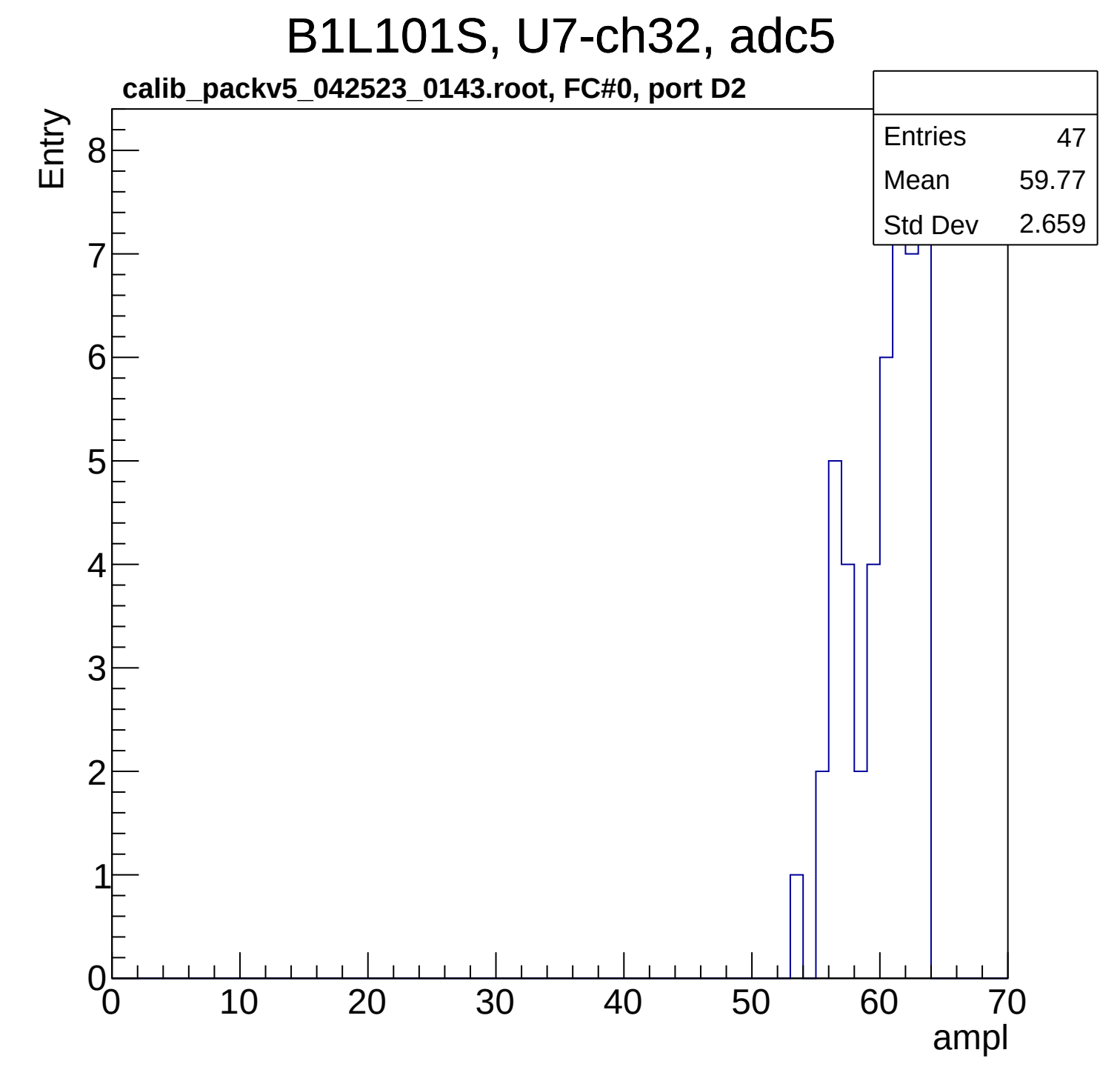
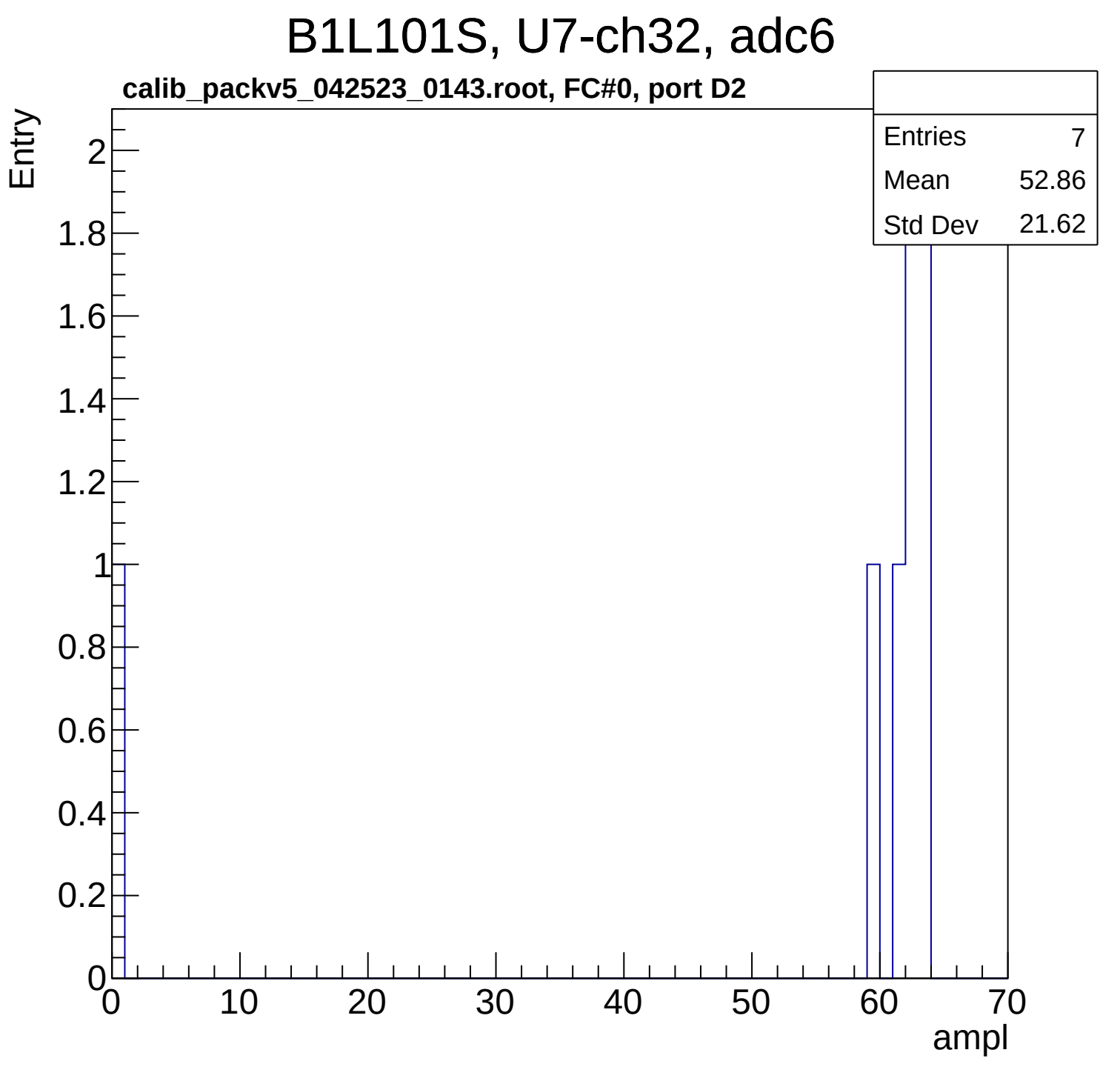
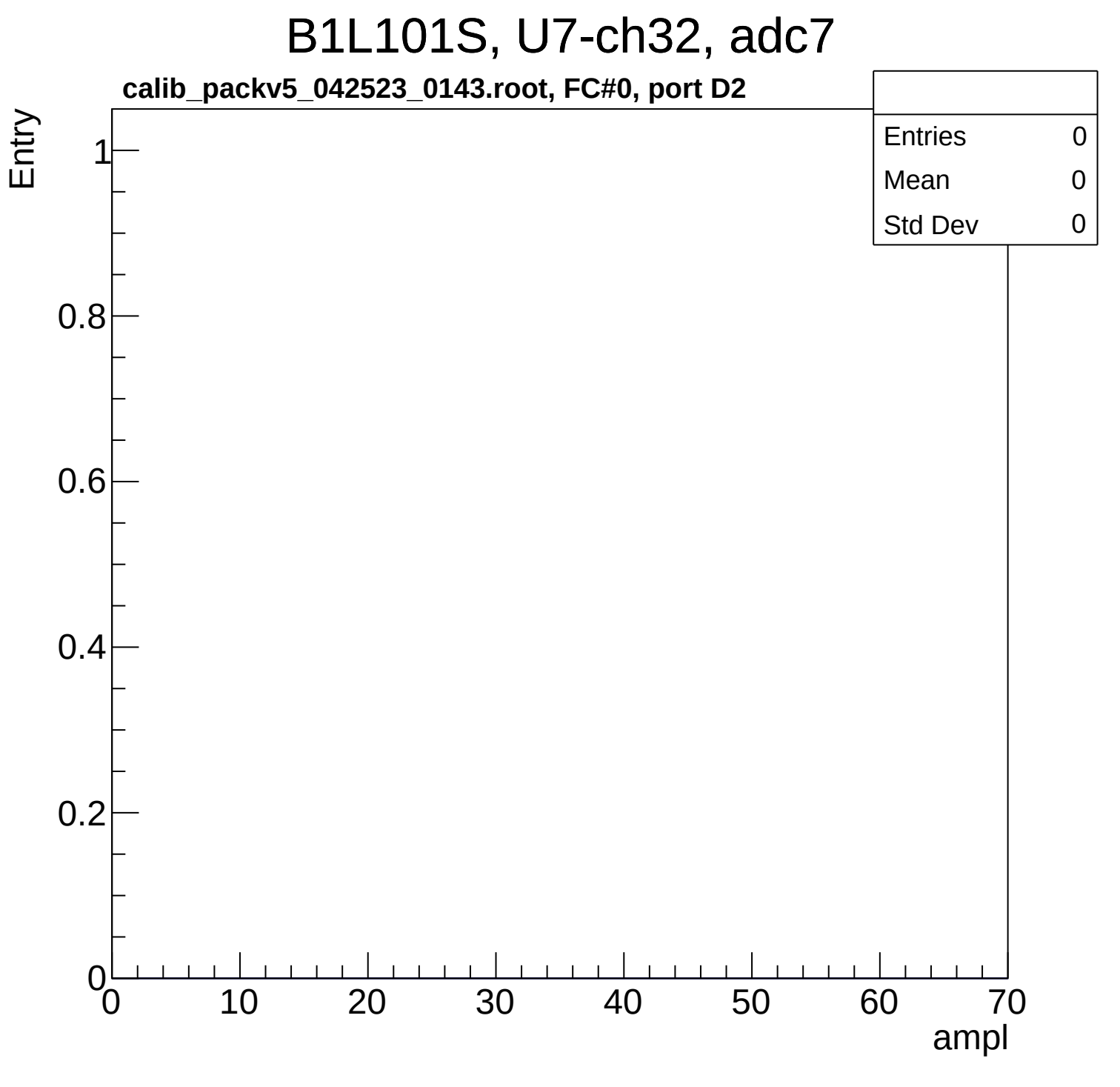
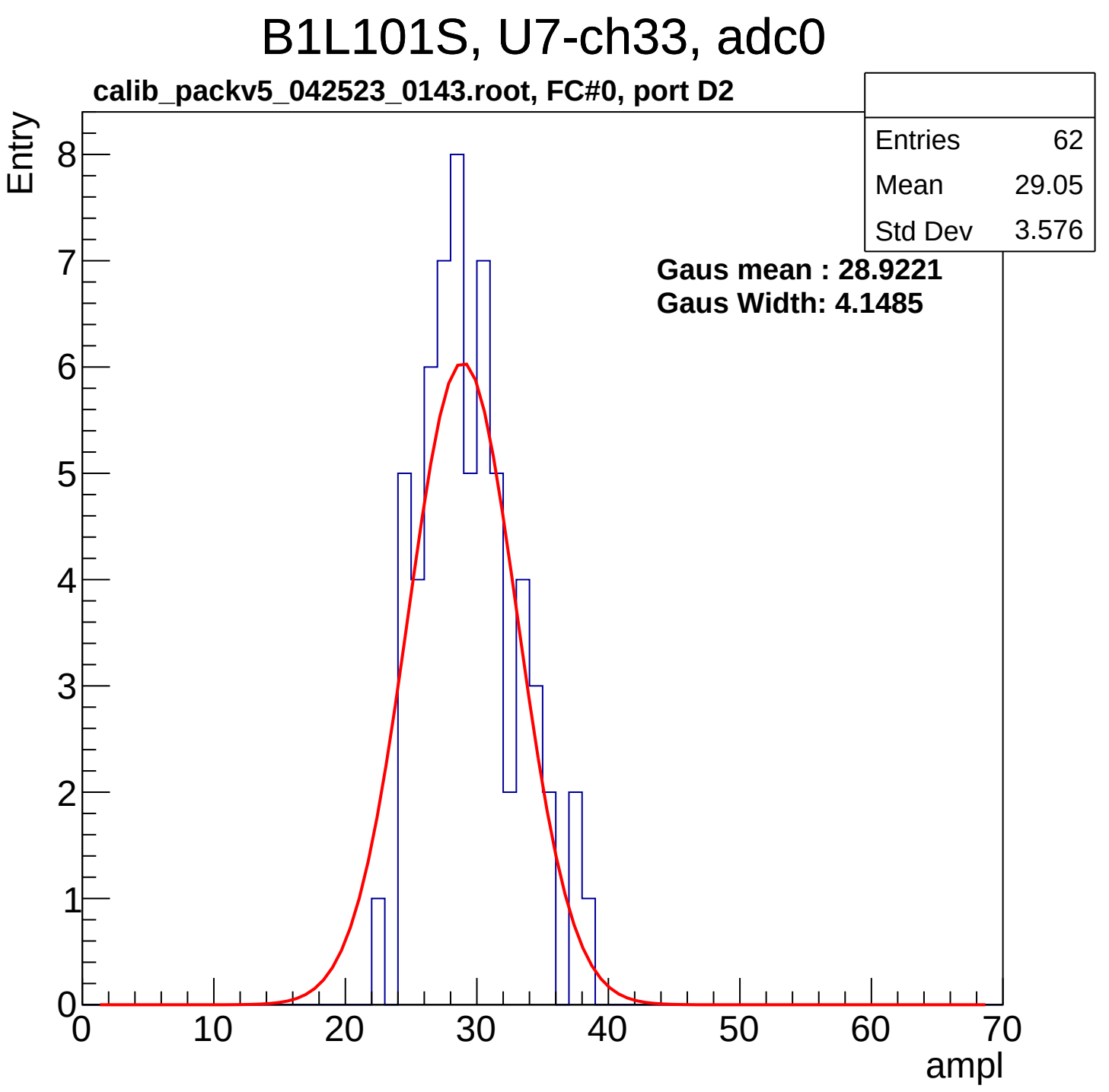

B1L101S, U7-ch32, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 50.51
Std Dev 3.381
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

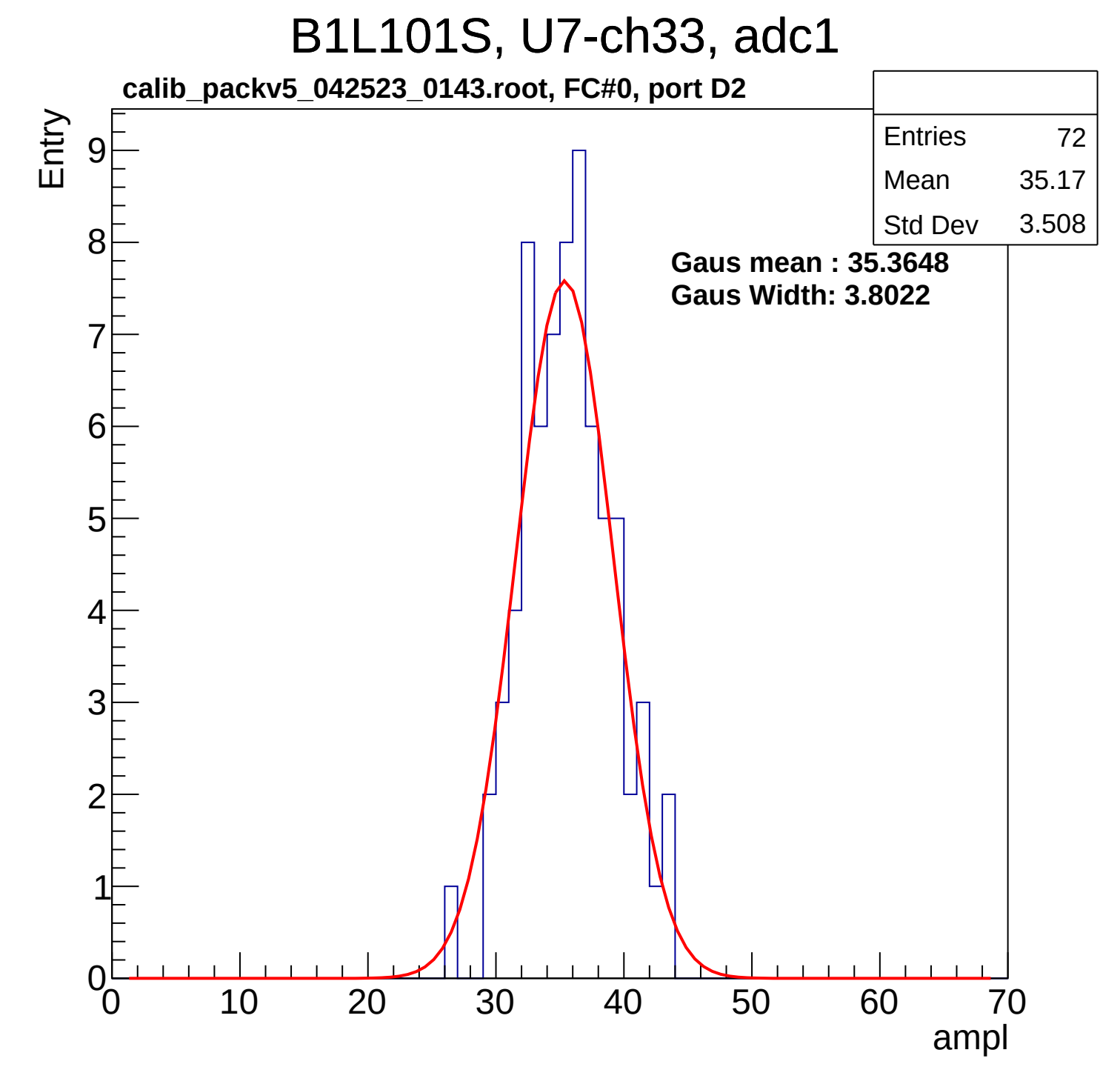

B1L101S, U7-ch32, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 40
Mean 56.35
Std Dev 2.842
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

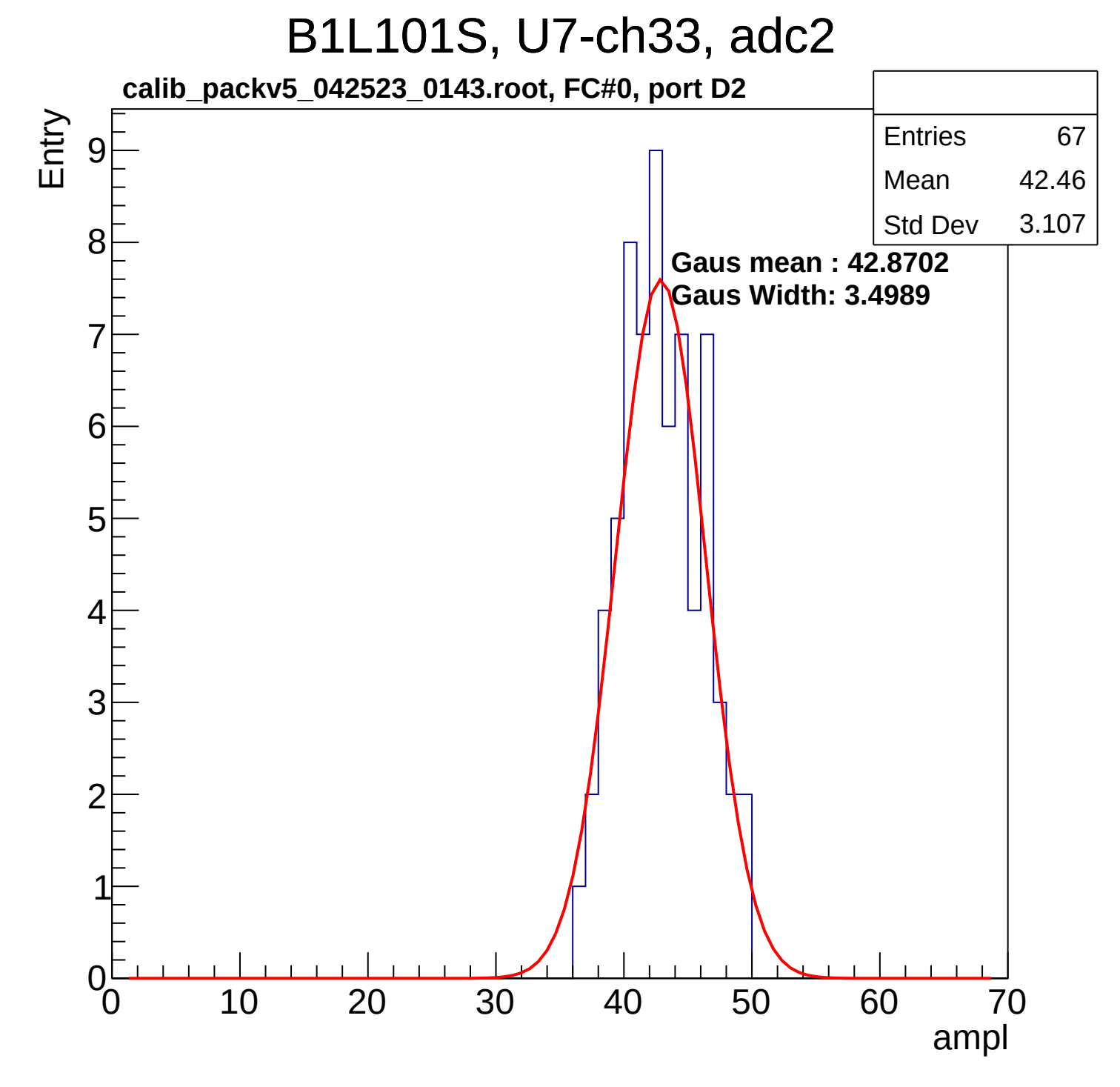

B1L101S, U7-ch32, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 59.77
Std Dev 2.659
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch32, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 52.86
Std Dev 21.62
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U7-ch32, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch33, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 29.05
Std Dev 3.576
Gaus mean : 28.9221
Gaus Width: 4.1485
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch33, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 35.17
Std Dev 3.508
Gaus mean : 35.3648
Gaus Width: 3.8022
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch33, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 42.46
Std Dev 3.107
Gaus mean : 42.8702
Gaus Width: 3.4989
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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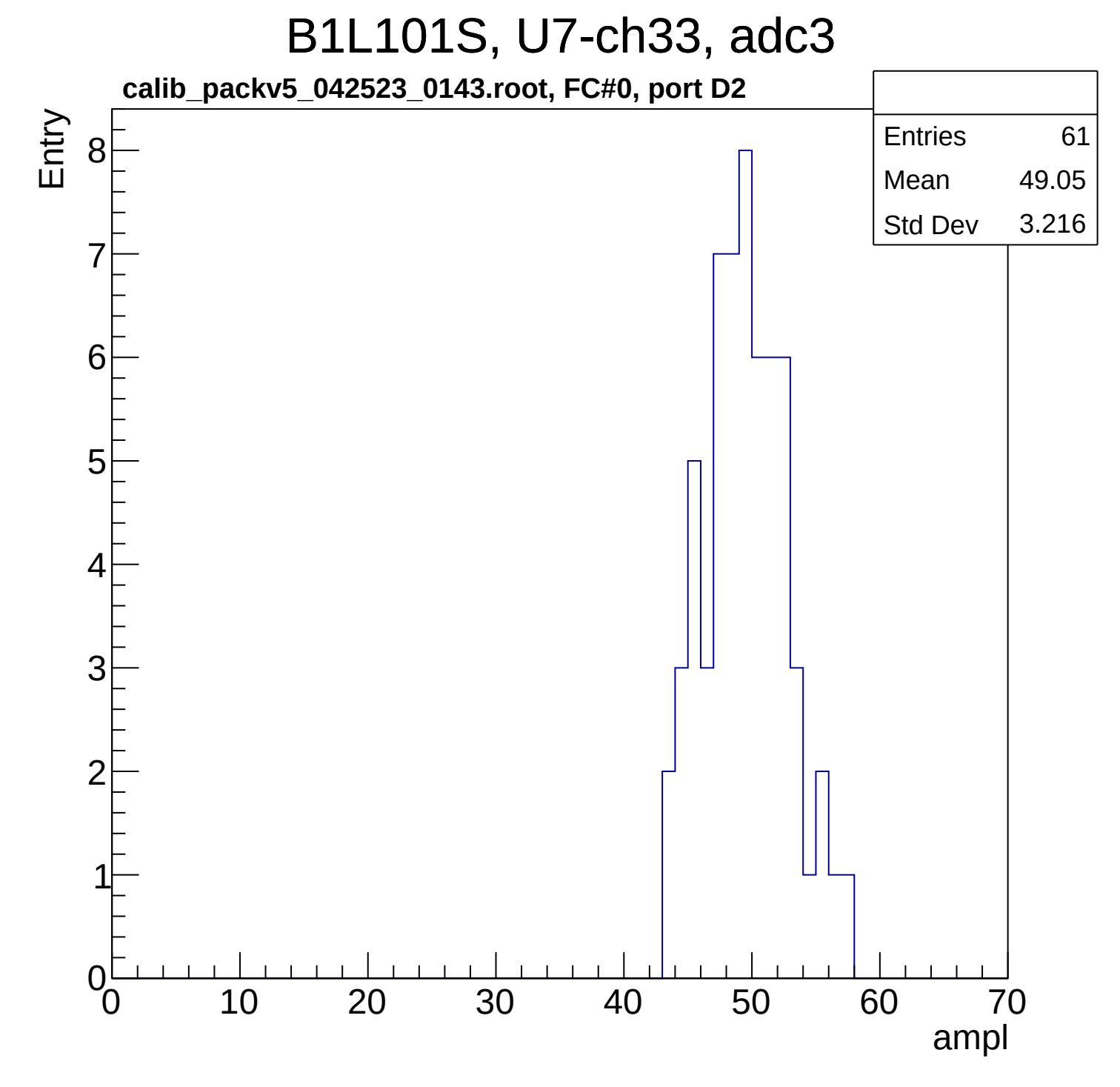
40
50
60
70


B1L101S, U7-ch33, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 49.05
Std Dev 3.216
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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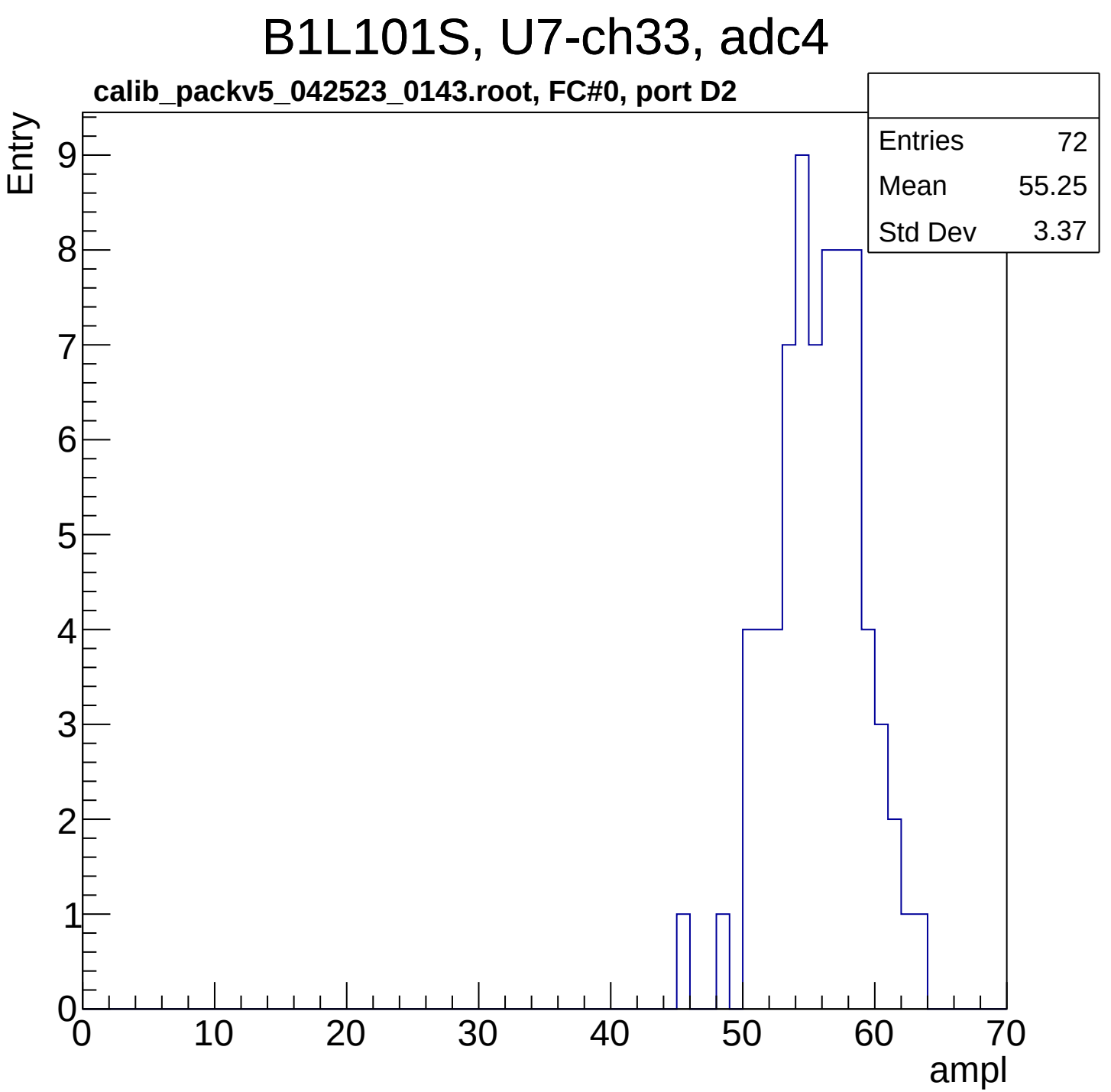
40
50
60
70


B1L101S, U7-ch33, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 55.25
Std Dev 3.37
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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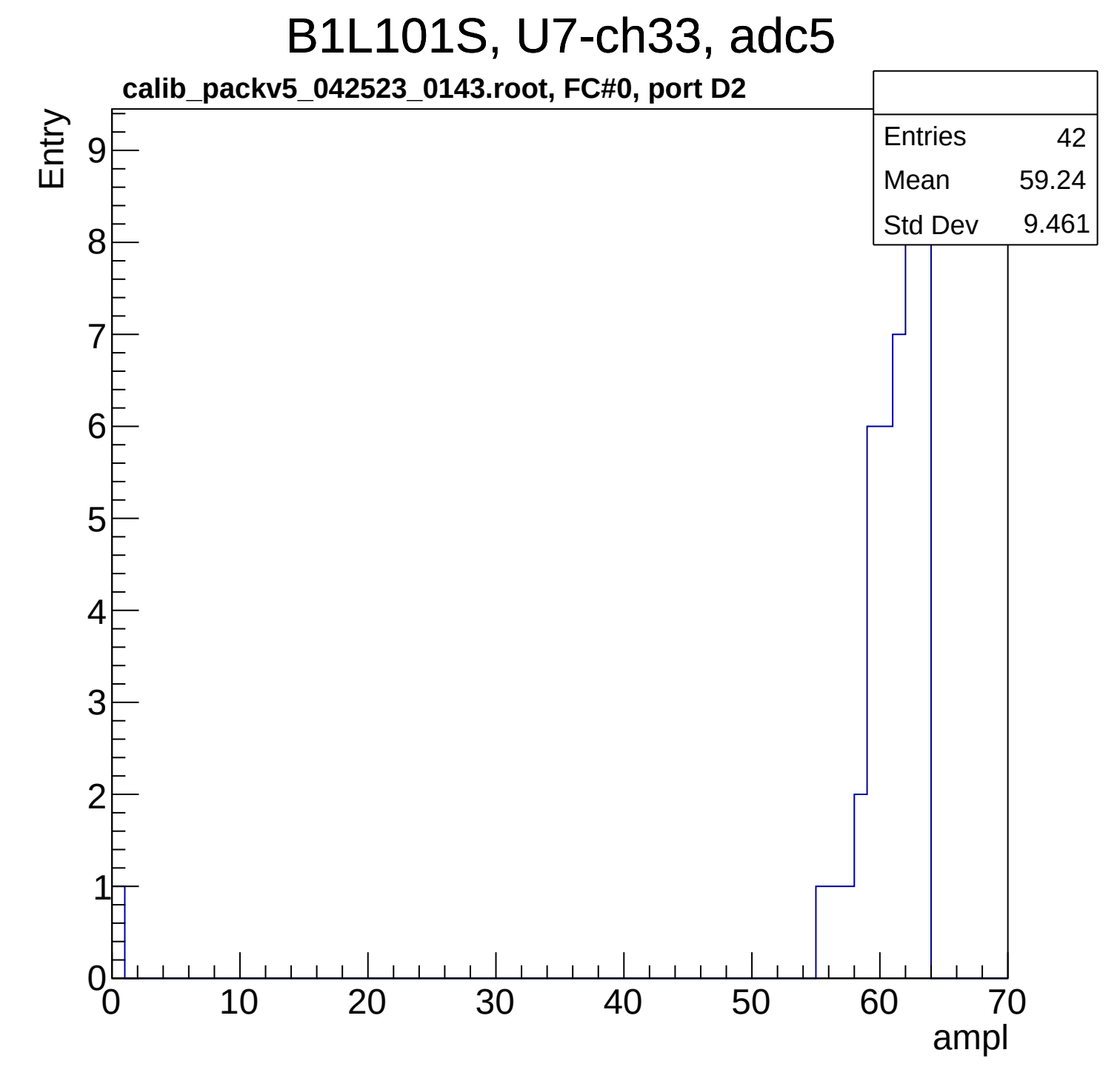
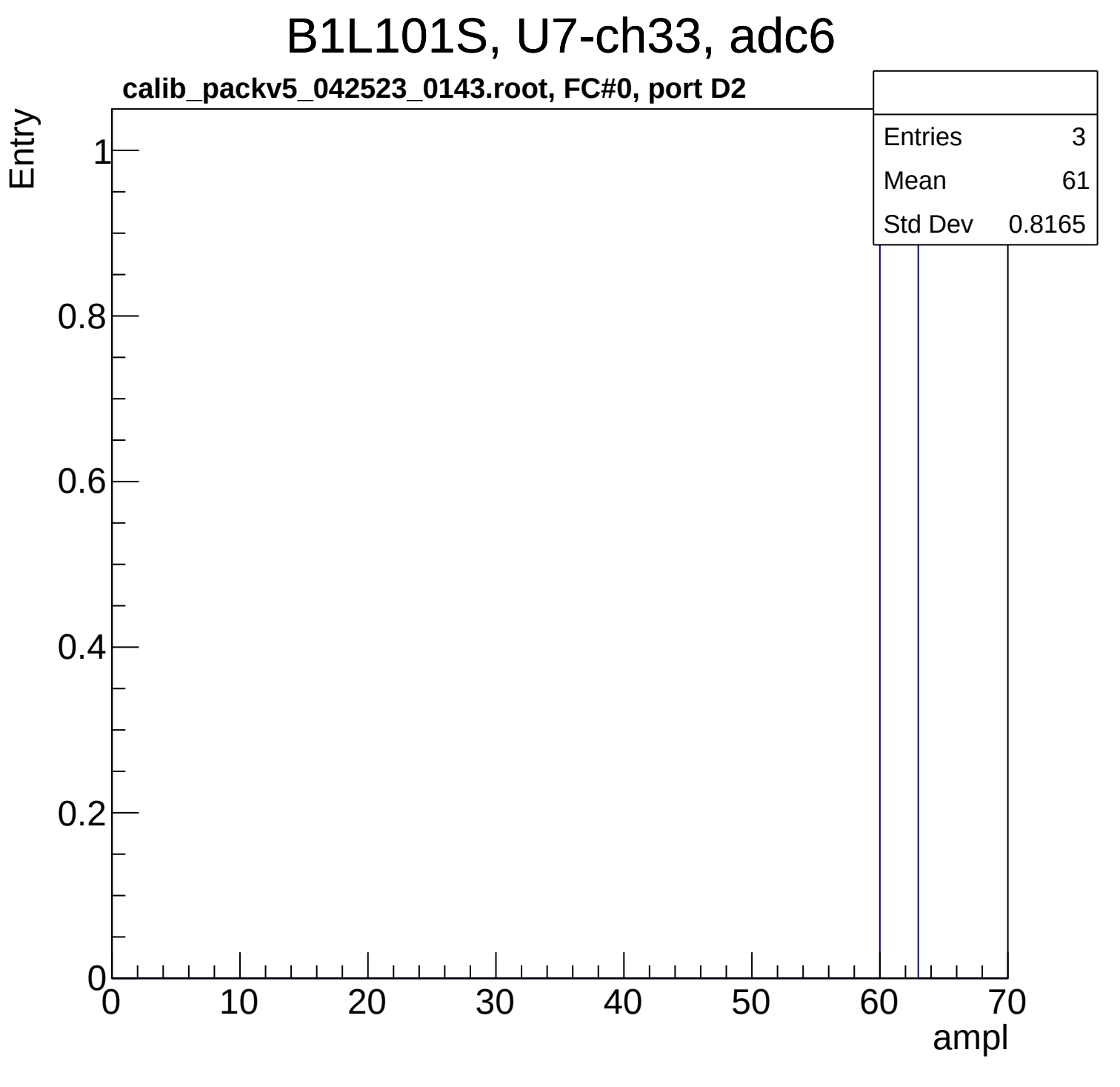

B1L101S, U7-ch33, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 59.24
Std Dev 9.461
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch33, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 61
Std Dev 0.8165
Entry
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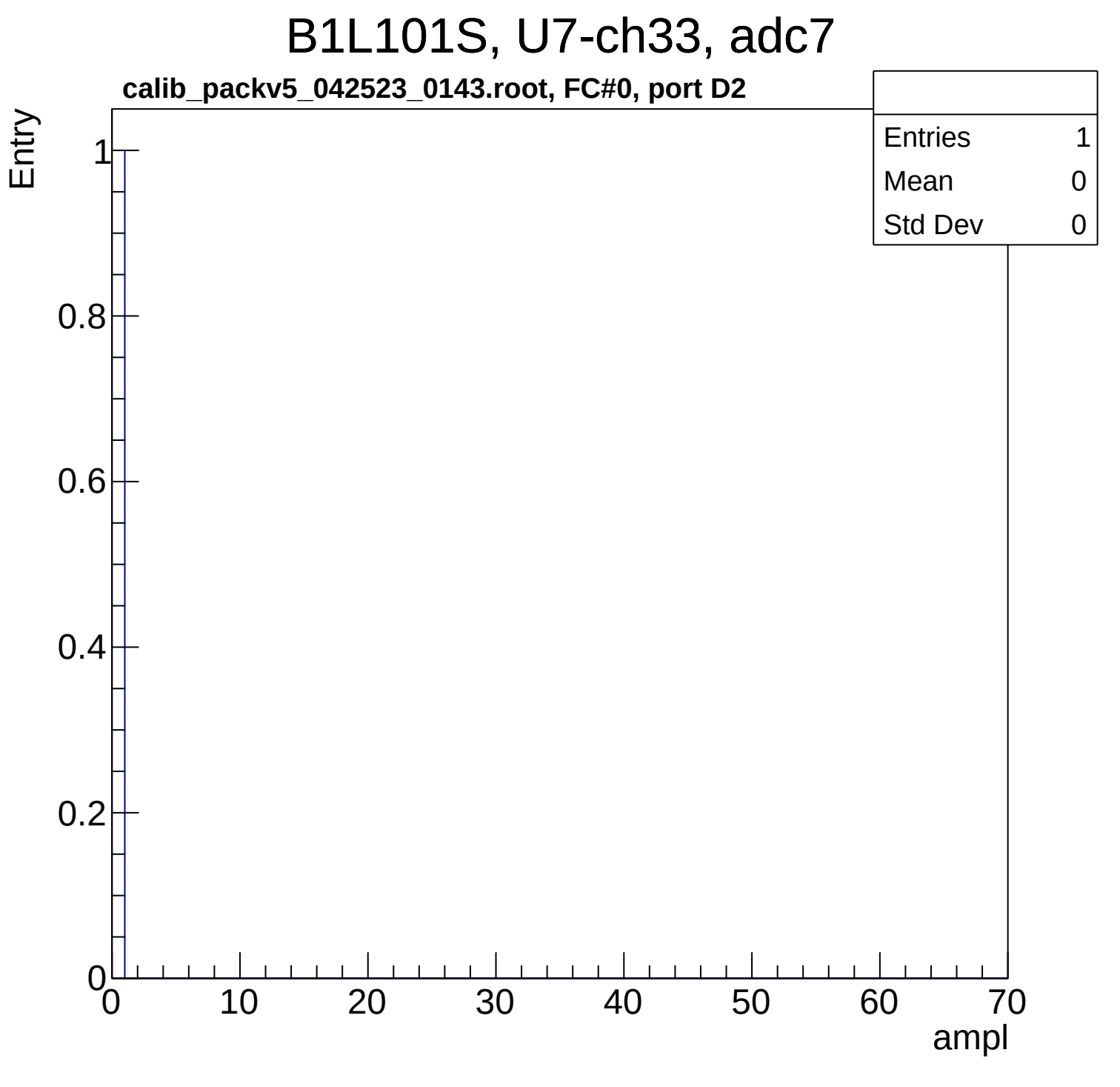
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch33, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
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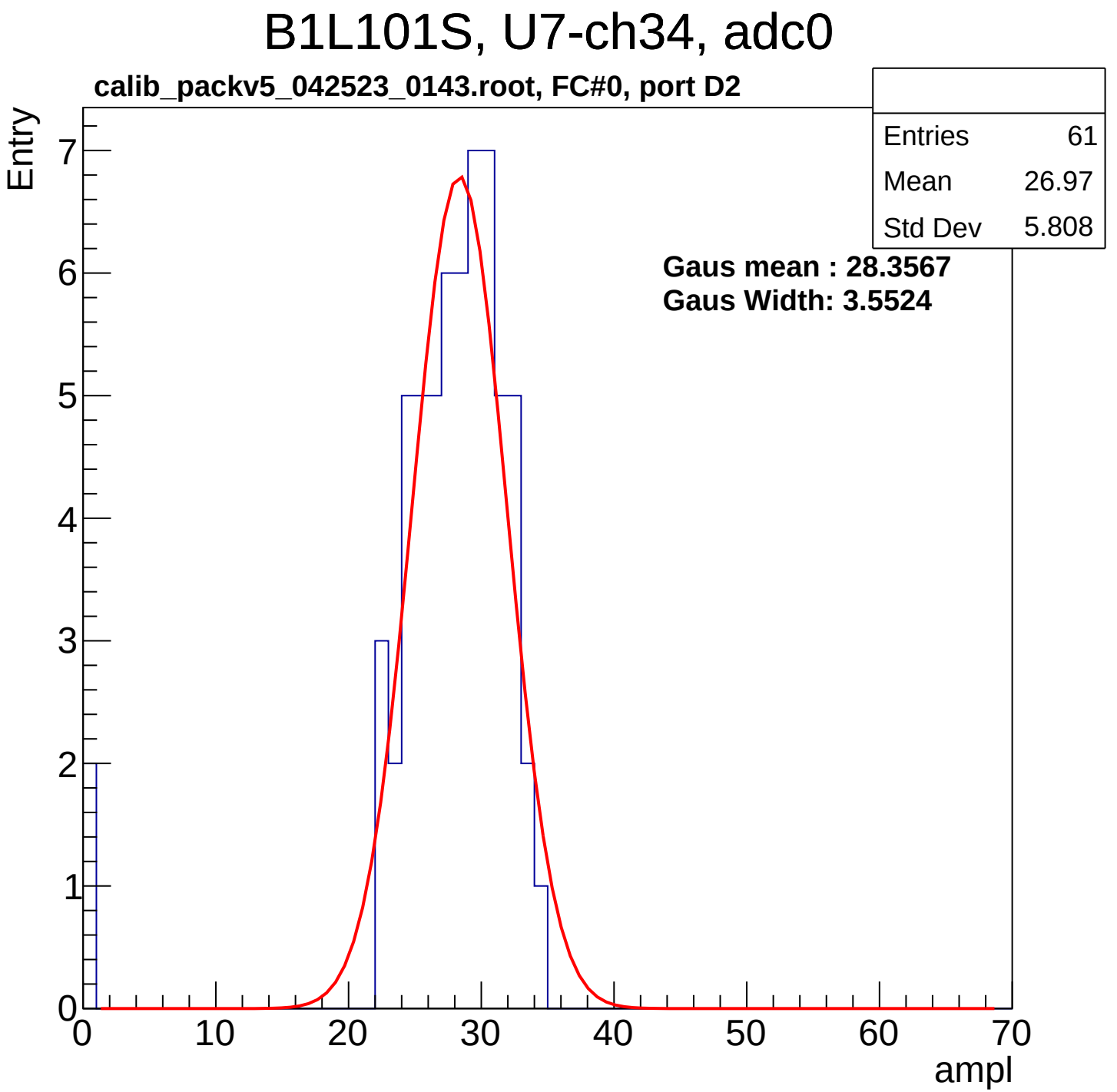
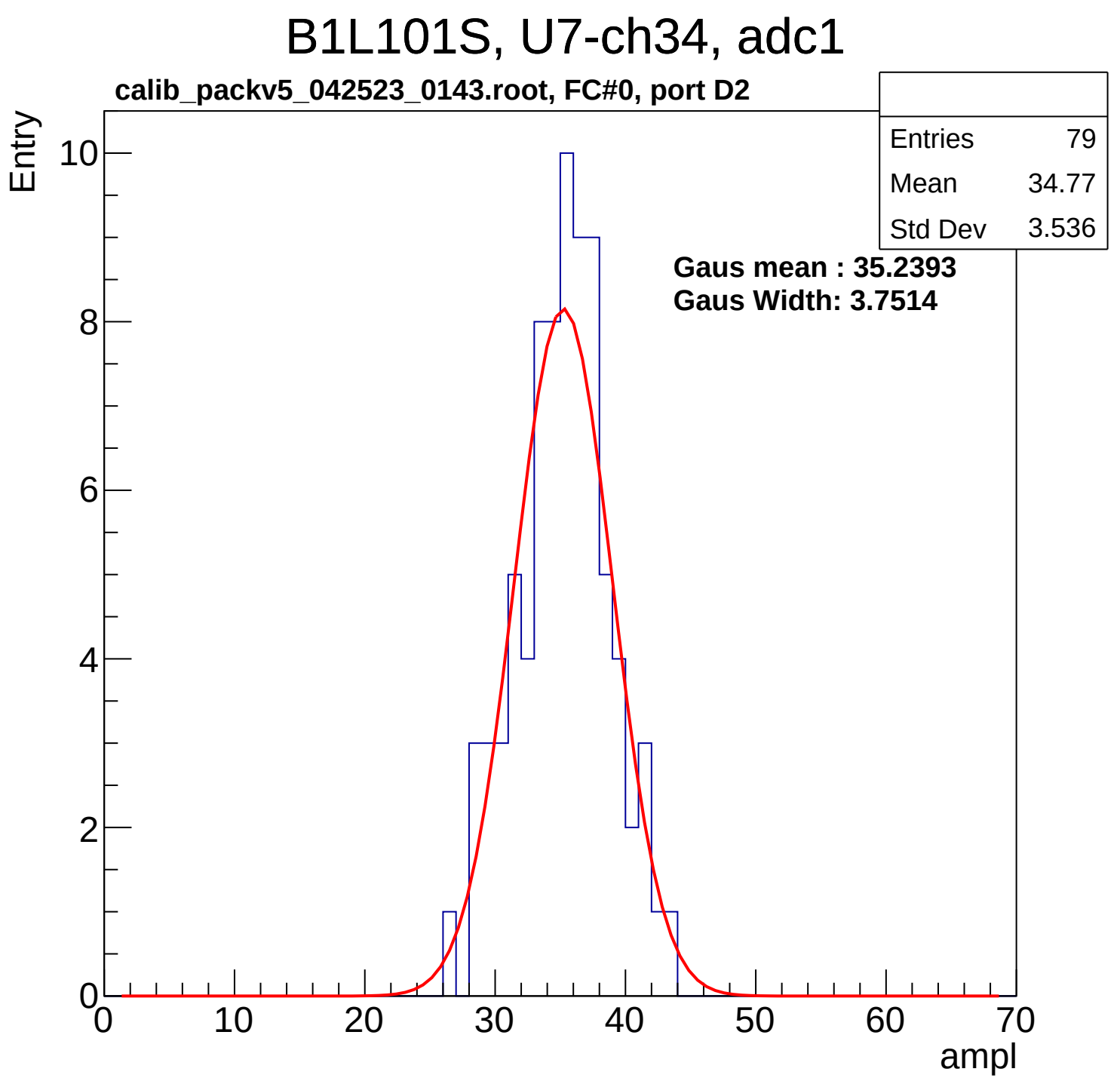
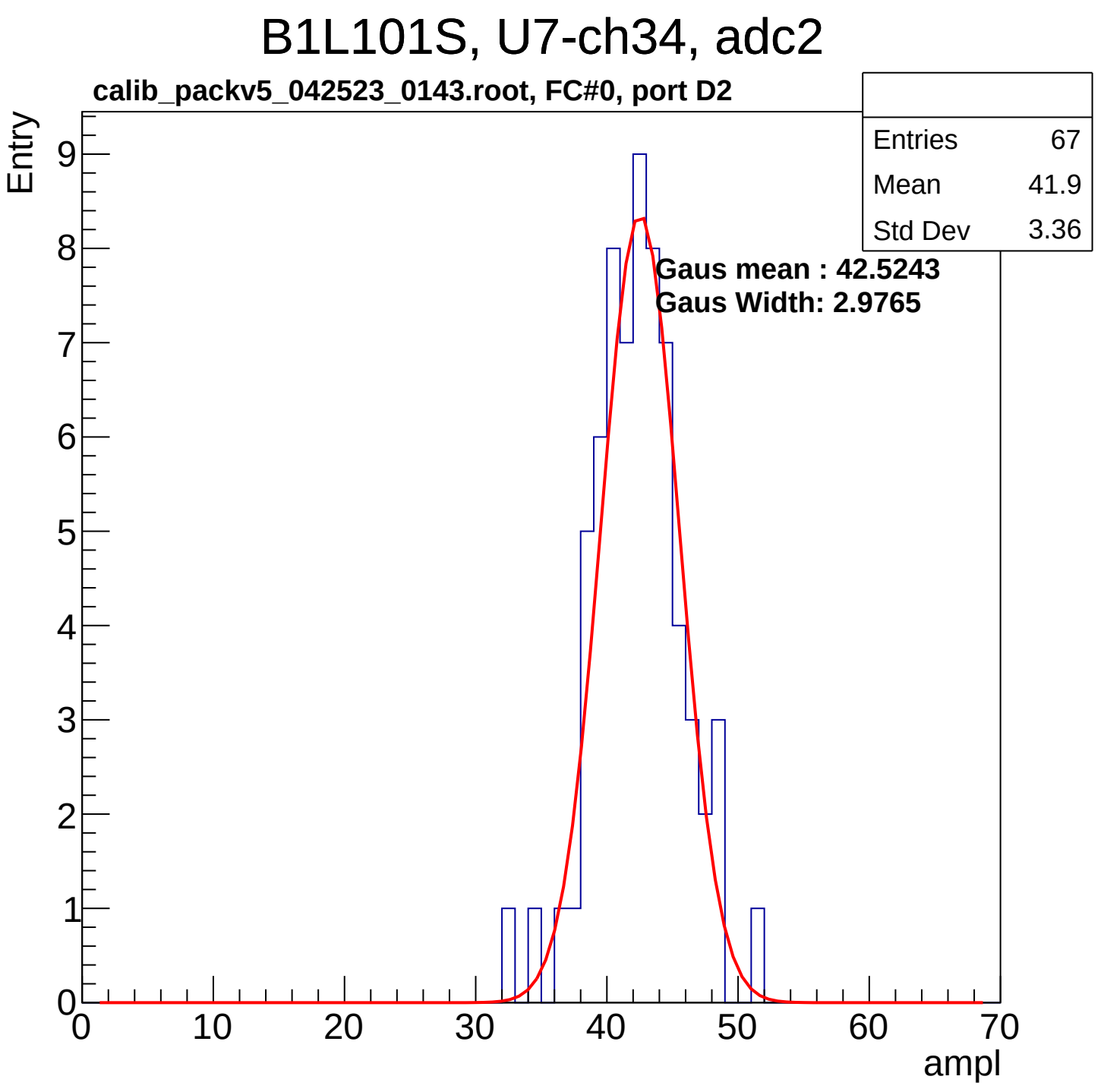
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch34, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 26.97
Std Dev 5.808
Gaus mean : 28.3567
Gaus Width: 3.5524
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U7-ch34, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 34.77
Std Dev 3.536
Gaus mean : 35.2393
Gaus Width: 3.7514
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch34, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 41.9
Std Dev 3.36
Gaus mean : 42.5243
Gaus Width: 2.9765
Entry
ampl
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3
4
5
6
7
8
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0
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60
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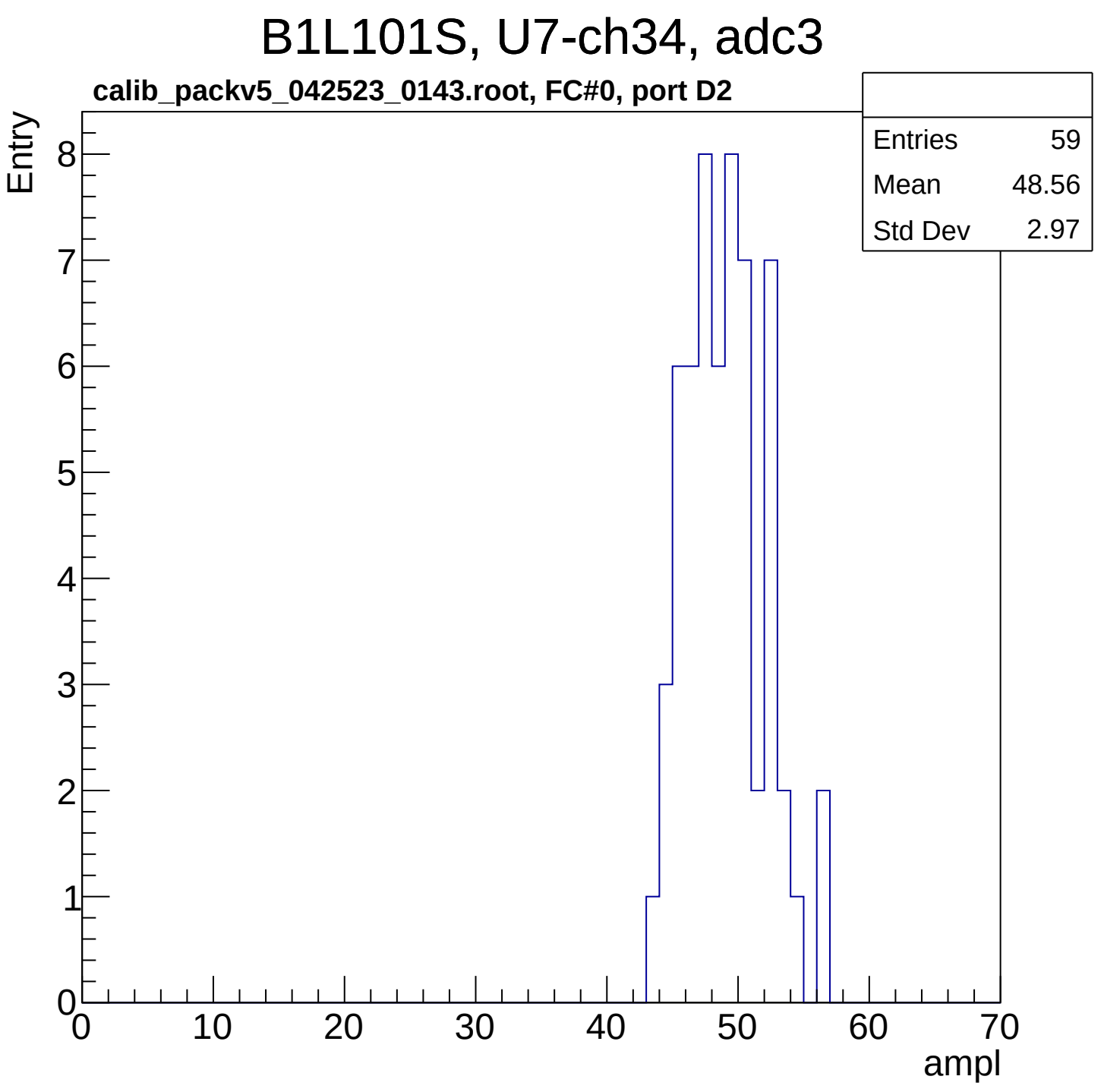
B1L101S, U7-ch34, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 48.56
Std Dev 2.97
Entry
ampl
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1
2
3
4
5
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7
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0
10
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40
50
60
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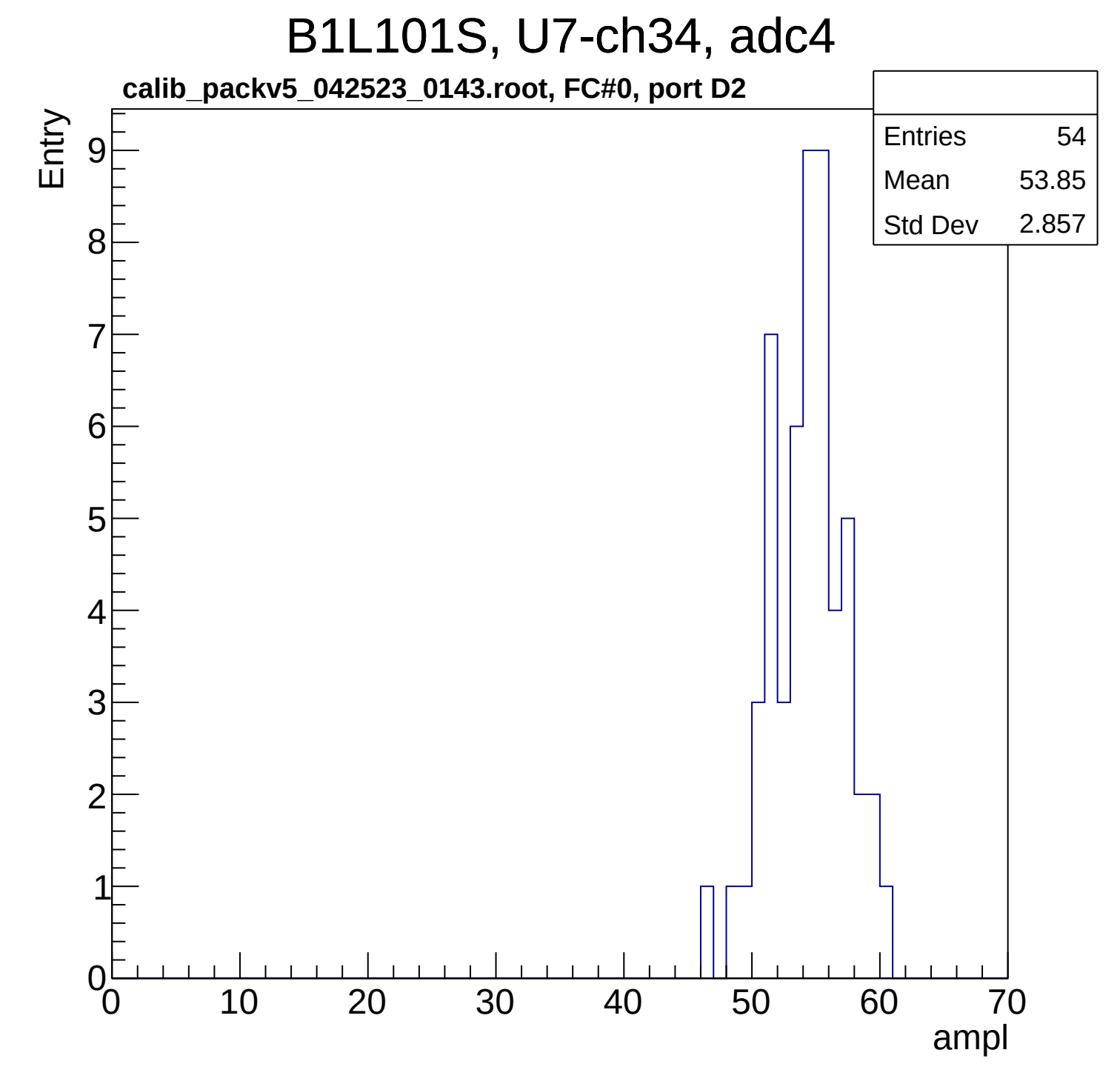
B1L101S, U7-ch34, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 53.85
Std Dev 2.857
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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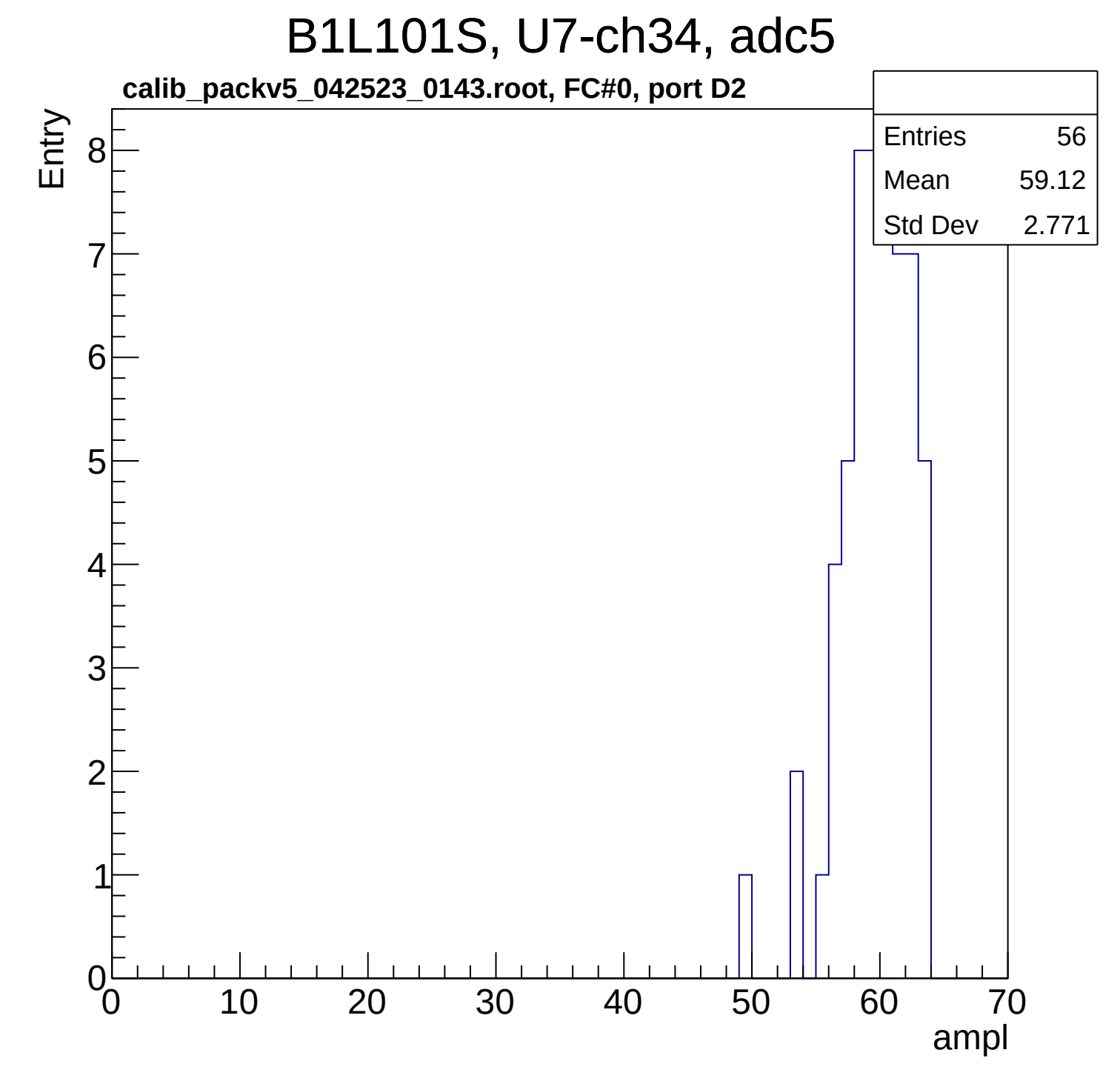
B1L101S, U7-ch34, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 59.12
Std Dev 2.771
Entry
ampl
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2
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4
5
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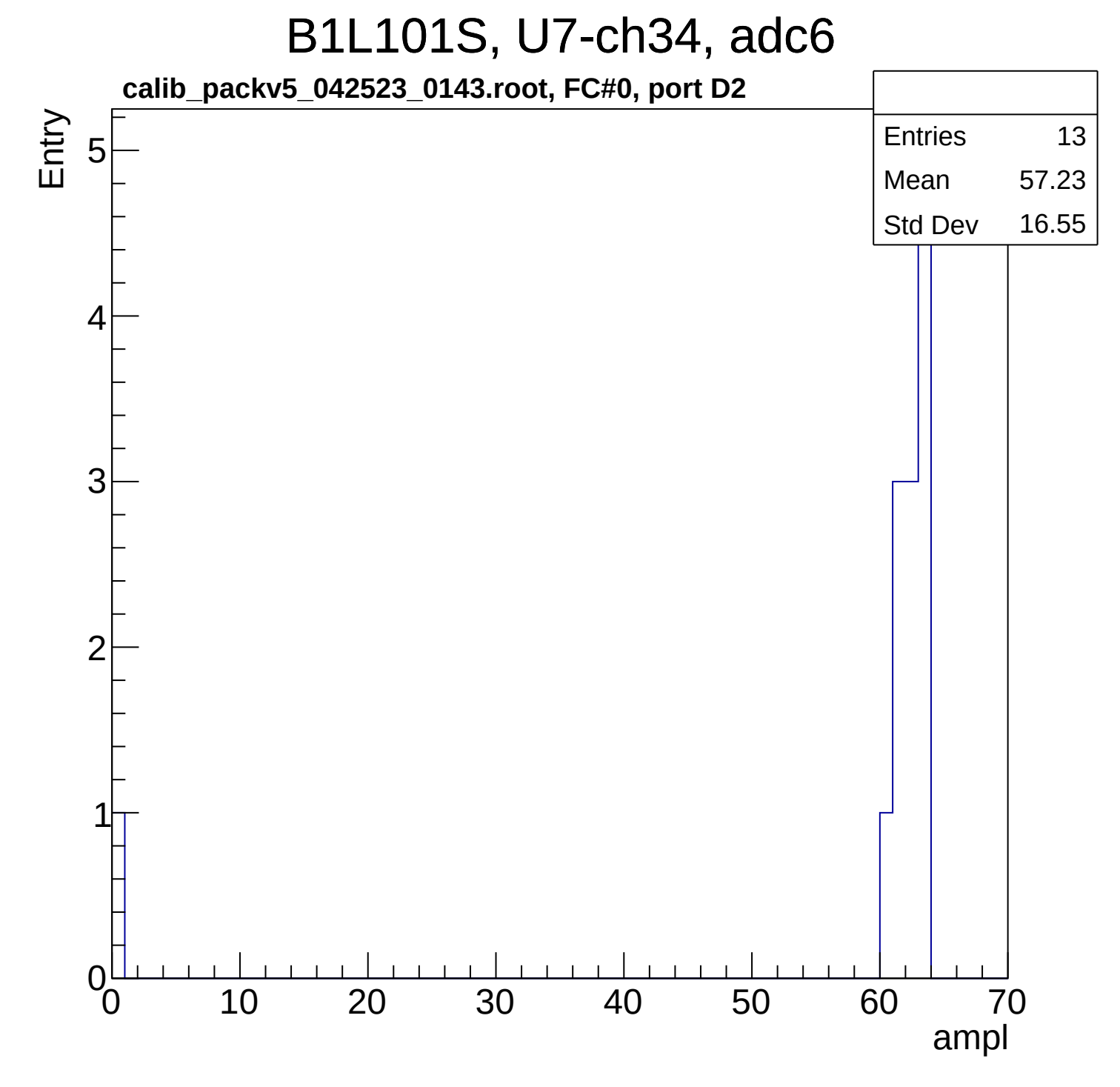
B1L101S, U7-ch34, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 13
Mean 57.23
Std Dev 16.55
Entry
0
1
2
3
4
5
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10
20
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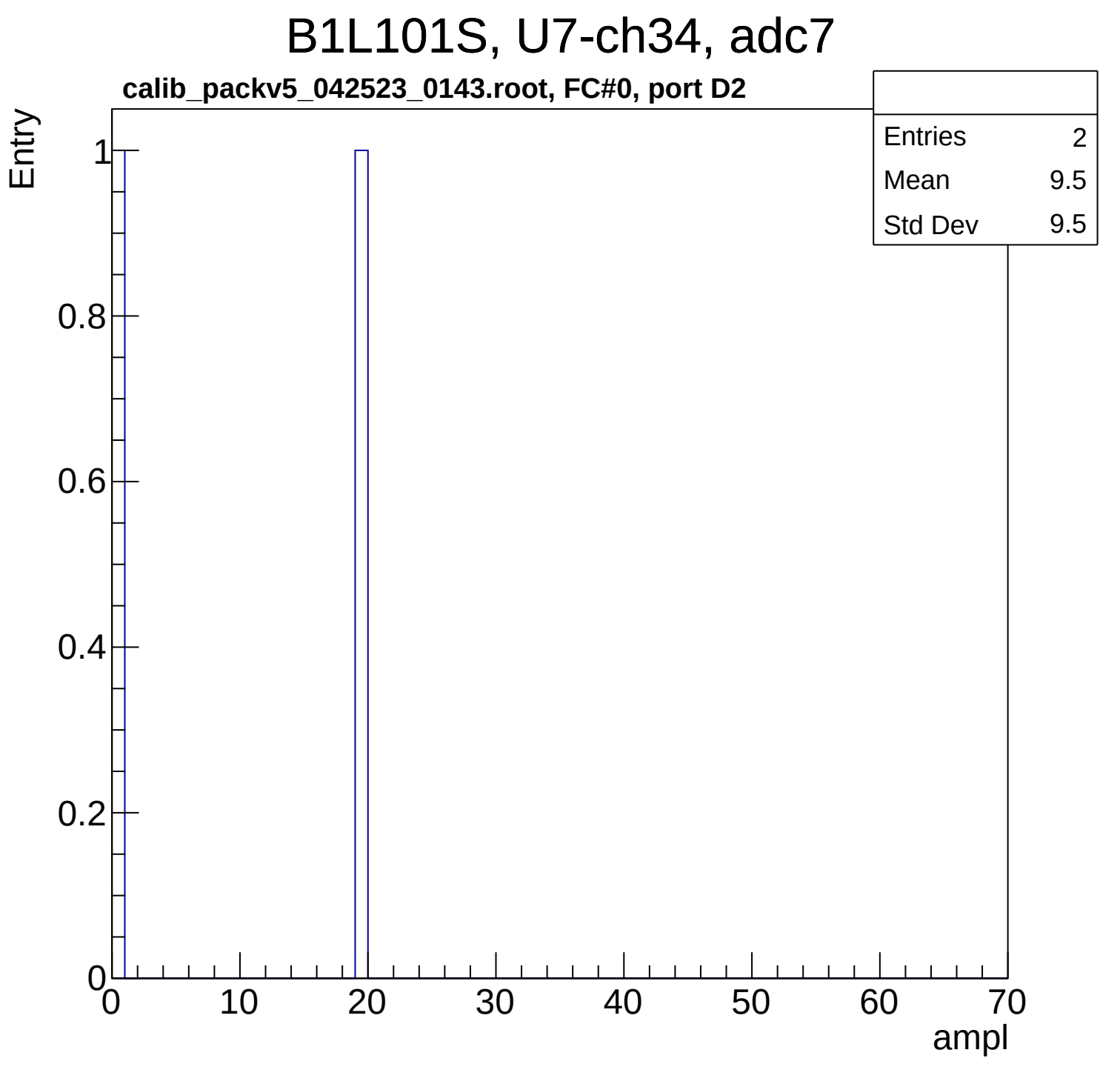
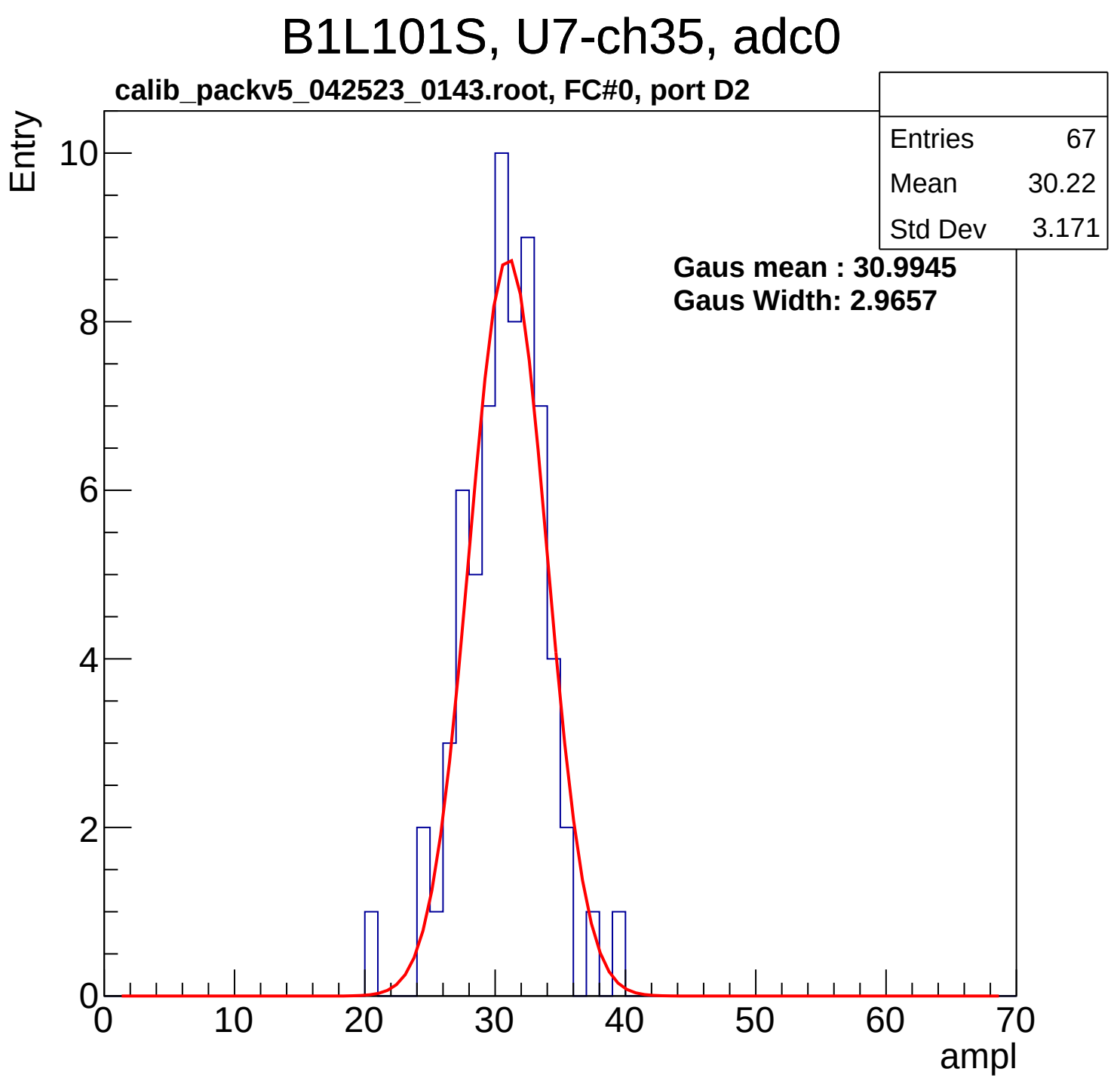
50
60
70
ampl


B1L101S, U7-ch34, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 9.5
Std Dev 9.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch35, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 30.22
Std Dev 3.171
Gaus mean : 30.9945
Gaus Width: 2.9657
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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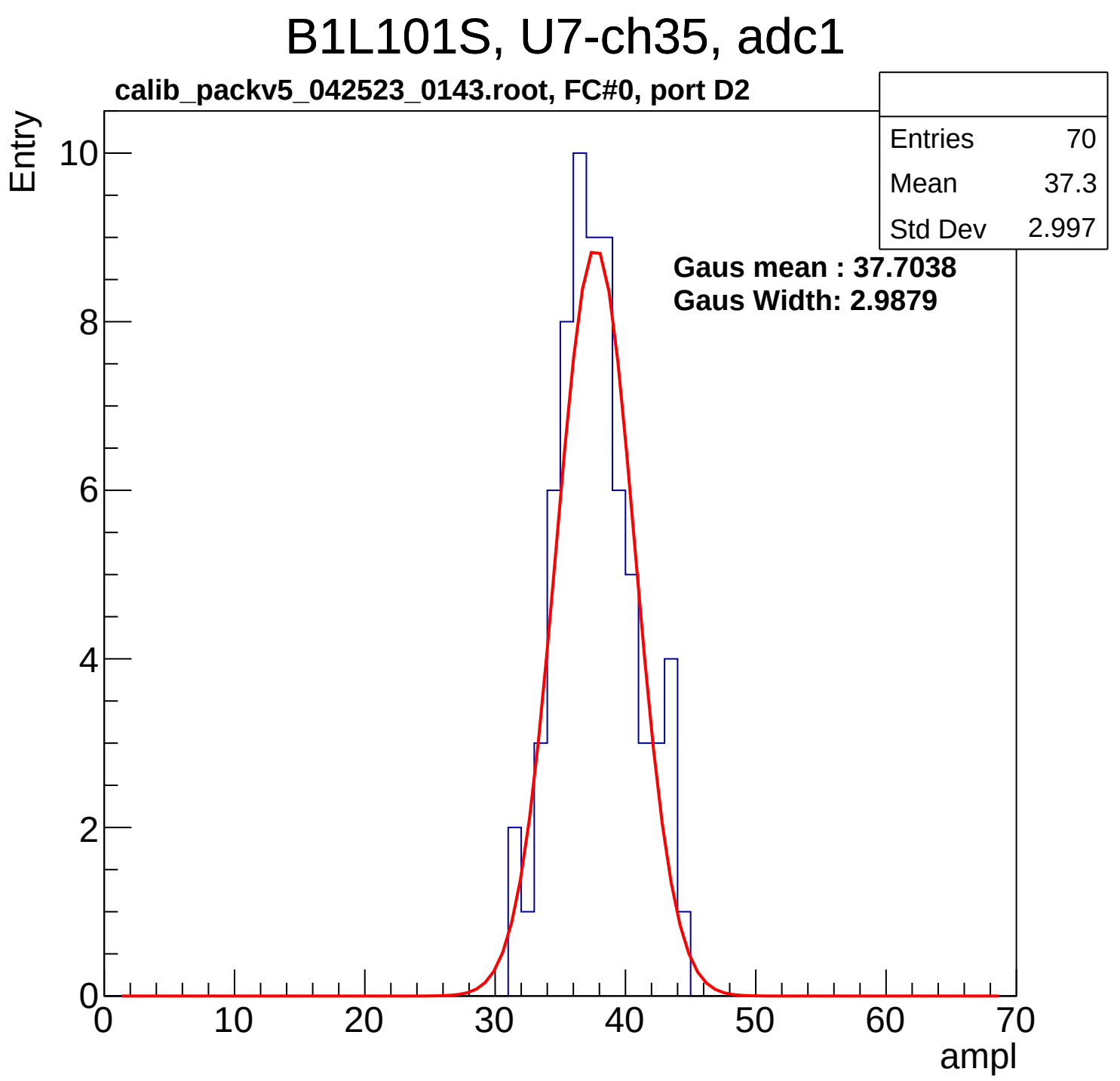
B1L101S, U7-ch35, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 37.3
Std Dev 2.997
Gaus mean : 37.7038
Gaus Width: 2.9879
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
50
60
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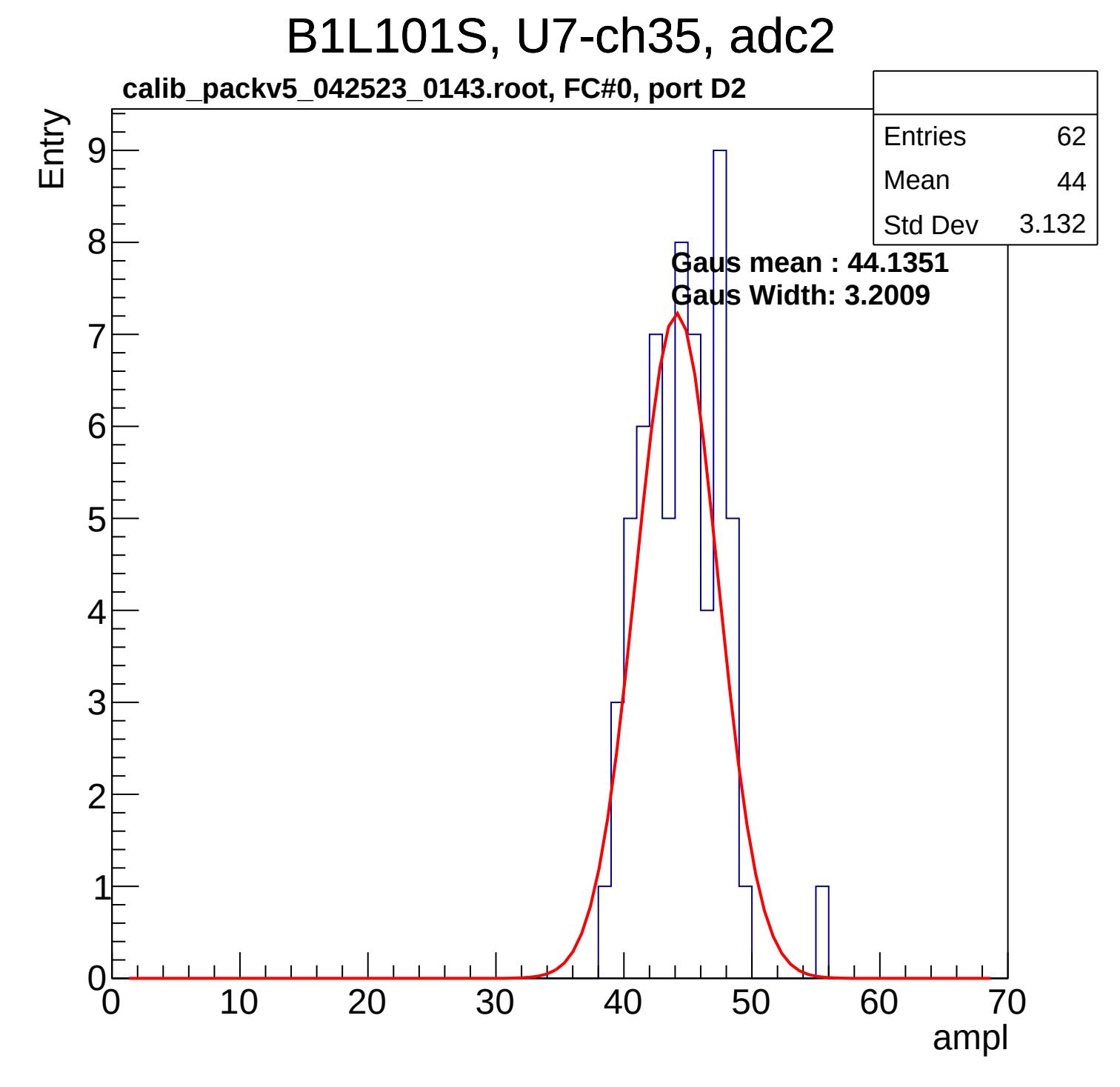
B1L101S, U7-ch35, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 44
Std Dev 3.132
Gaus mean : 44.1351
Gaus Width: 3.2009
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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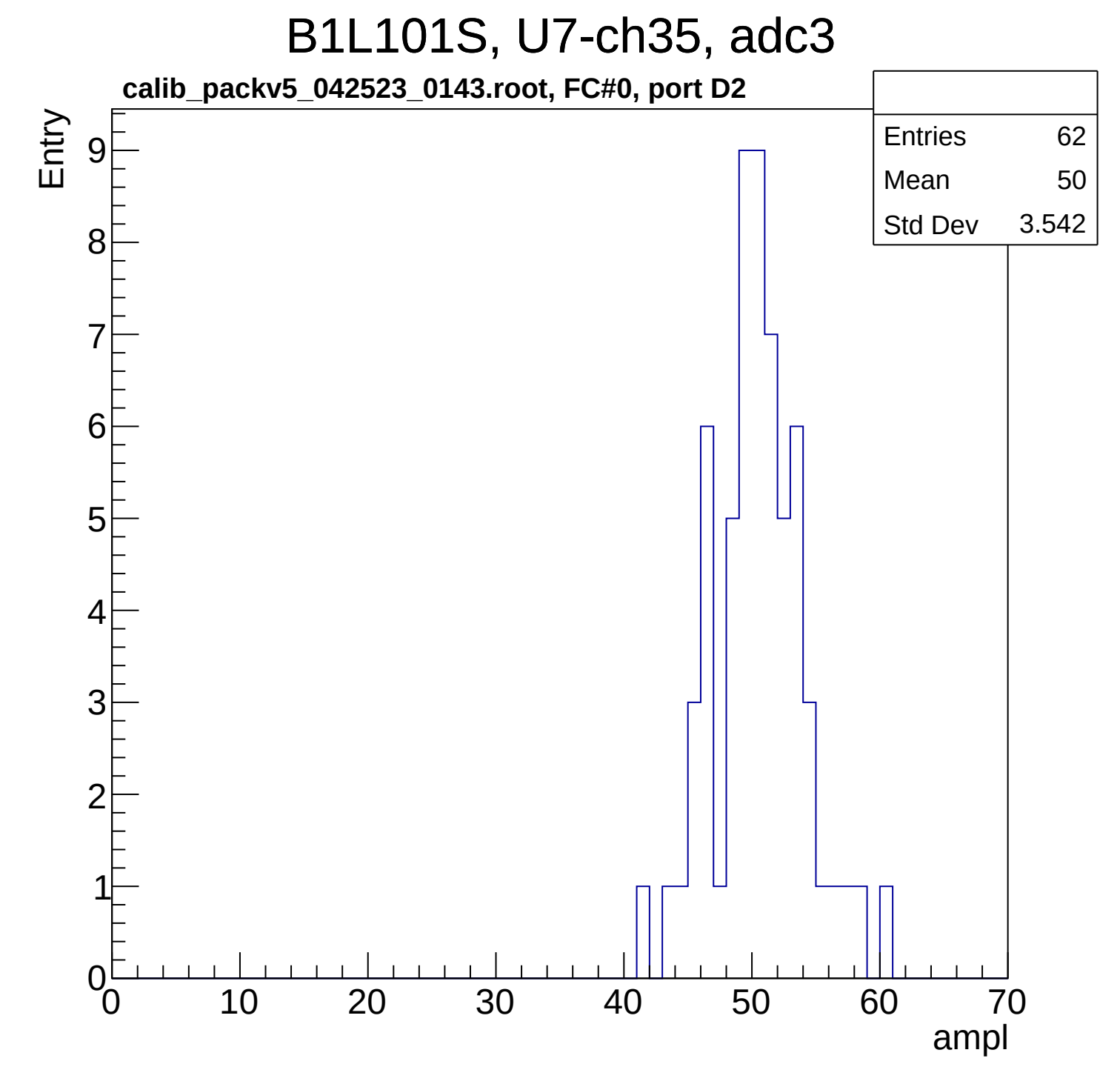
B1L101S, U7-ch35, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 50
Std Dev 3.542
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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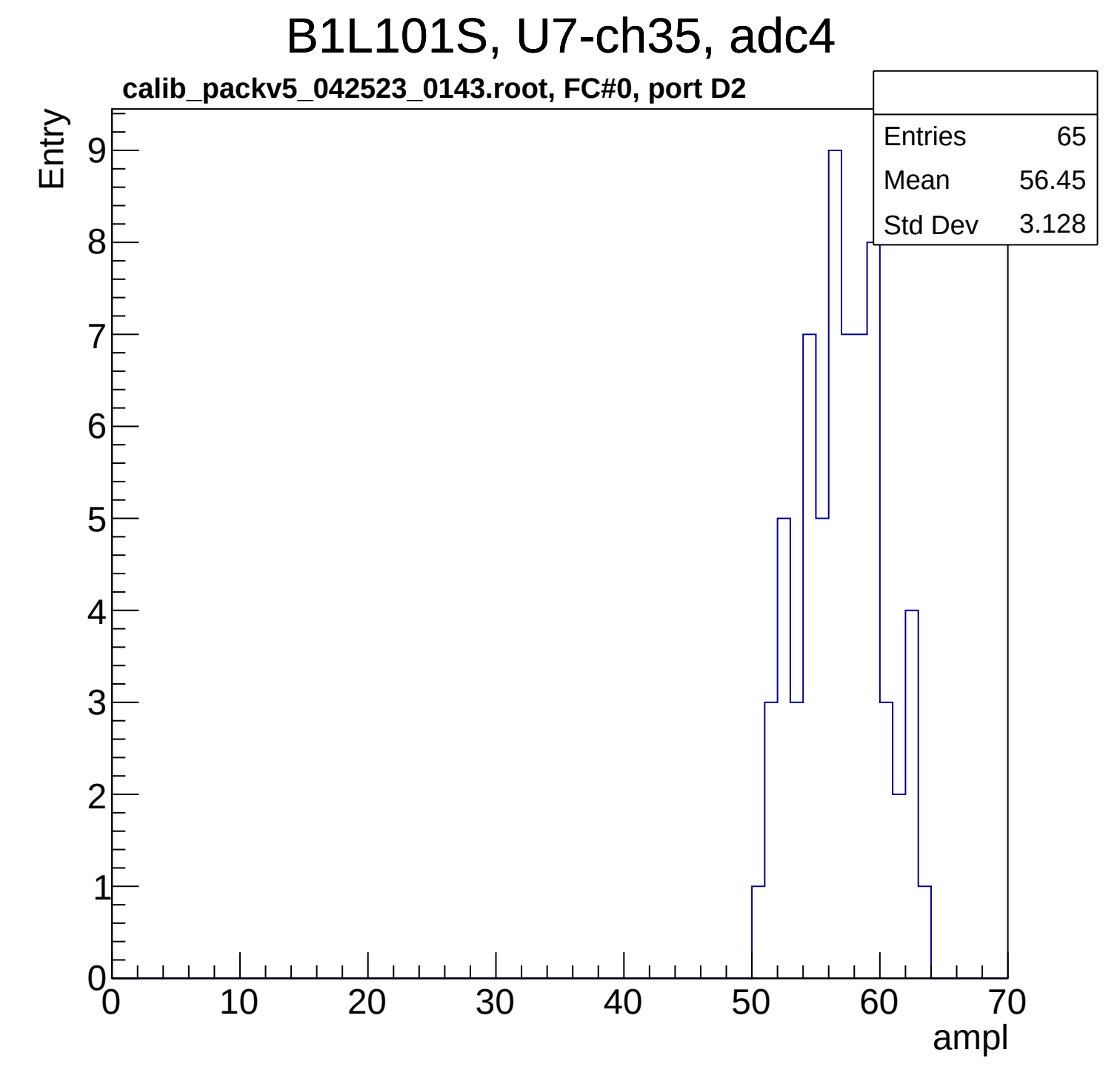
B1L101S, U7-ch35, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 56.45
Std Dev 3.128
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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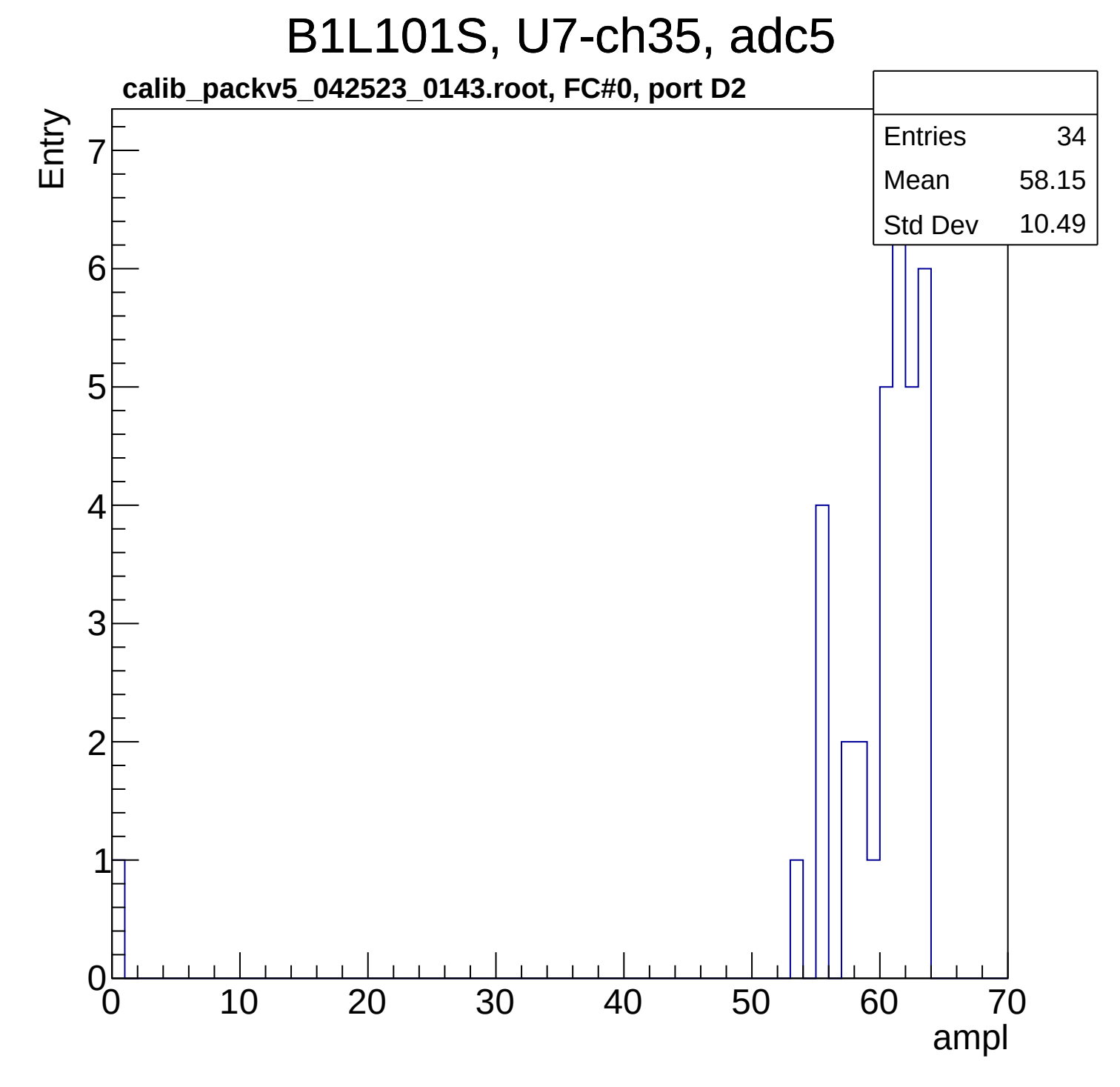
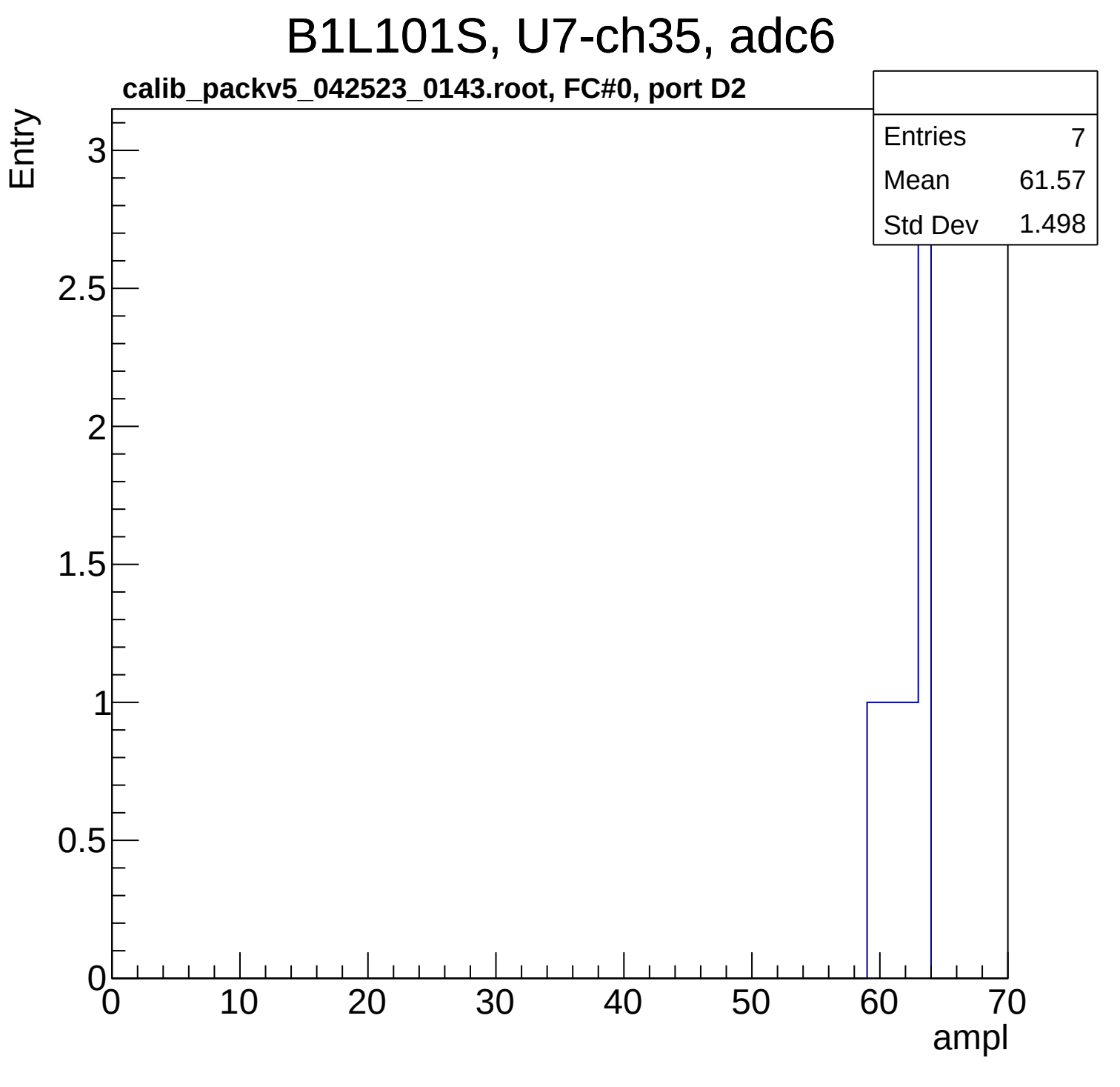
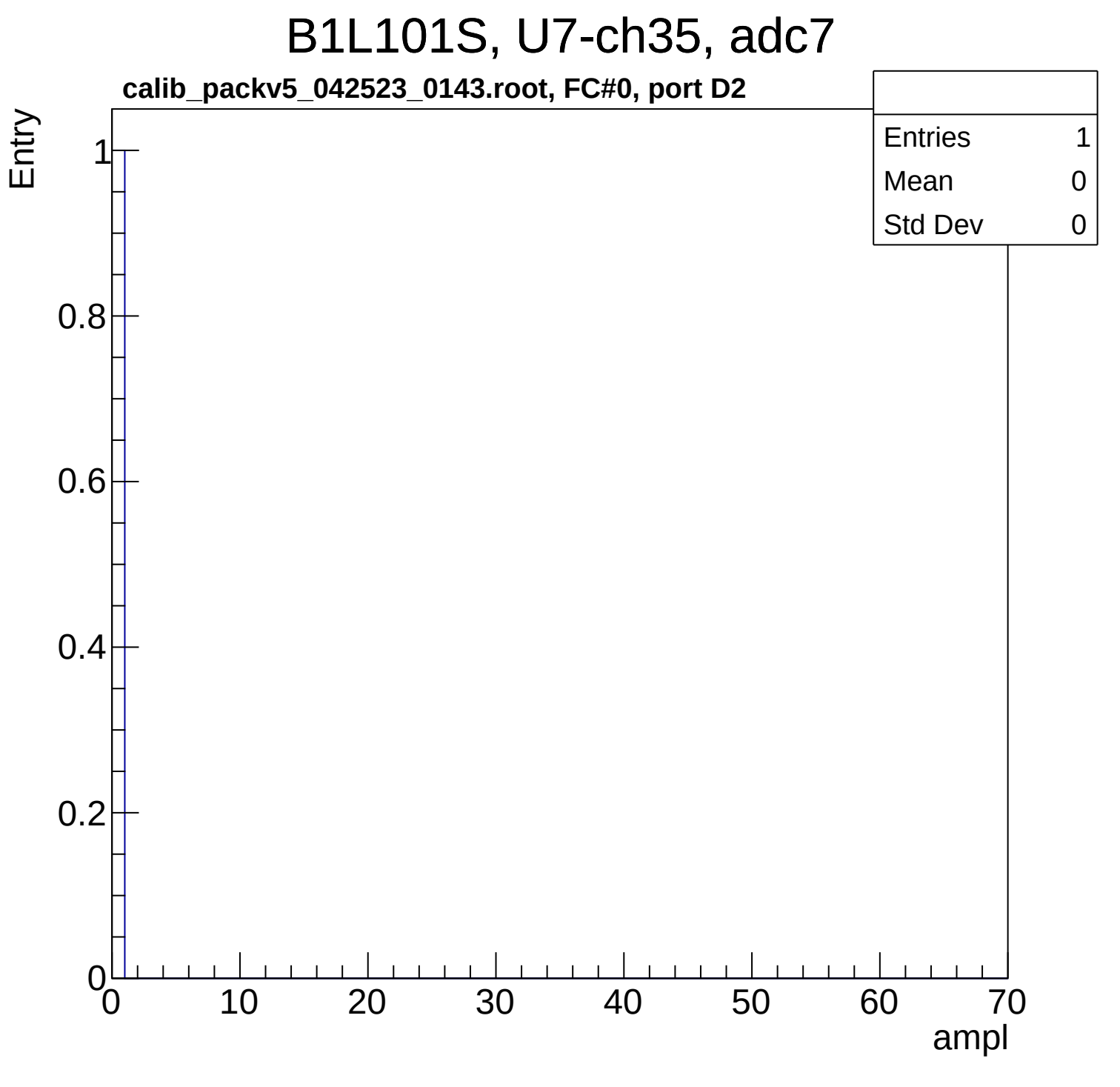
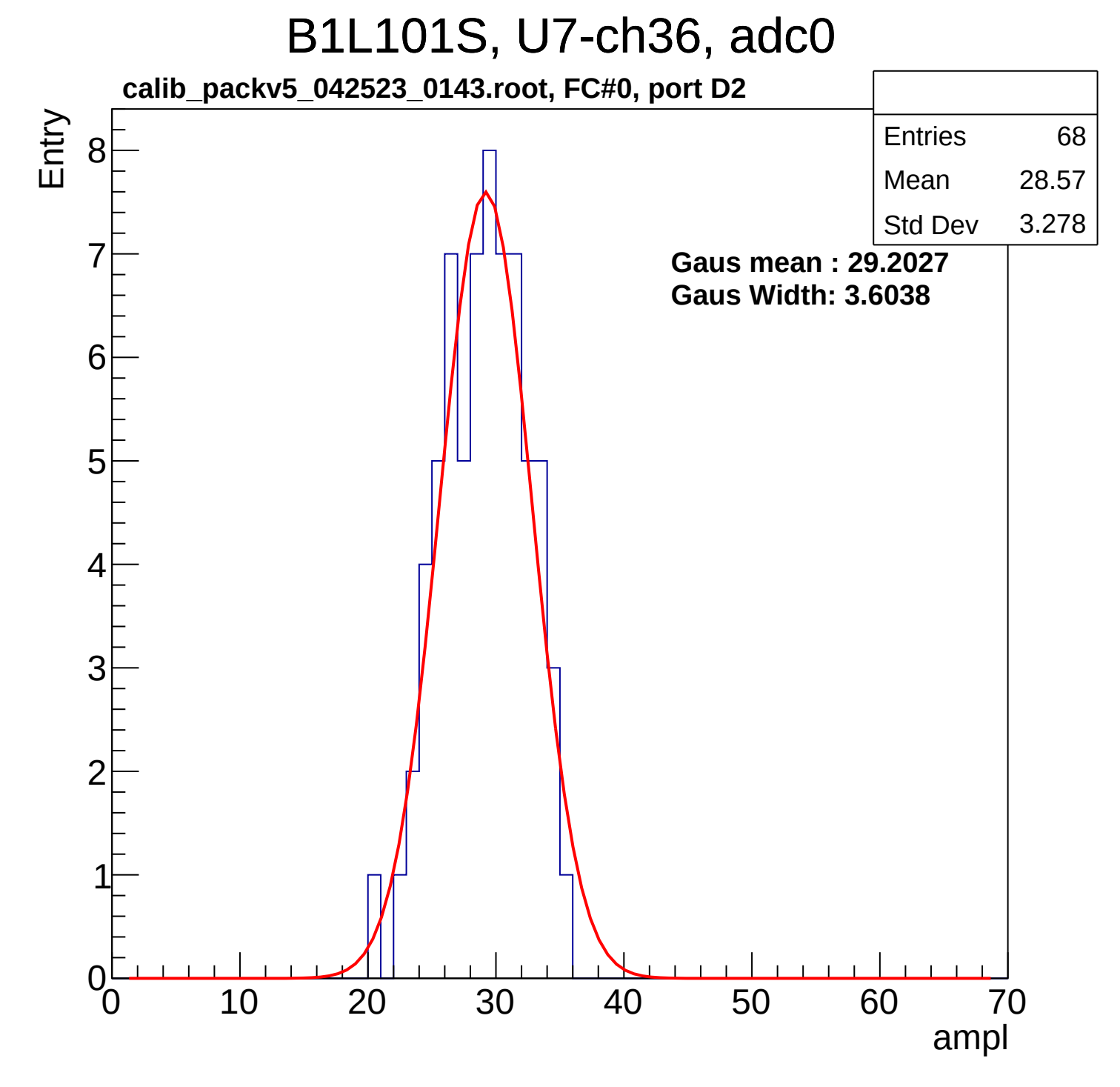

B1L101S, U7-ch35, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 34
Mean 58.15
Std Dev 10.49
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U7-ch35, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 61.57
Std Dev 1.498
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U7-ch35, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch36, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 28.57
Std Dev 3.278
Gaus mean : 29.2027
Gaus Width: 3.6038
Entry
ampl
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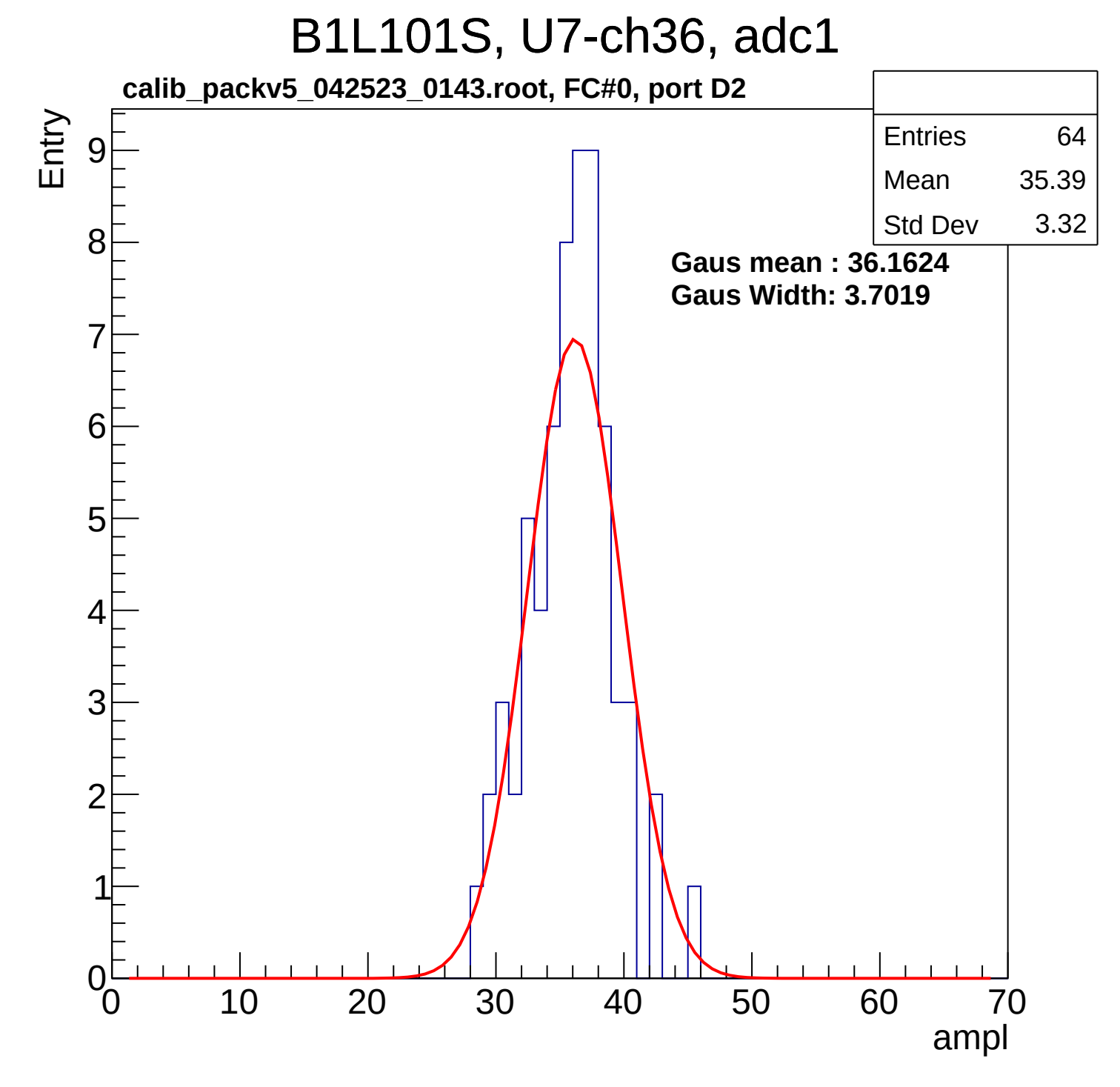
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch36, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 35.39
Std Dev 3.32
Gaus mean : 36.1624
Gaus Width: 3.7019
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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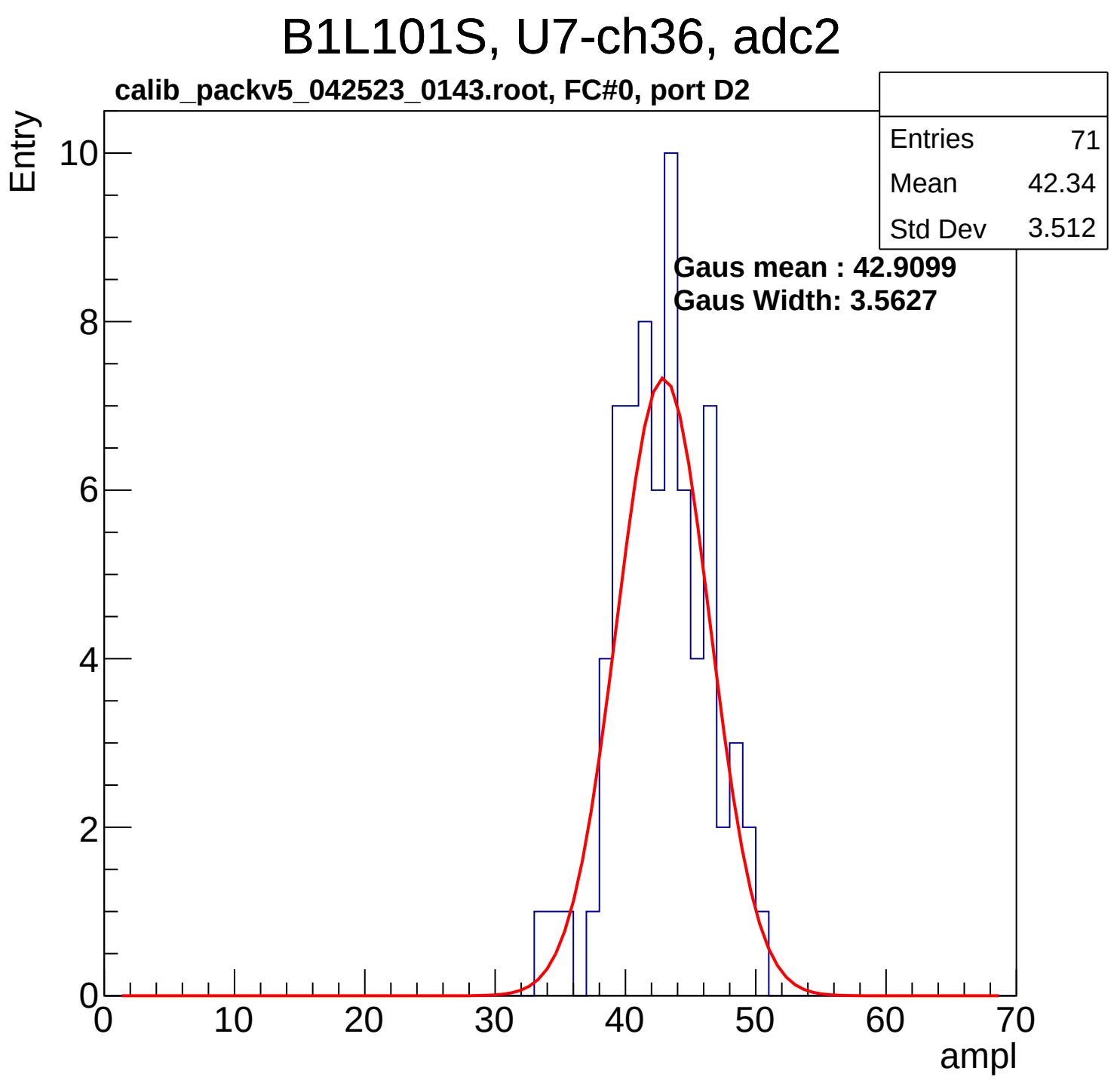
B1L101S, U7-ch36, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 42.34
Std Dev 3.512
Gaus mean : 42.9099
Gaus Width: 3.5627
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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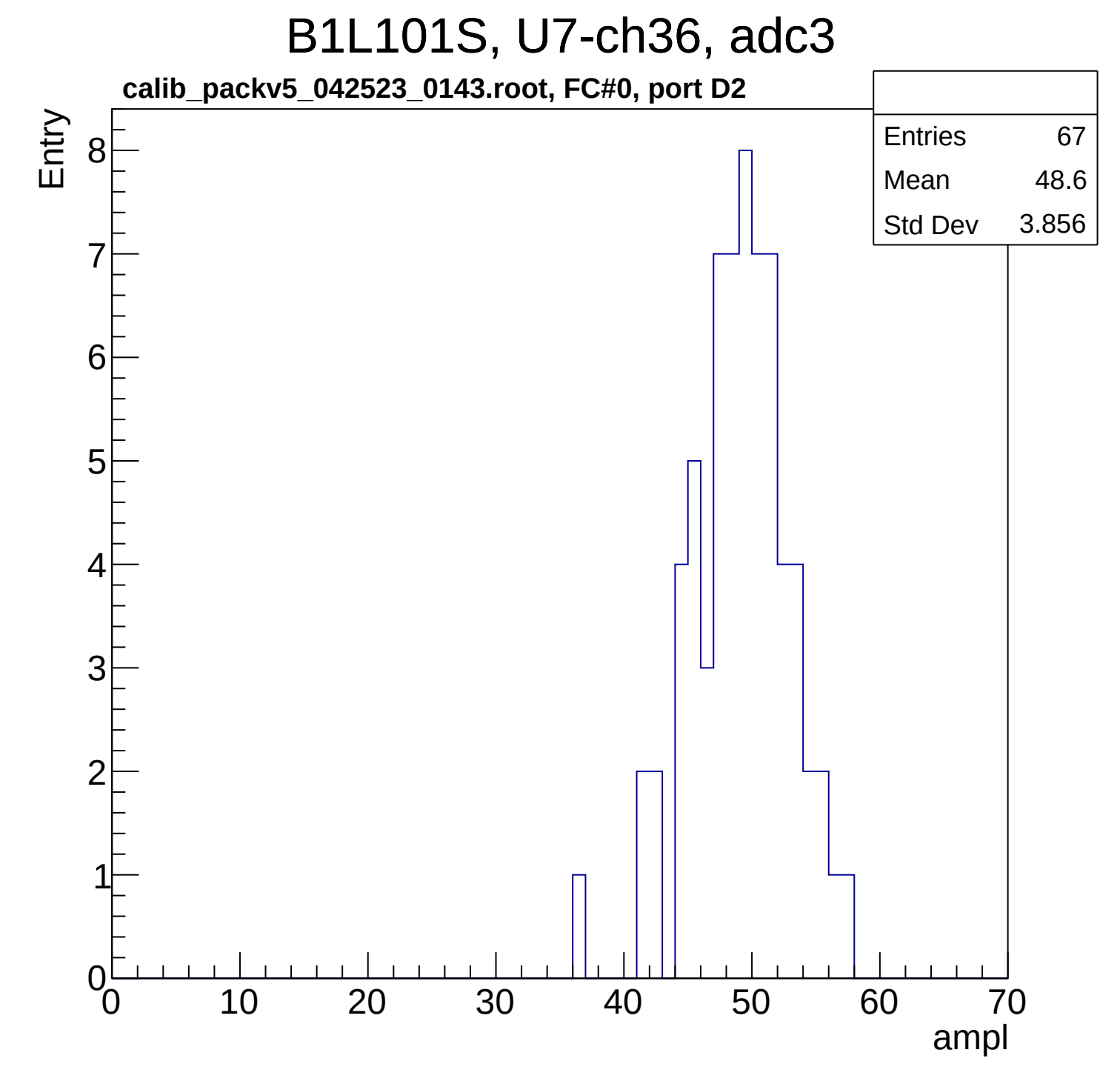
B1L101S, U7-ch36, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 48.6
Std Dev 3.856
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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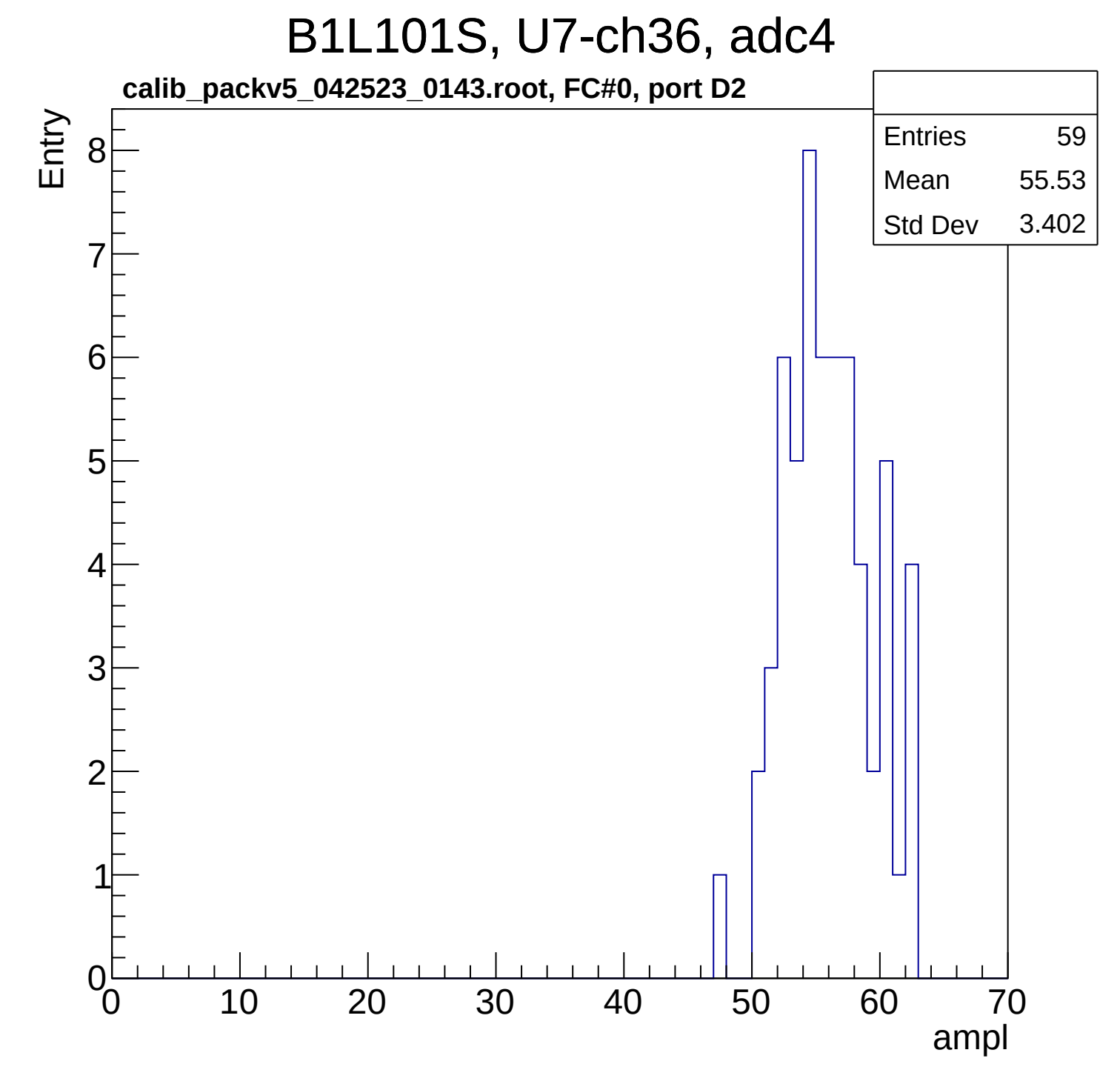
B1L101S, U7-ch36, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 55.53
Std Dev 3.402
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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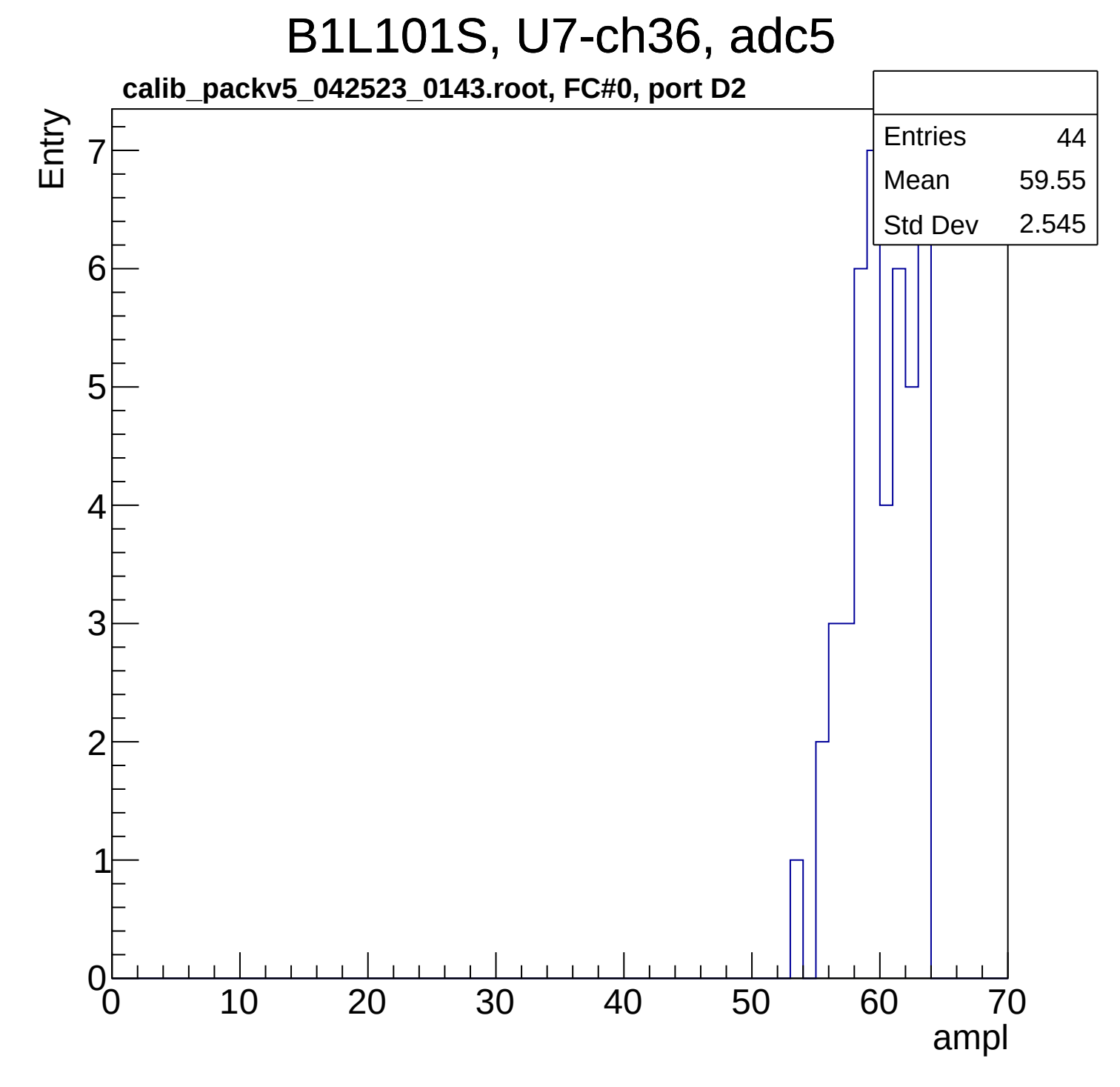
B1L101S, U7-ch36, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 44
Mean 59.55
Std Dev 2.545
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
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60
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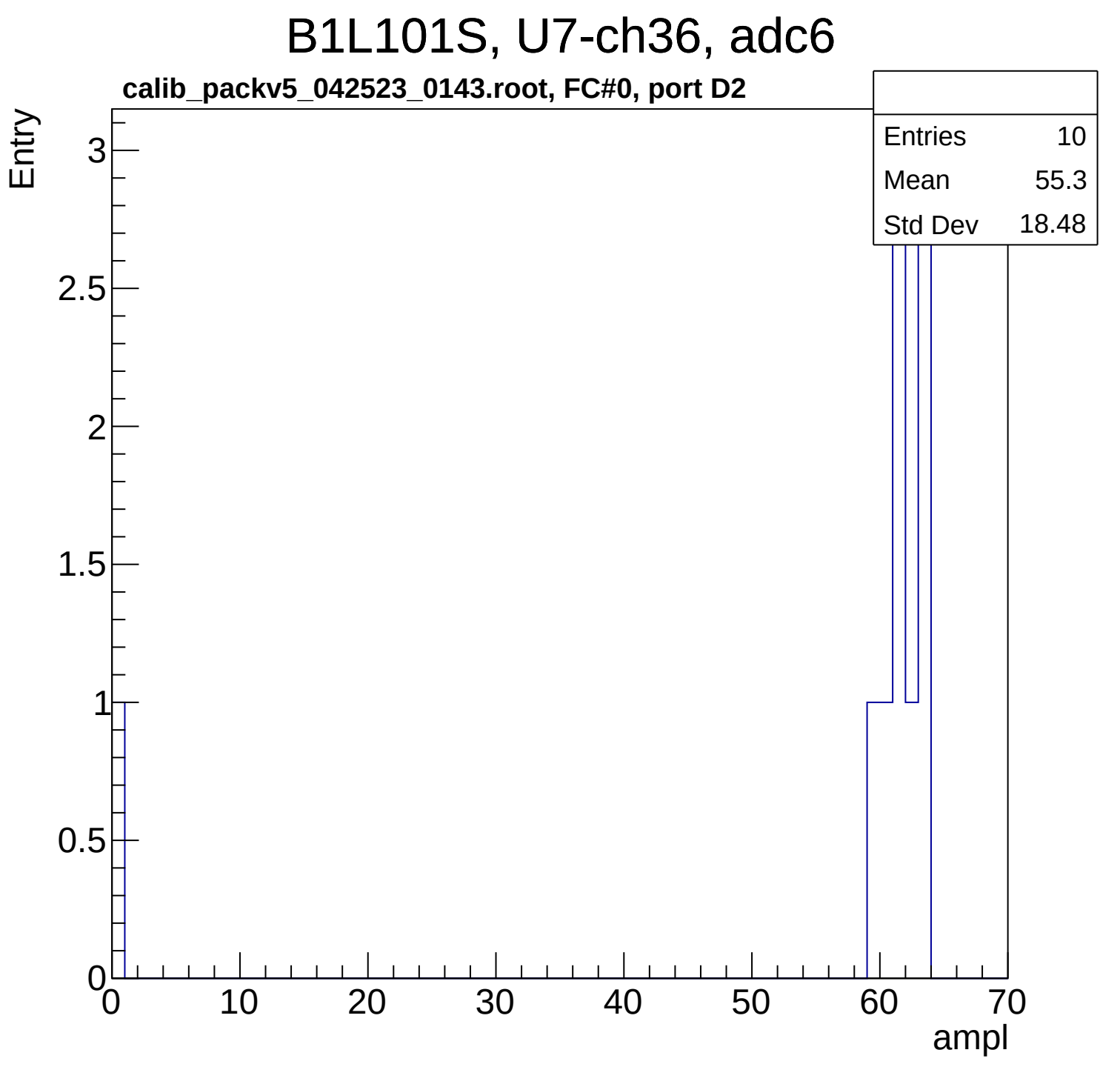
B1L101S, U7-ch36, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 55.3
Std Dev 18.48
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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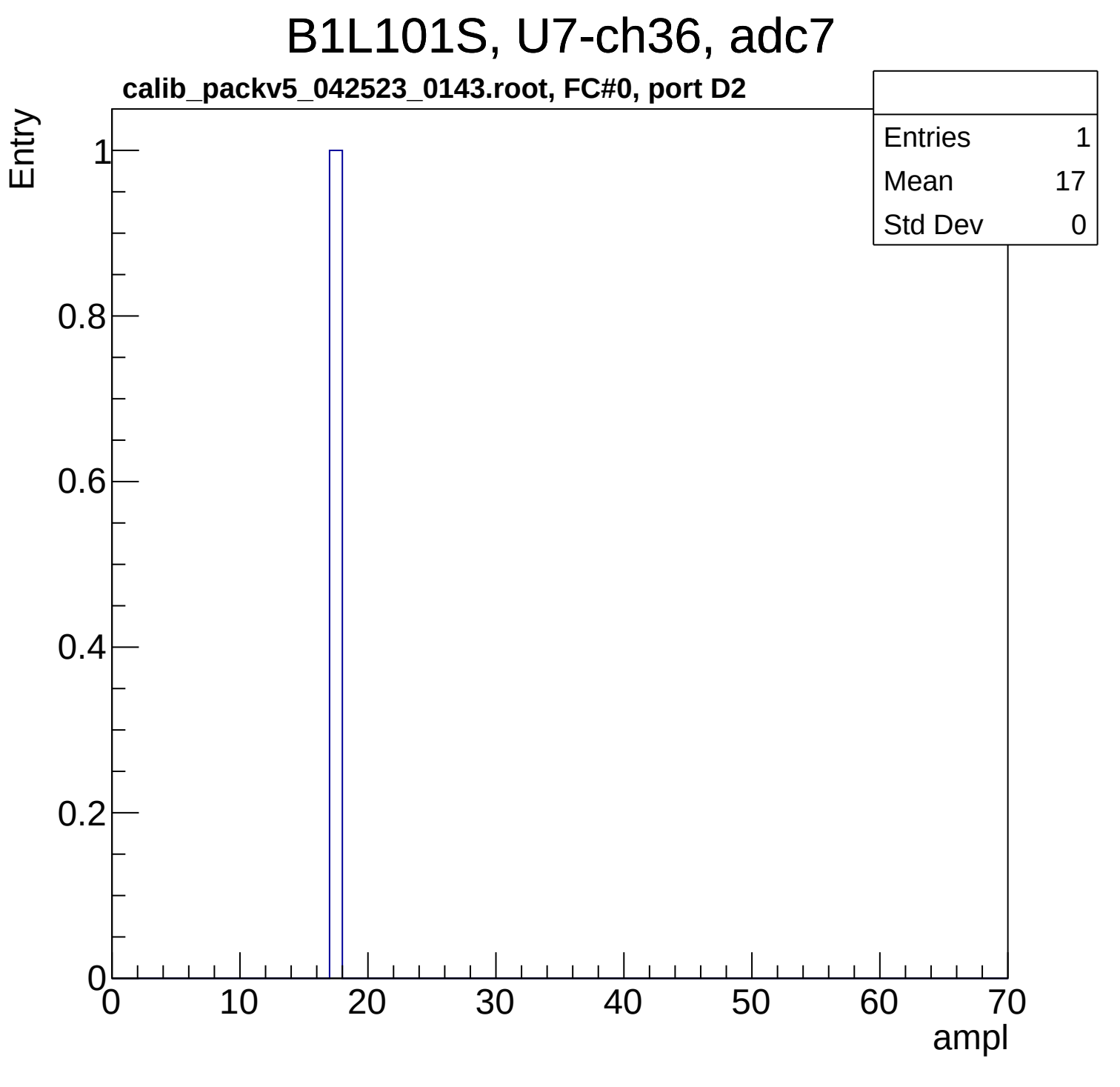
40
50
60
70


B1L101S, U7-ch36, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 17
Std Dev 0
Entry
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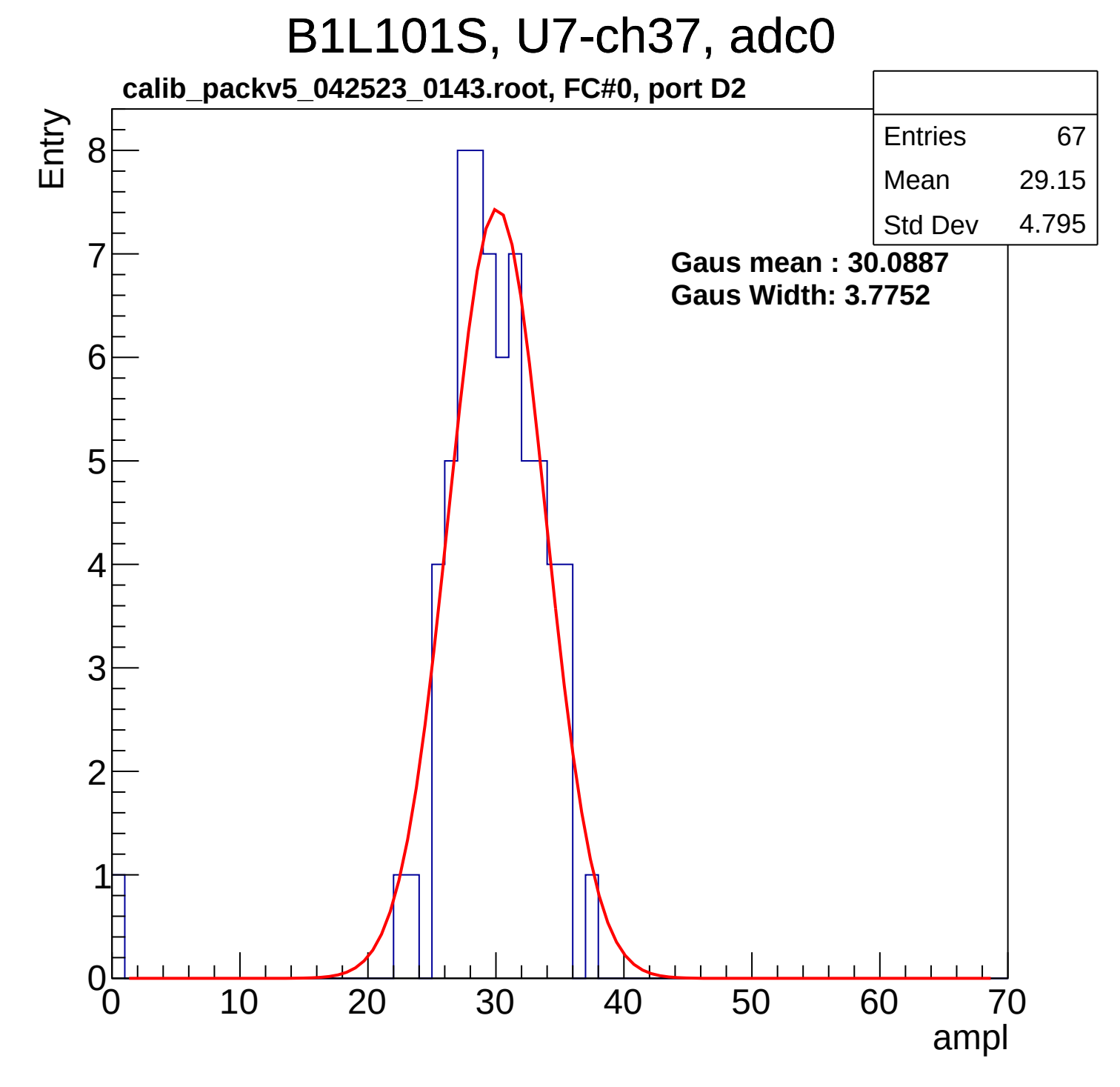
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch37, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 29.15
Std Dev 4.795
Gaus mean : 30.0887
Gaus Width: 3.7752
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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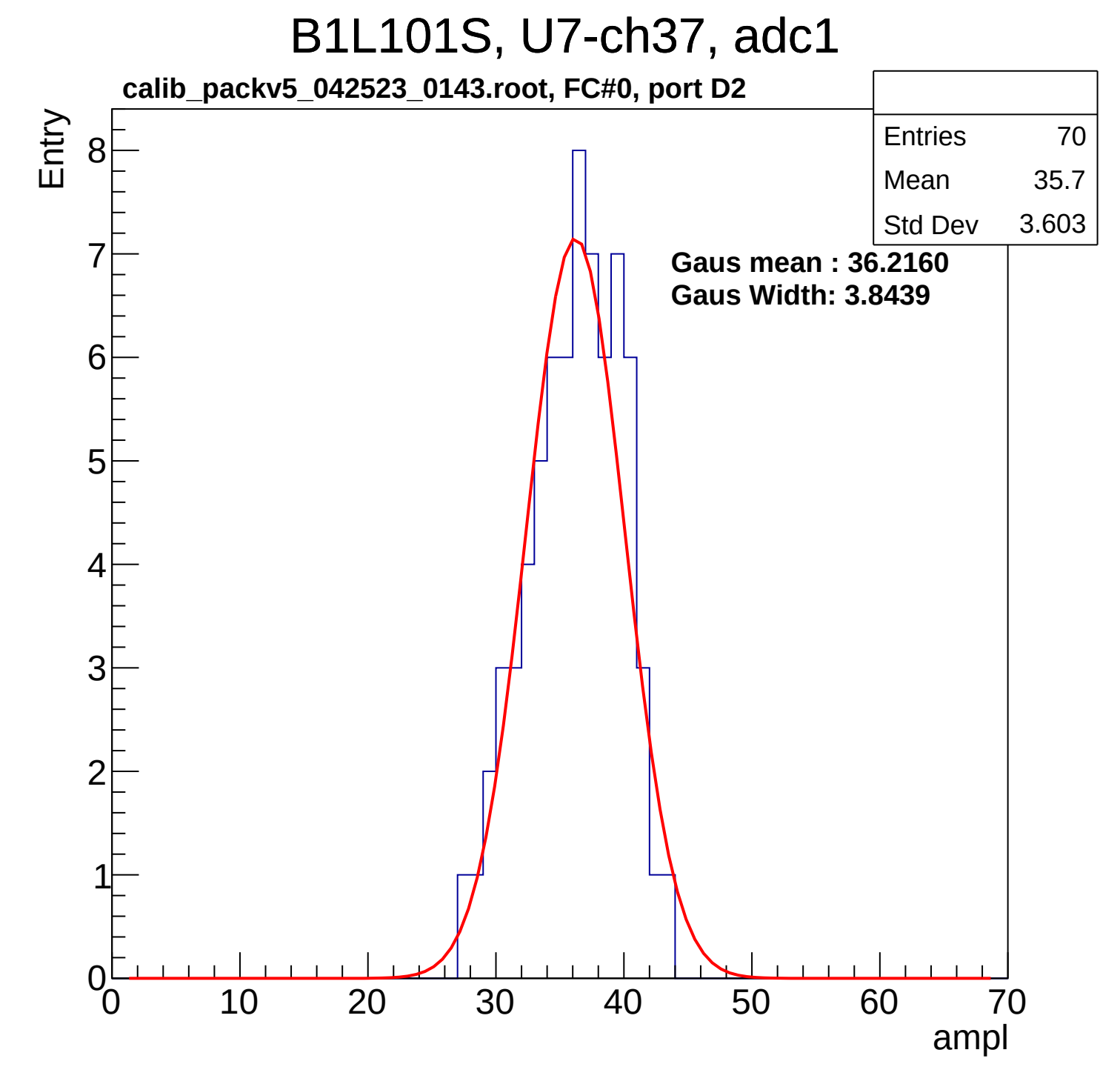
B1L101S, U7-ch37, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 35.7
Std Dev 3.603
Gaus mean : 36.2160
Gaus Width: 3.8439
Entry
ampl
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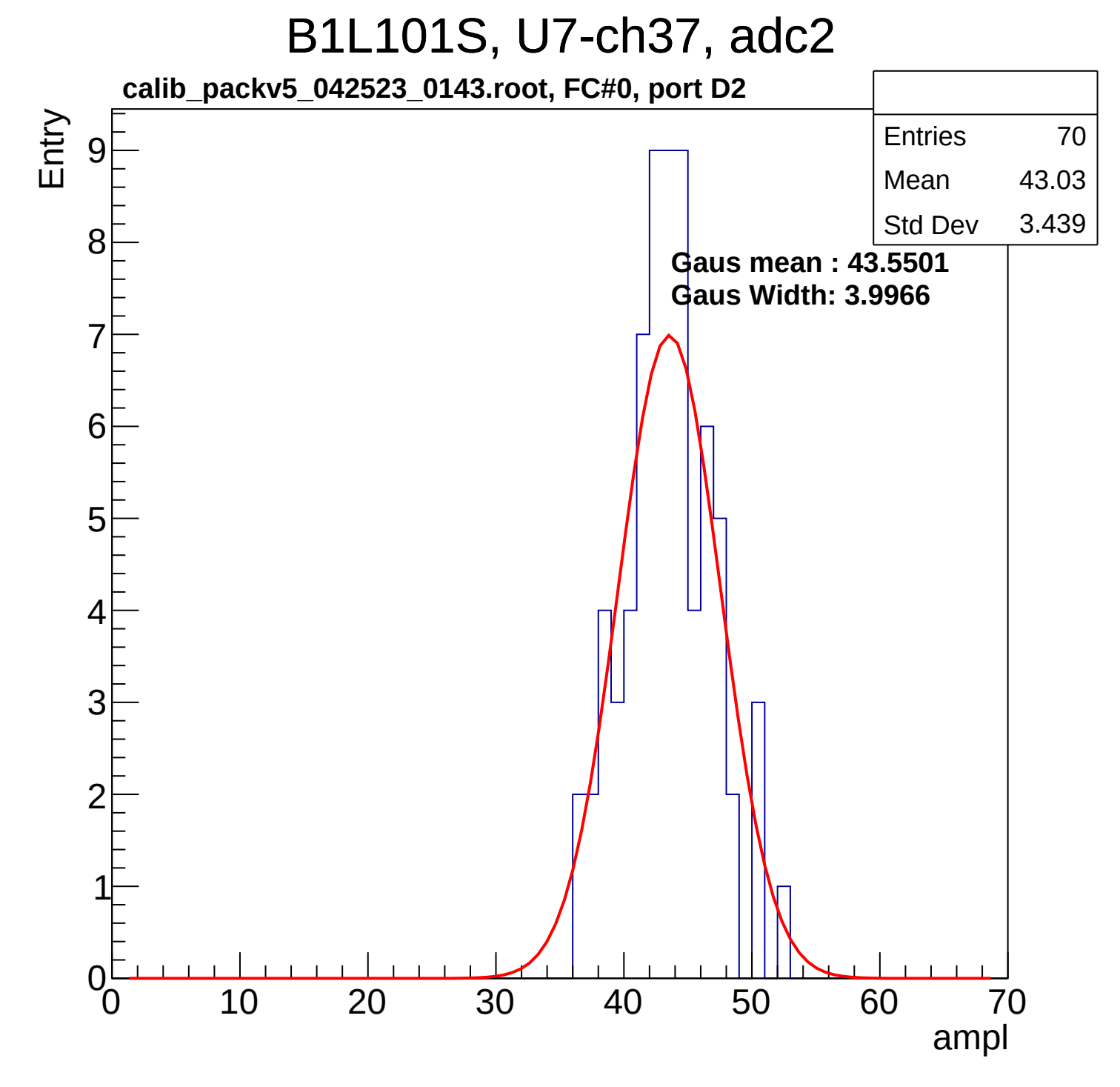
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch37, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 43.03
Std Dev 3.439
Gaus mean : 43.5501
Gaus Width: 3.9966
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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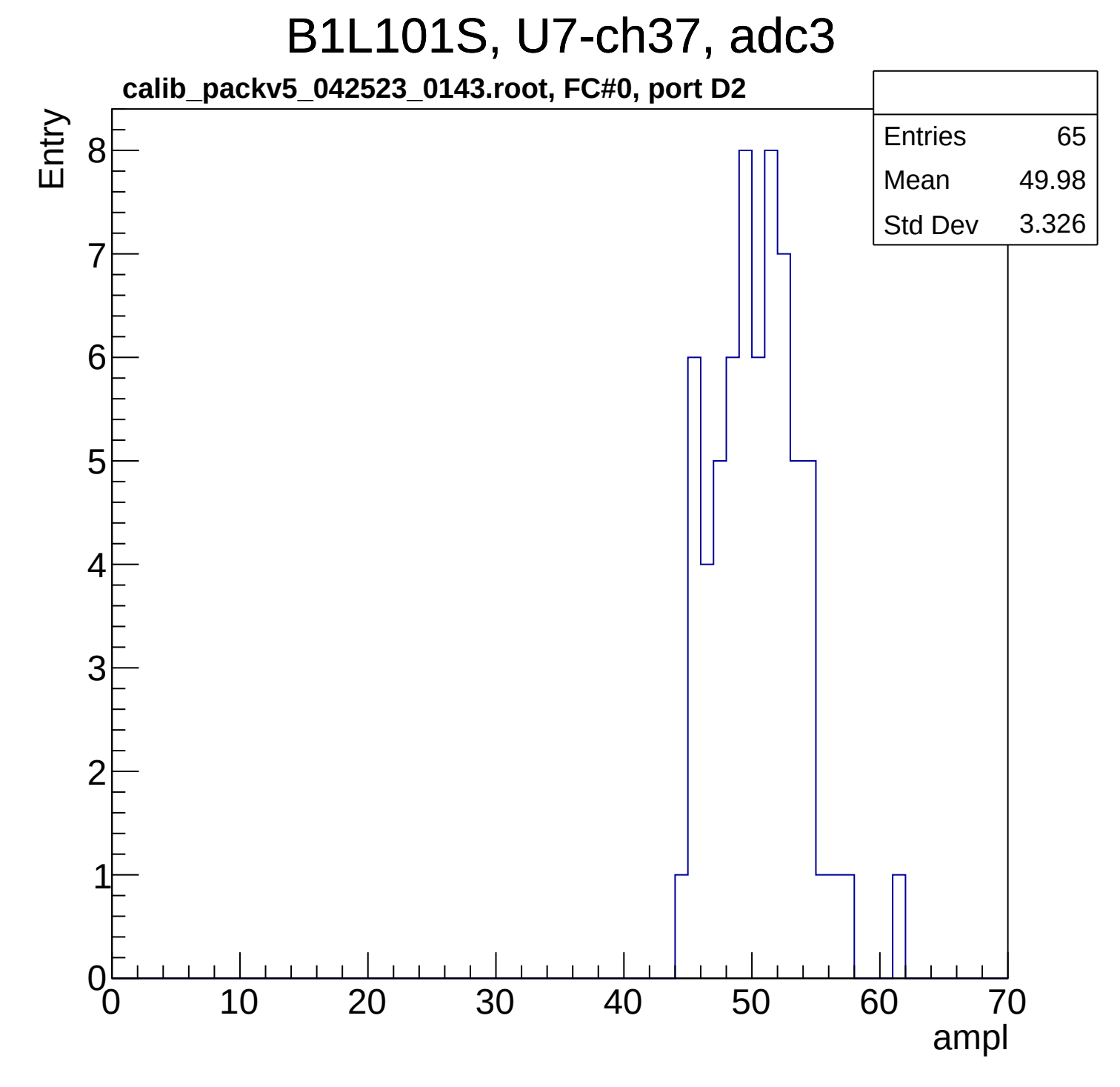
B1L101S, U7-ch37, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 49.98
Std Dev 3.326
Entry
ampl
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3
4
5
6
7
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0
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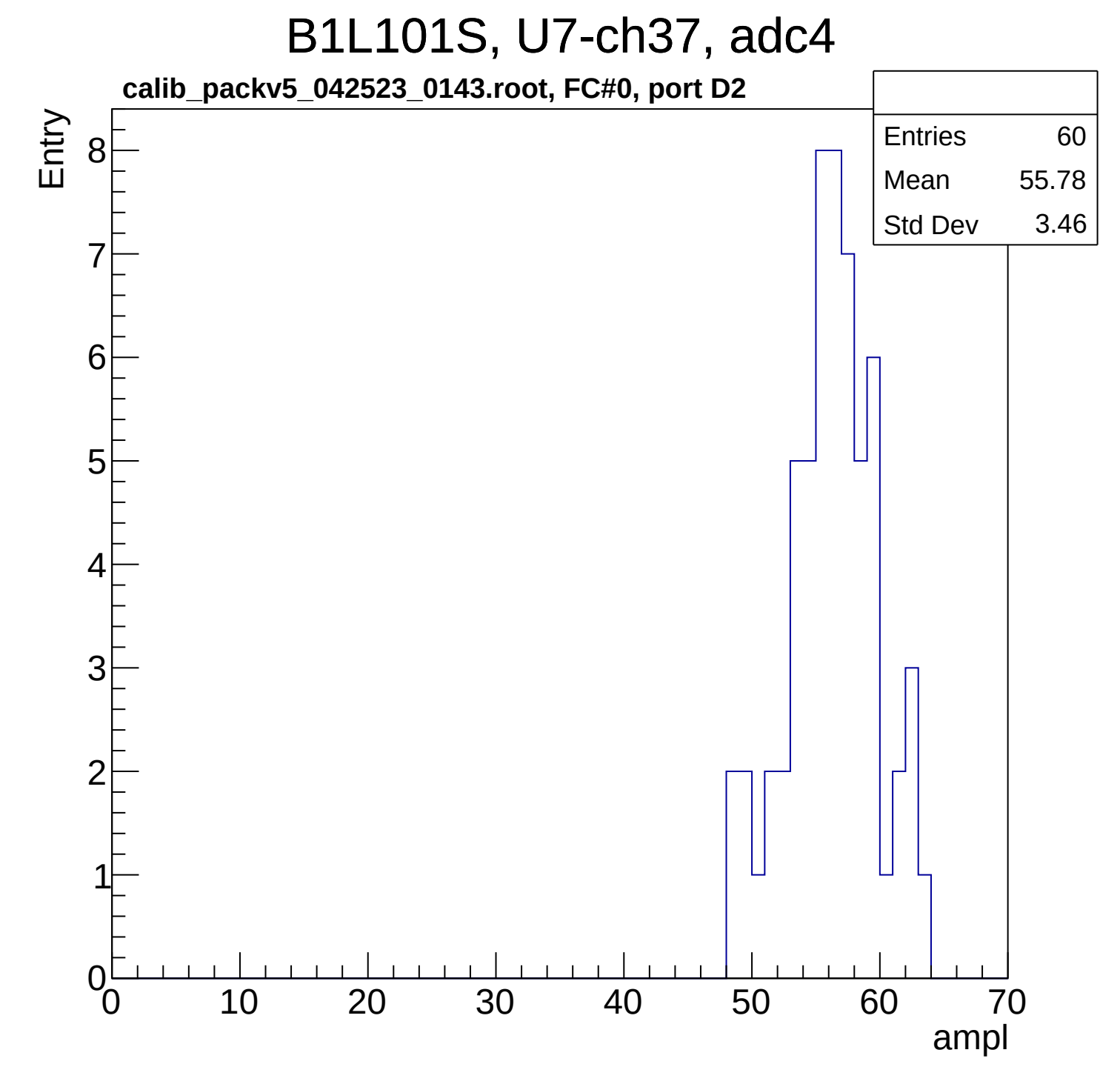
B1L101S, U7-ch37, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 55.78
Std Dev 3.46
Entry
ampl
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4
5
6
7
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0
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20
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40
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60
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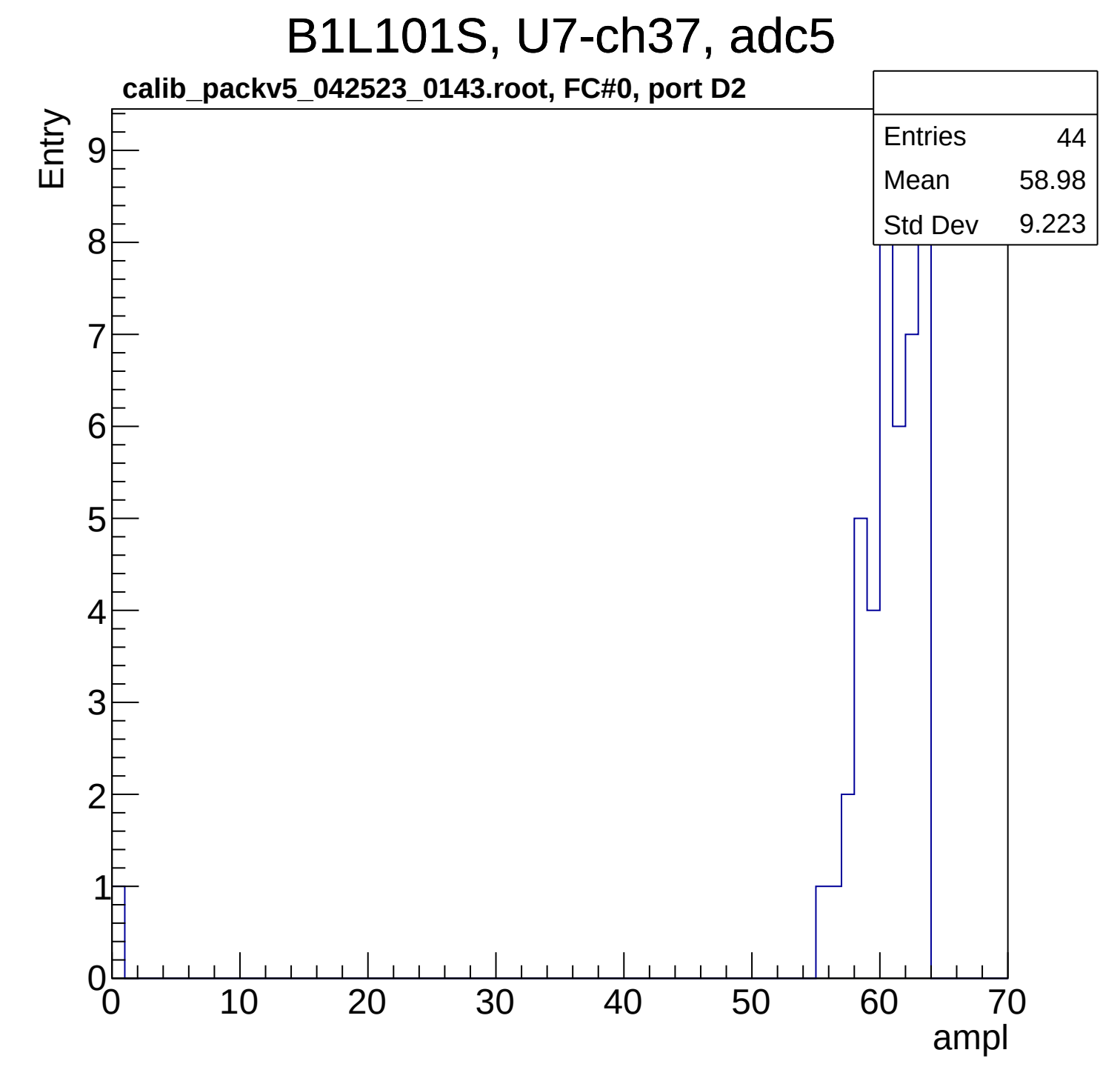
B1L101S, U7-ch37, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 44
Mean 58.98
Std Dev 9.223
Entry
ampl
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4
5
6
7
8
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0
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60
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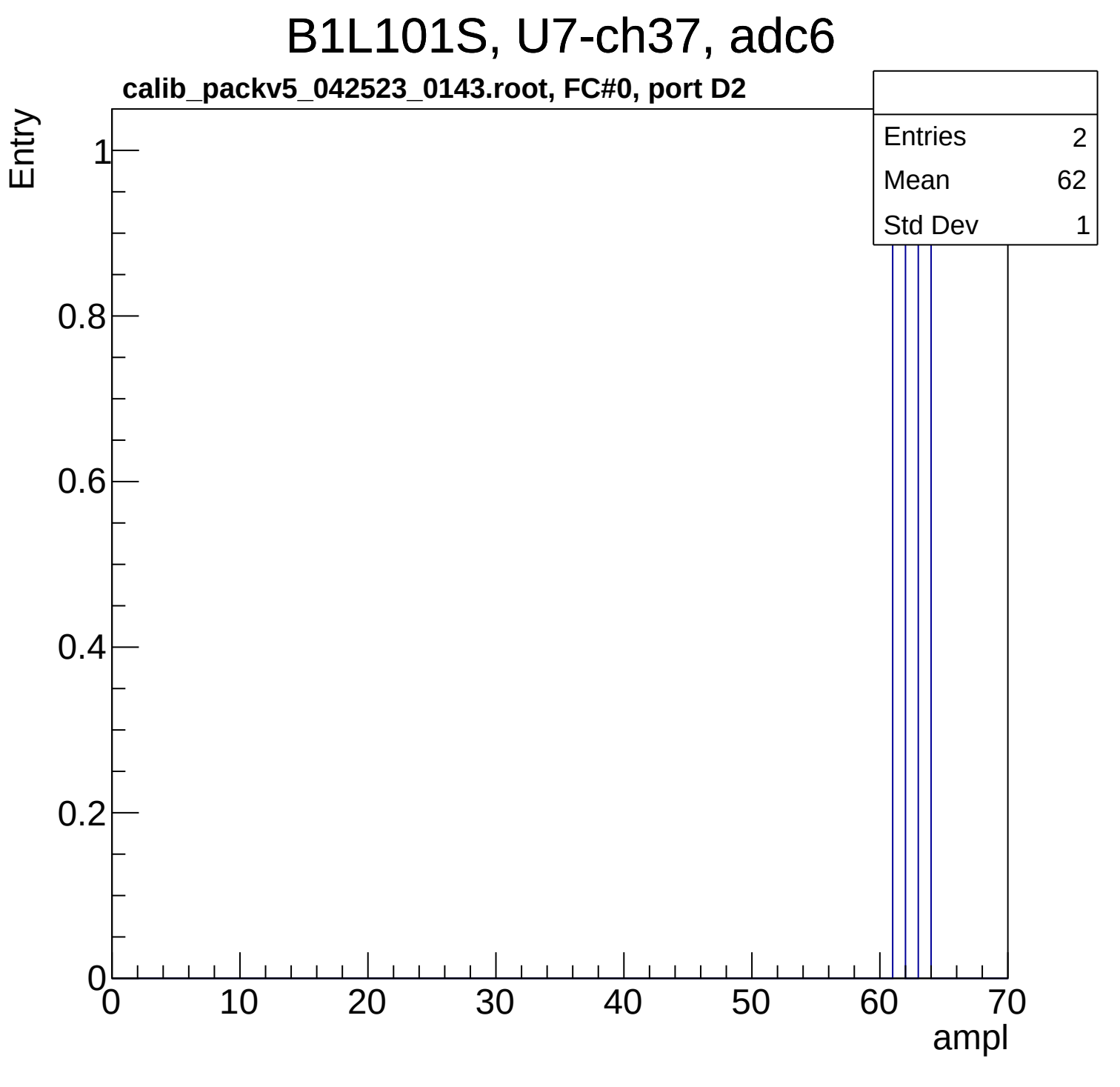
B1L101S, U7-ch37, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 62
Std Dev 1
Entry
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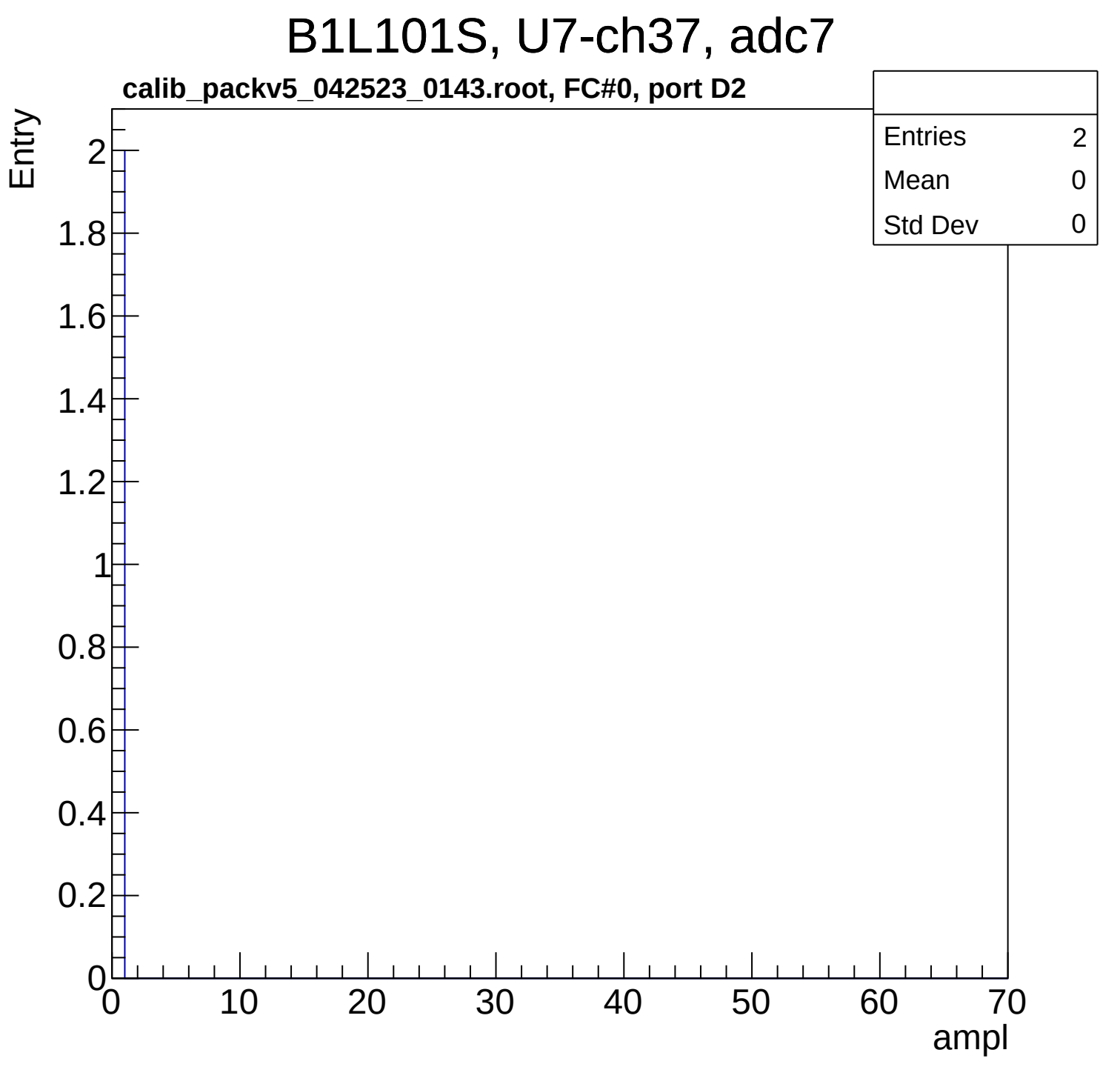
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch37, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
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40
50
60
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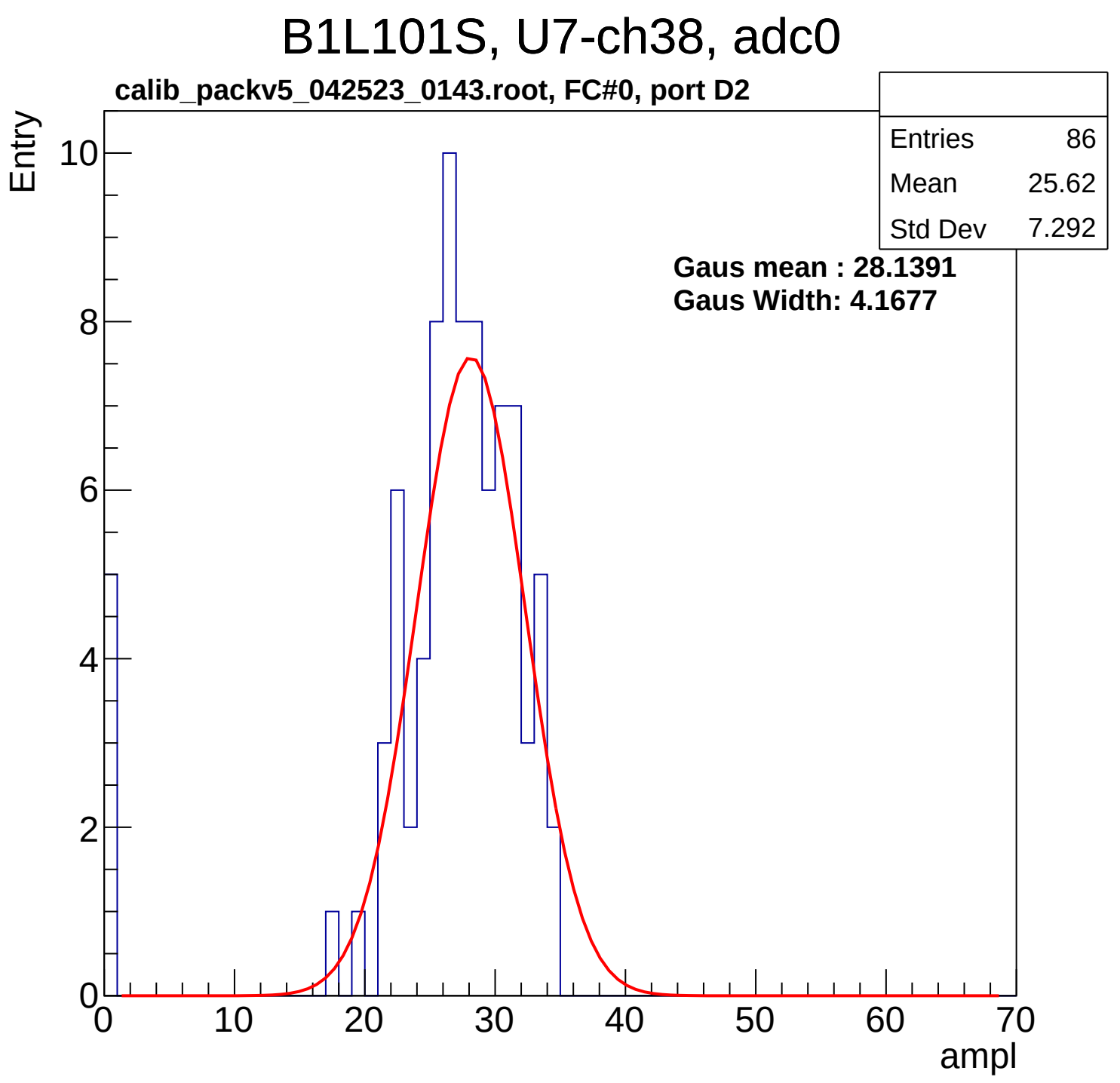
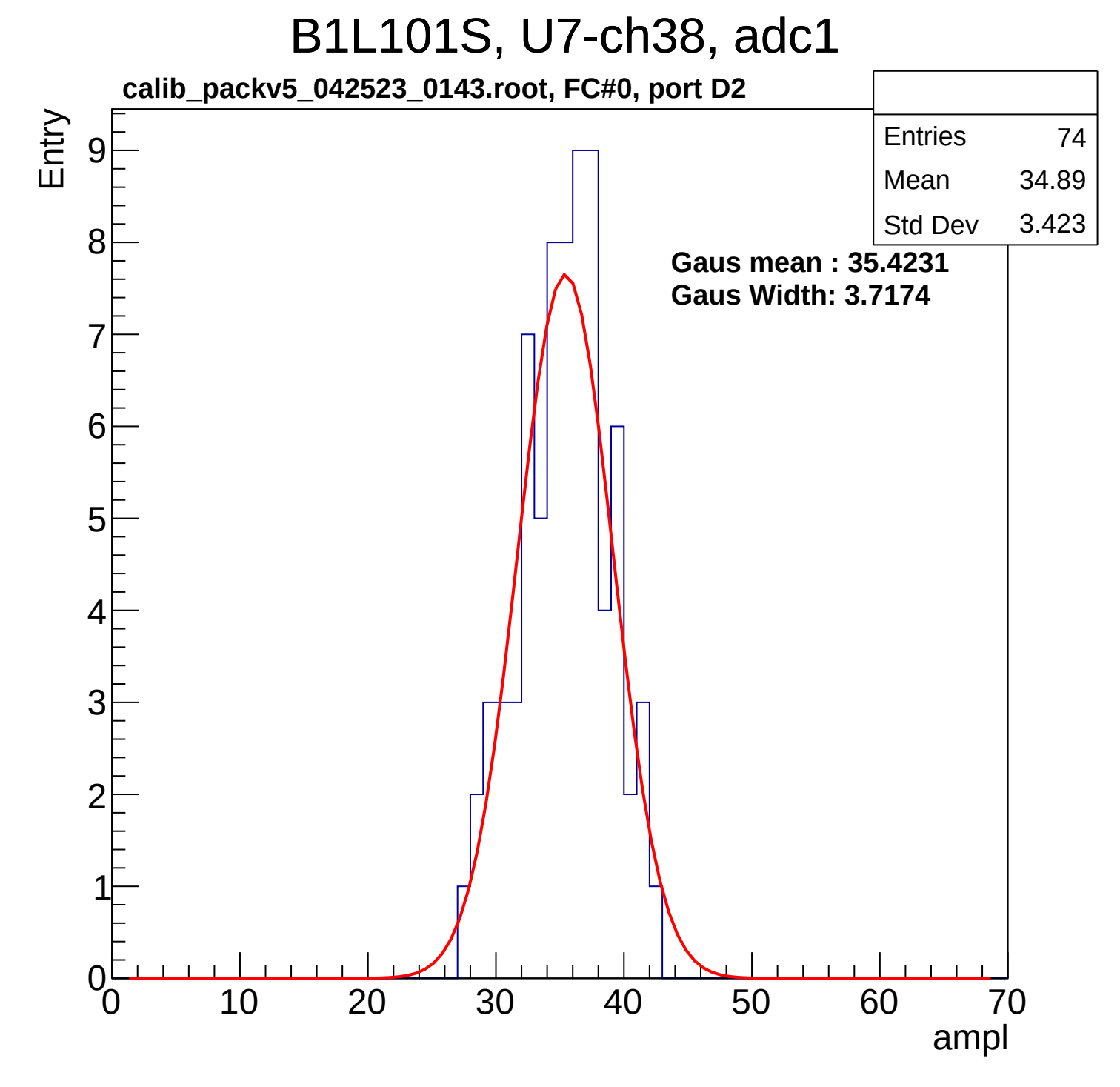

B1L101S, U7-ch38, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 86
Mean 25.62
Std Dev 7.292
Gaus mean : 28.1391
Gaus Width: 4.1677
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch38, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 34.89
Std Dev 3.423
Gaus mean : 35.4231
Gaus Width: 3.7174
Entry
ampl
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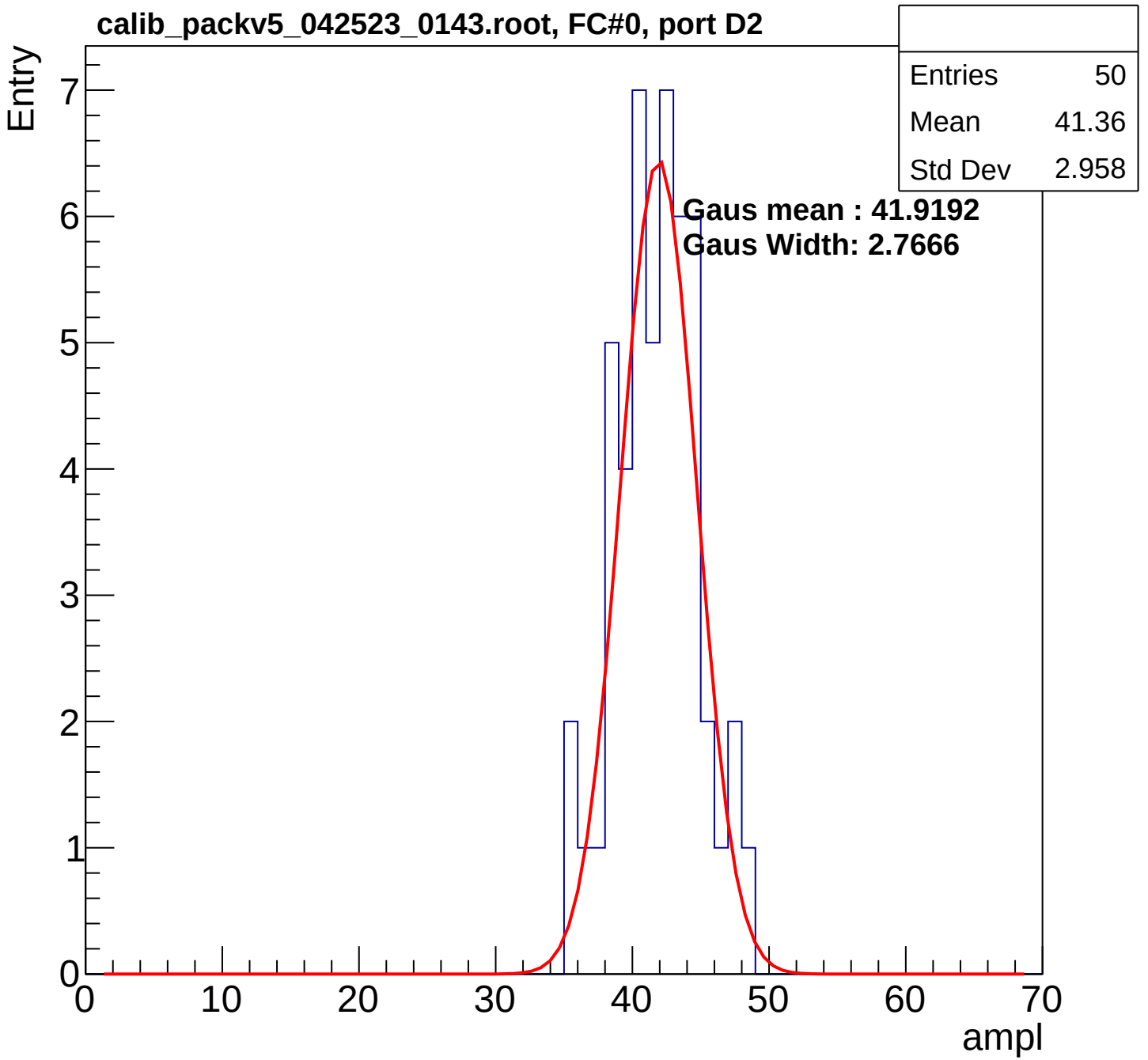
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L101S, U7-ch38, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 41.36
Std Dev 2.958
Gaus mean : 41.9192
Gaus Width: 2.7666
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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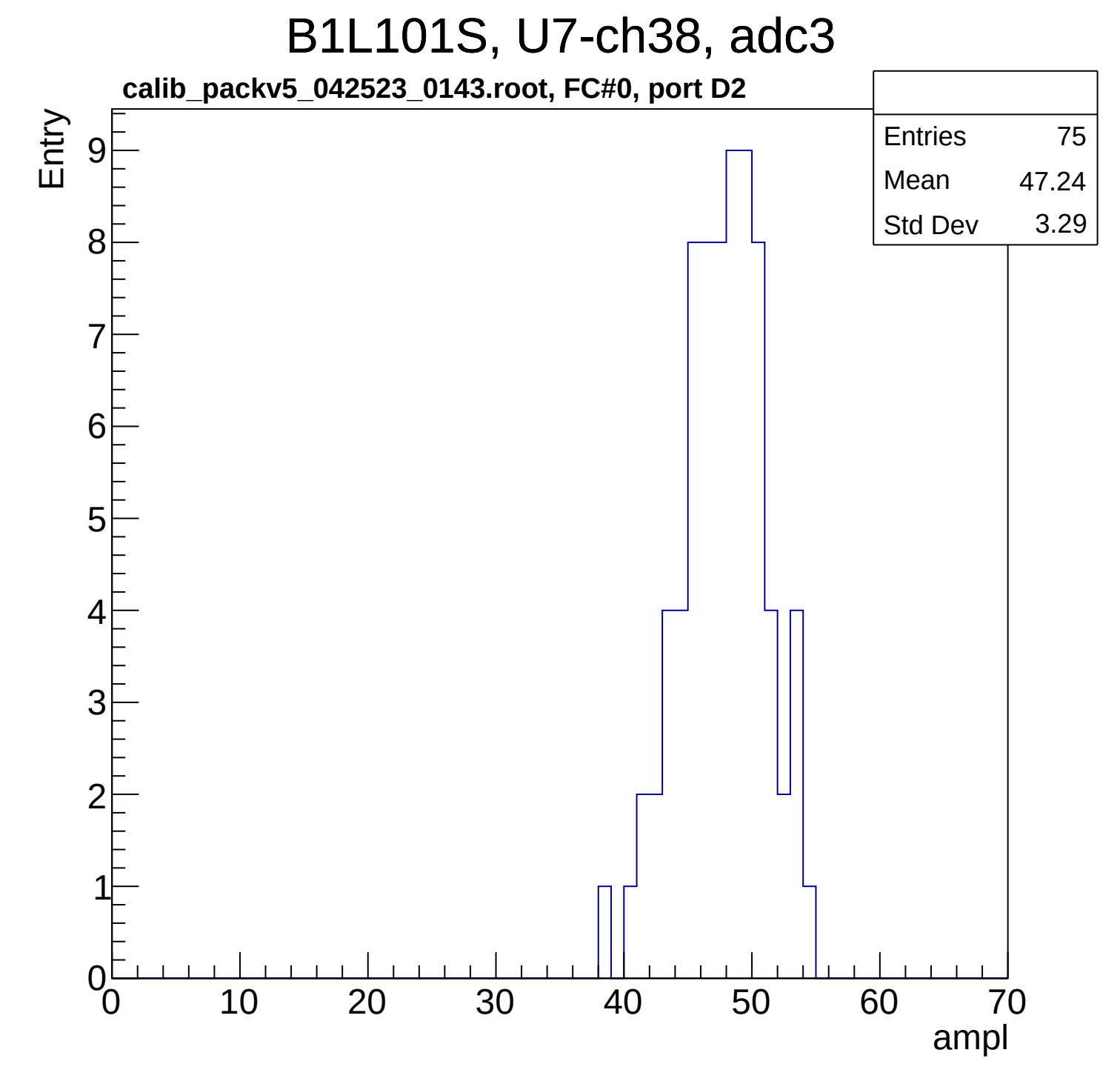
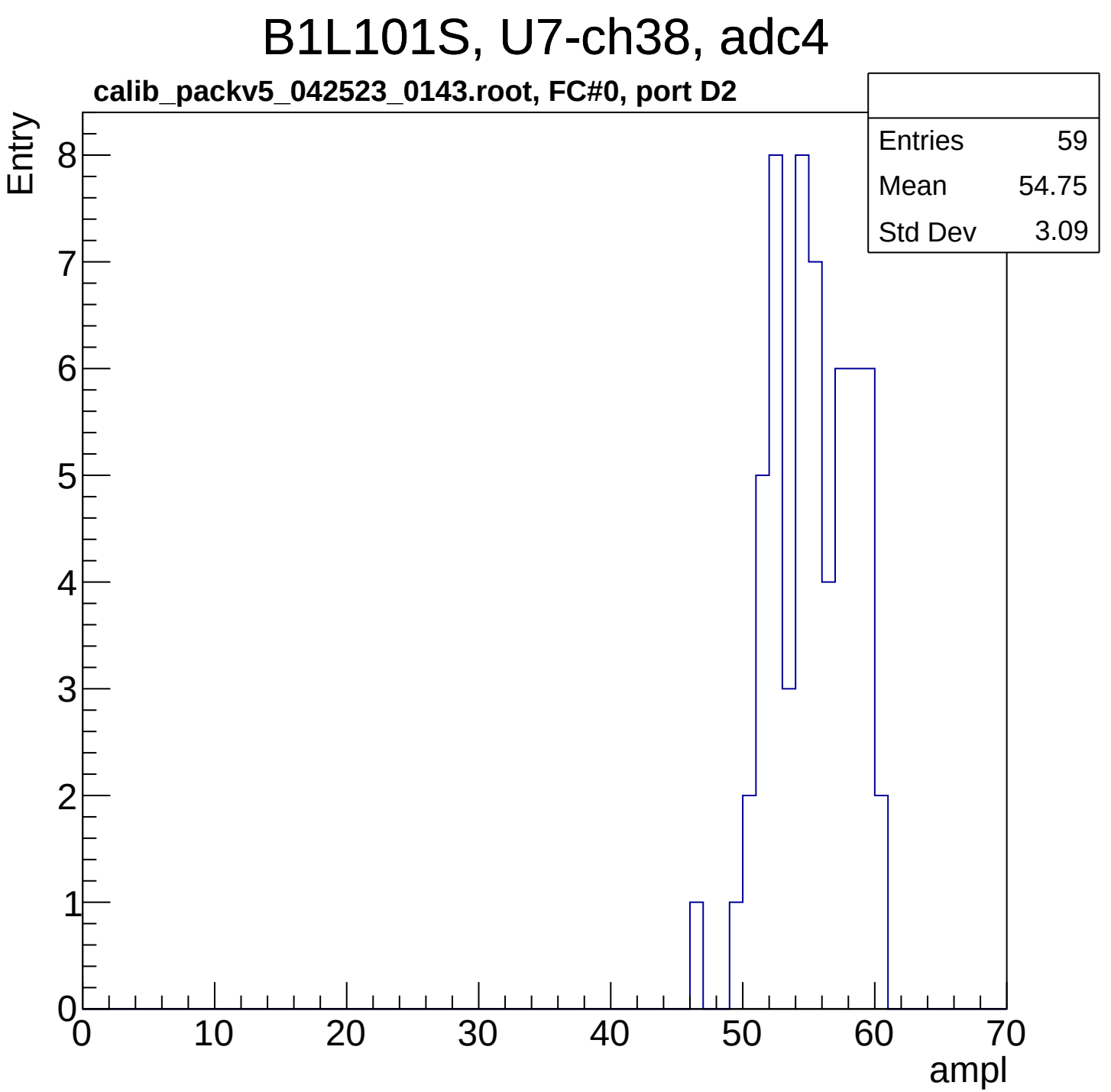

B1L101S, U7-ch38, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 47.24
Std Dev 3.29
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch38, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 54.75
Std Dev 3.09
Entry
ampl
0
1
2
3
4
5
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0
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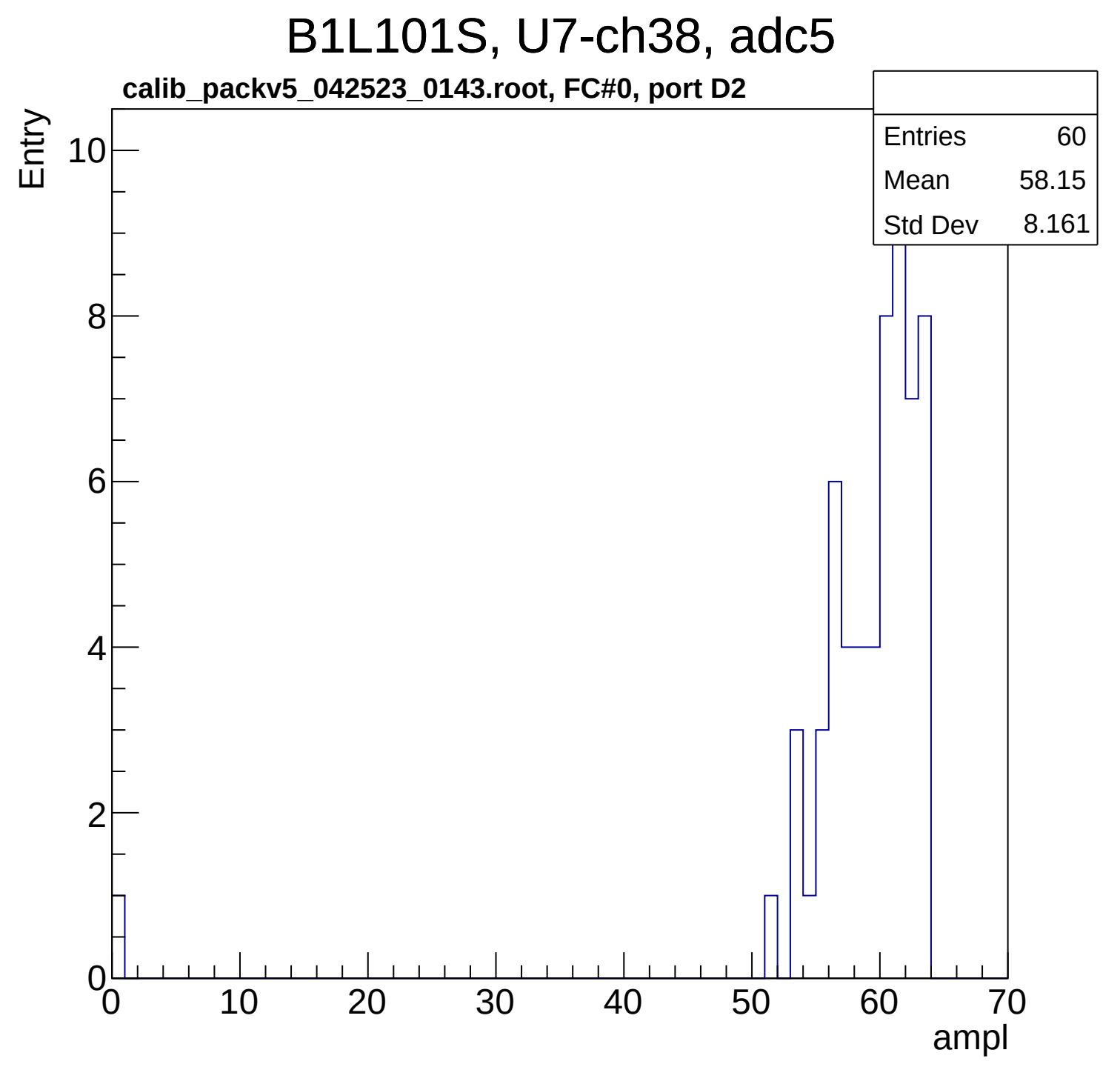
B1L101S, U7-ch38, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 58.15
Std Dev 8.161
Entry
ampl
0
2
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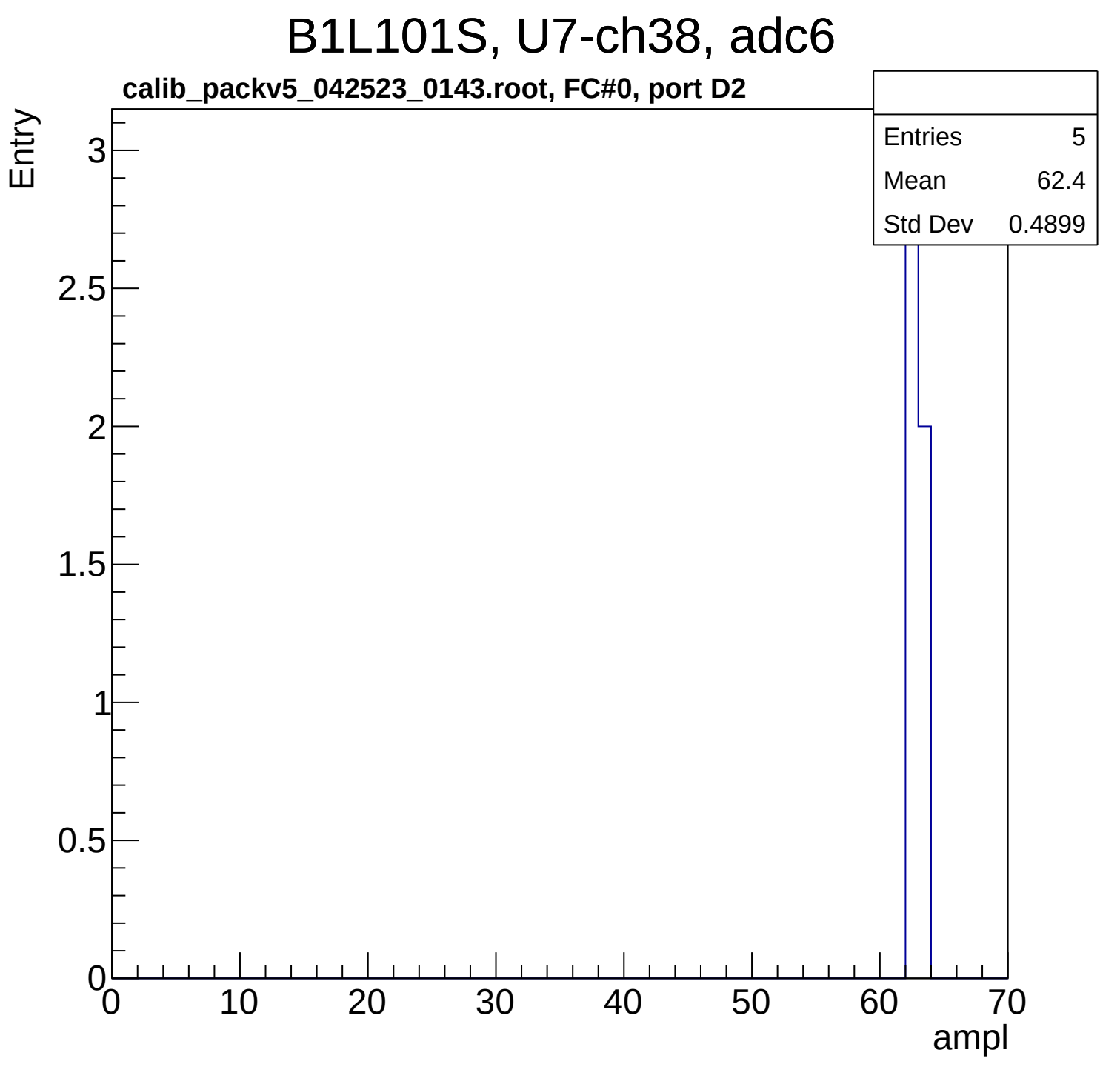
B1L101S, U7-ch38, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 62.4
Std Dev 0.4899
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
50
60
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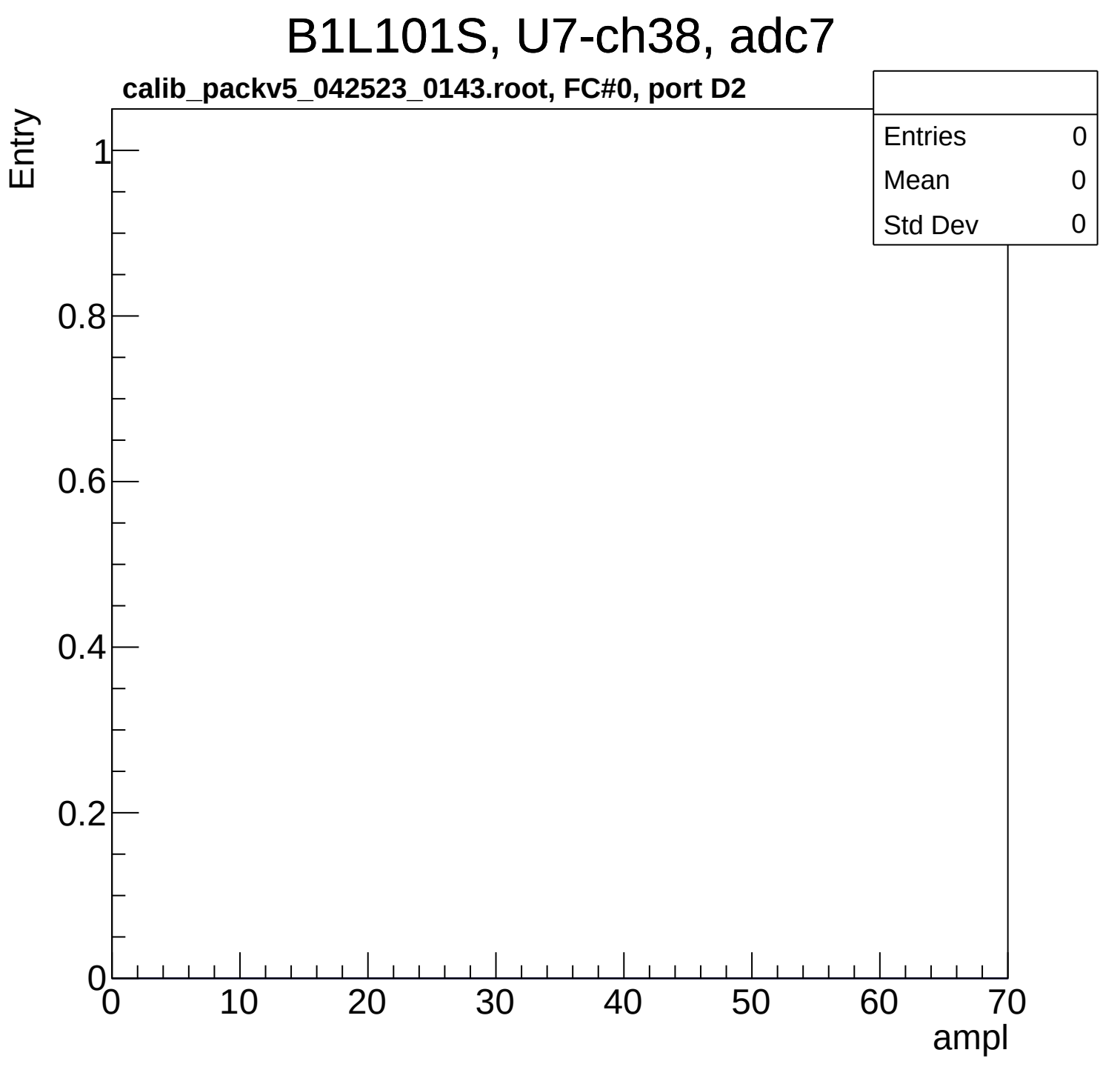
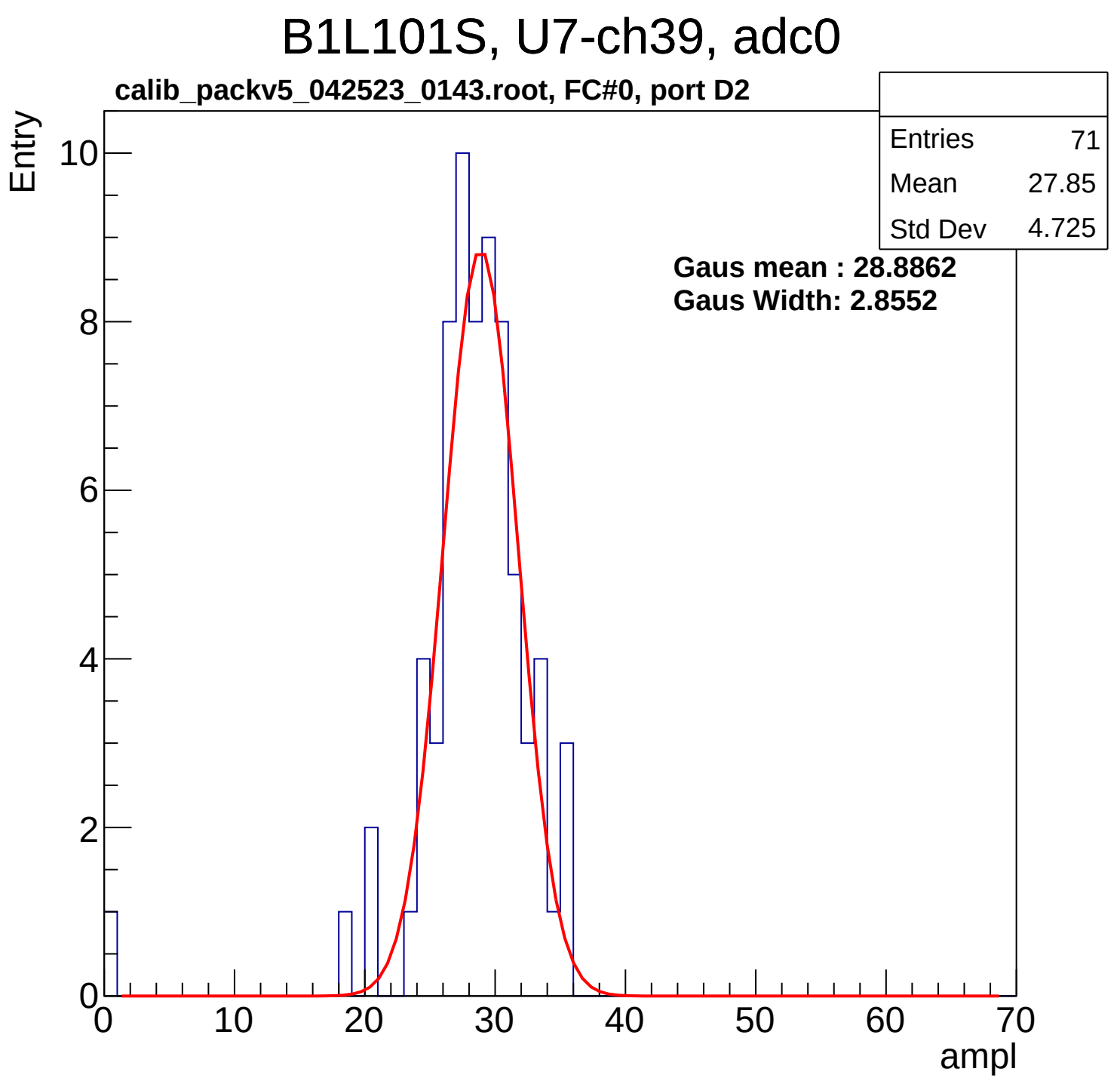

B1L101S, U7-ch38, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch39, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 27.85
Std Dev 4.725
Gaus mean : 28.8862
Gaus Width: 2.8552
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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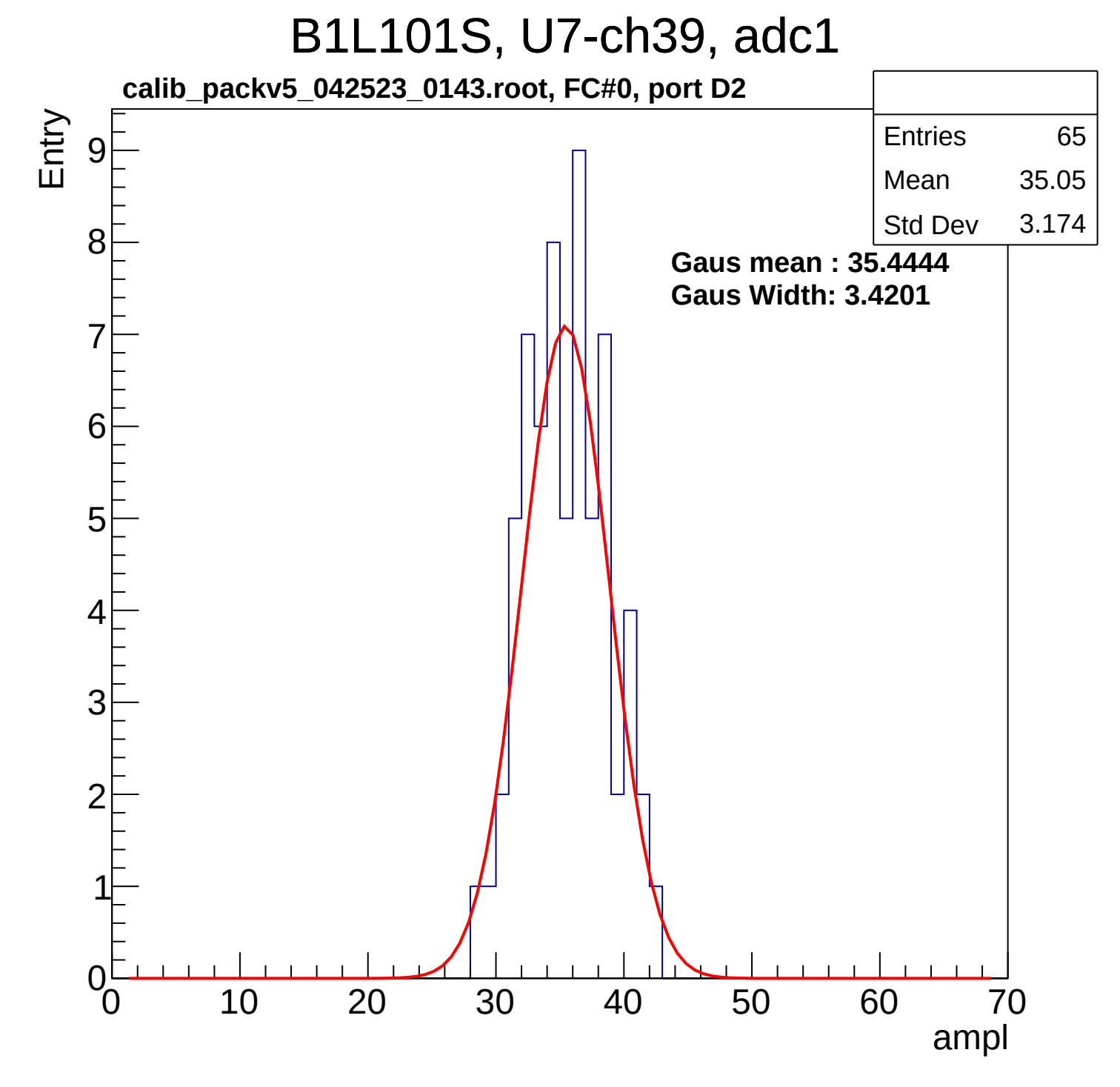
B1L101S, U7-ch39, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 35.05
Std Dev 3.174
Gaus mean : 35.4444
Gaus Width: 3.4201
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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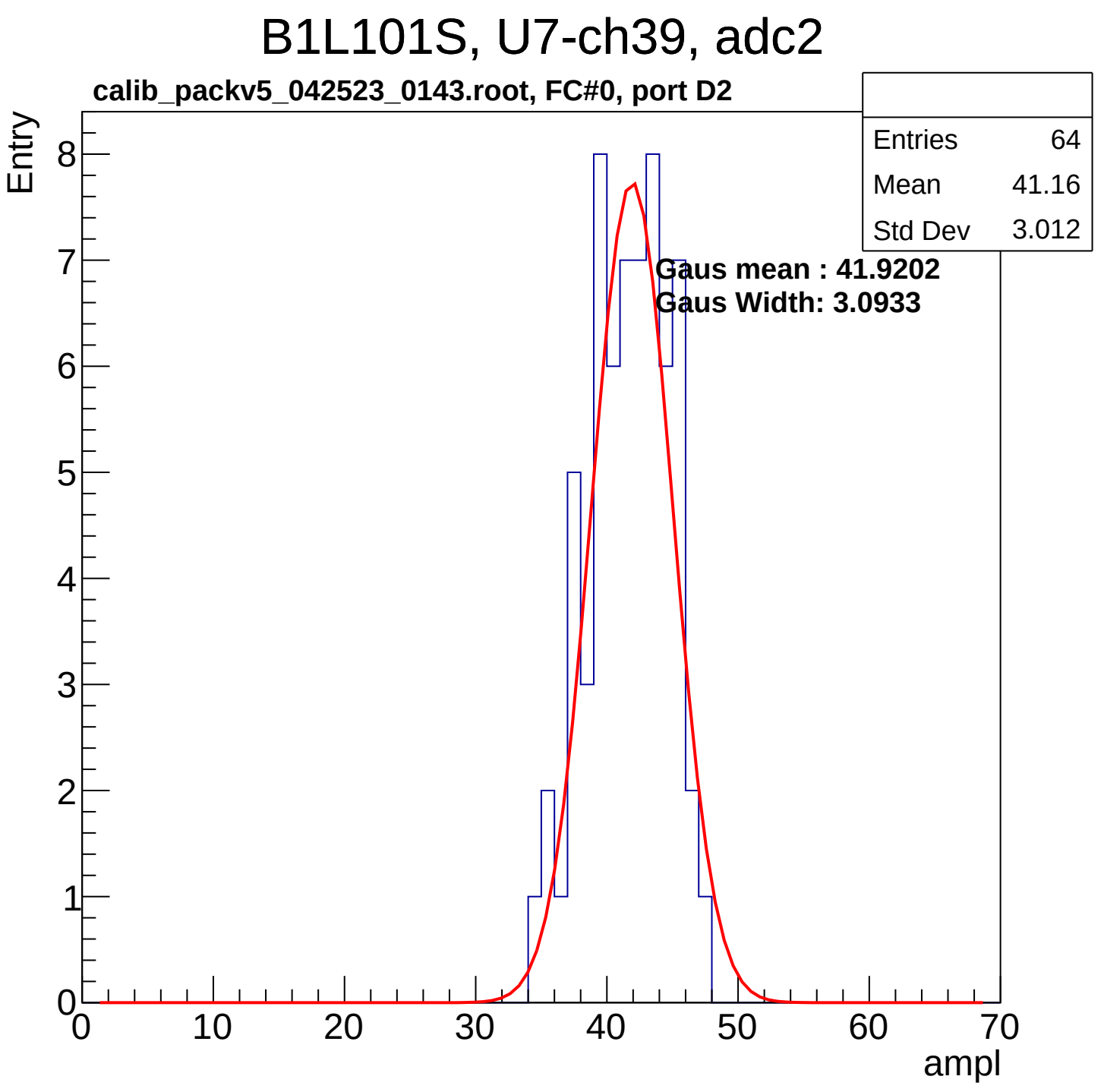
B1L101S, U7-ch39, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 41.16
Std Dev 3.012
Gaus mean : 41.9202
Gaus Width: 3.0933
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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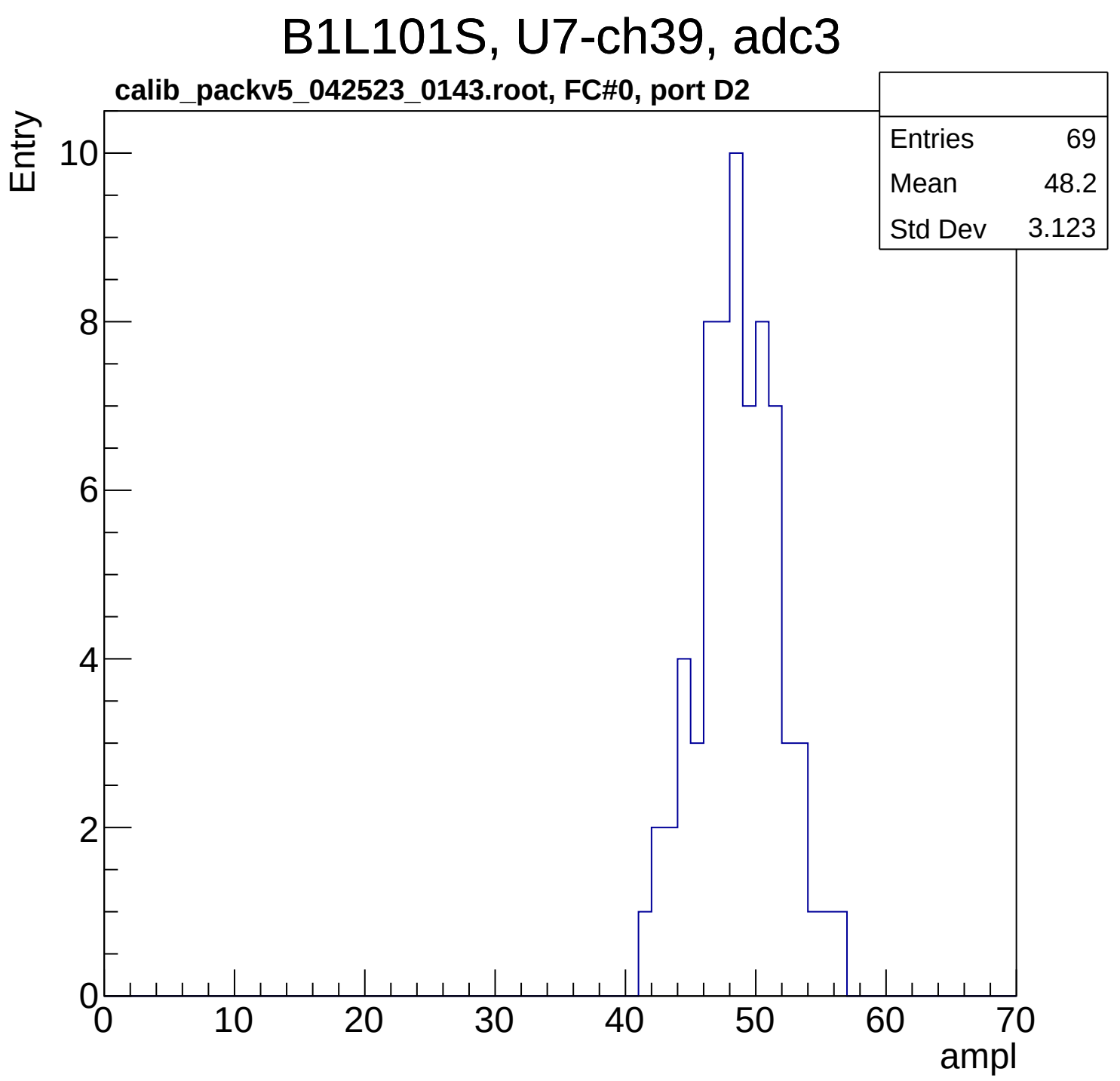
B1L101S, U7-ch39, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 48.2
Std Dev 3.123
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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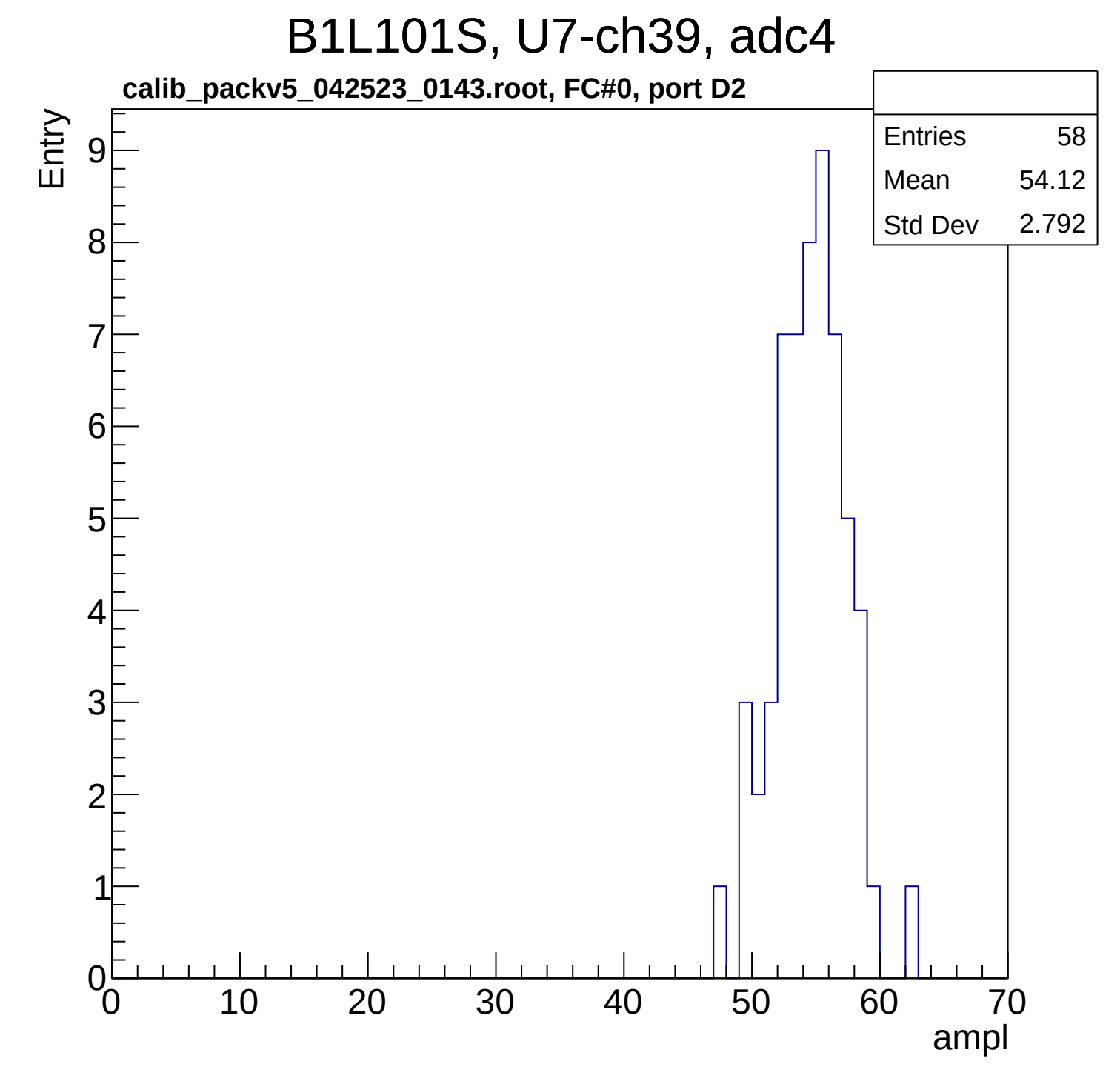
B1L101S, U7-ch39, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 54.12
Std Dev 2.792
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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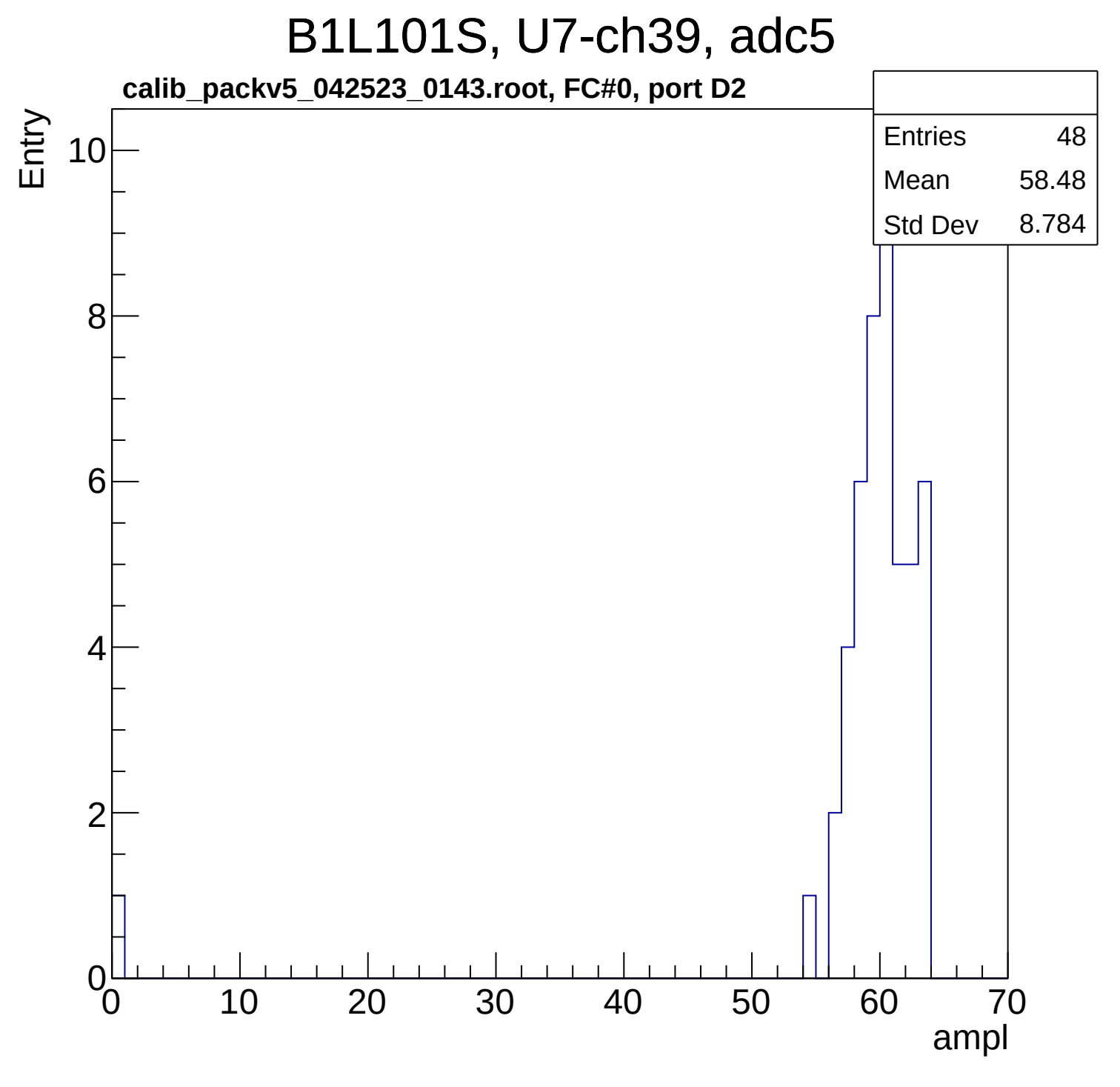
B1L101S, U7-ch39, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 58.48
Std Dev 8.784
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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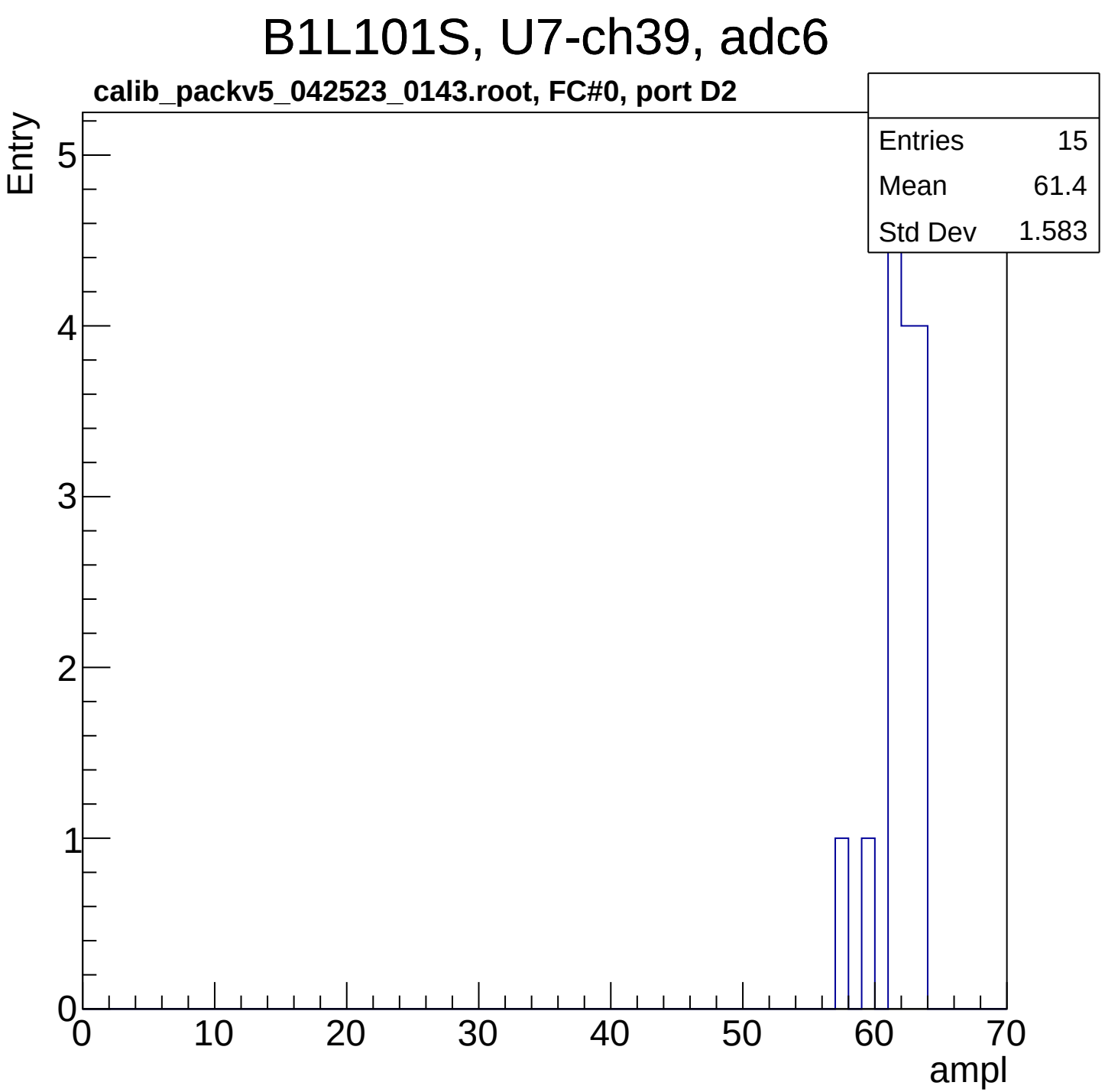
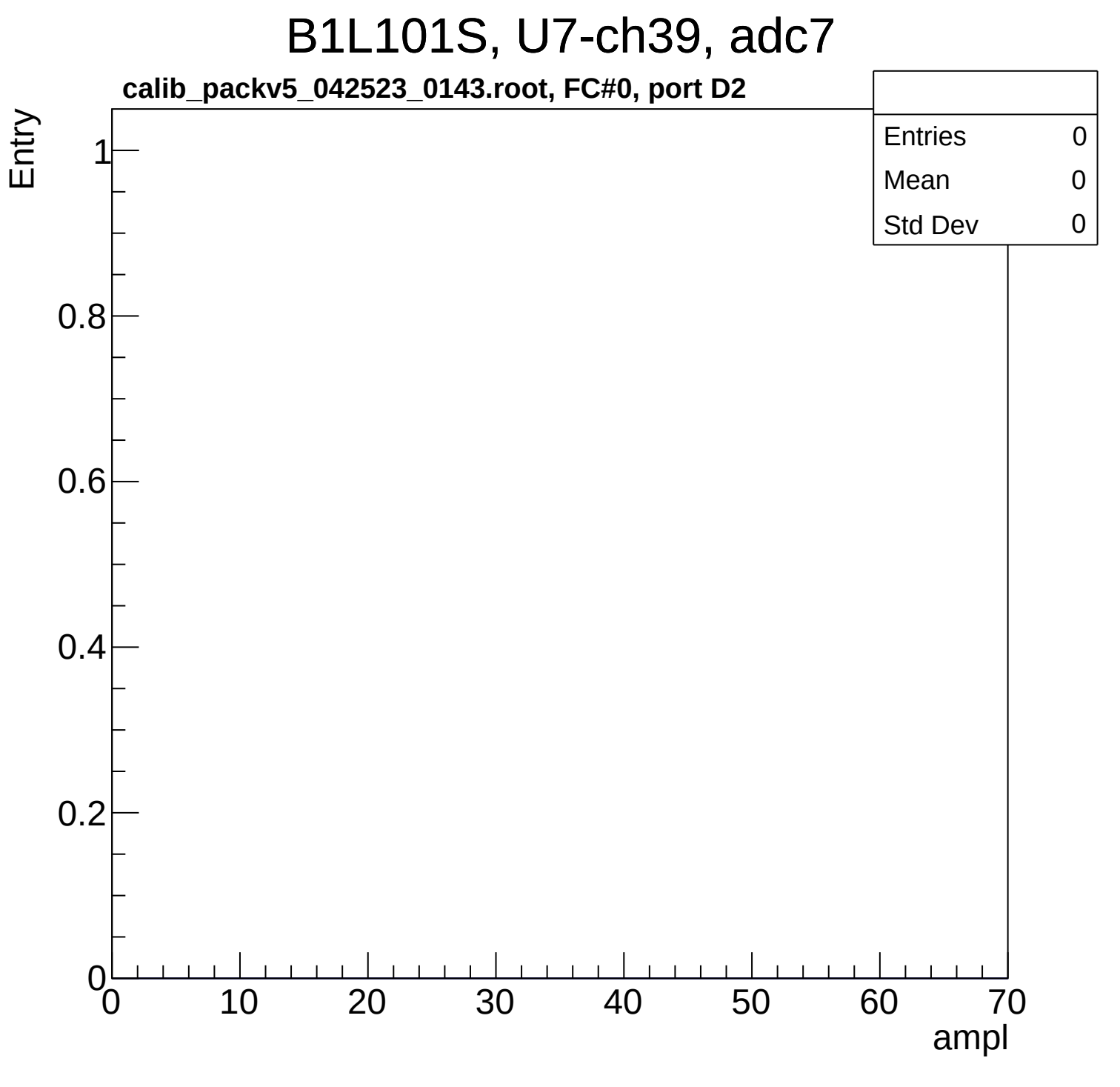
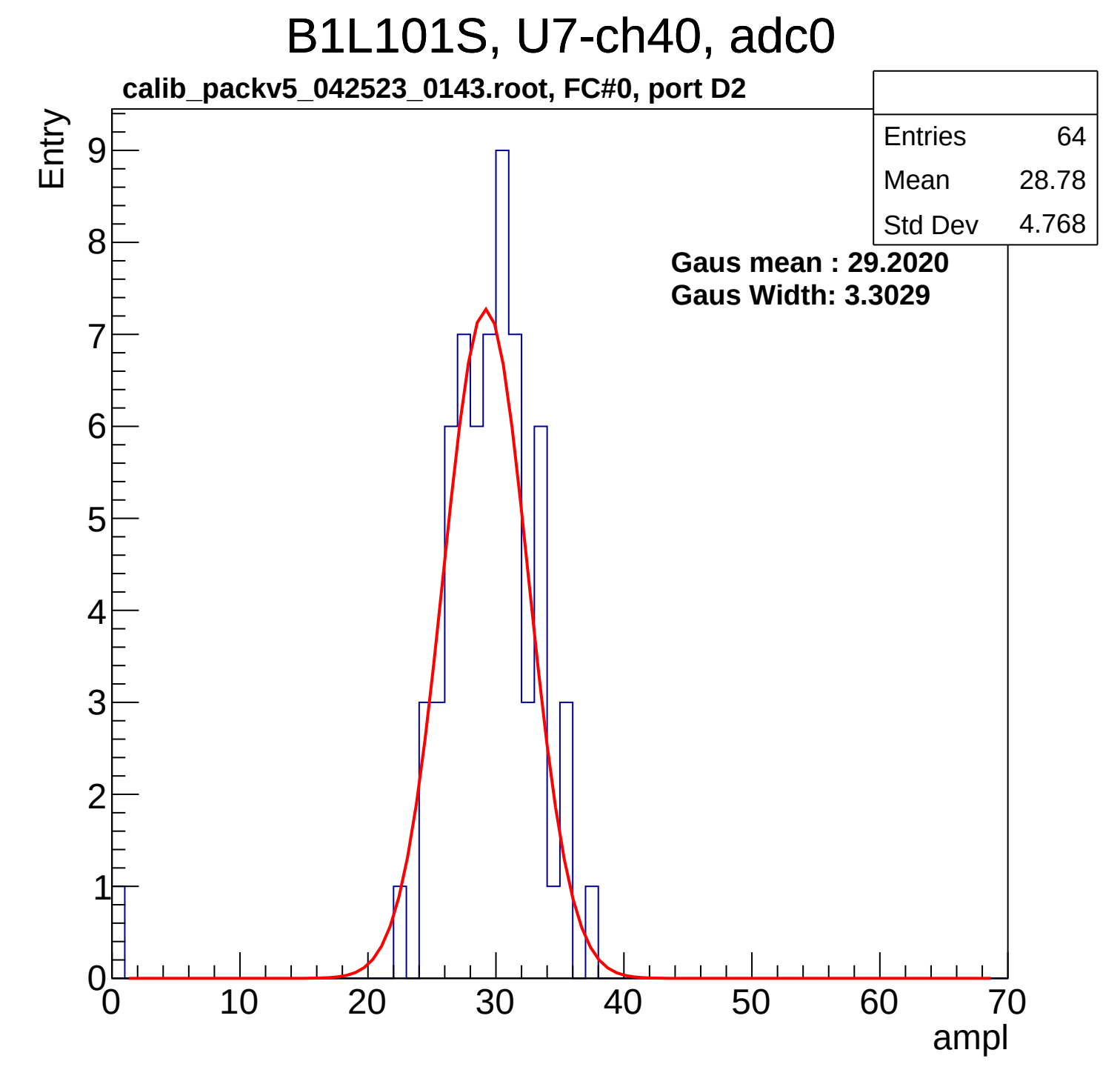

B1L101S, U7-ch39, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 15
Mean 61.4
Std Dev 1.583
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L101S, U7-ch39, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch40, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 28.78
Std Dev 4.768
Gaus mean : 29.2020
Gaus Width: 3.3029
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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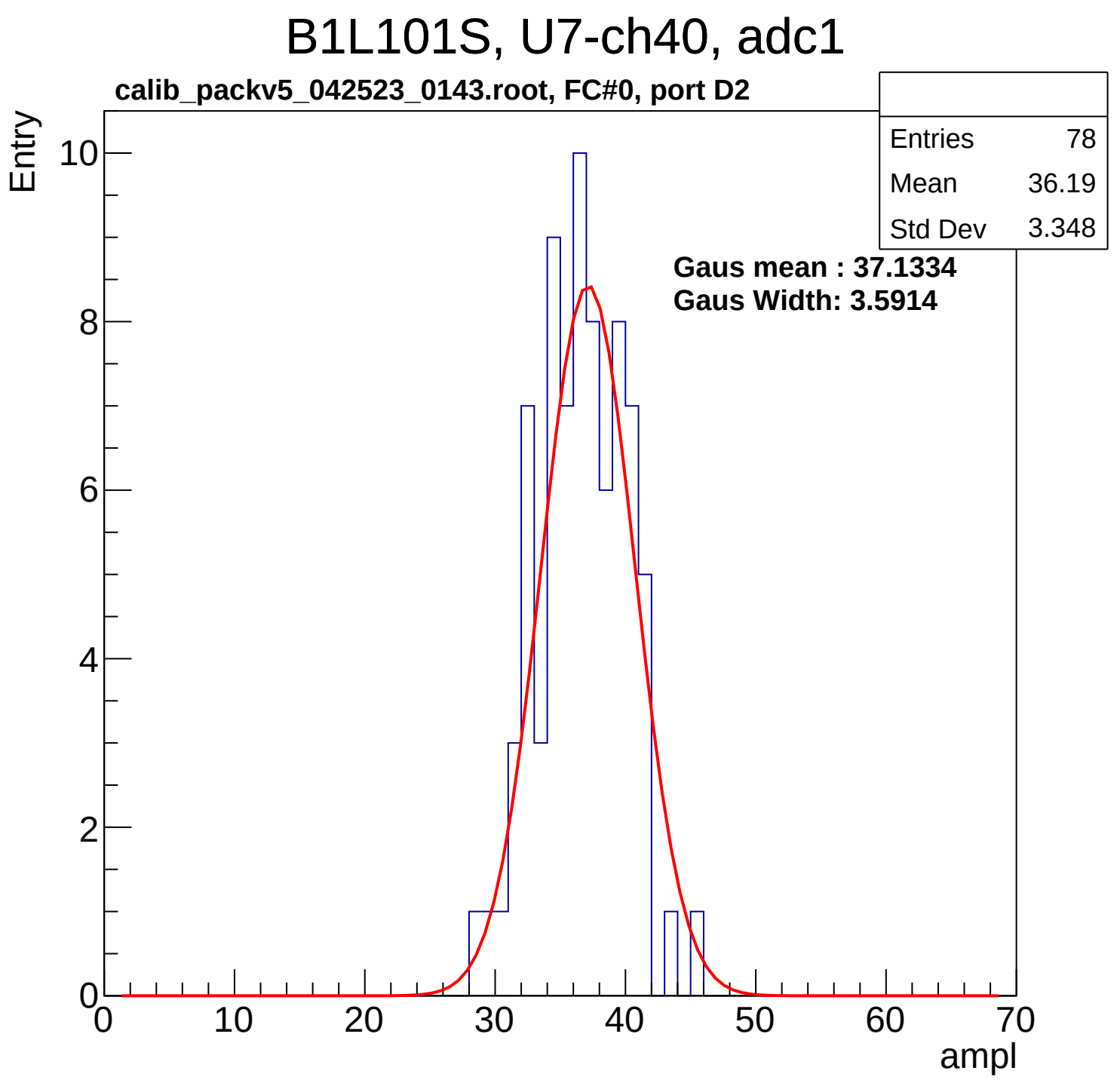
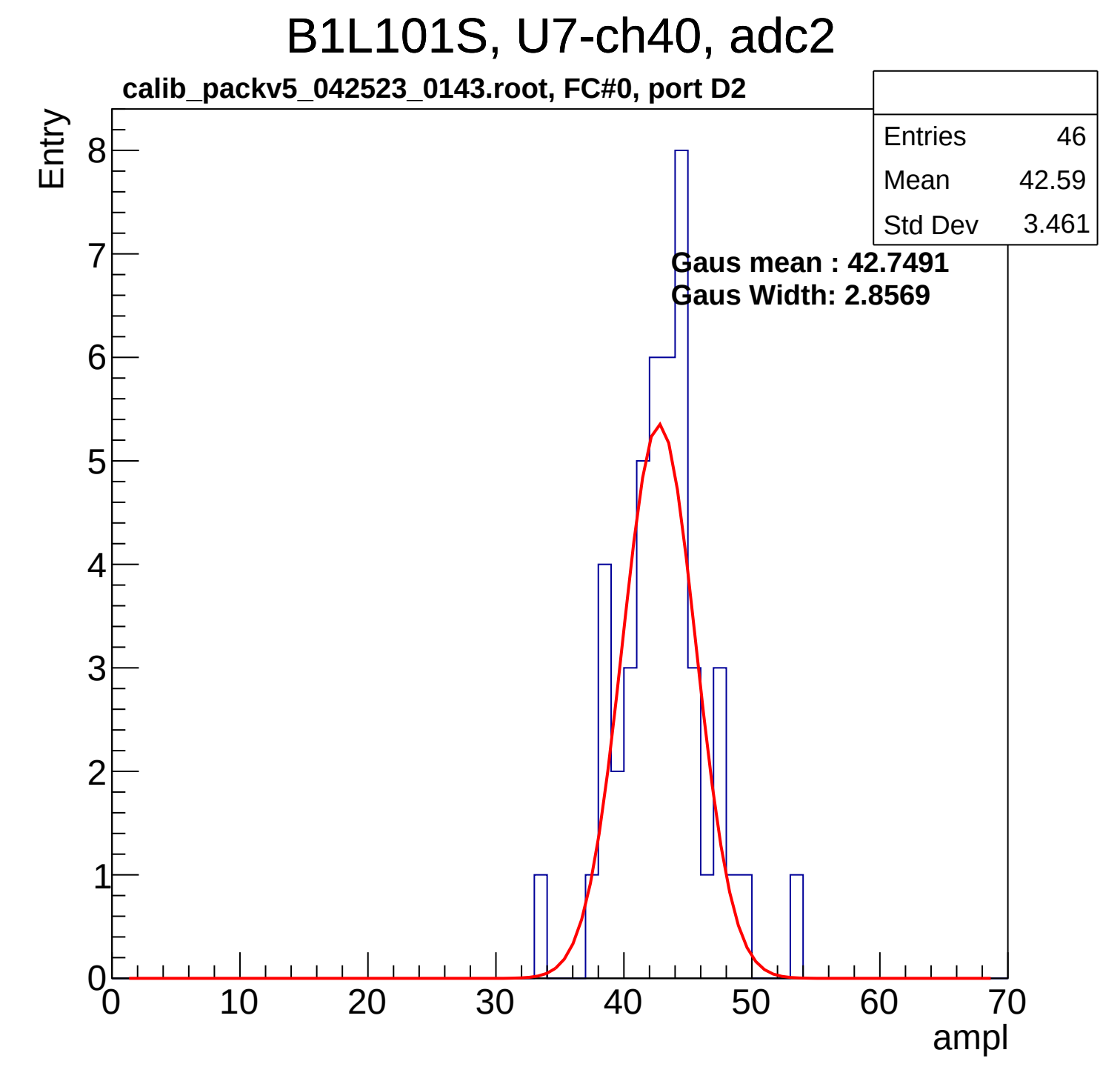

B1L101S, U7-ch40, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 36.19
Std Dev 3.348
Gaus mean : 37.1334
Gaus Width: 3.5914
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch40, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 42.59
Std Dev 3.461
Gaus mean : 42.7491
Gaus Width: 2.8569
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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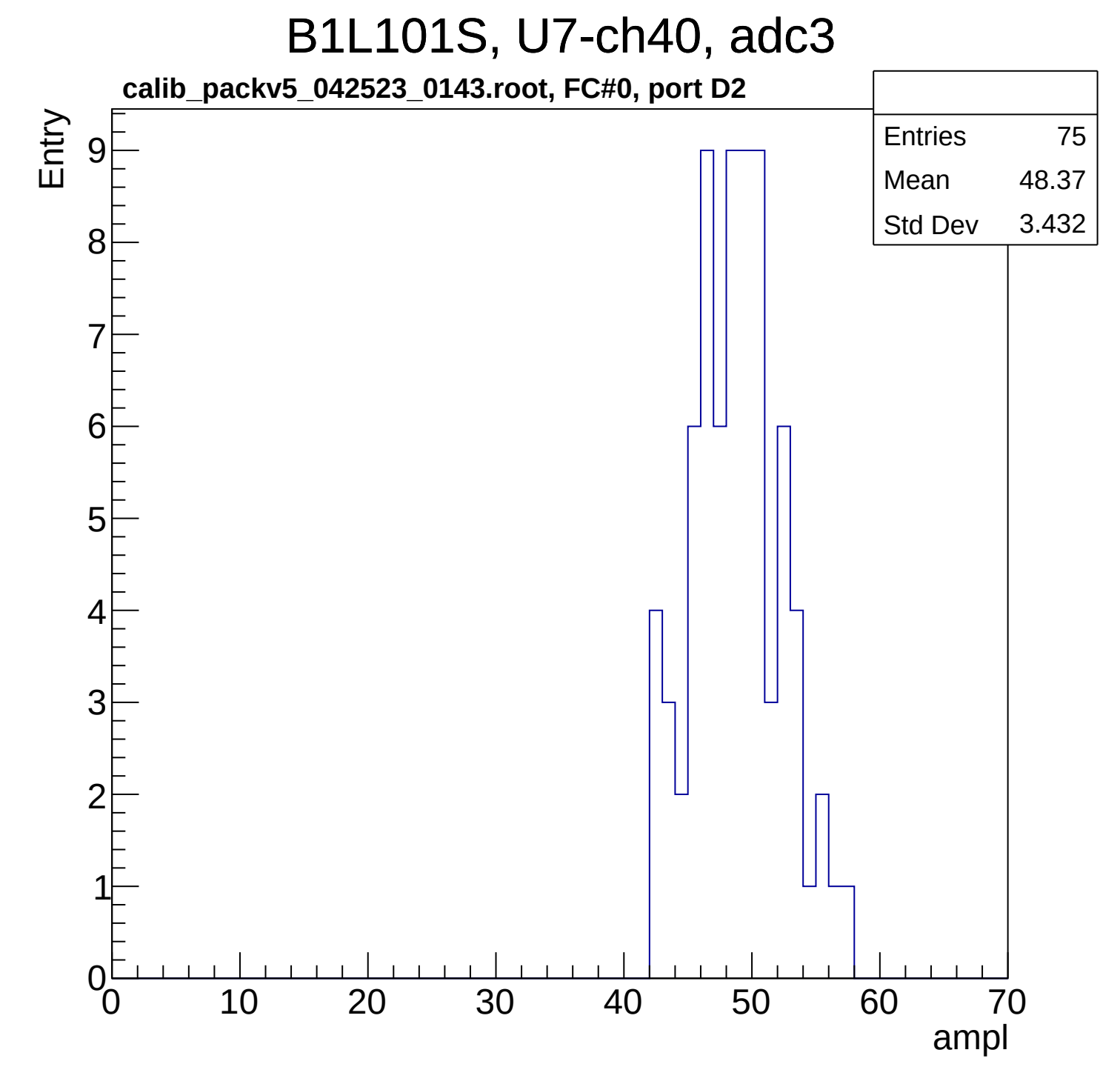
B1L101S, U7-ch40, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 48.37
Std Dev 3.432
Entry
ampl
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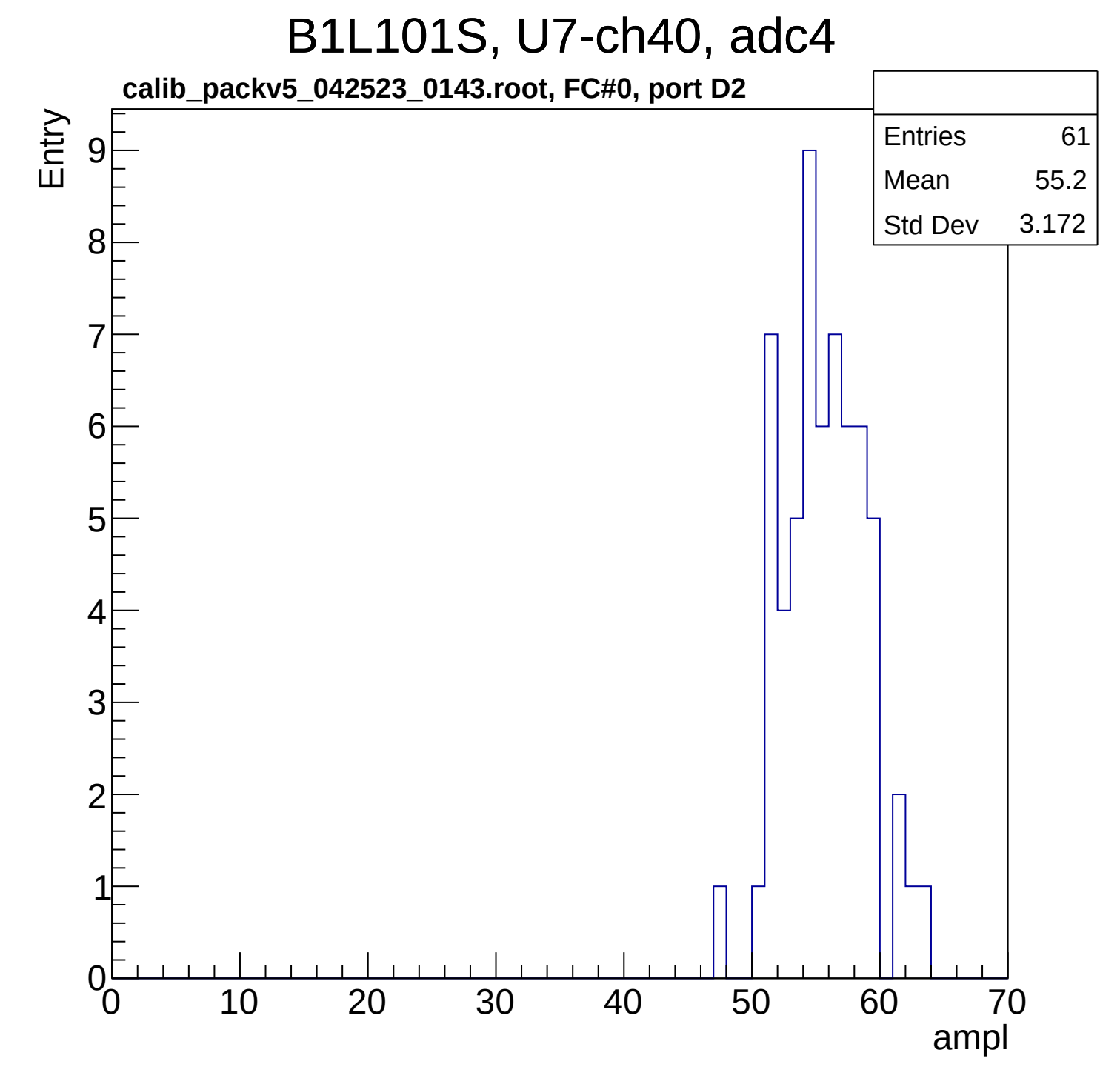
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch40, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 55.2
Std Dev 3.172
Entry
ampl
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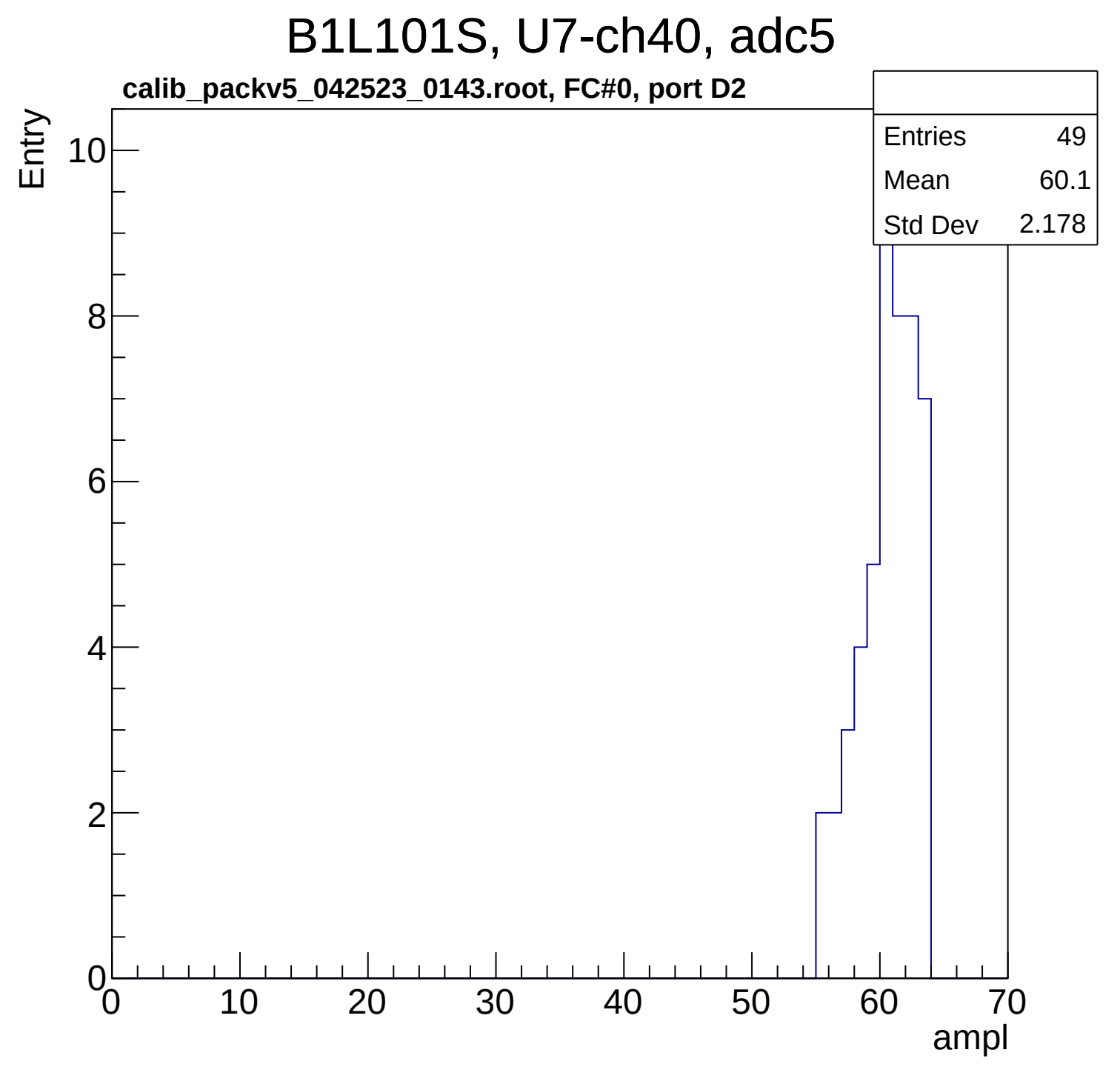
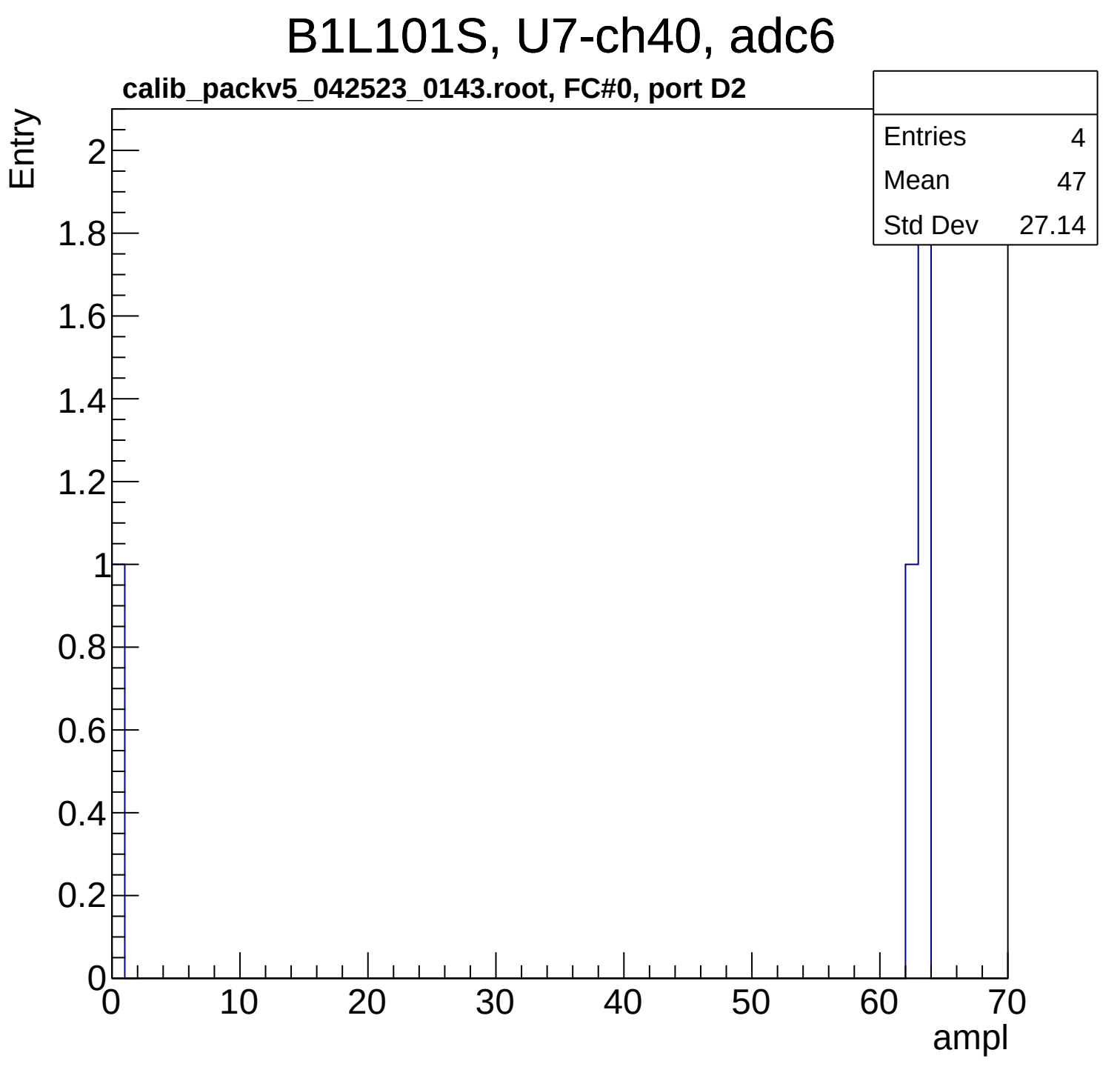
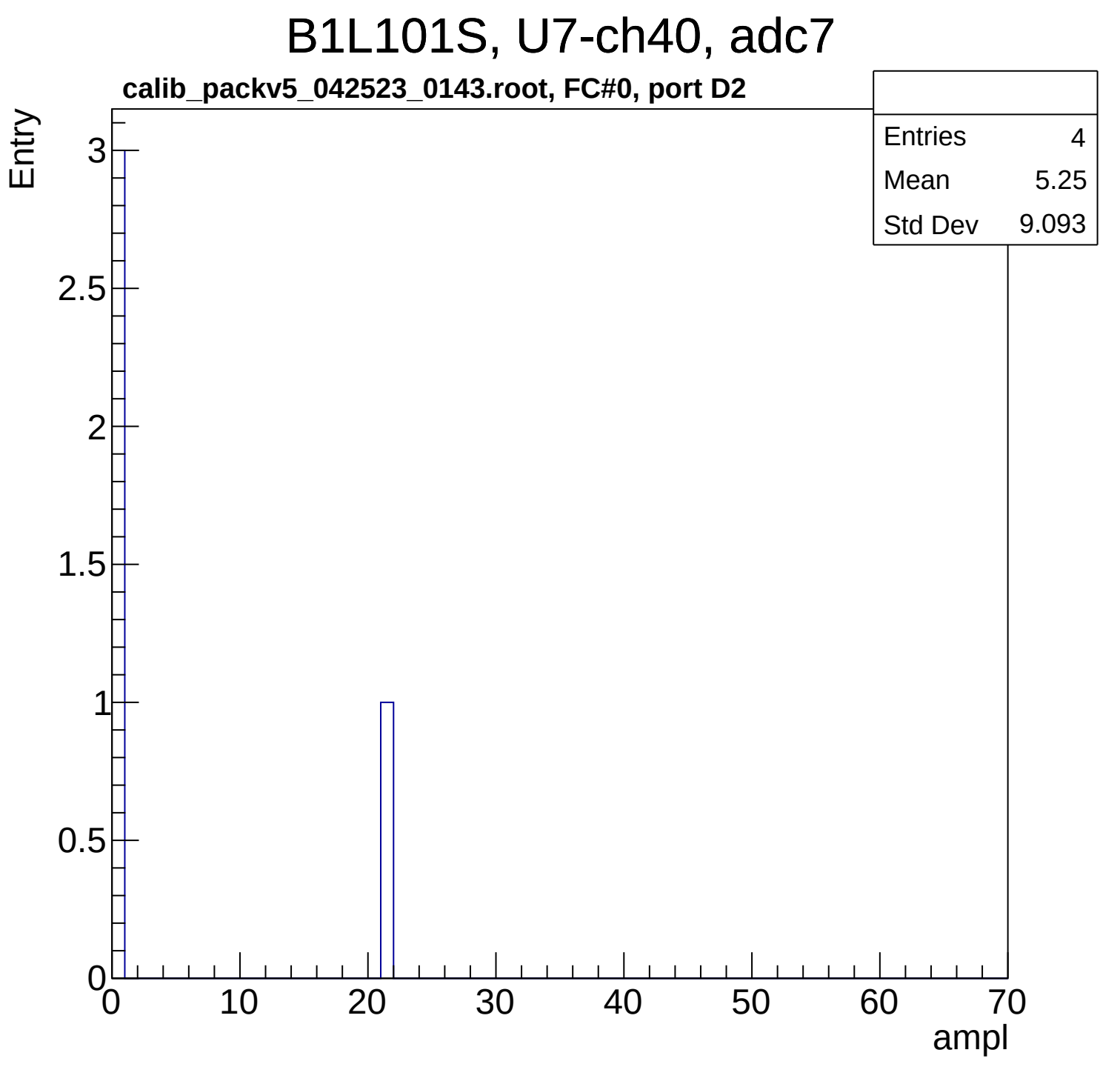
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch40, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 60.1
Std Dev 2.178
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch40, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 47
Std Dev 27.14
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U7-ch40, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 5.25
Std Dev 9.093
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
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60
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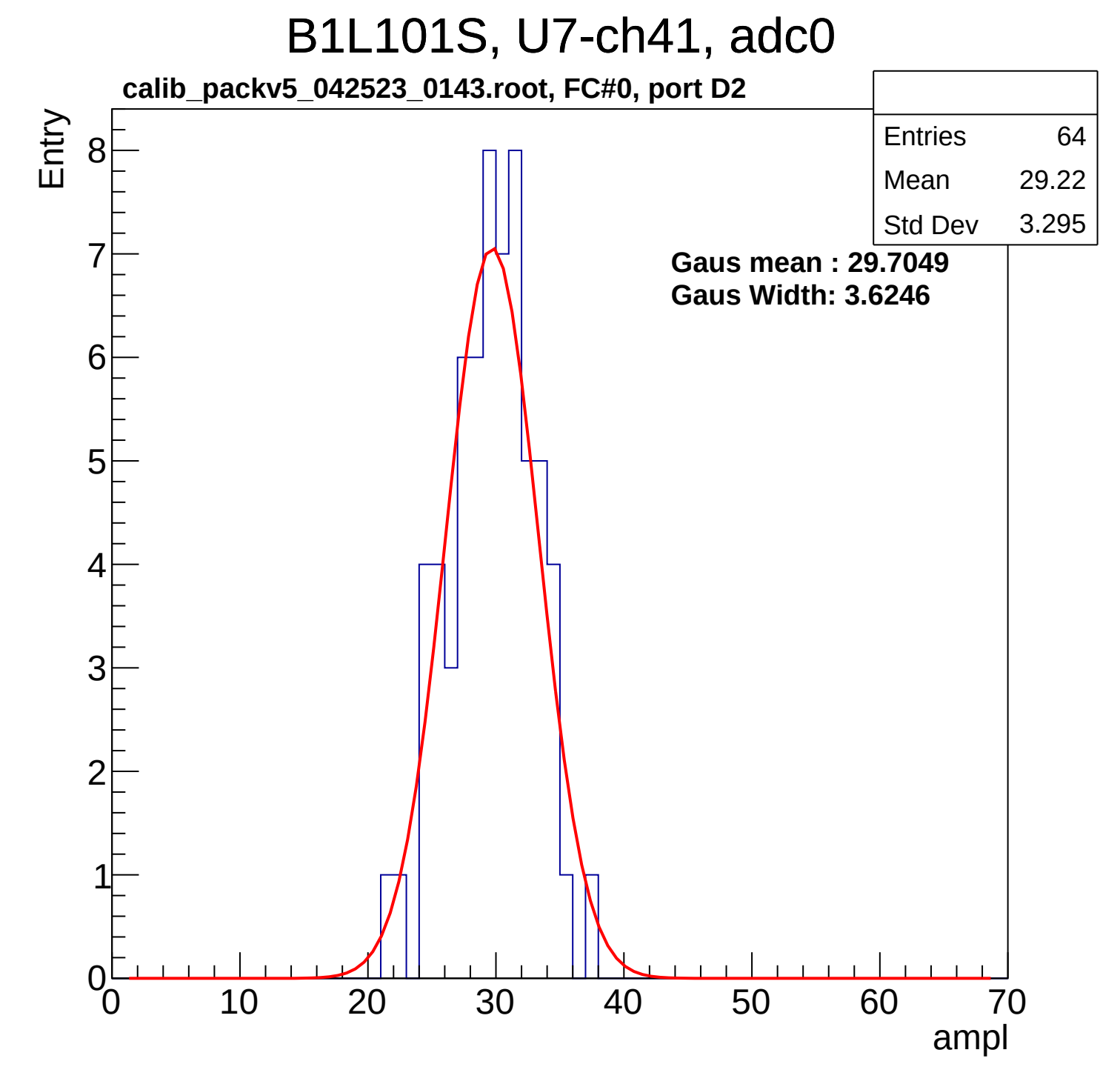
B1L101S, U7-ch41, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 29.22
Std Dev 3.295
Gaus mean : 29.7049
Gaus Width: 3.6246
Entry
ampl
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2
3
4
5
6
7
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0
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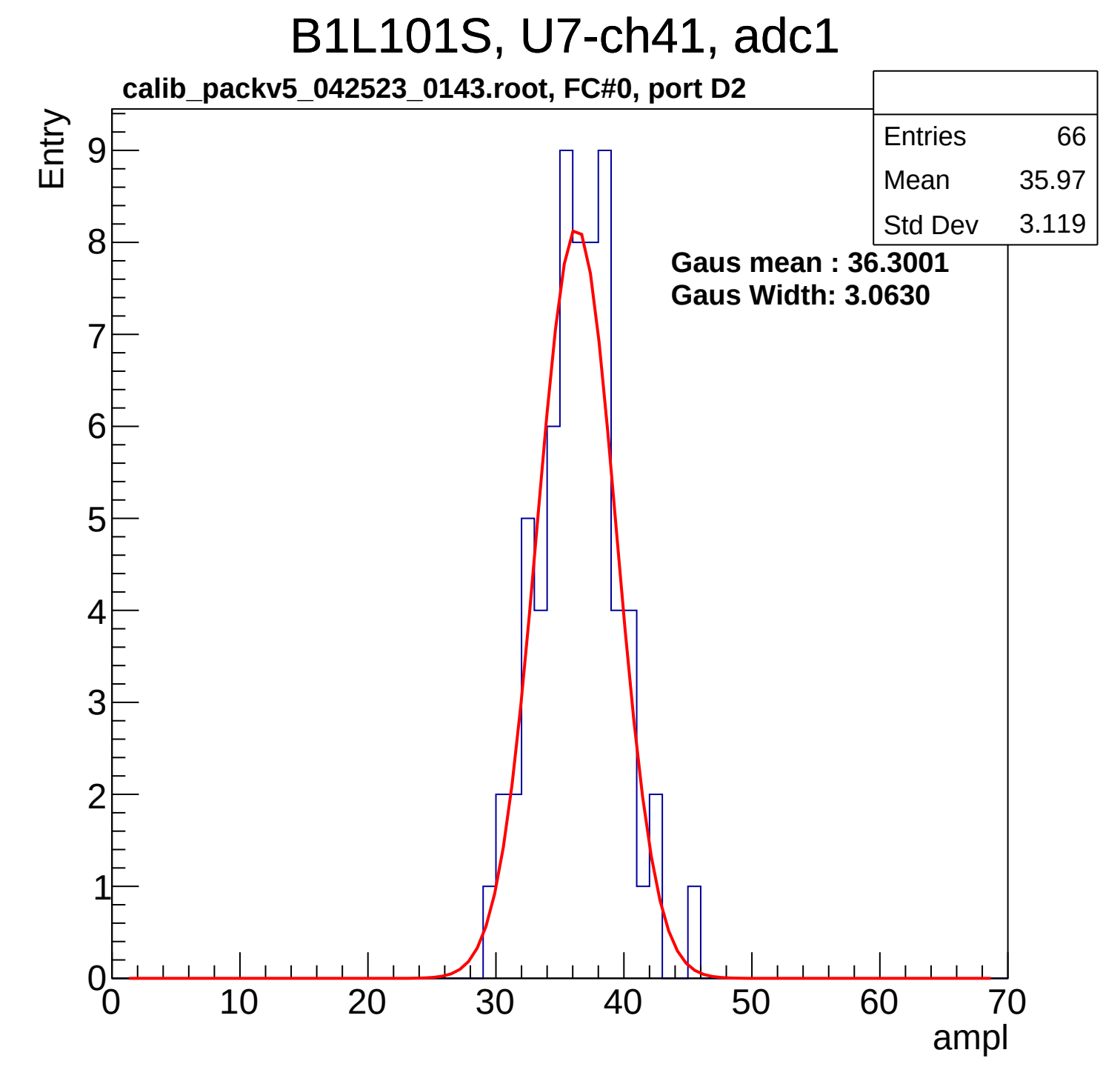
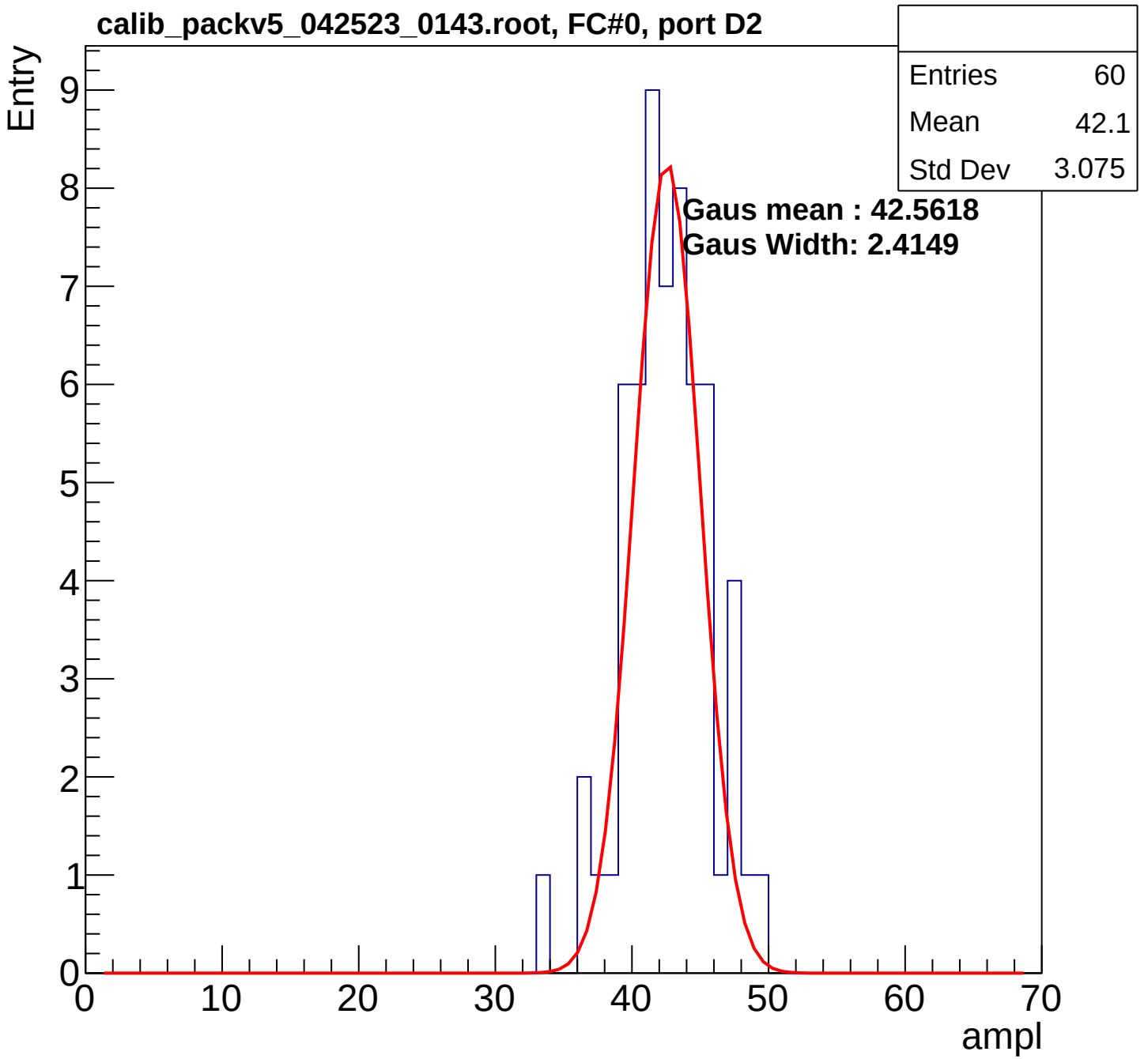
40
50
60
70


B1L101S, U7-ch41, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 35.97
Std Dev 3.119
Gaus mean : 36.3001
Gaus Width: 3.0630
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch41, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 42.1
Std Dev 3.075
Gaus mean : 42.5618
Gaus Width: 2.4149
Entry
ampl
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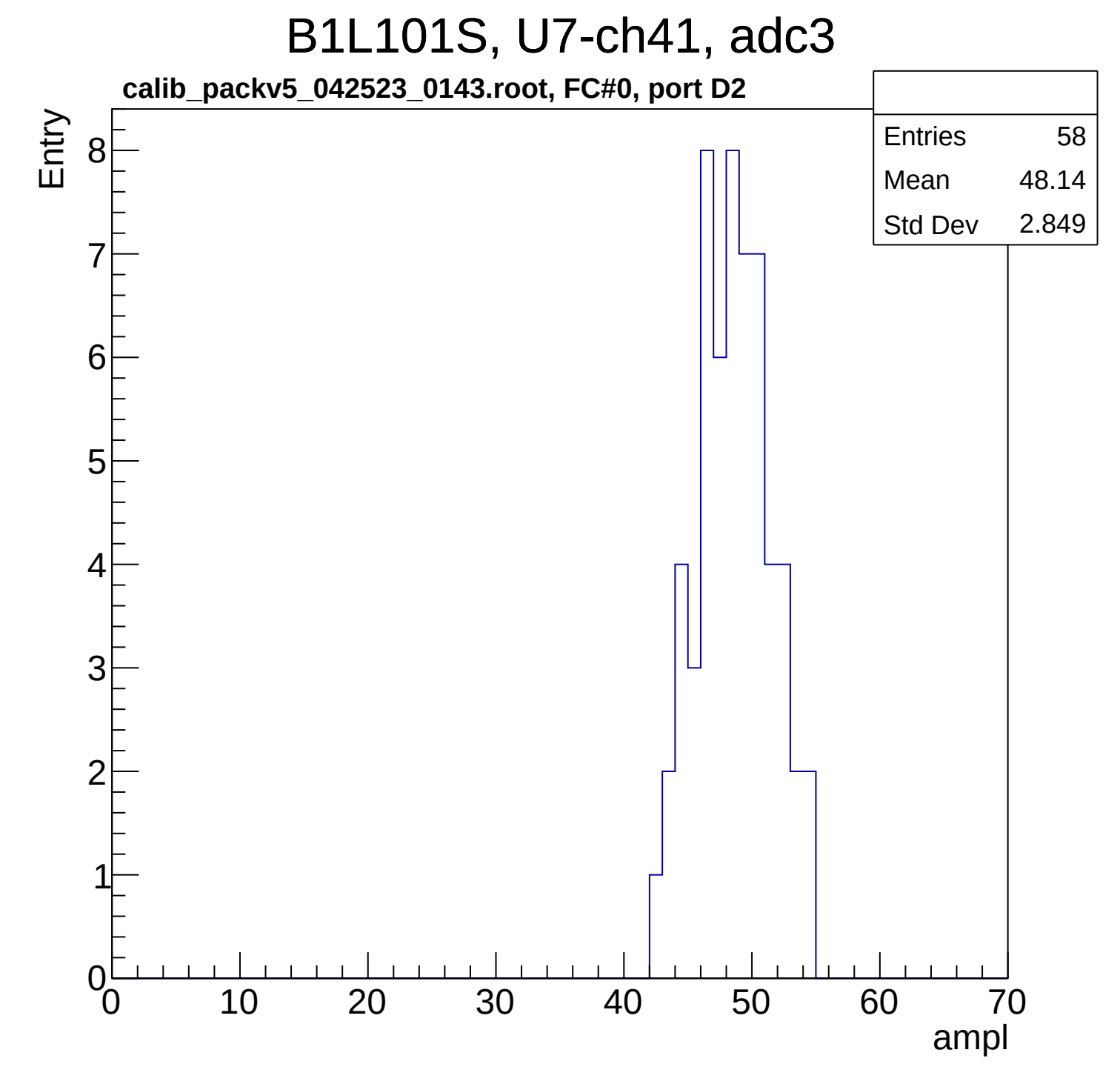
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch41, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 48.14
Std Dev 2.849
Entry
ampl
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5
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7
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0
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60
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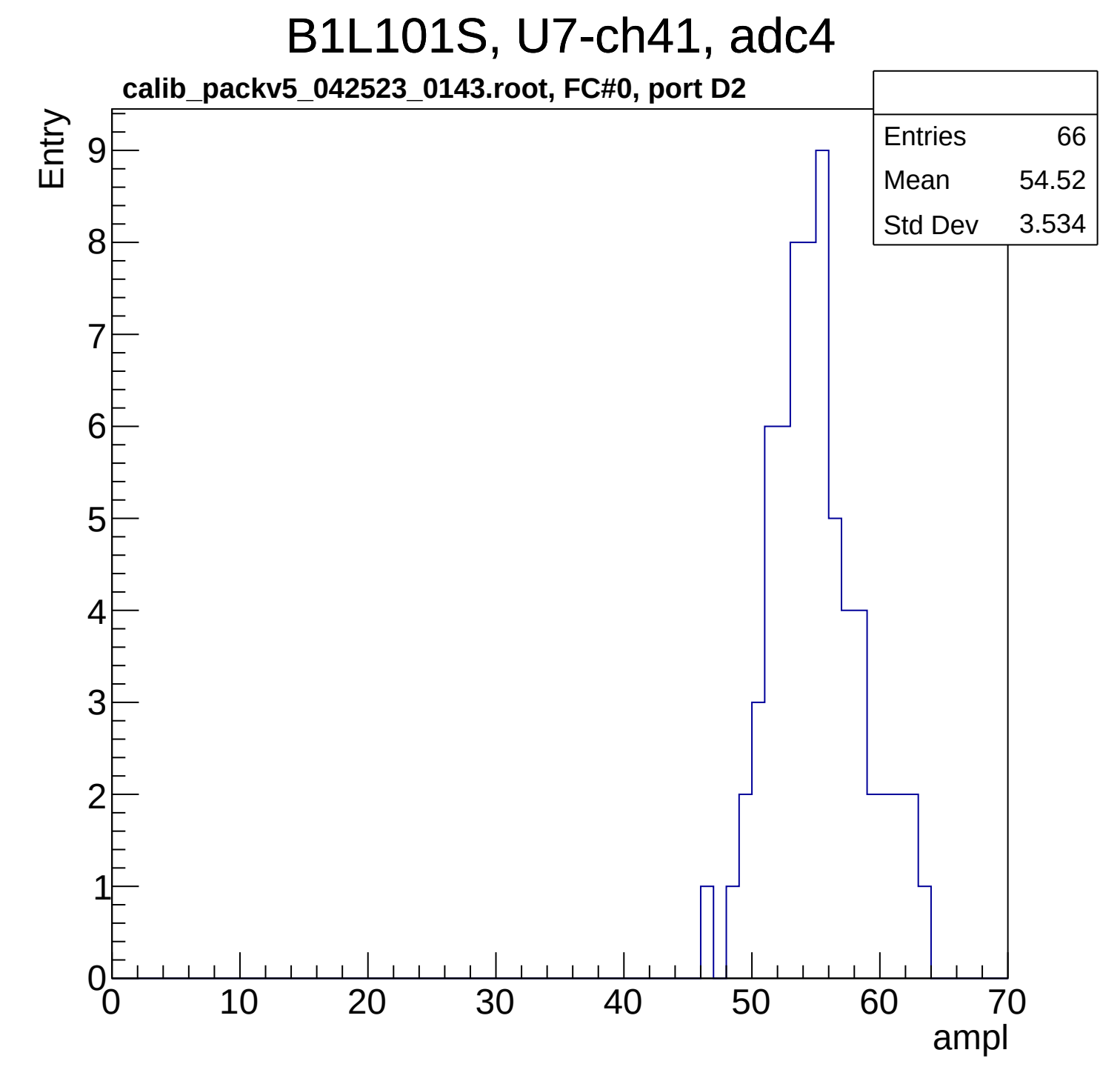
B1L101S, U7-ch41, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 54.52
Std Dev 3.534
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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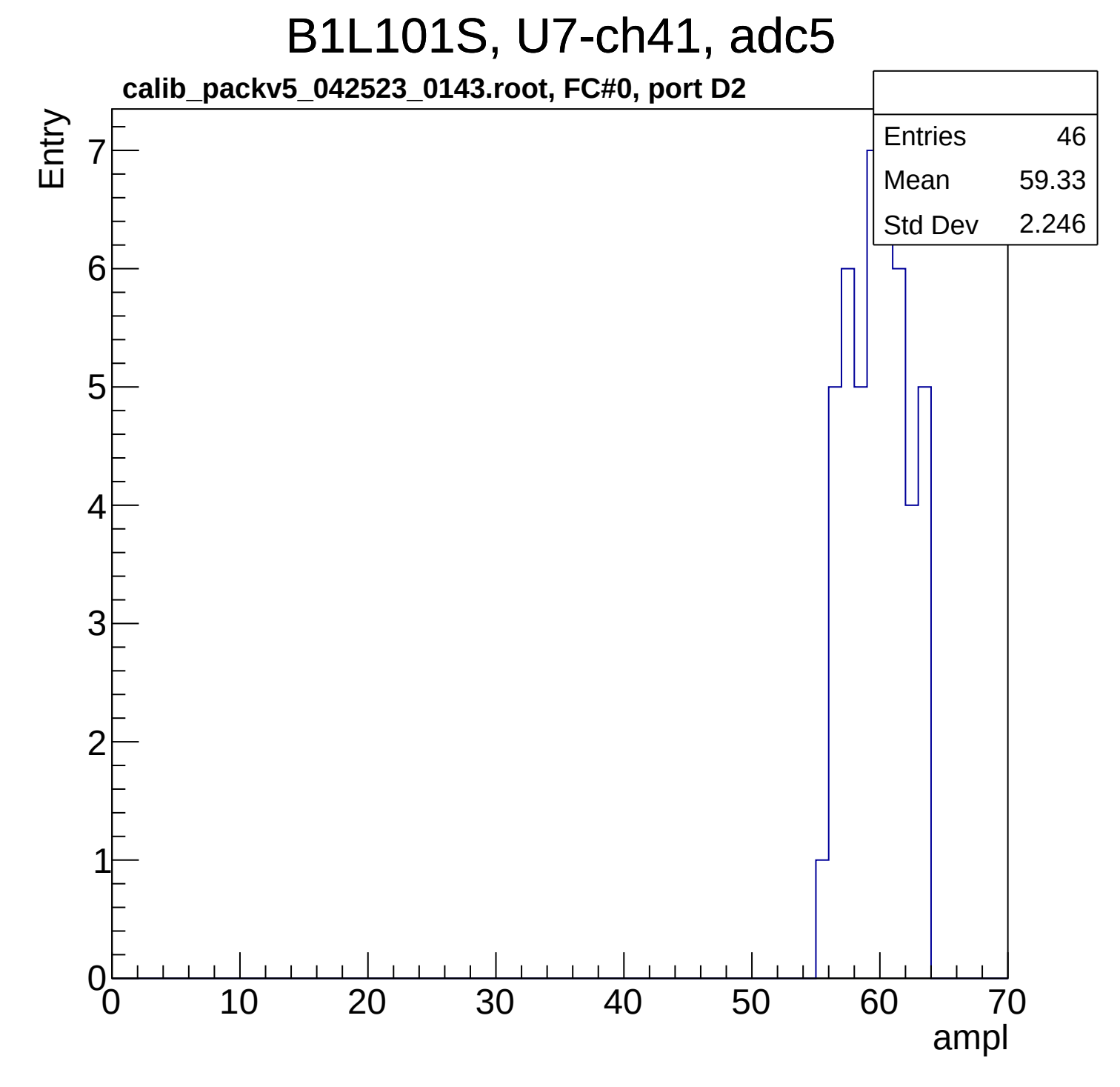
B1L101S, U7-ch41, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 59.33
Std Dev 2.246
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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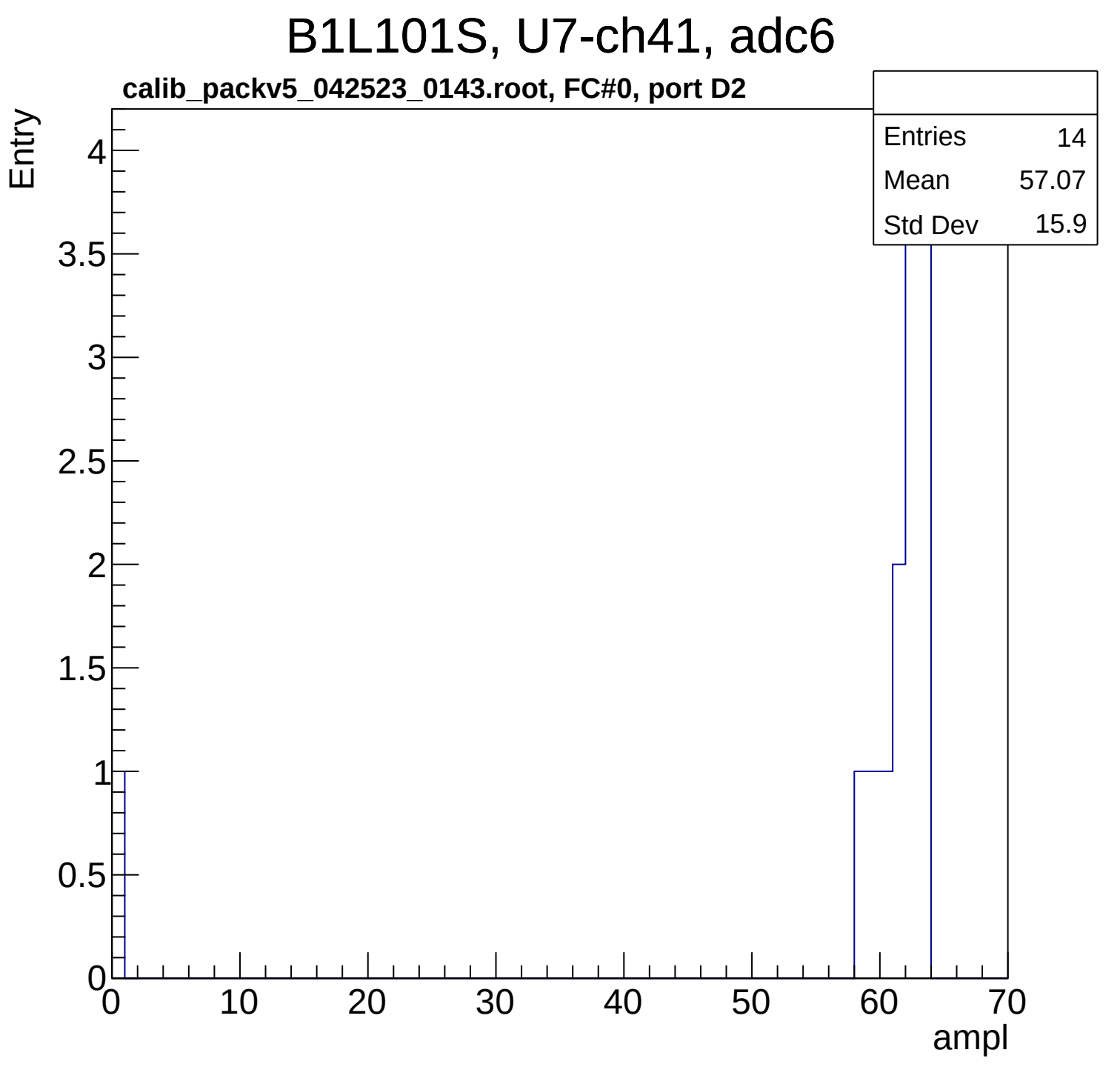
B1L101S, U7-ch41, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 14
Mean 57.07
Std Dev 15.9
Entry
ampl
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0.5
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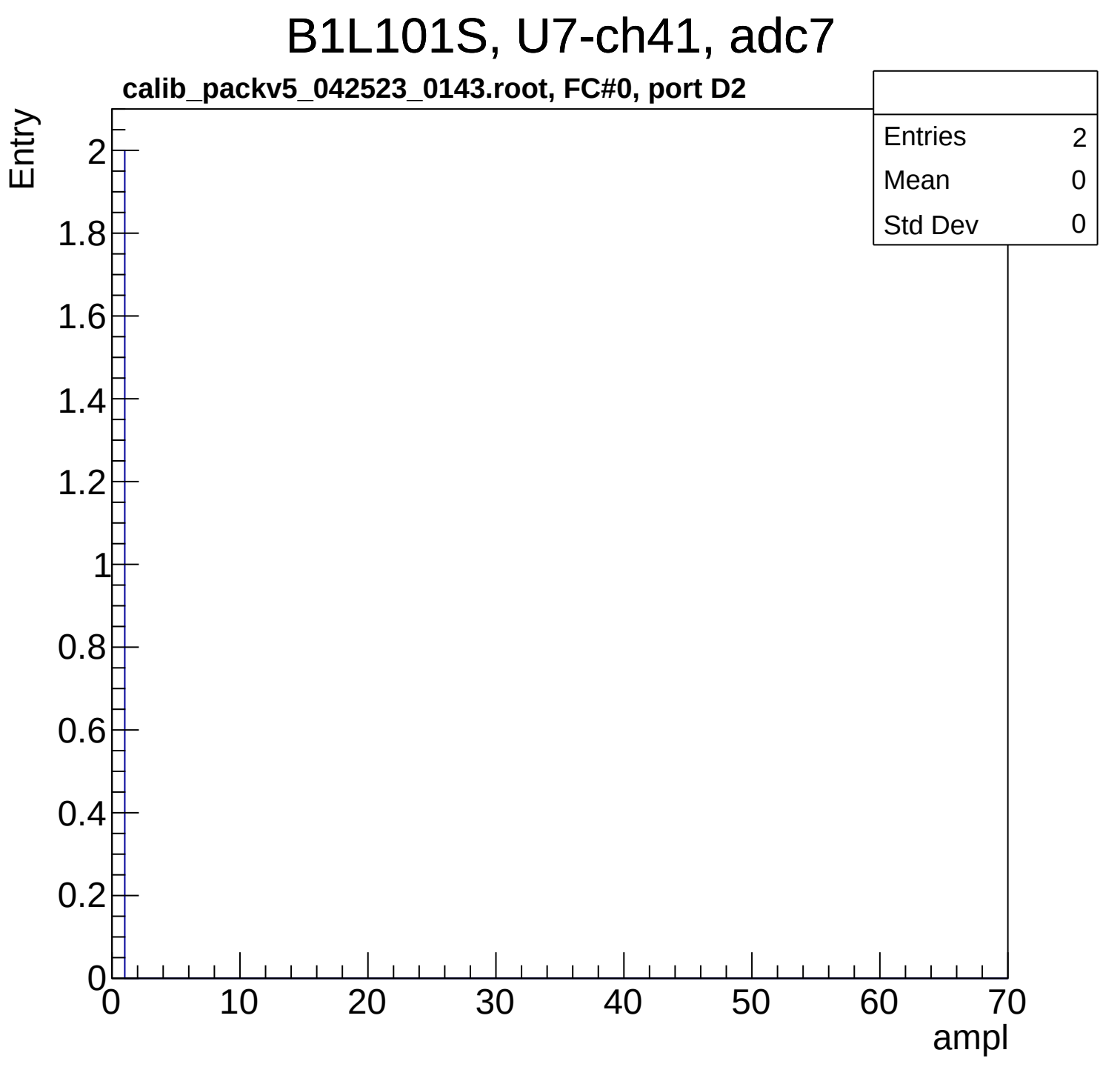
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L101S, U7-ch41, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
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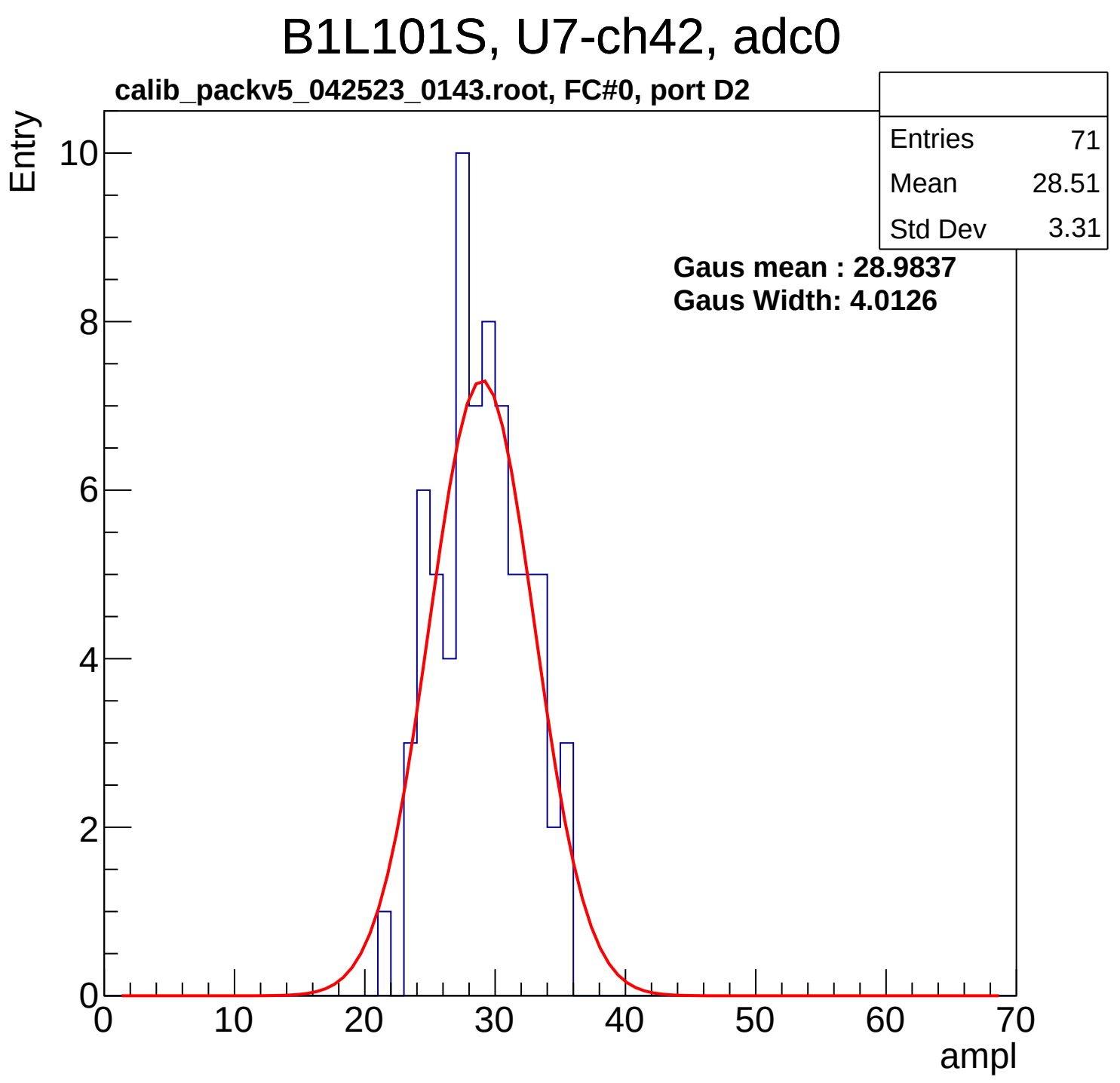
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U7-ch42, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 28.51
Std Dev 3.31
Gaus mean : 28.9837
Gaus Width: 4.0126
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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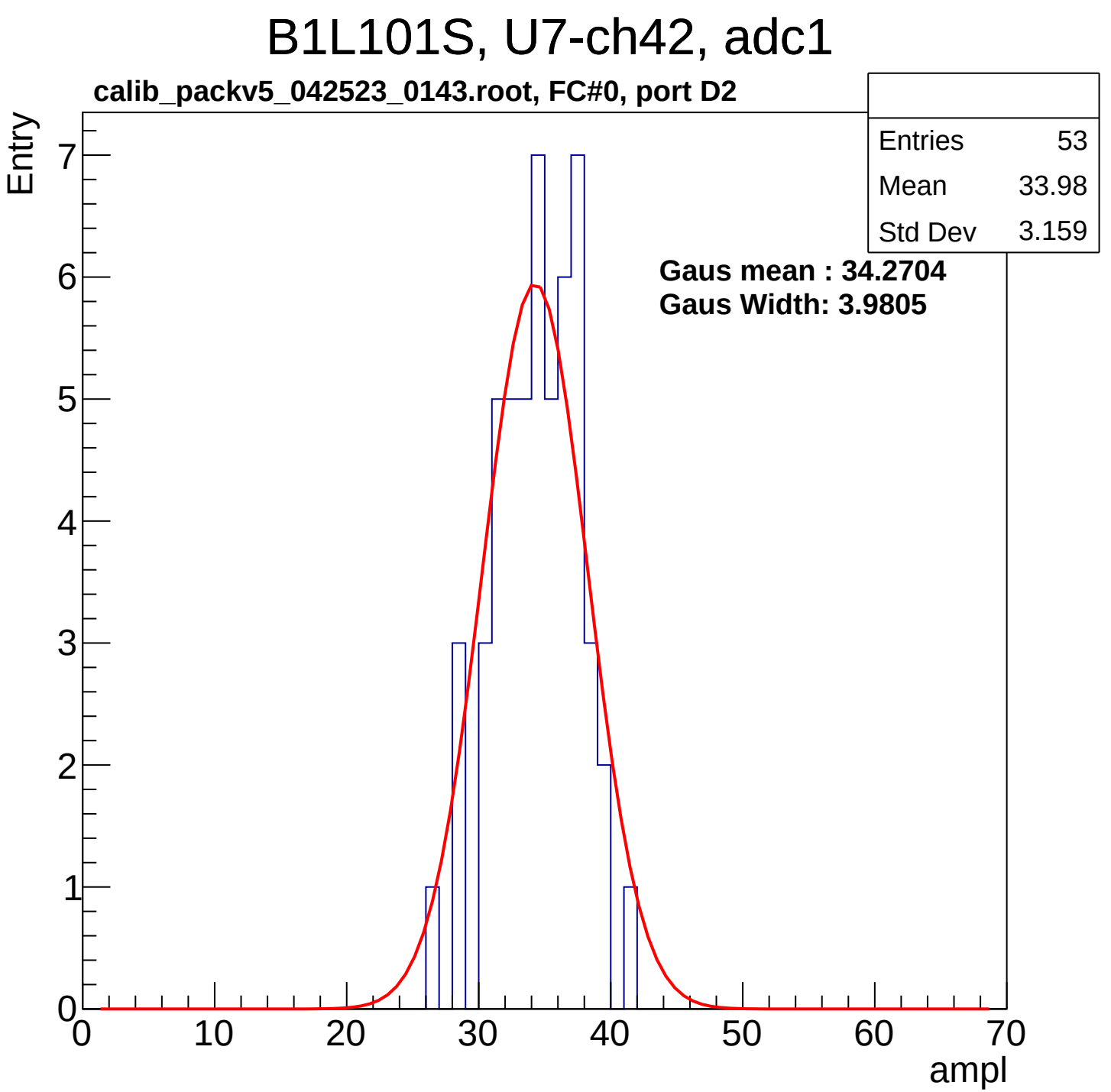
B1L101S, U7-ch42, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 33.98
Std Dev 3.159
Gaus mean : 34.2704
Gaus Width: 3.9805
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
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60
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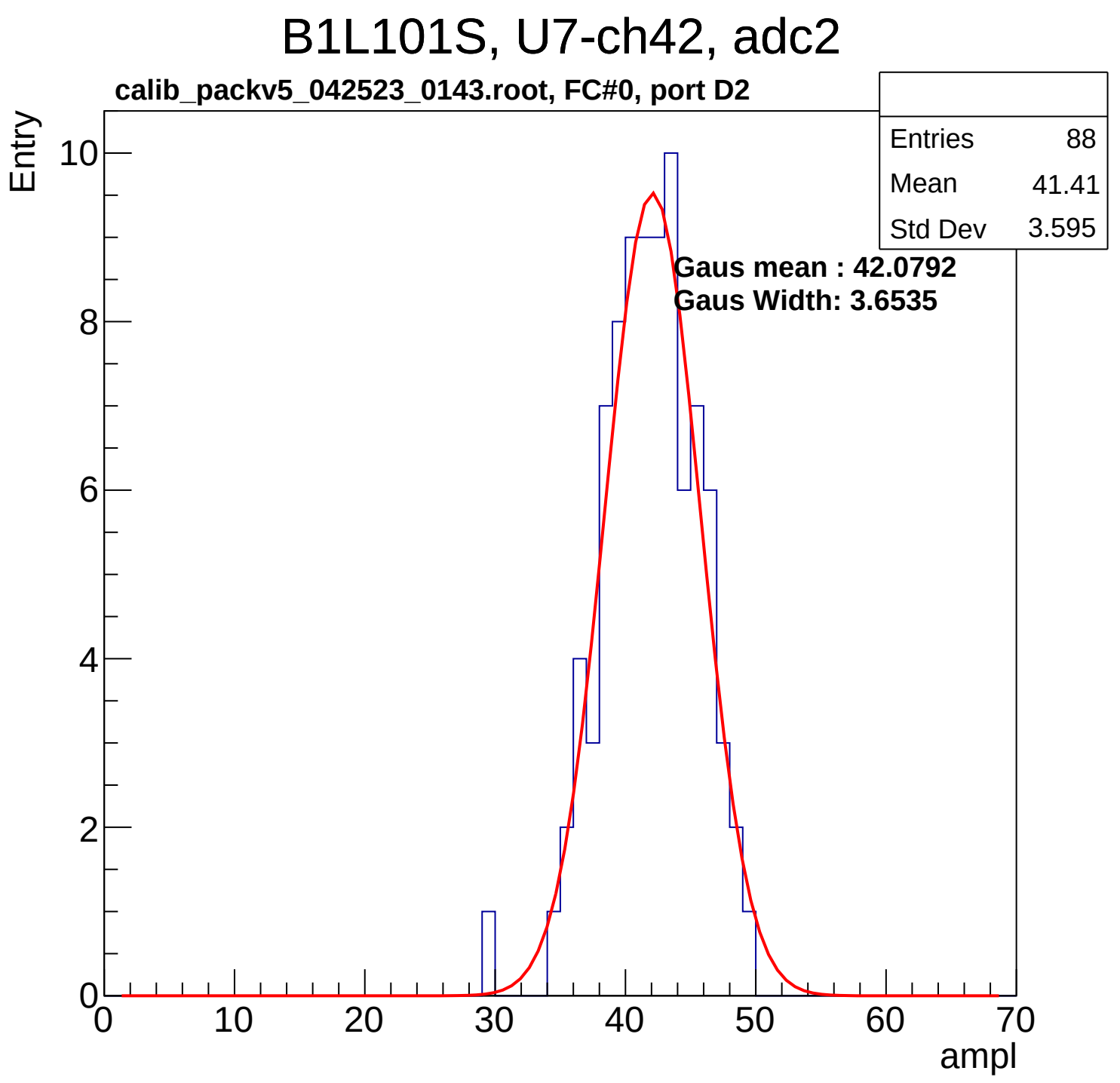
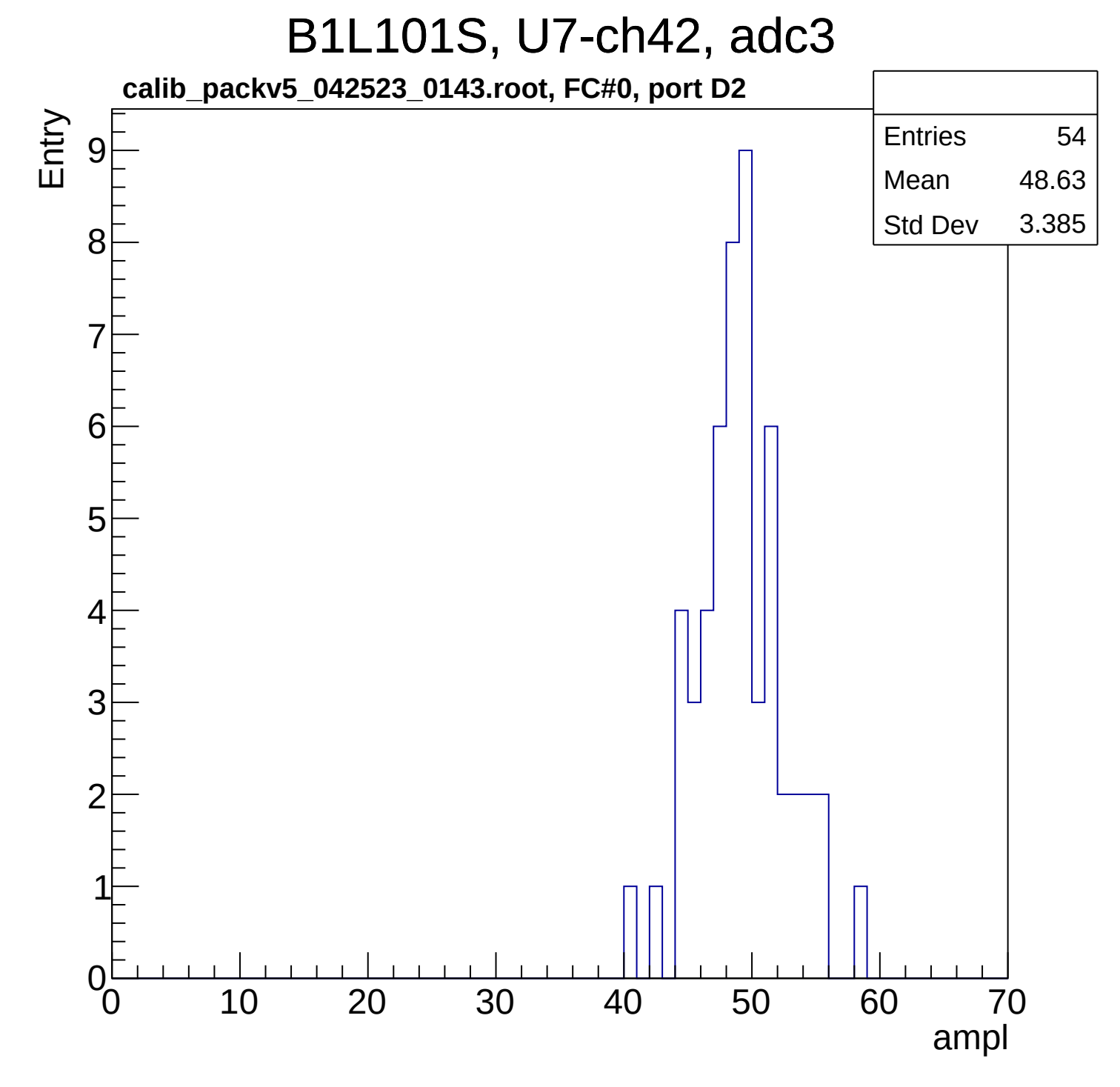

B1L101S, U7-ch42, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 88
Mean 41.41
Std Dev 3.595
Gaus mean : 42.0792
Gaus Width: 3.6535
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch42, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 48.63
Std Dev 3.385
Entry
ampl
0
1
2
3
4
5
6
7
8
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0
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40
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60
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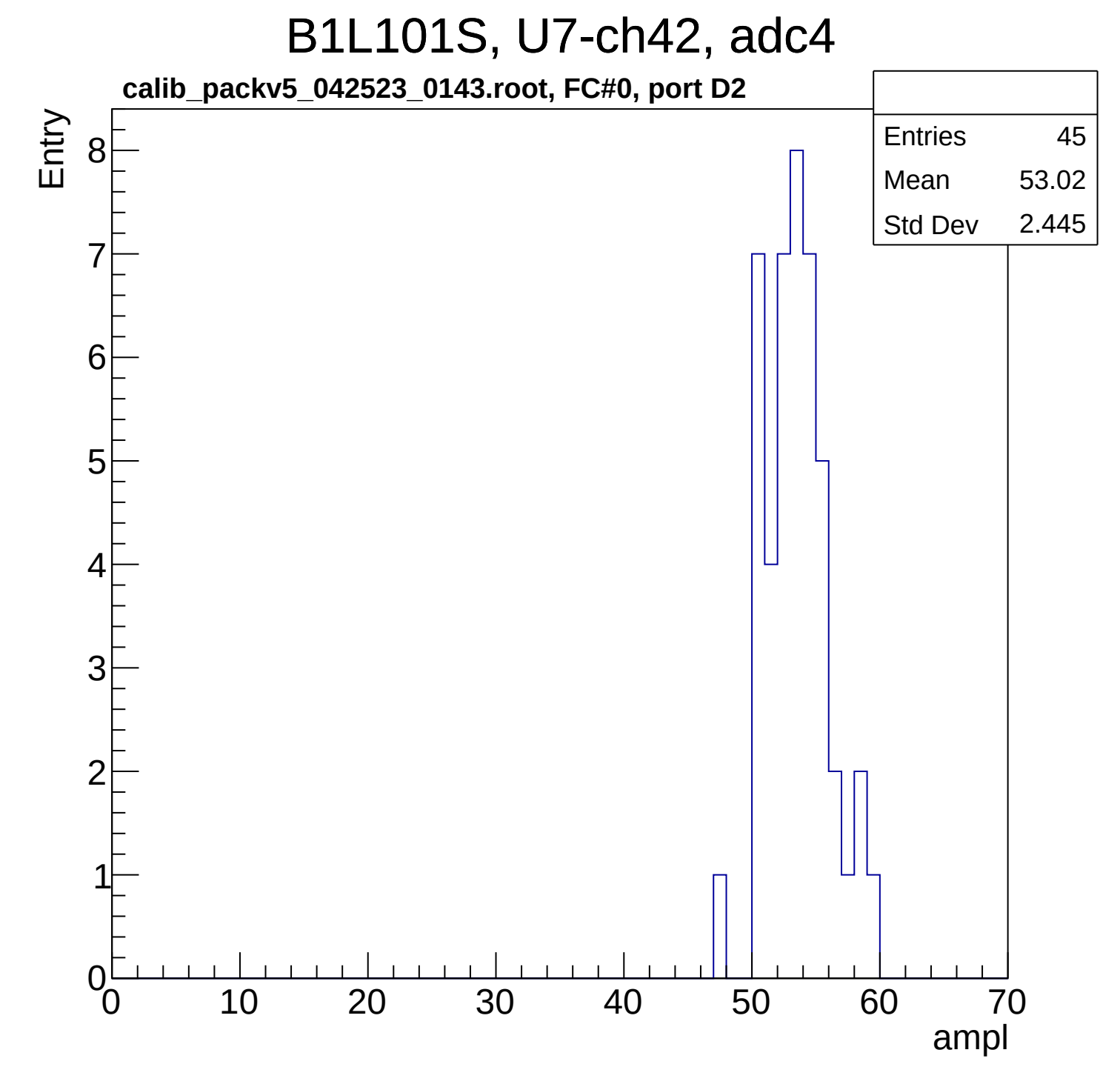
B1L101S, U7-ch42, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 53.02
Std Dev 2.445
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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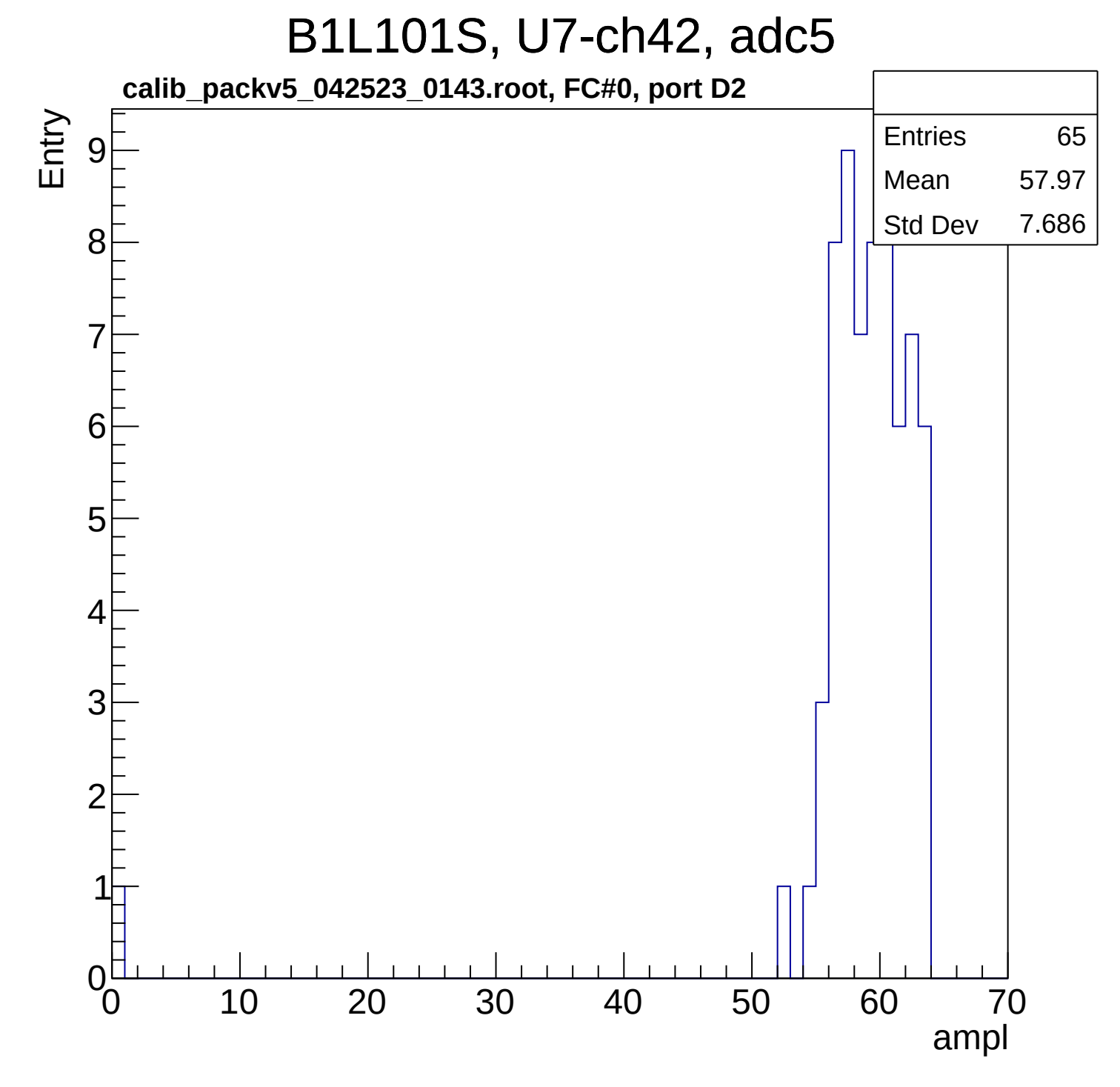
B1L101S, U7-ch42, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 57.97
Std Dev 7.686
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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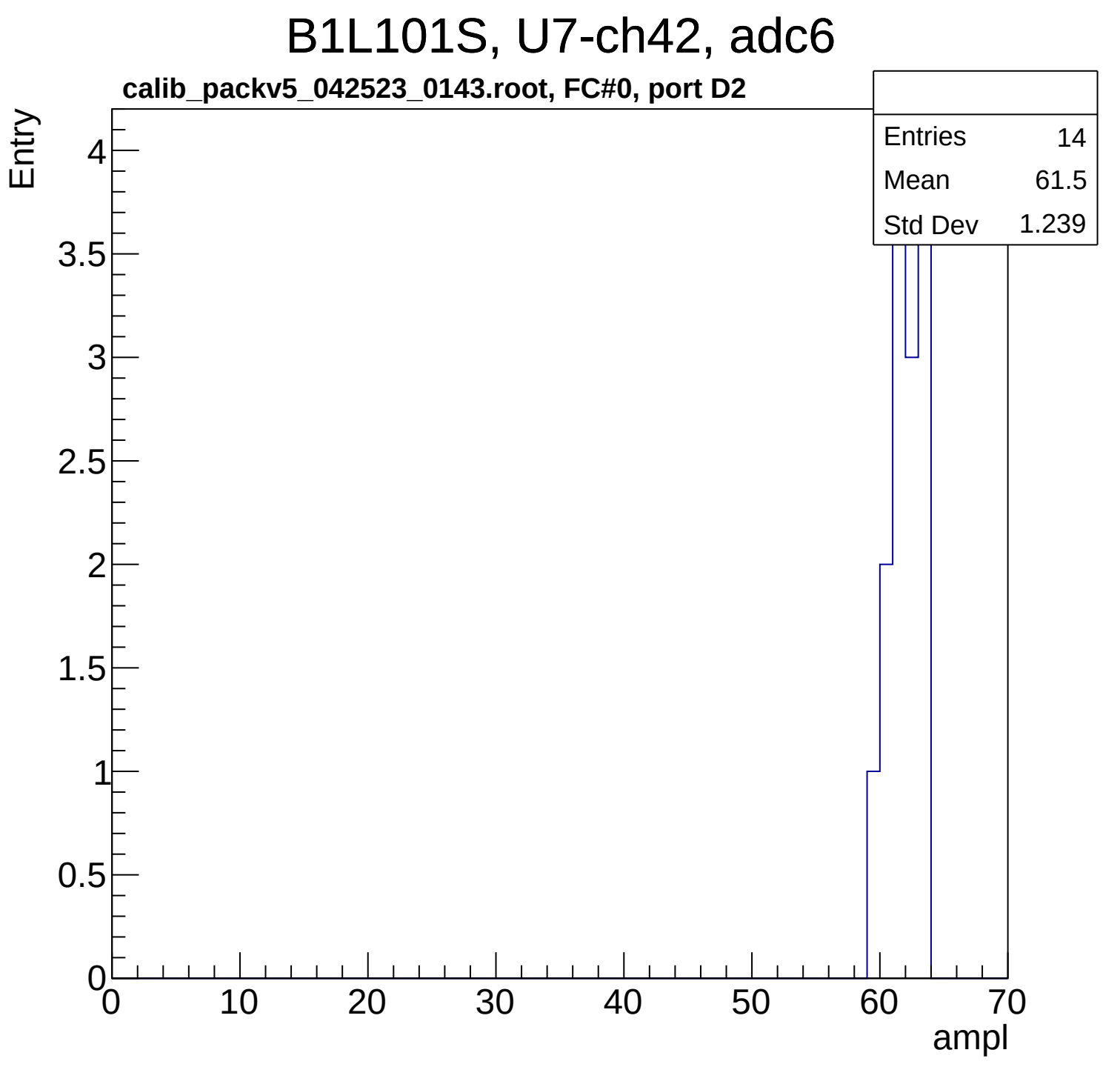
B1L101S, U7-ch42, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 14
Mean 61.5
Std Dev 1.239
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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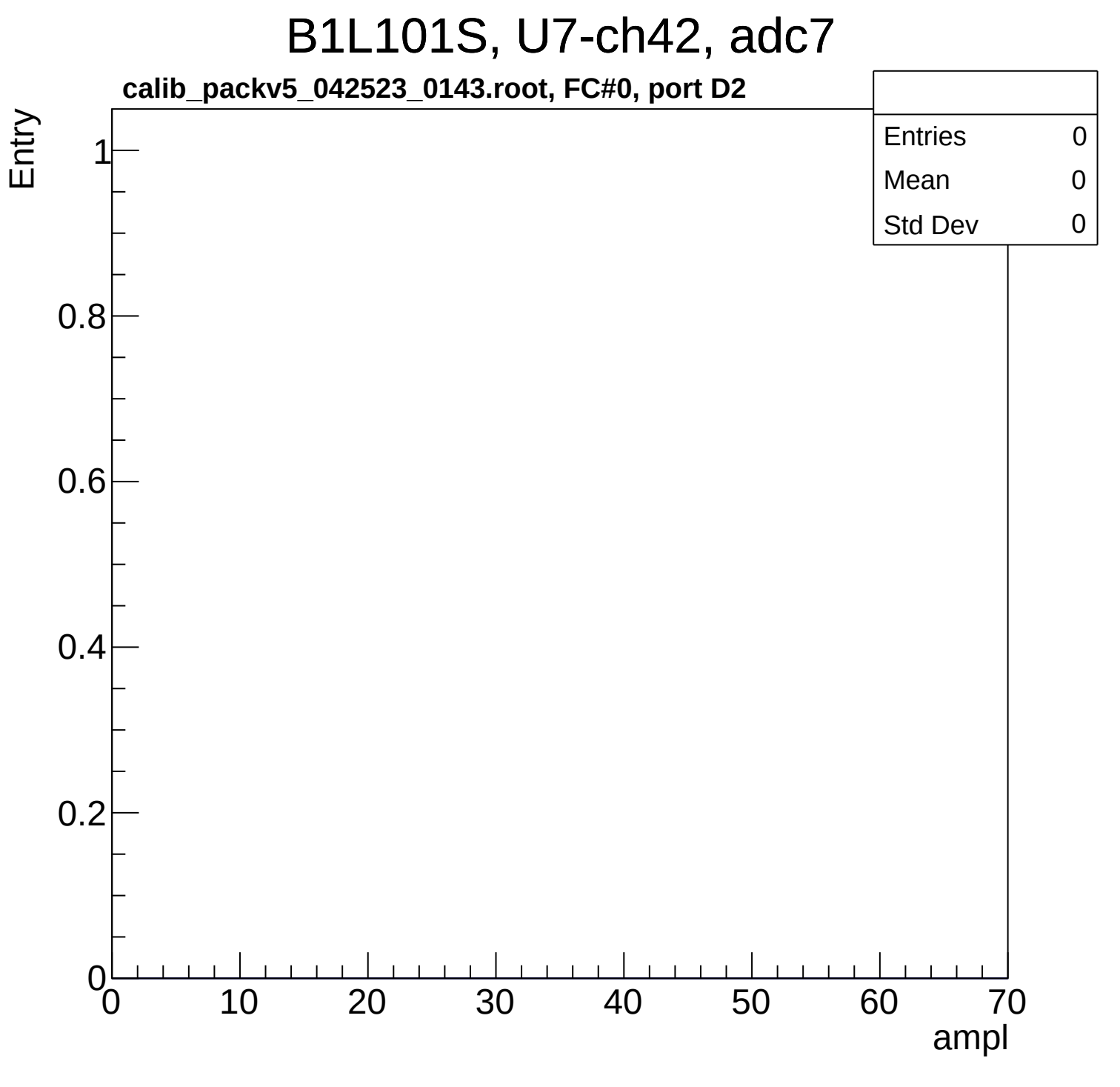
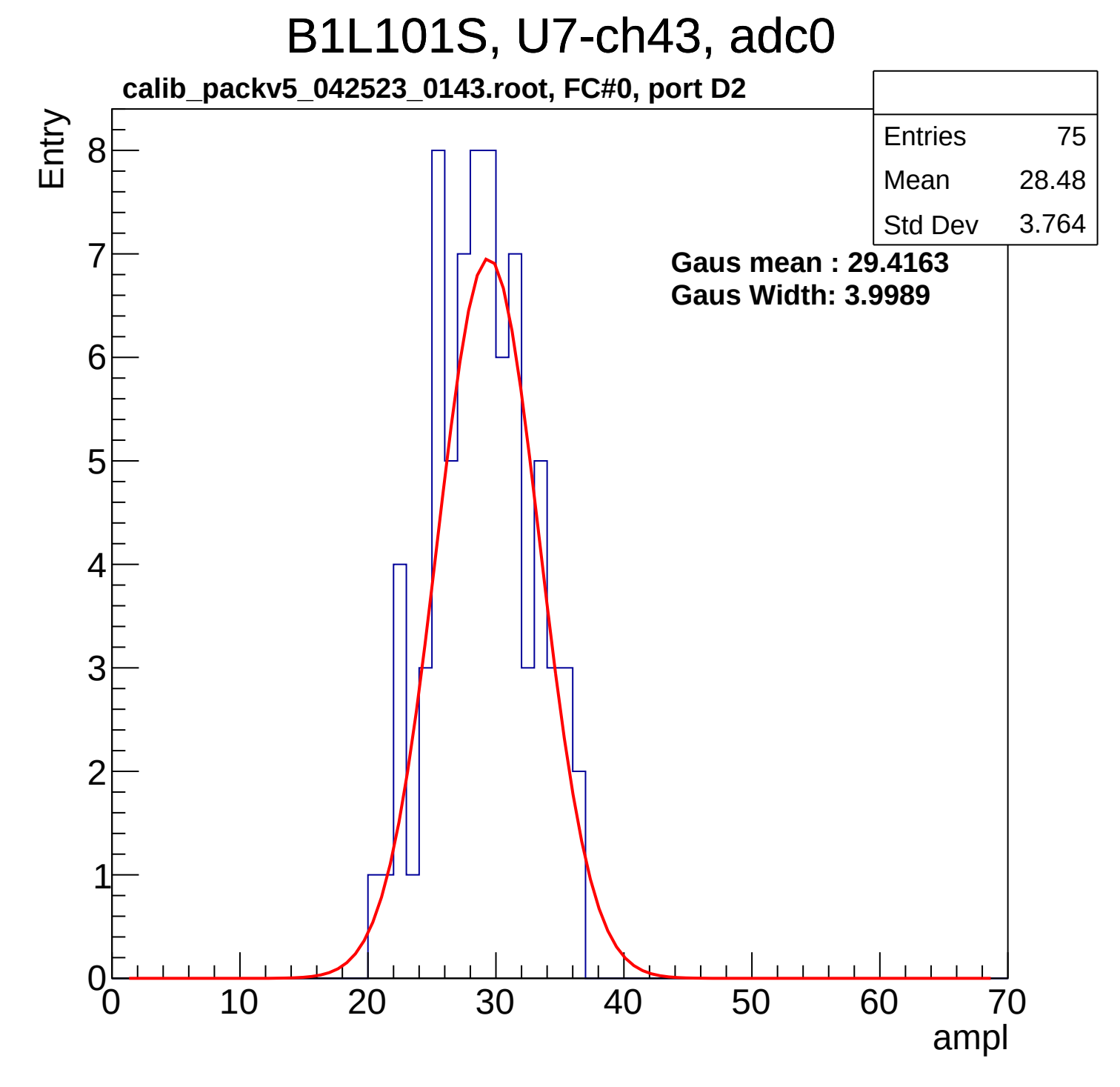
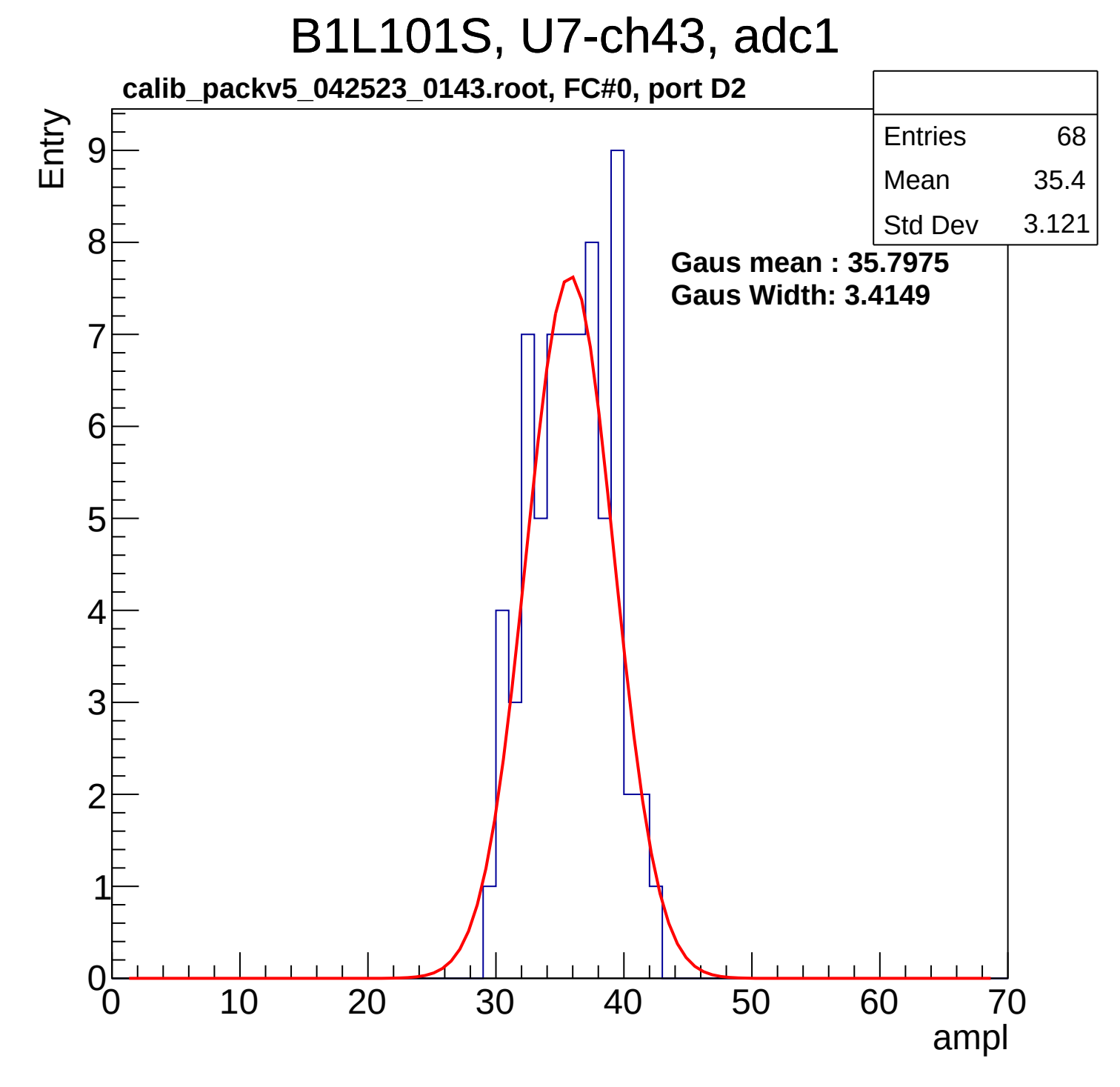
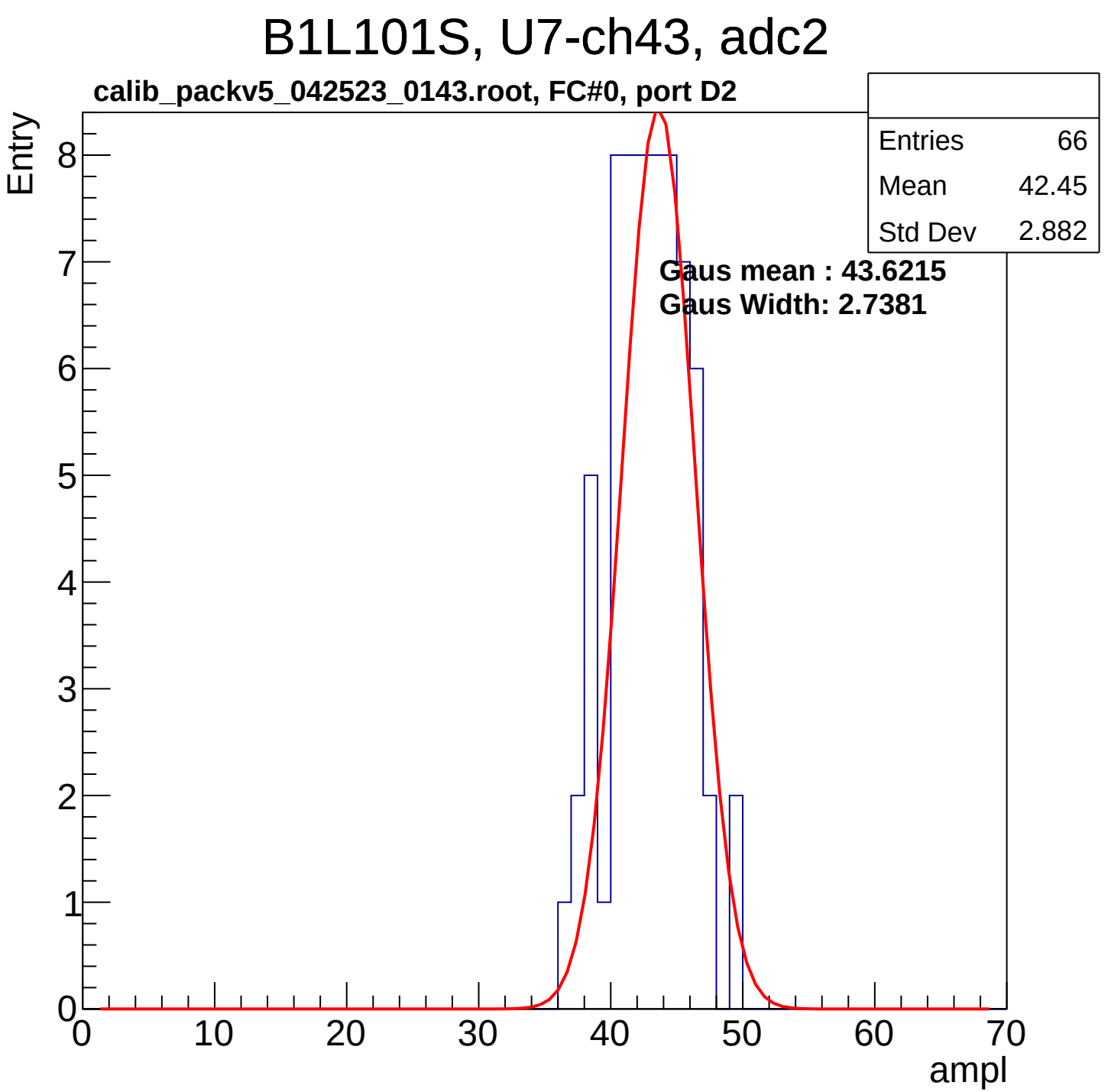
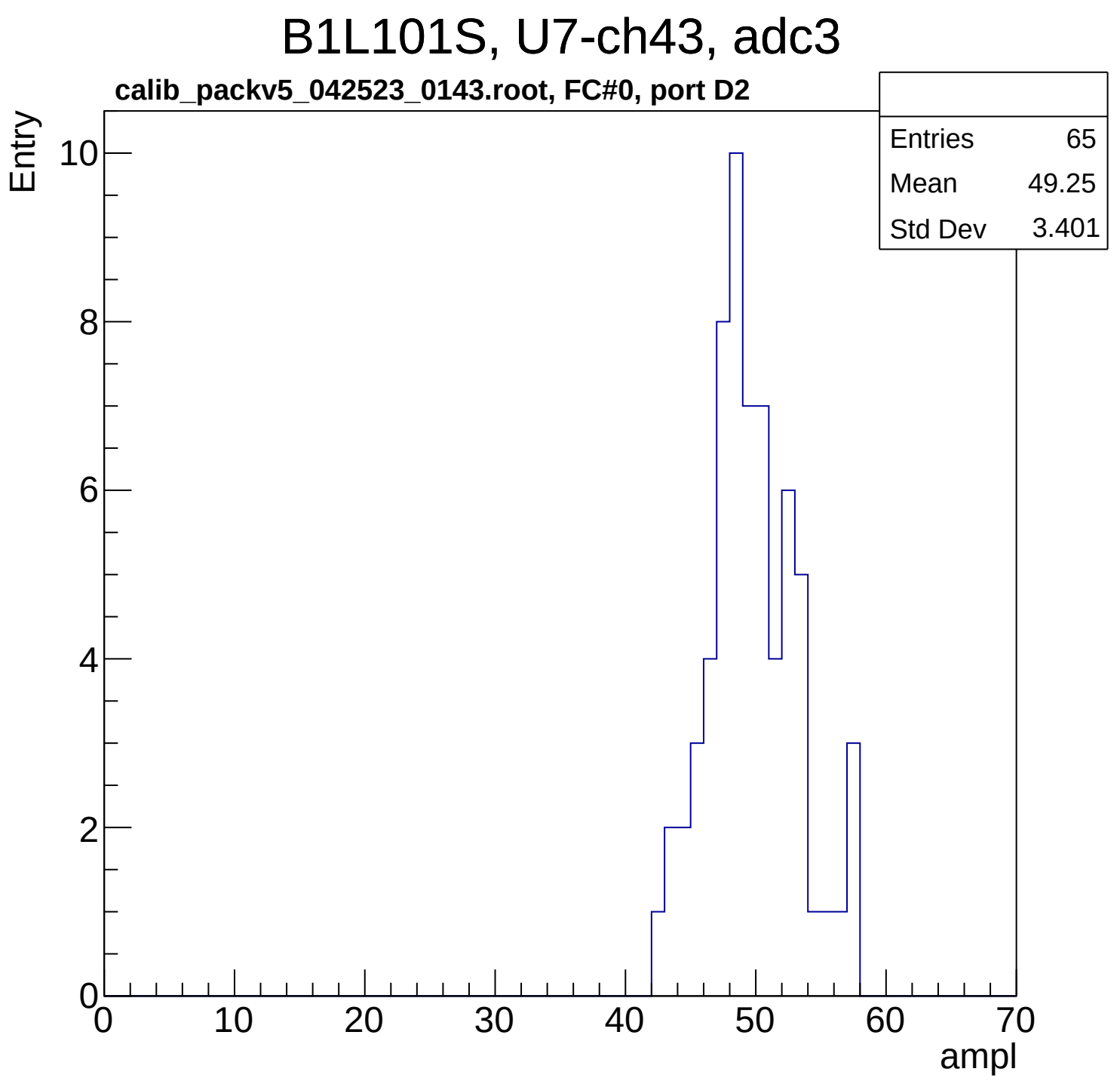
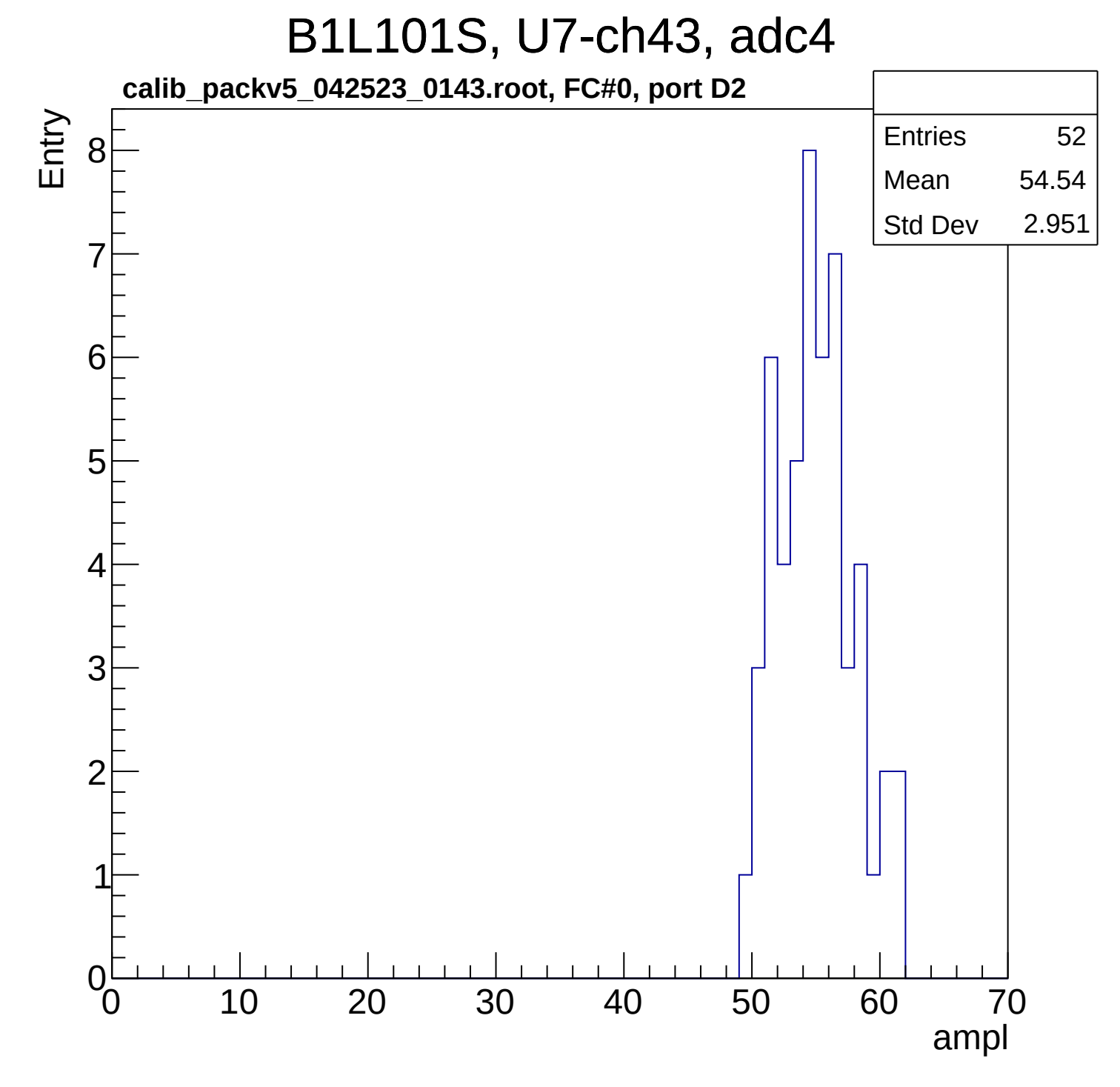

B1L101S, U7-ch42, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

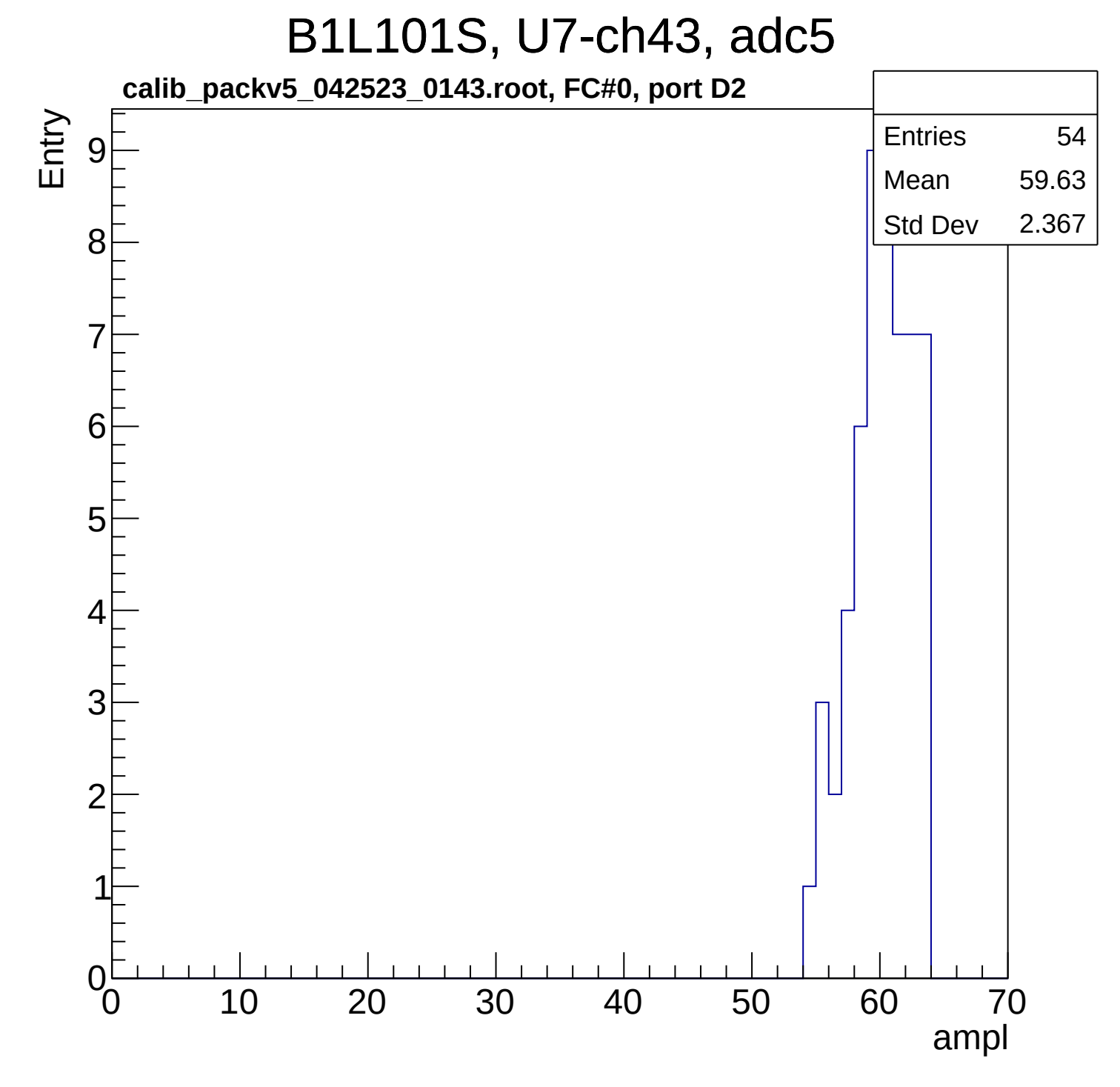

B1L101S, U7-ch43, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 28.48
Std Dev 3.764
Gaus mean : 29.4163
Gaus Width: 3.9989
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

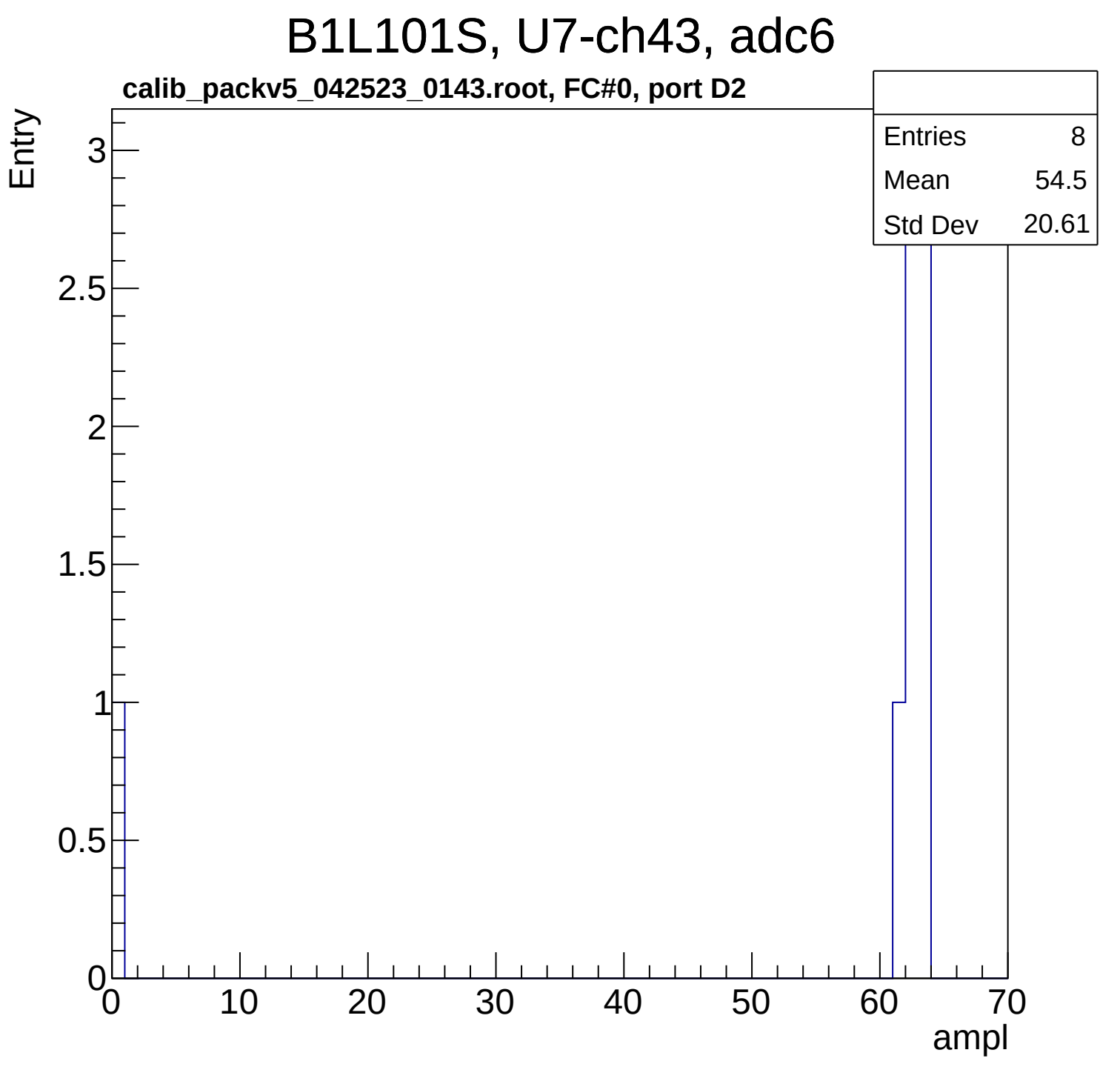

B1L101S, U7-ch43, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 35.4
Std Dev 3.121
Gaus mean : 35.7975
Gaus Width: 3.4149
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

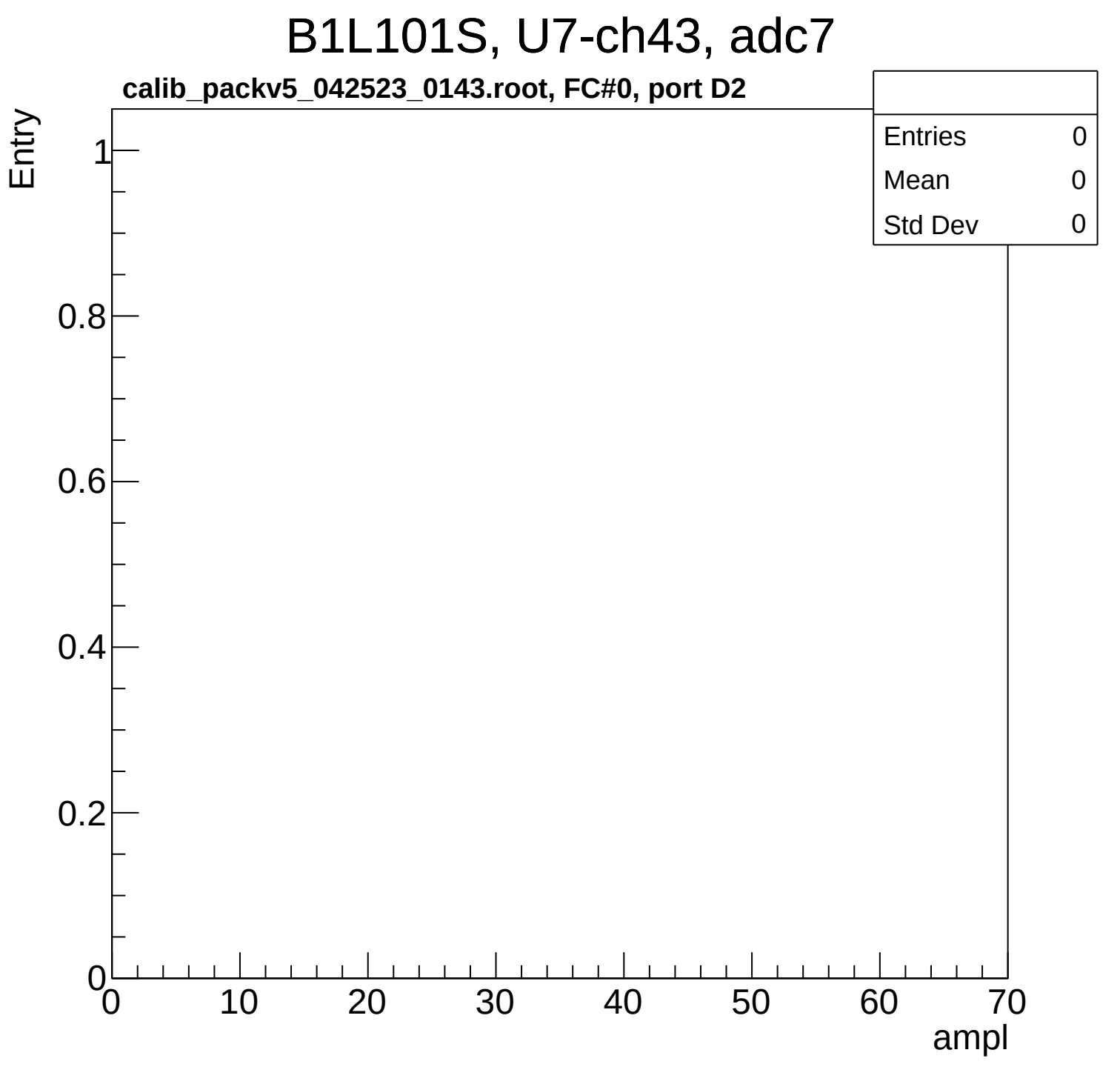

B1L101S, U7-ch43, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 42.45
Std Dev 2.882
Gaus mean : 43.6215
Gaus Width: 2.7381
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

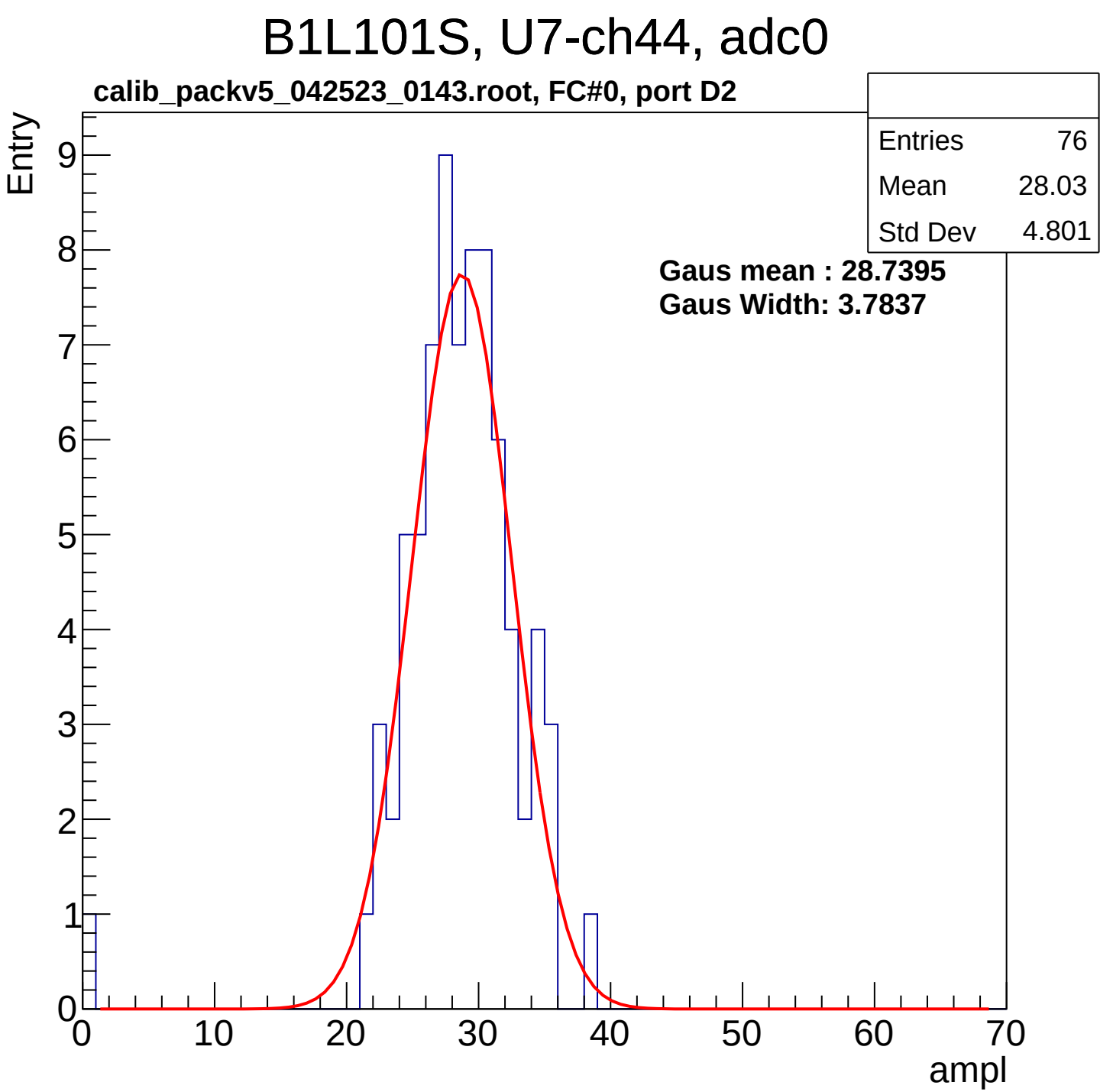

B1L101S, U7-ch43, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 49.25
Std Dev 3.401
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

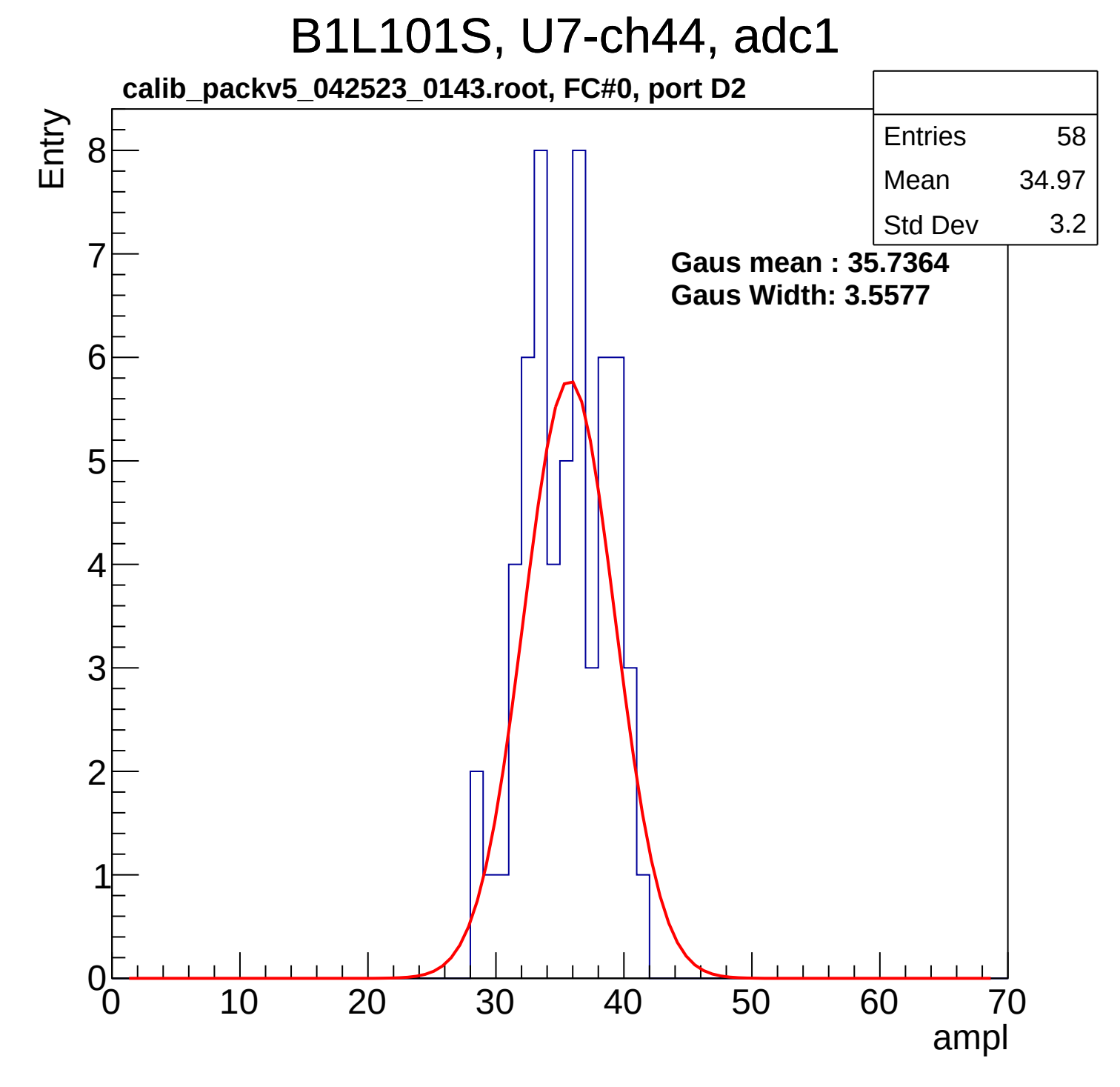

B1L101S, U7-ch43, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 54.54
Std Dev 2.951
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

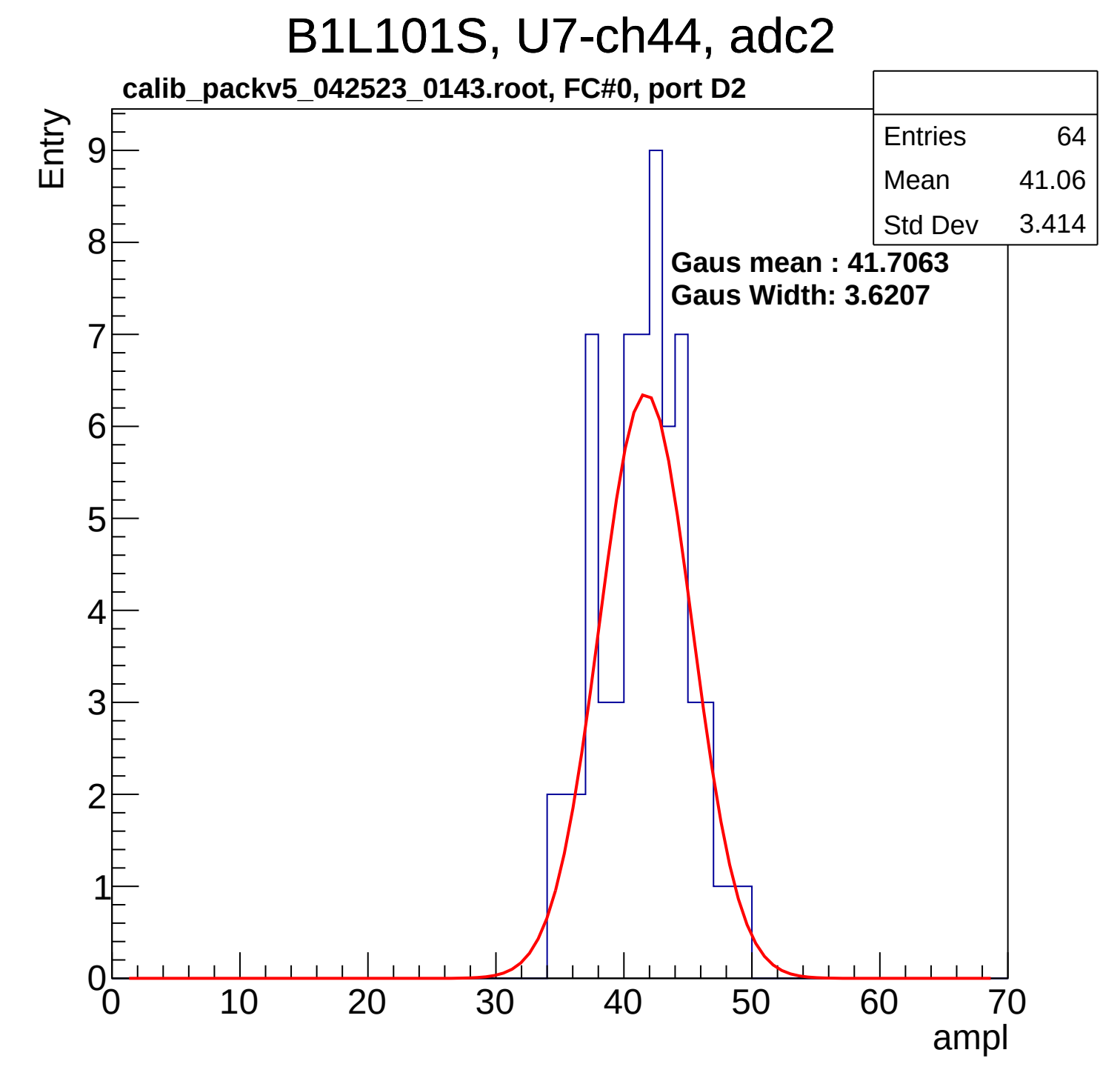

B1L101S, U7-ch43, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 59.63
Std Dev 2.367
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

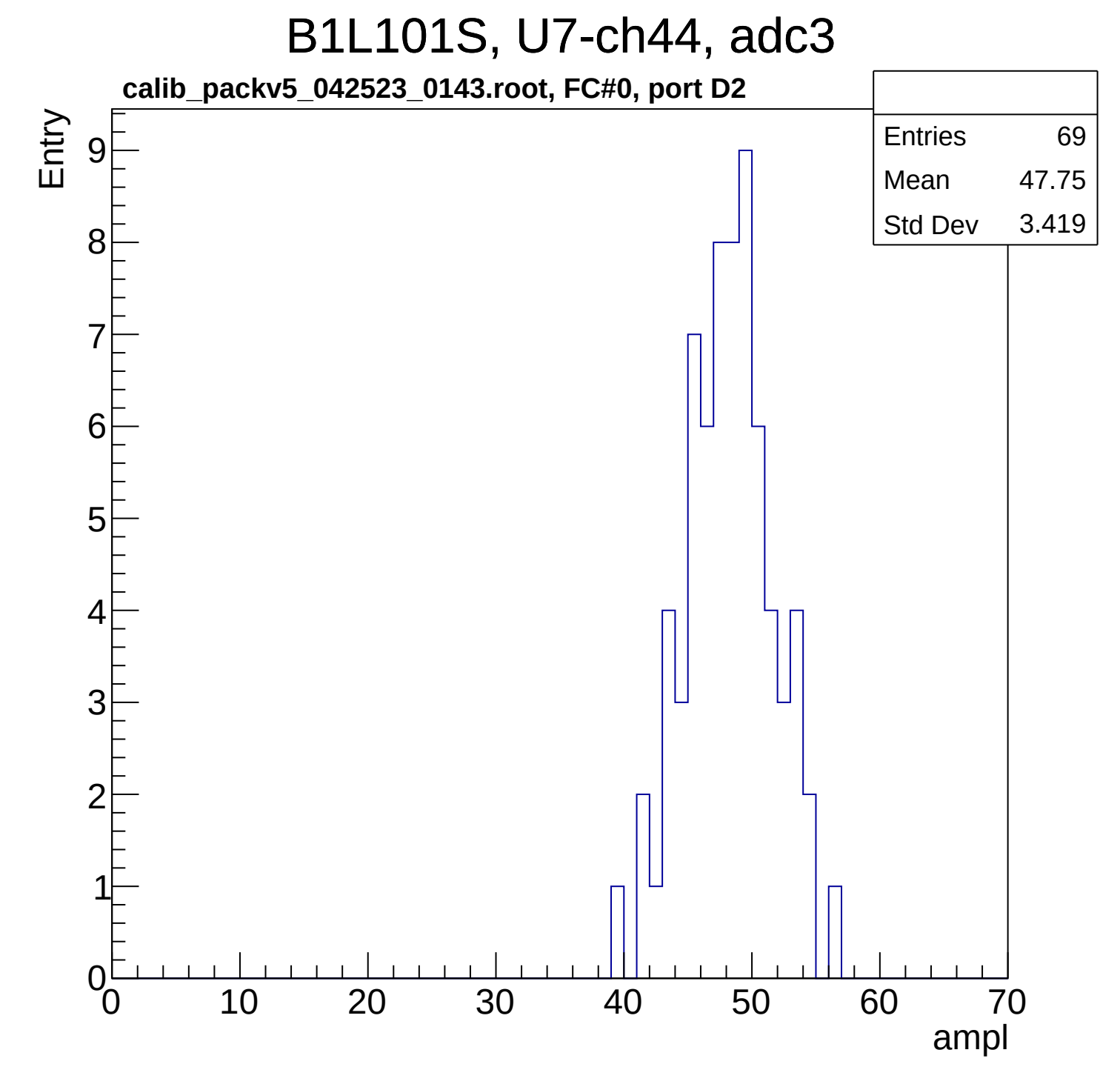

B1L101S, U7-ch43, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 54.5
Std Dev 20.61
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

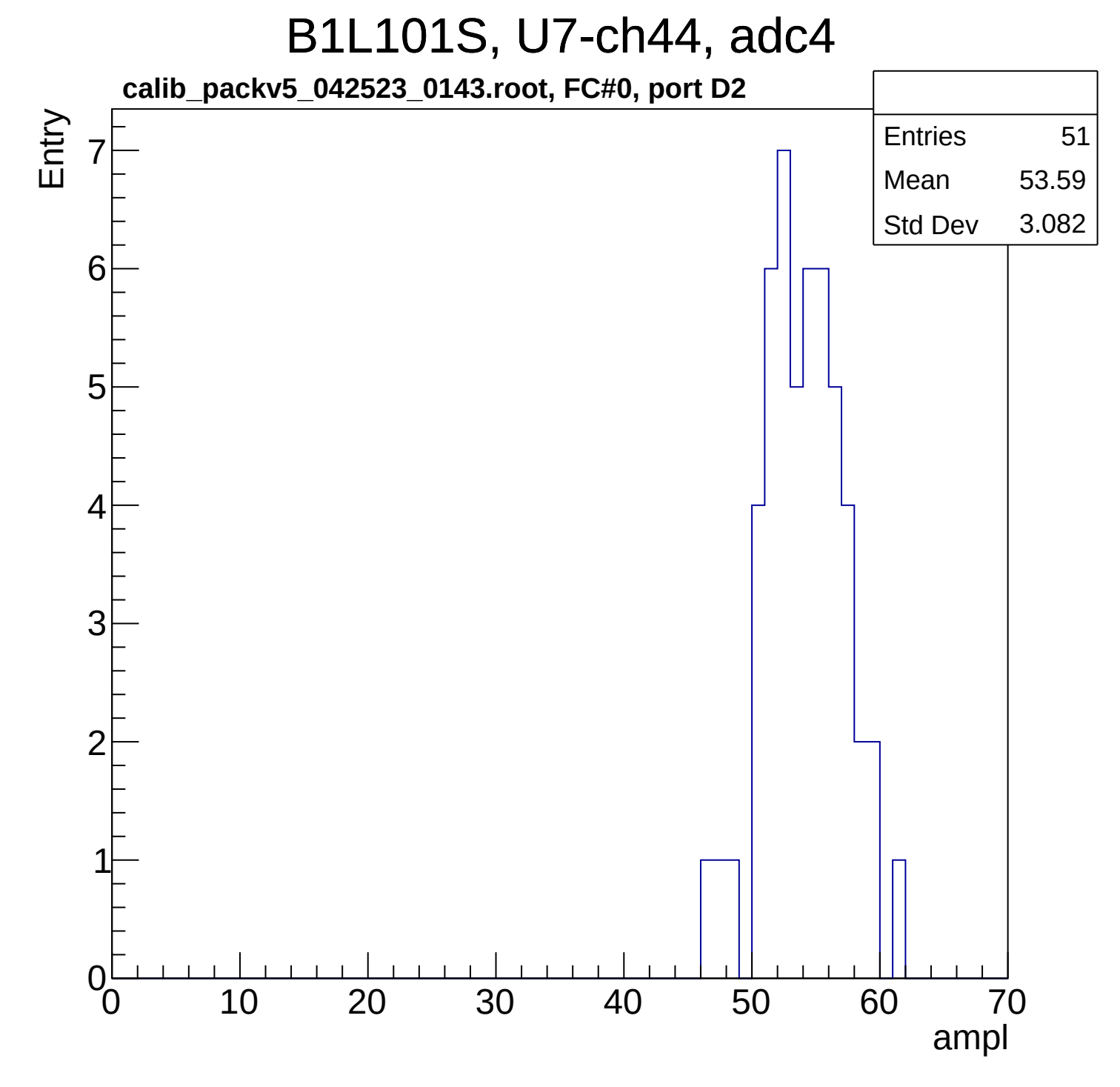

B1L101S, U7-ch43, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

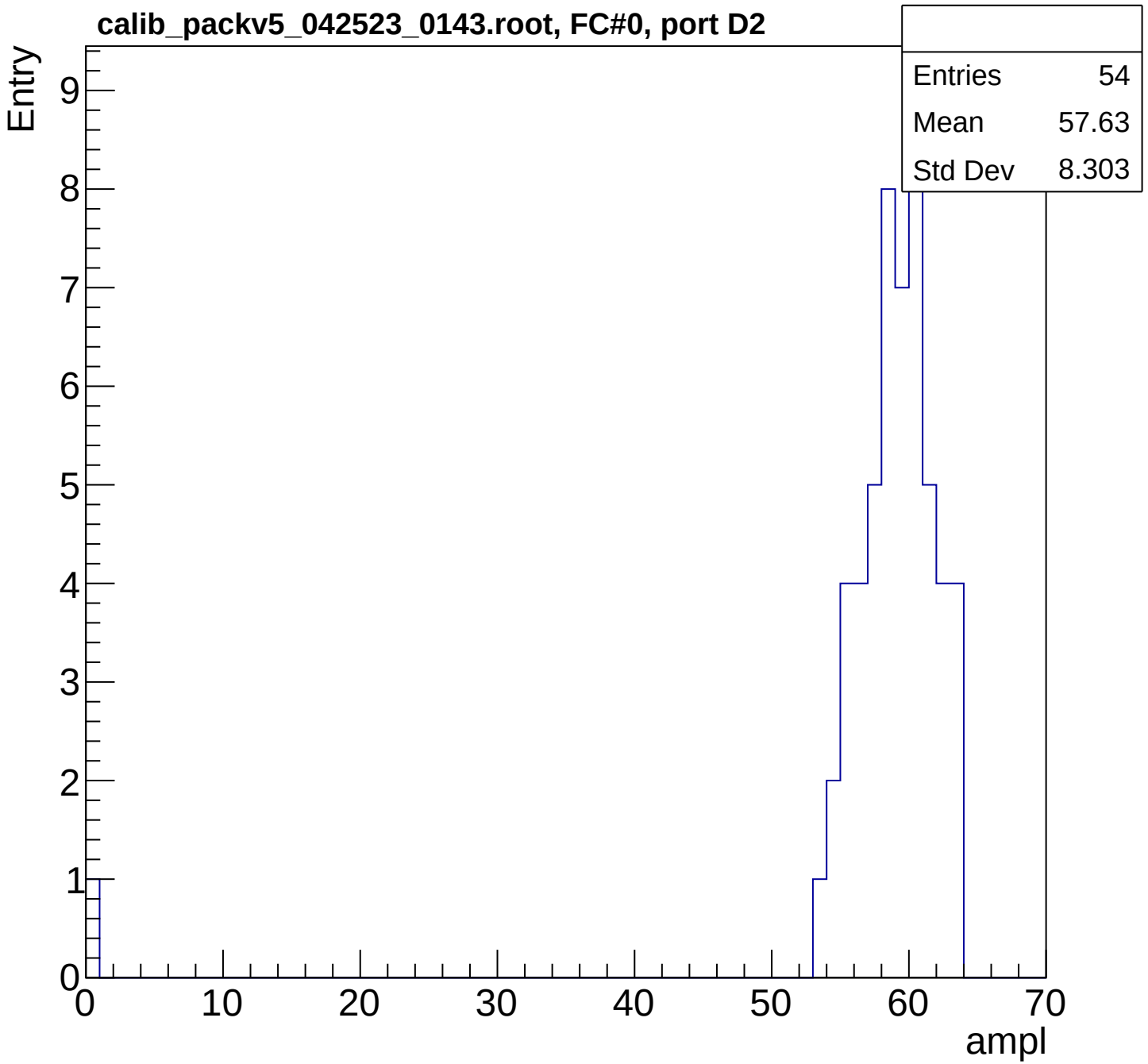

B1L101S, U7-ch44, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 28.03
Std Dev 4.801
Gaus mean : 28.7395
Gaus Width: 3.7837
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

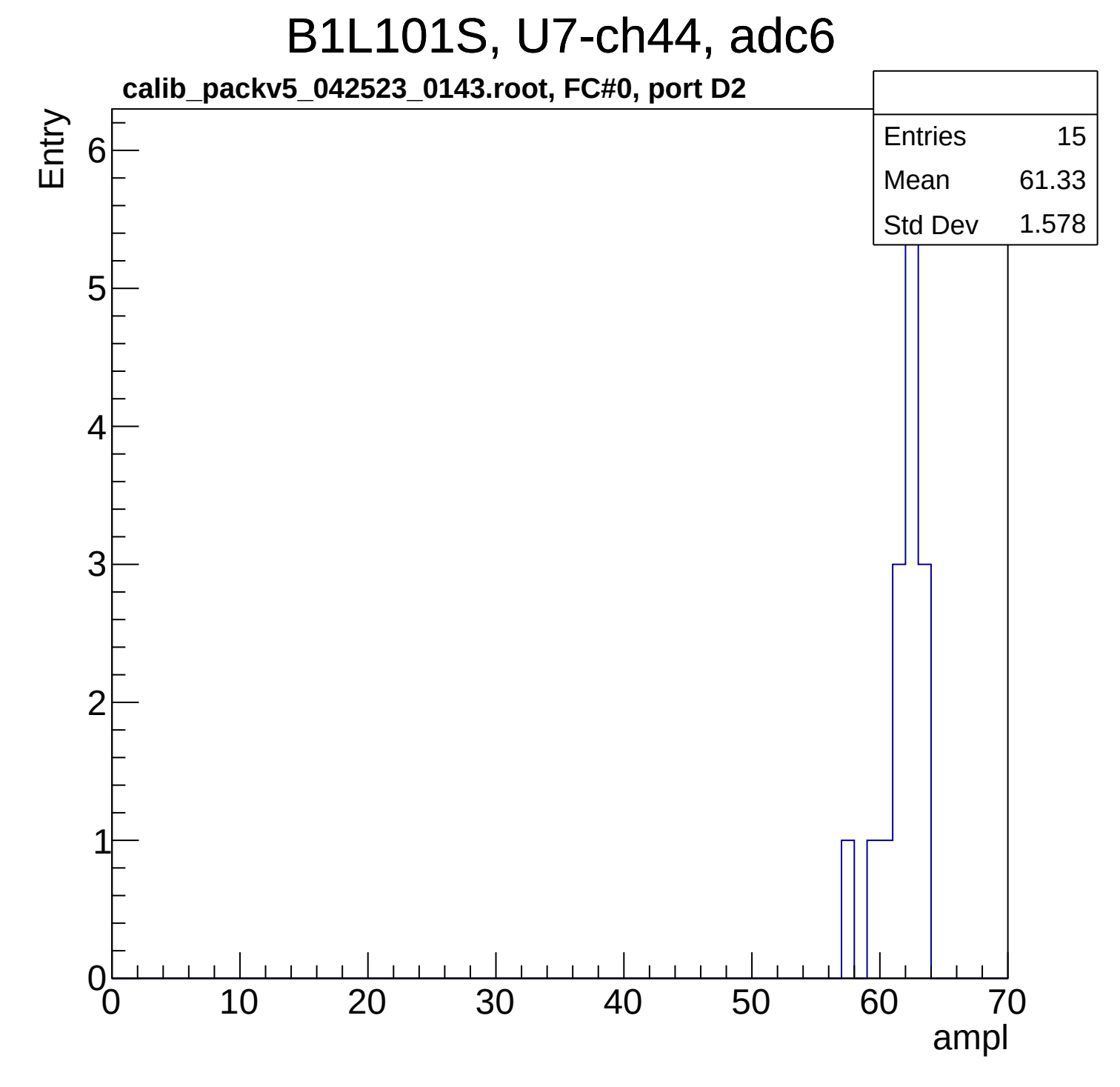

B1L101S, U7-ch44, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 34.97
Std Dev 3.2
Gaus mean : 35.7364
Gaus Width: 3.5577
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch44, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 41.06
Std Dev 3.414
Gaus mean : 41.7063
Gaus Width: 3.6207
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L101S, U7-ch44, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 47.75
Std Dev 3.419
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch44, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 53.59
Std Dev 3.082
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch44, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 57.63
Std Dev 8.303
Entry
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch44, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 15
Mean 61.33
Std Dev 1.578
Entry
ampl
0
1
2
3
4
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6
0
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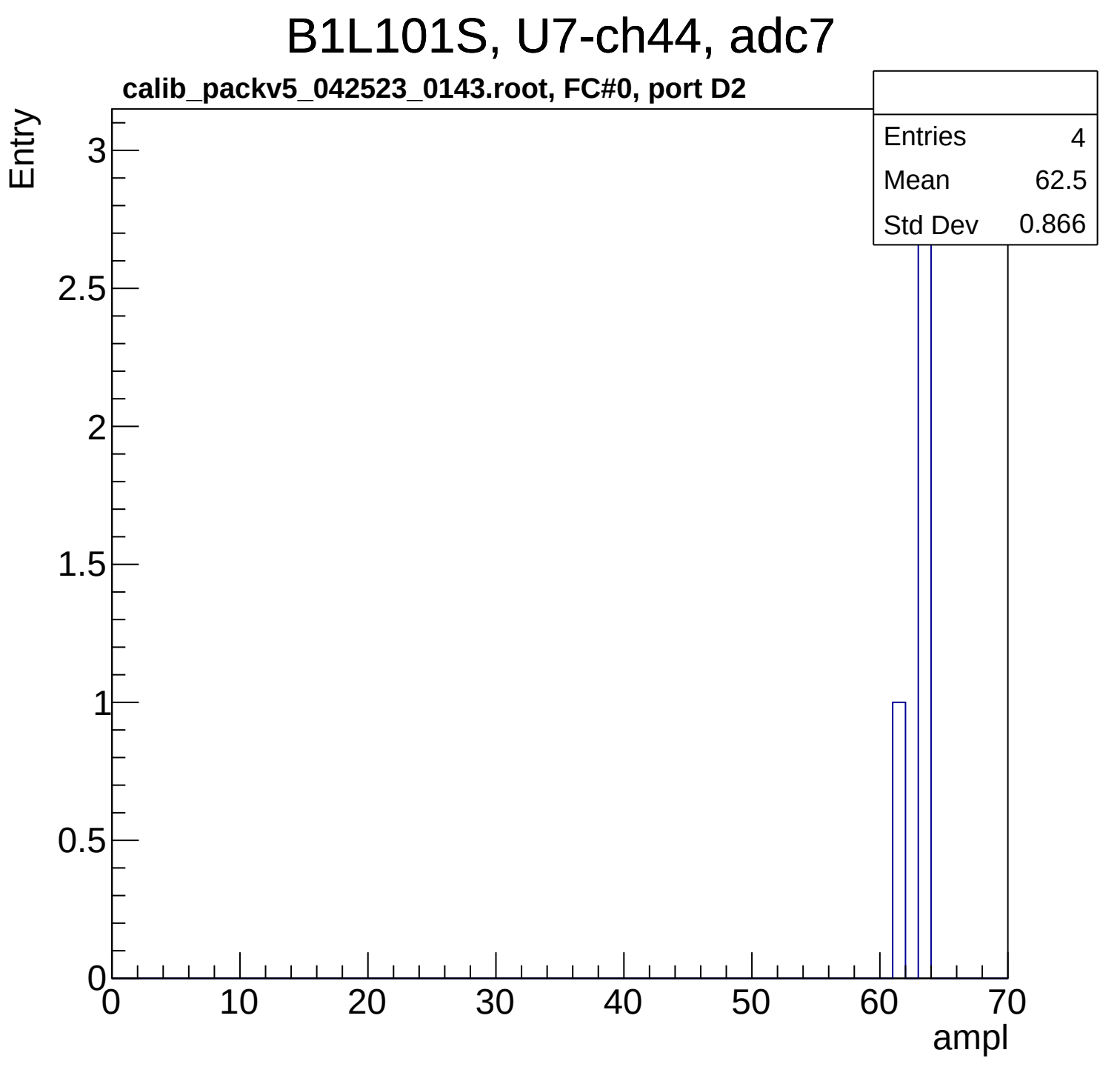
20
30
40
50
60
70


B1L101S, U7-ch44, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 62.5
Std Dev 0.866
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
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60
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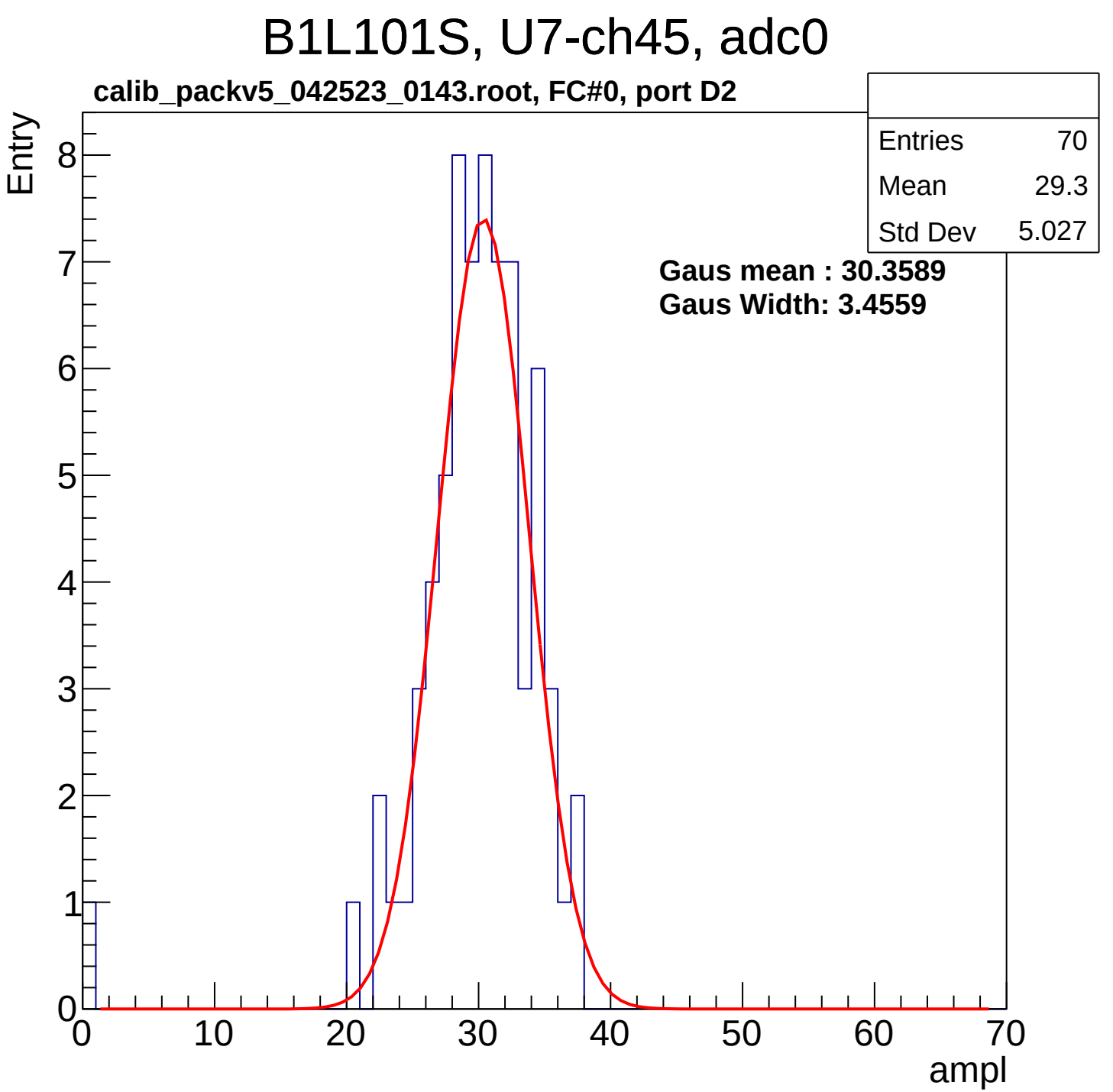
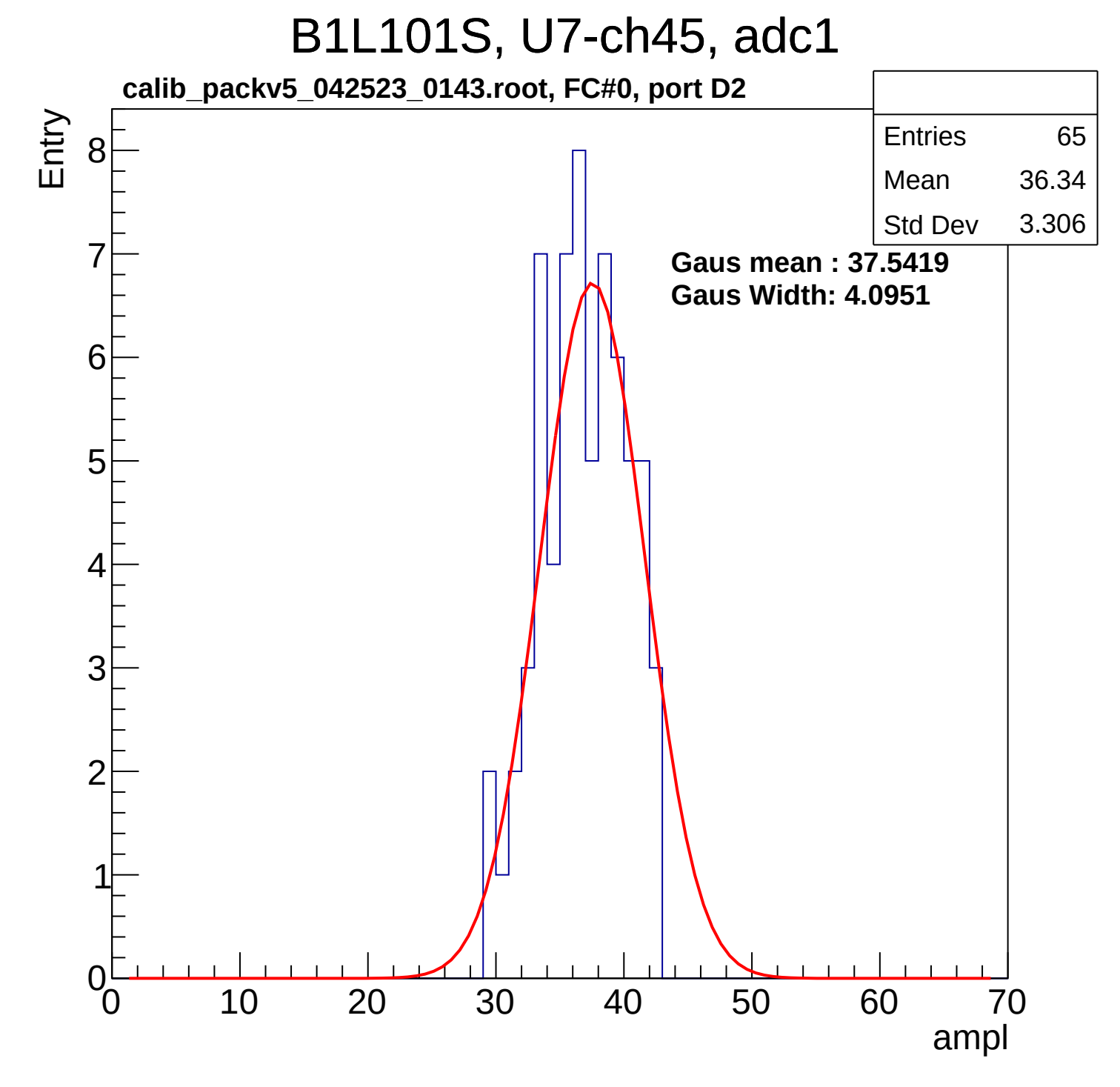
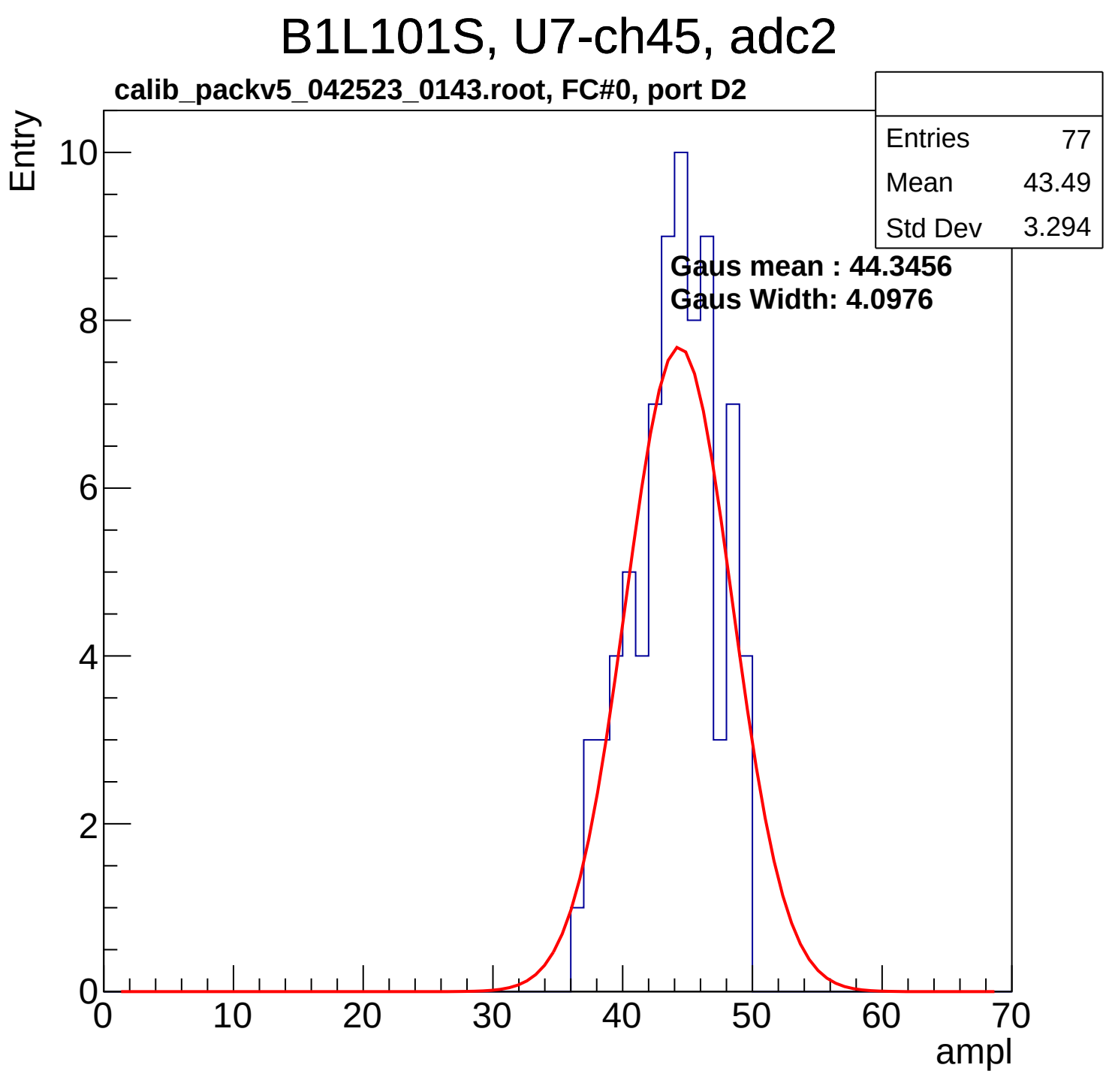
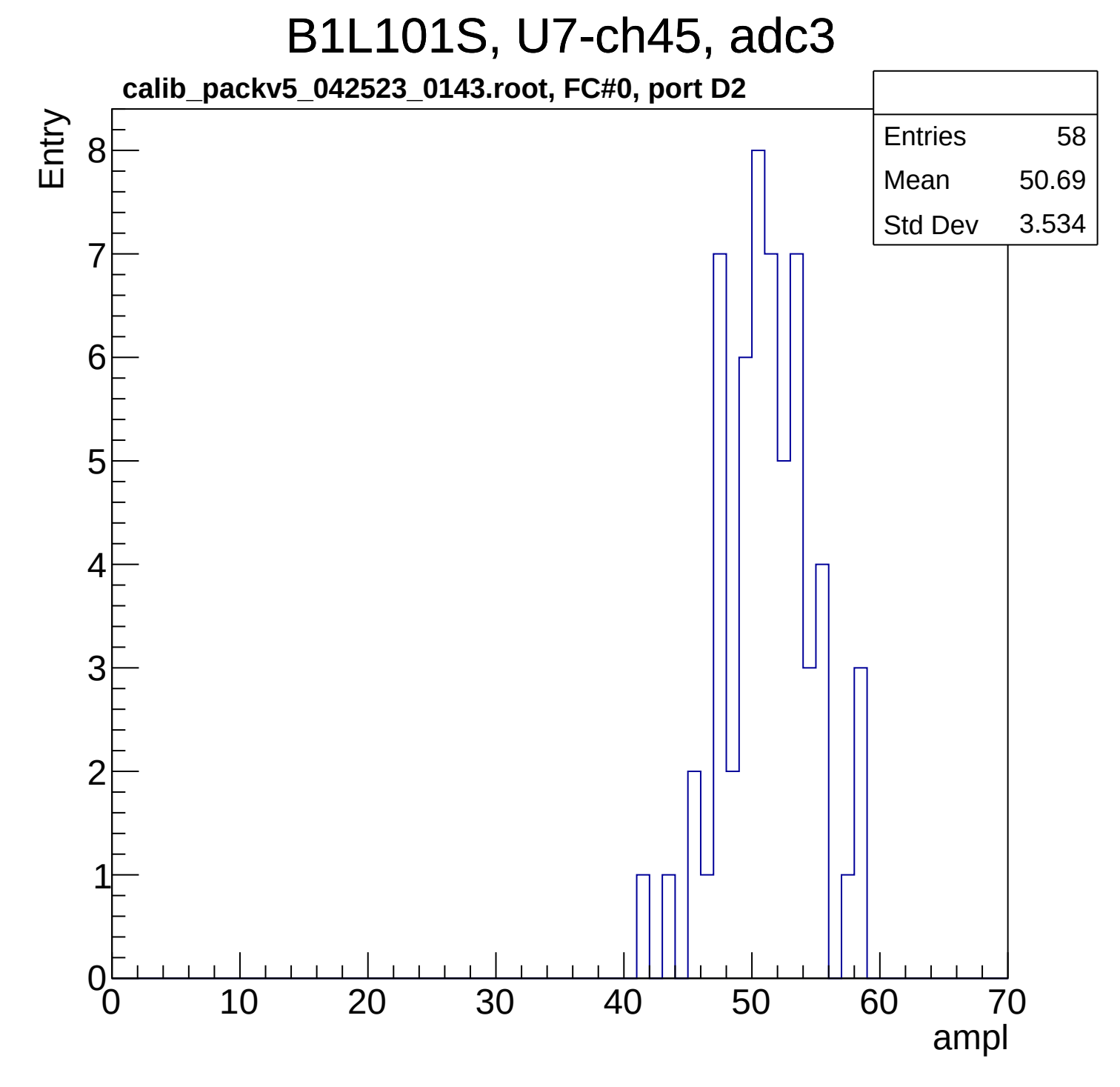
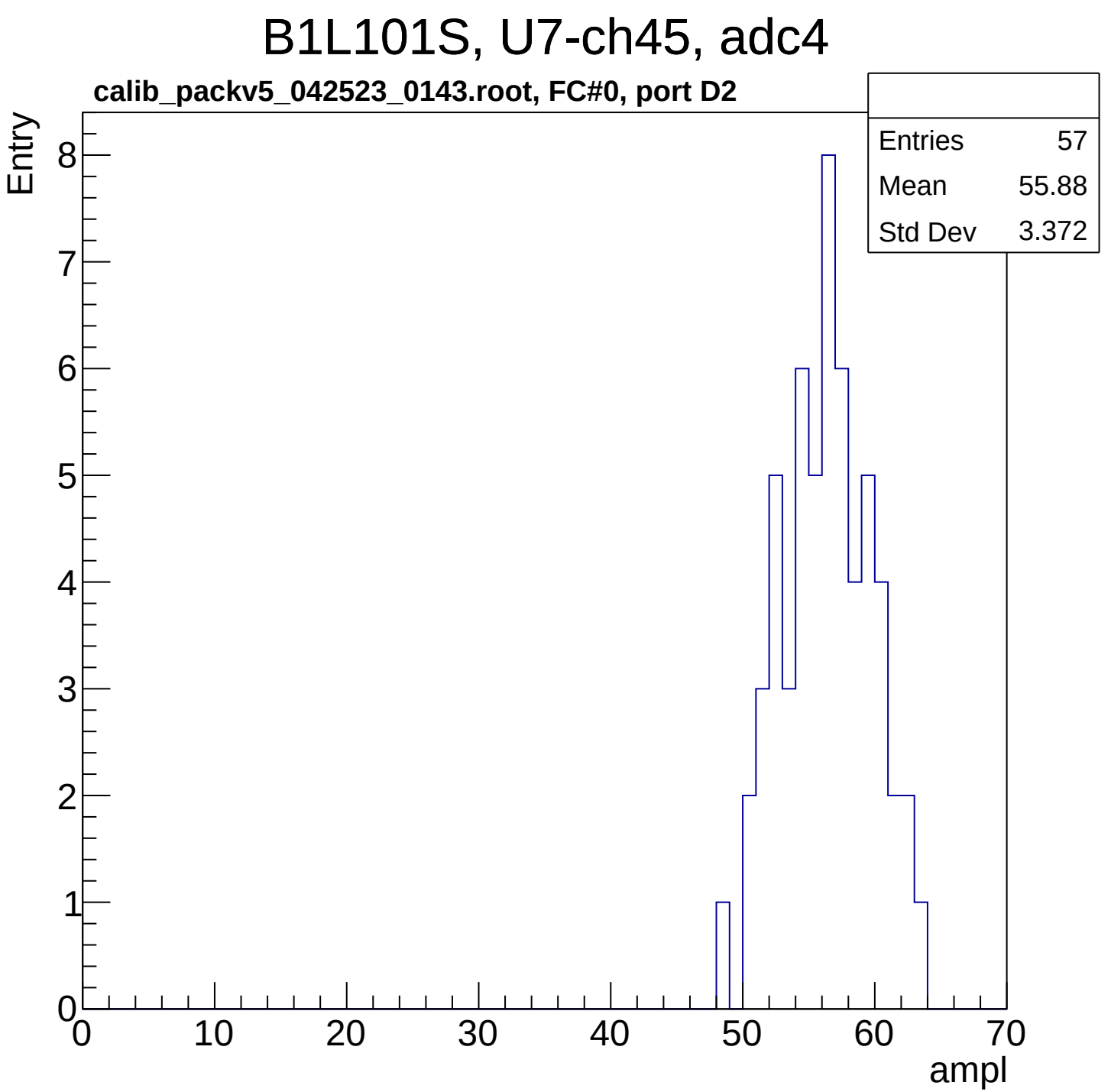
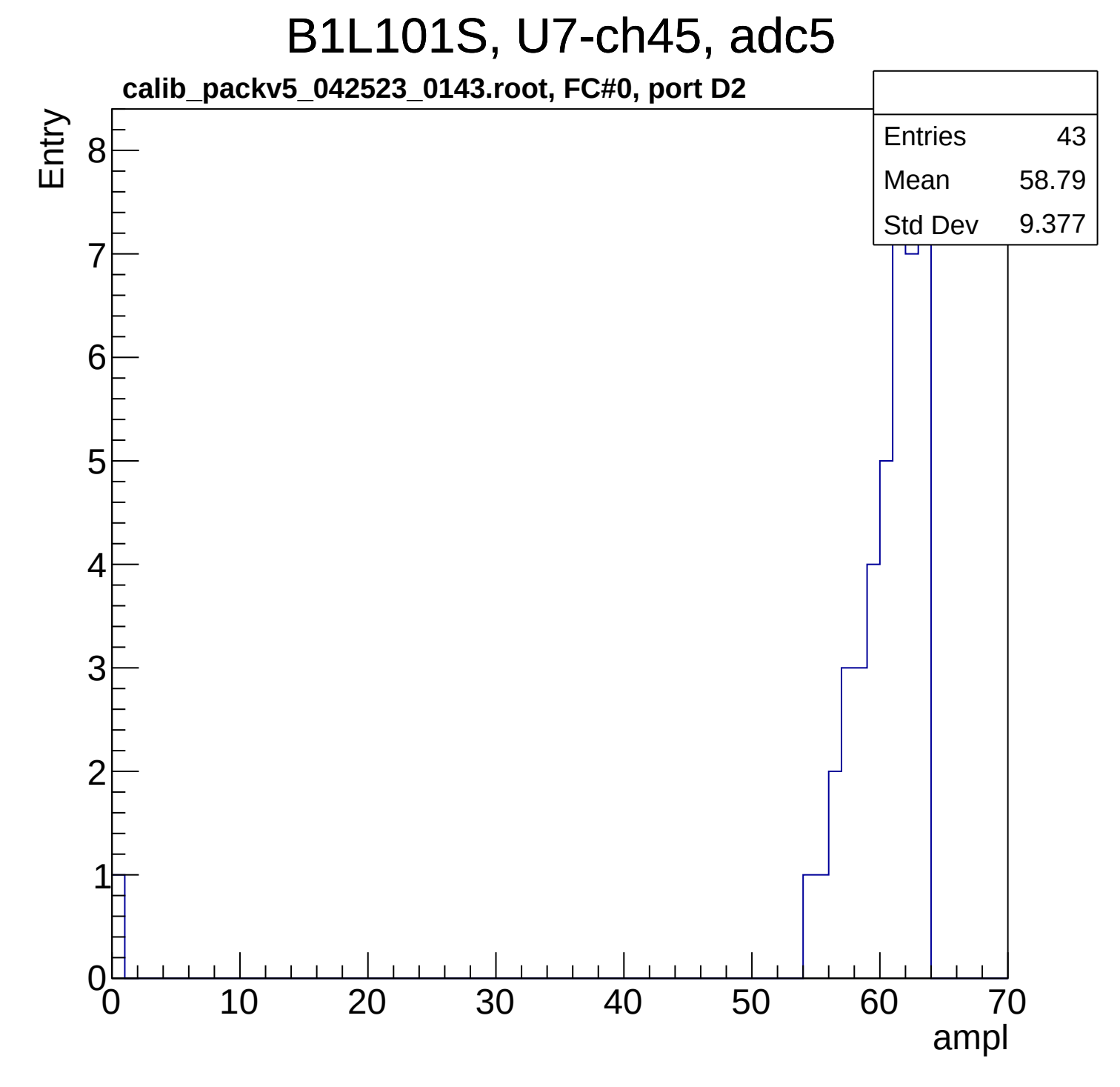

B1L101S, U7-ch45, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 29.3
Std Dev 5.027
Gaus mean : 30.3589
Gaus Width: 3.4559
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

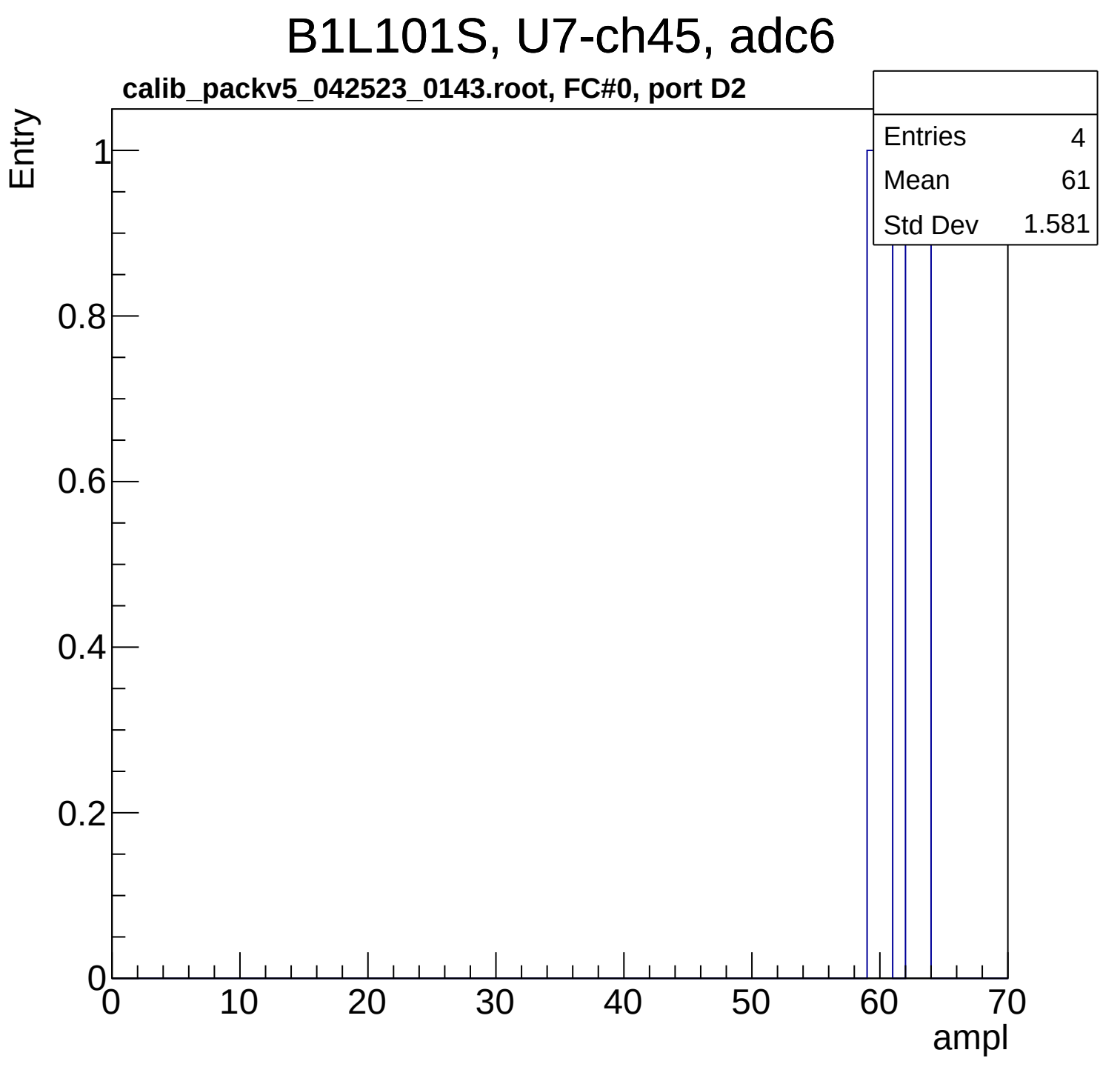

B1L101S, U7-ch45, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 36.34
Std Dev 3.306
Gaus mean : 37.5419
Gaus Width: 4.0951
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

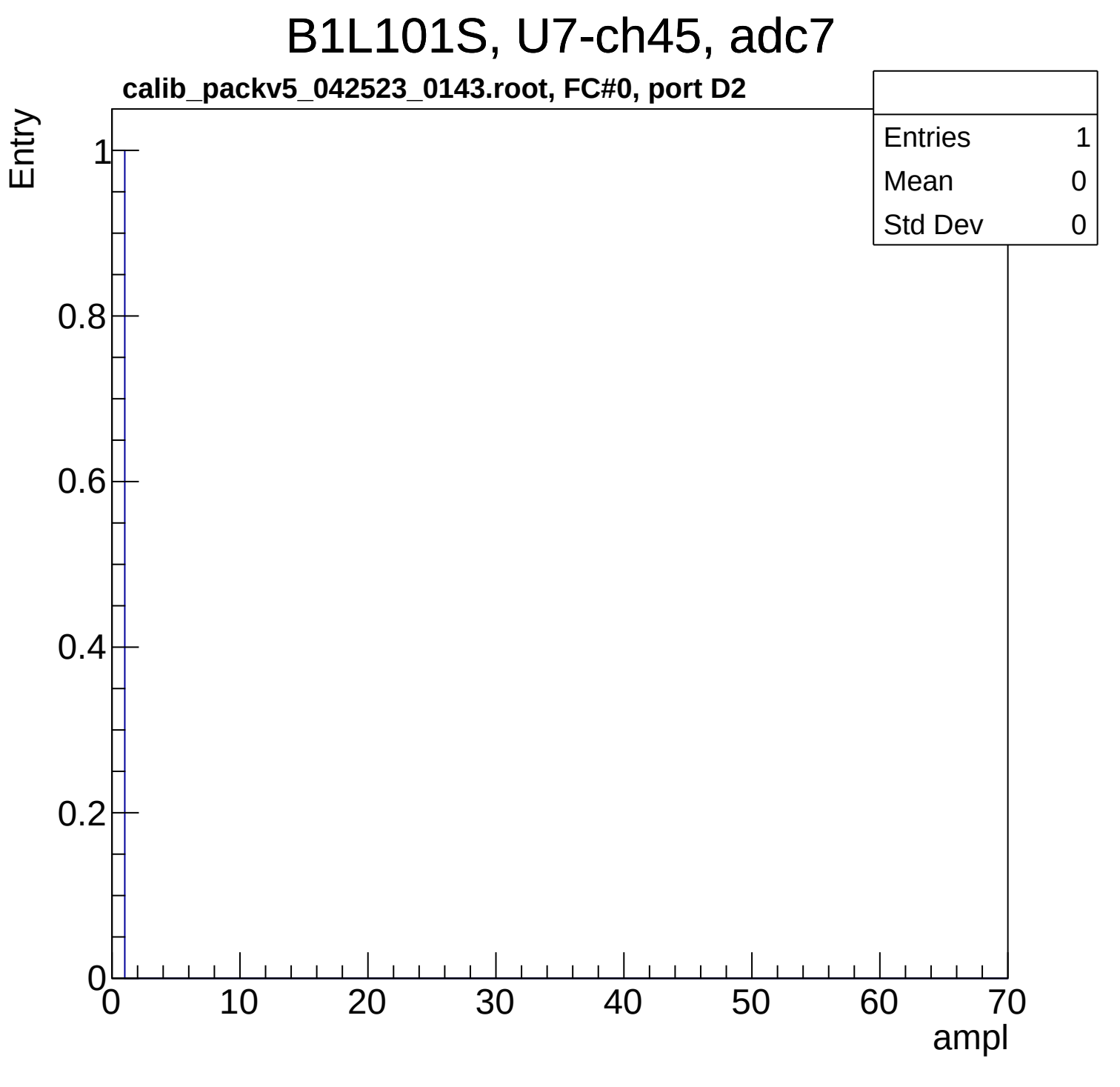

B1L101S, U7-ch45, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 43.49
Std Dev 3.294
Gaus mean : 44.3456
Gaus Width: 4.0976
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch45, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 50.69
Std Dev 3.534
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch45, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 55.88
Std Dev 3.372
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch45, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 43
Mean 58.79
Std Dev 9.377
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch45, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 61
Std Dev 1.581
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch45, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
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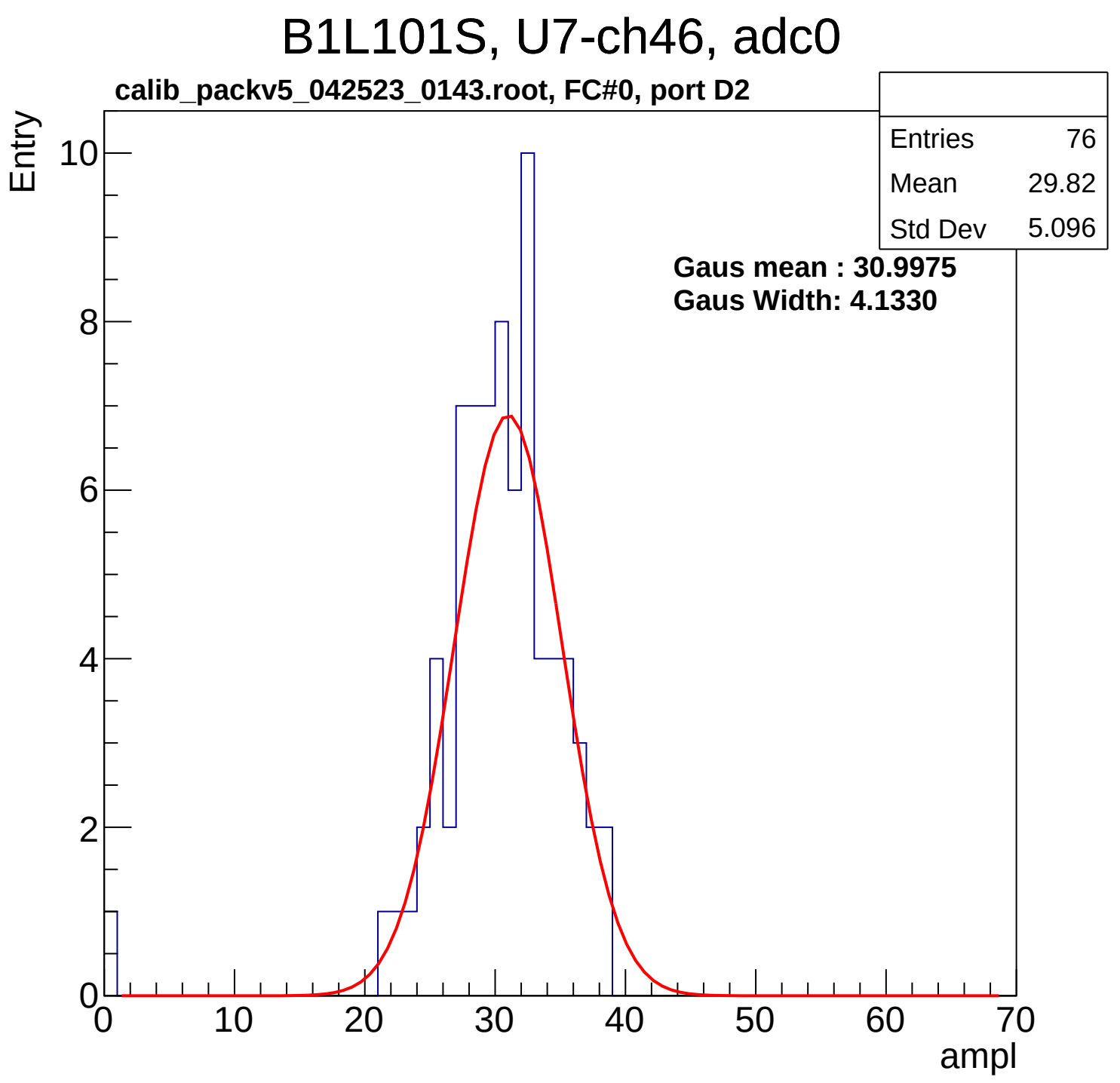
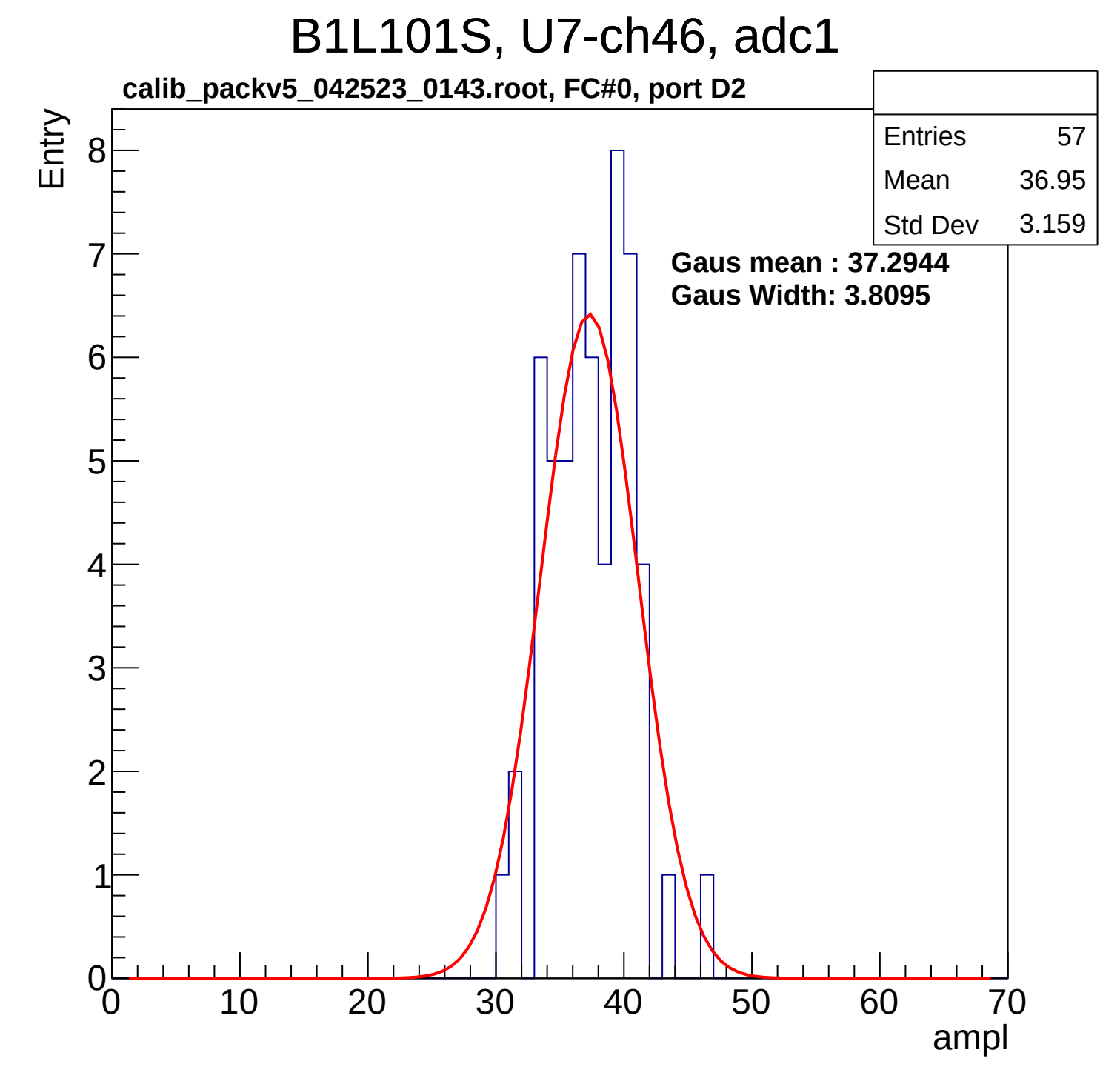
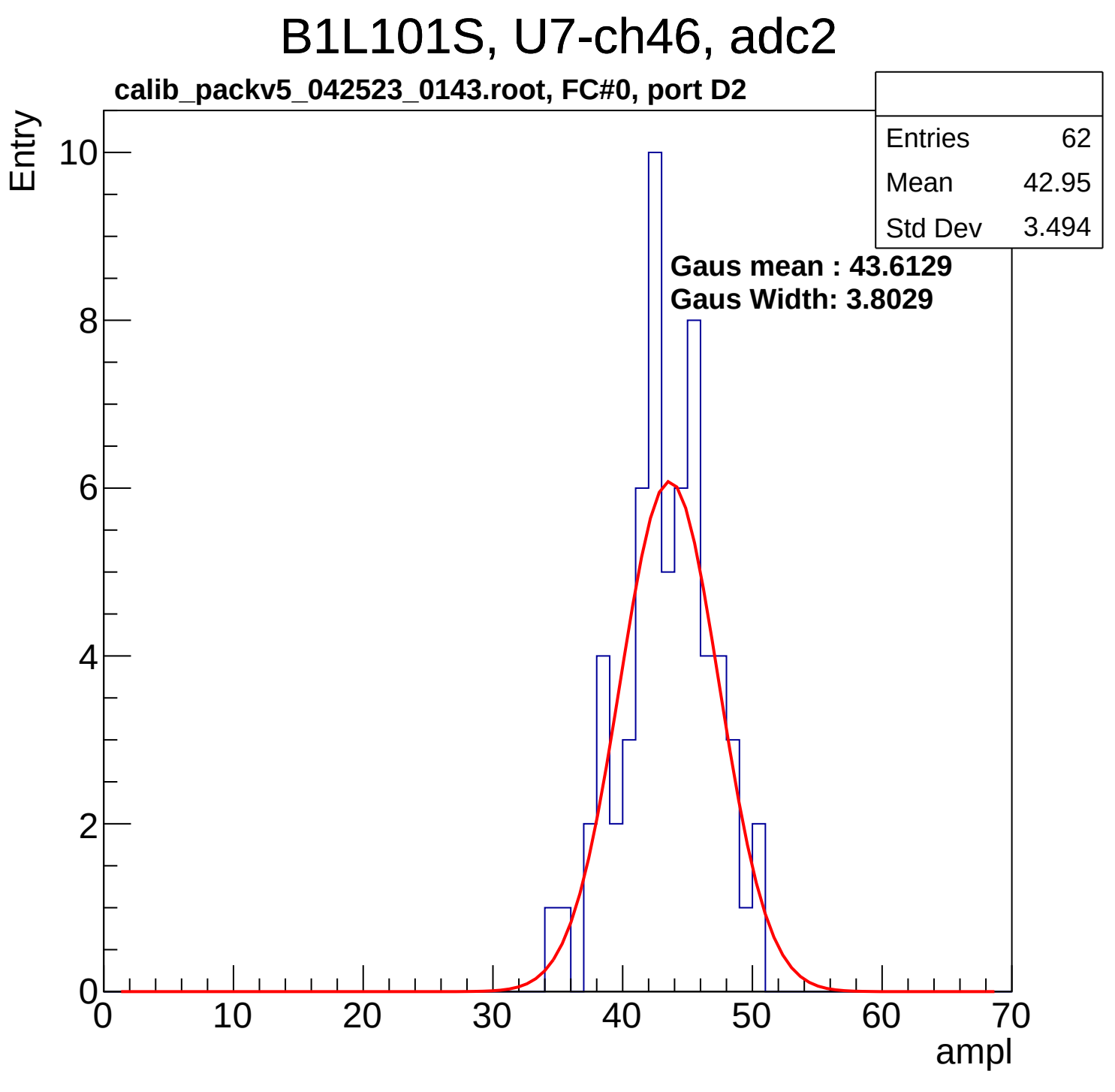
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch46, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 29.82
Std Dev 5.096
Gaus mean : 30.9975
Gaus Width: 4.1330
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch46, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 36.95
Std Dev 3.159
Gaus mean : 37.2944
Gaus Width: 3.8095
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch46, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 42.95
Std Dev 3.494
Gaus mean : 43.6129
Gaus Width: 3.8029
Entry
ampl
0
2
4
6
8
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0
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40
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60
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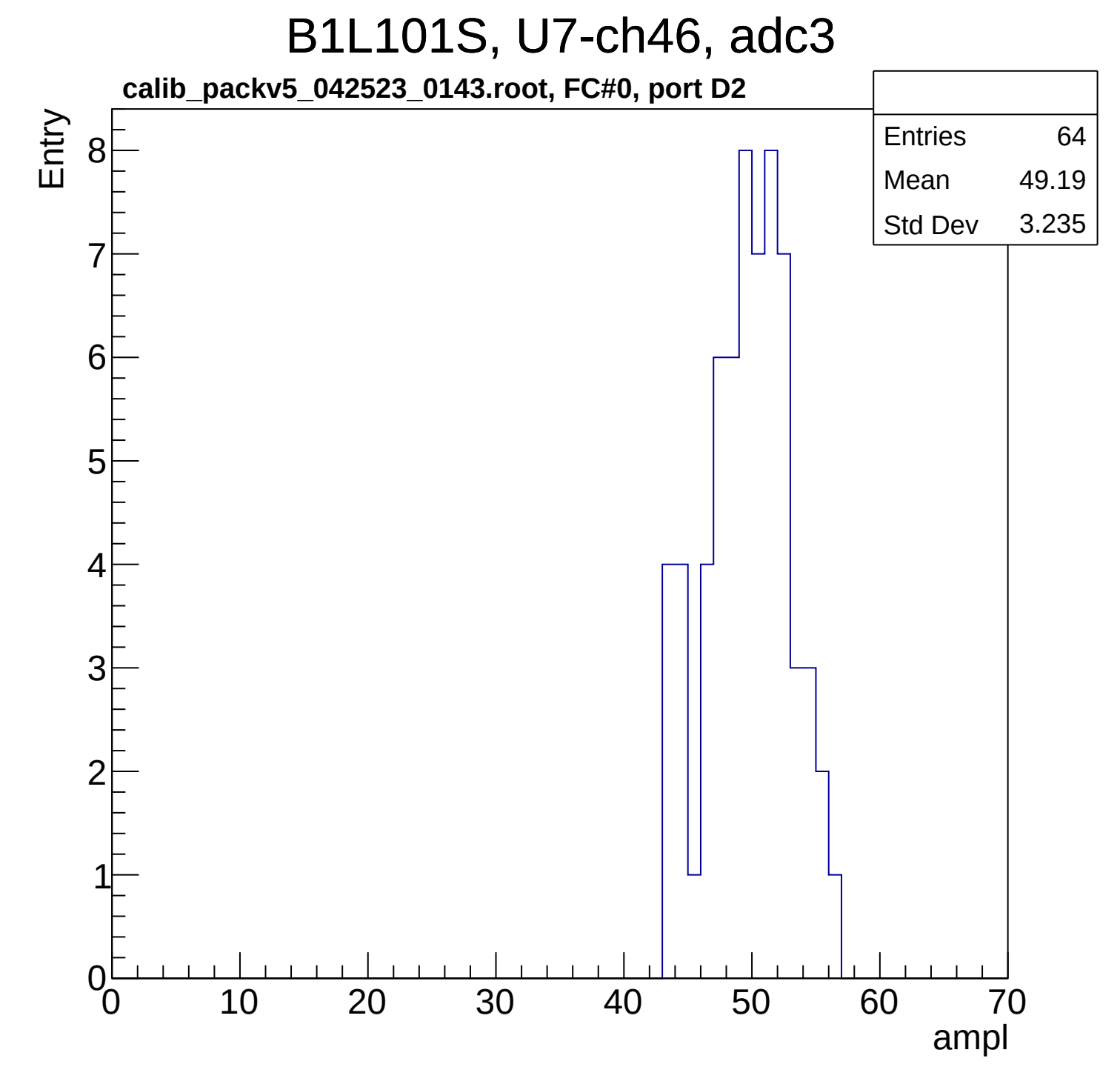
B1L101S, U7-ch46, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 49.19
Std Dev 3.235
Entry
ampl
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1
2
3
4
5
6
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8
0
10
20
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40
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60
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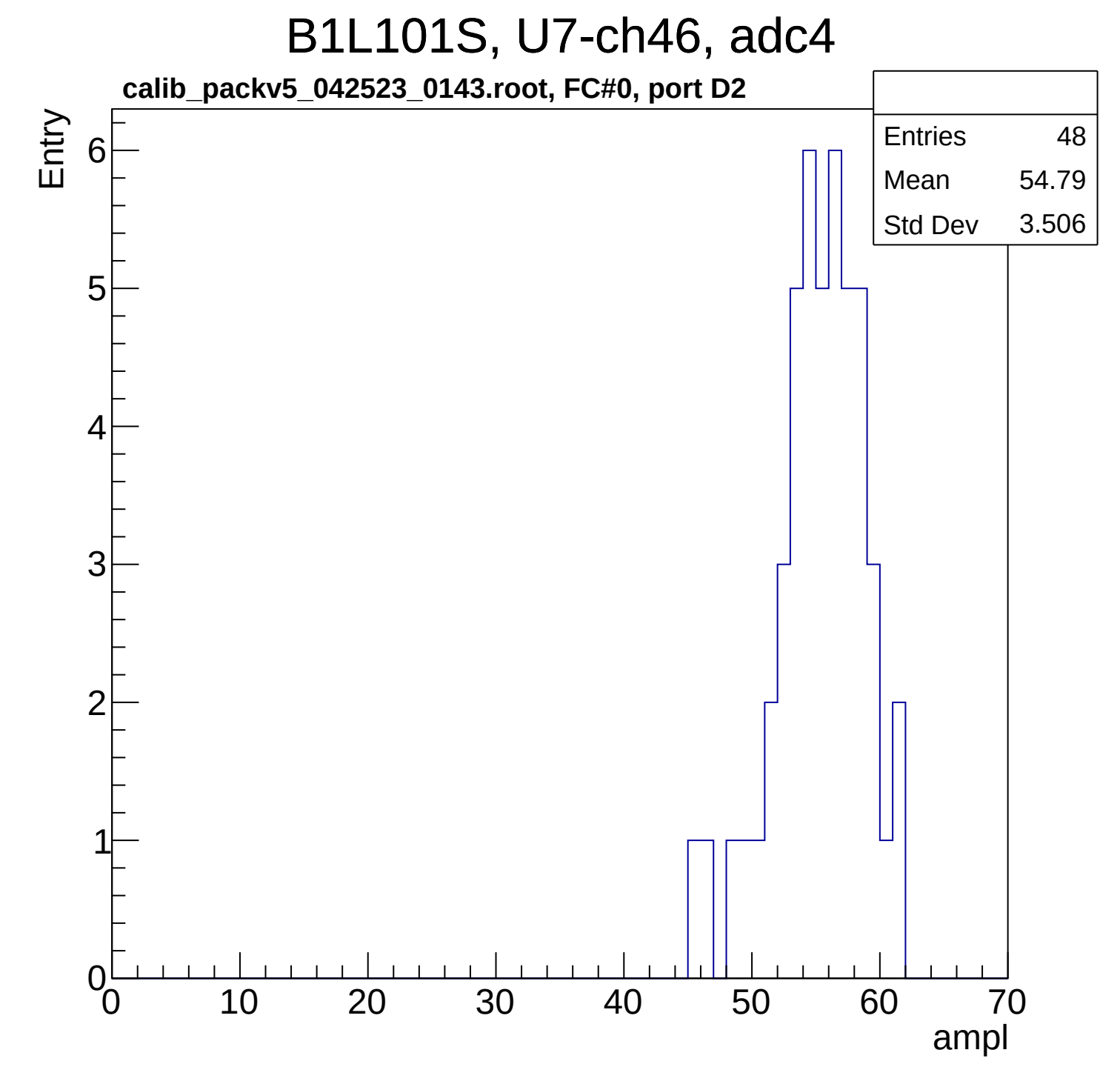
B1L101S, U7-ch46, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 54.79
Std Dev 3.506
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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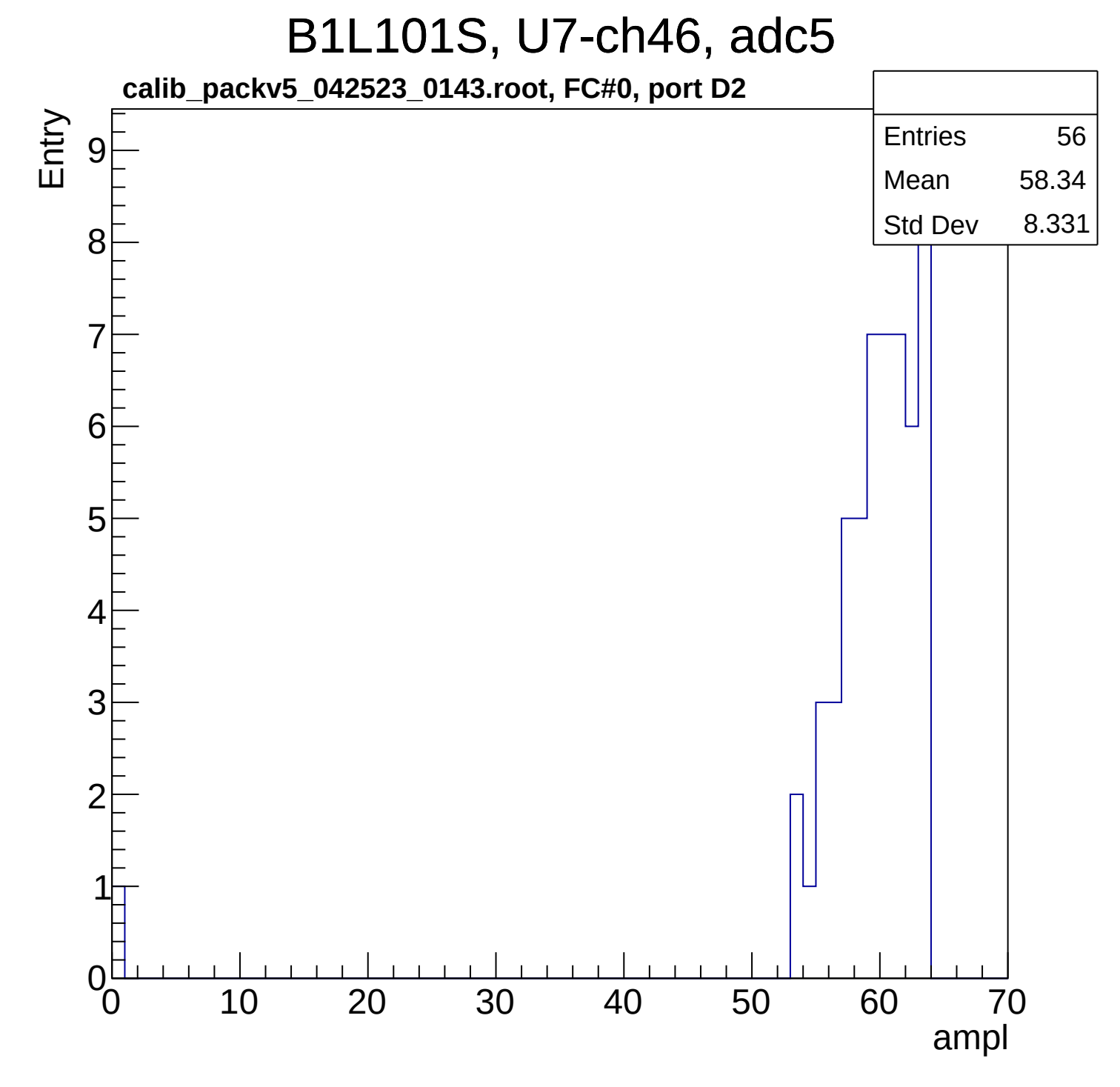
B1L101S, U7-ch46, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 58.34
Std Dev 8.331
Entry
ampl
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2
3
4
5
6
7
8
9
0
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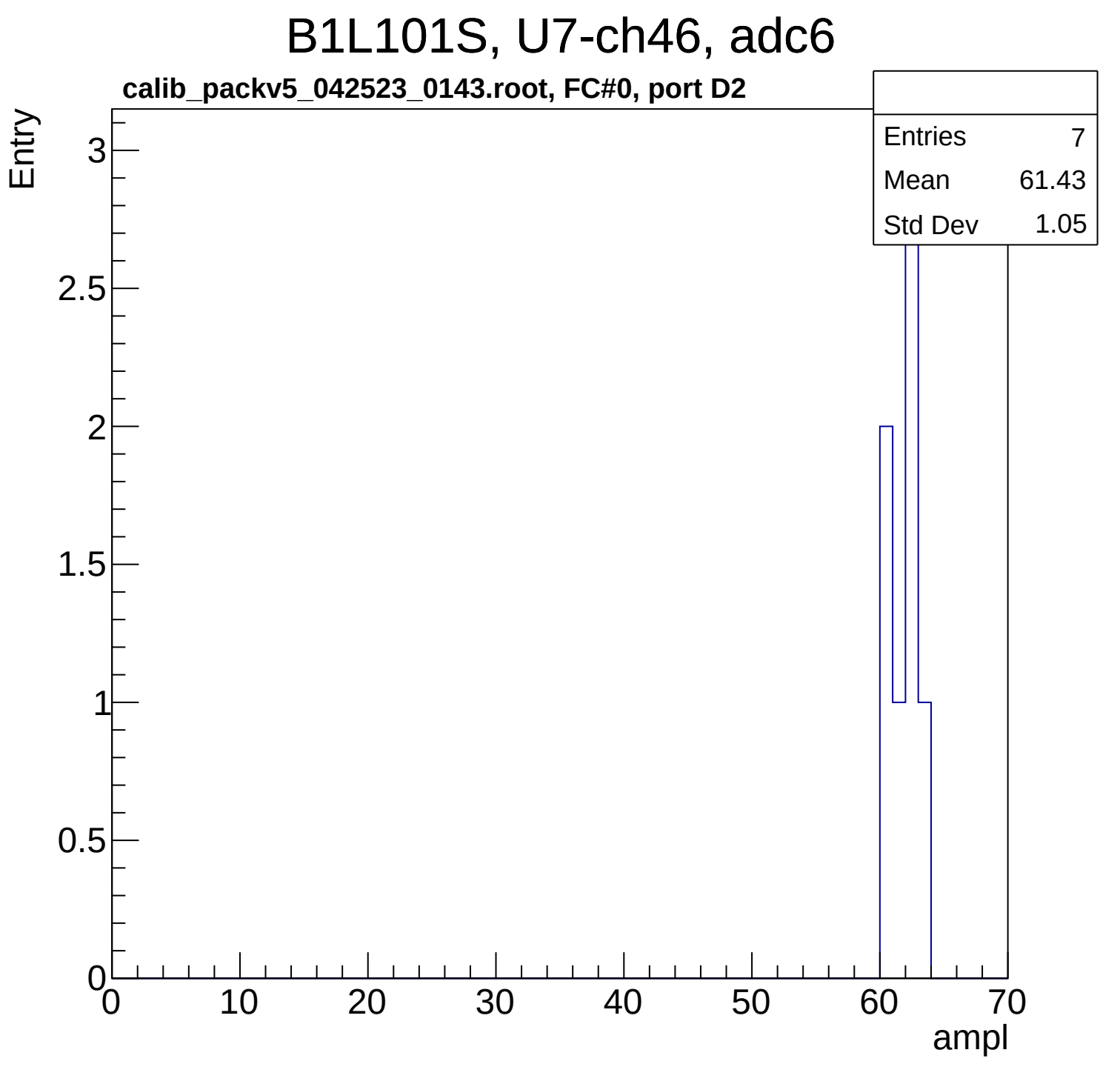
B1L101S, U7-ch46, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 61.43
Std Dev 1.05
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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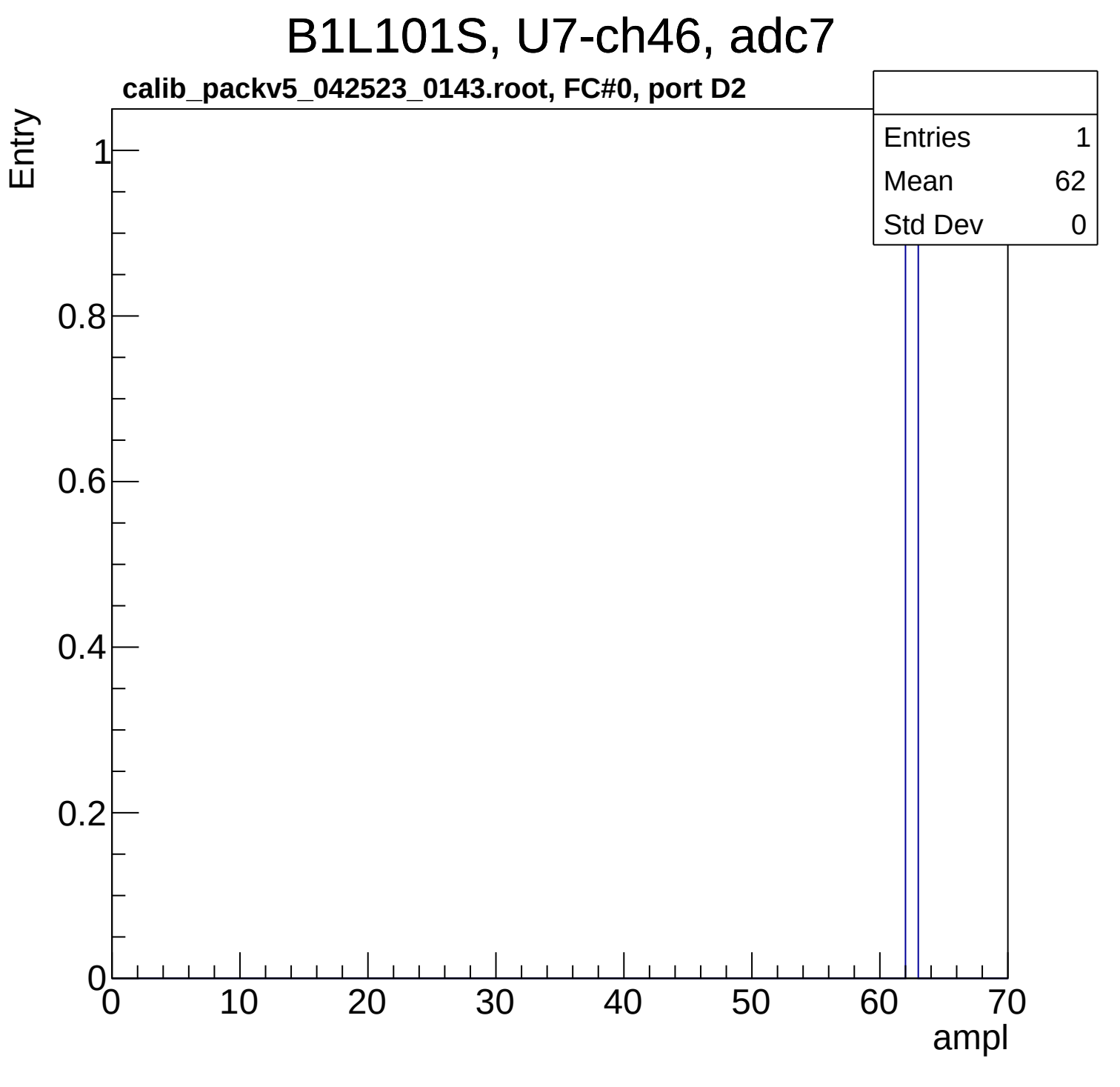
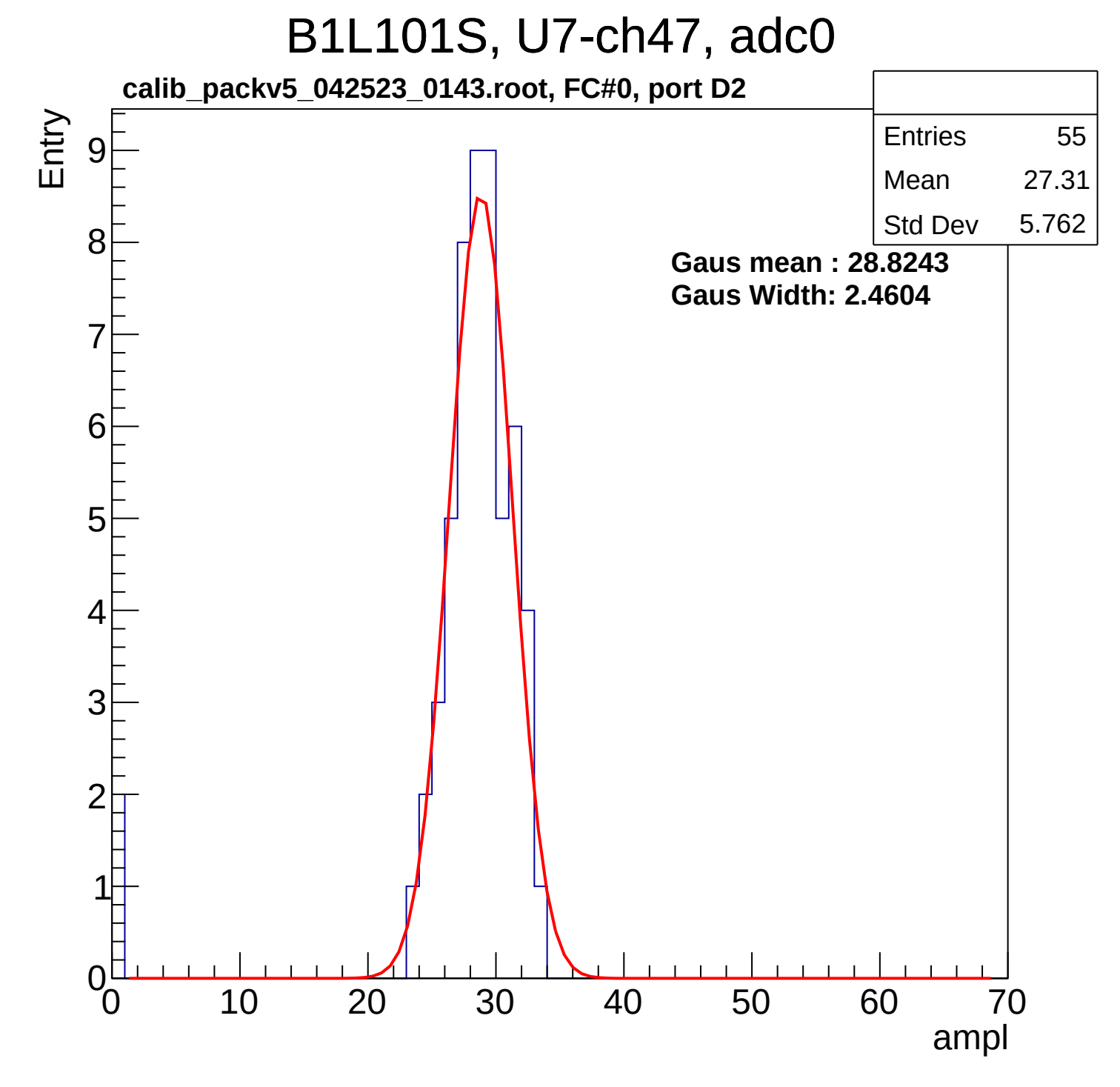

B1L101S, U7-ch46, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch47, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 27.31
Std Dev 5.762
Gaus mean : 28.8243
Gaus Width: 2.4604
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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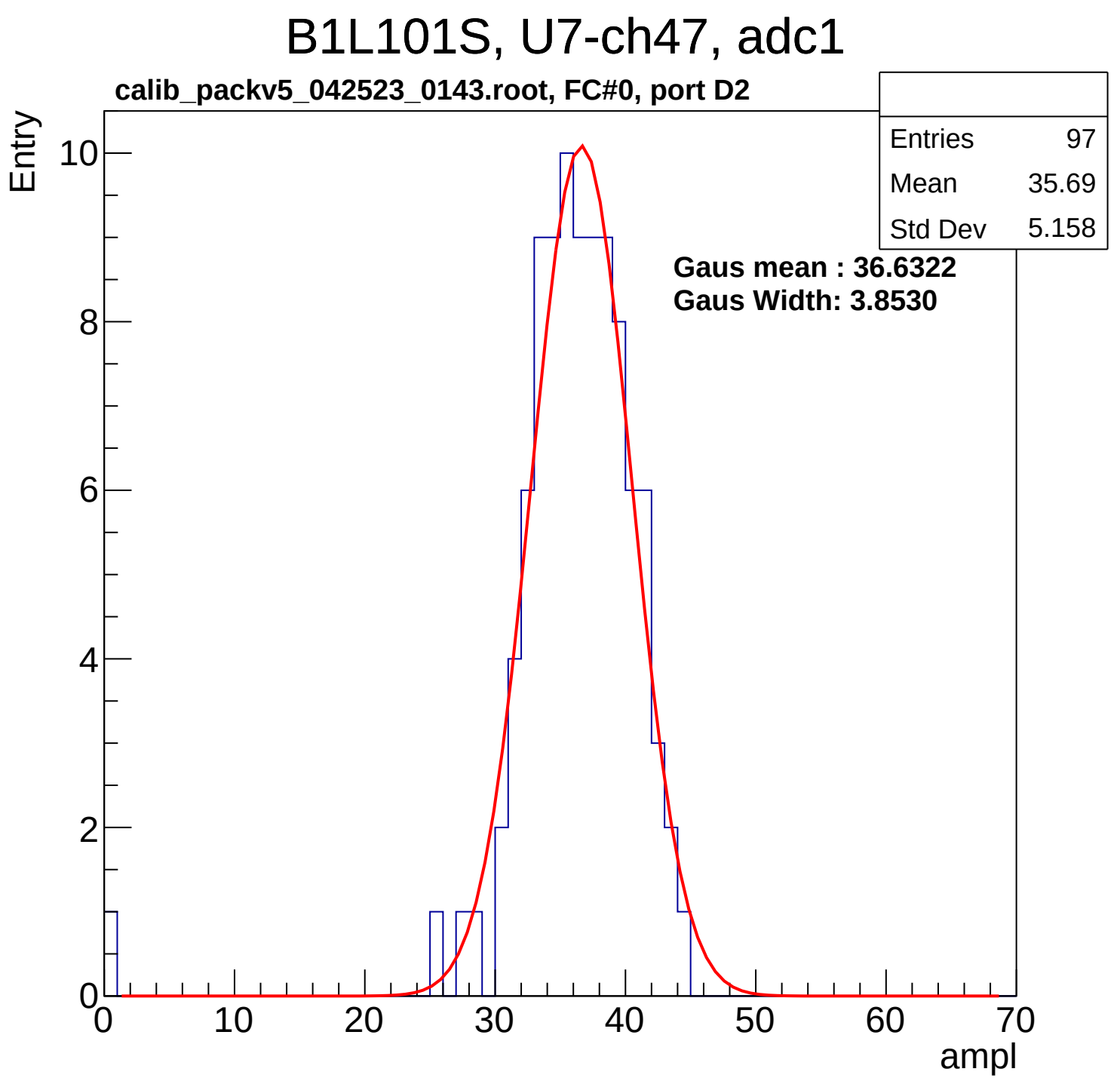
B1L101S, U7-ch47, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 97
Mean 35.69
Std Dev 5.158
Gaus mean : 36.6322
Gaus Width: 3.8530
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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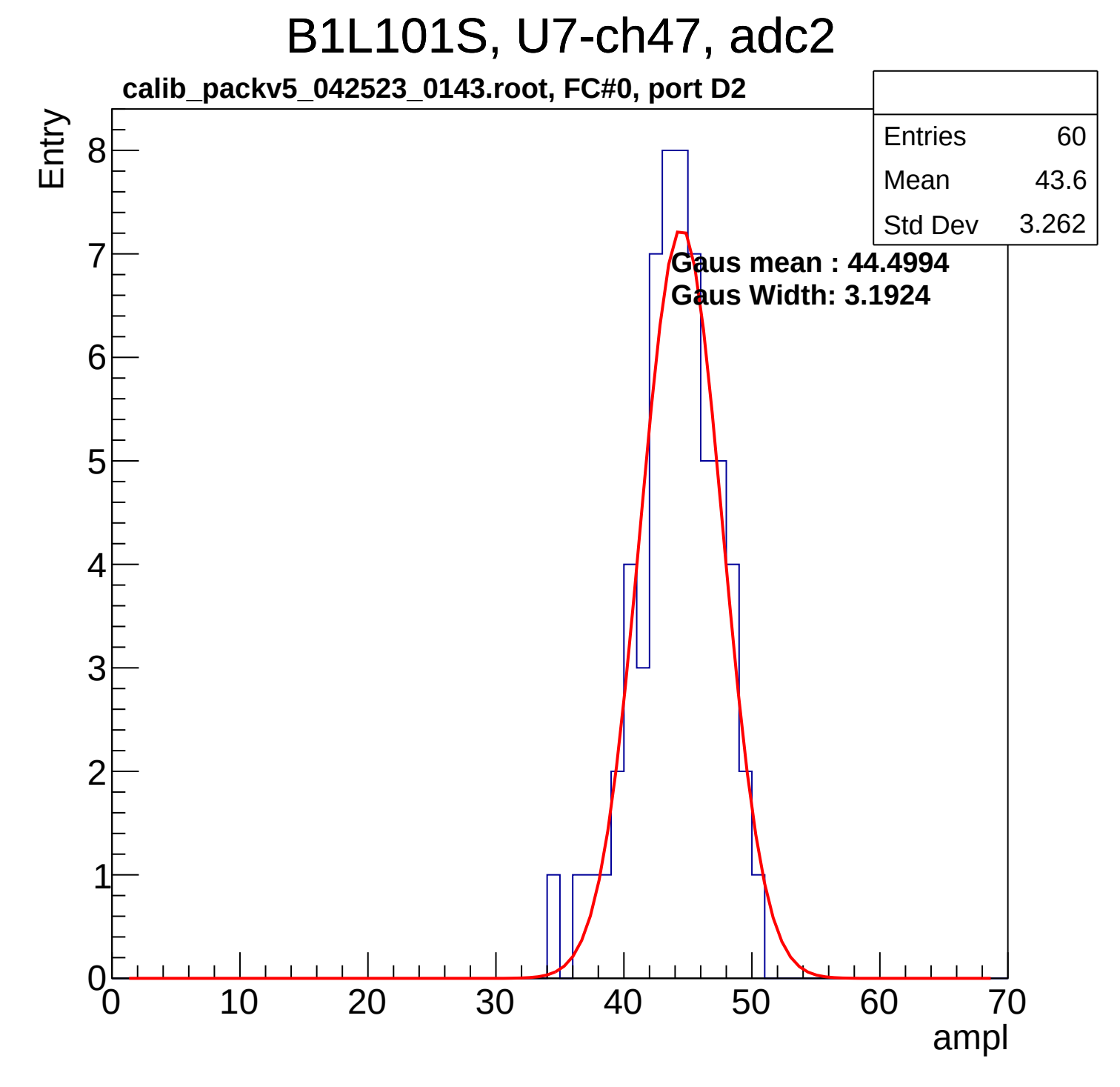
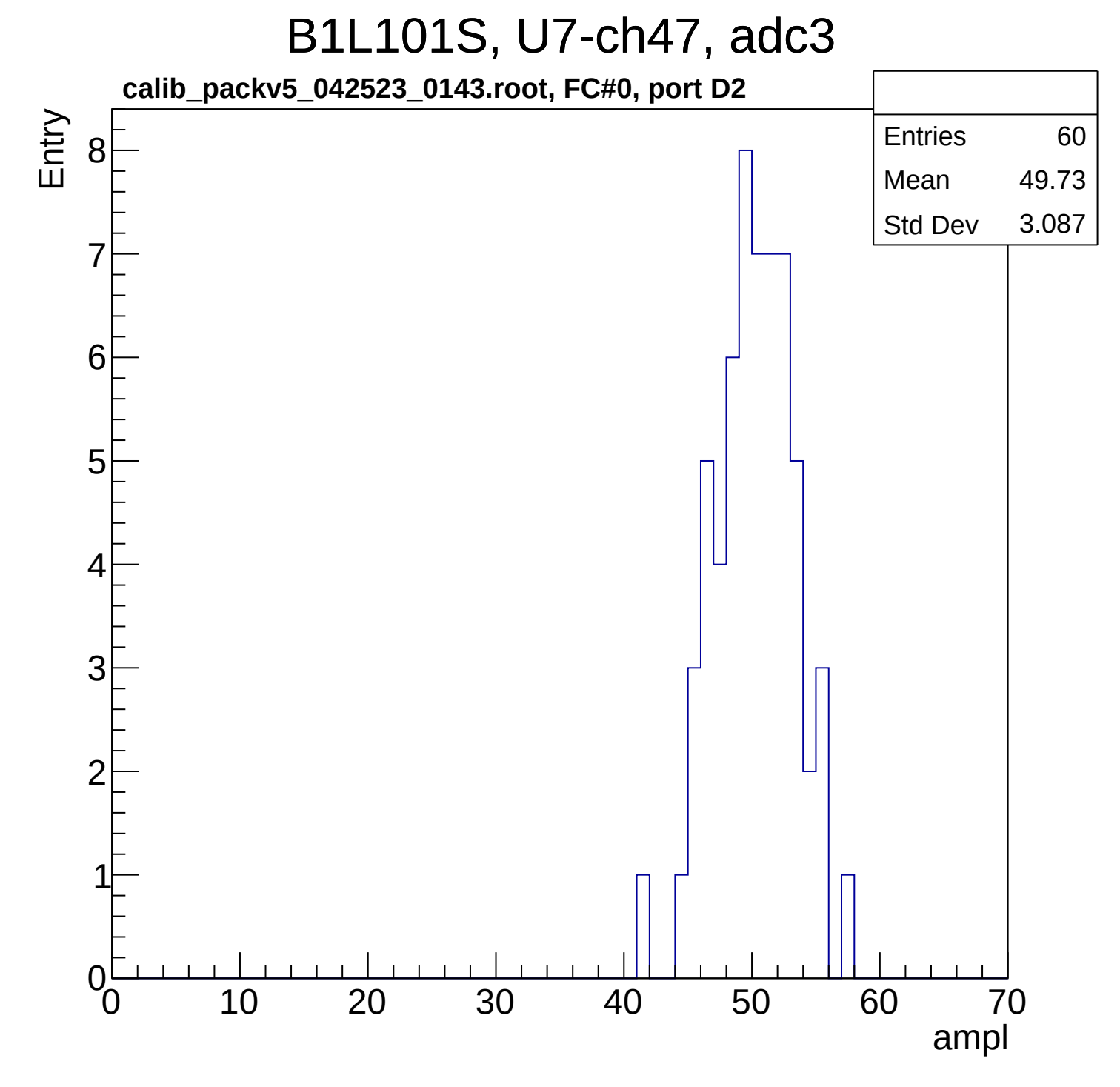
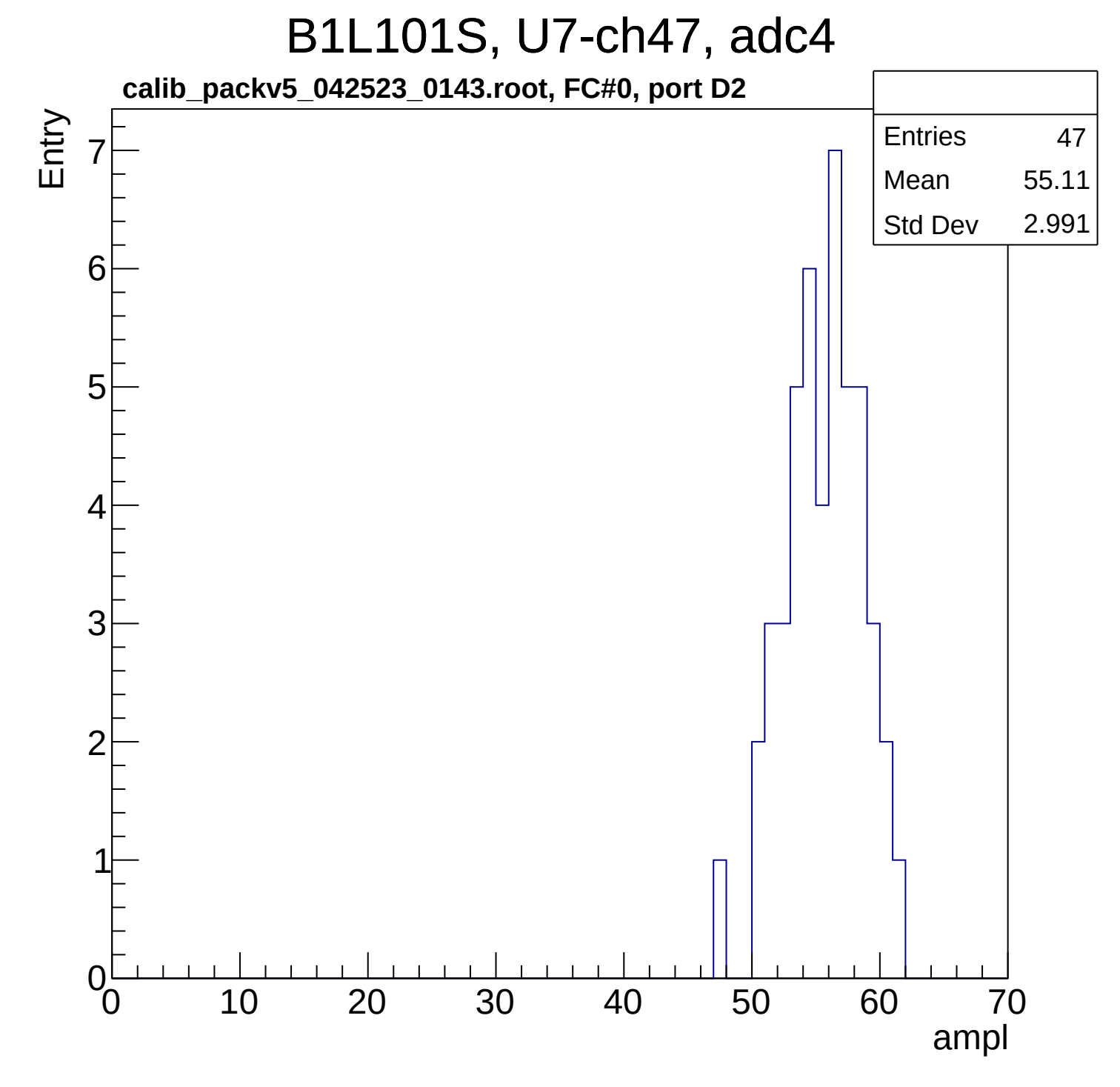

B1L101S, U7-ch47, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 43.6
Std Dev 3.262
Gaus mean : 44.4994
Gaus Width: 3.1924
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch47, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 49.73
Std Dev 3.087
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch47, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 55.11
Std Dev 2.991
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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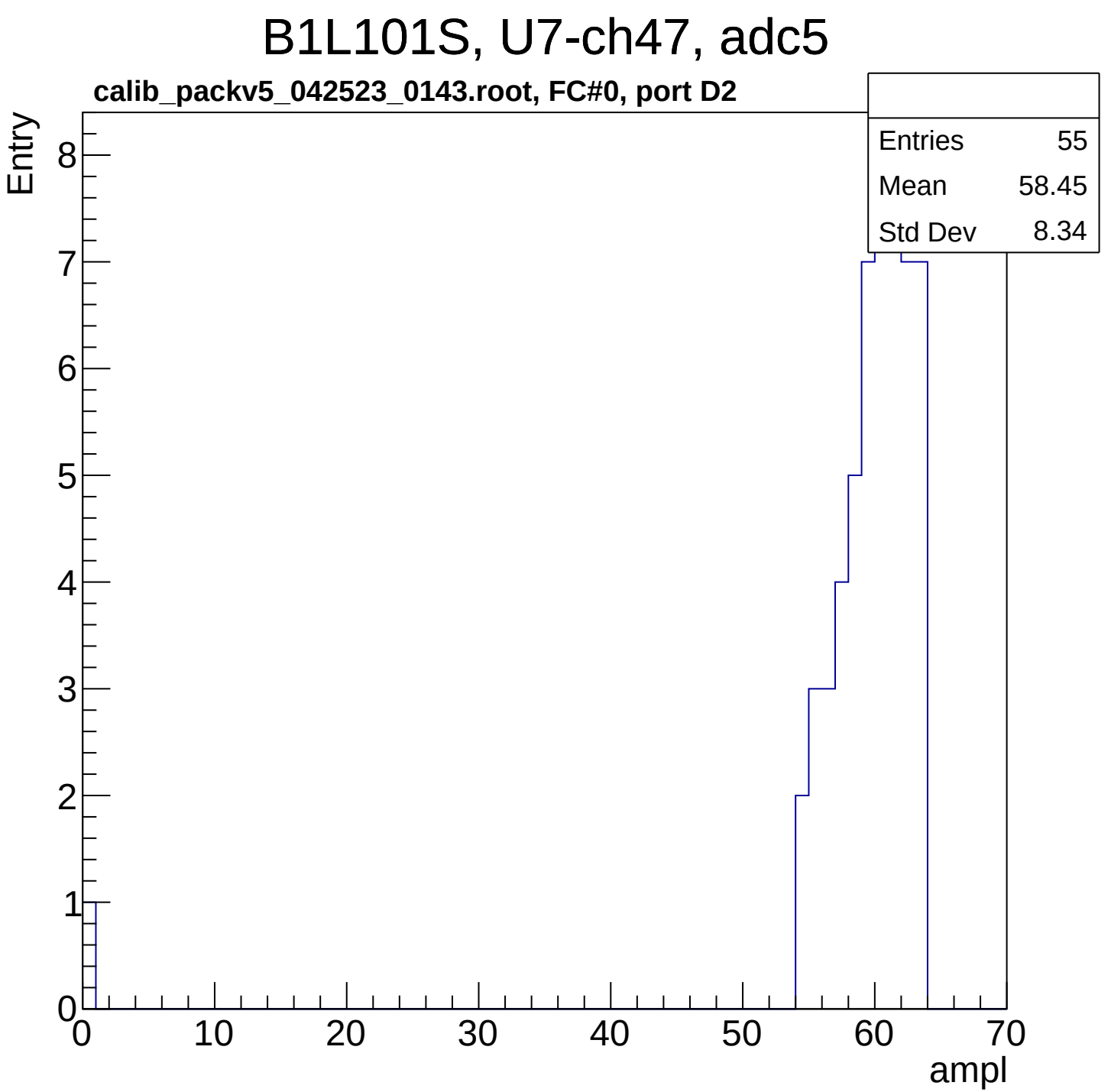
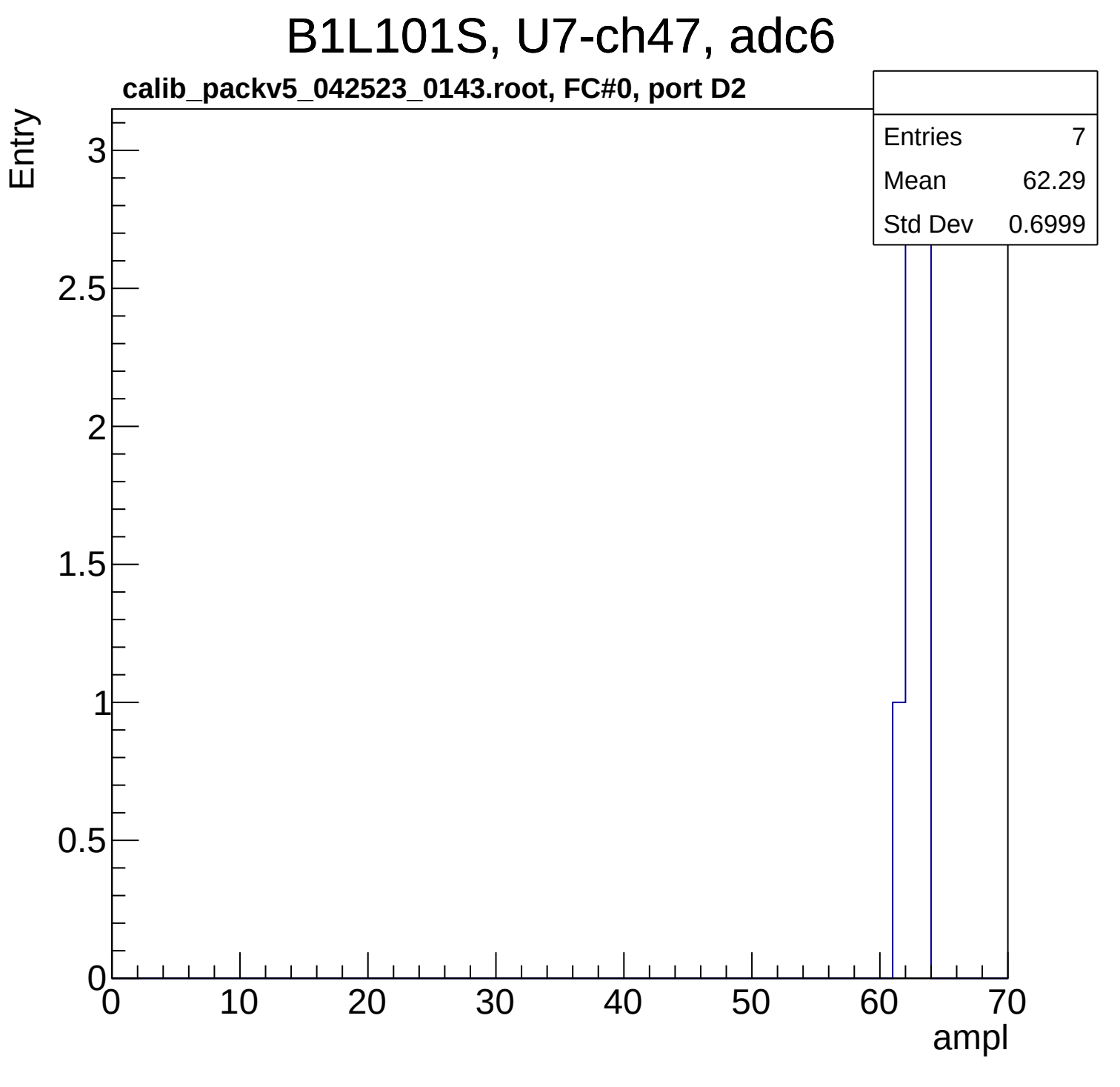

B1L101S, U7-ch47, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 58.45
Std Dev 8.34
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch47, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 62.29
Std Dev 0.6999
Entry
ampl
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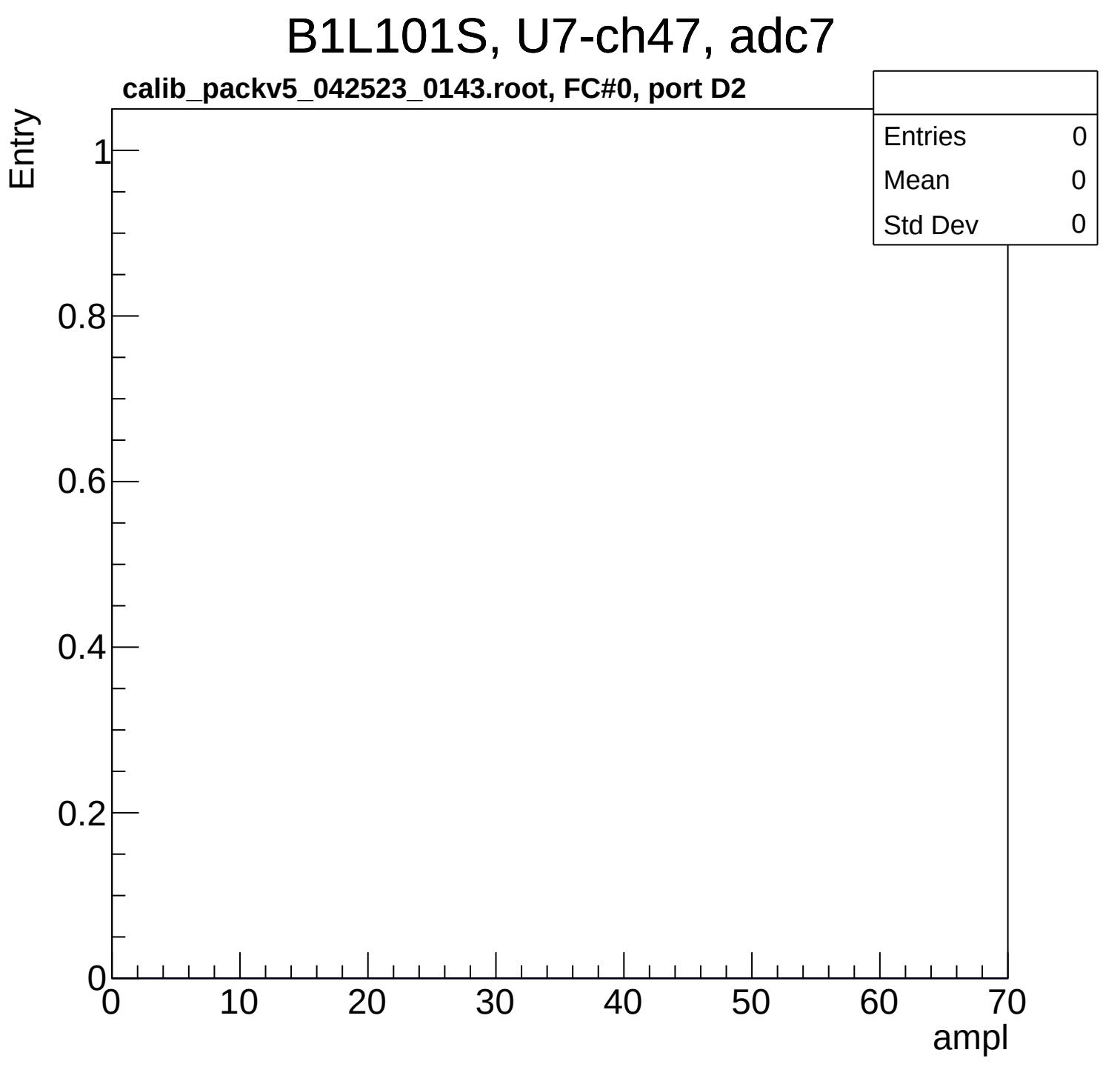
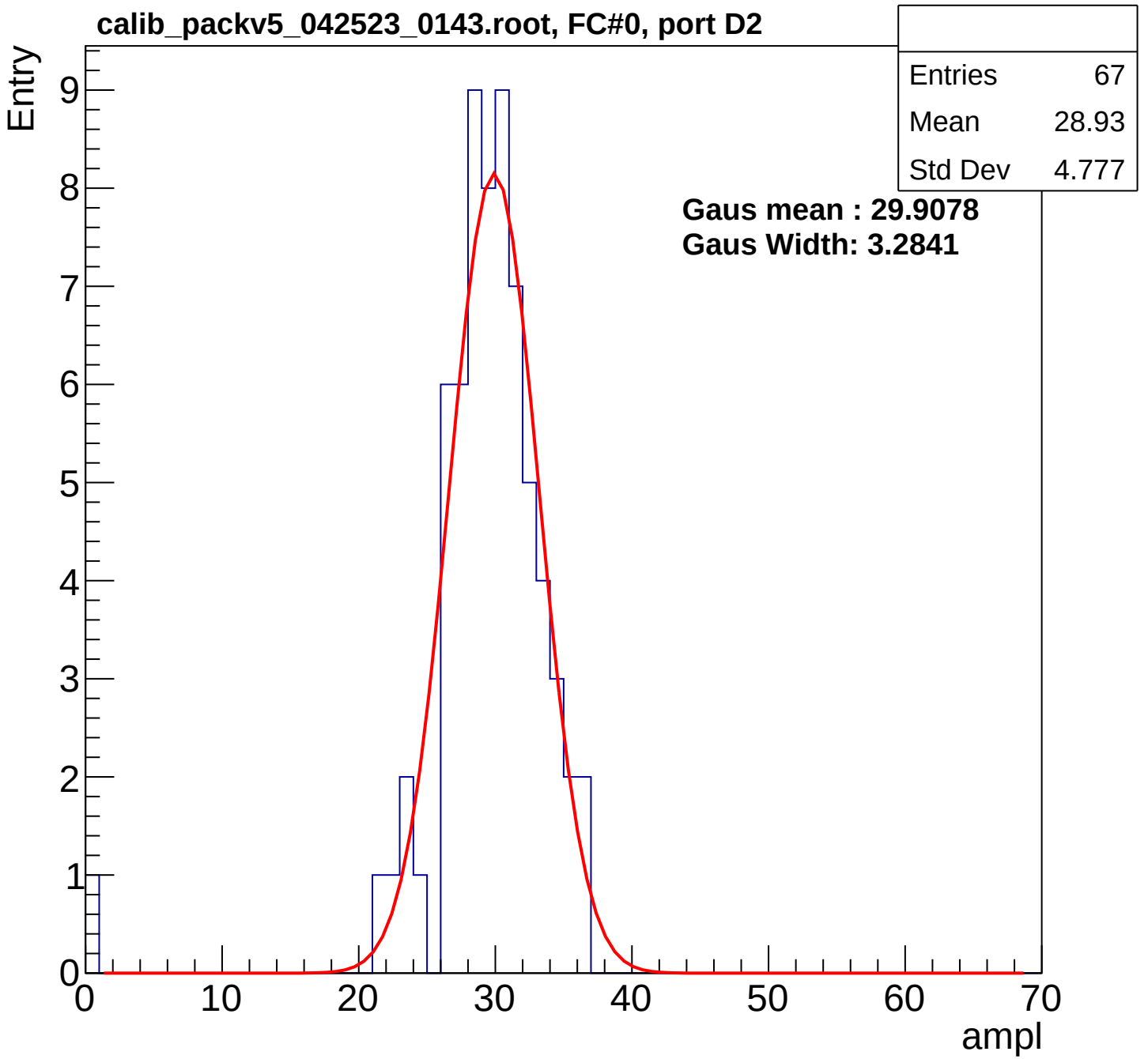
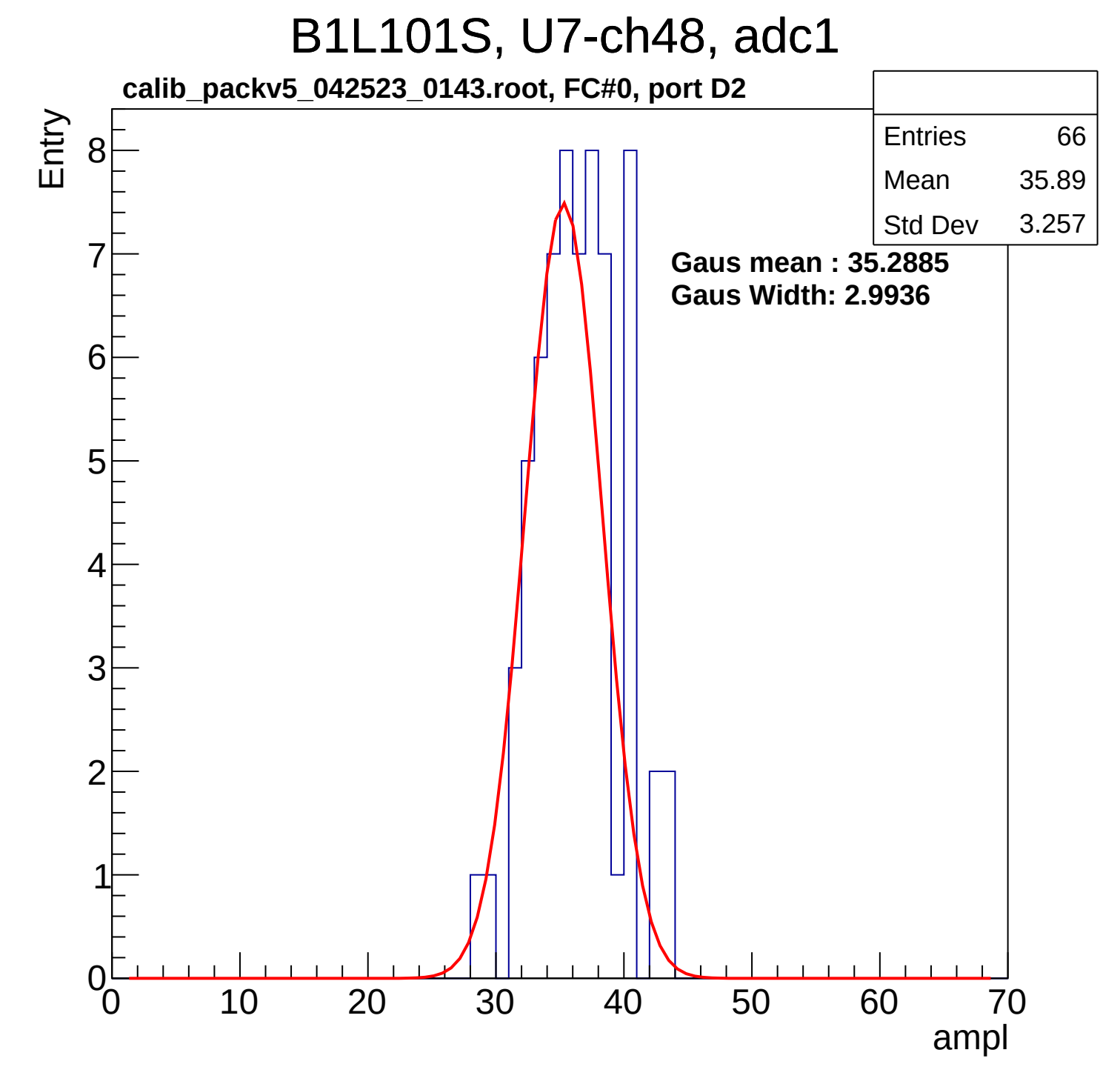
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U7-ch47, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch48, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 28.93
Std Dev 4.777
Gaus mean : 29.9078
Gaus Width: 3.2841
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch48, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 35.89
Std Dev 3.257
Gaus mean : 35.2885
Gaus Width: 2.9936
Entry
ampl
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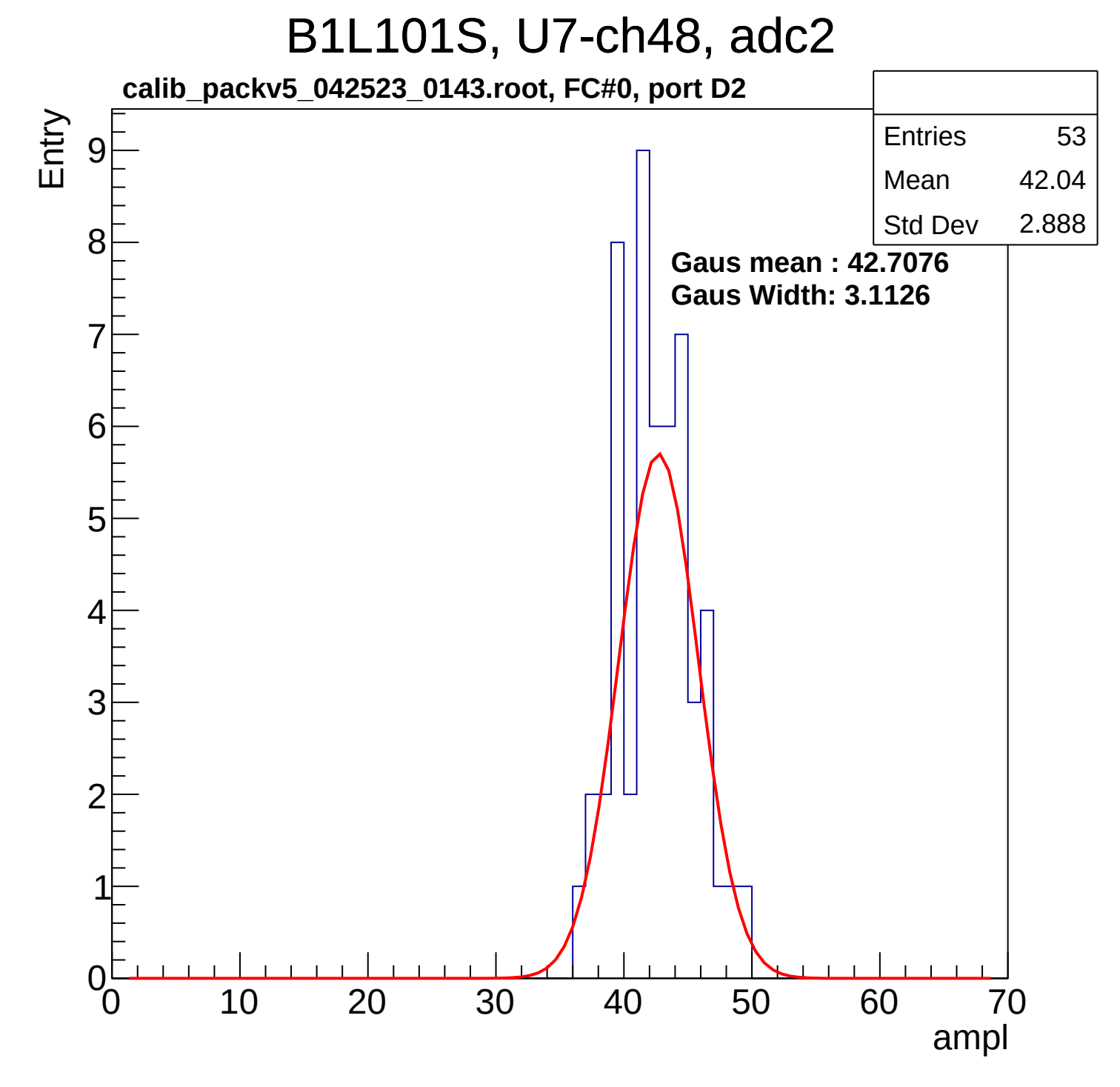
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch48, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 42.04
Std Dev 2.888
Gaus mean : 42.7076
Gaus Width: 3.1126
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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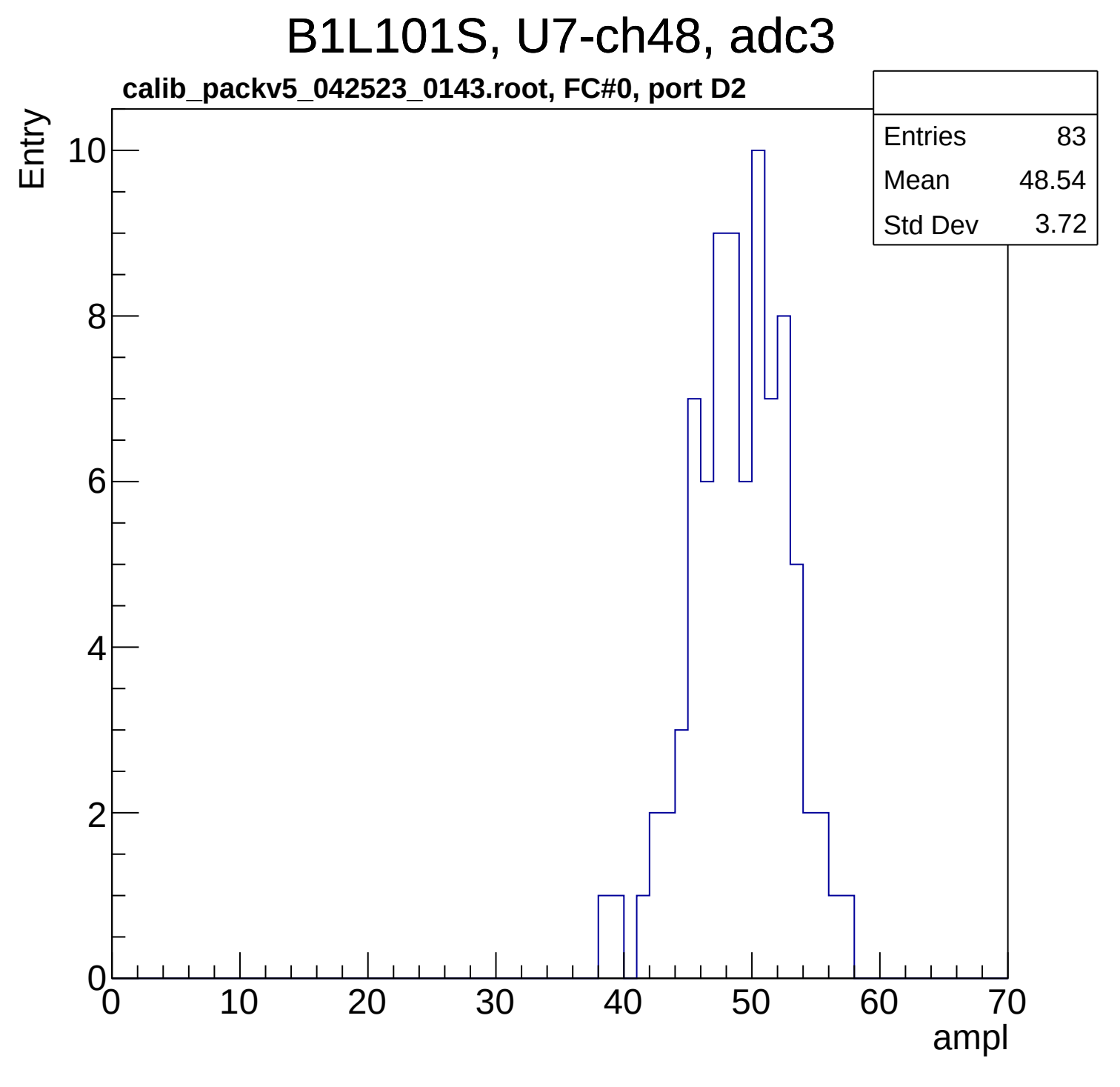
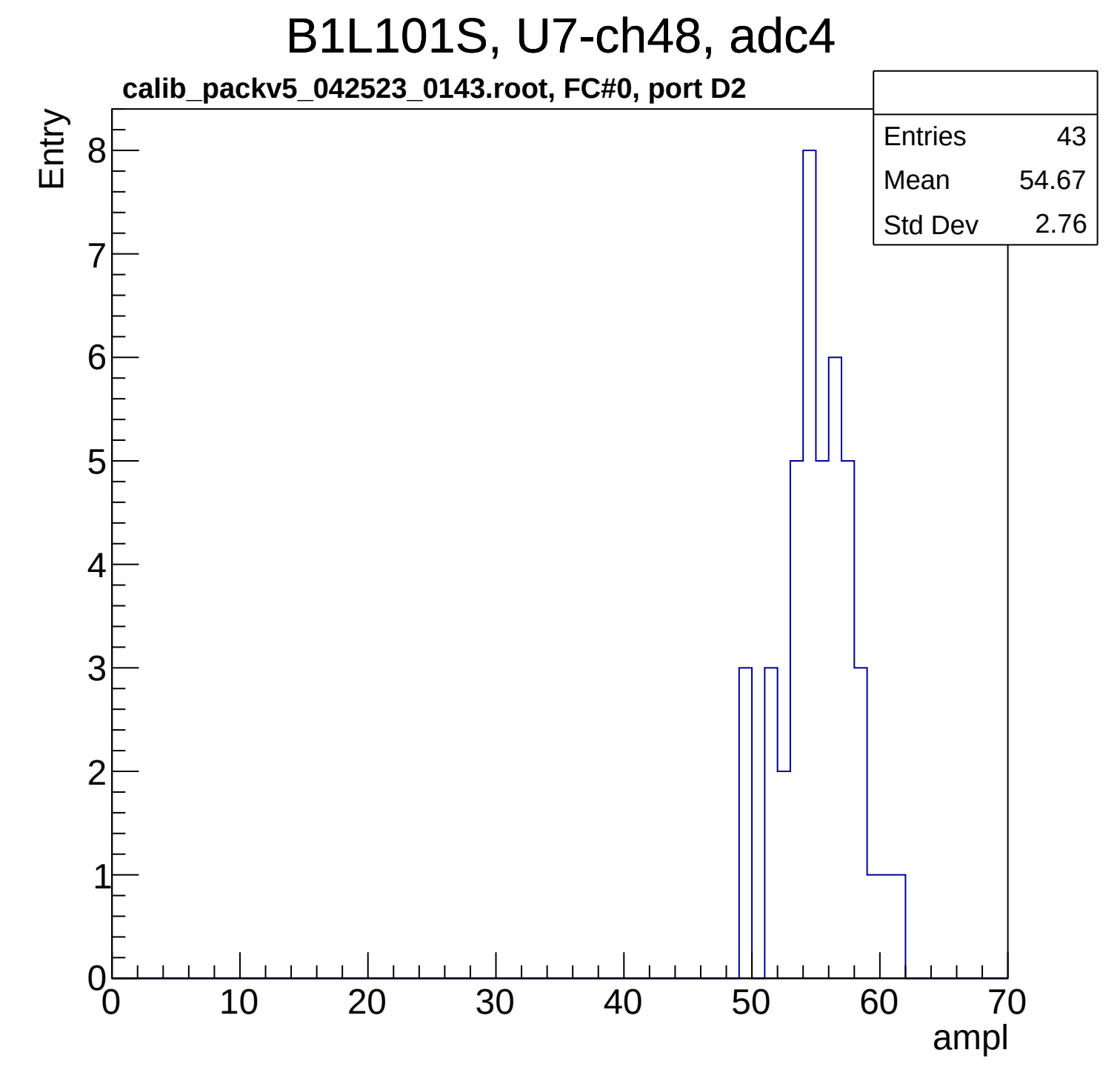
40
50
60
70


B1L101S, U7-ch48, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 83
Mean 48.54
Std Dev 3.72
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch48, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 43
Mean 54.67
Std Dev 2.76
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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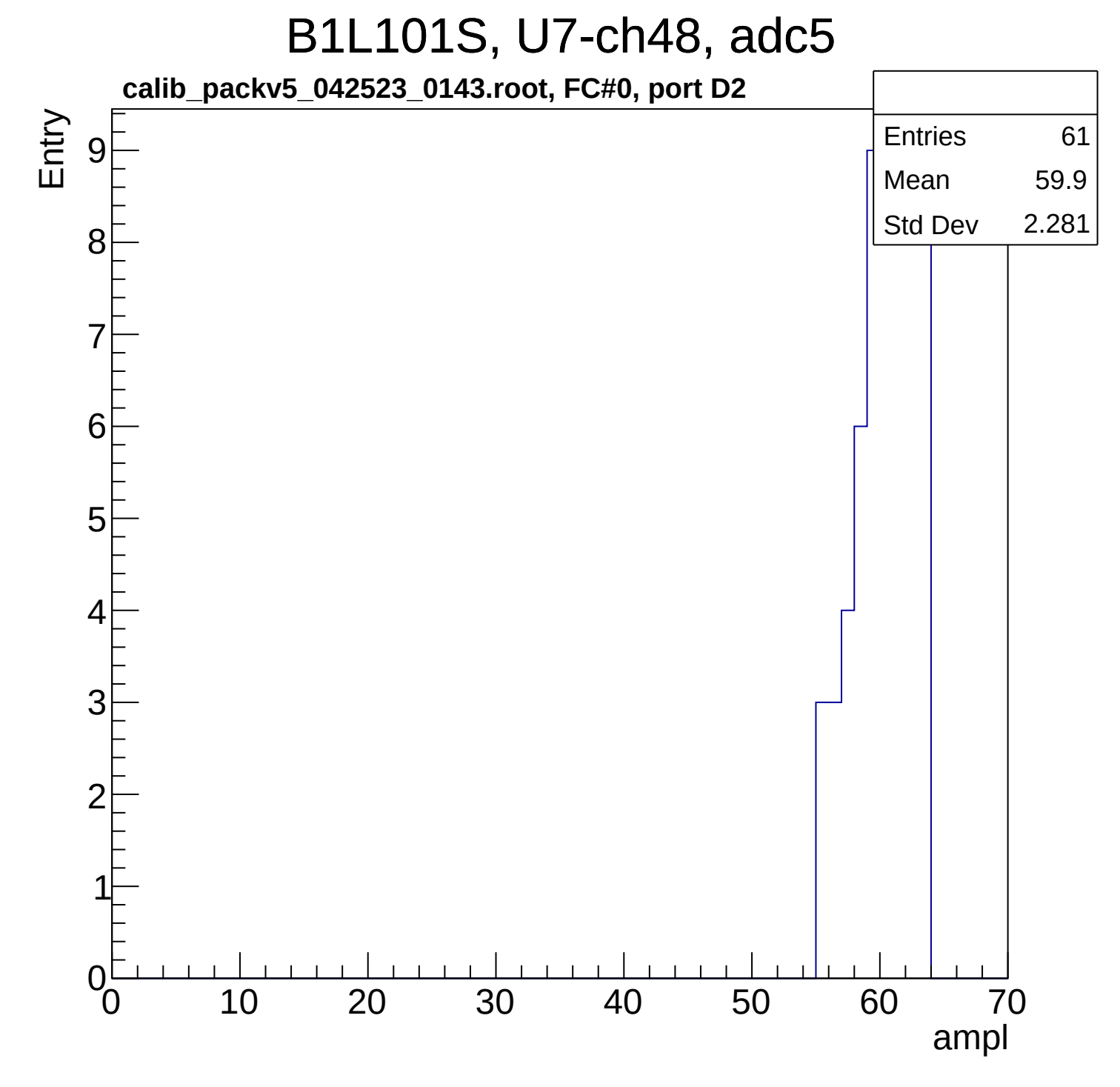
40
50
60
70


B1L101S, U7-ch48, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 59.9
Std Dev 2.281
Entry
ampl
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6
7
8
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0
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60
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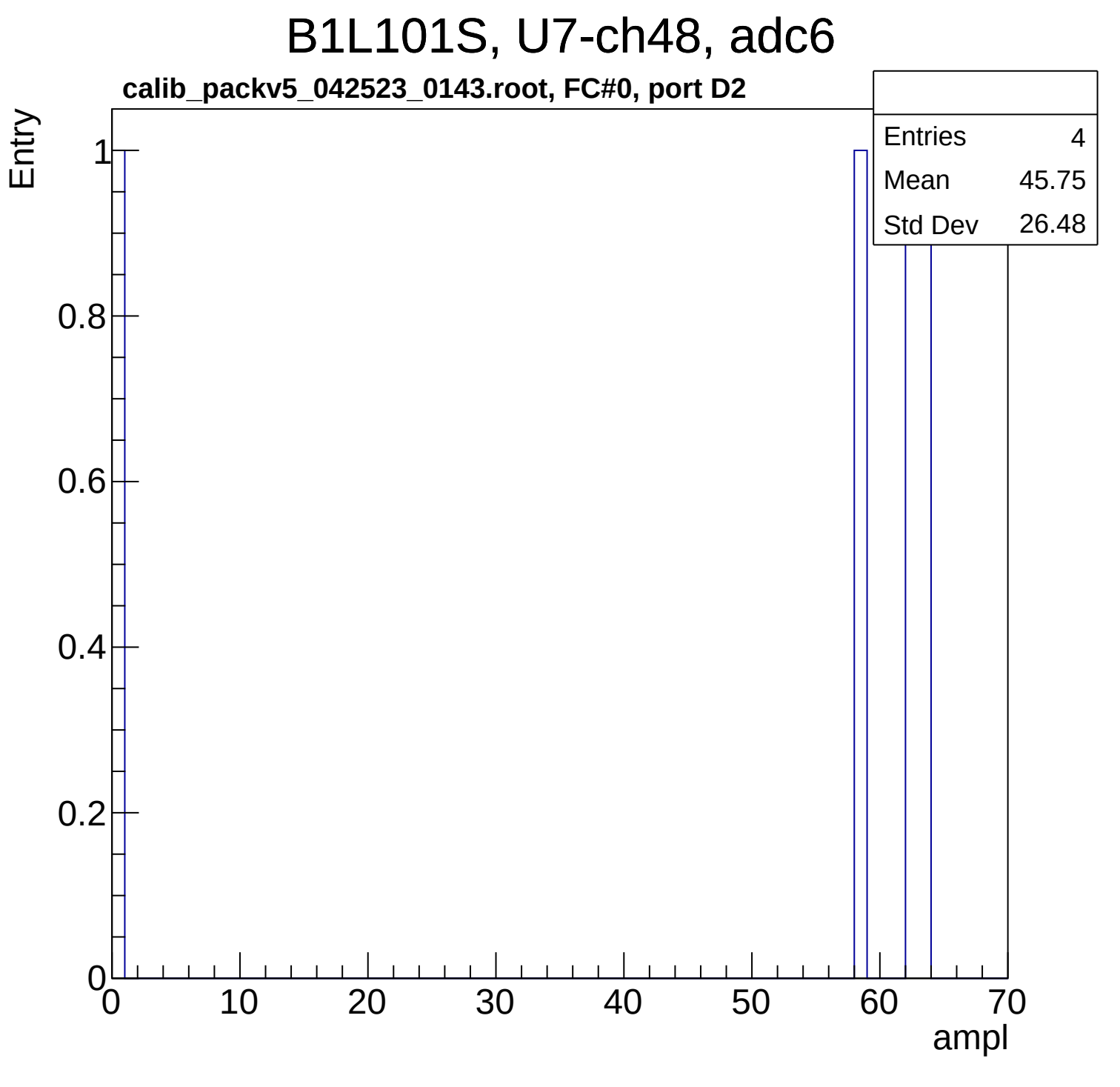
B1L101S, U7-ch48, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 45.75
Std Dev 26.48
Entry
ampl
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0.4
0.6
0.8
1
0
10
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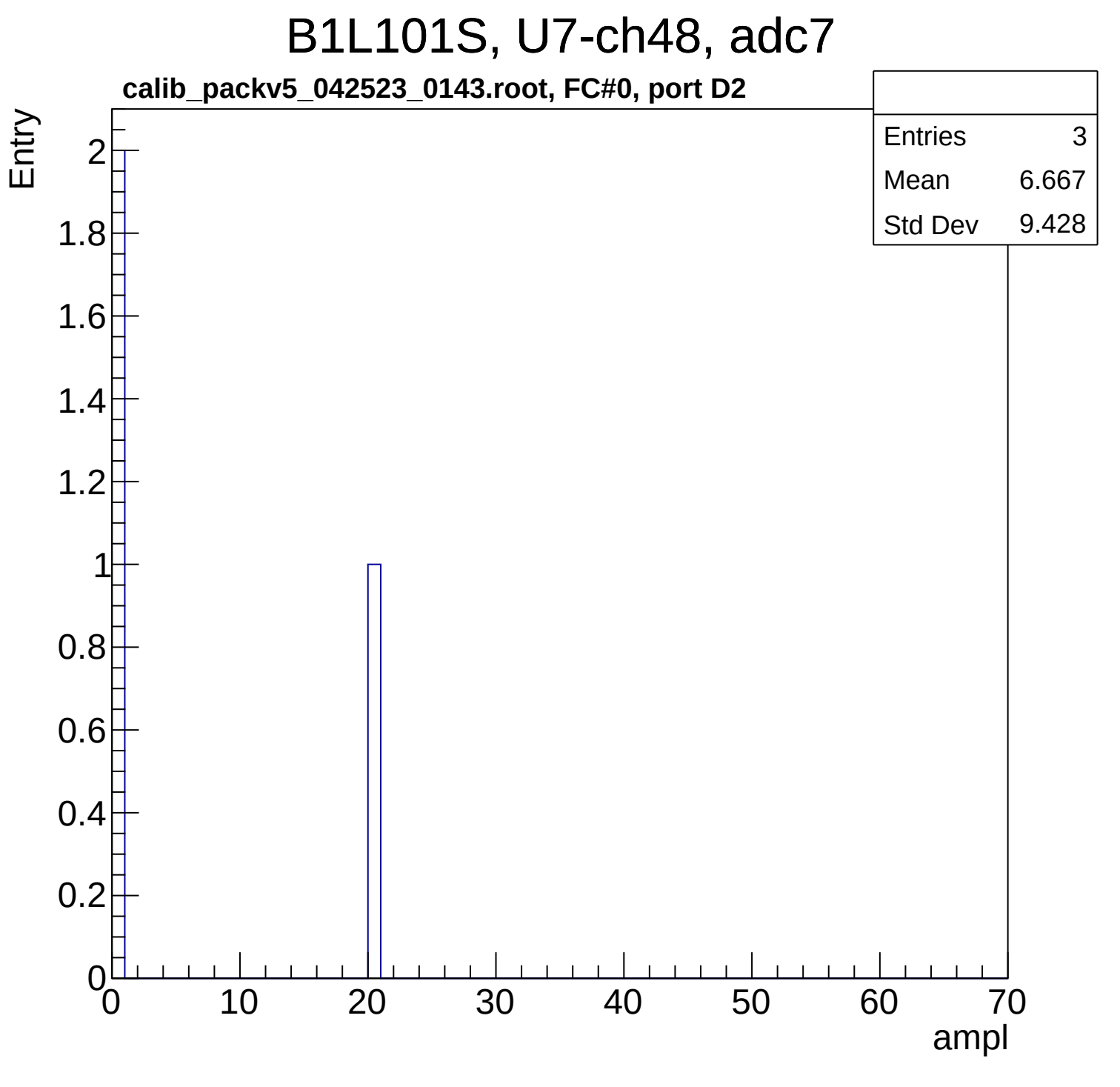
40
50
60
70


B1L101S, U7-ch48, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 6.667
Std Dev 9.428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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40
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60
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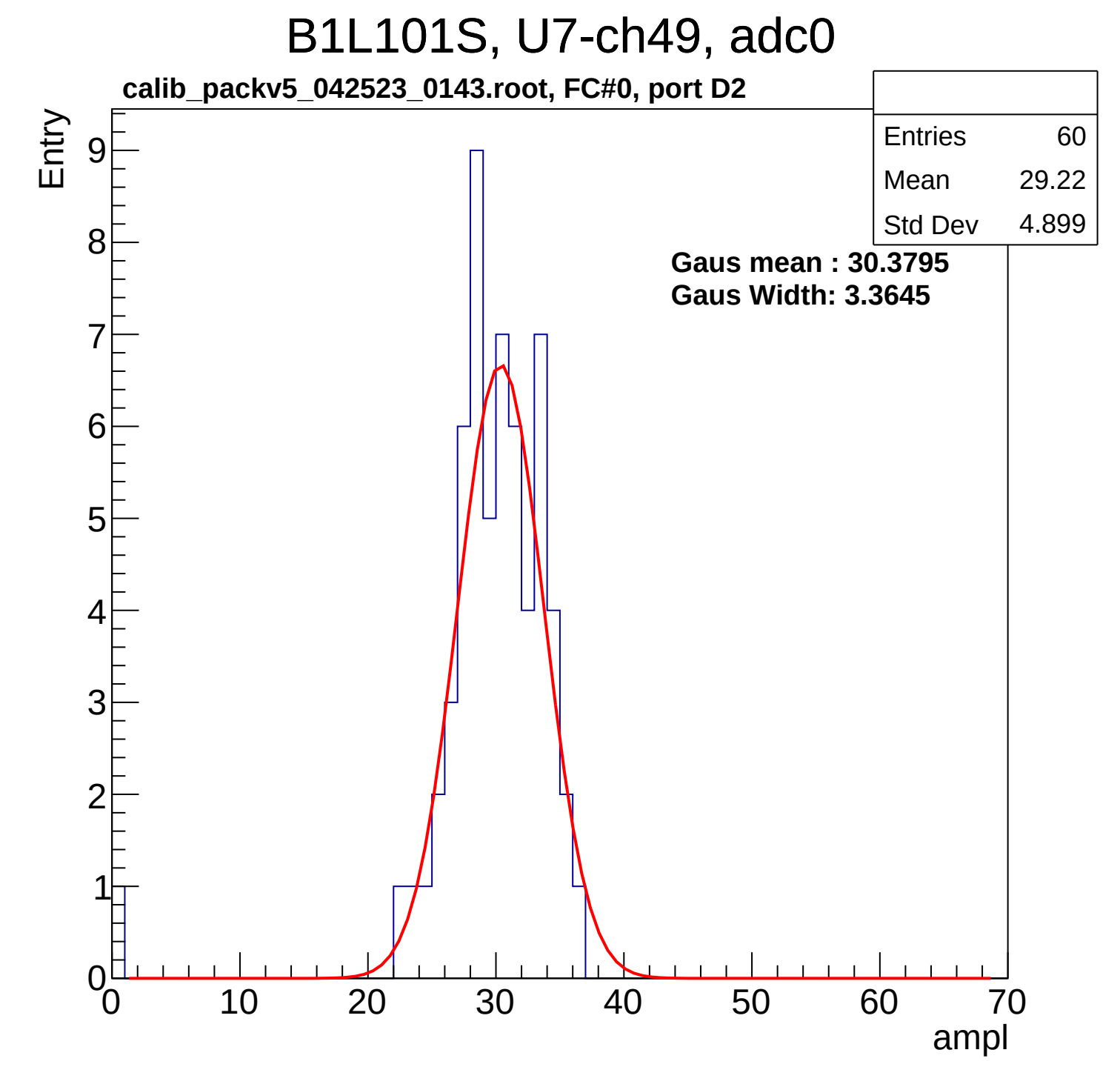
B1L101S, U7-ch49, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 29.22
Std Dev 4.899
Gaus mean : 30.3795
Gaus Width: 3.3645
Entry
ampl
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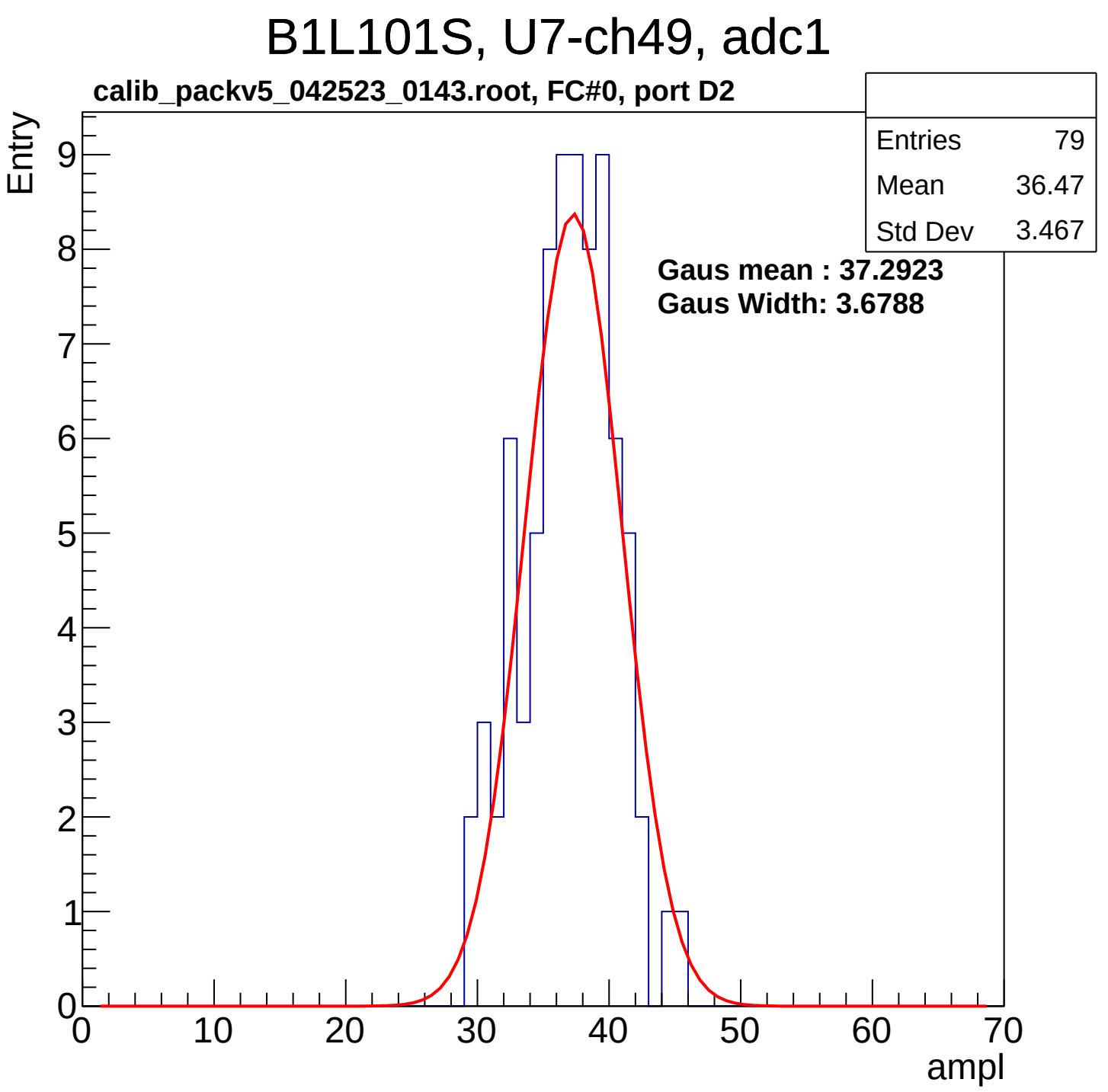
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch49, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 36.47
Std Dev 3.467
Gaus mean : 37.2923
Gaus Width: 3.6788
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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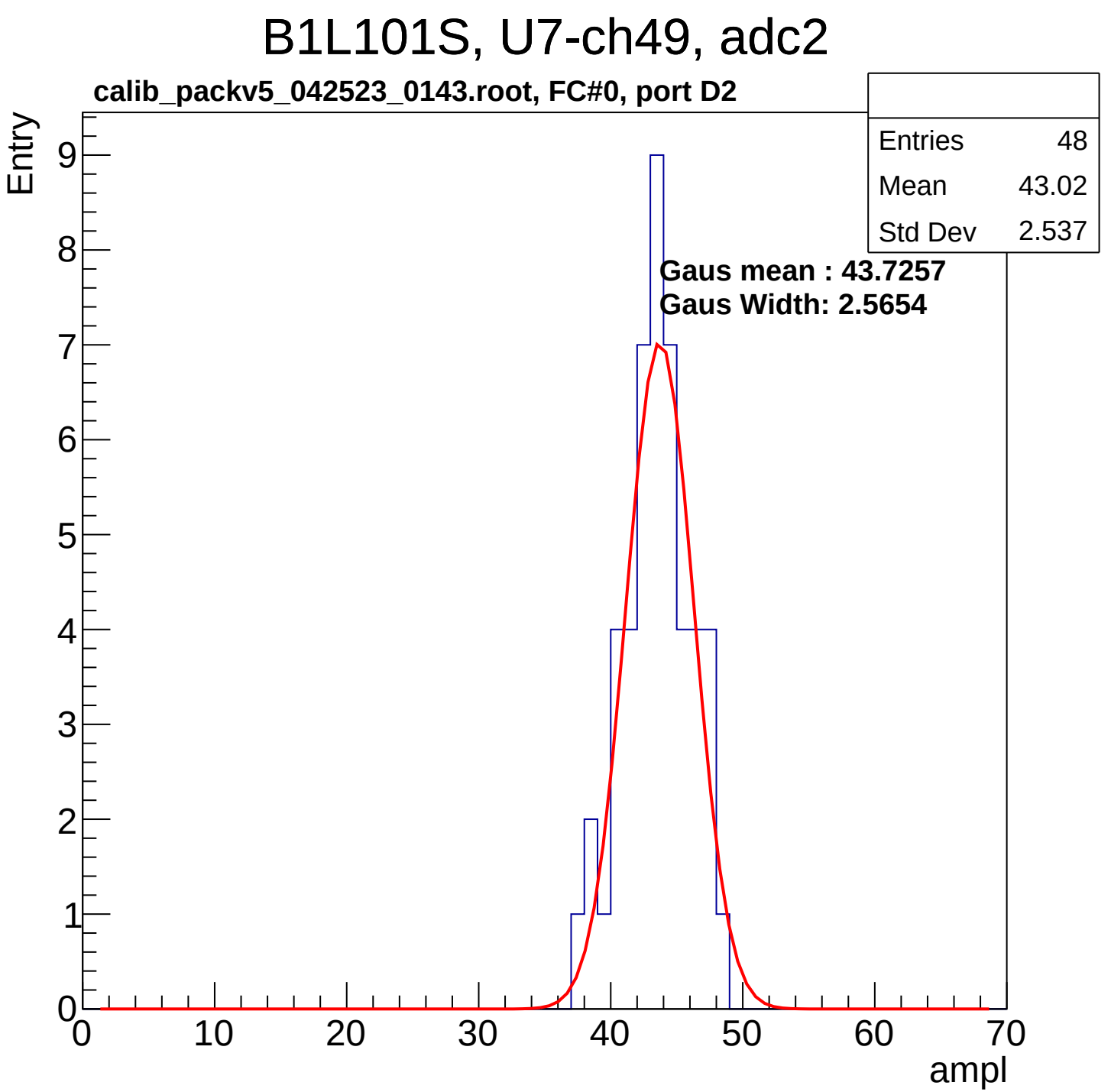
B1L101S, U7-ch49, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 43.02
Std Dev 2.537
Gaus mean : 43.7257
Gaus Width: 2.5654
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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60
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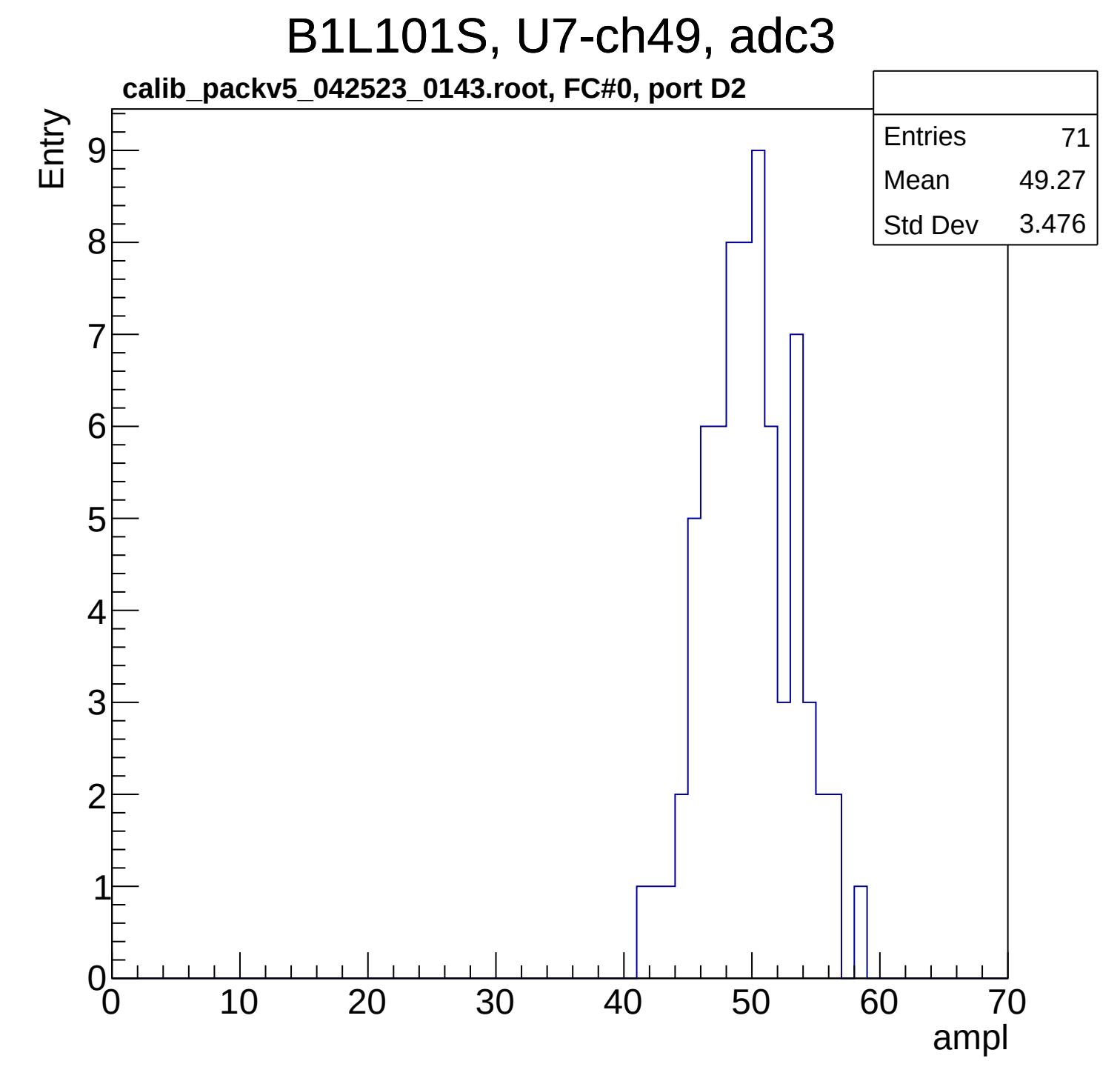
B1L101S, U7-ch49, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 49.27
Std Dev 3.476
Entry
ampl
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2
3
4
5
6
7
8
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0
10
20
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40
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60
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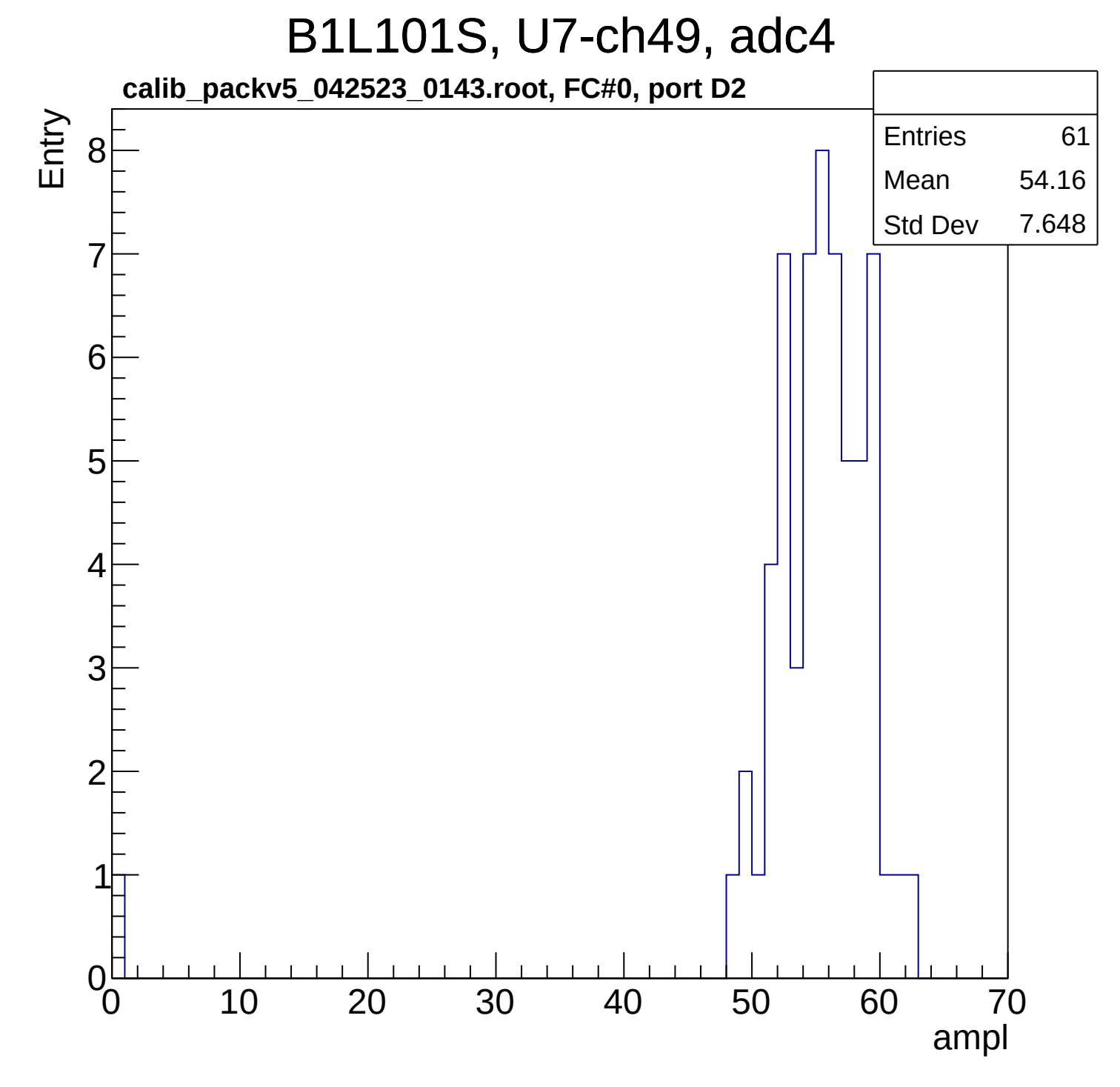
B1L101S, U7-ch49, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 54.16
Std Dev 7.648
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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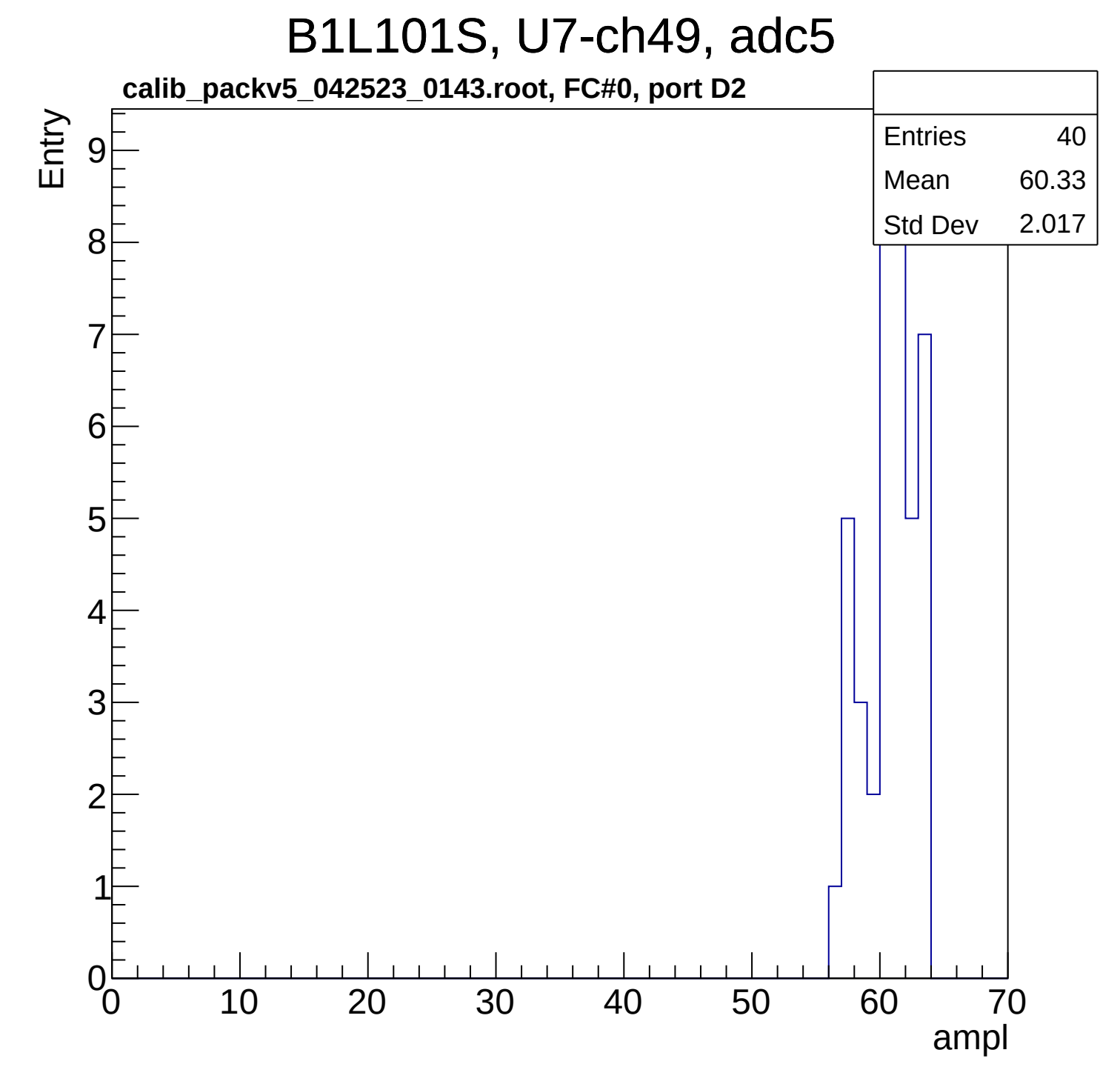
B1L101S, U7-ch49, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 40
Mean 60.33
Std Dev 2.017
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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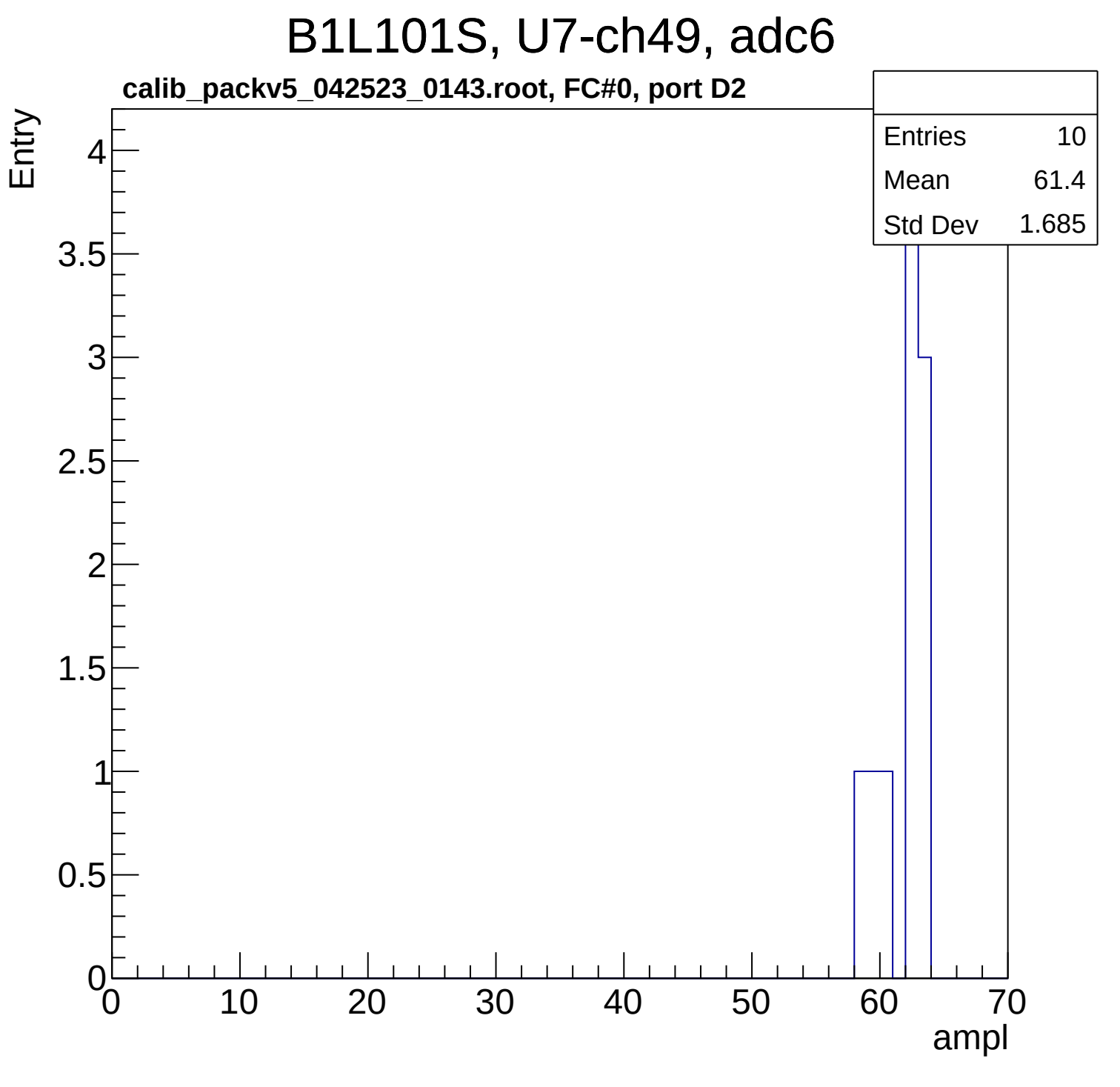
B1L101S, U7-ch49, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 61.4
Std Dev 1.685
Entry
ampl
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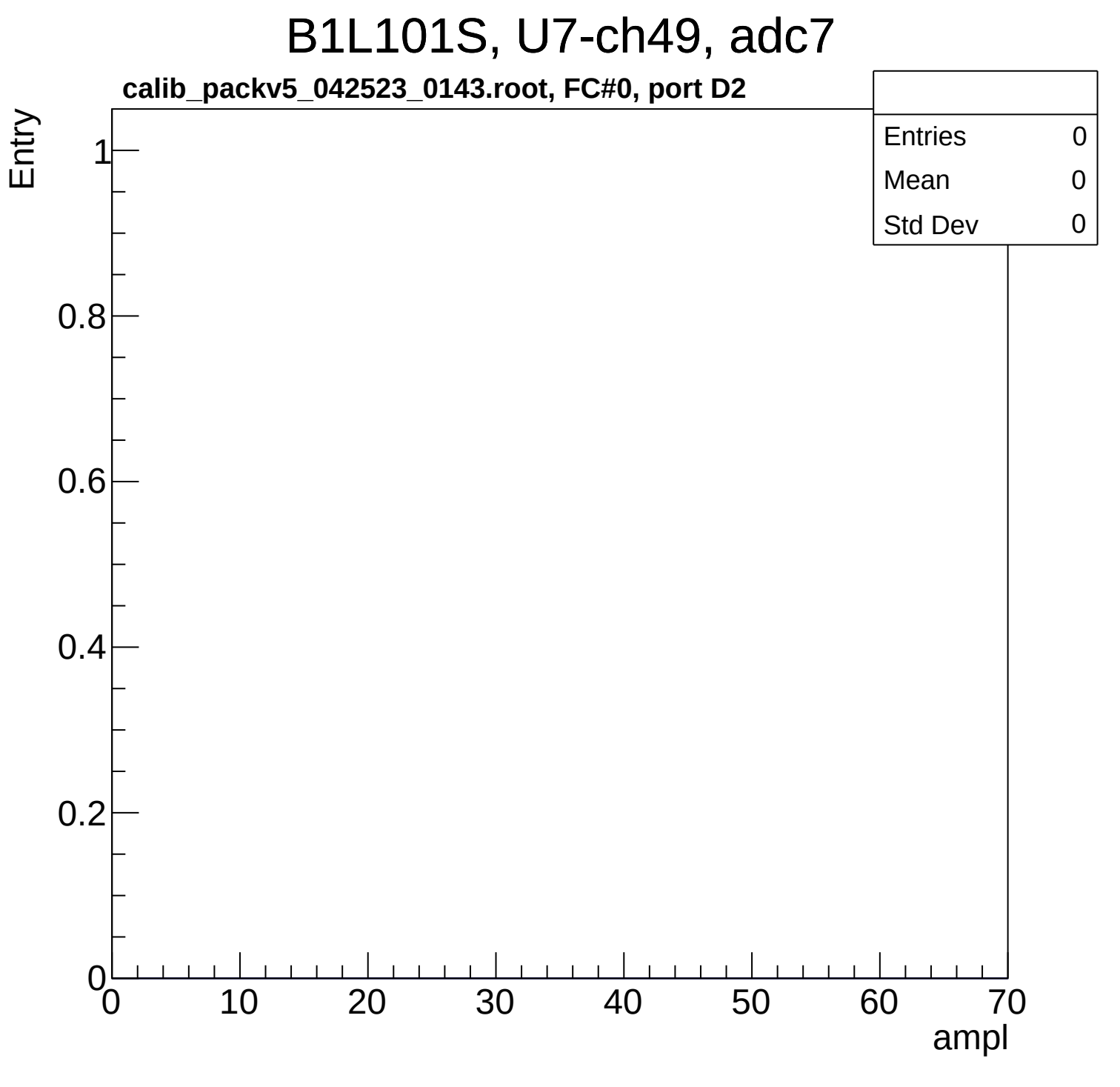
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L101S, U7-ch49, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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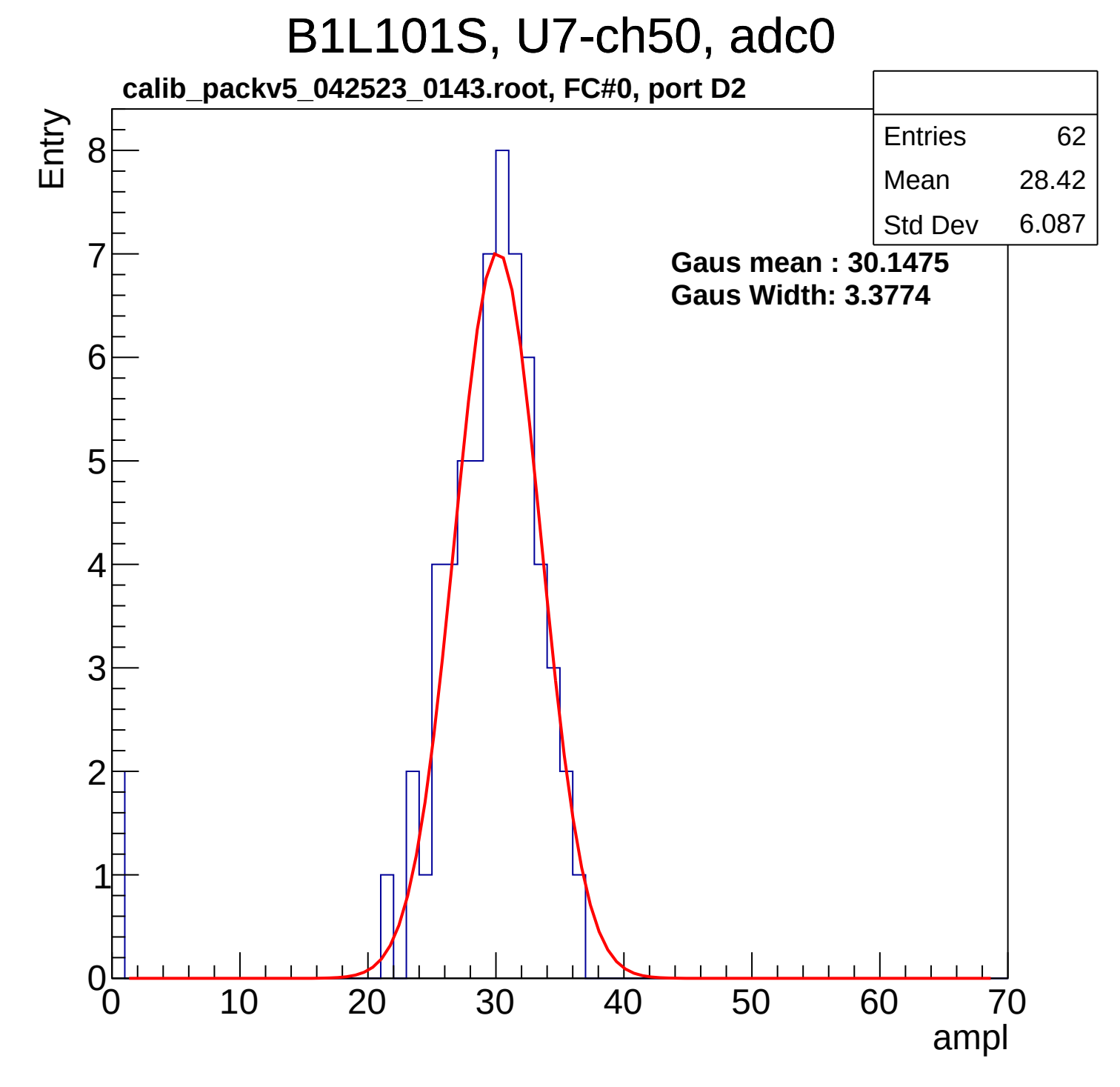
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch50, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 28.42
Std Dev 6.087
Gaus mean : 30.1475
Gaus Width: 3.3774
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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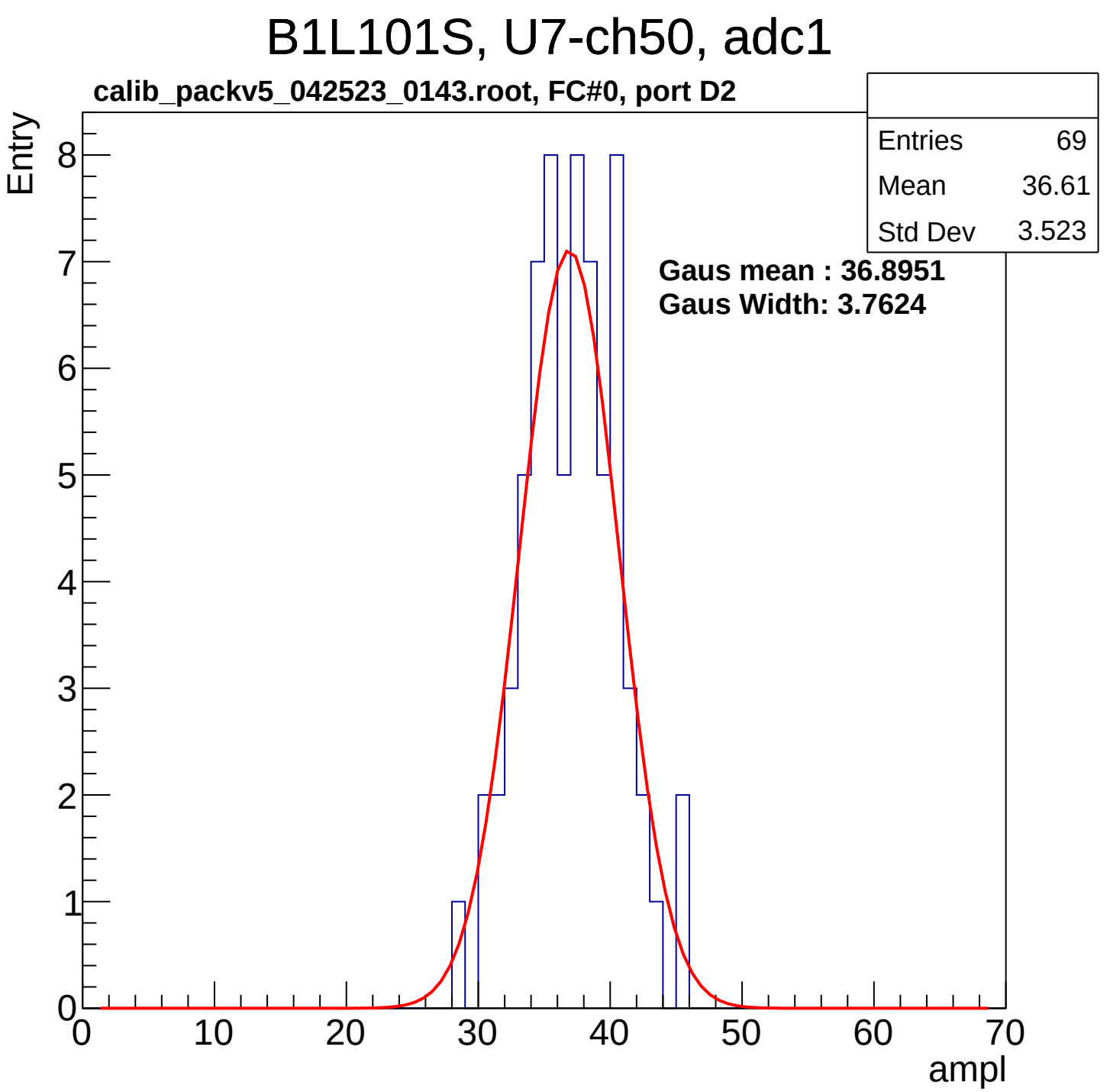
B1L101S, U7-ch50, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 36.61
Std Dev 3.523
Gaus mean : 36.8951
Gaus Width: 3.7624
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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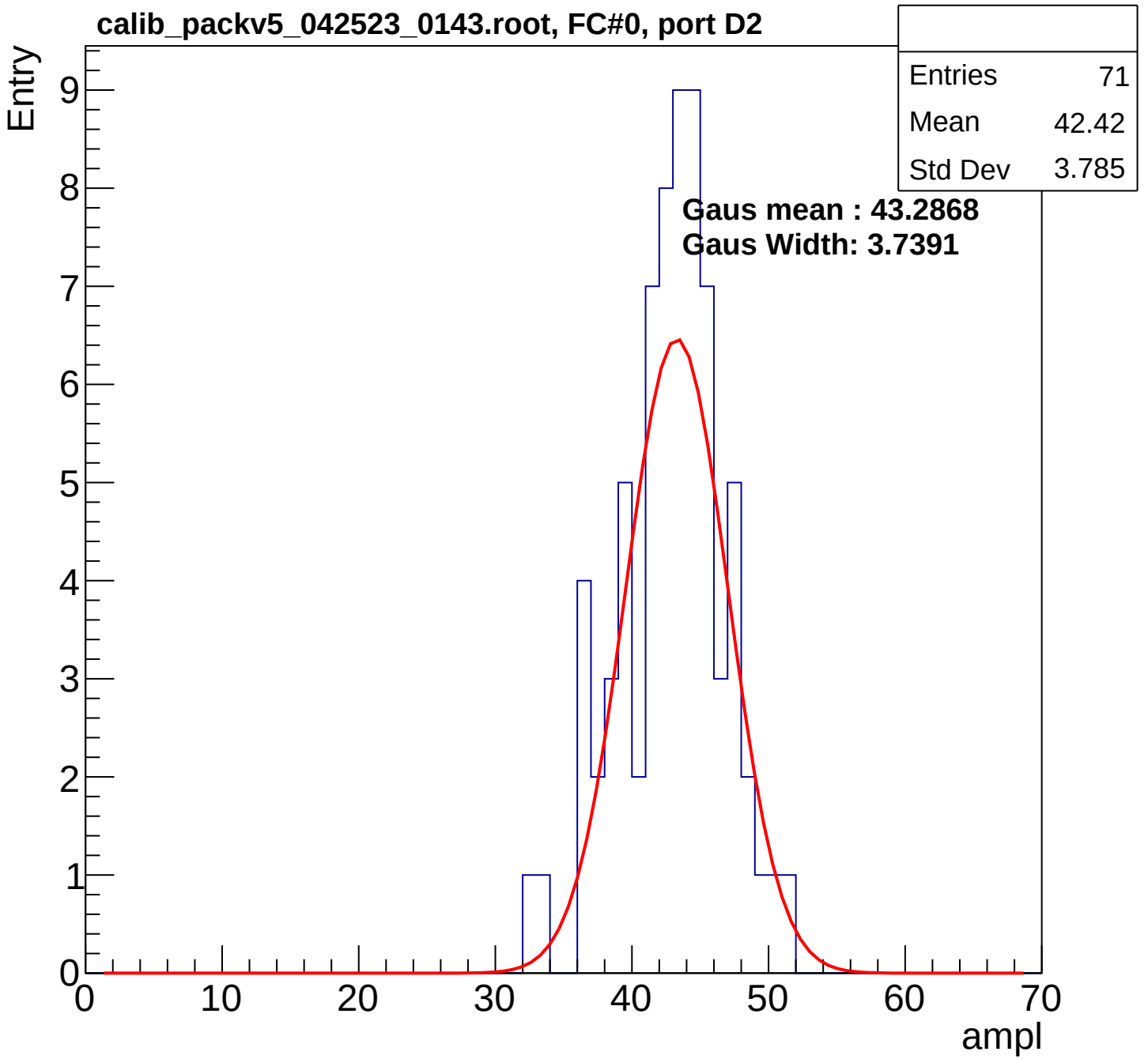
B1L101S, U7-ch50, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 42.42
Std Dev 3.785
Gaus mean : 43.2868
Gaus Width: 3.7391
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
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40
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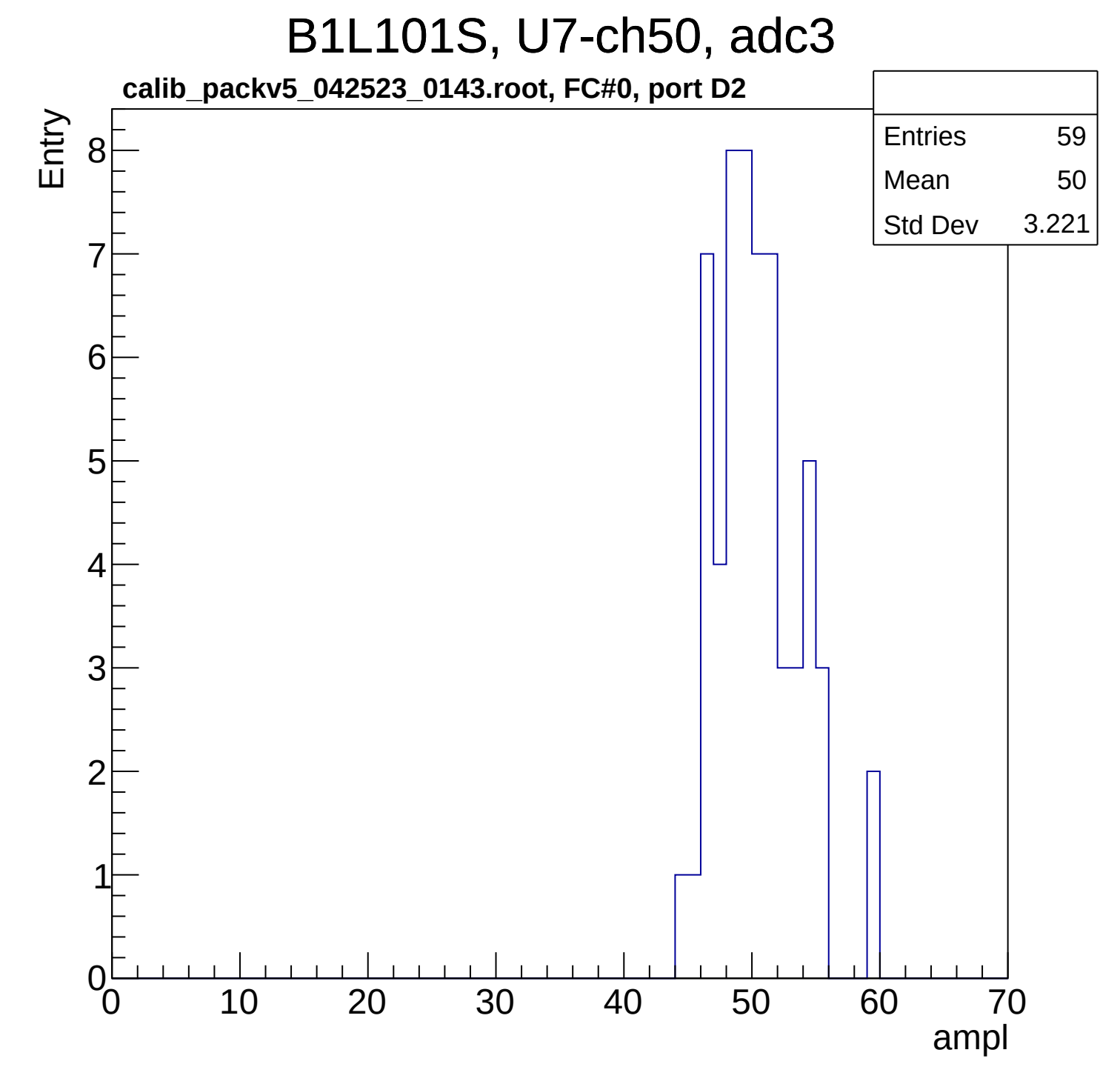
B1L101S, U7-ch50, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 50
Std Dev 3.221
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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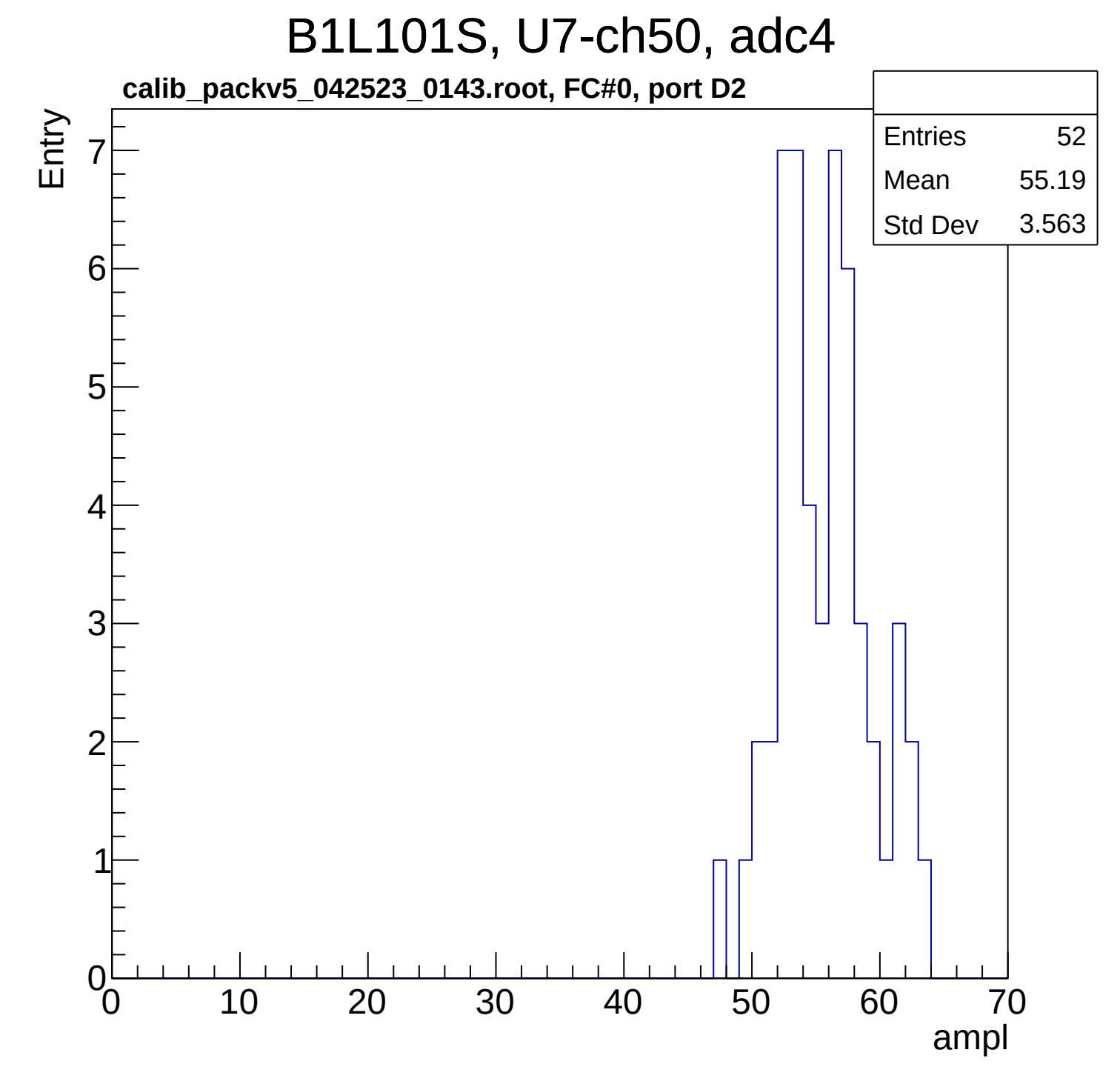
B1L101S, U7-ch50, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 55.19
Std Dev 3.563
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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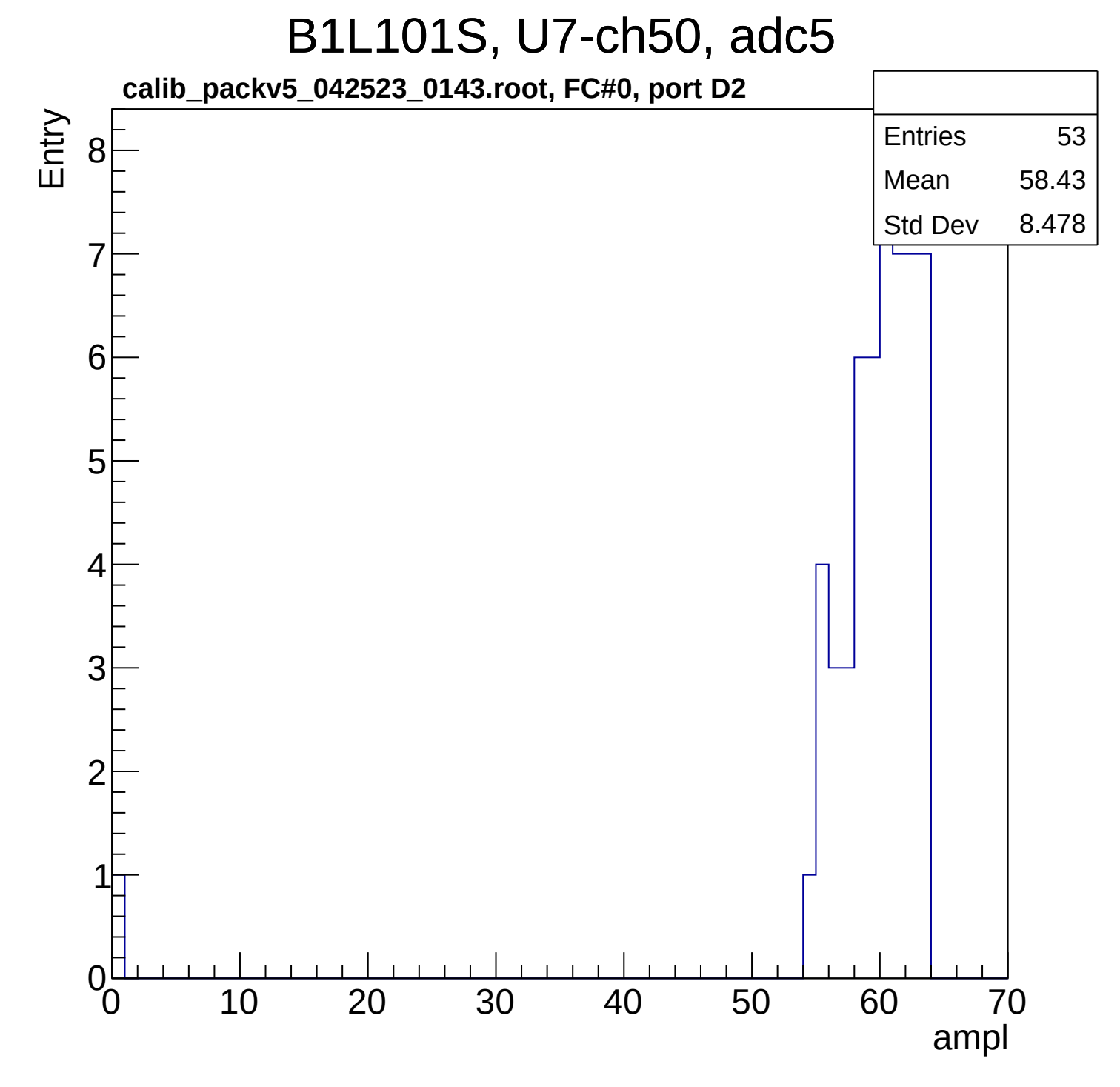
B1L101S, U7-ch50, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 58.43
Std Dev 8.478
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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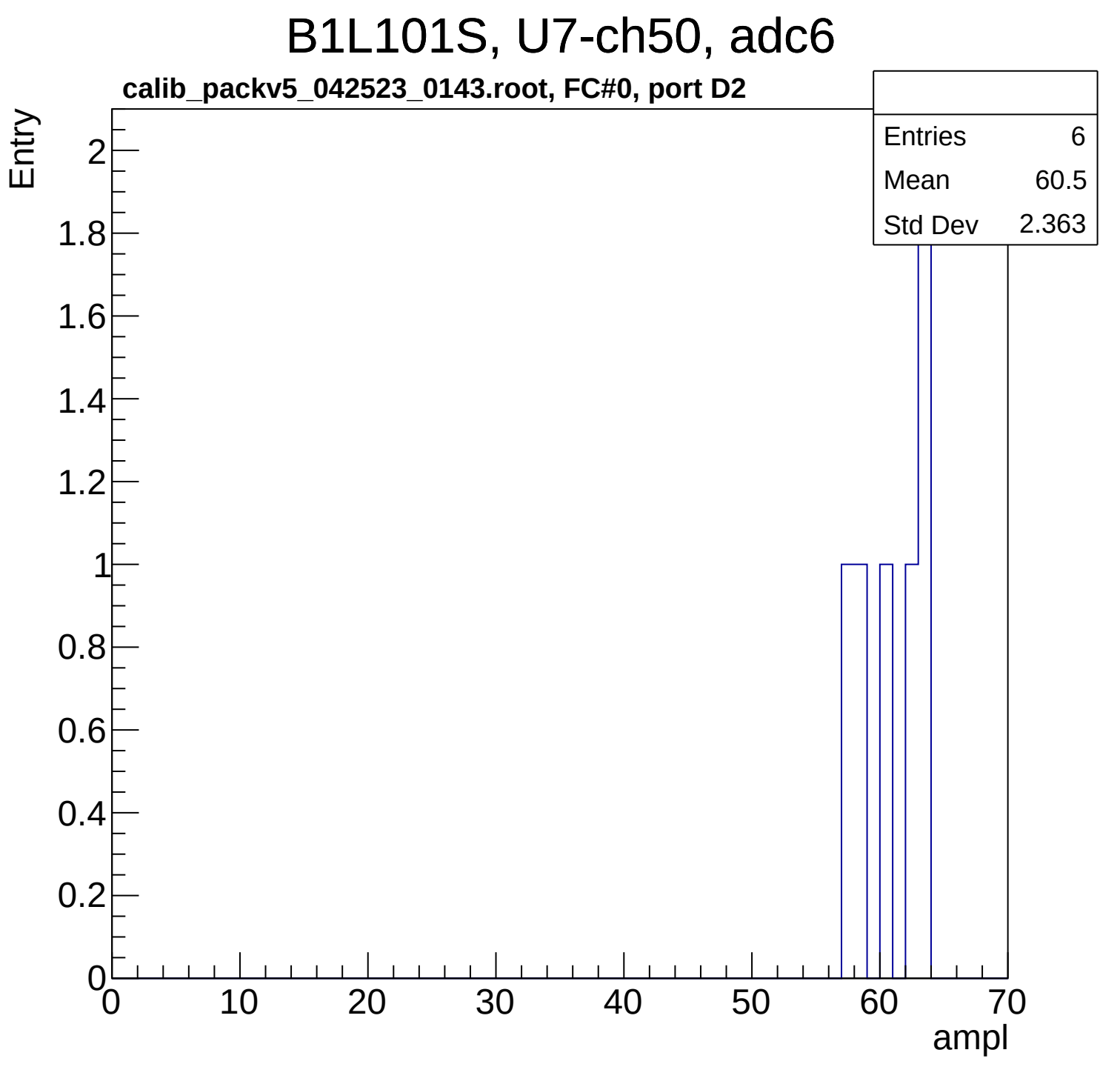
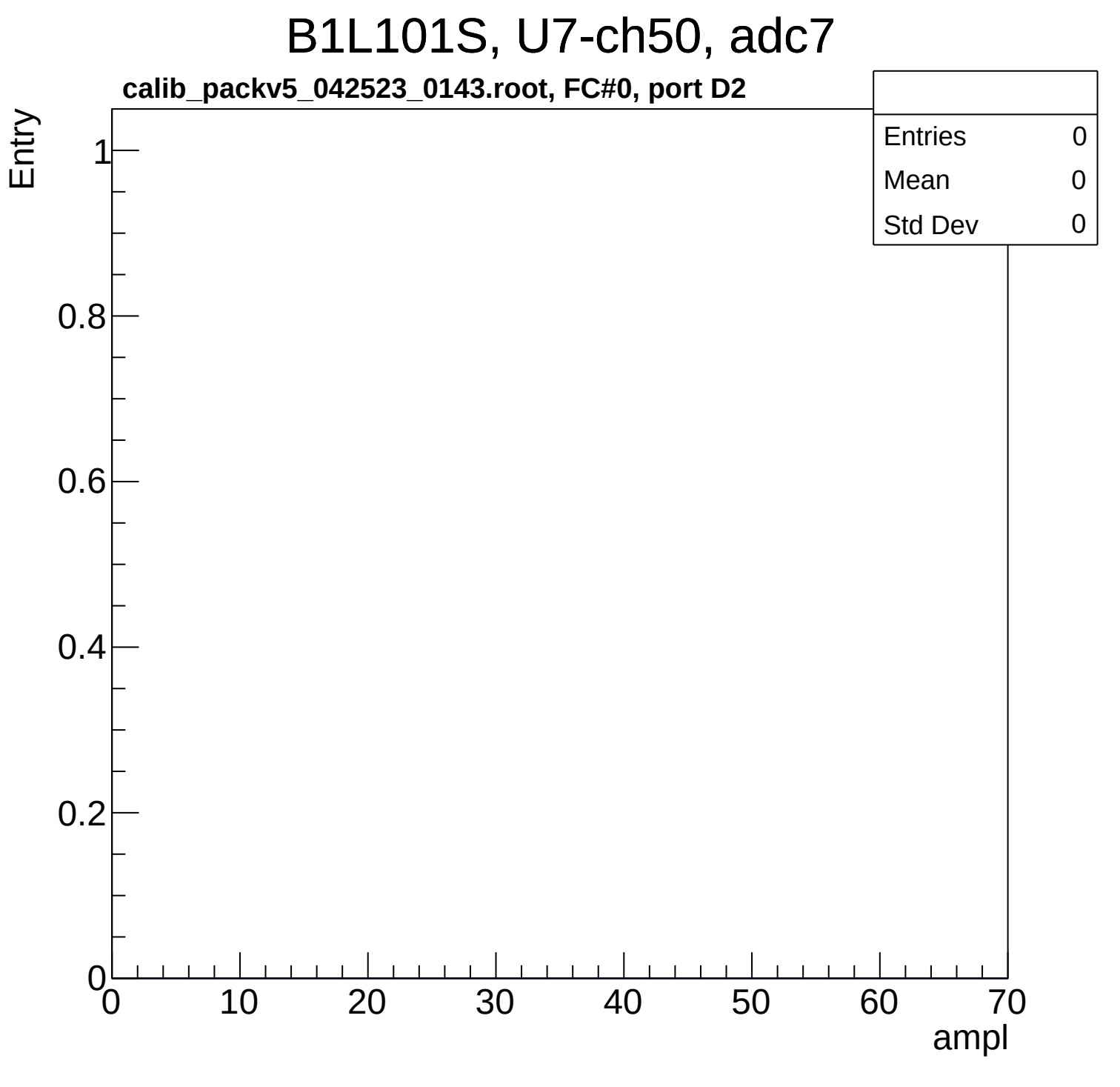
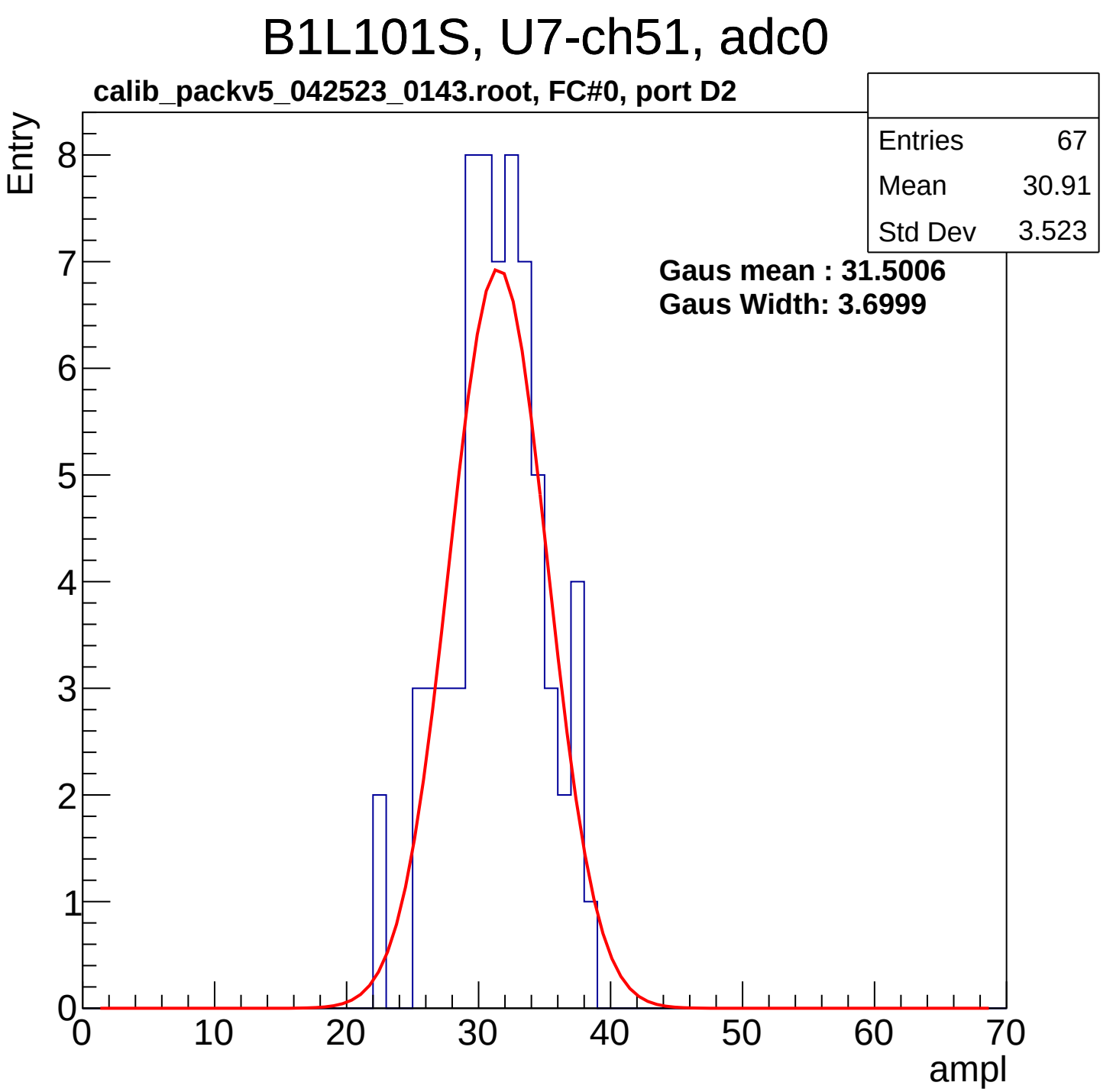

B1L101S, U7-ch50, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 60.5
Std Dev 2.363
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U7-ch50, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch51, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 30.91
Std Dev 3.523
Gaus mean : 31.5006
Gaus Width: 3.6999
Entry
ampl
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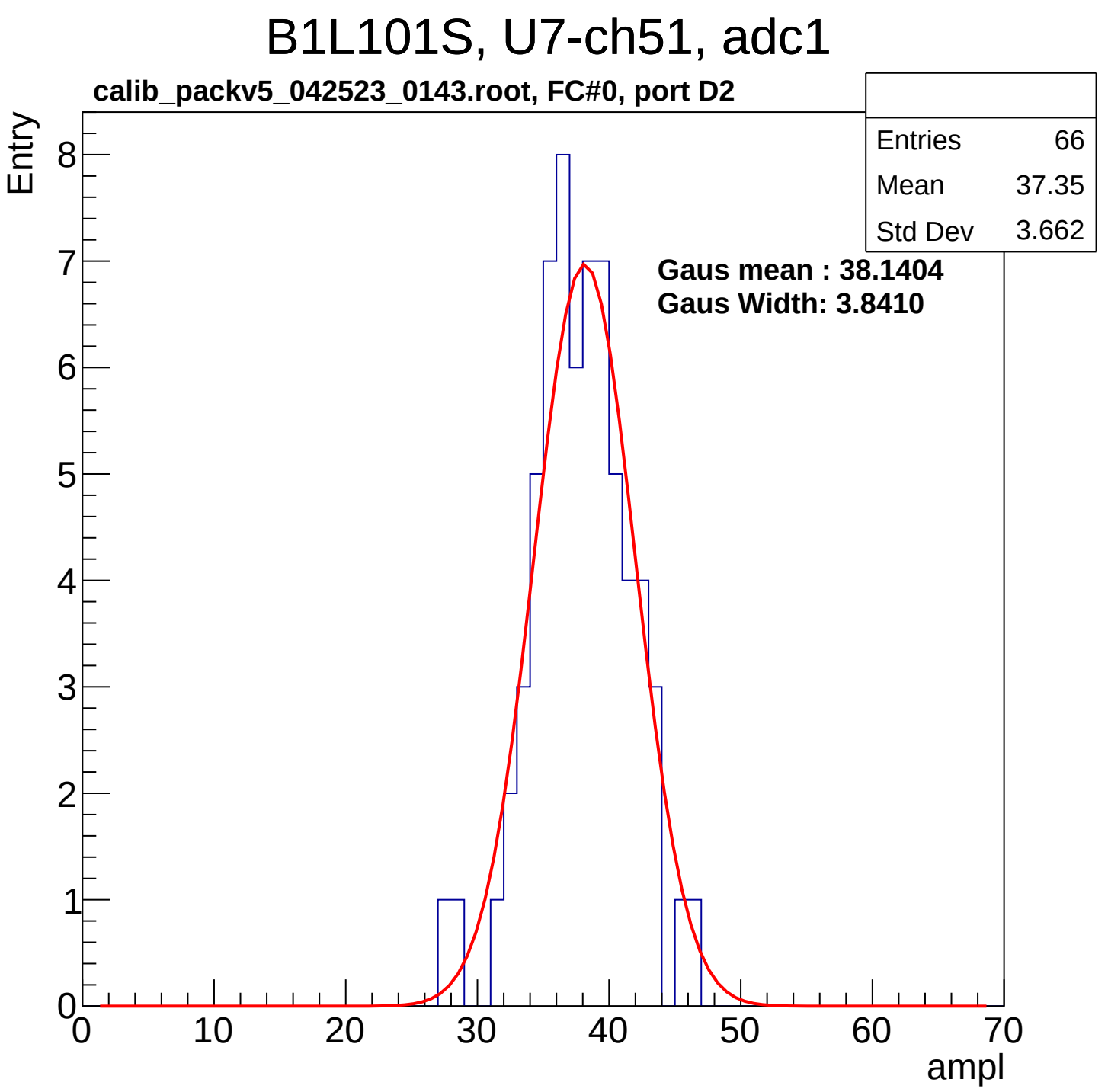
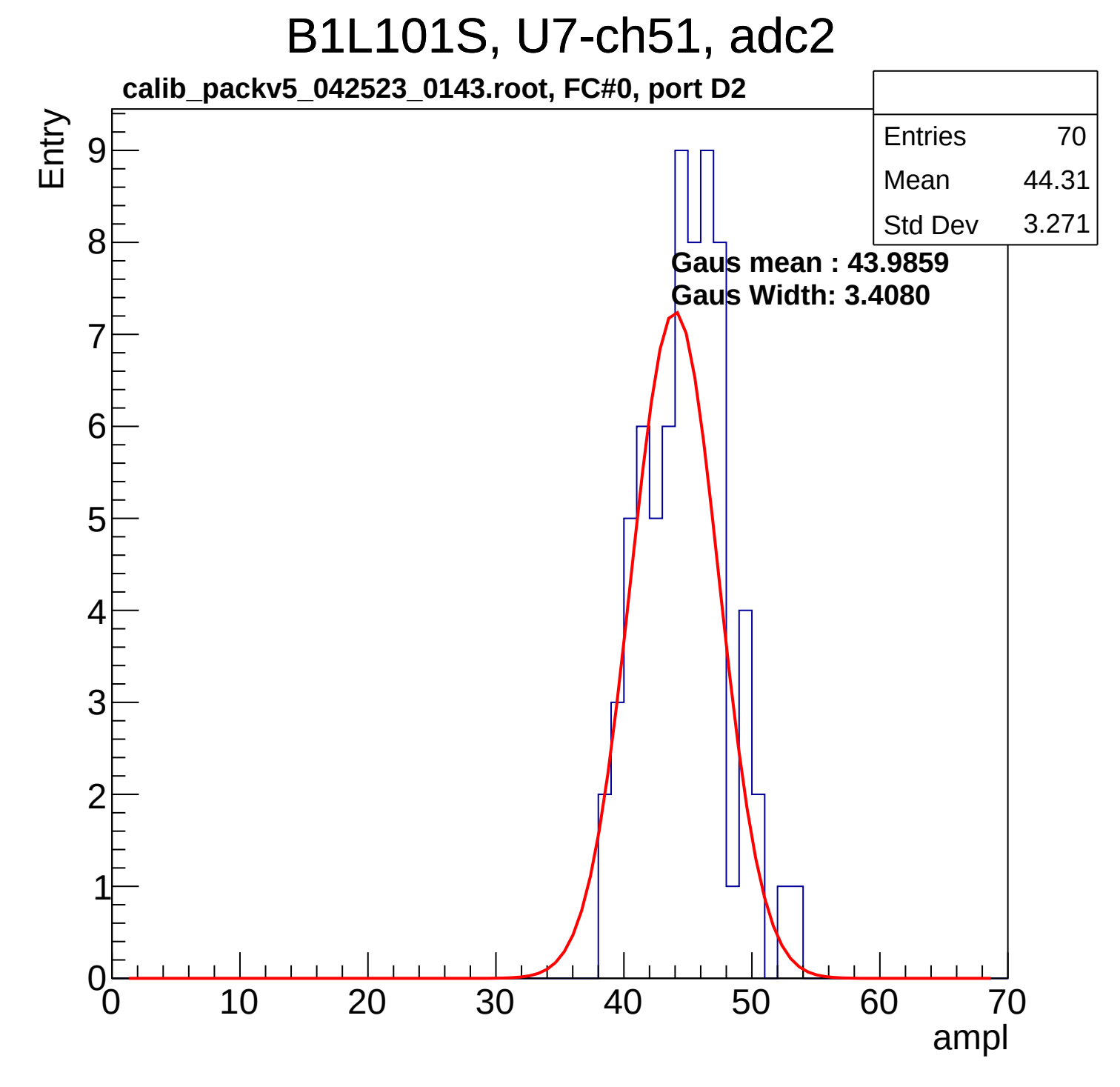
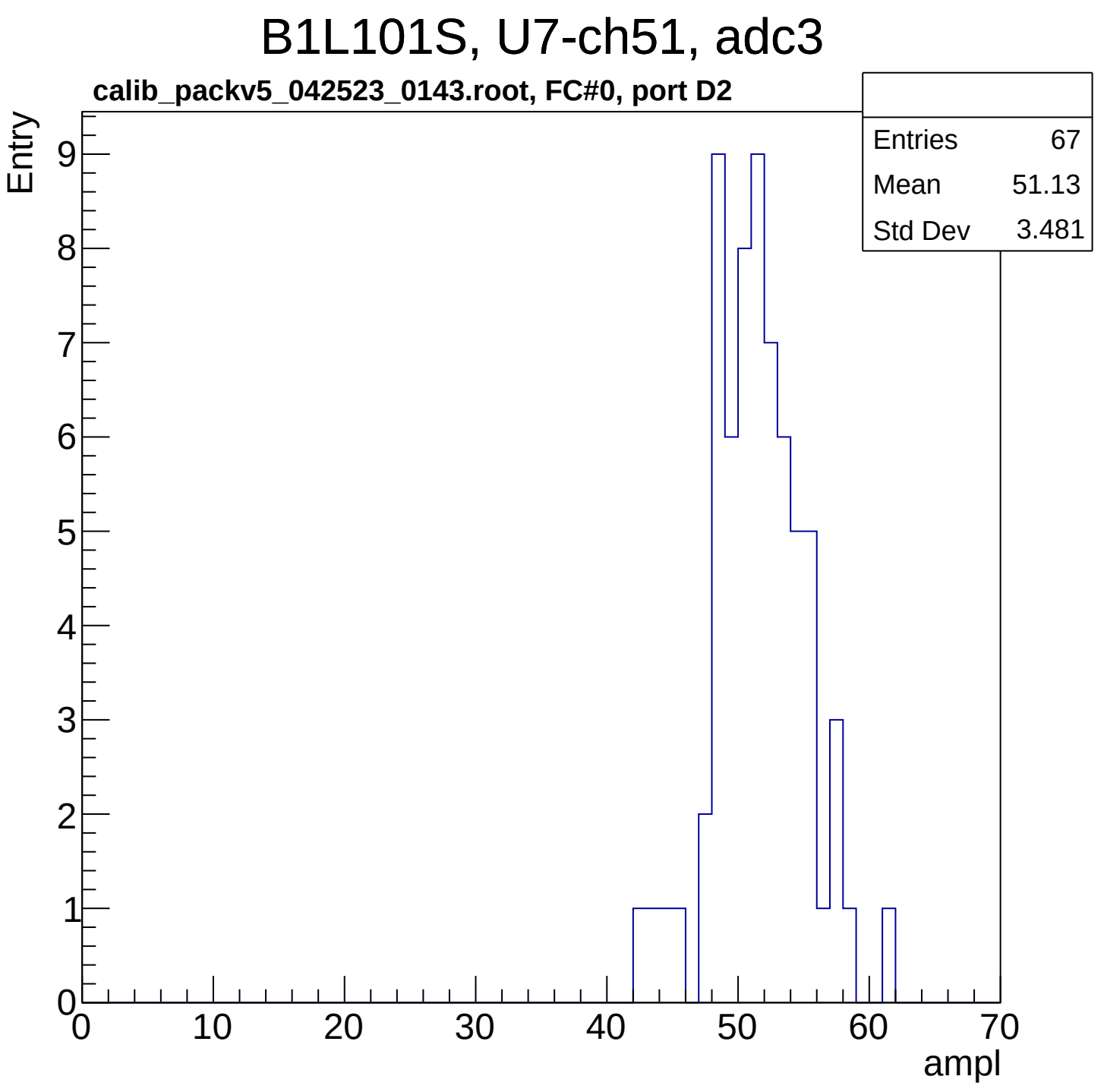
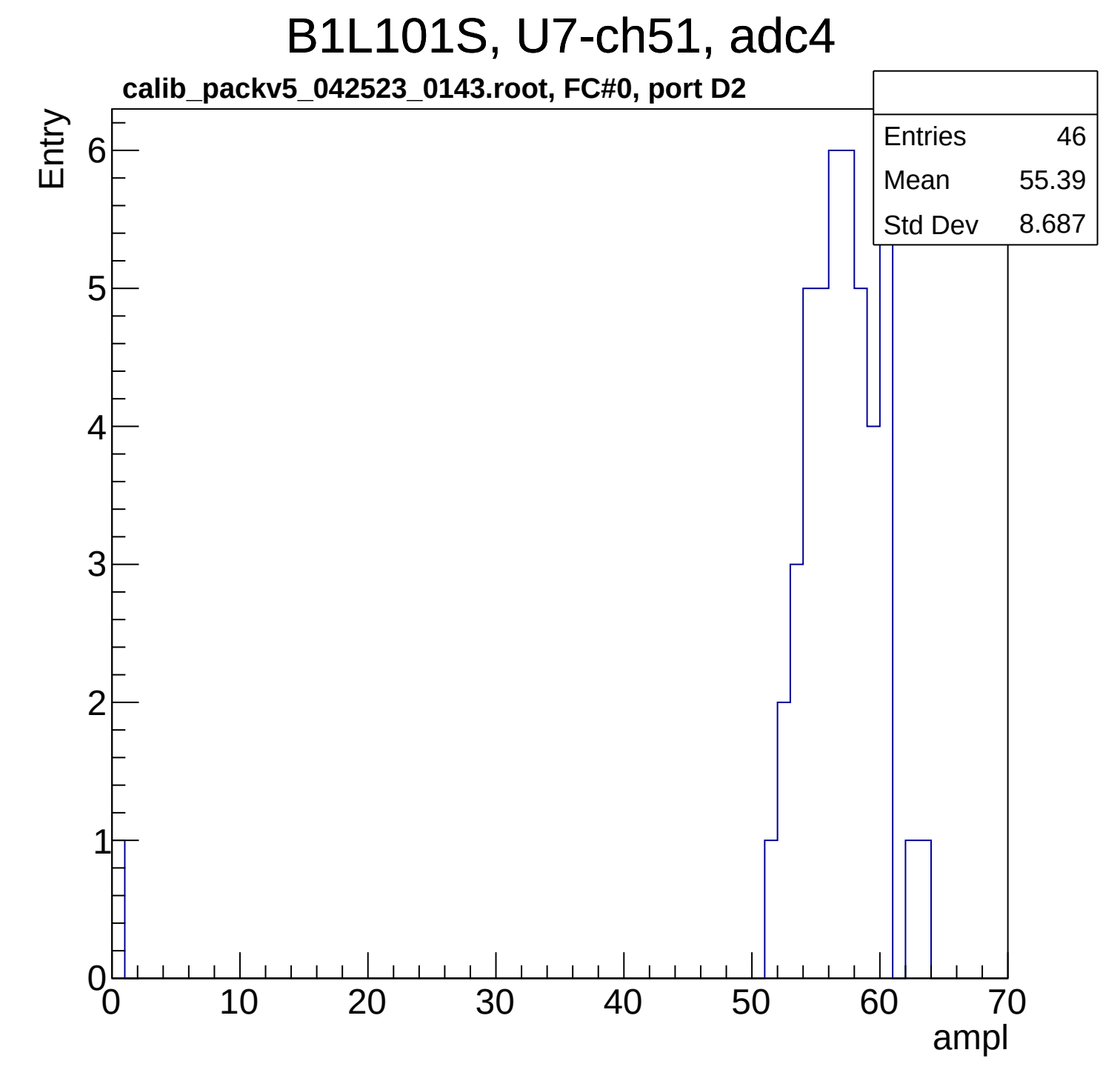
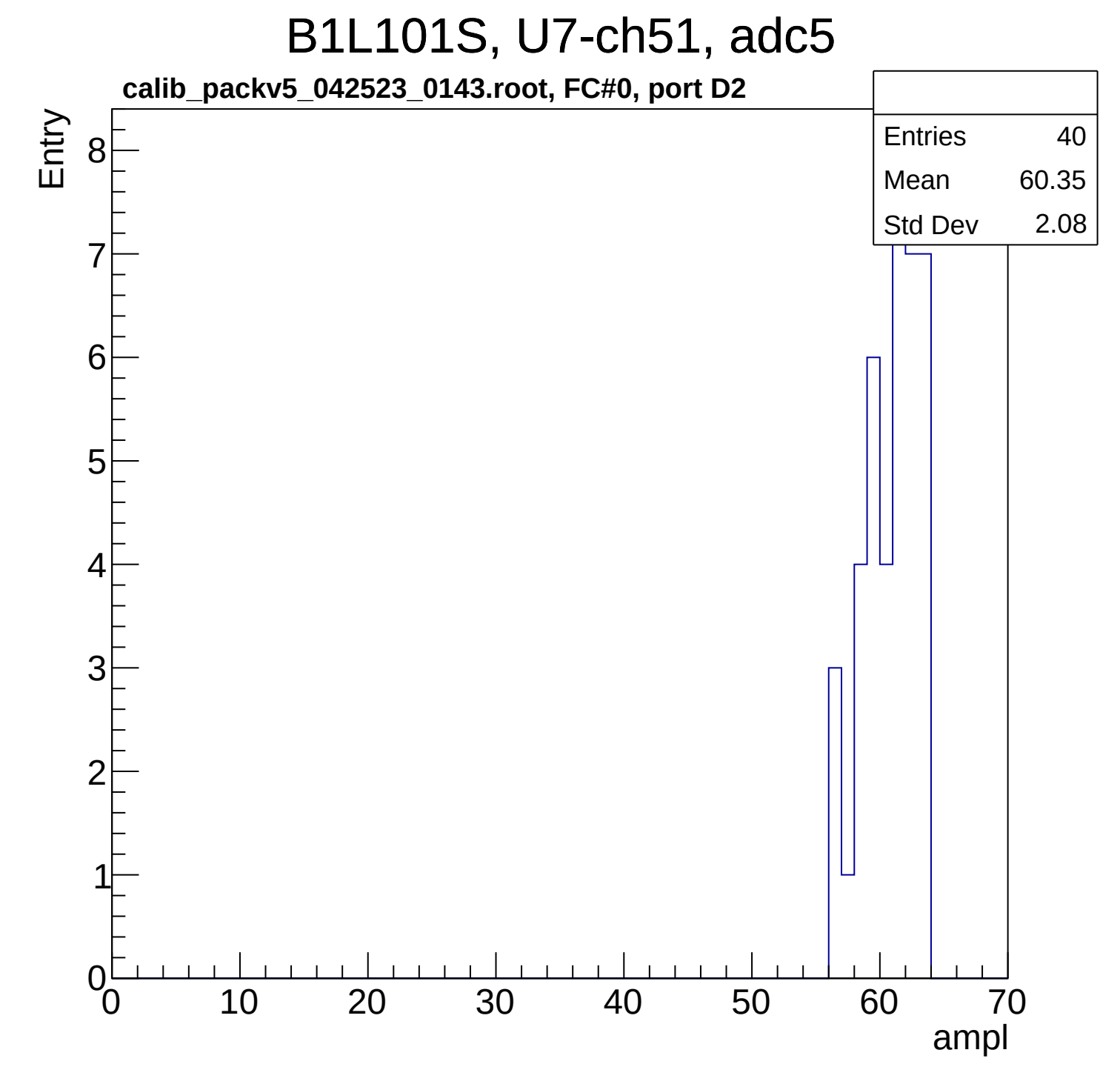
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch51, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 37.35
Std Dev 3.662
Gaus mean : 38.1404
Gaus Width: 3.8410
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch51, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 44.31
Std Dev 3.271
Gaus mean : 43.9859
Gaus Width: 3.4080
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch51, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 51.13
Std Dev 3.481
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch51, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 55.39
Std Dev 8.687
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L101S, U7-ch51, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 40
Mean 60.35
Std Dev 2.08
Entry
ampl
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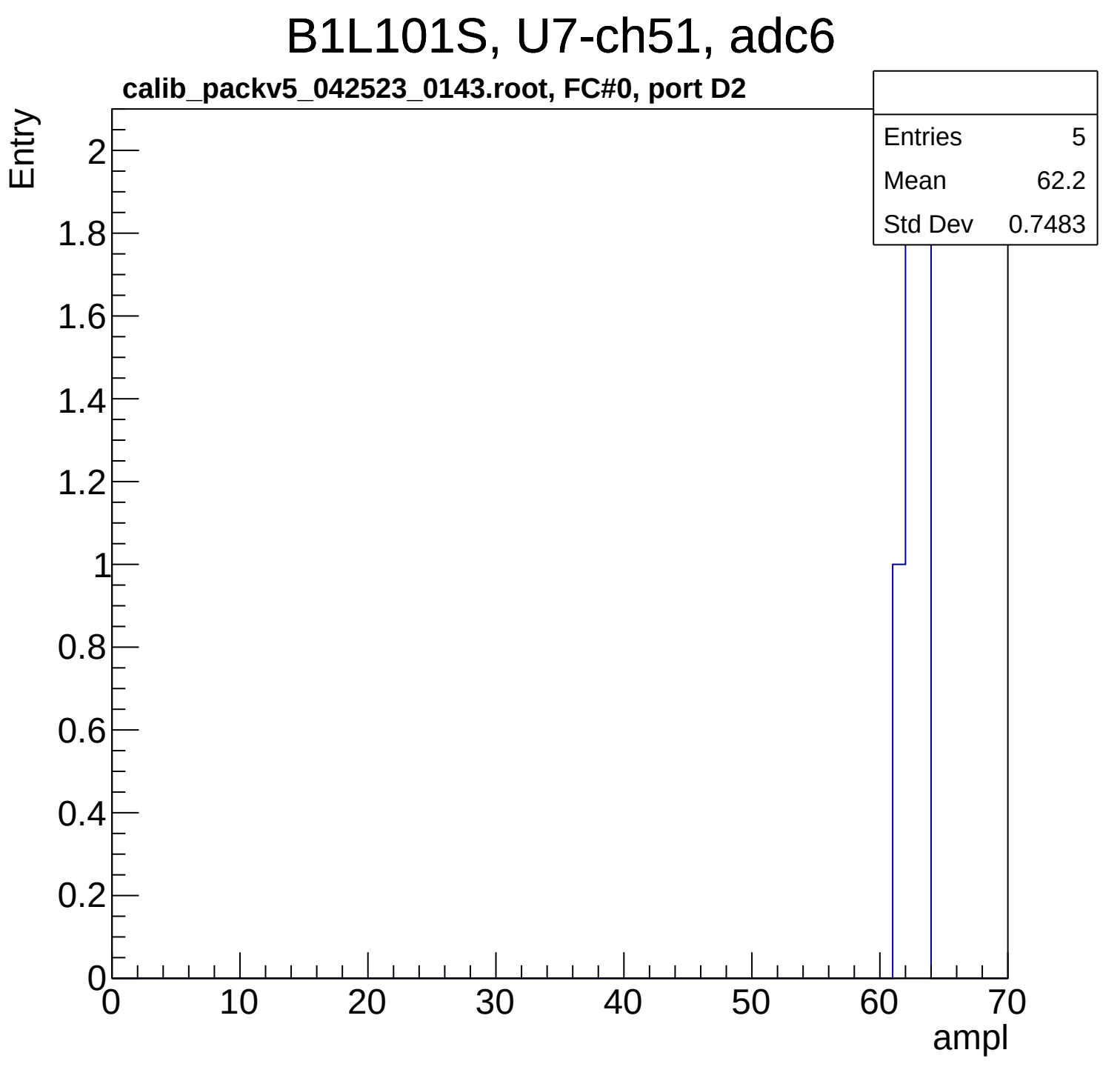
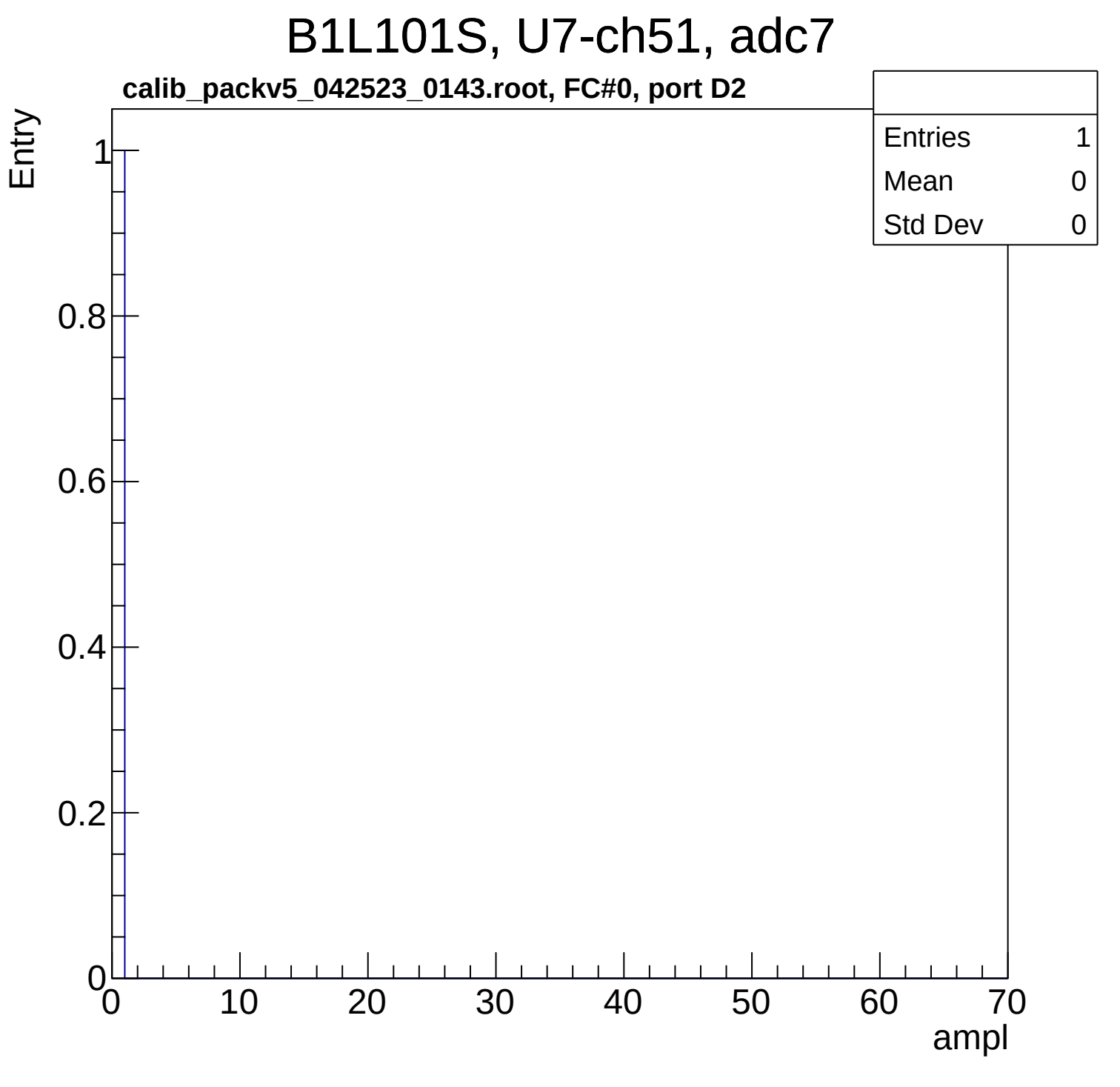
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch51, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 62.2
Std Dev 0.7483
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U7-ch51, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
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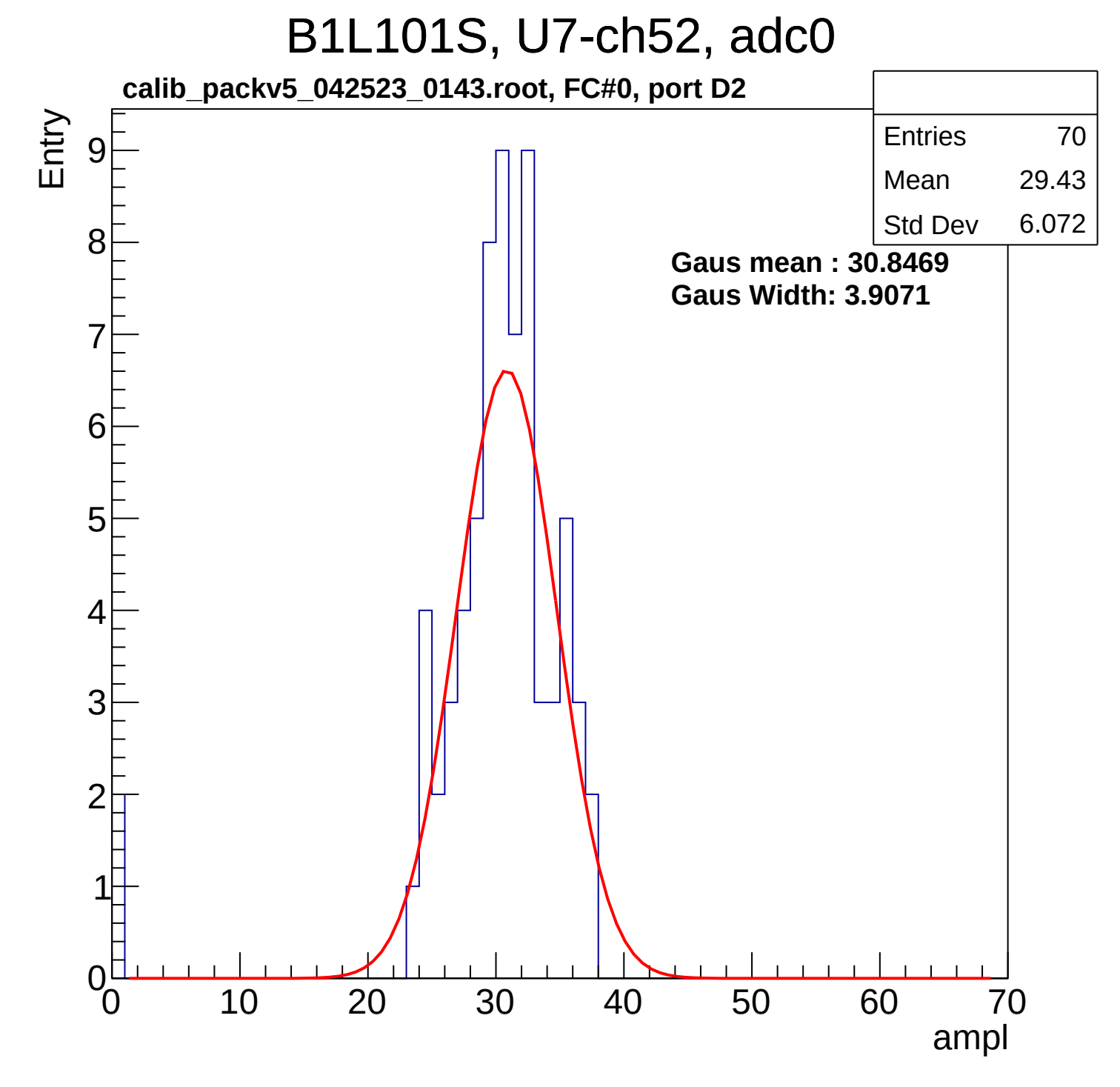
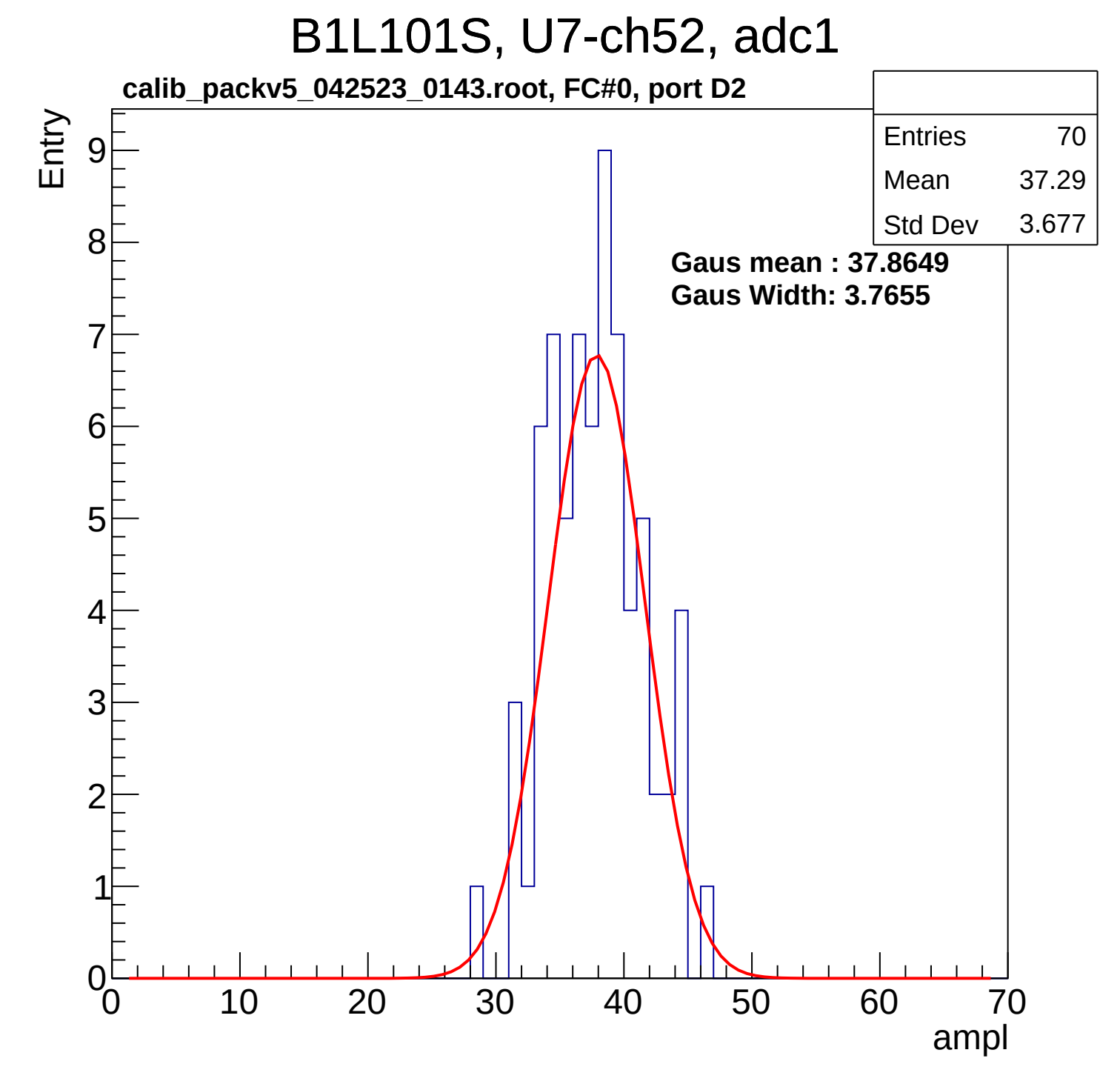
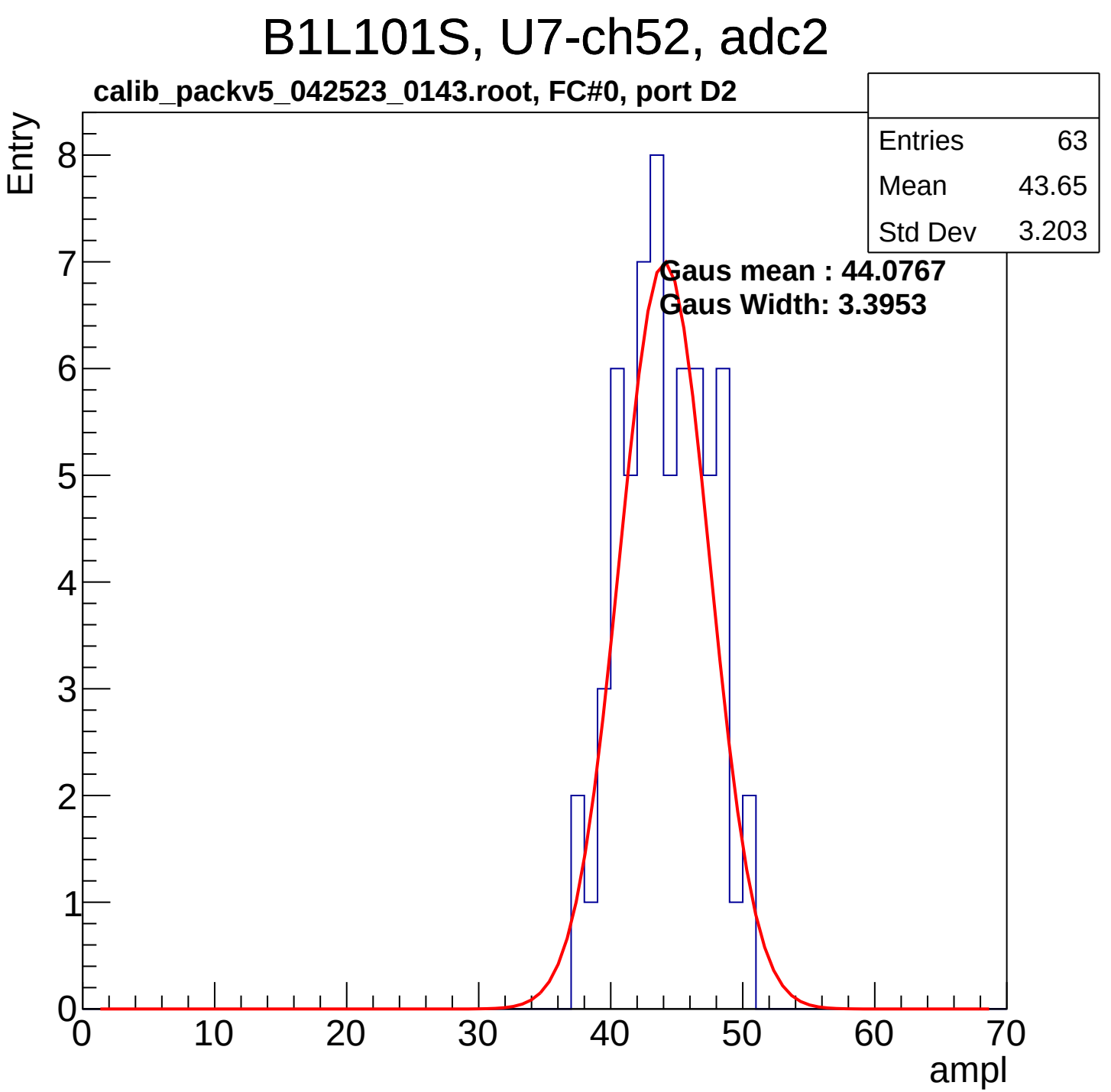
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch52, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 29.43
Std Dev 6.072
Gaus mean : 30.8469
Gaus Width: 3.9071
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch52, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 37.29
Std Dev 3.677
Gaus mean : 37.8649
Gaus Width: 3.7655
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L101S, U7-ch52, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 43.65
Std Dev 3.203
Gaus mean : 44.0767
Gaus Width: 3.3953
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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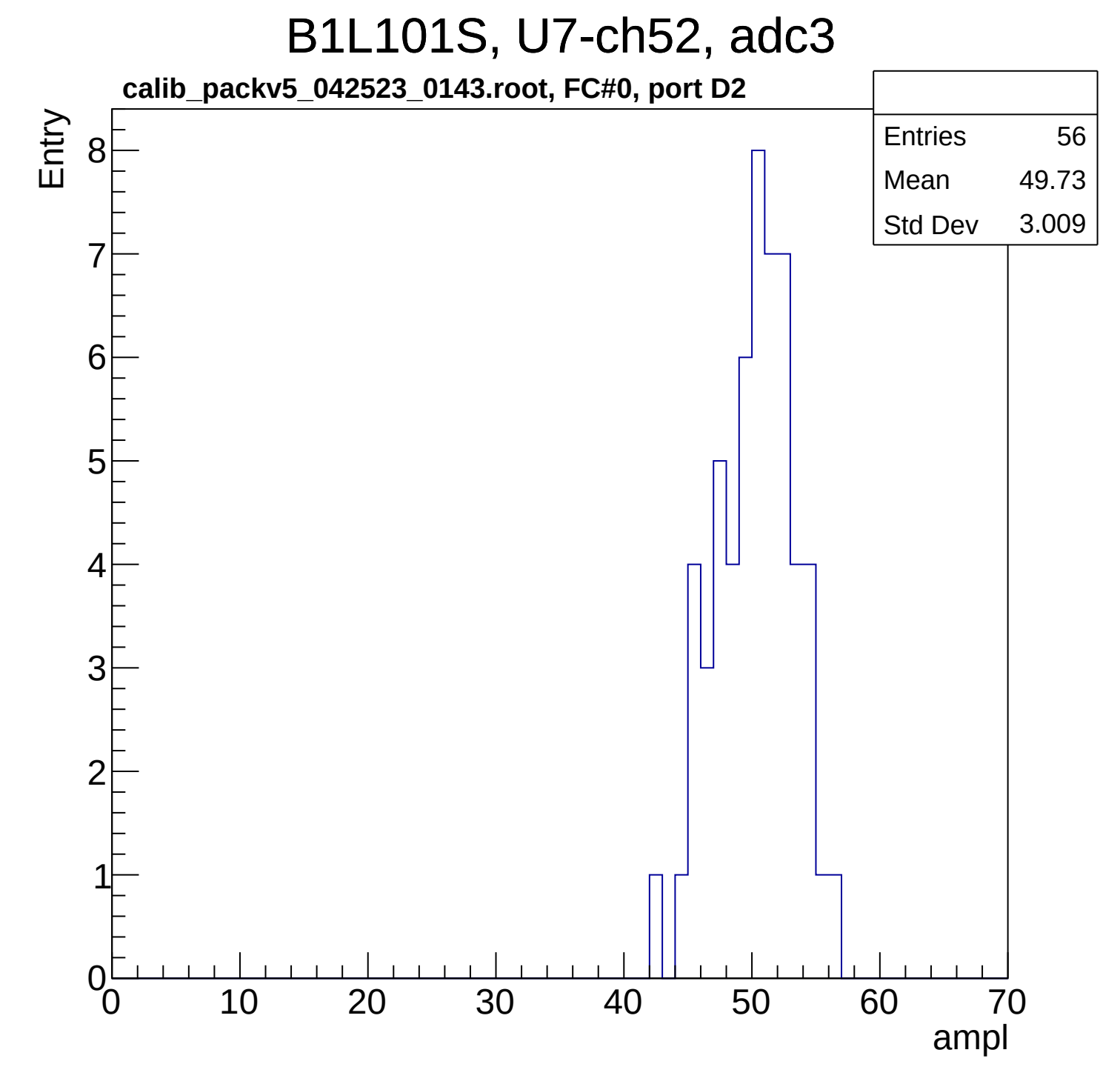
40
50
60
70


B1L101S, U7-ch52, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 49.73
Std Dev 3.009
Entry
ampl
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1
2
3
4
5
6
7
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0
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40
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60
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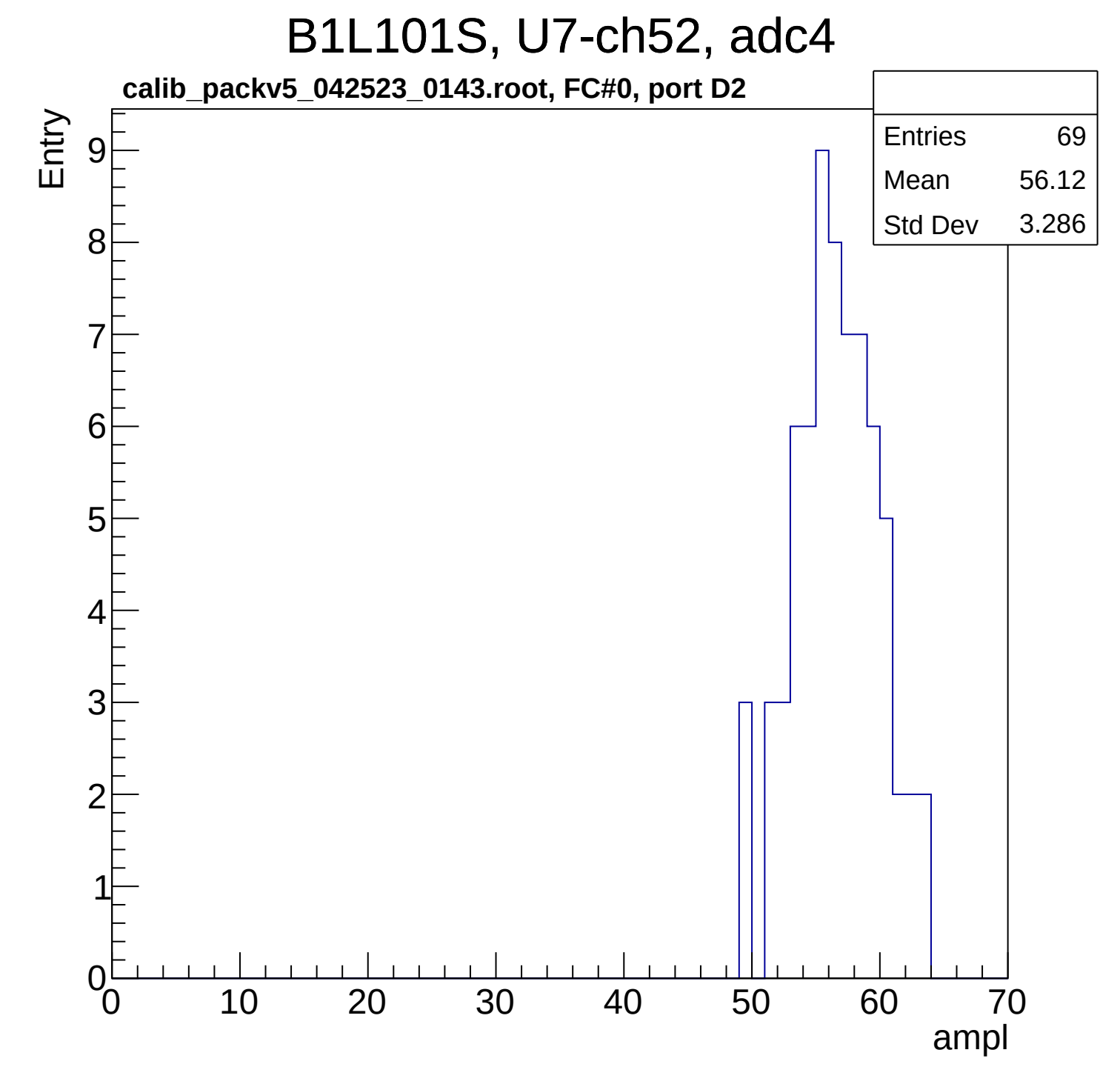
B1L101S, U7-ch52, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 56.12
Std Dev 3.286
Entry
ampl
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6
7
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0
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40
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60
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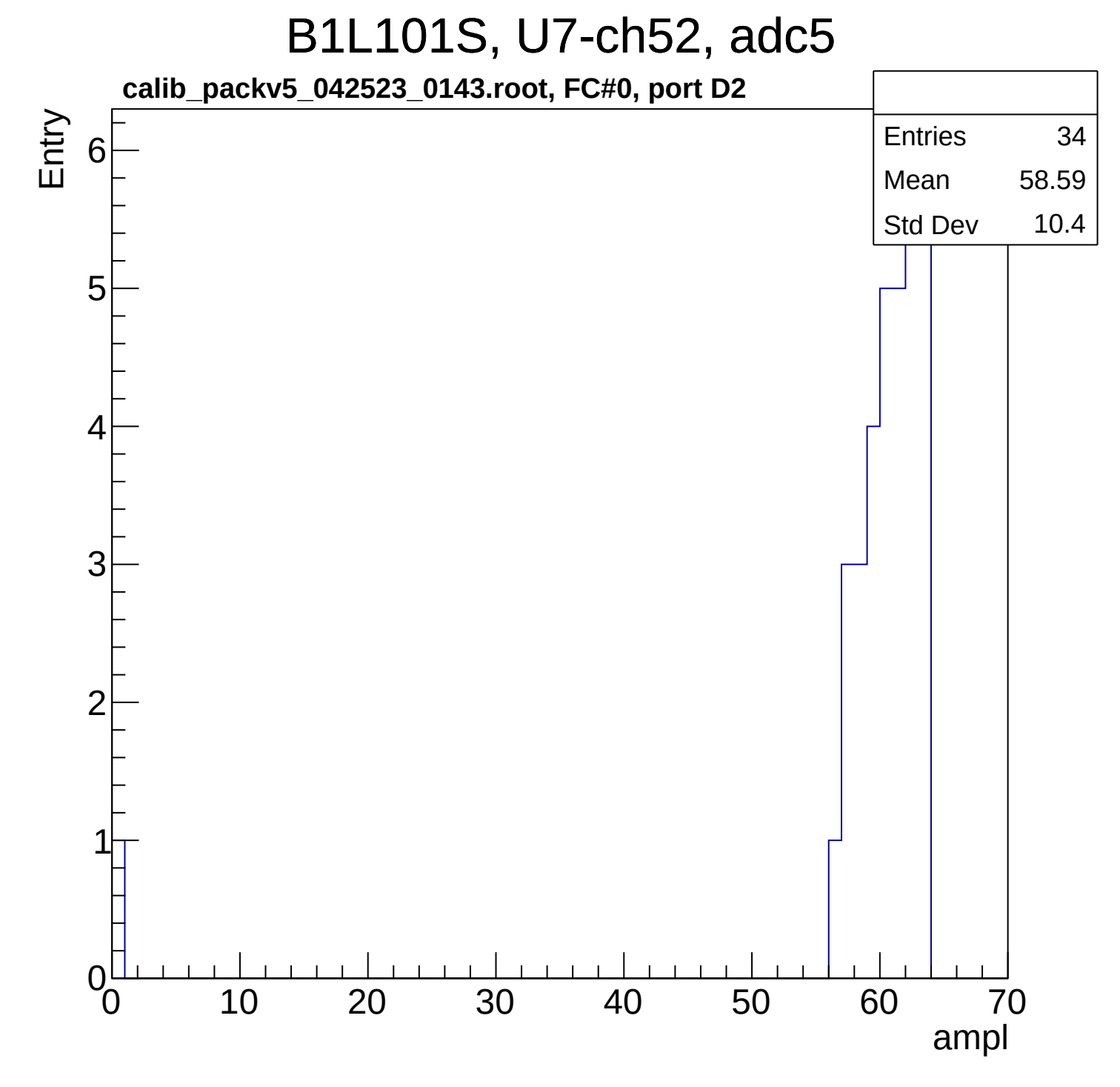
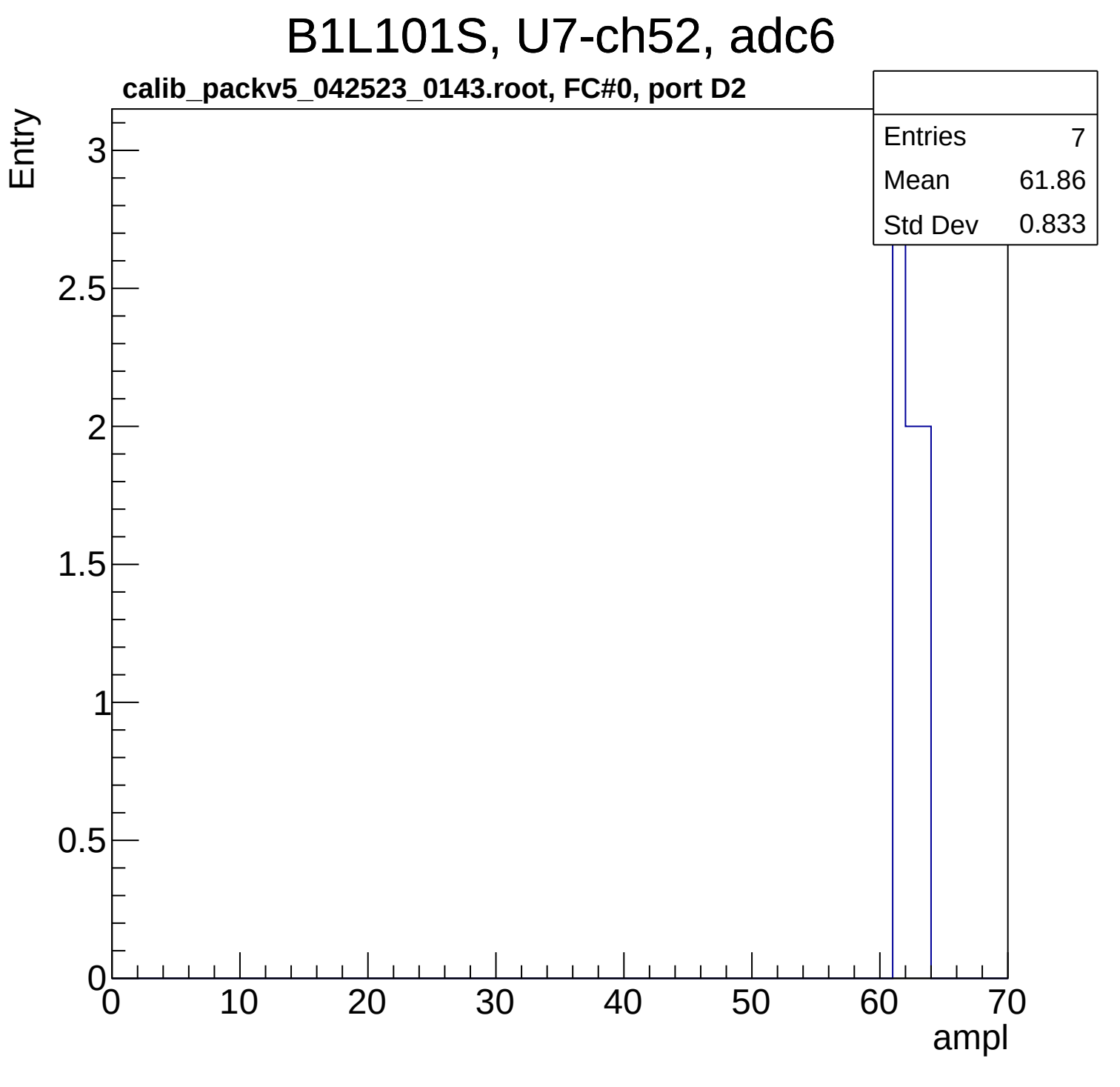

B1L101S, U7-ch52, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 34
Mean 58.59
Std Dev 10.4
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch52, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 61.86
Std Dev 0.833
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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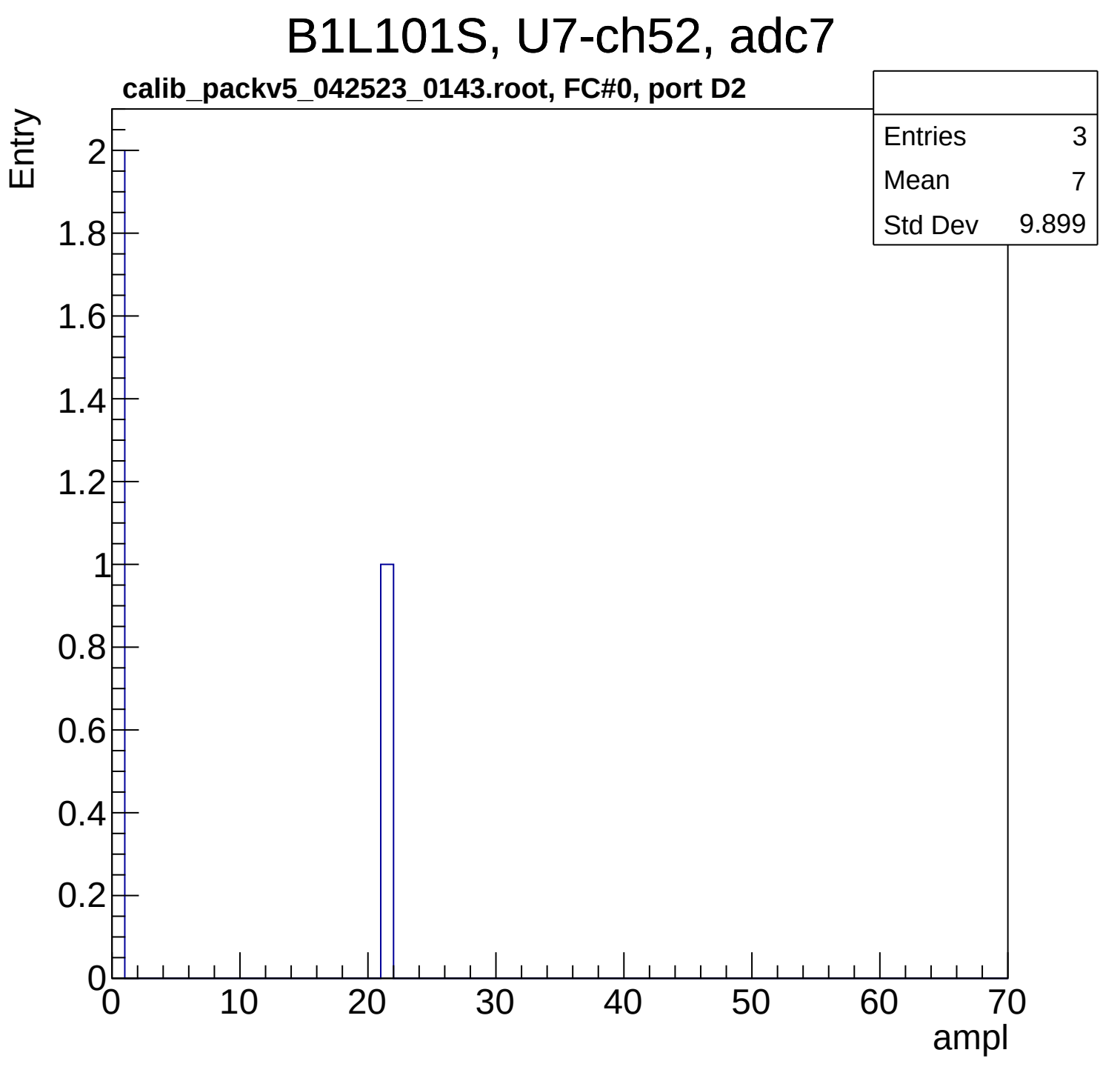
40
50
60
70


B1L101S, U7-ch52, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 7
Std Dev 9.899
Entry
ampl
0
0.2
0.4
0.6
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1.2
1.4
1.6
1.8
2
0
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40
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60
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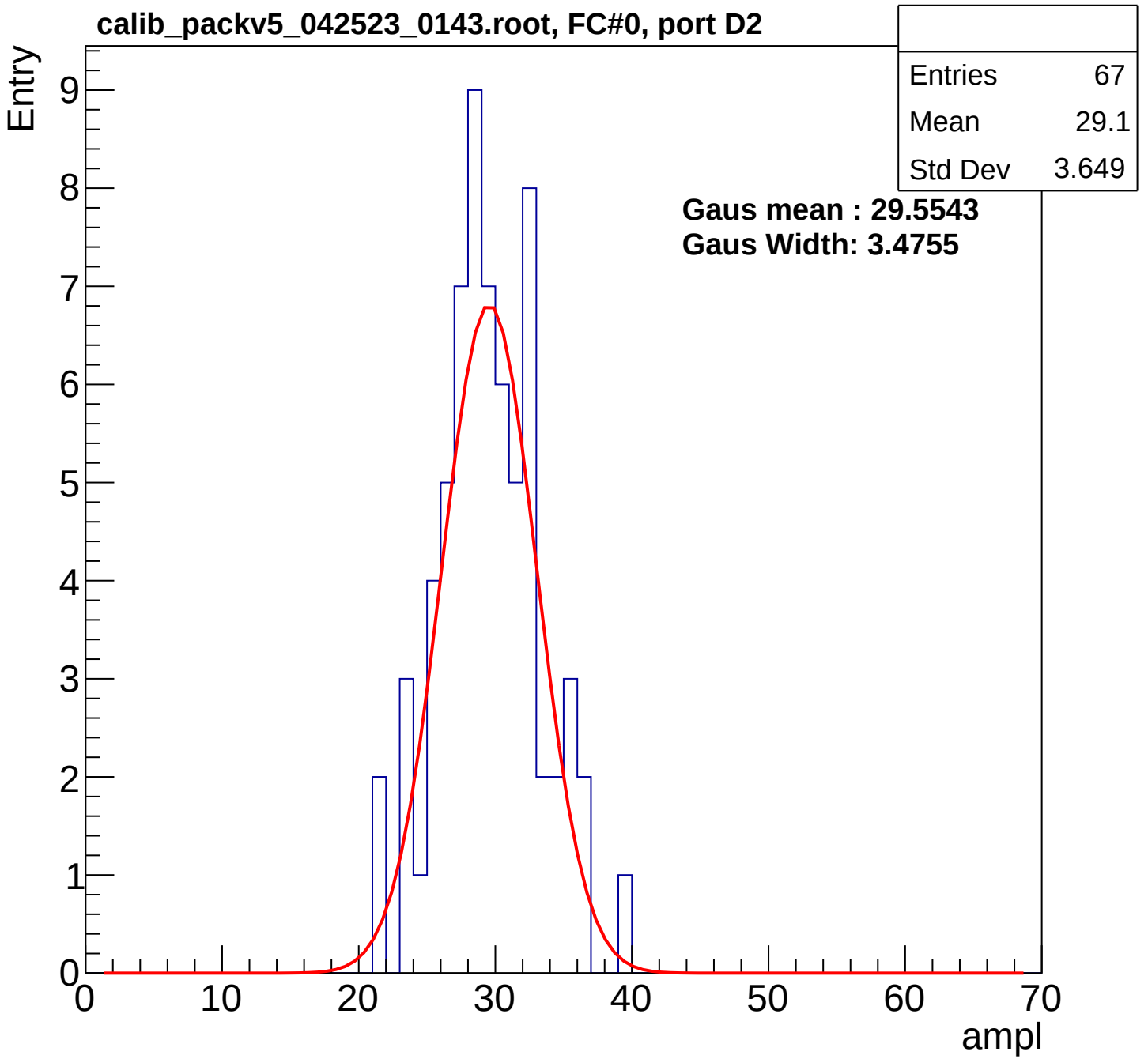
B1L101S, U7-ch53, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 29.1
Std Dev 3.649
Gaus mean : 29.5543
Gaus Width: 3.4755
Entry
ampl
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2
3
4
5
6
7
8
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0
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20
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40
50
60
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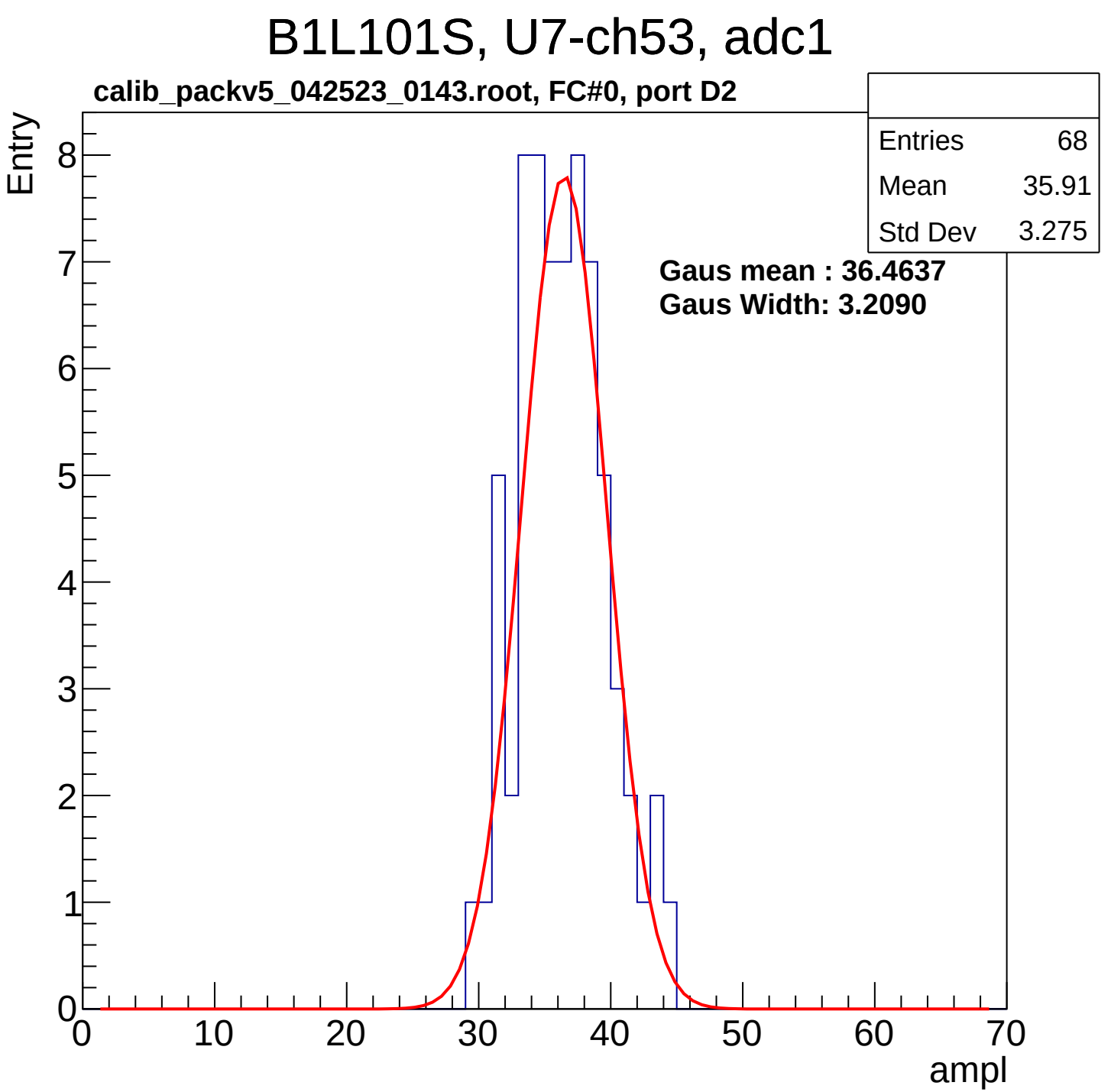
B1L101S, U7-ch53, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 35.91
Std Dev 3.275
Gaus mean : 36.4637
Gaus Width: 3.2090
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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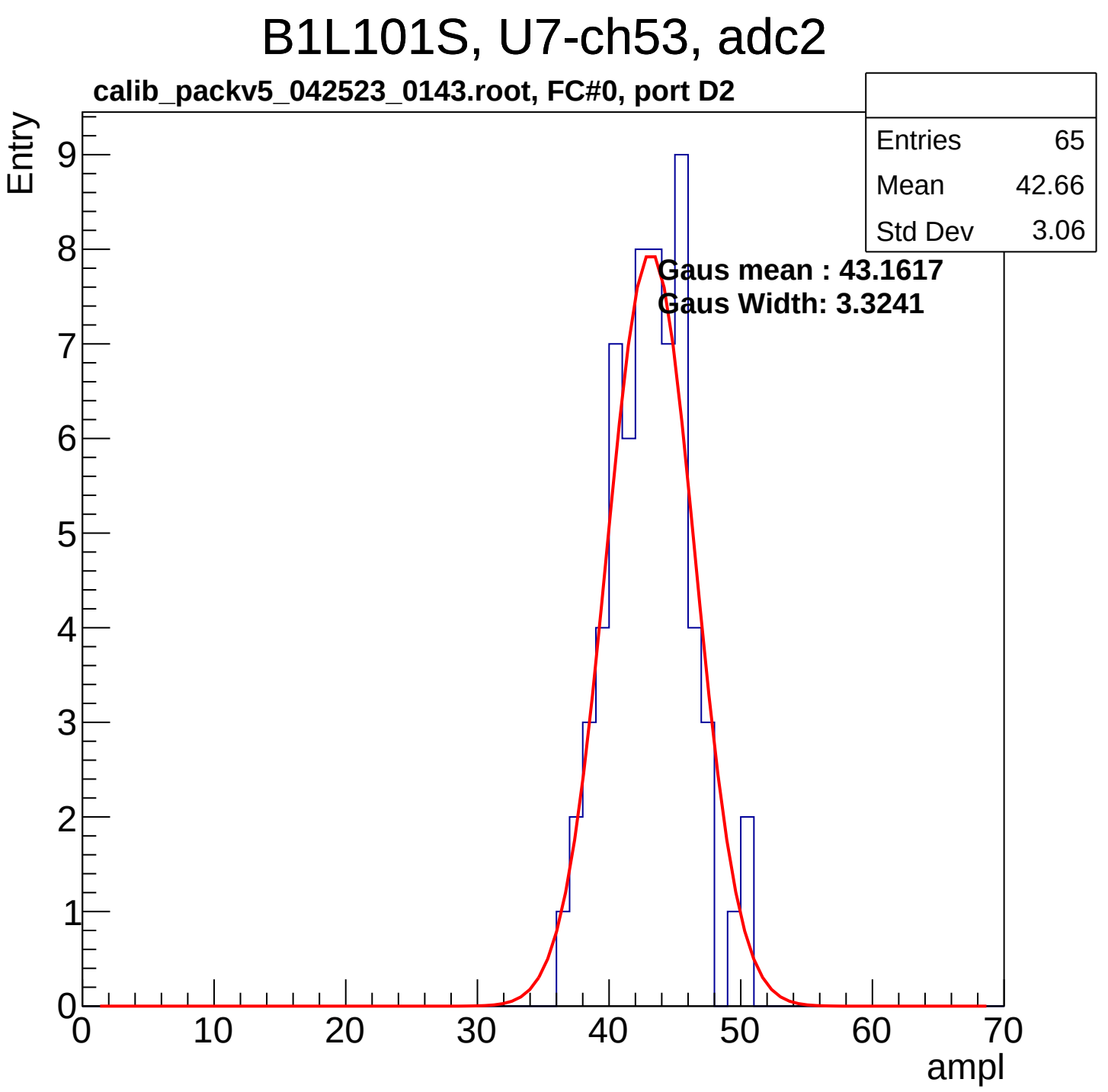
B1L101S, U7-ch53, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 42.66
Std Dev 3.06
Gaus mean : 43.1617
Gaus Width: 3.3241
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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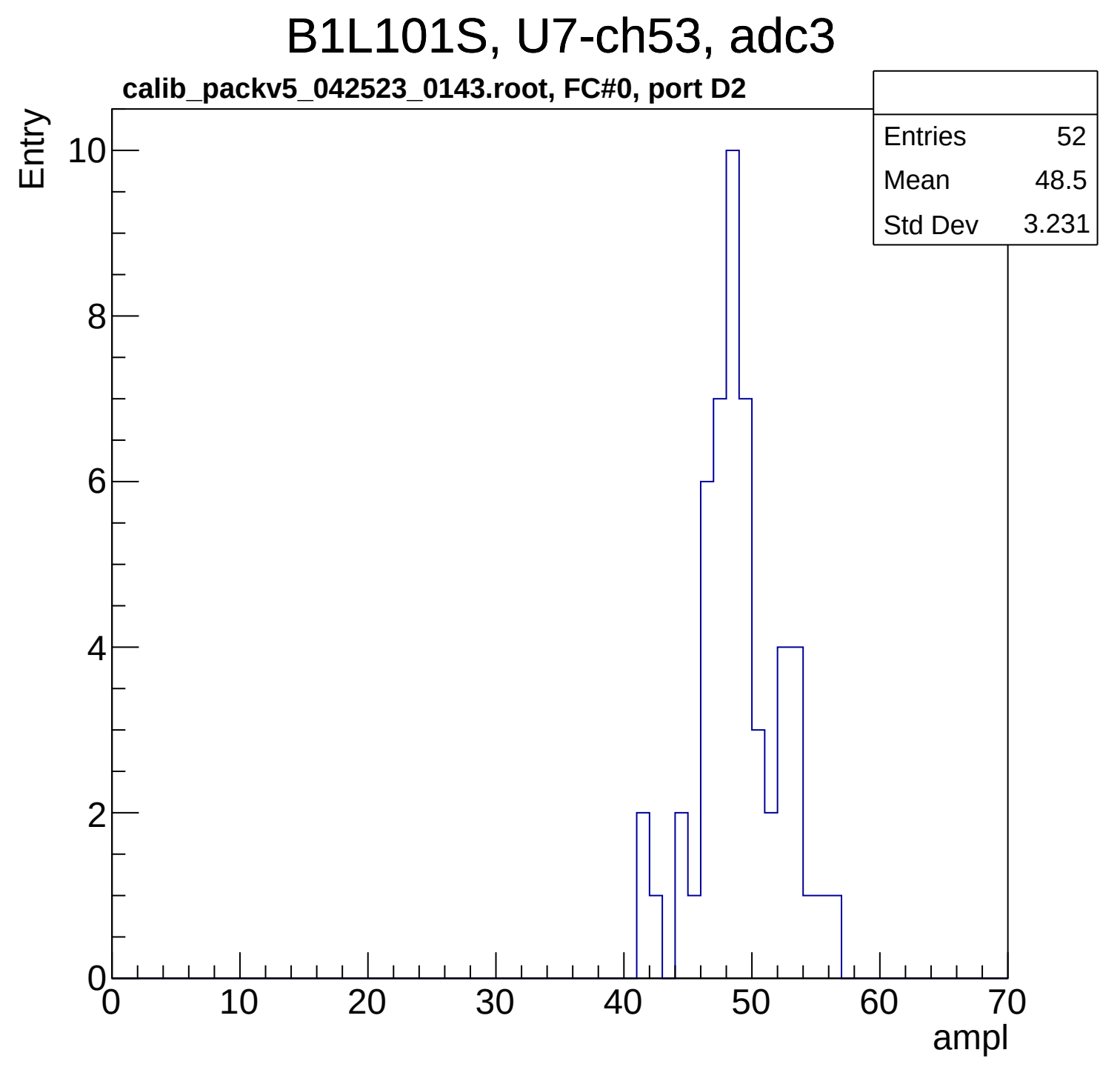
B1L101S, U7-ch53, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 48.5
Std Dev 3.231
Entry
ampl
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4
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0
10
20
30
40
50
60
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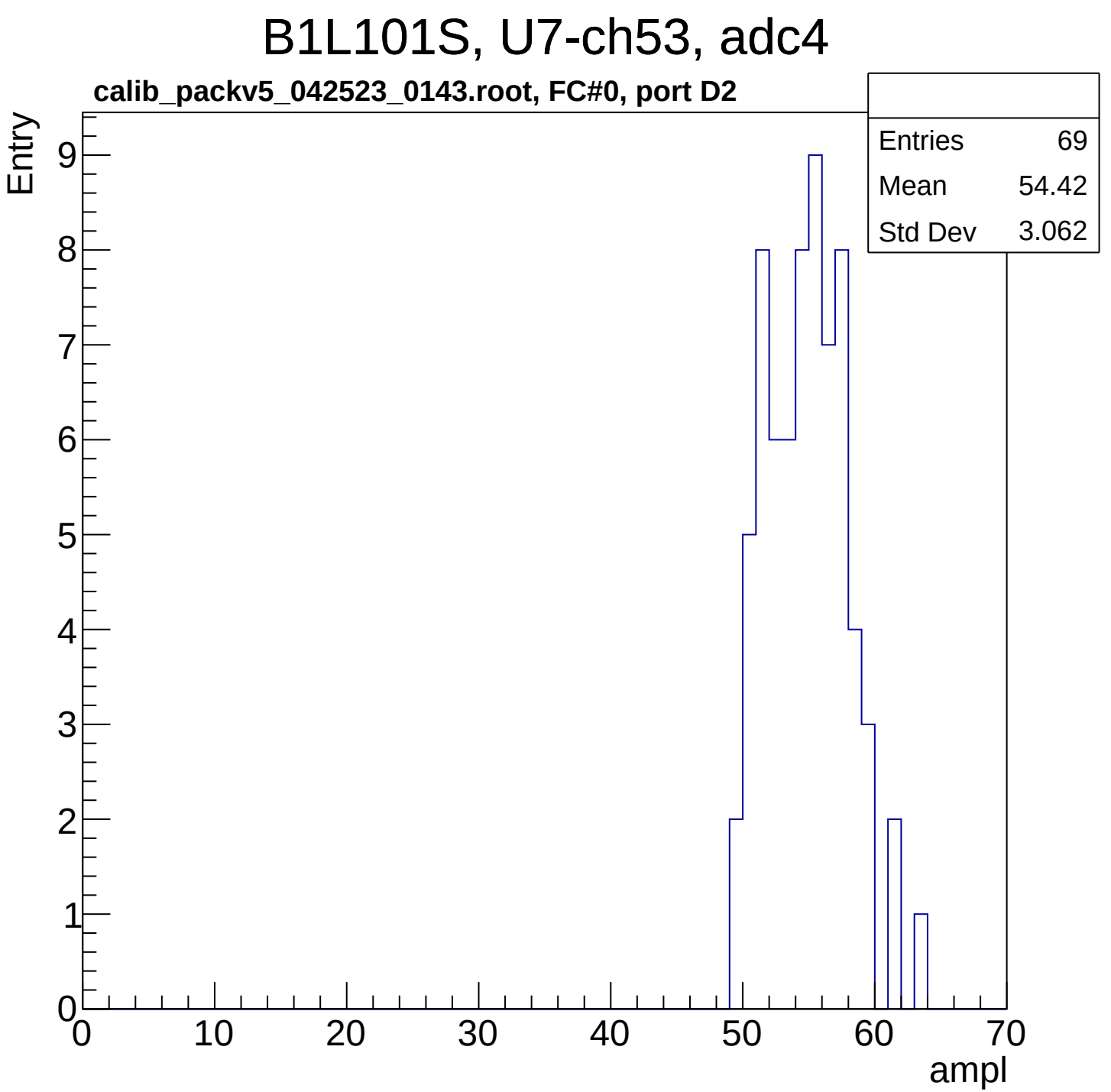
B1L101S, U7-ch53, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 54.42
Std Dev 3.062
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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30
40
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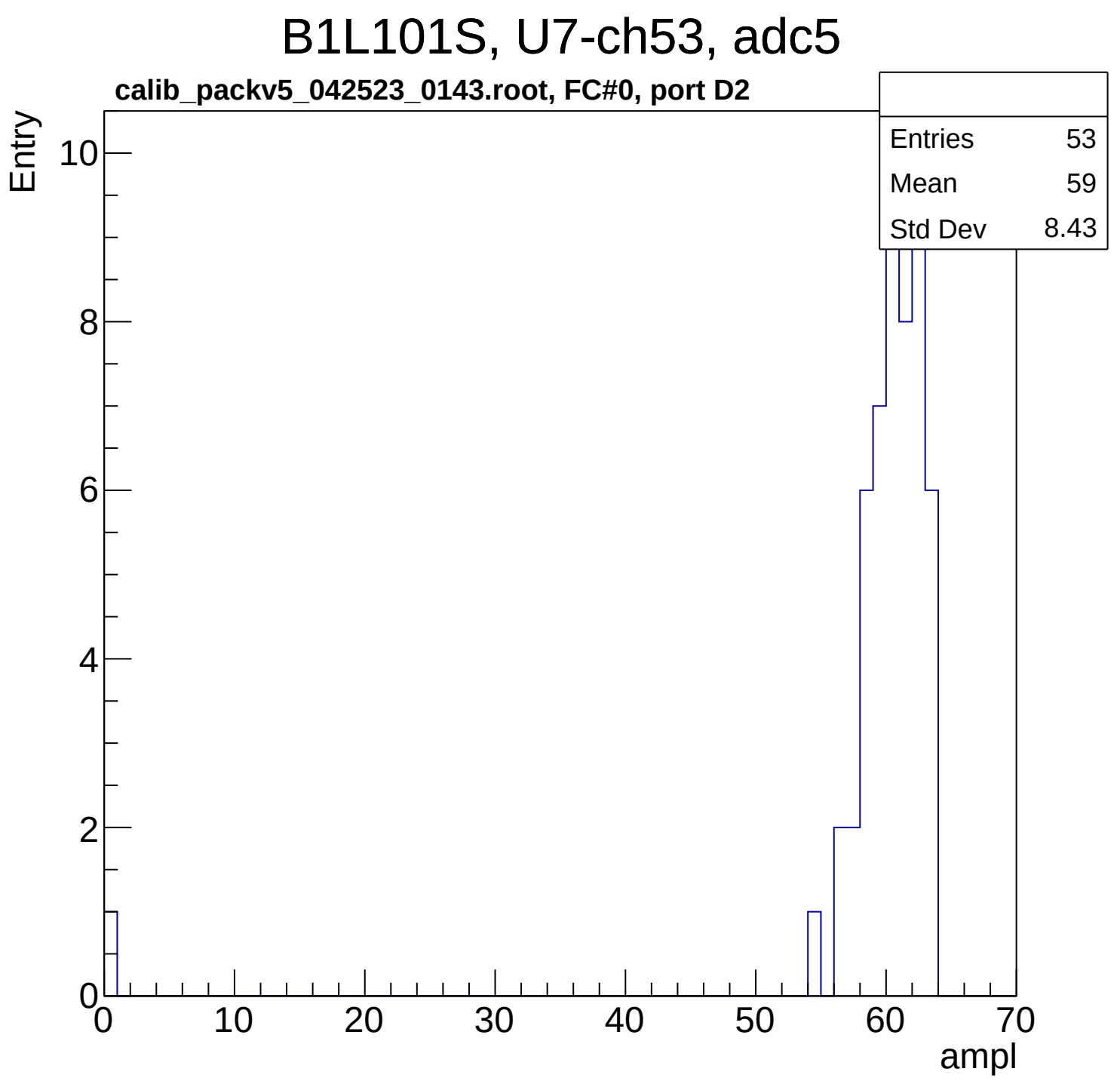
B1L101S, U7-ch53, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 59
Std Dev 8.43
Entry
0
2
4
6
8
10
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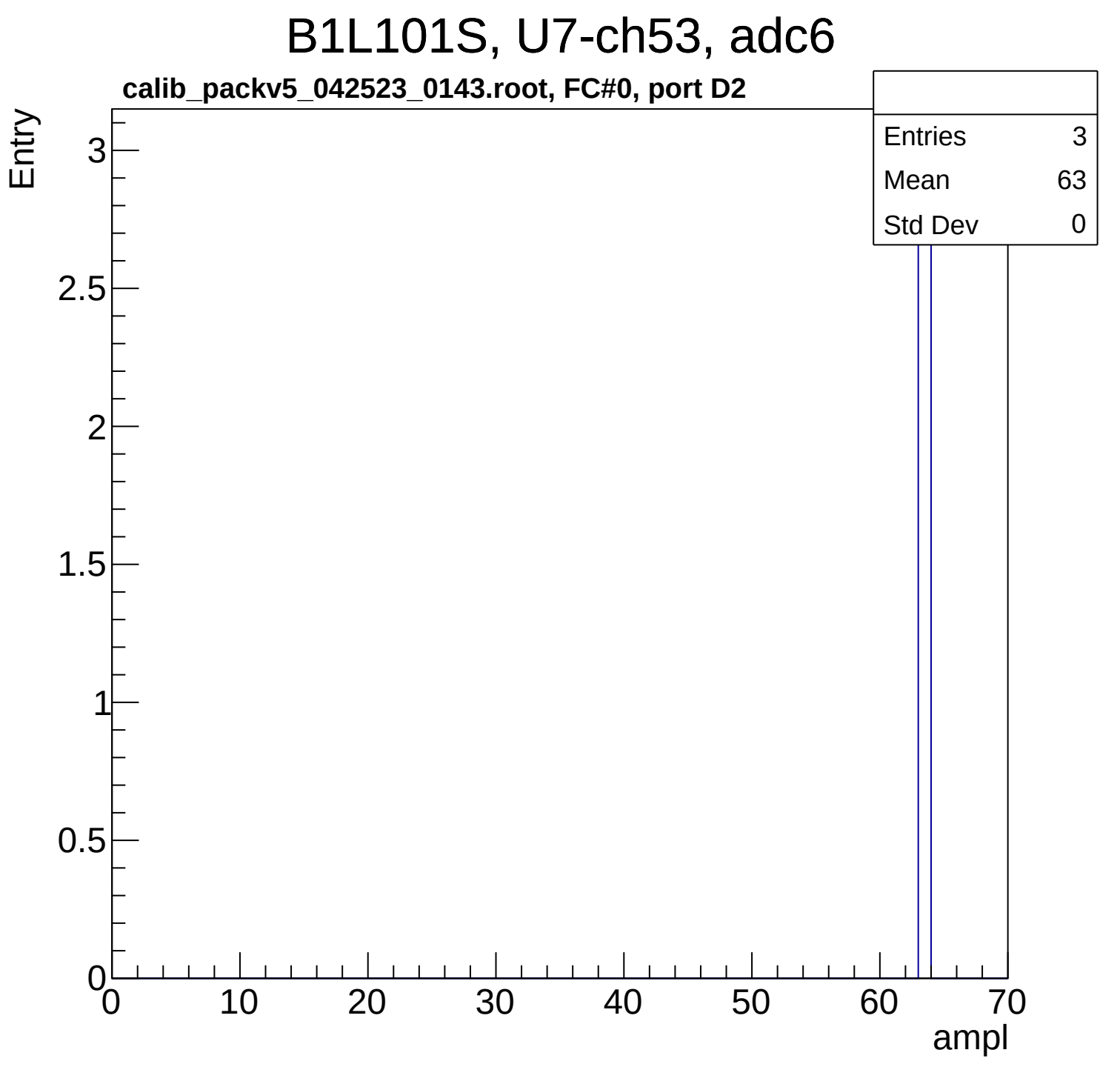
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch53, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 63
Std Dev 0
Entry
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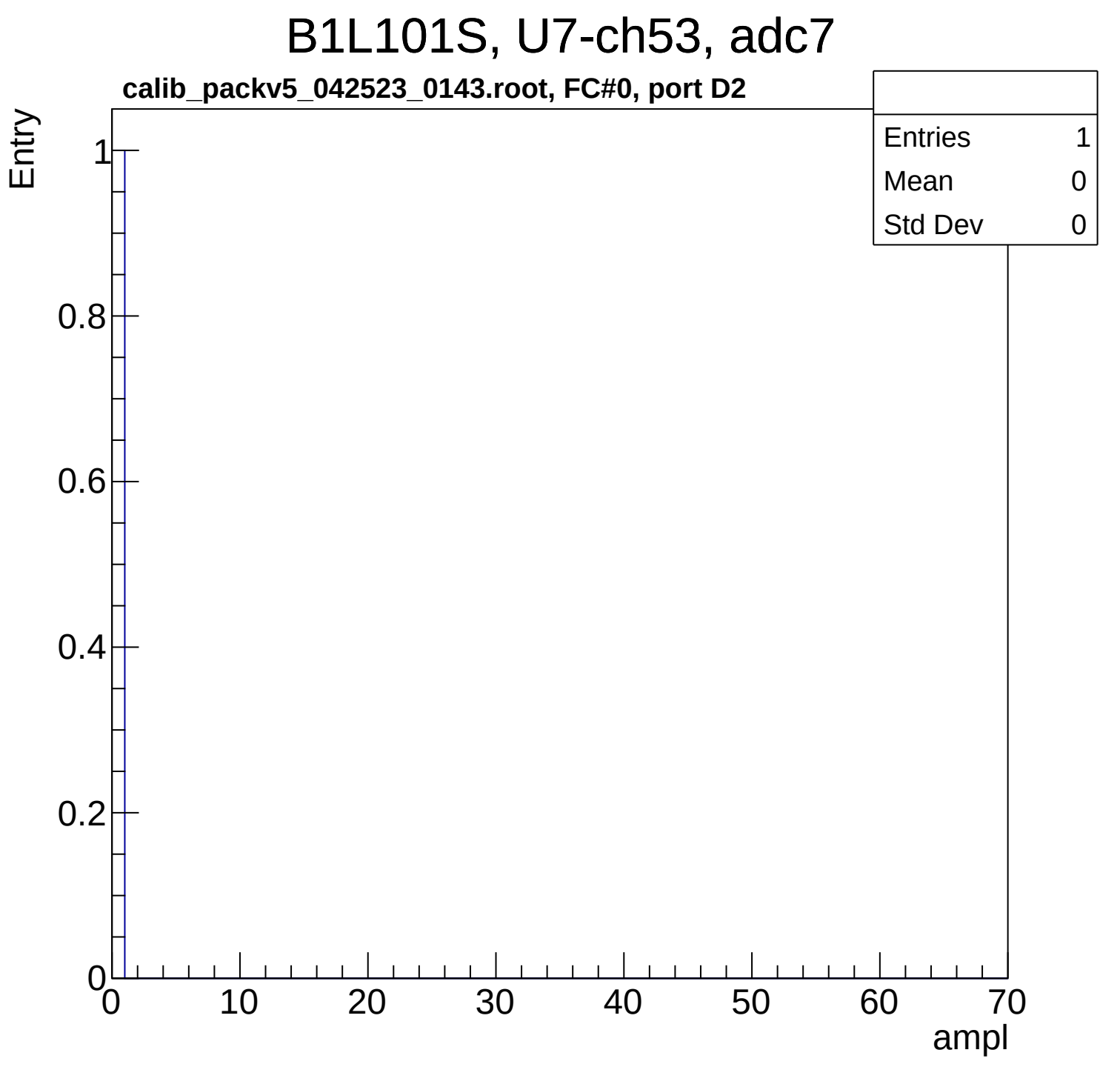
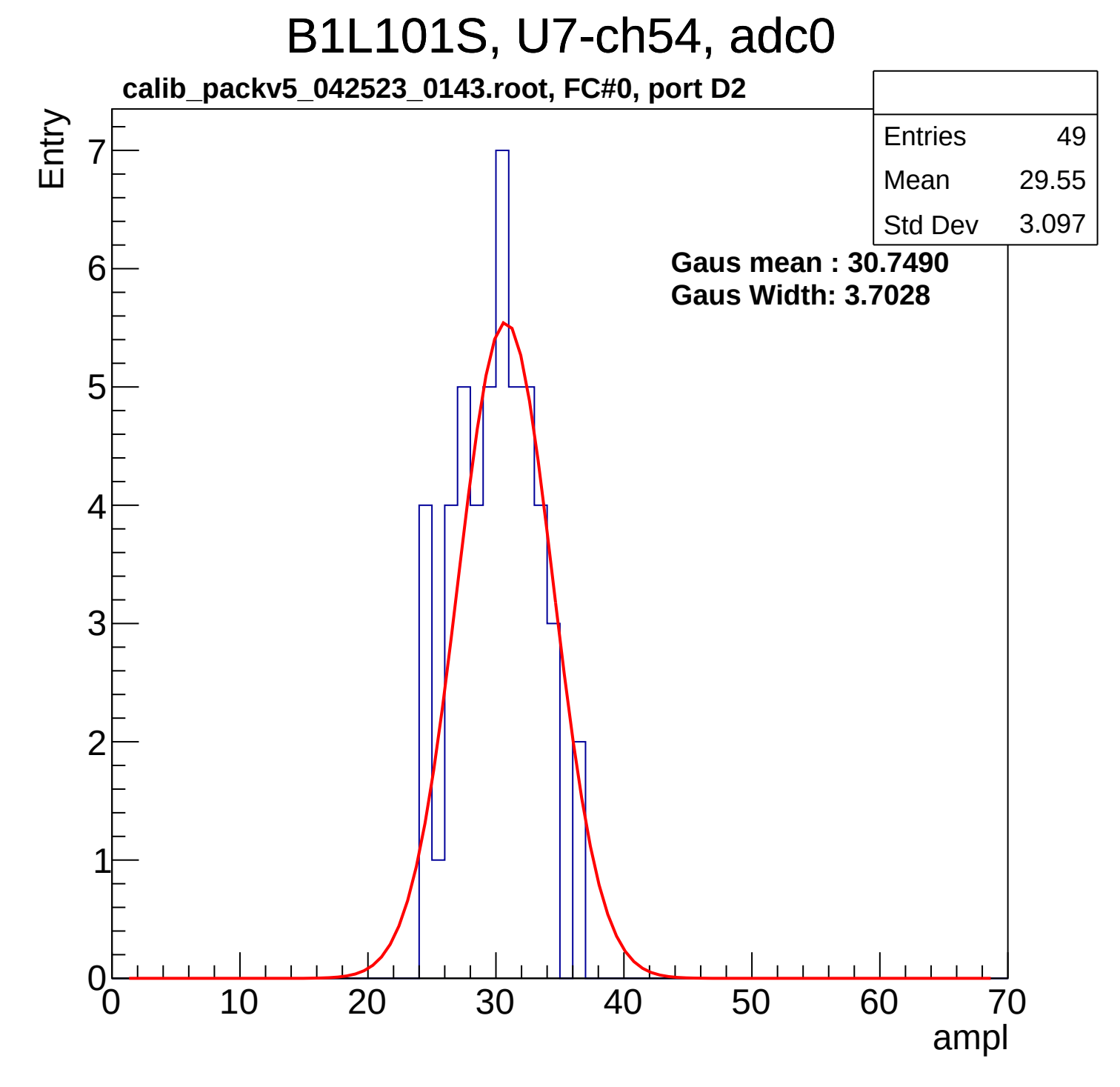
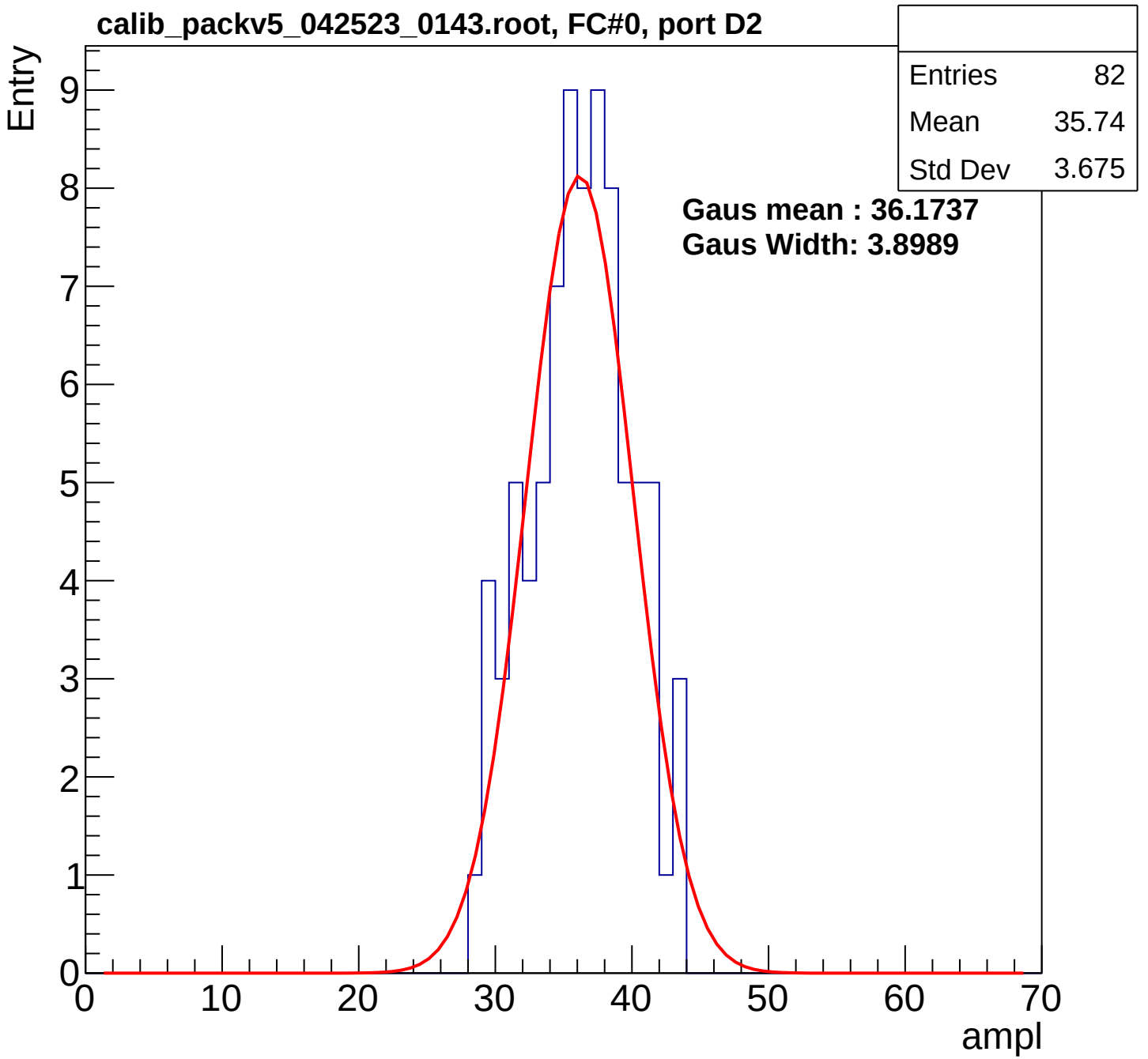
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch53, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch54, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 29.55
Std Dev 3.097
Gaus mean : 30.7490
Gaus Width: 3.7028
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U7-ch54, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 82
Mean 35.74
Std Dev 3.675
Gaus mean : 36.1737
Gaus Width: 3.8989
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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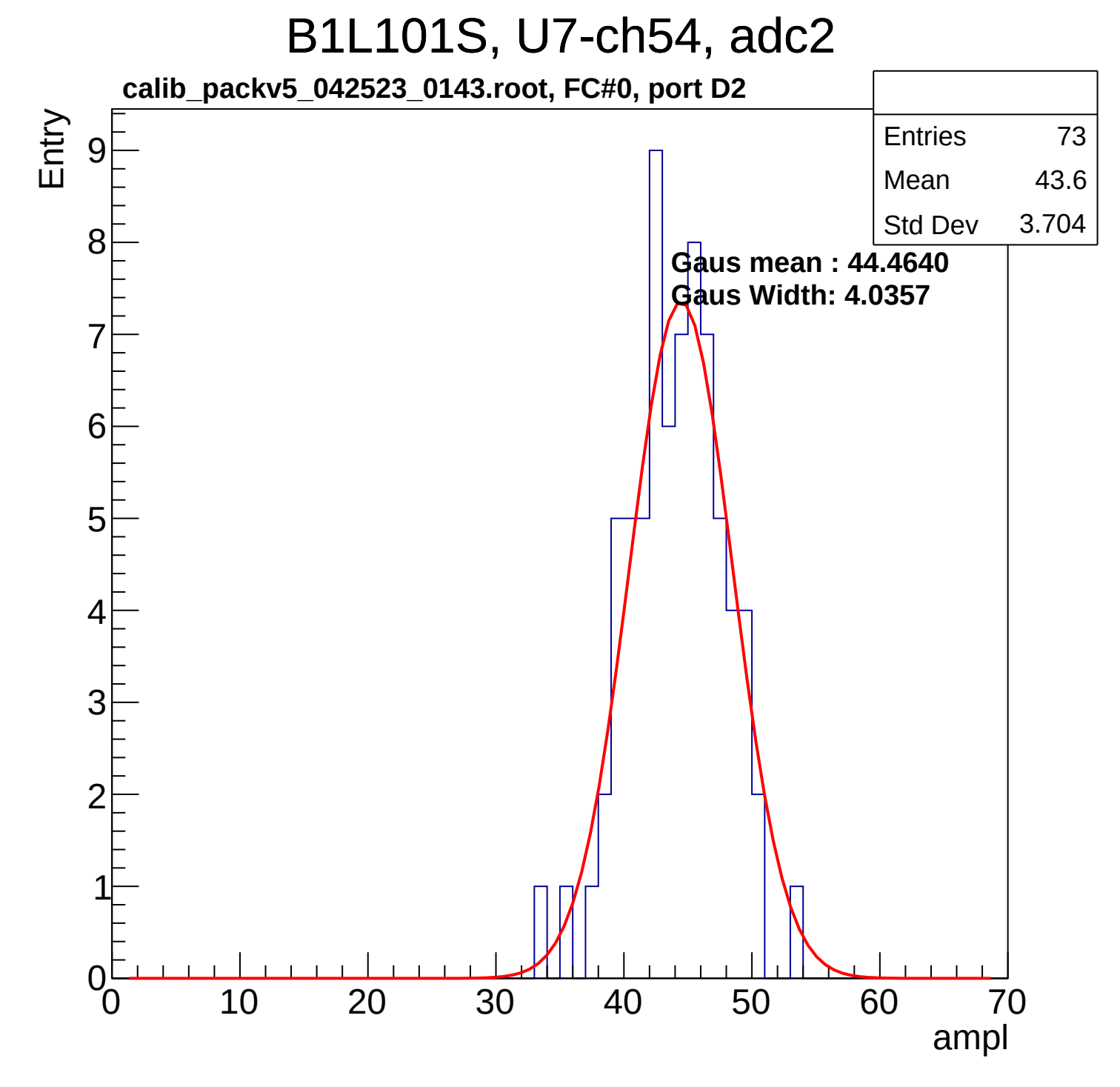
B1L101S, U7-ch54, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 43.6
Std Dev 3.704
Gaus mean : 44.4640
Gaus Width: 4.0357
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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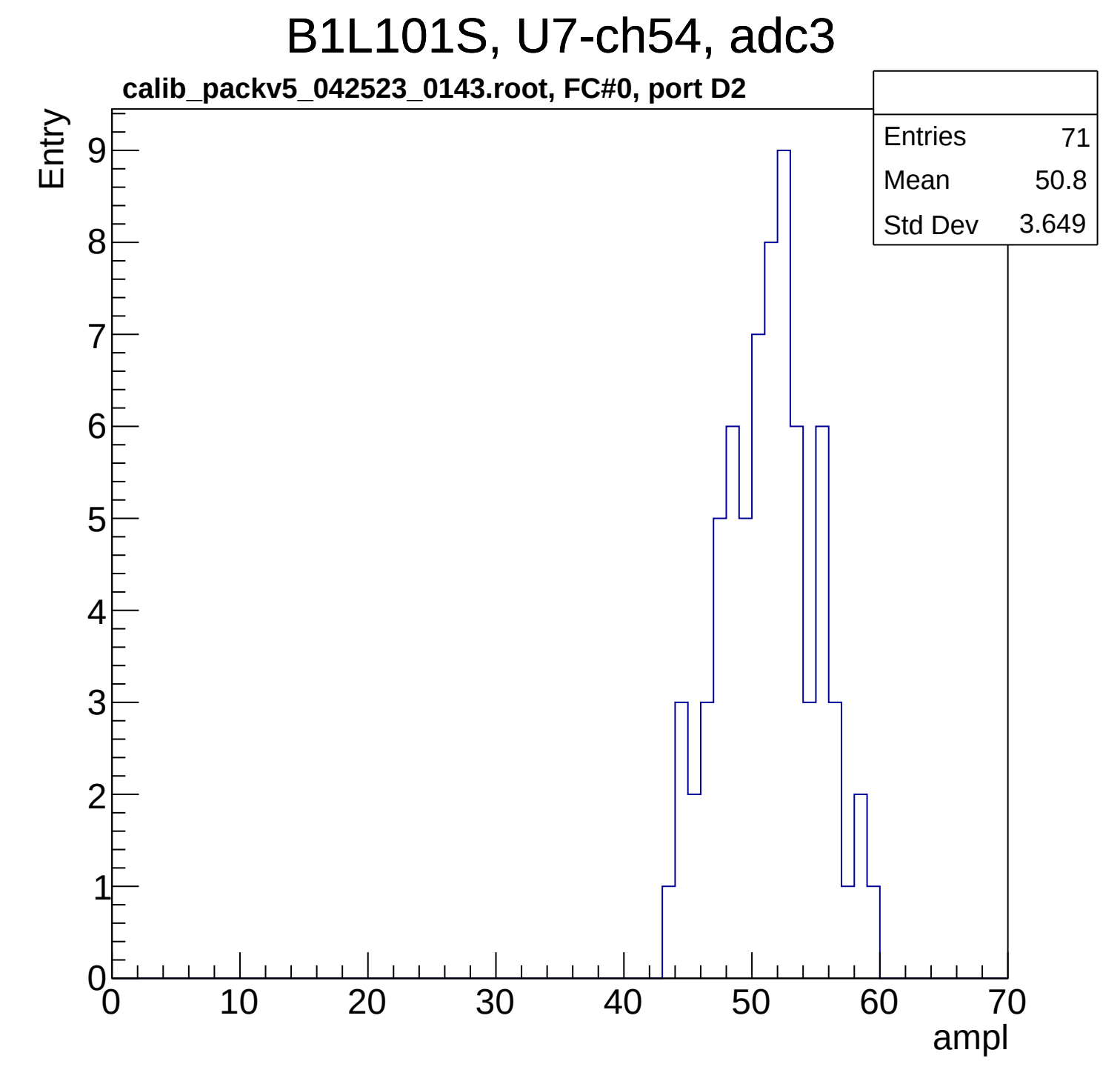
B1L101S, U7-ch54, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 50.8
Std Dev 3.649
Entry
ampl
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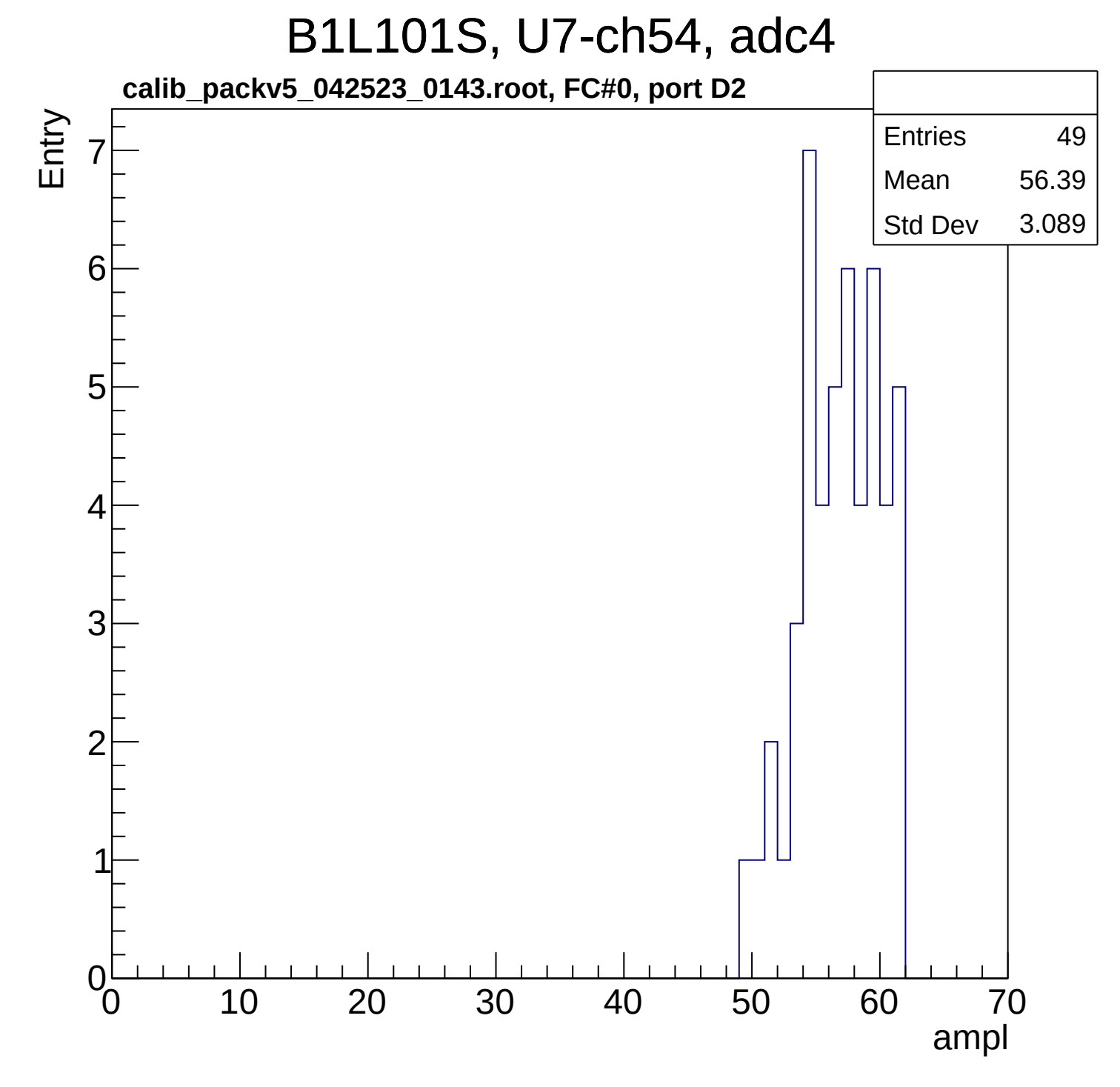
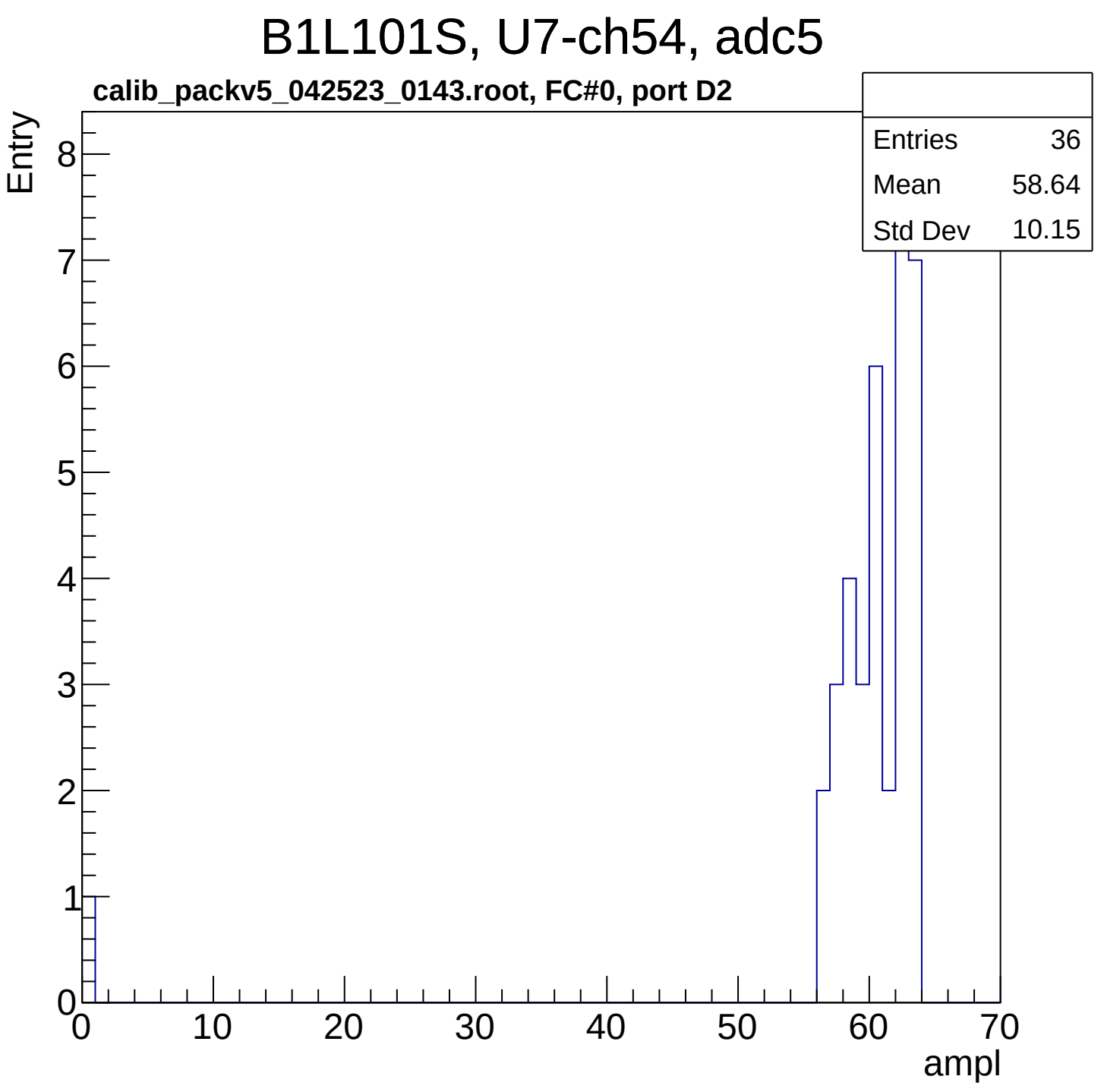
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch54, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 56.39
Std Dev 3.089
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U7-ch54, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 36
Mean 58.64
Std Dev 10.15
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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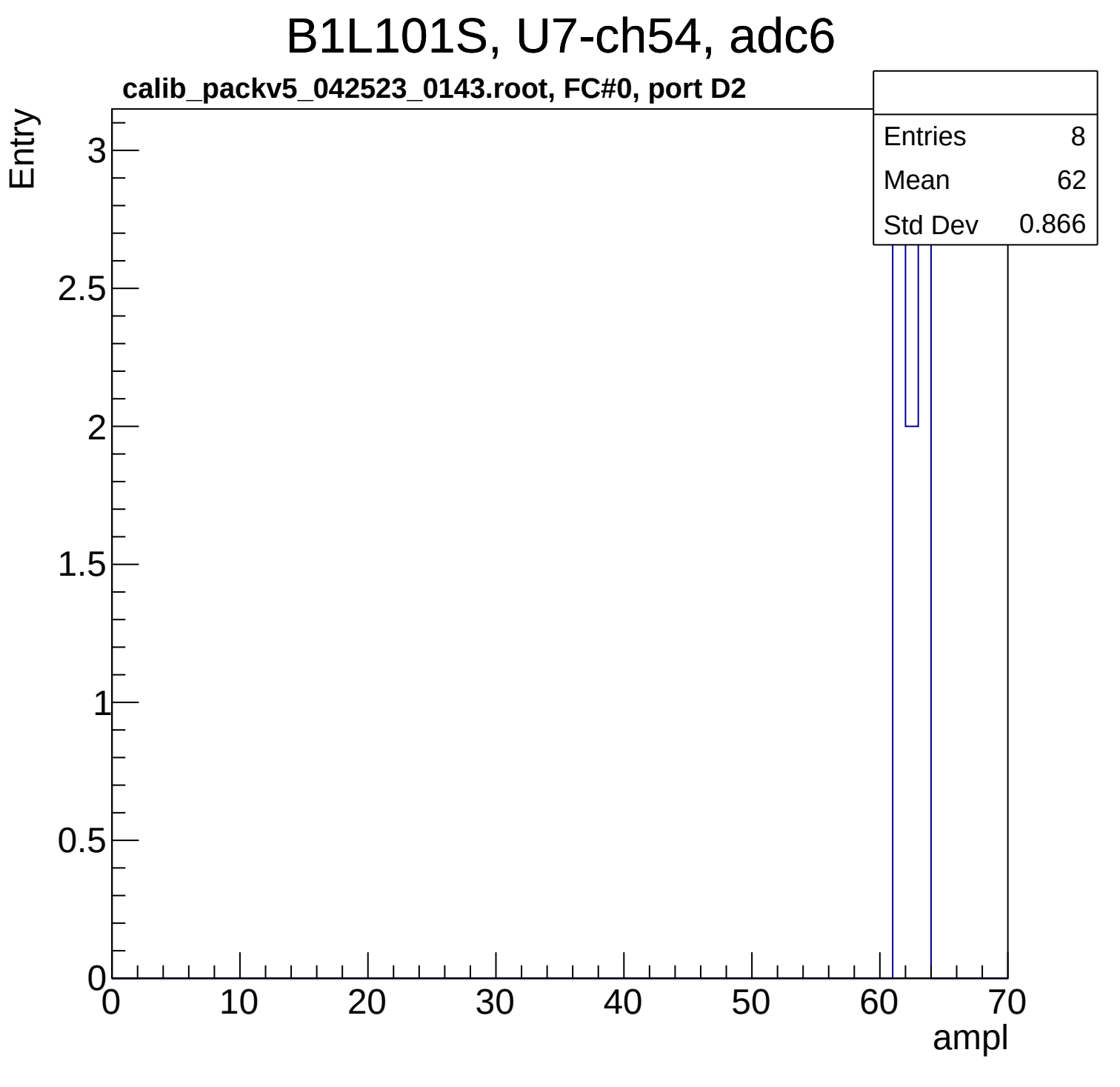
B1L101S, U7-ch54, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 62
Std Dev 0.866
Entry
ampl
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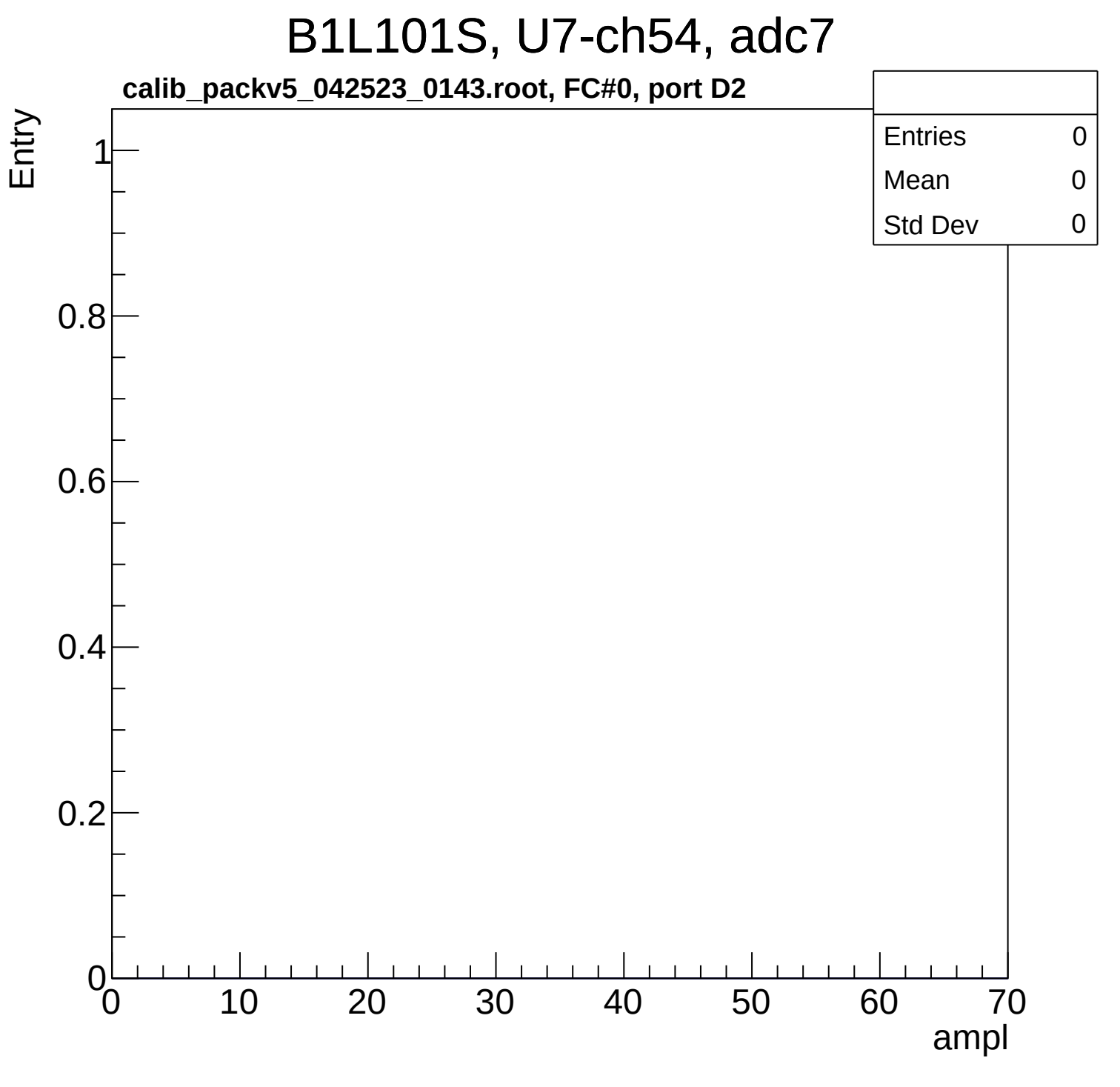
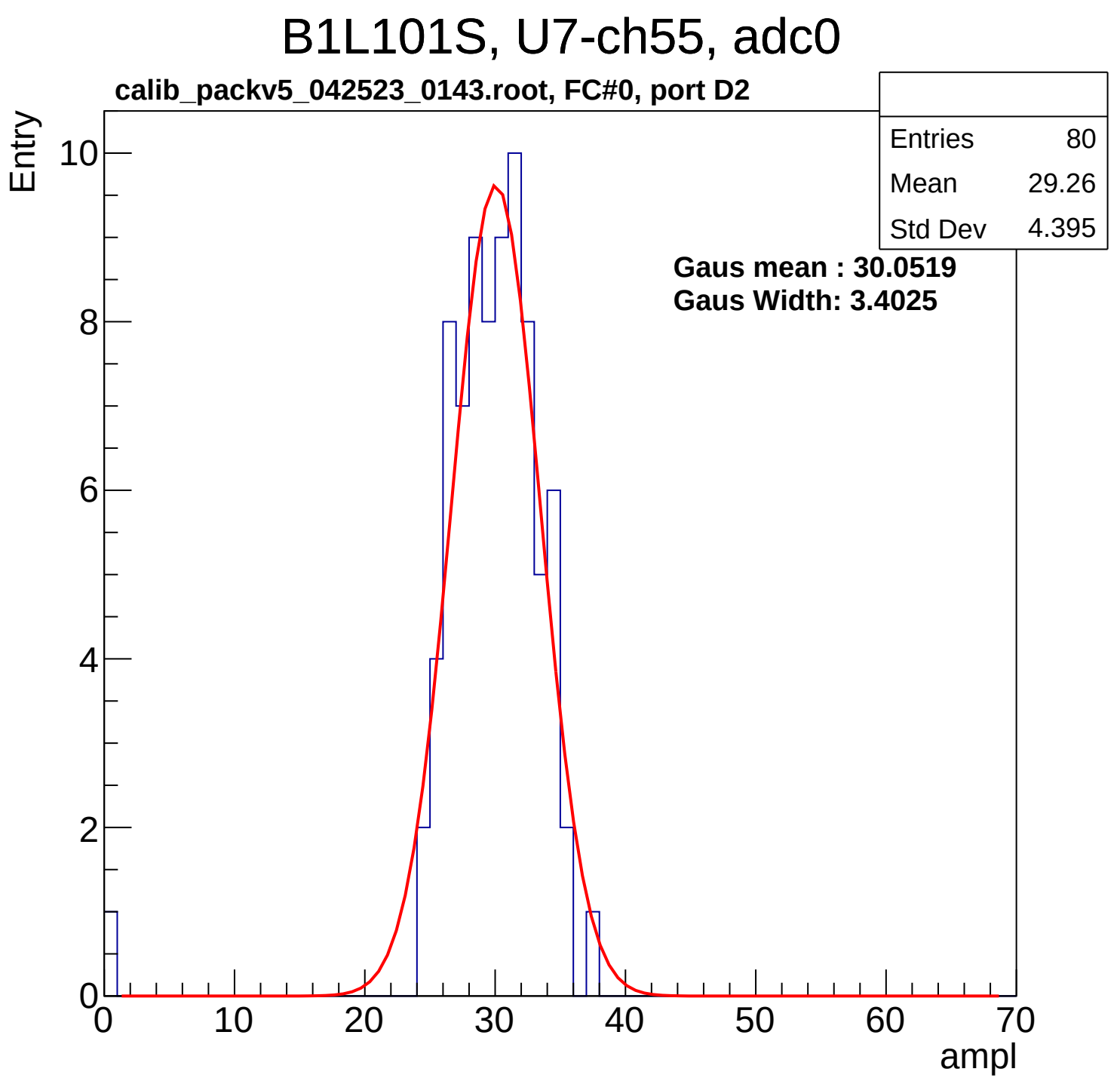
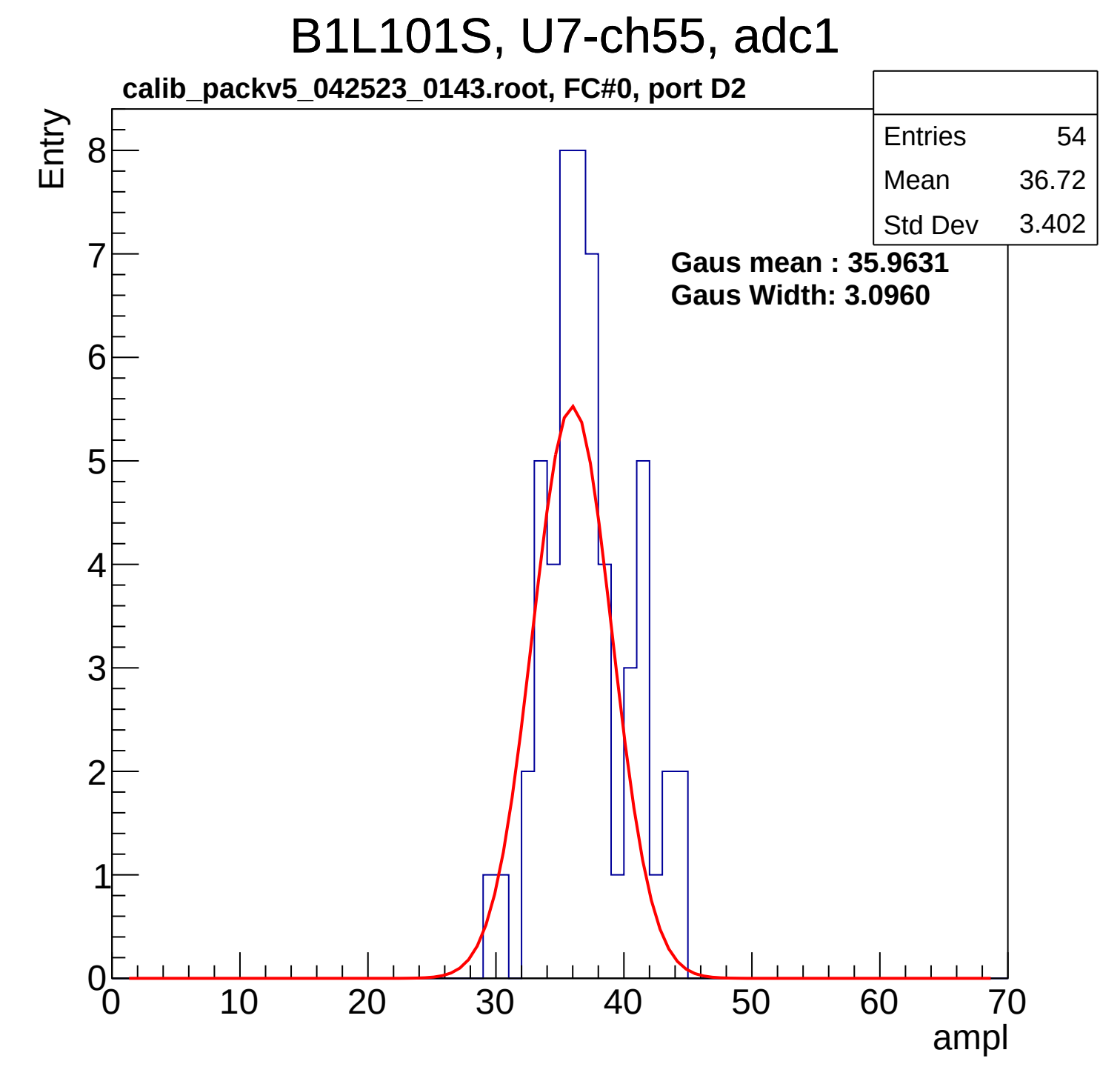
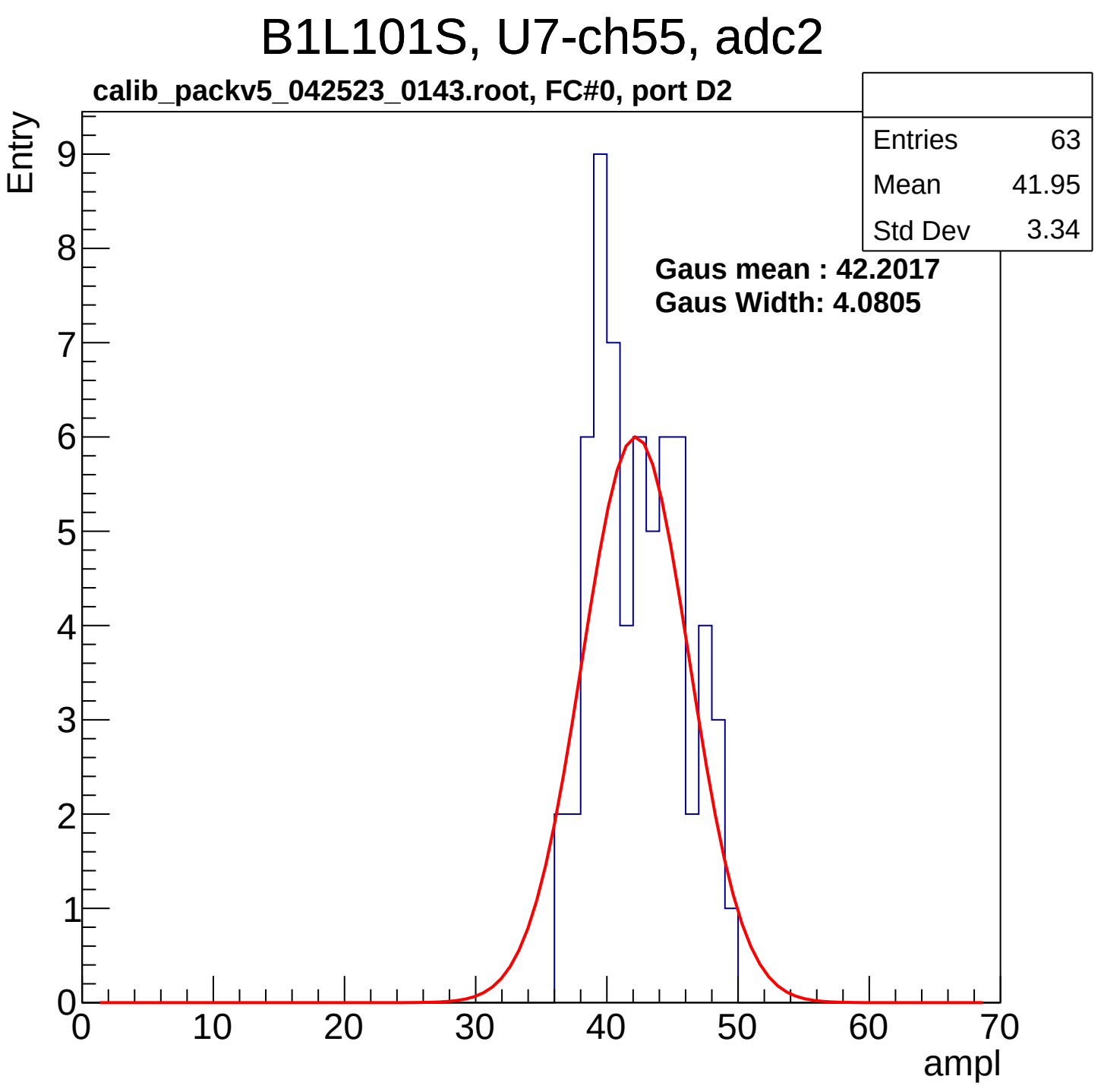
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U7-ch54, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch55, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 80
Mean 29.26
Std Dev 4.395
Gaus mean : 30.0519
Gaus Width: 3.4025
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch55, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 36.72
Std Dev 3.402
Gaus mean : 35.9631
Gaus Width: 3.0960
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch55, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 41.95
Std Dev 3.34
Gaus mean : 42.2017
Gaus Width: 4.0805
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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40
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60
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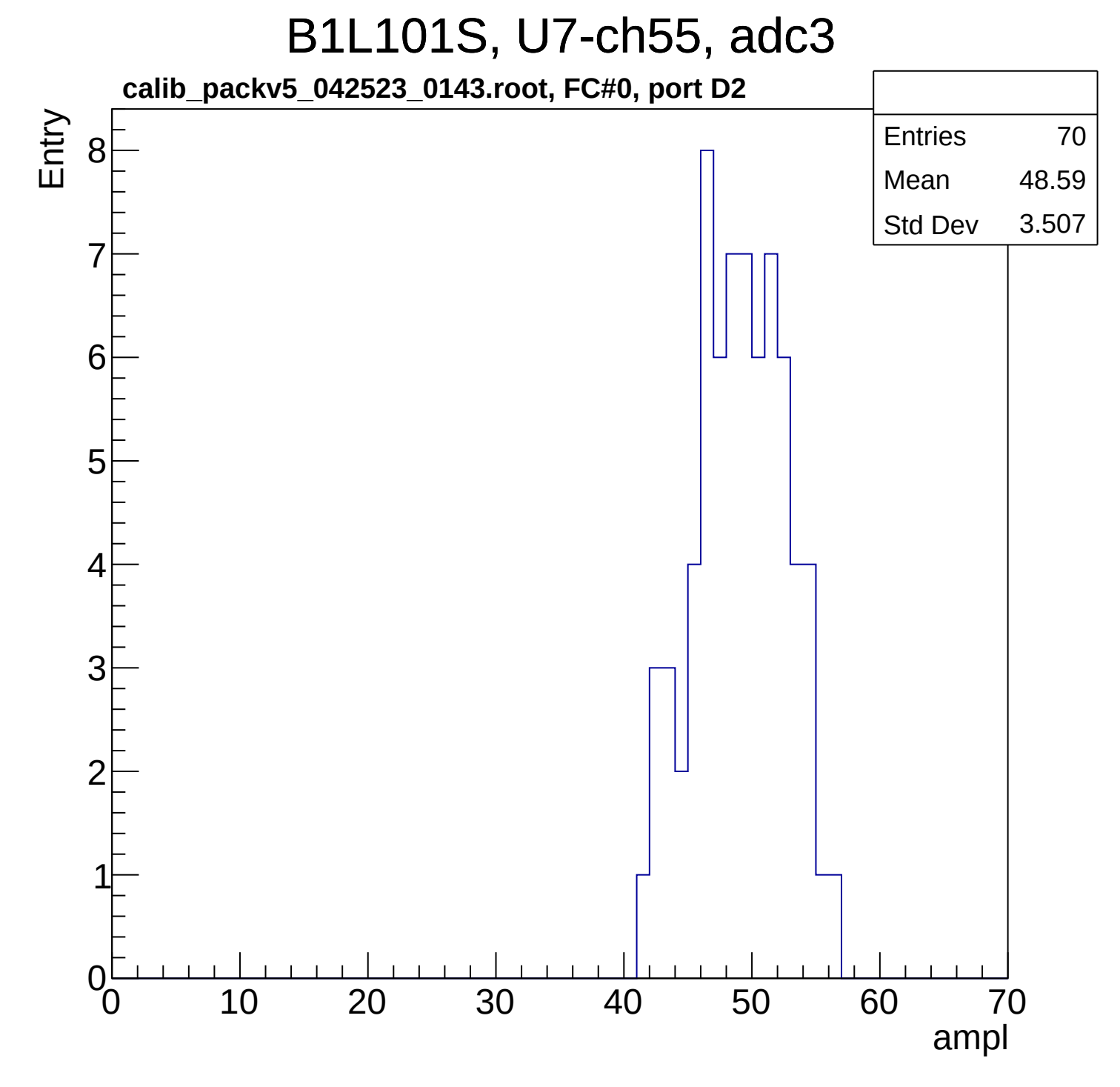
B1L101S, U7-ch55, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 48.59
Std Dev 3.507
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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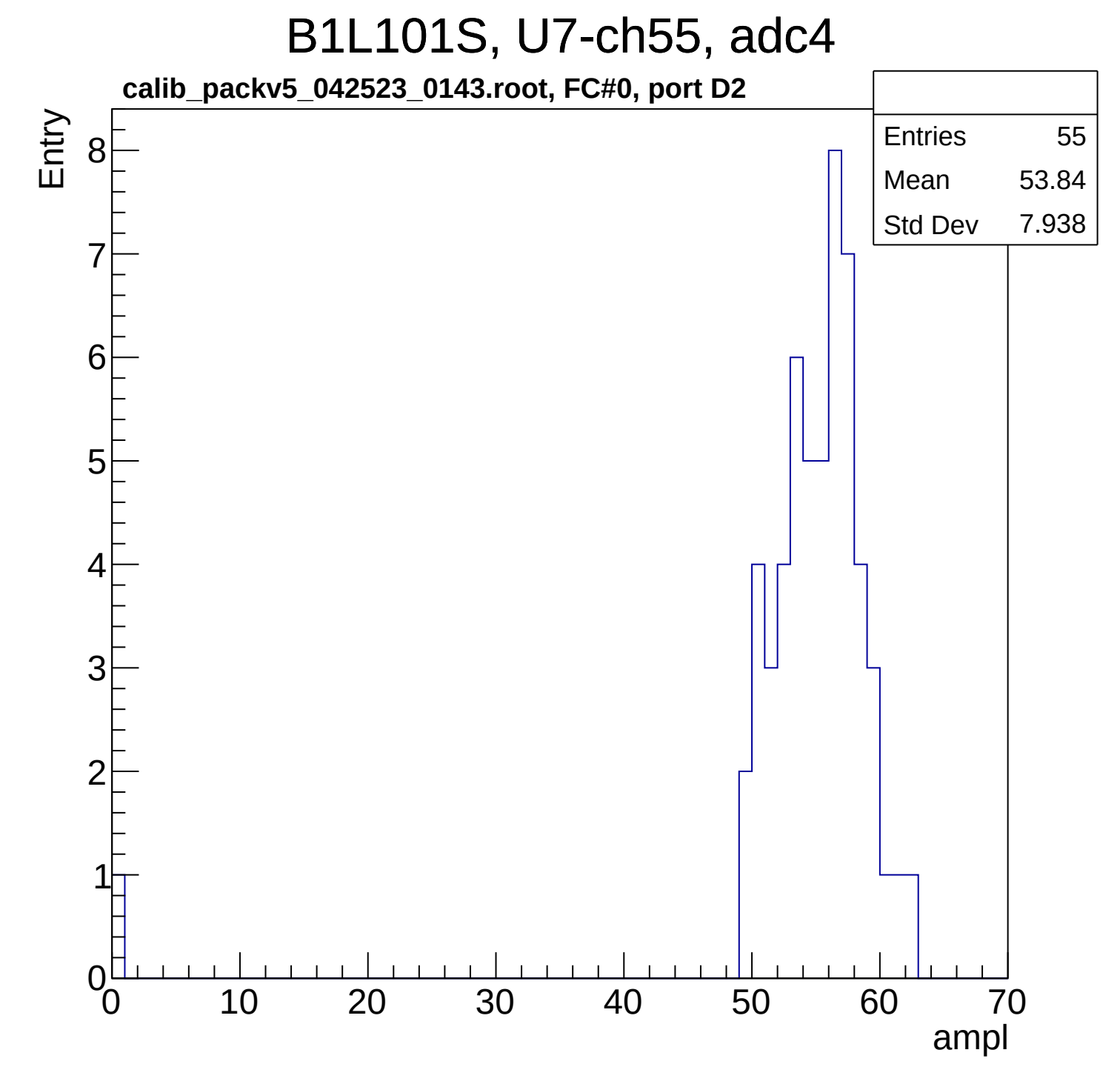
B1L101S, U7-ch55, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 53.84
Std Dev 7.938
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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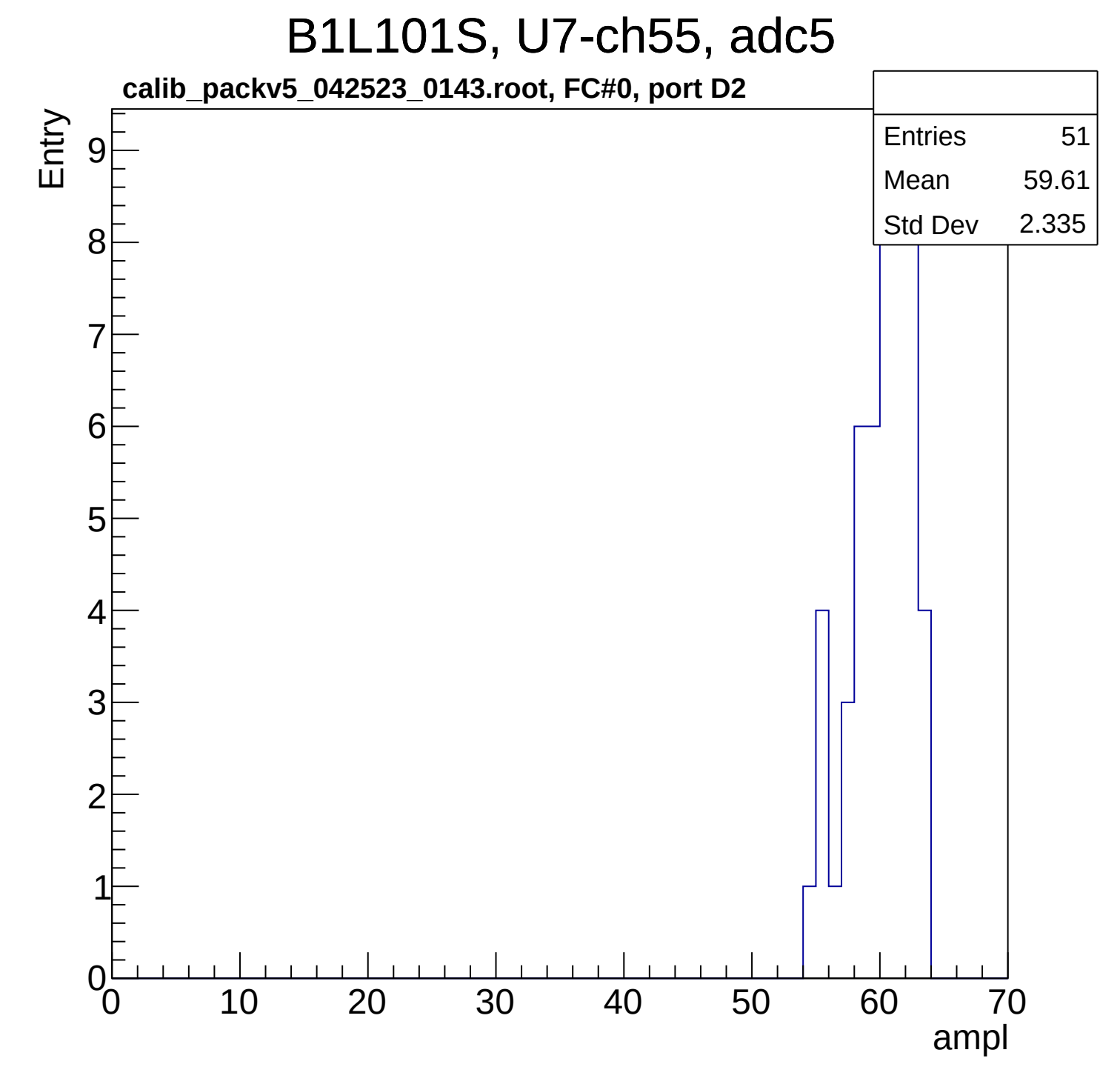
B1L101S, U7-ch55, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 59.61
Std Dev 2.335
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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50
60
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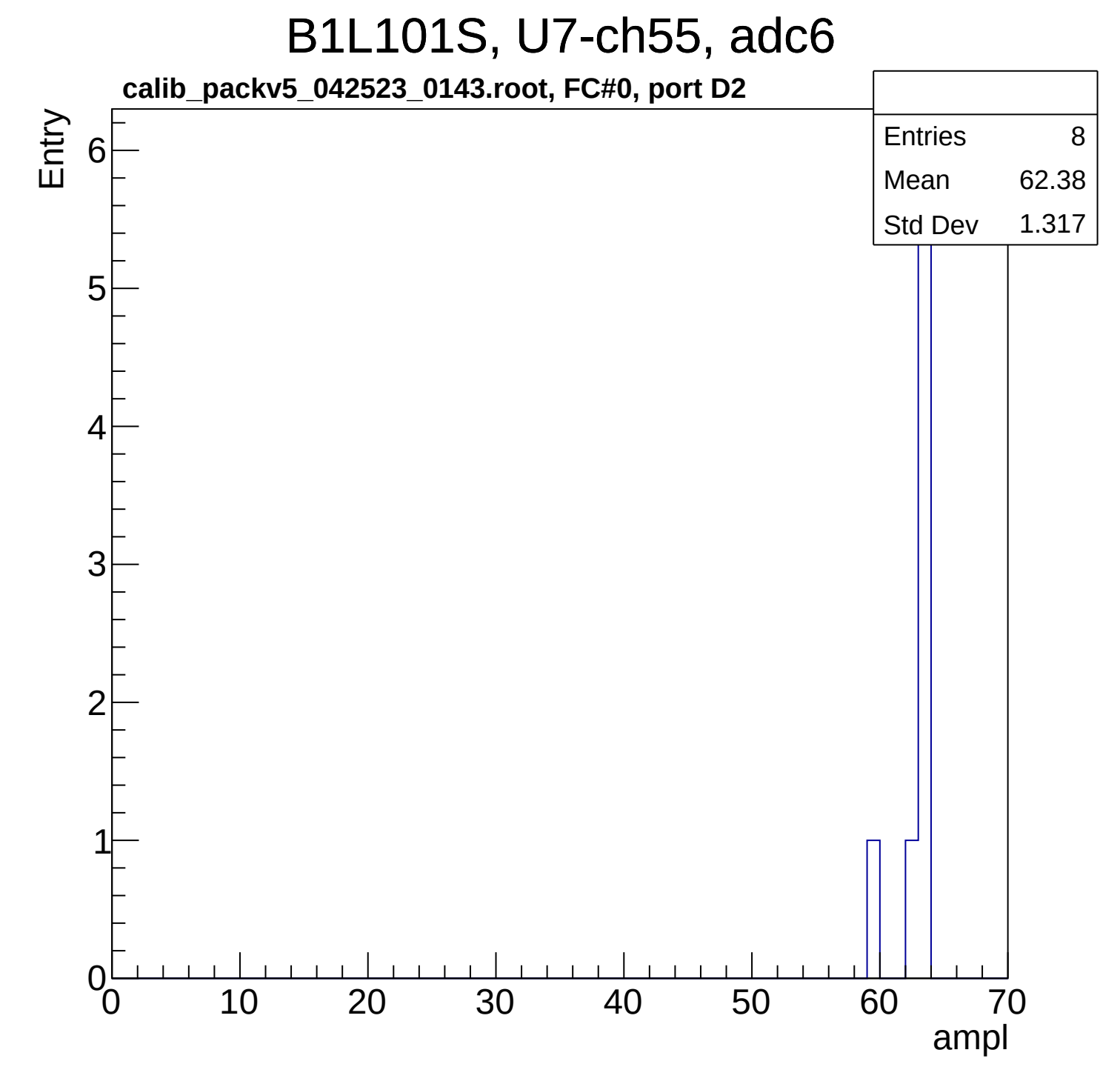
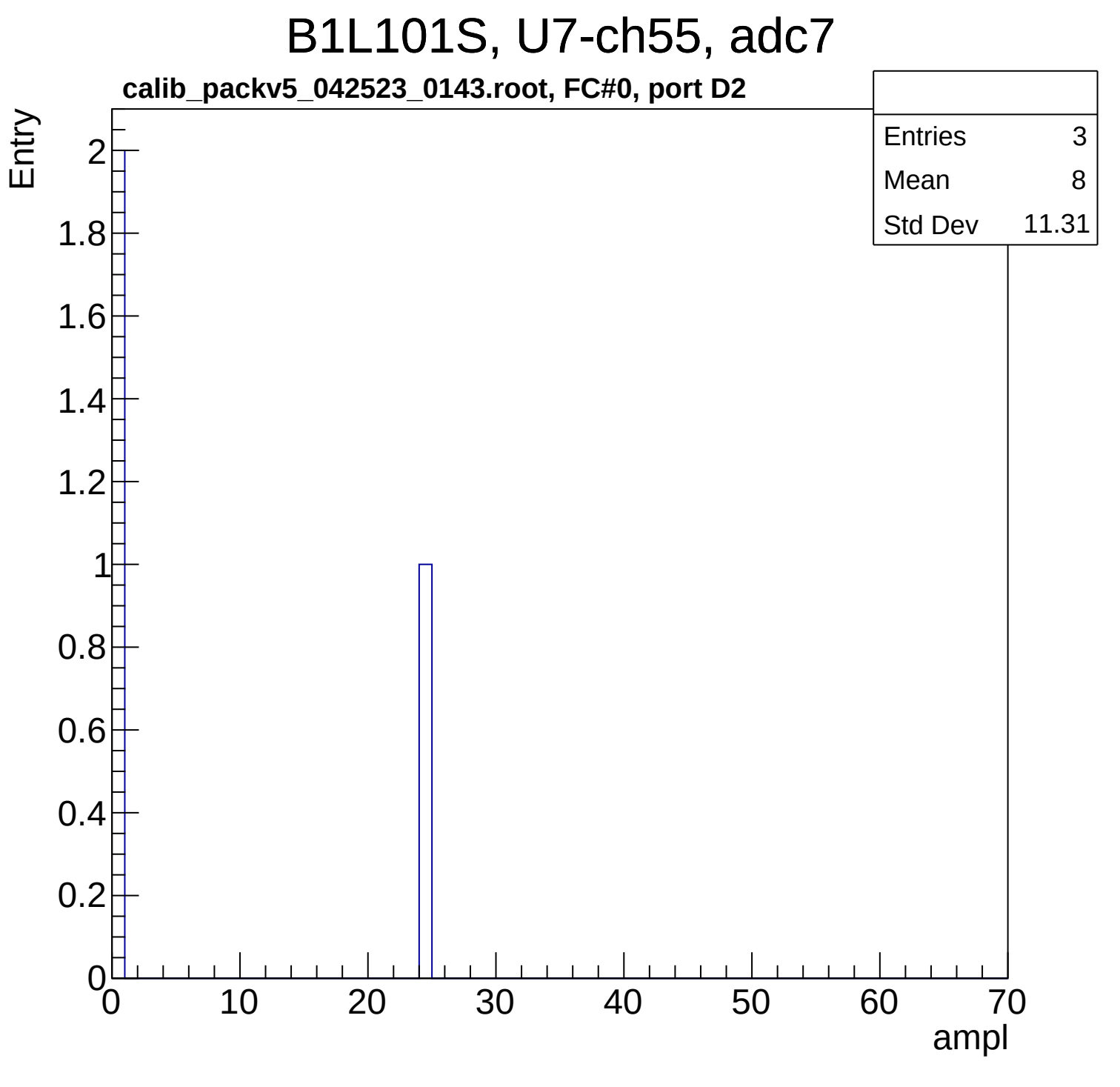

B1L101S, U7-ch55, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 62.38
Std Dev 1.317
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L101S, U7-ch55, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 8
Std Dev 11.31
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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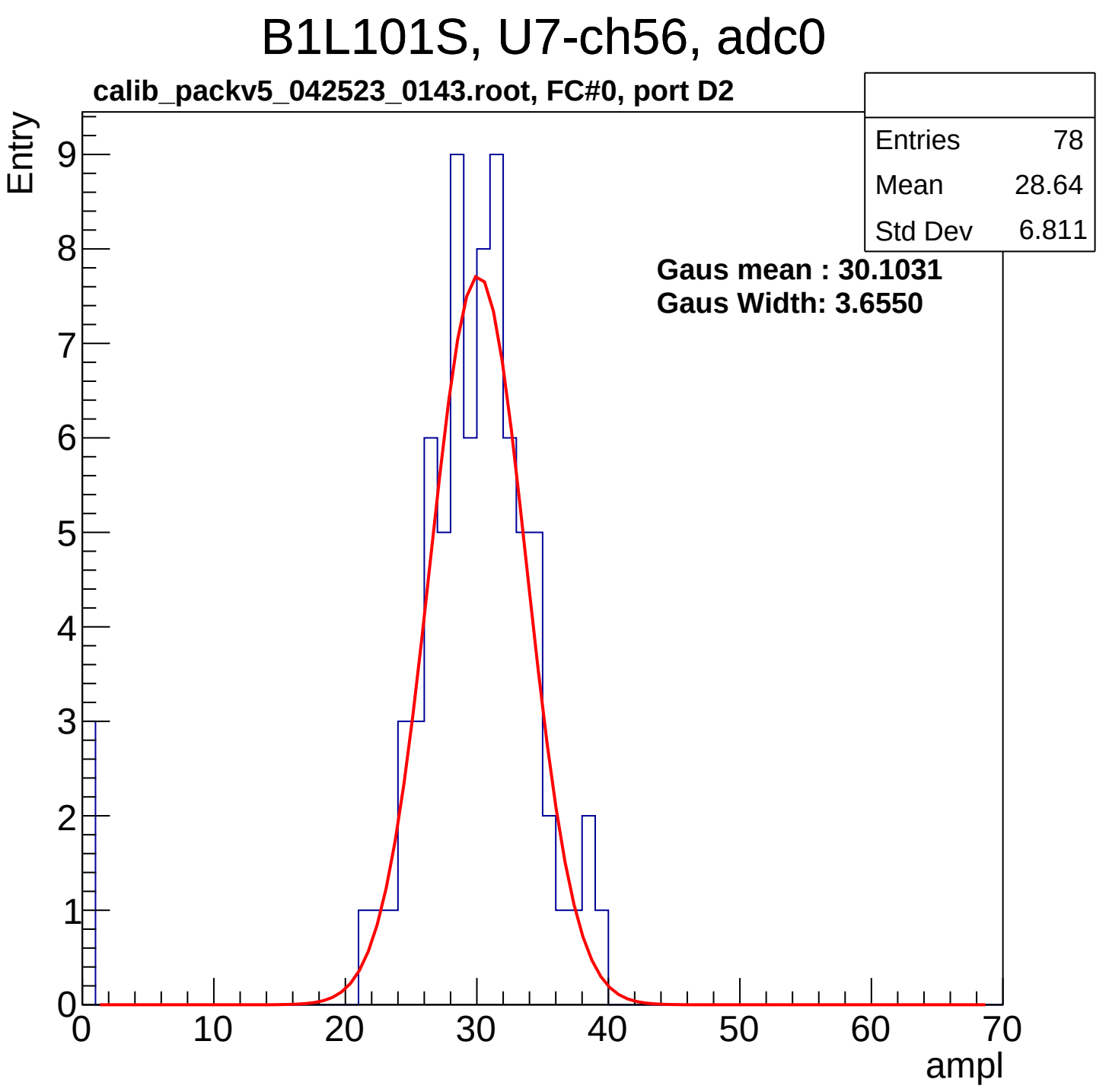
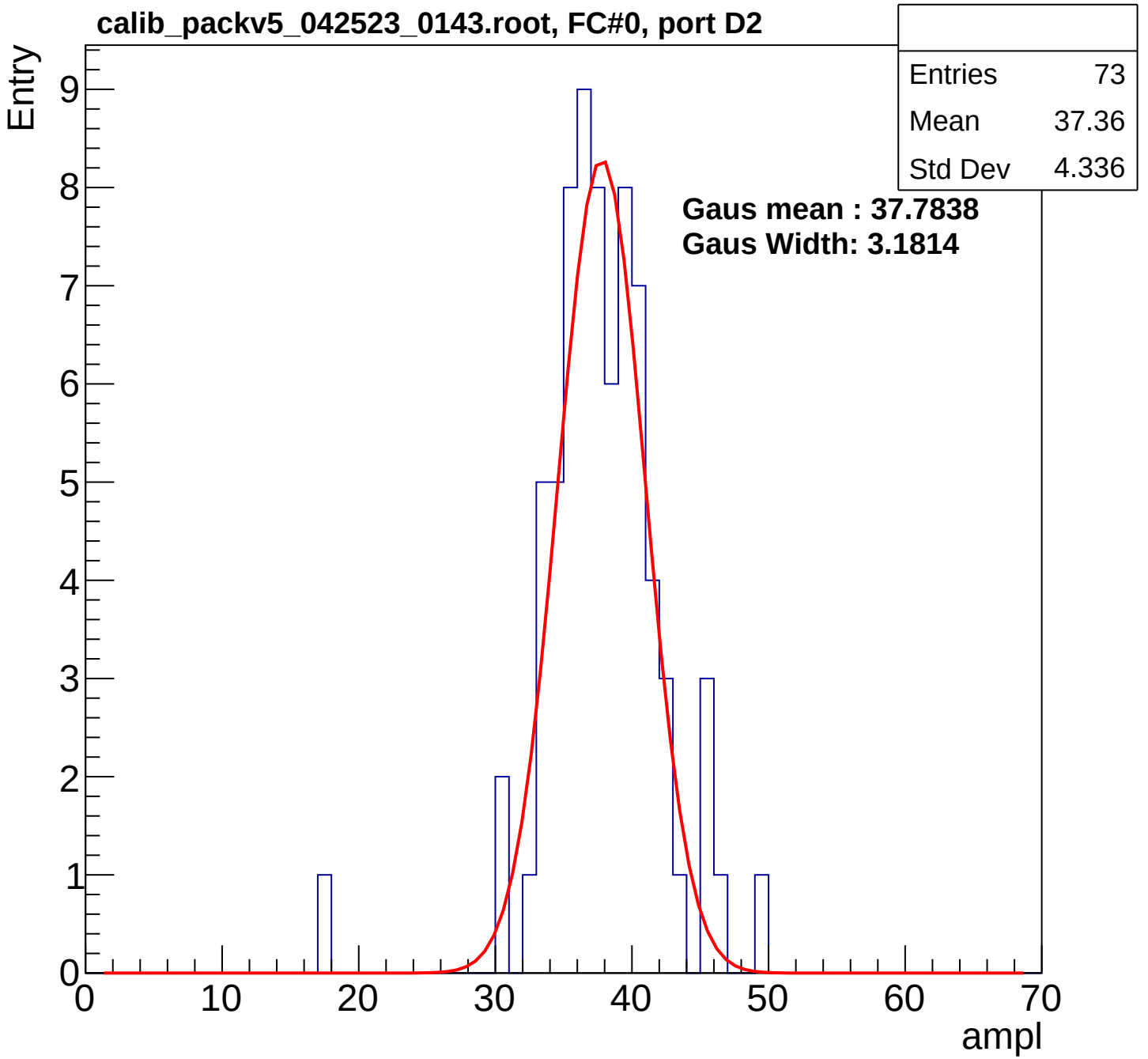
40
50
60
70


B1L101S, U7-ch56, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 28.64
Std Dev 6.811
Gaus mean : 30.1031
Gaus Width: 3.6550
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch56, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 37.36
Std Dev 4.336
Gaus mean : 37.7838
Gaus Width: 3.1814
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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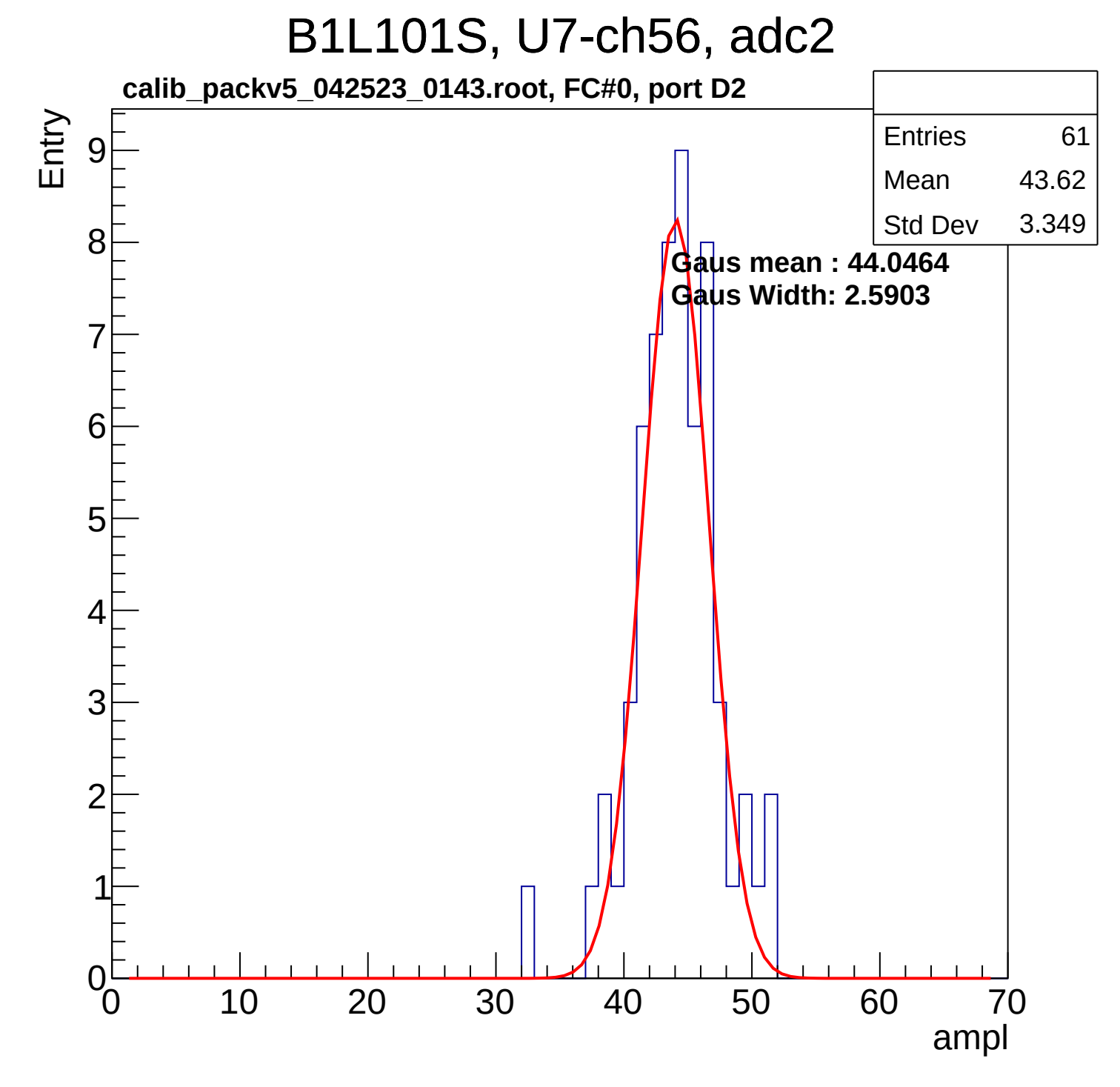
B1L101S, U7-ch56, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 43.62
Std Dev 3.349
Gaus mean : 44.0464
Gaus Width: 2.5903
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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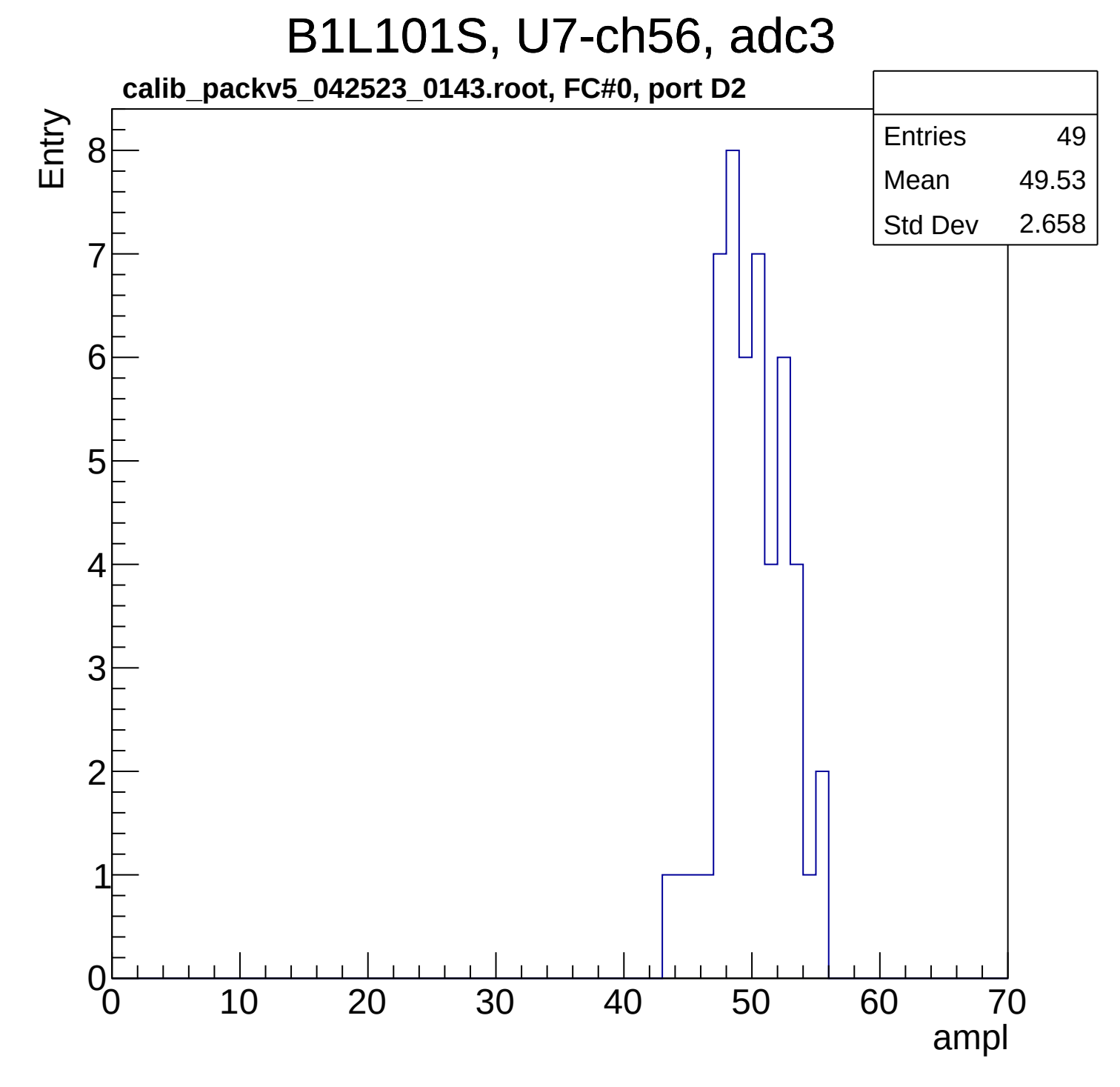
B1L101S, U7-ch56, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 49.53
Std Dev 2.658
Entry
ampl
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0
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60
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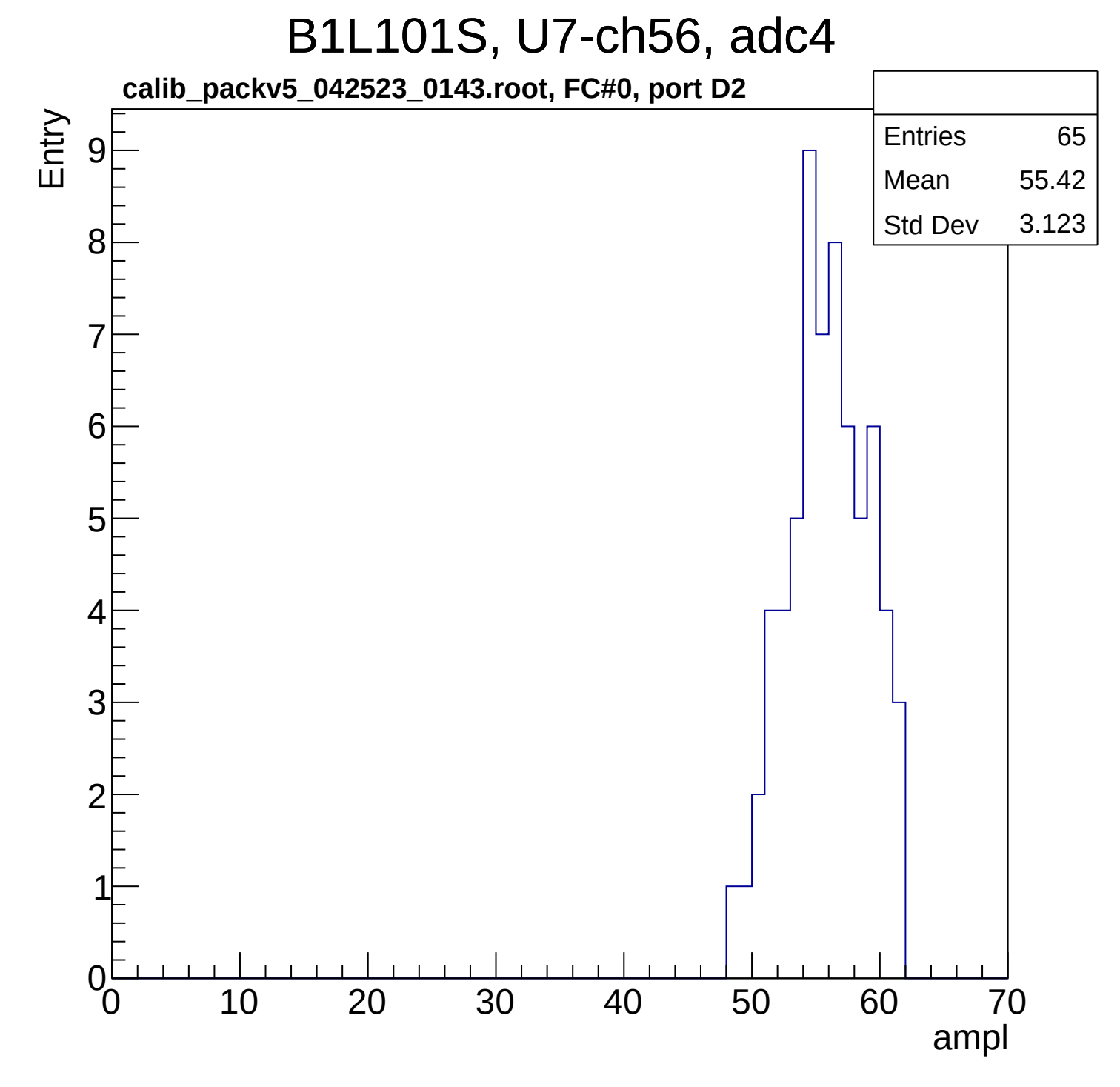
B1L101S, U7-ch56, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 55.42
Std Dev 3.123
Entry
ampl
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2
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4
5
6
7
8
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0
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40
50
60
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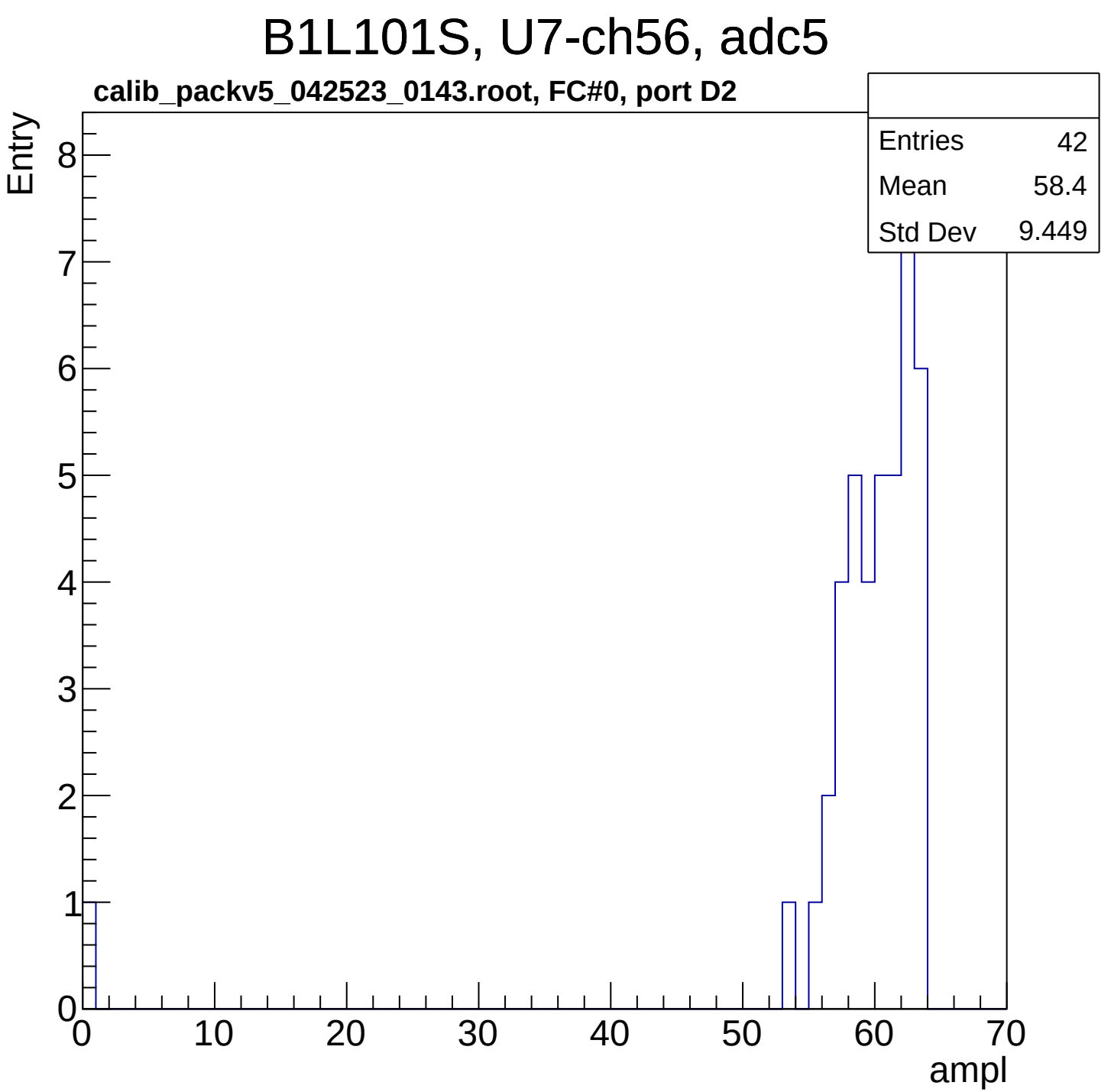
B1L101S, U7-ch56, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 58.4
Std Dev 9.449
Entry
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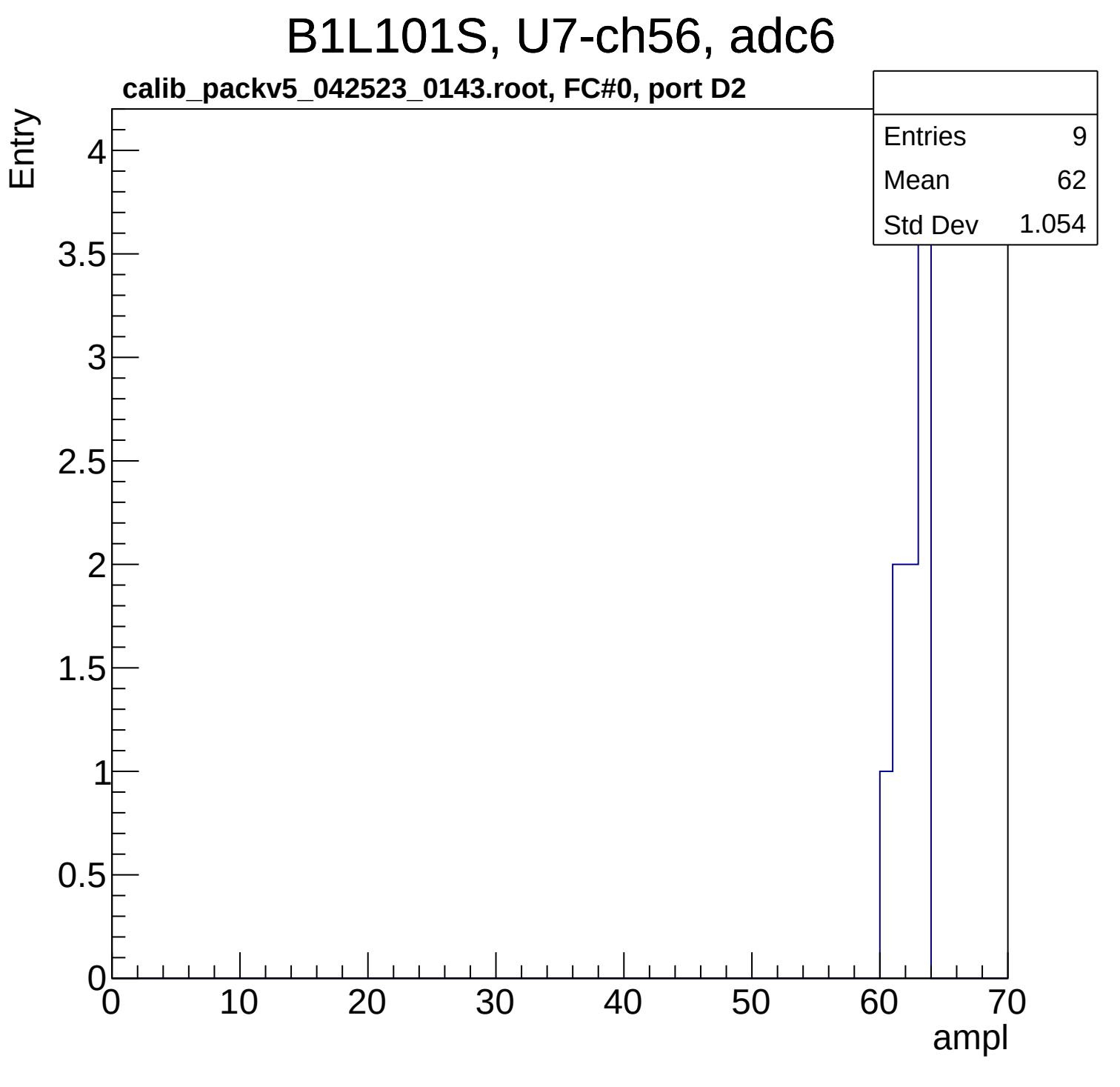
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch56, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 62
Std Dev 1.054
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
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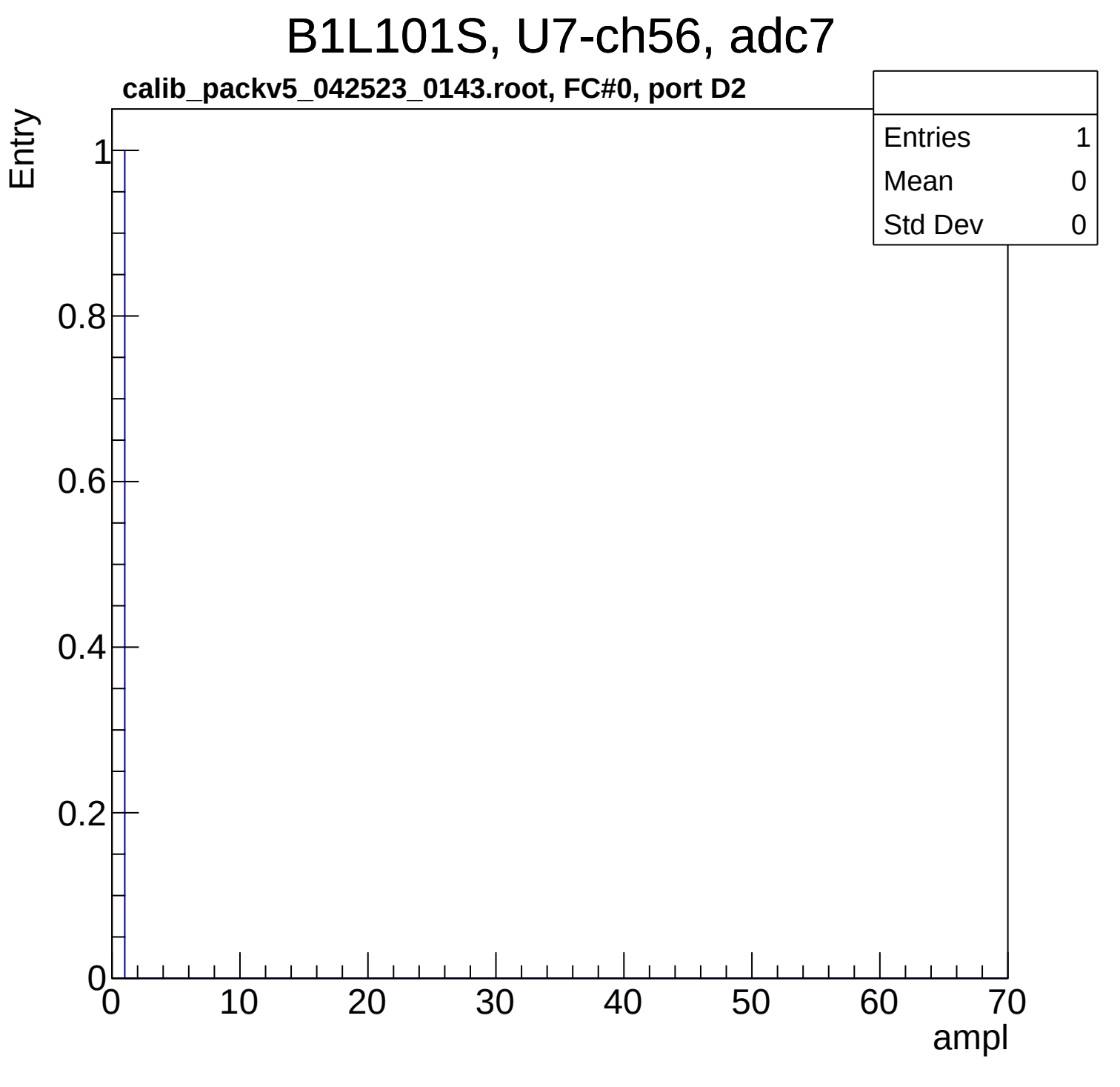
20
30
40
50
60
70


B1L101S, U7-ch56, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
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0.6
0.4
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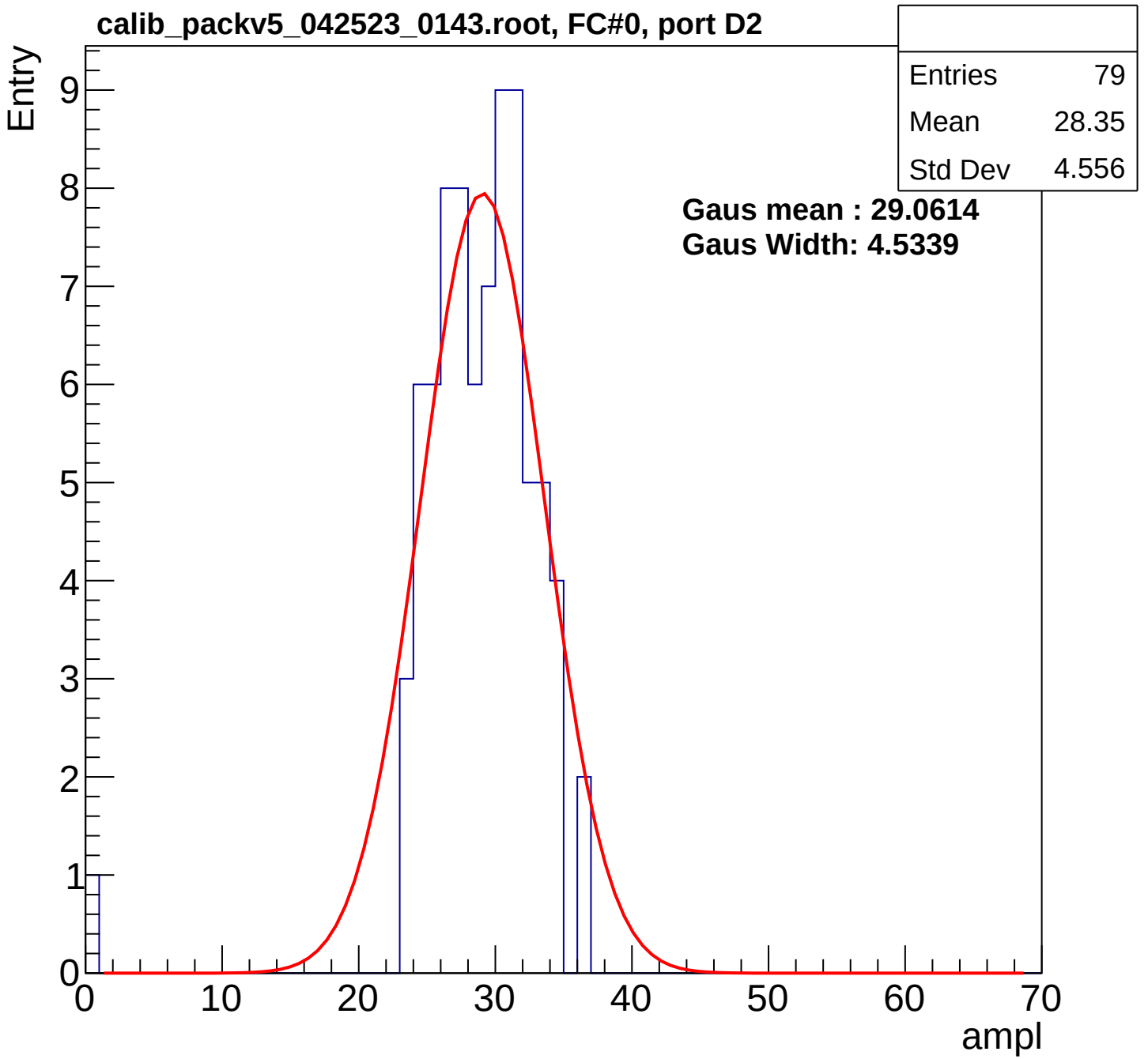
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch57, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 28.35
Std Dev 4.556
Gaus mean : 29.0614
Gaus Width: 4.5339
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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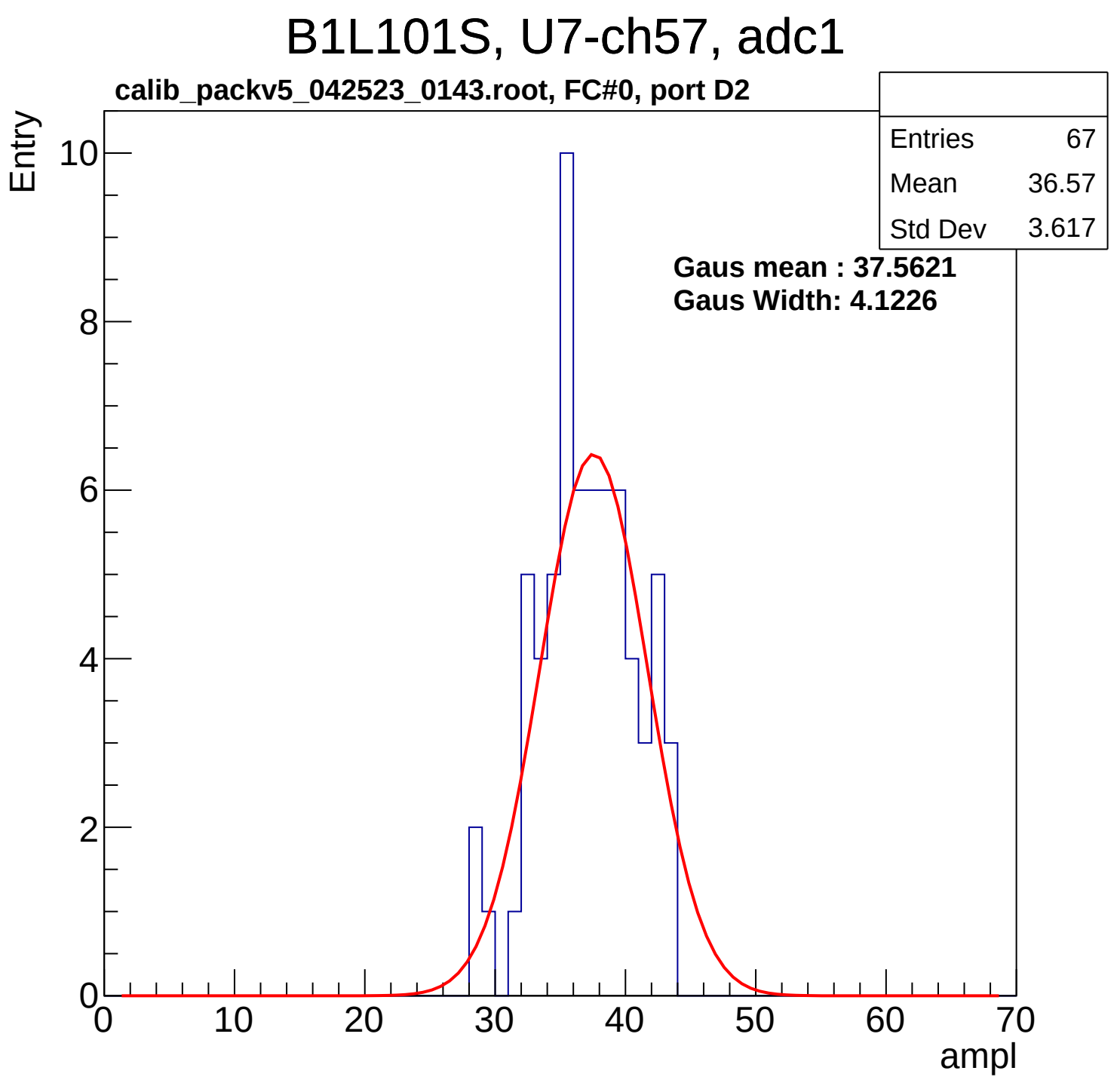
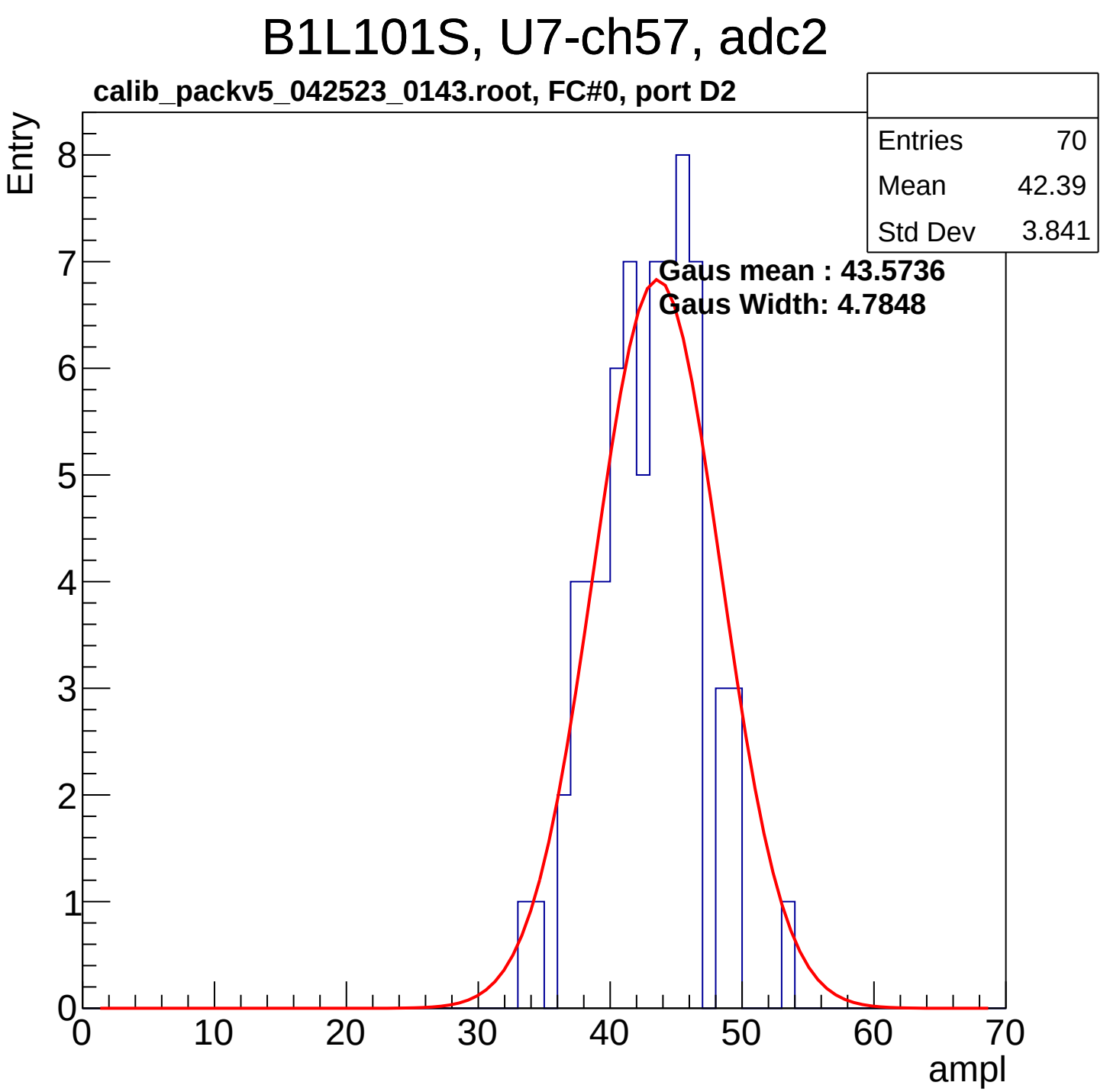
40
50
60
70


B1L101S, U7-ch57, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 36.57
Std Dev 3.617
Gaus mean : 37.5621
Gaus Width: 4.1226
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch57, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 42.39
Std Dev 3.841
Gaus mean : 43.5736
Gaus Width: 4.7848
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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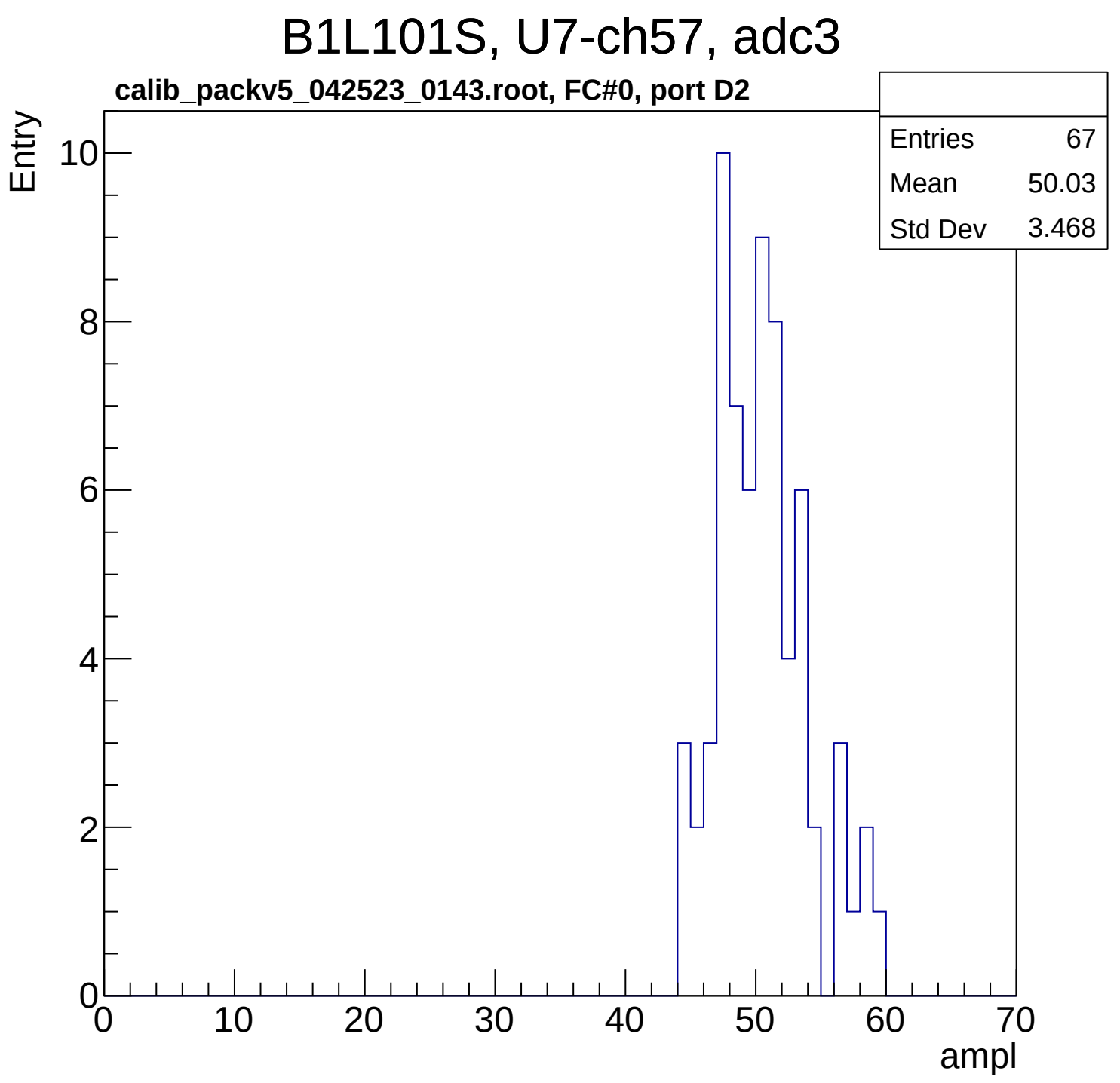
B1L101S, U7-ch57, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 50.03
Std Dev 3.468
Entry
ampl
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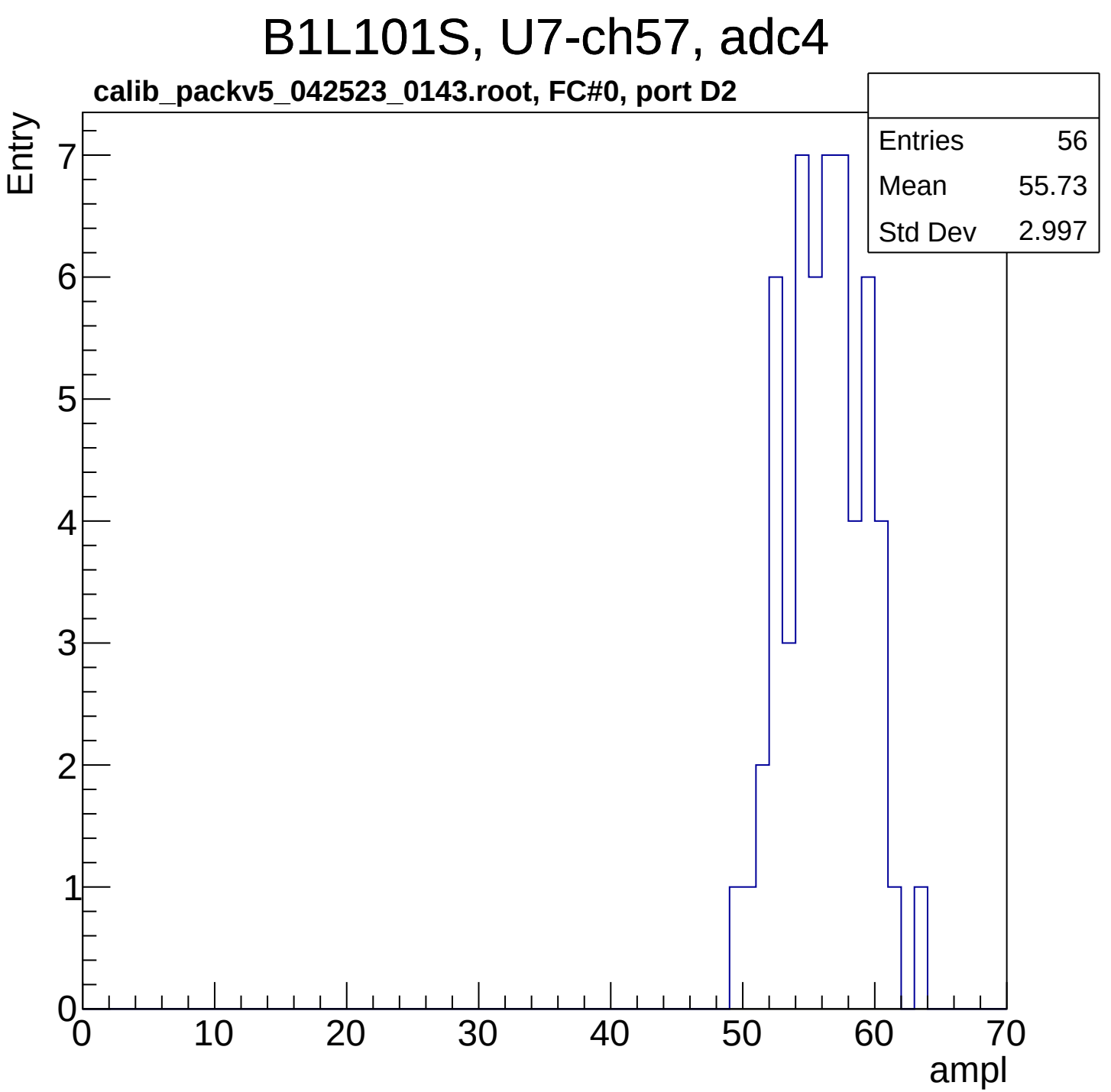
B1L101S, U7-ch57, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 55.73
Std Dev 2.997
Entry
ampl
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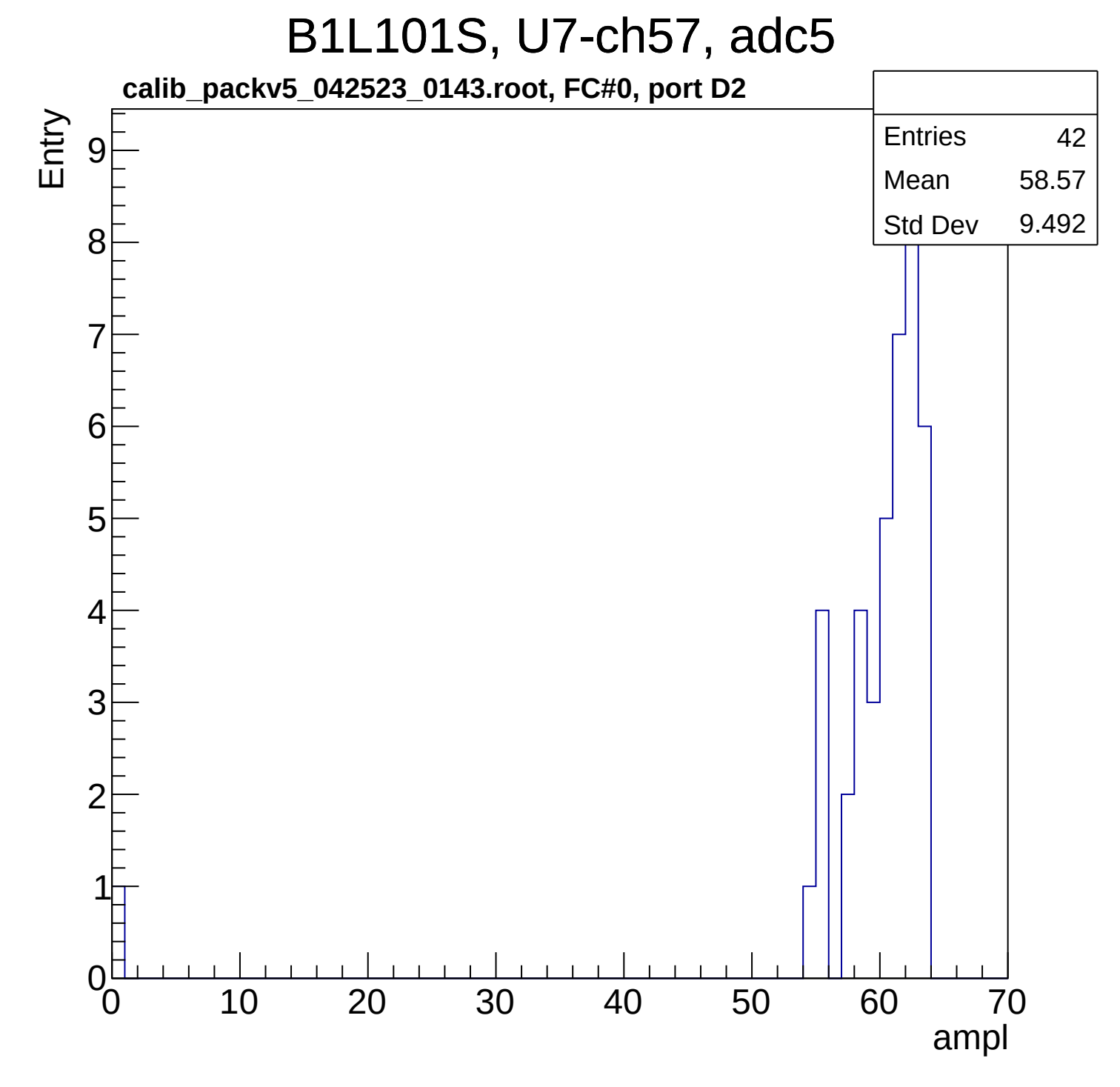
B1L101S, U7-ch57, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 58.57
Std Dev 9.492
Entry
ampl
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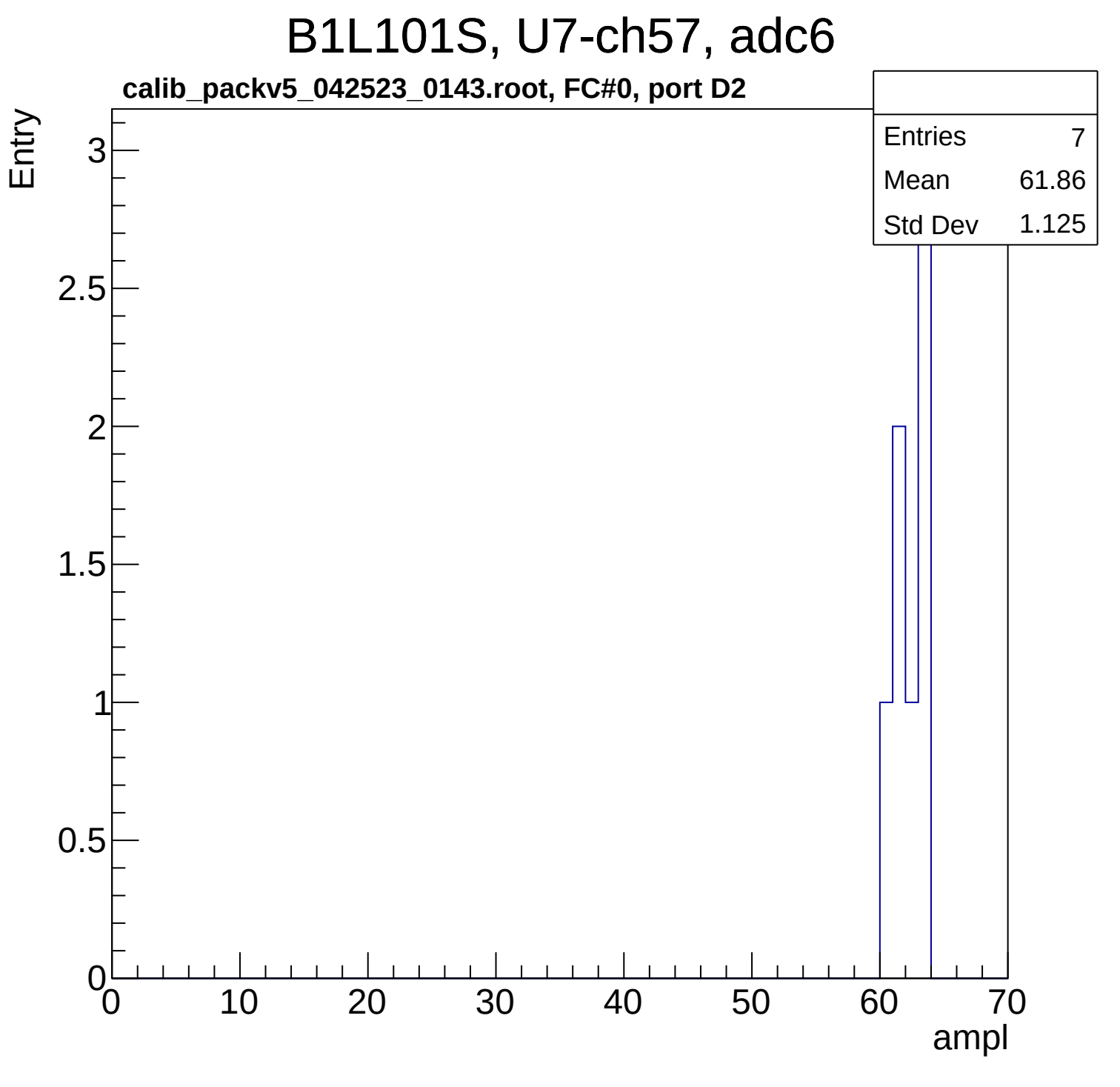
B1L101S, U7-ch57, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 61.86
Std Dev 1.125
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
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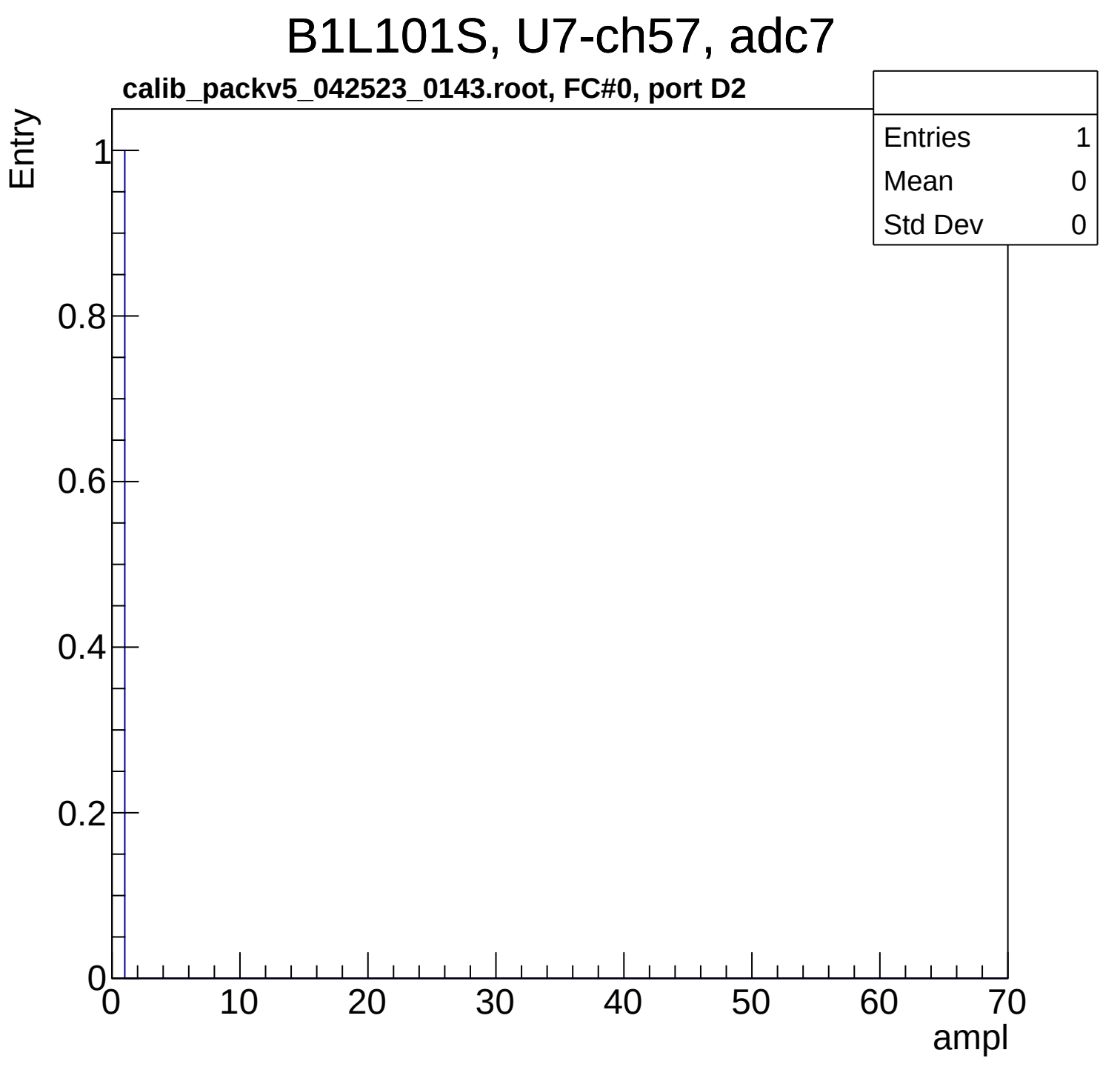
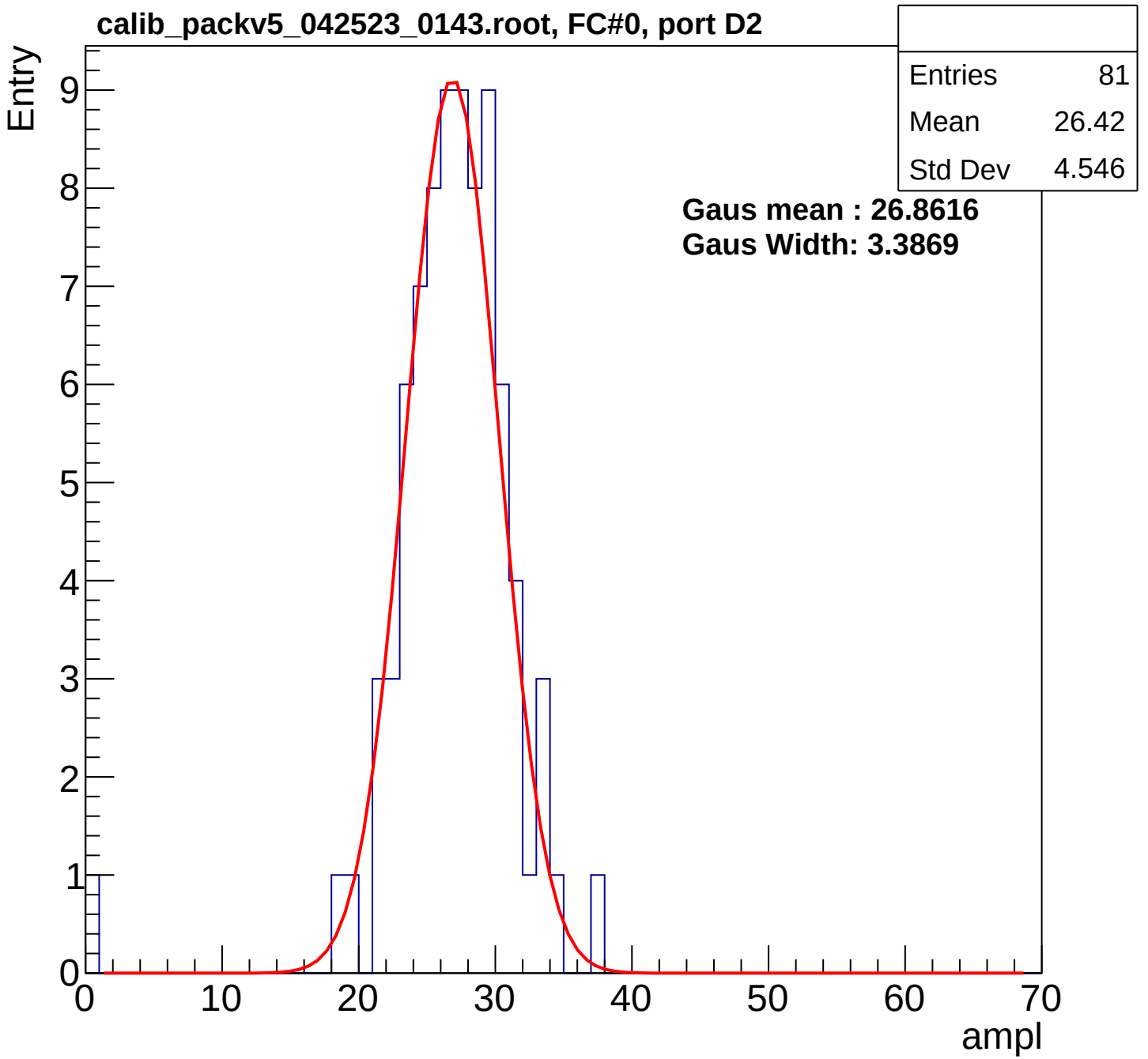
40
50
60
70


B1L101S, U7-ch57, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch58, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 81
Mean 26.42
Std Dev 4.546
Gaus mean : 26.8616
Gaus Width: 3.3869
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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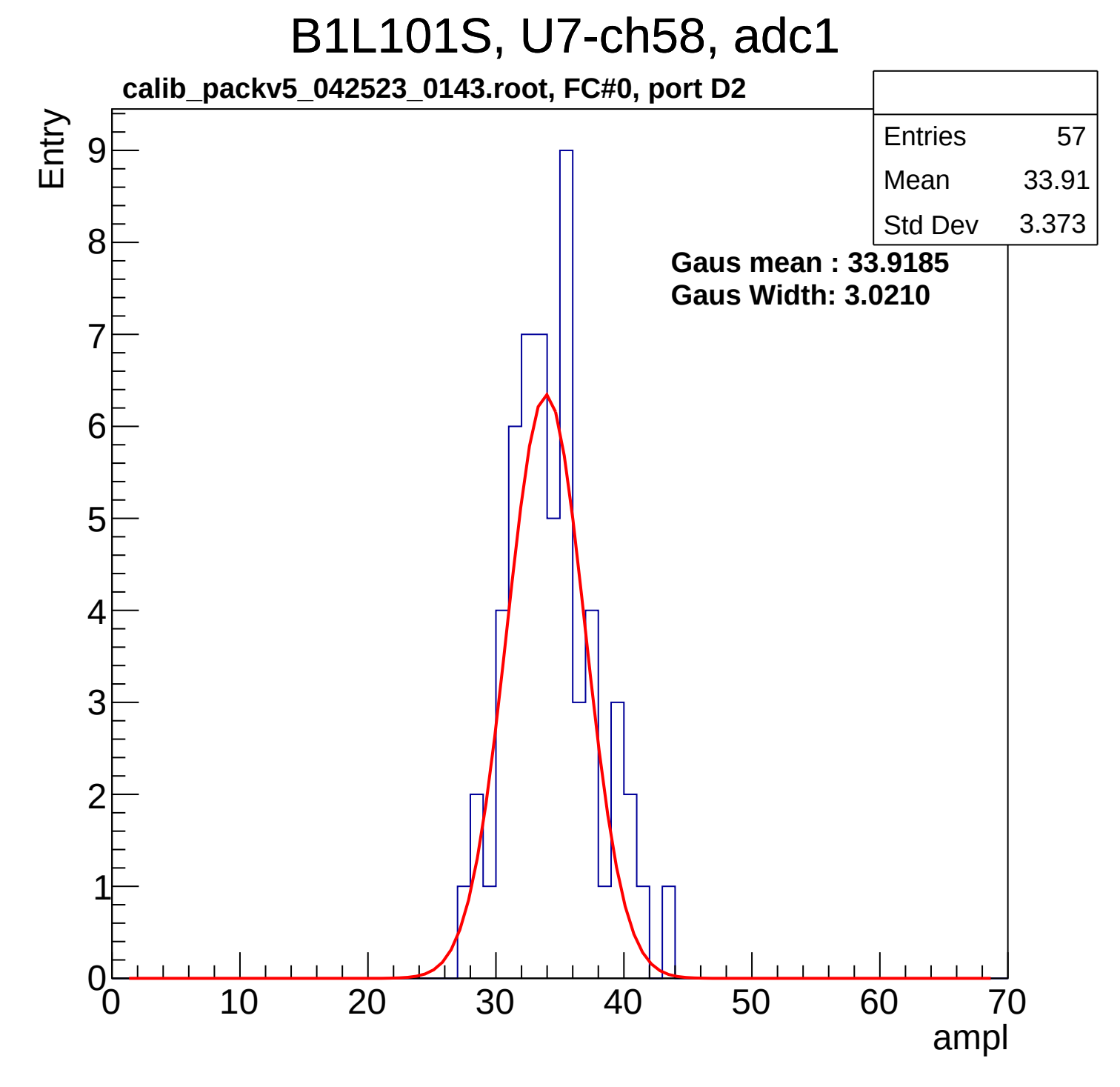
B1L101S, U7-ch58, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 33.91
Std Dev 3.373
Gaus mean : 33.9185
Gaus Width: 3.0210
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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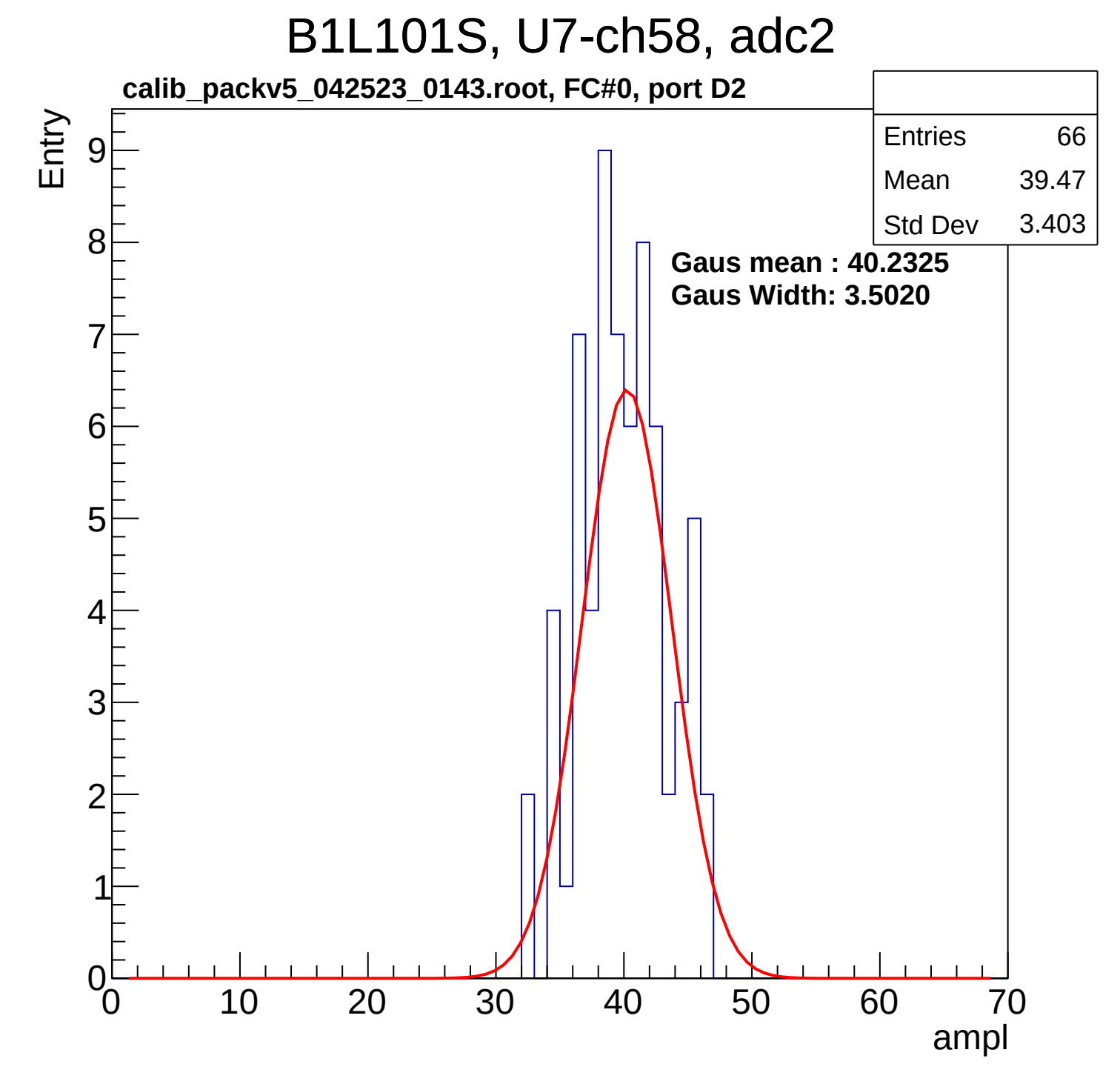
B1L101S, U7-ch58, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 39.47
Std Dev 3.403
Gaus mean : 40.2325
Gaus Width: 3.5020
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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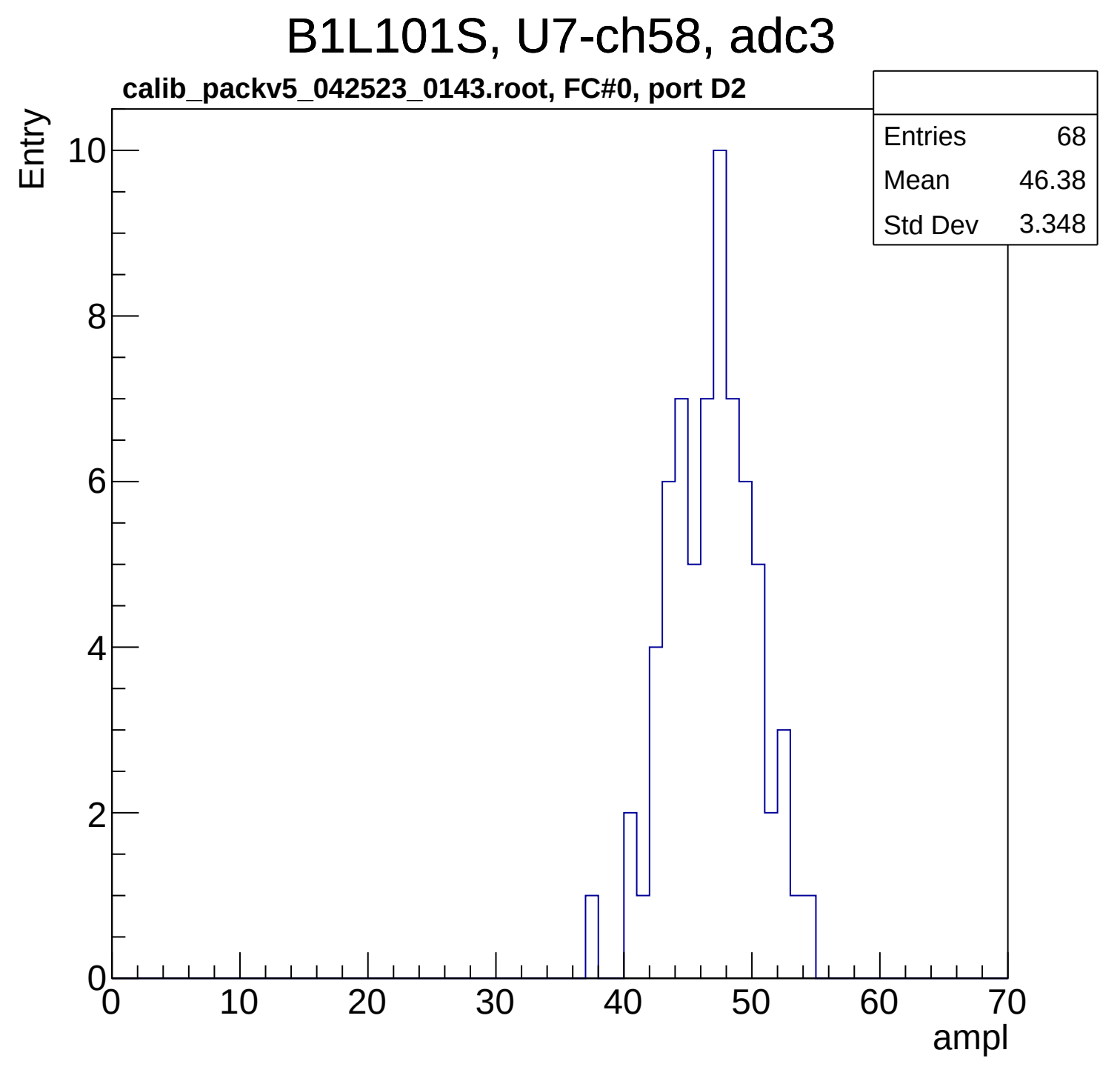
B1L101S, U7-ch58, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 46.38
Std Dev 3.348
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
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60
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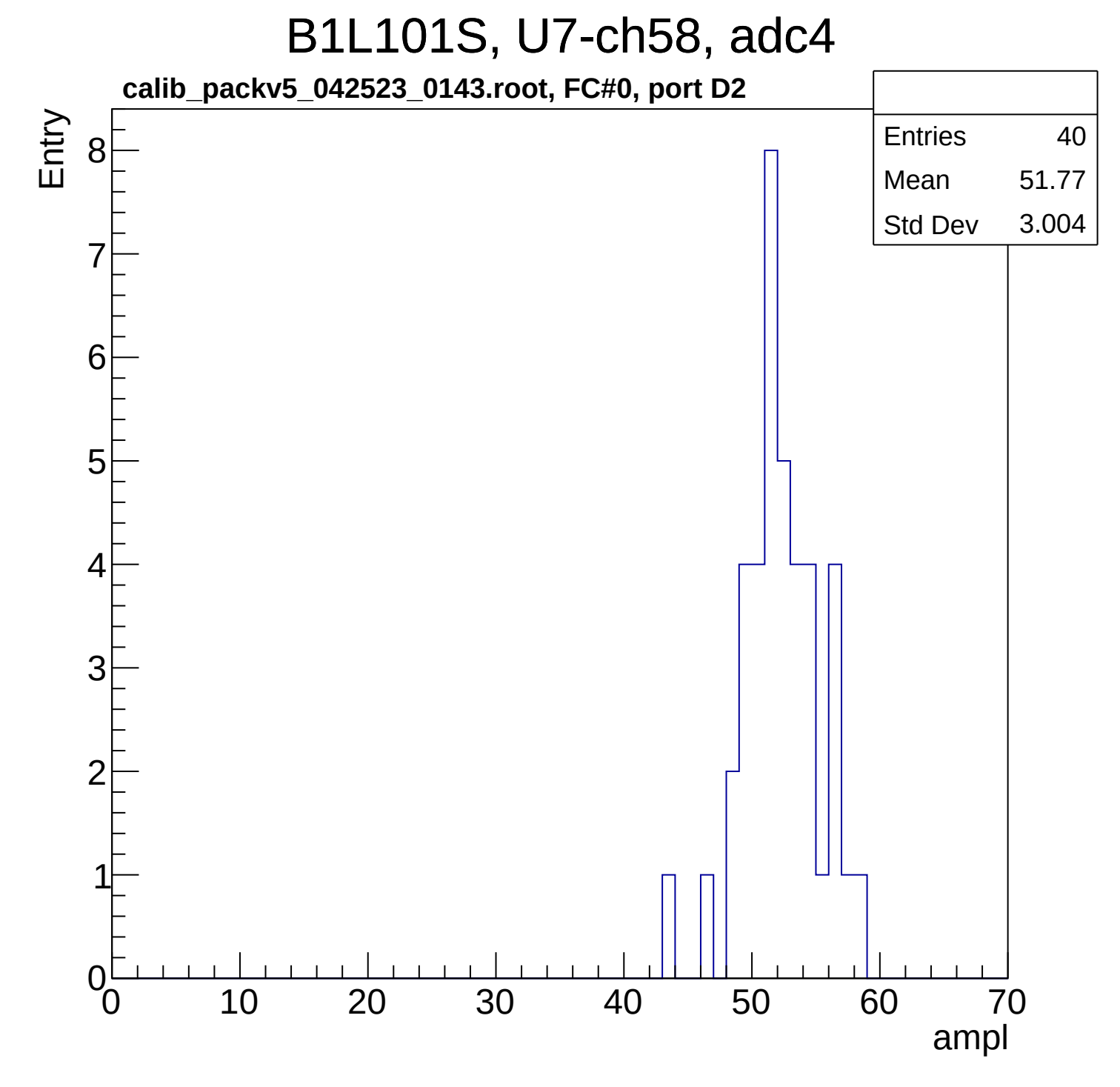
B1L101S, U7-ch58, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 40
Mean 51.77
Std Dev 3.004
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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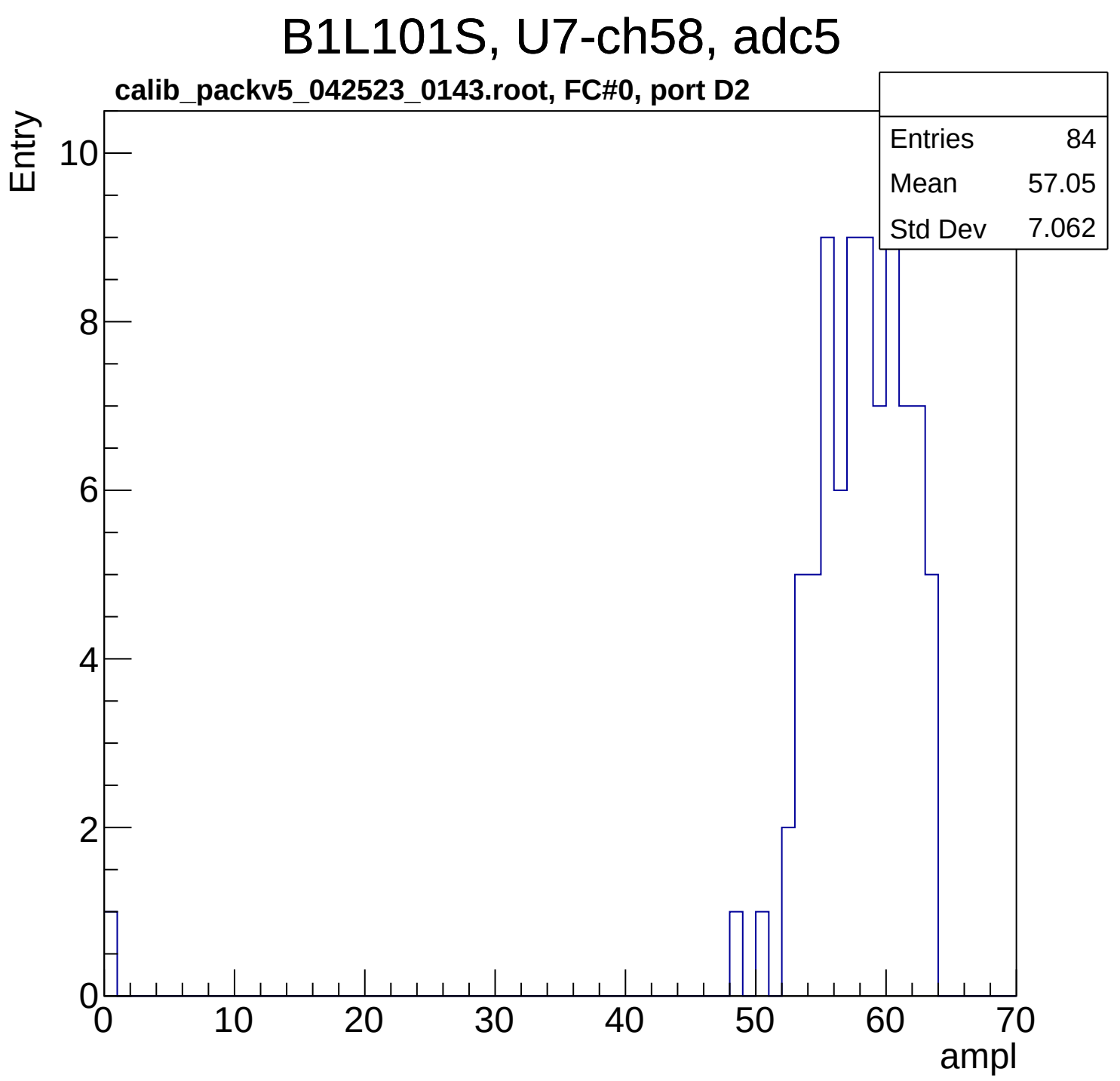
B1L101S, U7-ch58, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 84
Mean 57.05
Std Dev 7.062
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
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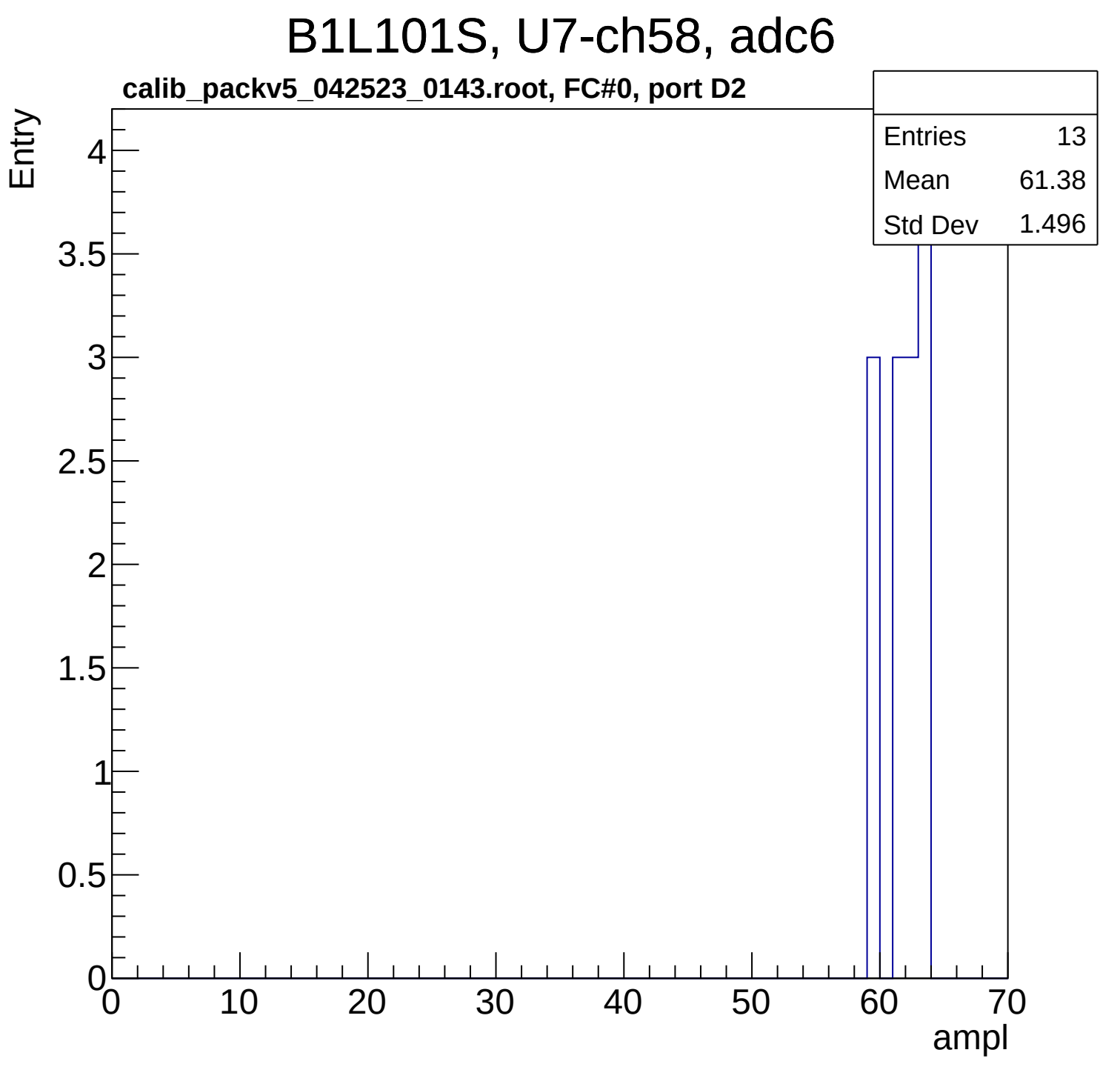
60
70


B1L101S, U7-ch58, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 13
Mean 61.38
Std Dev 1.496
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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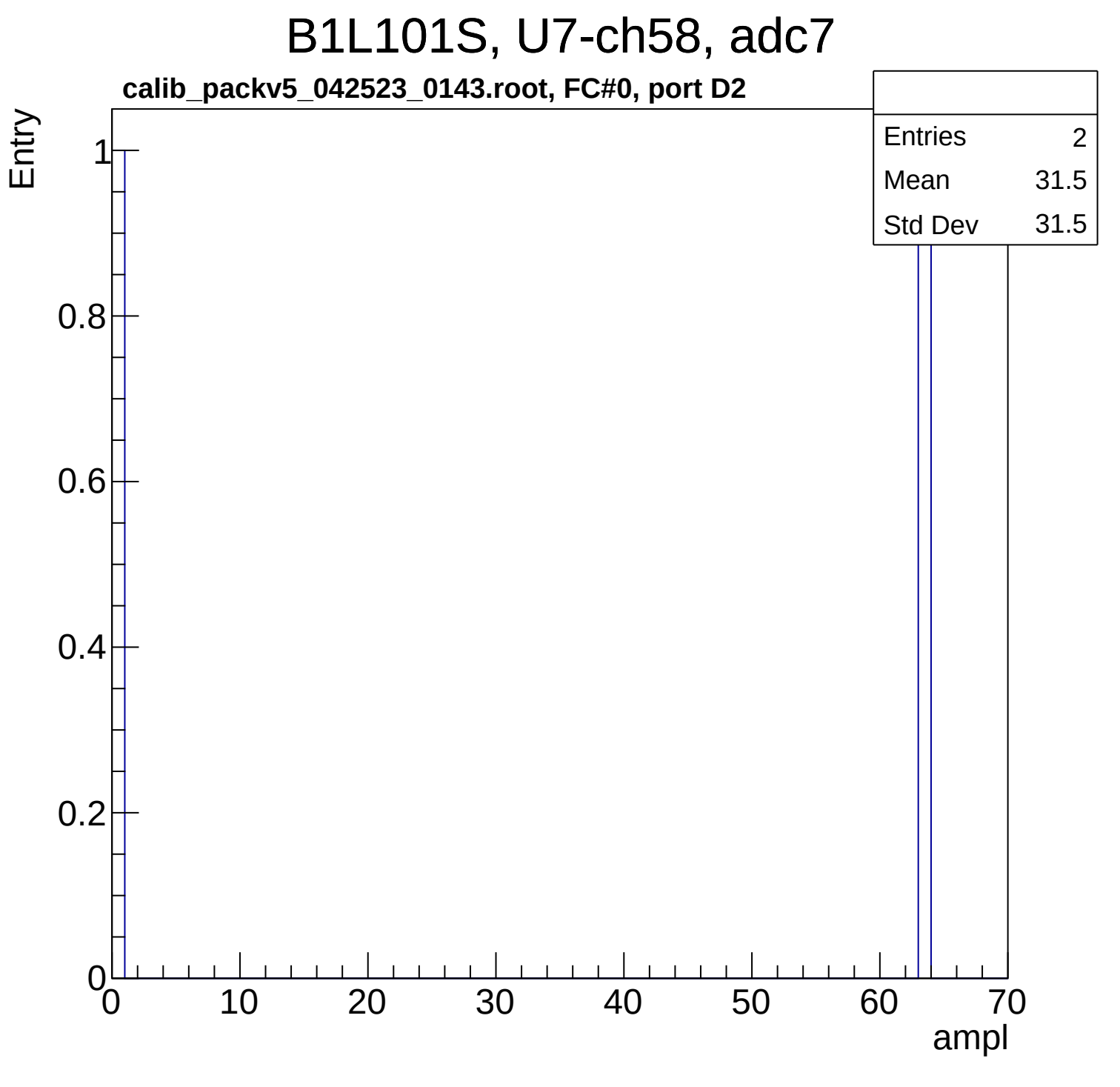
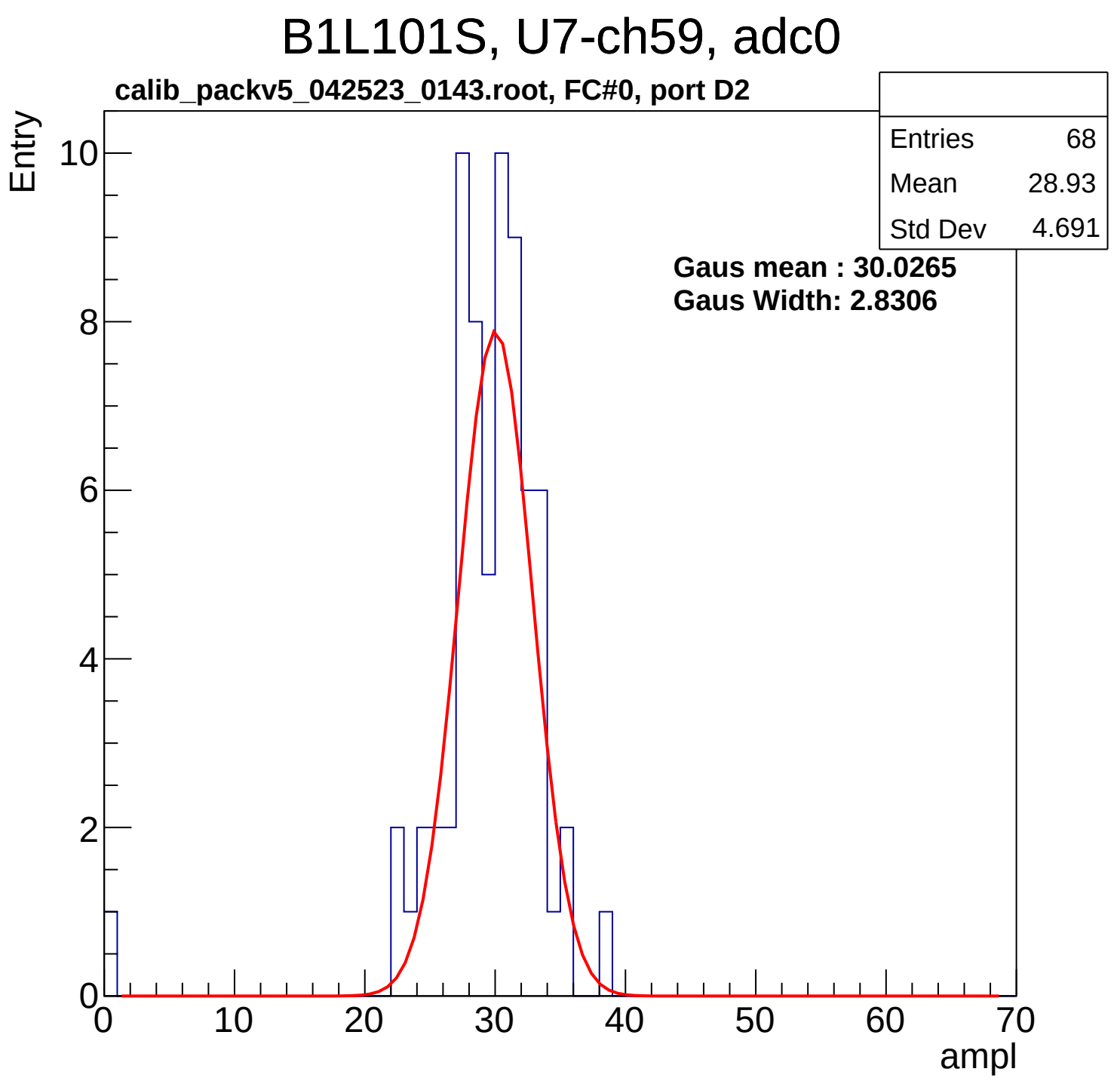
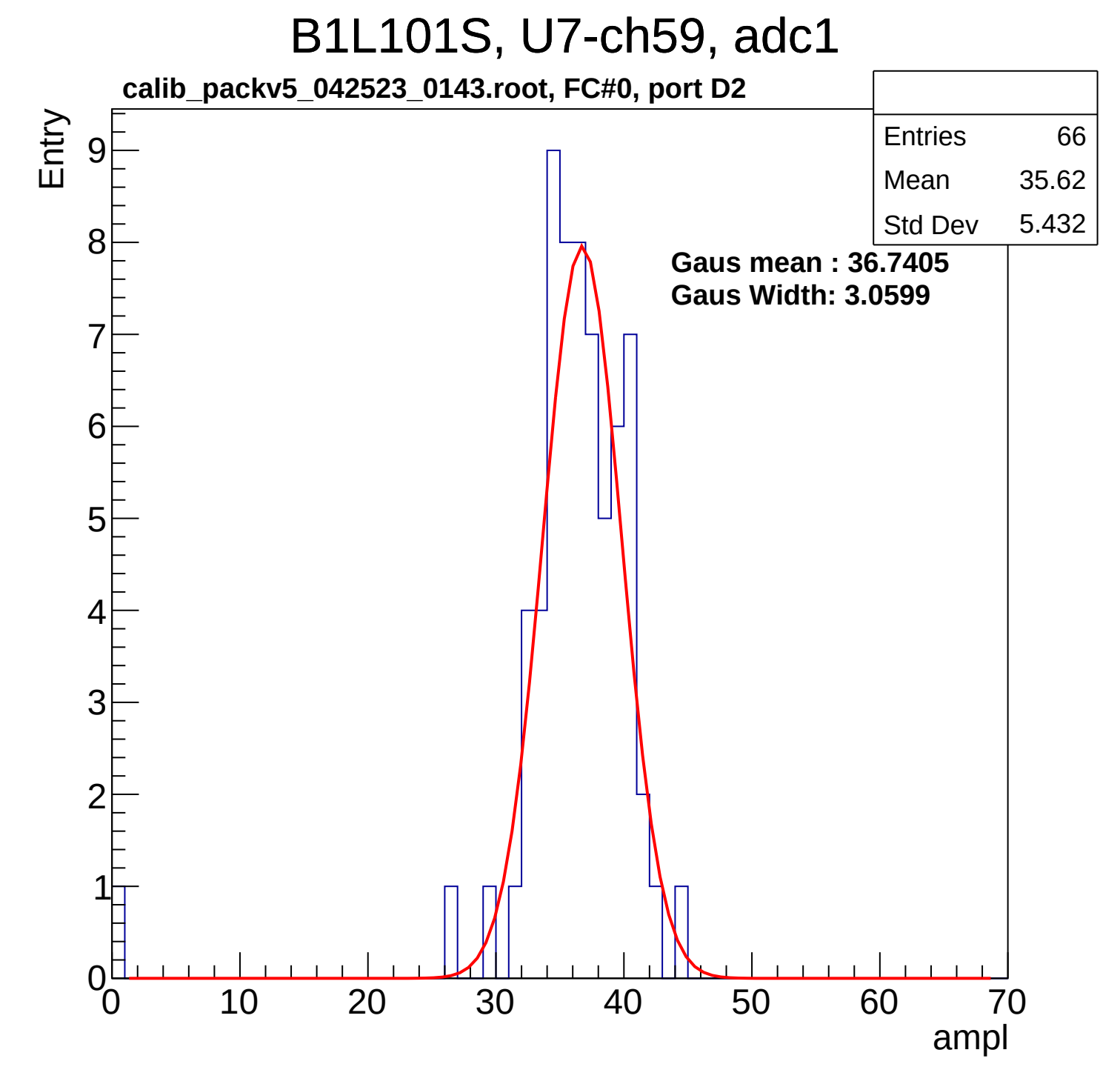

B1L101S, U7-ch58, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch59, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 28.93
Std Dev 4.691
Gaus mean : 30.0265
Gaus Width: 2.8306
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch59, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 35.62
Std Dev 5.432
Gaus mean : 36.7405
Gaus Width: 3.0599
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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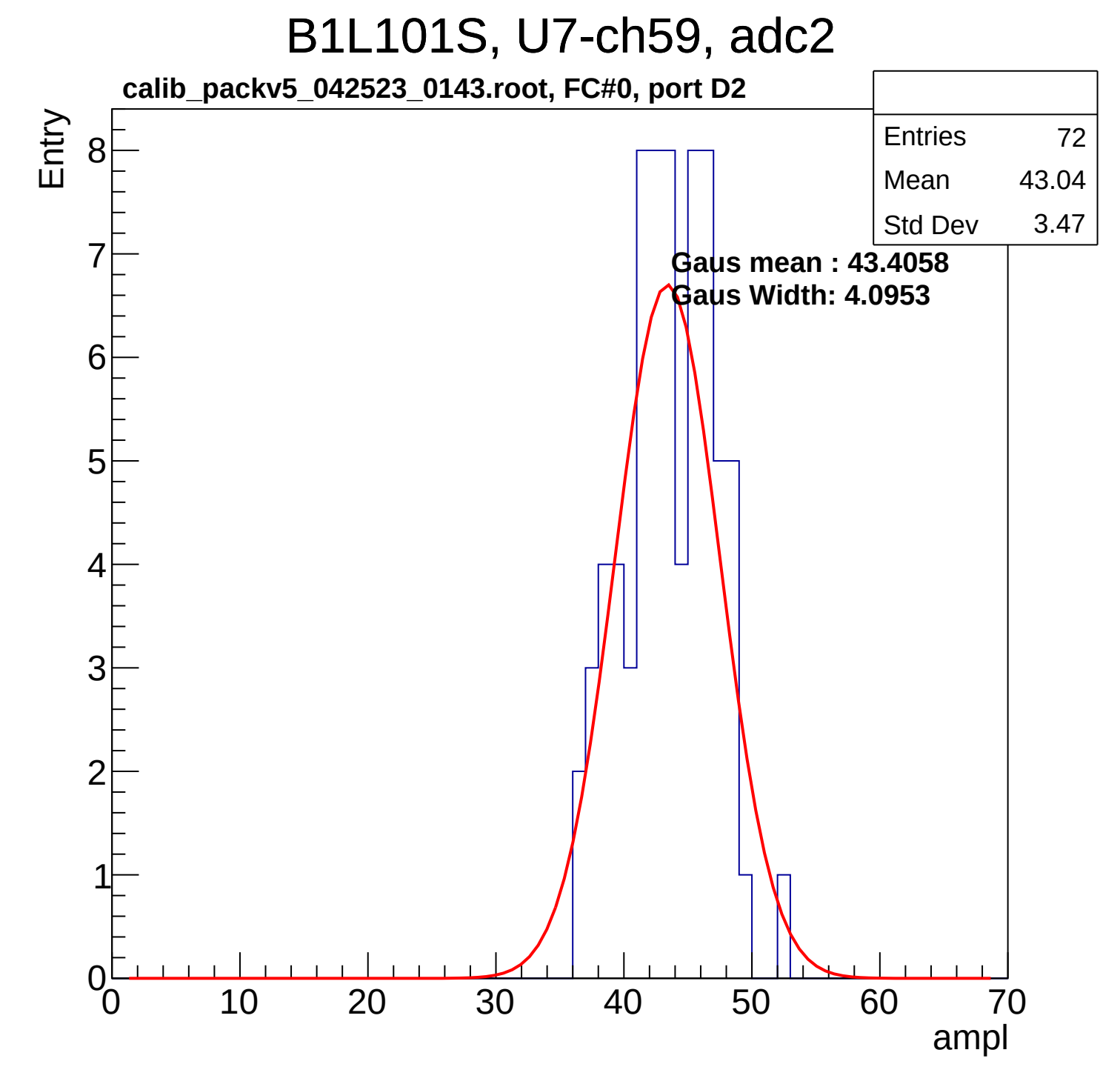
B1L101S, U7-ch59, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 43.04
Std Dev 3.47
Gaus mean : 43.4058
Gaus Width: 4.0953
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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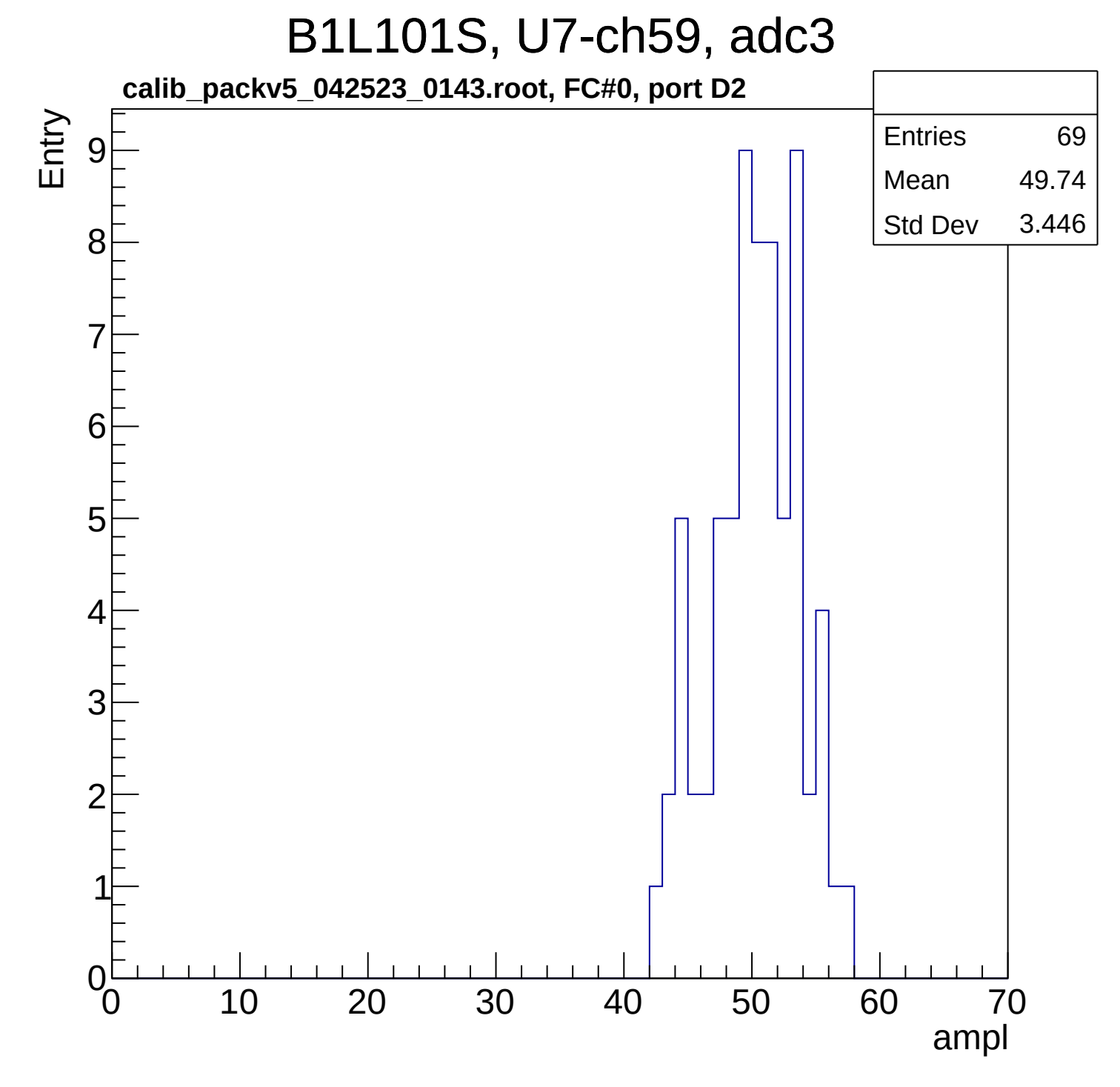
B1L101S, U7-ch59, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 49.74
Std Dev 3.446
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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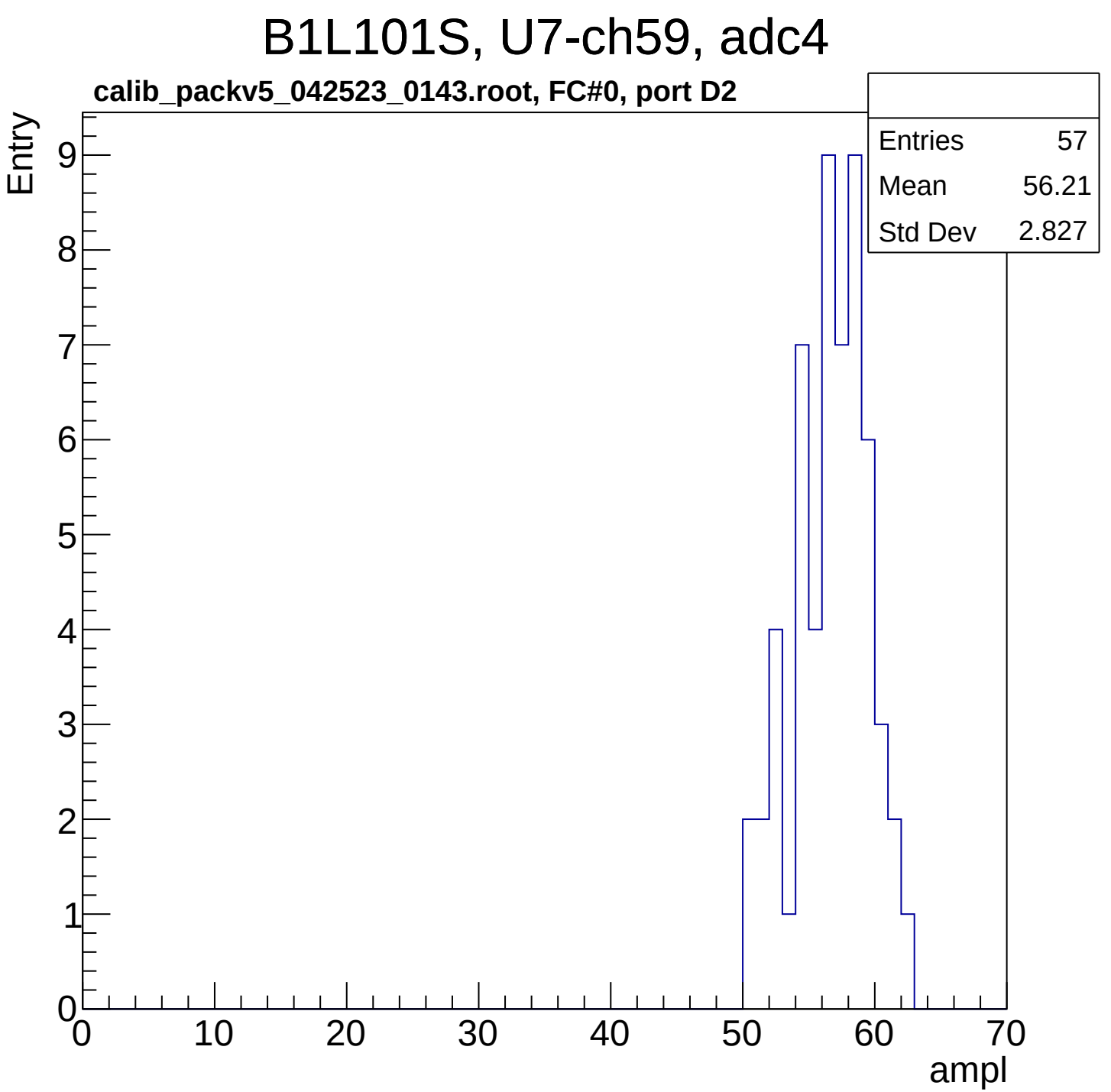
B1L101S, U7-ch59, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 56.21
Std Dev 2.827
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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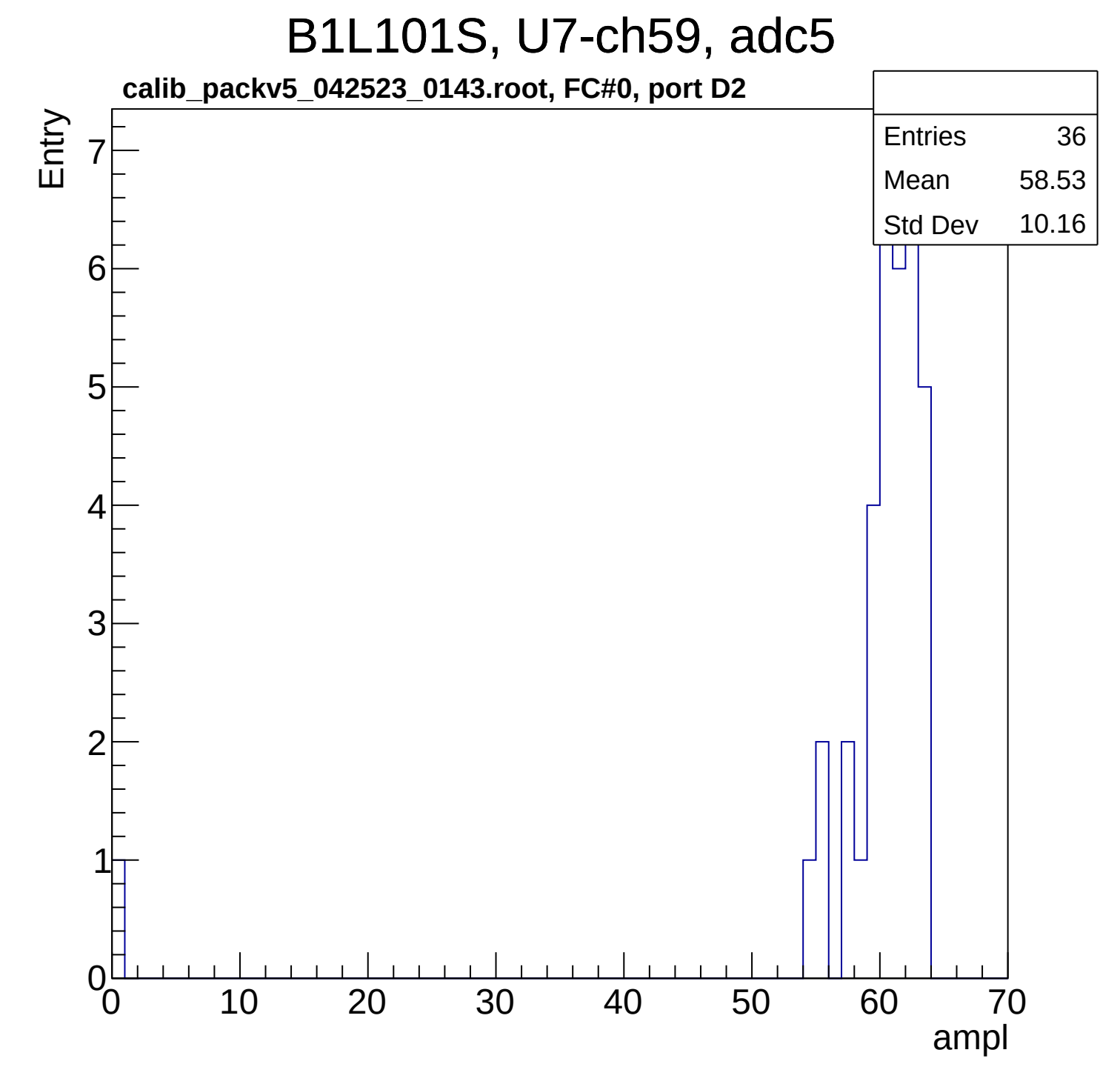
60
70


B1L101S, U7-ch59, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 36
Mean 58.53
Std Dev 10.16
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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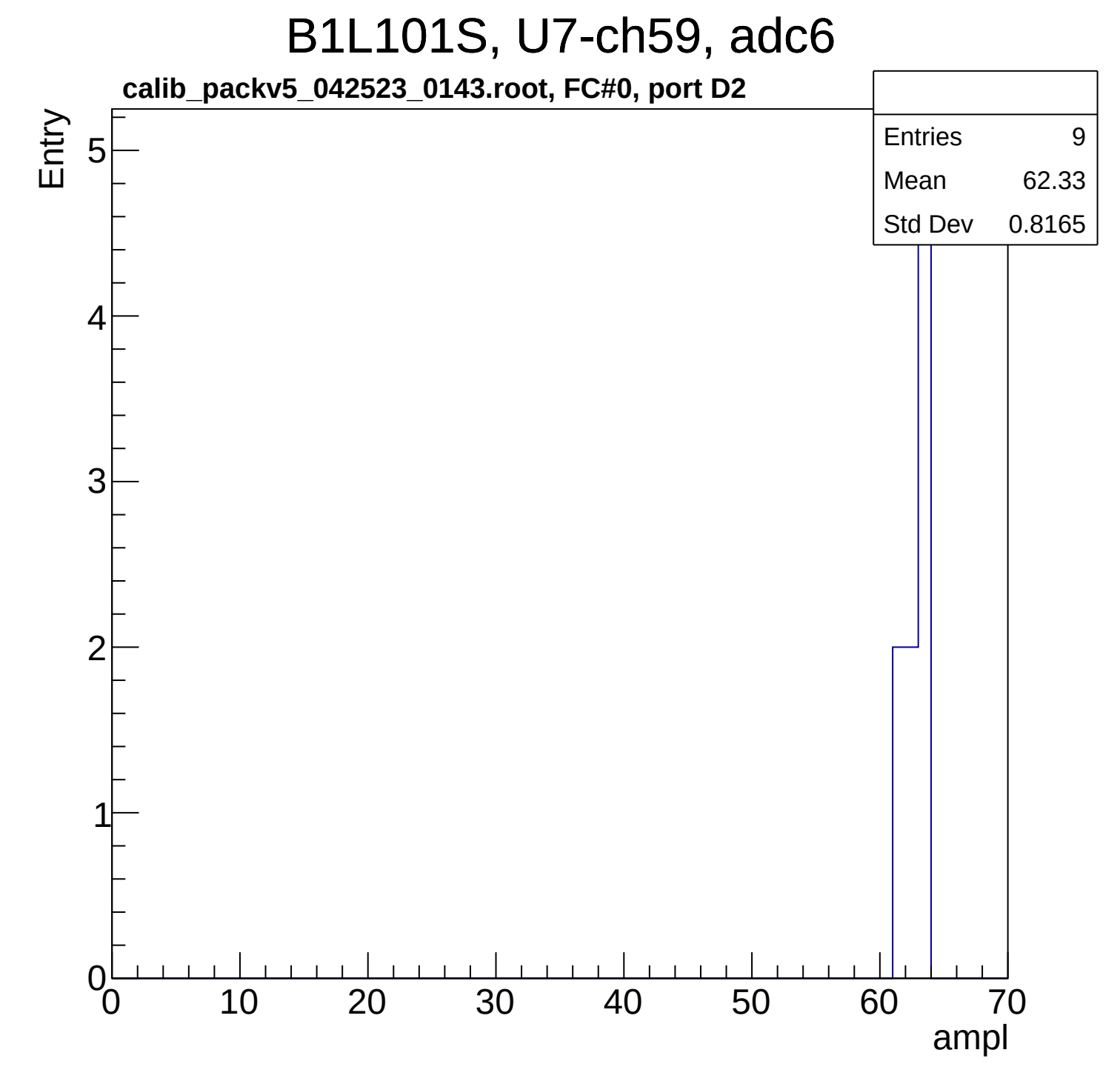
B1L101S, U7-ch59, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 62.33
Std Dev 0.8165
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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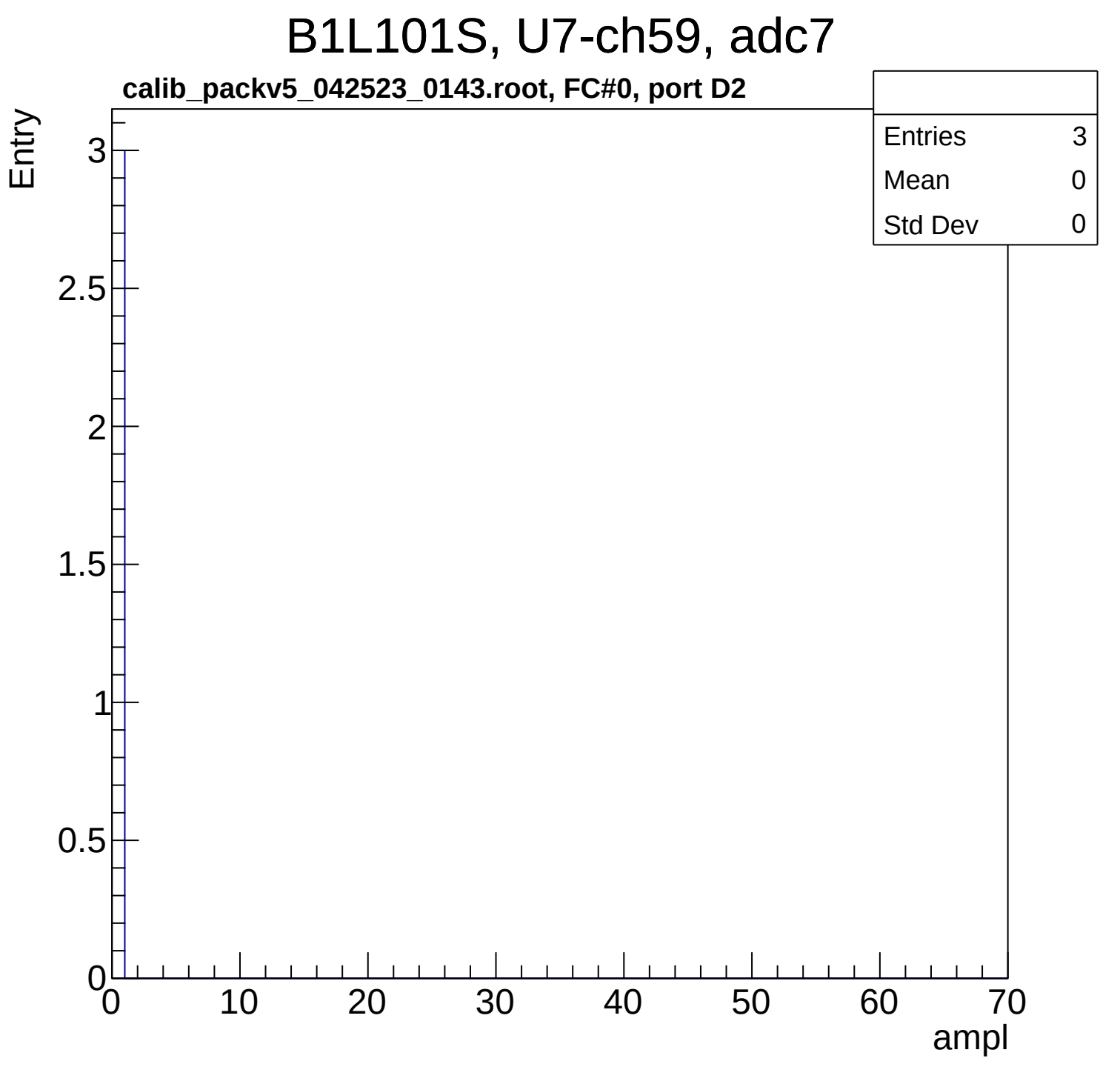
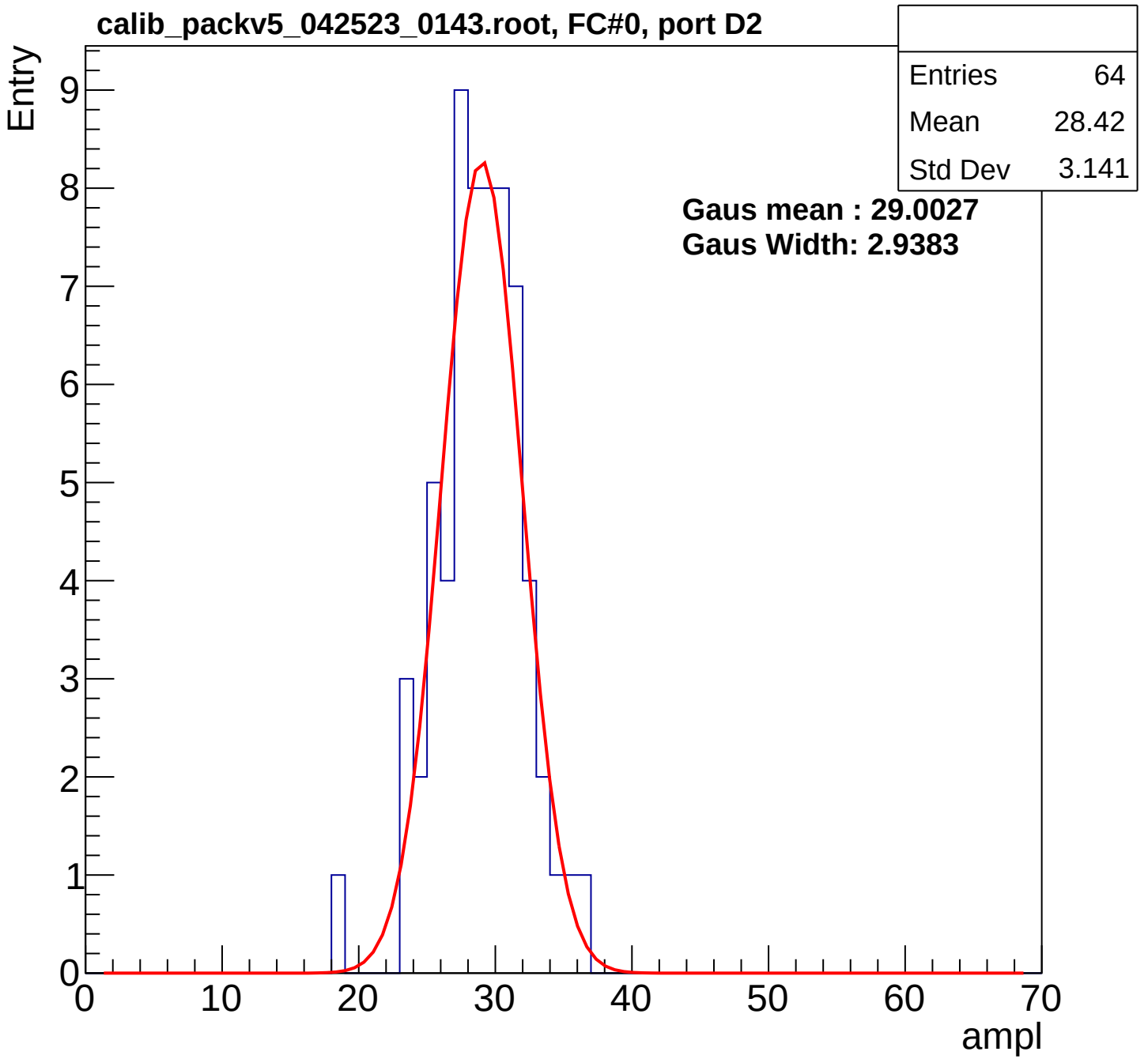
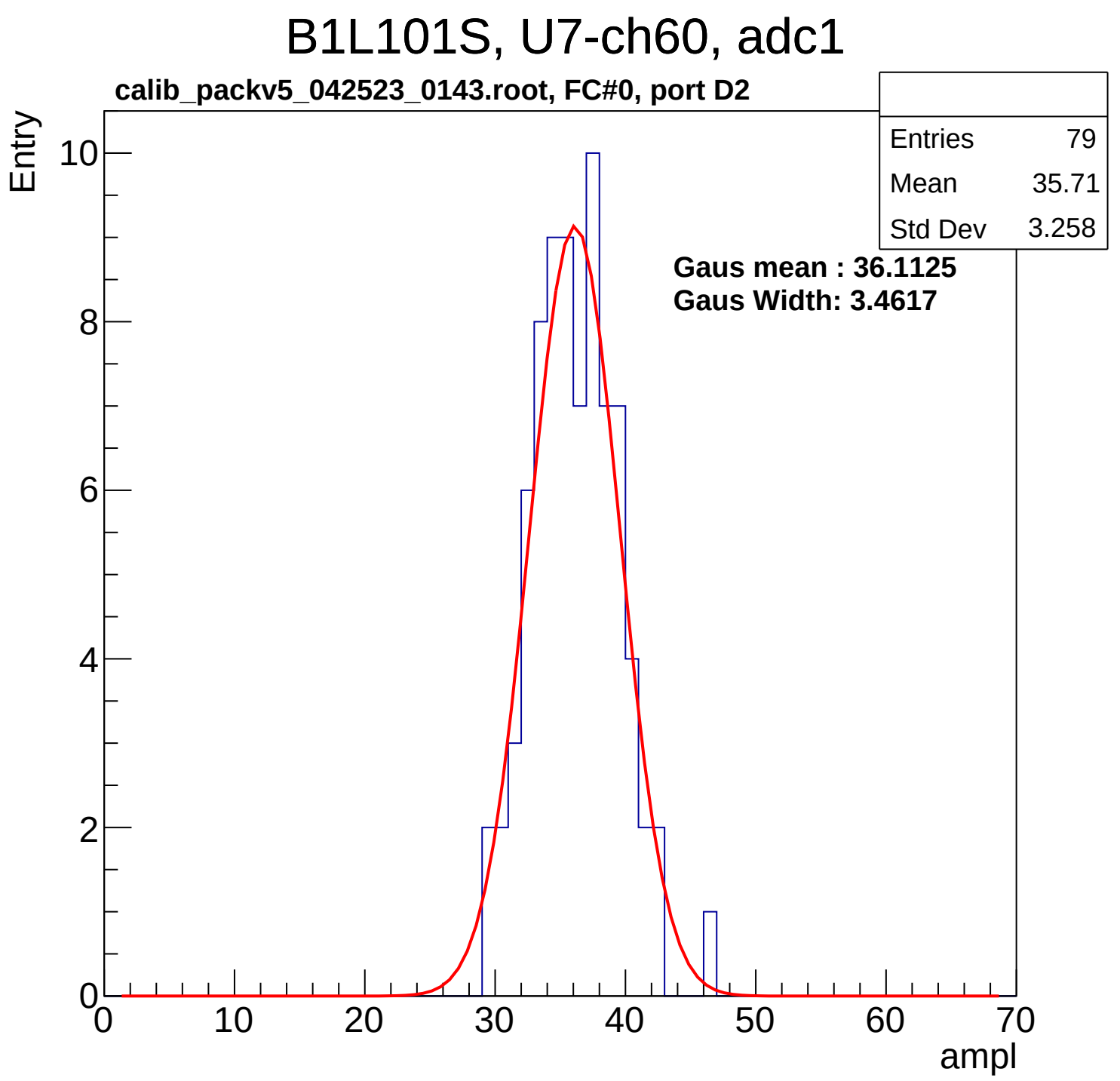

B1L101S, U7-ch59, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 0
Std Dev 0
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch60, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 28.42
Std Dev 3.141
Gaus mean : 29.0027
Gaus Width: 2.9383
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch60, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 35.71
Std Dev 3.258
Gaus mean : 36.1125
Gaus Width: 3.4617
Entry
ampl
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2
4
6
8
10
0
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20
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40
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60
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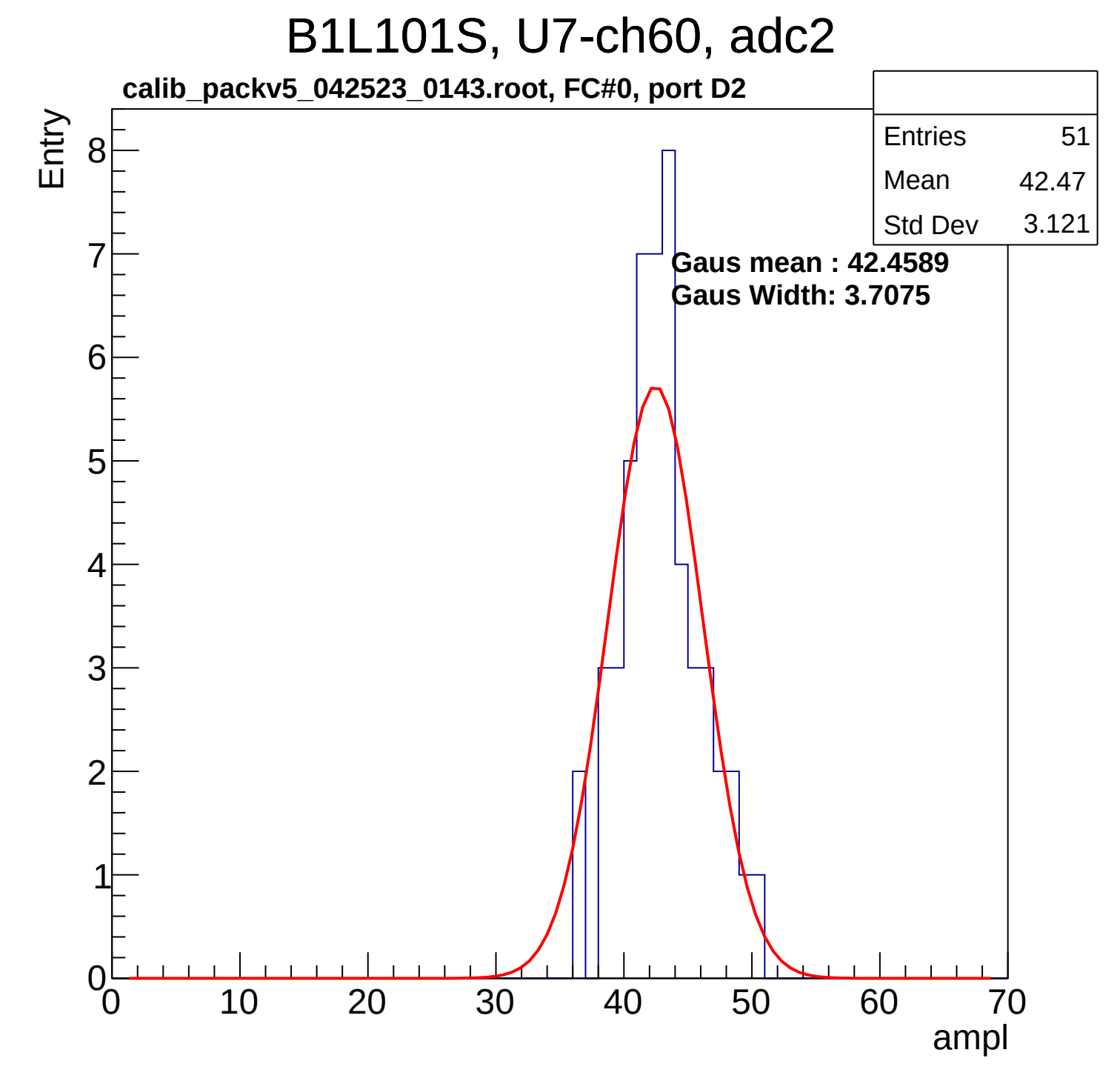
B1L101S, U7-ch60, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 42.47
Std Dev 3.121
Gaus mean : 42.4589
Gaus Width: 3.7075
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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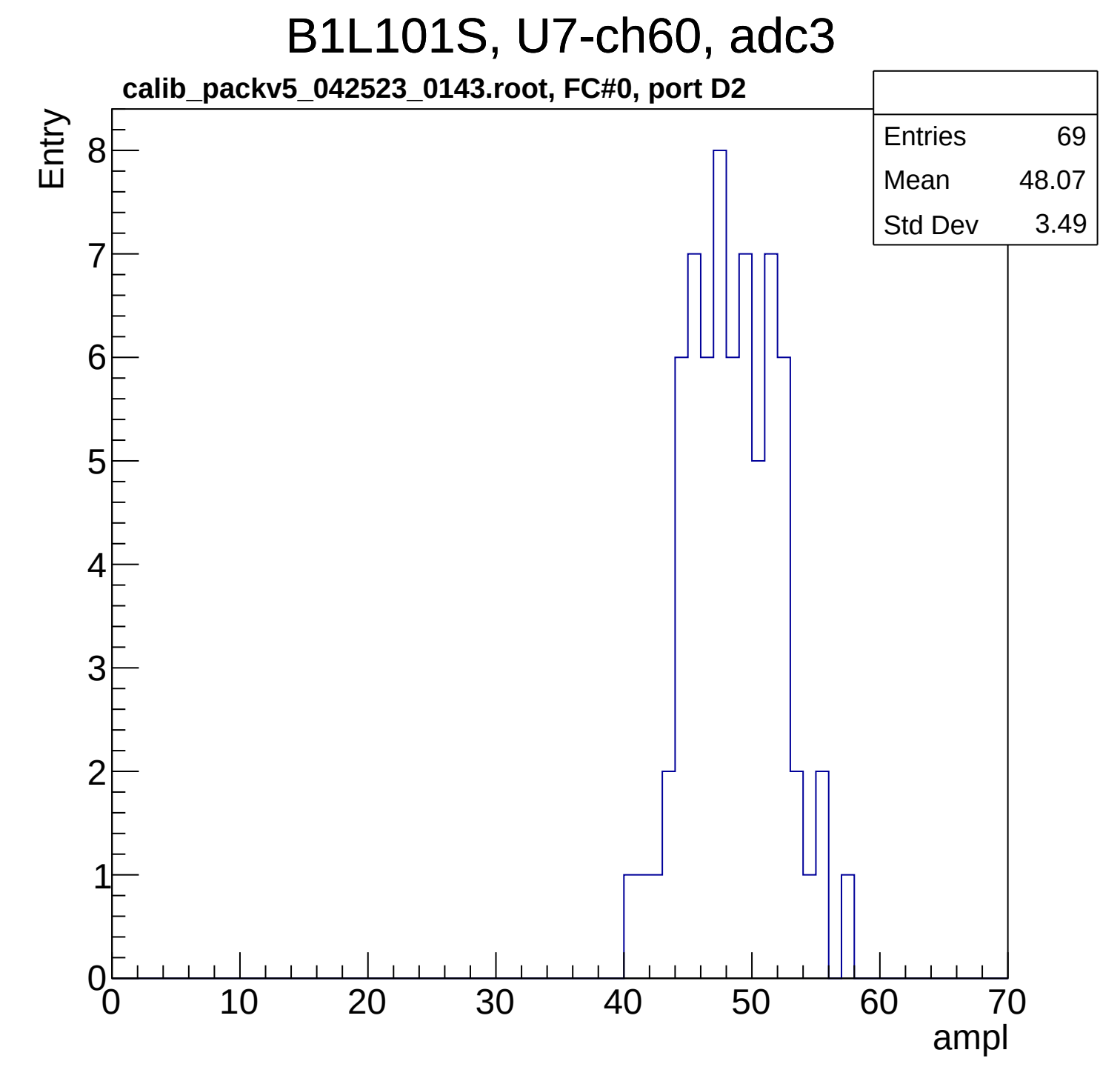
B1L101S, U7-ch60, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 48.07
Std Dev 3.49
Entry
ampl
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3
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5
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0
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60
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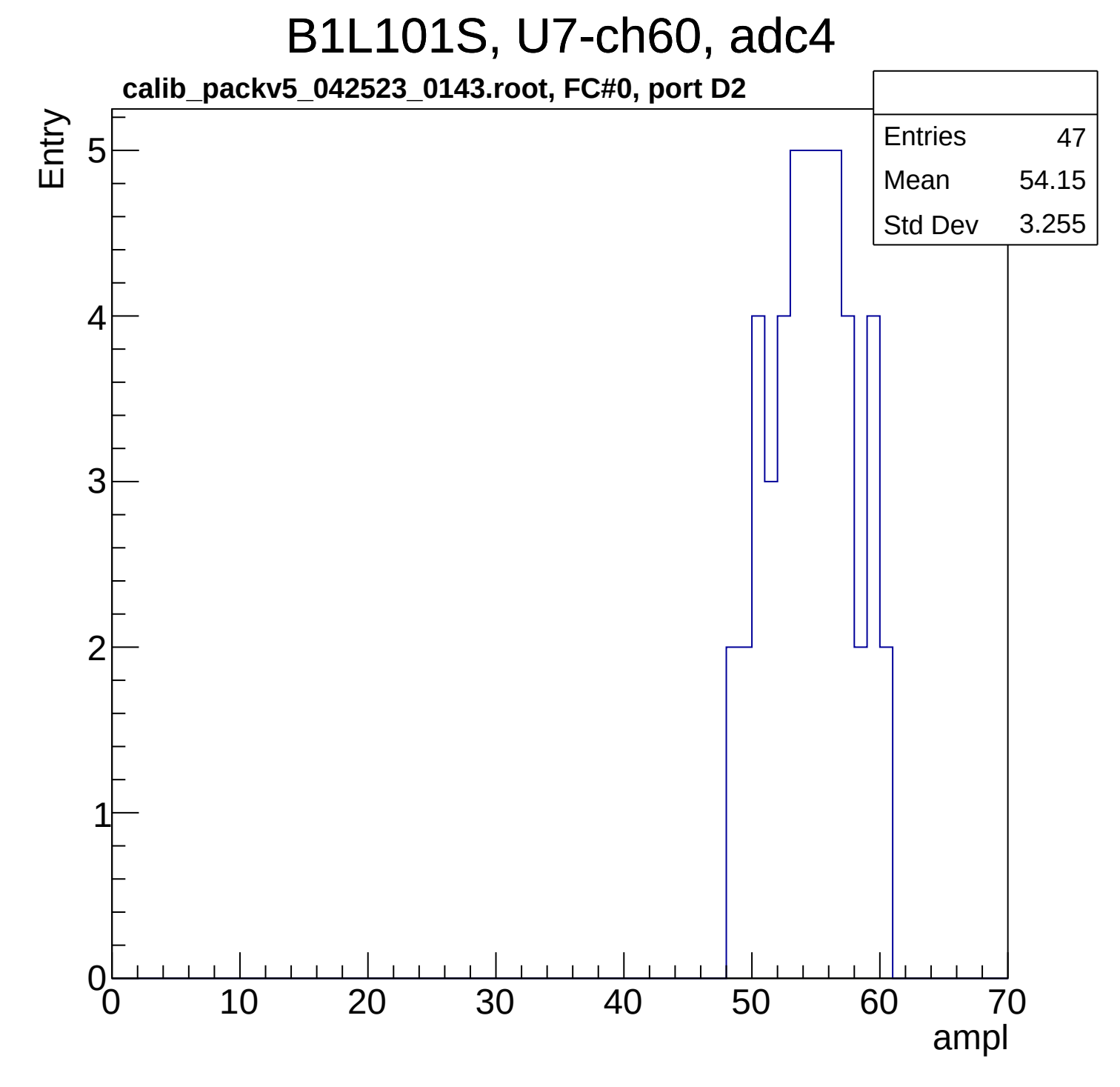
B1L101S, U7-ch60, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 54.15
Std Dev 3.255
Entry
ampl
0
1
2
3
4
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0
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20
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40
50
60
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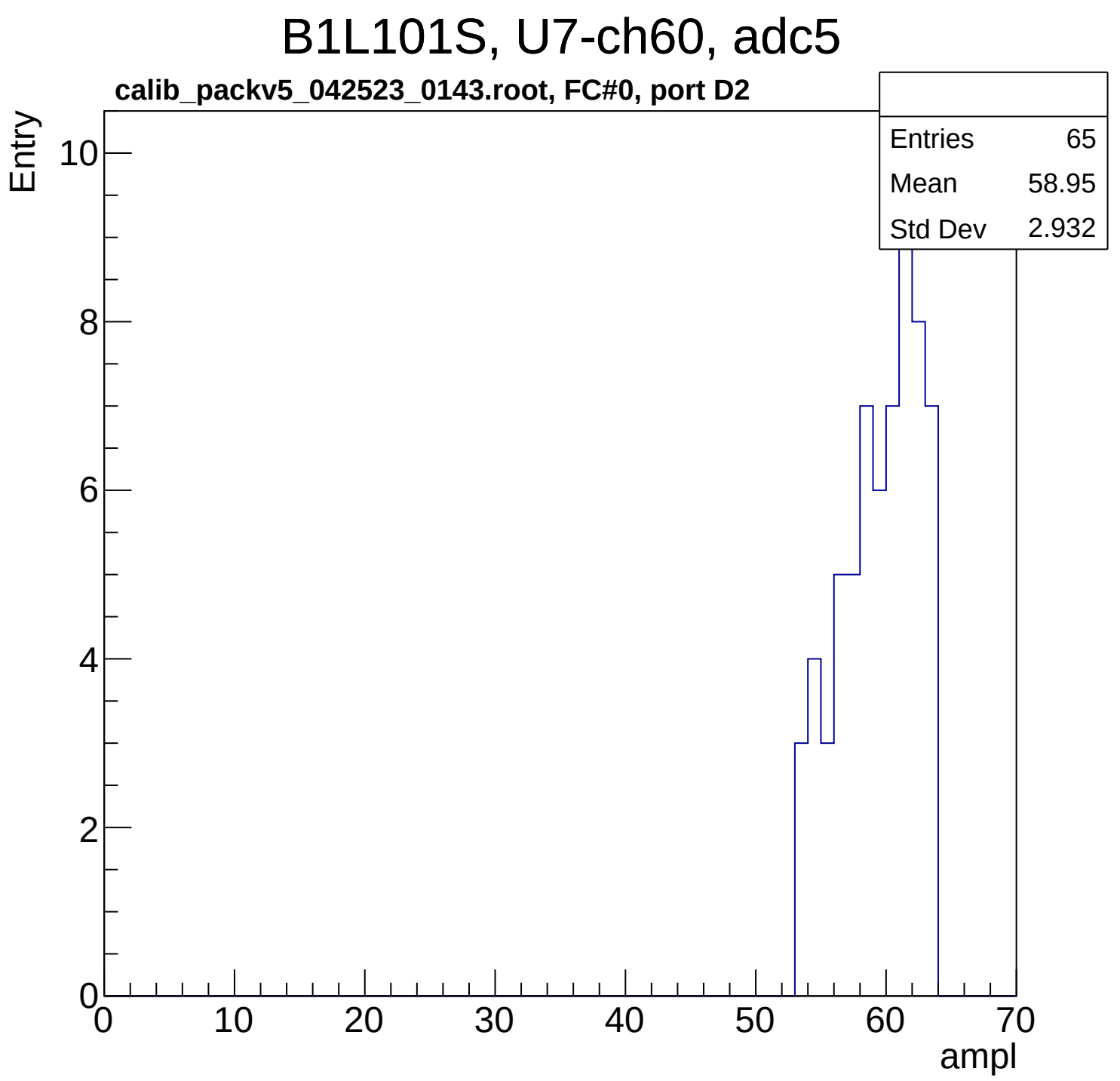
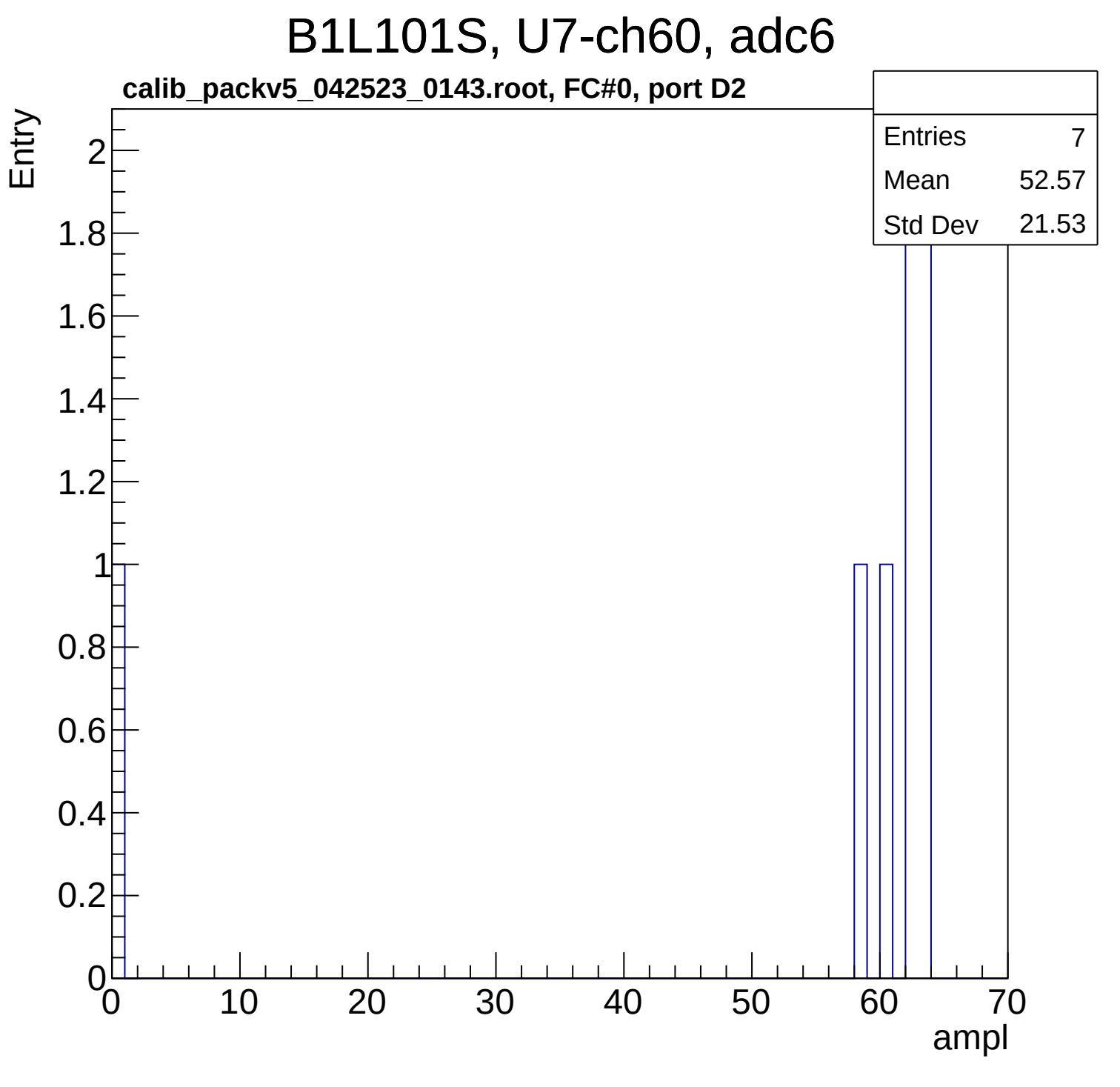

B1L101S, U7-ch60, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 58.95
Std Dev 2.932
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch60, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 52.57
Std Dev 21.53
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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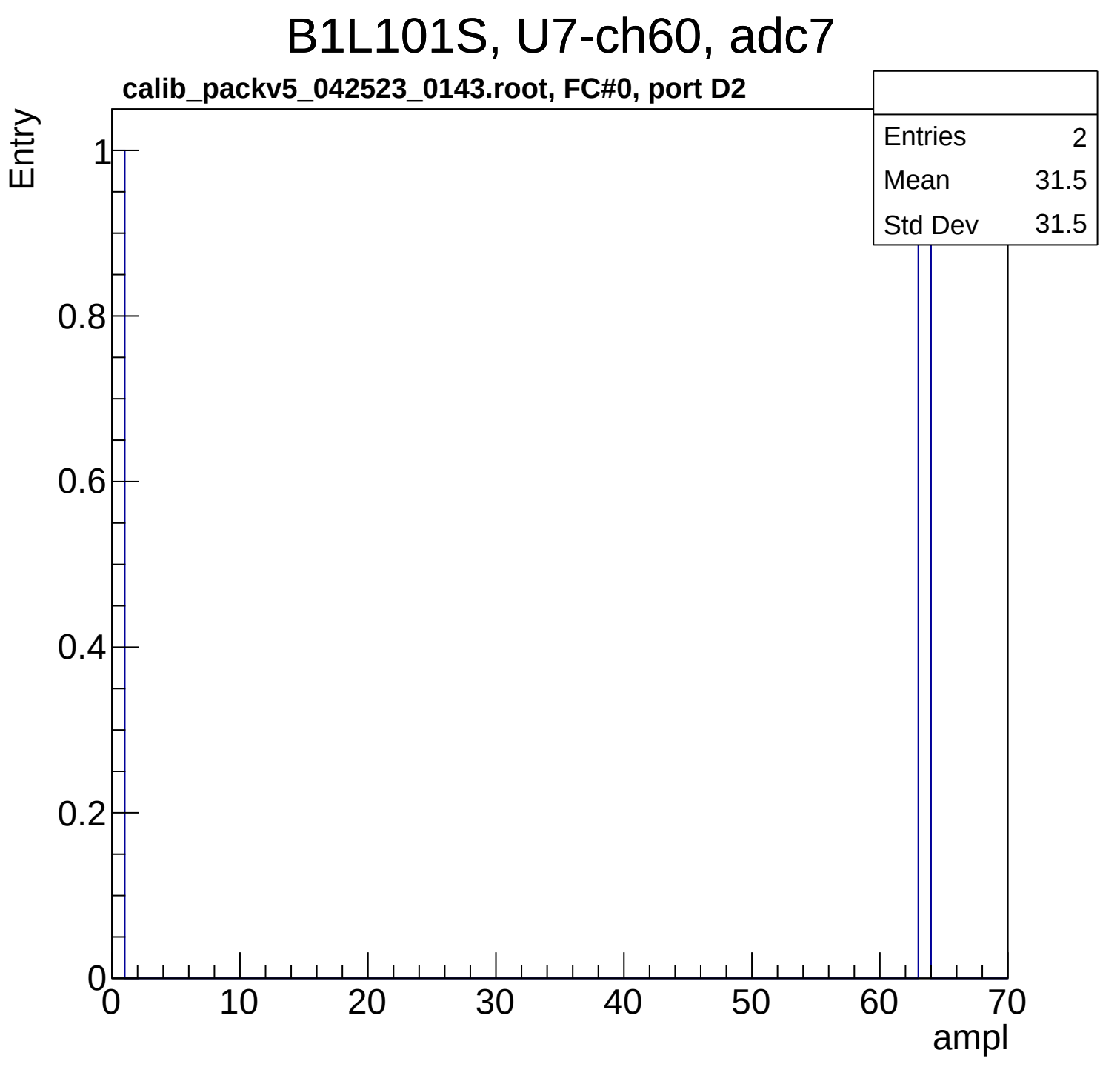
B1L101S, U7-ch60, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
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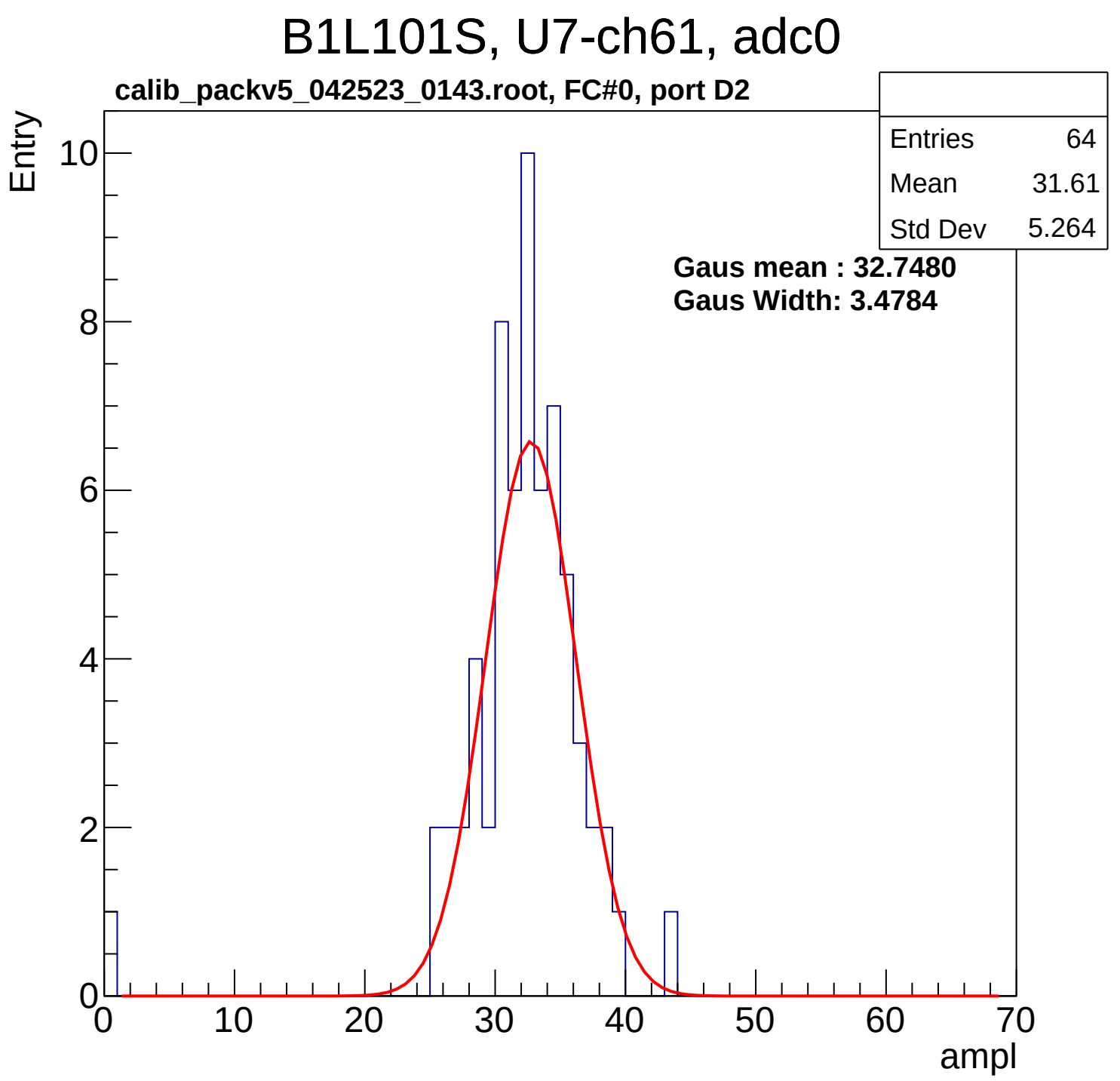
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch61, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 31.61
Std Dev 5.264
Gaus mean : 32.7480
Gaus Width: 3.4784
Entry
ampl
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2
4
6
8
10
0
10
20
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40
50
60
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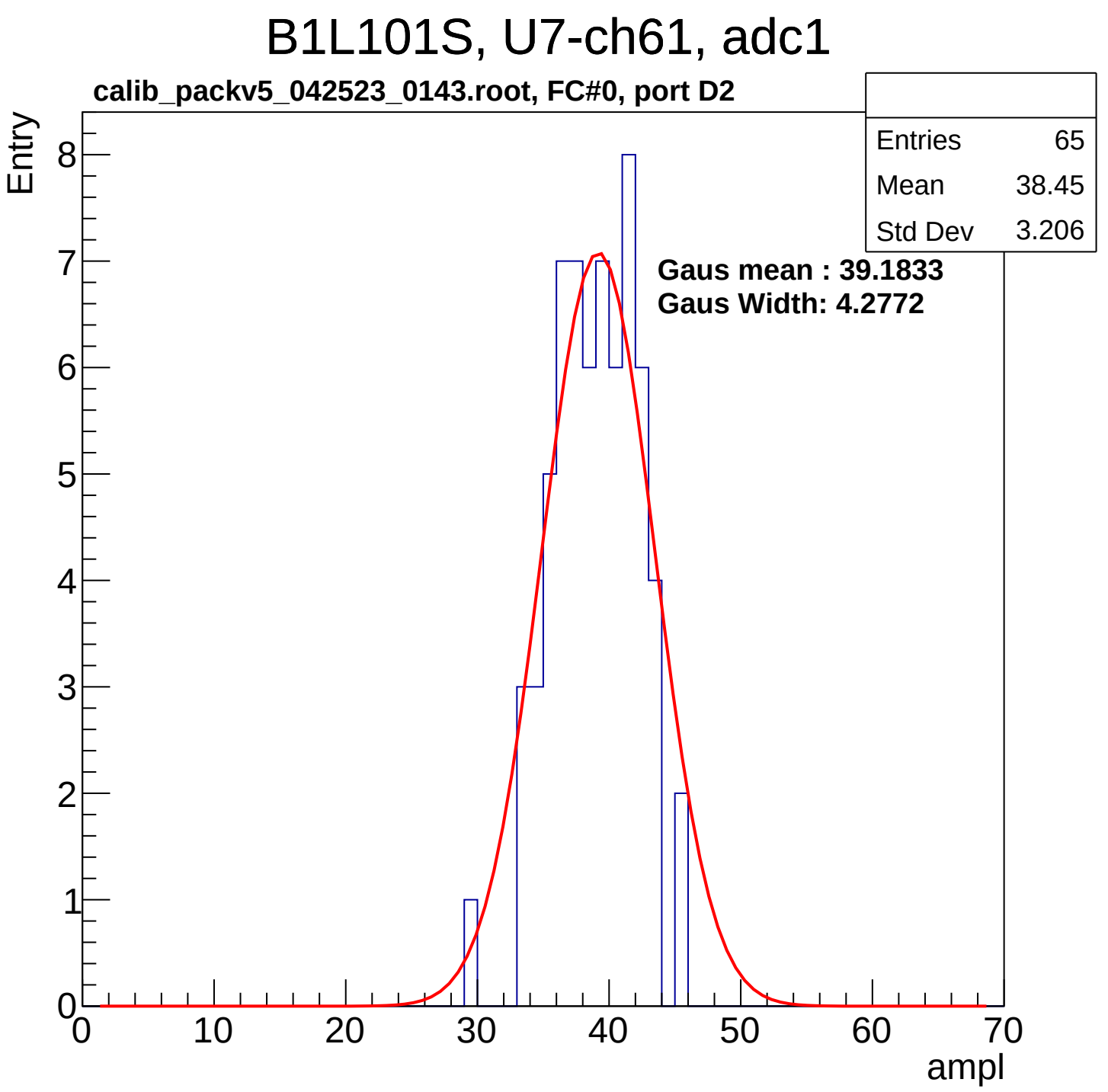
B1L101S, U7-ch61, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 38.45
Std Dev 3.206
Gaus mean : 39.1833
Gaus Width: 4.2772
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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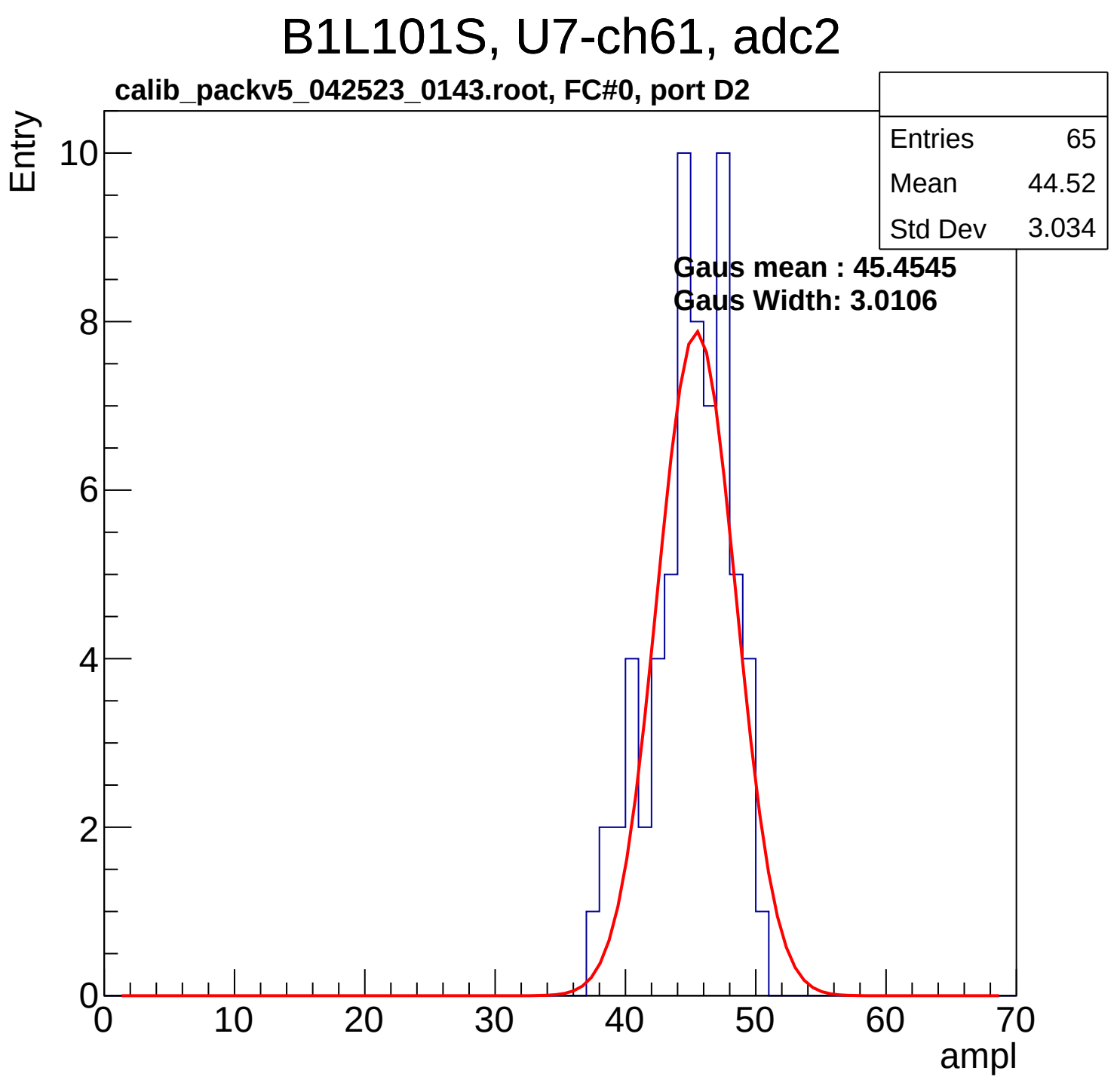
B1L101S, U7-ch61, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 44.52
Std Dev 3.034
Gaus mean : 45.4545
Gaus Width: 3.0106
Entry
ampl
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4
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0
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50
60
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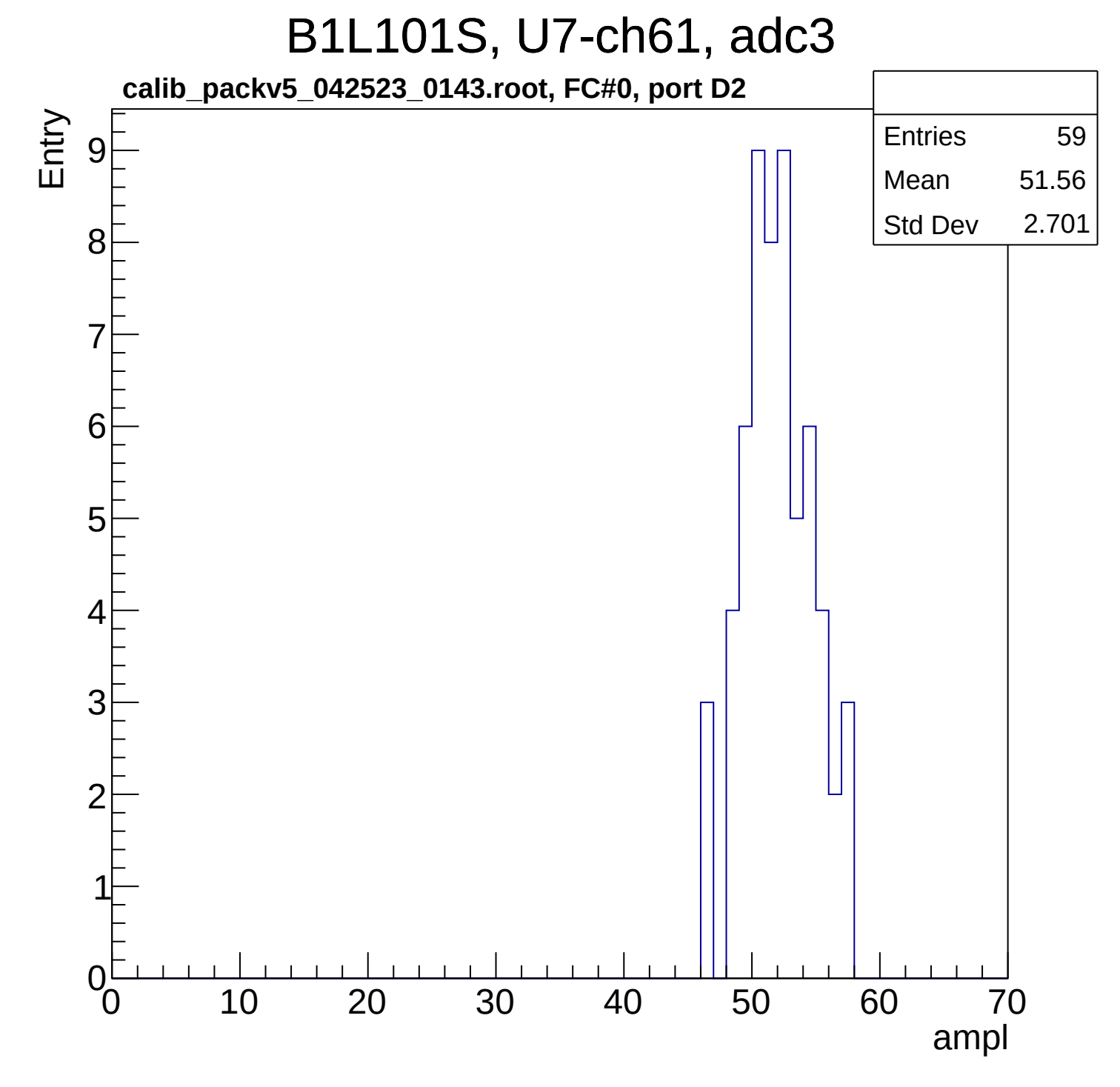
B1L101S, U7-ch61, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 51.56
Std Dev 2.701
Entry
ampl
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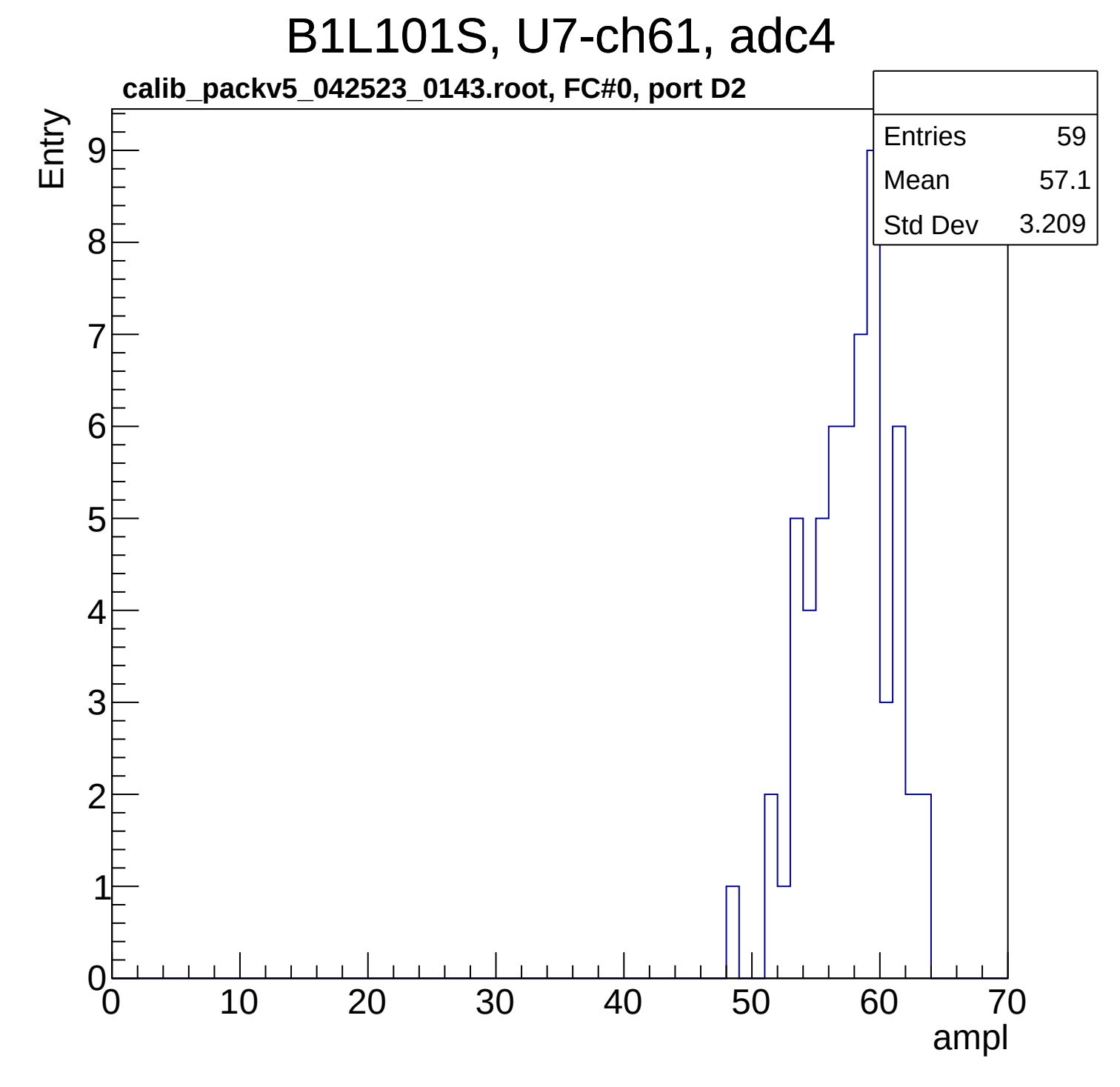
B1L101S, U7-ch61, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 57.1
Std Dev 3.209
Entry
ampl
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3
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5
6
7
8
9
0
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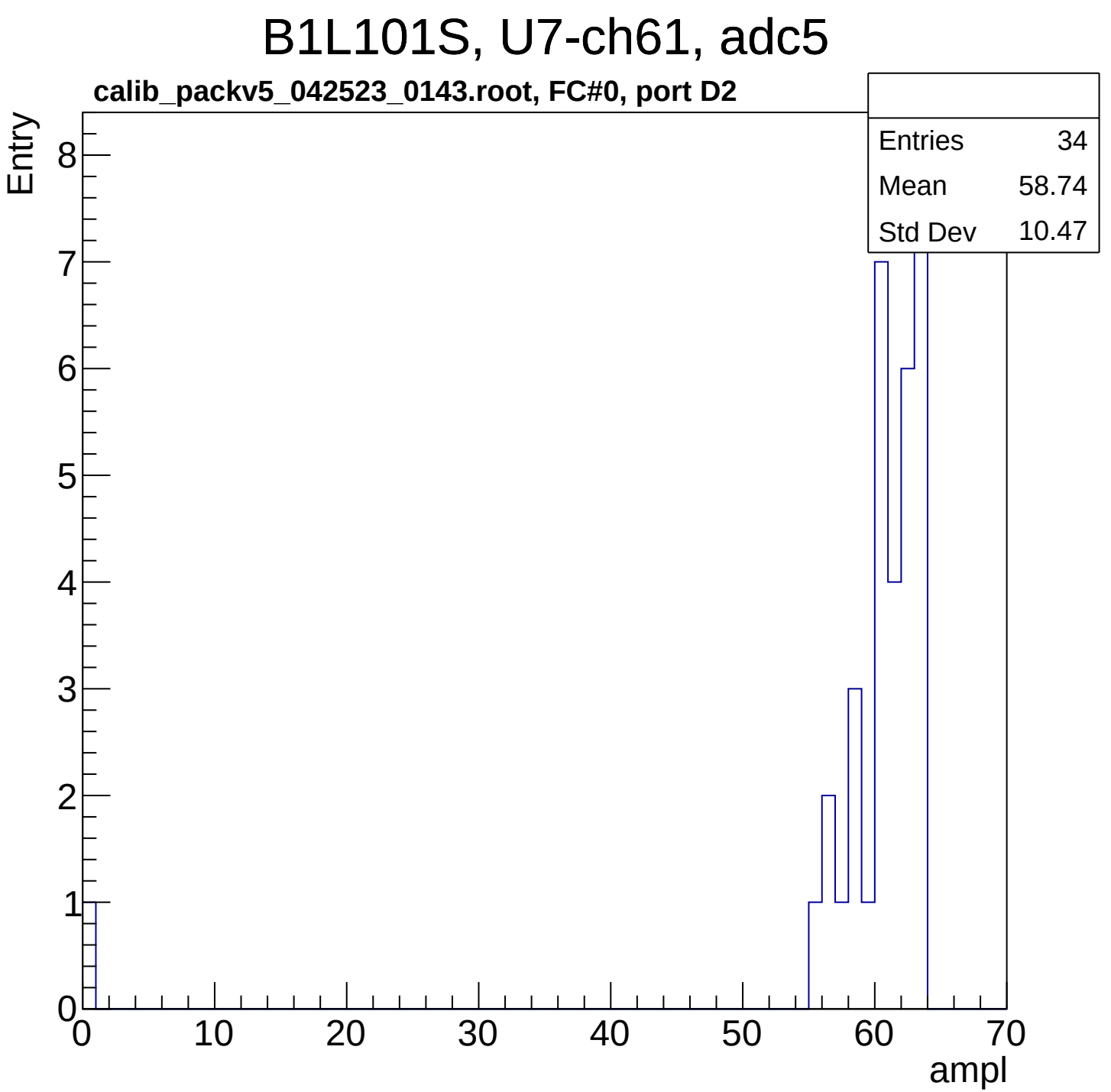
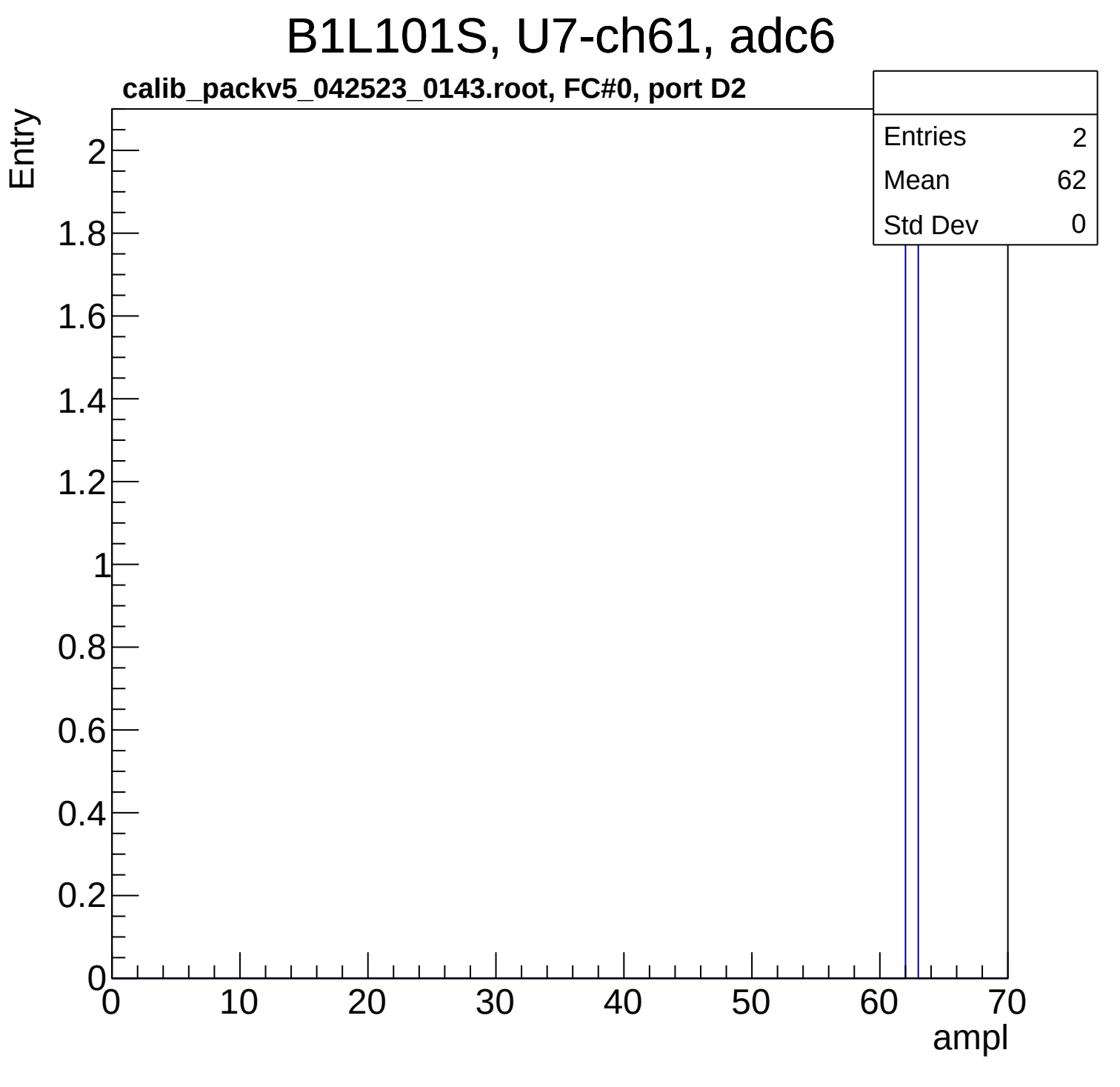

B1L101S, U7-ch61, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 34
Mean 58.74
Std Dev 10.47
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch61, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 62
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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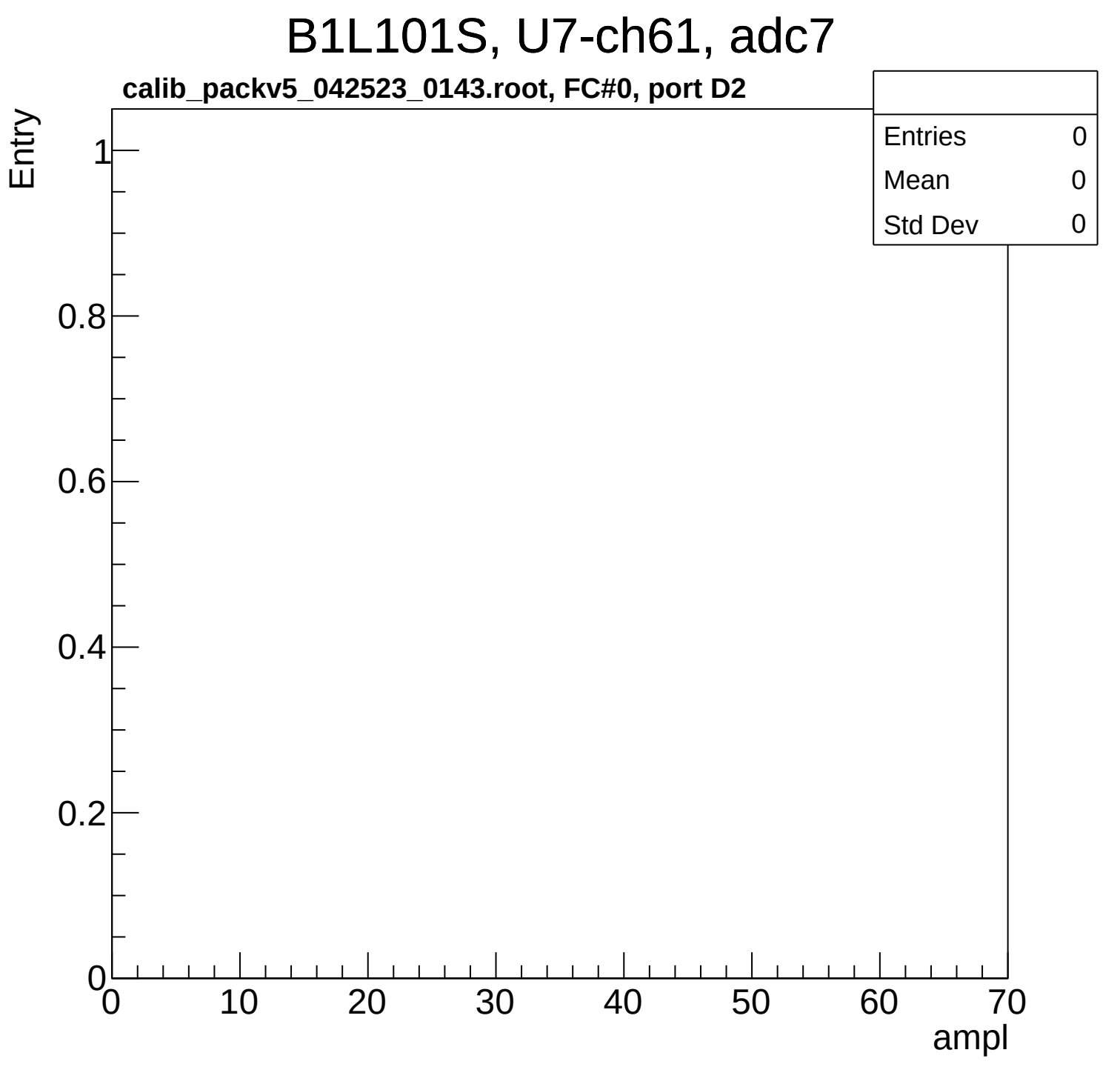
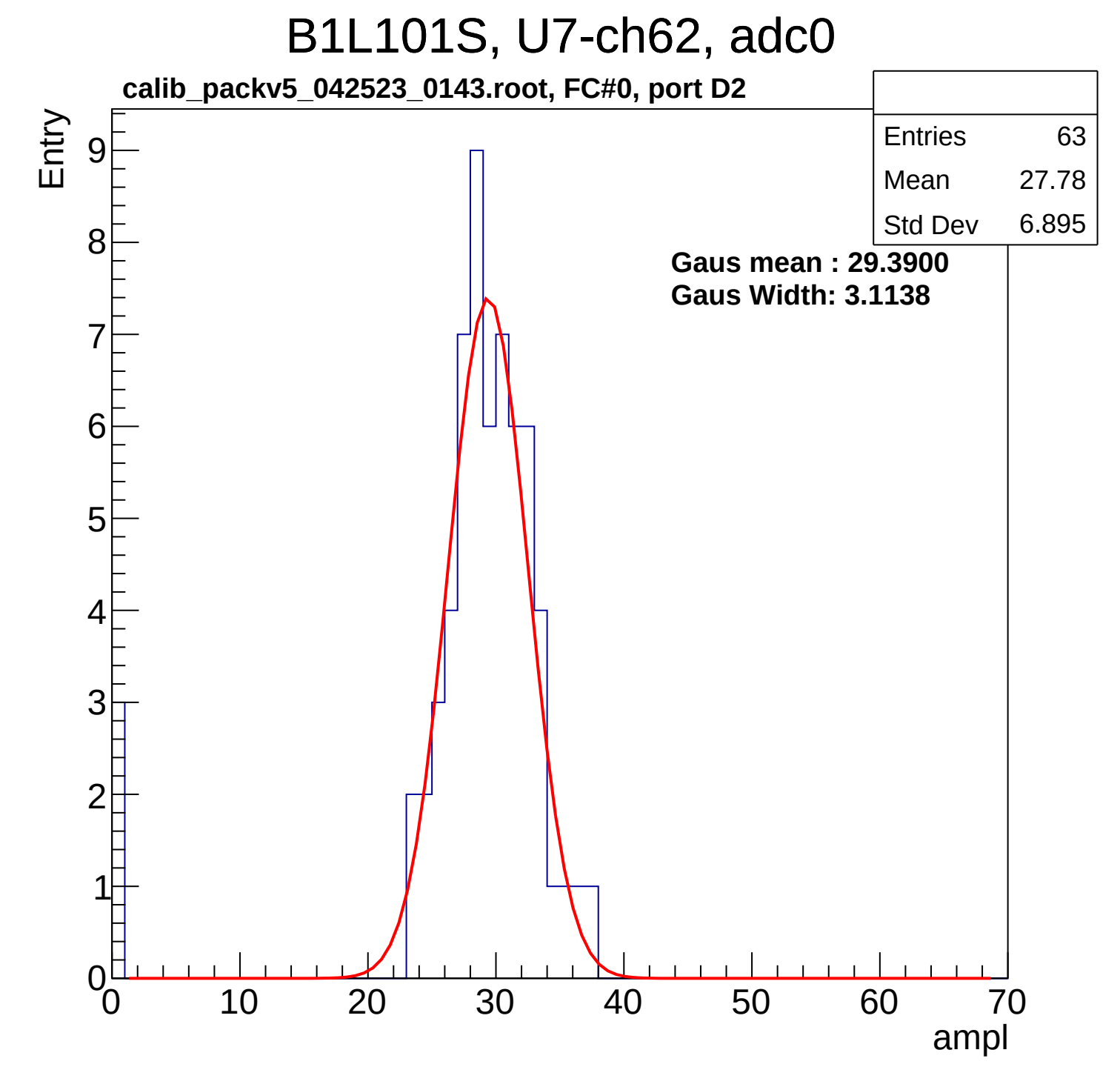
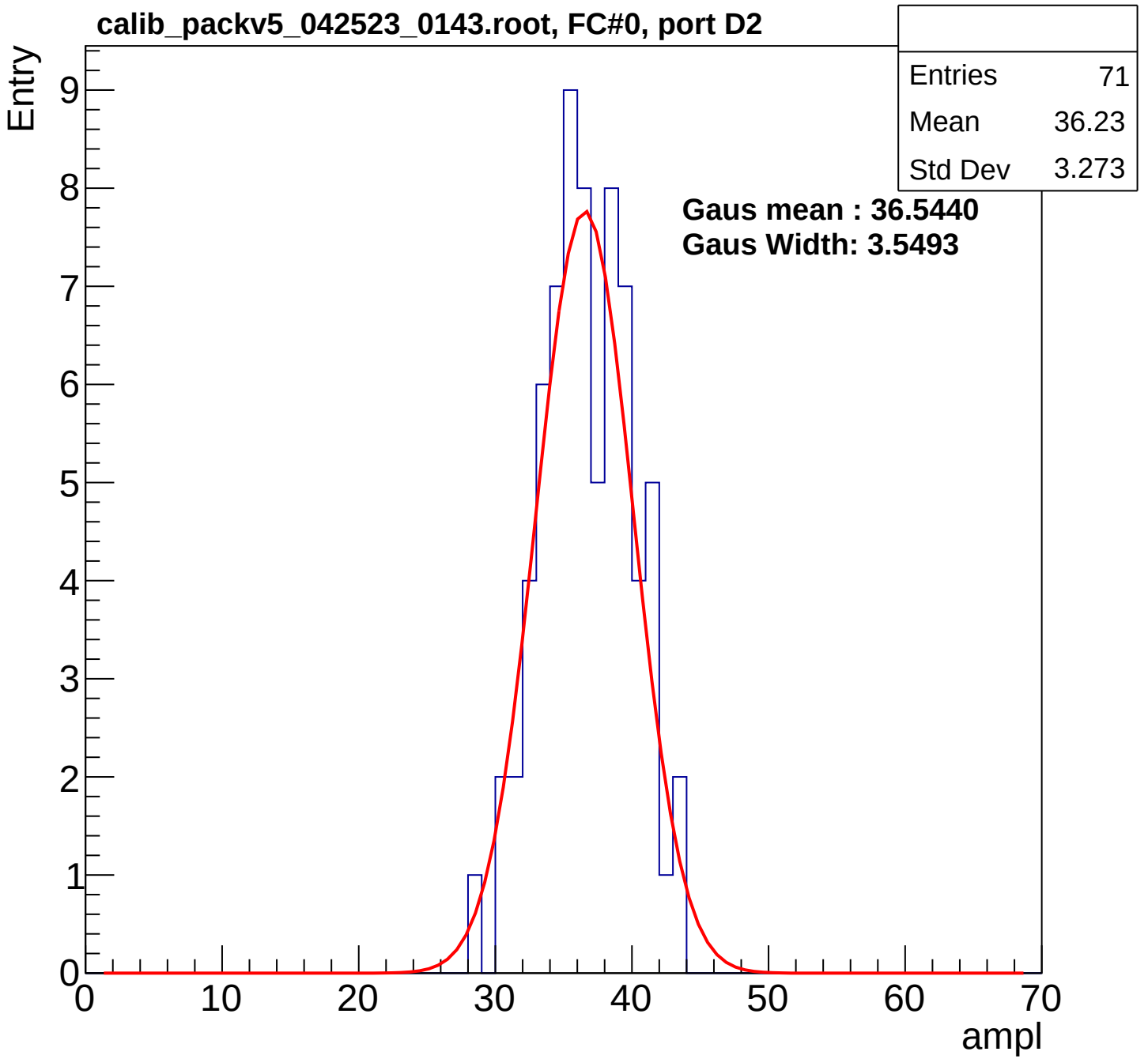
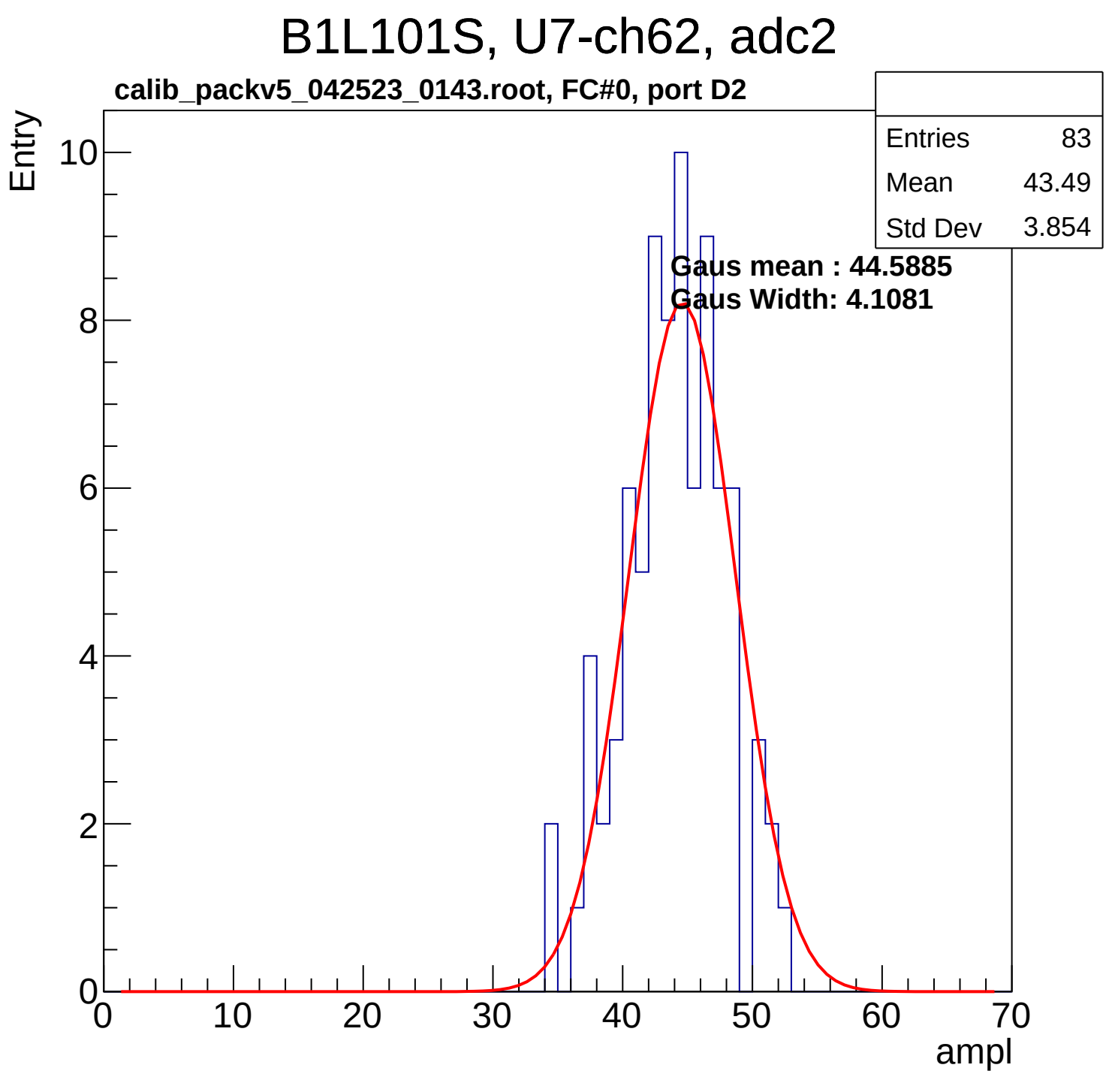
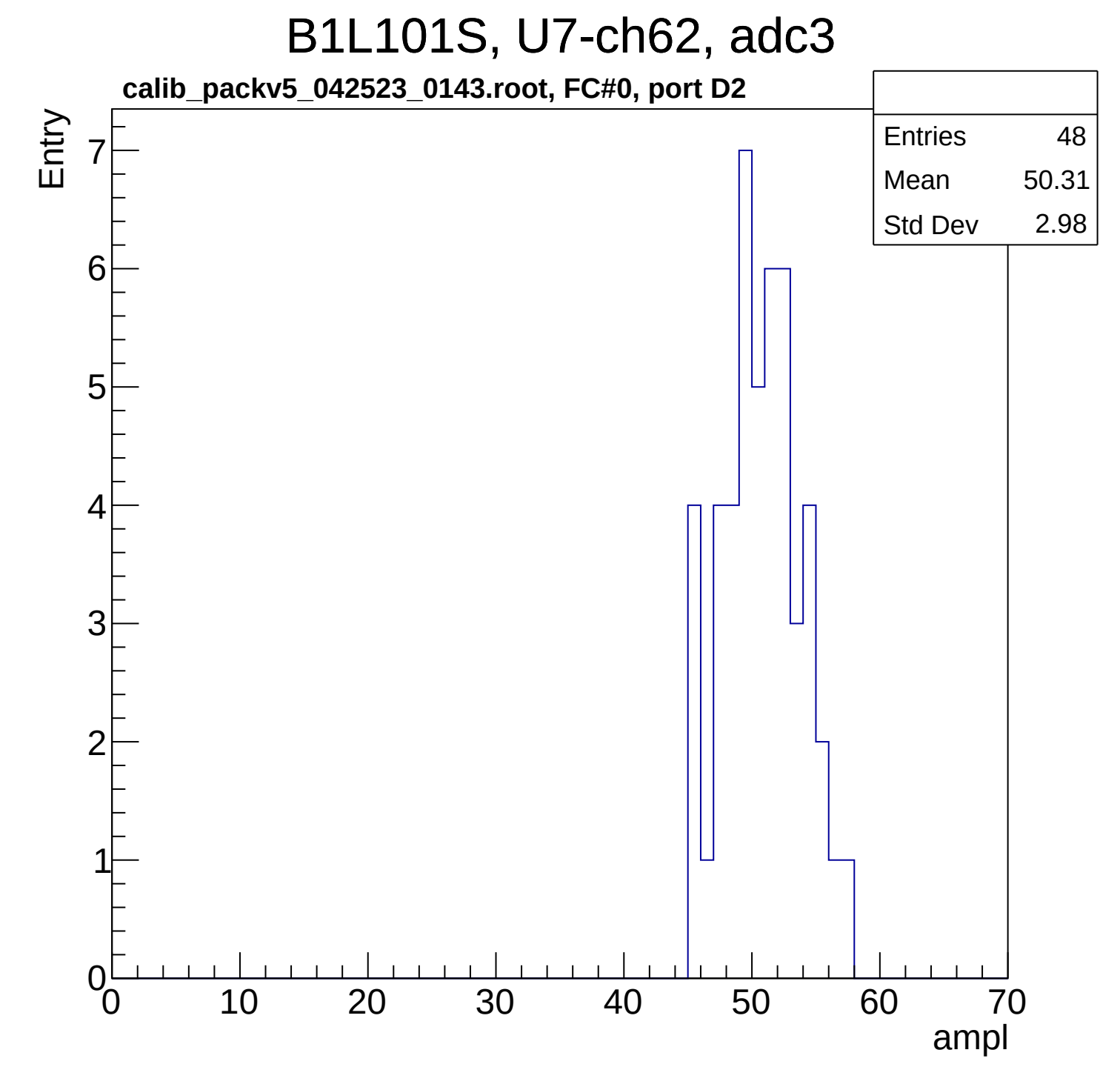
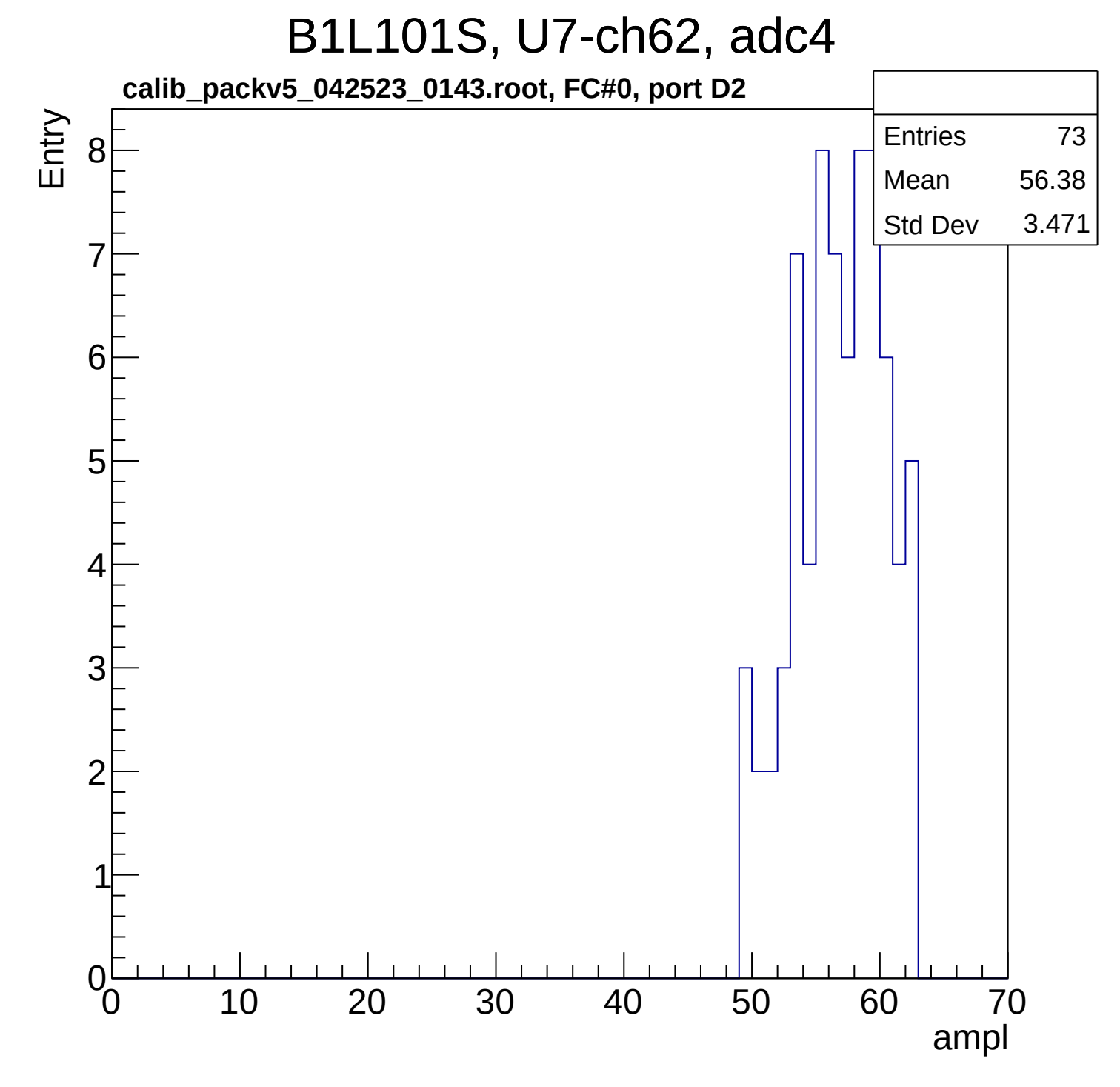

B1L101S, U7-ch61, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch62, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 27.78
Std Dev 6.895
Gaus mean : 29.3900
Gaus Width: 3.1138
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch62, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 36.23
Std Dev 3.273
Gaus mean : 36.5440
Gaus Width: 3.5493
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L101S, U7-ch62, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 83
Mean 43.49
Std Dev 3.854
Gaus mean : 44.5885
Gaus Width: 4.1081
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch62, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 50.31
Std Dev 2.98
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U7-ch62, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 56.38
Std Dev 3.471
Entry
ampl
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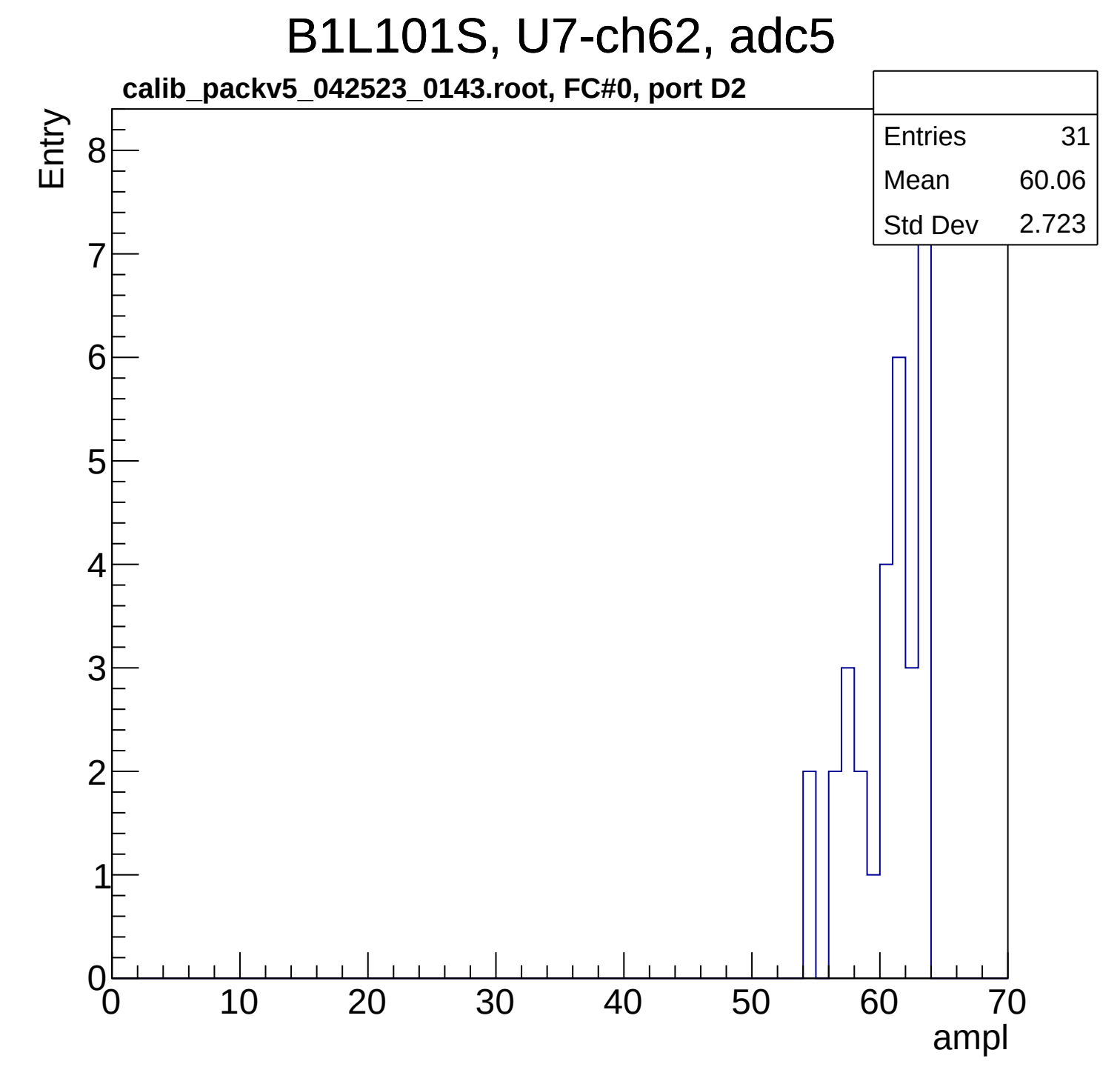
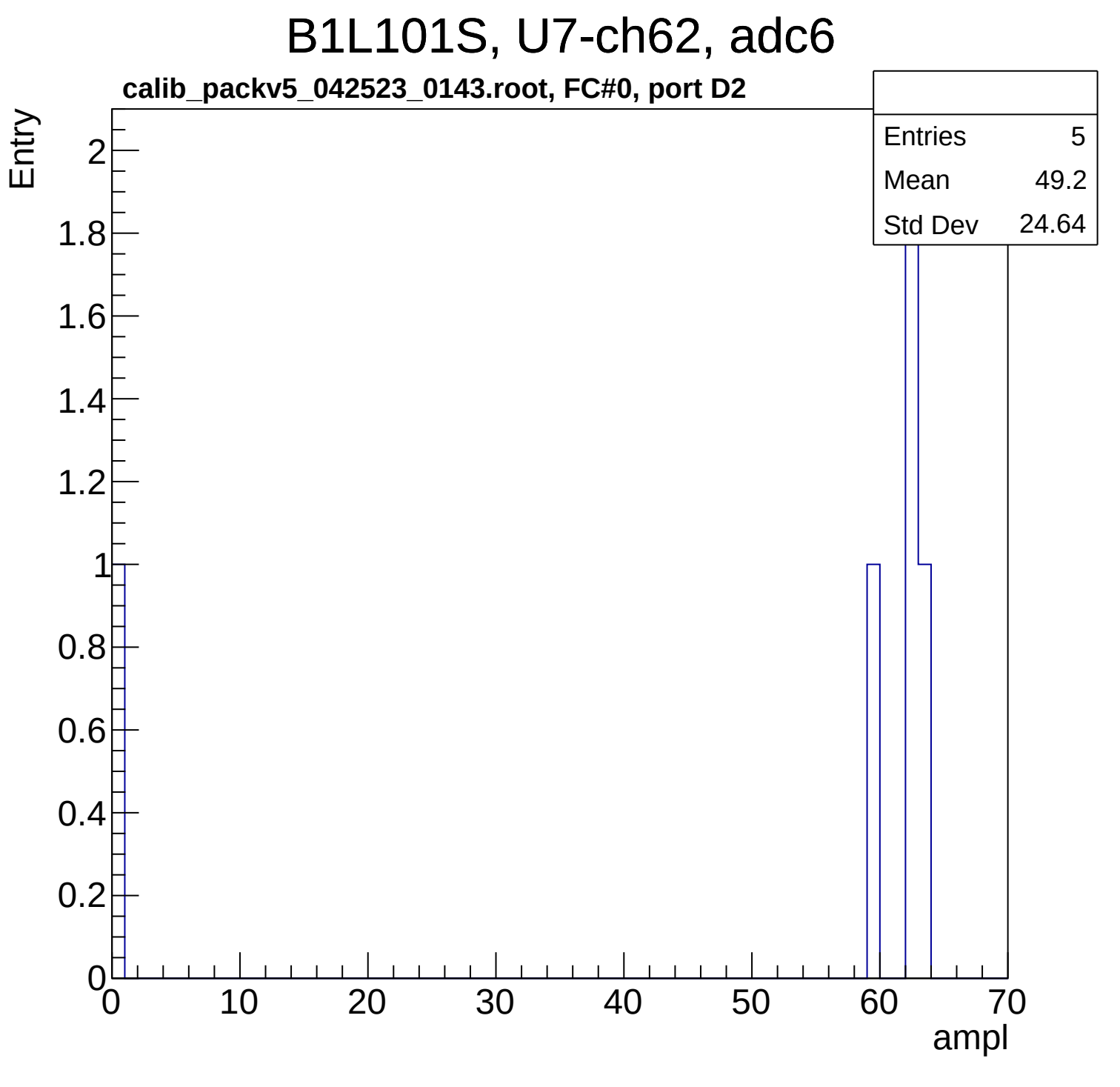
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch62, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 31
Mean 60.06
Std Dev 2.723
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch62, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 49.2
Std Dev 24.64
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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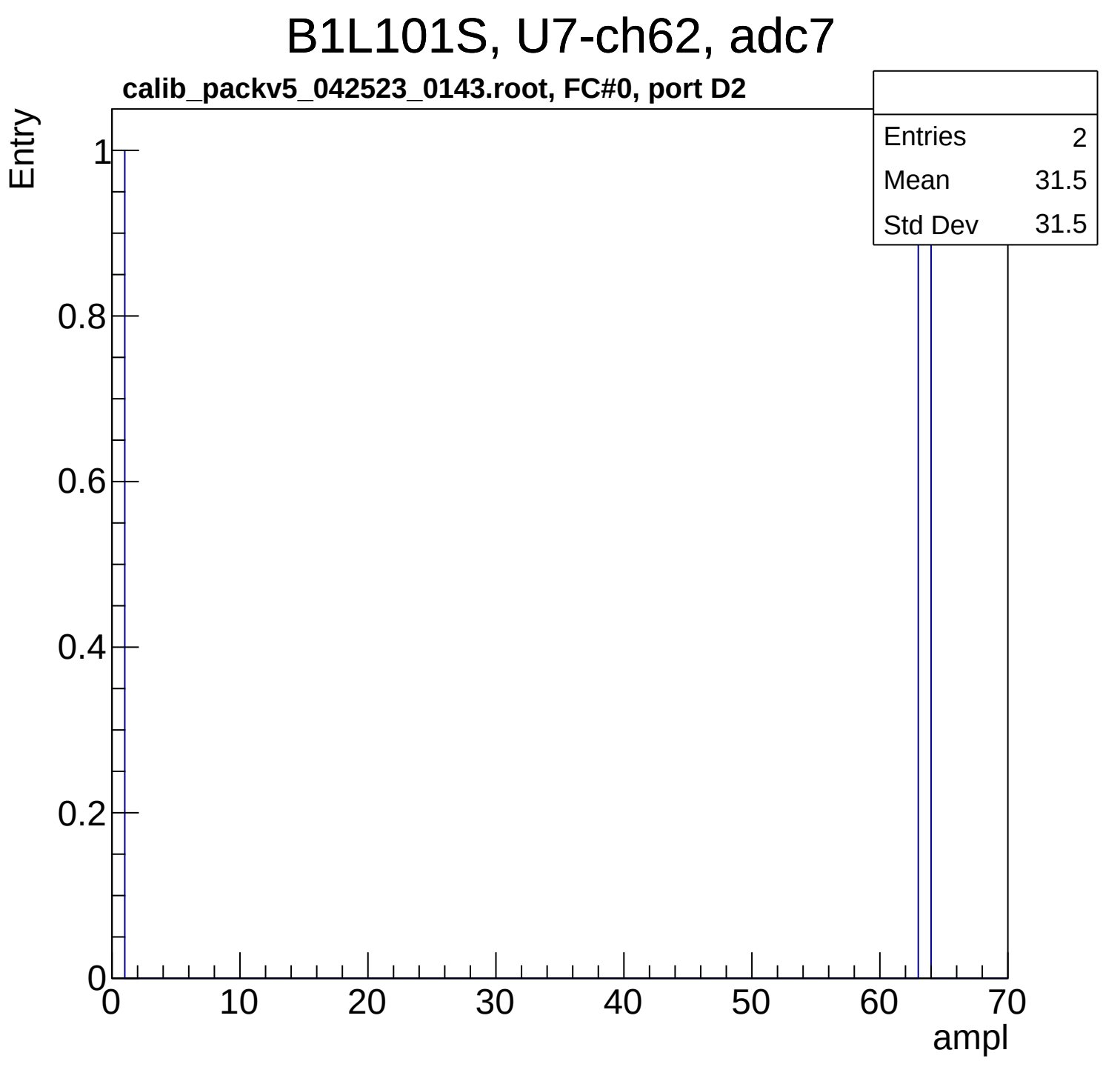
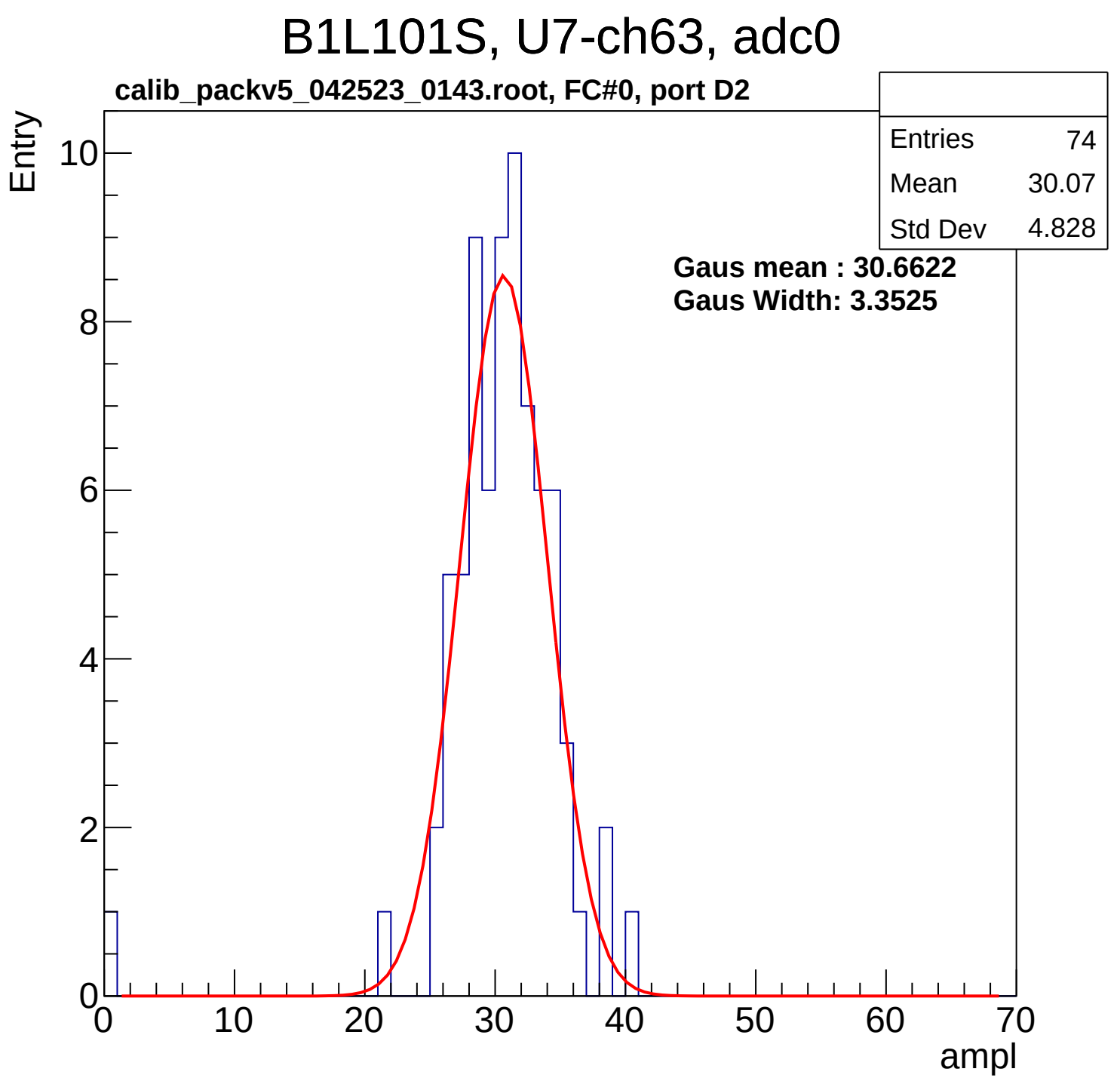
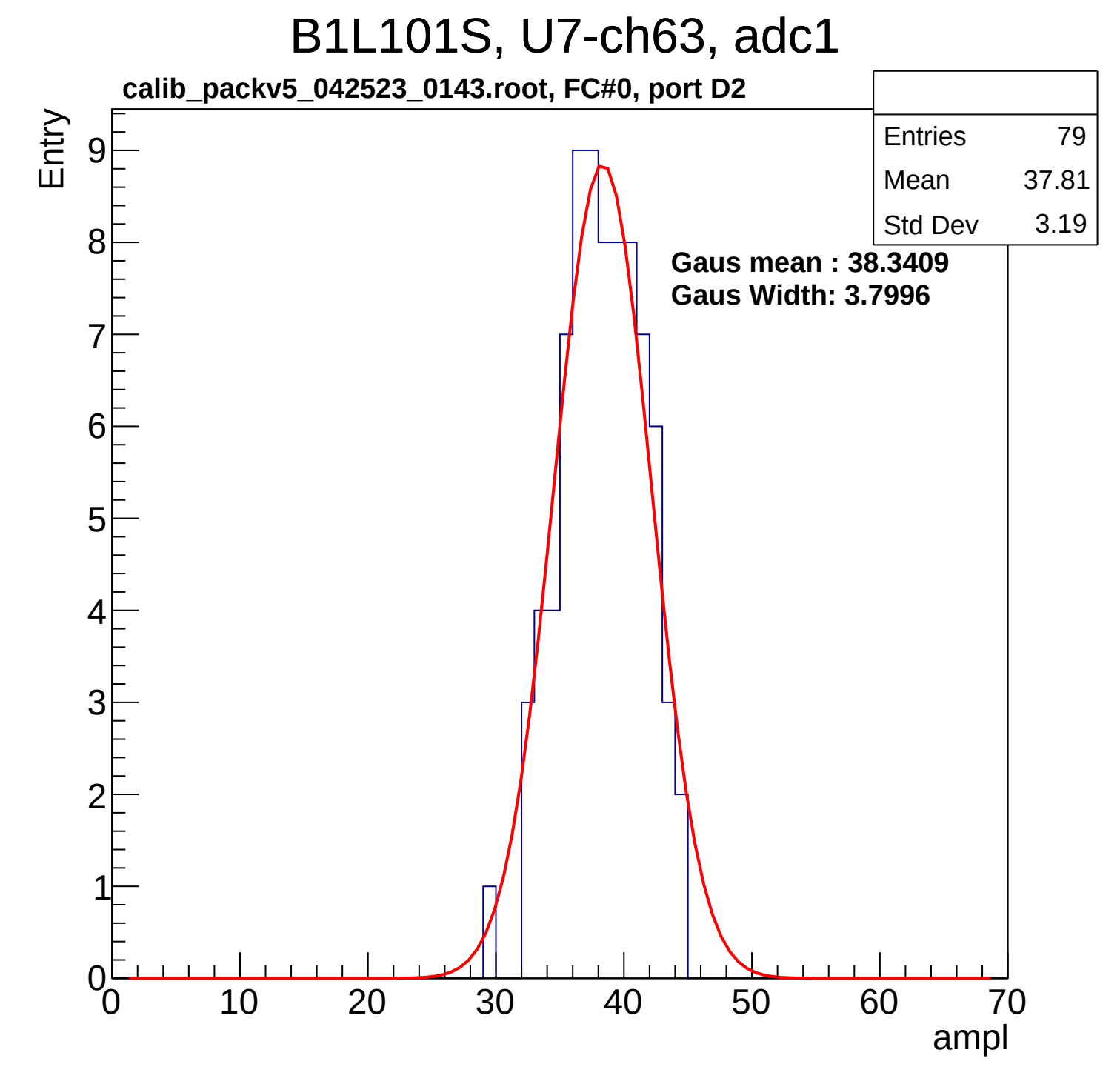
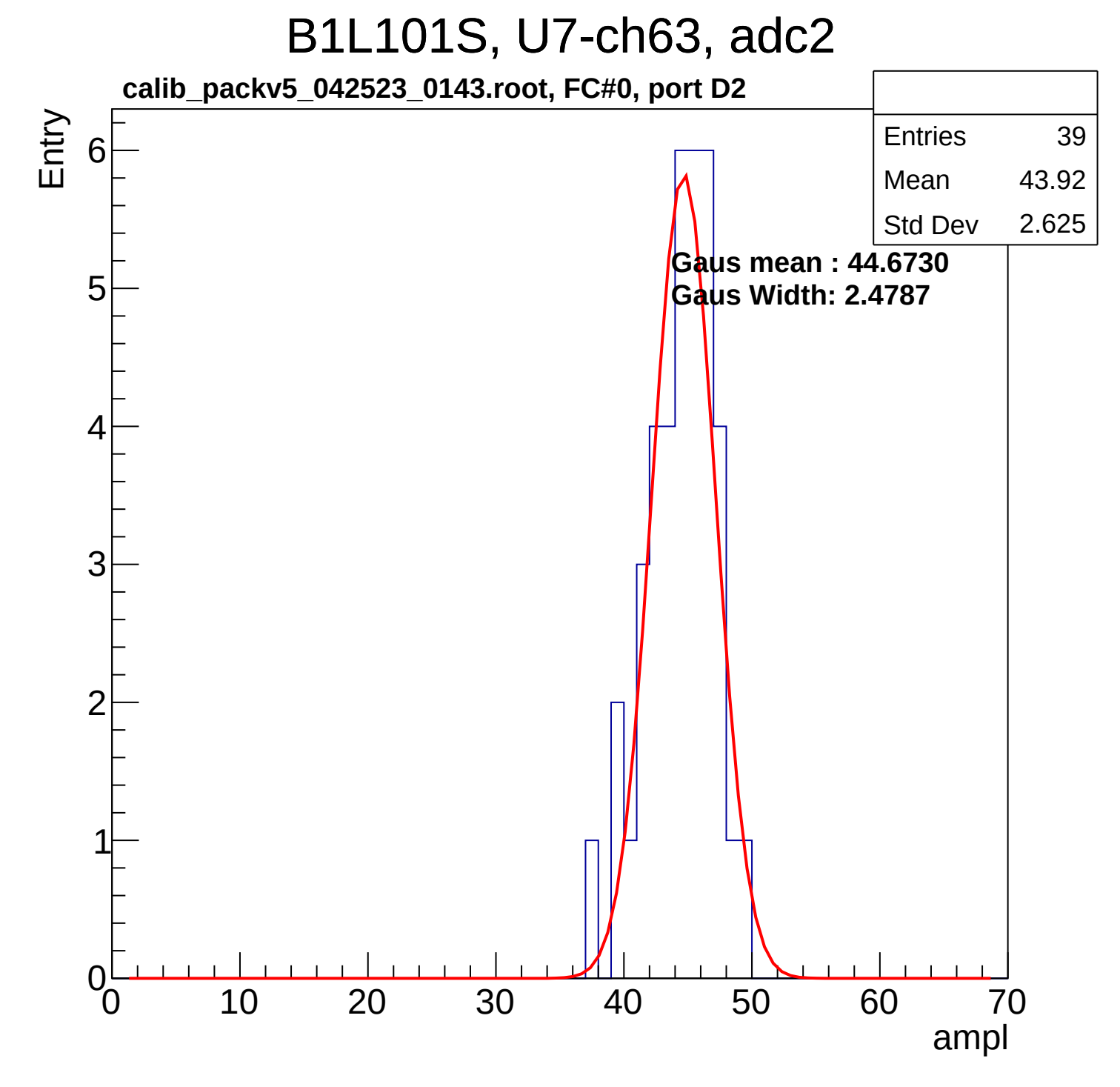

B1L101S, U7-ch62, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch63, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 30.07
Std Dev 4.828
Gaus mean : 30.6622
Gaus Width: 3.3525
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch63, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 37.81
Std Dev 3.19
Gaus mean : 38.3409
Gaus Width: 3.7996
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch63, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 39
Mean 43.92
Std Dev 2.625
Gaus mean : 44.6730
Gaus Width: 2.4787
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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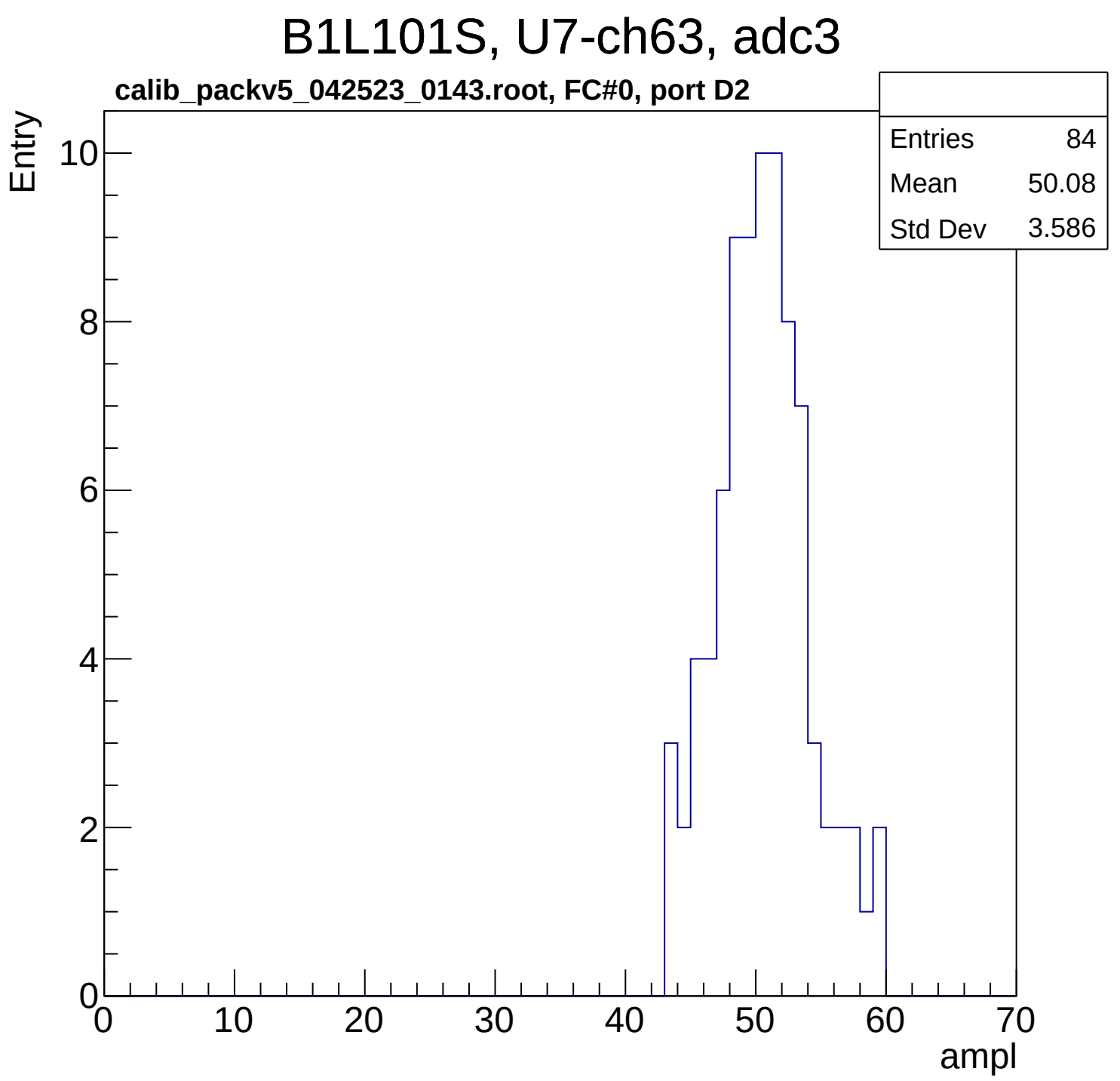
B1L101S, U7-ch63, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 84
Mean 50.08
Std Dev 3.586
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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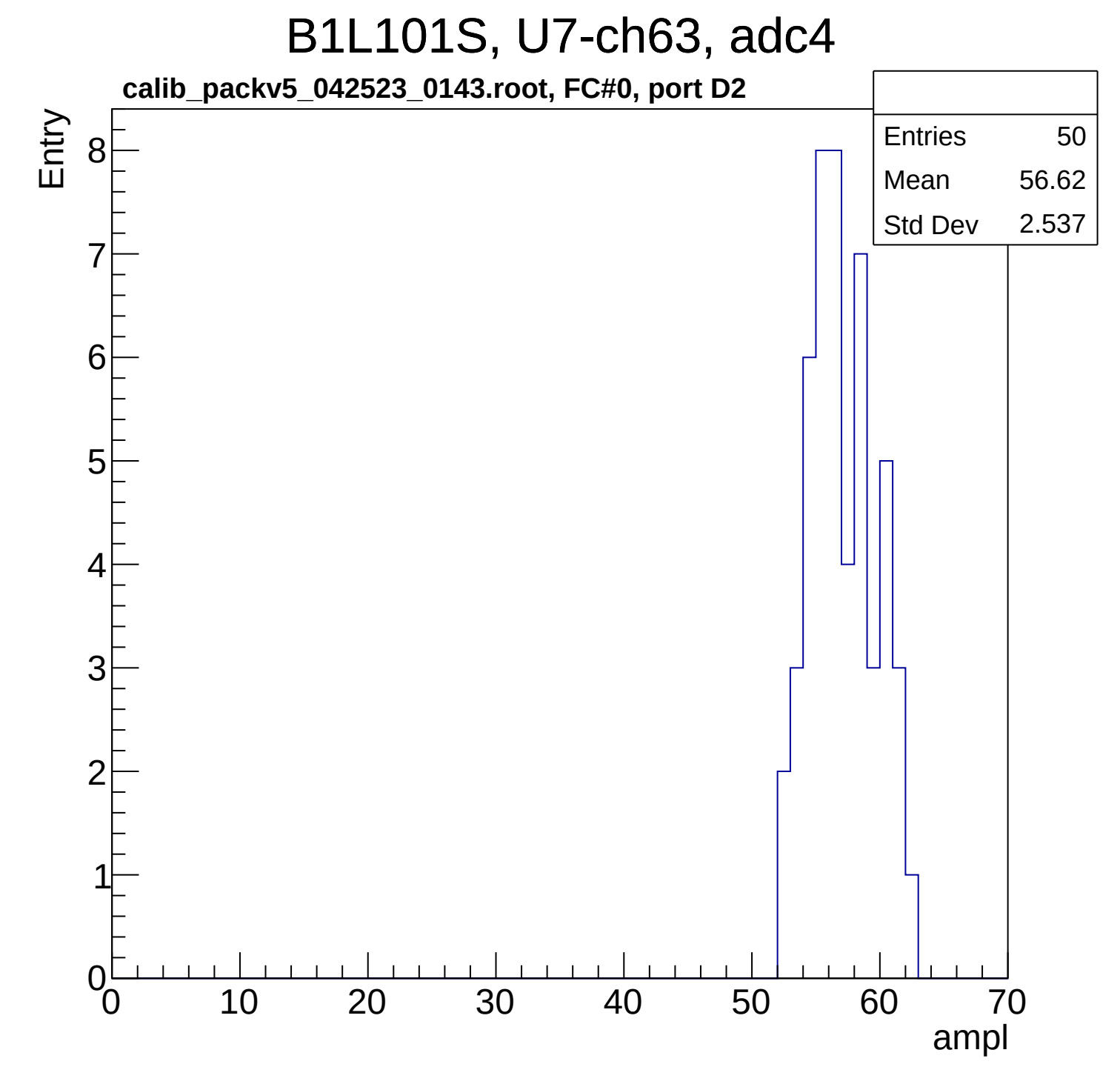
B1L101S, U7-ch63, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 56.62
Std Dev 2.537
Entry
ampl
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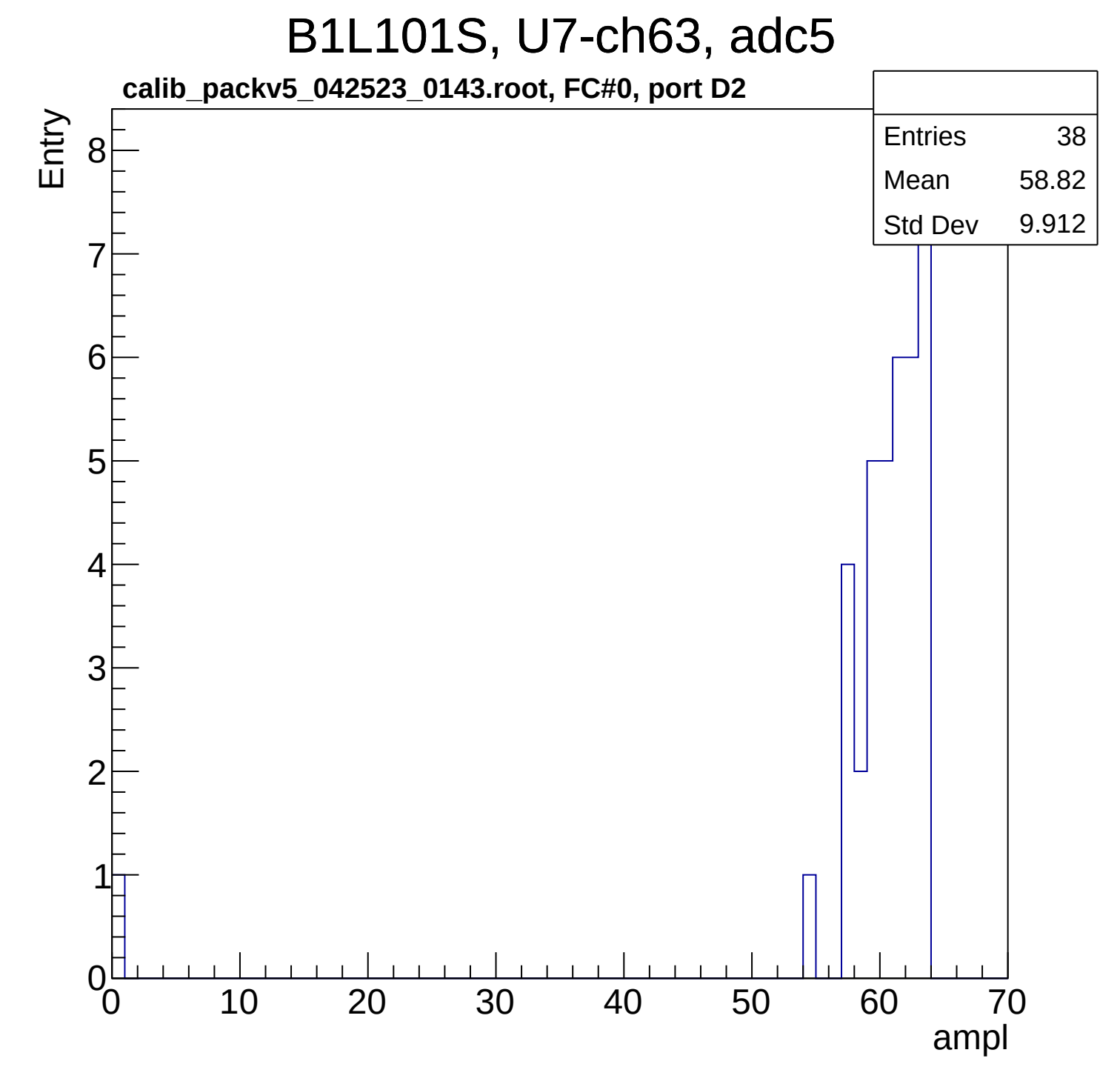
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch63, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 38
Mean 58.82
Std Dev 9.912
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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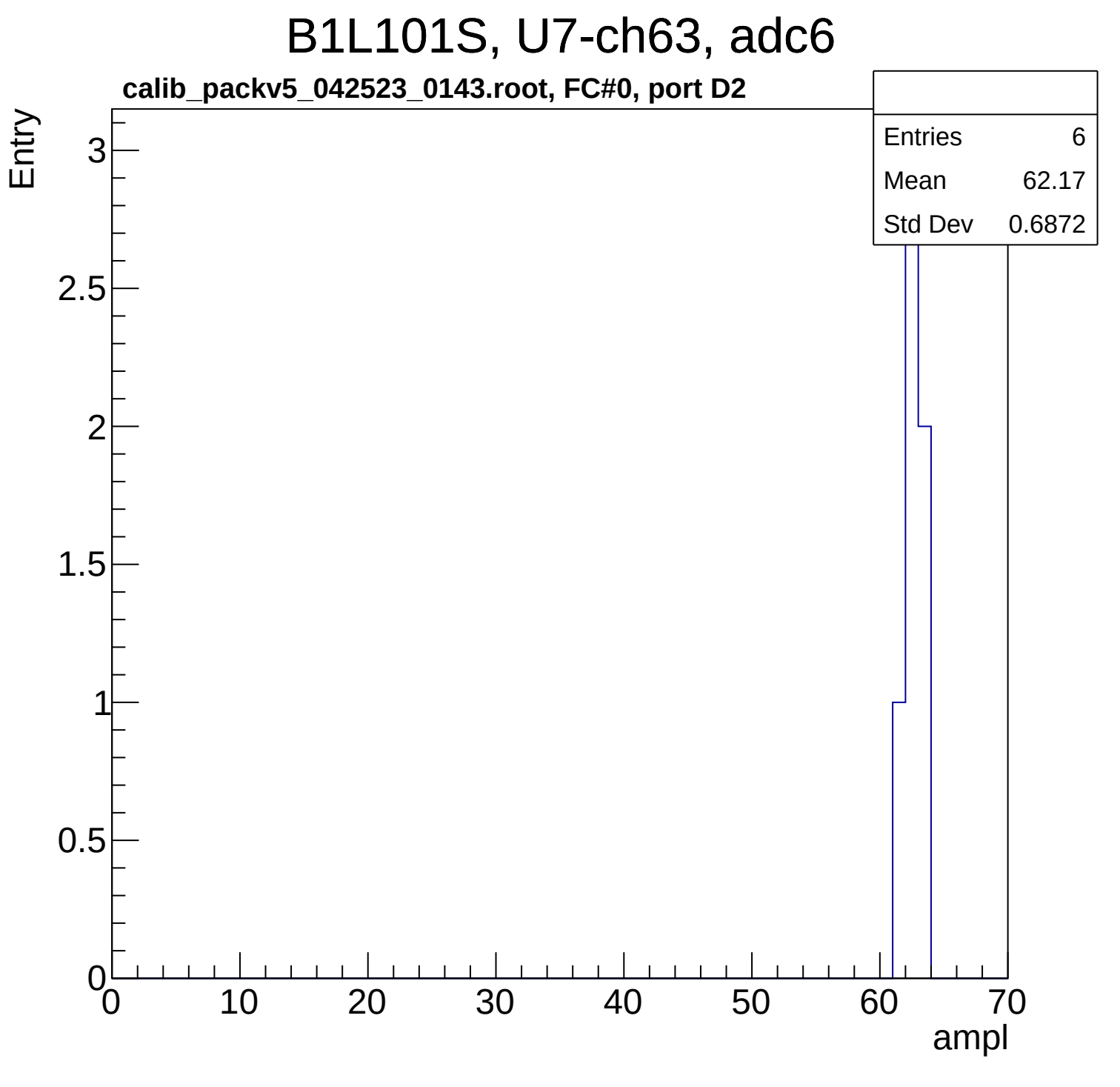
B1L101S, U7-ch63, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 62.17
Std Dev 0.6872
Entry
ampl
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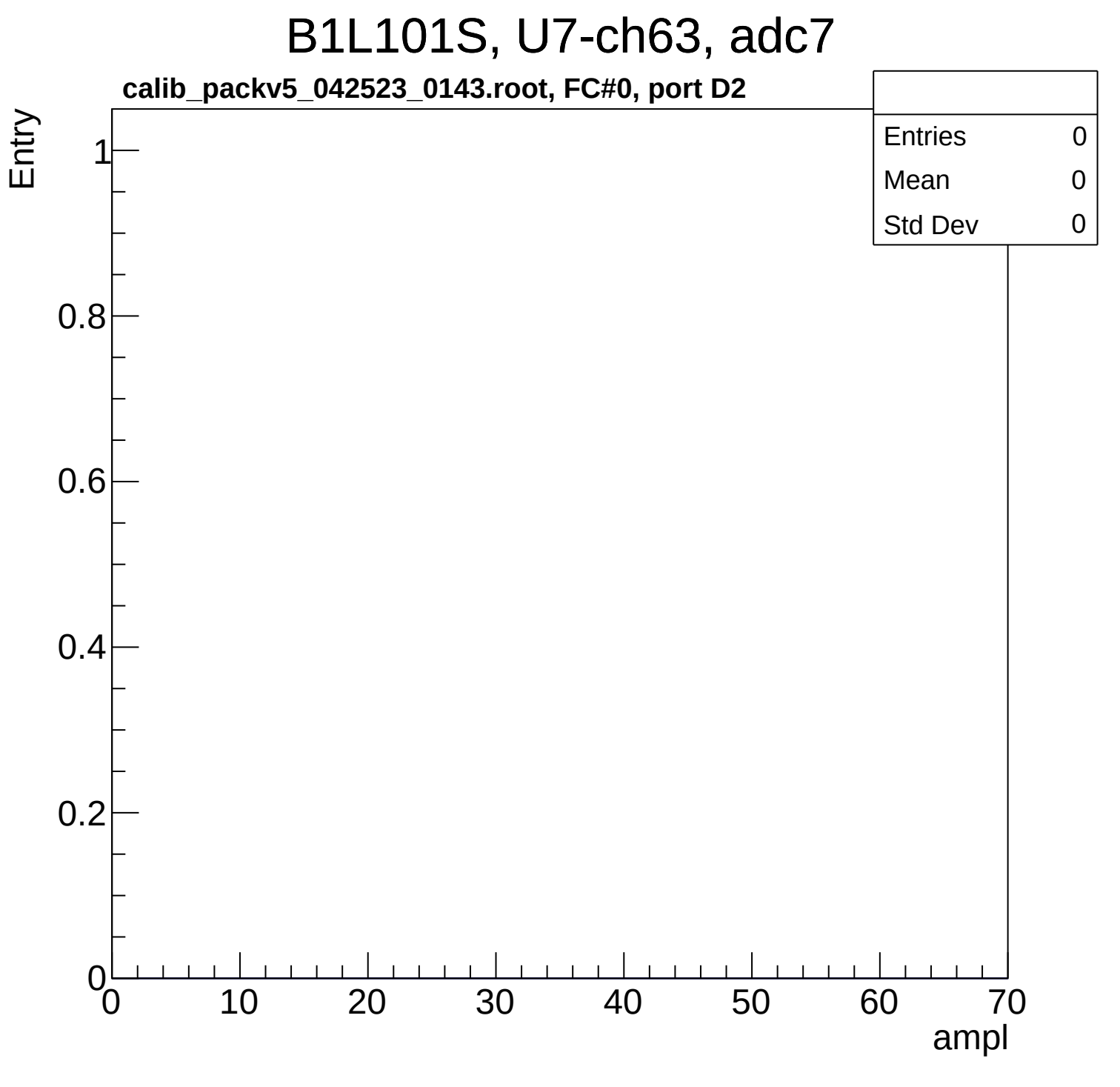
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U7-ch63, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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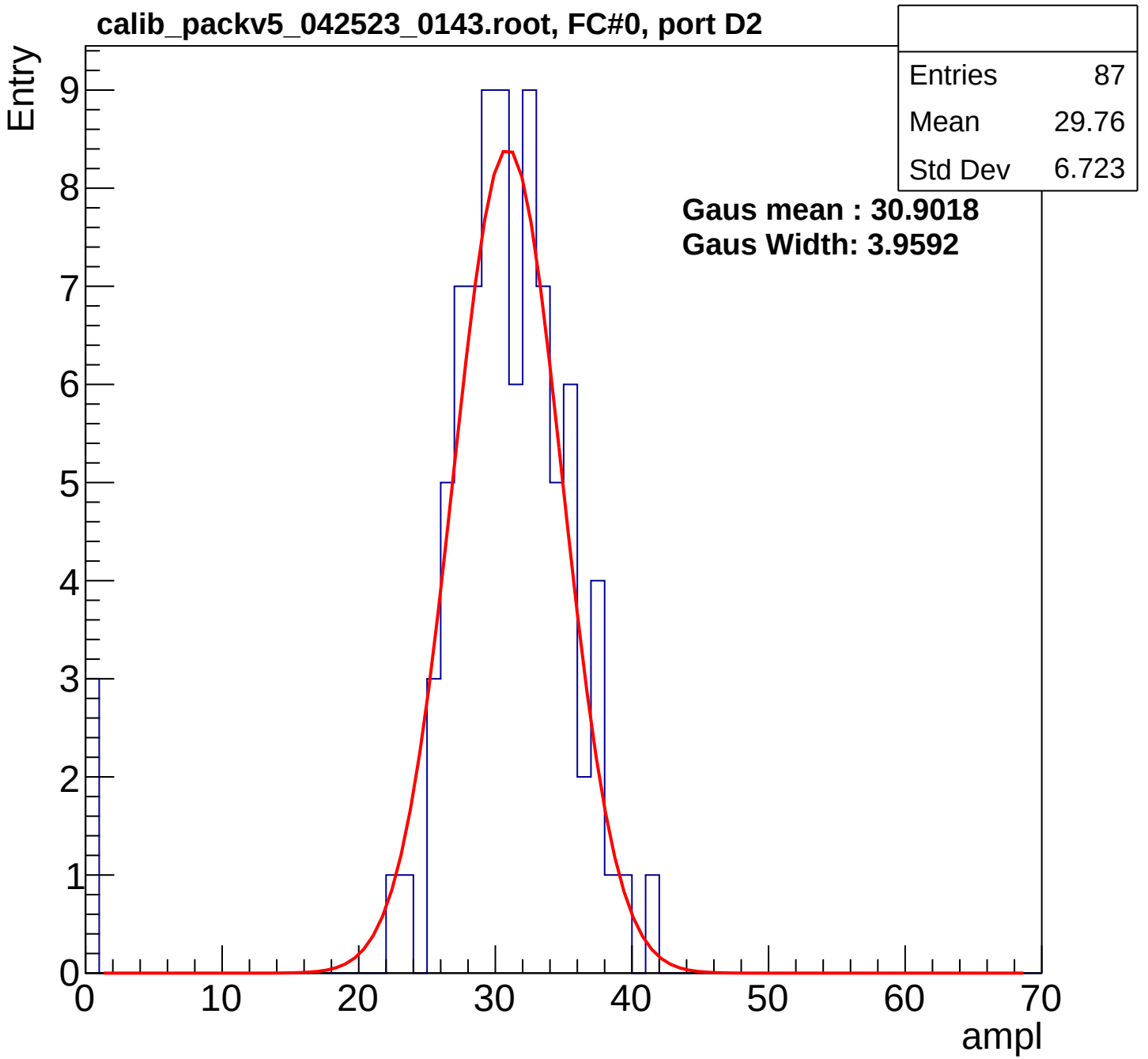
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch64, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 87
Mean 29.76
Std Dev 6.723
Gaus mean : 30.9018
Gaus Width: 3.9592
Entry
ampl
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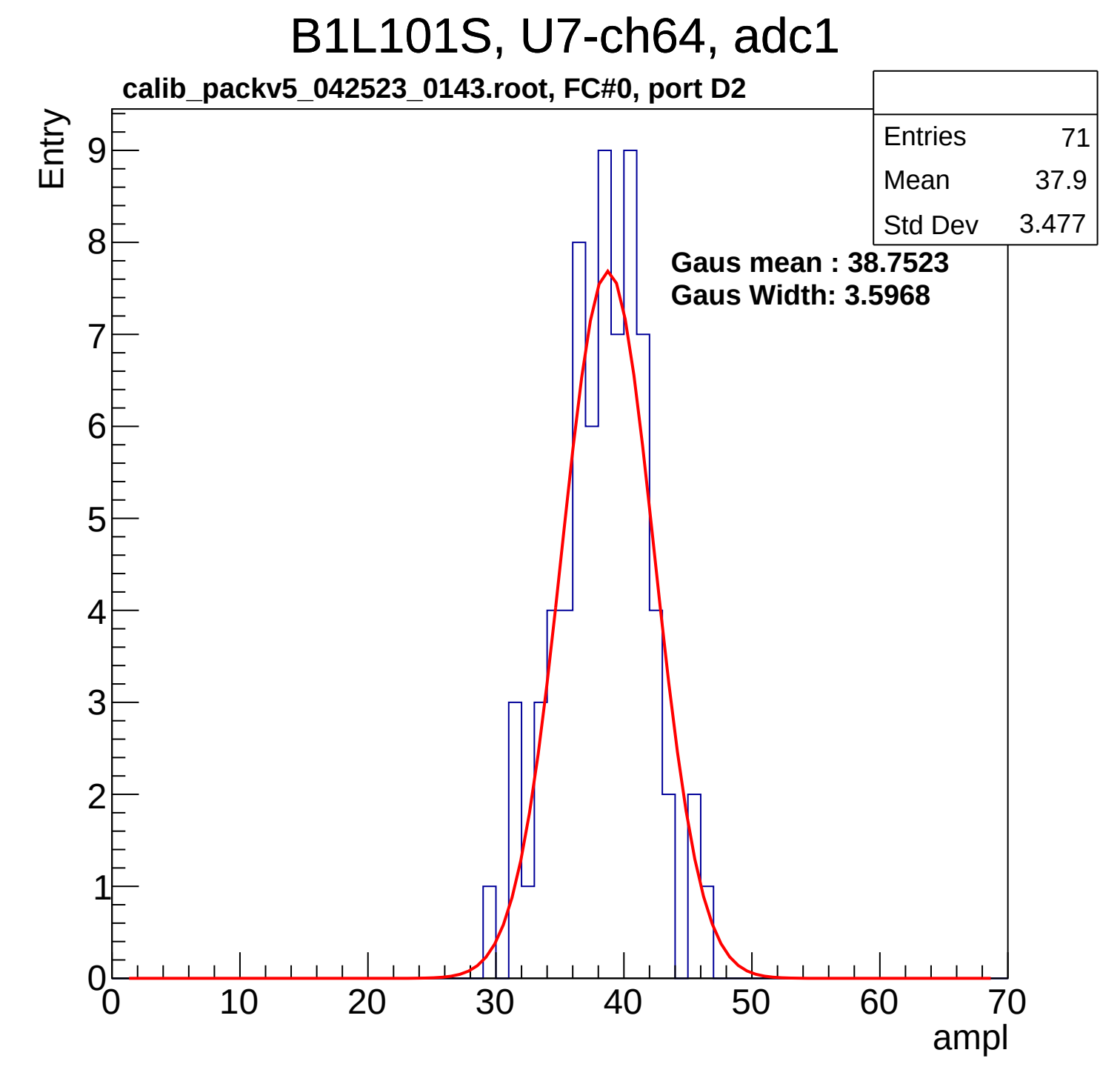
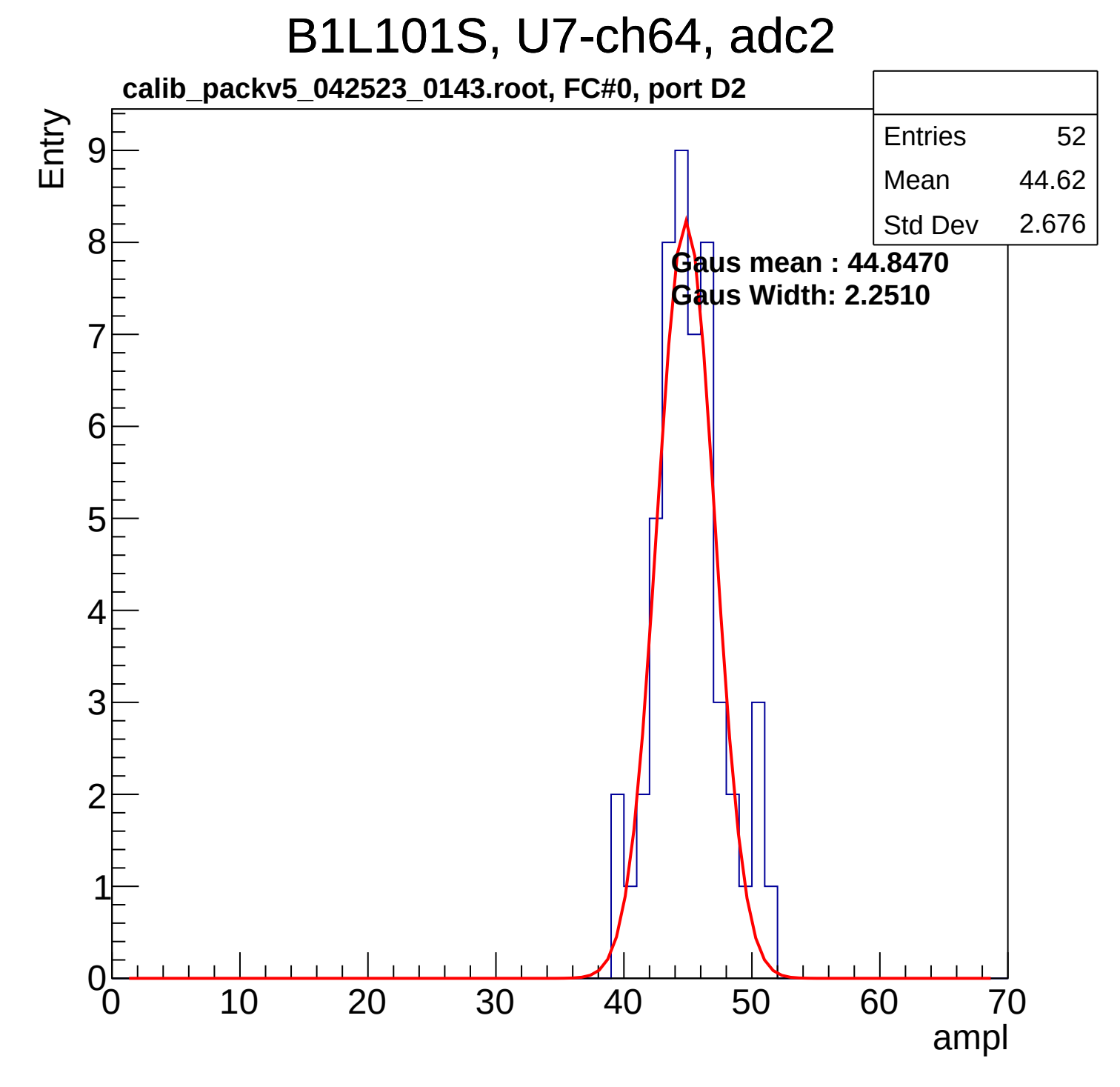
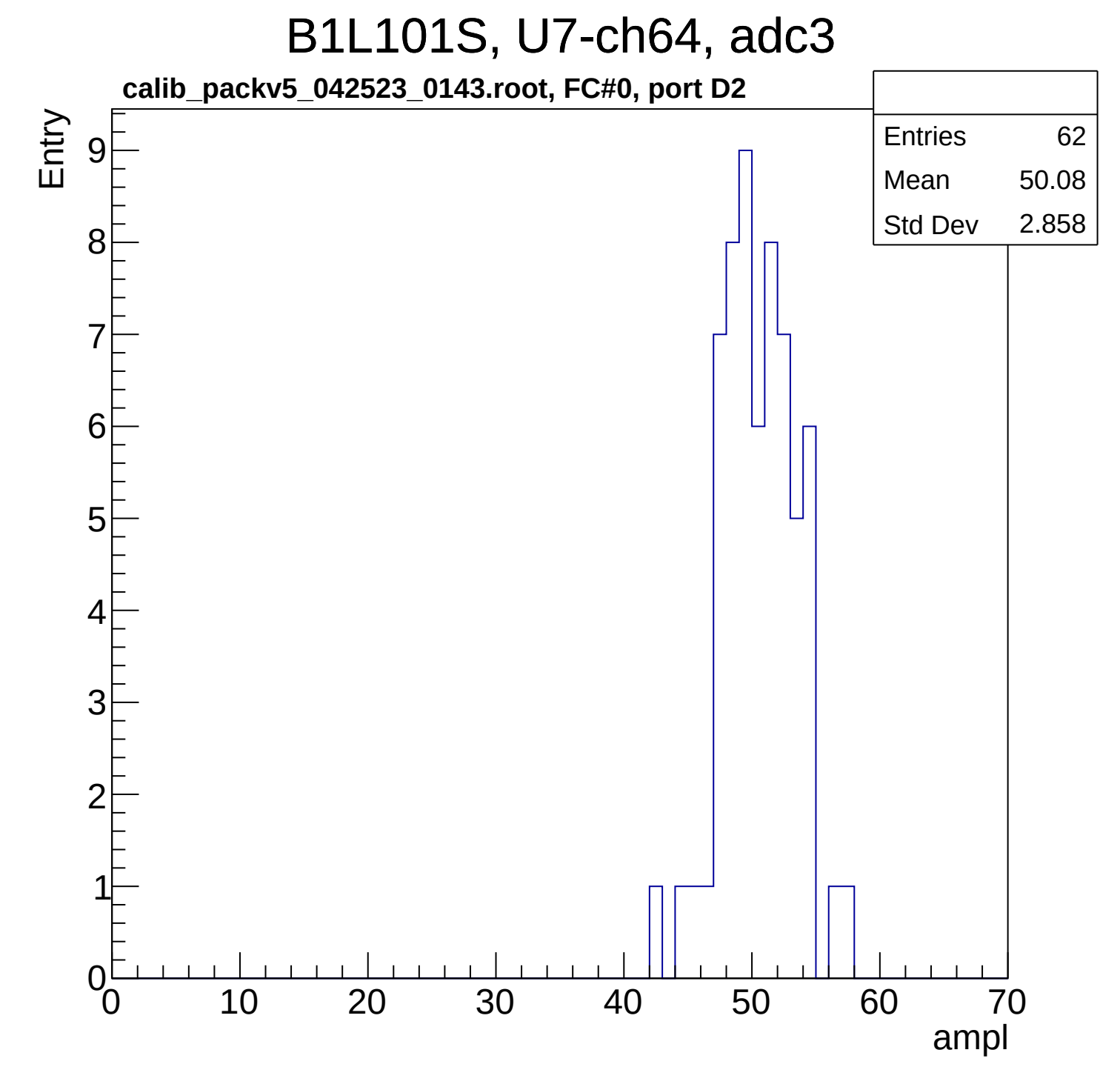
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch64, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 37.9
Std Dev 3.477
Gaus mean : 38.7523
Gaus Width: 3.5968
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch64, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 44.62
Std Dev 2.676
Gaus mean : 44.8470
Gaus Width: 2.2510
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch64, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 50.08
Std Dev 2.858
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
50
60
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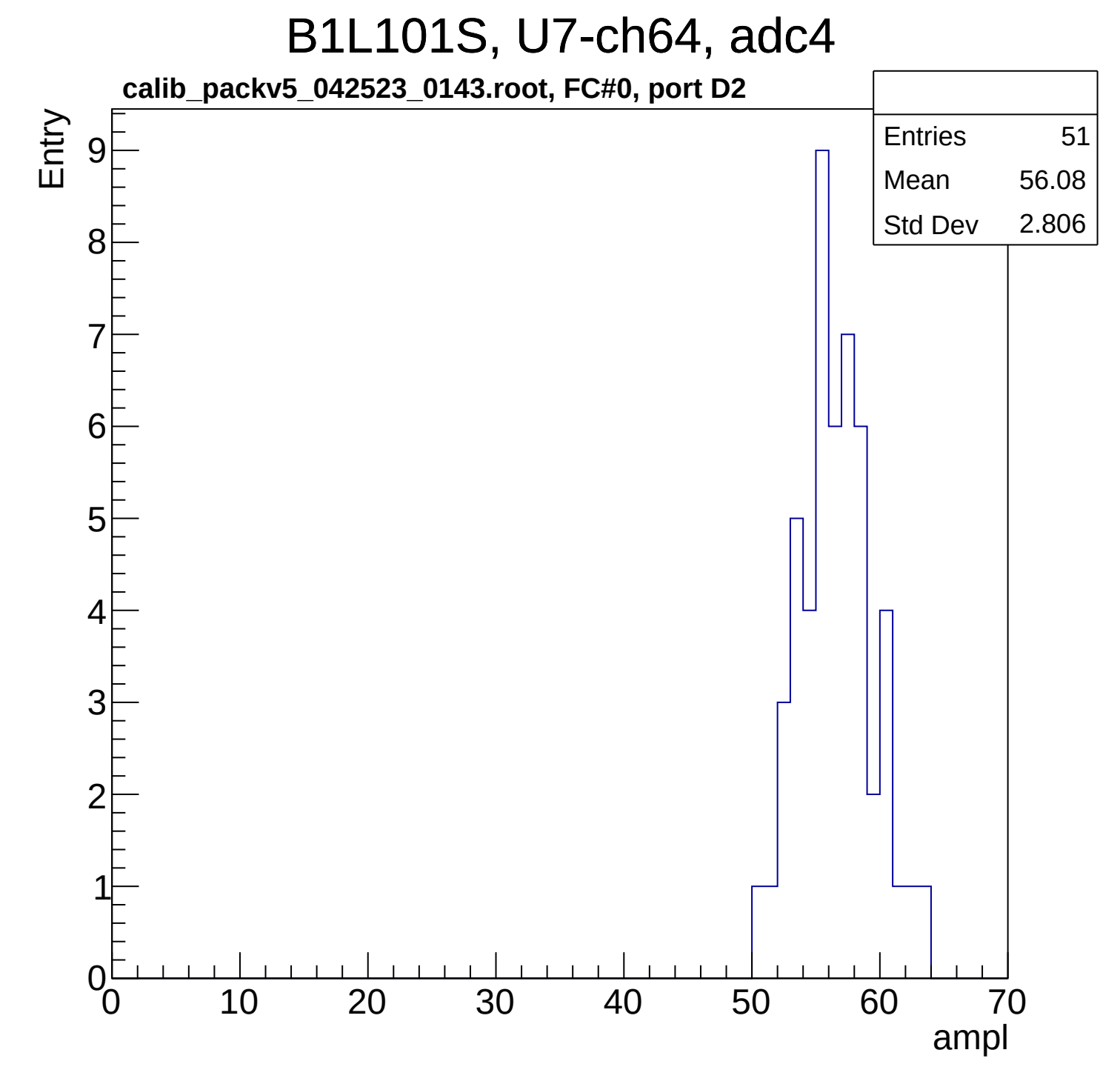
B1L101S, U7-ch64, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 56.08
Std Dev 2.806
Entry
ampl
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3
4
5
6
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8
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0
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60
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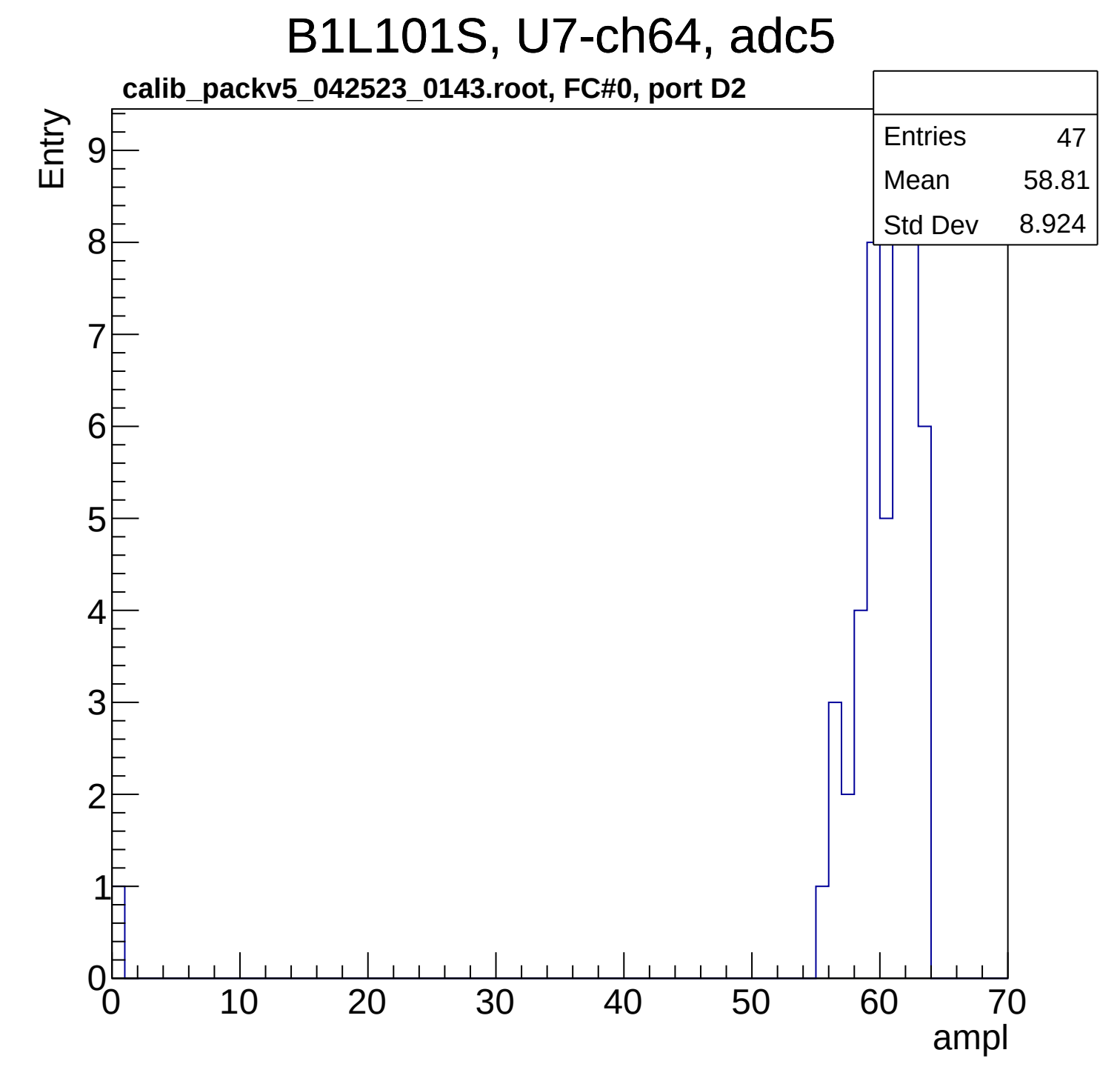
B1L101S, U7-ch64, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 58.81
Std Dev 8.924
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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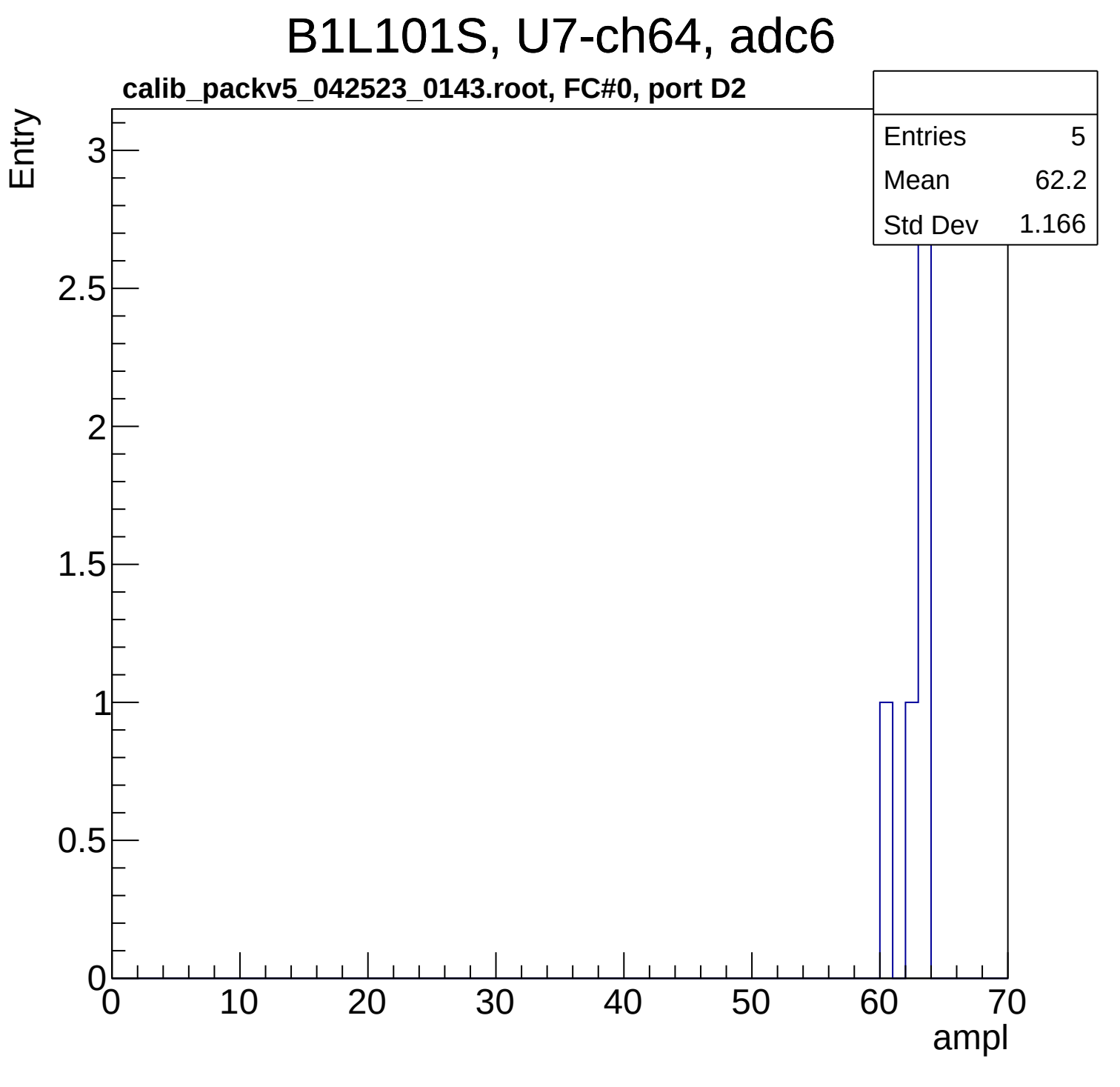
B1L101S, U7-ch64, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 62.2
Std Dev 1.166
Entry
ampl
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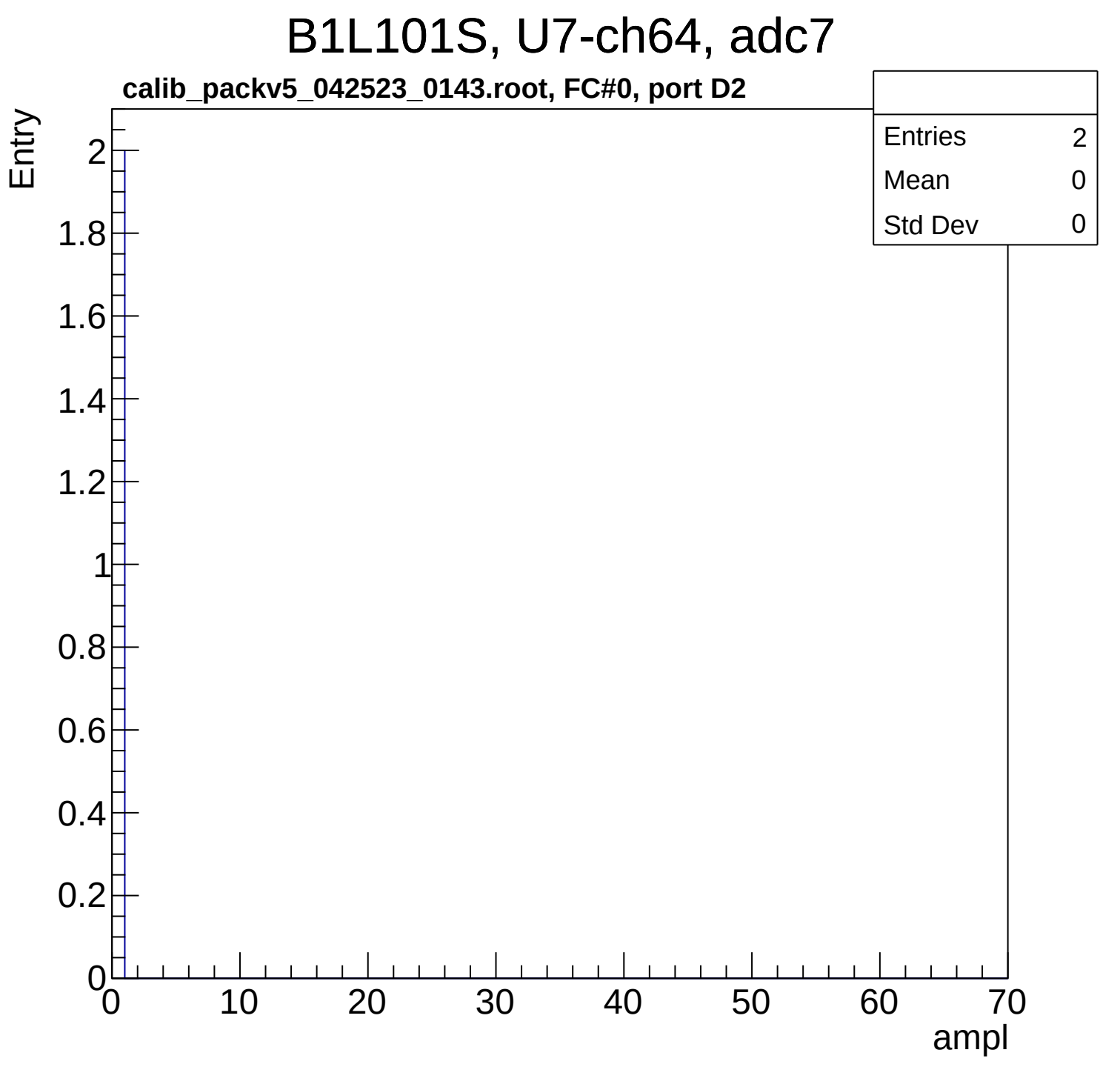
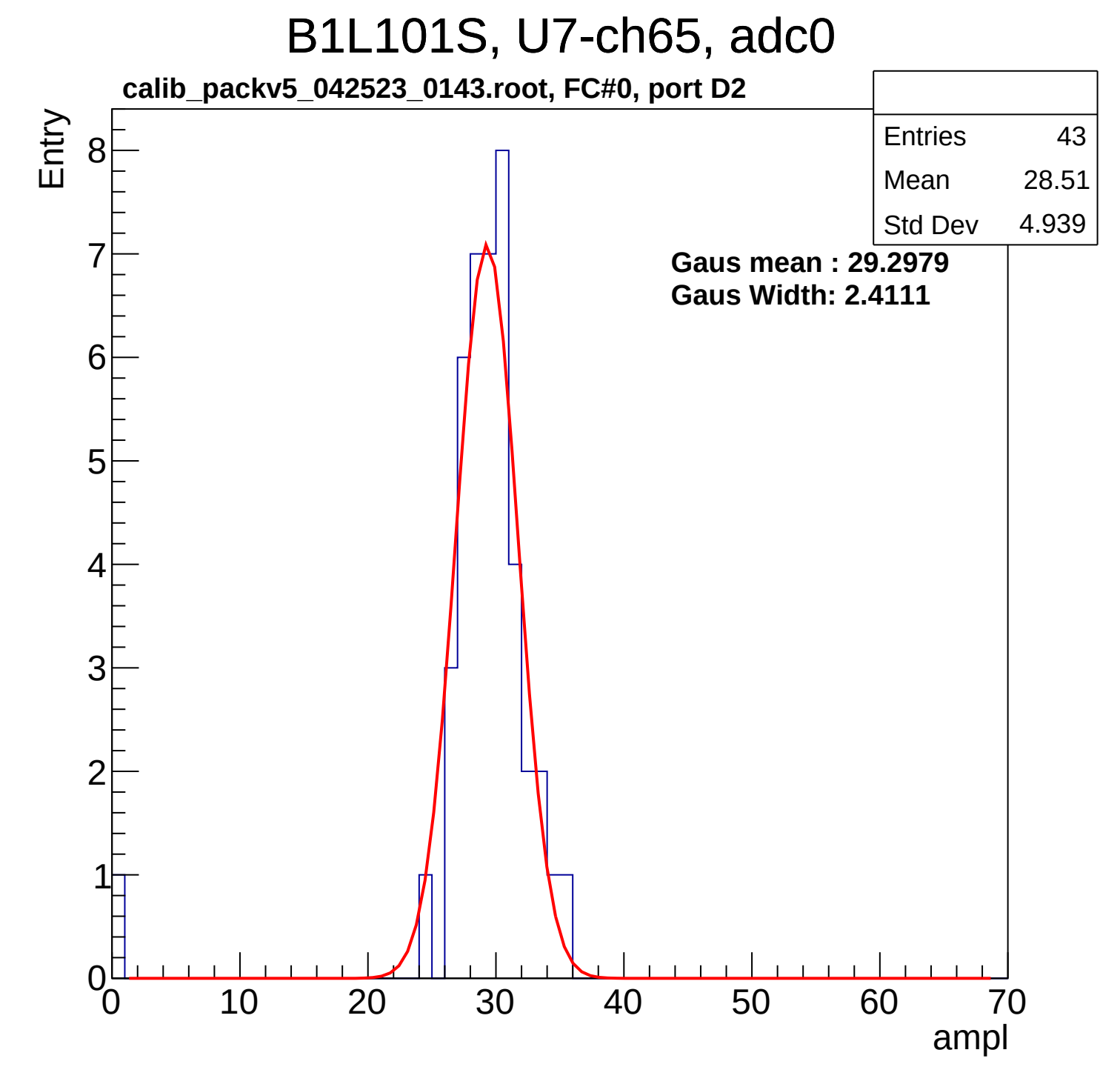
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U7-ch64, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch65, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 43
Mean 28.51
Std Dev 4.939
Gaus mean : 29.2979
Gaus Width: 2.4111
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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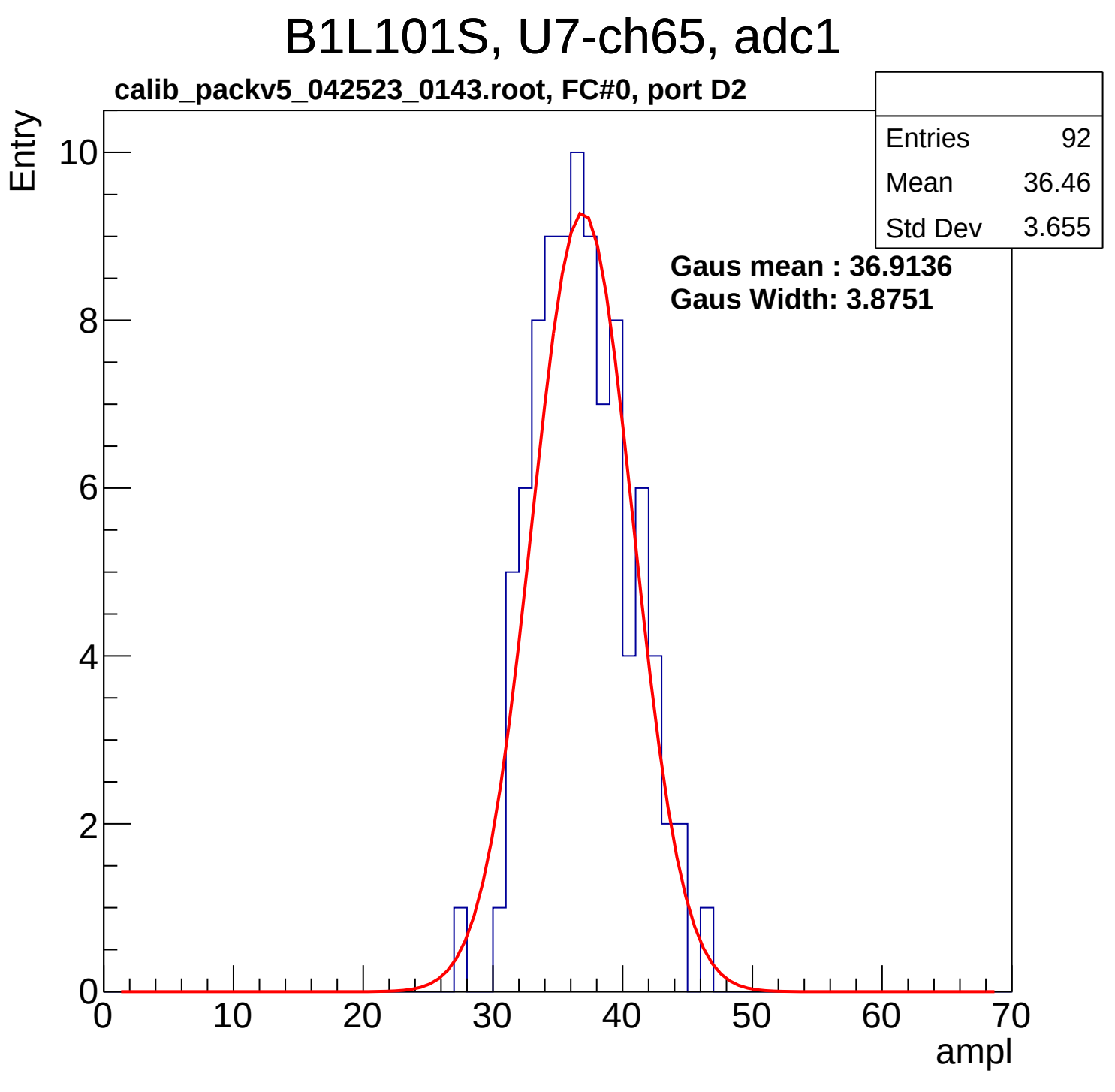
B1L101S, U7-ch65, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 92
Mean 36.46
Std Dev 3.655
Gaus mean : 36.9136
Gaus Width: 3.8751
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
50
60
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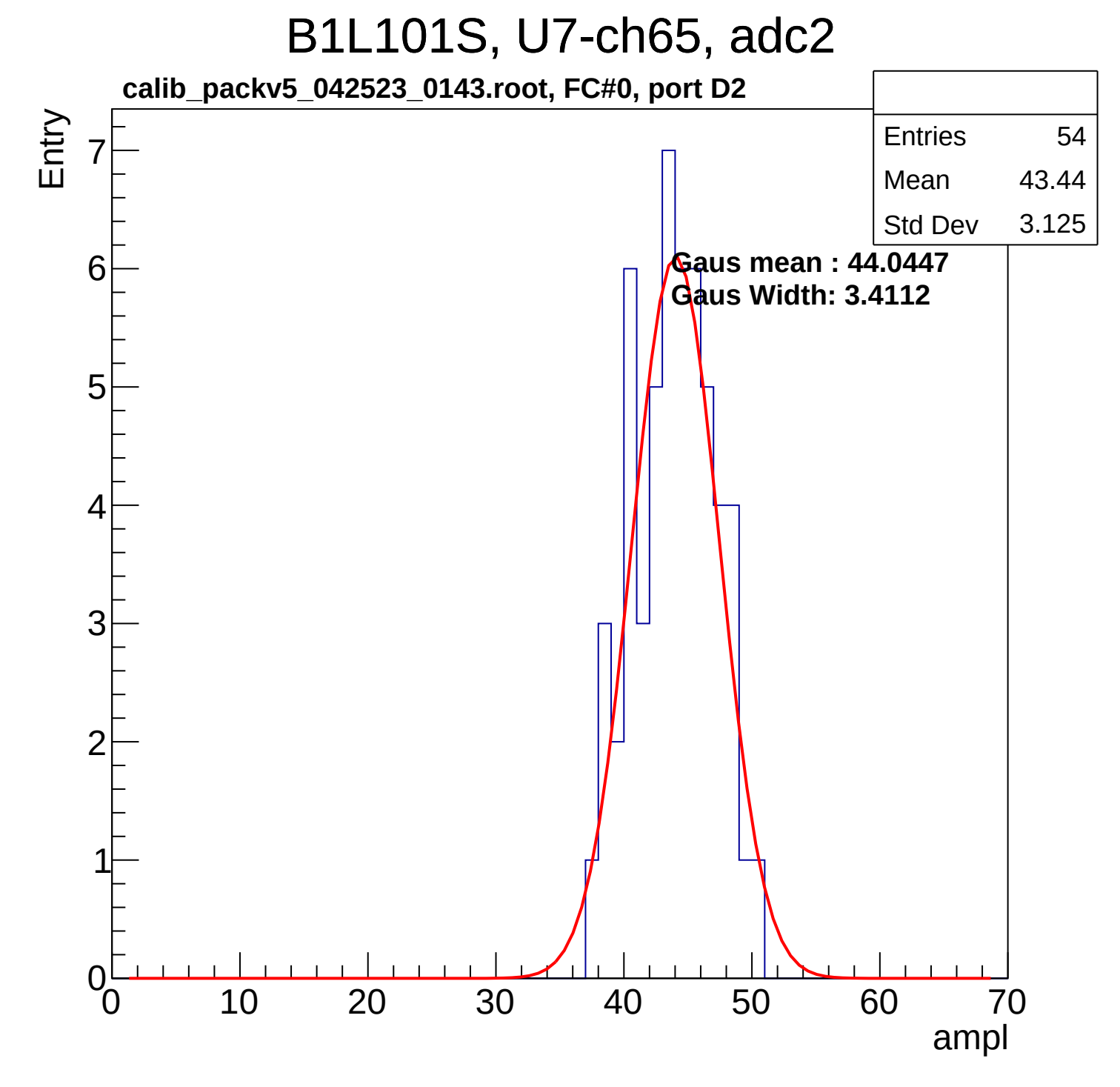
B1L101S, U7-ch65, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 43.44
Std Dev 3.125
Gaus mean : 44.0447
Gaus Width: 3.4112
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
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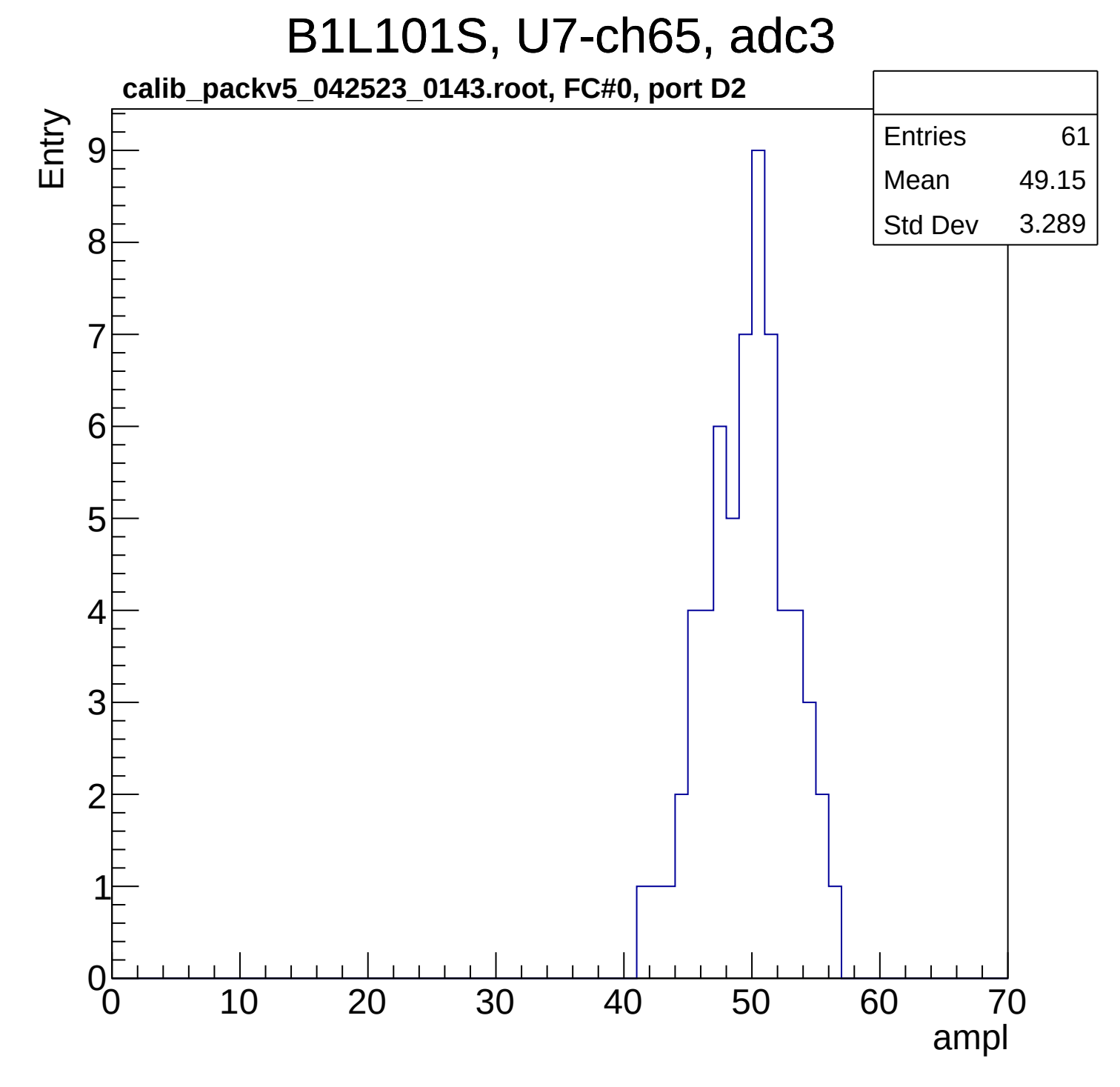
60
70


B1L101S, U7-ch65, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 49.15
Std Dev 3.289
Entry
ampl
0
1
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6
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0
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60
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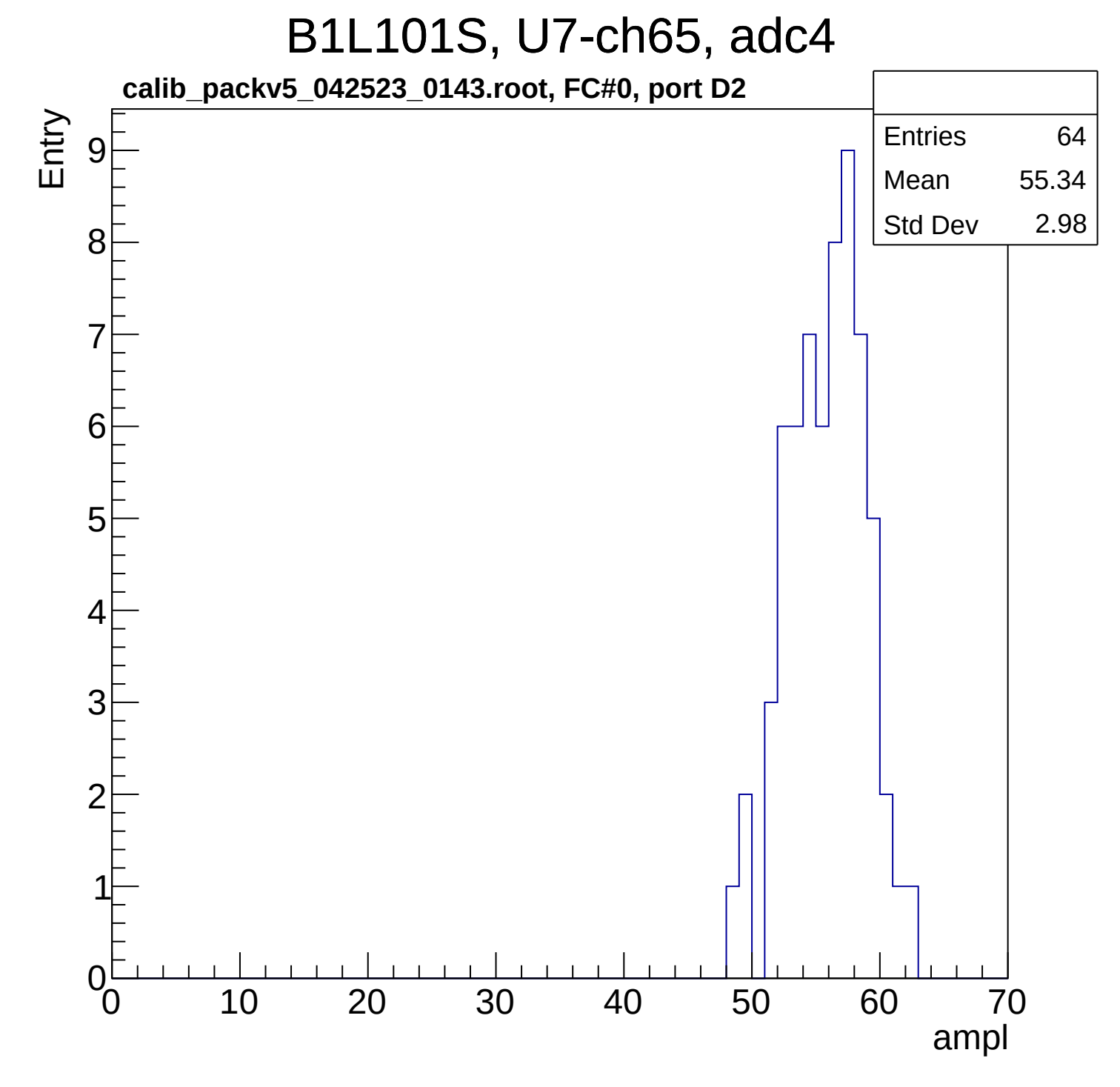
B1L101S, U7-ch65, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 55.34
Std Dev 2.98
Entry
ampl
0
1
2
3
4
5
6
7
8
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0
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20
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40
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60
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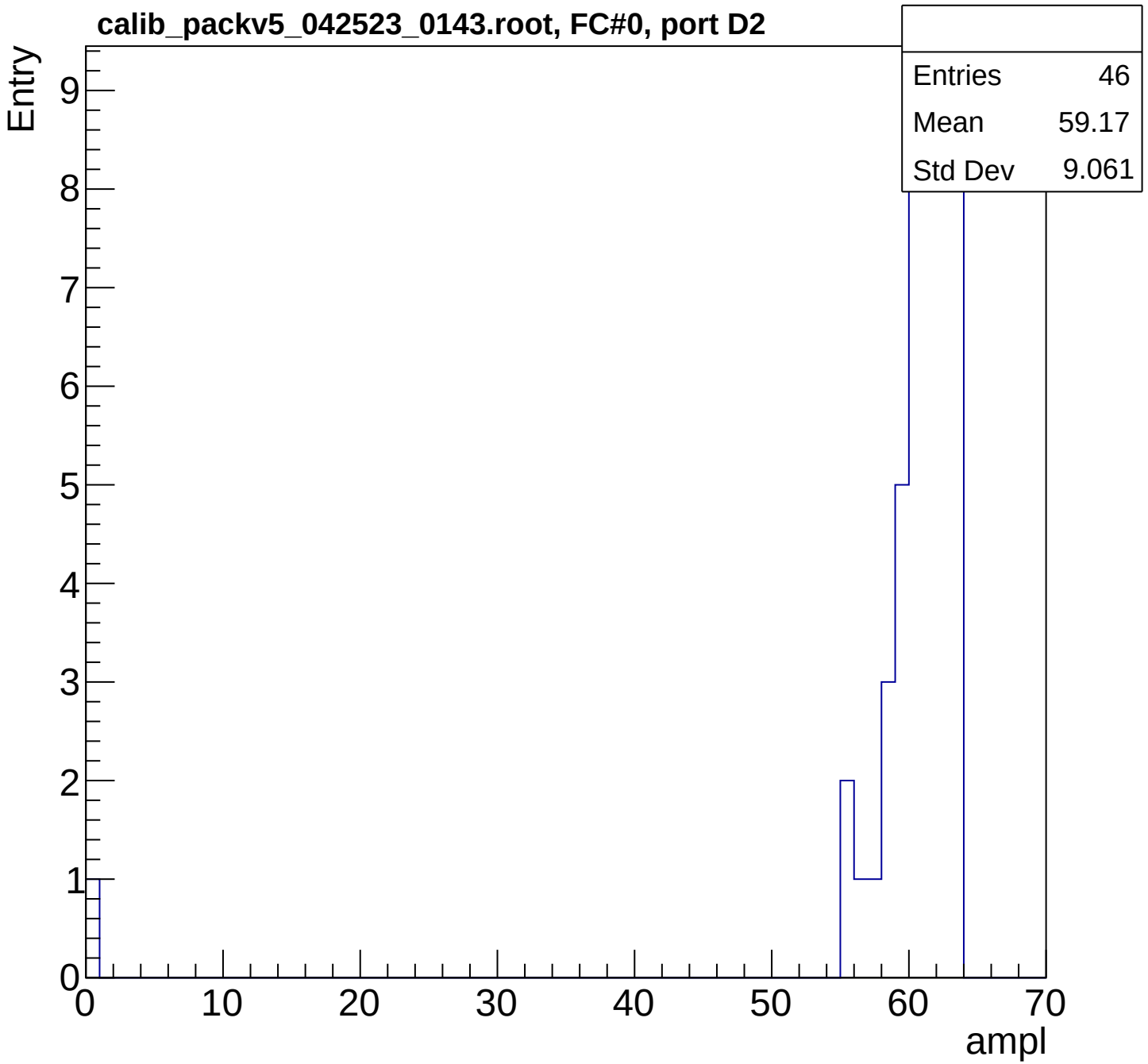
B1L101S, U7-ch65, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 59.17
Std Dev 9.061
Entry
ampl
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2
3
4
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6
7
8
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0
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40
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60
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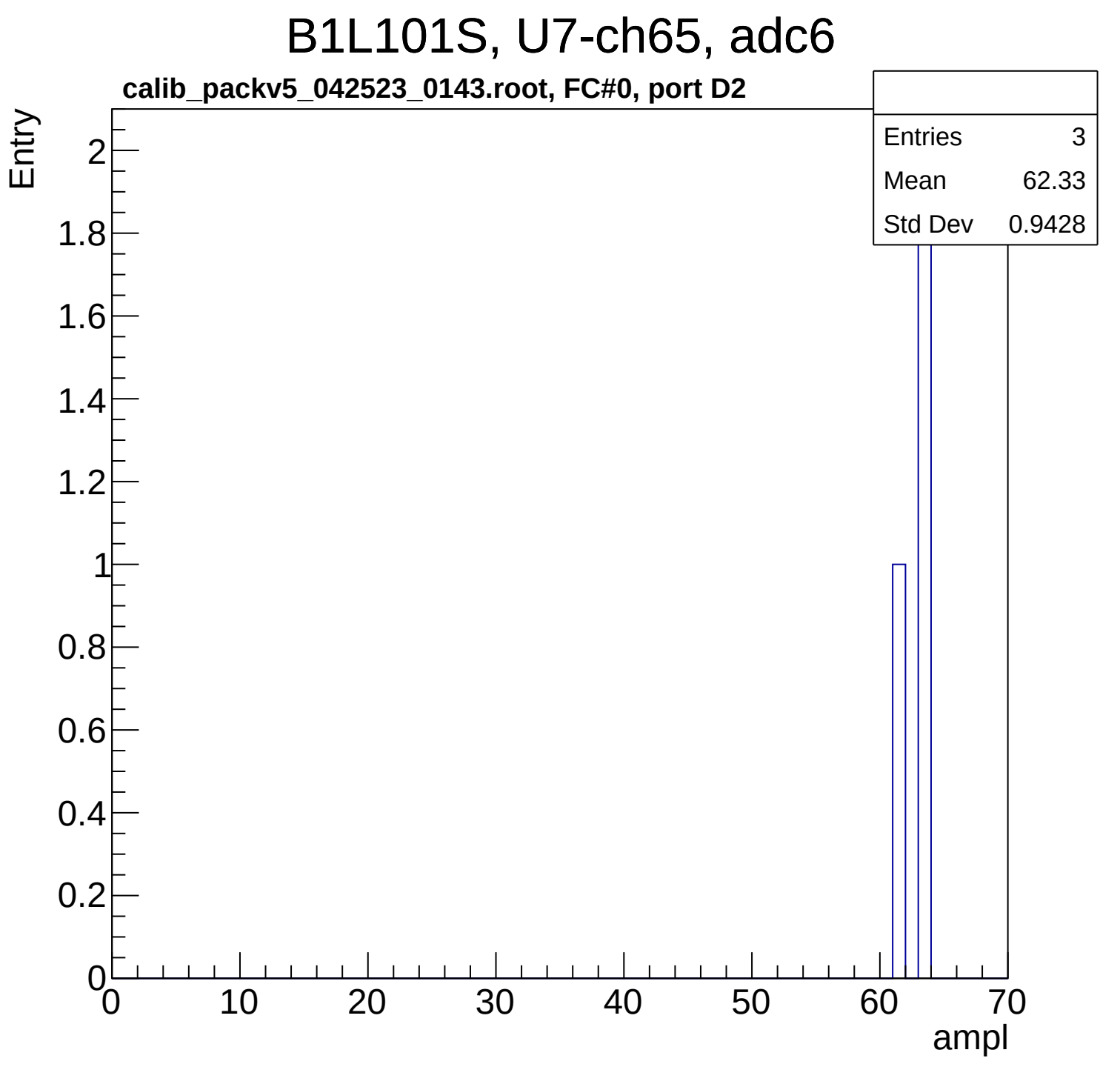
B1L101S, U7-ch65, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 62.33
Std Dev 0.9428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
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40
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60
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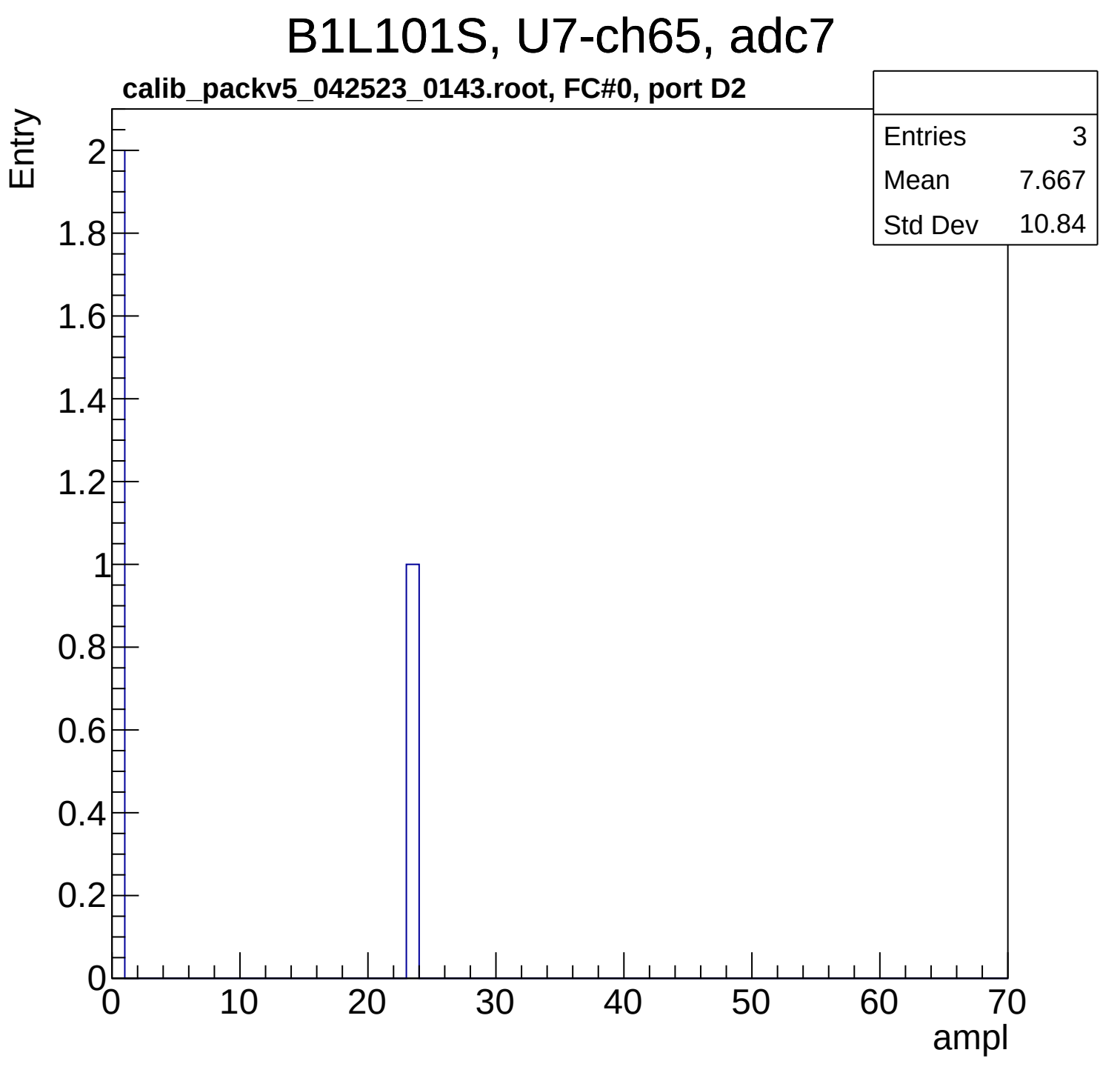
B1L101S, U7-ch65, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 7.667
Std Dev 10.84
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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20
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40
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60
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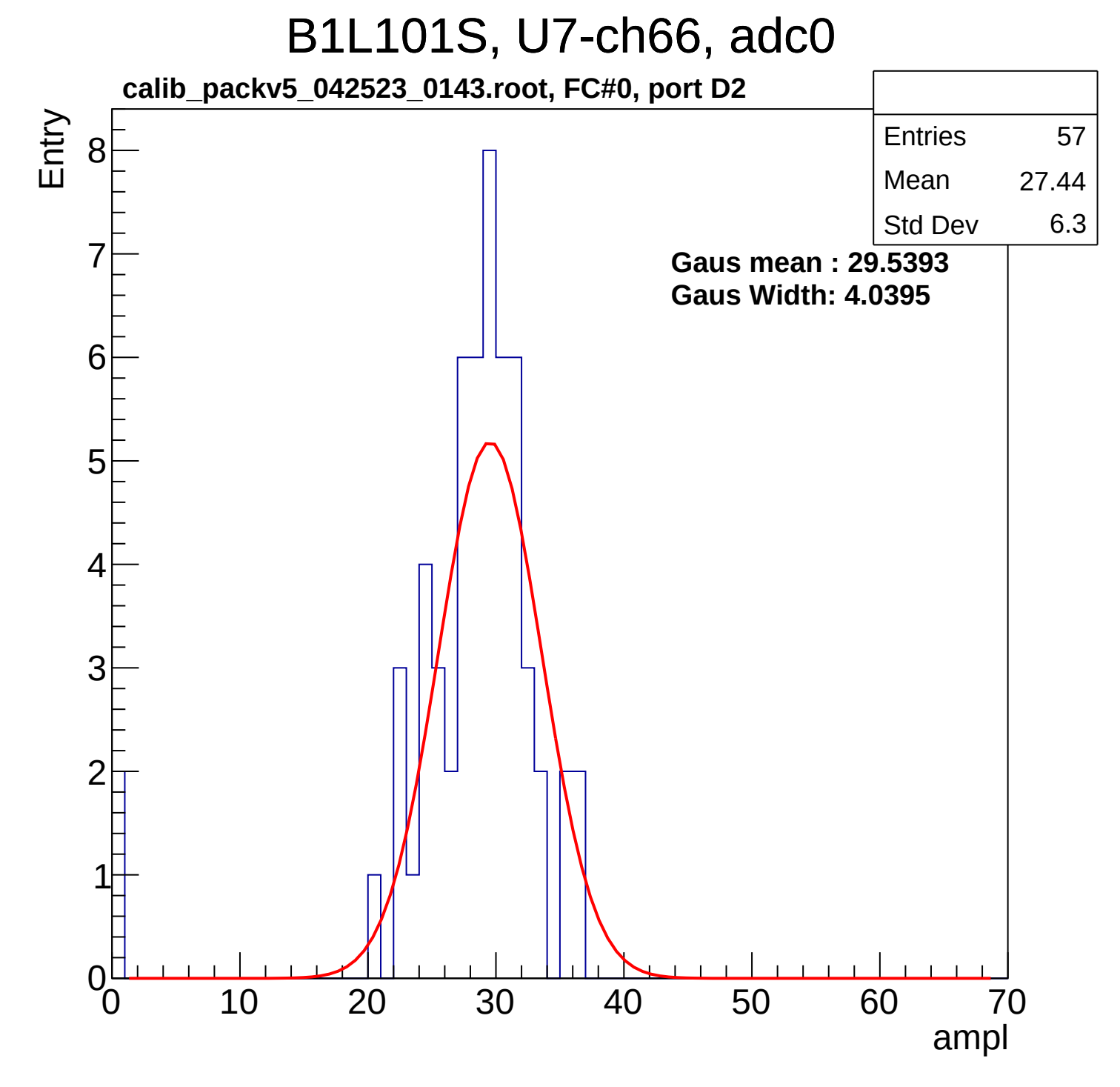
B1L101S, U7-ch66, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 27.44
Std Dev 6.3
Gaus mean : 29.5393
Gaus Width: 4.0395
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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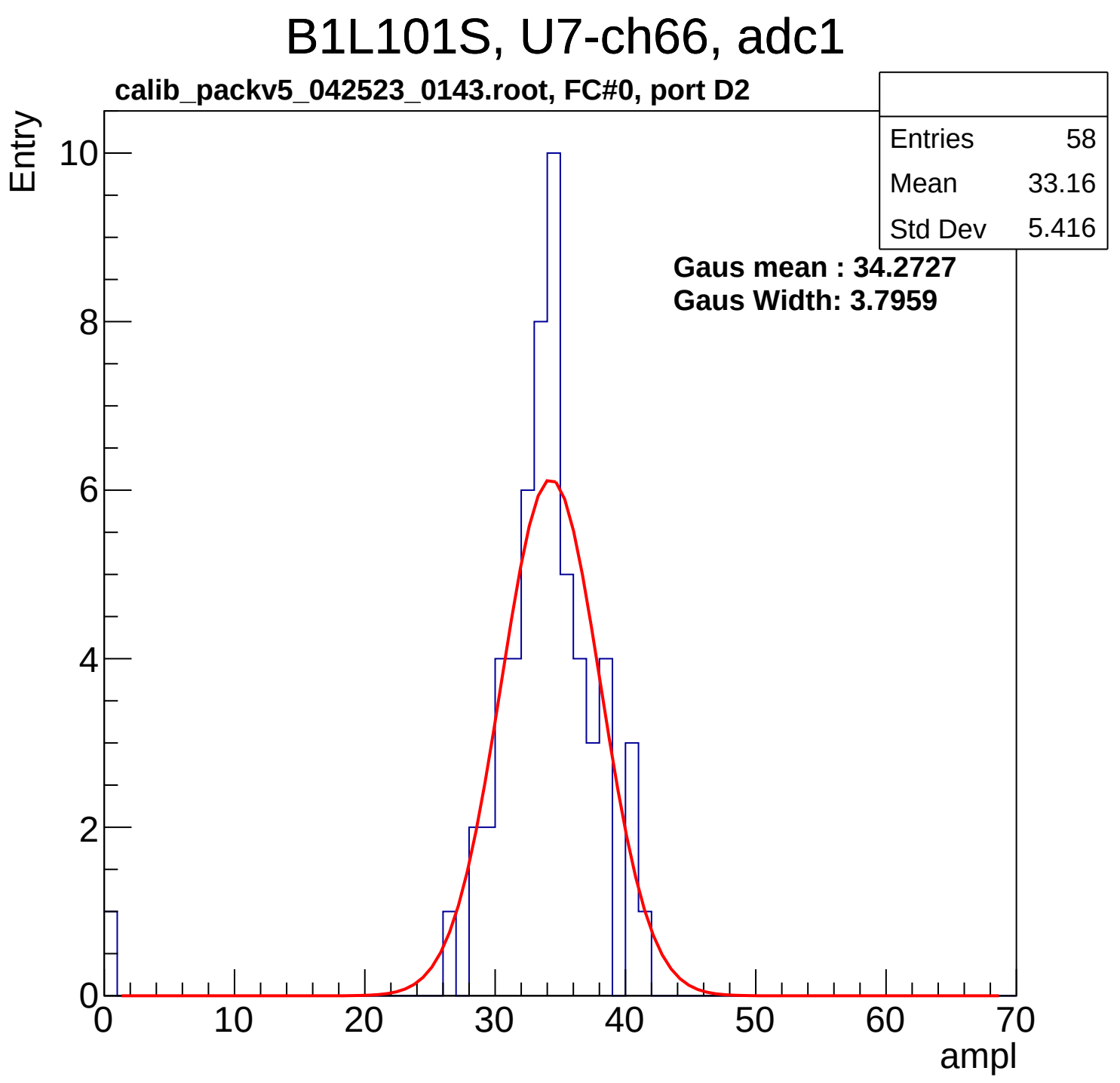
B1L101S, U7-ch66, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 33.16
Std Dev 5.416
Gaus mean : 34.2727
Gaus Width: 3.7959
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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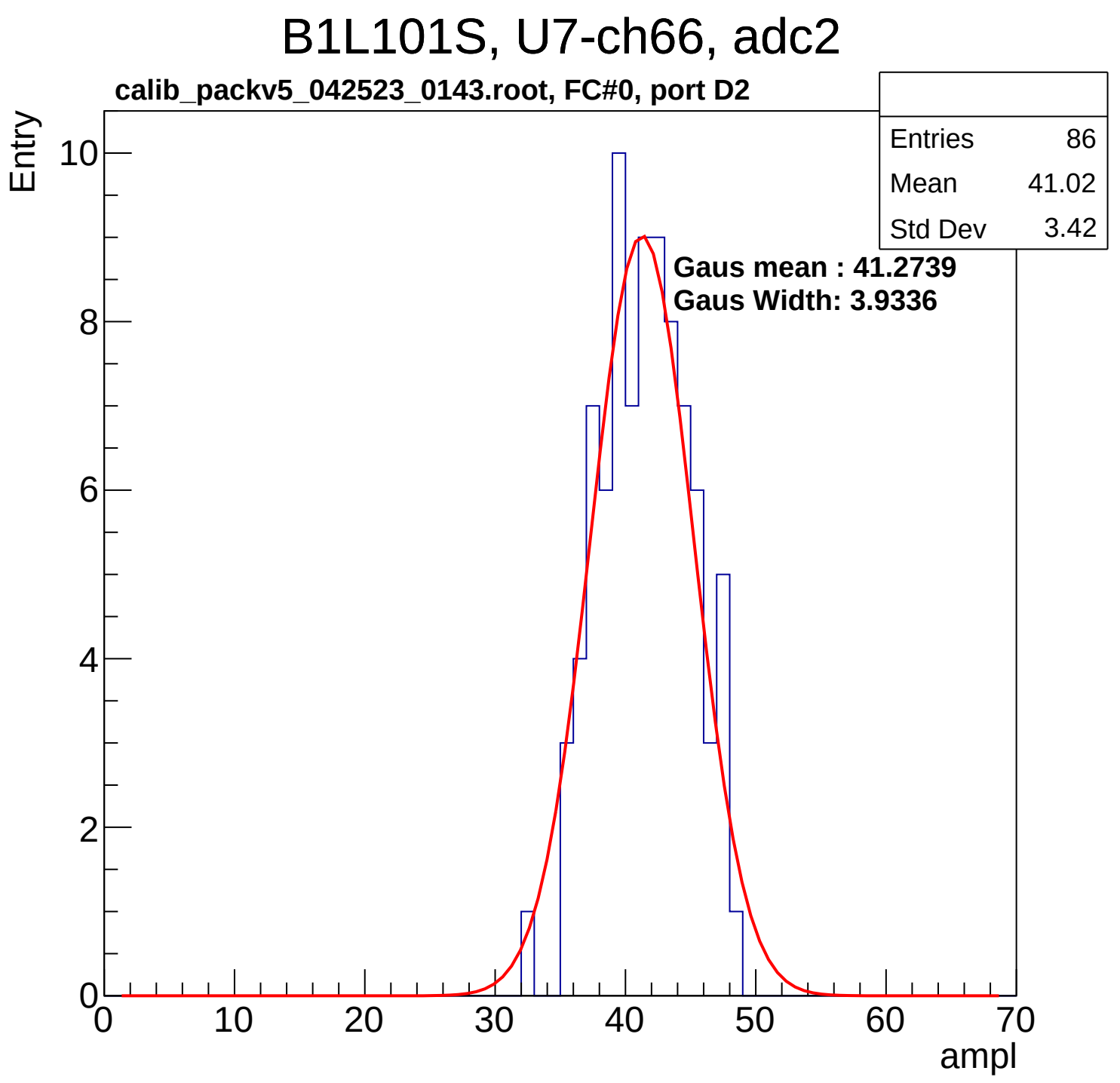
B1L101S, U7-ch66, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 86
Mean 41.02
Std Dev 3.42
Gaus mean : 41.2739
Gaus Width: 3.9336
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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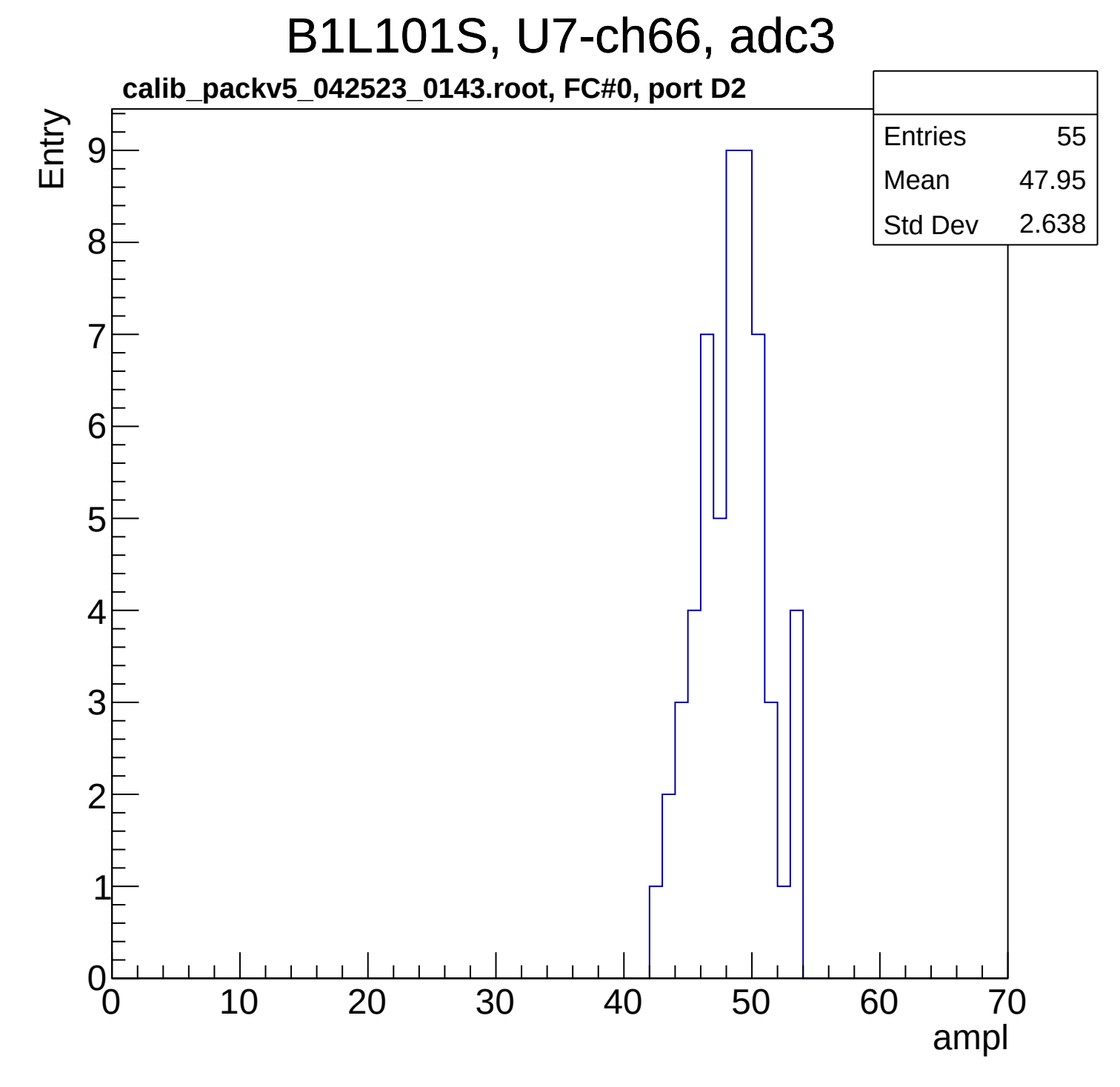
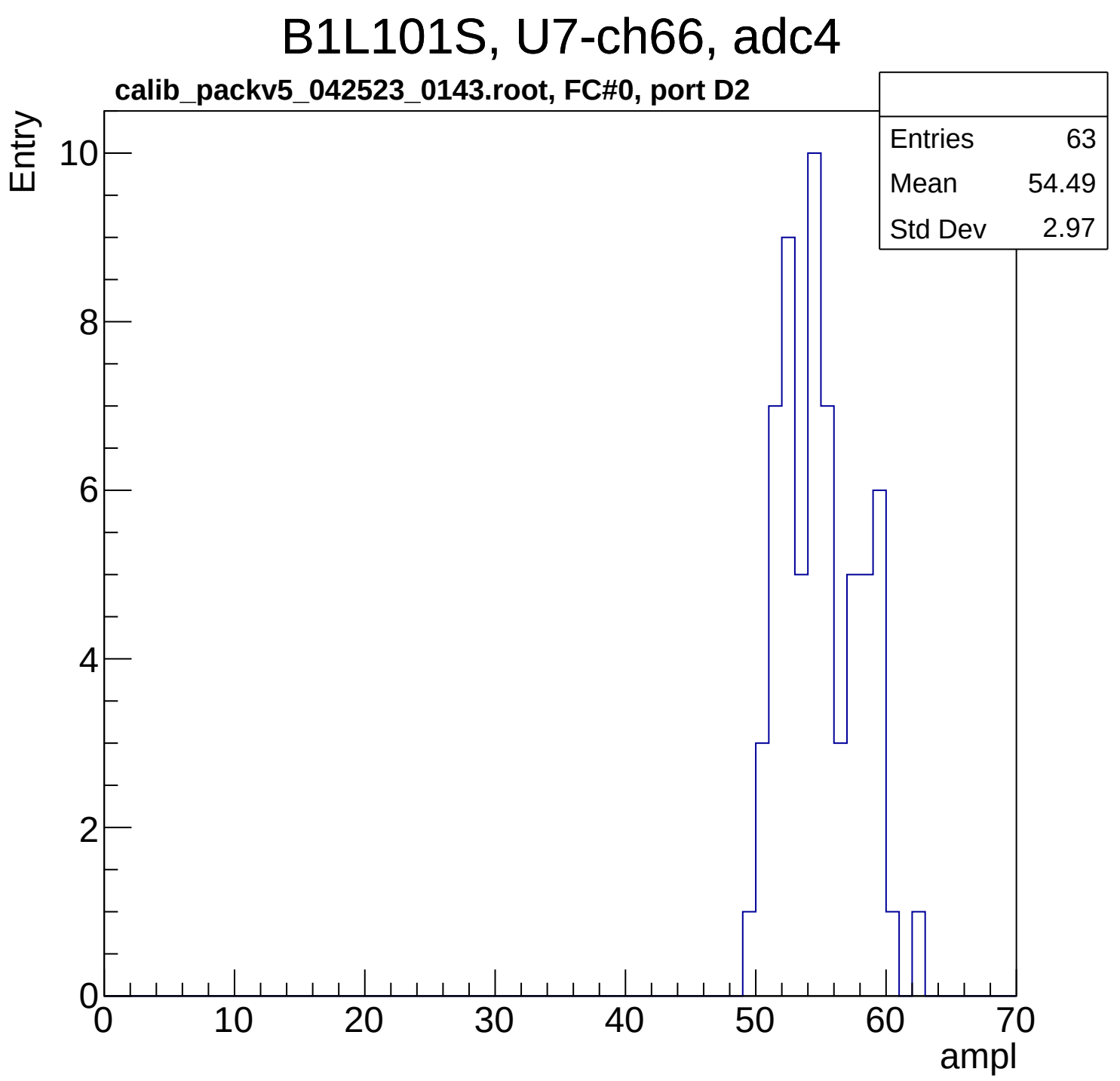
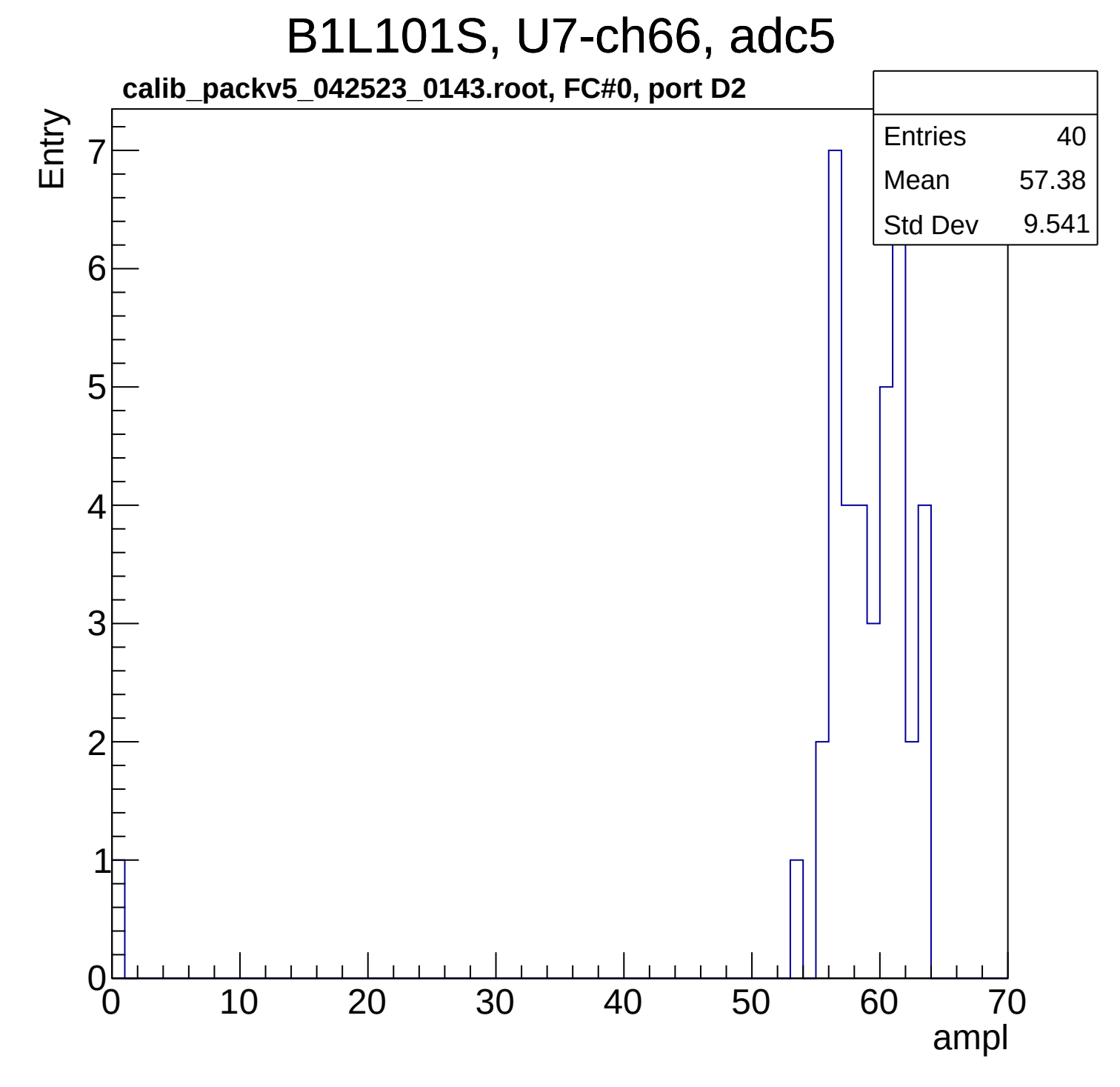

B1L101S, U7-ch66, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 47.95
Std Dev 2.638
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch66, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 54.49
Std Dev 2.97
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch66, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 40
Mean 57.38
Std Dev 9.541
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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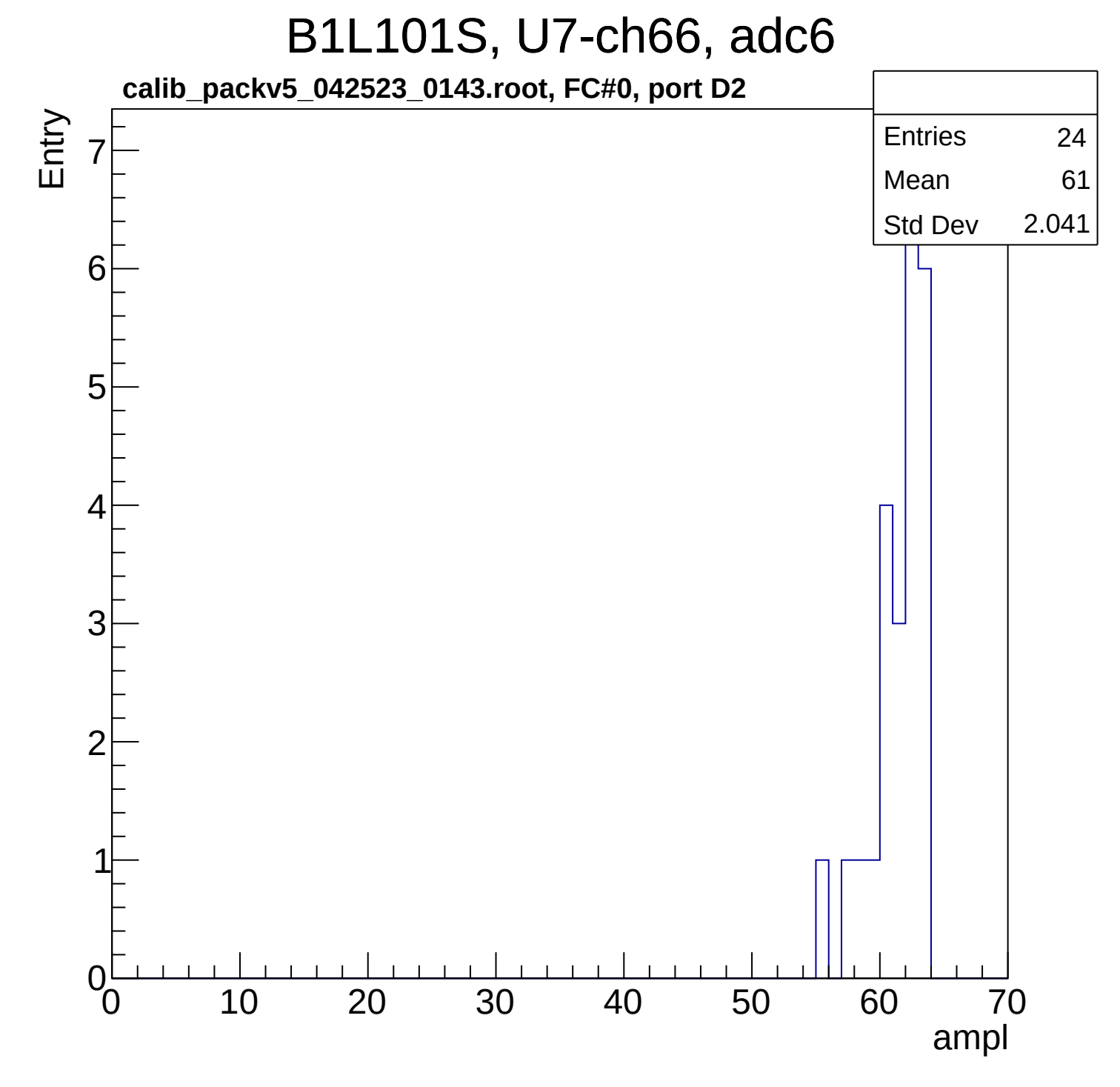
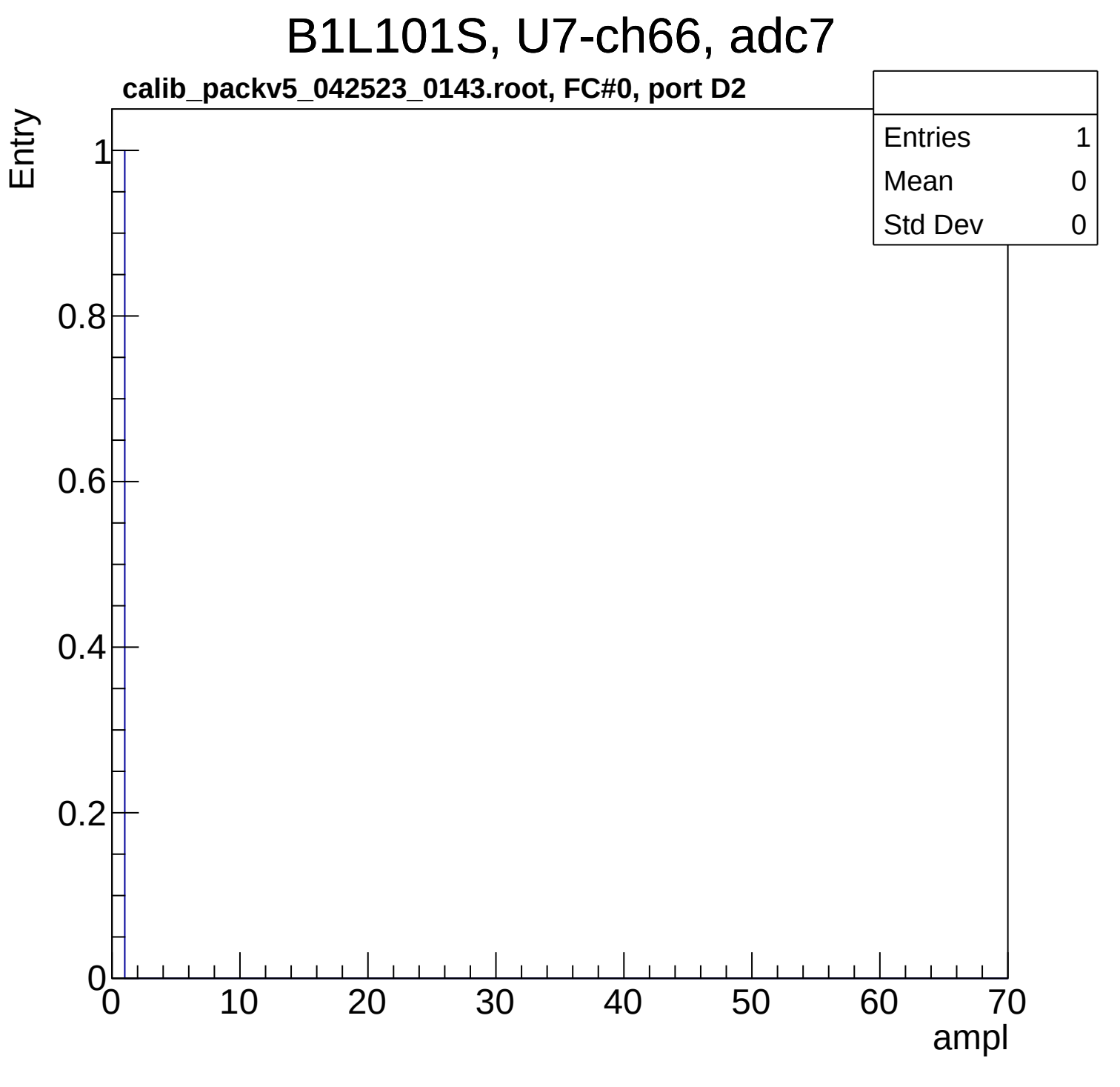
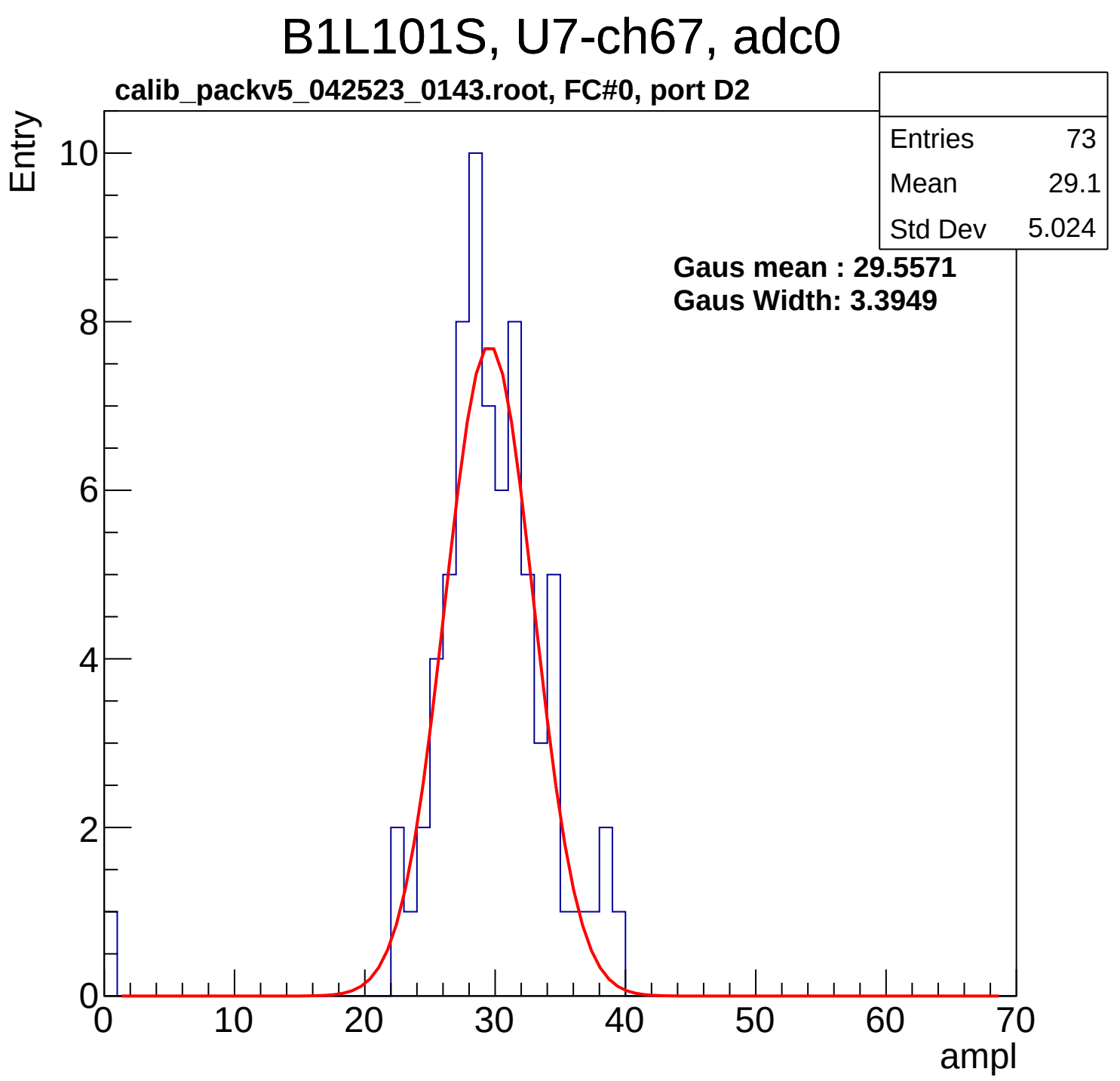
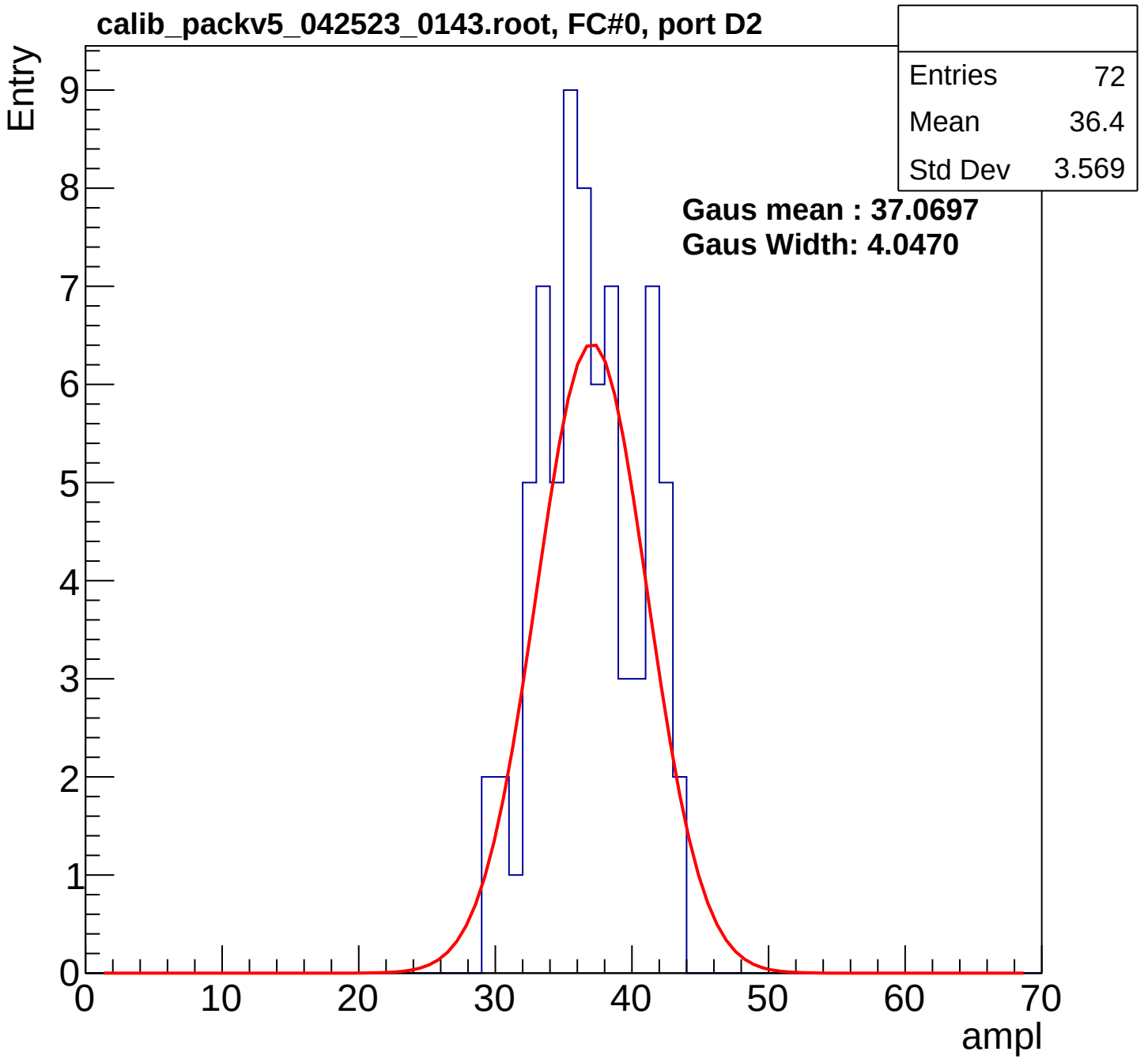
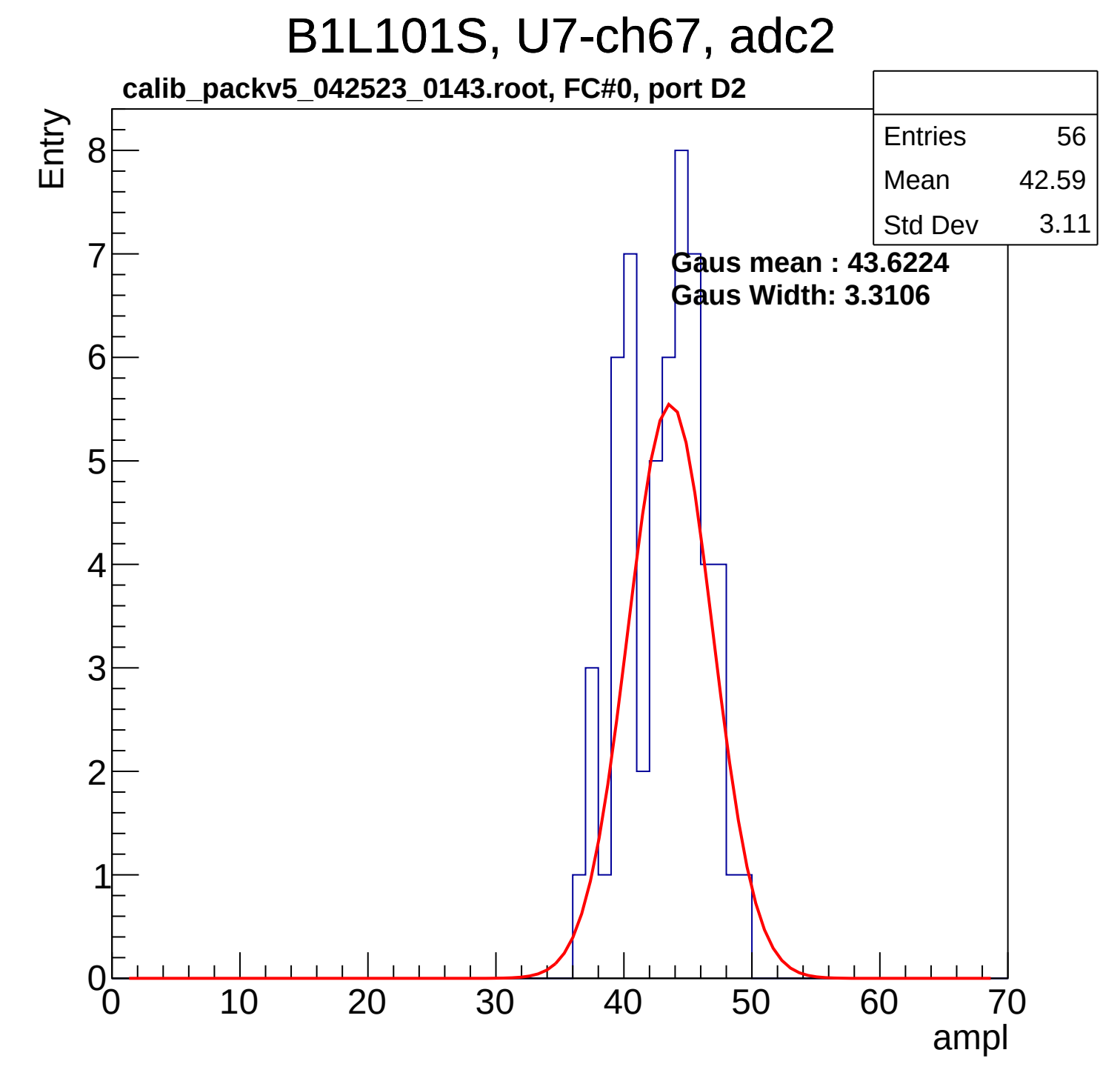

B1L101S, U7-ch66, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 24
Mean 61
Std Dev 2.041
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U7-ch66, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch67, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 29.1
Std Dev 5.024
Gaus mean : 29.5571
Gaus Width: 3.3949
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch67, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 36.4
Std Dev 3.569
Gaus mean : 37.0697
Gaus Width: 4.0470
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch67, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 42.59
Std Dev 3.11
Gaus mean : 43.6224
Gaus Width: 3.3106
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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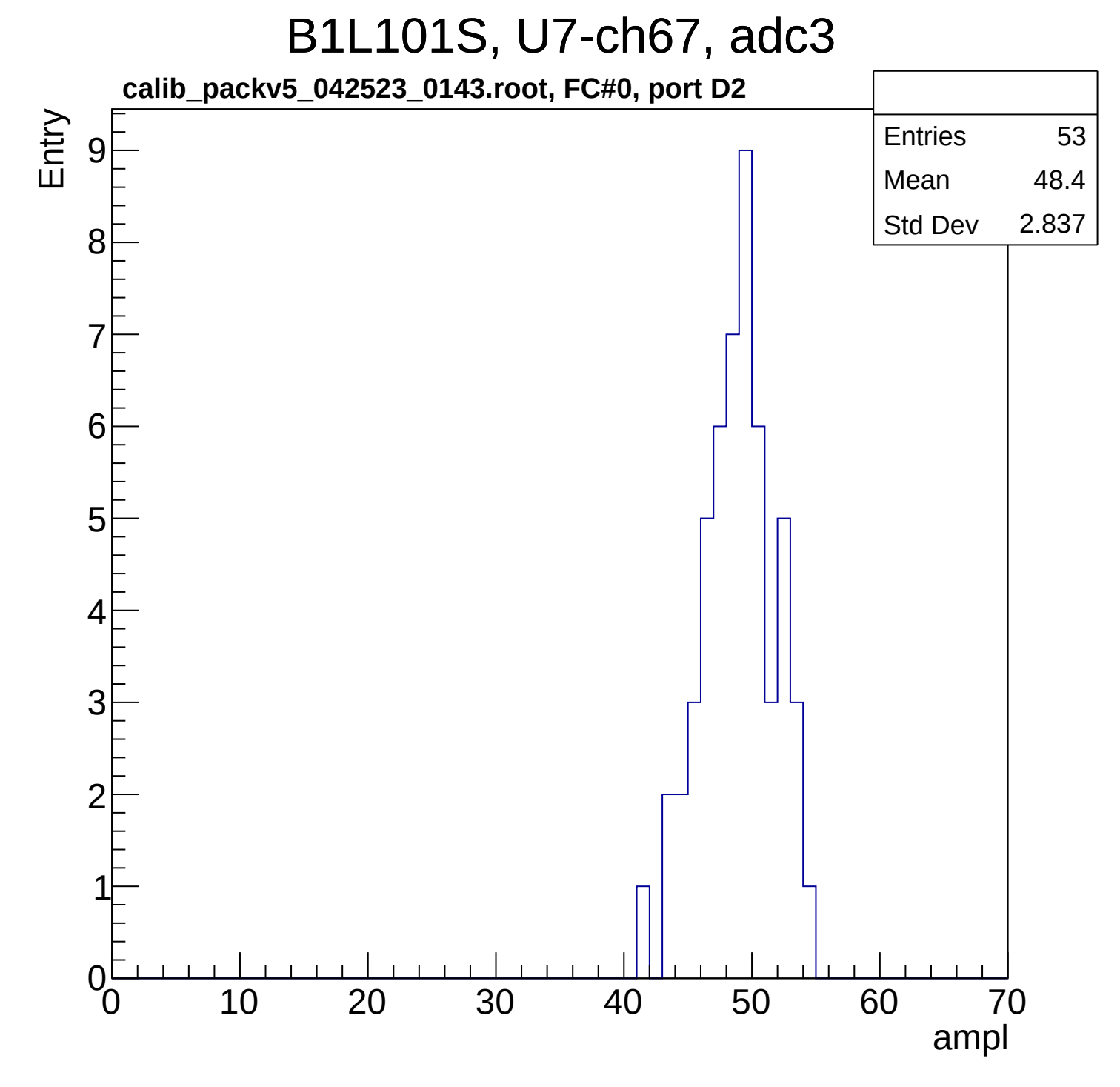
B1L101S, U7-ch67, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 48.4
Std Dev 2.837
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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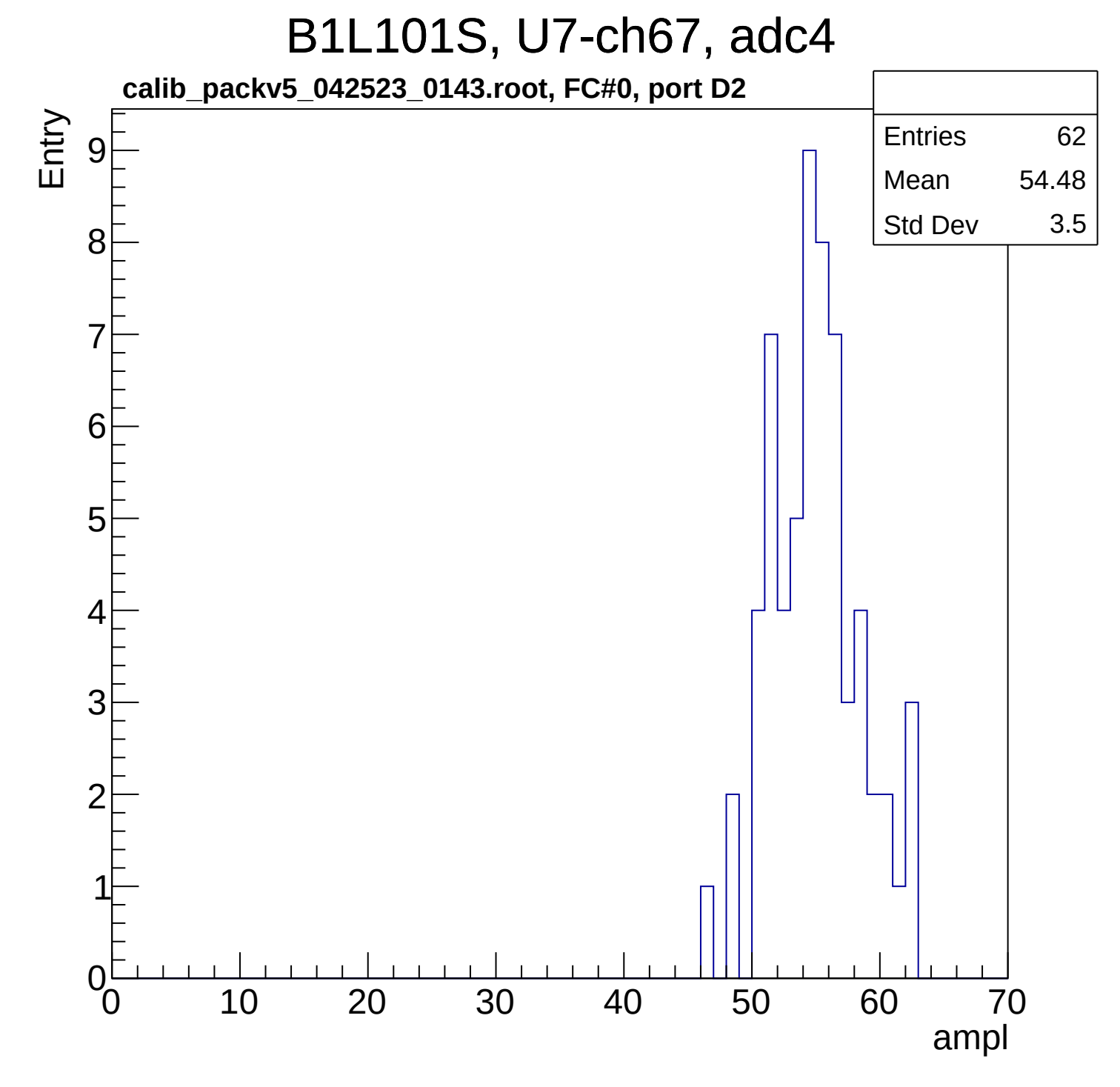
40
50
60
70


B1L101S, U7-ch67, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 54.48
Std Dev 3.5
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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40
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60
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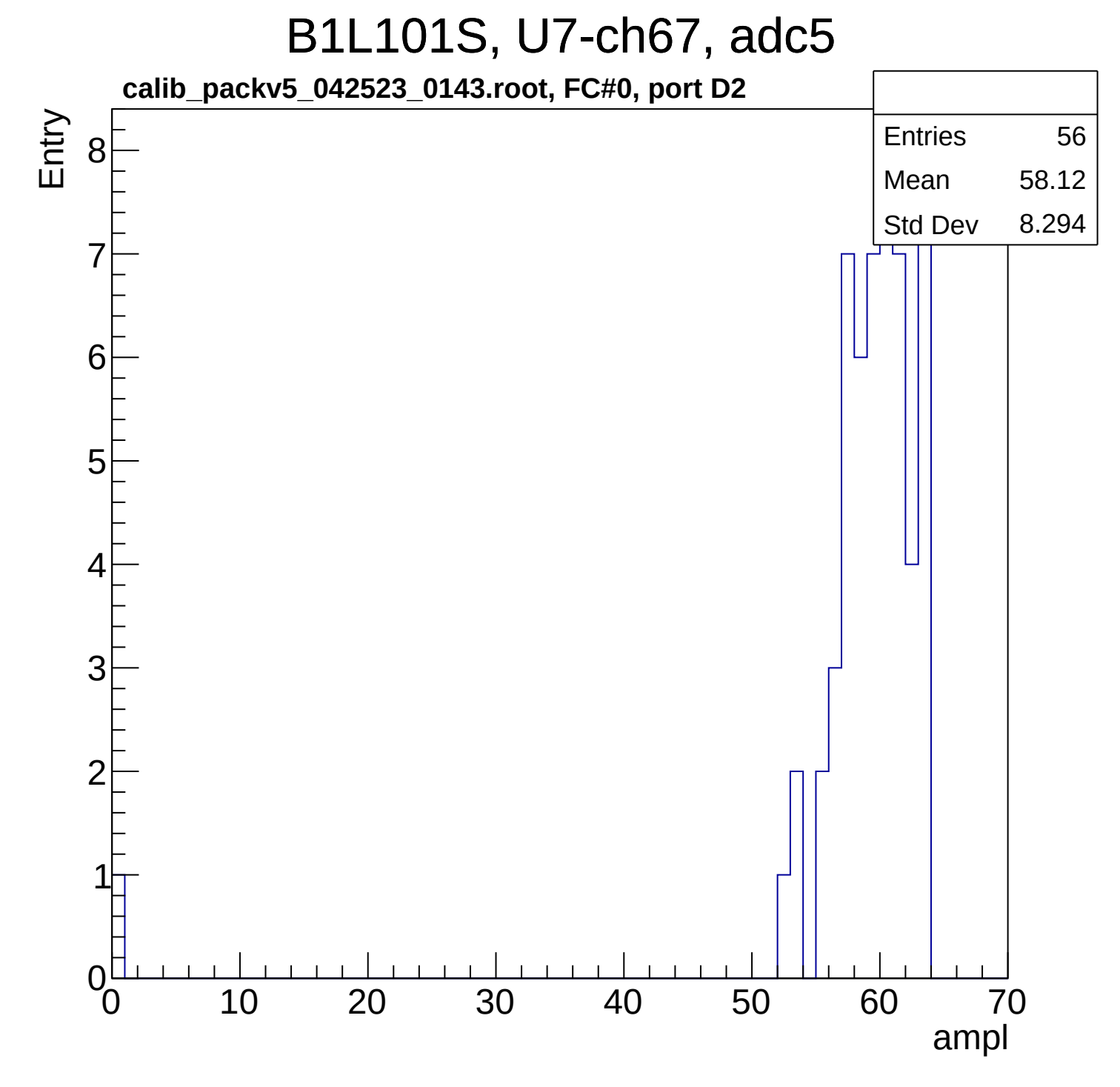
B1L101S, U7-ch67, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 58.12
Std Dev 8.294
Entry
ampl
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2
3
4
5
6
7
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0
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40
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60
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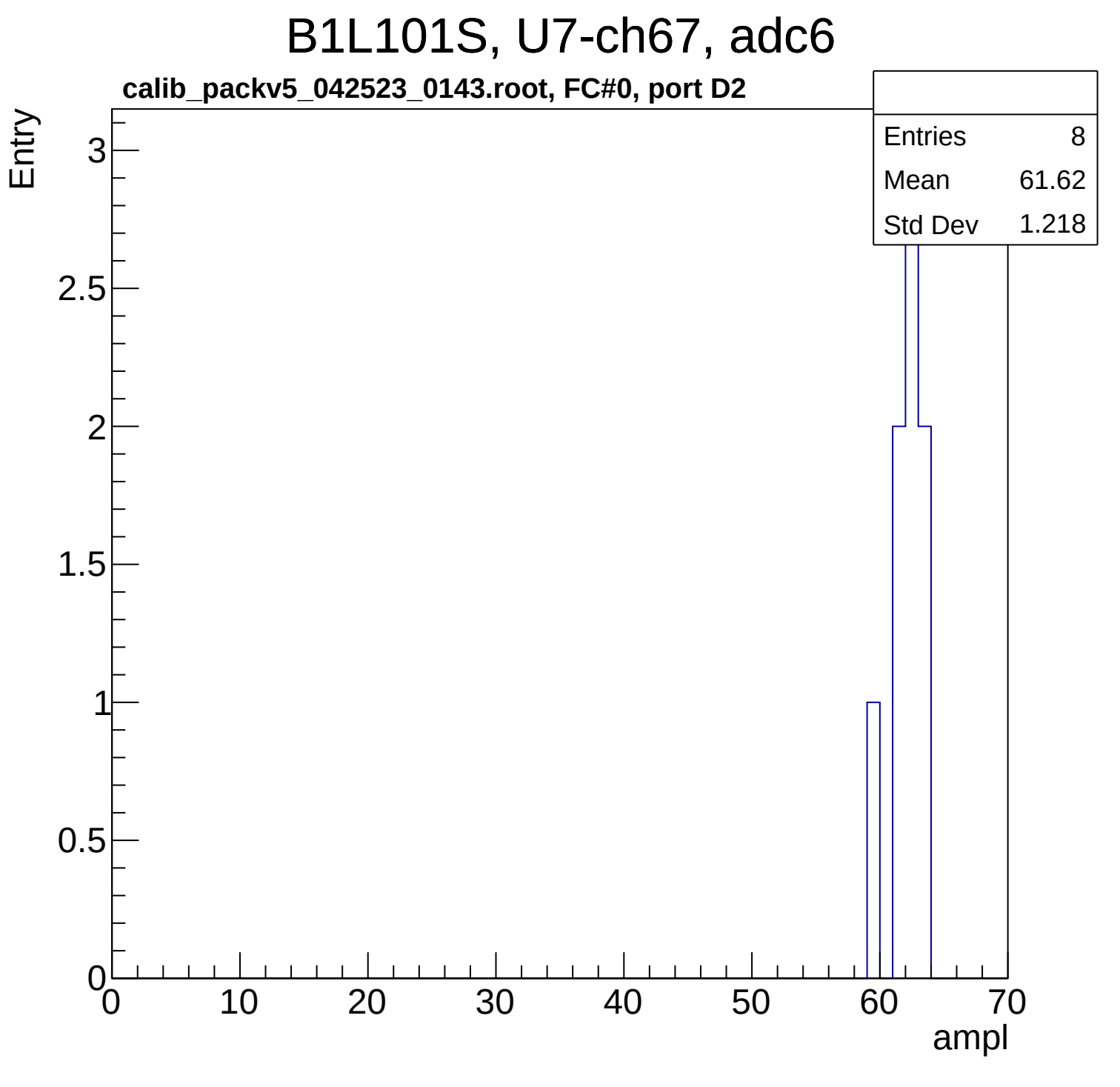
B1L101S, U7-ch67, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 61.62
Std Dev 1.218
Entry
ampl
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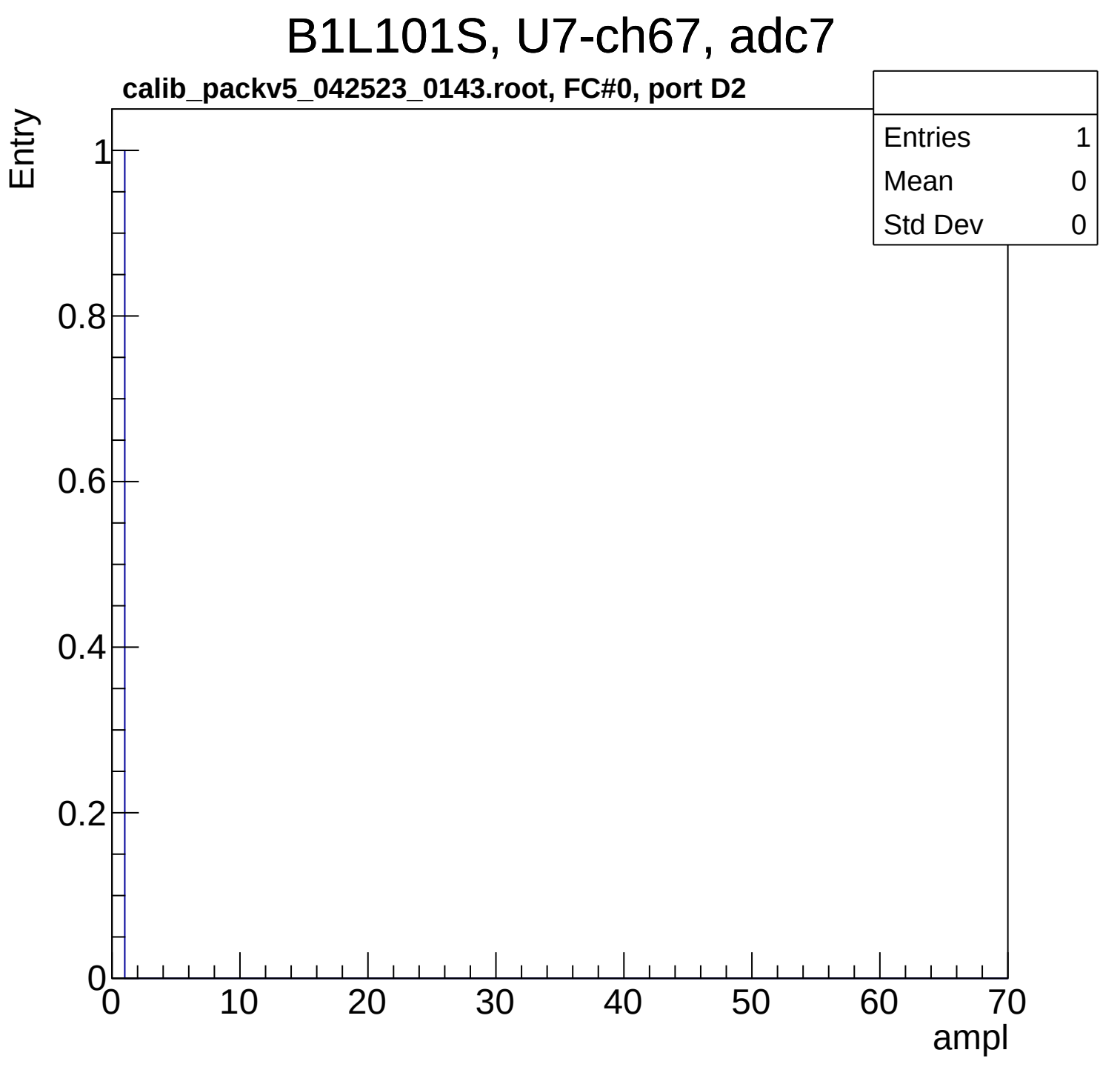
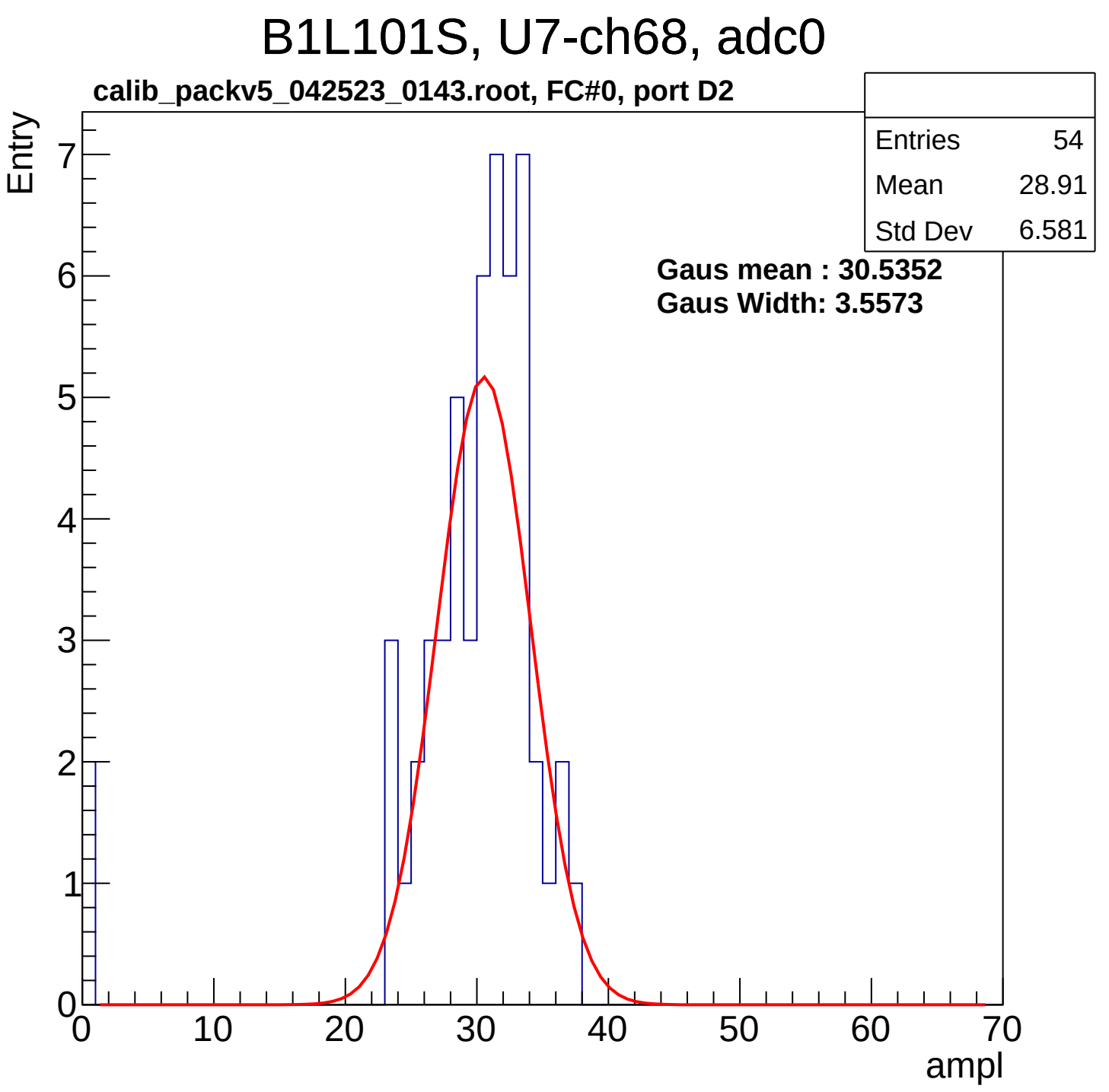
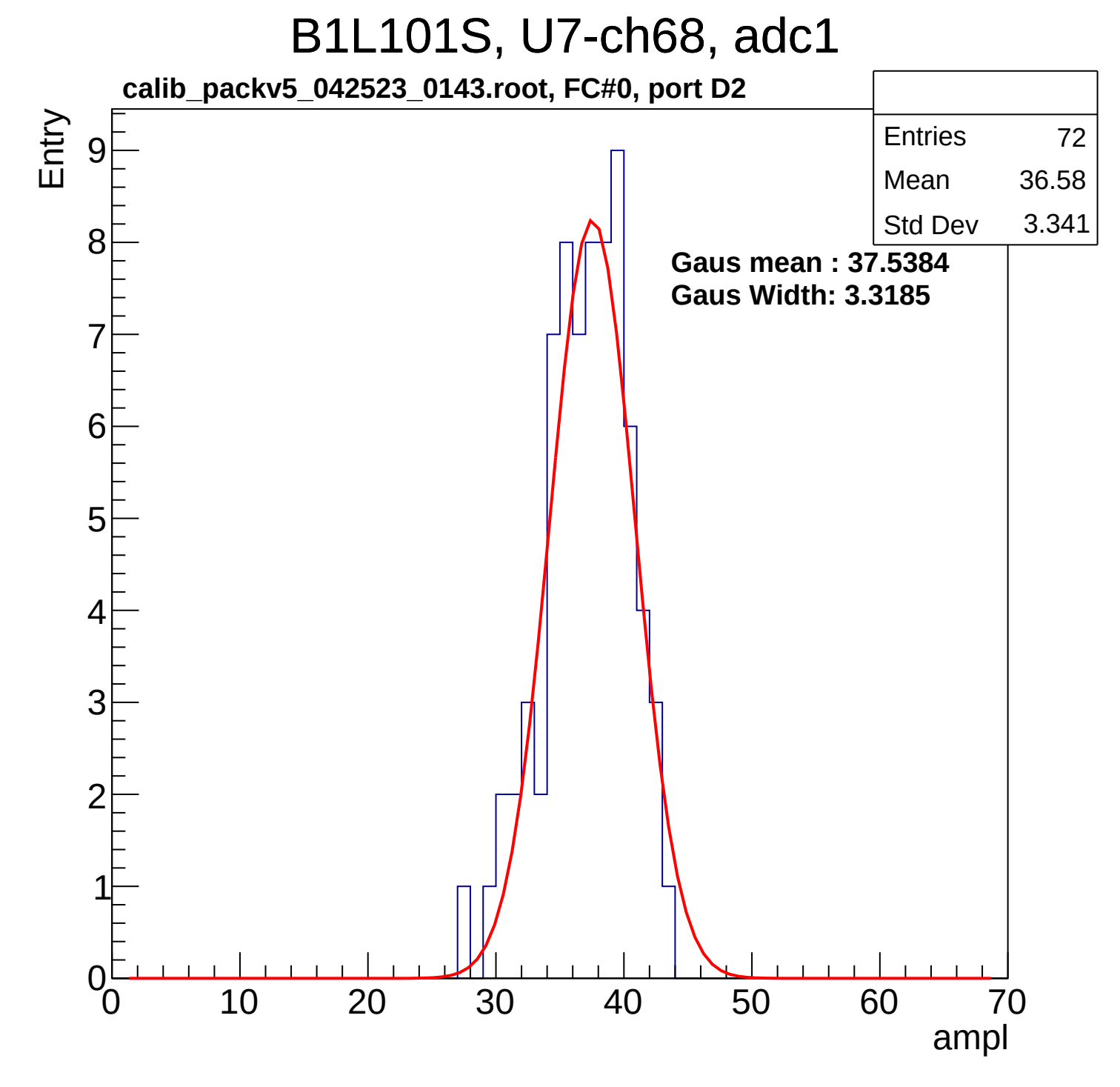
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U7-ch67, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch68, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 28.91
Std Dev 6.581
Gaus mean : 30.5352
Gaus Width: 3.5573
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U7-ch68, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 36.58
Std Dev 3.341
Gaus mean : 37.5384
Gaus Width: 3.3185
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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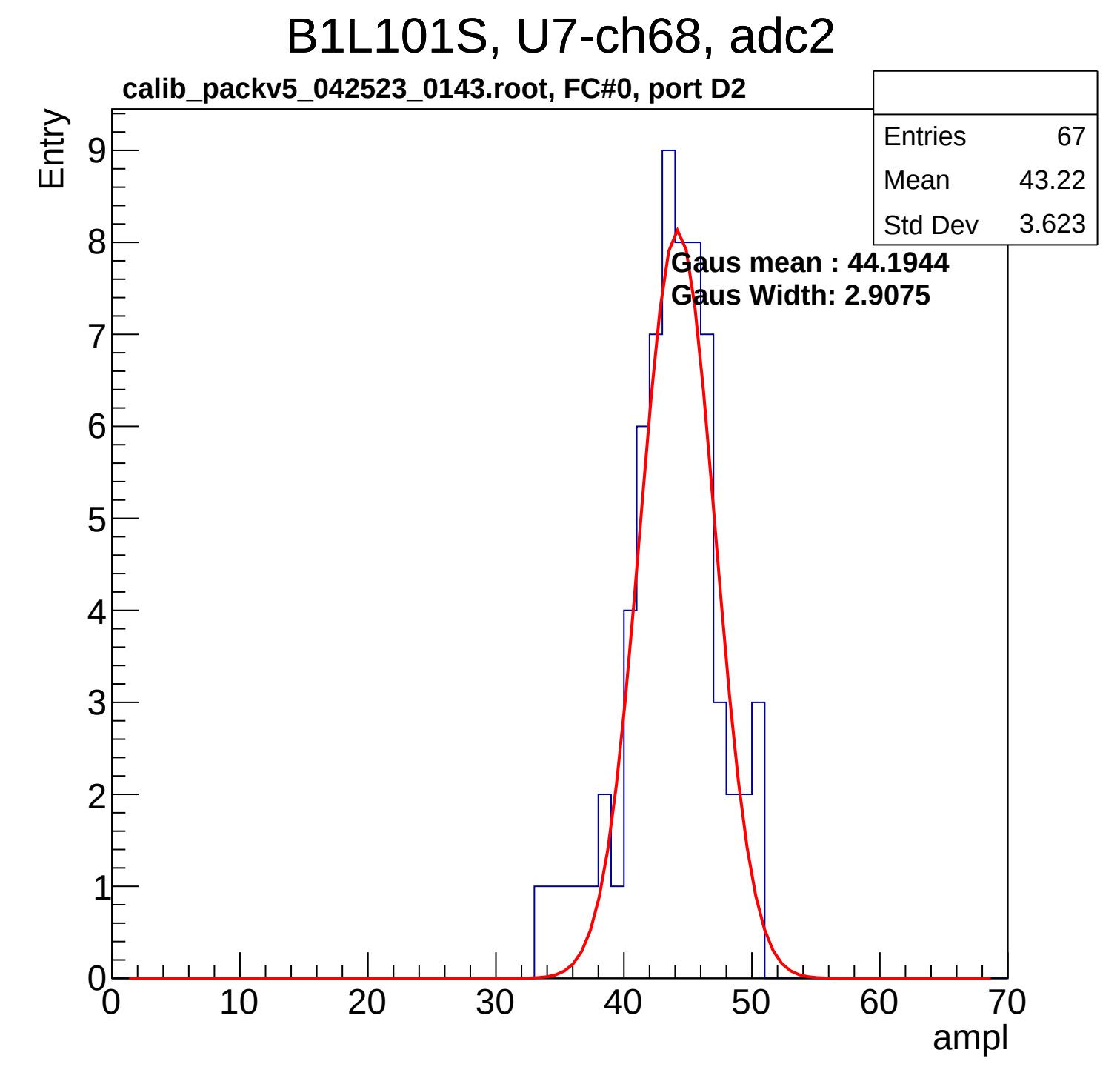
B1L101S, U7-ch68, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 43.22
Std Dev 3.623
Gaus mean : 44.1944
Gaus Width: 2.9075
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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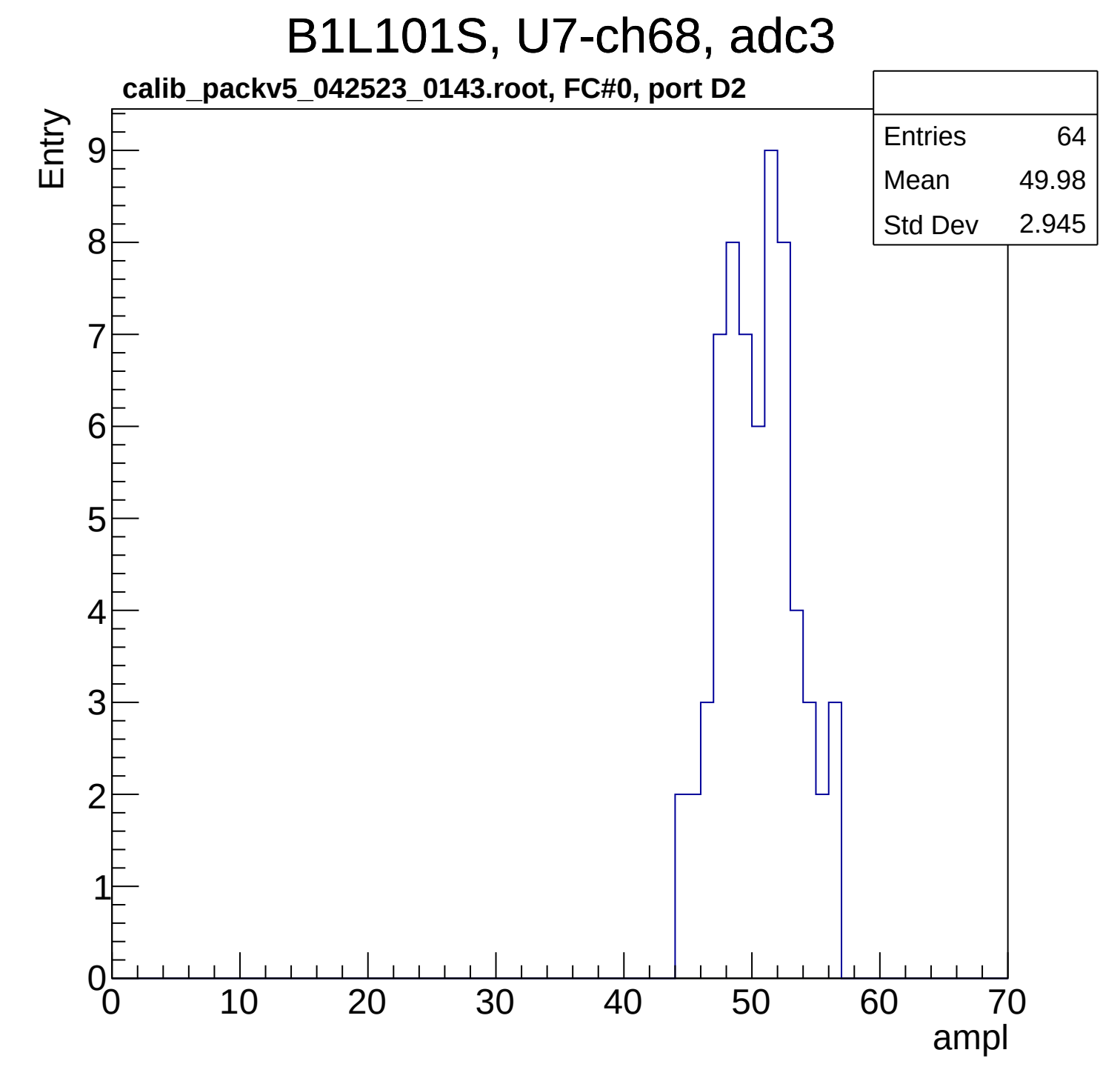
B1L101S, U7-ch68, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 49.98
Std Dev 2.945
Entry
ampl
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2
3
4
5
6
7
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0
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60
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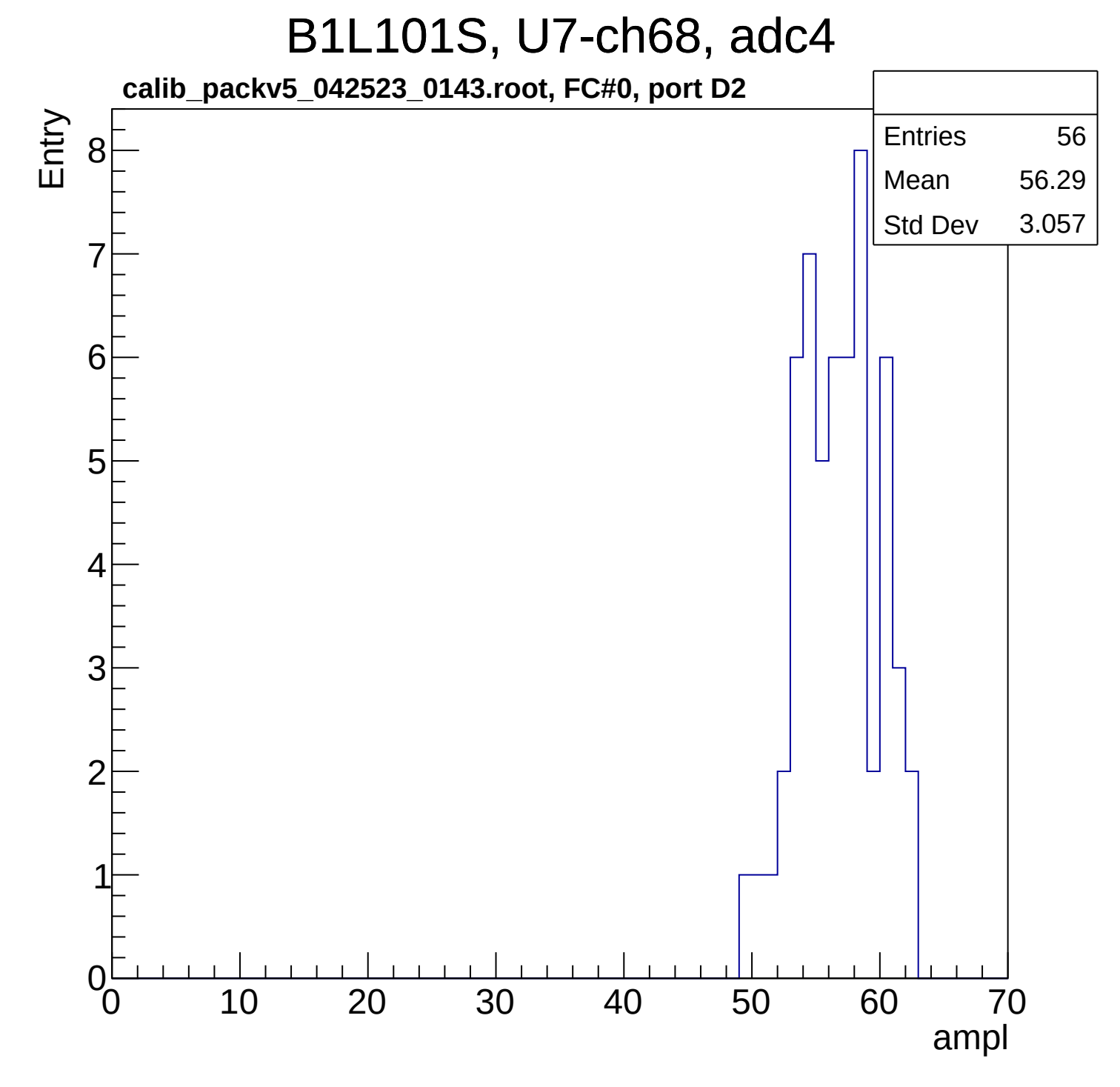
B1L101S, U7-ch68, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 56.29
Std Dev 3.057
Entry
ampl
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2
3
4
5
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0
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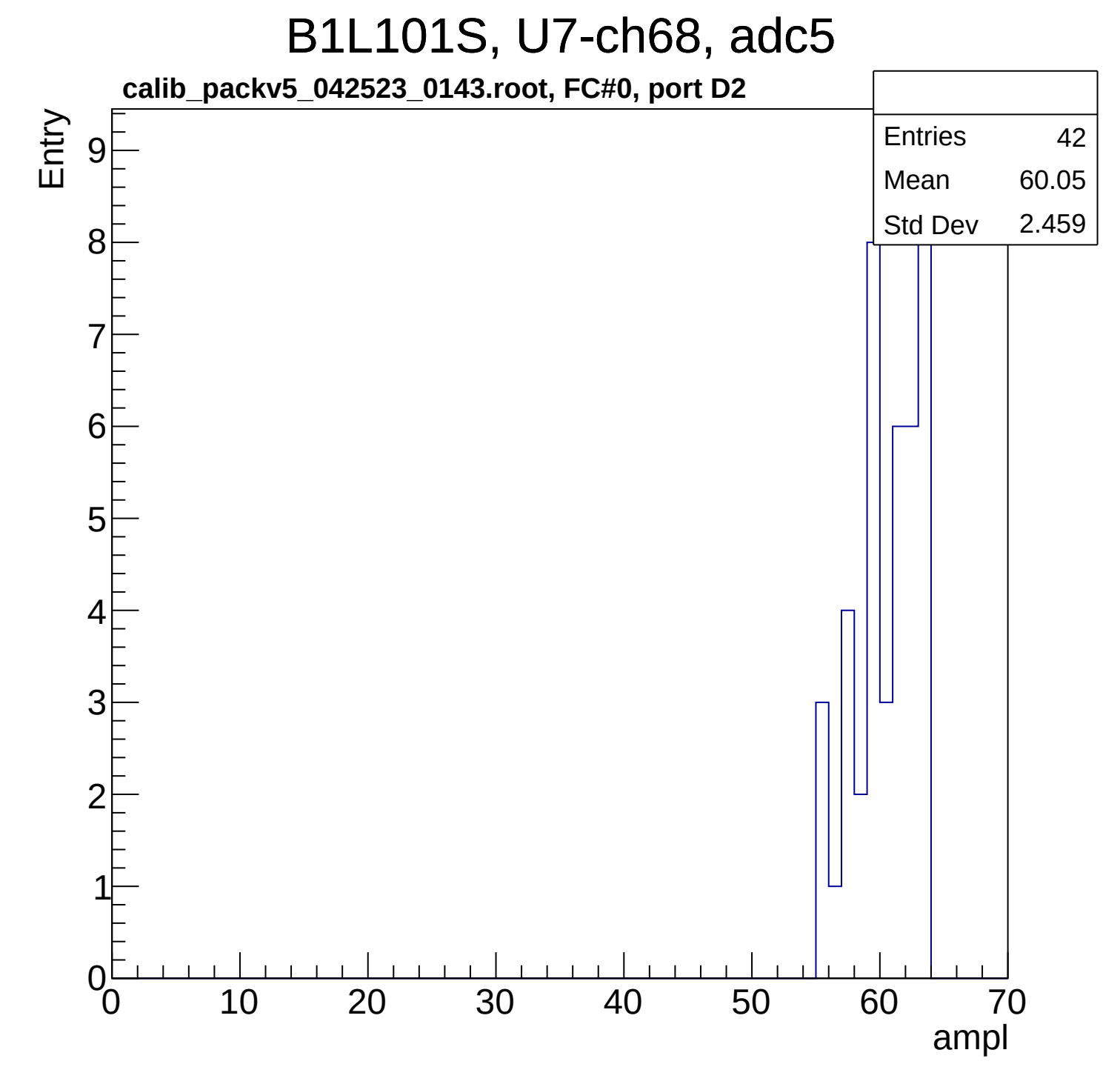
B1L101S, U7-ch68, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 60.05
Std Dev 2.459
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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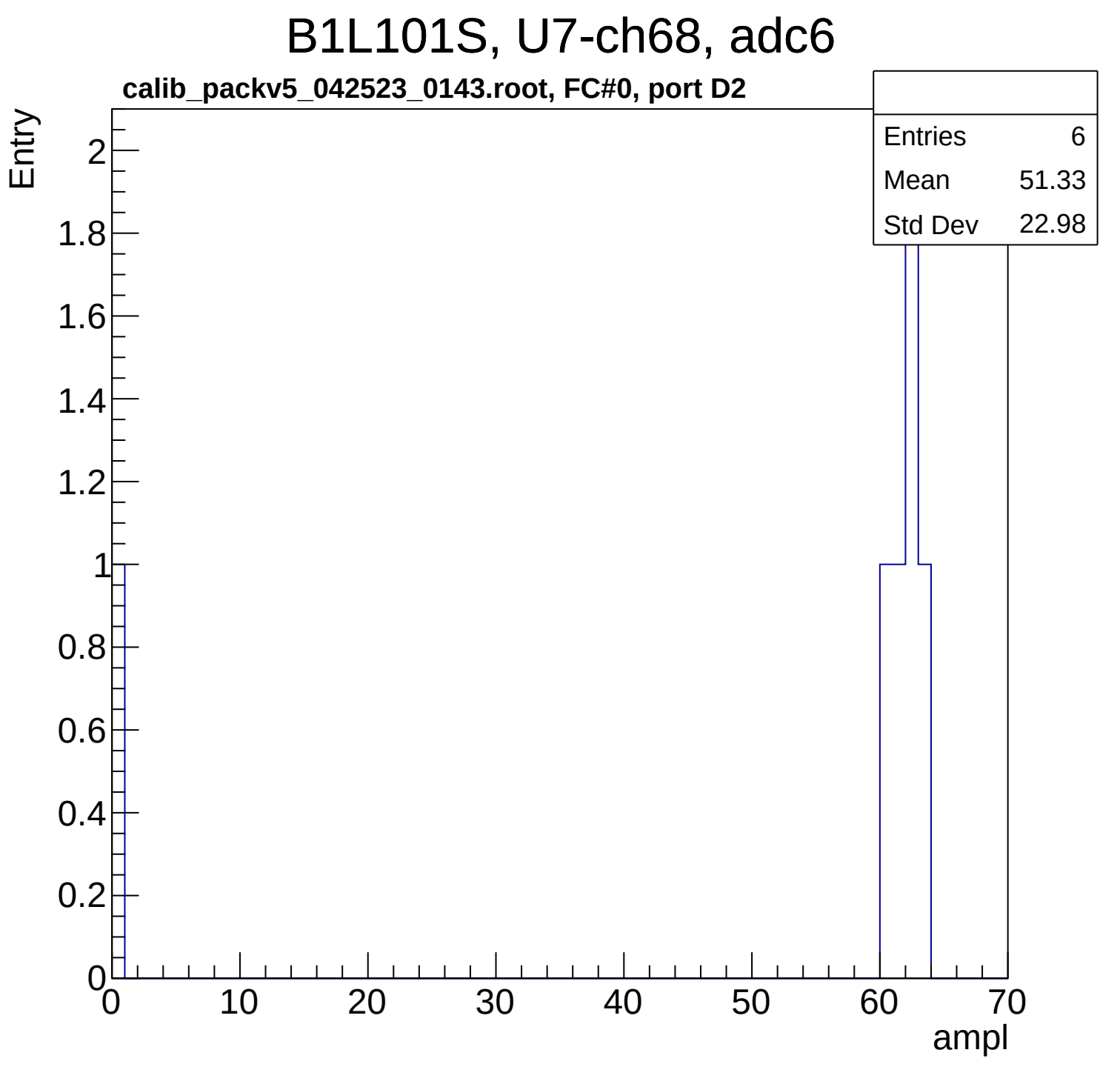
B1L101S, U7-ch68, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 51.33
Std Dev 22.98
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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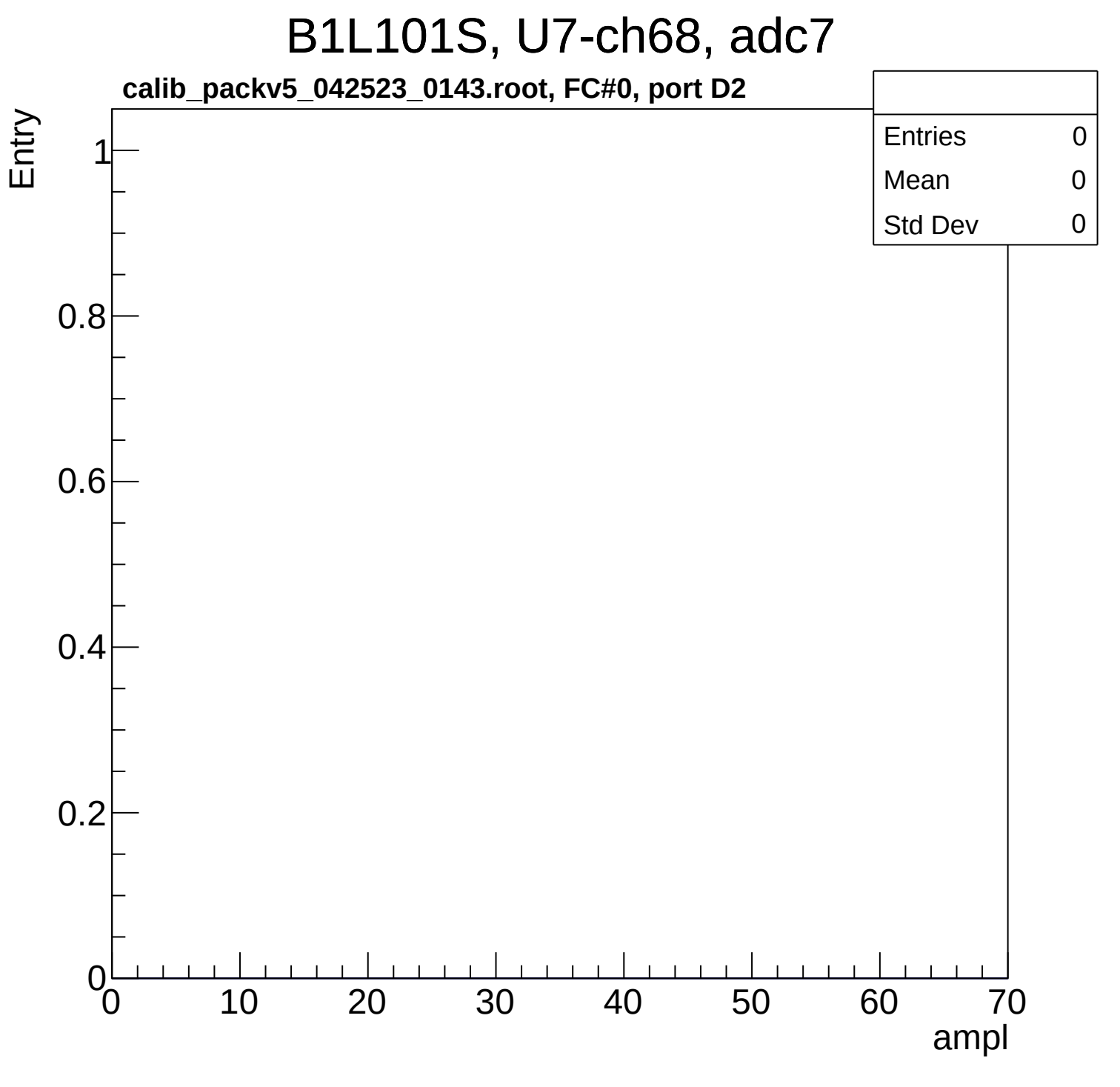
40
50
60
70


B1L101S, U7-ch68, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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0.6
0.4
0.2
0
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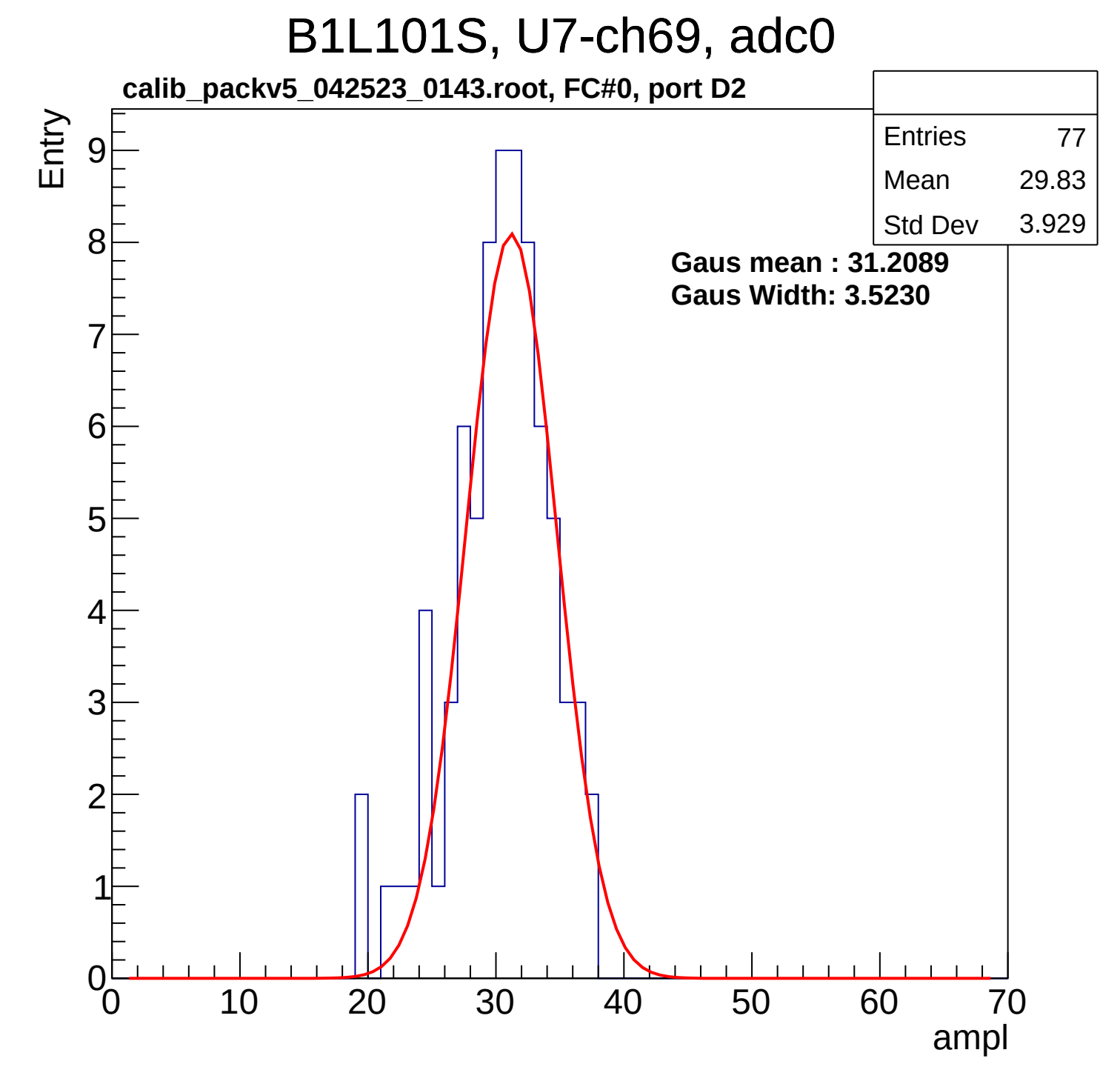
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch69, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 29.83
Std Dev 3.929
Gaus mean : 31.2089
Gaus Width: 3.5230
Entry
ampl
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2
3
4
5
6
7
8
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0
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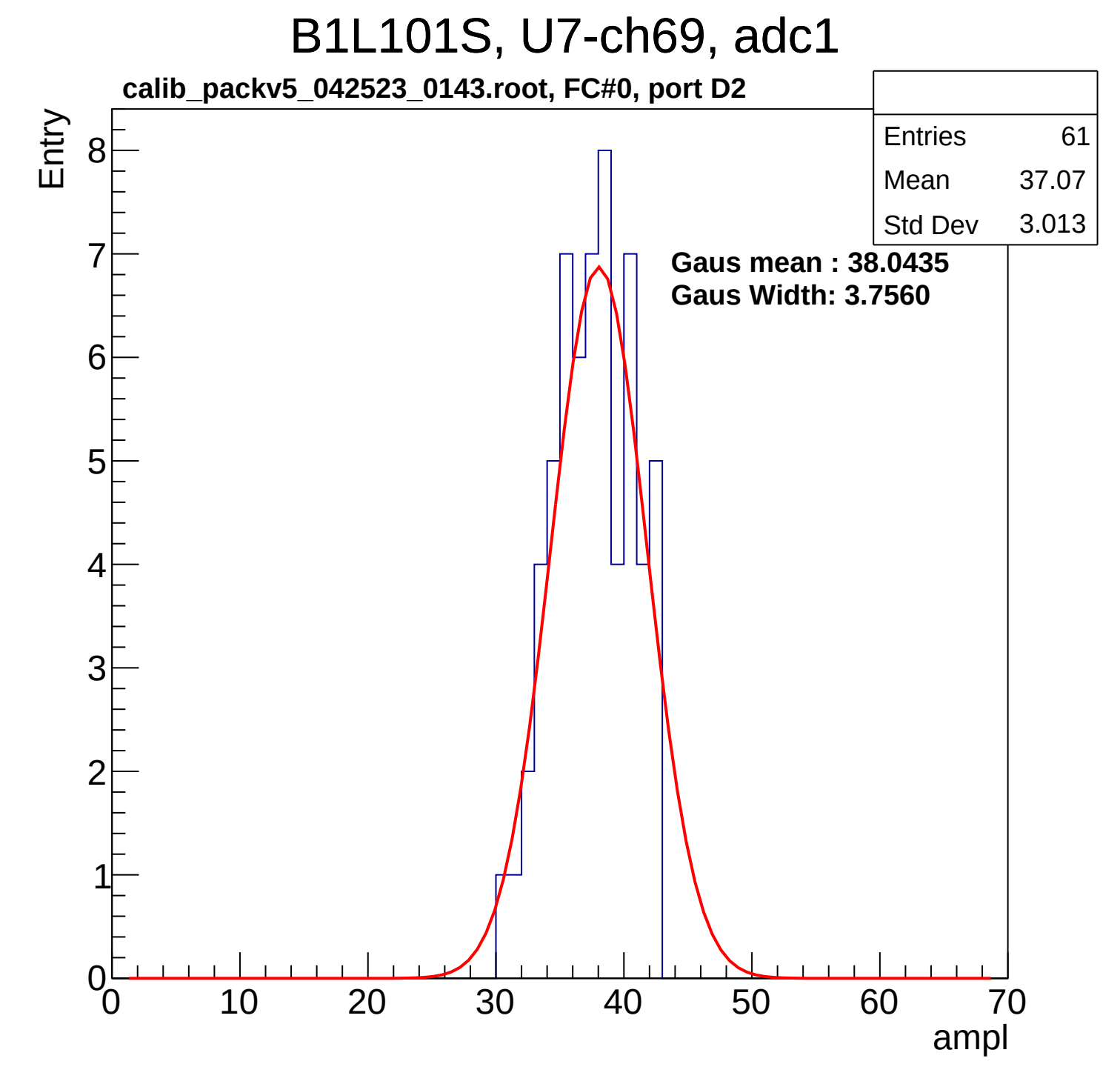
B1L101S, U7-ch69, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 37.07
Std Dev 3.013
Gaus mean : 38.0435
Gaus Width: 3.7560
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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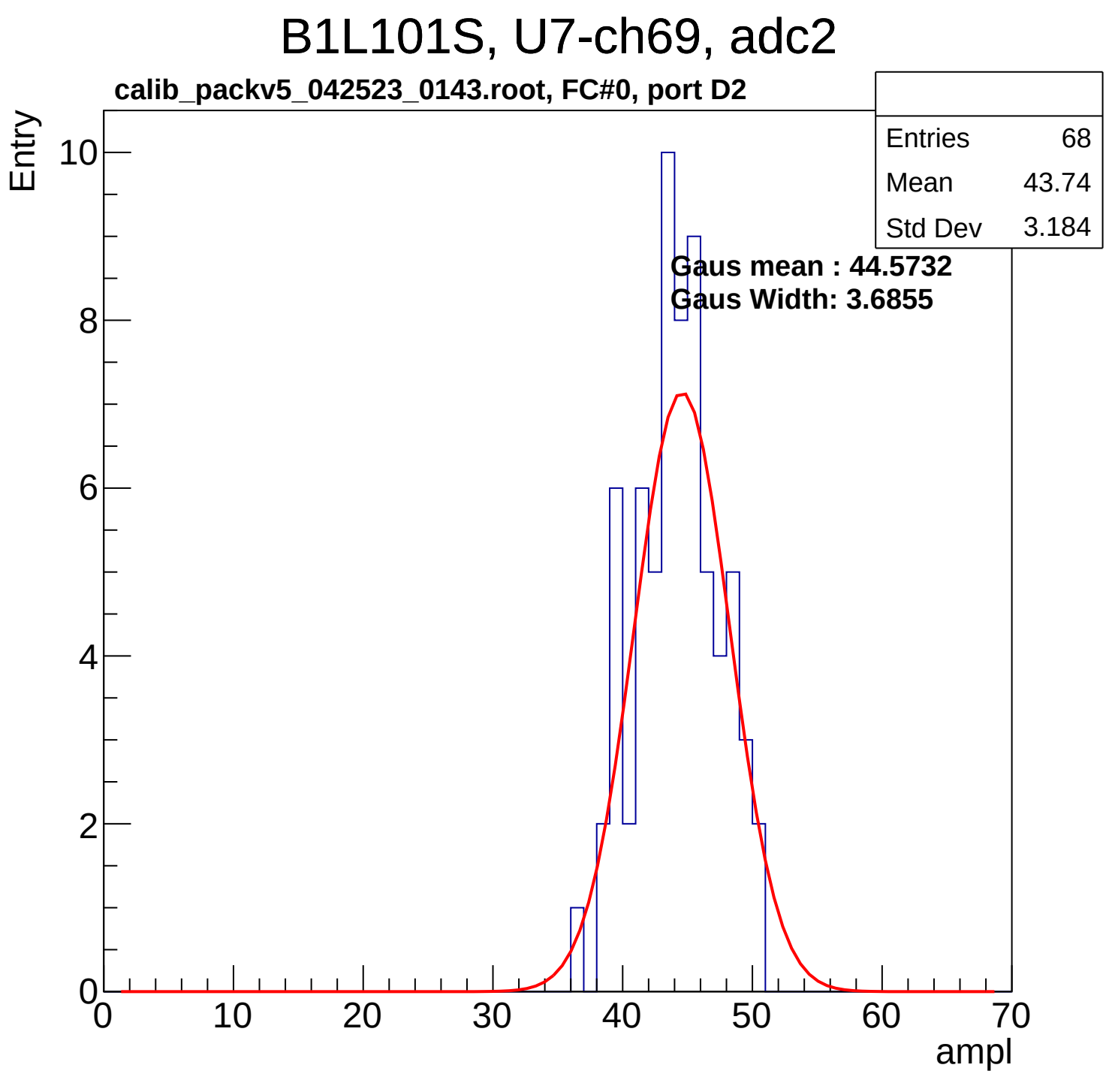
B1L101S, U7-ch69, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 43.74
Std Dev 3.184
Gaus mean : 44.5732
Gaus Width: 3.6855
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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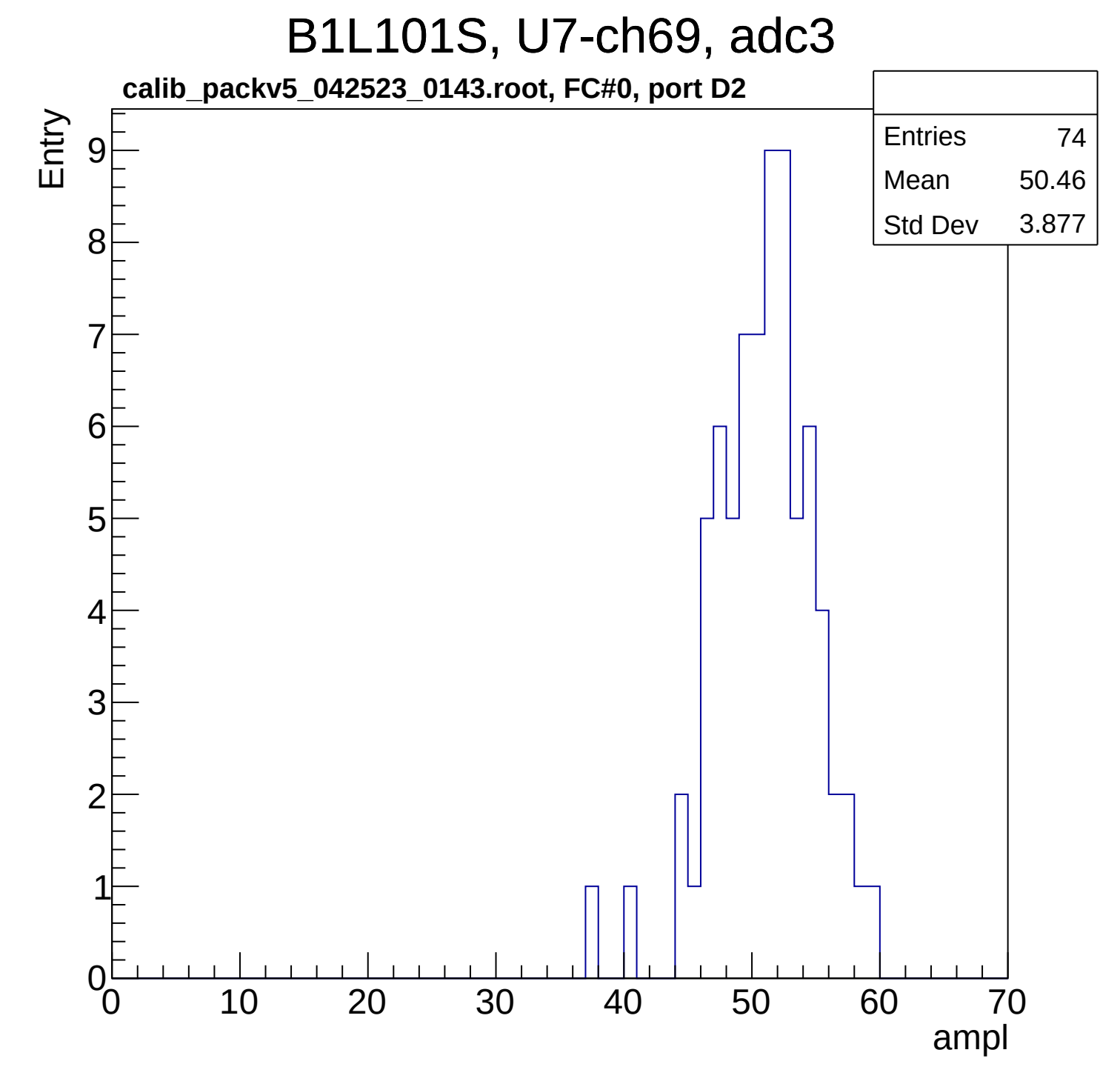
B1L101S, U7-ch69, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 50.46
Std Dev 3.877
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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40
50
60
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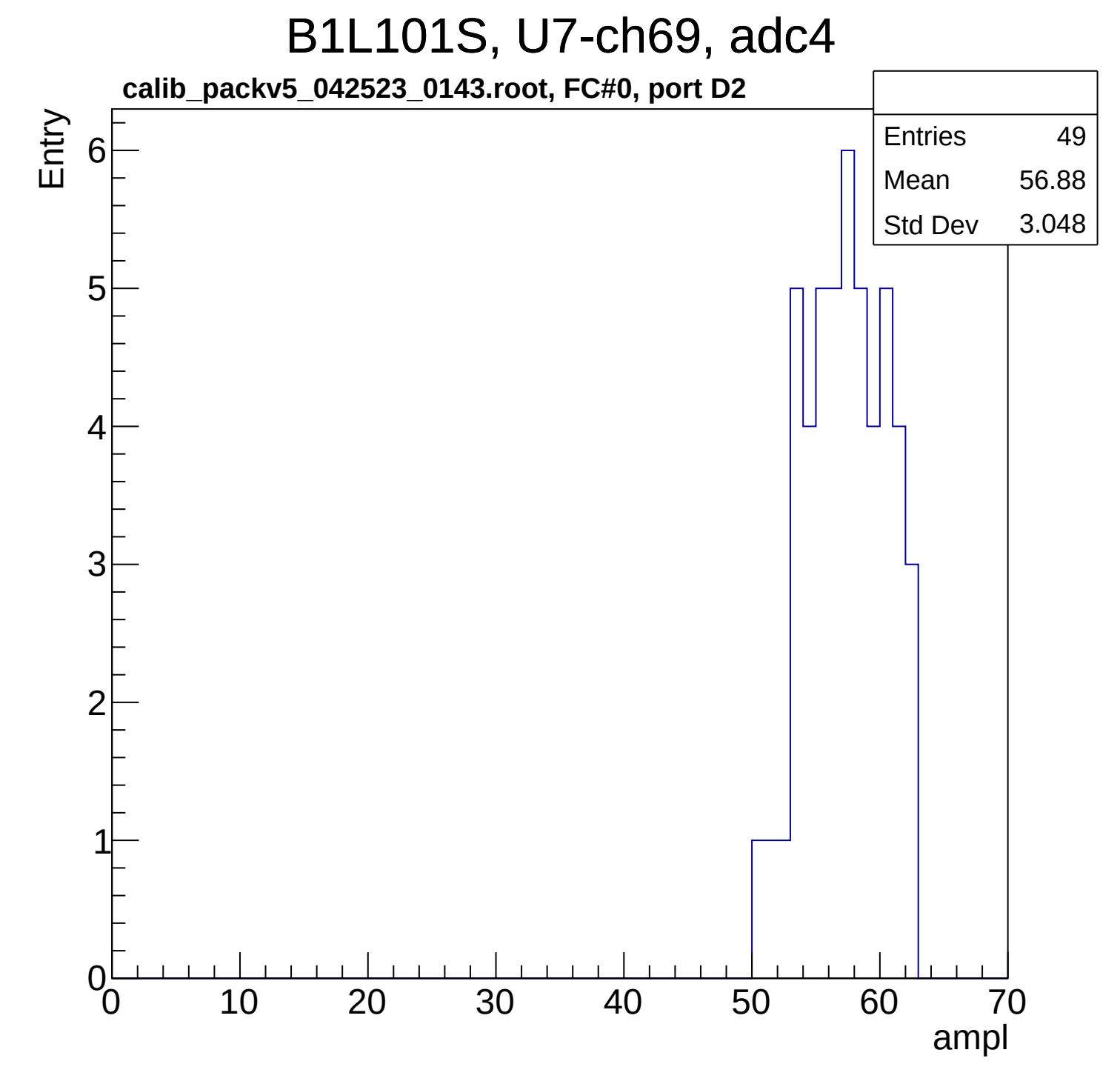
B1L101S, U7-ch69, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 56.88
Std Dev 3.048
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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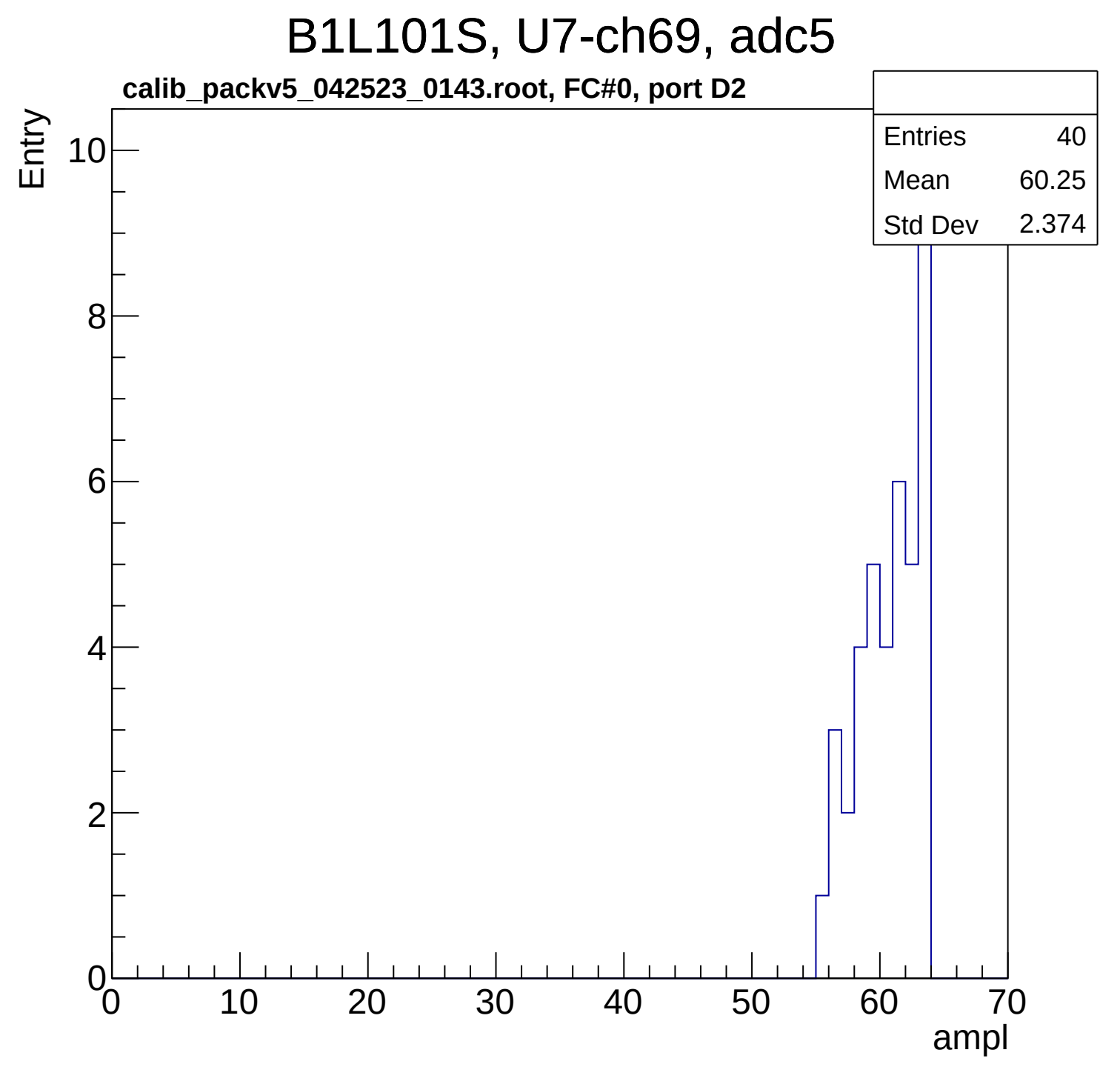
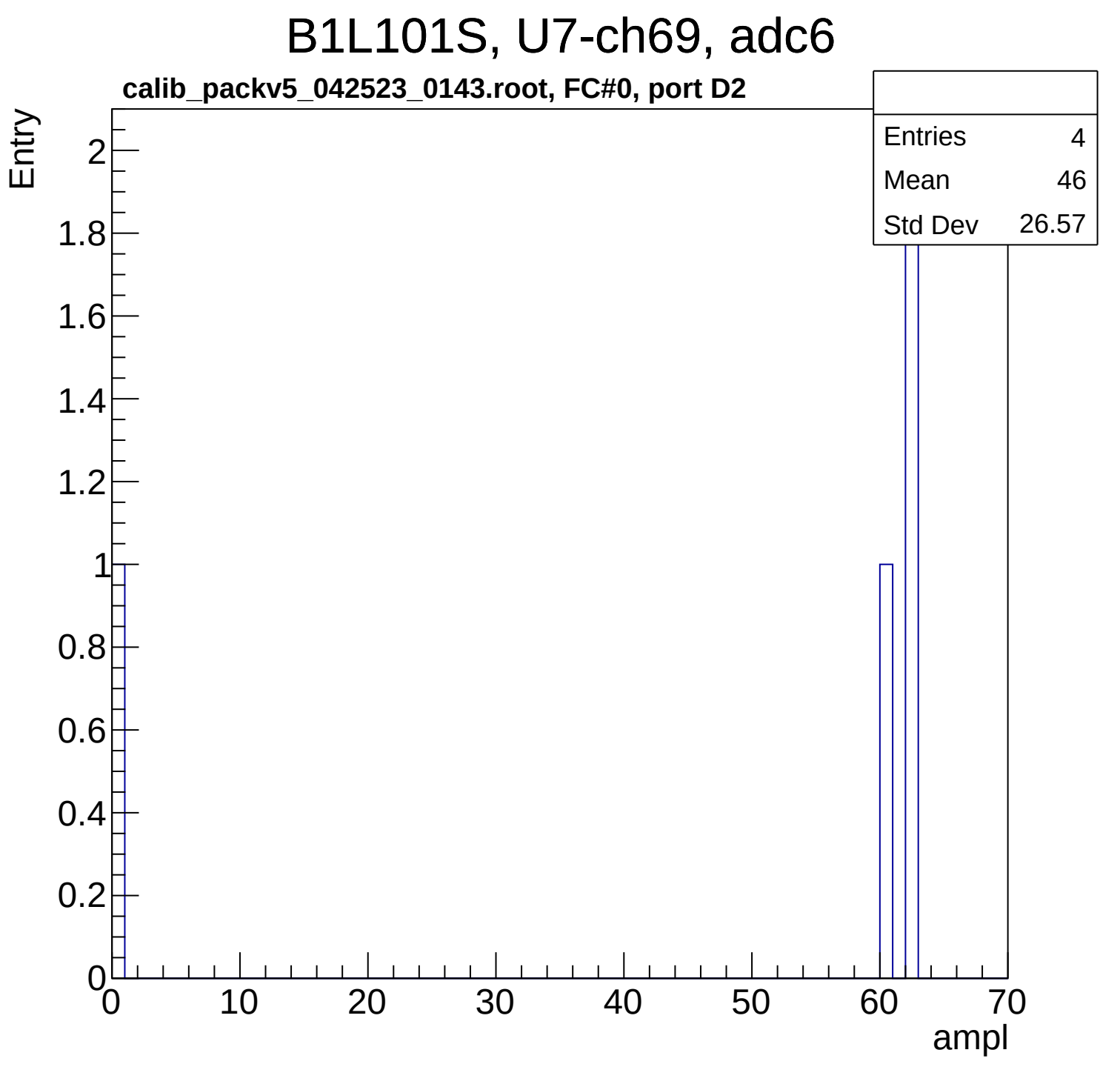
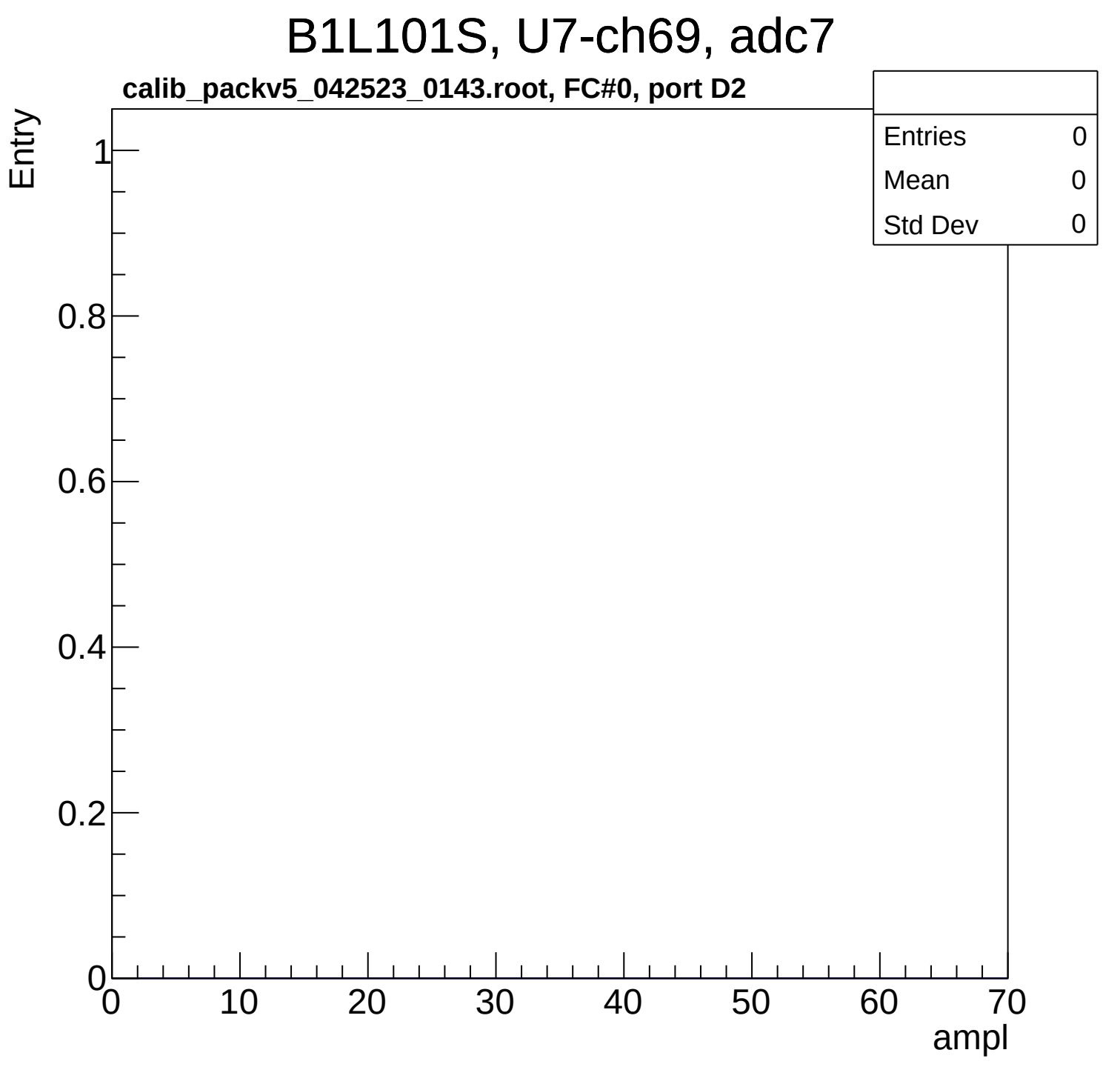
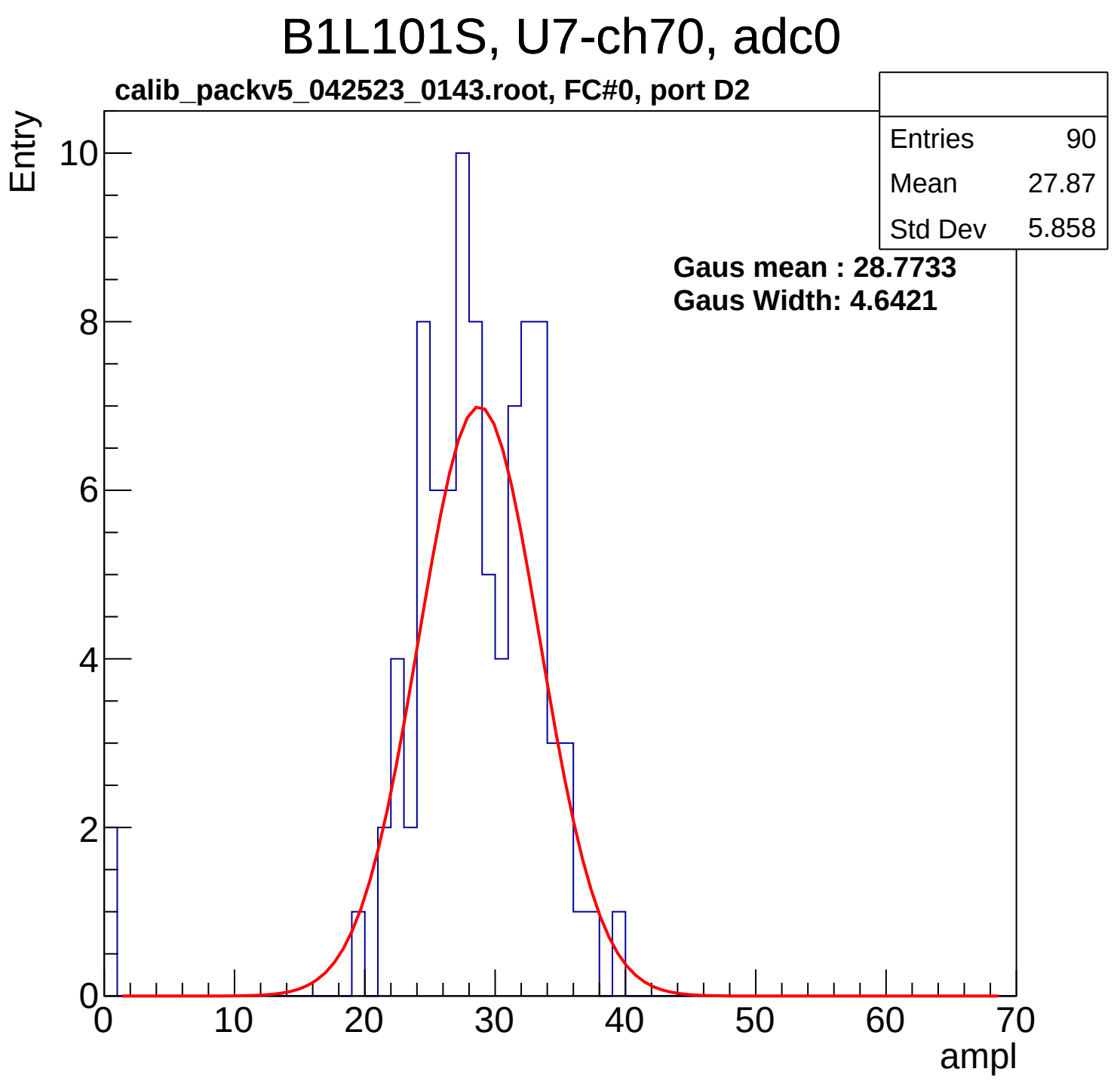
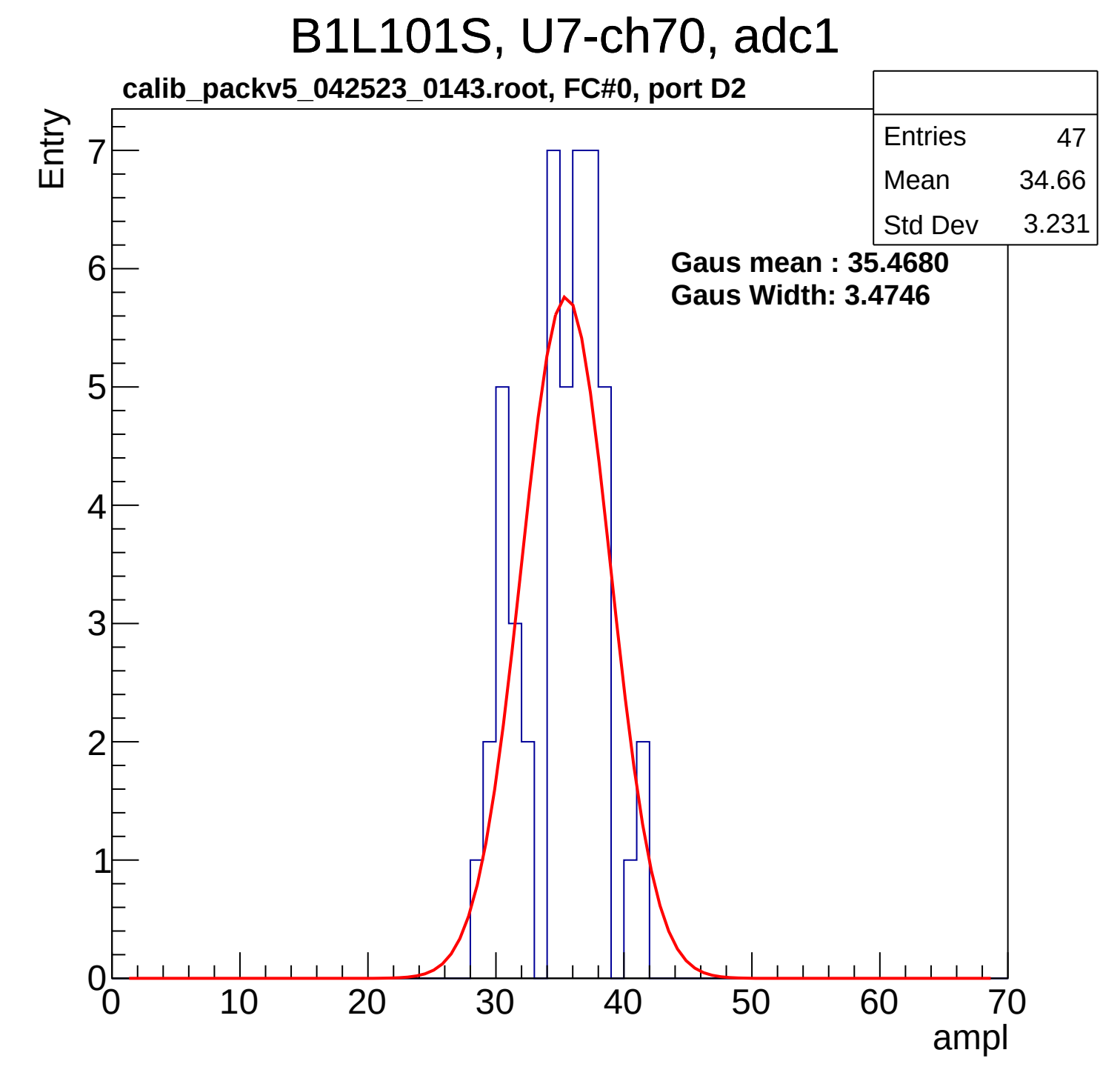

B1L101S, U7-ch69, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 40
Mean 60.25
Std Dev 2.374
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch69, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 46
Std Dev 26.57
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U7-ch69, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch70, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 90
Mean 27.87
Std Dev 5.858
Gaus mean : 28.7733
Gaus Width: 4.6421
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch70, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 34.66
Std Dev 3.231
Gaus mean : 35.4680
Gaus Width: 3.4746
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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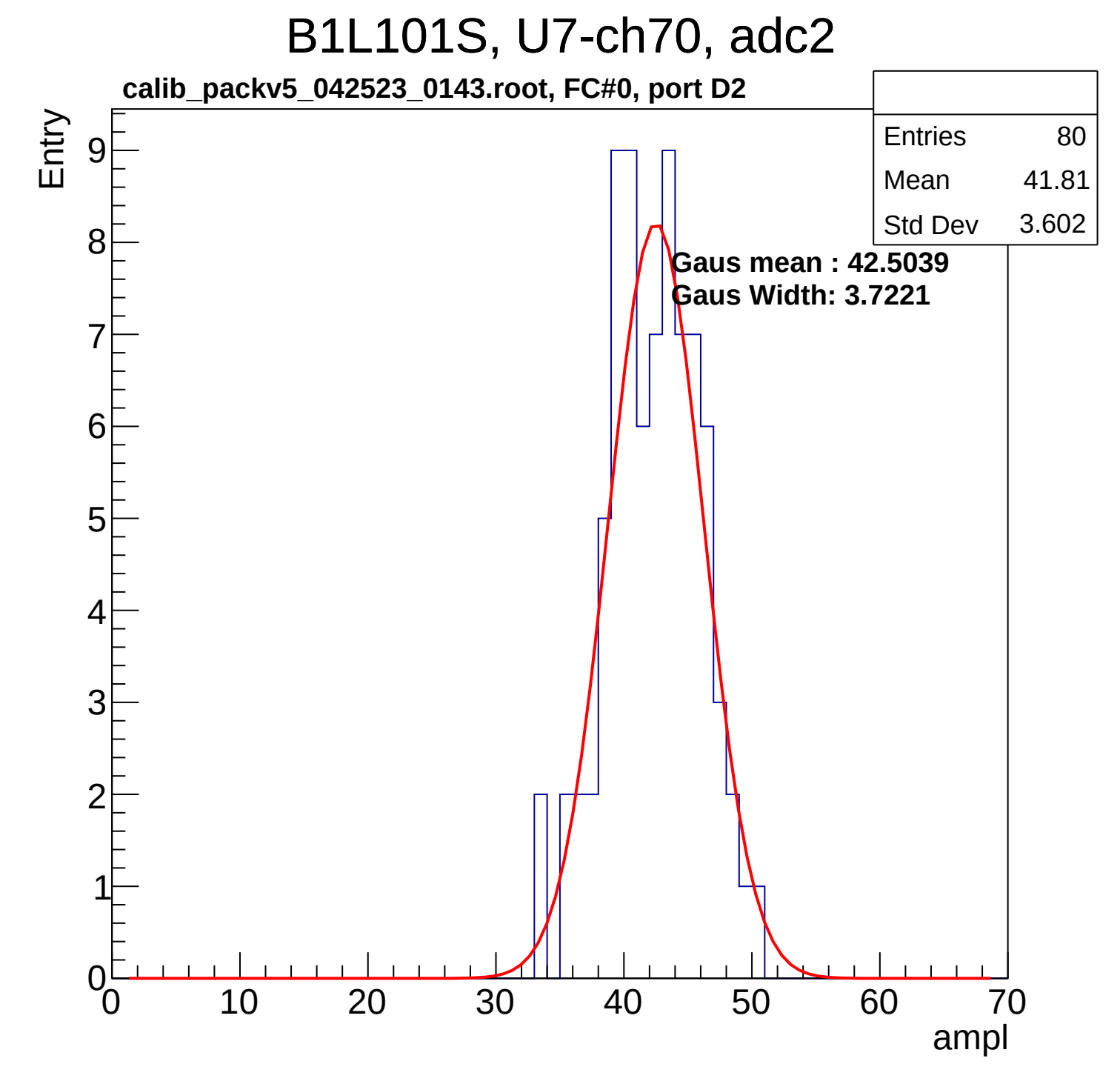
B1L101S, U7-ch70, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 80
Mean 41.81
Std Dev 3.602
Gaus mean : 42.5039
Gaus Width: 3.7221
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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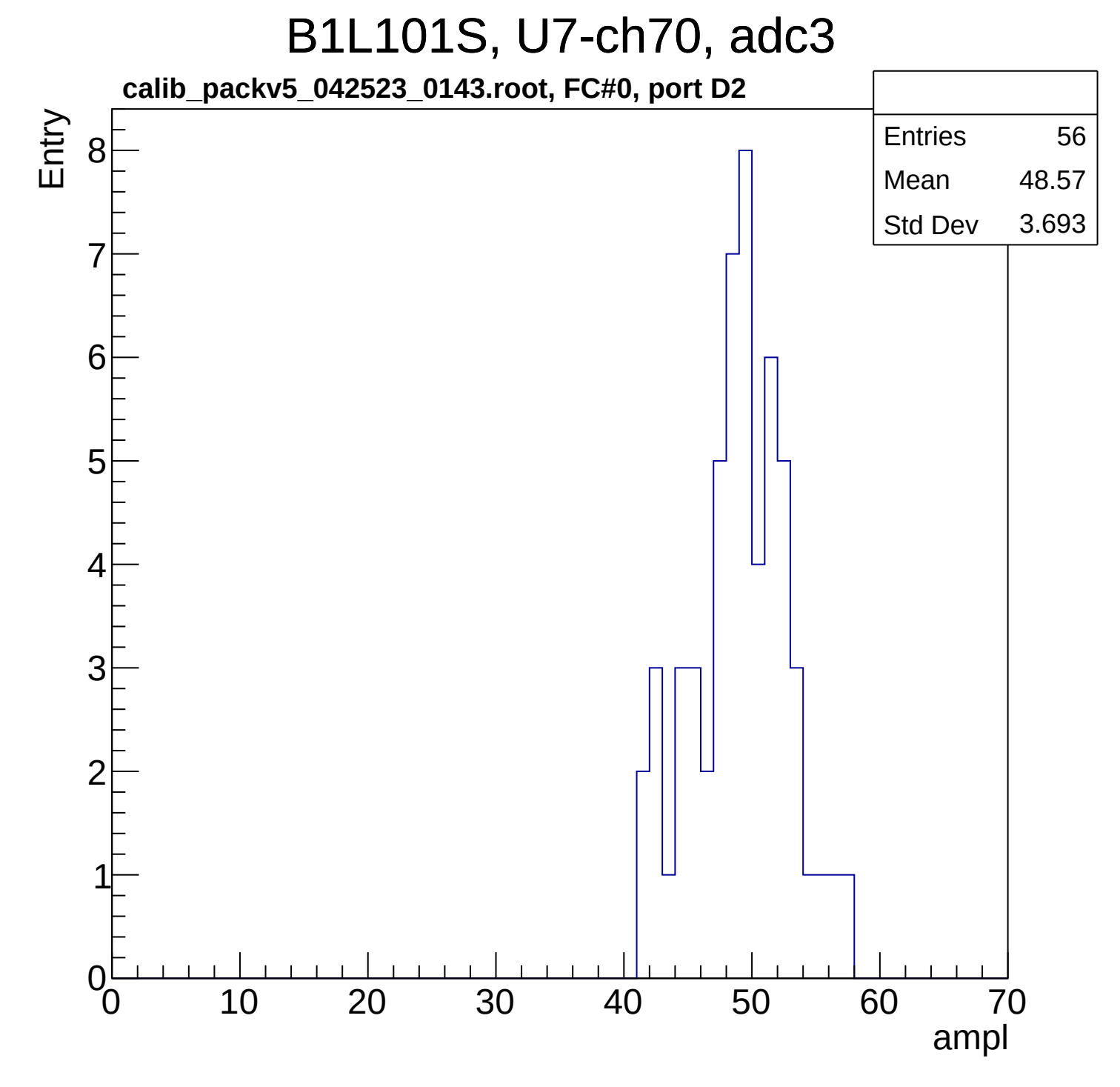
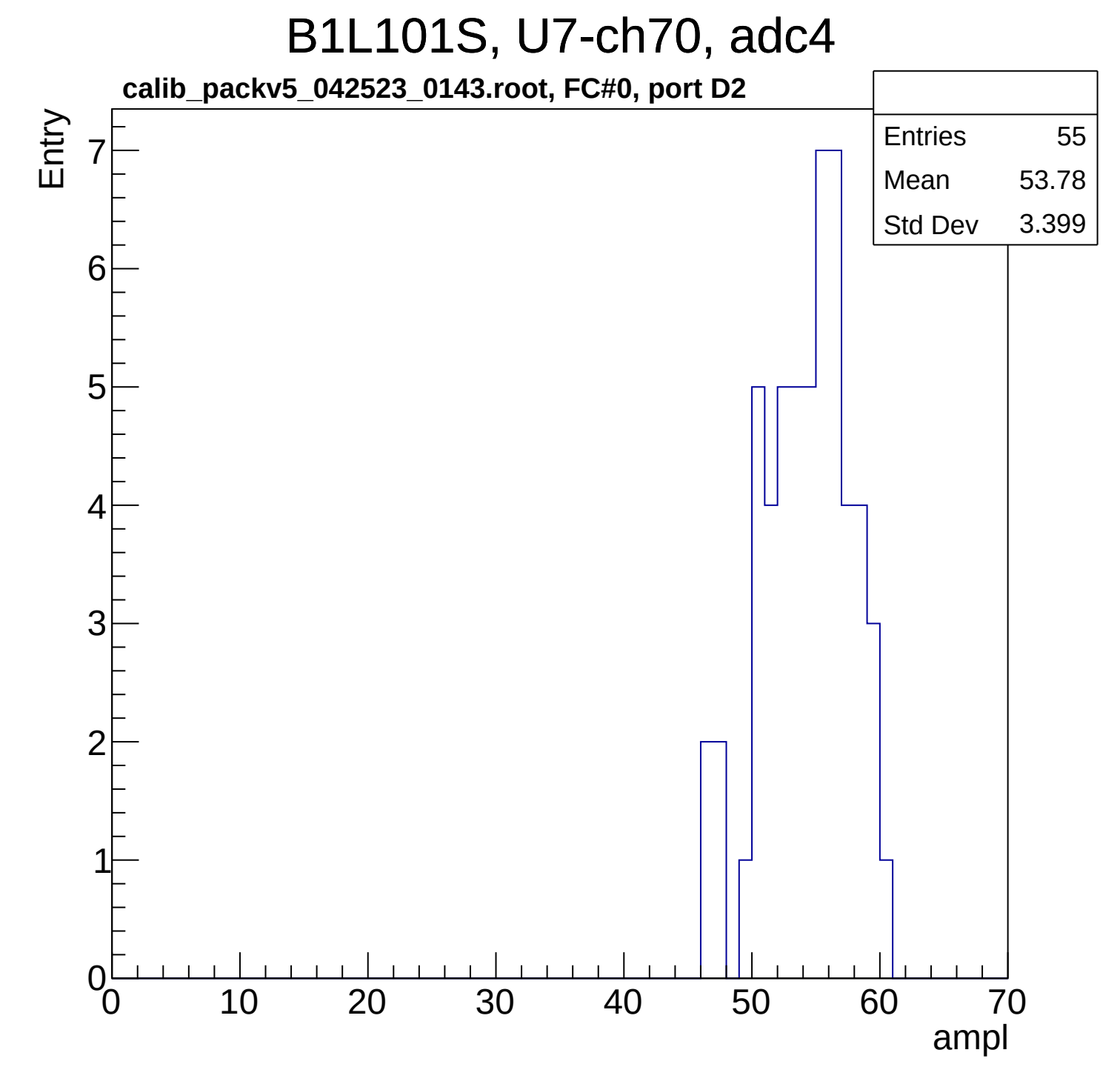
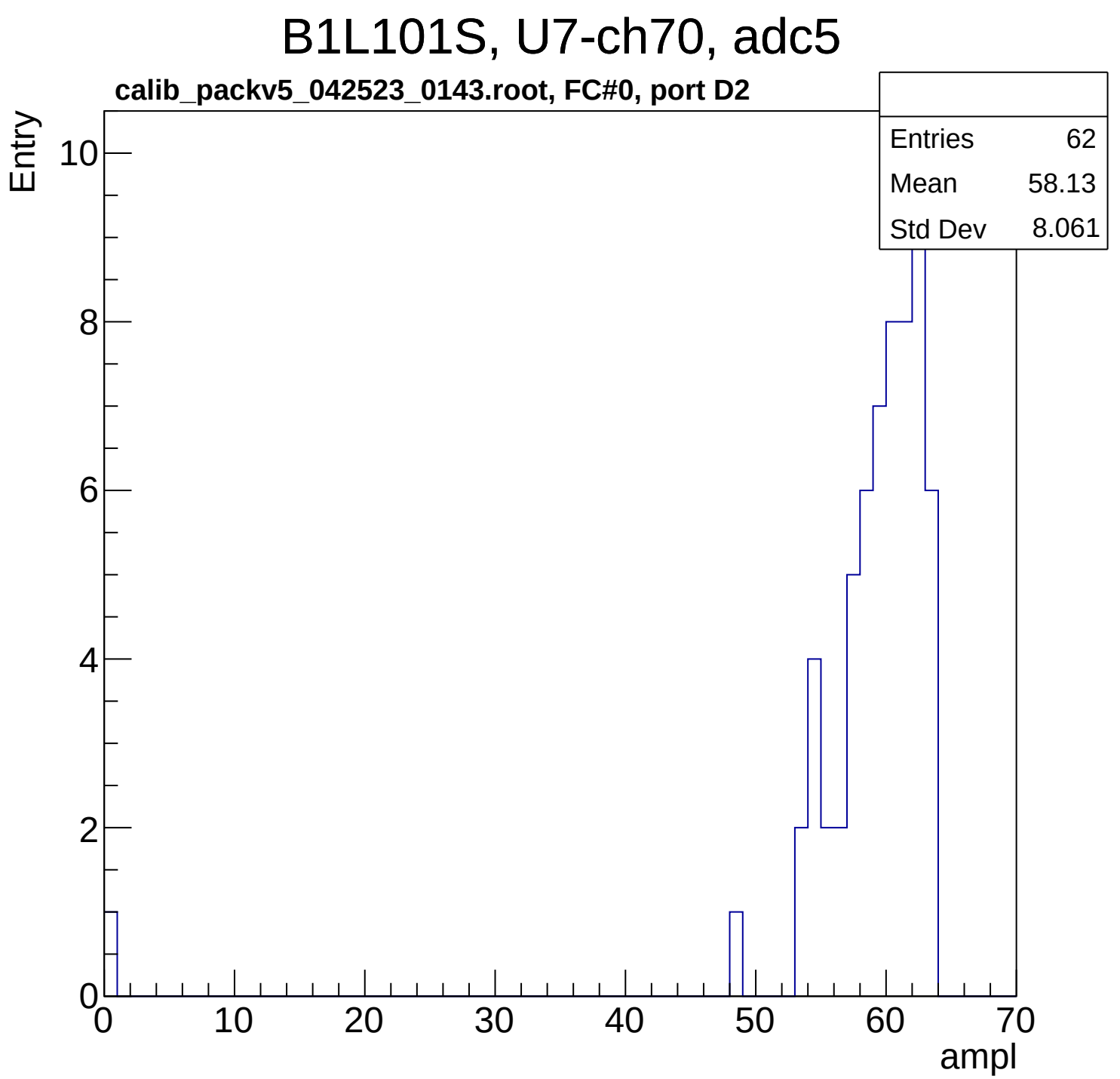
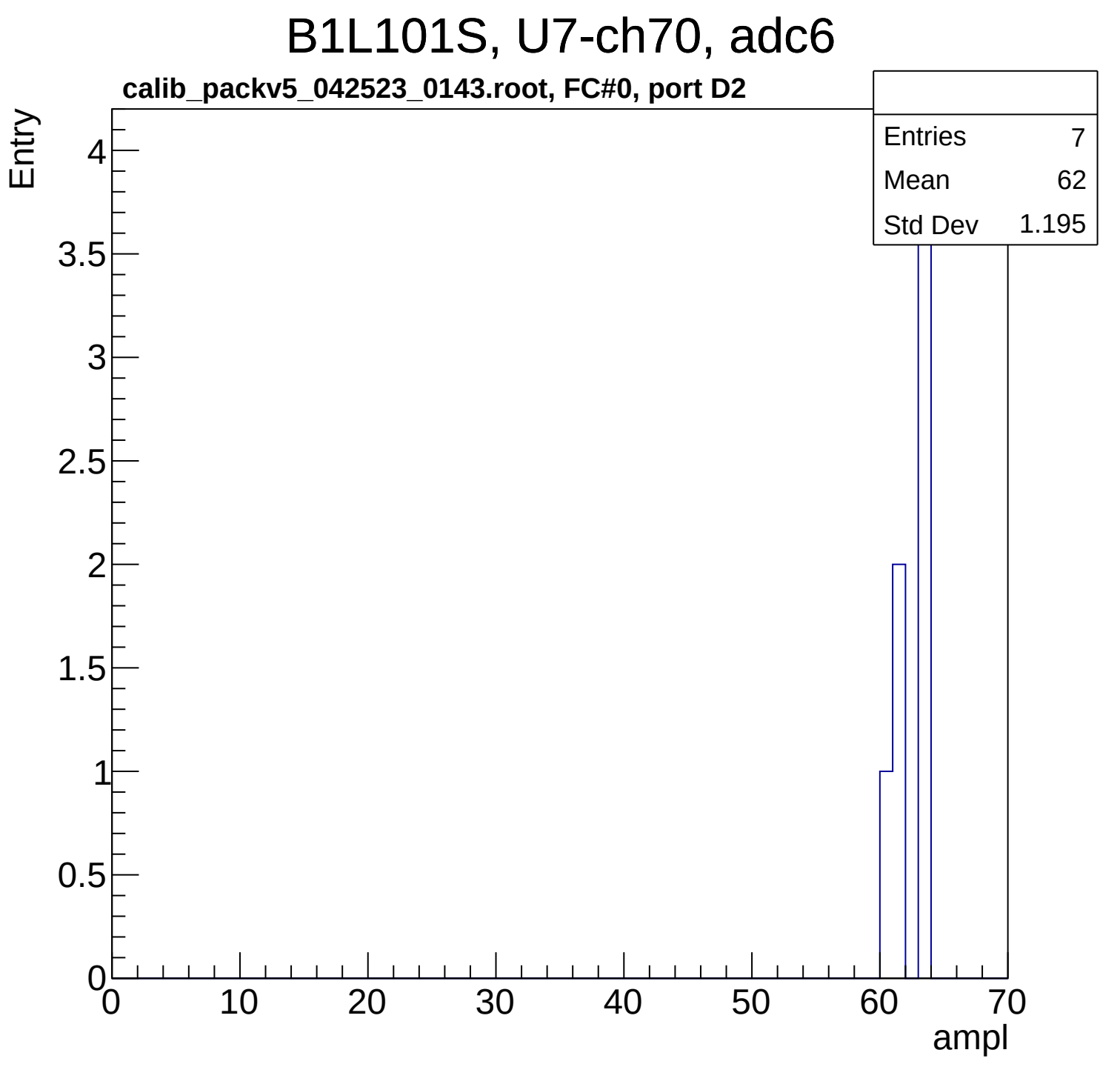

B1L101S, U7-ch70, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 48.57
Std Dev 3.693
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch70, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 53.78
Std Dev 3.399
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U7-ch70, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 58.13
Std Dev 8.061
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch70, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 62
Std Dev 1.195
Entry
ampl
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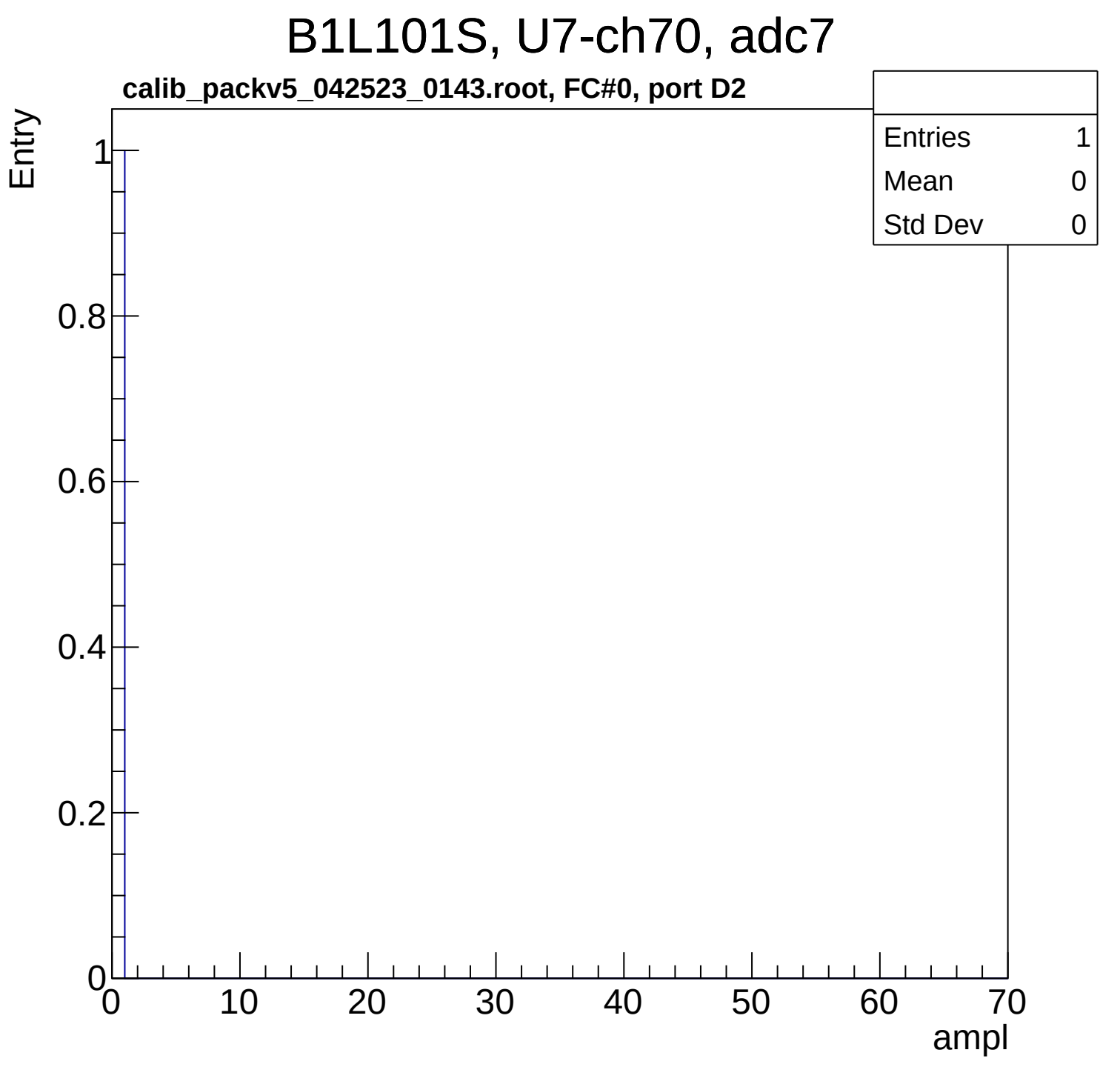
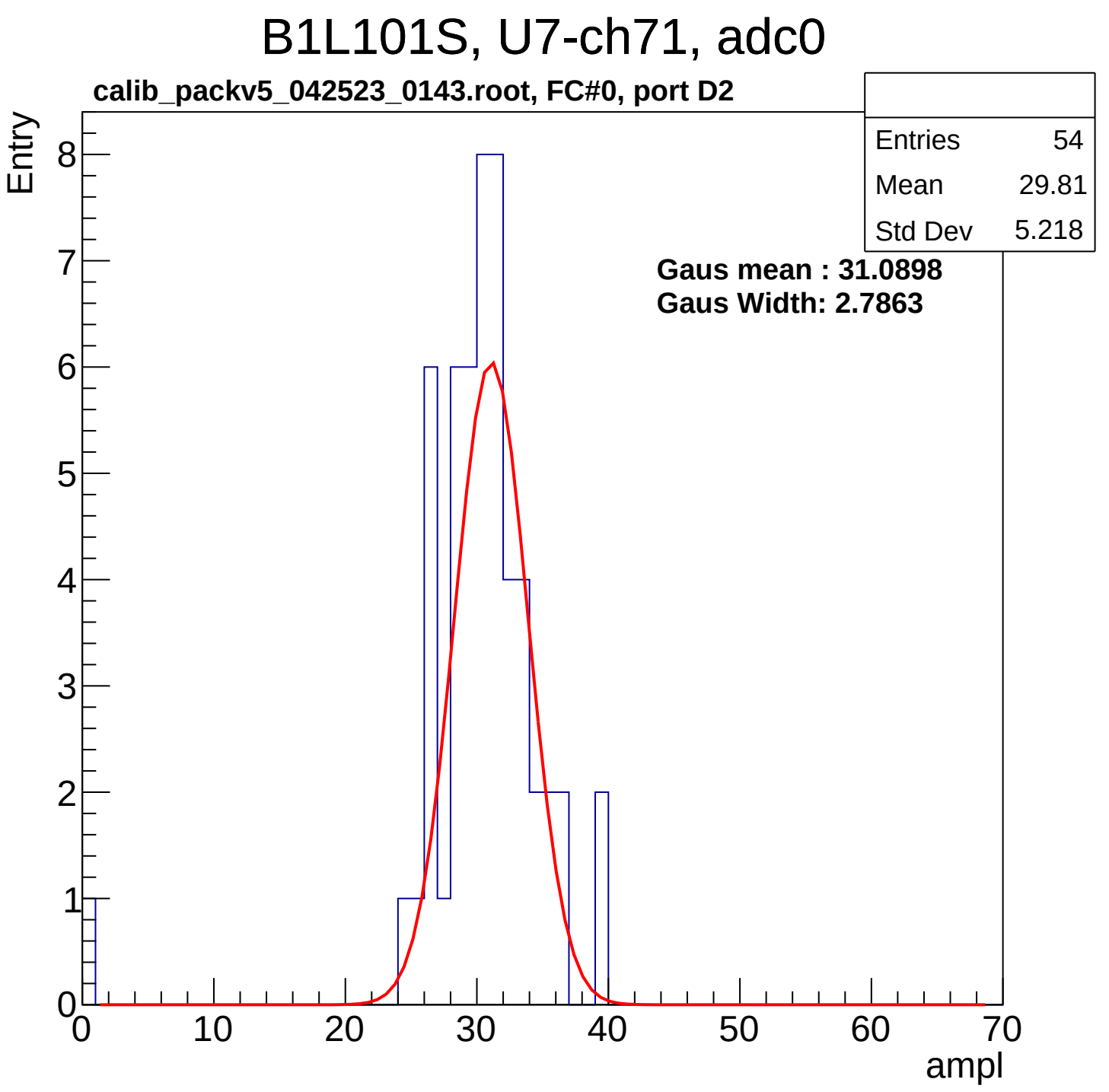
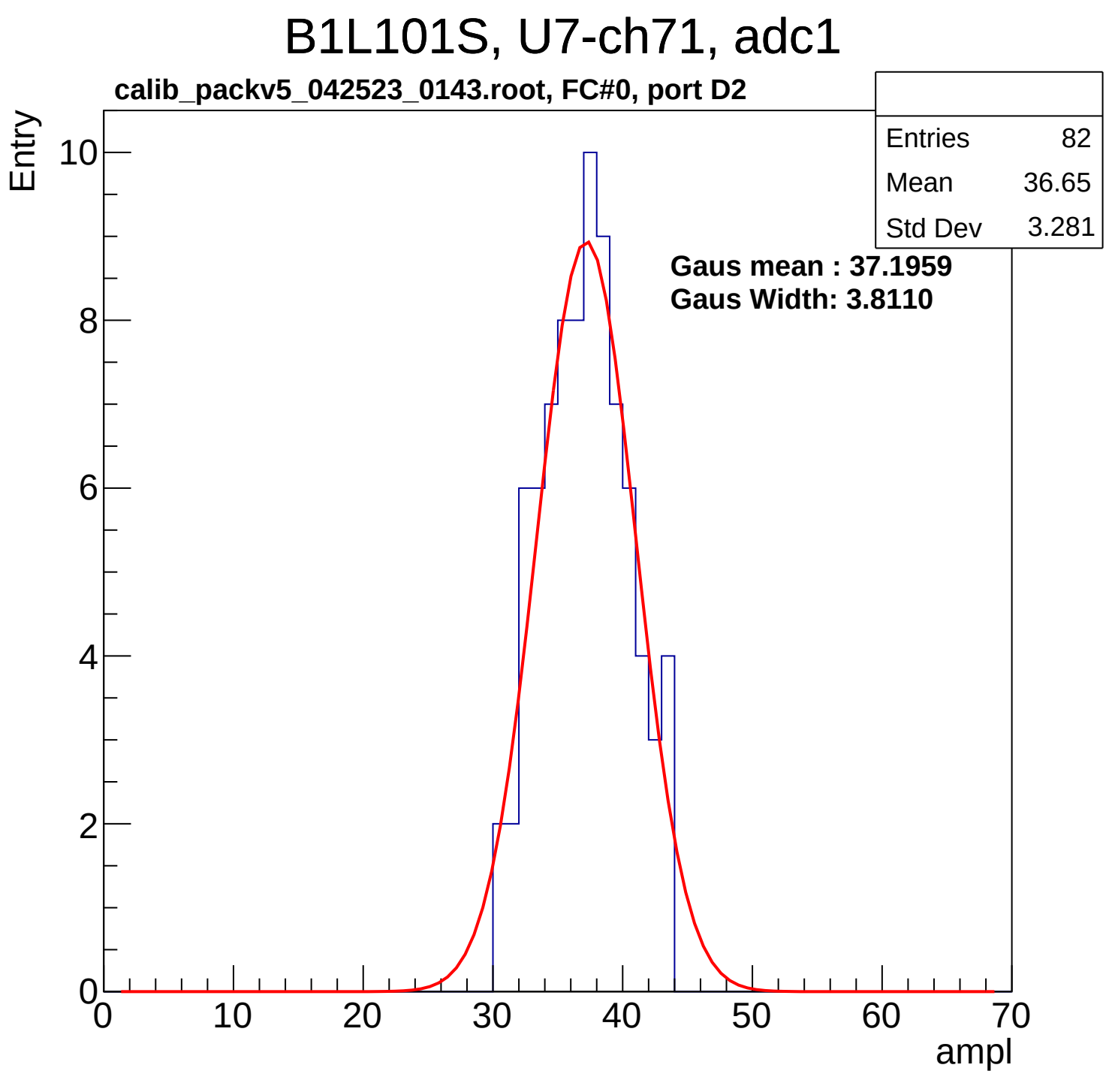
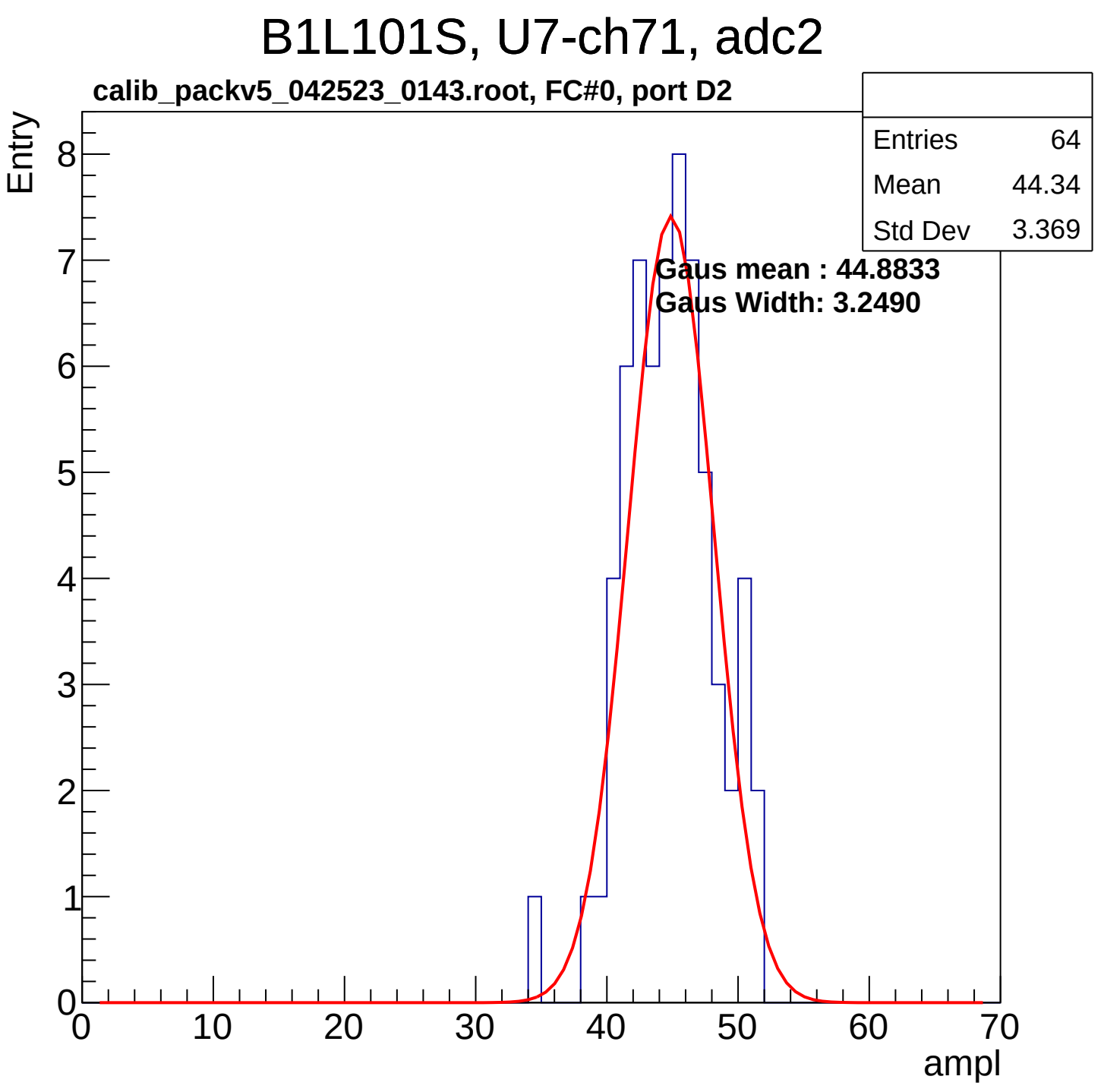
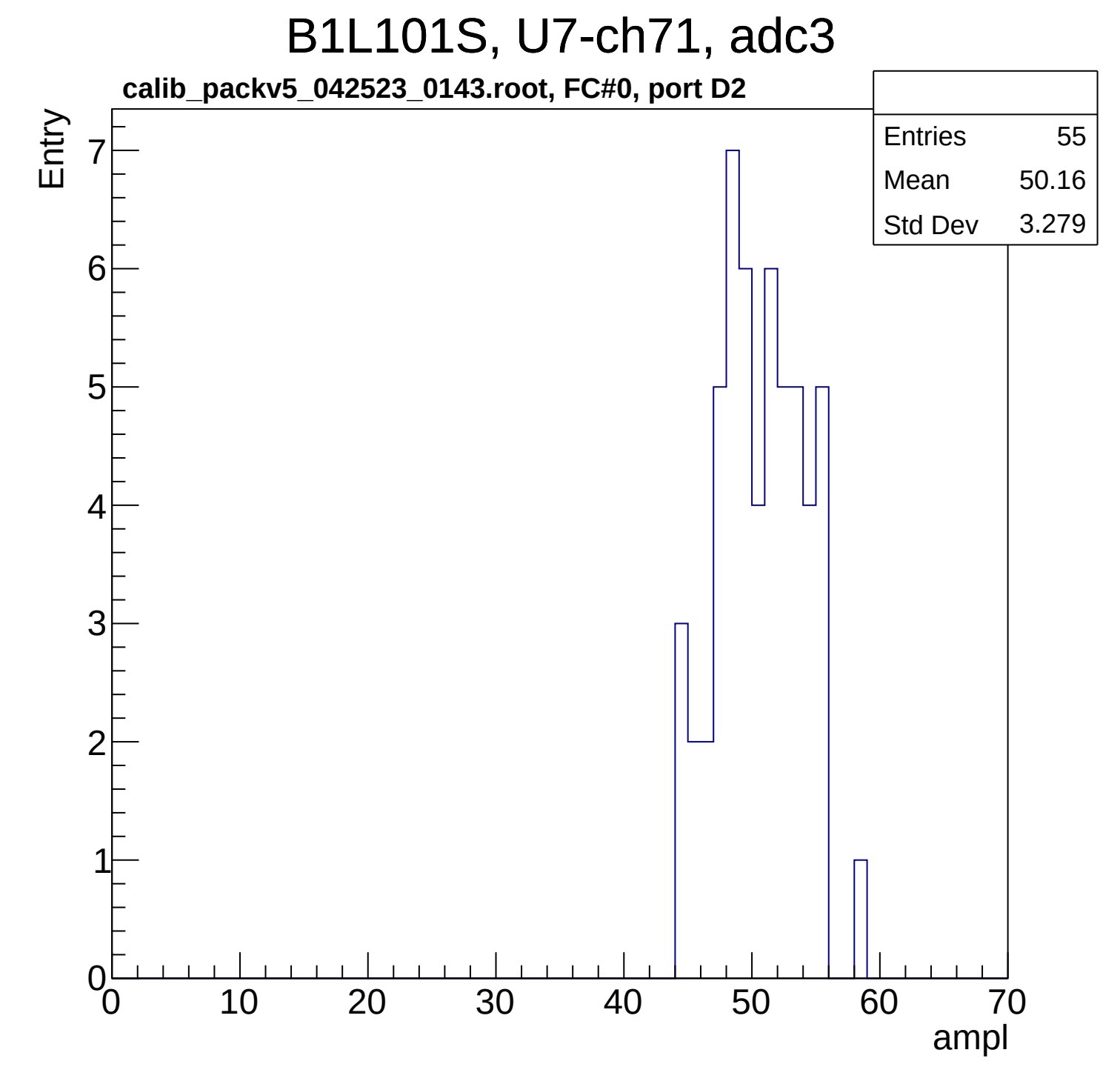
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

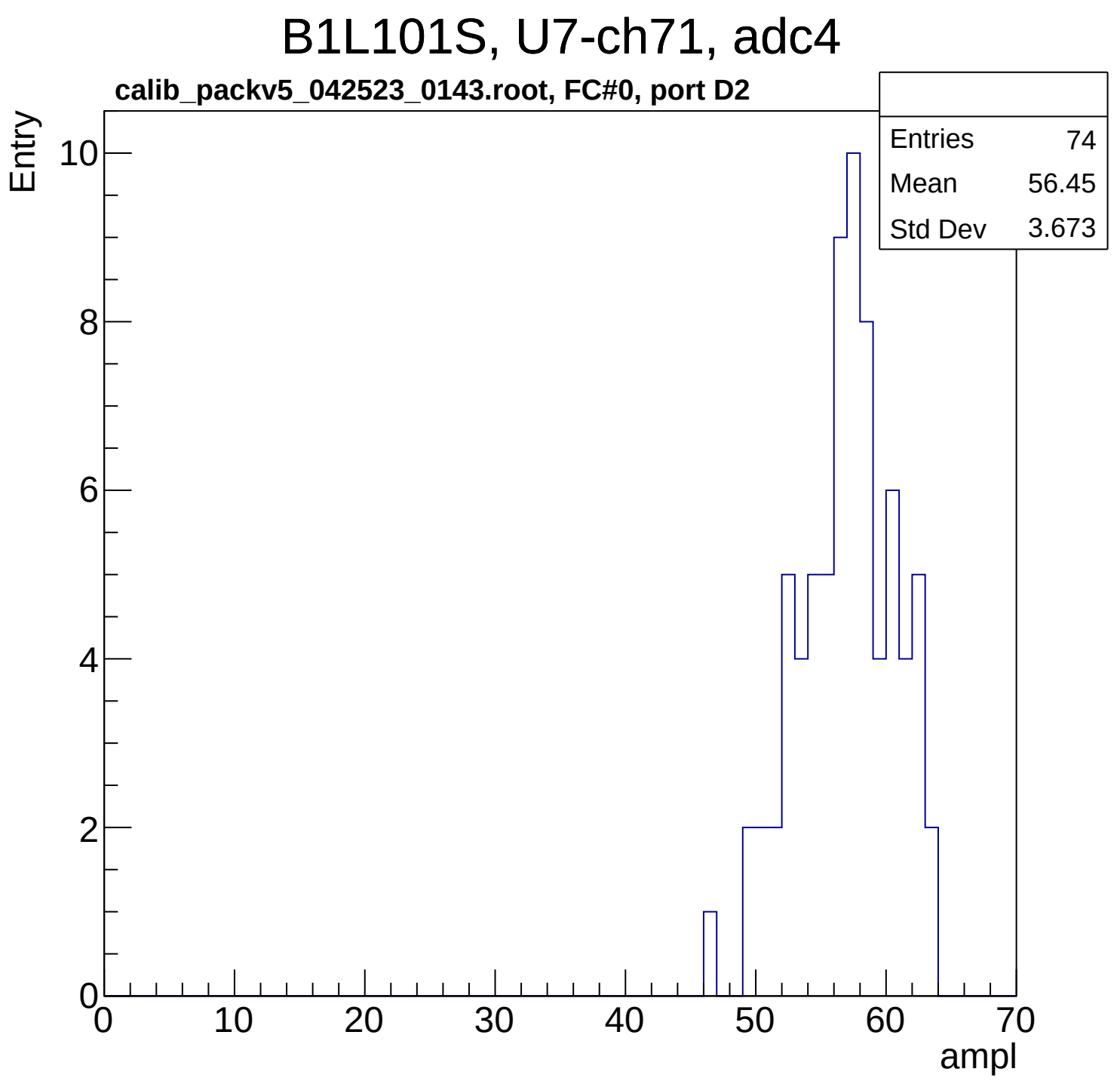

B1L101S, U7-ch70, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

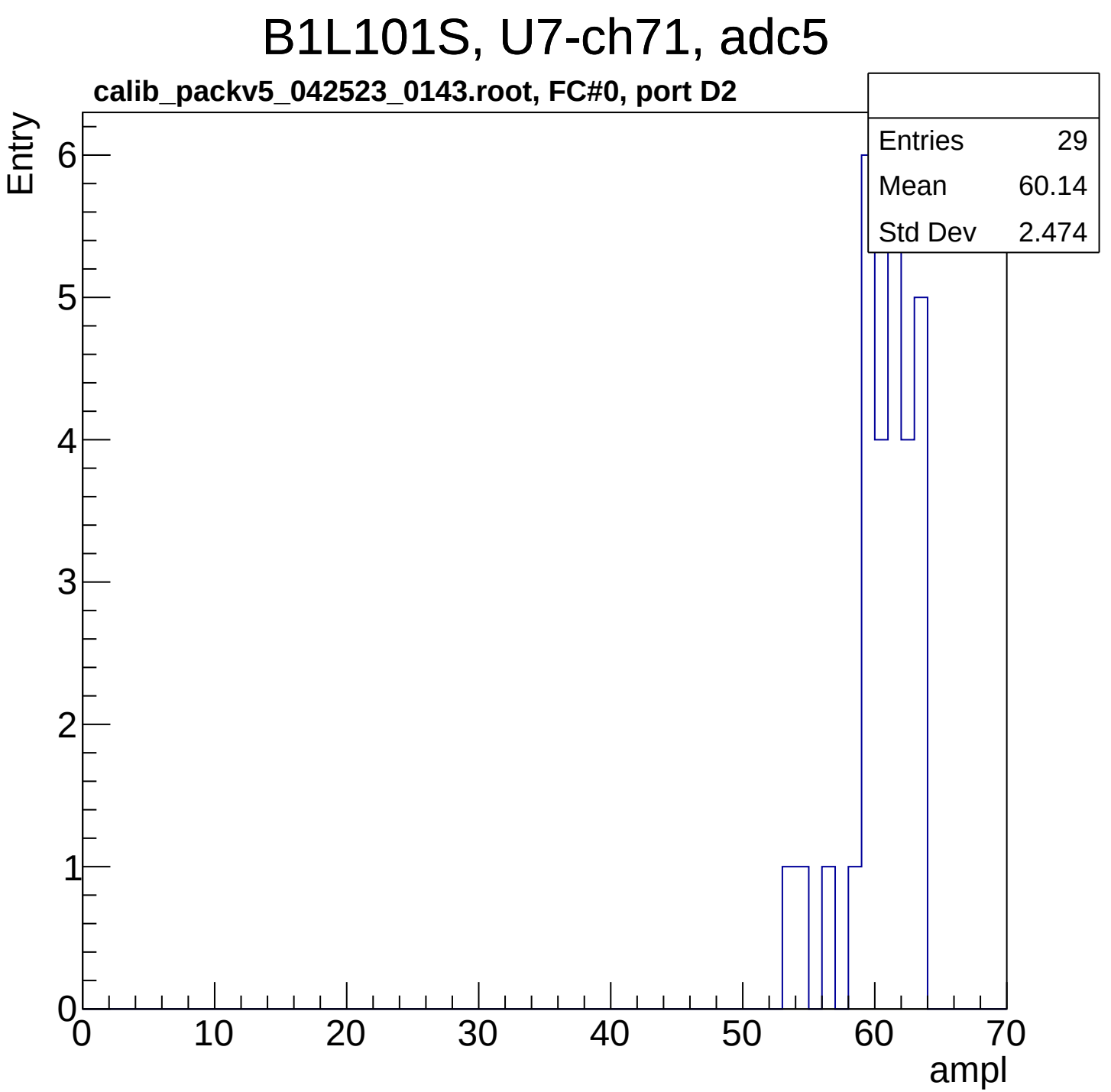

B1L101S, U7-ch71, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 29.81
Std Dev 5.218
Gaus mean : 31.0898
Gaus Width: 2.7863
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

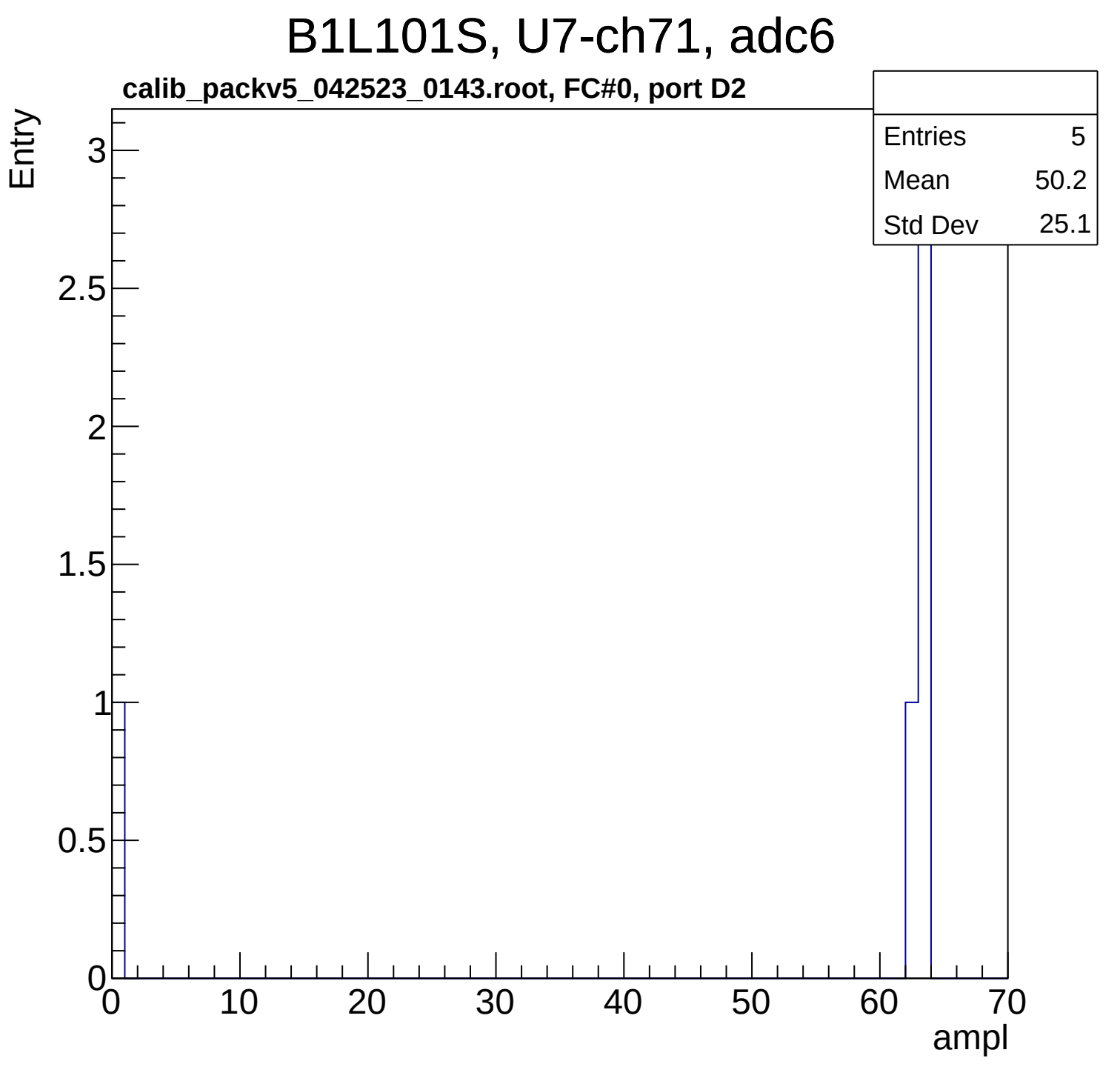

B1L101S, U7-ch71, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 82
Mean 36.65
Std Dev 3.281
Gaus mean : 37.1959
Gaus Width: 3.8110
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch71, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 44.34
Std Dev 3.369
Gaus mean : 44.8833
Gaus Width: 3.2490
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch71, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 50.16
Std Dev 3.279
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U7-ch71, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 56.45
Std Dev 3.673
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch71, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 29
Mean 60.14
Std Dev 2.474
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L101S, U7-ch71, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 50.2
Std Dev 25.1
Entry
ampl
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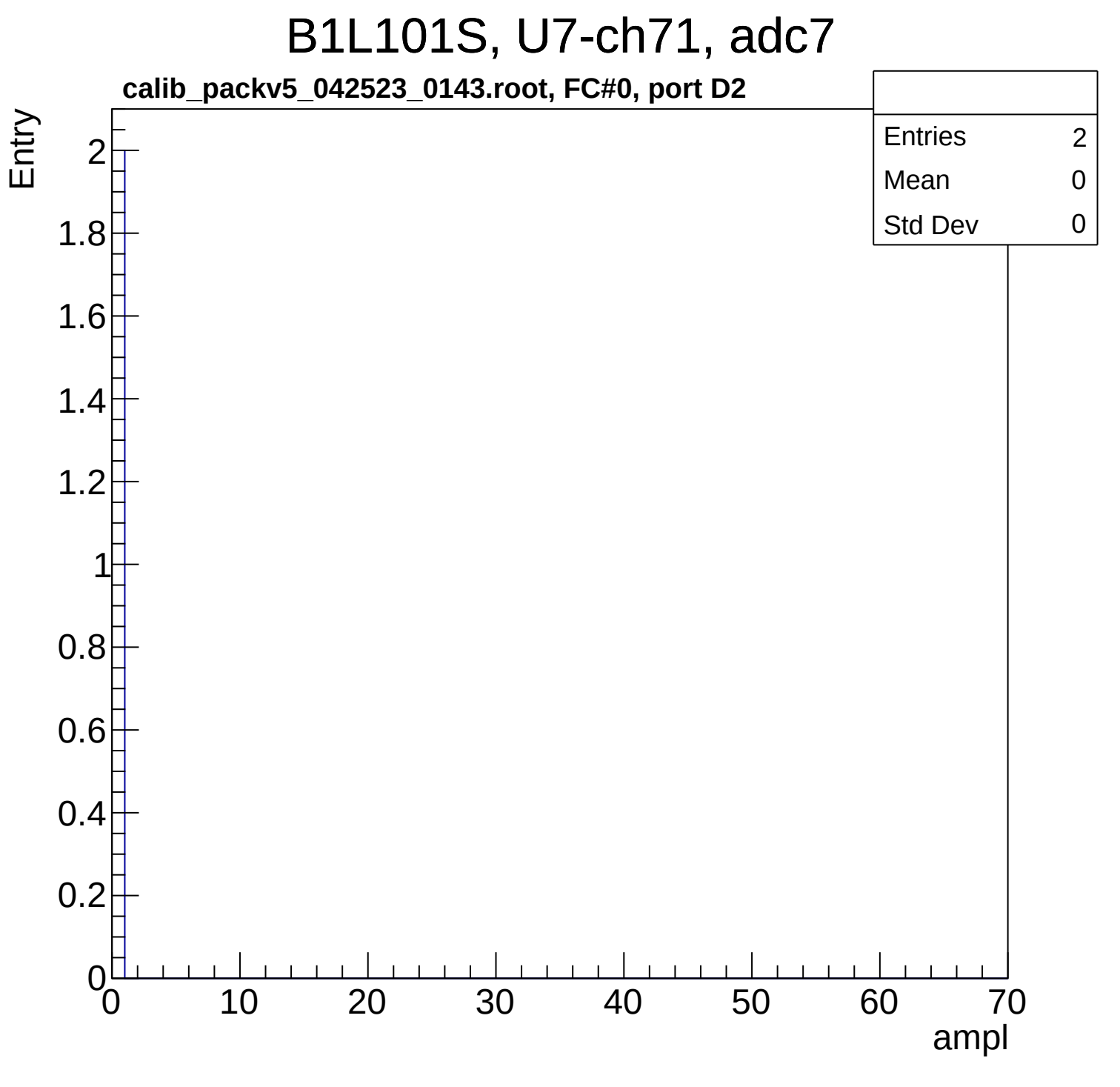
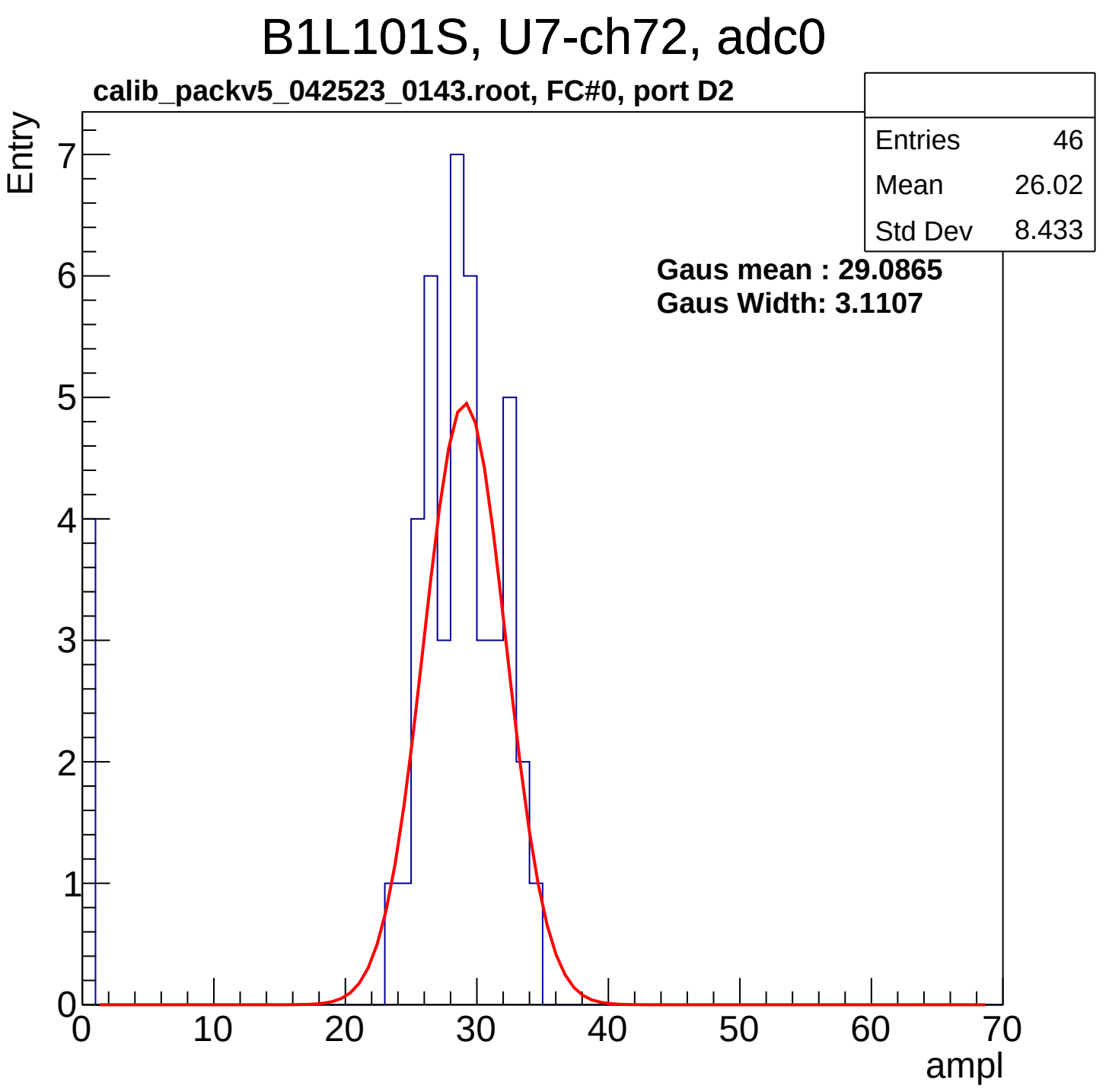
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U7-ch71, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U7-ch72, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 26.02
Std Dev 8.433
Gaus mean : 29.0865
Gaus Width: 3.1107
Entry
ampl
0
1
2
3
4
5
6
7
0
10
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40
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60
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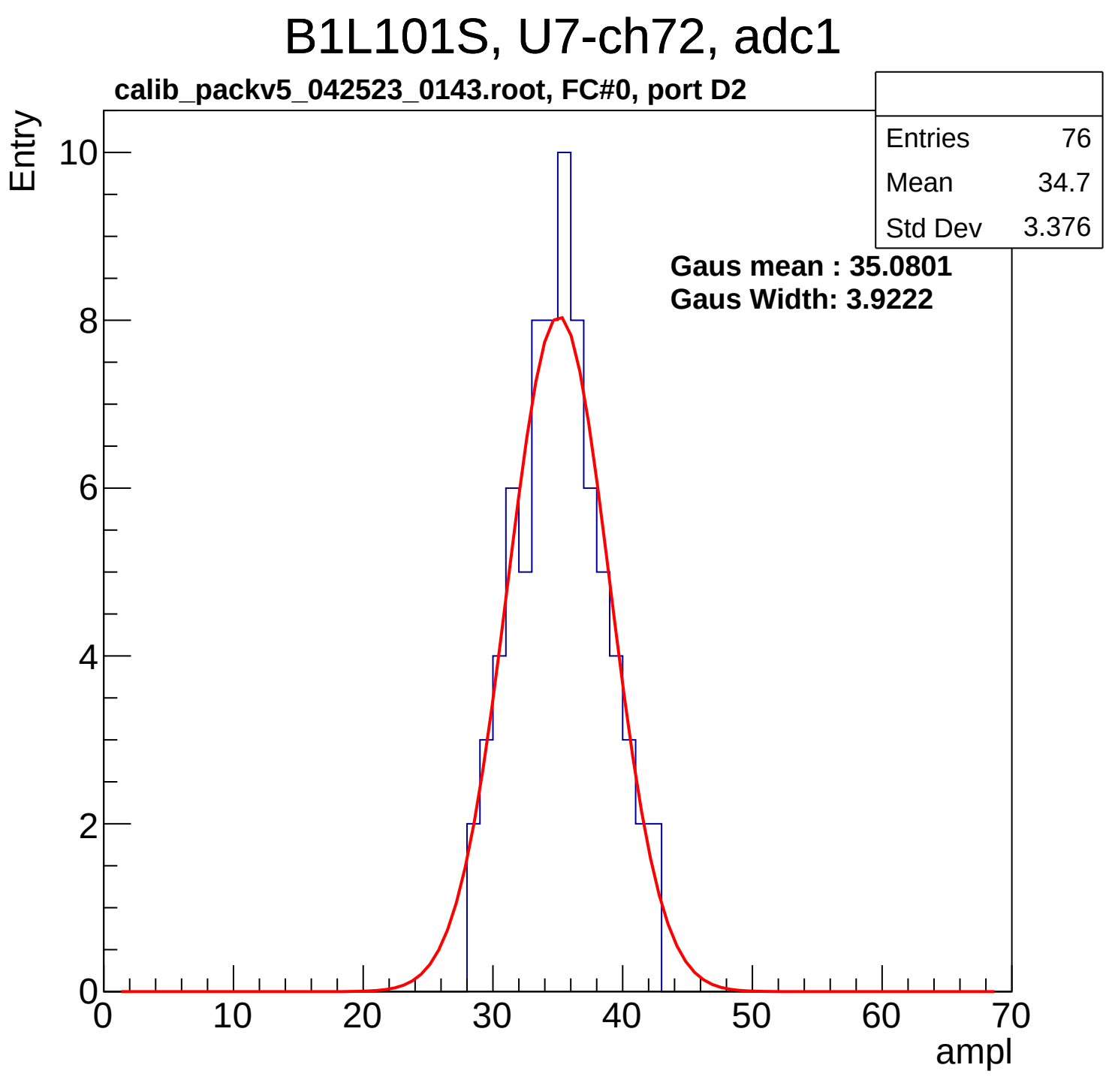
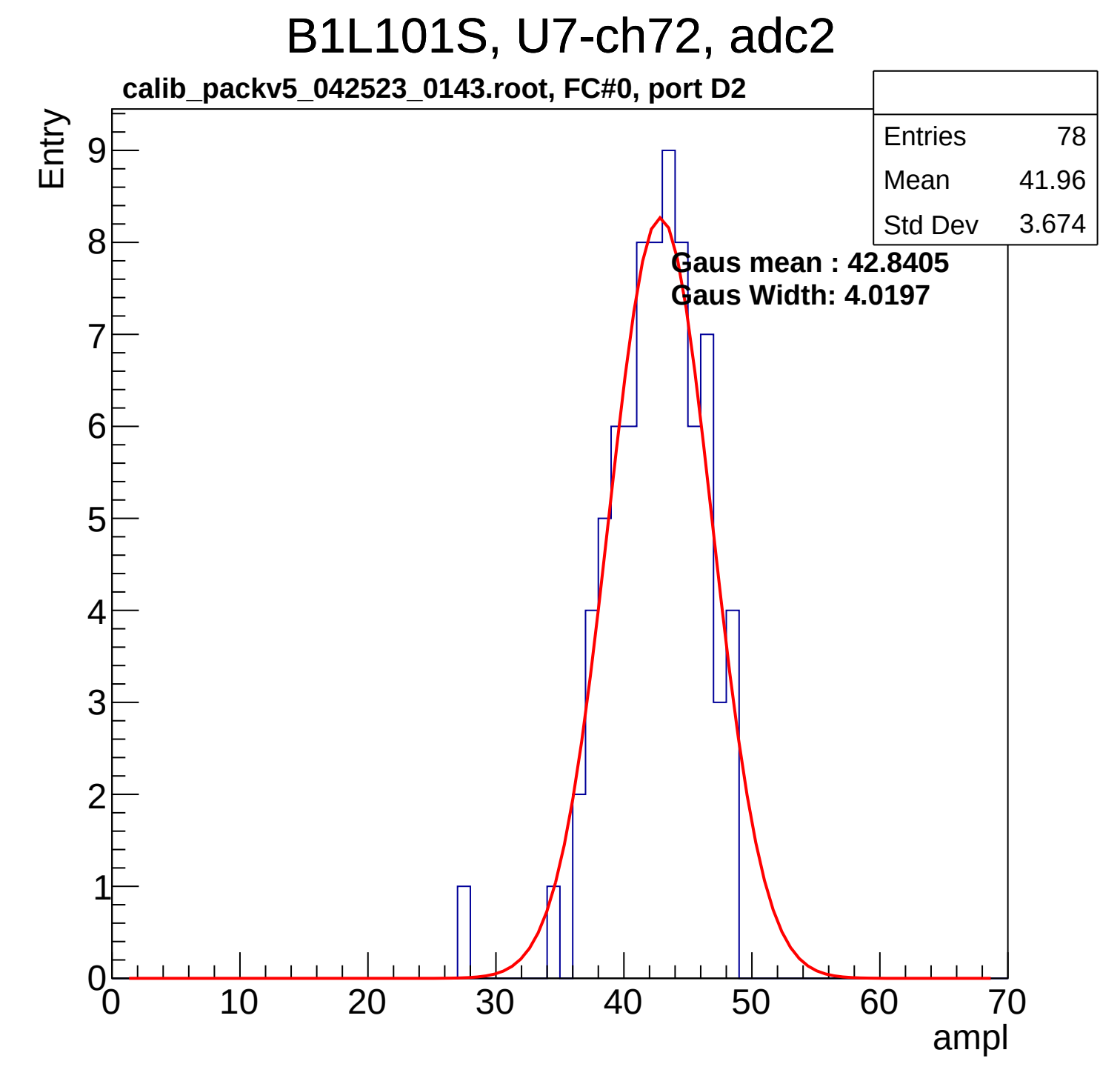
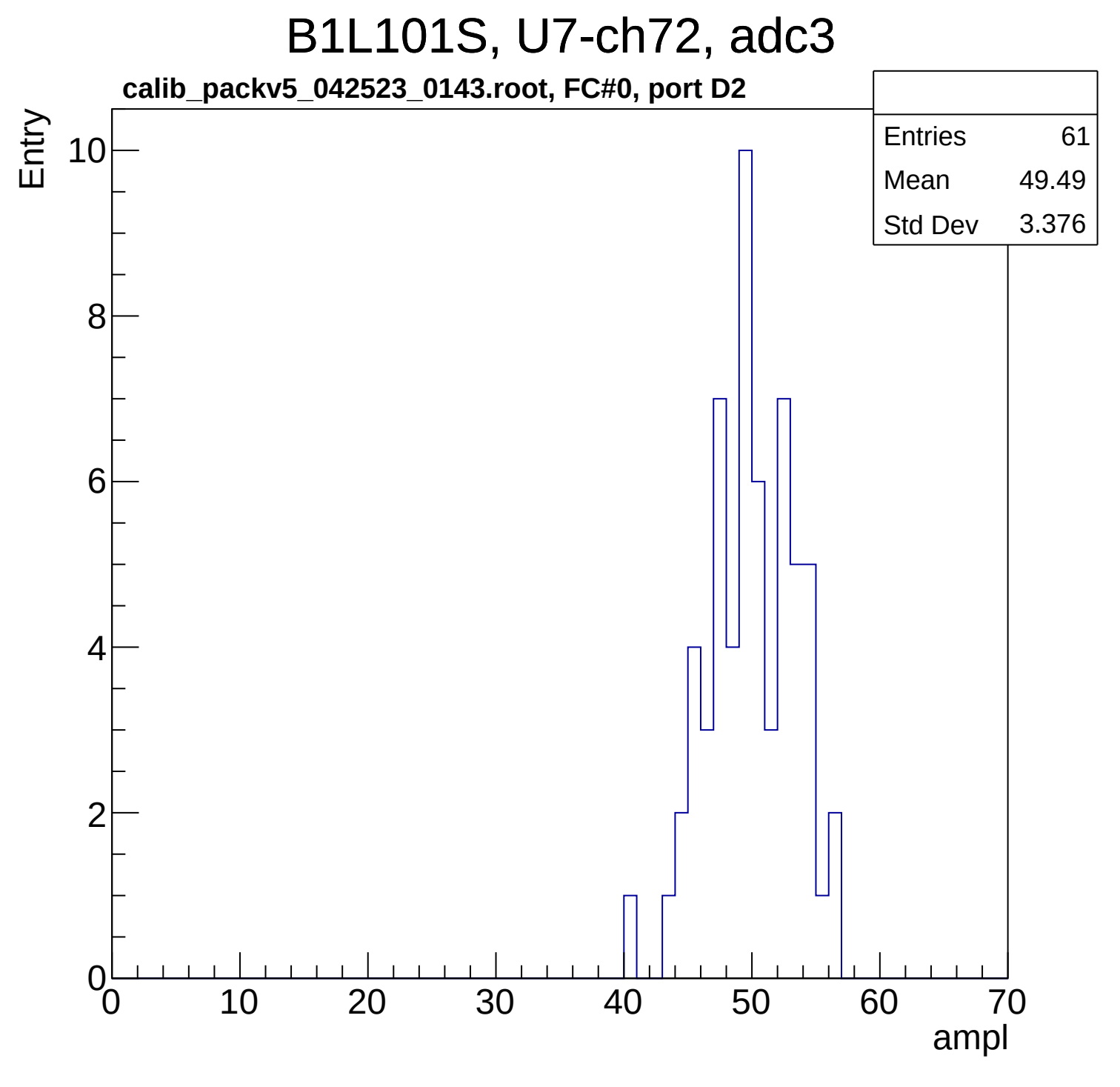
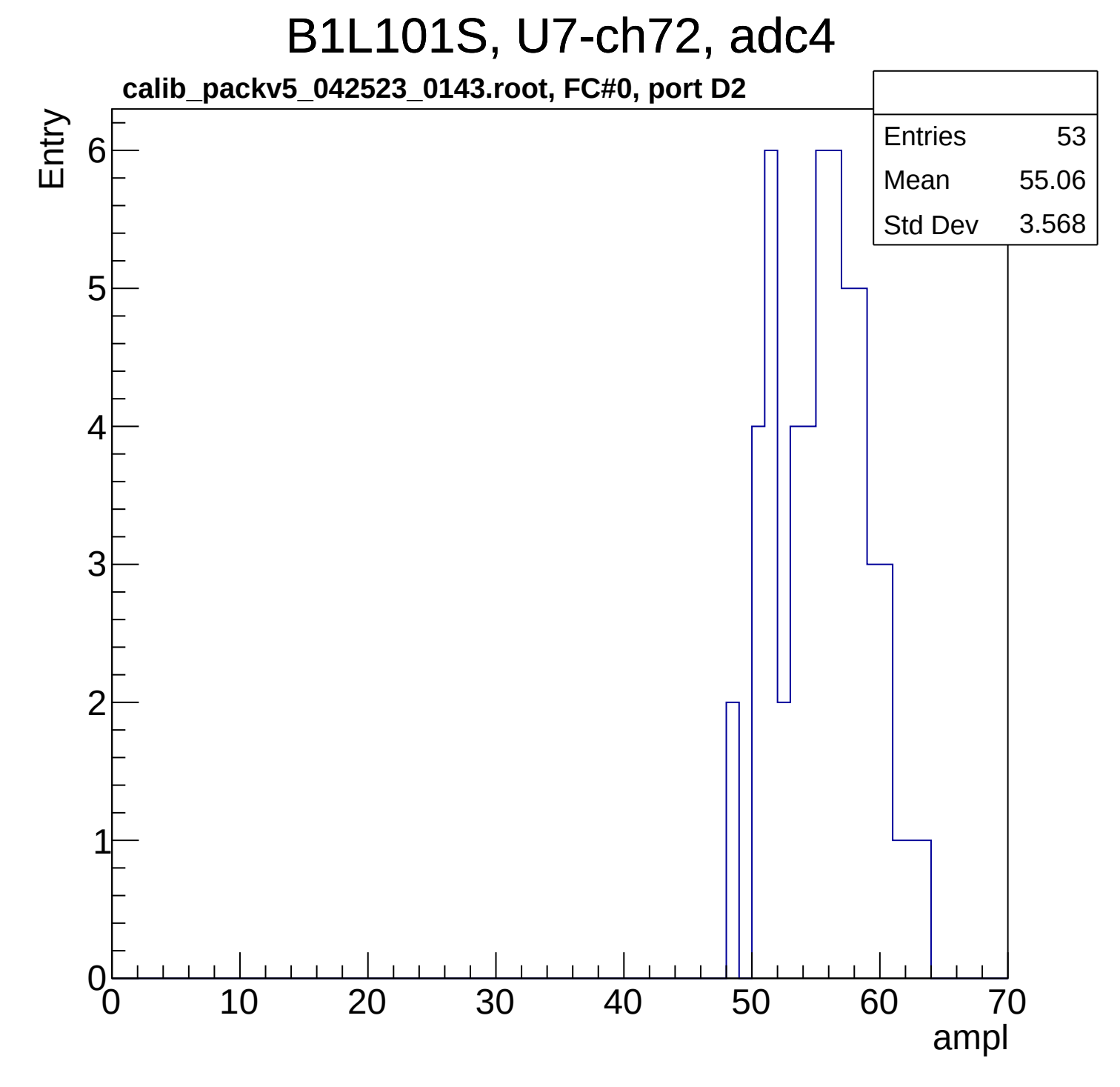
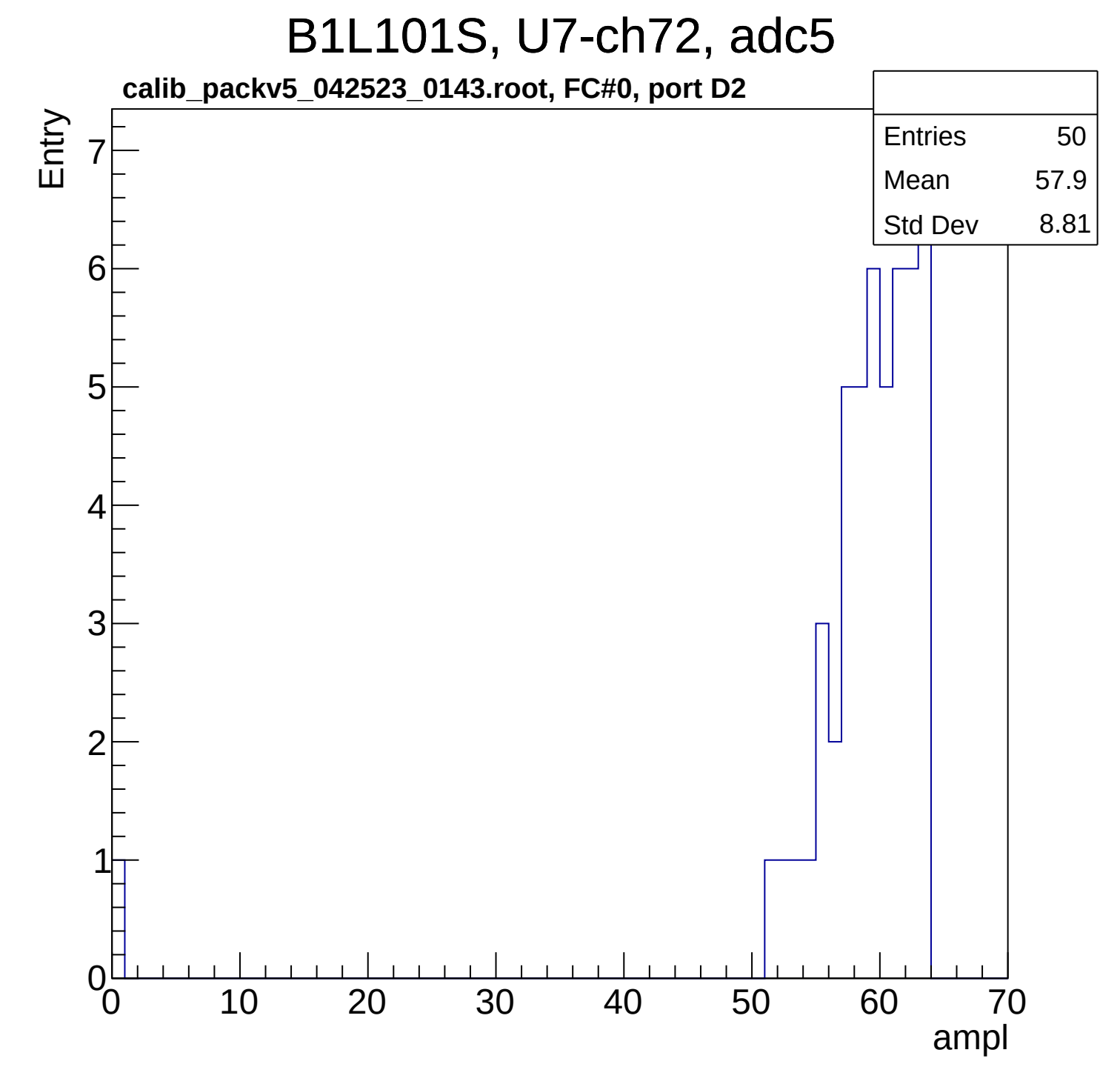
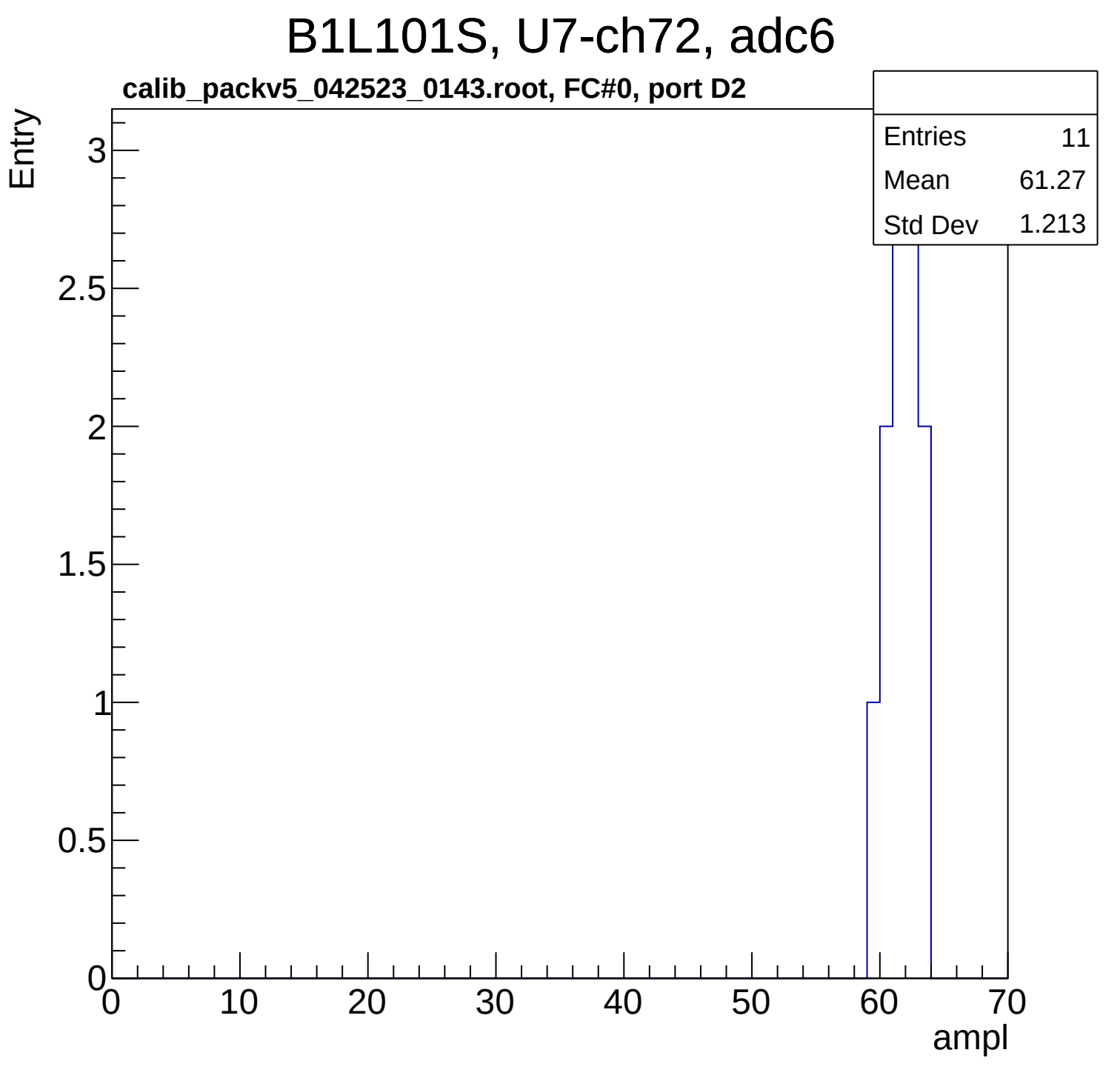

B1L101S, U7-ch72, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 34.7
Std Dev 3.376
Gaus mean : 35.0801
Gaus Width: 3.9222
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch72, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 41.96
Std Dev 3.674
Gaus mean : 42.8405
Gaus Width: 4.0197
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch72, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 49.49
Std Dev 3.376
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch72, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 55.06
Std Dev 3.568
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L101S, U7-ch72, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 57.9
Std Dev 8.81
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U7-ch72, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 11
Mean 61.27
Std Dev 1.213
Entry
ampl
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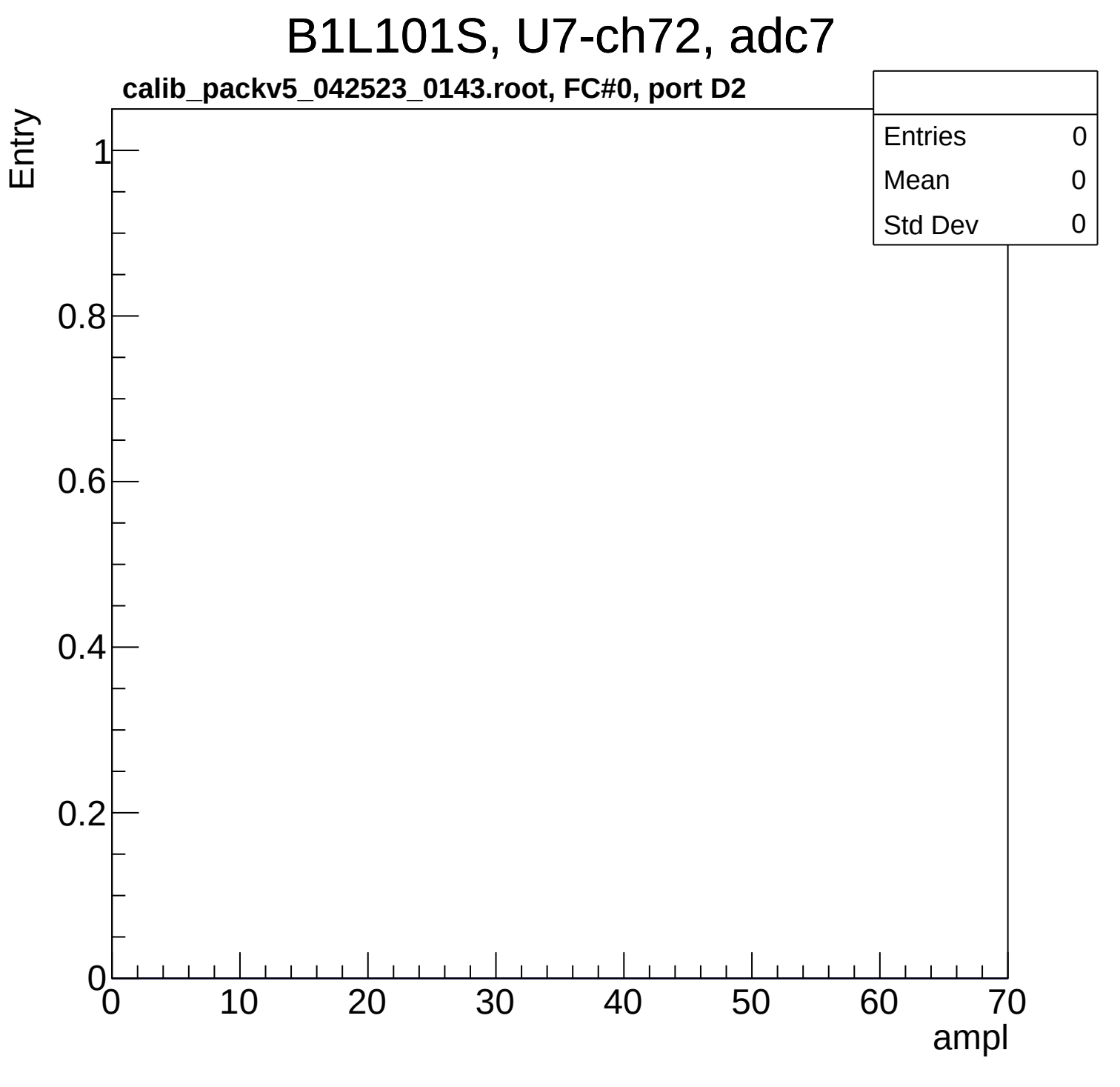
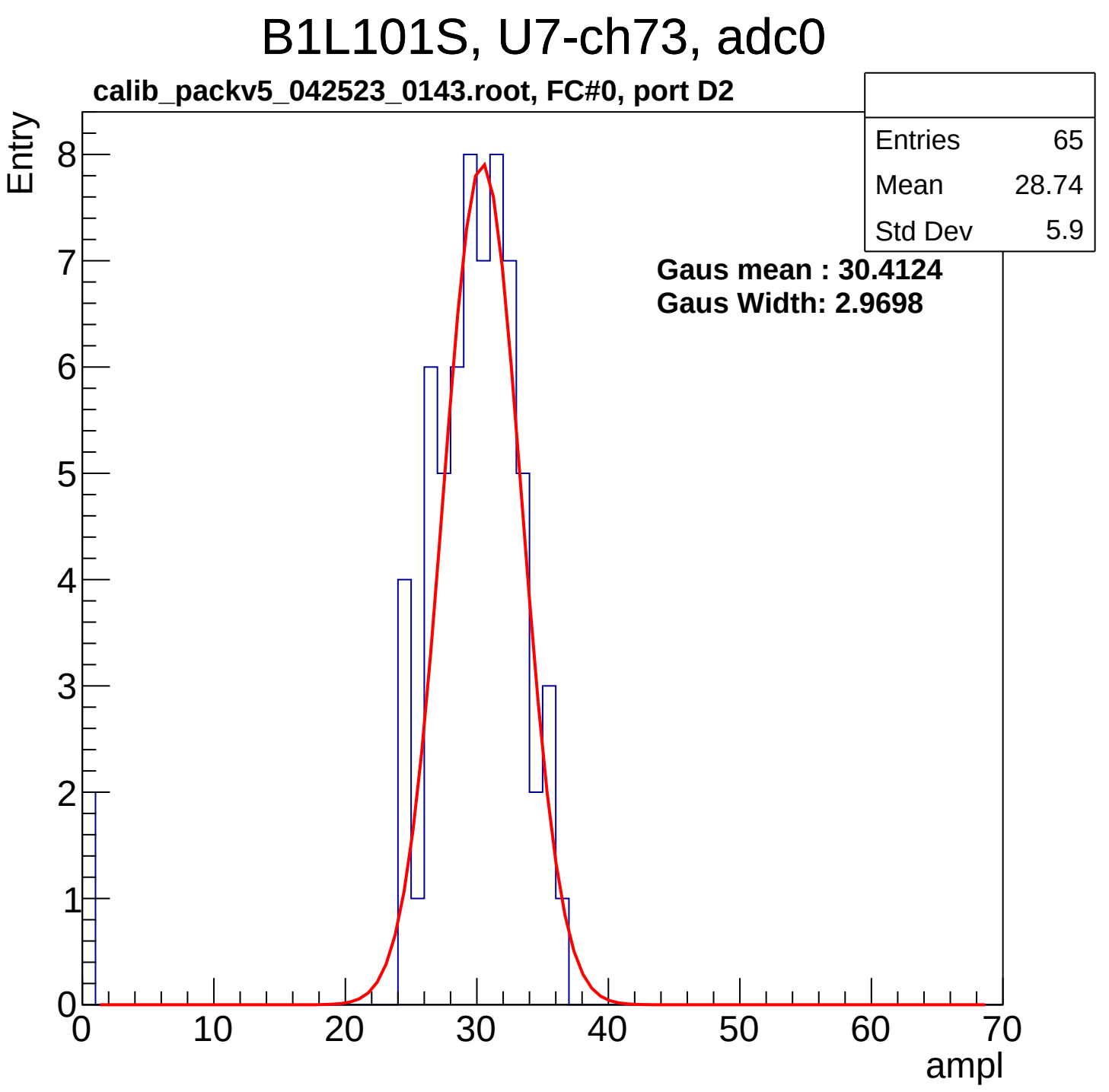
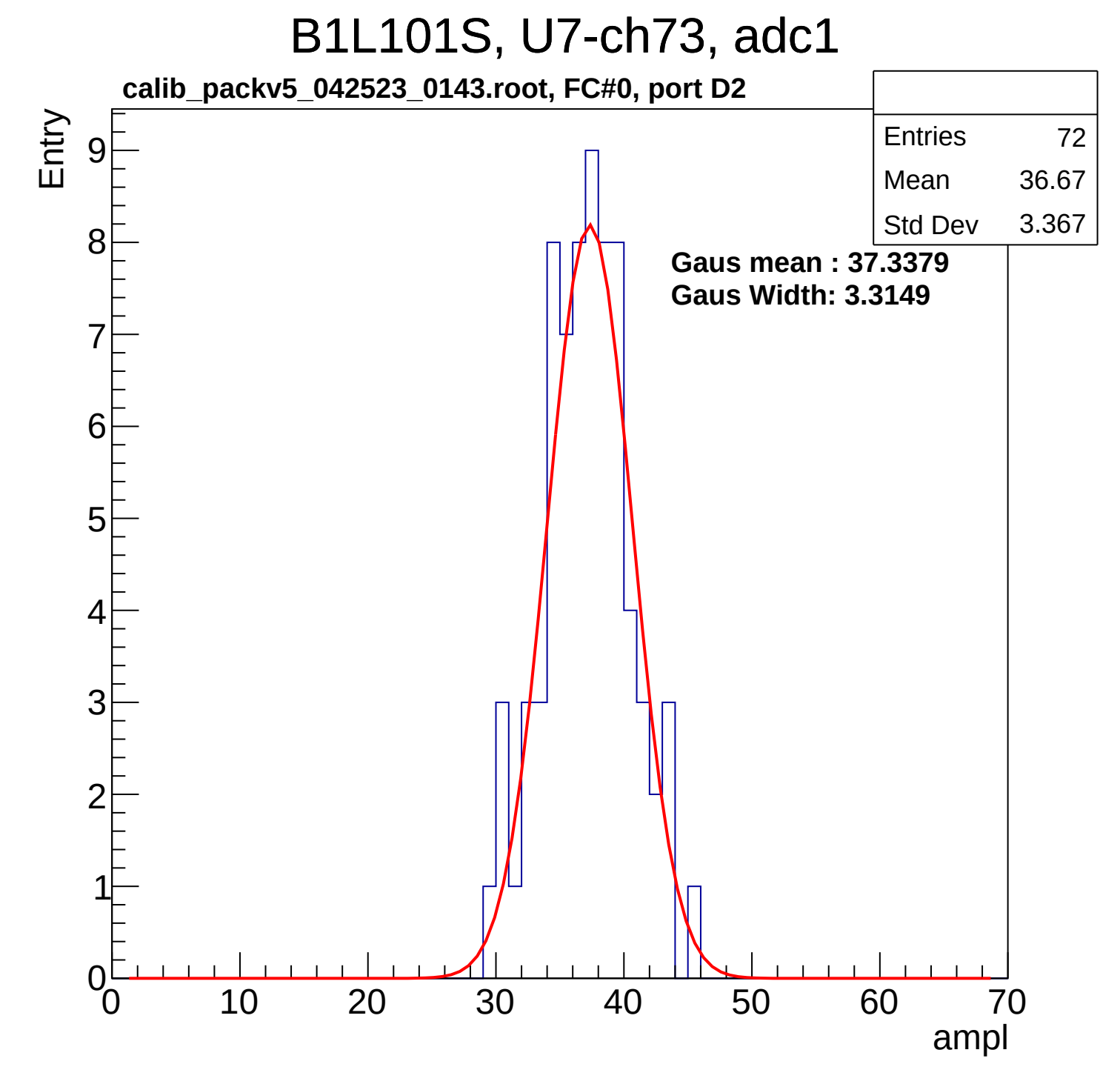
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U7-ch72, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch73, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 28.74
Std Dev 5.9
Gaus mean : 30.4124
Gaus Width: 2.9698
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch73, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 36.67
Std Dev 3.367
Gaus mean : 37.3379
Gaus Width: 3.3149
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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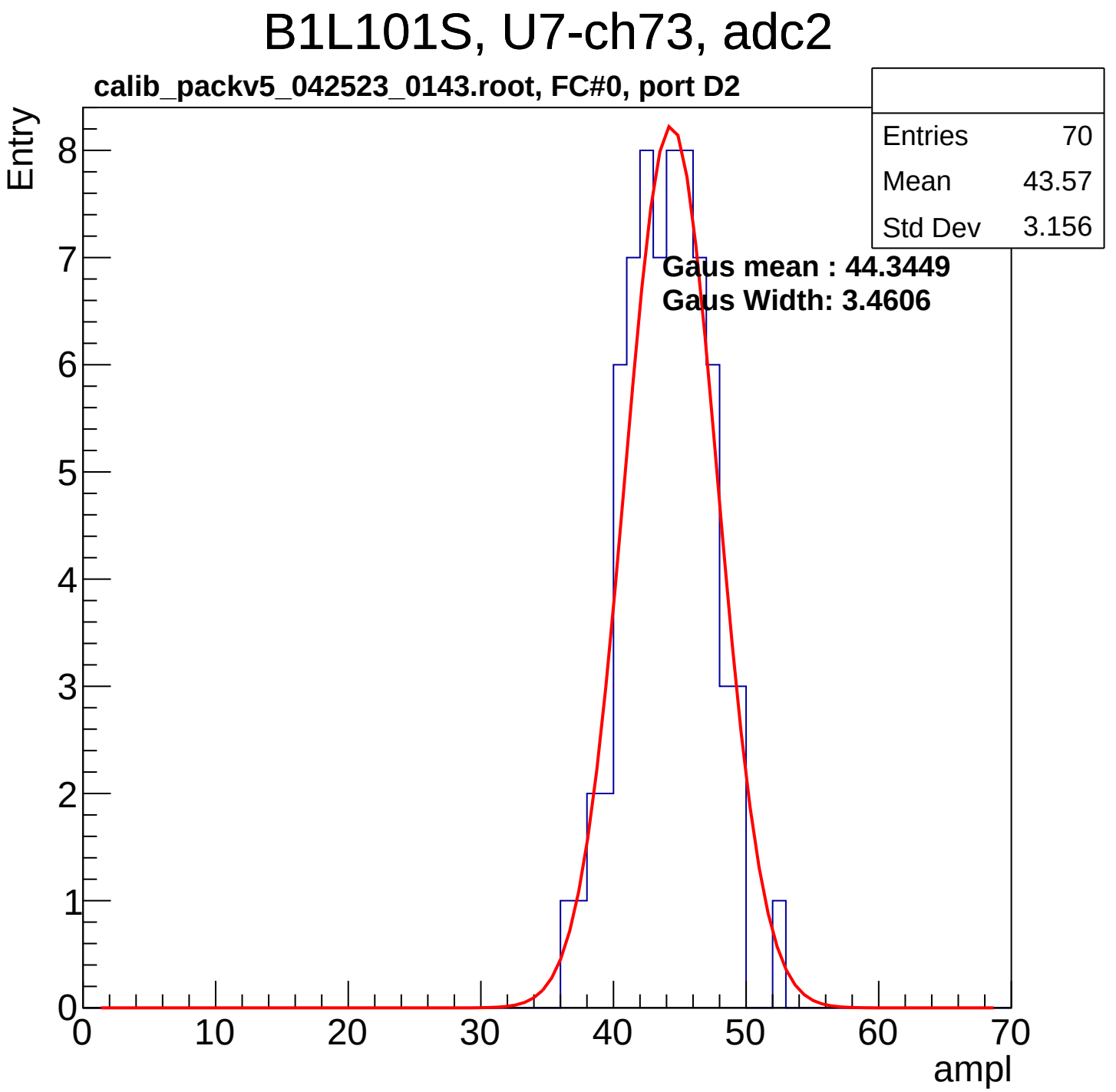
B1L101S, U7-ch73, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 43.57
Std Dev 3.156
Gaus mean : 44.3449
Gaus Width: 3.4606
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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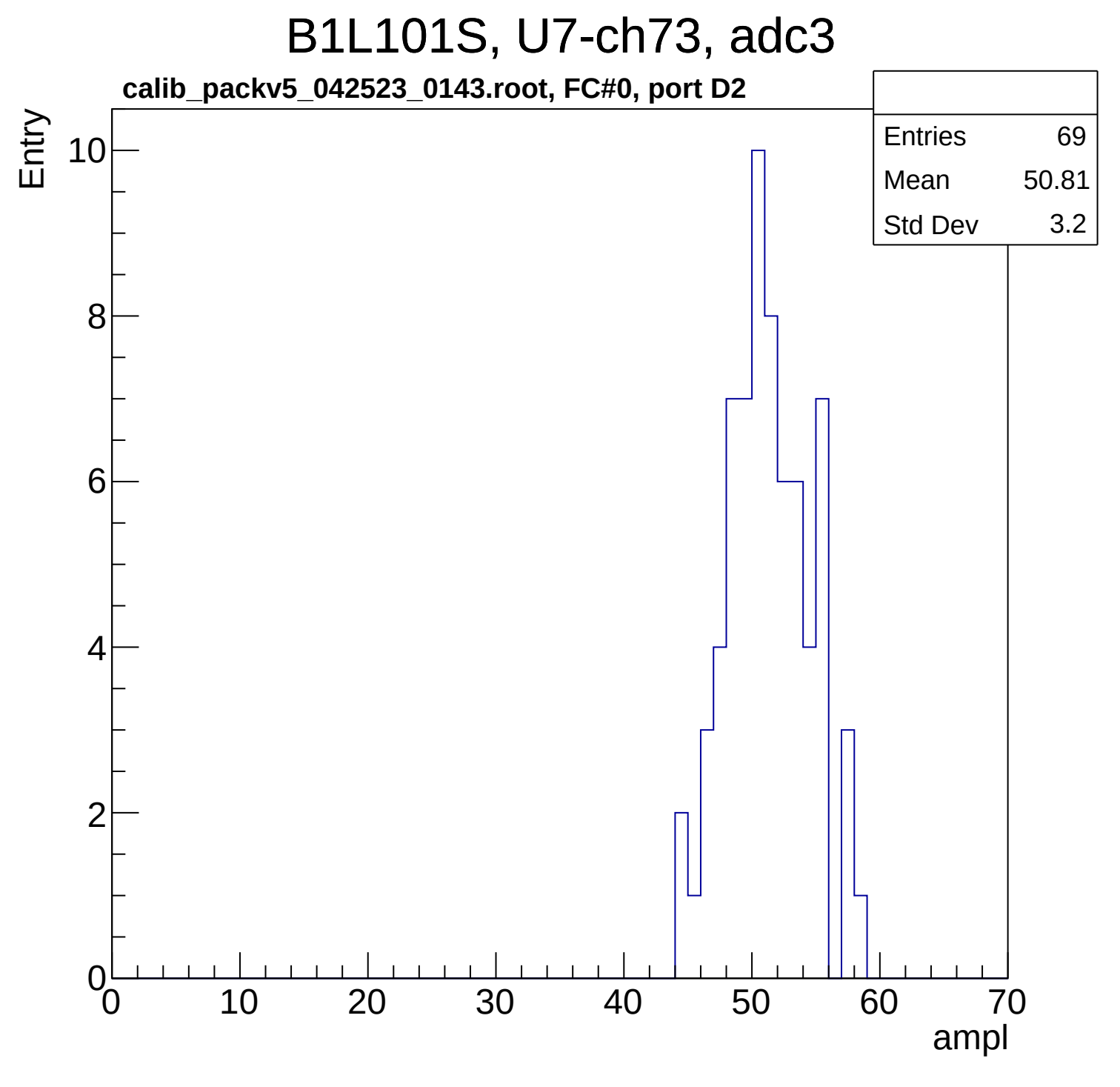
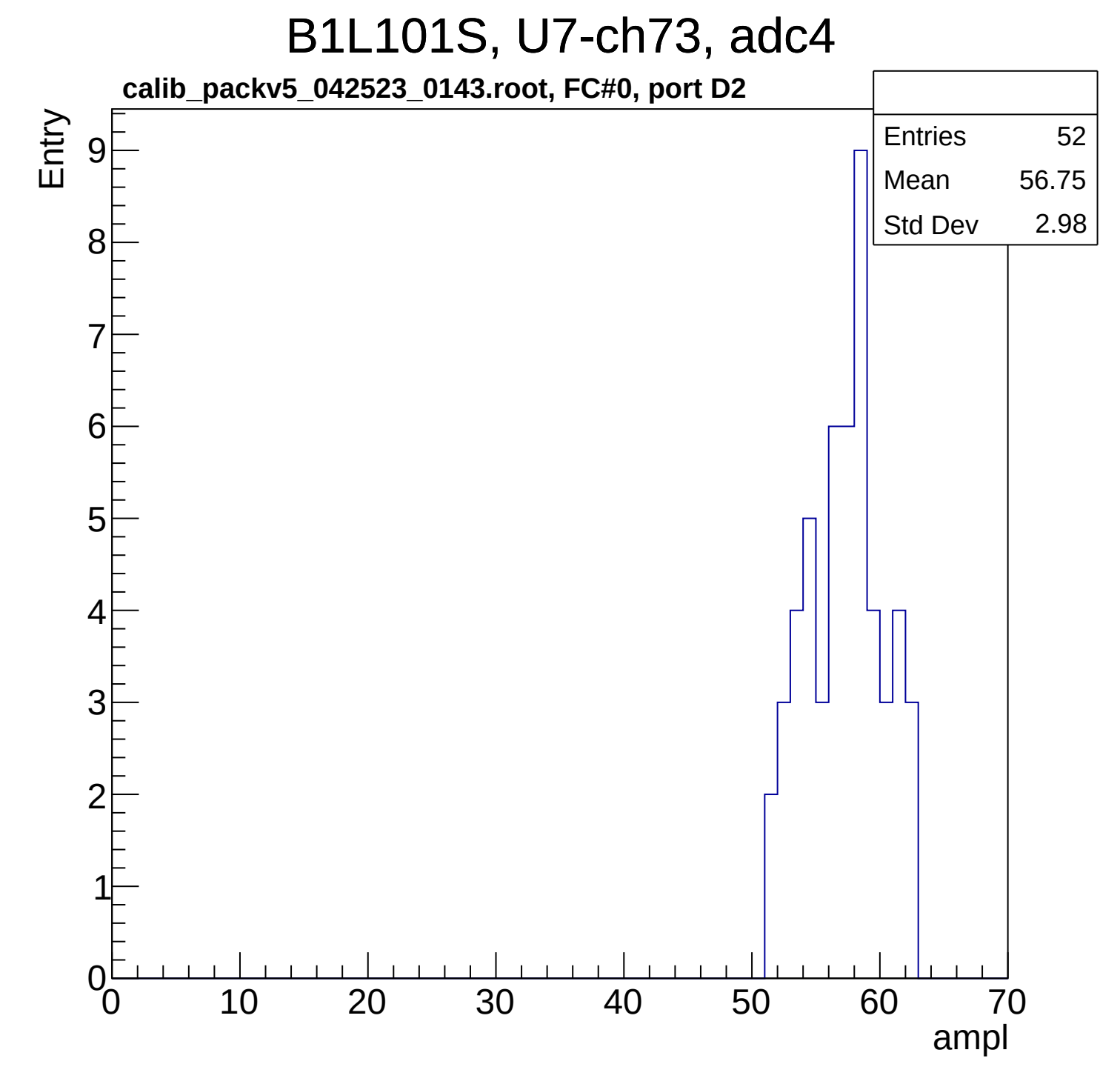
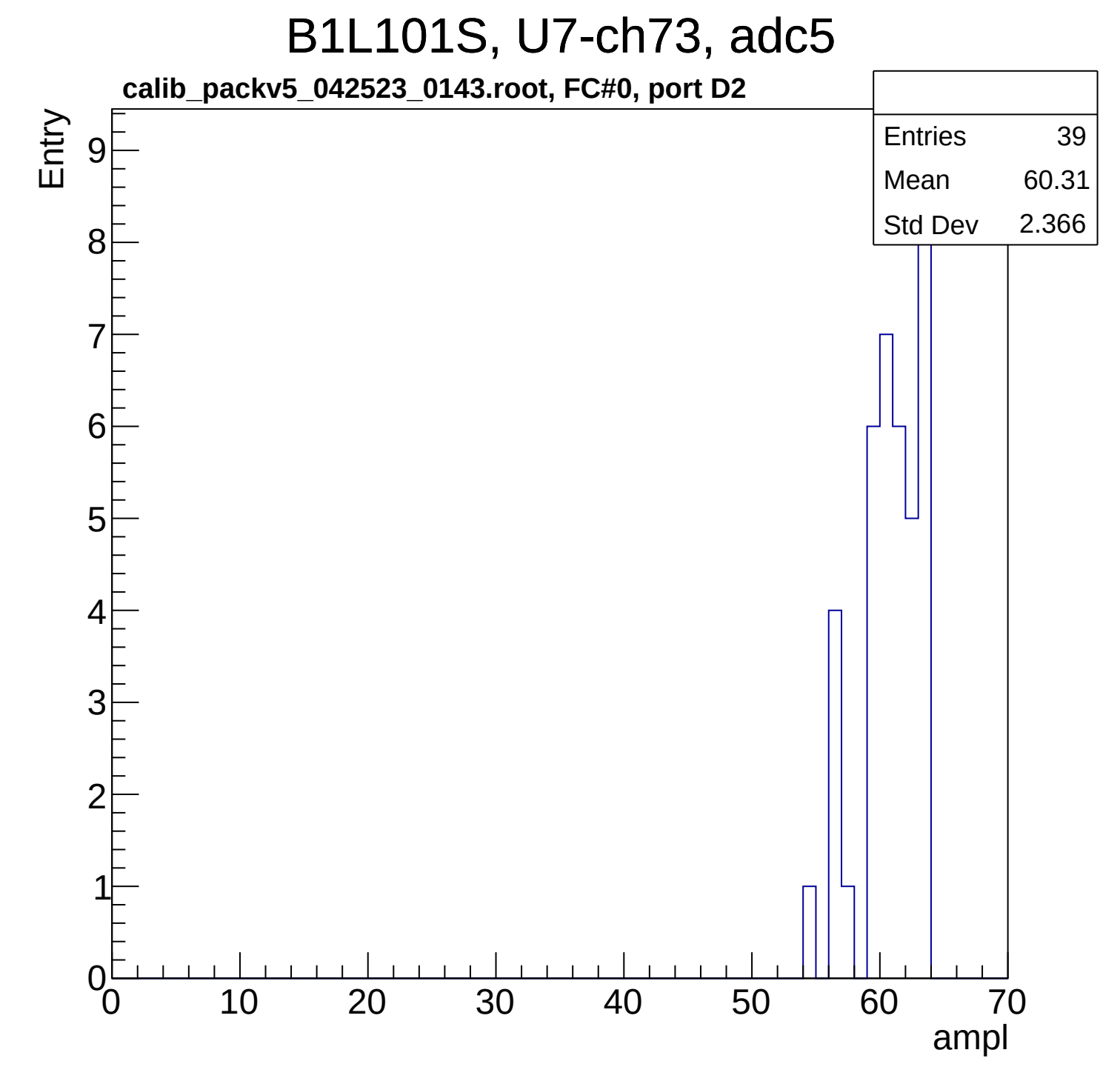

B1L101S, U7-ch73, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 50.81
Std Dev 3.2
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch73, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 56.75
Std Dev 2.98
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch73, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 39
Mean 60.31
Std Dev 2.366
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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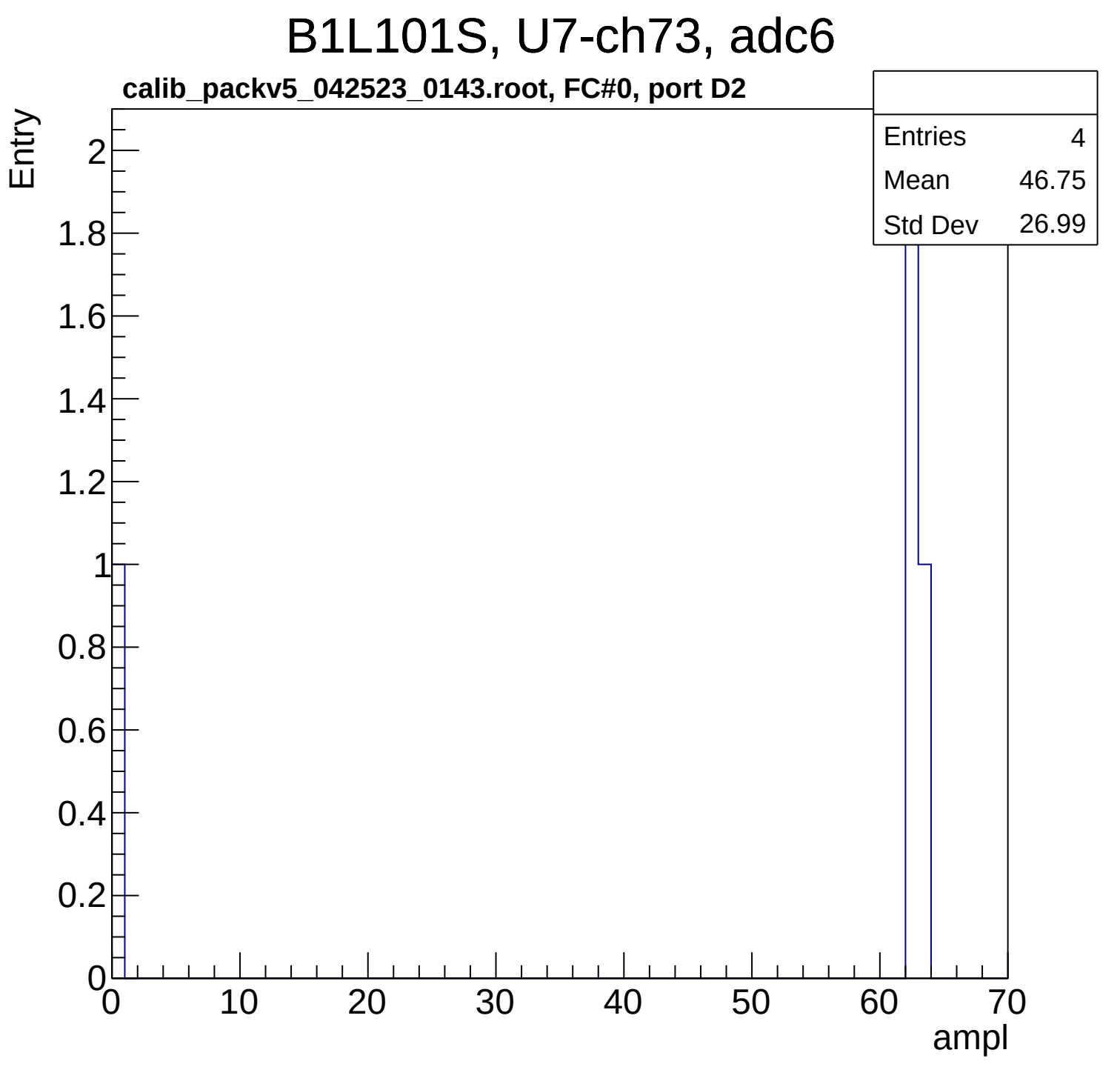
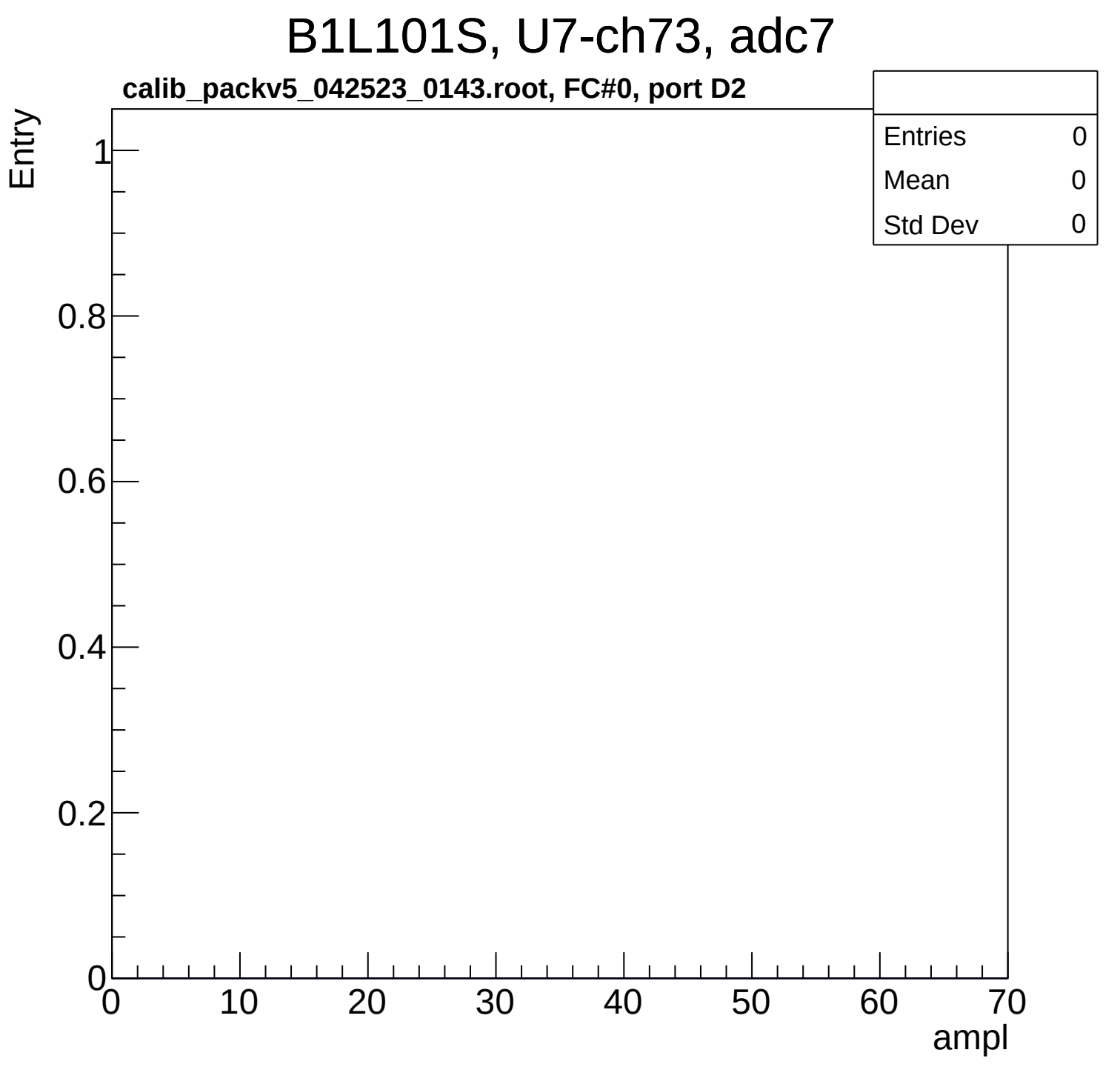
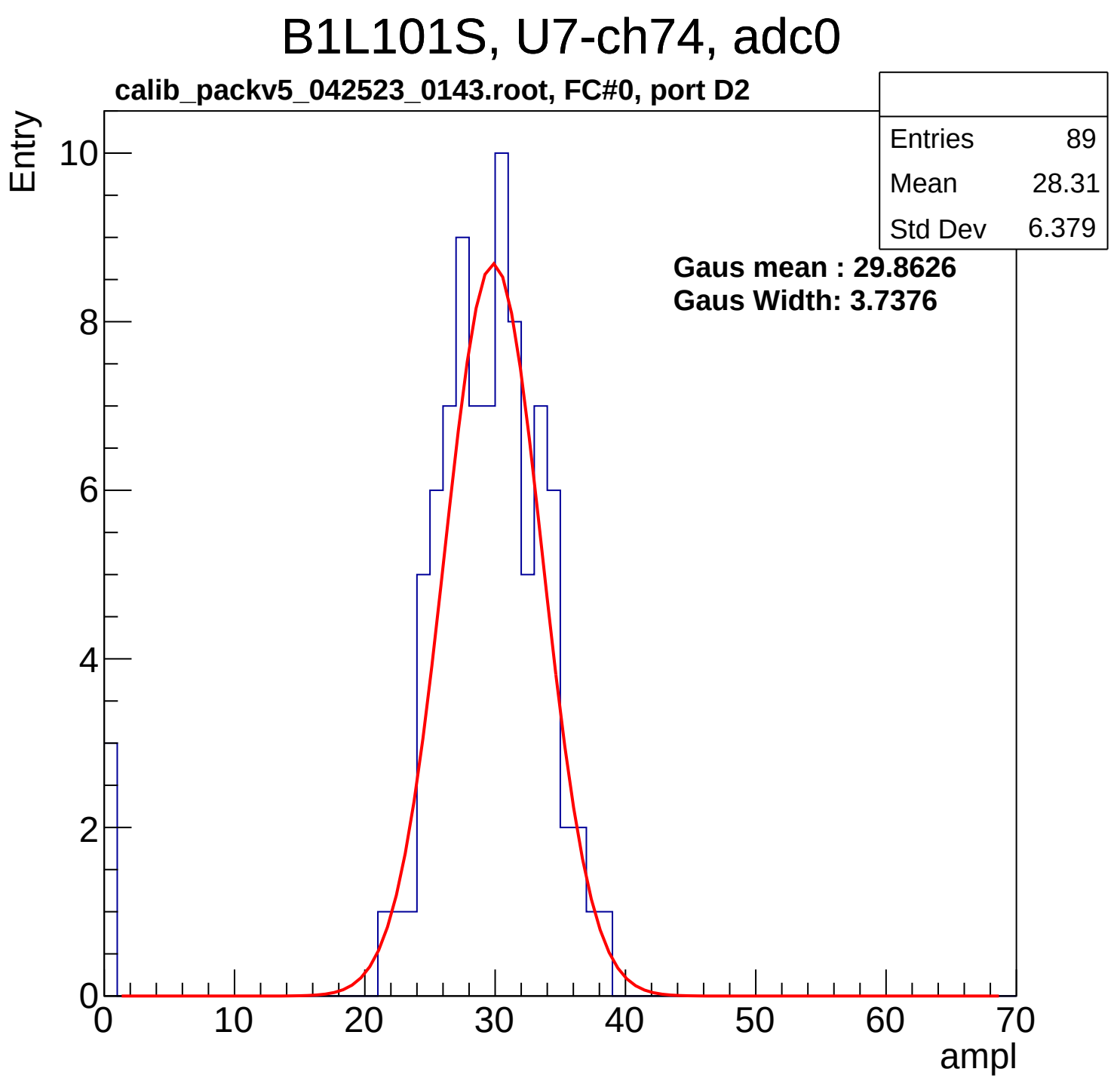
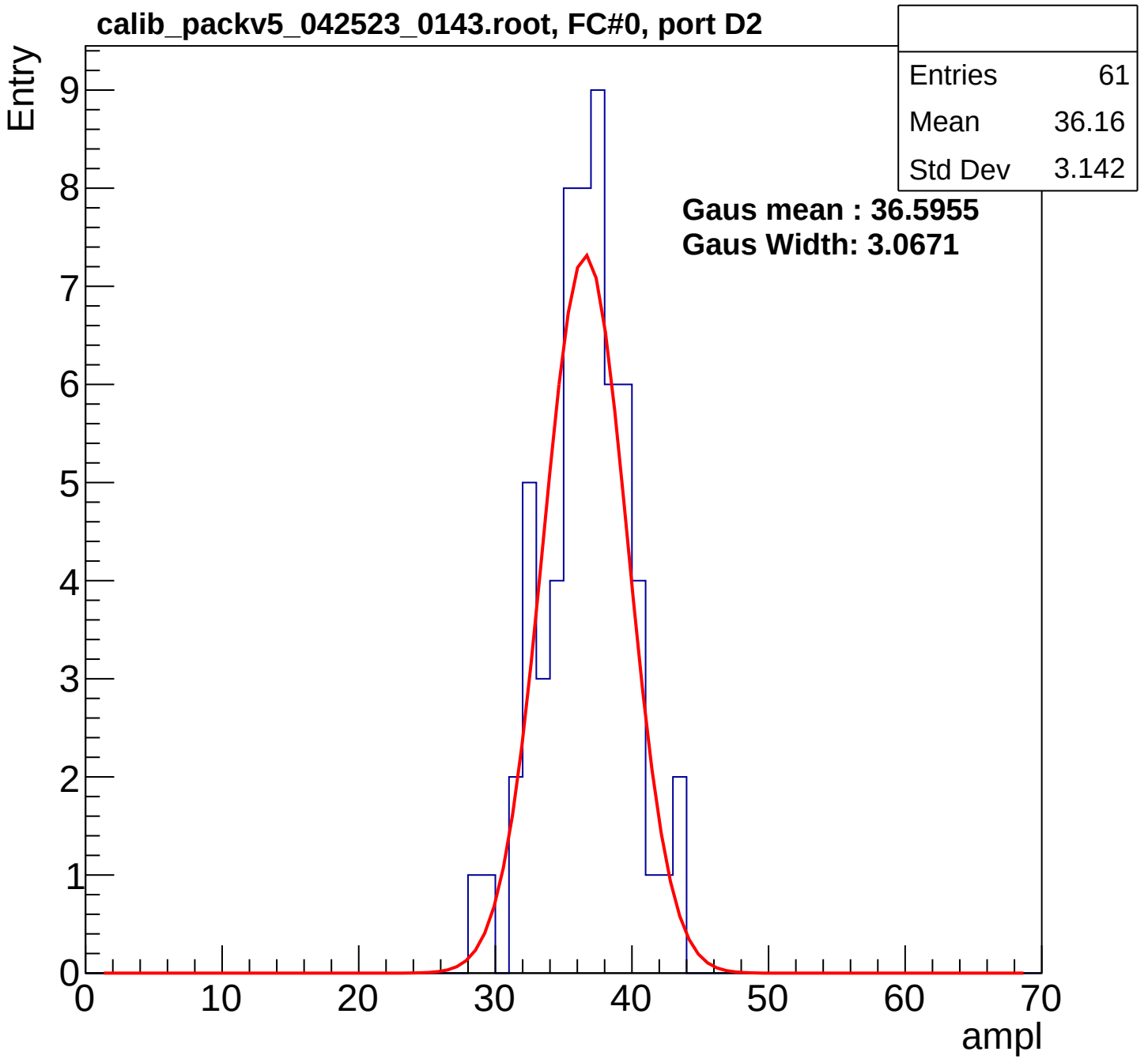
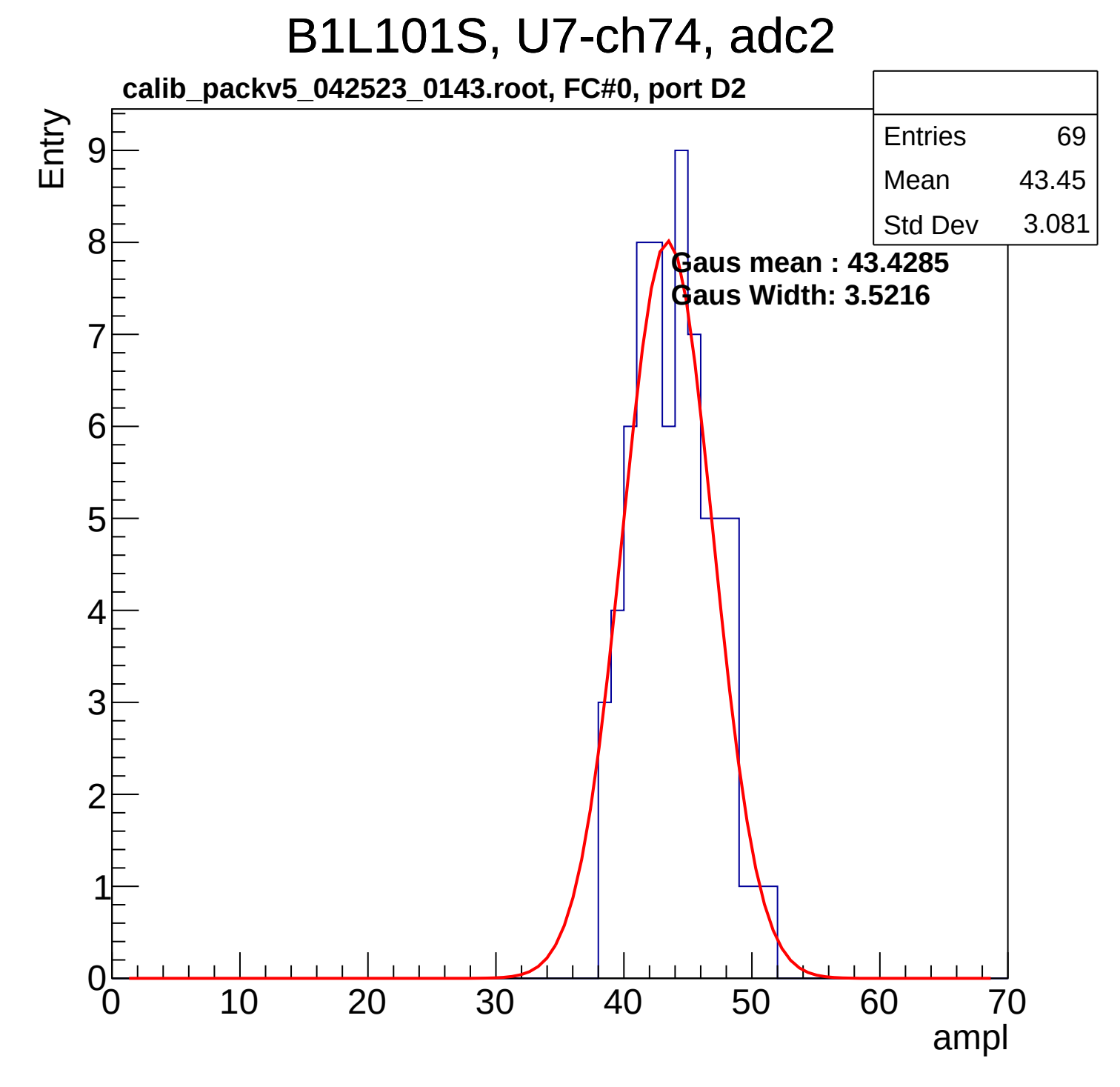

B1L101S, U7-ch73, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 46.75
Std Dev 26.99
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U7-ch73, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch74, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 89
Mean 28.31
Std Dev 6.379
Gaus mean : 29.8626
Gaus Width: 3.7376
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch74, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 36.16
Std Dev 3.142
Gaus mean : 36.5955
Gaus Width: 3.0671
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch74, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 43.45
Std Dev 3.081
Gaus mean : 43.4285
Gaus Width: 3.5216
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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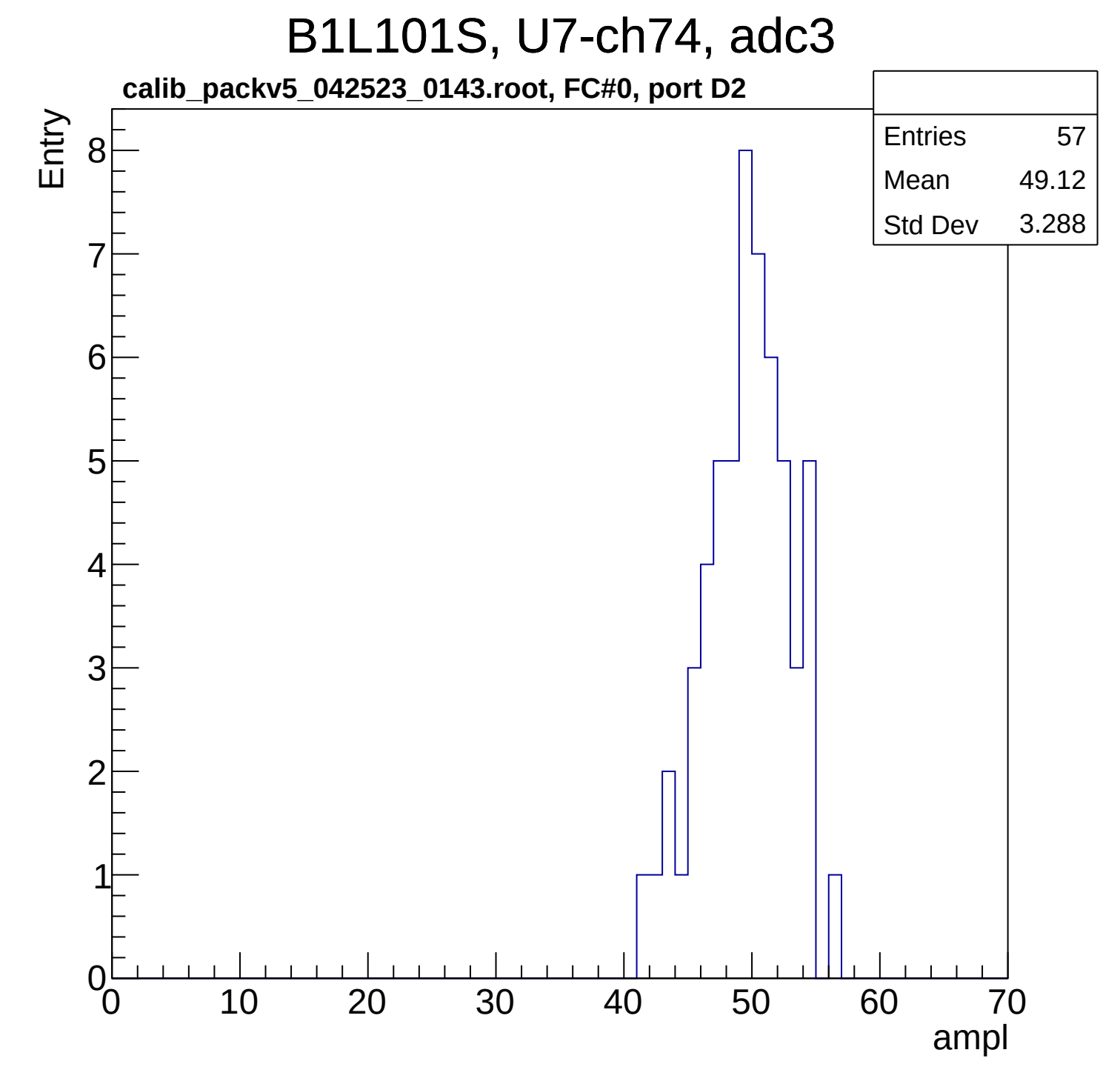
B1L101S, U7-ch74, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 49.12
Std Dev 3.288
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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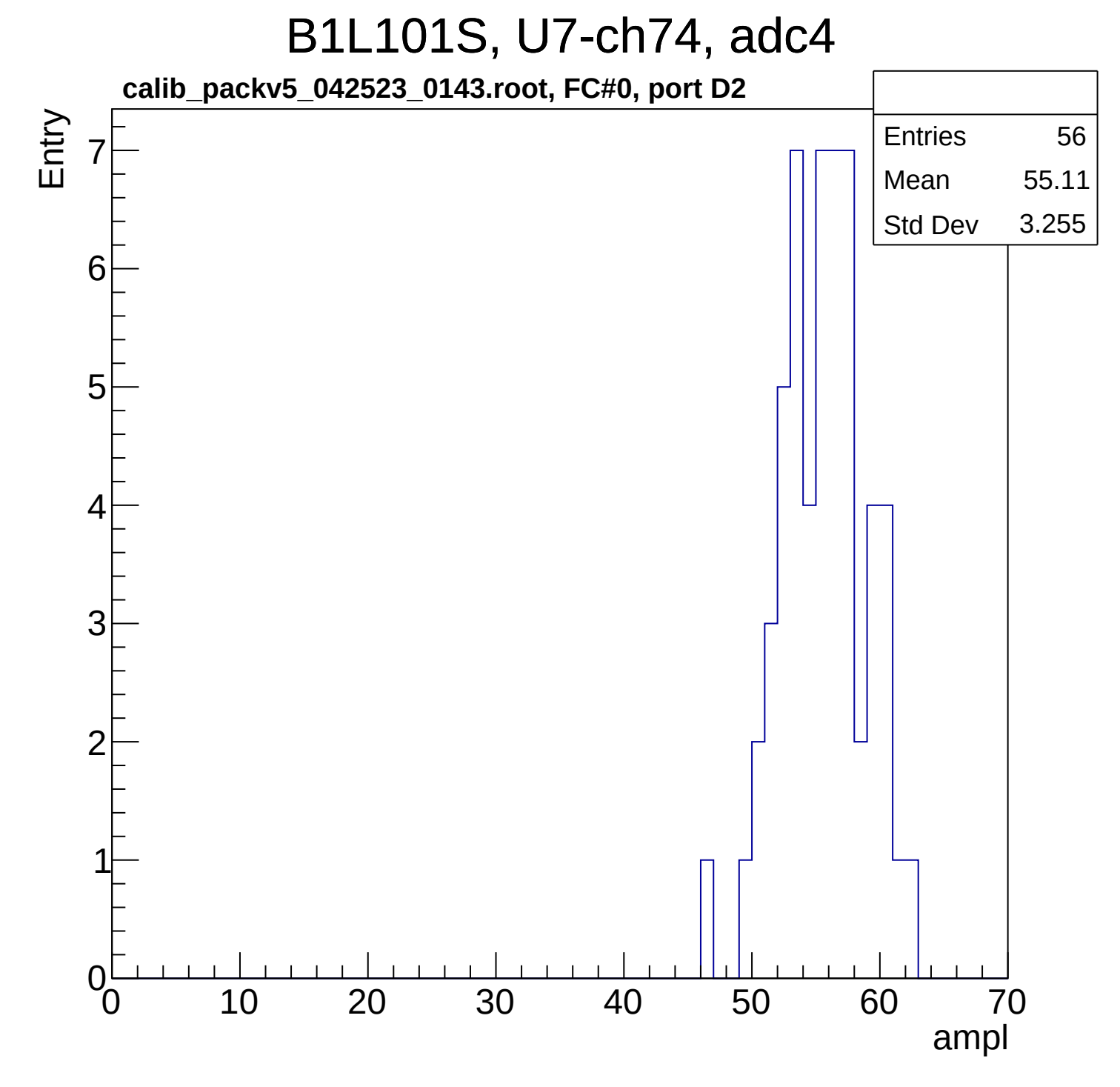
B1L101S, U7-ch74, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 55.11
Std Dev 3.255
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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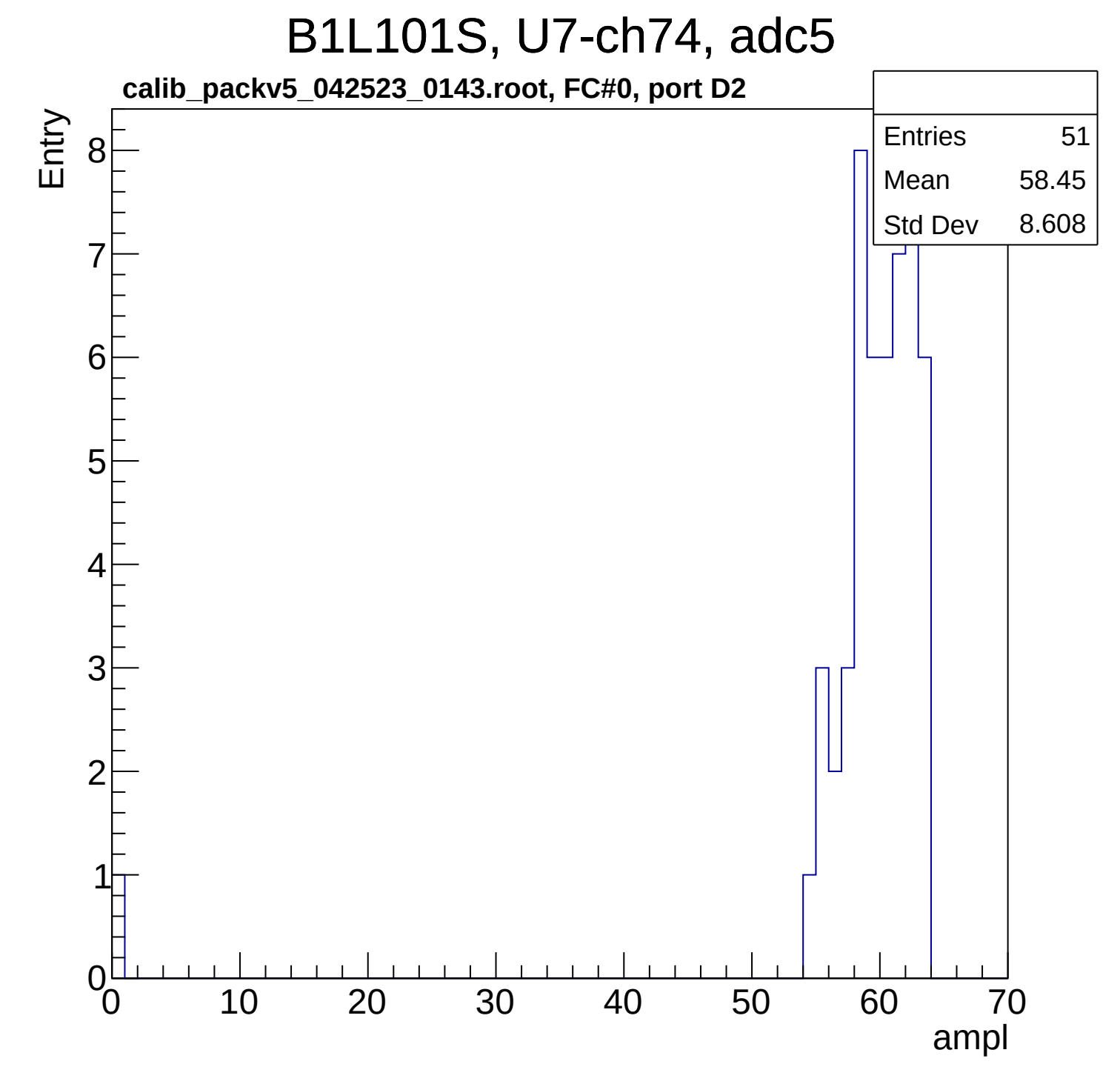
B1L101S, U7-ch74, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 58.45
Std Dev 8.608
Entry
ampl
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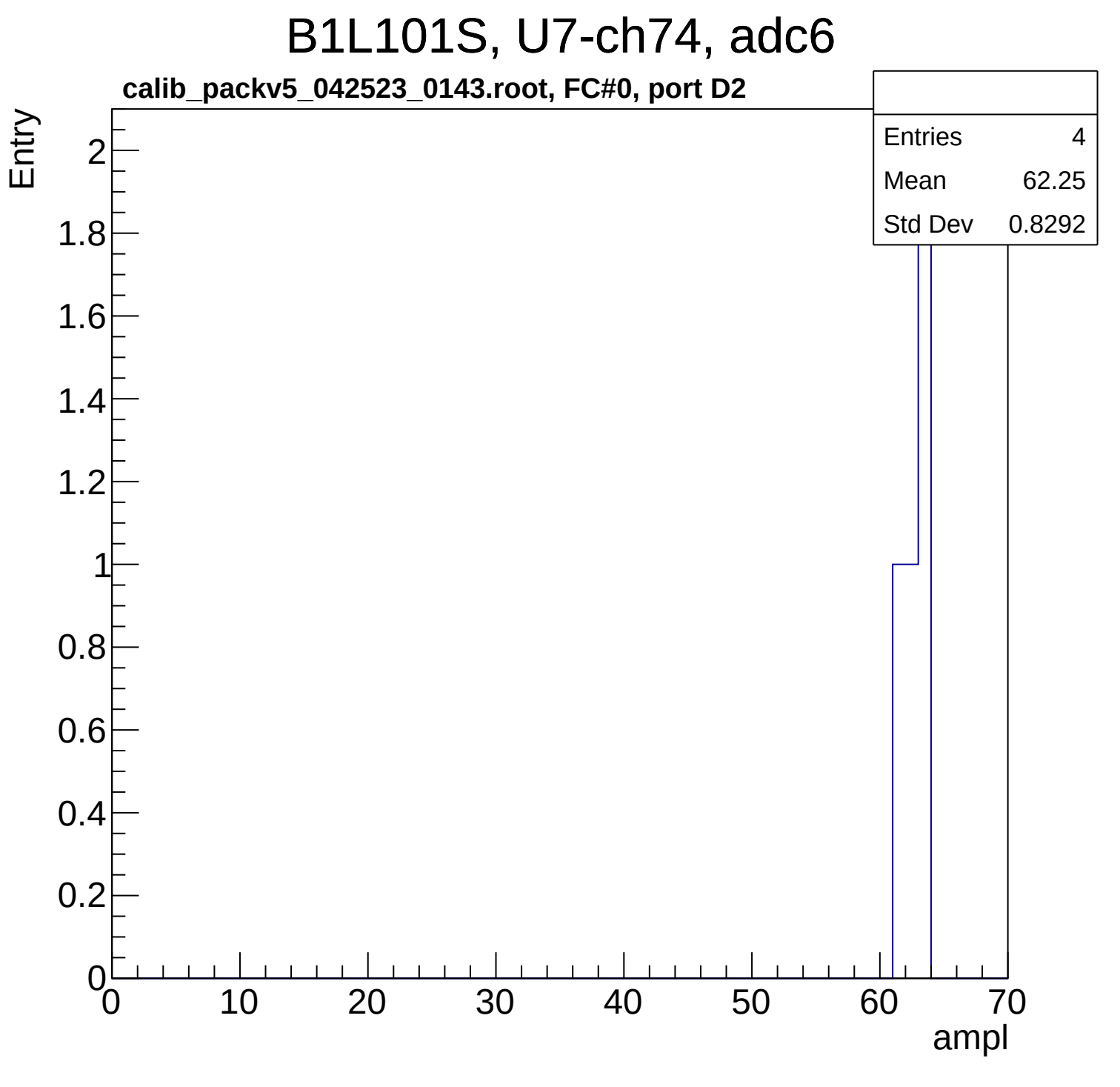
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch74, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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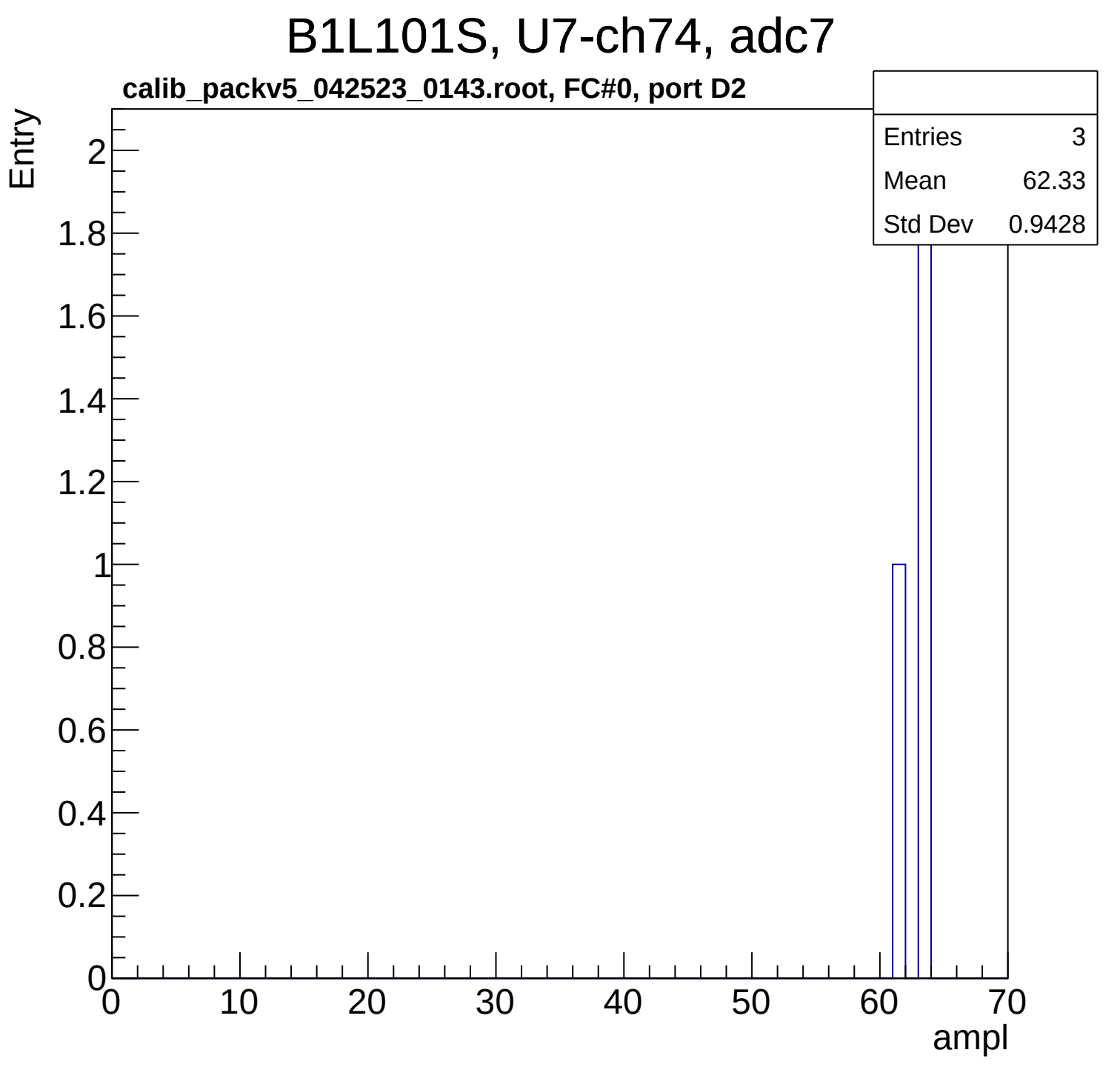
20
30
40
50
60
70


B1L101S, U7-ch74, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 62.33
Std Dev 0.9428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
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40
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60
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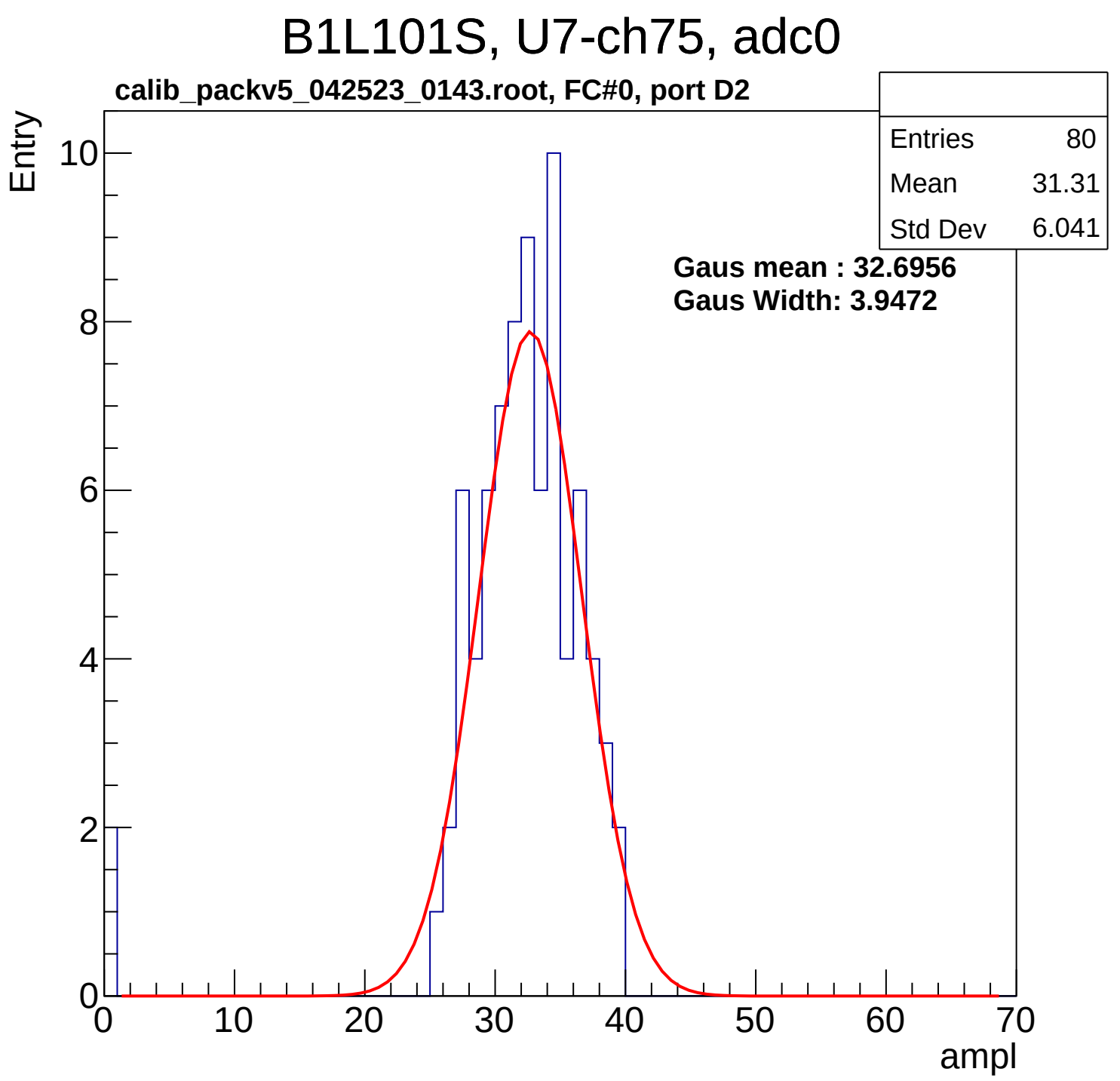
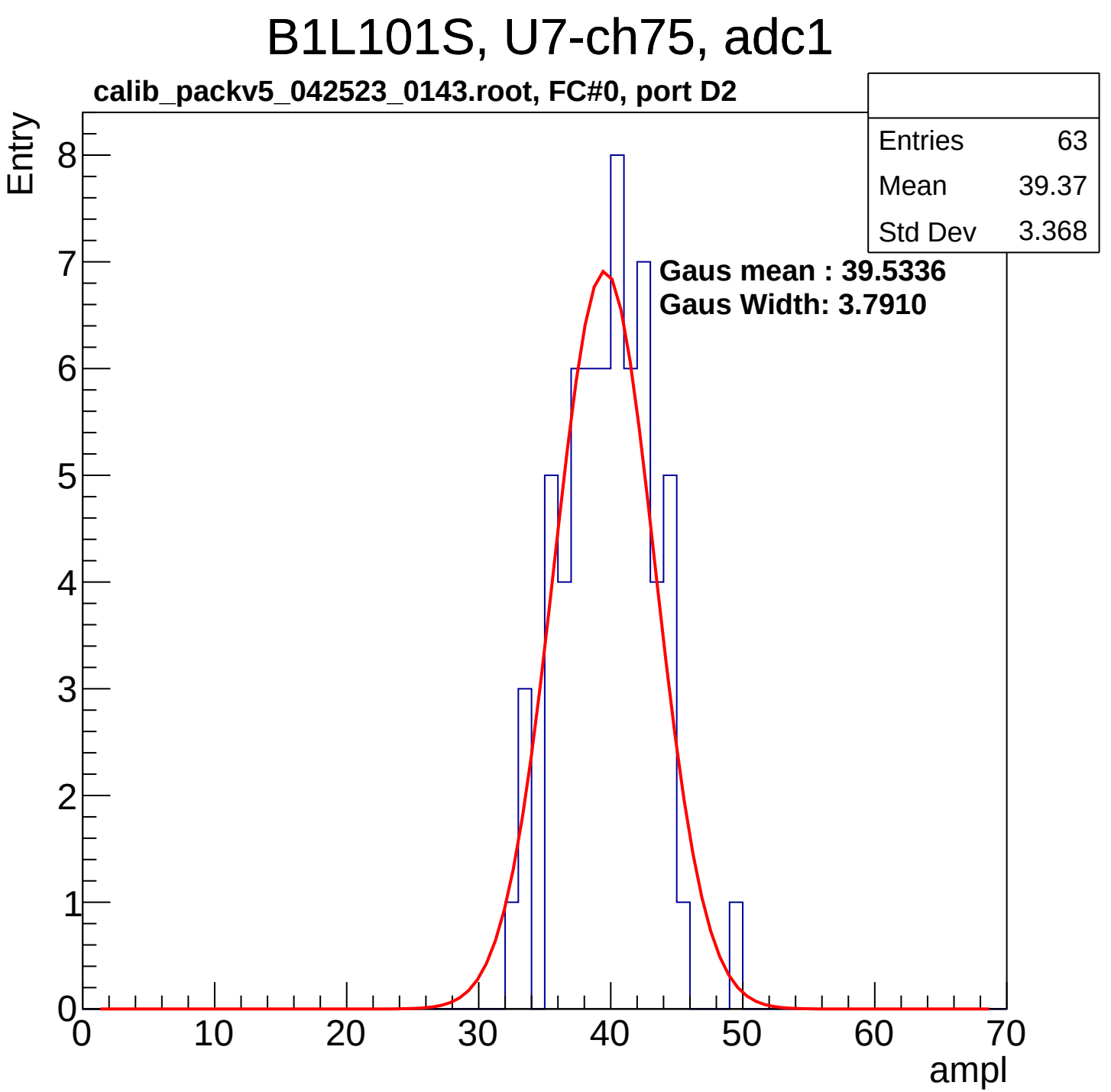

B1L101S, U7-ch75, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 80
Mean 31.31
Std Dev 6.041
Gaus mean : 32.6956
Gaus Width: 3.9472
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch75, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 39.37
Std Dev 3.368
Gaus mean : 39.5336
Gaus Width: 3.7910
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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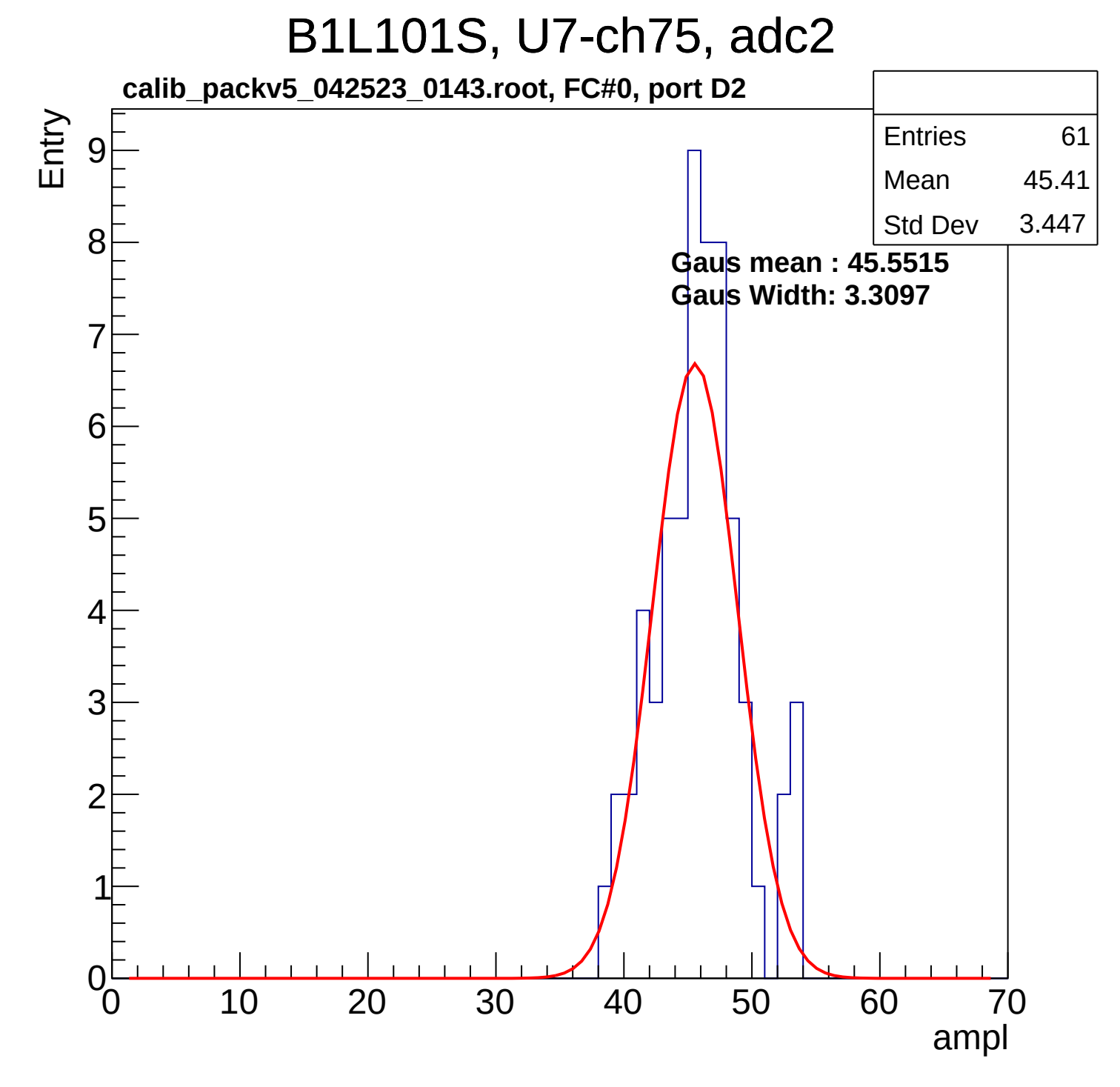
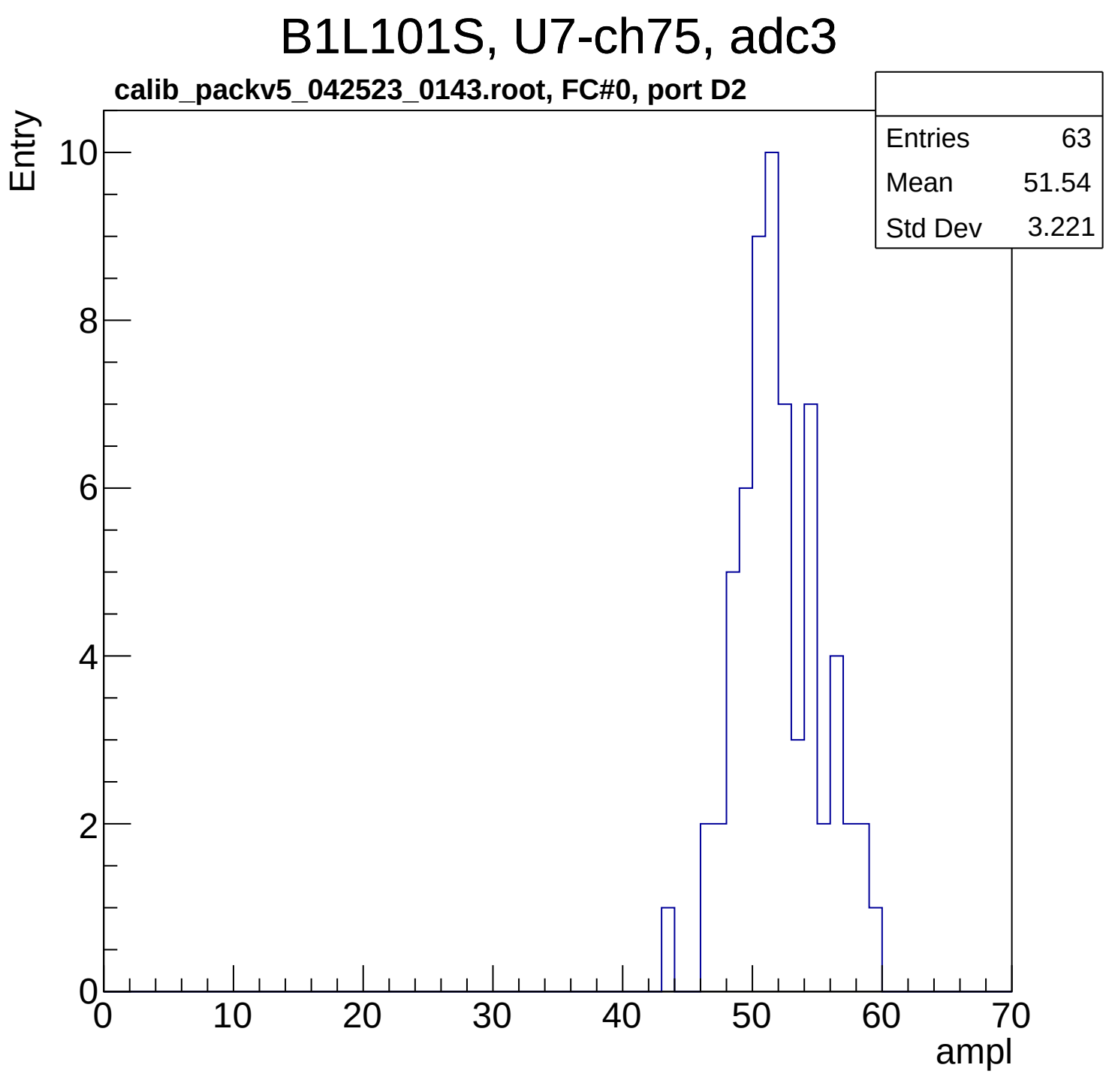
40
50
60
70


B1L101S, U7-ch75, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 45.41
Std Dev 3.447
Gaus mean : 45.5515
Gaus Width: 3.3097
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch75, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 51.54
Std Dev 3.221
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
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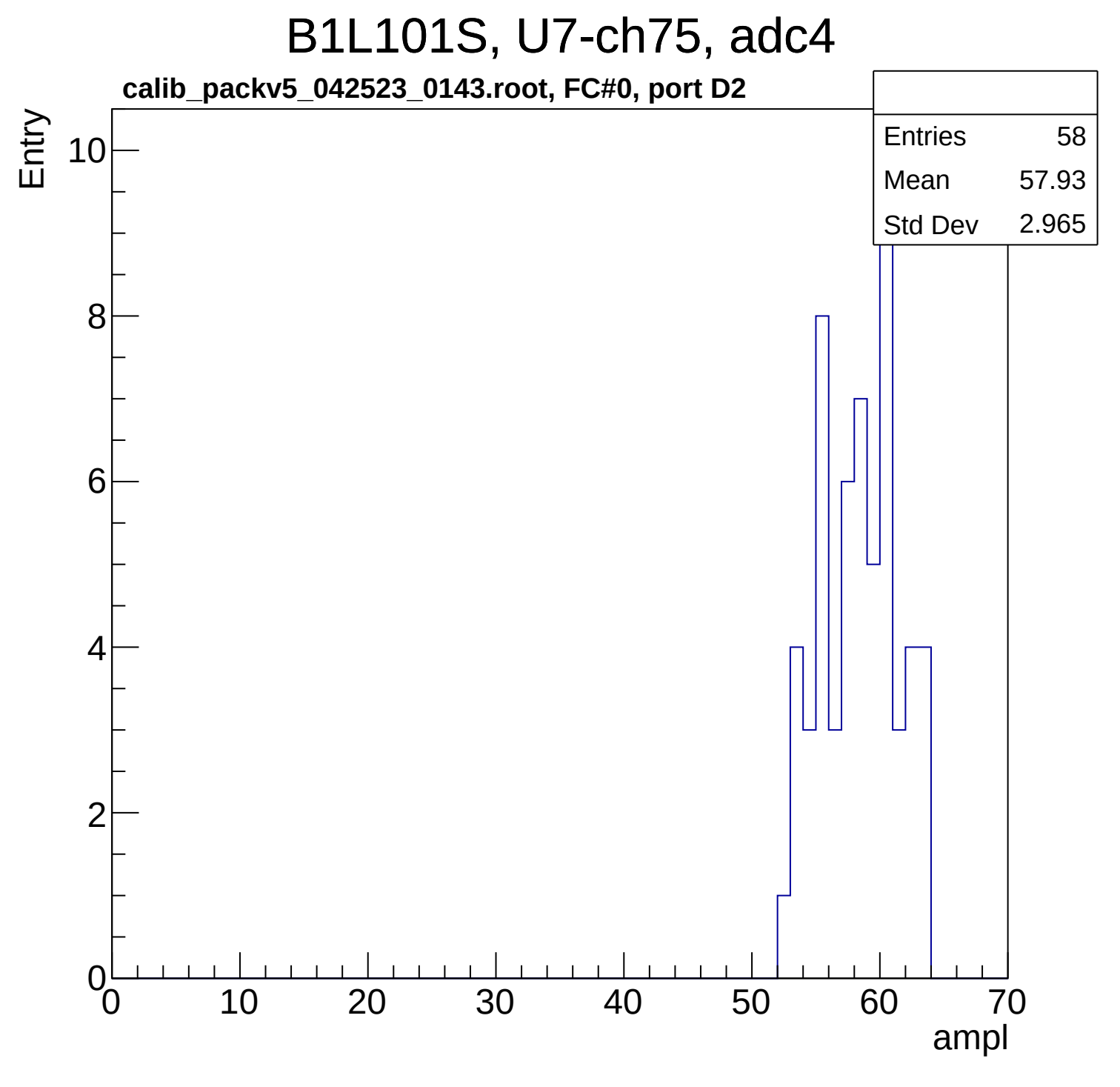
60
70


B1L101S, U7-ch75, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 57.93
Std Dev 2.965
Entry
ampl
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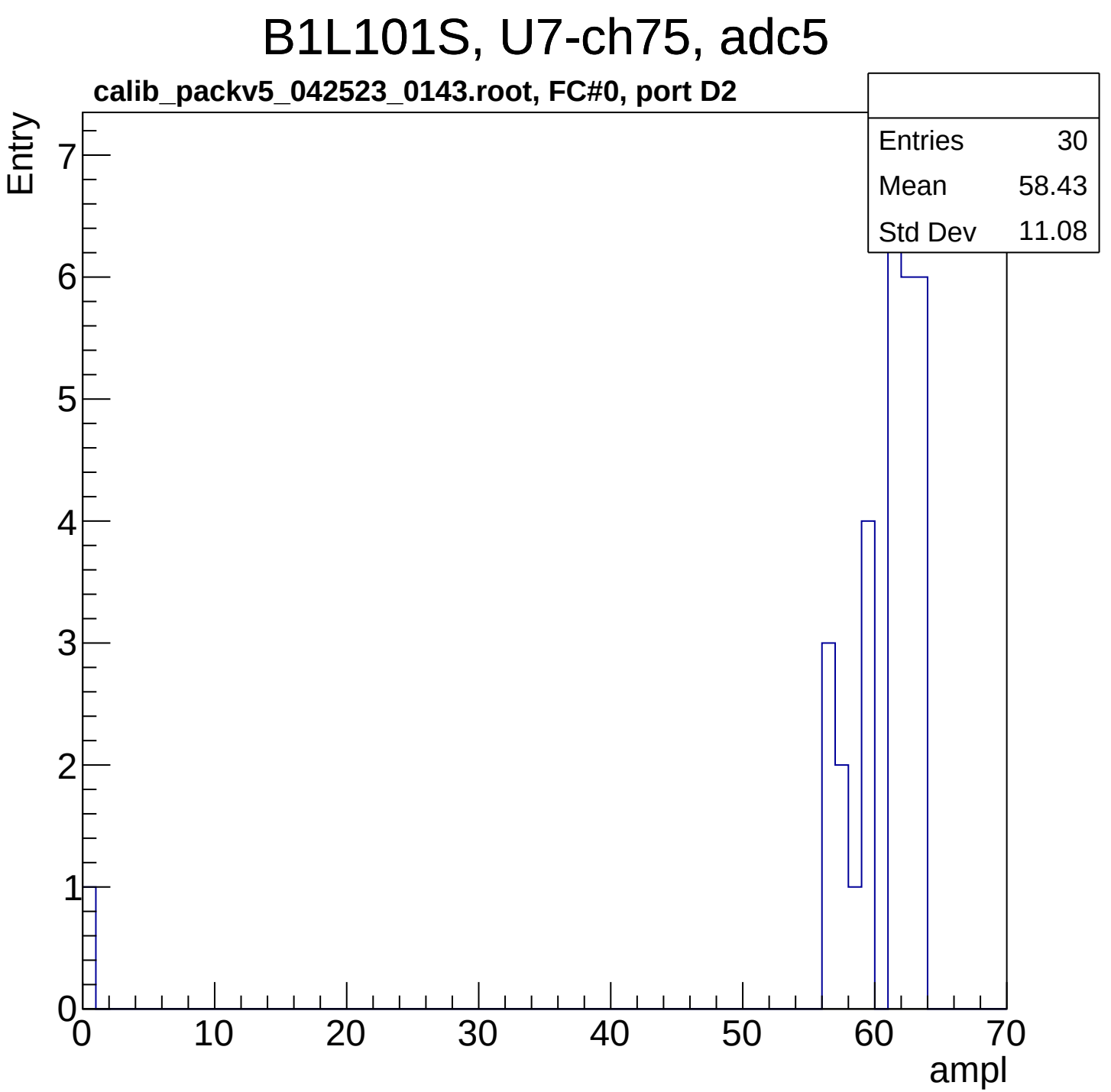
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch75, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 30
Mean 58.43
Std Dev 11.08
Entry
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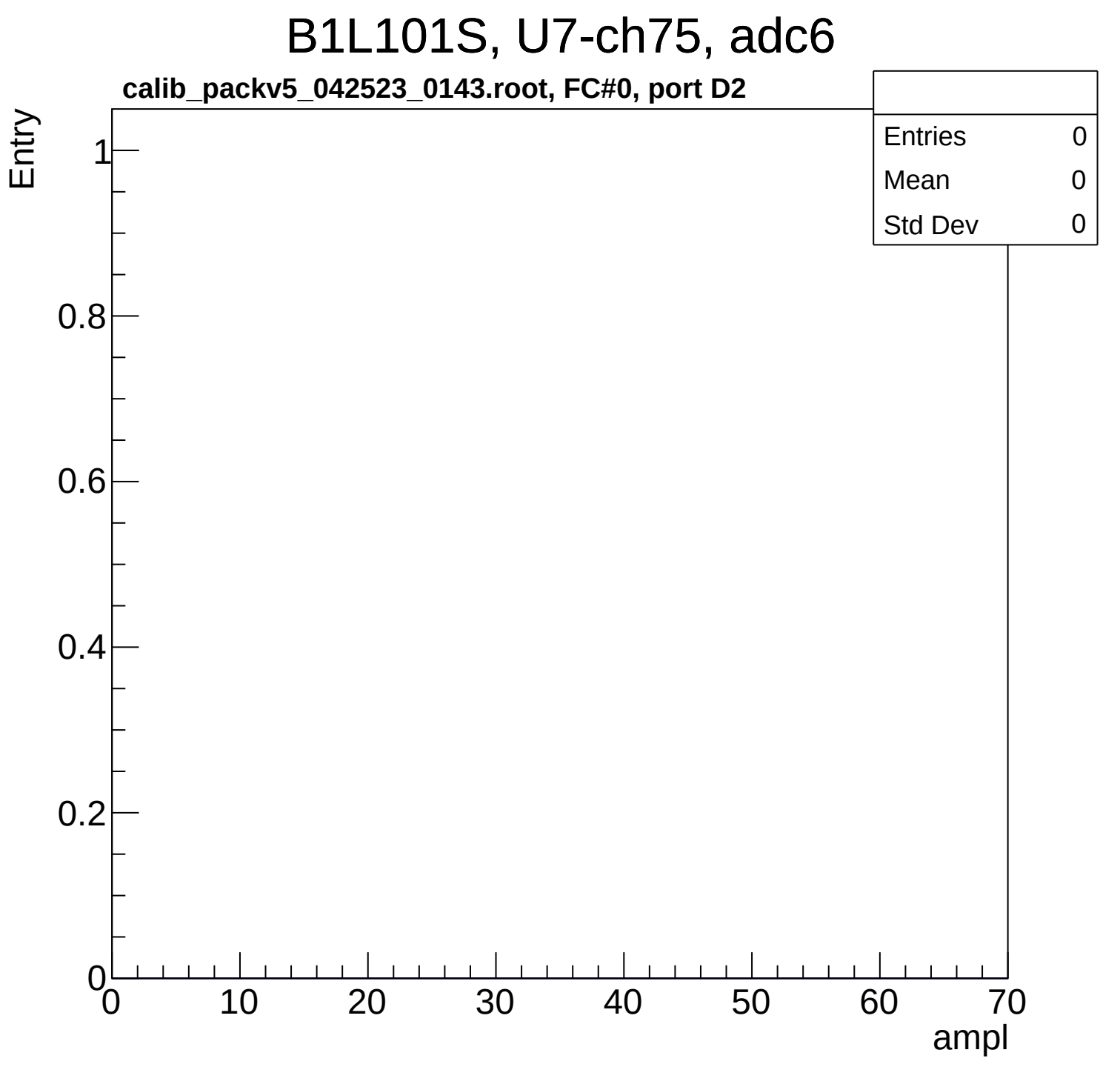
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch75, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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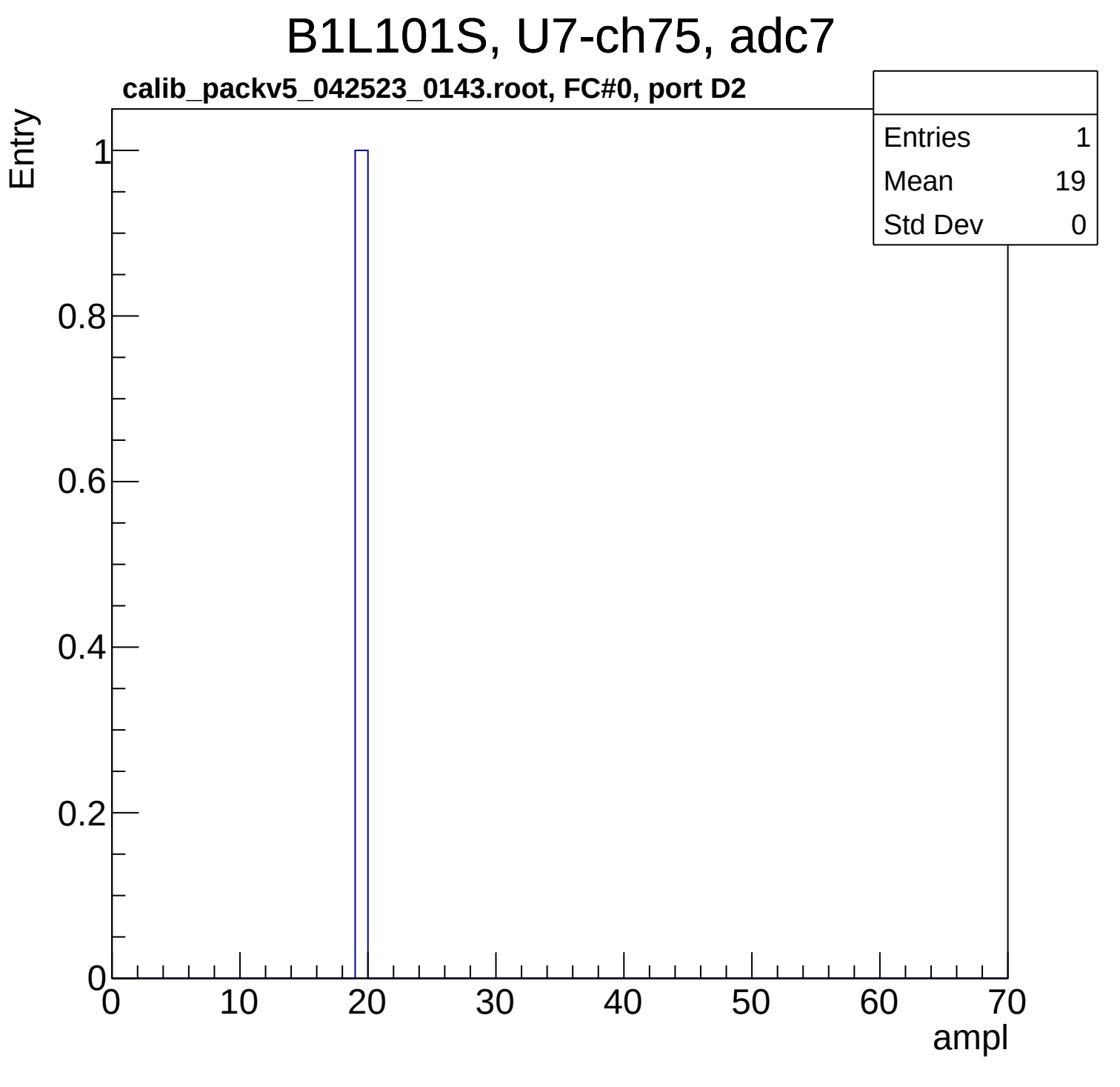
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch75, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 19
Std Dev 0
Entry
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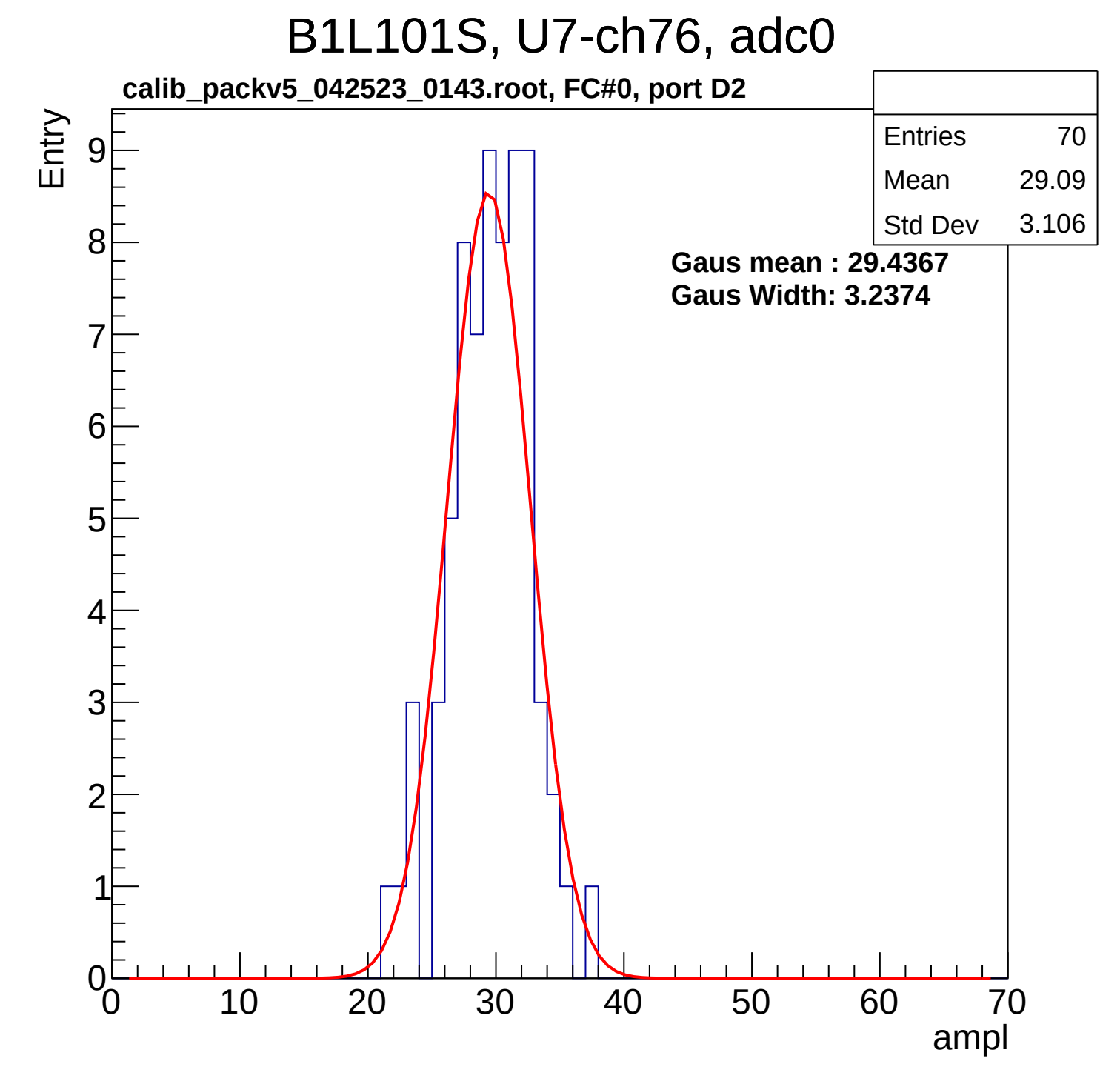
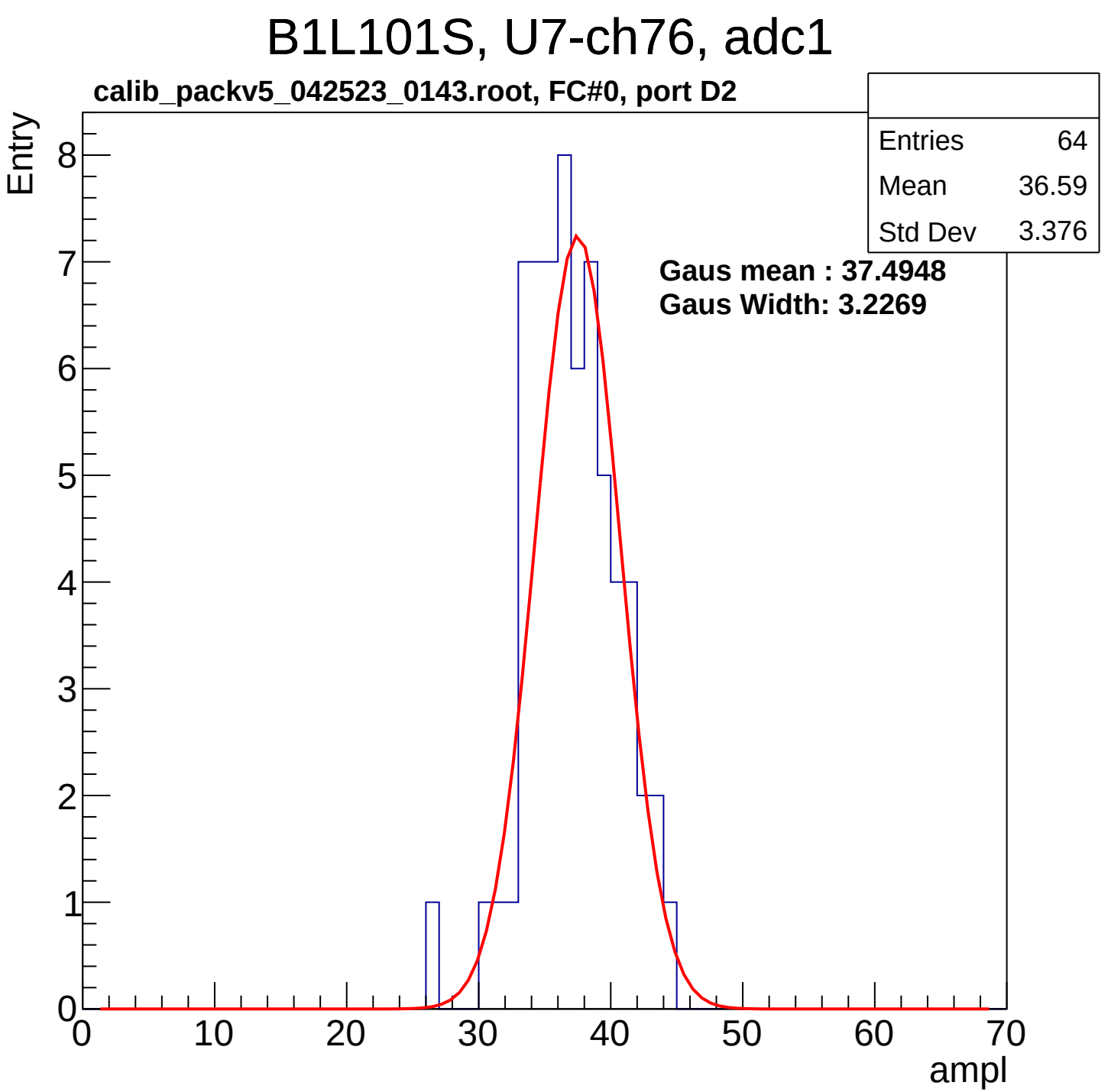
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch76, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 29.09
Std Dev 3.106
Gaus mean : 29.4367
Gaus Width: 3.2374
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch76, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 36.59
Std Dev 3.376
Gaus mean : 37.4948
Gaus Width: 3.2269
Entry
ampl
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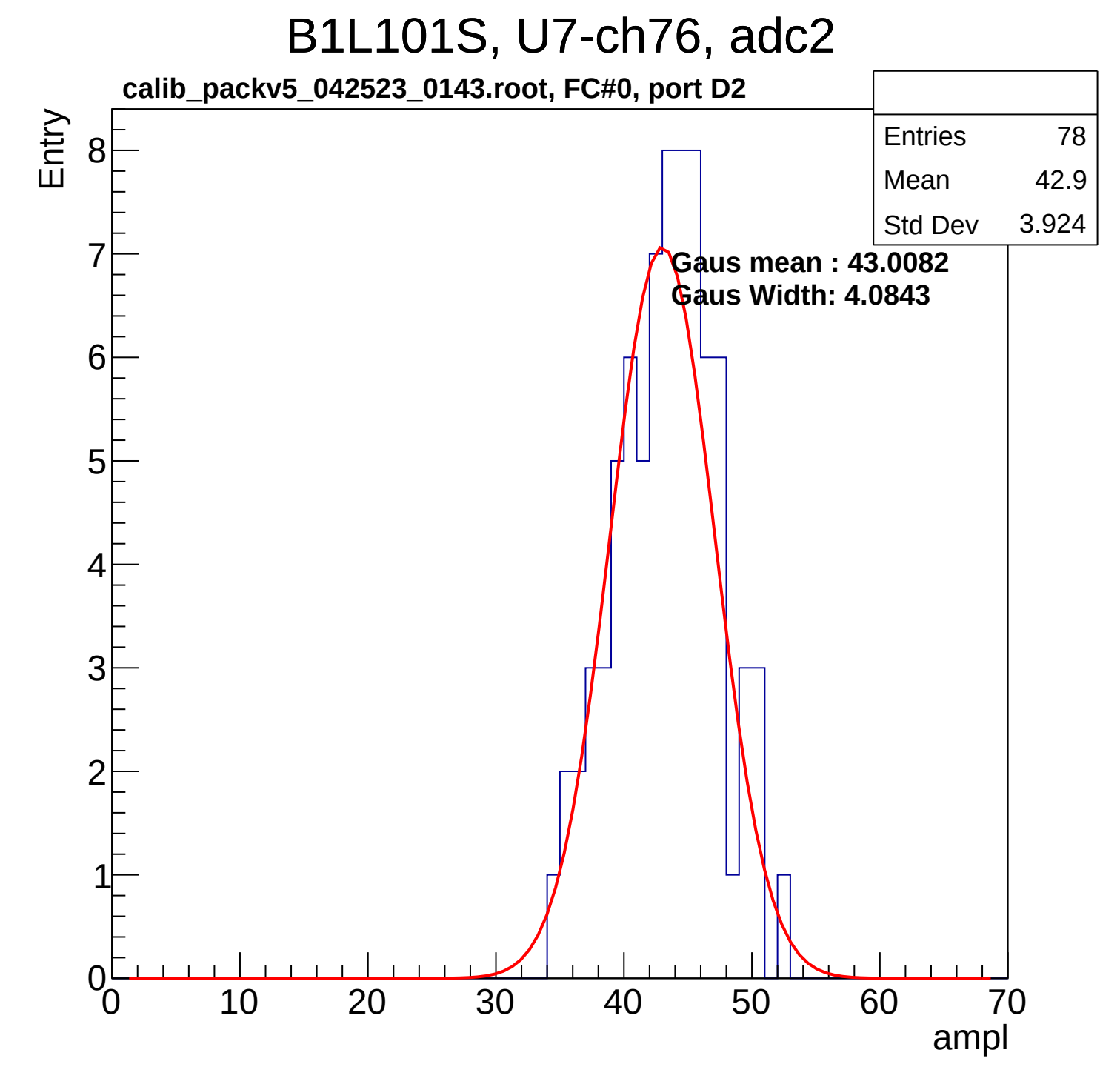
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch76, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 42.9
Std Dev 3.924
Gaus mean : 43.0082
Gaus Width: 4.0843
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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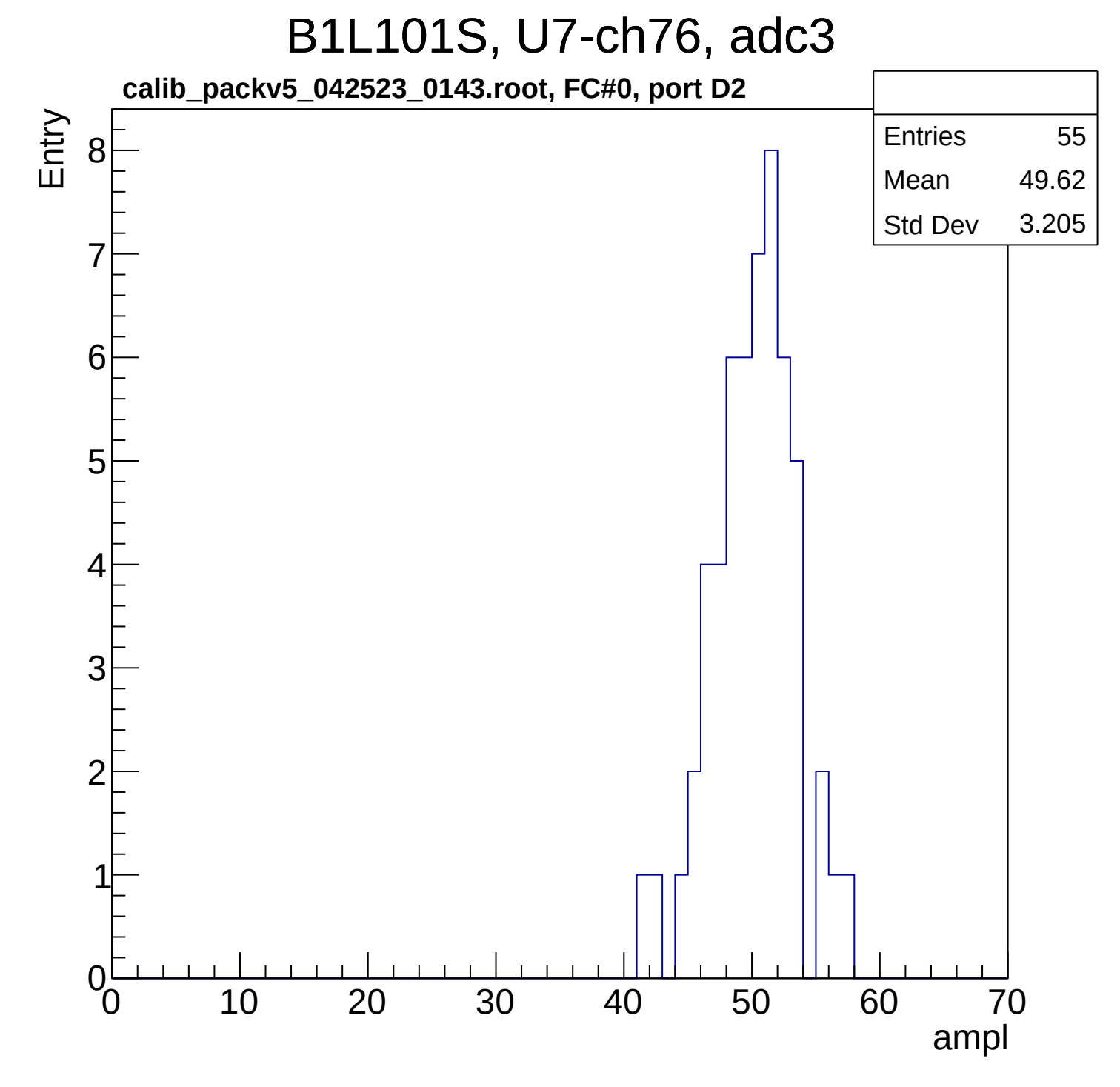
40
50
60
70


B1L101S, U7-ch76, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 49.62
Std Dev 3.205
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
50
60
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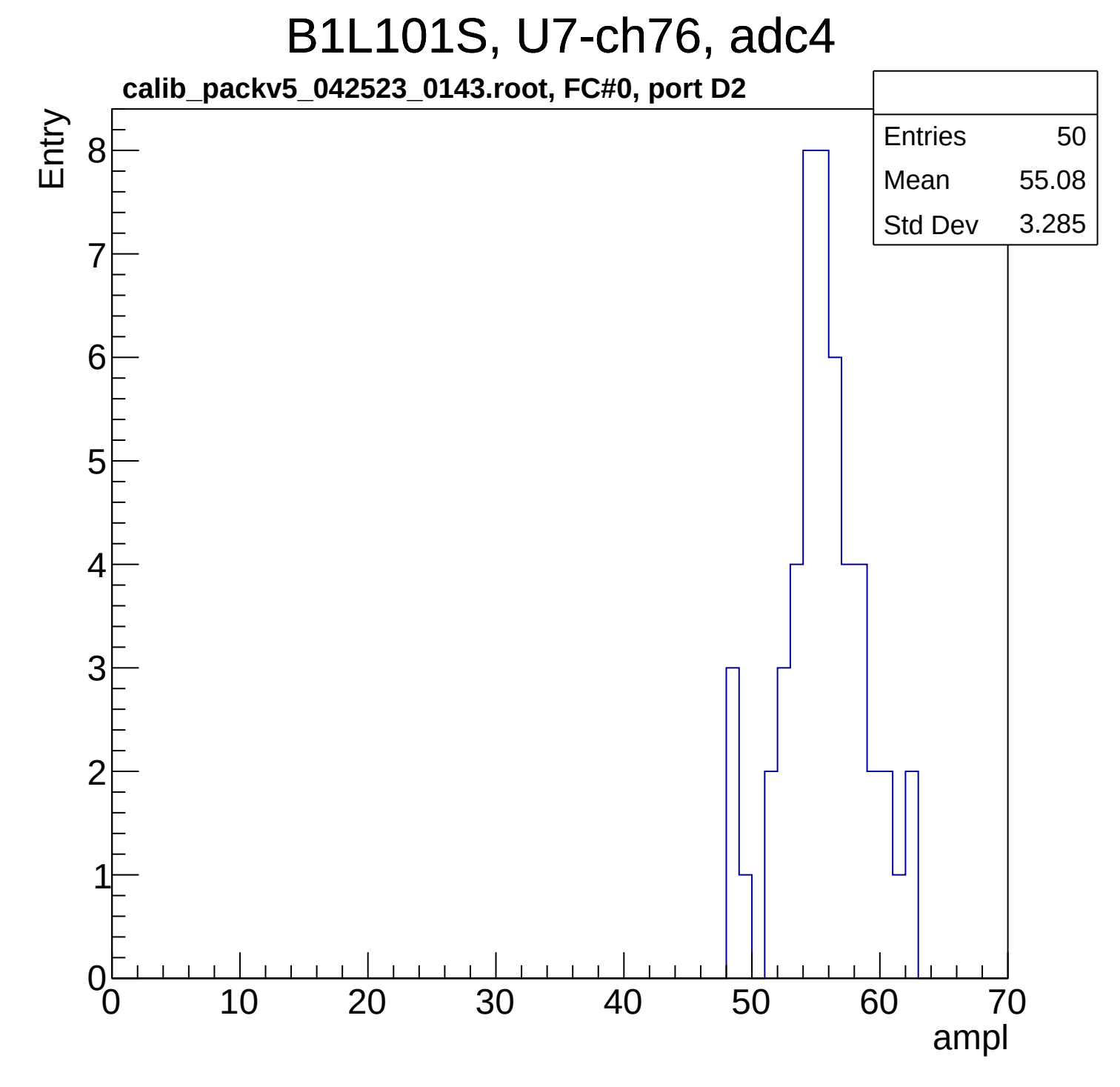
B1L101S, U7-ch76, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 55.08
Std Dev 3.285
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
50
60
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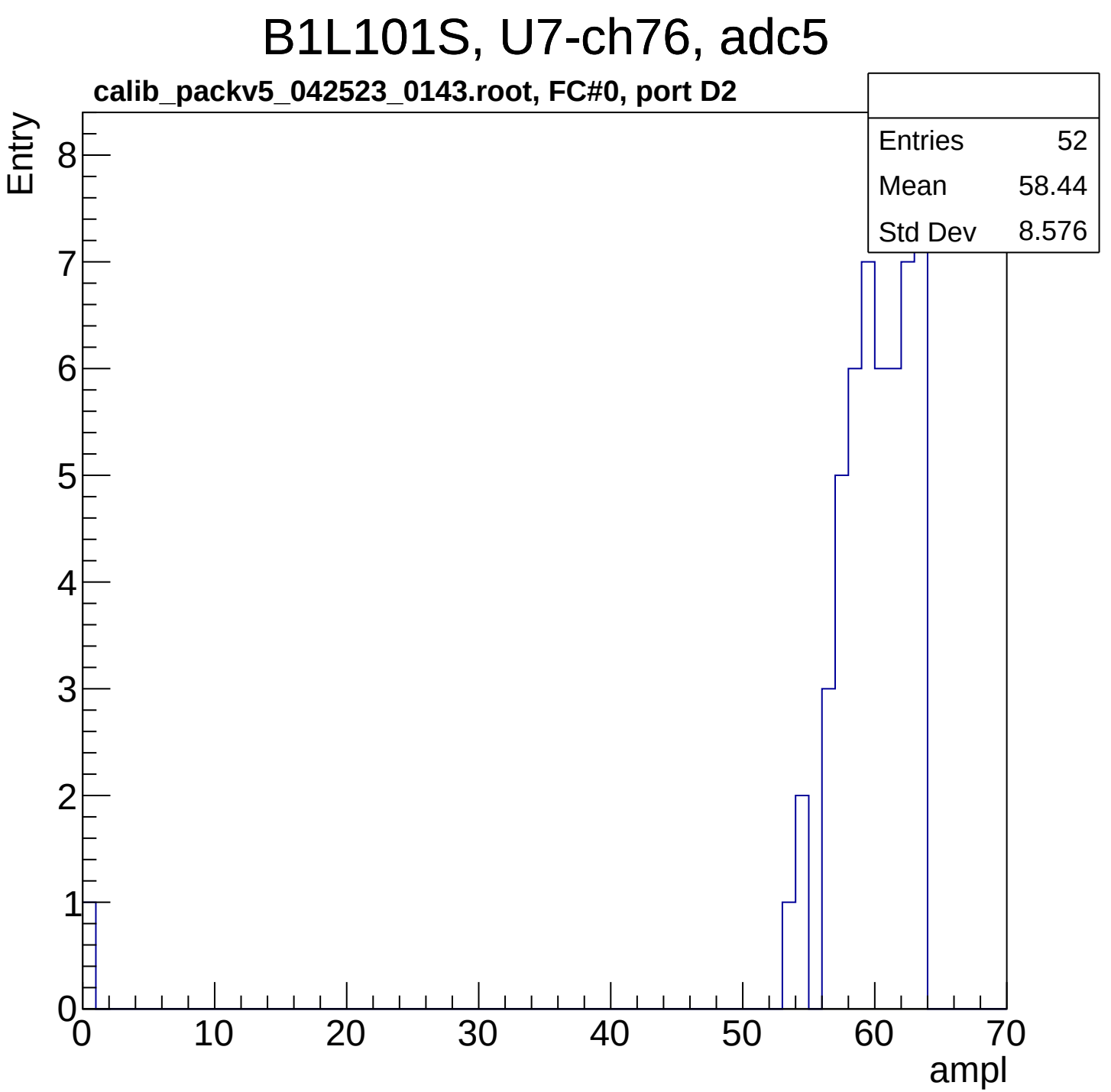
B1L101S, U7-ch76, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 58.44
Std Dev 8.576
Entry
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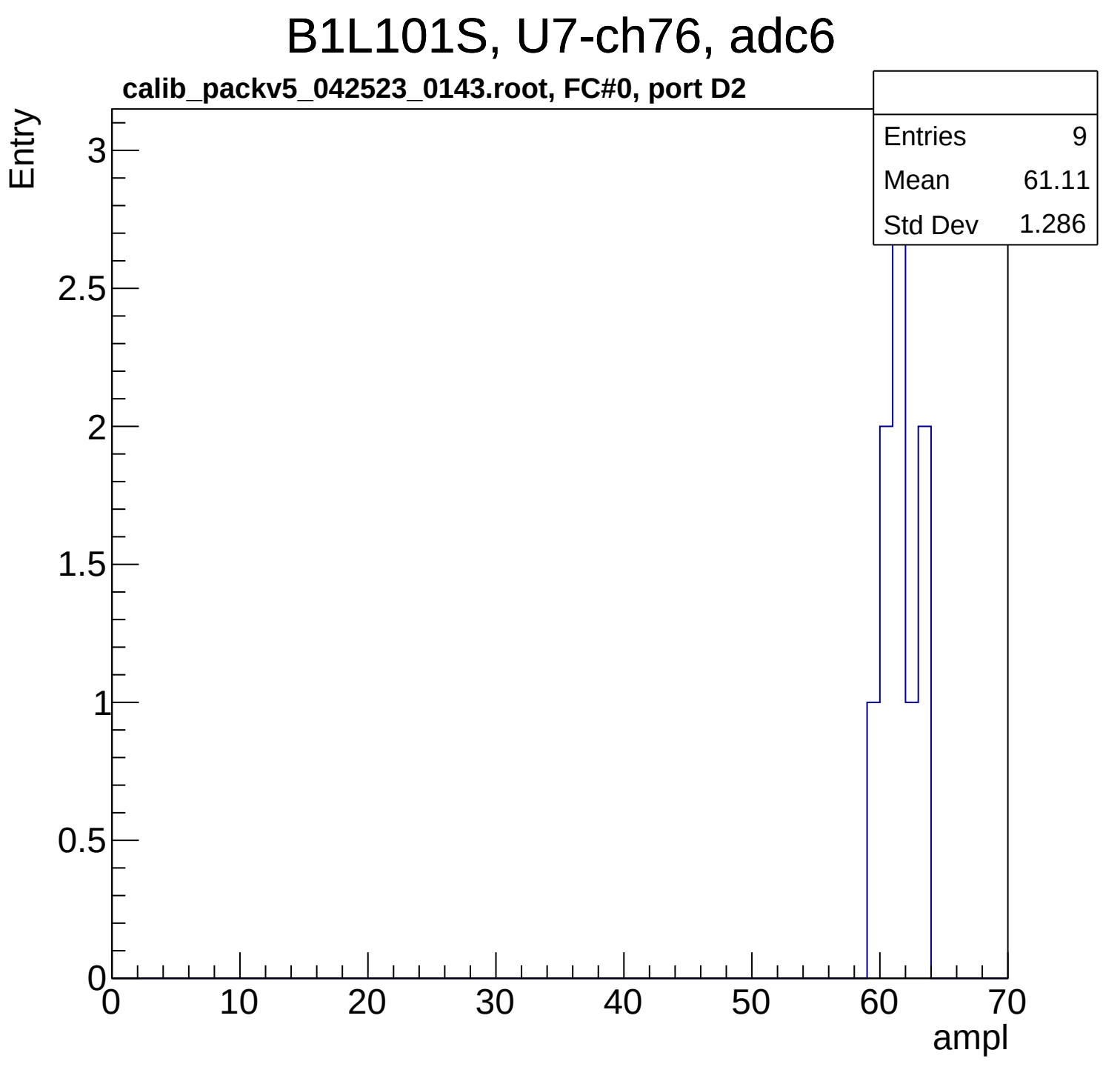
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch76, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 61.11
Std Dev 1.286
Entry
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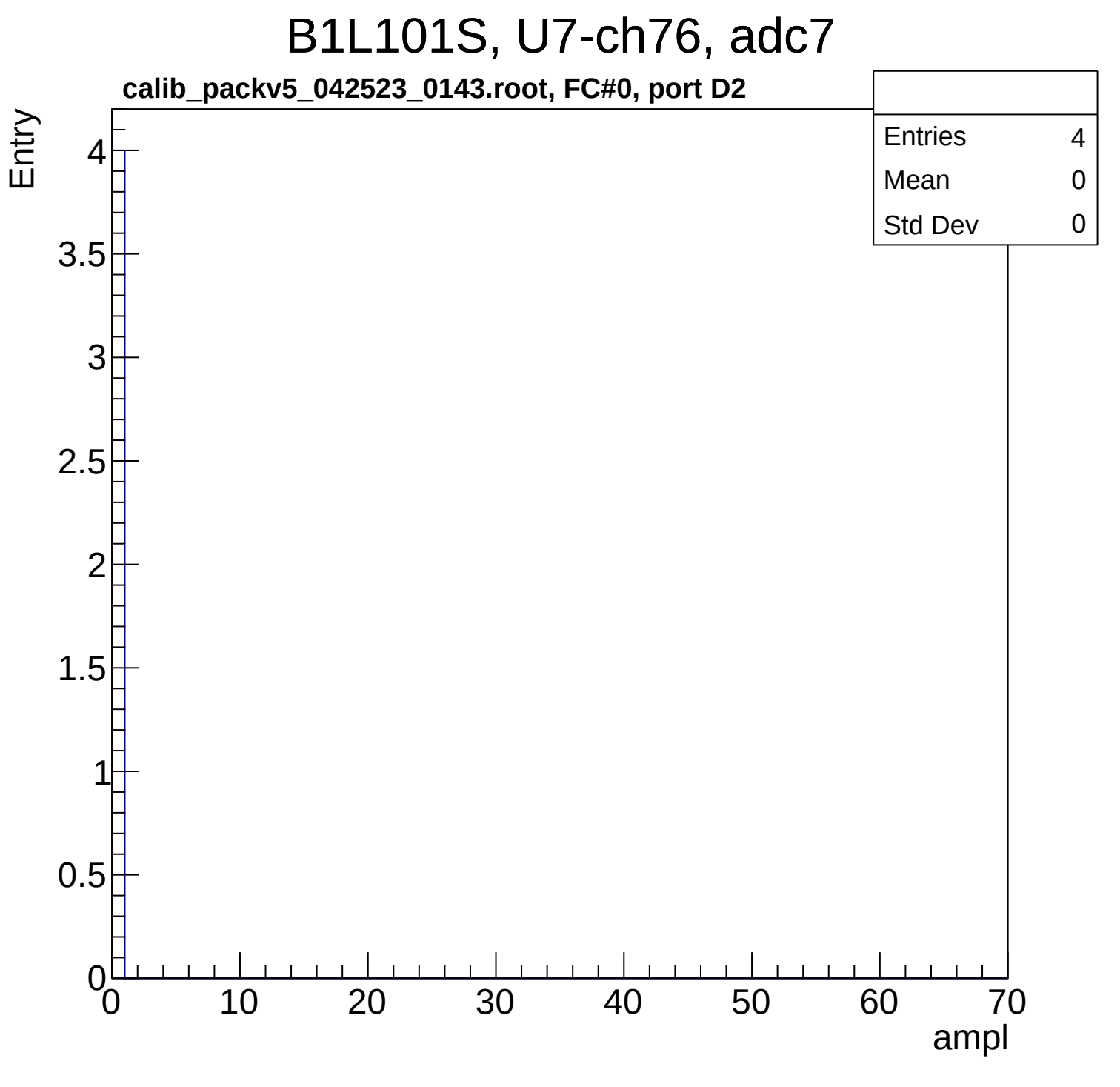
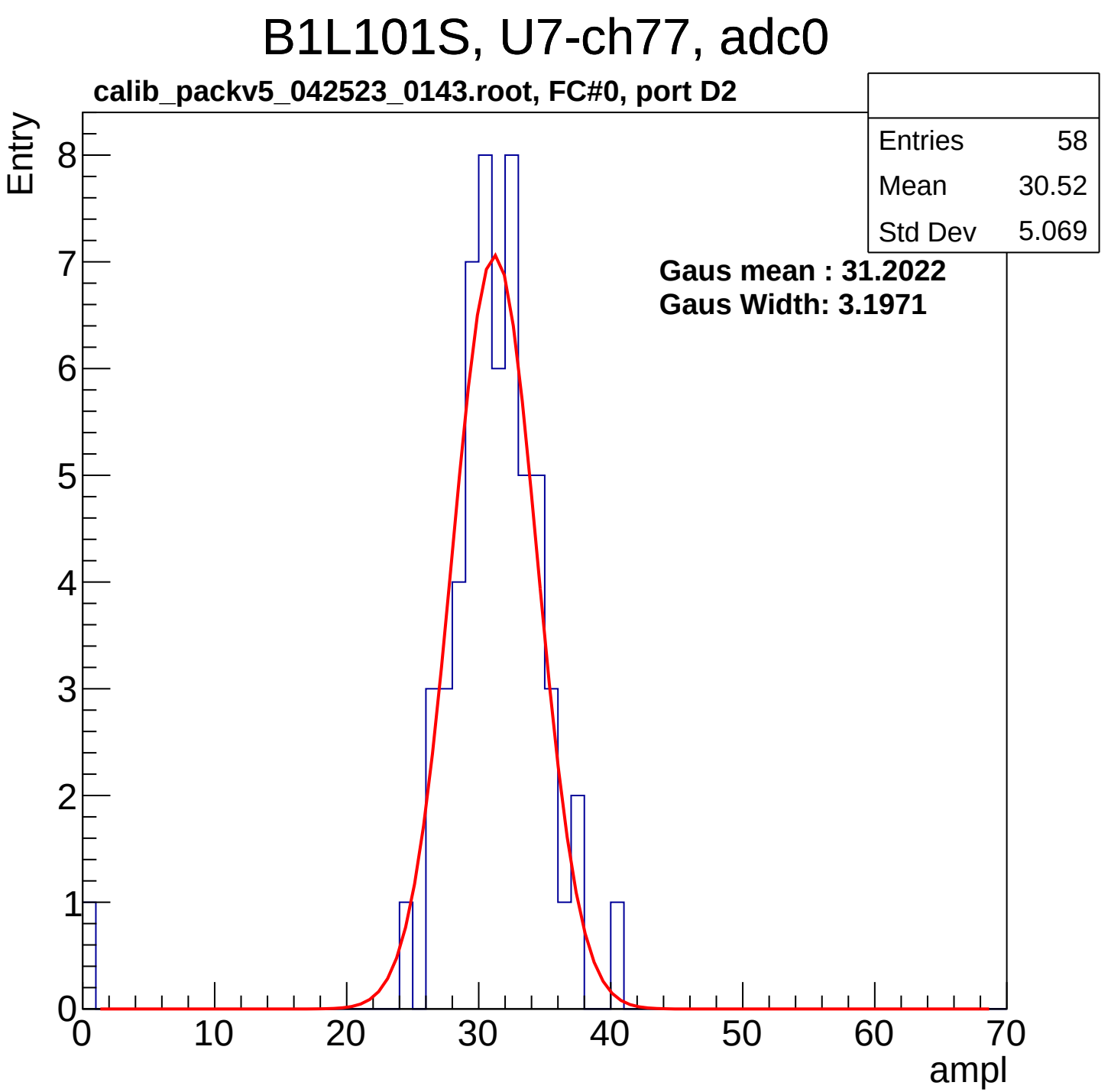
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch76, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 0
Std Dev 0
Entry
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch77, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 30.52
Std Dev 5.069
Gaus mean : 31.2022
Gaus Width: 3.1971
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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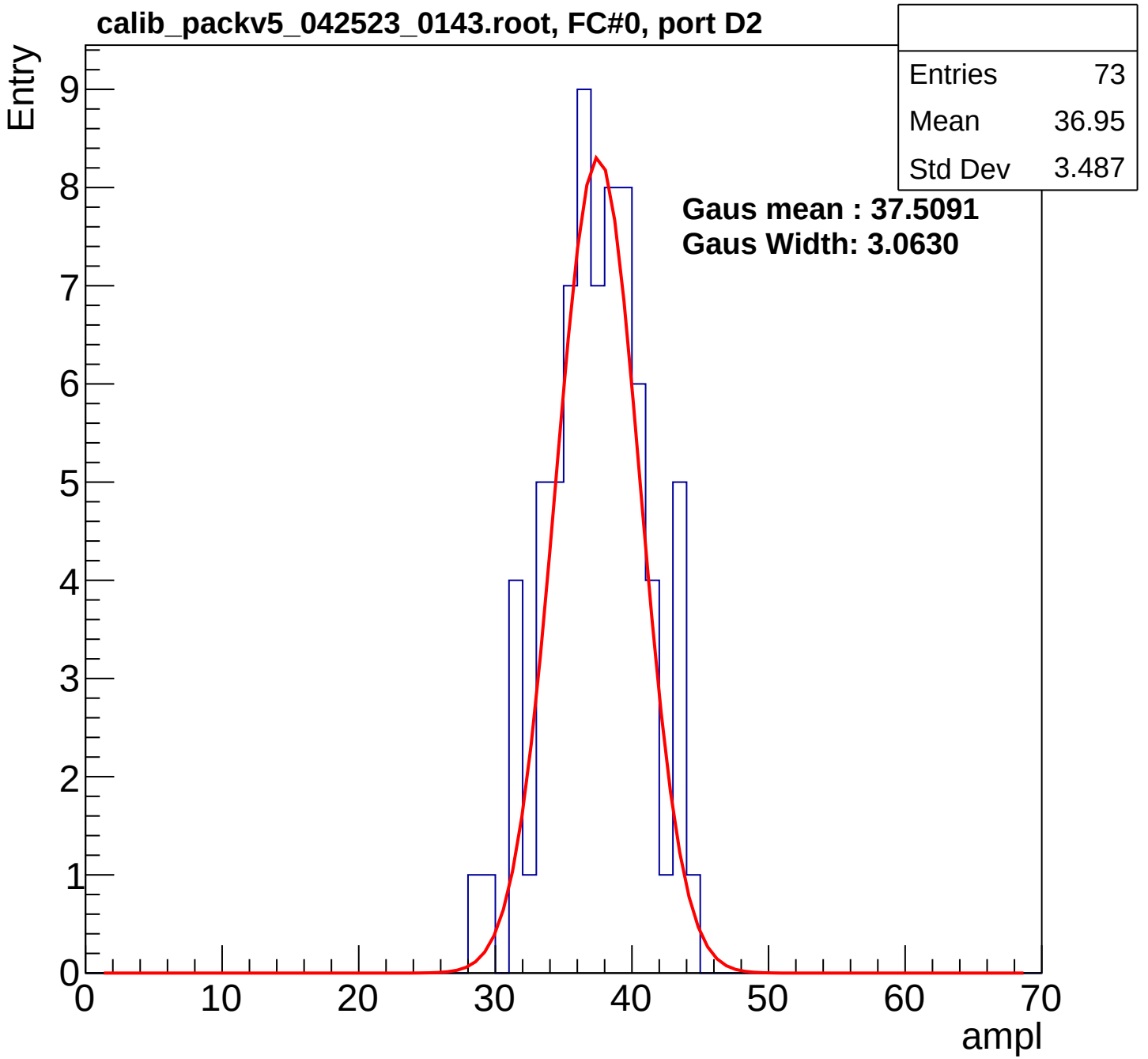
B1L101S, U7-ch77, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 36.95
Std Dev 3.487
Gaus mean : 37.5091
Gaus Width: 3.0630
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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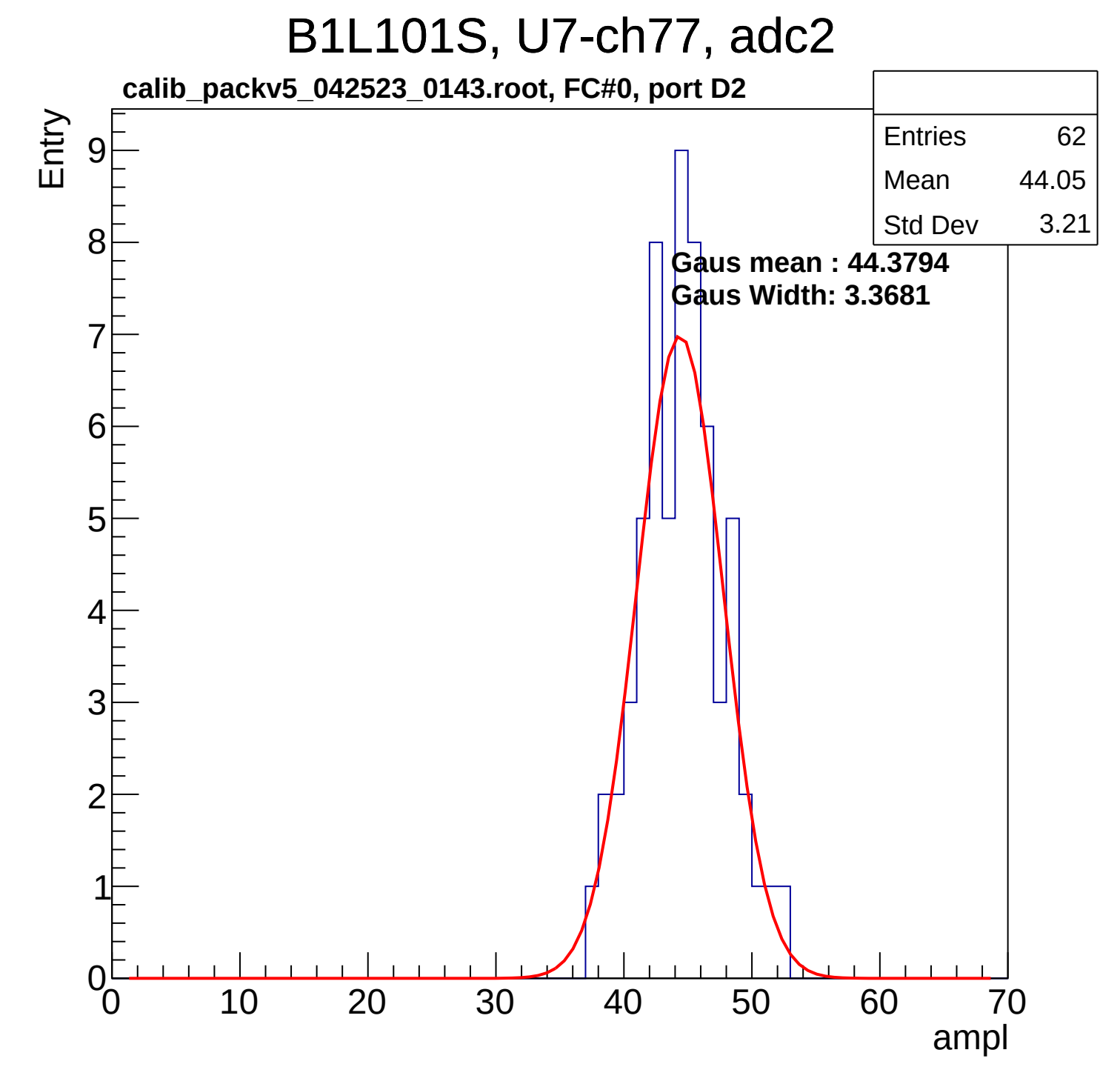
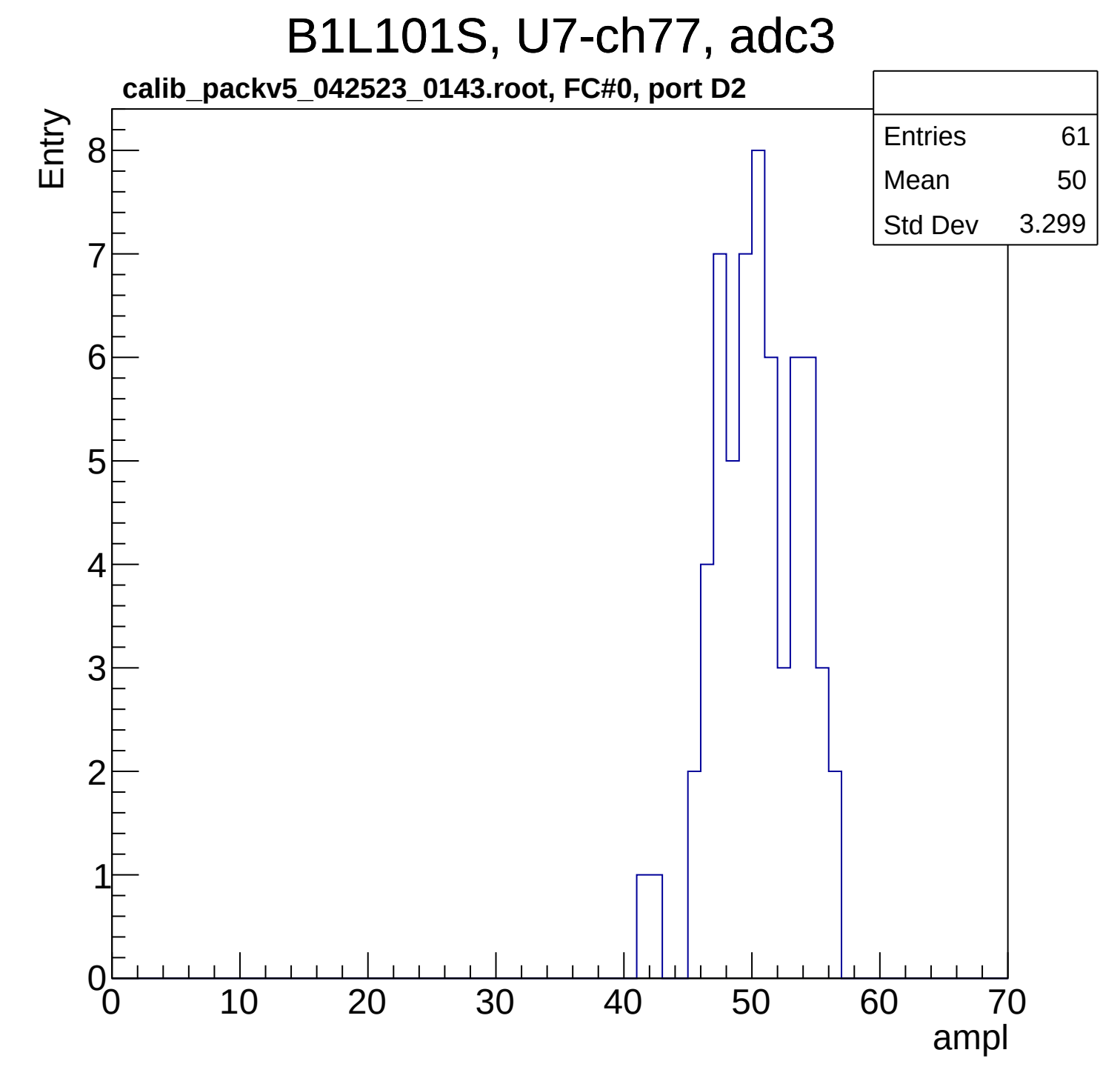
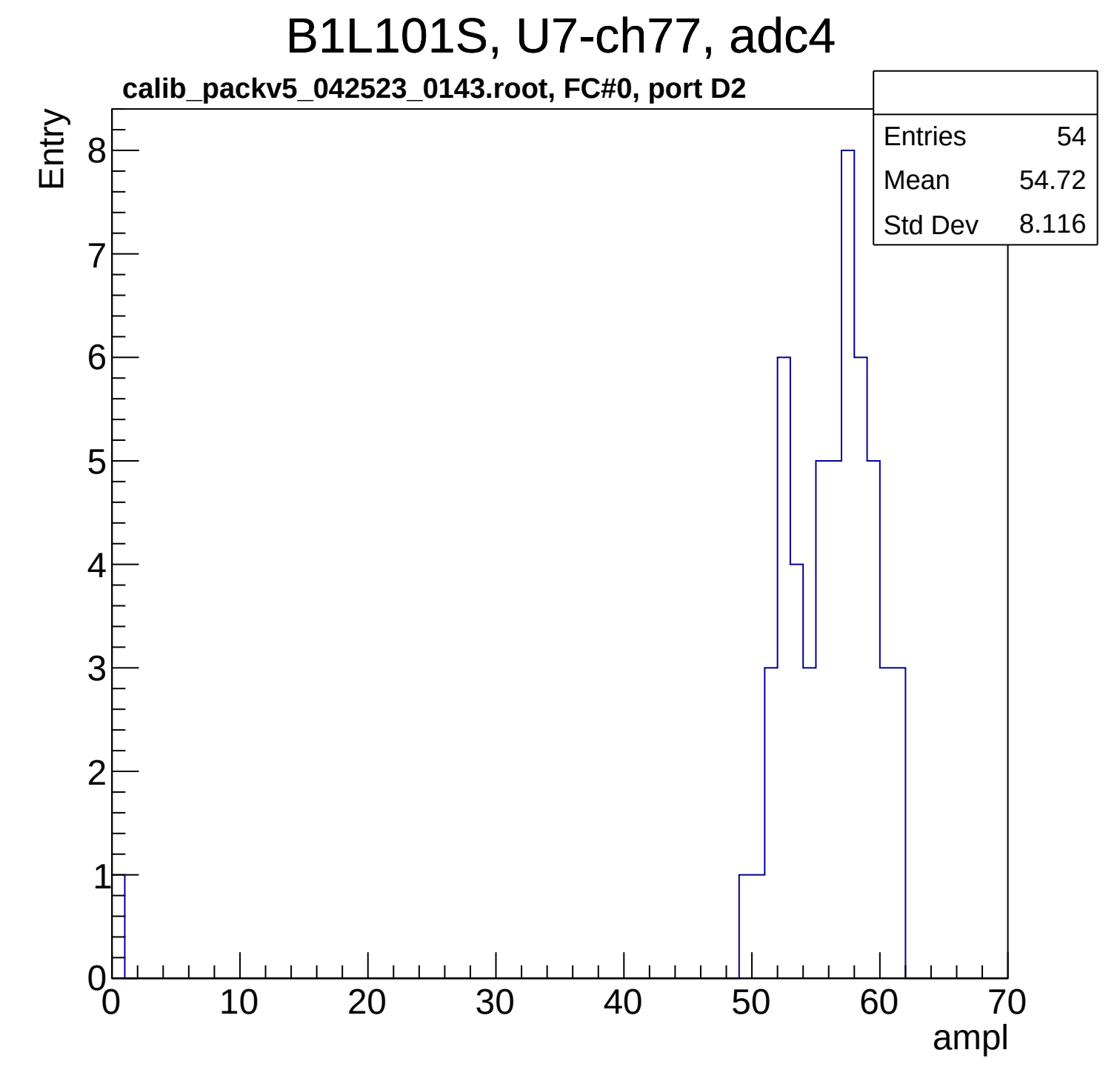

B1L101S, U7-ch77, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 44.05
Std Dev 3.21
Gaus mean : 44.3794
Gaus Width: 3.3681
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch77, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 50
Std Dev 3.299
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch77, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 54.72
Std Dev 8.116
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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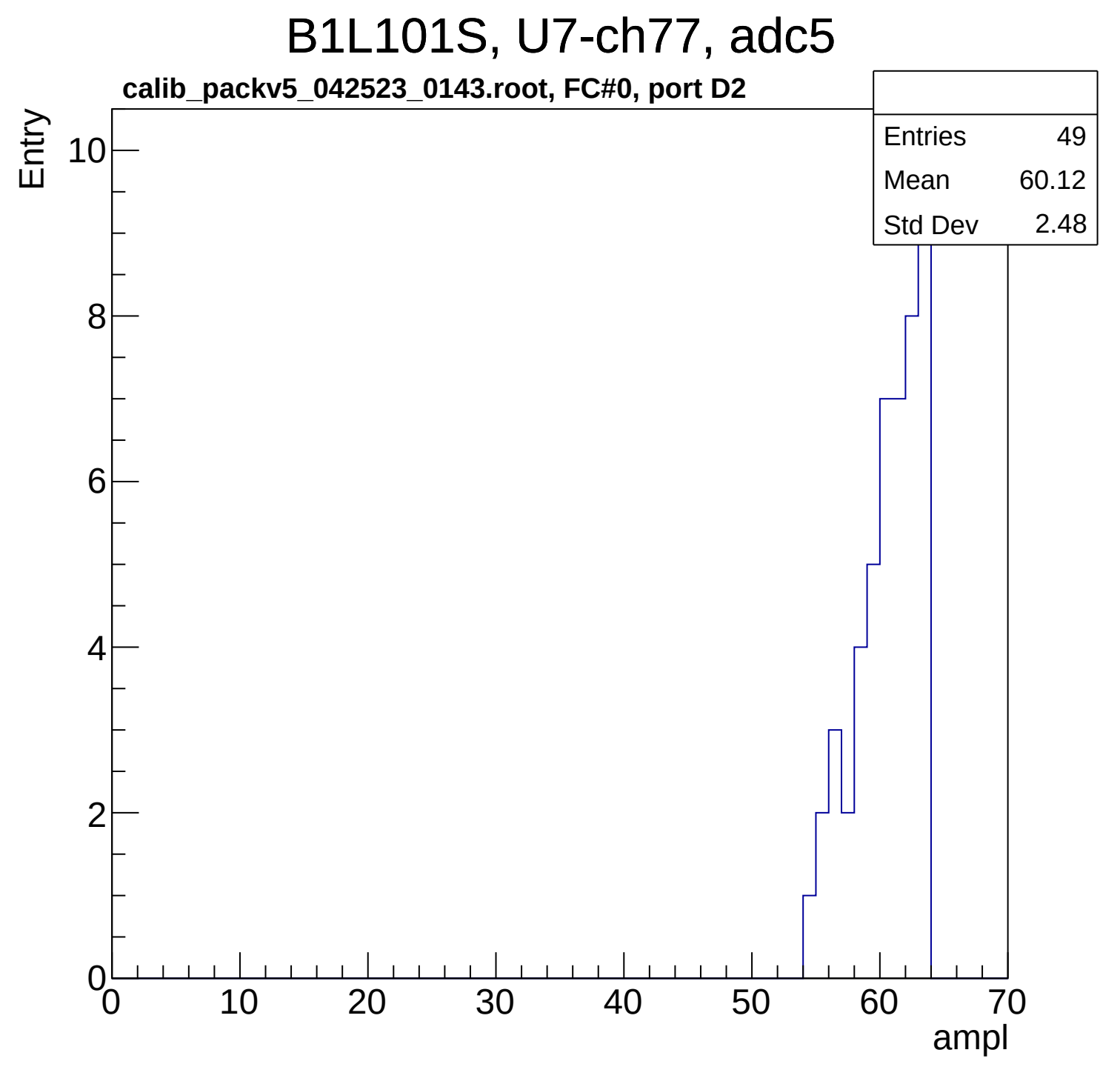
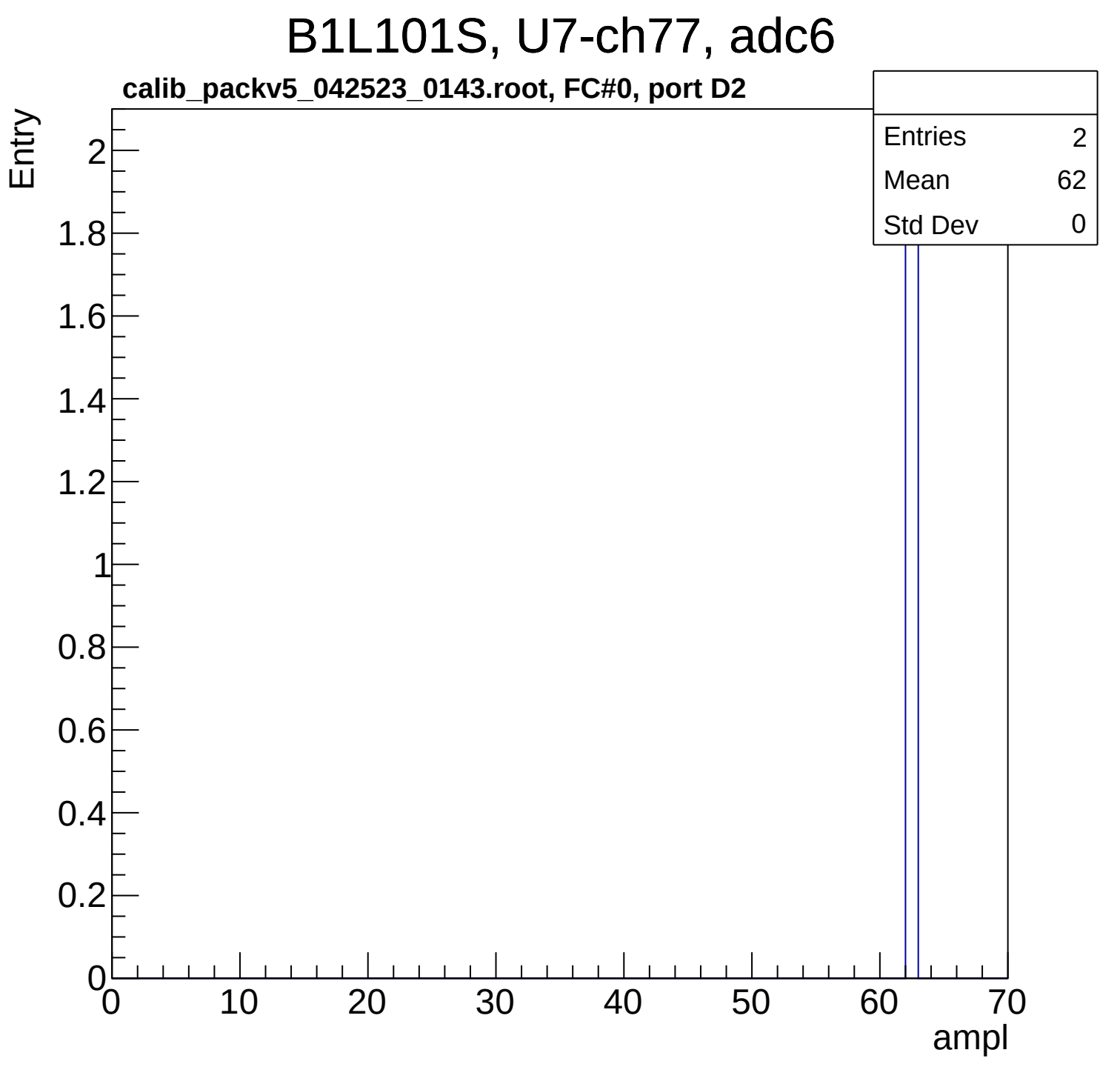
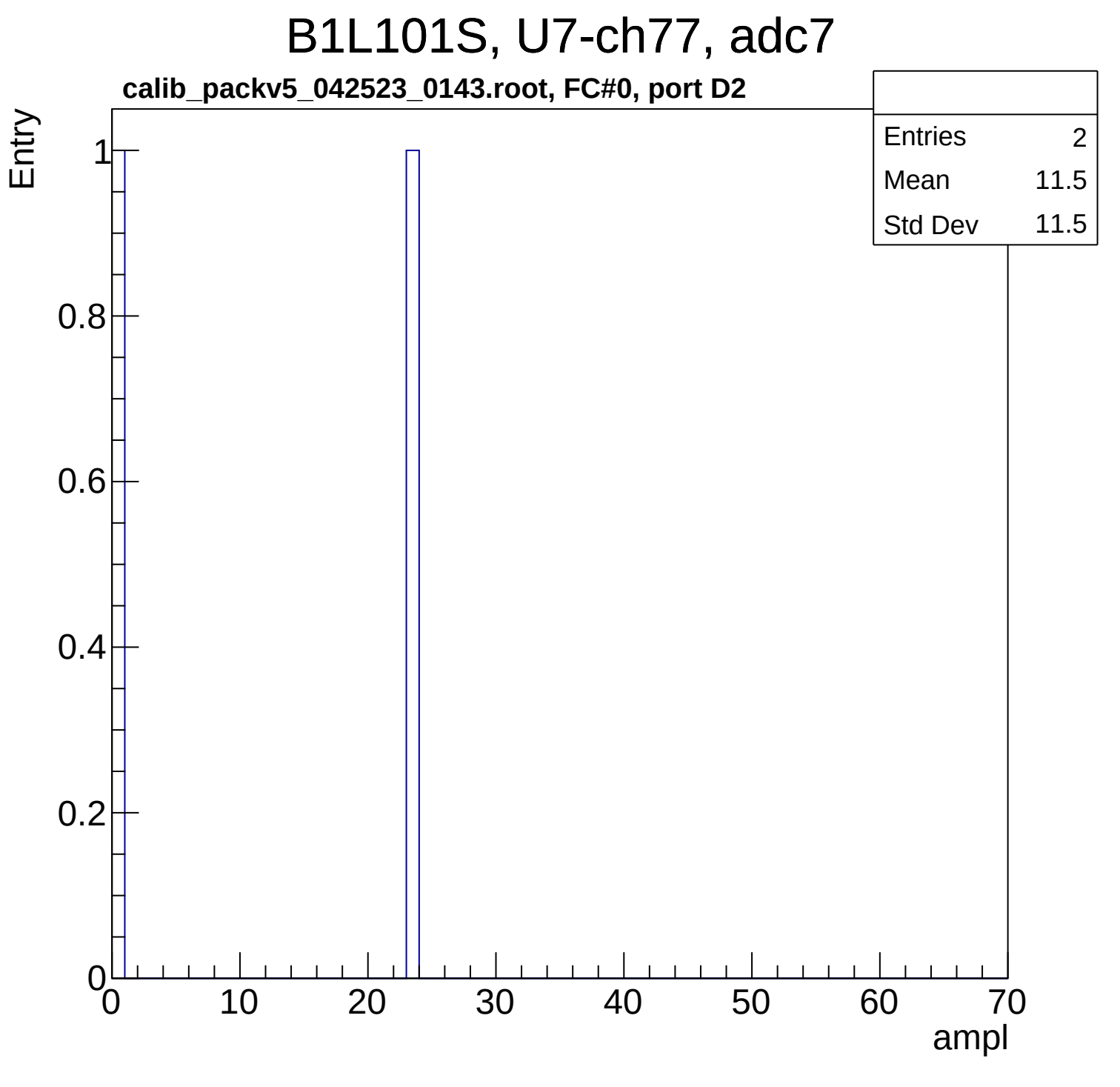
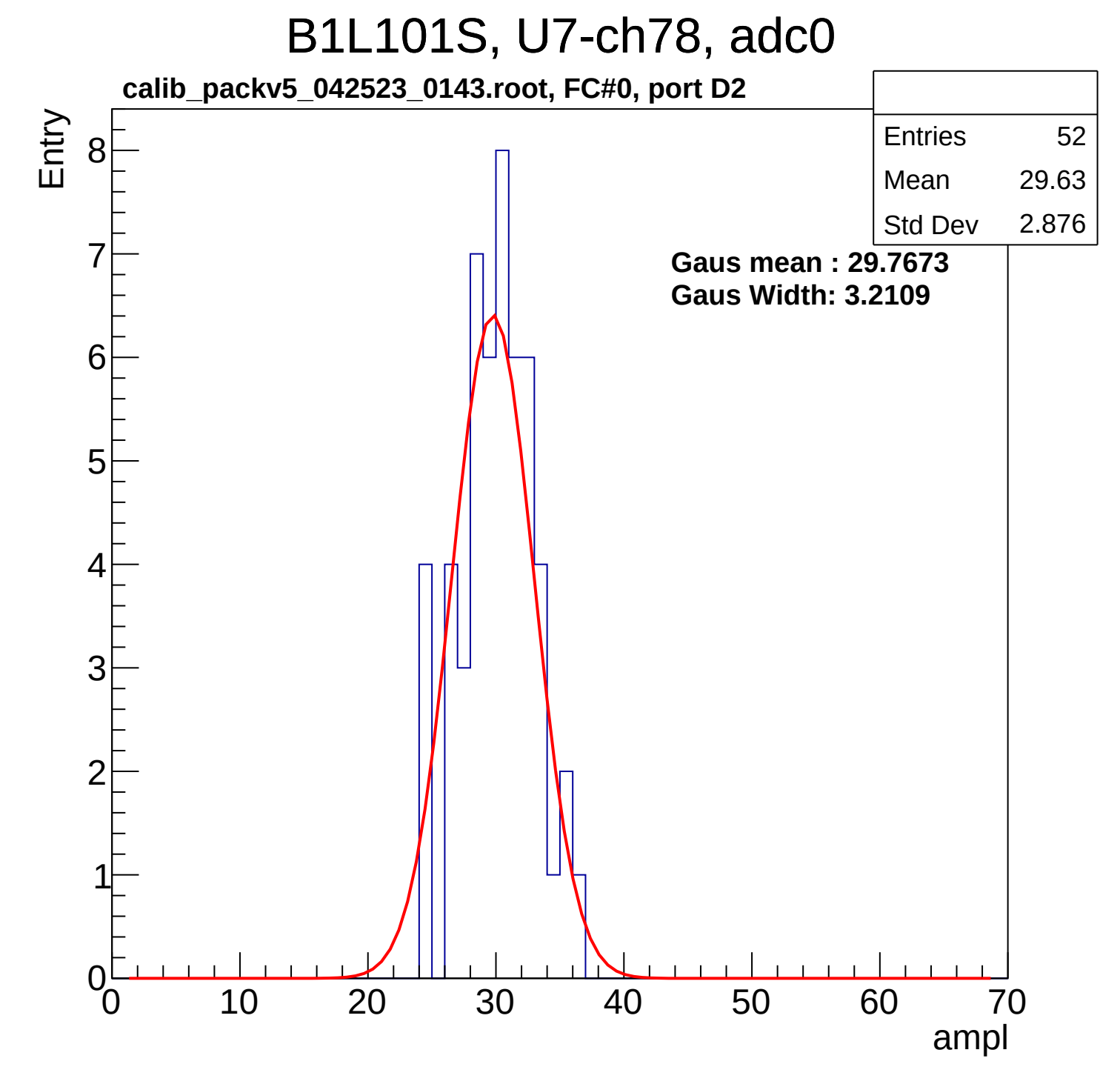
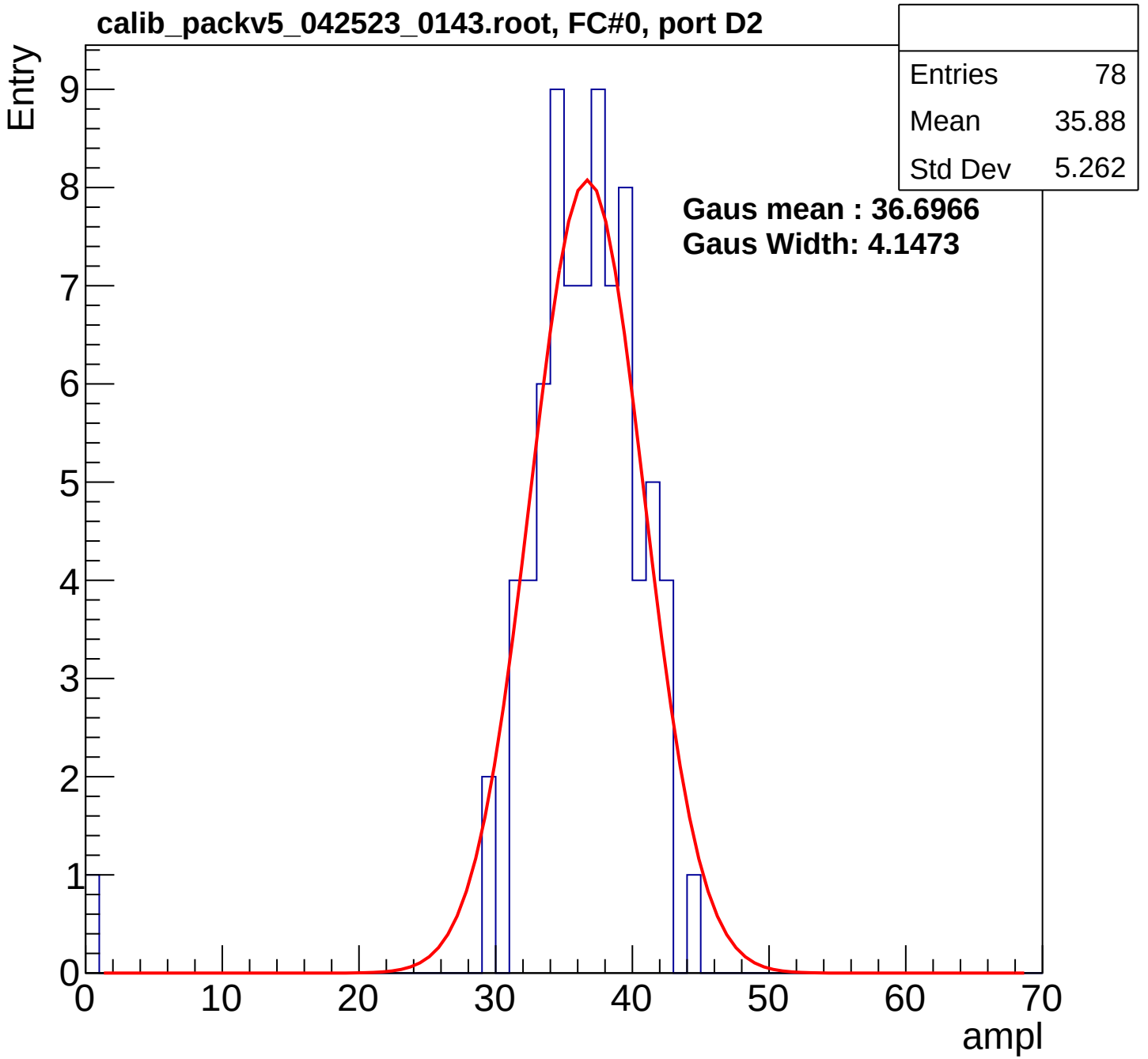
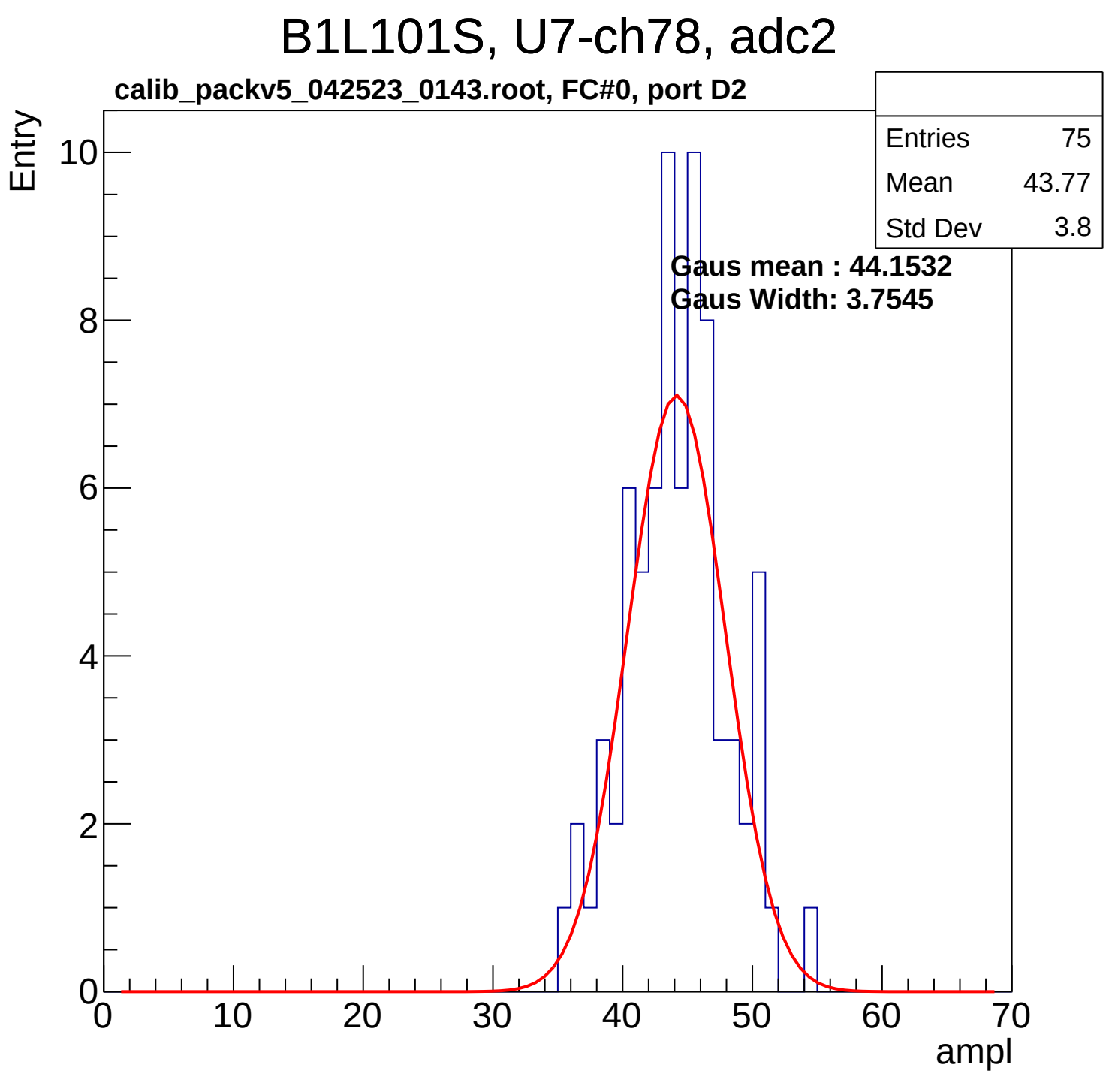

B1L101S, U7-ch77, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 60.12
Std Dev 2.48
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

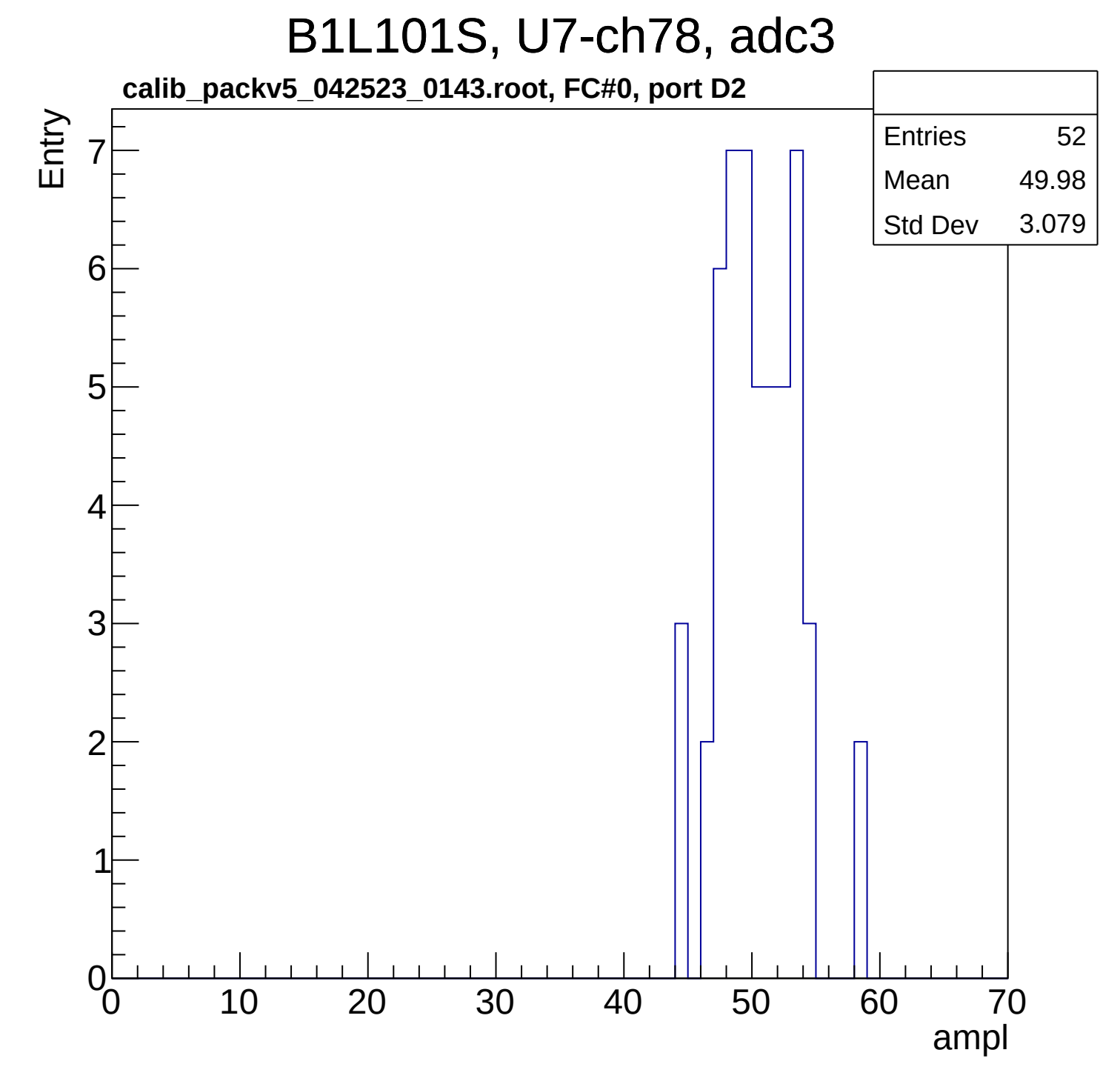

B1L101S, U7-ch77, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 62
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

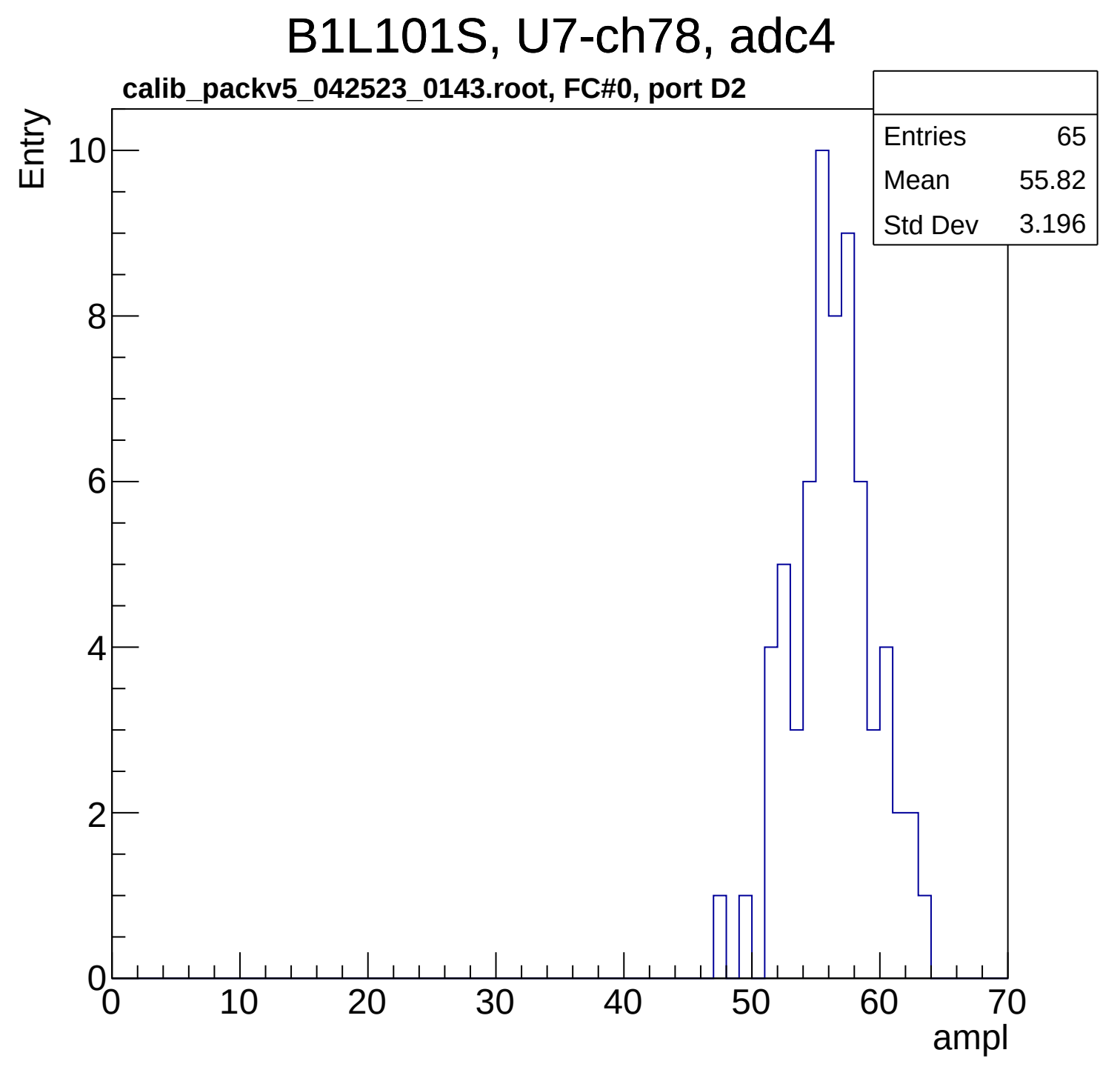

B1L101S, U7-ch77, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 11.5
Std Dev 11.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

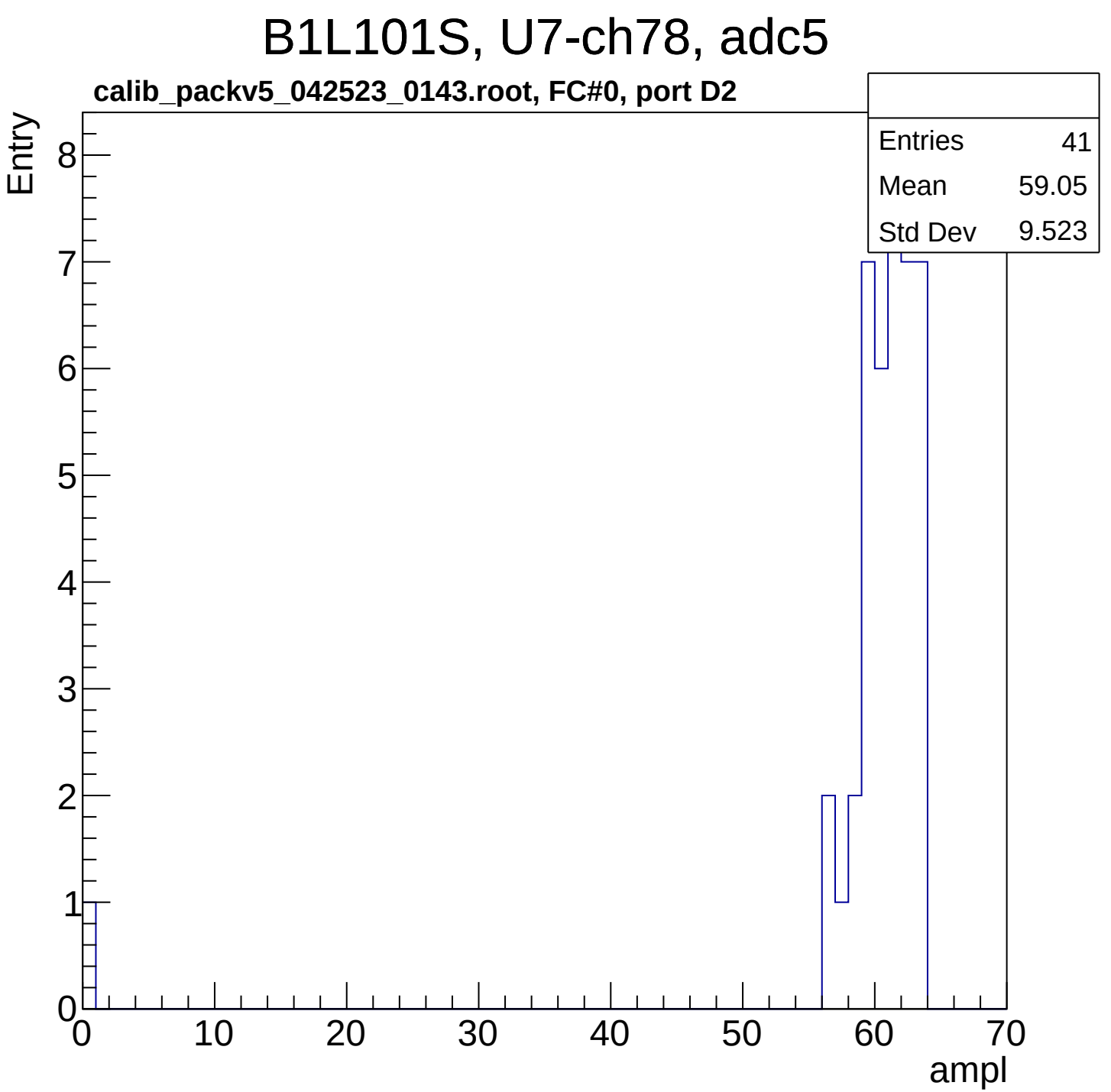

B1L101S, U7-ch78, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 29.63
Std Dev 2.876
Gaus mean : 29.7673
Gaus Width: 3.2109
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

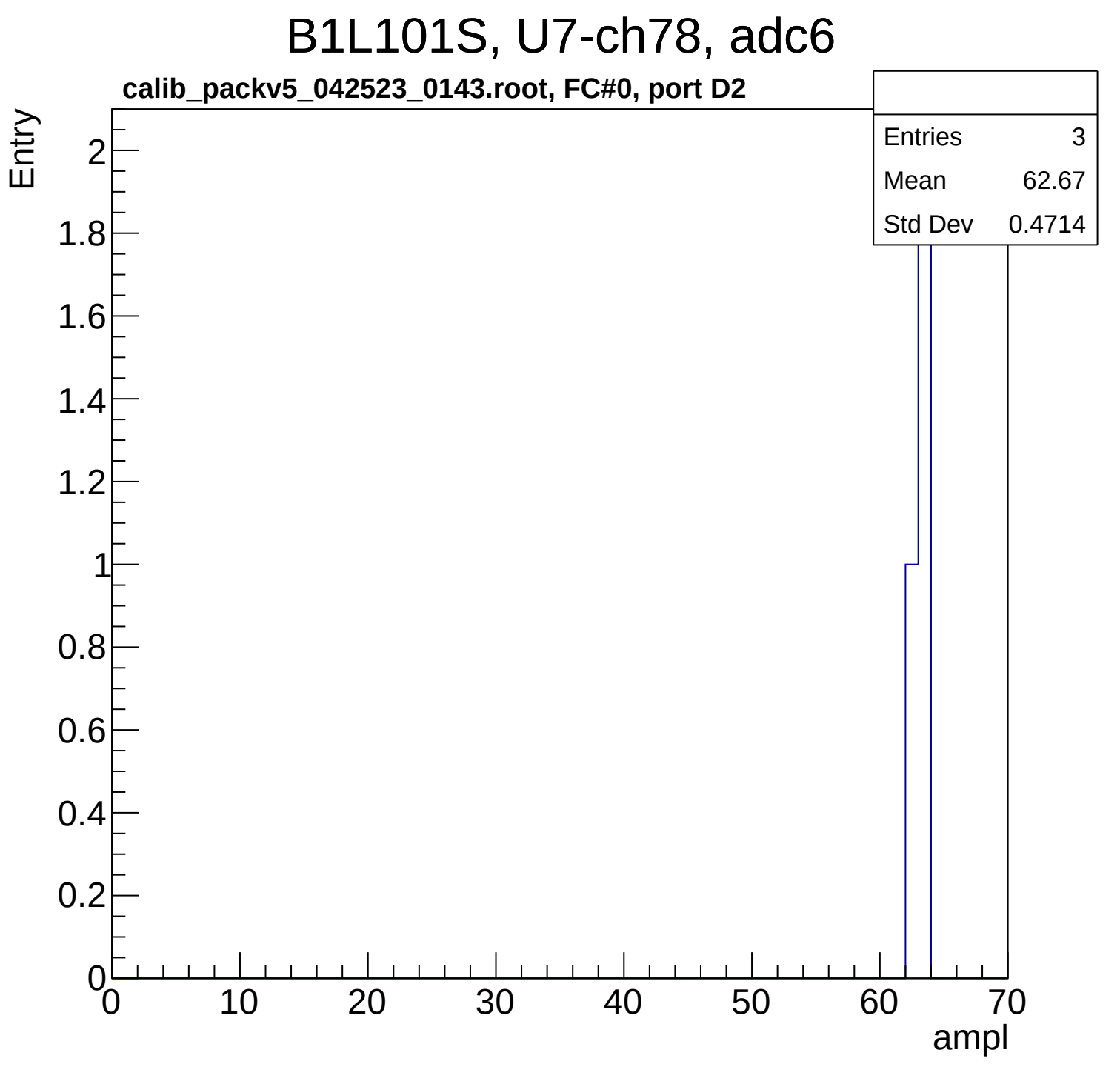

B1L101S, U7-ch78, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 35.88
Std Dev 5.262
Gaus mean : 36.6966
Gaus Width: 4.1473
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

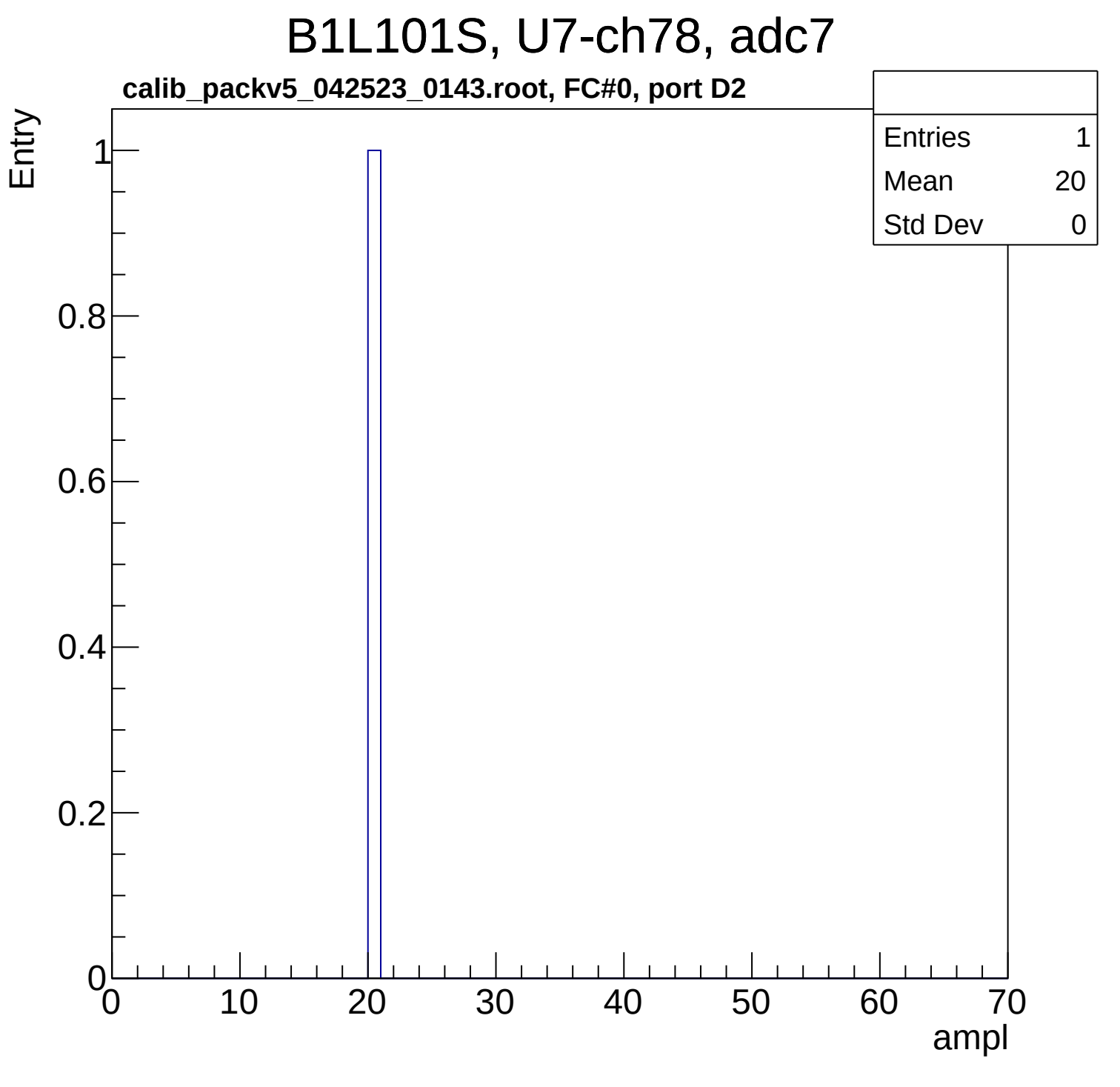

B1L101S, U7-ch78, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 43.77
Std Dev 3.8
Gaus mean : 44.1532
Gaus Width: 3.7545
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

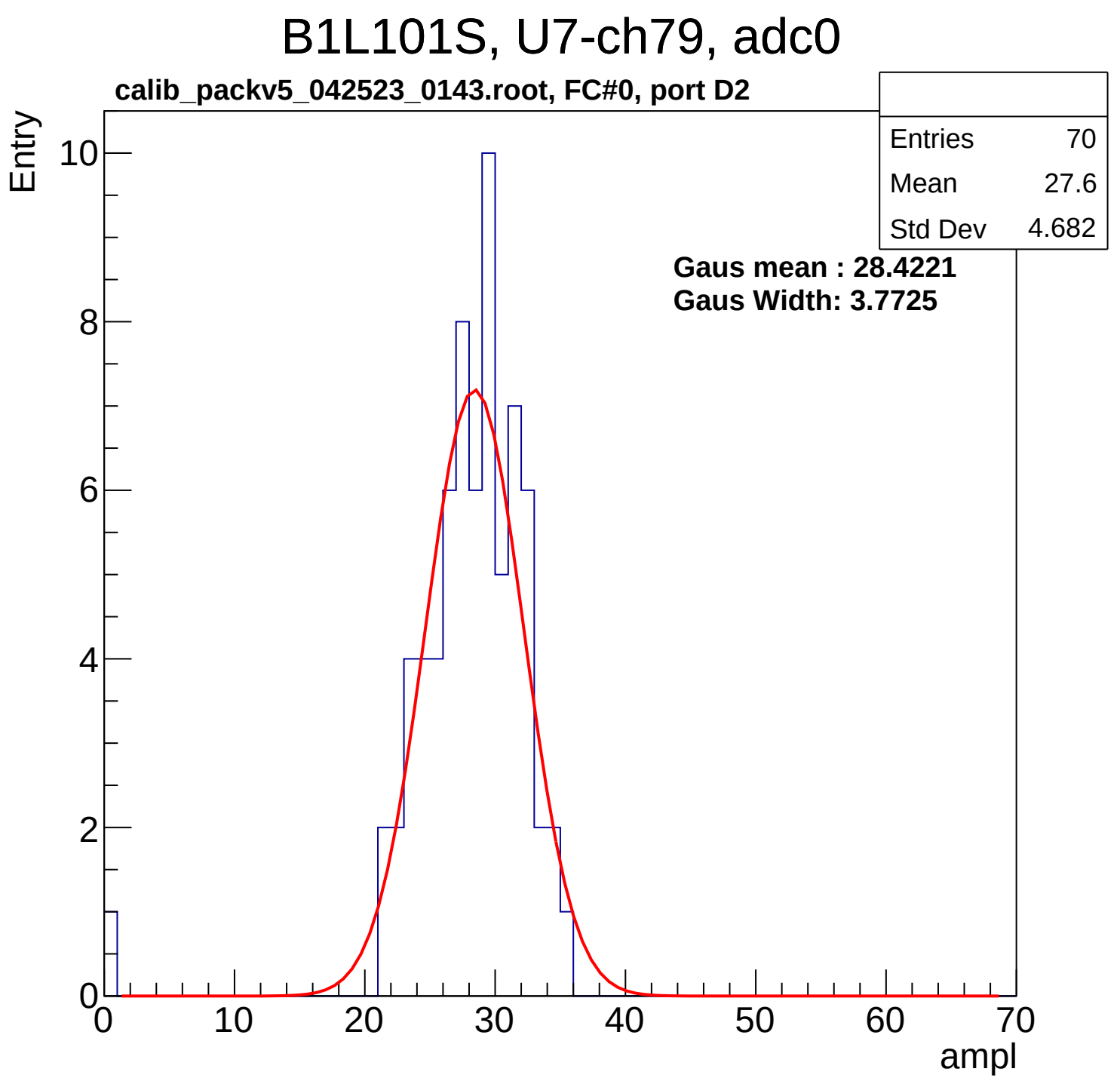

B1L101S, U7-ch78, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 49.98
Std Dev 3.079
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

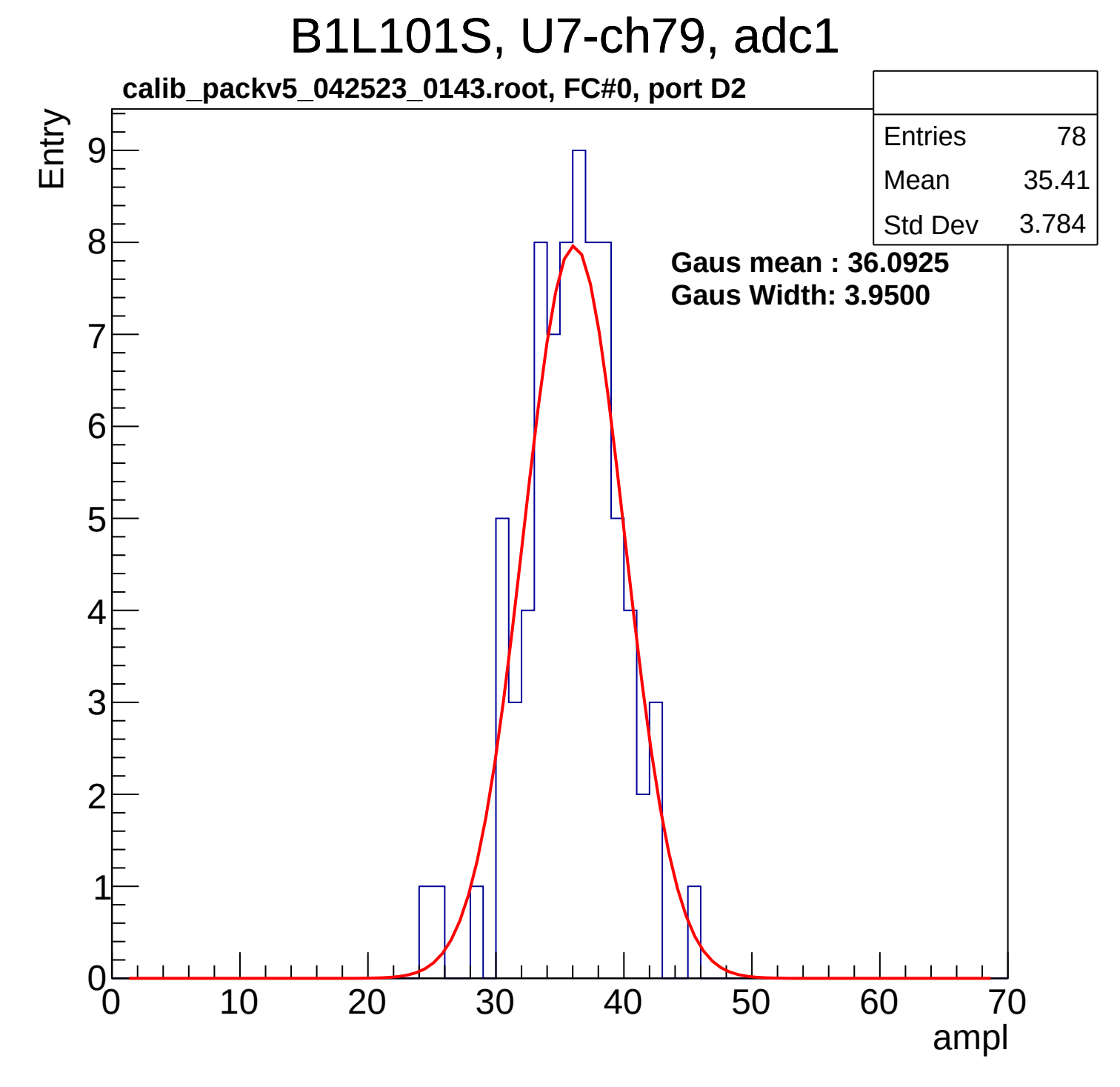

B1L101S, U7-ch78, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 55.82
Std Dev 3.196
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch78, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 41
Mean 59.05
Std Dev 9.523
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch78, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U7-ch78, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 20
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch79, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 27.6
Std Dev 4.682
Gaus mean : 28.4221
Gaus Width: 3.7725
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch79, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 35.41
Std Dev 3.784
Gaus mean : 36.0925
Gaus Width: 3.9500
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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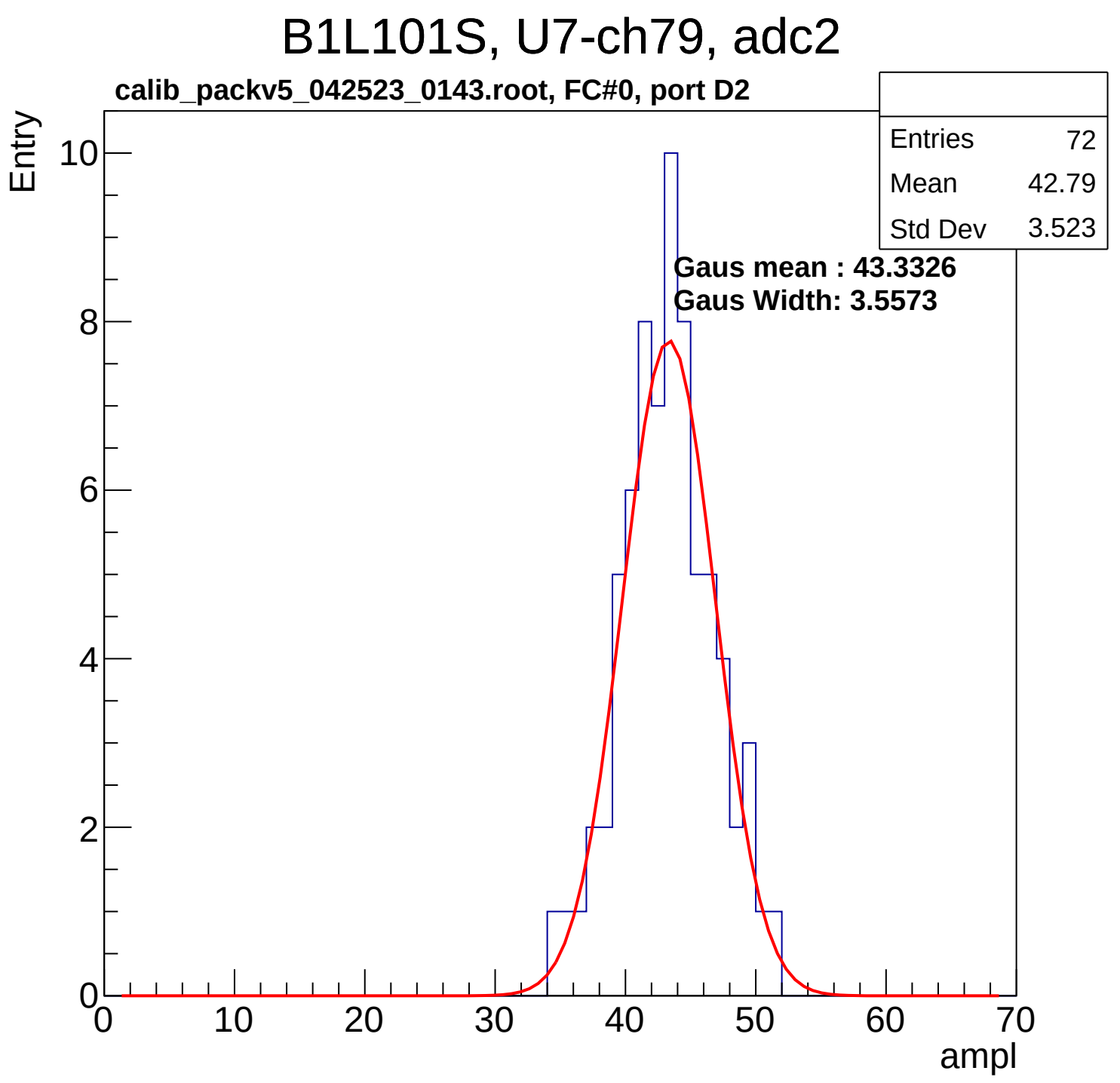
60
70


B1L101S, U7-ch79, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 42.79
Std Dev 3.523
Gaus mean : 43.3326
Gaus Width: 3.5573
Entry
ampl
0
2
4
6
8
10
0
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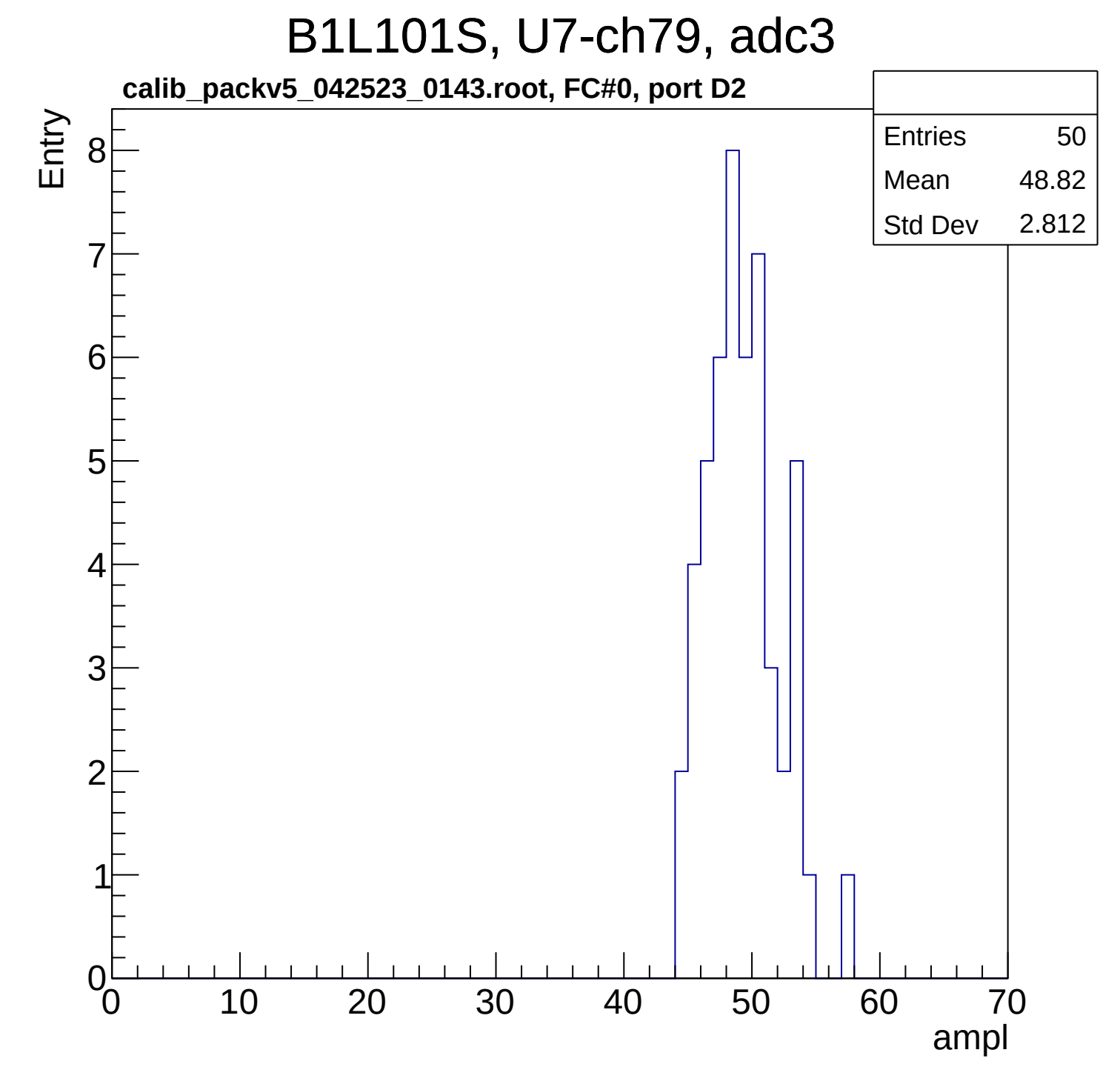
20
30
40
50
60
70


B1L101S, U7-ch79, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 48.82
Std Dev 2.812
Entry
ampl
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60
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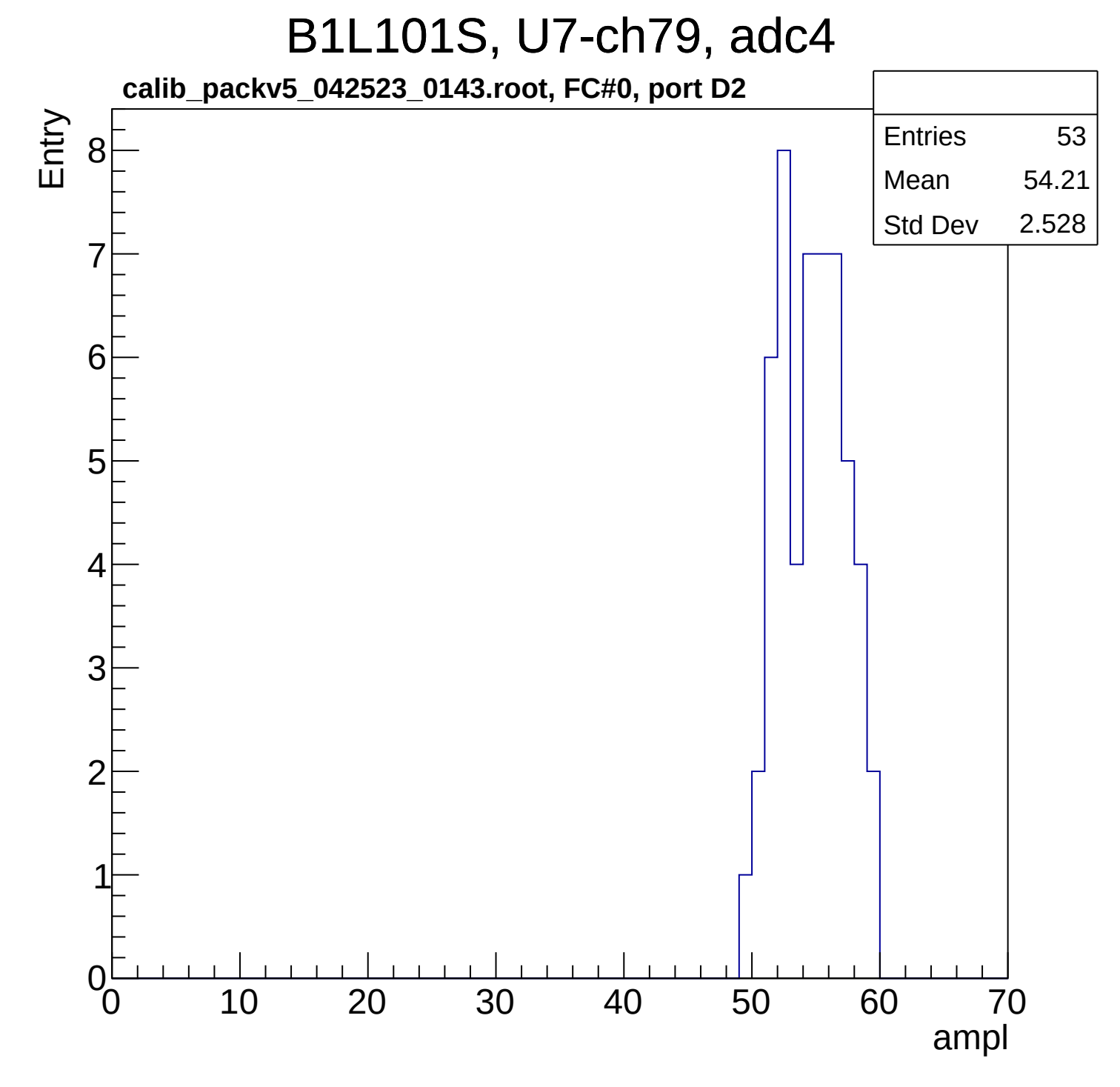
B1L101S, U7-ch79, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 54.21
Std Dev 2.528
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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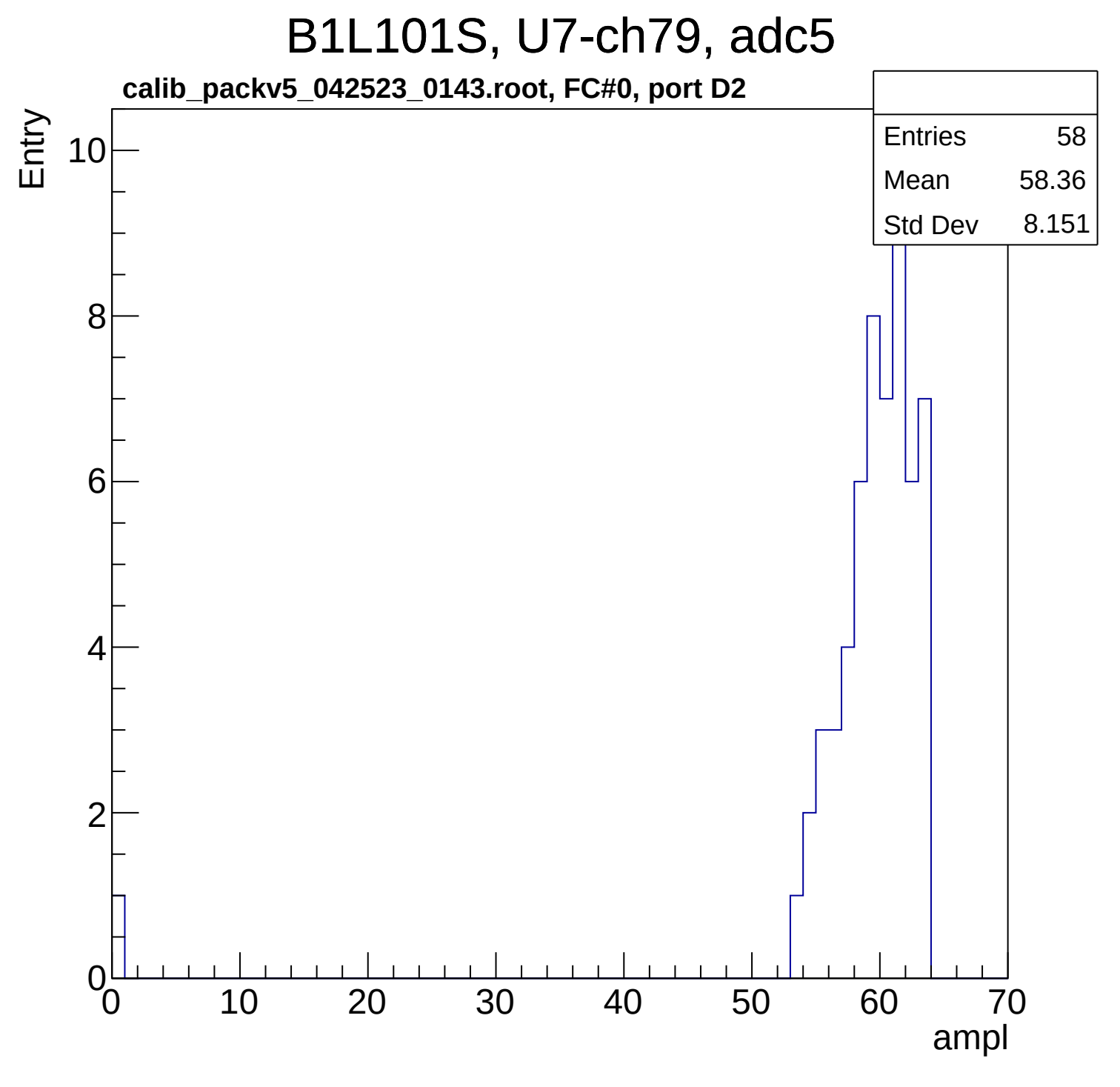
B1L101S, U7-ch79, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 58.36
Std Dev 8.151
Entry
ampl
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2
4
6
8
10
0
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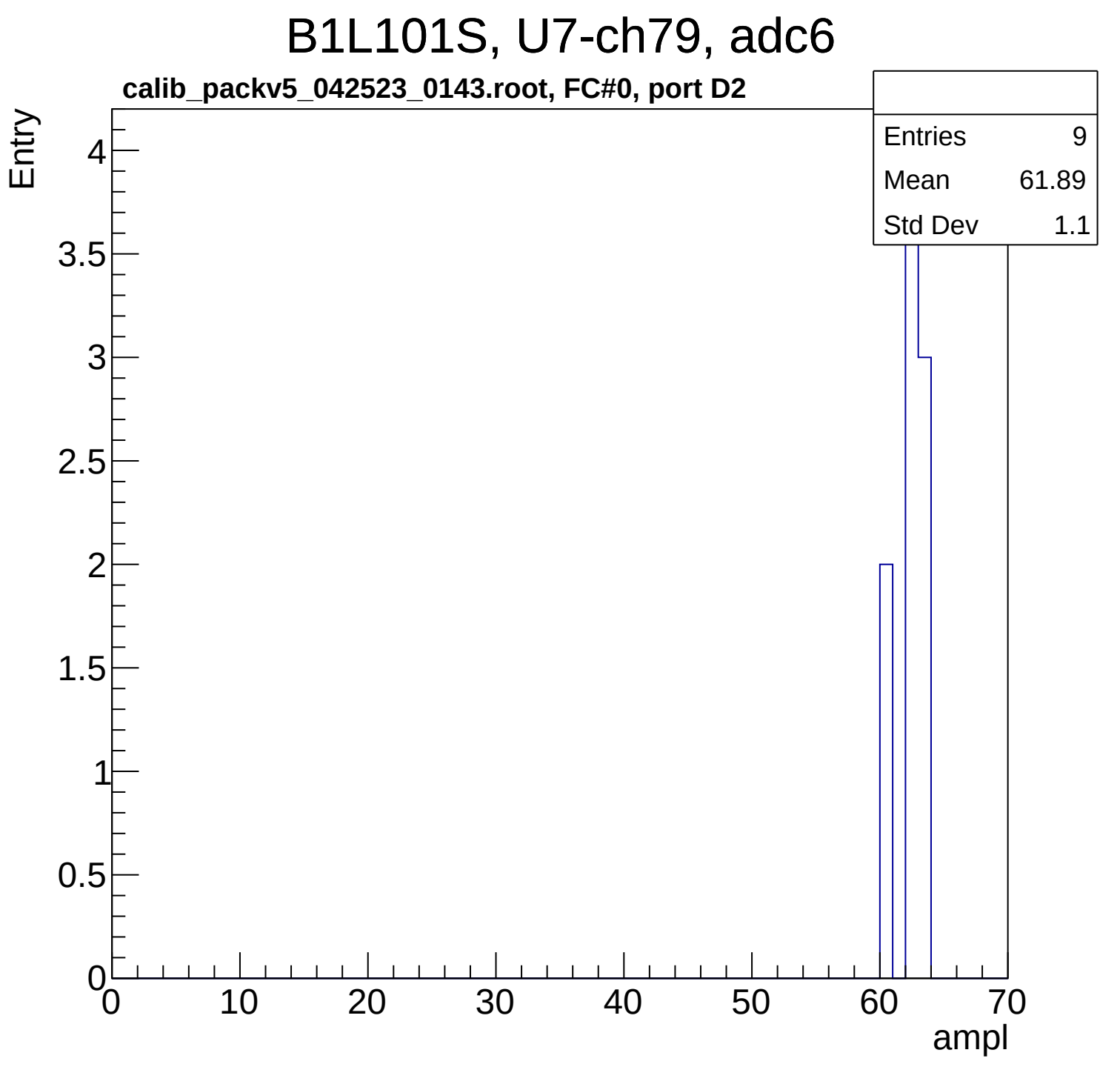
20
30
40
50
60
70


B1L101S, U7-ch79, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 61.89
Std Dev 1.1
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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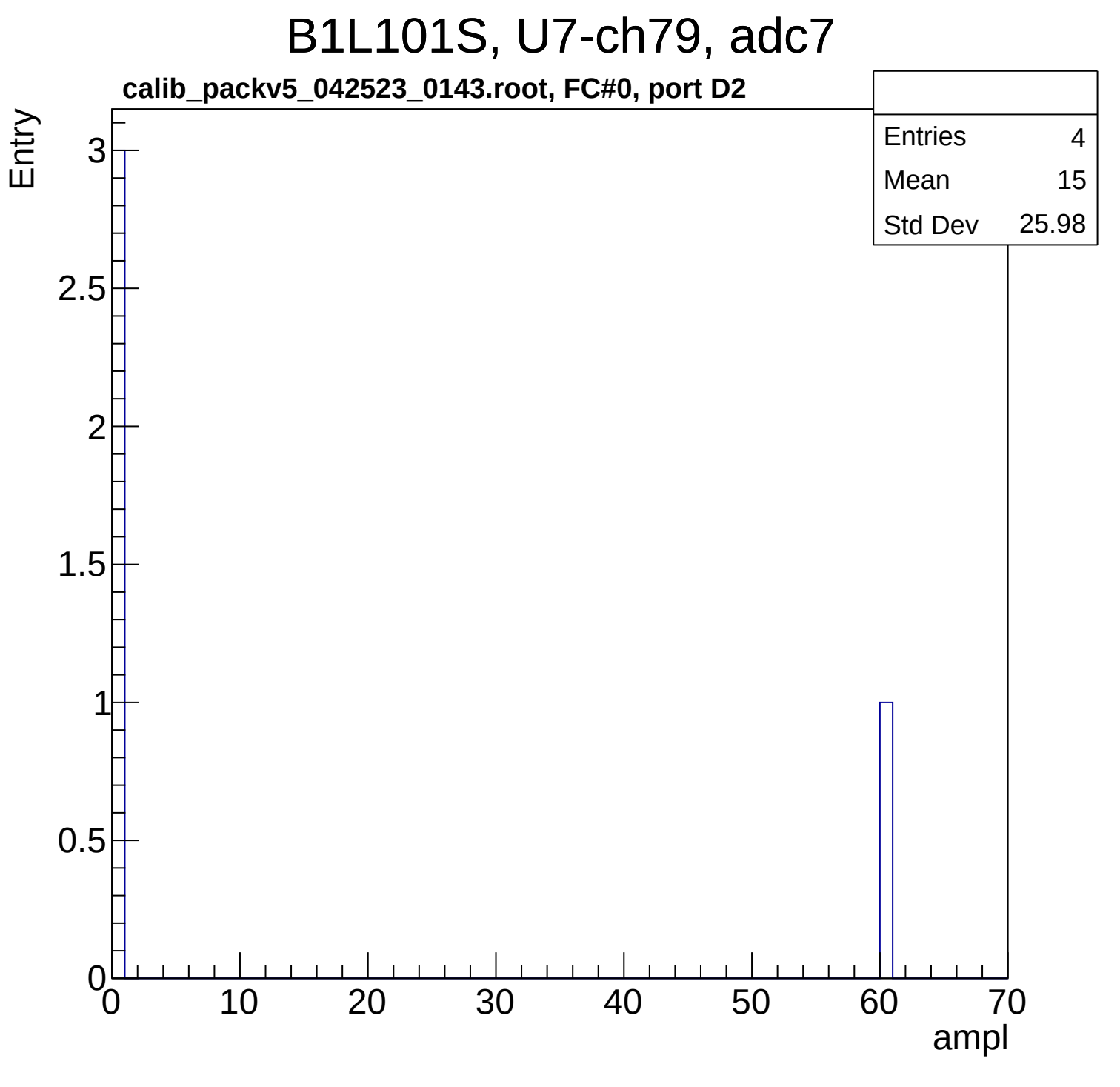
B1L101S, U7-ch79, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 15
Std Dev 25.98
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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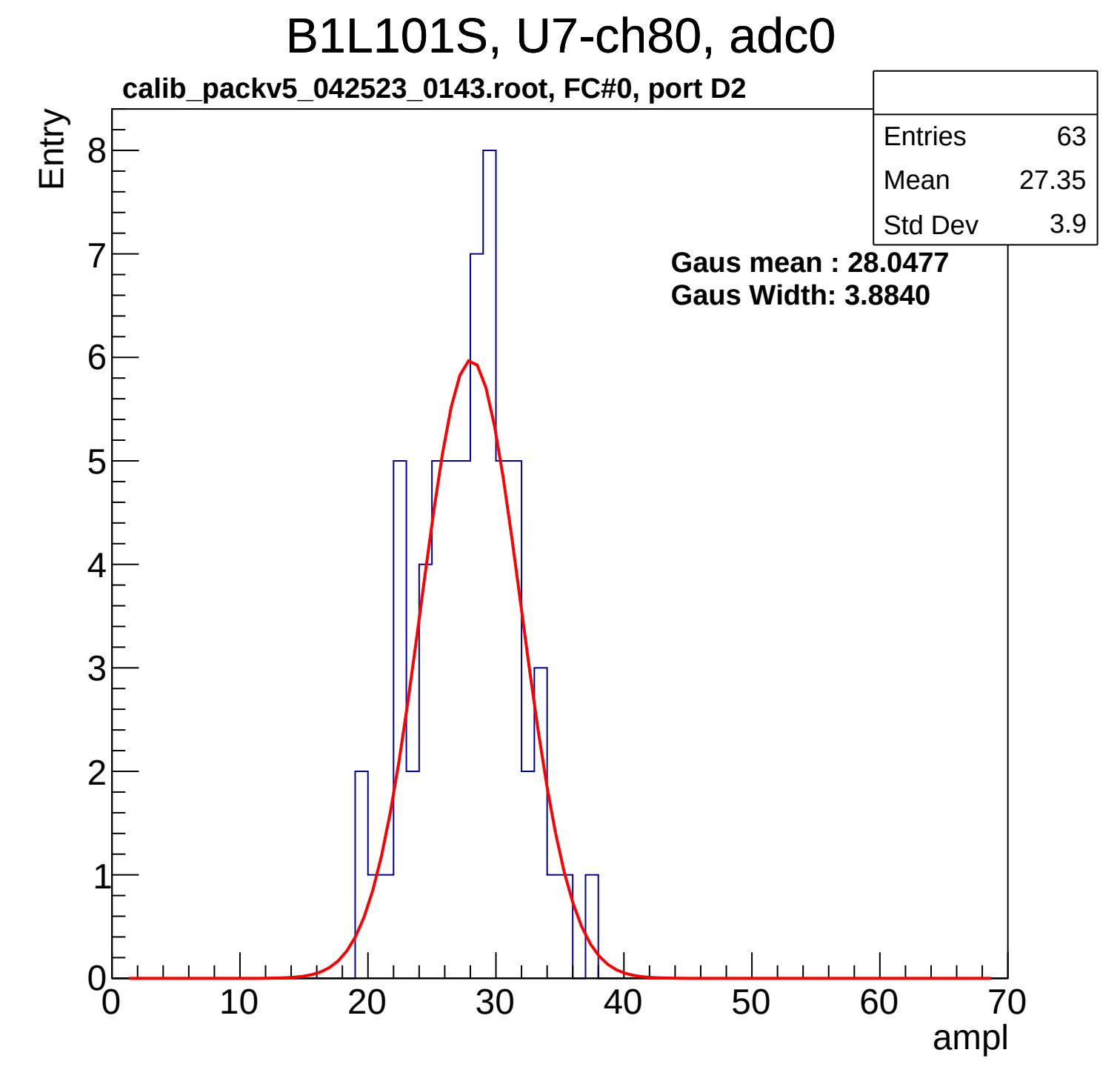
20
30
40
50
60
70


B1L101S, U7-ch80, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 27.35
Std Dev 3.9
Gaus mean : 28.0477
Gaus Width: 3.8840
Entry
ampl
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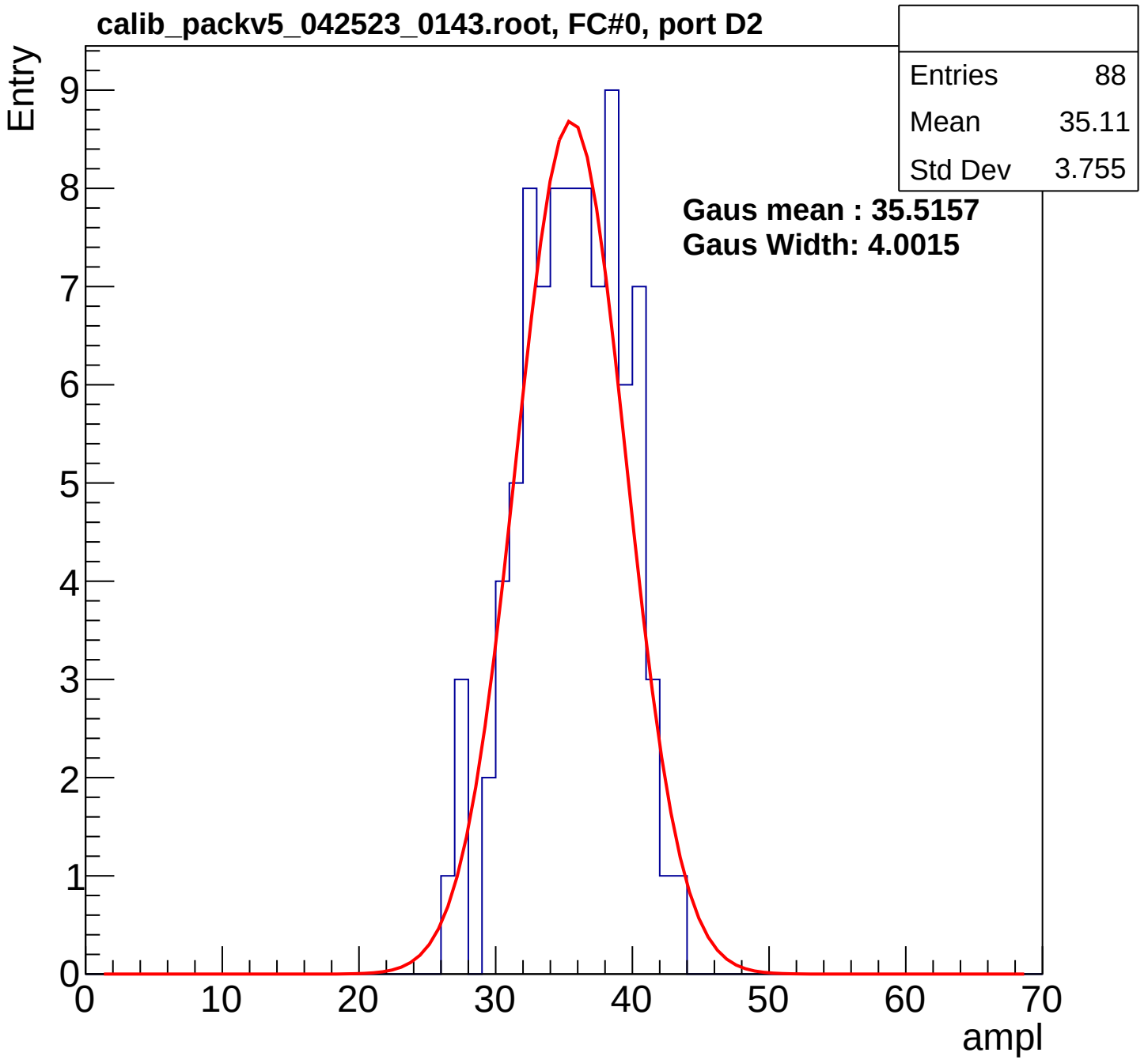
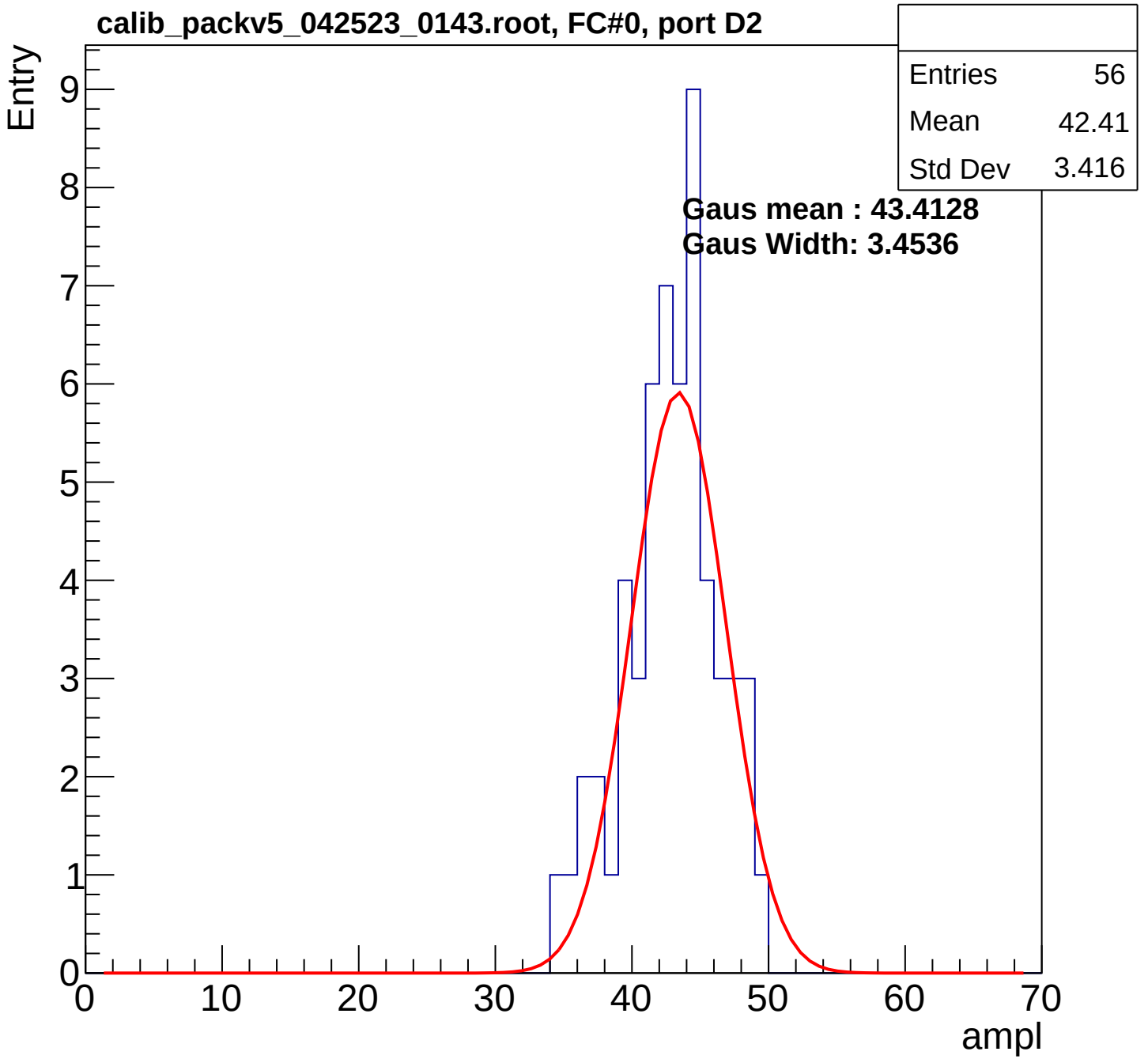
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch80, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 88
Mean 35.11
Std Dev 3.755
Gaus mean : 35.5157
Gaus Width: 4.0015
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L101S, U7-ch80, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 42.41
Std Dev 3.416
Gaus mean : 43.4128
Gaus Width: 3.4536
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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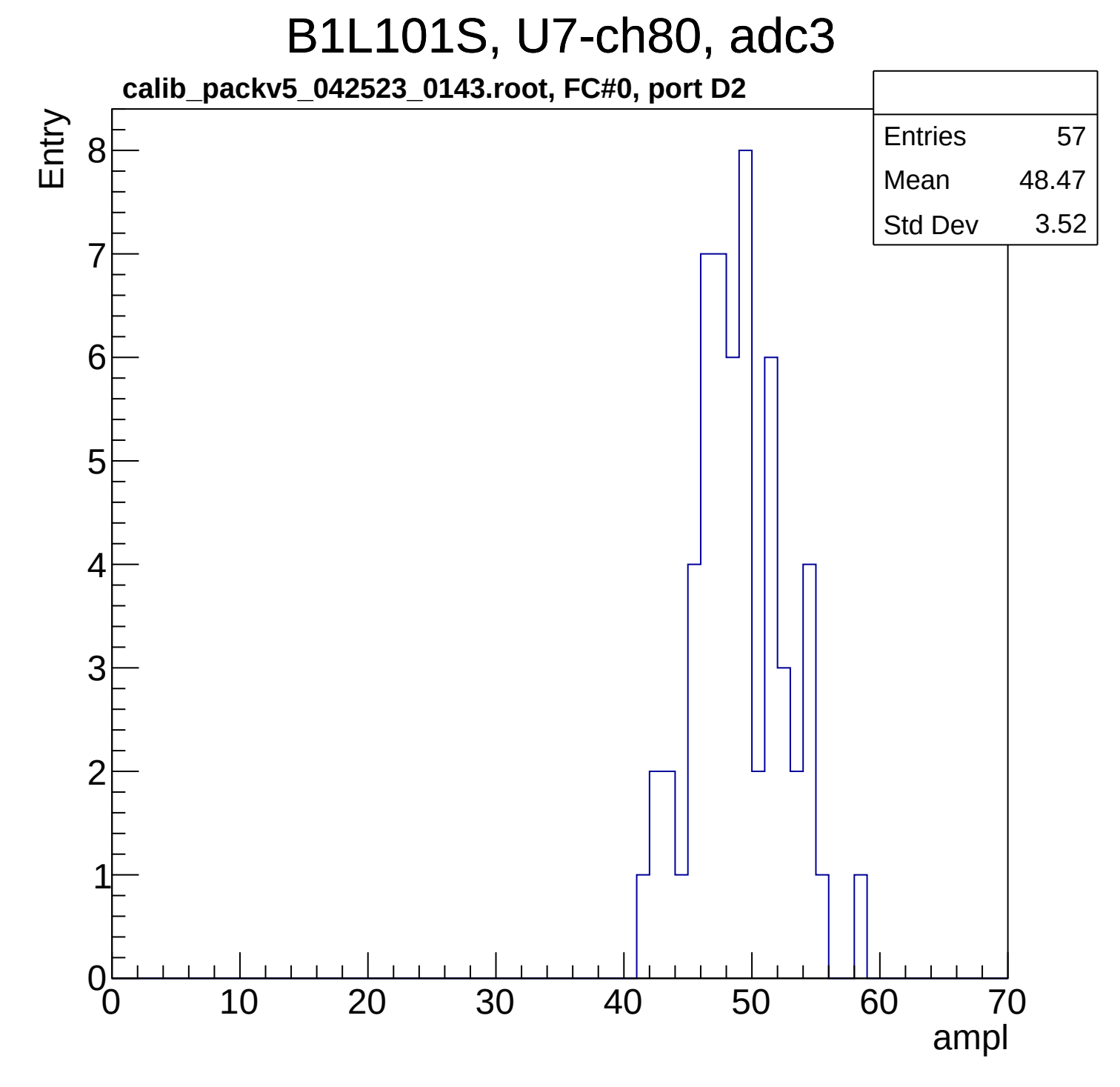
B1L101S, U7-ch80, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 48.47
Std Dev 3.52
Entry
ampl
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1
2
3
4
5
6
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0
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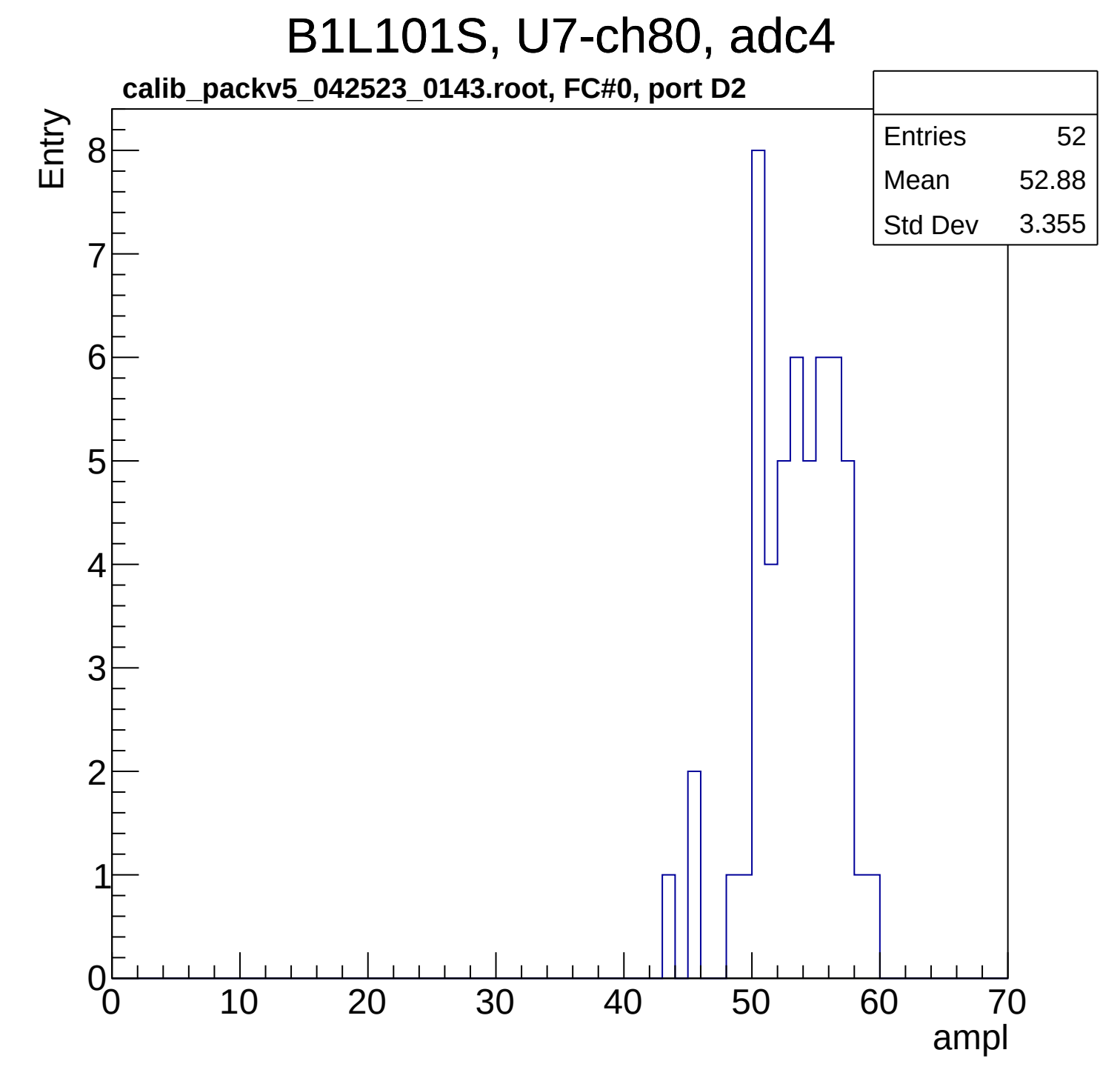
B1L101S, U7-ch80, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 52.88
Std Dev 3.355
Entry
ampl
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2
3
4
5
6
7
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0
10
20
30
40
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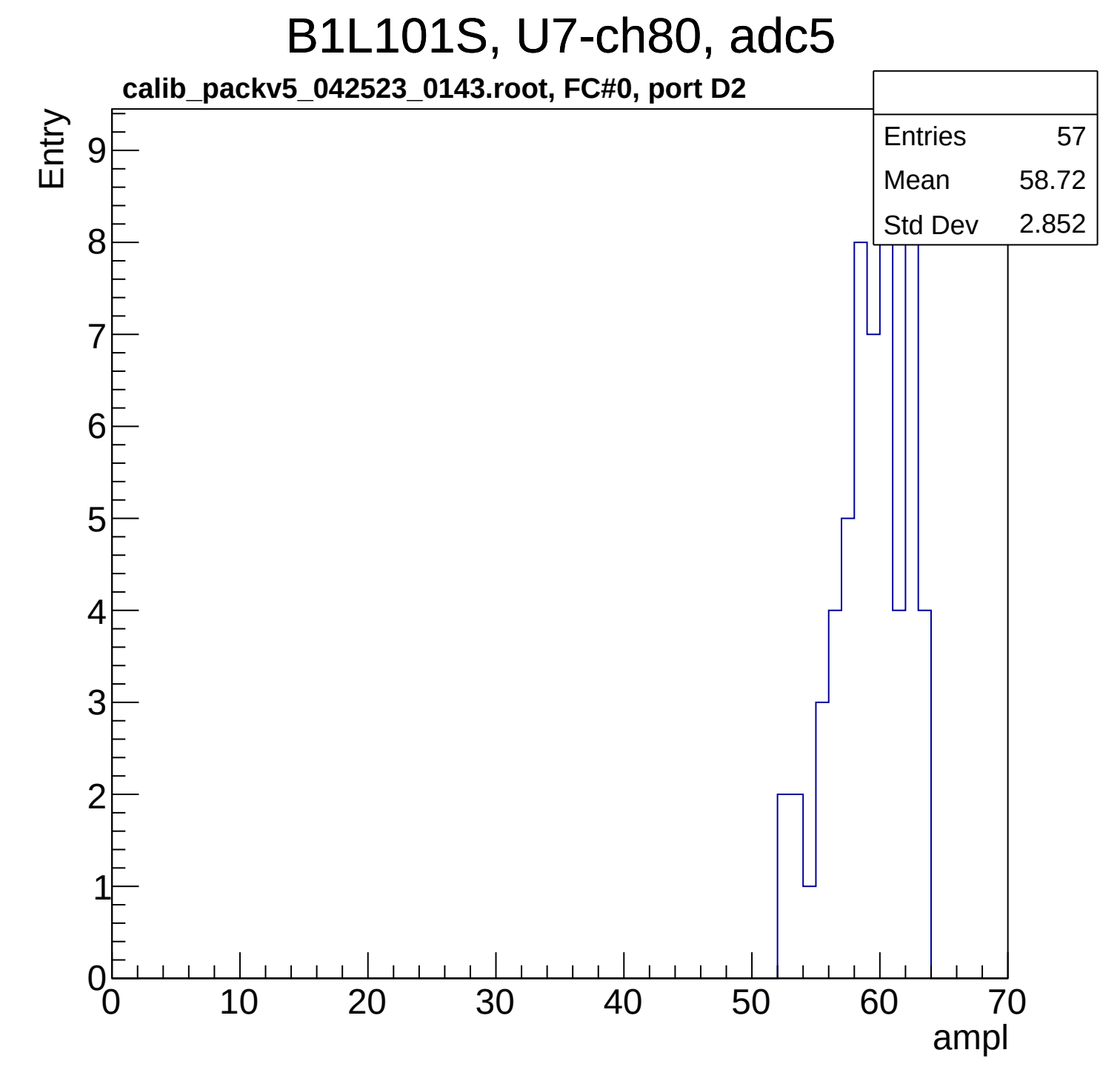
B1L101S, U7-ch80, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 58.72
Std Dev 2.852
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
50
60
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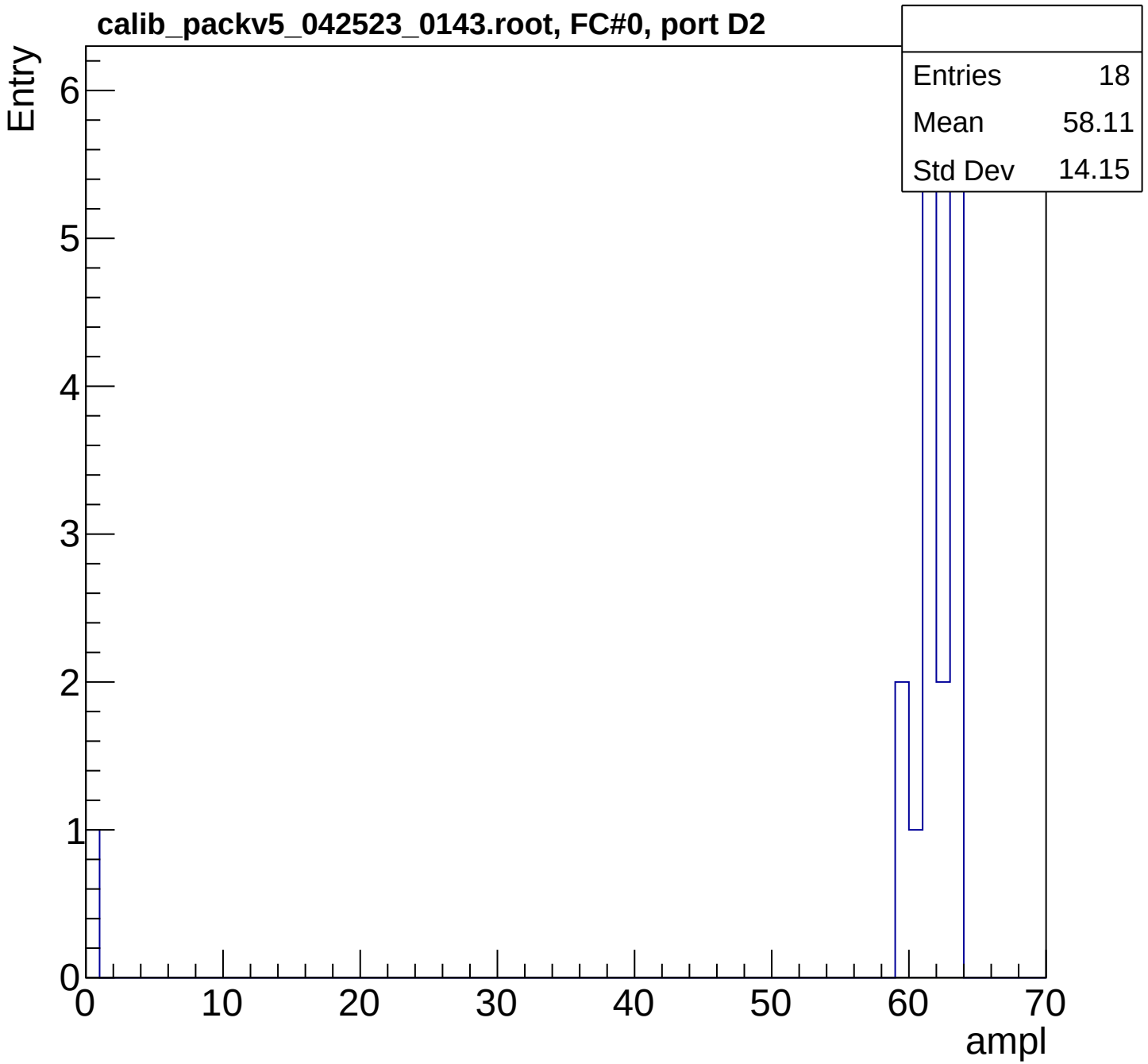
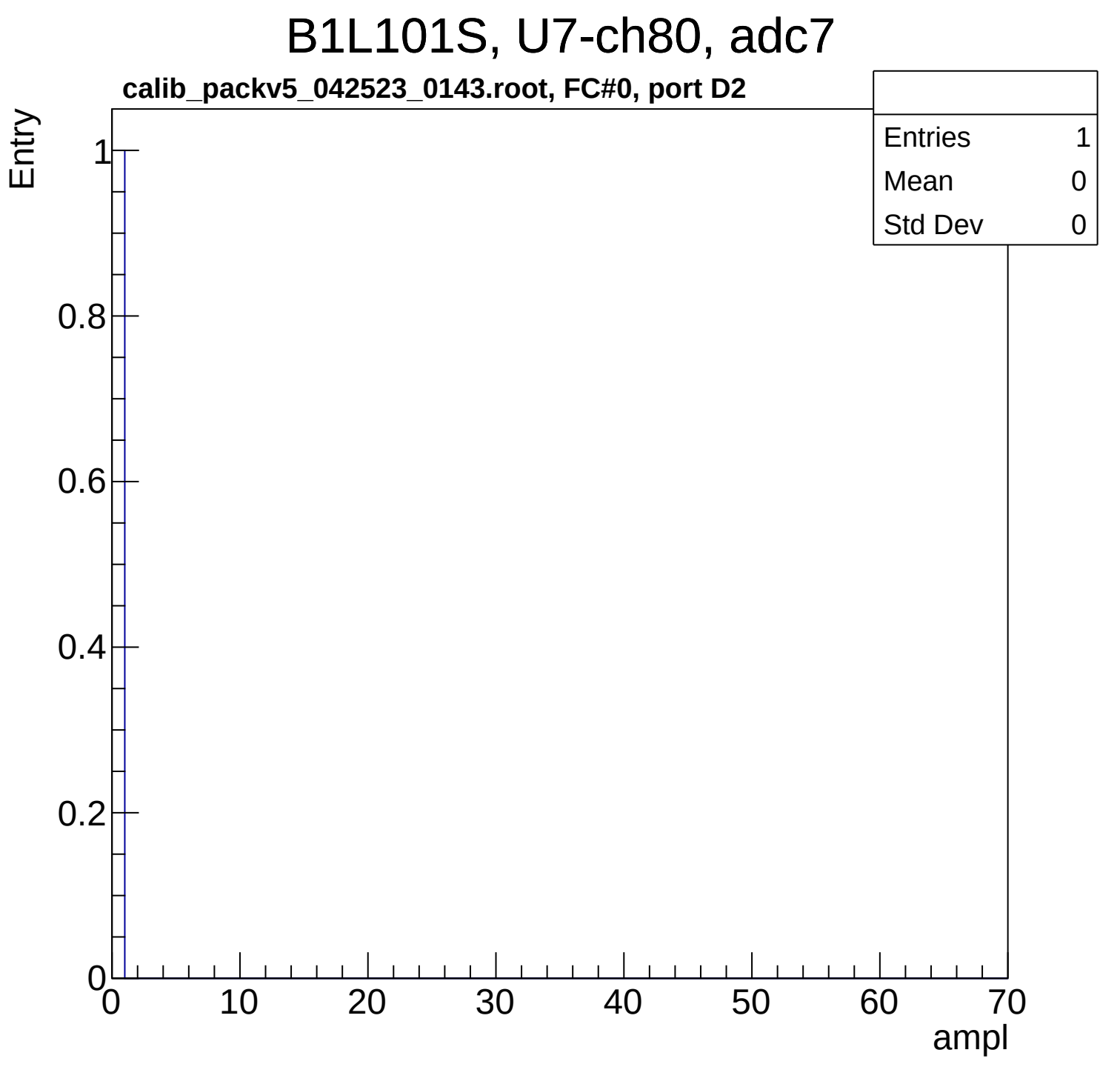
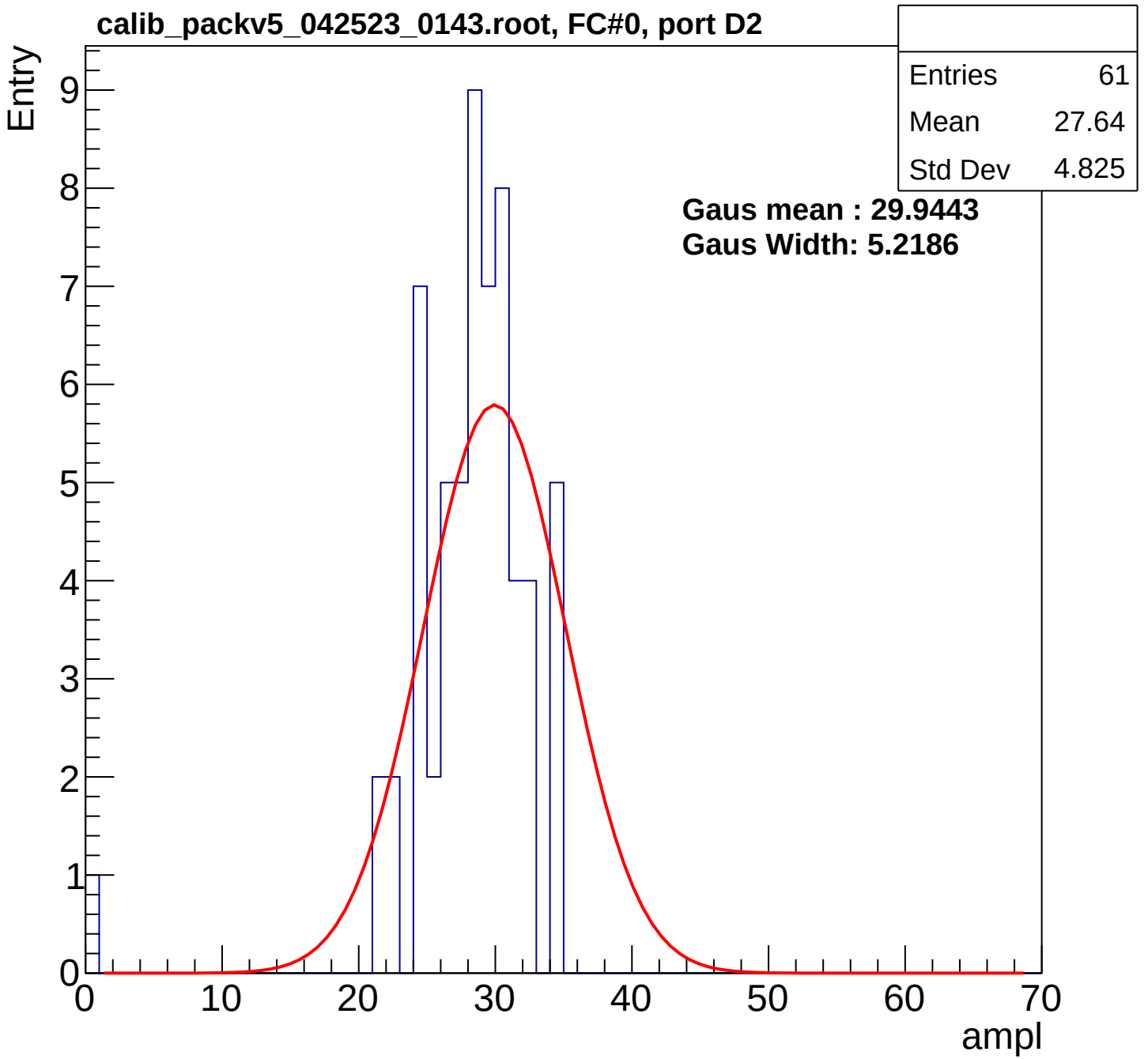
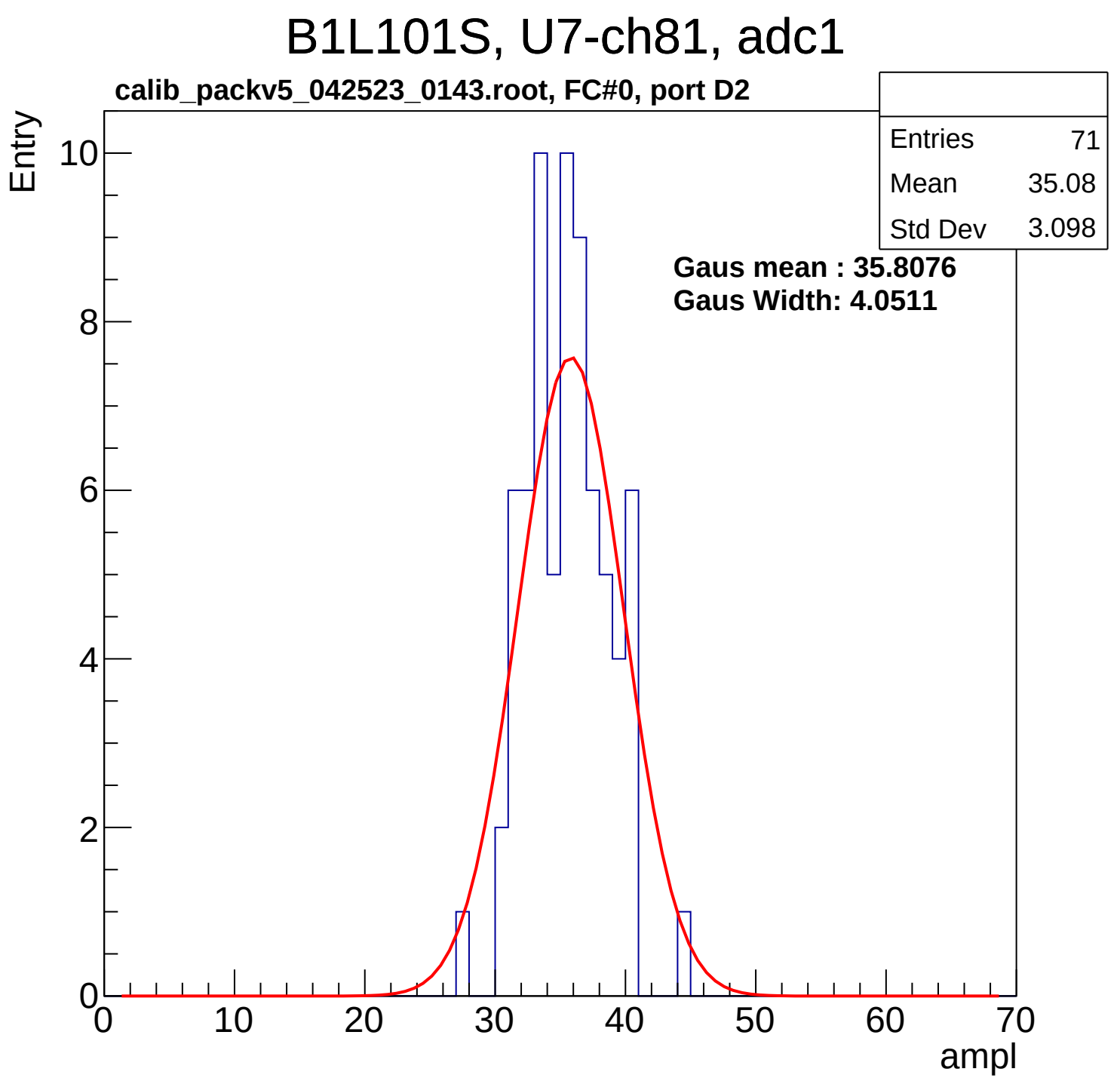
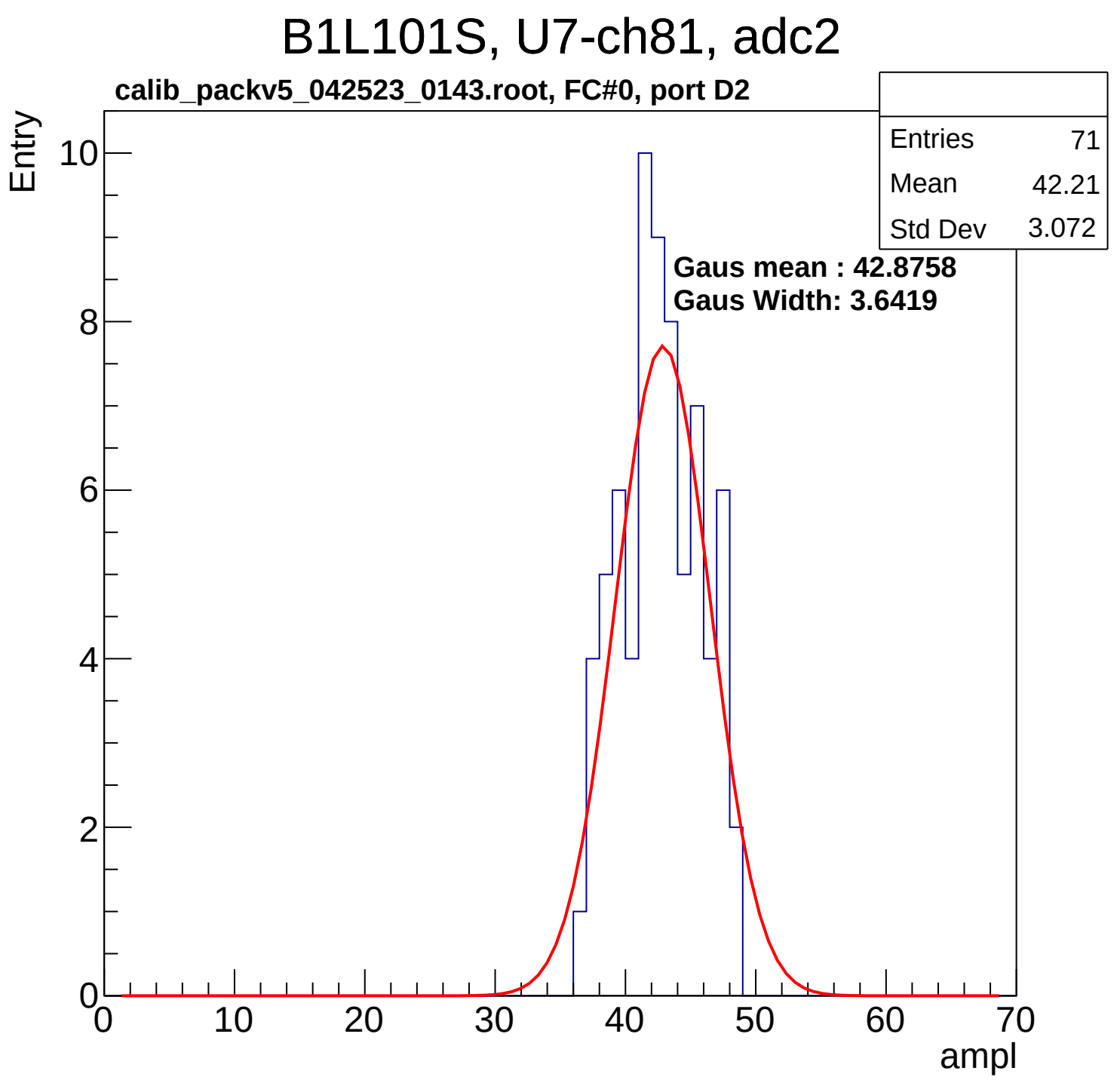
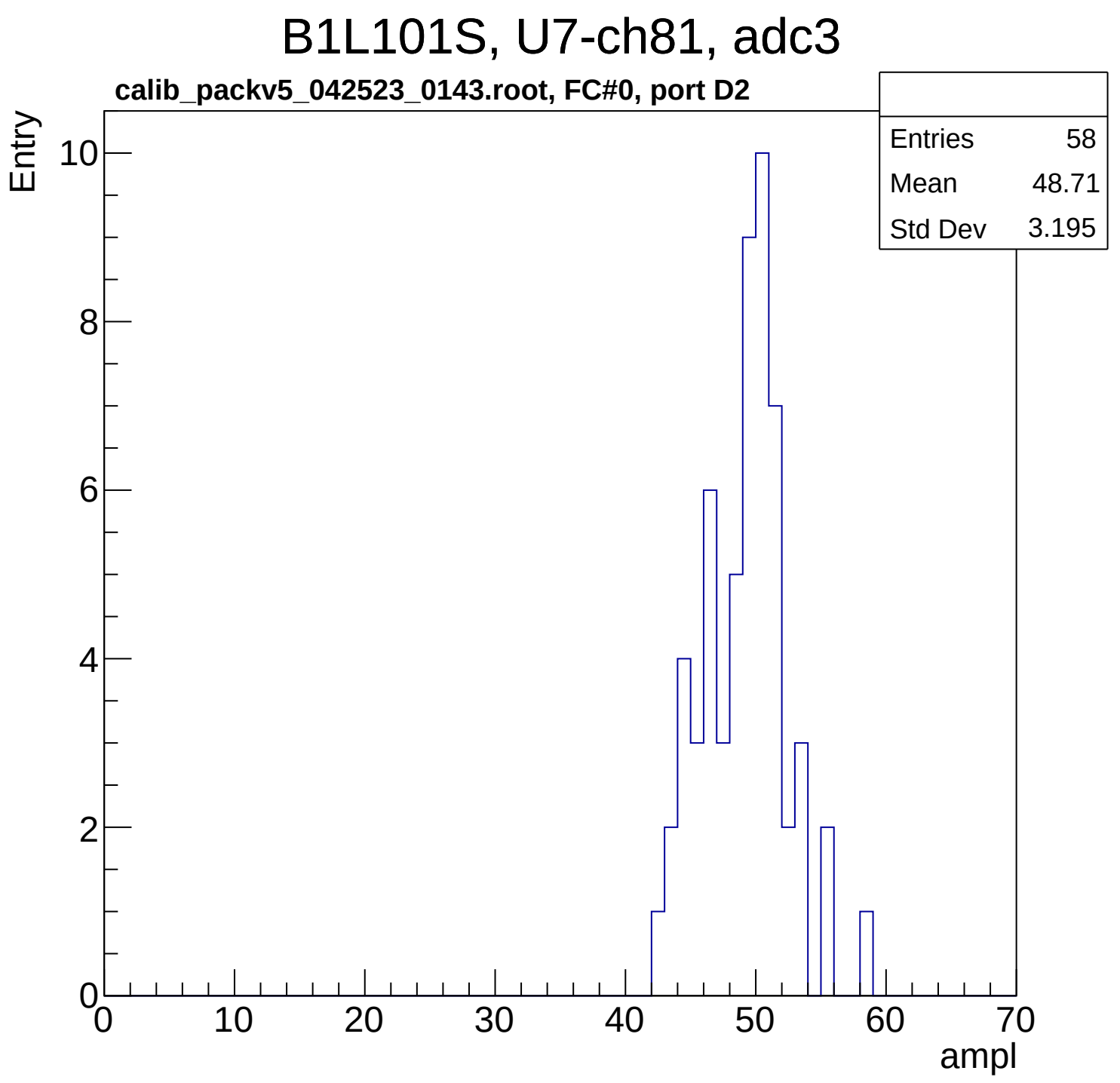

B1L101S, U7-ch80, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 18
Mean 58.11
Std Dev 14.15
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

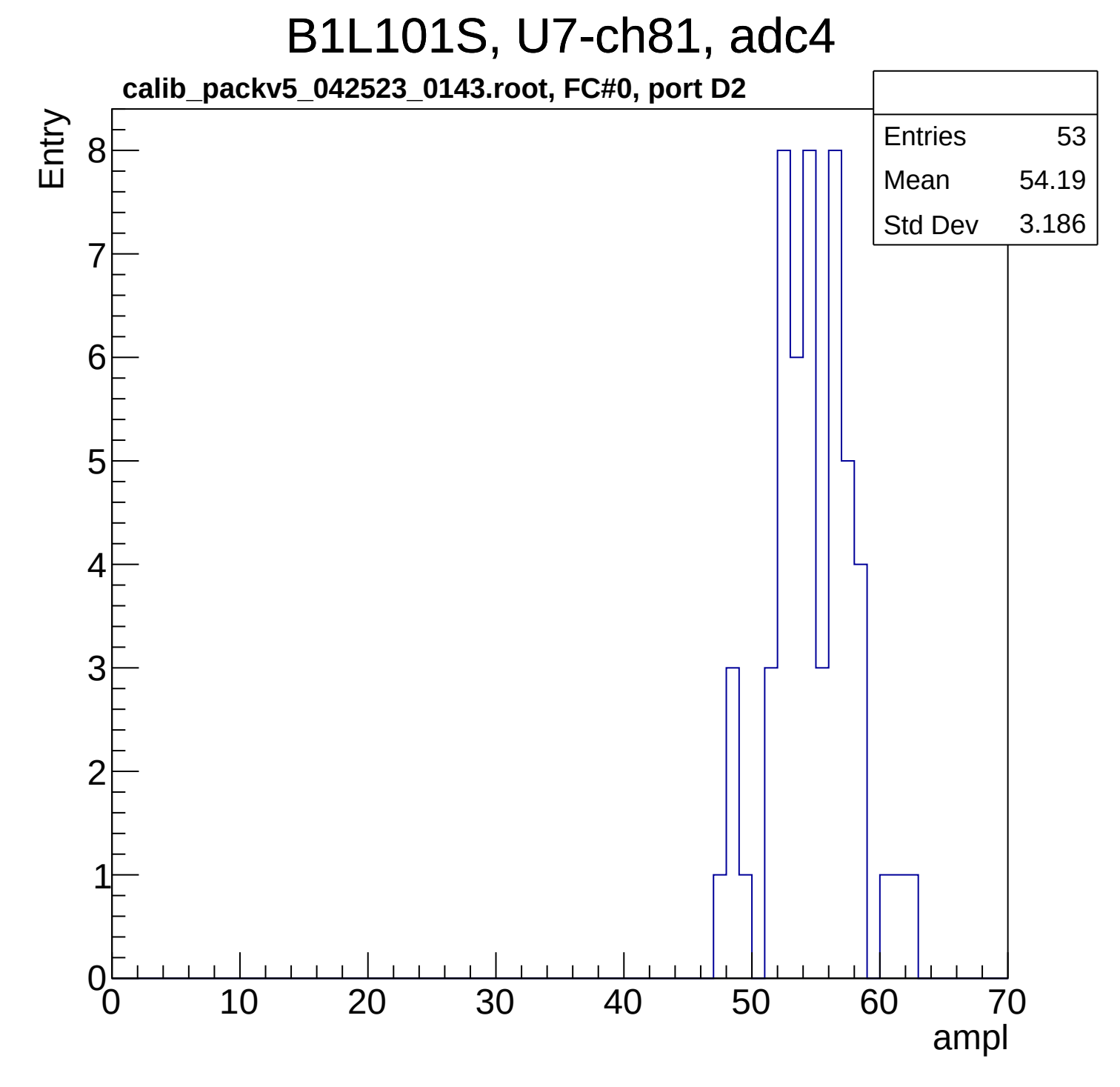

B1L101S, U7-ch80, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch81, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 27.64
Std Dev 4.825
Gaus mean : 29.9443
Gaus Width: 5.2186
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch81, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 35.08
Std Dev 3.098
Gaus mean : 35.8076
Gaus Width: 4.0511
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch81, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 42.21
Std Dev 3.072
Gaus mean : 42.8758
Gaus Width: 3.6419
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch81, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 48.71
Std Dev 3.195
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch81, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 54.19
Std Dev 3.186
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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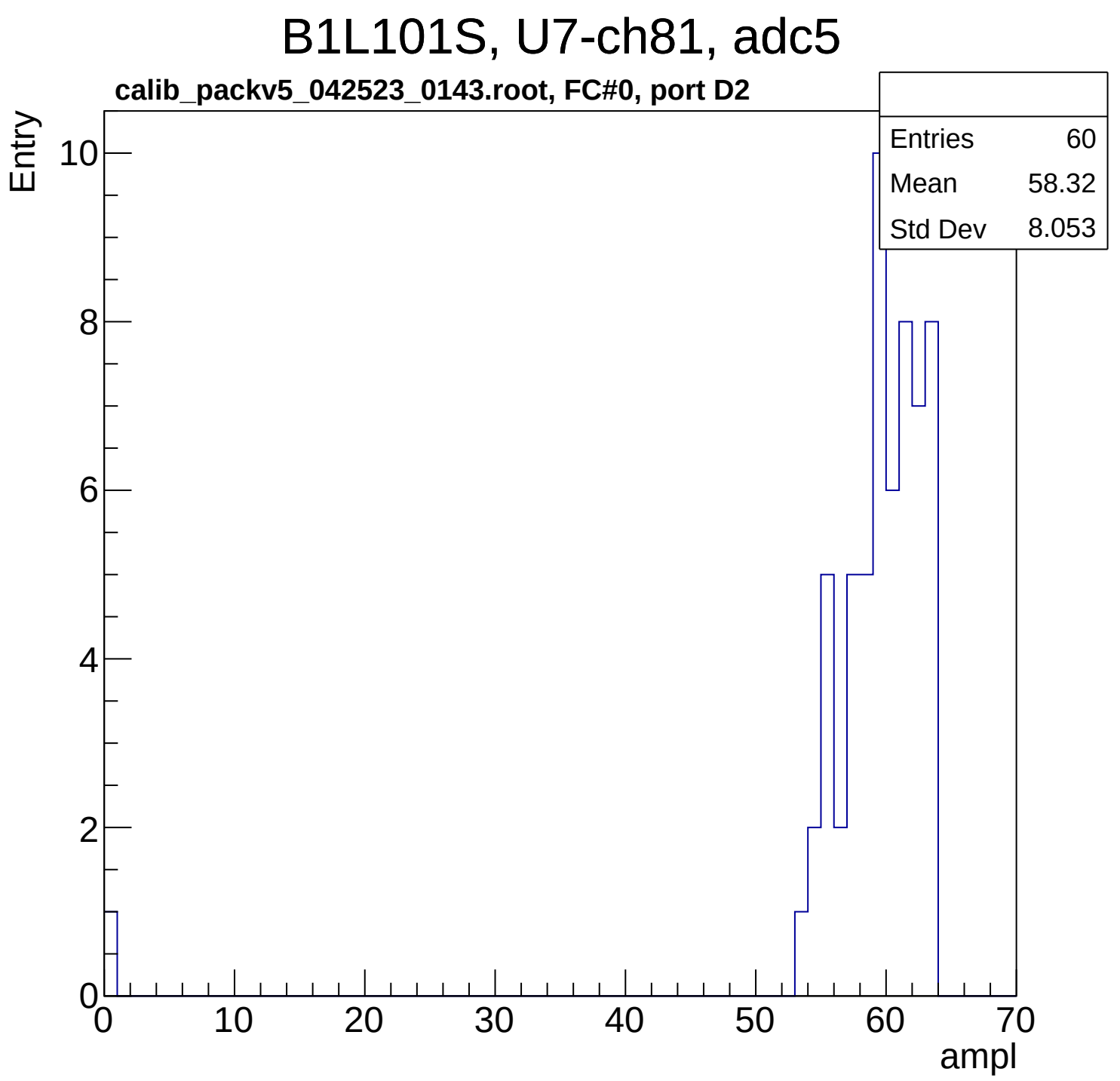
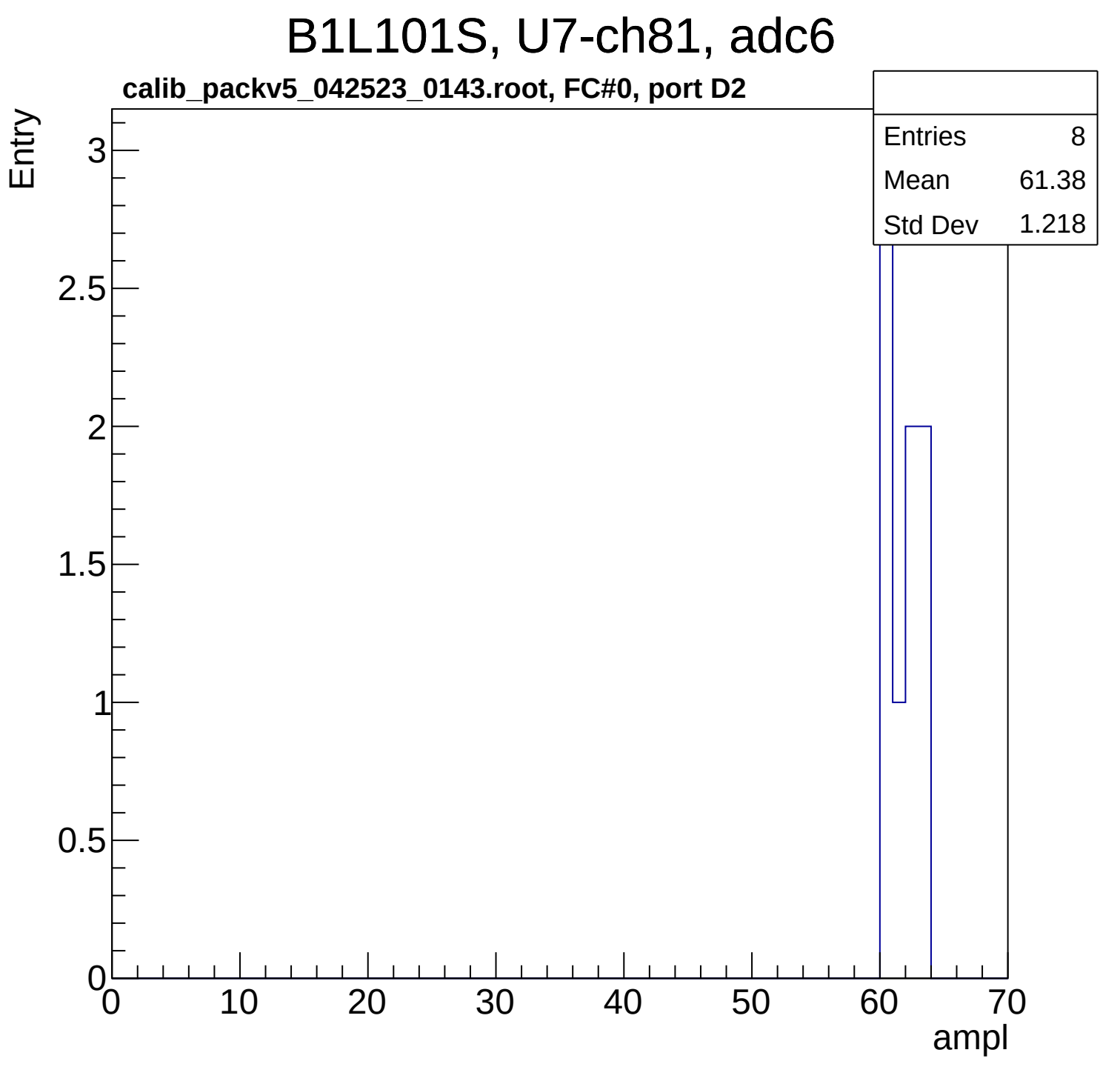
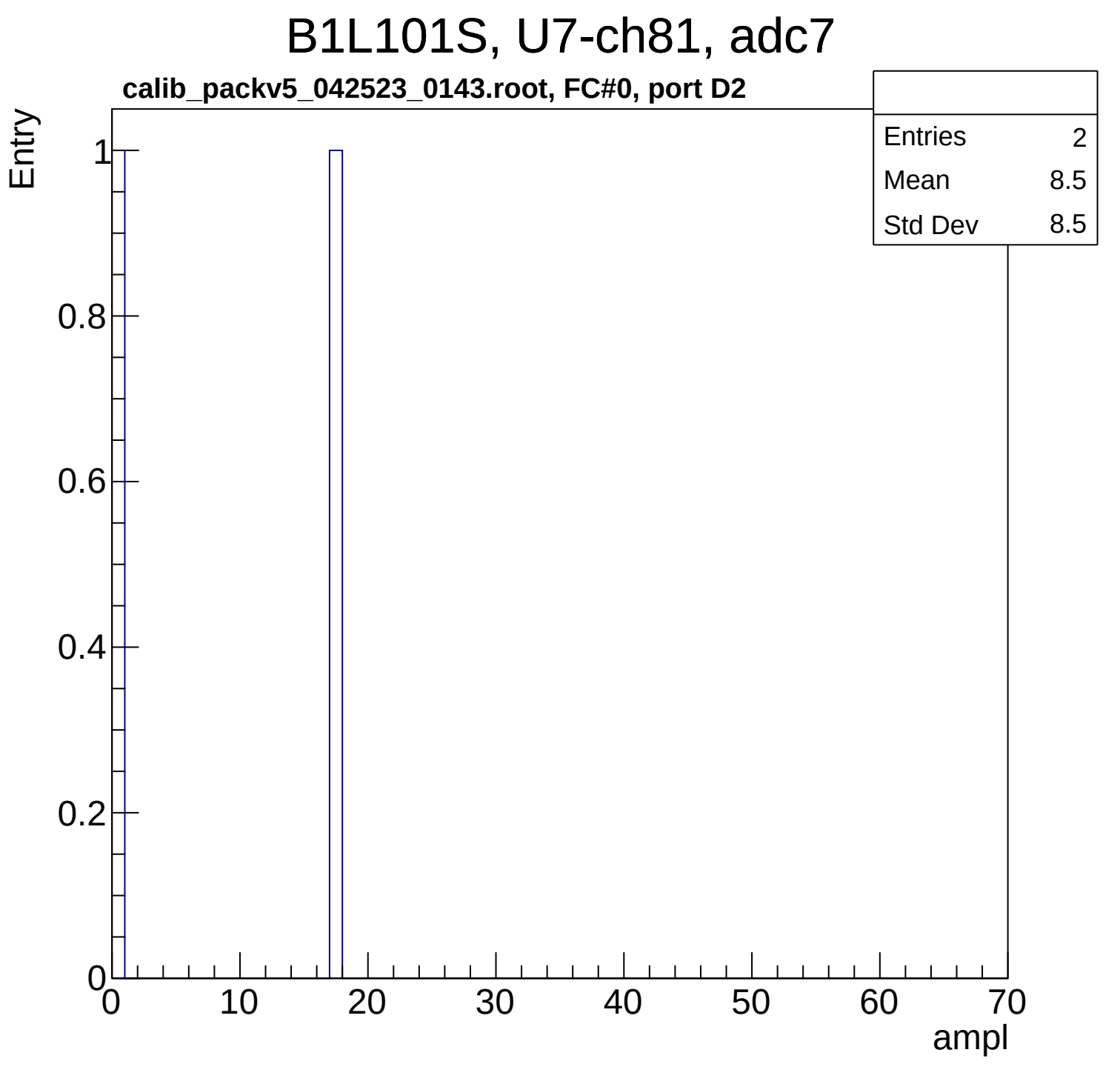
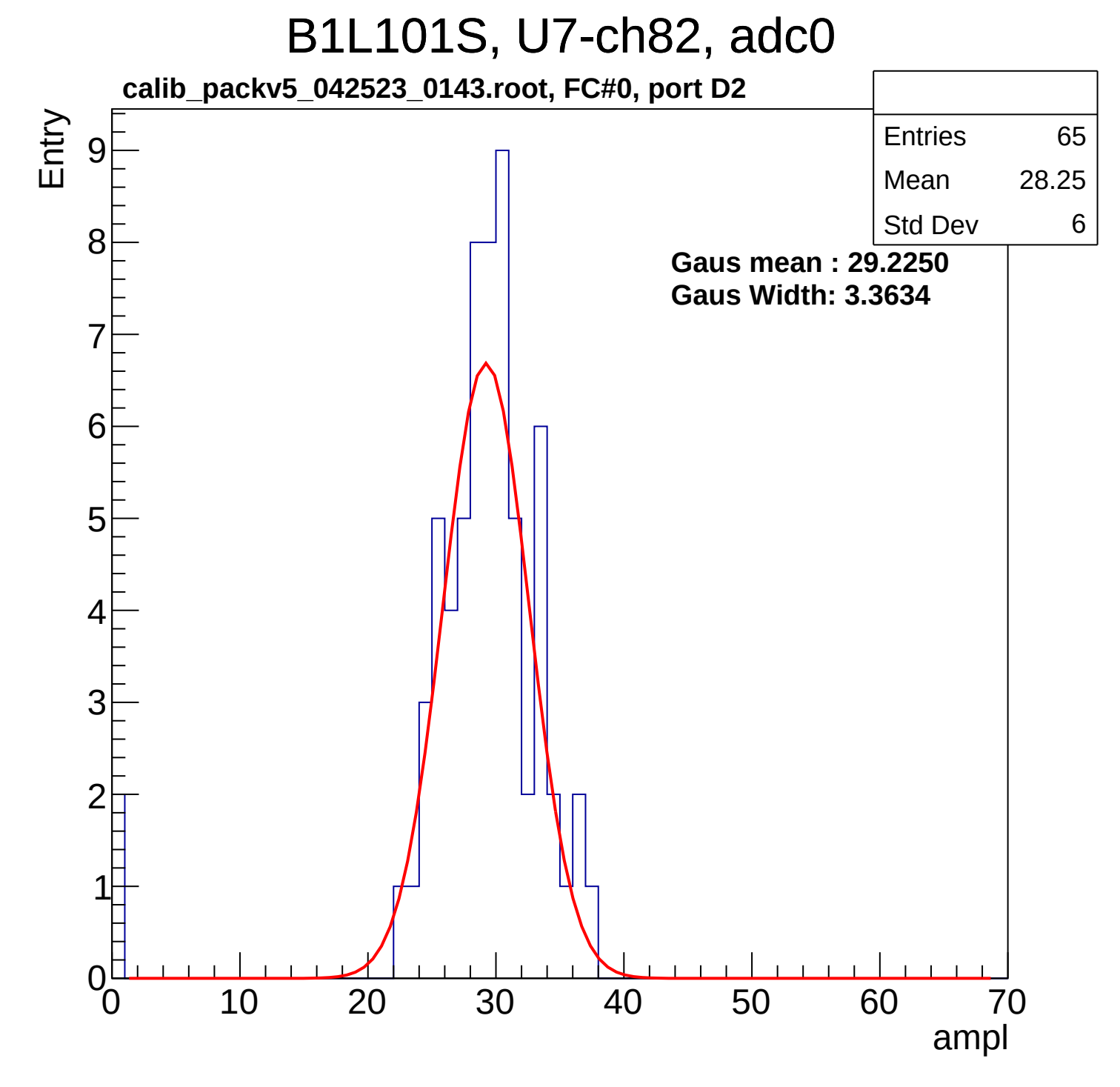
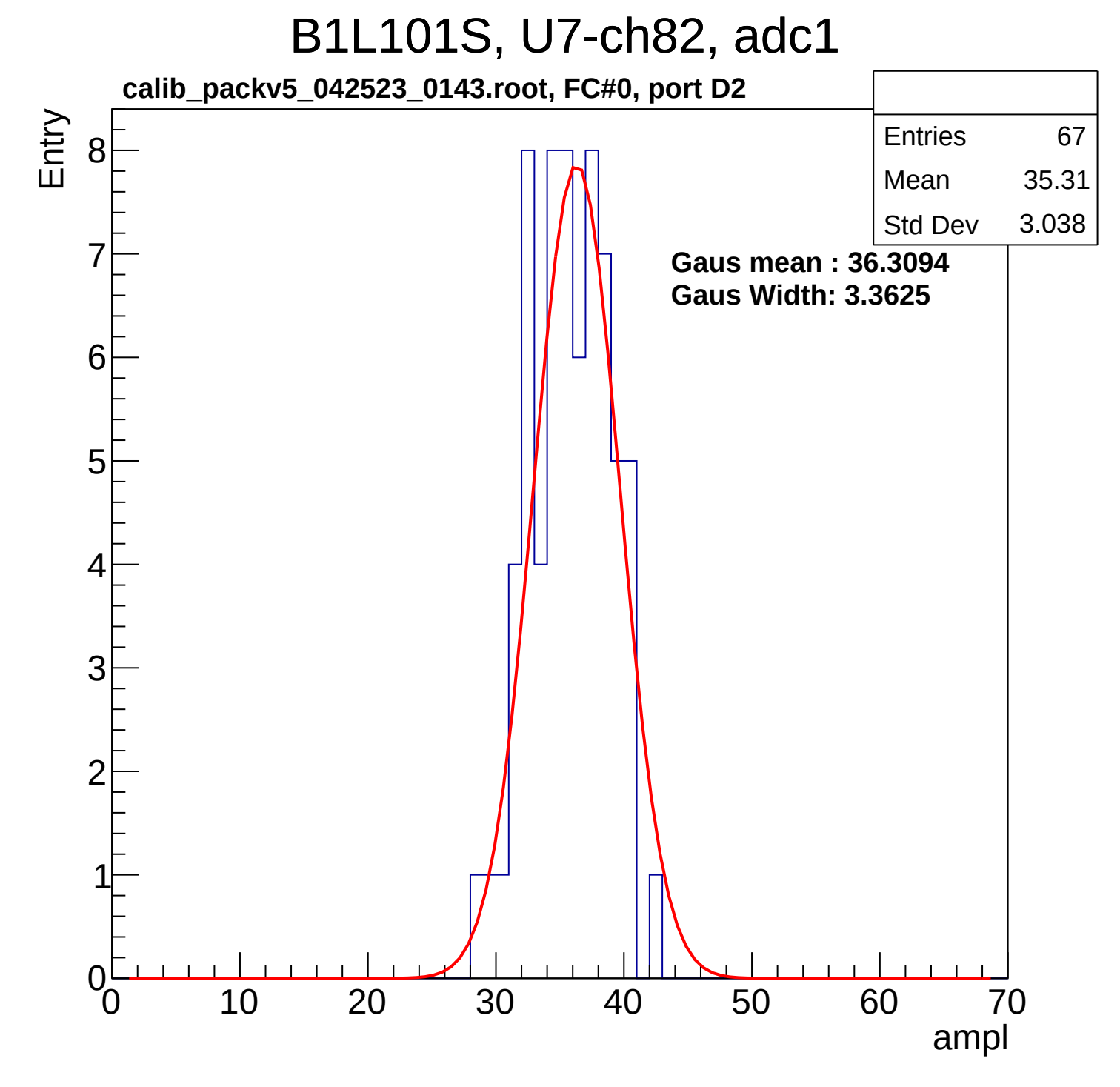
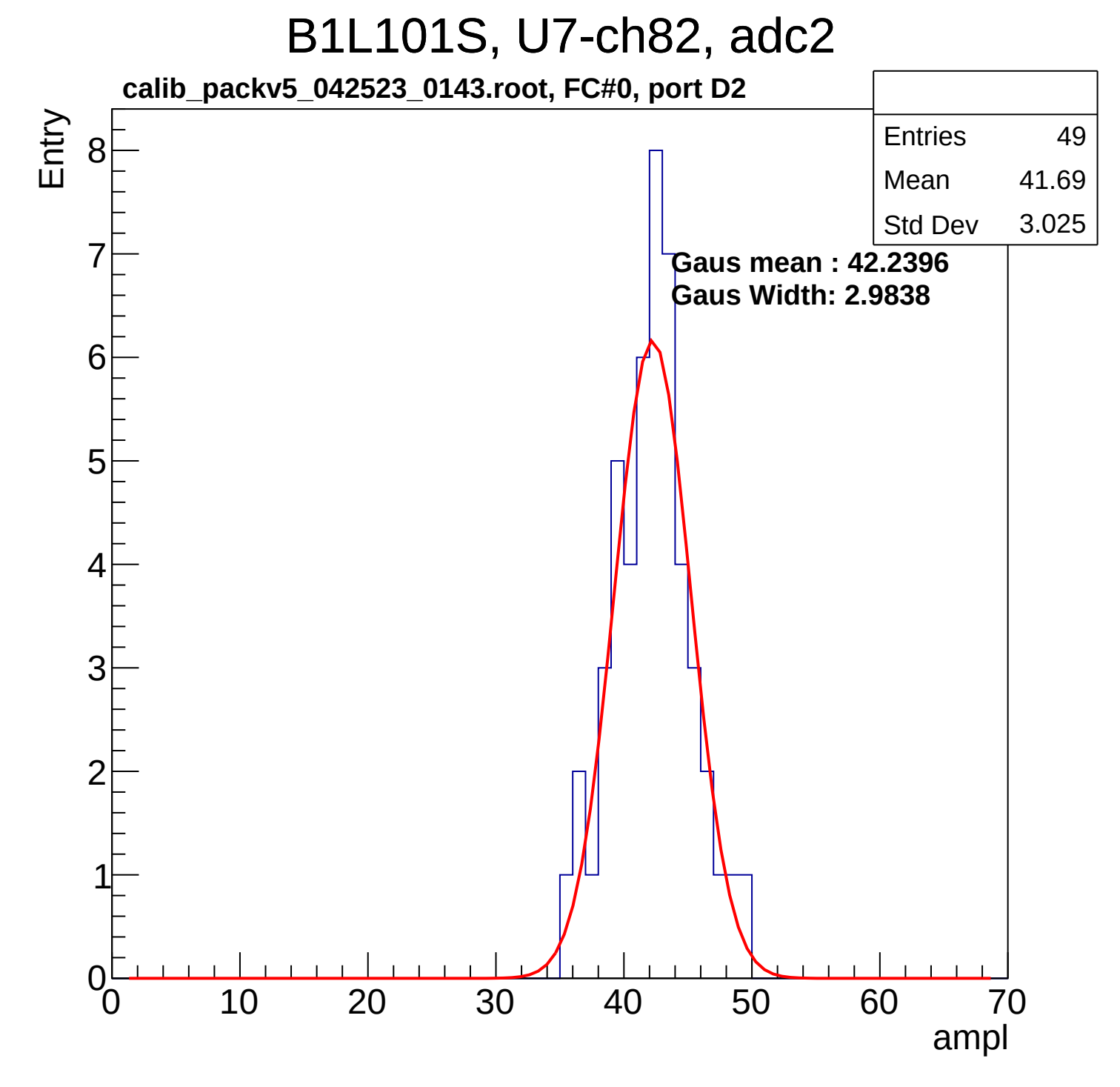

B1L101S, U7-ch81, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 58.32
Std Dev 8.053
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch81, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 61.38
Std Dev 1.218
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U7-ch81, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 8.5
Std Dev 8.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L101S, U7-ch82, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 28.25
Std Dev 6
Gaus mean : 29.2250
Gaus Width: 3.3634
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch82, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 35.31
Std Dev 3.038
Gaus mean : 36.3094
Gaus Width: 3.3625
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch82, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 41.69
Std Dev 3.025
Gaus mean : 42.2396
Gaus Width: 2.9838
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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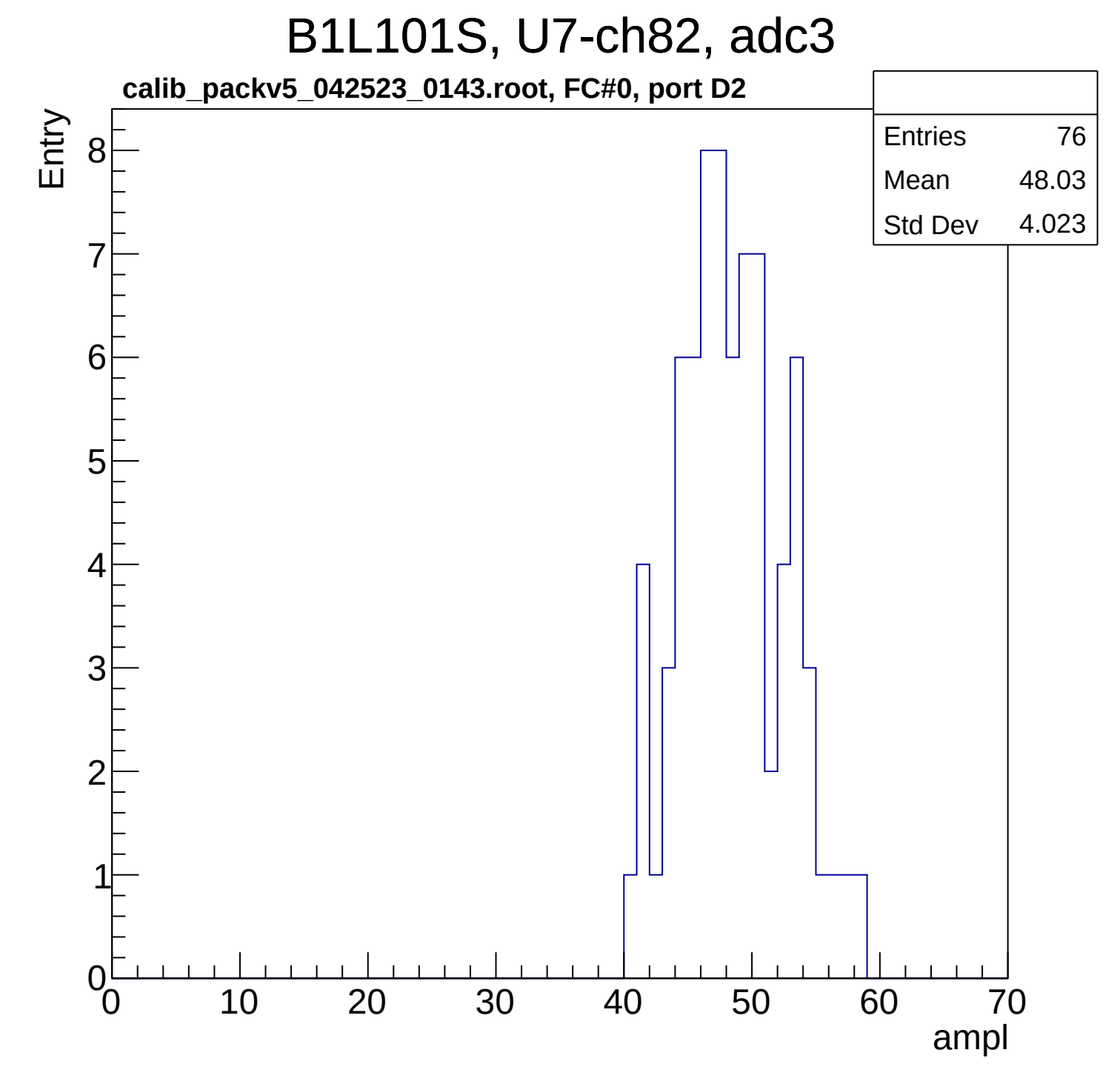
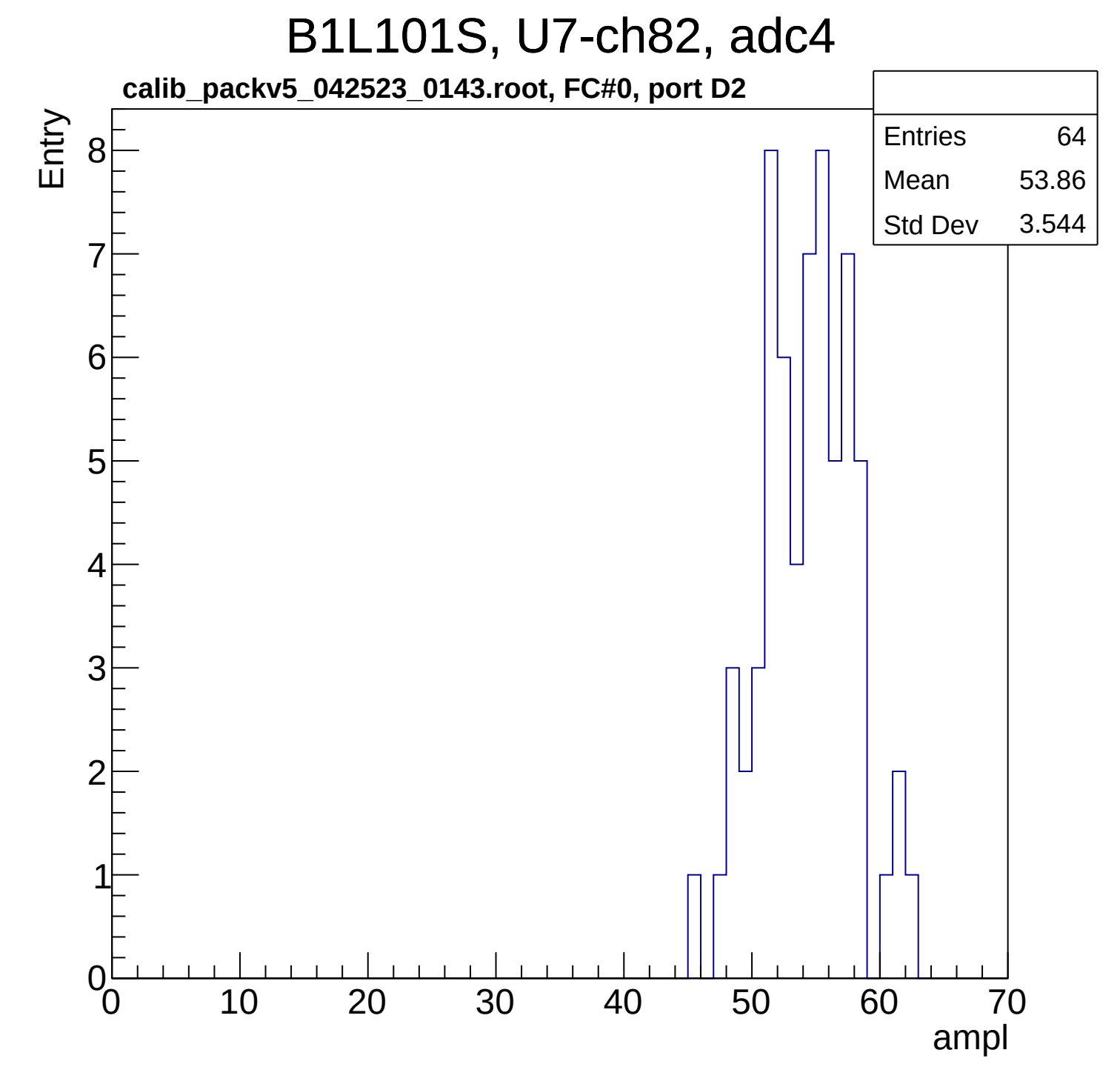
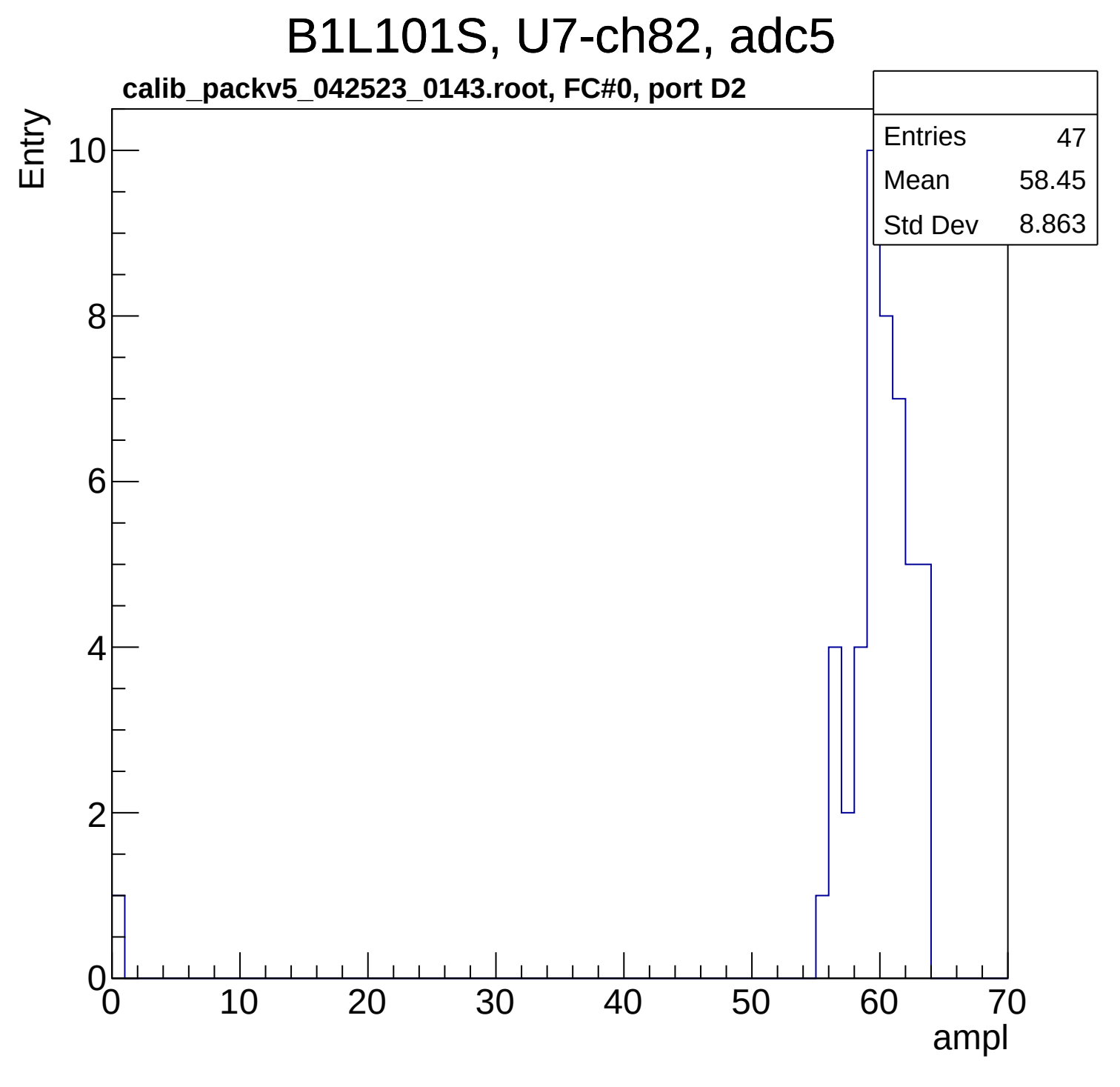
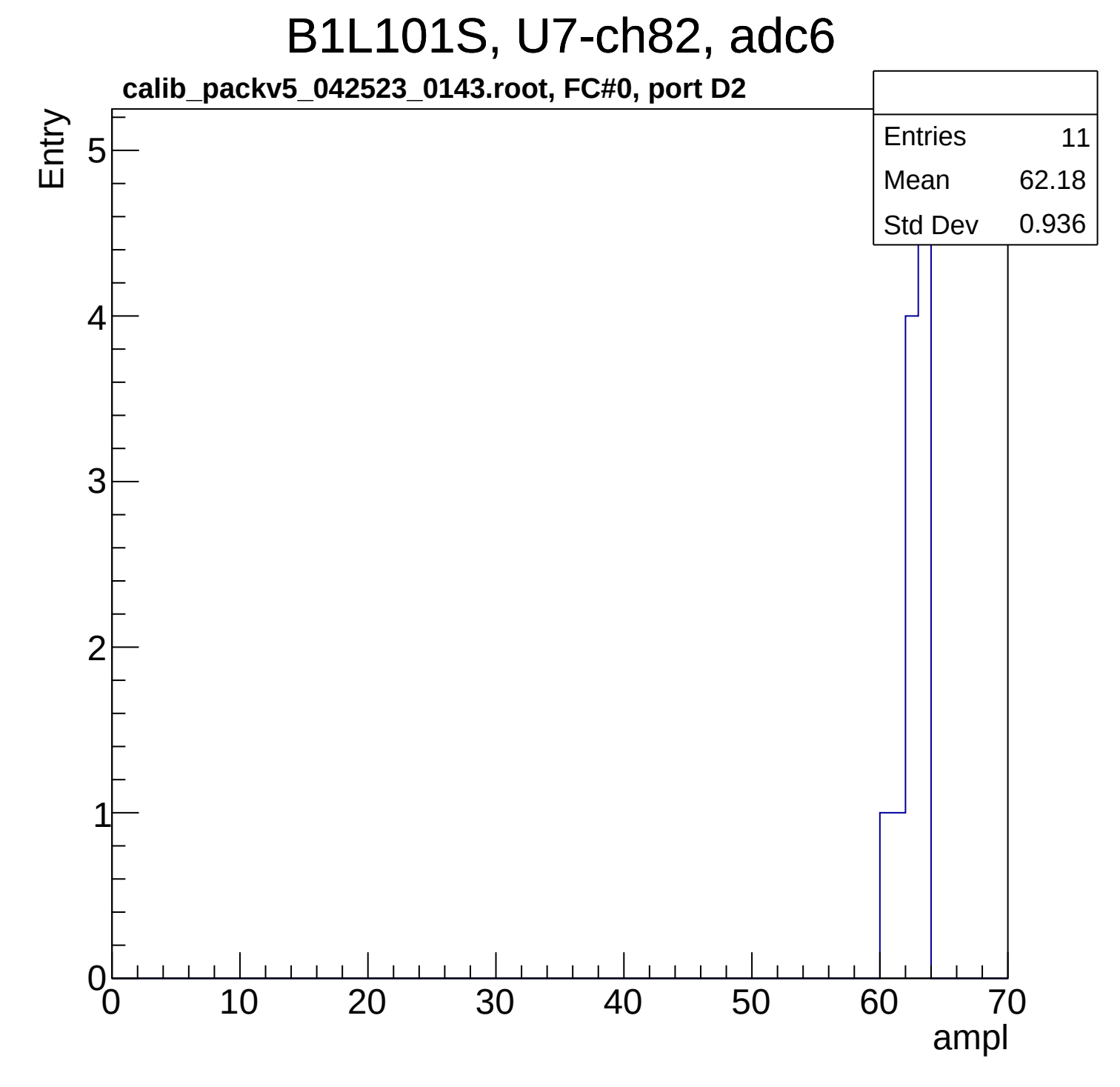
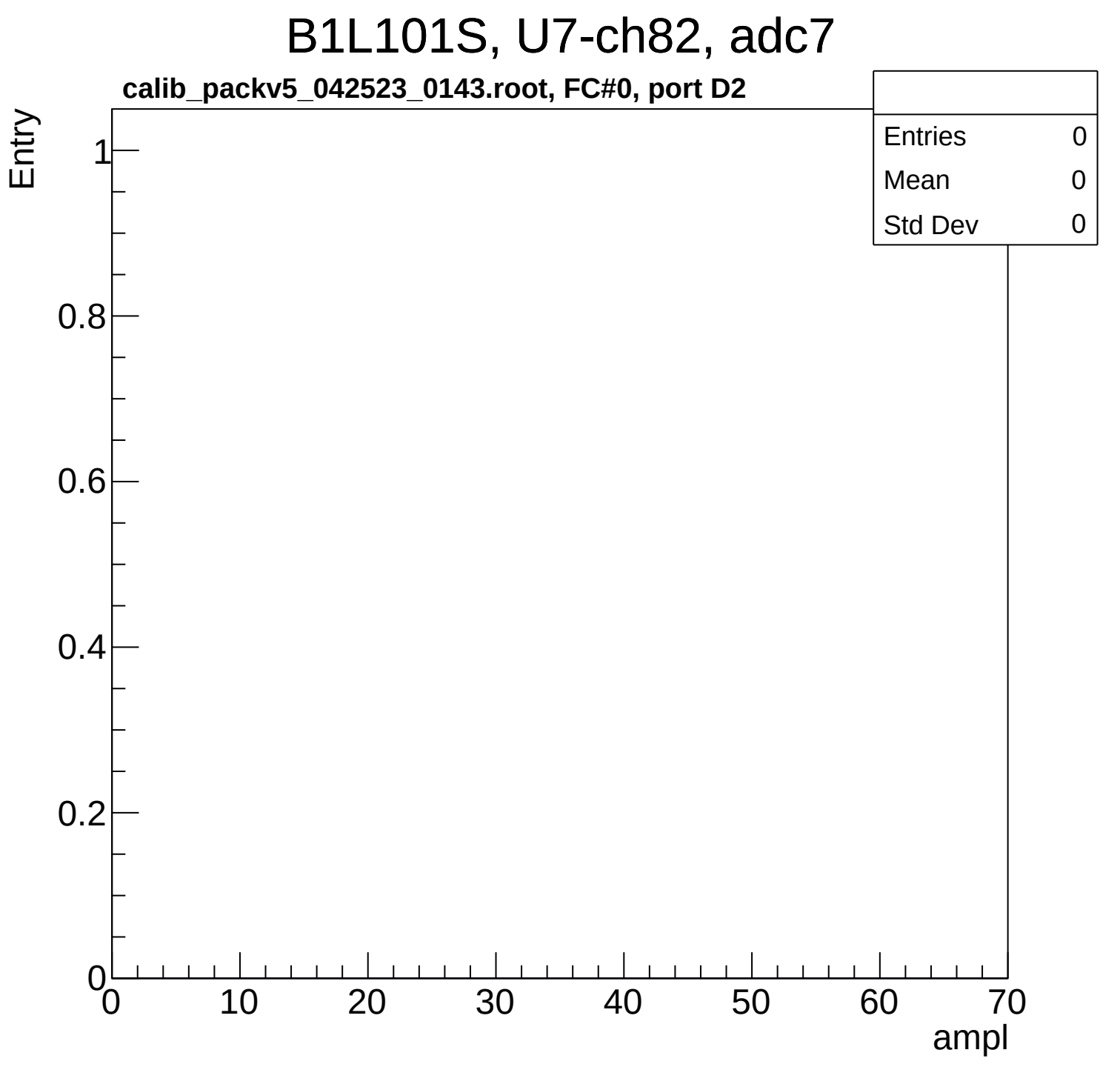
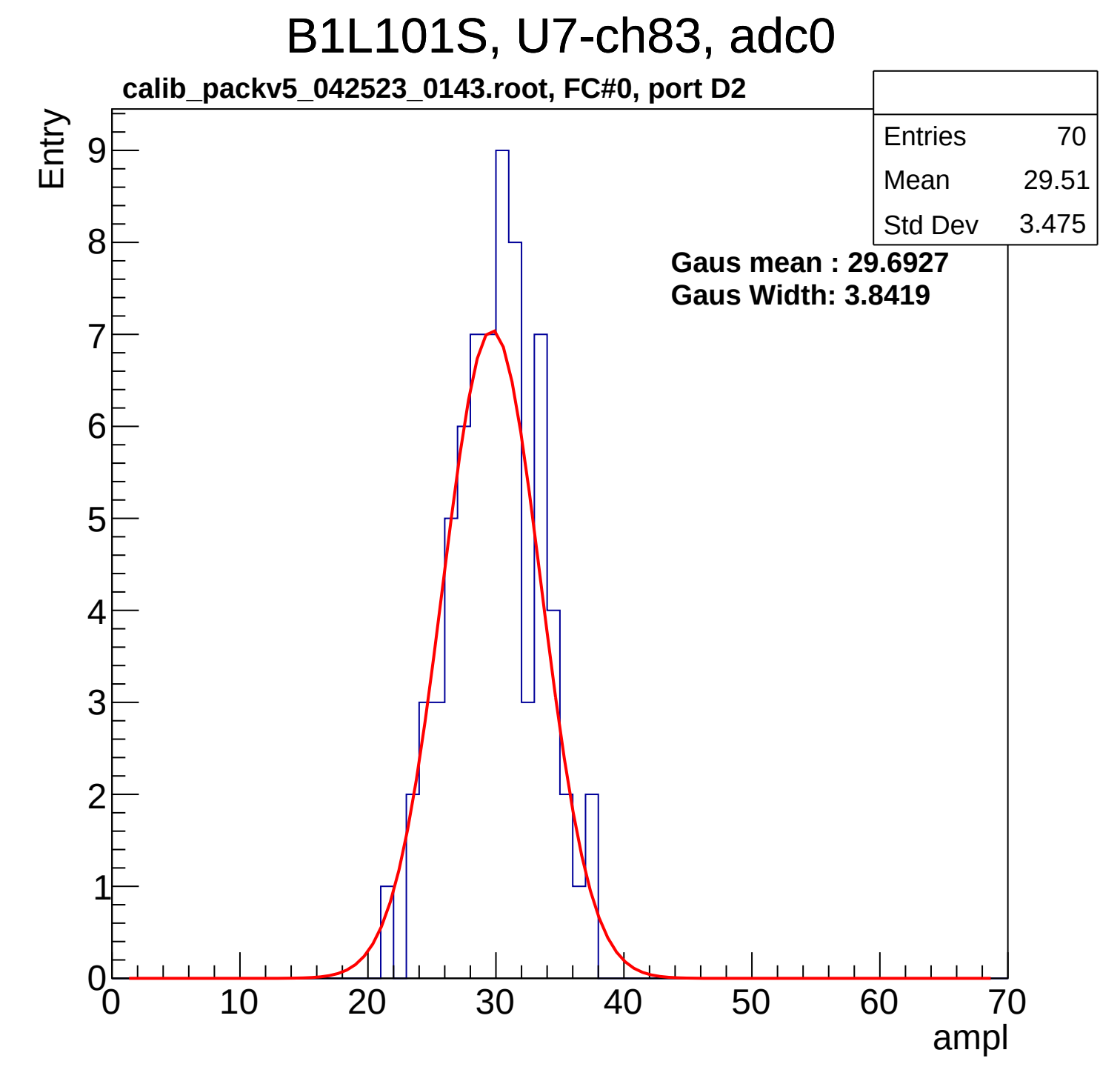

B1L101S, U7-ch82, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 48.03
Std Dev 4.023
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

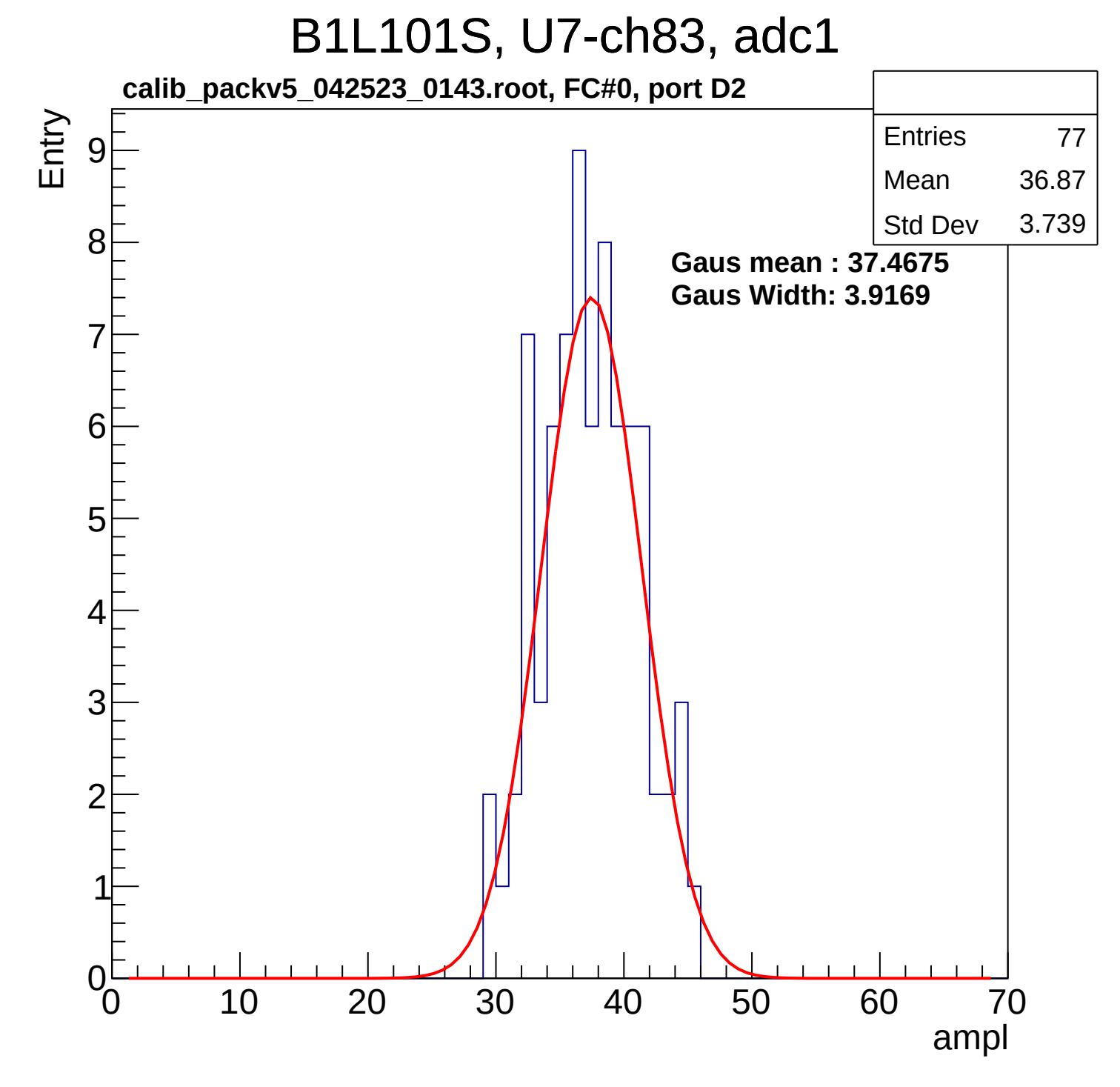

B1L101S, U7-ch82, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 53.86
Std Dev 3.544
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

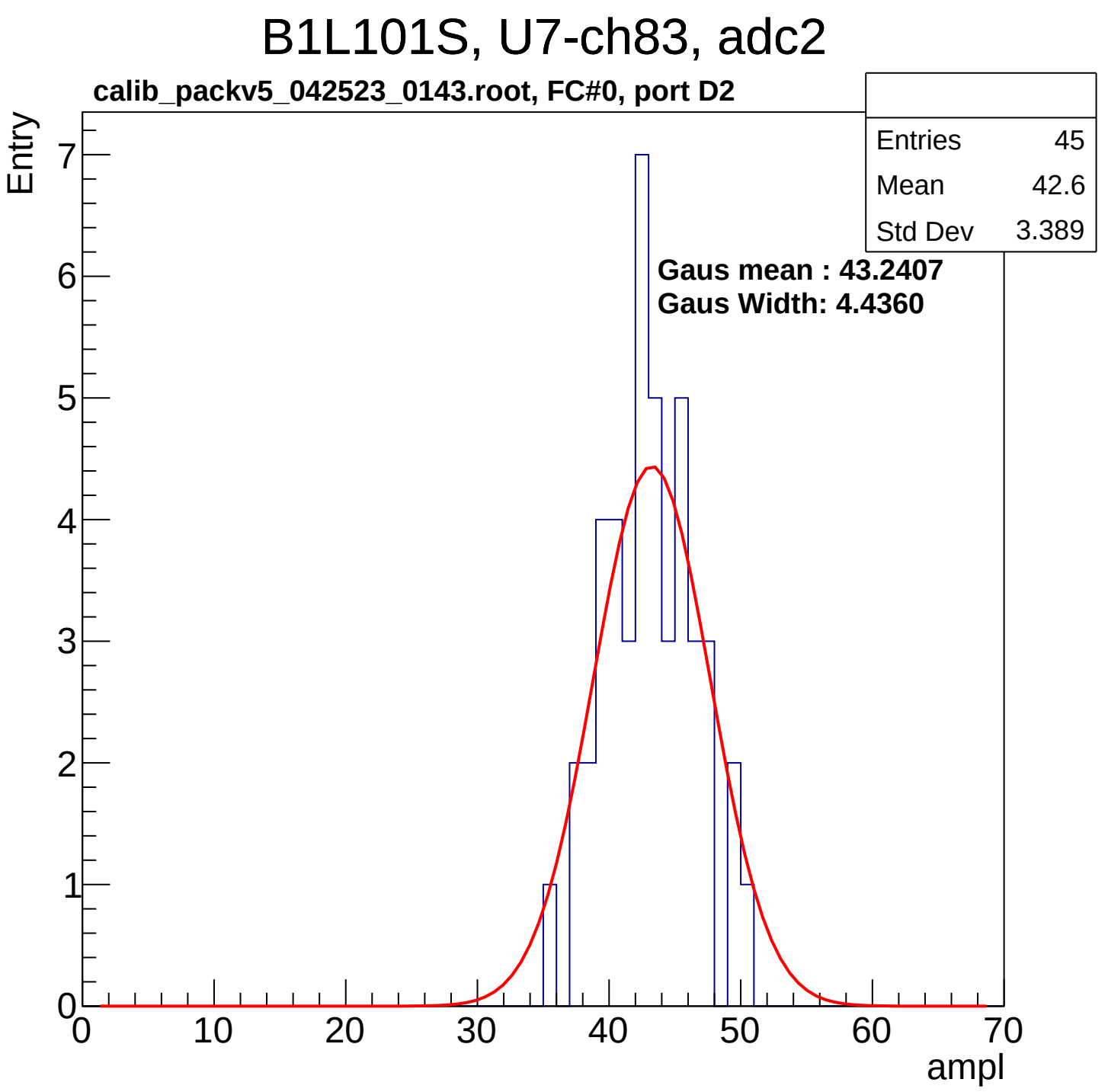

B1L101S, U7-ch82, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 58.45
Std Dev 8.863
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch82, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 11
Mean 62.18
Std Dev 0.936
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch82, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch83, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 29.51
Std Dev 3.475
Gaus mean : 29.6927
Gaus Width: 3.8419
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch83, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 36.87
Std Dev 3.739
Gaus mean : 37.4675
Gaus Width: 3.9169
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L101S, U7-ch83, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 42.6
Std Dev 3.389
Gaus mean : 43.2407
Gaus Width: 4.4360
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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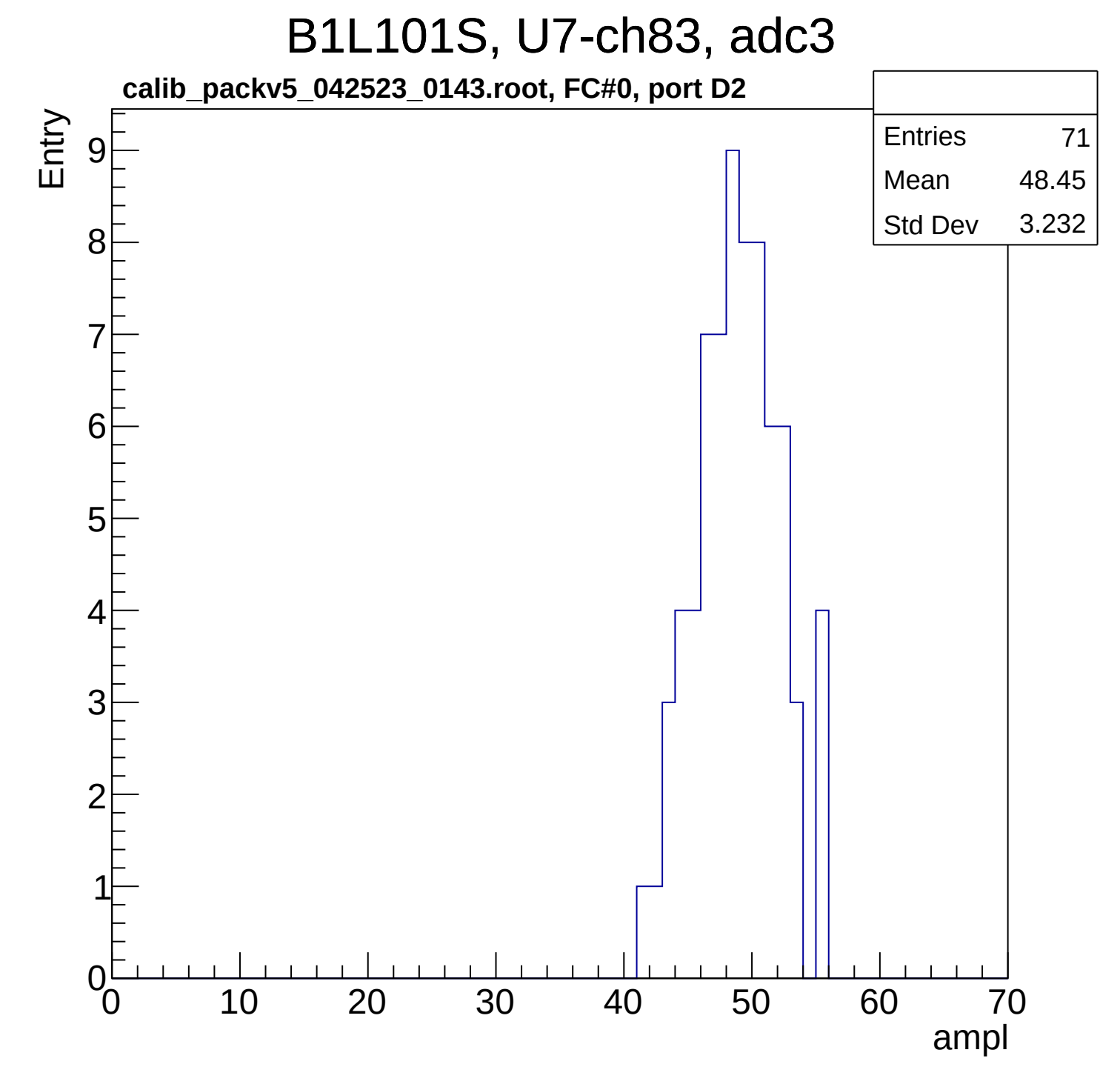
B1L101S, U7-ch83, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 48.45
Std Dev 3.232
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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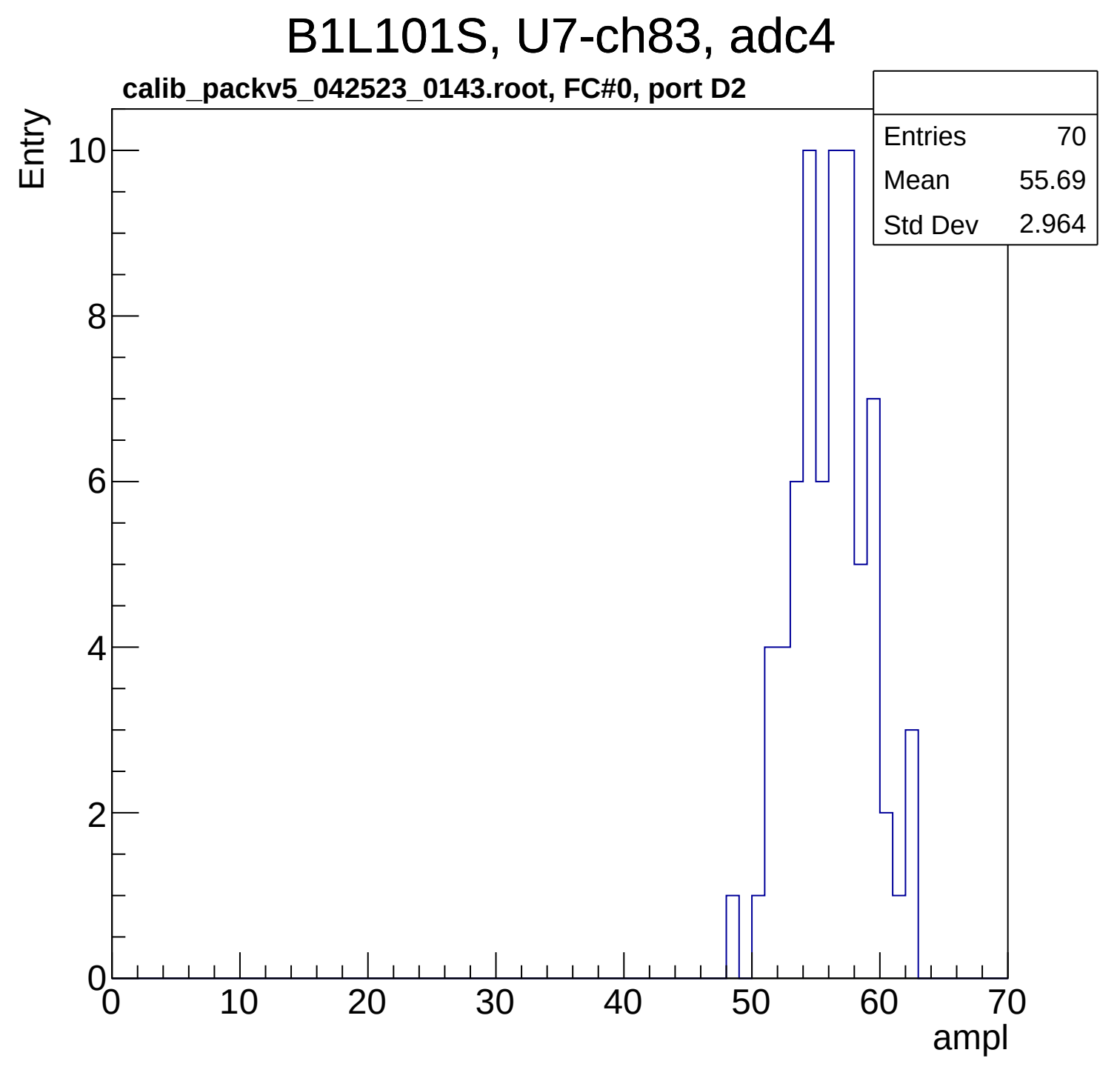
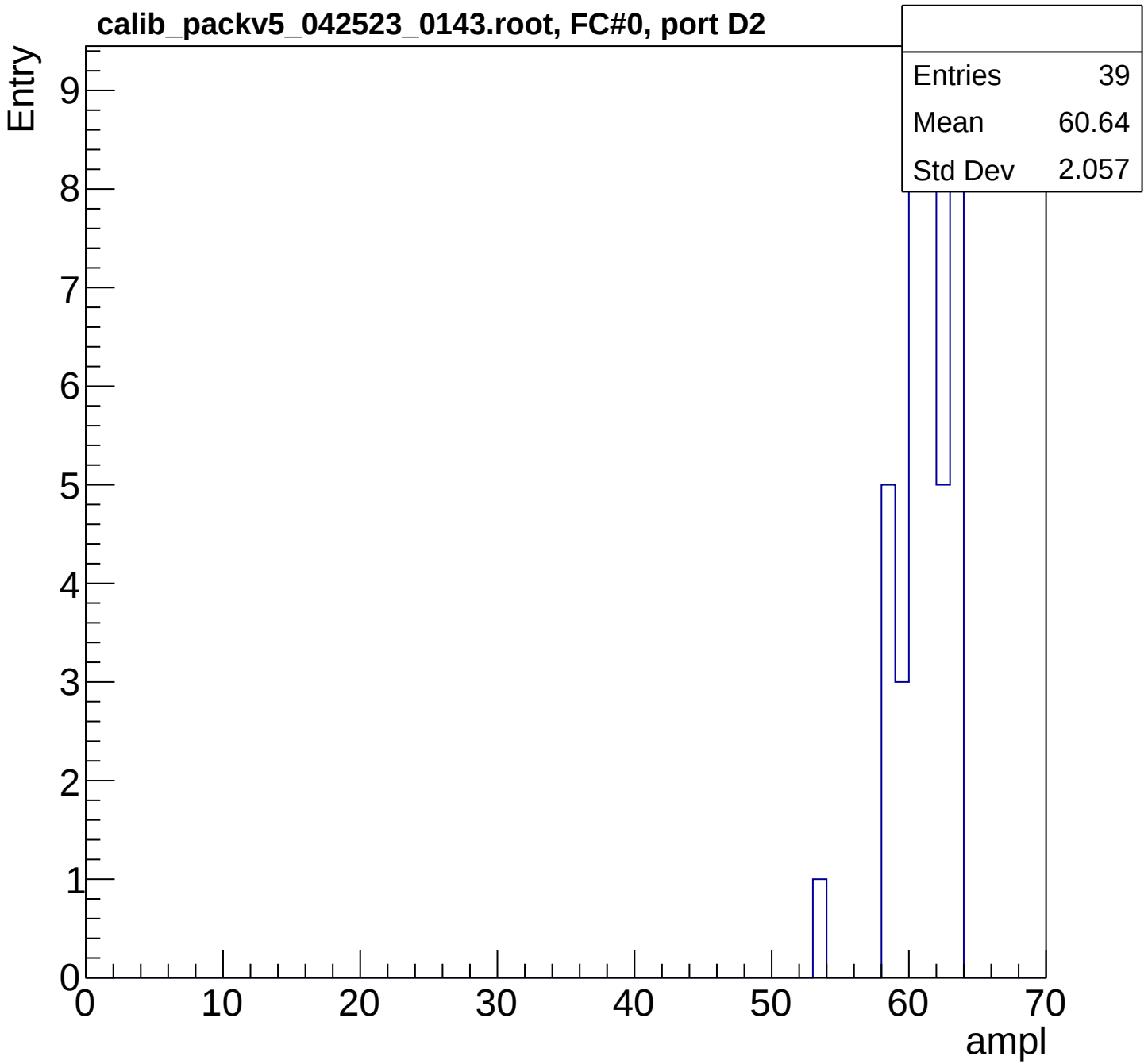

B1L101S, U7-ch83, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 55.69
Std Dev 2.964
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch83, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 39
Mean 60.64
Std Dev 2.057
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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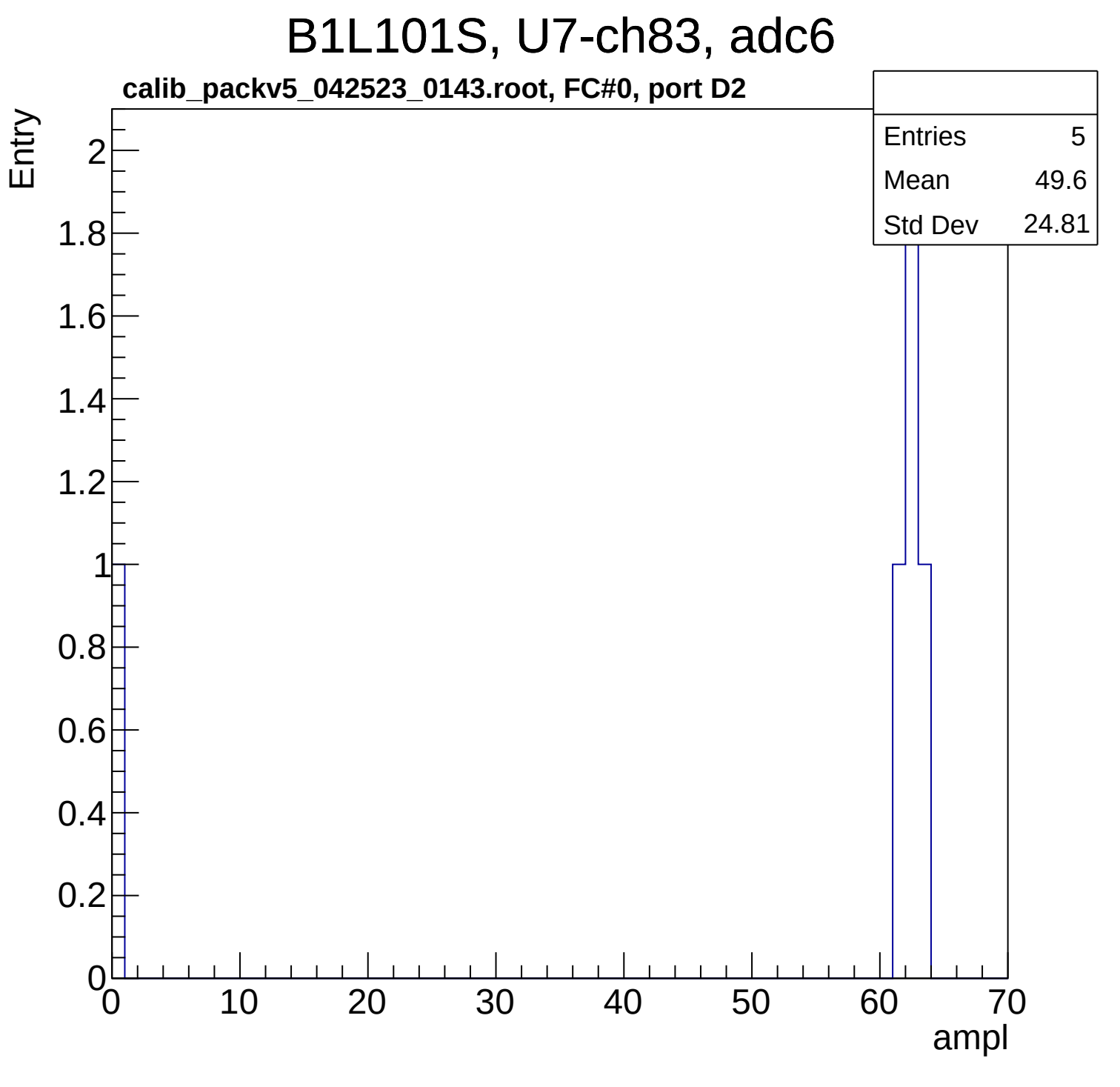
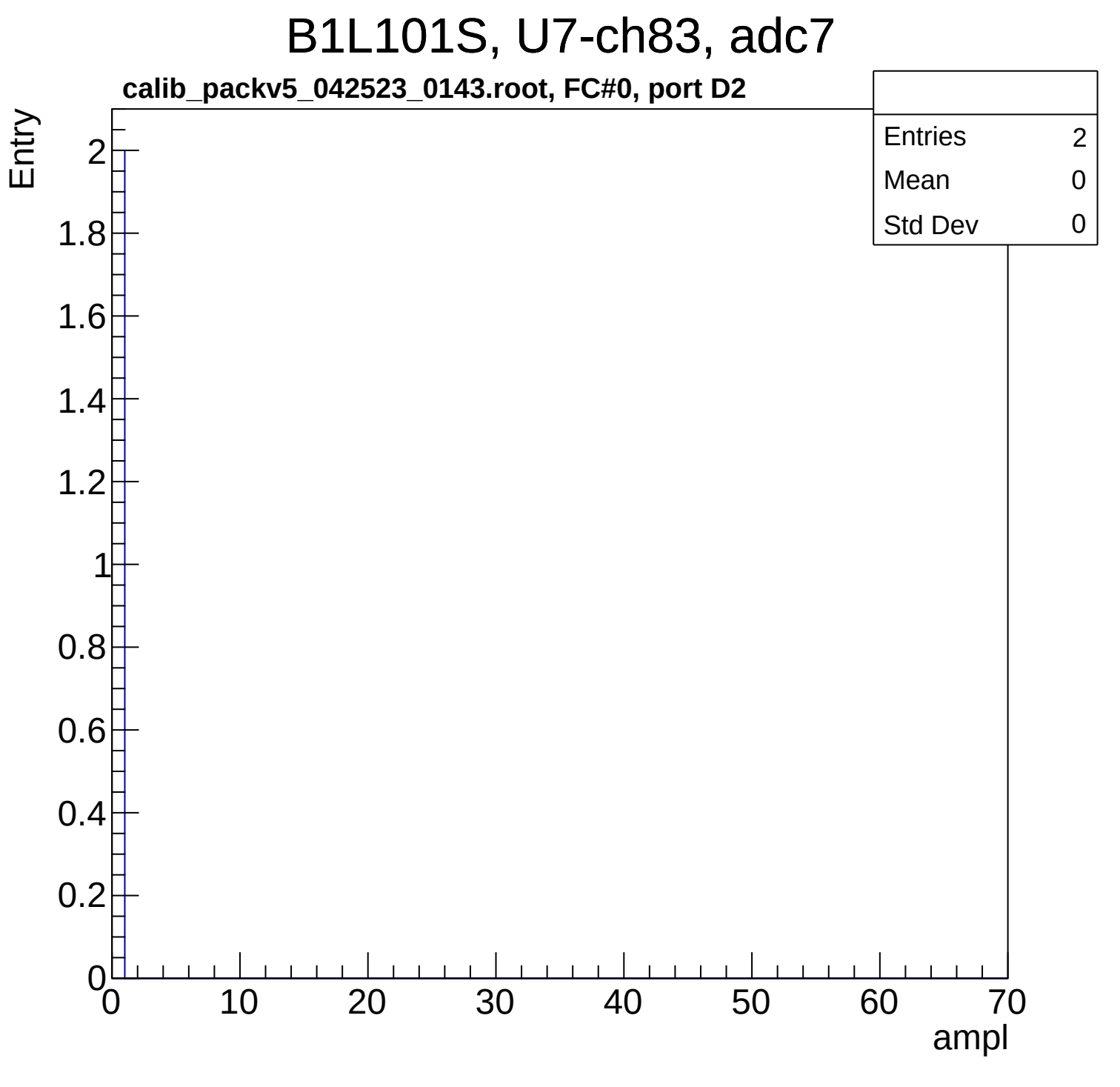
40
50
60
70


B1L101S, U7-ch83, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 49.6
Std Dev 24.81
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U7-ch83, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
50
60
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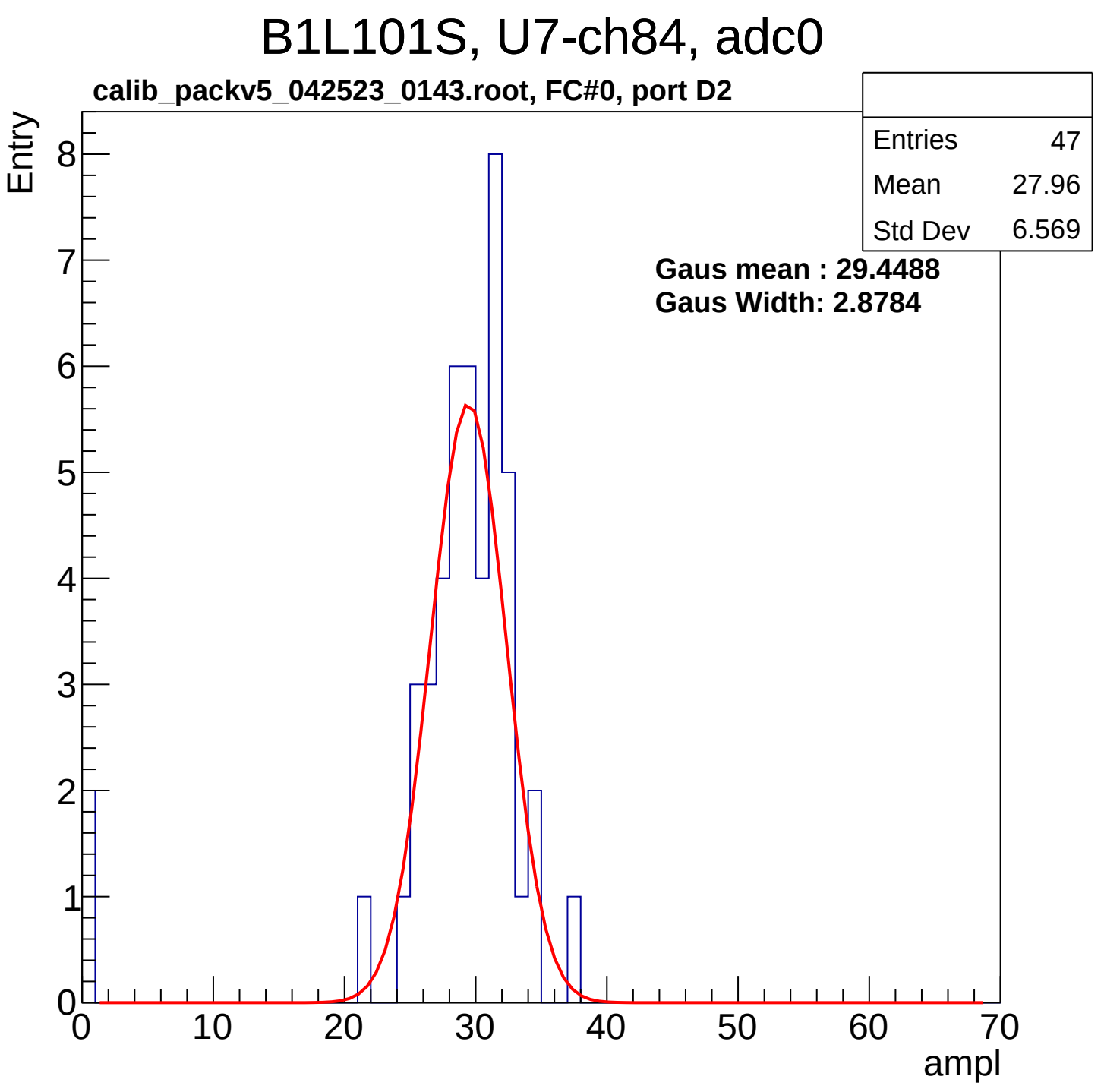
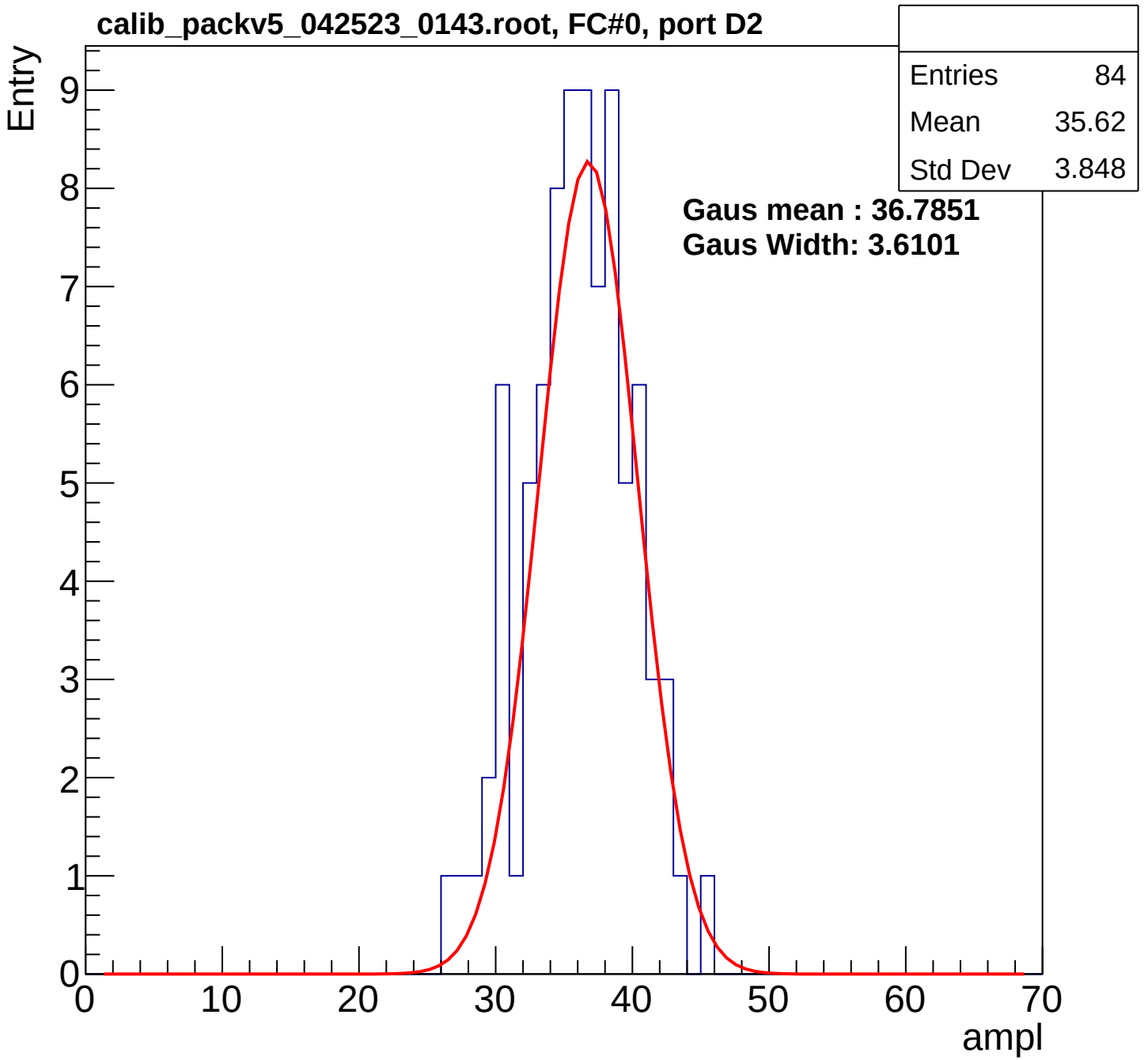
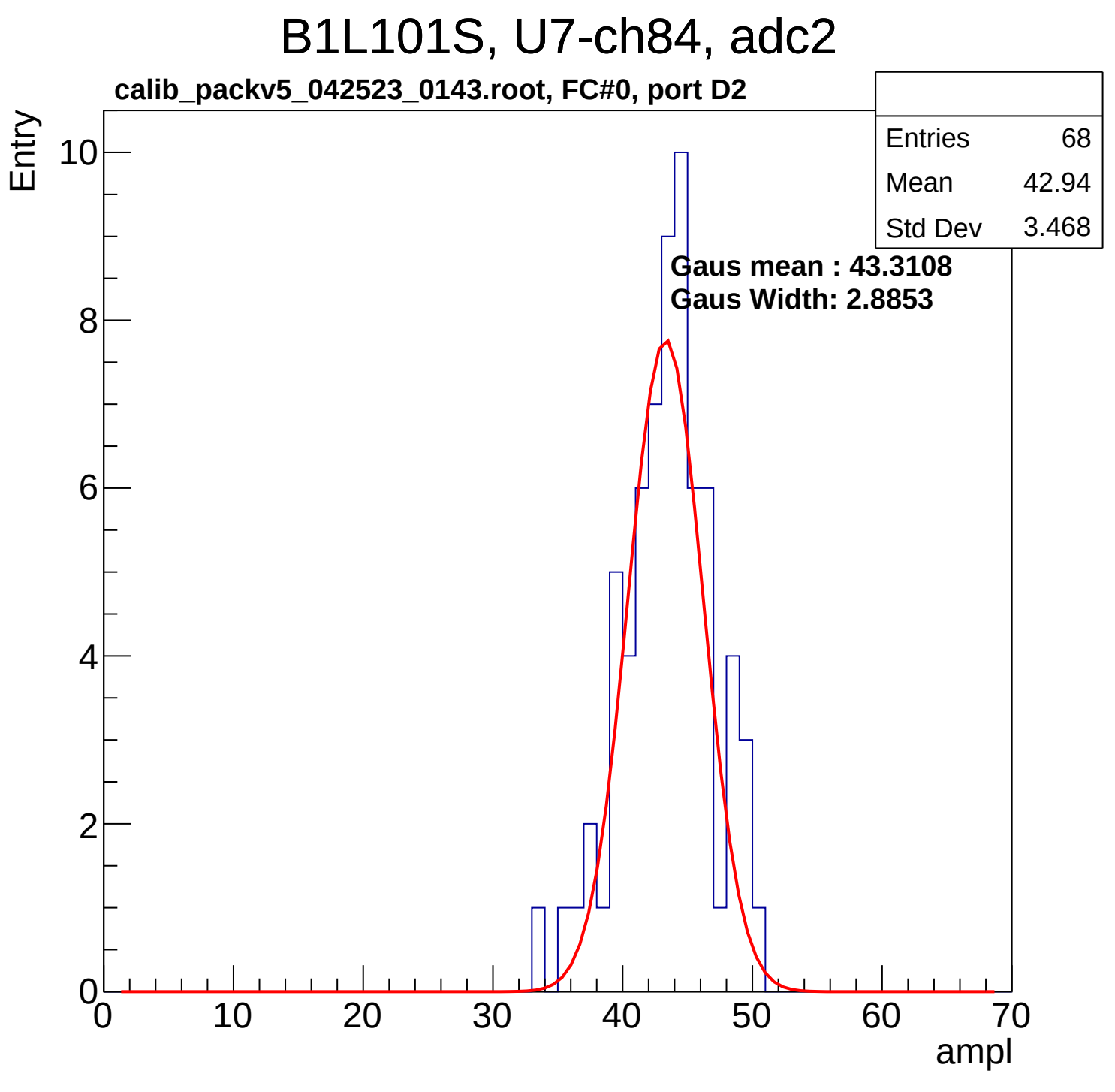
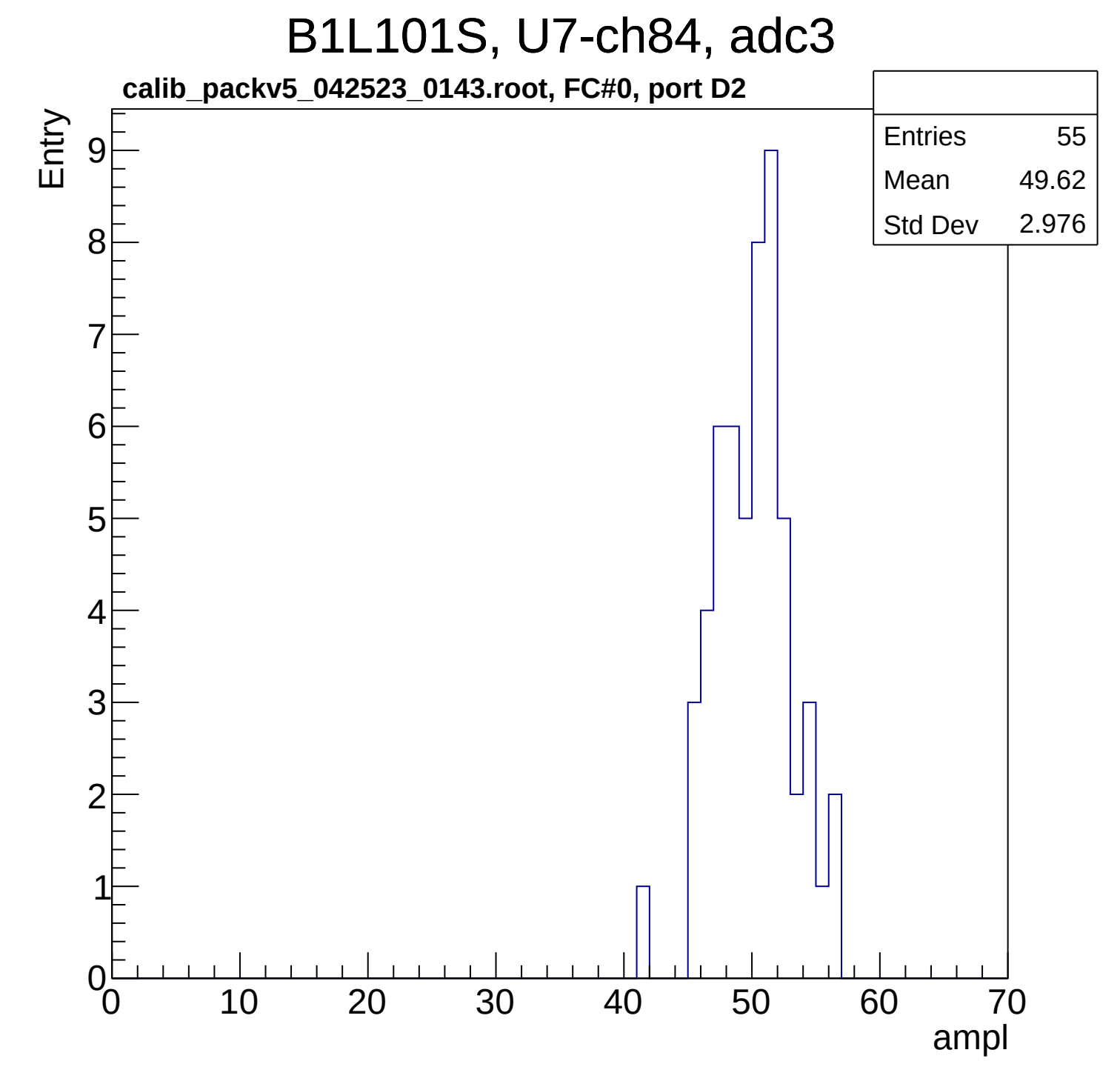

B1L101S, U7-ch84, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 27.96
Std Dev 6.569
Gaus mean : 29.4488
Gaus Width: 2.8784
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch84, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 84
Mean 35.62
Std Dev 3.848
Gaus mean : 36.7851
Gaus Width: 3.6101
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch84, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 42.94
Std Dev 3.468
Gaus mean : 43.3108
Gaus Width: 2.8853
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch84, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 49.62
Std Dev 2.976
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
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40
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60
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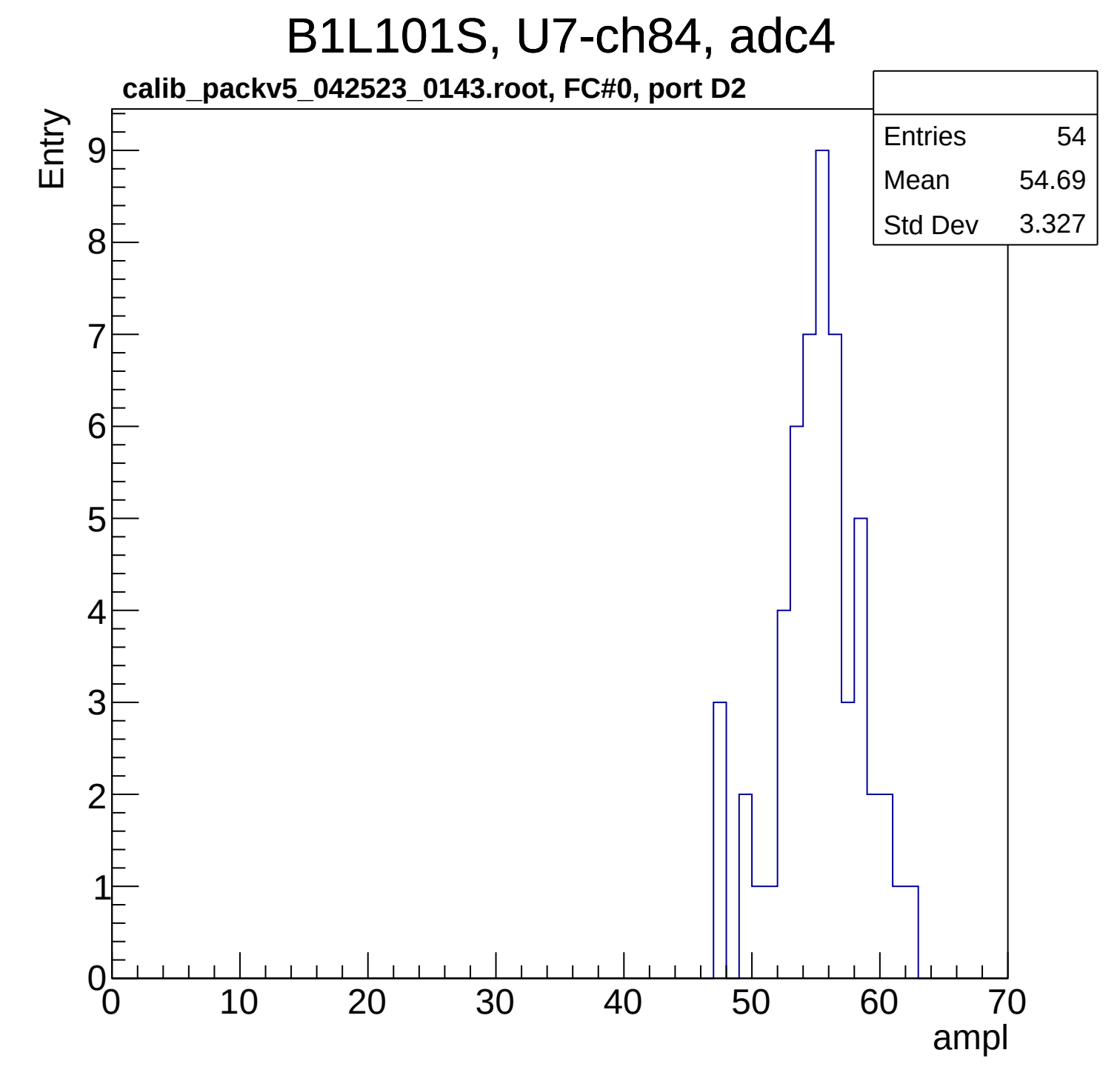
B1L101S, U7-ch84, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 54.69
Std Dev 3.327
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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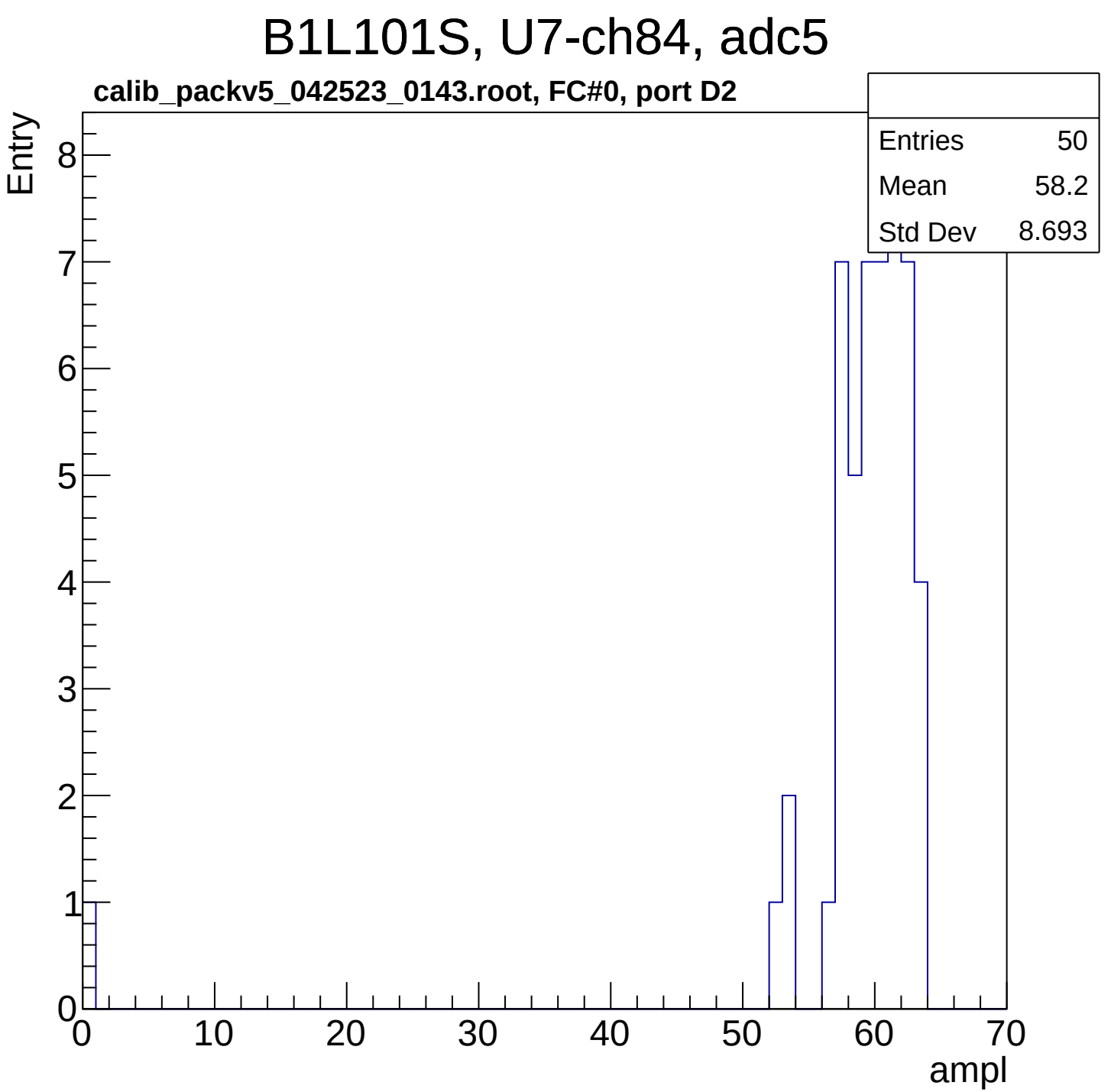
B1L101S, U7-ch84, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 58.2
Std Dev 8.693
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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20
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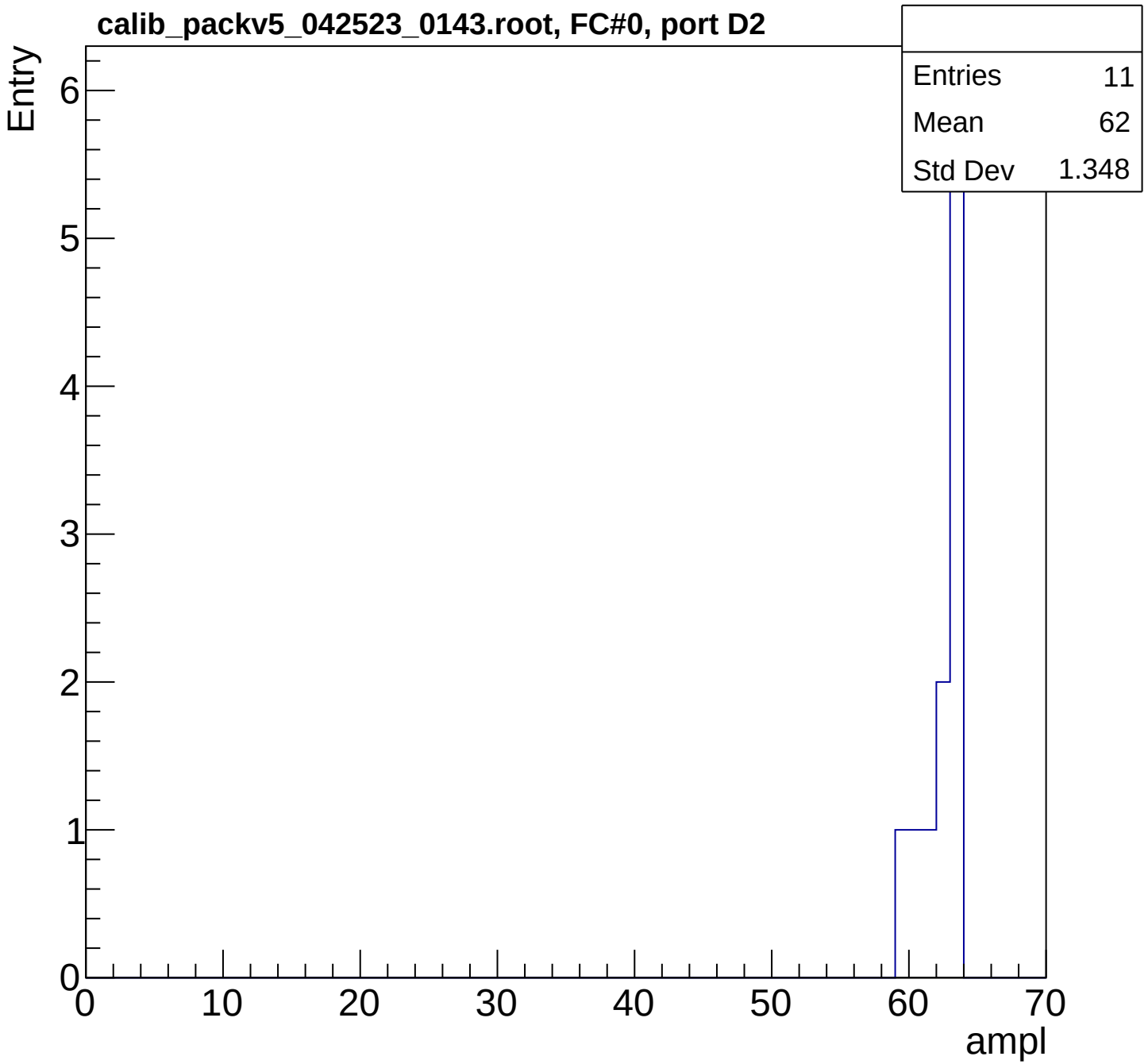
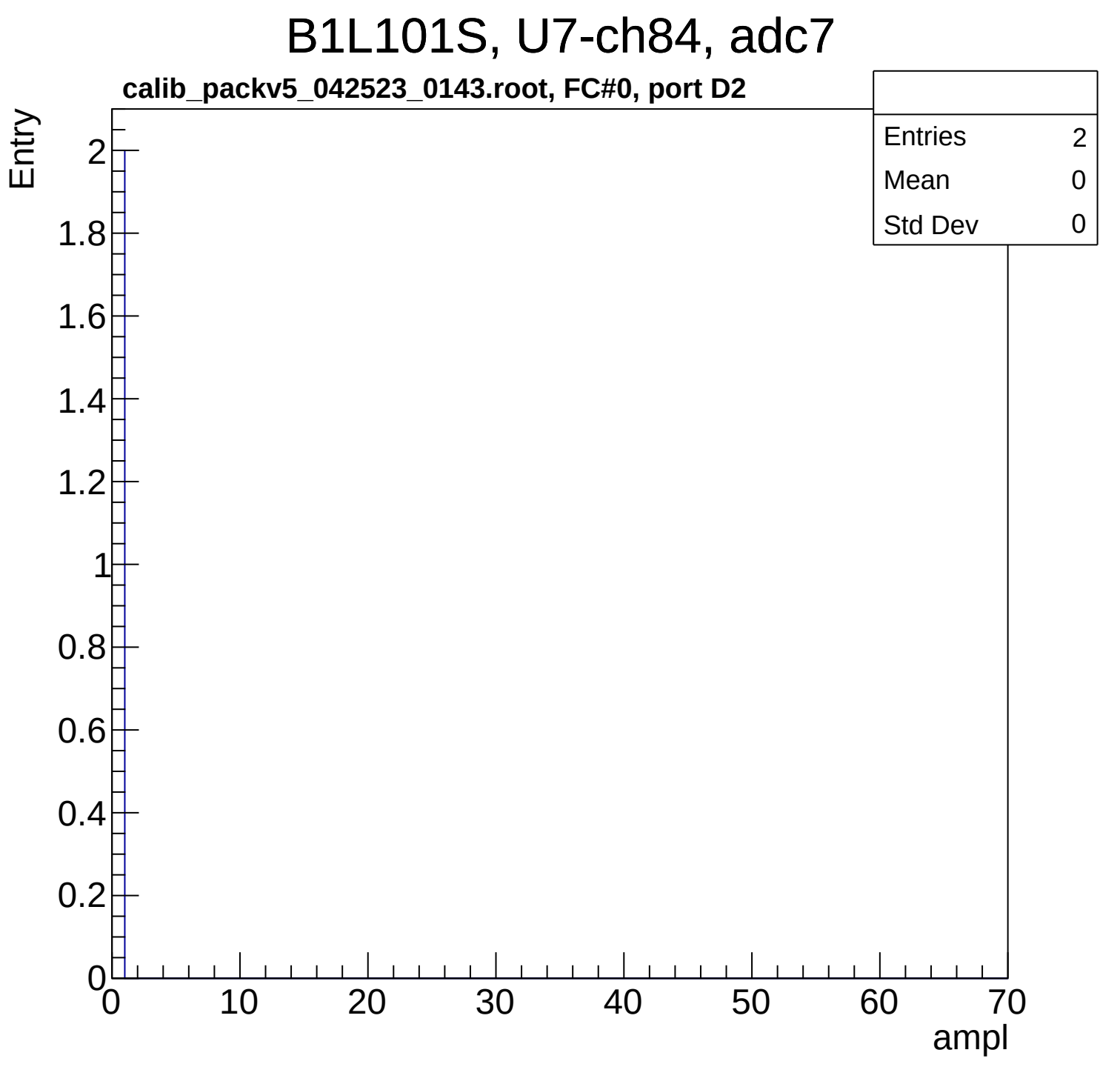
40
50
60
70


B1L101S, U7-ch84, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 11
Mean 62
Std Dev 1.348
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch84, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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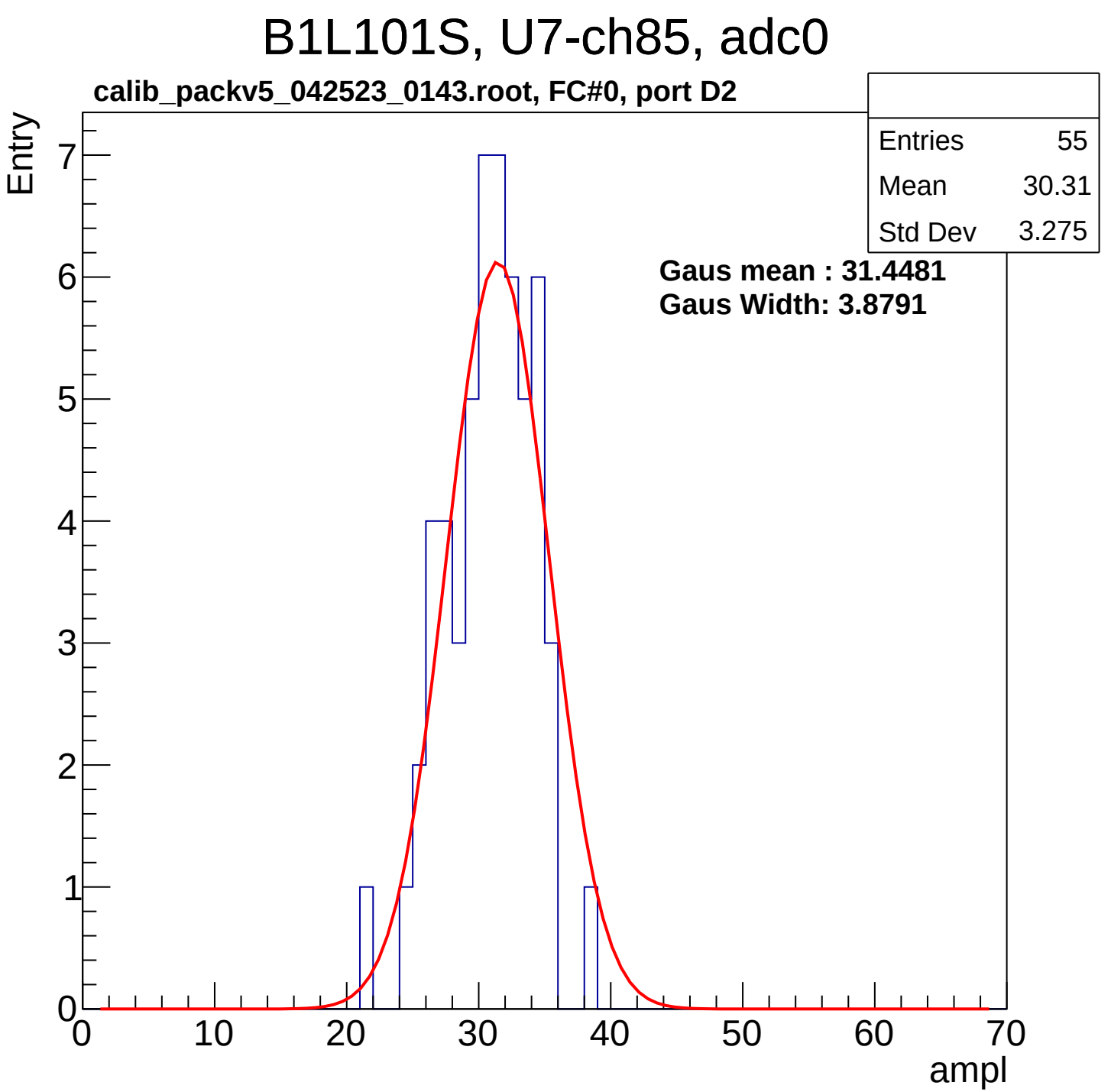
B1L101S, U7-ch85, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 30.31
Std Dev 3.275
Gaus mean : 31.4481
Gaus Width: 3.8791
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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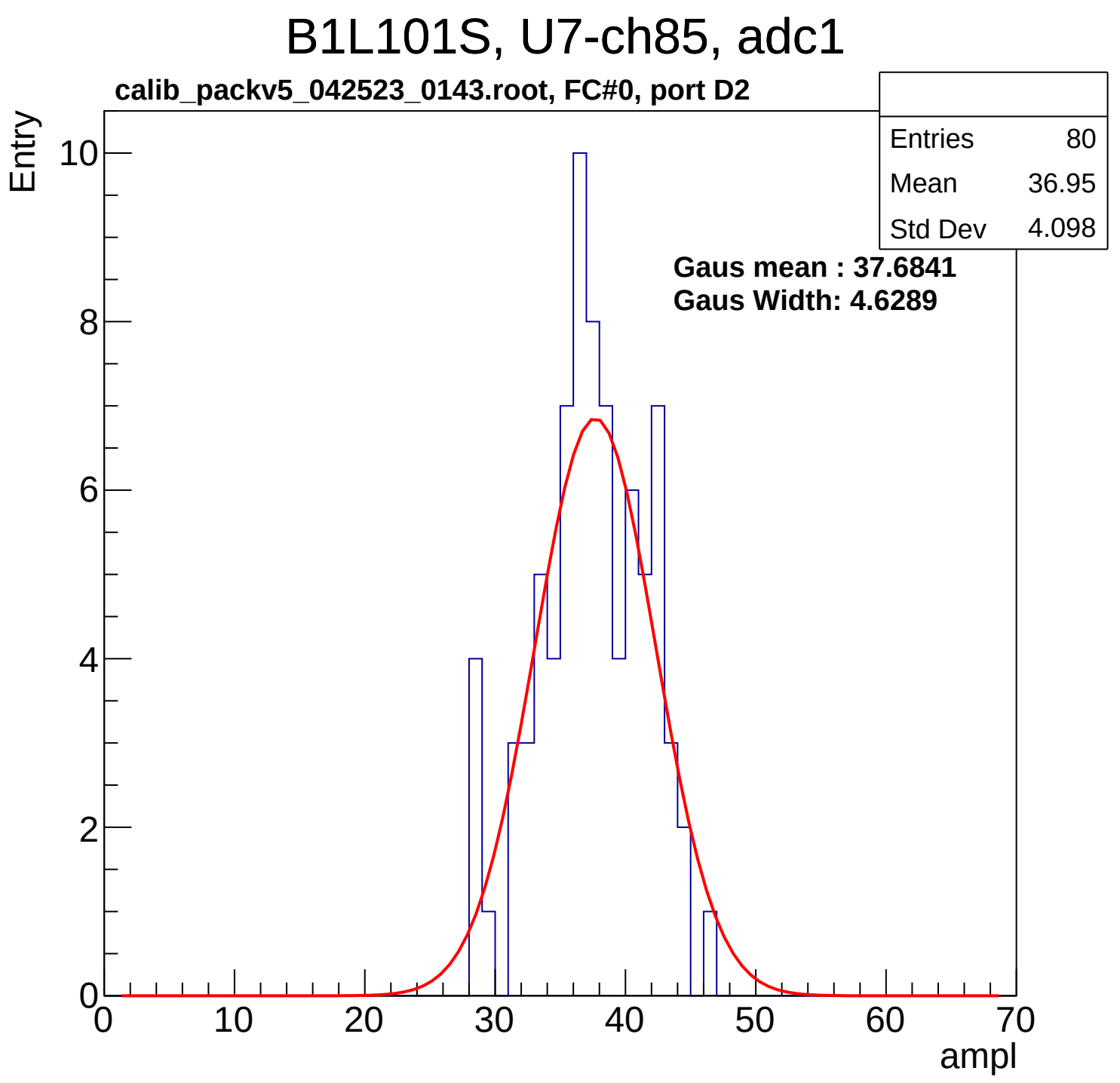
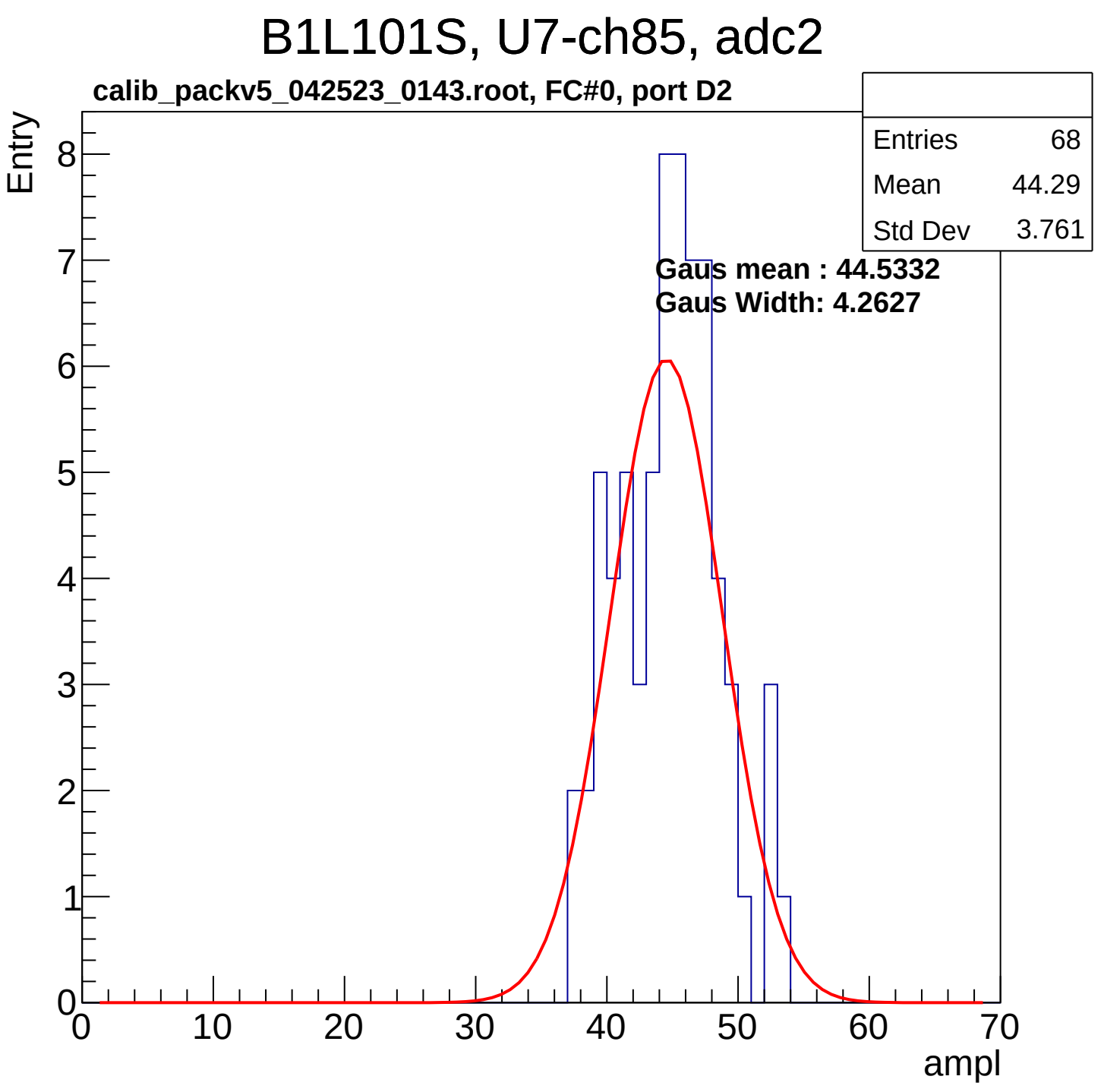

B1L101S, U7-ch85, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 80
Mean 36.95
Std Dev 4.098
Gaus mean : 37.6841
Gaus Width: 4.6289
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch85, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 44.29
Std Dev 3.761
Gaus mean : 44.5332
Gaus Width: 4.2627
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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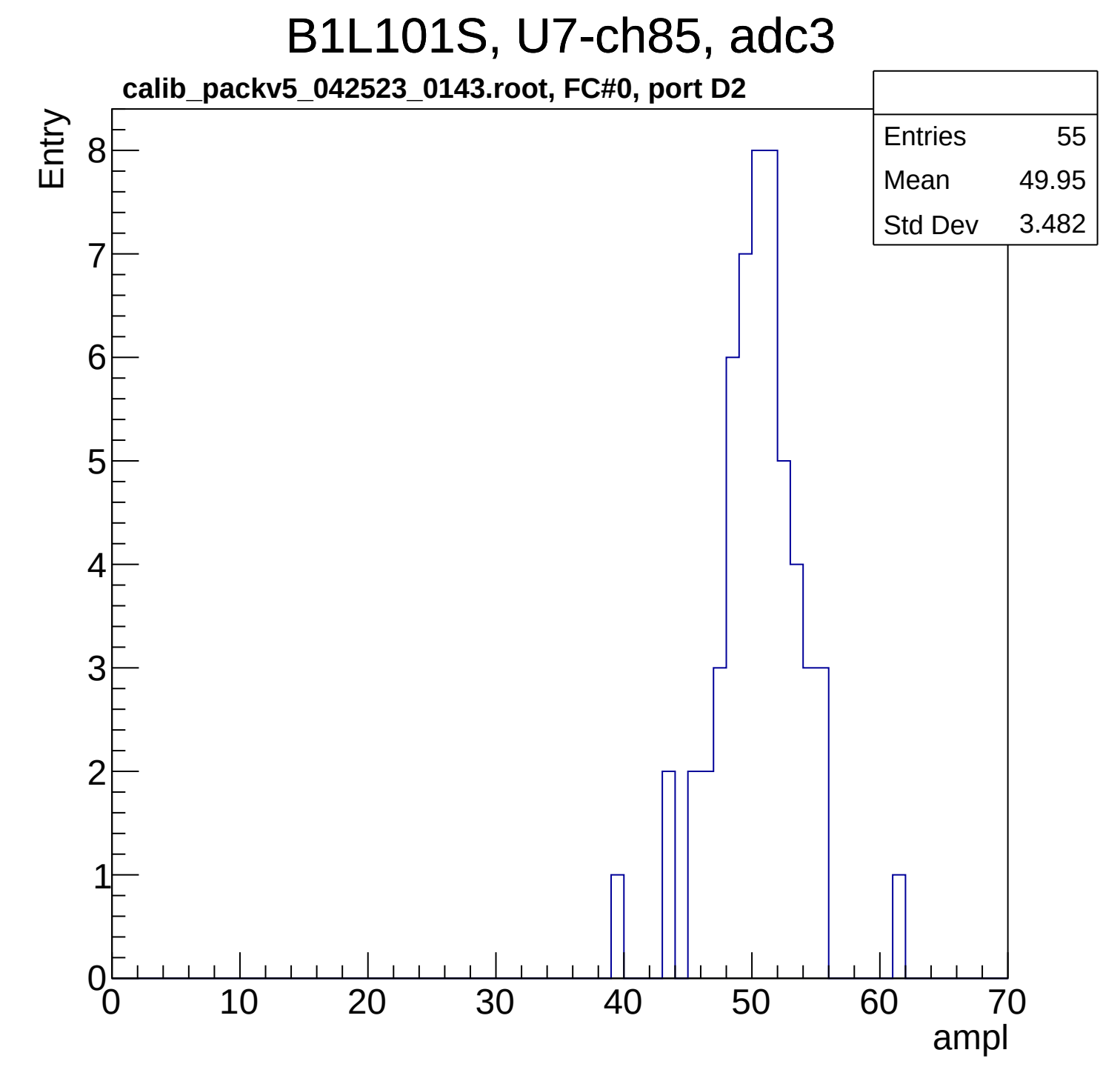
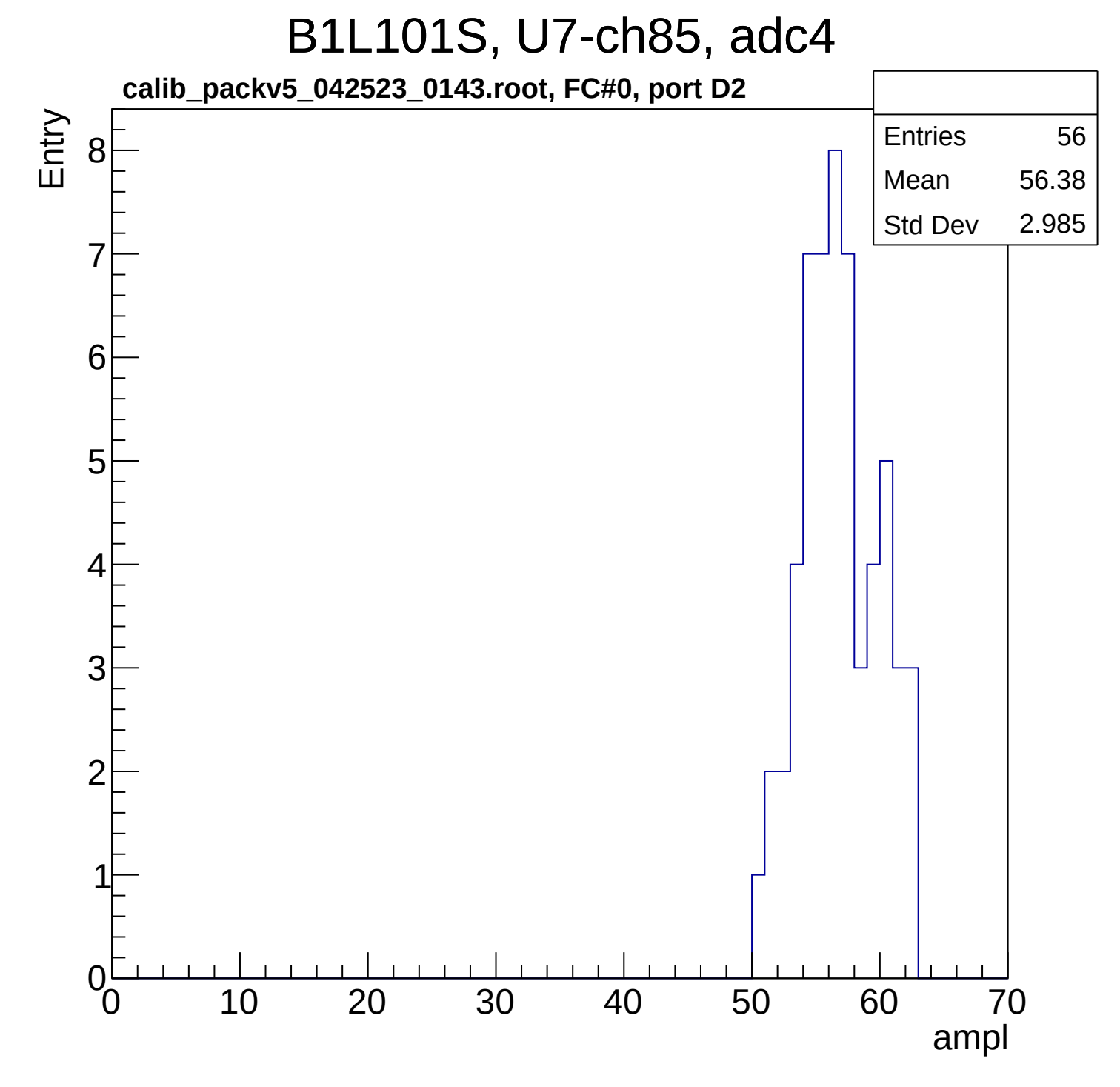

B1L101S, U7-ch85, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 49.95
Std Dev 3.482
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch85, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 56.38
Std Dev 2.985
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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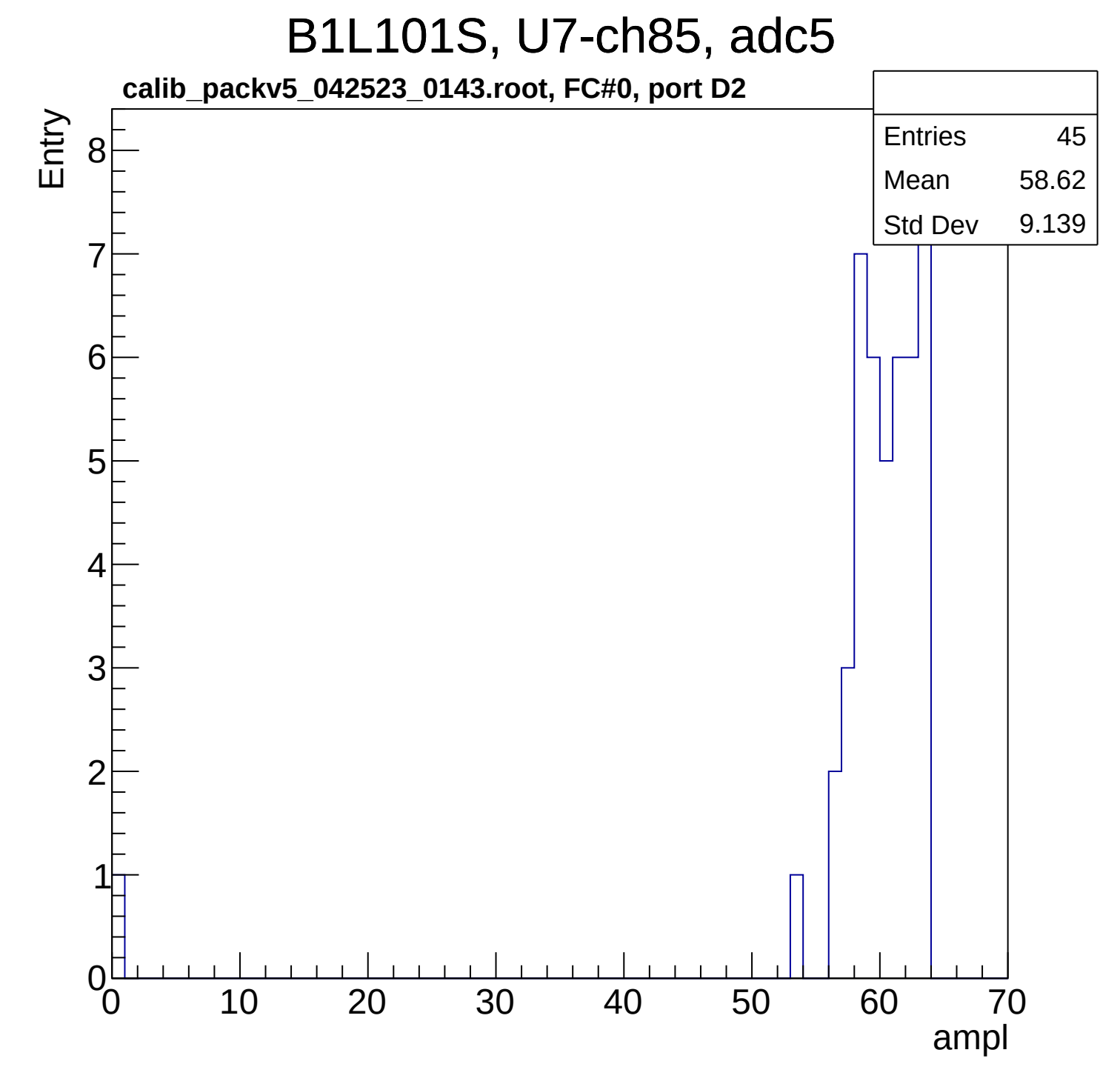
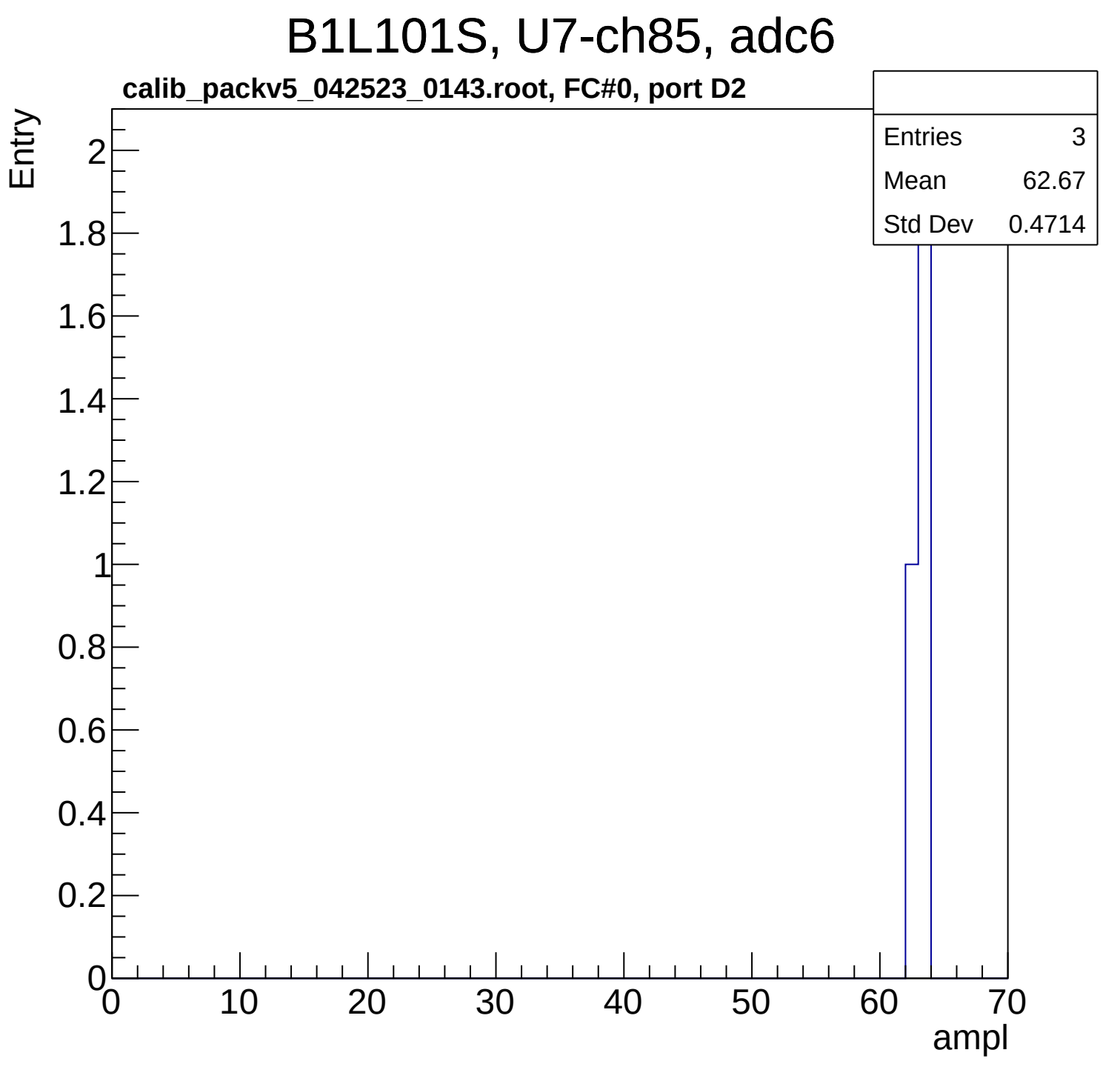
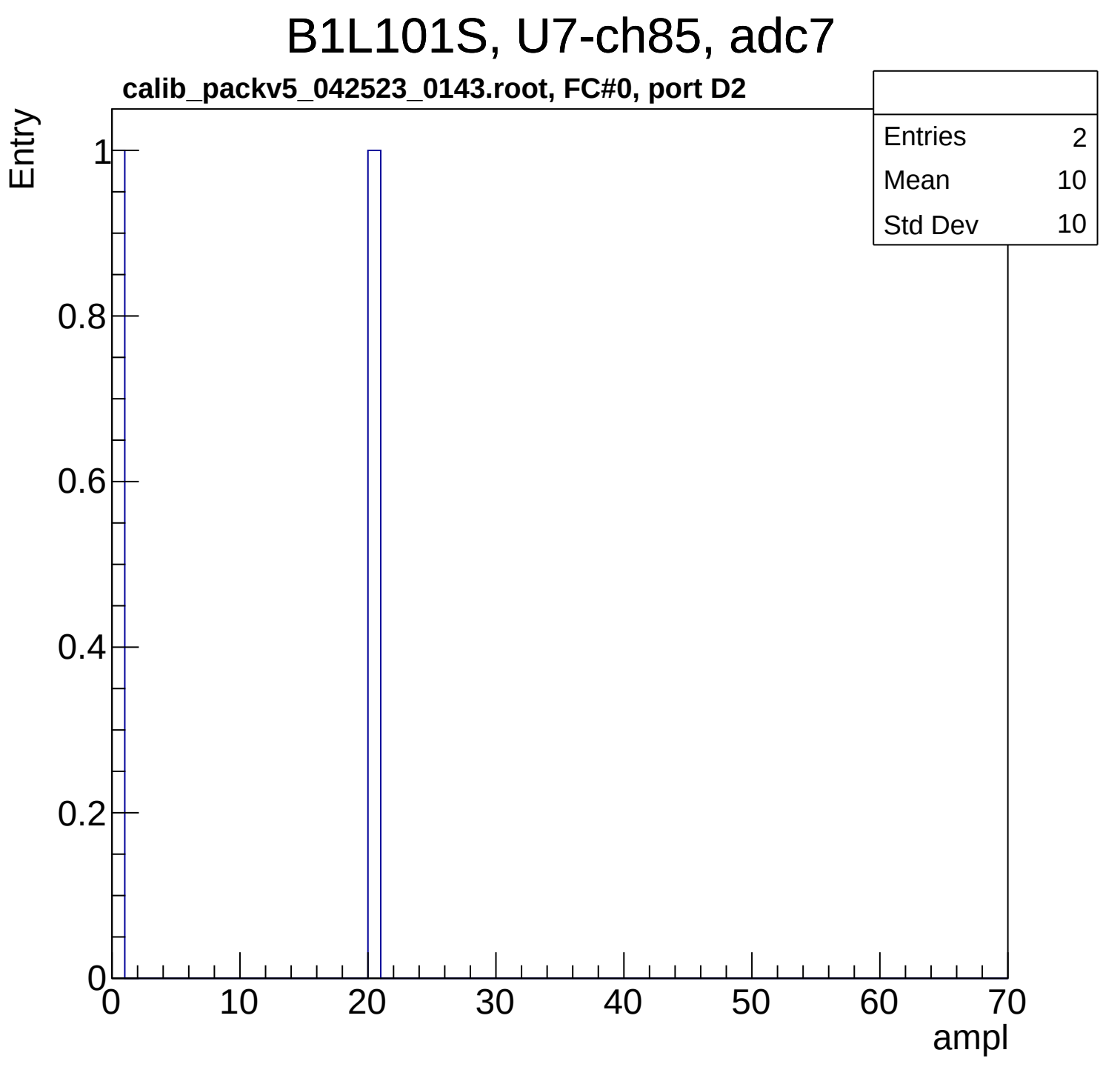
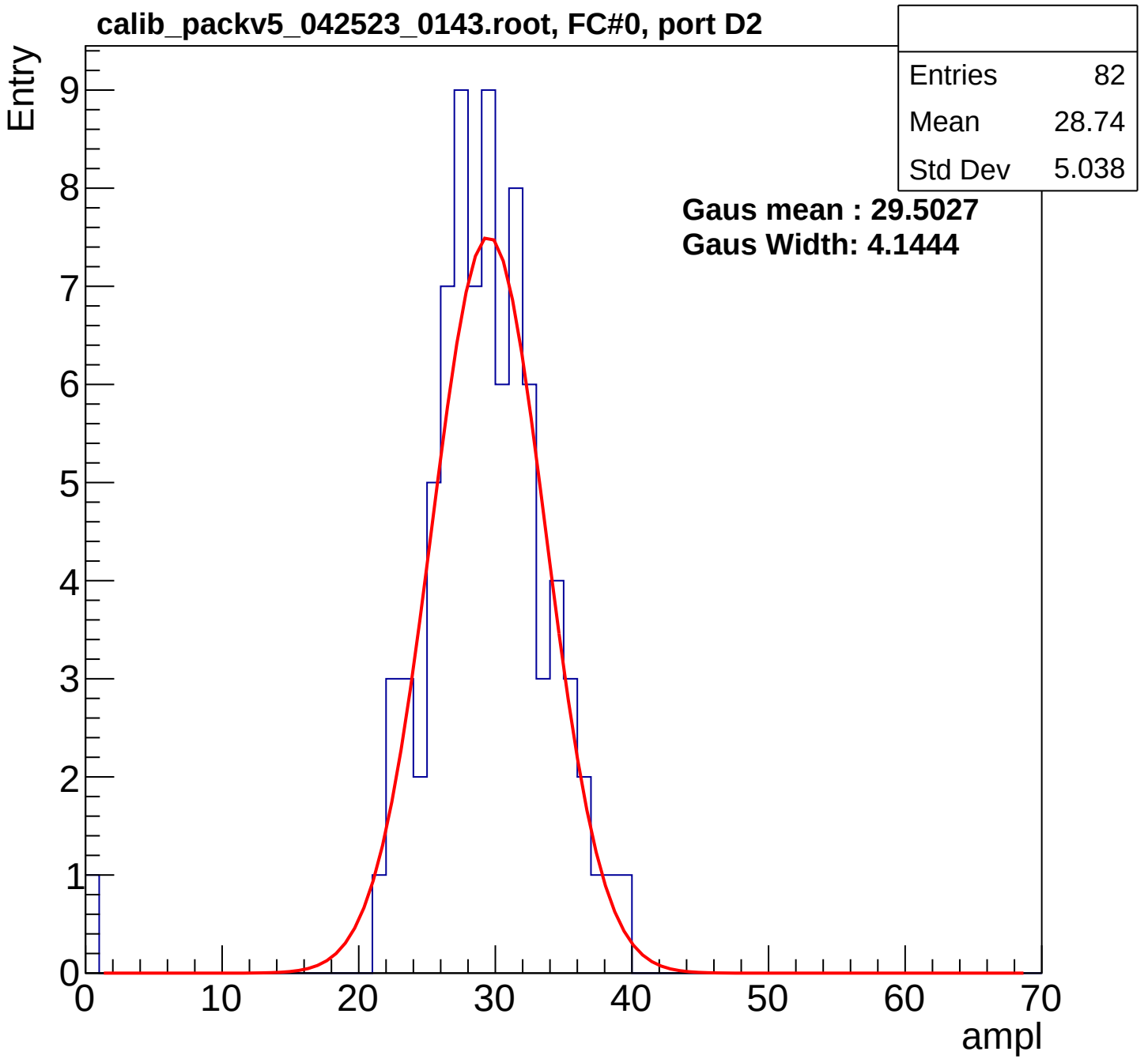

B1L101S, U7-ch85, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 58.62
Std Dev 9.139
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch85, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U7-ch85, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 10
Std Dev 10
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch86, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 82
Mean 28.74
Std Dev 5.038
Gaus mean : 29.5027
Gaus Width: 4.1444
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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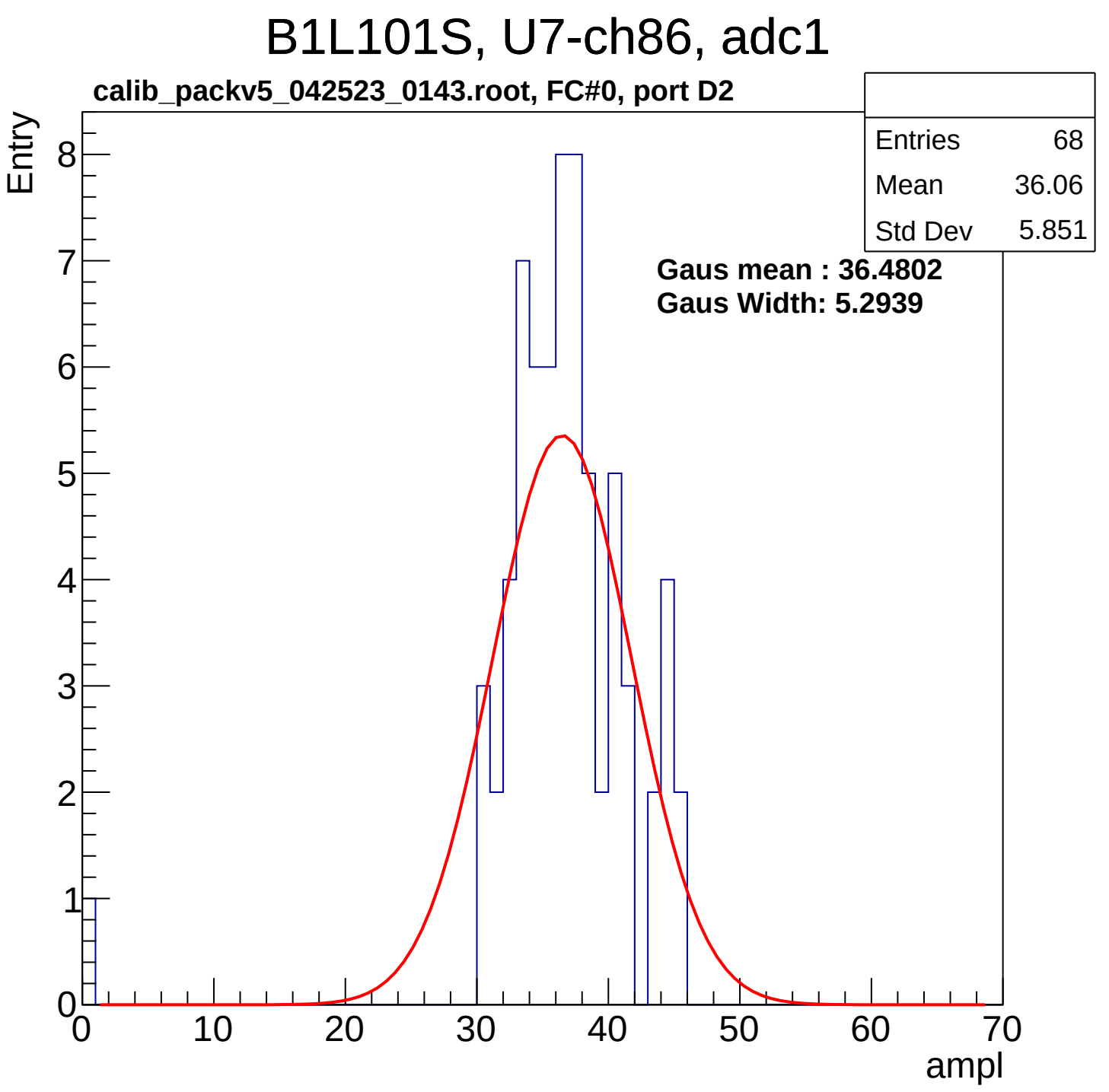
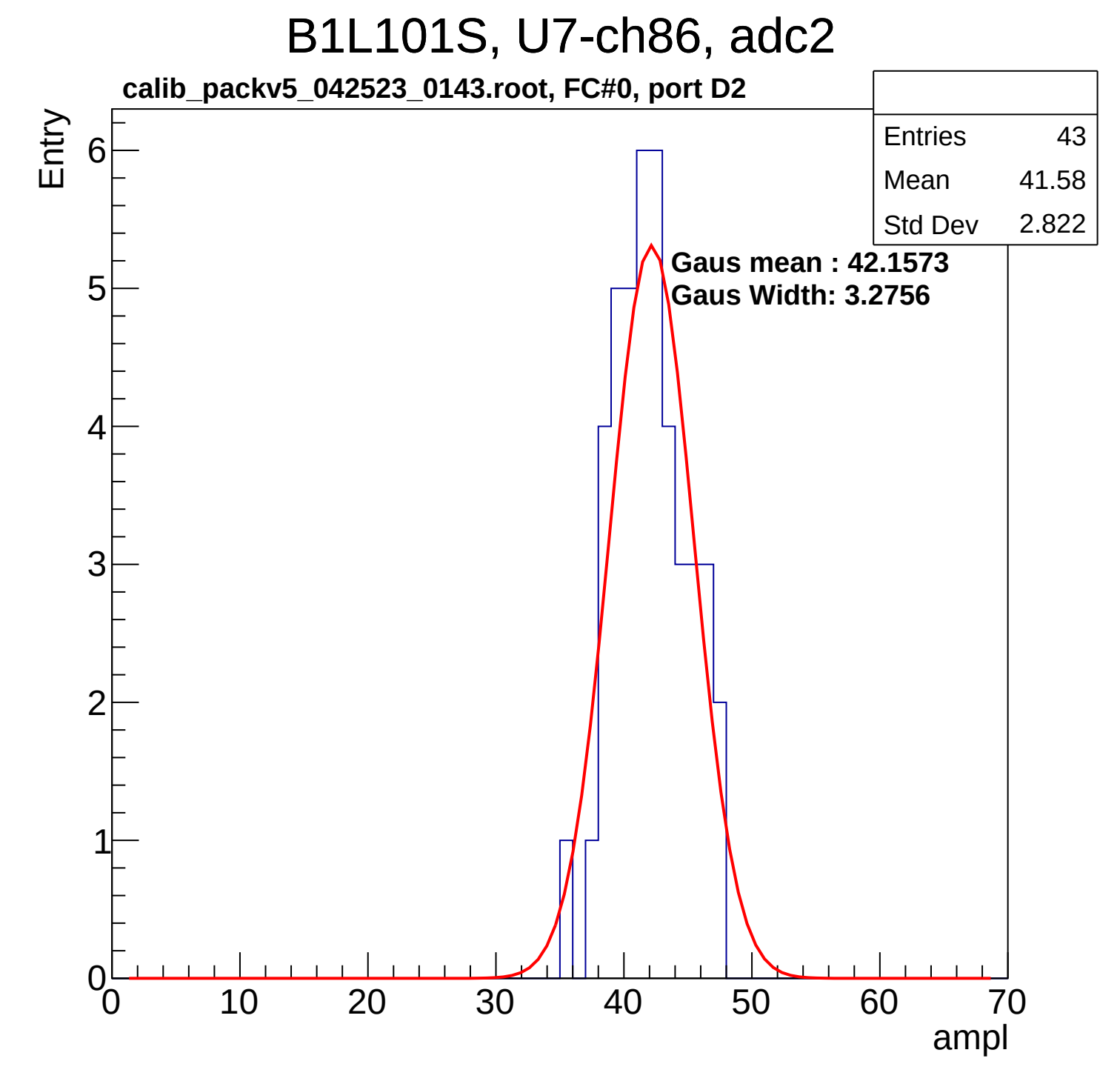
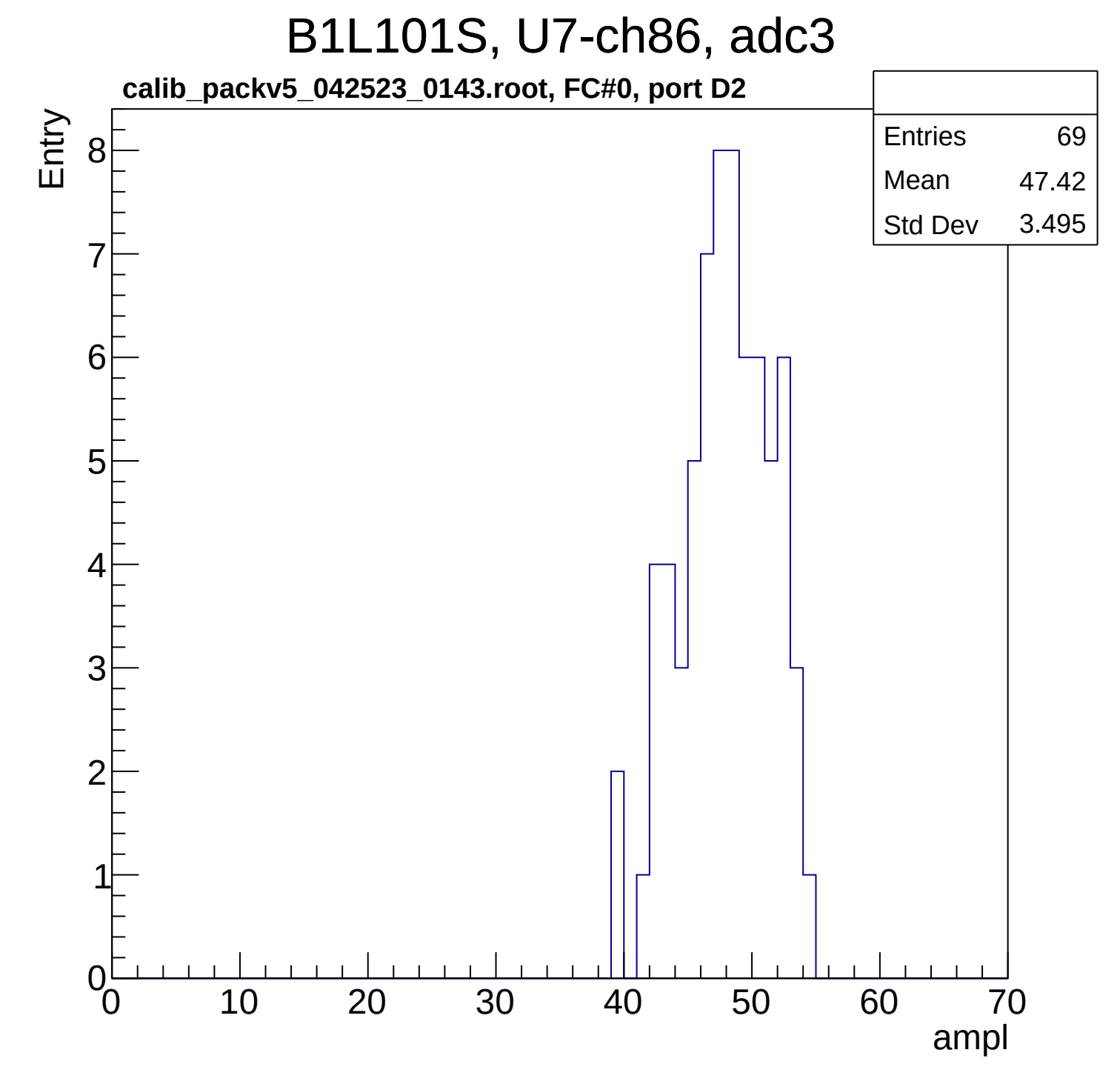

B1L101S, U7-ch86, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 36.06
Std Dev 5.851
Gaus mean : 36.4802
Gaus Width: 5.2939
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch86, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 43
Mean 41.58
Std Dev 2.822
Gaus mean : 42.1573
Gaus Width: 3.2756
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L101S, U7-ch86, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 47.42
Std Dev 3.495
Entry
ampl
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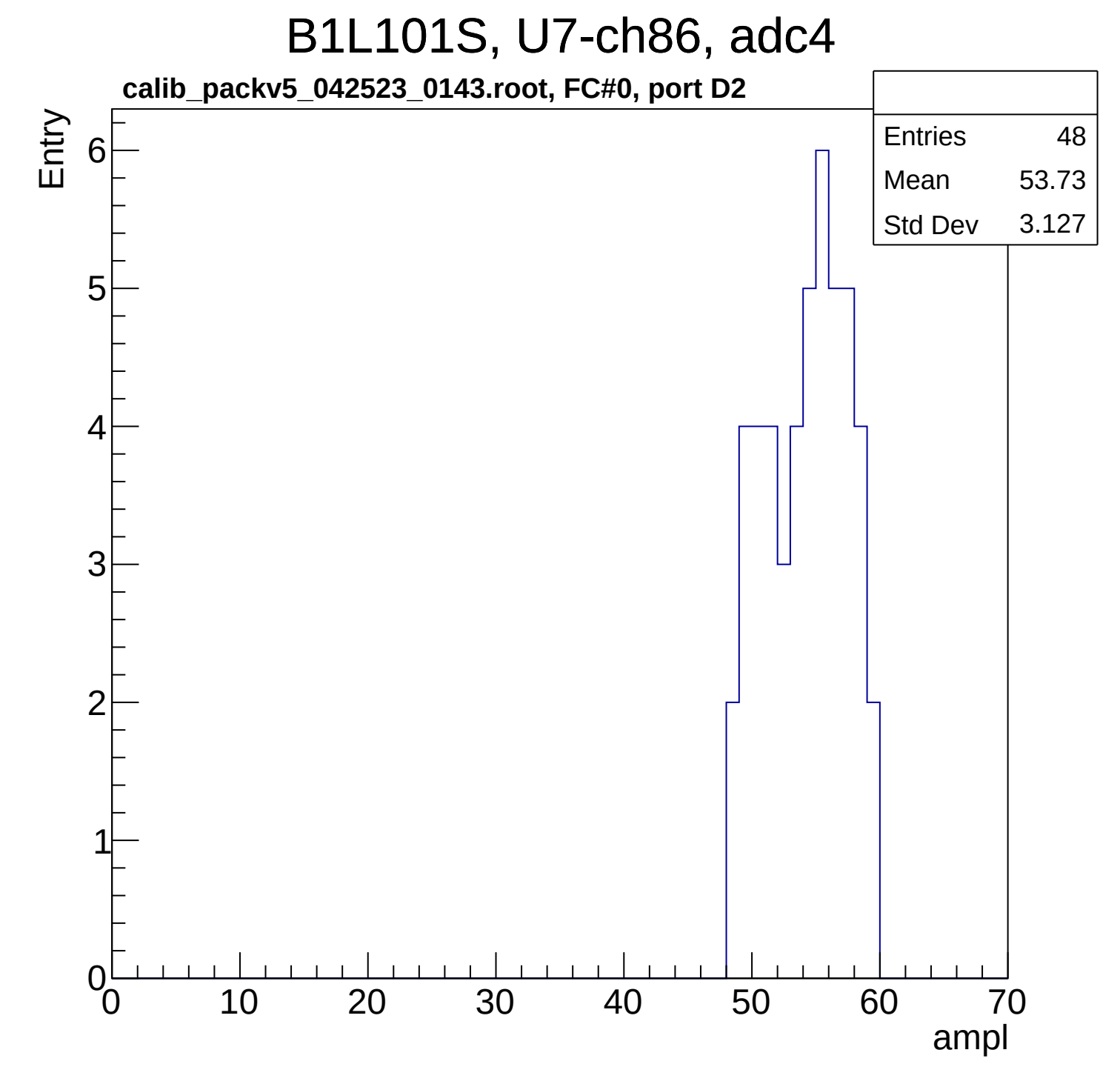
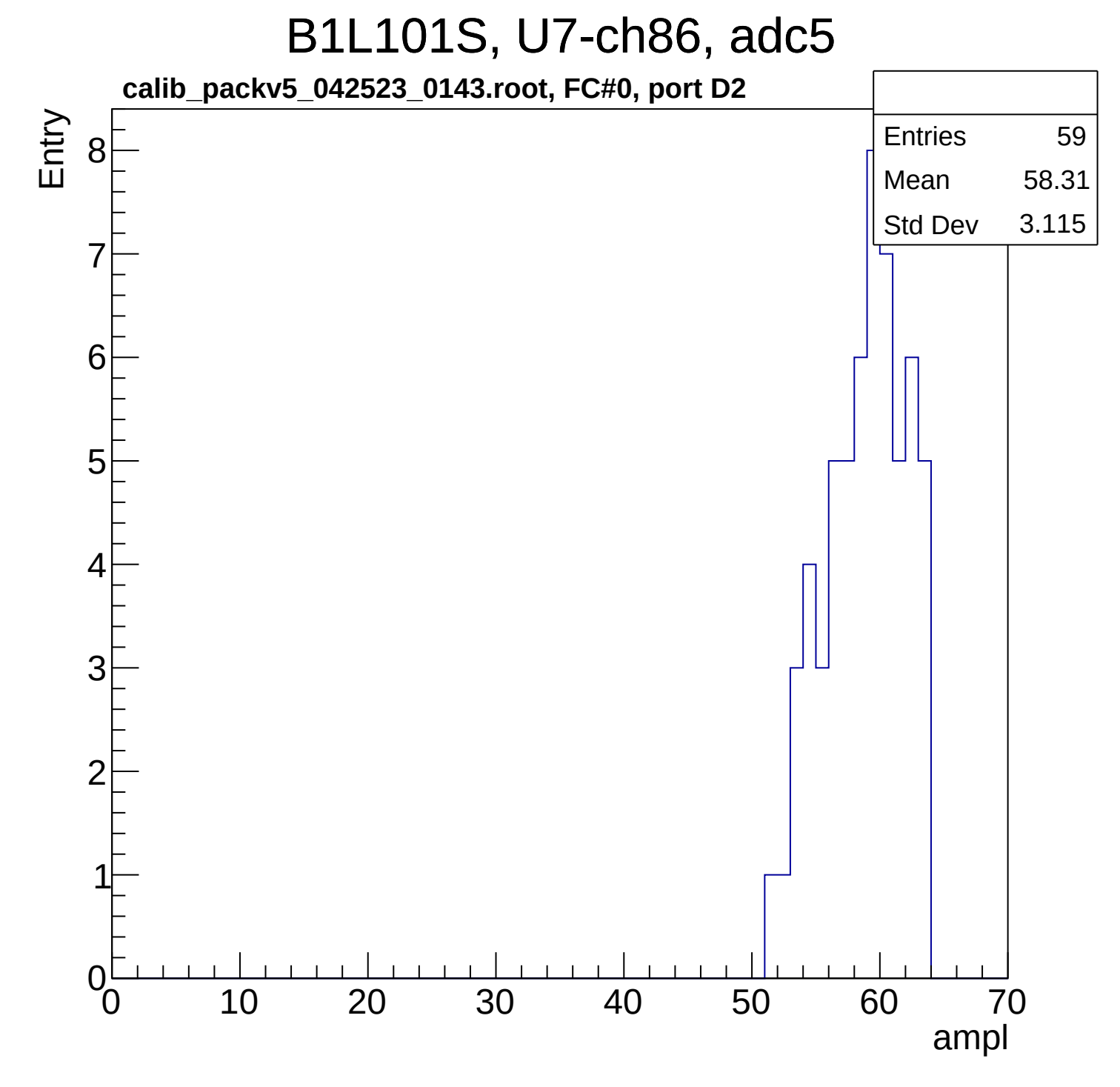
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch86, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 53.73
Std Dev 3.127
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch86, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 58.31
Std Dev 3.115
Entry
ampl
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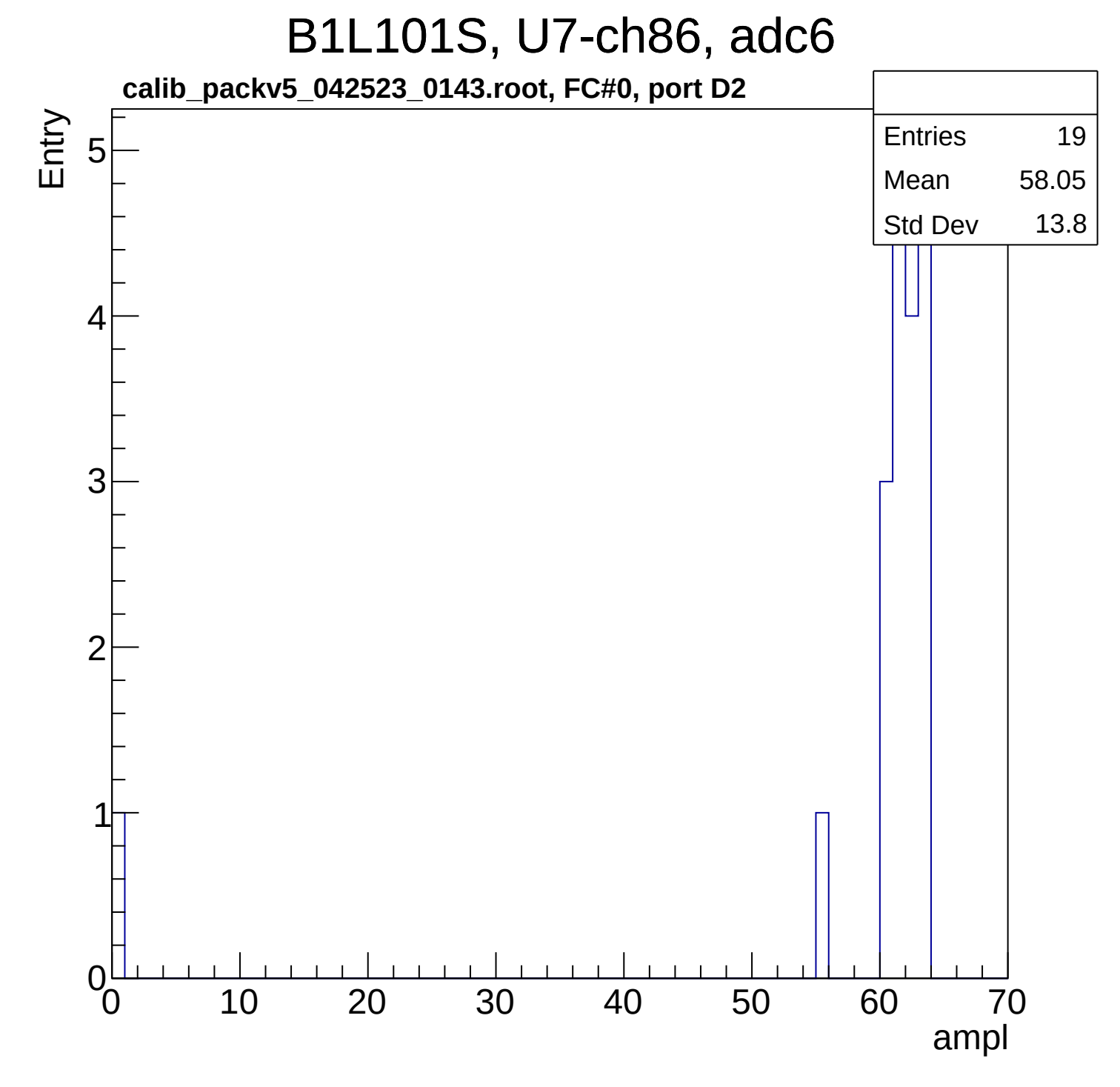
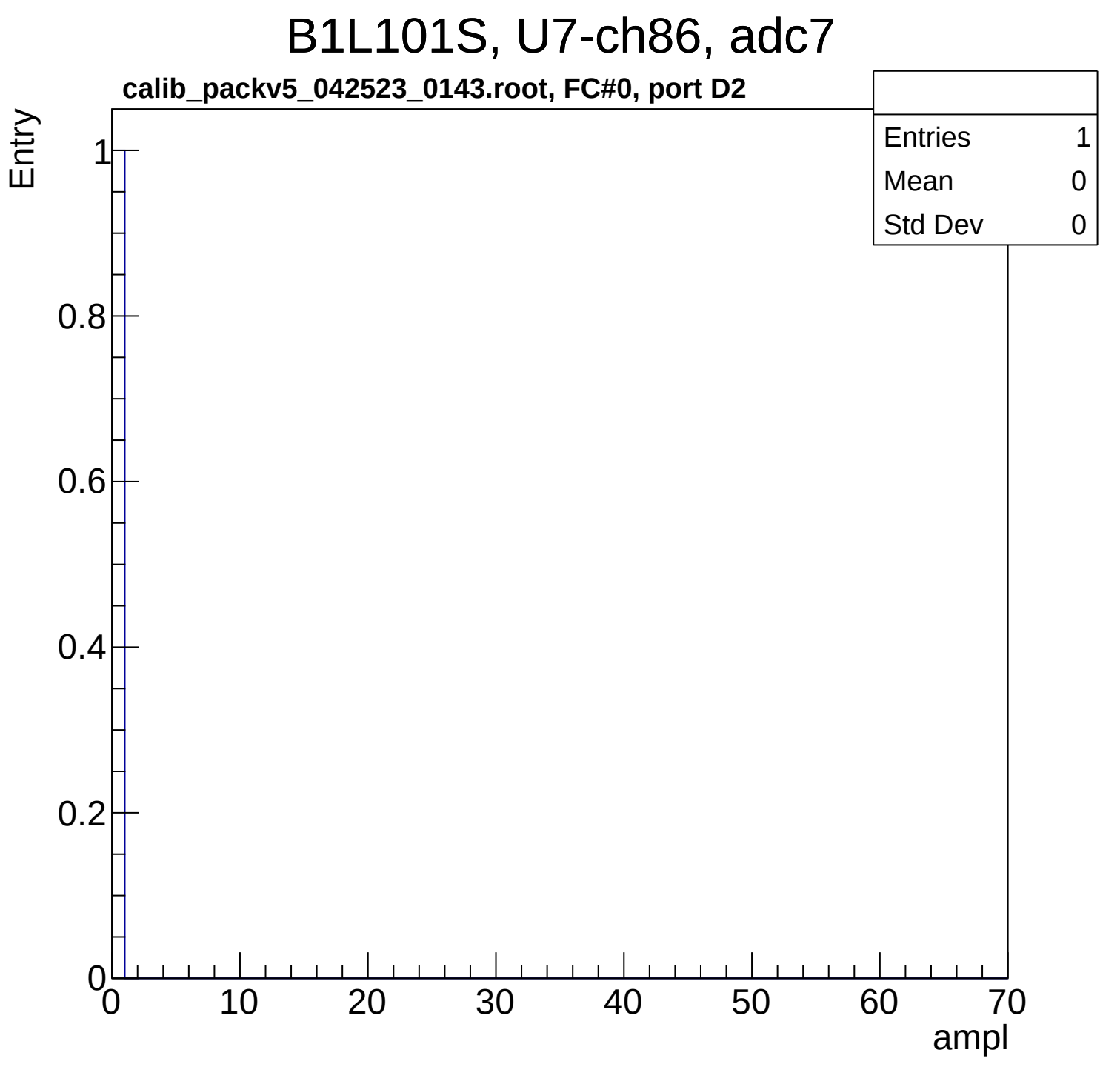
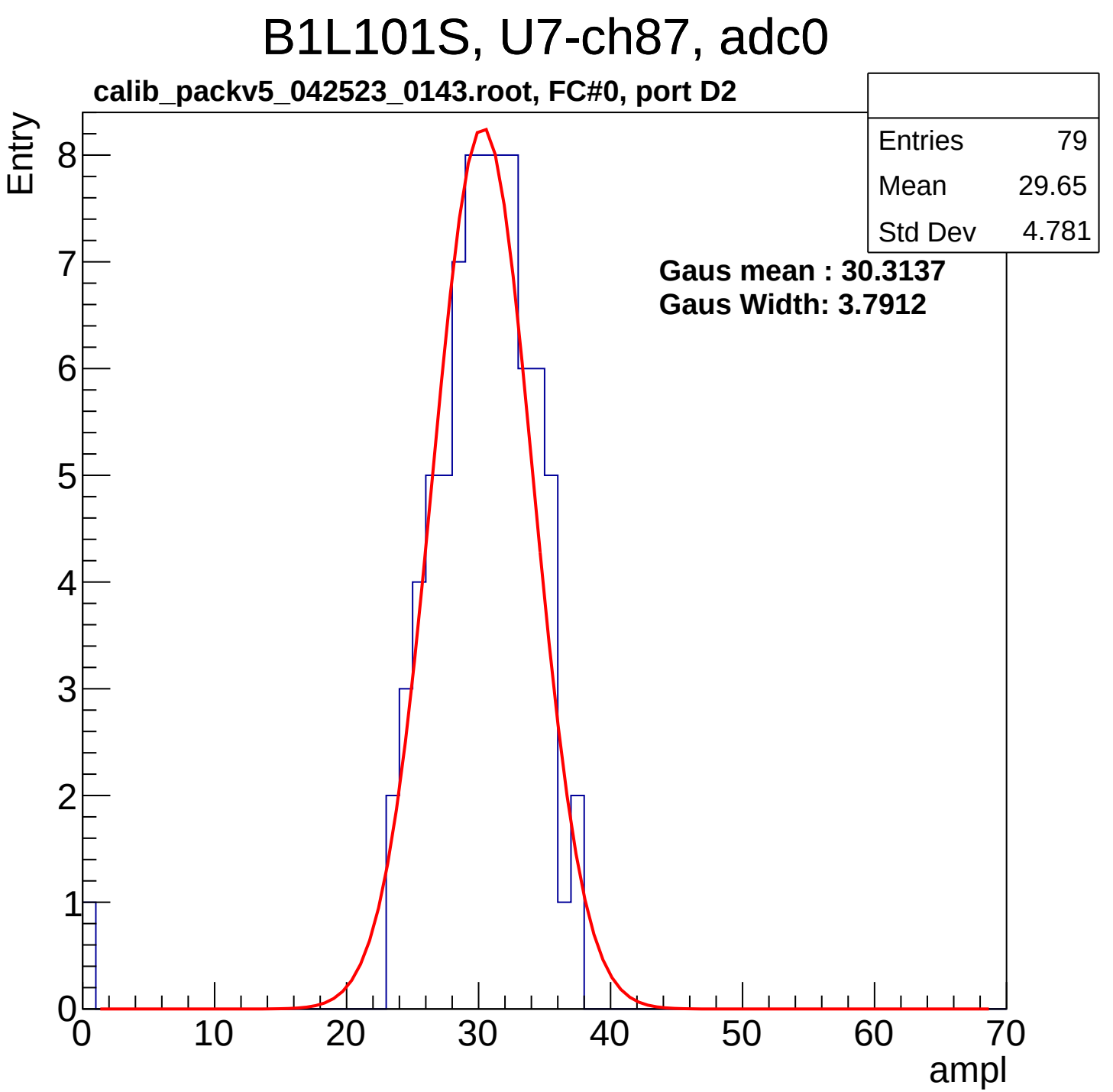
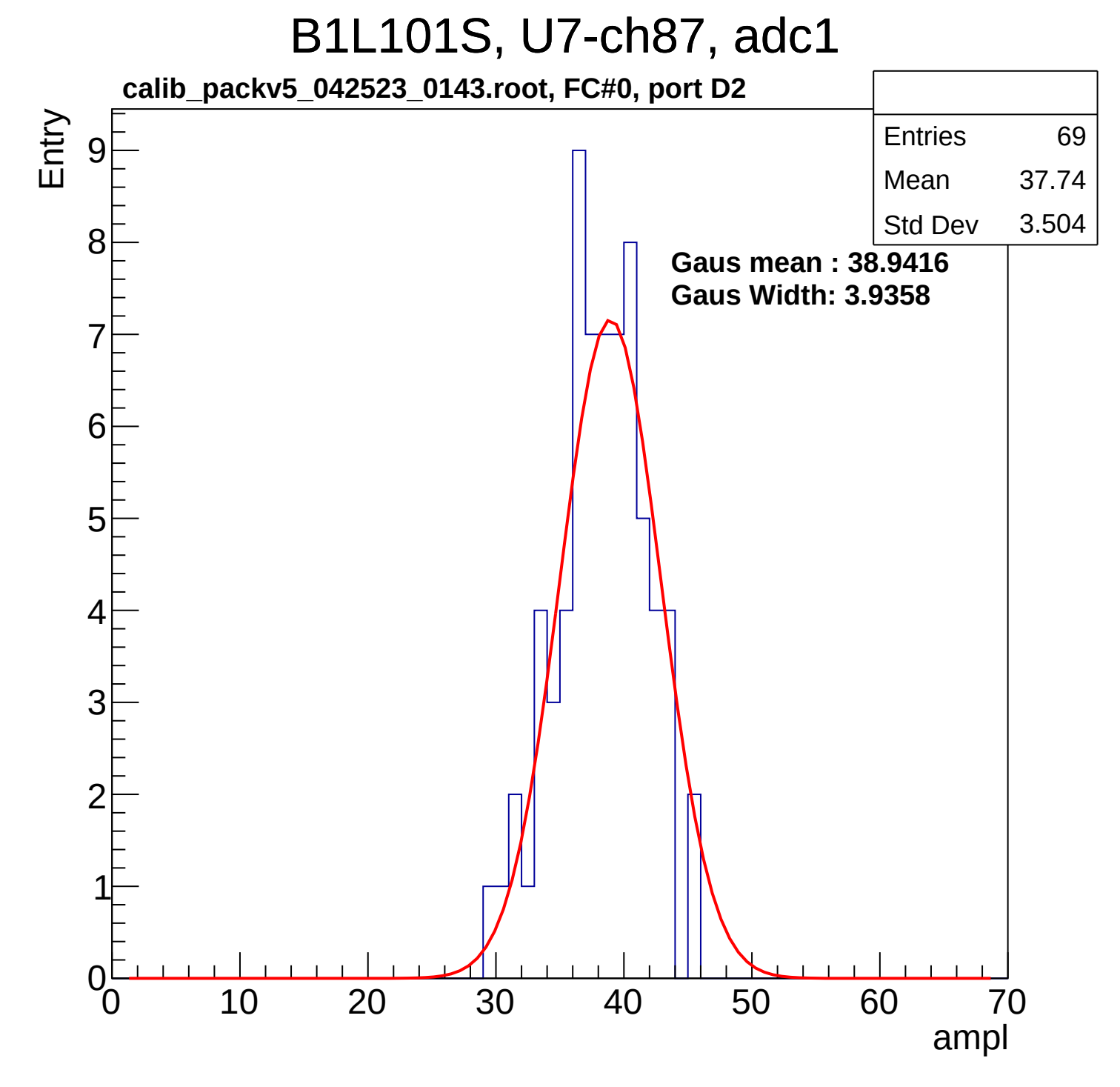
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch86, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 19
Mean 58.05
Std Dev 13.8
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L101S, U7-ch86, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch87, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 29.65
Std Dev 4.781
Gaus mean : 30.3137
Gaus Width: 3.7912
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch87, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 37.74
Std Dev 3.504
Gaus mean : 38.9416
Gaus Width: 3.9358
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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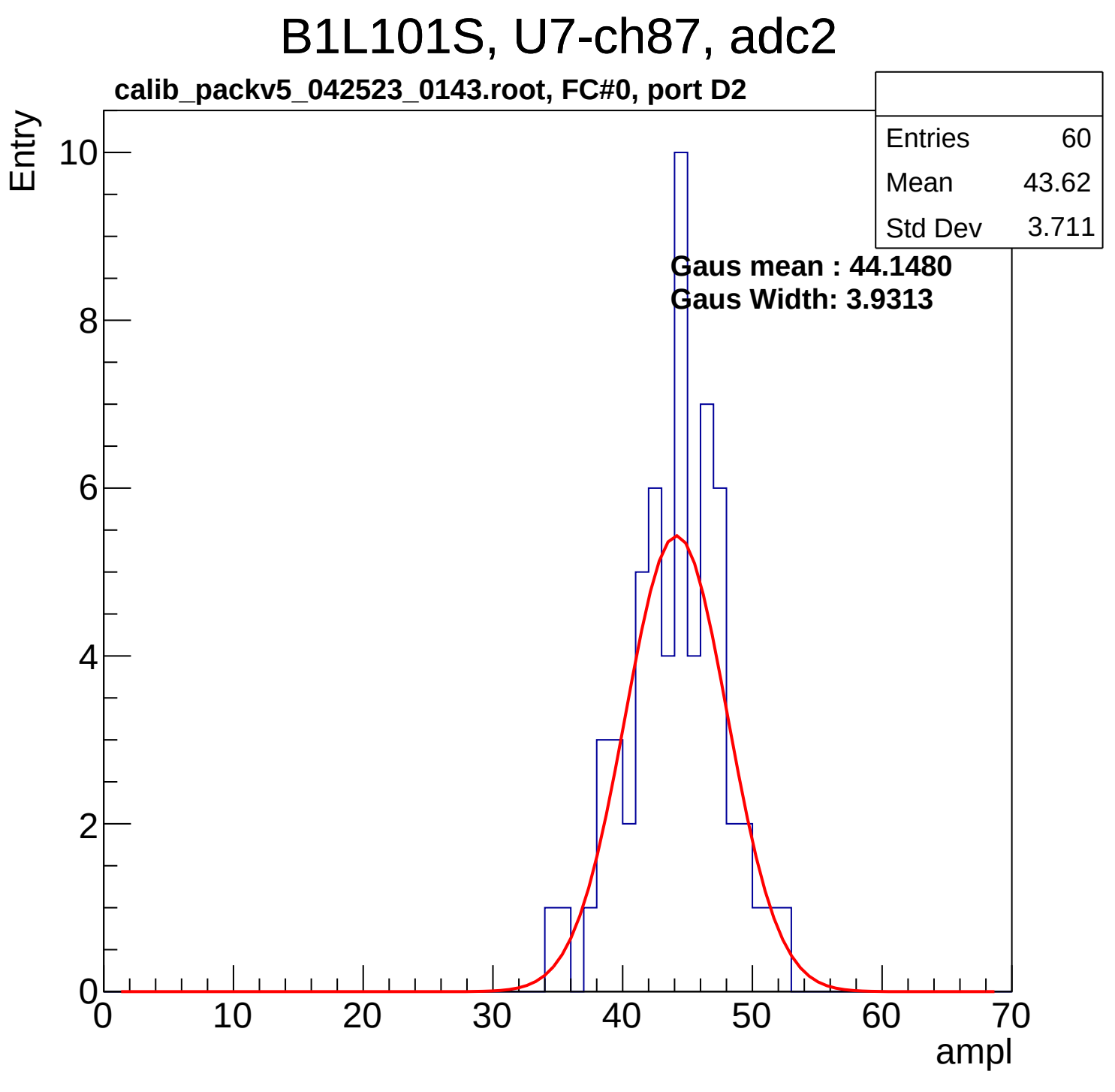
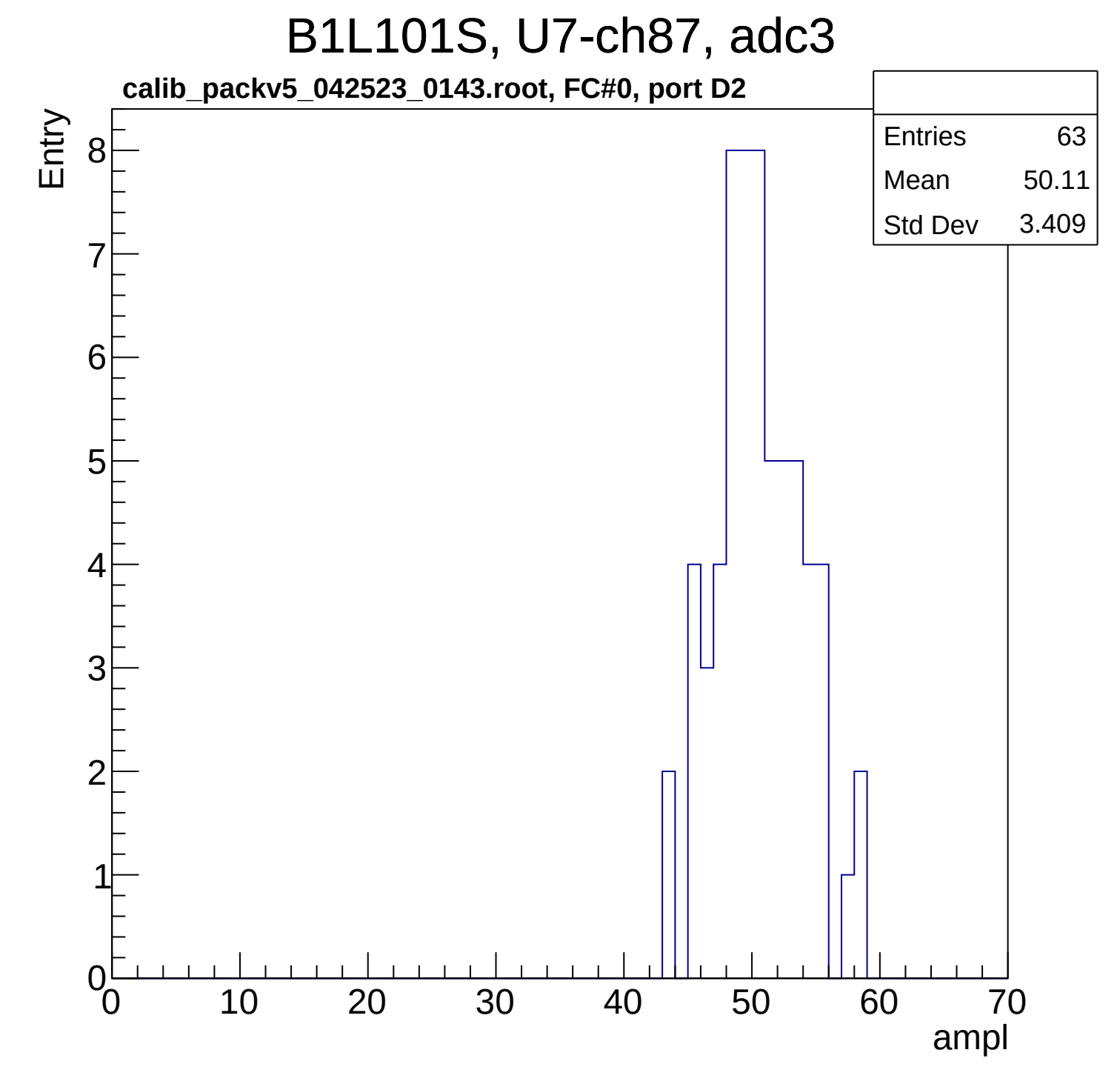
40
50
60
70


B1L101S, U7-ch87, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 43.62
Std Dev 3.711
Gaus mean : 44.1480
Gaus Width: 3.9313
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch87, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 50.11
Std Dev 3.409
Entry
ampl
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1
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3
4
5
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7
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0
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20
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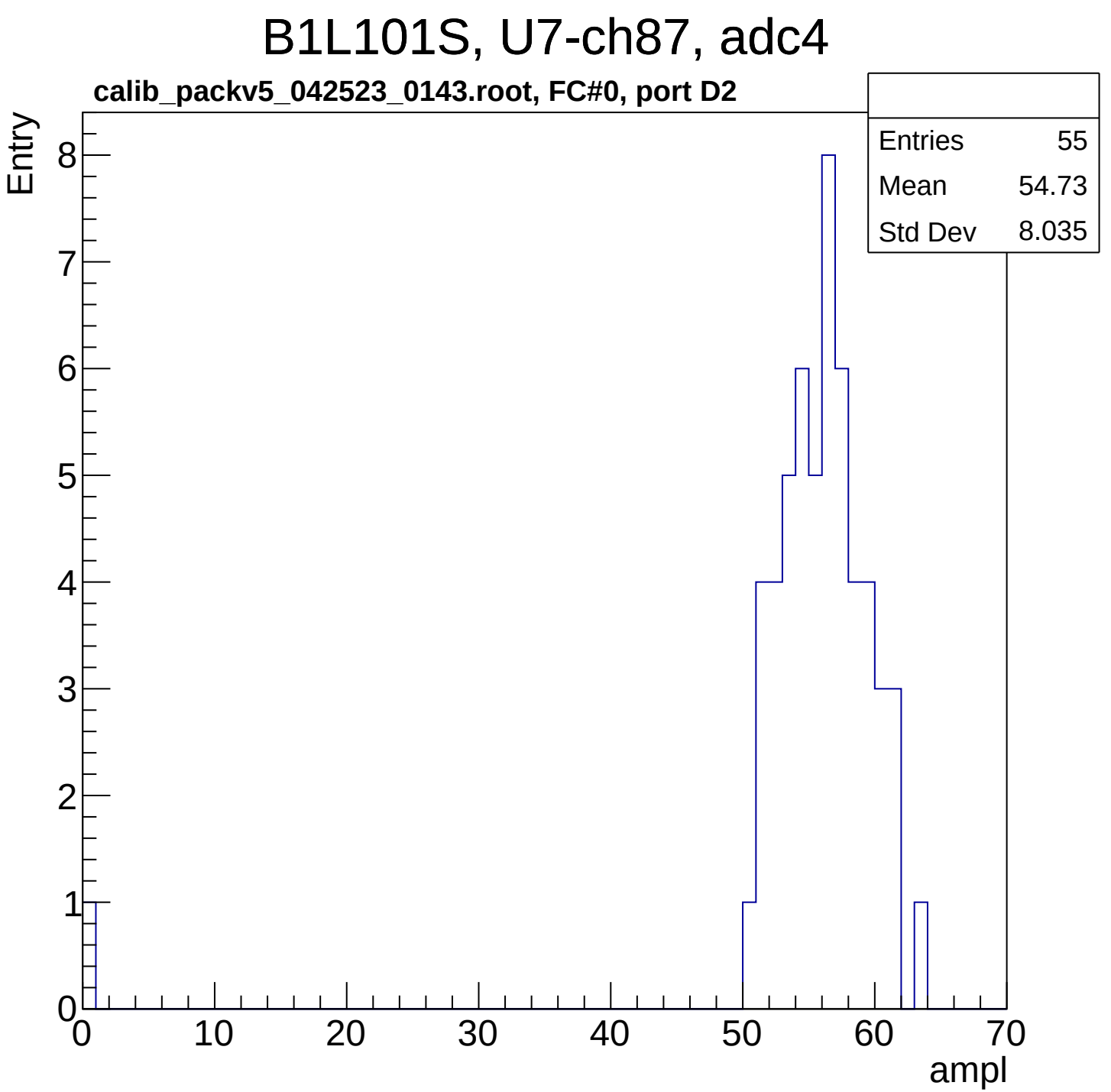
40
50
60
70


B1L101S, U7-ch87, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 54.73
Std Dev 8.035
Entry
0
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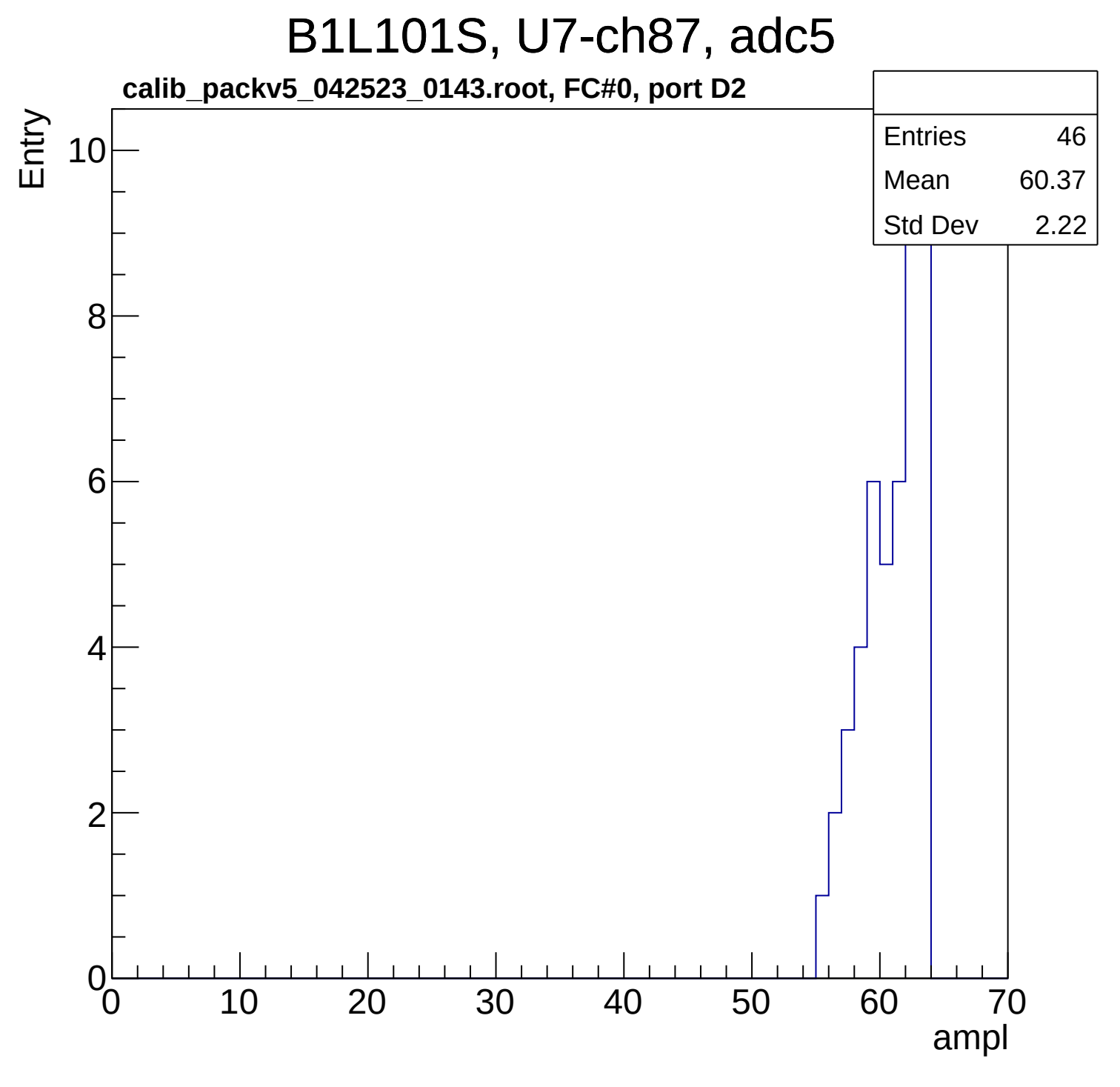
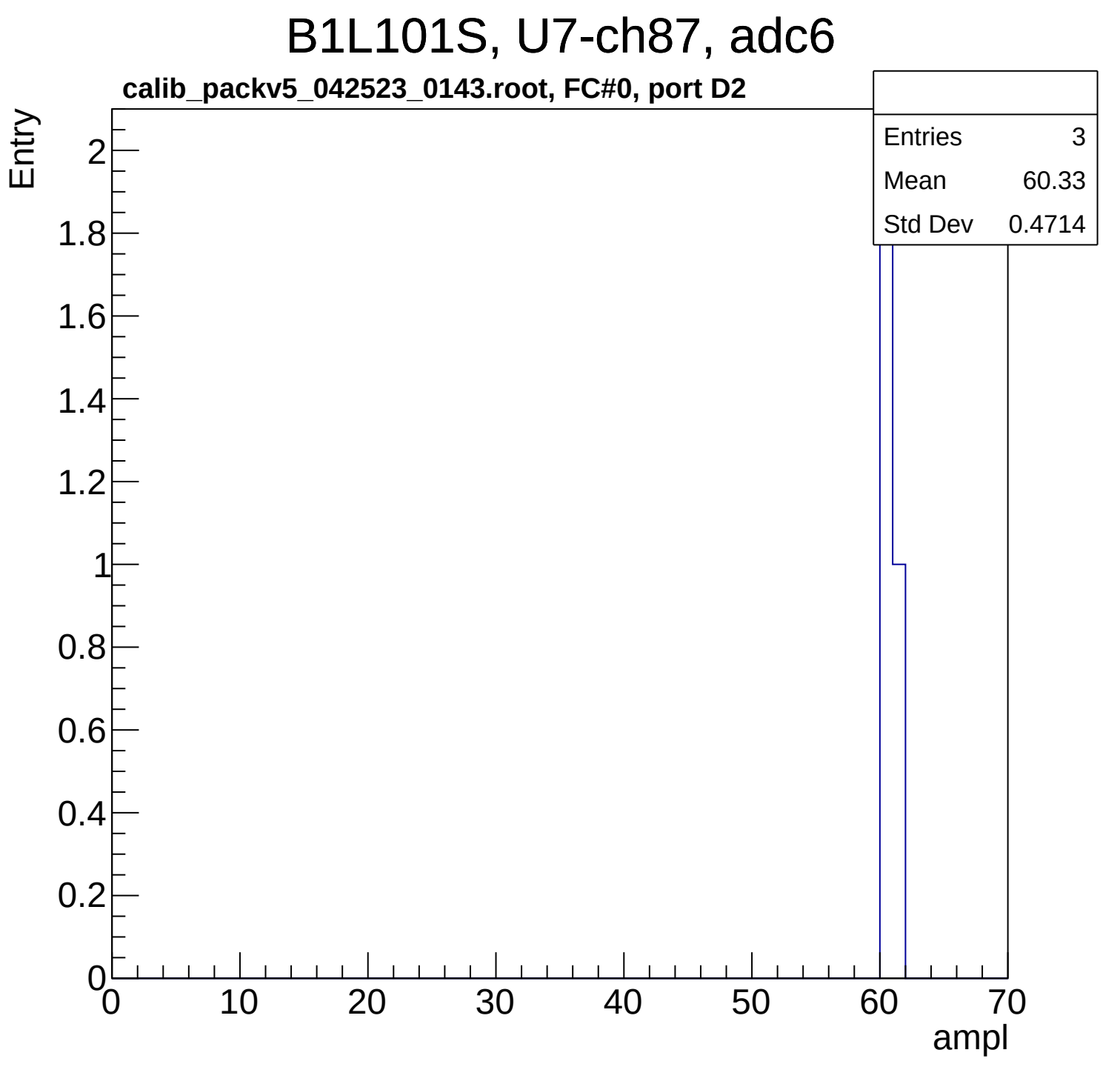
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch87, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 60.37
Std Dev 2.22
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch87, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 60.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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20
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40
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60
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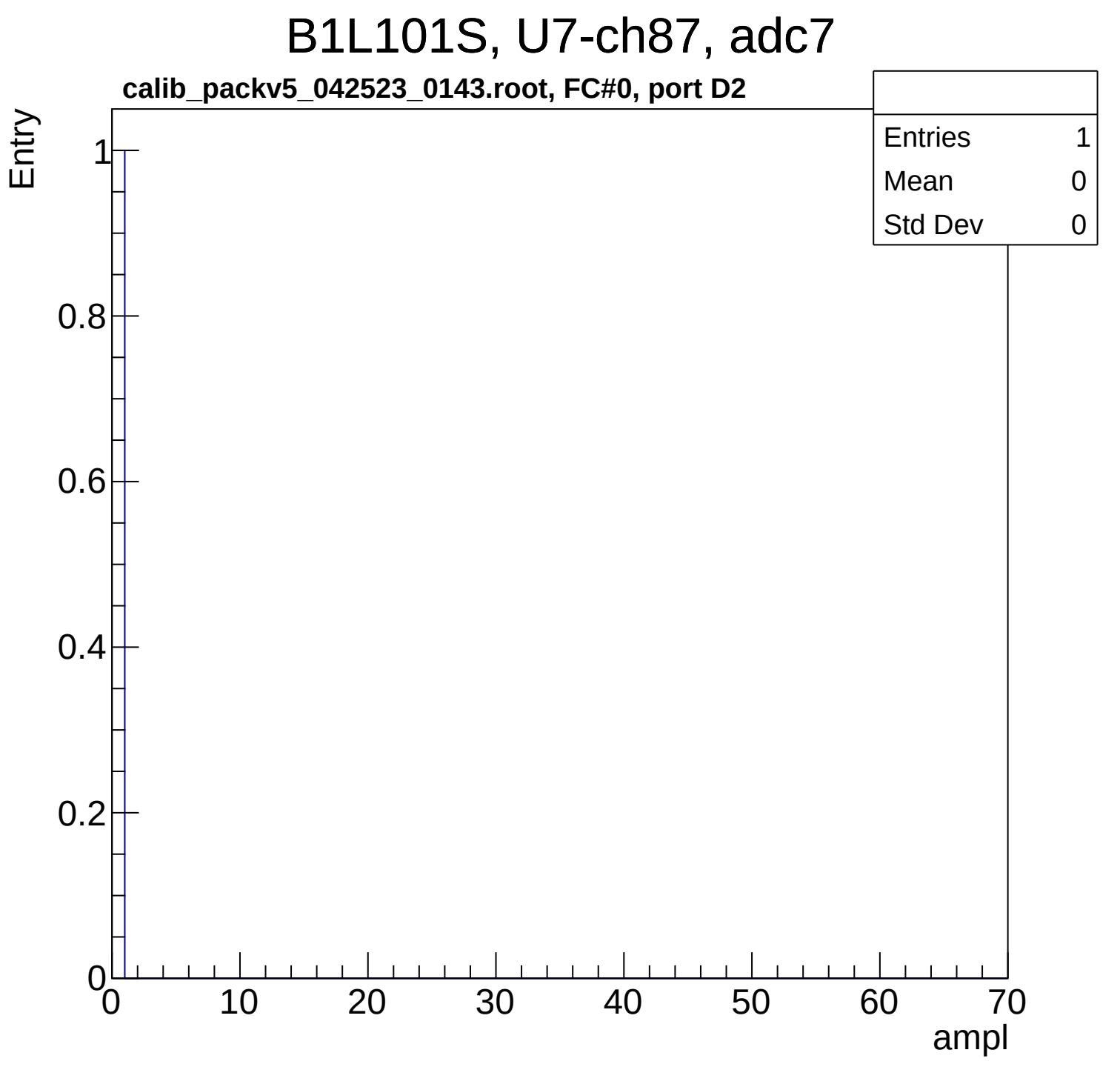
B1L101S, U7-ch87, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
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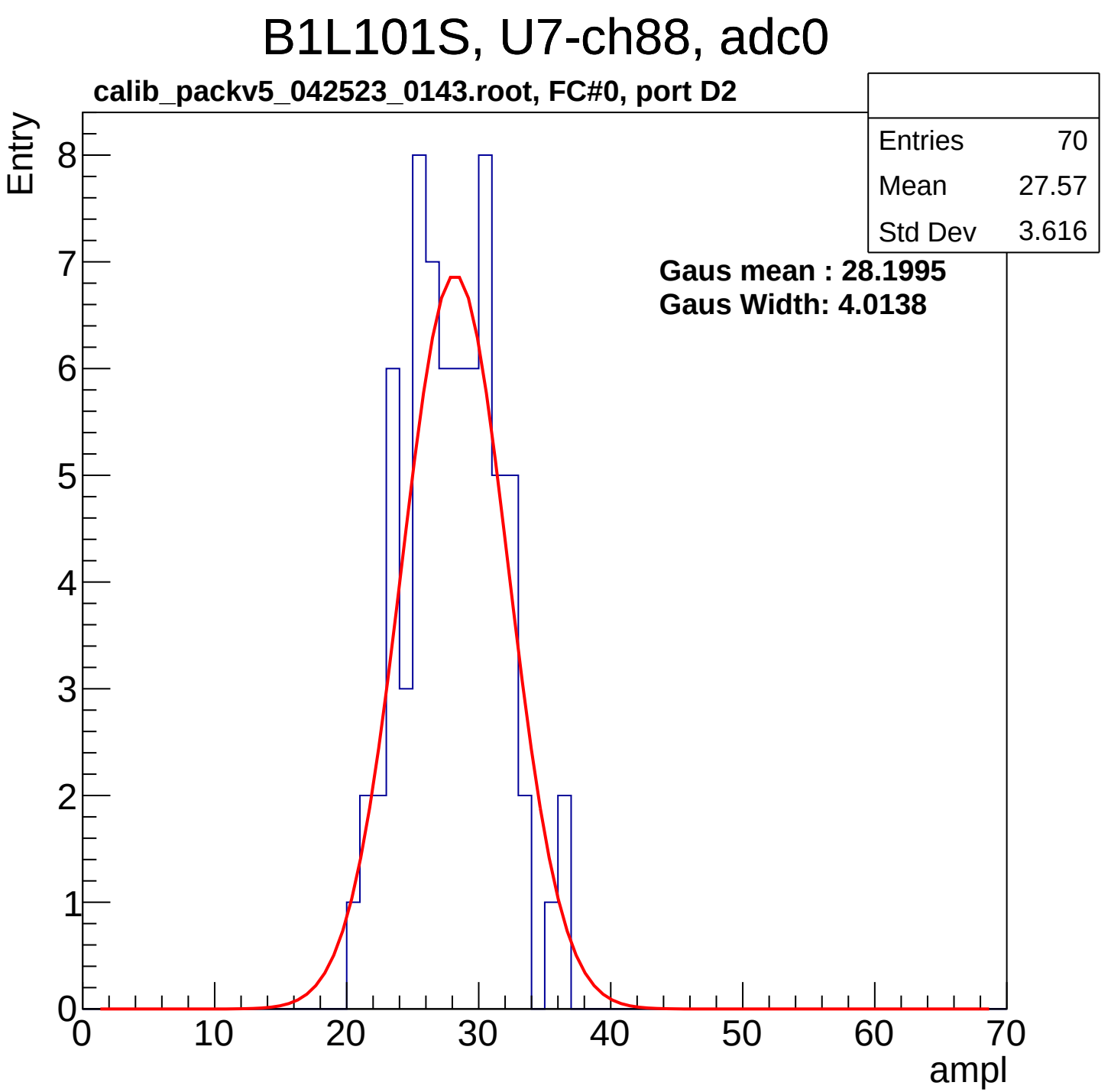
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch88, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 27.57
Std Dev 3.616
Gaus mean : 28.1995
Gaus Width: 4.0138
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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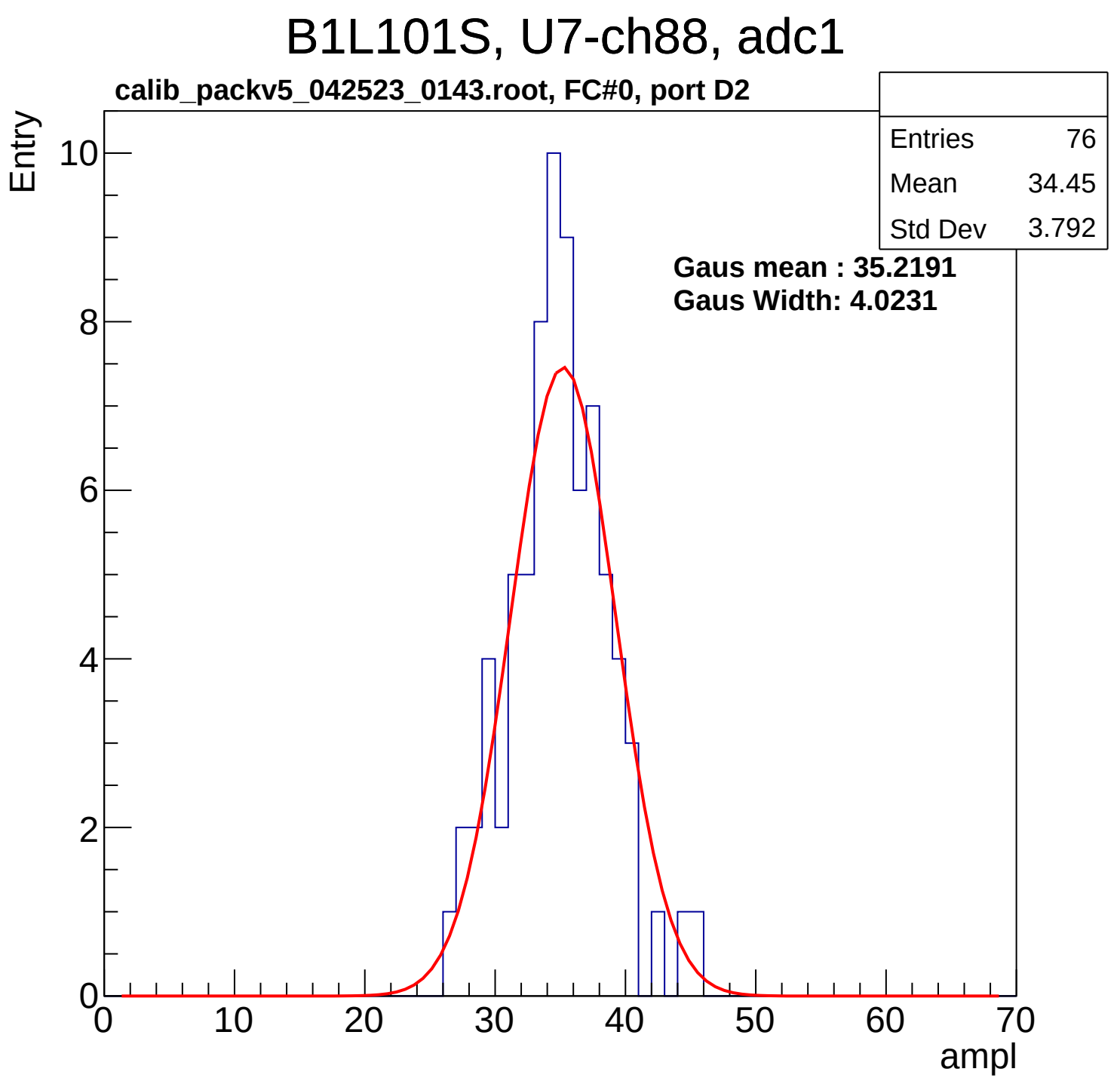
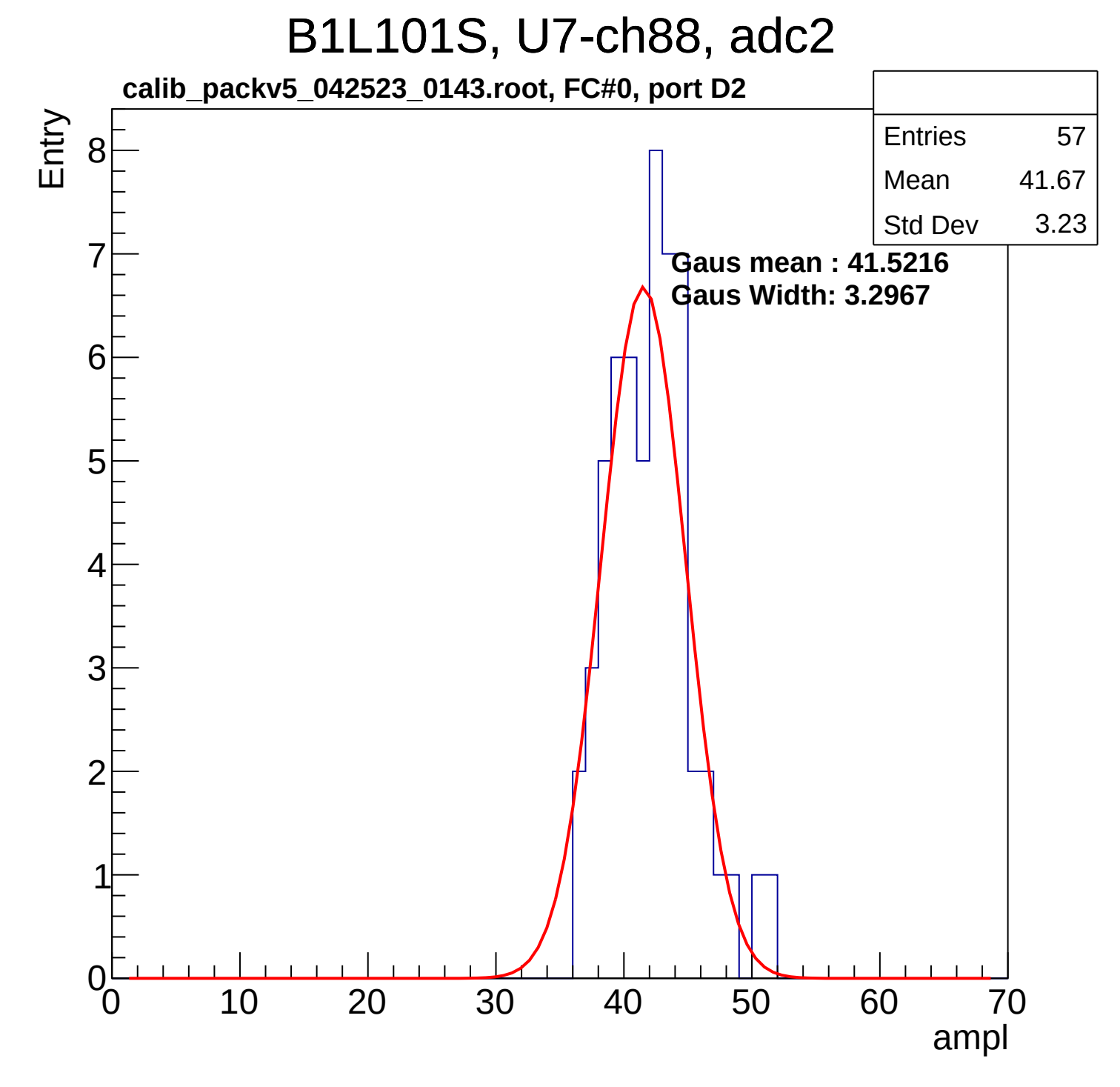
40
50
60
70


B1L101S, U7-ch88, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 34.45
Std Dev 3.792
Gaus mean : 35.2191
Gaus Width: 4.0231
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch88, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 41.67
Std Dev 3.23
Gaus mean : 41.5216
Gaus Width: 3.2967
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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60
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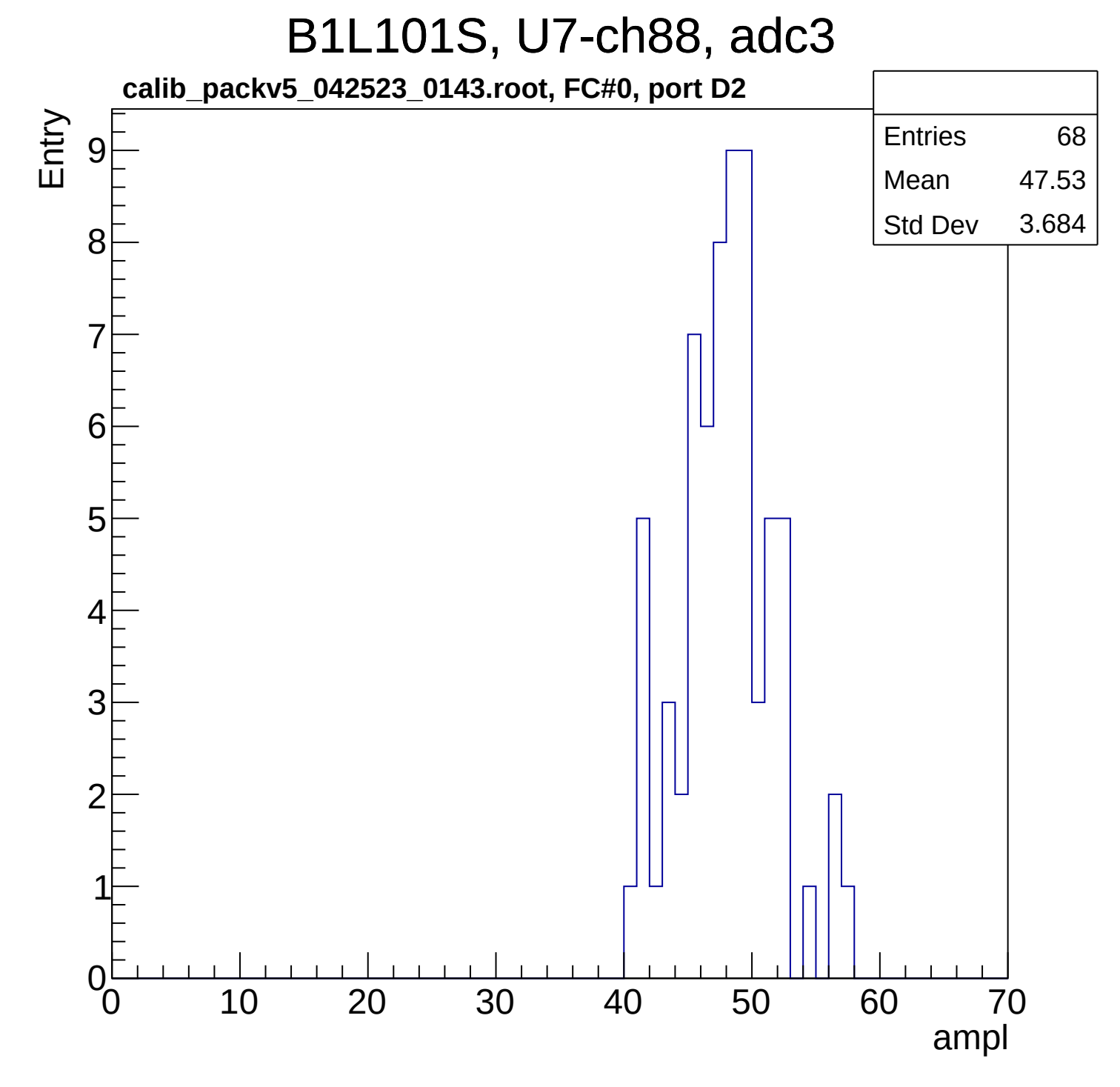
B1L101S, U7-ch88, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 47.53
Std Dev 3.684
Entry
ampl
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2
3
4
5
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7
8
9
0
10
20
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40
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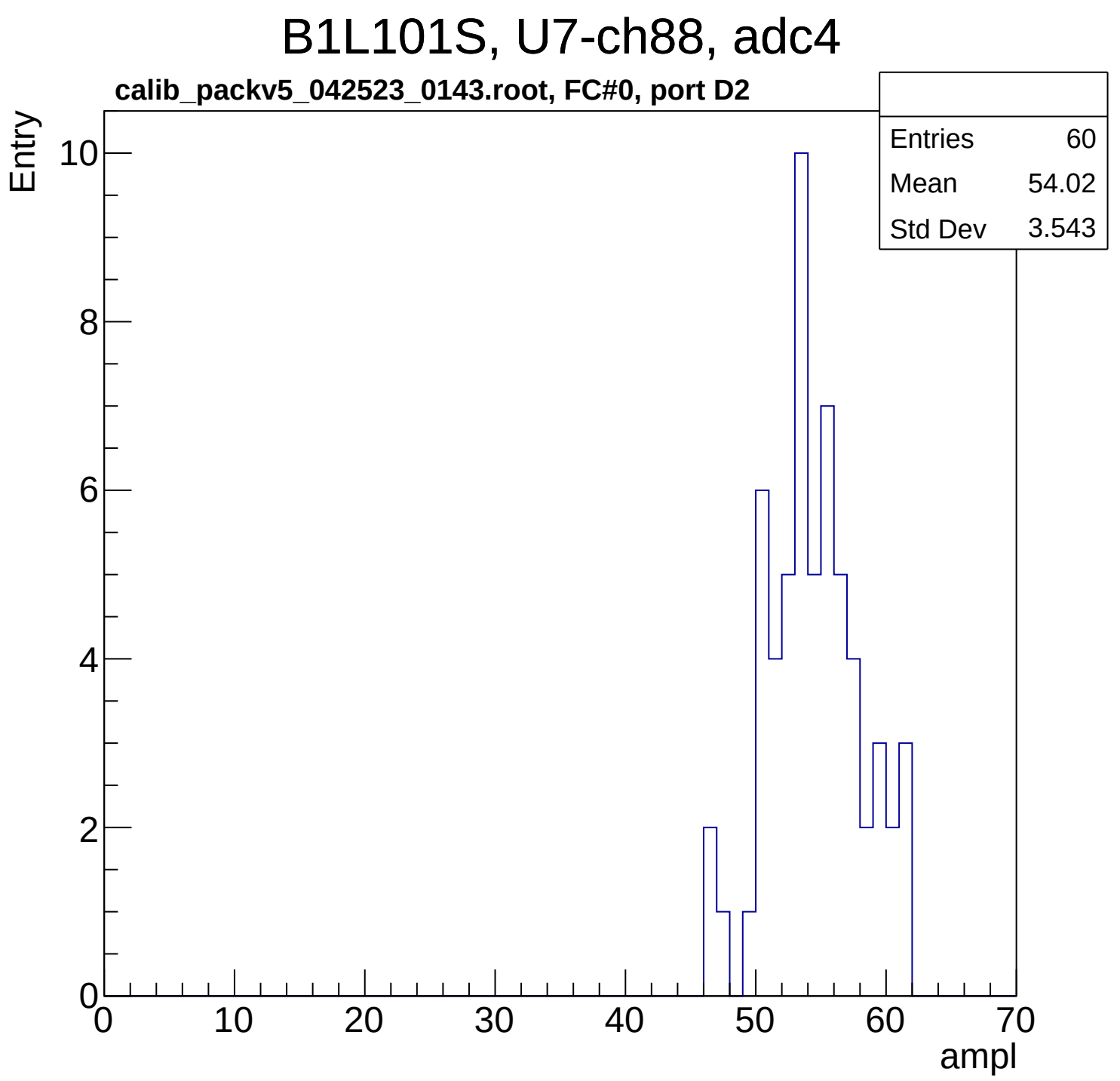
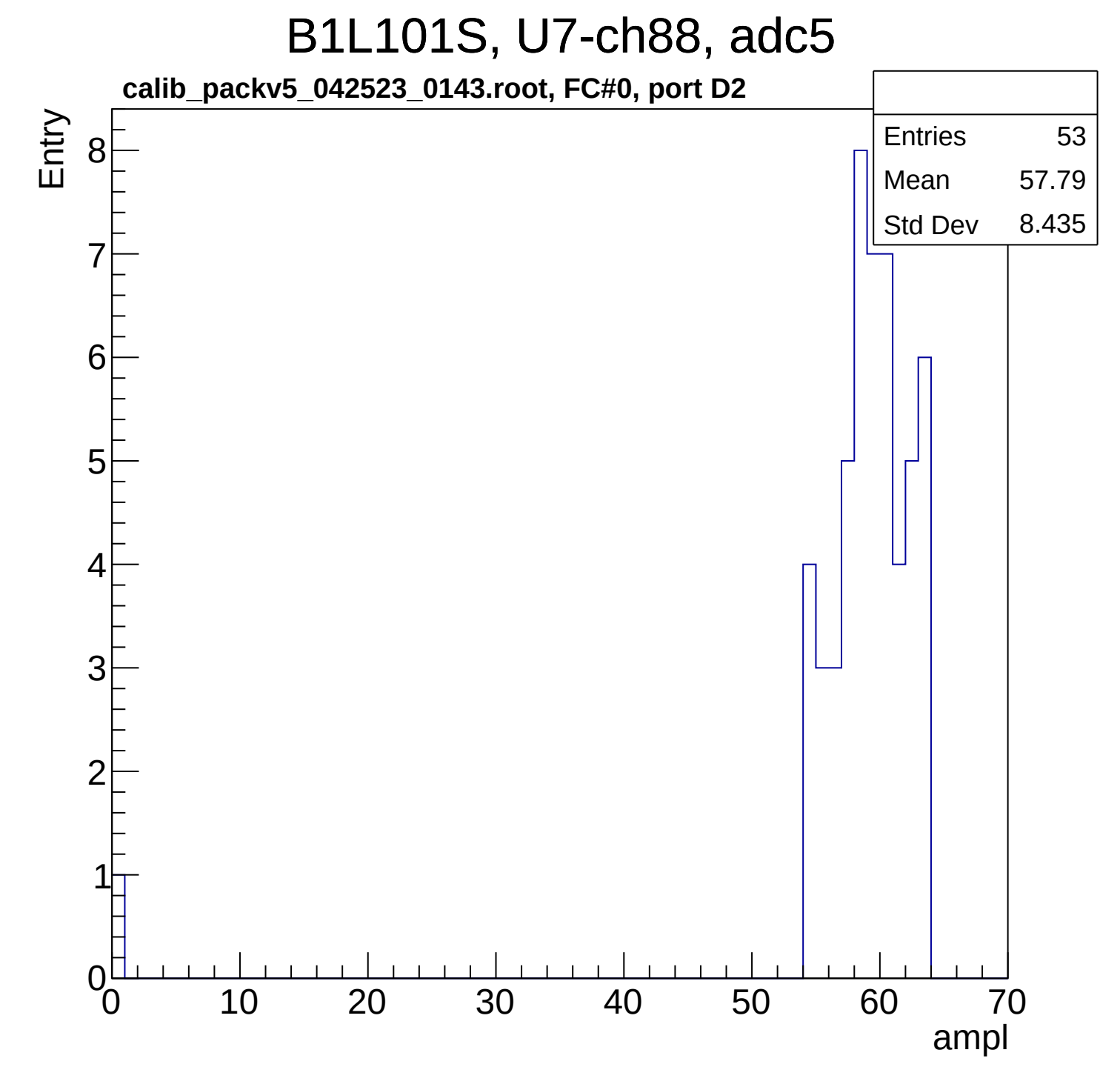

B1L101S, U7-ch88, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 54.02
Std Dev 3.543
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch88, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 57.79
Std Dev 8.435
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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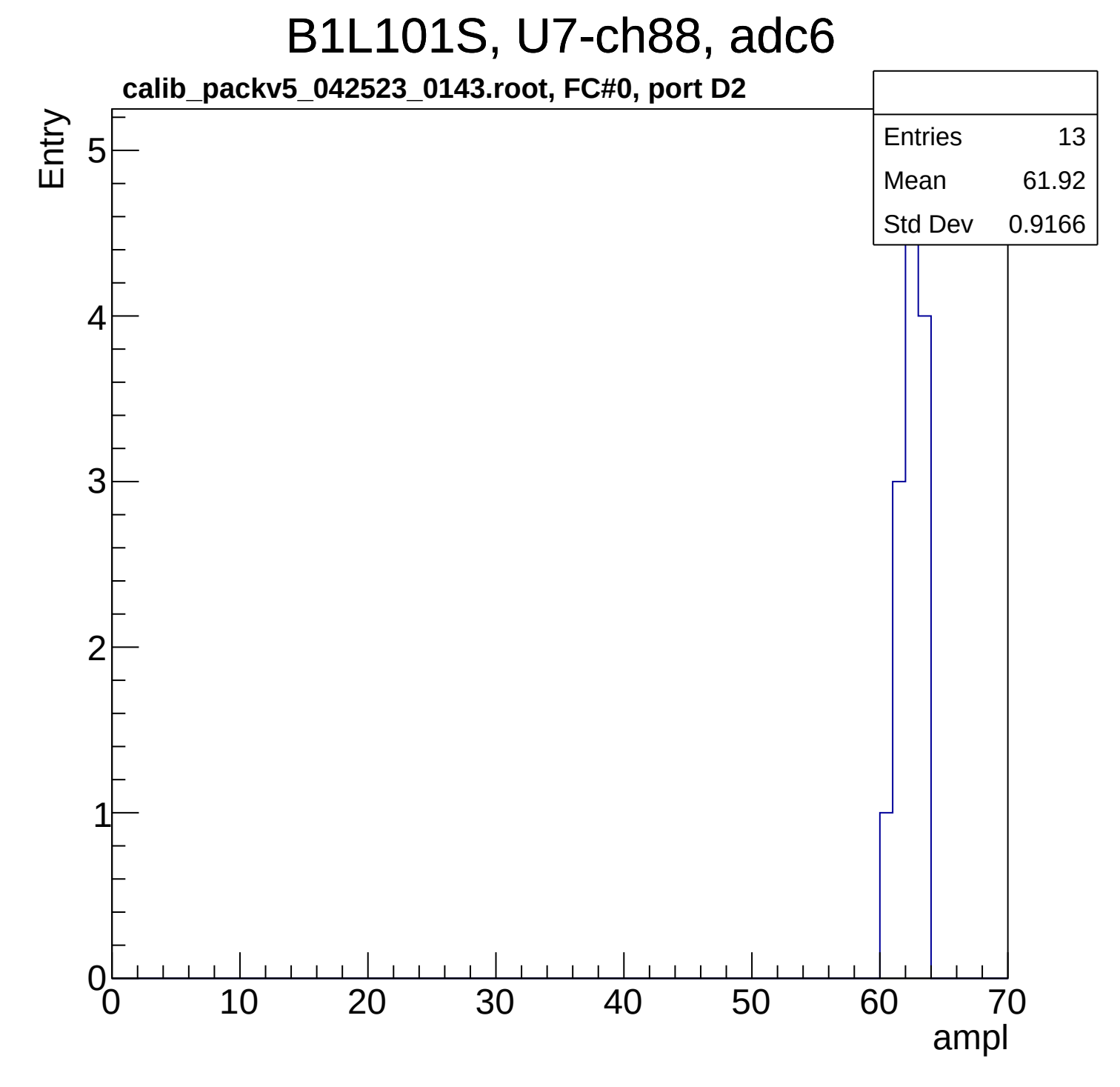
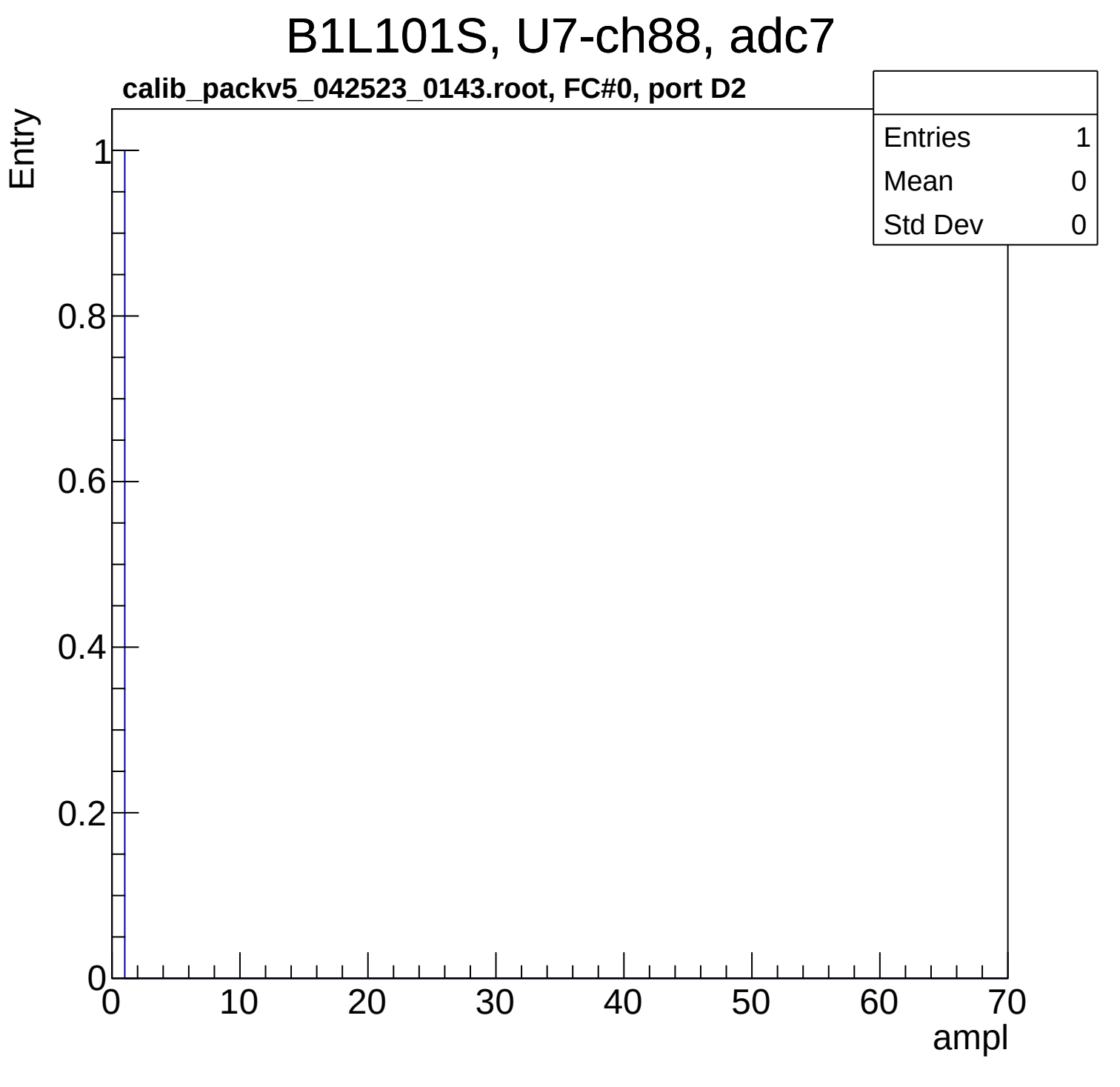
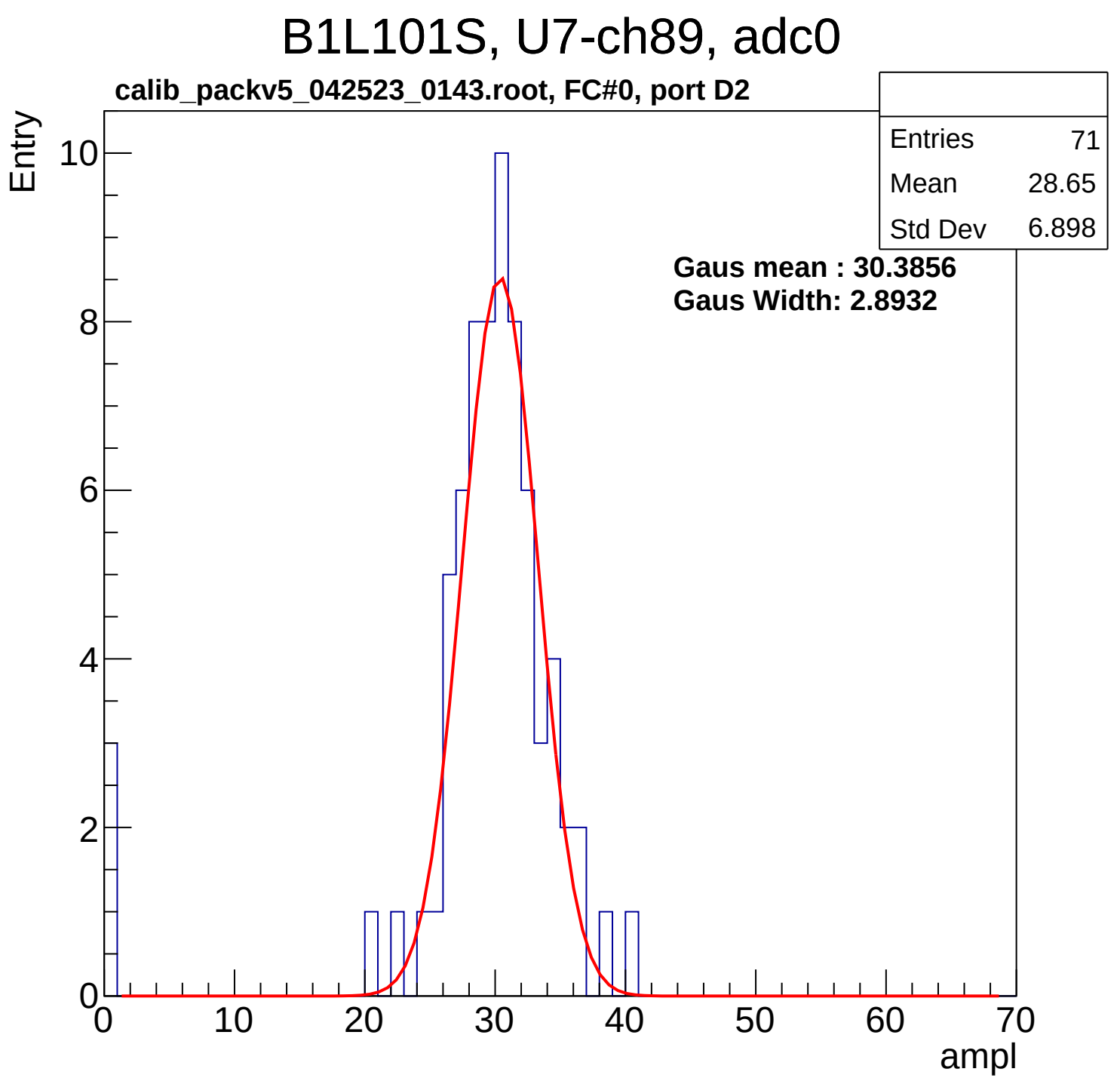
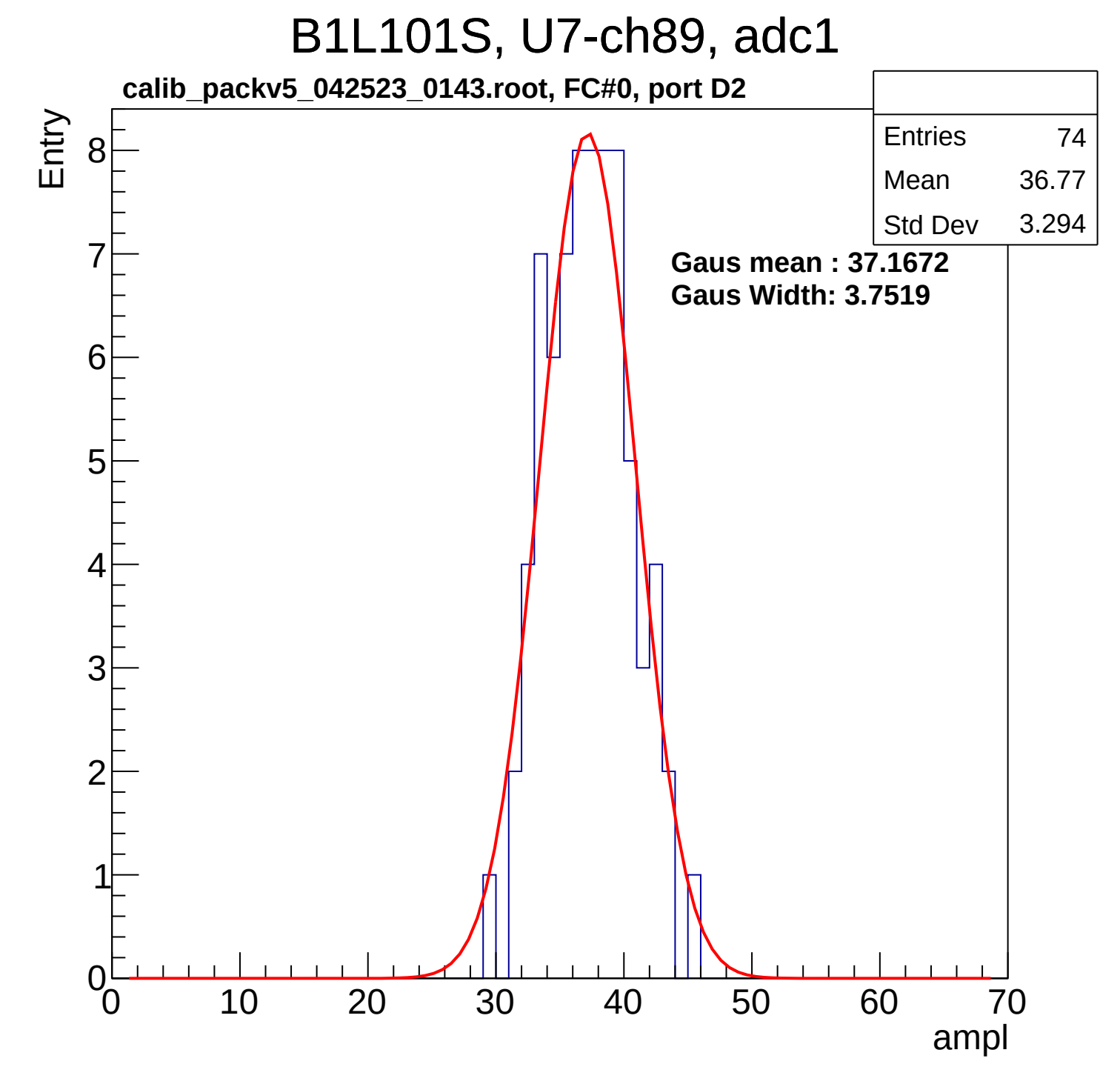
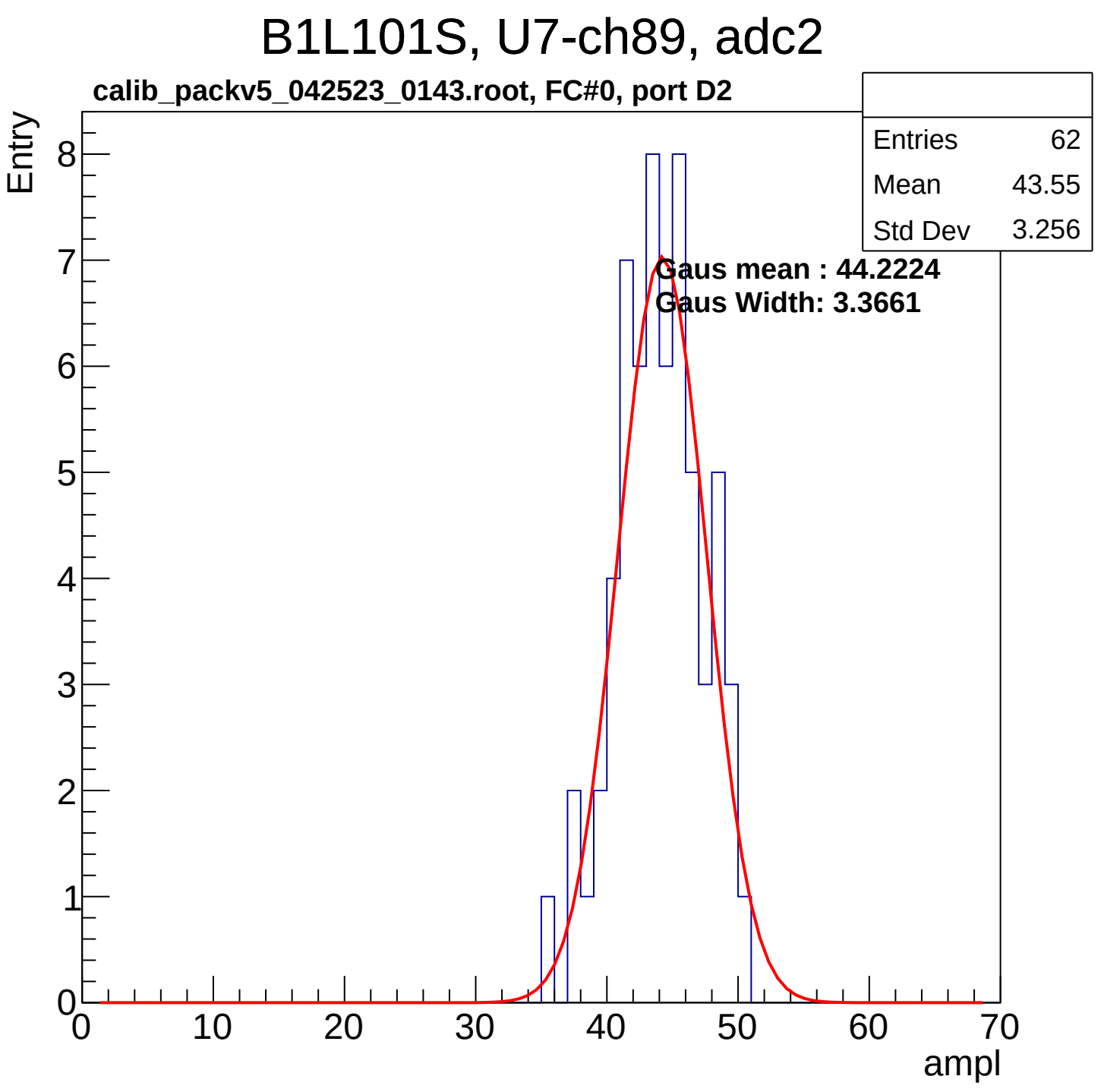
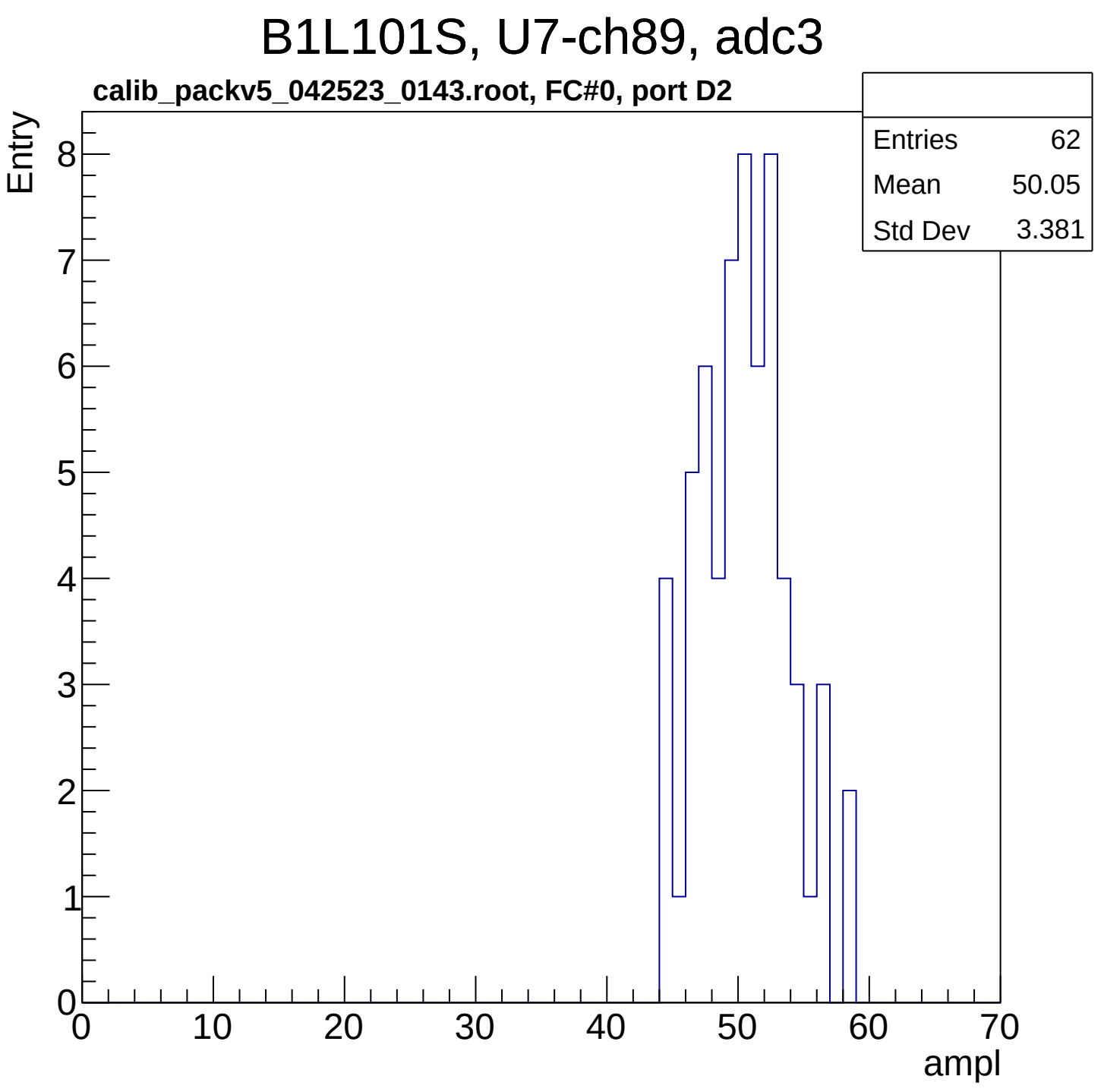

B1L101S, U7-ch88, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 13
Mean 61.92
Std Dev 0.9166
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

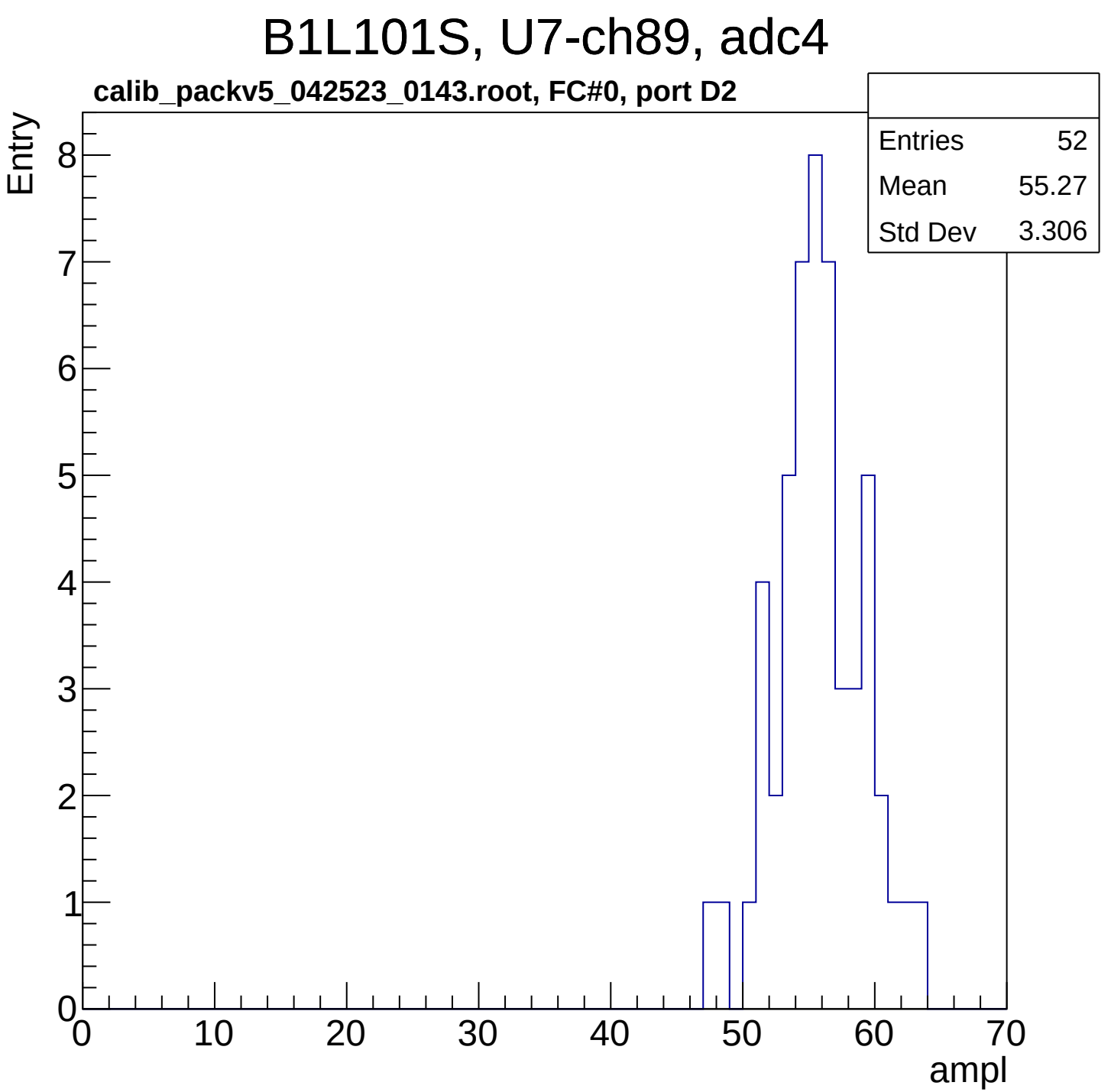

B1L101S, U7-ch88, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

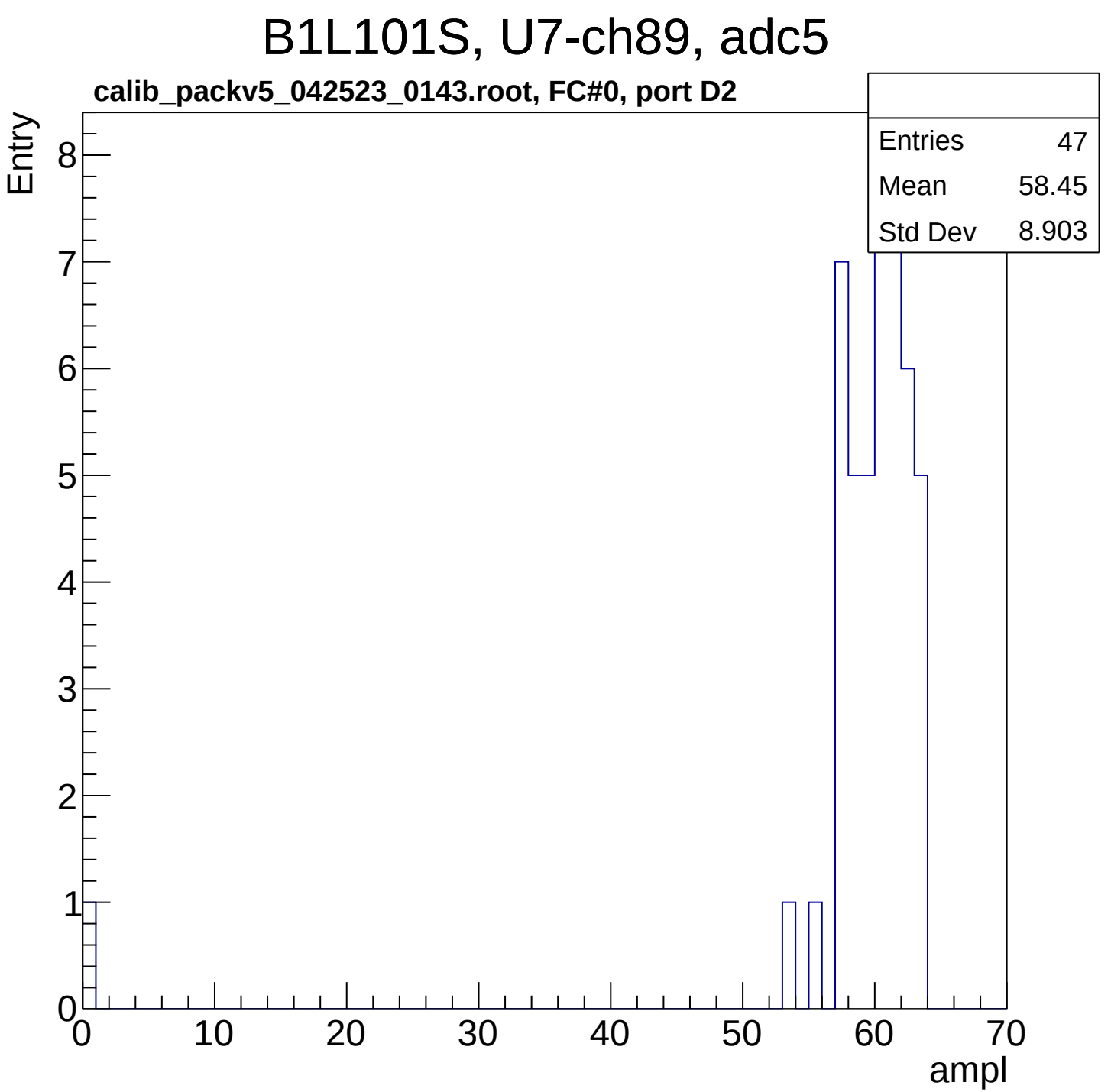

B1L101S, U7-ch89, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 28.65
Std Dev 6.898
Gaus mean : 30.3856
Gaus Width: 2.8932
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

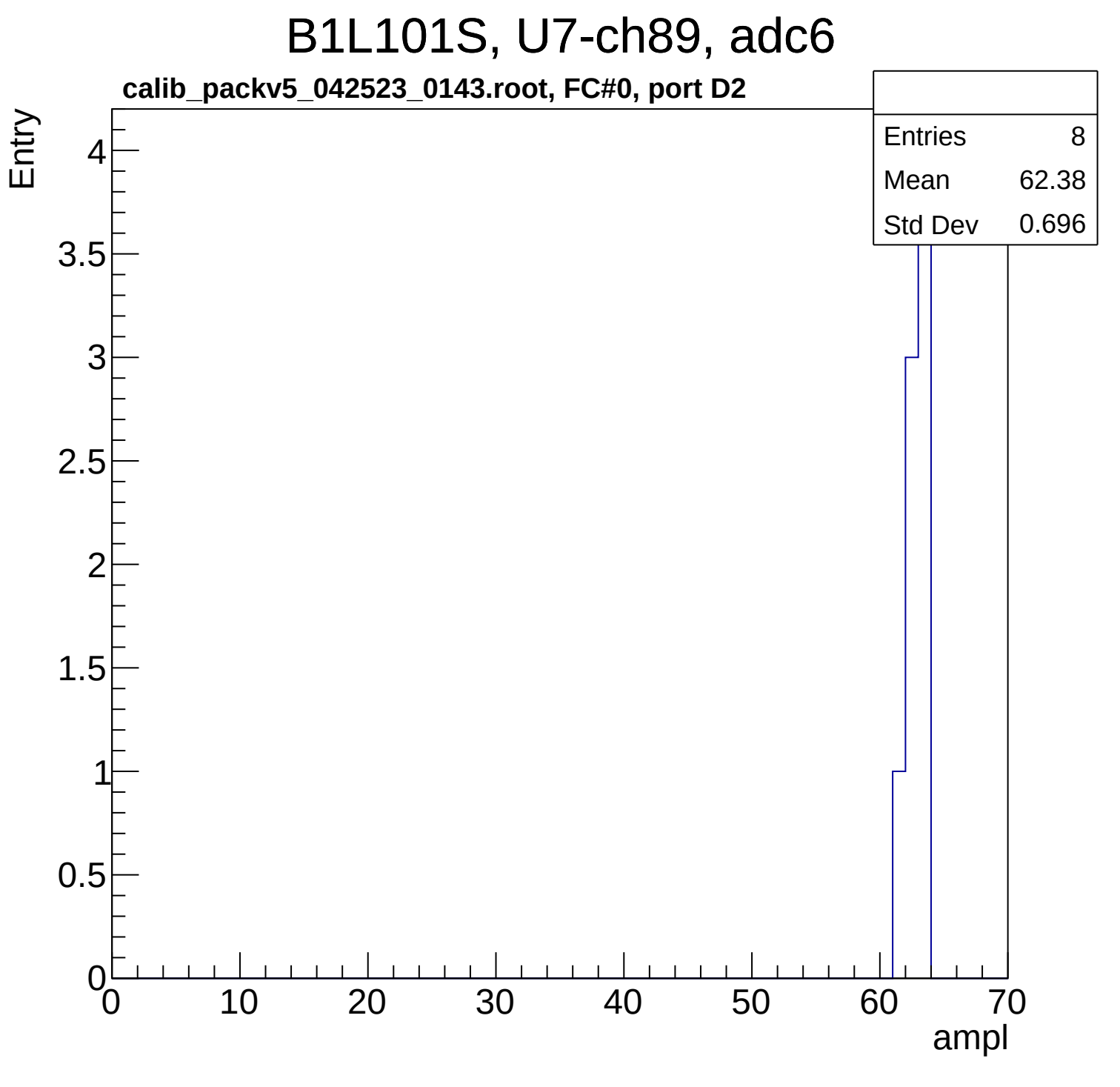

B1L101S, U7-ch89, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 36.77
Std Dev 3.294
Gaus mean : 37.1672
Gaus Width: 3.7519
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

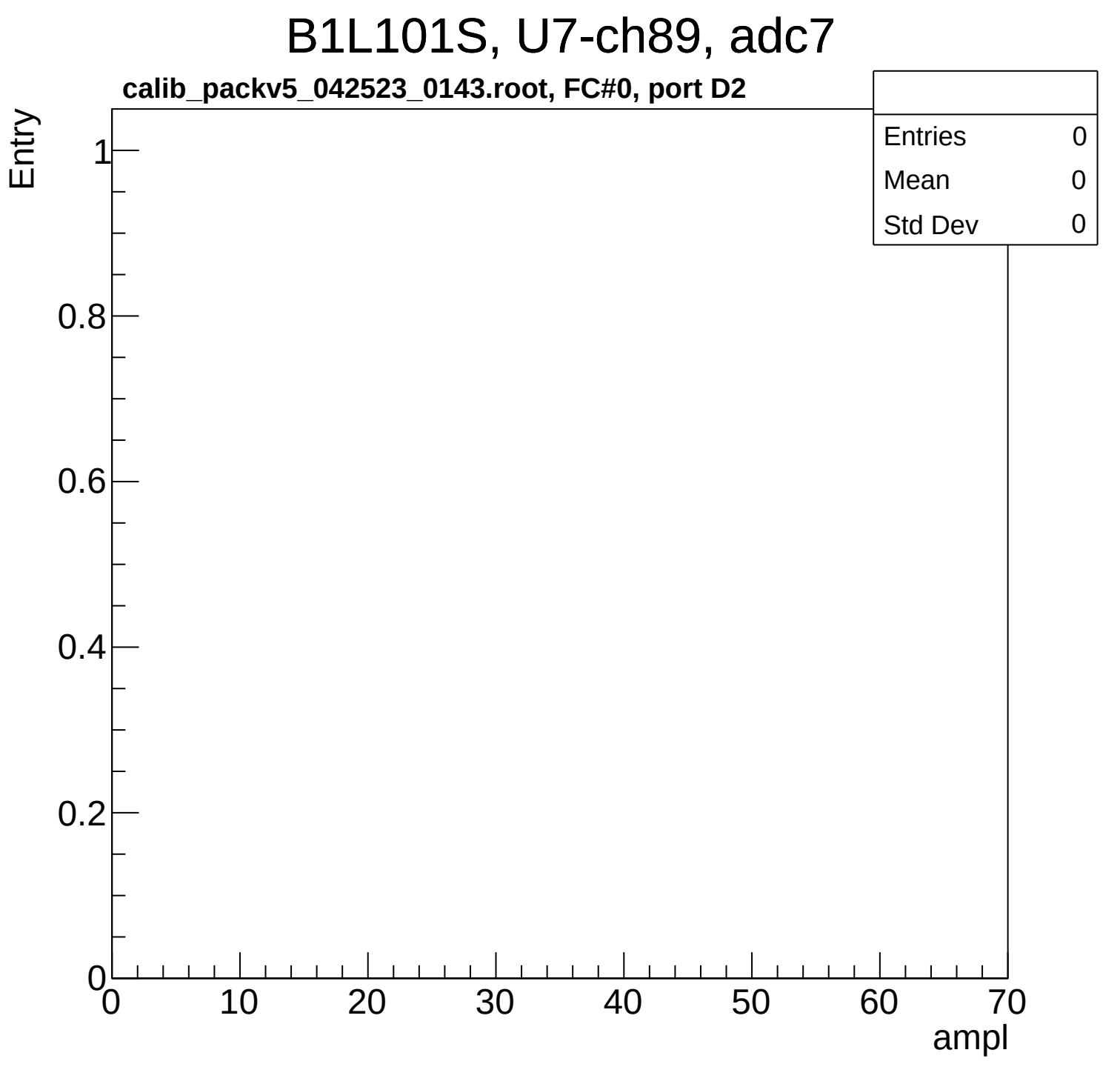

B1L101S, U7-ch89, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 43.55
Std Dev 3.256
Gaus mean : 44.2224
Gaus Width: 3.3661
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

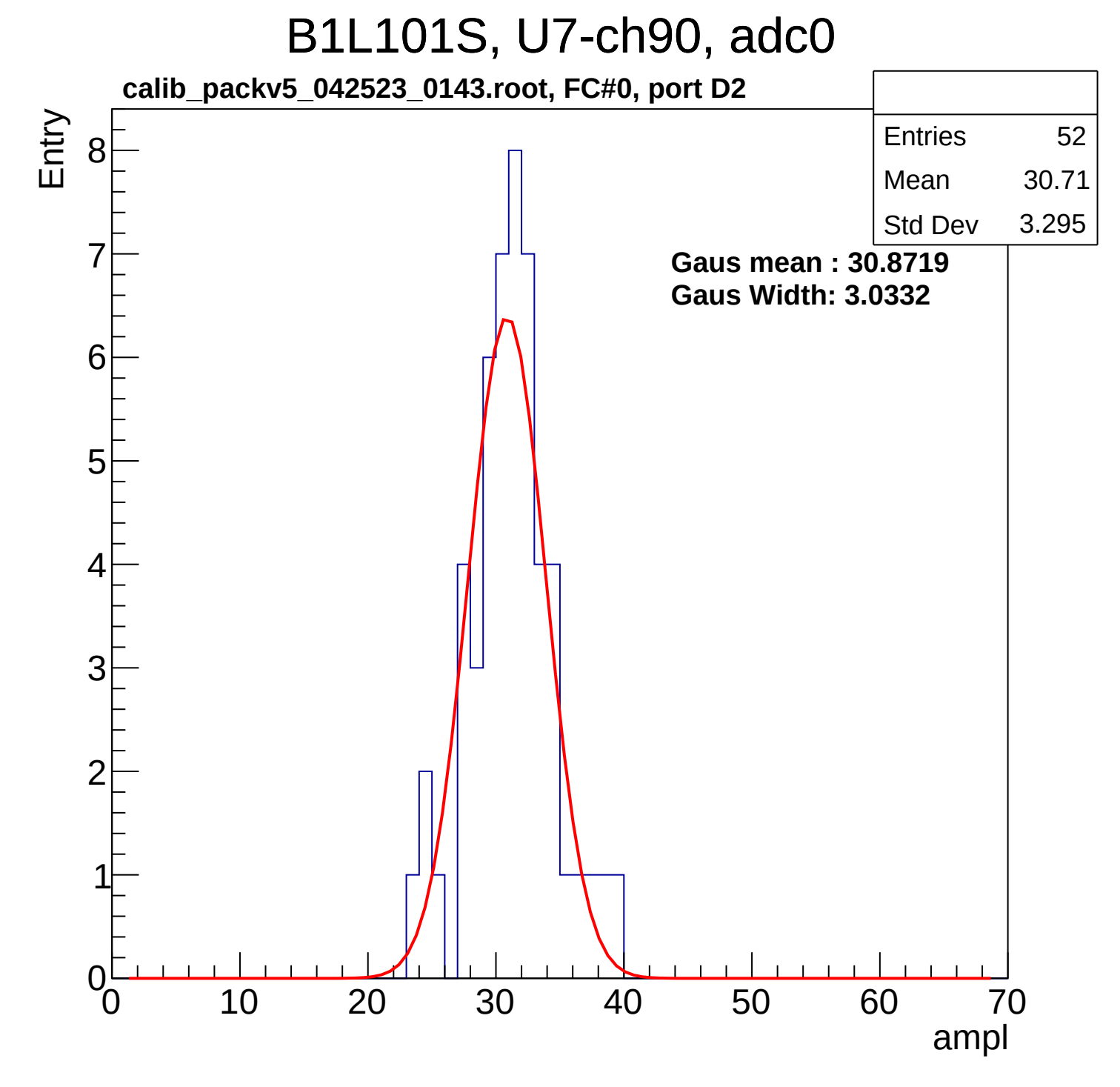

B1L101S, U7-ch89, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 50.05
Std Dev 3.381
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

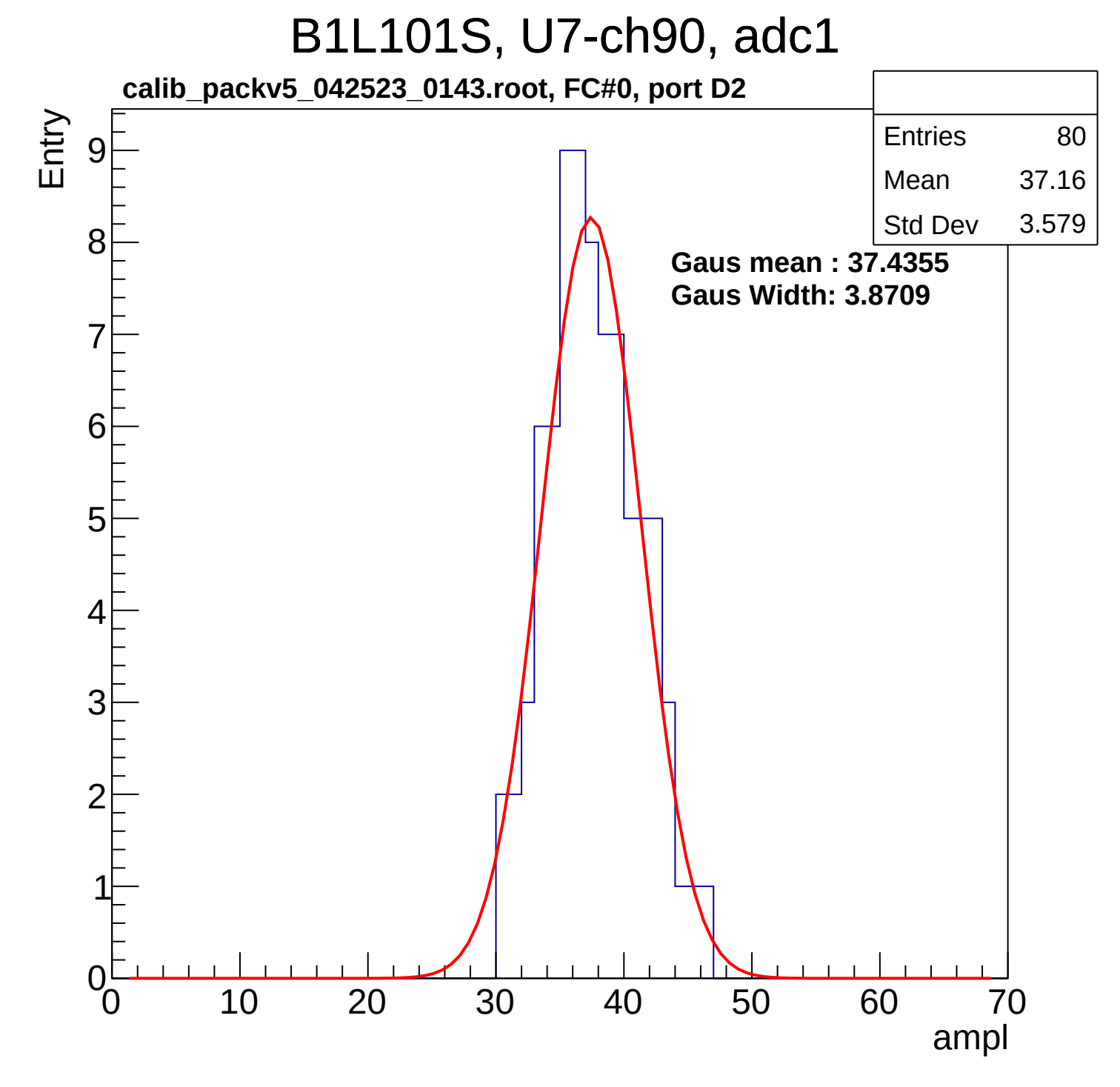

B1L101S, U7-ch89, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 55.27
Std Dev 3.306
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

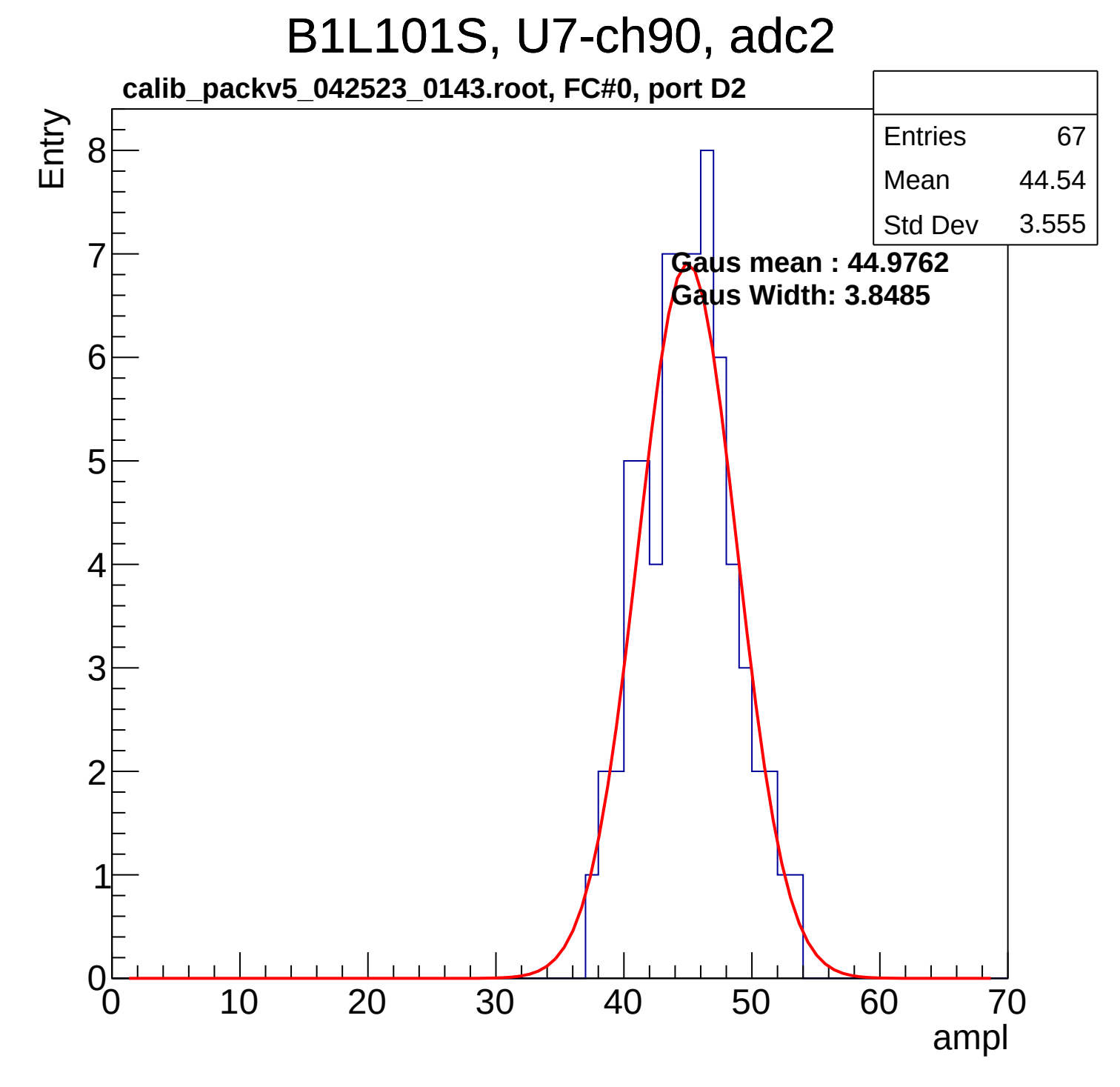

B1L101S, U7-ch89, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 58.45
Std Dev 8.903
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

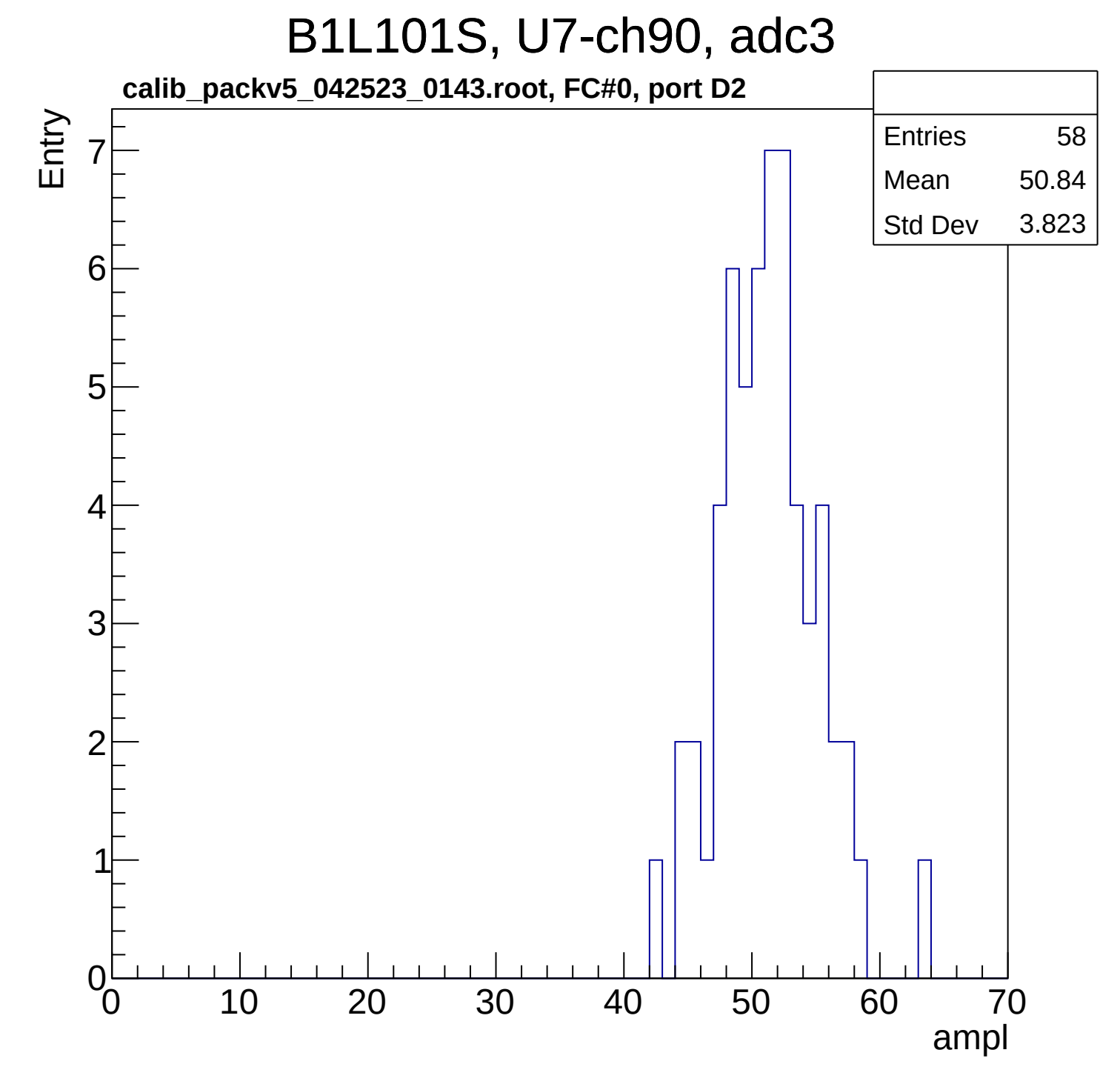

B1L101S, U7-ch89, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 62.38
Std Dev 0.696
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

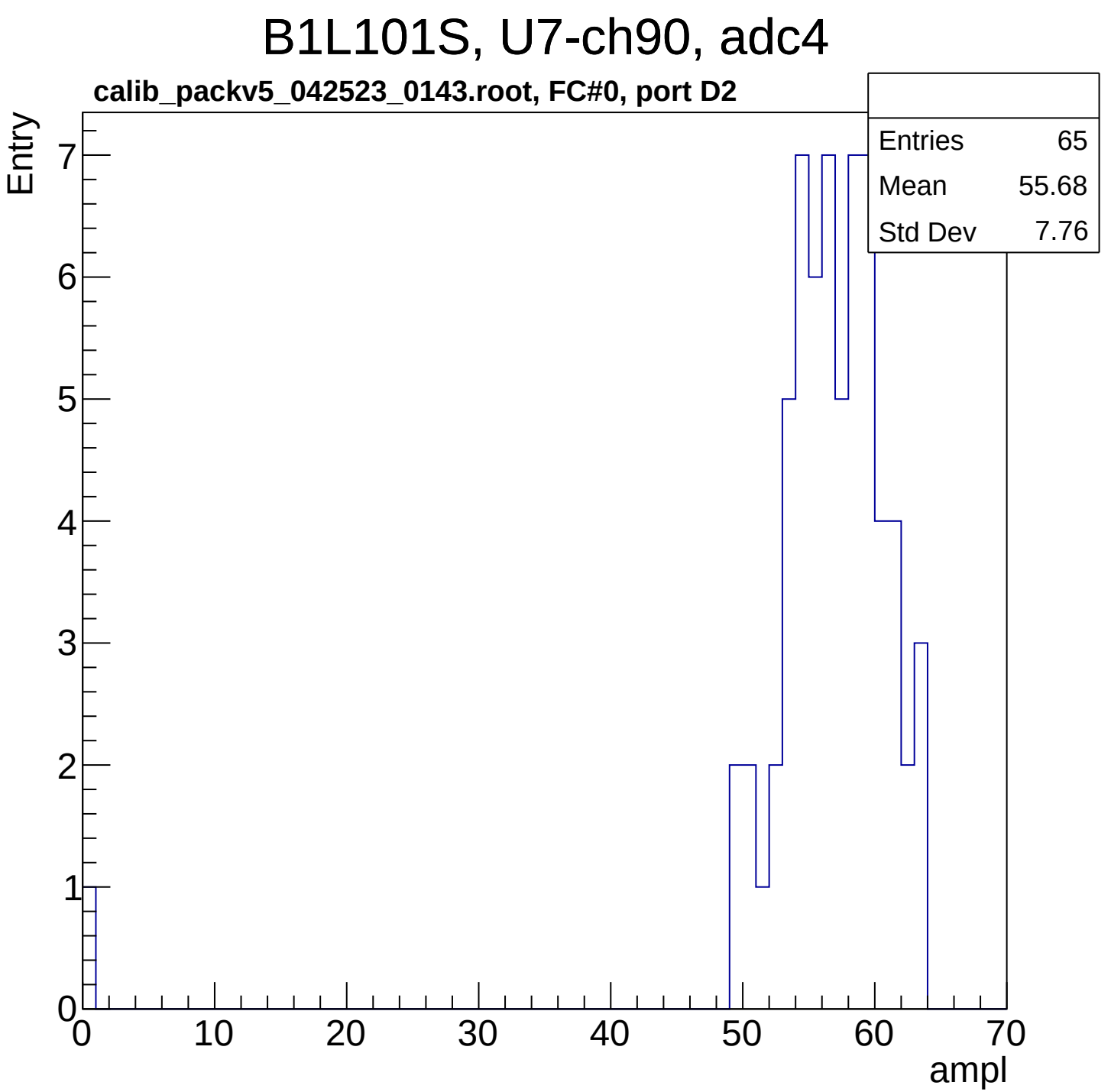

B1L101S, U7-ch89, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

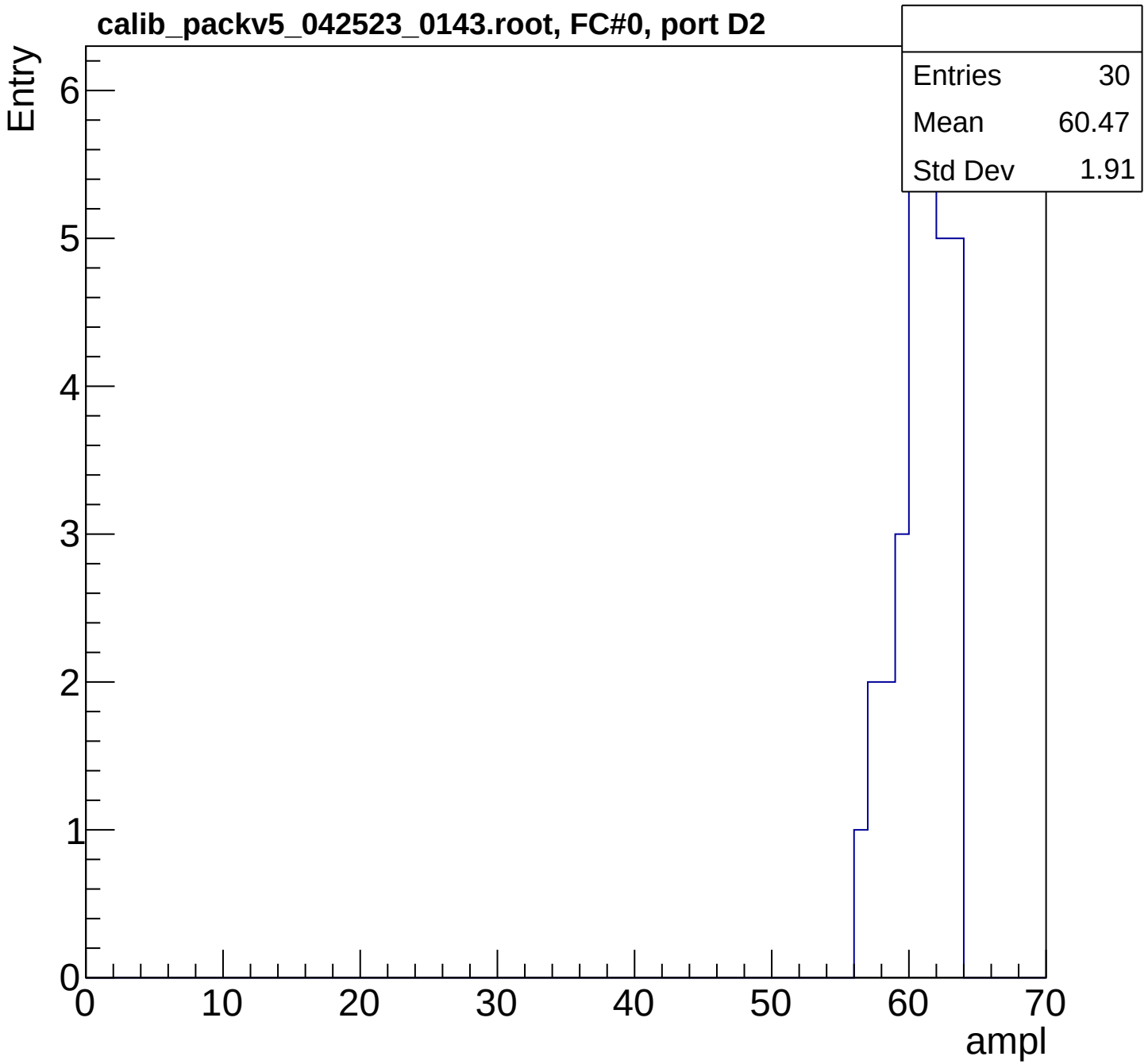

B1L101S, U7-ch90, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 30.71
Std Dev 3.295
Gaus mean : 30.8719
Gaus Width: 3.0332
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

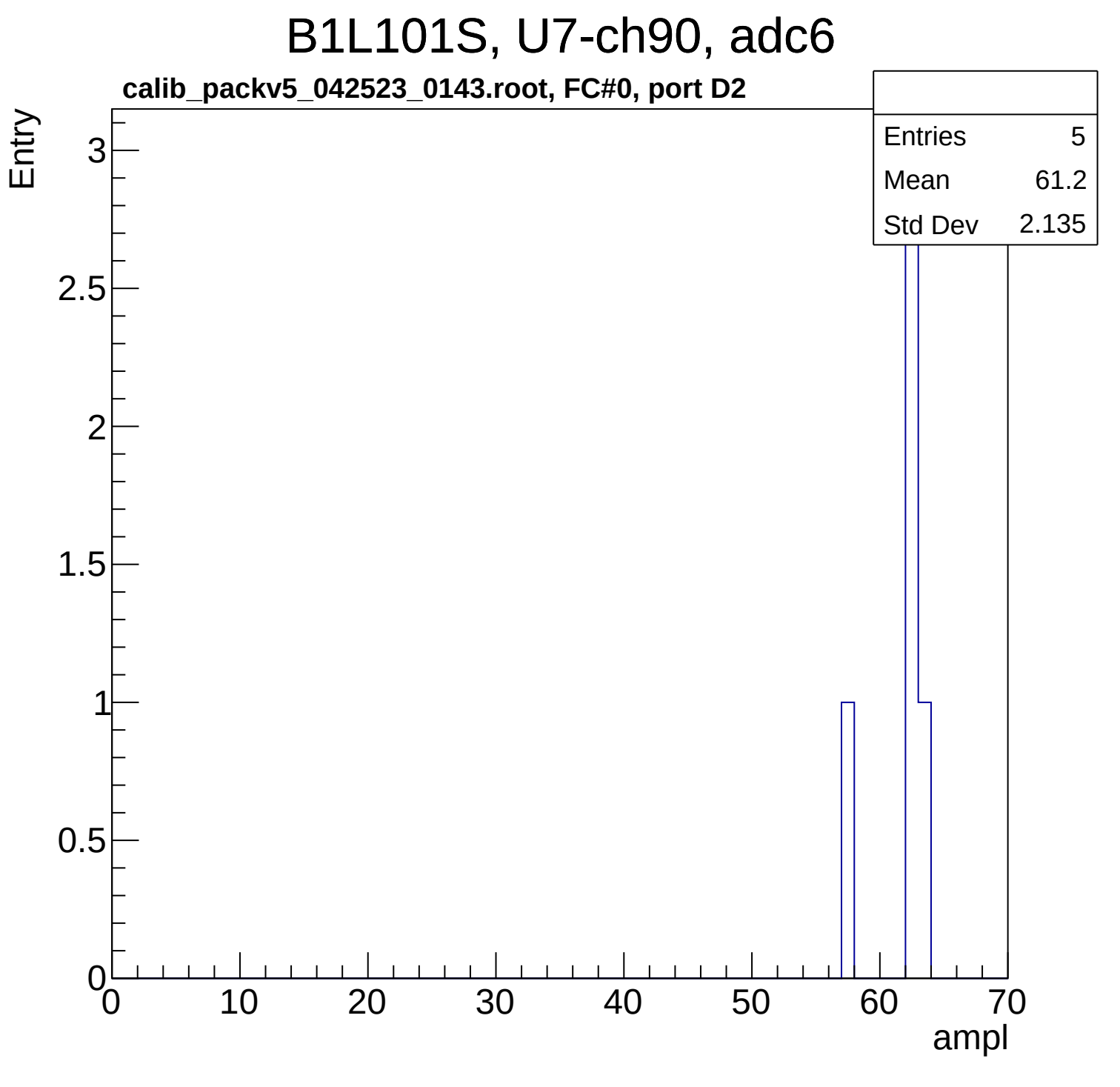

B1L101S, U7-ch90, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 80
Mean 37.16
Std Dev 3.579
Gaus mean : 37.4355
Gaus Width: 3.8709
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

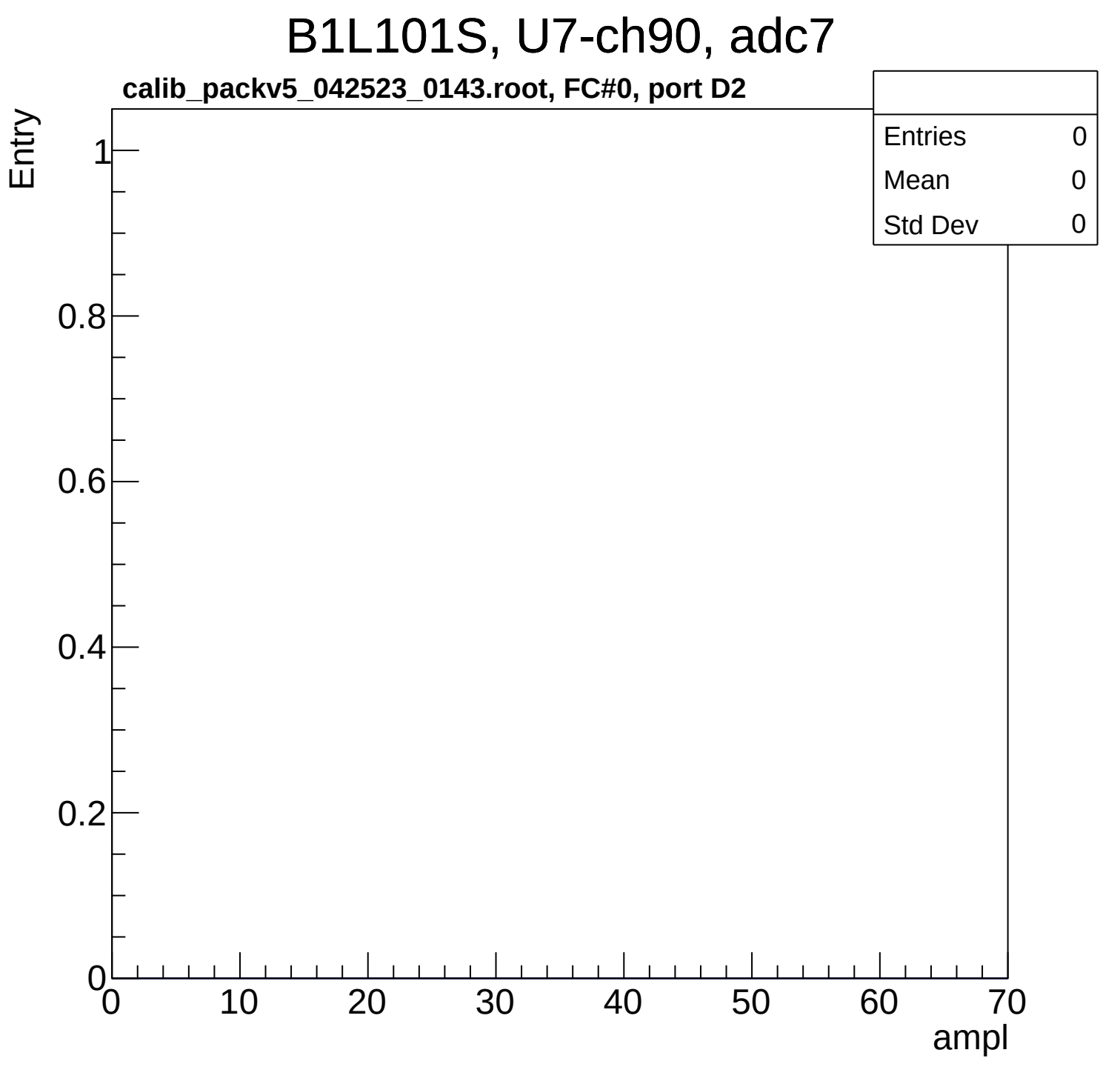

B1L101S, U7-ch90, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 44.54
Std Dev 3.555
Gaus mean : 44.9762
Gaus Width: 3.8485
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

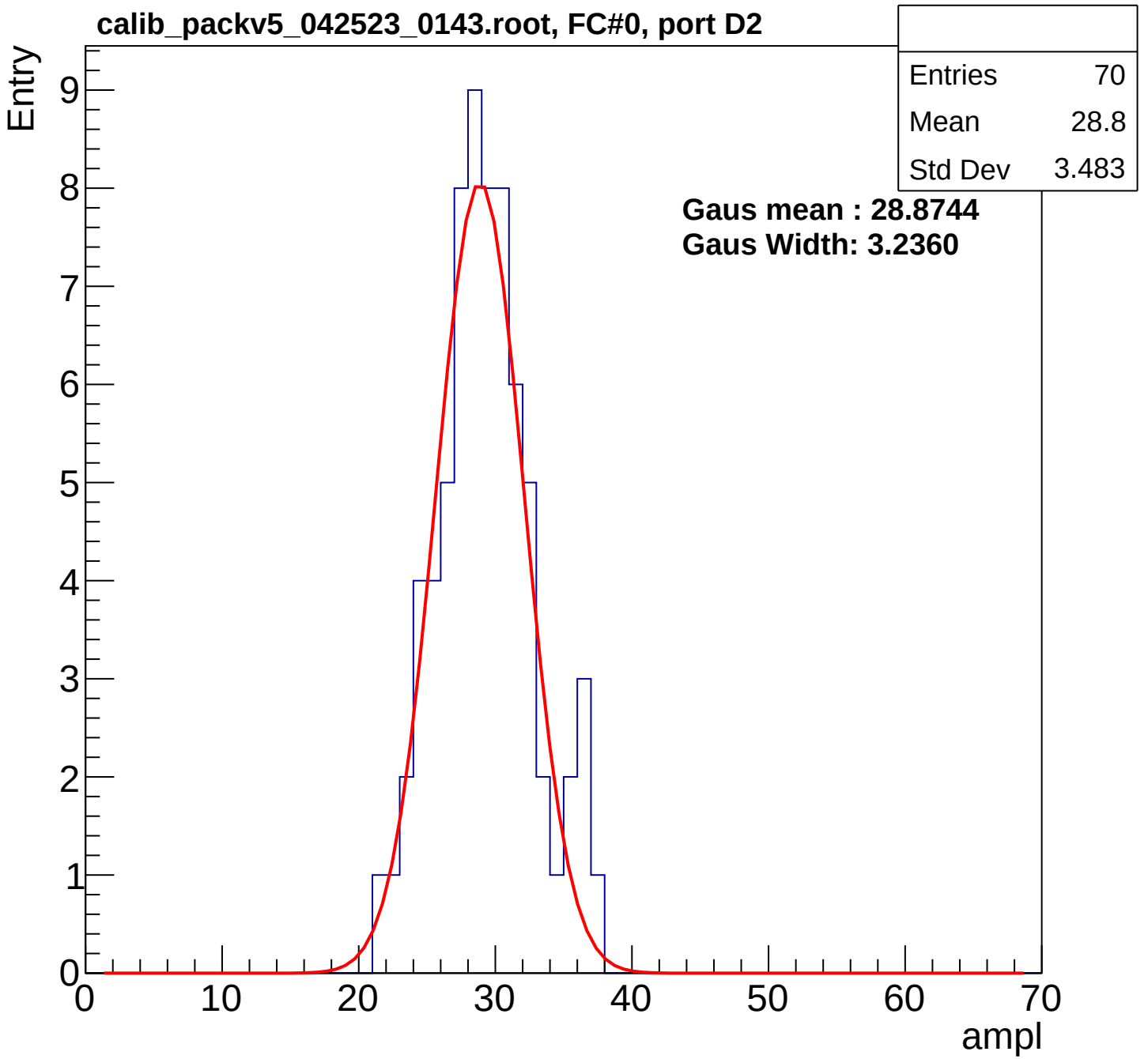

B1L101S, U7-ch90, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 50.84
Std Dev 3.823
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

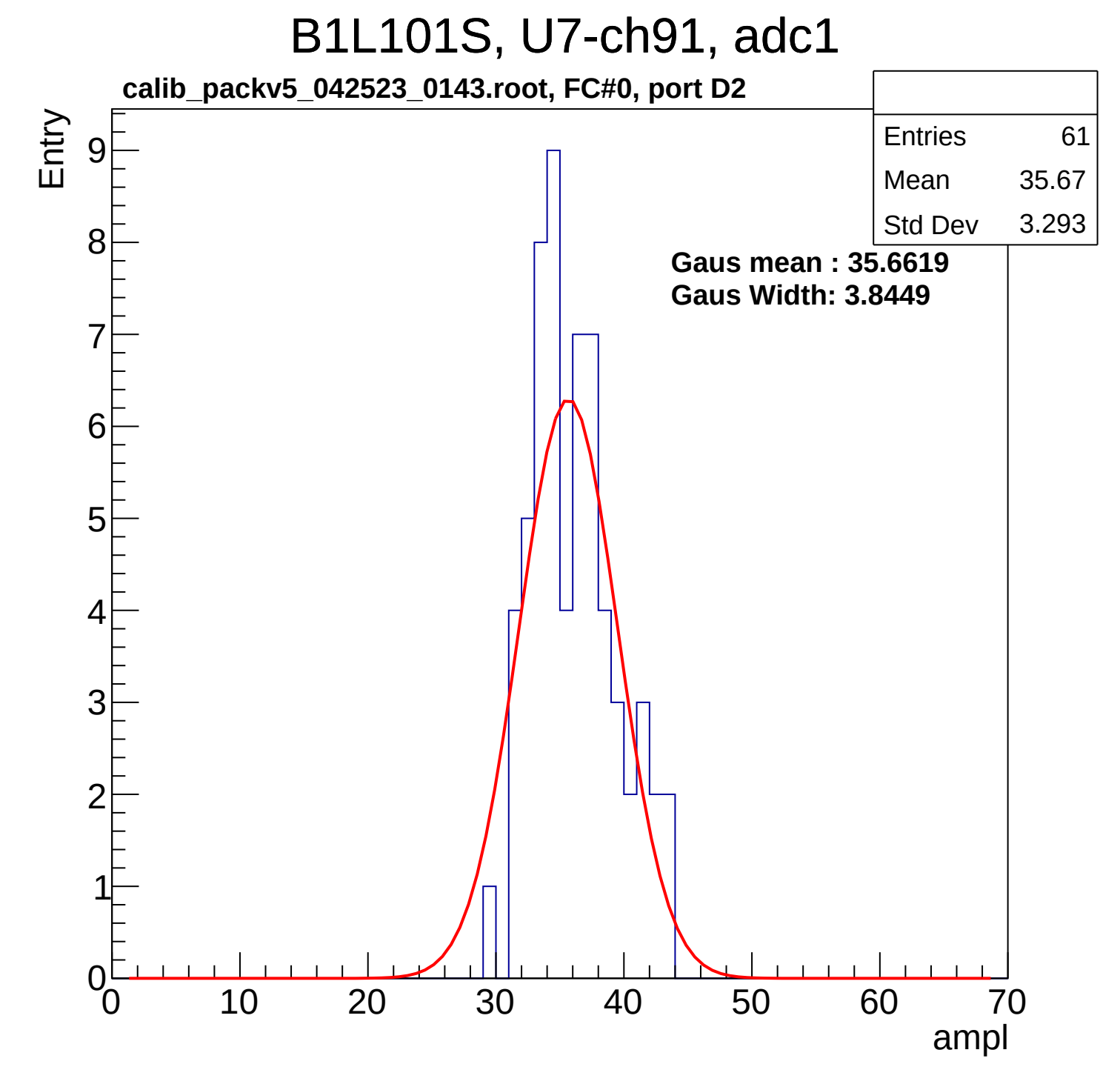

B1L101S, U7-ch90, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 55.68
Std Dev 7.76
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

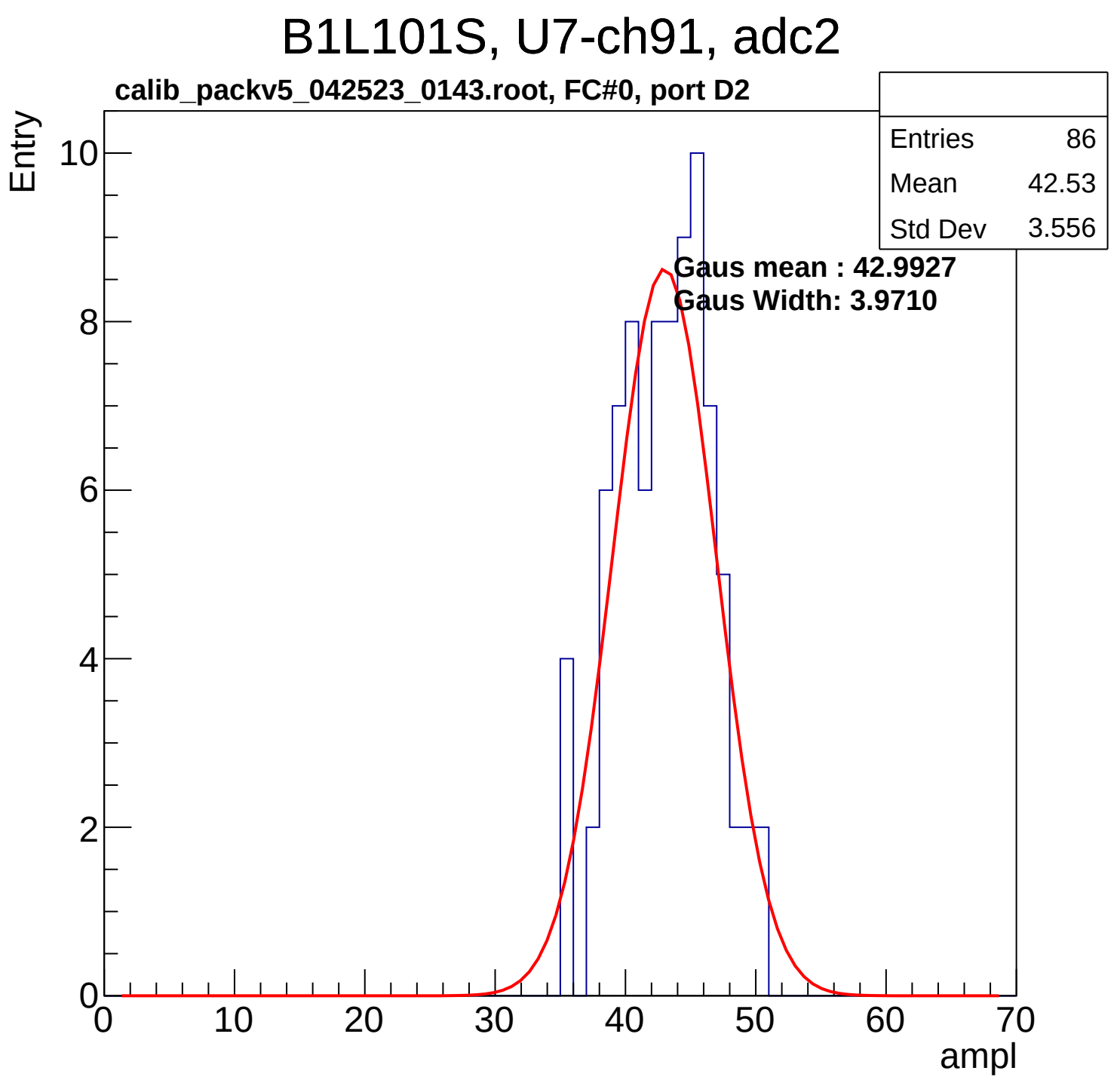

B1L101S, U7-ch90, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 30
Mean 60.47
Std Dev 1.91
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

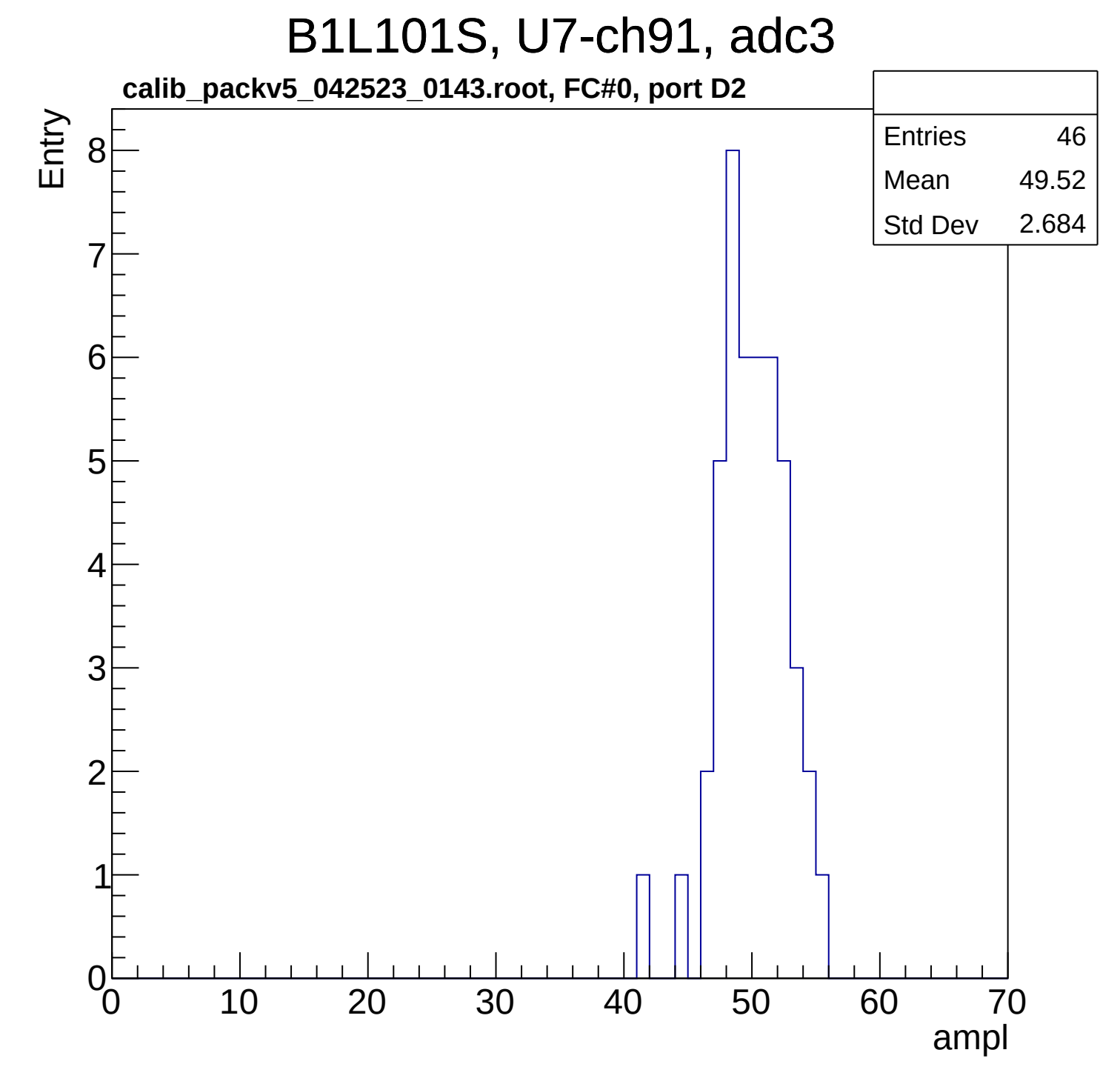

B1L101S, U7-ch90, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 61.2
Std Dev 2.135
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U7-ch90, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch91, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 28.8
Std Dev 3.483
Gaus mean : 28.8744
Gaus Width: 3.2360
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch91, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 35.67
Std Dev 3.293
Gaus mean : 35.6619
Gaus Width: 3.8449
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch91, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 86
Mean 42.53
Std Dev 3.556
Gaus mean : 42.9927
Gaus Width: 3.9710
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch91, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 49.52
Std Dev 2.684
Entry
ampl
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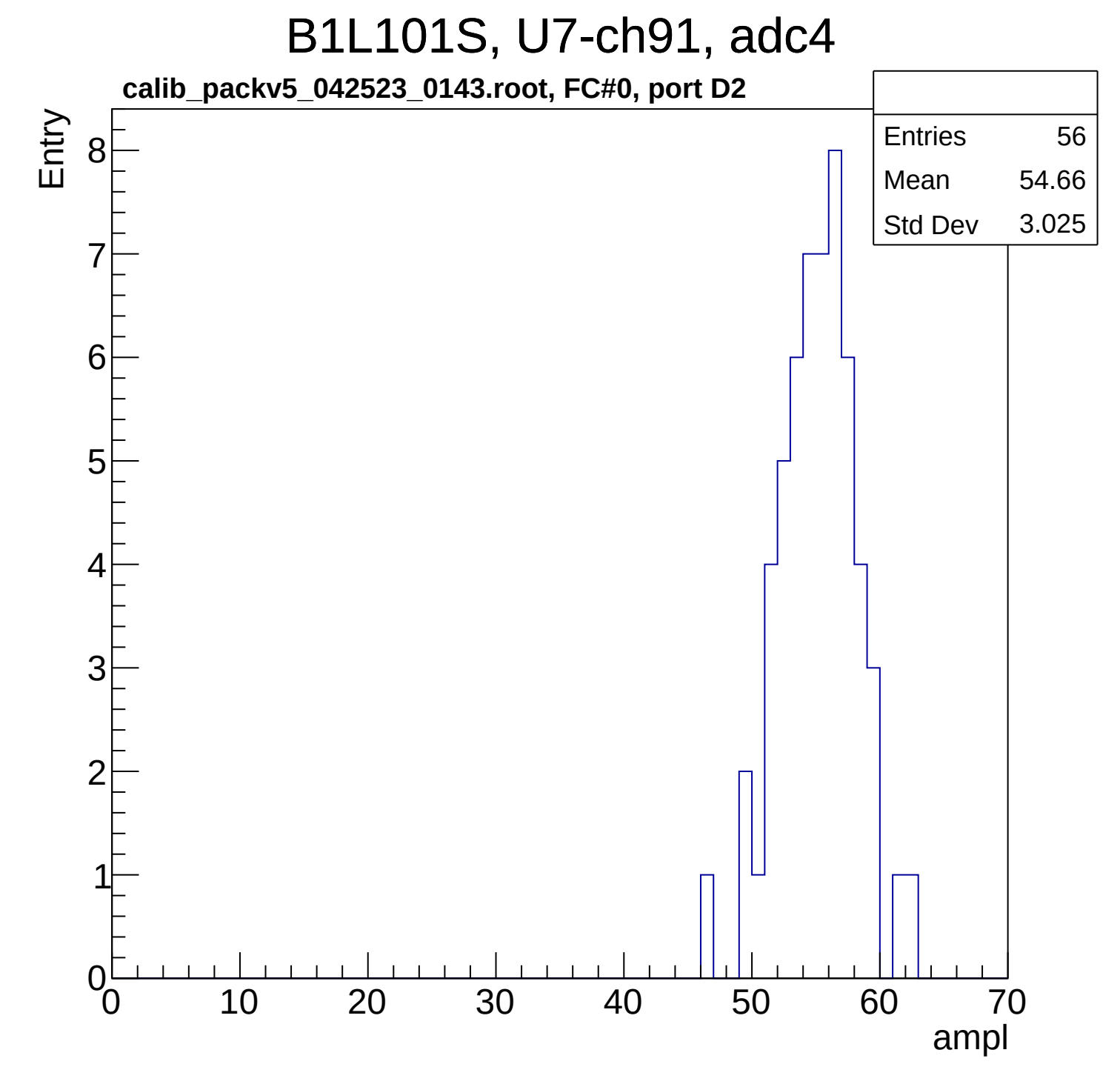
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch91, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 54.66
Std Dev 3.025
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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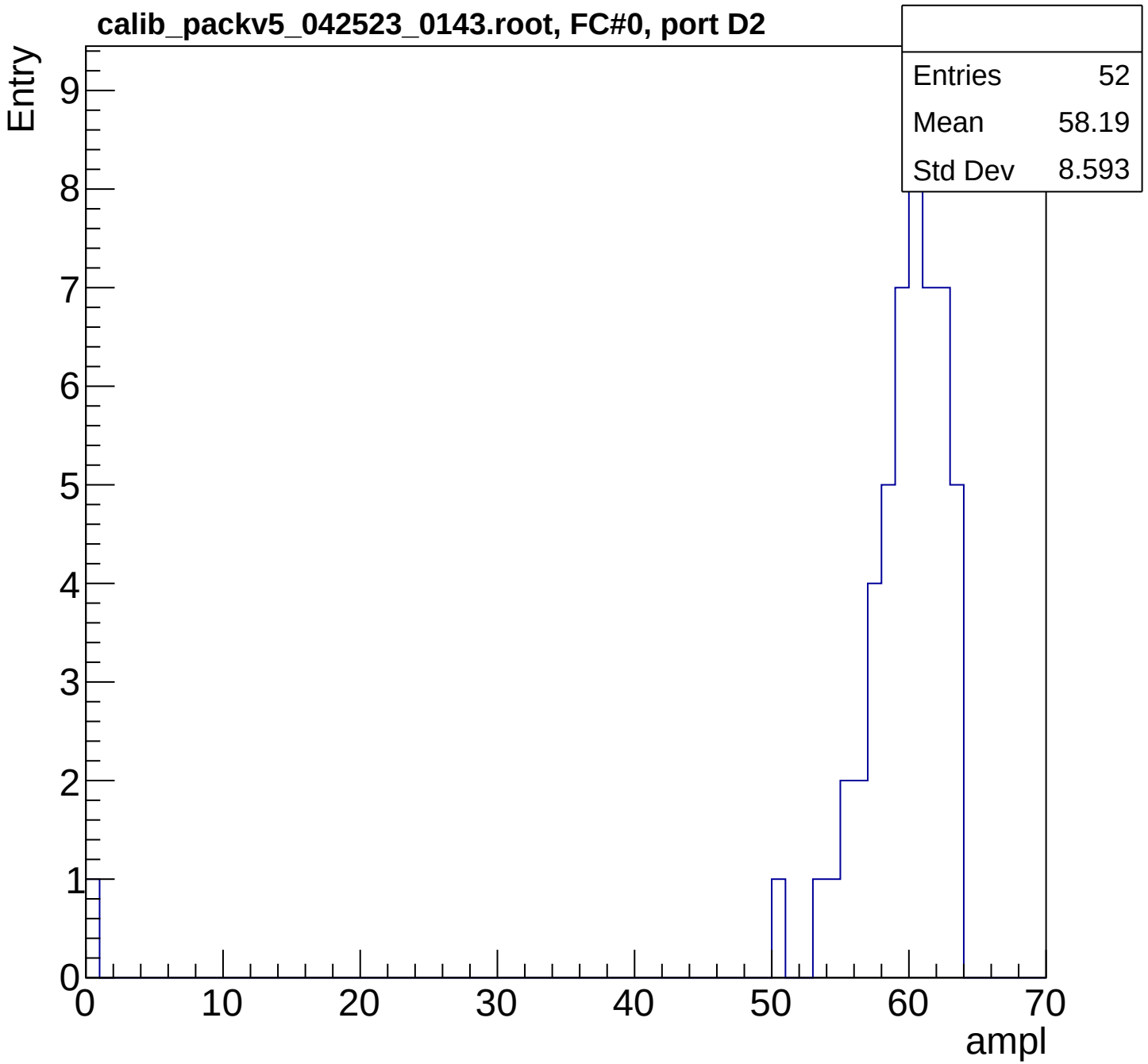
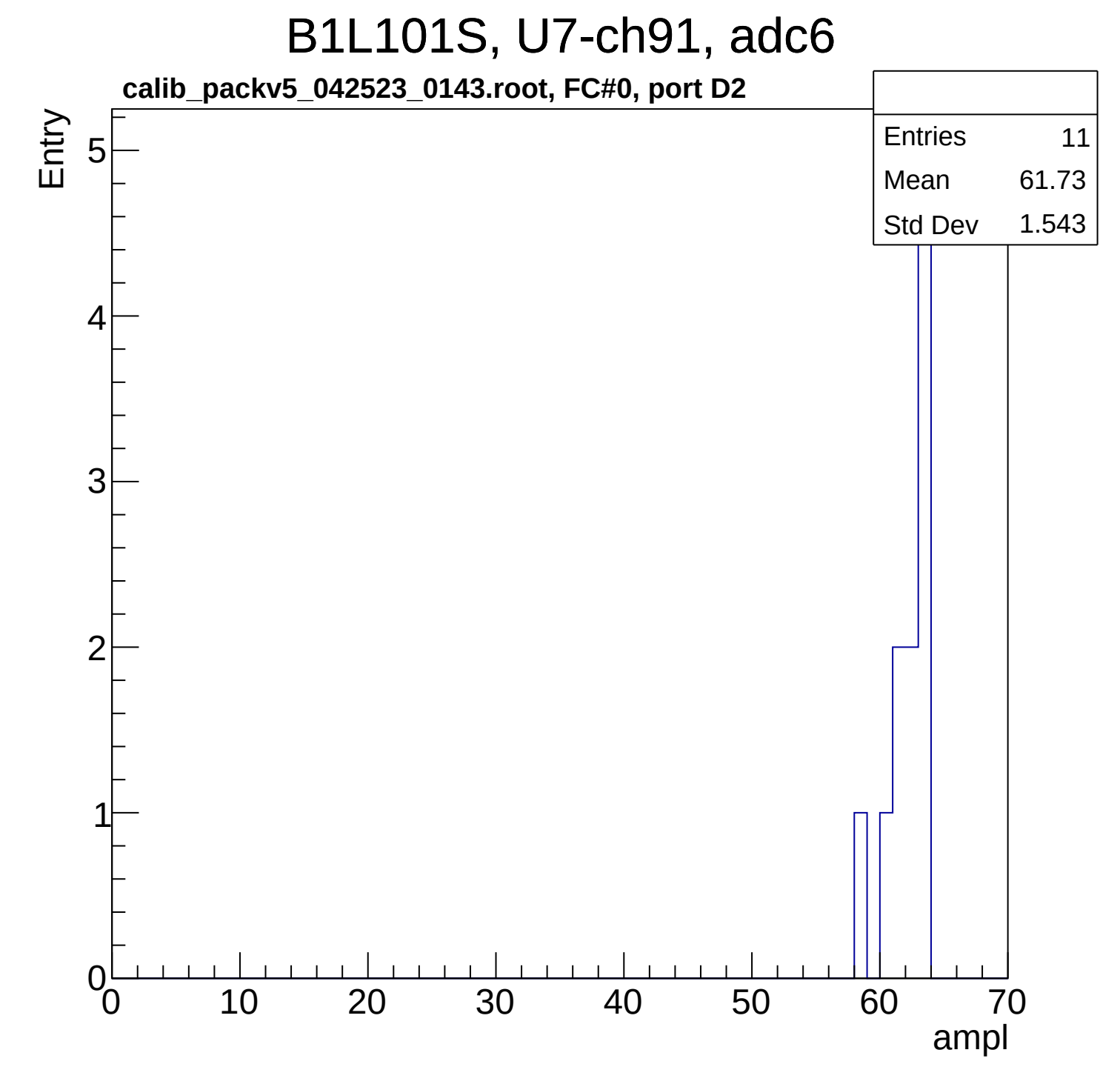
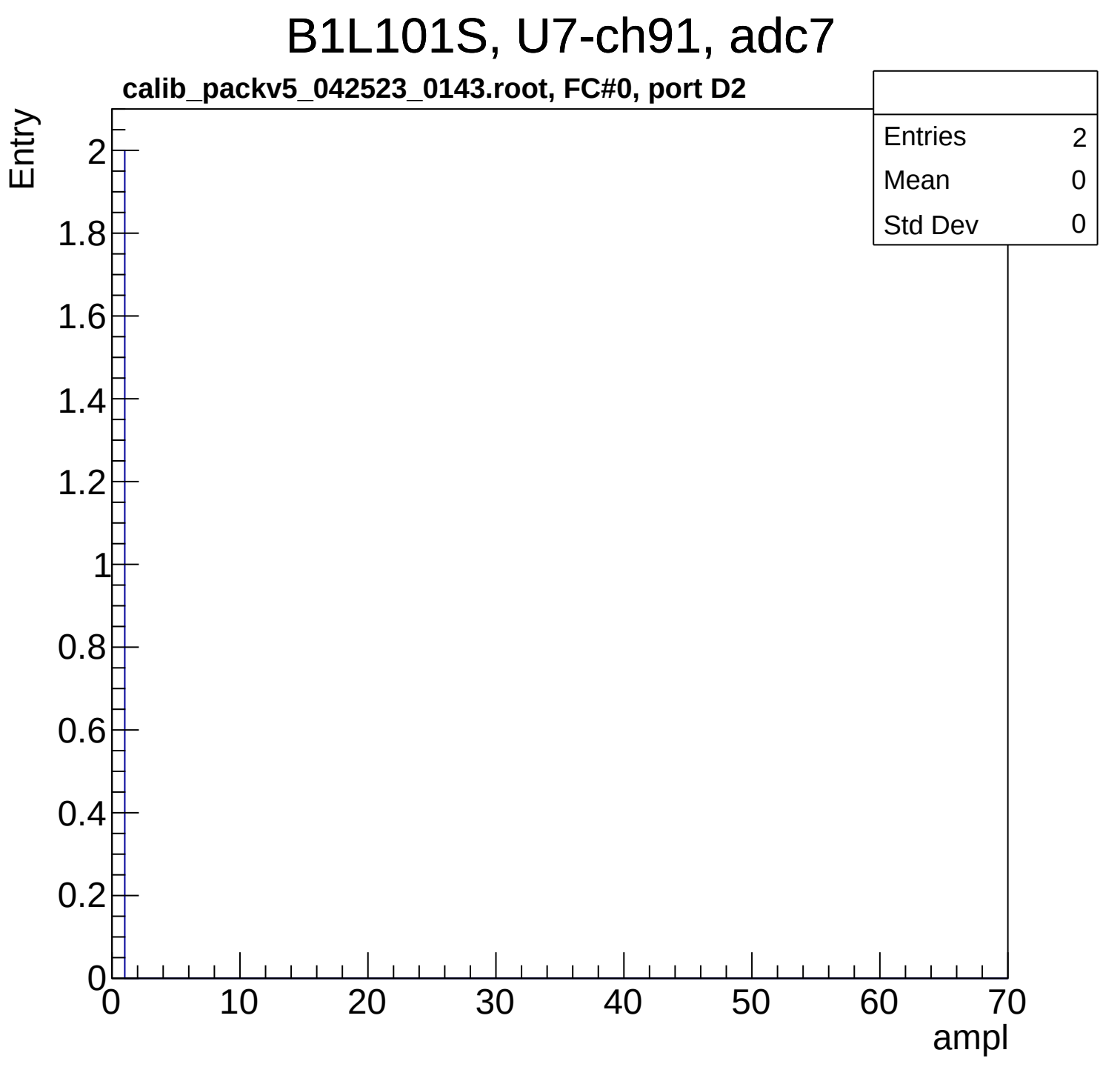
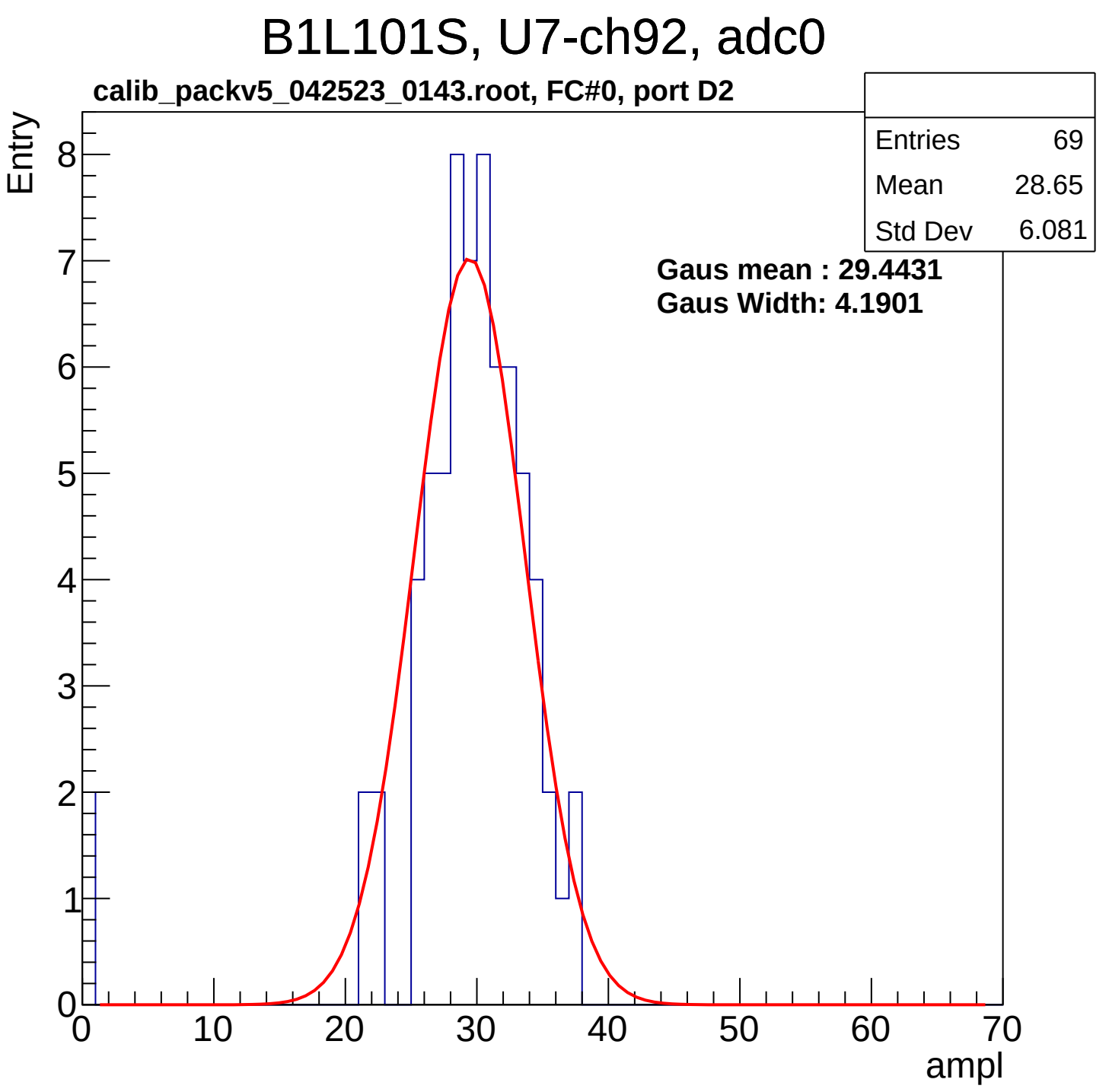
40
50
60
70


B1L101S, U7-ch91, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 58.19
Std Dev 8.593
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch91, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 11
Mean 61.73
Std Dev 1.543
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L101S, U7-ch91, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U7-ch92, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 28.65
Std Dev 6.081
Gaus mean : 29.4431
Gaus Width: 4.1901
Entry
ampl
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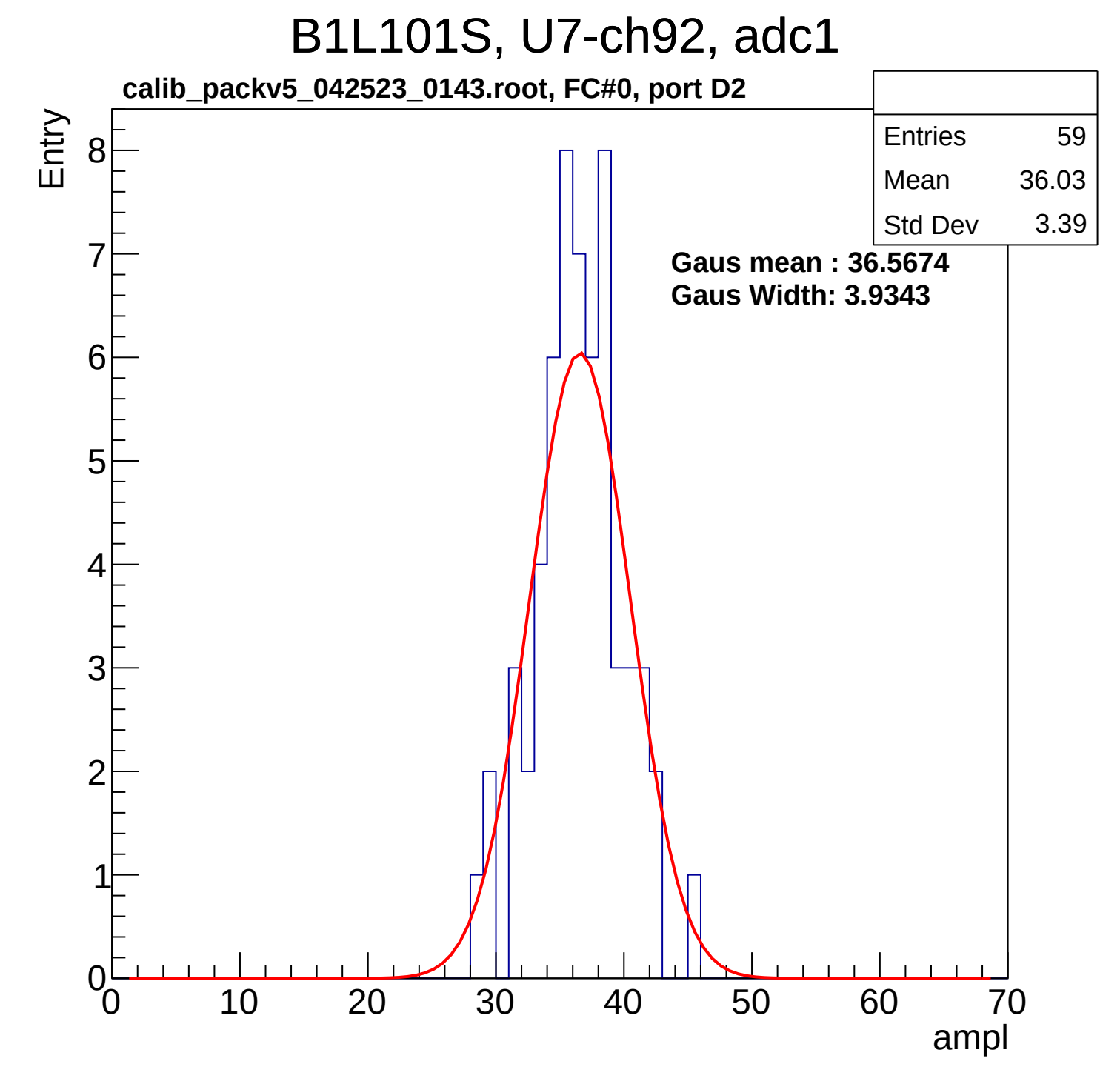
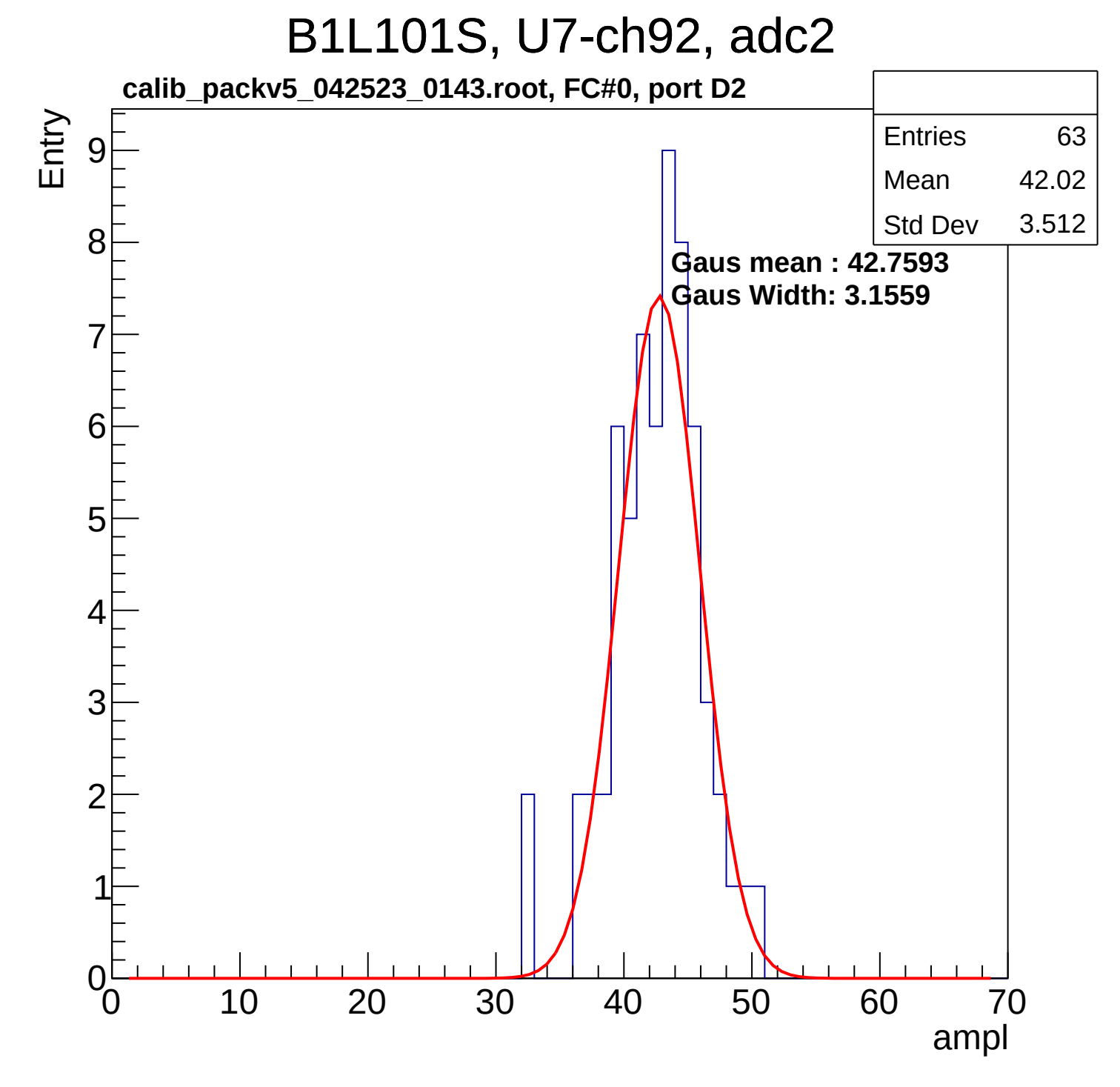
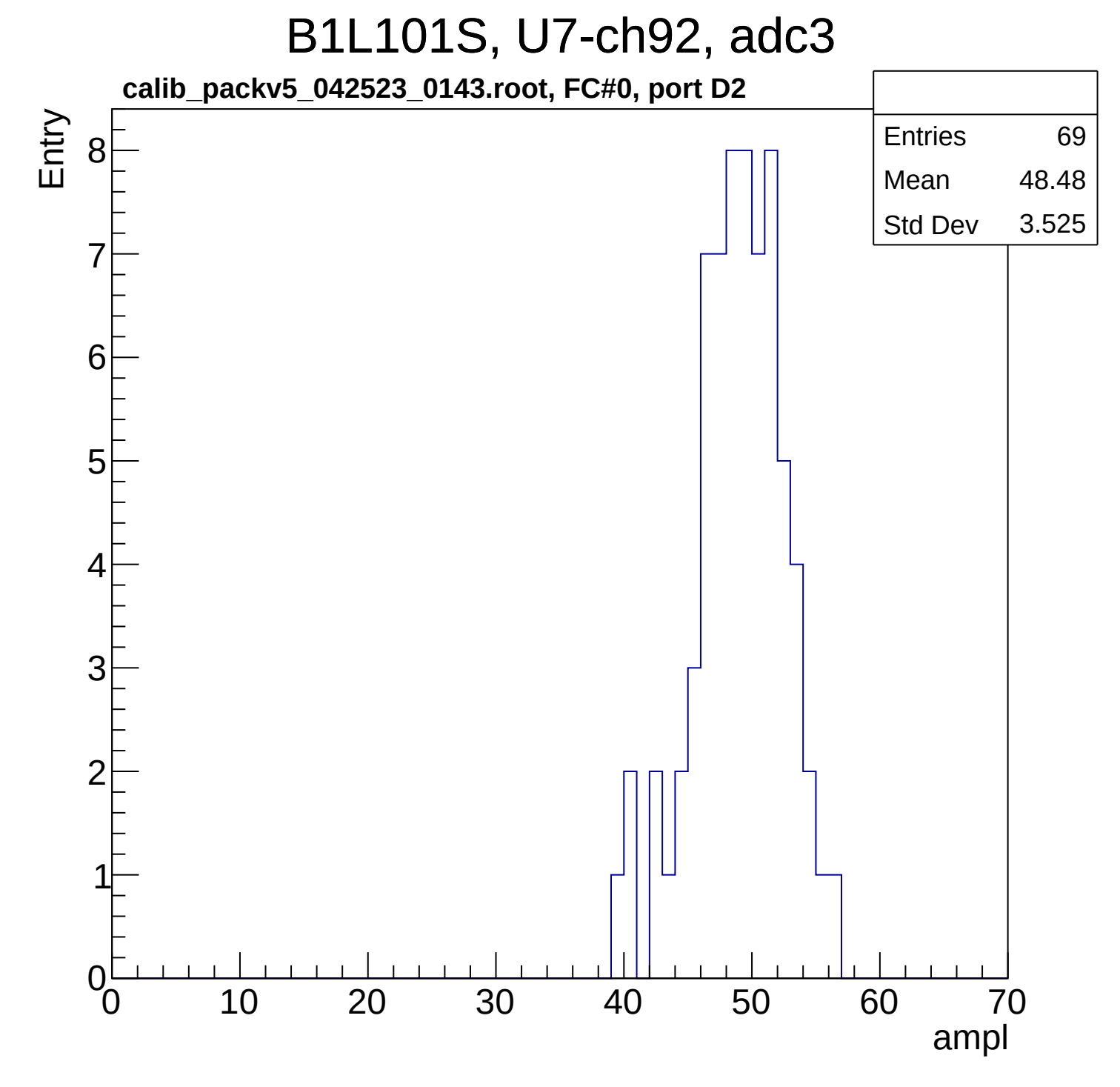
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch92, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 36.03
Std Dev 3.39
Gaus mean : 36.5674
Gaus Width: 3.9343
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch92, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 42.02
Std Dev 3.512
Gaus mean : 42.7593
Gaus Width: 3.1559
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch92, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 48.48
Std Dev 3.525
Entry
ampl
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1
2
3
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5
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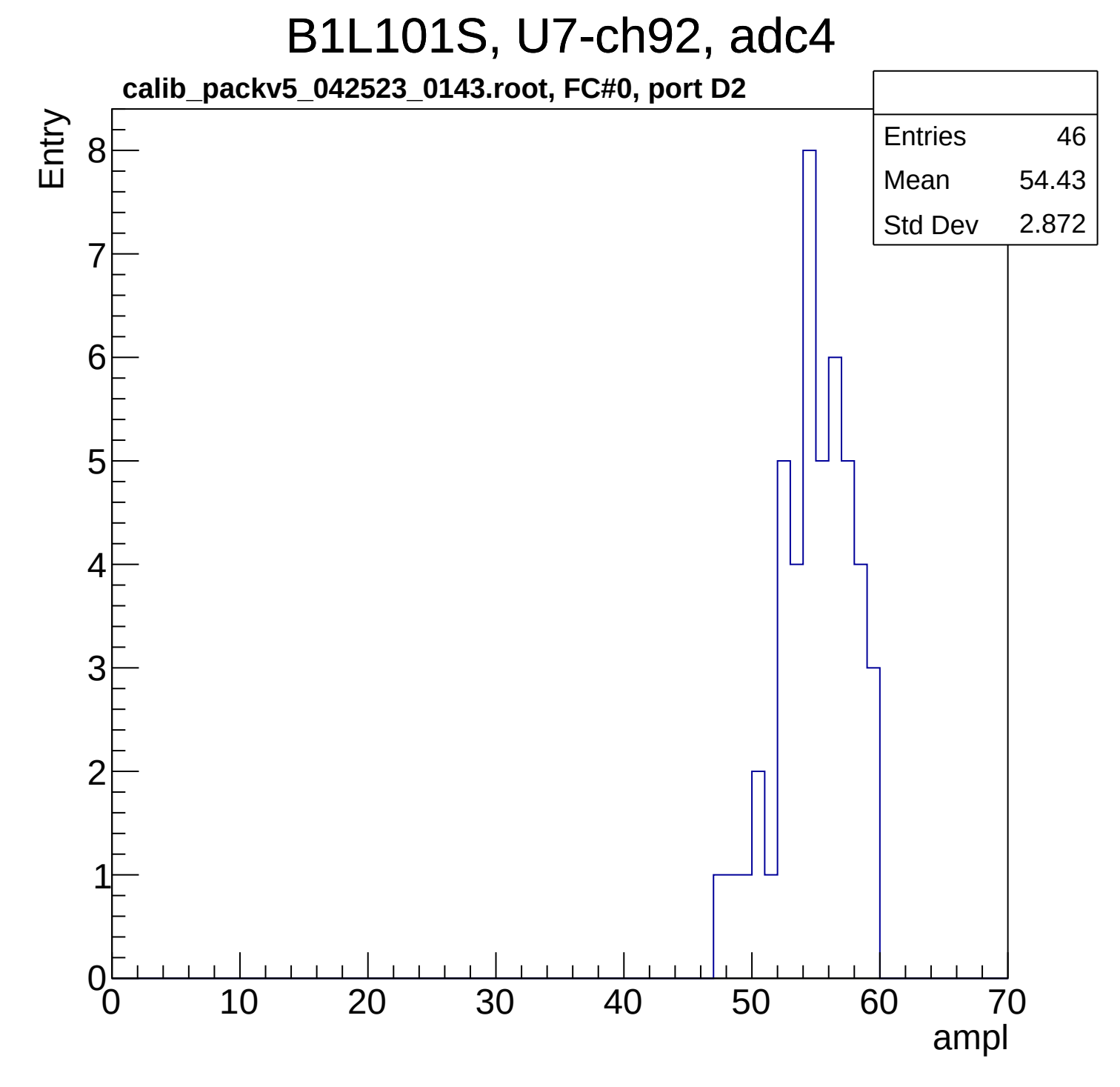
B1L101S, U7-ch92, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 54.43
Std Dev 2.872
Entry
ampl
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1
2
3
4
5
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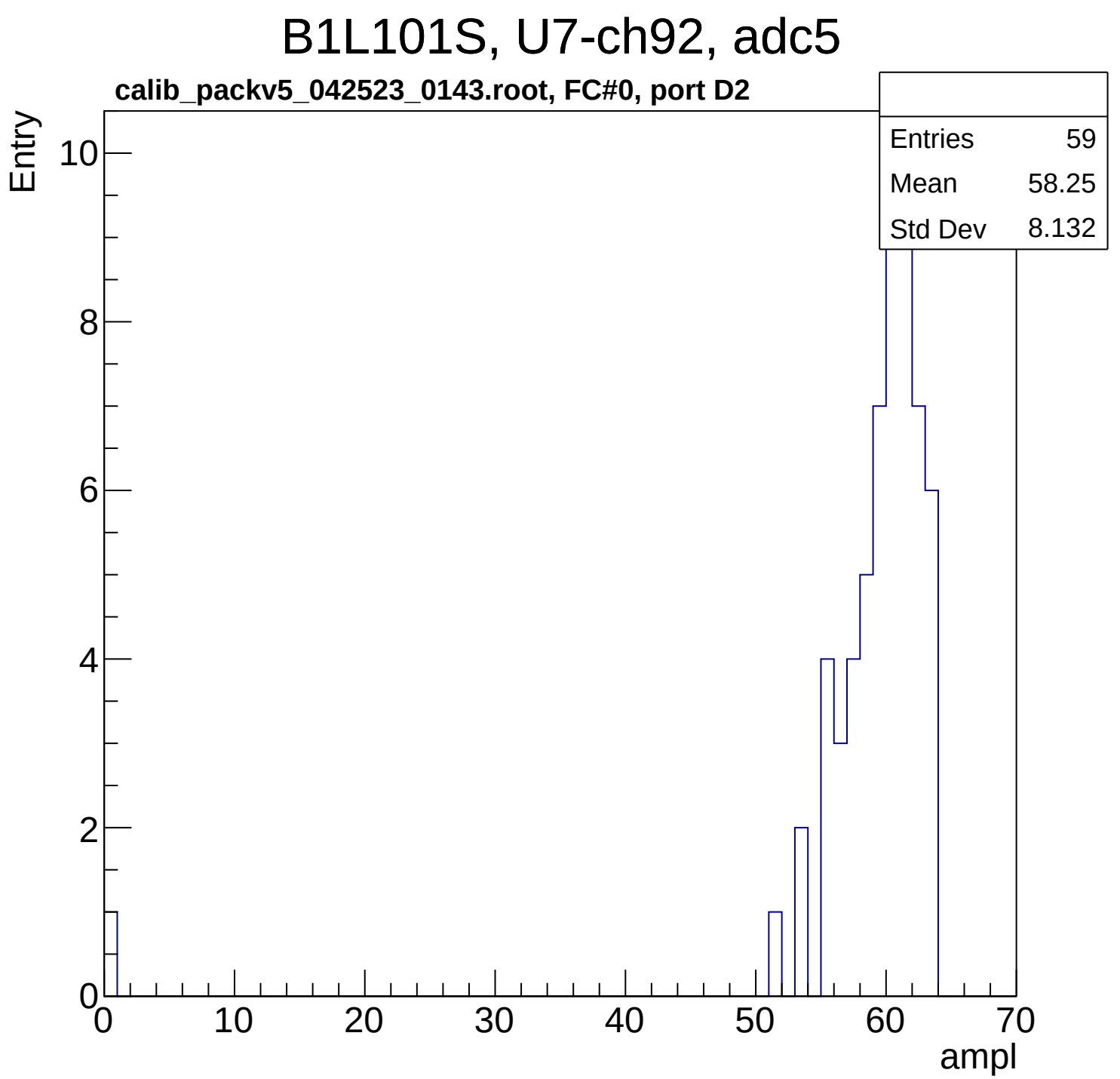
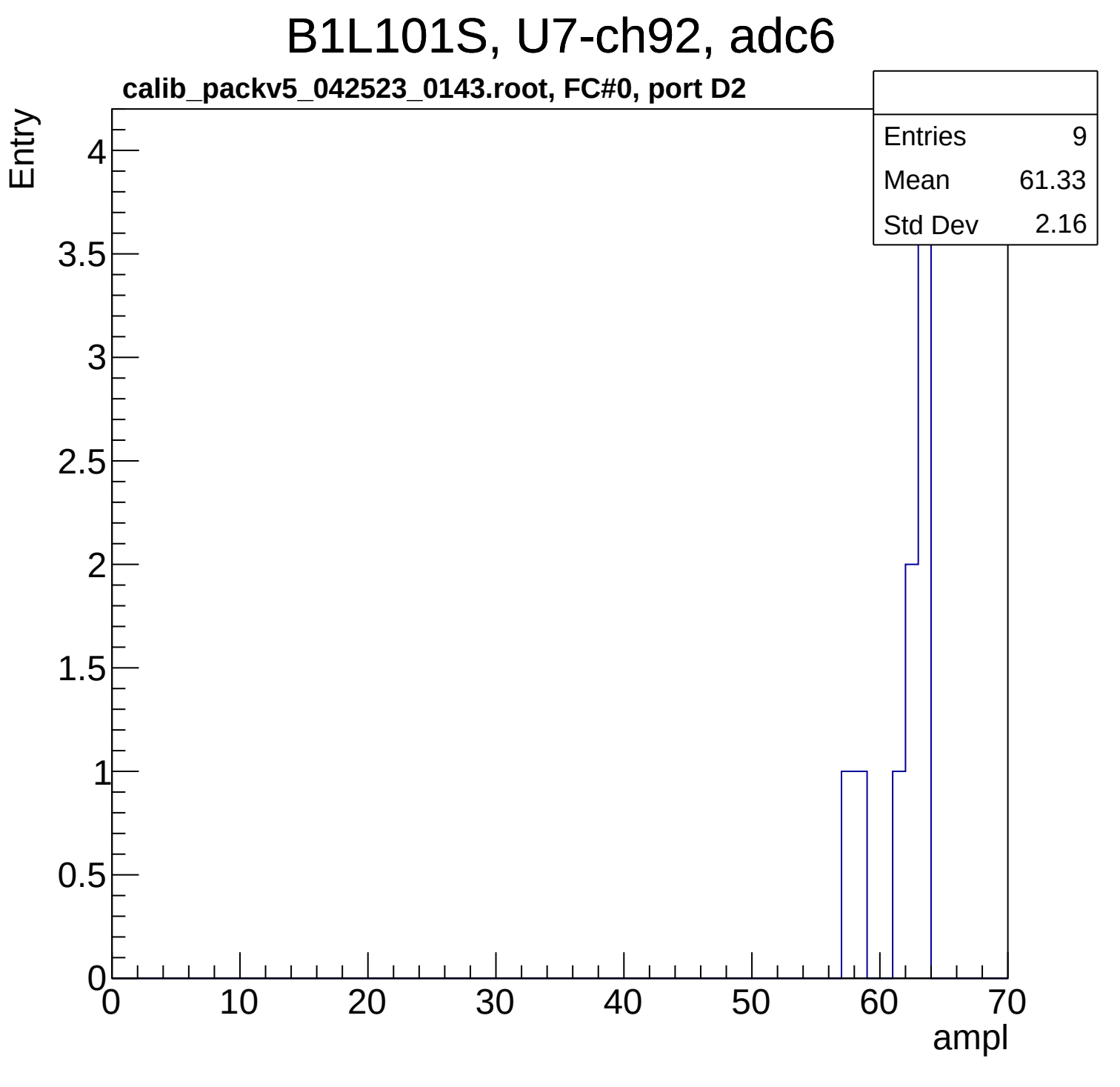

B1L101S, U7-ch92, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 58.25
Std Dev 8.132
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch92, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 61.33
Std Dev 2.16
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
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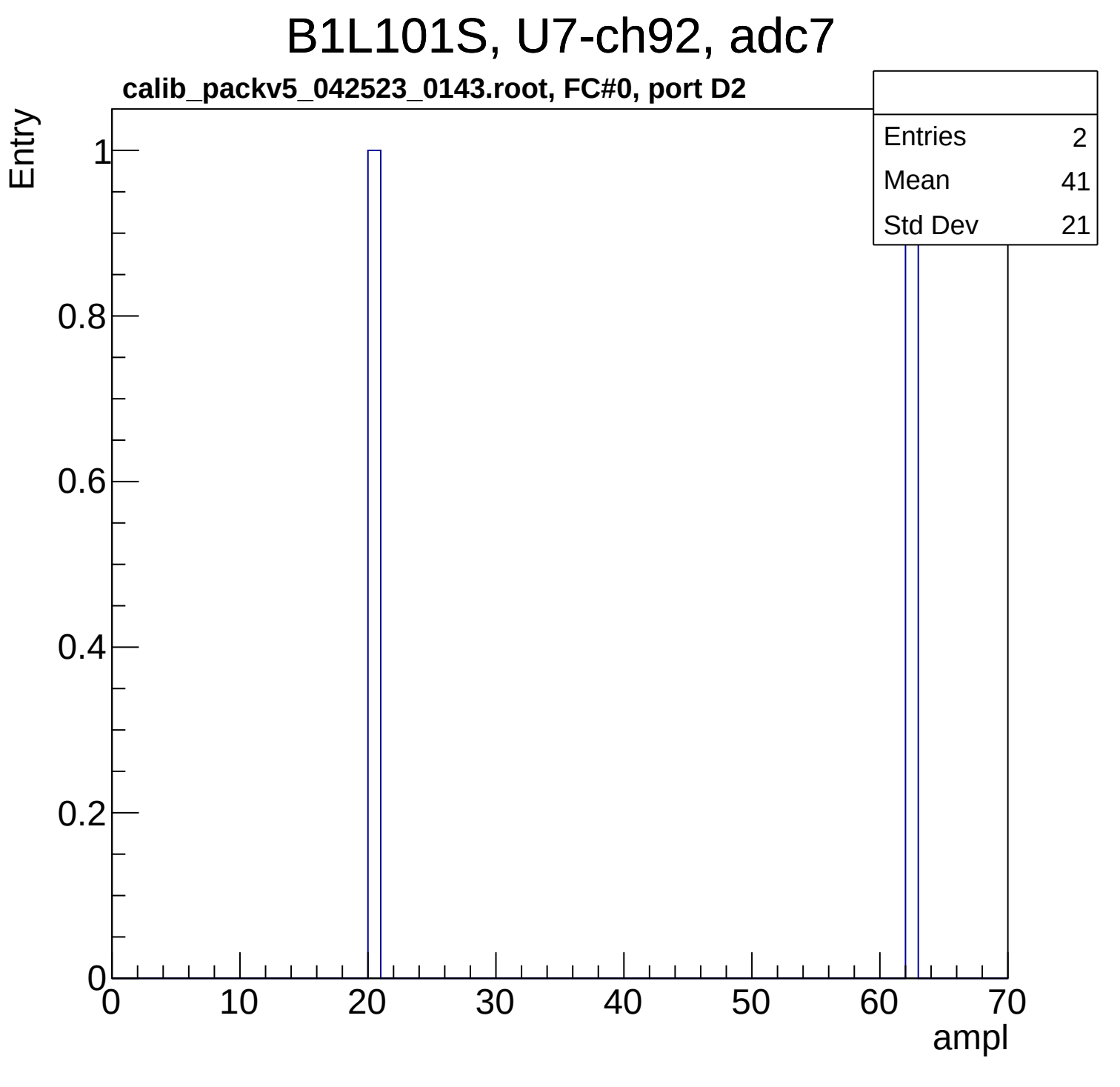
B1L101S, U7-ch92, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 41
Std Dev 21
Entry
ampl
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0.2
0.4
0.6
0.8
1
0
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40
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60
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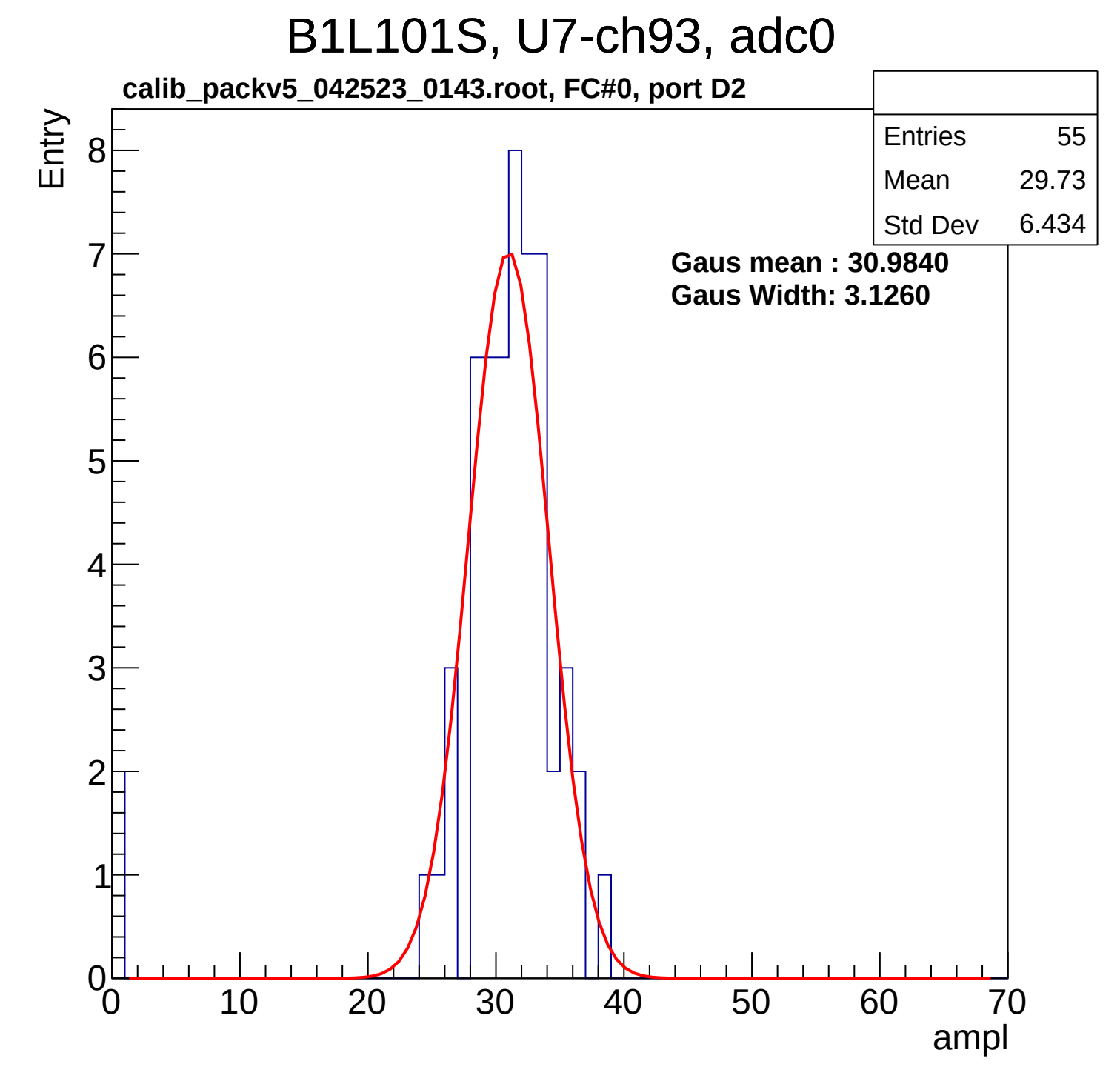
B1L101S, U7-ch93, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 29.73
Std Dev 6.434
Gaus mean : 30.9840
Gaus Width: 3.1260
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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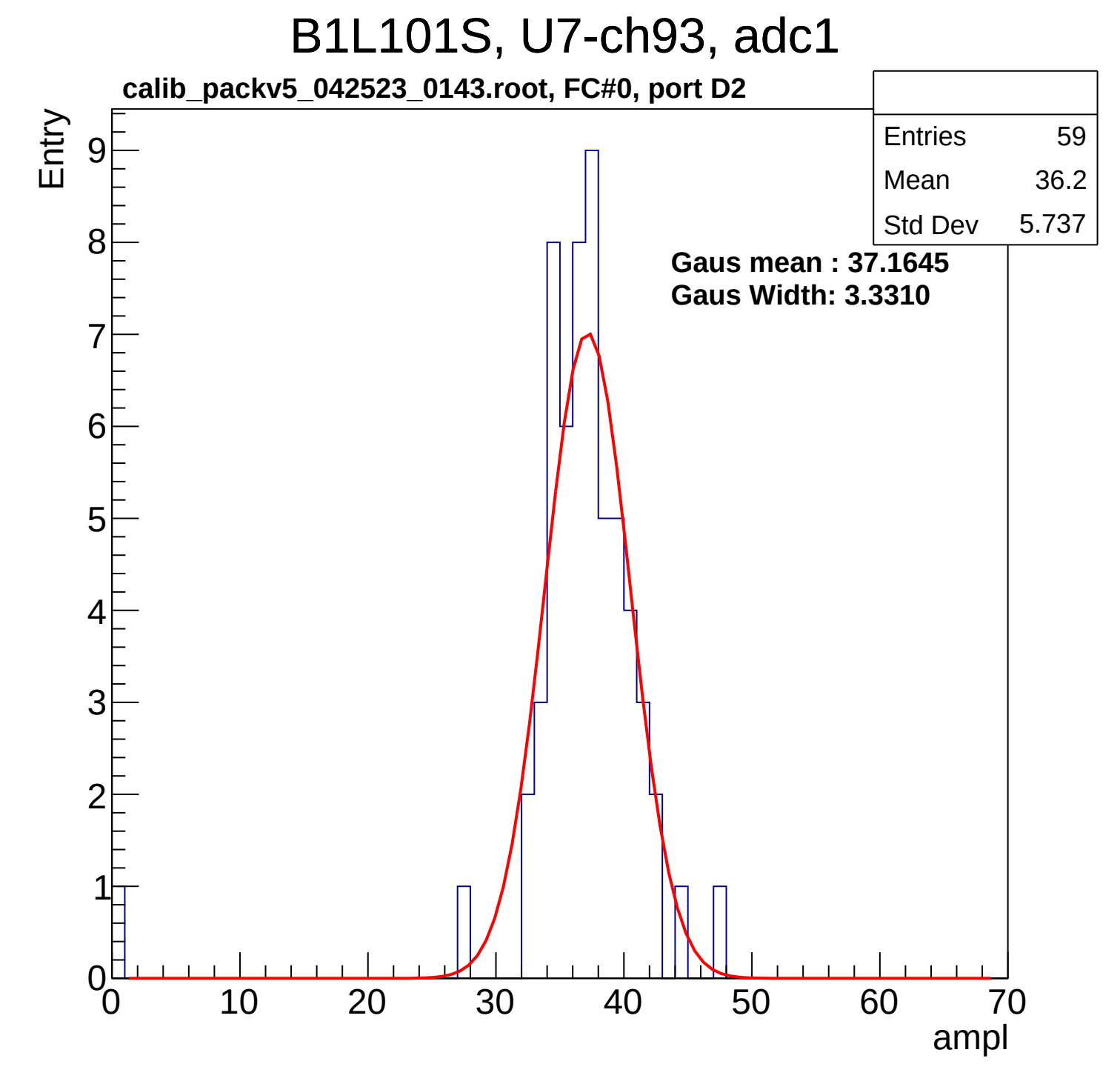
B1L101S, U7-ch93, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 36.2
Std Dev 5.737
Gaus mean : 37.1645
Gaus Width: 3.3310
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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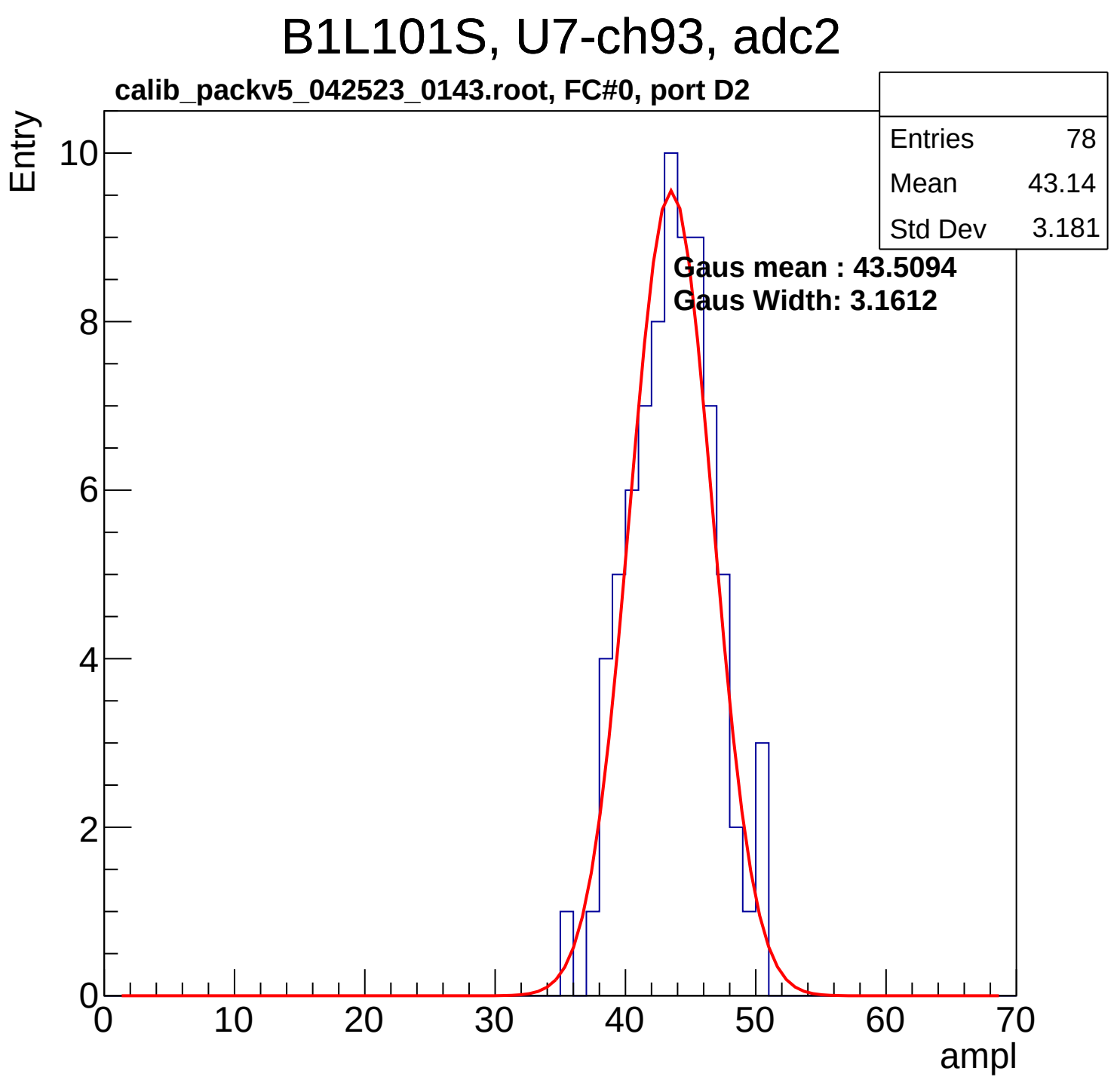
B1L101S, U7-ch93, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 43.14
Std Dev 3.181
Gaus mean : 43.5094
Gaus Width: 3.1612
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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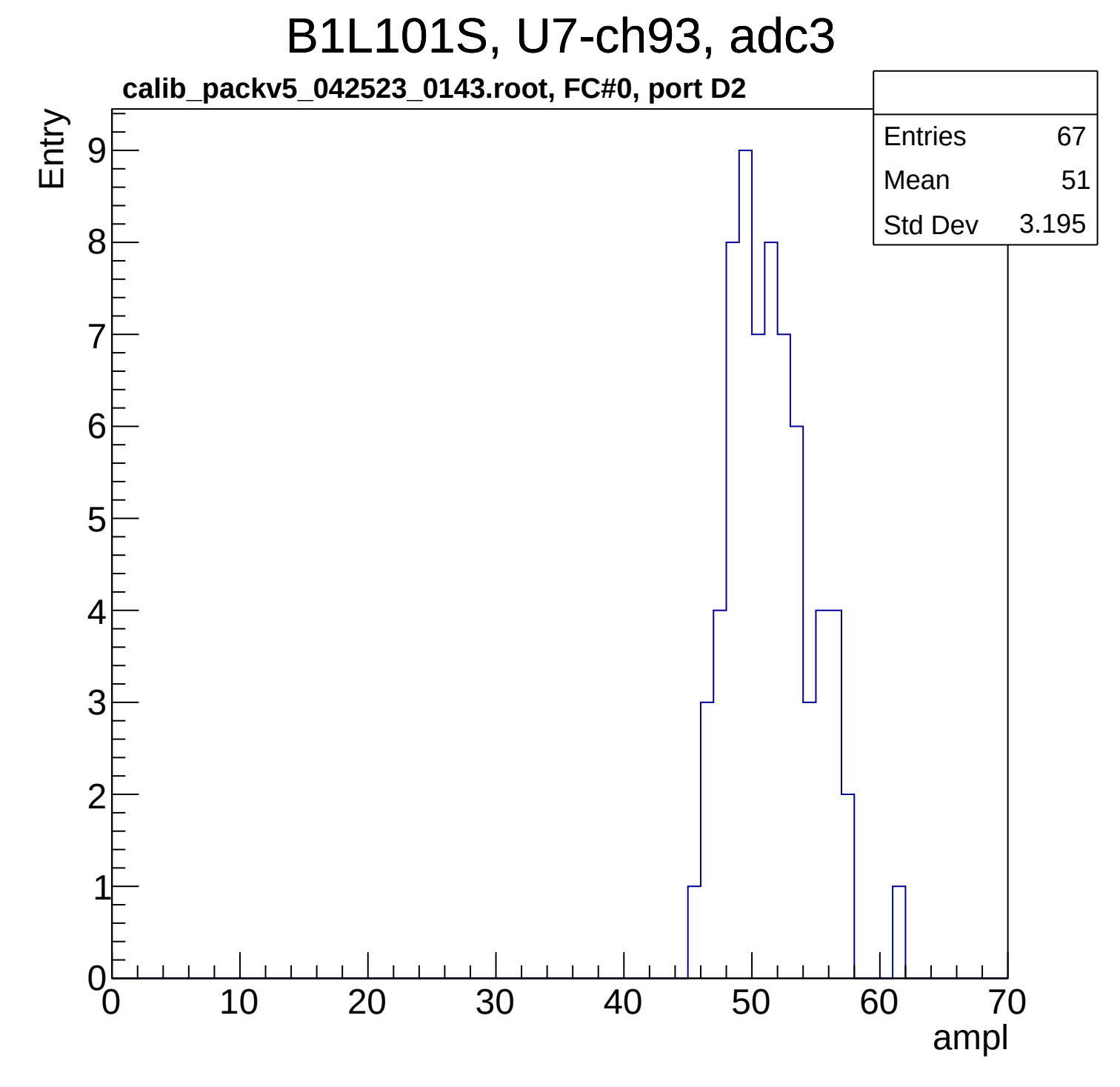
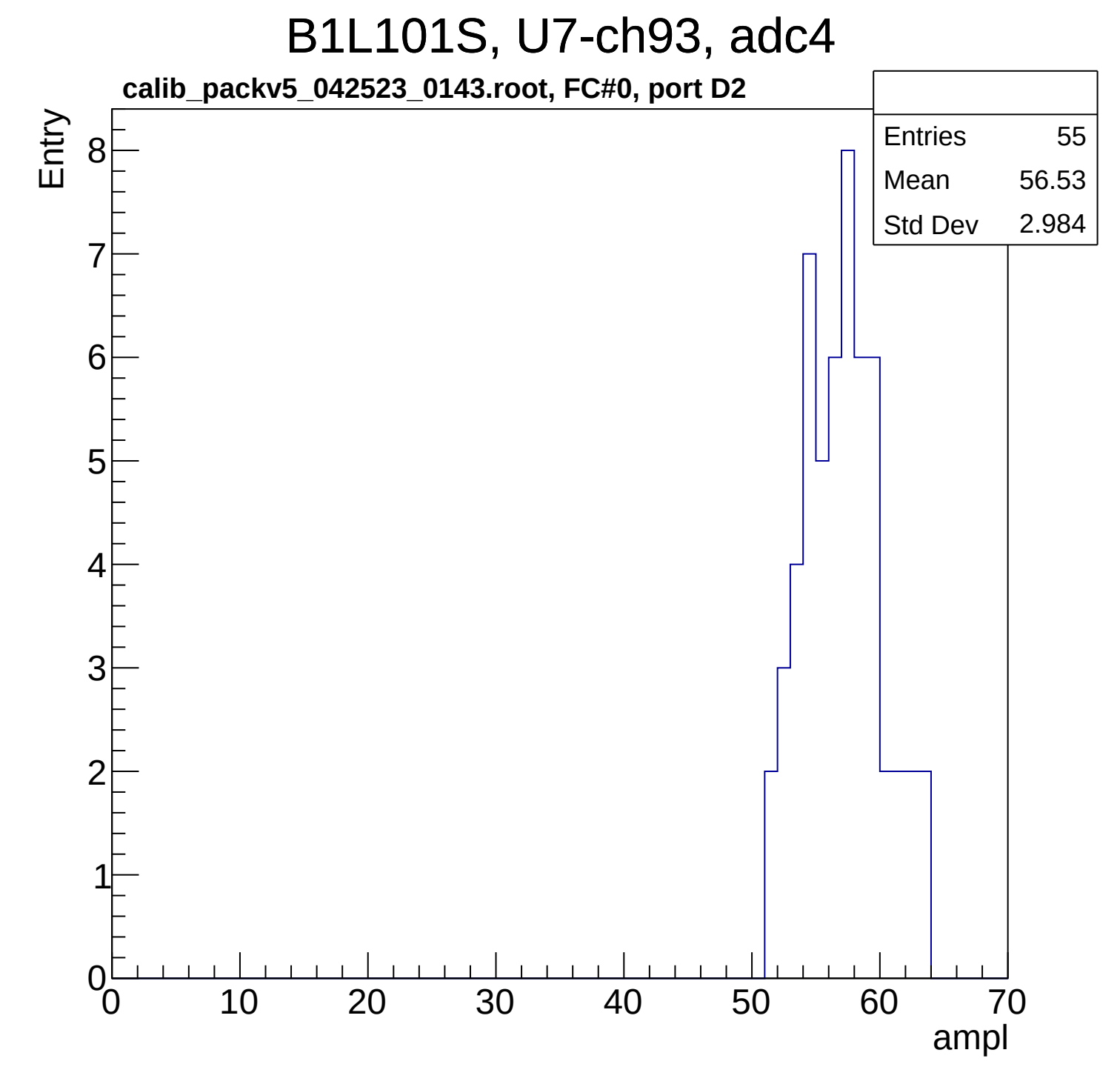
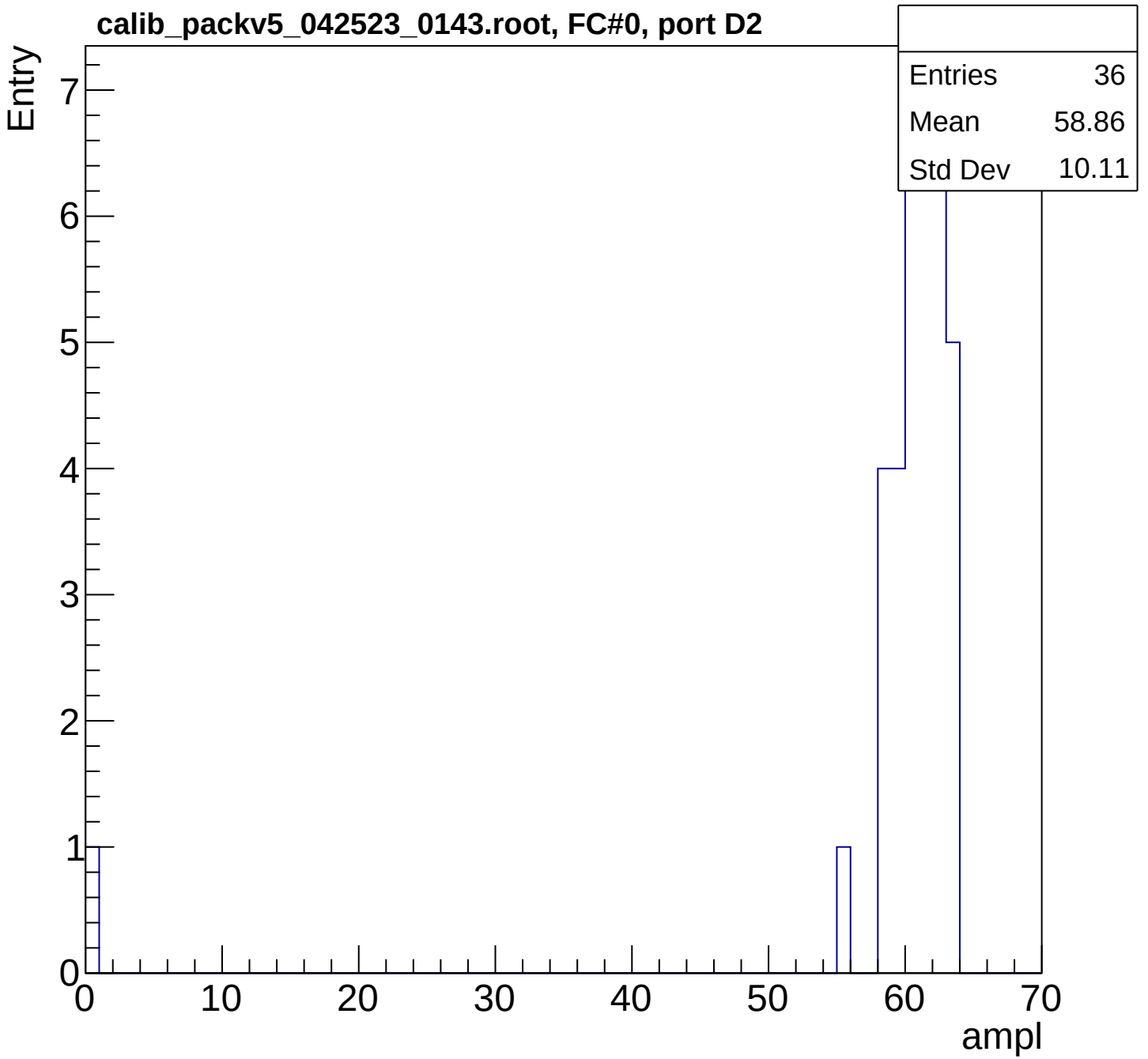
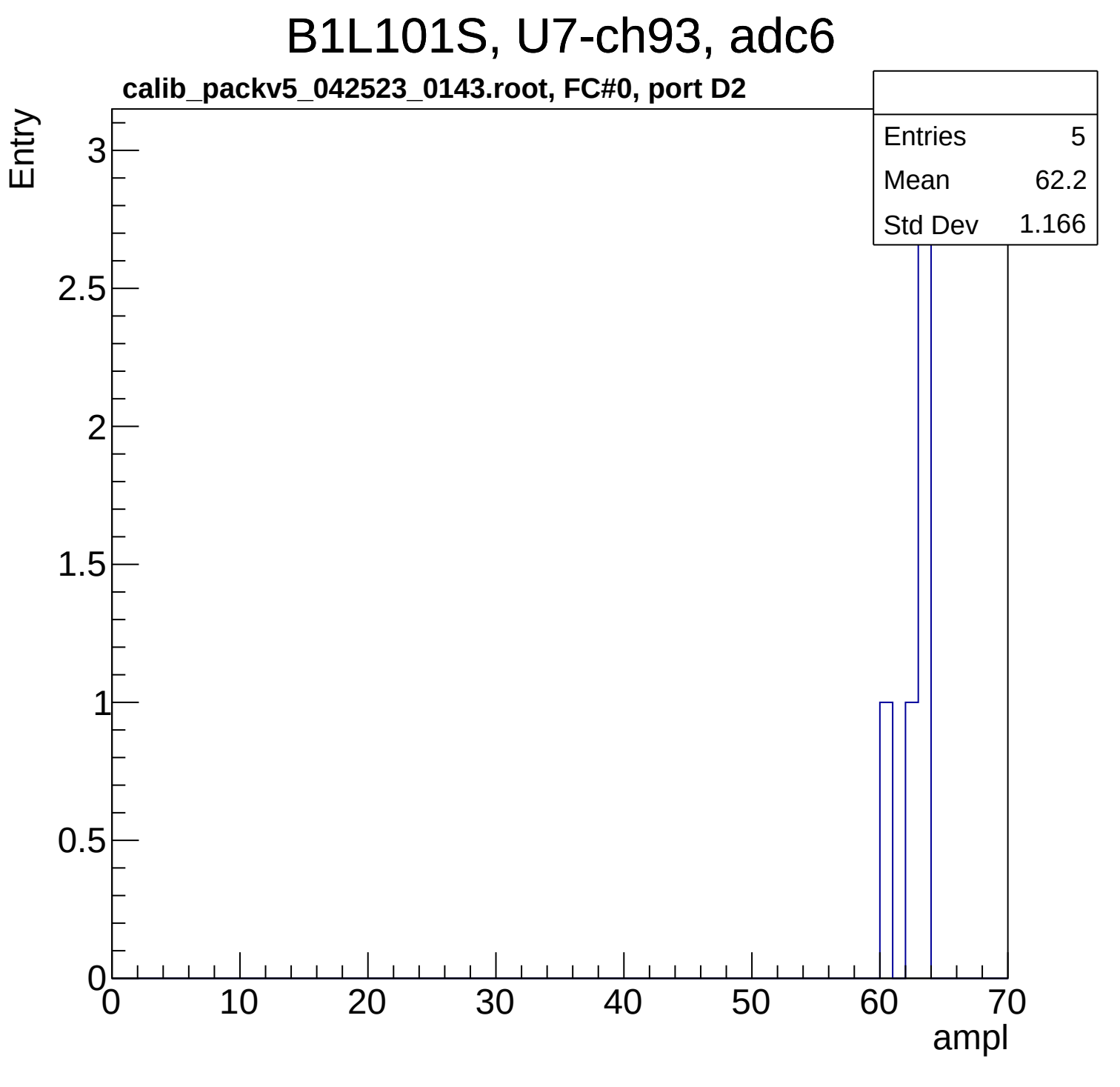

B1L101S, U7-ch93, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 51
Std Dev 3.195
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch93, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 56.53
Std Dev 2.984
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch93, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 36
Mean 58.86
Std Dev 10.11
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch93, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 62.2
Std Dev 1.166
Entry
ampl
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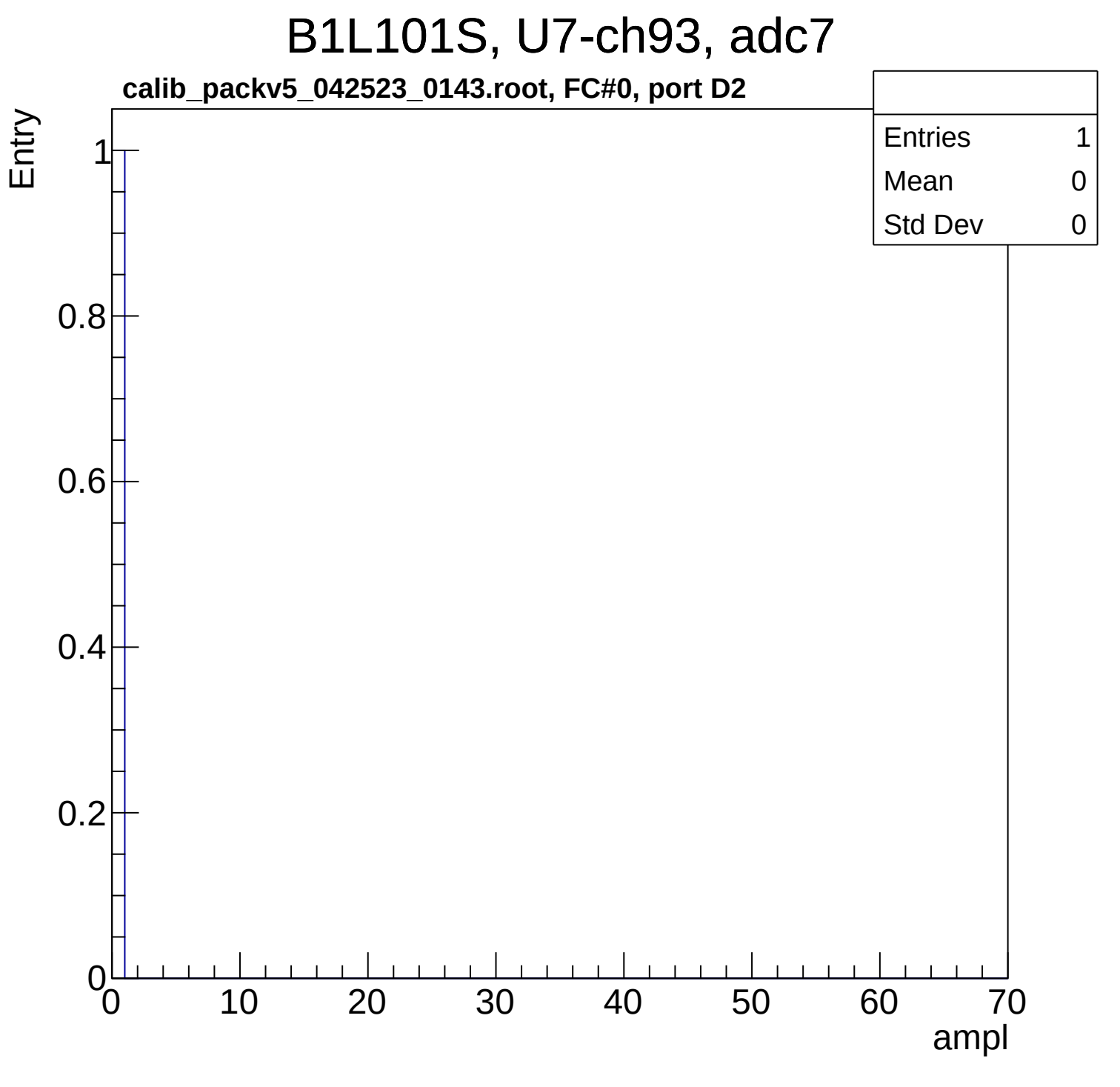
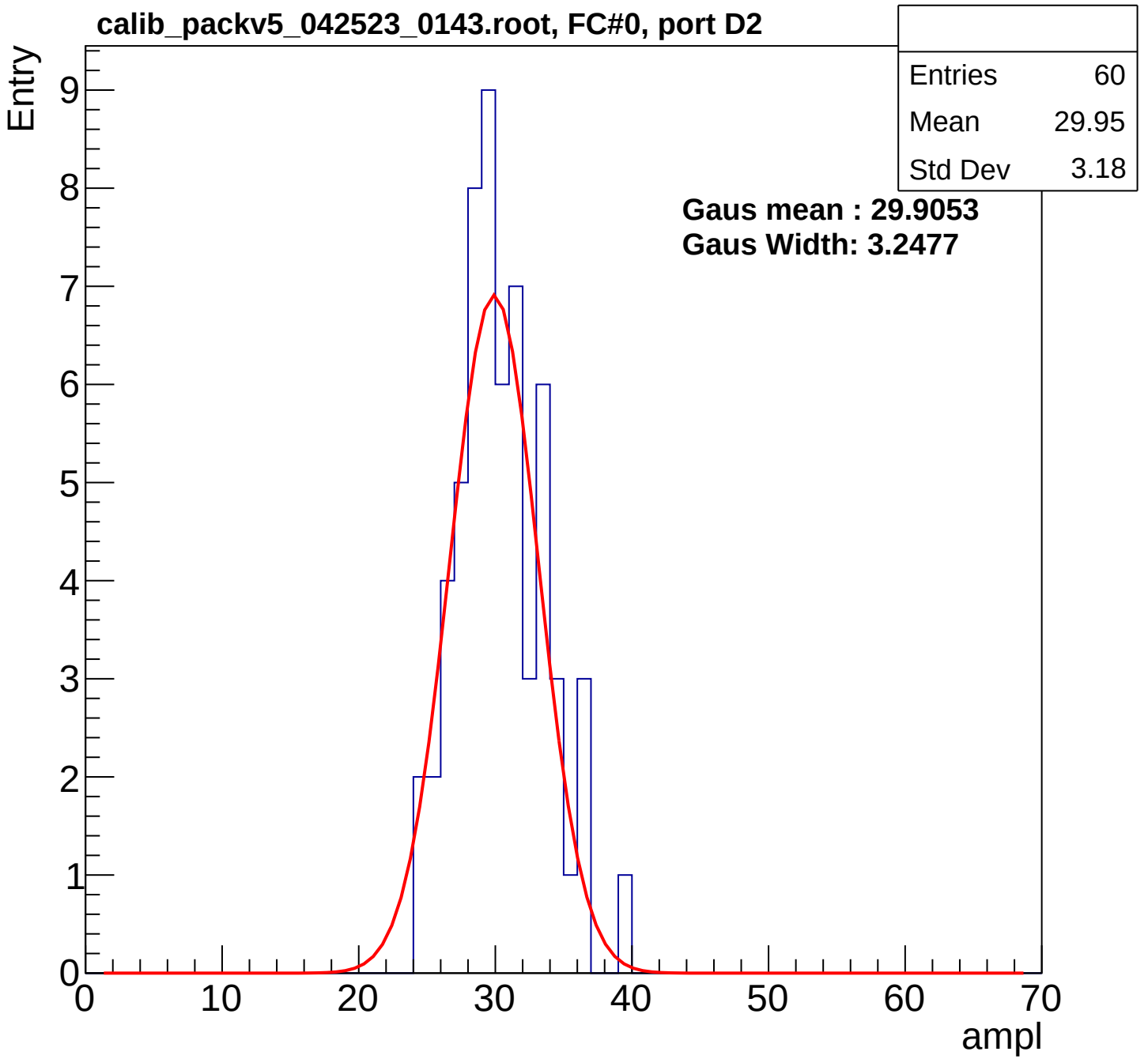
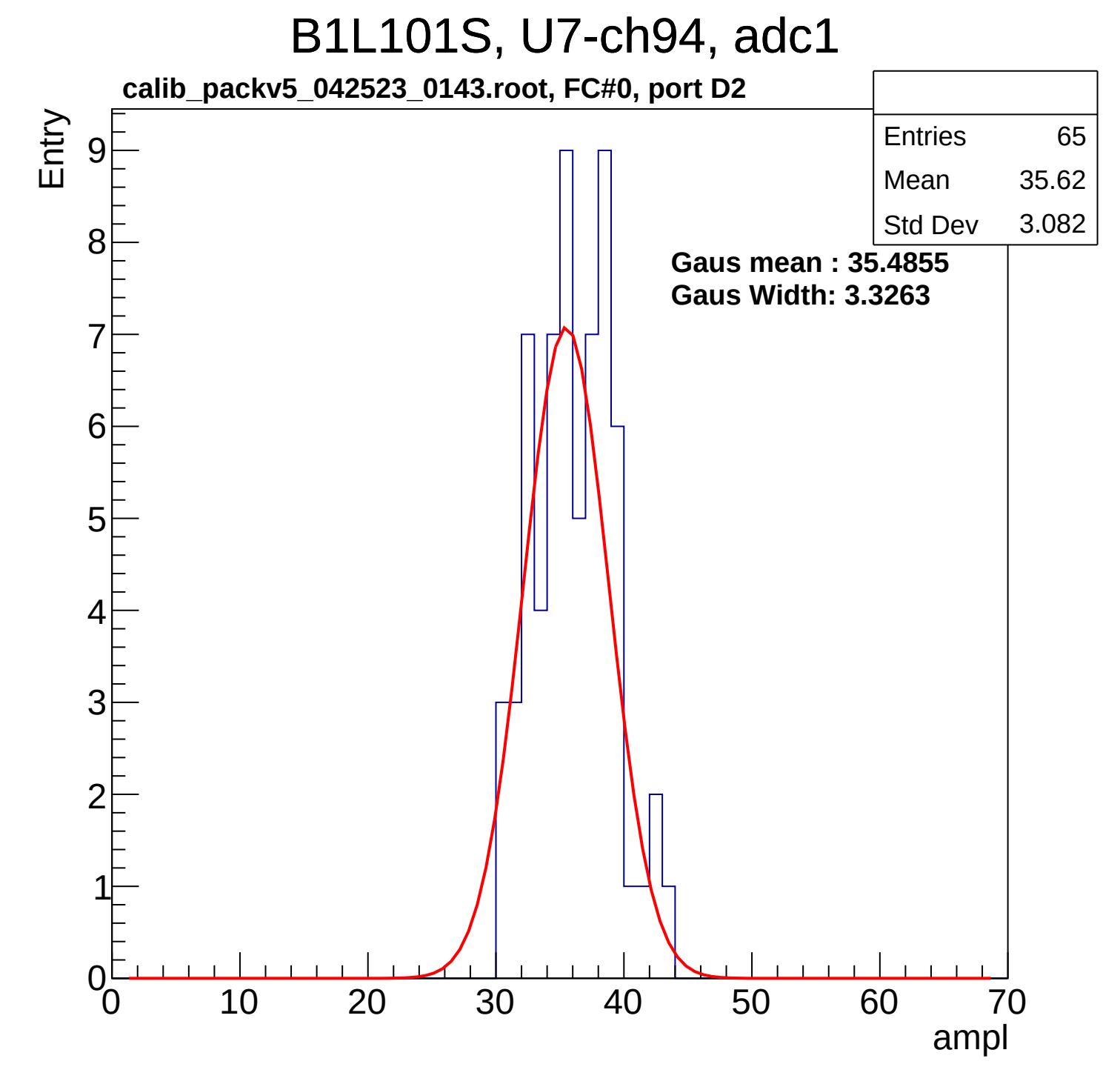
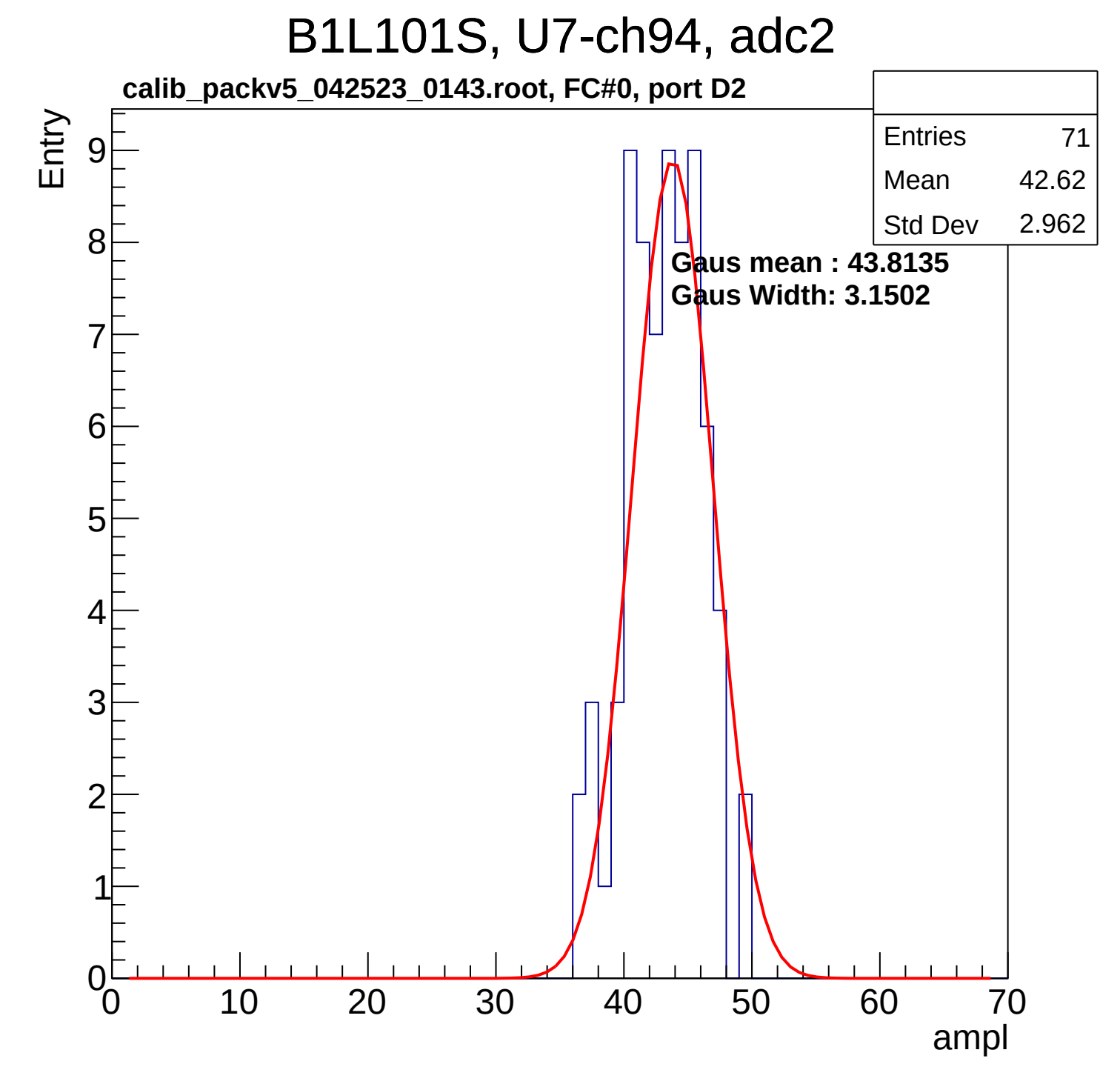
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U7-ch93, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch94, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 29.95
Std Dev 3.18
Gaus mean : 29.9053
Gaus Width: 3.2477
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch94, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 35.62
Std Dev 3.082
Gaus mean : 35.4855
Gaus Width: 3.3263
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L101S, U7-ch94, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 42.62
Std Dev 2.962
Gaus mean : 43.8135
Gaus Width: 3.1502
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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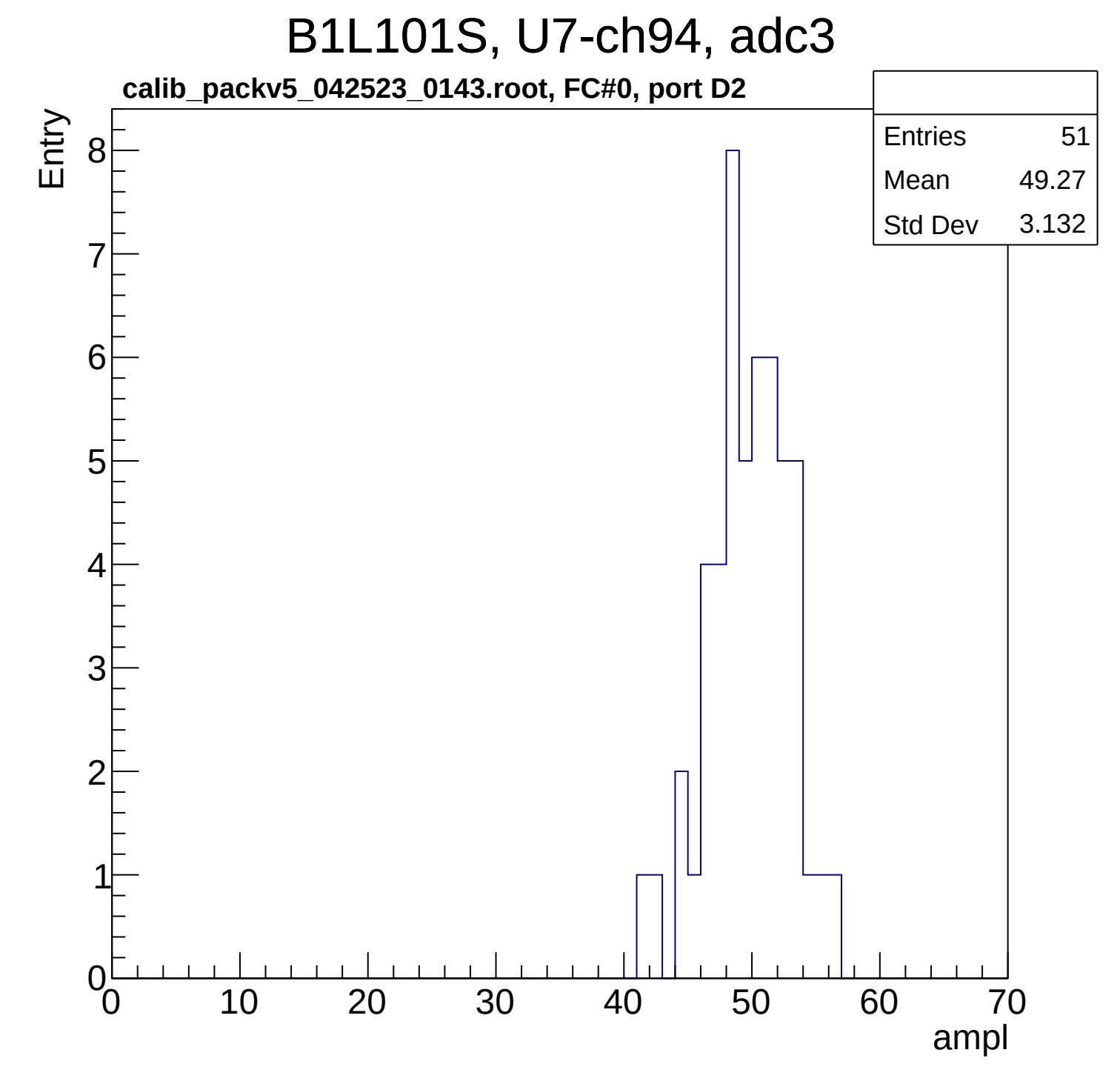
B1L101S, U7-ch94, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 49.27
Std Dev 3.132
Entry
ampl
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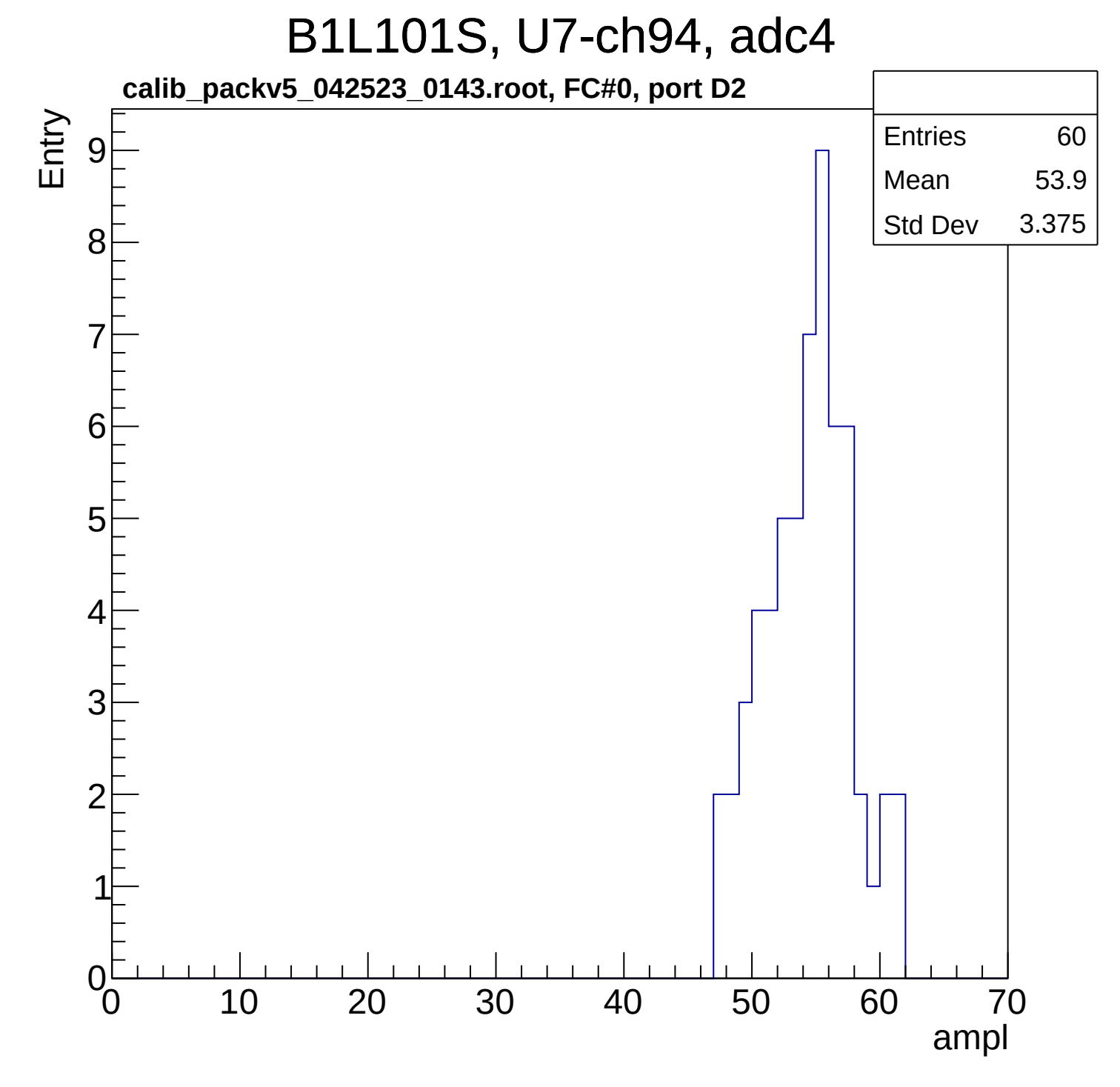
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch94, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 53.9
Std Dev 3.375
Entry
ampl
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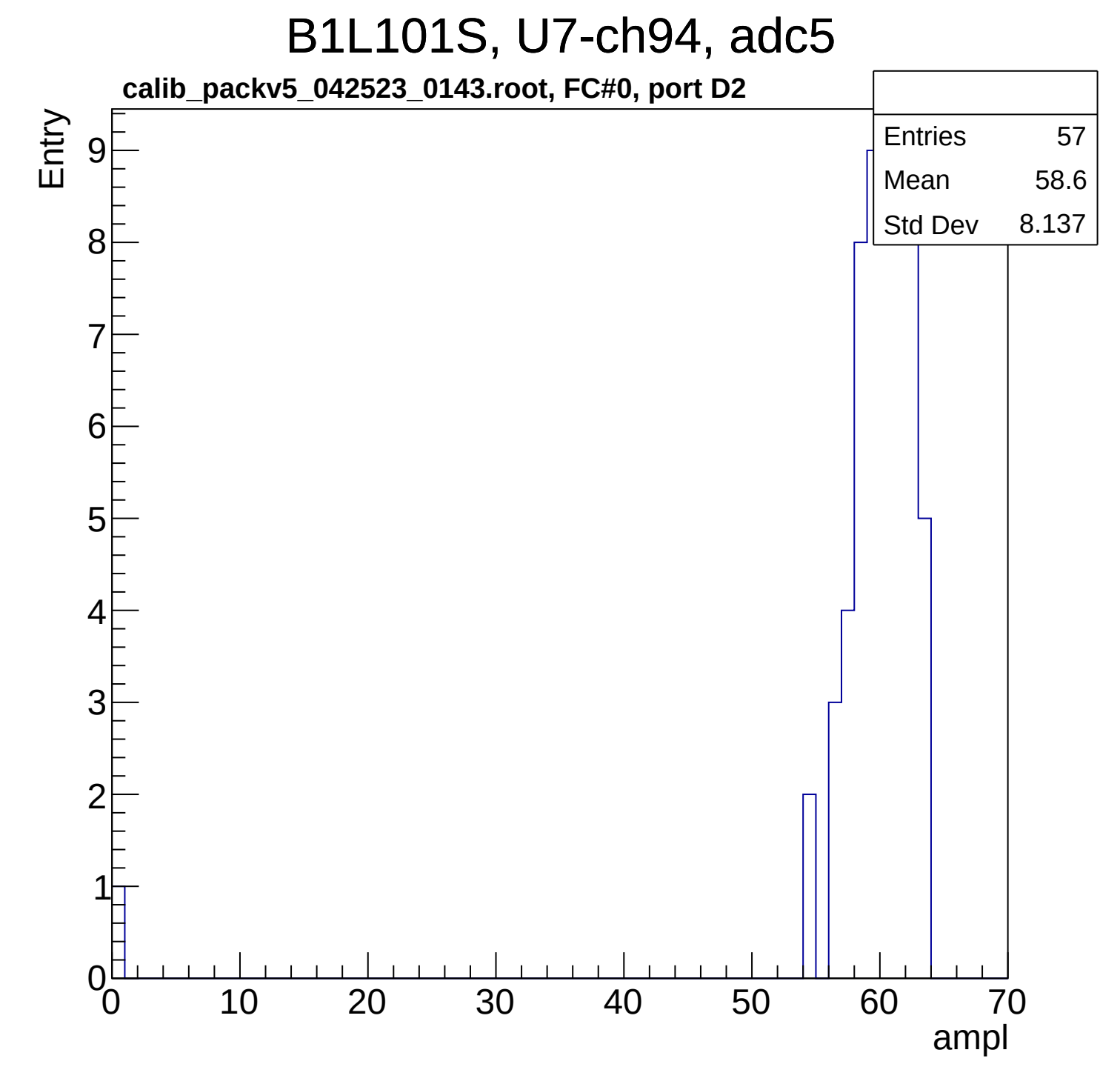
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch94, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 58.6
Std Dev 8.137
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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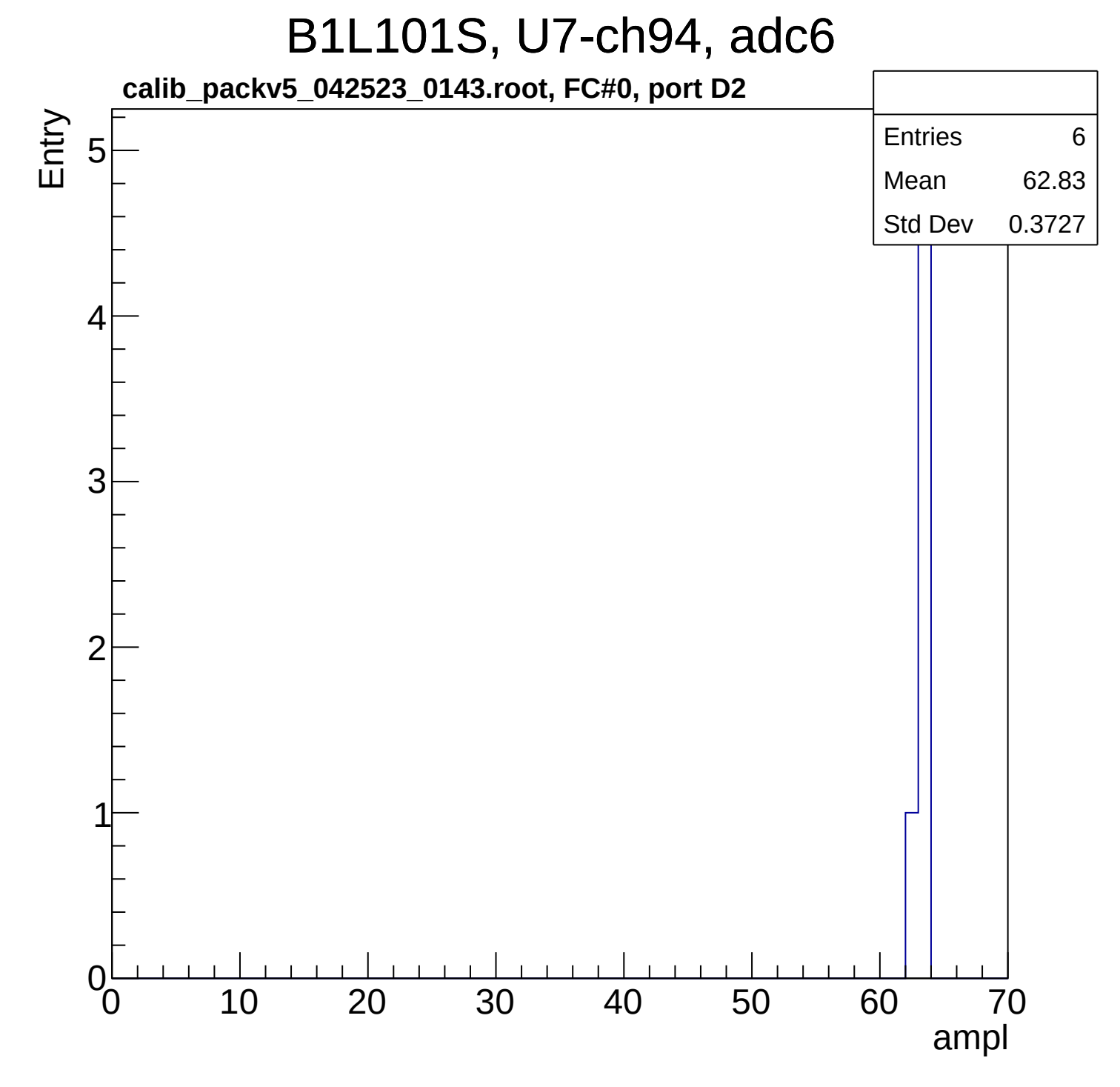
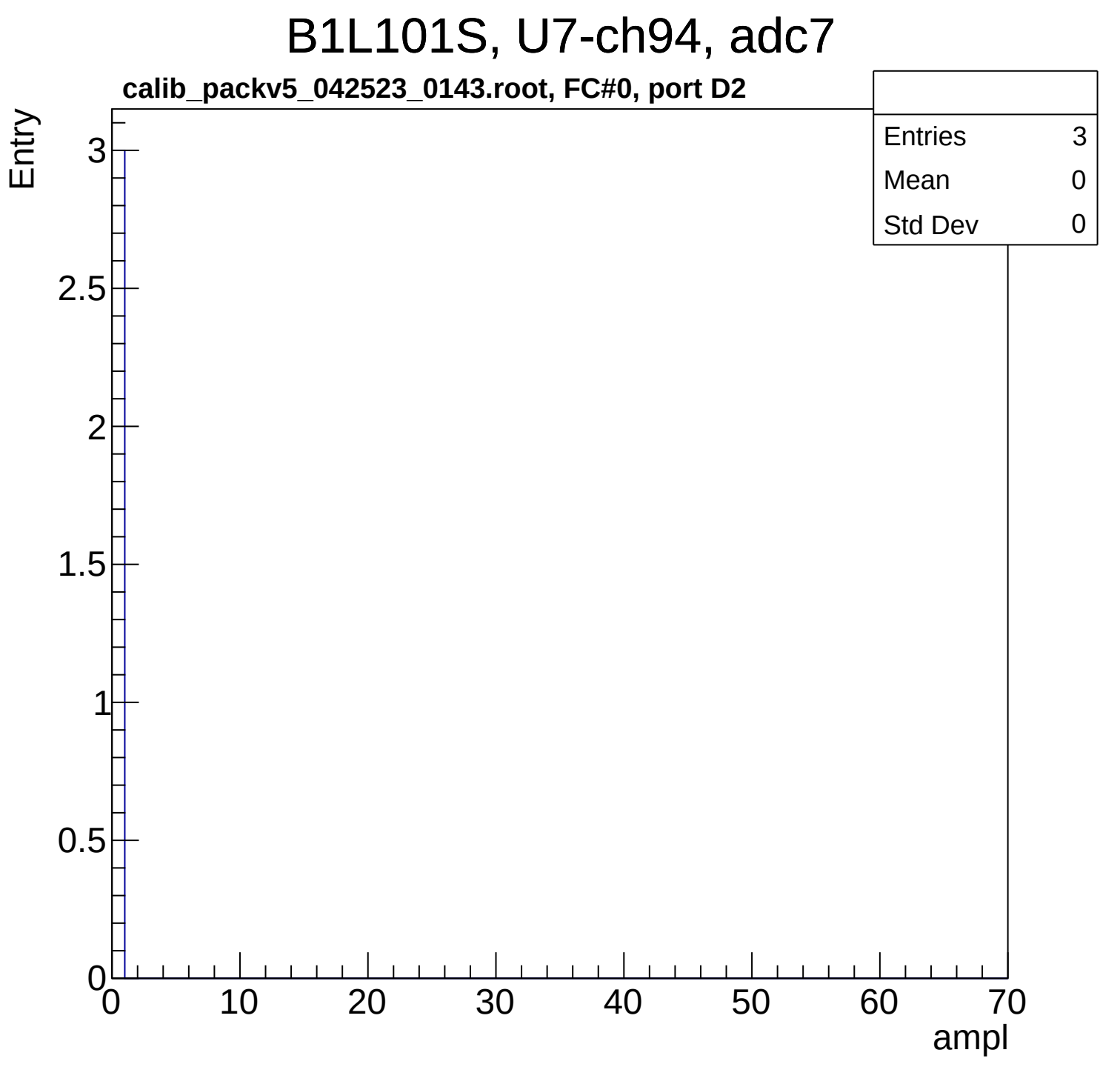
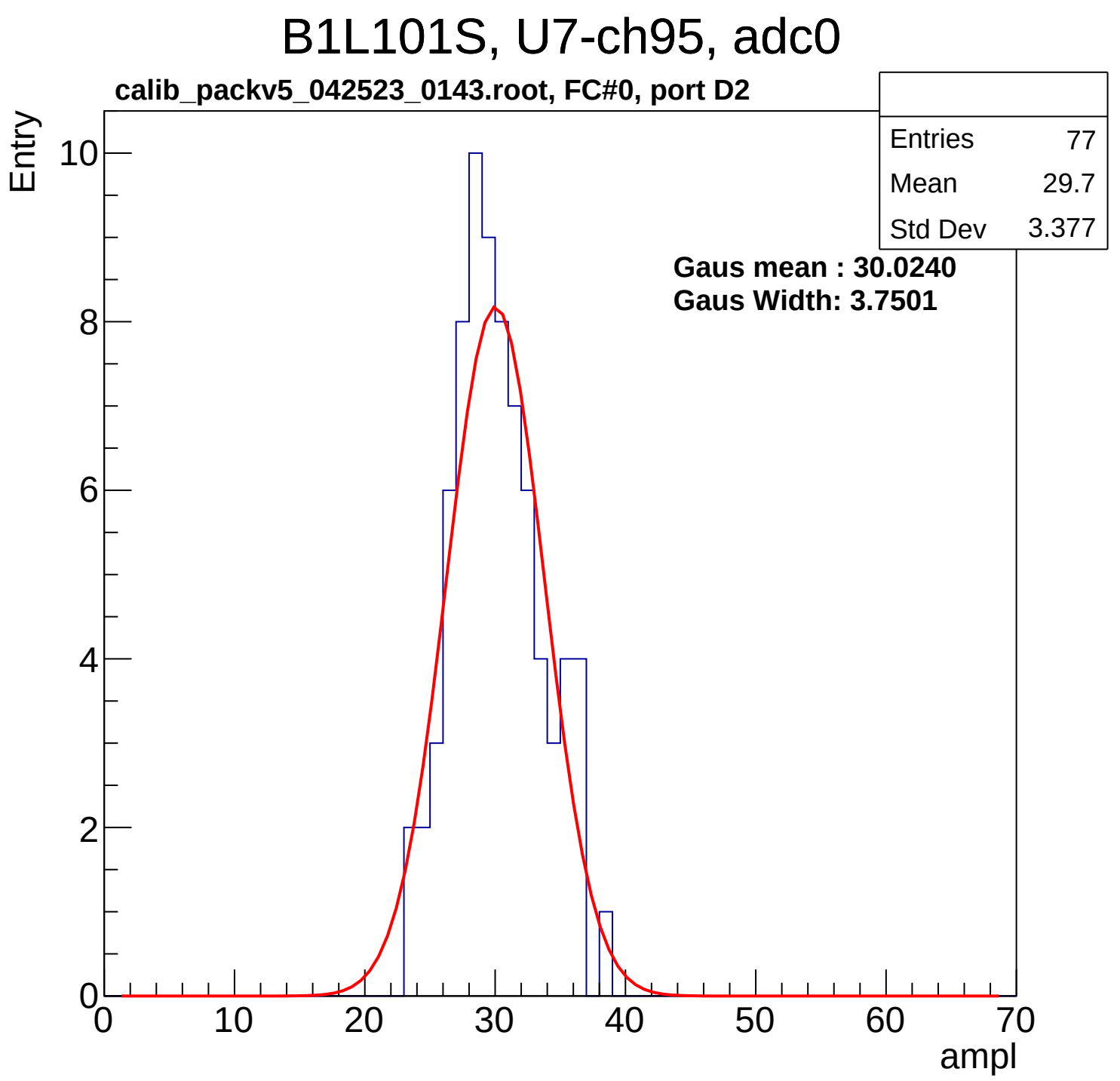
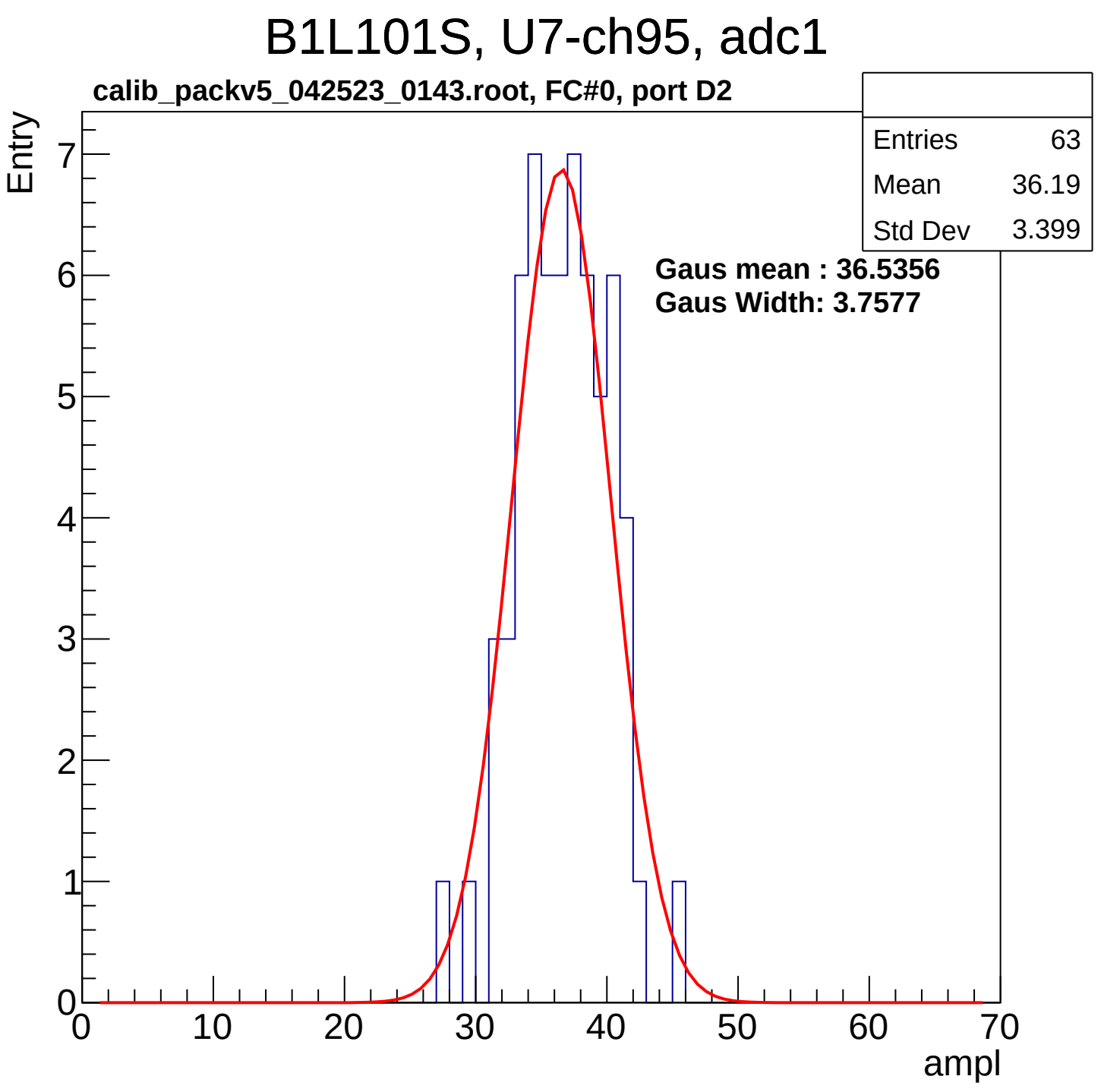
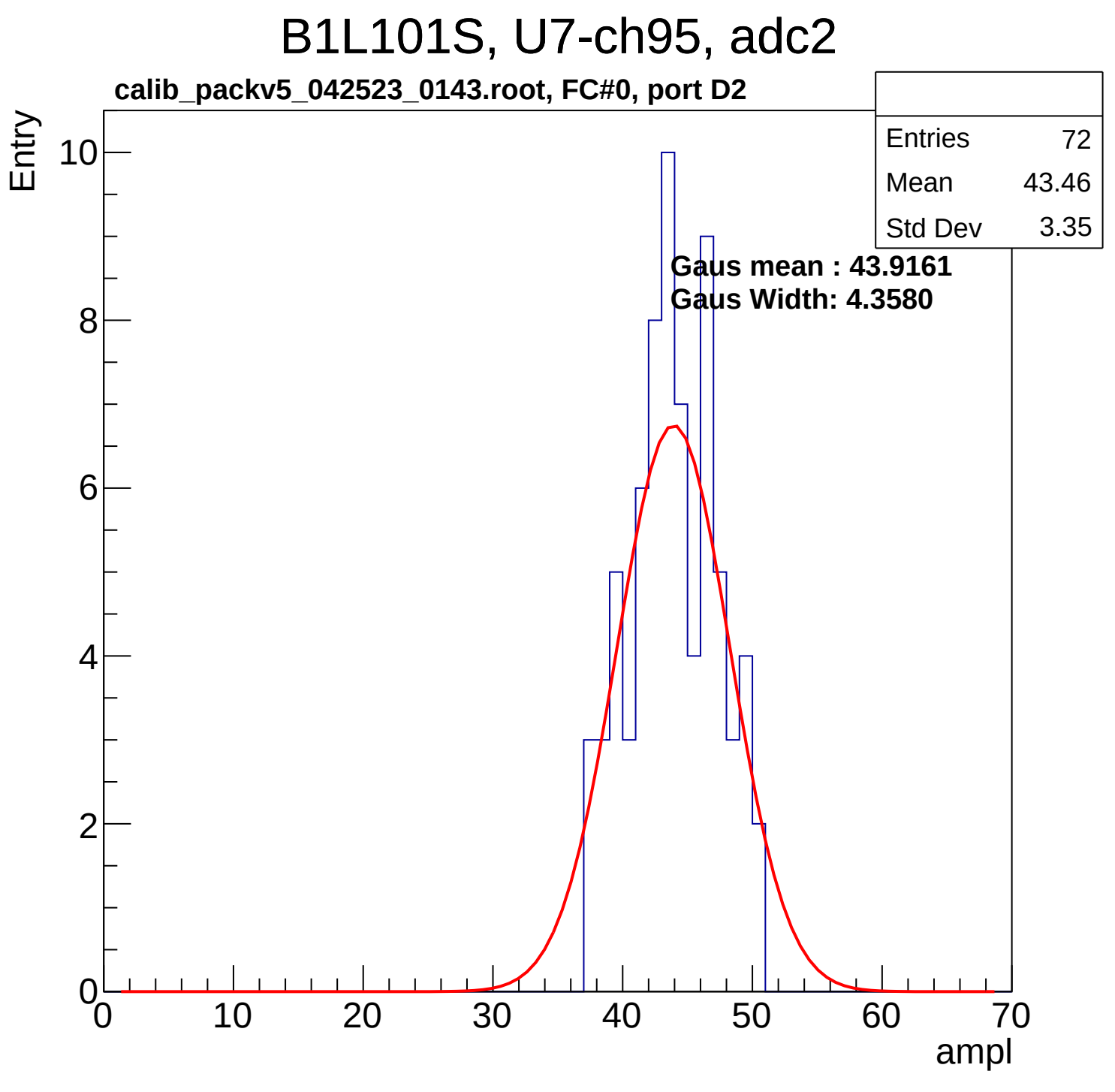
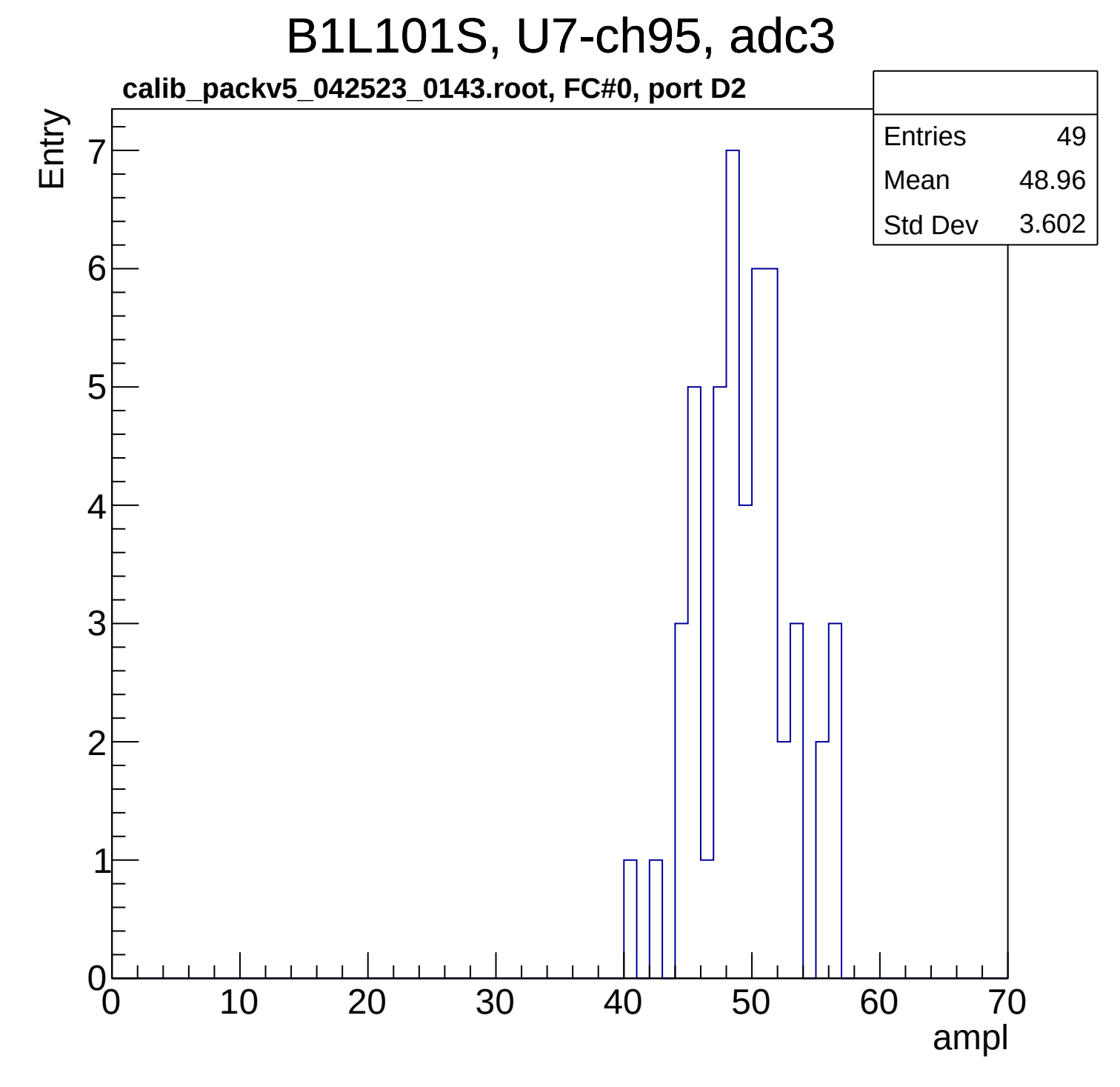

B1L101S, U7-ch94, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 62.83
Std Dev 0.3727
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch94, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 0
Std Dev 0
Entry
3
2.5
2
1.5
1
0.5
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch95, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 29.7
Std Dev 3.377
Gaus mean : 30.0240
Gaus Width: 3.7501
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch95, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 36.19
Std Dev 3.399
Gaus mean : 36.5356
Gaus Width: 3.7577
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U7-ch95, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 43.46
Std Dev 3.35
Gaus mean : 43.9161
Gaus Width: 4.3580
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch95, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 48.96
Std Dev 3.602
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
50
60
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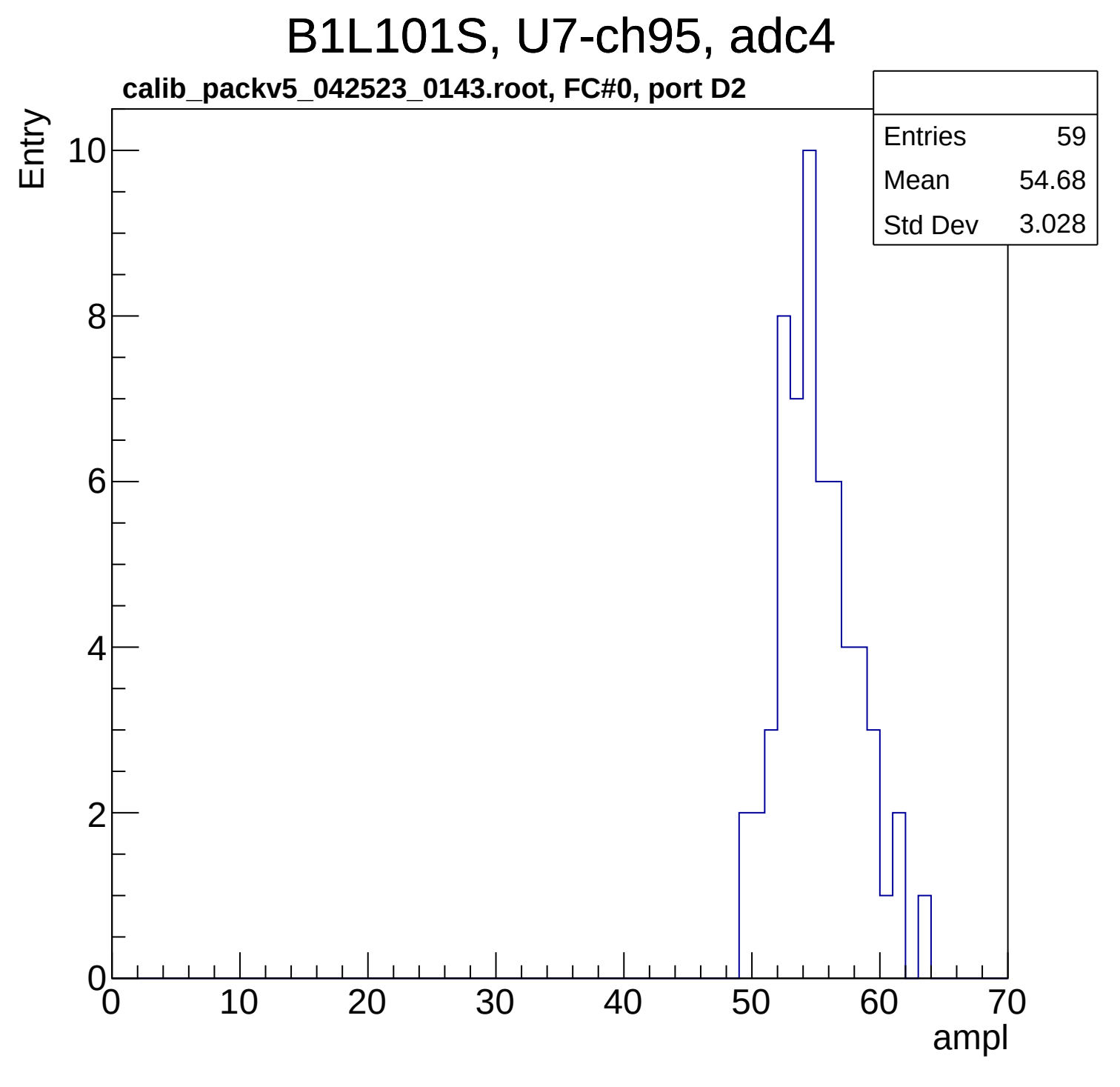
B1L101S, U7-ch95, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 54.68
Std Dev 3.028
Entry
ampl
0
2
4
6
8
10
0
10
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30
40
50
60
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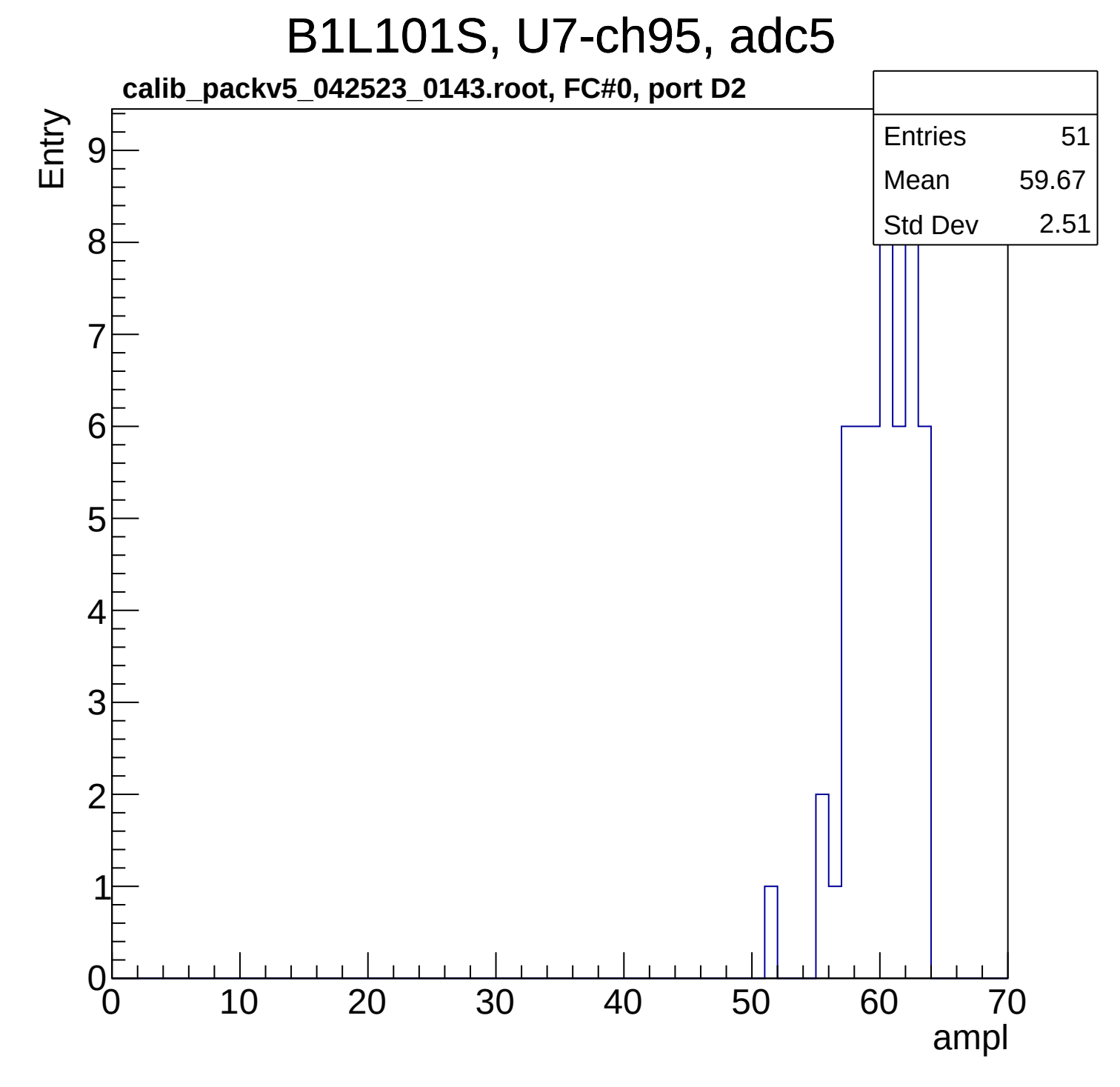
B1L101S, U7-ch95, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 59.67
Std Dev 2.51
Entry
ampl
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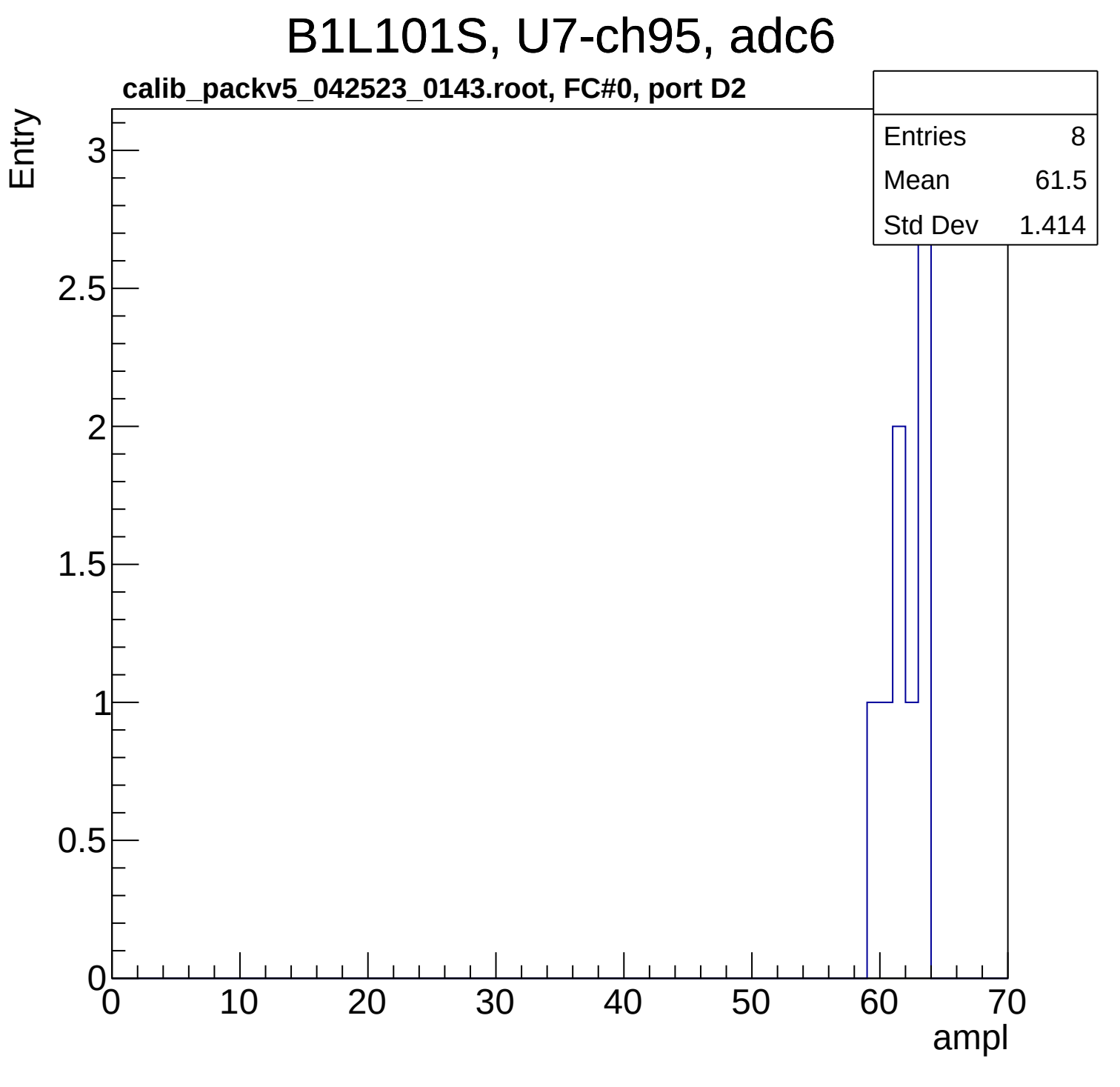
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch95, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 61.5
Std Dev 1.414
Entry
ampl
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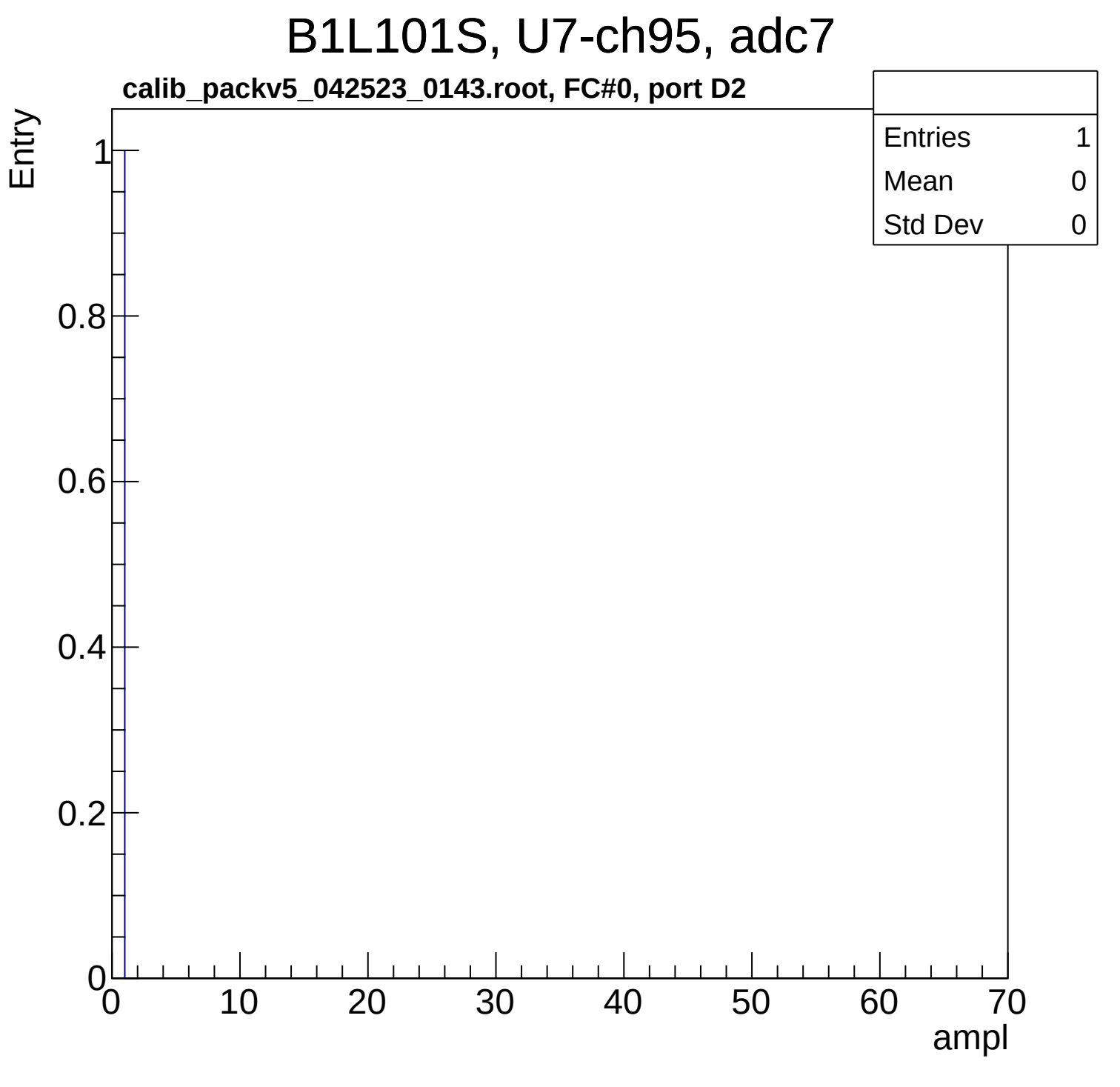
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U7-ch95, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
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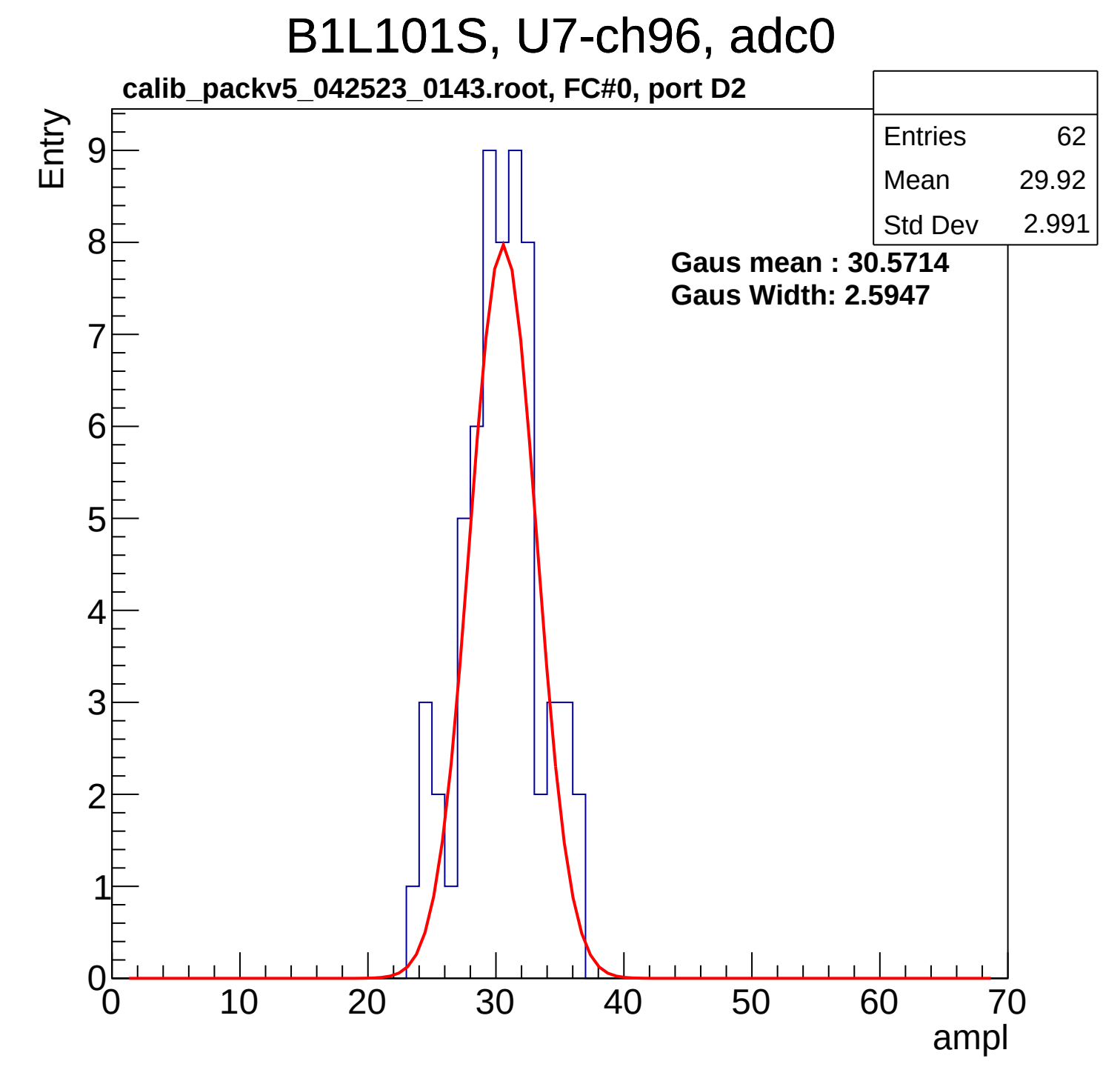
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch96, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 29.92
Std Dev 2.991
Gaus mean : 30.5714
Gaus Width: 2.5947
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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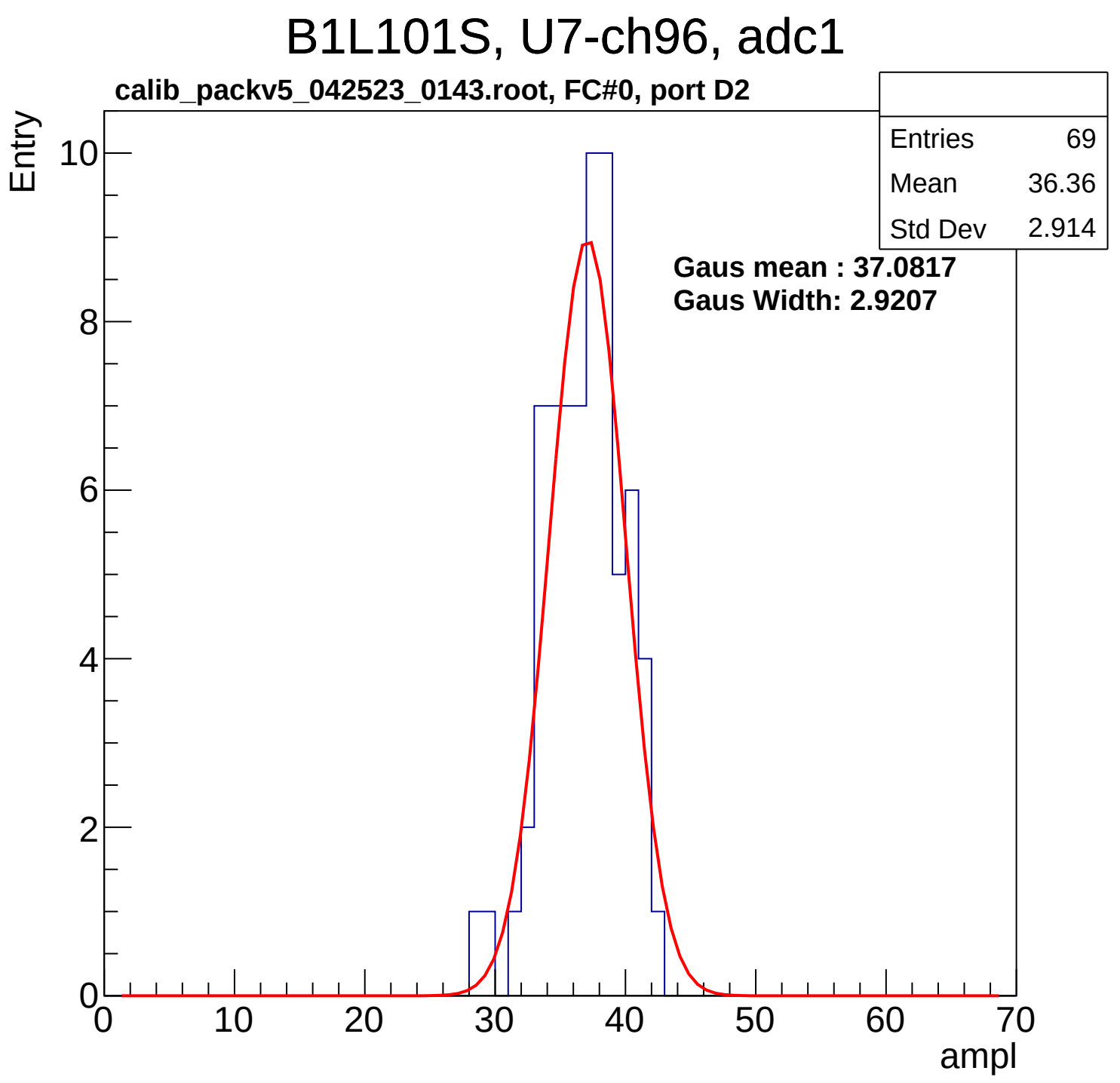
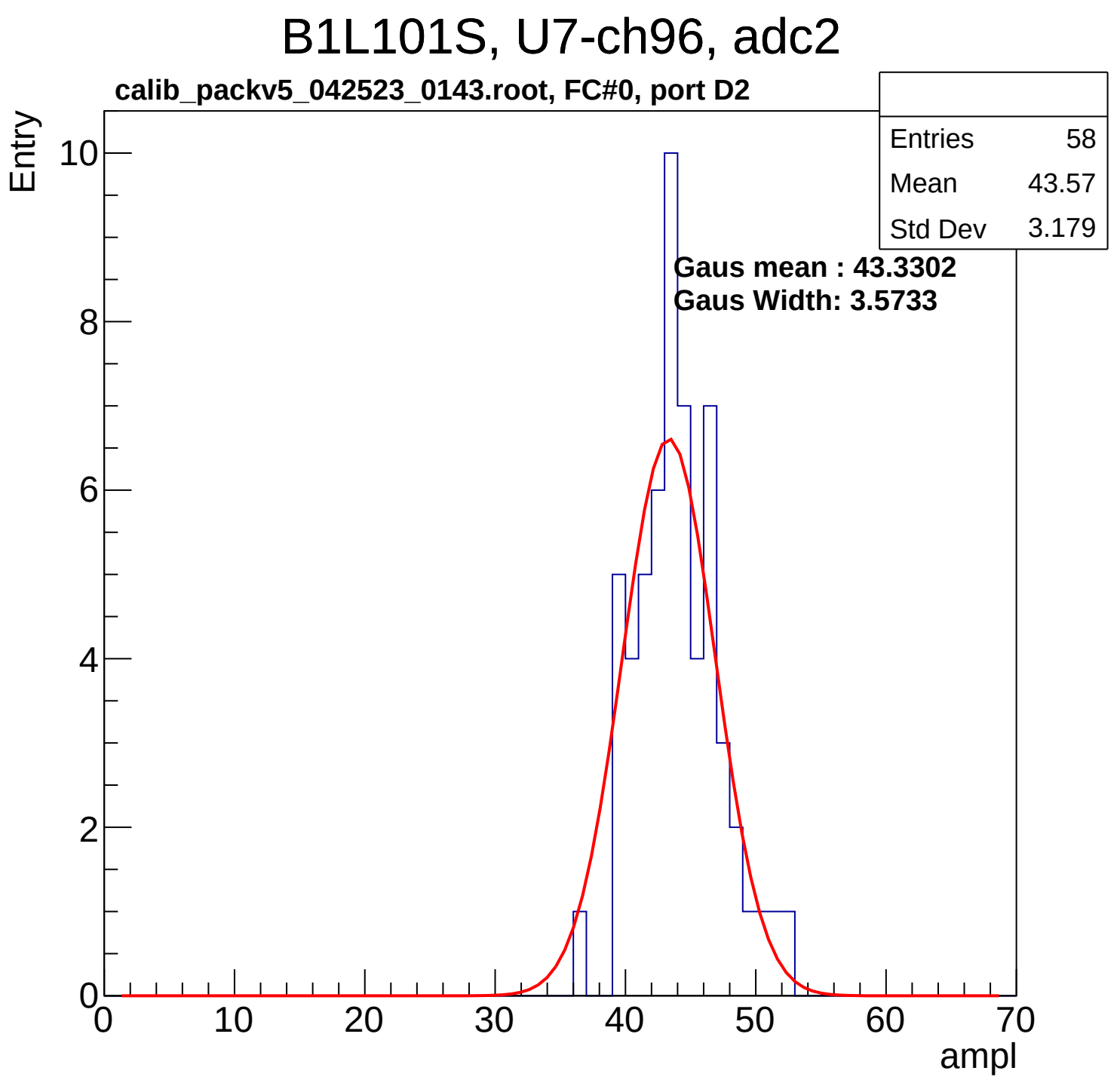
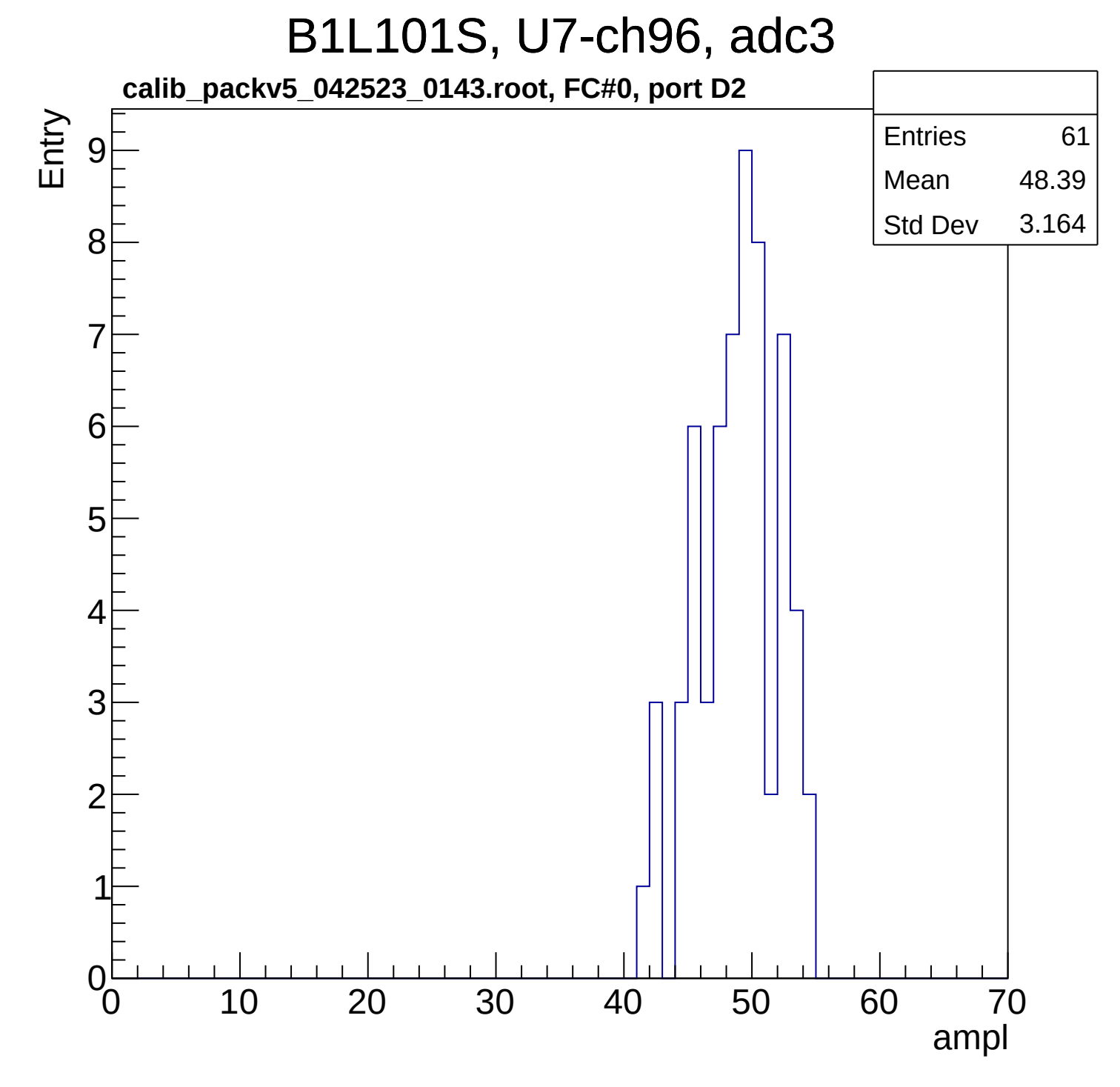

B1L101S, U7-ch96, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 36.36
Std Dev 2.914
Gaus mean : 37.0817
Gaus Width: 2.9207
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch96, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 43.57
Std Dev 3.179
Gaus mean : 43.3302
Gaus Width: 3.5733
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch96, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 48.39
Std Dev 3.164
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
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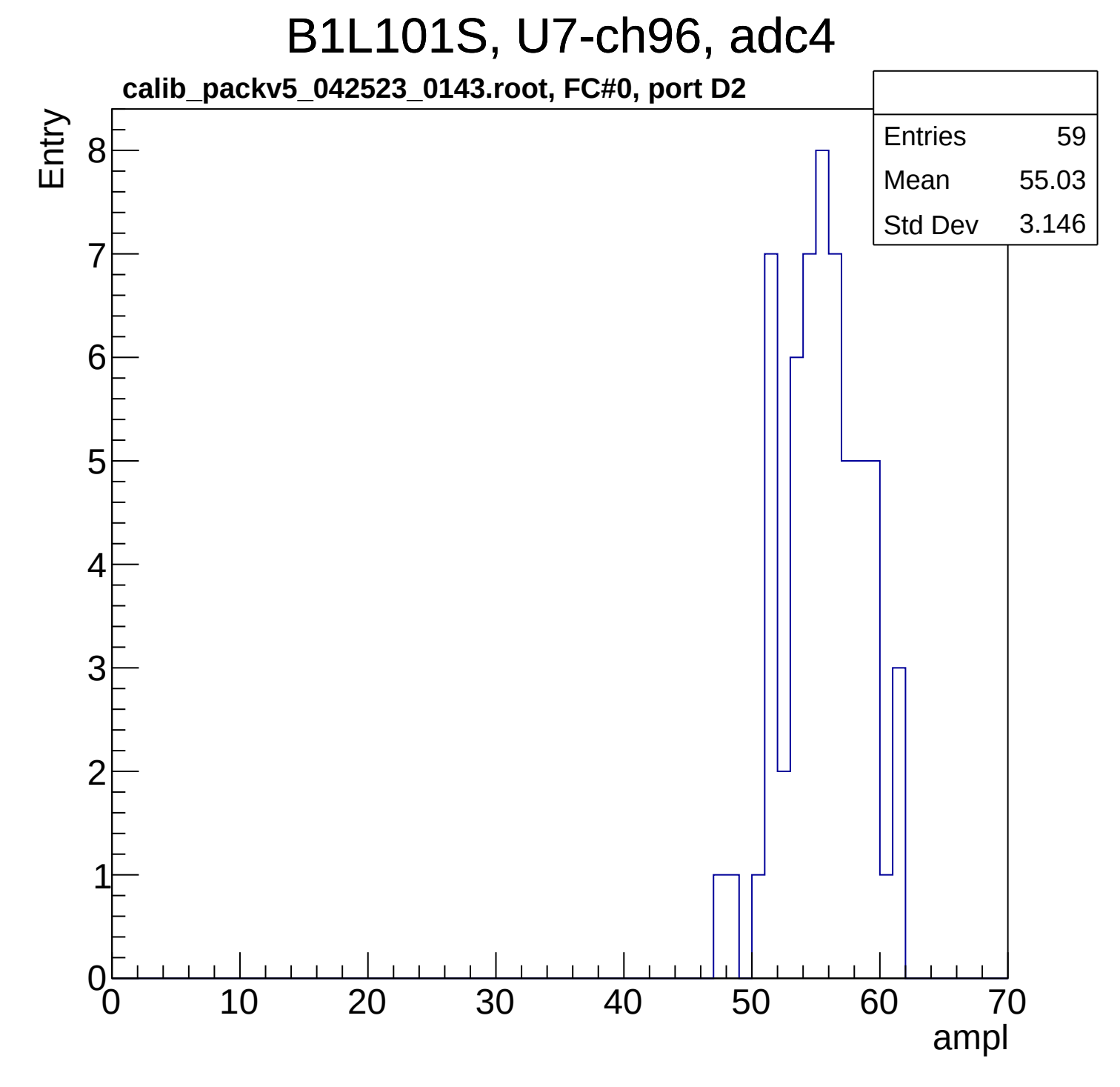
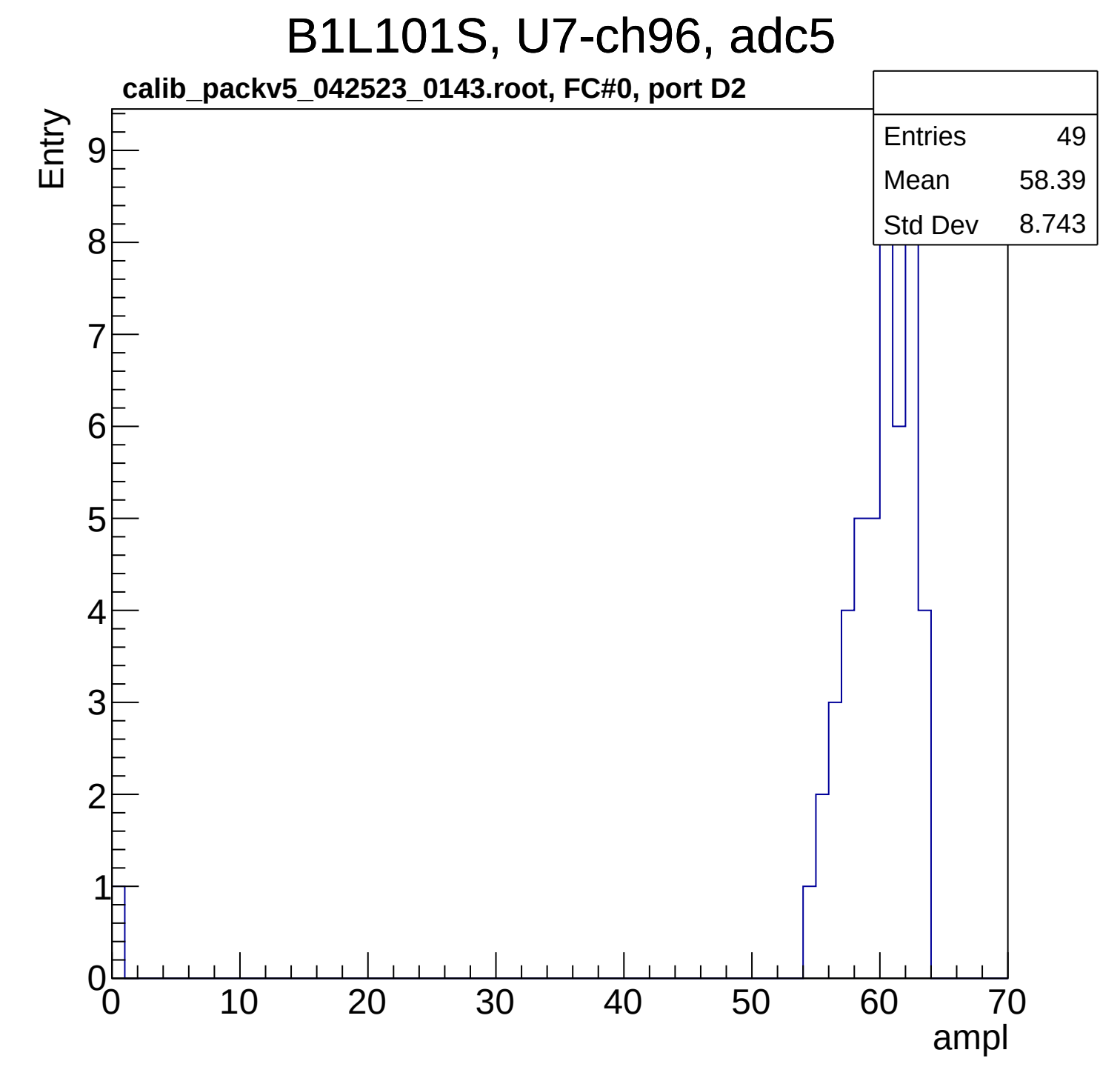

B1L101S, U7-ch96, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 55.03
Std Dev 3.146
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch96, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 58.39
Std Dev 8.743
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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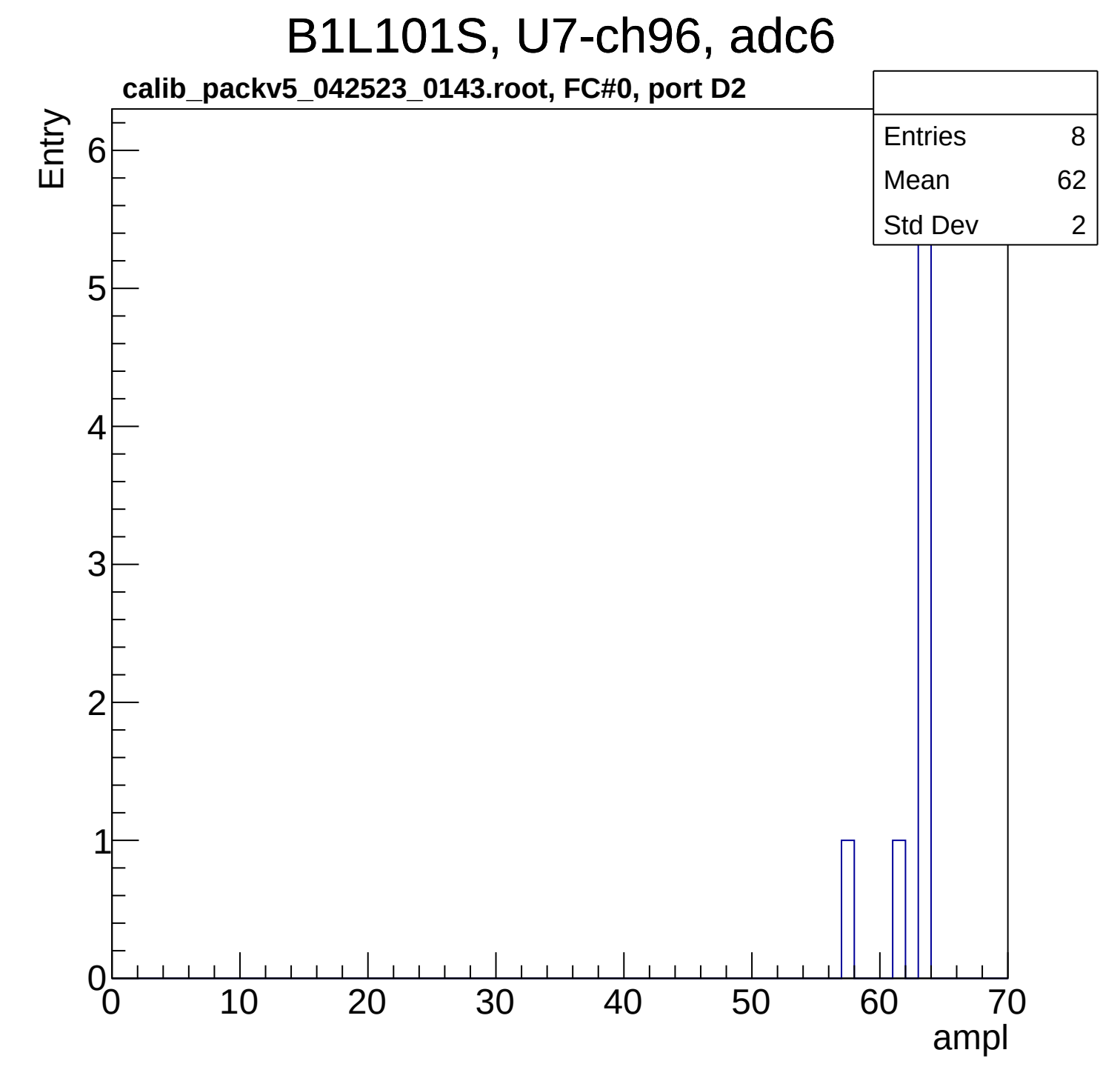
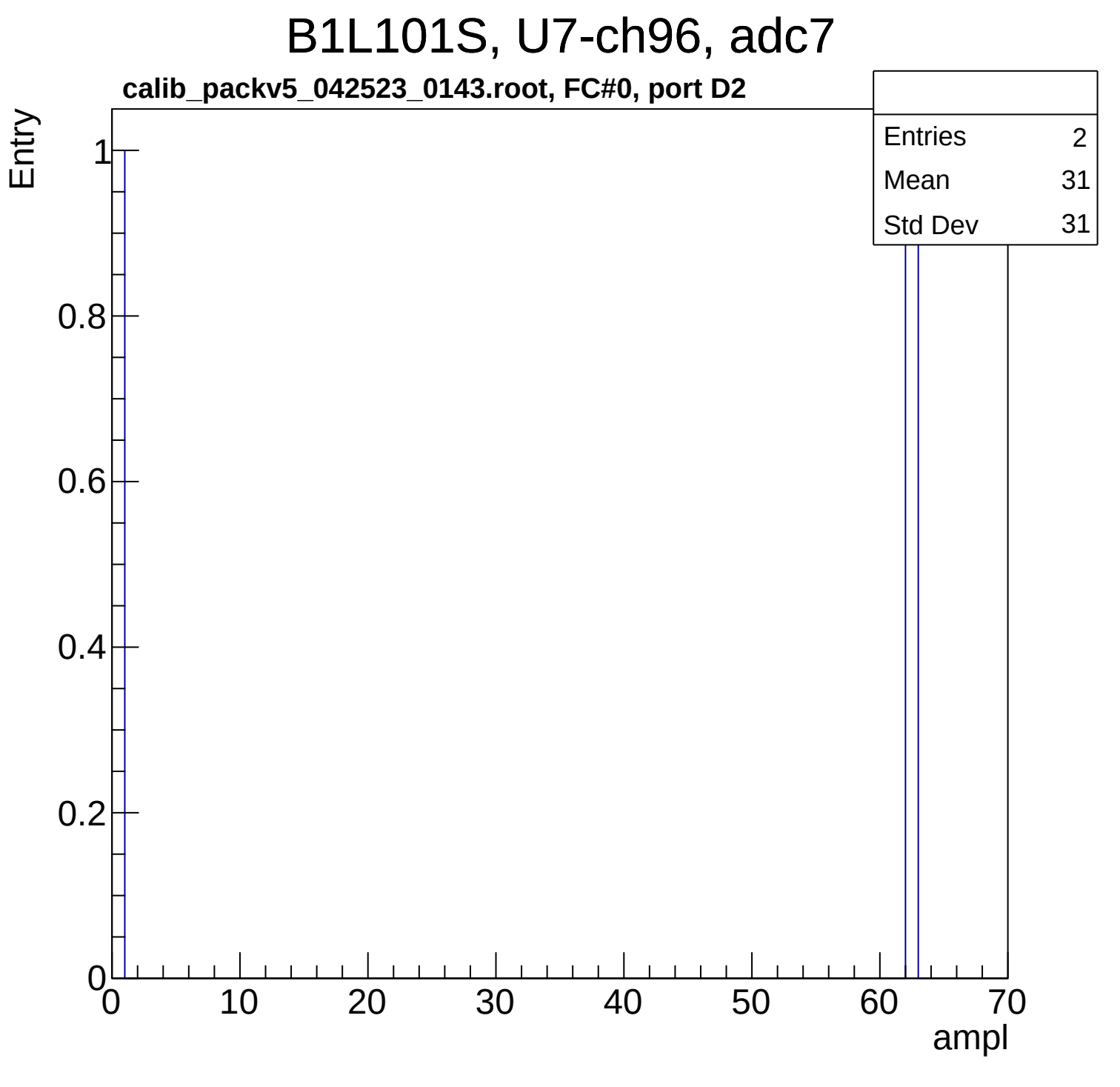
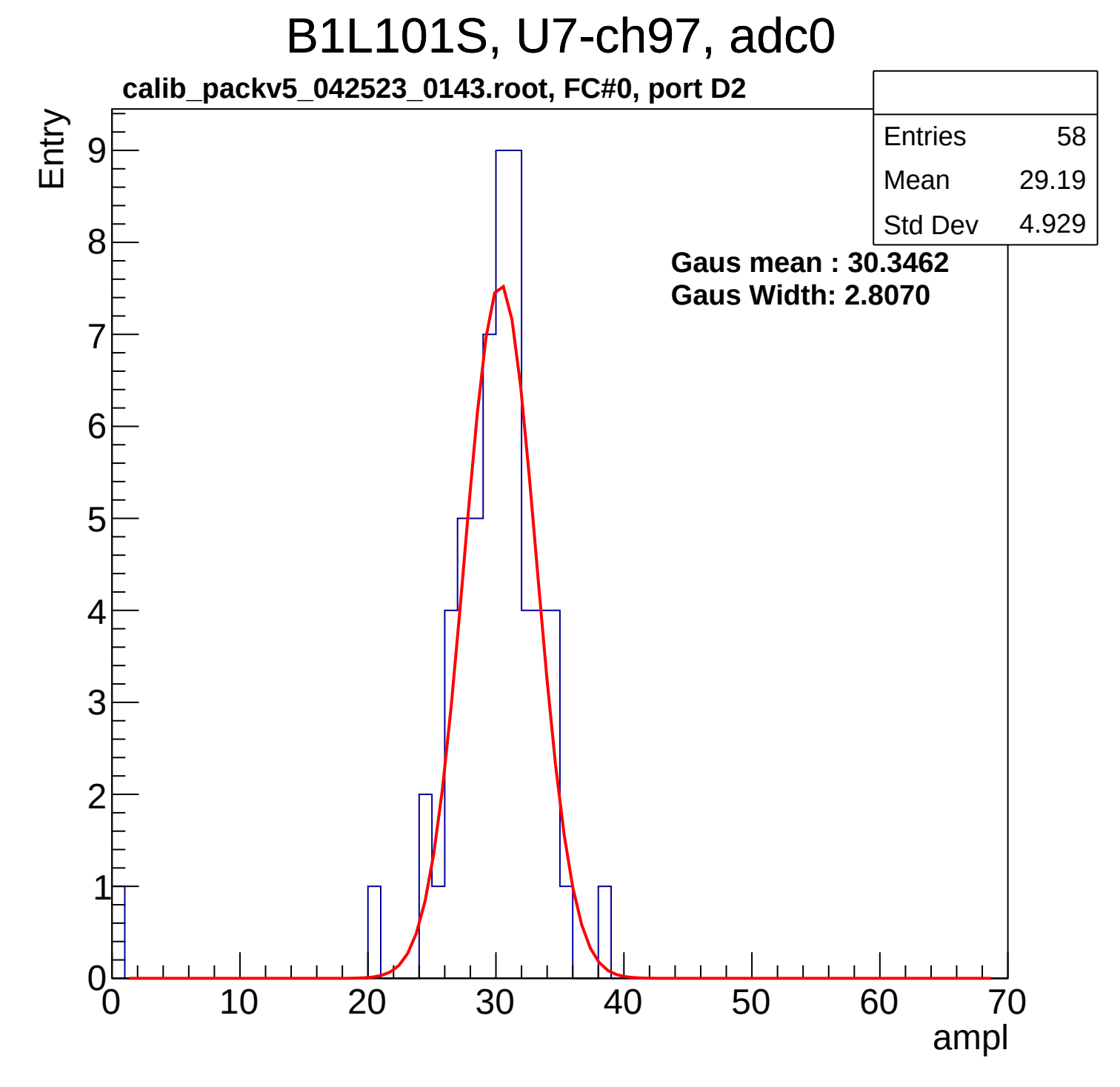
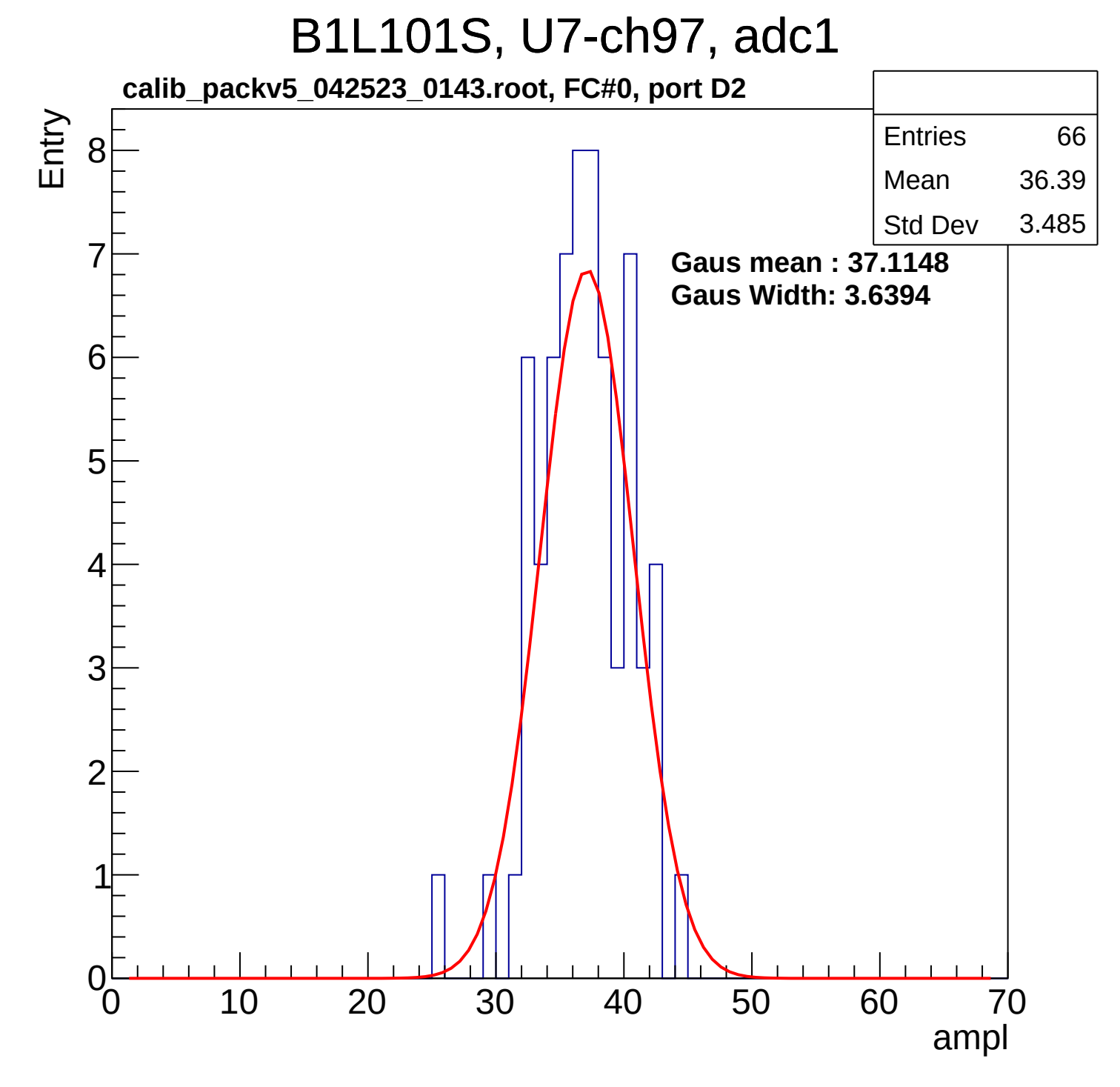
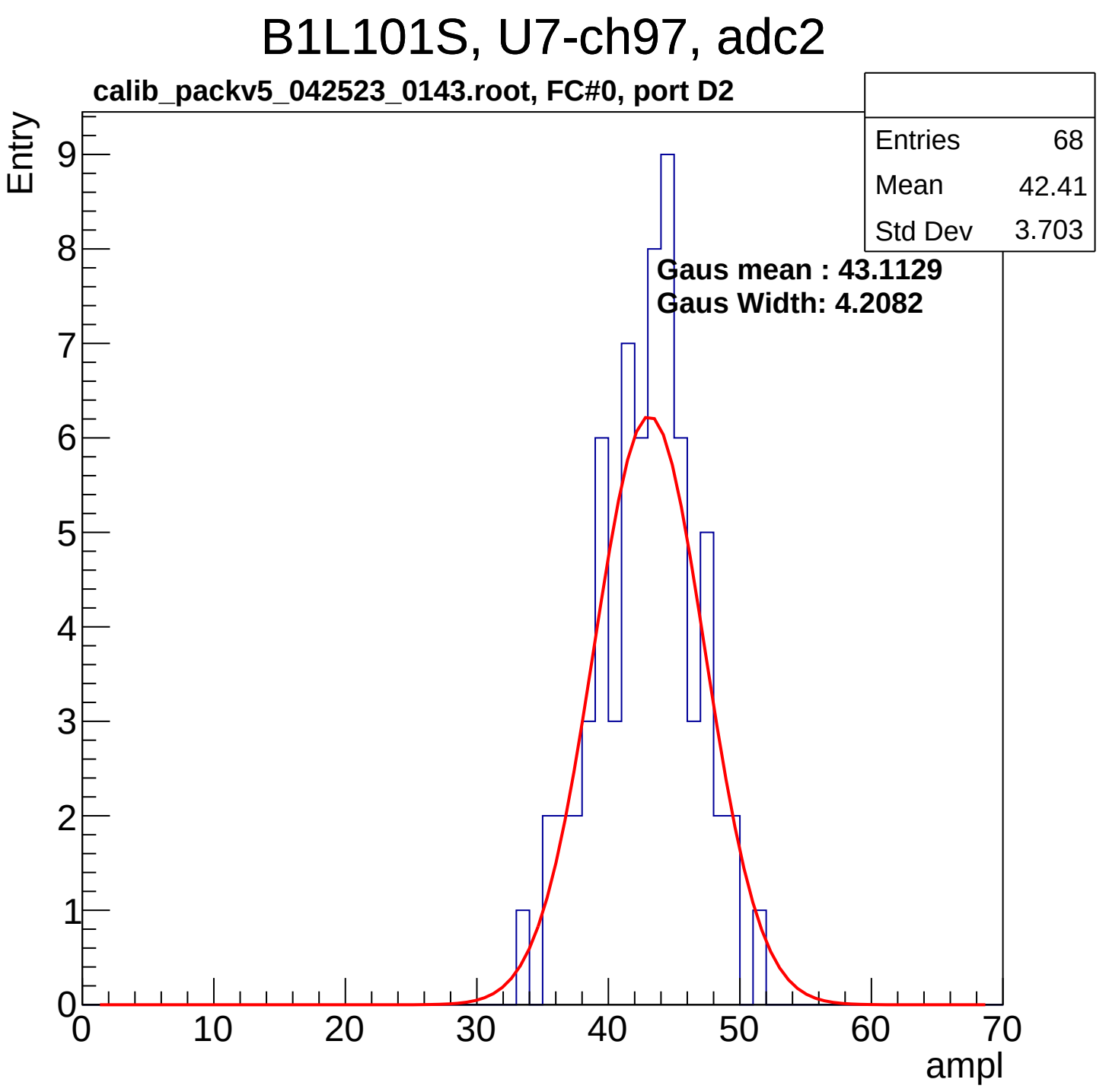
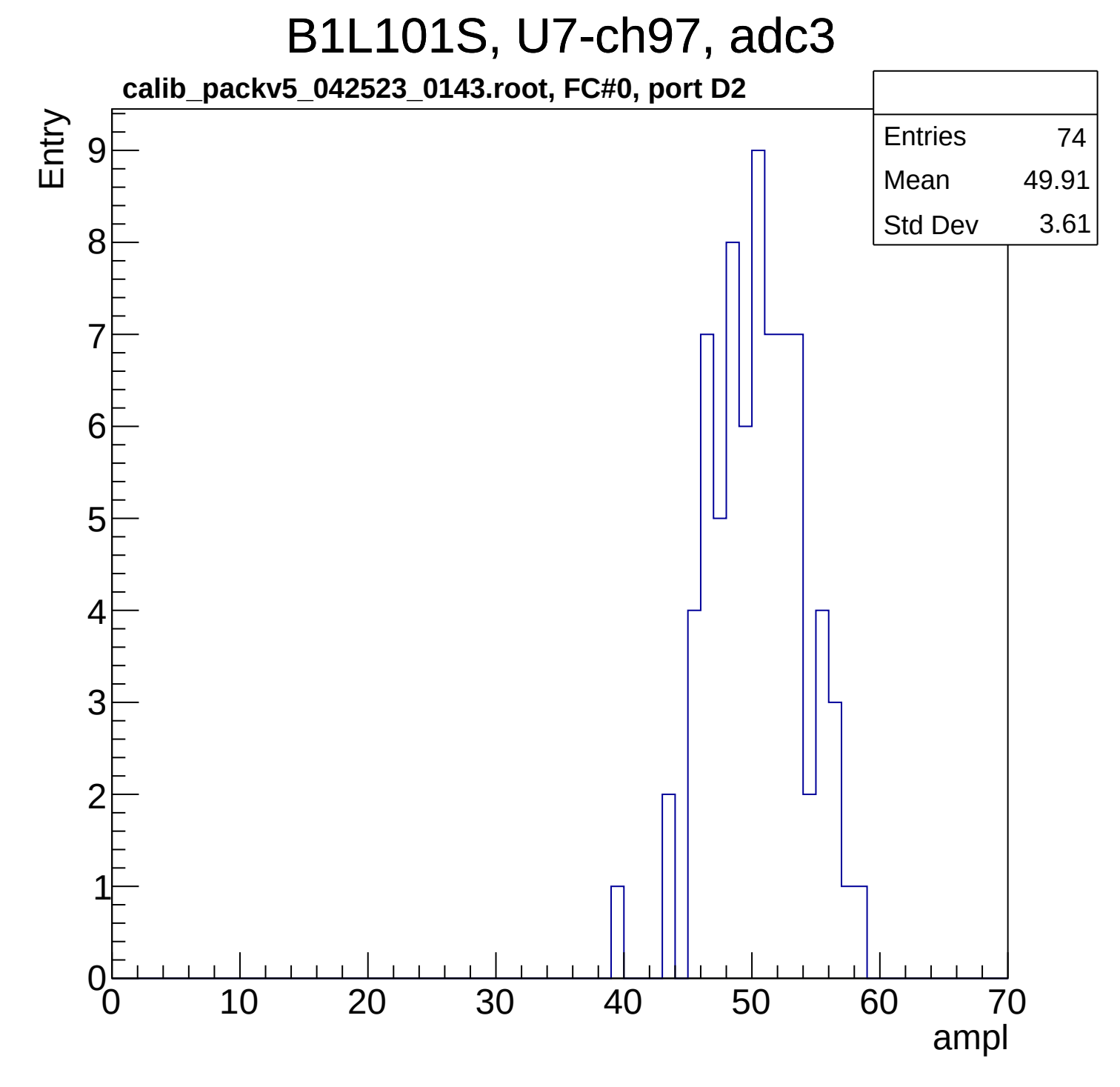

B1L101S, U7-ch96, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 62
Std Dev 2
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

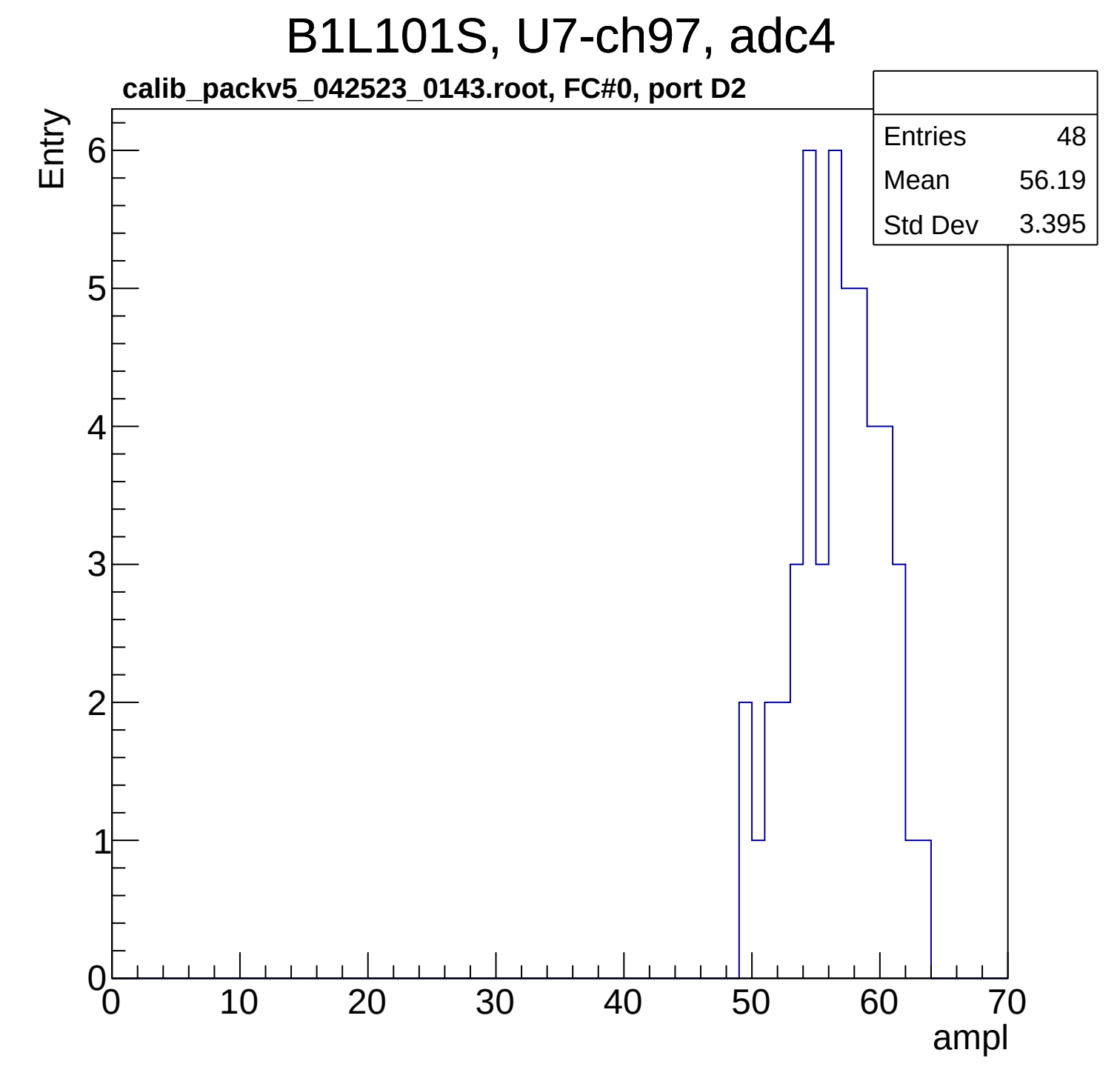

B1L101S, U7-ch96, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 31
Std Dev 31
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

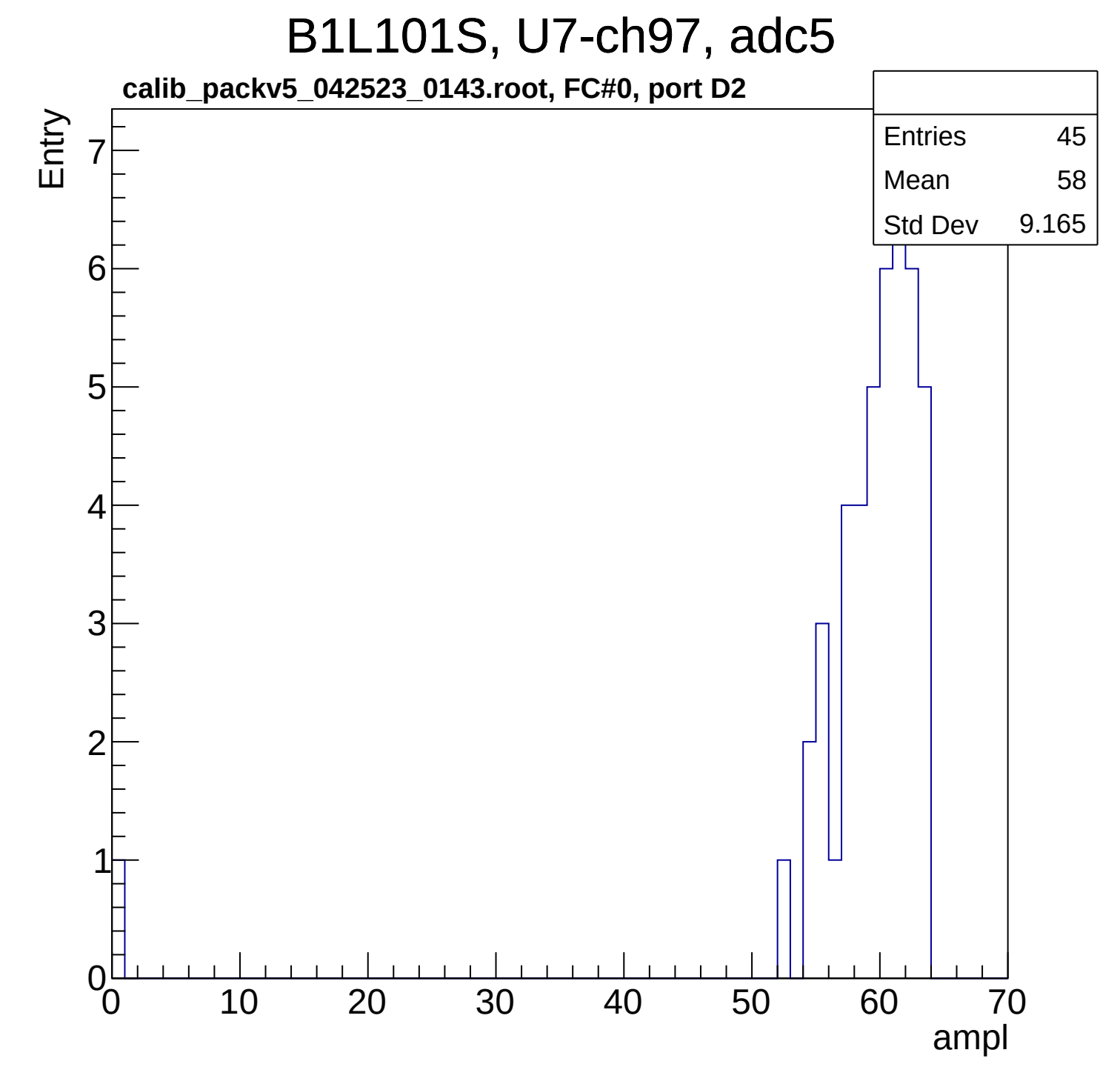

B1L101S, U7-ch97, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 29.19
Std Dev 4.929
Gaus mean : 30.3462
Gaus Width: 2.8070
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch97, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 36.39
Std Dev 3.485
Gaus mean : 37.1148
Gaus Width: 3.6394
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch97, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 42.41
Std Dev 3.703
Gaus mean : 43.1129
Gaus Width: 4.2082
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch97, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 49.91
Std Dev 3.61
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch97, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 56.19
Std Dev 3.395
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L101S, U7-ch97, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 58
Std Dev 9.165
Entry
ampl
0
1
2
3
4
5
6
7
0
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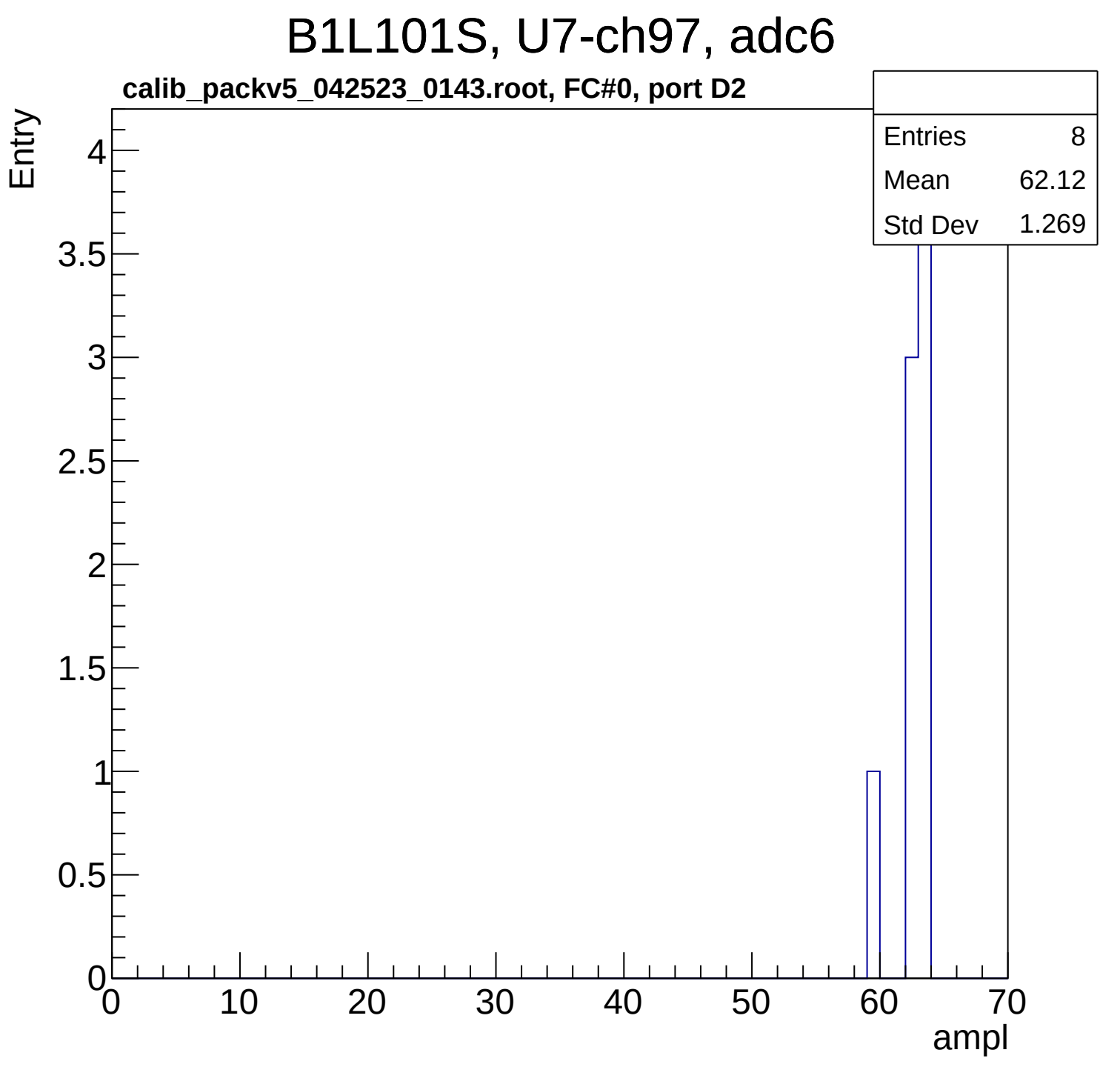
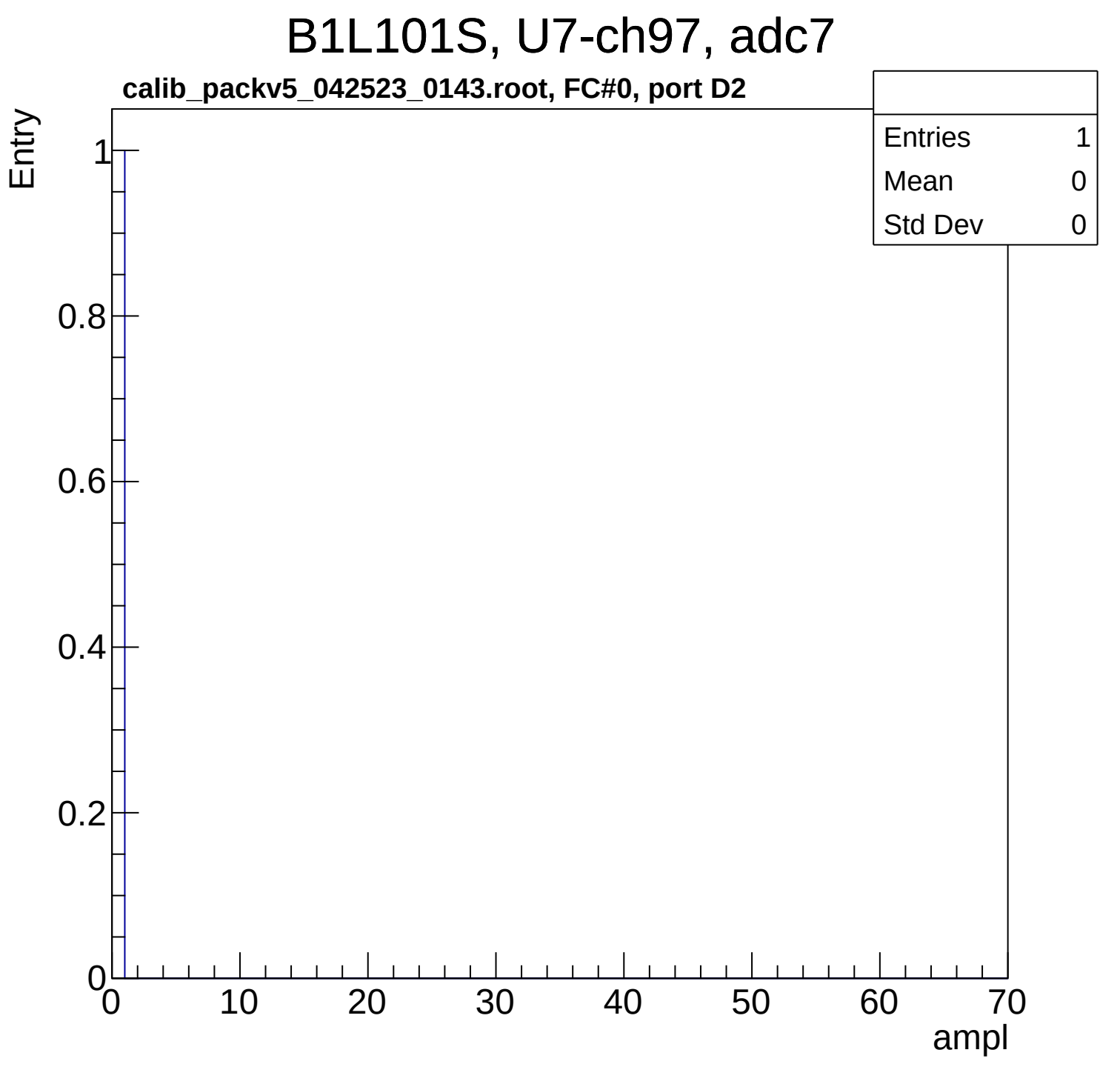
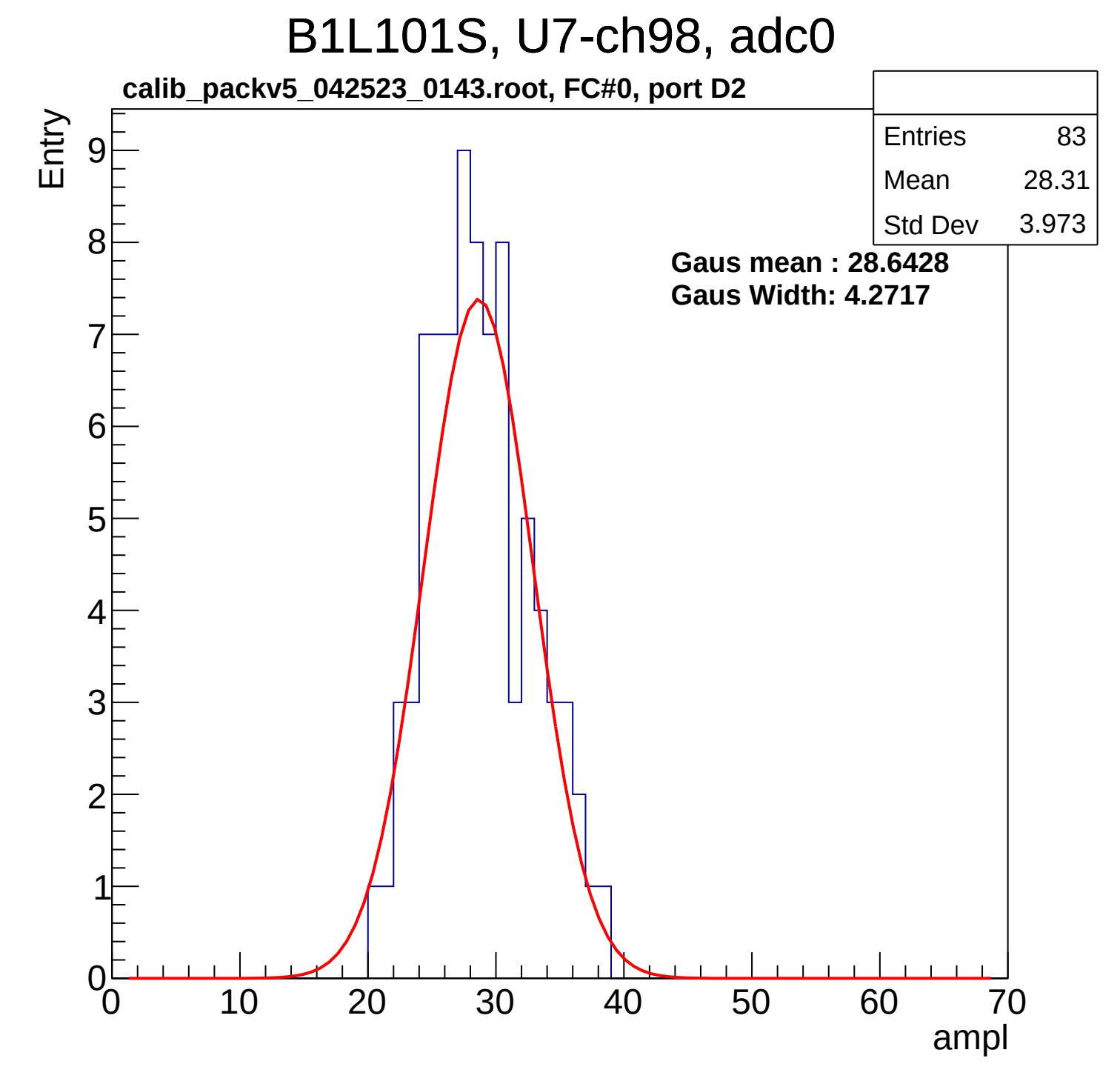
20
30
40
50
60
70


B1L101S, U7-ch97, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 62.12
Std Dev 1.269
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L101S, U7-ch97, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch98, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 83
Mean 28.31
Std Dev 3.973
Gaus mean : 28.6428
Gaus Width: 4.2717
Entry
ampl
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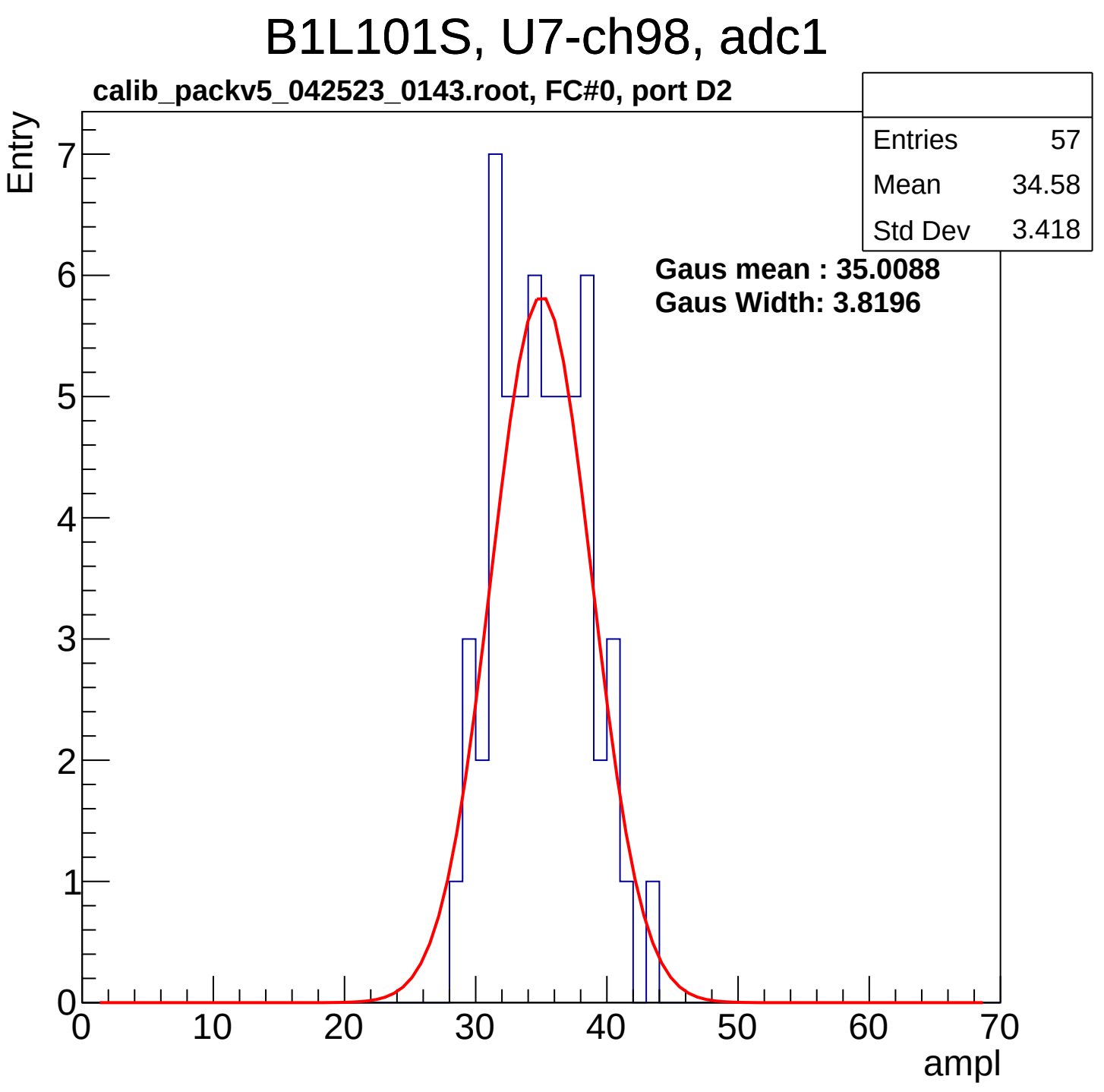
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch98, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 34.58
Std Dev 3.418
Gaus mean : 35.0088
Gaus Width: 3.8196
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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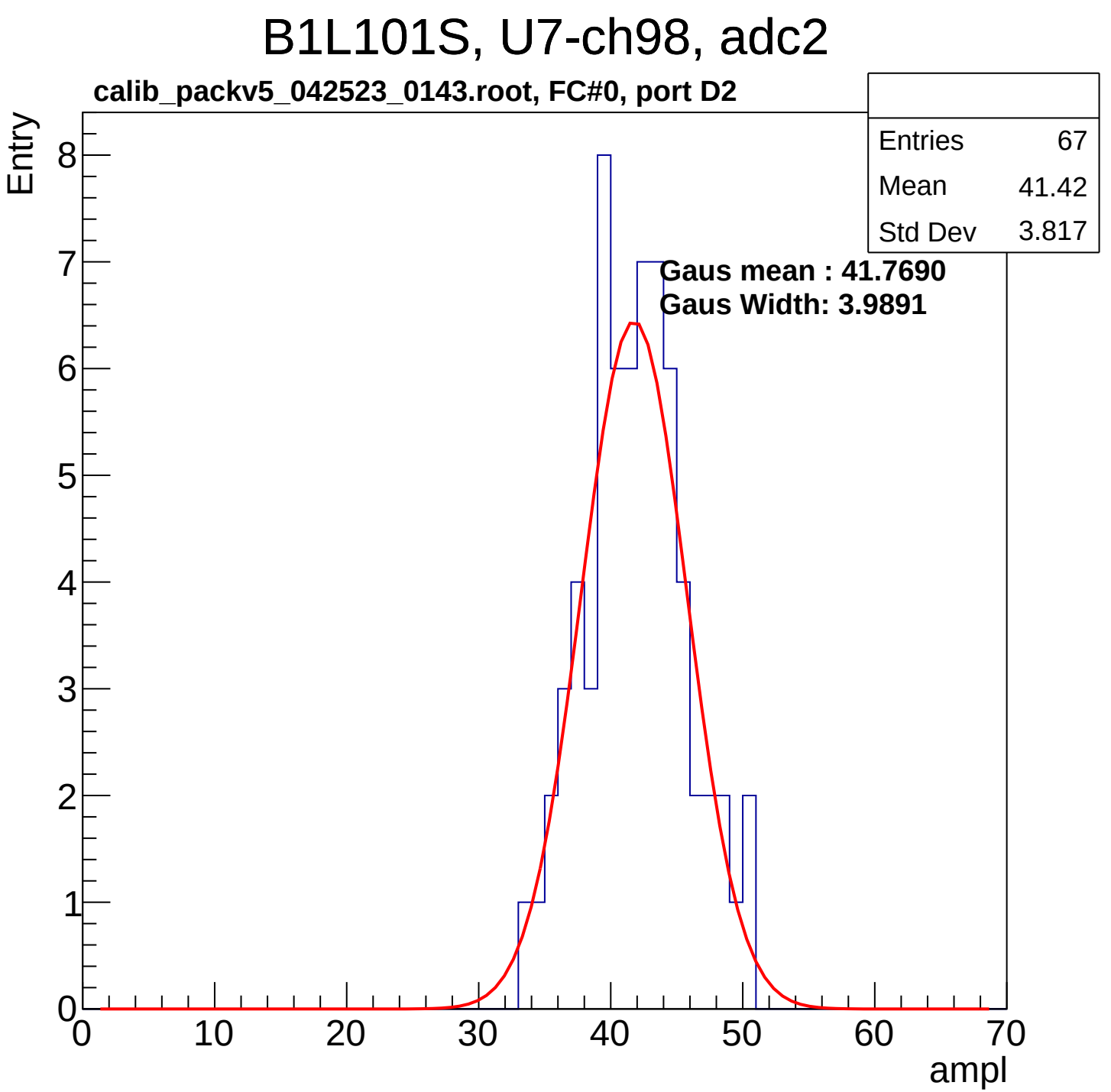
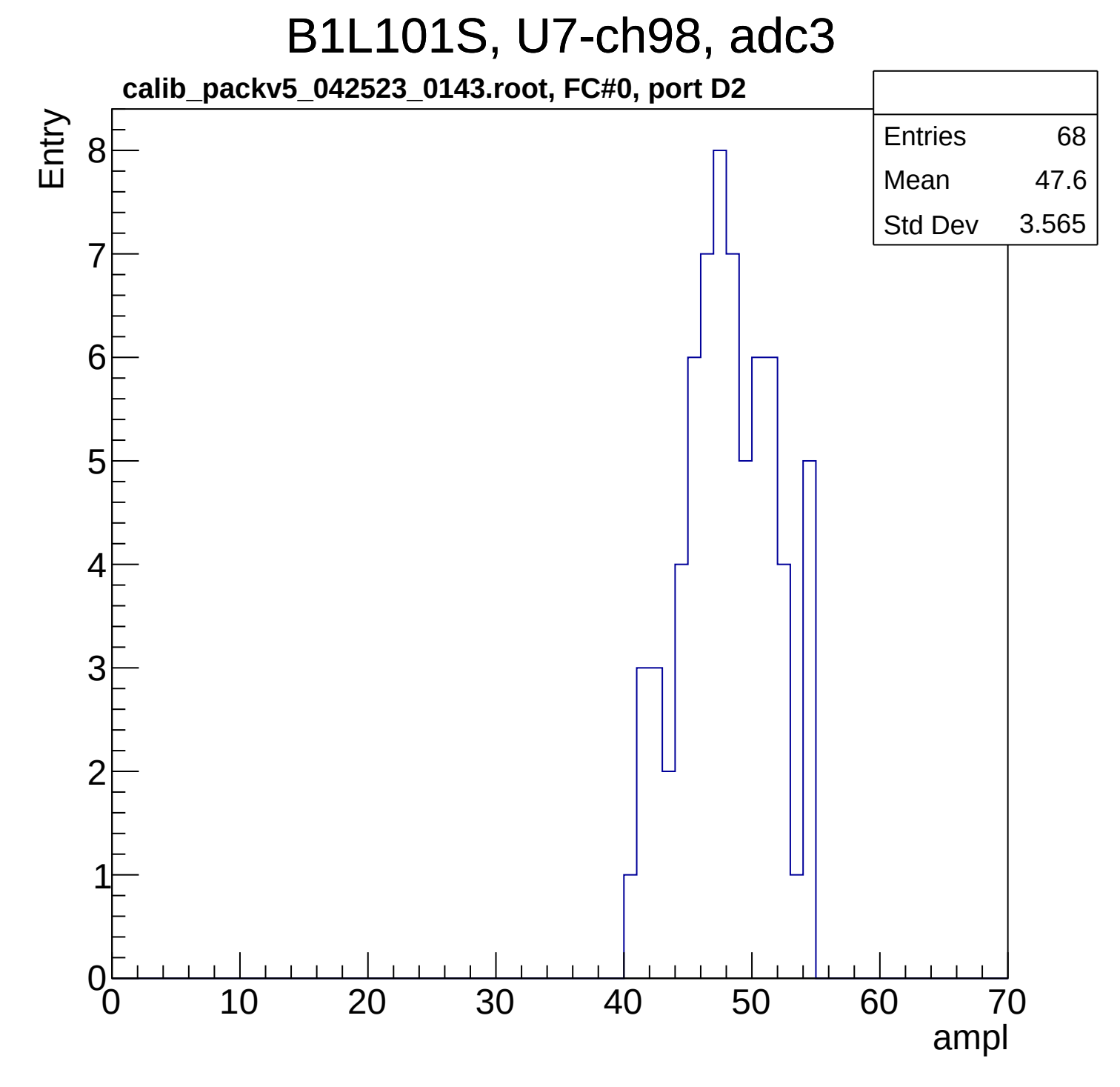
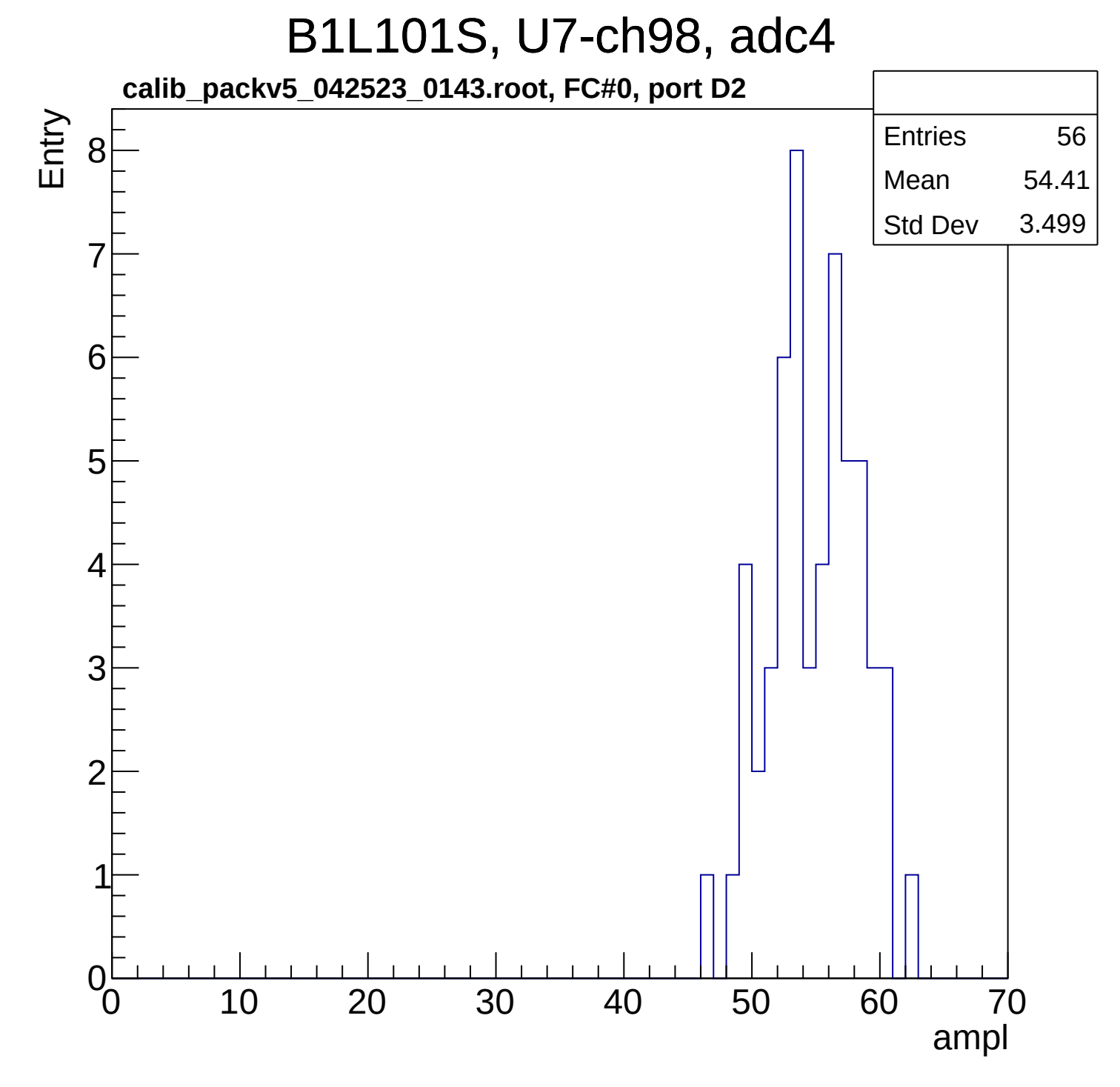

B1L101S, U7-ch98, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 41.42
Std Dev 3.817
Gaus mean : 41.7690
Gaus Width: 3.9891
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch98, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 47.6
Std Dev 3.565
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch98, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 54.41
Std Dev 3.499
Entry
ampl
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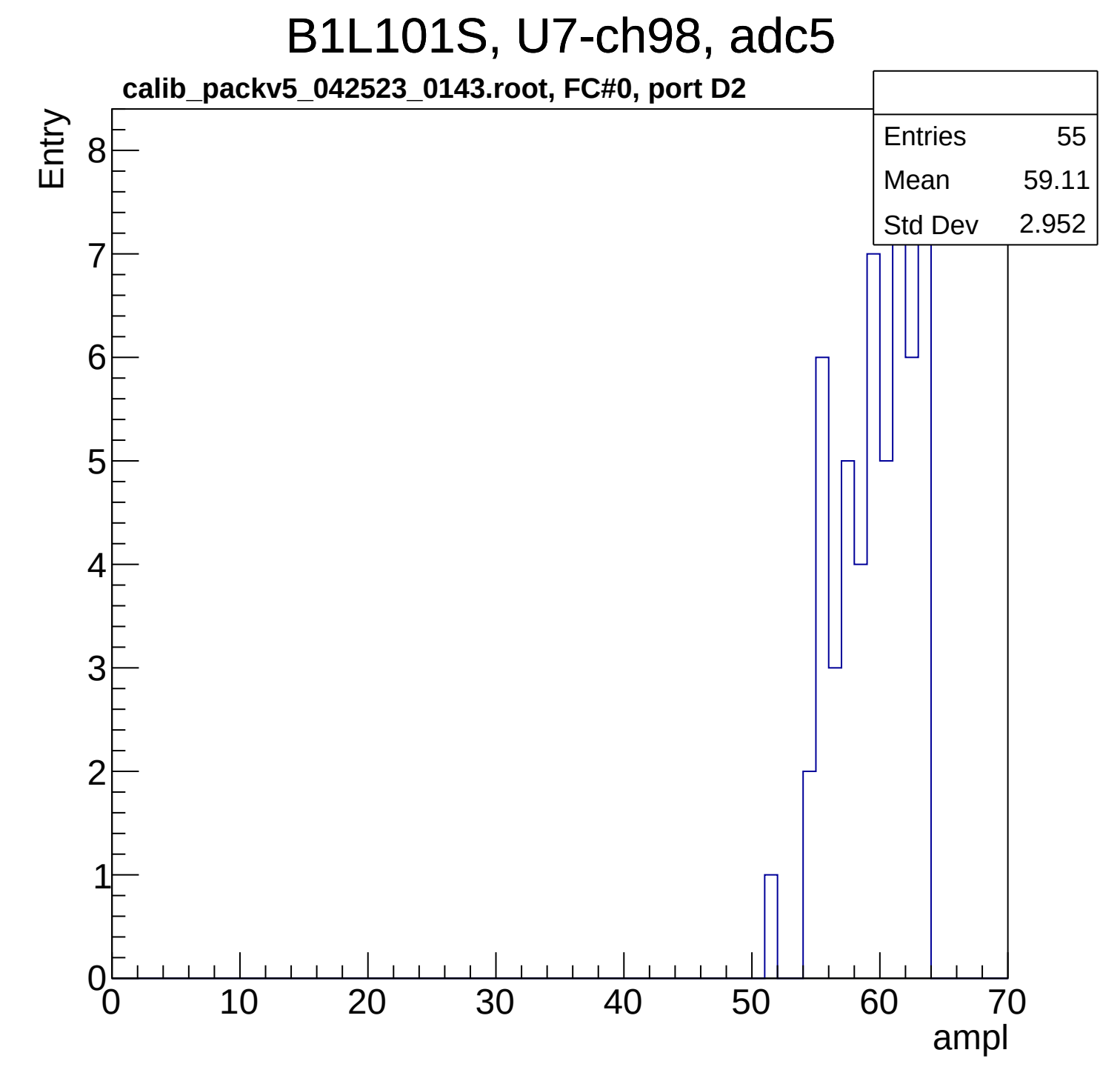
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch98, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 59.11
Std Dev 2.952
Entry
ampl
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1
2
3
4
5
6
7
8
0
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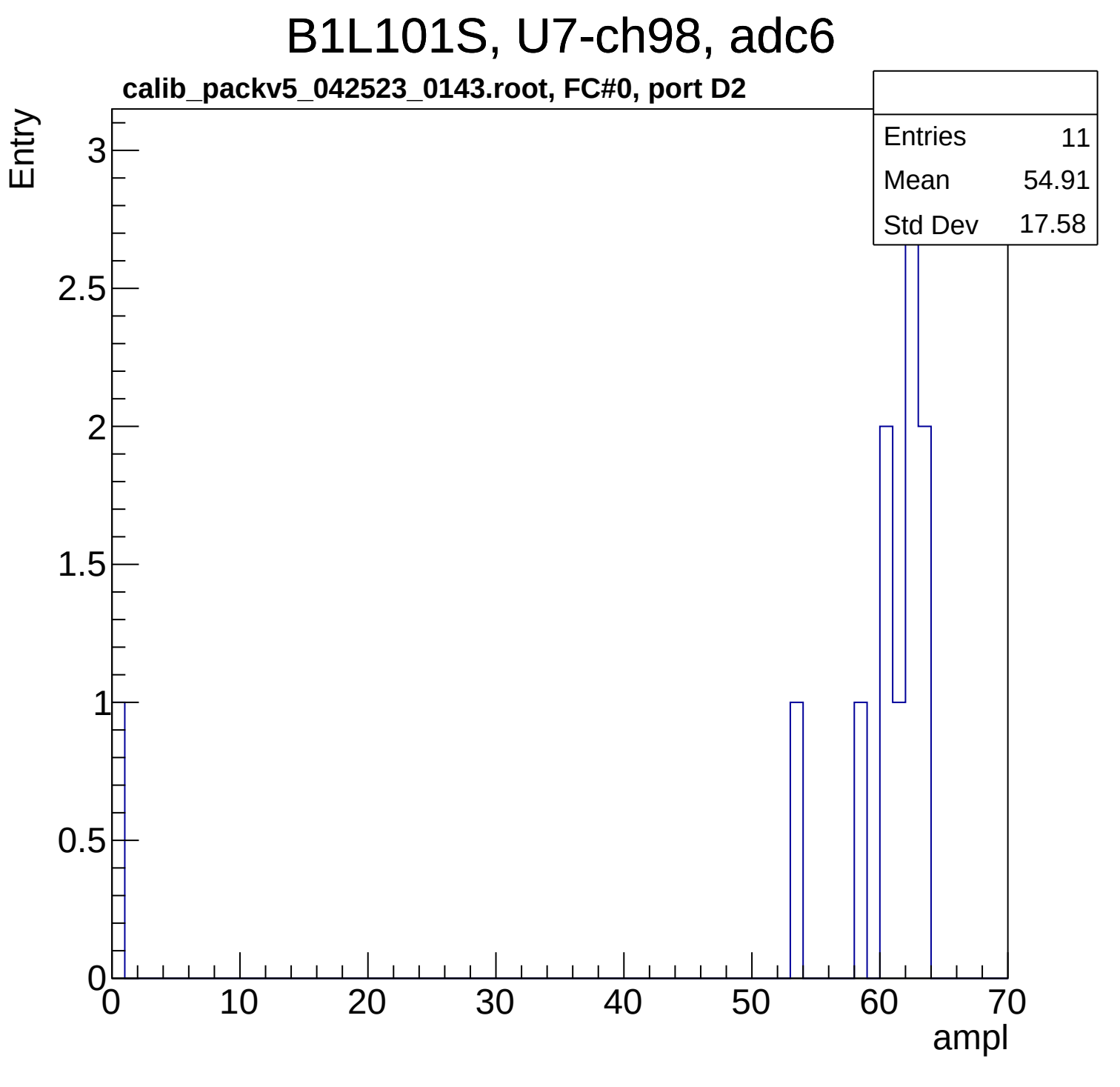
20
30
40
50
60
70


B1L101S, U7-ch98, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 11
Mean 54.91
Std Dev 17.58
Entry
ampl
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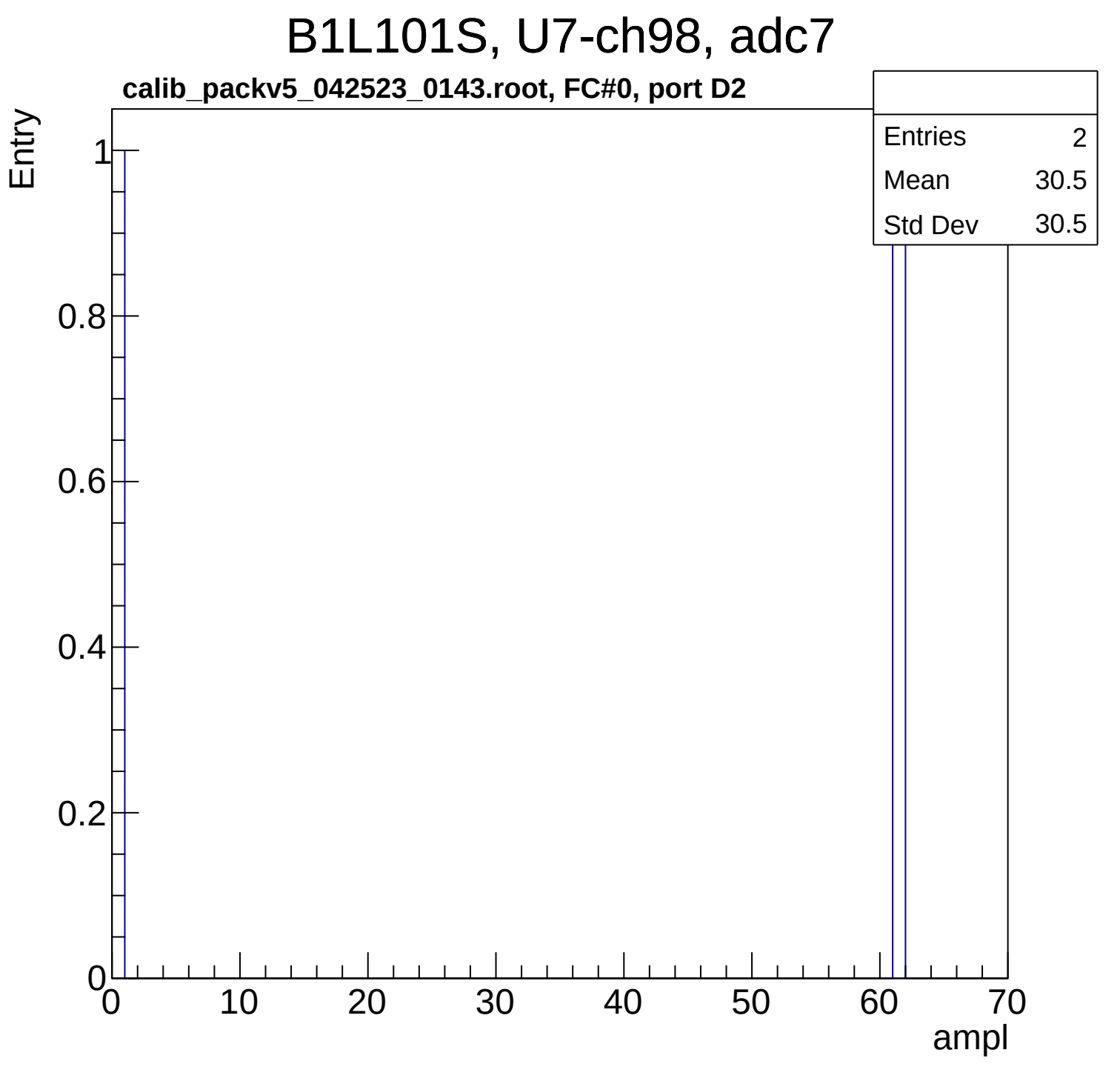
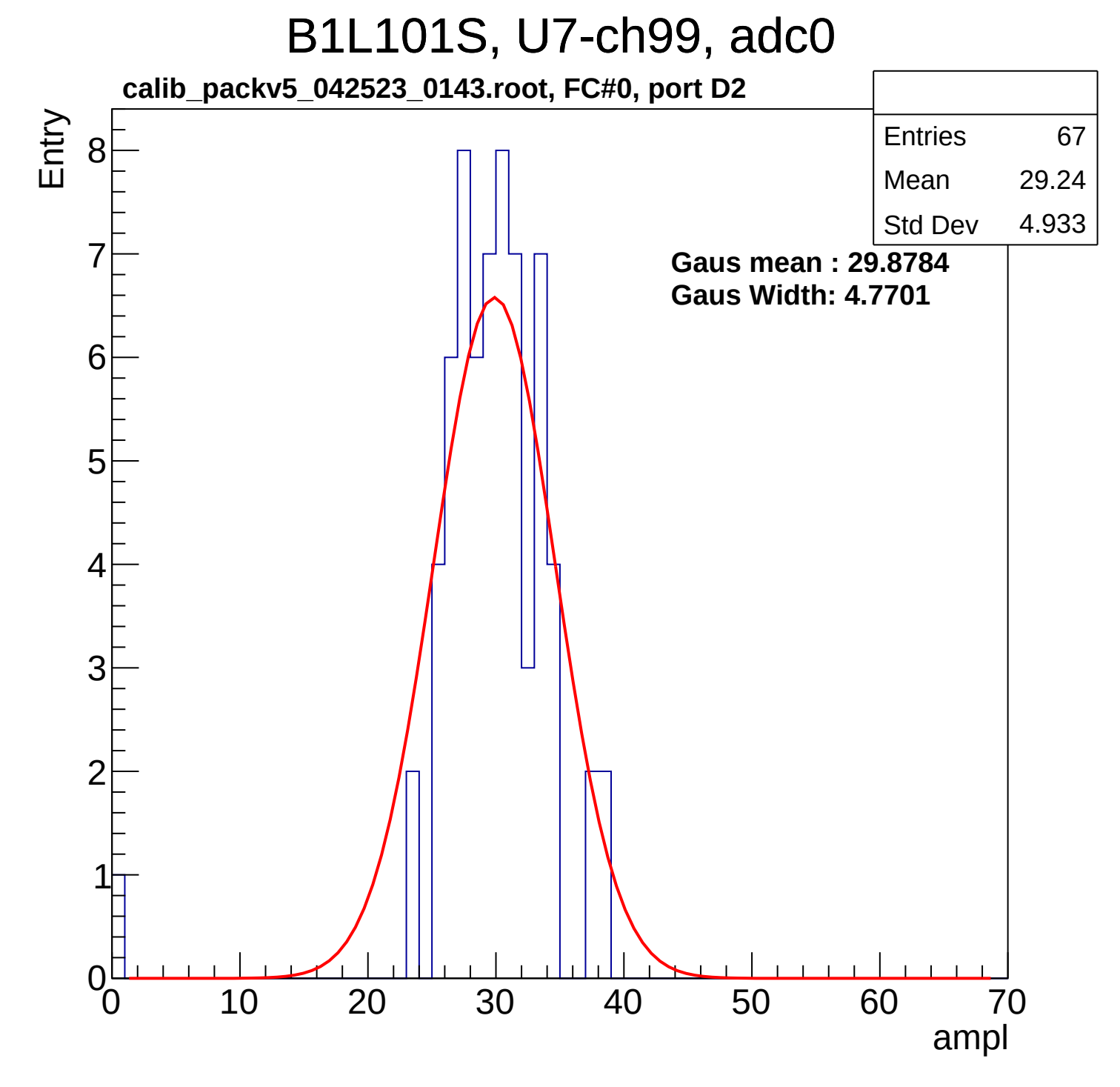
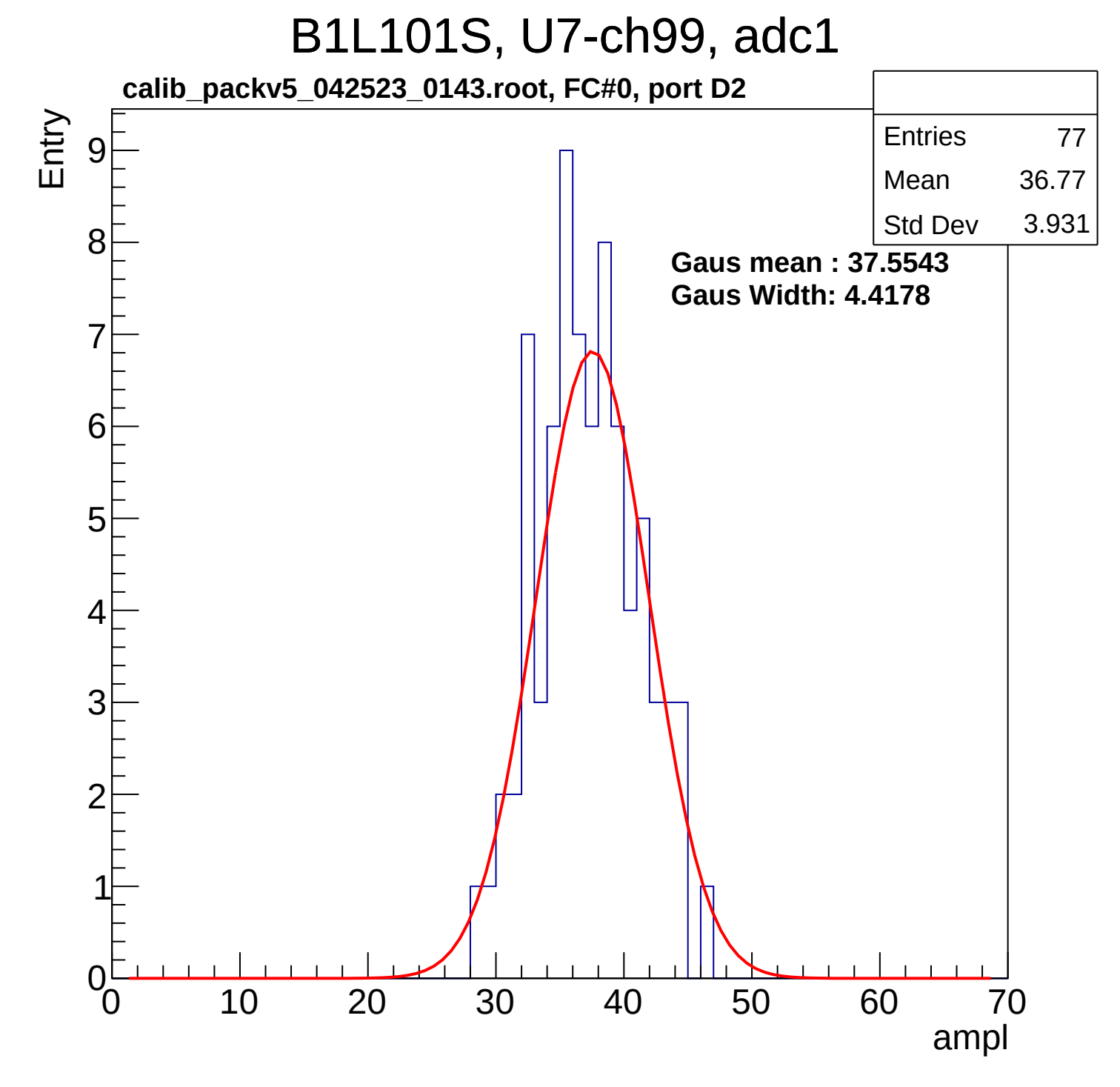
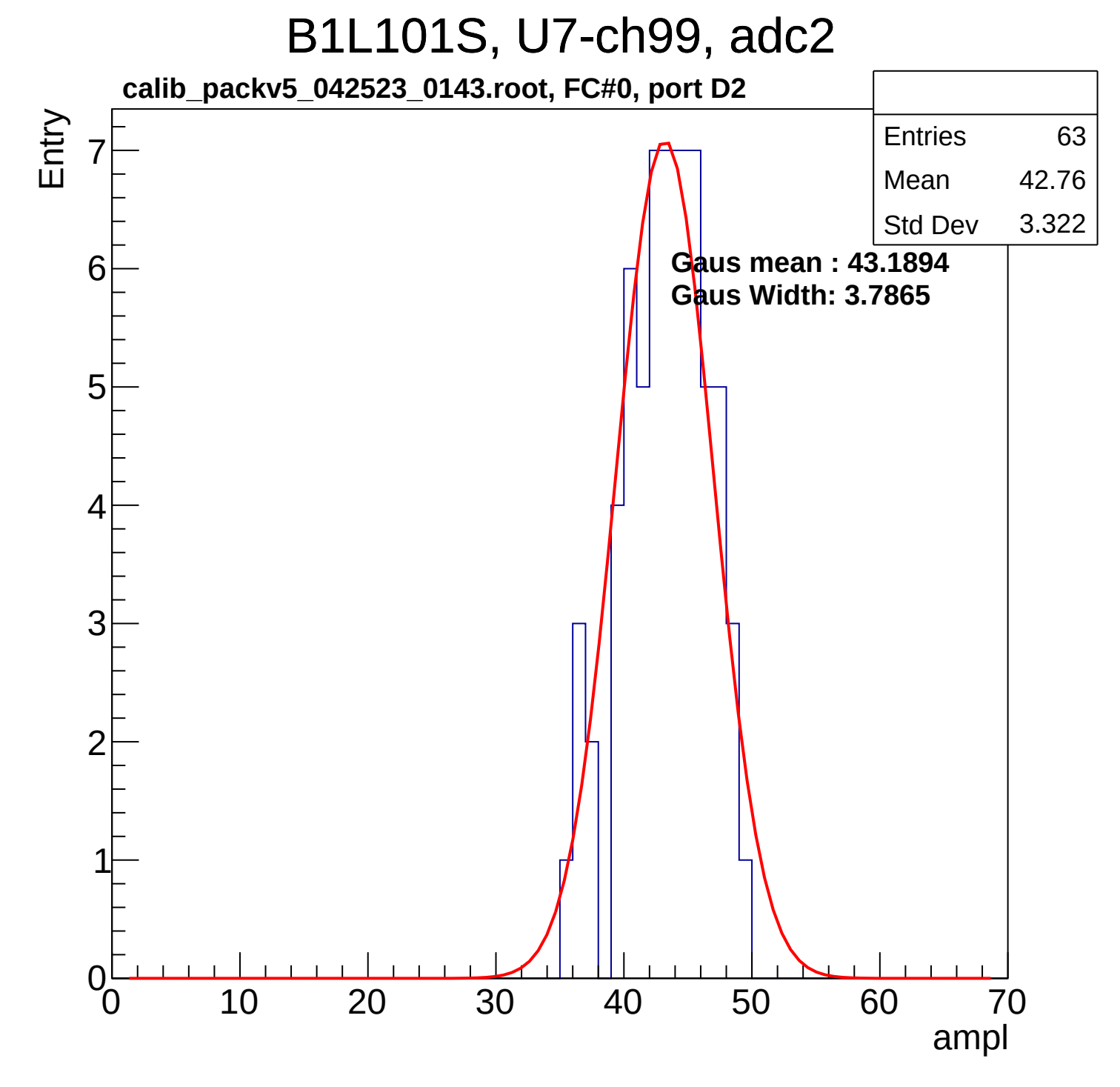
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U7-ch98, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 30.5
Std Dev 30.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch99, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 29.24
Std Dev 4.933
Gaus mean : 29.8784
Gaus Width: 4.7701
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch99, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 36.77
Std Dev 3.931
Gaus mean : 37.5543
Gaus Width: 4.4178
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch99, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 42.76
Std Dev 3.322
Gaus mean : 43.1894
Gaus Width: 3.7865
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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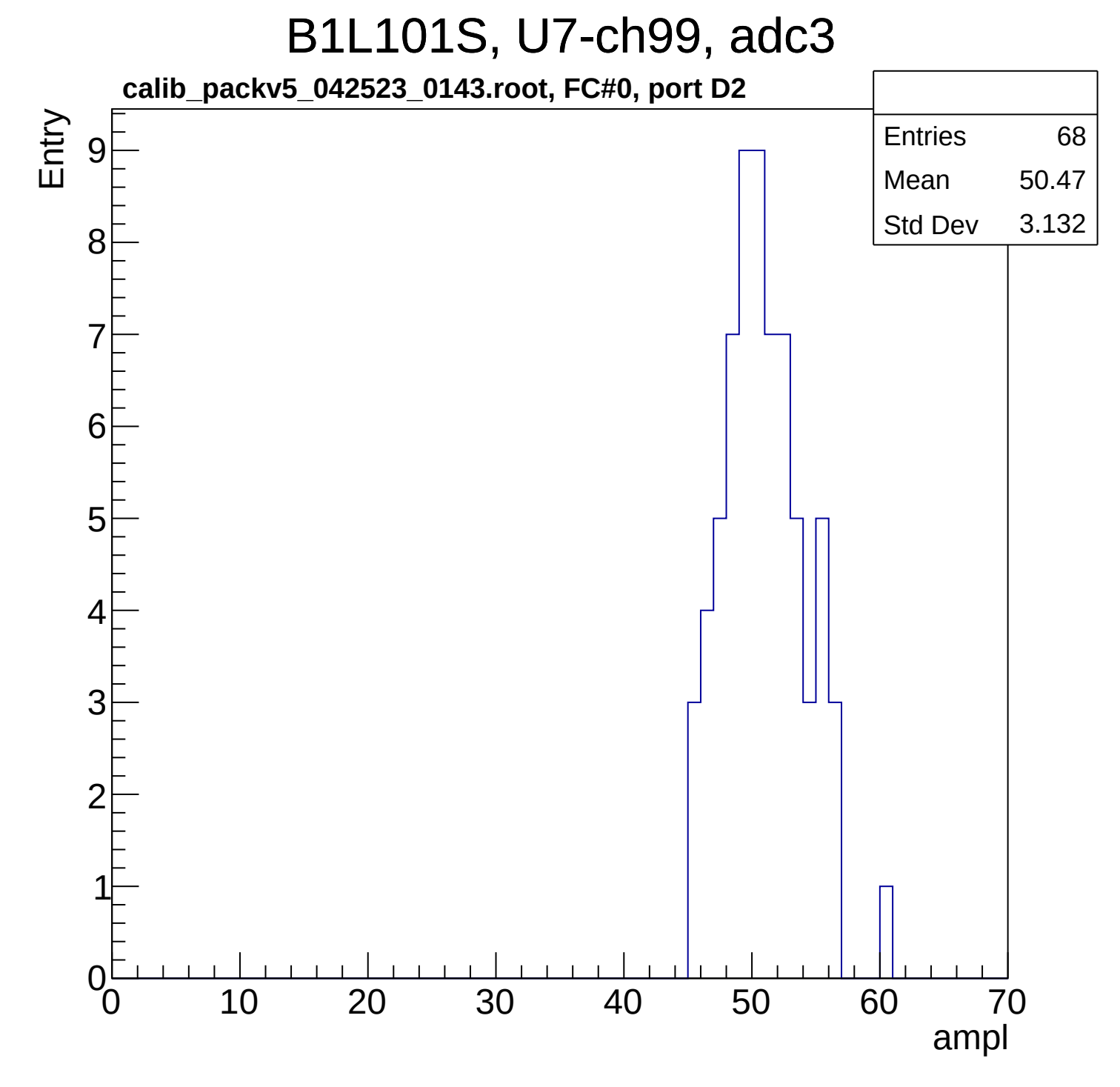
B1L101S, U7-ch99, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 50.47
Std Dev 3.132
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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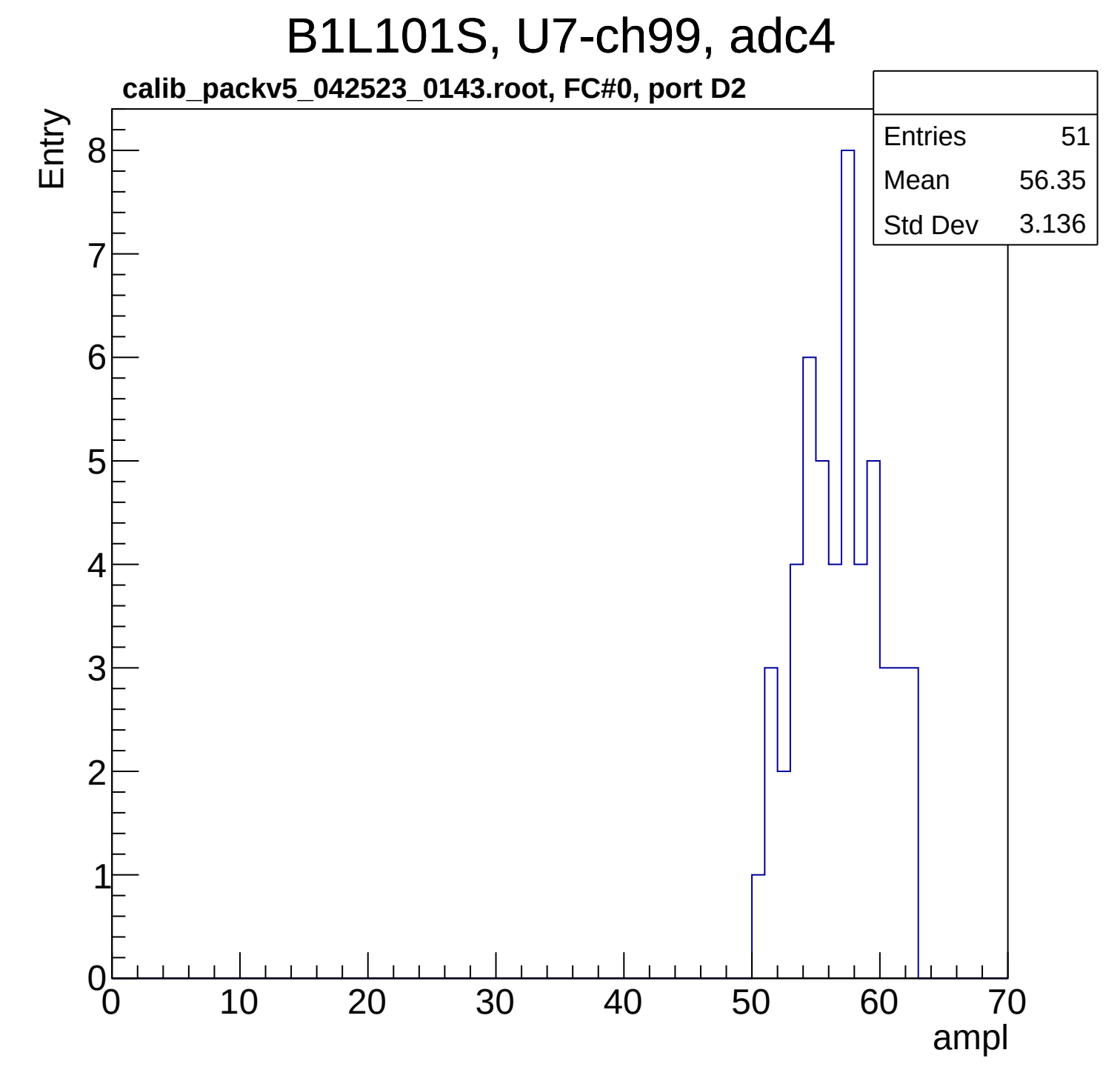
B1L101S, U7-ch99, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 56.35
Std Dev 3.136
Entry
ampl
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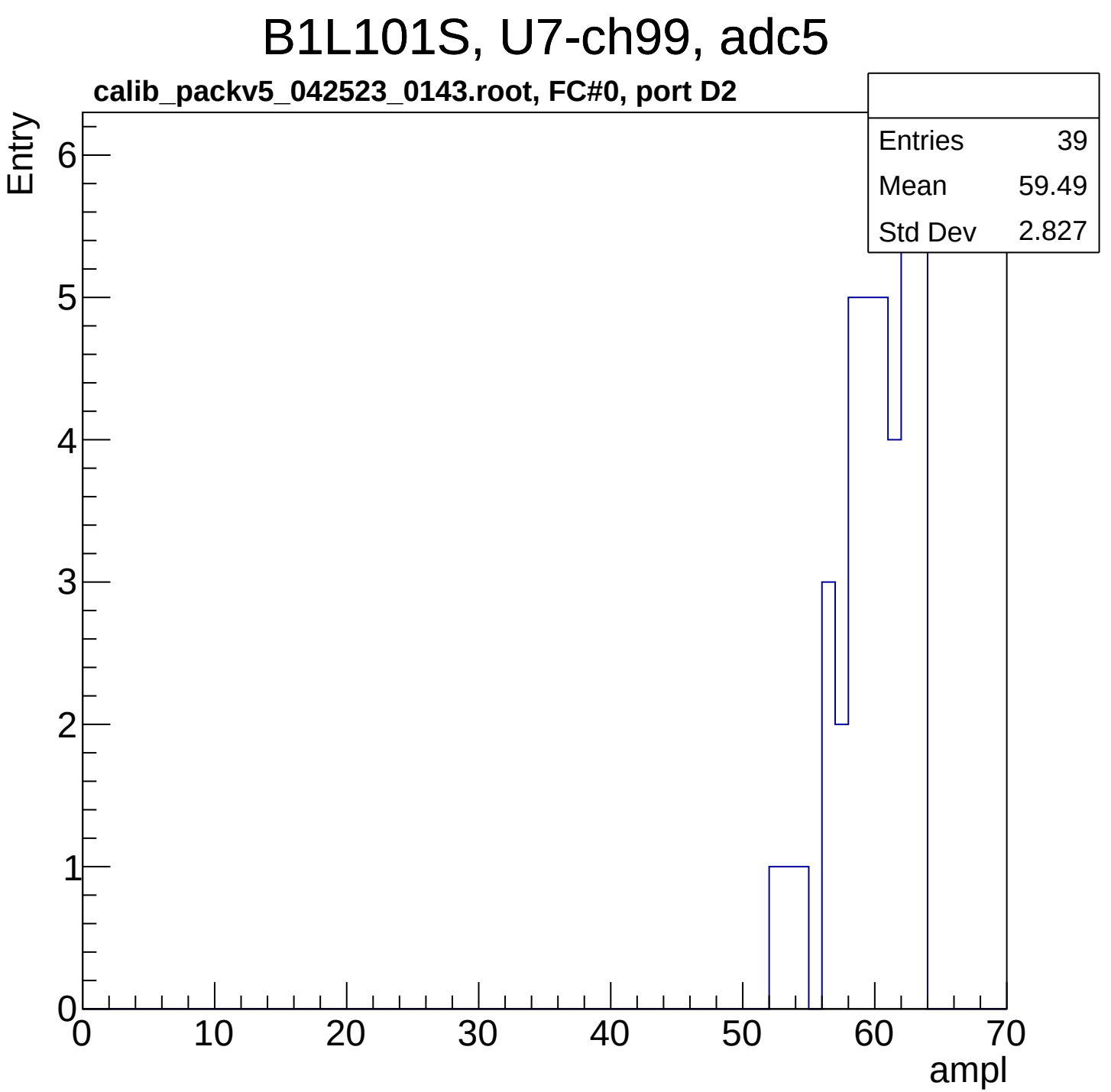
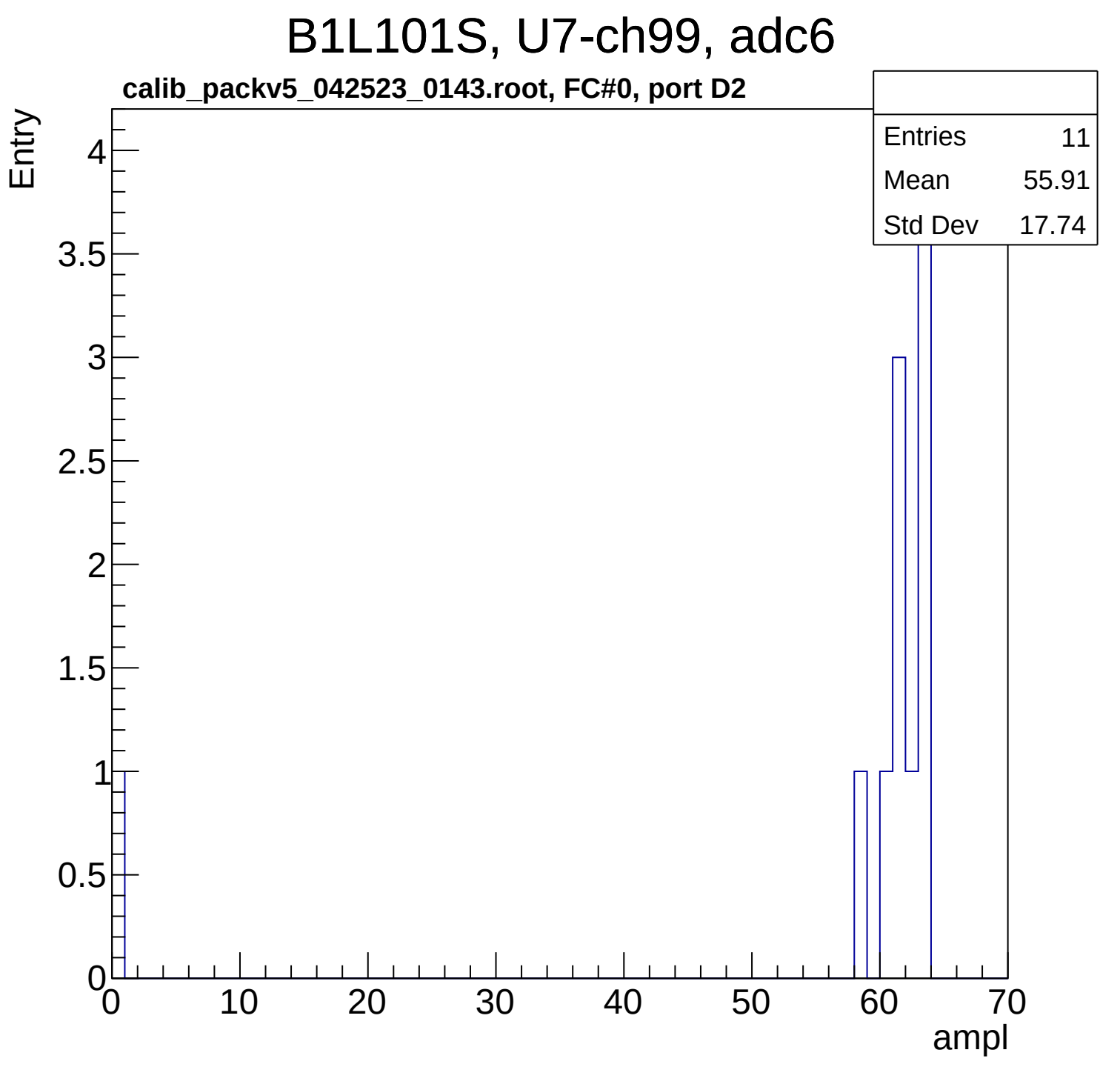
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch99, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 39
Mean 59.49
Std Dev 2.827
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch99, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 11
Mean 55.91
Std Dev 17.74
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
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60
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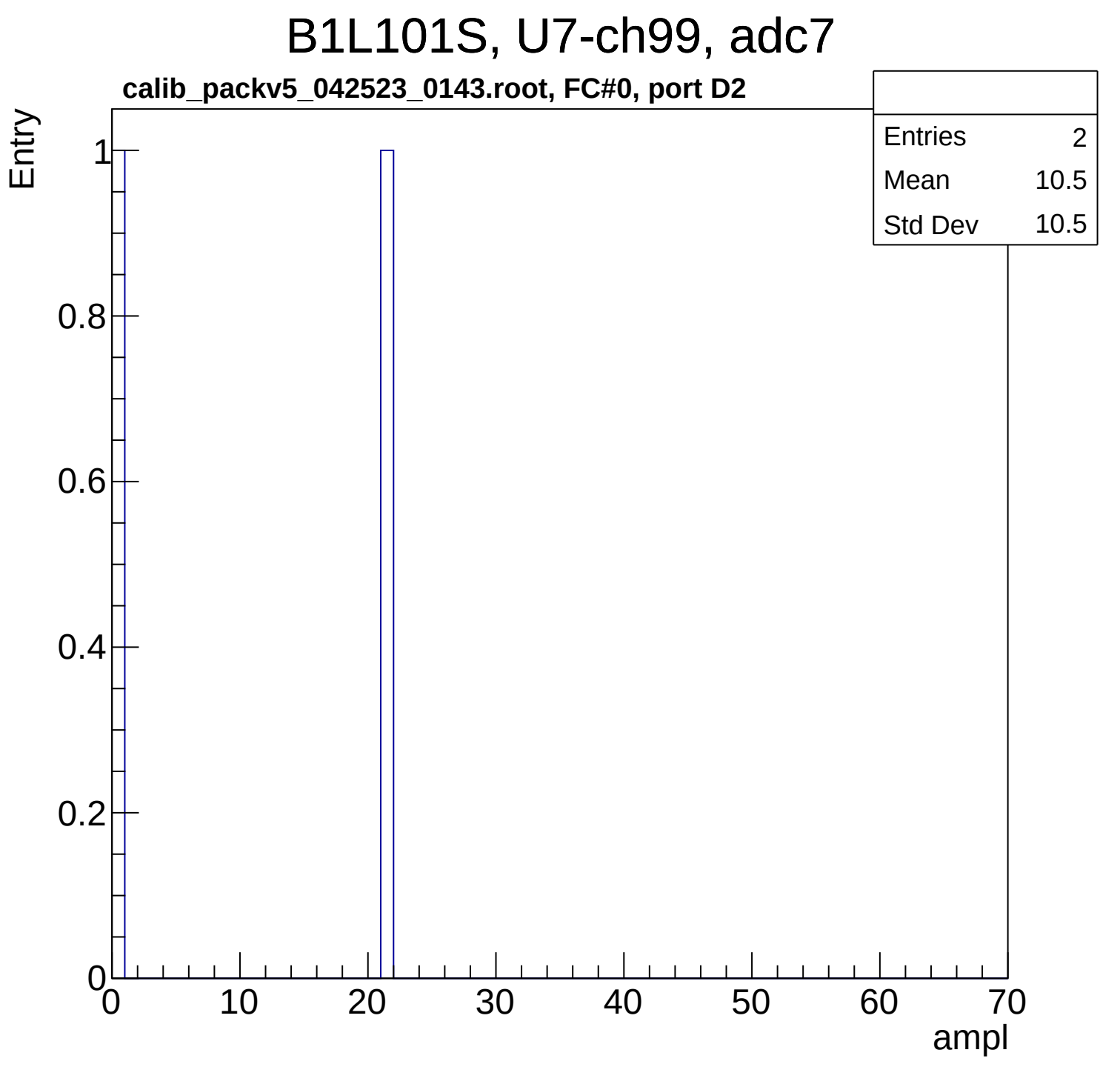
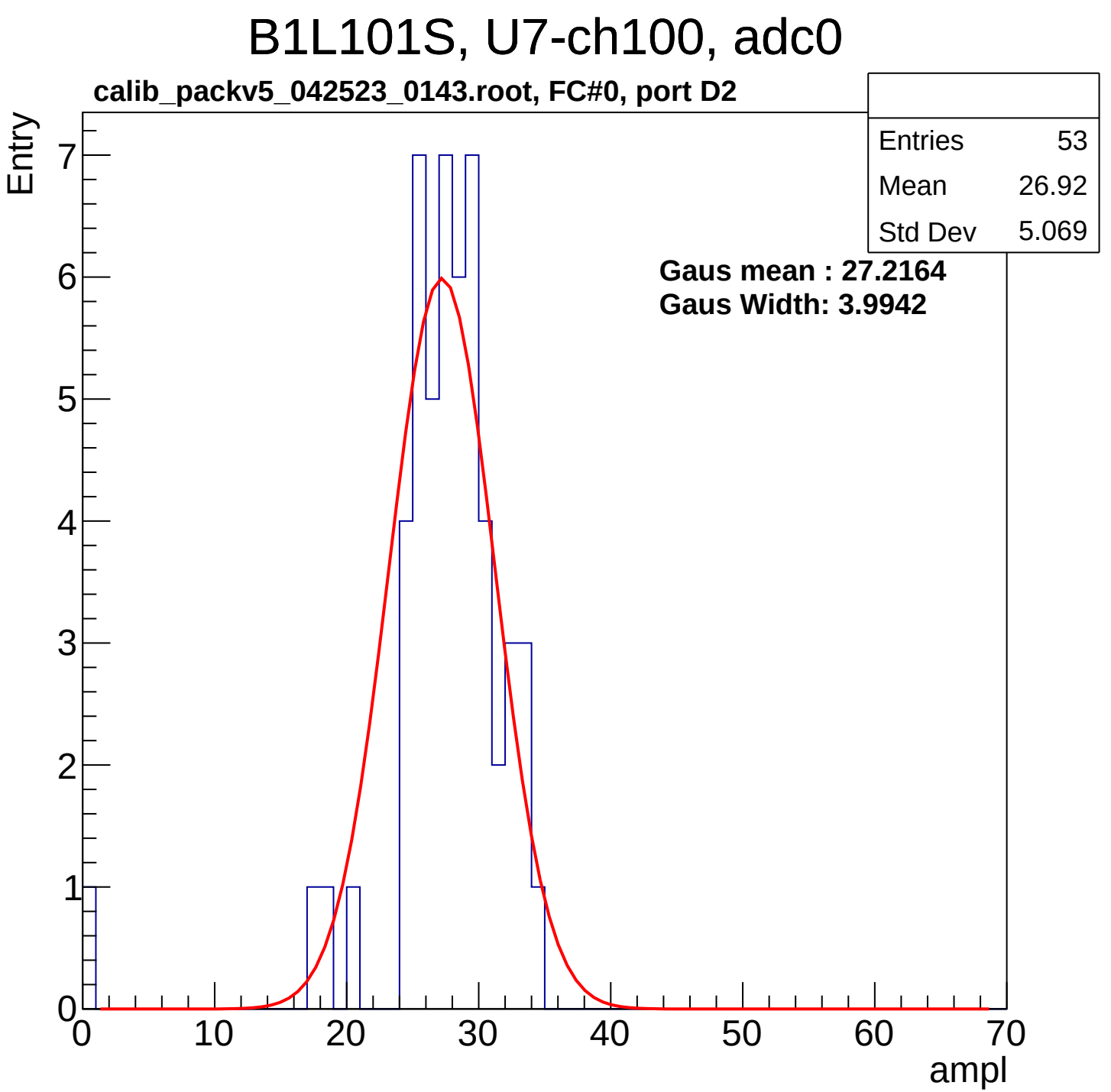
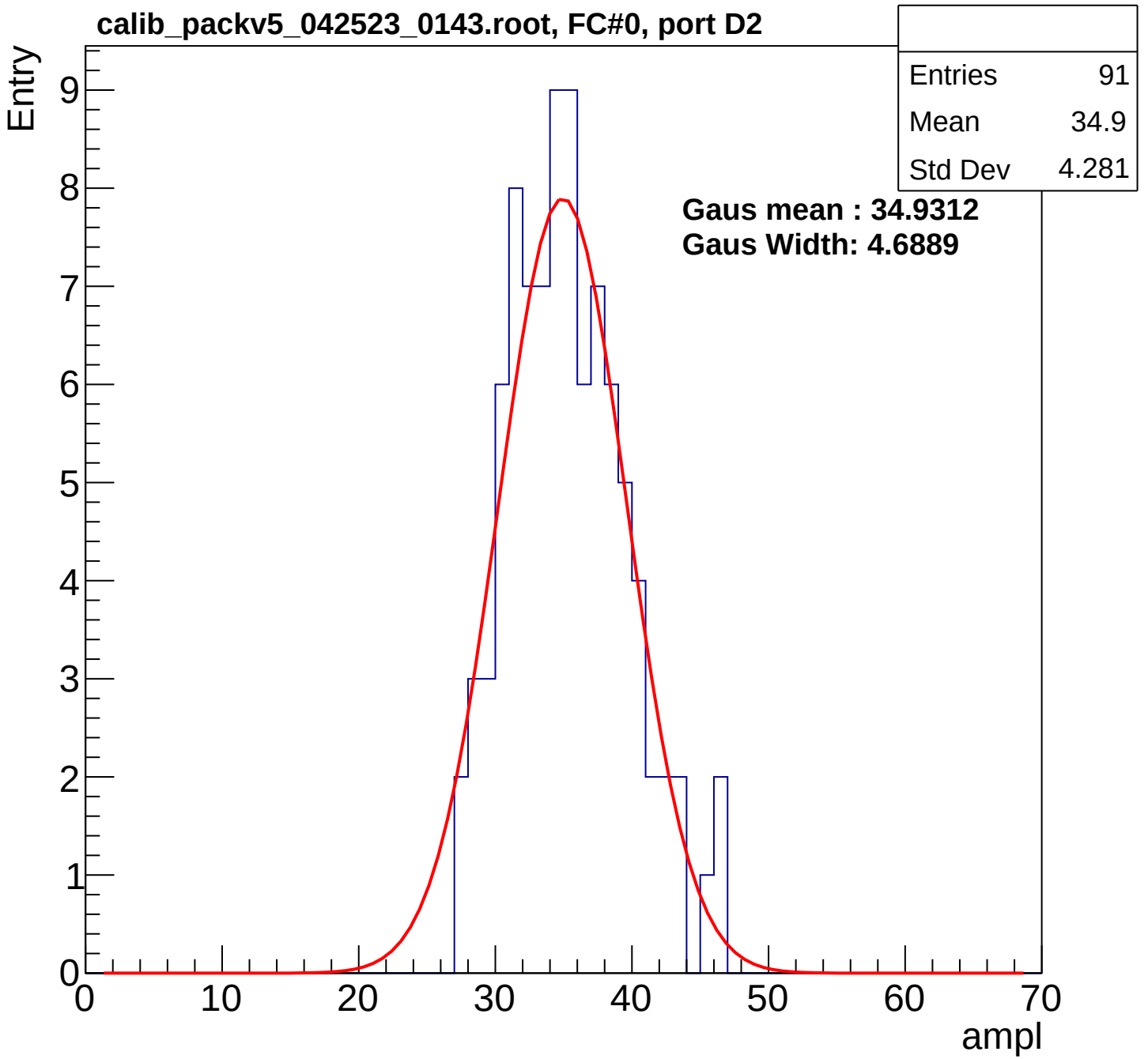

B1L101S, U7-ch99, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 10.5
Std Dev 10.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch100, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 26.92
Std Dev 5.069
Gaus mean : 27.2164
Gaus Width: 3.9942
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U7-ch100, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 91
Mean 34.9
Std Dev 4.281
Gaus mean : 34.9312
Gaus Width: 4.6889
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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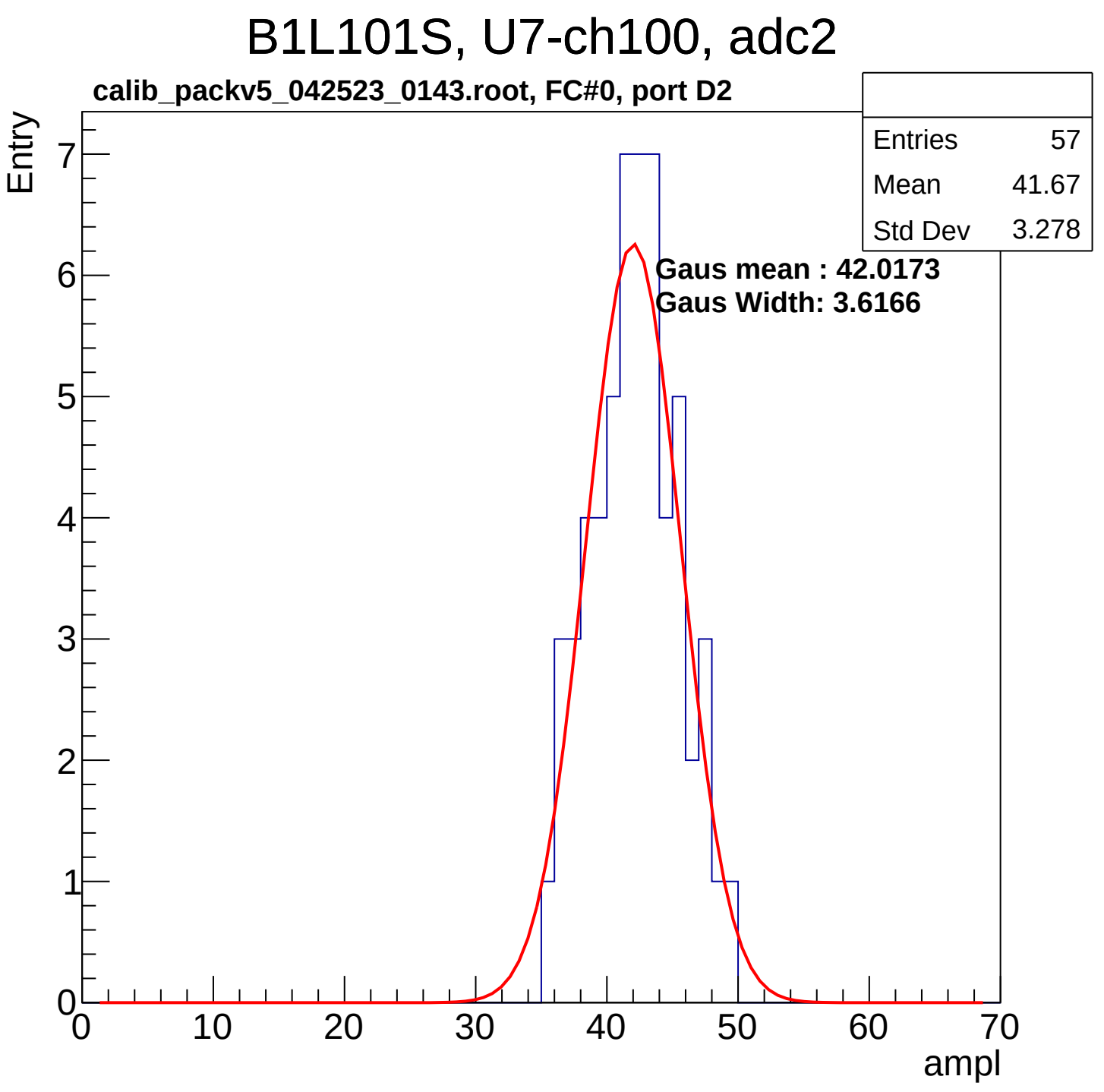
B1L101S, U7-ch100, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 41.67
Std Dev 3.278
Gaus mean : 42.0173
Gaus Width: 3.6166
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
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60
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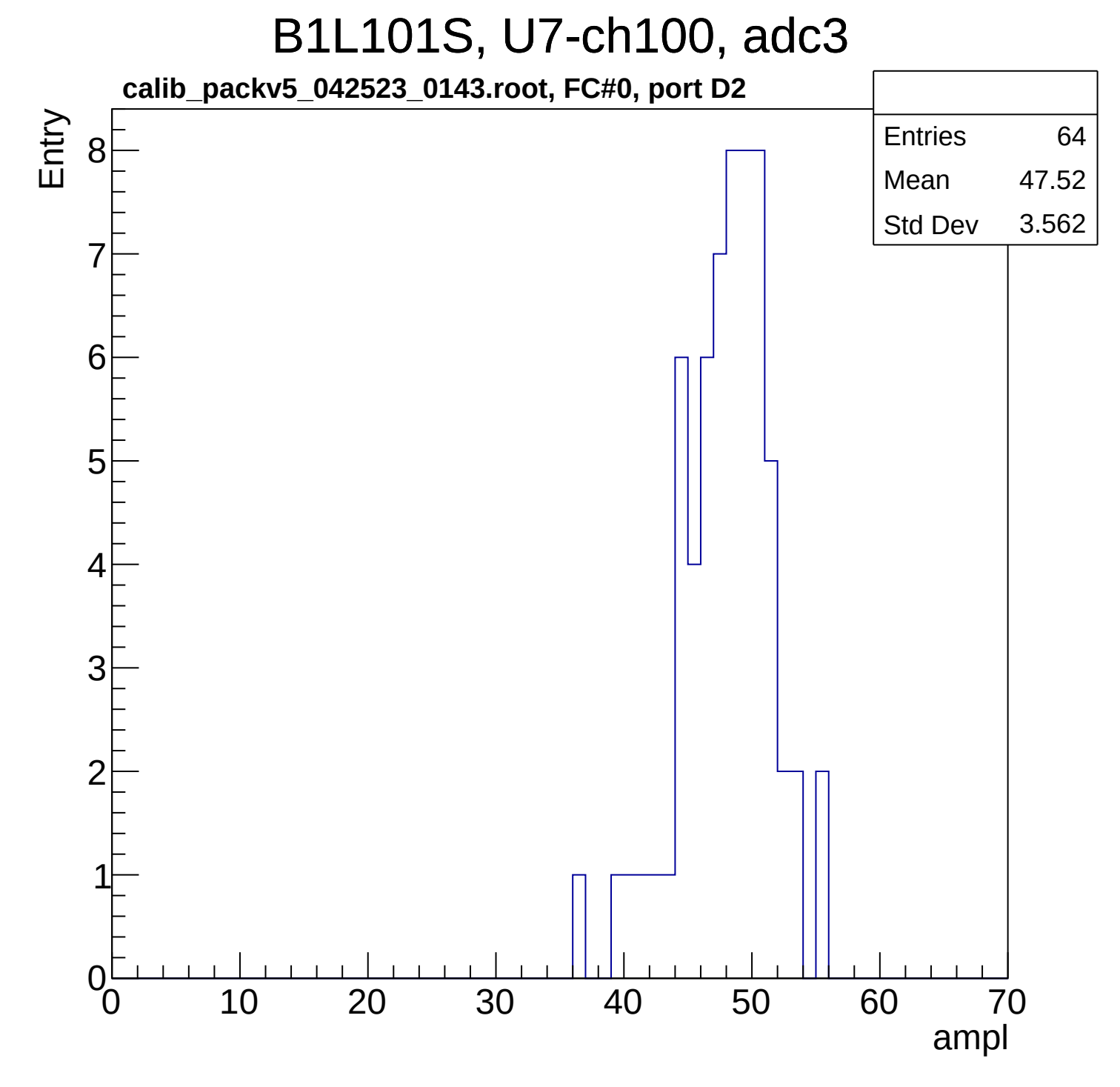
B1L101S, U7-ch100, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 47.52
Std Dev 3.562
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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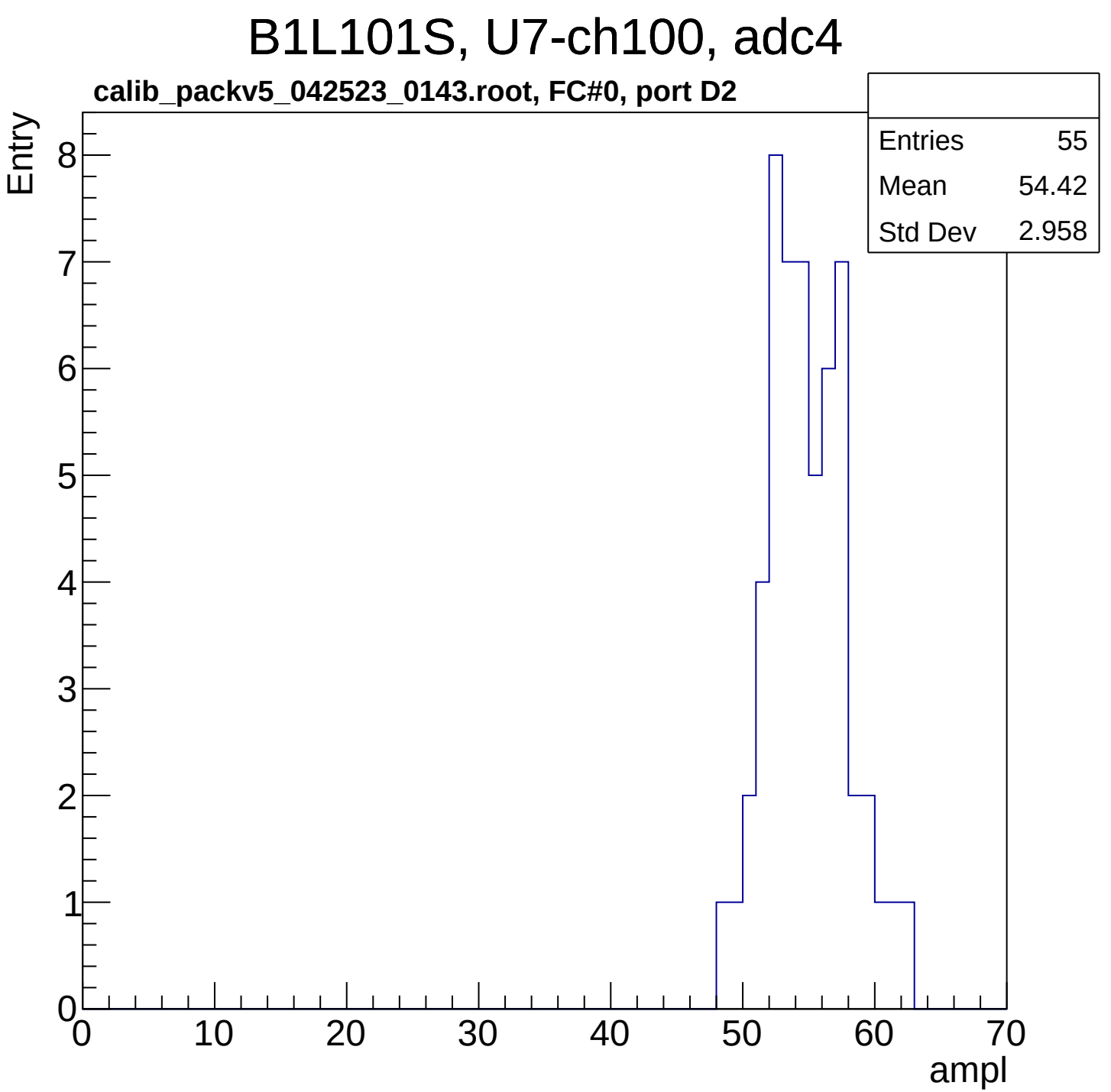
B1L101S, U7-ch100, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 54.42
Std Dev 2.958
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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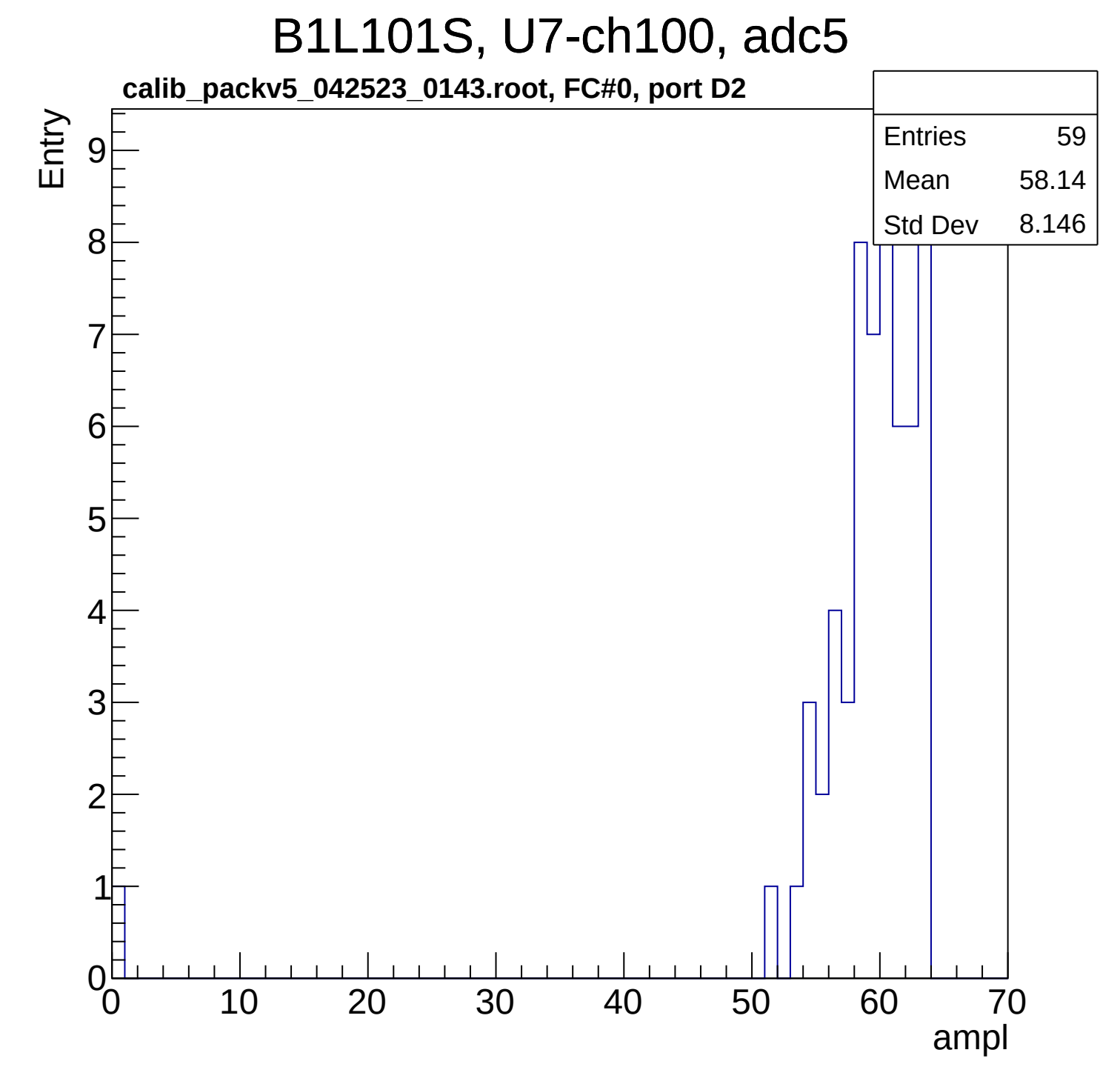
B1L101S, U7-ch100, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 58.14
Std Dev 8.146
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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60
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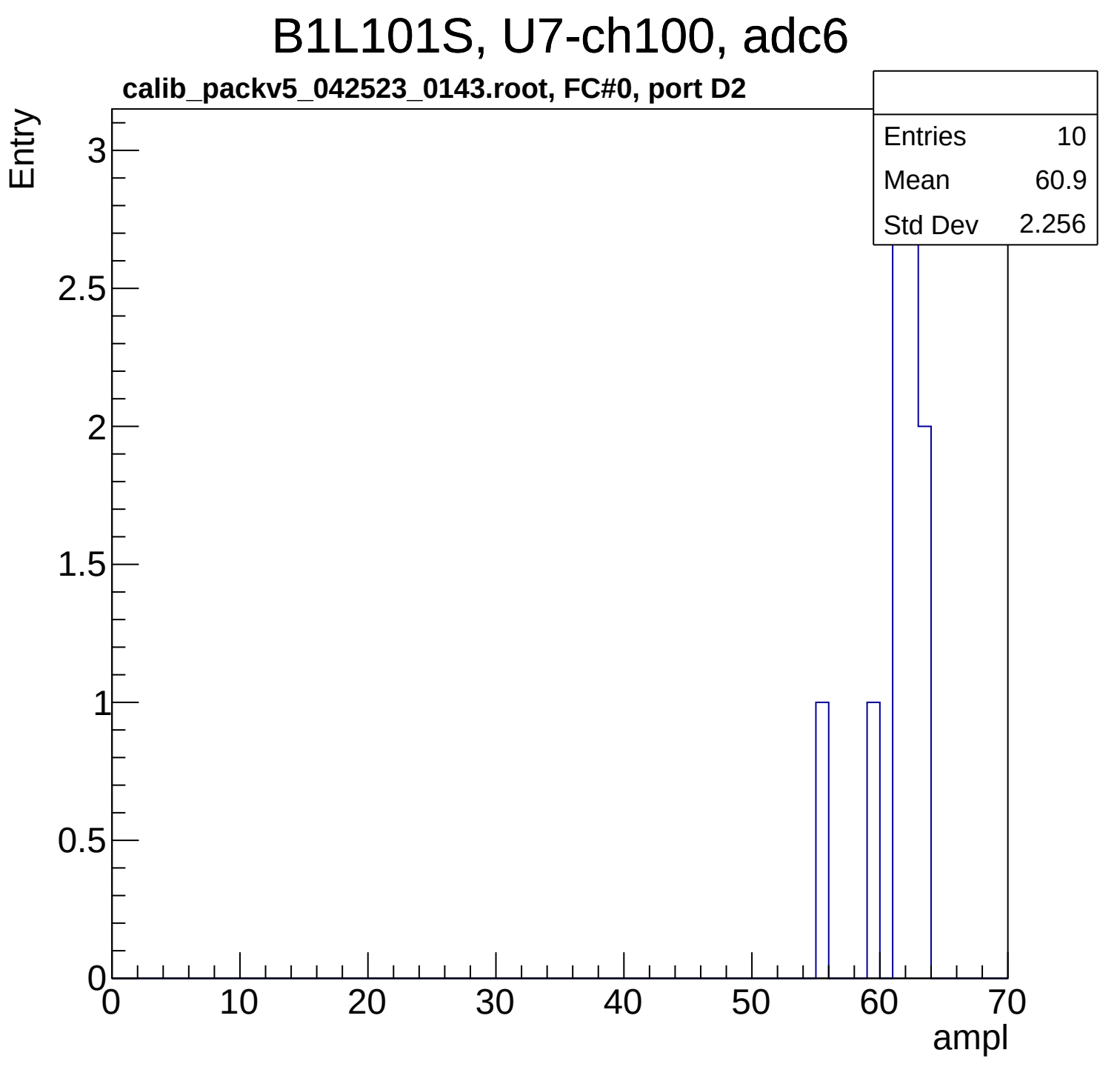
B1L101S, U7-ch100, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 60.9
Std Dev 2.256
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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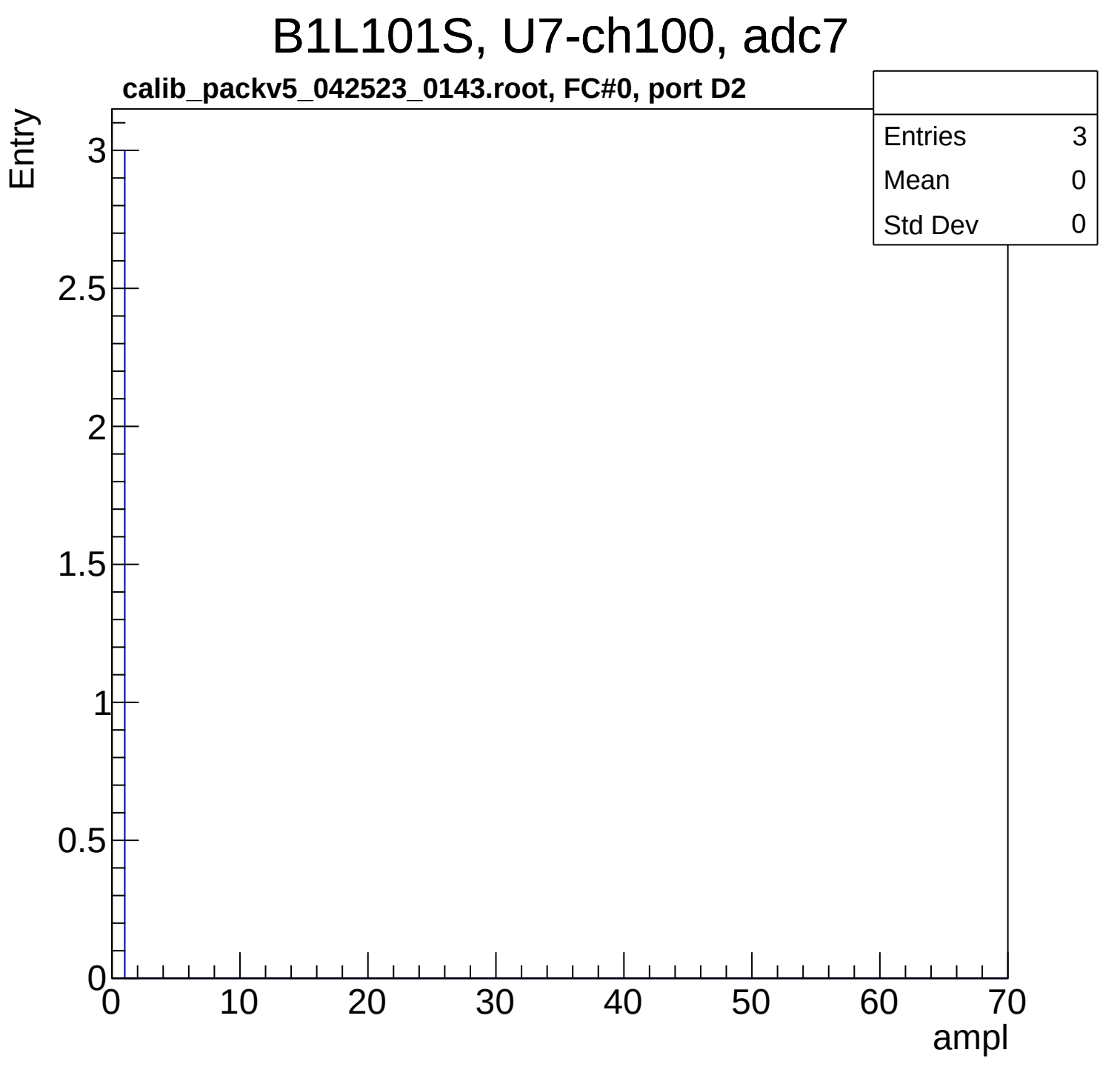
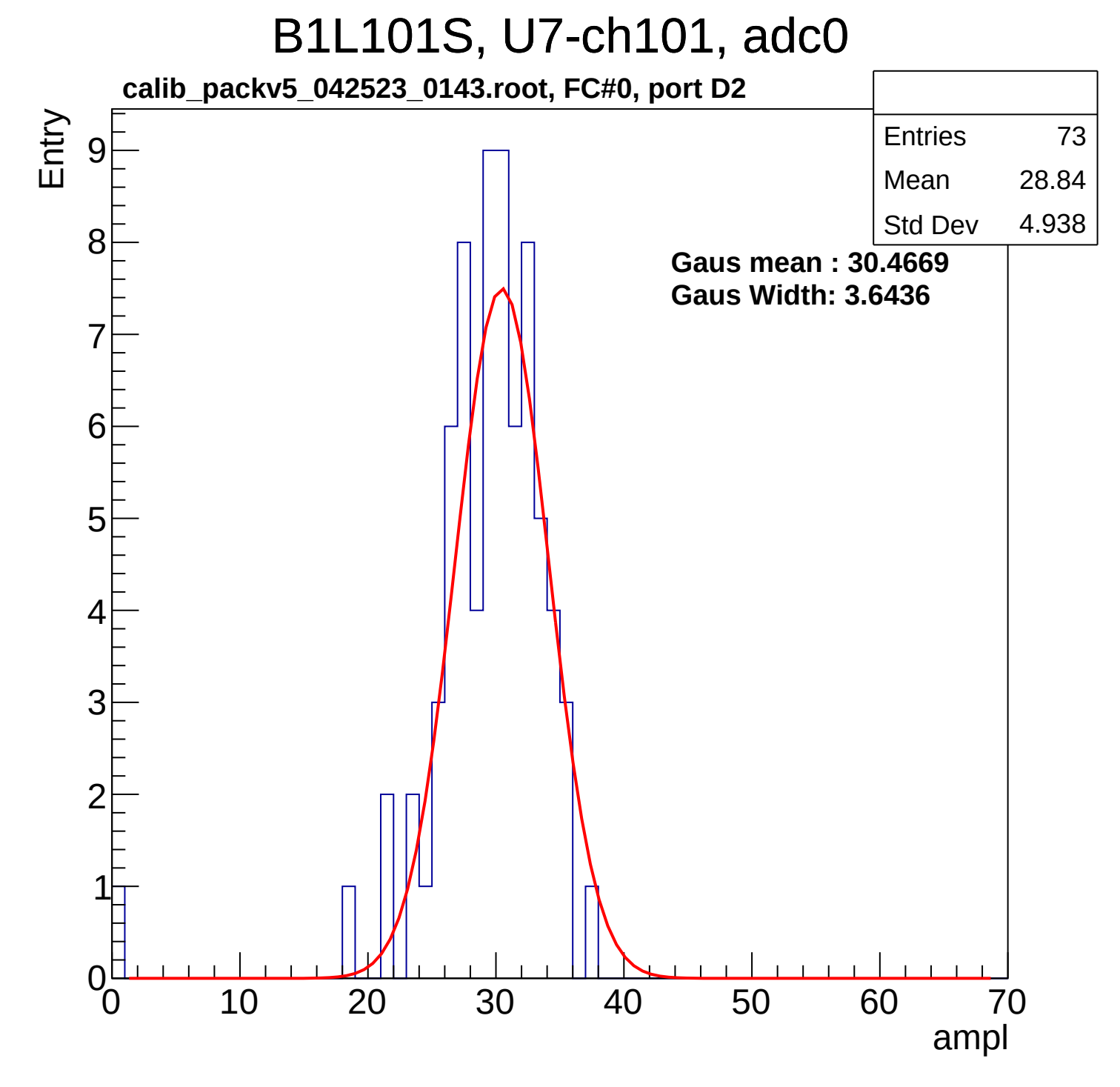

B1L101S, U7-ch100, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 0
Std Dev 0
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch101, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 28.84
Std Dev 4.938
Gaus mean : 30.4669
Gaus Width: 3.6436
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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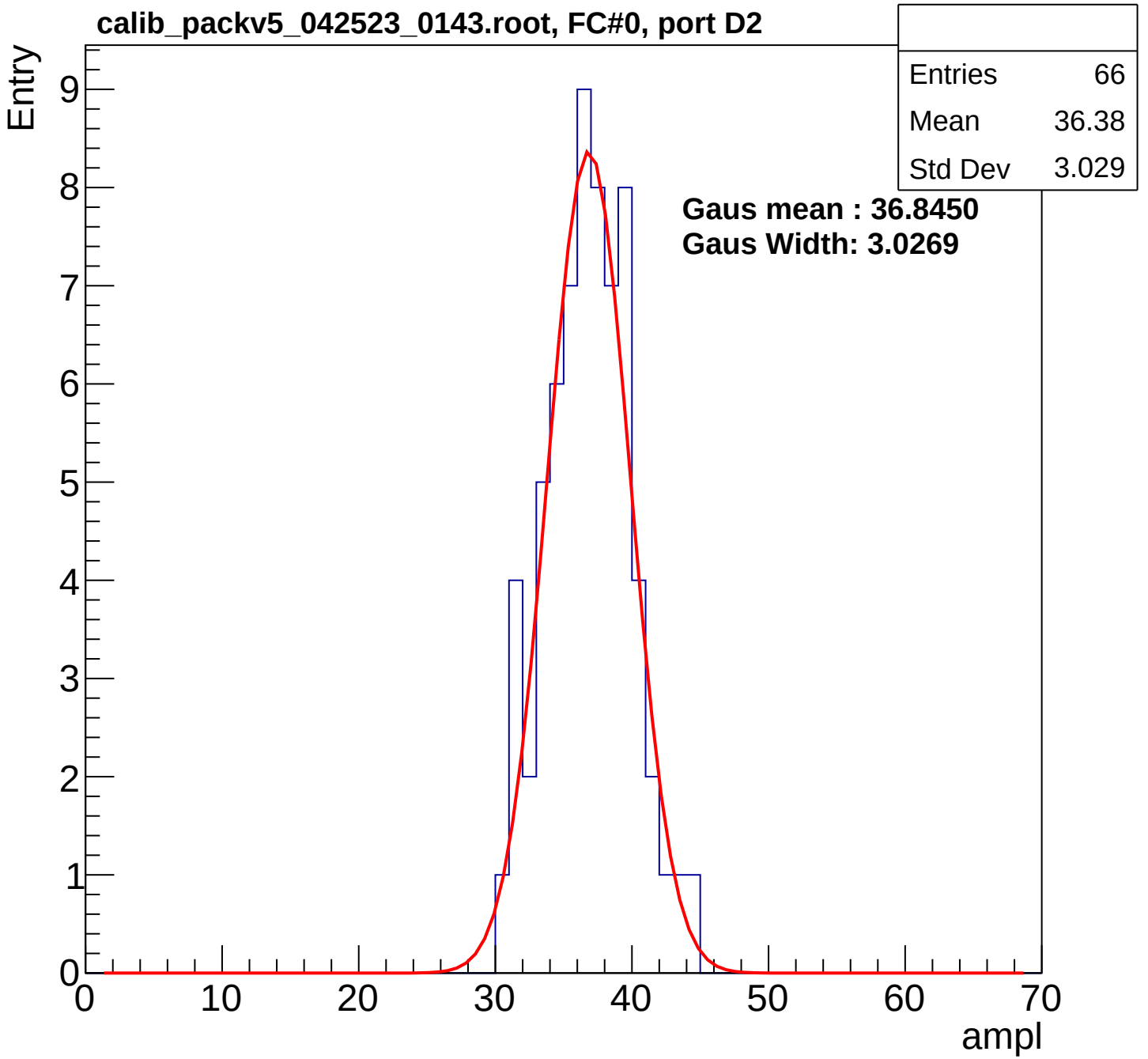
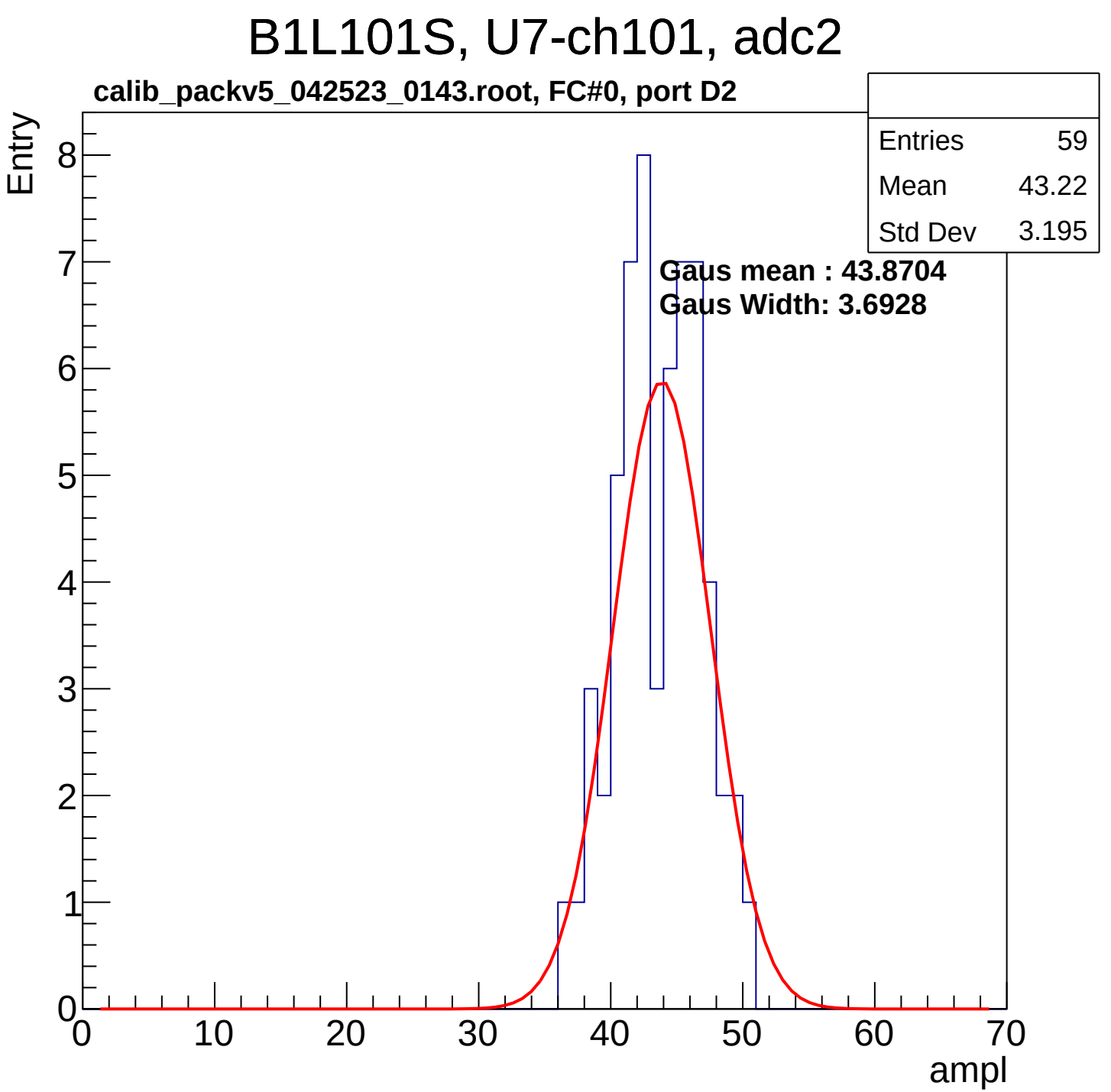

B1L101S, U7-ch101, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 36.38
Std Dev 3.029
Gaus mean : 36.8450
Gaus Width: 3.0269
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch101, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 43.22
Std Dev 3.195
Gaus mean : 43.8704
Gaus Width: 3.6928
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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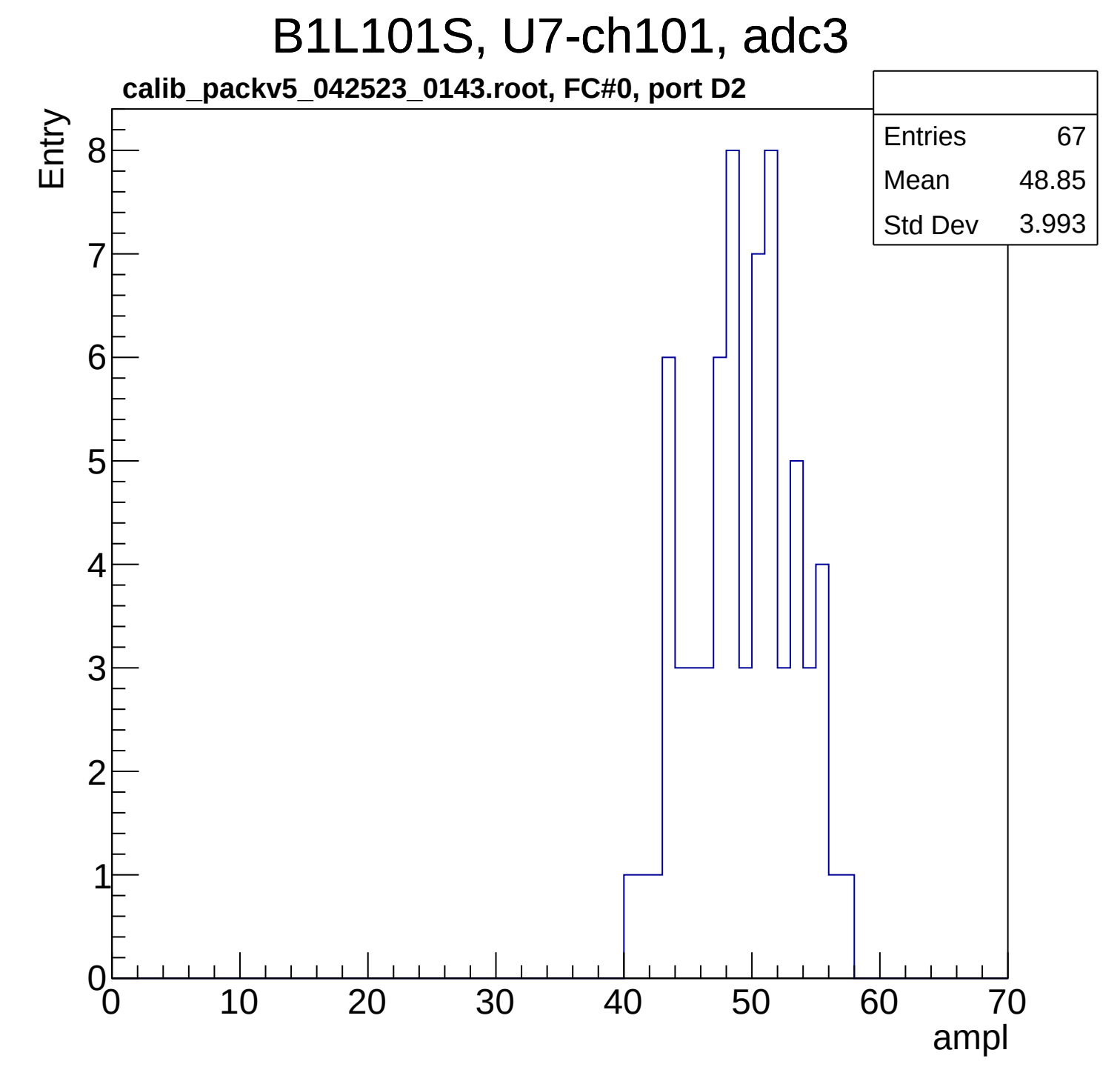
B1L101S, U7-ch101, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 48.85
Std Dev 3.993
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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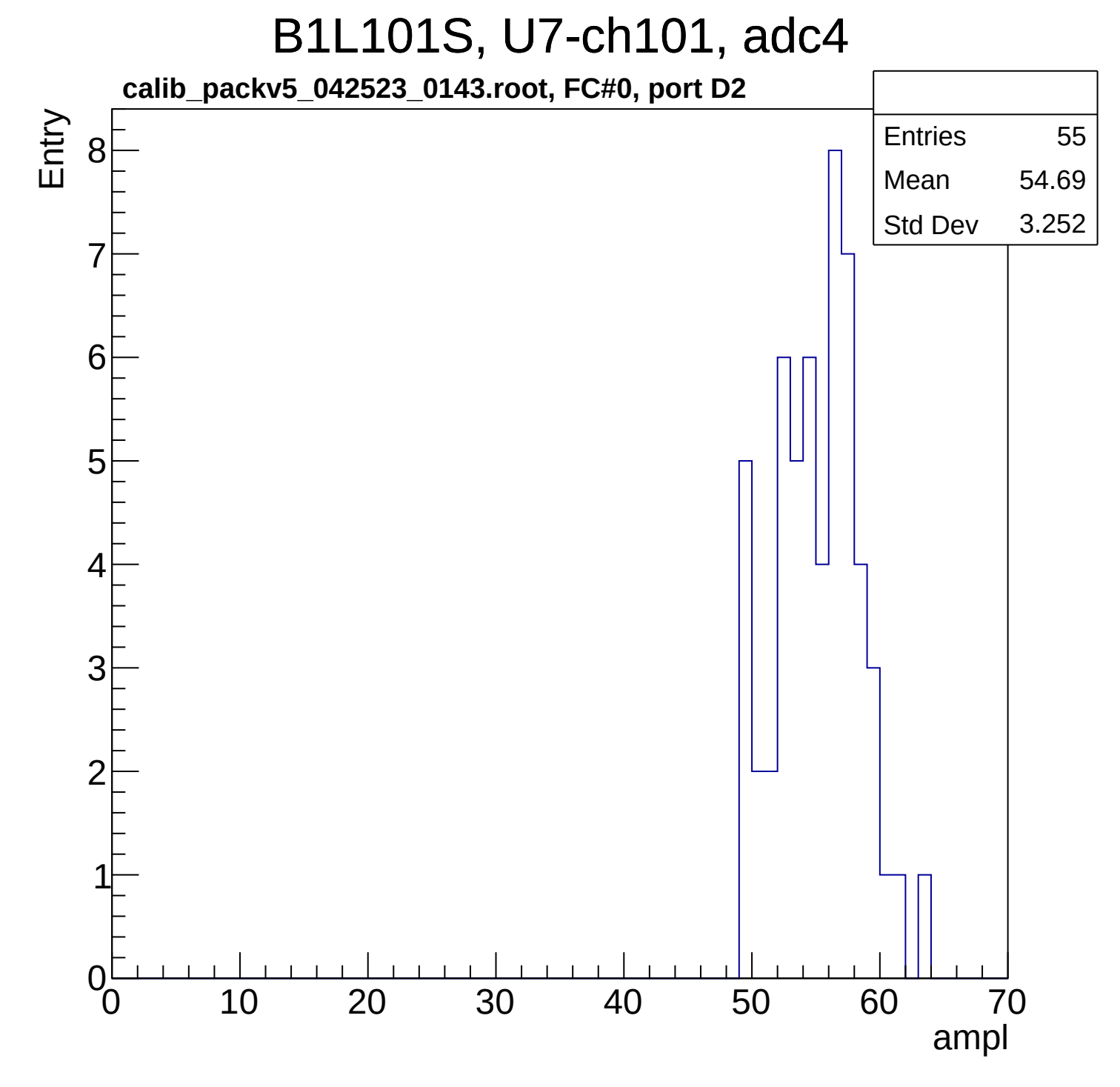
B1L101S, U7-ch101, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 54.69
Std Dev 3.252
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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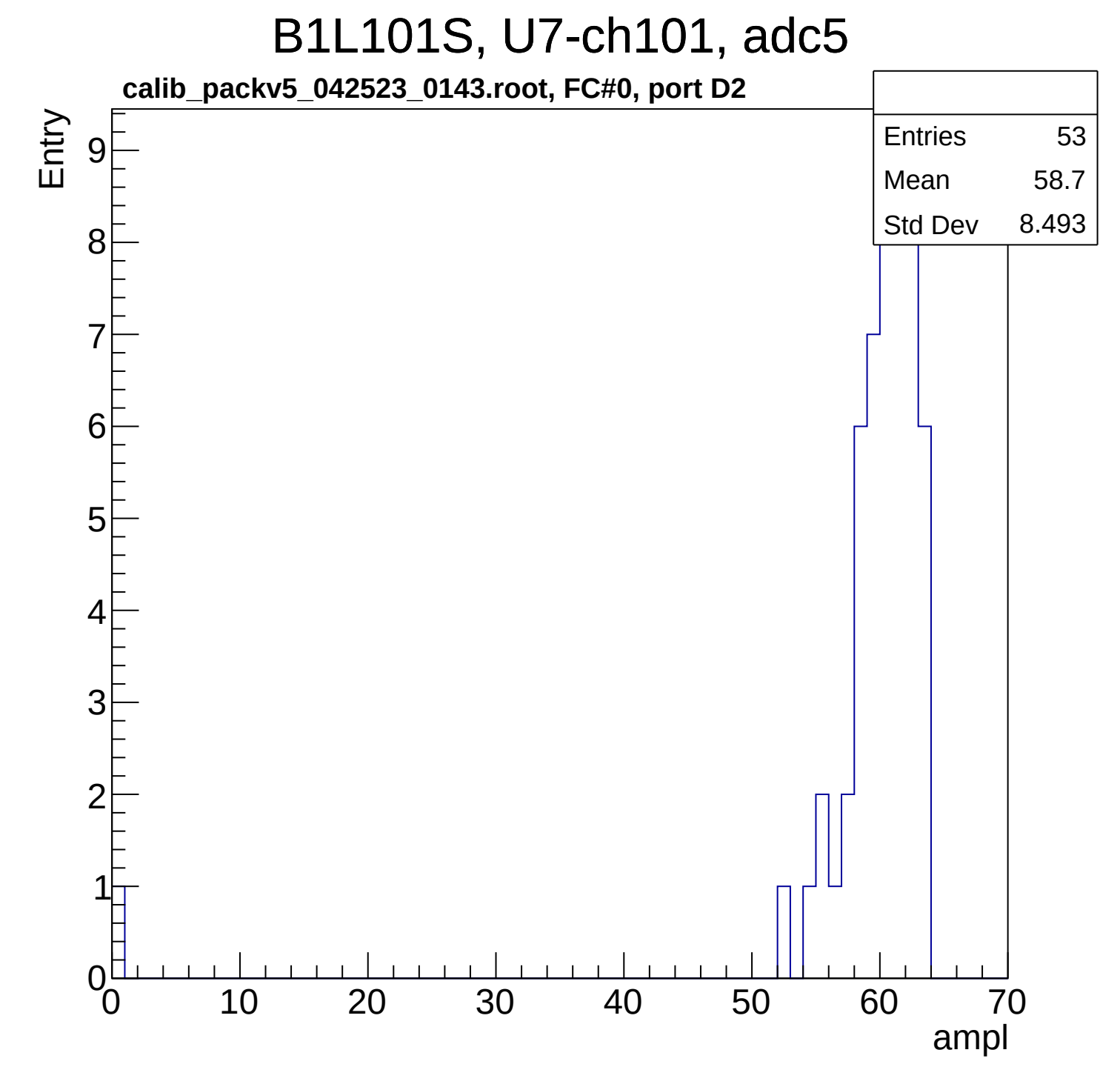
B1L101S, U7-ch101, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 58.7
Std Dev 8.493
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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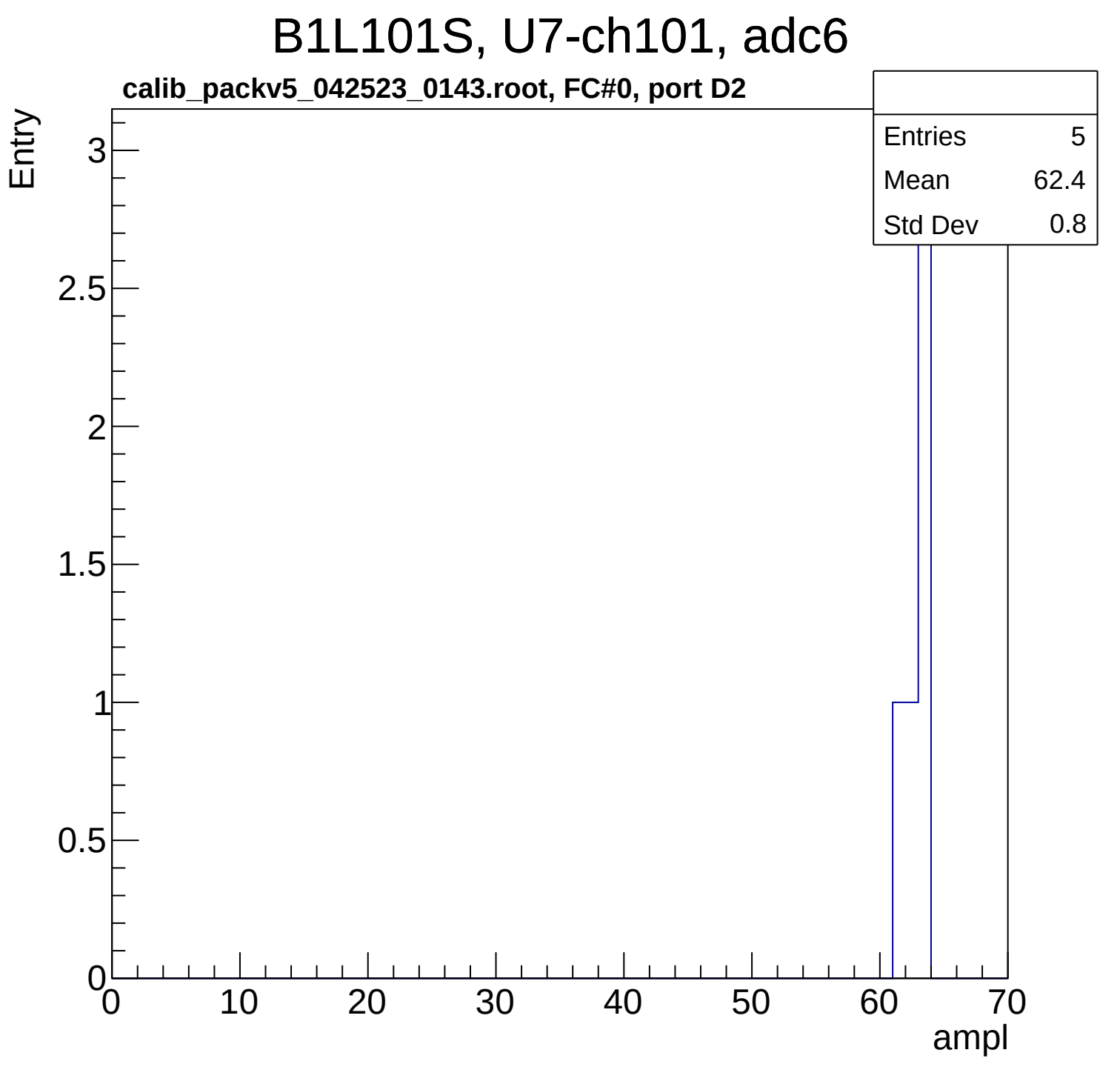
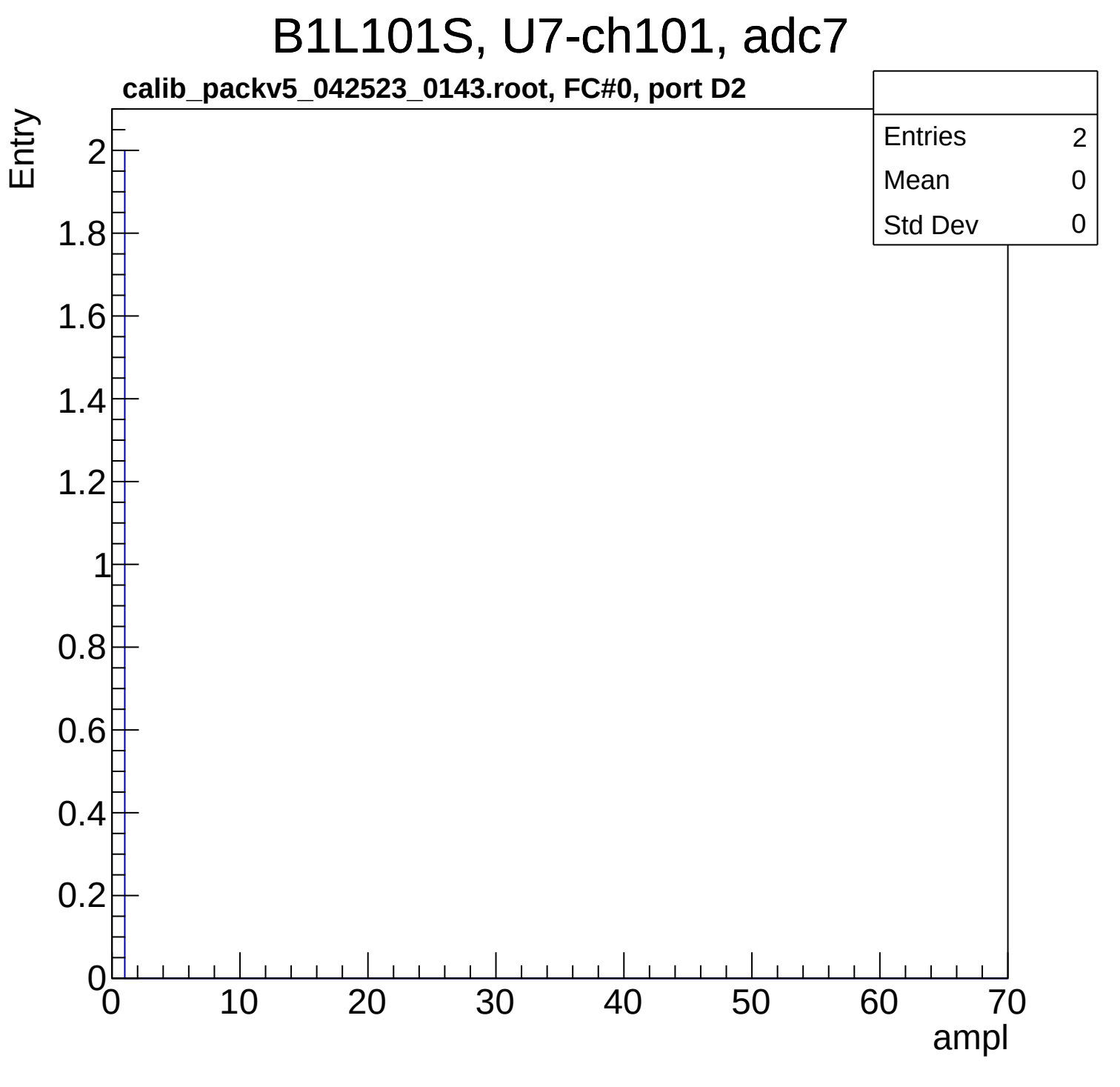

B1L101S, U7-ch101, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 62.4
Std Dev 0.8
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U7-ch101, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
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0.8
0.6
0.4
0.2
0
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10
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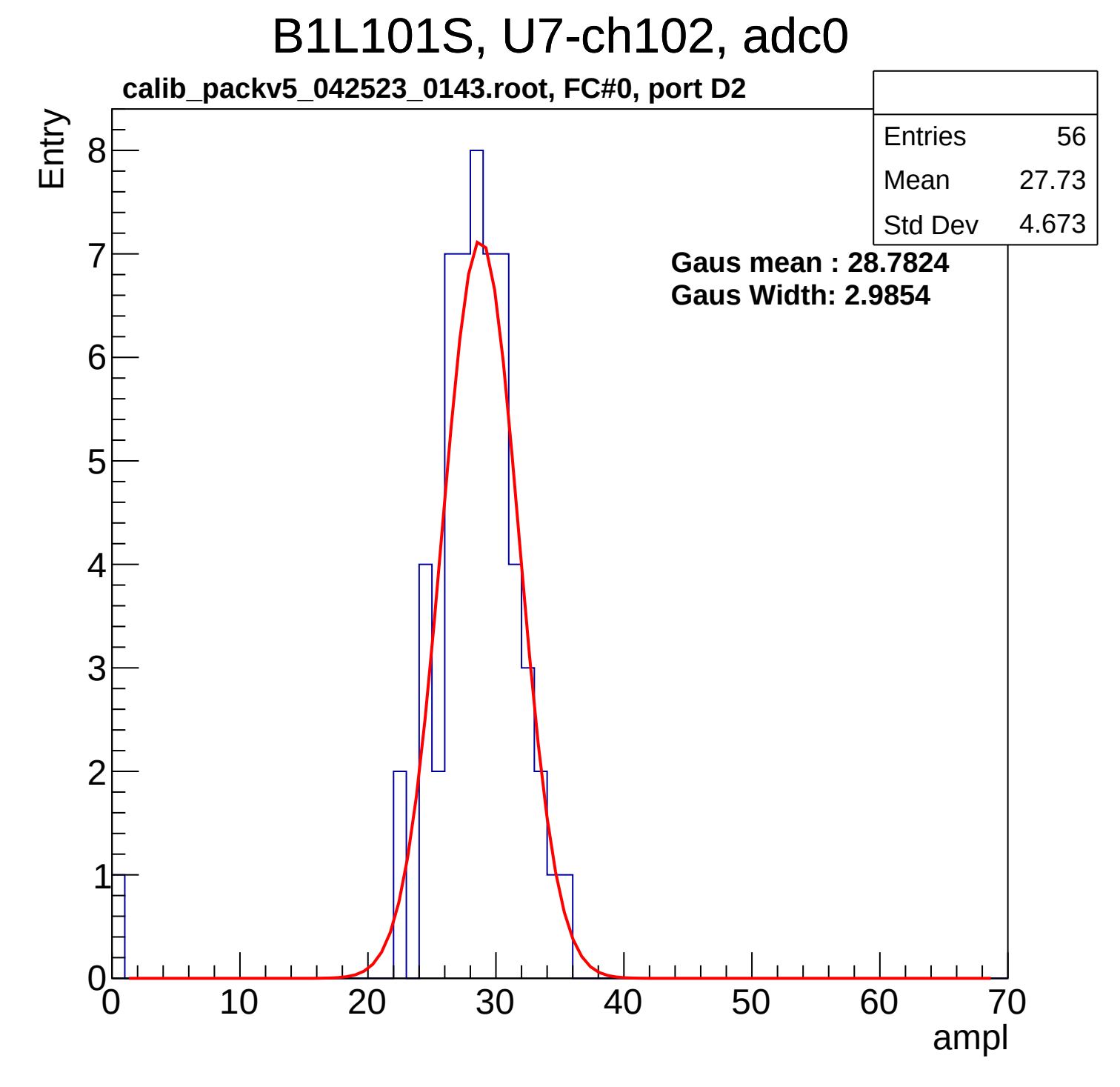
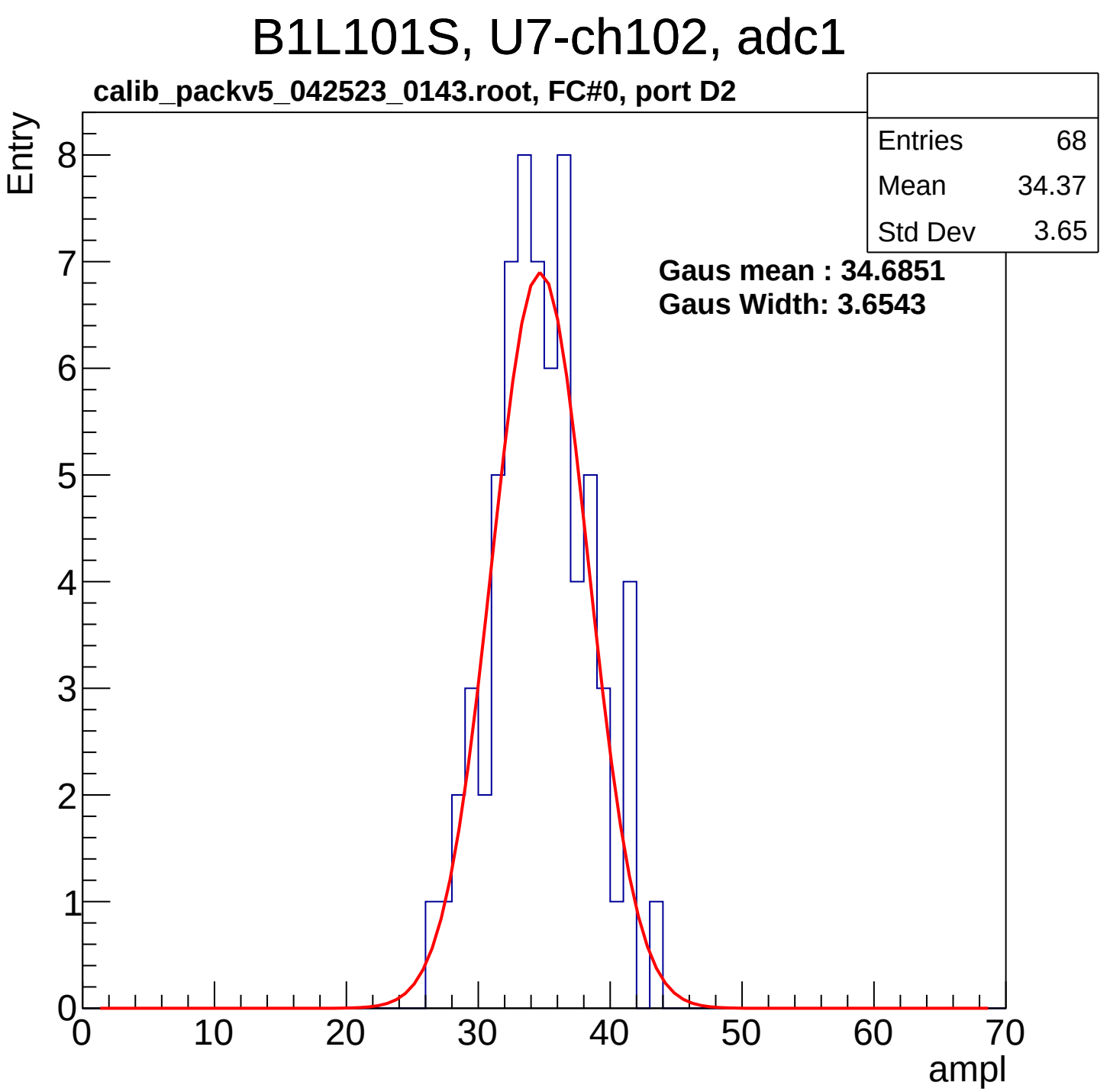
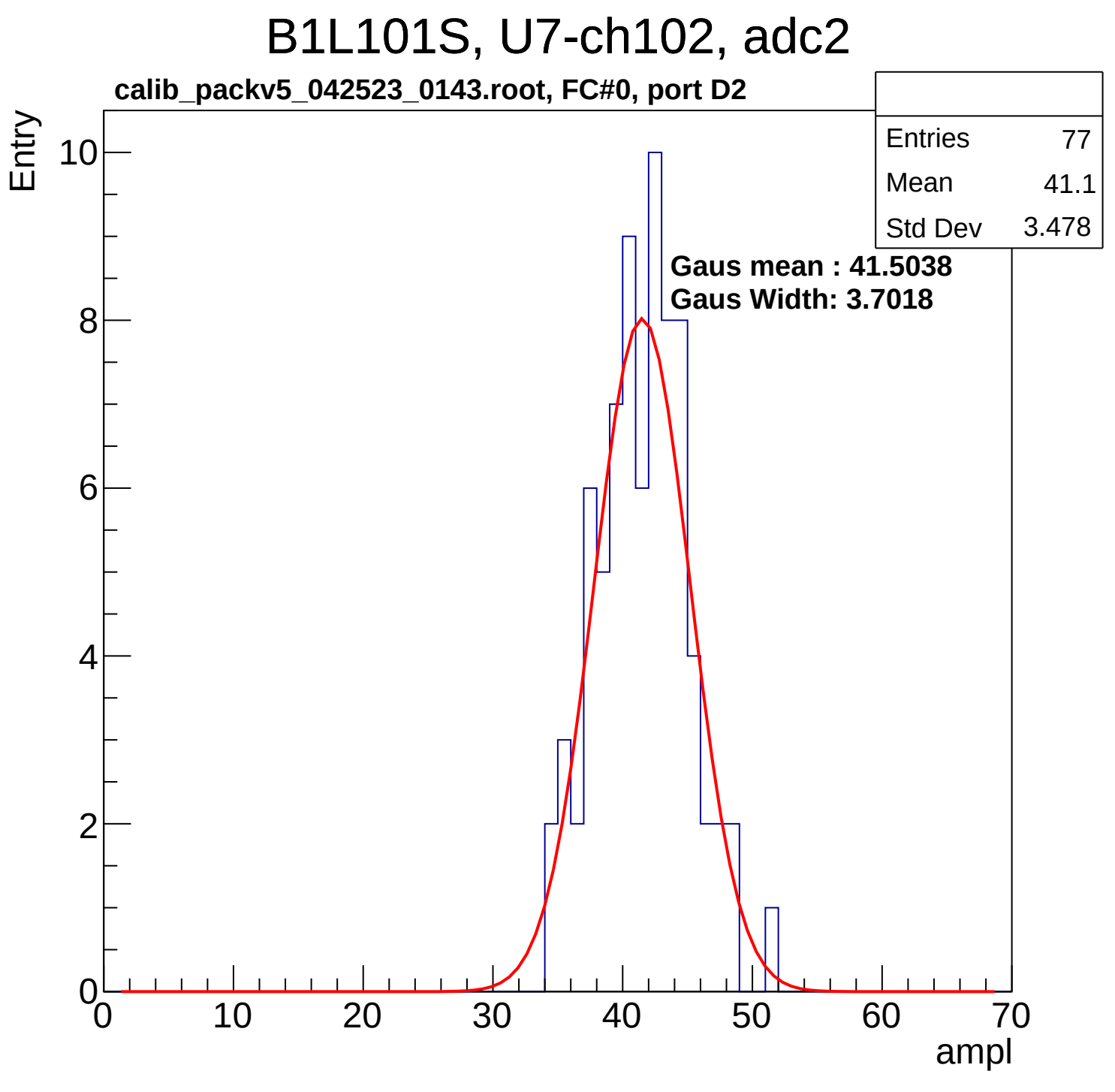
50
60
70
ampl


B1L101S, U7-ch102, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 27.73
Std Dev 4.673
Gaus mean : 28.7824
Gaus Width: 2.9854
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch102, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 34.37
Std Dev 3.65
Gaus mean : 34.6851
Gaus Width: 3.6543
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch102, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 41.1
Std Dev 3.478
Gaus mean : 41.5038
Gaus Width: 3.7018
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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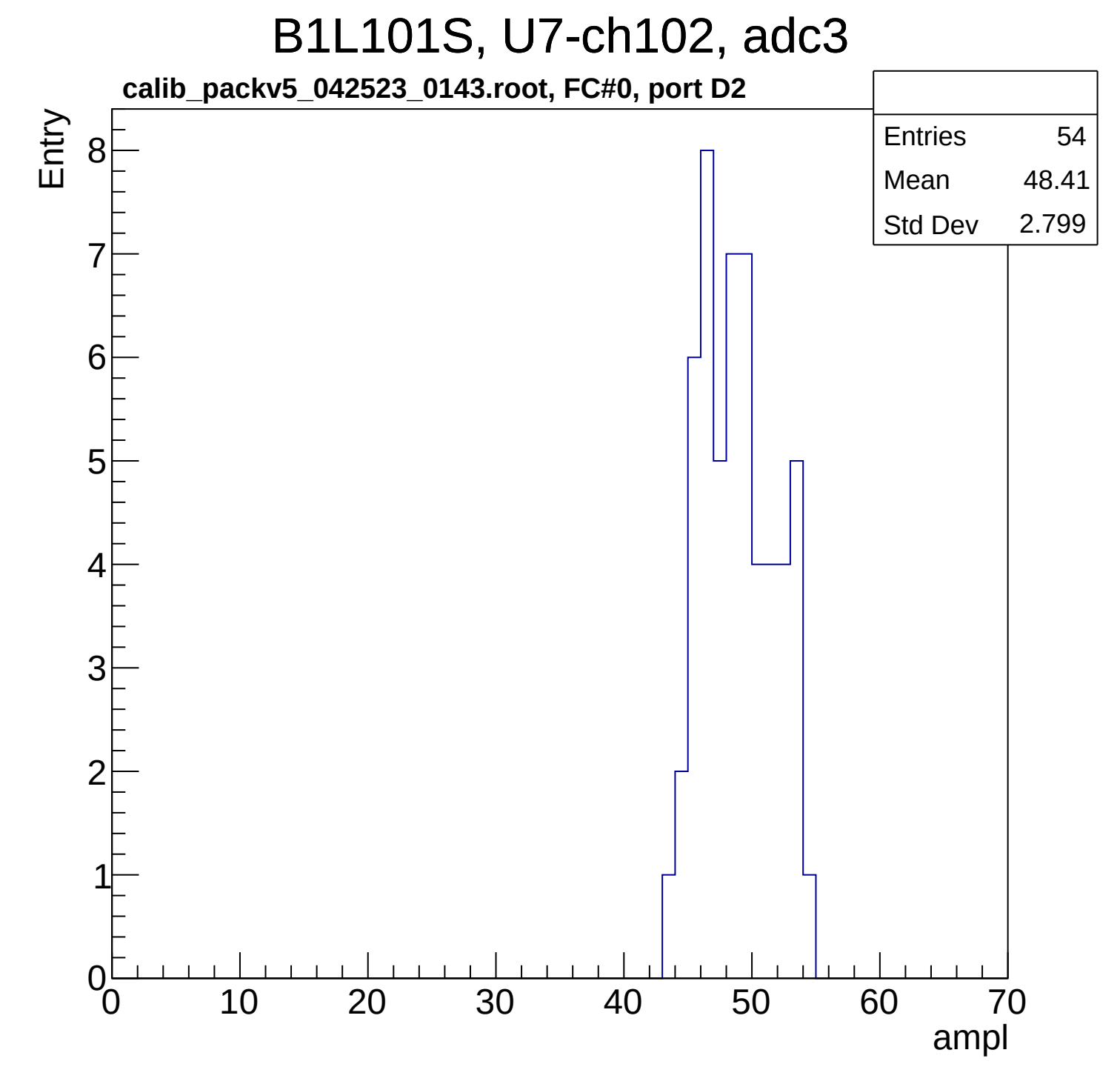
B1L101S, U7-ch102, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 48.41
Std Dev 2.799
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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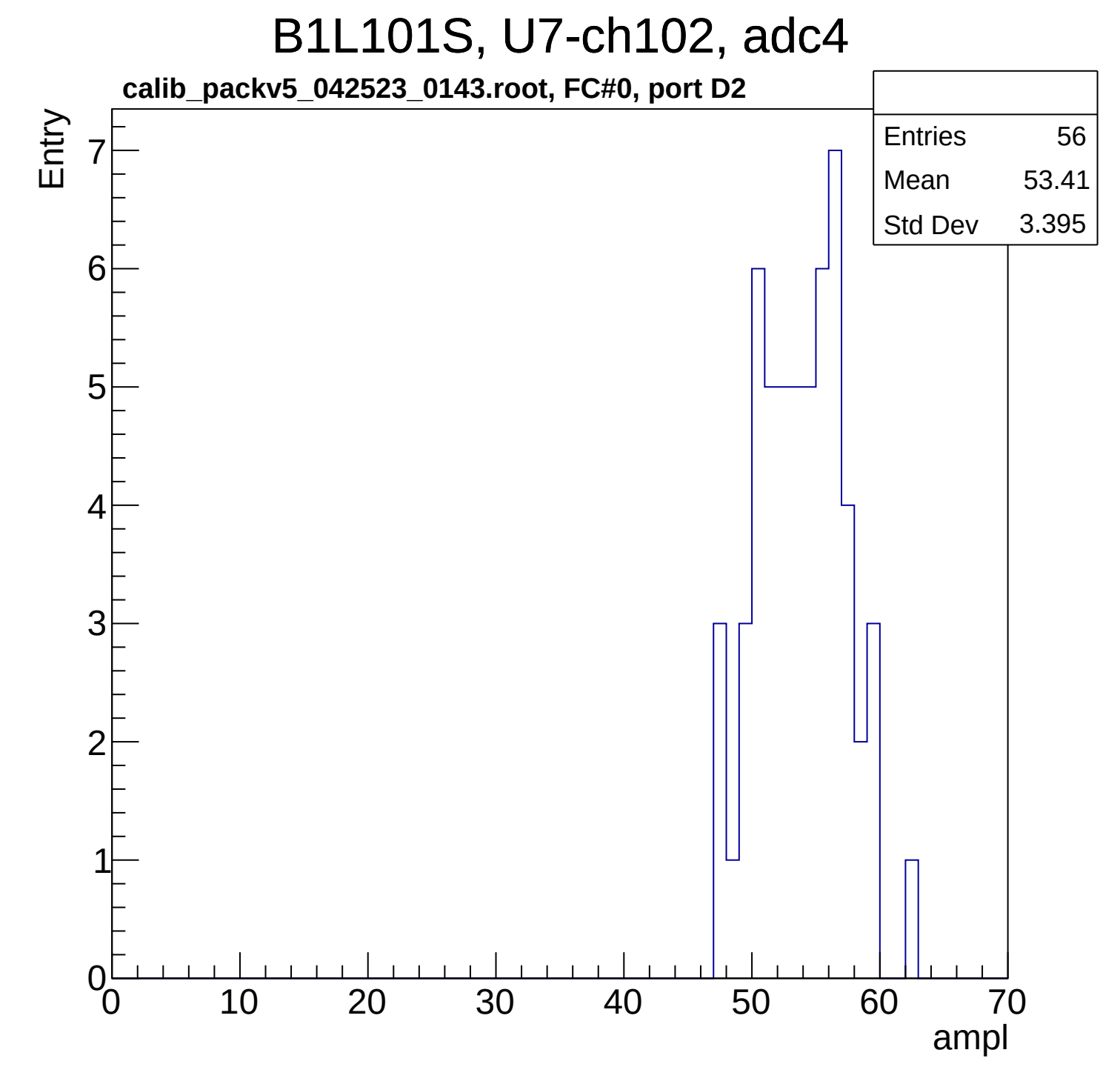
B1L101S, U7-ch102, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 53.41
Std Dev 3.395
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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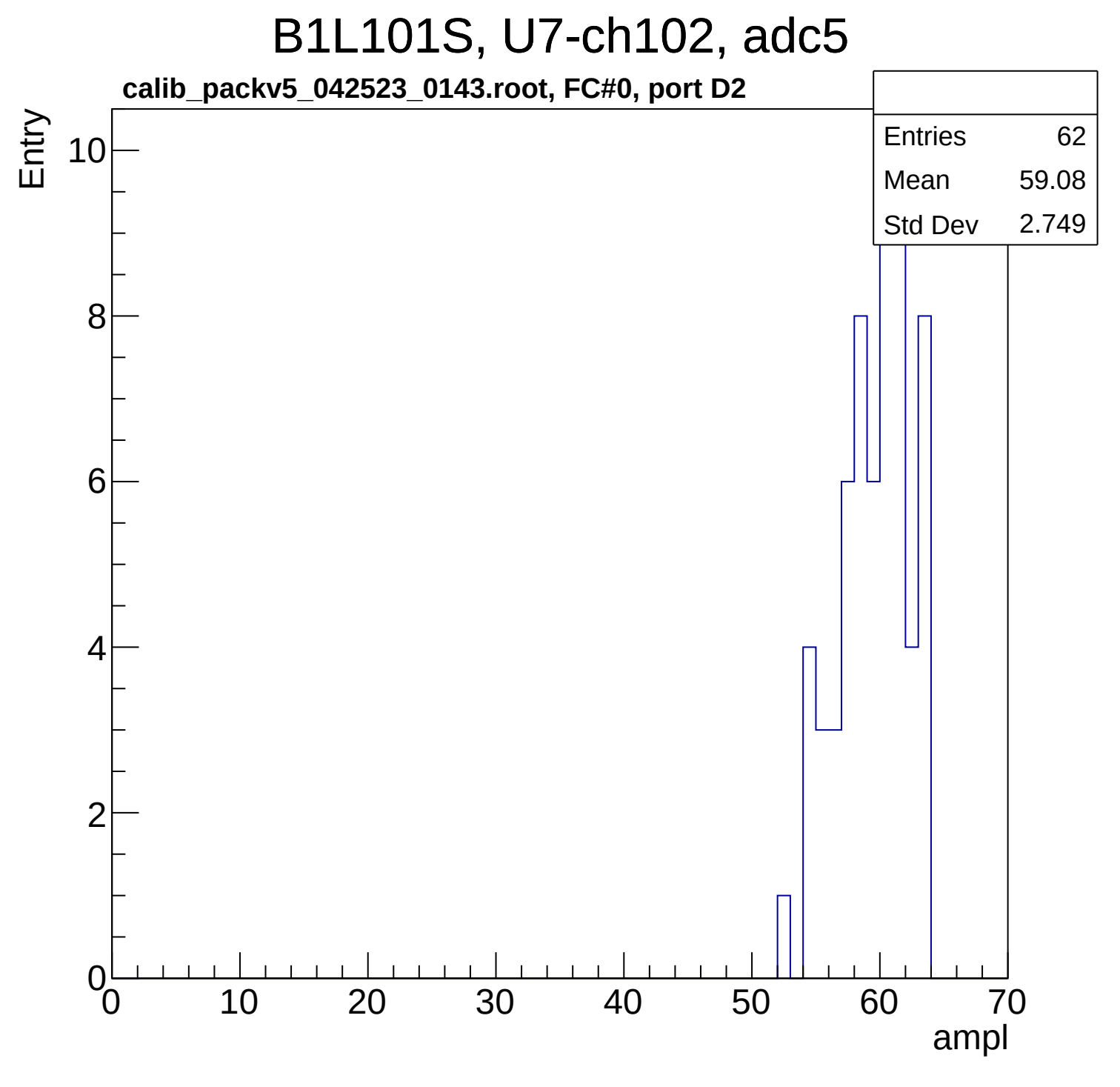
50
60
70


B1L101S, U7-ch102, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 59.08
Std Dev 2.749
Entry
ampl
0
2
4
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0
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60
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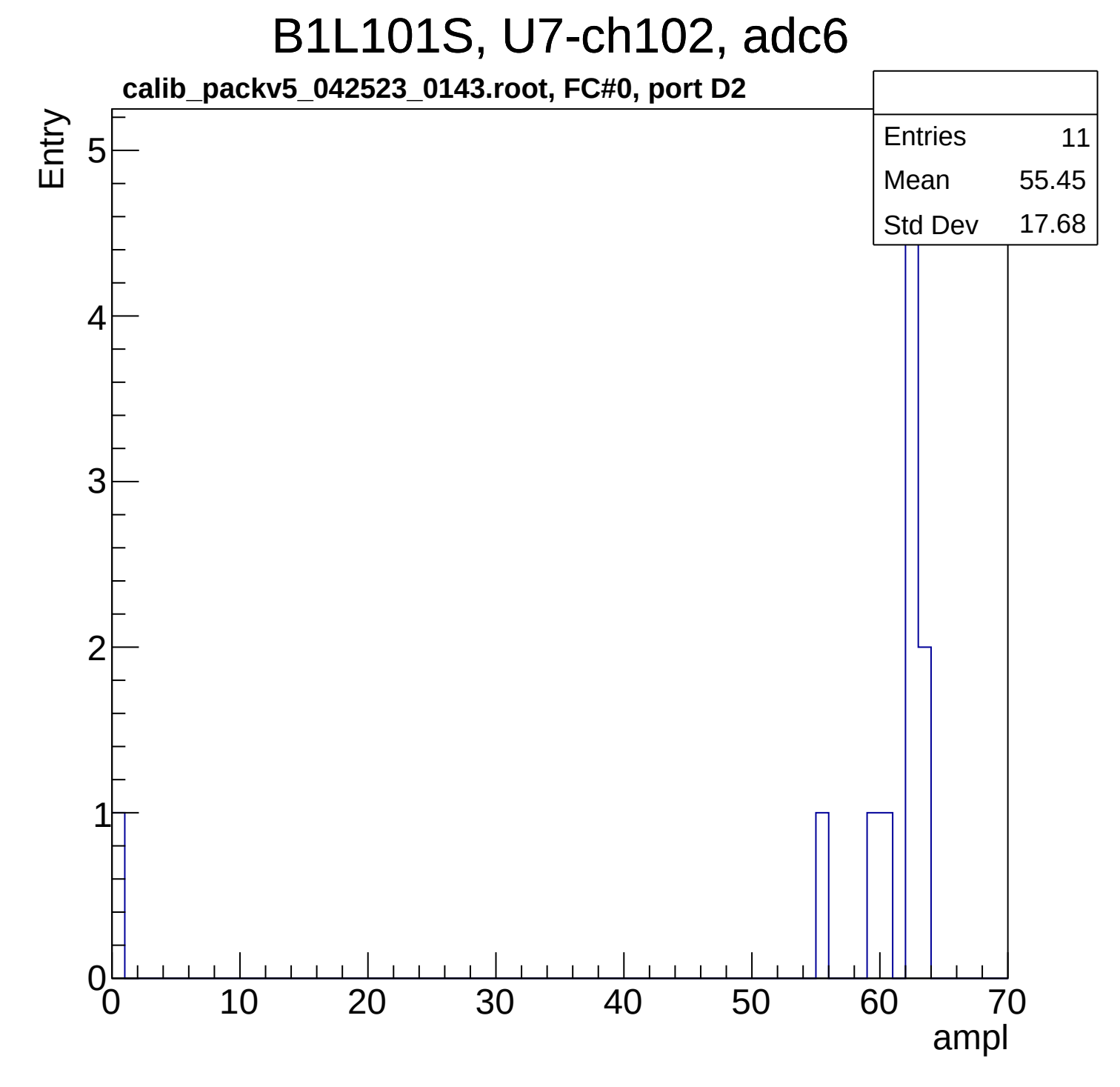
B1L101S, U7-ch102, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 11
Mean 55.45
Std Dev 17.68
Entry
ampl
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1
2
3
4
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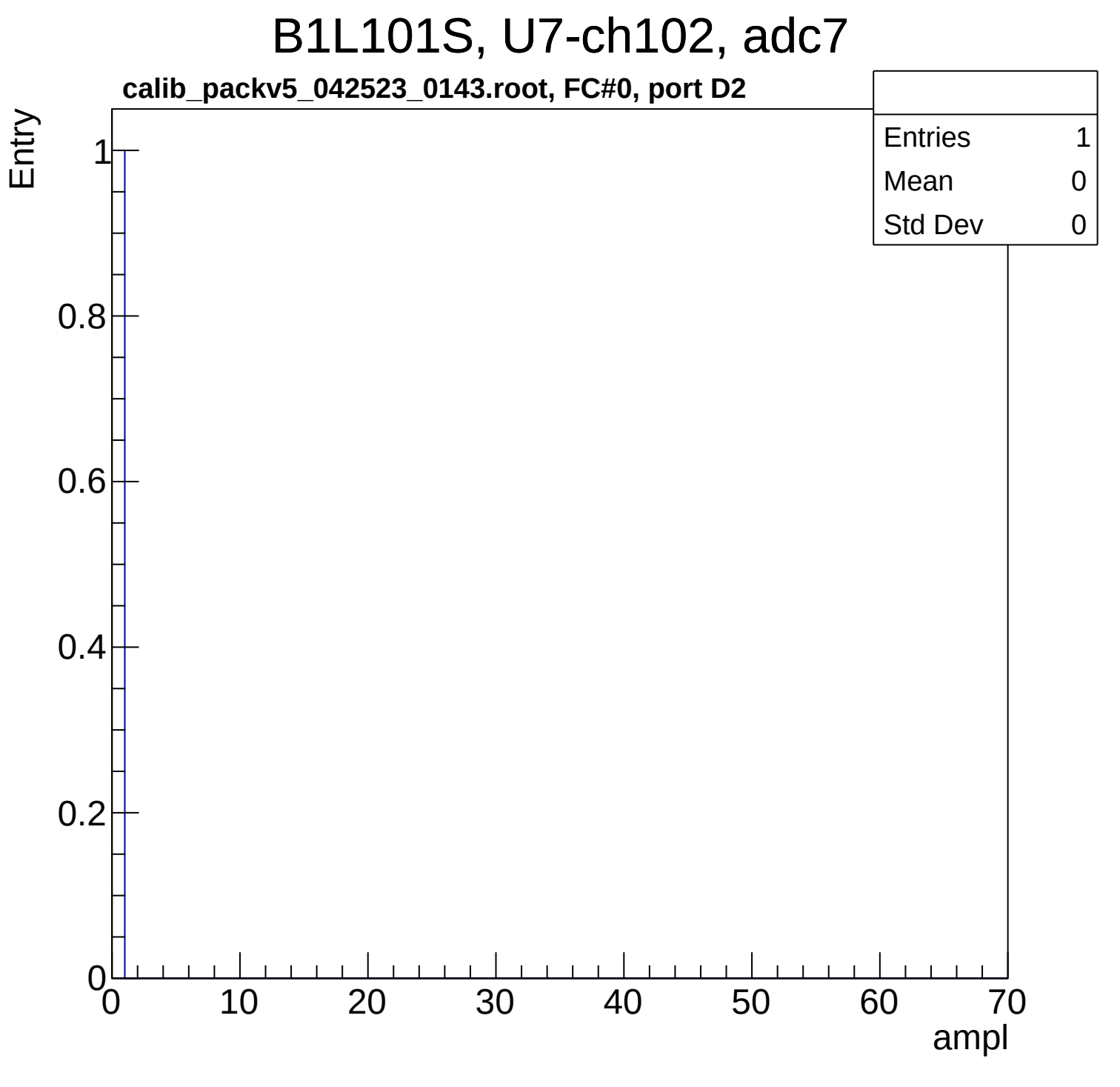
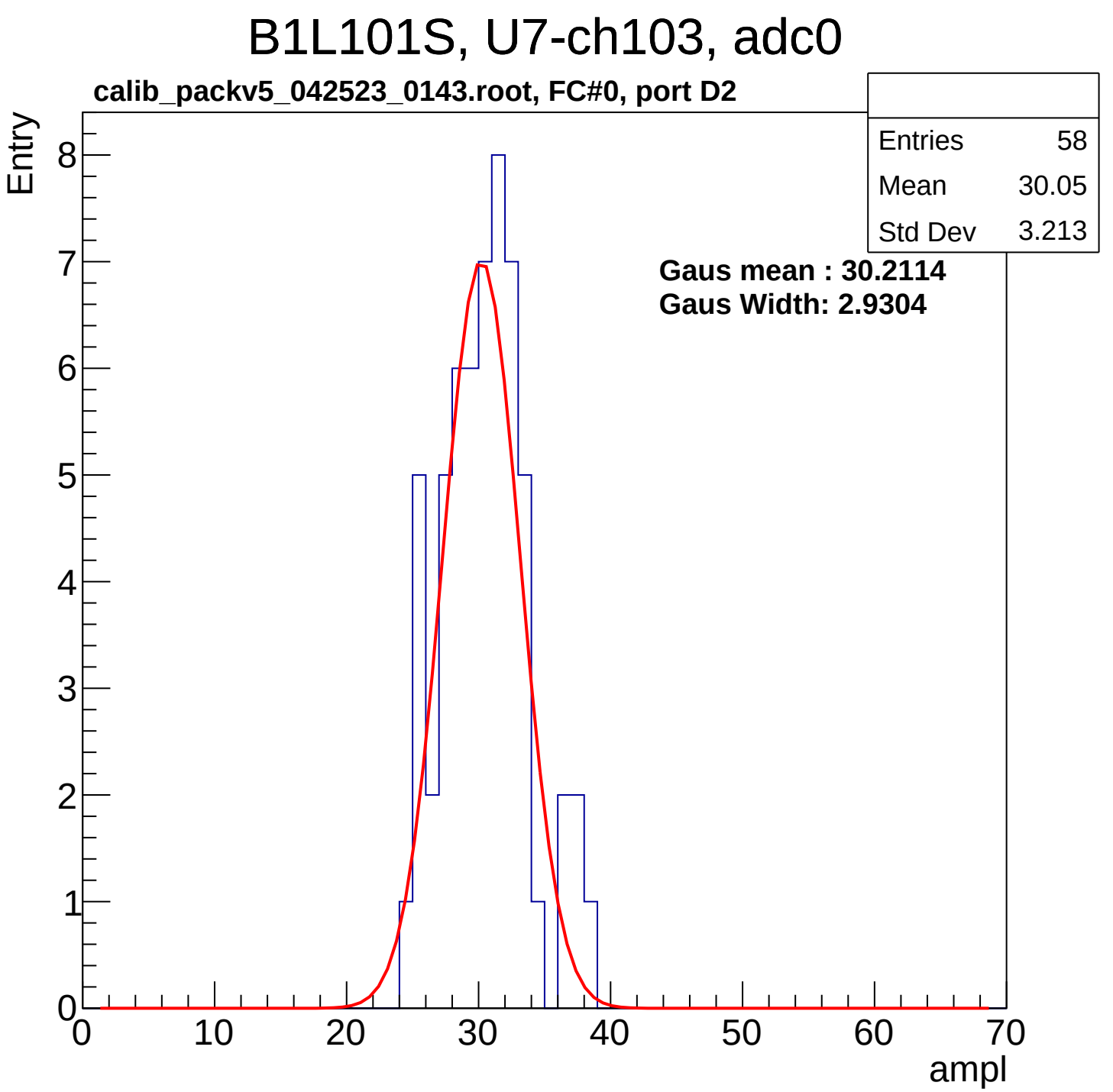
0
10
20
30
40
50
60
70


B1L101S, U7-ch102, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch103, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 30.05
Std Dev 3.213
Gaus mean : 30.2114
Gaus Width: 2.9304
Entry
ampl
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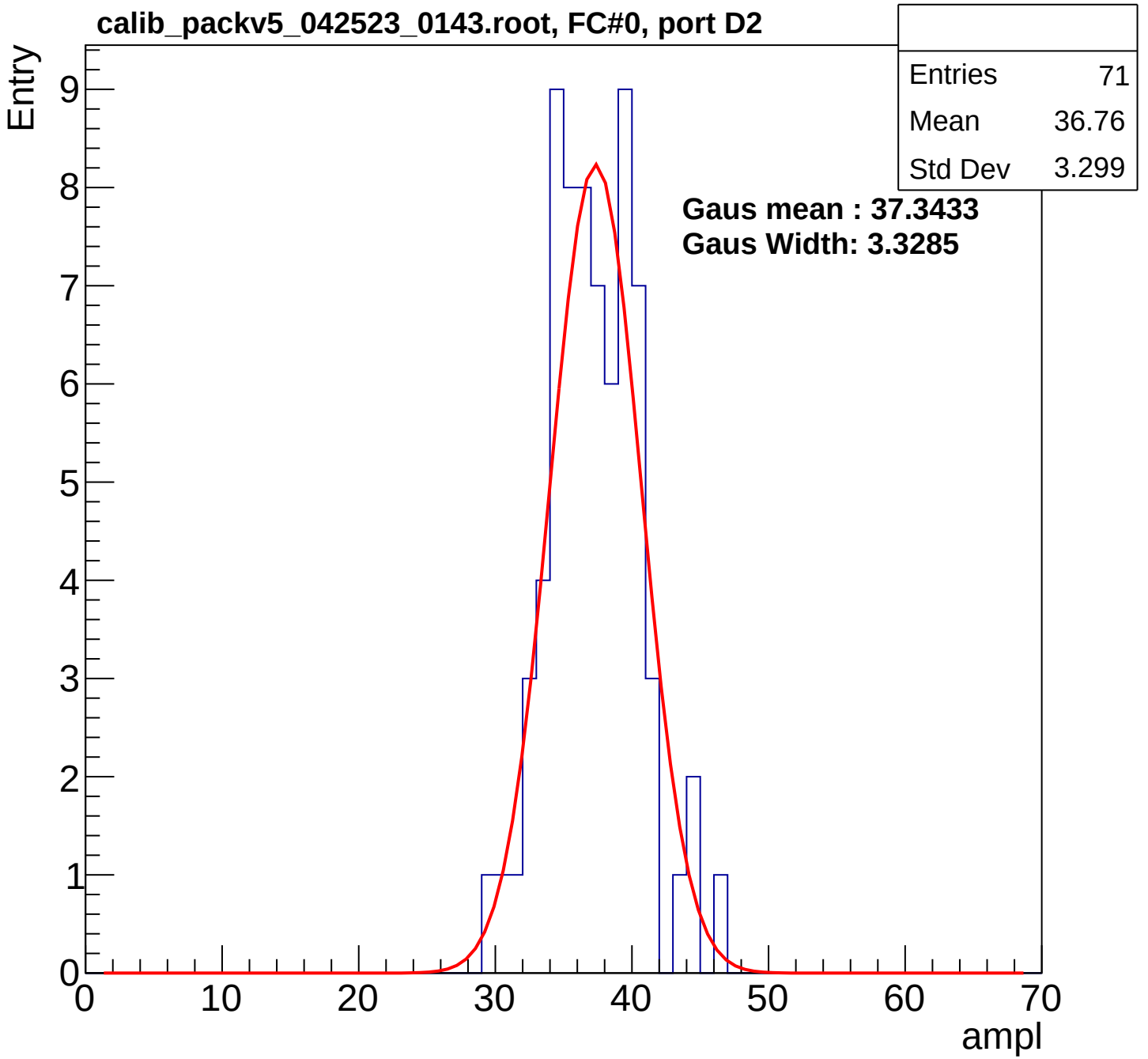
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch103, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 36.76
Std Dev 3.299
Gaus mean : 37.3433
Gaus Width: 3.3285
Entry
ampl
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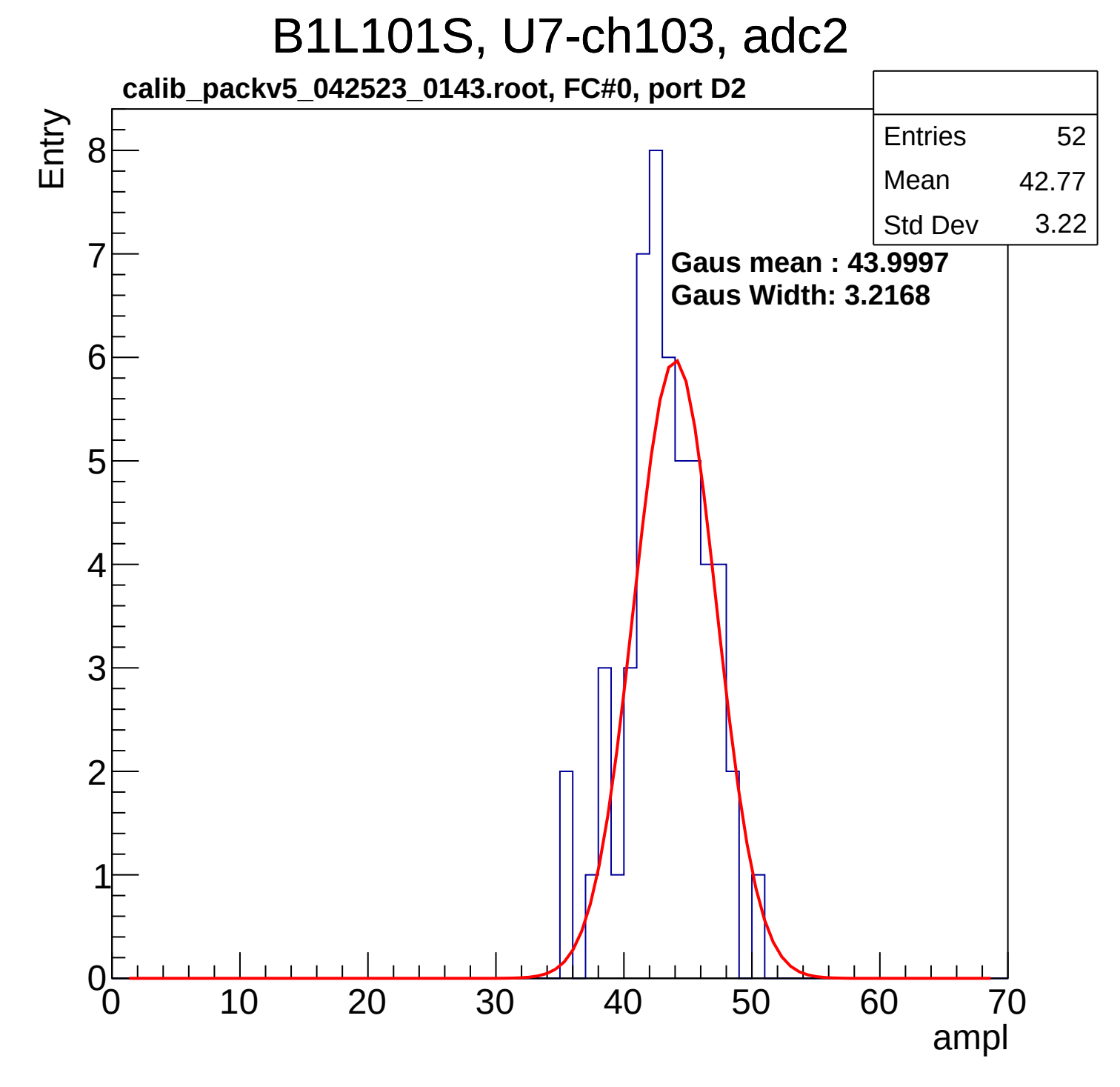
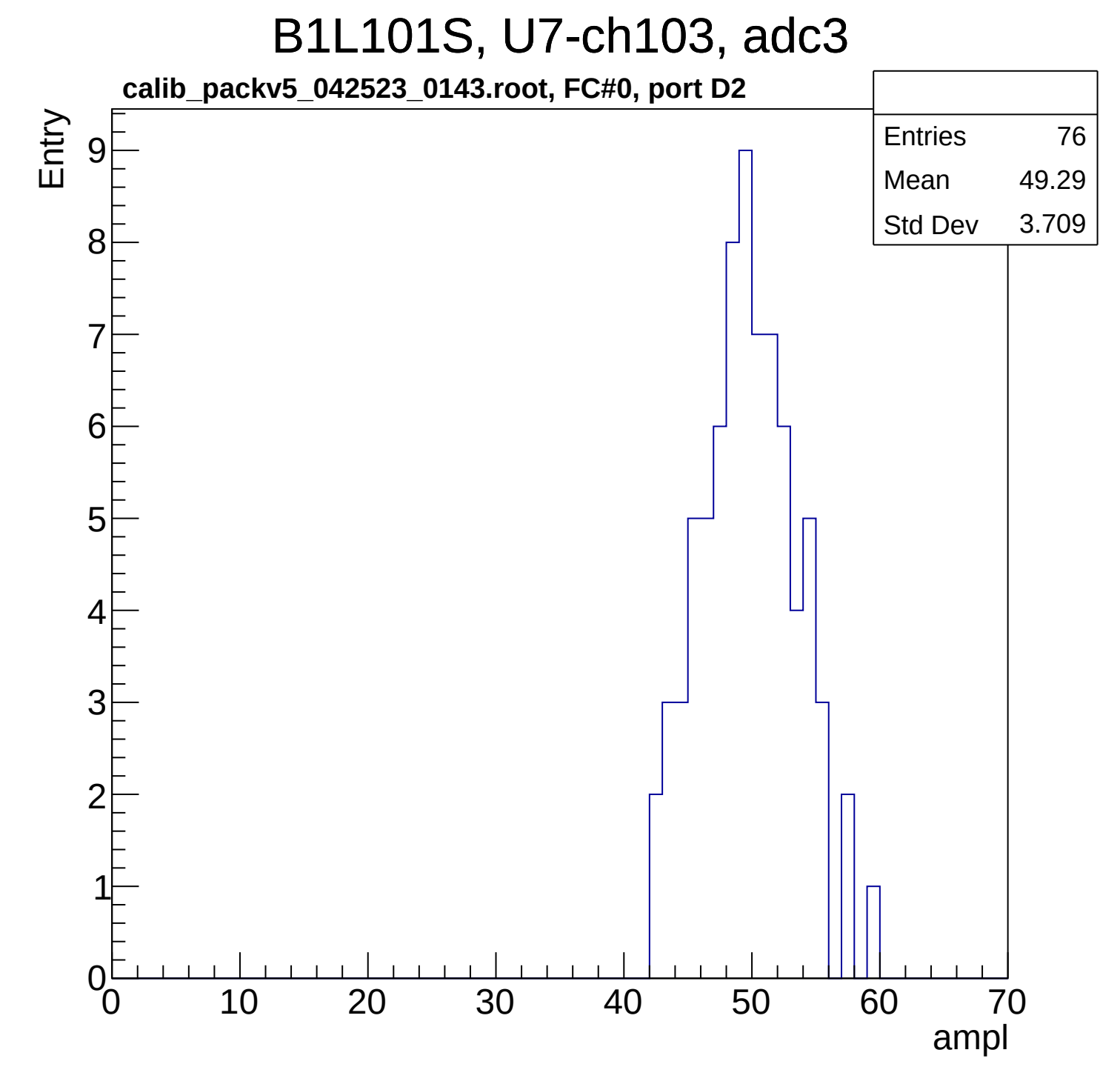
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch103, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 42.77
Std Dev 3.22
Gaus mean : 43.9997
Gaus Width: 3.2168
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch103, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 49.29
Std Dev 3.709
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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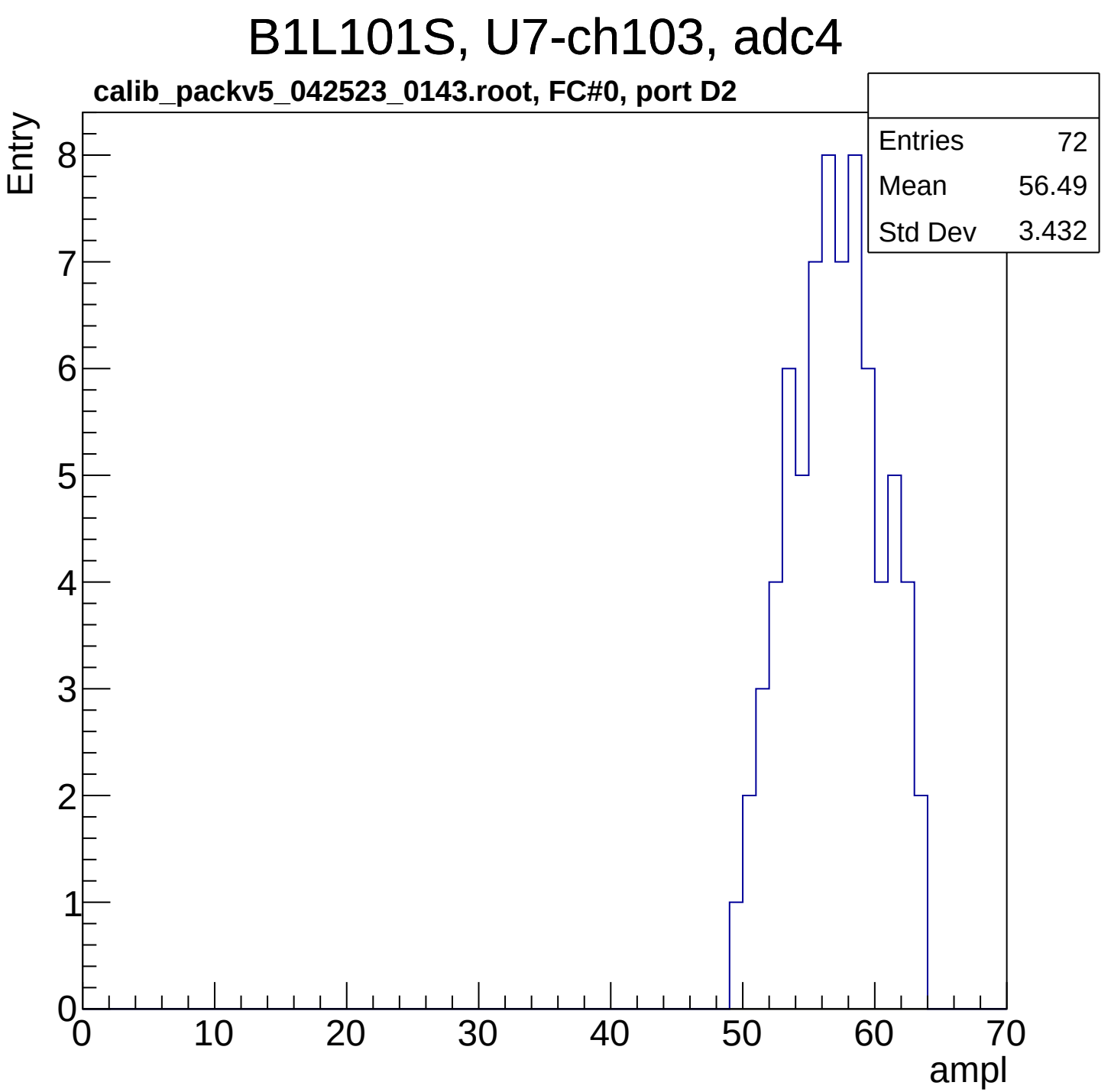
B1L101S, U7-ch103, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 56.49
Std Dev 3.432
Entry
ampl
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1
2
3
4
5
6
7
8
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20
30
40
50
60
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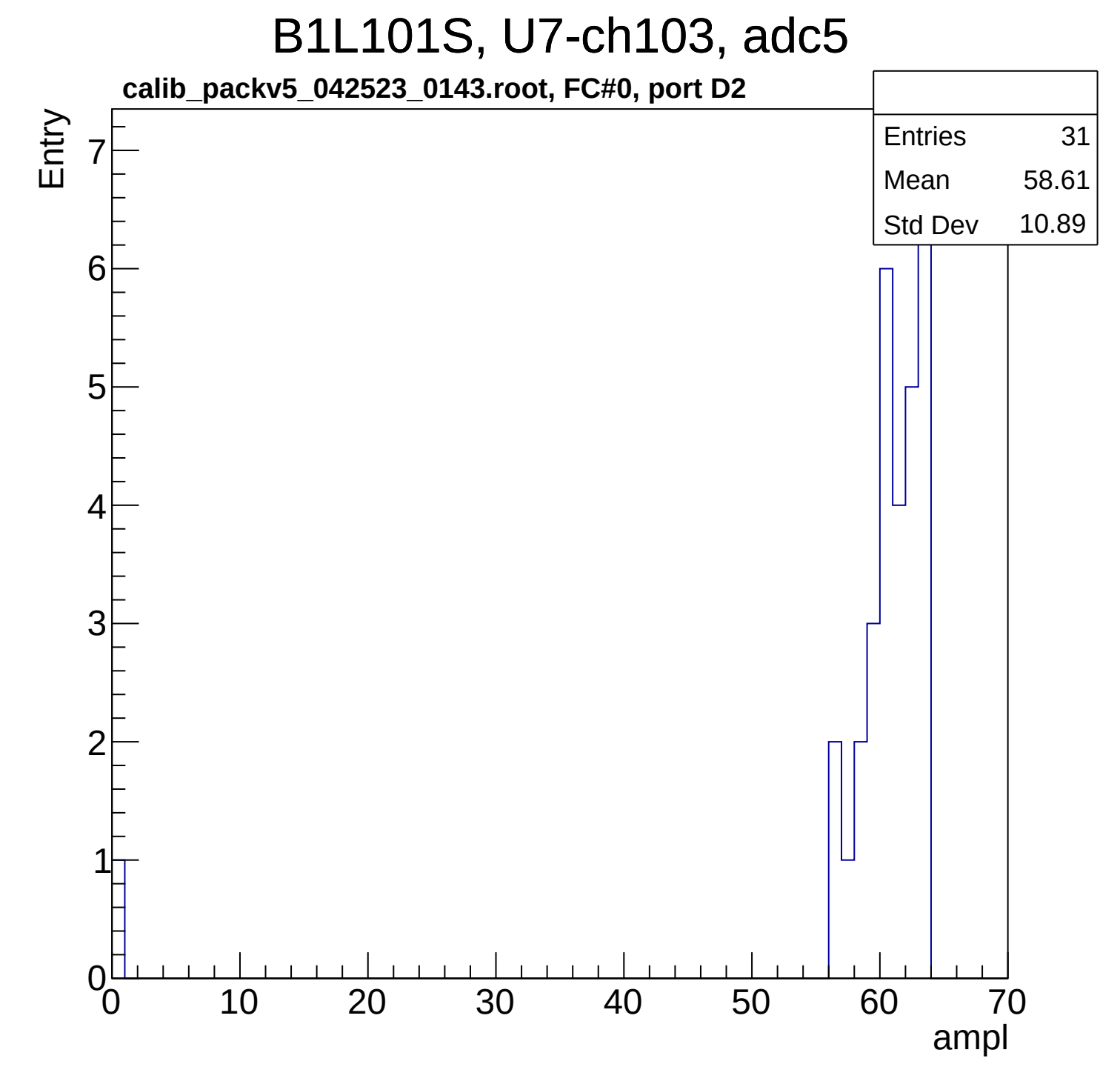
B1L101S, U7-ch103, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 31
Mean 58.61
Std Dev 10.89
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
30
40
50
60
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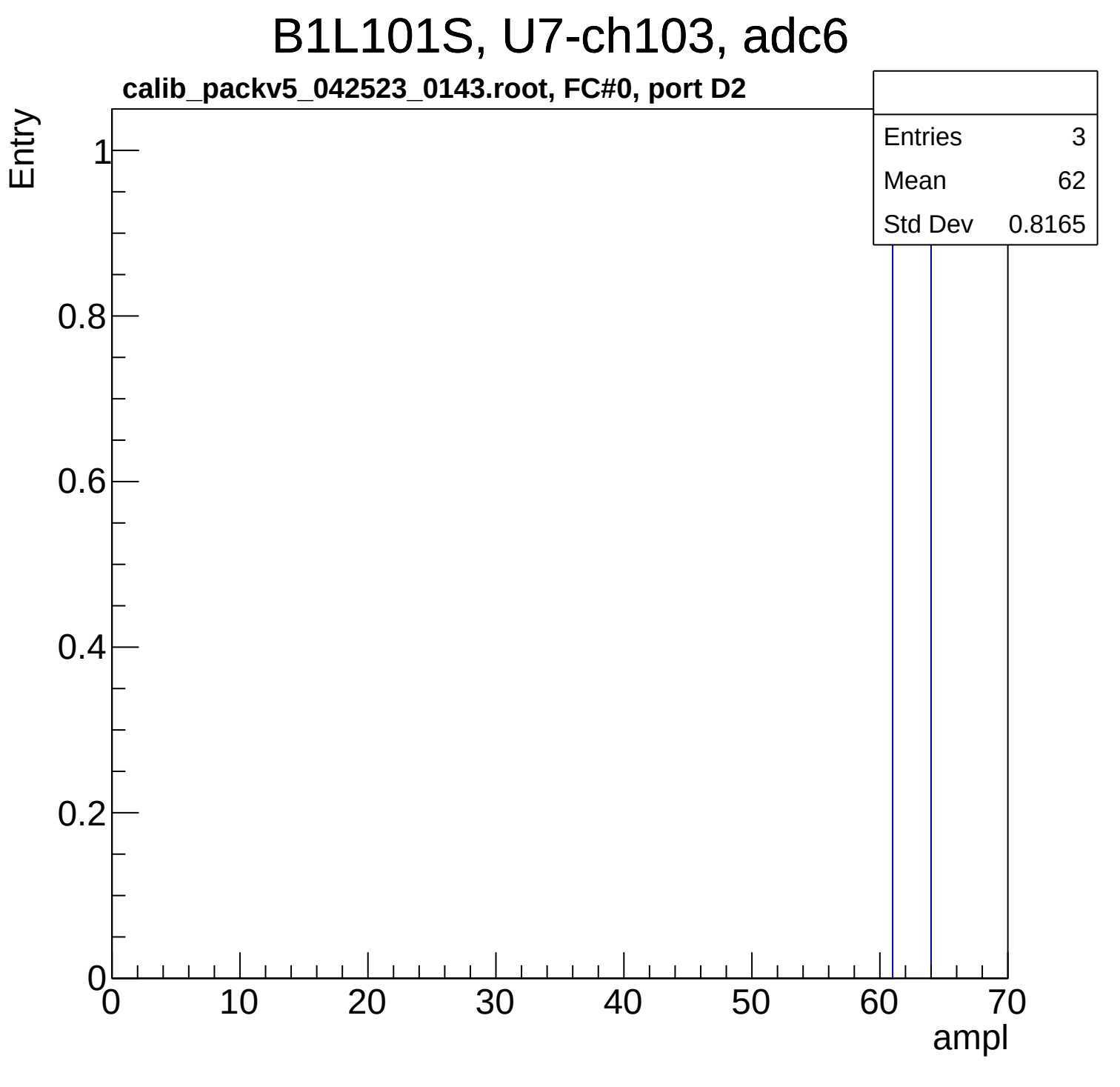
B1L101S, U7-ch103, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 62
Std Dev 0.8165
Entry
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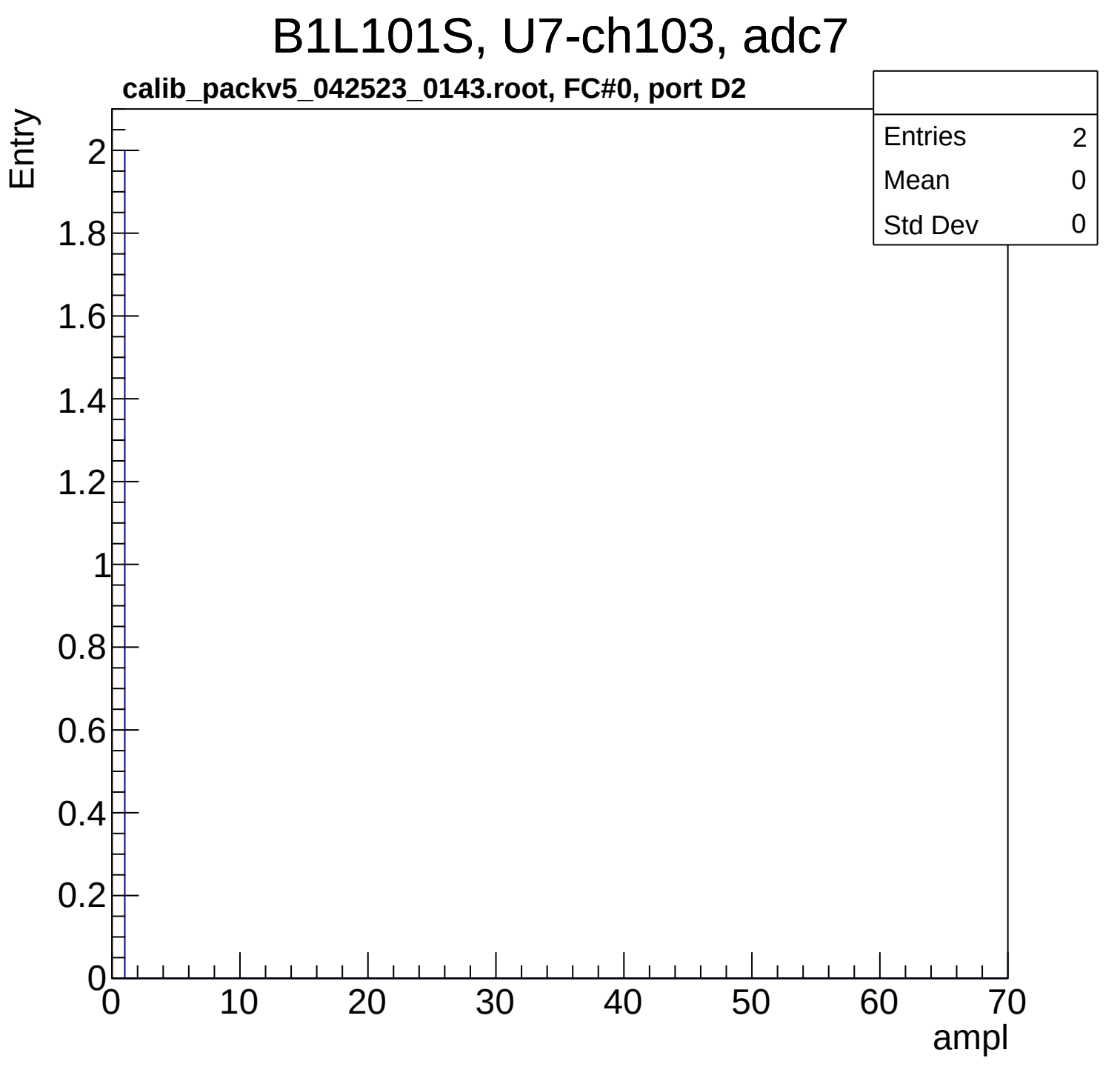
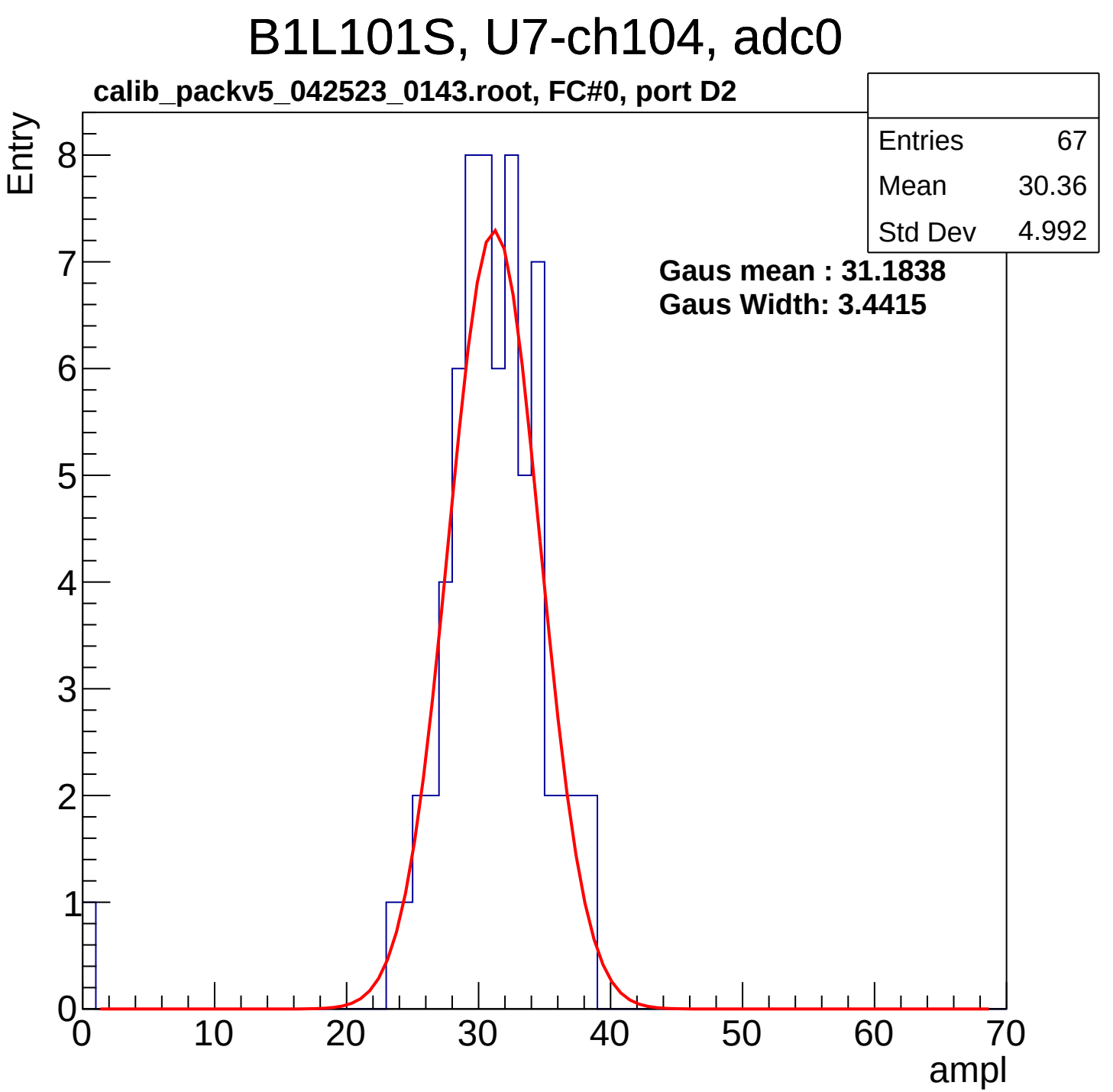
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch103, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U7-ch104, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 30.36
Std Dev 4.992
Gaus mean : 31.1838
Gaus Width: 3.4415
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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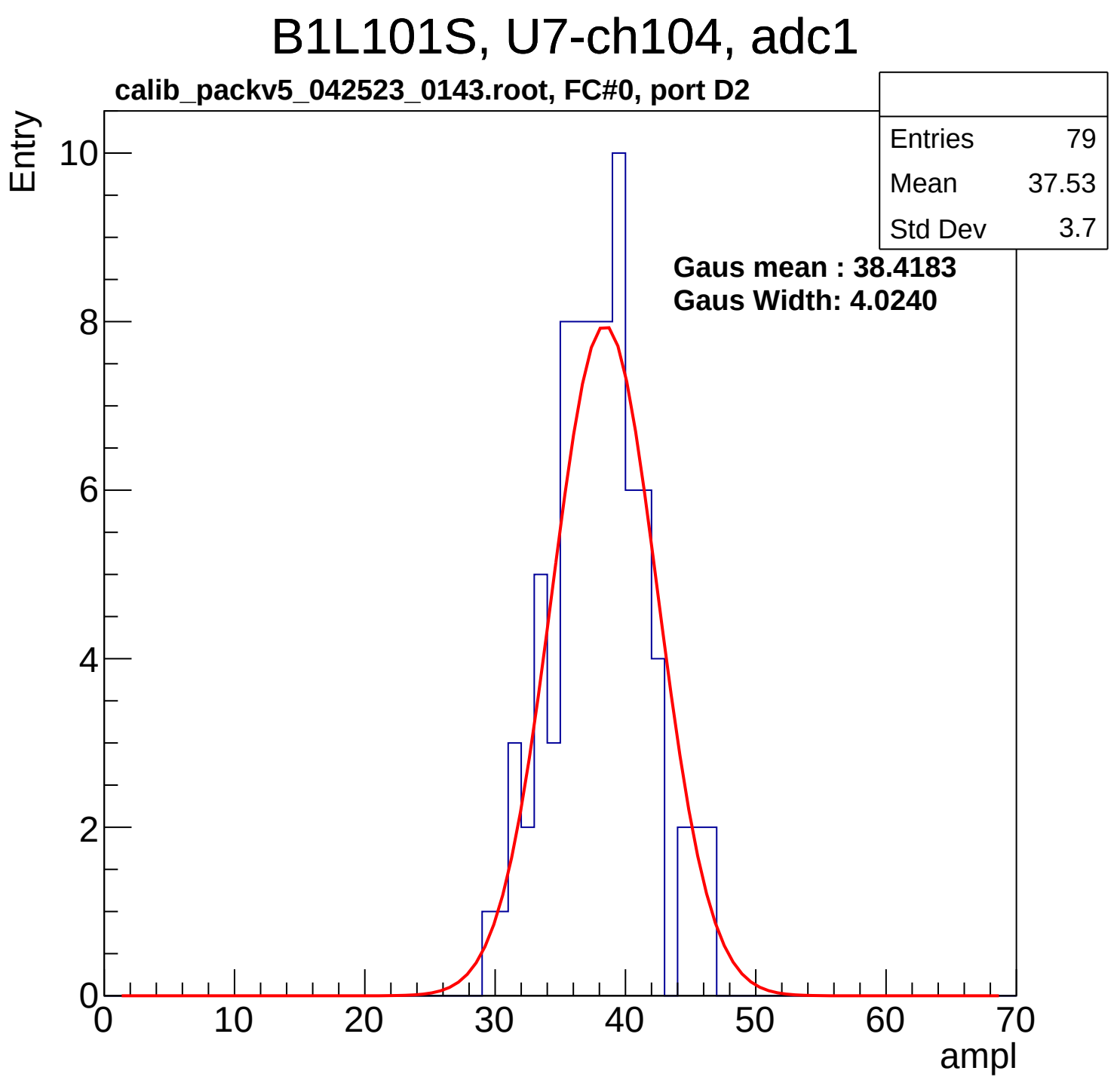
B1L101S, U7-ch104, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 37.53
Std Dev 3.7
Gaus mean : 38.4183
Gaus Width: 4.0240
Entry
ampl
0
2
4
6
8
10
0
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30
40
50
60
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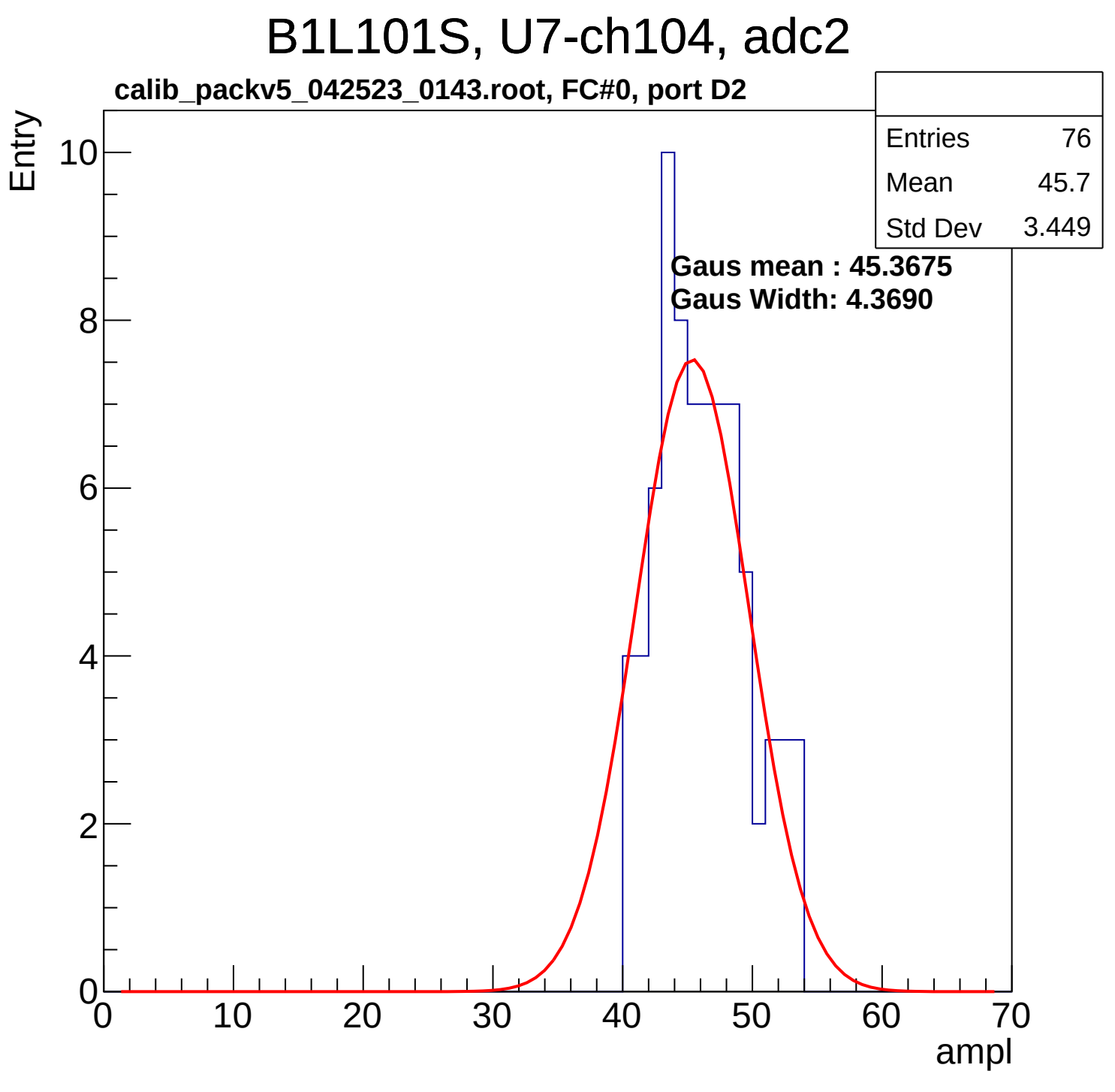
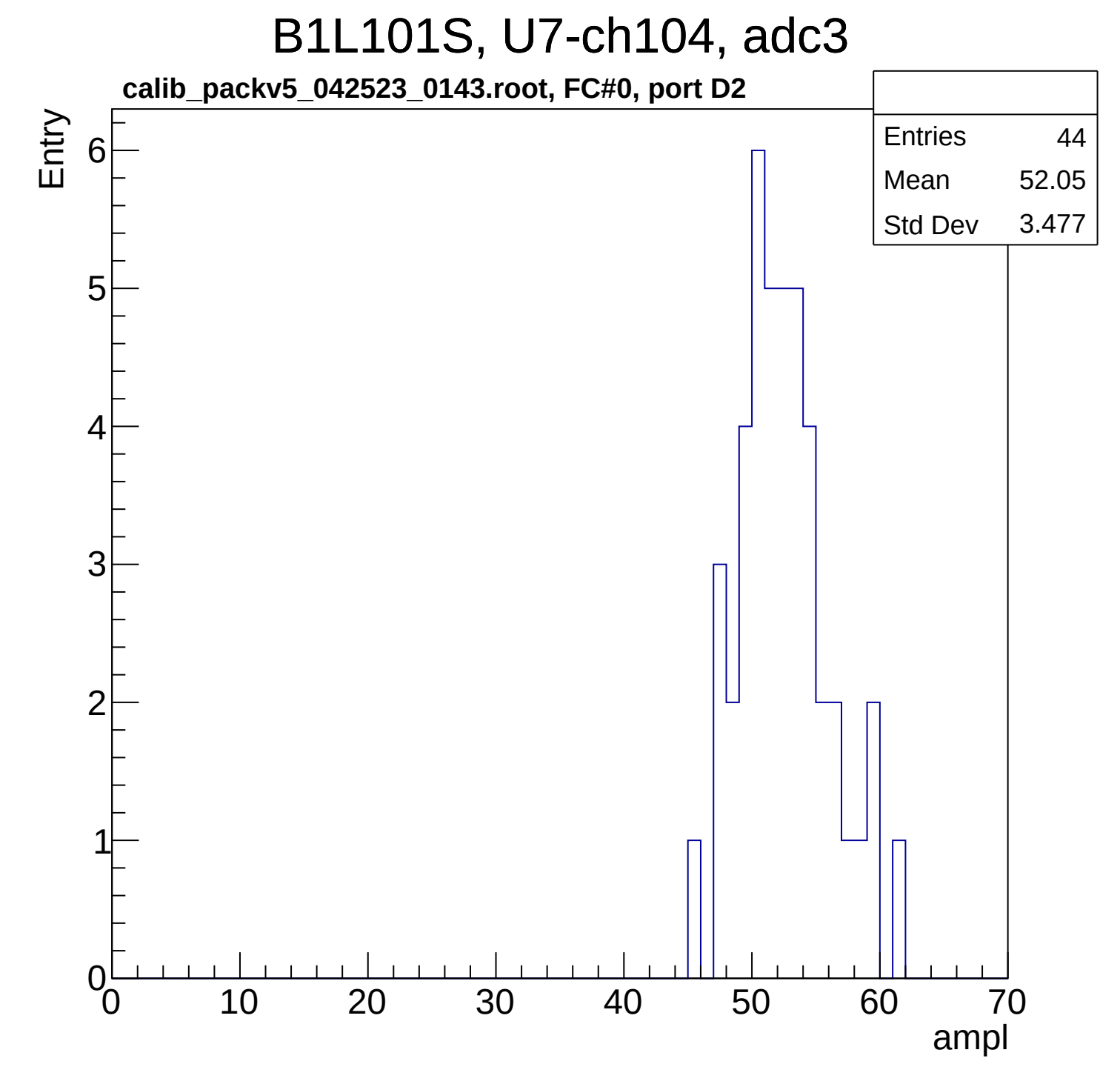

B1L101S, U7-ch104, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 45.7
Std Dev 3.449
Gaus mean : 45.3675
Gaus Width: 4.3690
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch104, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 44
Mean 52.05
Std Dev 3.477
Entry
ampl
0
1
2
3
4
5
6
0
10
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30
40
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60
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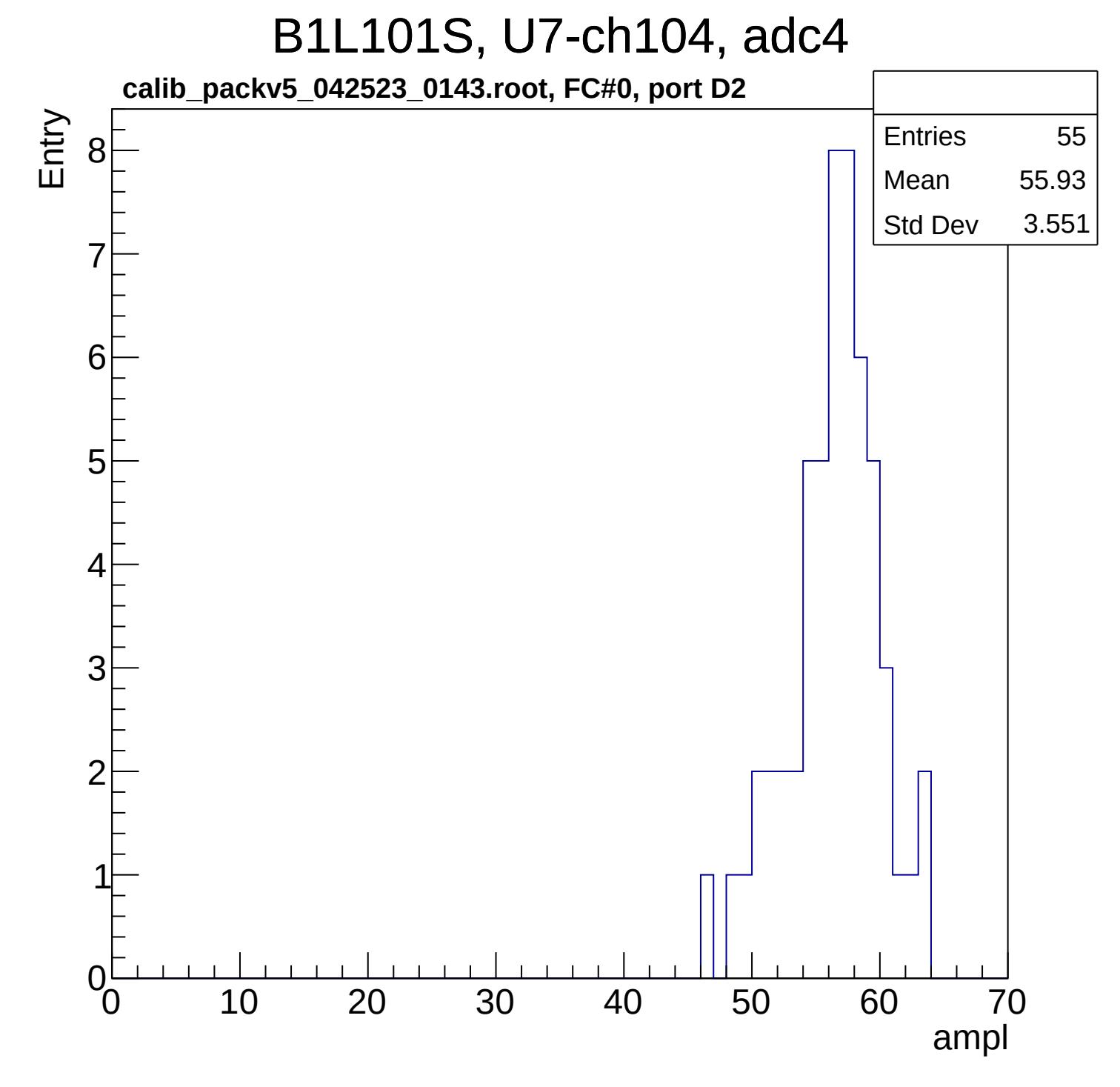
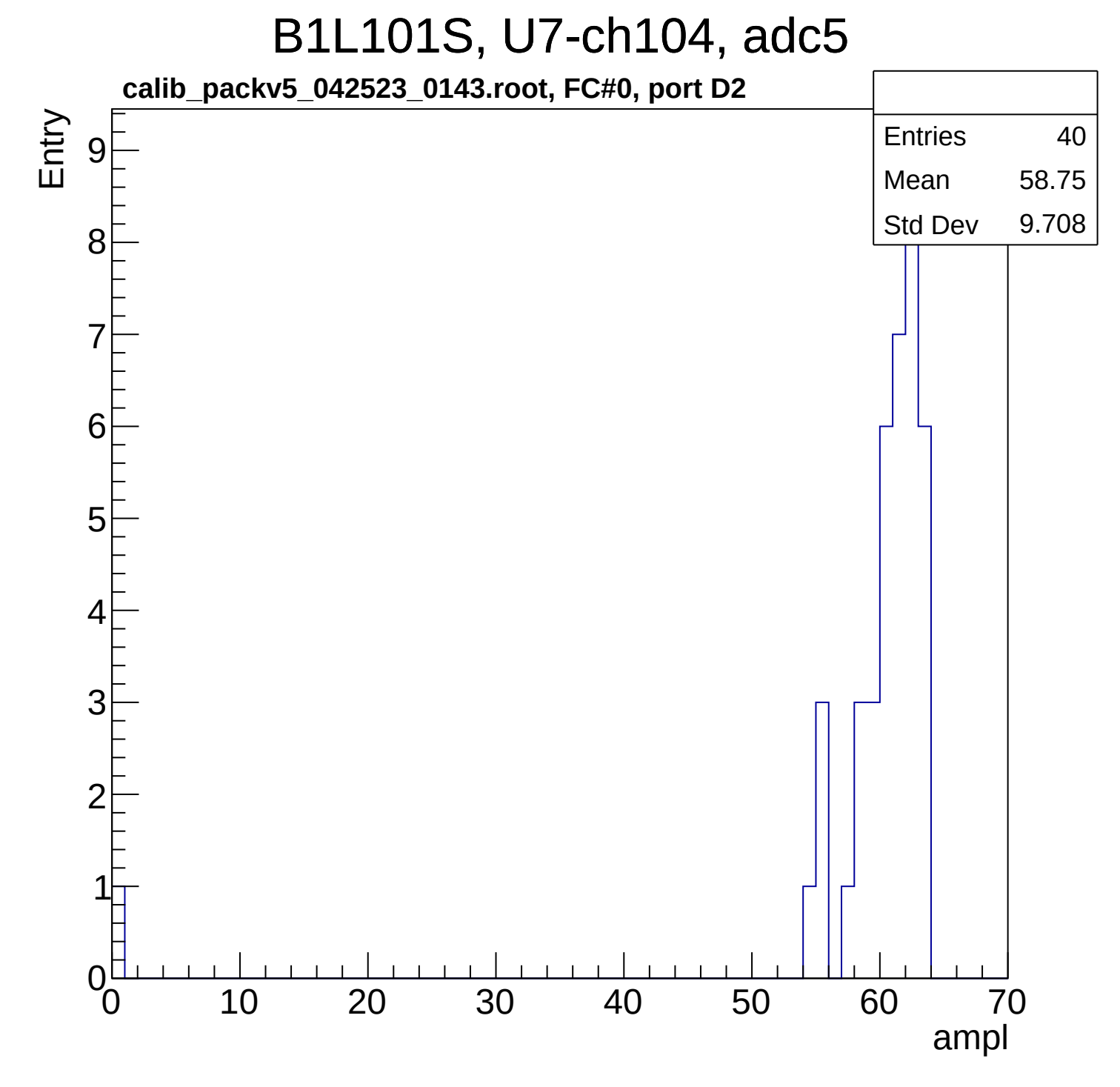

B1L101S, U7-ch104, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 55.93
Std Dev 3.551
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch104, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 40
Mean 58.75
Std Dev 9.708
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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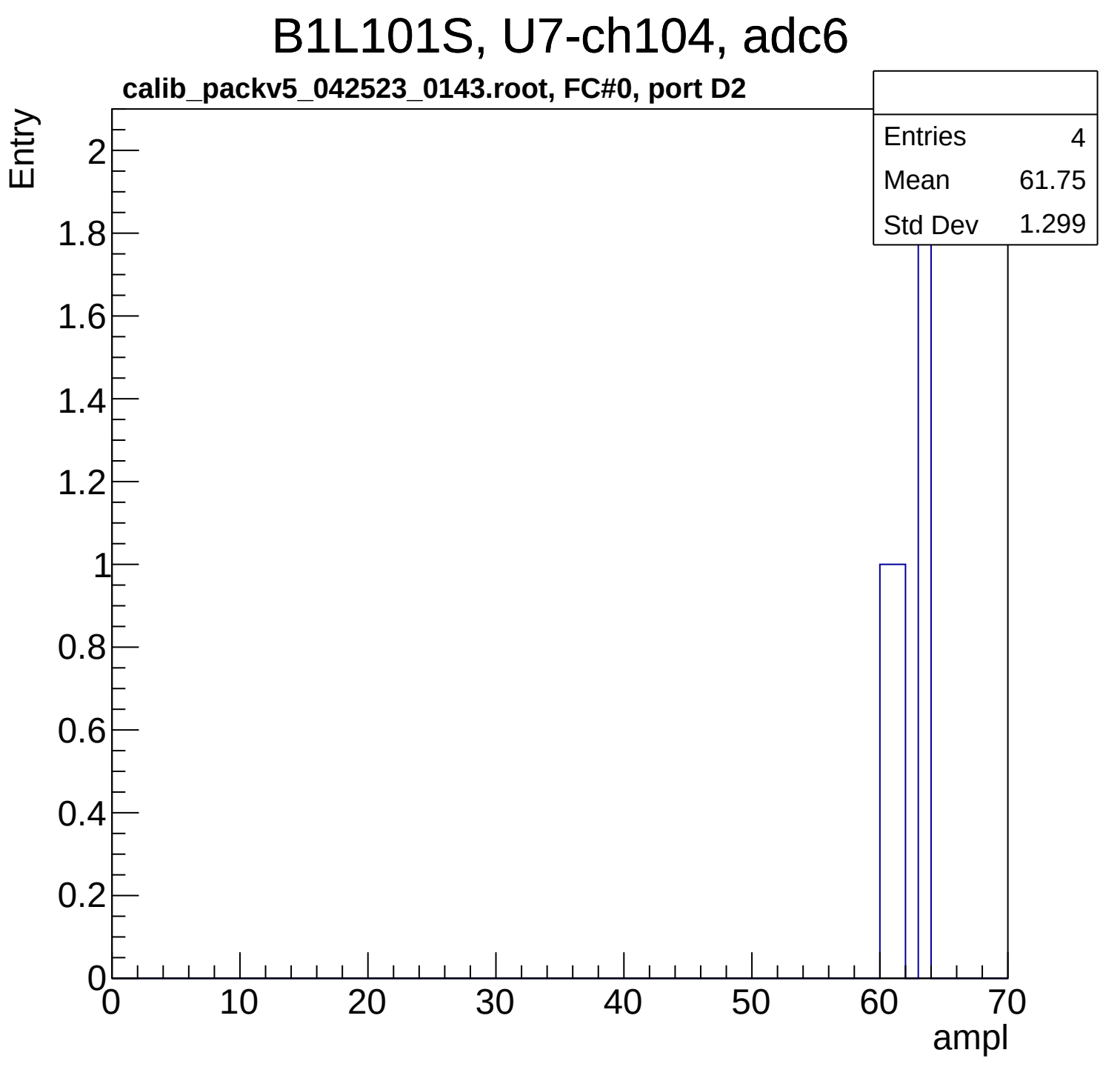
B1L101S, U7-ch104, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 61.75
Std Dev 1.299
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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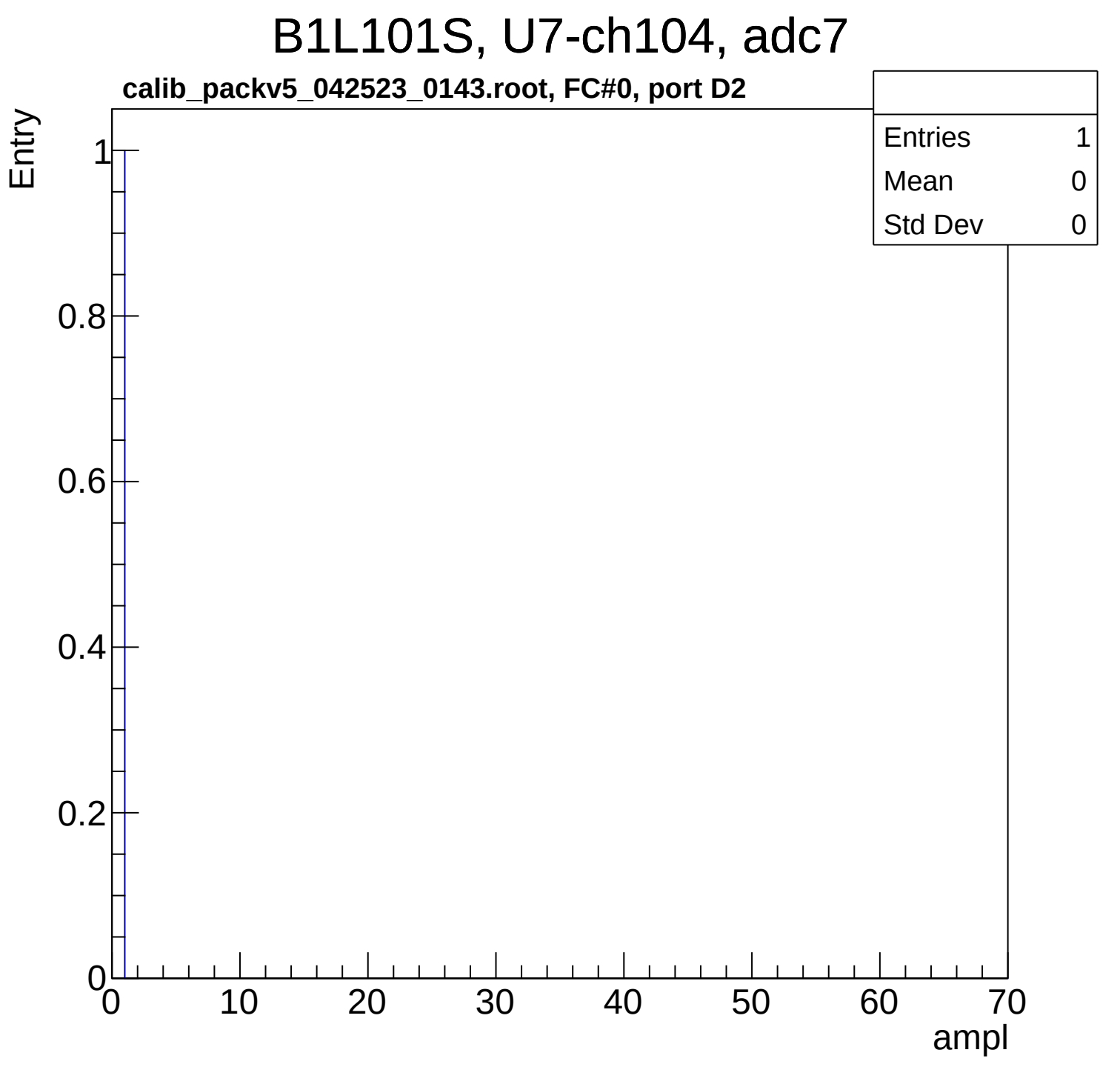
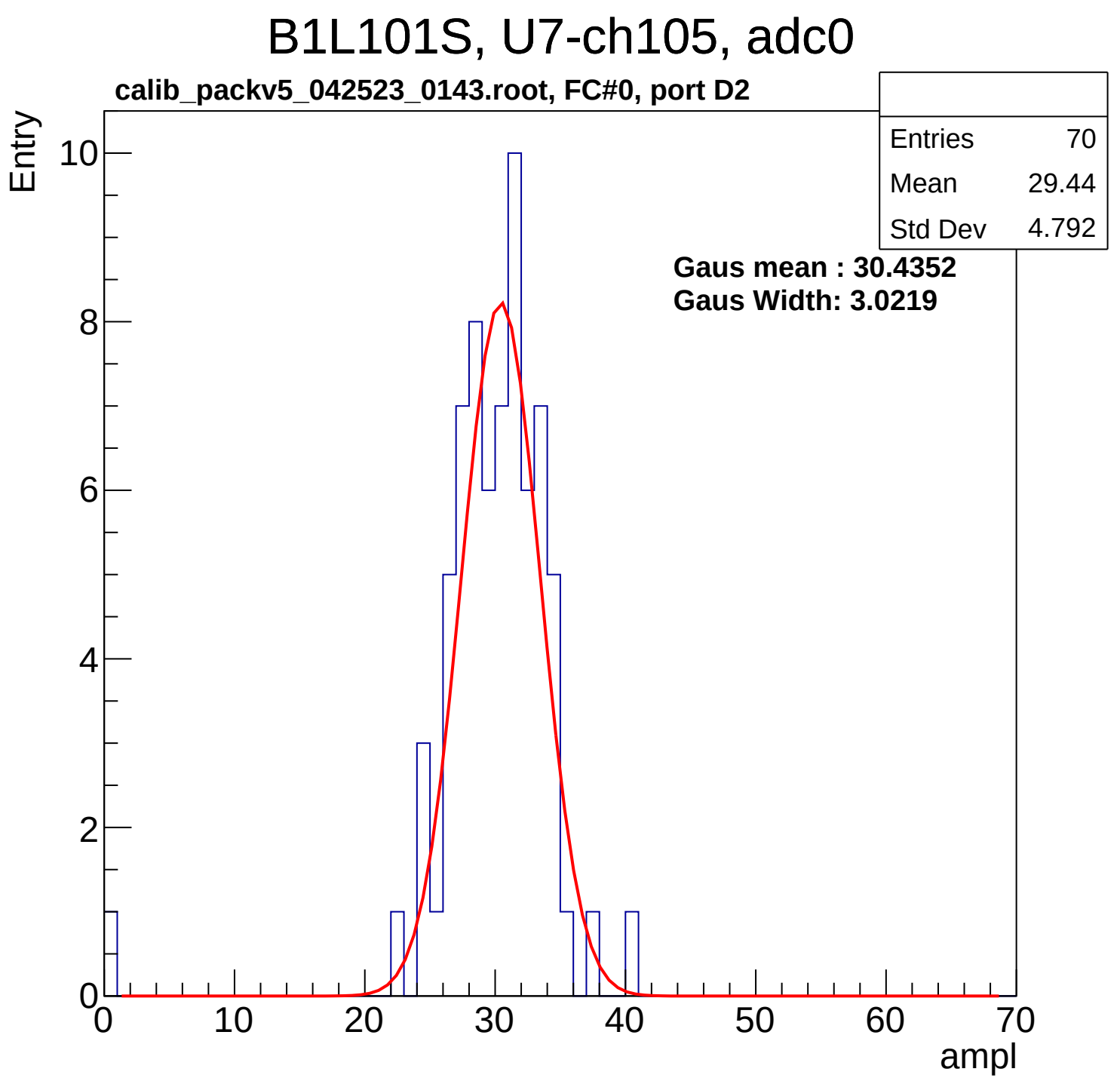
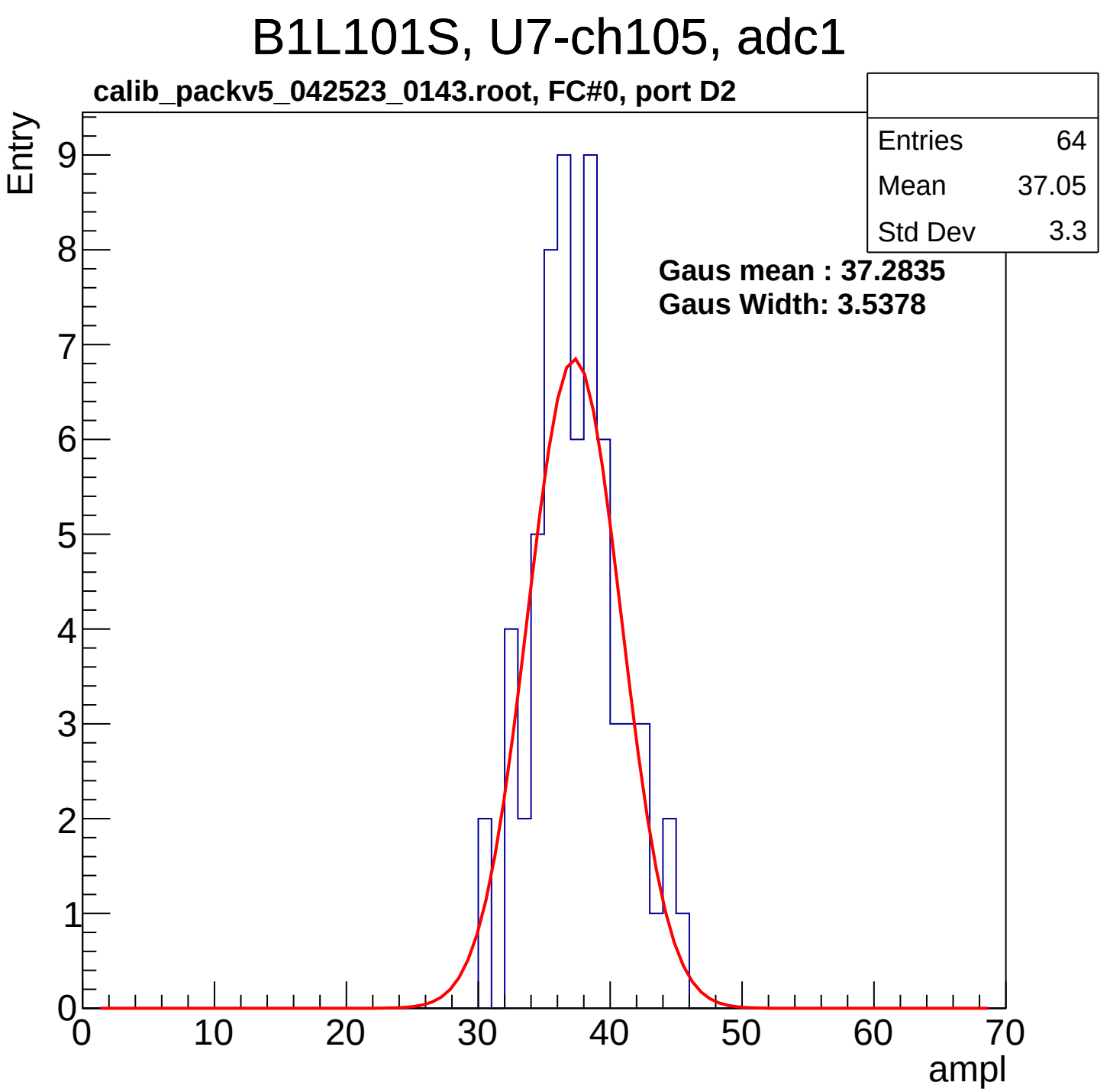
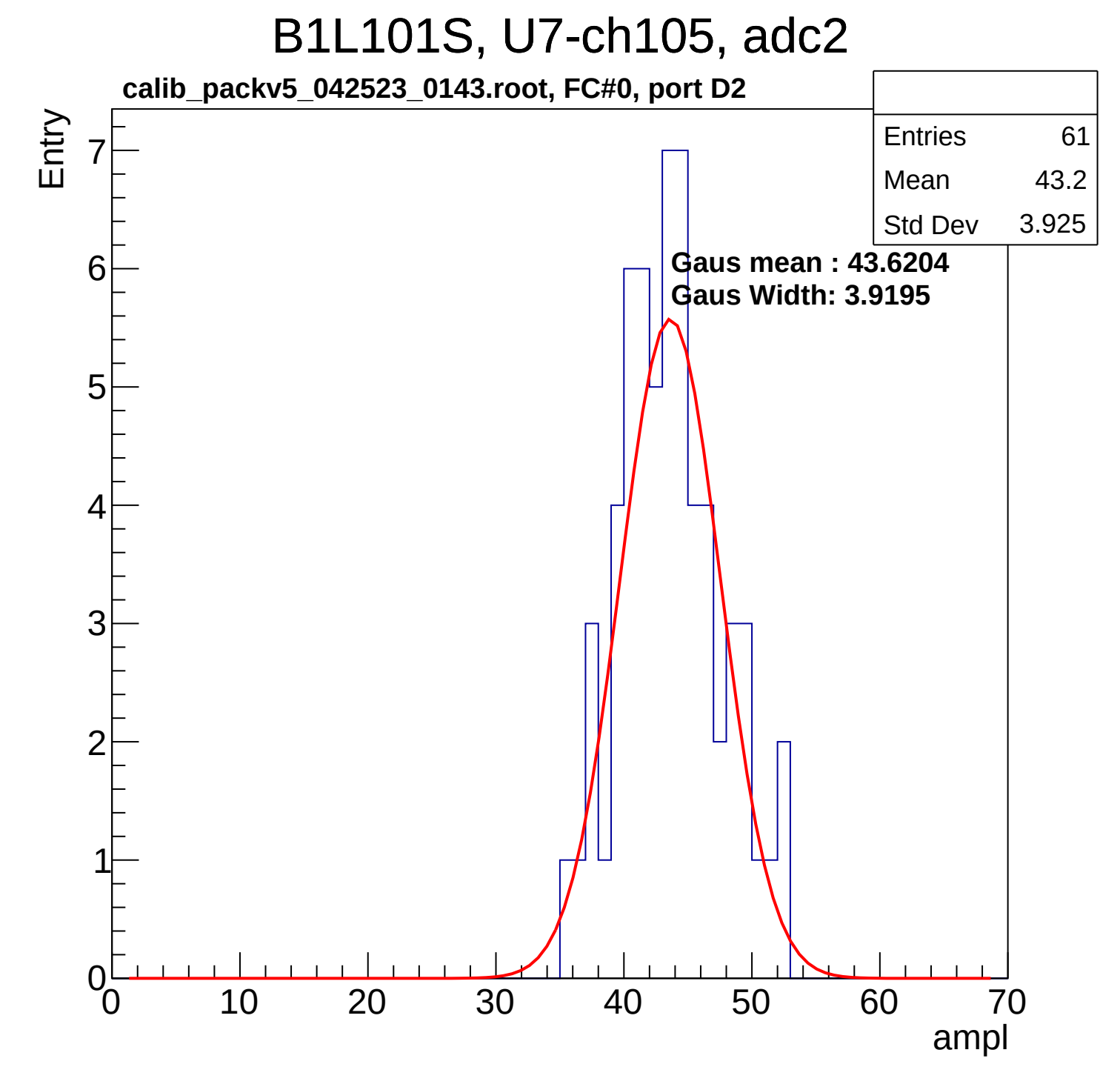
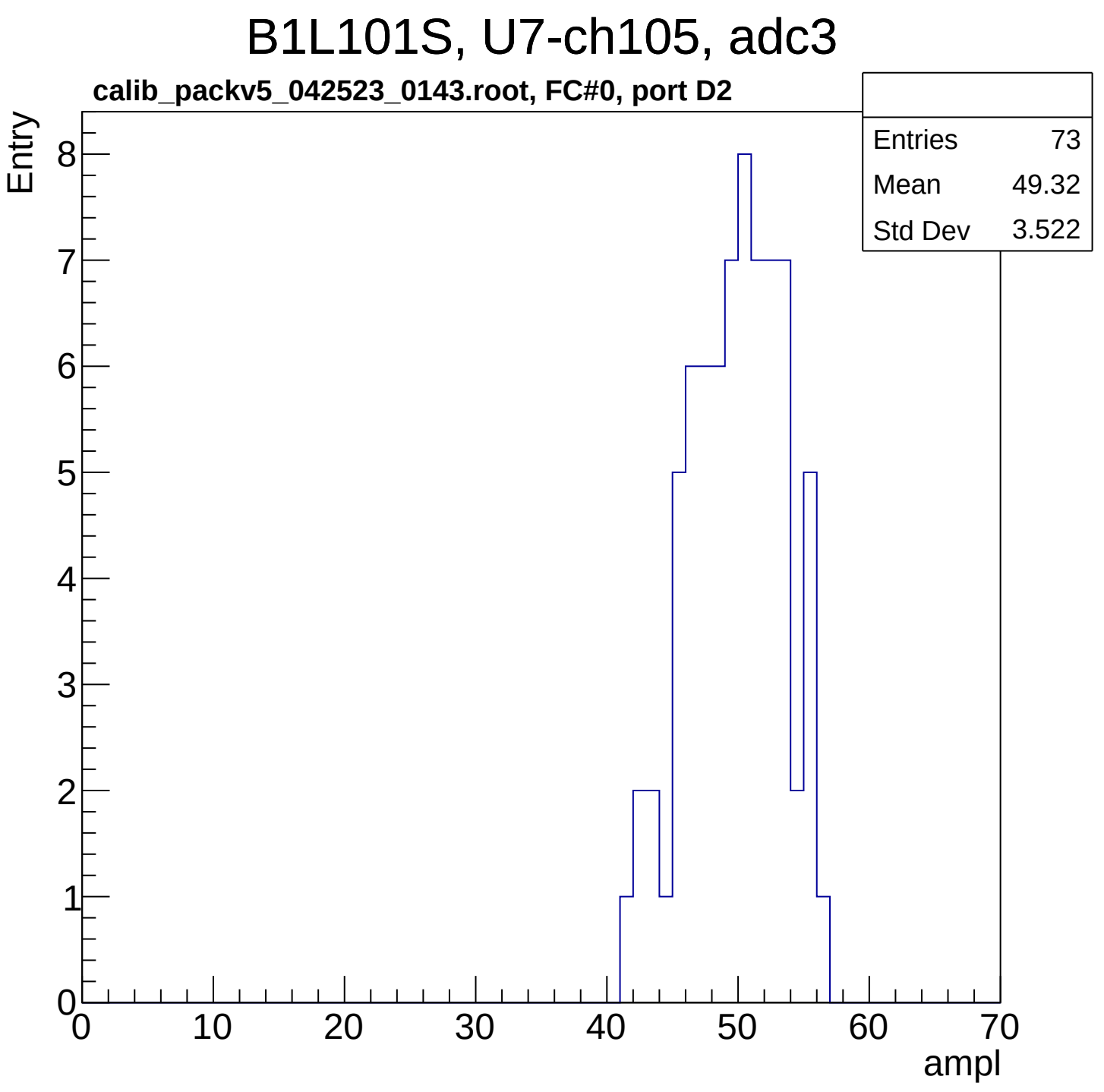
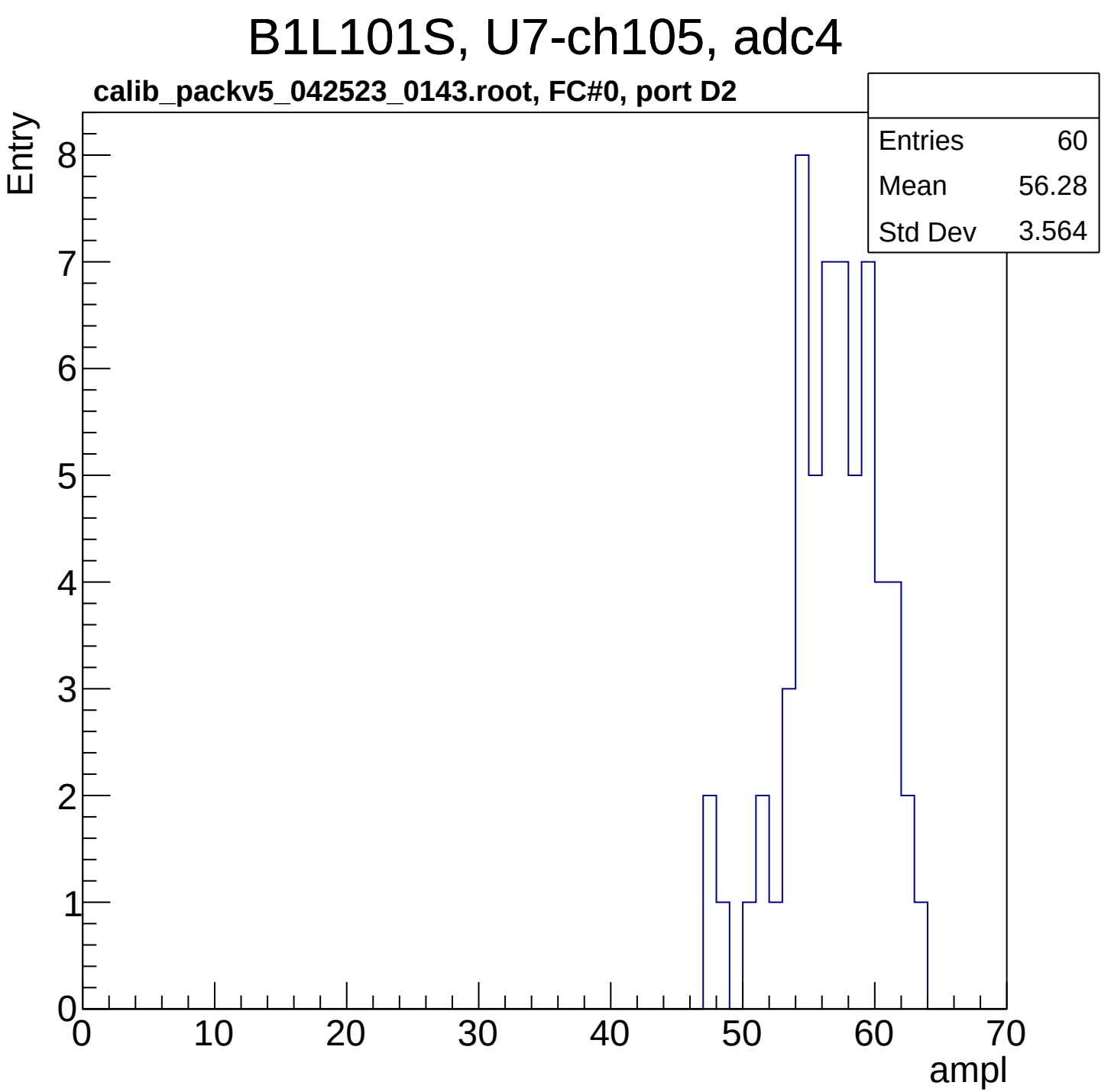

B1L101S, U7-ch104, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

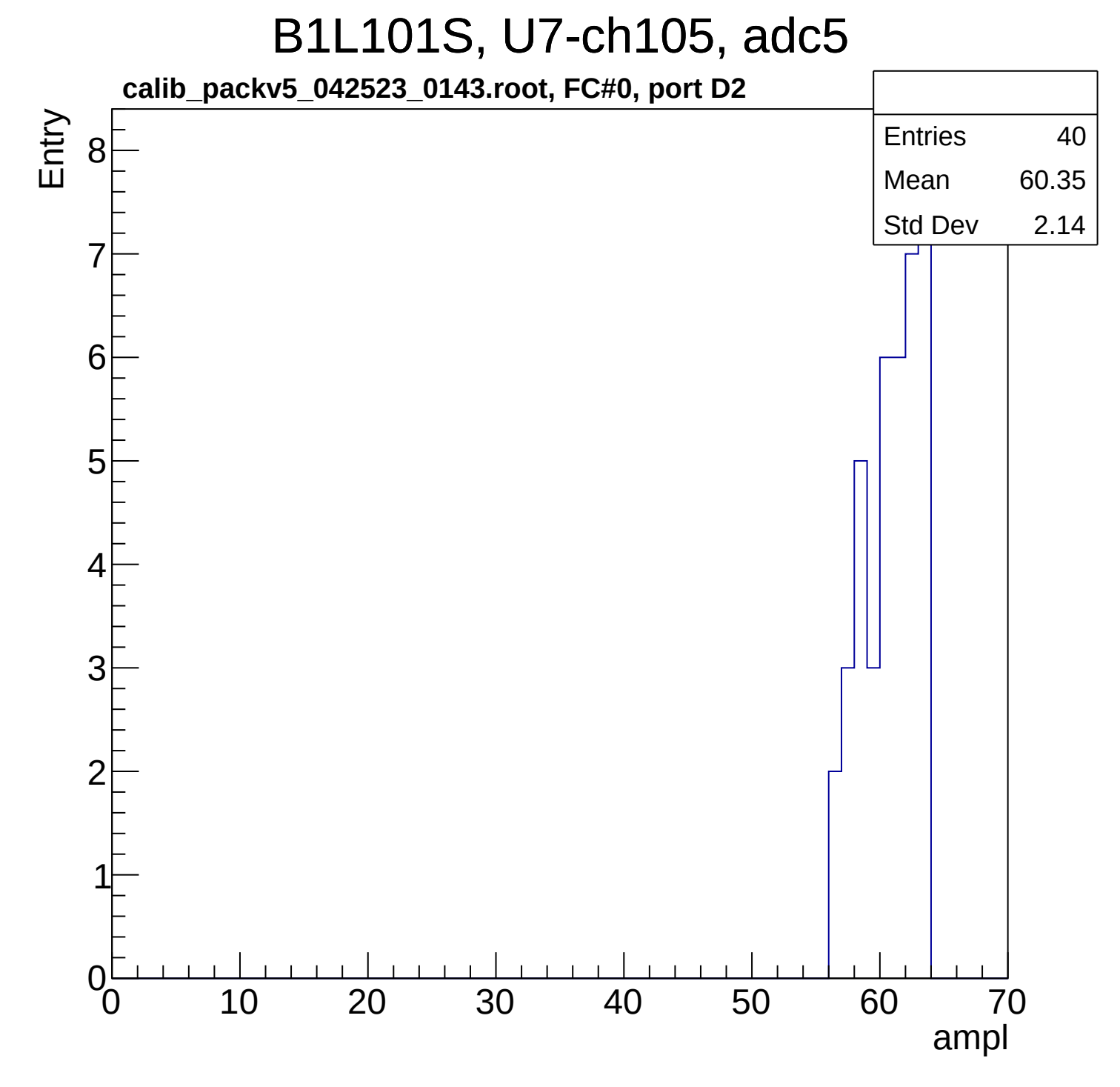

B1L101S, U7-ch105, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 29.44
Std Dev 4.792
Gaus mean : 30.4352
Gaus Width: 3.0219
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

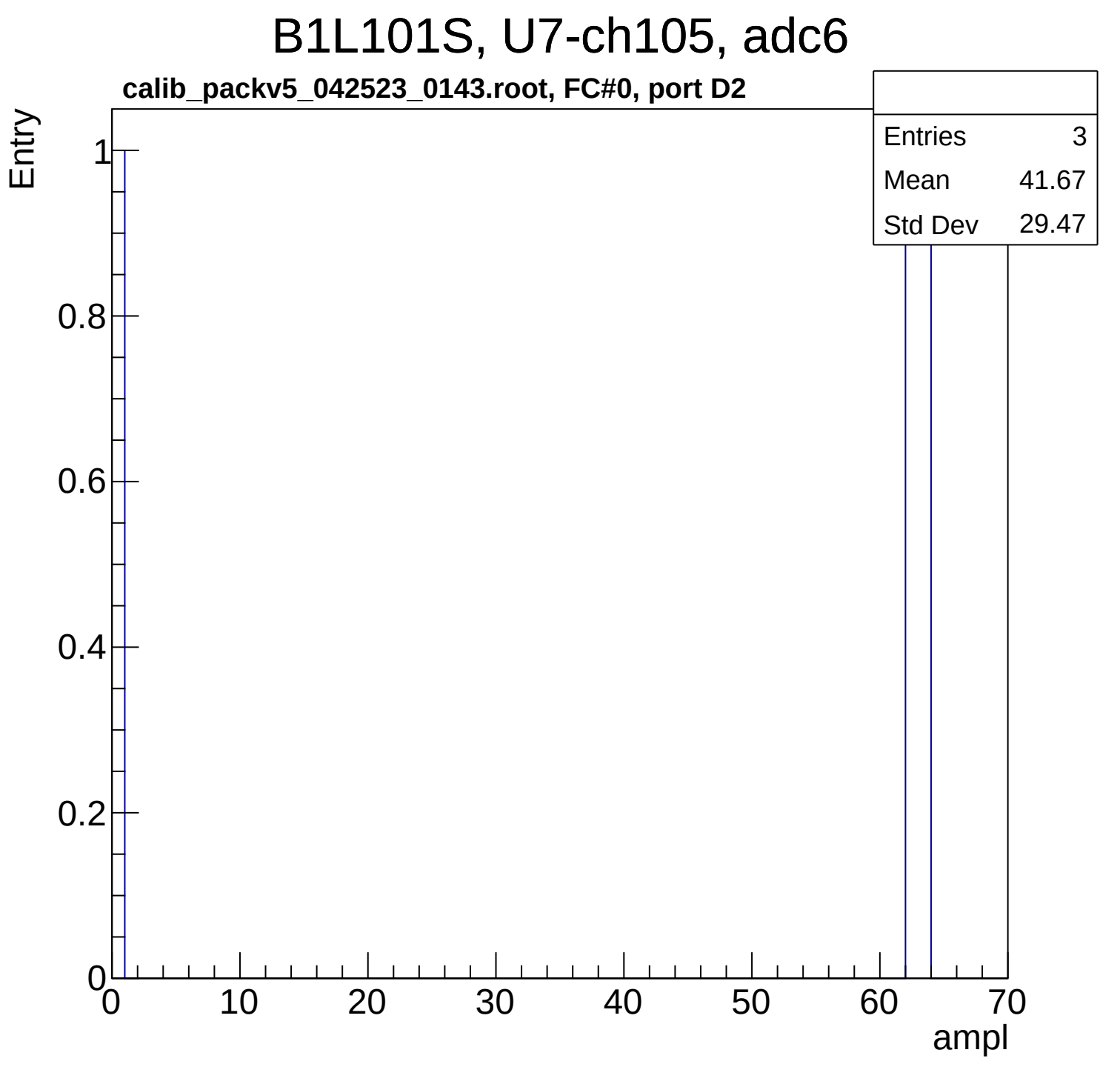

B1L101S, U7-ch105, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 37.05
Std Dev 3.3
Gaus mean : 37.2835
Gaus Width: 3.5378
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

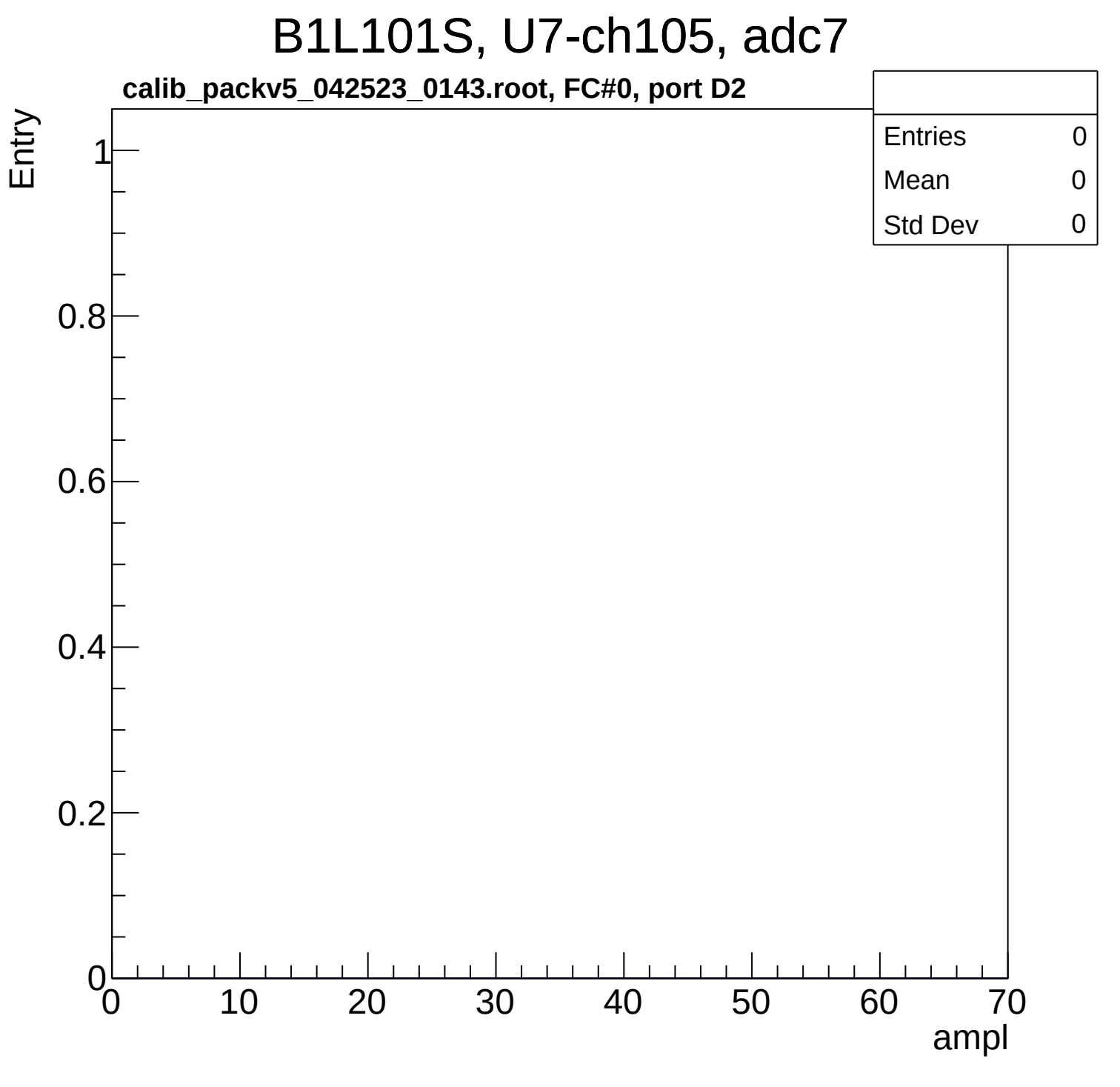

B1L101S, U7-ch105, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 43.2
Std Dev 3.925
Gaus mean : 43.6204
Gaus Width: 3.9195
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

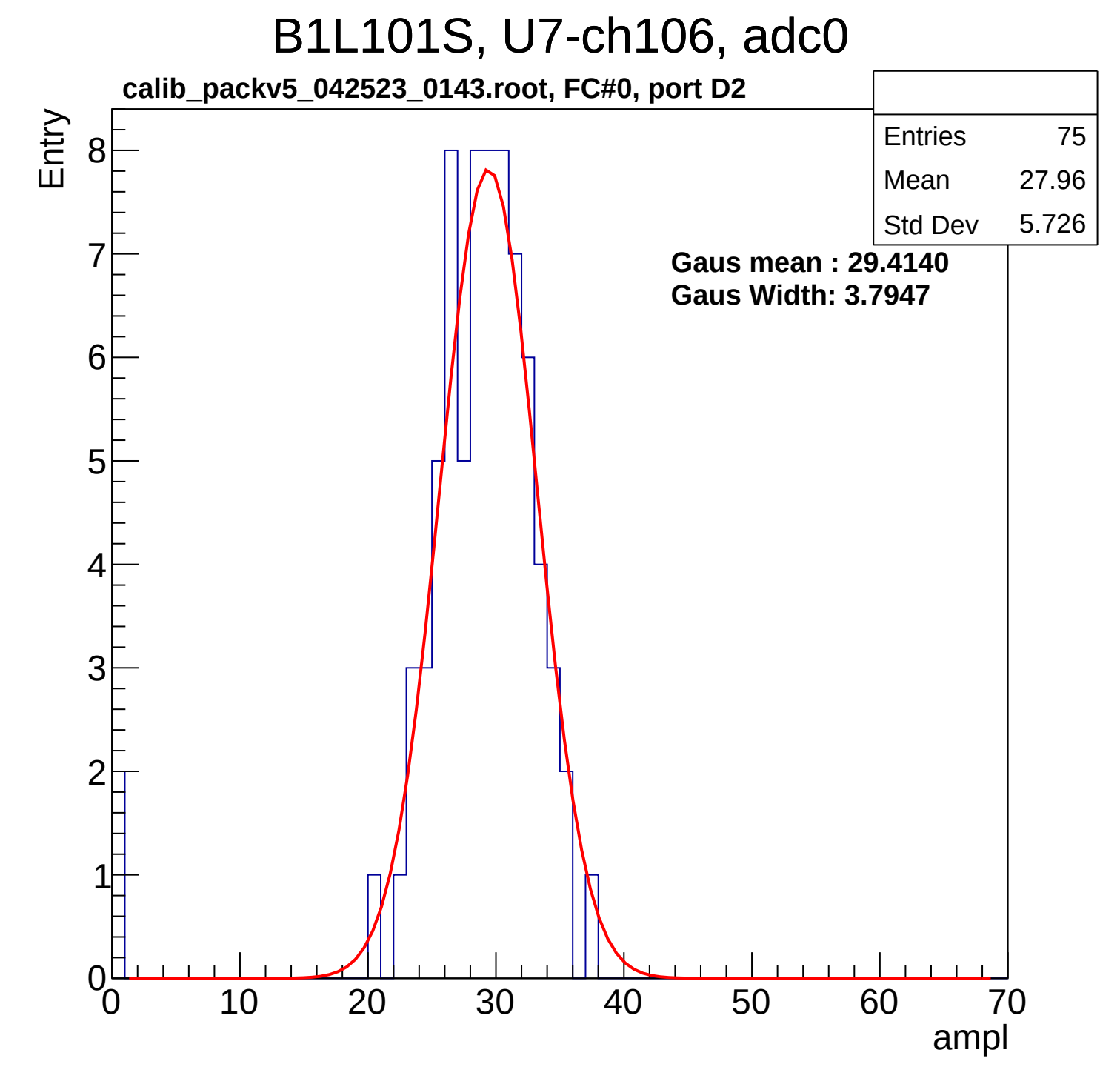

B1L101S, U7-ch105, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 49.32
Std Dev 3.522
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

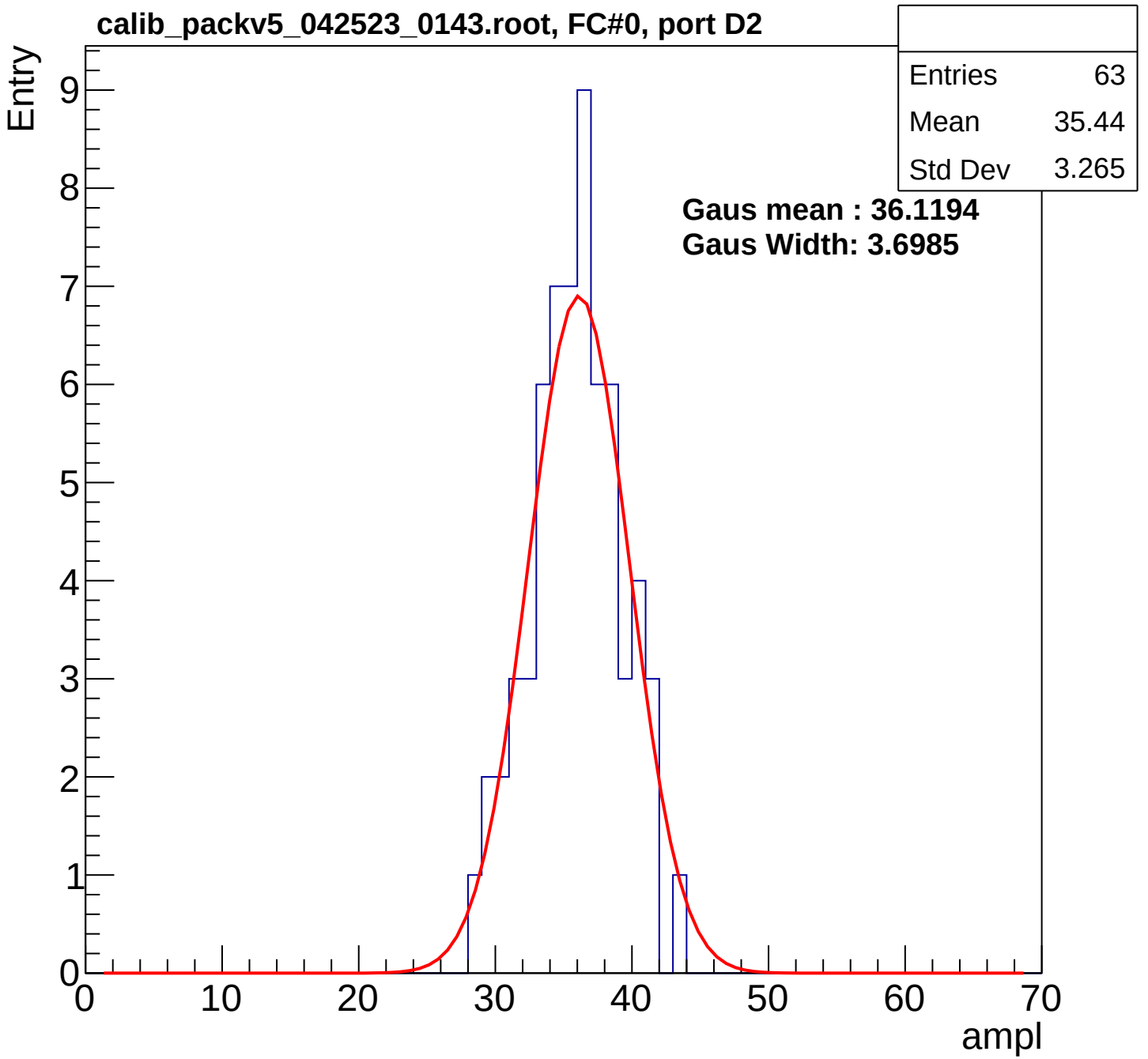

B1L101S, U7-ch105, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 56.28
Std Dev 3.564
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

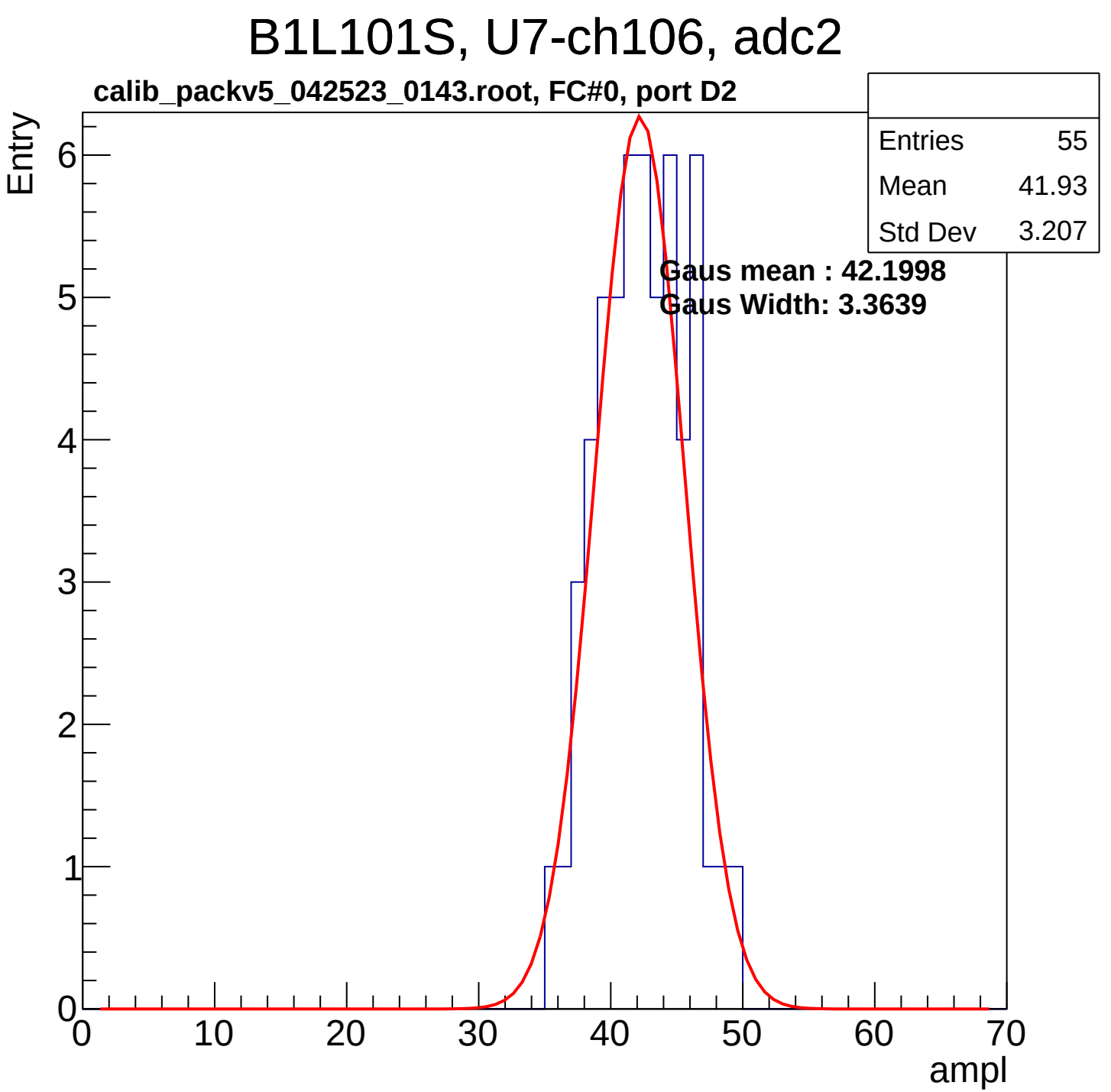

B1L101S, U7-ch105, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 40
Mean 60.35
Std Dev 2.14
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch105, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 41.67
Std Dev 29.47
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch105, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch106, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 27.96
Std Dev 5.726
Gaus mean : 29.4140
Gaus Width: 3.7947
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch106, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 35.44
Std Dev 3.265
Gaus mean : 36.1194
Gaus Width: 3.6985
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch106, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 41.93
Std Dev 3.207
Gaus mean : 42.1998
Gaus Width: 3.3639
Entry
ampl
0
1
2
3
4
5
6
0
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20
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60
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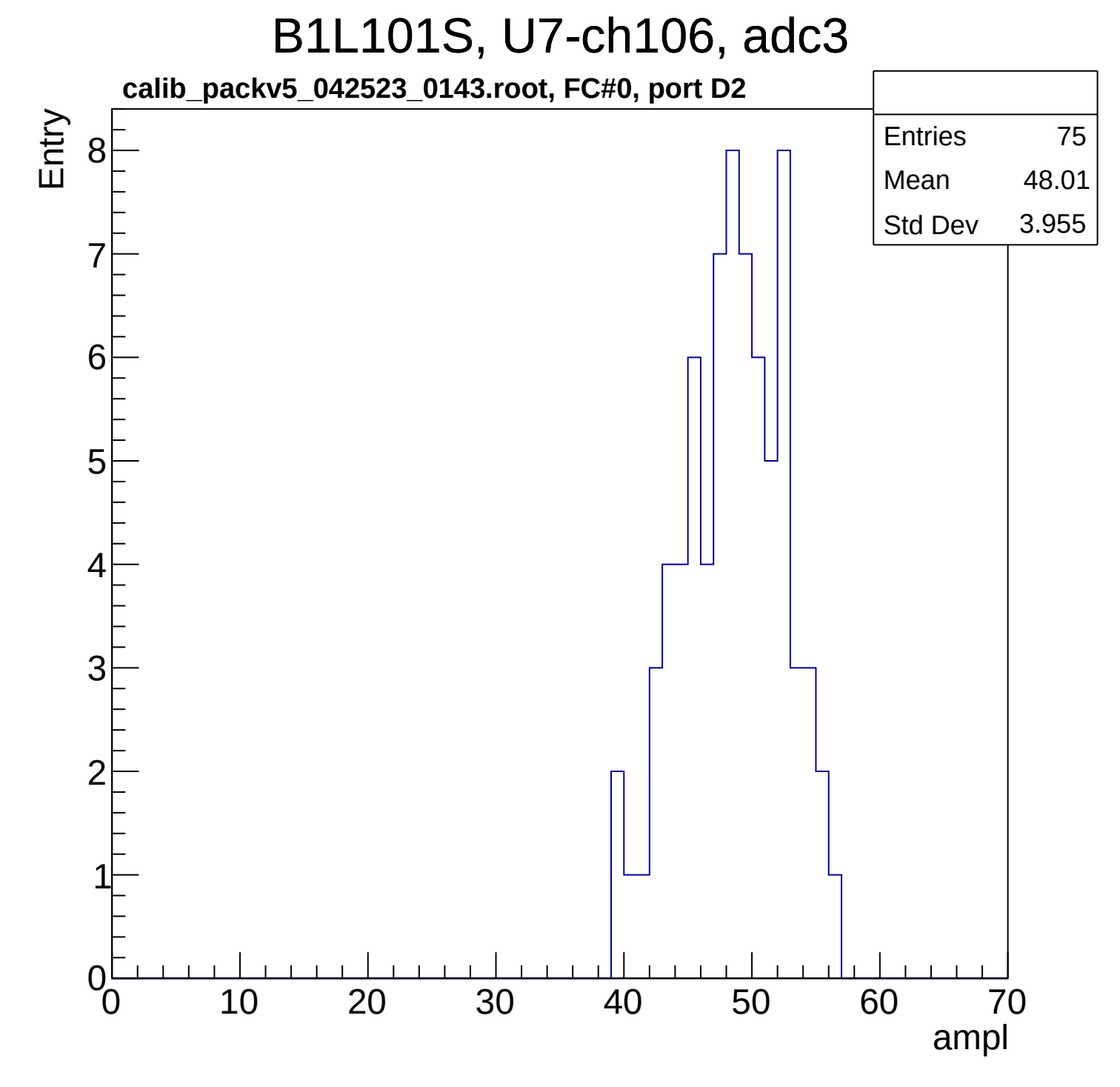
B1L101S, U7-ch106, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 48.01
Std Dev 3.955
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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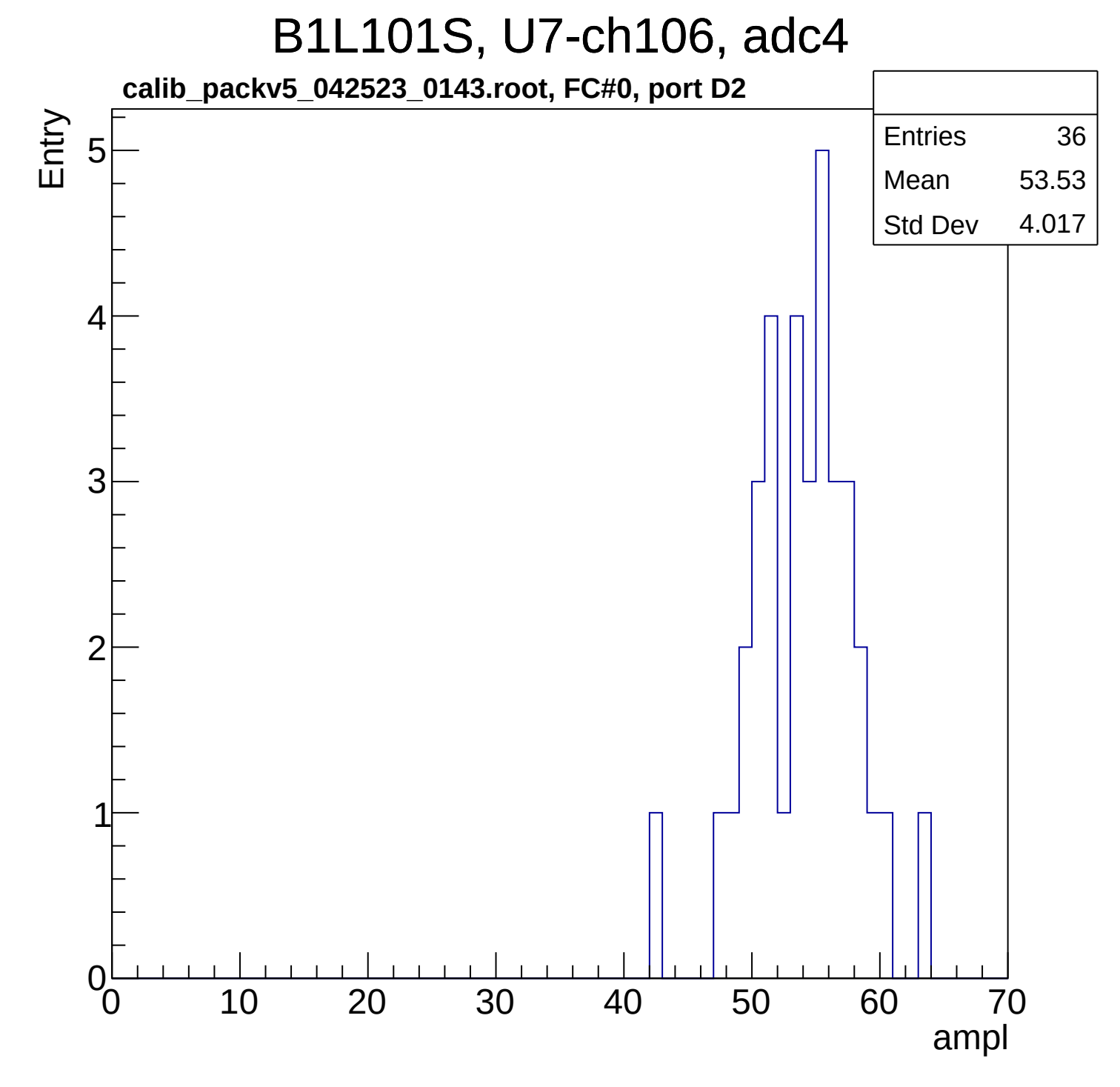
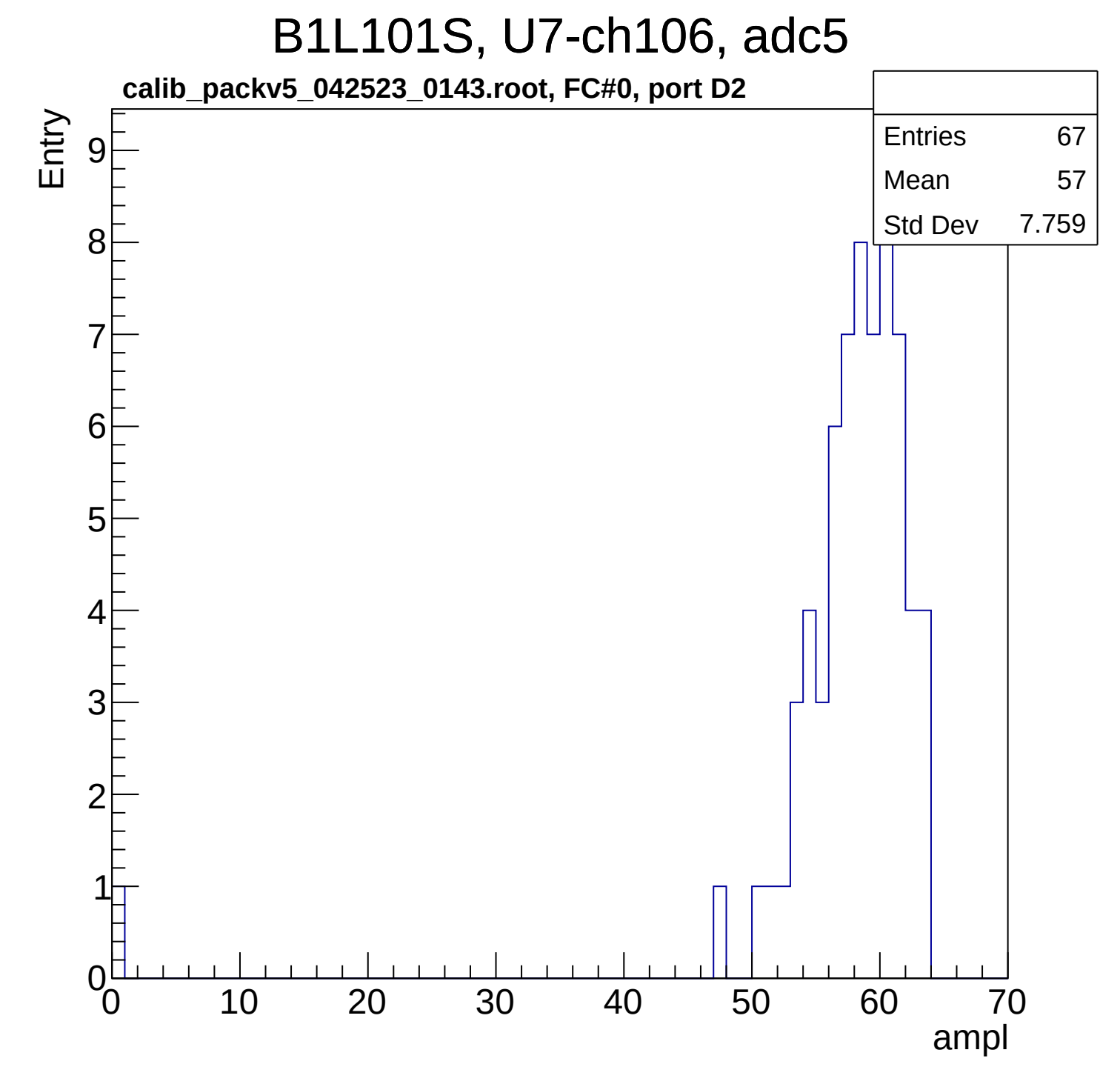
40
50
60
70


B1L101S, U7-ch106, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 36
Mean 53.53
Std Dev 4.017
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L101S, U7-ch106, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 57
Std Dev 7.759
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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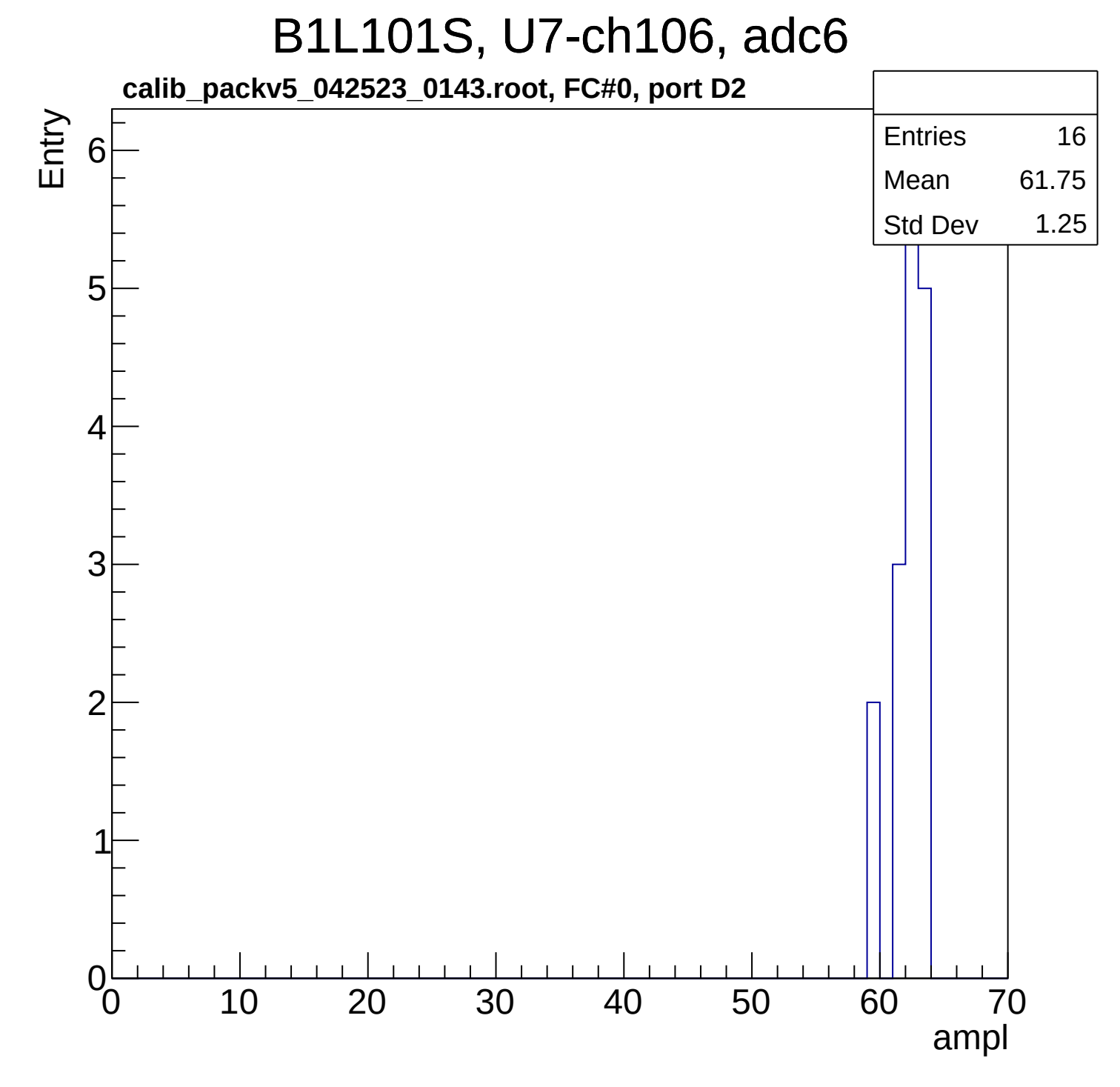
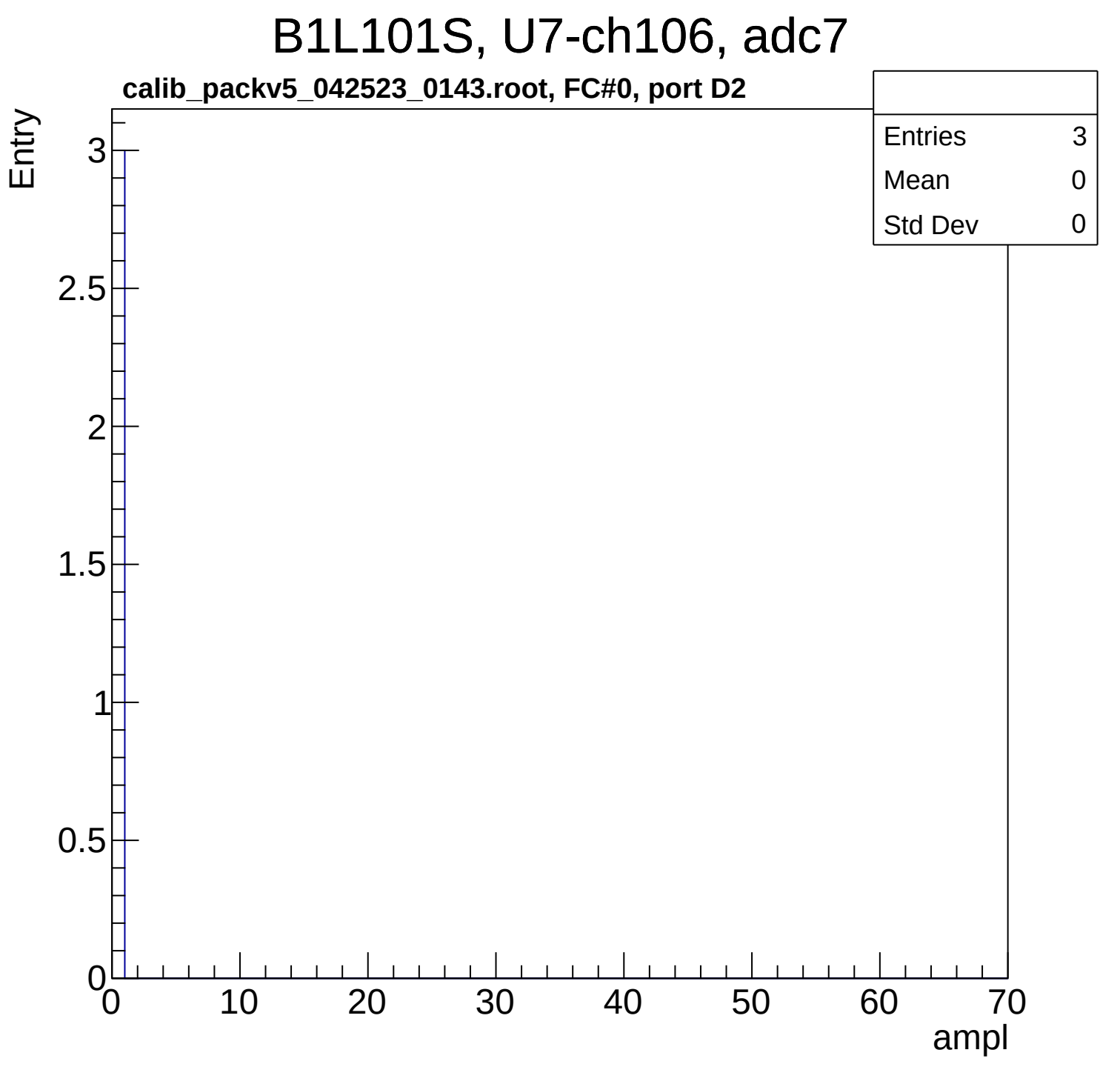

B1L101S, U7-ch106, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 16
Mean 61.75
Std Dev 1.25
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch106, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 0
Std Dev 0
Entry
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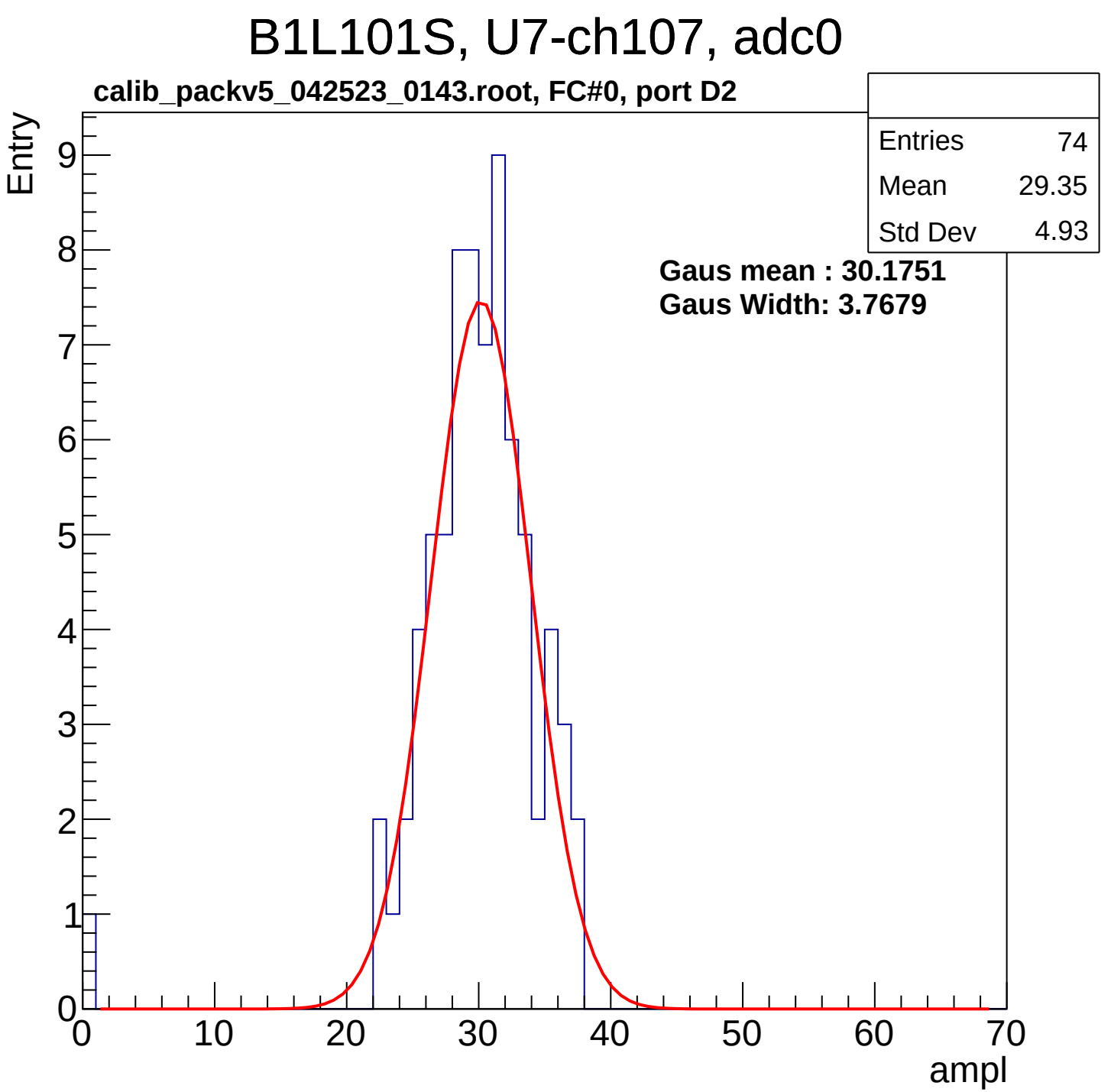
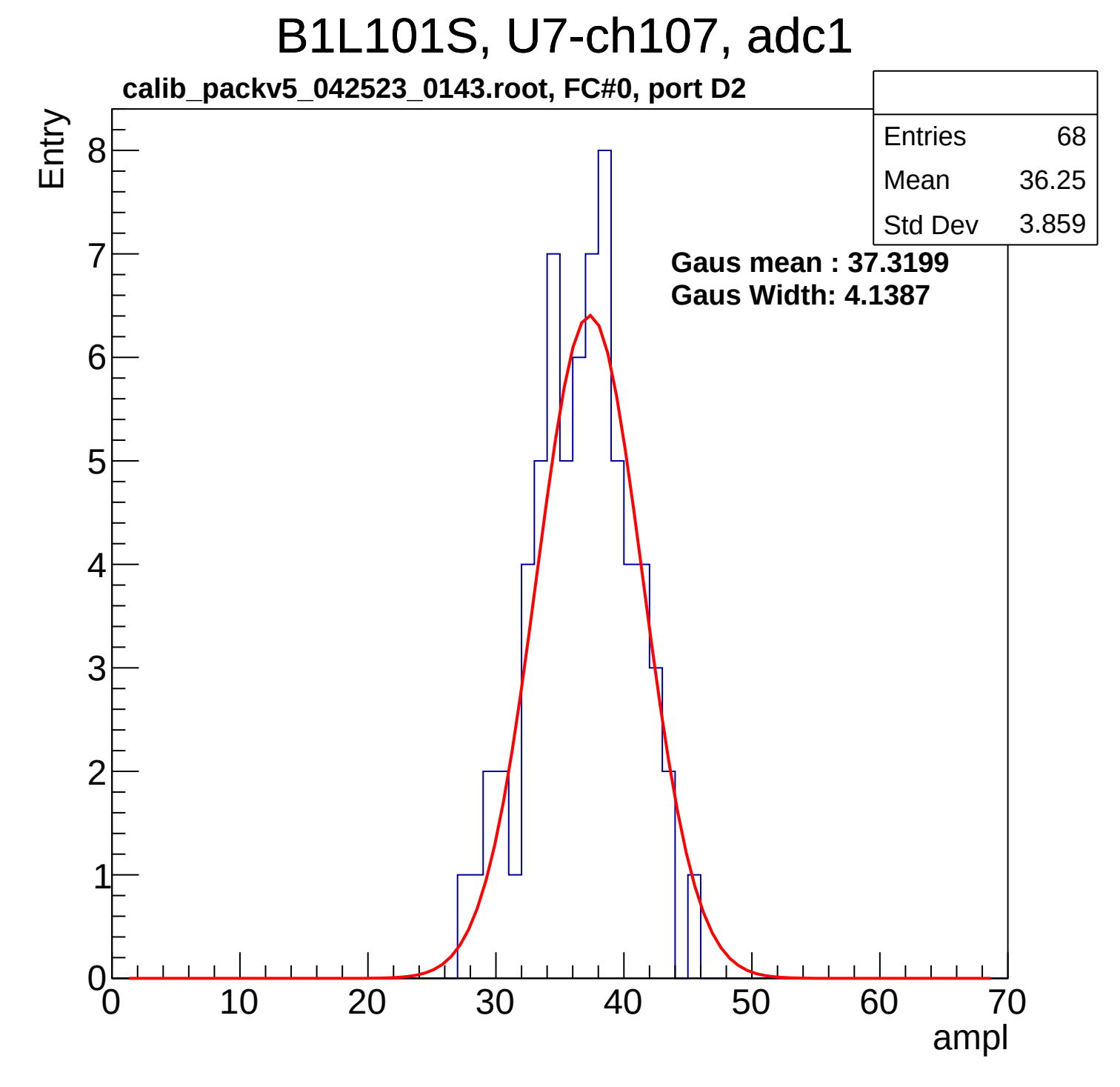
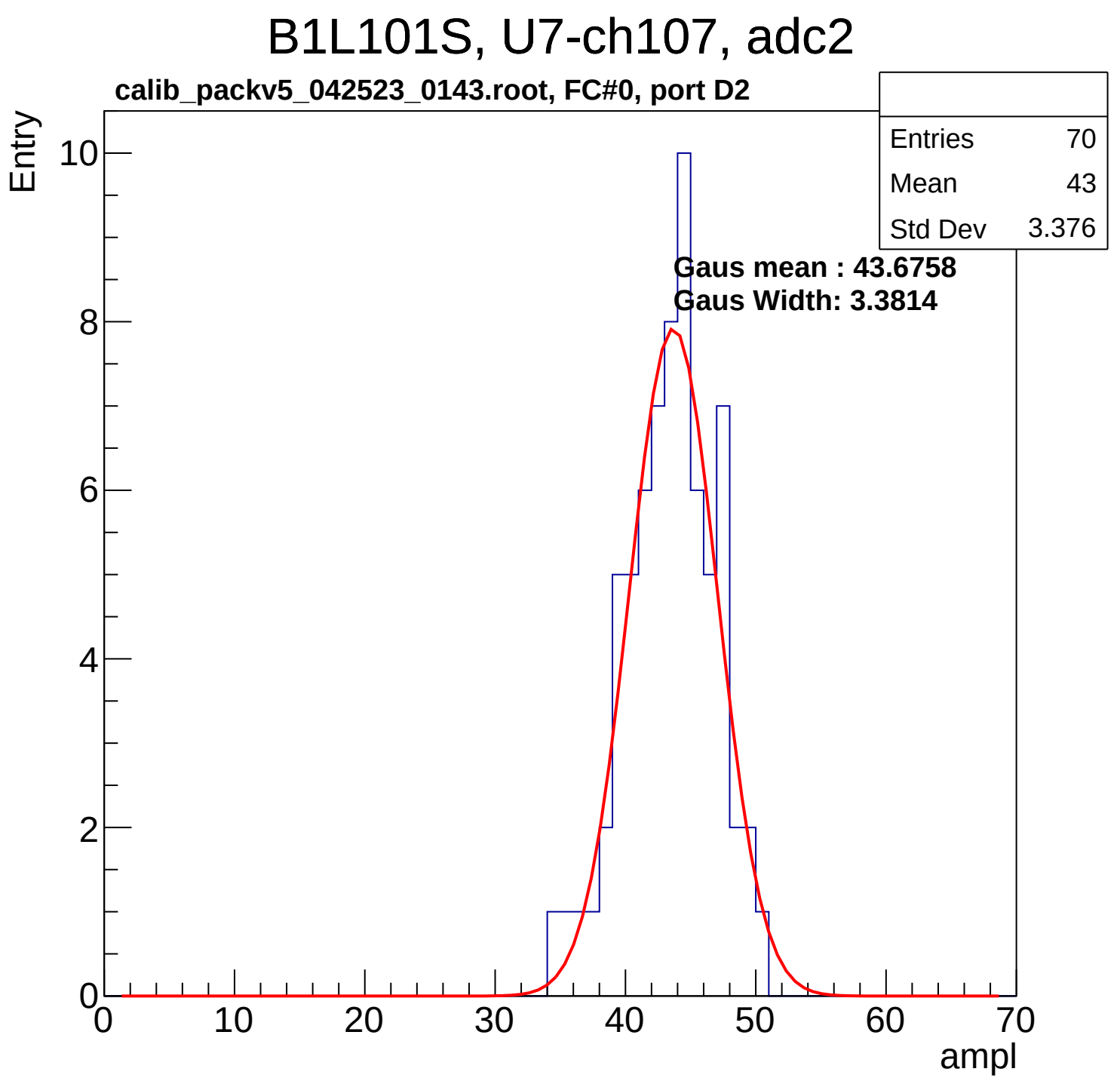
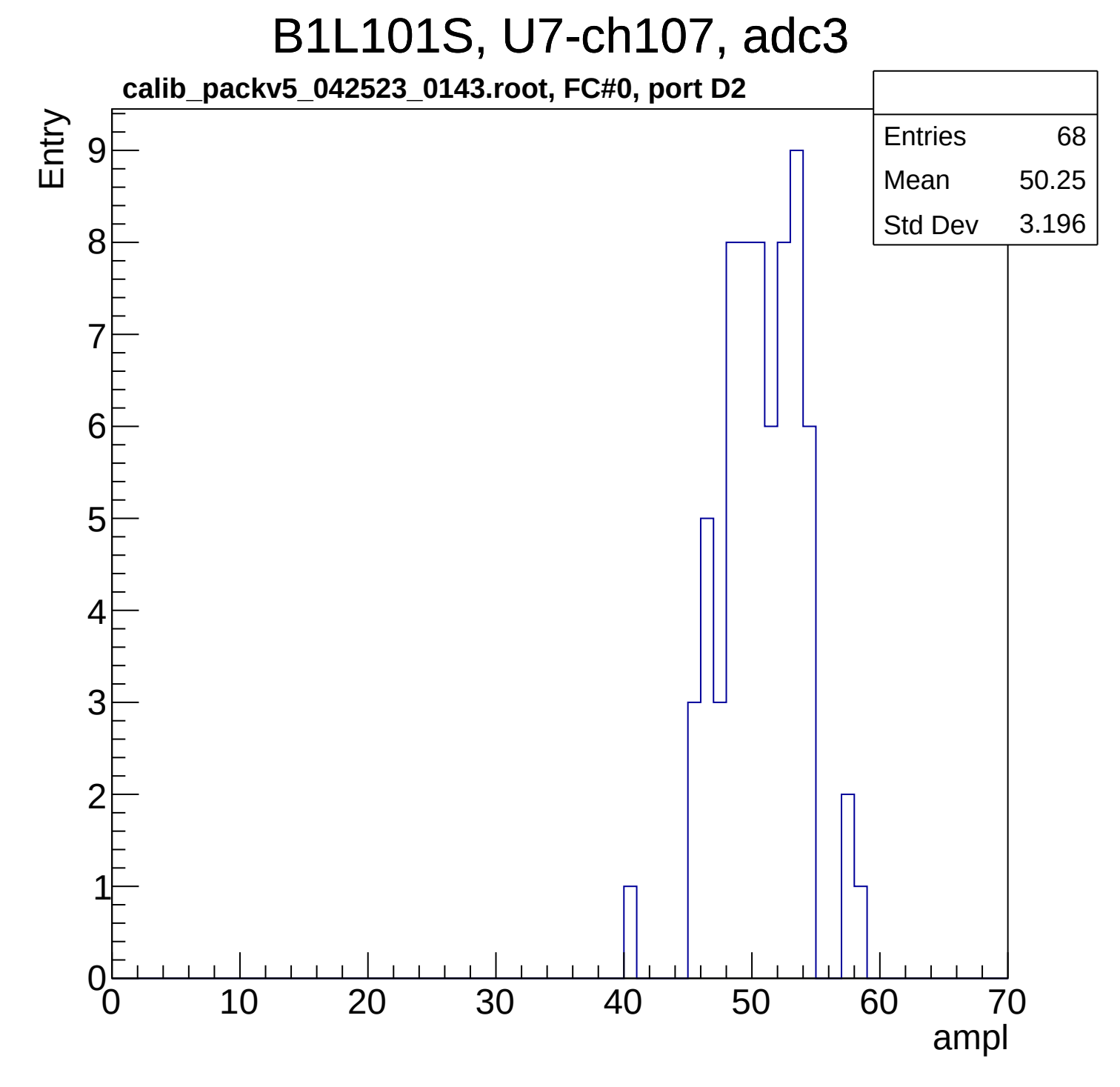
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch107, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 29.35
Std Dev 4.93
Gaus mean : 30.1751
Gaus Width: 3.7679
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch107, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 36.25
Std Dev 3.859
Gaus mean : 37.3199
Gaus Width: 4.1387
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch107, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 43
Std Dev 3.376
Gaus mean : 43.6758
Gaus Width: 3.3814
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch107, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 50.25
Std Dev 3.196
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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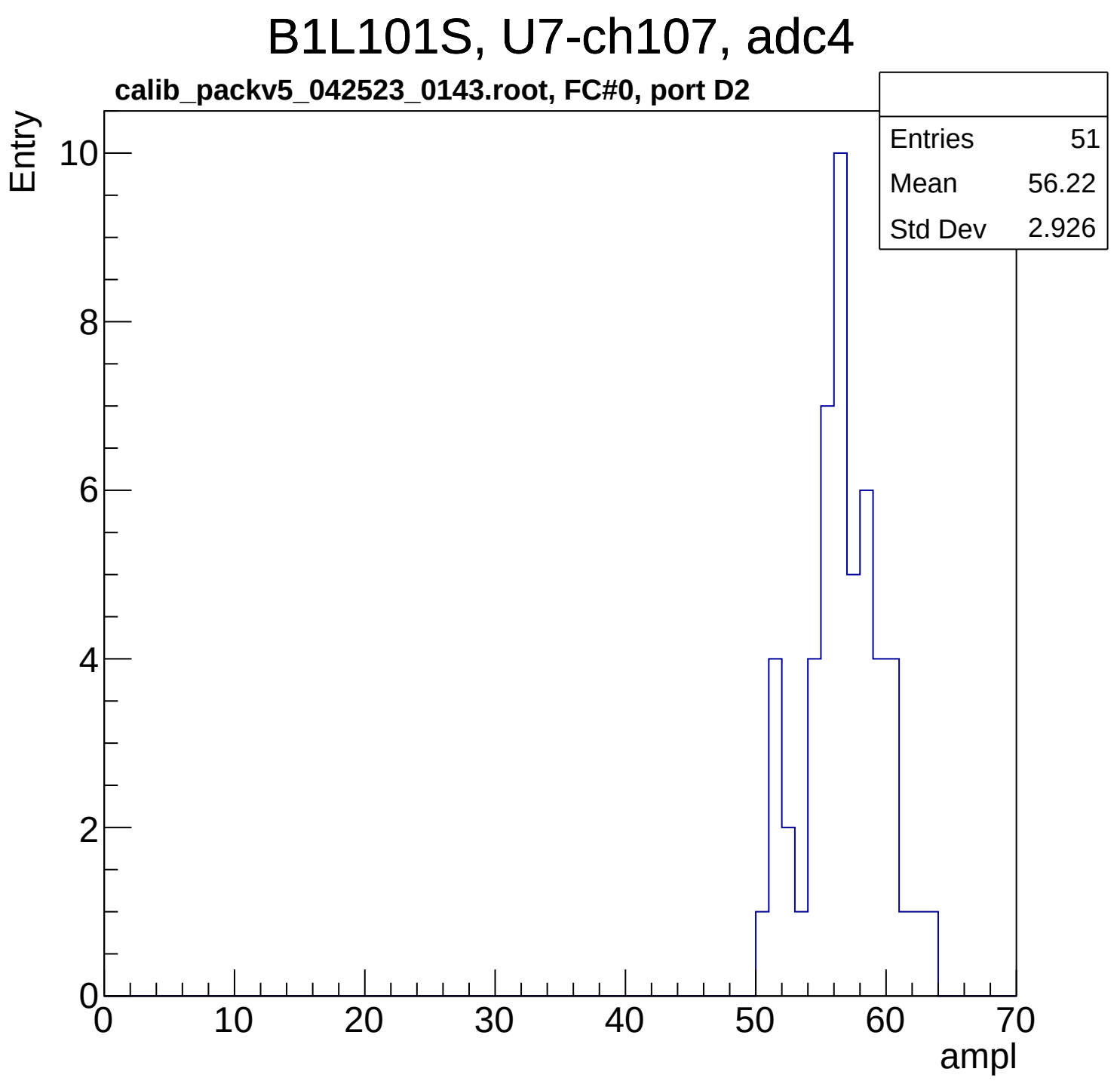
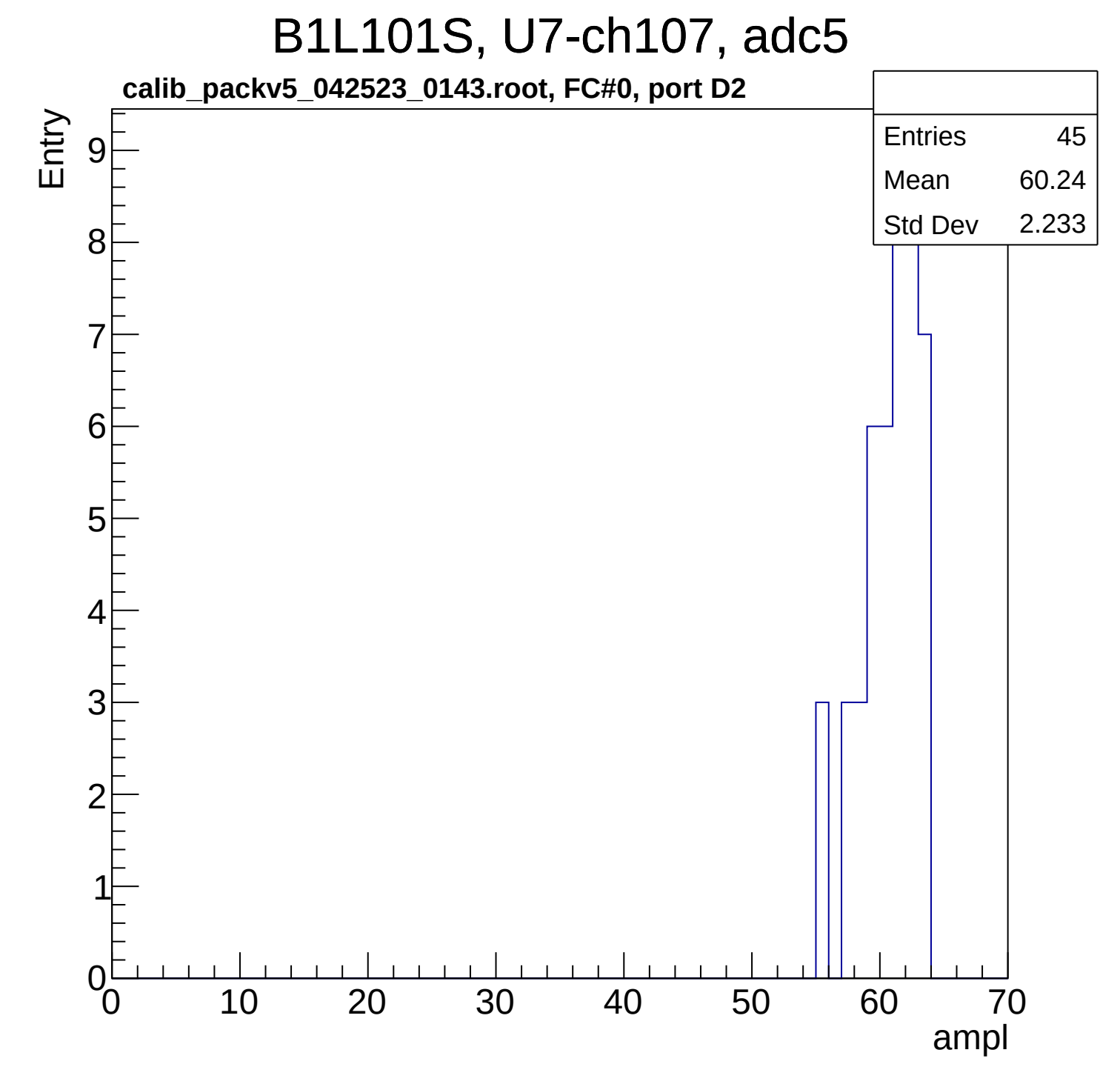

B1L101S, U7-ch107, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 56.22
Std Dev 2.926
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch107, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 60.24
Std Dev 2.233
Entry
ampl
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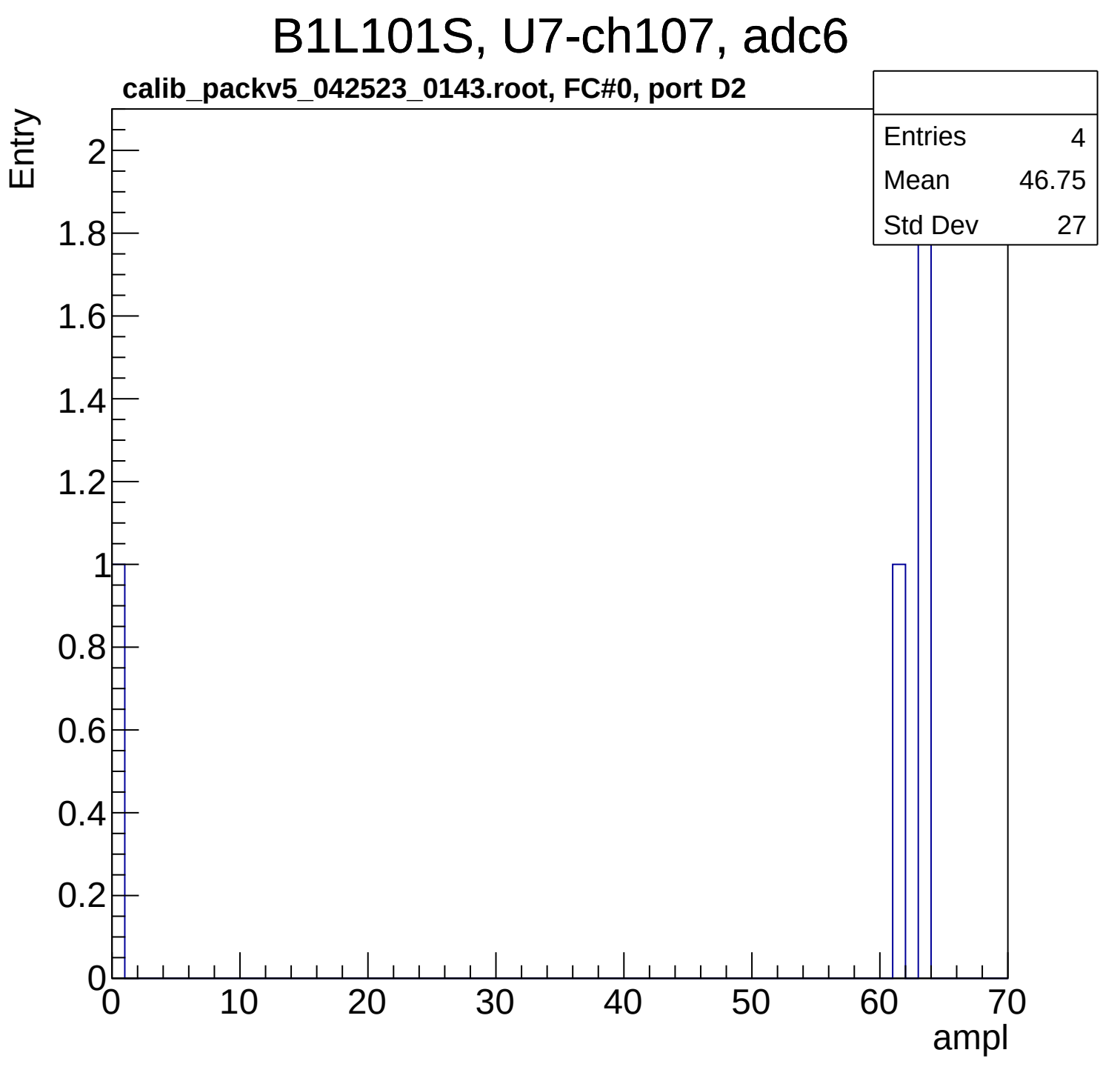
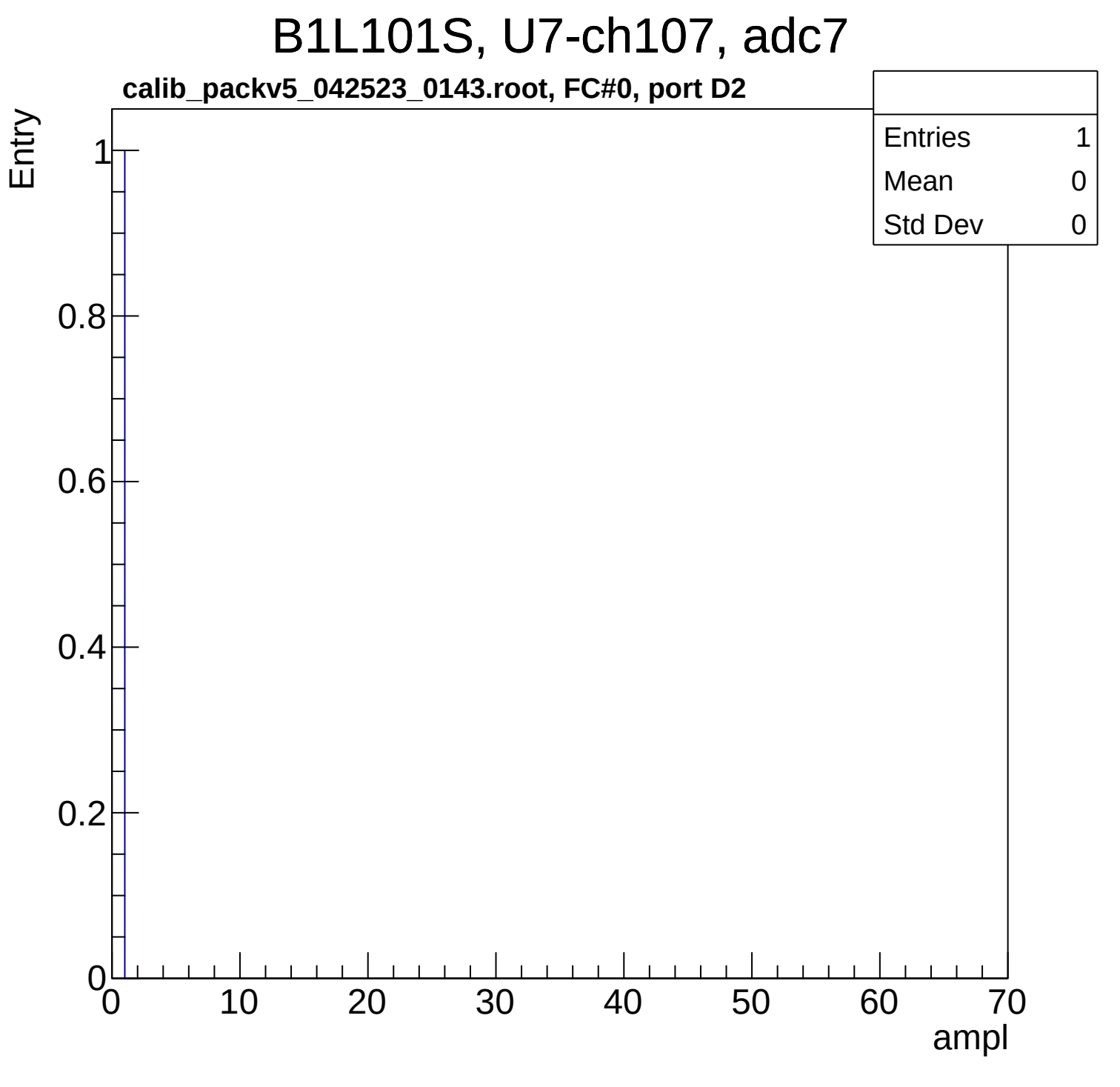
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch107, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 46.75
Std Dev 27
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U7-ch107, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
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0.6
0.4
0.2
0
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10
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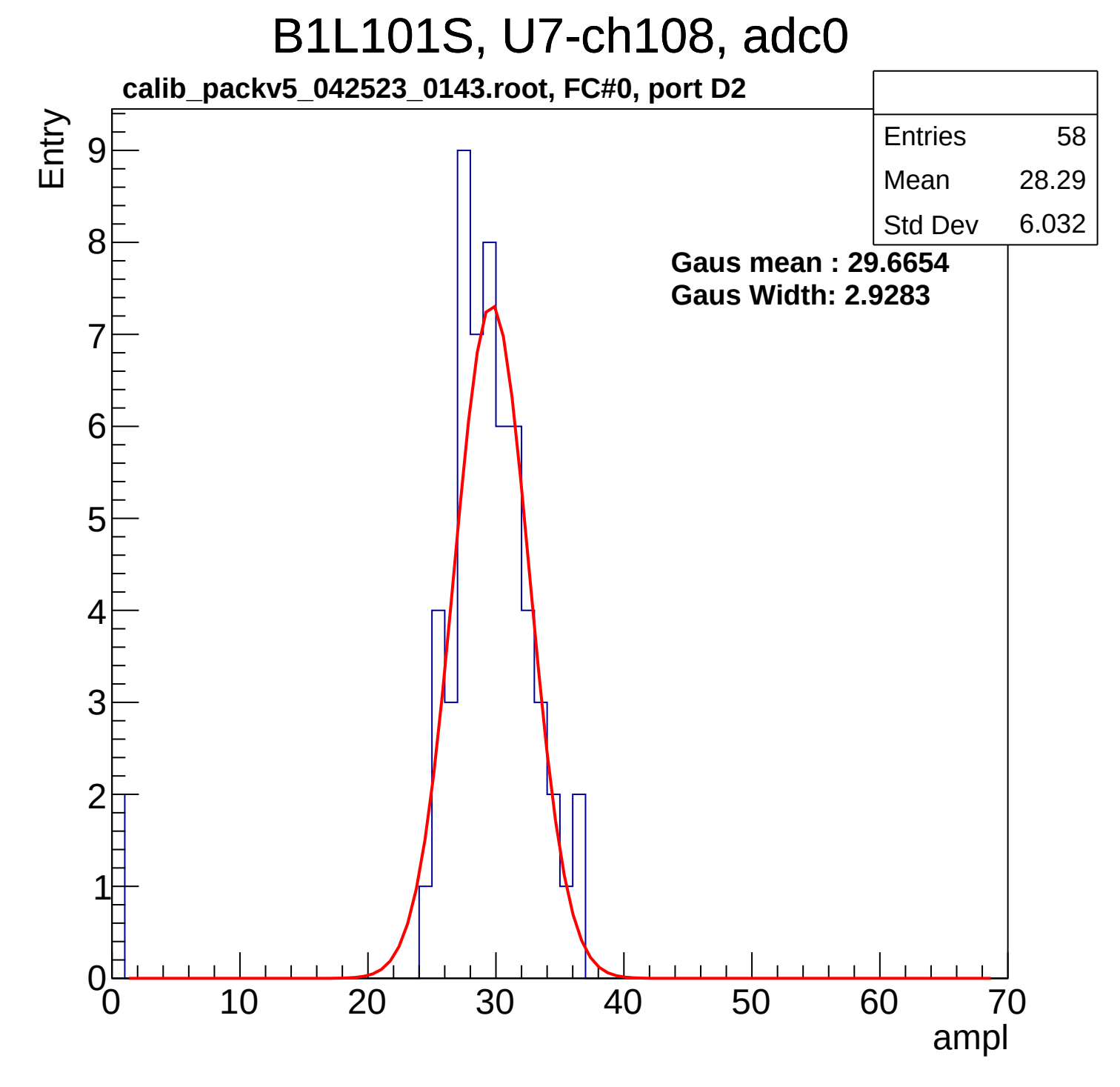
50
60
70
ampl


B1L101S, U7-ch108, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 28.29
Std Dev 6.032
Gaus mean : 29.6654
Gaus Width: 2.9283
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
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40
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60
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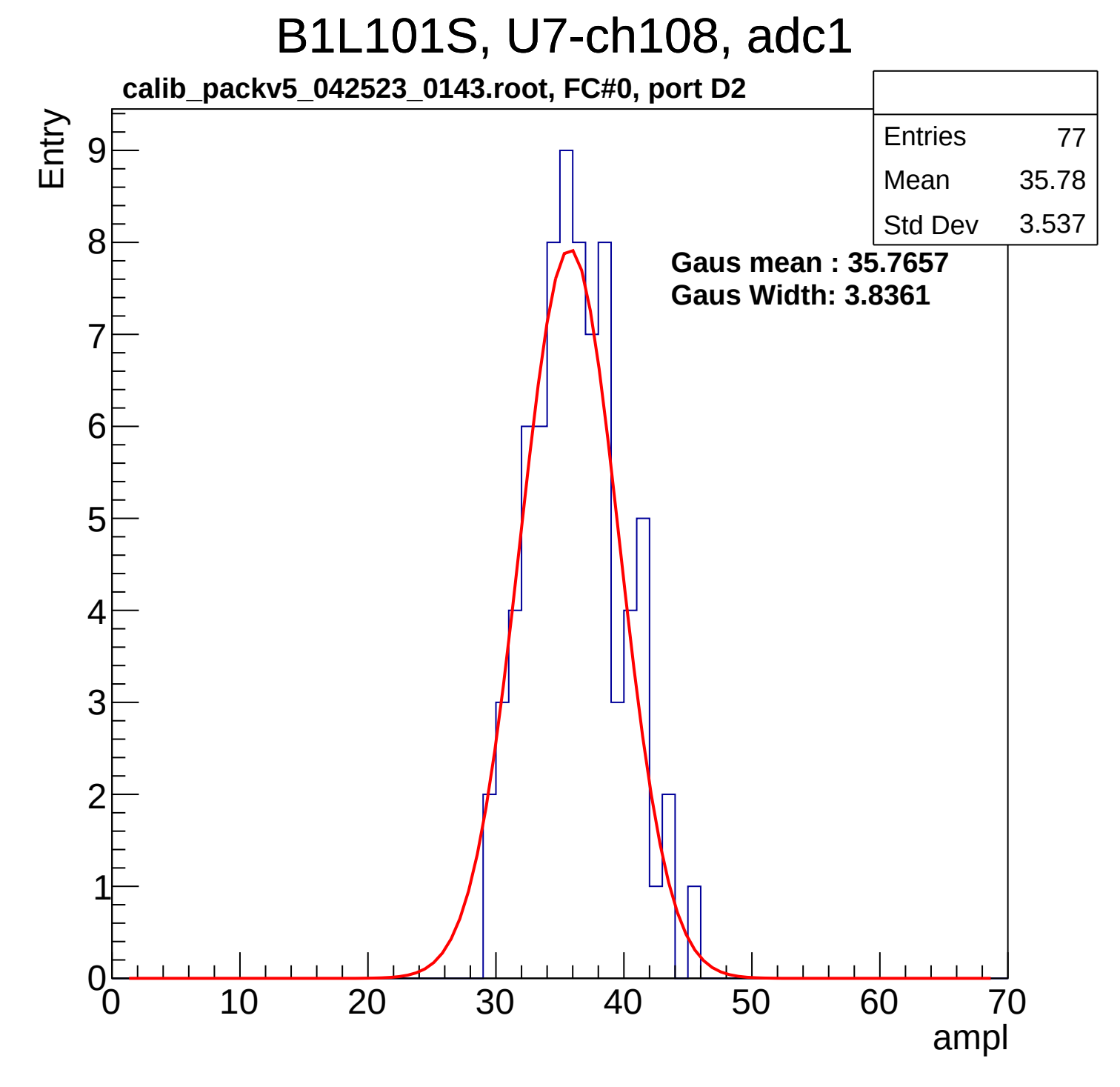
B1L101S, U7-ch108, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 35.78
Std Dev 3.537
Gaus mean : 35.7657
Gaus Width: 3.8361
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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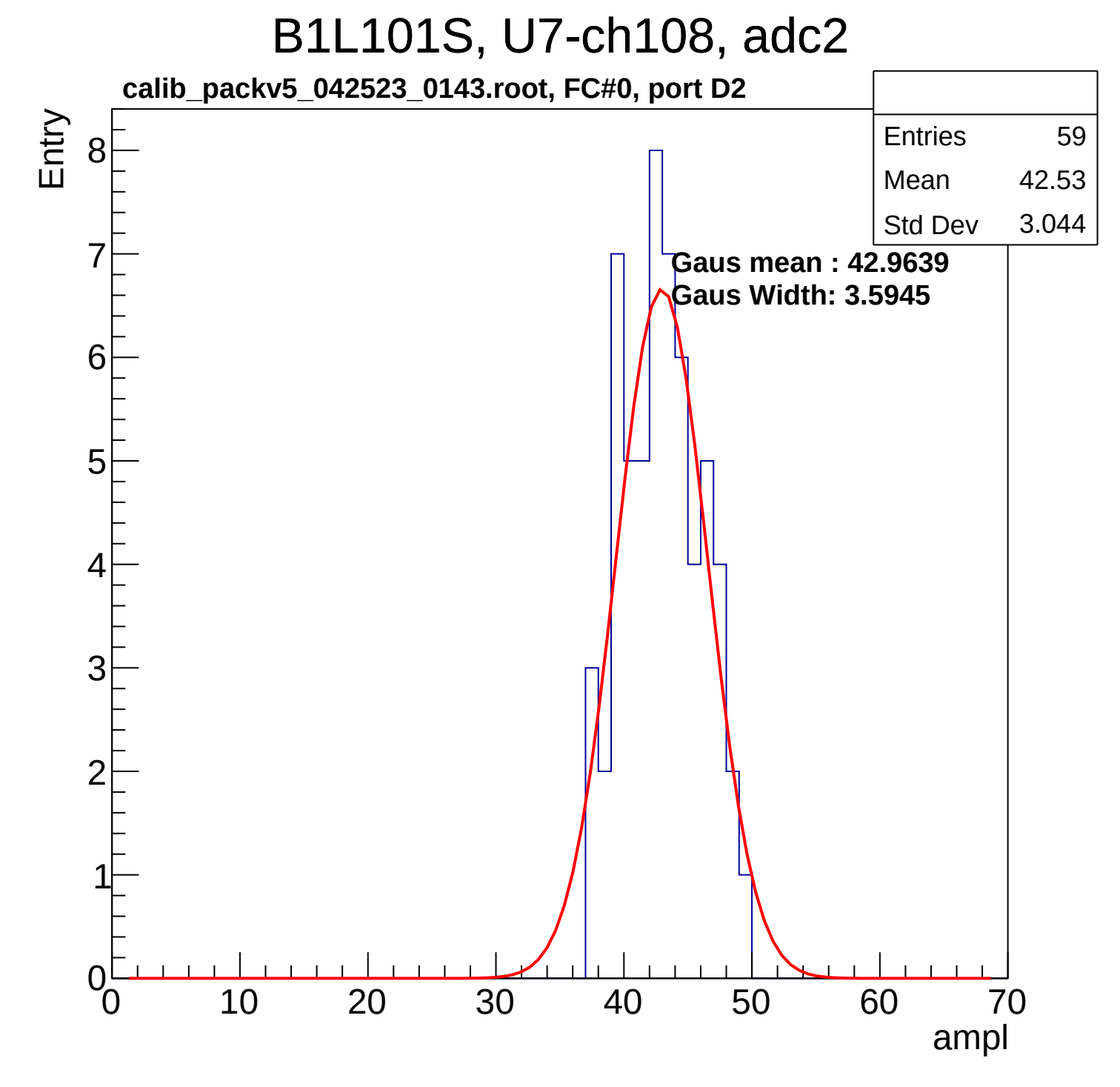
B1L101S, U7-ch108, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 42.53
Std Dev 3.044
Gaus mean : 42.9639
Gaus Width: 3.5945
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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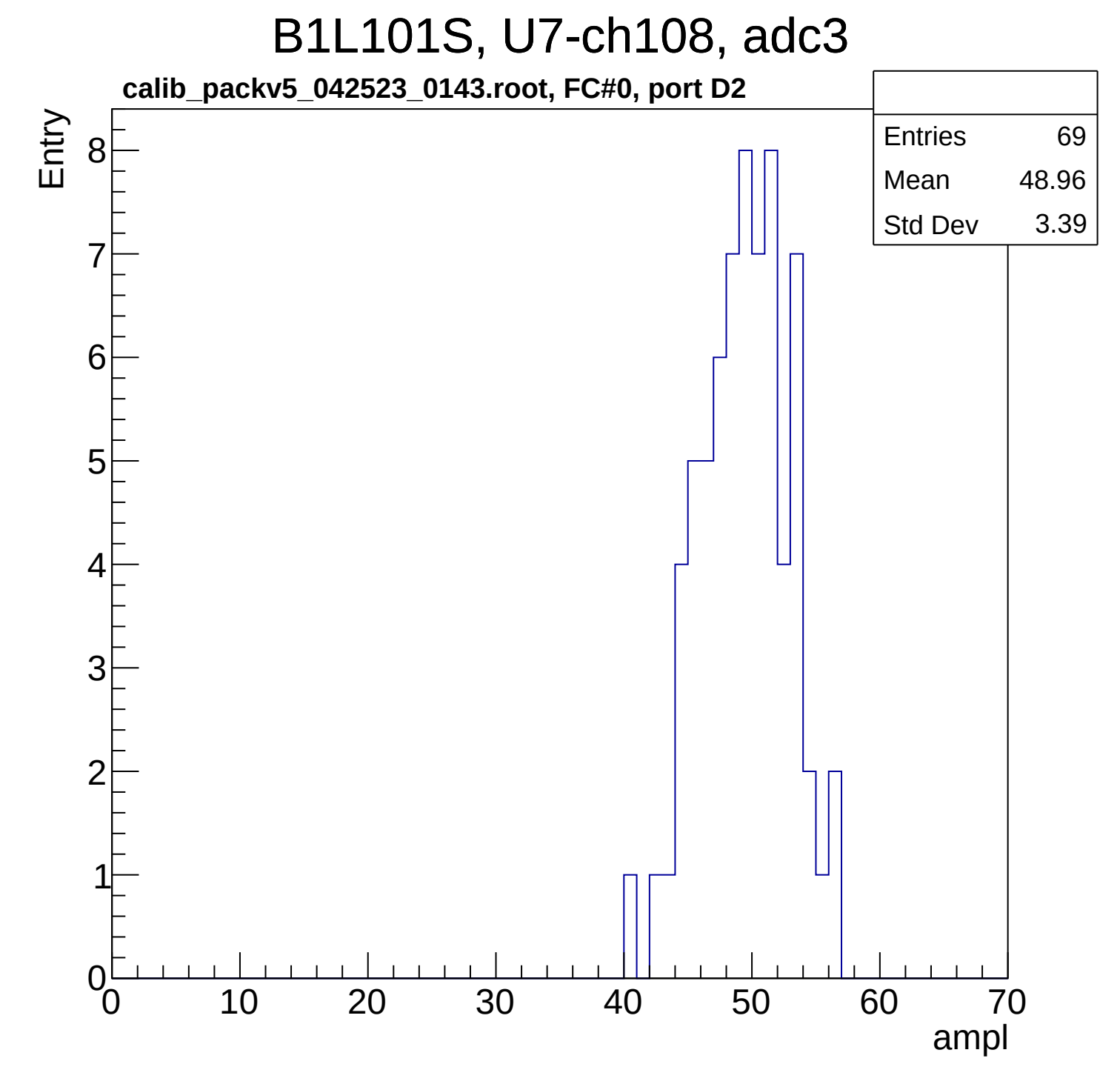
B1L101S, U7-ch108, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 48.96
Std Dev 3.39
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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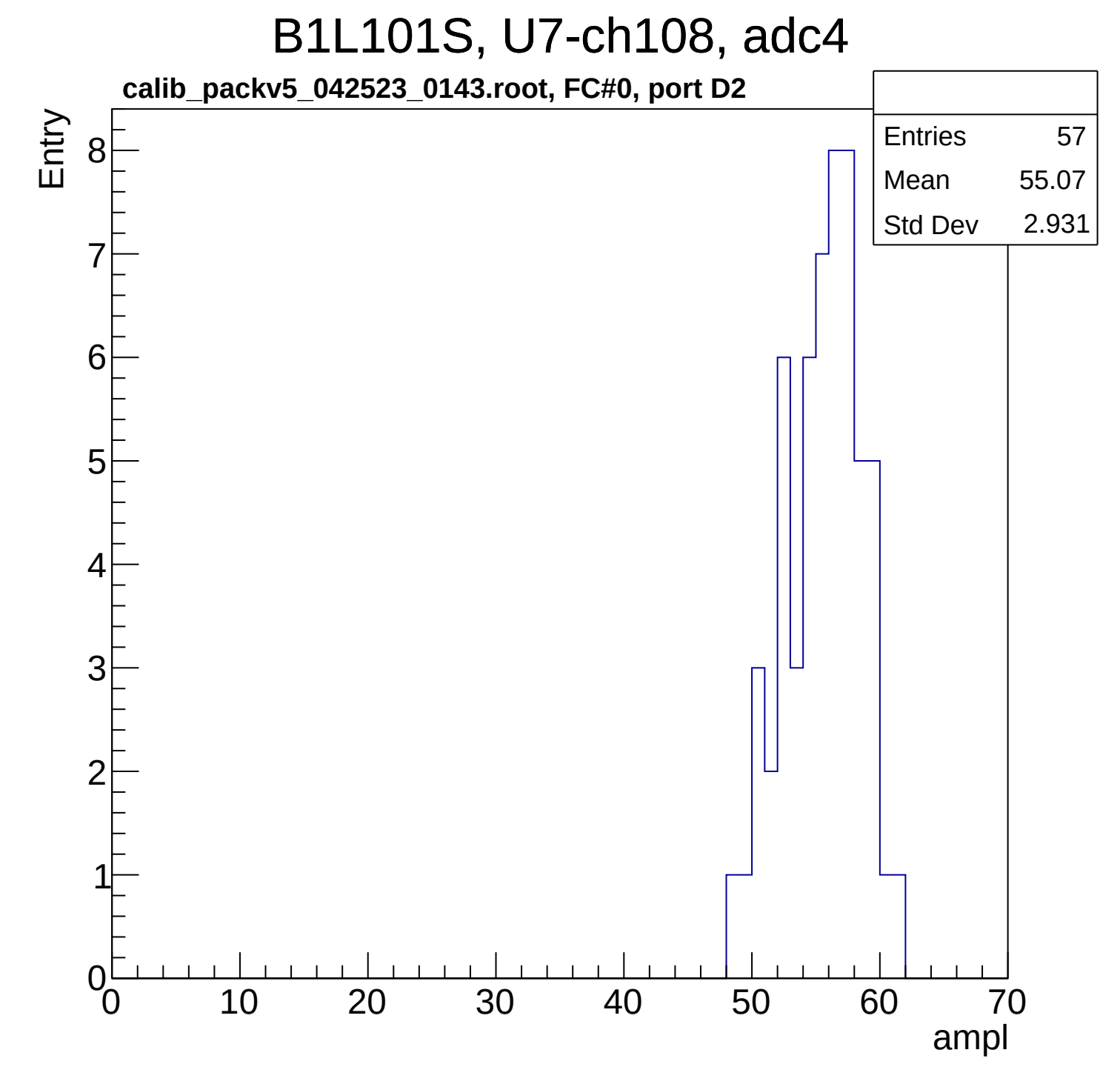
B1L101S, U7-ch108, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 55.07
Std Dev 2.931
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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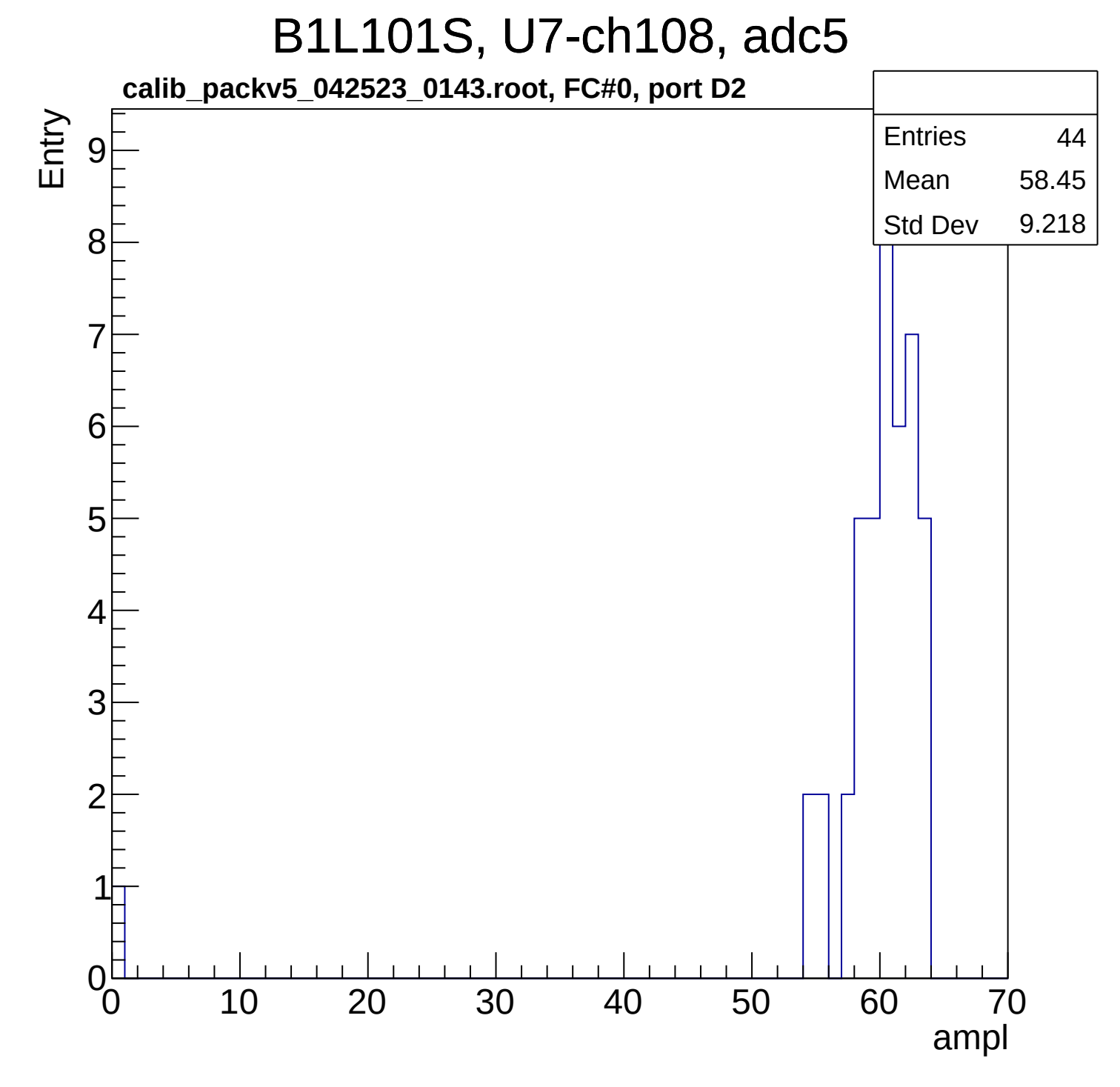
B1L101S, U7-ch108, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 44
Mean 58.45
Std Dev 9.218
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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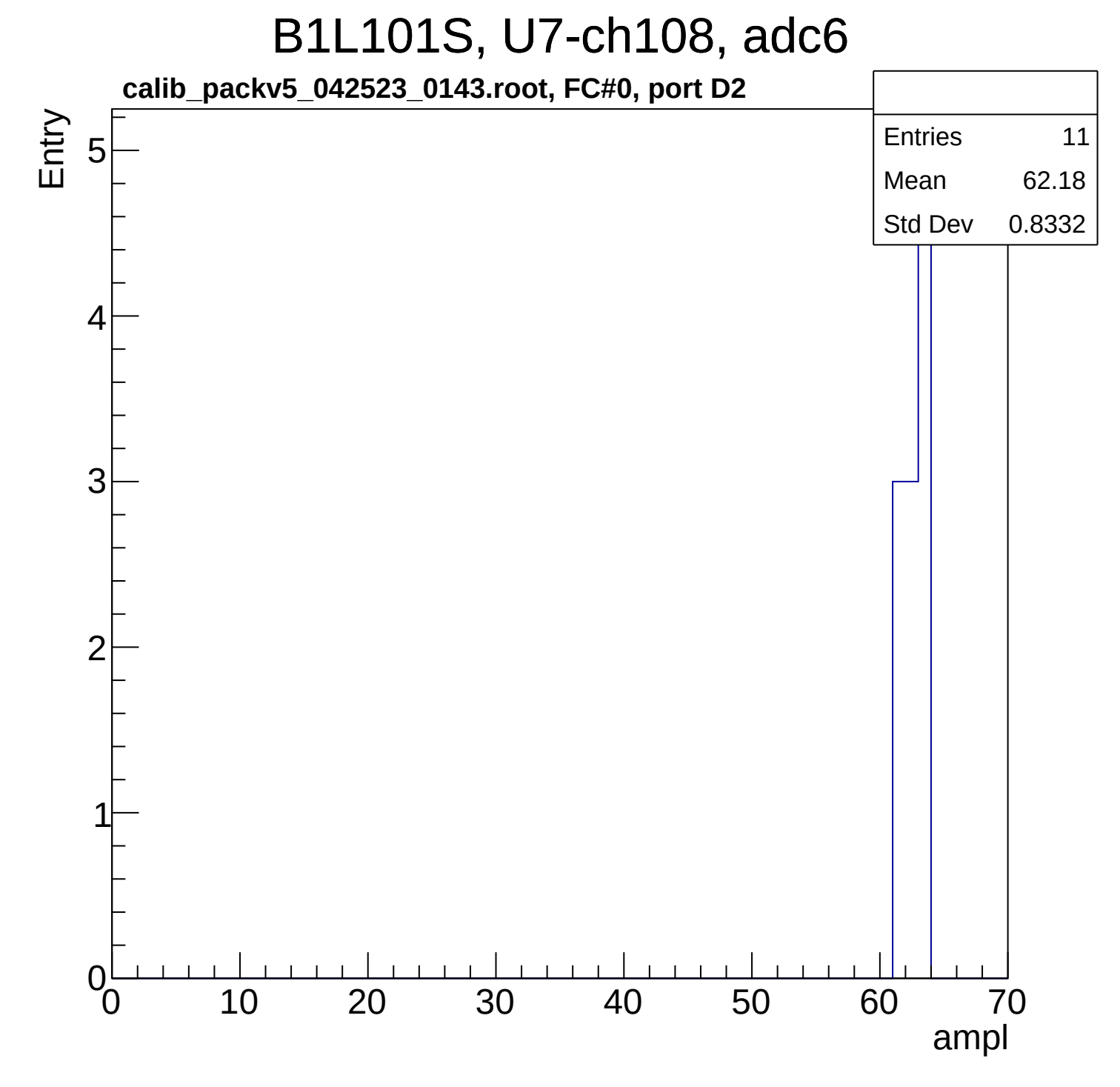
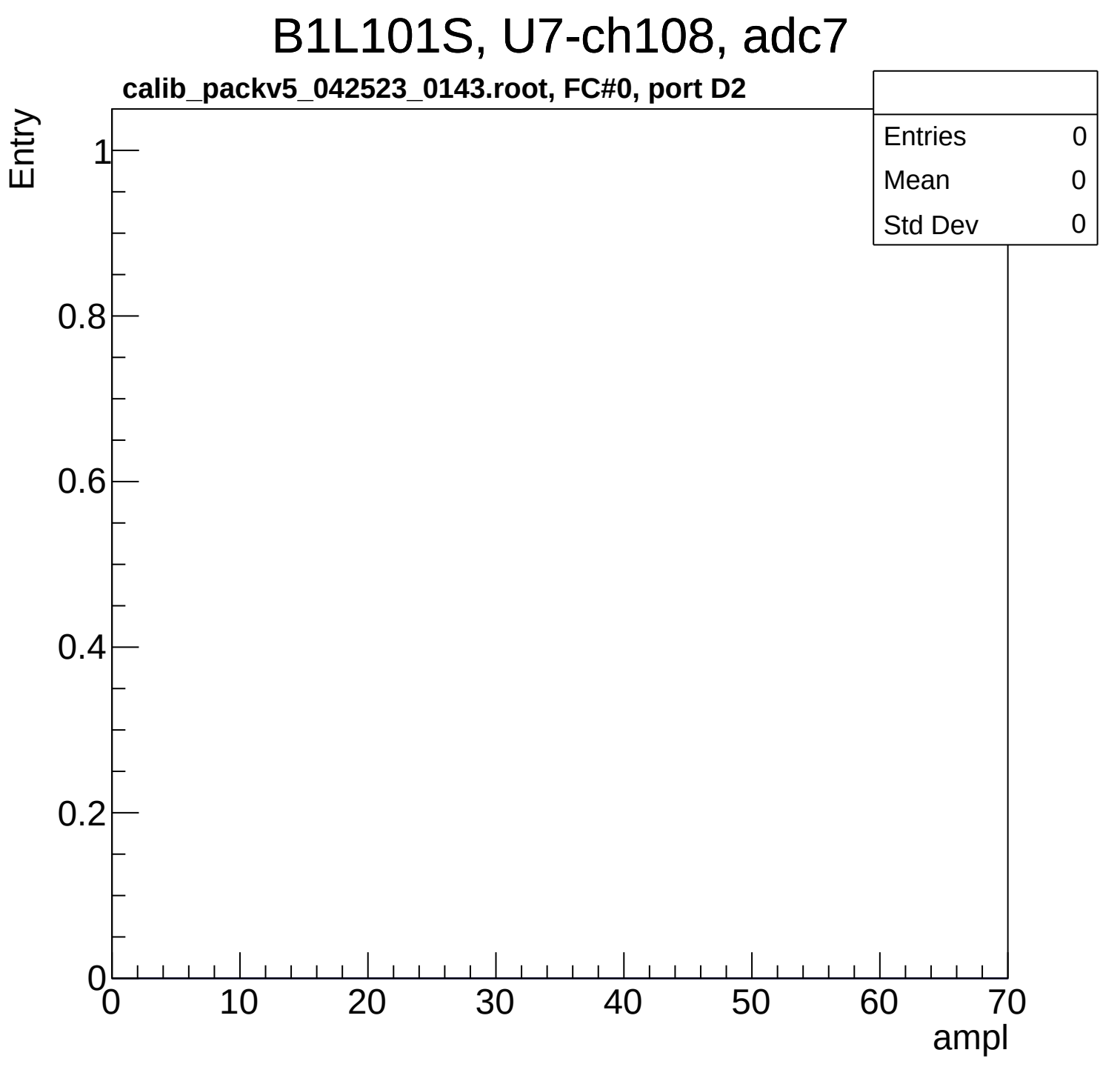
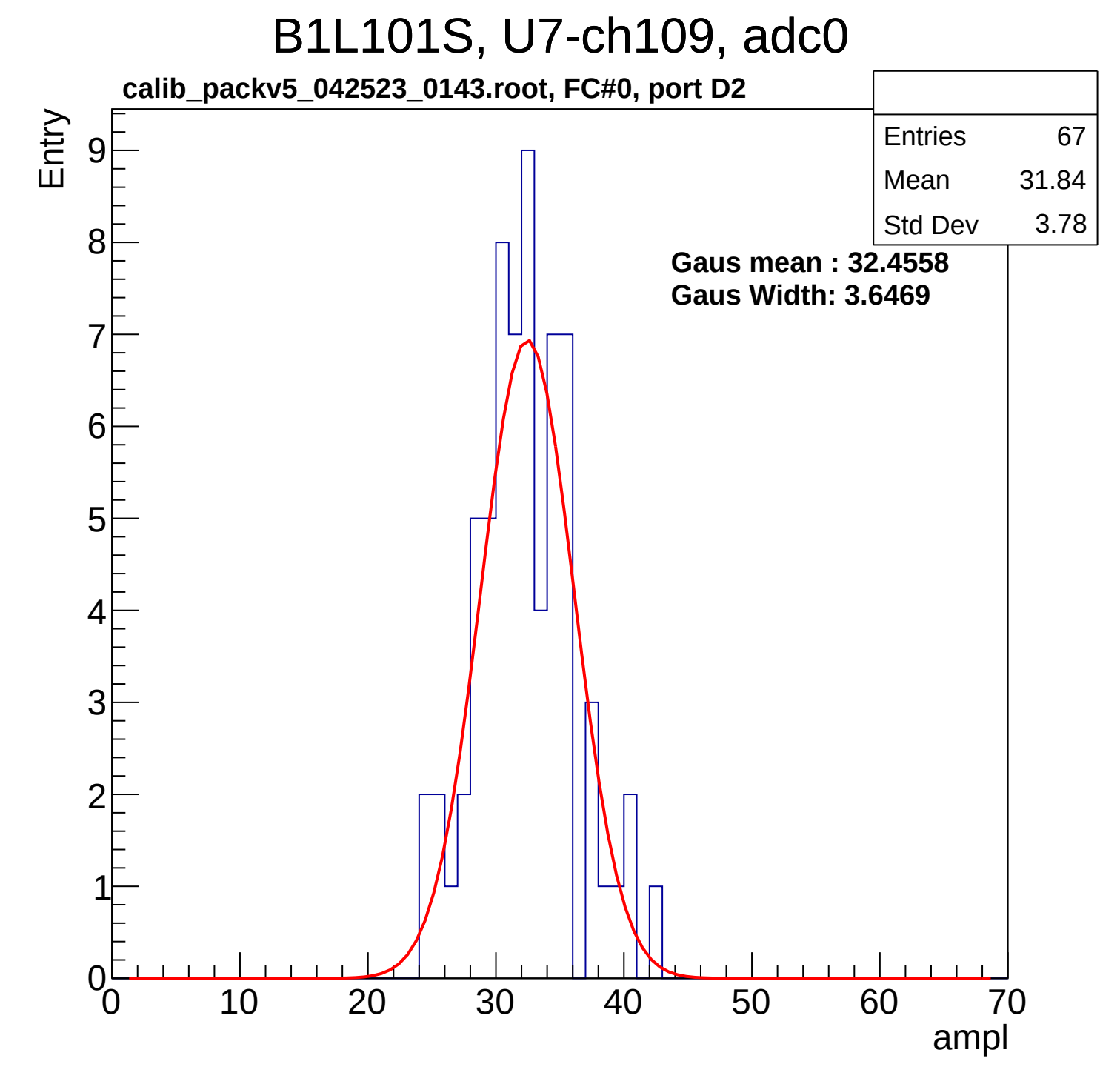
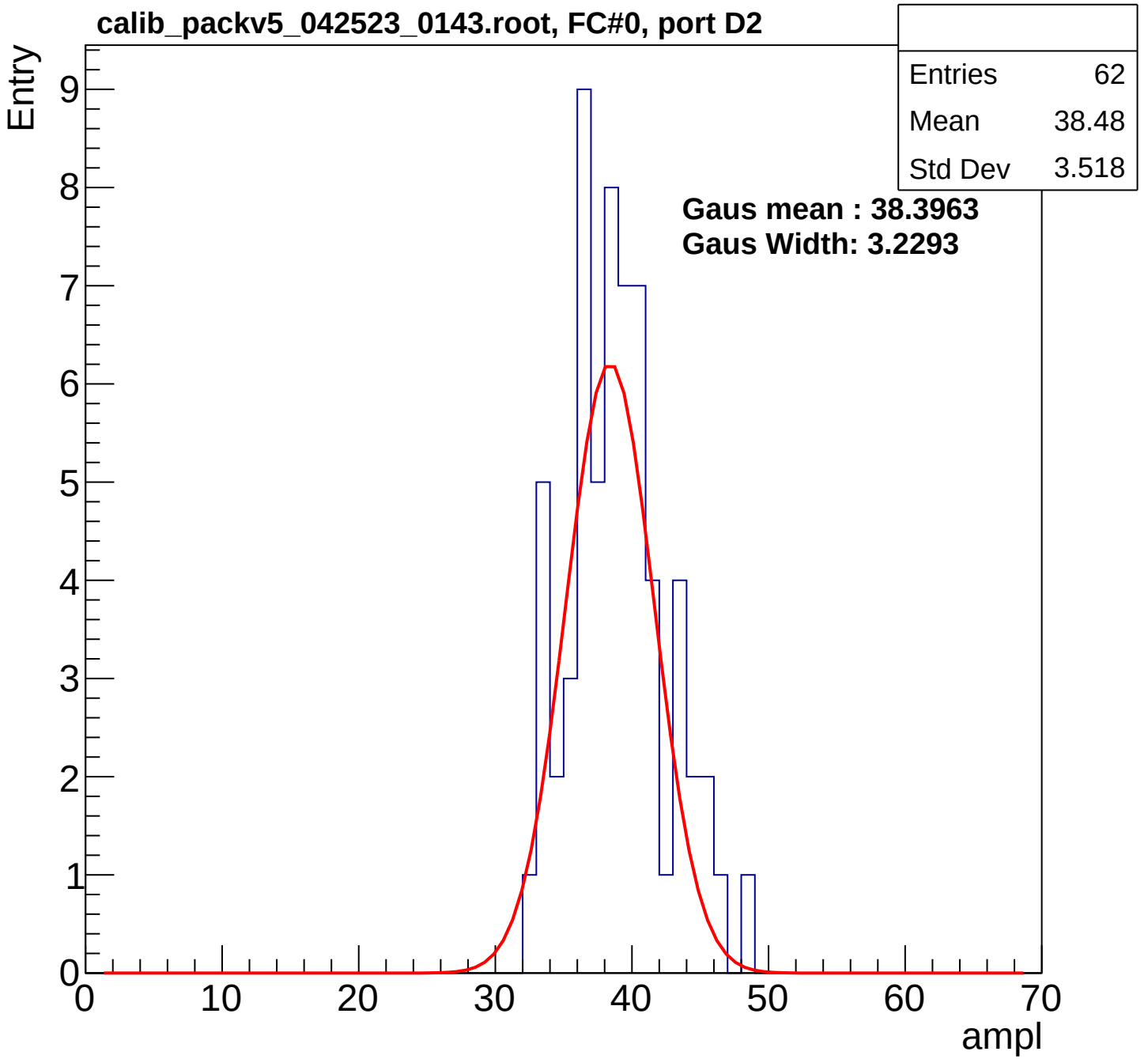

B1L101S, U7-ch108, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 11
Mean 62.18
Std Dev 0.8332
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch108, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch109, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 31.84
Std Dev 3.78
Gaus mean : 32.4558
Gaus Width: 3.6469
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch109, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 38.48
Std Dev 3.518
Gaus mean : 38.3963
Gaus Width: 3.2293
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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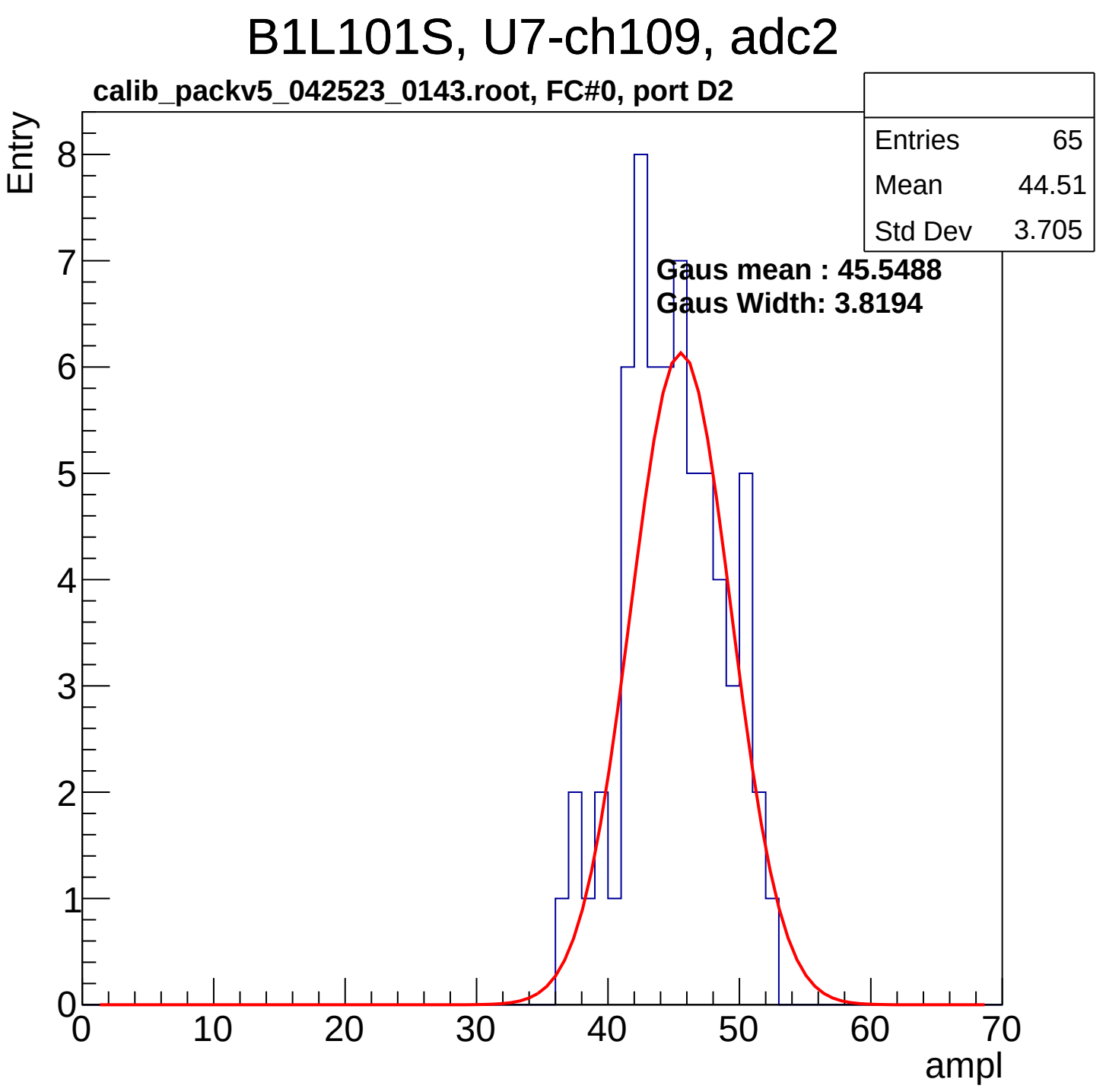
B1L101S, U7-ch109, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 44.51
Std Dev 3.705
Gaus mean : 45.5488
Gaus Width: 3.8194
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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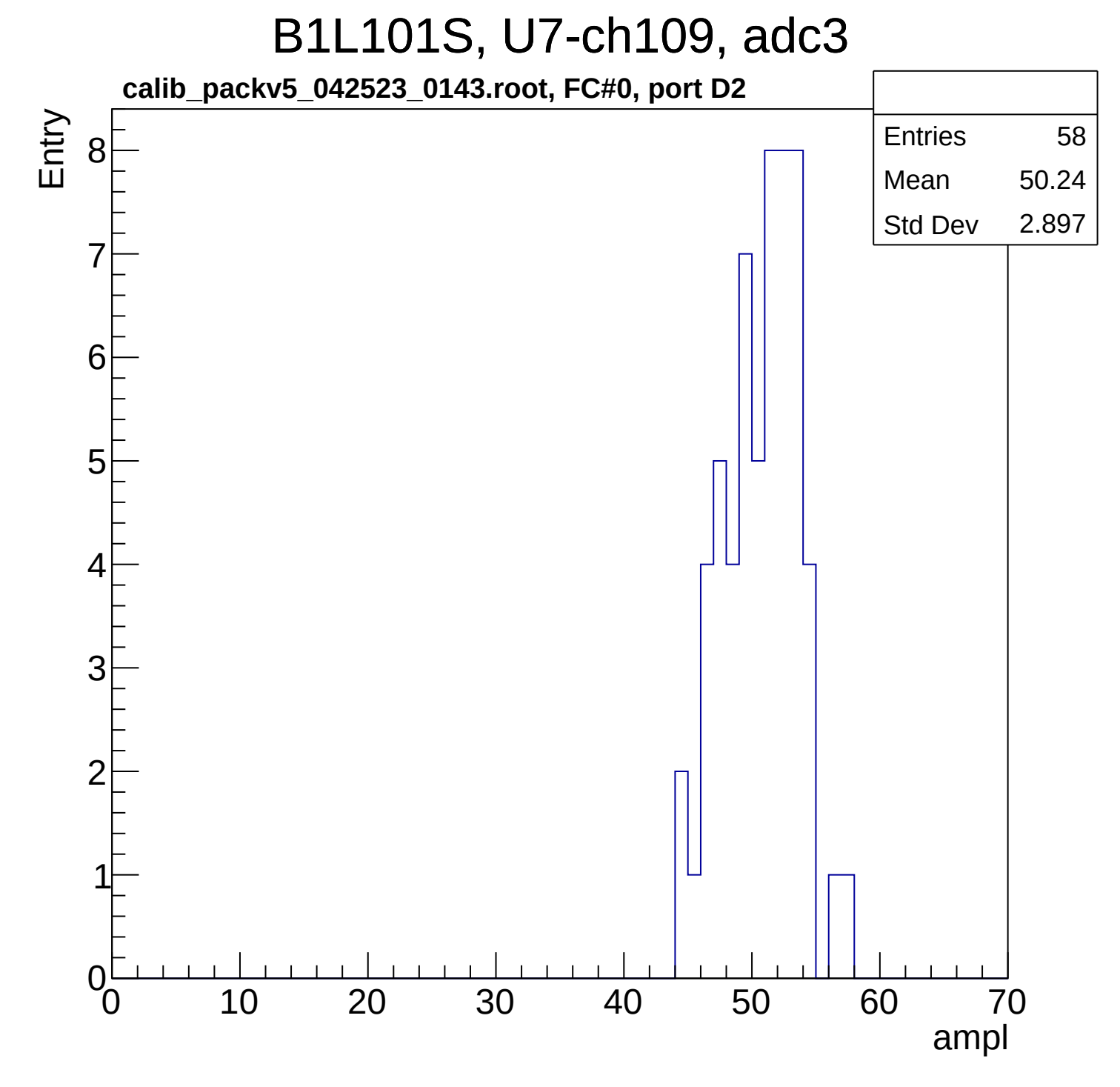
B1L101S, U7-ch109, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 50.24
Std Dev 2.897
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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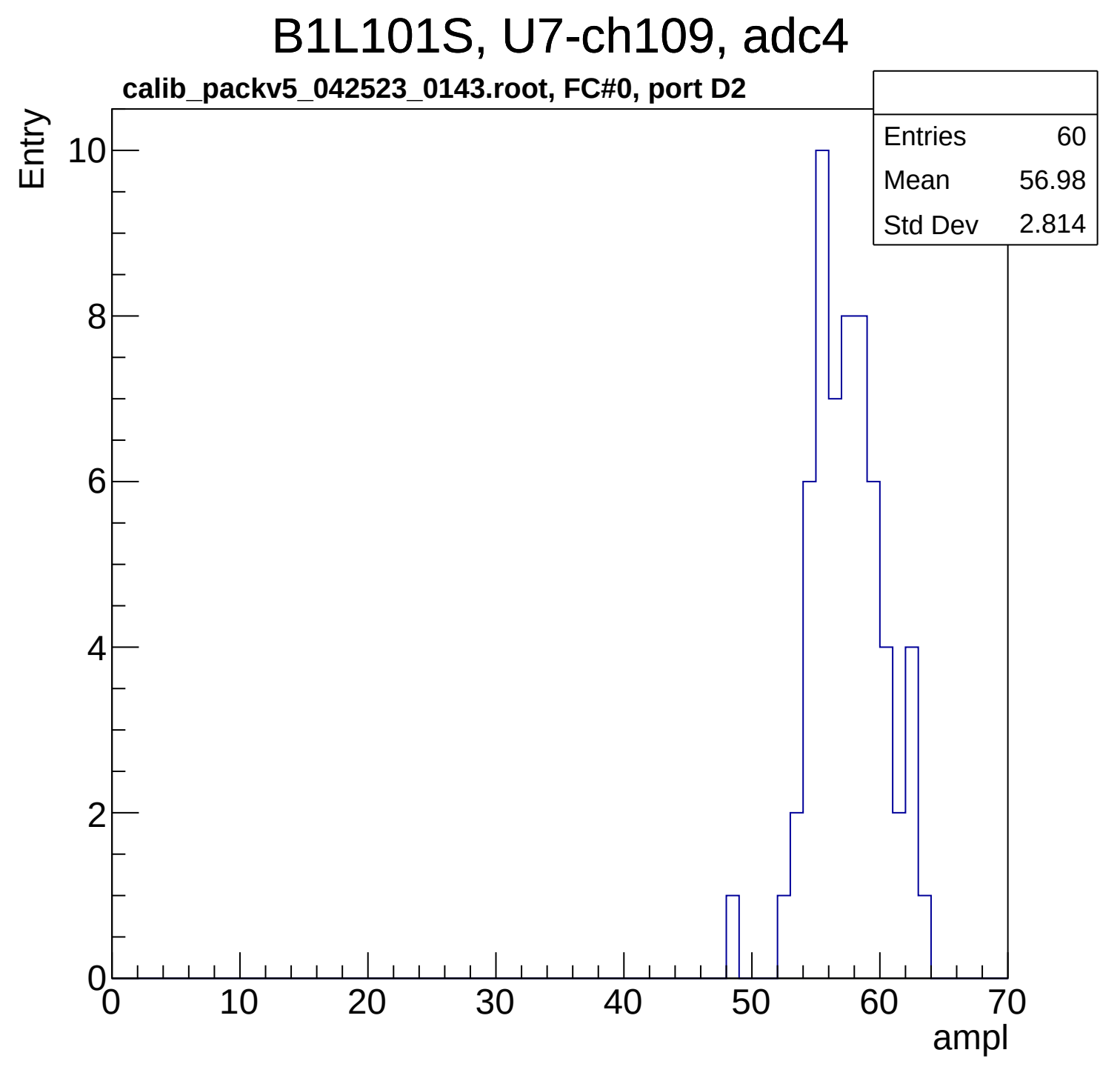
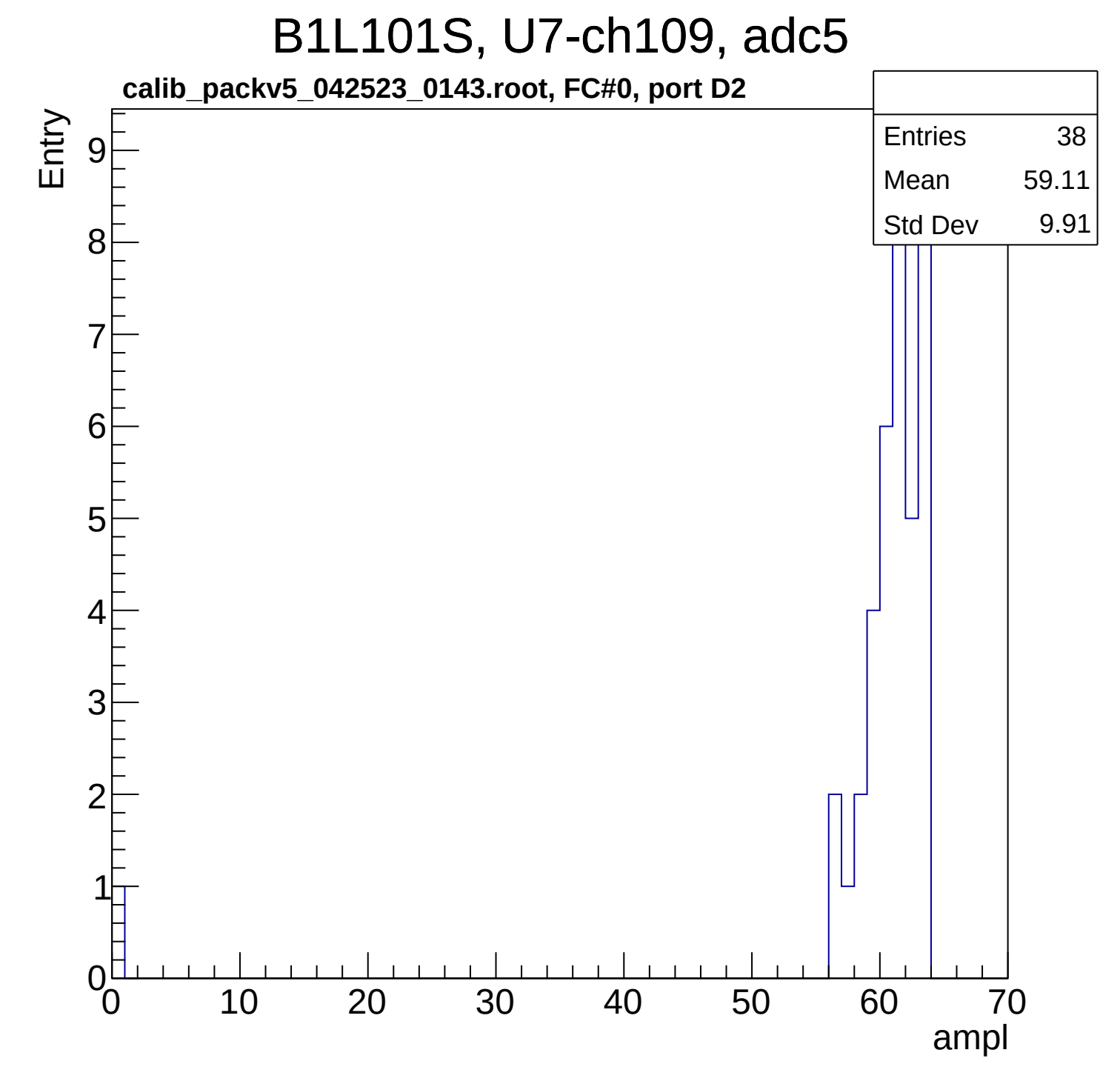
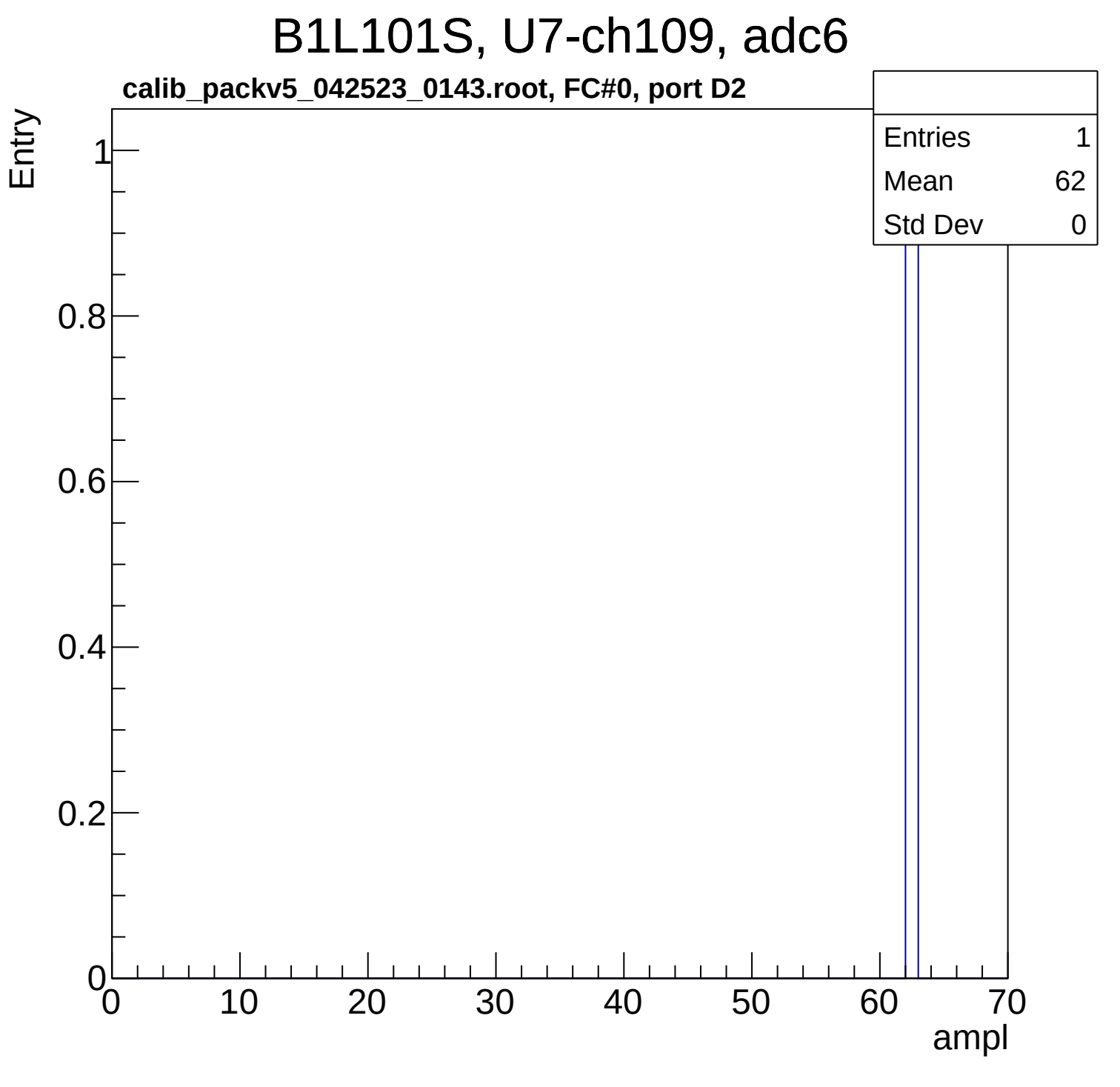

B1L101S, U7-ch109, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 56.98
Std Dev 2.814
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch109, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 38
Mean 59.11
Std Dev 9.91
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch109, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 62
Std Dev 0
Entry
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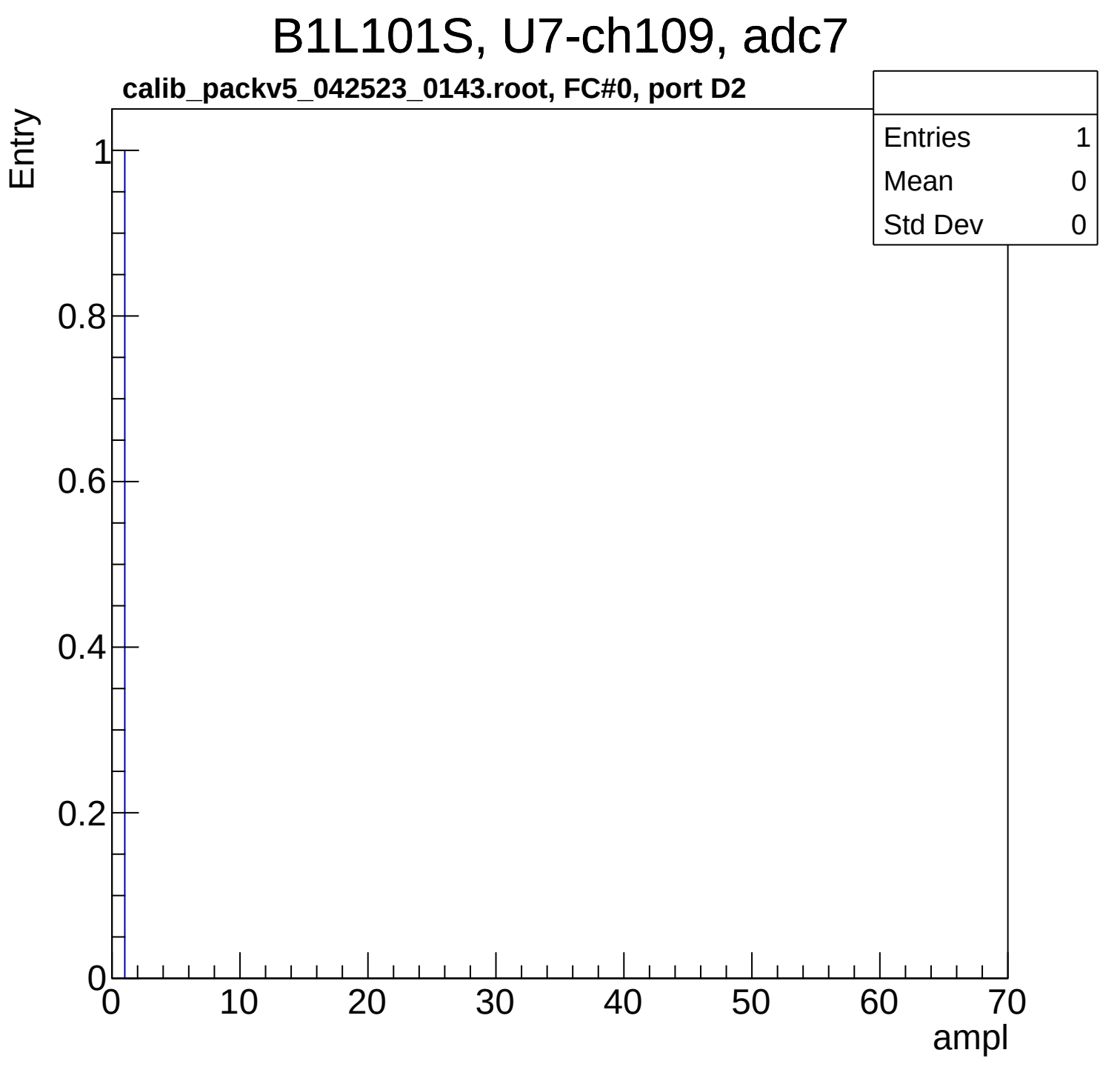
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch109, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
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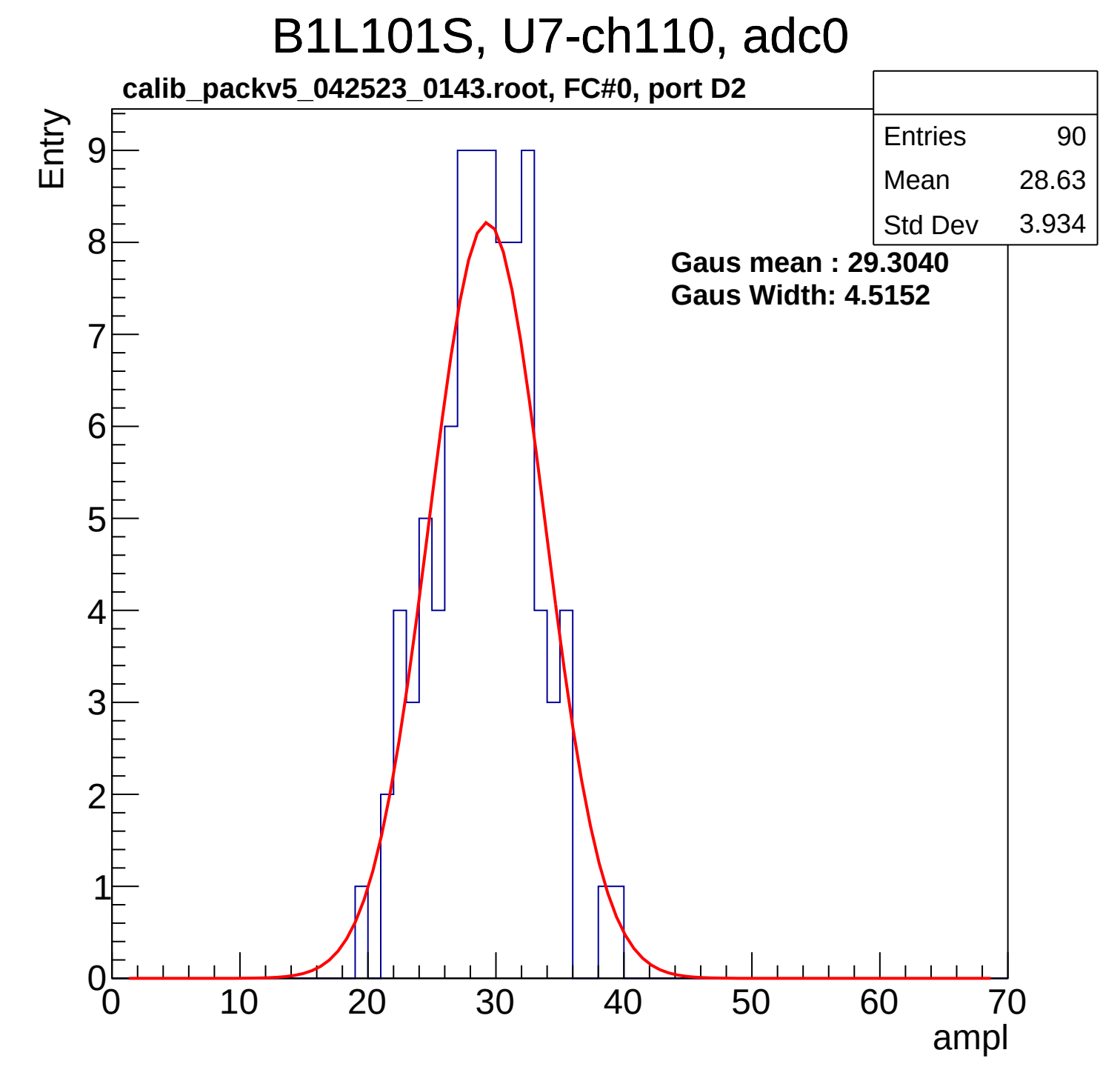
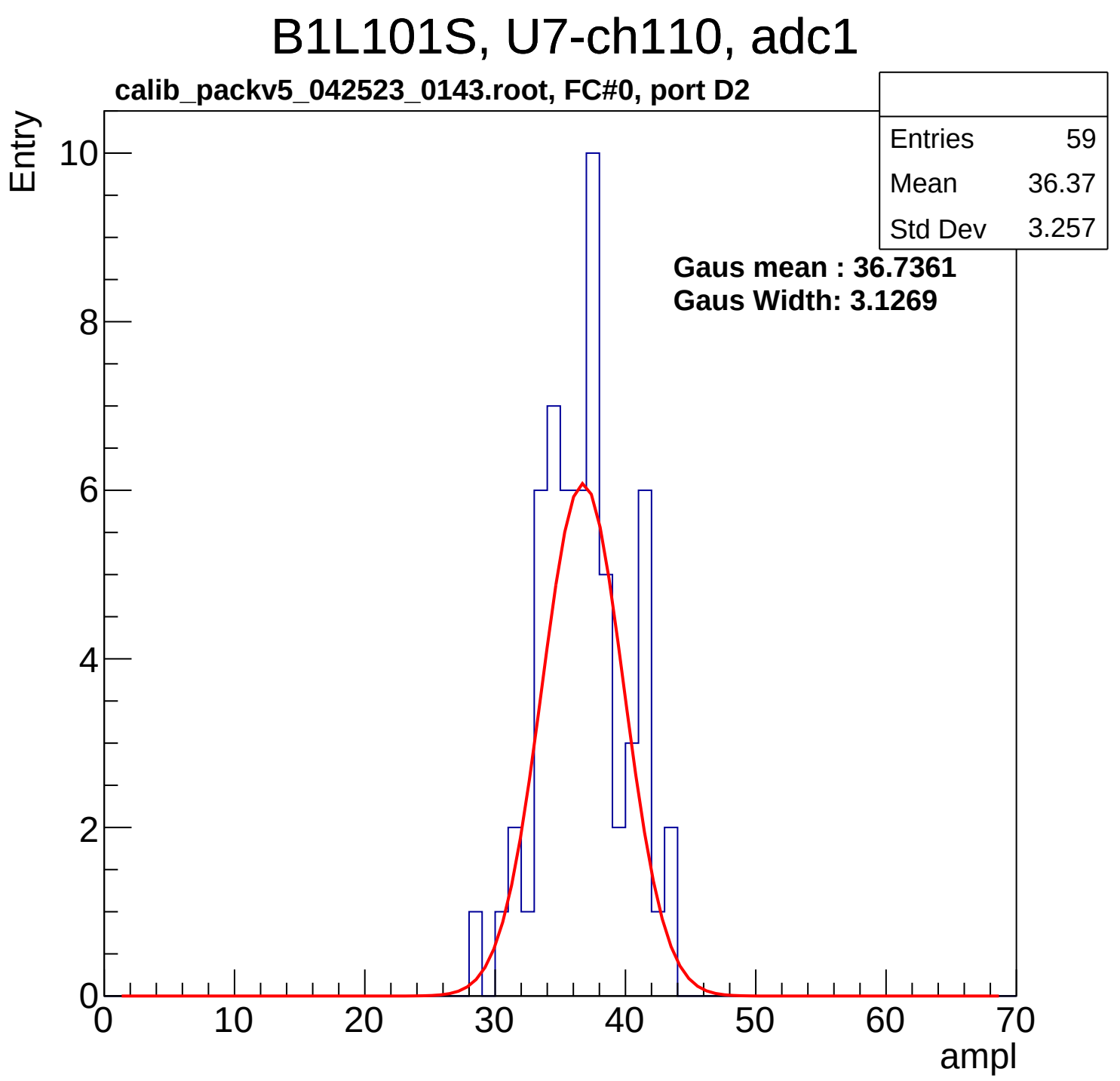
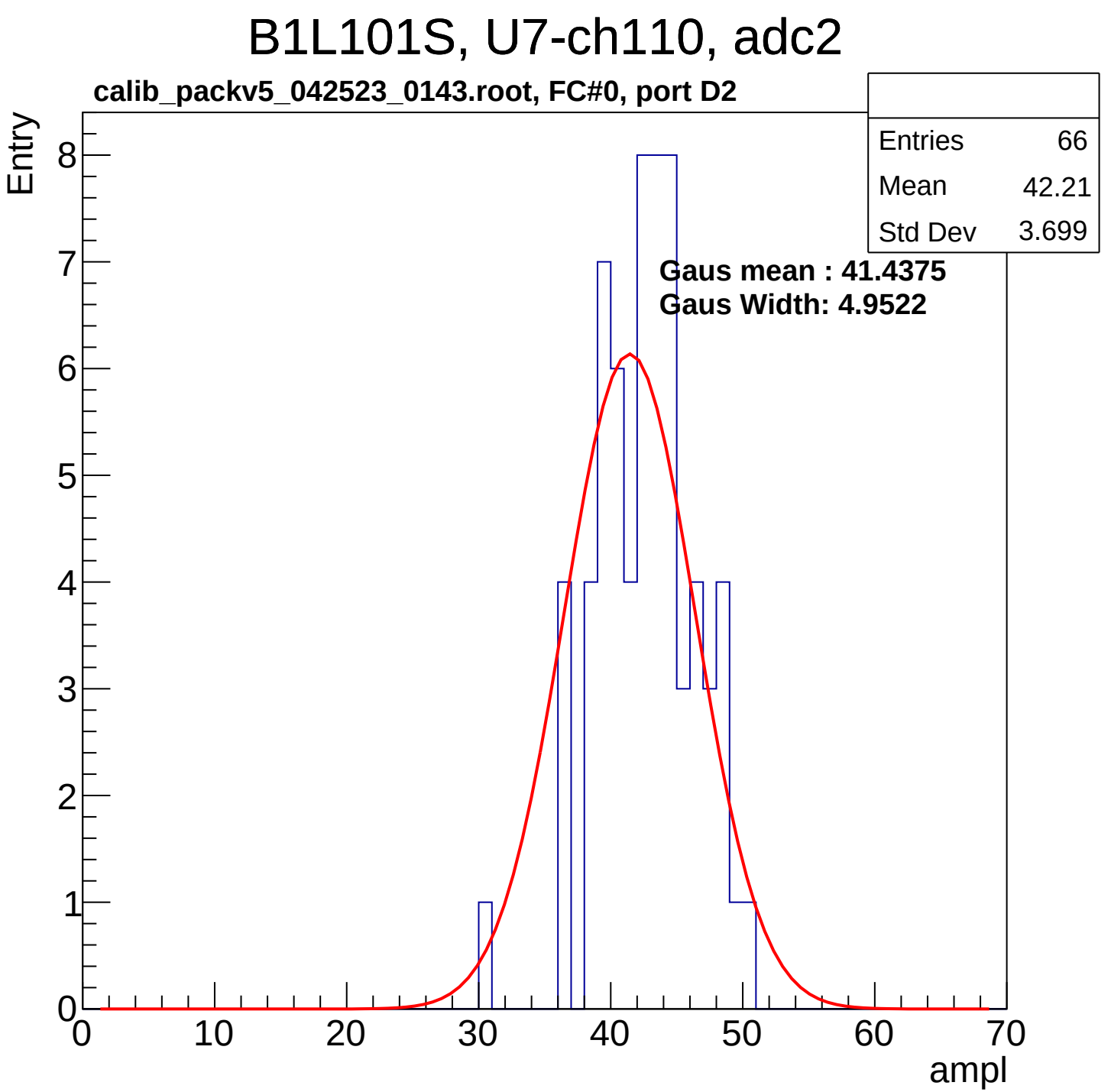
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch110, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 90
Mean 28.63
Std Dev 3.934
Gaus mean : 29.3040
Gaus Width: 4.5152
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch110, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 36.37
Std Dev 3.257
Gaus mean : 36.7361
Gaus Width: 3.1269
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch110, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 42.21
Std Dev 3.699
Gaus mean : 41.4375
Gaus Width: 4.9522
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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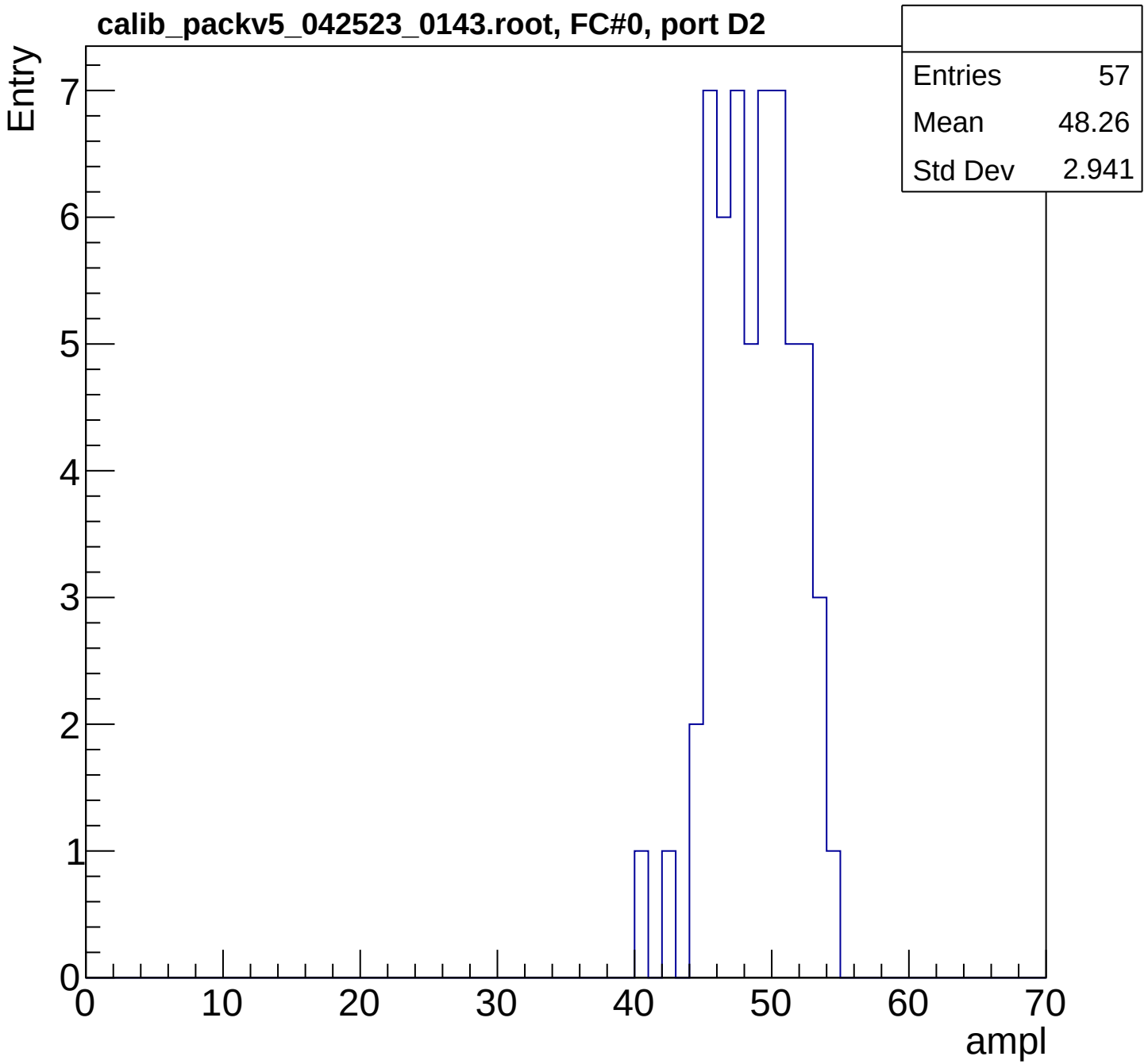
B1L101S, U7-ch110, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 48.26
Std Dev 2.941
Entry
ampl
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1
2
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4
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0
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60
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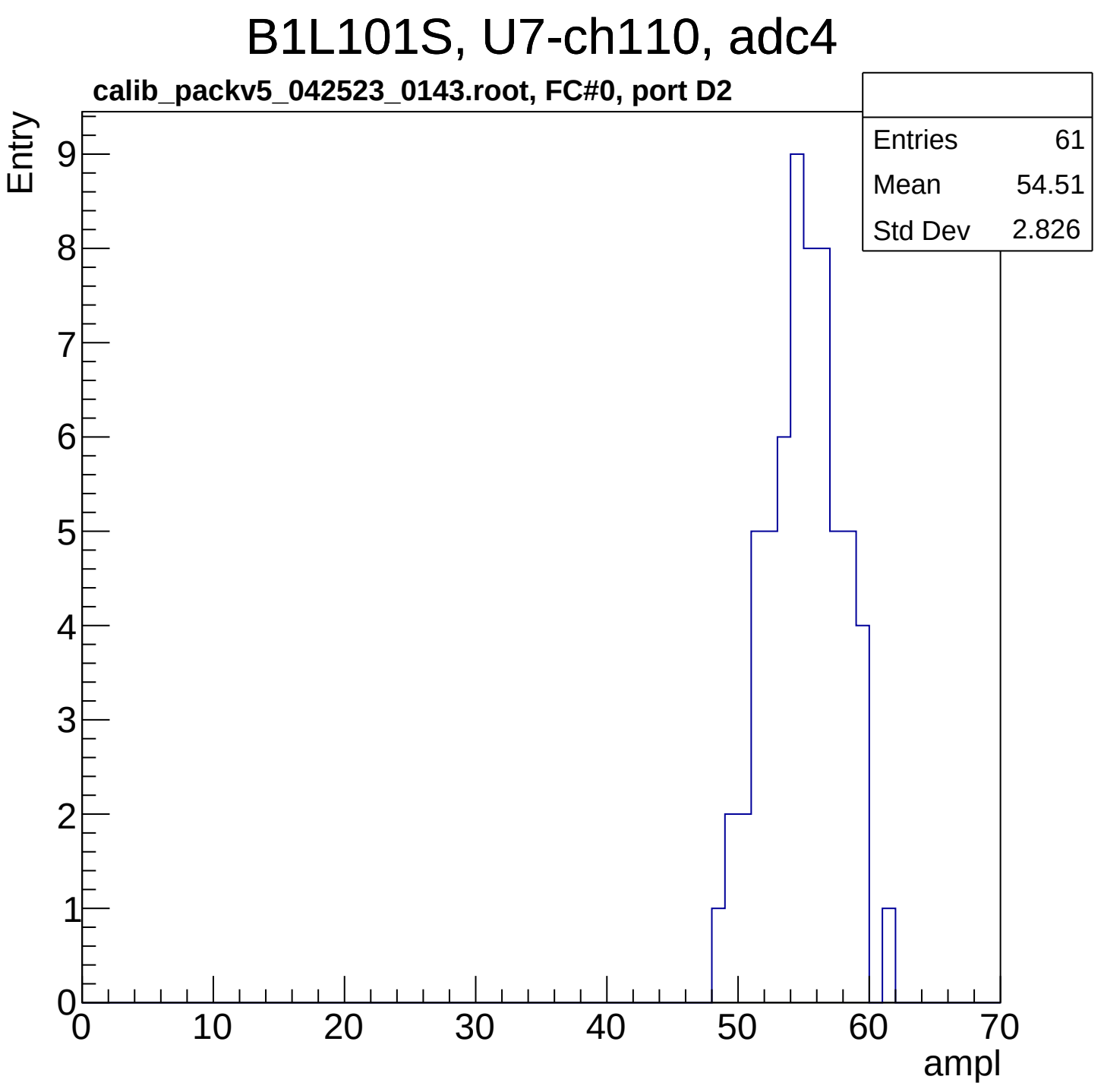
B1L101S, U7-ch110, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 54.51
Std Dev 2.826
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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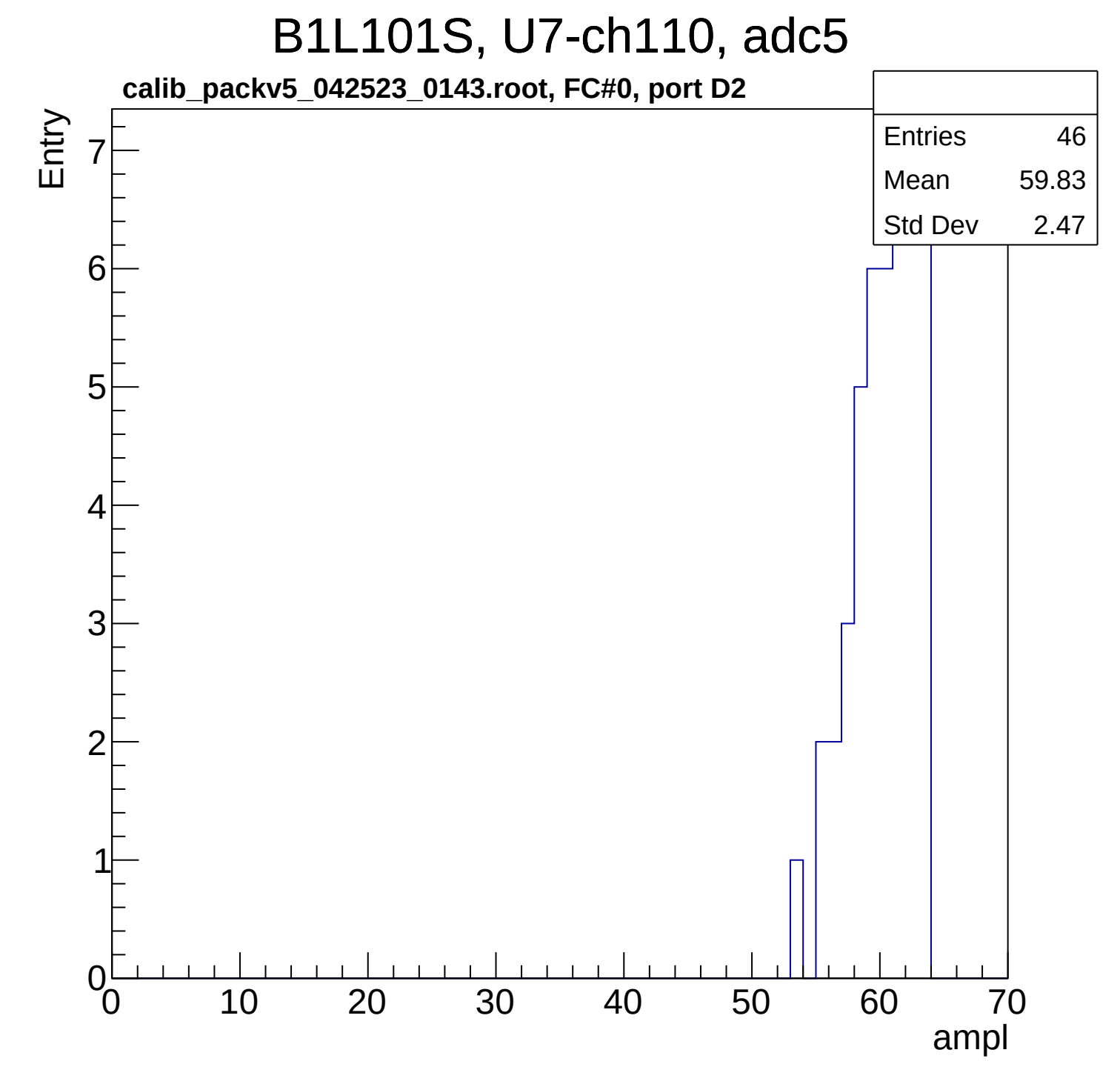
60
70


B1L101S, U7-ch110, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 59.83
Std Dev 2.47
Entry
ampl
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4
5
6
7
0
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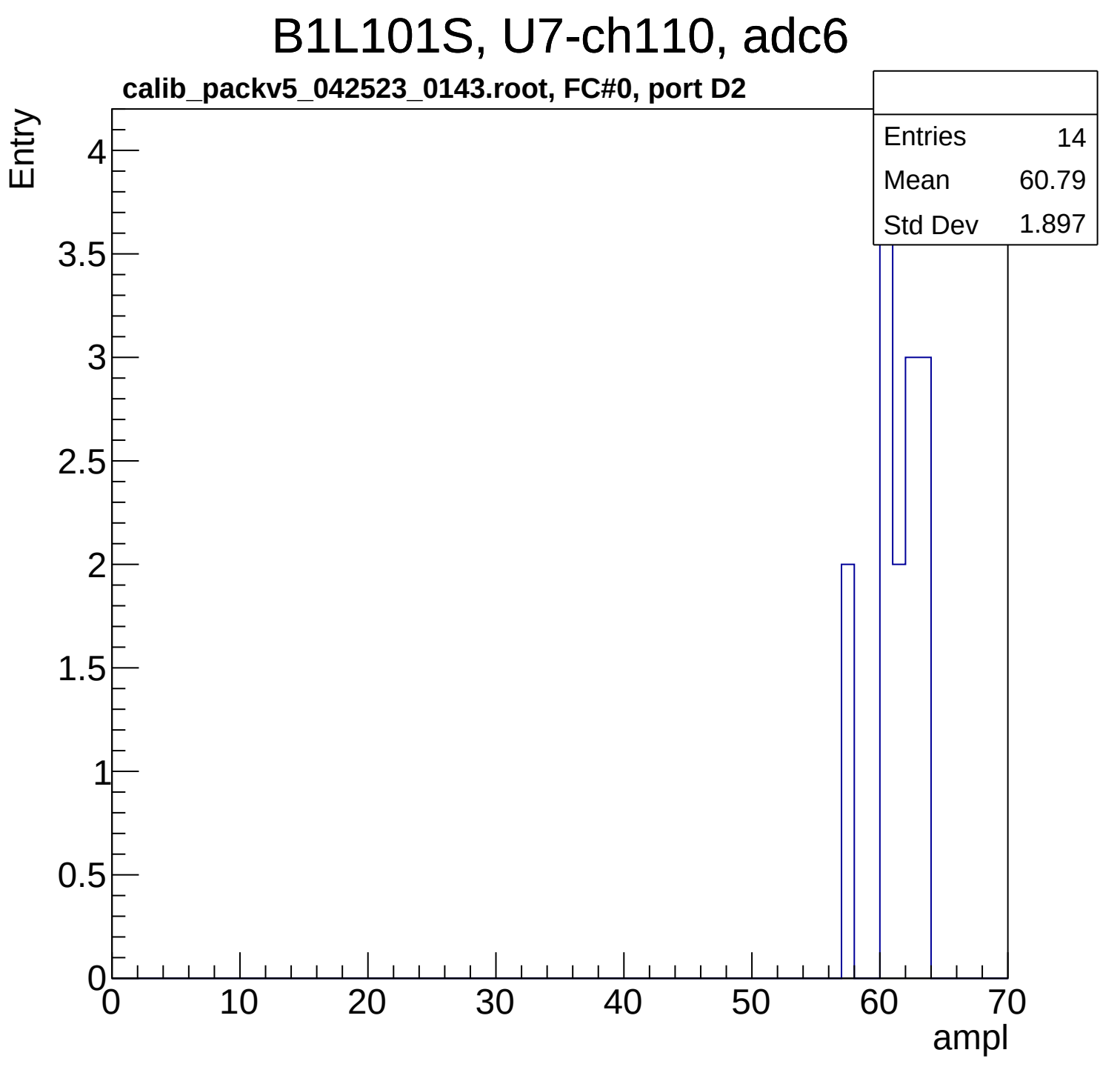
20
30
40
50
60
70


B1L101S, U7-ch110, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 14
Mean 60.79
Std Dev 1.897
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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20
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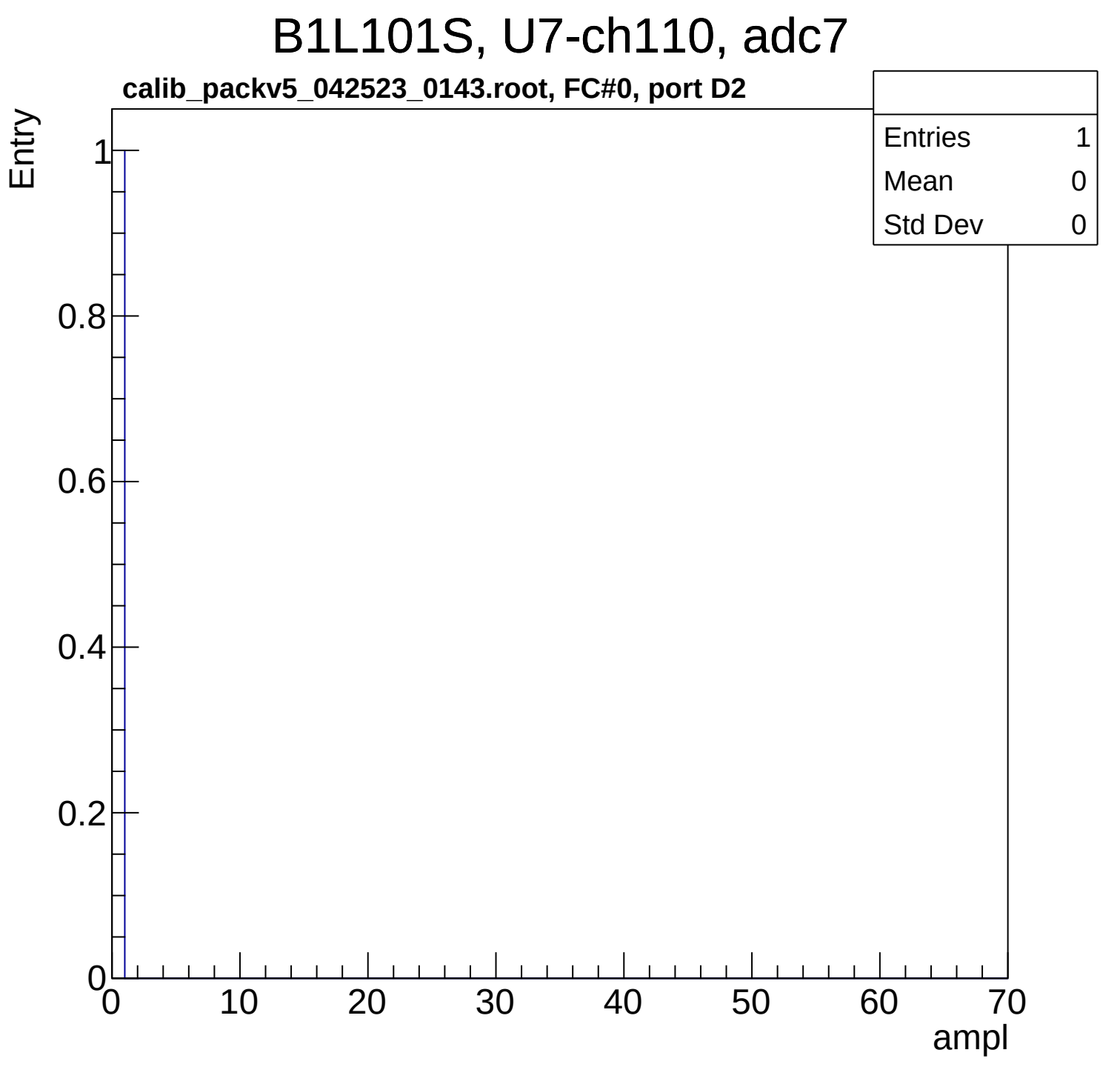
40
50
60
70


B1L101S, U7-ch110, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
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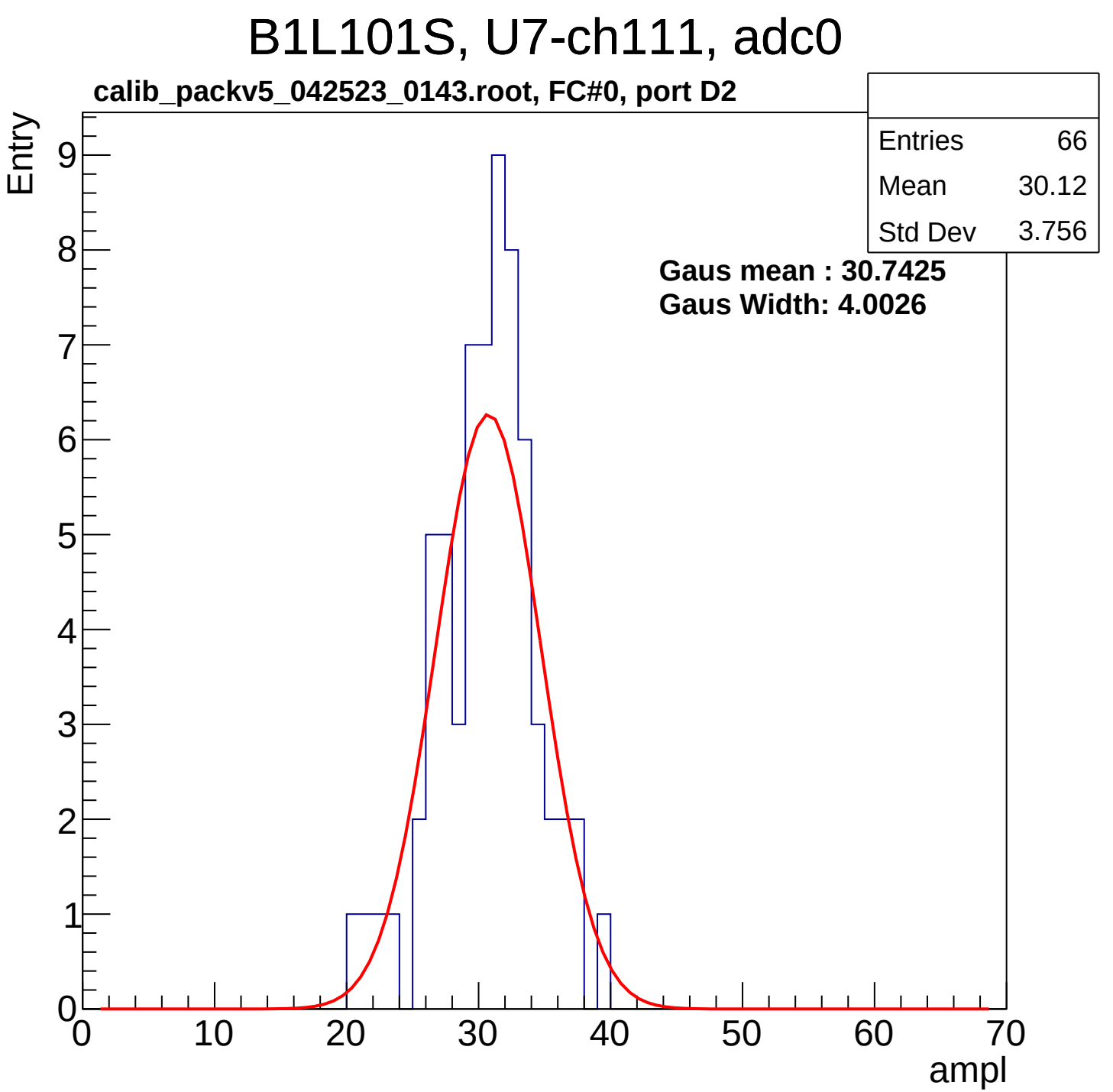
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch111, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 30.12
Std Dev 3.756
Gaus mean : 30.7425
Gaus Width: 4.0026
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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30
40
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60
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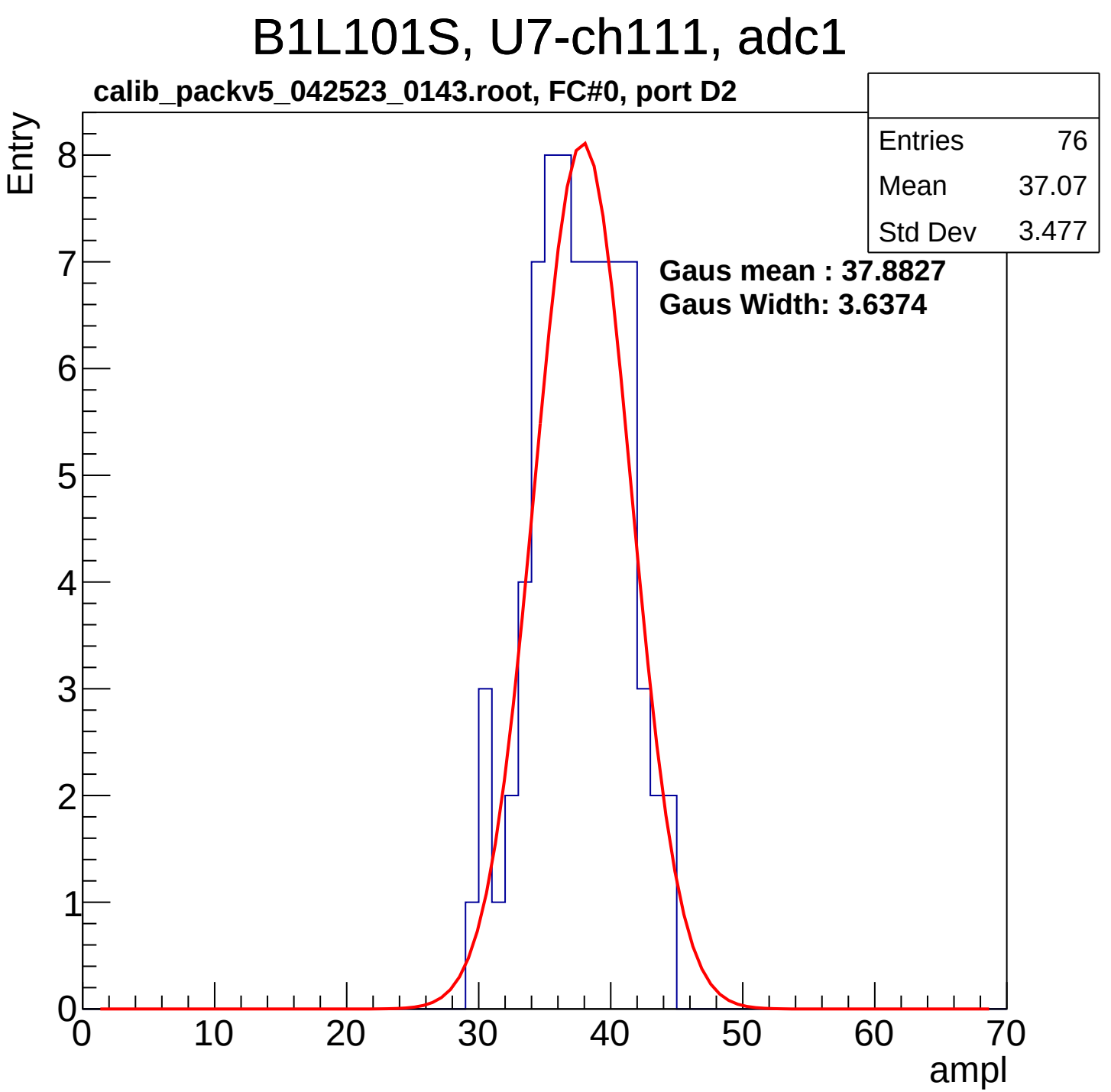
B1L101S, U7-ch111, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 37.07
Std Dev 3.477
Gaus mean : 37.8827
Gaus Width: 3.6374
Entry
ampl
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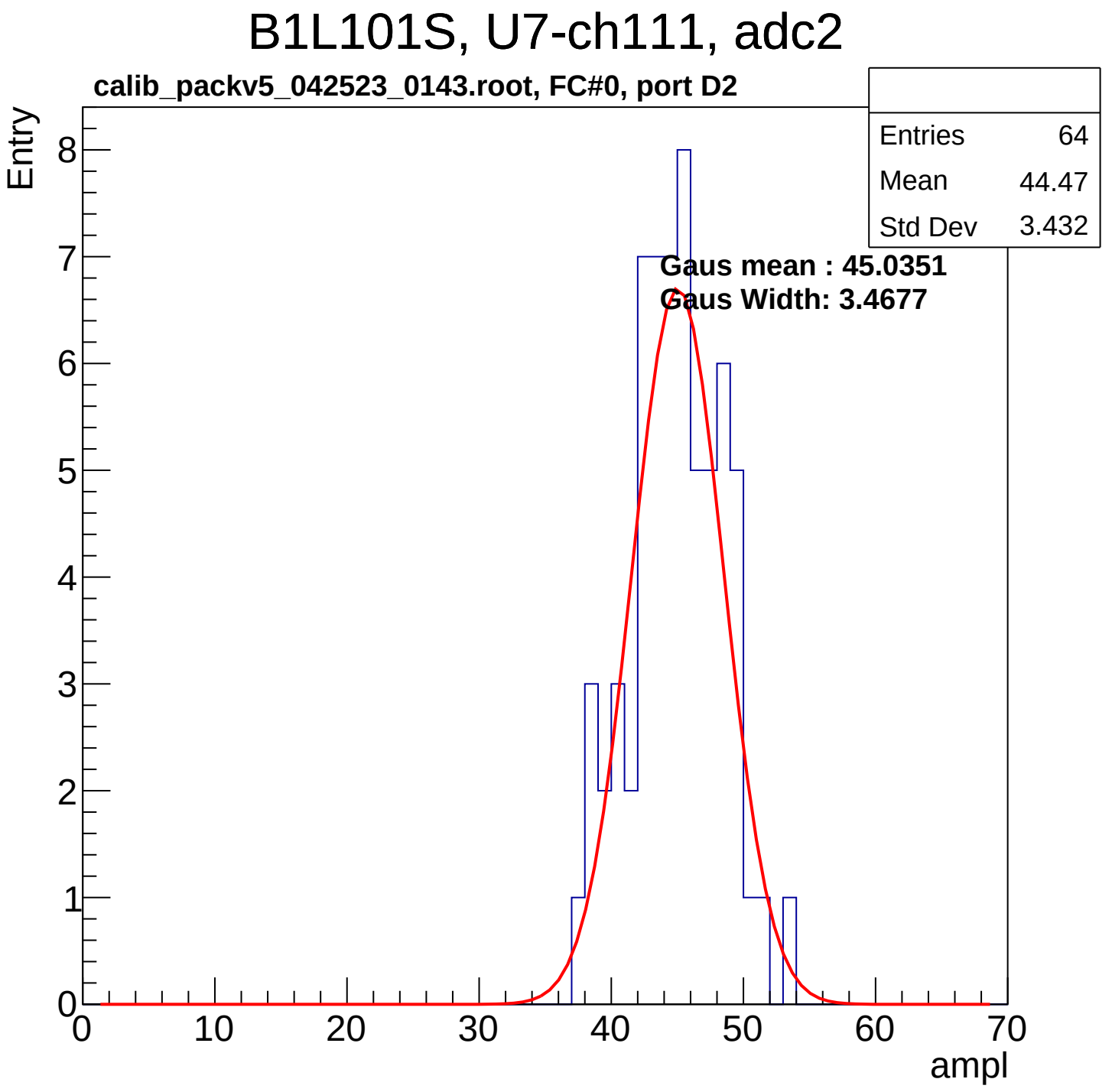
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch111, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 44.47
Std Dev 3.432
Gaus mean : 45.0351
Gaus Width: 3.4677
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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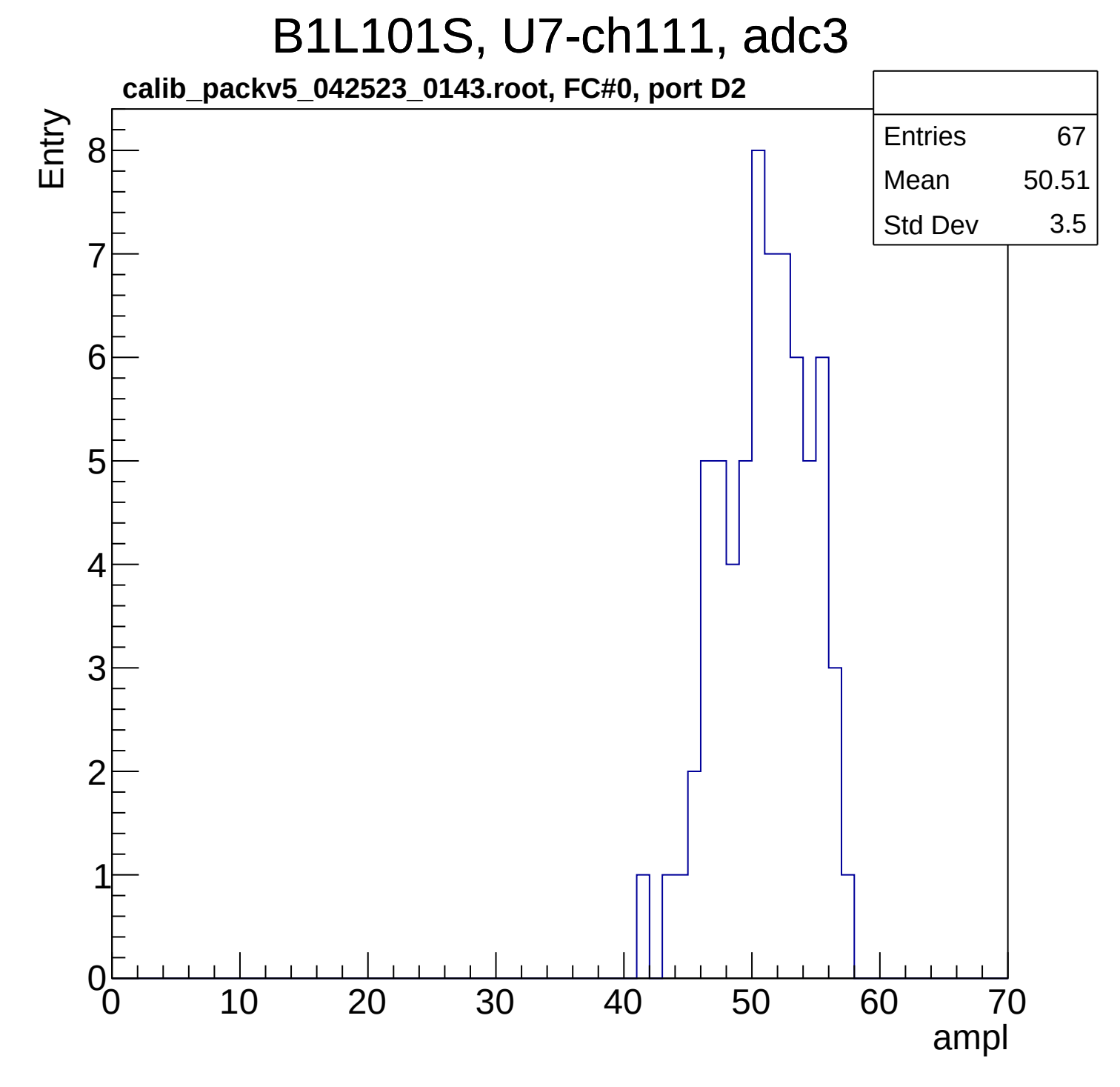
B1L101S, U7-ch111, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 50.51
Std Dev 3.5
Entry
ampl
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2
3
4
5
6
7
8
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40
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60
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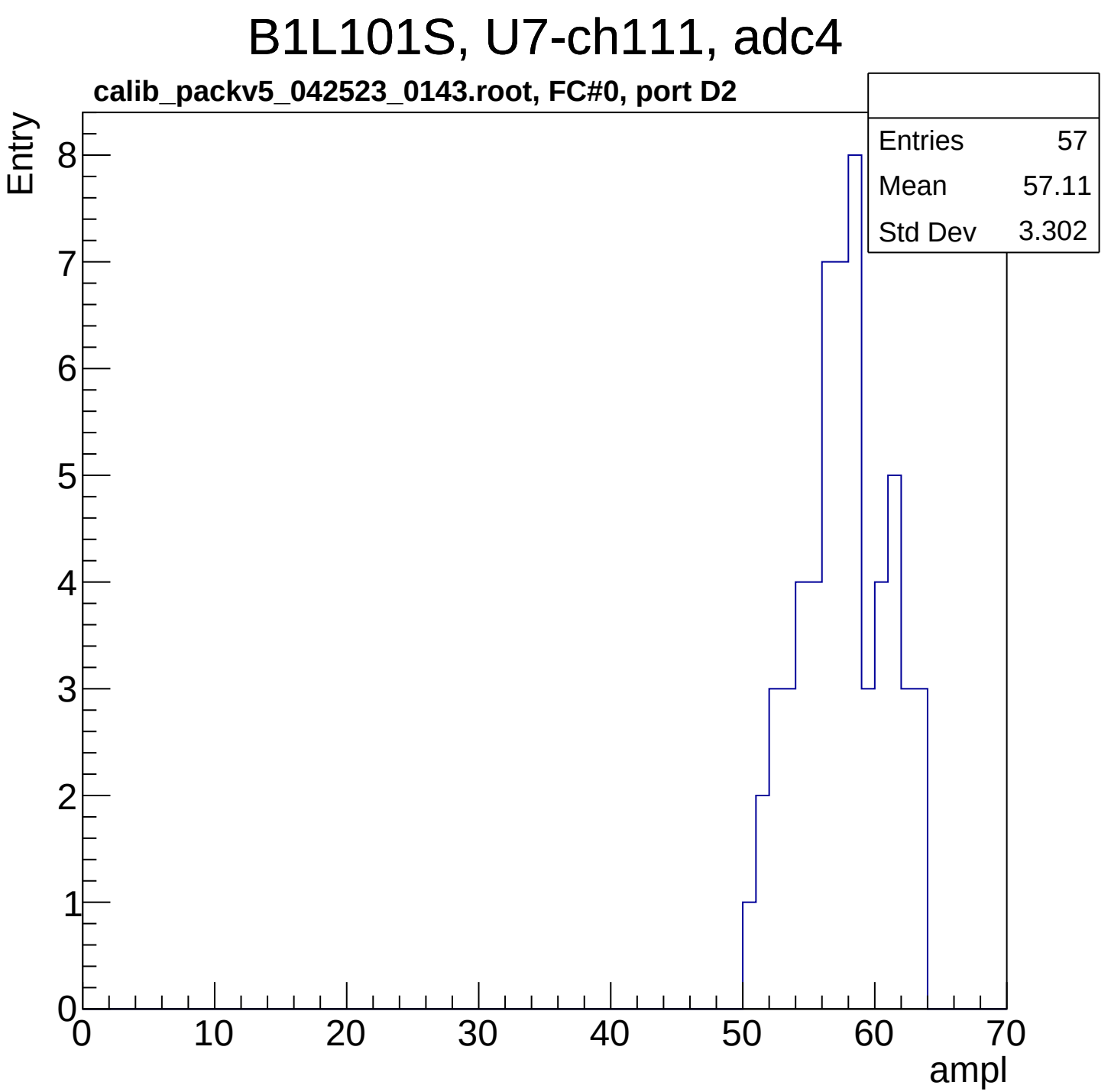
B1L101S, U7-ch111, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 57.11
Std Dev 3.302
Entry
ampl
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1
2
3
4
5
6
7
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0
10
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40
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60
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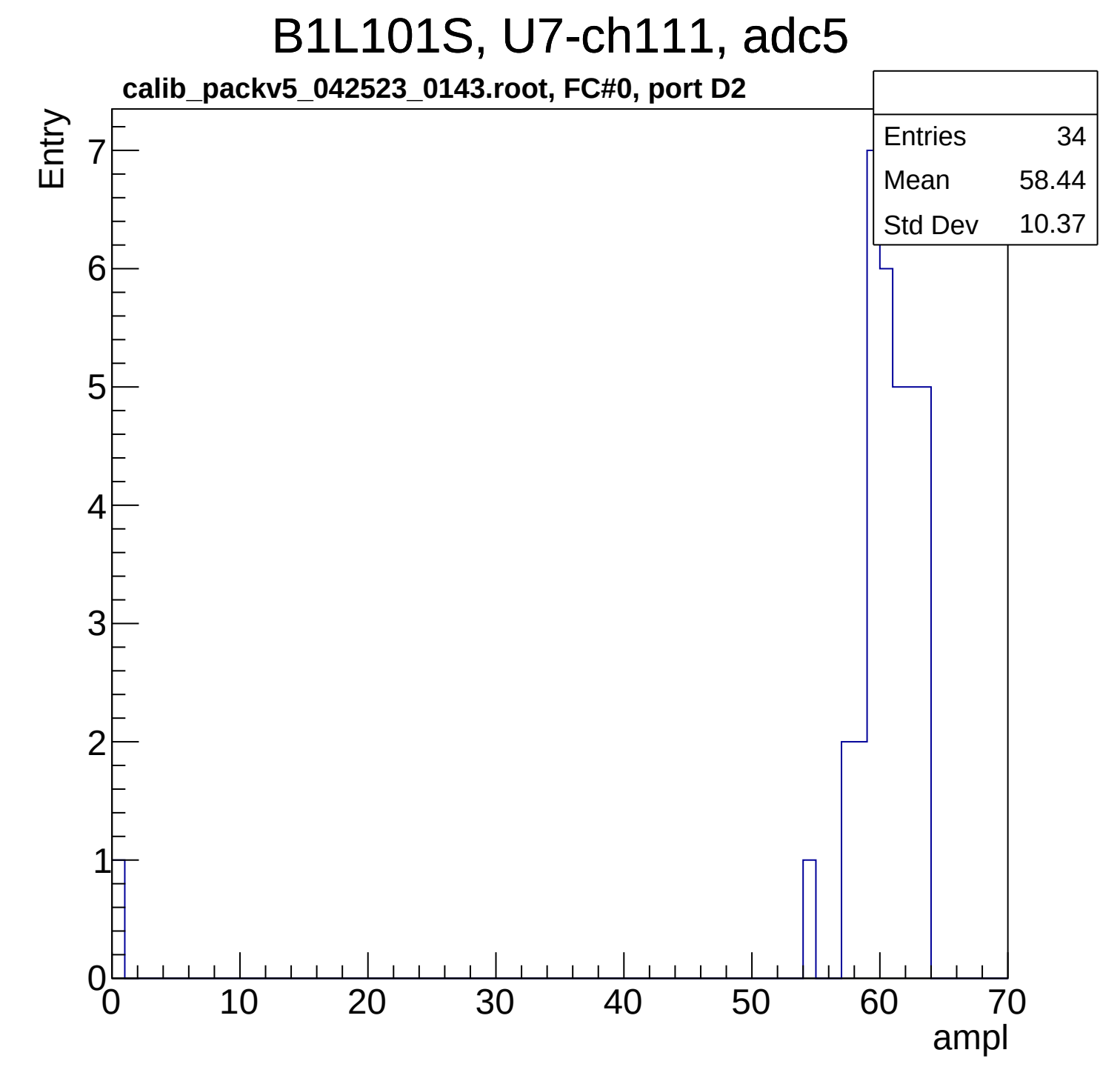
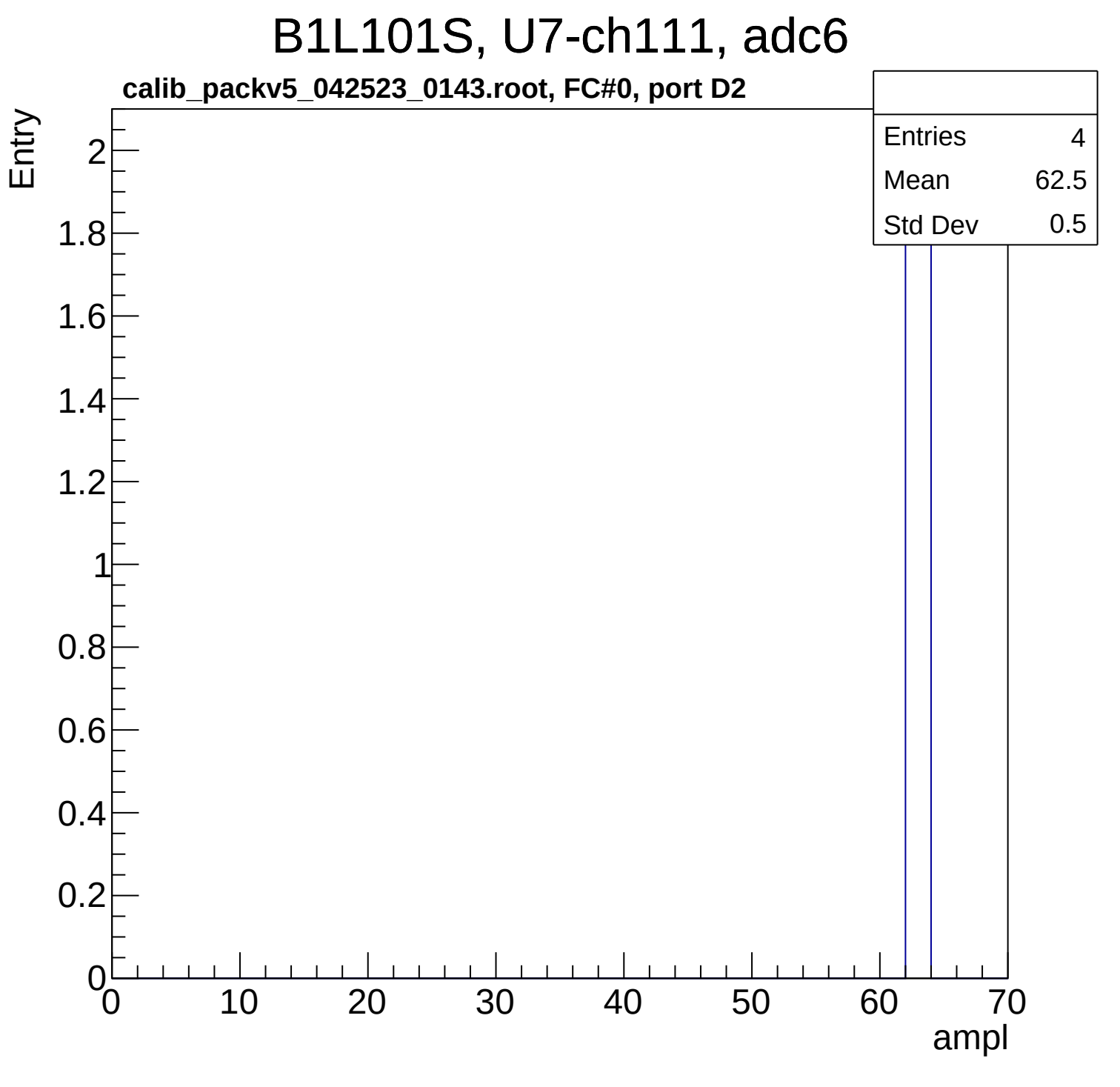
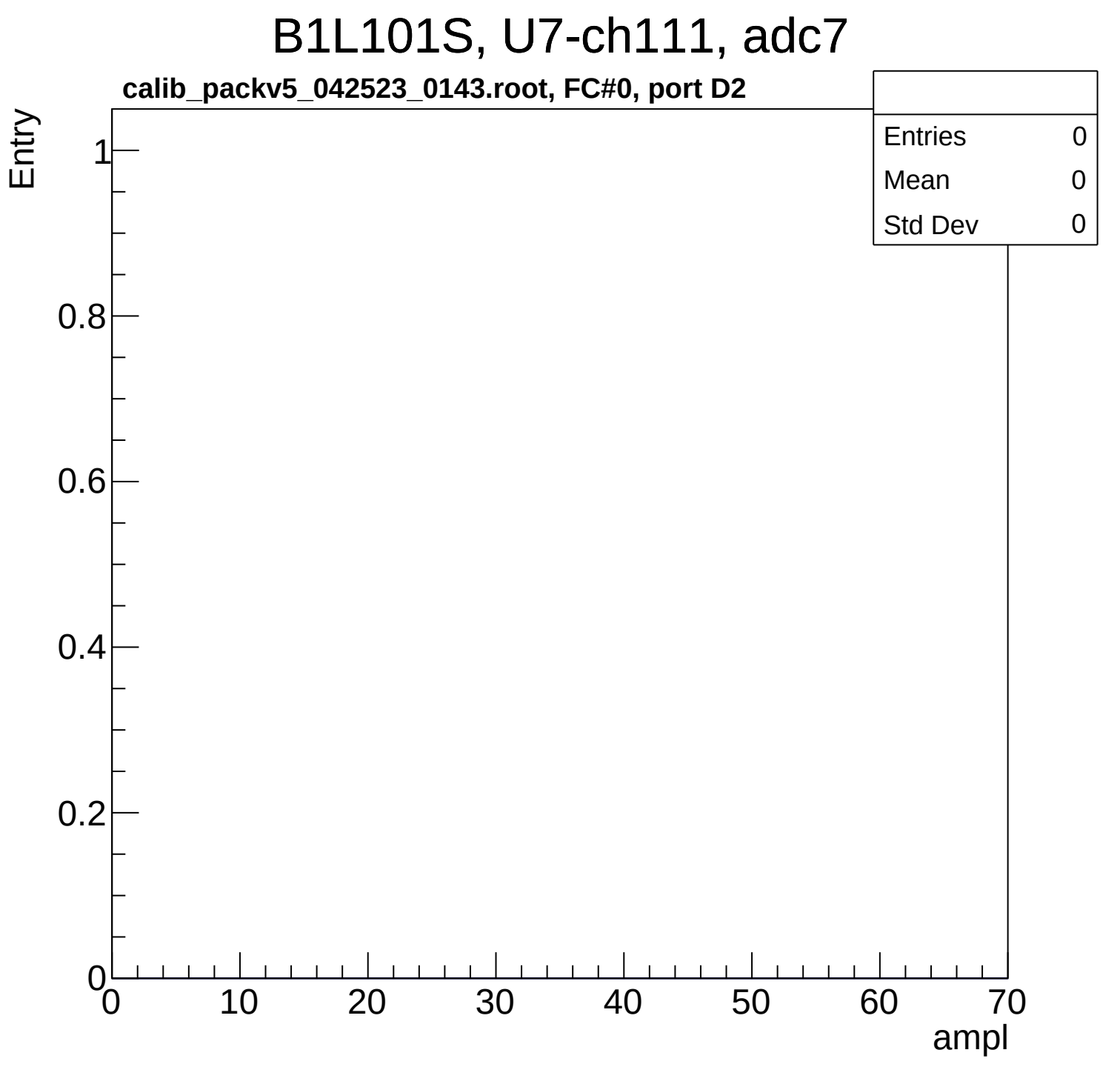
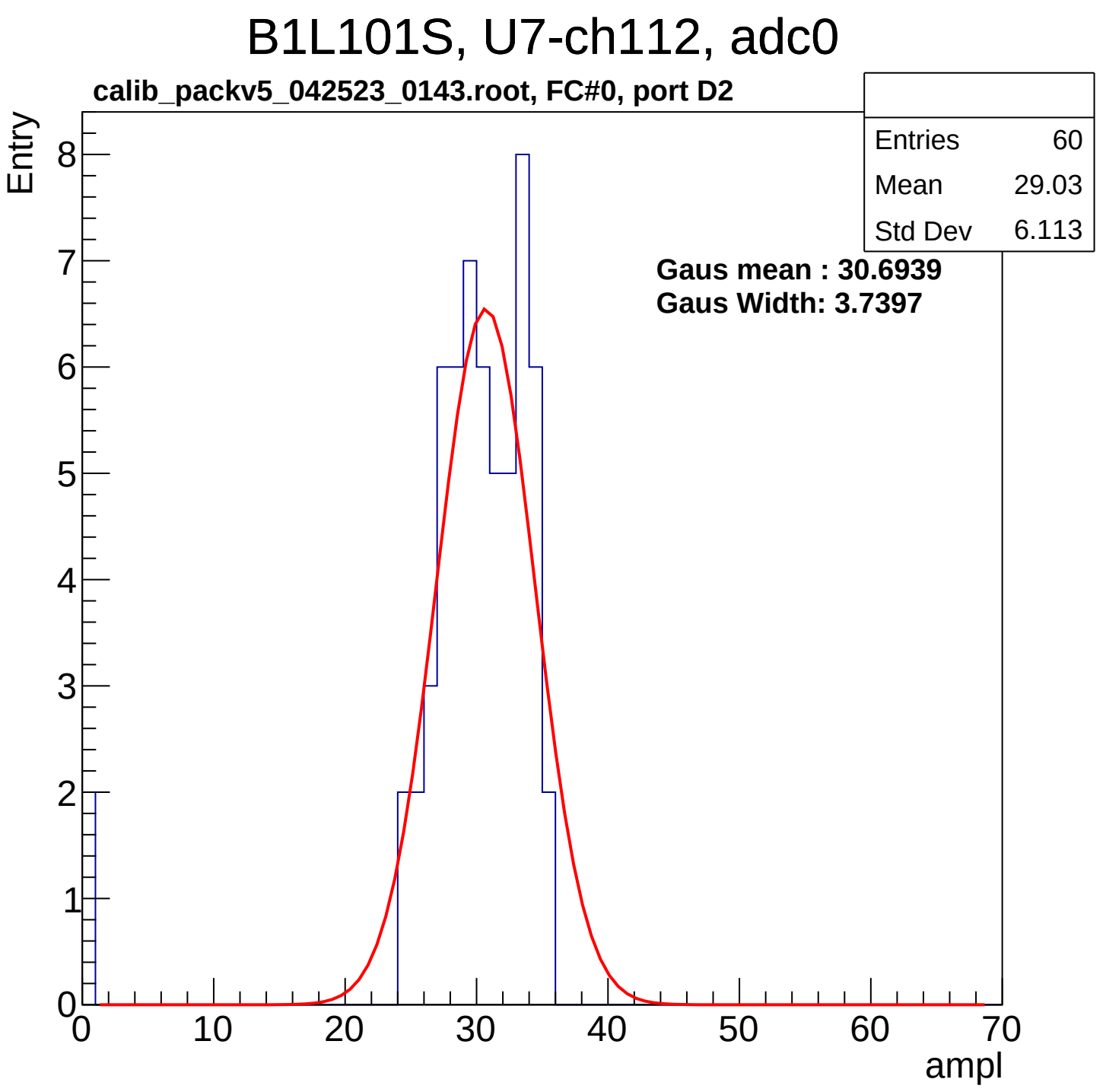
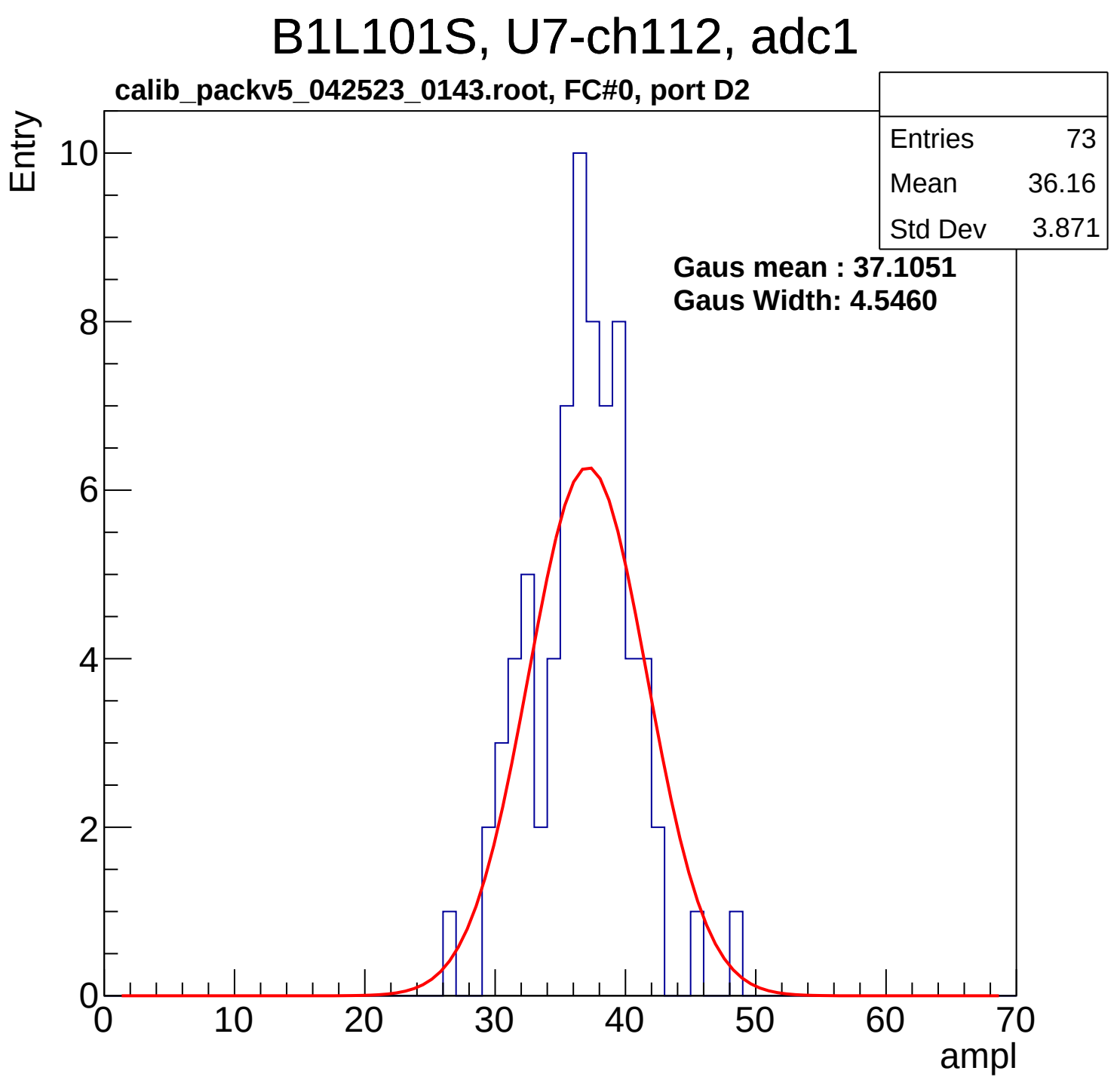
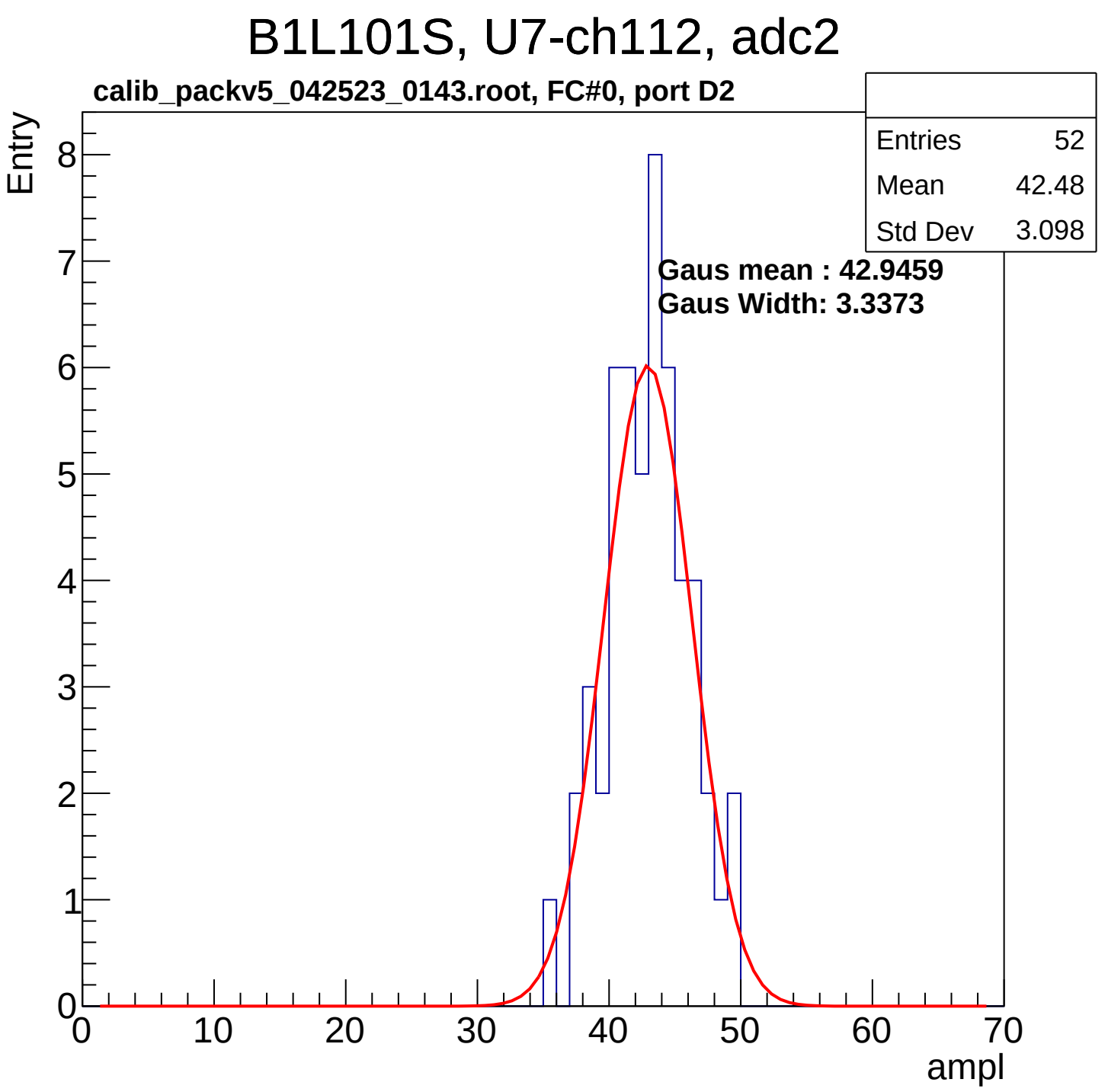

B1L101S, U7-ch111, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 34
Mean 58.44
Std Dev 10.37
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

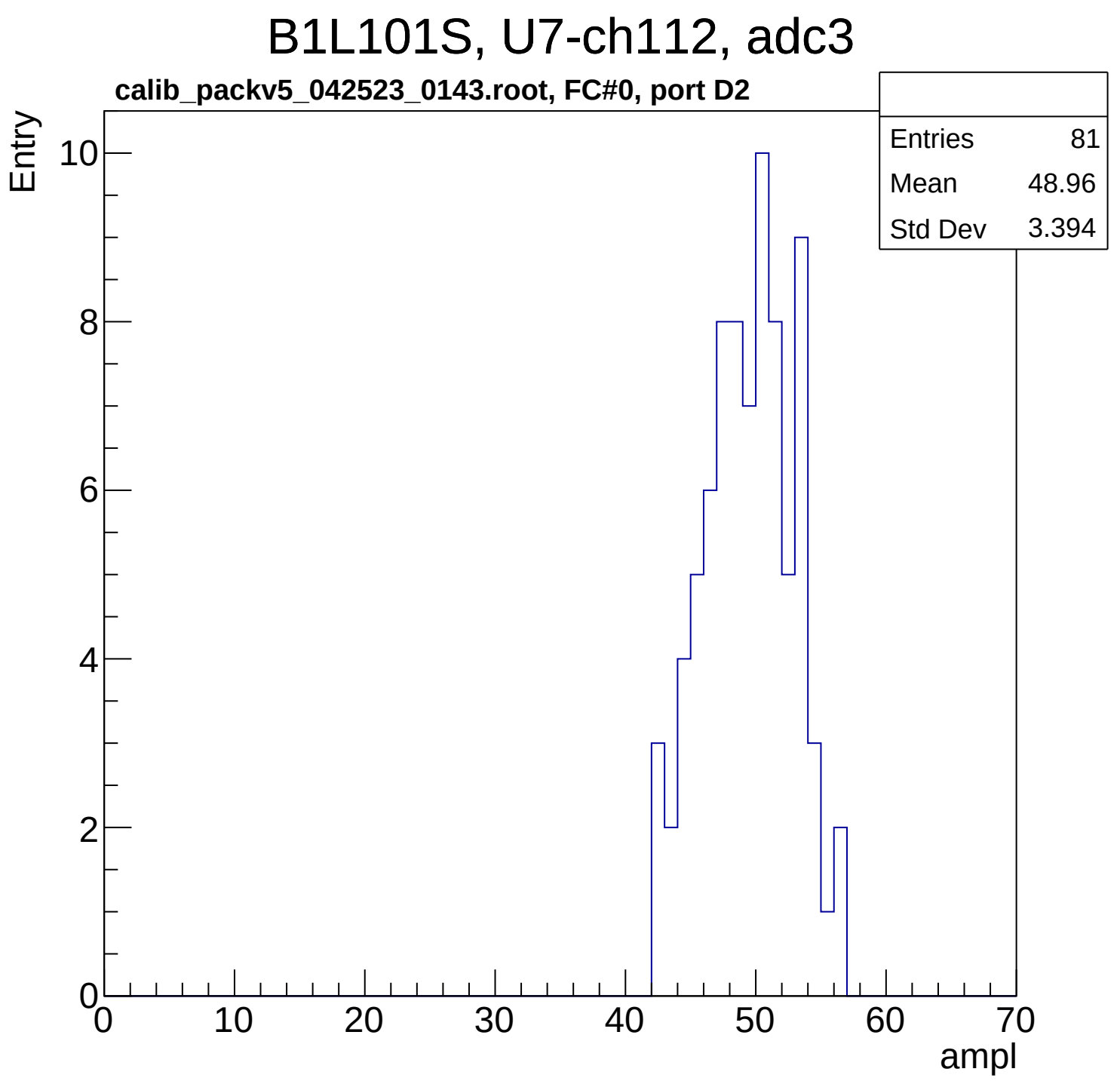

B1L101S, U7-ch111, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 62.5
Std Dev 0.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

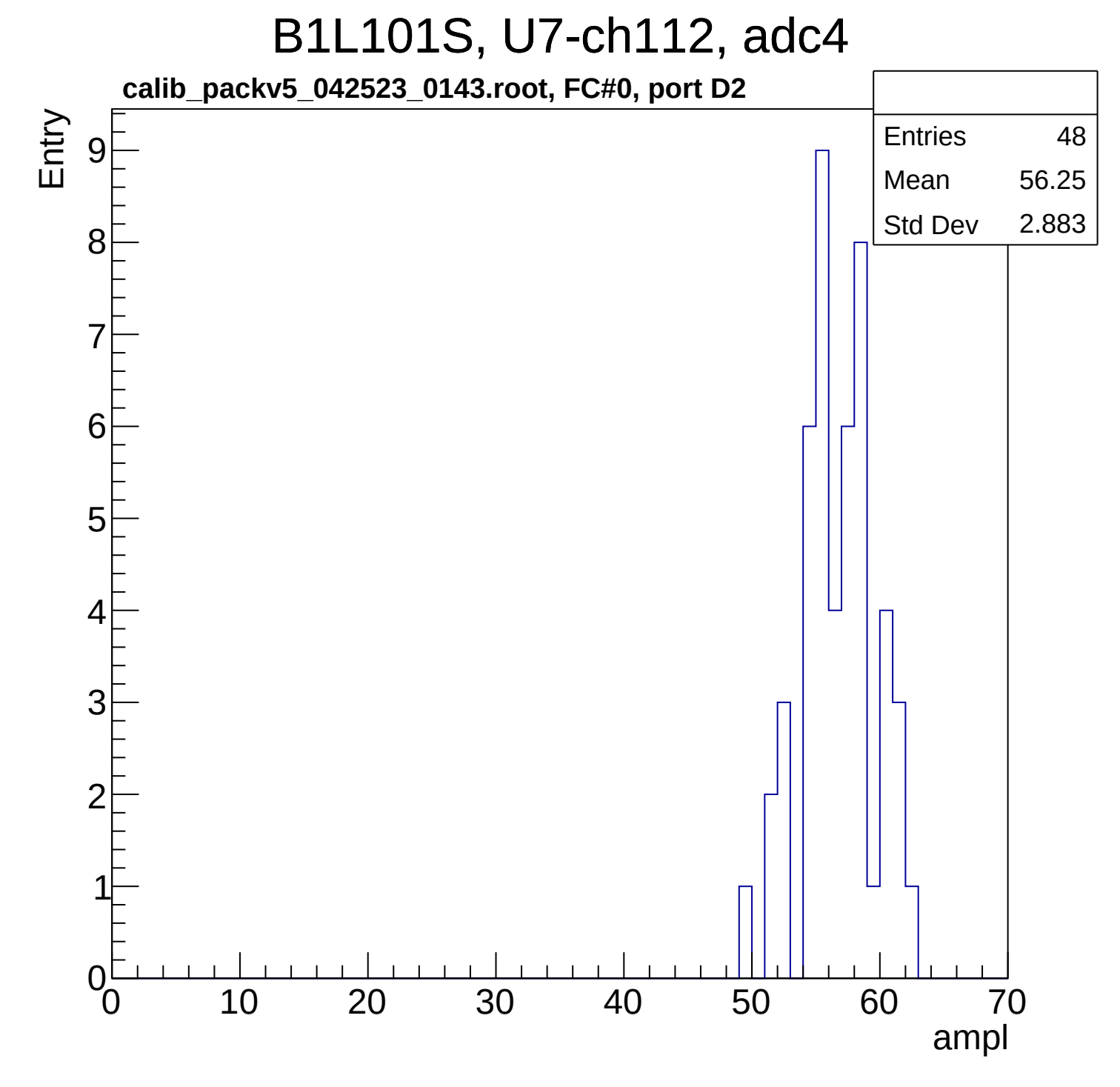

B1L101S, U7-ch111, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

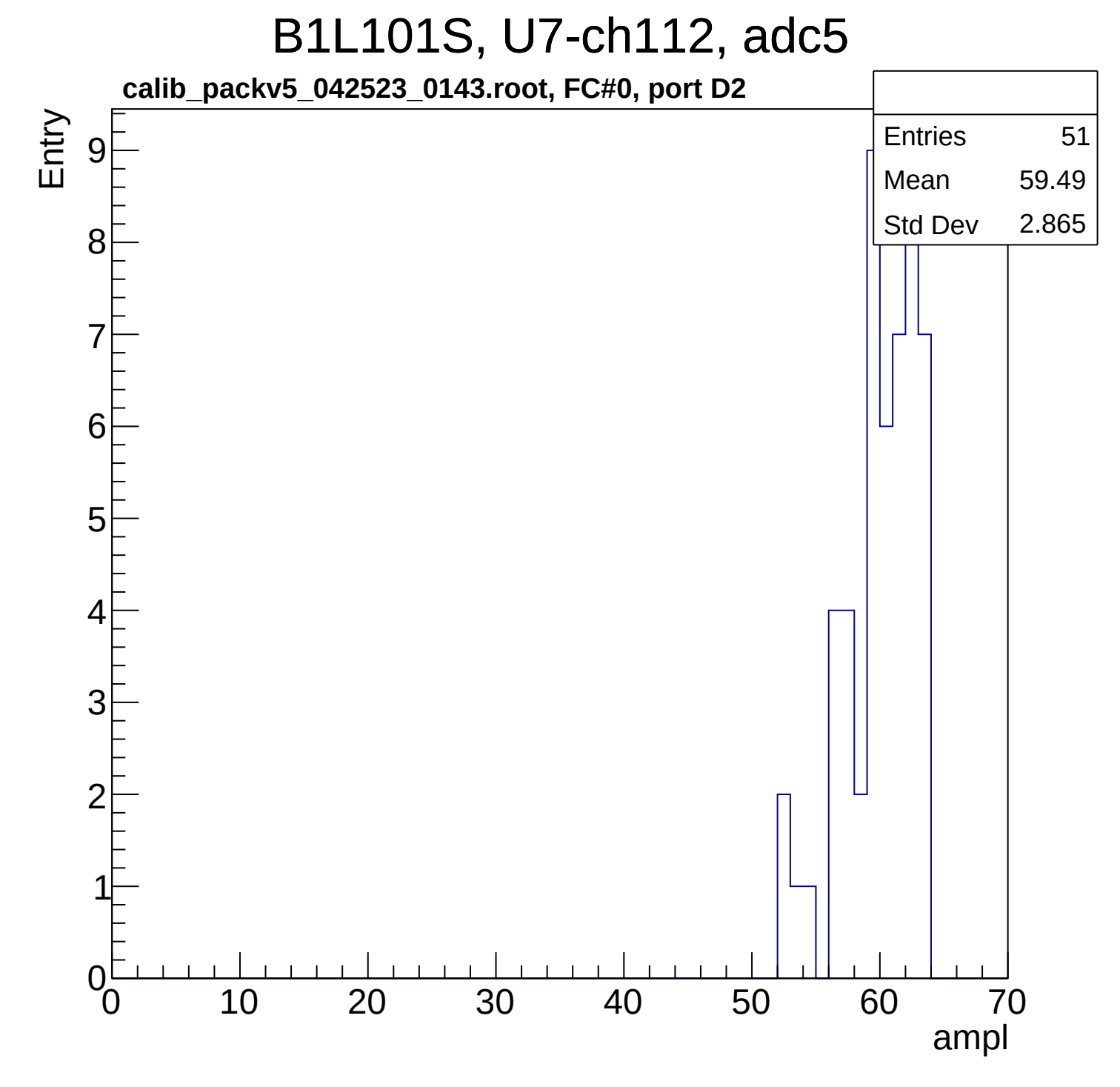

B1L101S, U7-ch112, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 29.03
Std Dev 6.113
Gaus mean : 30.6939
Gaus Width: 3.7397
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

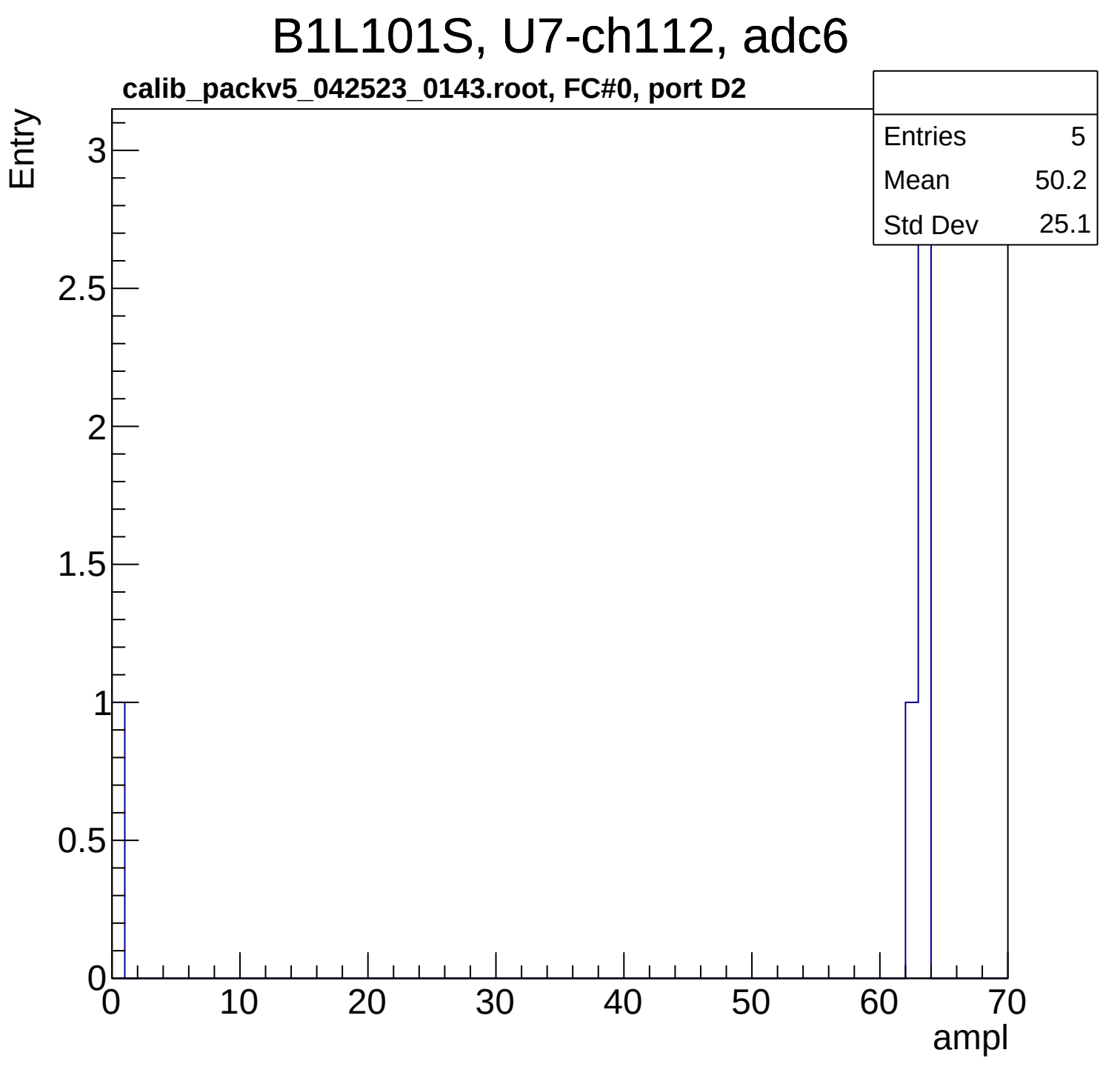

B1L101S, U7-ch112, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 36.16
Std Dev 3.871
Gaus mean : 37.1051
Gaus Width: 4.5460
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

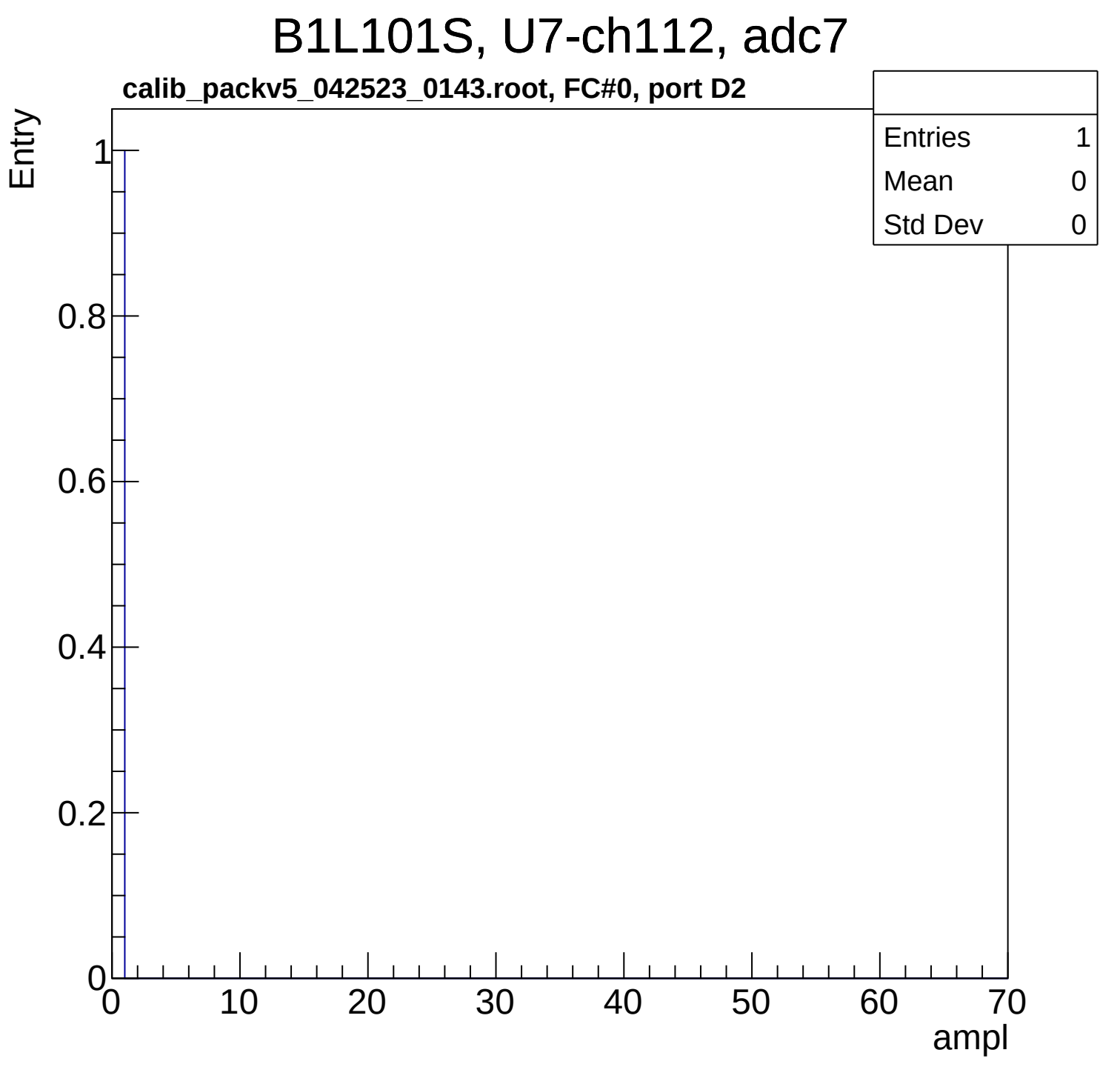

B1L101S, U7-ch112, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 42.48
Std Dev 3.098
Gaus mean : 42.9459
Gaus Width: 3.3373
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

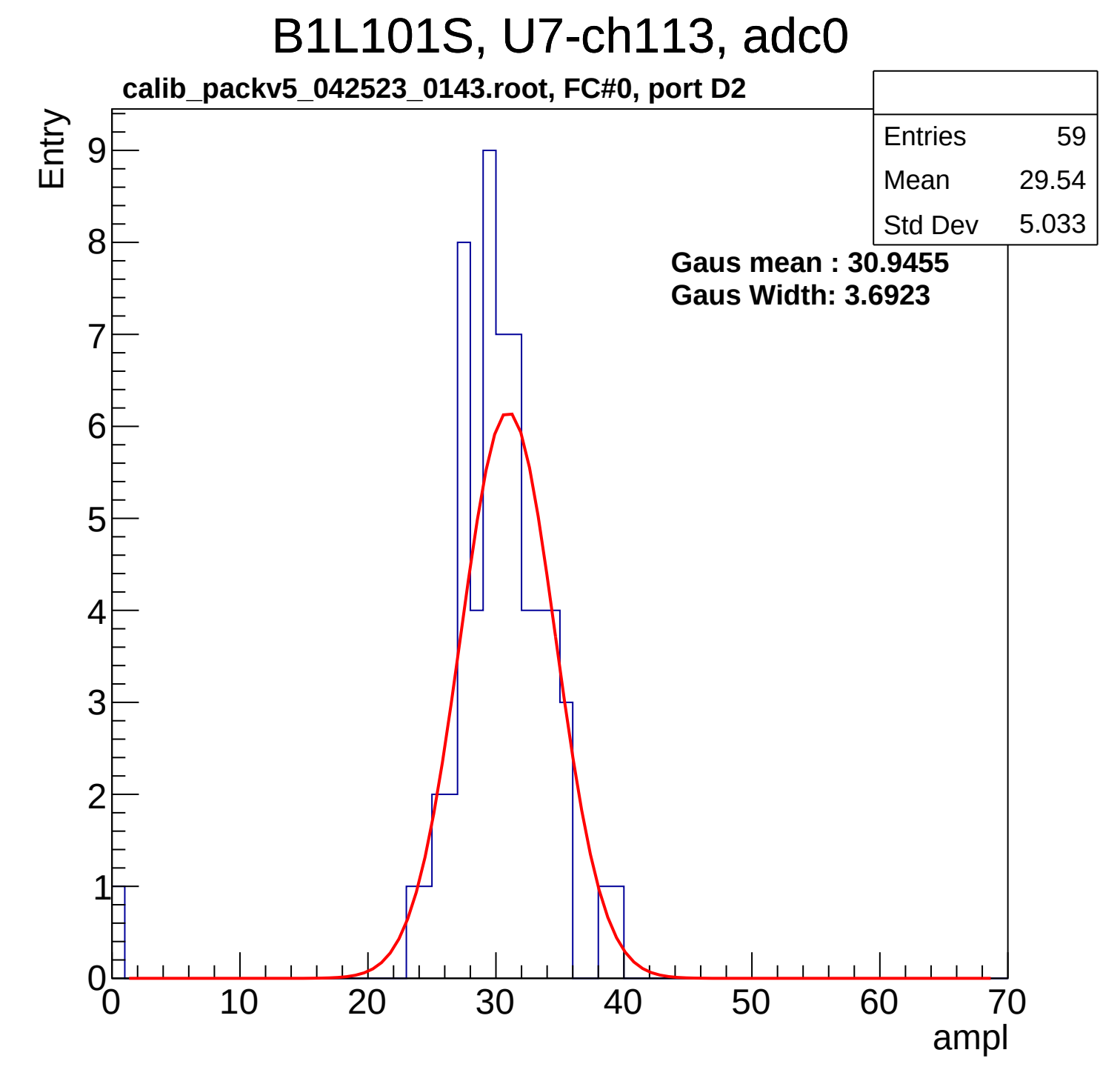

B1L101S, U7-ch112, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 81
Mean 48.96
Std Dev 3.394
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

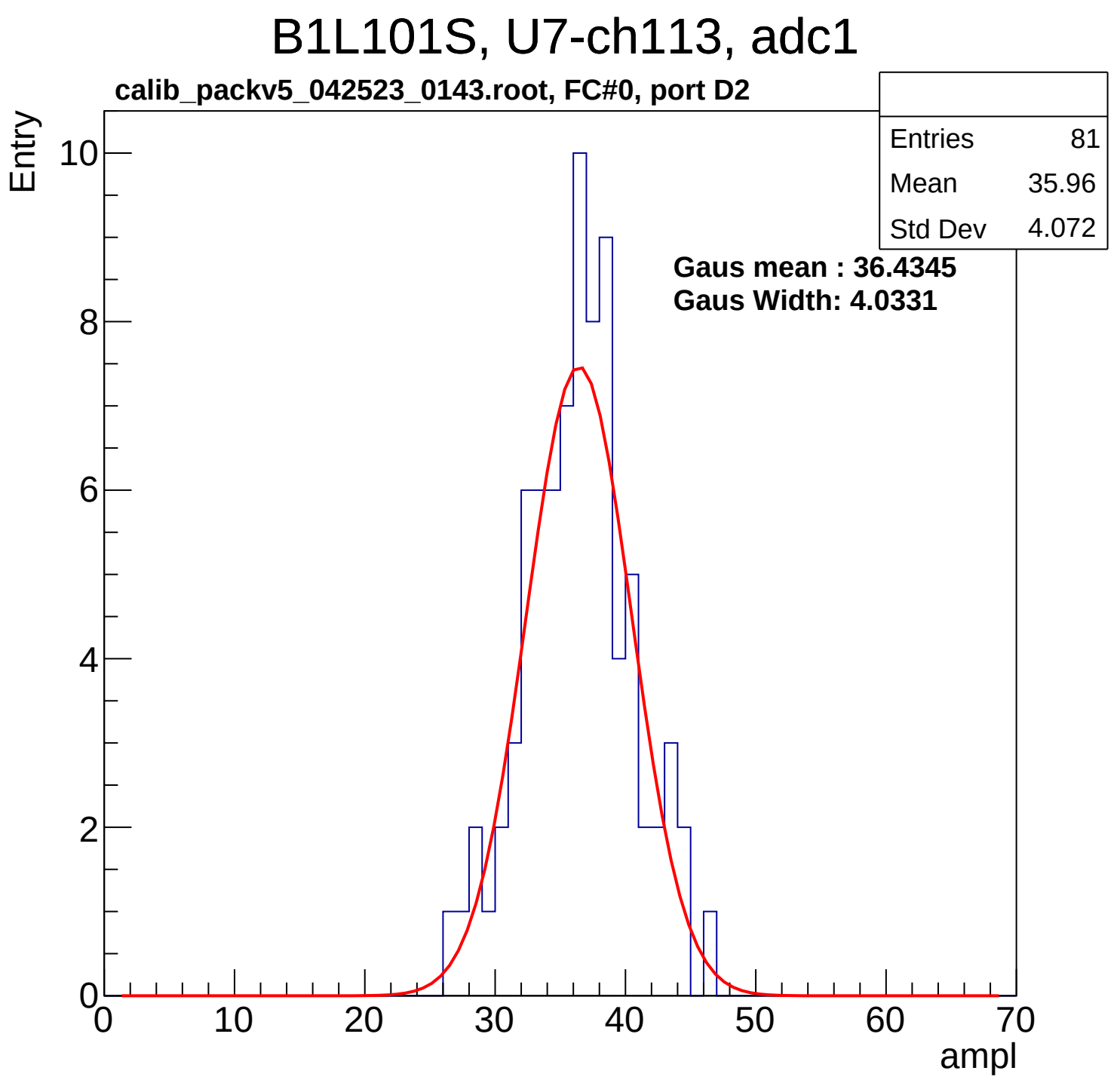

B1L101S, U7-ch112, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 56.25
Std Dev 2.883
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

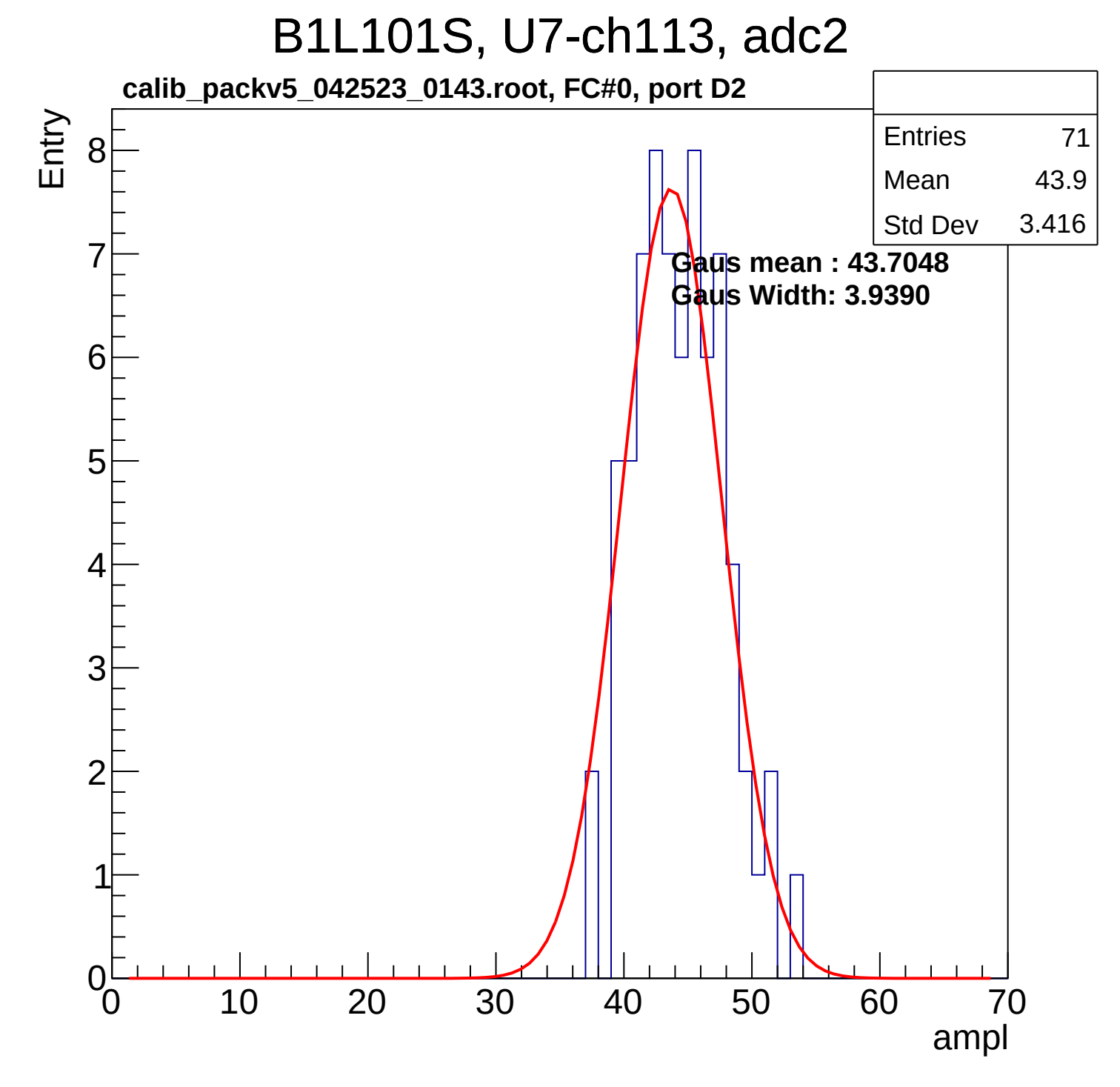

B1L101S, U7-ch112, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 59.49
Std Dev 2.865
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

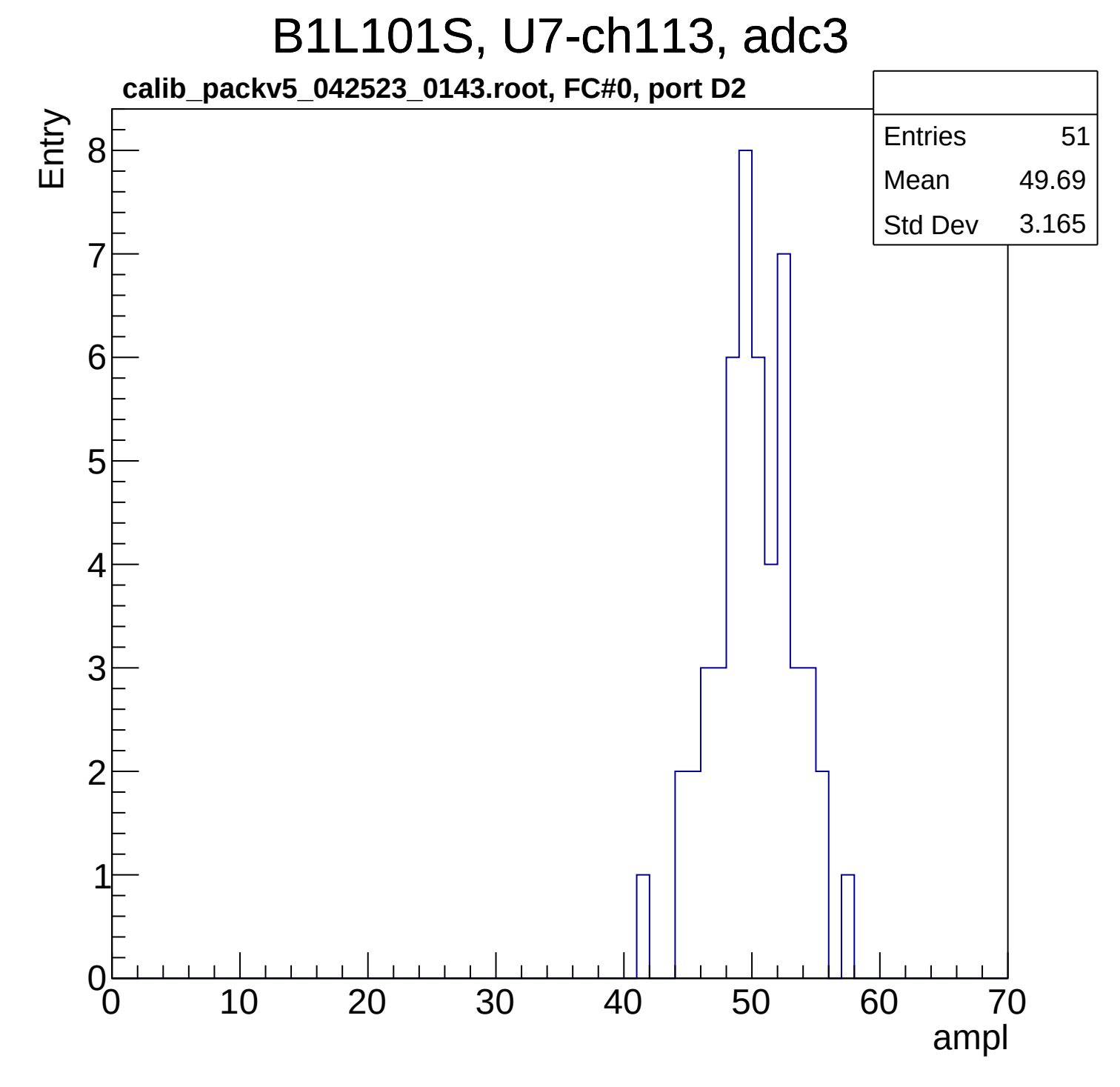

B1L101S, U7-ch112, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 50.2
Std Dev 25.1
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

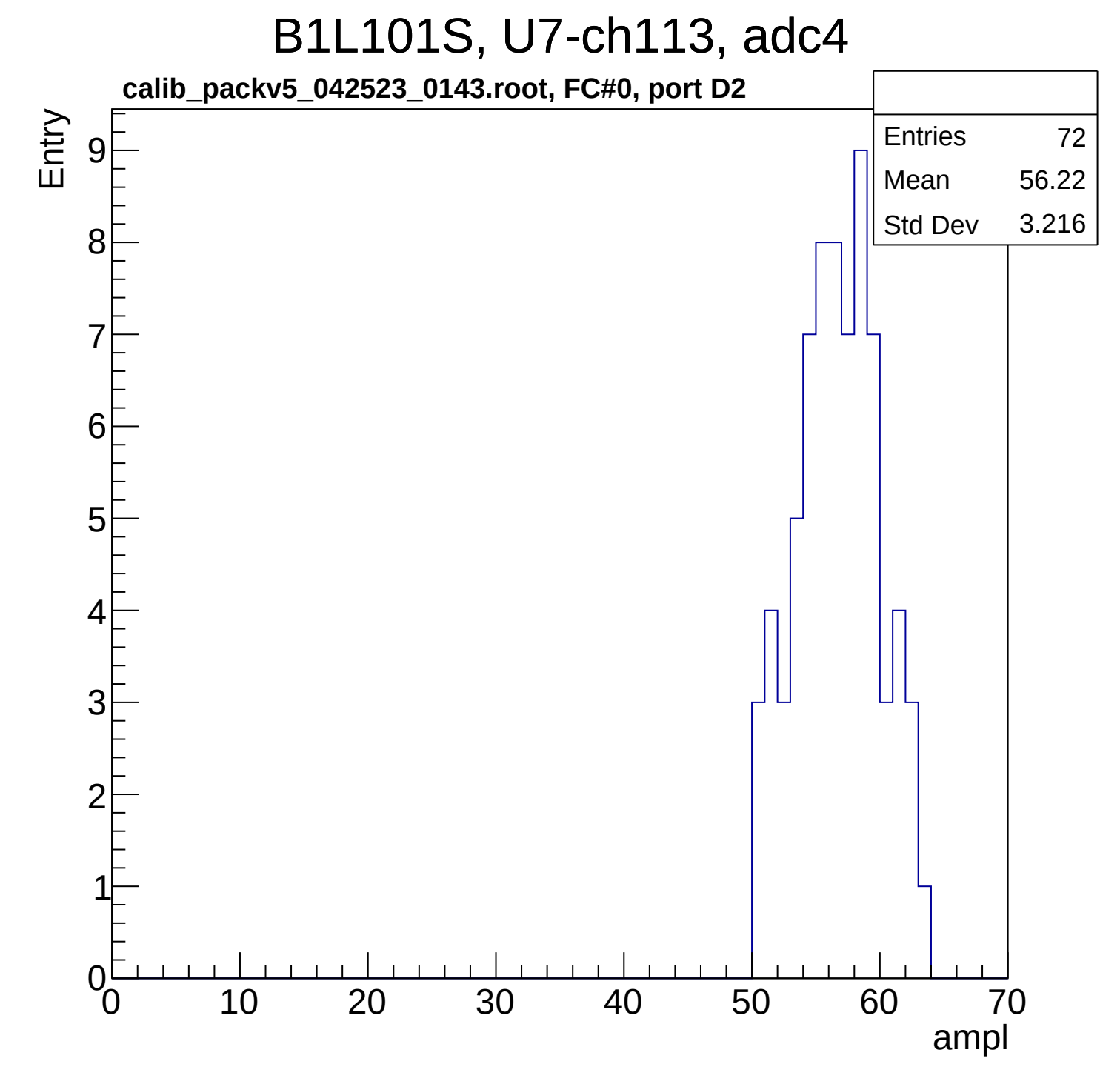

B1L101S, U7-ch112, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch113, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 29.54
Std Dev 5.033
Gaus mean : 30.9455
Gaus Width: 3.6923
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch113, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 81
Mean 35.96
Std Dev 4.072
Gaus mean : 36.4345
Gaus Width: 4.0331
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch113, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 43.9
Std Dev 3.416
Gaus mean : 43.7048
Gaus Width: 3.9390
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch113, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 49.69
Std Dev 3.165
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch113, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 56.22
Std Dev 3.216
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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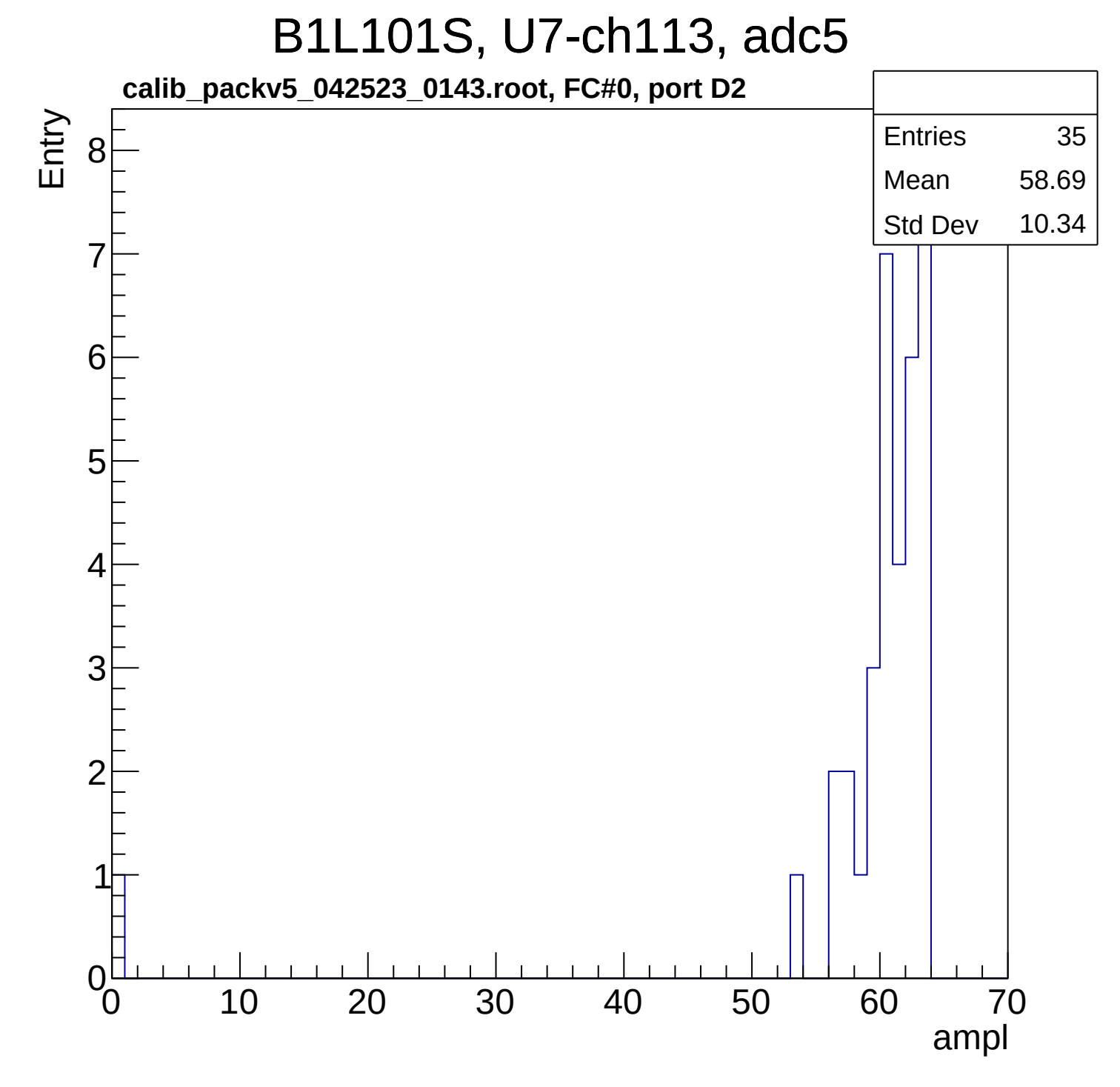
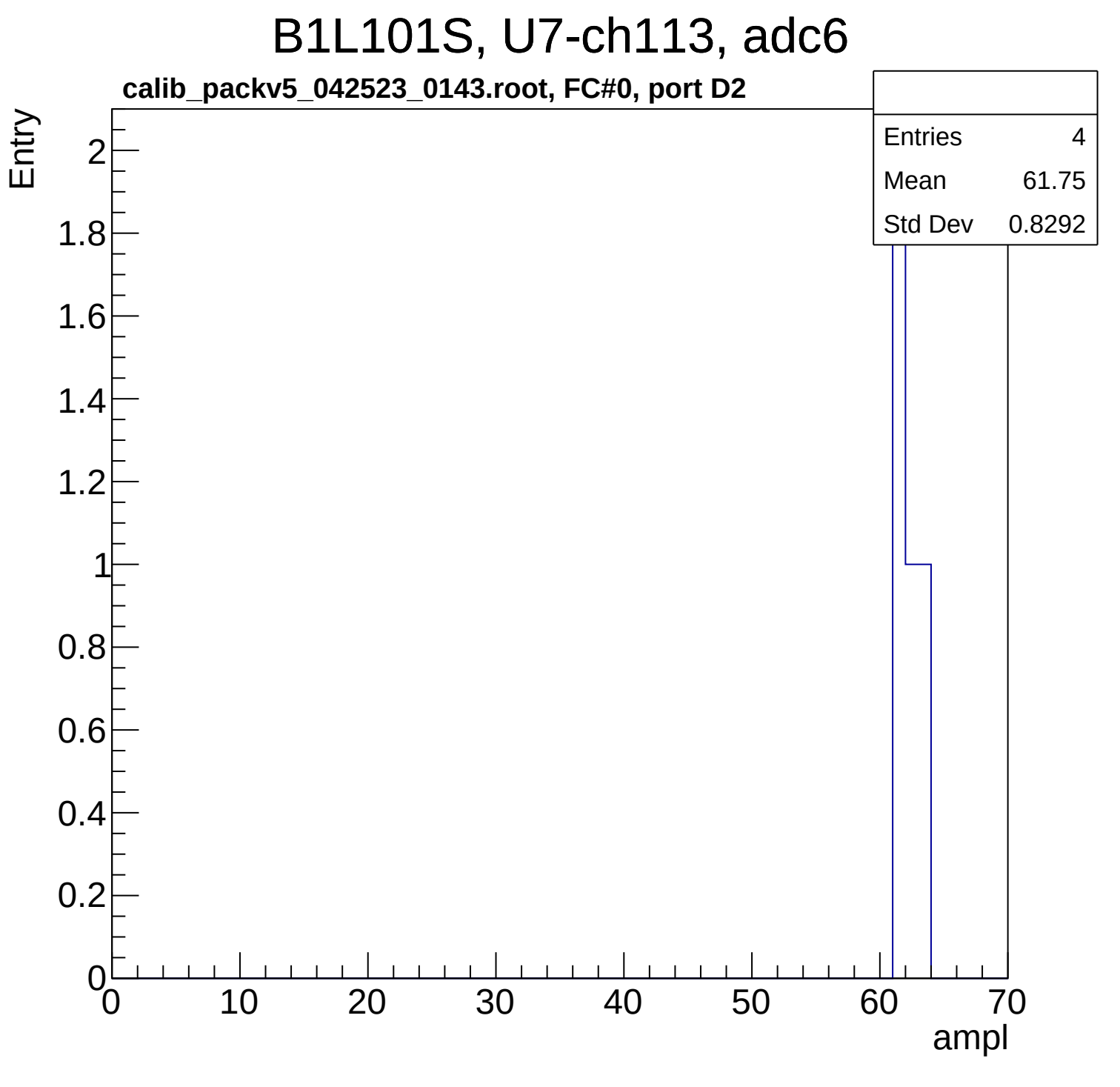
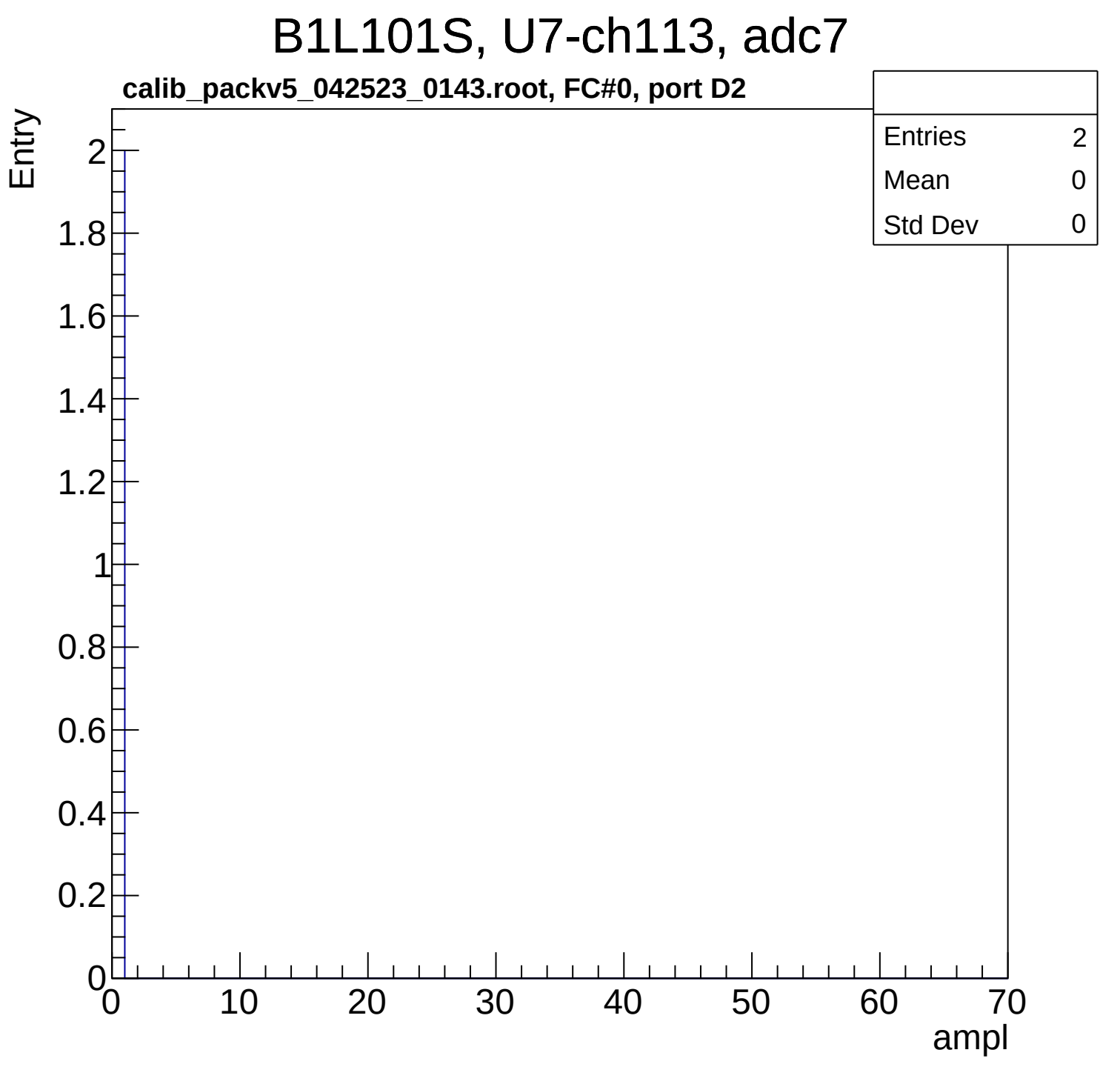
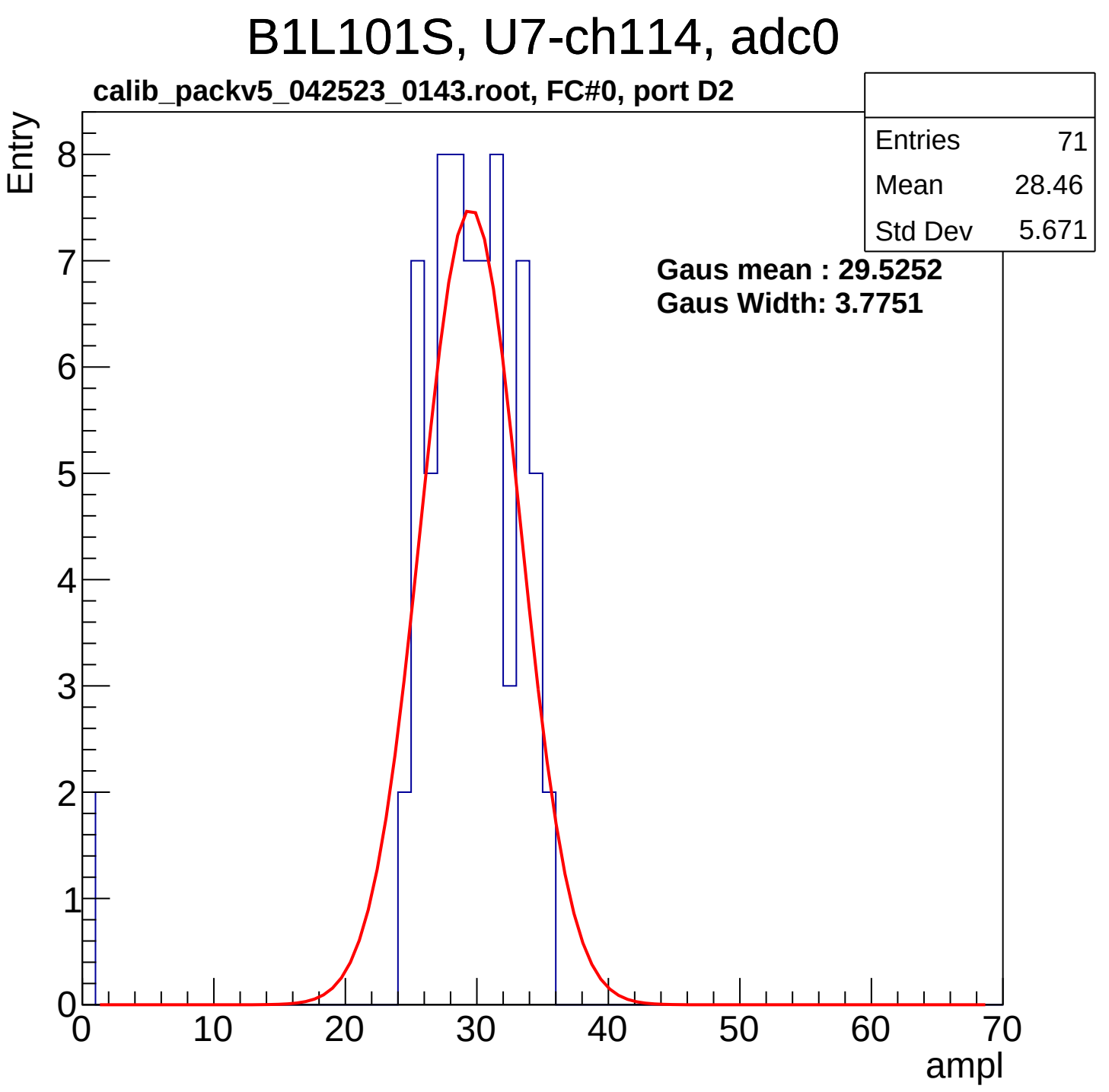
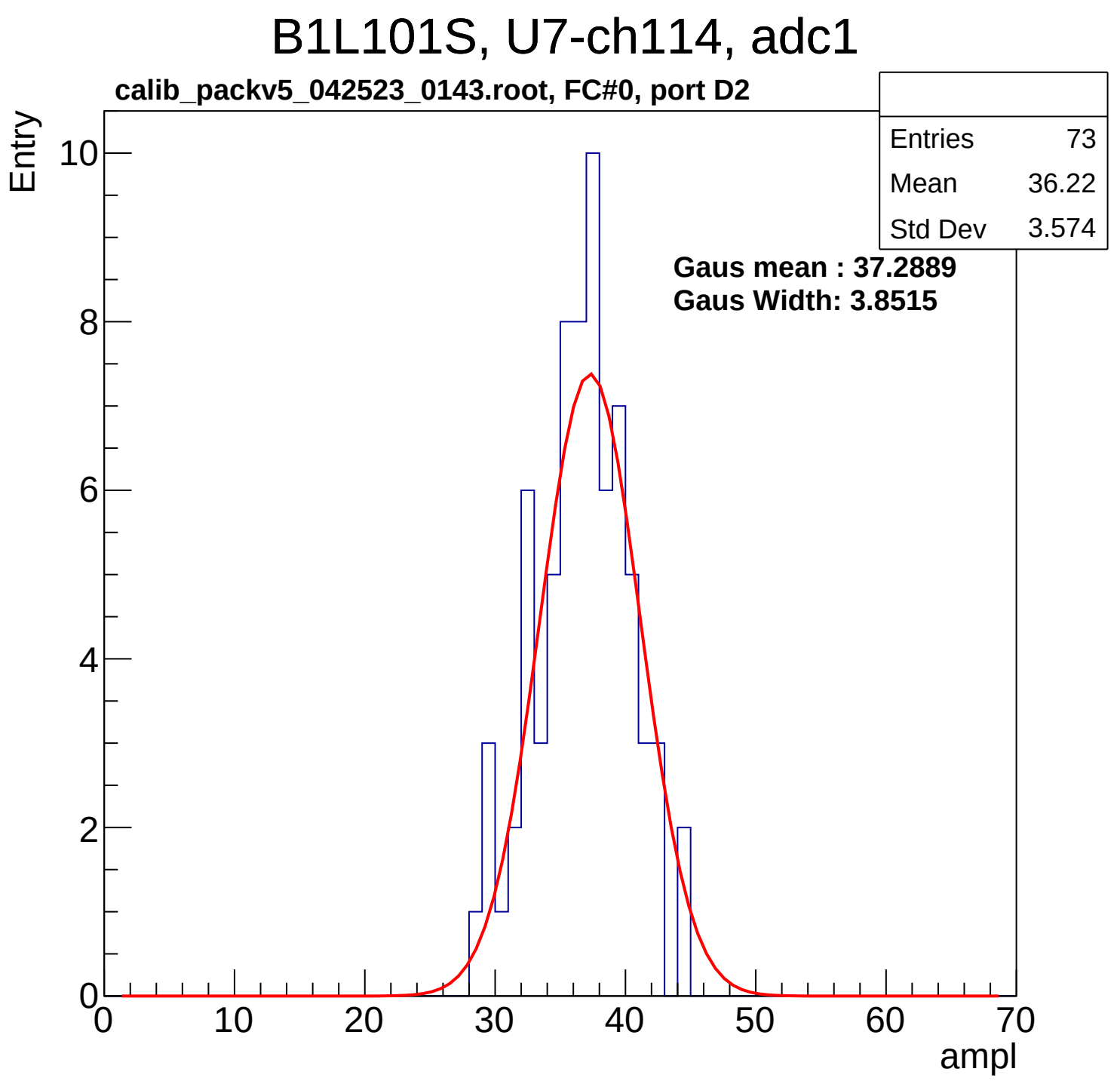
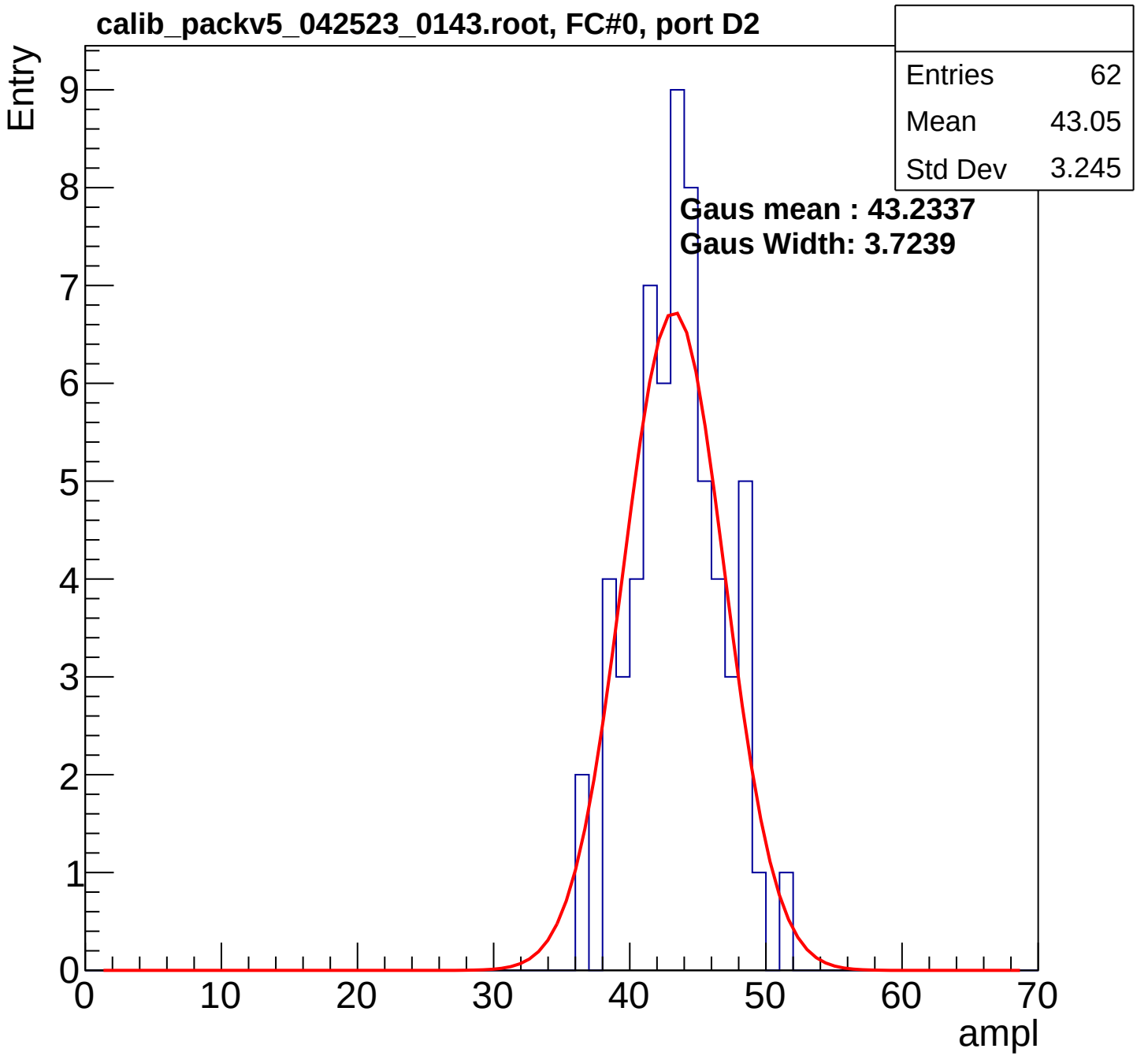

B1L101S, U7-ch113, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 35
Mean 58.69
Std Dev 10.34
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

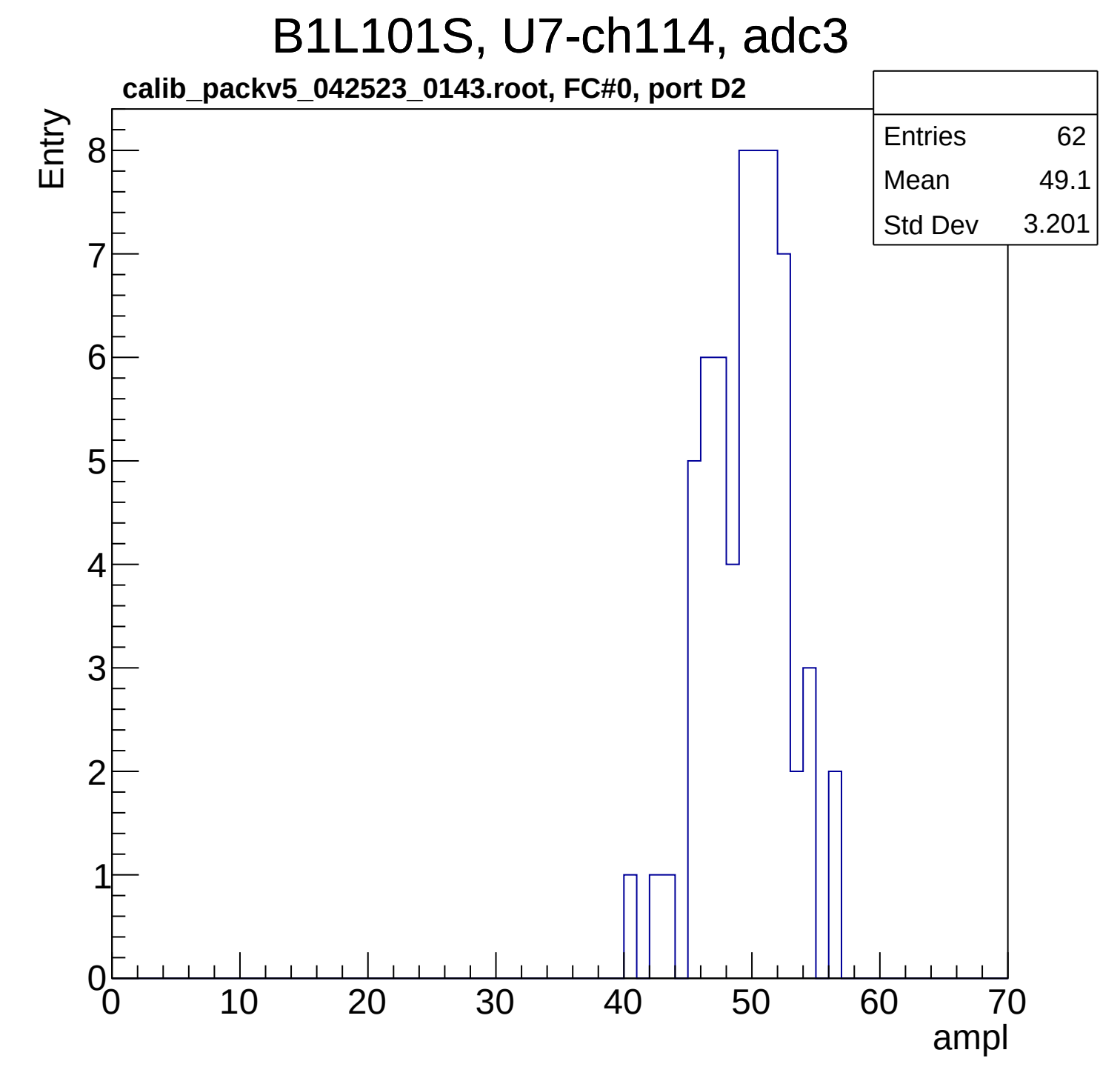

B1L101S, U7-ch113, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 61.75
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U7-ch113, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch114, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 28.46
Std Dev 5.671
Gaus mean : 29.5252
Gaus Width: 3.7751
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch114, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 36.22
Std Dev 3.574
Gaus mean : 37.2889
Gaus Width: 3.8515
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch114, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 43.05
Std Dev 3.245
Gaus mean : 43.2337
Gaus Width: 3.7239
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L101S, U7-ch114, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 49.1
Std Dev 3.201
Entry
ampl
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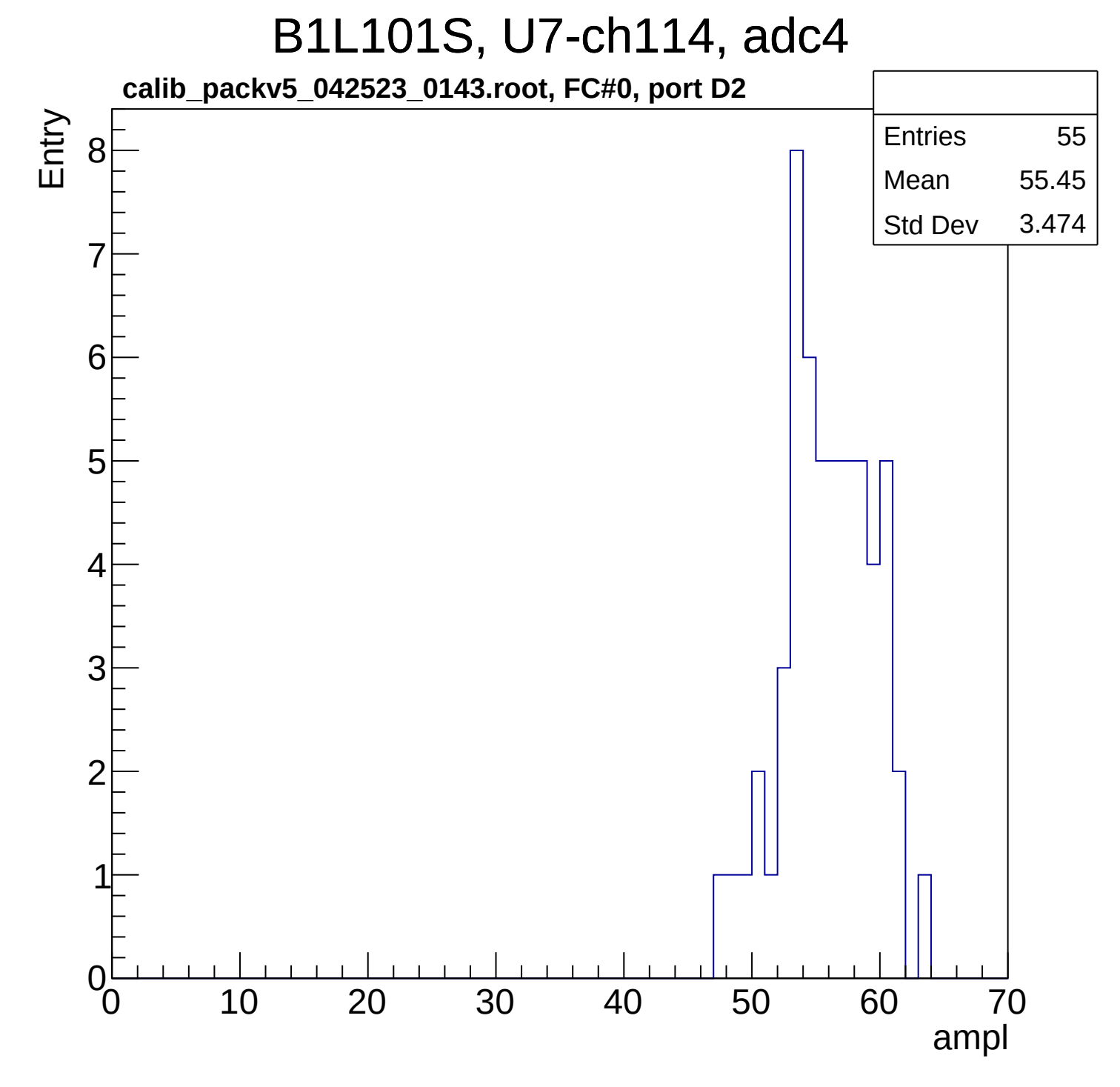
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch114, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 55.45
Std Dev 3.474
Entry
ampl
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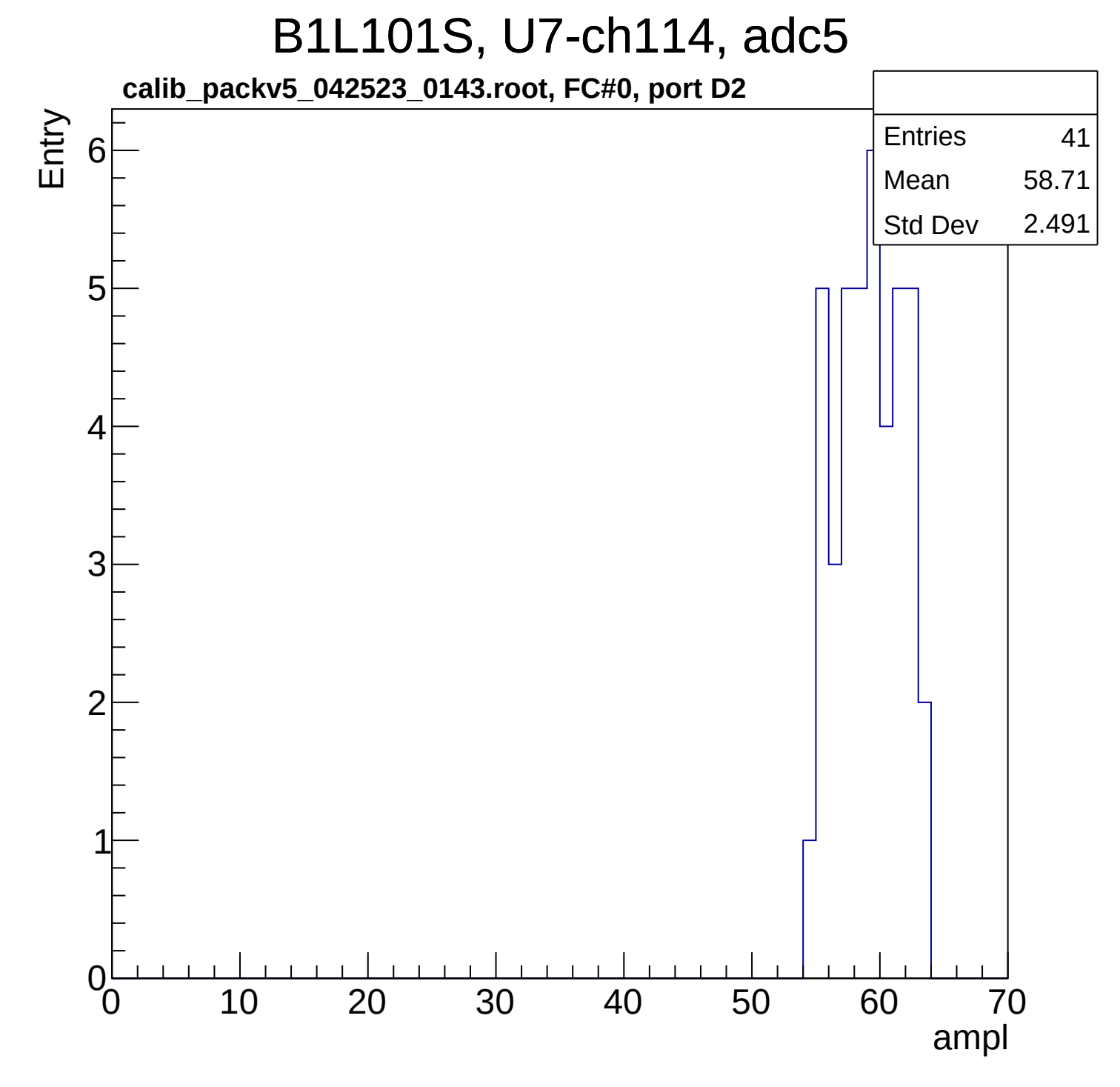
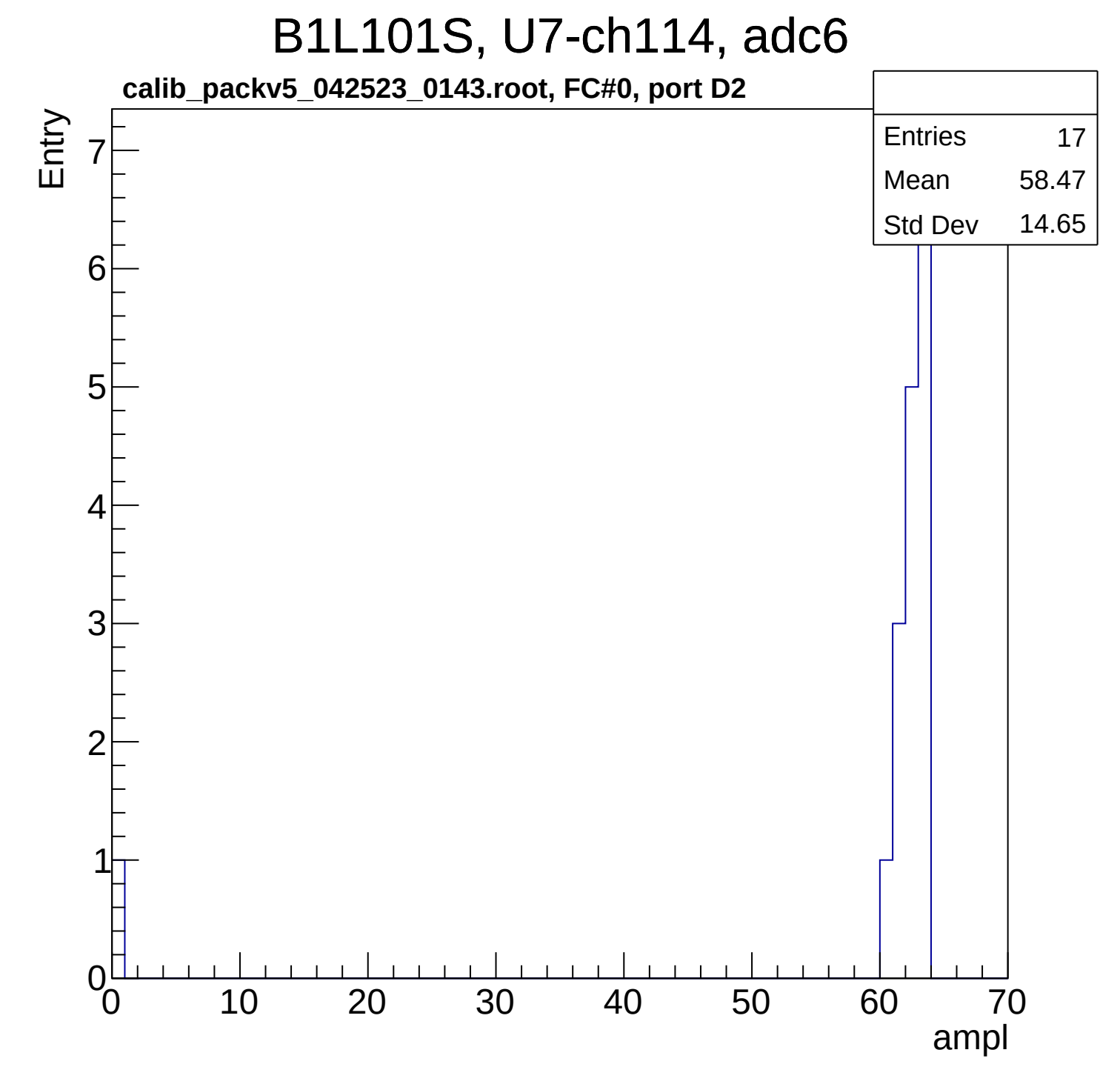
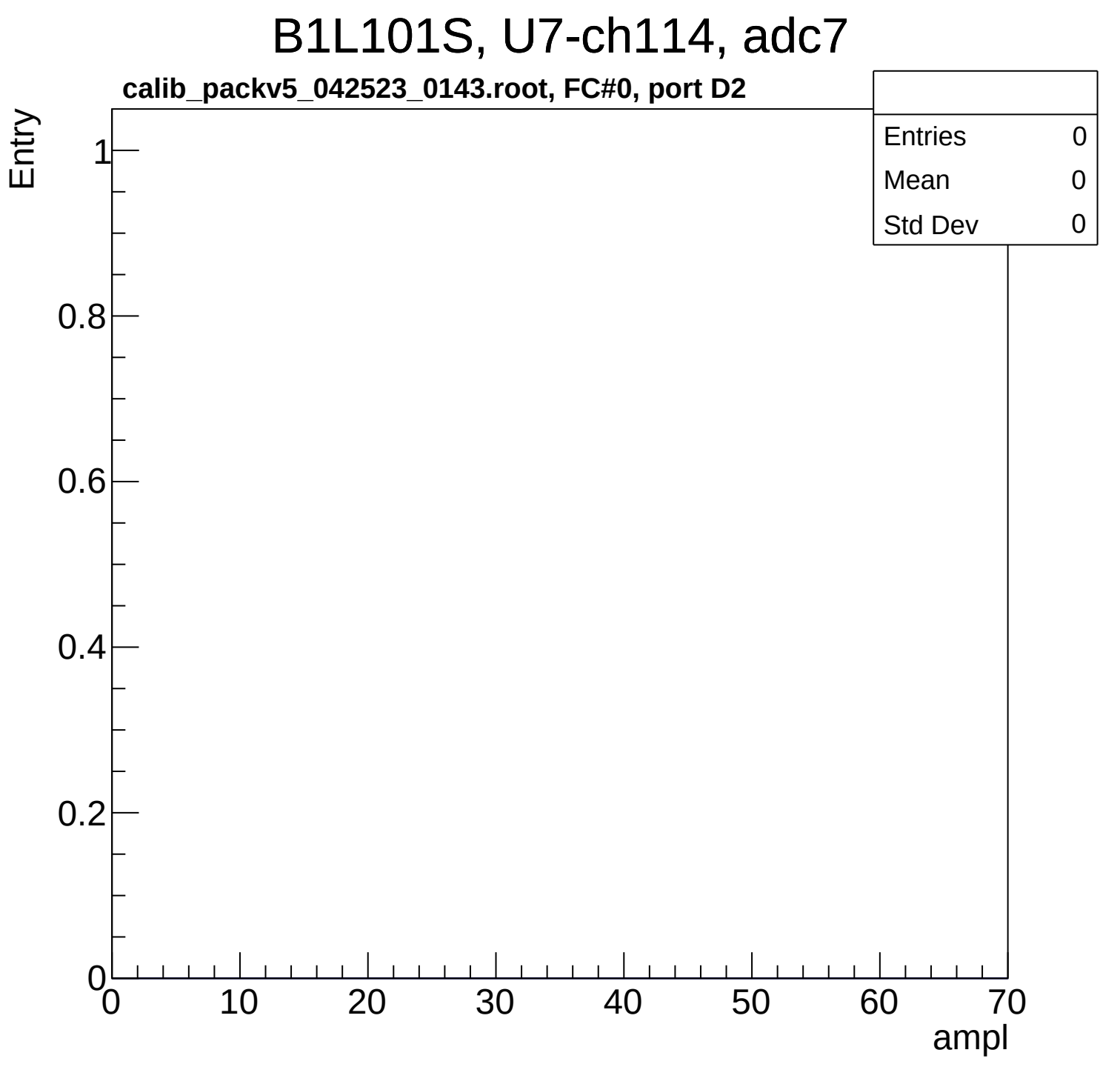
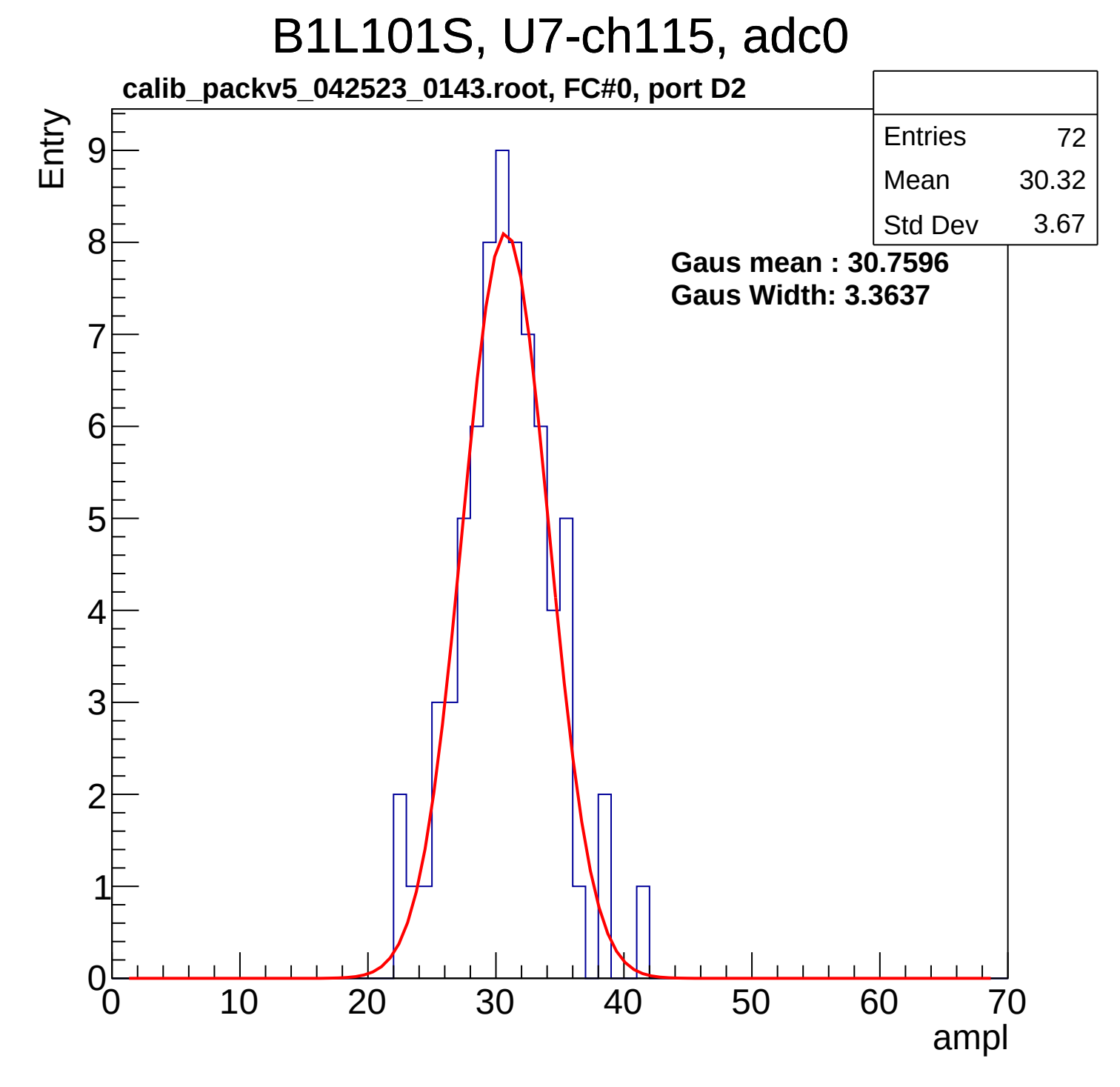
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch114, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 41
Mean 58.71
Std Dev 2.491
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L101S, U7-ch114, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 17
Mean 58.47
Std Dev 14.65
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch114, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch115, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 30.32
Std Dev 3.67
Gaus mean : 30.7596
Gaus Width: 3.3637
Entry
ampl
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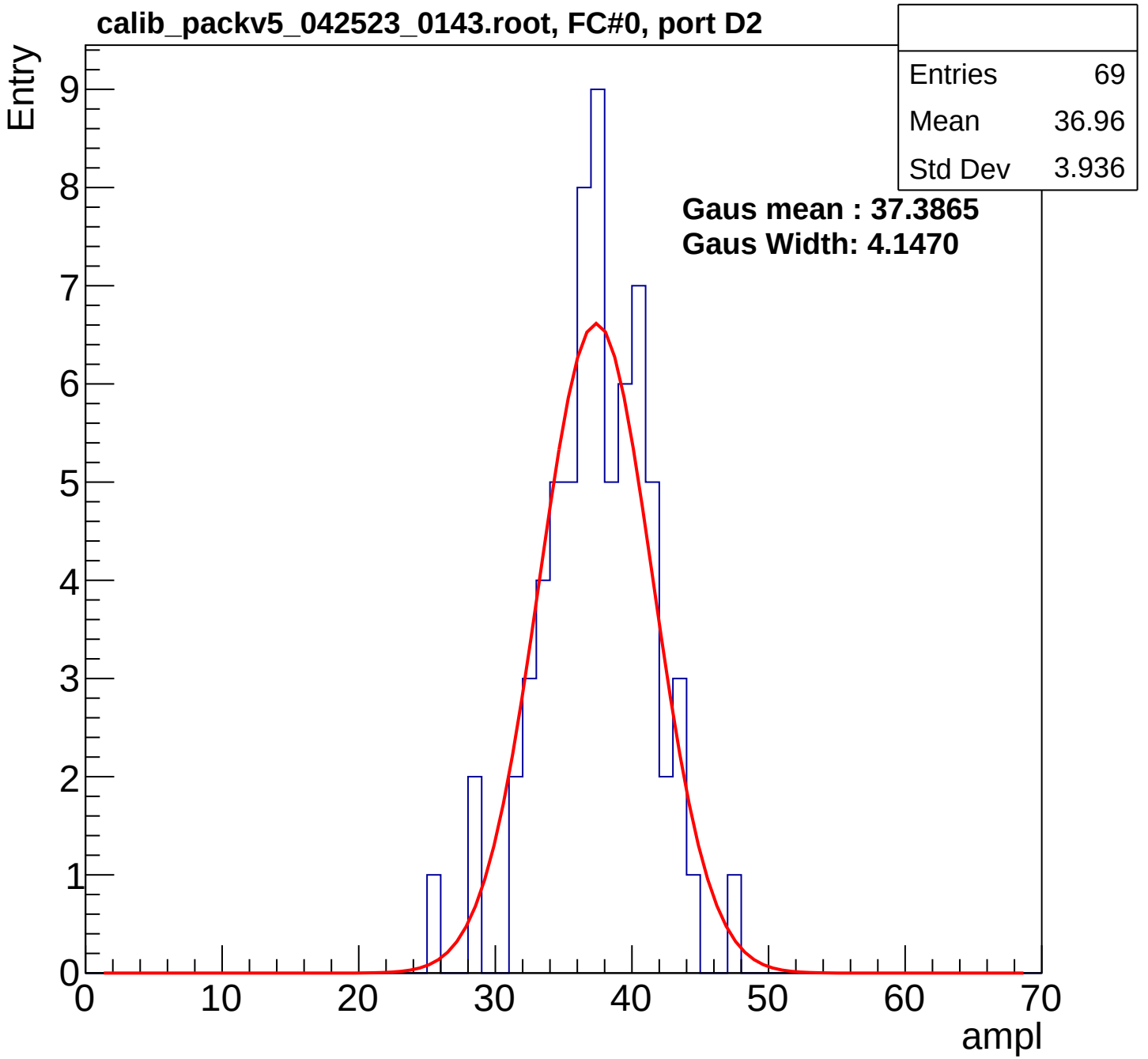
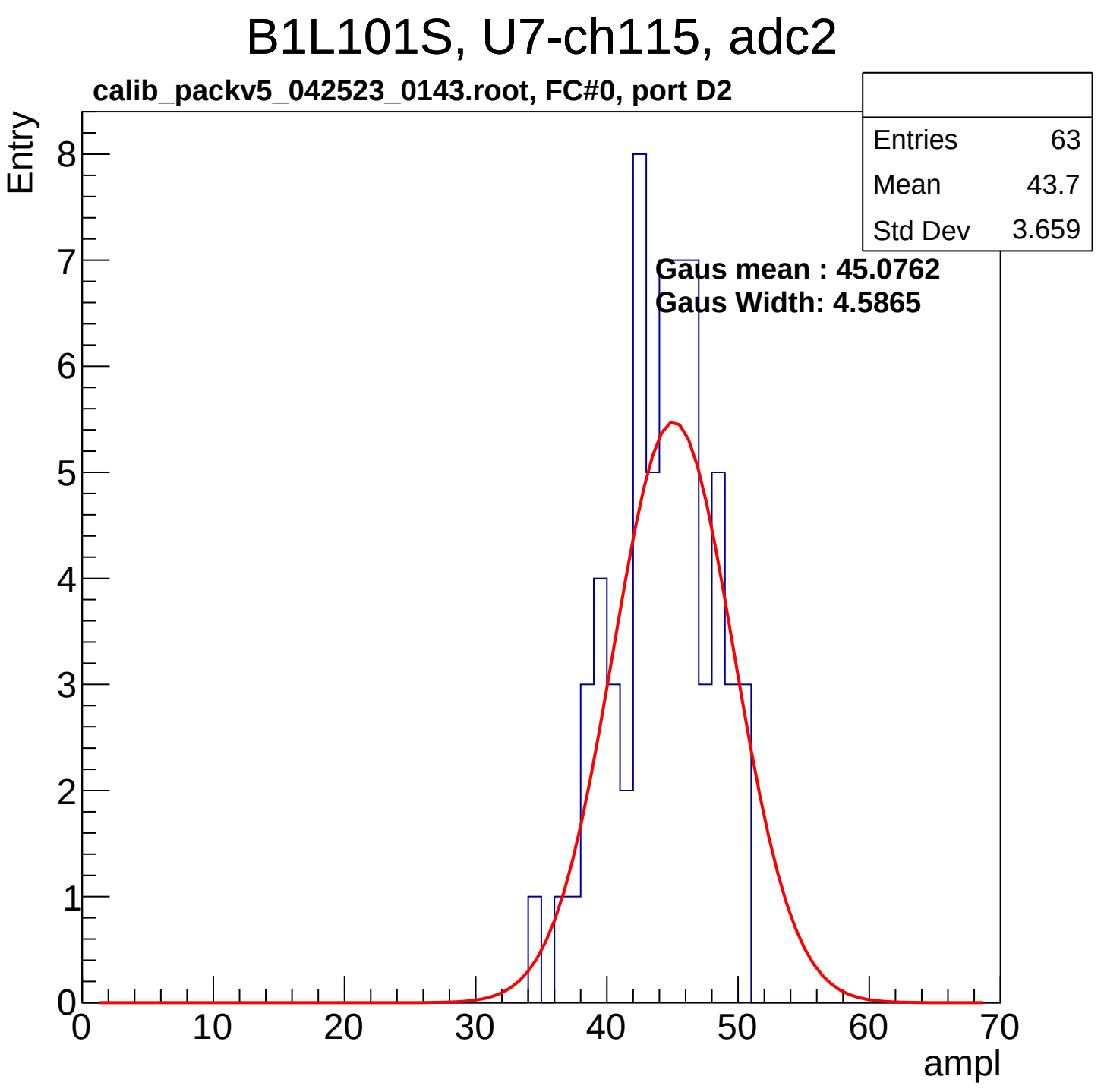
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch115, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 36.96
Std Dev 3.936
Gaus mean : 37.3865
Gaus Width: 4.1470
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch115, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 43.7
Std Dev 3.659
Gaus mean : 45.0762
Gaus Width: 4.5865
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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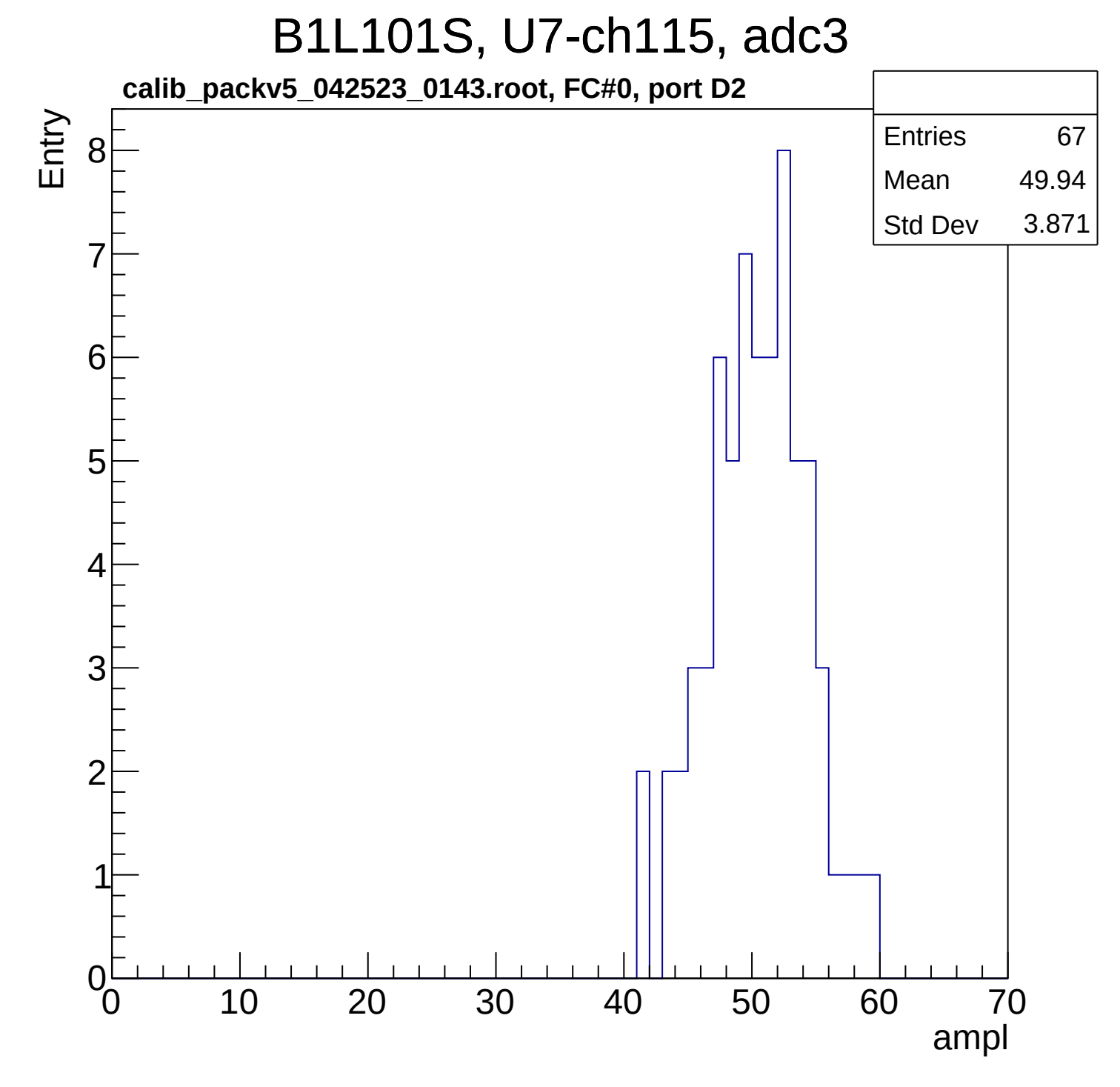
B1L101S, U7-ch115, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 49.94
Std Dev 3.871
Entry
ampl
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2
3
4
5
6
7
8
0
10
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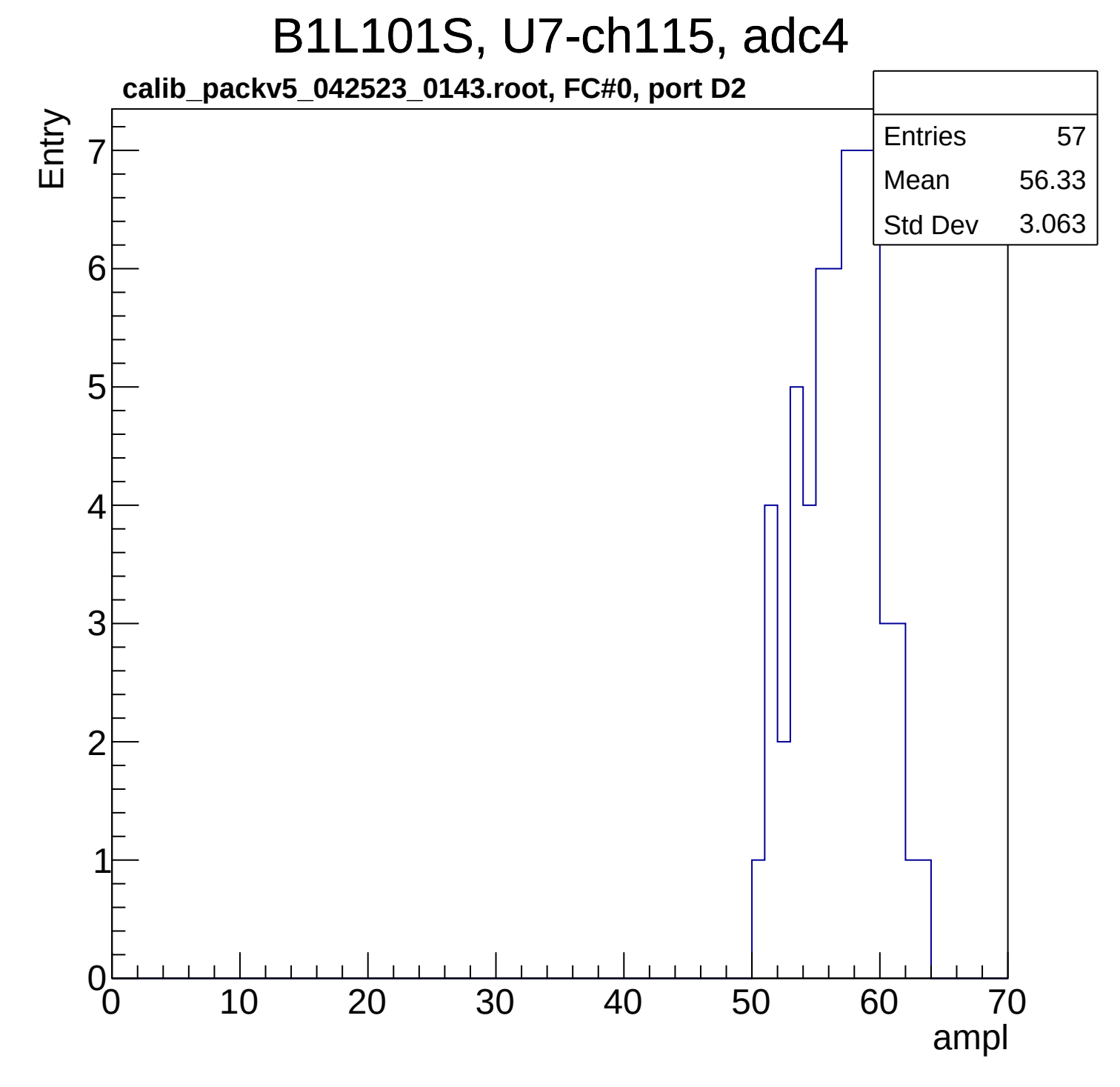
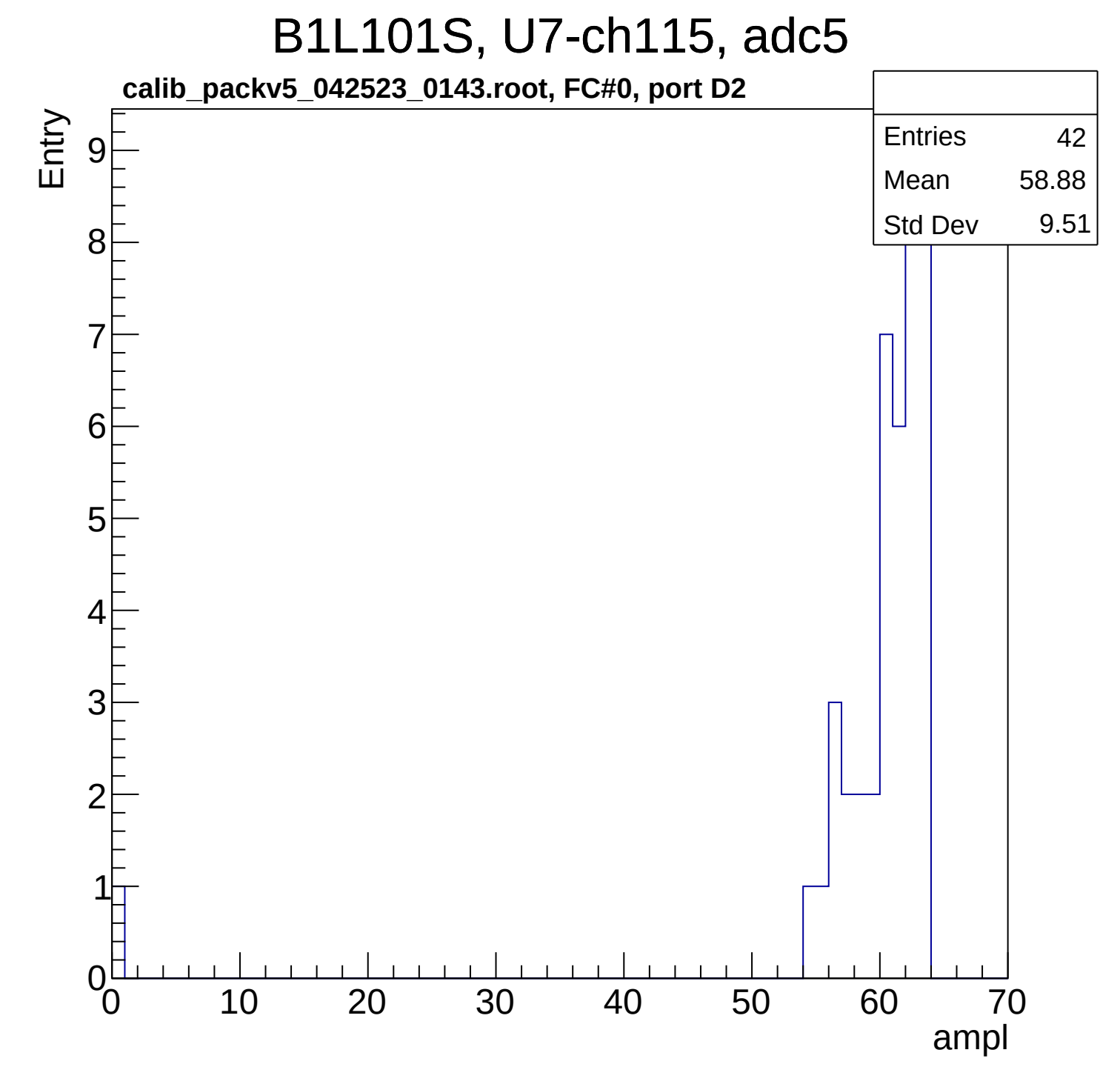
50
60
70


B1L101S, U7-ch115, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 56.33
Std Dev 3.063
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U7-ch115, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 58.88
Std Dev 9.51
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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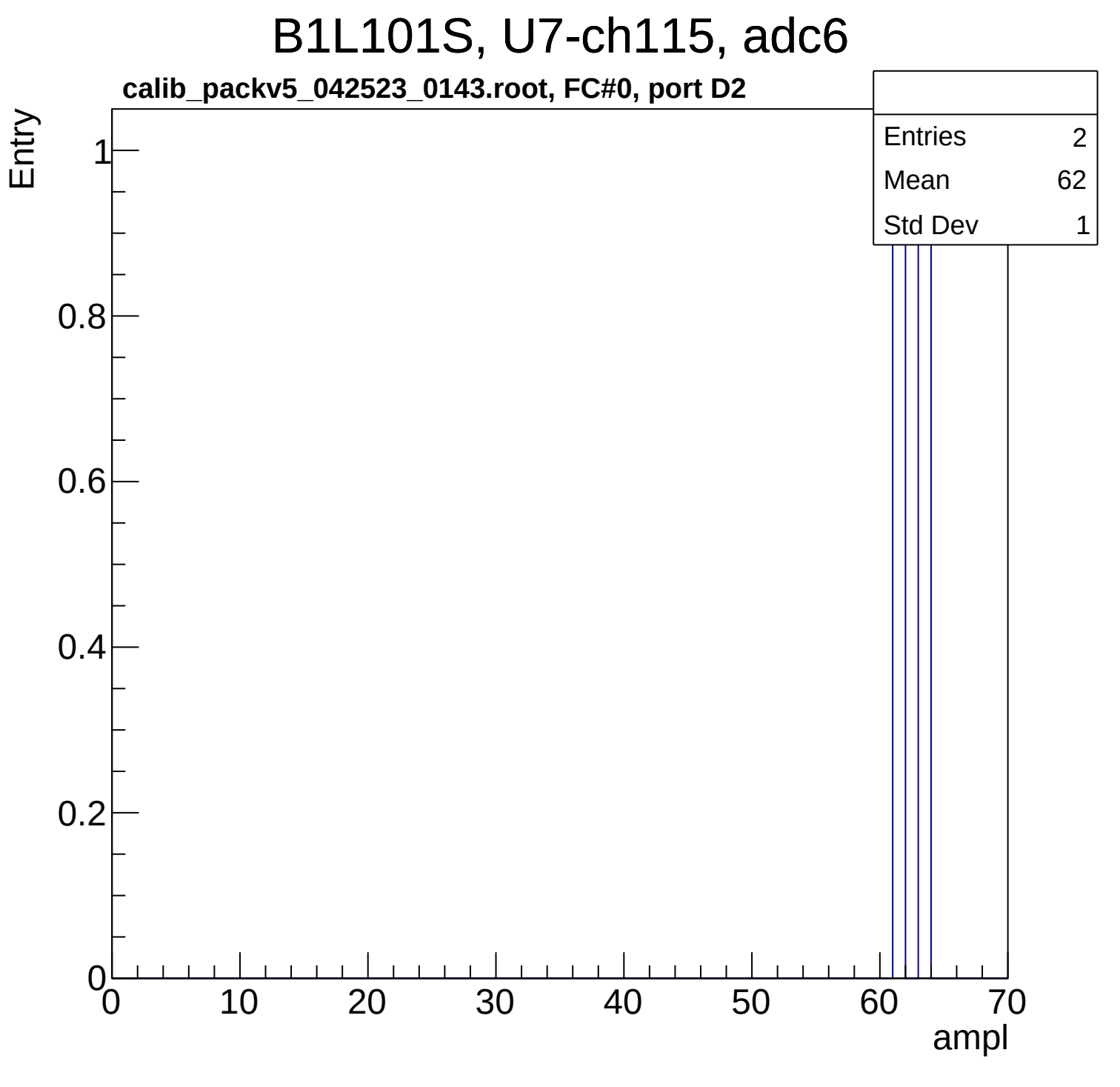
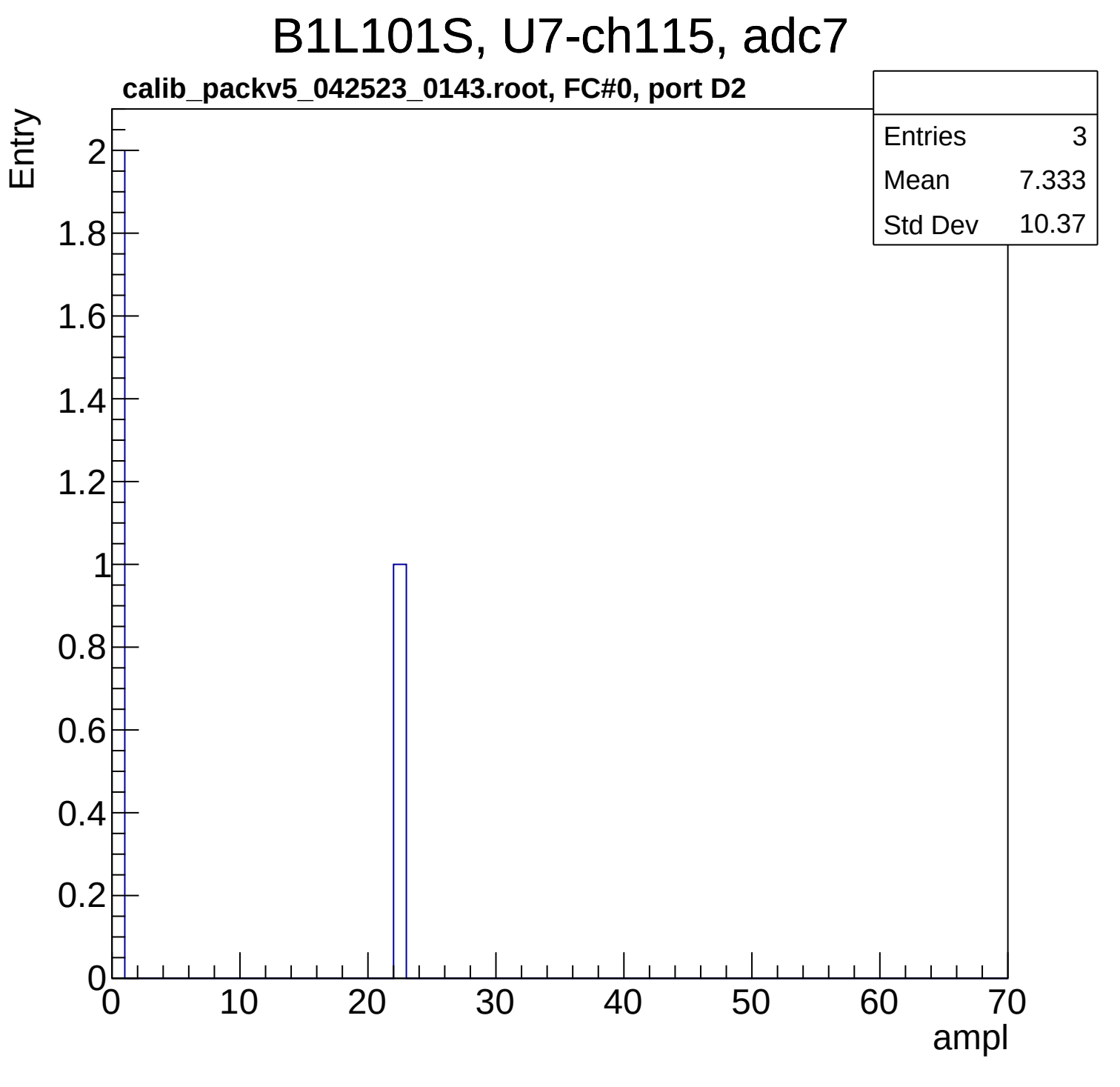

B1L101S, U7-ch115, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 62
Std Dev 1
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch115, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 7.333
Std Dev 10.37
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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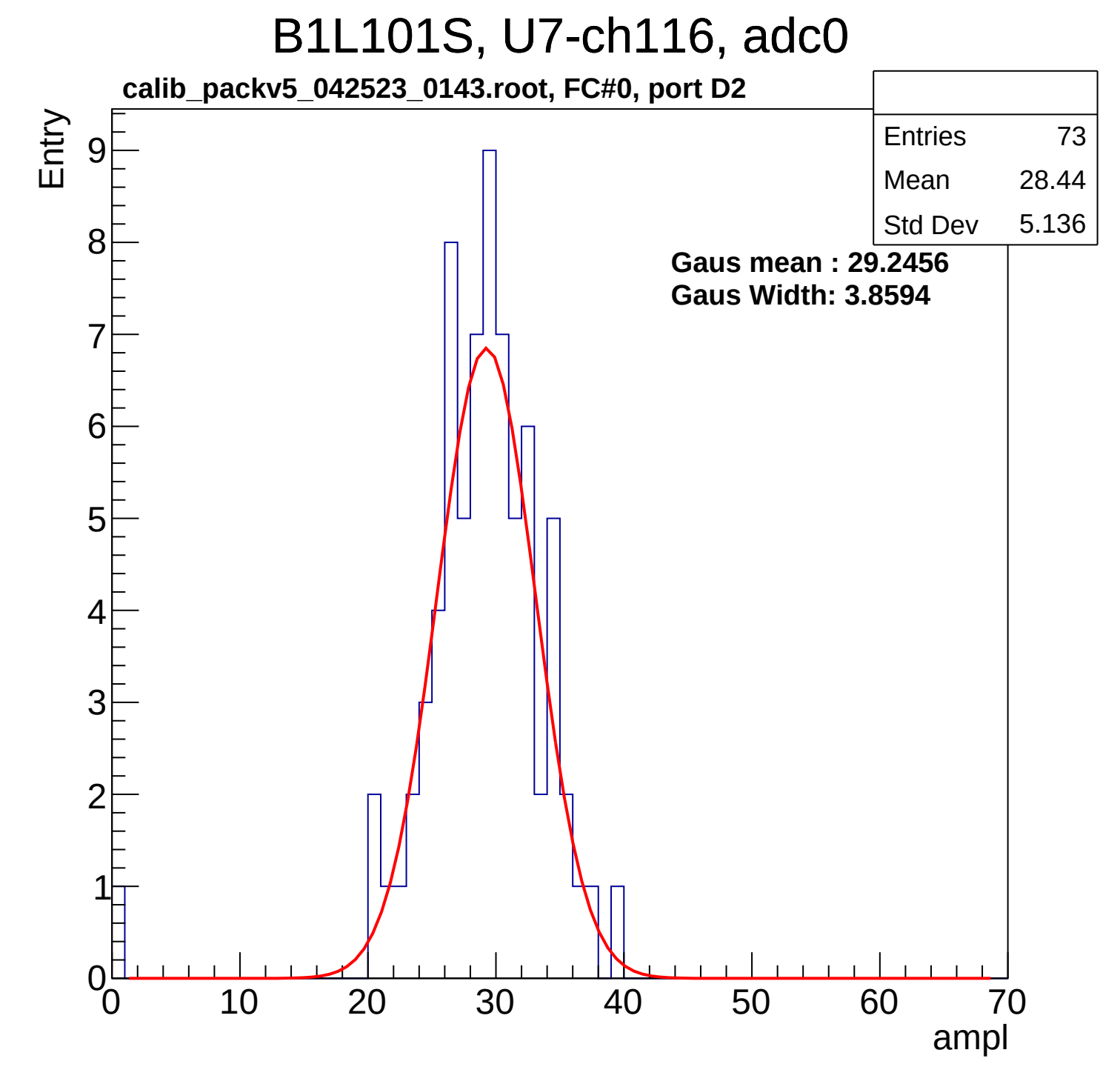
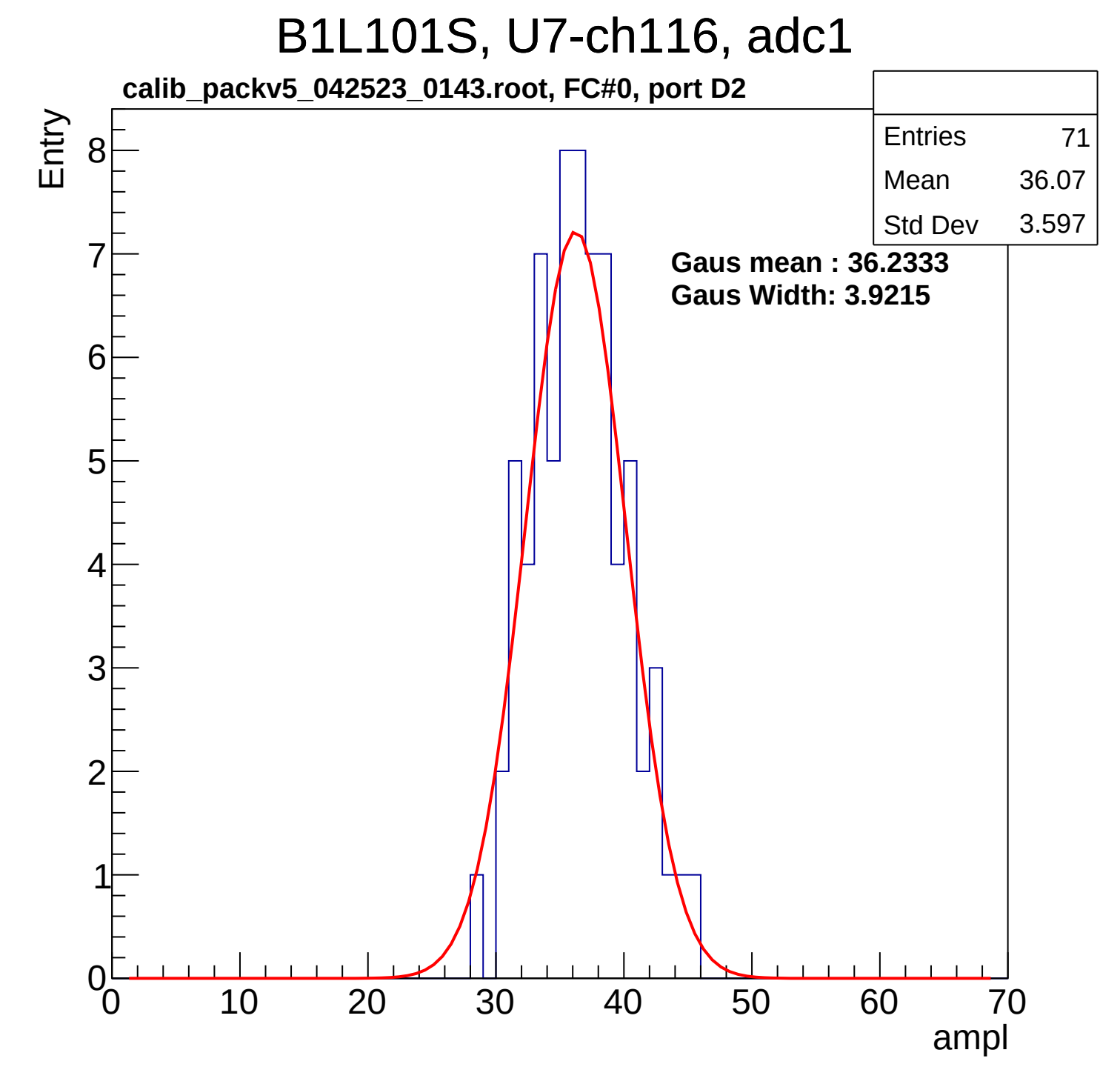

B1L101S, U7-ch116, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 28.44
Std Dev 5.136
Gaus mean : 29.2456
Gaus Width: 3.8594
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch116, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 36.07
Std Dev 3.597
Gaus mean : 36.2333
Gaus Width: 3.9215
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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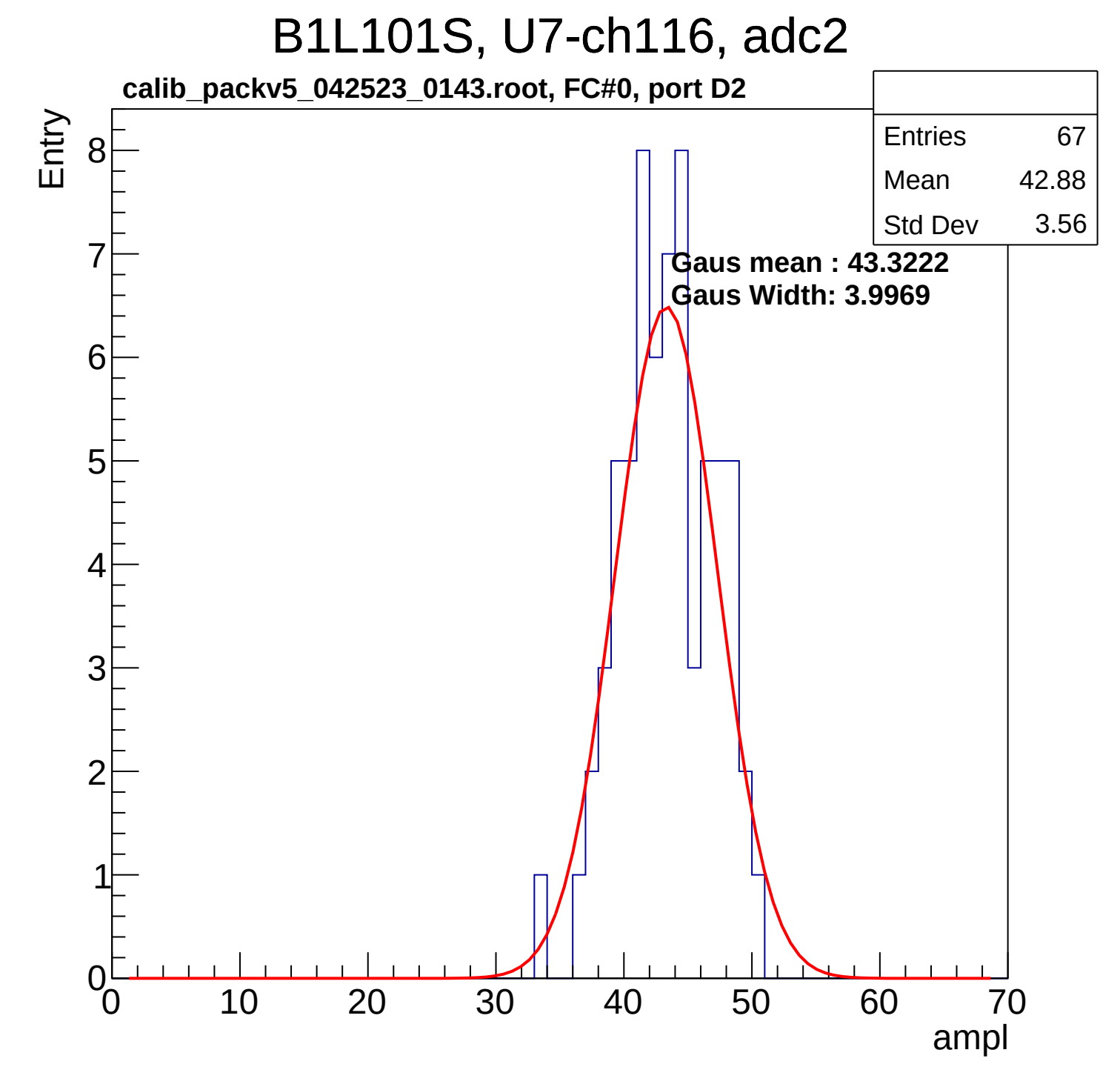
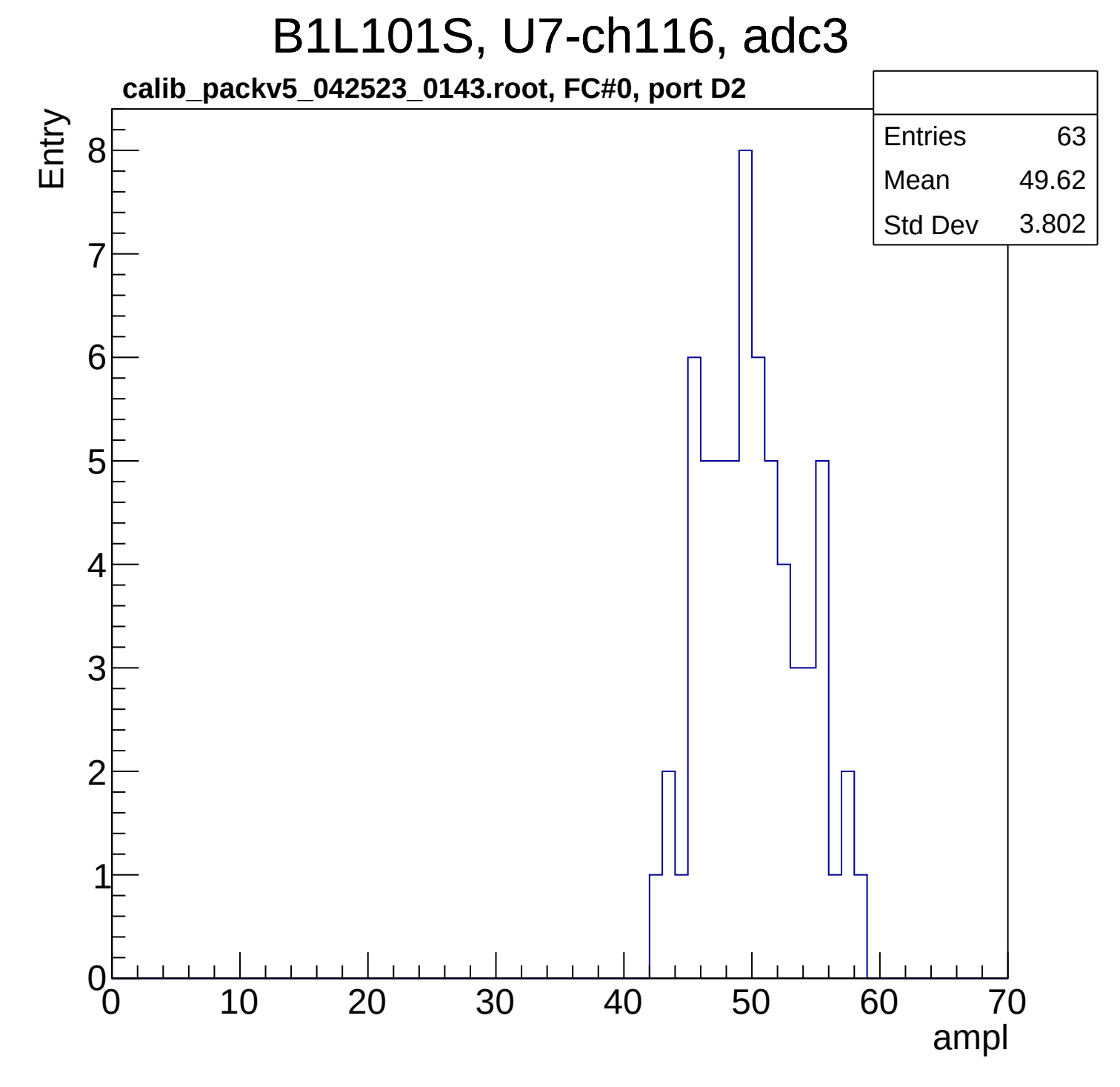
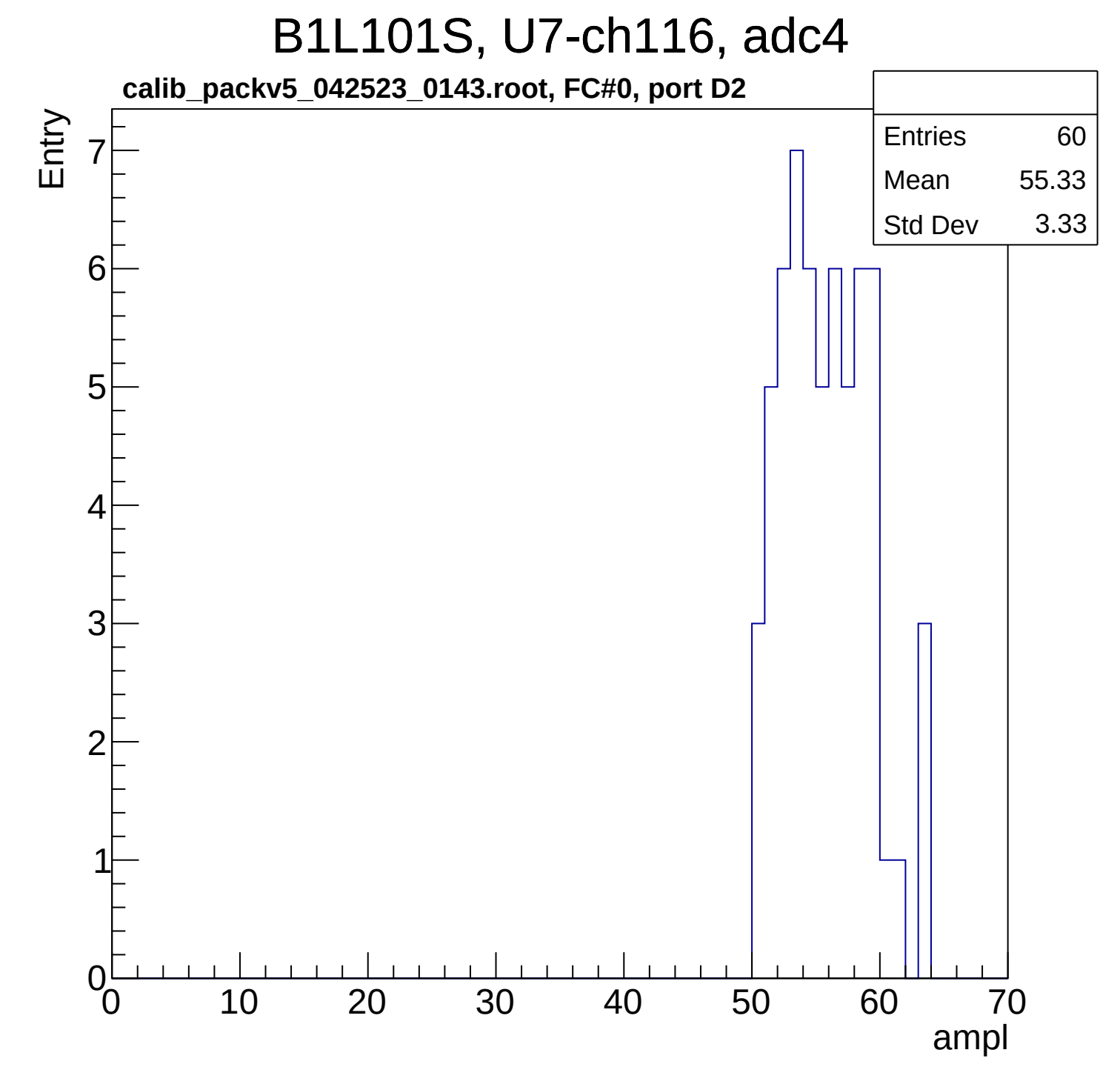
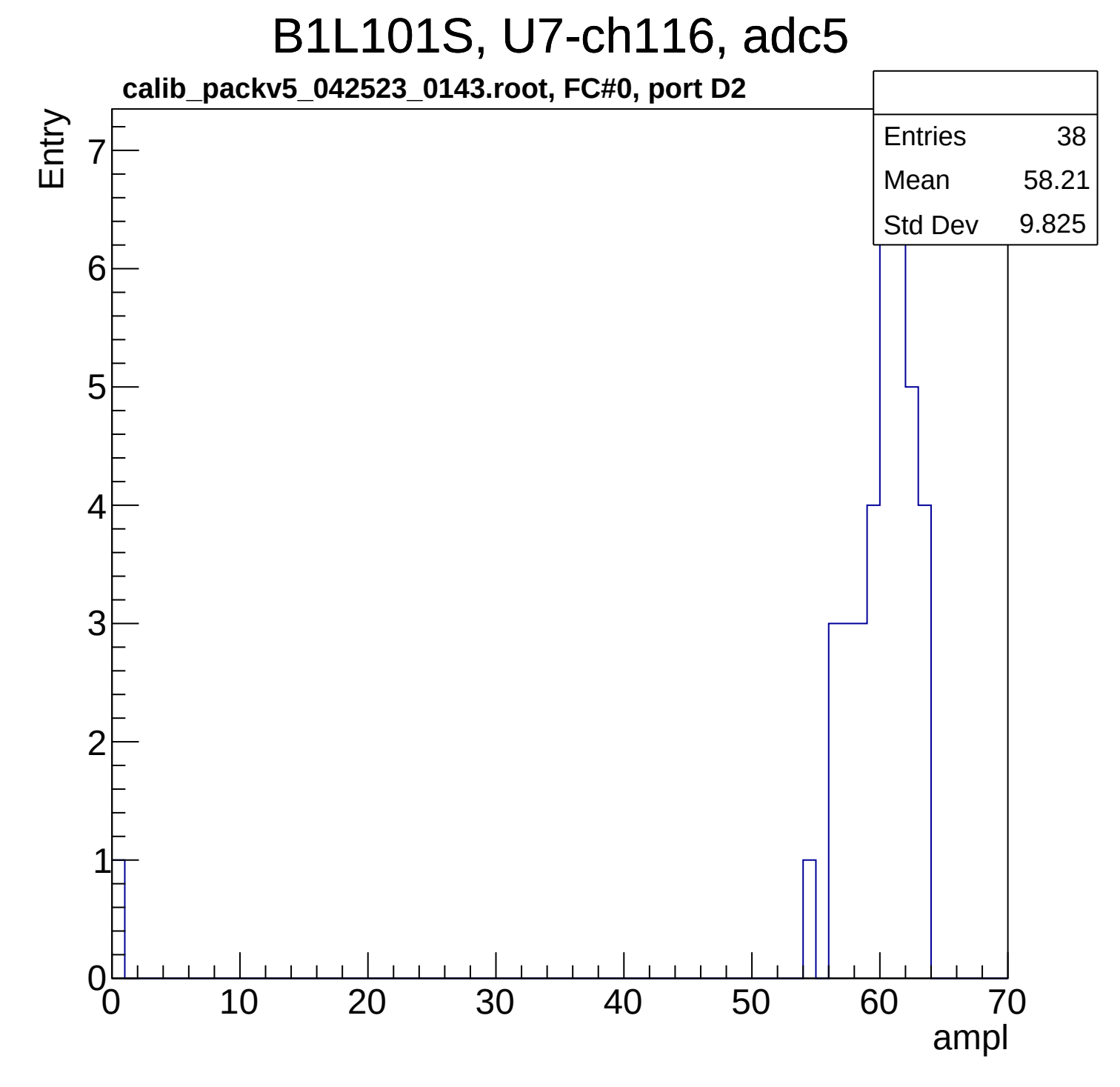
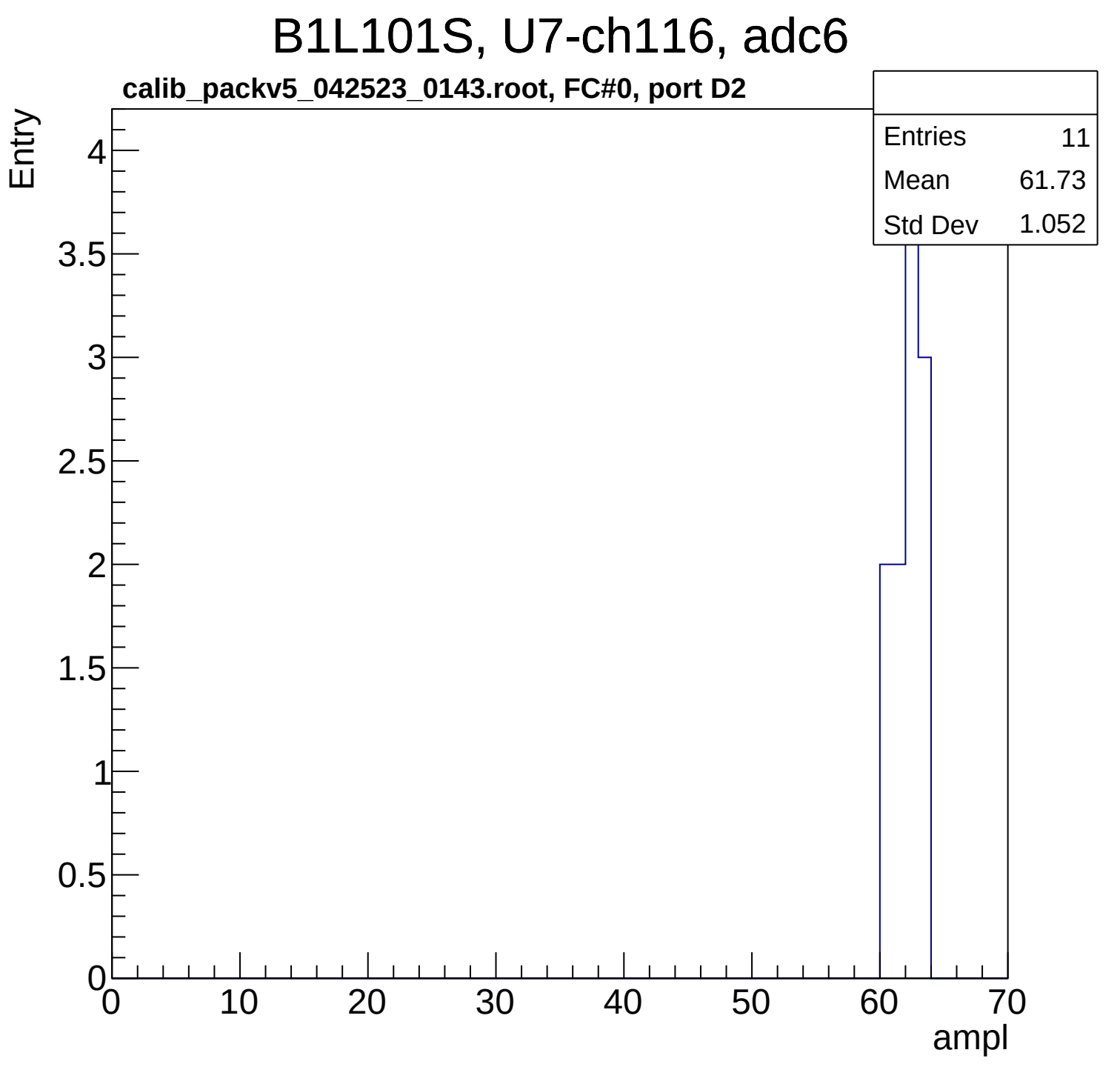
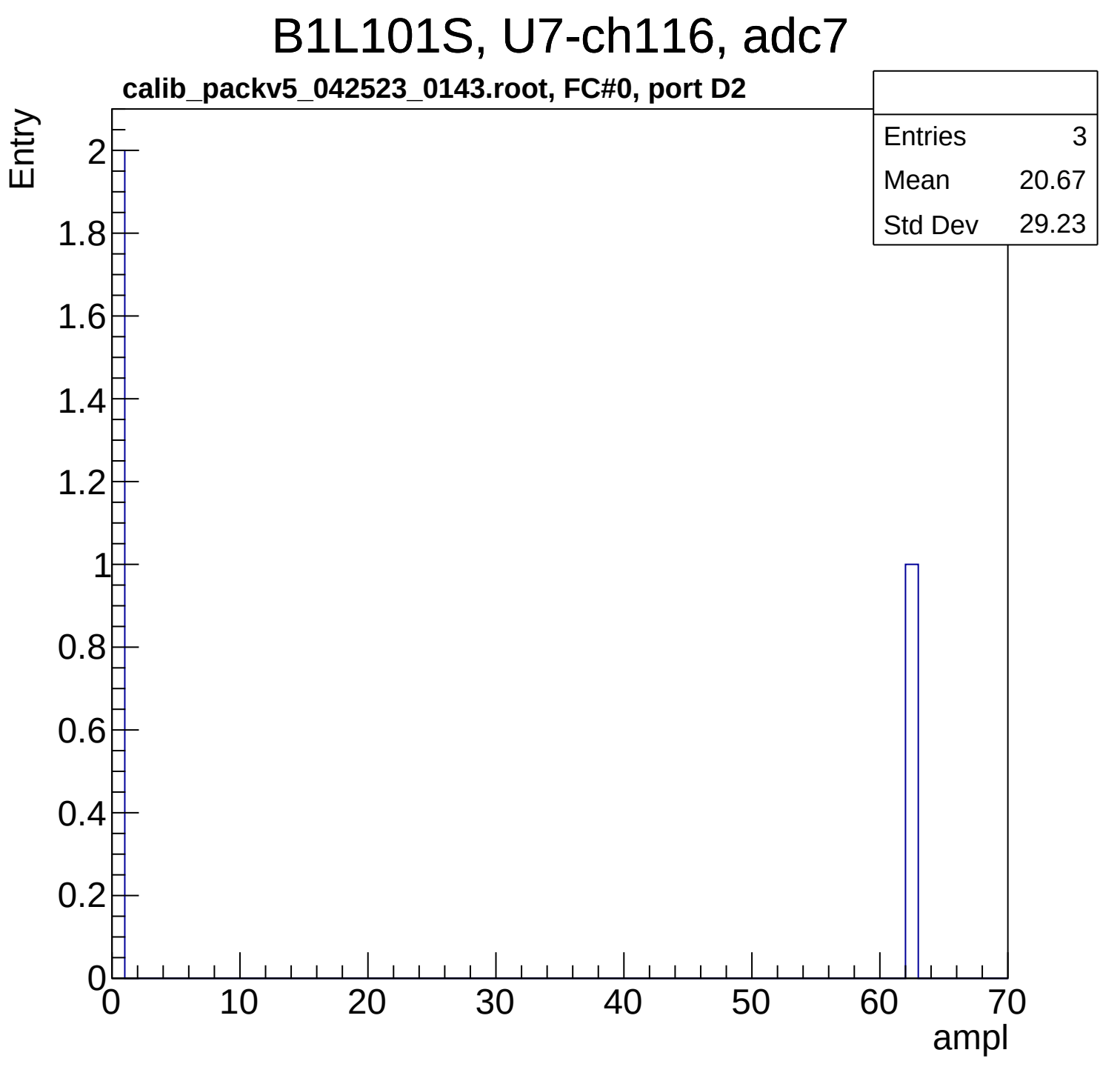

B1L101S, U7-ch116, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 42.88
Std Dev 3.56
Gaus mean : 43.3222
Gaus Width: 3.9969
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

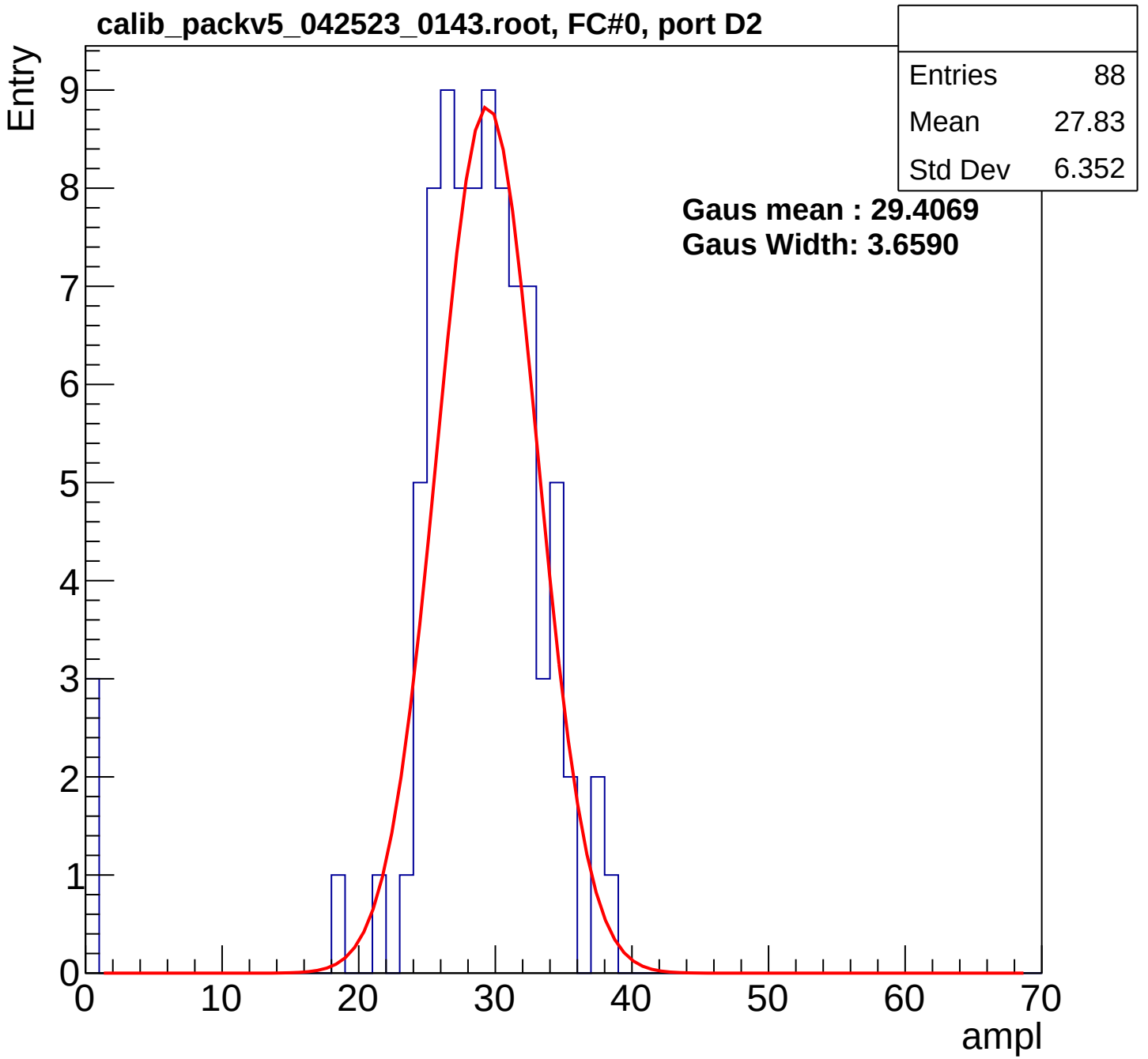

B1L101S, U7-ch116, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 49.62
Std Dev 3.802
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

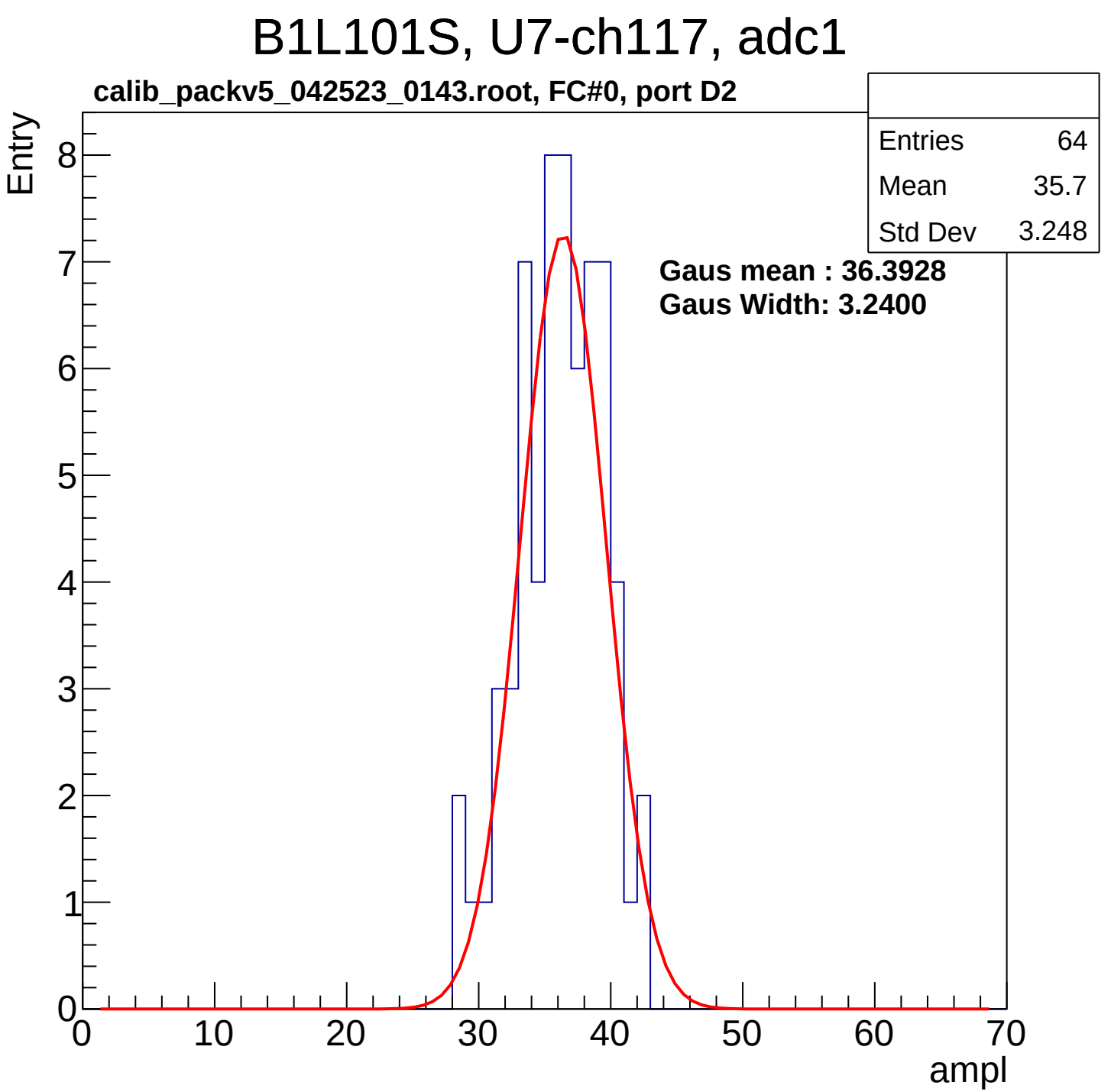

B1L101S, U7-ch116, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 55.33
Std Dev 3.33
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

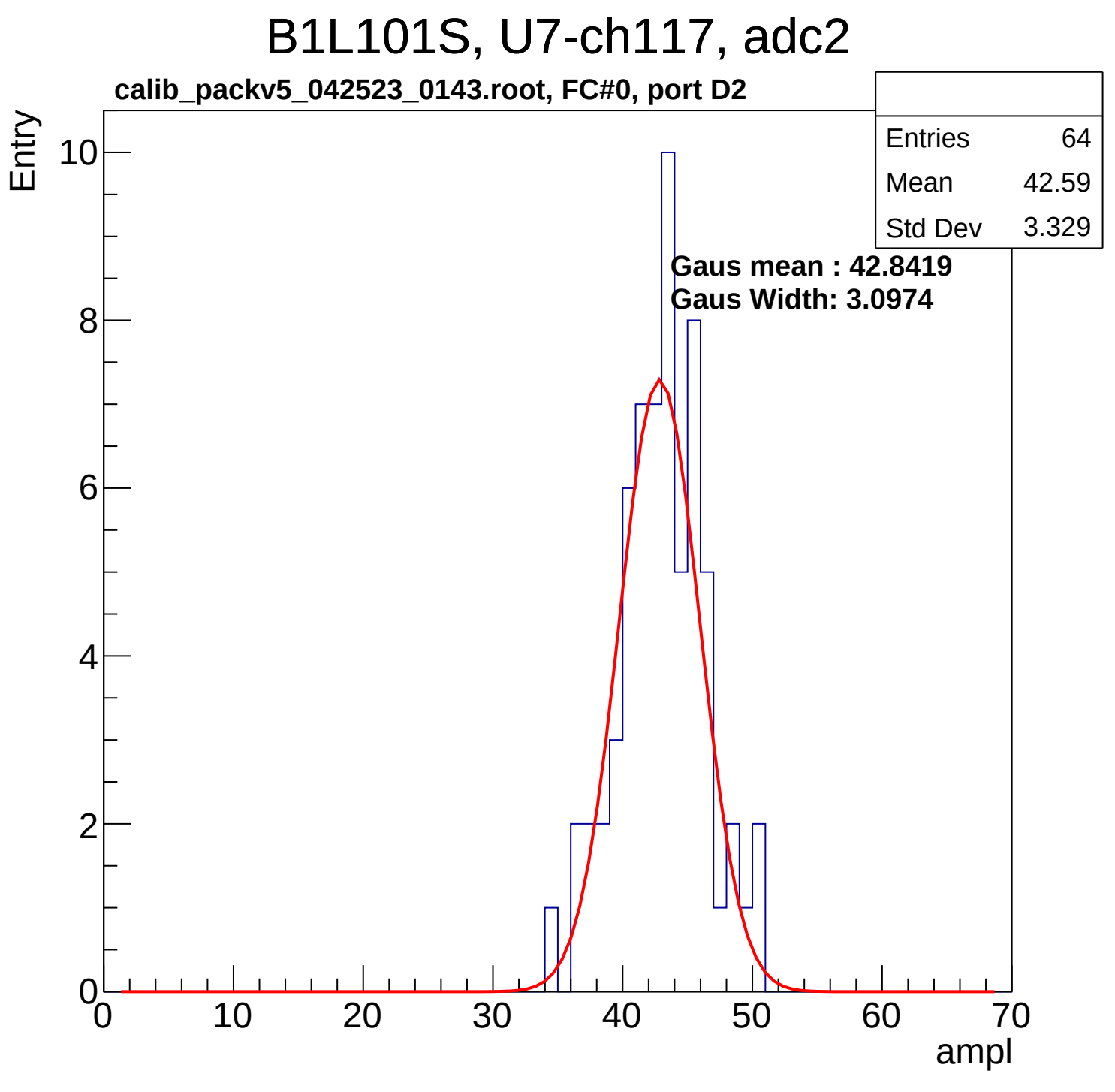

B1L101S, U7-ch116, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 38
Mean 58.21
Std Dev 9.825
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

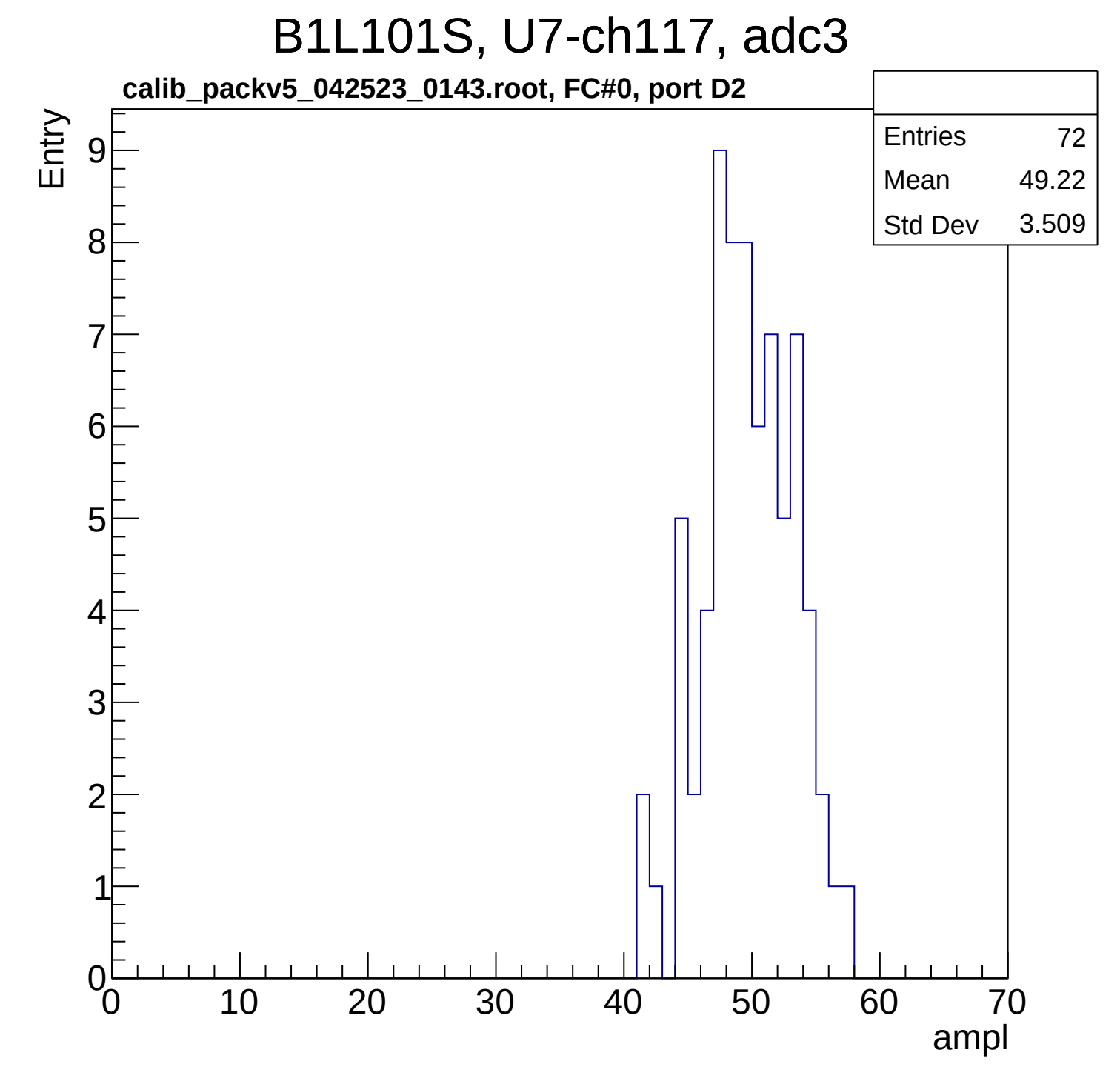

B1L101S, U7-ch116, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 11
Mean 61.73
Std Dev 1.052
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

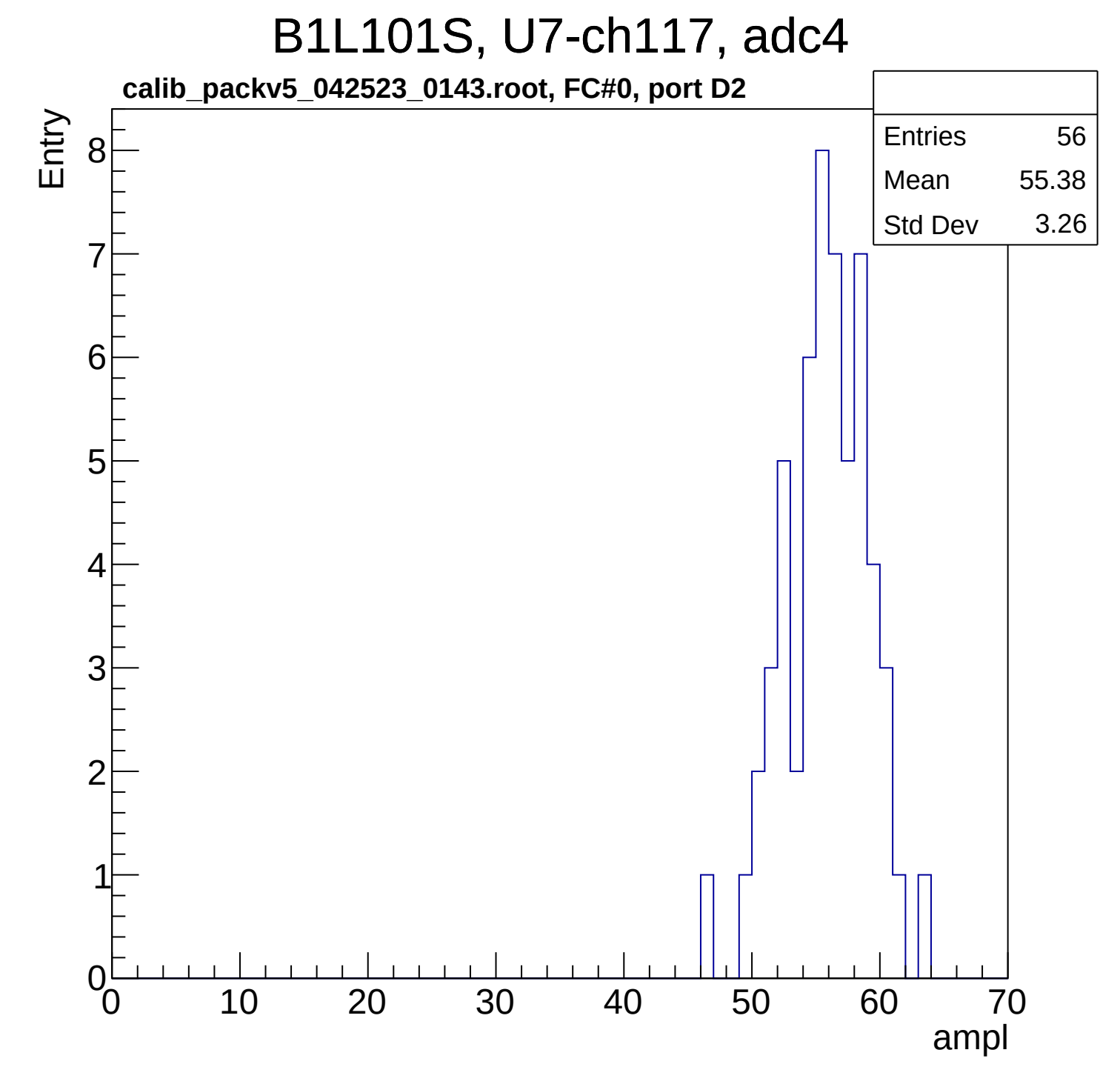

B1L101S, U7-ch116, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 20.67
Std Dev 29.23
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U7-ch117, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 88
Mean 27.83
Std Dev 6.352
Gaus mean : 29.4069
Gaus Width: 3.6590
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L101S, U7-ch117, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 35.7
Std Dev 3.248
Gaus mean : 36.3928
Gaus Width: 3.2400
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch117, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 42.59
Std Dev 3.329
Gaus mean : 42.8419
Gaus Width: 3.0974
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch117, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 49.22
Std Dev 3.509
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch117, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 55.38
Std Dev 3.26
Entry
ampl
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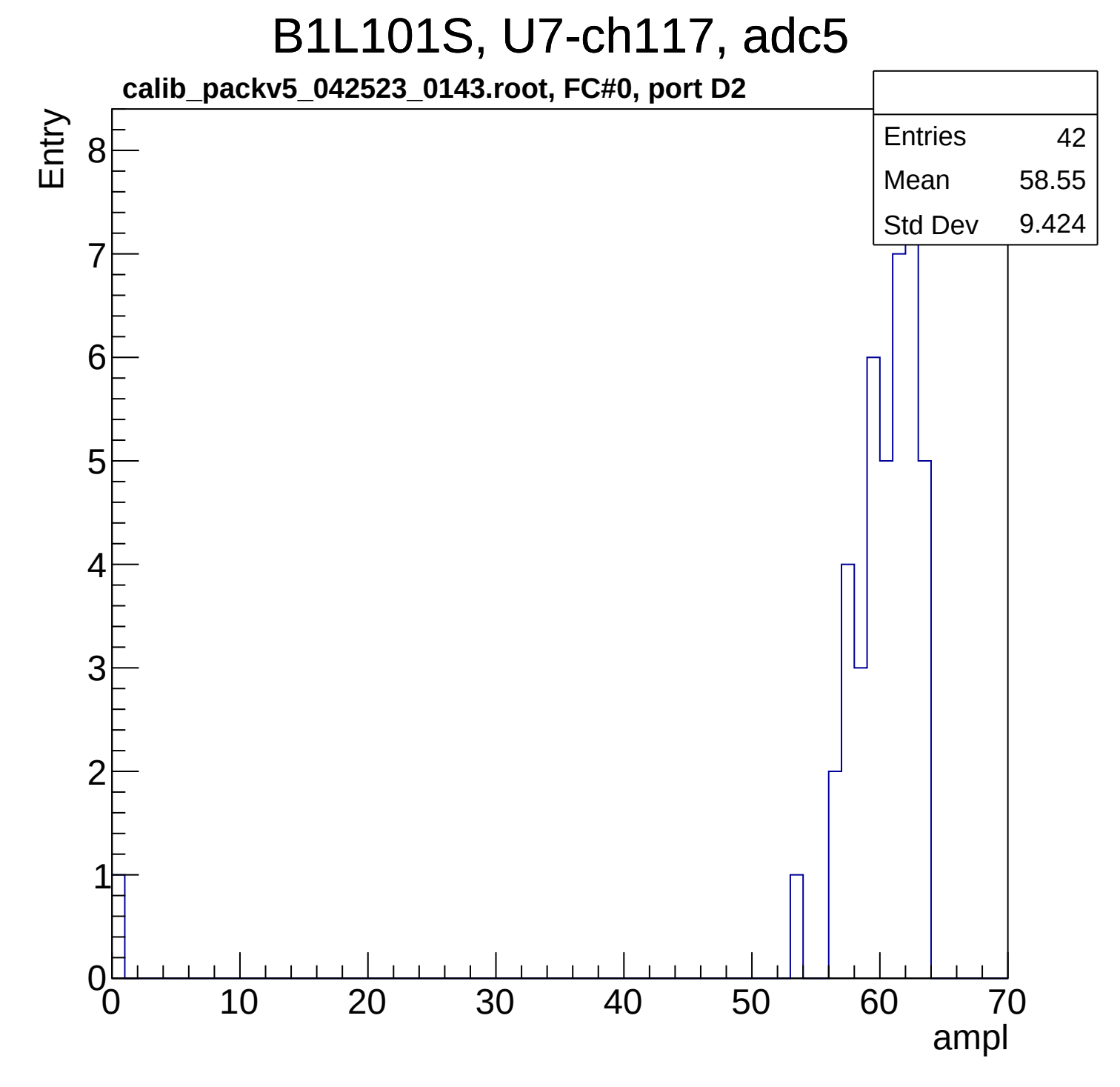
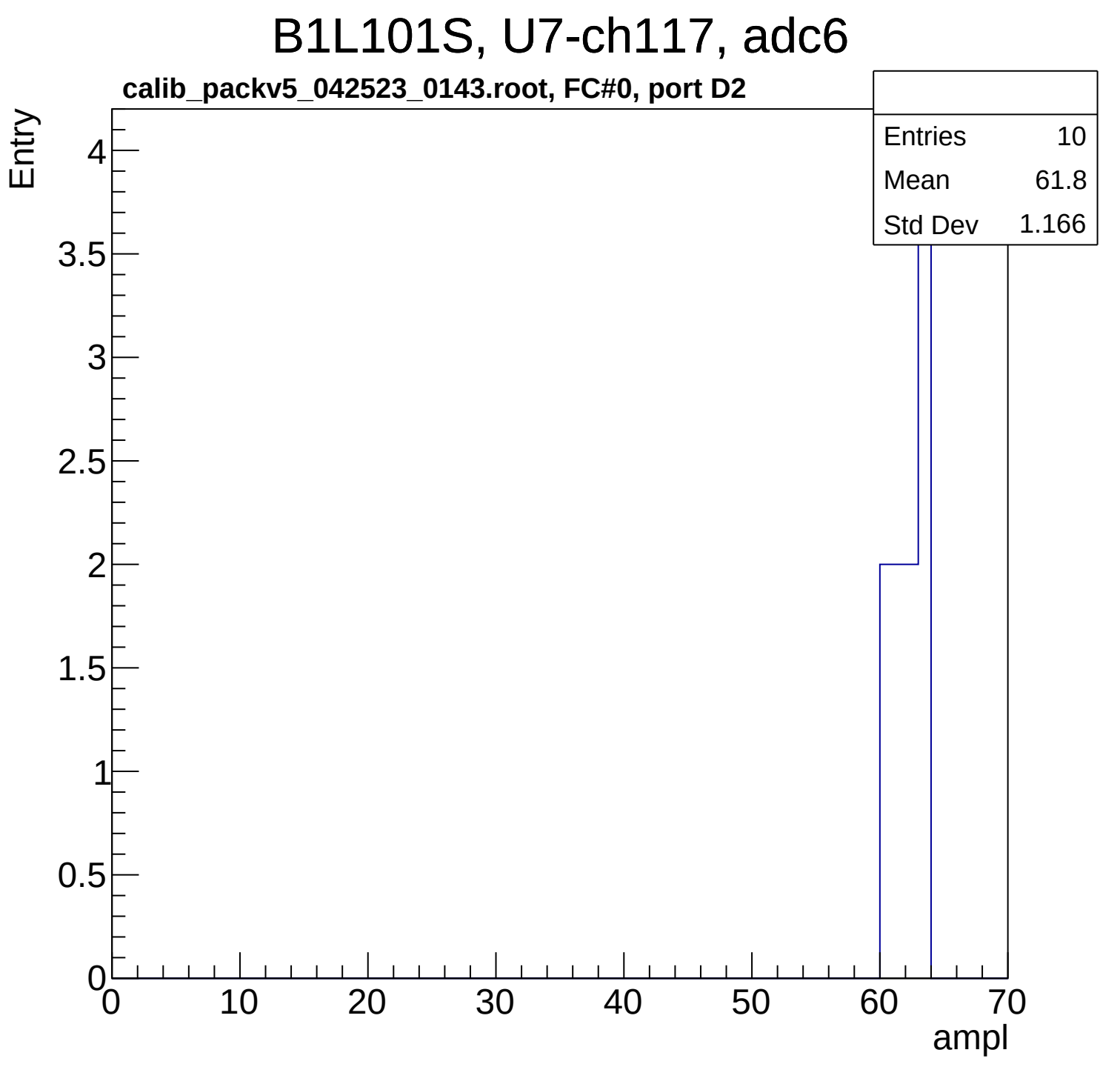
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch117, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 58.55
Std Dev 9.424
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch117, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 61.8
Std Dev 1.166
Entry
ampl
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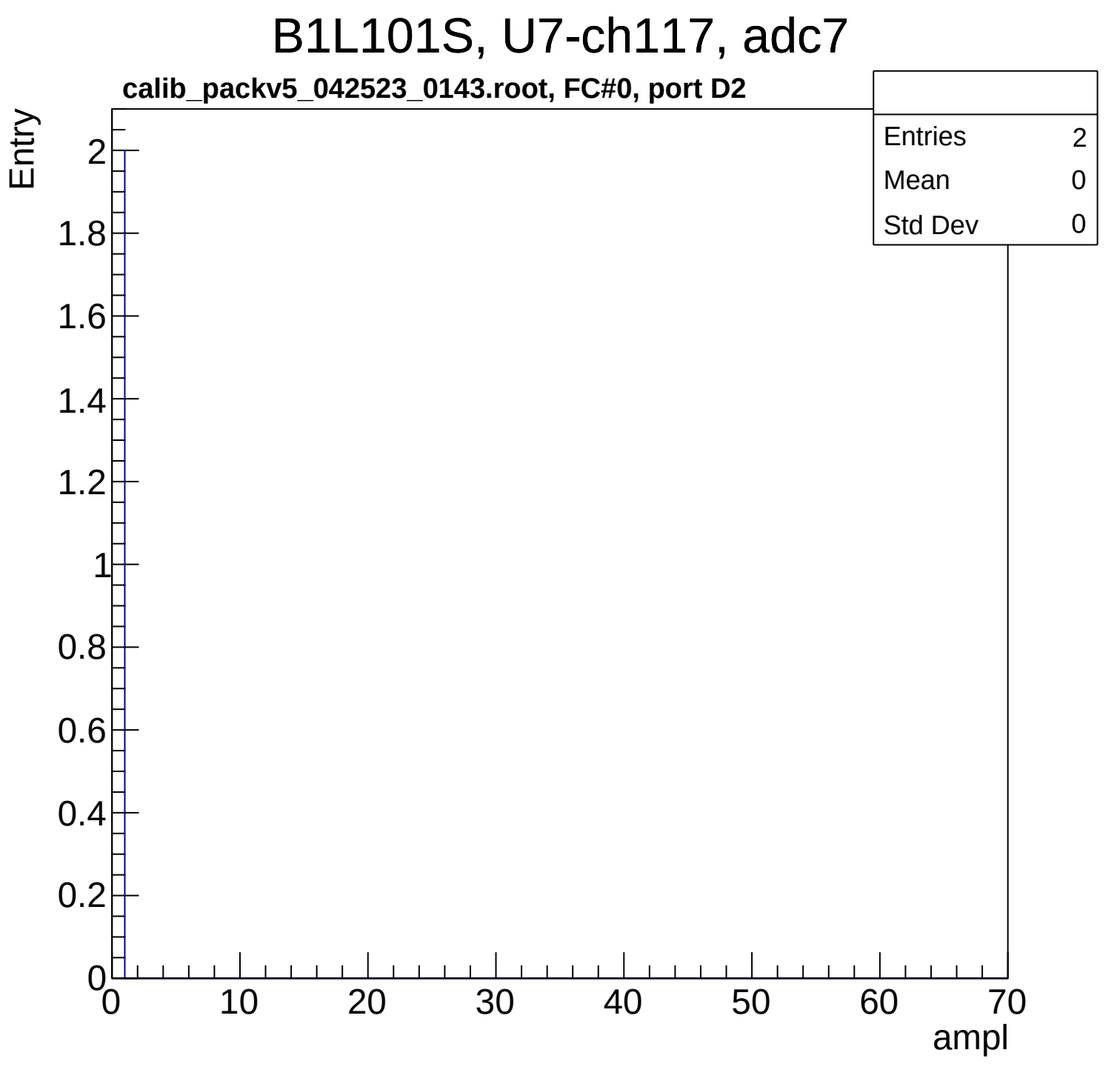
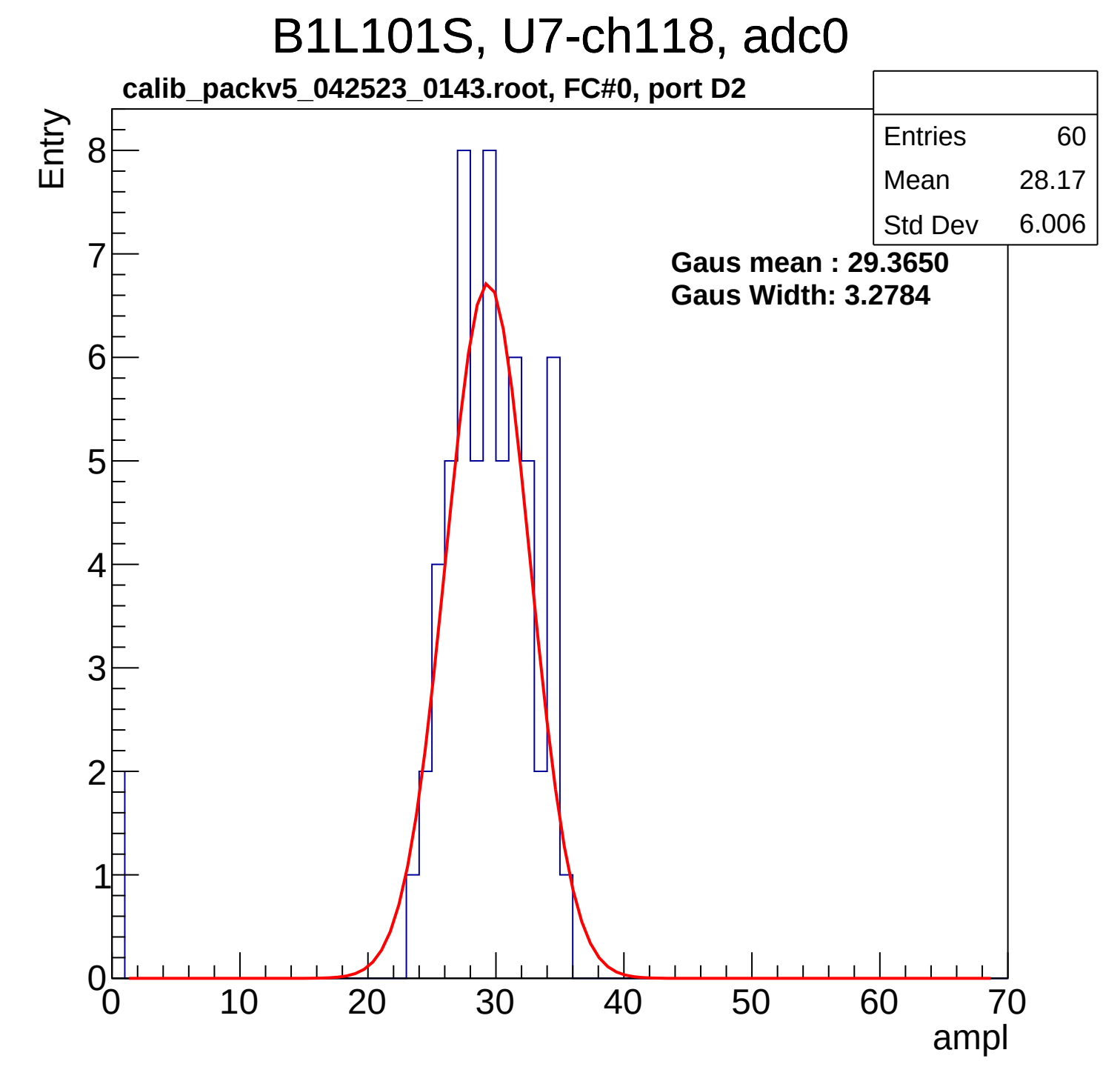
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L101S, U7-ch117, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U7-ch118, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 28.17
Std Dev 6.006
Gaus mean : 29.3650
Gaus Width: 3.2784
Entry
ampl
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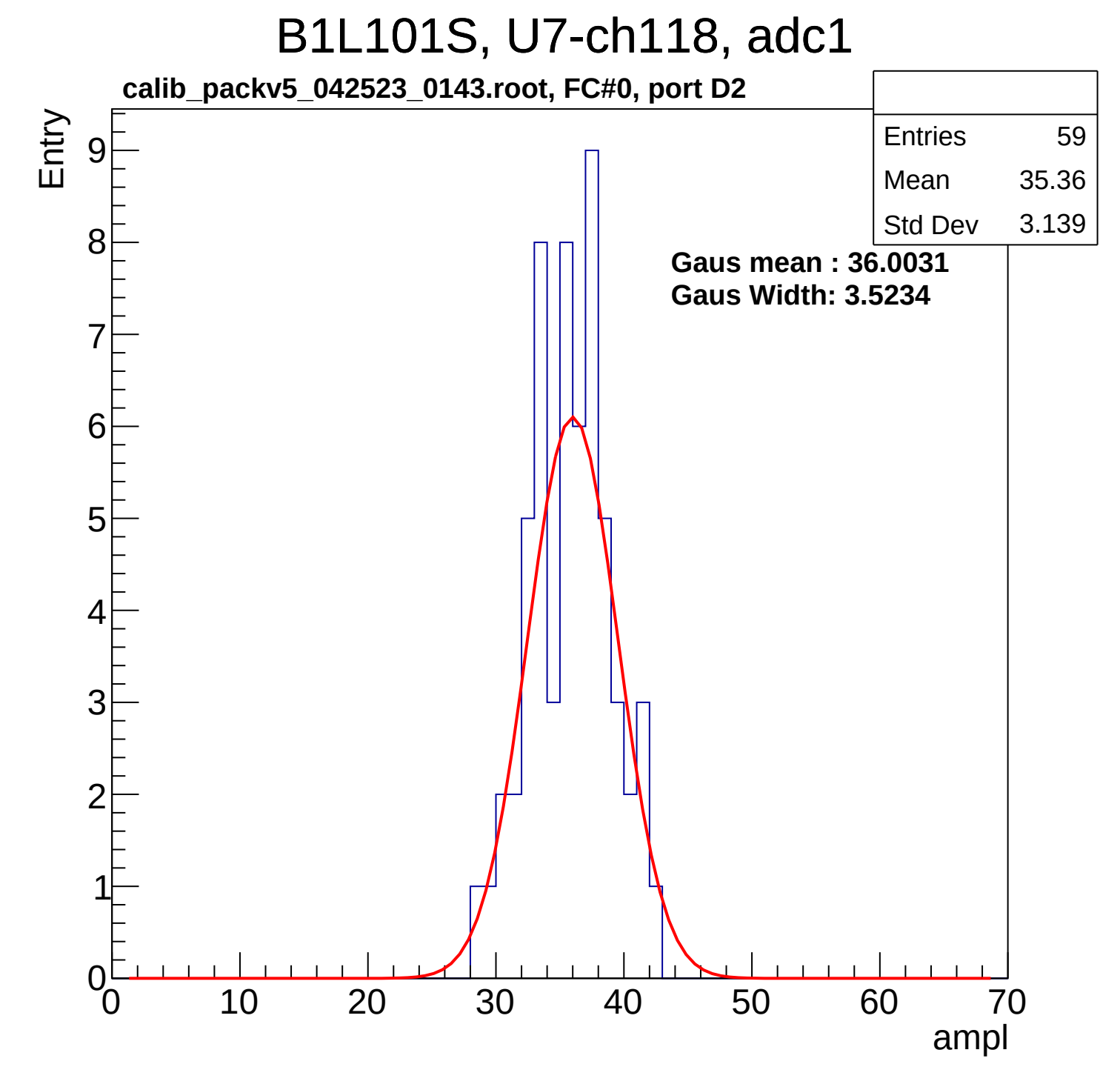
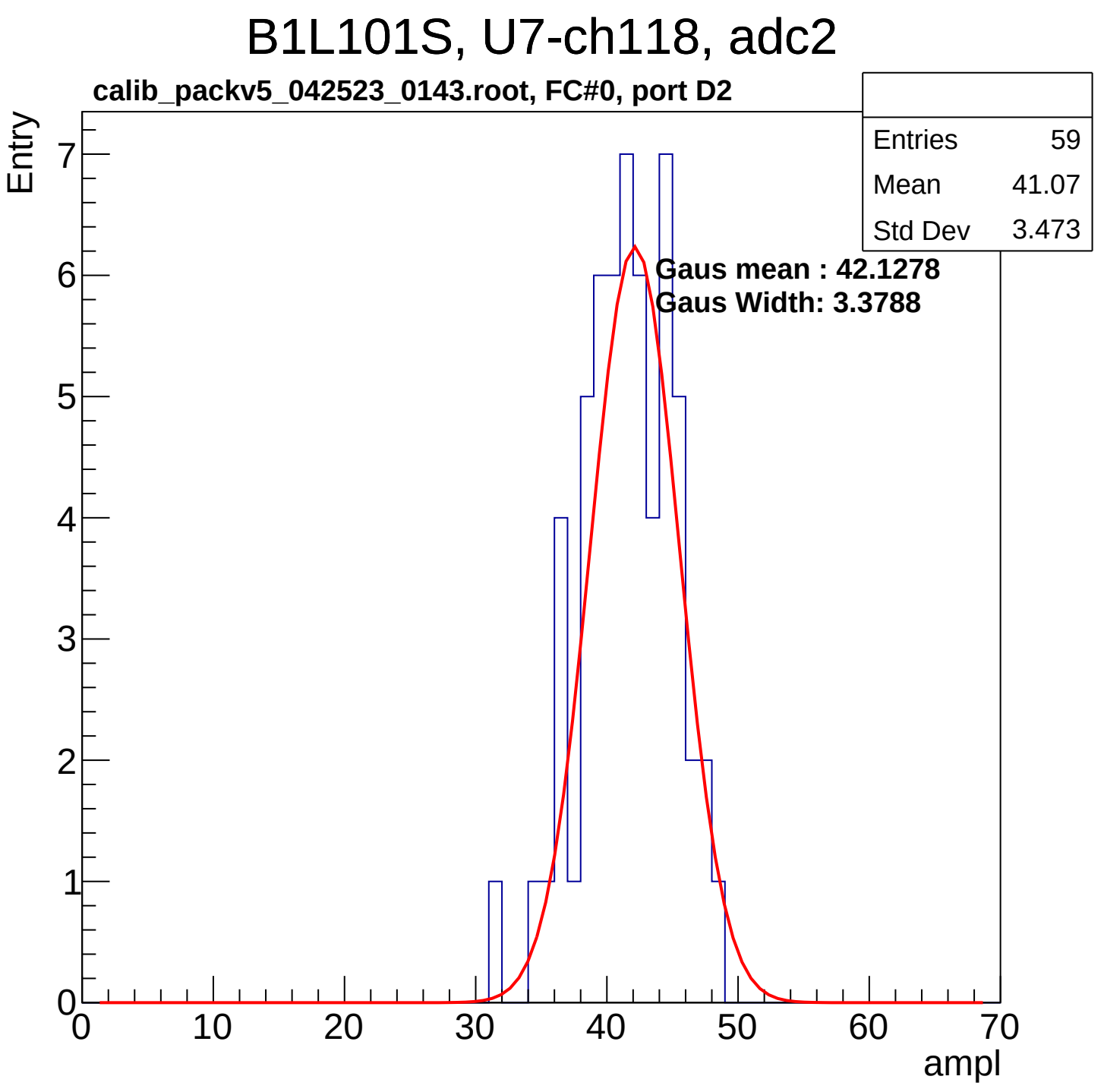
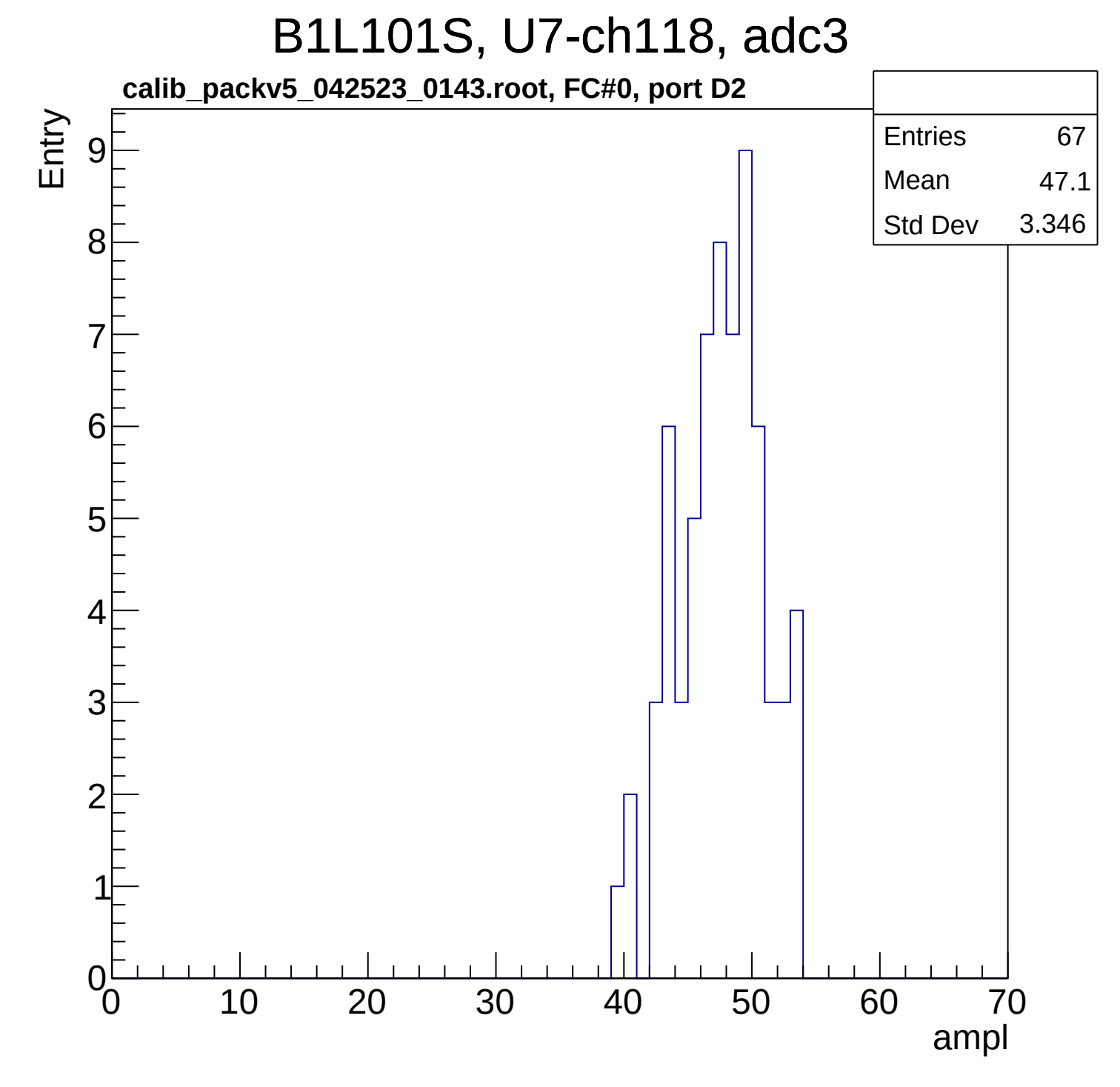
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch118, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 35.36
Std Dev 3.139
Gaus mean : 36.0031
Gaus Width: 3.5234
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch118, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 41.07
Std Dev 3.473
Gaus mean : 42.1278
Gaus Width: 3.3788
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U7-ch118, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 47.1
Std Dev 3.346
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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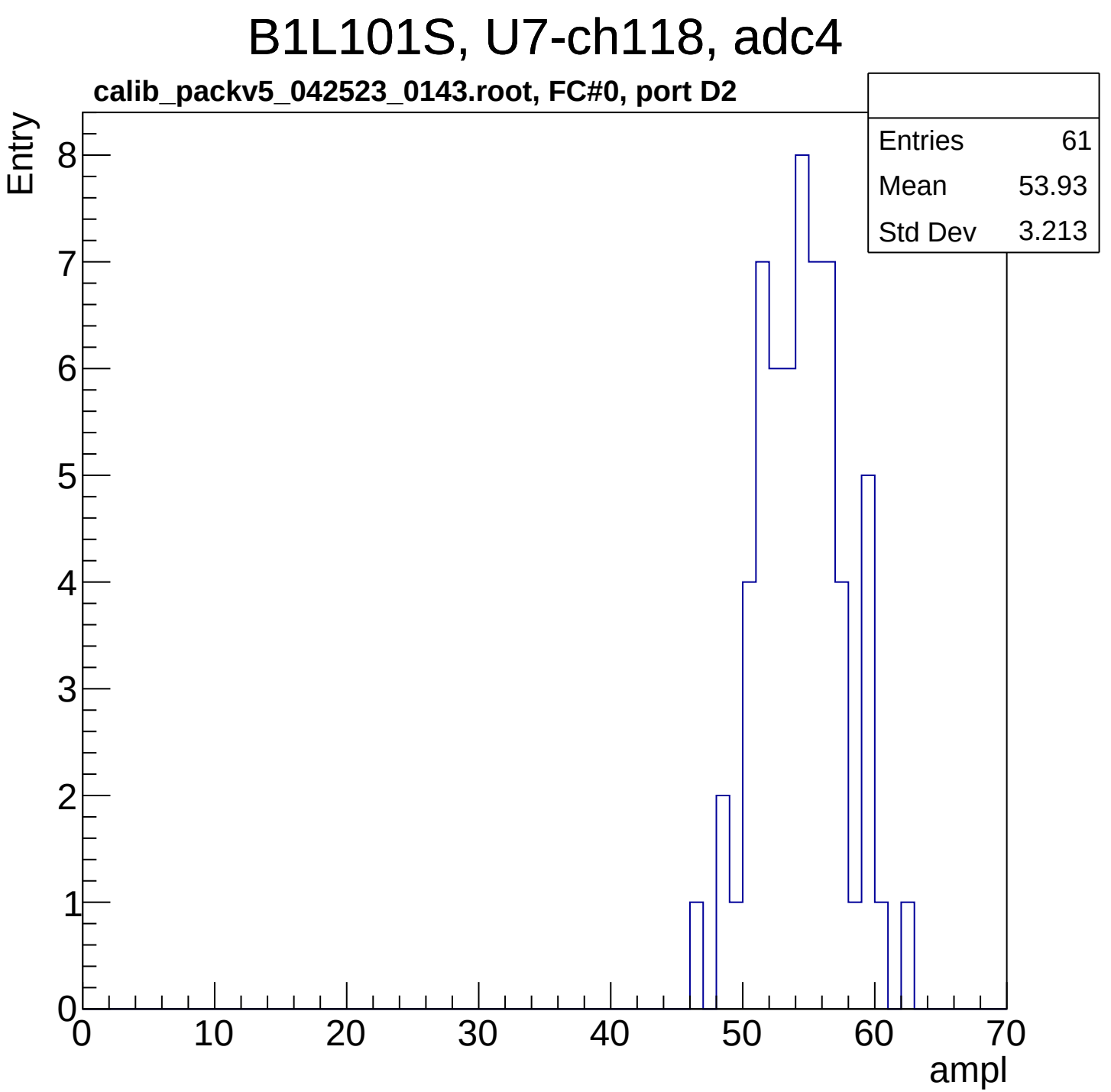
40
50
60
70


B1L101S, U7-ch118, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 53.93
Std Dev 3.213
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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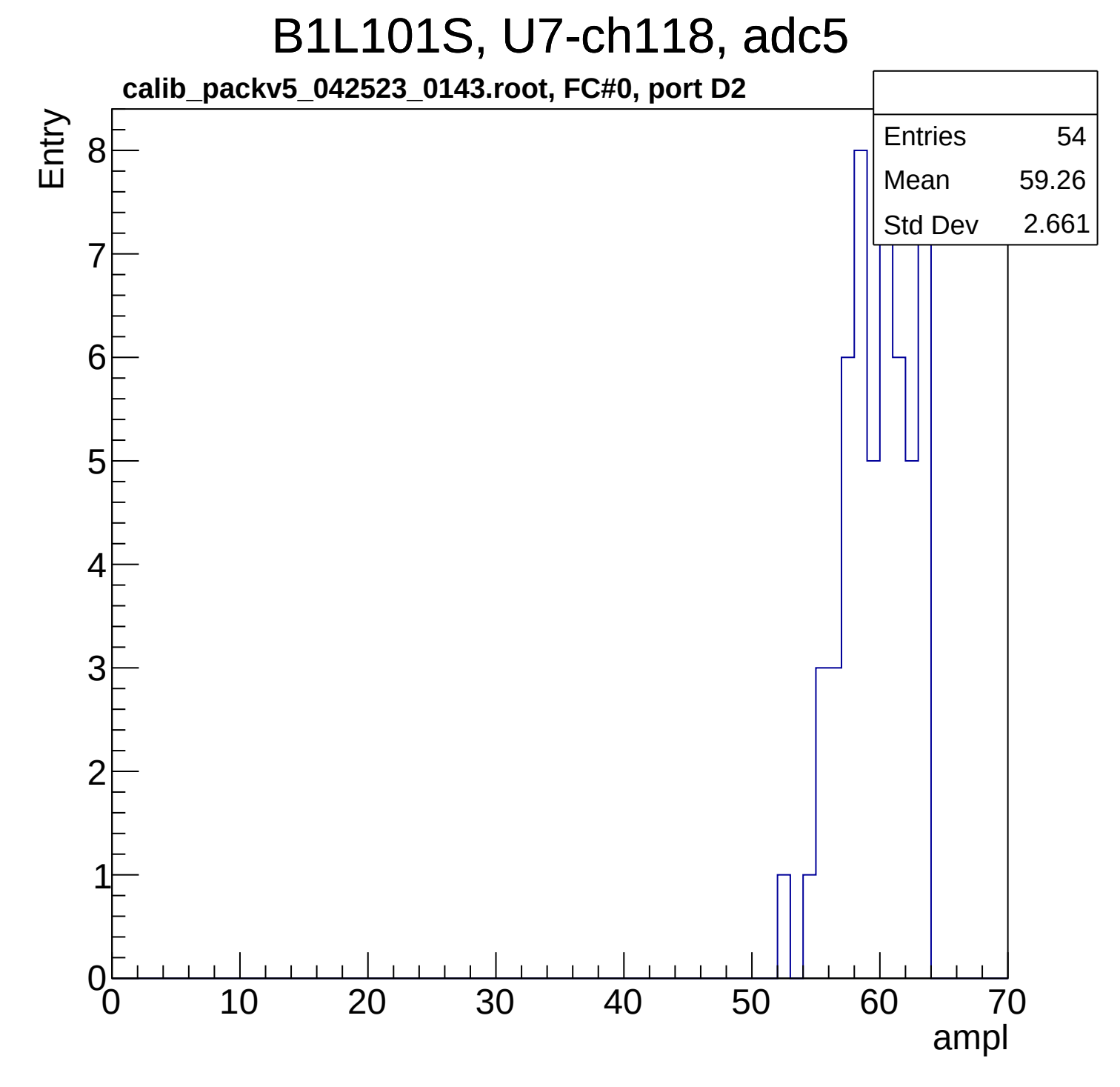
B1L101S, U7-ch118, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 59.26
Std Dev 2.661
Entry
ampl
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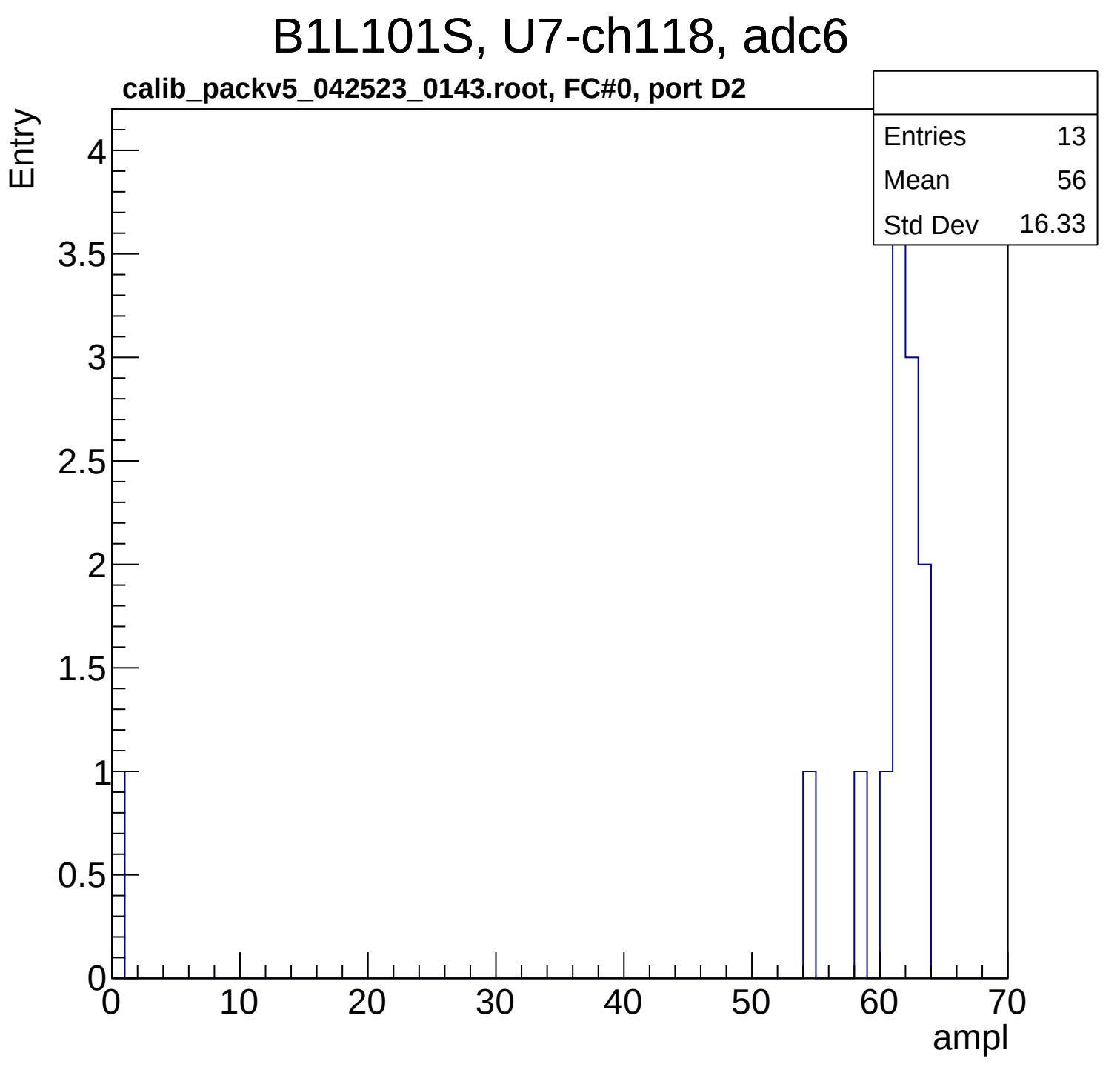
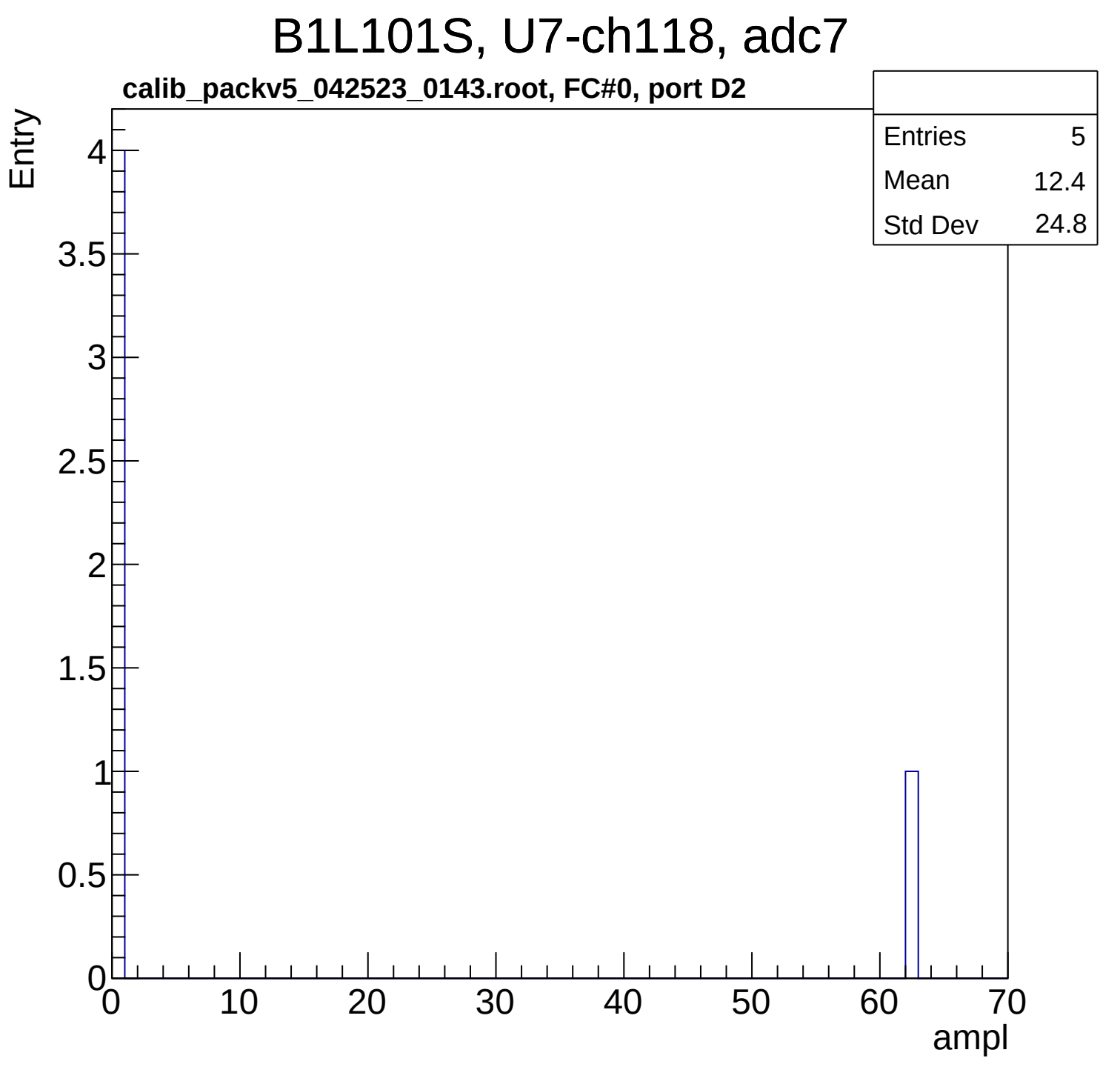
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch118, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 13
Mean 56
Std Dev 16.33
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L101S, U7-ch118, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 12.4
Std Dev 24.8
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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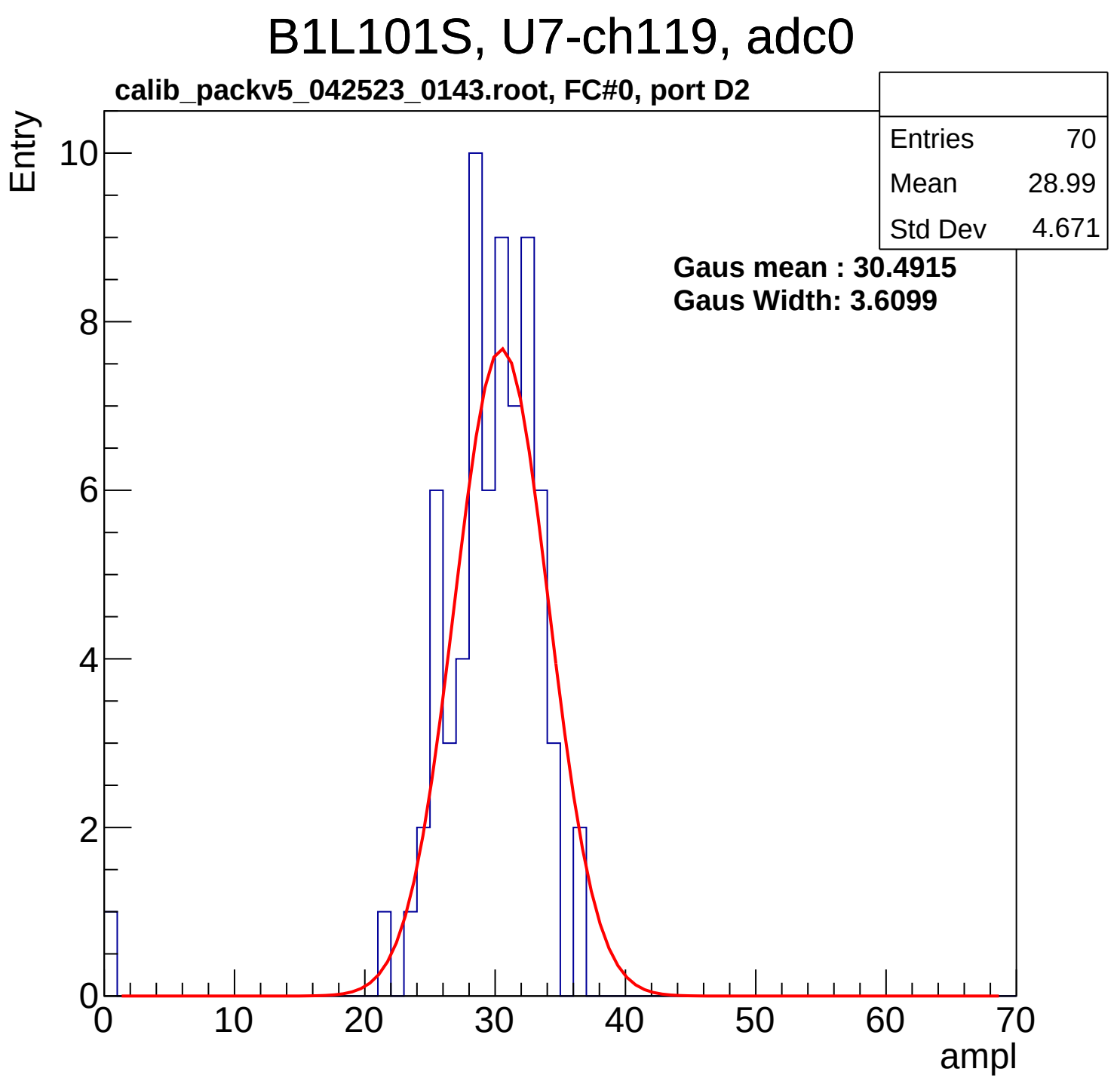
B1L101S, U7-ch119, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 28.99
Std Dev 4.671
Gaus mean : 30.4915
Gaus Width: 3.6099
Entry
ampl
0
2
4
6
8
10
0
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20
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40
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60
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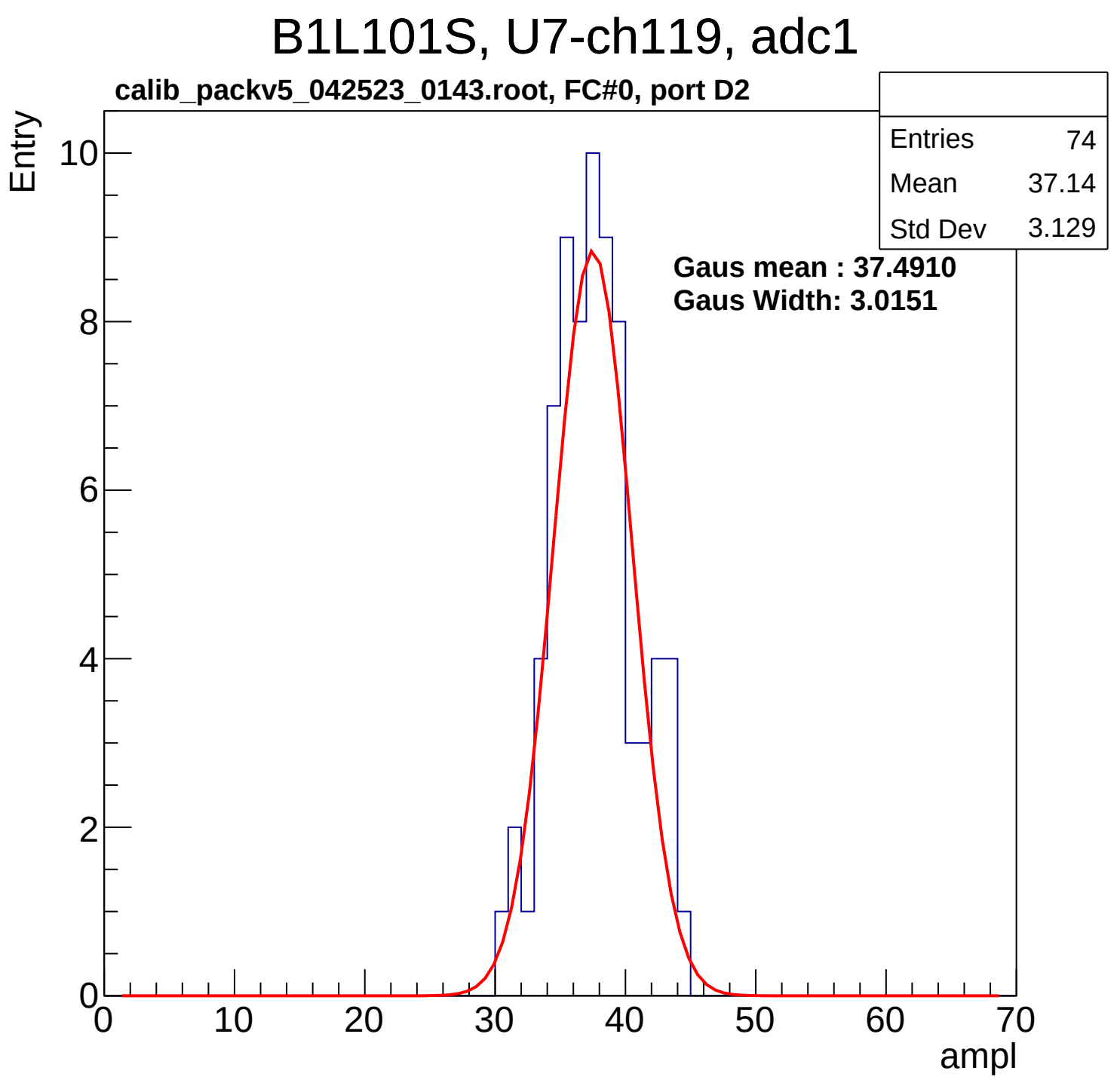
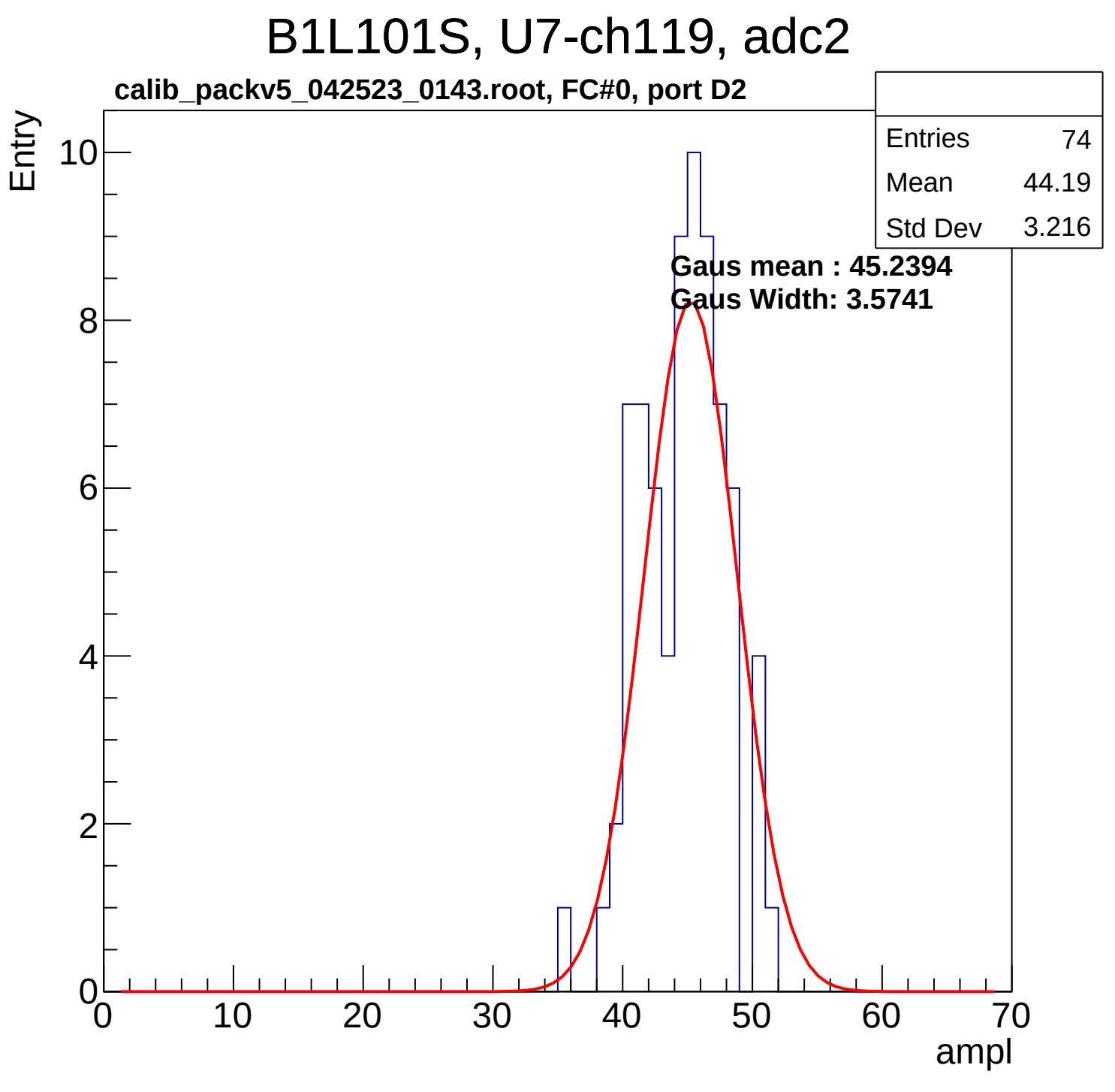
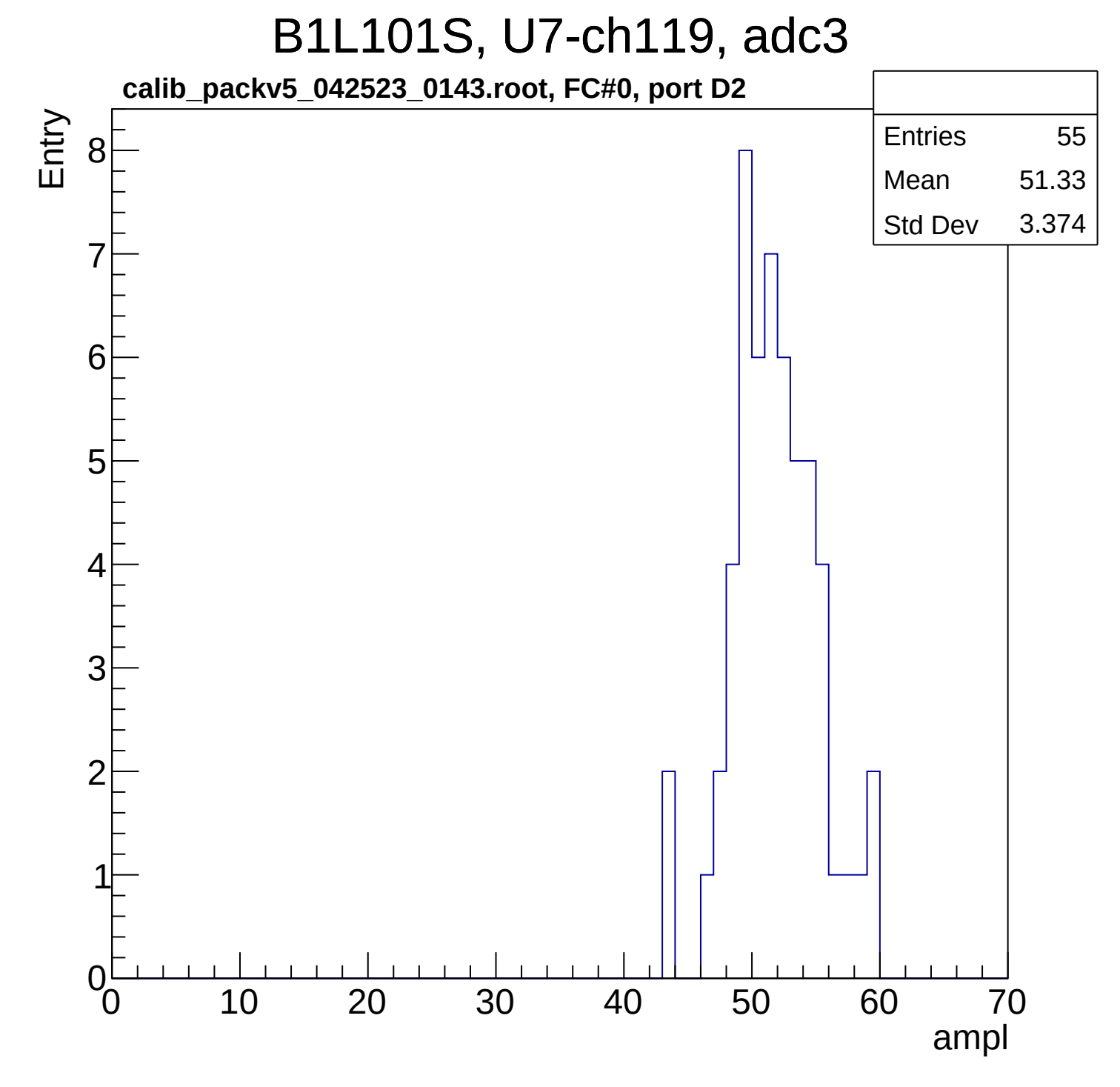

B1L101S, U7-ch119, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 37.14
Std Dev 3.129
Gaus mean : 37.4910
Gaus Width: 3.0151
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch119, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 44.19
Std Dev 3.216
Gaus mean : 45.2394
Gaus Width: 3.5741
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch119, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 51.33
Std Dev 3.374
Entry
ampl
0
1
2
3
4
5
6
7
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0
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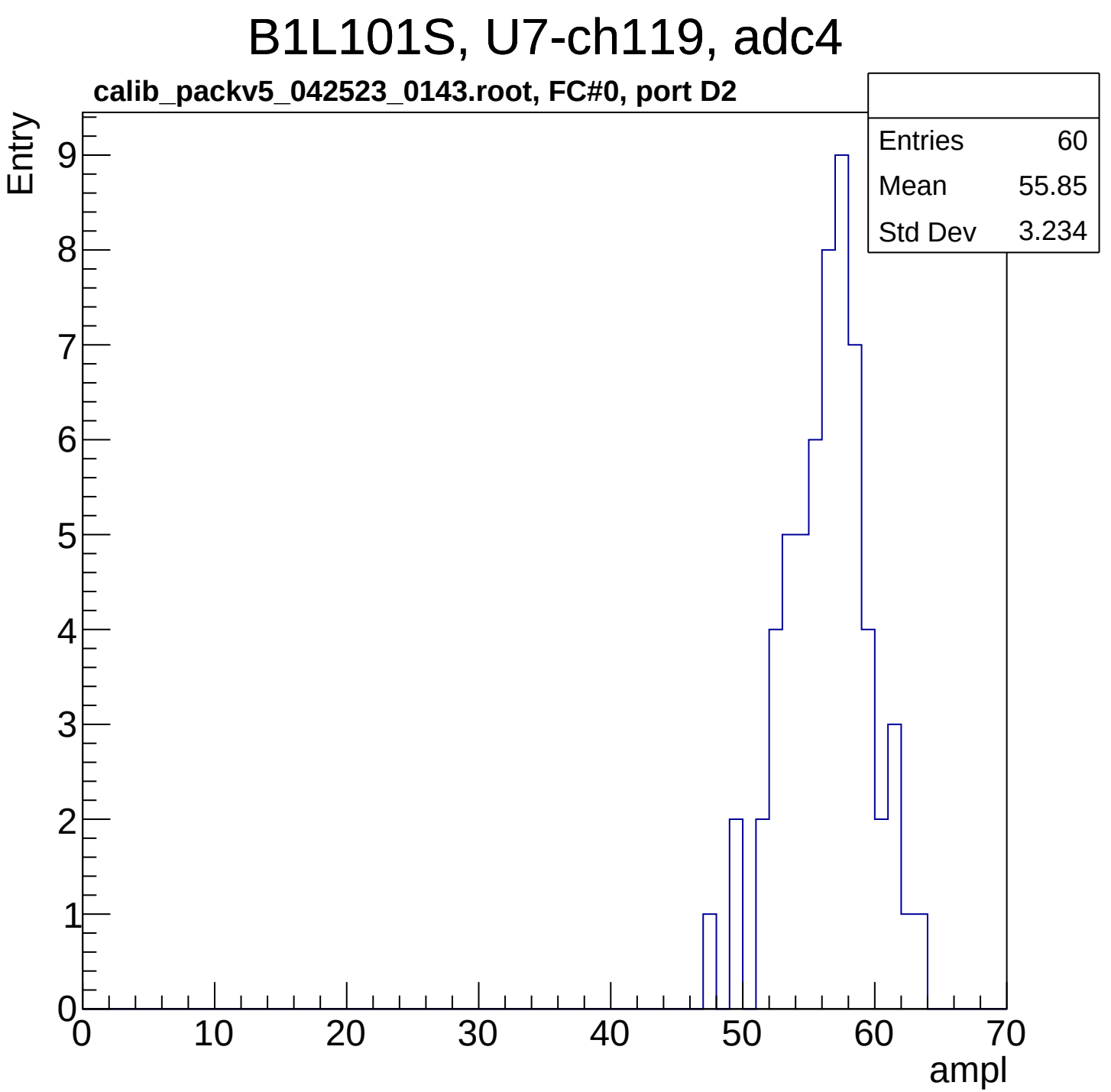
B1L101S, U7-ch119, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 55.85
Std Dev 3.234
Entry
ampl
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2
3
4
5
6
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0
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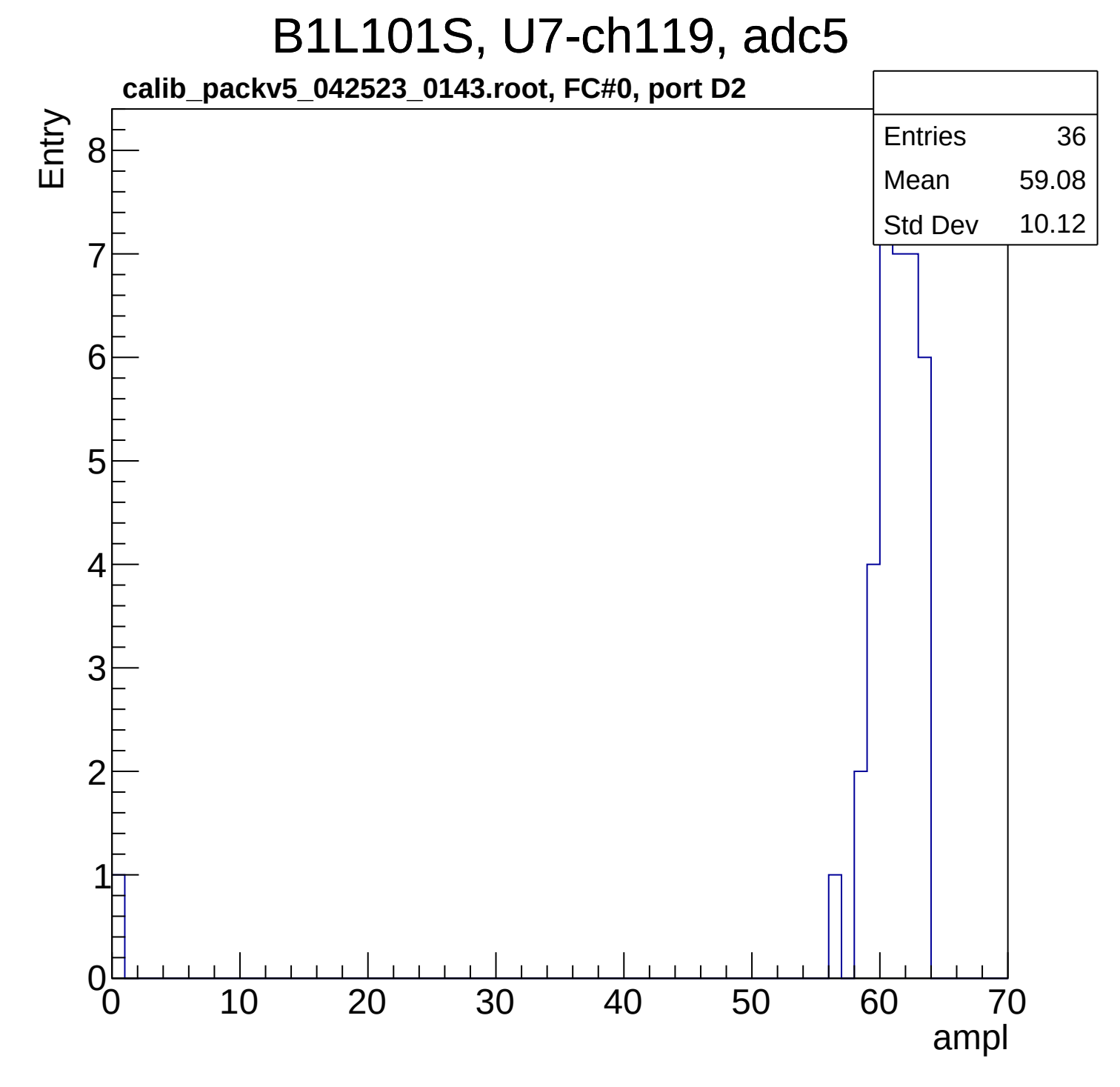
B1L101S, U7-ch119, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 36
Mean 59.08
Std Dev 10.12
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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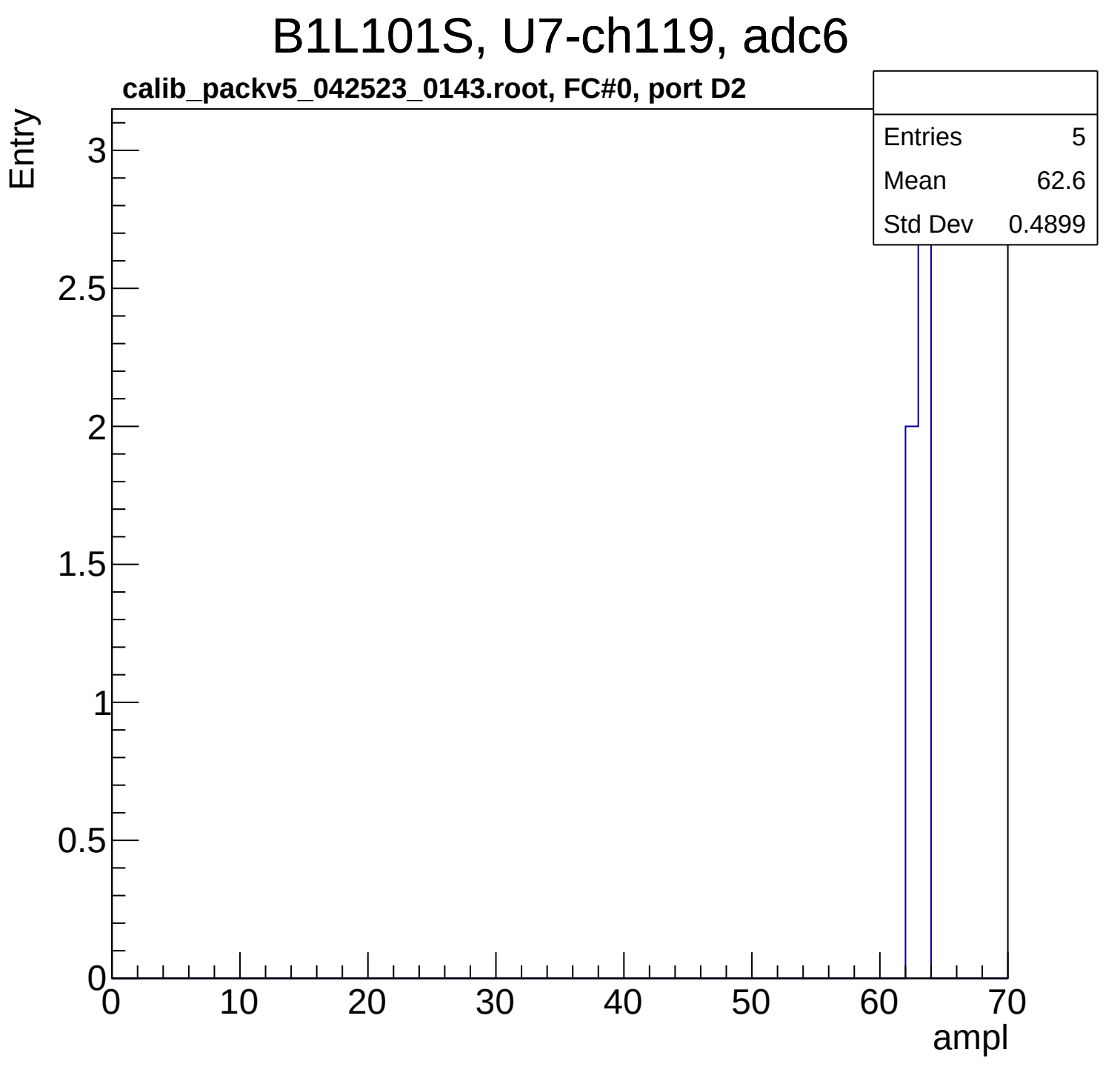
B1L101S, U7-ch119, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 62.6
Std Dev 0.4899
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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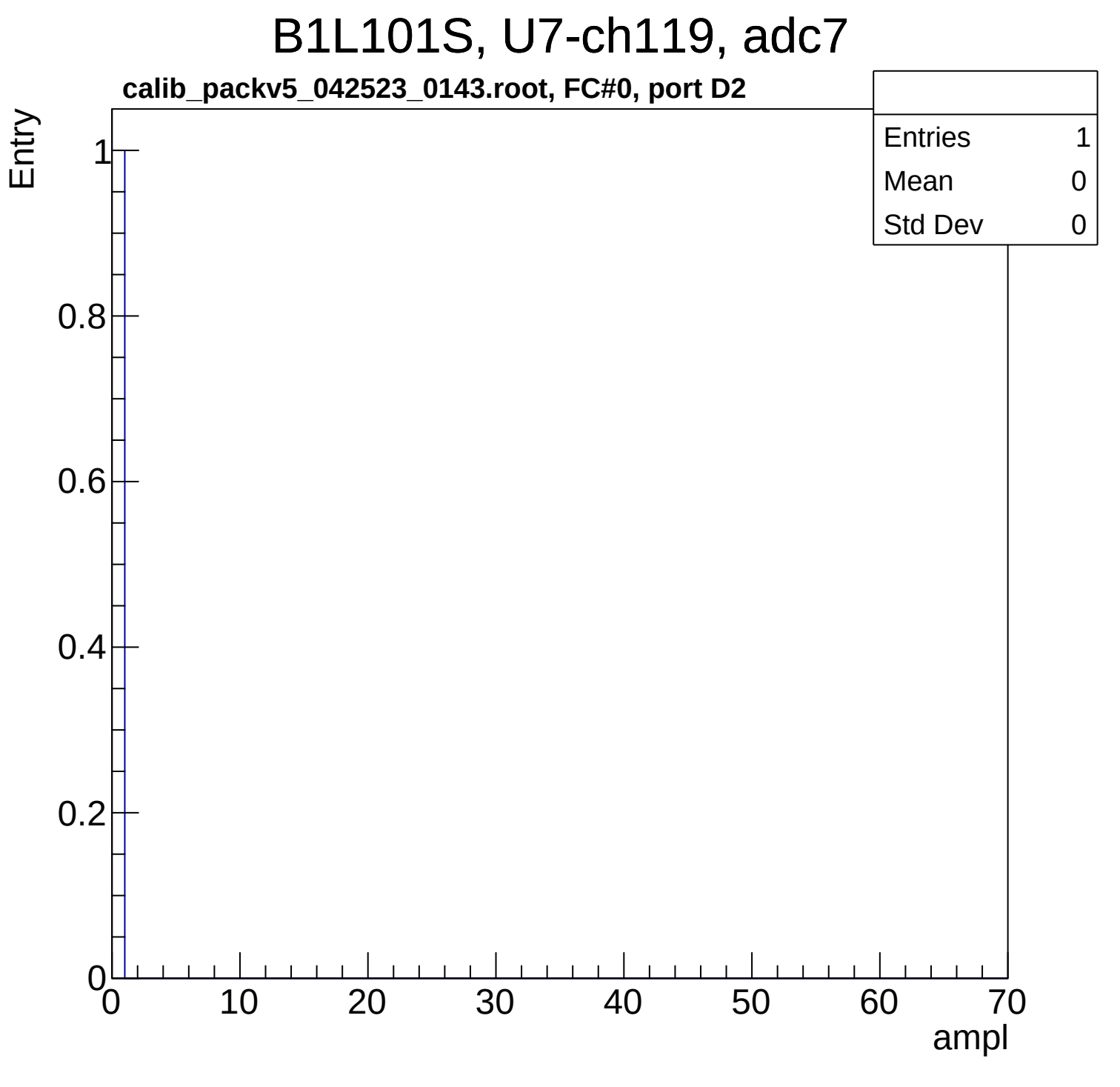
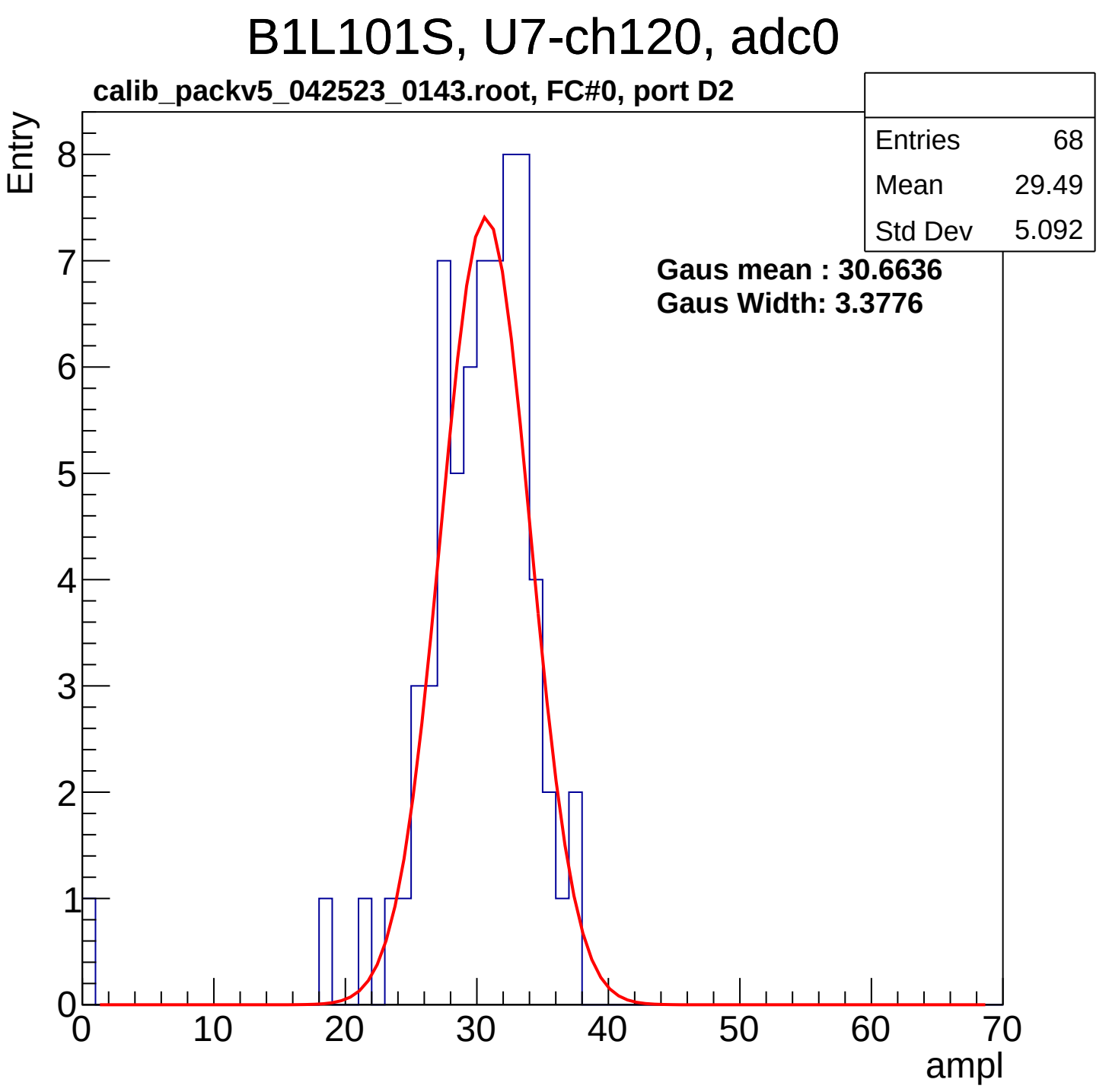
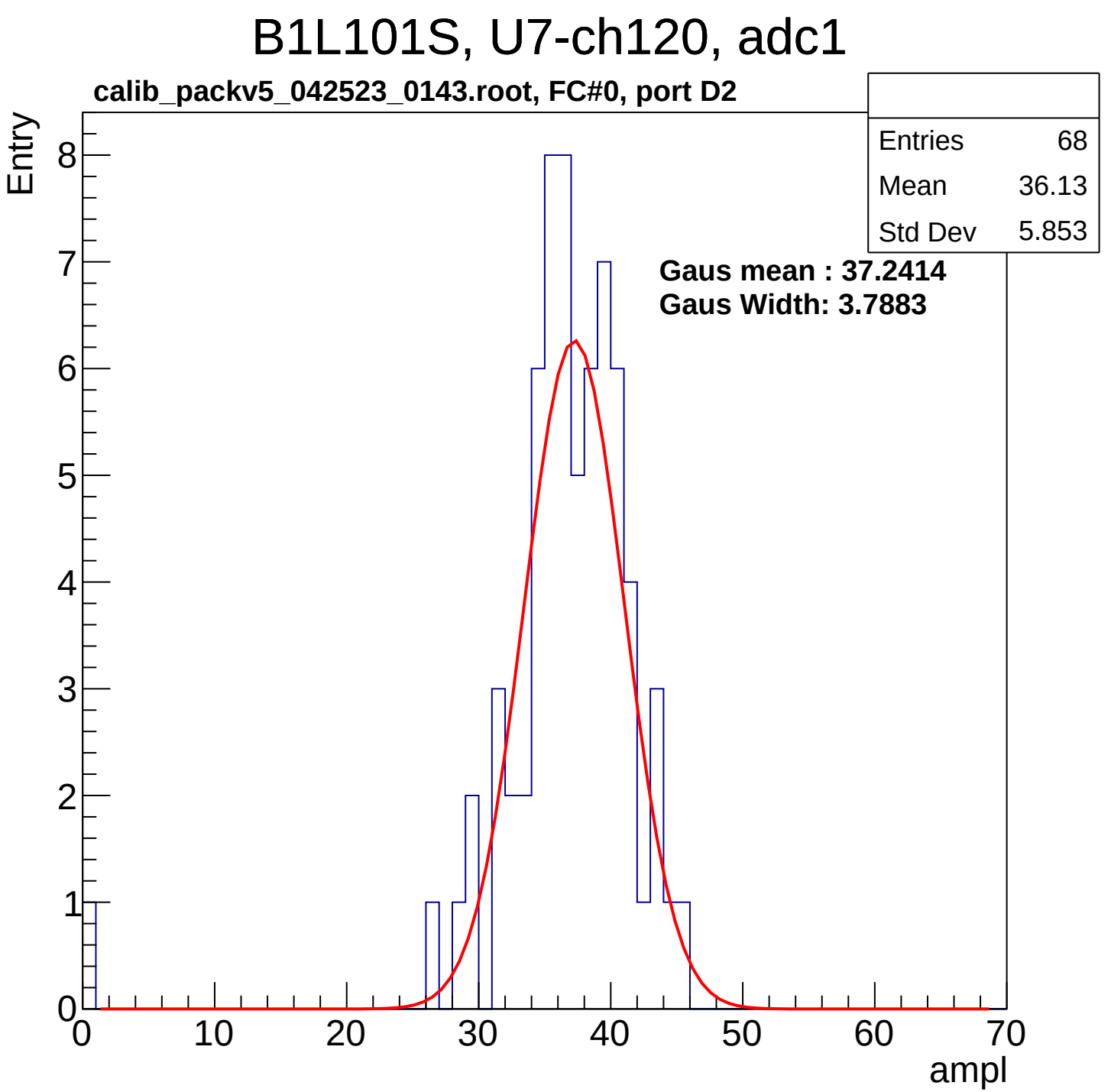

B1L101S, U7-ch119, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch120, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 29.49
Std Dev 5.092
Gaus mean : 30.6636
Gaus Width: 3.3776
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch120, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 36.13
Std Dev 5.853
Gaus mean : 37.2414
Gaus Width: 3.7883
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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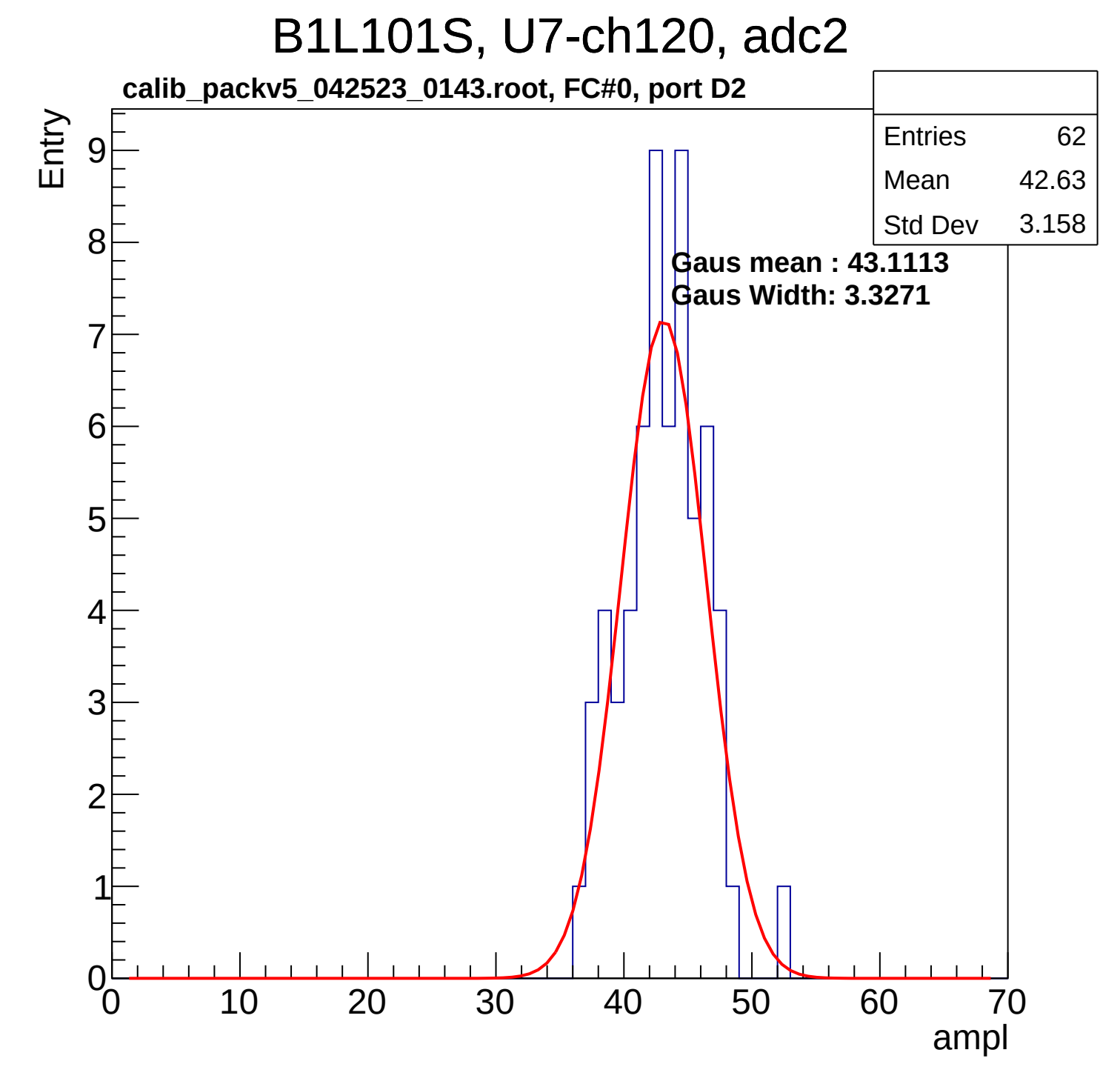
B1L101S, U7-ch120, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 42.63
Std Dev 3.158
Gaus mean : 43.1113
Gaus Width: 3.3271
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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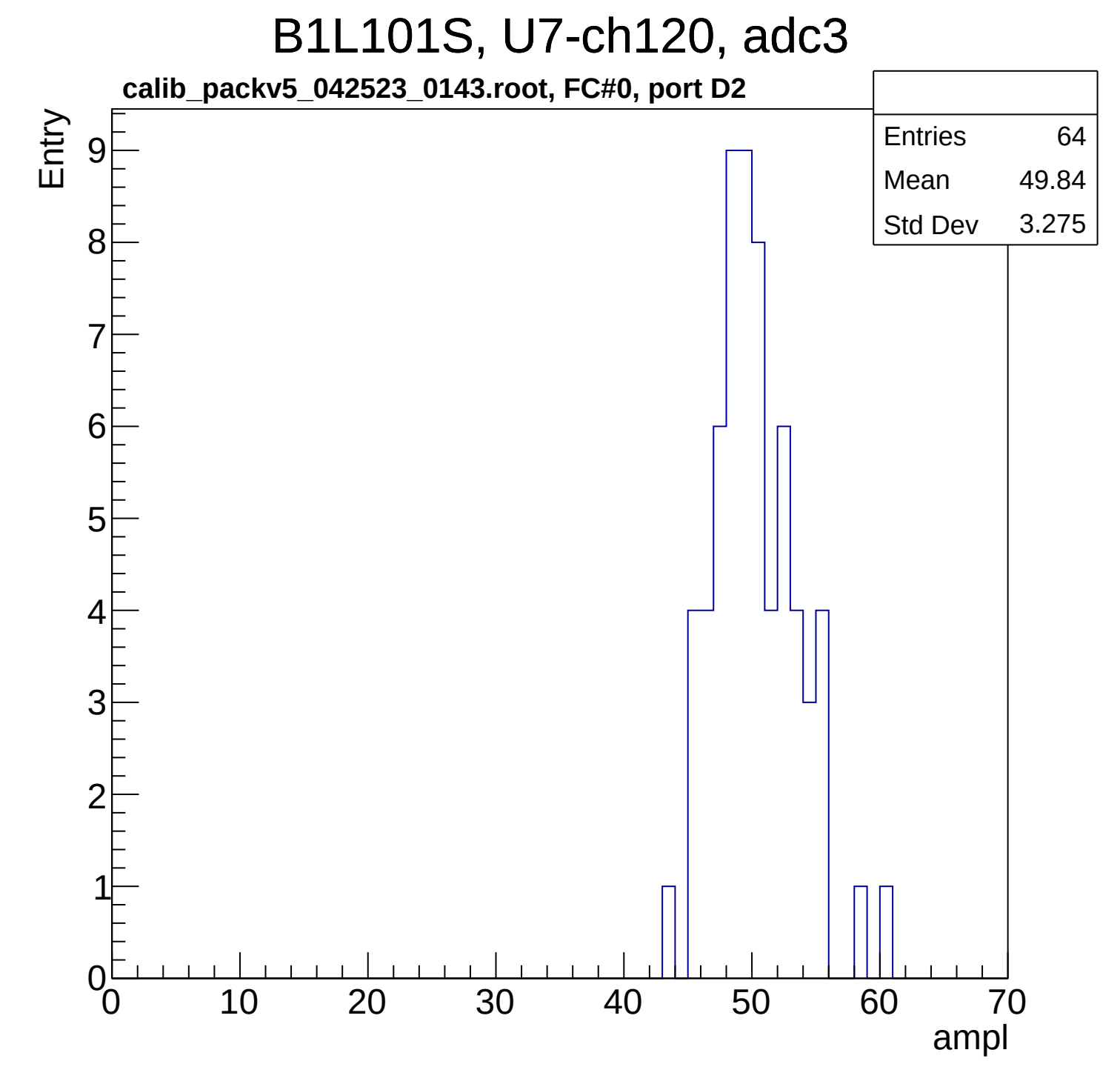
B1L101S, U7-ch120, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 49.84
Std Dev 3.275
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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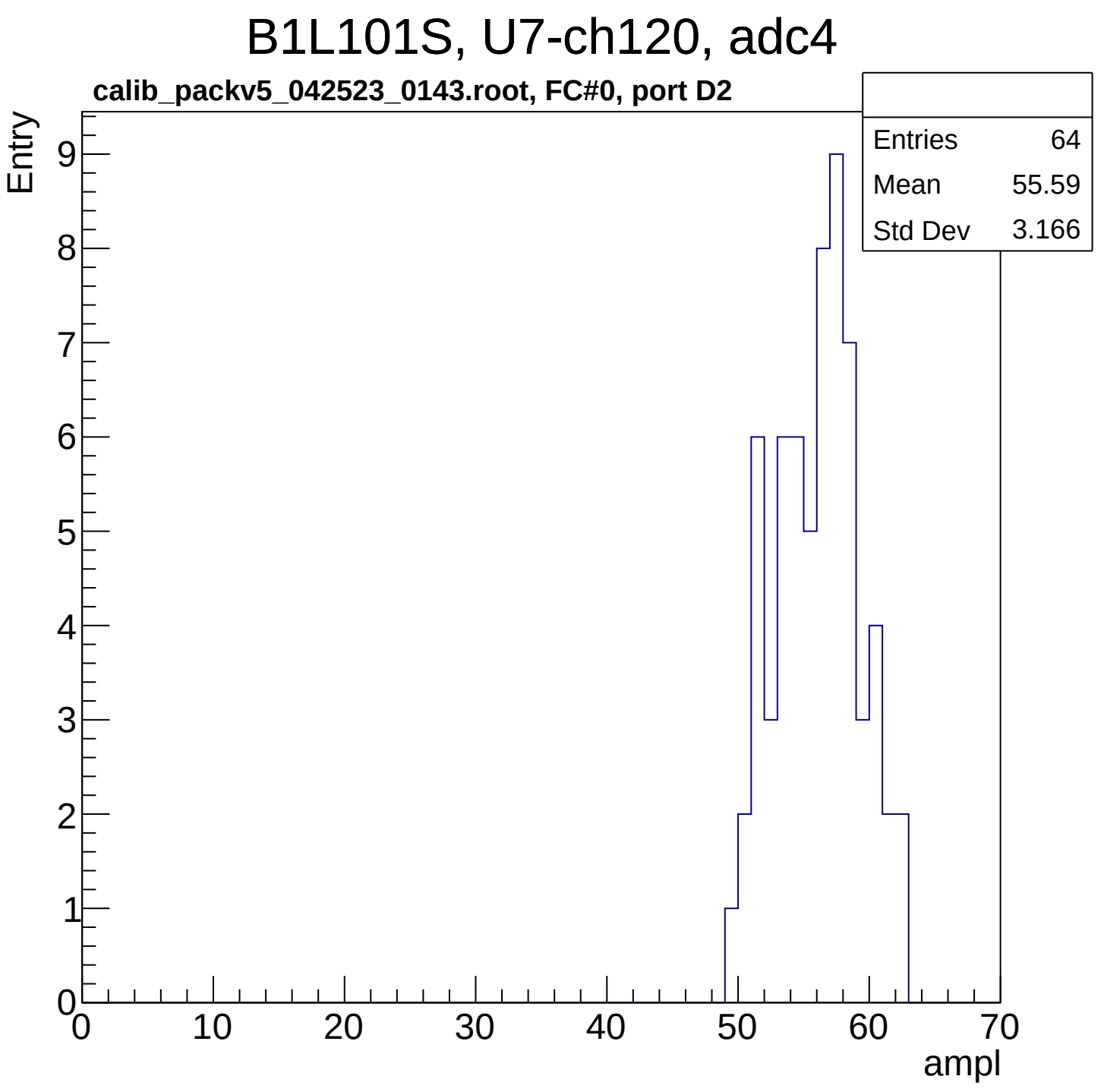
B1L101S, U7-ch120, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 55.59
Std Dev 3.166
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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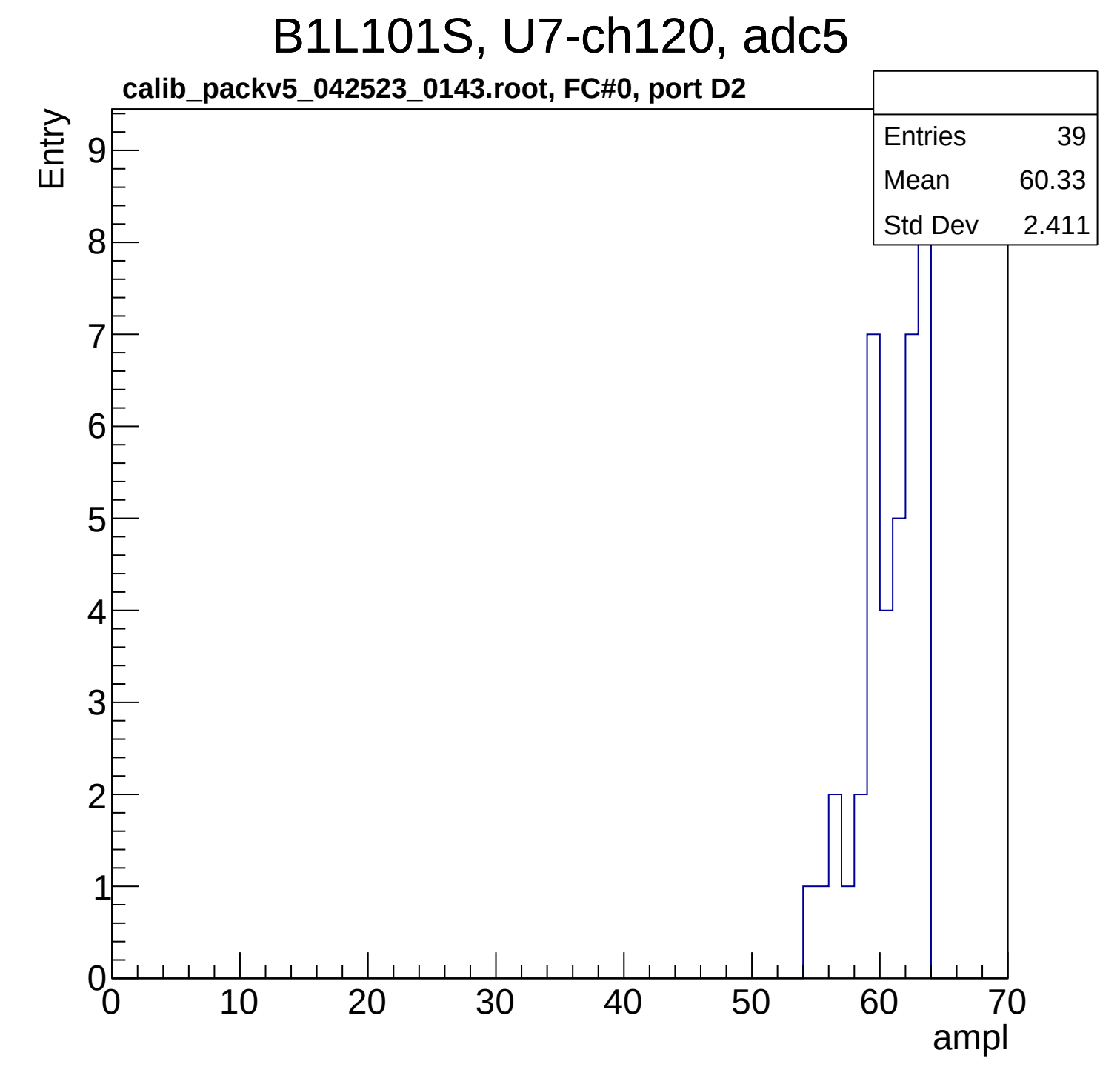
B1L101S, U7-ch120, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 39
Mean 60.33
Std Dev 2.411
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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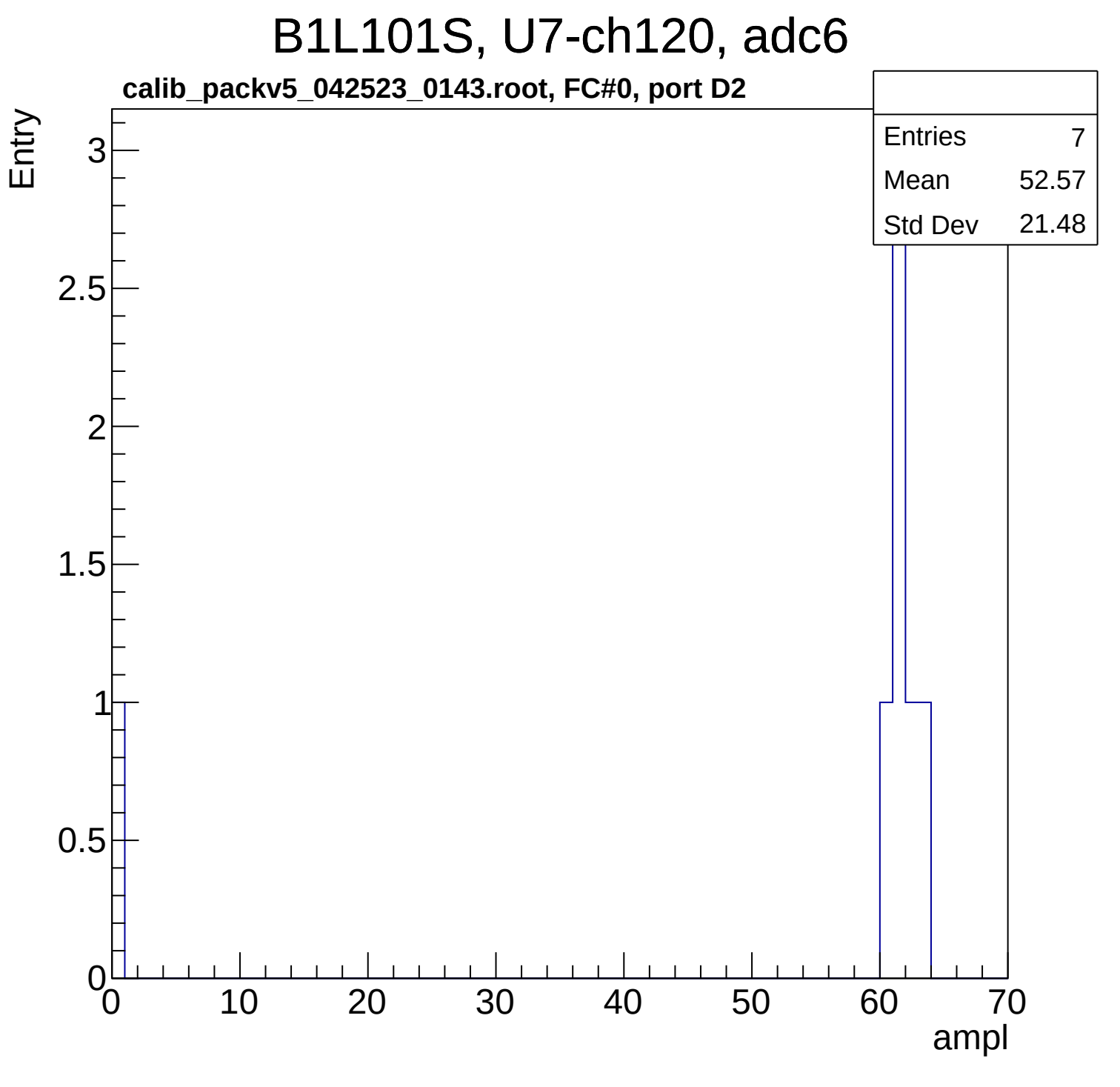
B1L101S, U7-ch120, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 52.57
Std Dev 21.48
Entry
ampl
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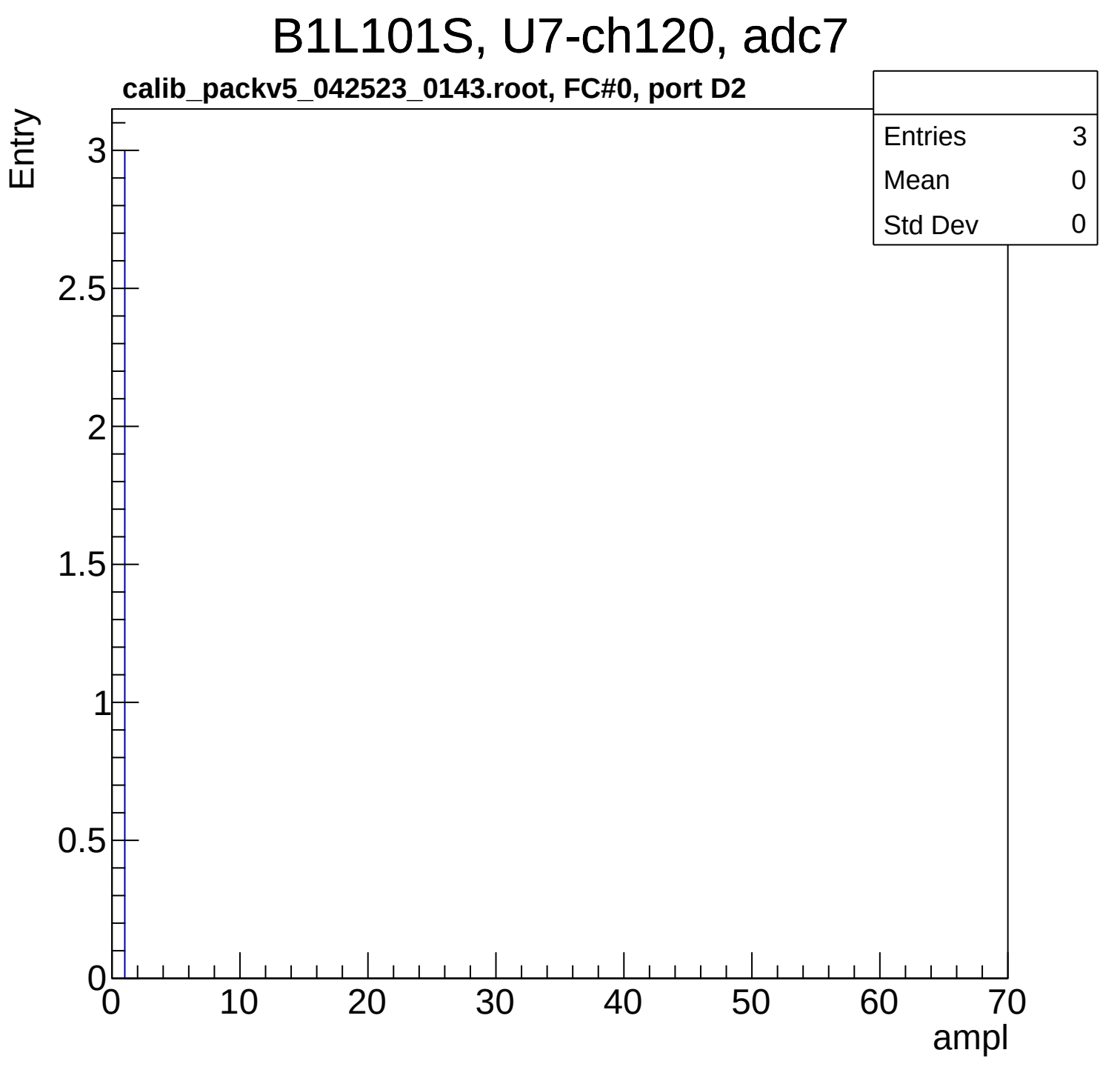
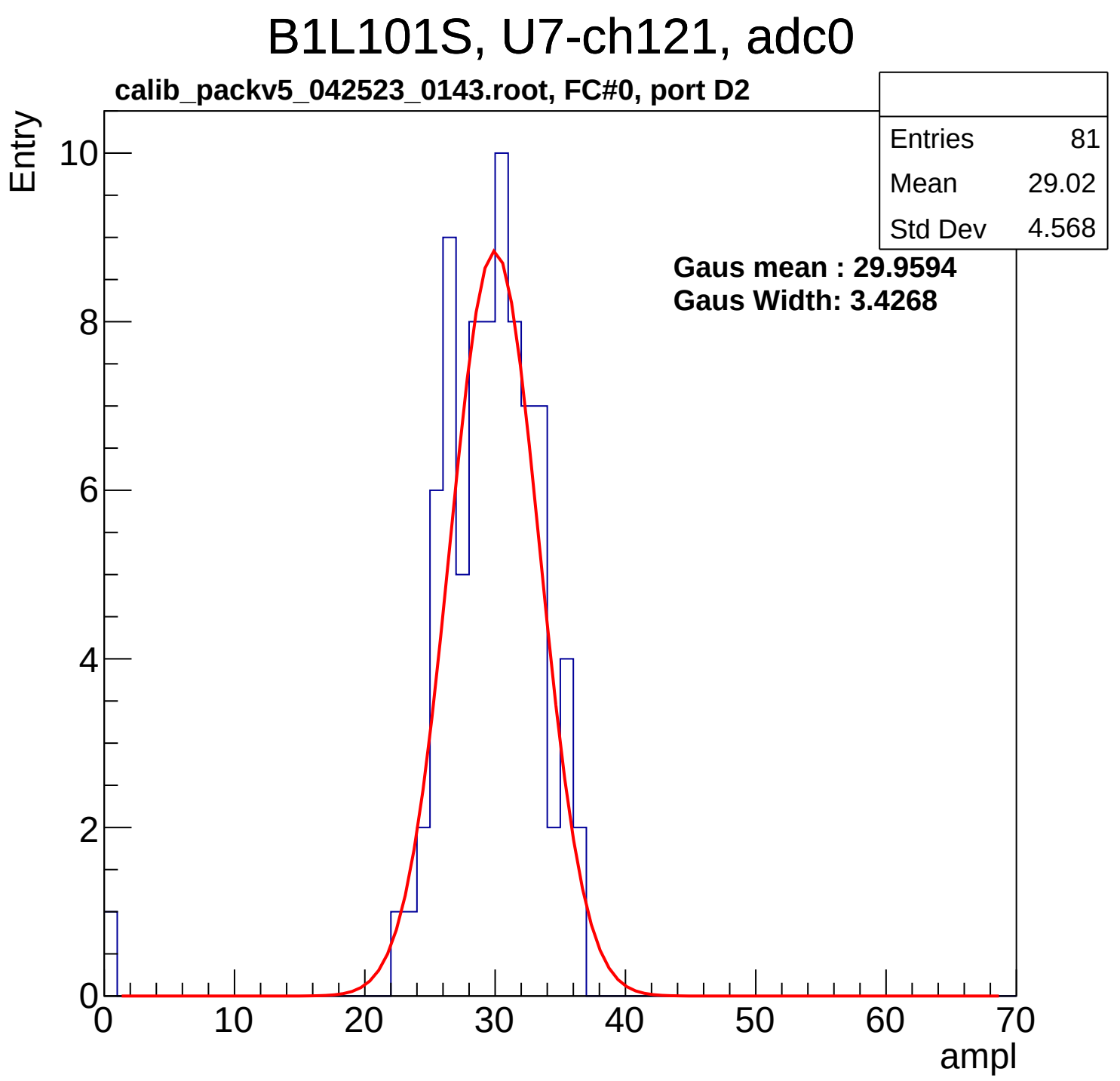
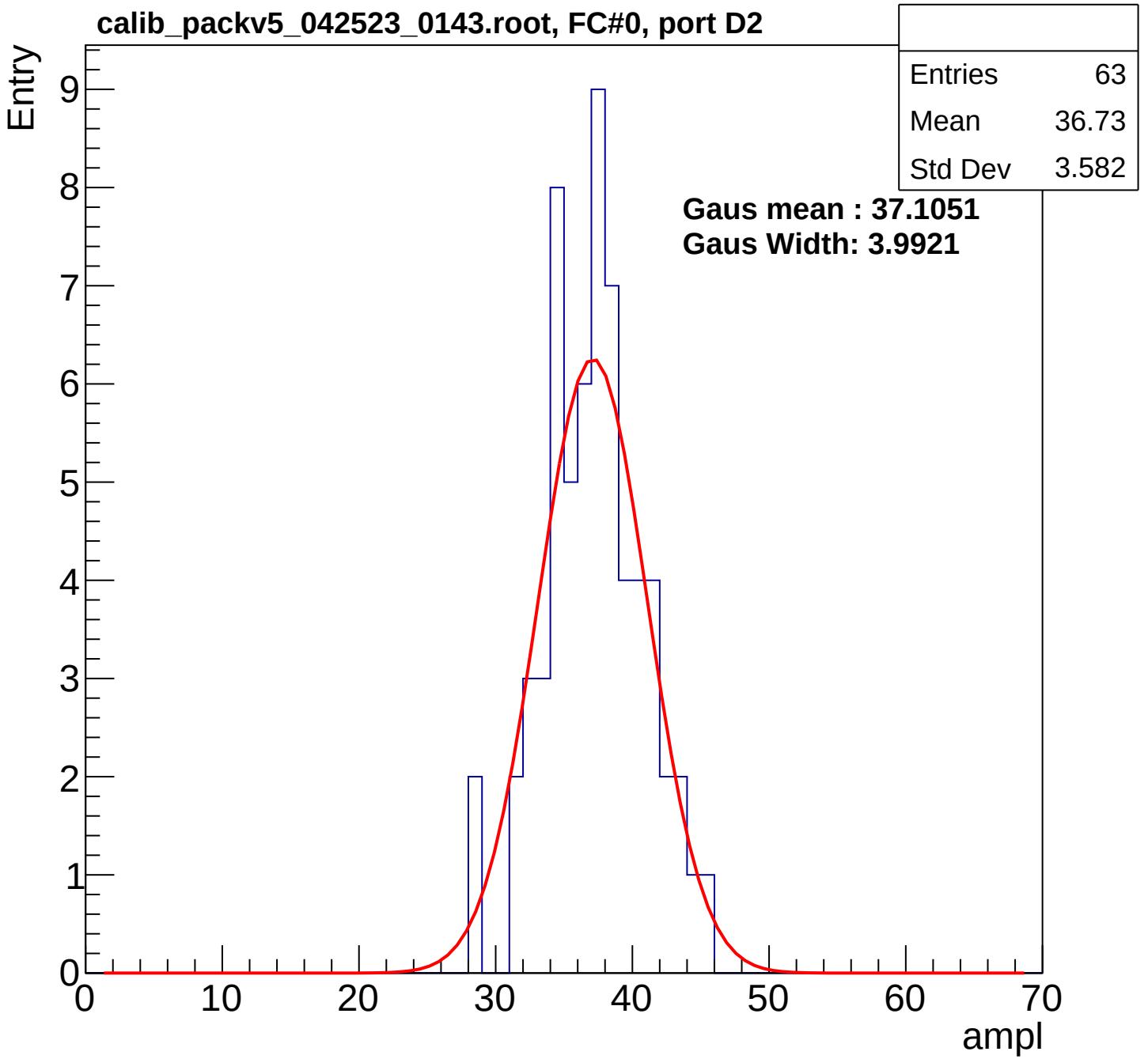
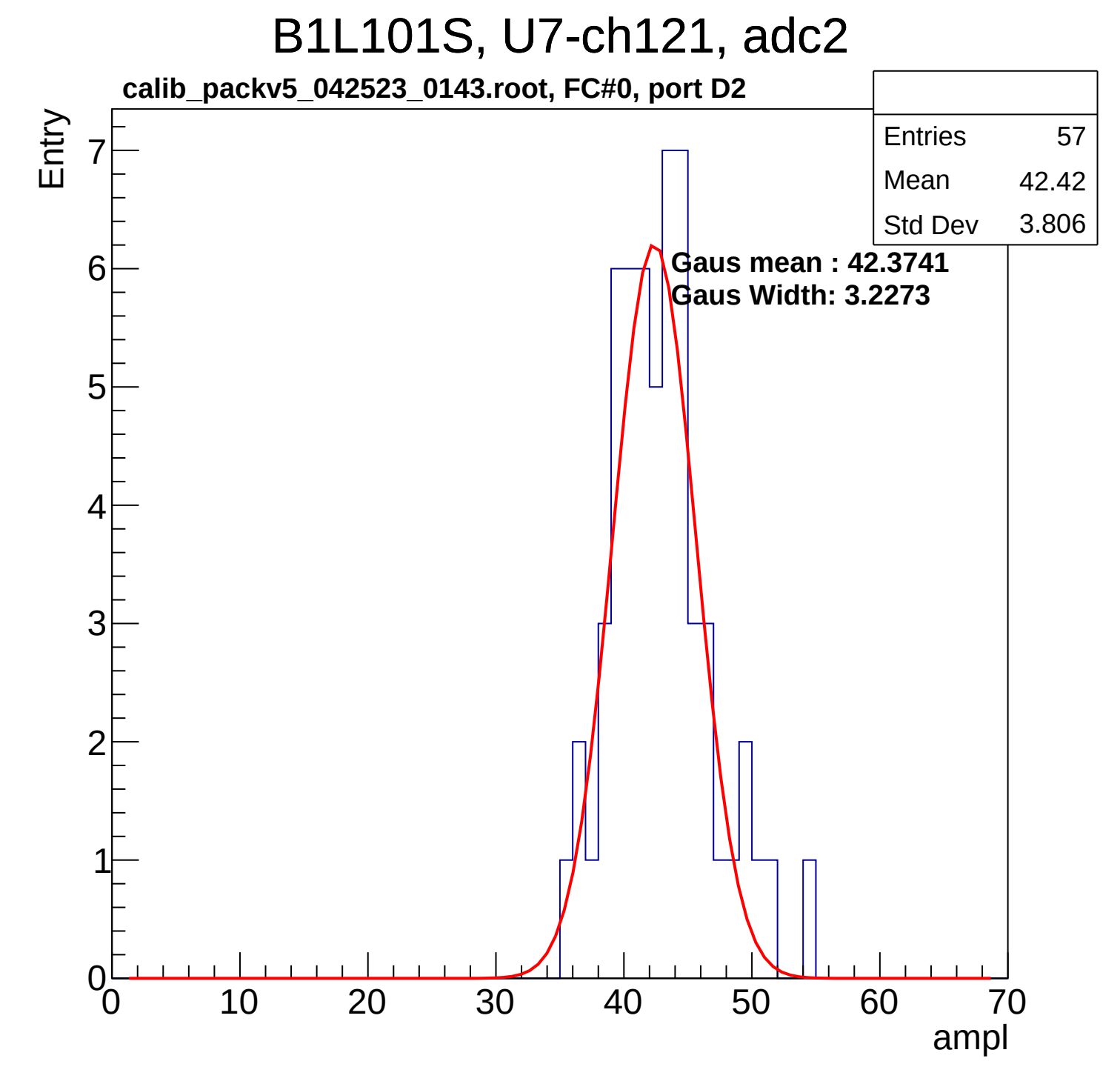
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U7-ch120, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 0
Std Dev 0
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch121, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 81
Mean 29.02
Std Dev 4.568
Gaus mean : 29.9594
Gaus Width: 3.4268
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch121, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 36.73
Std Dev 3.582
Gaus mean : 37.1051
Gaus Width: 3.9921
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch121, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 42.42
Std Dev 3.806
Gaus mean : 42.3741
Gaus Width: 3.2273
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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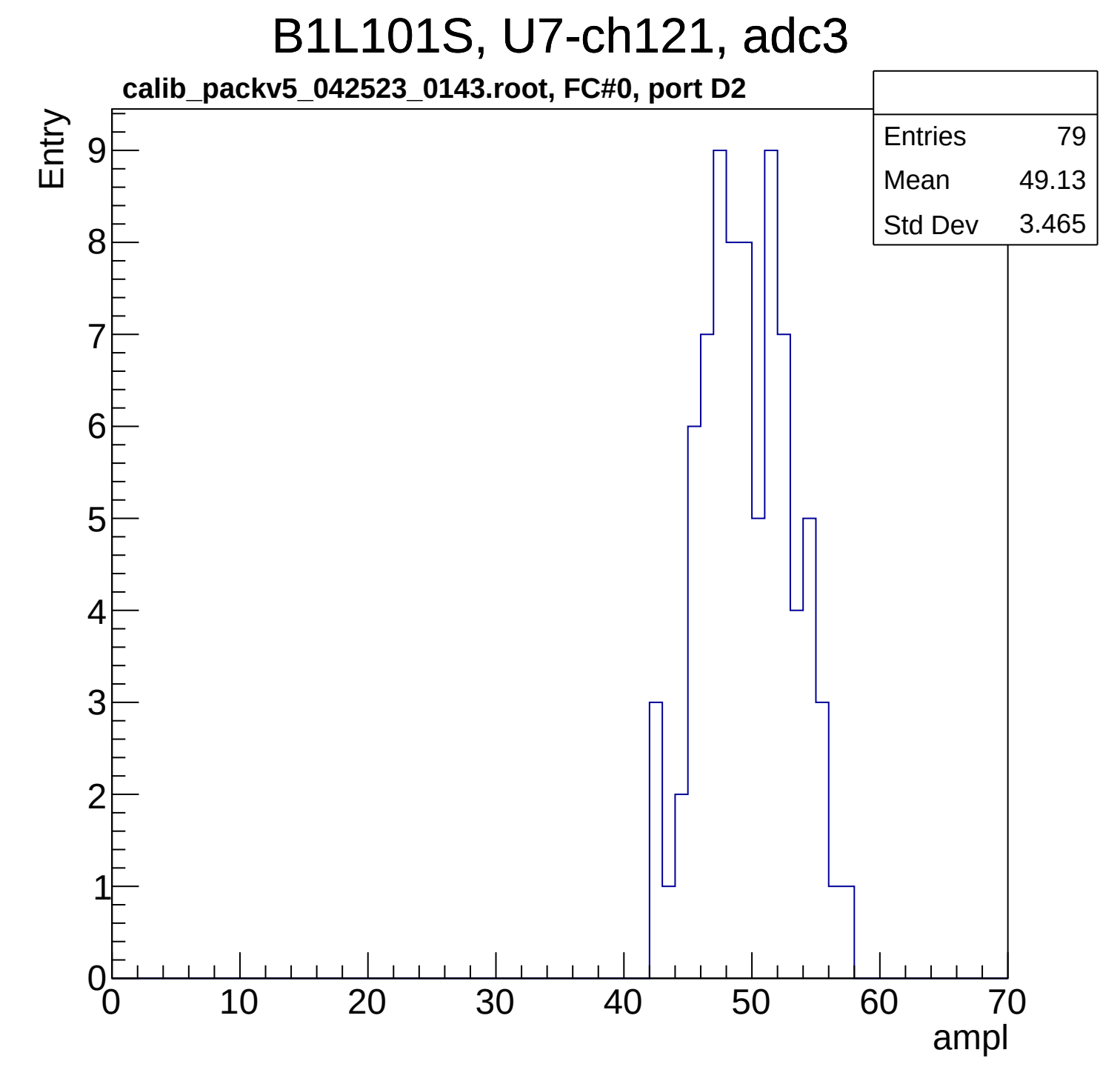
B1L101S, U7-ch121, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 49.13
Std Dev 3.465
Entry
ampl
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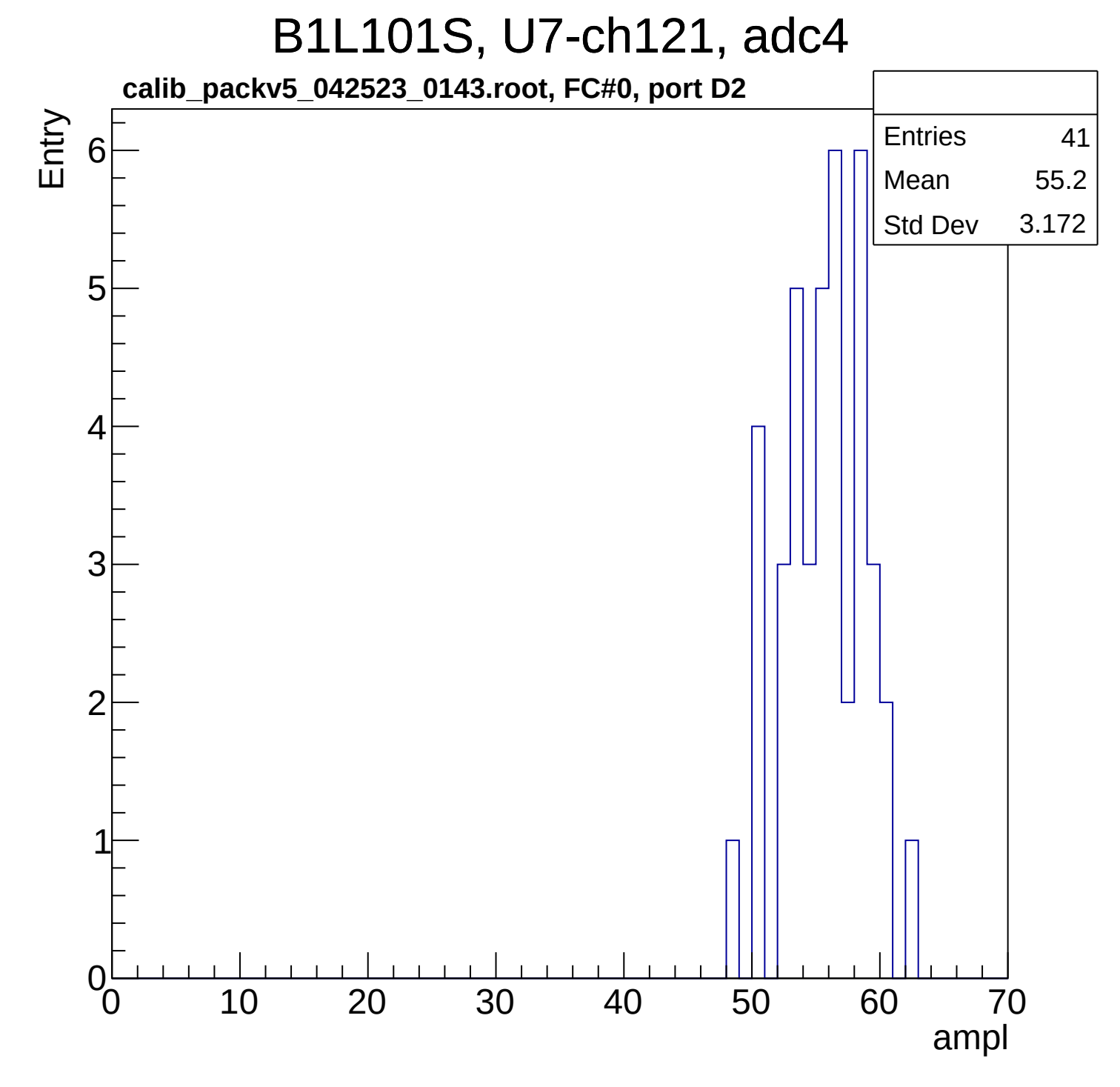
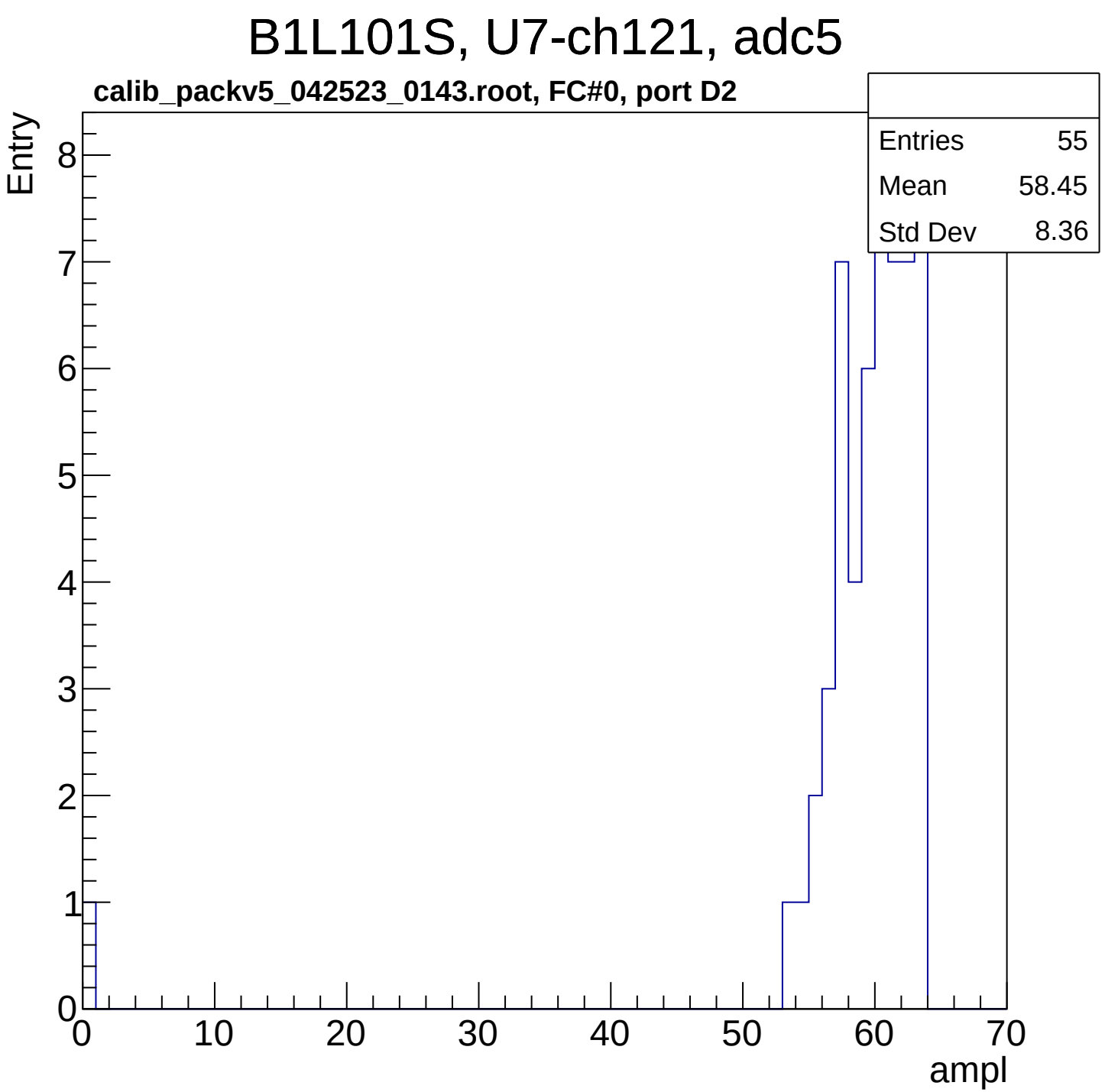
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch121, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 41
Mean 55.2
Std Dev 3.172
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L101S, U7-ch121, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 58.45
Std Dev 8.36
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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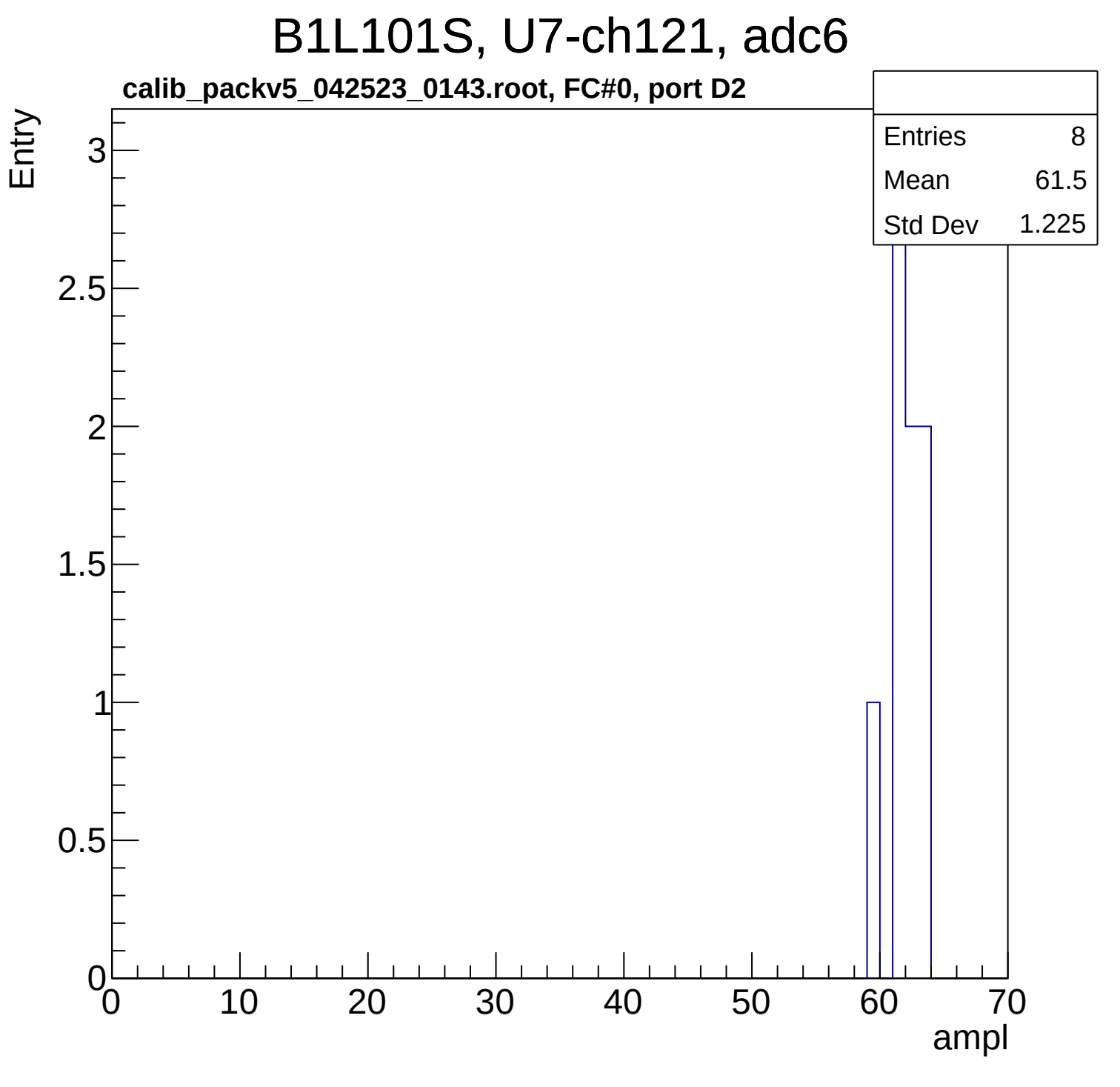
B1L101S, U7-ch121, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 61.5
Std Dev 1.225
Entry
ampl
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0.5
1
1.5
2
2.5
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0
10
20
30
40
50
60
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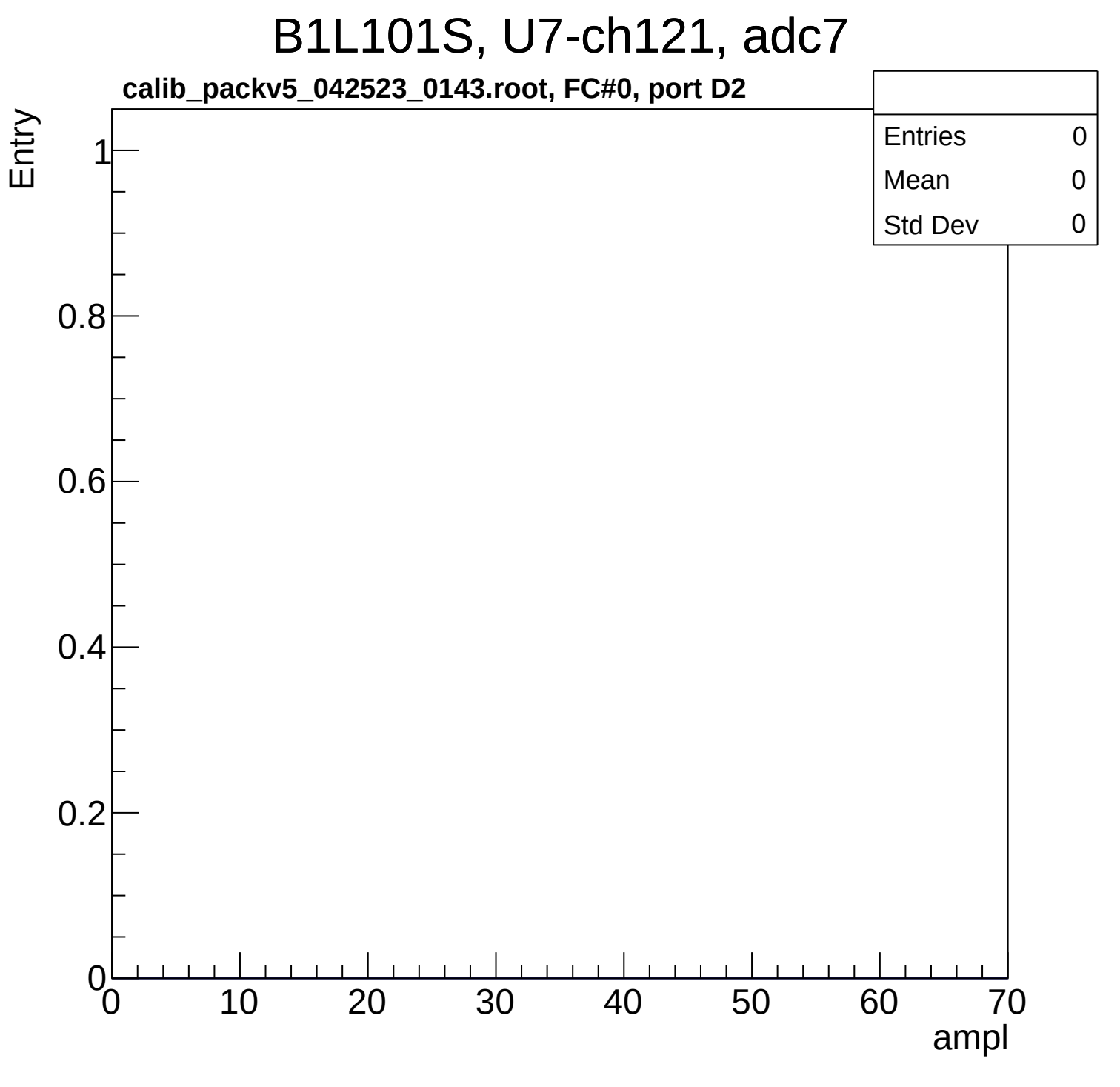
B1L101S, U7-ch121, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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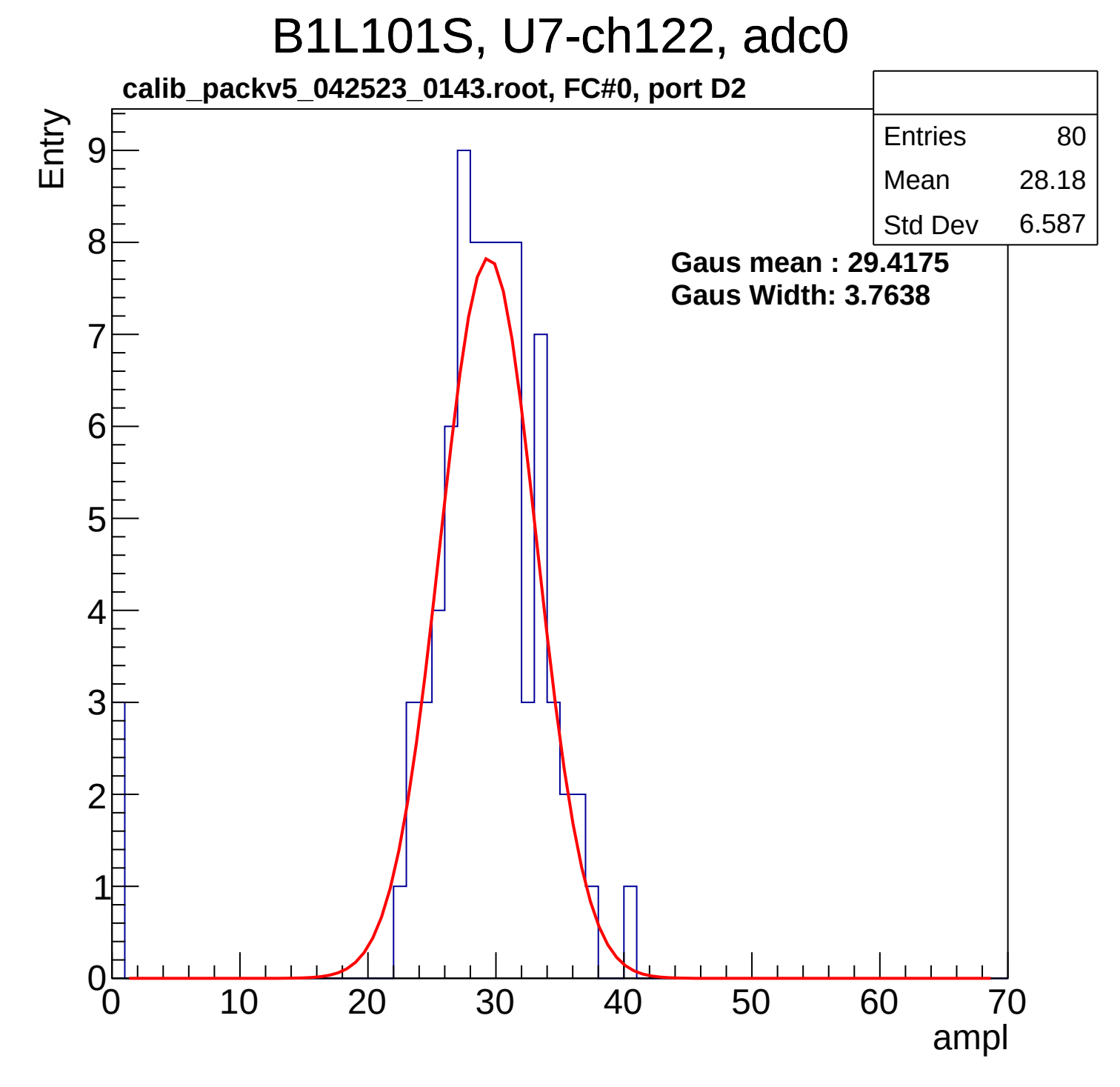
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch122, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 80
Mean 28.18
Std Dev 6.587
Gaus mean : 29.4175
Gaus Width: 3.7638
Entry
ampl
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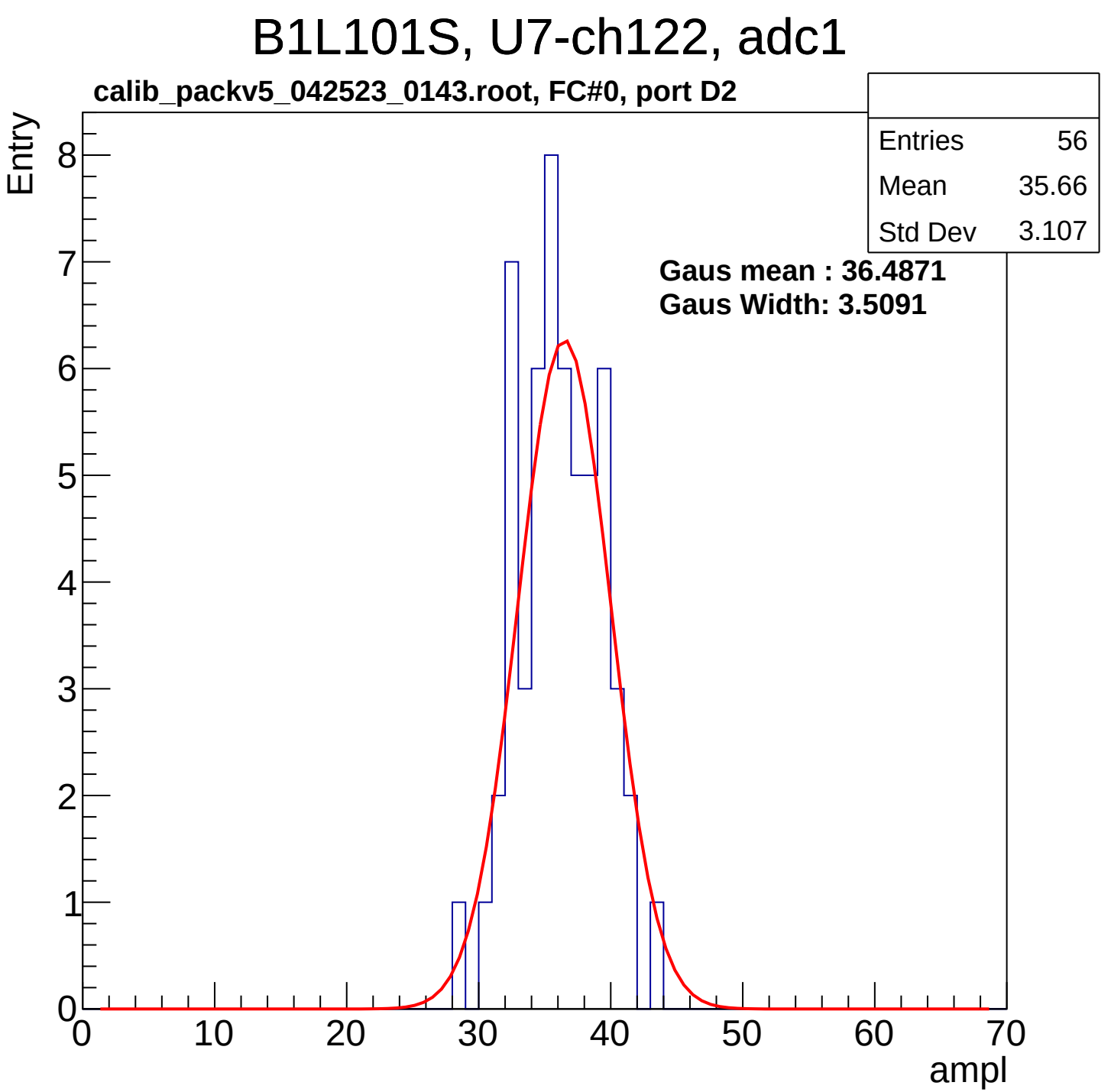
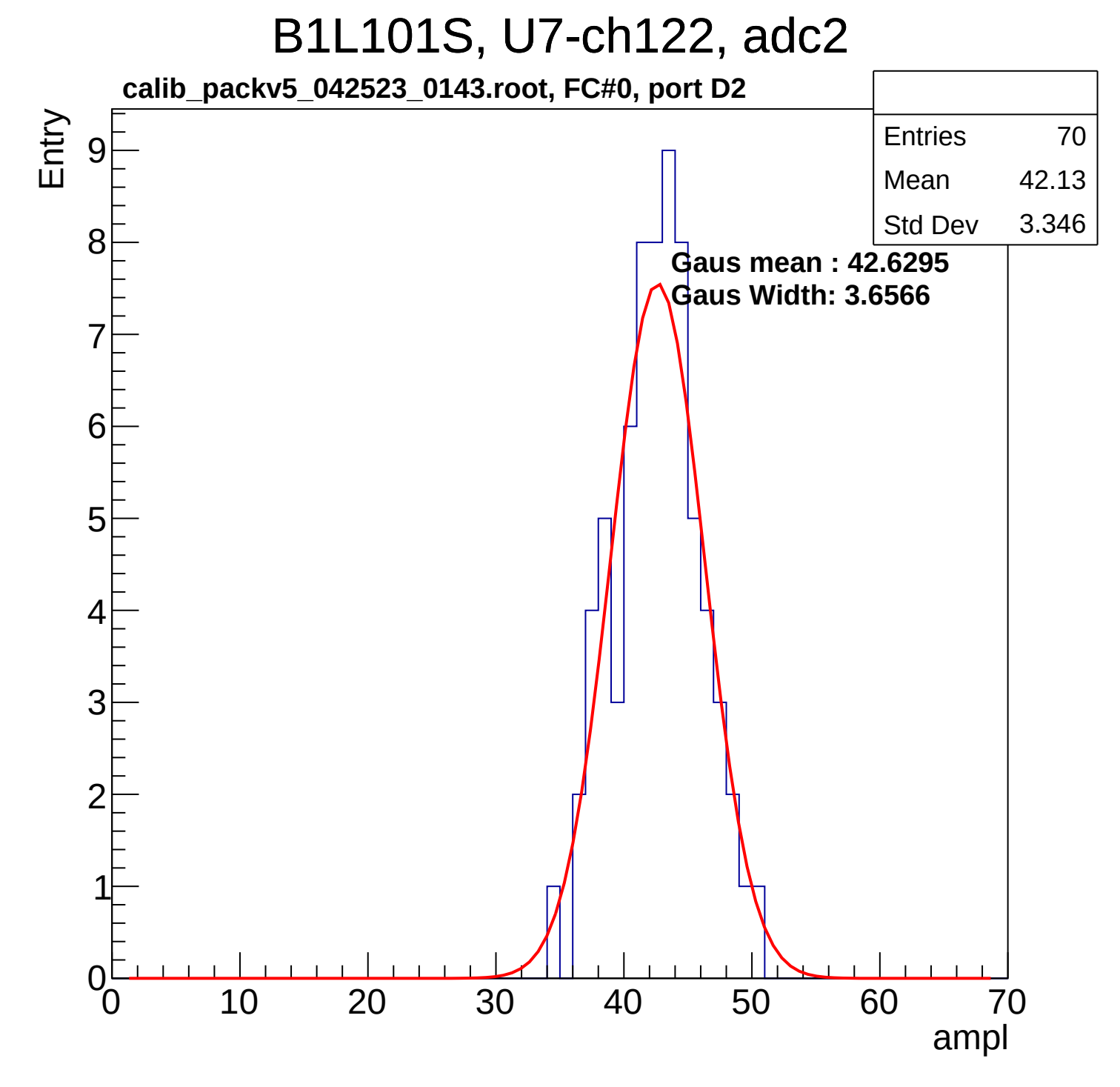
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch122, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 35.66
Std Dev 3.107
Gaus mean : 36.4871
Gaus Width: 3.5091
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch122, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 42.13
Std Dev 3.346
Gaus mean : 42.6295
Gaus Width: 3.6566
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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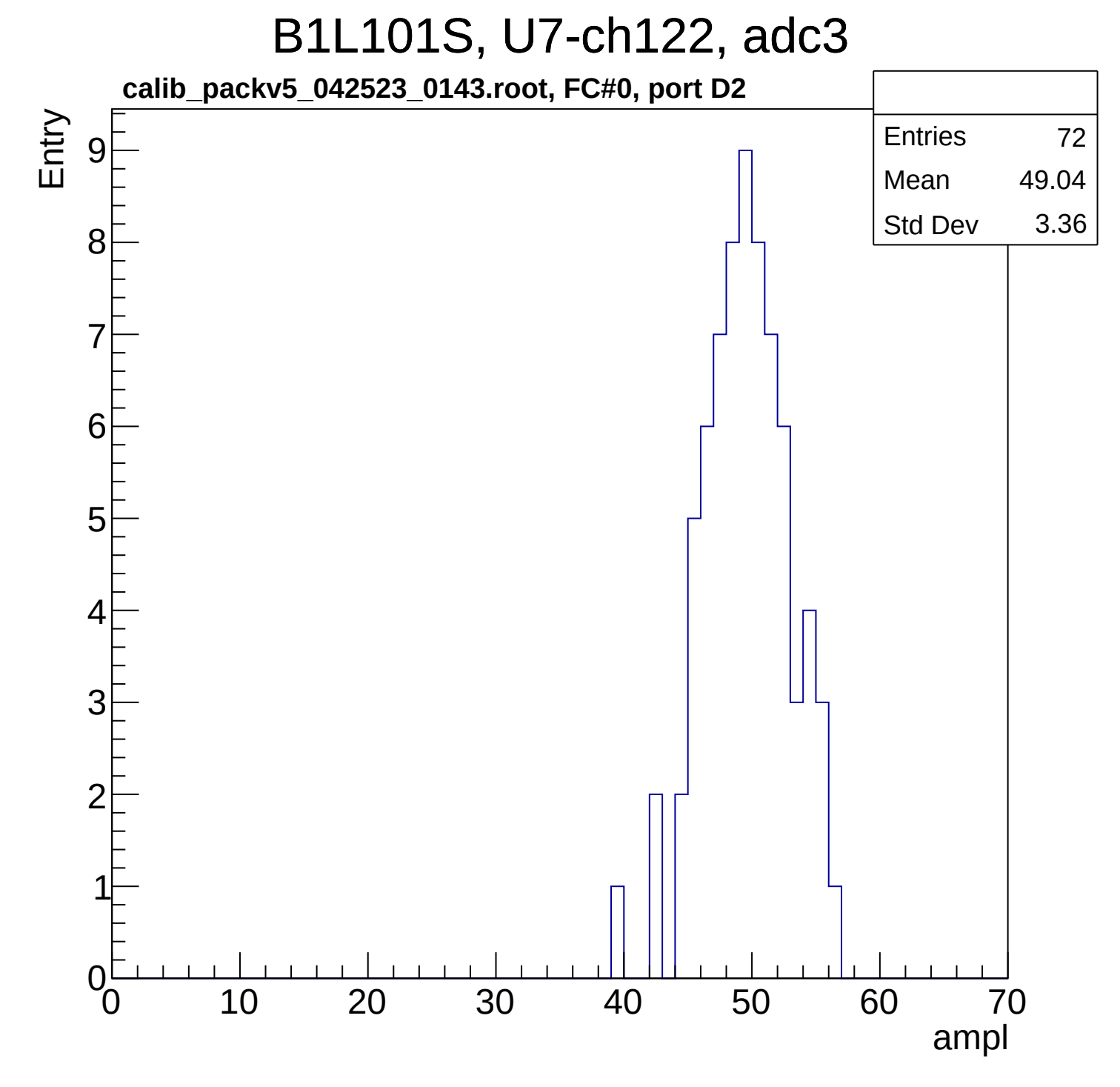
40
50
60
70


B1L101S, U7-ch122, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 49.04
Std Dev 3.36
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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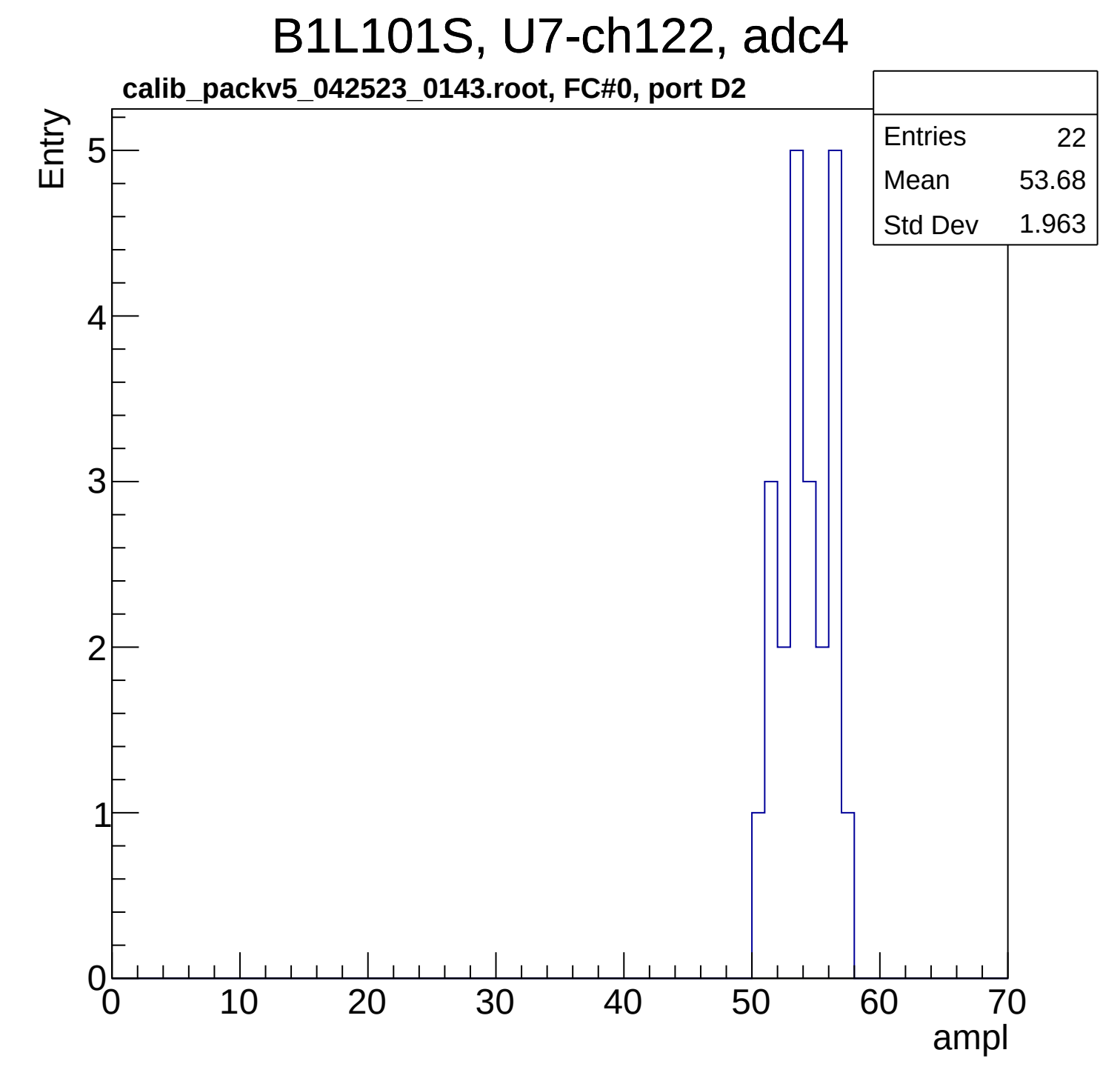
B1L101S, U7-ch122, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 22
Mean 53.68
Std Dev 1.963
Entry
ampl
0
1
2
3
4
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0
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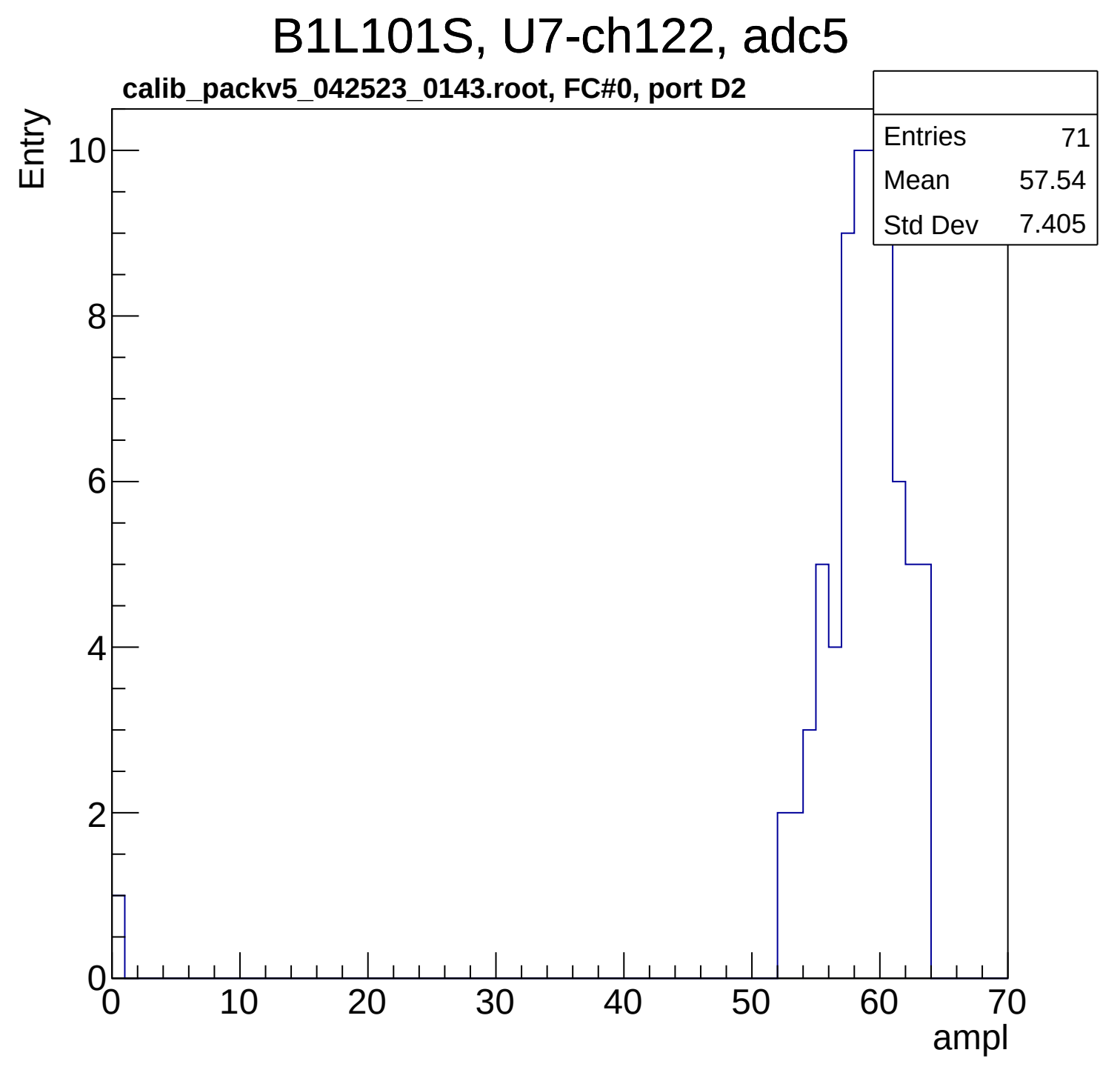
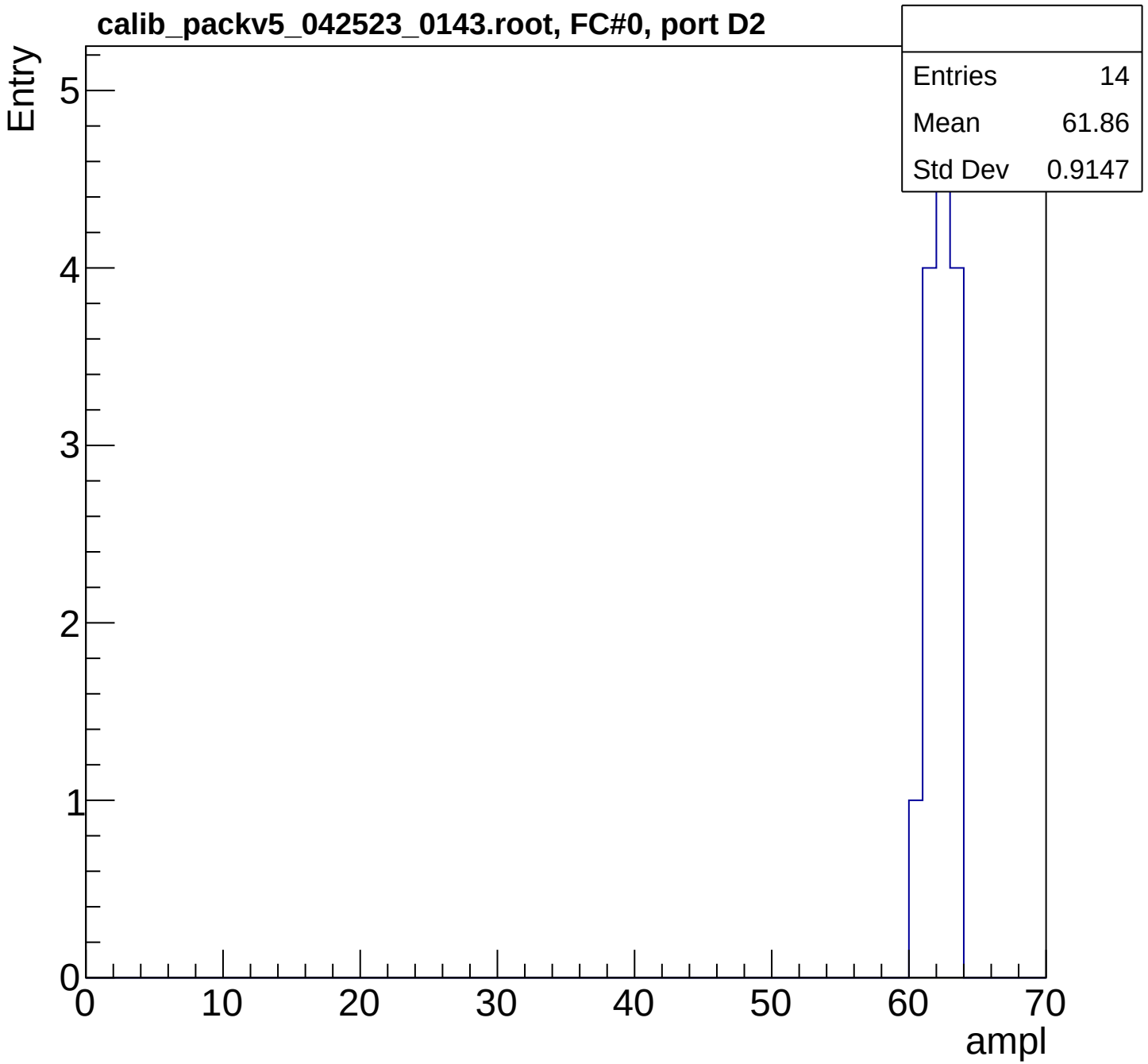
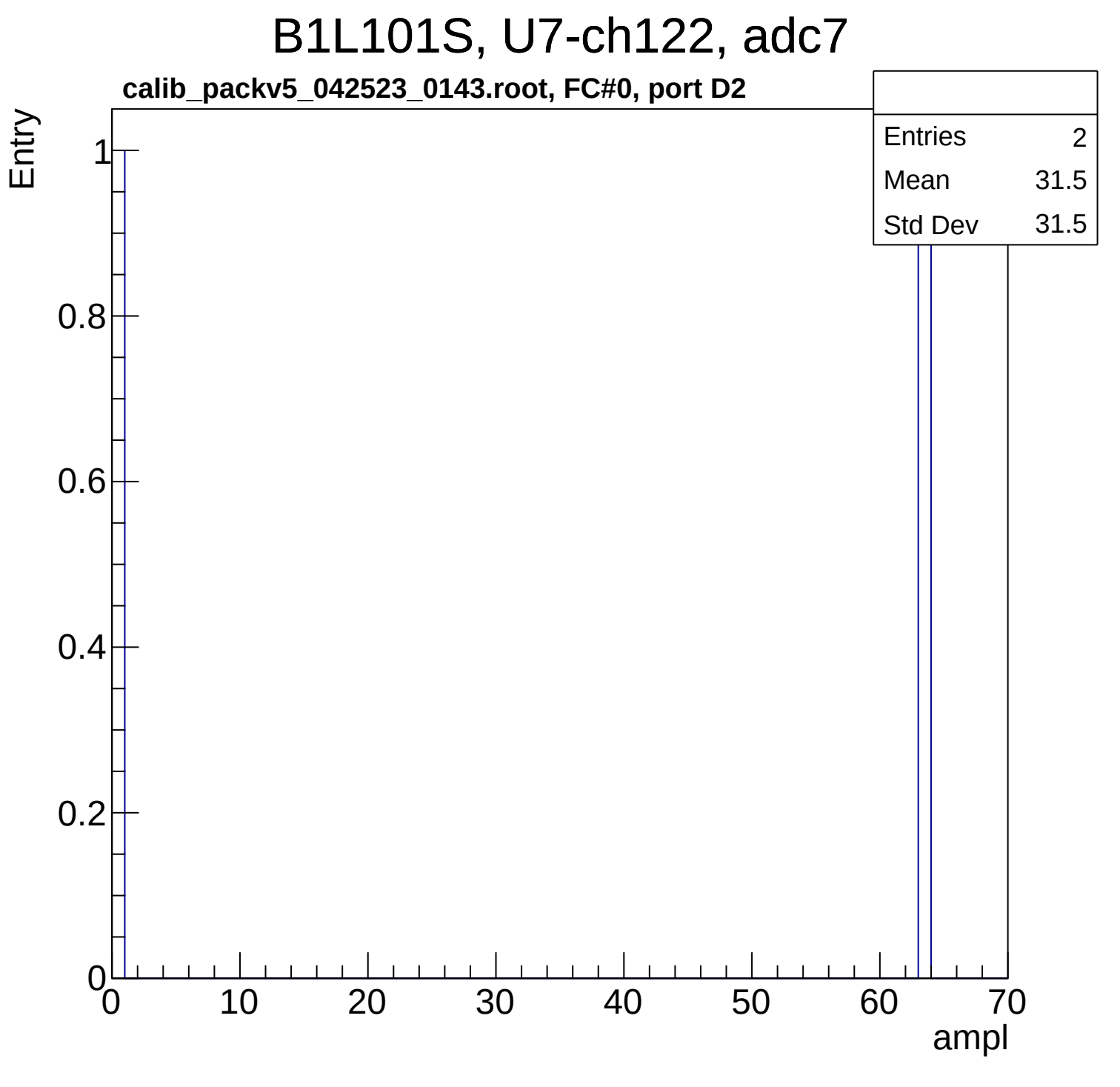
40
50
60
70


B1L101S, U7-ch122, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 57.54
Std Dev 7.405
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch122, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 14
Mean 61.86
Std Dev 0.9147
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch122, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
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0.6
0.4
0.2
0
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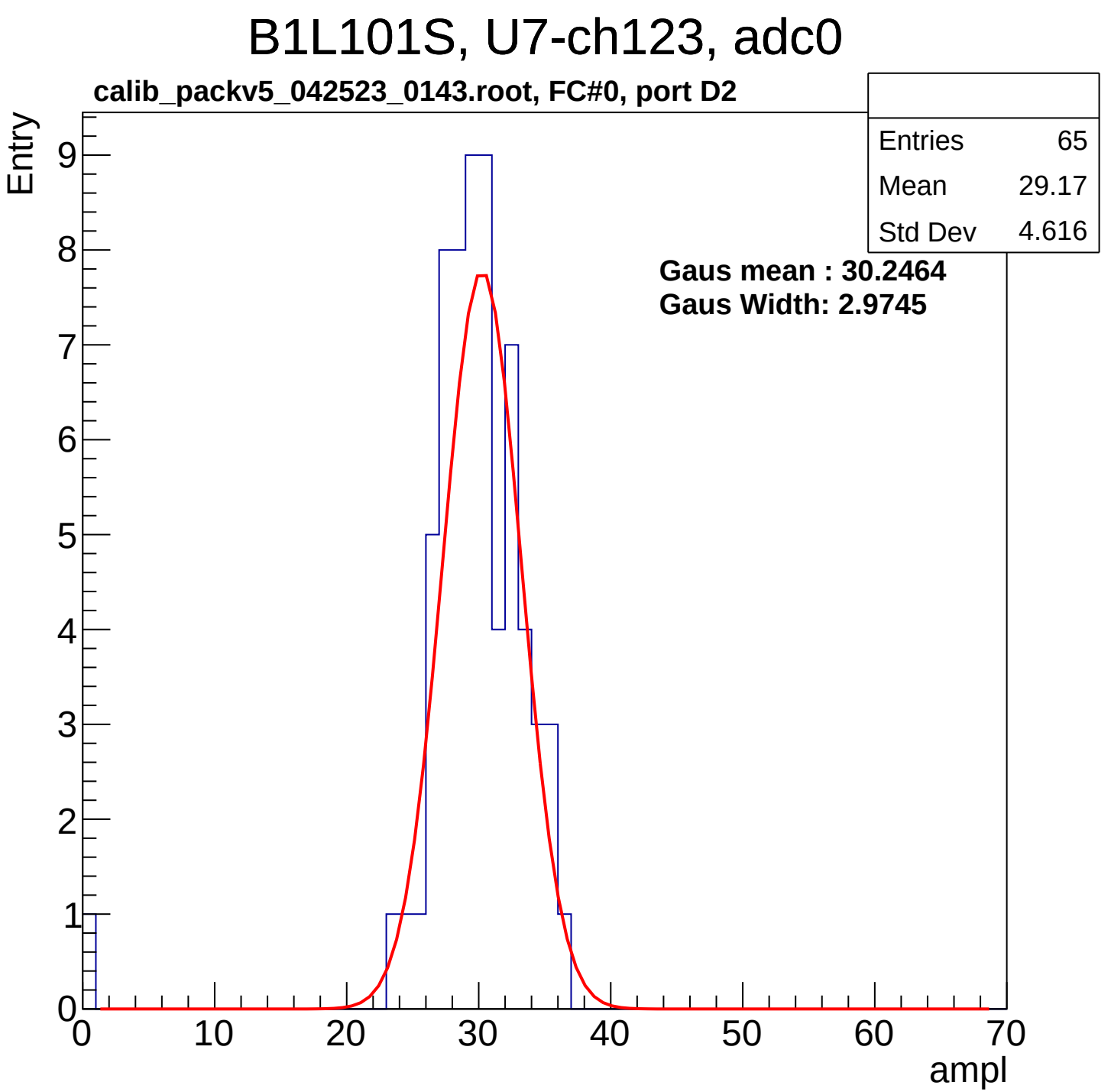
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch123, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 29.17
Std Dev 4.616
Gaus mean : 30.2464
Gaus Width: 2.9745
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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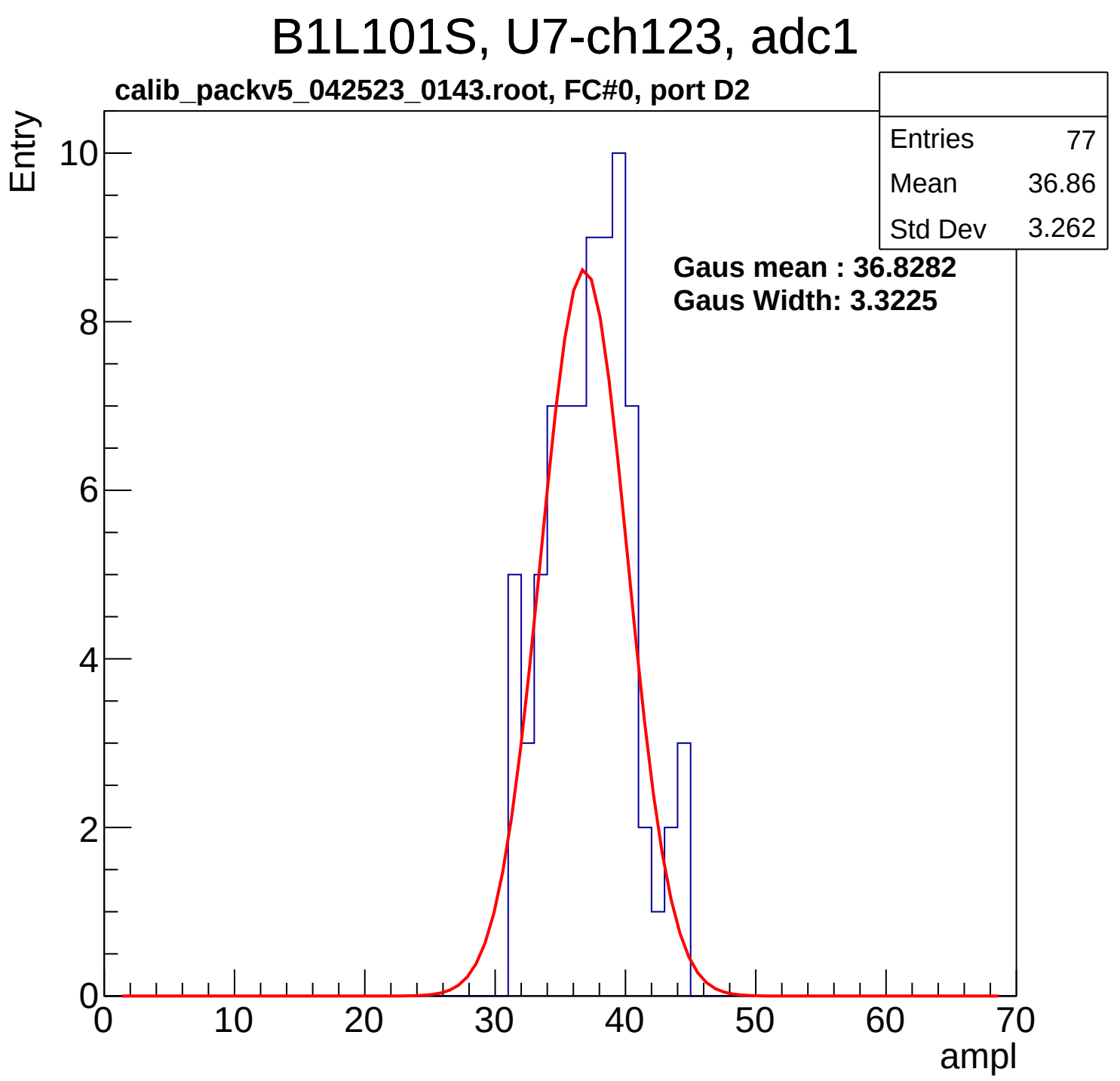
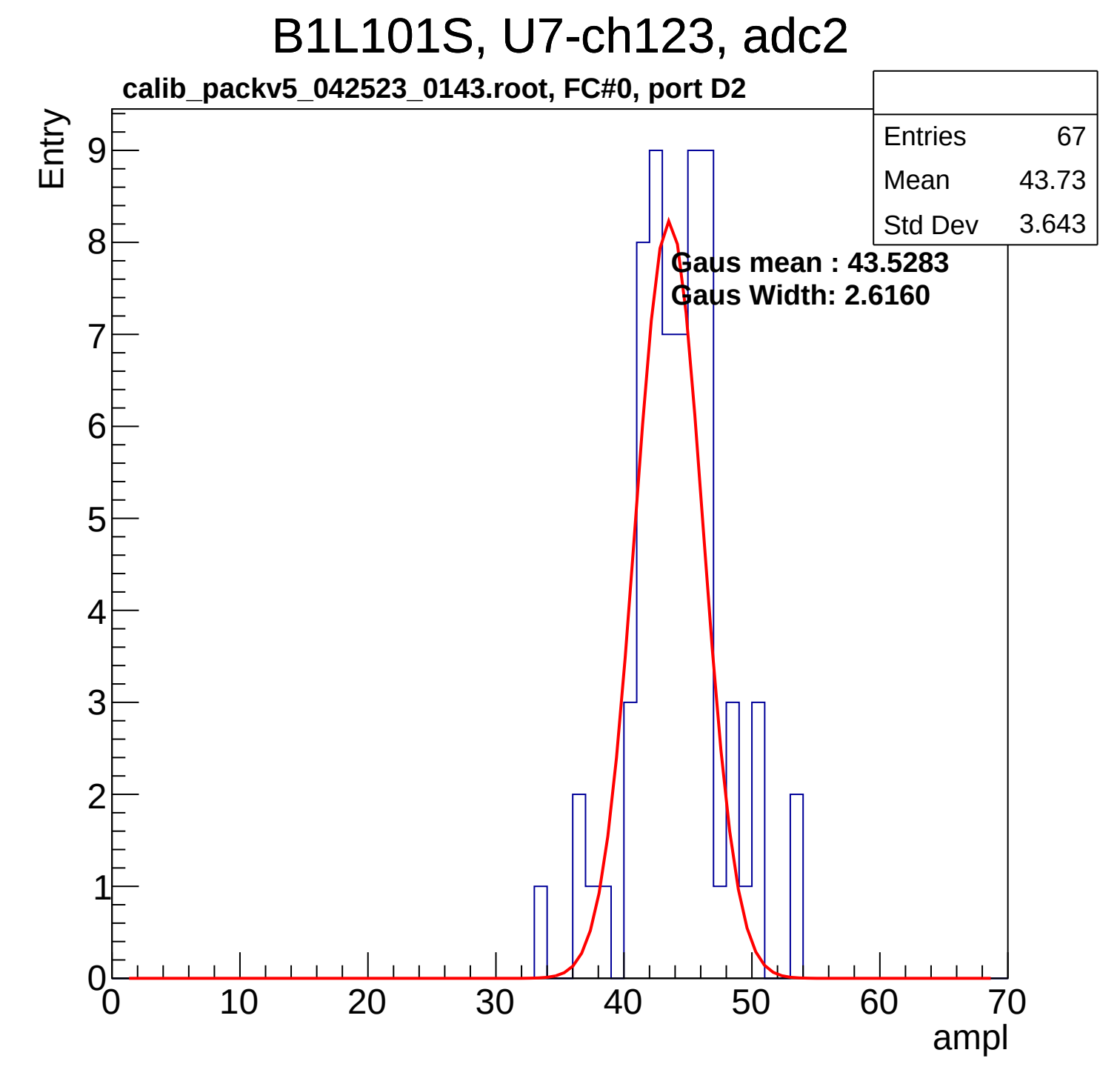

B1L101S, U7-ch123, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 36.86
Std Dev 3.262
Gaus mean : 36.8282
Gaus Width: 3.3225
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch123, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 43.73
Std Dev 3.643
Gaus mean : 43.5283
Gaus Width: 2.6160
Entry
ampl
0
1
2
3
4
5
6
7
8
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0
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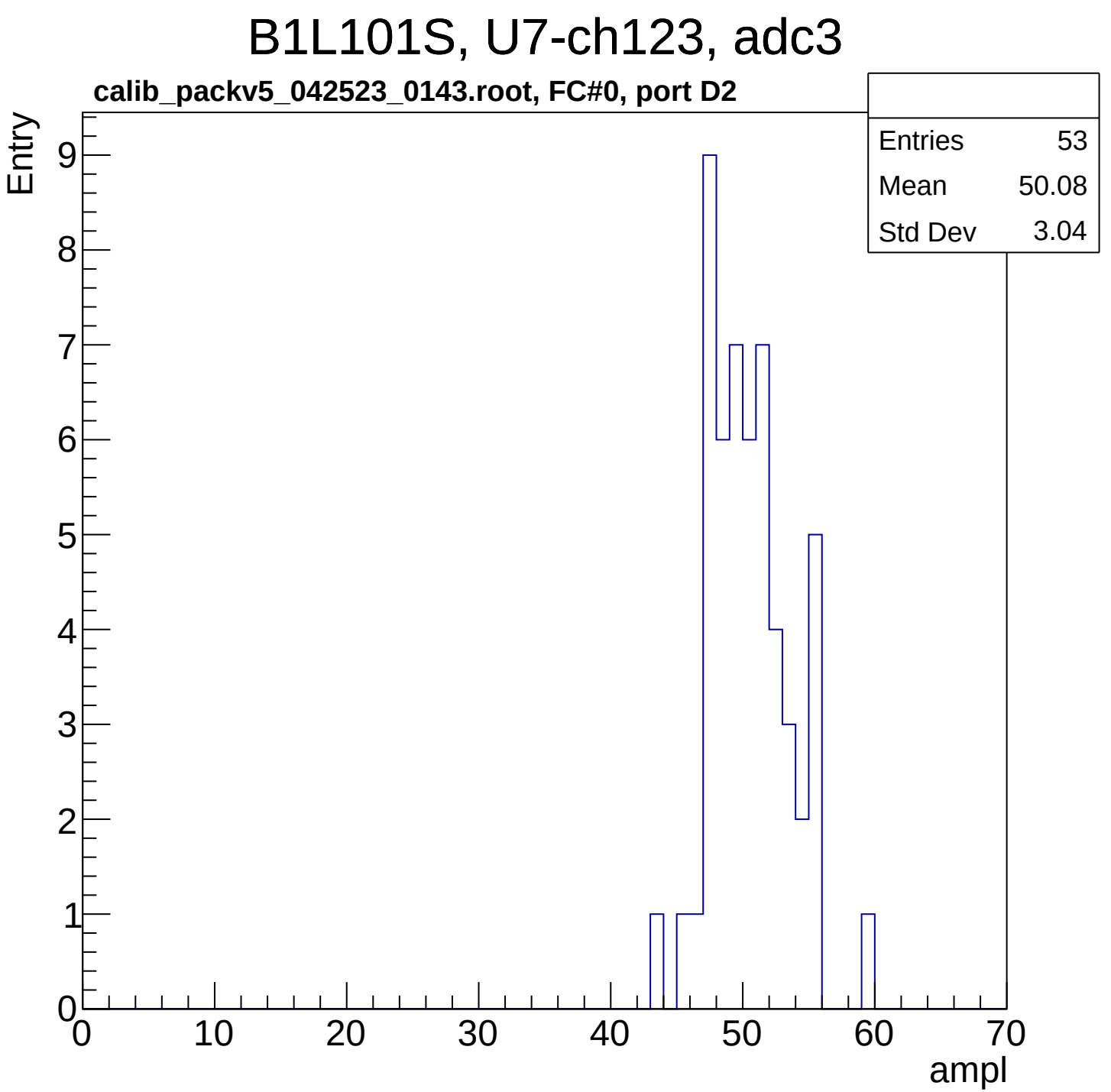
B1L101S, U7-ch123, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 50.08
Std Dev 3.04
Entry
ampl
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2
3
4
5
6
7
8
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0
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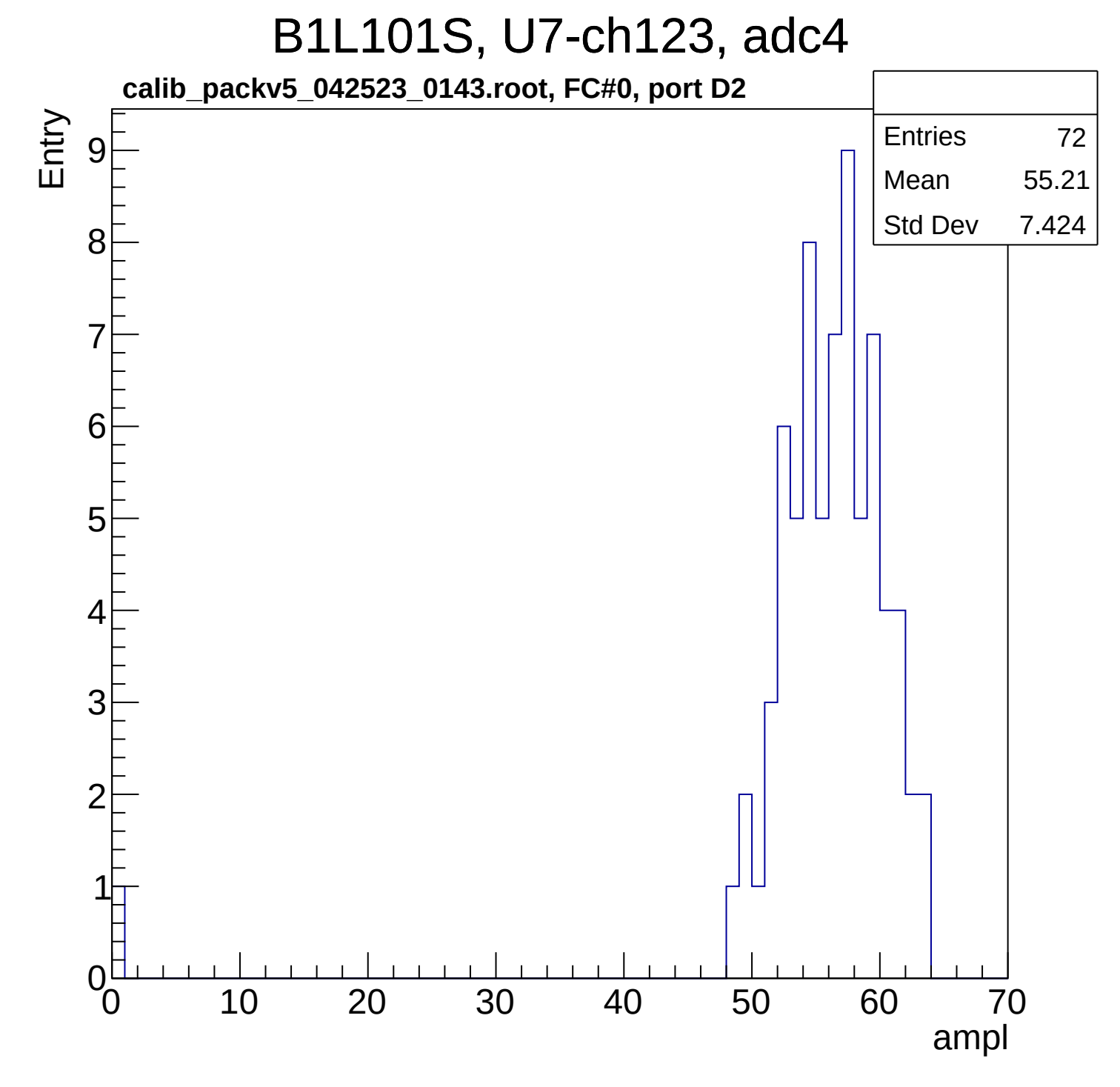
B1L101S, U7-ch123, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 55.21
Std Dev 7.424
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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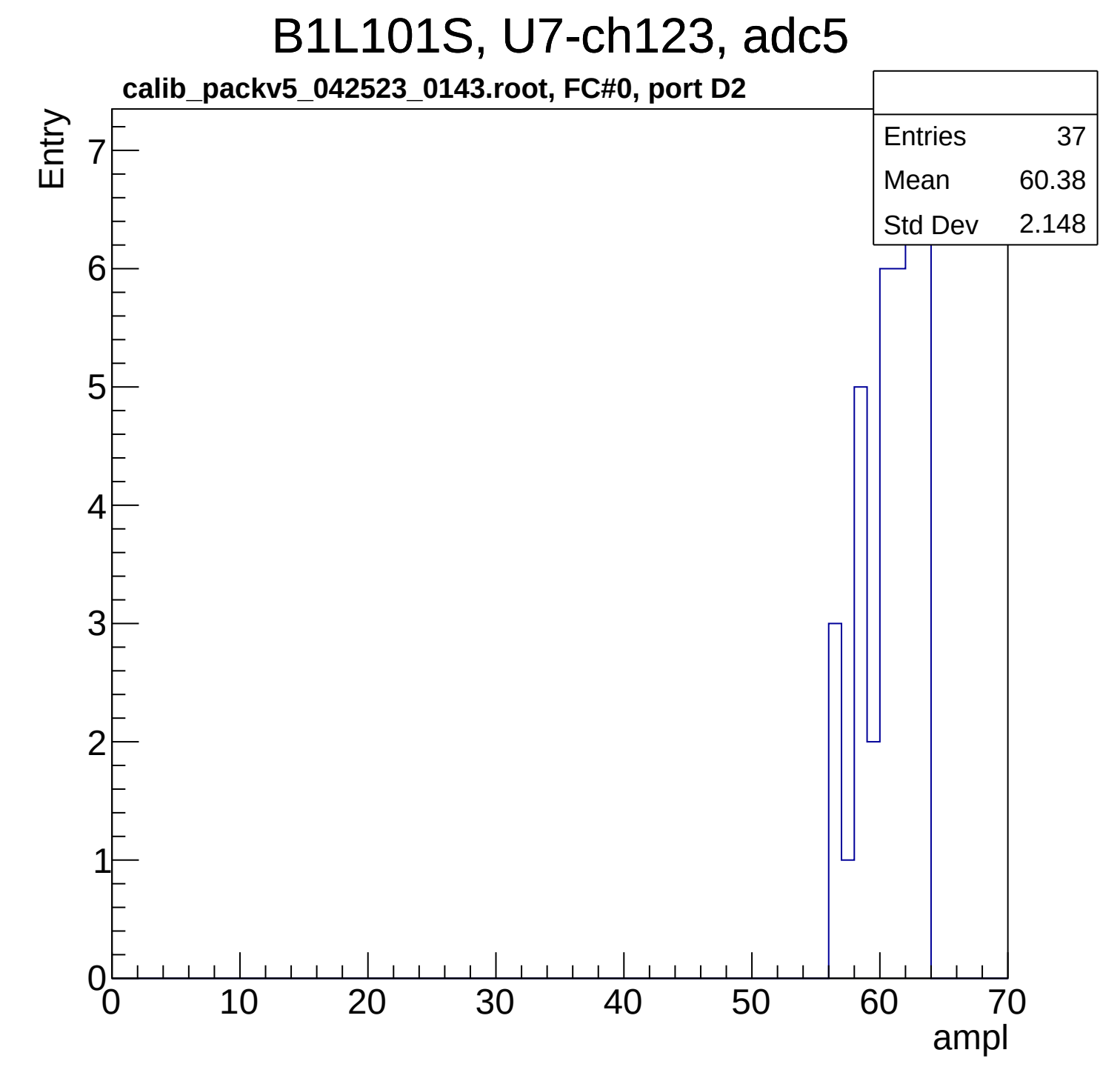
B1L101S, U7-ch123, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 37
Mean 60.38
Std Dev 2.148
Entry
ampl
0
1
2
3
4
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6
7
0
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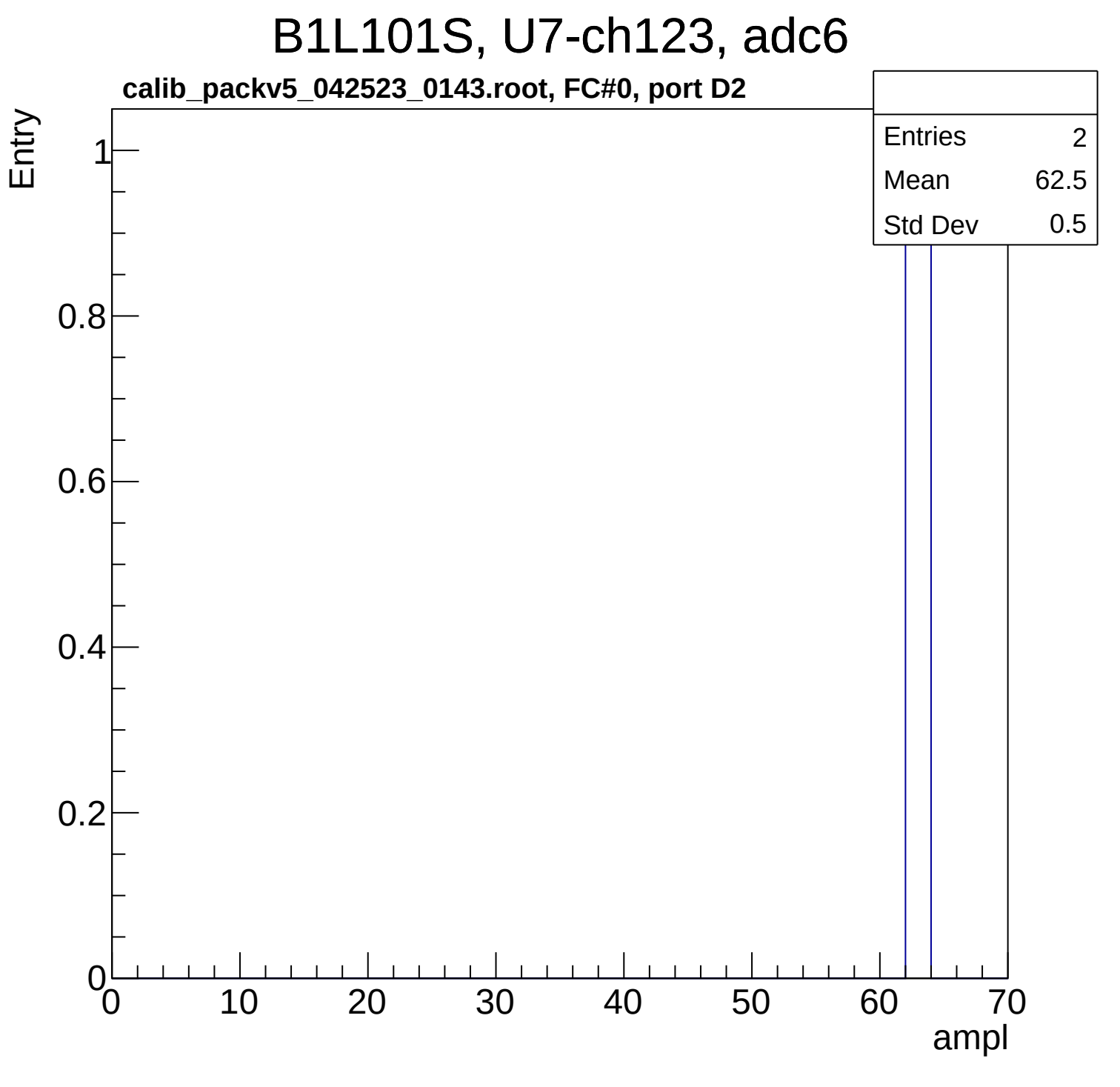
B1L101S, U7-ch123, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
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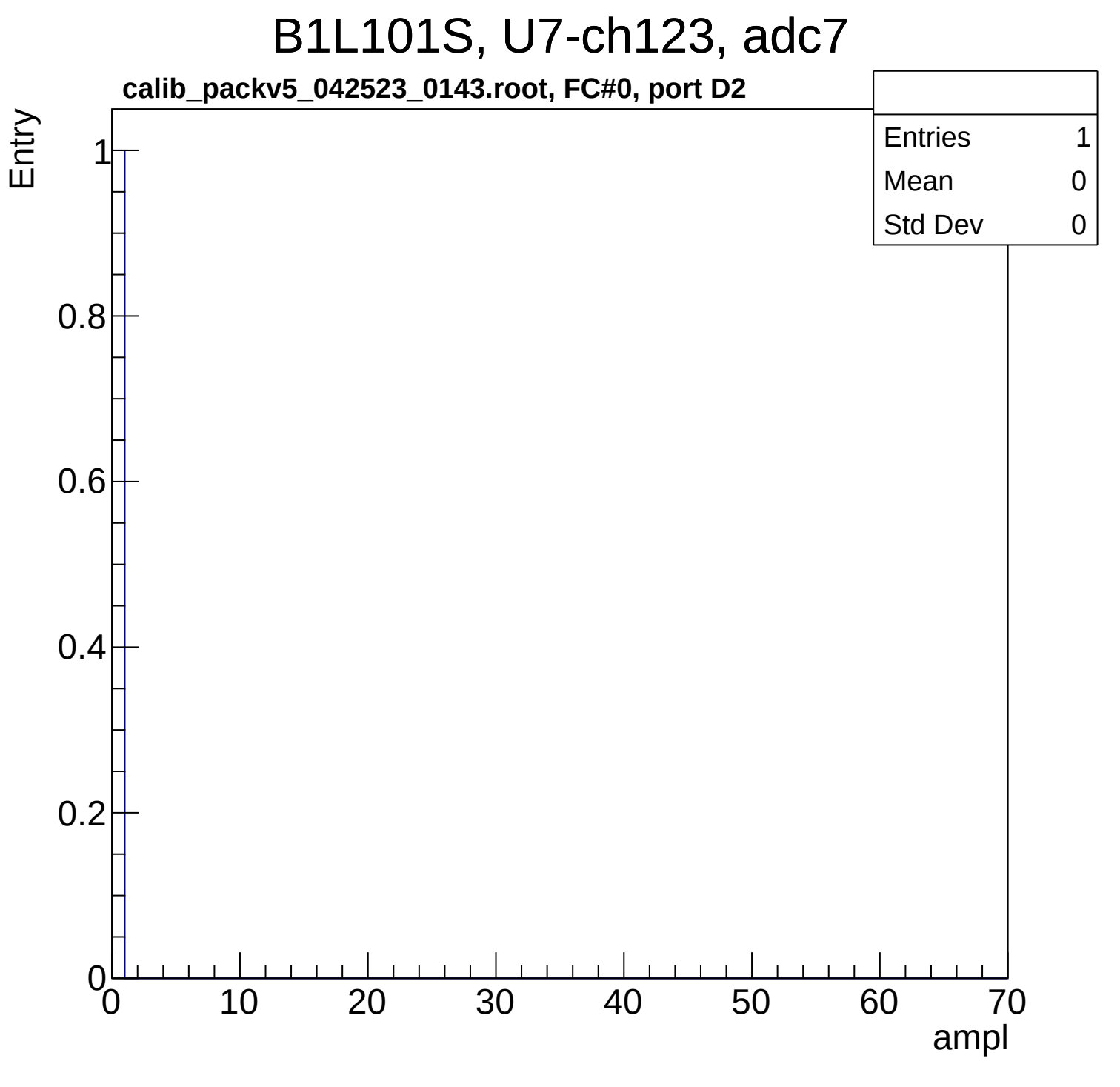
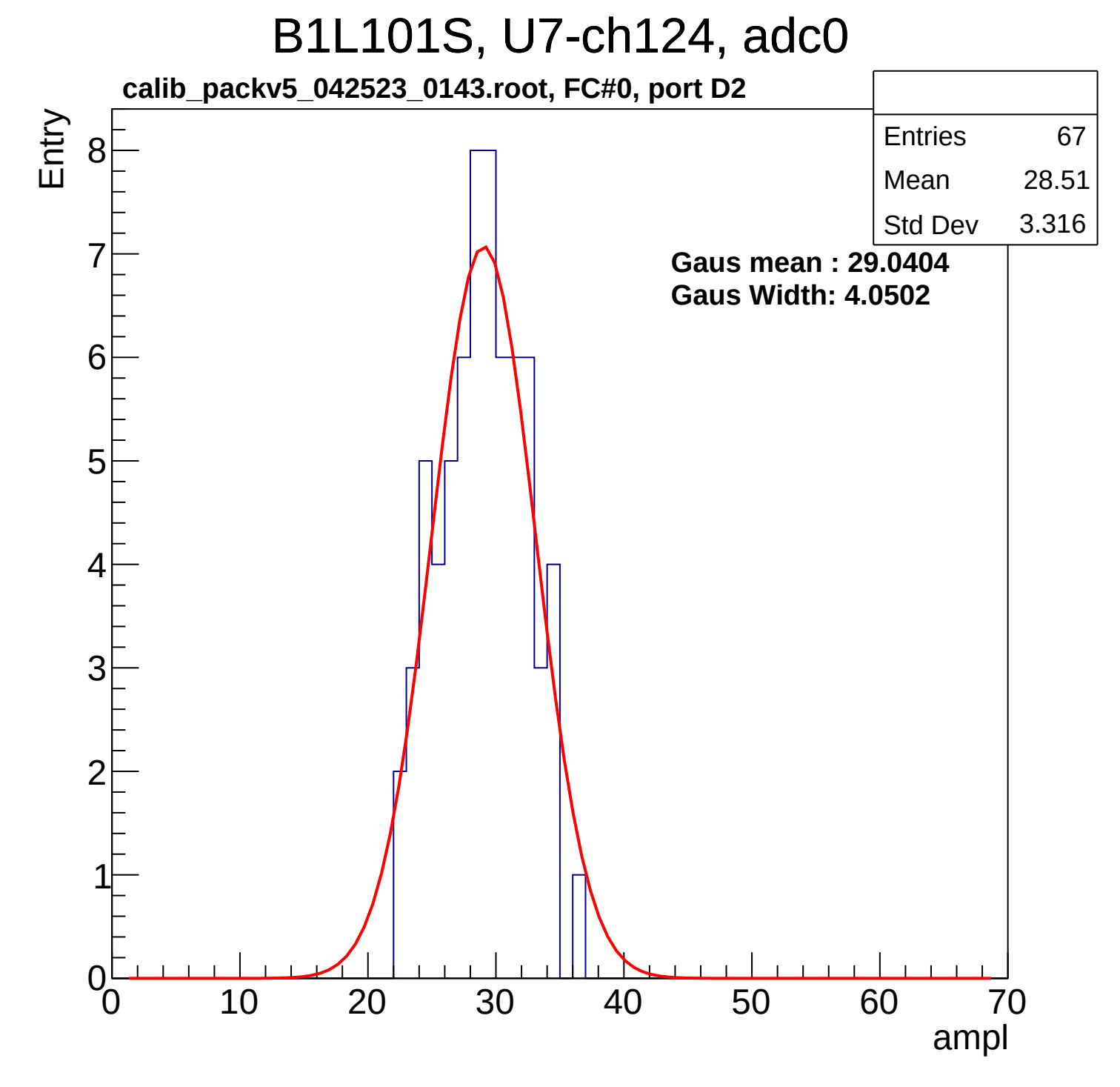
40
50
60
70
ampl


B1L101S, U7-ch123, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch124, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 28.51
Std Dev 3.316
Gaus mean : 29.0404
Gaus Width: 4.0502
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
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40
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60
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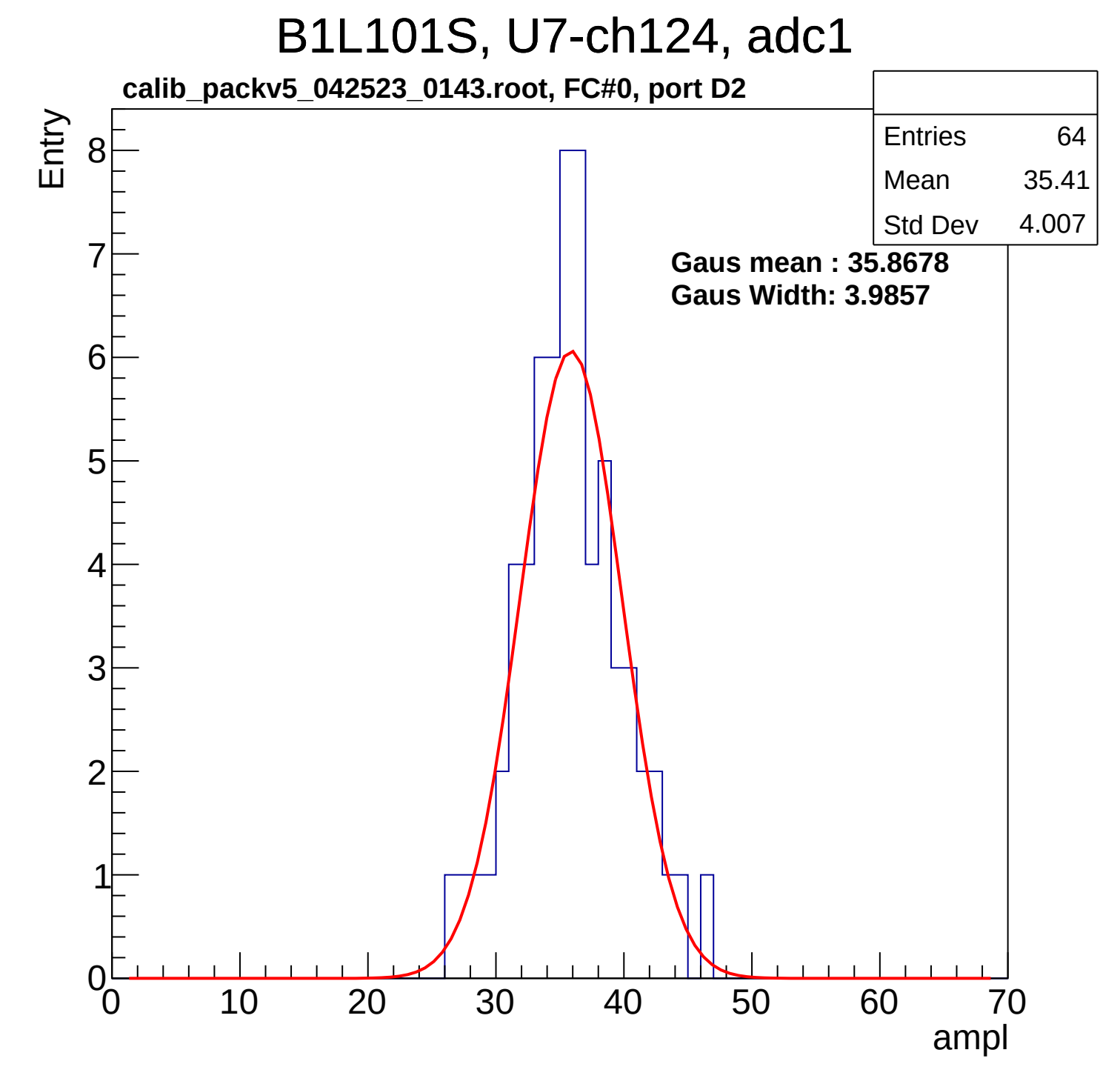
B1L101S, U7-ch124, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 35.41
Std Dev 4.007
Gaus mean : 35.8678
Gaus Width: 3.9857
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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40
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60
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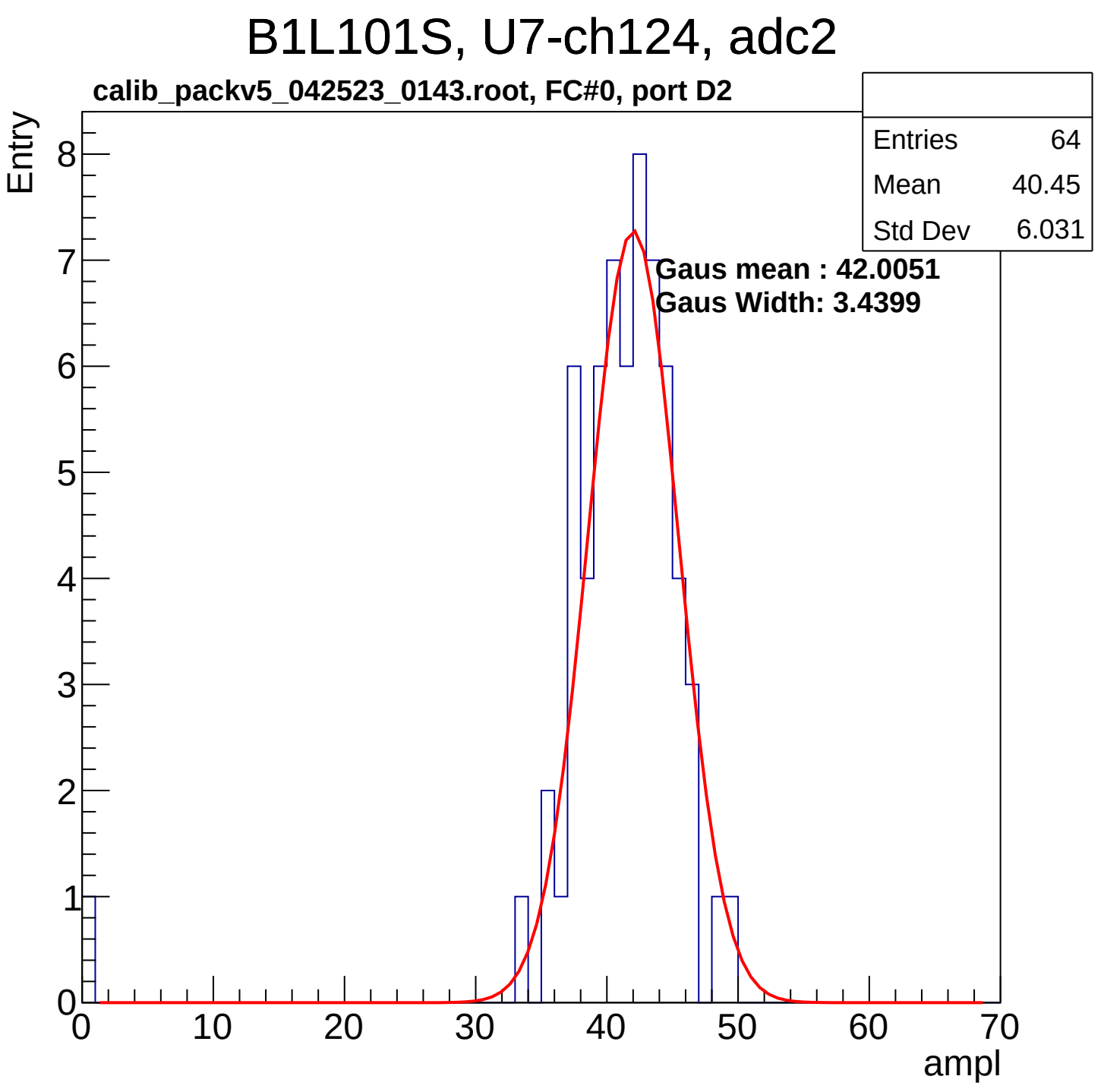
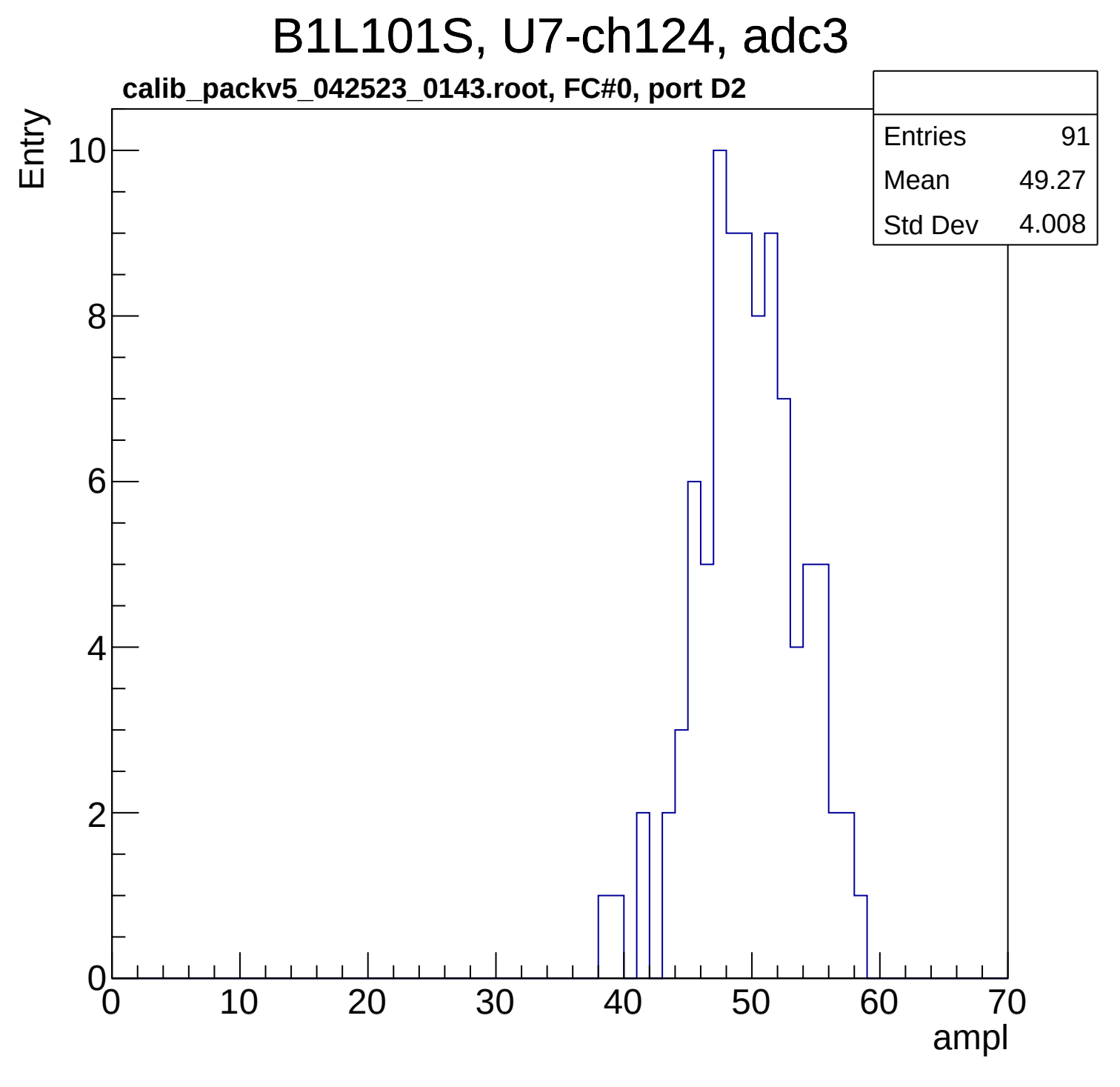
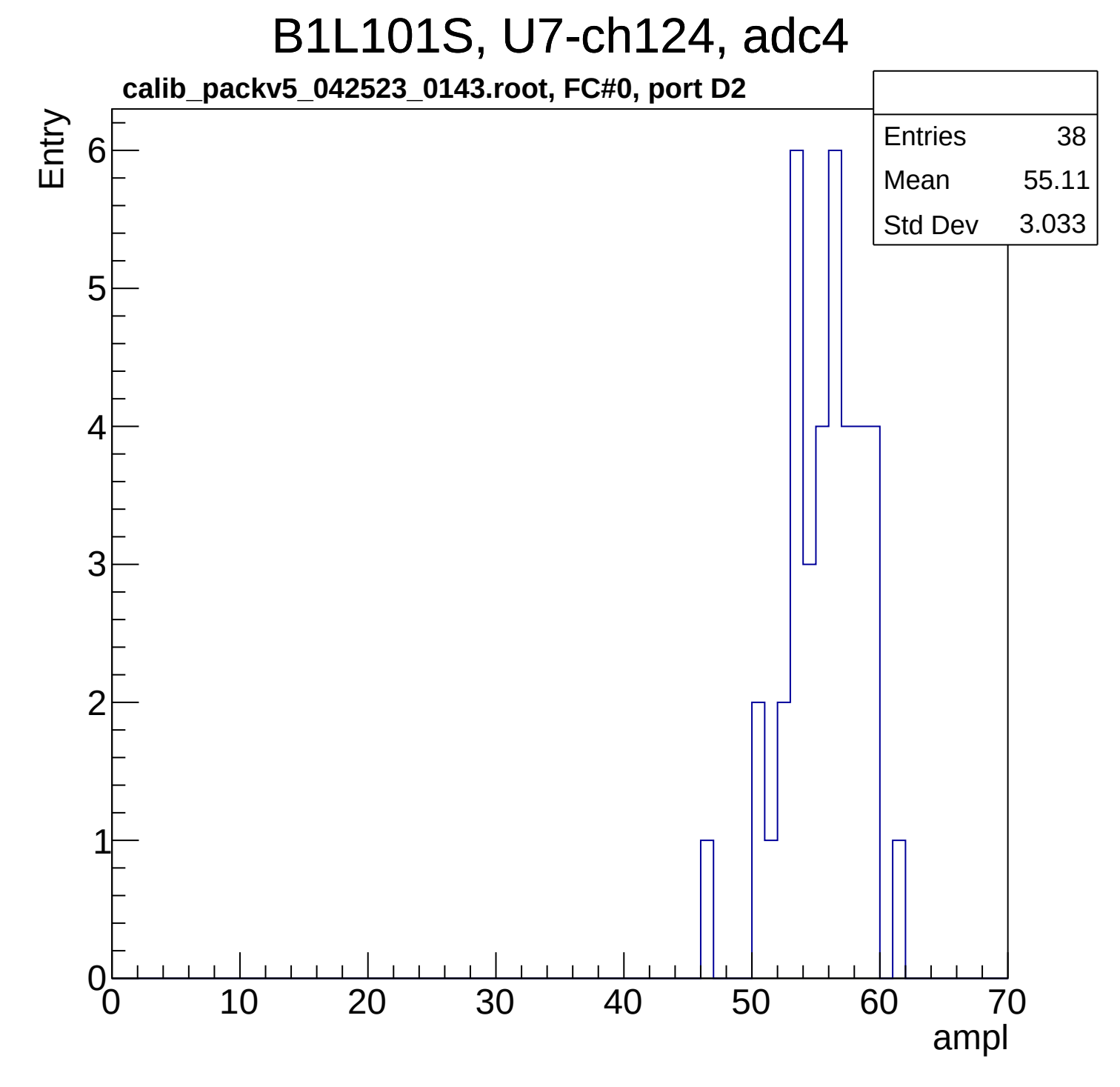

B1L101S, U7-ch124, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 40.45
Std Dev 6.031
Gaus mean : 42.0051
Gaus Width: 3.4399
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch124, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 91
Mean 49.27
Std Dev 4.008
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch124, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 38
Mean 55.11
Std Dev 3.033
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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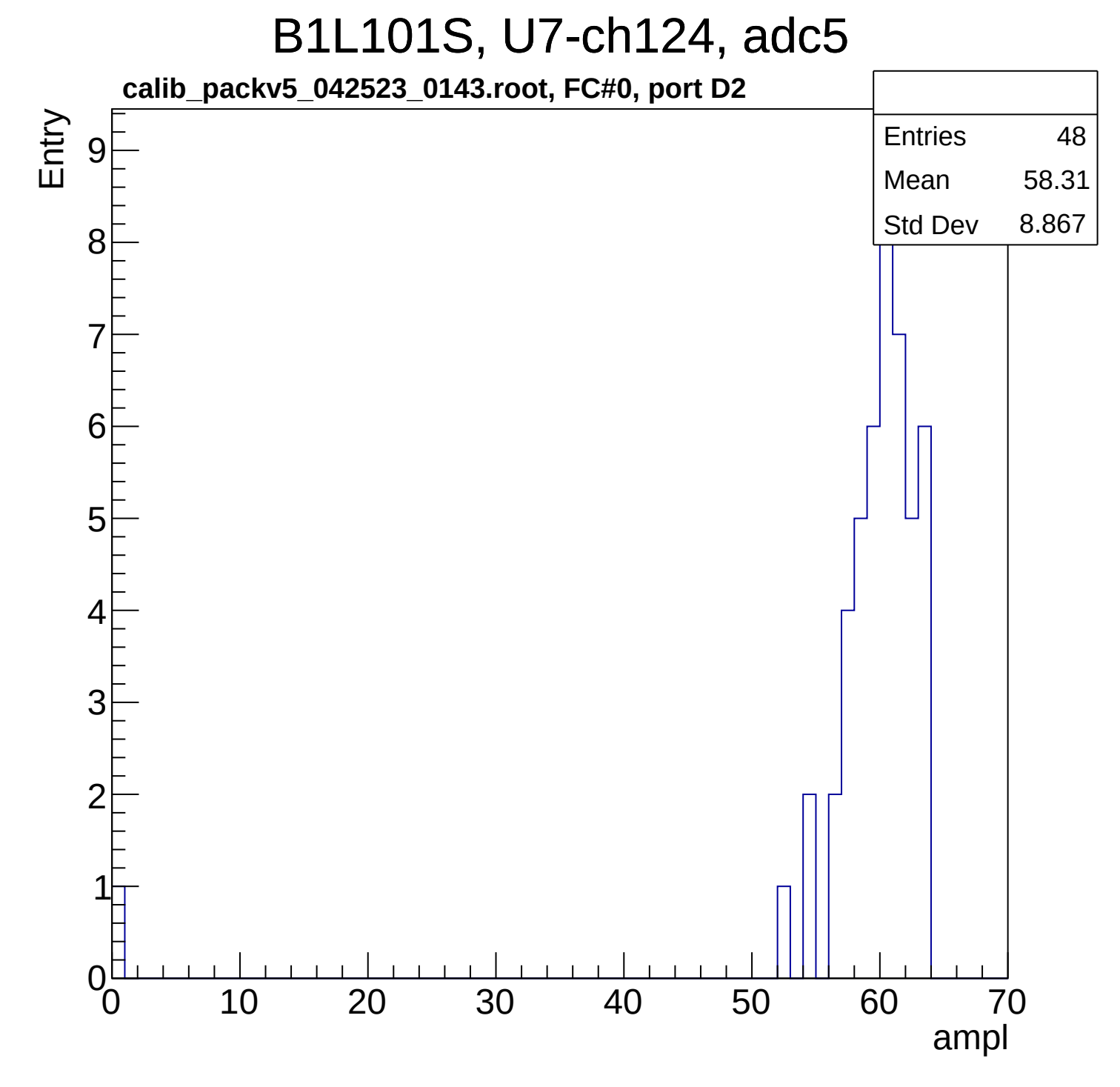
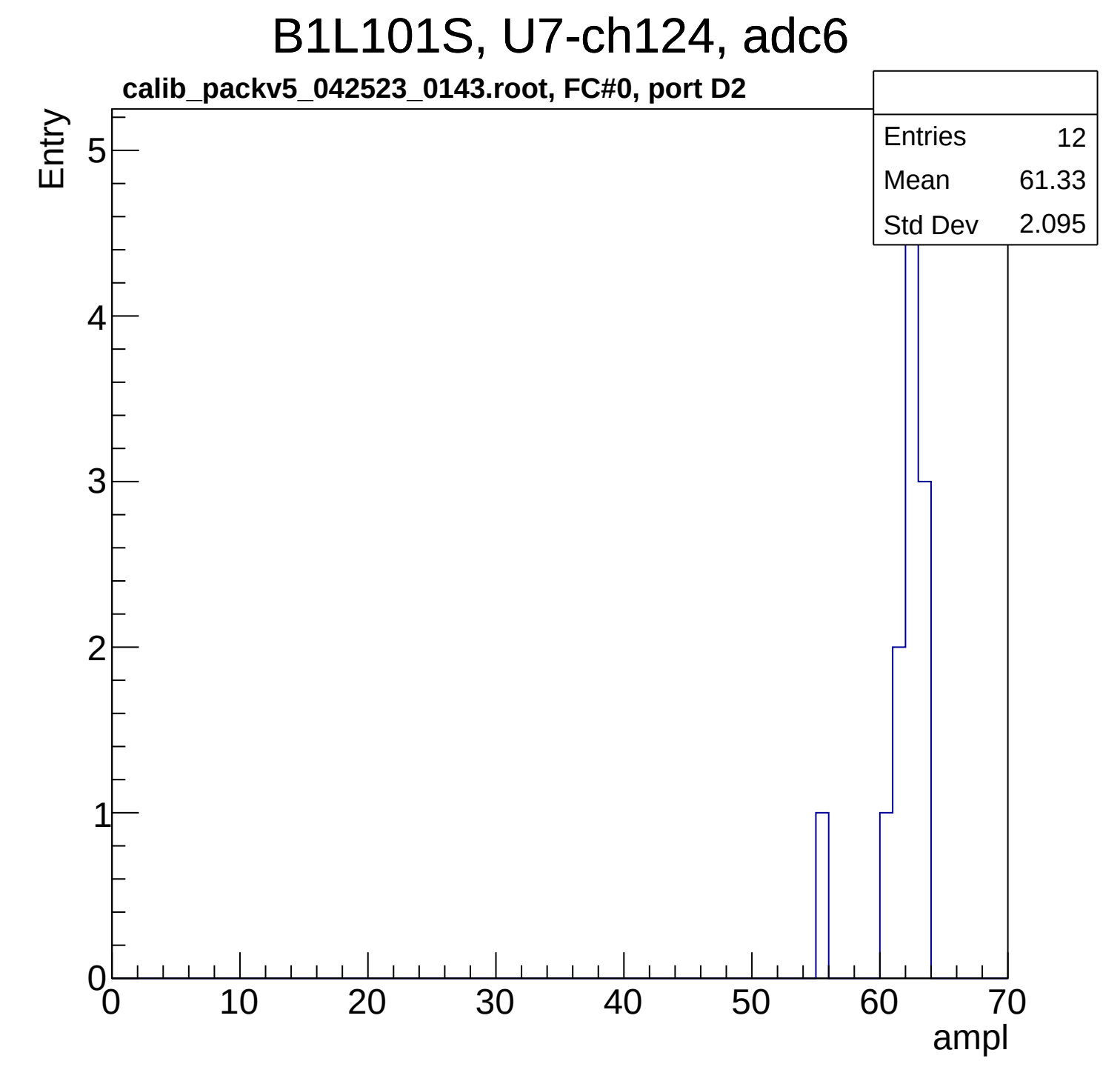
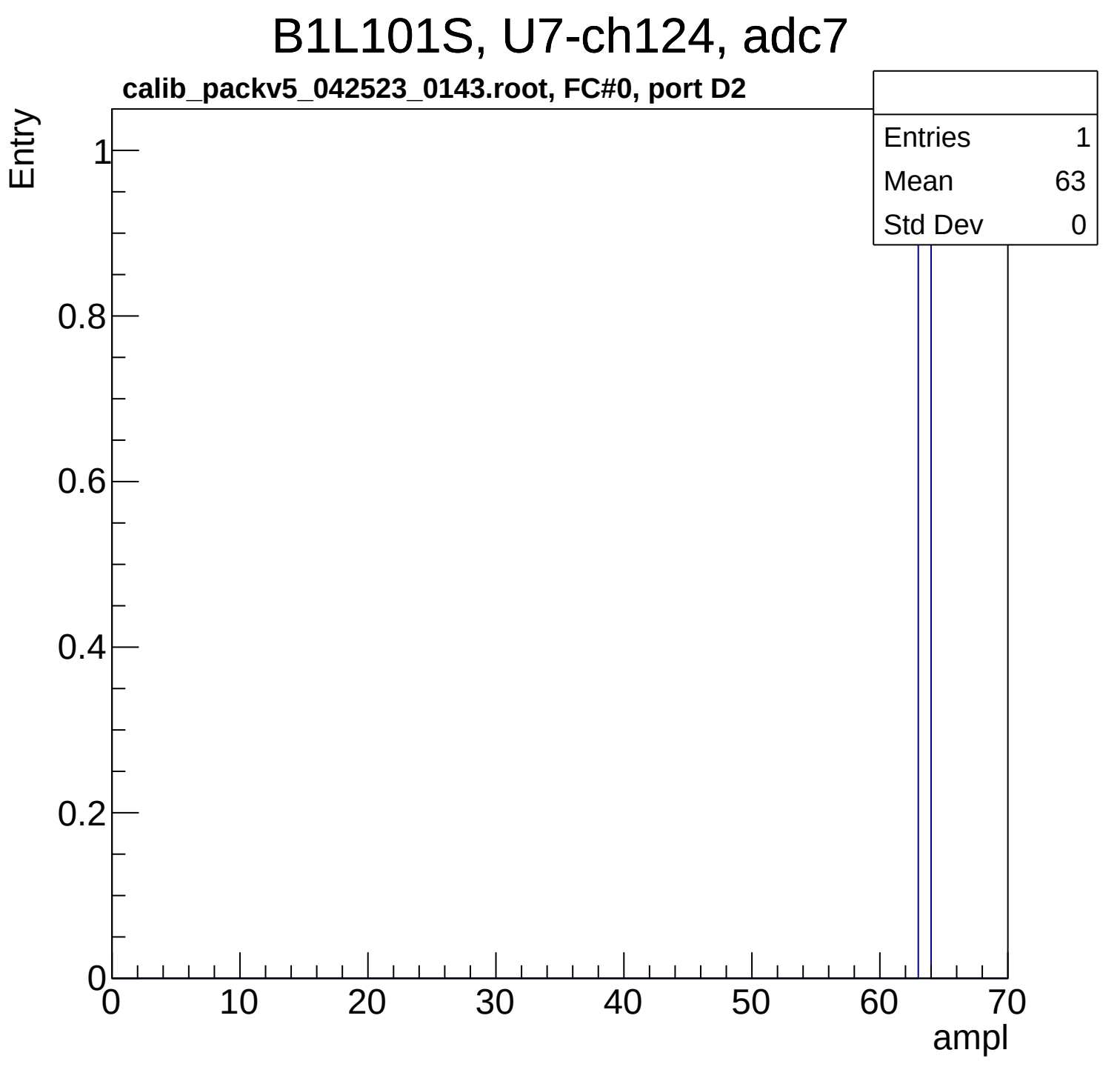
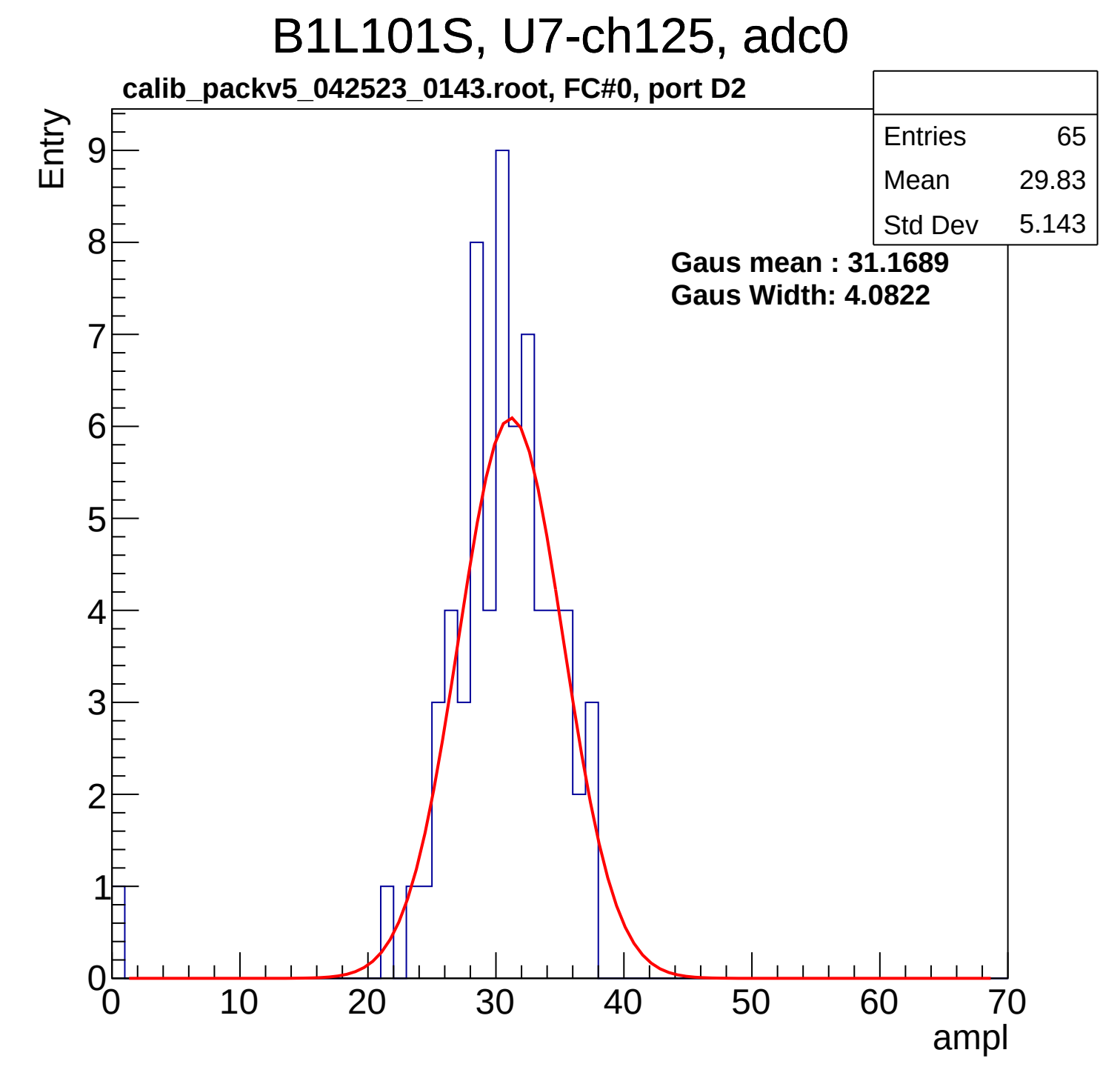
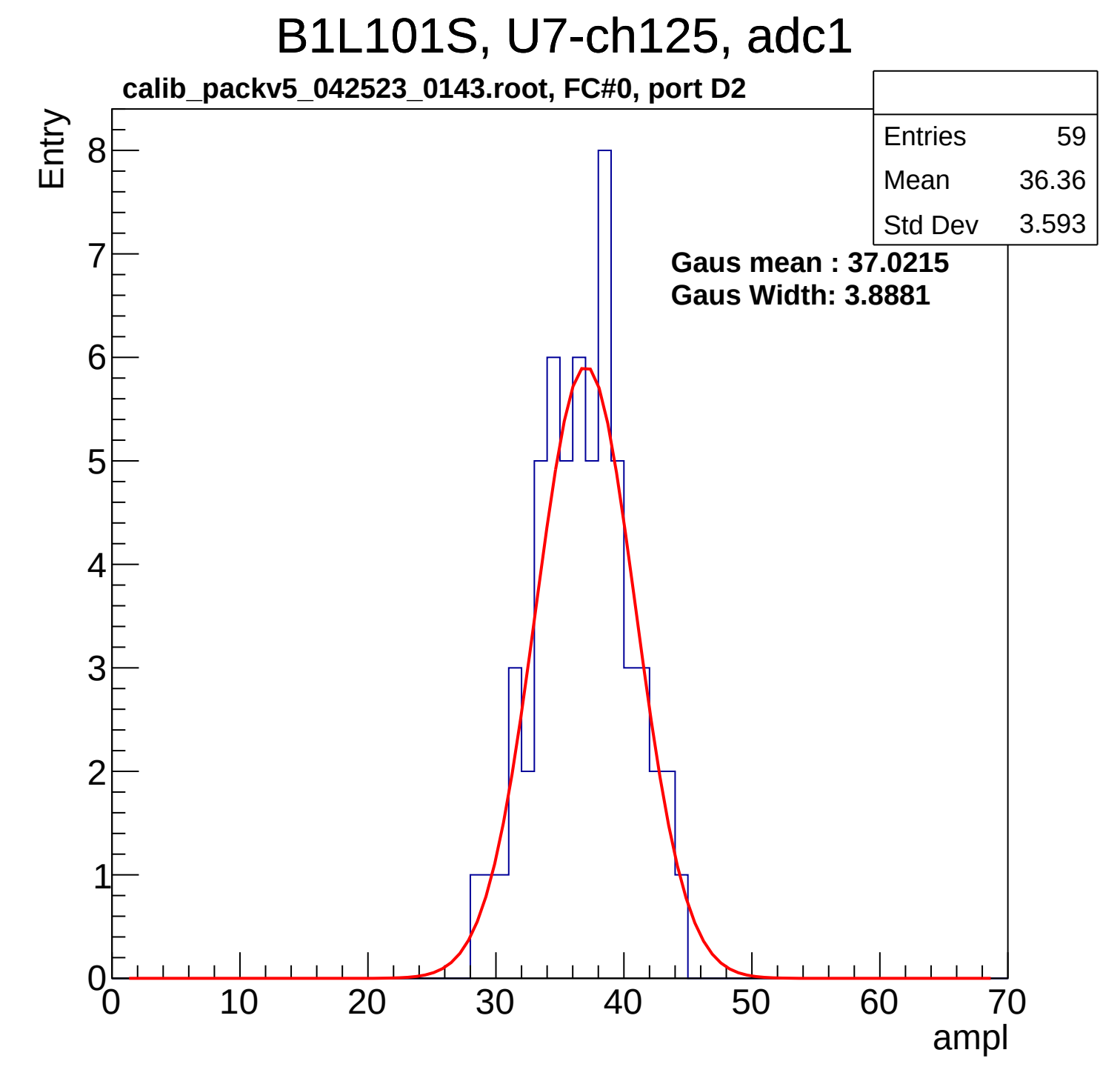
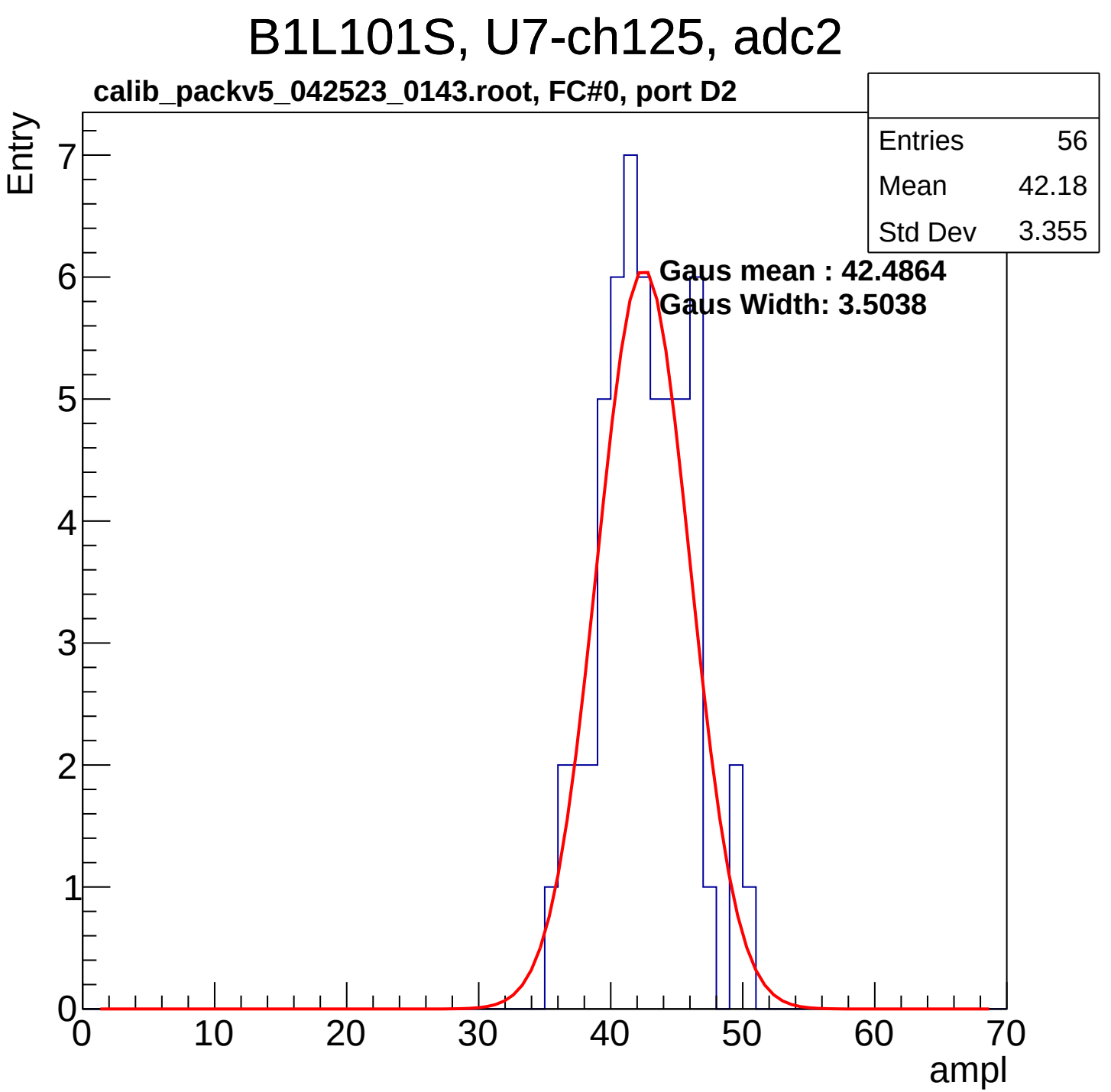

B1L101S, U7-ch124, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 58.31
Std Dev 8.867
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

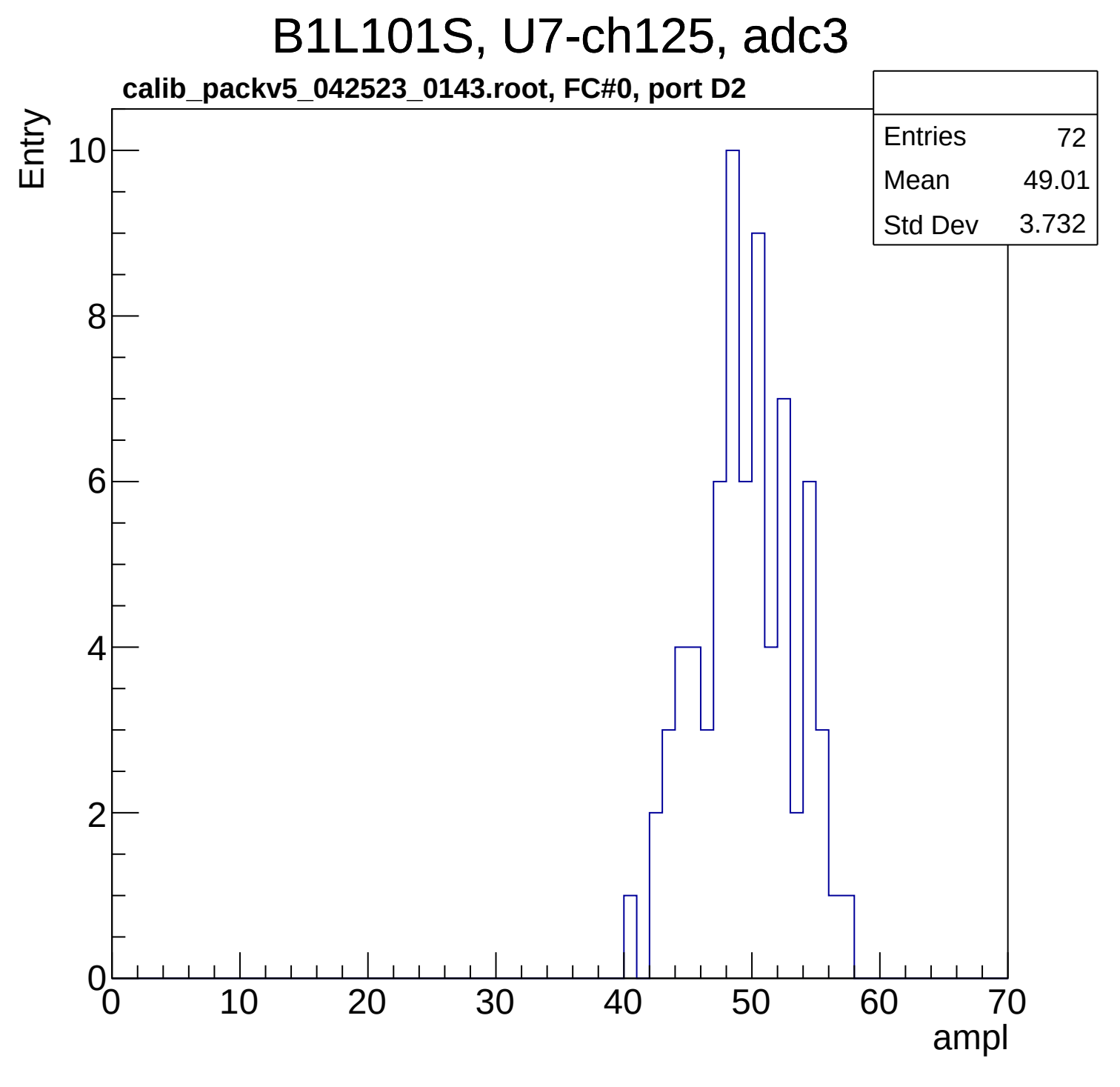

B1L101S, U7-ch124, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 12
Mean 61.33
Std Dev 2.095
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

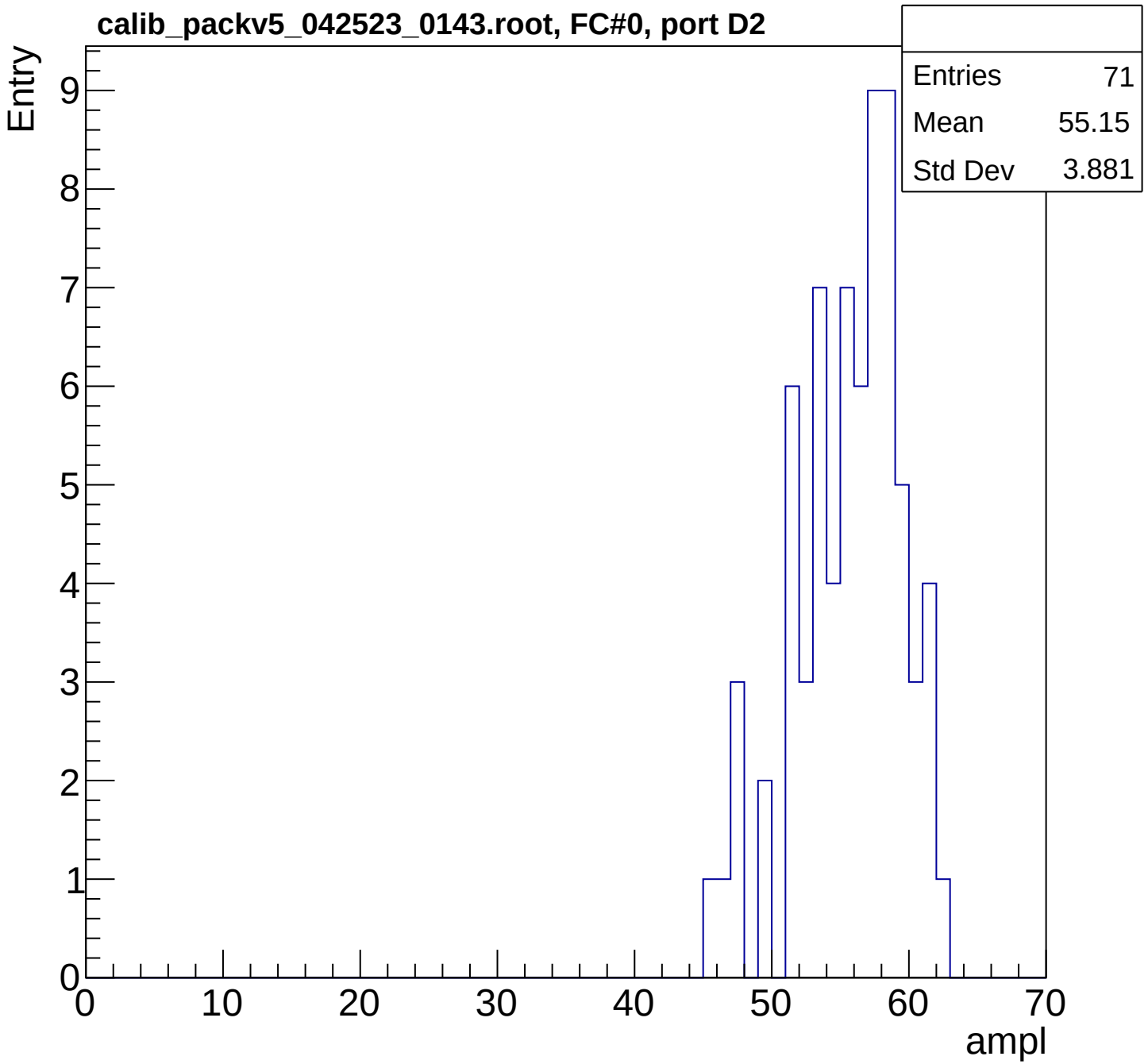

B1L101S, U7-ch124, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch125, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 29.83
Std Dev 5.143
Gaus mean : 31.1689
Gaus Width: 4.0822
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch125, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 36.36
Std Dev 3.593
Gaus mean : 37.0215
Gaus Width: 3.8881
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch125, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 42.18
Std Dev 3.355
Gaus mean : 42.4864
Gaus Width: 3.5038
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U7-ch125, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 49.01
Std Dev 3.732
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch125, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 55.15
Std Dev 3.881
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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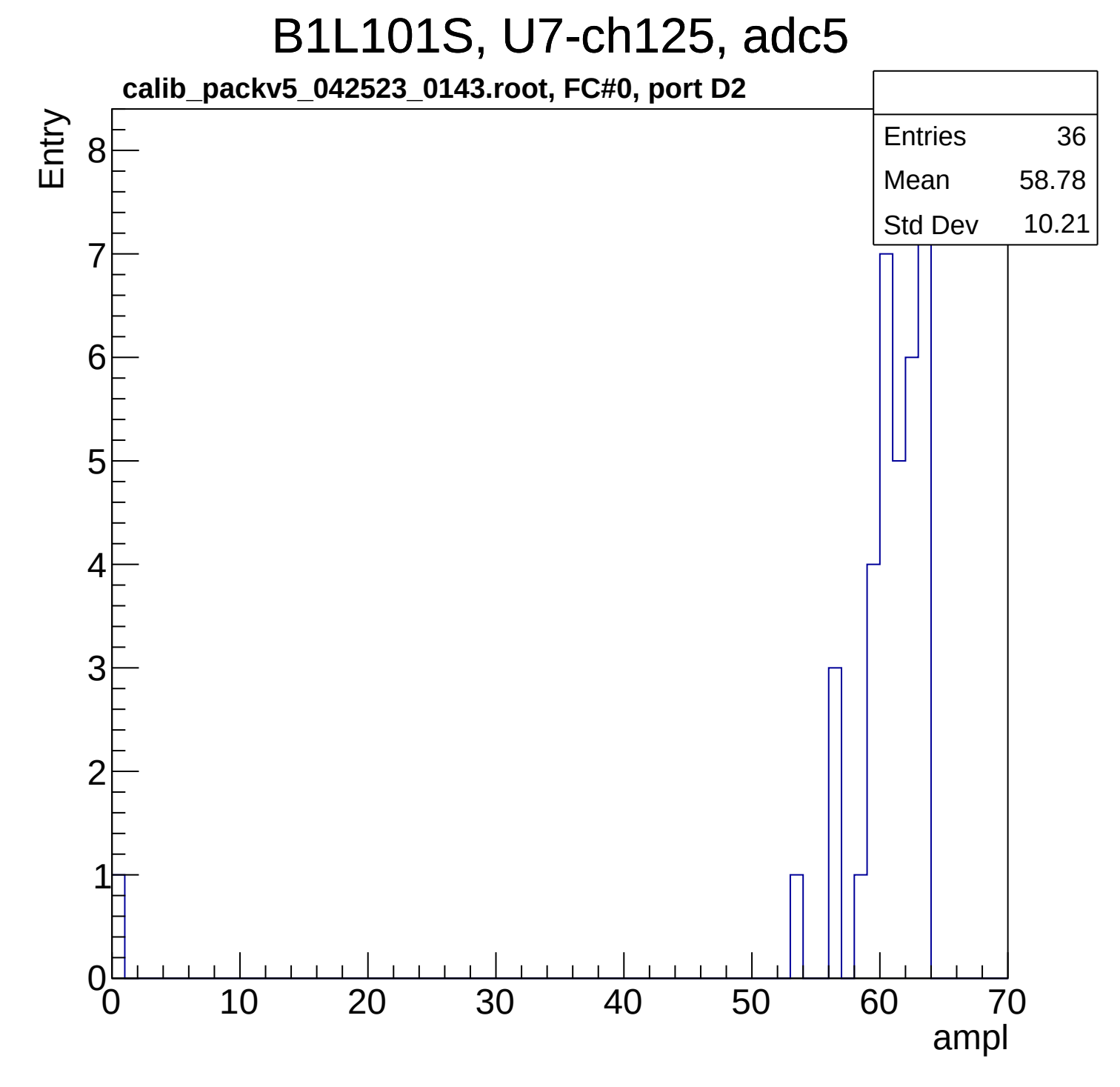
B1L101S, U7-ch125, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 36
Mean 58.78
Std Dev 10.21
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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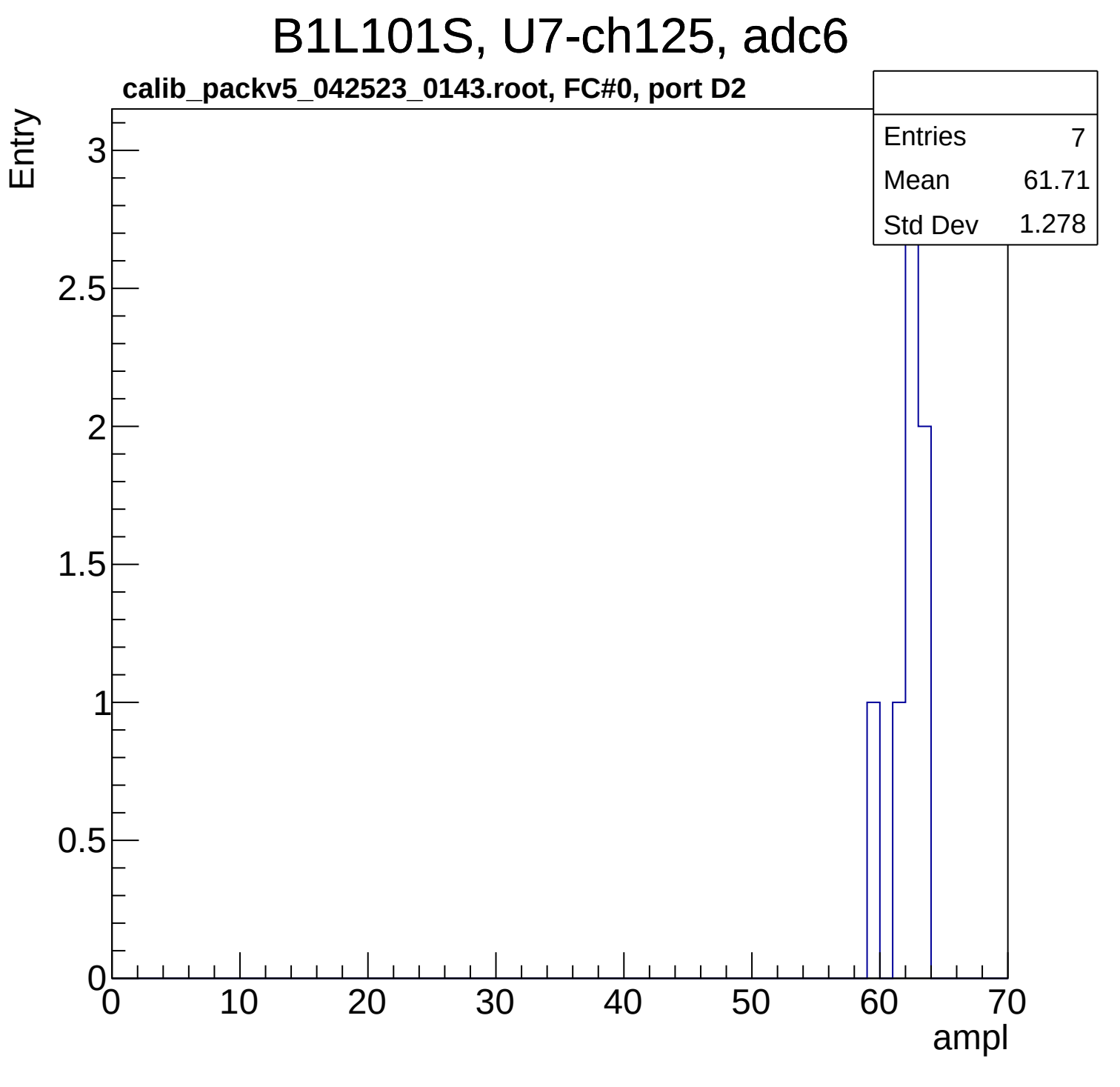
B1L101S, U7-ch125, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 61.71
Std Dev 1.278
Entry
ampl
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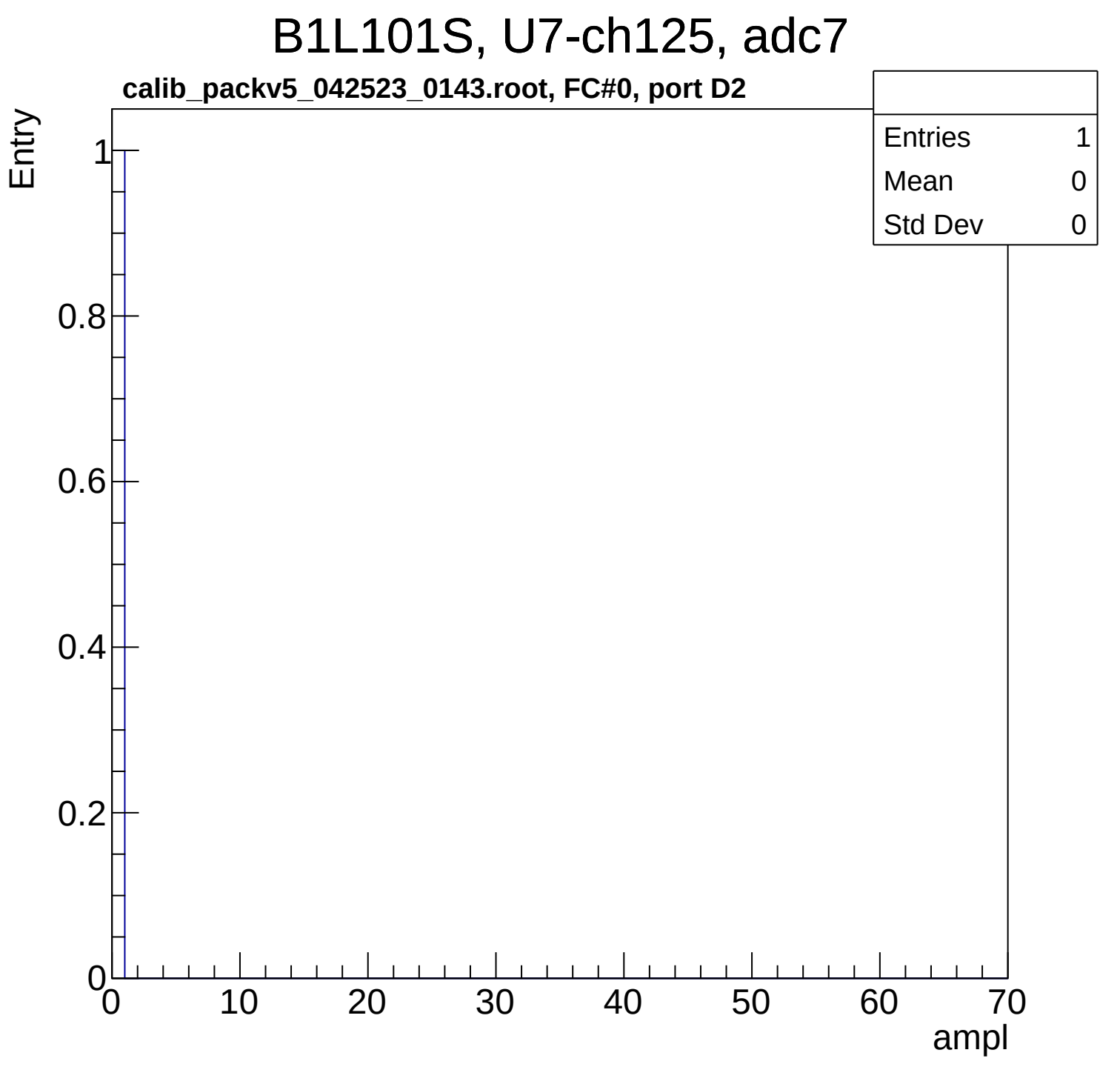
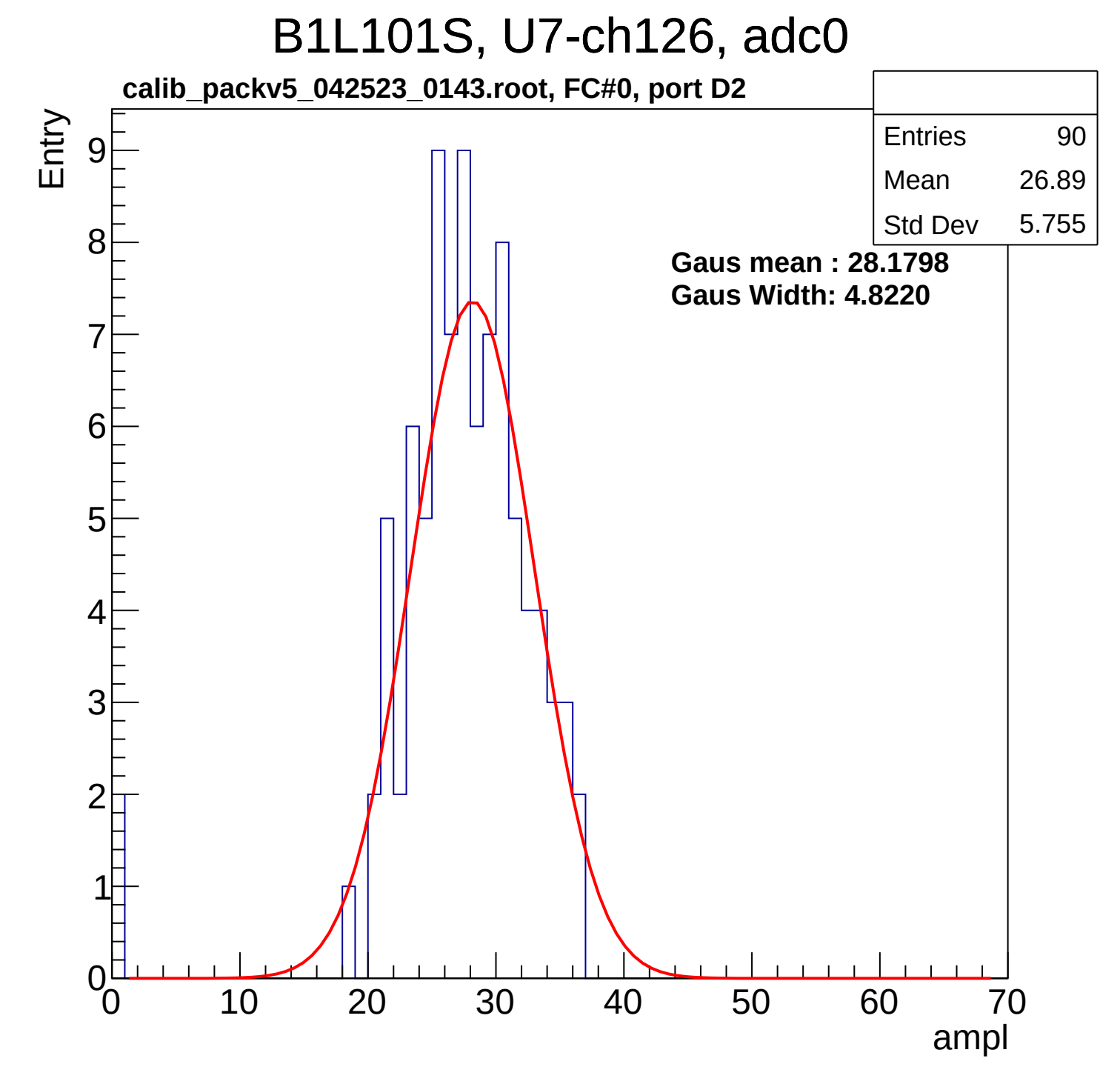
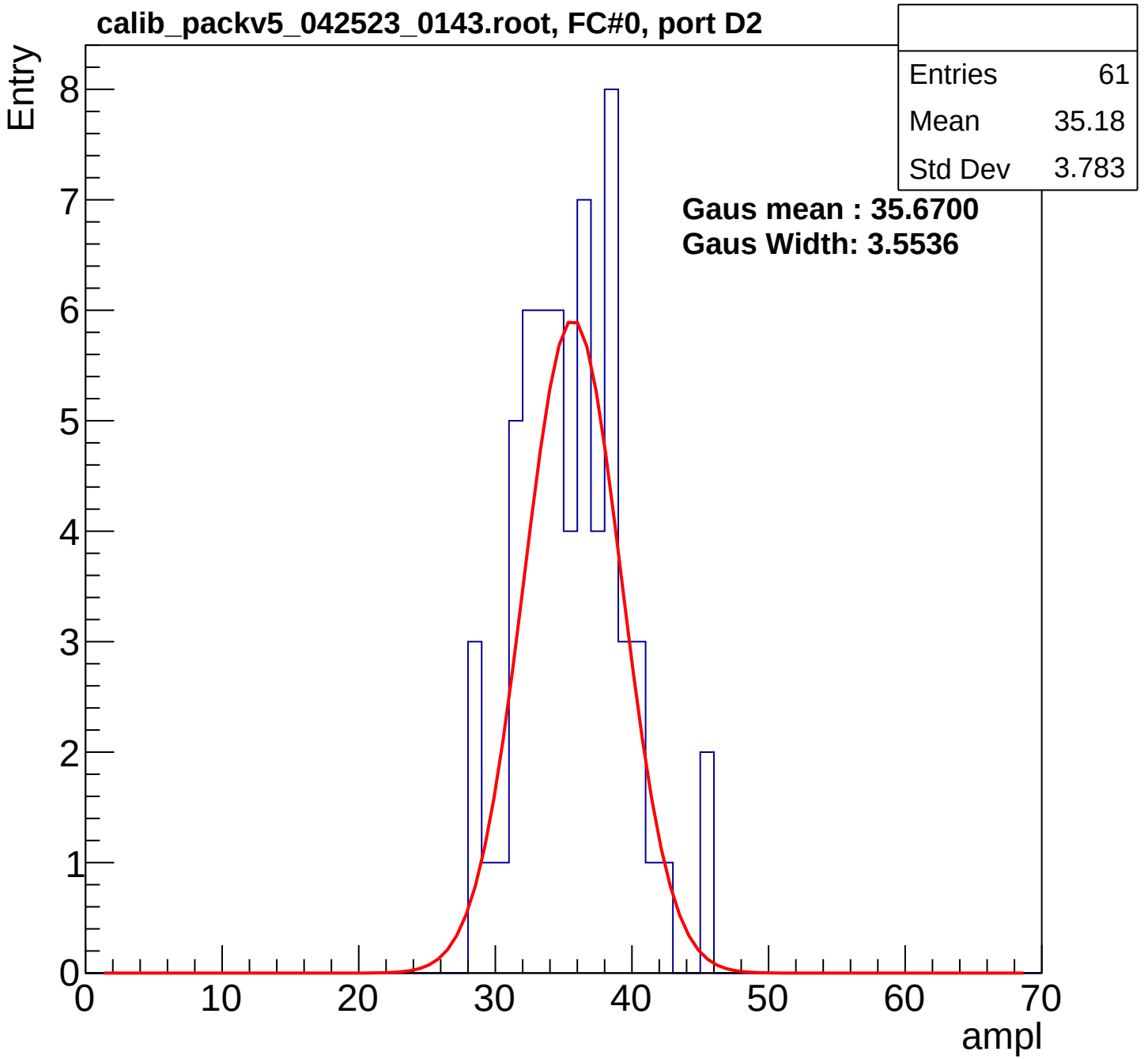
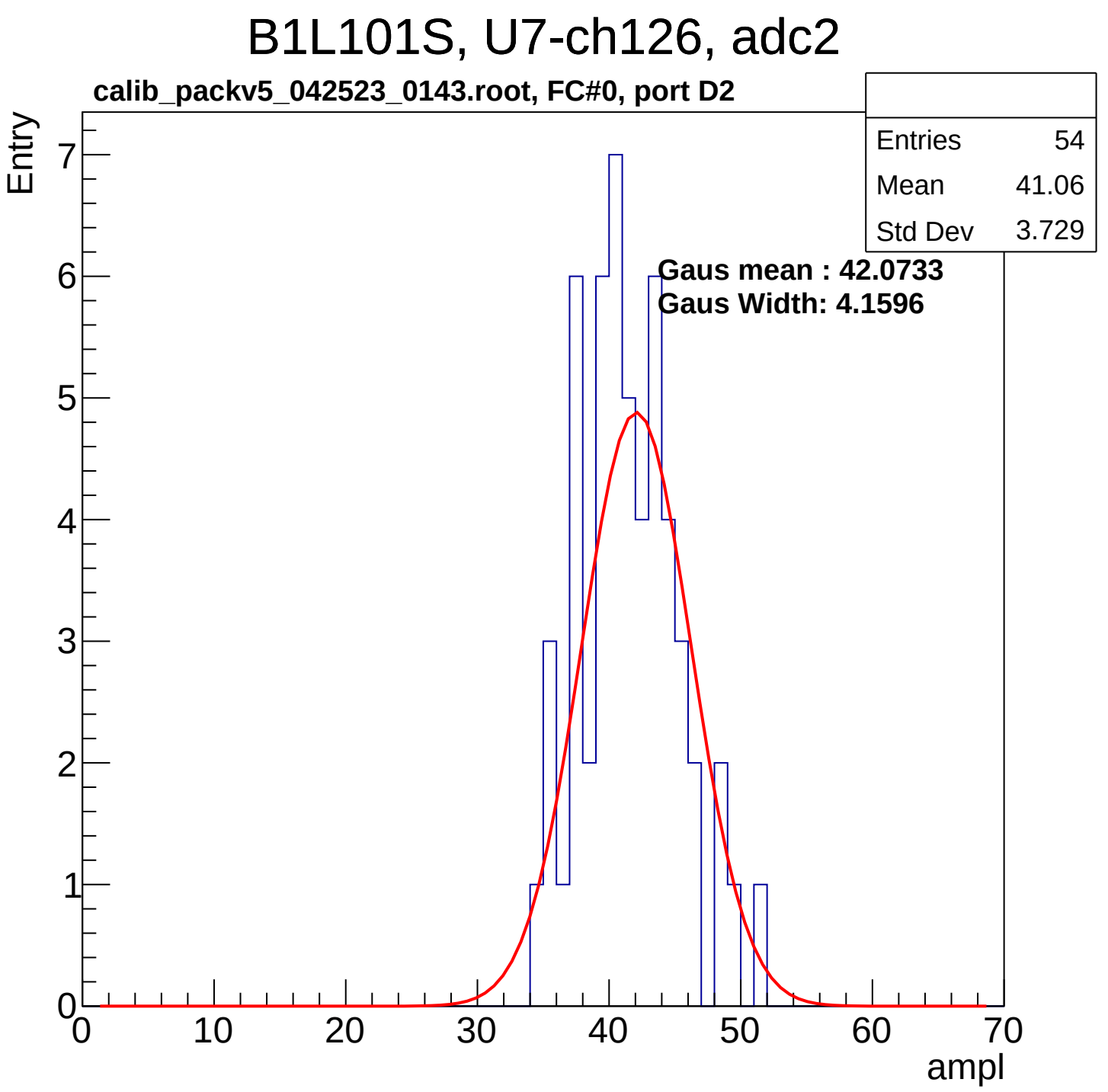
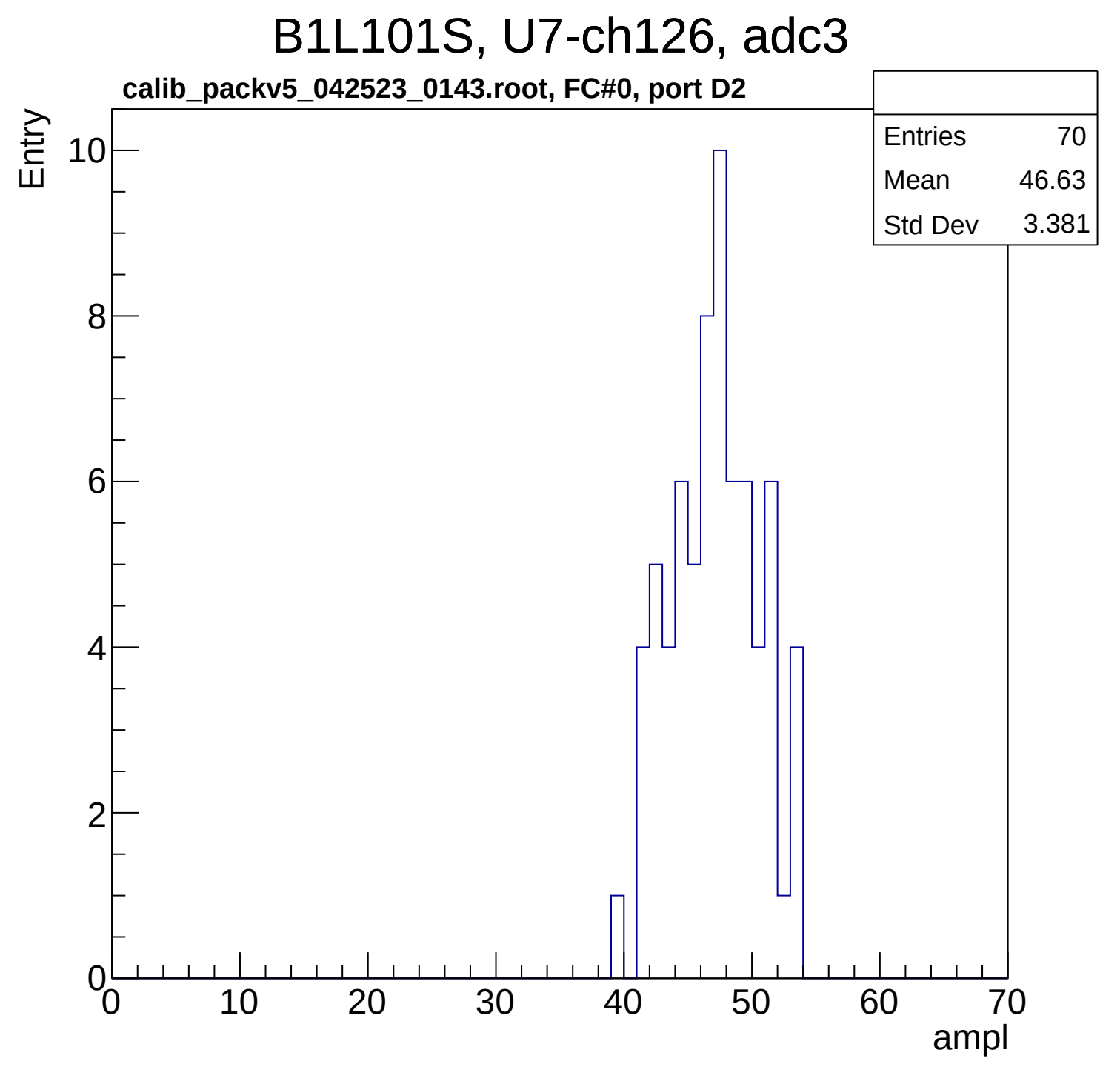
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

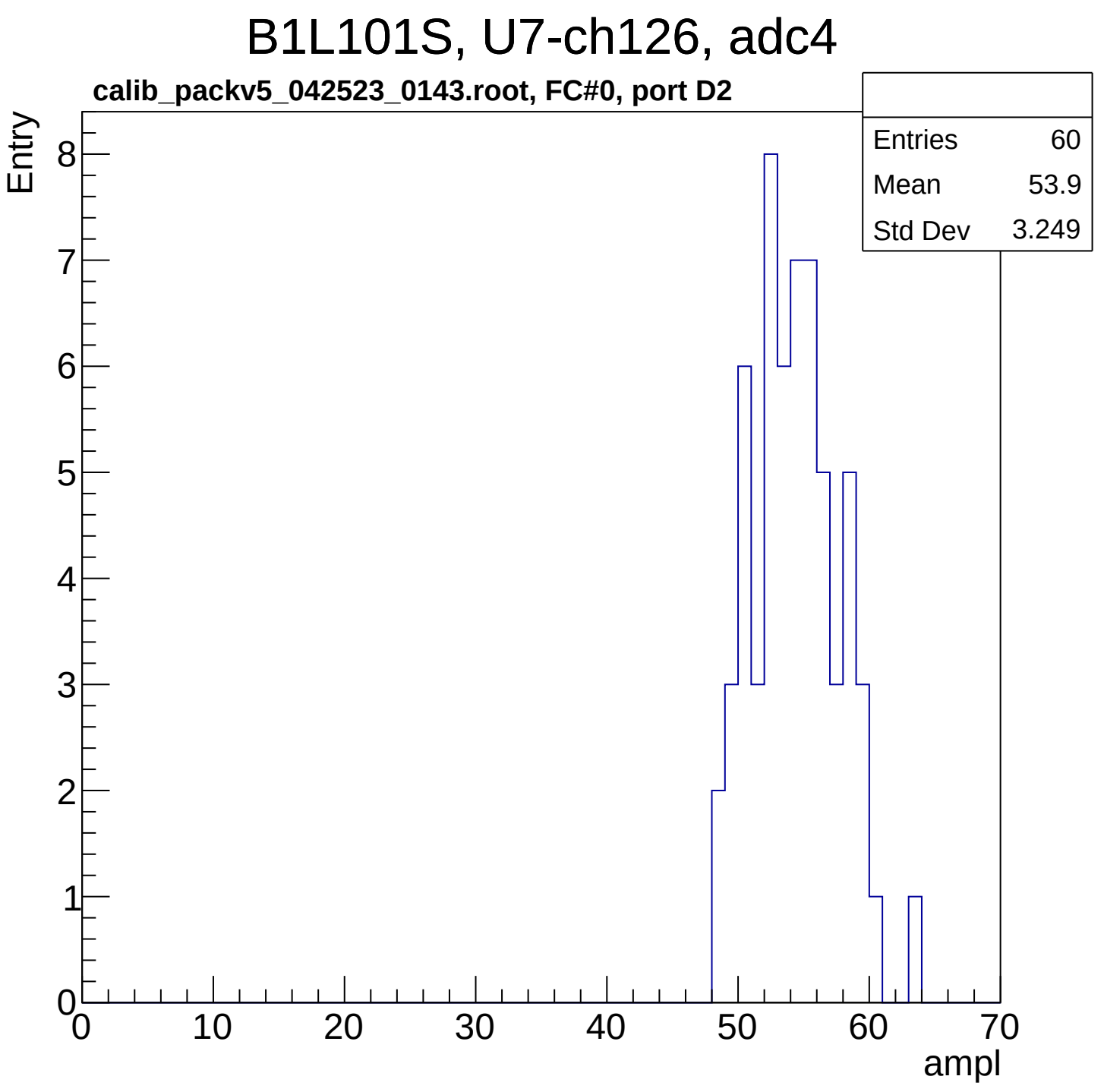

B1L101S, U7-ch125, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch126, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 90
Mean 26.89
Std Dev 5.755
Gaus mean : 28.1798
Gaus Width: 4.8220
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch126, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 35.18
Std Dev 3.783
Gaus mean : 35.6700
Gaus Width: 3.5536
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch126, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 41.06
Std Dev 3.729
Gaus mean : 42.0733
Gaus Width: 4.1596
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U7-ch126, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 46.63
Std Dev 3.381
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U7-ch126, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 53.9
Std Dev 3.249
Entry
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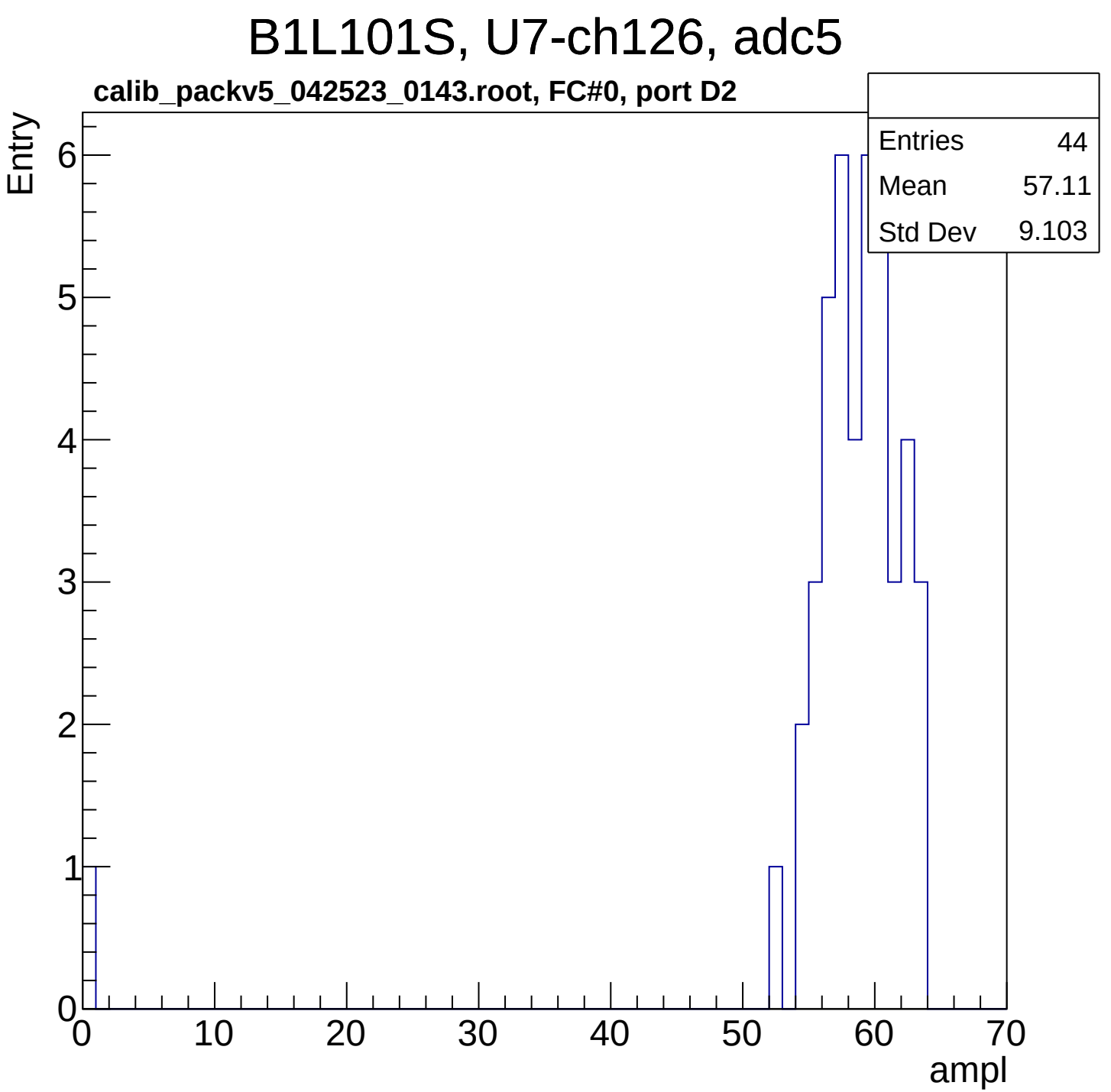
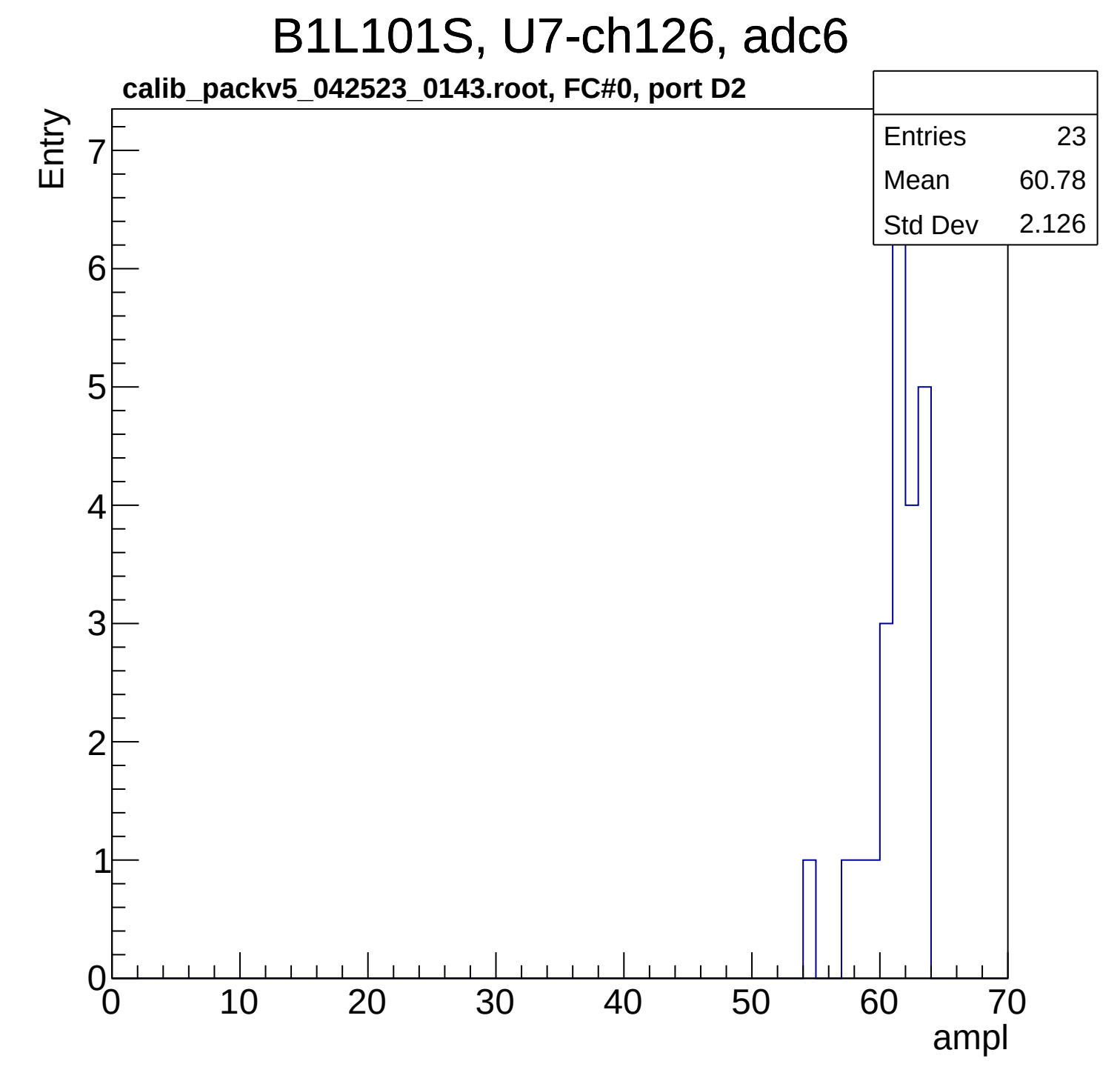
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L101S, U7-ch126, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 44
Mean 57.11
Std Dev 9.103
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L101S, U7-ch126, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 23
Mean 60.78
Std Dev 2.126
Entry
ampl
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2
3
4
5
6
7
0
10
20
30
40
50
60
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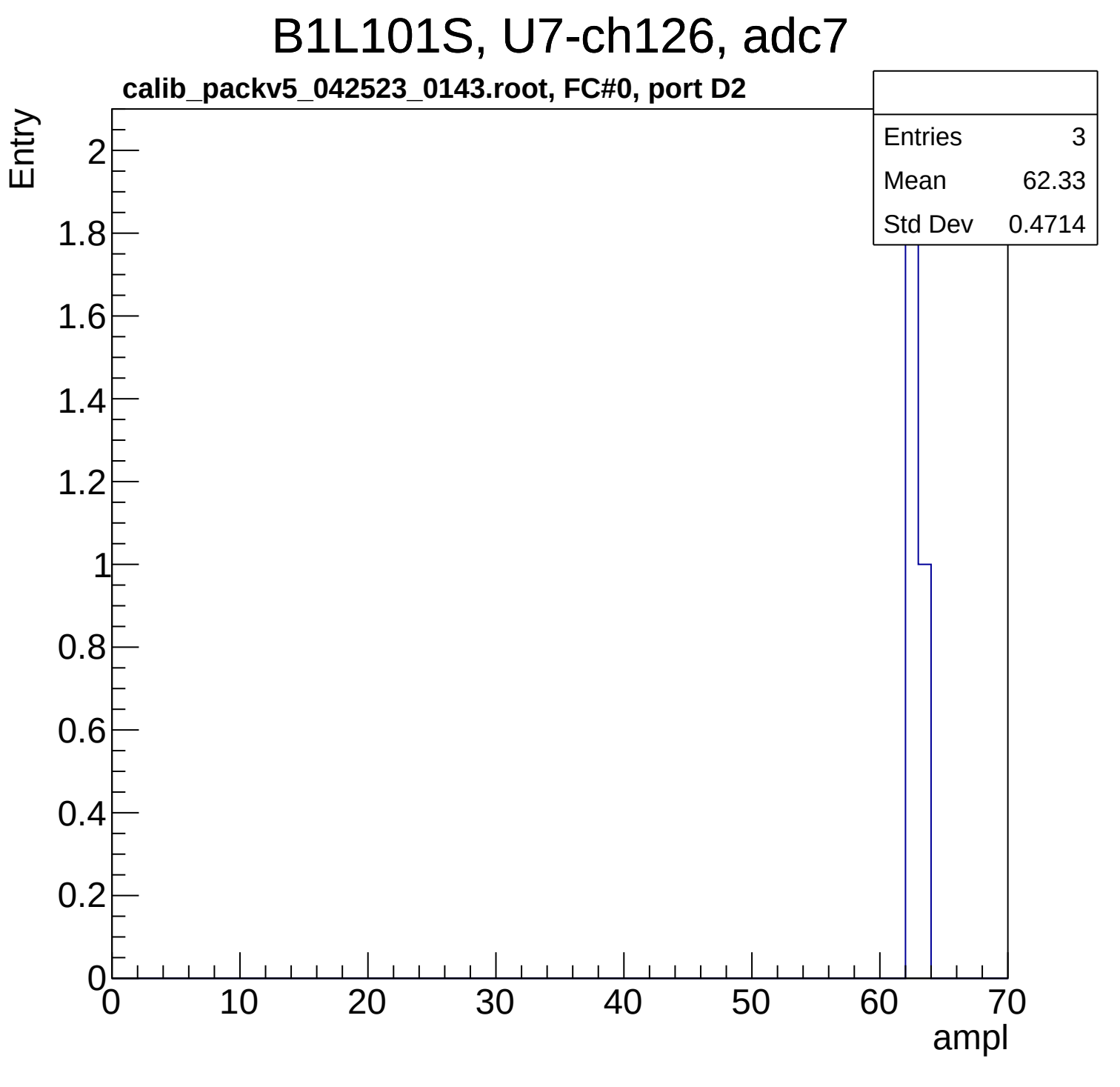
B1L101S, U7-ch126, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
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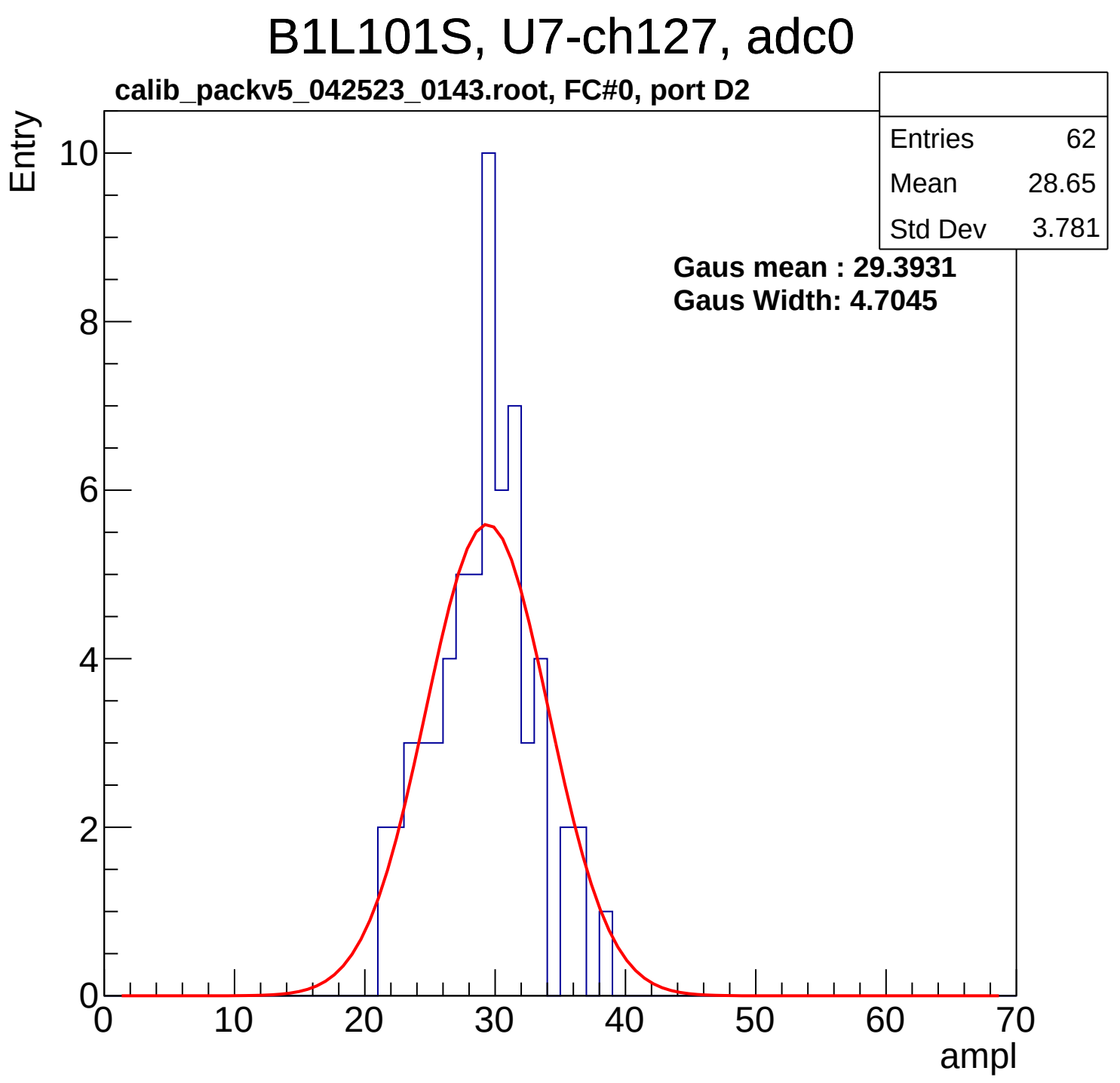
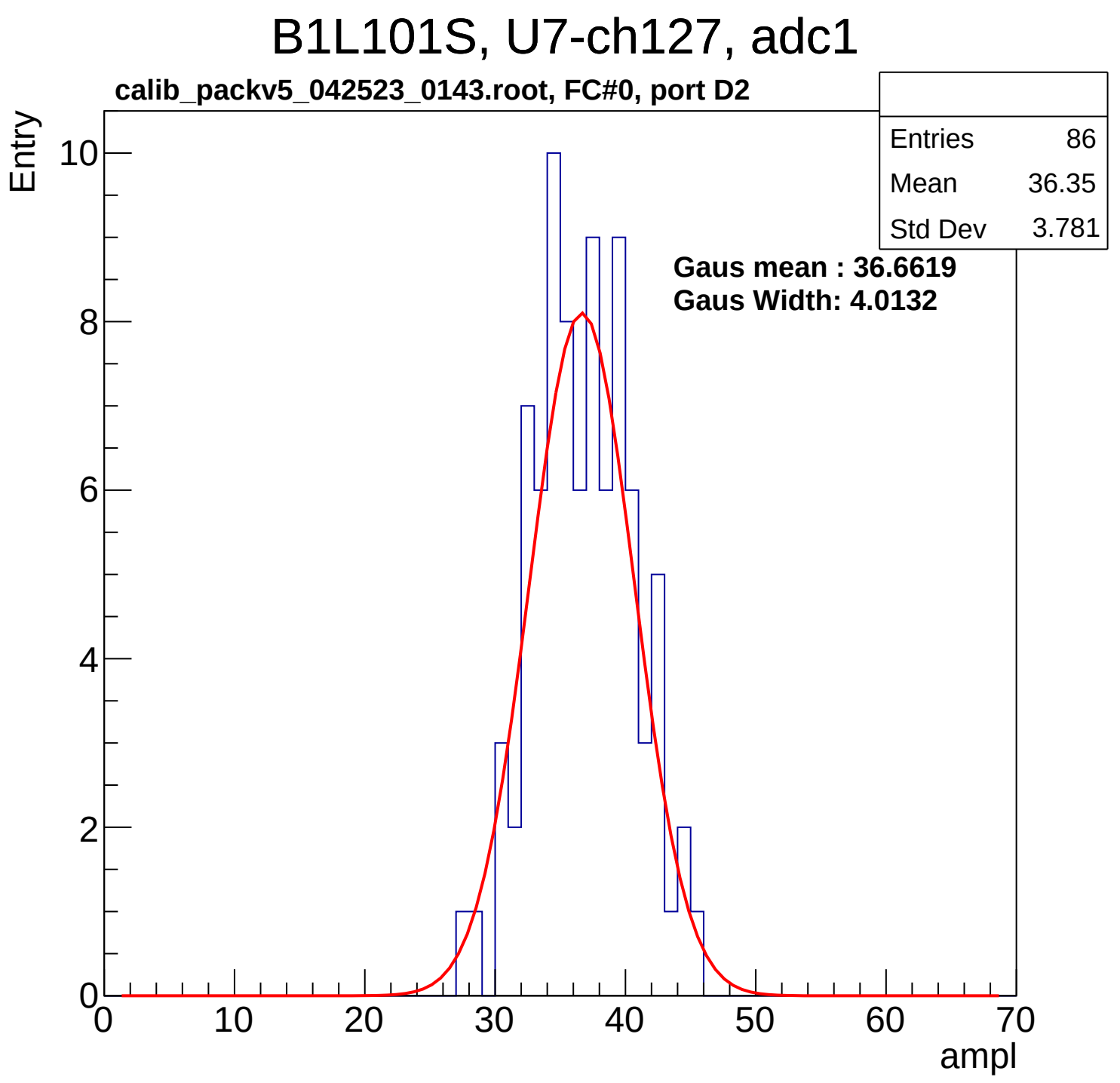
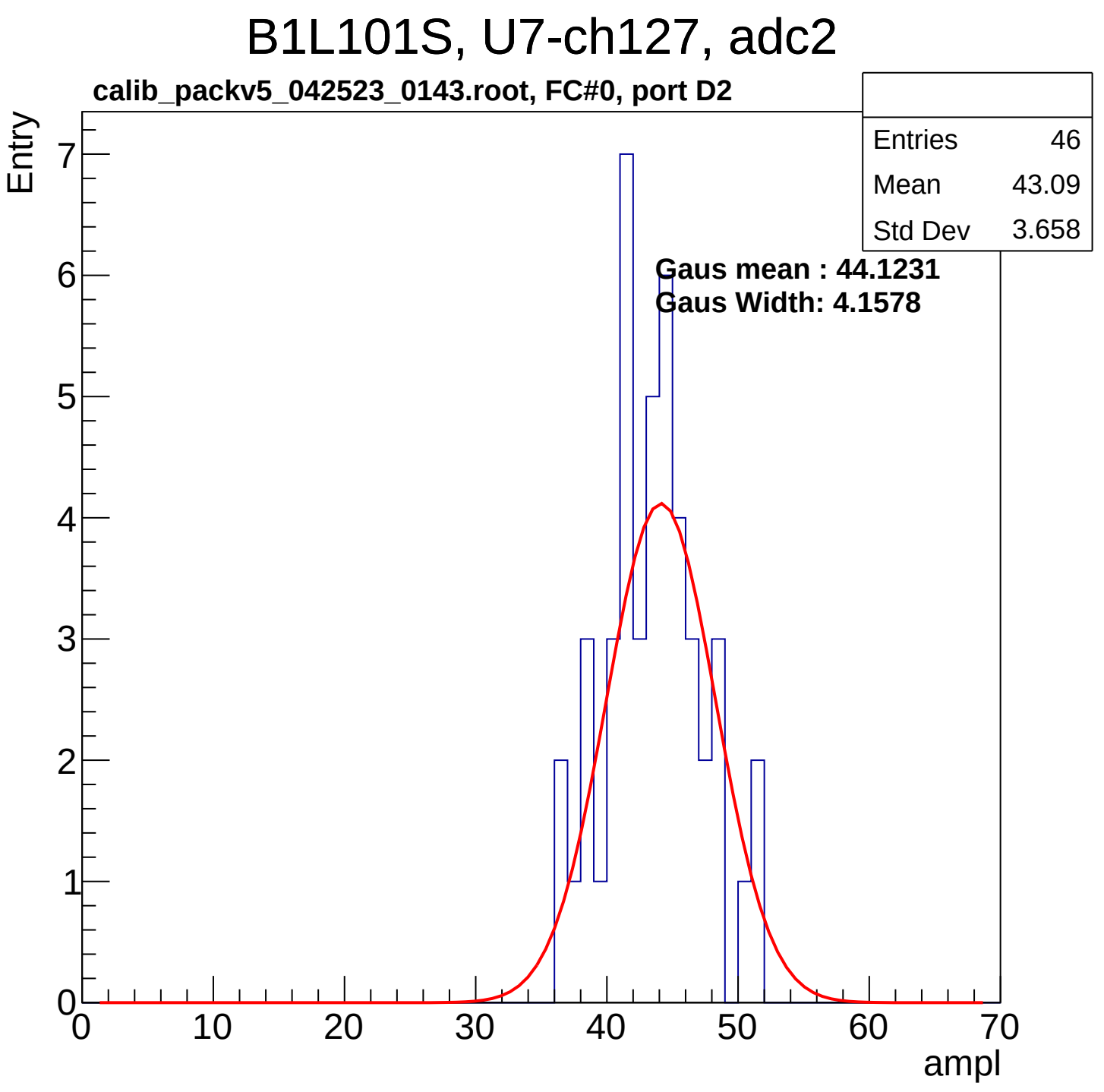
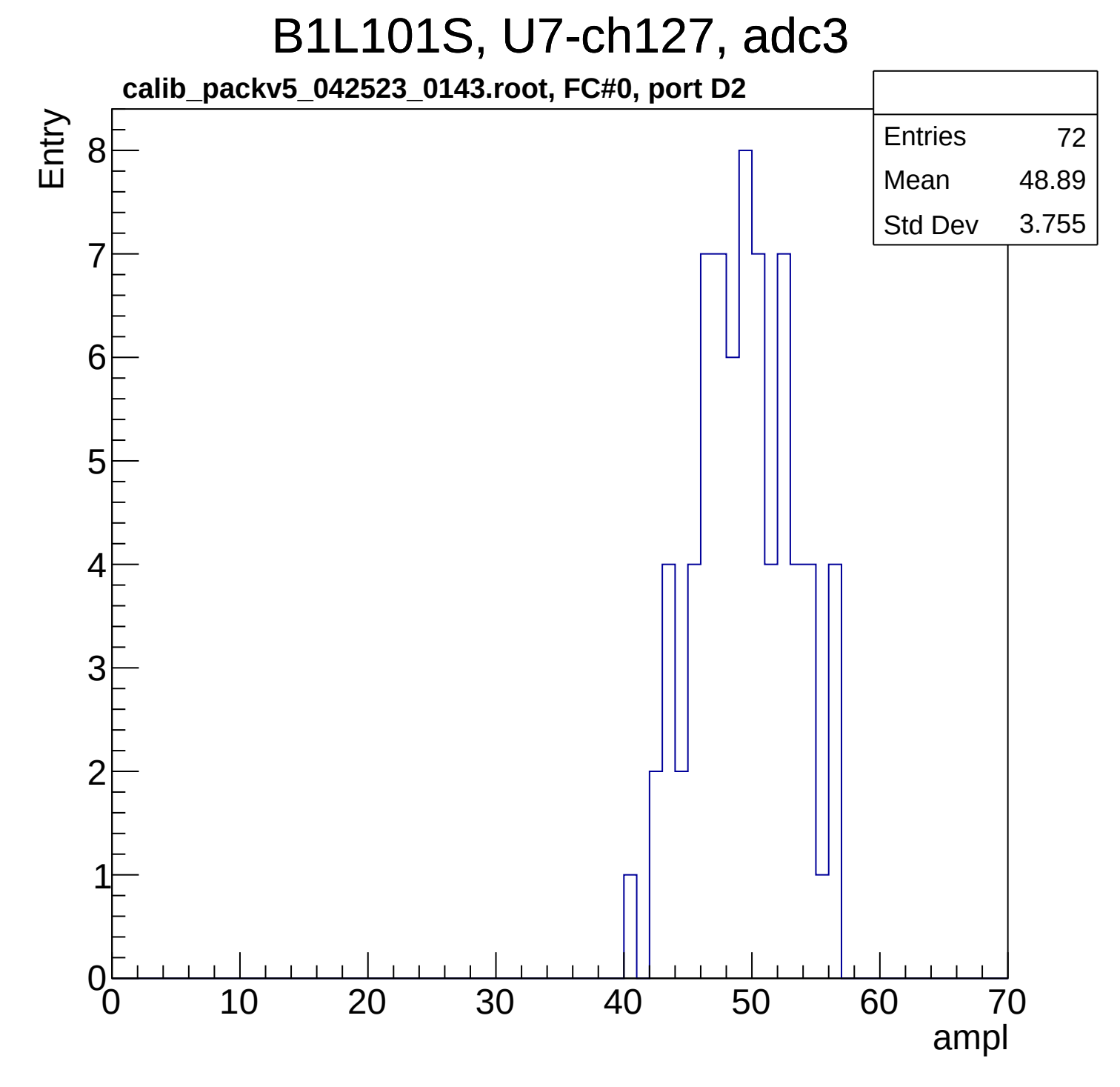
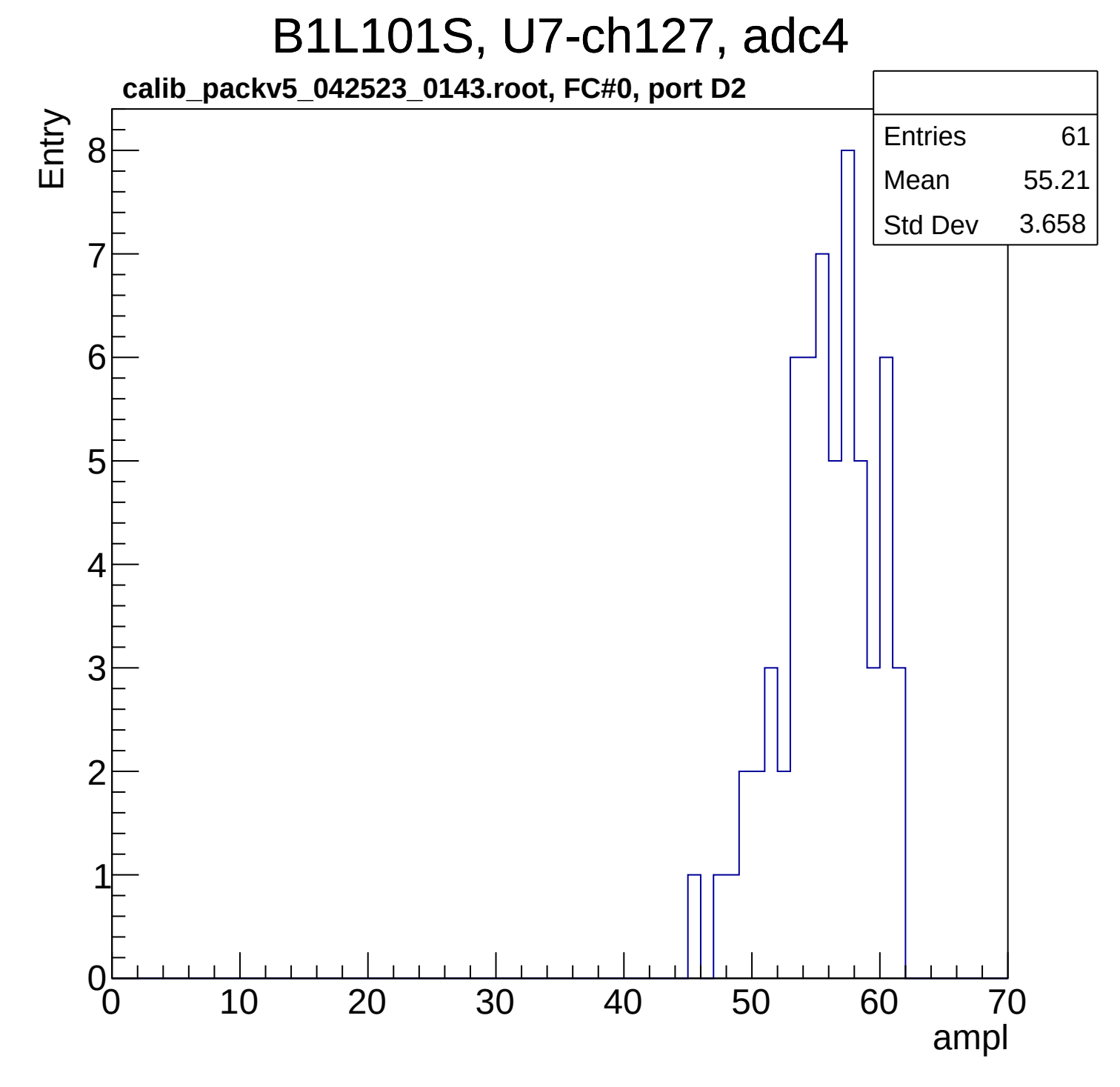
60
70

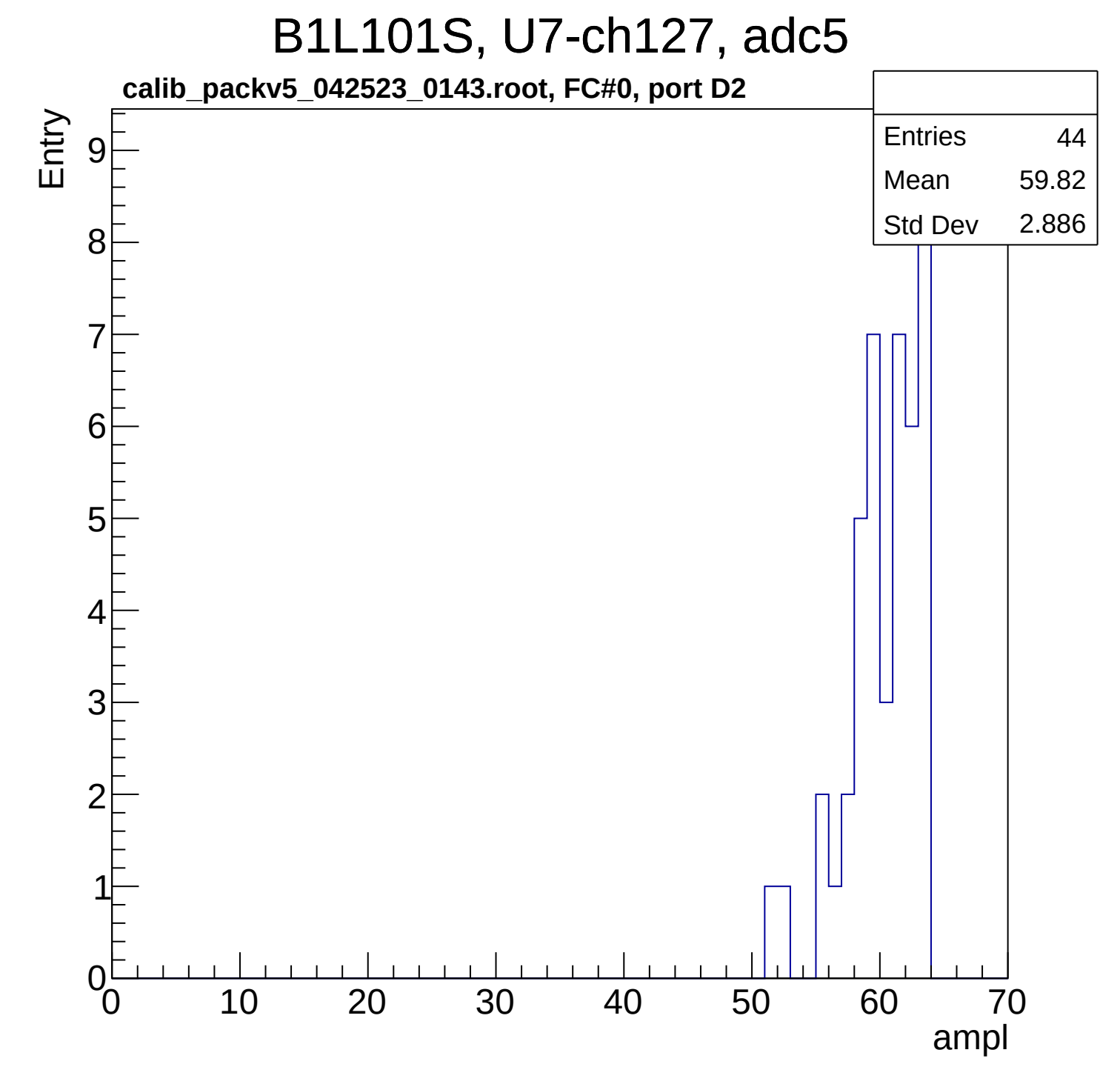

B1L101S, U7-ch127, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 28.65
Std Dev 3.781
Gaus mean : 29.3931
Gaus Width: 4.7045
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

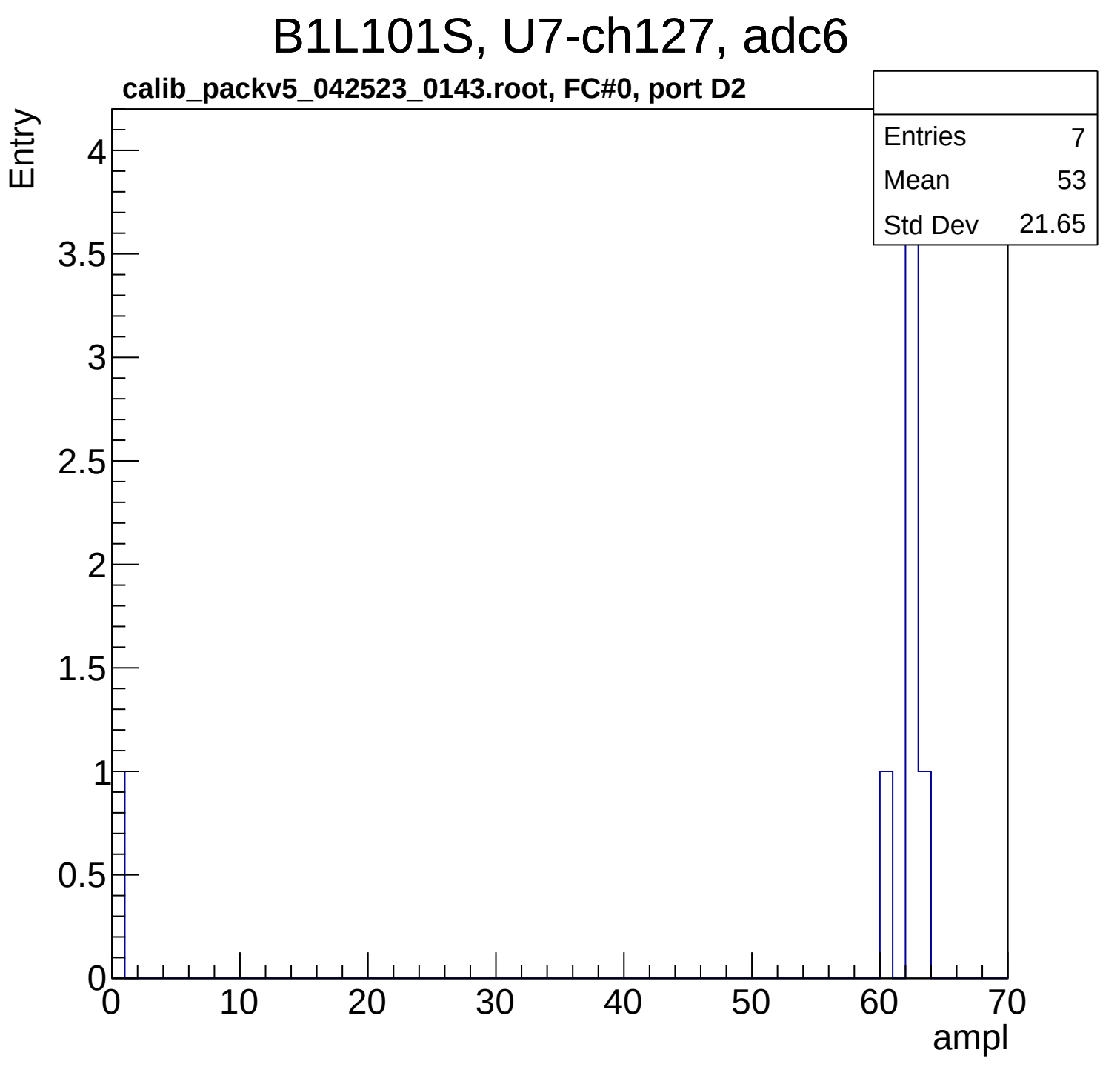

B1L101S, U7-ch127, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 86
Mean 36.35
Std Dev 3.781
Gaus mean : 36.6619
Gaus Width: 4.0132
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

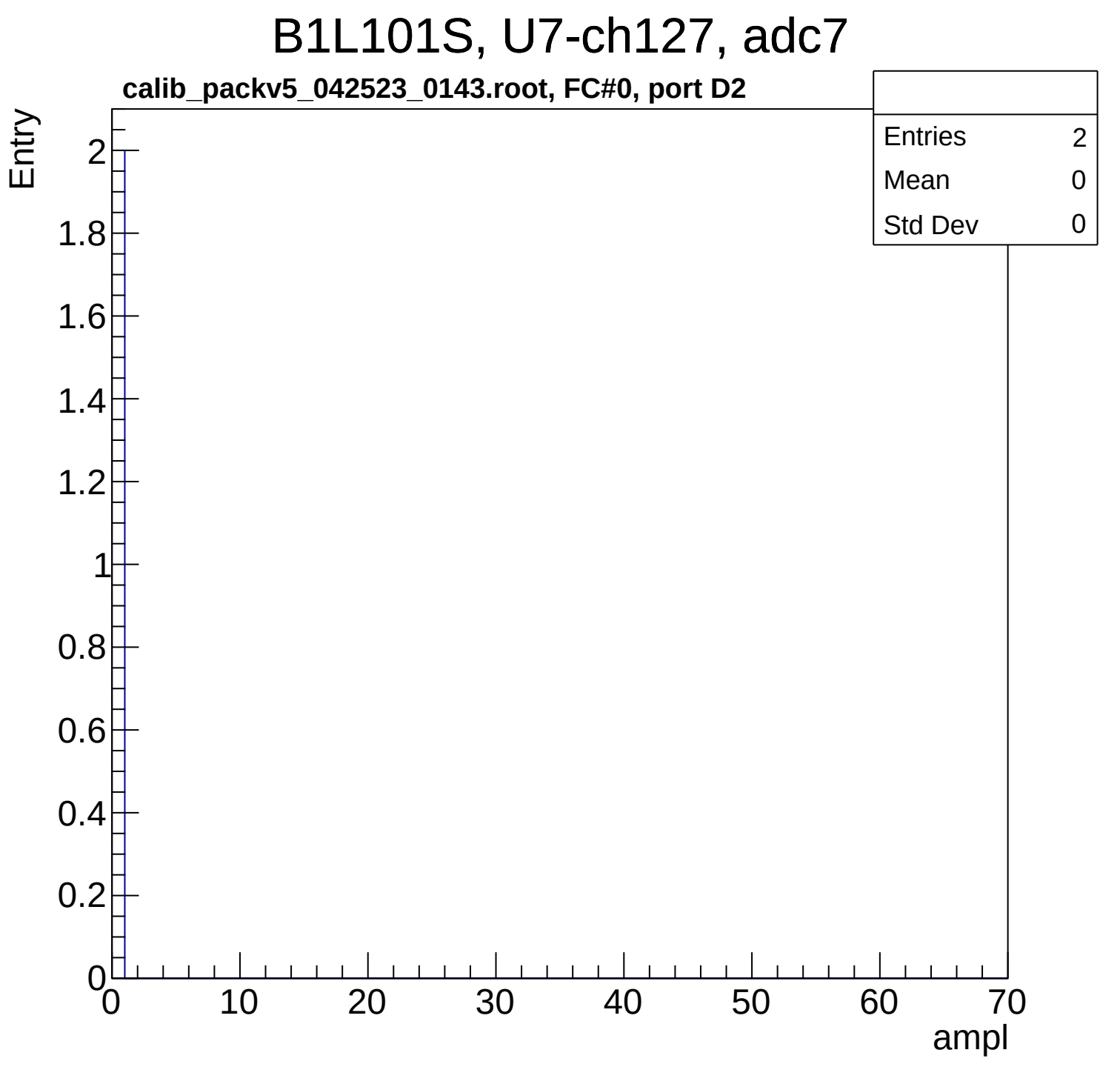

B1L101S, U7-ch127, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 43.09
Std Dev 3.658
Gaus mean : 44.1231
Gaus Width: 4.1578
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

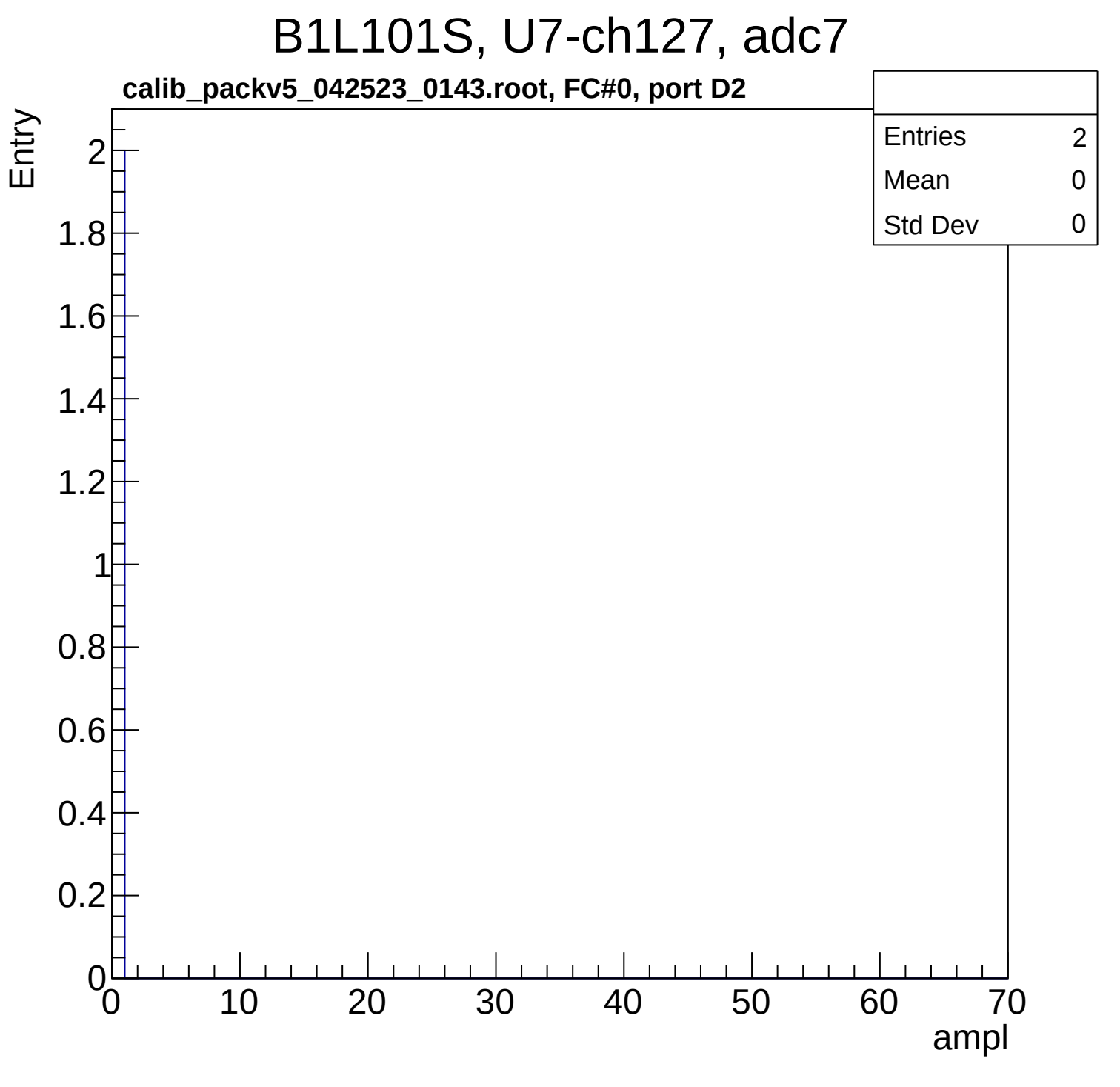

B1L101S, U7-ch127, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 48.89
Std Dev 3.755
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch127, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 55.21
Std Dev 3.658
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U7-ch127, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 44
Mean 59.82
Std Dev 2.886
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U7-ch127, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 53
Std Dev 21.65
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L101S, U7-ch127, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U7-ch127, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70