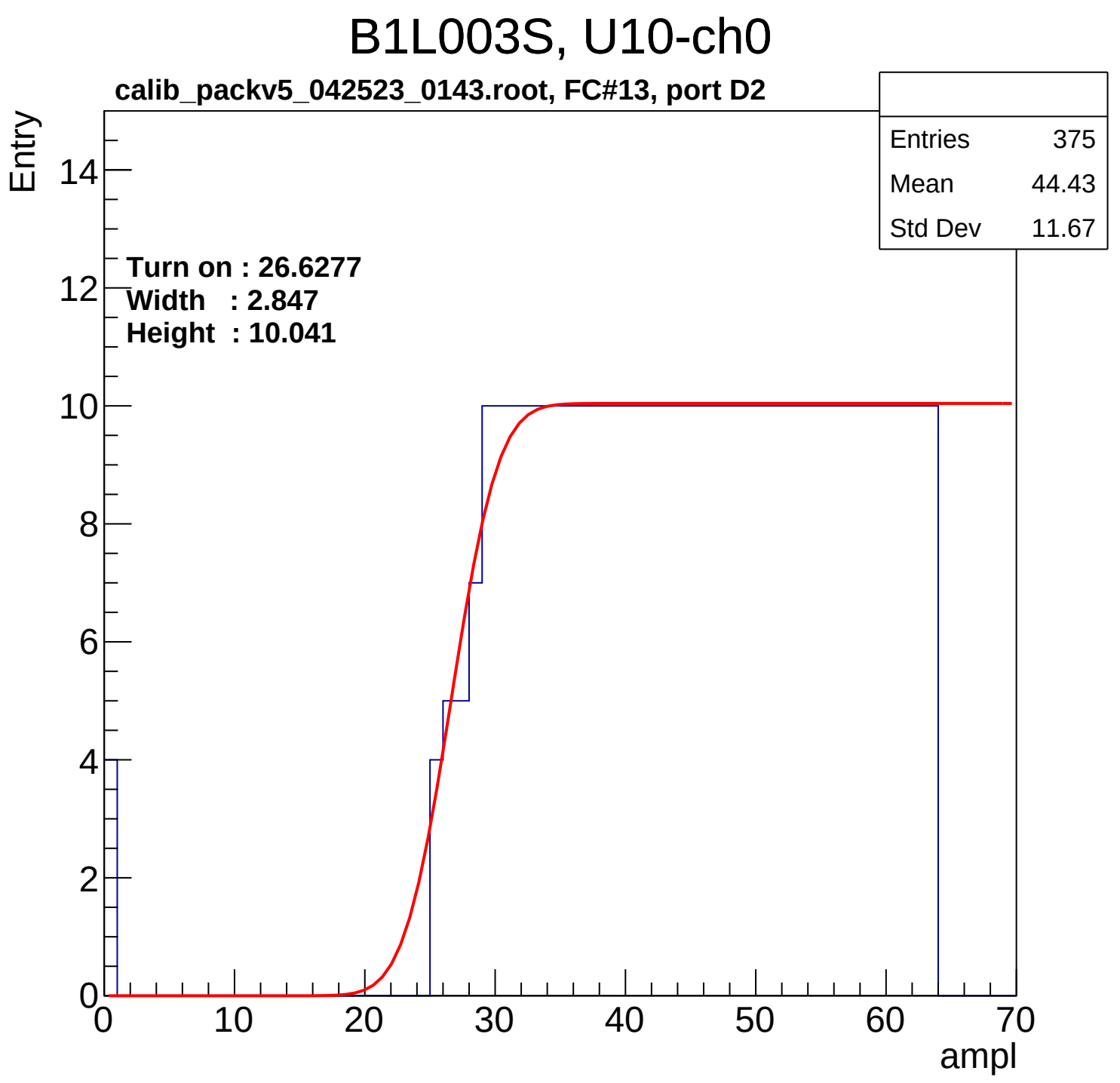
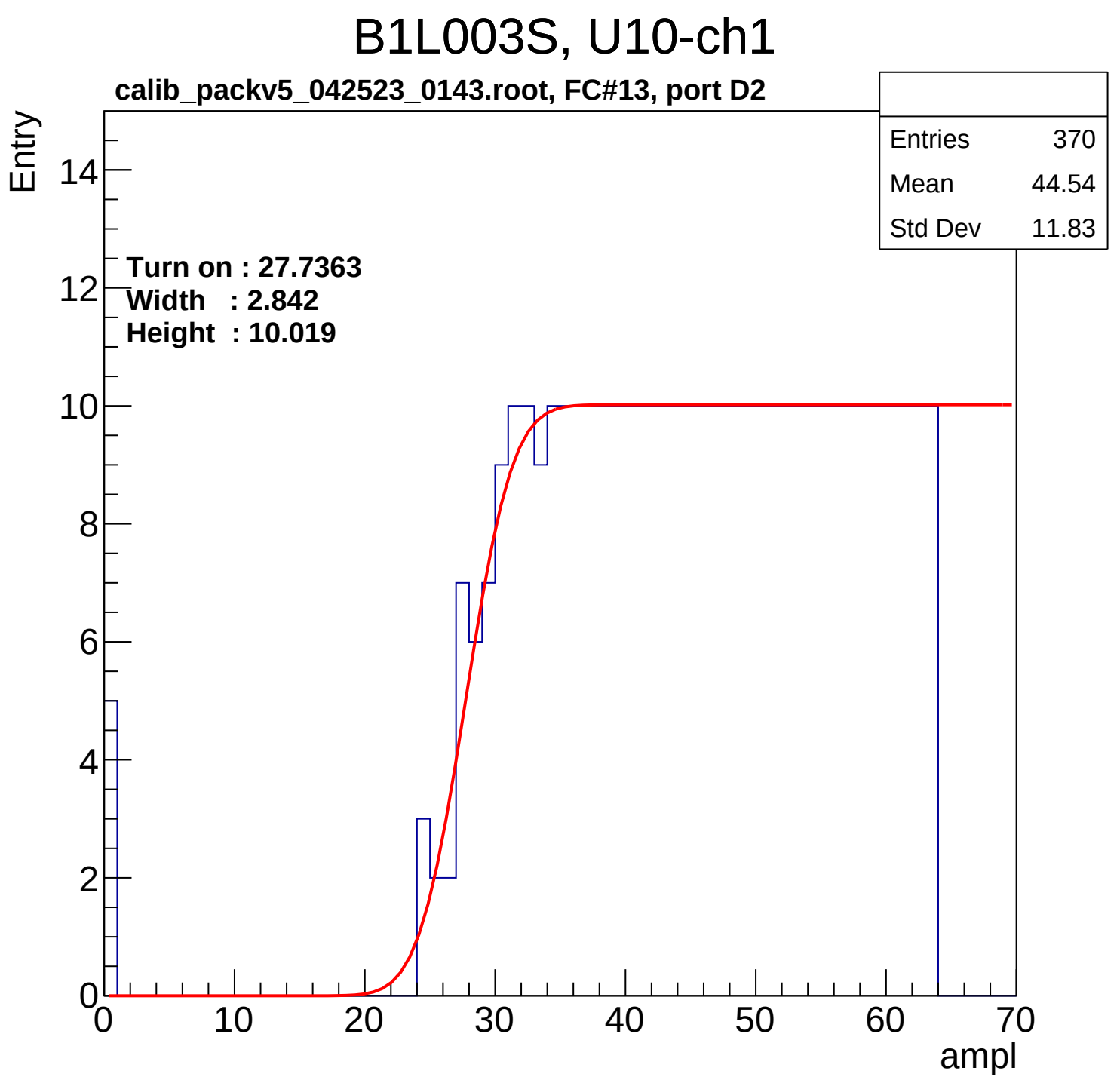
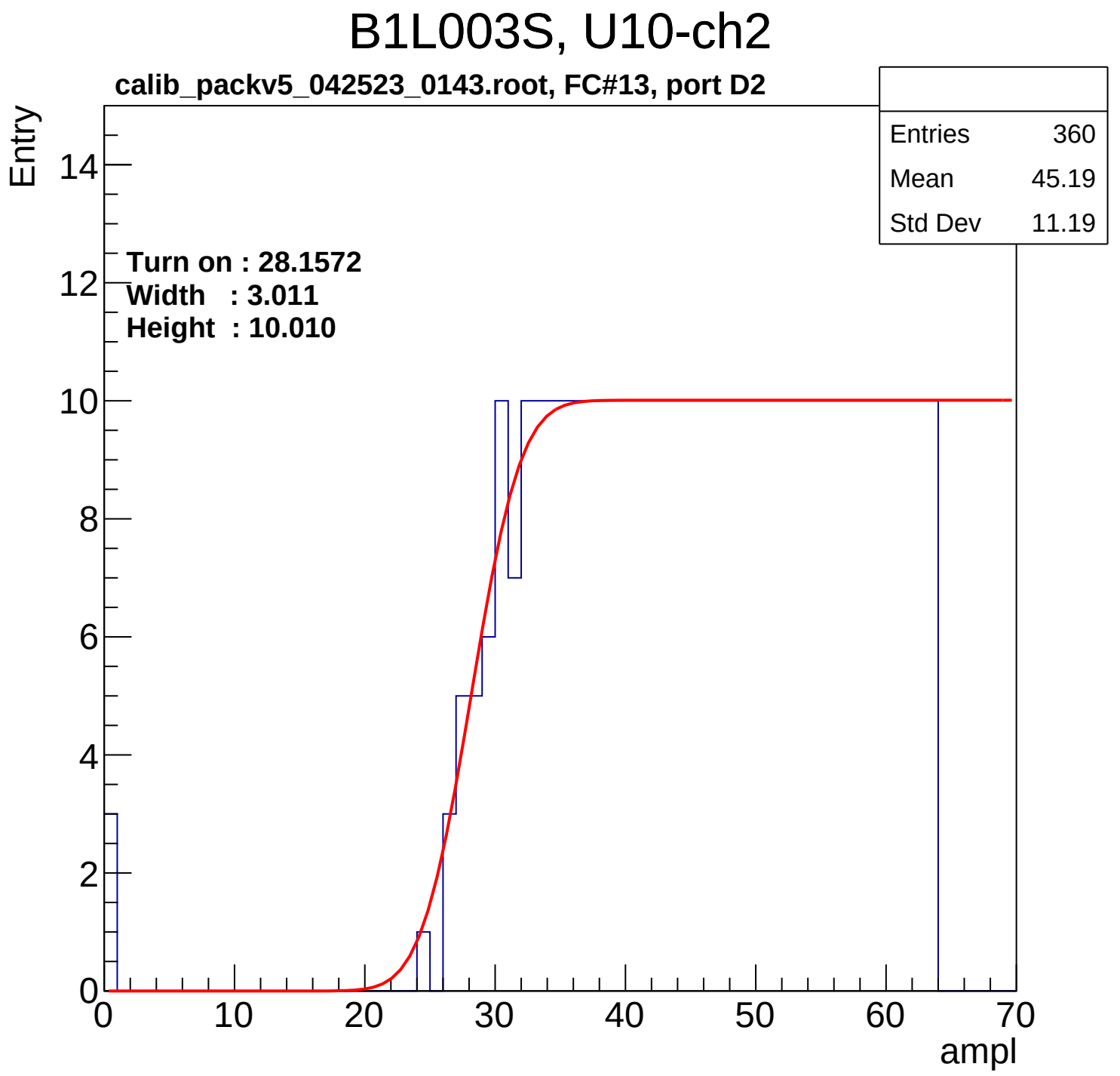
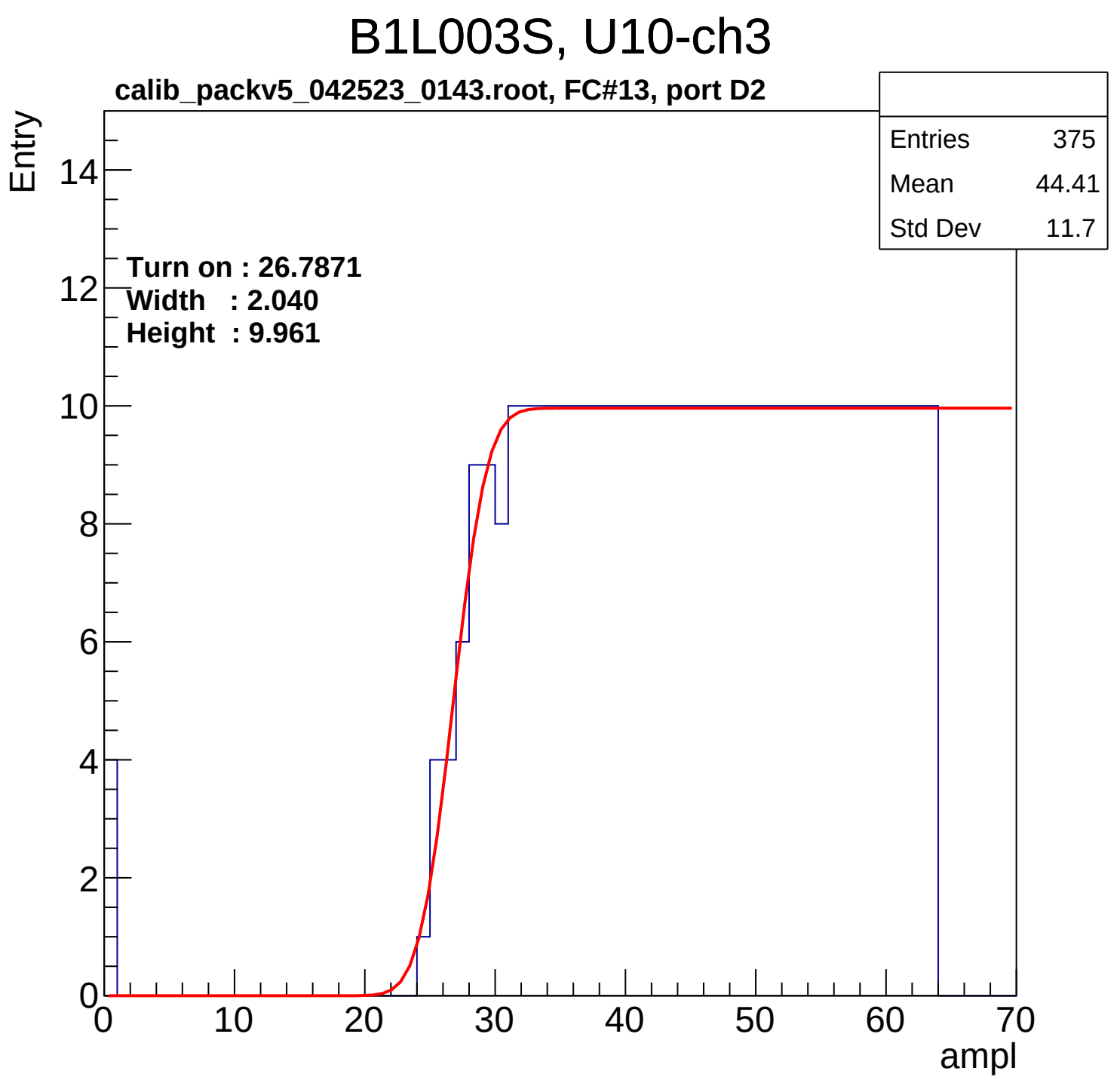
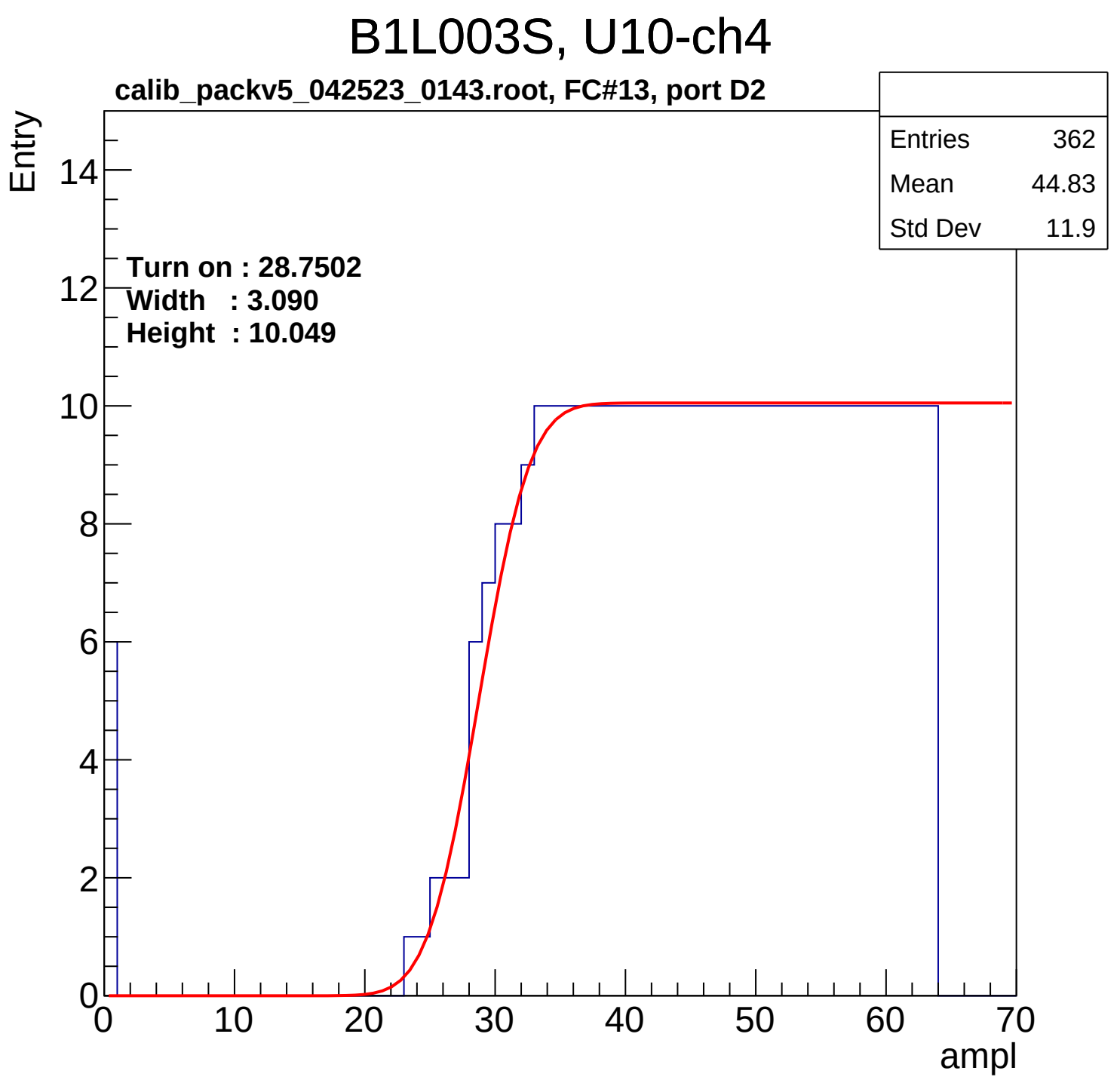
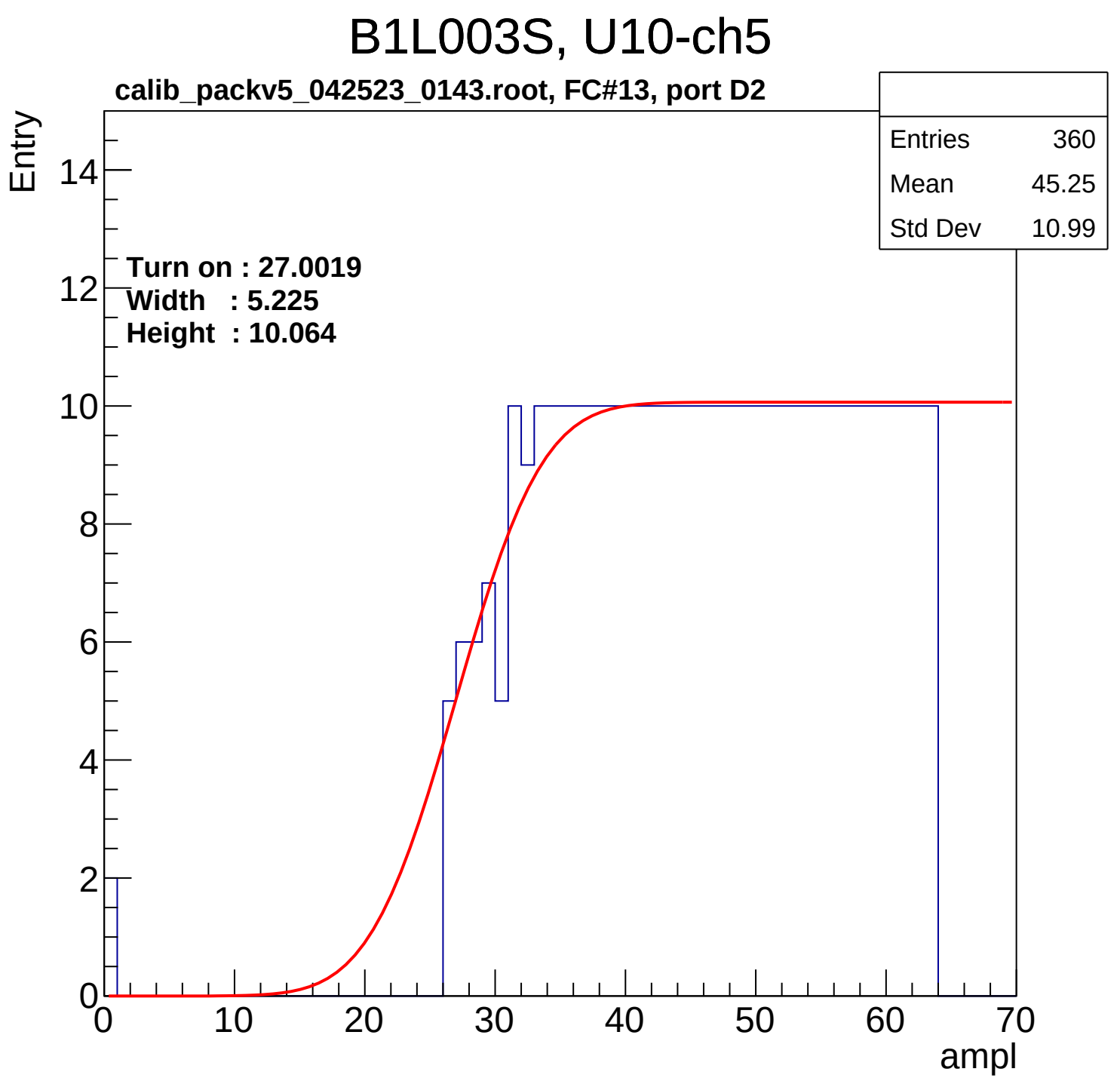

B1L003S, U10-ch0
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.43
Std Dev 11.67
Turn on : 26.6277
Width : 2.847
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

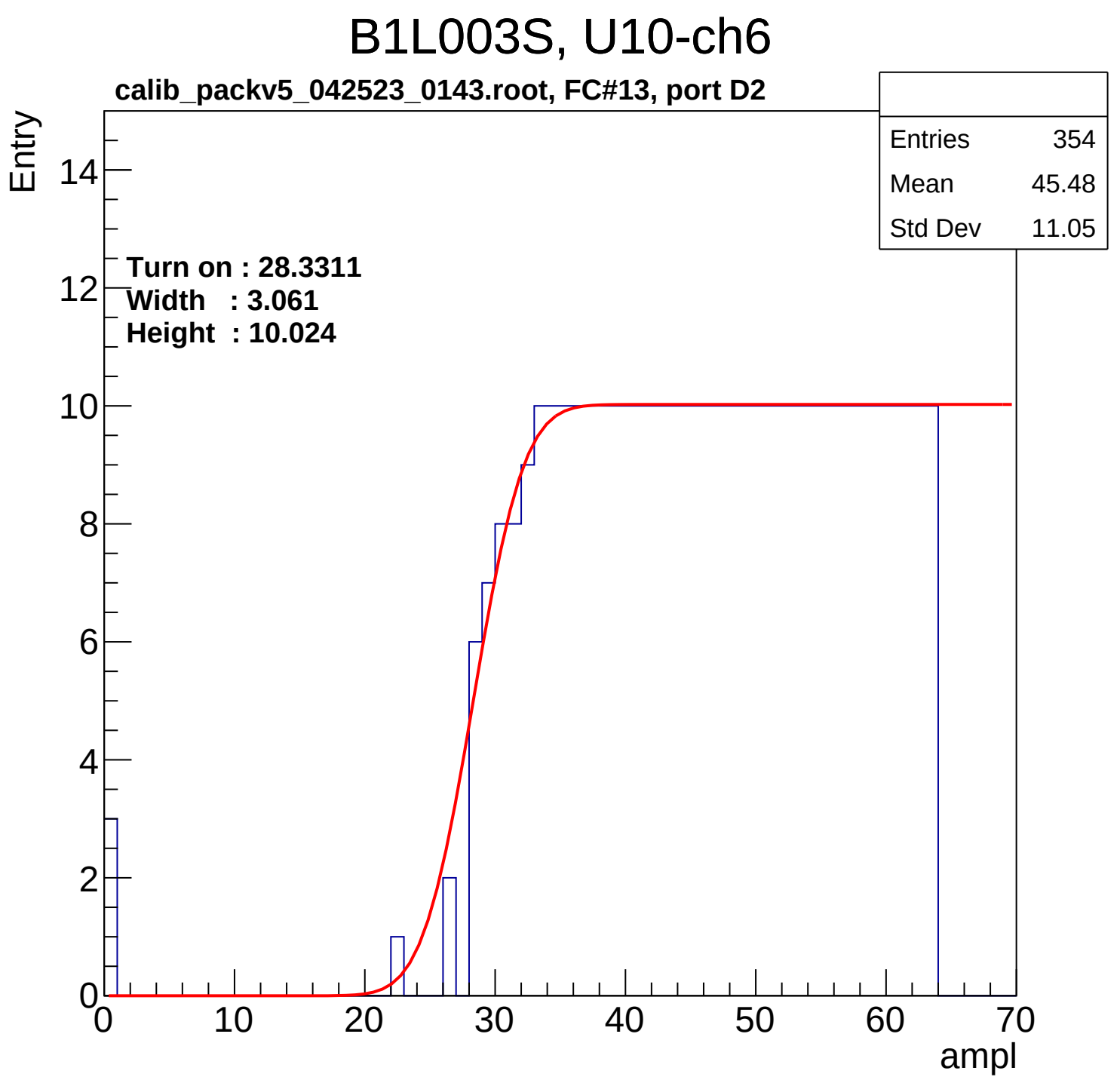

B1L003S, U10-ch1
calib_packv5_042523_0143.root, FC#13, port D2
Entries 370
Mean 44.54
Std Dev 11.83
Turn on : 27.7363
Width : 2.842
Height : 10.019
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

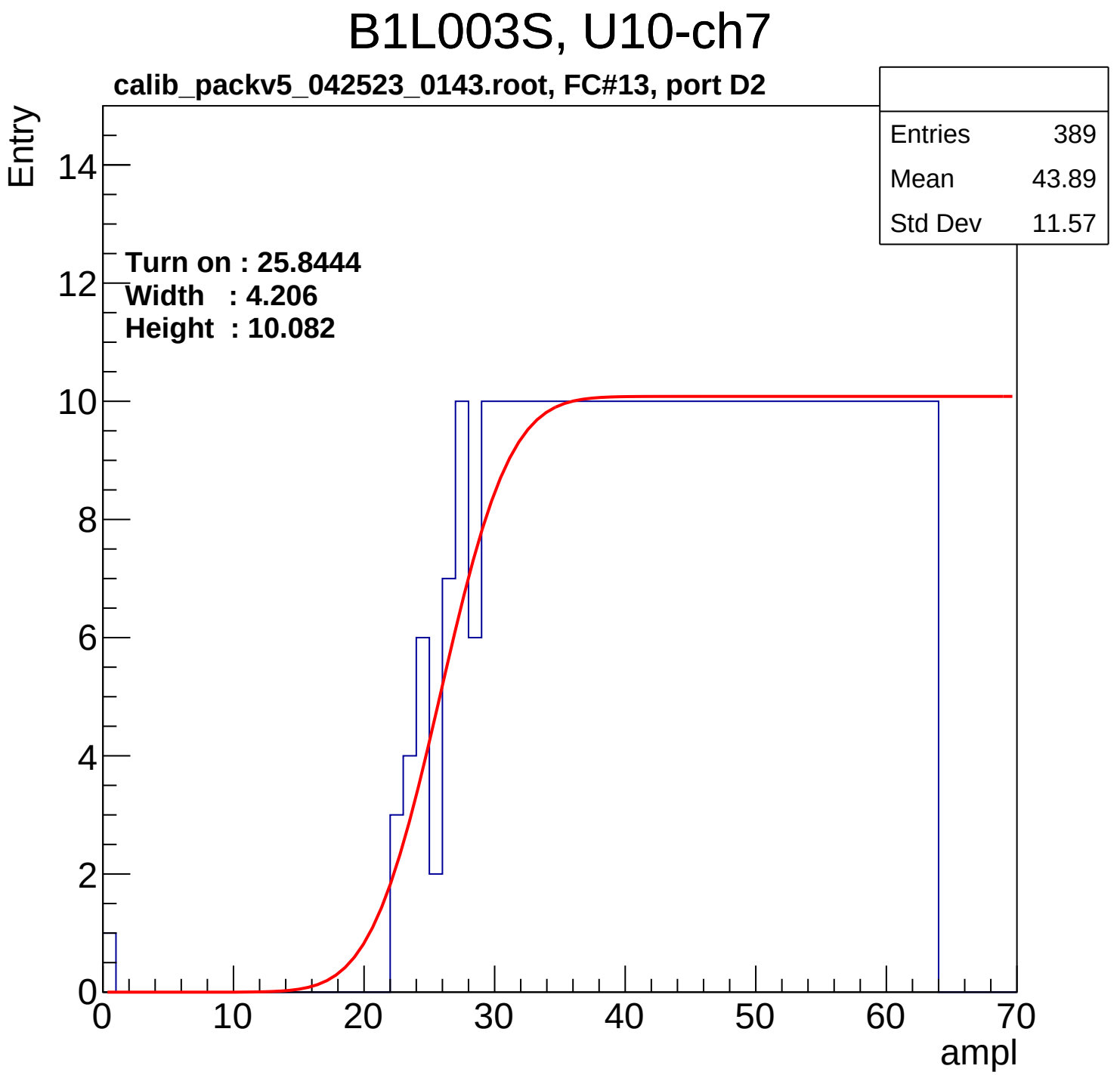

B1L003S, U10-ch2
calib_packv5_042523_0143.root, FC#13, port D2
Entries 360
Mean 45.19
Std Dev 11.19
Turn on : 28.1572
Width : 3.011
Height : 10.010
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

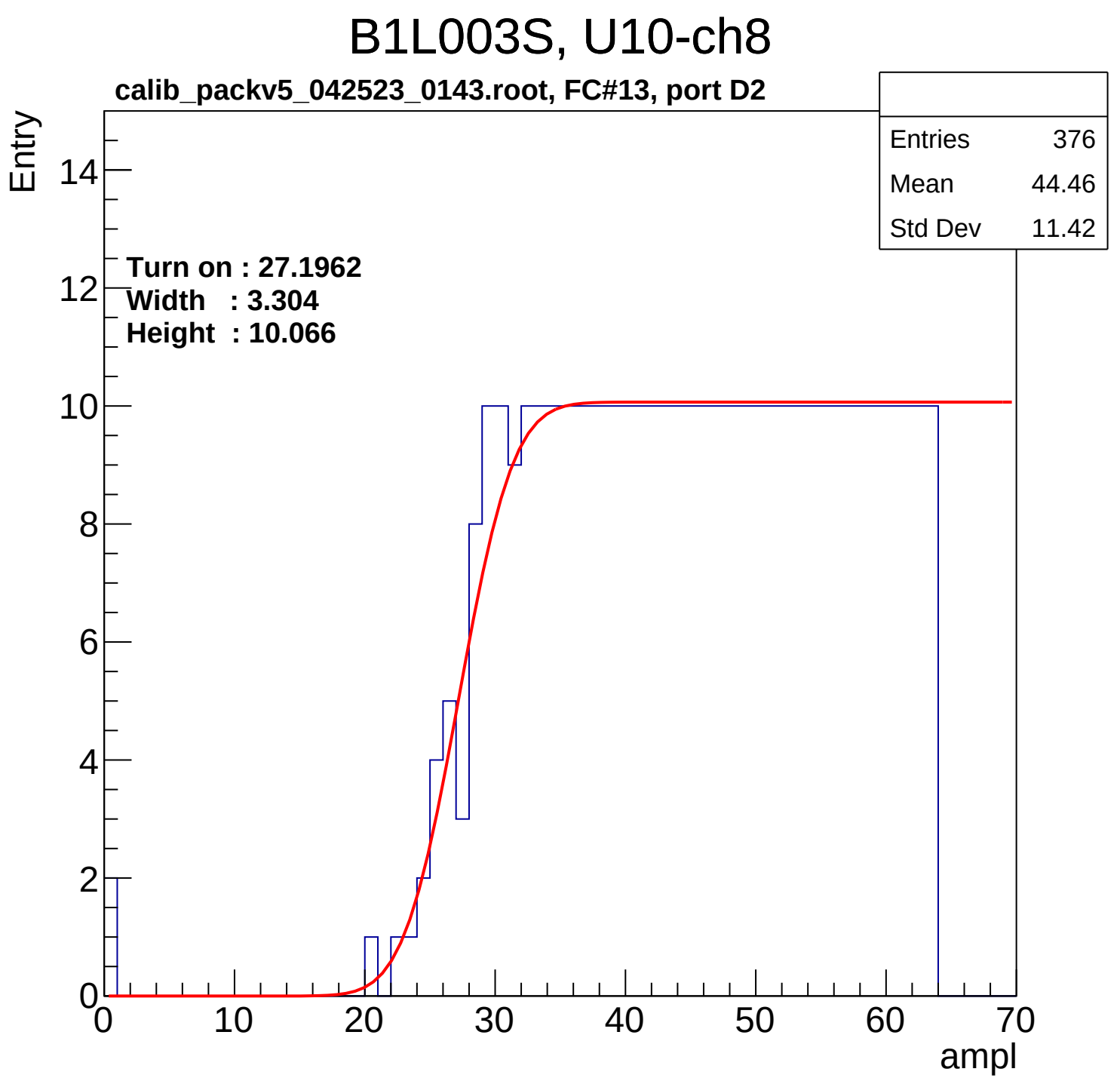

B1L003S, U10-ch3
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.41
Std Dev 11.7
Turn on : 26.7871
Width : 2.040
Height : 9.961
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

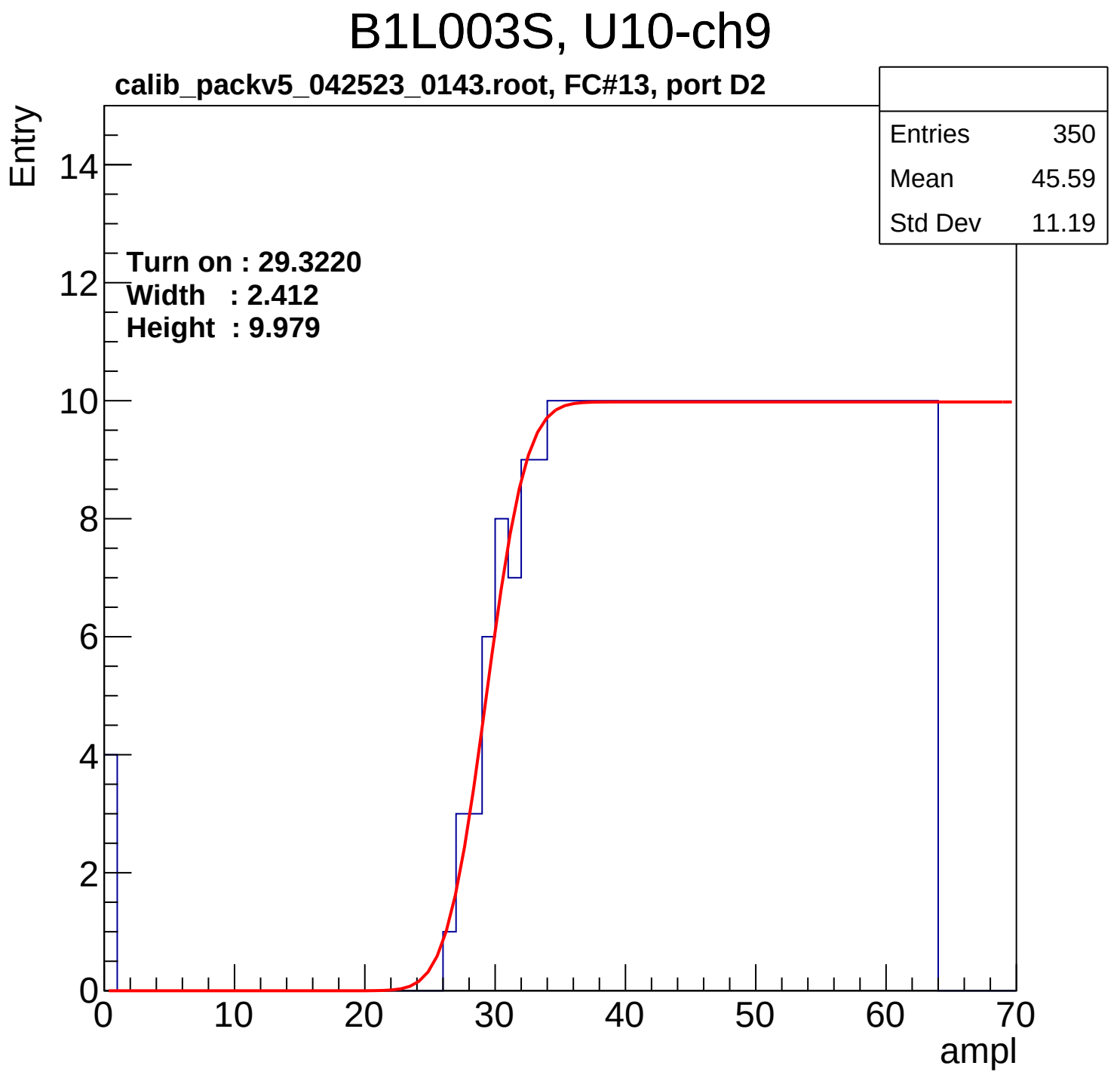

B1L003S, U10-ch4
calib_packv5_042523_0143.root, FC#13, port D2
Entries 362
Mean 44.83
Std Dev 11.9
Turn on : 28.7502
Width : 3.090
Height : 10.049
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

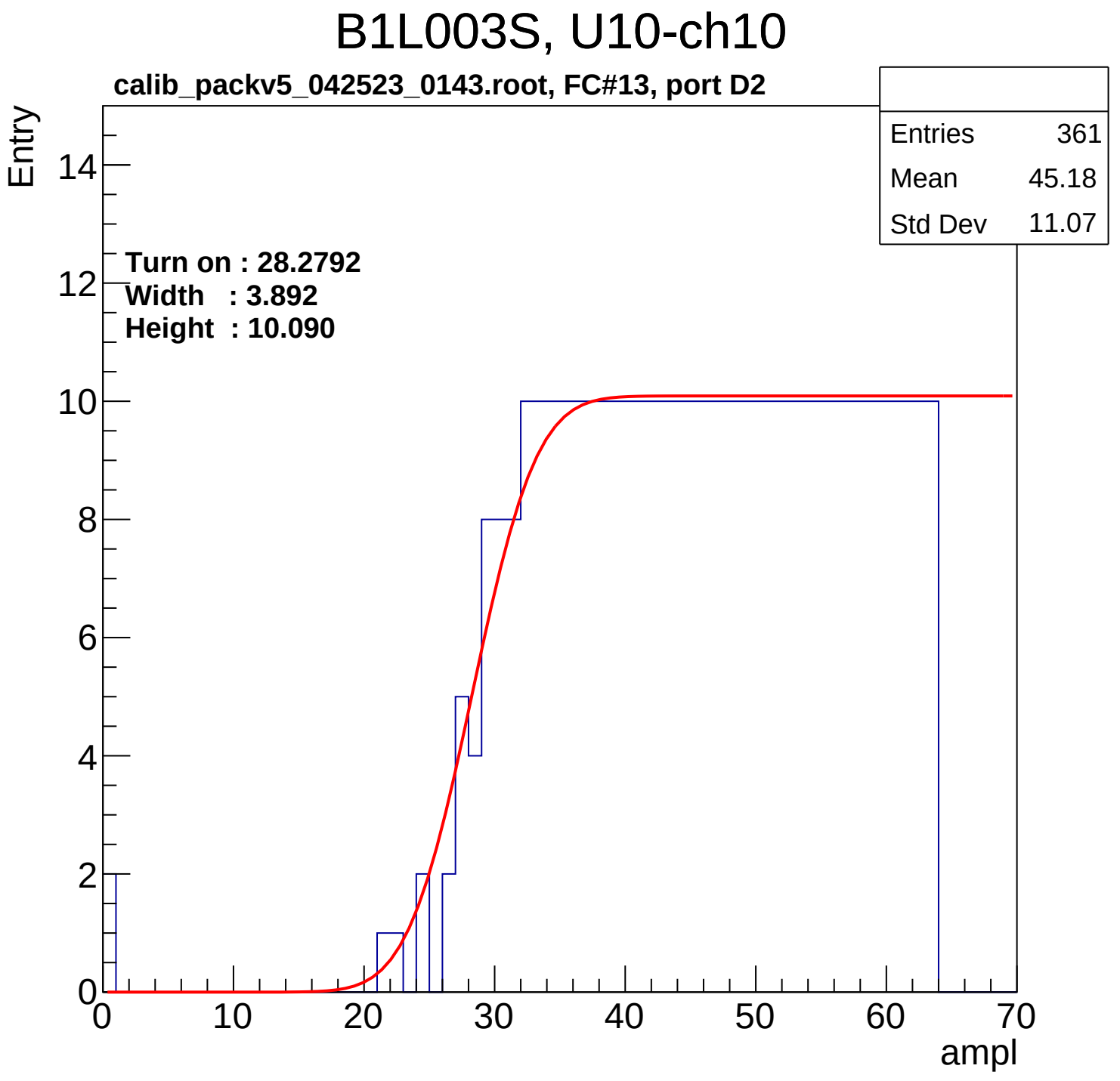

B1L003S, U10-ch5
calib_packv5_042523_0143.root, FC#13, port D2
Entries 360
Mean 45.25
Std Dev 10.99
Turn on : 27.0019
Width : 5.225
Height : 10.064
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

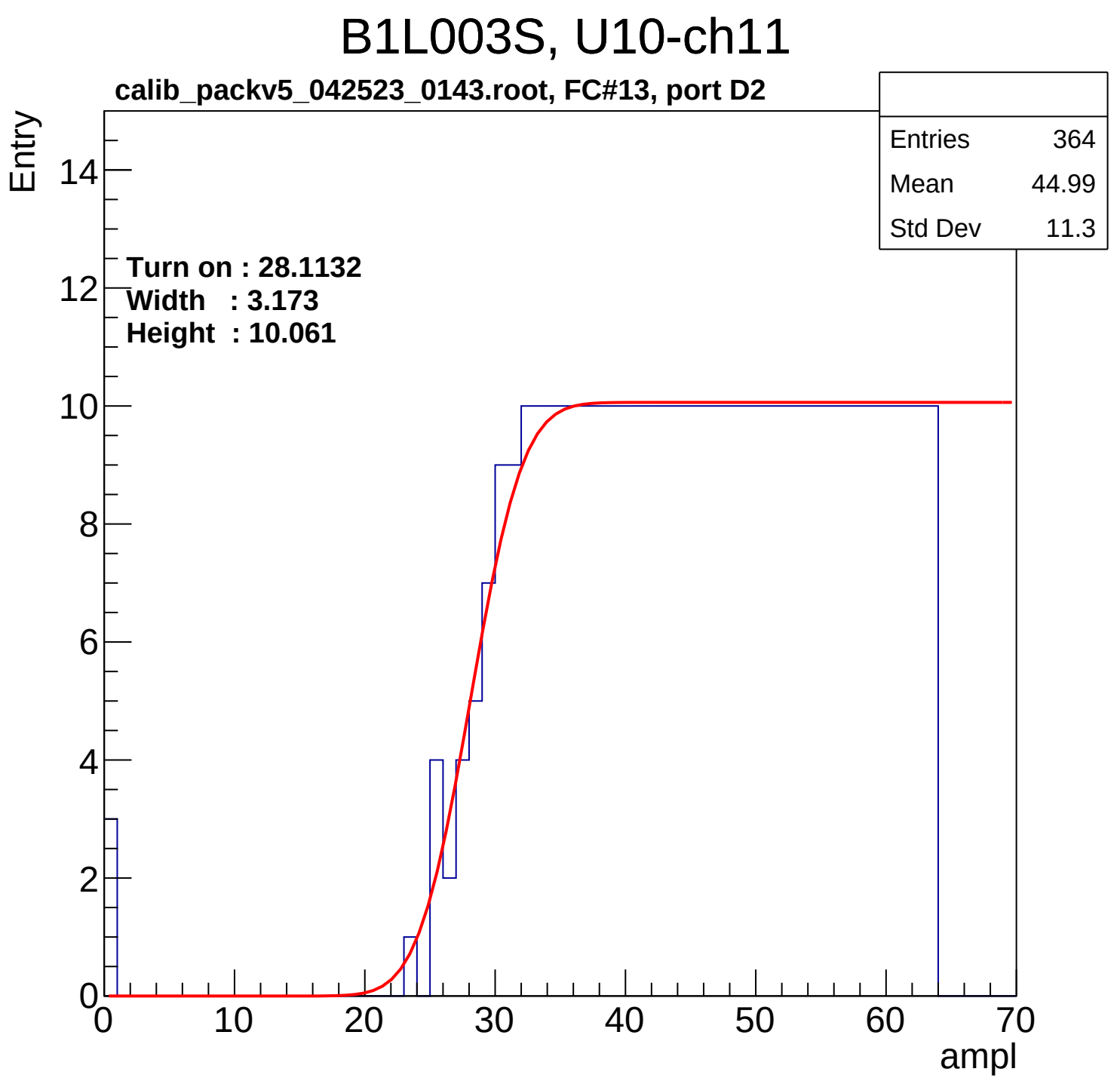

B1L003S, U10-ch6
calib_packv5_042523_0143.root, FC#13, port D2
Entries 354
Mean 45.48
Std Dev 11.05
Turn on : 28.3311
Width : 3.061
Height : 10.024
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

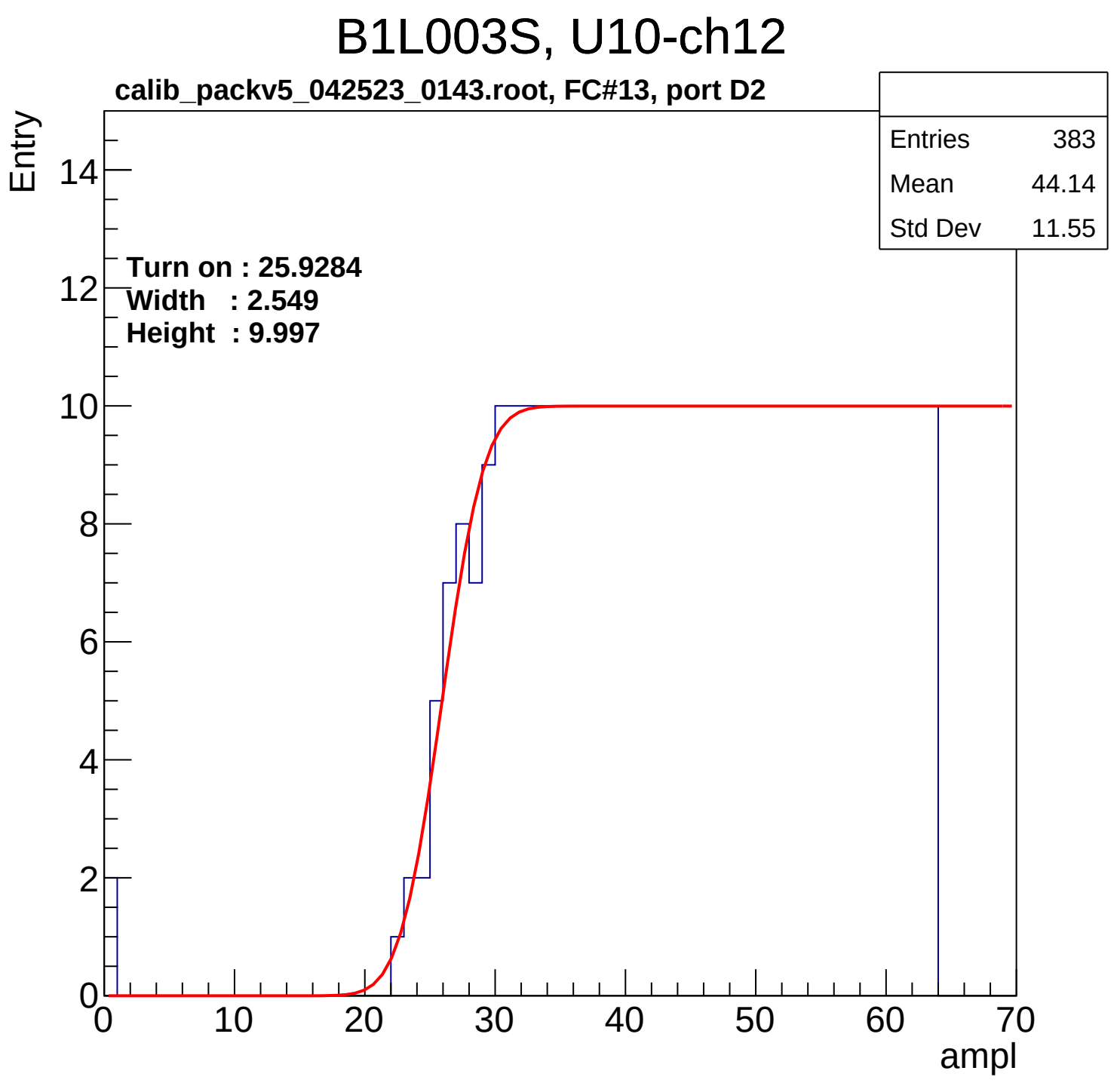

B1L003S, U10-ch7
calib_packv5_042523_0143.root, FC#13, port D2
Entries 389
Mean 43.89
Std Dev 11.57
Turn on : 25.8444
Width : 4.206
Height : 10.082
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

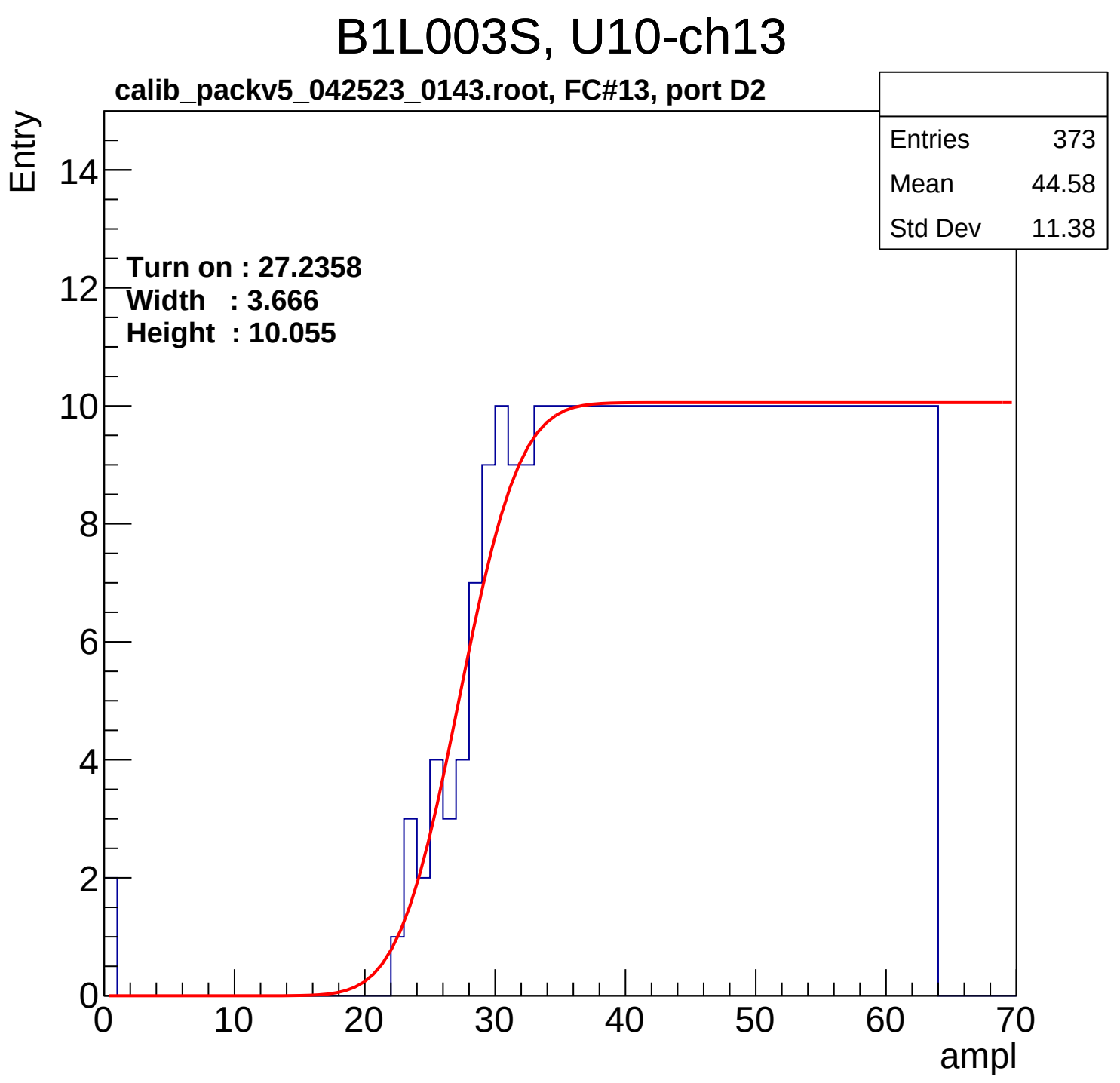

B1L003S, U10-ch8
calib_packv5_042523_0143.root, FC#13, port D2
Entries 376
Mean 44.46
Std Dev 11.42
Turn on : 27.1962
Width : 3.304
Height : 10.066
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

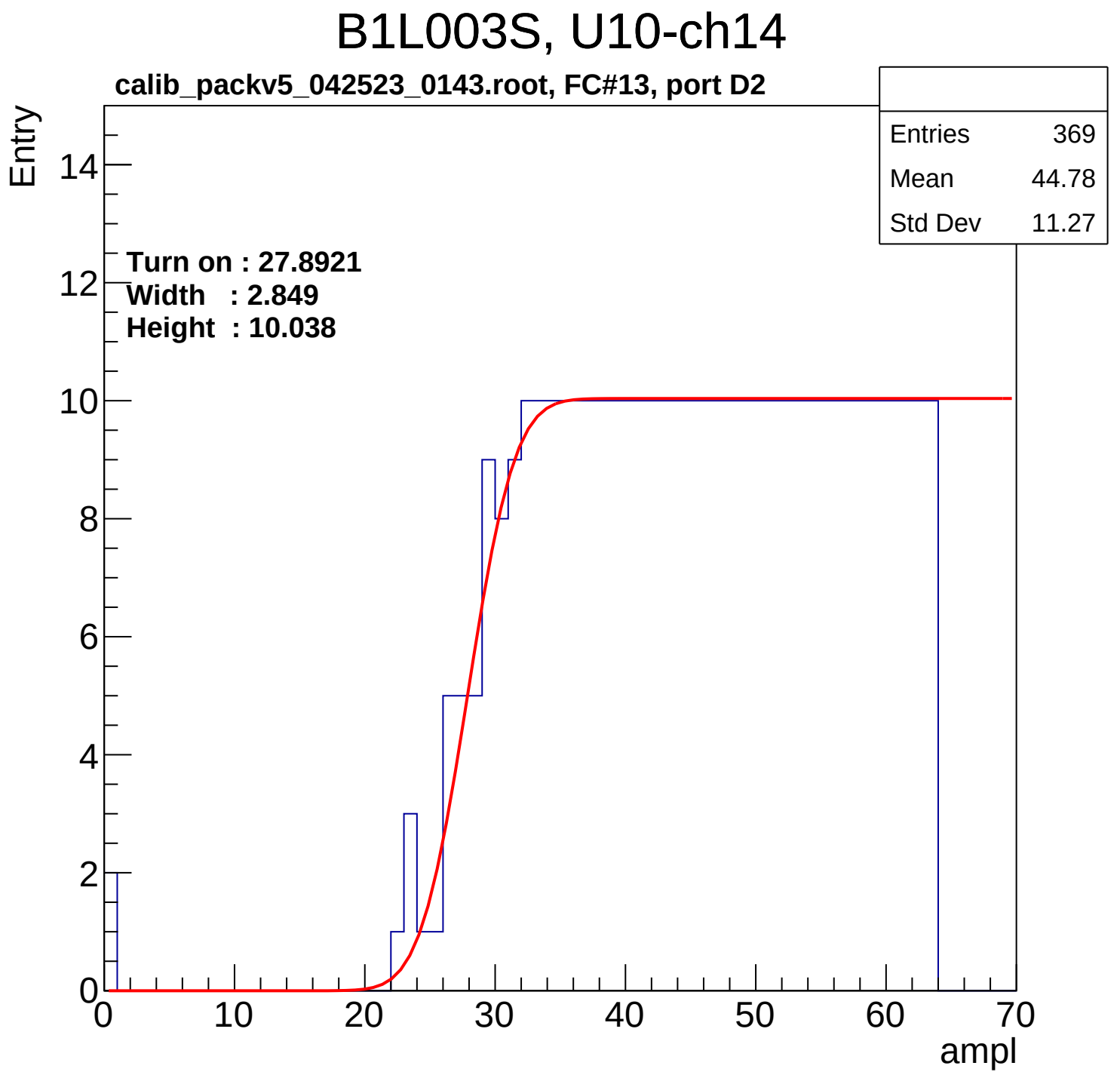

B1L003S, U10-ch9
calib_packv5_042523_0143.root, FC#13, port D2
Entries 350
Mean 45.59
Std Dev 11.19
Turn on : 29.3220
Width : 2.412
Height : 9.979
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

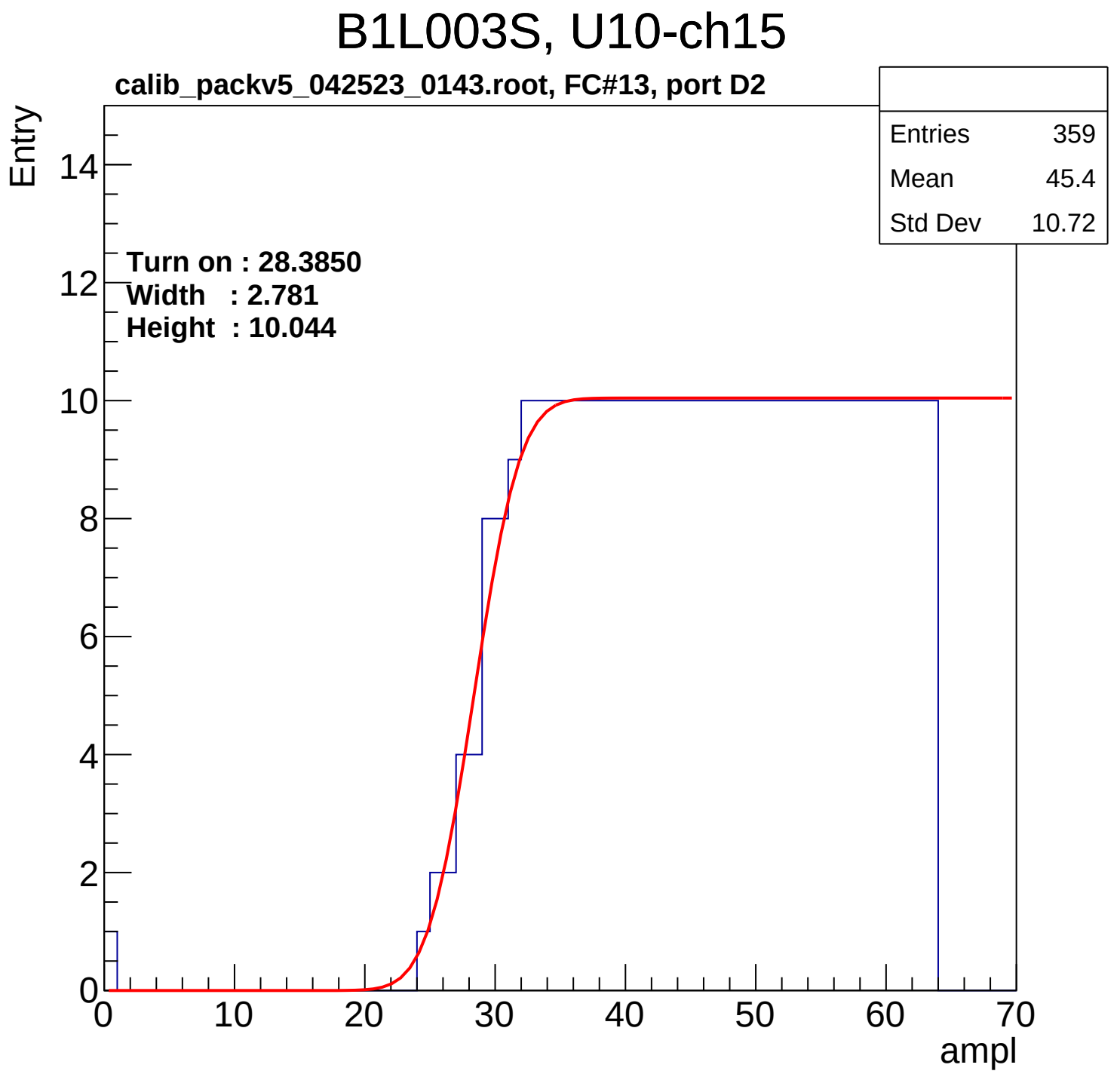

B1L003S, U10-ch10
calib_packv5_042523_0143.root, FC#13, port D2
Entries 361
Mean 45.18
Std Dev 11.07
Turn on : 28.2792
Width : 3.892
Height : 10.090
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

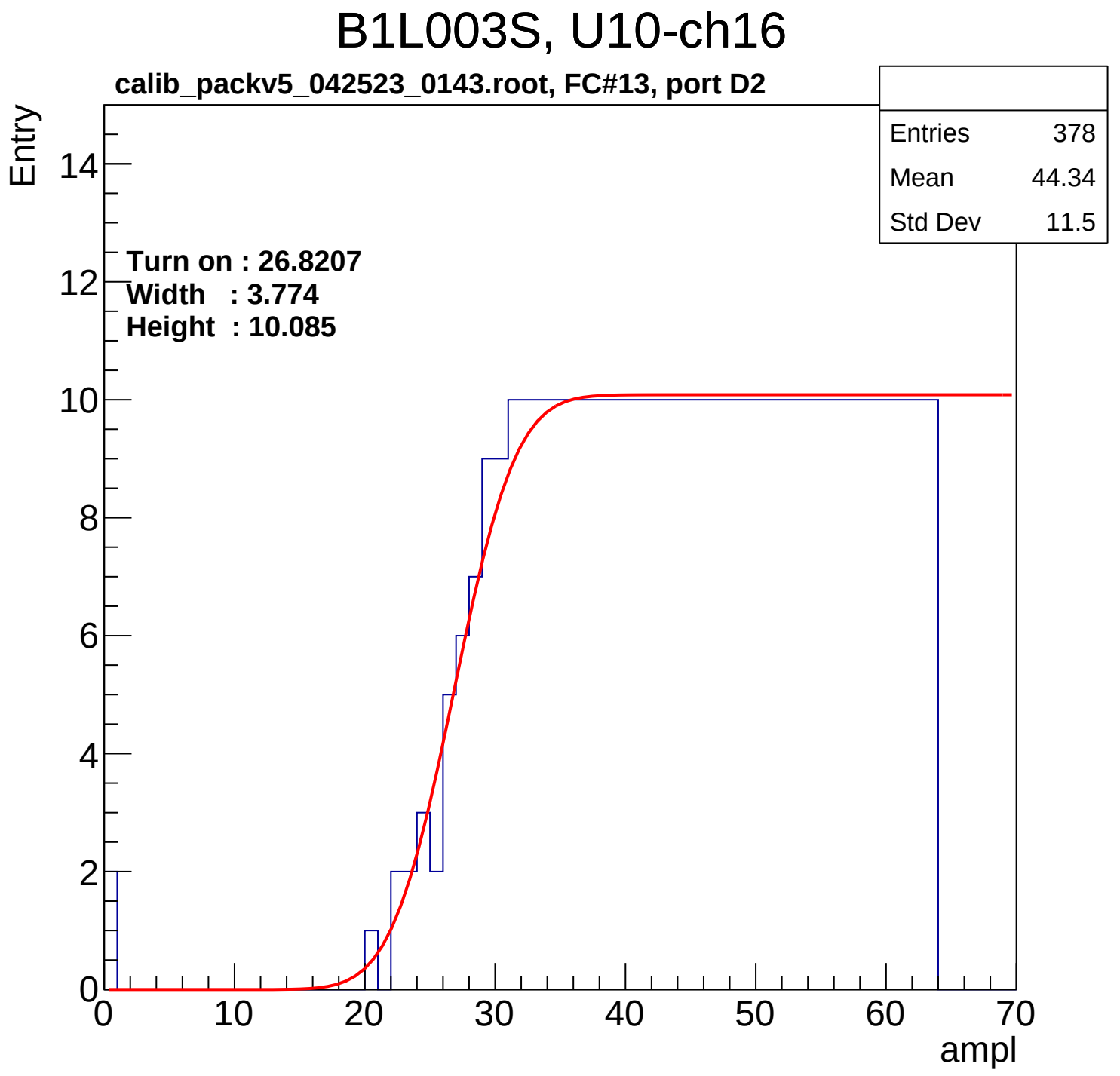

B1L003S, U10-ch11
calib_packv5_042523_0143.root, FC#13, port D2
Entries 364
Mean 44.99
Std Dev 11.3
Turn on : 28.1132
Width : 3.173
Height : 10.061
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

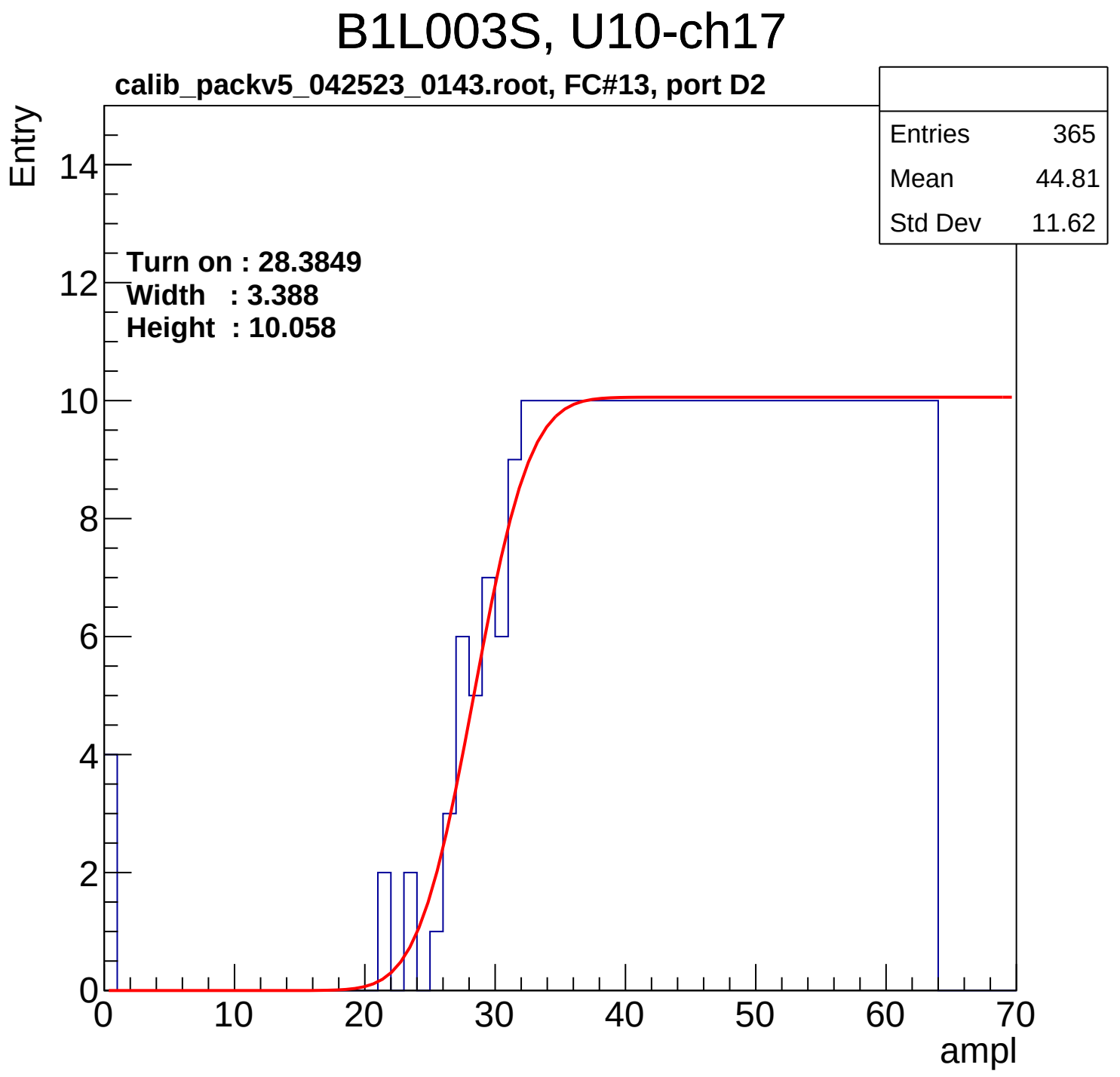

B1L003S, U10-ch12
calib_packv5_042523_0143.root, FC#13, port D2
Entries 383
Mean 44.14
Std Dev 11.55
Turn on : 25.9284
Width : 2.549
Height : 9.997
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

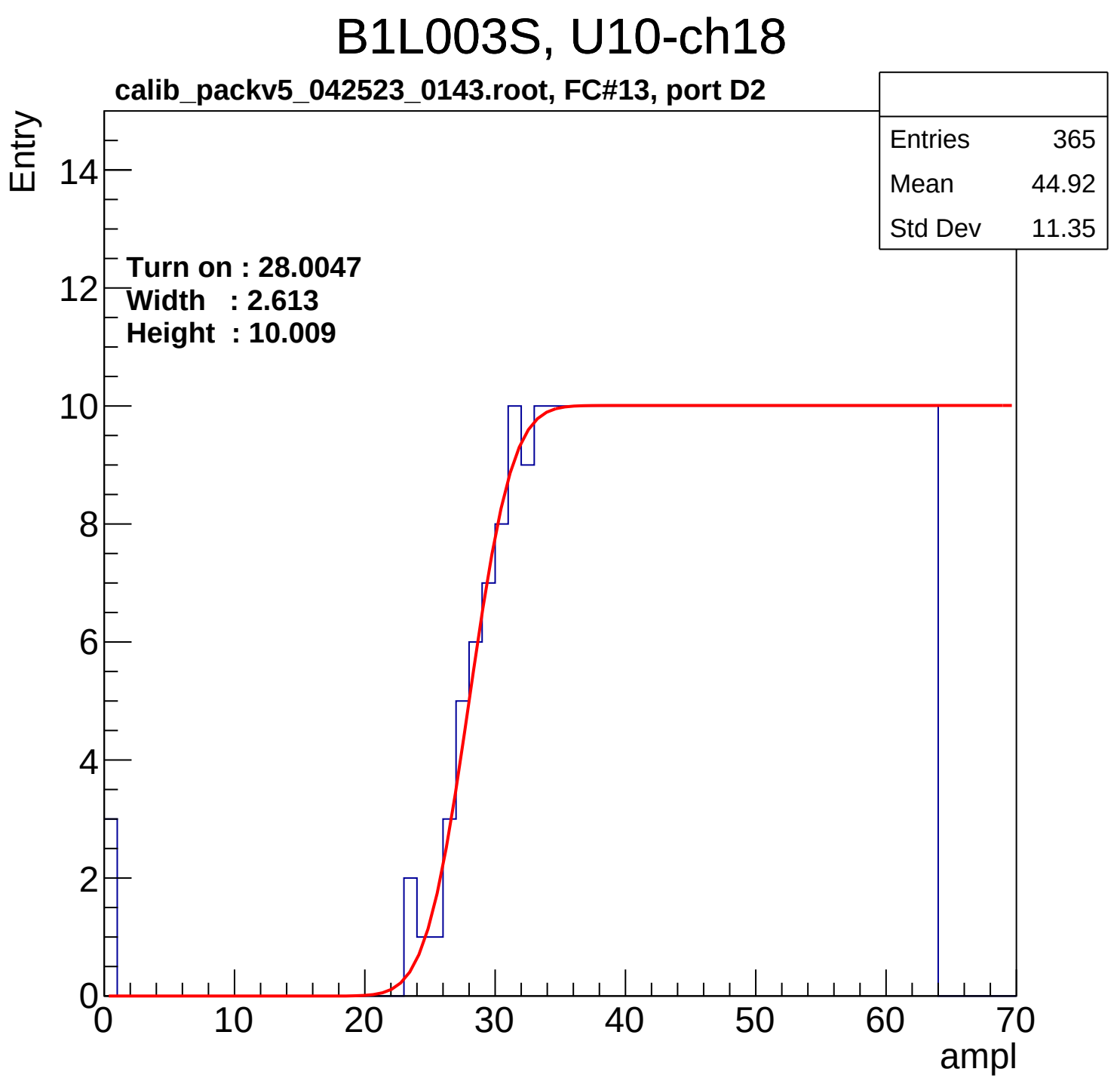

B1L003S, U10-ch13
calib_packv5_042523_0143.root, FC#13, port D2
Entries 373
Mean 44.58
Std Dev 11.38
Turn on : 27.2358
Width : 3.666
Height : 10.055
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

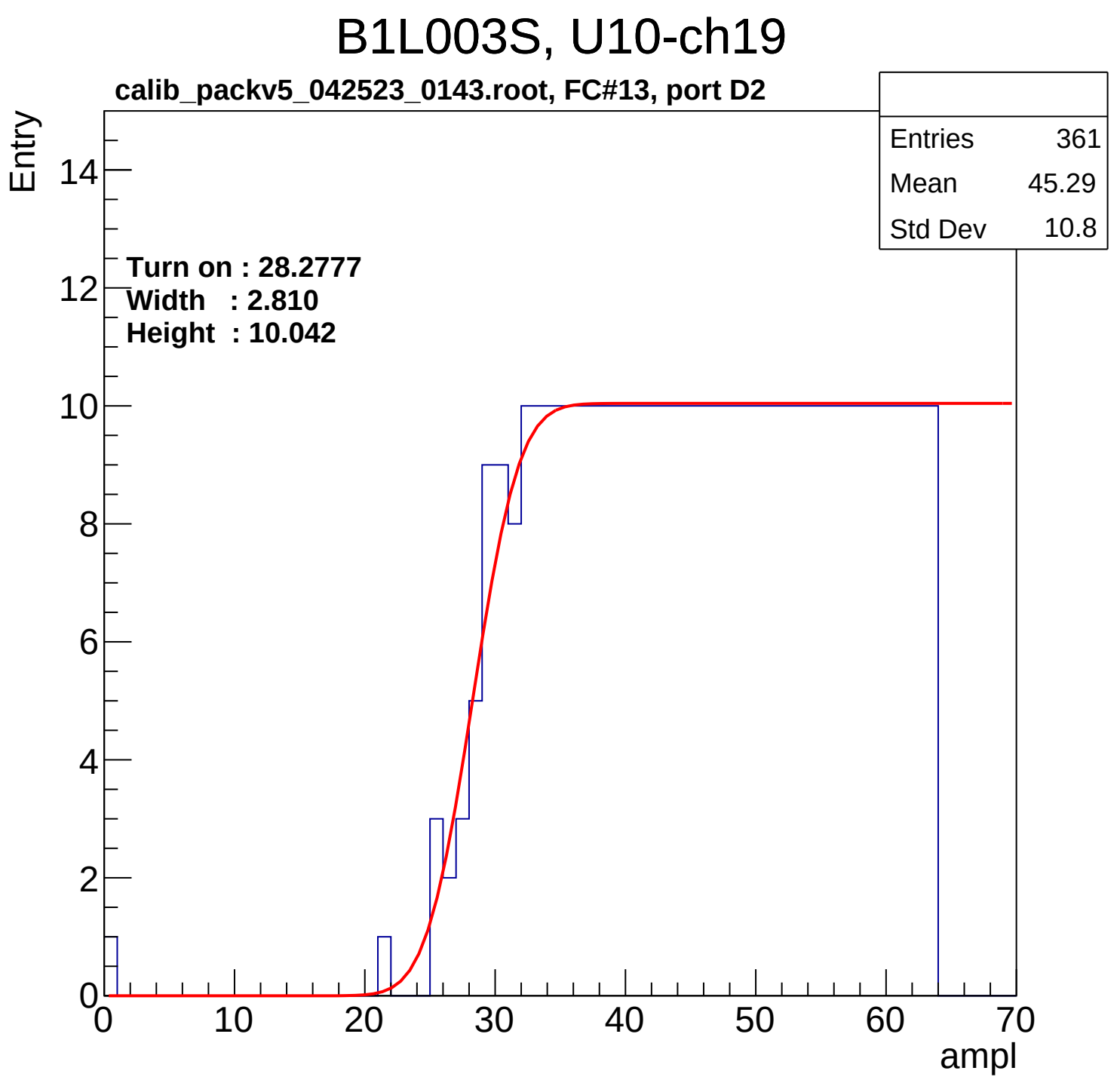

B1L003S, U10-ch14
calib_packv5_042523_0143.root, FC#13, port D2
Entries 369
Mean 44.78
Std Dev 11.27
Turn on : 27.8921
Width : 2.849
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

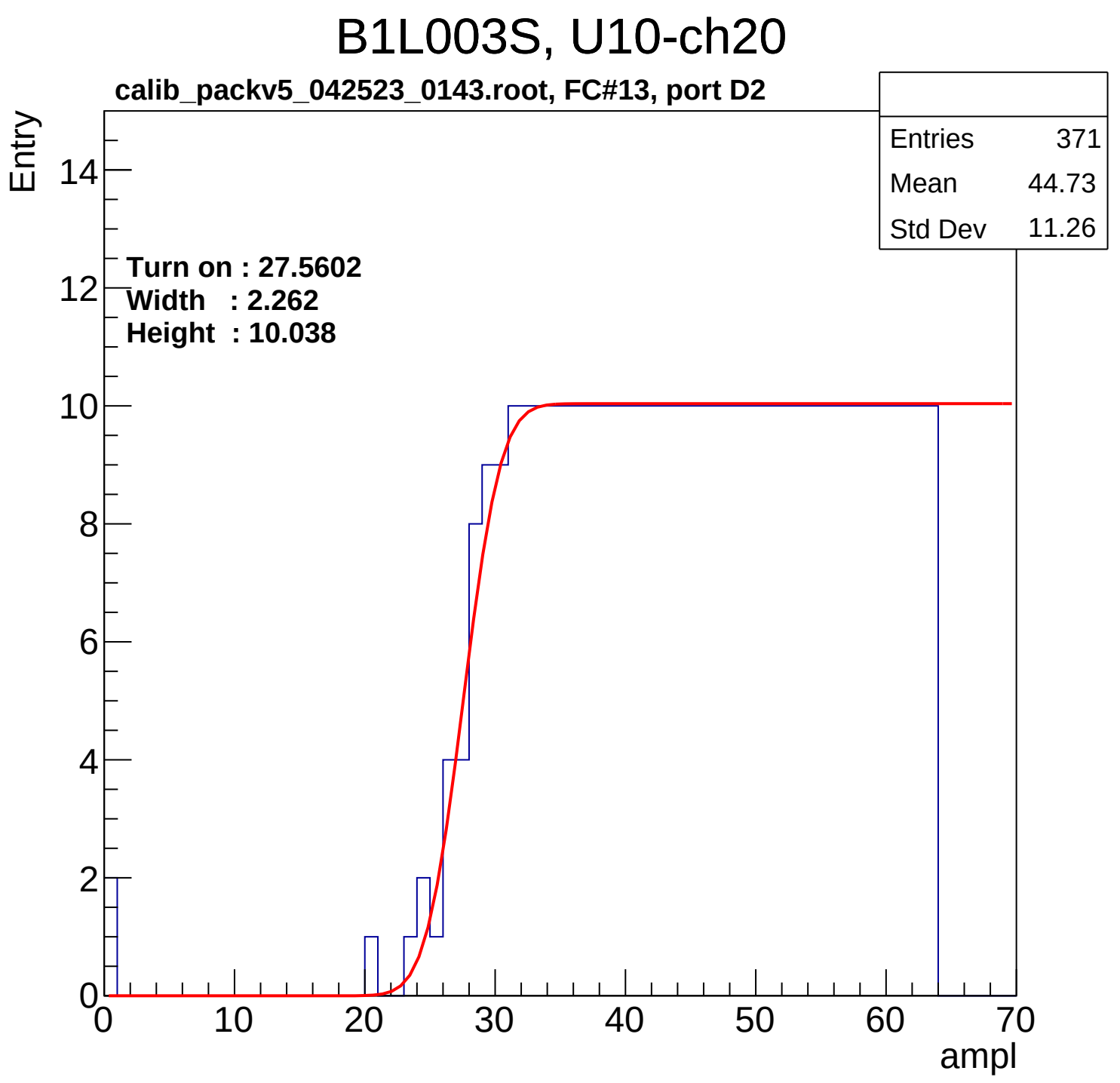

B1L003S, U10-ch15
calib_packv5_042523_0143.root, FC#13, port D2
Entries 359
Mean 45.4
Std Dev 10.72
Turn on : 28.3850
Width : 2.781
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

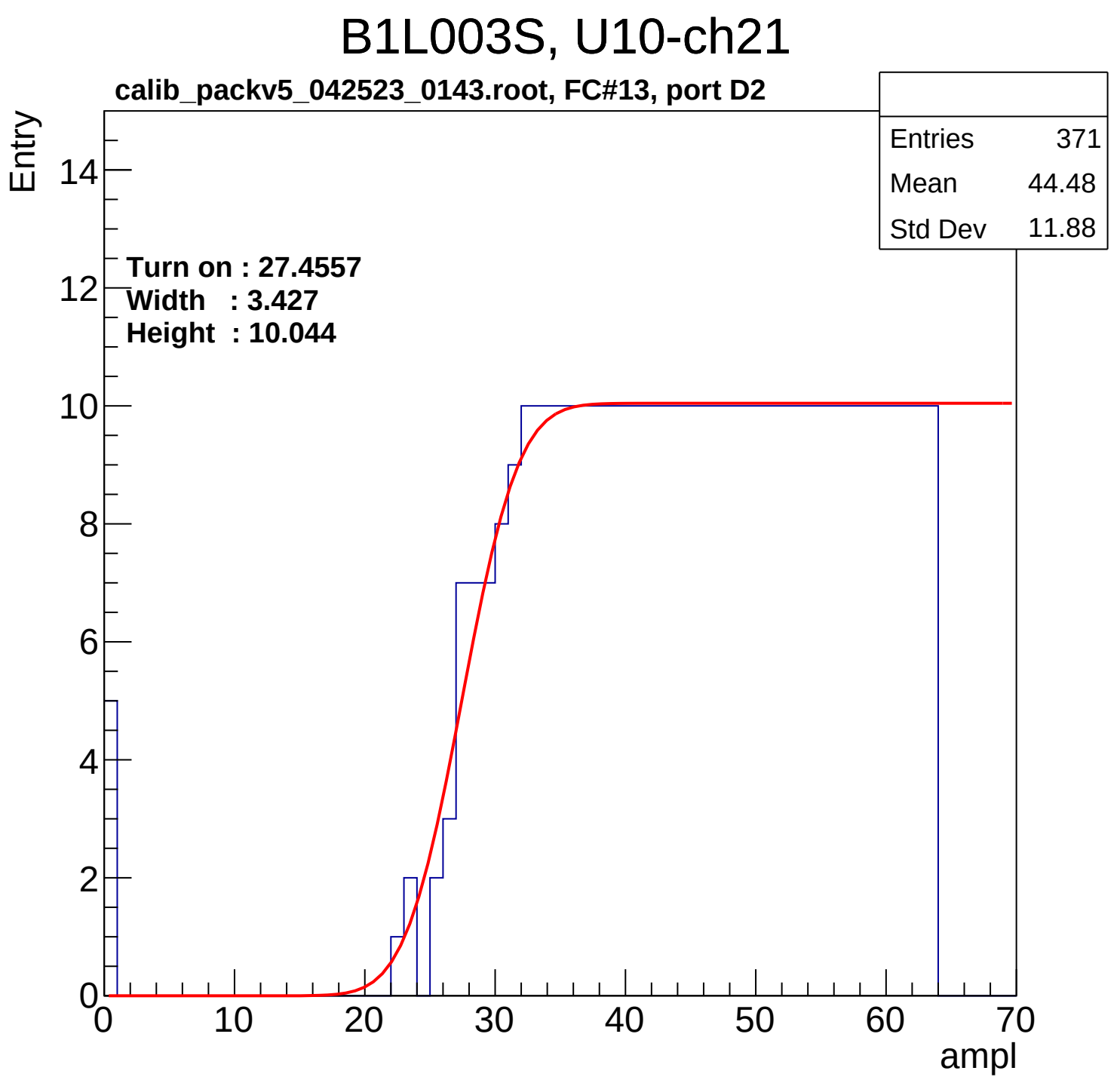

B1L003S, U10-ch16
calib_packv5_042523_0143.root, FC#13, port D2
Entries 378
Mean 44.34
Std Dev 11.5
Turn on : 26.8207
Width : 3.774
Height : 10.085
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

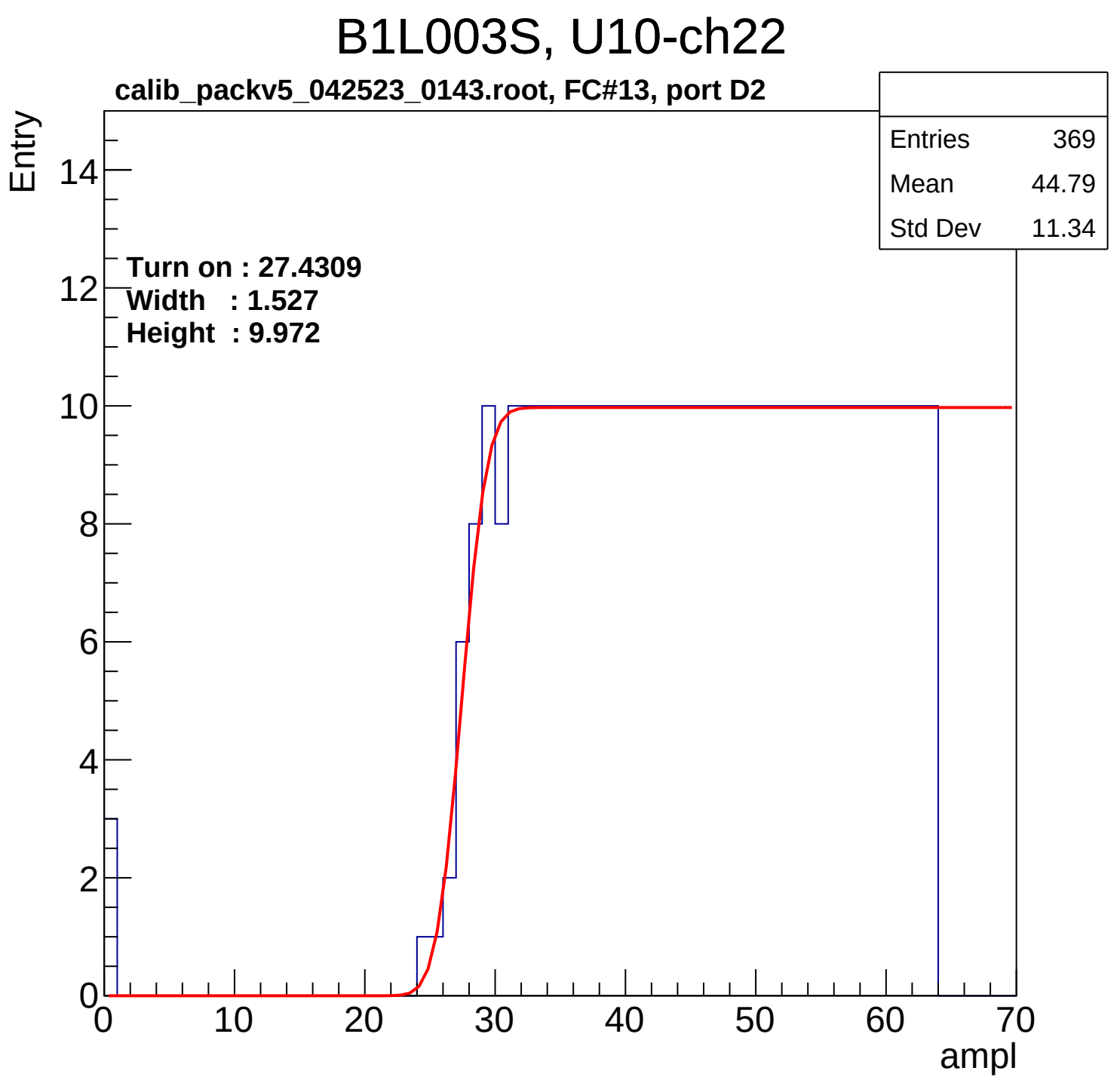

B1L003S, U10-ch17
calib_packv5_042523_0143.root, FC#13, port D2
Entries 365
Mean 44.81
Std Dev 11.62
Turn on : 28.3849
Width : 3.388
Height : 10.058
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

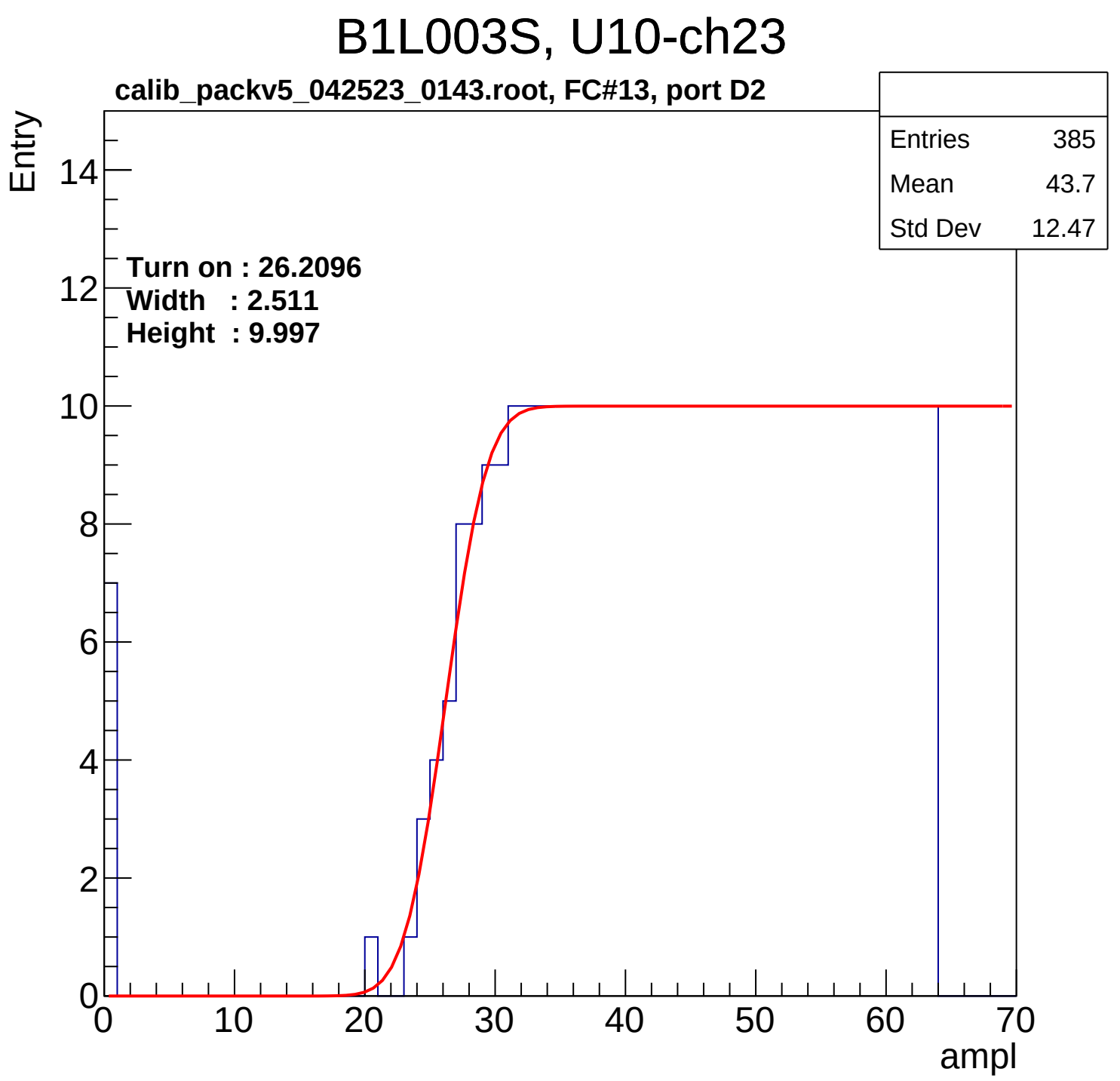

B1L003S, U10-ch18
calib_packv5_042523_0143.root, FC#13, port D2
Entries 365
Mean 44.92
Std Dev 11.35
Turn on : 28.0047
Width : 2.613
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

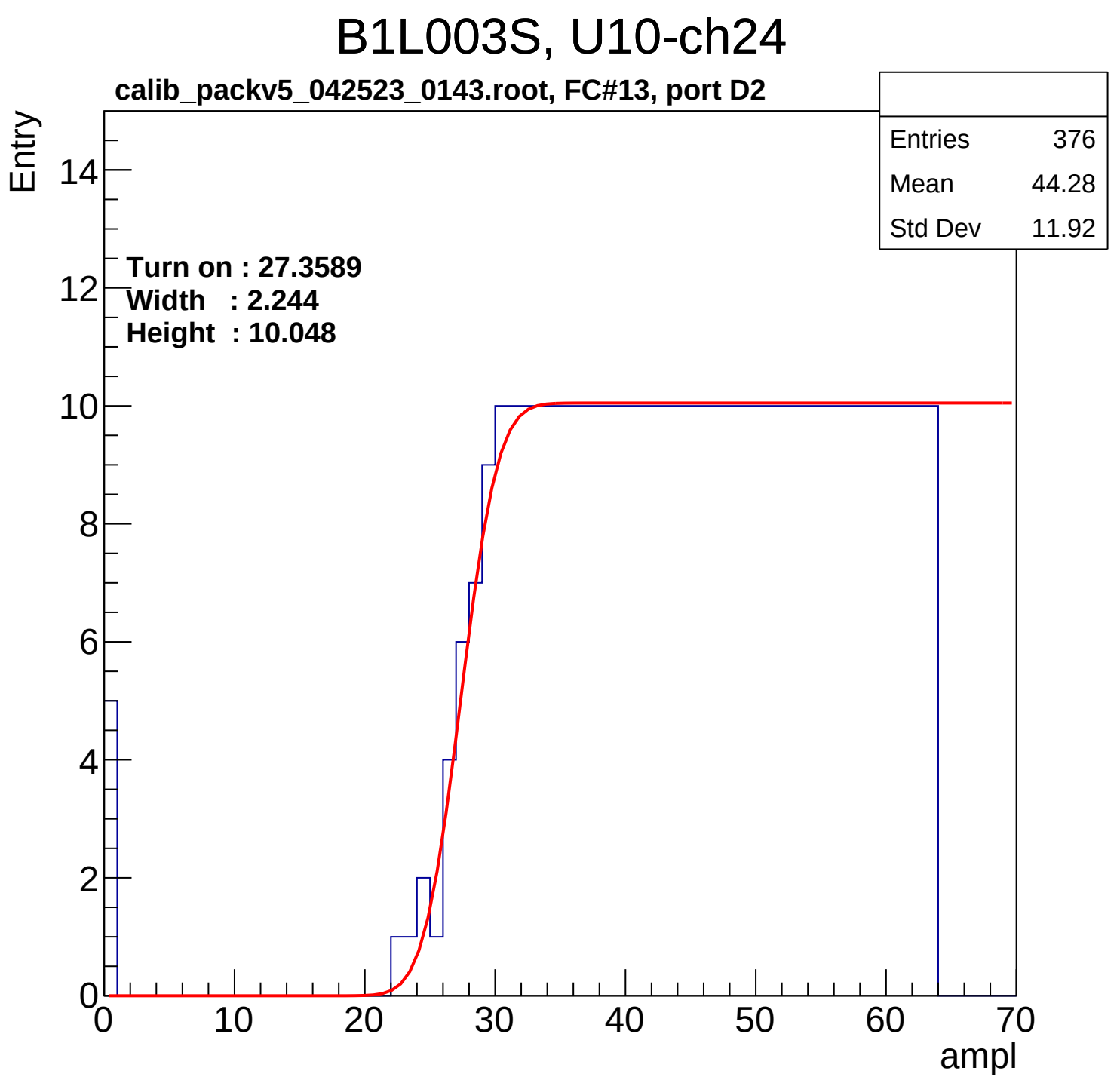

B1L003S, U10-ch19
calib_packv5_042523_0143.root, FC#13, port D2
Entries 361
Mean 45.29
Std Dev 10.8
Turn on : 28.2777
Width : 2.810
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

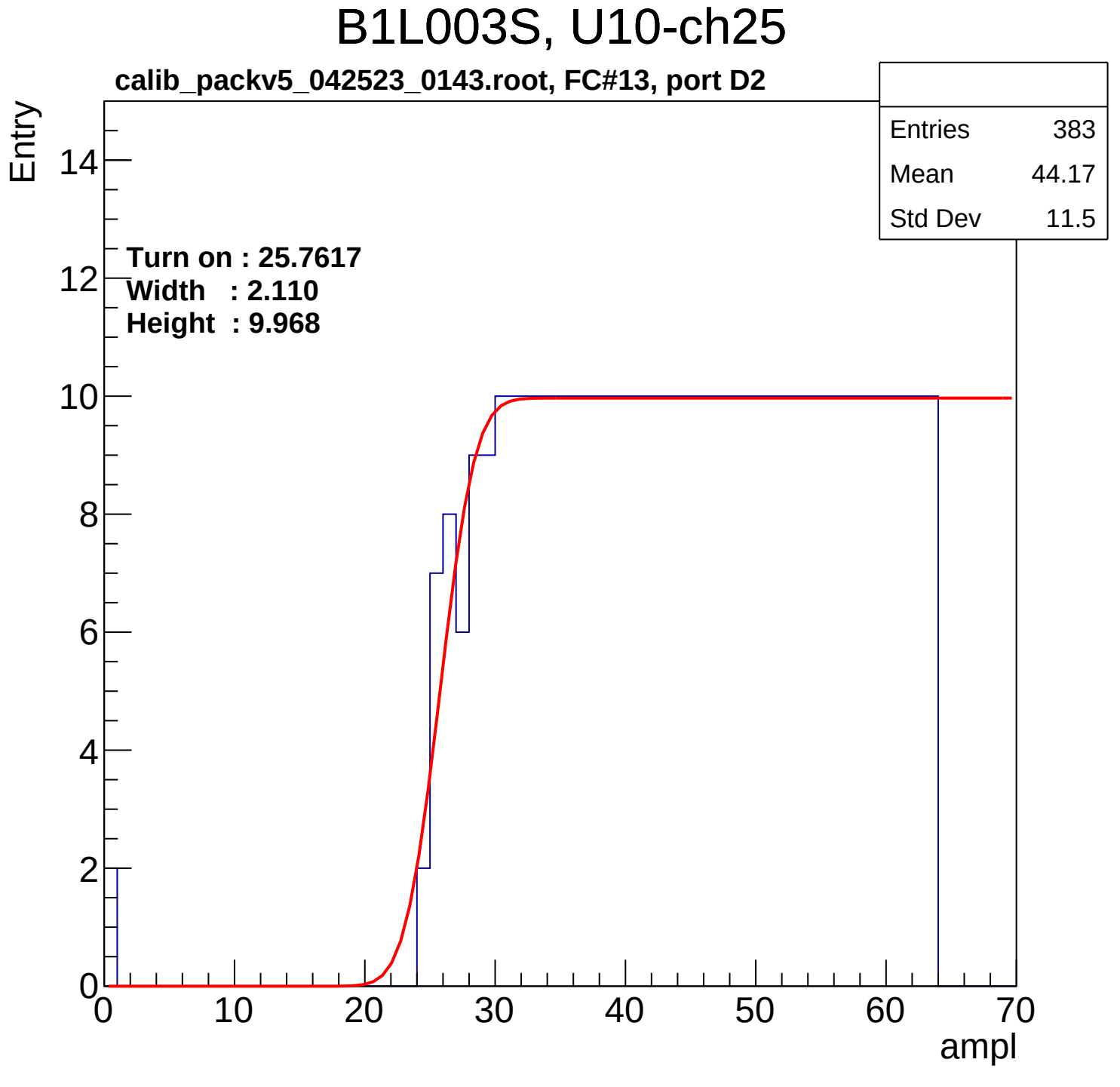

B1L003S, U10-ch20
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.73
Std Dev 11.26
Turn on : 27.5602
Width : 2.262
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

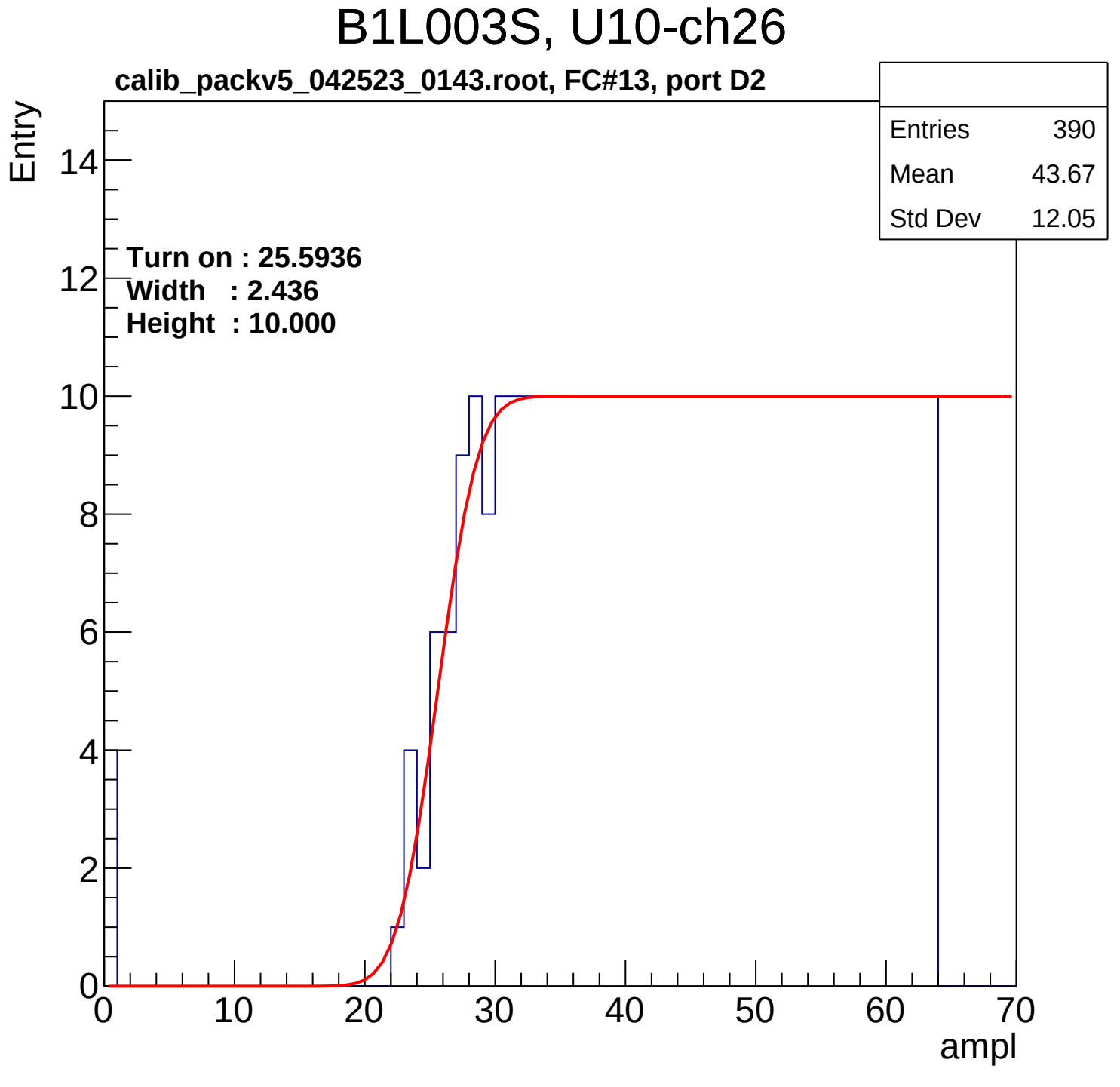

B1L003S, U10-ch21
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.48
Std Dev 11.88
Turn on : 27.4557
Width : 3.427
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

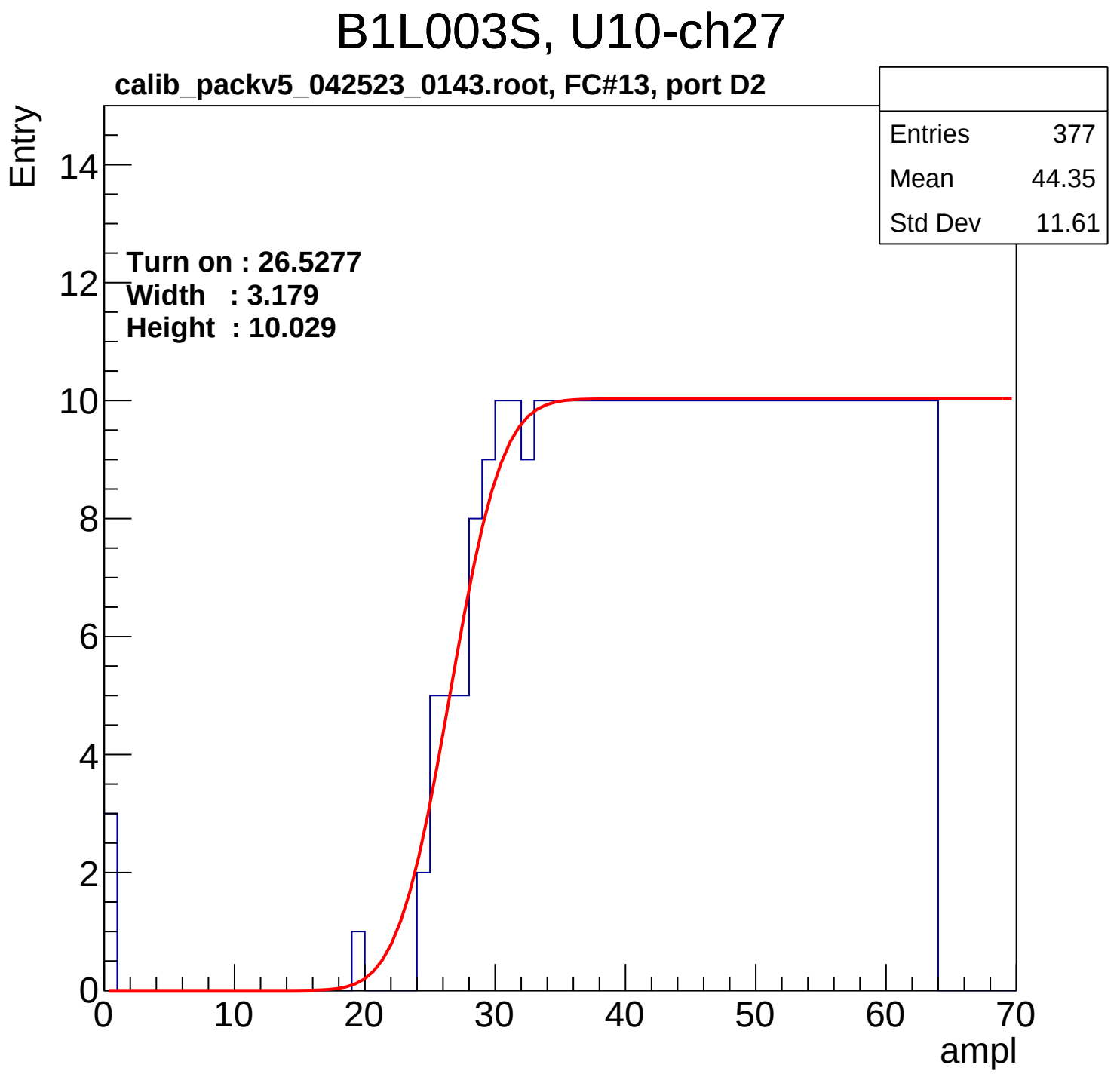

B1L003S, U10-ch22
calib_packv5_042523_0143.root, FC#13, port D2
Entries 369
Mean 44.79
Std Dev 11.34
Turn on : 27.4309
Width : 1.527
Height : 9.972
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

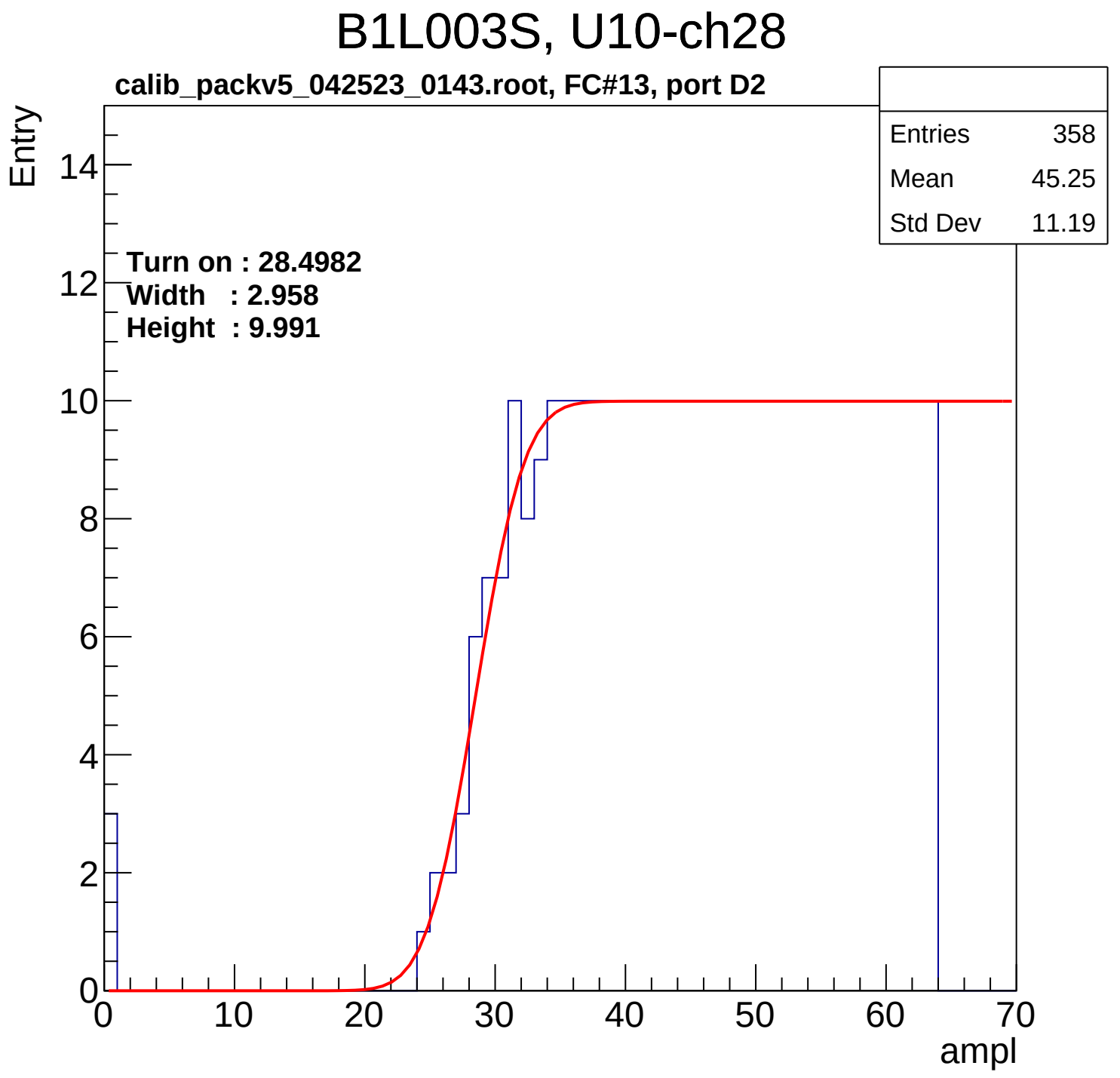

B1L003S, U10-ch23
calib_packv5_042523_0143.root, FC#13, port D2
Entries 385
Mean 43.7
Std Dev 12.47
Turn on : 26.2096
Width : 2.511
Height : 9.997
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

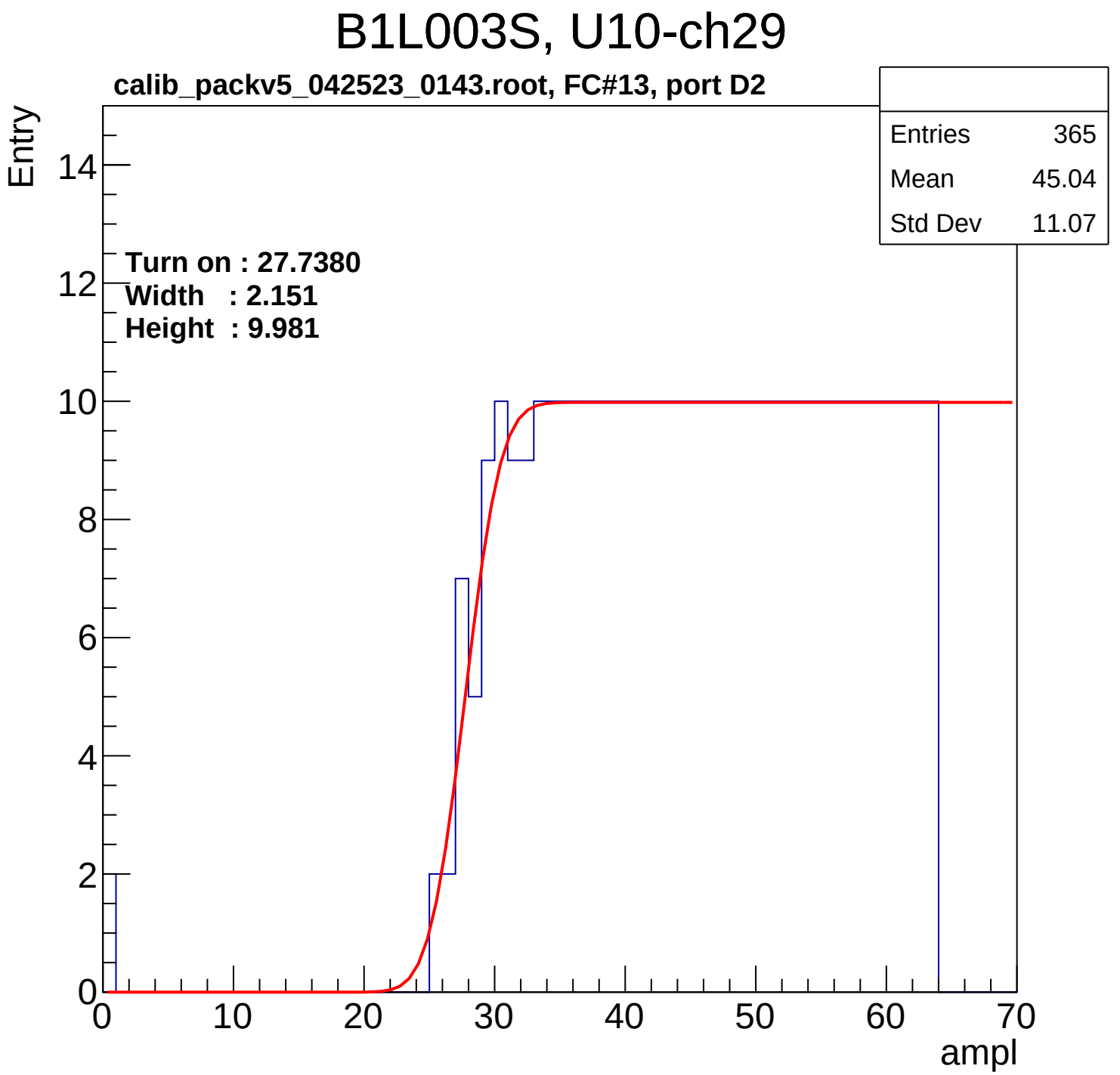

B1L003S, U10-ch24
calib_packv5_042523_0143.root, FC#13, port D2
Entries 376
Mean 44.28
Std Dev 11.92
Turn on : 27.3589
Width : 2.244
Height : 10.048
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

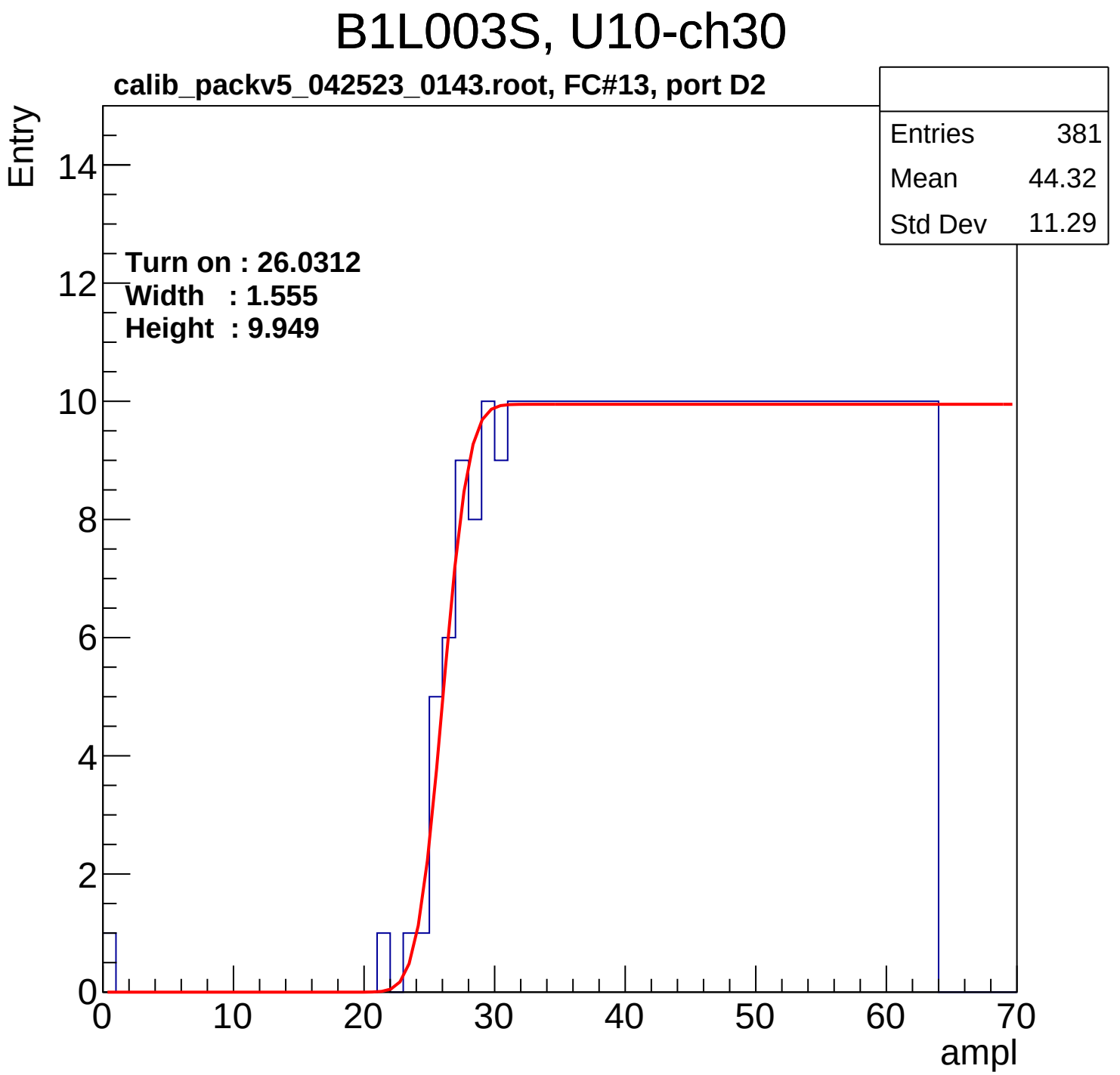

B1L003S, U10-ch25
calib_packv5_042523_0143.root, FC#13, port D2
Entries 383
Mean 44.17
Std Dev 11.5
Turn on : 25.7617
Width : 2.110
Height : 9.968
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

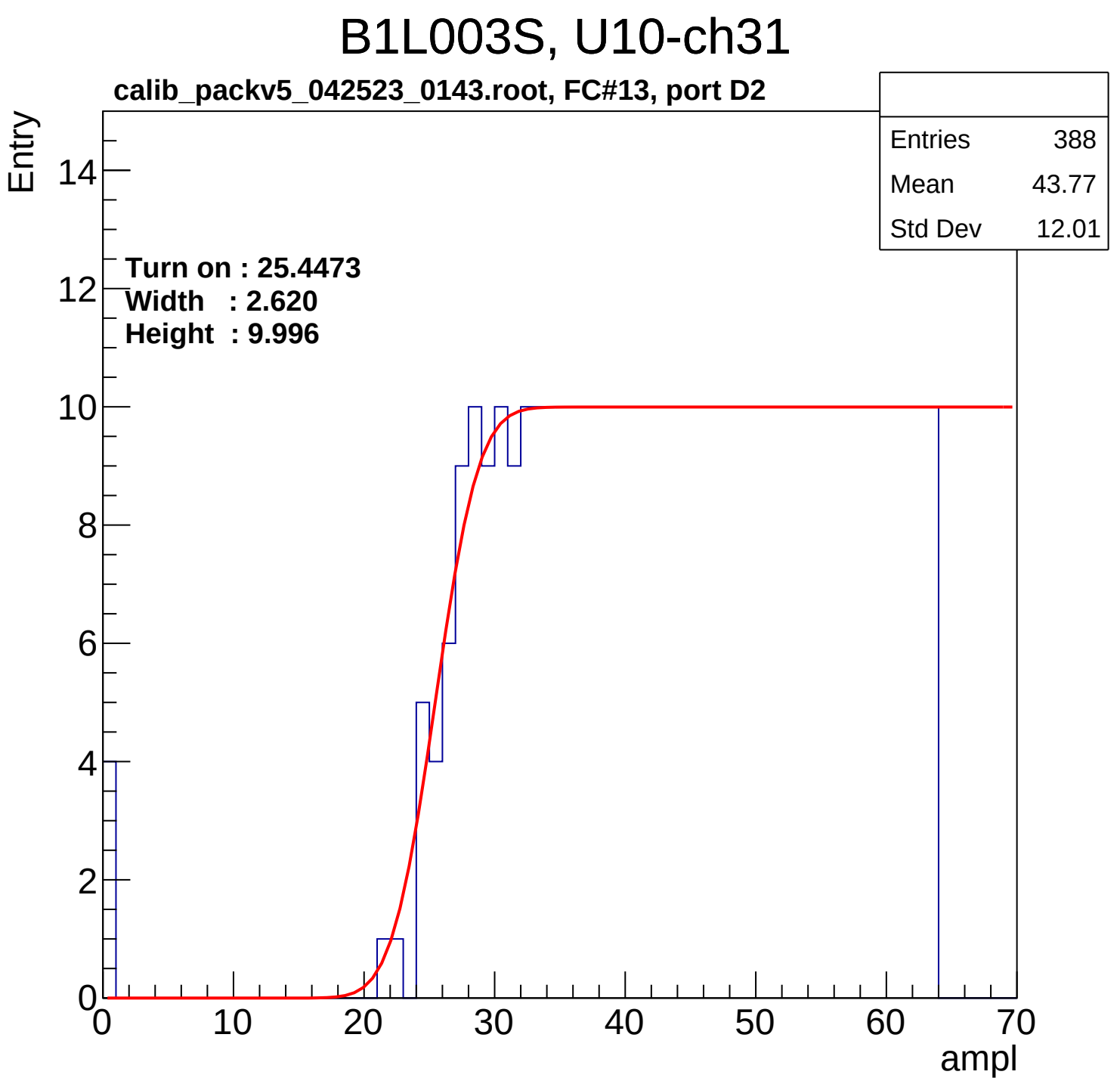

B1L003S, U10-ch26
calib_packv5_042523_0143.root, FC#13, port D2
Entries 390
Mean 43.67
Std Dev 12.05
Turn on : 25.5936
Width : 2.436
Height : 10.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

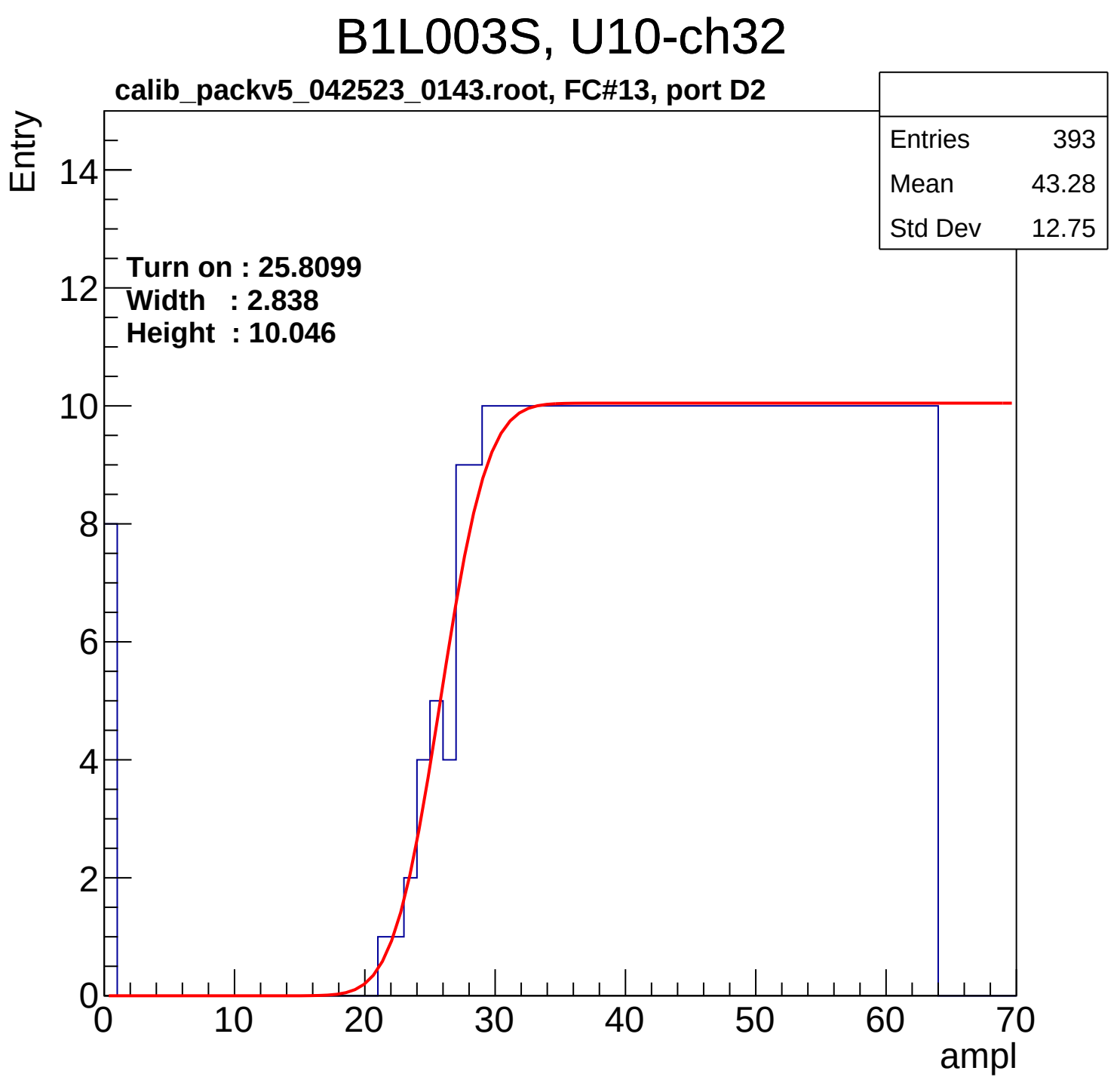

B1L003S, U10-ch27
calib_packv5_042523_0143.root, FC#13, port D2
Entries 377
Mean 44.35
Std Dev 11.61
Turn on : 26.5277
Width : 3.179
Height : 10.029
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

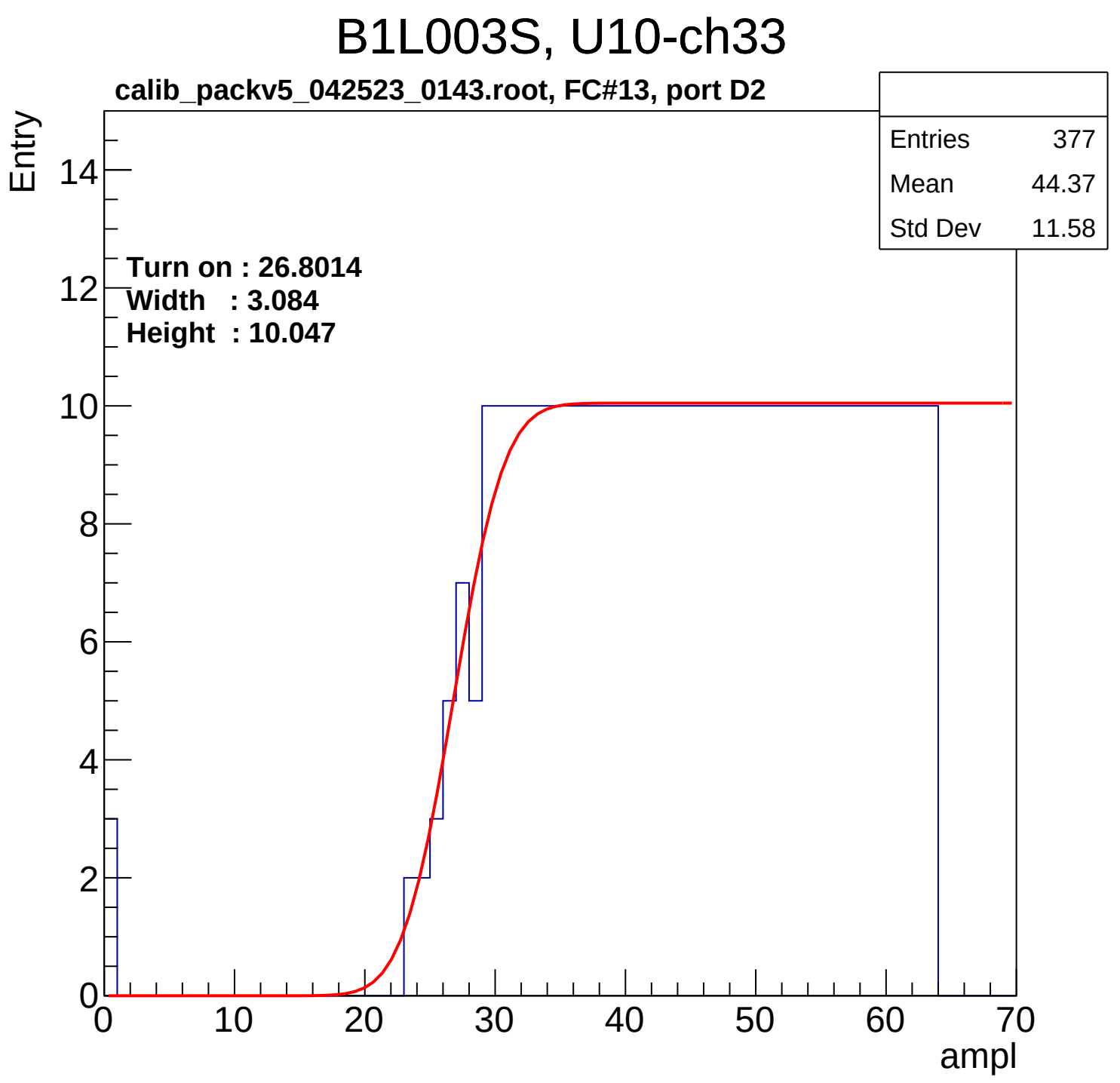

B1L003S, U10-ch28
calib_packv5_042523_0143.root, FC#13, port D2
Entries 358
Mean 45.25
Std Dev 11.19
Turn on : 28.4982
Width : 2.958
Height : 9.991
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

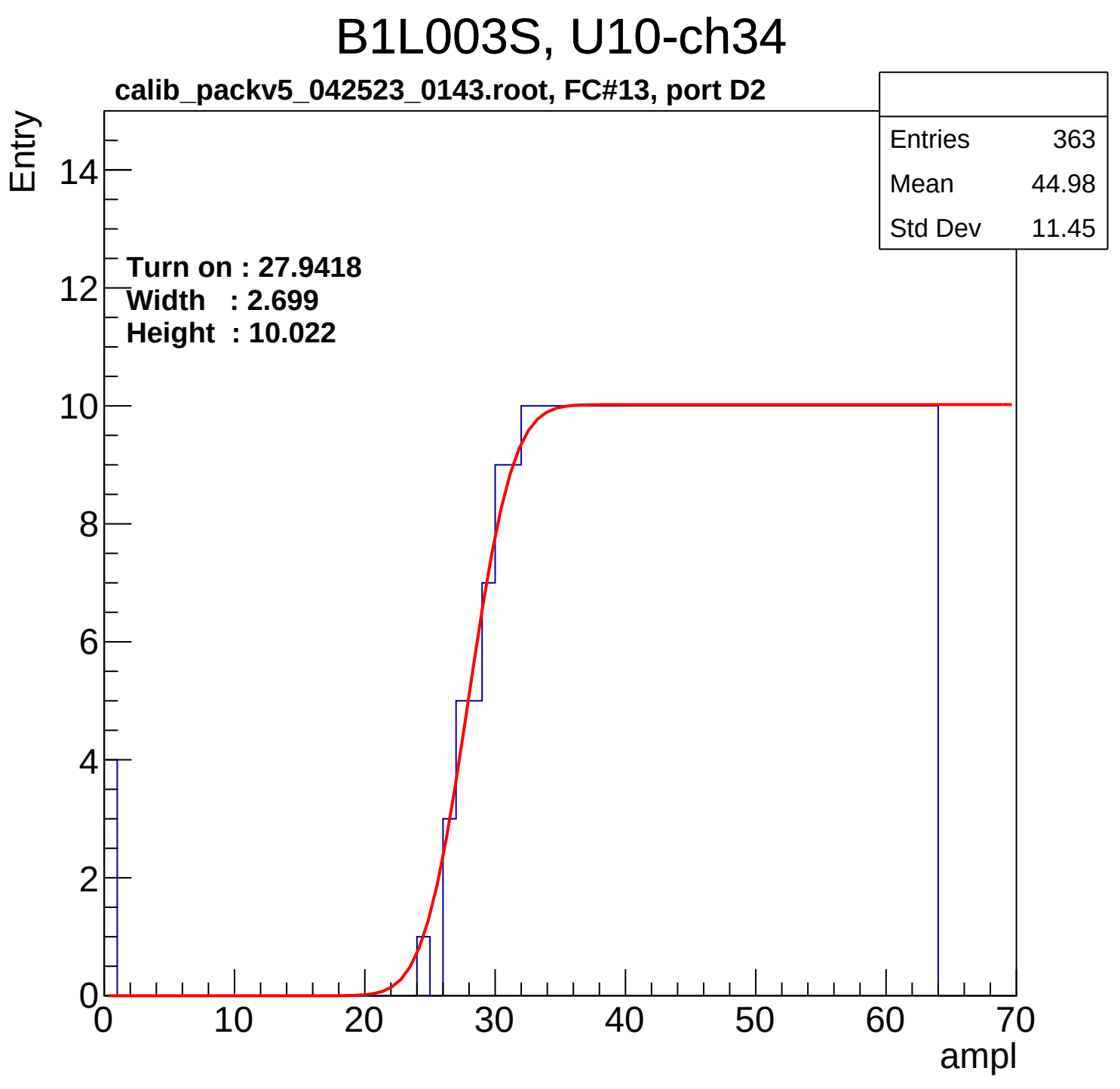

B1L003S, U10-ch29
calib_packv5_042523_0143.root, FC#13, port D2
Entries 365
Mean 45.04
Std Dev 11.07
Turn on : 27.7380
Width : 2.151
Height : 9.981
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

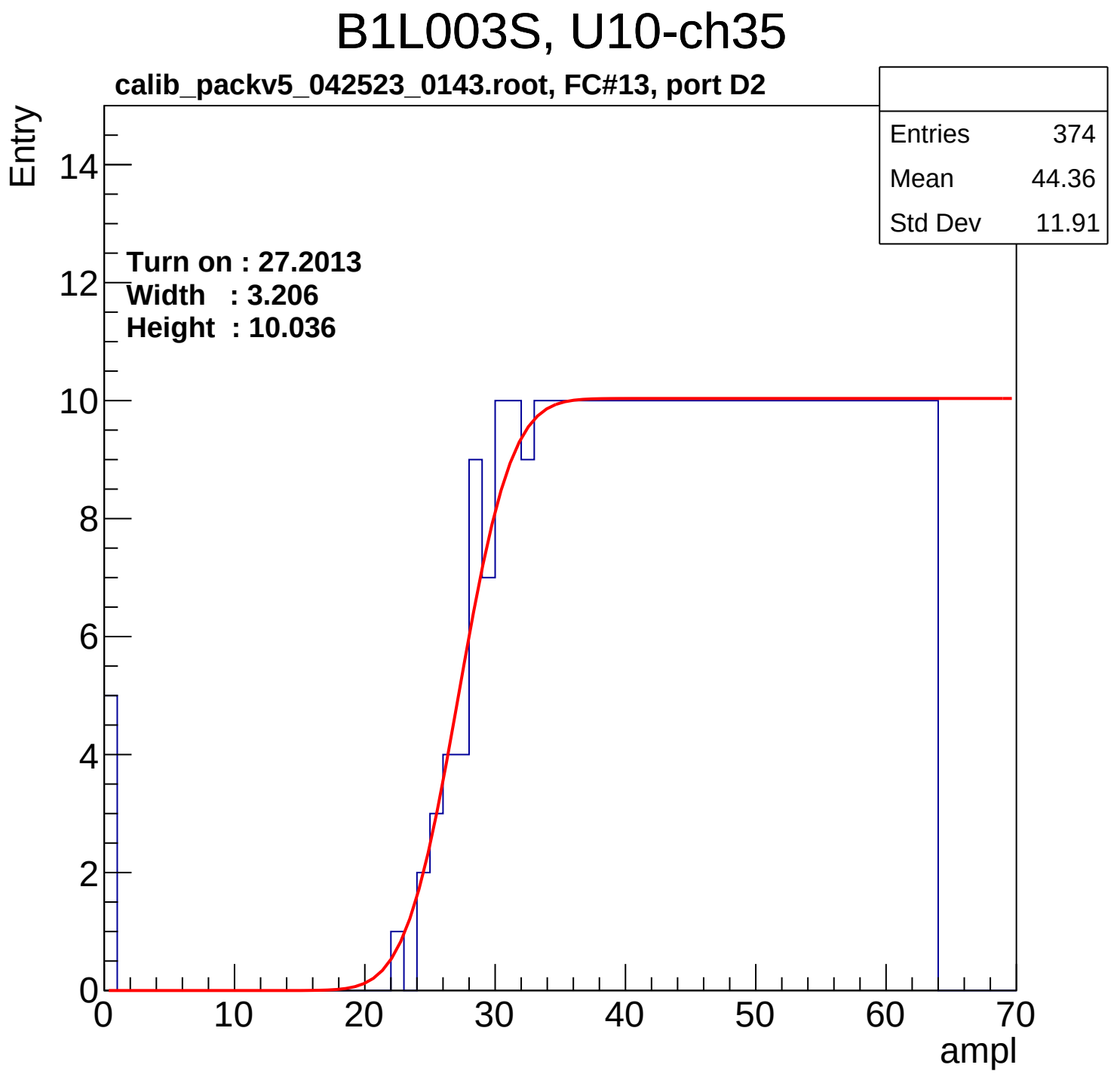

B1L003S, U10-ch30
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 44.32
Std Dev 11.29
Turn on : 26.0312
Width : 1.555
Height : 9.949
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

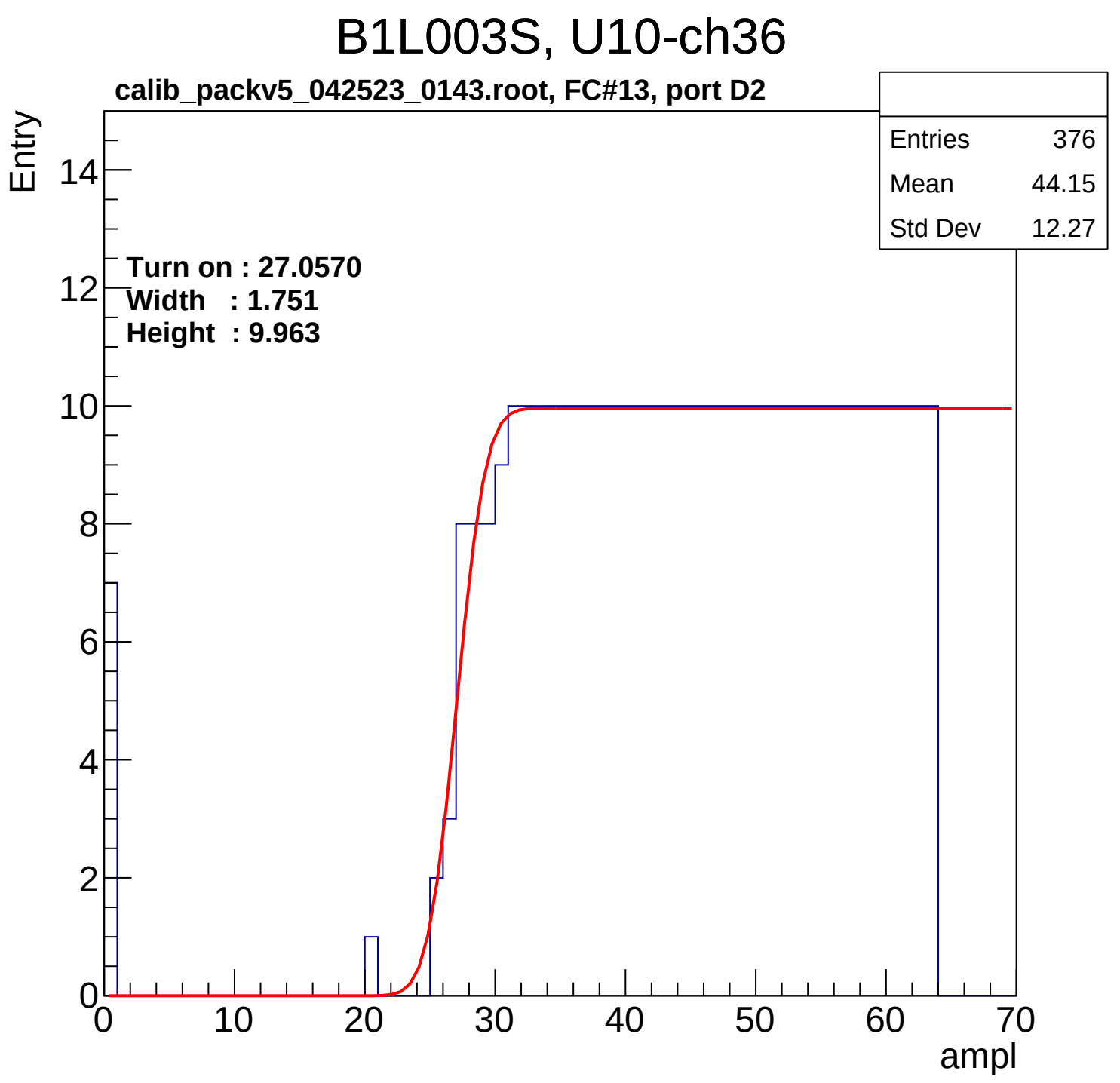

B1L003S, U10-ch31
calib_packv5_042523_0143.root, FC#13, port D2
Entries 388
Mean 43.77
Std Dev 12.01
Turn on : 25.4473
Width : 2.620
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

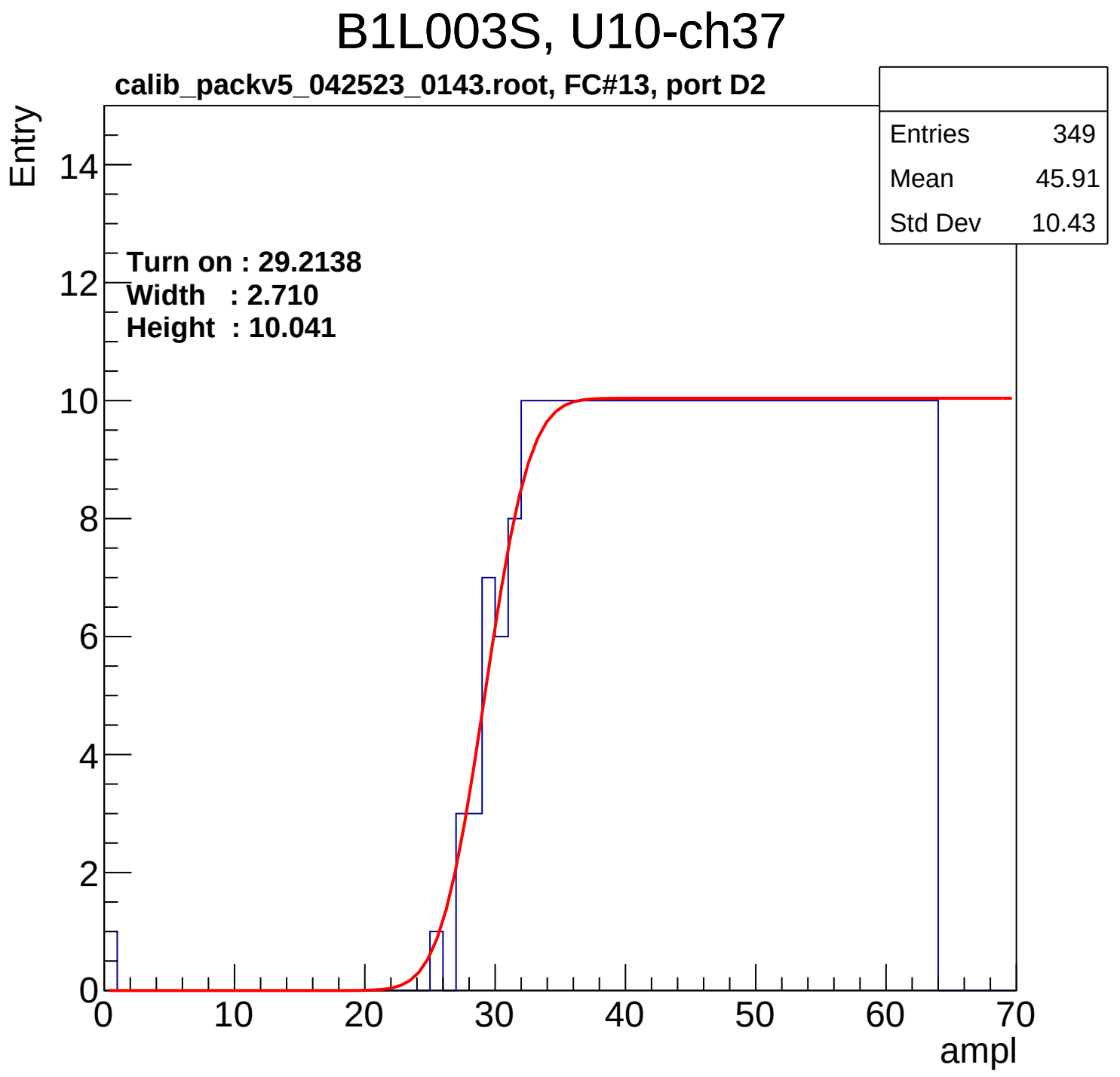

B1L003S, U10-ch32
calib_packv5_042523_0143.root, FC#13, port D2
Entries 393
Mean 43.28
Std Dev 12.75
Turn on : 25.8099
Width : 2.838
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

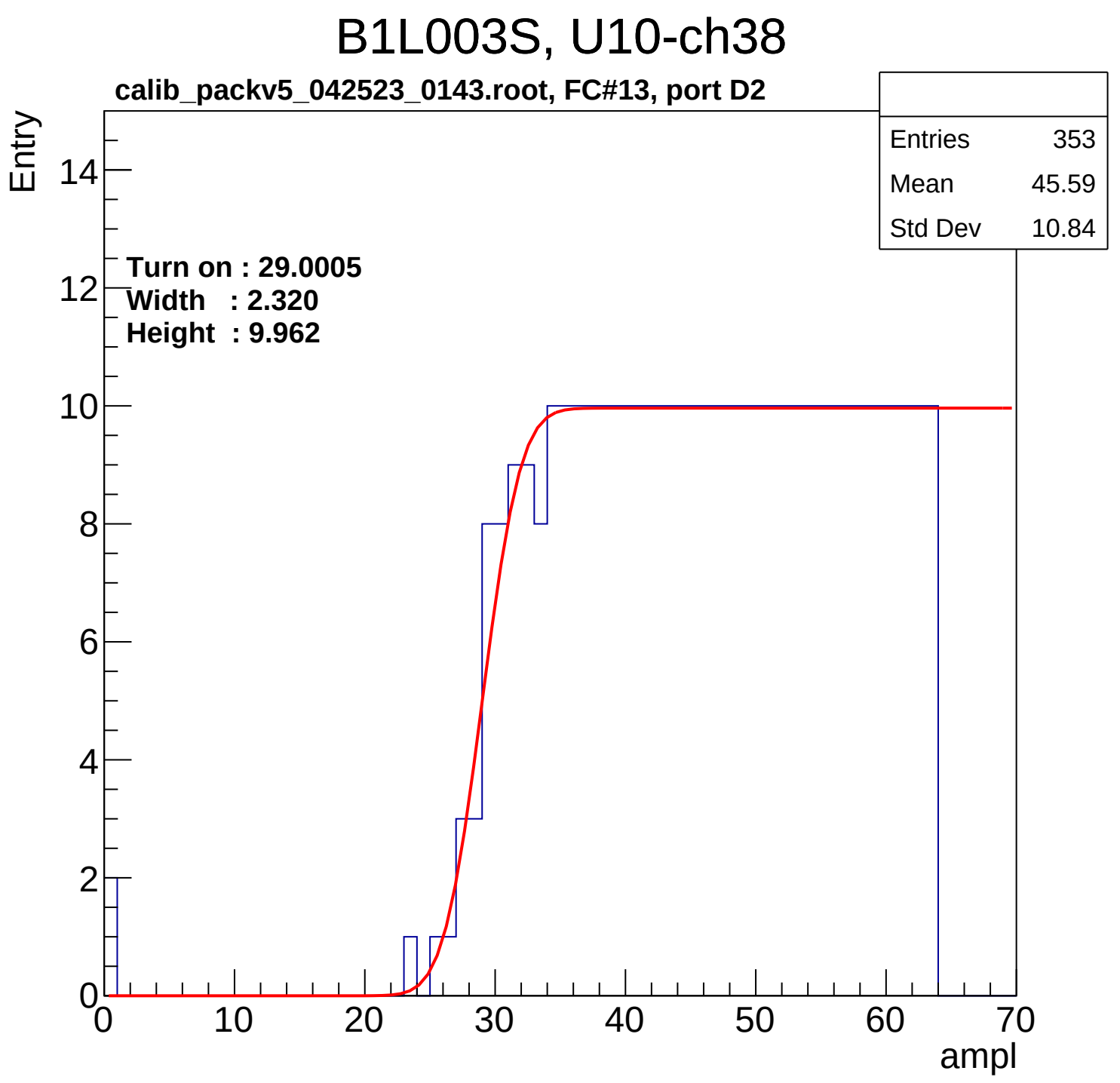

B1L003S, U10-ch33
calib_packv5_042523_0143.root, FC#13, port D2
Entries 377
Mean 44.37
Std Dev 11.58
Turn on : 26.8014
Width : 3.084
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

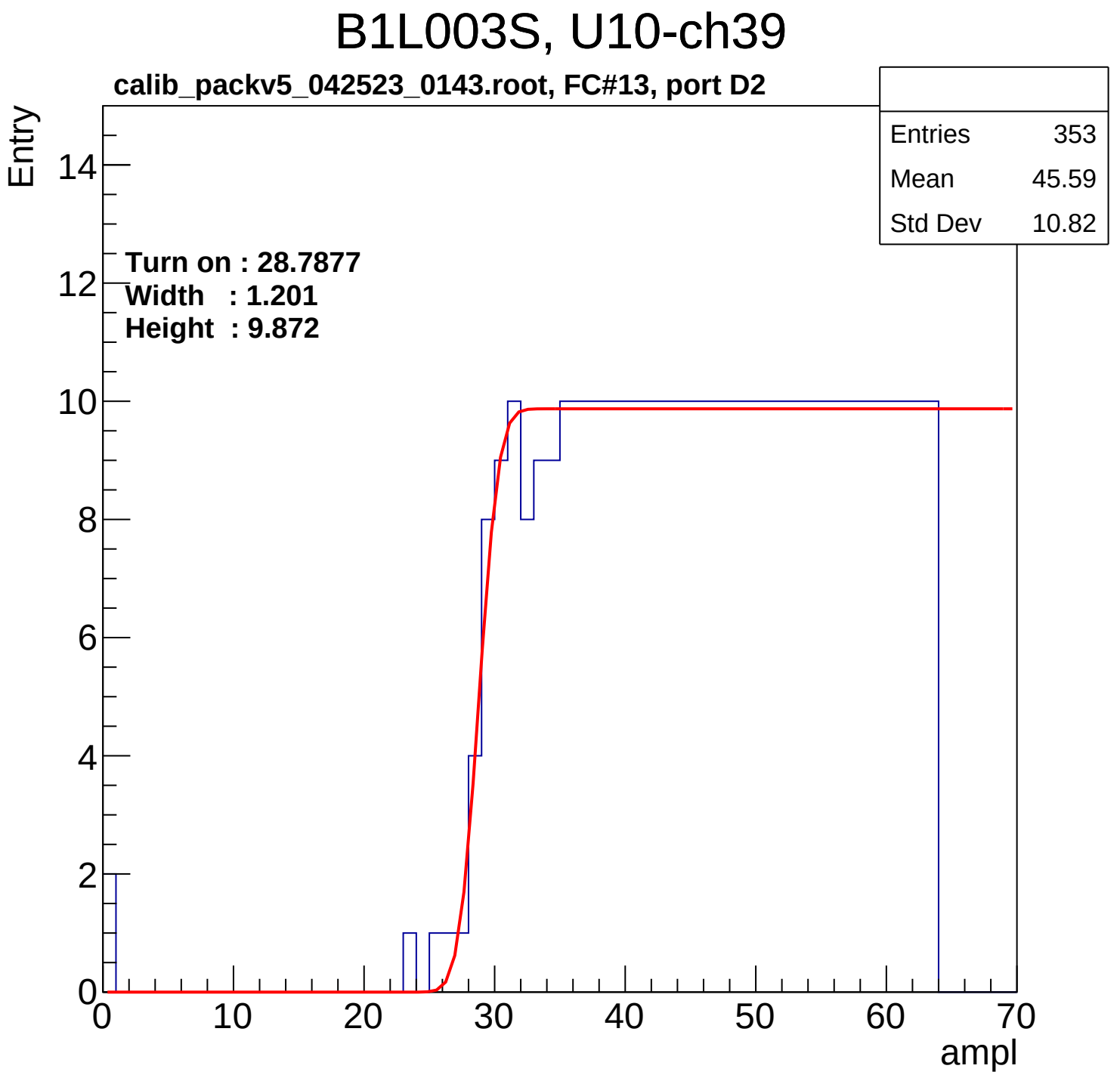

B1L003S, U10-ch34
calib_packv5_042523_0143.root, FC#13, port D2
Entries 363
Mean 44.98
Std Dev 11.45
Turn on : 27.9418
Width : 2.699
Height : 10.022
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

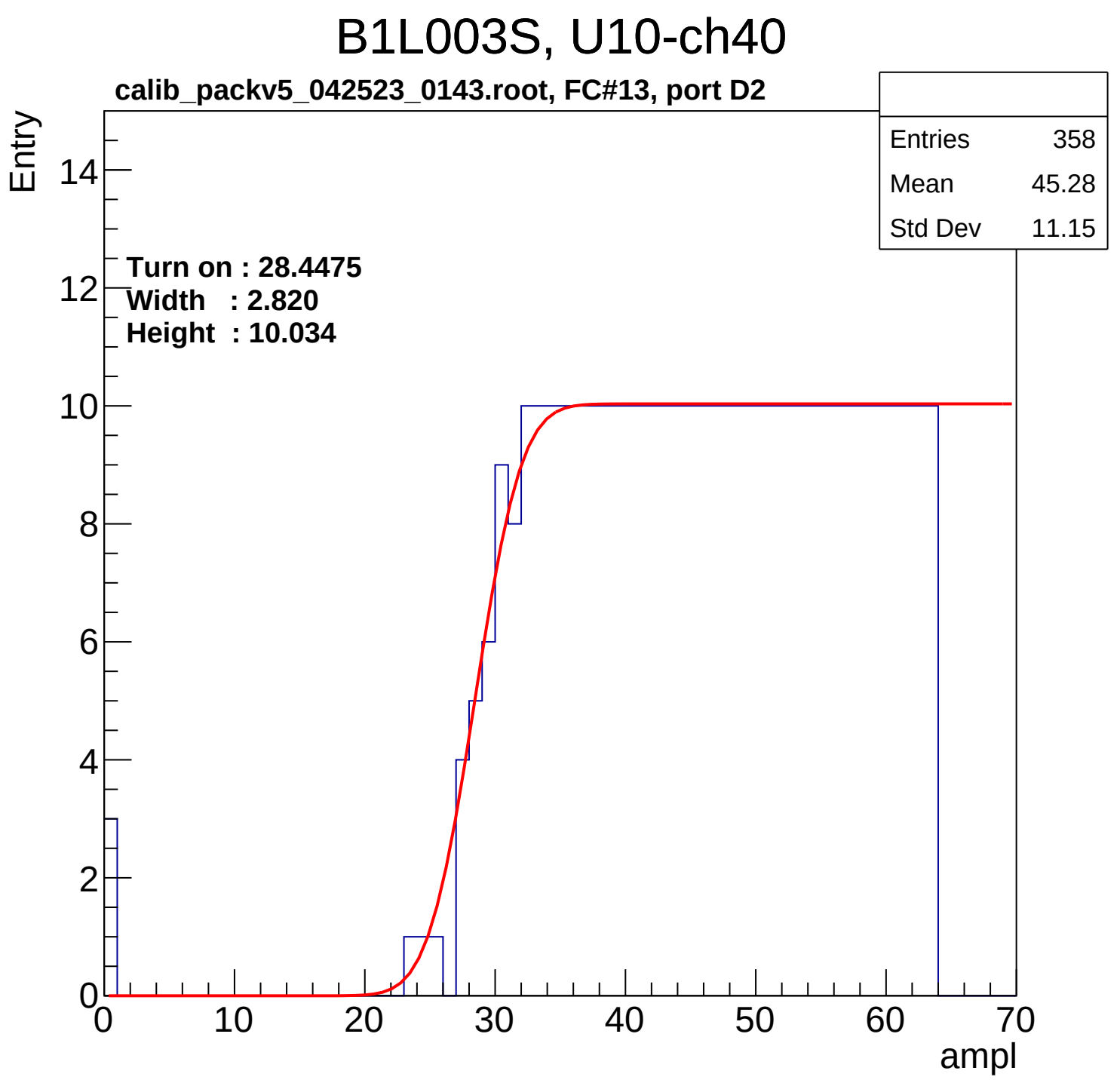

B1L003S, U10-ch35
calib_packv5_042523_0143.root, FC#13, port D2
Entries 374
Mean 44.36
Std Dev 11.91
Turn on : 27.2013
Width : 3.206
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

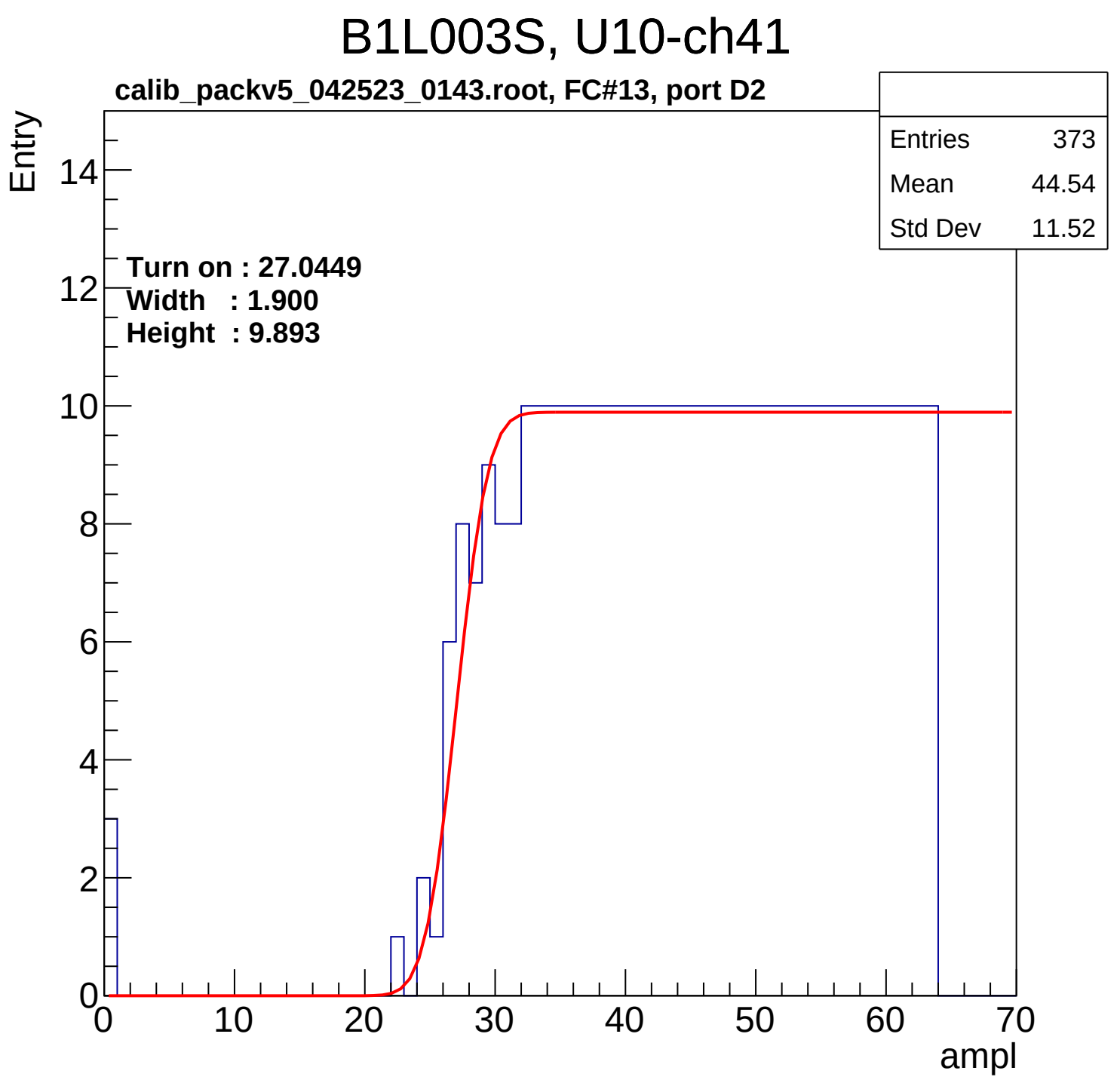

B1L003S, U10-ch36
calib_packv5_042523_0143.root, FC#13, port D2
Entries 376
Mean 44.15
Std Dev 12.27
Turn on : 27.0570
Width : 1.751
Height : 9.963
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

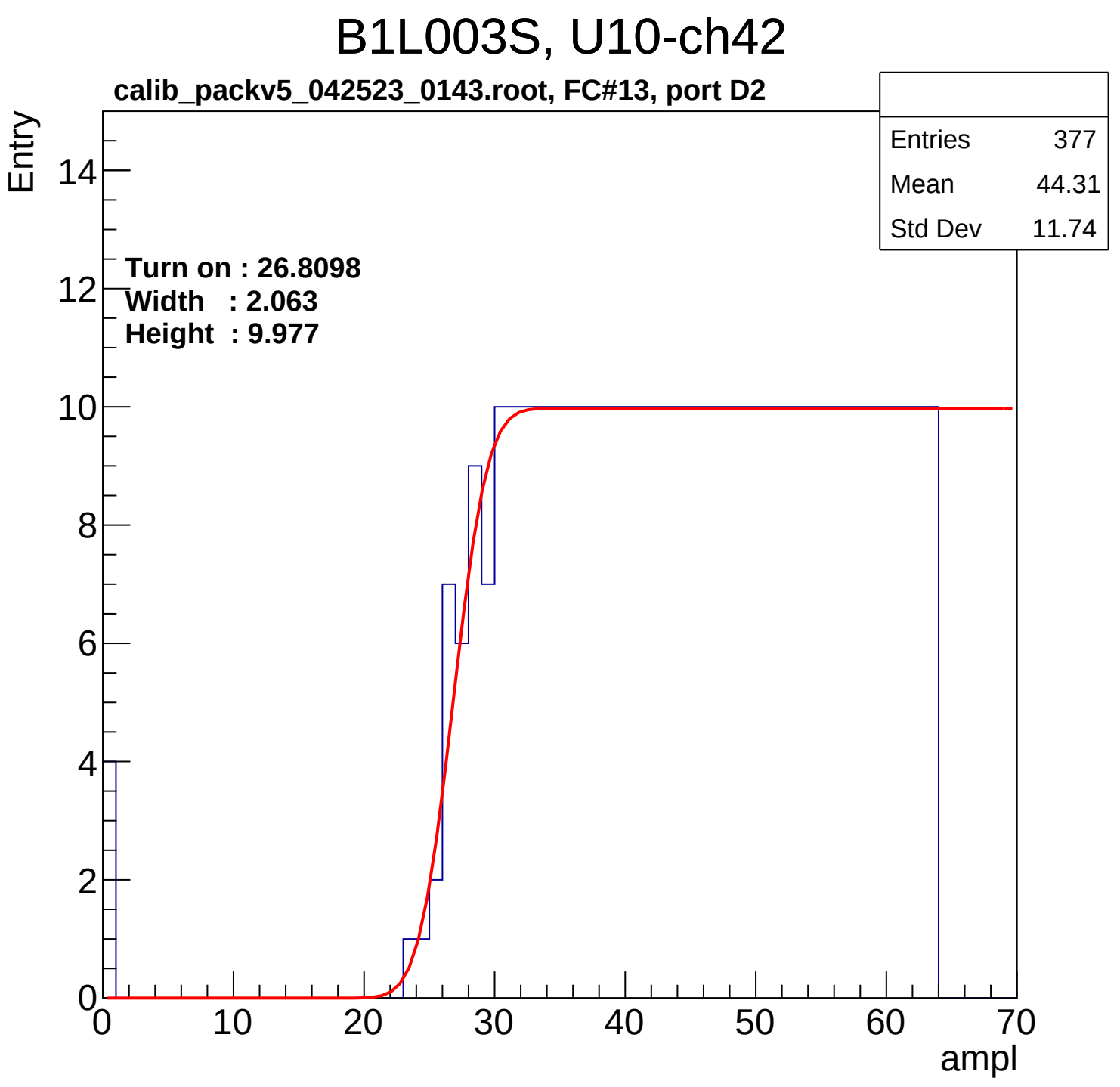

B1L003S, U10-ch37
calib_packv5_042523_0143.root, FC#13, port D2
Entries 349
Mean 45.91
Std Dev 10.43
Turn on : 29.2138
Width : 2.710
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

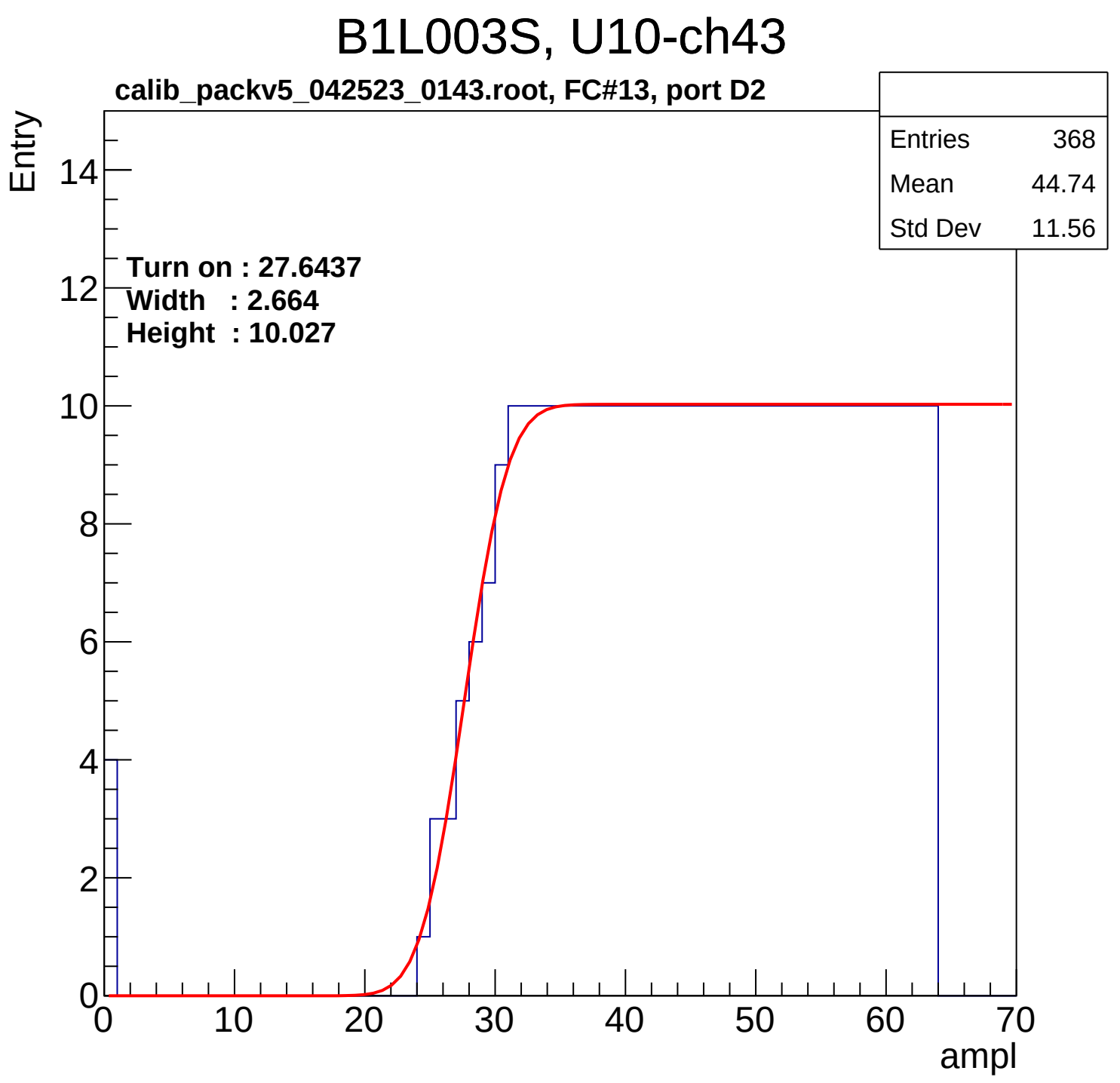

B1L003S, U10-ch38
calib_packv5_042523_0143.root, FC#13, port D2
Entries 353
Mean 45.59
Std Dev 10.84
Turn on : 29.0005
Width : 2.320
Height : 9.962
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

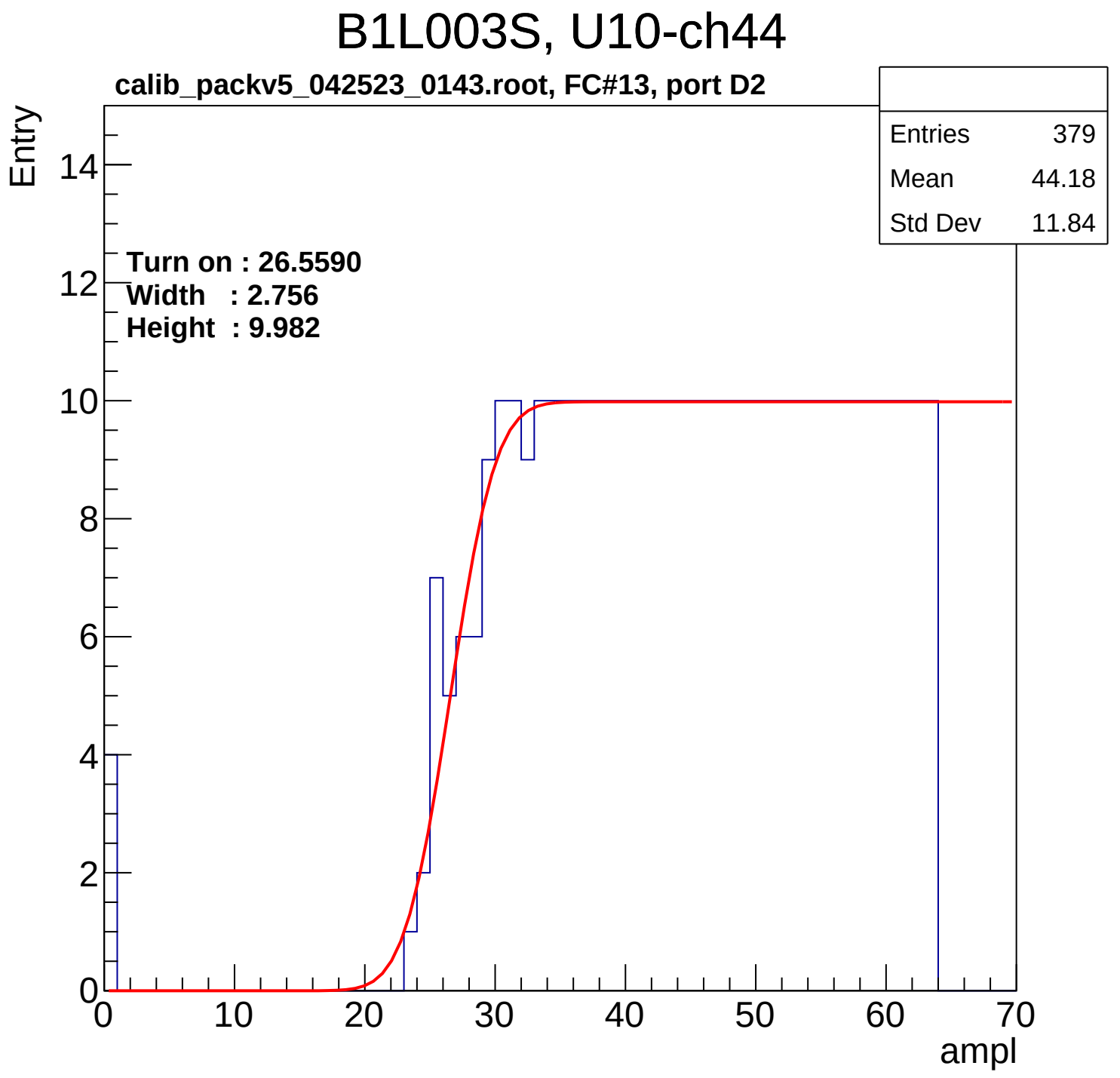

B1L003S, U10-ch39
calib_packv5_042523_0143.root, FC#13, port D2
Entries 353
Mean 45.59
Std Dev 10.82
Turn on : 28.7877
Width : 1.201
Height : 9.872
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

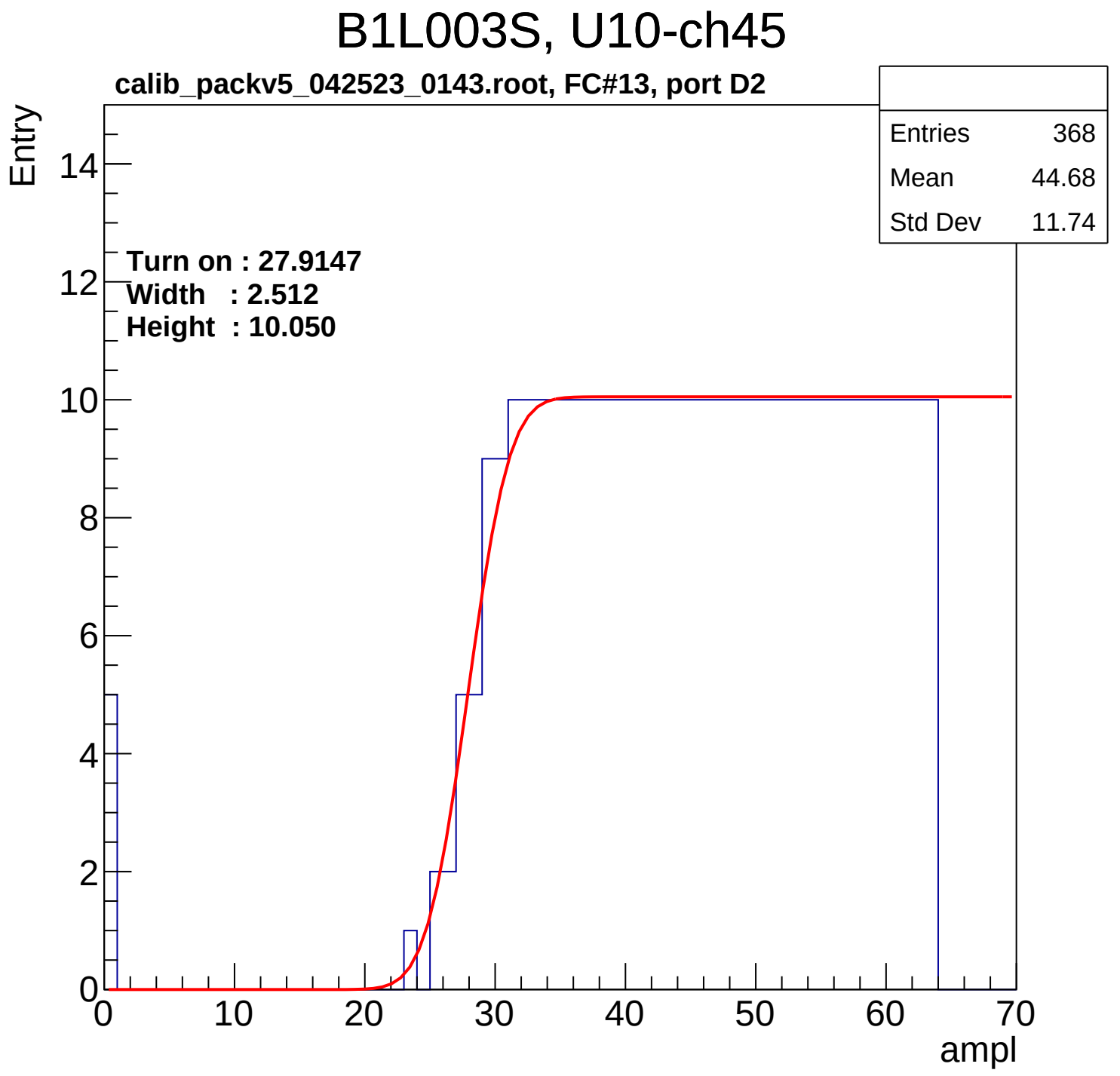

B1L003S, U10-ch40
calib_packv5_042523_0143.root, FC#13, port D2
Entries 358
Mean 45.28
Std Dev 11.15
Turn on : 28.4475
Width : 2.820
Height : 10.034
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

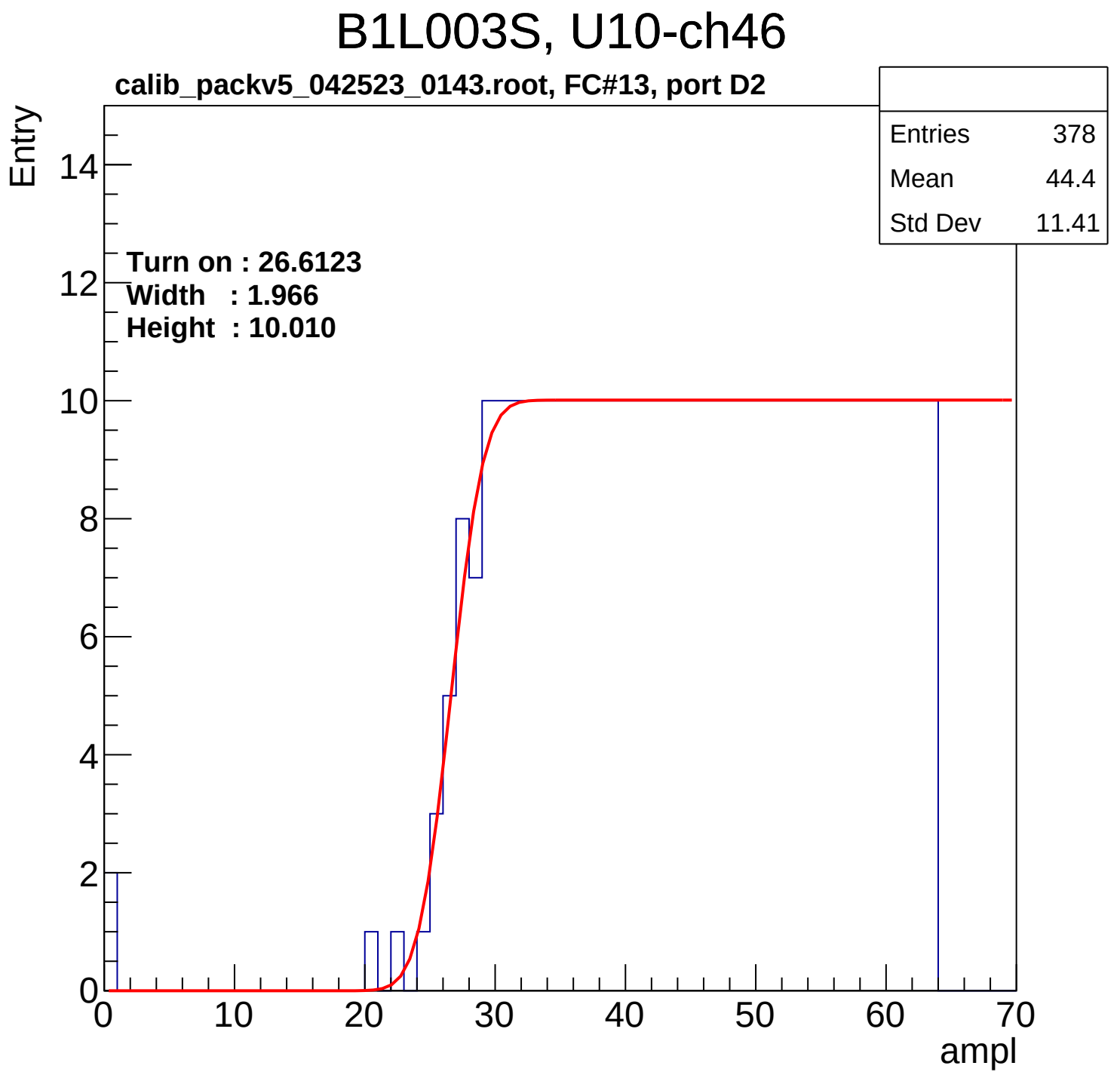

B1L003S, U10-ch41
calib_packv5_042523_0143.root, FC#13, port D2
Entries 373
Mean 44.54
Std Dev 11.52
Turn on : 27.0449
Width : 1.900
Height : 9.893
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

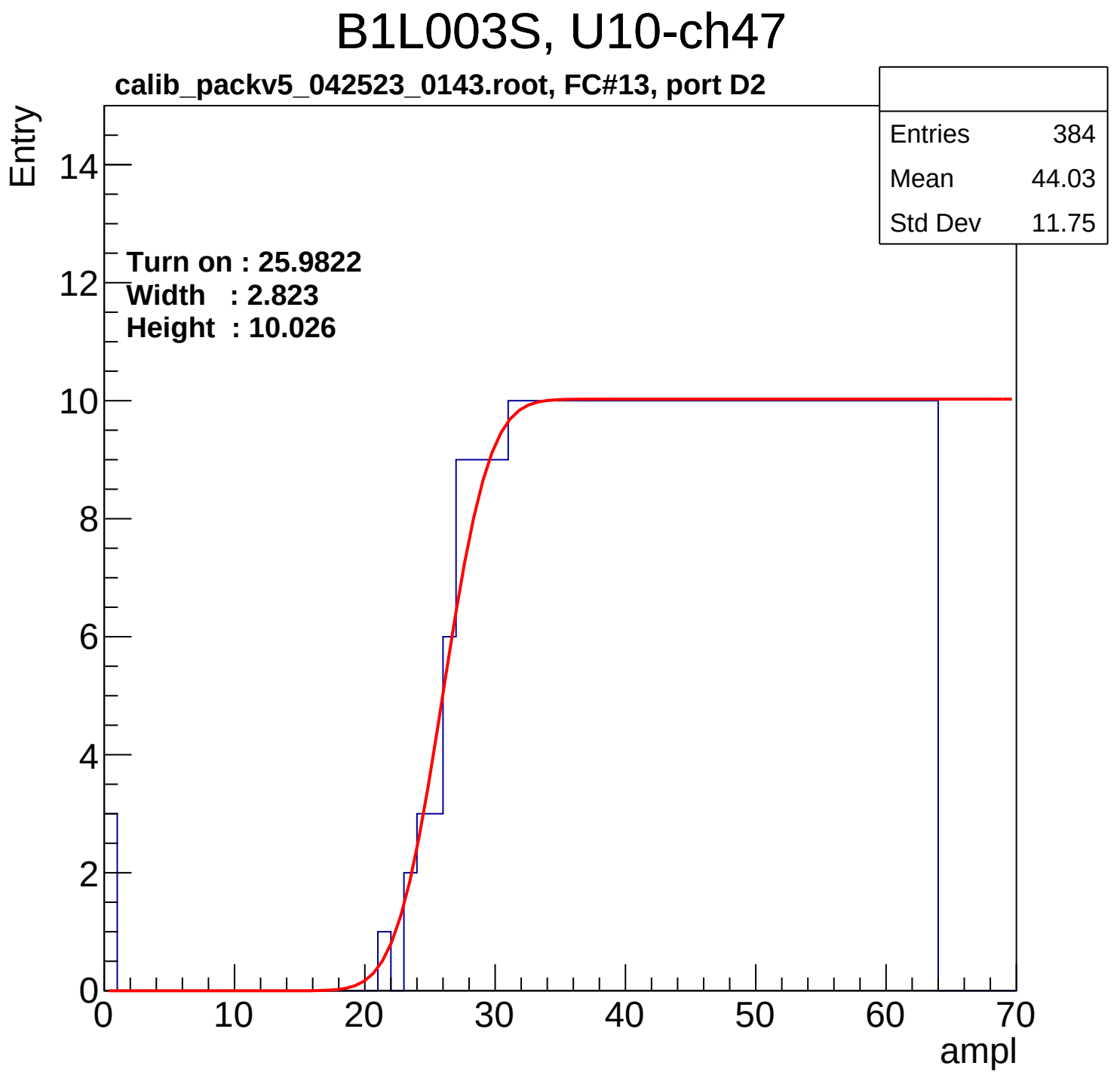

B1L003S, U10-ch42
calib_packv5_042523_0143.root, FC#13, port D2
Entries 377
Mean 44.31
Std Dev 11.74
Turn on : 26.8098
Width : 2.063
Height : 9.977
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

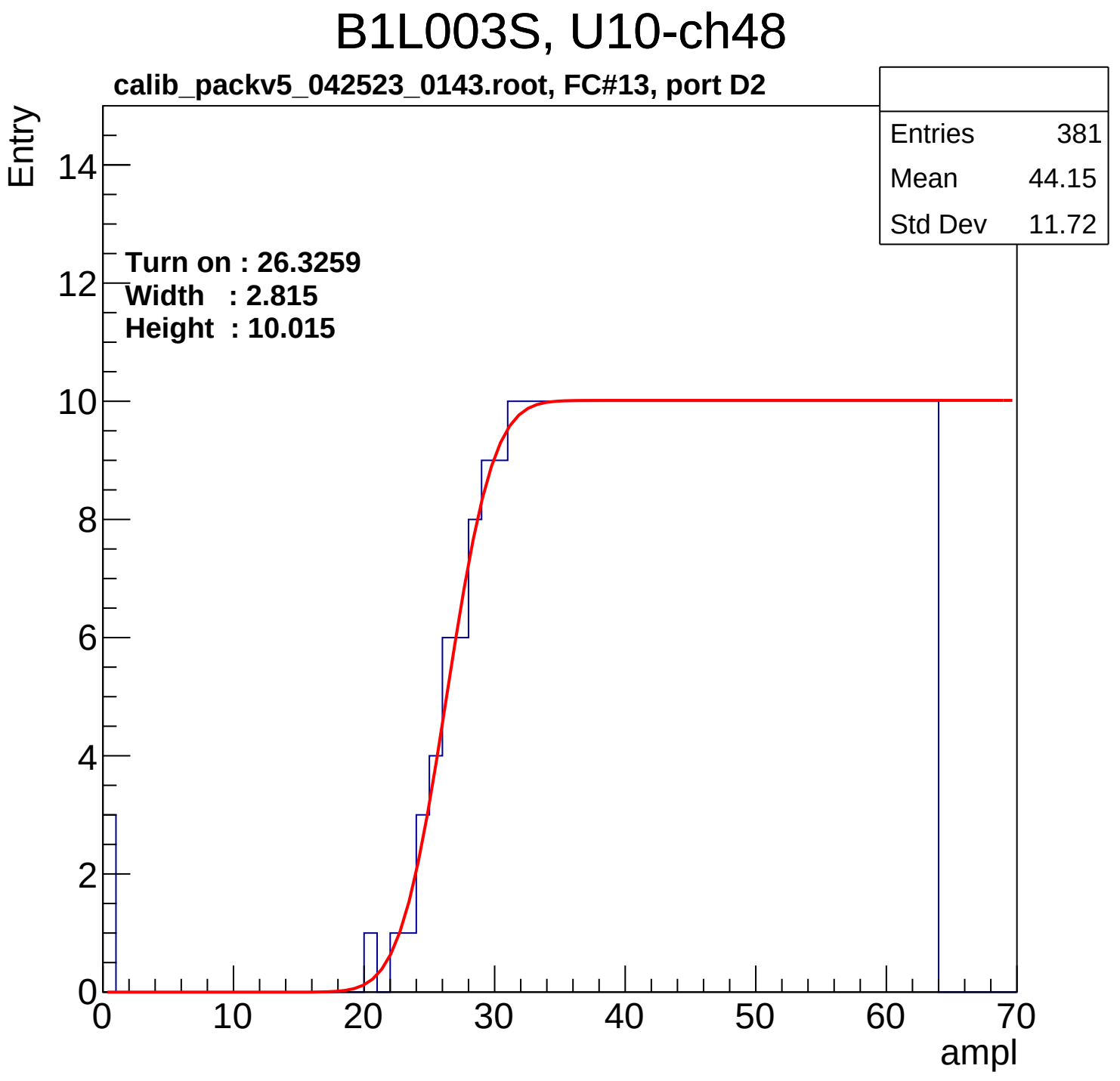

B1L003S, U10-ch43
calib_packv5_042523_0143.root, FC#13, port D2
Entries 368
Mean 44.74
Std Dev 11.56
Turn on : 27.6437
Width : 2.664
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

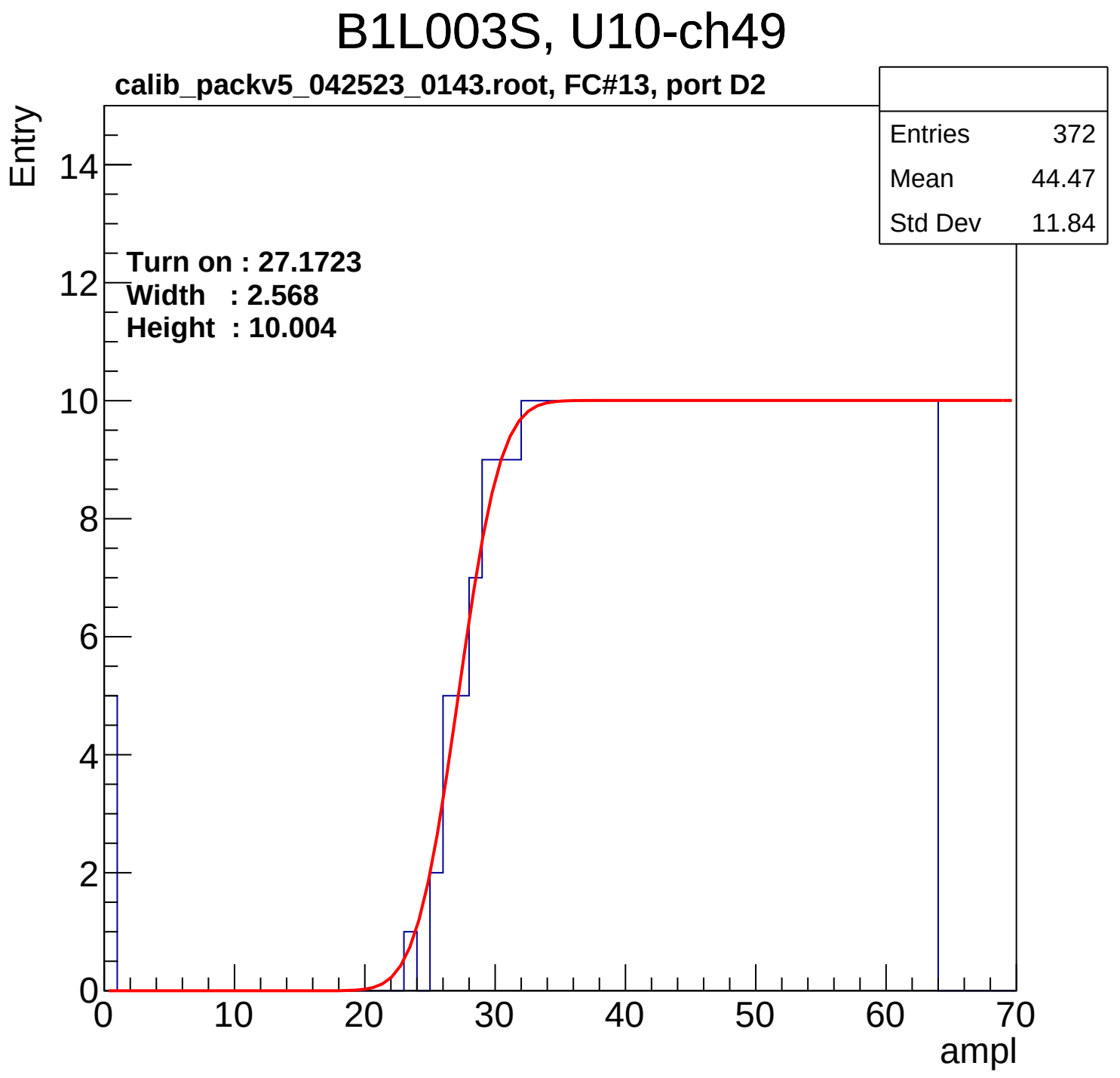

B1L003S, U10-ch44
calib_packv5_042523_0143.root, FC#13, port D2
Entries 379
Mean 44.18
Std Dev 11.84
Turn on : 26.5590
Width : 2.756
Height : 9.982
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

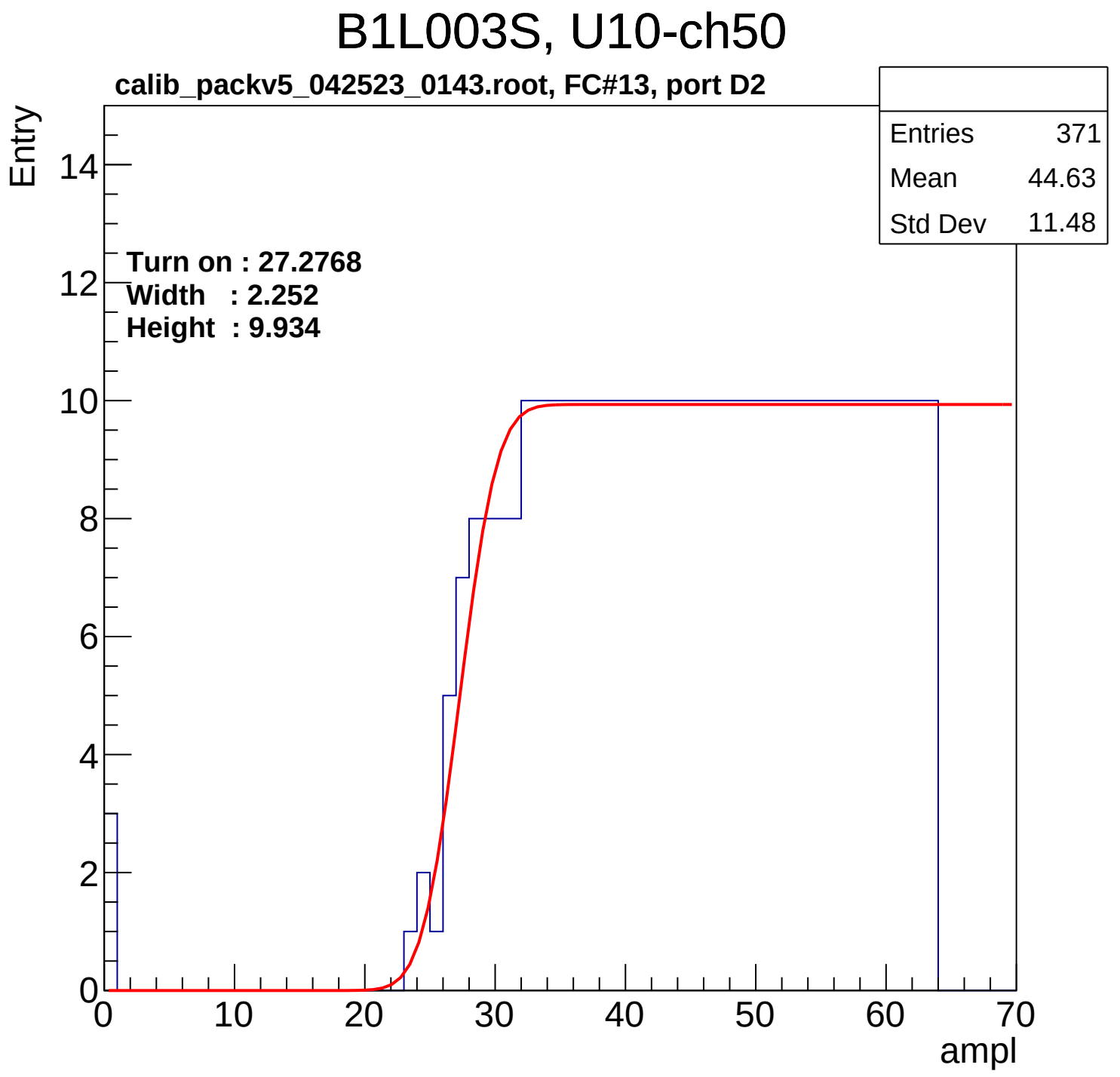

B1L003S, U10-ch45
calib_packv5_042523_0143.root, FC#13, port D2
Entries 368
Mean 44.68
Std Dev 11.74
Turn on : 27.9147
Width : 2.512
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

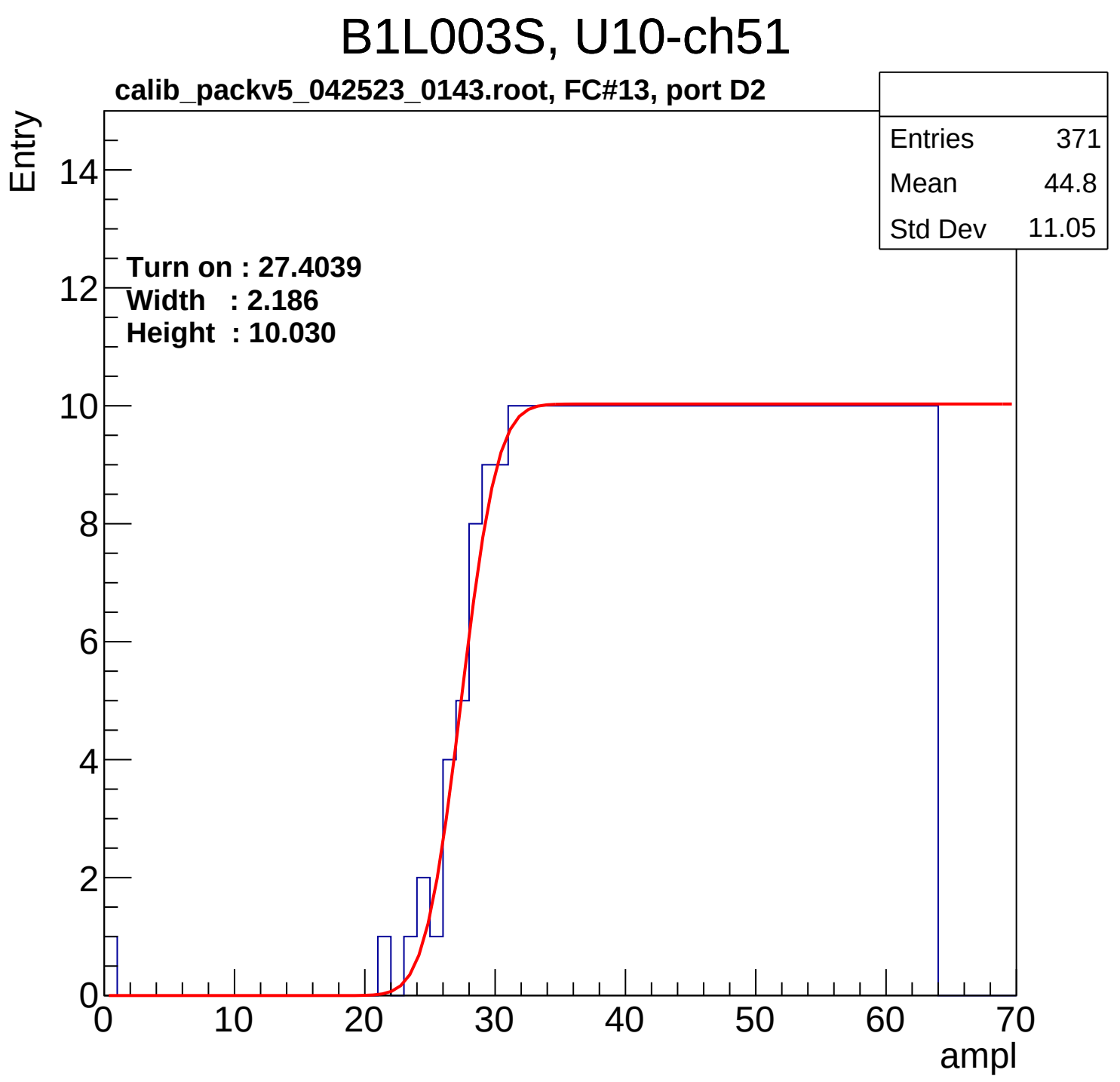

B1L003S, U10-ch46
calib_packv5_042523_0143.root, FC#13, port D2
Entries 378
Mean 44.4
Std Dev 11.41
Turn on : 26.6123
Width : 1.966
Height : 10.010
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

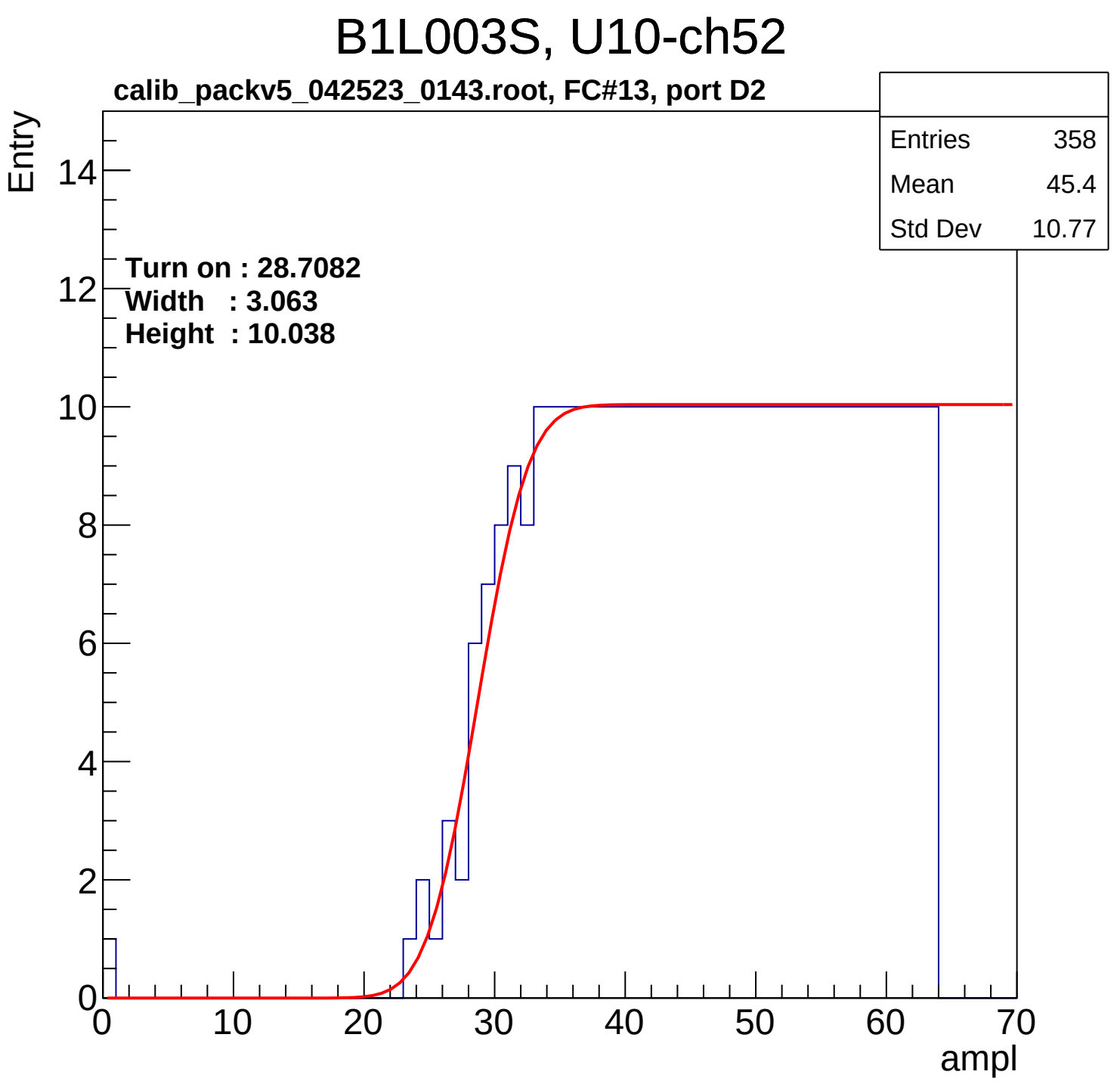

B1L003S, U10-ch47
calib_packv5_042523_0143.root, FC#13, port D2
Entries 384
Mean 44.03
Std Dev 11.75
Turn on : 25.9822
Width : 2.823
Height : 10.026
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

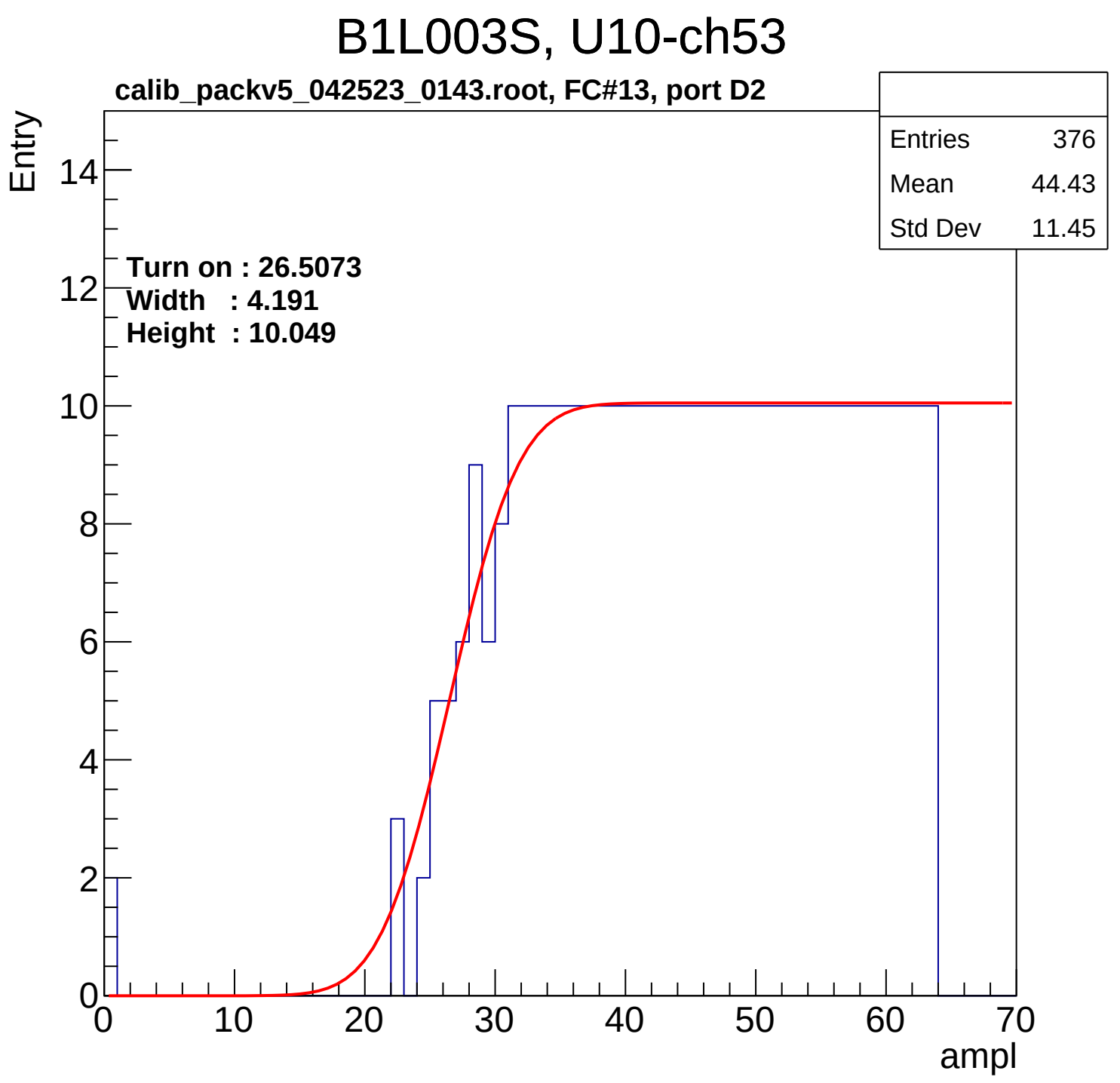

B1L003S, U10-ch48
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 44.15
Std Dev 11.72
Turn on : 26.3259
Width : 2.815
Height : 10.015
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

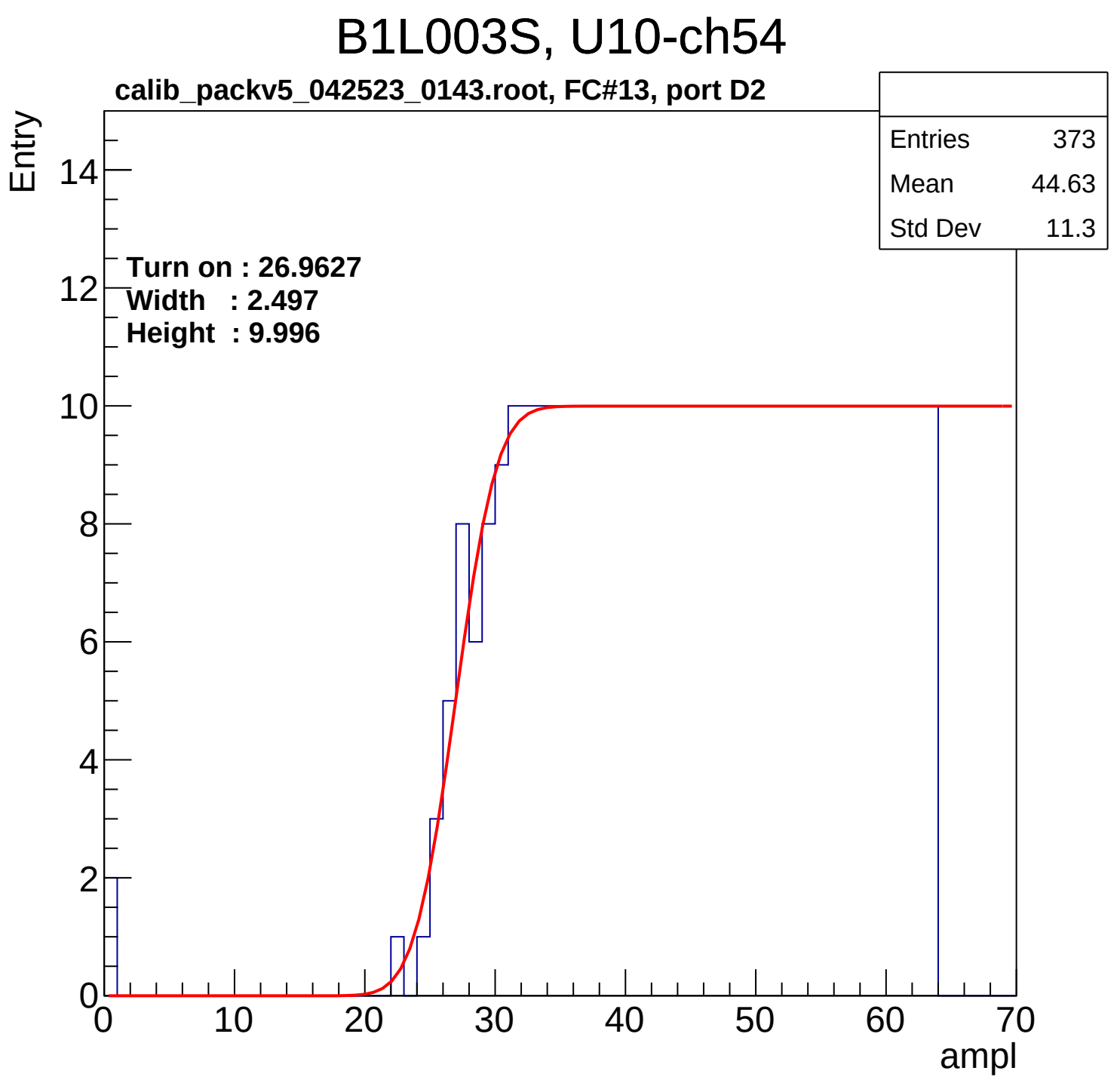

B1L003S, U10-ch49
calib_packv5_042523_0143.root, FC#13, port D2
Entries 372
Mean 44.47
Std Dev 11.84
Turn on : 27.1723
Width : 2.568
Height : 10.004
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

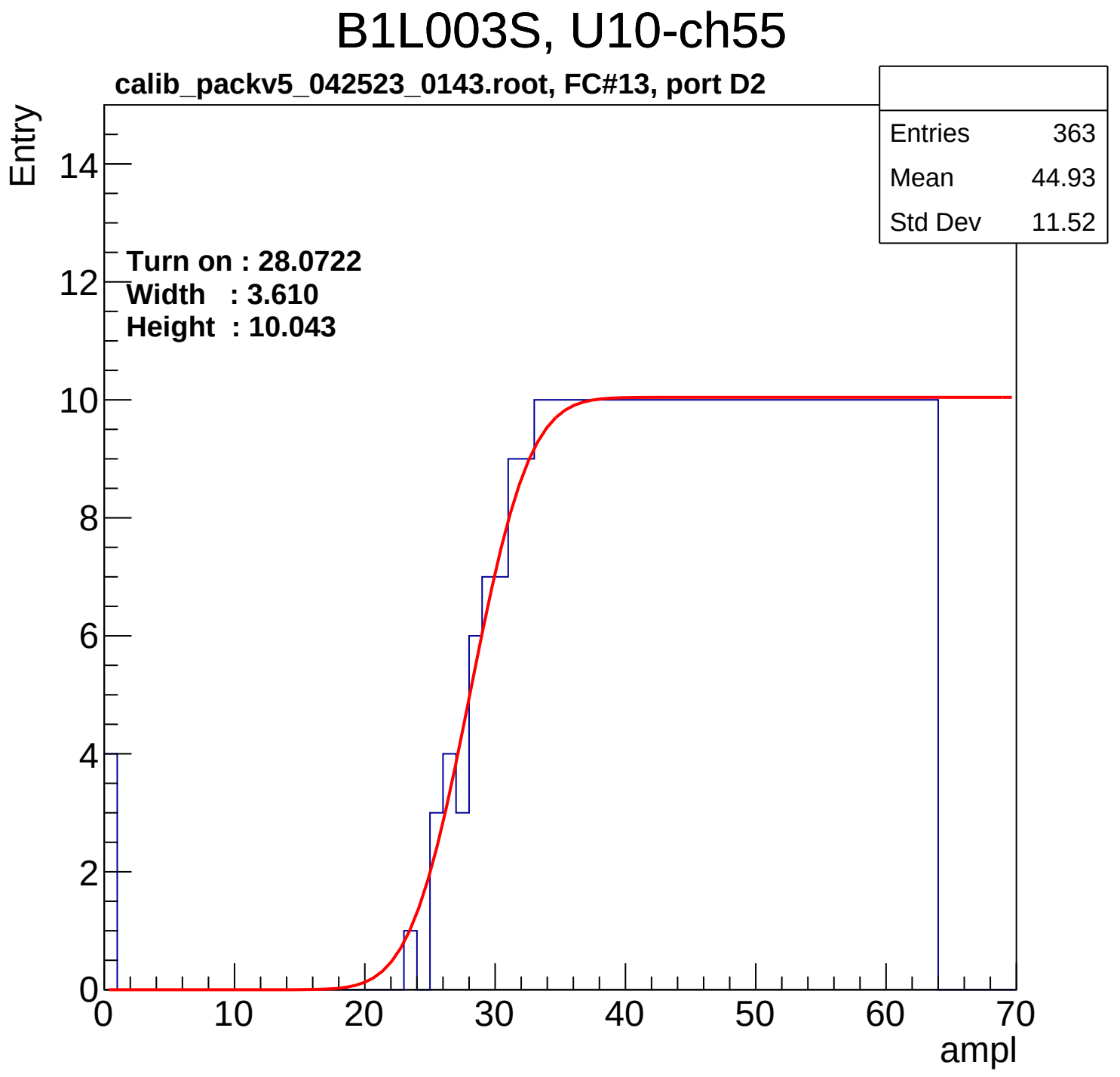

B1L003S, U10-ch50
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.63
Std Dev 11.48
Turn on : 27.2768
Width : 2.252
Height : 9.934
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

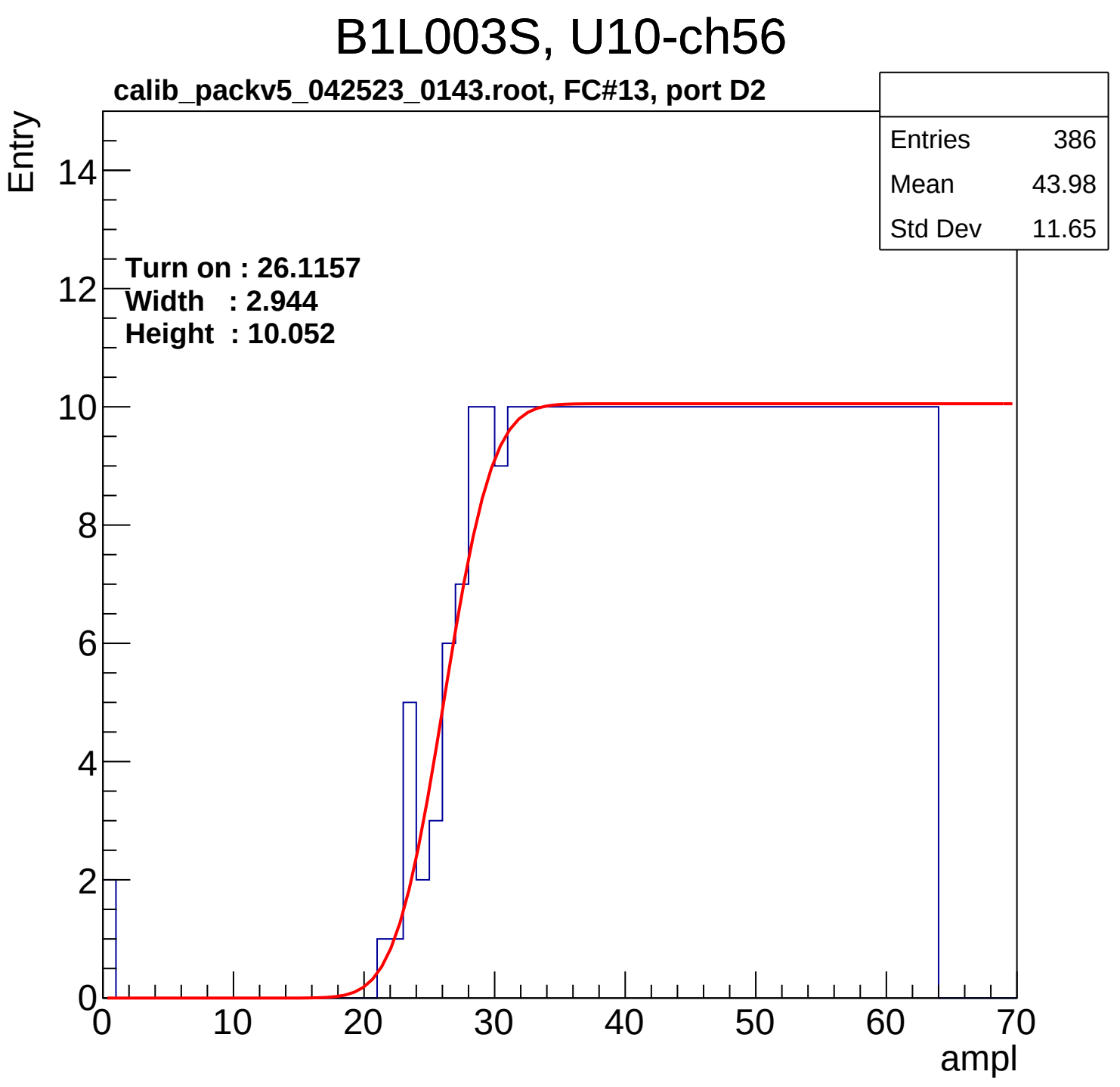

B1L003S, U10-ch51
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.8
Std Dev 11.05
Turn on : 27.4039
Width : 2.186
Height : 10.030
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

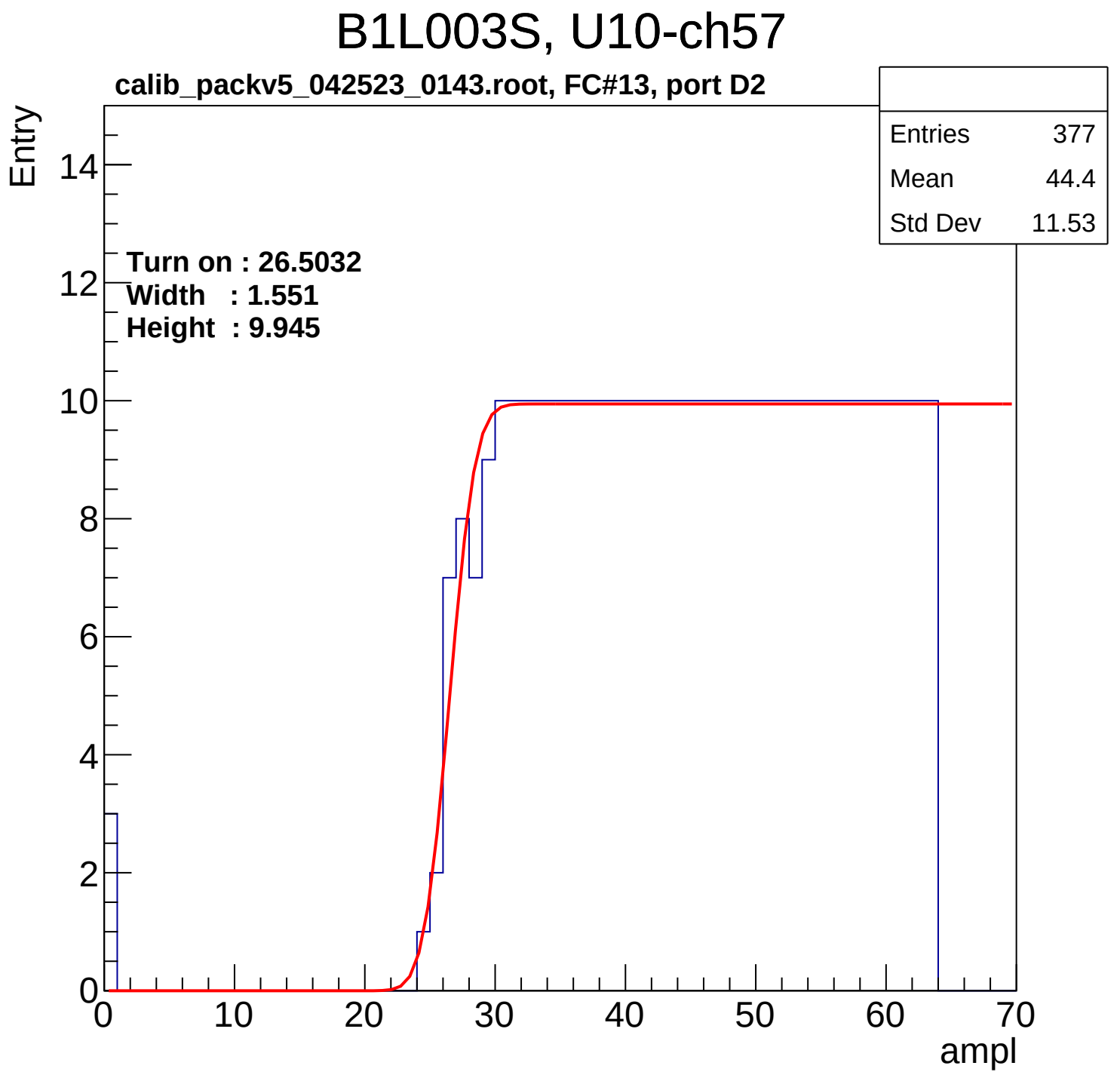

B1L003S, U10-ch52
calib_packv5_042523_0143.root, FC#13, port D2
Entries 358
Mean 45.4
Std Dev 10.77
Turn on : 28.7082
Width : 3.063
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

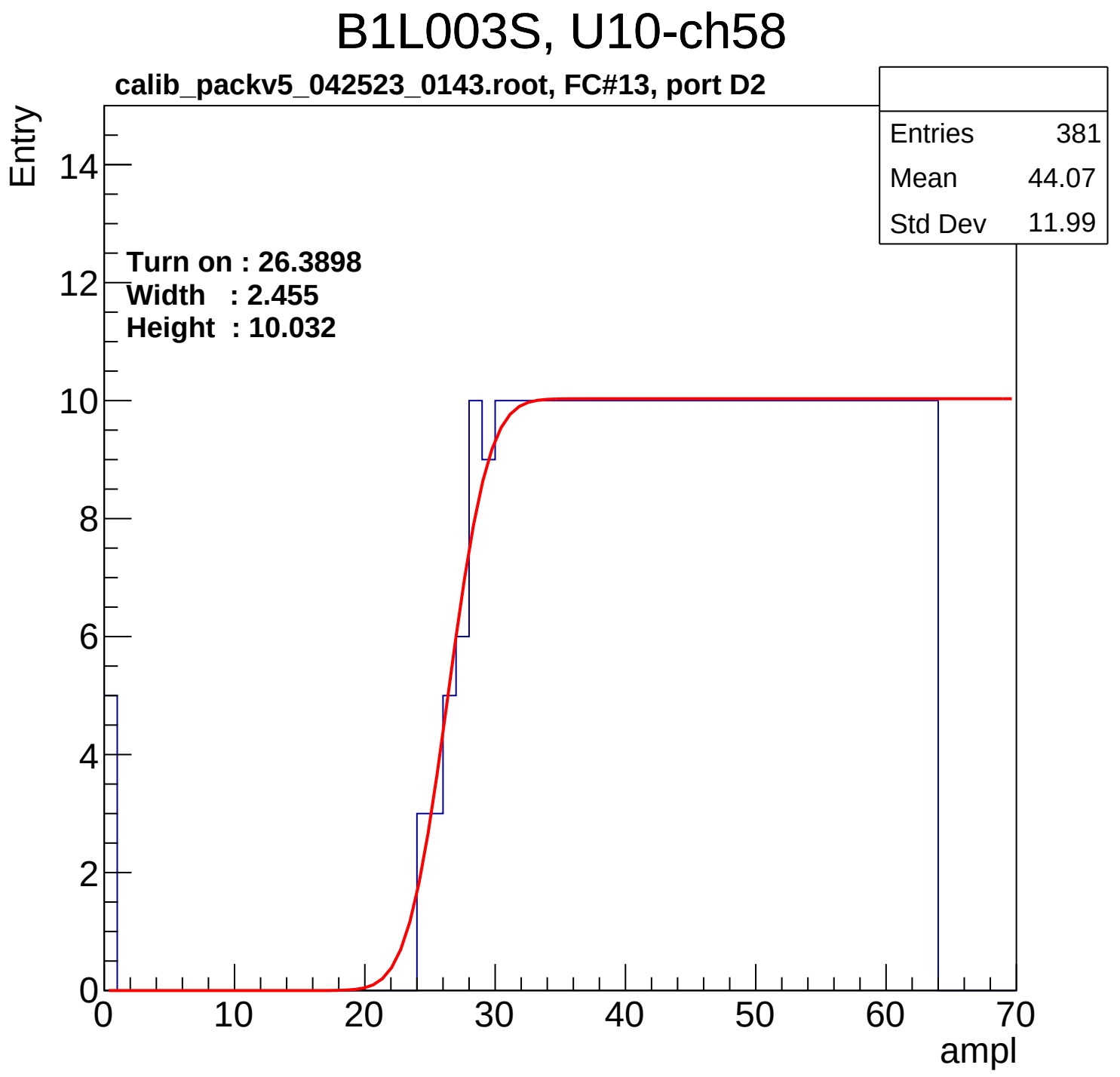

B1L003S, U10-ch53
calib_packv5_042523_0143.root, FC#13, port D2
Entries 376
Mean 44.43
Std Dev 11.45
Turn on : 26.5073
Width : 4.191
Height : 10.049
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

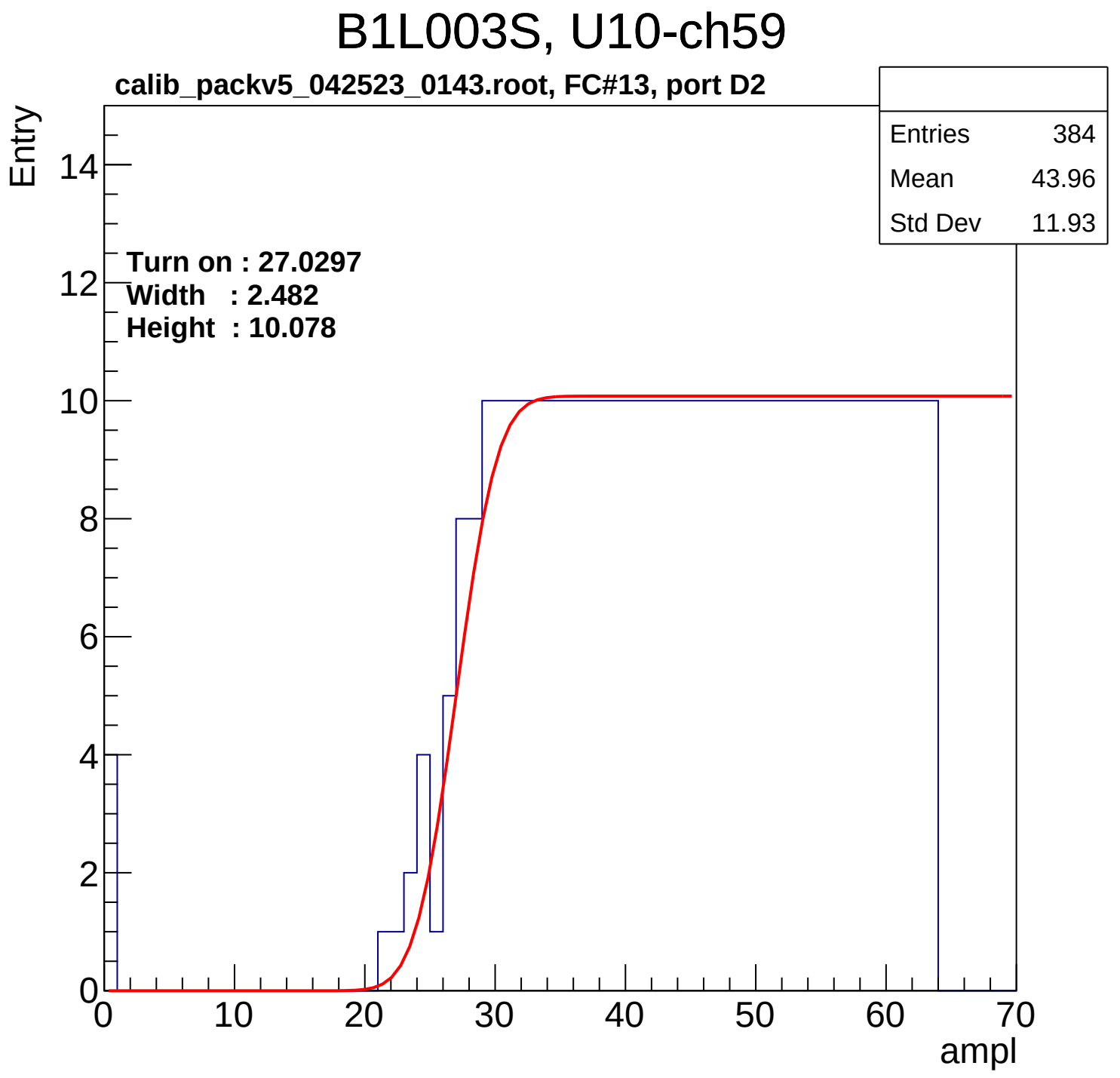

B1L003S, U10-ch54
calib_packv5_042523_0143.root, FC#13, port D2
Entries 373
Mean 44.63
Std Dev 11.3
Turn on : 26.9627
Width : 2.497
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

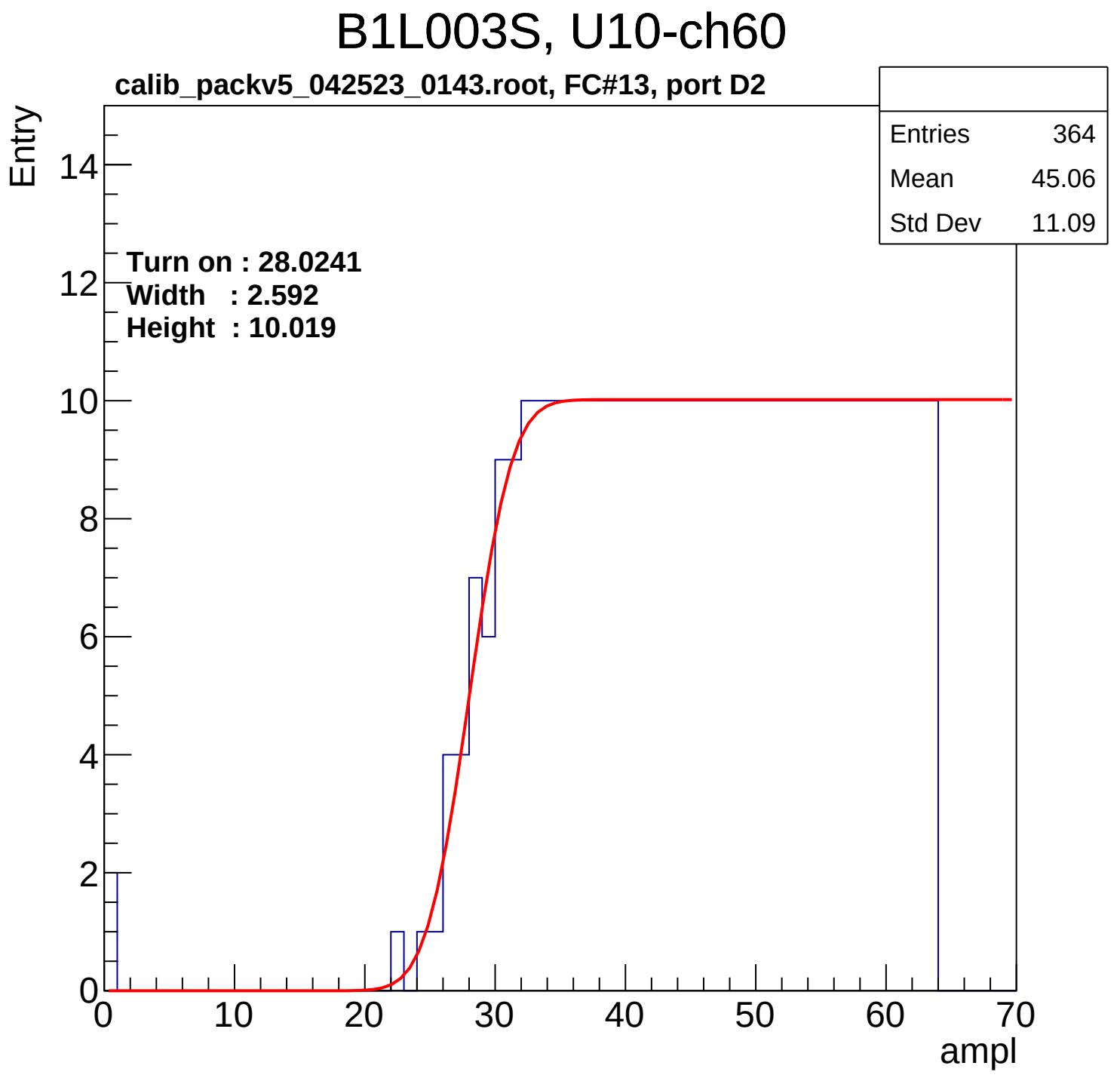

B1L003S, U10-ch55
calib_packv5_042523_0143.root, FC#13, port D2
Entries 363
Mean 44.93
Std Dev 11.52
Turn on : 28.0722
Width : 3.610
Height : 10.043
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

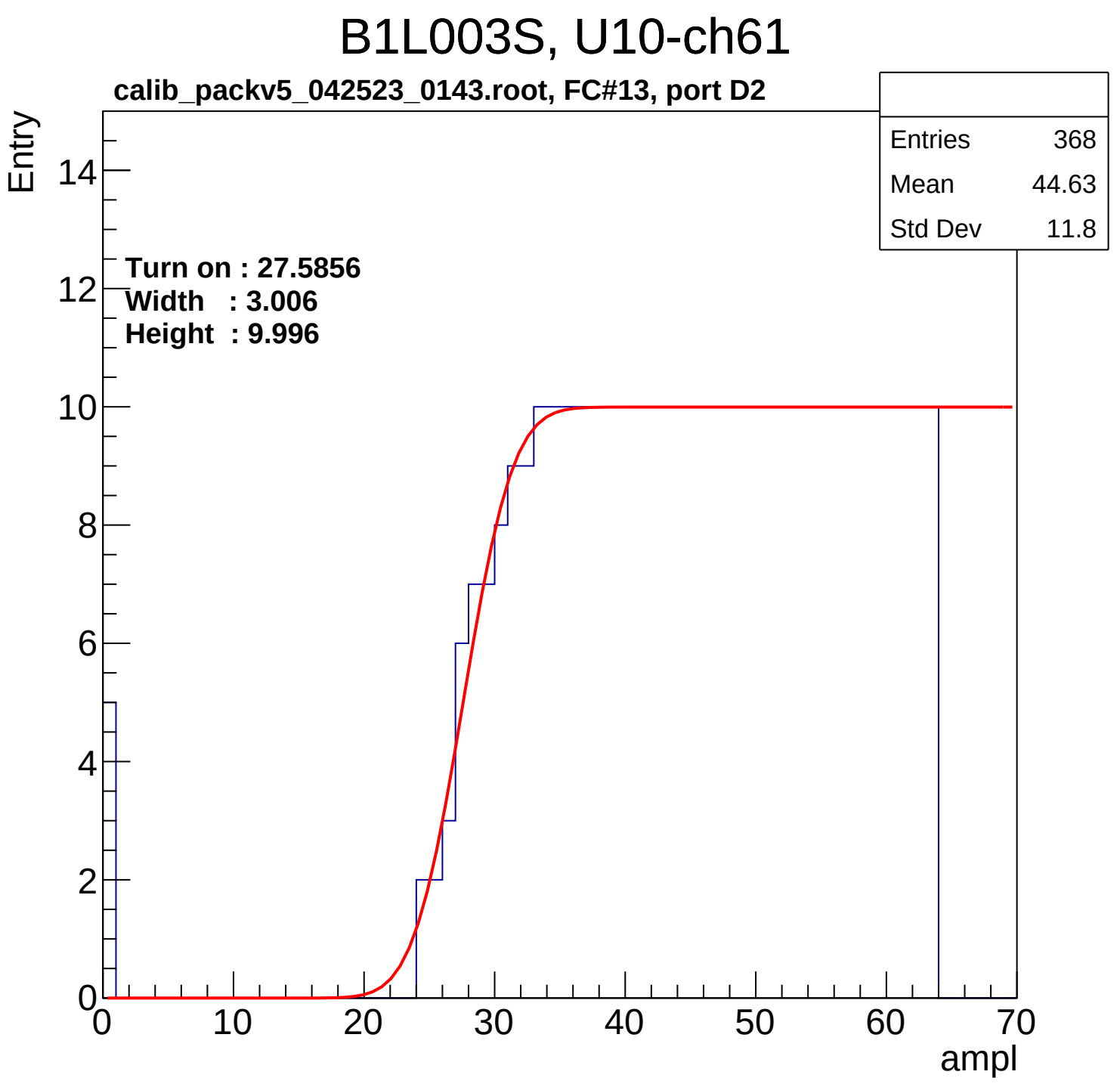

B1L003S, U10-ch56
calib_packv5_042523_0143.root, FC#13, port D2
Entries 386
Mean 43.98
Std Dev 11.65
Turn on : 26.1157
Width : 2.944
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

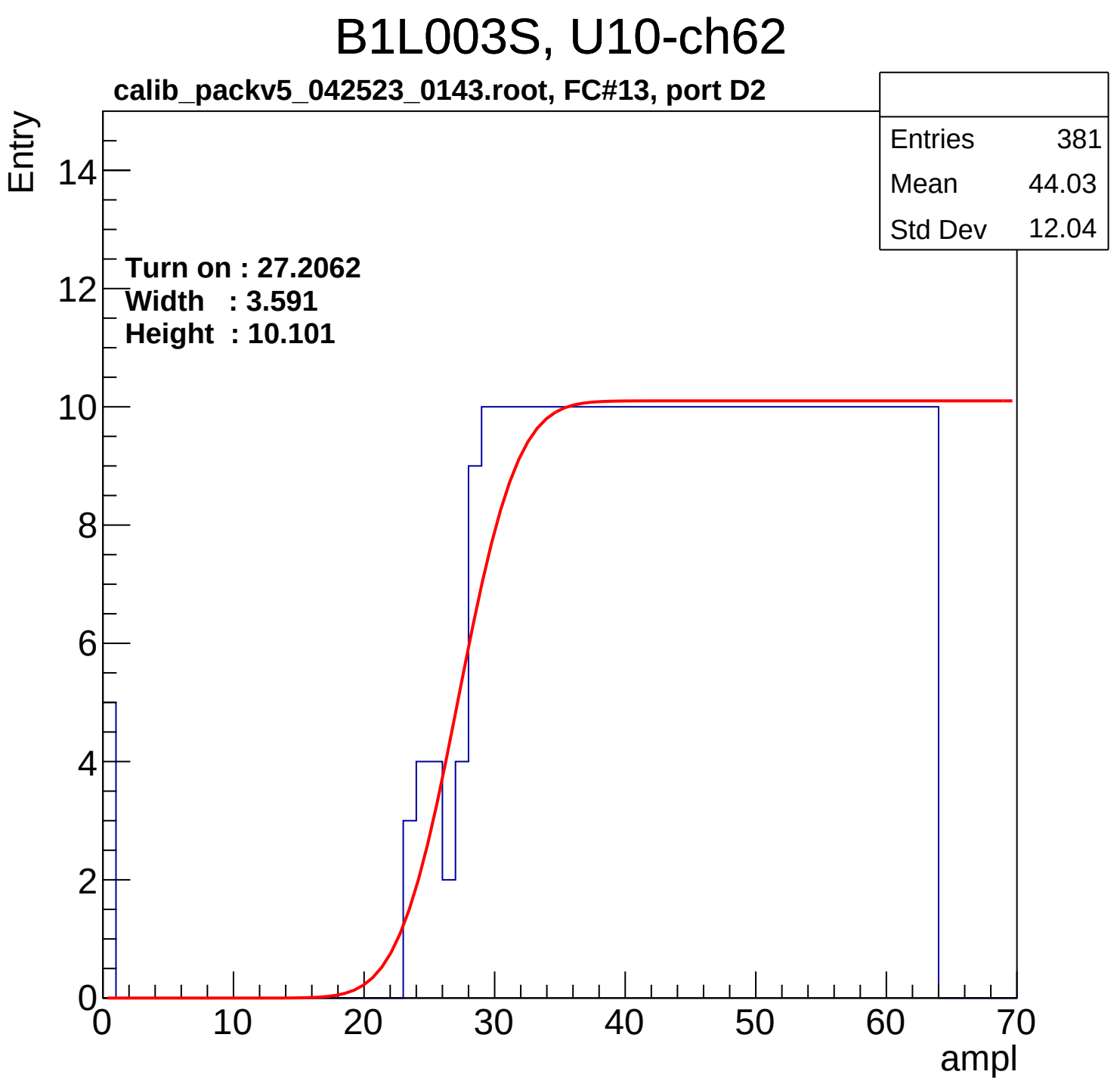

B1L003S, U10-ch57
calib_packv5_042523_0143.root, FC#13, port D2
Entries 377
Mean 44.4
Std Dev 11.53
Turn on : 26.5032
Width : 1.551
Height : 9.945
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

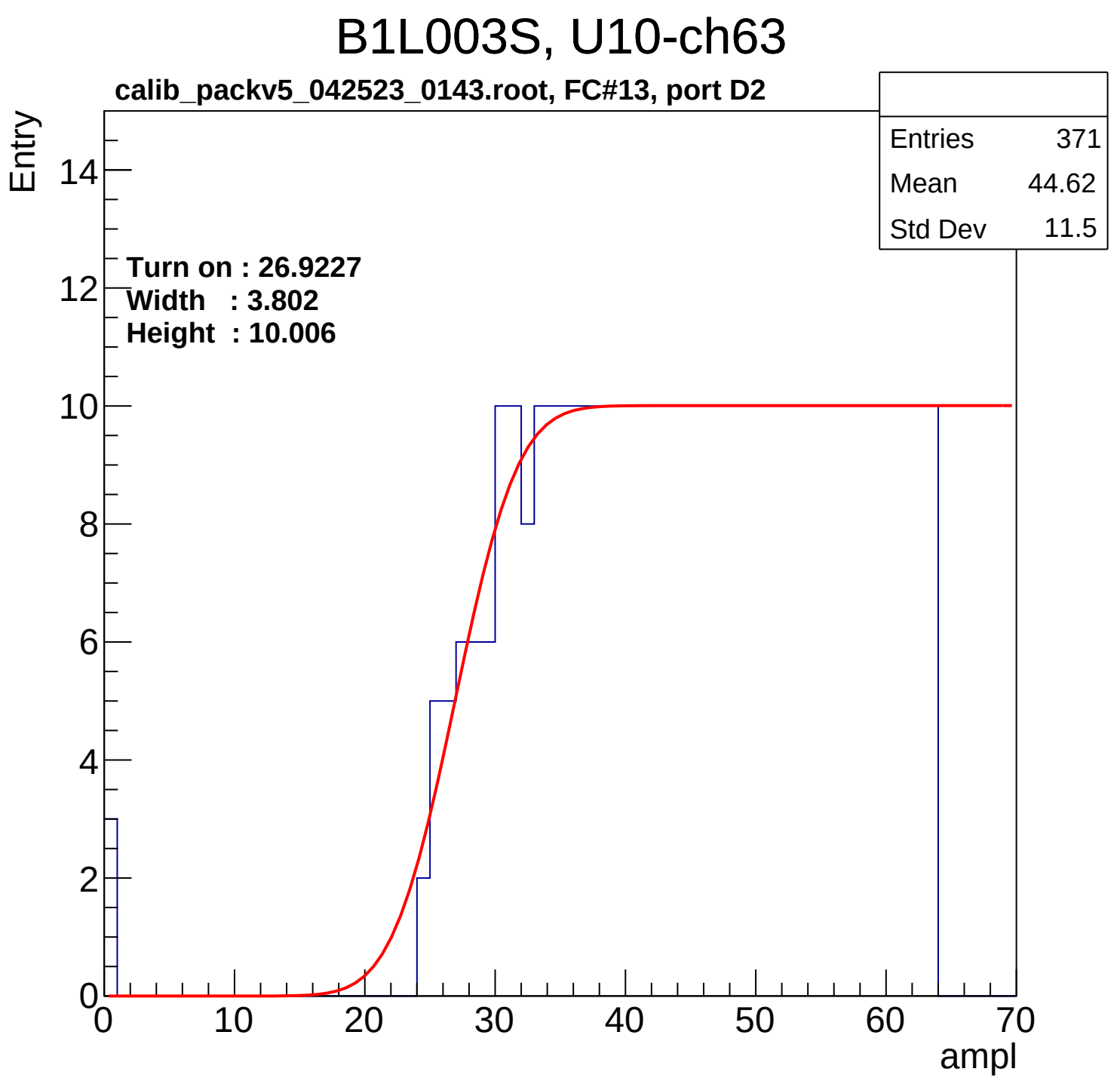

B1L003S, U10-ch58
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 44.07
Std Dev 11.99
Turn on : 26.3898
Width : 2.455
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

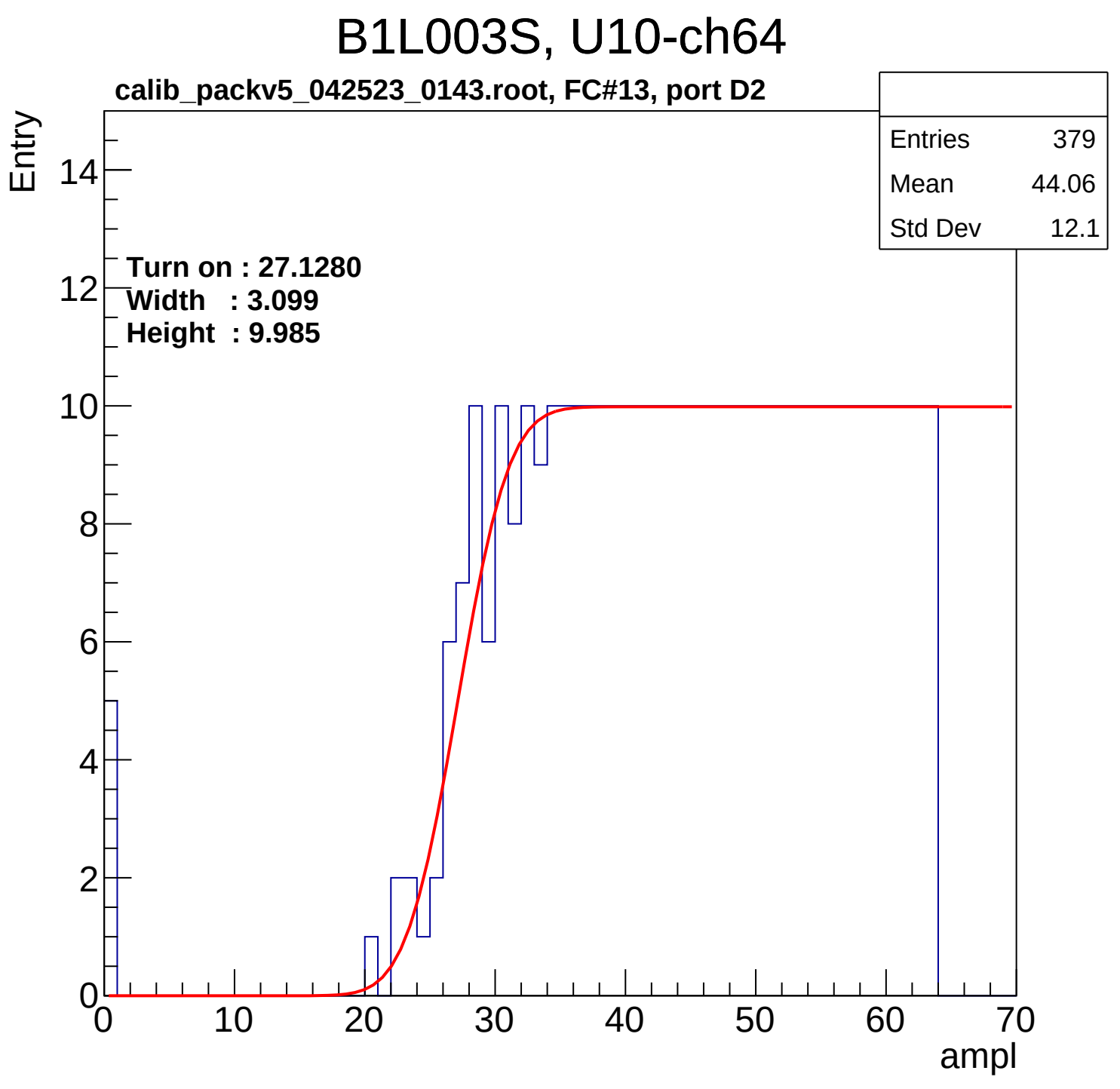

B1L003S, U10-ch59
calib_packv5_042523_0143.root, FC#13, port D2
Entries 384
Mean 43.96
Std Dev 11.93
Turn on : 27.0297
Width : 2.482
Height : 10.078
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

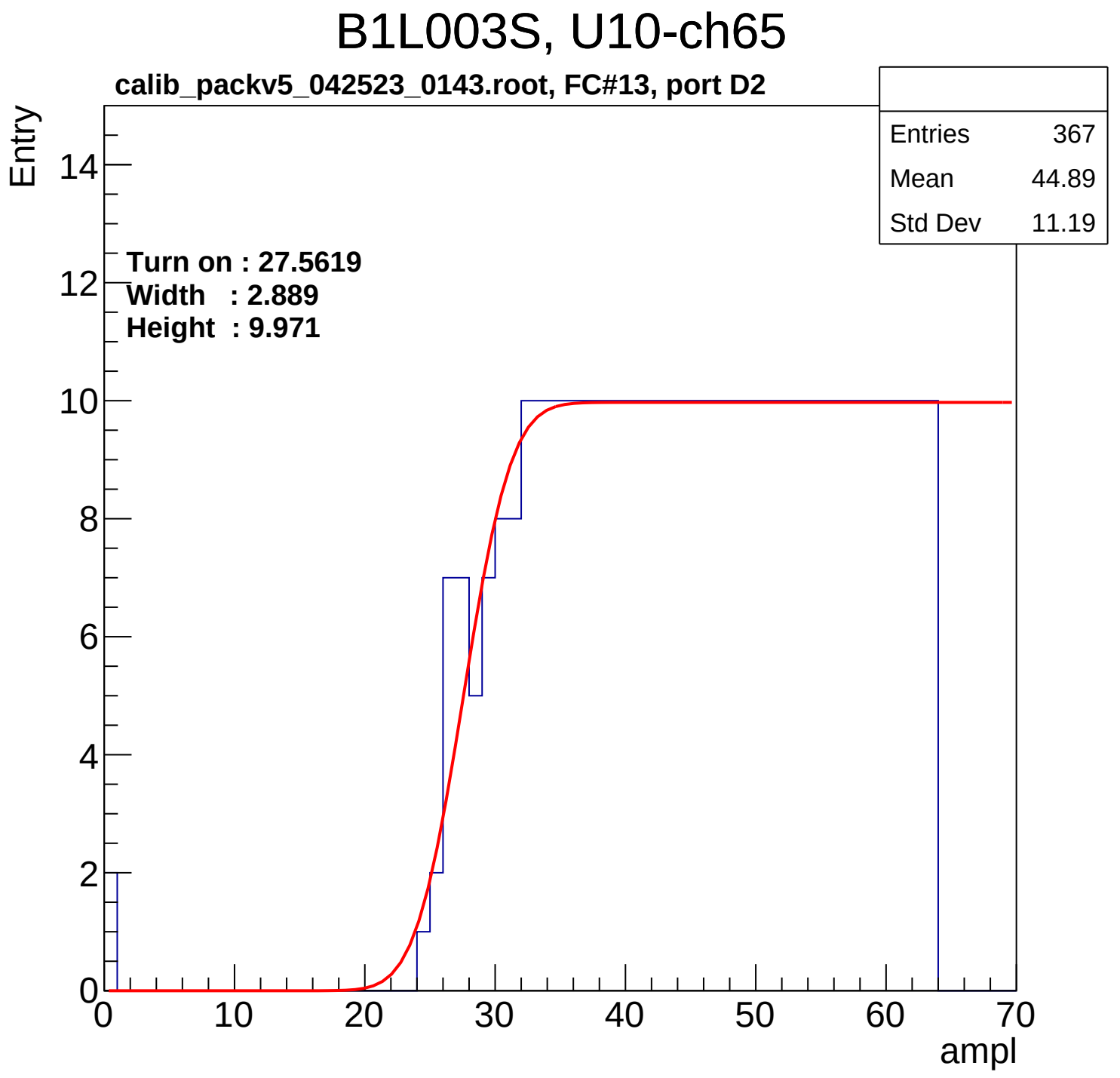

B1L003S, U10-ch60
calib_packv5_042523_0143.root, FC#13, port D2
Entries 364
Mean 45.06
Std Dev 11.09
Turn on : 28.0241
Width : 2.592
Height : 10.019
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

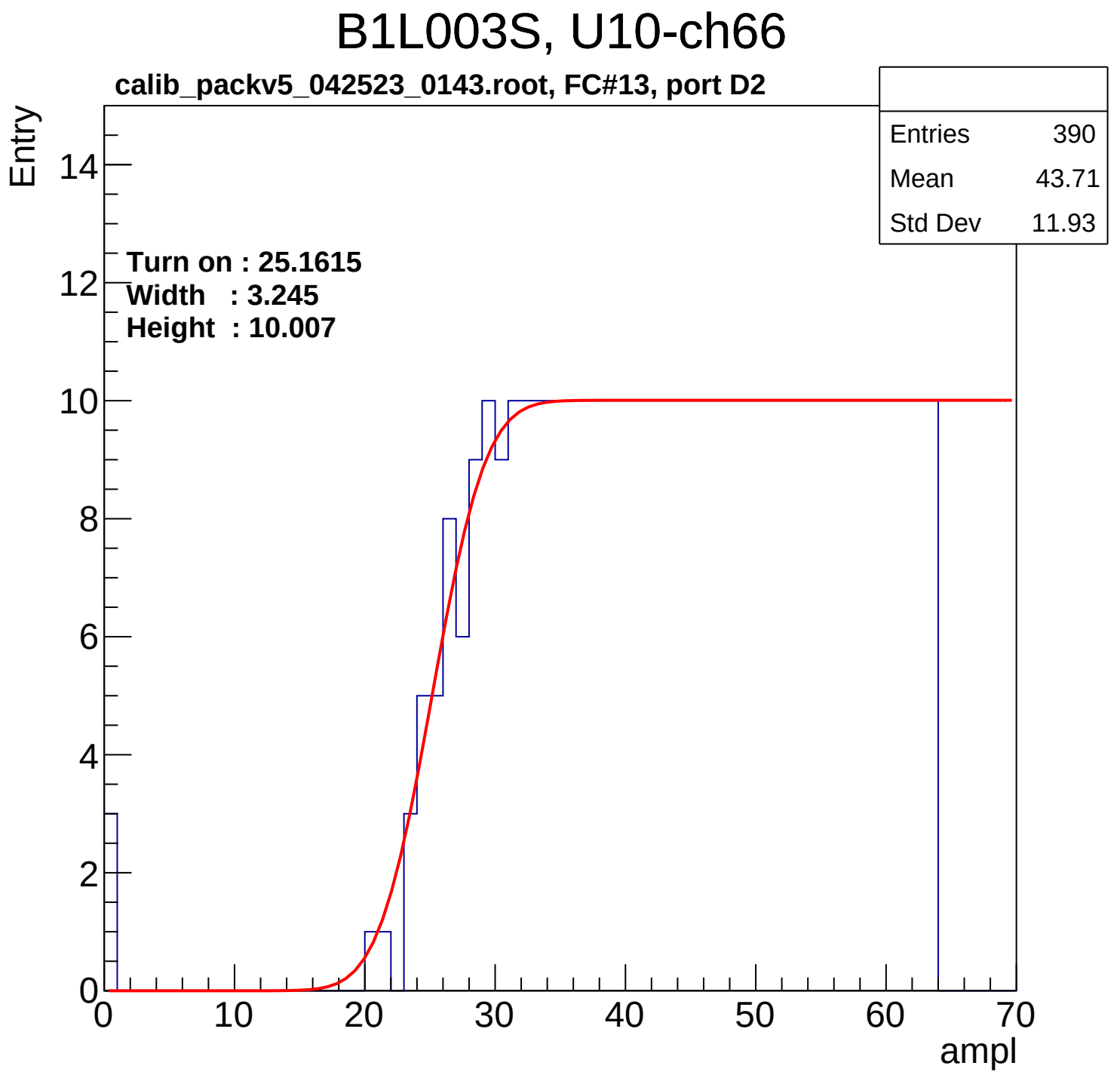

B1L003S, U10-ch61
calib_packv5_042523_0143.root, FC#13, port D2
Entries 368
Mean 44.63
Std Dev 11.8
Turn on : 27.5856
Width : 3.006
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

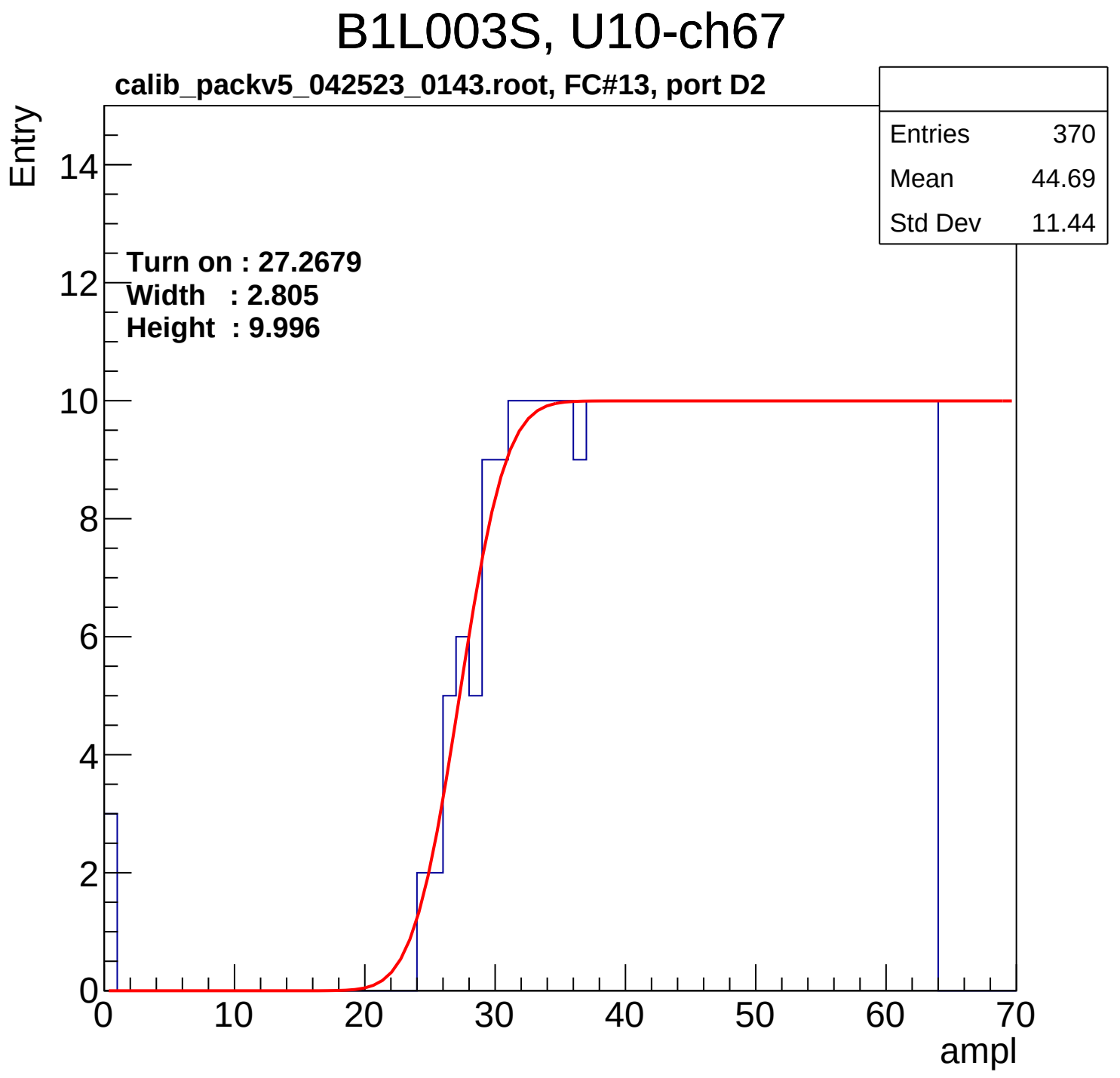

B1L003S, U10-ch62
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 44.03
Std Dev 12.04
Turn on : 27.2062
Width : 3.591
Height : 10.101
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

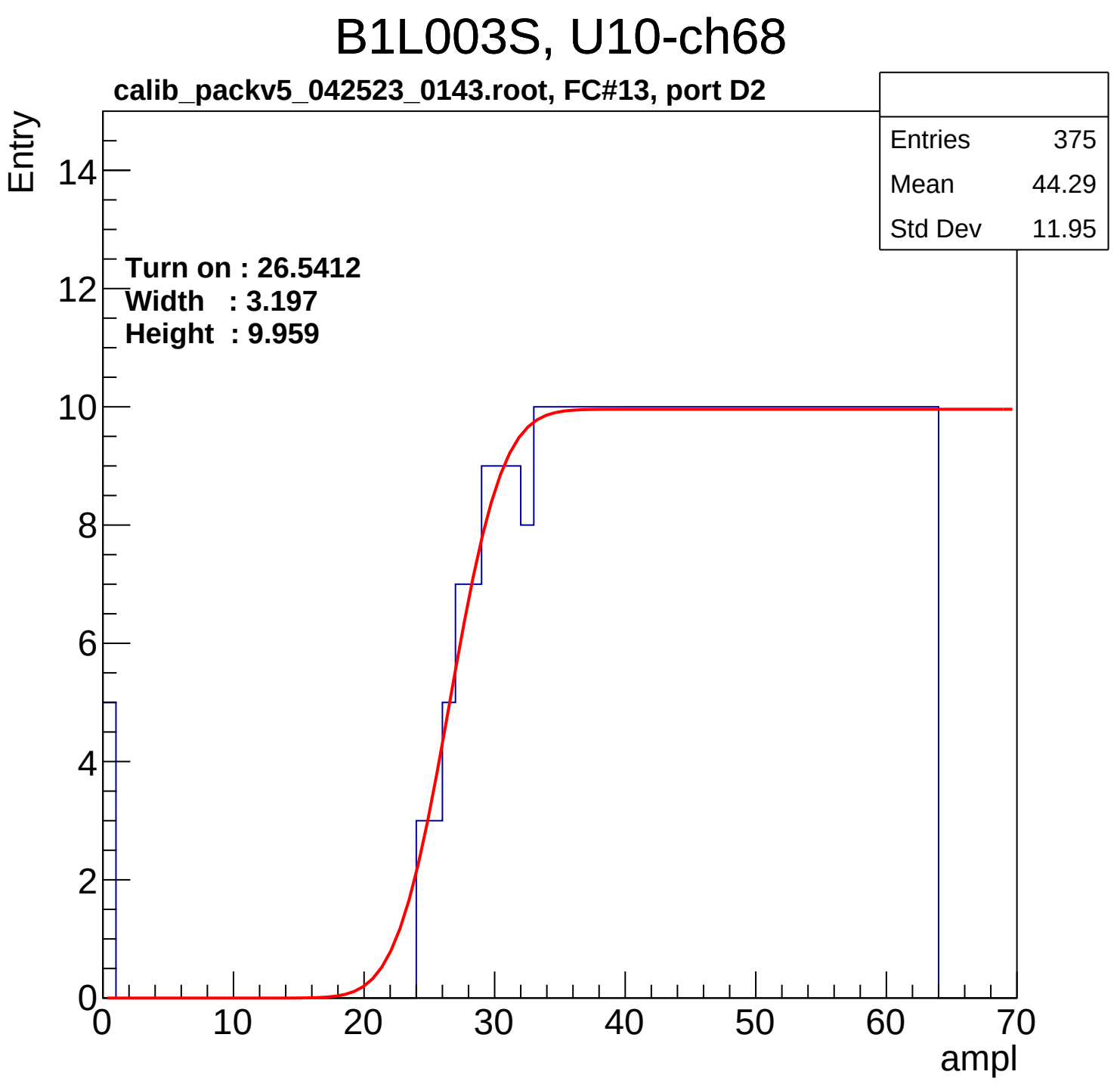

B1L003S, U10-ch63
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.62
Std Dev 11.5
Turn on : 26.9227
Width : 3.802
Height : 10.006
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

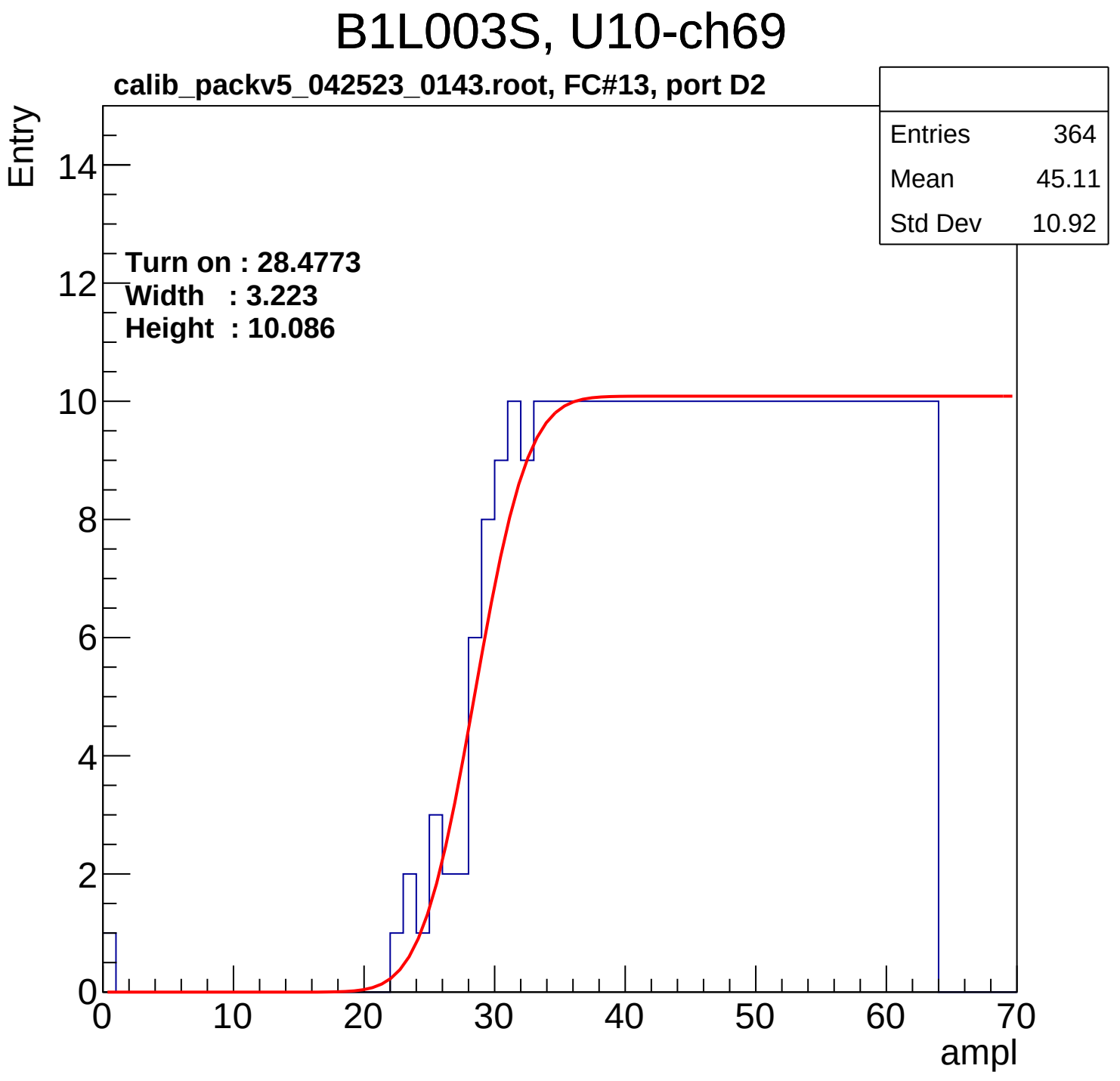

B1L003S, U10-ch64
calib_packv5_042523_0143.root, FC#13, port D2
Entries 379
Mean 44.06
Std Dev 12.1
Turn on : 27.1280
Width : 3.099
Height : 9.985
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

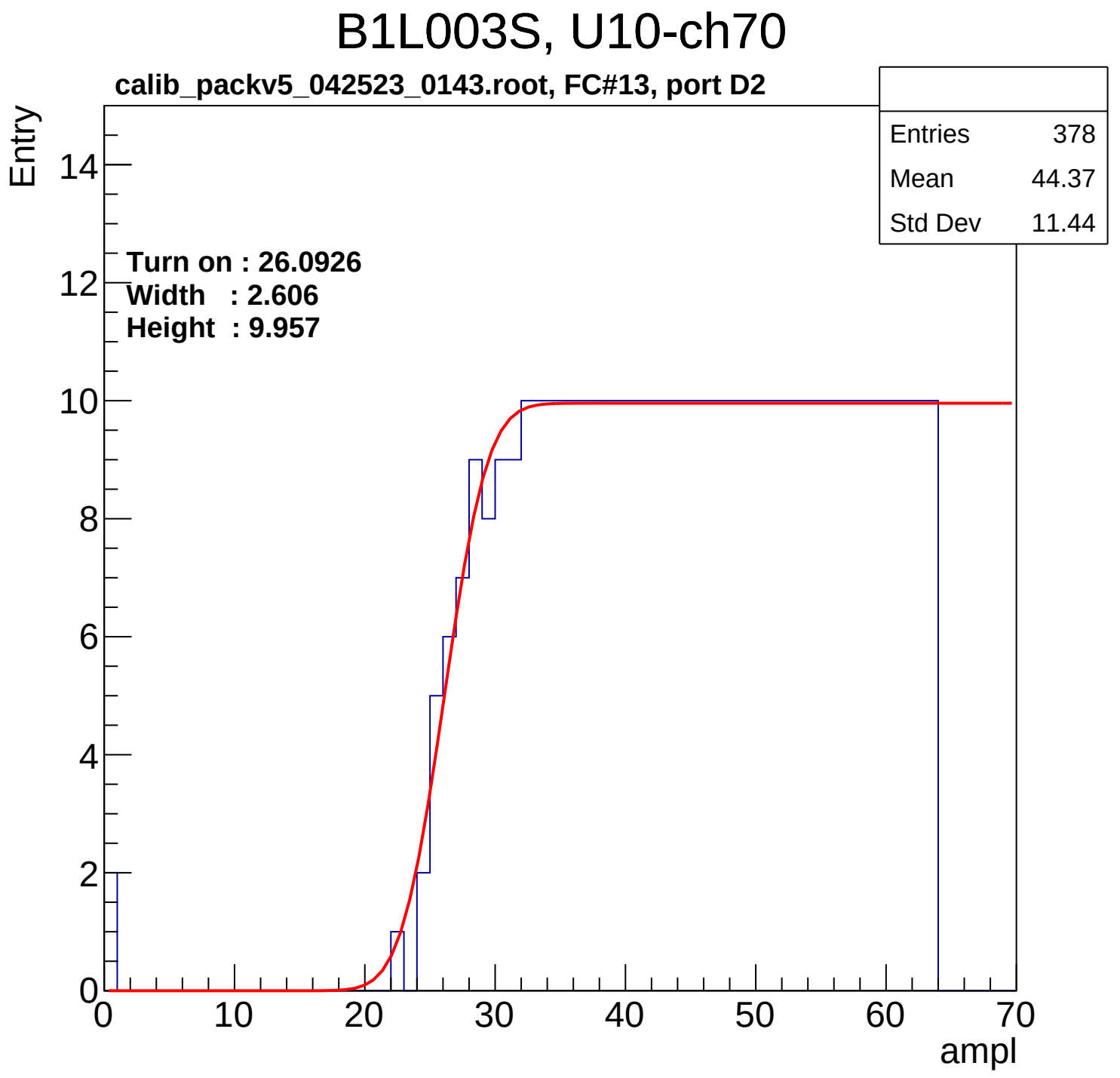

B1L003S, U10-ch65
calib_packv5_042523_0143.root, FC#13, port D2
Entries 367
Mean 44.89
Std Dev 11.19
Turn on : 27.5619
Width : 2.889
Height : 9.971
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

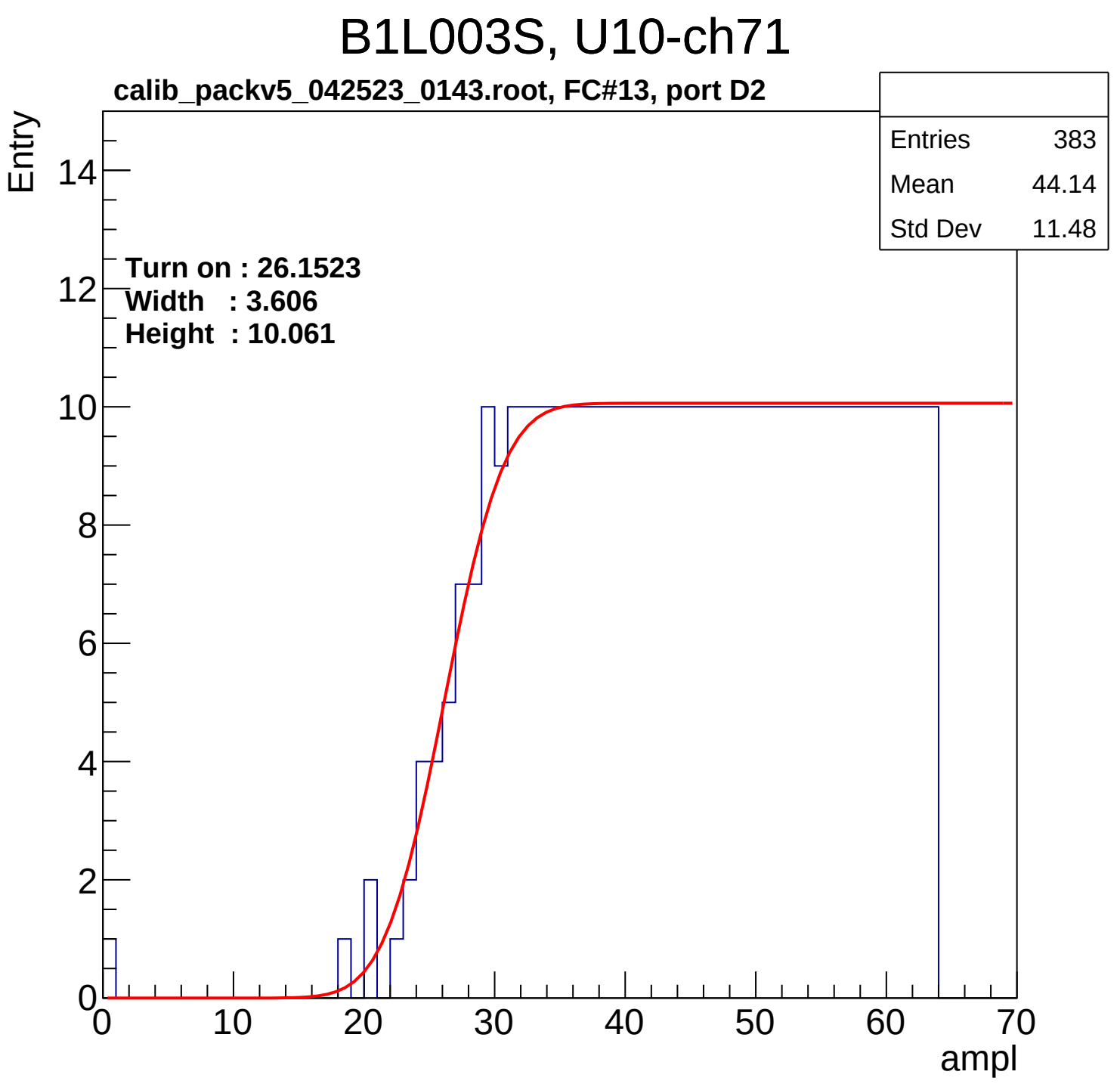

B1L003S, U10-ch66
calib_packv5_042523_0143.root, FC#13, port D2
Entries 390
Mean 43.71
Std Dev 11.93
Turn on : 25.1615
Width : 3.245
Height : 10.007
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

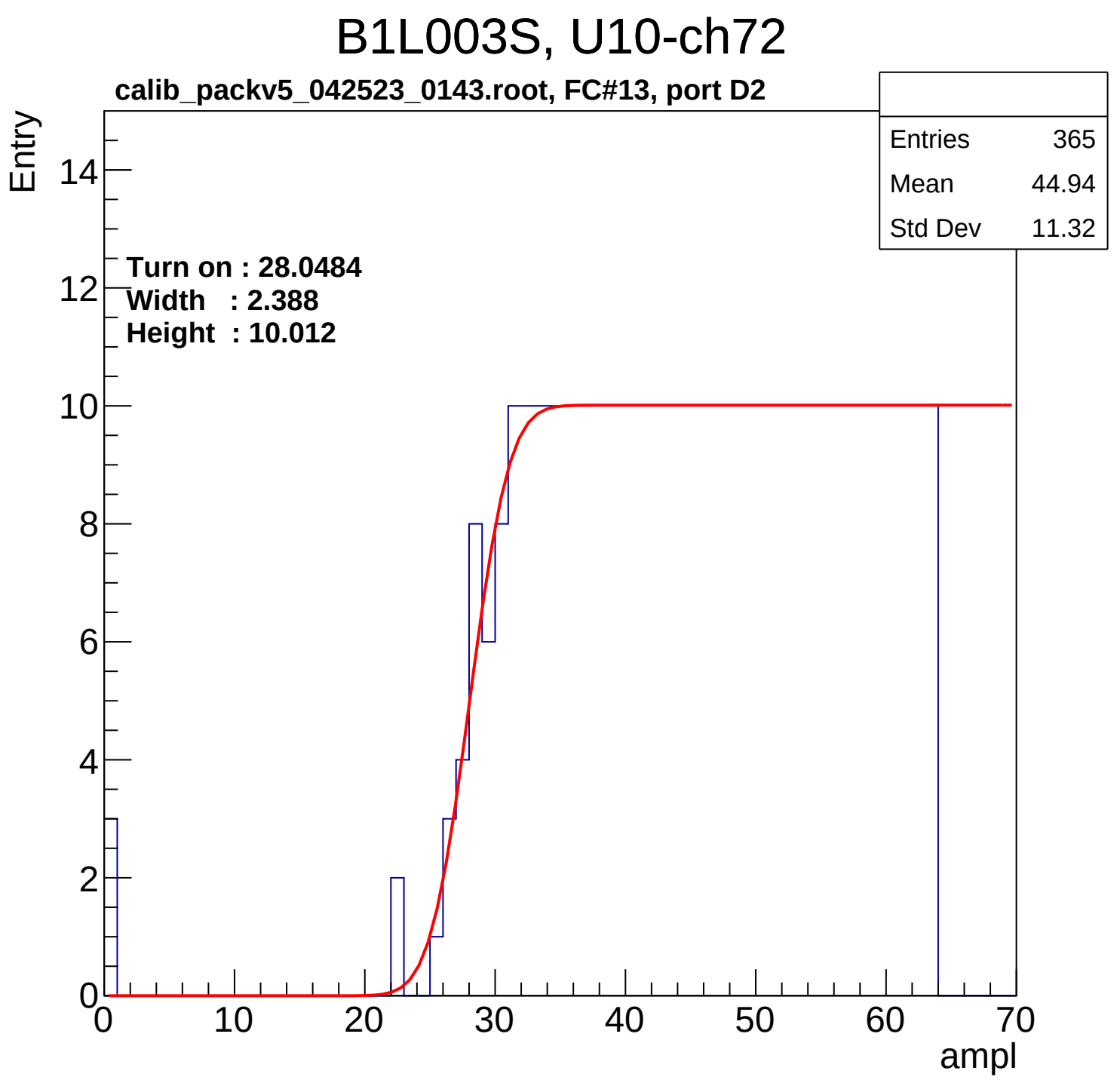

B1L003S, U10-ch67
calib_packv5_042523_0143.root, FC#13, port D2
Entries 370
Mean 44.69
Std Dev 11.44
Turn on : 27.2679
Width : 2.805
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

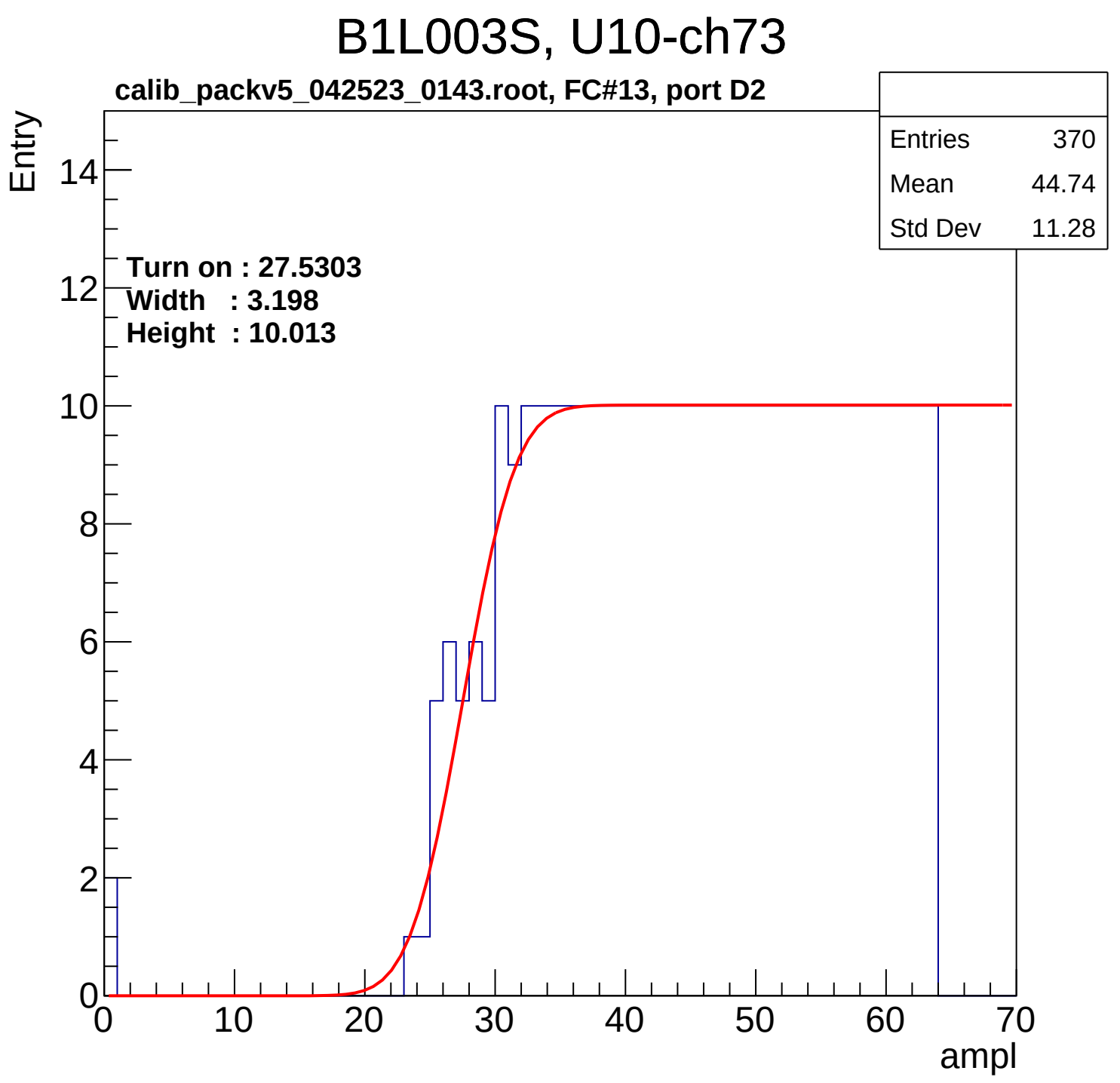

B1L003S, U10-ch68
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.29
Std Dev 11.95
Turn on : 26.5412
Width : 3.197
Height : 9.959
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

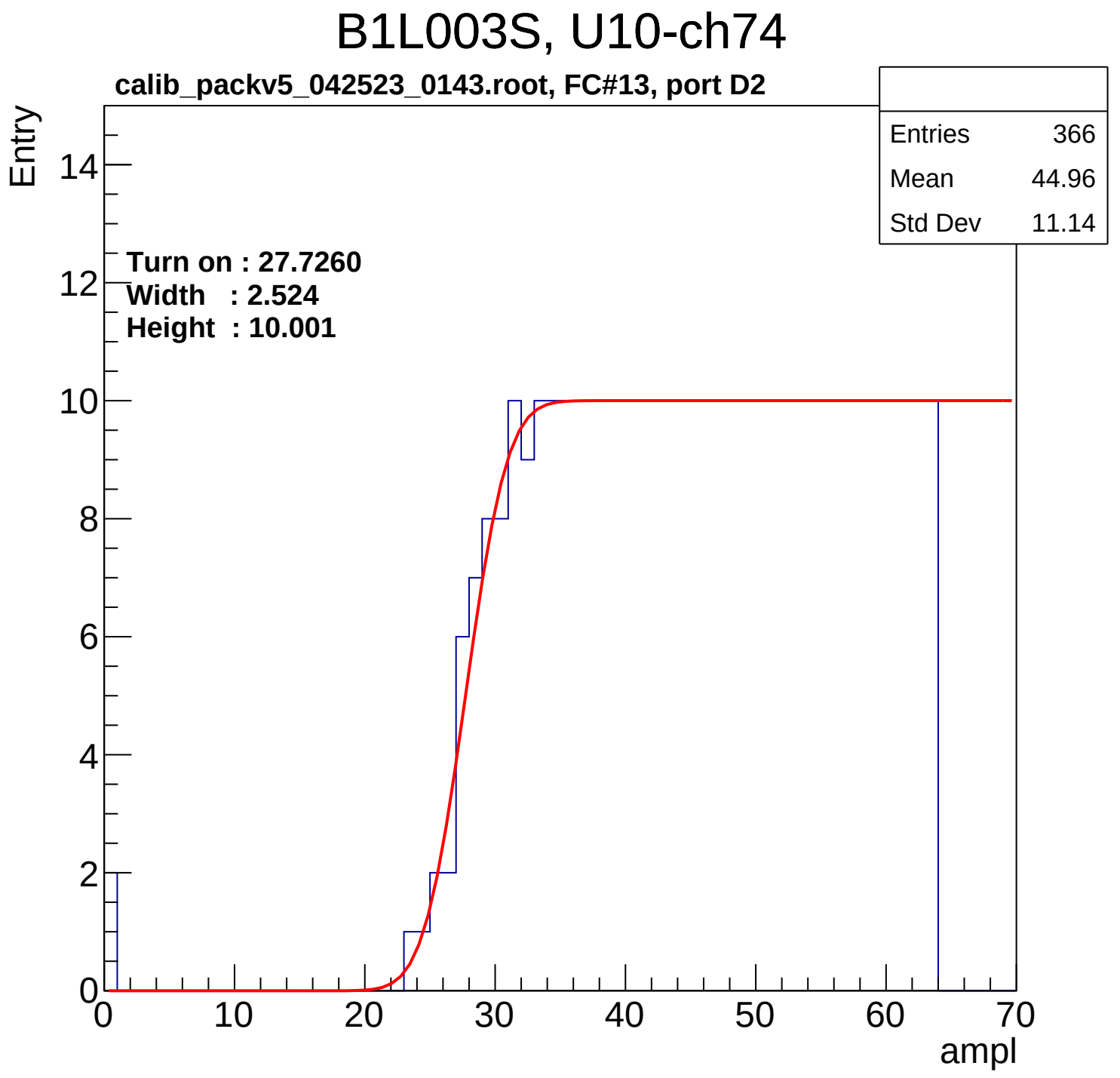

B1L003S, U10-ch69
calib_packv5_042523_0143.root, FC#13, port D2
Entries 364
Mean 45.11
Std Dev 10.92
Turn on : 28.4773
Width : 3.223
Height : 10.086
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

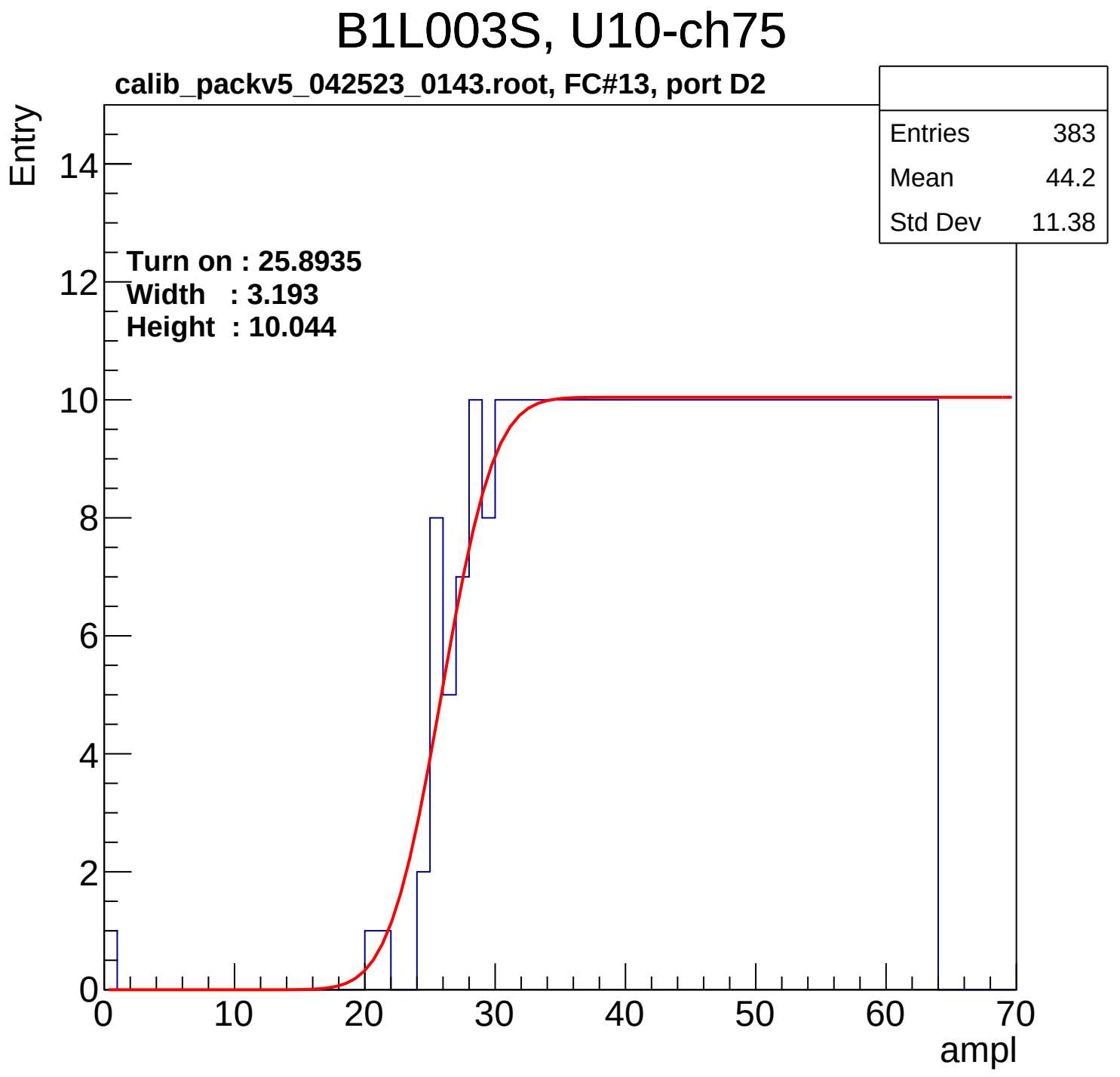

B1L003S, U10-ch70
calib_packv5_042523_0143.root, FC#13, port D2
Entries 378
Mean 44.37
Std Dev 11.44
Turn on : 26.0926
Width : 2.606
Height : 9.957
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

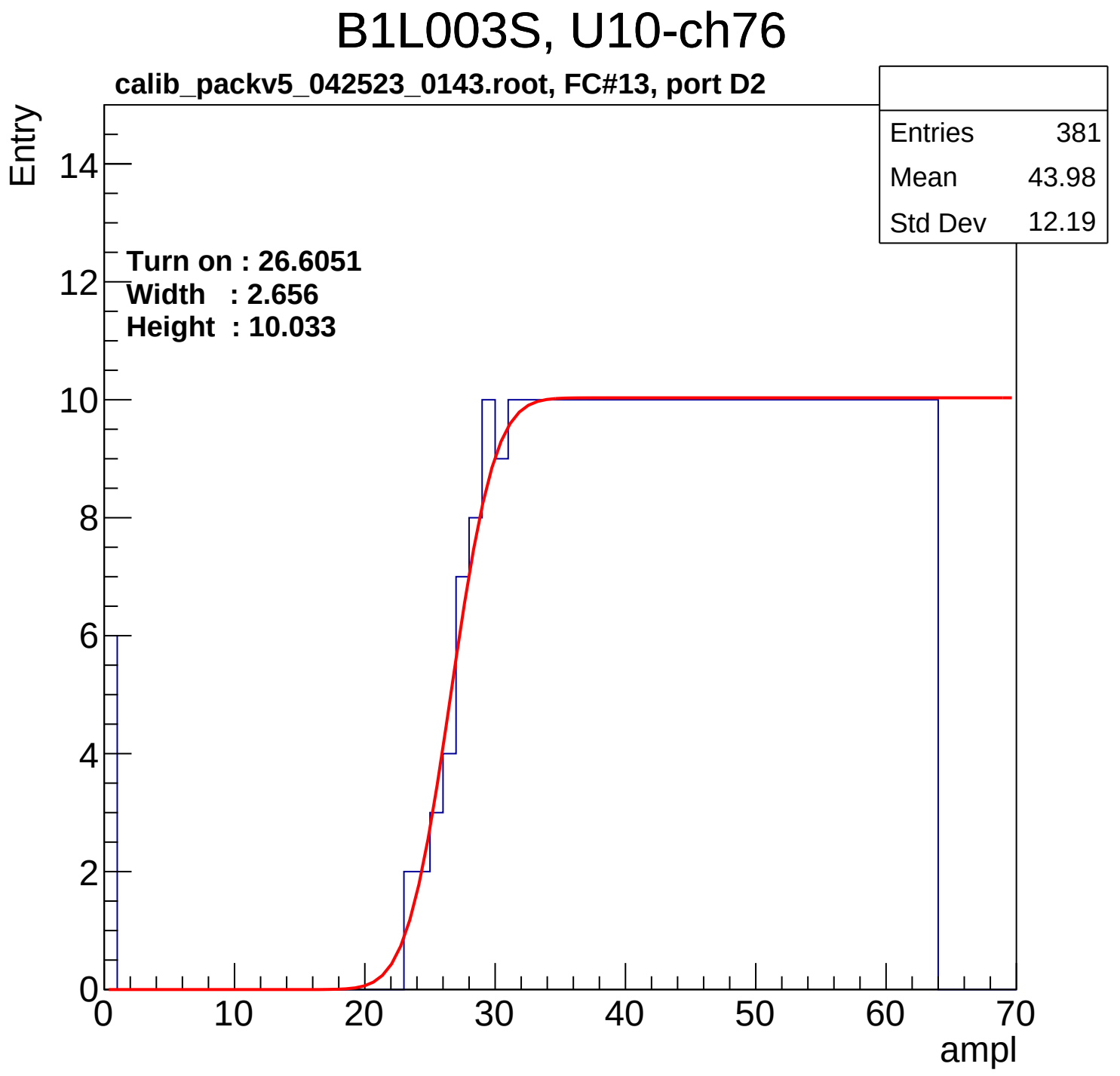

B1L003S, U10-ch71
calib_packv5_042523_0143.root, FC#13, port D2
Entries 383
Mean 44.14
Std Dev 11.48
Turn on : 26.1523
Width : 3.606
Height : 10.061
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

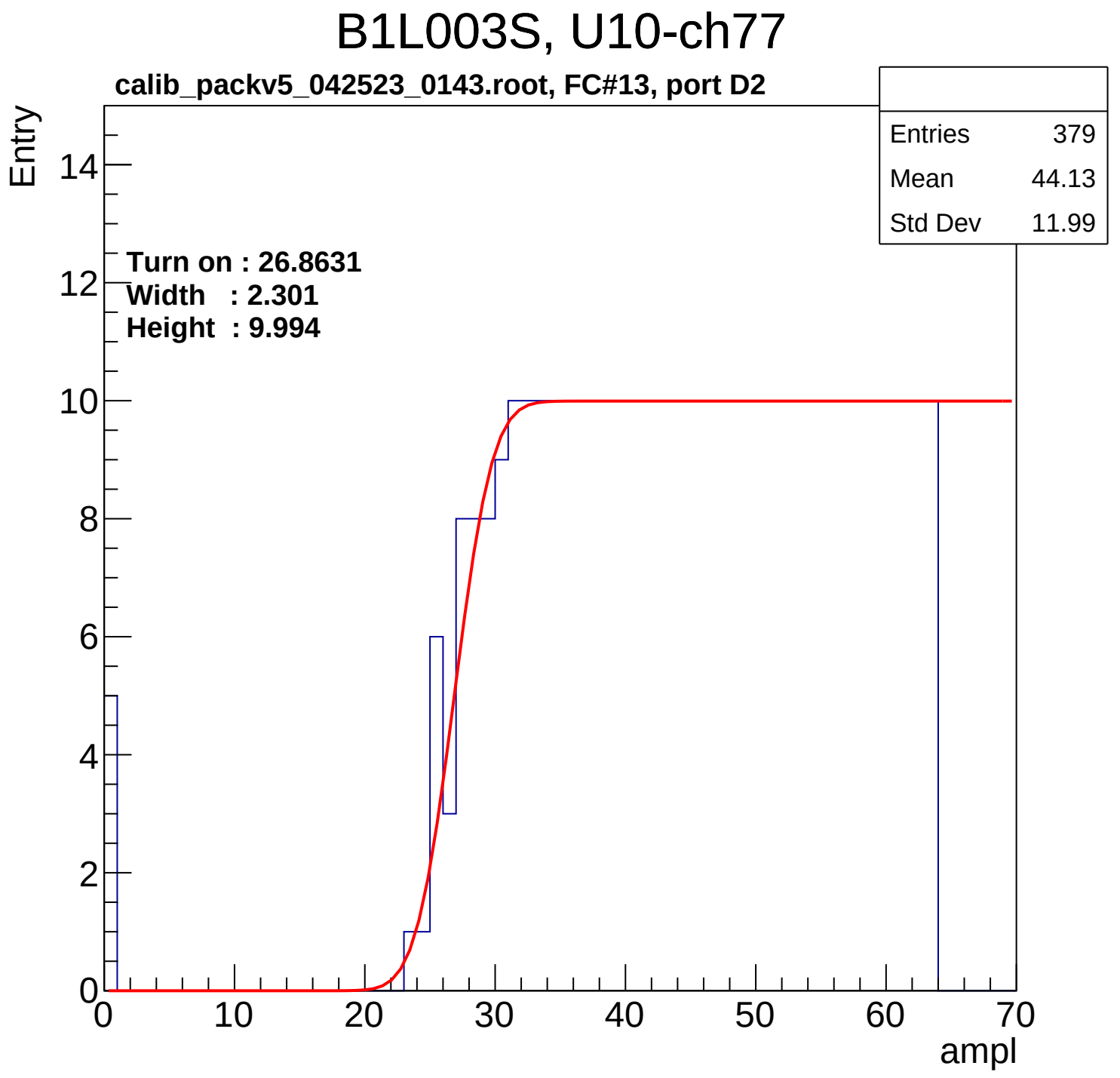

B1L003S, U10-ch72
calib_packv5_042523_0143.root, FC#13, port D2
Entries 365
Mean 44.94
Std Dev 11.32
Turn on : 28.0484
Width : 2.388
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

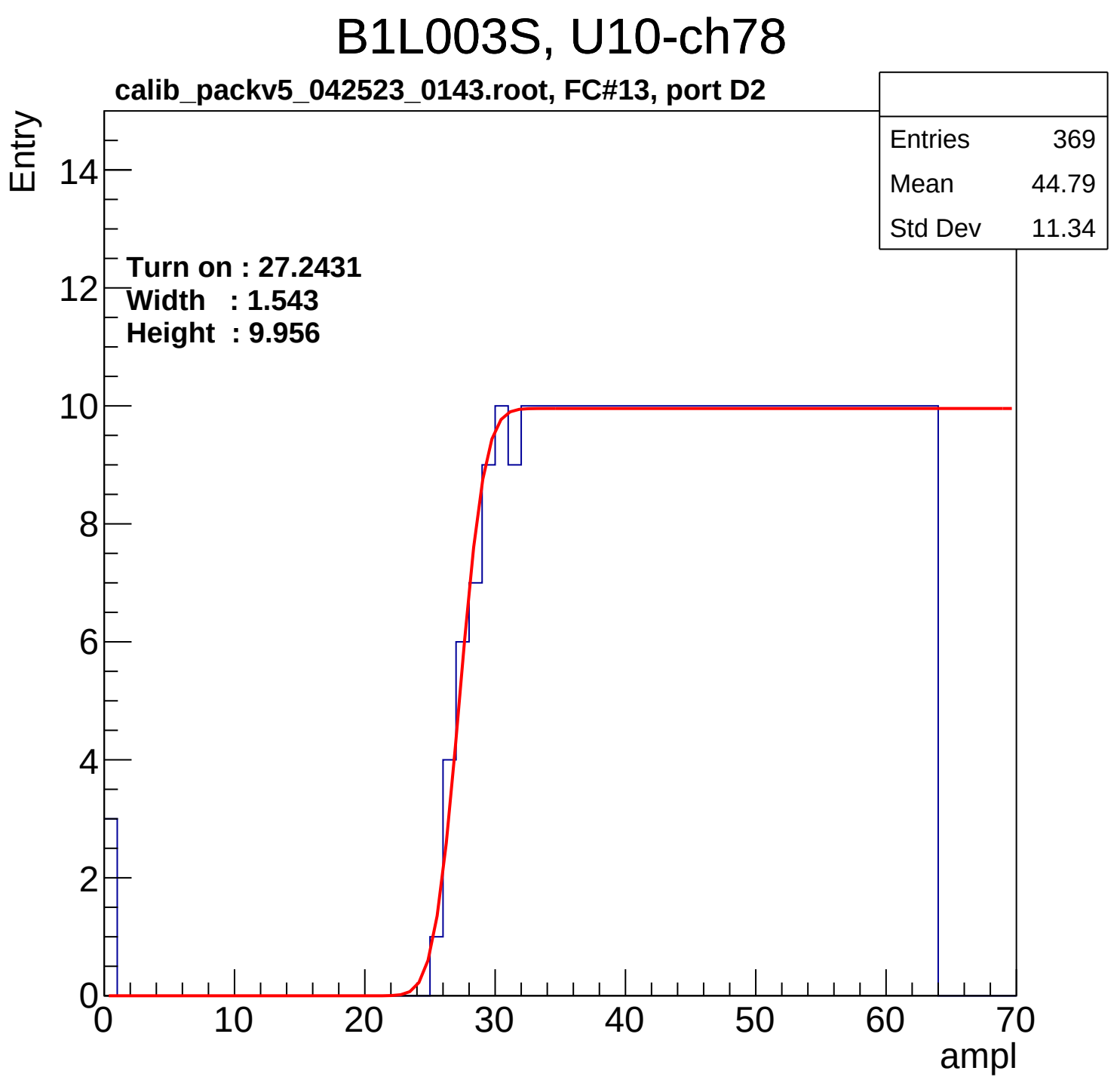

B1L003S, U10-ch73
calib_packv5_042523_0143.root, FC#13, port D2
Entries 370
Mean 44.74
Std Dev 11.28
Turn on : 27.5303
Width : 3.198
Height : 10.013
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

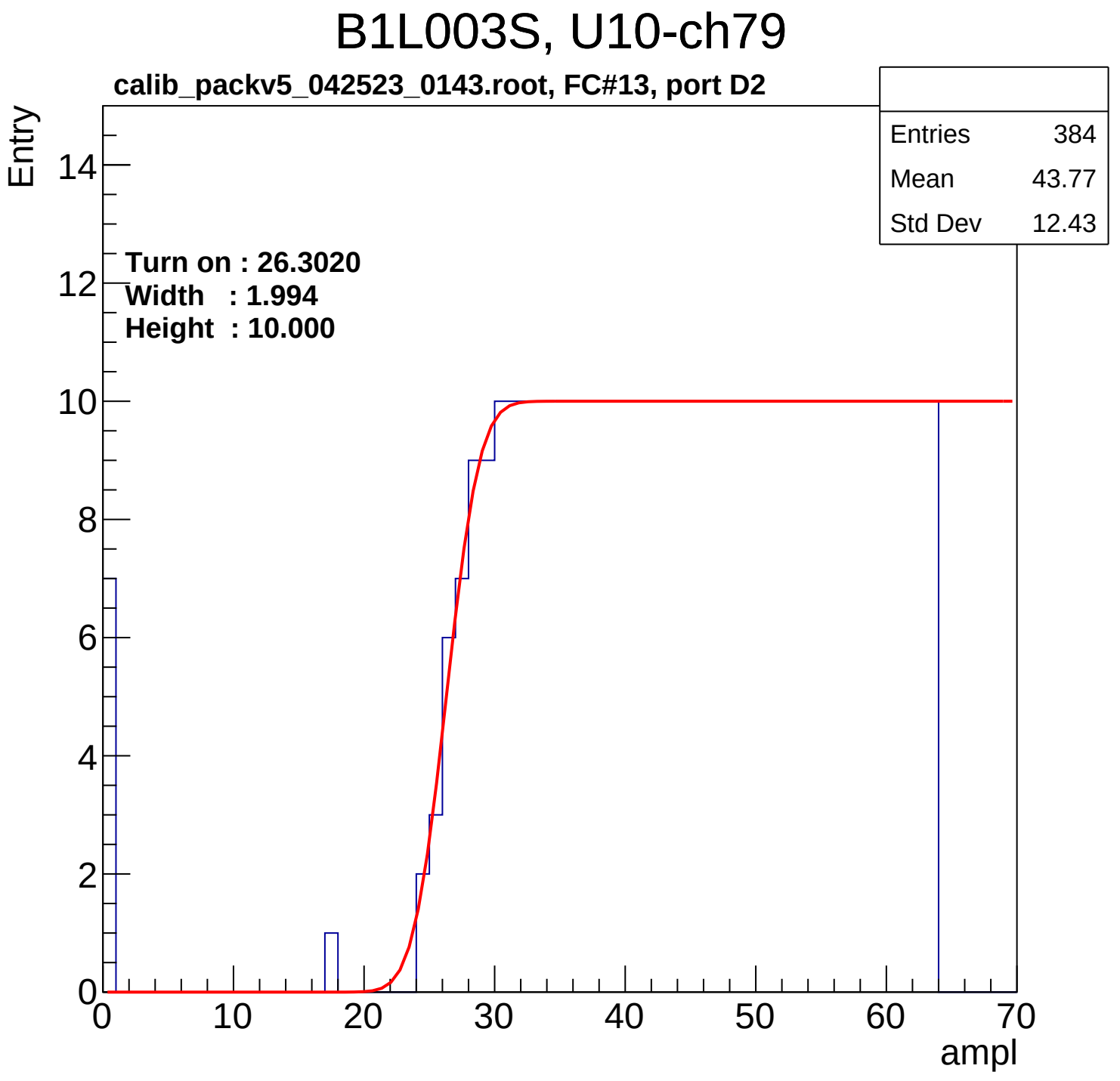

B1L003S, U10-ch74
calib_packv5_042523_0143.root, FC#13, port D2
Entries 366
Mean 44.96
Std Dev 11.14
Turn on : 27.7260
Width : 2.524
Height : 10.001
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

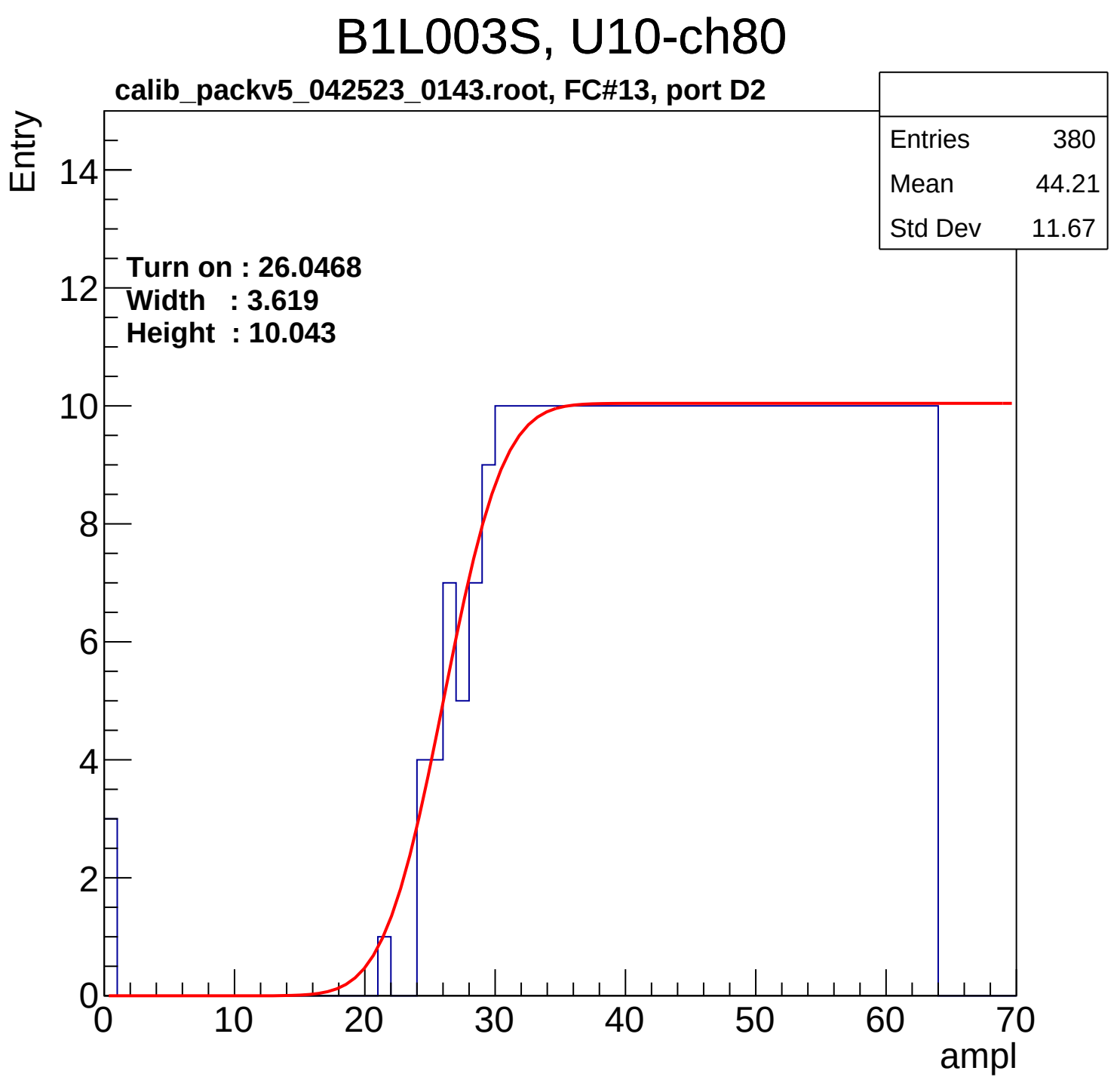

B1L003S, U10-ch75
calib_packv5_042523_0143.root, FC#13, port D2
Entries 383
Mean 44.2
Std Dev 11.38
Turn on : 25.8935
Width : 3.193
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

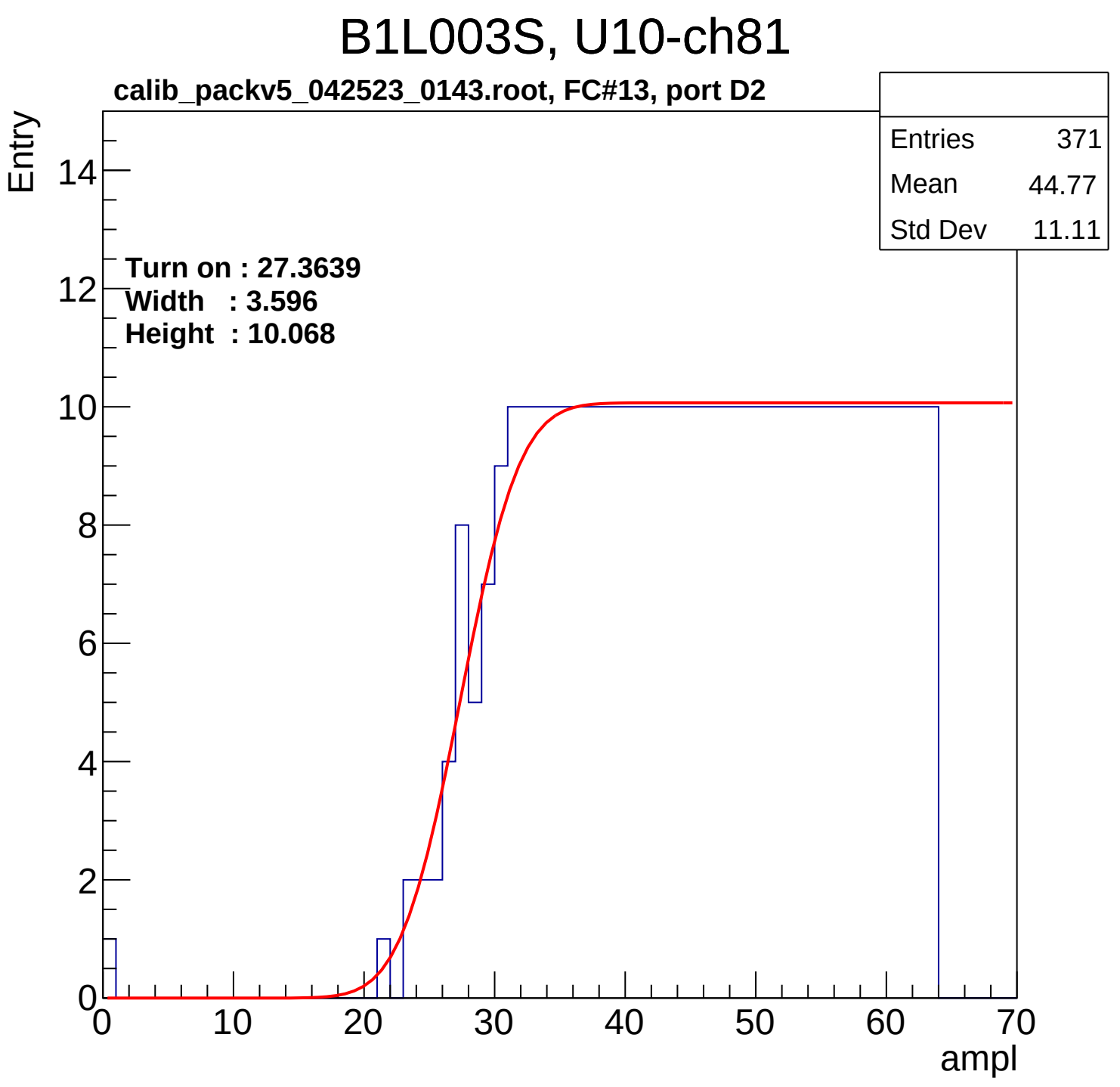

B1L003S, U10-ch76
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 43.98
Std Dev 12.19
Turn on : 26.6051
Width : 2.656
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

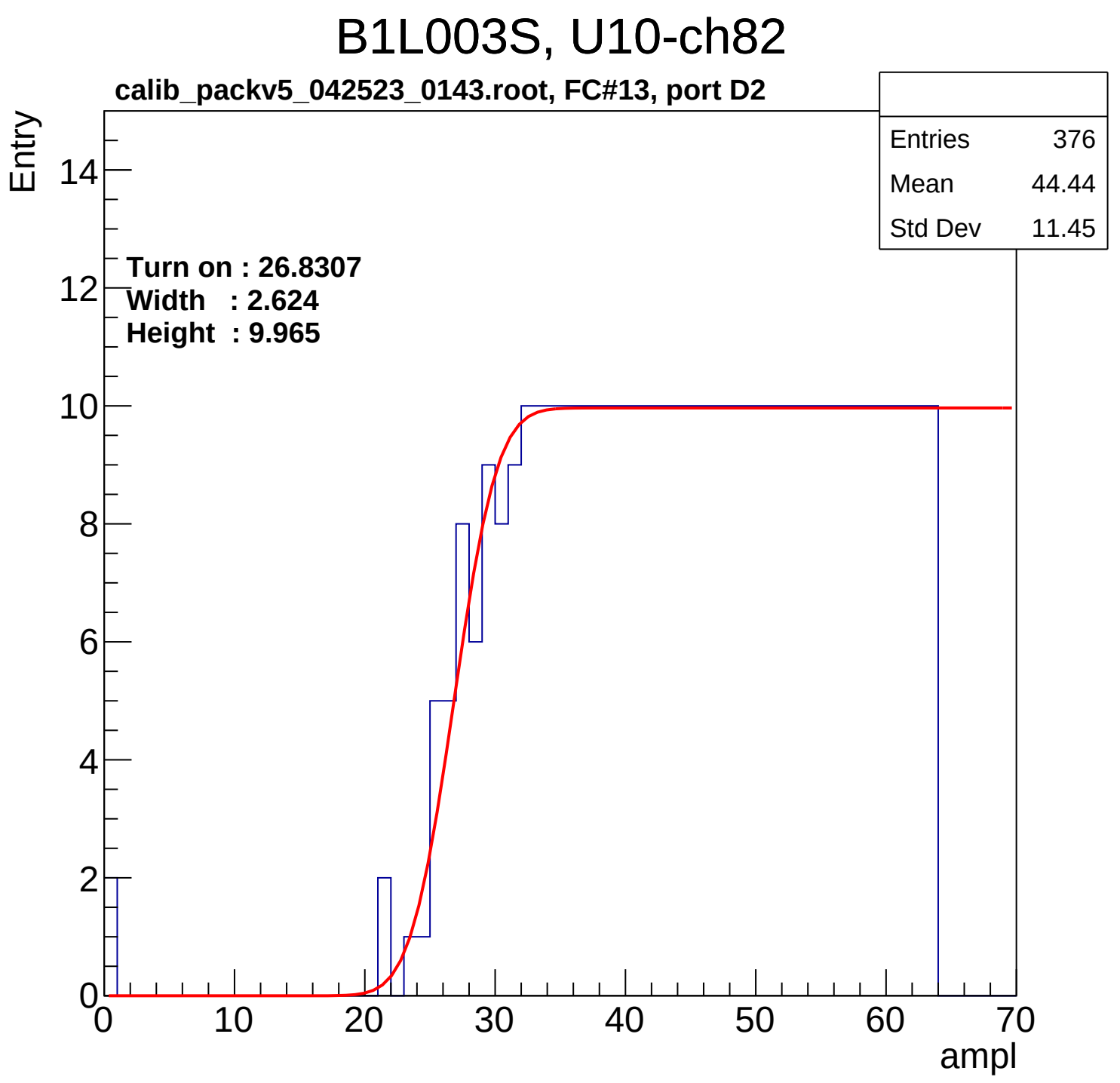

B1L003S, U10-ch77
calib_packv5_042523_0143.root, FC#13, port D2
Entries 379
Mean 44.13
Std Dev 11.99
Turn on : 26.8631
Width : 2.301
Height : 9.994
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

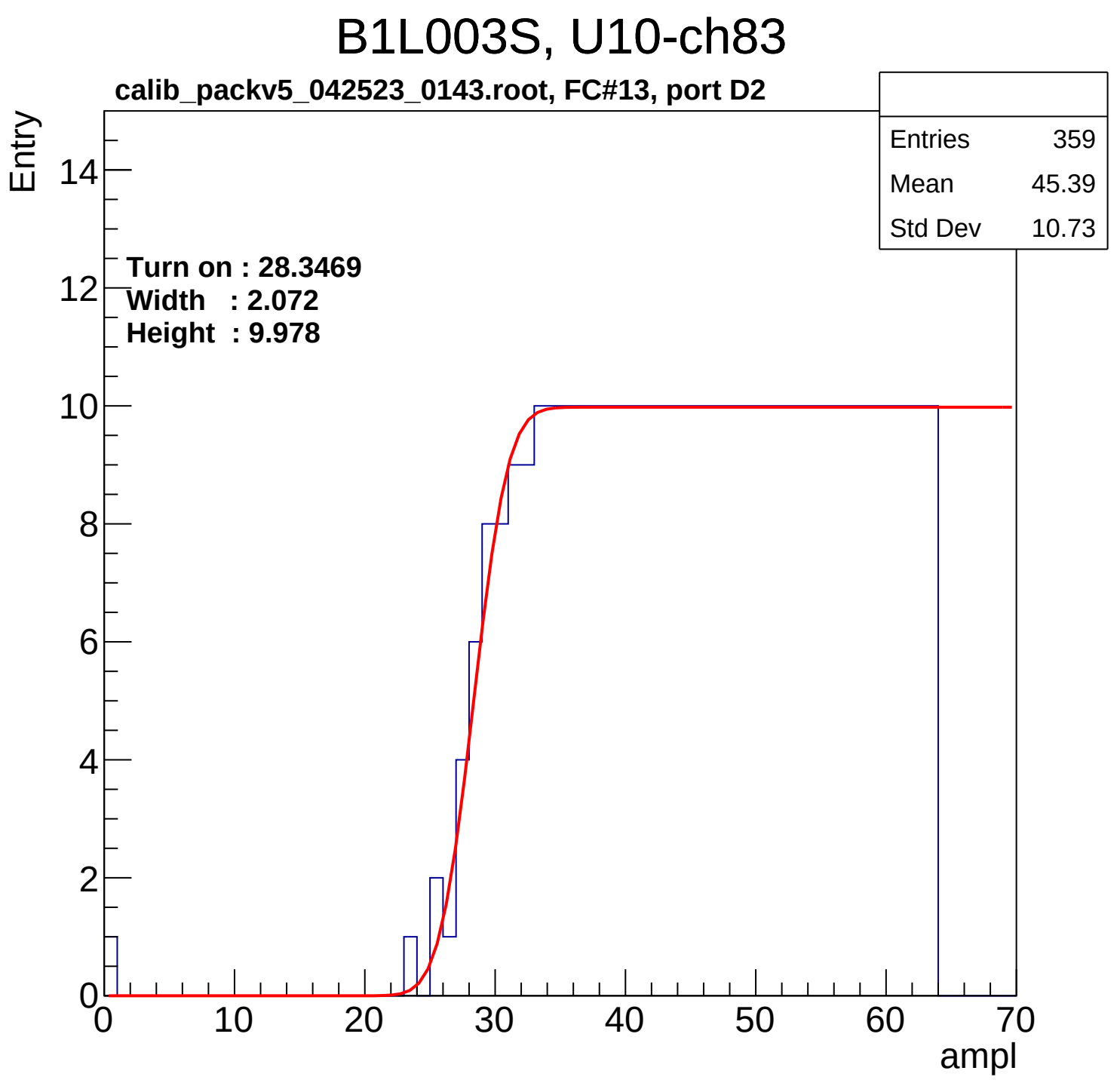

B1L003S, U10-ch78
calib_packv5_042523_0143.root, FC#13, port D2
Entries 369
Mean 44.79
Std Dev 11.34
Turn on : 27.2431
Width : 1.543
Height : 9.956
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

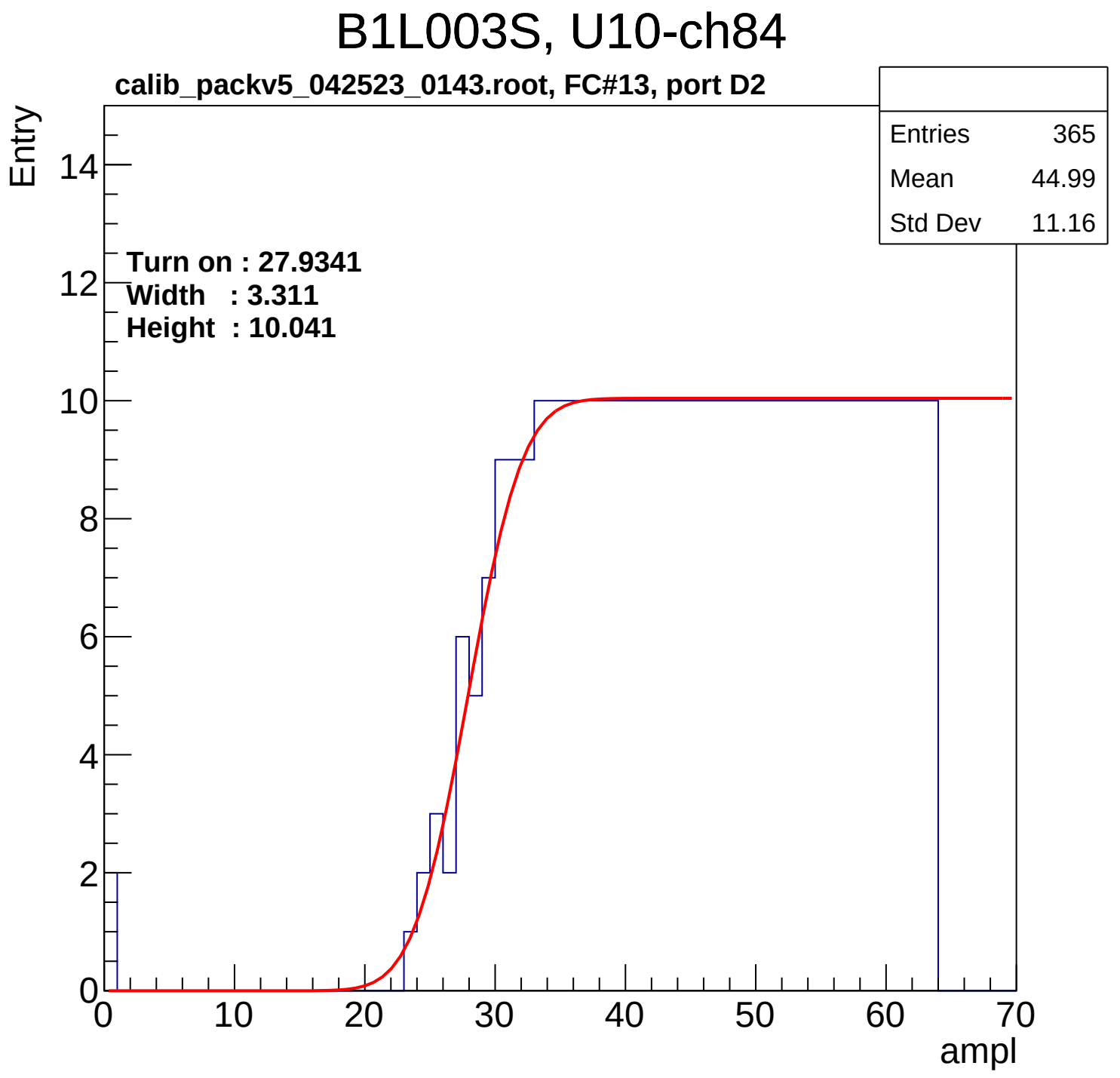

B1L003S, U10-ch79
calib_packv5_042523_0143.root, FC#13, port D2
Entries 384
Mean 43.77
Std Dev 12.43
Turn on : 26.3020
Width : 1.994
Height : 10.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

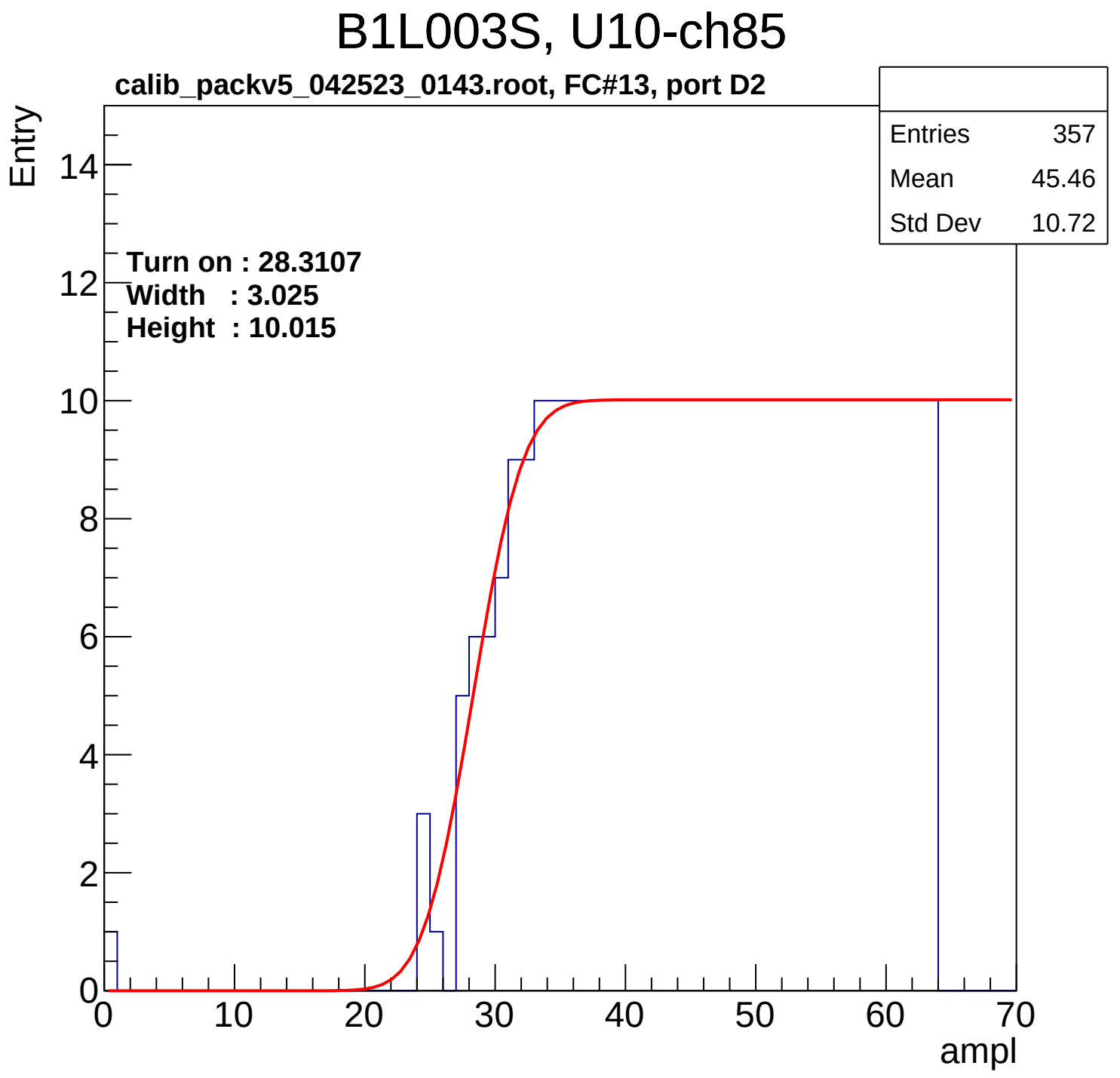

B1L003S, U10-ch80
calib_packv5_042523_0143.root, FC#13, port D2
Entries 380
Mean 44.21
Std Dev 11.67
Turn on : 26.0468
Width : 3.619
Height : 10.043
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

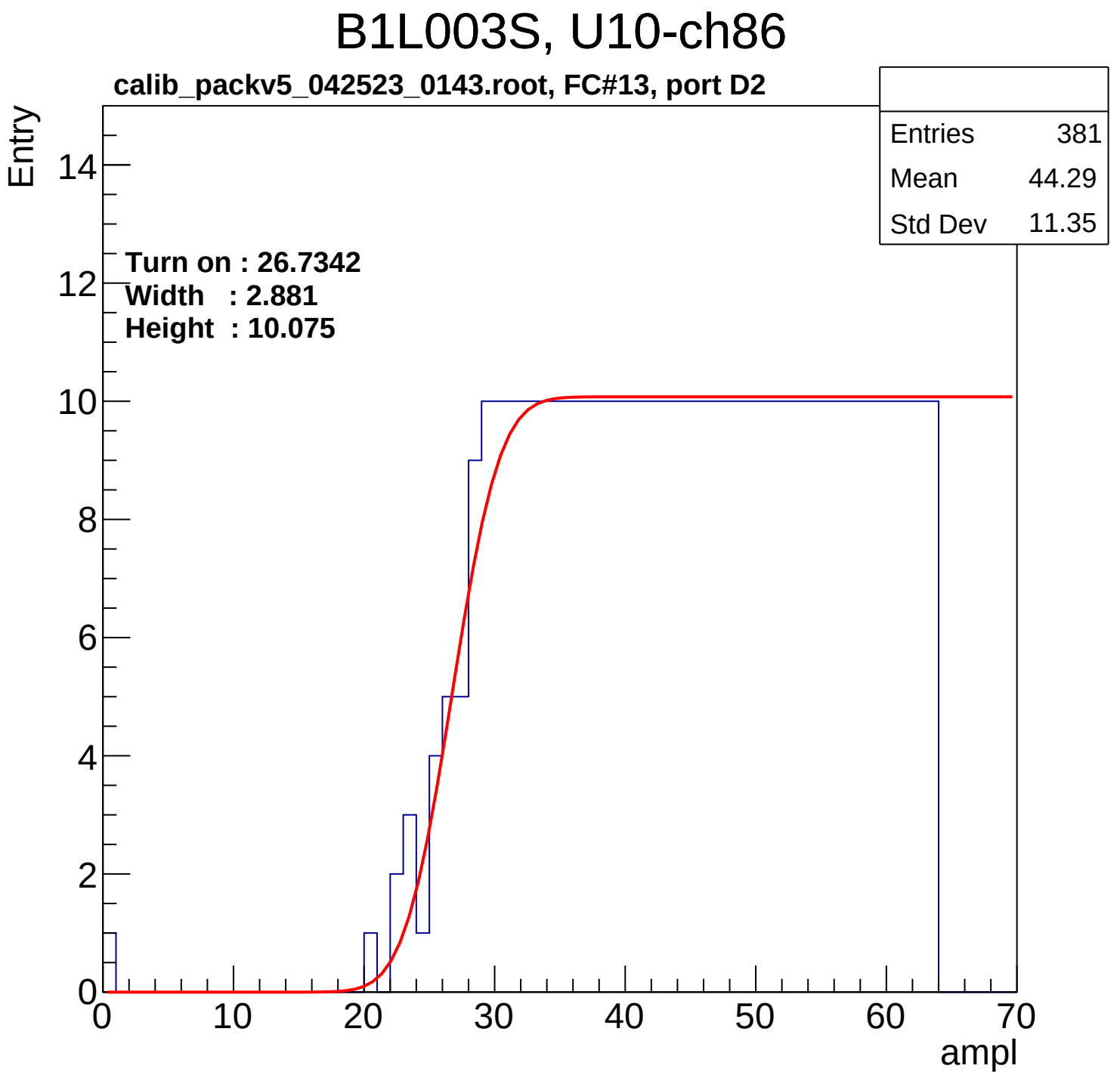

B1L003S, U10-ch81
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.77
Std Dev 11.11
Turn on : 27.3639
Width : 3.596
Height : 10.068
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

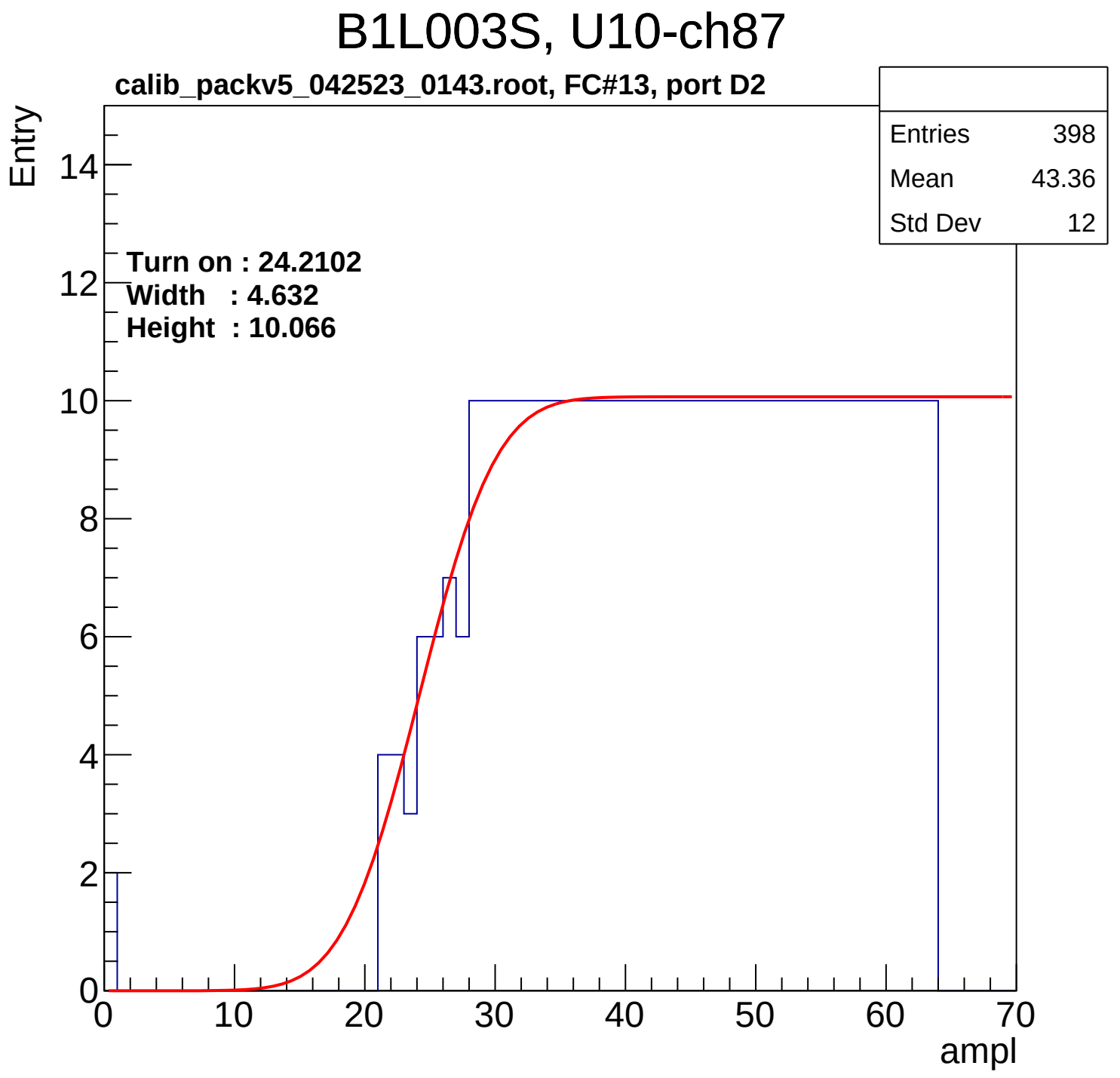

B1L003S, U10-ch82
calib_packv5_042523_0143.root, FC#13, port D2
Entries 376
Mean 44.44
Std Dev 11.45
Turn on : 26.8307
Width : 2.624
Height : 9.965
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

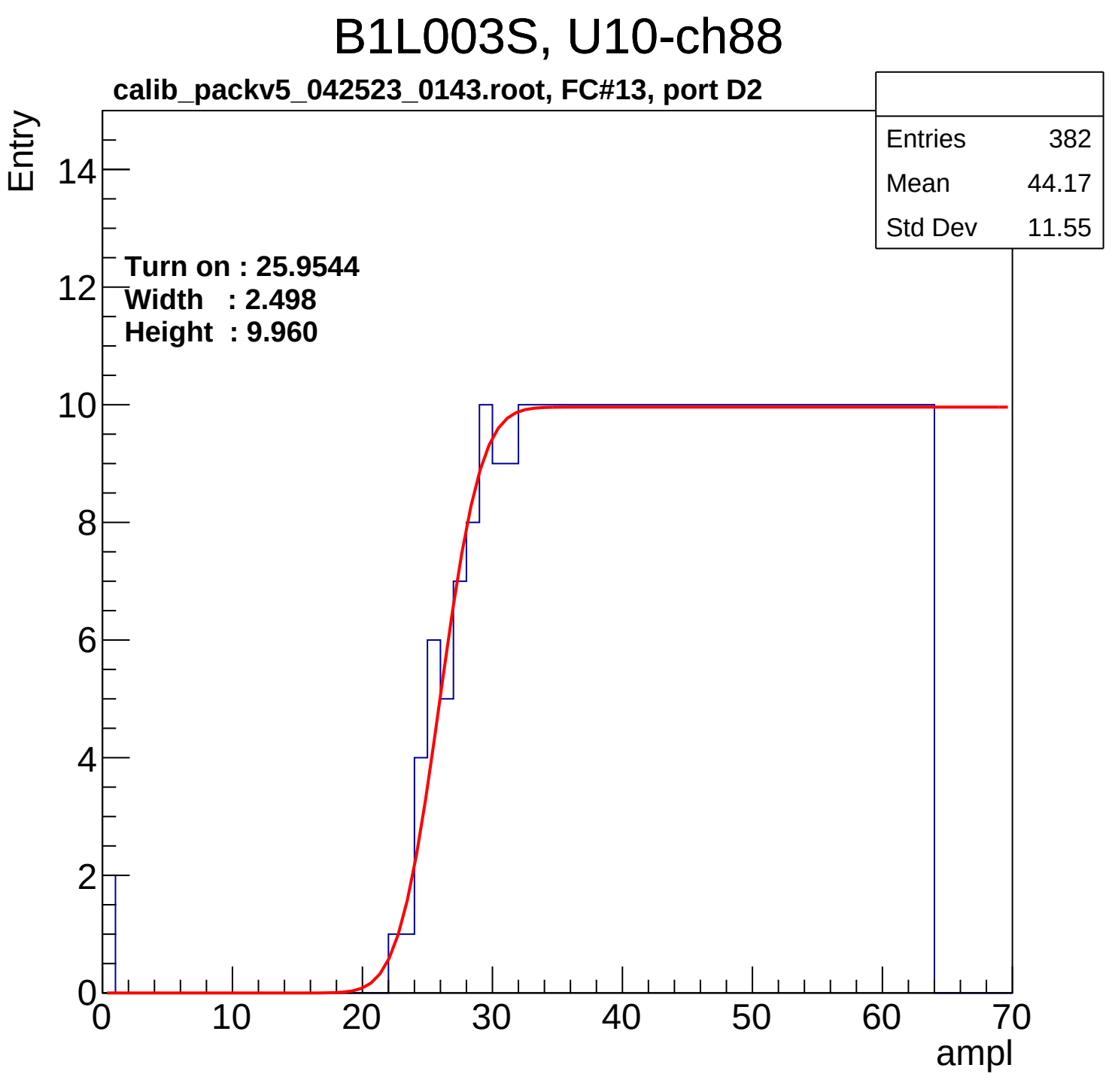

B1L003S, U10-ch83
calib_packv5_042523_0143.root, FC#13, port D2
Entries 359
Mean 45.39
Std Dev 10.73
Turn on : 28.3469
Width : 2.072
Height : 9.978
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

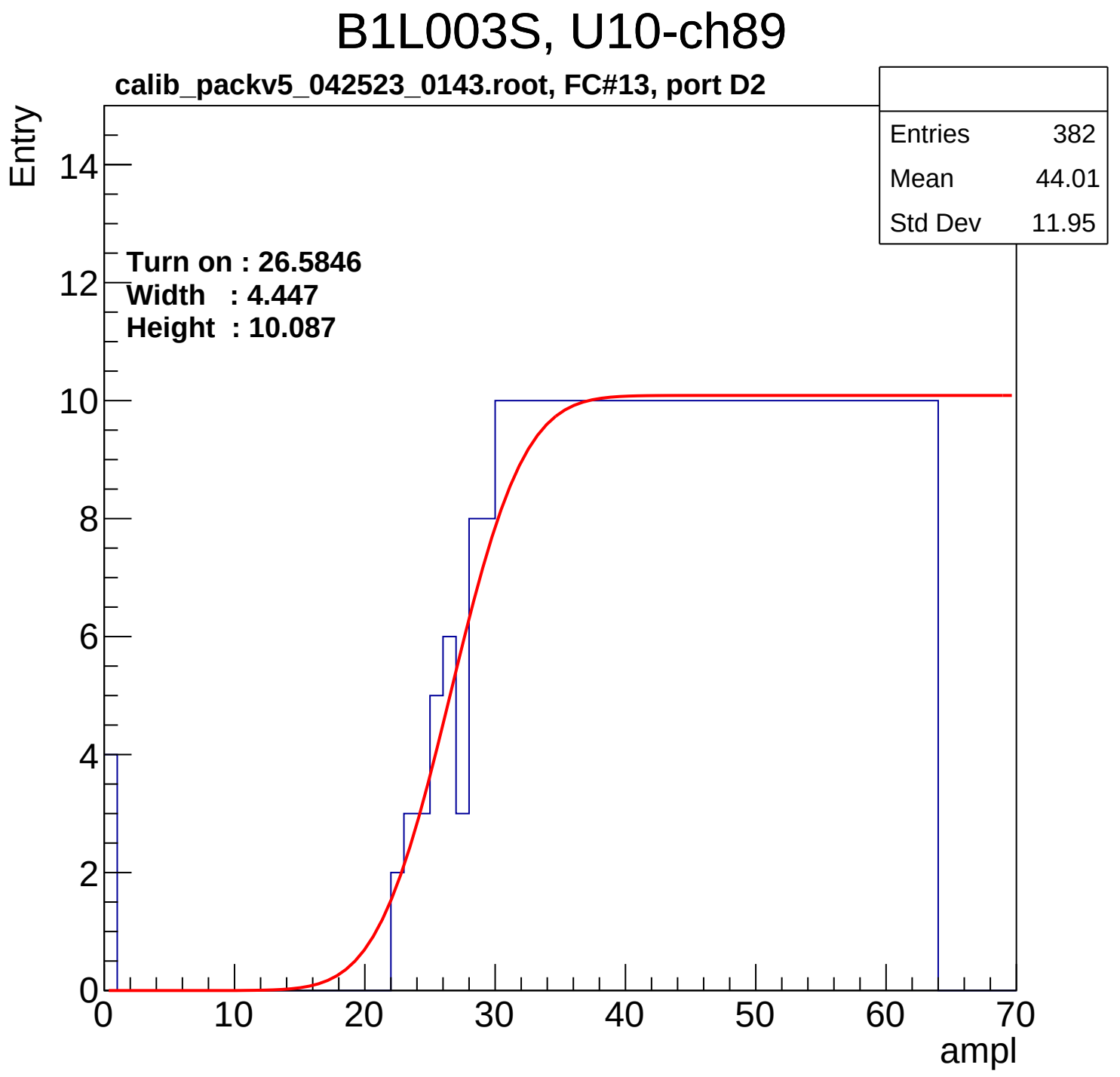

B1L003S, U10-ch84
calib_packv5_042523_0143.root, FC#13, port D2
Entries 365
Mean 44.99
Std Dev 11.16
Turn on : 27.9341
Width : 3.311
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

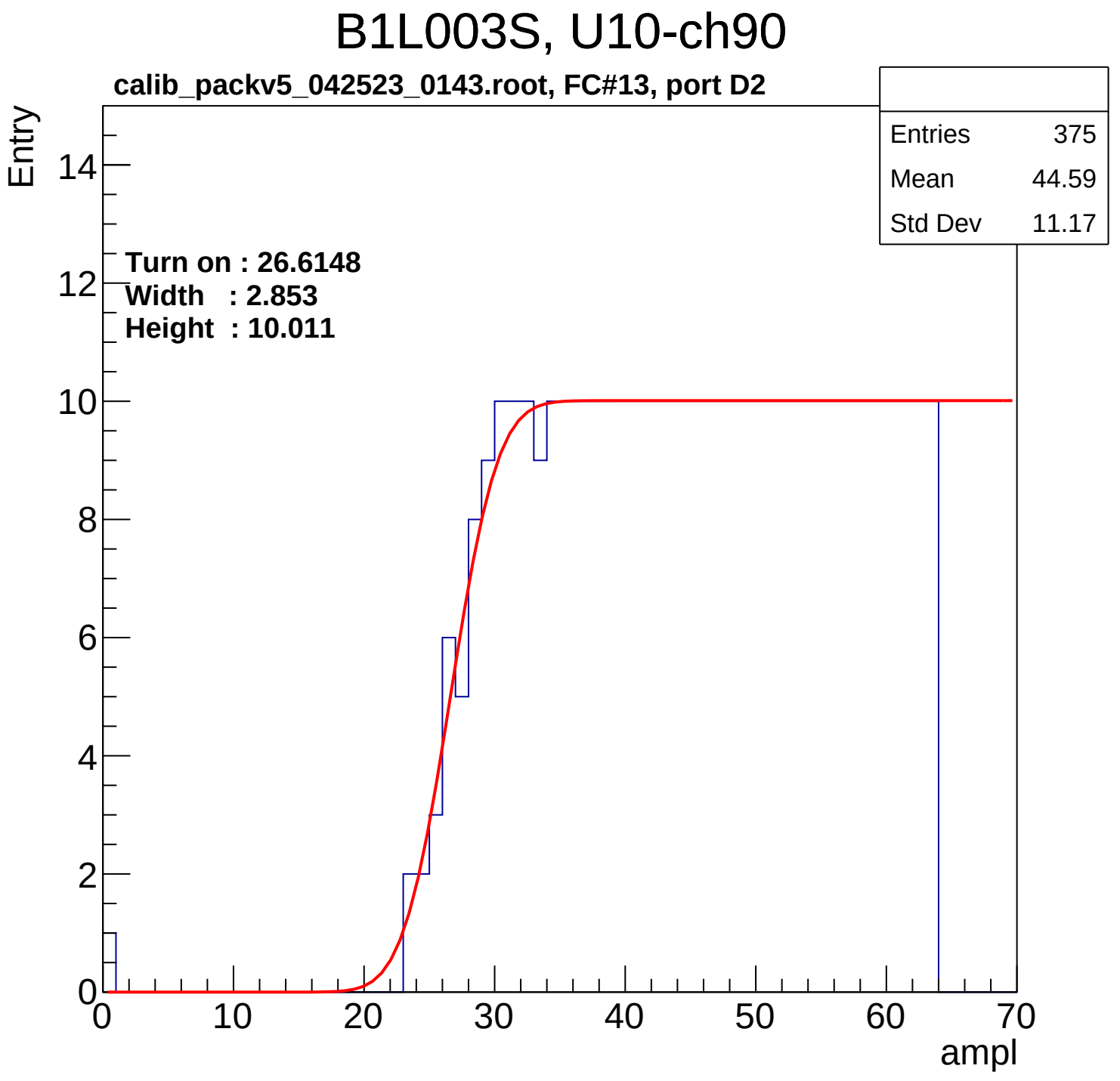

B1L003S, U10-ch85
calib_packv5_042523_0143.root, FC#13, port D2
Entries 357
Mean 45.46
Std Dev 10.72
Turn on : 28.3107
Width : 3.025
Height : 10.015
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

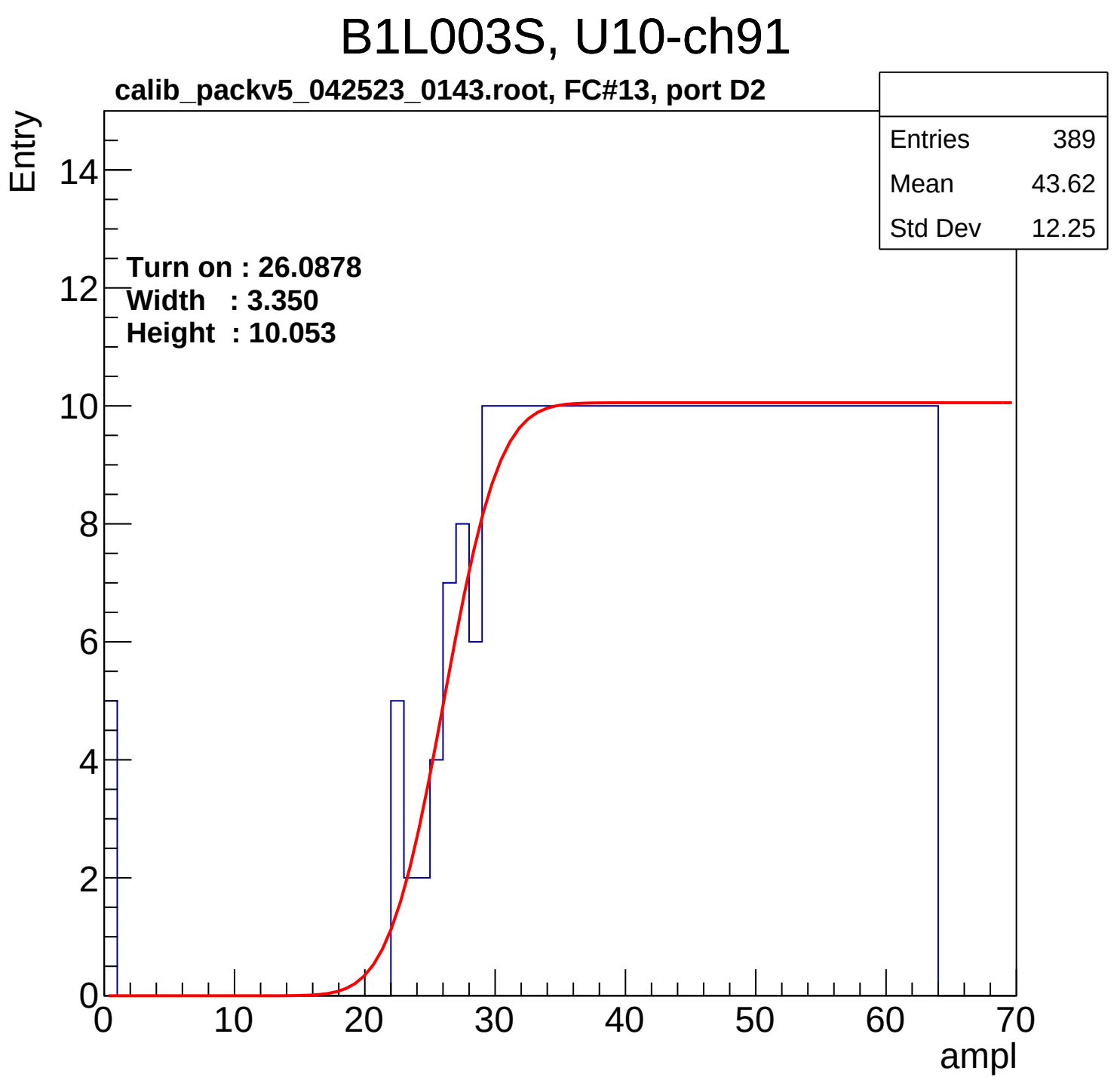

B1L003S, U10-ch86
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 44.29
Std Dev 11.35
Turn on : 26.7342
Width : 2.881
Height : 10.075
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

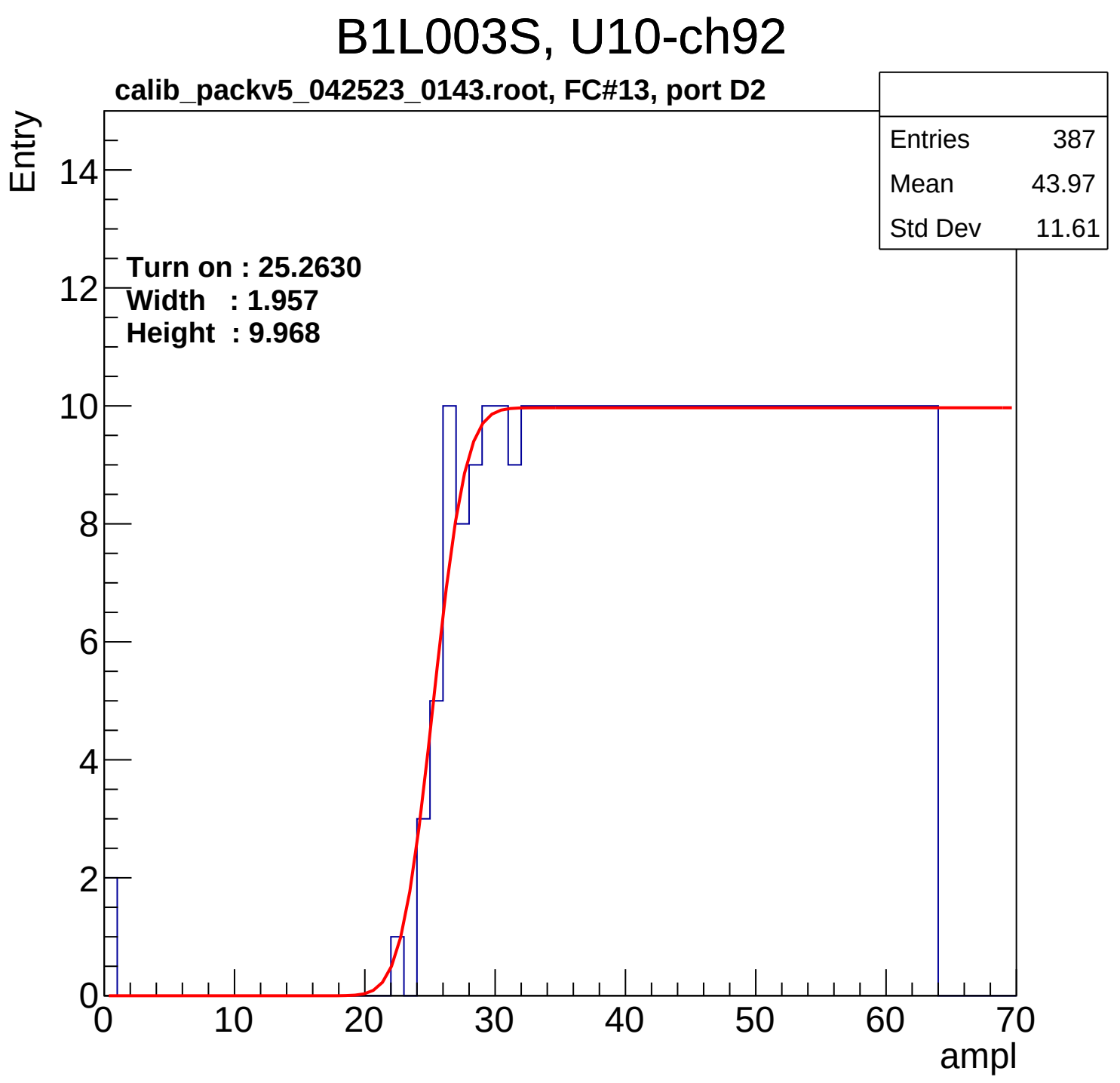

B1L003S, U10-ch87
calib_packv5_042523_0143.root, FC#13, port D2
Entries 398
Mean 43.36
Std Dev 12
Turn on : 24.2102
Width : 4.632
Height : 10.066
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

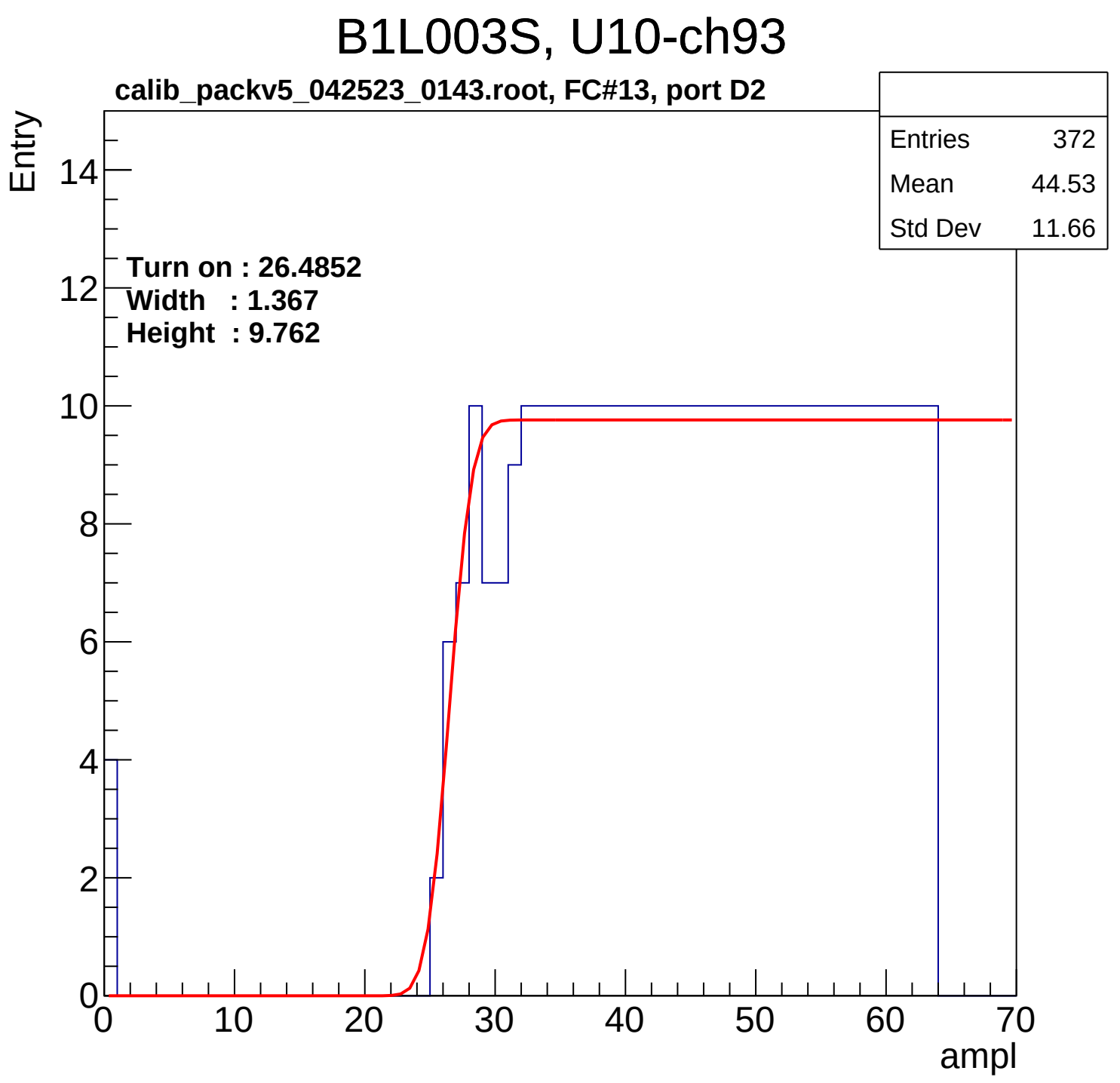

B1L003S, U10-ch88
calib_packv5_042523_0143.root, FC#13, port D2
Entries 382
Mean 44.17
Std Dev 11.55
Turn on : 25.9544
Width : 2.498
Height : 9.960
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

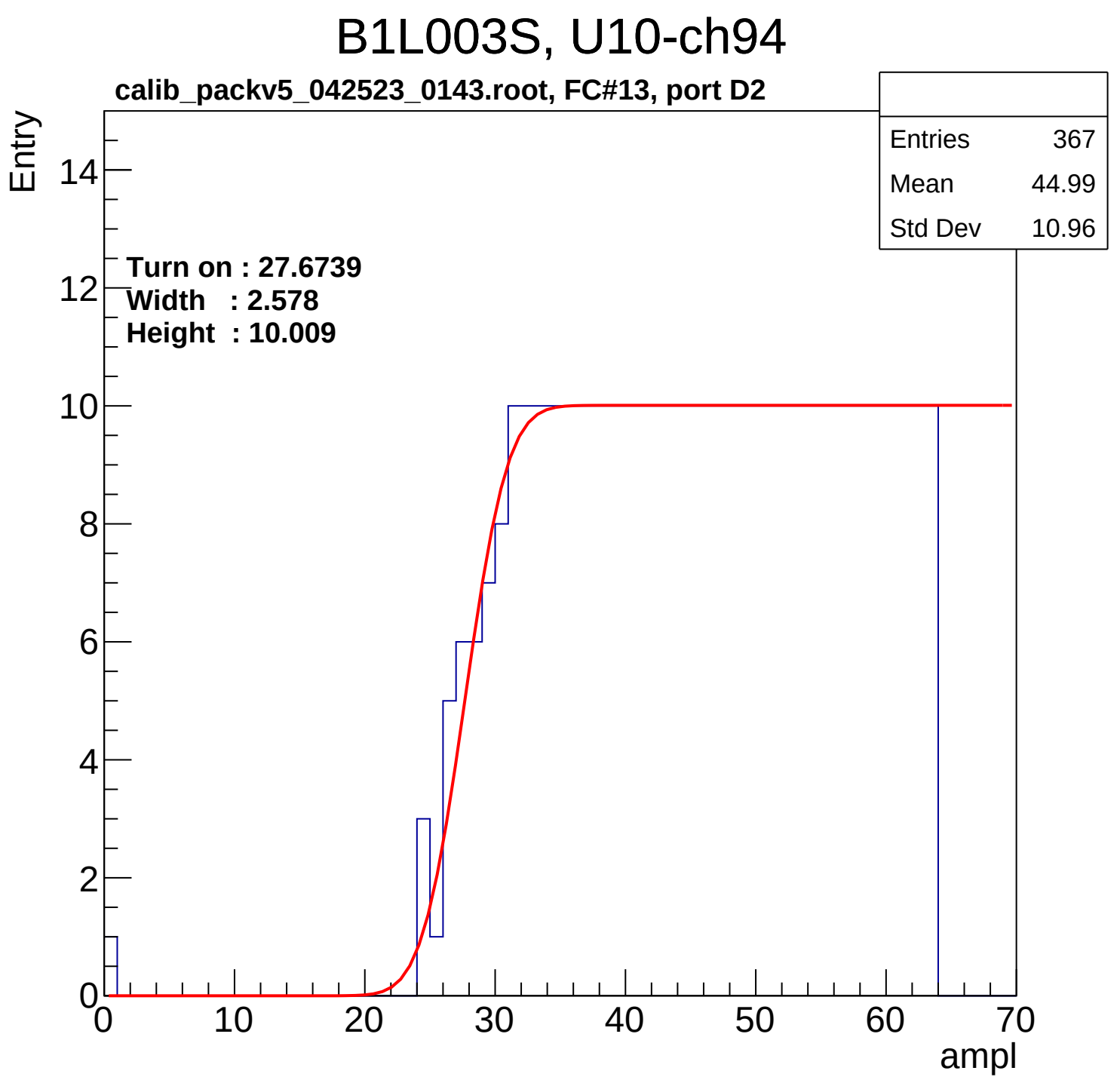

B1L003S, U10-ch89
calib_packv5_042523_0143.root, FC#13, port D2
Entries 382
Mean 44.01
Std Dev 11.95
Turn on : 26.5846
Width : 4.447
Height : 10.087
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

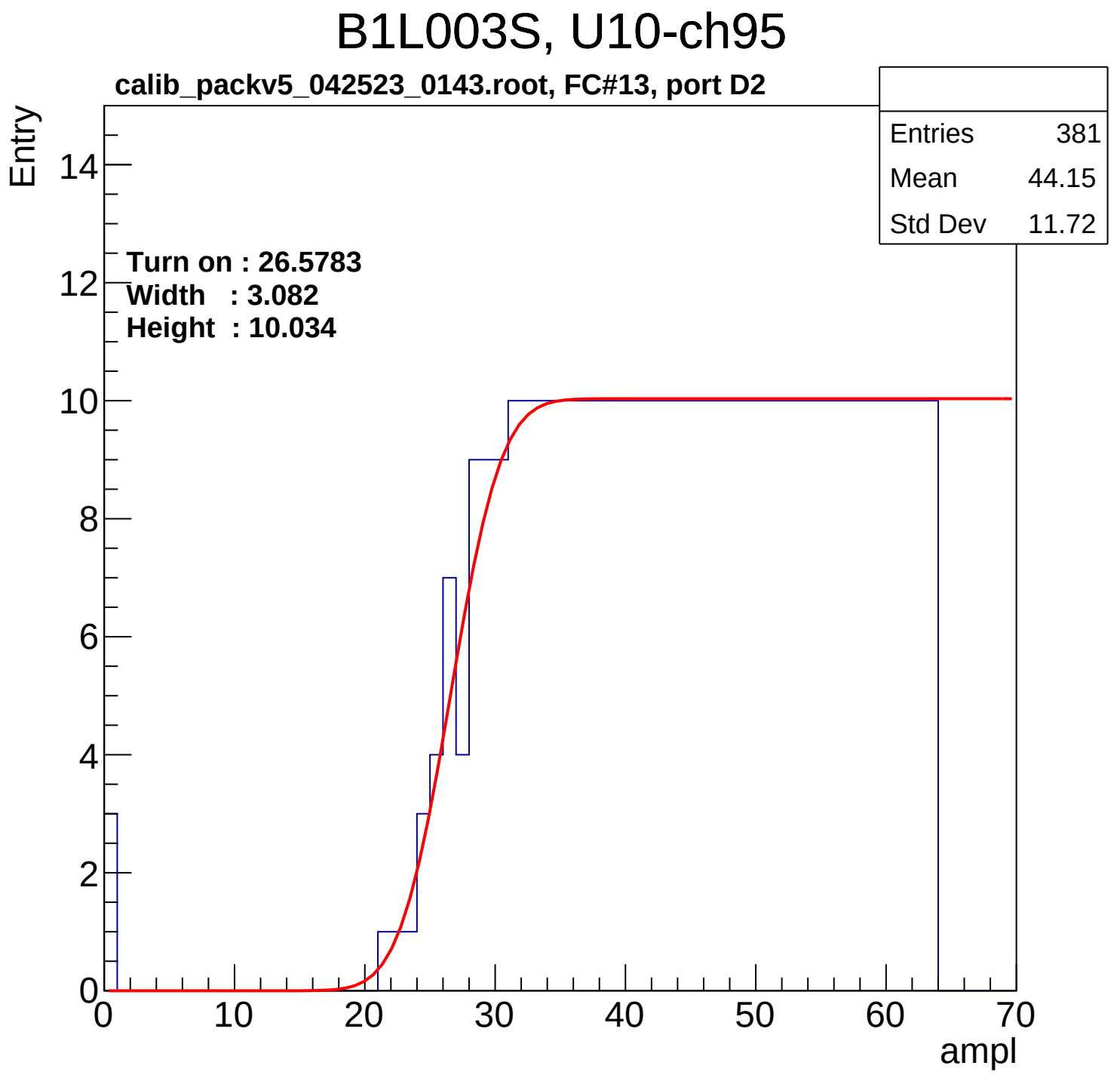

B1L003S, U10-ch90
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.59
Std Dev 11.17
Turn on : 26.6148
Width : 2.853
Height : 10.011
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

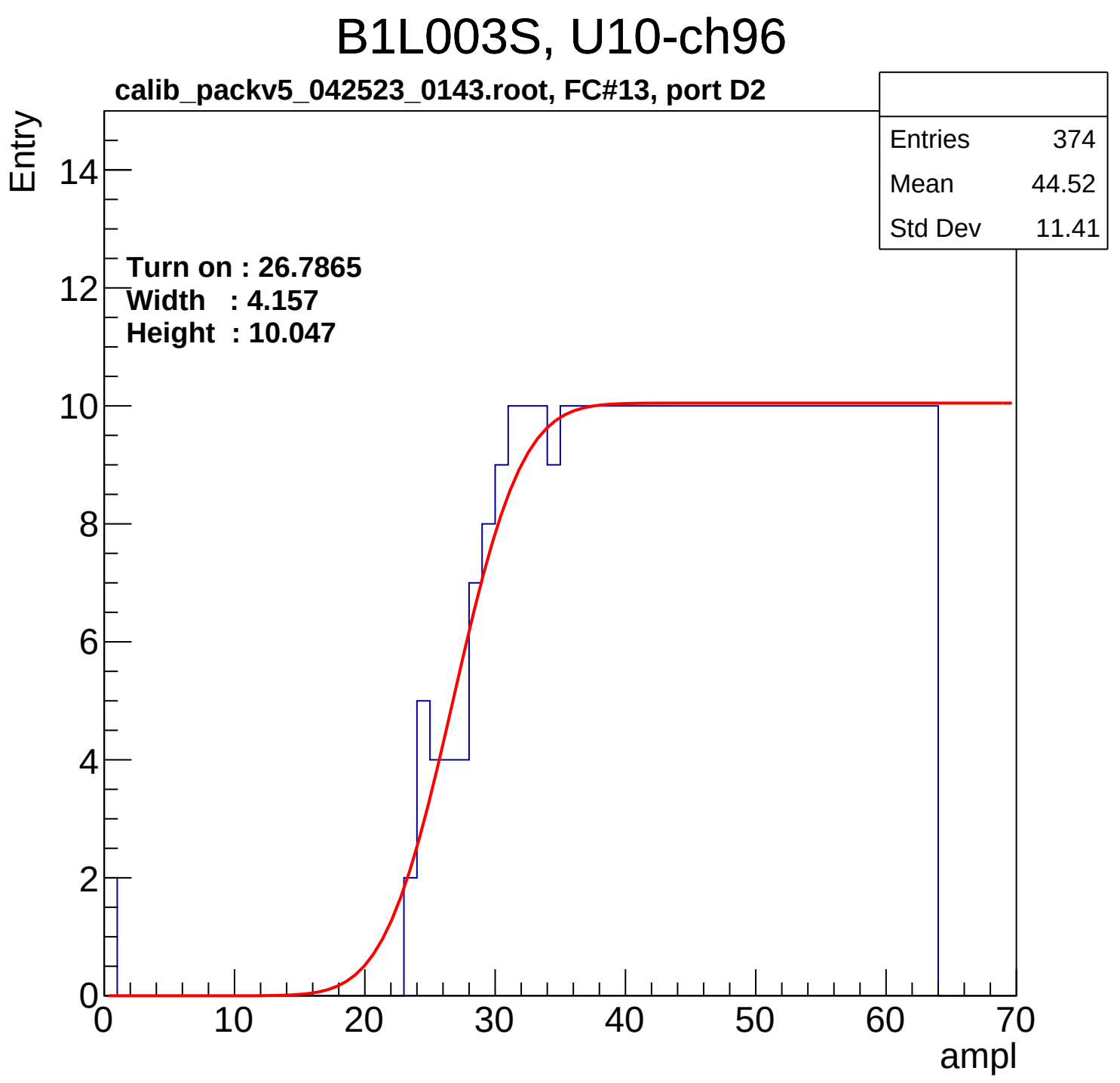

B1L003S, U10-ch91
calib_packv5_042523_0143.root, FC#13, port D2
Entries 389
Mean 43.62
Std Dev 12.25
Turn on : 26.0878
Width : 3.350
Height : 10.053
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

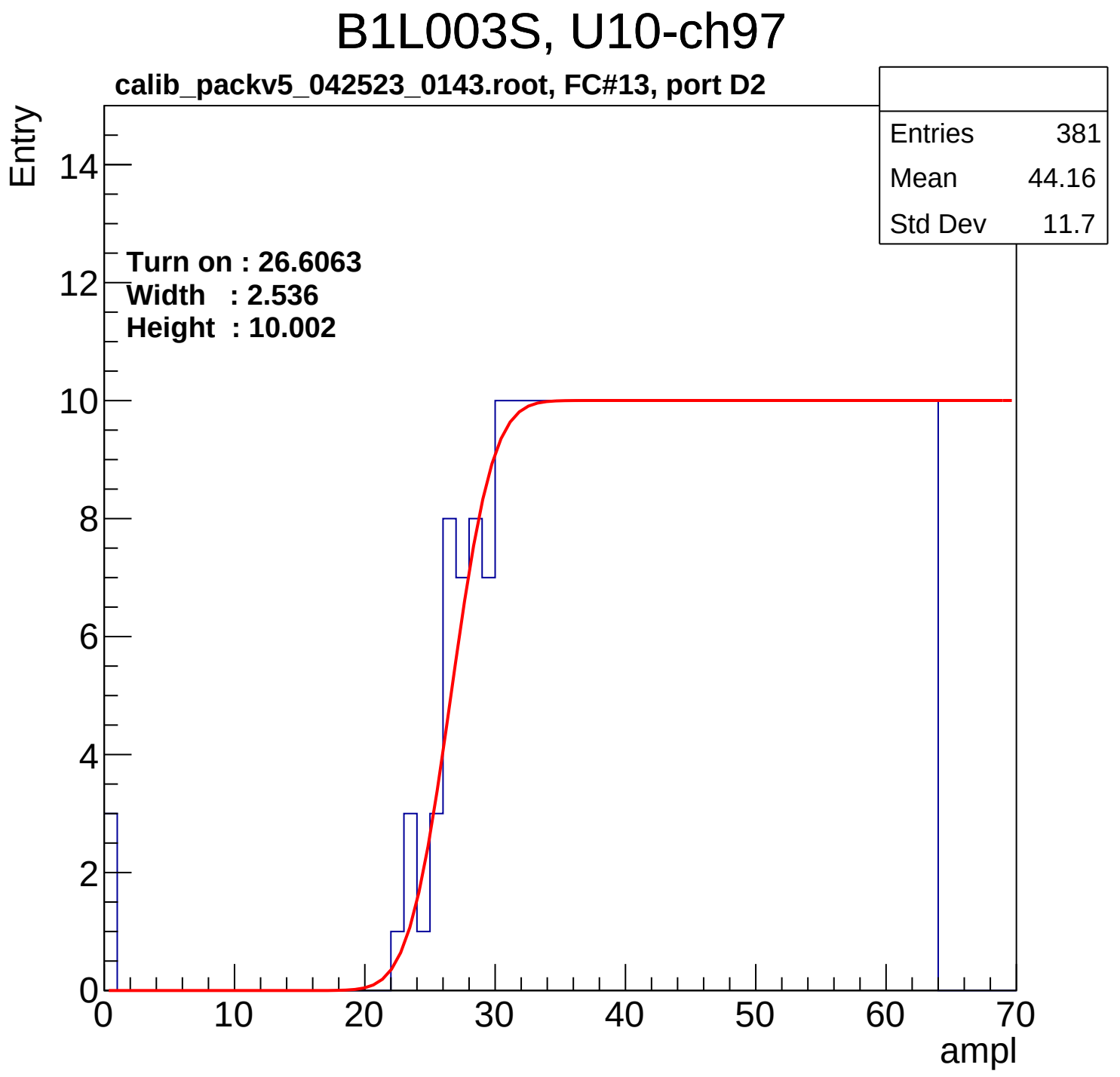

B1L003S, U10-ch92
calib_packv5_042523_0143.root, FC#13, port D2
Entries 387
Mean 43.97
Std Dev 11.61
Turn on : 25.2630
Width : 1.957
Height : 9.968
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

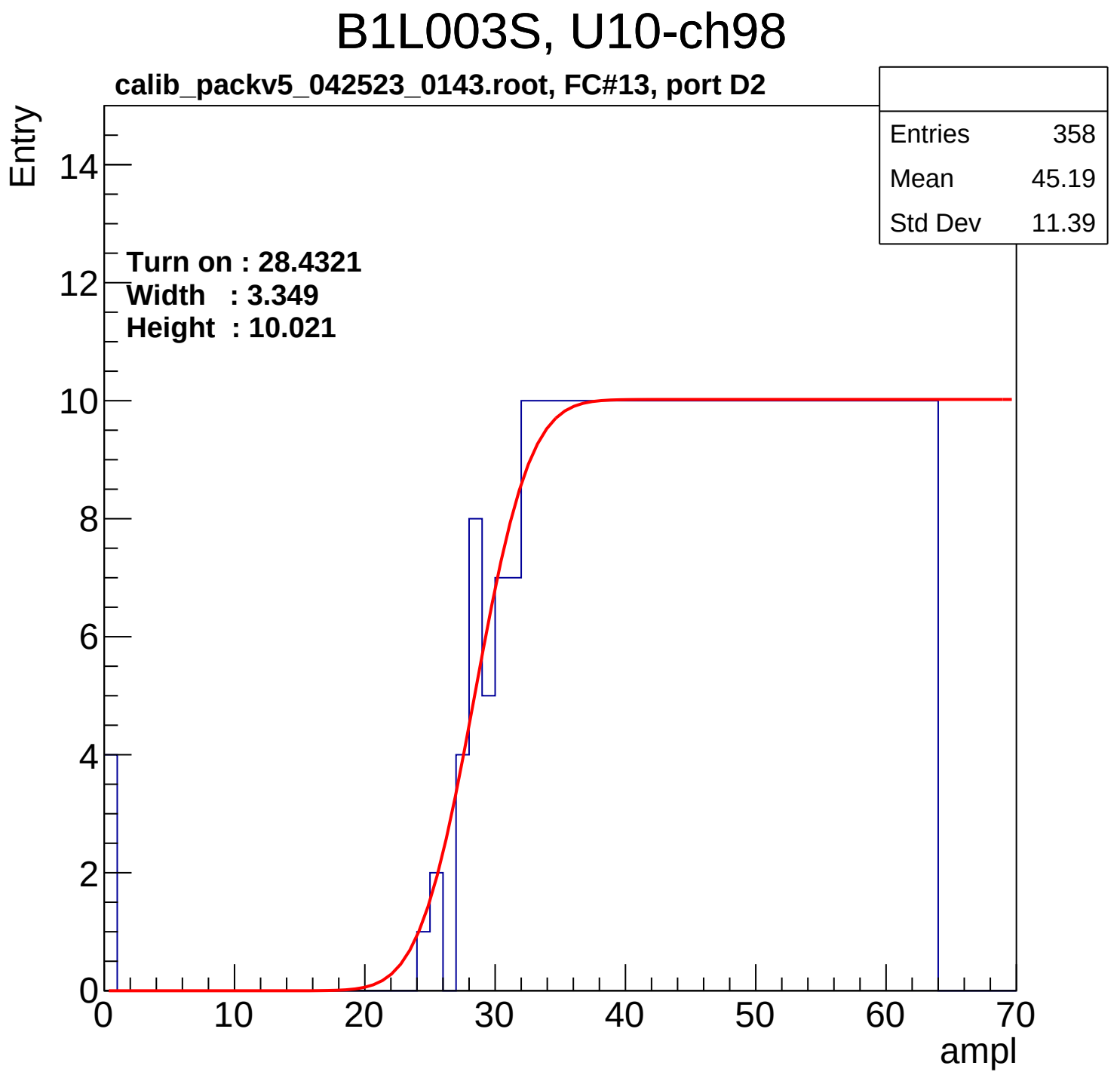

B1L003S, U10-ch93
calib_packv5_042523_0143.root, FC#13, port D2
Entries 372
Mean 44.53
Std Dev 11.66
Turn on : 26.4852
Width : 1.367
Height : 9.762
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

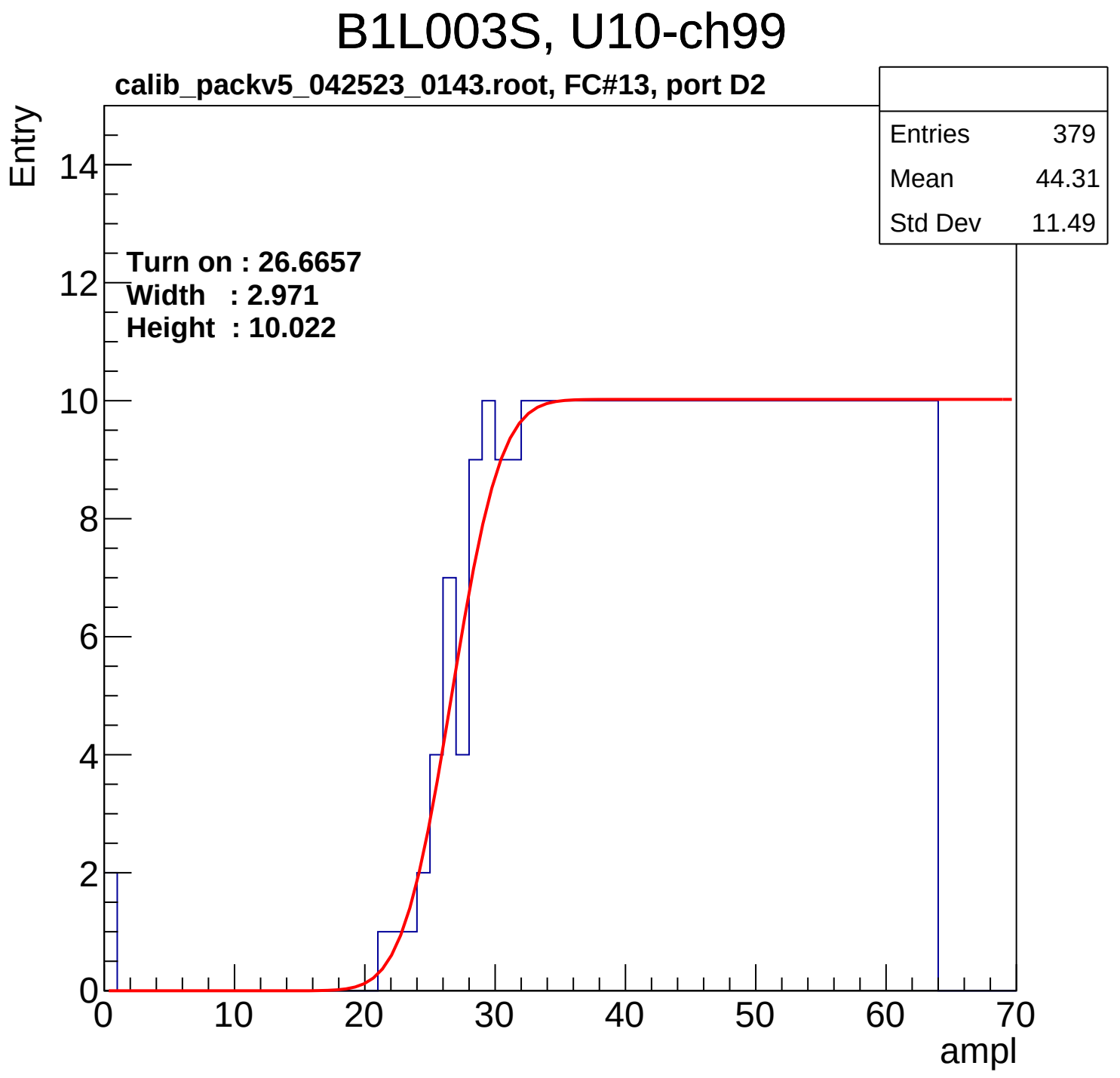

B1L003S, U10-ch94
calib_packv5_042523_0143.root, FC#13, port D2
Entries 367
Mean 44.99
Std Dev 10.96
Turn on : 27.6739
Width : 2.578
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

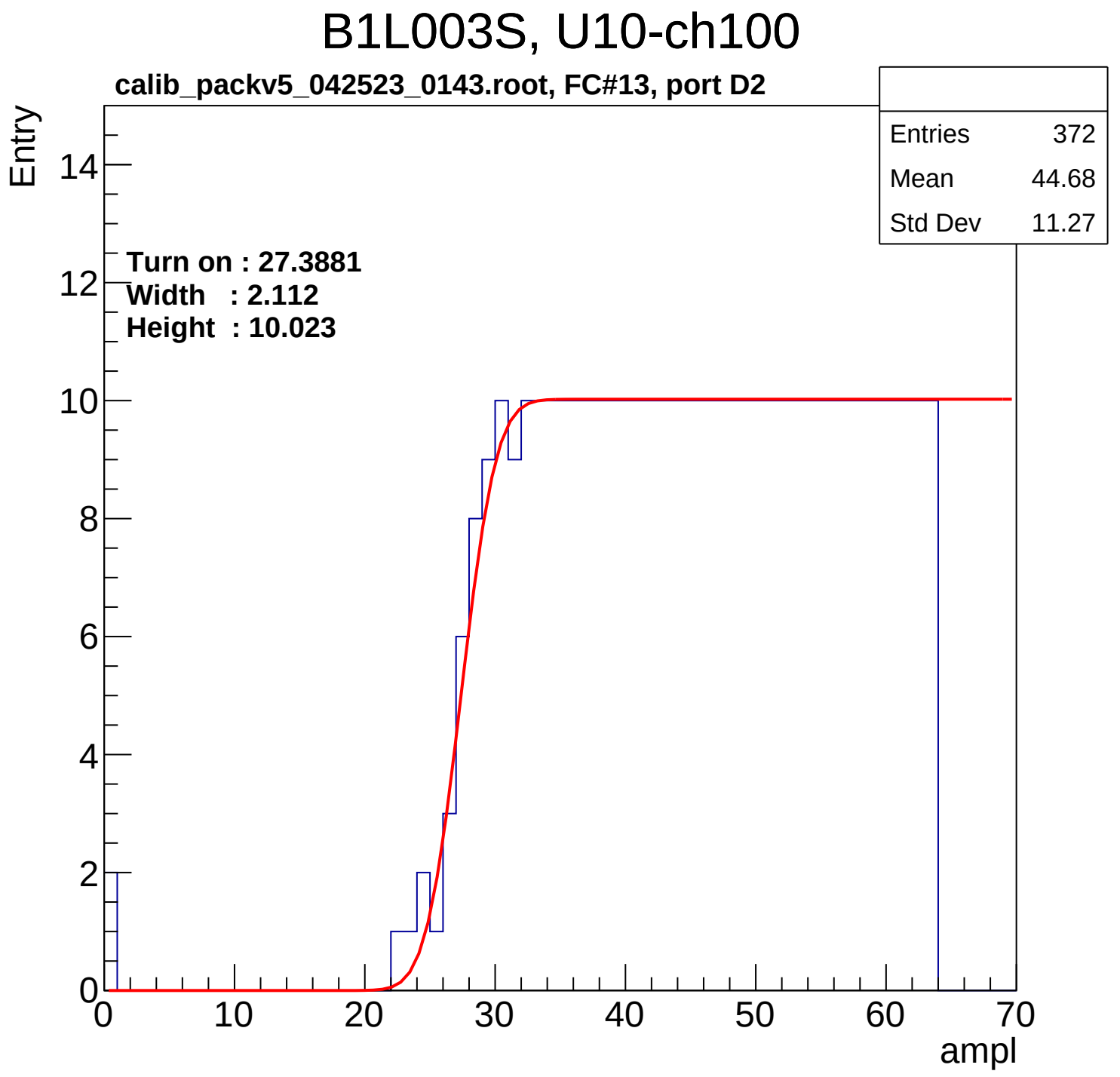

B1L003S, U10-ch95
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 44.15
Std Dev 11.72
Turn on : 26.5783
Width : 3.082
Height : 10.034
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

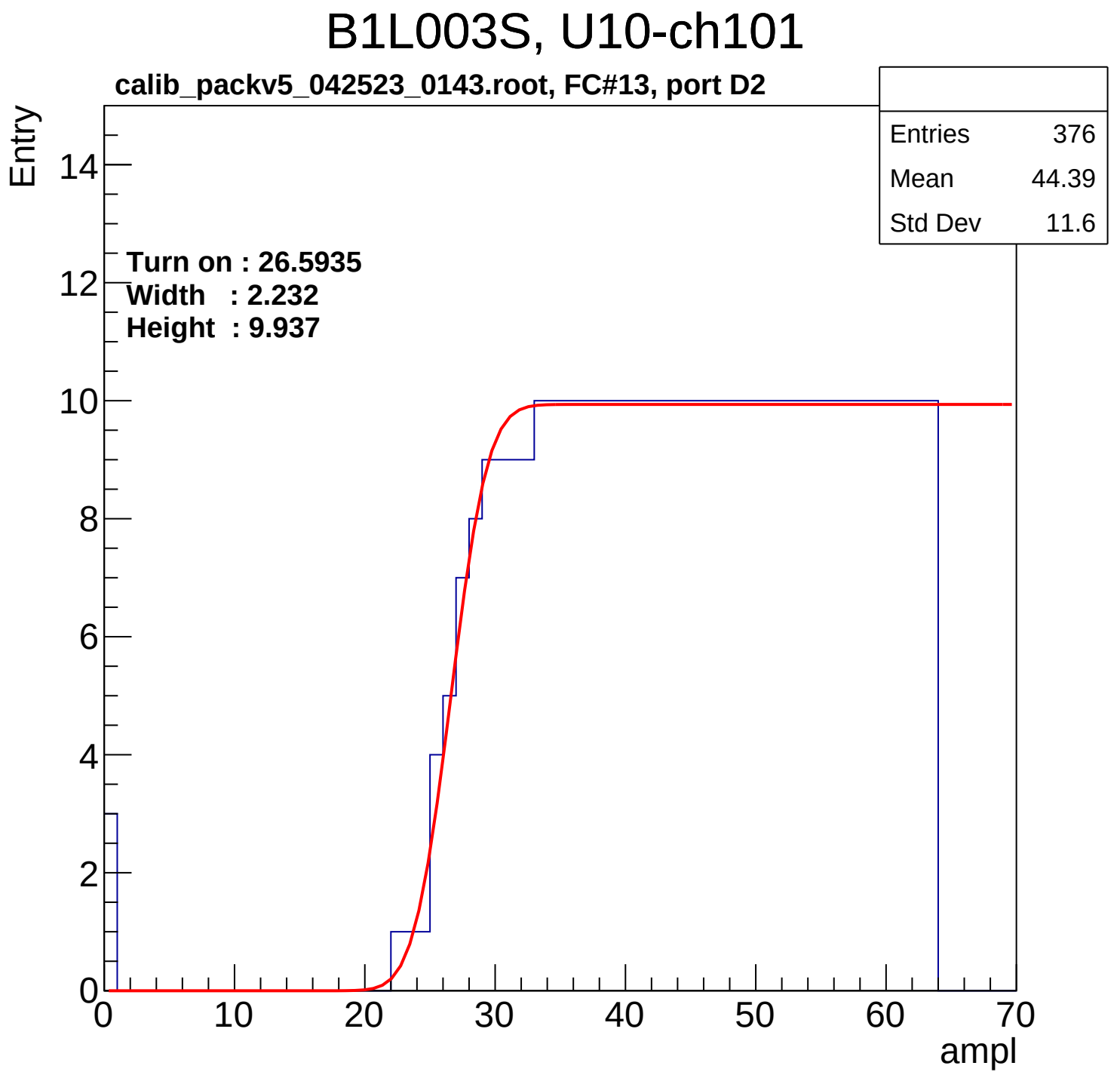

B1L003S, U10-ch96
calib_packv5_042523_0143.root, FC#13, port D2
Entries 374
Mean 44.52
Std Dev 11.41
Turn on : 26.7865
Width : 4.157
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

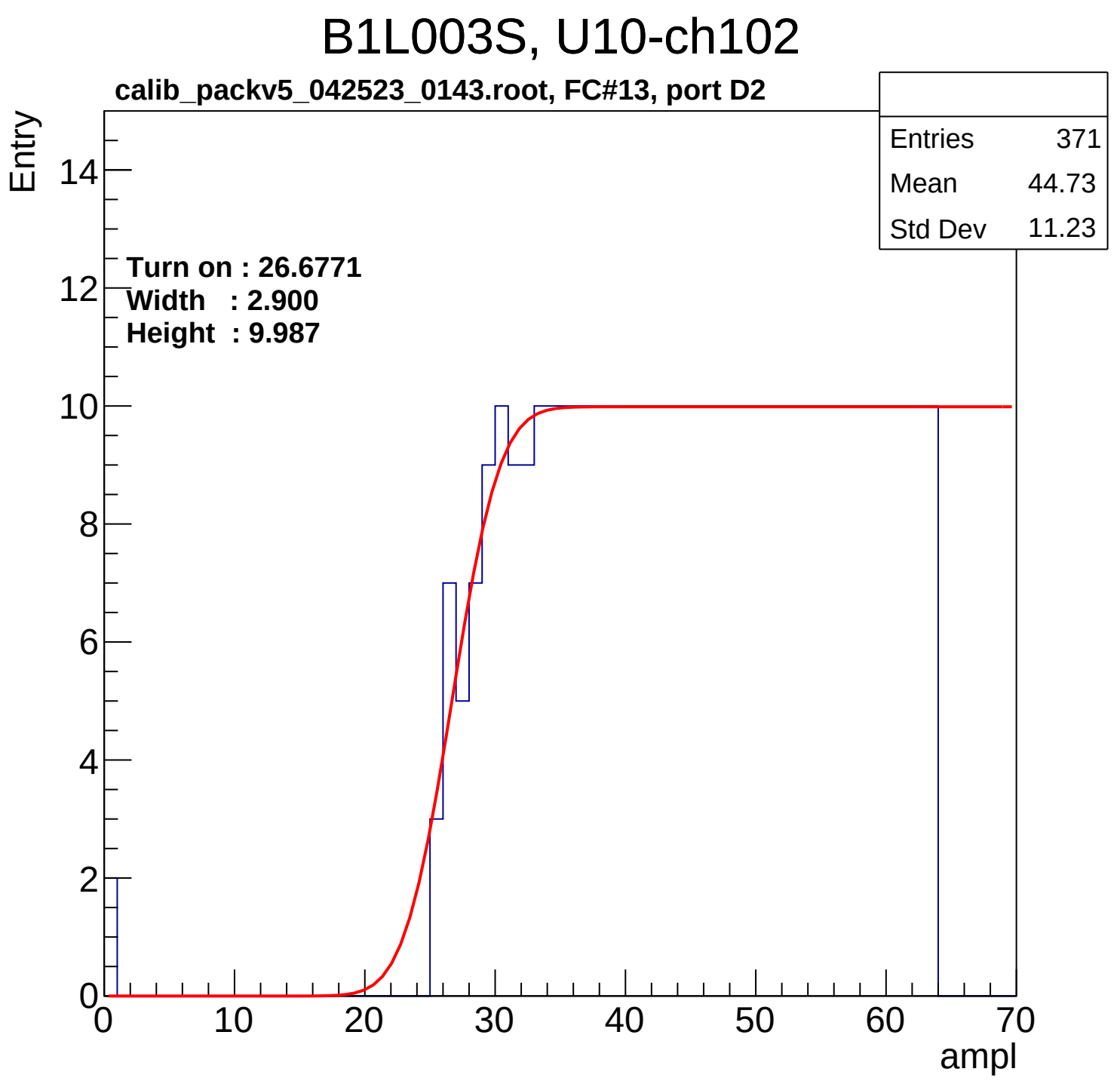

B1L003S, U10-ch97
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 44.16
Std Dev 11.7
Turn on : 26.6063
Width : 2.536
Height : 10.002
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

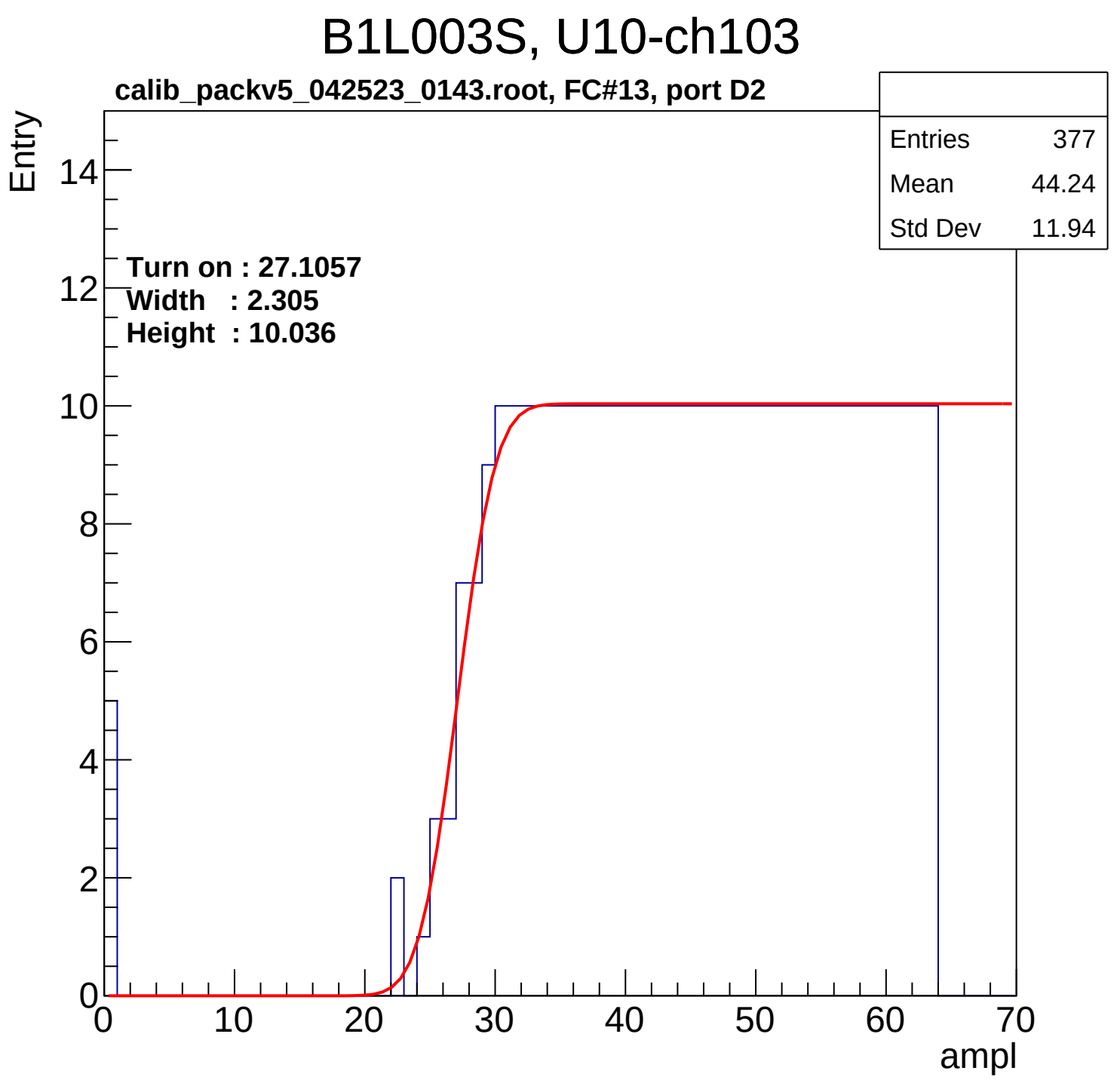

B1L003S, U10-ch98
calib_packv5_042523_0143.root, FC#13, port D2
Entries 358
Mean 45.19
Std Dev 11.39
Turn on : 28.4321
Width : 3.349
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

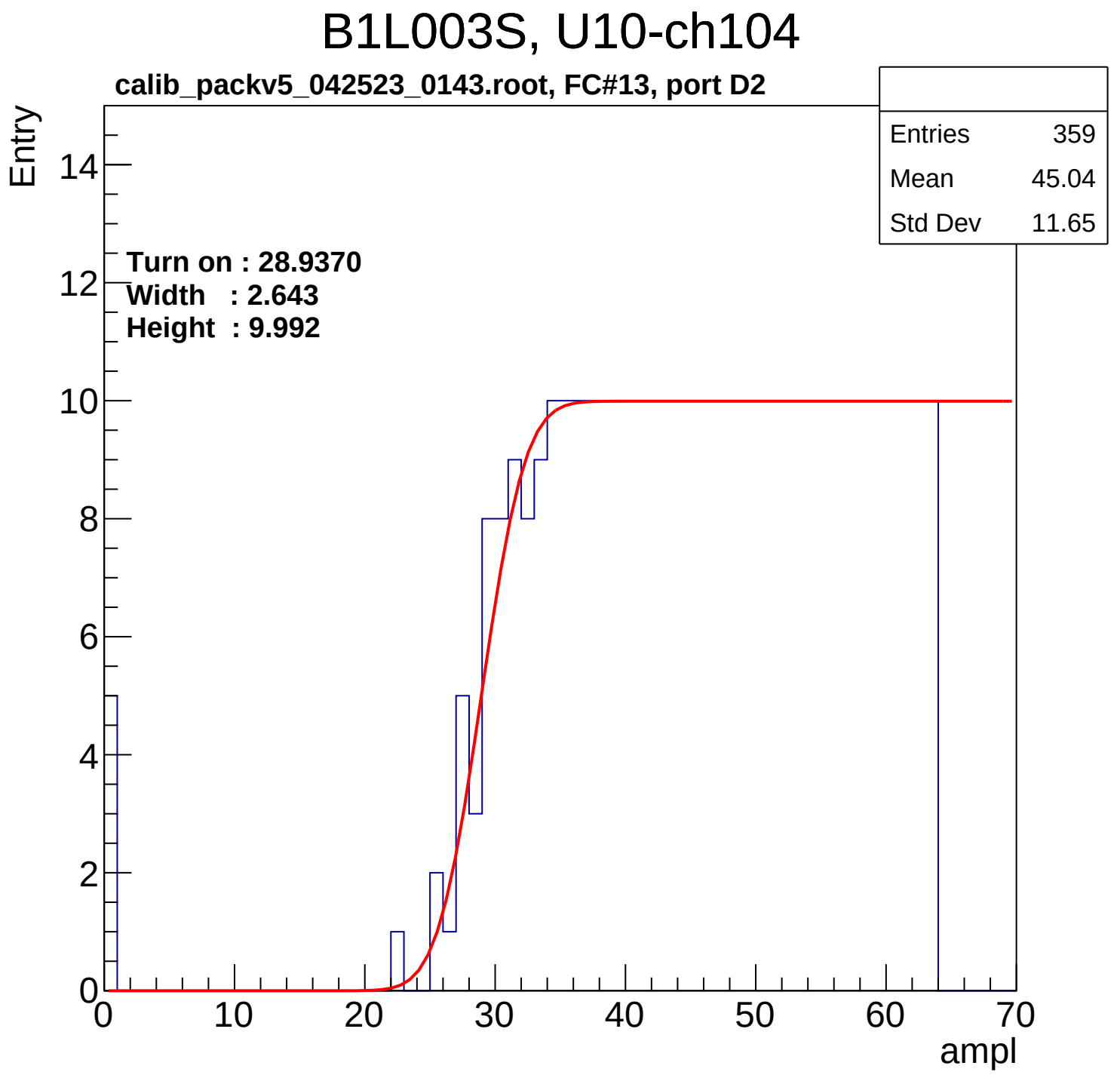

B1L003S, U10-ch99
calib_packv5_042523_0143.root, FC#13, port D2
Entries 379
Mean 44.31
Std Dev 11.49
Turn on : 26.6657
Width : 2.971
Height : 10.022
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

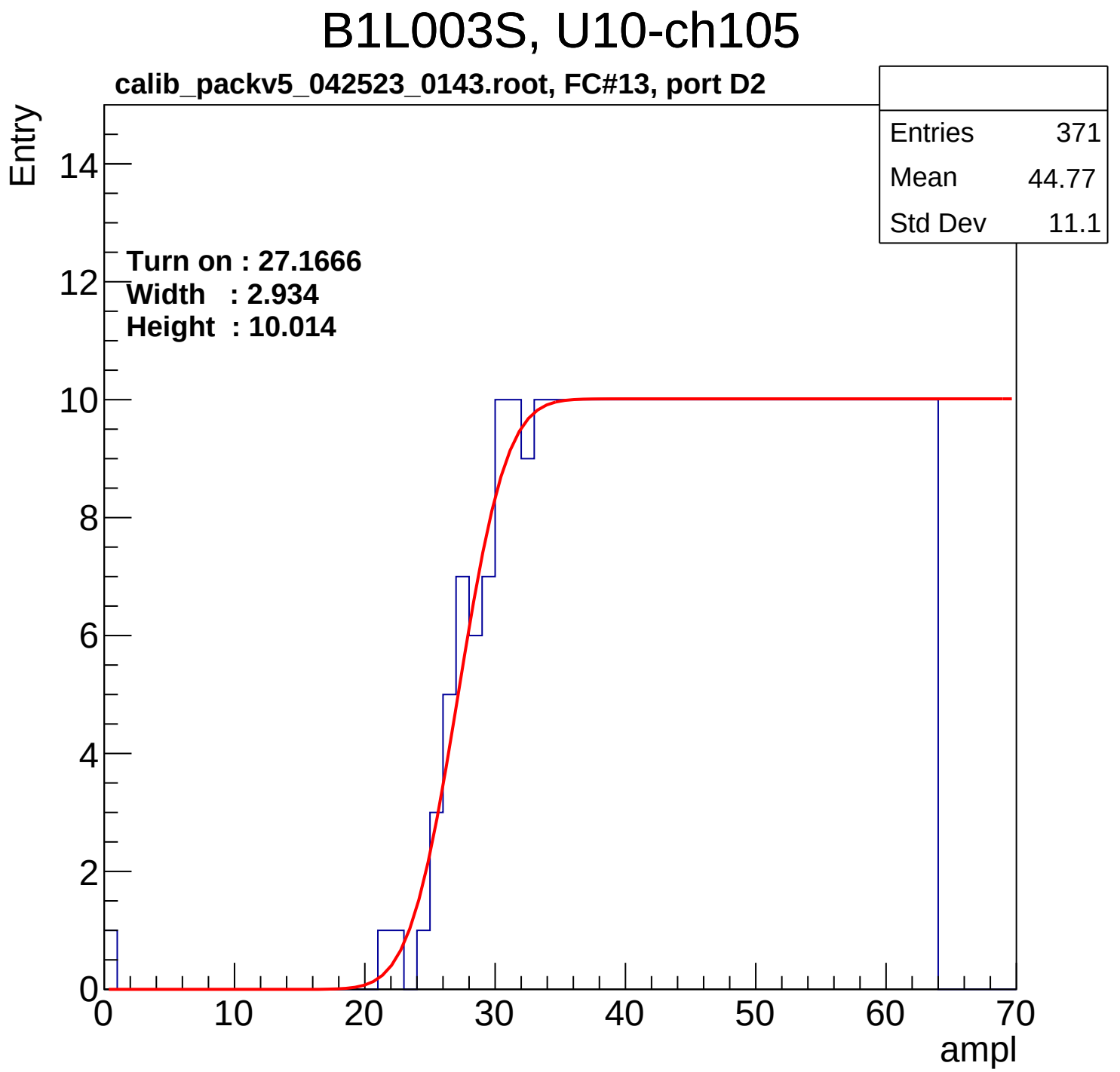

B1L003S, U10-ch100
calib_packv5_042523_0143.root, FC#13, port D2
Entries 372
Mean 44.68
Std Dev 11.27
Turn on : 27.3881
Width : 2.112
Height : 10.023
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

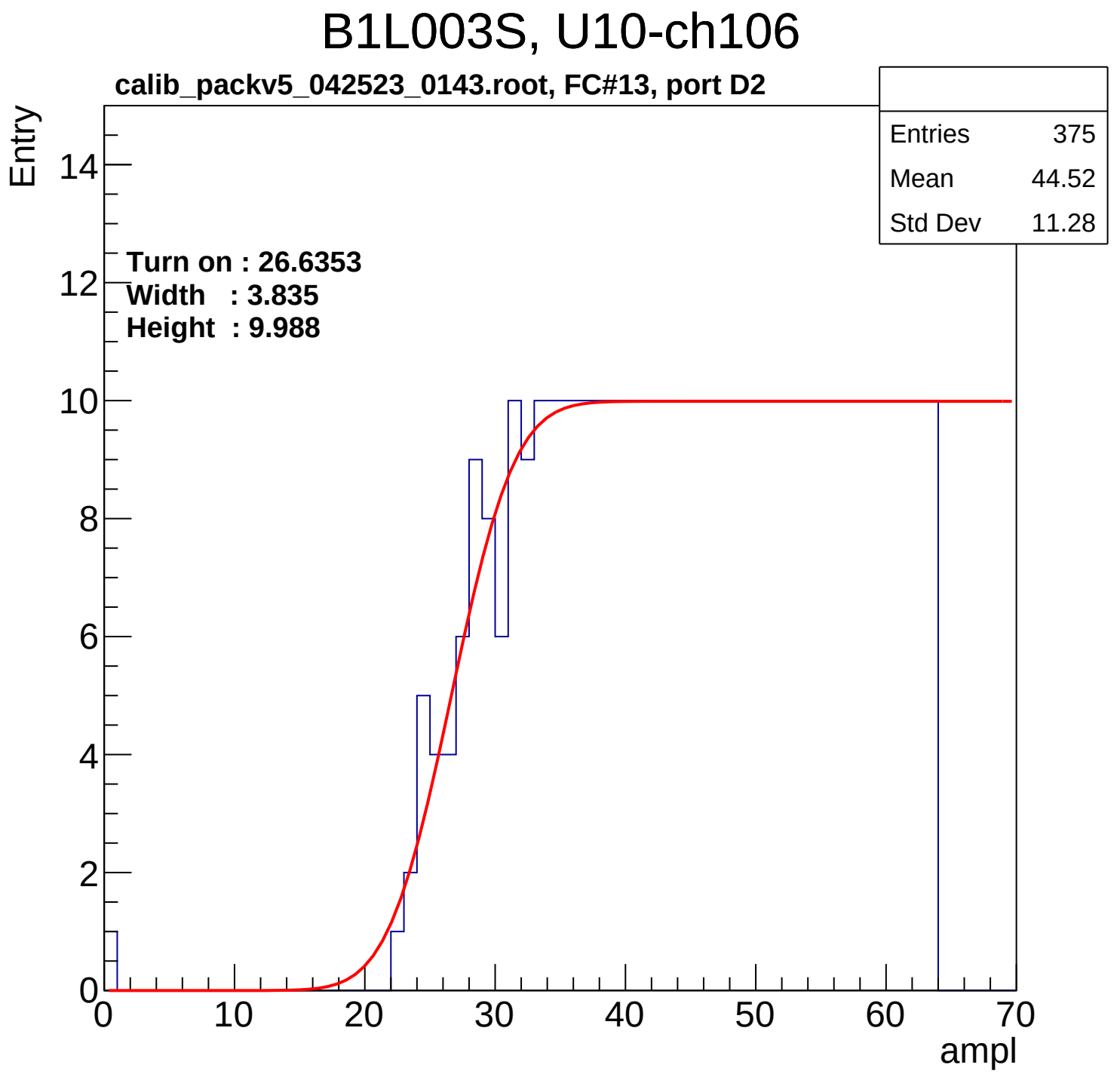

B1L003S, U10-ch101
calib_packv5_042523_0143.root, FC#13, port D2
Entries 376
Mean 44.39
Std Dev 11.6
Turn on : 26.5935
Width : 2.232
Height : 9.937
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

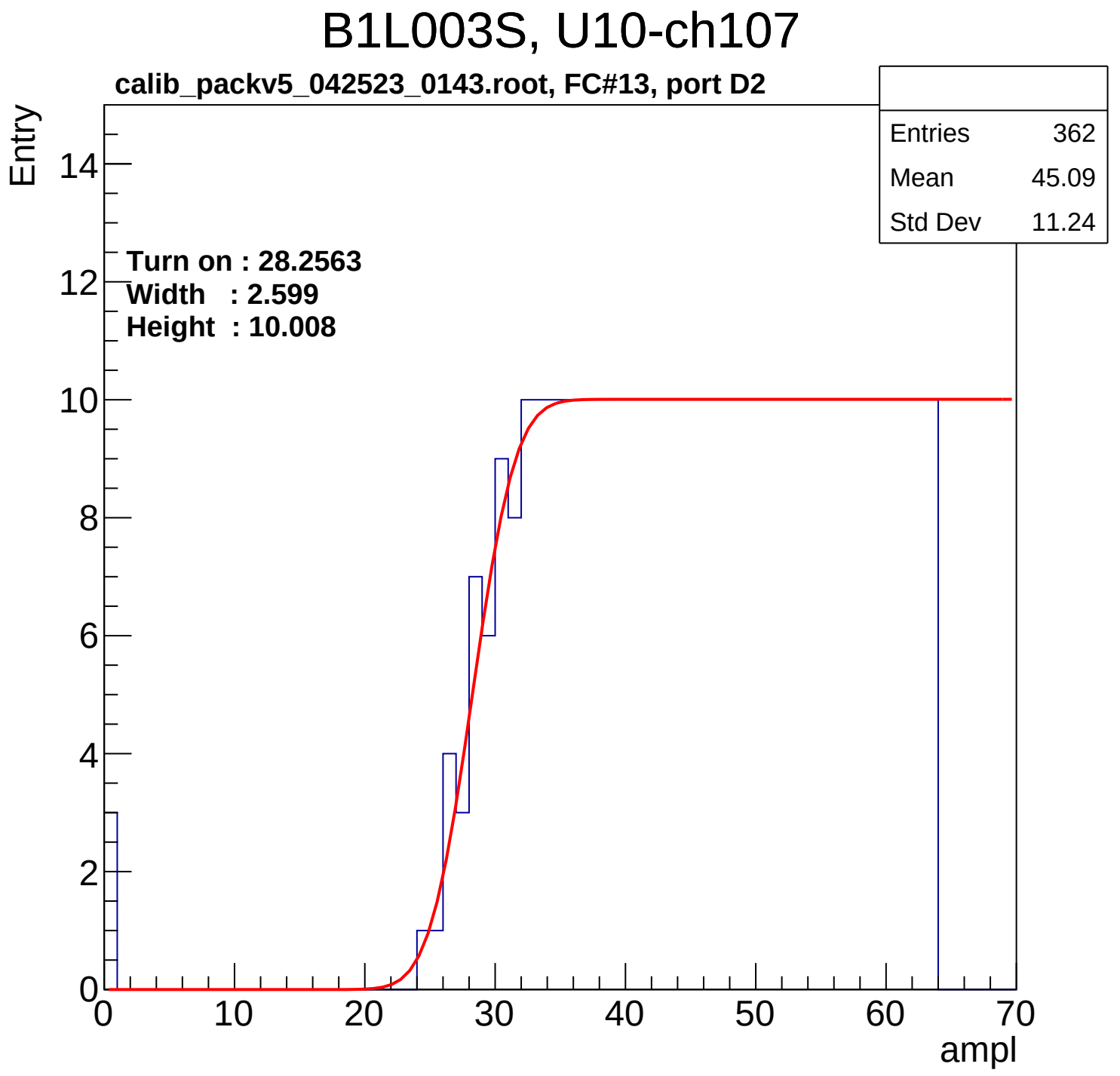

B1L003S, U10-ch102
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.73
Std Dev 11.23
Turn on : 26.6771
Width : 2.900
Height : 9.987
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

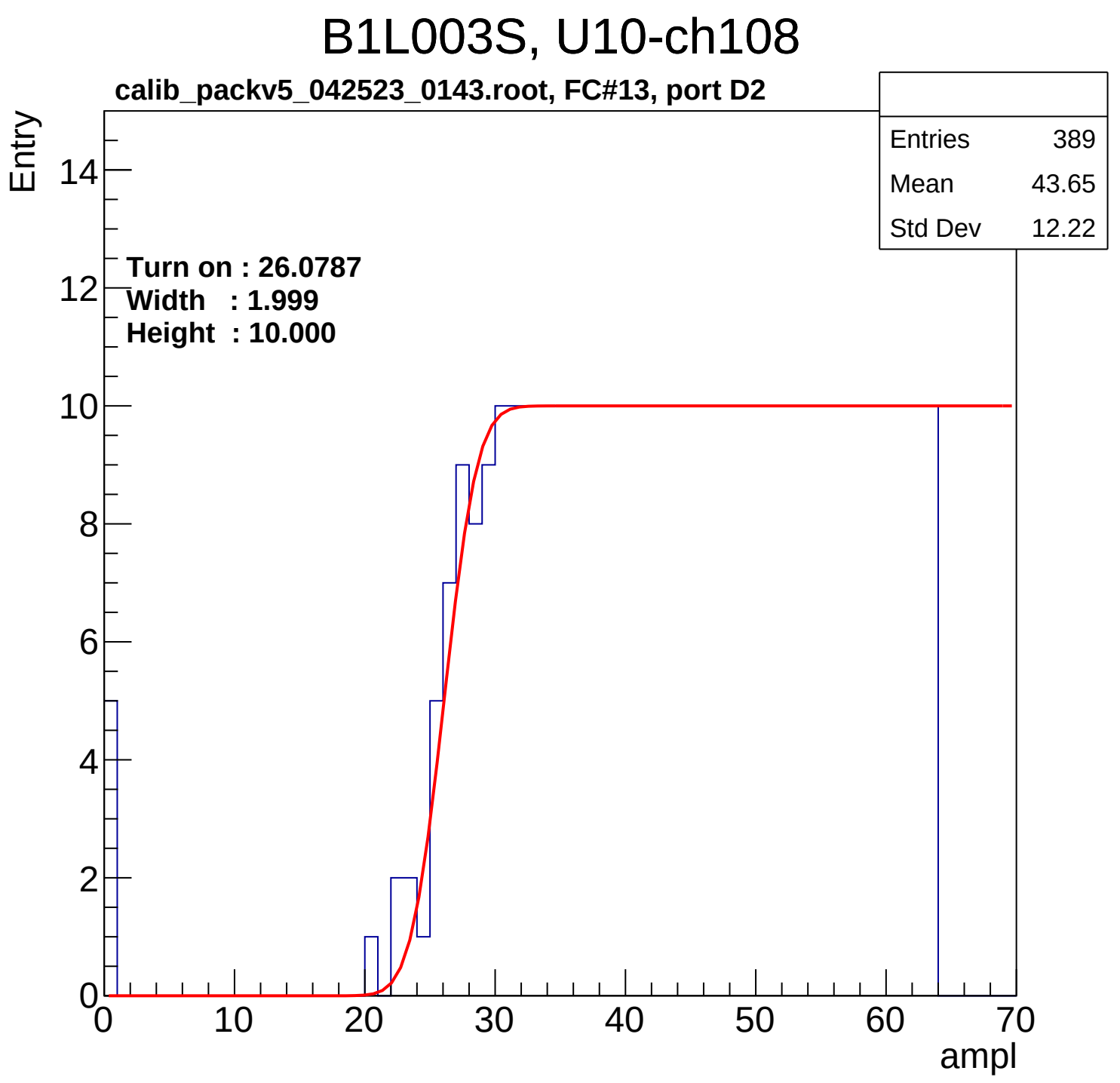

B1L003S, U10-ch103
calib_packv5_042523_0143.root, FC#13, port D2
Entries 377
Mean 44.24
Std Dev 11.94
Turn on : 27.1057
Width : 2.305
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

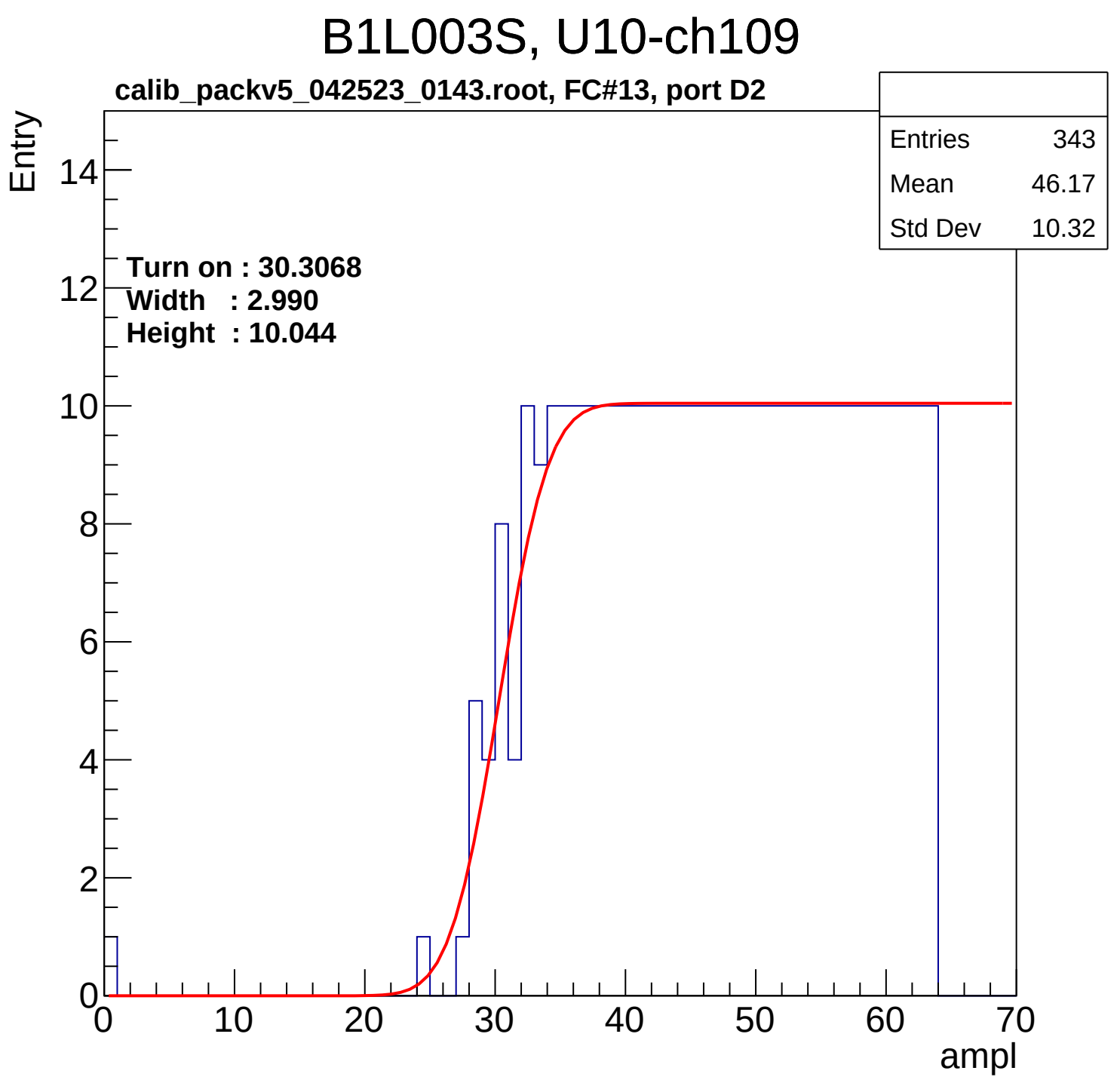

B1L003S, U10-ch104
calib_packv5_042523_0143.root, FC#13, port D2
Entries 359
Mean 45.04
Std Dev 11.65
Turn on : 28.9370
Width : 2.643
Height : 9.992
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

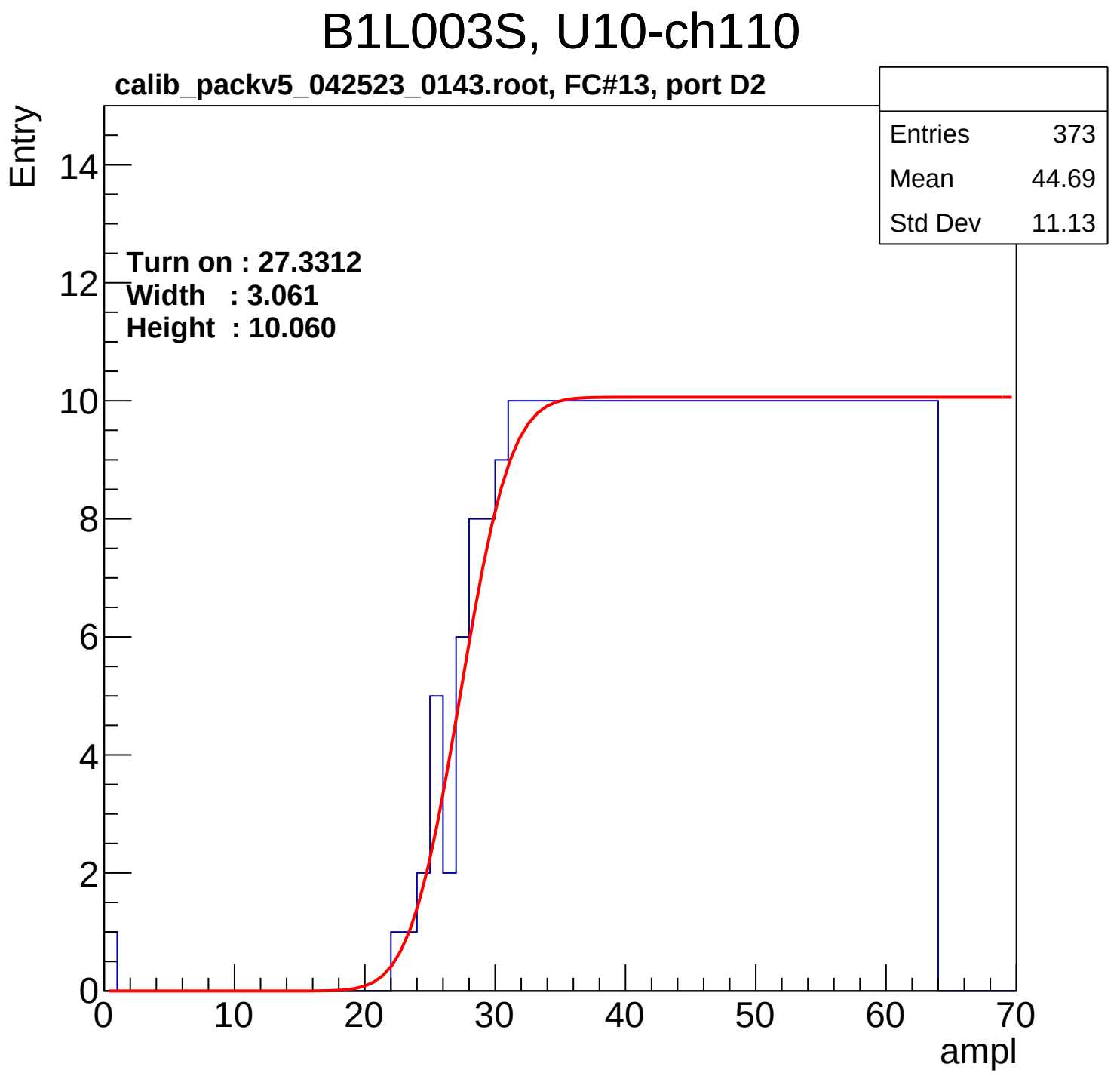

B1L003S, U10-ch105
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.77
Std Dev 11.1
Turn on : 27.1666
Width : 2.934
Height : 10.014
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

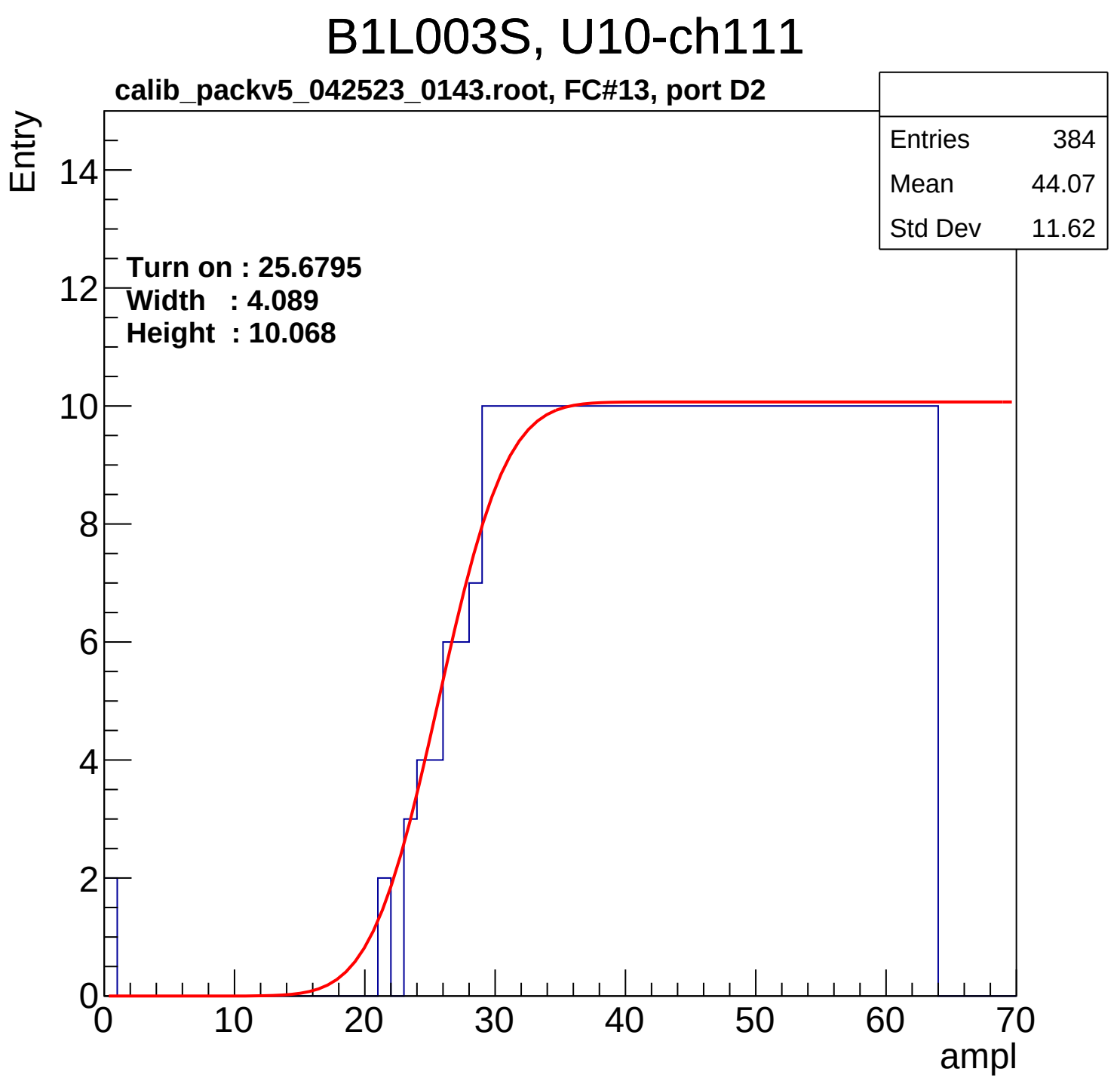

B1L003S, U10-ch106
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.52
Std Dev 11.28
Turn on : 26.6353
Width : 3.835
Height : 9.988
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

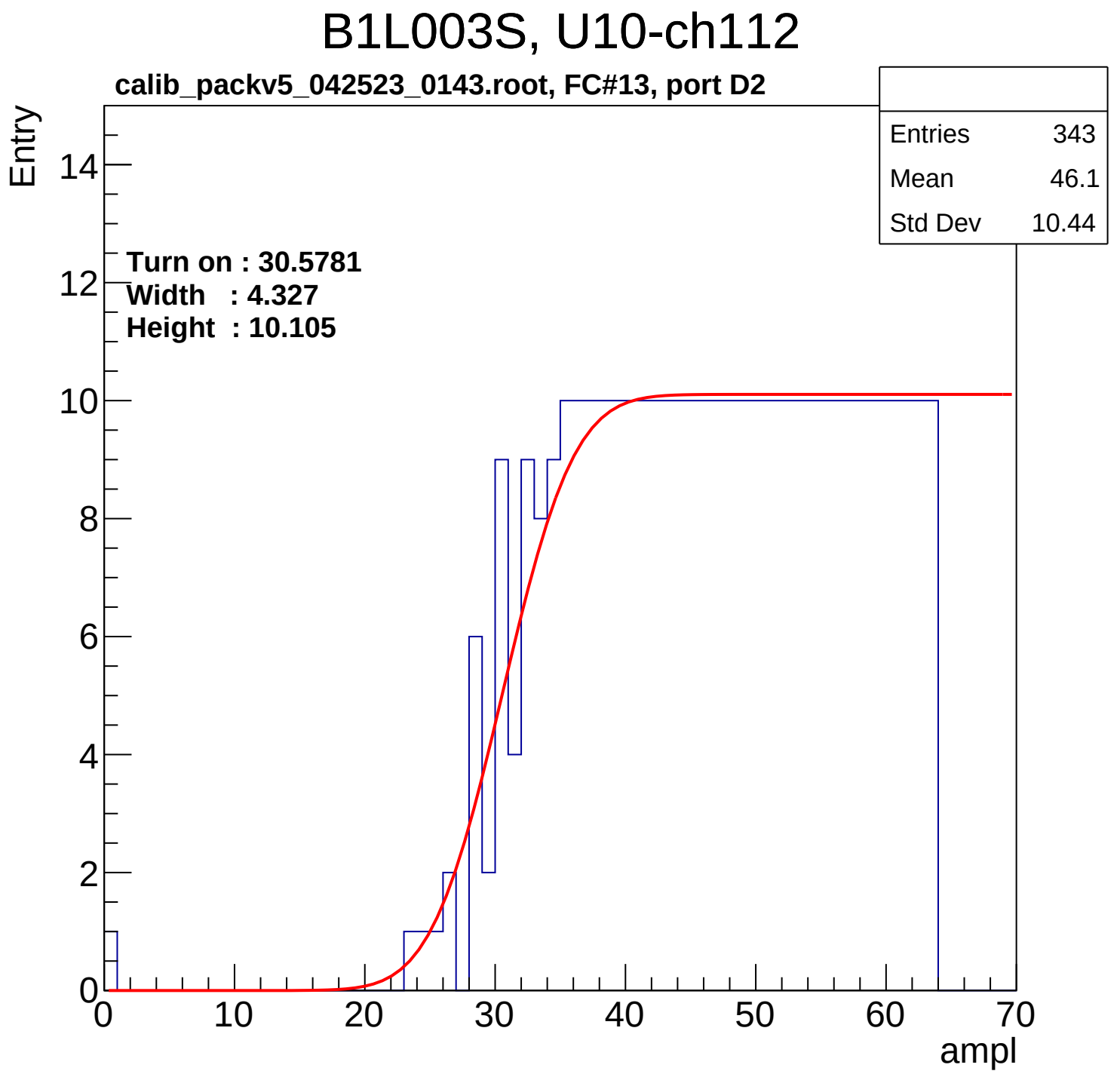

B1L003S, U10-ch107
calib_packv5_042523_0143.root, FC#13, port D2
Entries 362
Mean 45.09
Std Dev 11.24
Turn on : 28.2563
Width : 2.599
Height : 10.008
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

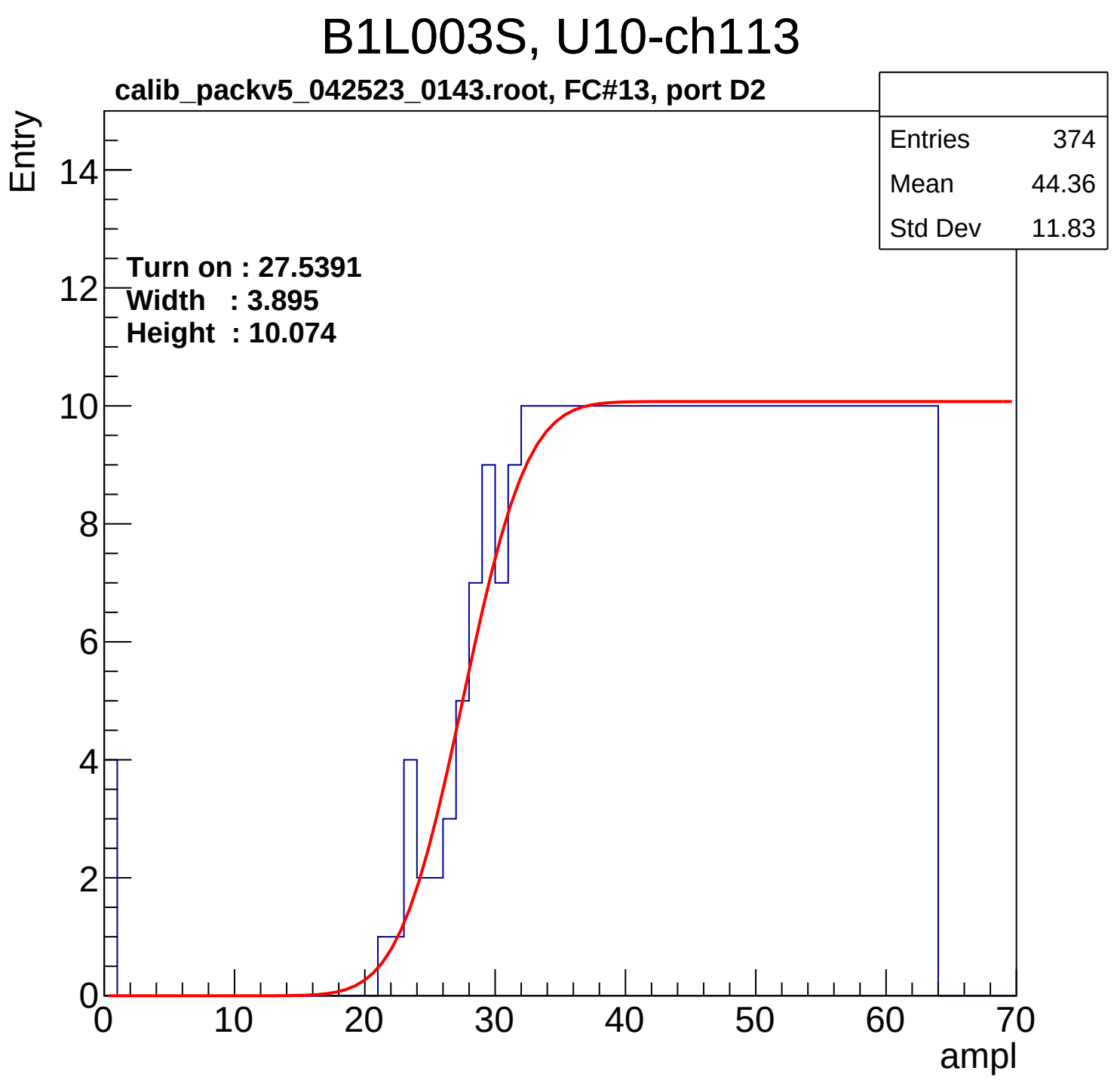

B1L003S, U10-ch108
calib_packv5_042523_0143.root, FC#13, port D2
Entries 389
Mean 43.65
Std Dev 12.22
Turn on : 26.0787
Width : 1.999
Height : 10.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

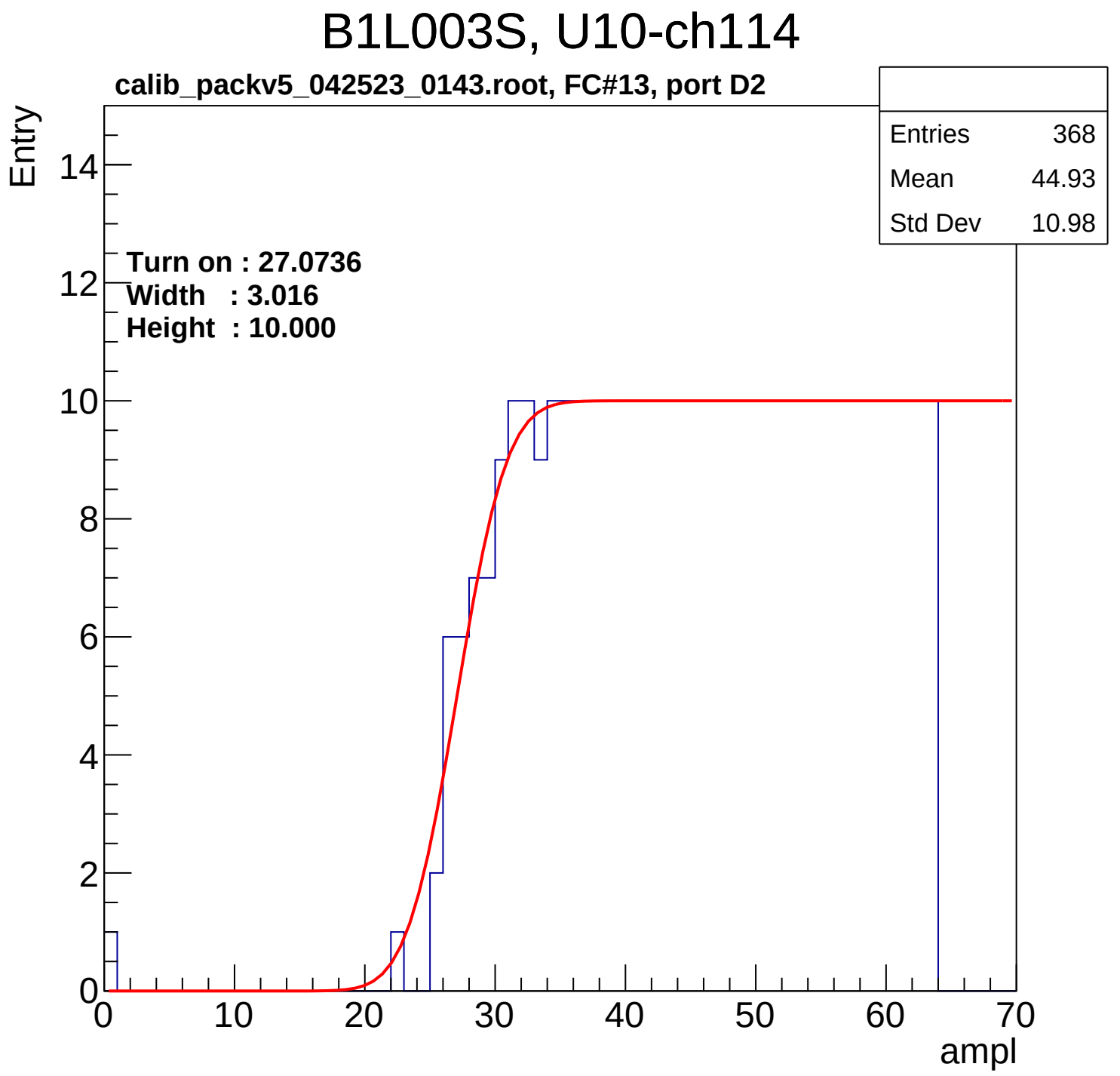

B1L003S, U10-ch109
calib_packv5_042523_0143.root, FC#13, port D2
Entries 343
Mean 46.17
Std Dev 10.32
Turn on : 30.3068
Width : 2.990
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

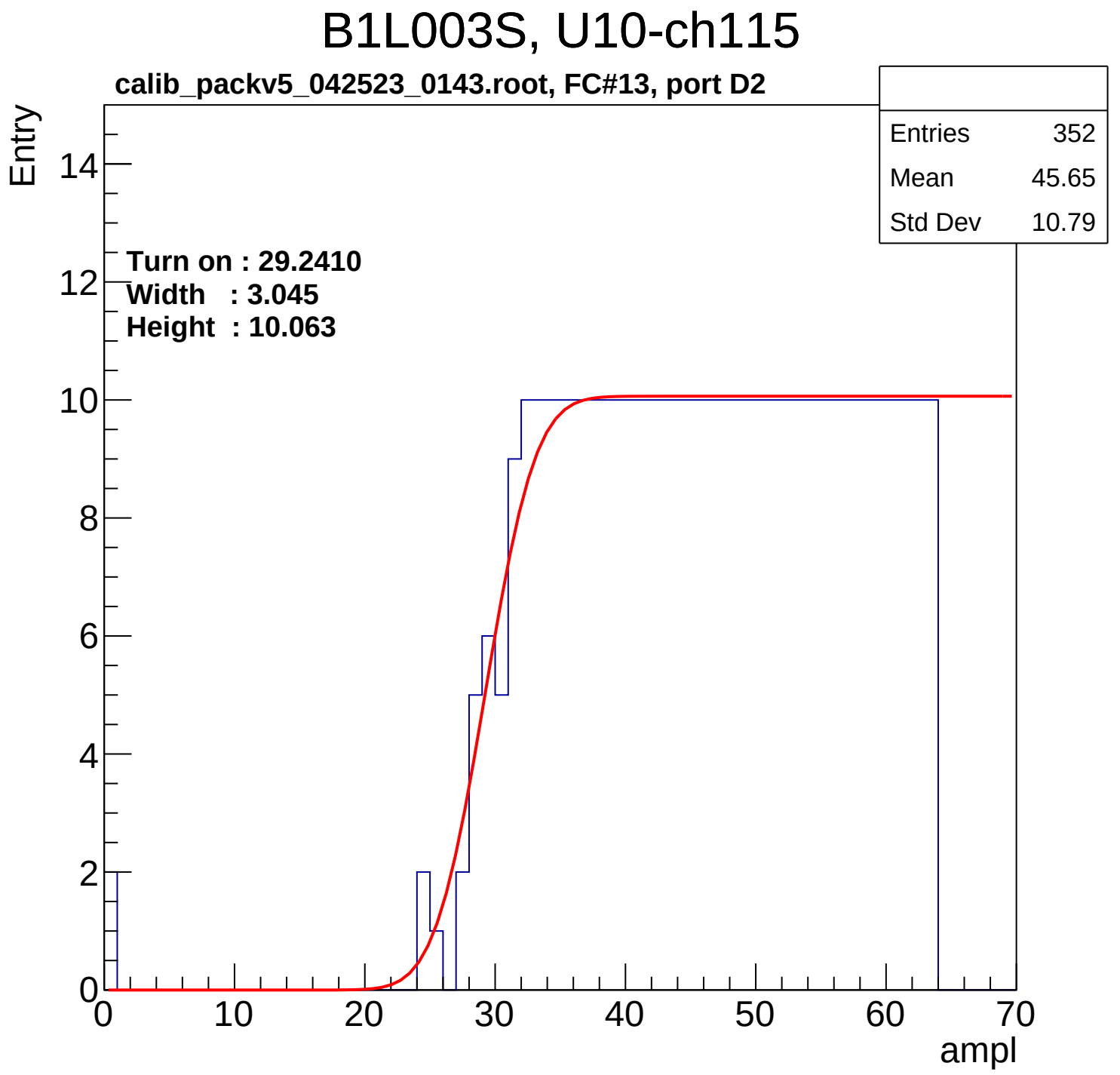

B1L003S, U10-ch110
calib_packv5_042523_0143.root, FC#13, port D2
Entries 373
Mean 44.69
Std Dev 11.13
Turn on : 27.3312
Width : 3.061
Height : 10.060
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

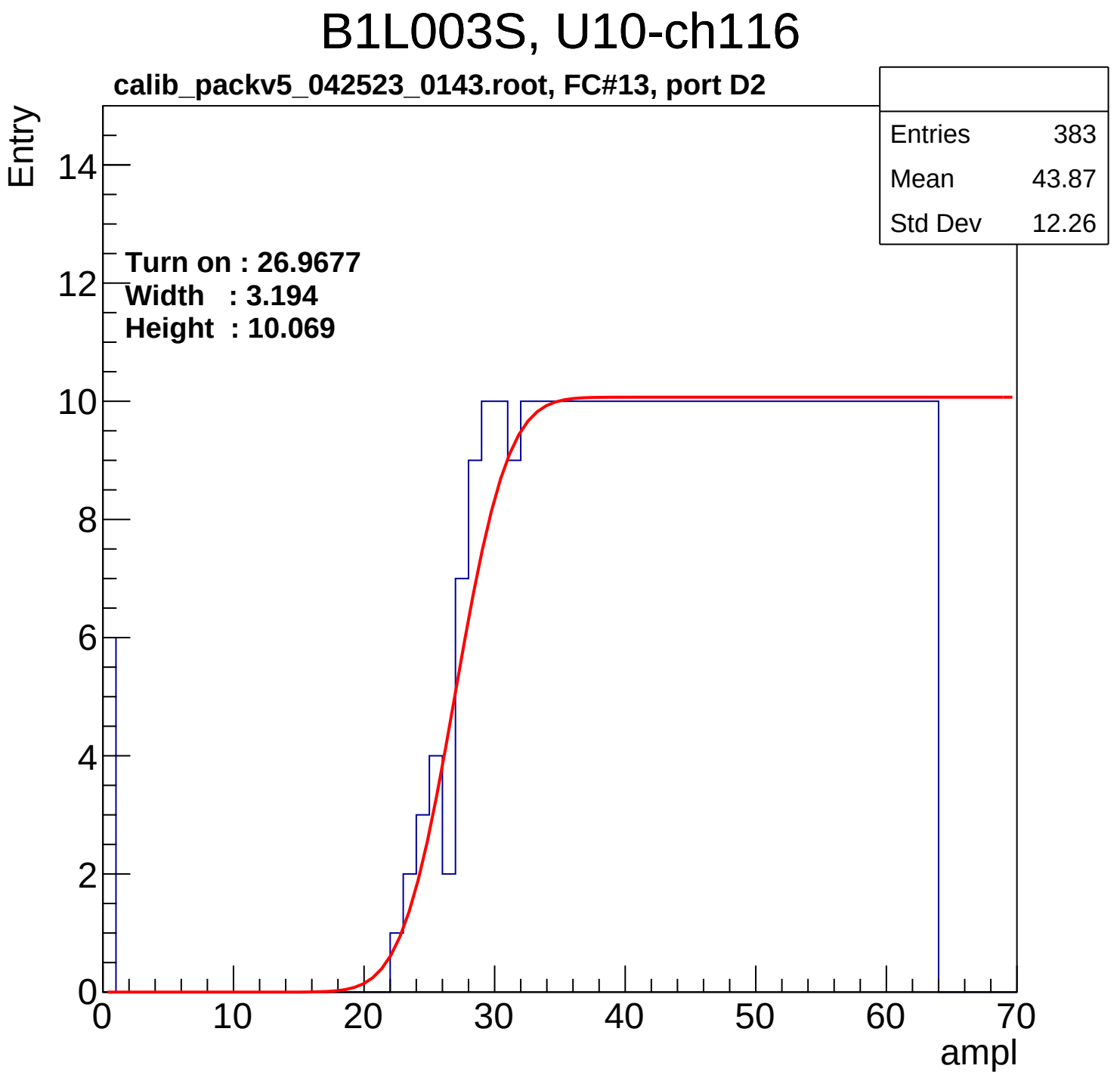

B1L003S, U10-ch111
calib_packv5_042523_0143.root, FC#13, port D2
Entries 384
Mean 44.07
Std Dev 11.62
Turn on : 25.6795
Width : 4.089
Height : 10.068
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

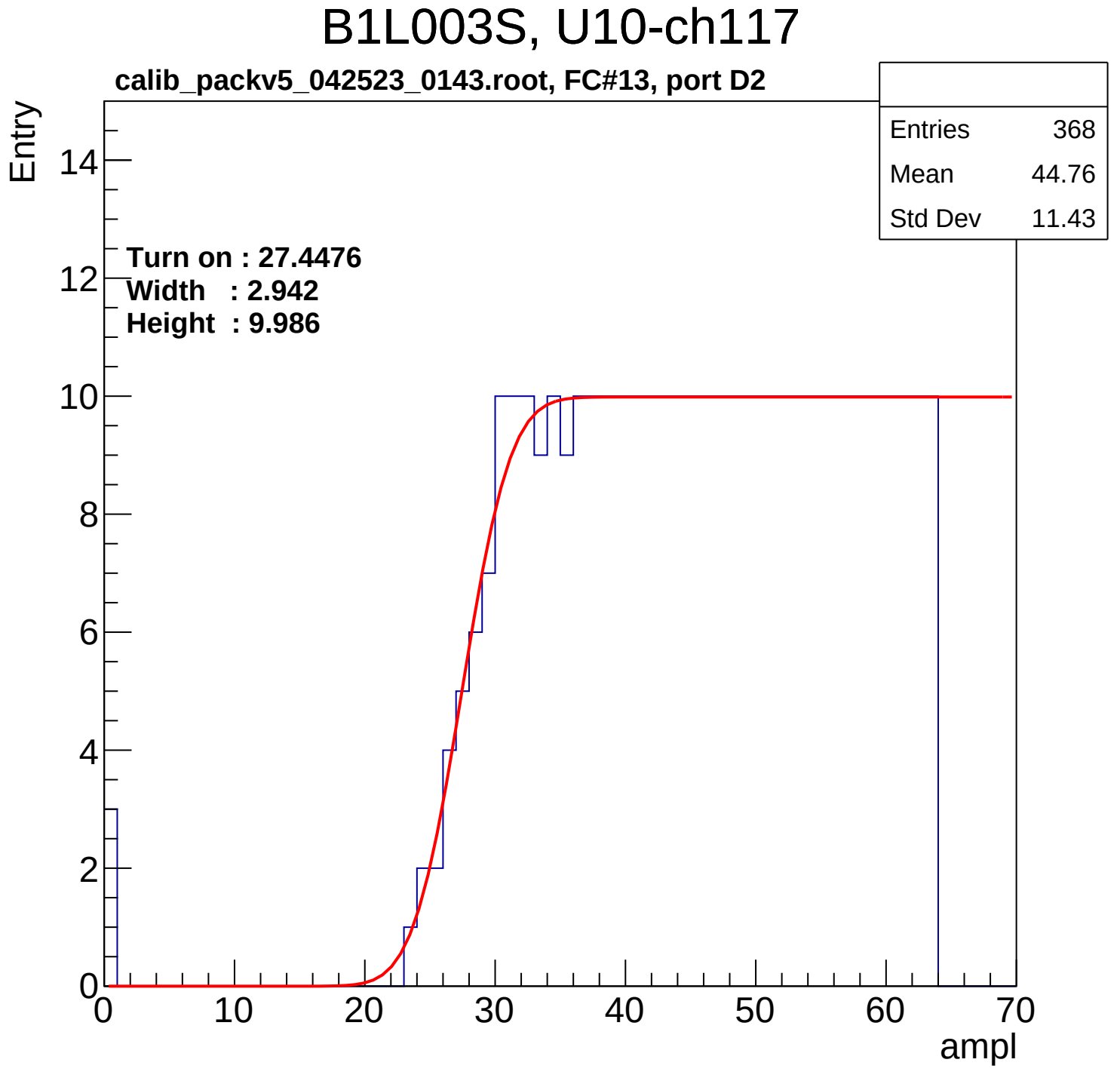

B1L003S, U10-ch112
calib_packv5_042523_0143.root, FC#13, port D2
Entries 343
Mean 46.1
Std Dev 10.44
Turn on : 30.5781
Width : 4.327
Height : 10.105
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

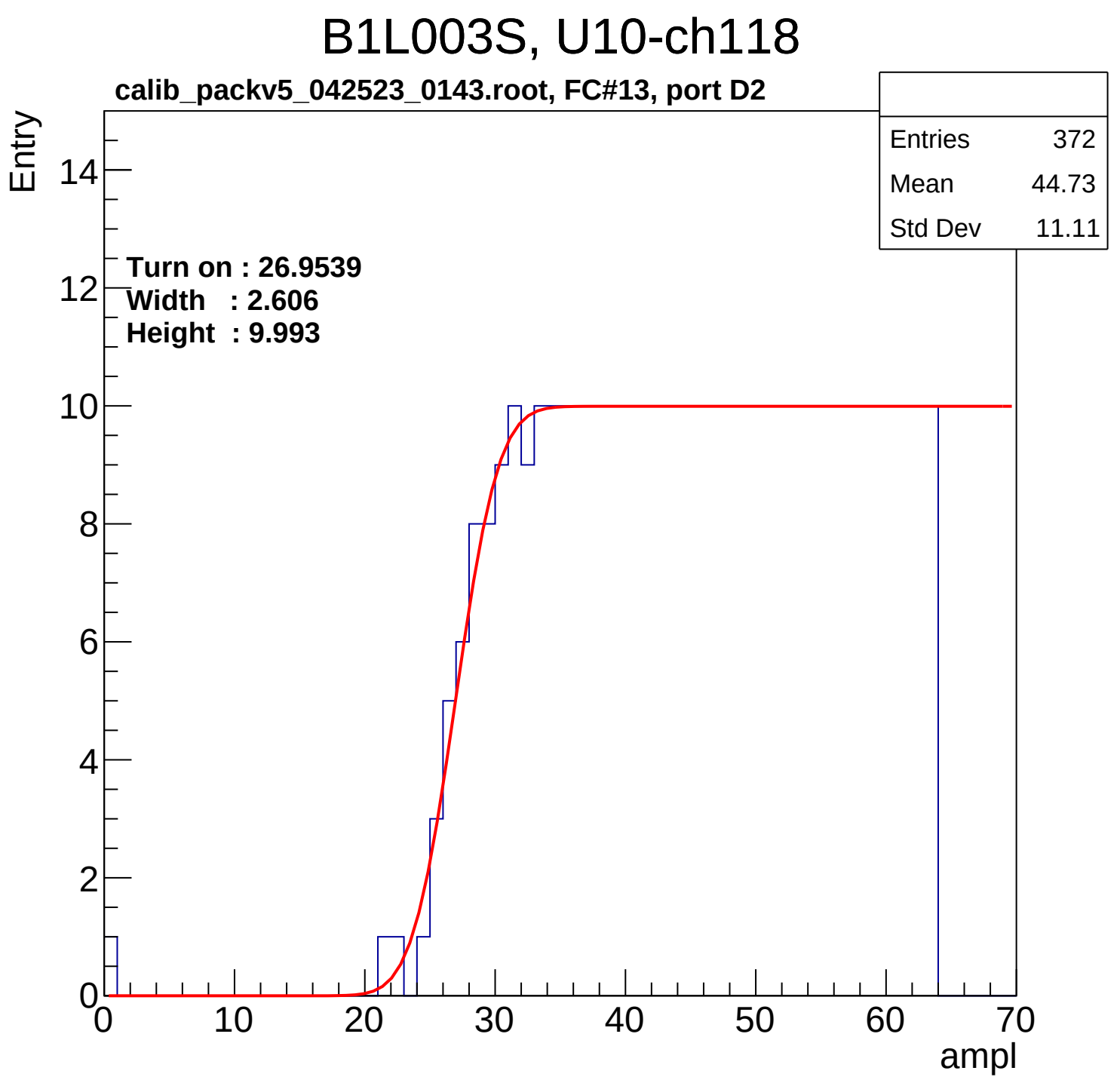

B1L003S, U10-ch113
calib_packv5_042523_0143.root, FC#13, port D2
Entries 374
Mean 44.36
Std Dev 11.83
Turn on : 27.5391
Width : 3.895
Height : 10.074
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

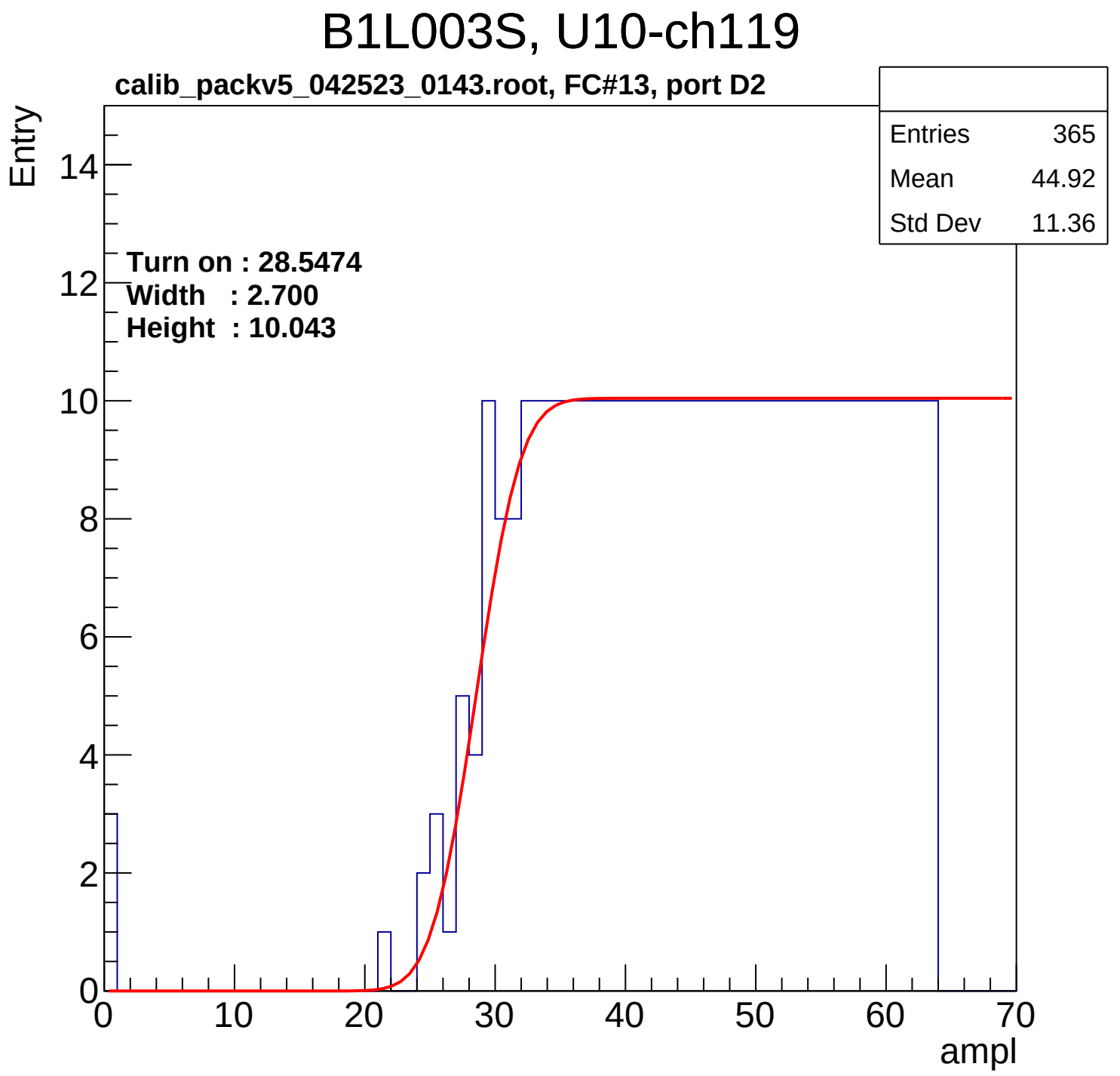

B1L003S, U10-ch114
calib_packv5_042523_0143.root, FC#13, port D2
Entries 368
Mean 44.93
Std Dev 10.98
Turn on : 27.0736
Width : 3.016
Height : 10.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

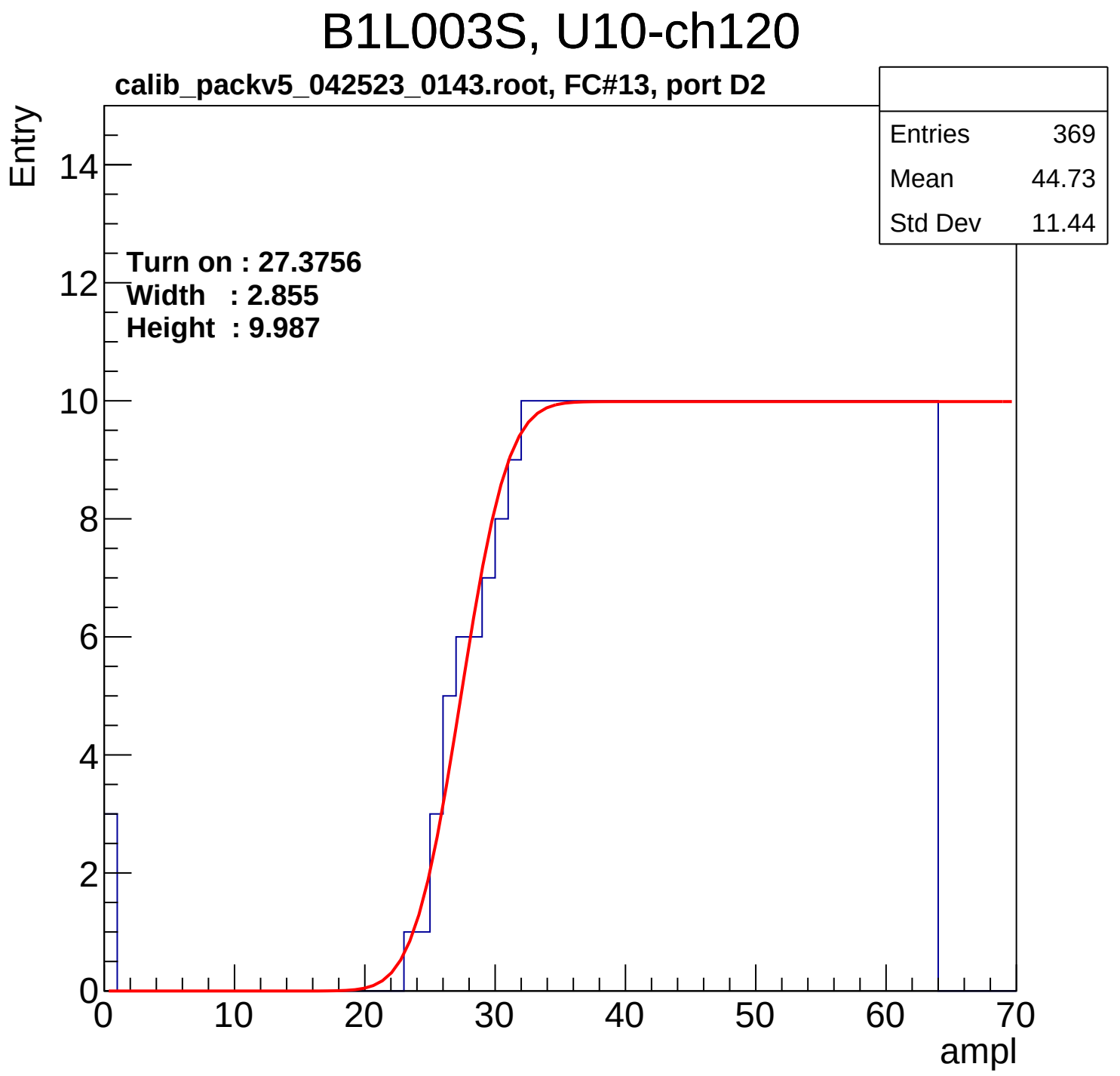

B1L003S, U10-ch115
calib_packv5_042523_0143.root, FC#13, port D2
Entries 352
Mean 45.65
Std Dev 10.79
Turn on : 29.2410
Width : 3.045
Height : 10.063
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

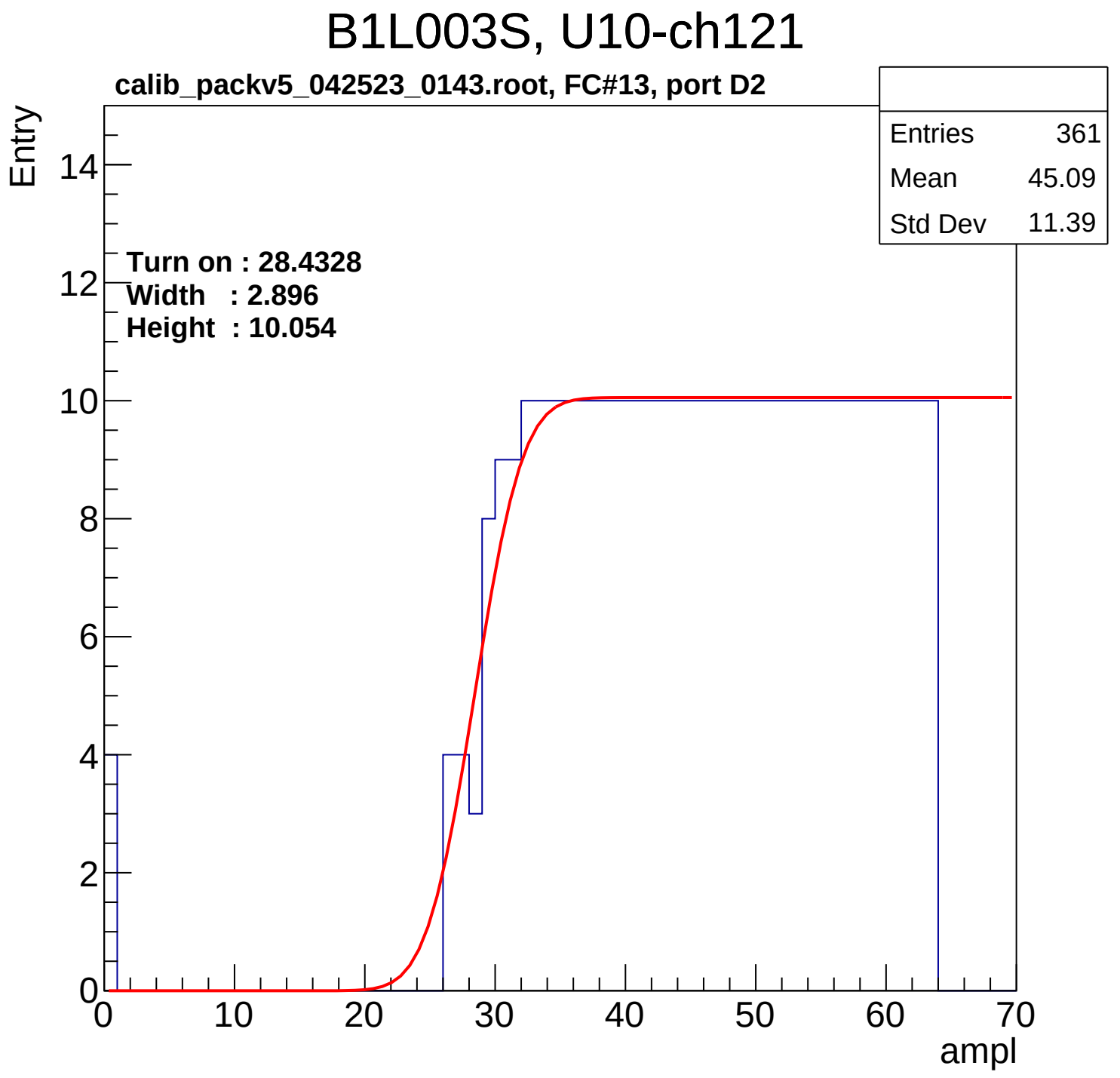

B1L003S, U10-ch116
calib_packv5_042523_0143.root, FC#13, port D2
Entries 383
Mean 43.87
Std Dev 12.26
Turn on : 26.9677
Width : 3.194
Height : 10.069
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

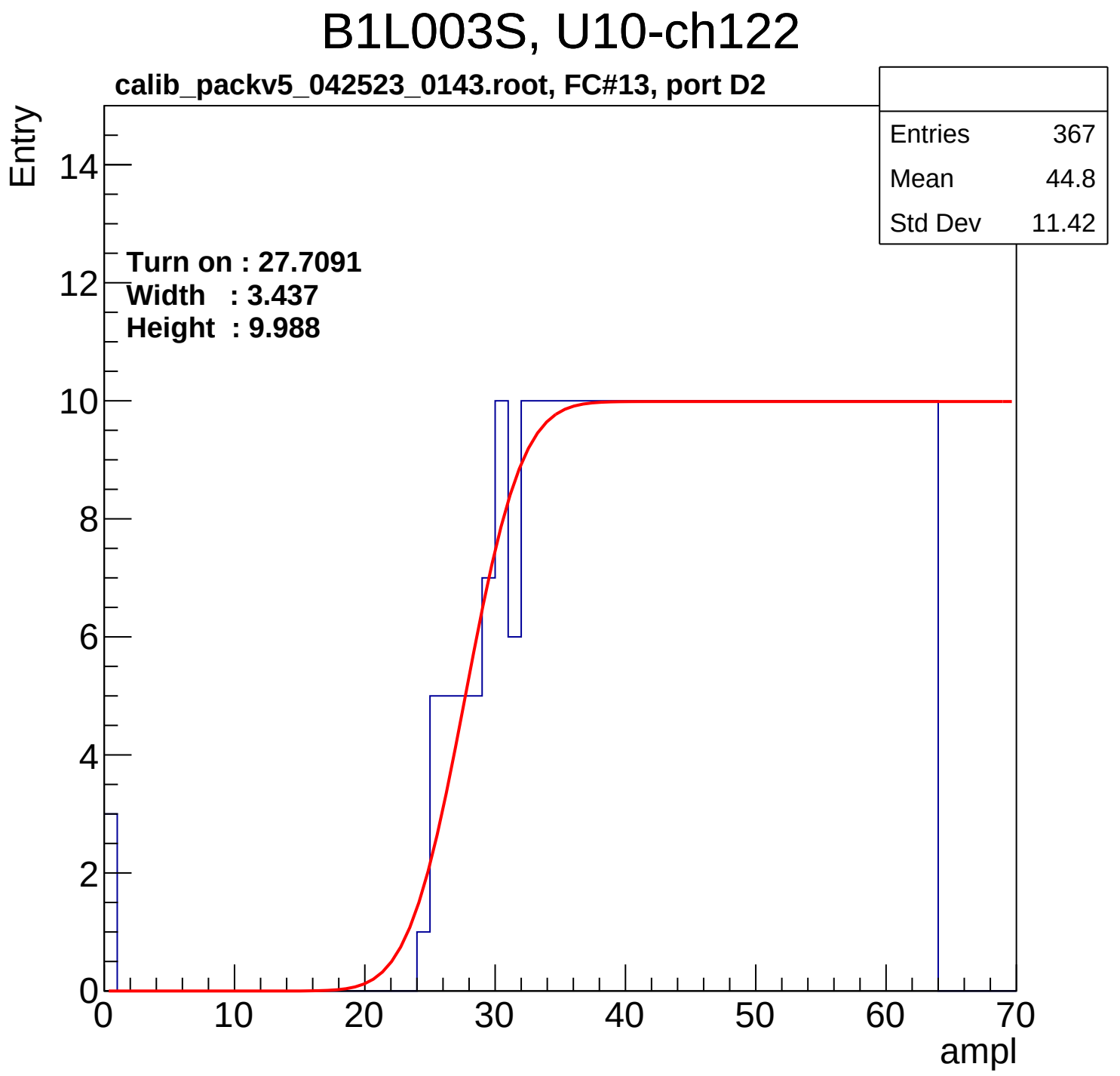

B1L003S, U10-ch117
calib_packv5_042523_0143.root, FC#13, port D2
Entries 368
Mean 44.76
Std Dev 11.43
Turn on : 27.4476
Width : 2.942
Height : 9.986
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

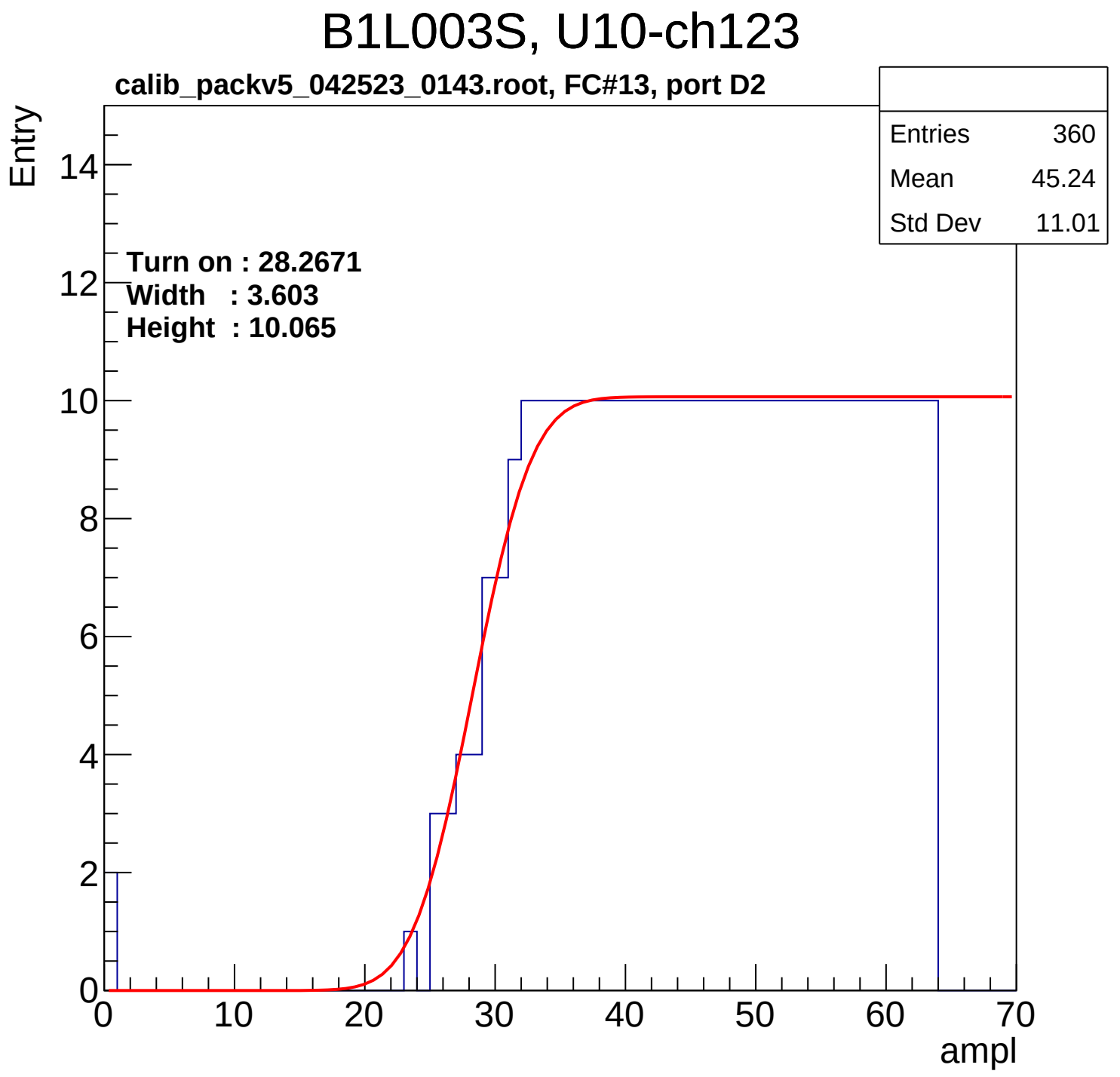

B1L003S, U10-ch118
calib_packv5_042523_0143.root, FC#13, port D2
Entries 372
Mean 44.73
Std Dev 11.11
Turn on : 26.9539
Width : 2.606
Height : 9.993
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

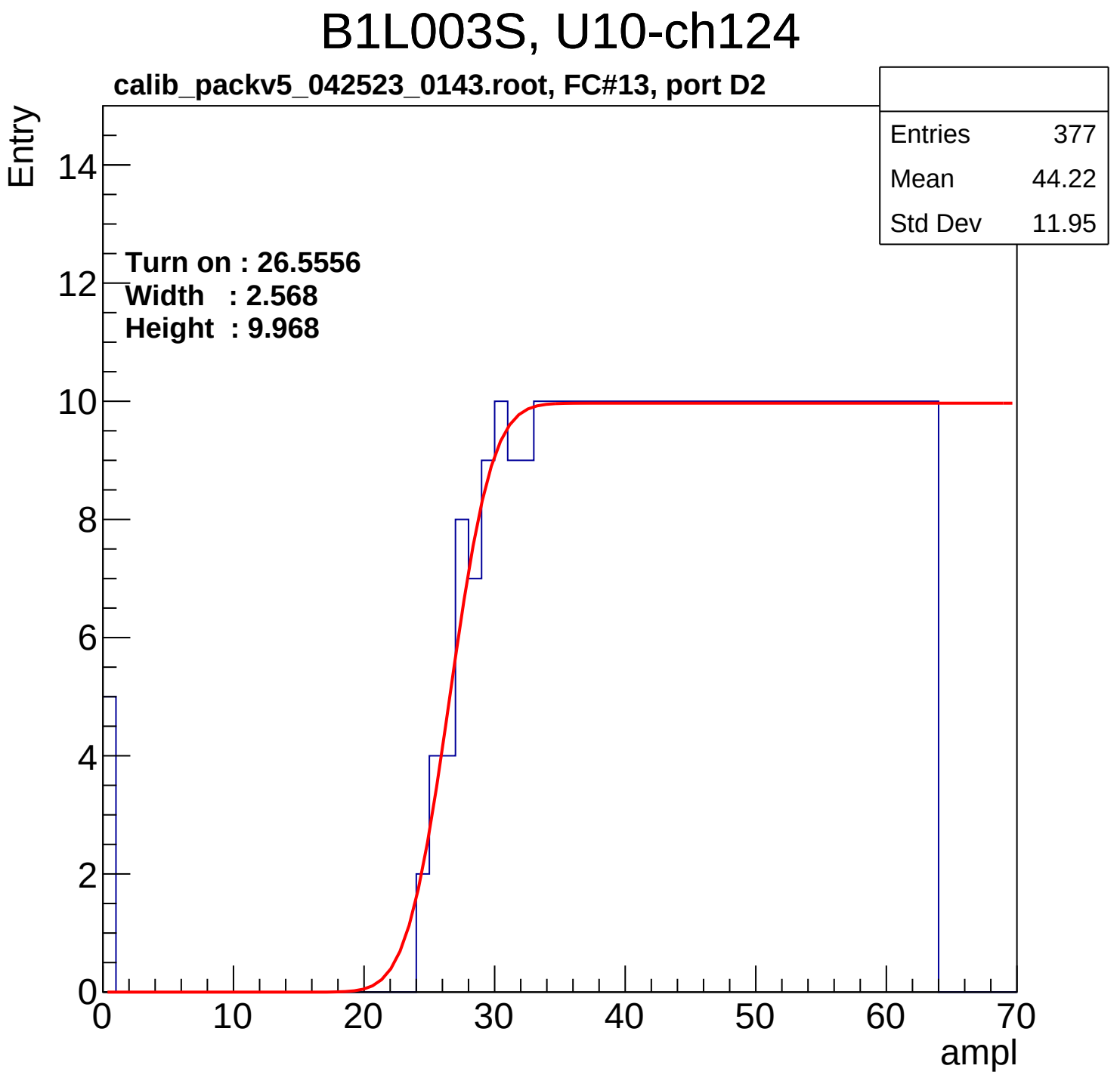

B1L003S, U10-ch119
calib_packv5_042523_0143.root, FC#13, port D2
Entries 365
Mean 44.92
Std Dev 11.36
Turn on : 28.5474
Width : 2.700
Height : 10.043
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

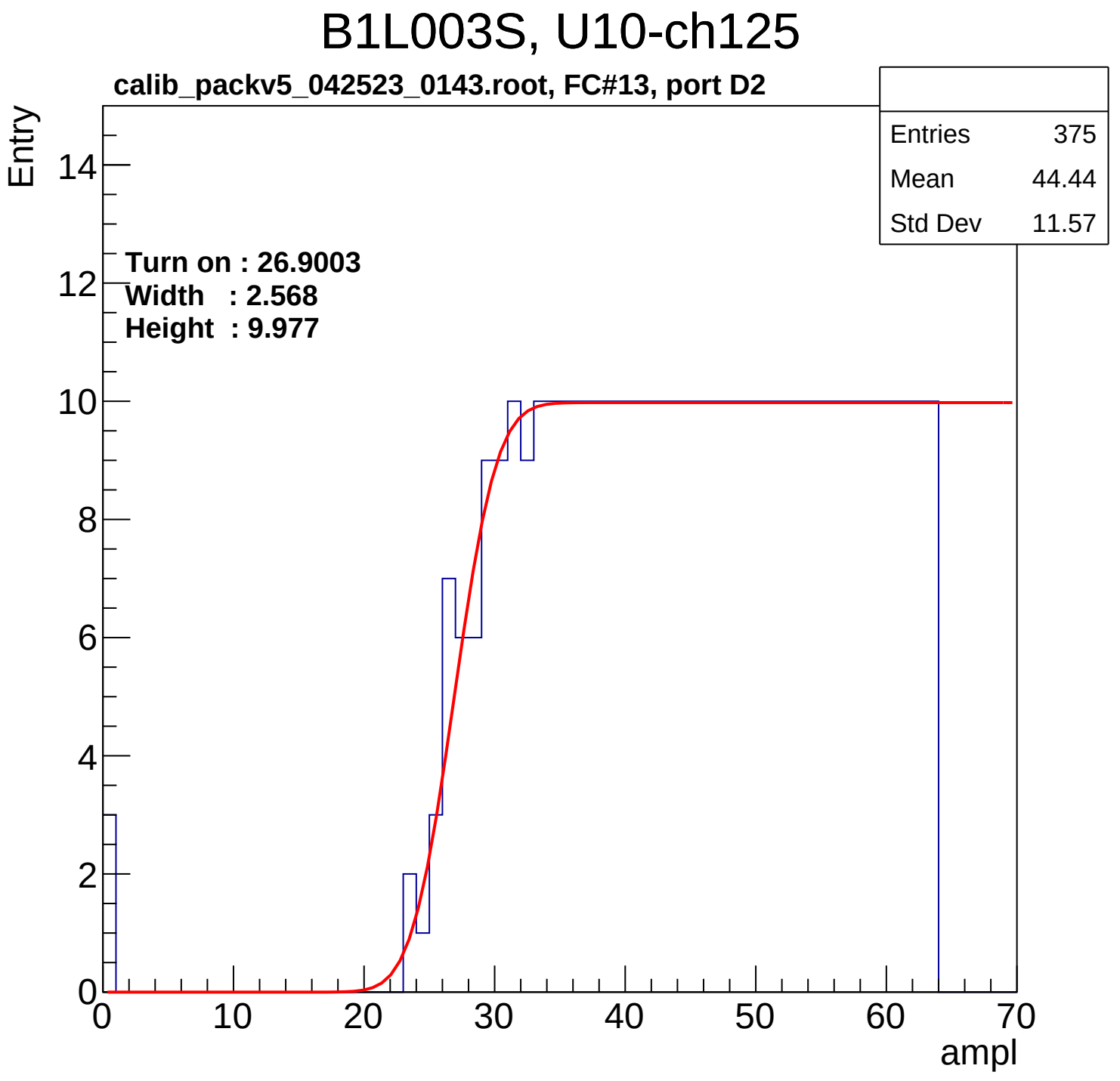

B1L003S, U10-ch120
calib_packv5_042523_0143.root, FC#13, port D2
Entries 369
Mean 44.73
Std Dev 11.44
Turn on : 27.3756
Width : 2.855
Height : 9.987
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

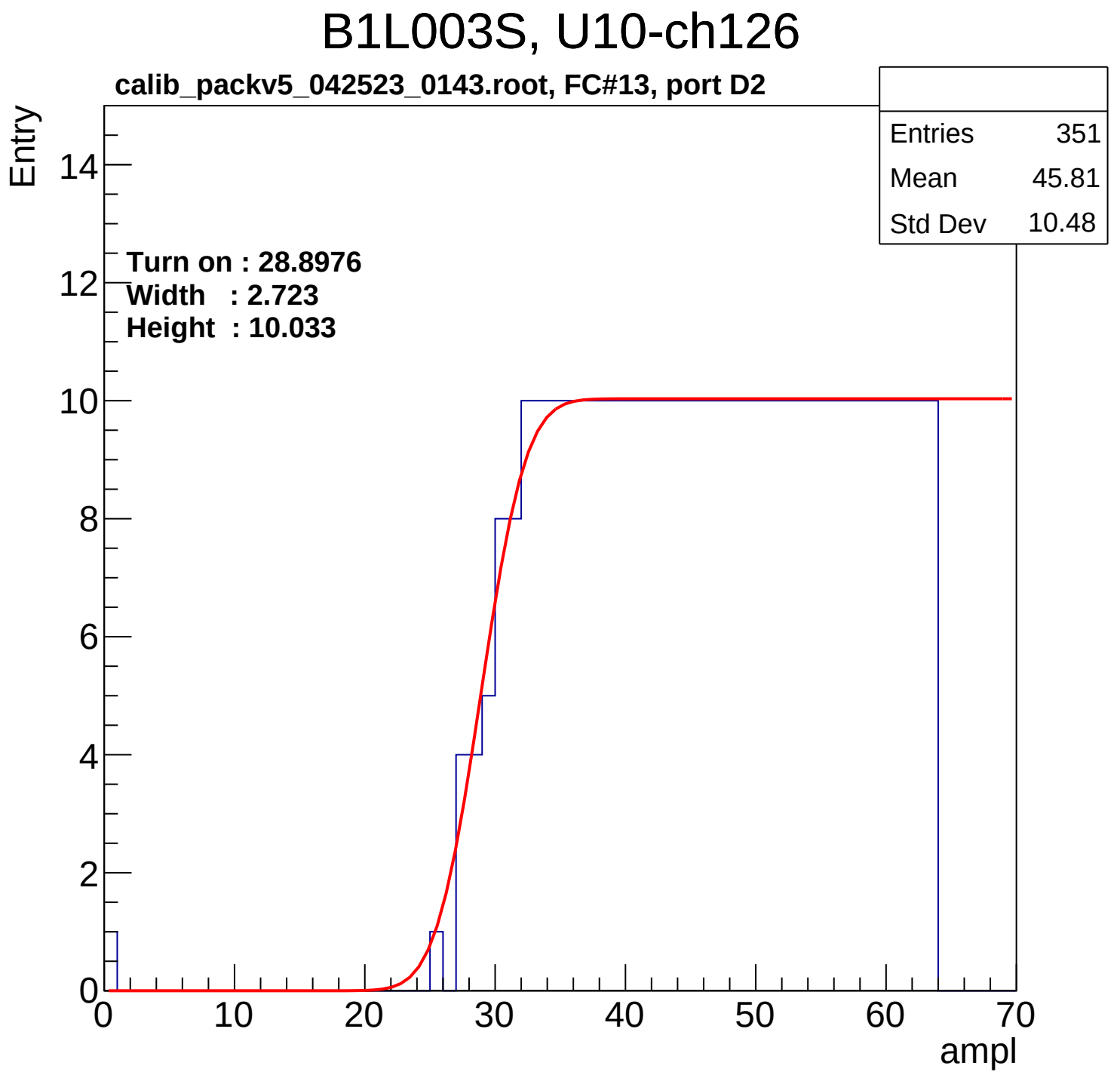

B1L003S, U10-ch121
calib_packv5_042523_0143.root, FC#13, port D2
Entries 361
Mean 45.09
Std Dev 11.39
Turn on : 28.4328
Width : 2.896
Height : 10.054
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

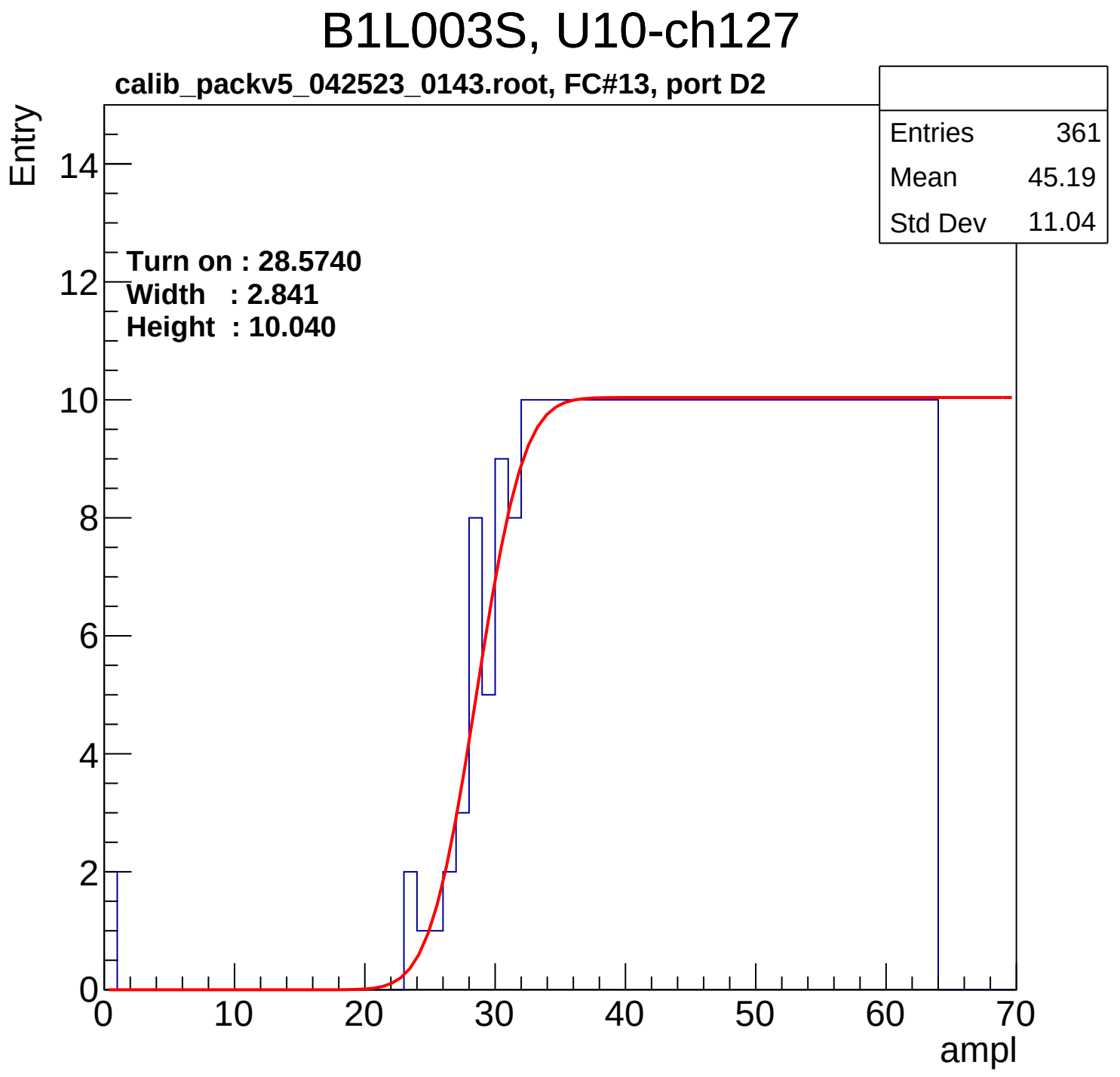

B1L003S, U10-ch122
calib_packv5_042523_0143.root, FC#13, port D2
Entries 367
Mean 44.8
Std Dev 11.42
Turn on : 27.7091
Width : 3.437
Height : 9.988
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

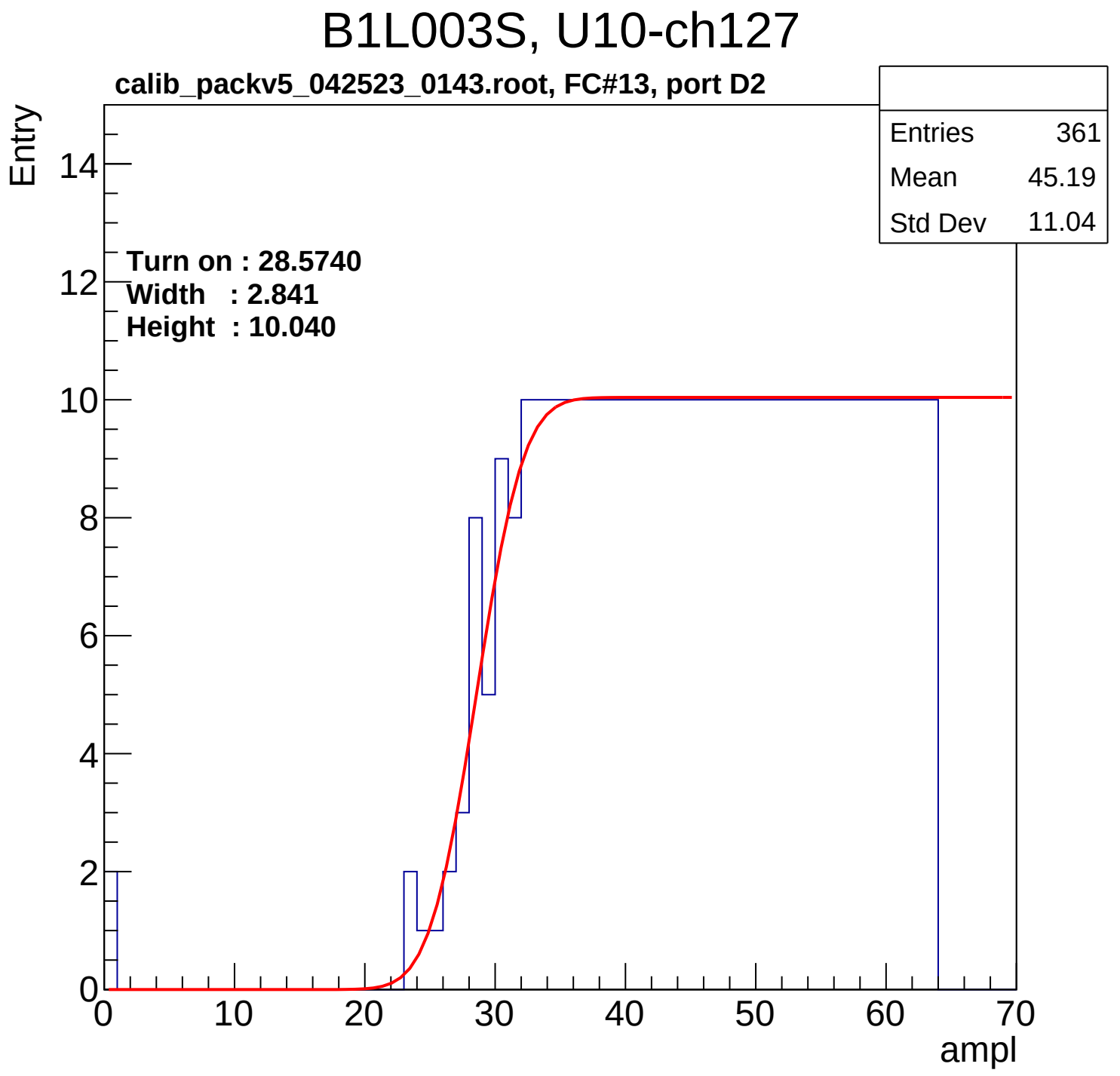

B1L003S, U10-ch123
calib_packv5_042523_0143.root, FC#13, port D2
Entries 360
Mean 45.24
Std Dev 11.01
Turn on : 28.2671
Width : 3.603
Height : 10.065
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U10-ch124
calib_packv5_042523_0143.root, FC#13, port D2
Entries 377
Mean 44.22
Std Dev 11.95
Turn on : 26.5556
Width : 2.568
Height : 9.968
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U10-ch125
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.44
Std Dev 11.57
Turn on : 26.9003
Width : 2.568
Height : 9.977
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U10-ch126
calib_packv5_042523_0143.root, FC#13, port D2
Entries 351
Mean 45.81
Std Dev 10.48
Turn on : 28.8976
Width : 2.723
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U10-ch127
calib_packv5_042523_0143.root, FC#13, port D2
Entries 361
Mean 45.19
Std Dev 11.04
Turn on : 28.5740
Width : 2.841
Height : 10.040
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U10-ch127
calib_packv5_042523_0143.root, FC#13, port D2
Entries 361
Mean 45.19
Std Dev 11.04
Turn on : 28.5740
Width : 2.841
Height : 10.040
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70