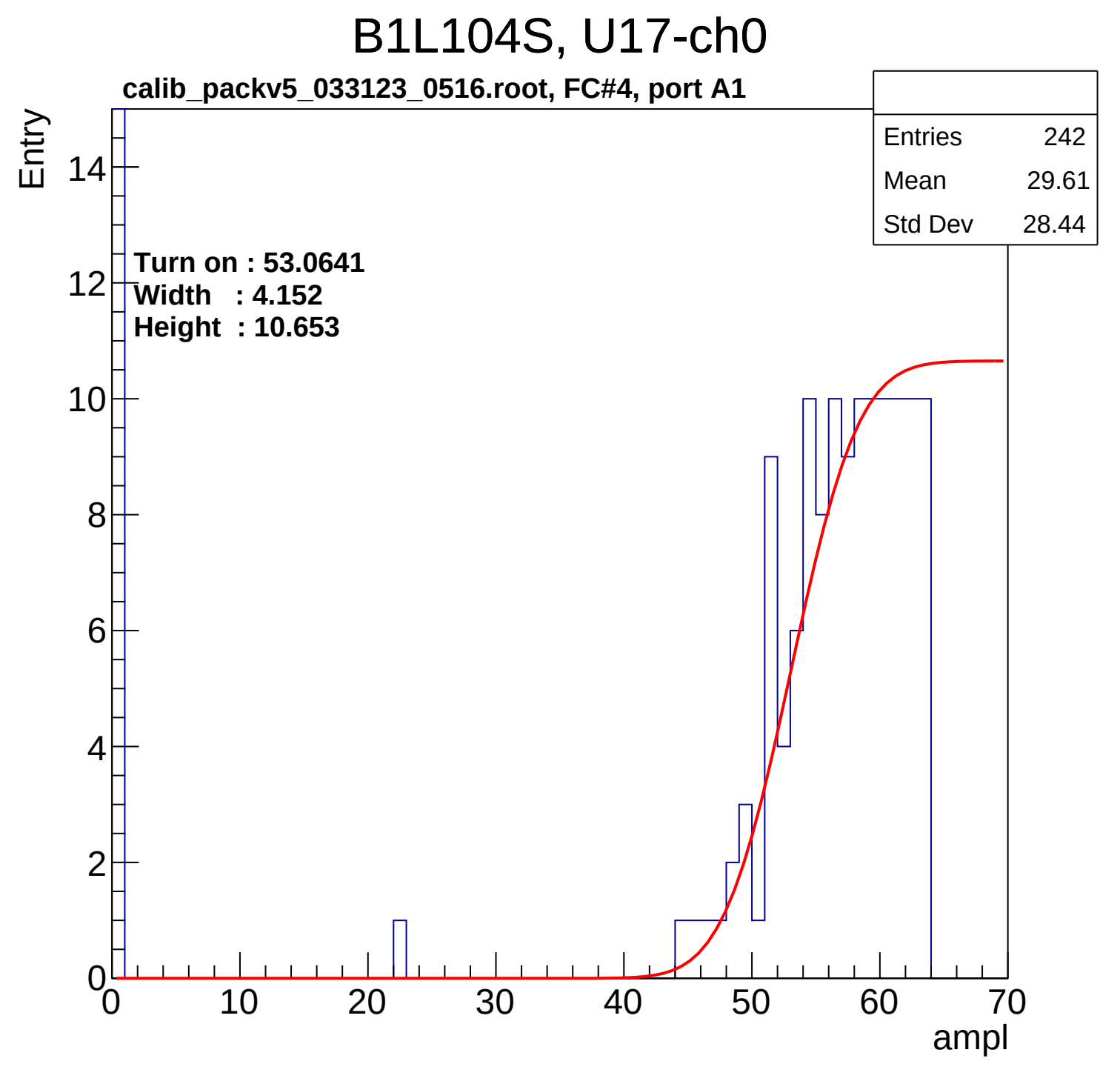
B1L104S, U17-ch0
calib_packv5_033123_0516.root, FC#4, port A1
Entries 242
Mean 29.61
Std Dev 28.44
Turn on : 53.0641
Width : 4.152
Height : 10.653
Entry
ampl
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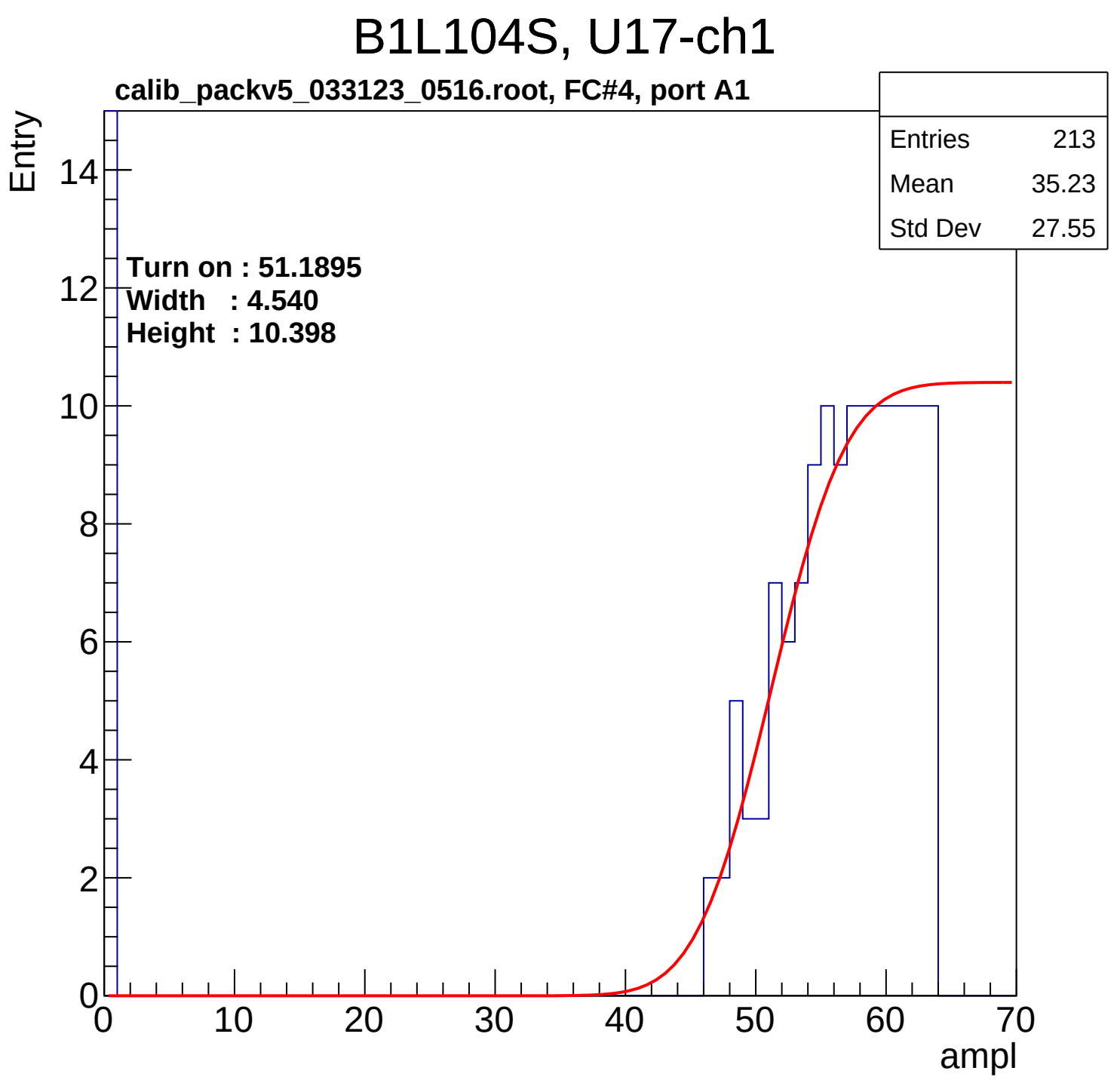
B1L104S, U17-ch1
calib_packv5_033123_0516.root, FC#4, port A1
Entries 213
Mean 35.23
Std Dev 27.55
Turn on : 51.1895
Width : 4.540
Height : 10.398
Entry
ampl
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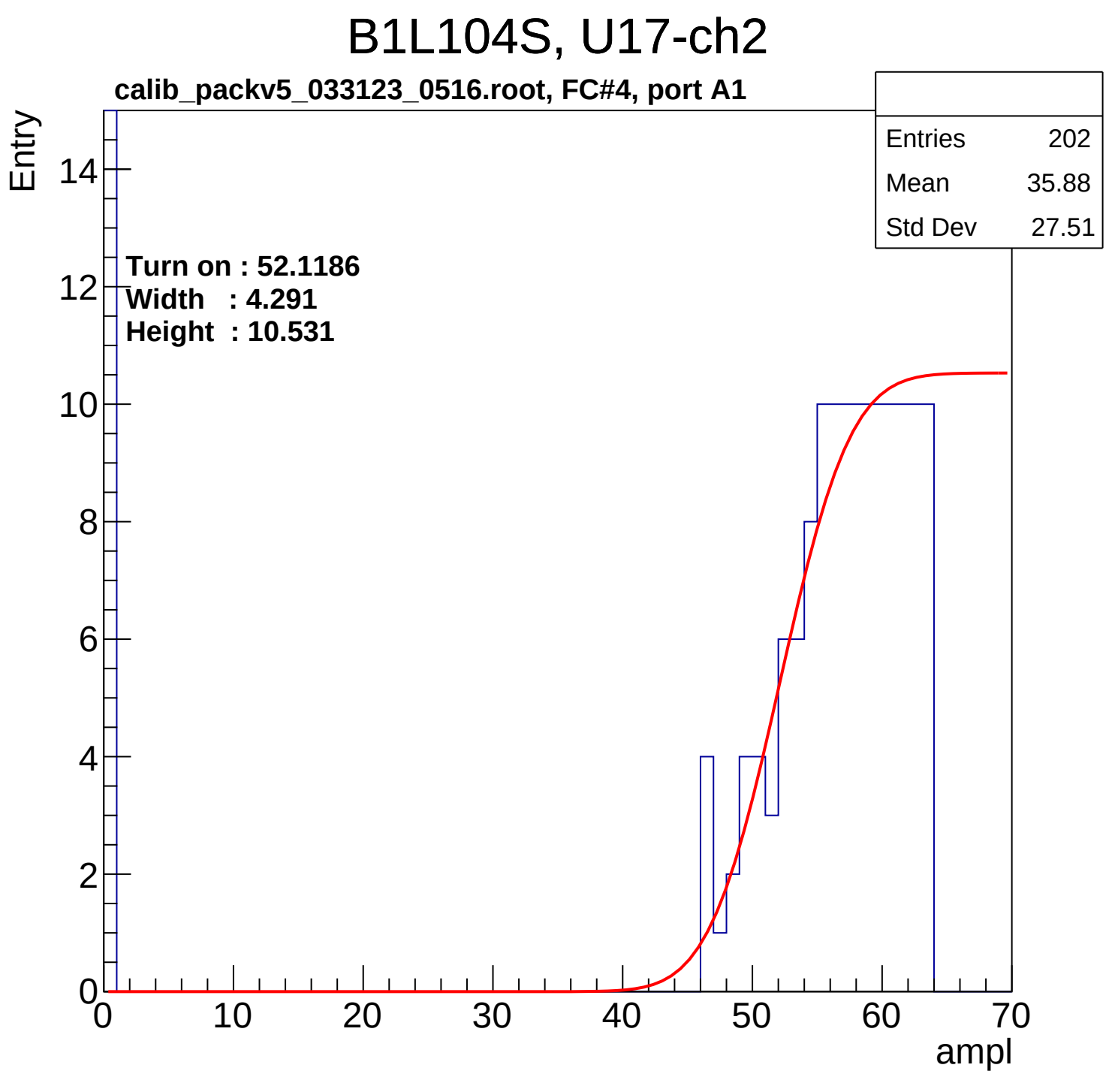
B1L104S, U17-ch2
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 35.88
Std Dev 27.51
Turn on : 52.1186
Width : 4.291
Height : 10.531
Entry
ampl
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6
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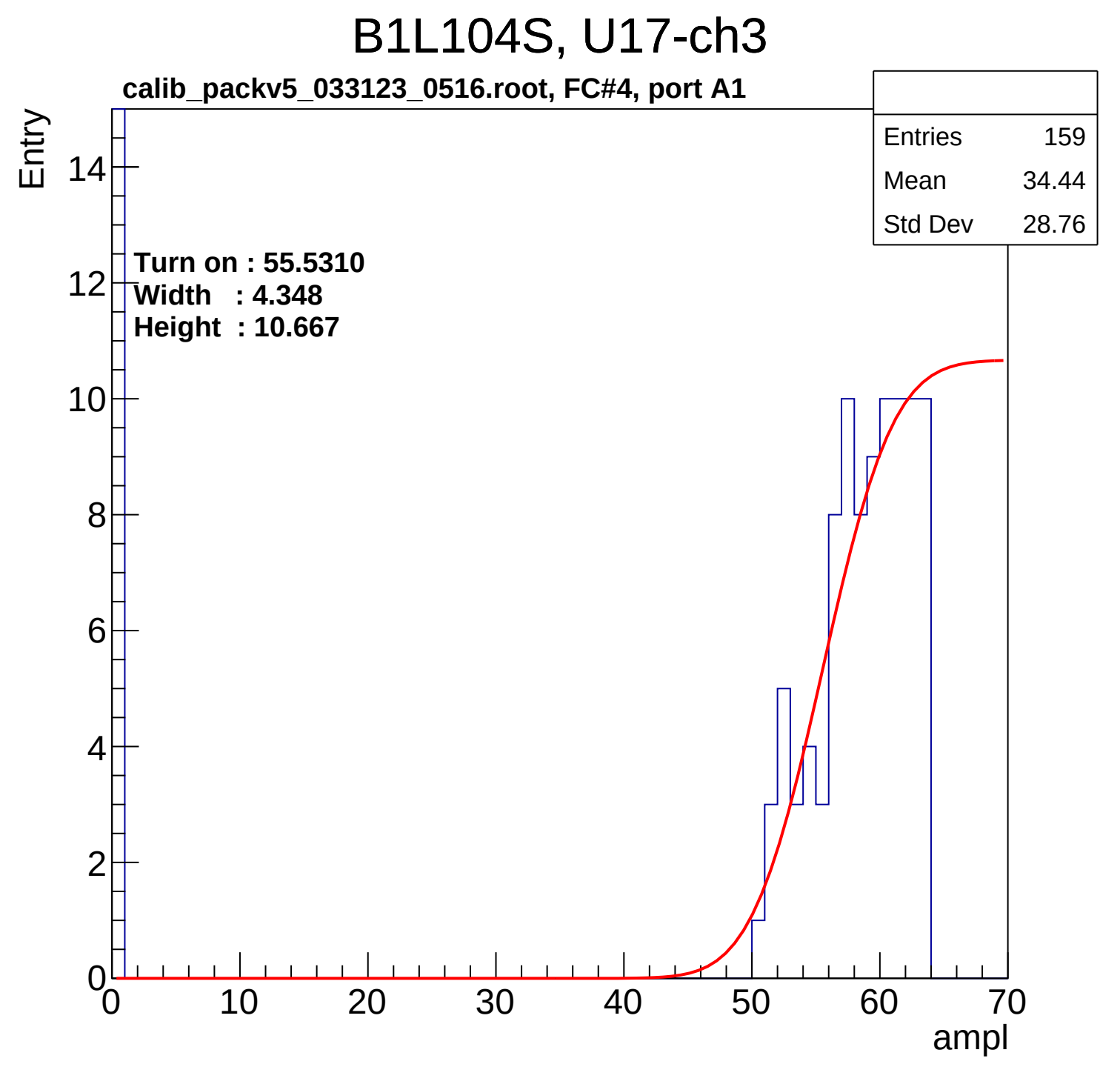
B1L104S, U17-ch3
calib_packv5_033123_0516.root, FC#4, port A1
Entries 159
Mean 34.44
Std Dev 28.76
Turn on : 55.5310
Width : 4.348
Height : 10.667
Entry
ampl
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2
4
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8
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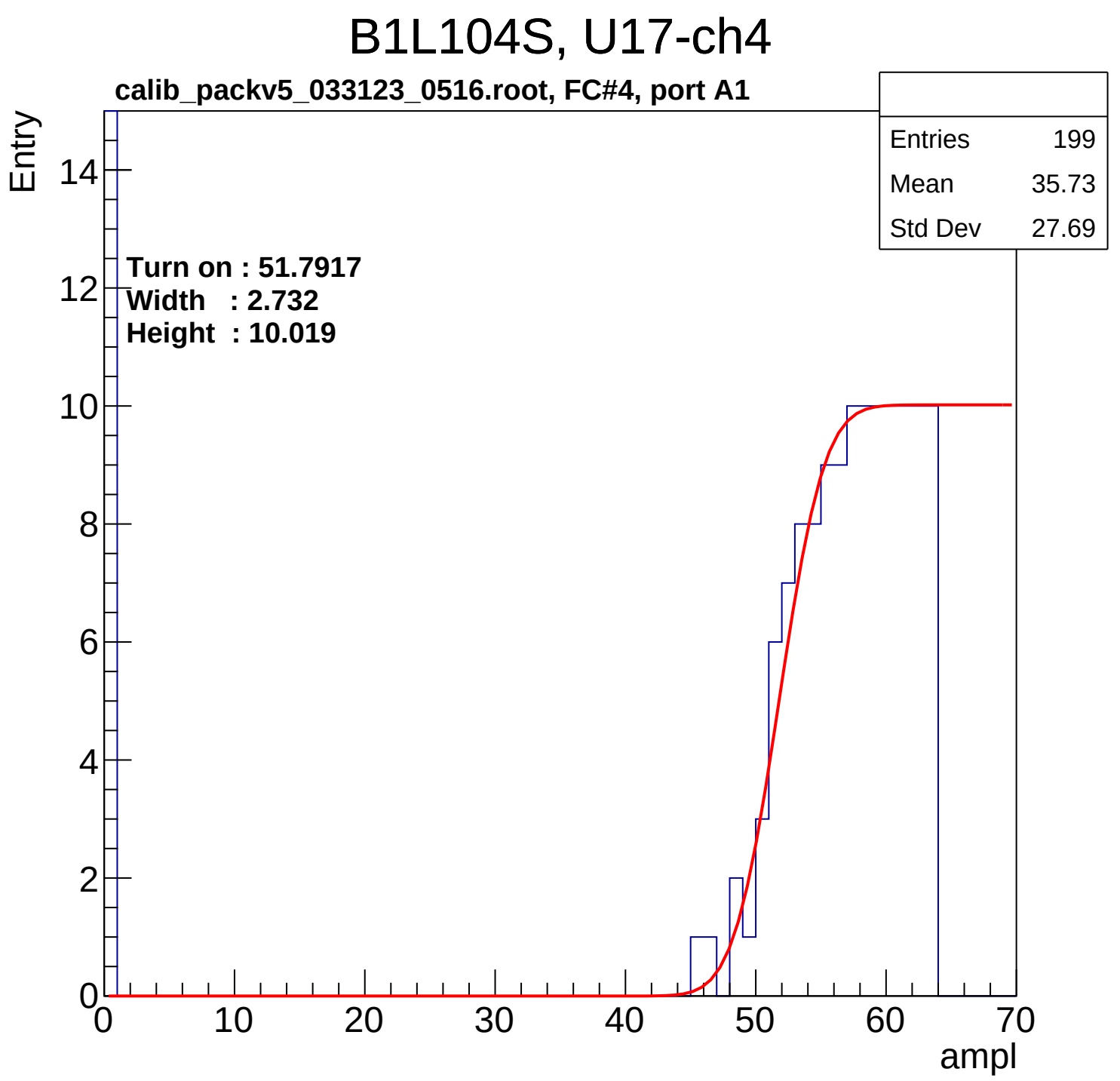
B1L104S, U17-ch4
calib_packv5_033123_0516.root, FC#4, port A1
Entries 199
Mean 35.73
Std Dev 27.69
Turn on : 51.7917
Width : 2.732
Height : 10.019
Entry
ampl
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2
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6
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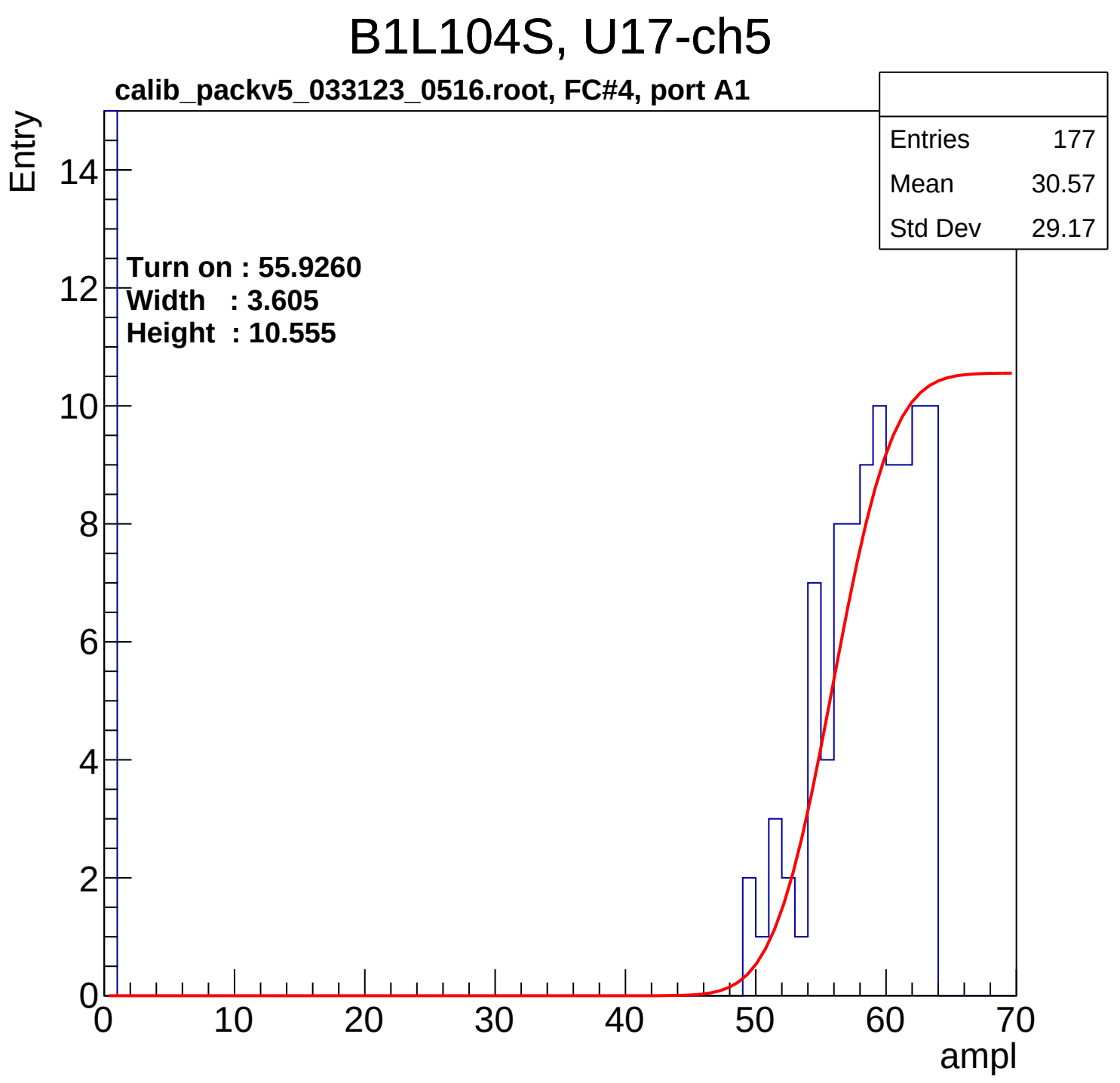
B1L104S, U17-ch5
calib_packv5_033123_0516.root, FC#4, port A1
Entries 177
Mean 30.57
Std Dev 29.17
Turn on : 55.9260
Width : 3.605
Height : 10.555
Entry
ampl
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2
4
6
8
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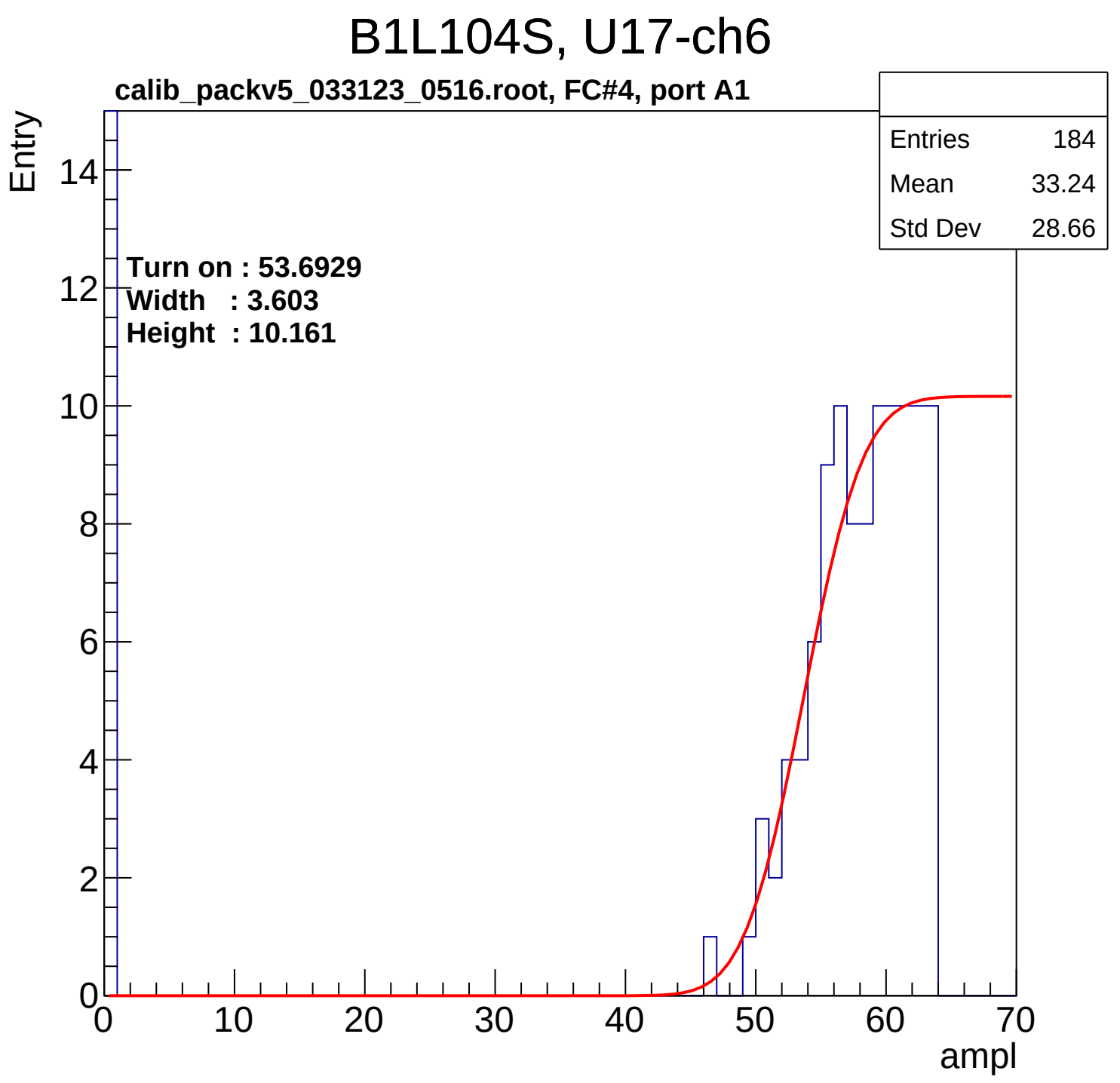
B1L104S, U17-ch6
calib_packv5_033123_0516.root, FC#4, port A1
Entries 184
Mean 33.24
Std Dev 28.66
Turn on : 53.6929
Width : 3.603
Height : 10.161
Entry
ampl
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2
4
6
8
10
12
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0
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60
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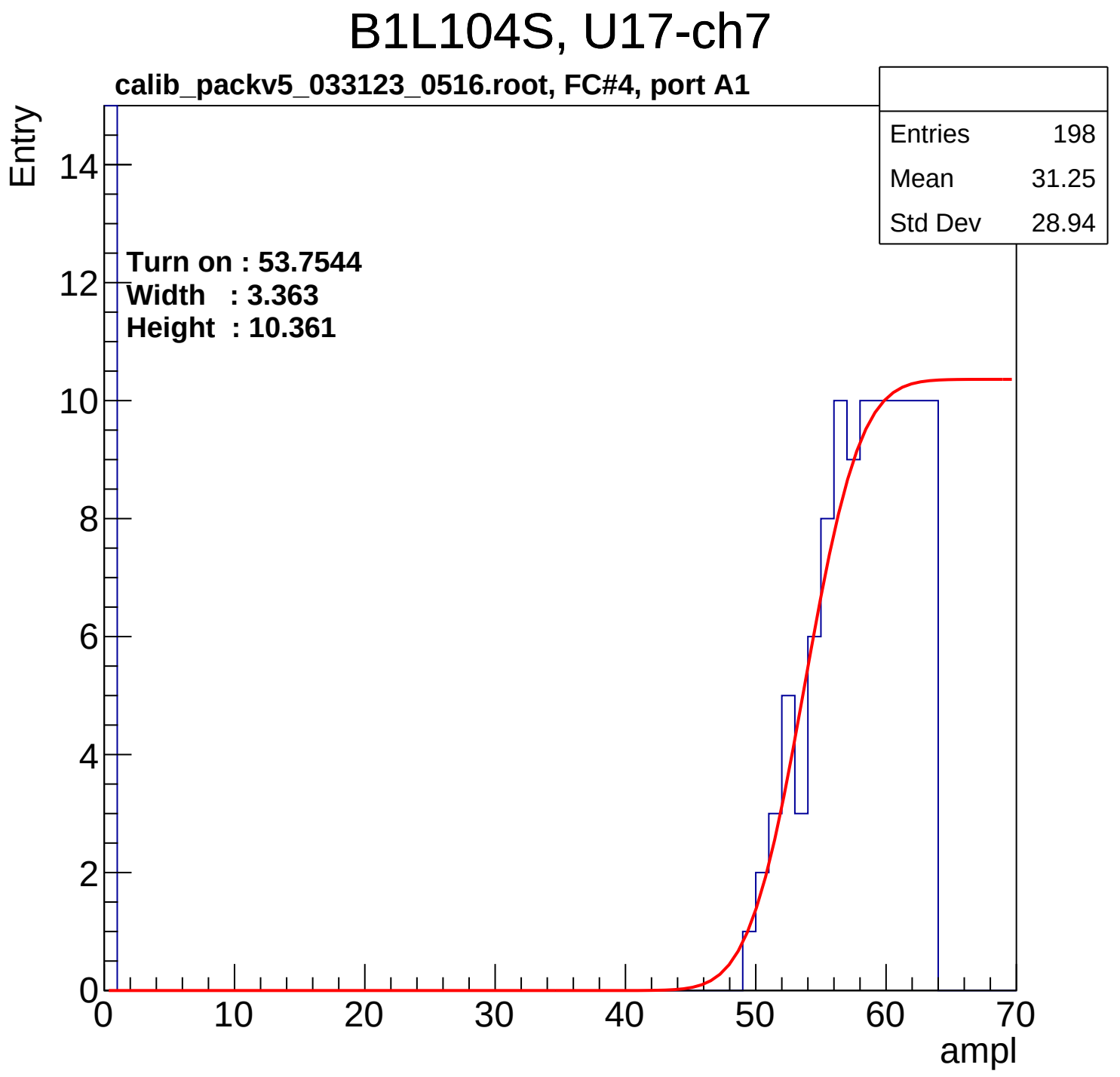
B1L104S, U17-ch7
calib_packv5_033123_0516.root, FC#4, port A1
Entries 198
Mean 31.25
Std Dev 28.94
Turn on : 53.7544
Width : 3.363
Height : 10.361
Entry
ampl
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6
8
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0
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60
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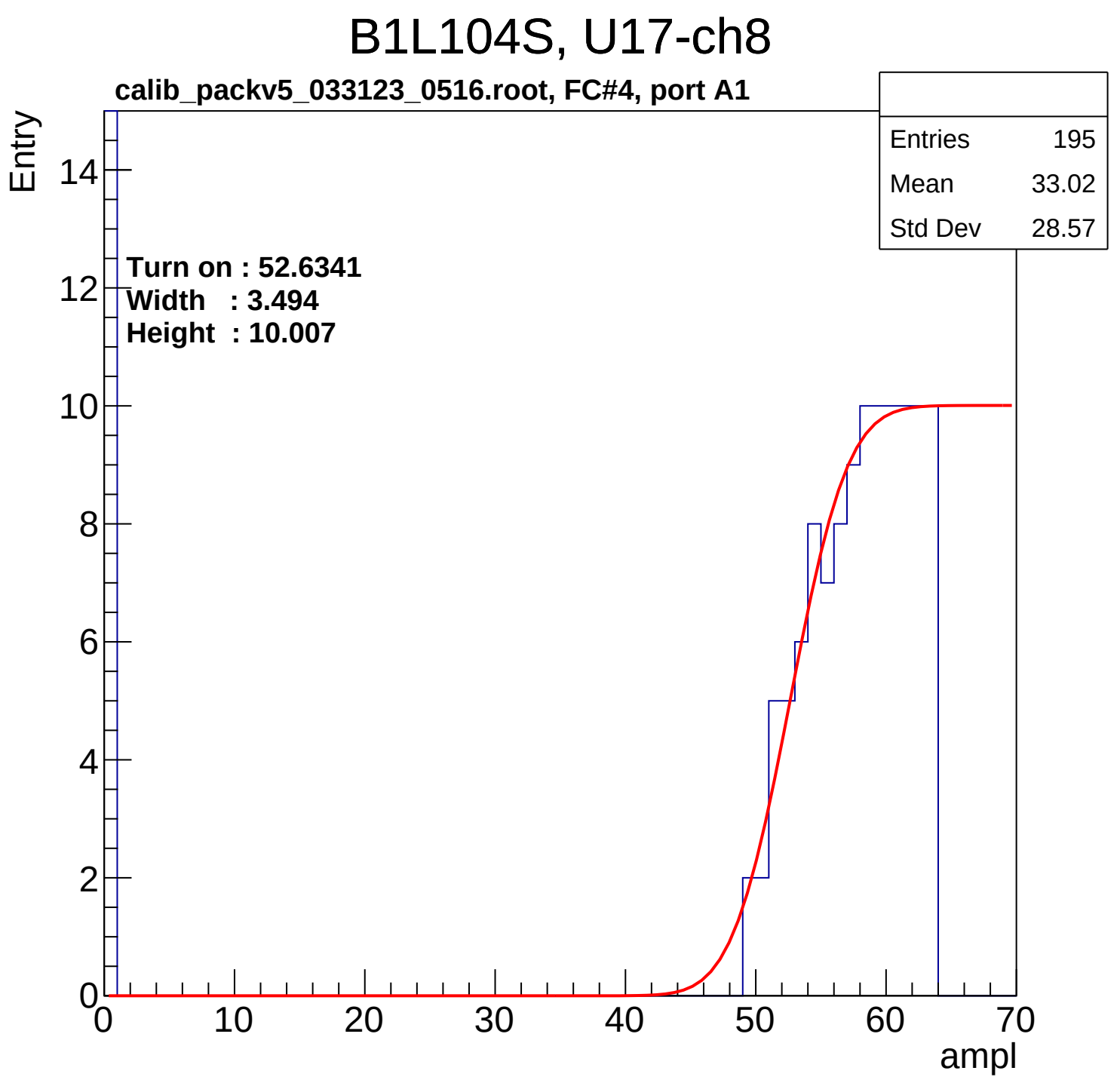
B1L104S, U17-ch8
calib_packv5_033123_0516.root, FC#4, port A1
Entries 195
Mean 33.02
Std Dev 28.57
Turn on : 52.6341
Width : 3.494
Height : 10.007
Entry
ampl
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2
4
6
8
10
12
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0
10
20
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60
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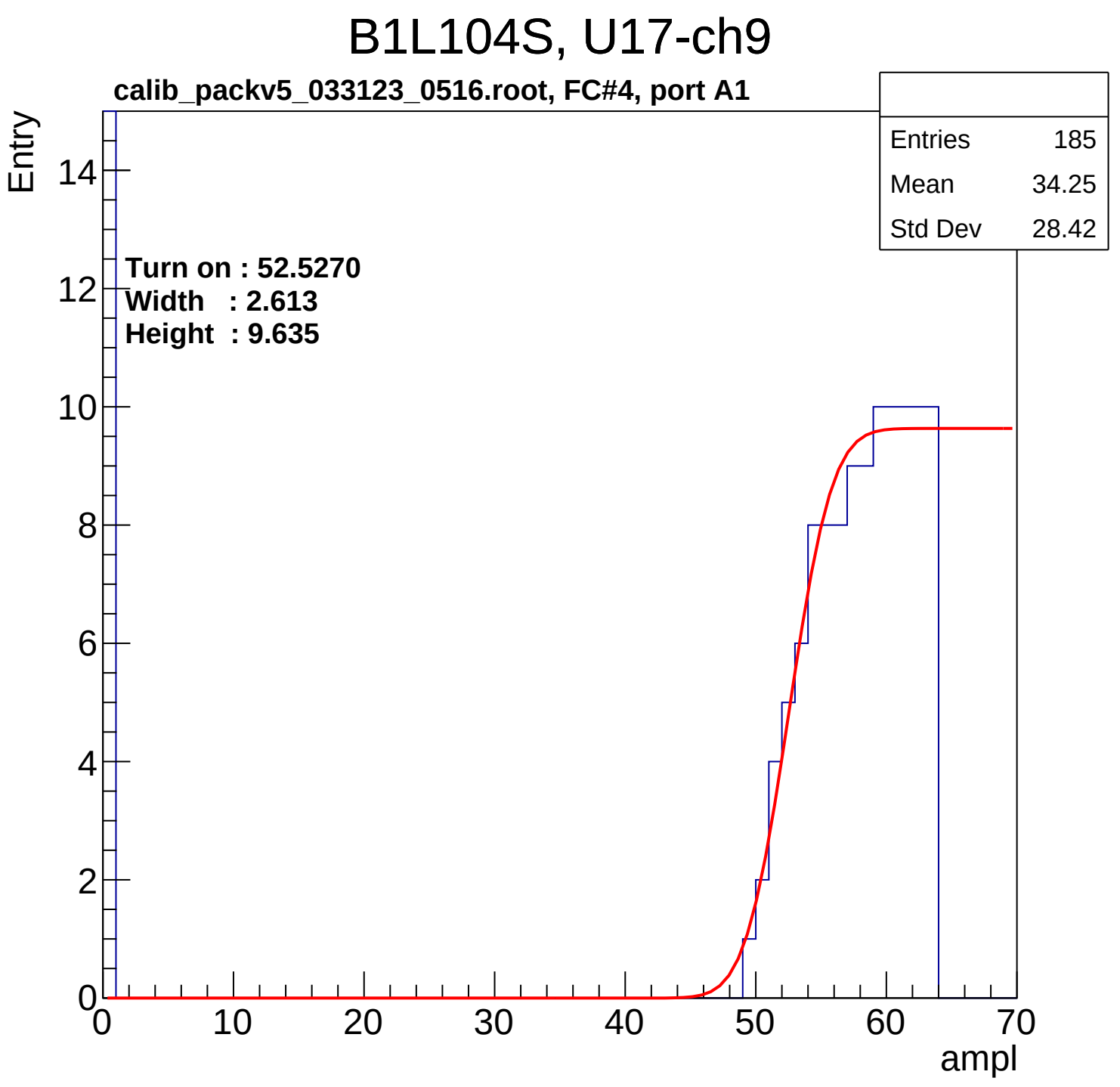
B1L104S, U17-ch9
calib_packv5_033123_0516.root, FC#4, port A1
Entries 185
Mean 34.25
Std Dev 28.42
Turn on : 52.5270
Width : 2.613
Height : 9.635
Entry
ampl
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2
4
6
8
10
12
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0
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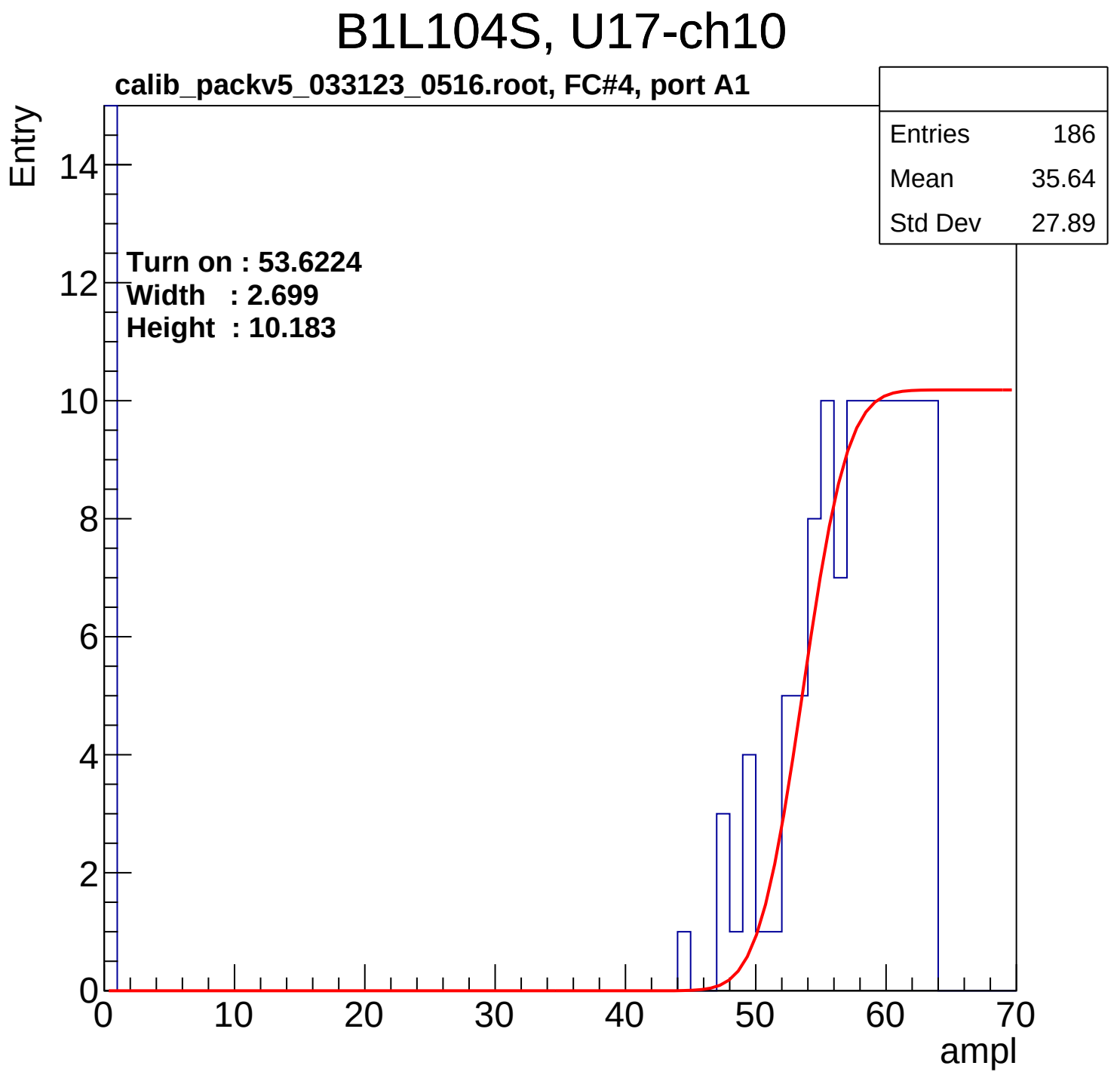
B1L104S, U17-ch10
calib_packv5_033123_0516.root, FC#4, port A1
Entries 186
Mean 35.64
Std Dev 27.89
Turn on : 53.6224
Width : 2.699
Height : 10.183
Entry
ampl
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6
8
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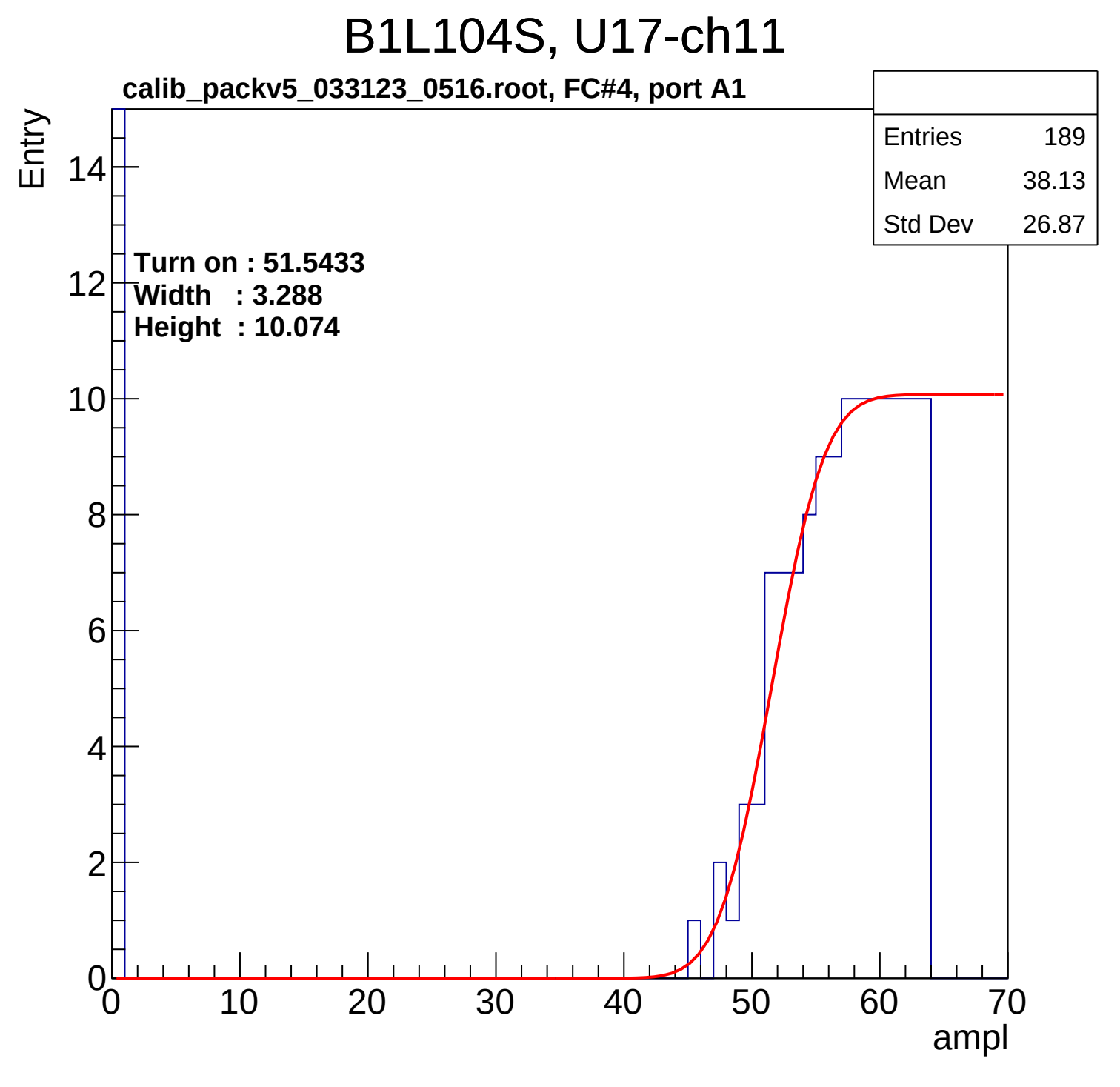
B1L104S, U17-ch11
calib_packv5_033123_0516.root, FC#4, port A1
Entries 189
Mean 38.13
Std Dev 26.87
Turn on : 51.5433
Width : 3.288
Height : 10.074
Entry
ampl
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6
8
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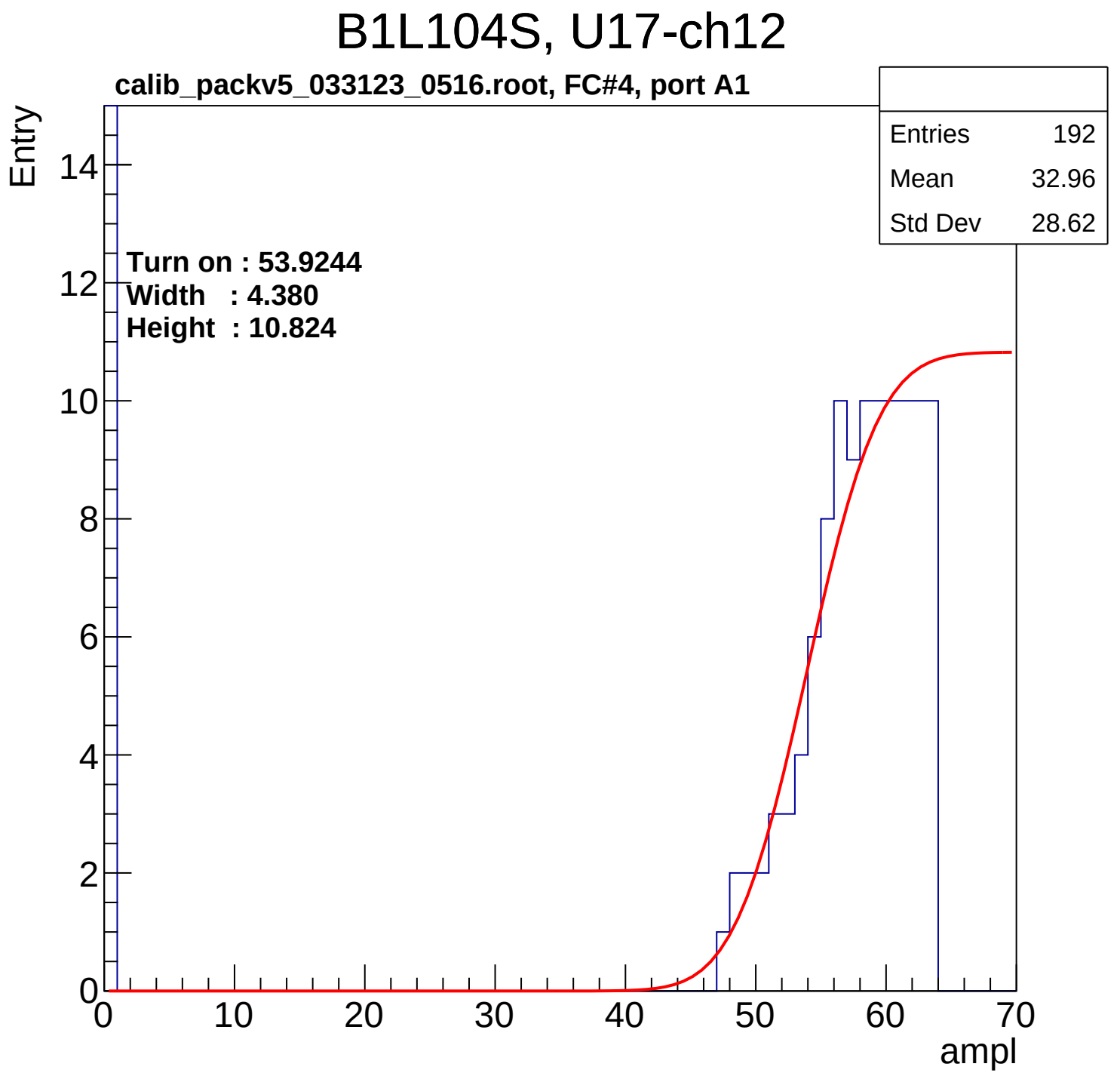
B1L104S, U17-ch12
calib_packv5_033123_0516.root, FC#4, port A1
Entries 192
Mean 32.96
Std Dev 28.62
Turn on : 53.9244
Width : 4.380
Height : 10.824
Entry
ampl
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6
8
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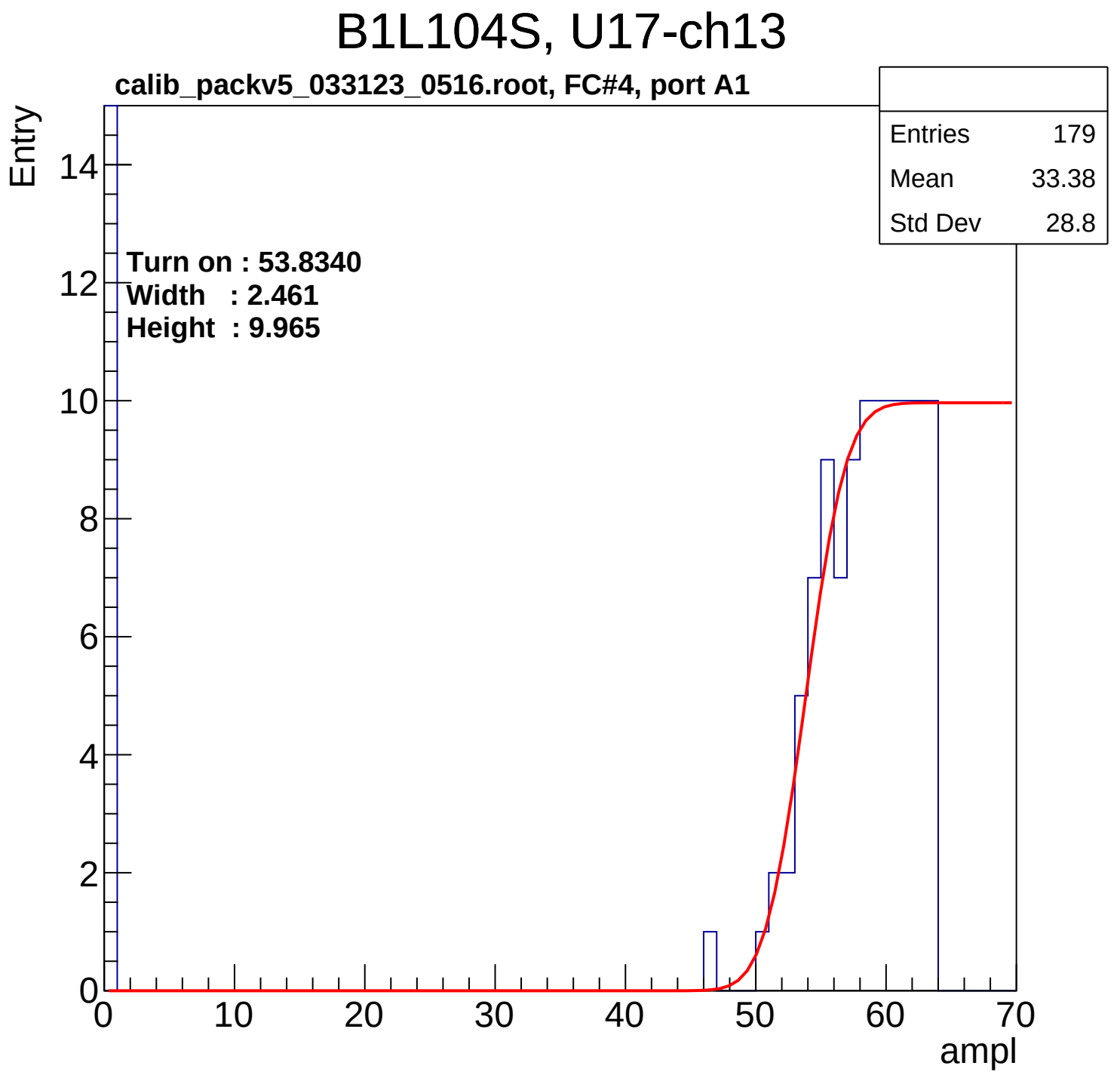
B1L104S, U17-ch13
calib_packv5_033123_0516.root, FC#4, port A1
Entries 179
Mean 33.38
Std Dev 28.8
Turn on : 53.8340
Width : 2.461
Height : 9.965
Entry
ampl
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6
8
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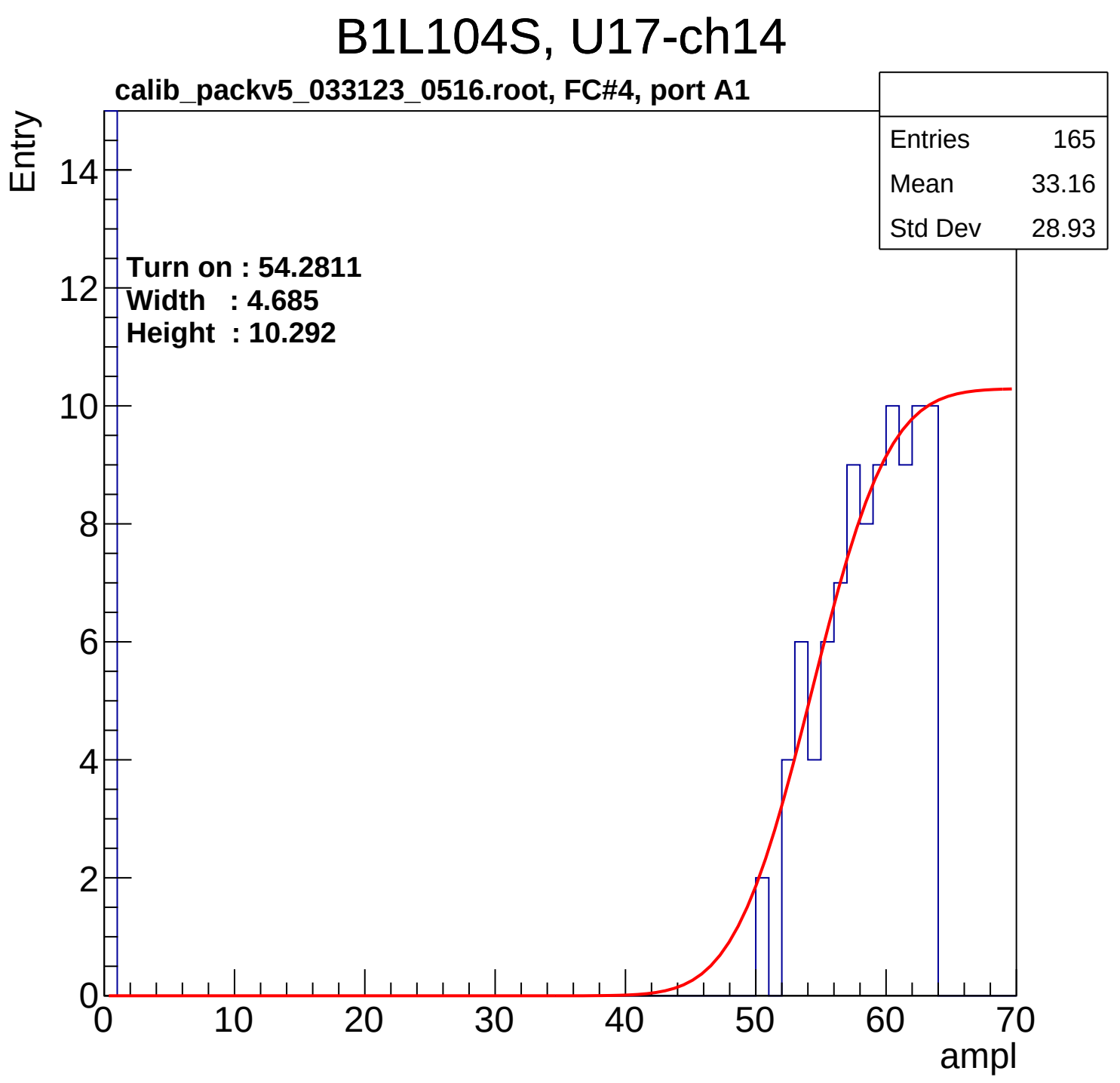
B1L104S, U17-ch14
calib_packv5_033123_0516.root, FC#4, port A1
Entries 165
Mean 33.16
Std Dev 28.93
Turn on : 54.2811
Width : 4.685
Height : 10.292
Entry
ampl
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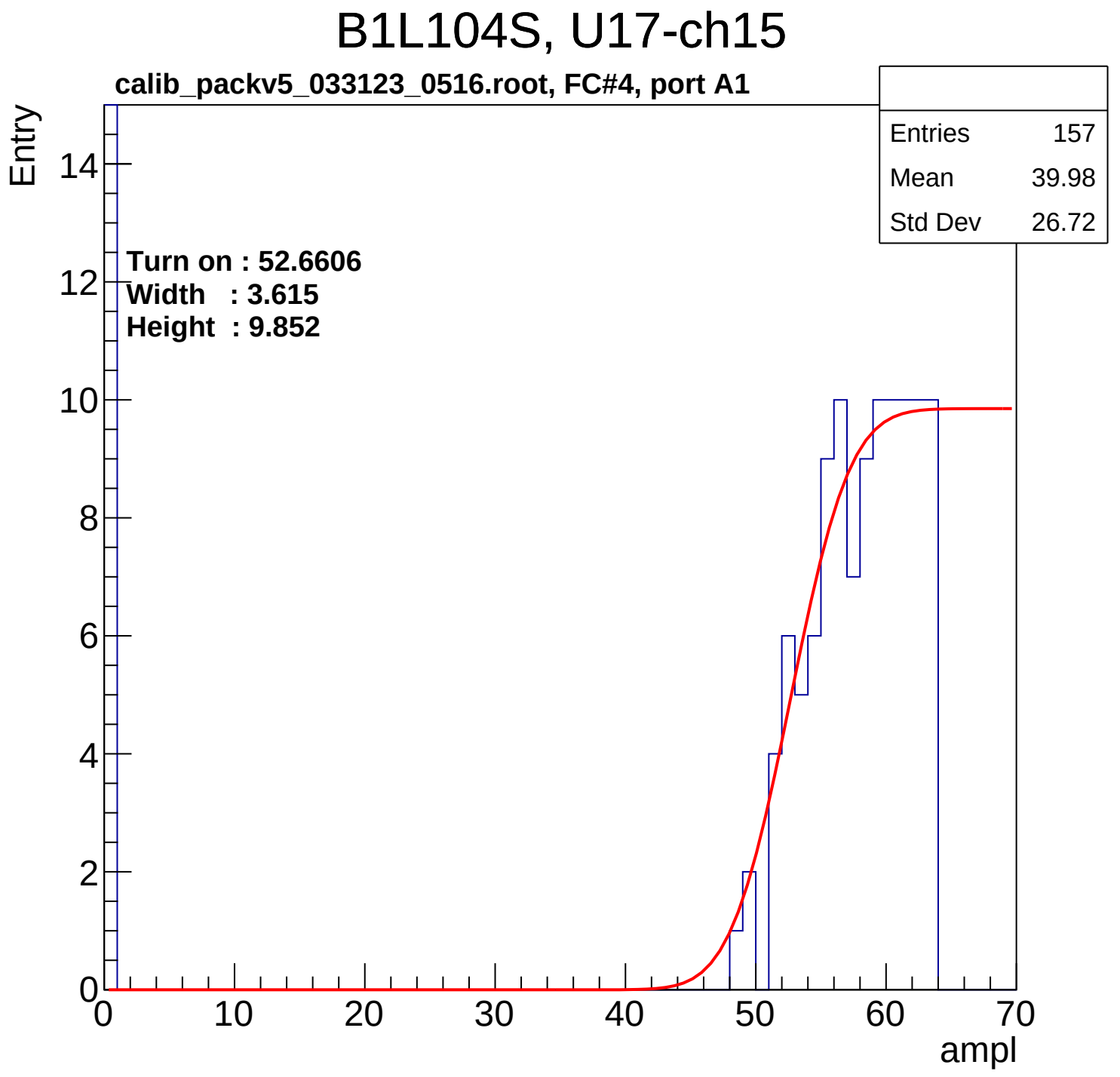
B1L104S, U17-ch15
calib_packv5_033123_0516.root, FC#4, port A1
Entries 157
Mean 39.98
Std Dev 26.72
Turn on : 52.6606
Width : 3.615
Height : 9.852
Entry
ampl
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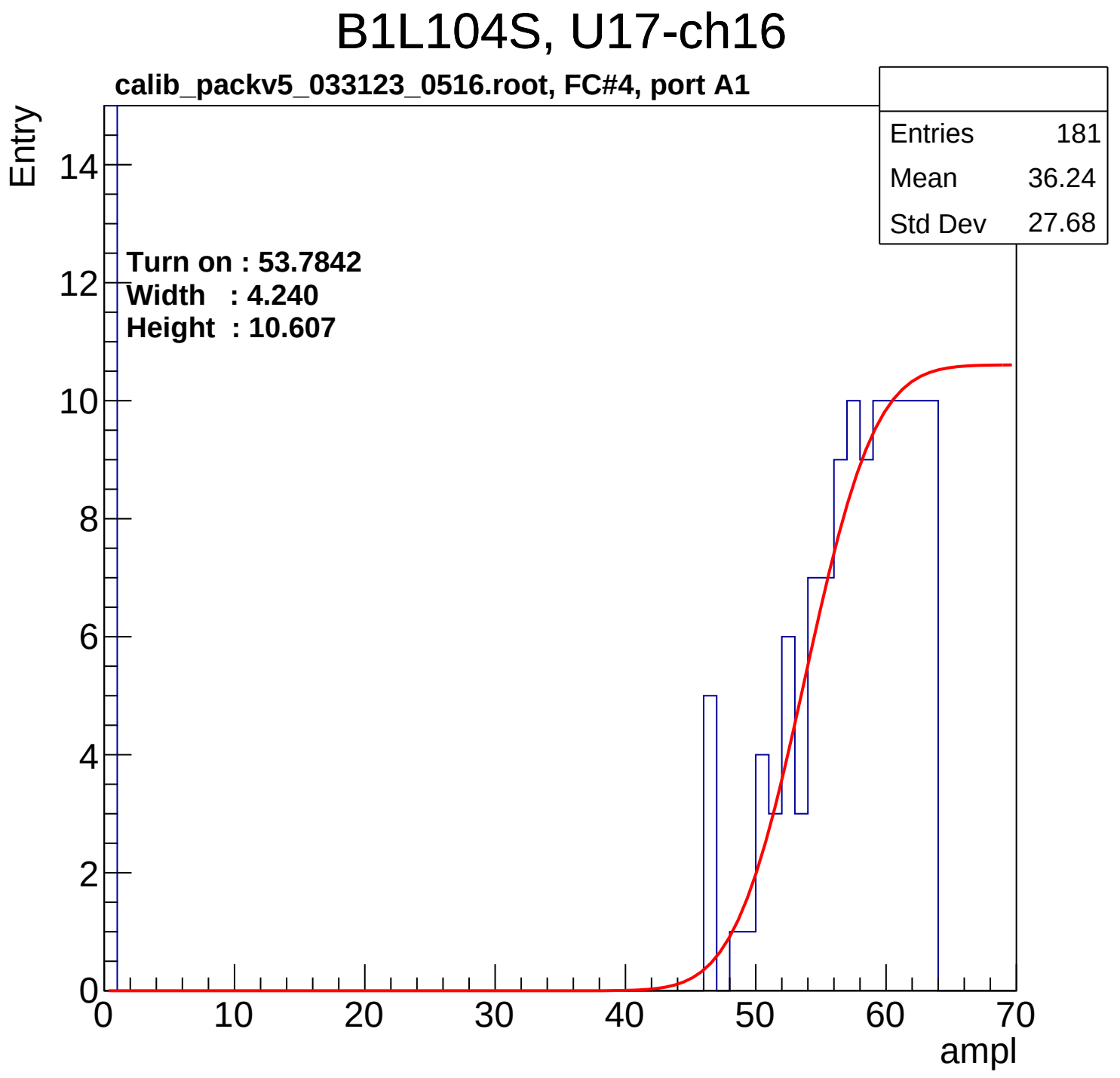
B1L104S, U17-ch16
calib_packv5_033123_0516.root, FC#4, port A1
Entries 181
Mean 36.24
Std Dev 27.68
Turn on : 53.7842
Width : 4.240
Height : 10.607
Entry
ampl
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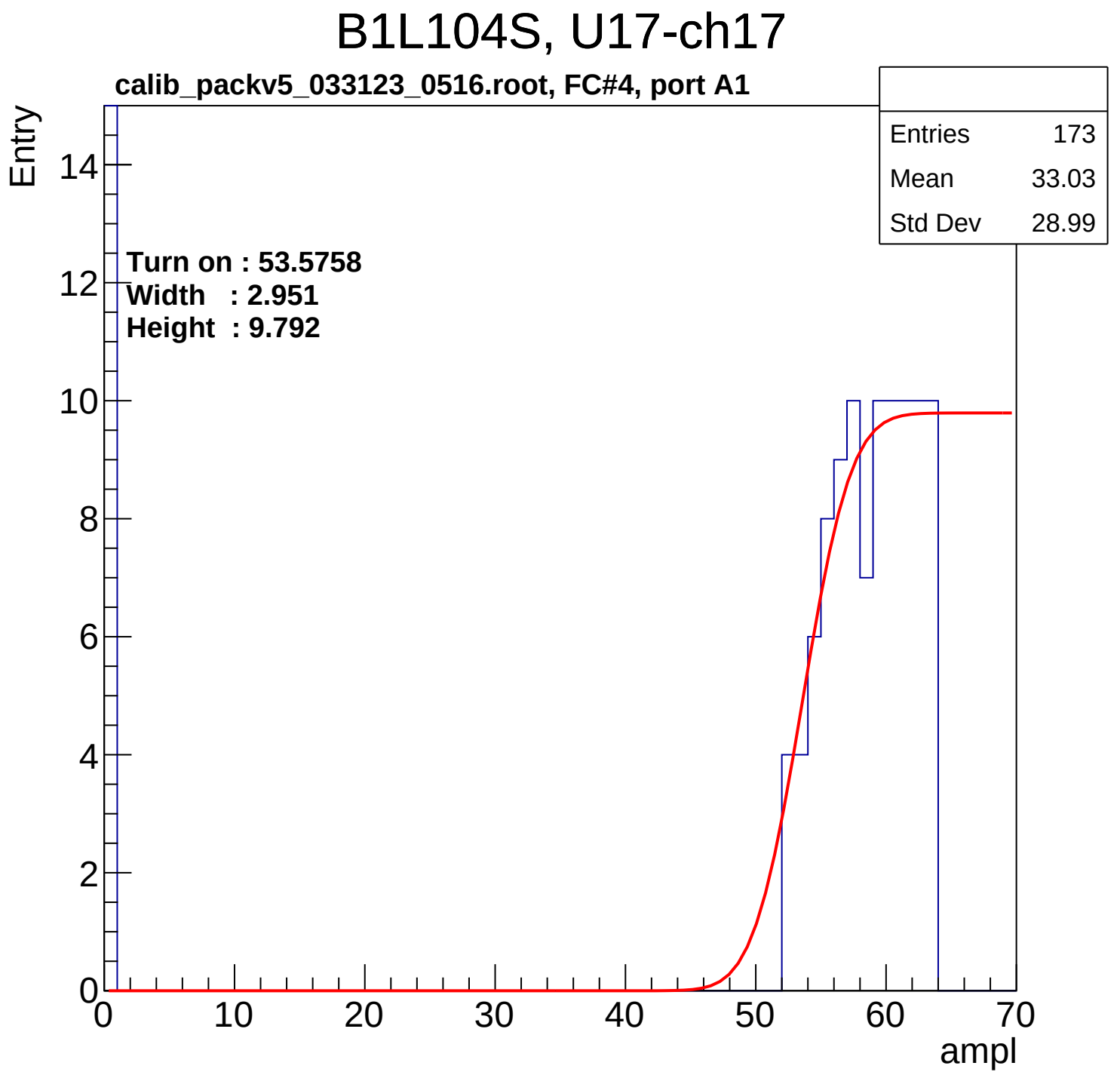
B1L104S, U17-ch17
calib_packv5_033123_0516.root, FC#4, port A1
Entries 173
Mean 33.03
Std Dev 28.99
Turn on : 53.5758
Width : 2.951
Height : 9.792
Entry
ampl
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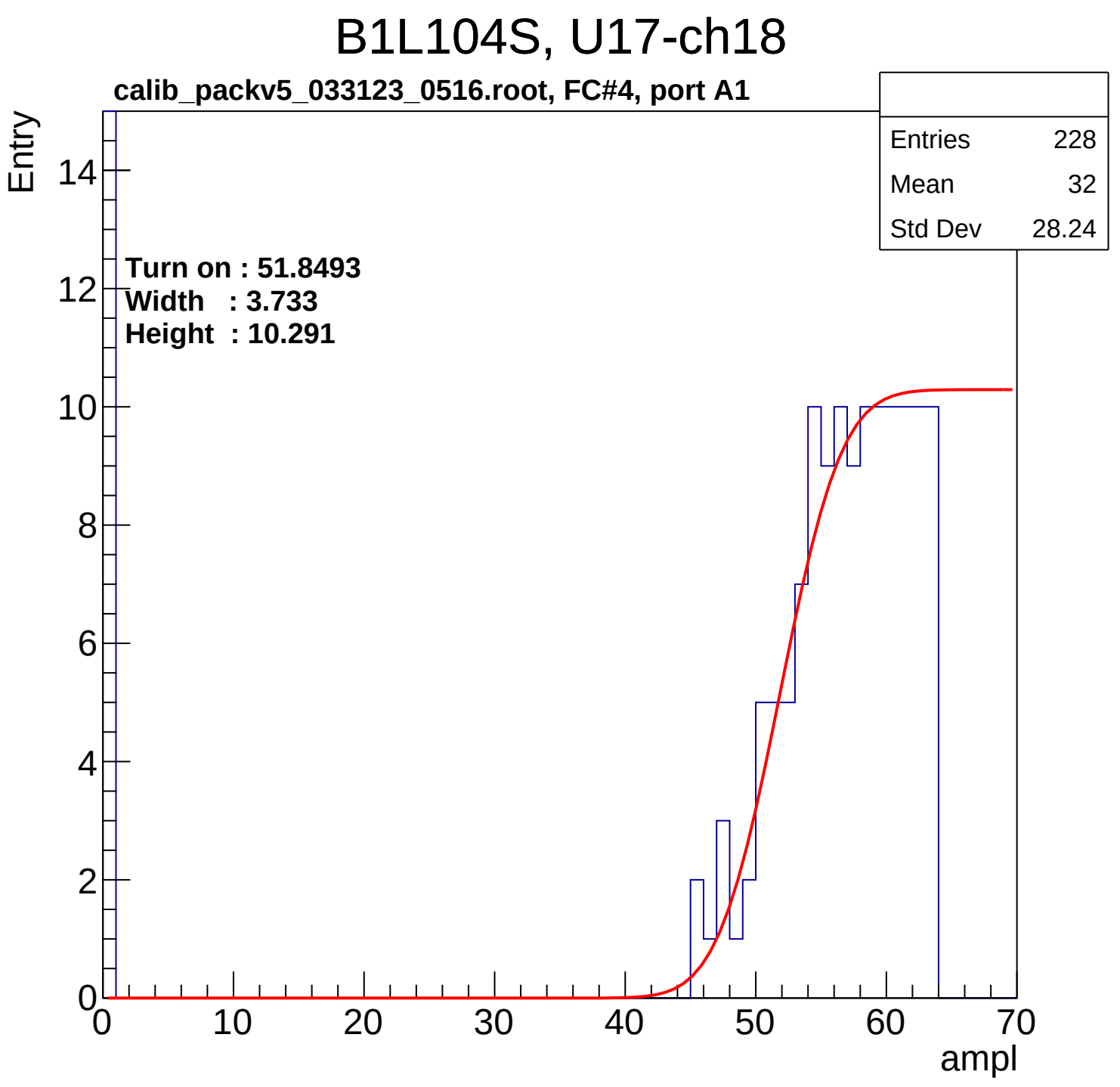
B1L104S, U17-ch18
calib_packv5_033123_0516.root, FC#4, port A1
Entries 228
Mean 32
Std Dev 28.24
Turn on : 51.8493
Width : 3.733
Height : 10.291
Entry
ampl
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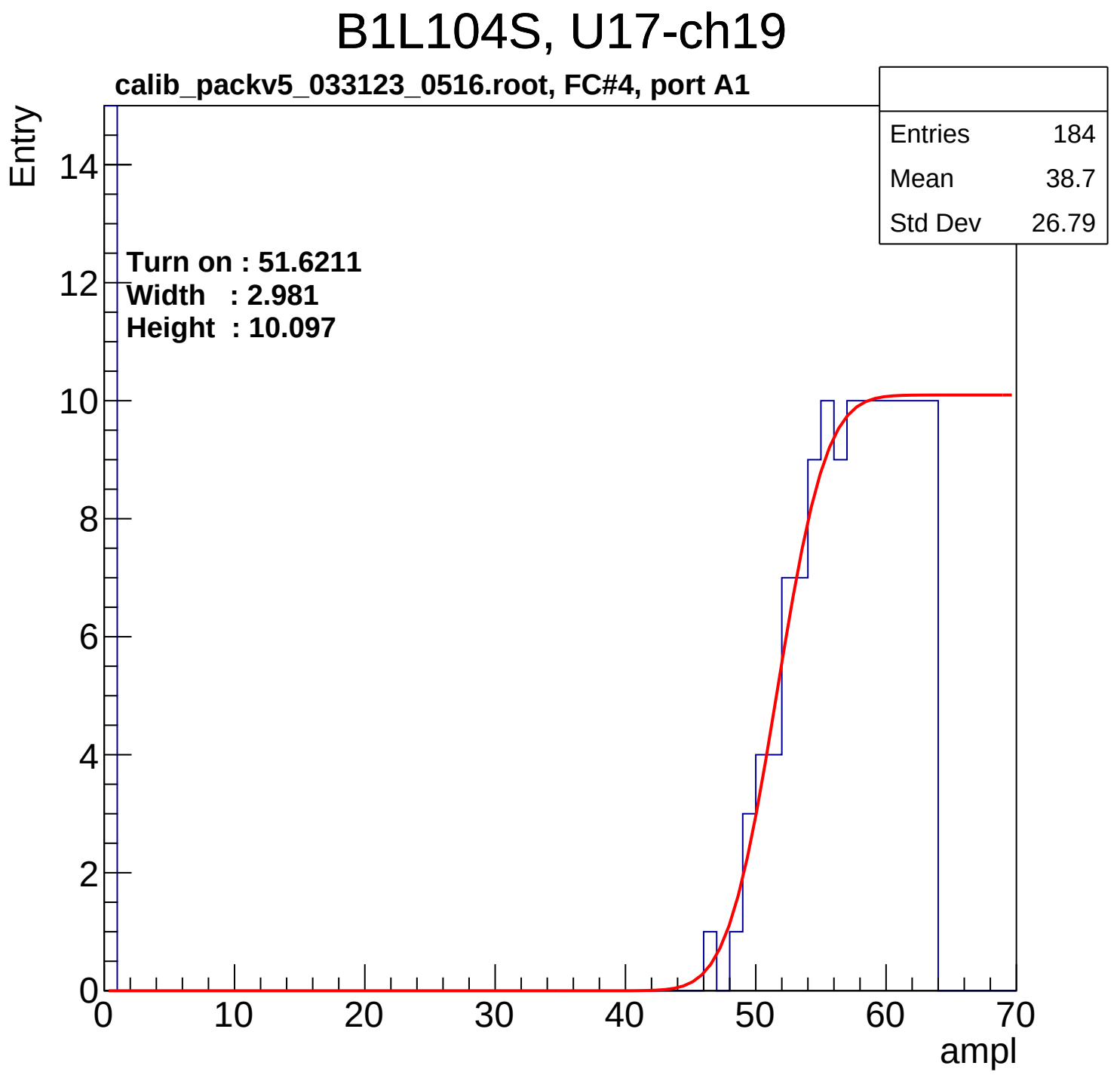
B1L104S, U17-ch19
calib_packv5_033123_0516.root, FC#4, port A1
Entries 184
Mean 38.7
Std Dev 26.79
Turn on : 51.6211
Width : 2.981
Height : 10.097
Entry
ampl
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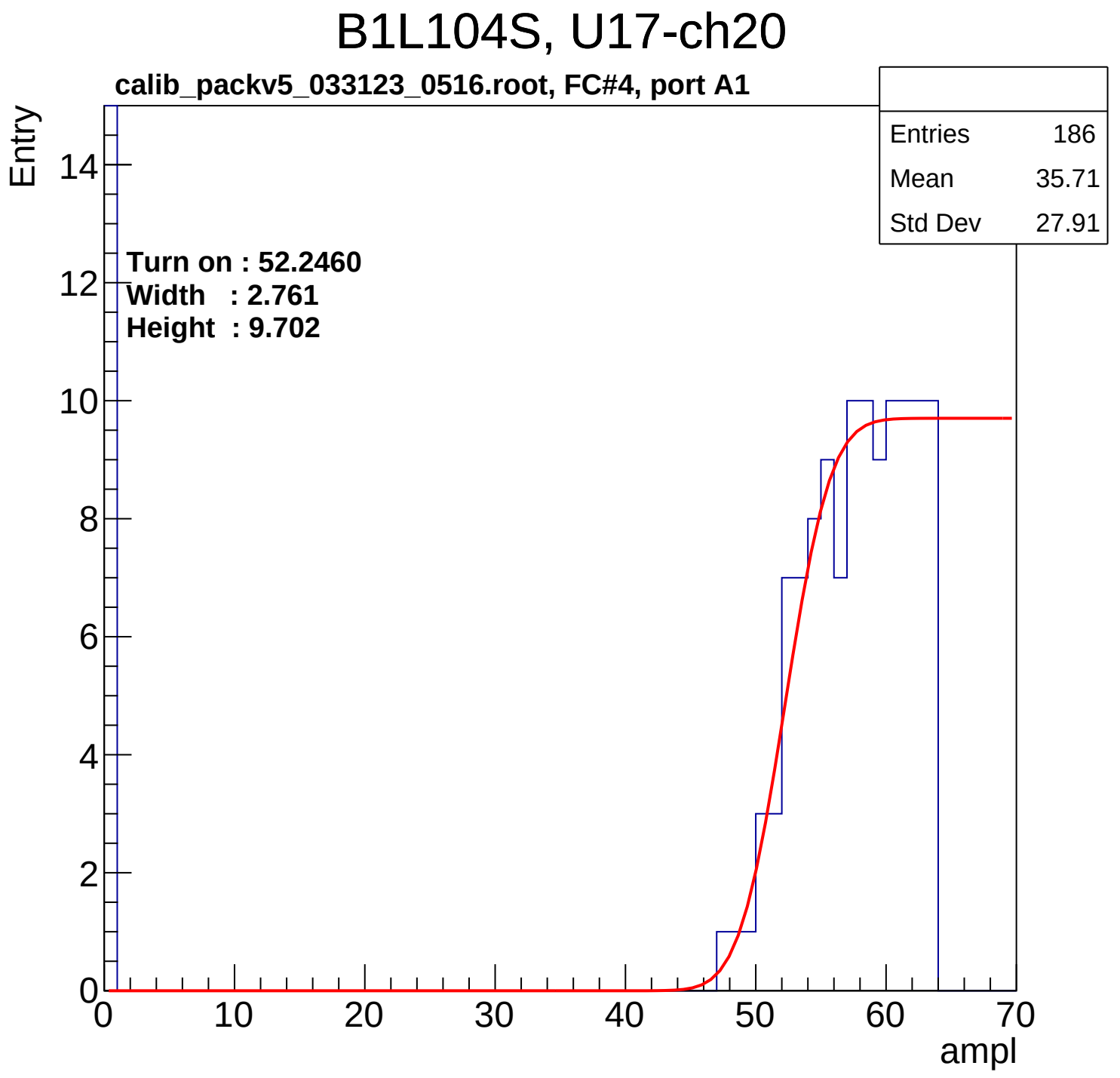
B1L104S, U17-ch20
calib_packv5_033123_0516.root, FC#4, port A1
Entries 186
Mean 35.71
Std Dev 27.91
Turn on : 52.2460
Width : 2.761
Height : 9.702
Entry
ampl
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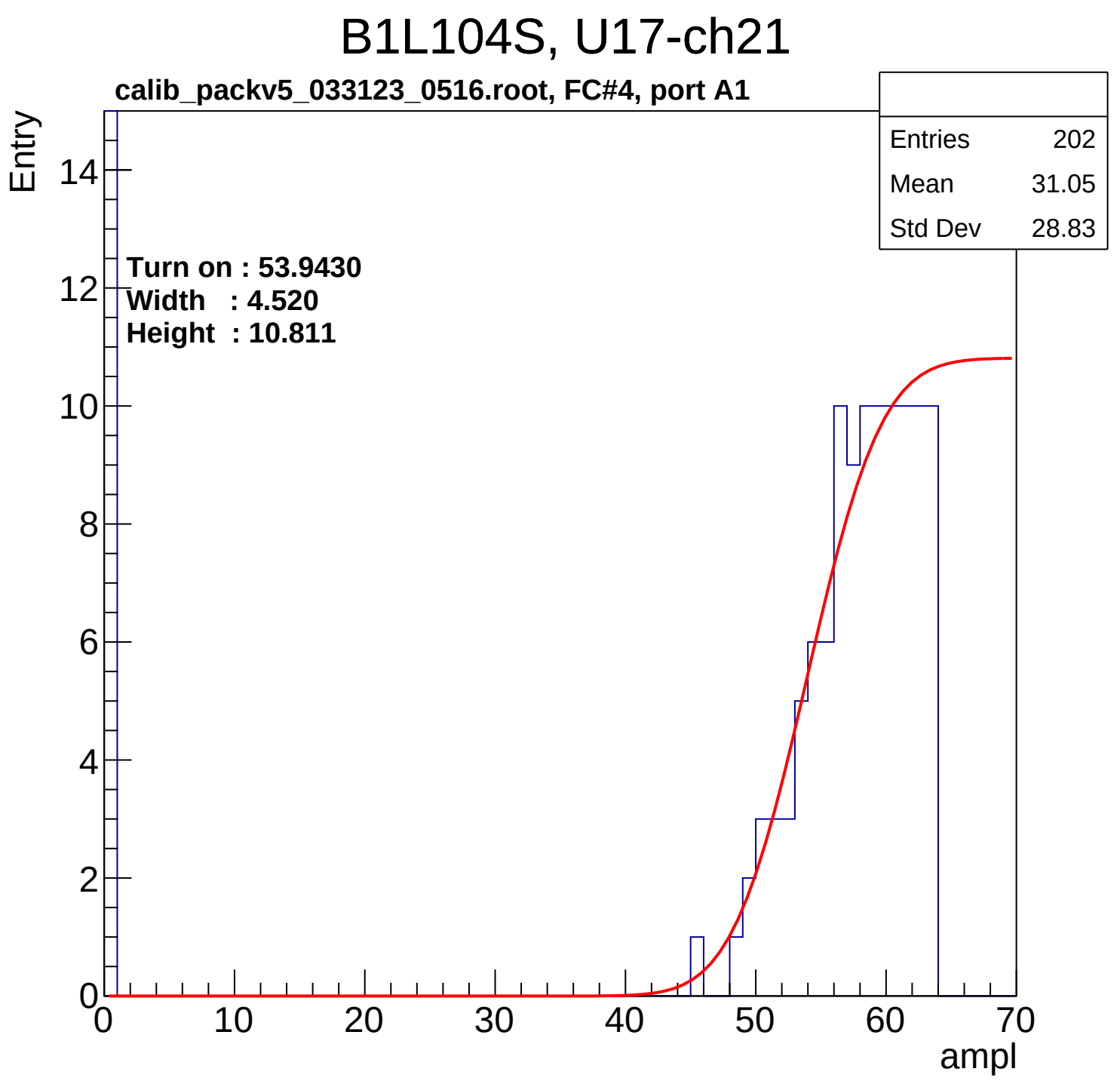
B1L104S, U17-ch21
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 31.05
Std Dev 28.83
Turn on : 53.9430
Width : 4.520
Height : 10.811
Entry
ampl
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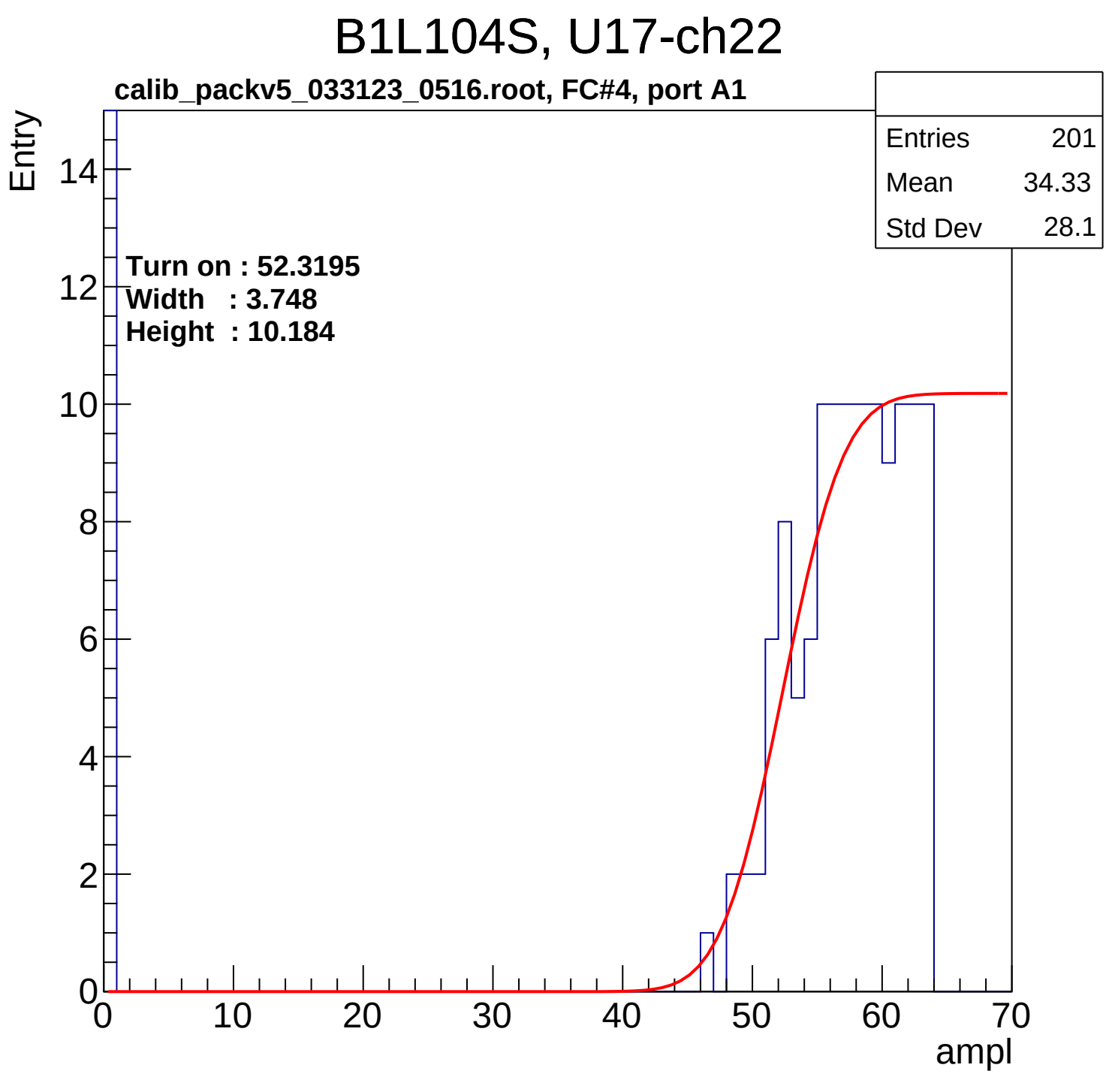
B1L104S, U17-ch22
calib_packv5_033123_0516.root, FC#4, port A1
Entries 201
Mean 34.33
Std Dev 28.1
Turn on : 52.3195
Width : 3.748
Height : 10.184
Entry
ampl
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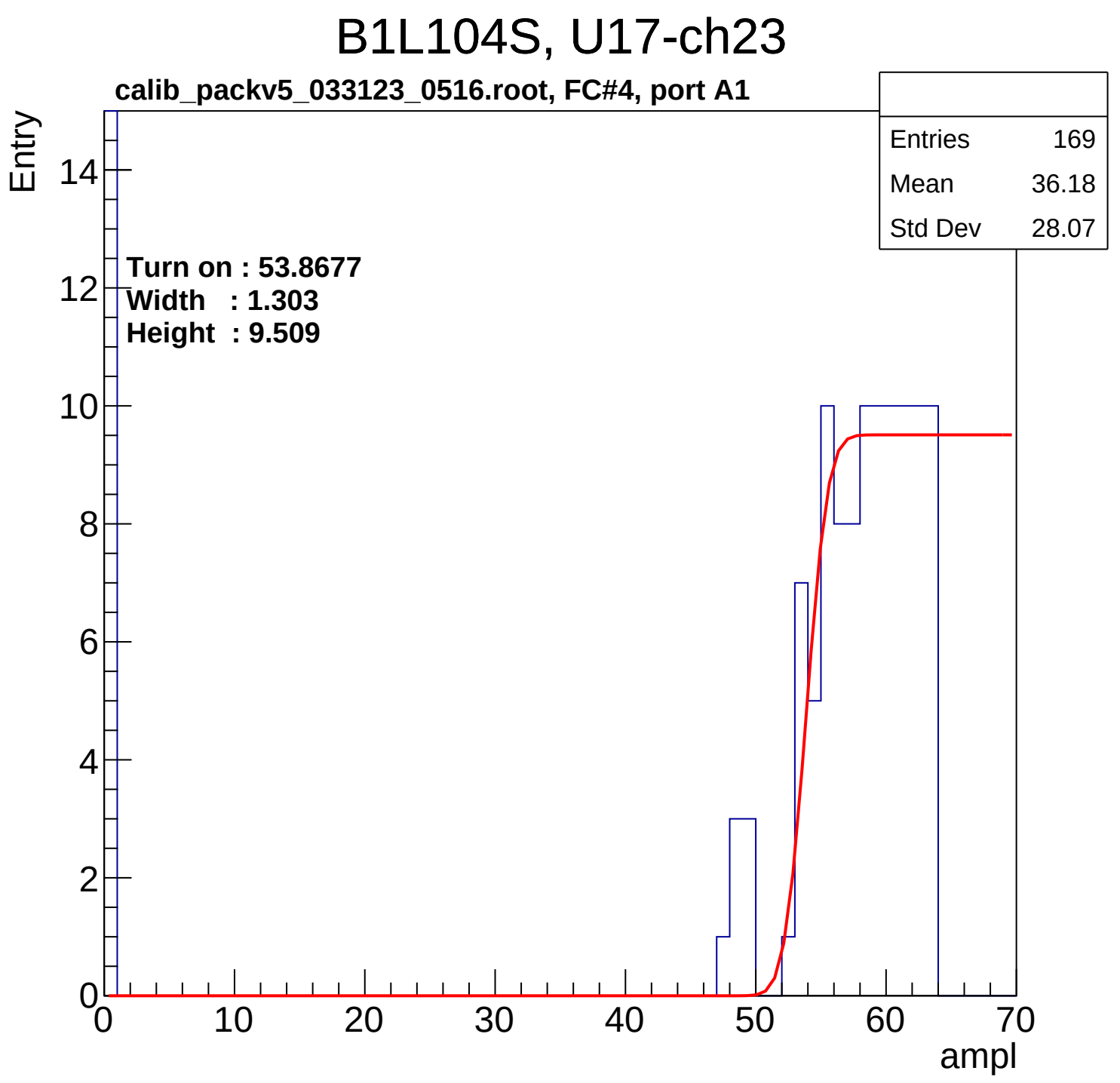
B1L104S, U17-ch23
calib_packv5_033123_0516.root, FC#4, port A1
Entries 169
Mean 36.18
Std Dev 28.07
Turn on : 53.8677
Width : 1.303
Height : 9.509
Entry
ampl
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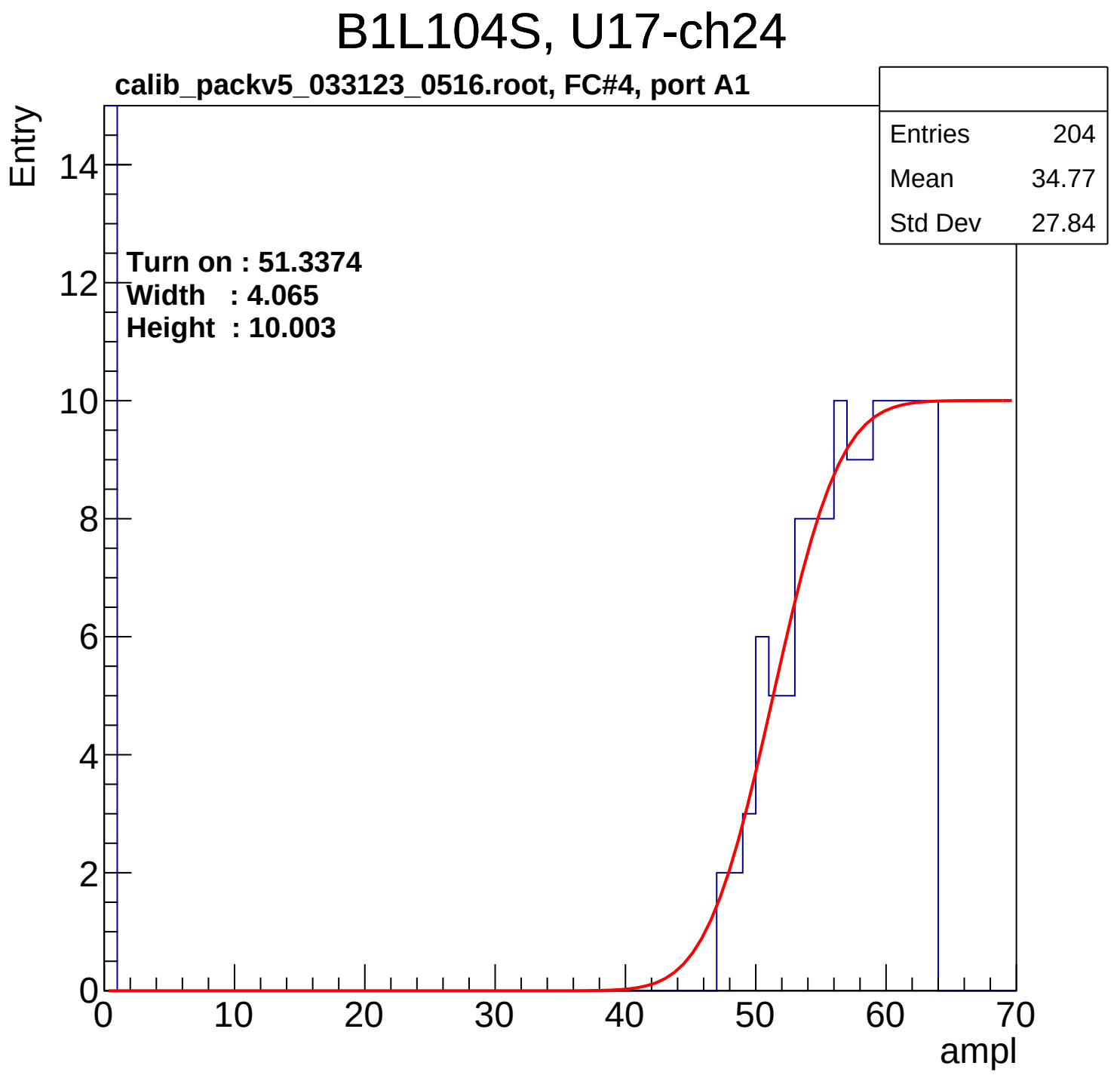
B1L104S, U17-ch24
calib_packv5_033123_0516.root, FC#4, port A1
Entries 204
Mean 34.77
Std Dev 27.84
Turn on : 51.3374
Width : 4.065
Height : 10.003
Entry
ampl
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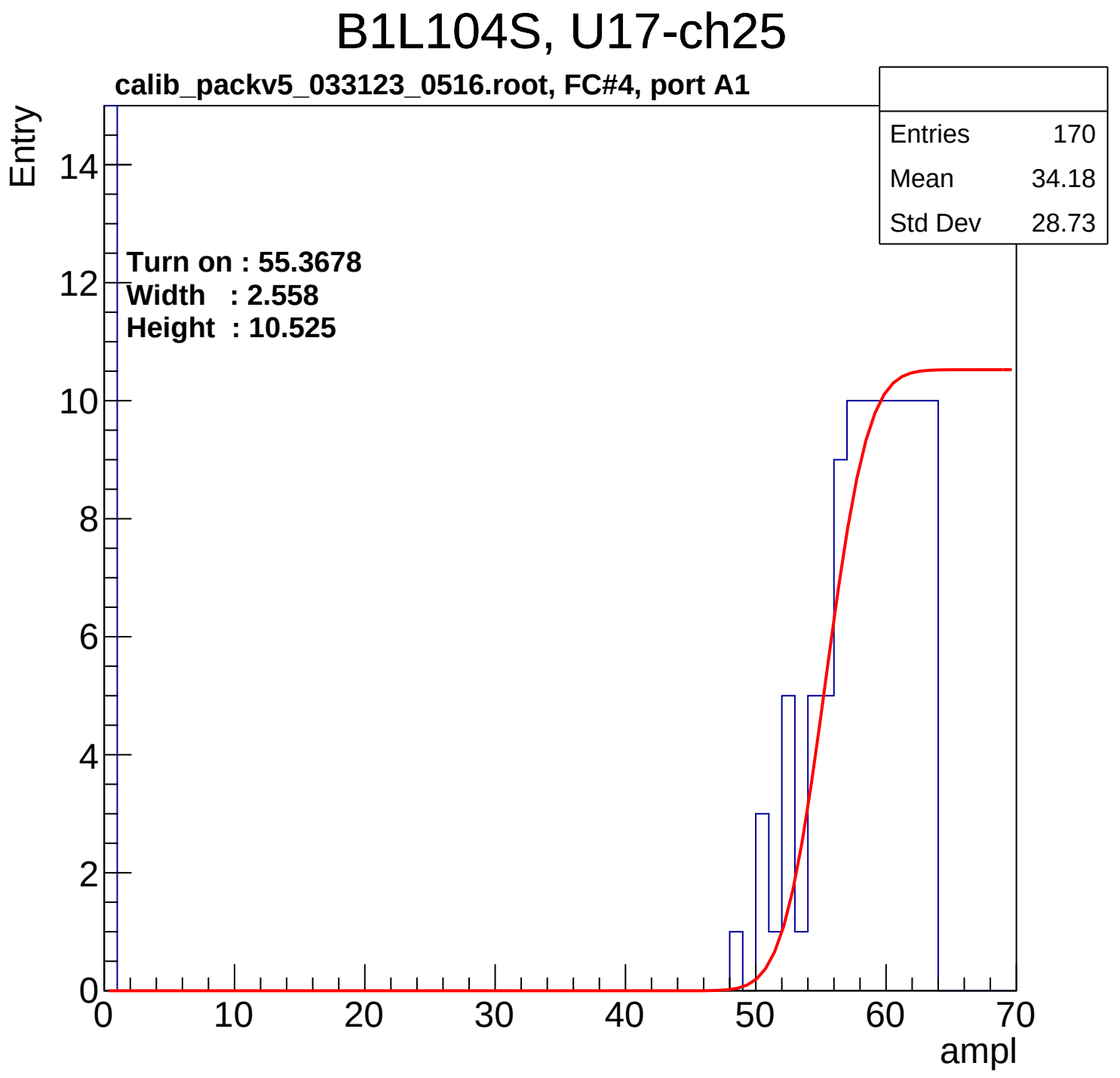
B1L104S, U17-ch25
calib_packv5_033123_0516.root, FC#4, port A1
Entries 170
Mean 34.18
Std Dev 28.73
Turn on : 55.3678
Width : 2.558
Height : 10.525
Entry
ampl
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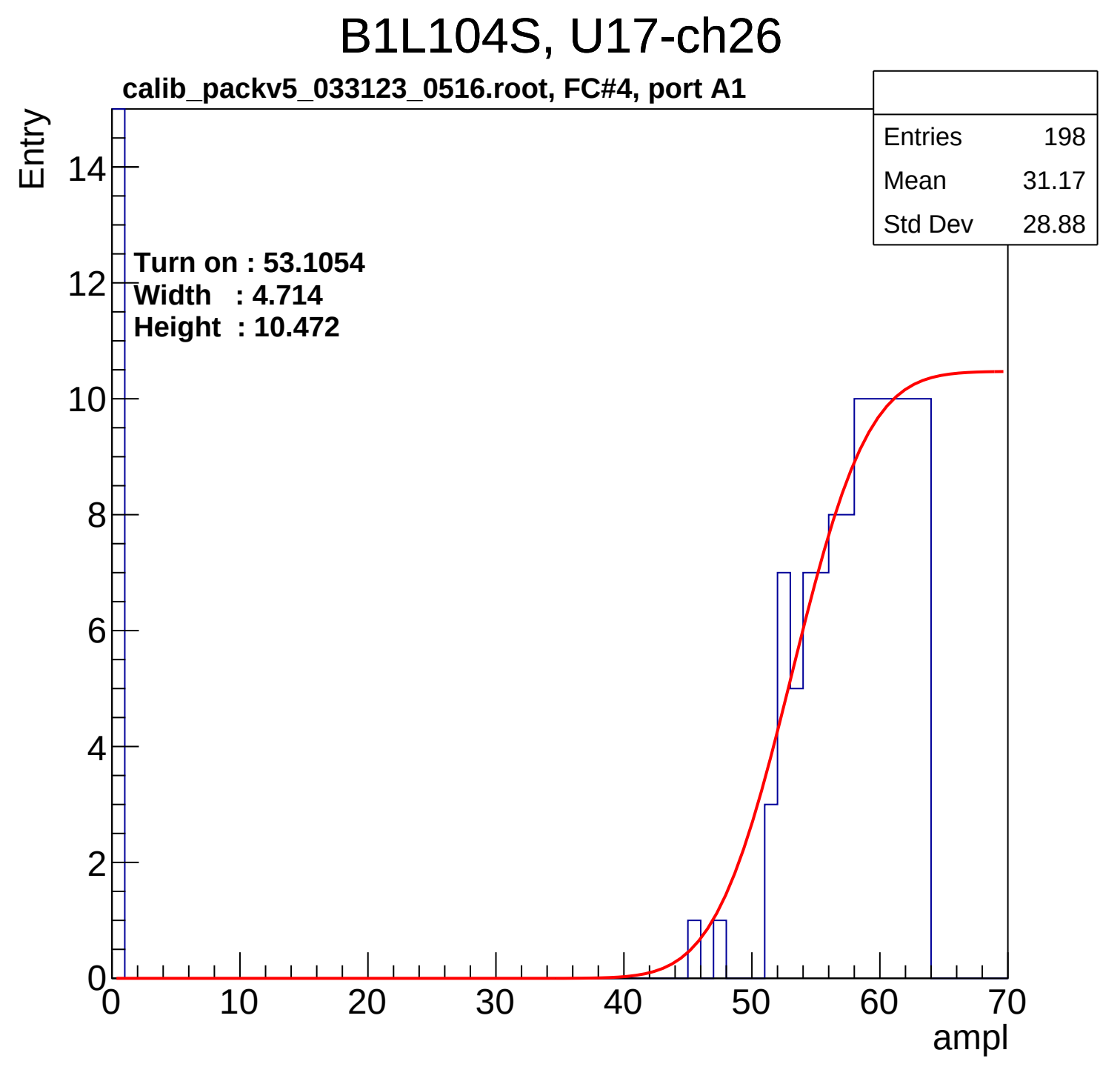
B1L104S, U17-ch26
calib_packv5_033123_0516.root, FC#4, port A1
Entries 198
Mean 31.17
Std Dev 28.88
Turn on : 53.1054
Width : 4.714
Height : 10.472
Entry
ampl
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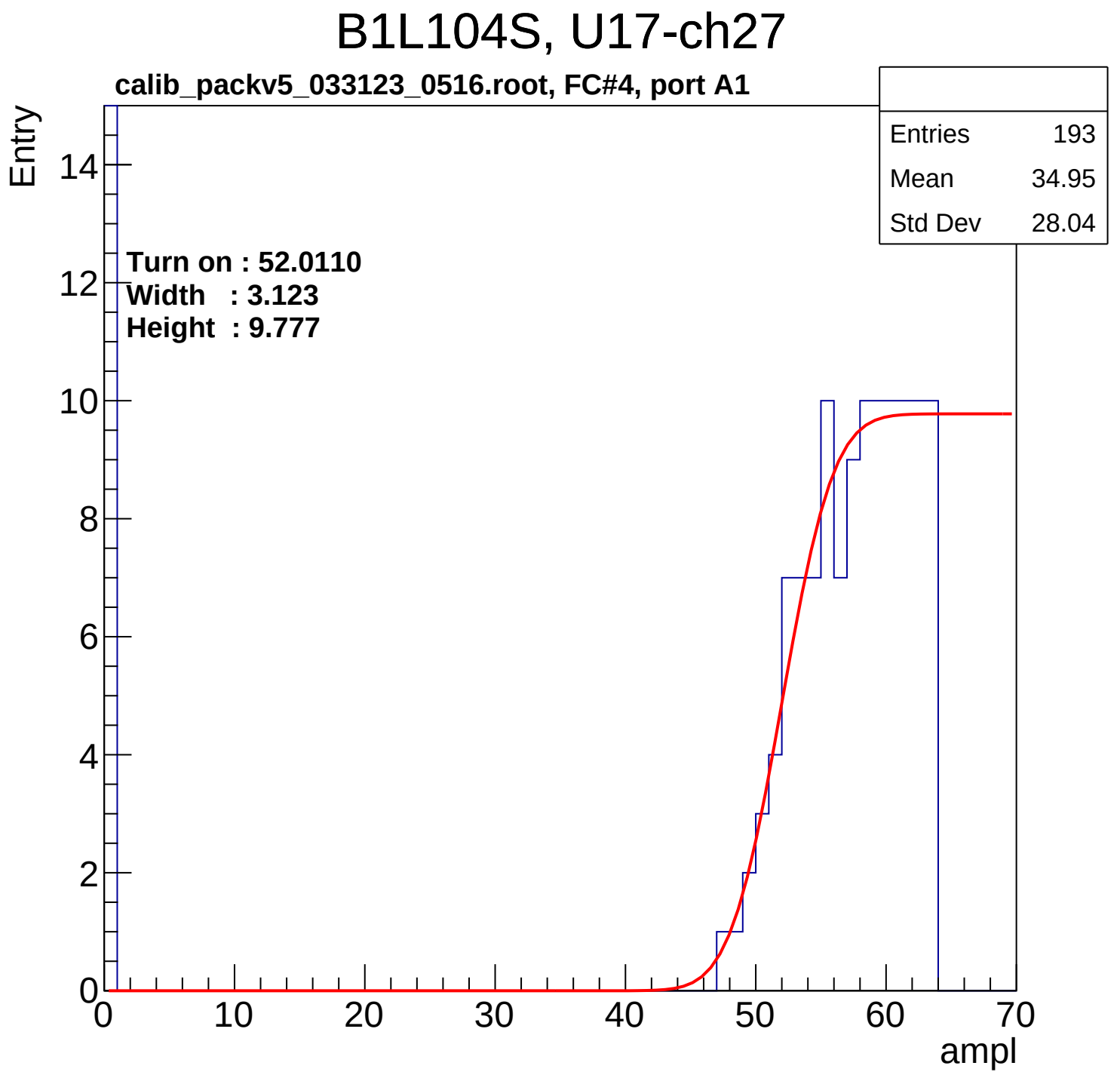
B1L104S, U17-ch27
calib_packv5_033123_0516.root, FC#4, port A1
Entries 193
Mean 34.95
Std Dev 28.04
Turn on : 52.0110
Width : 3.123
Height : 9.777
Entry
ampl
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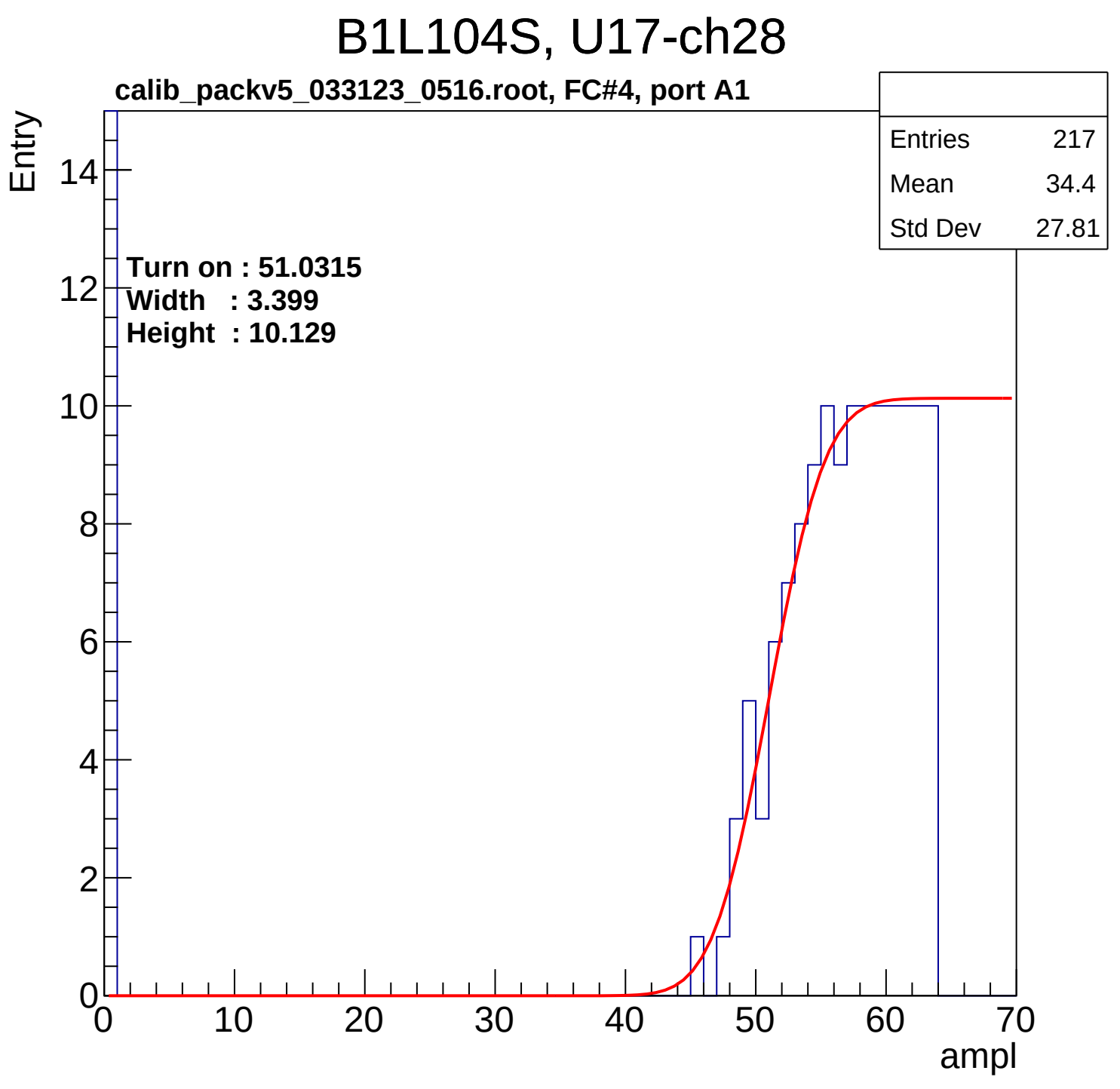
B1L104S, U17-ch28
calib_packv5_033123_0516.root, FC#4, port A1
Entries 217
Mean 34.4
Std Dev 27.81
Turn on : 51.0315
Width : 3.399
Height : 10.129
Entry
ampl
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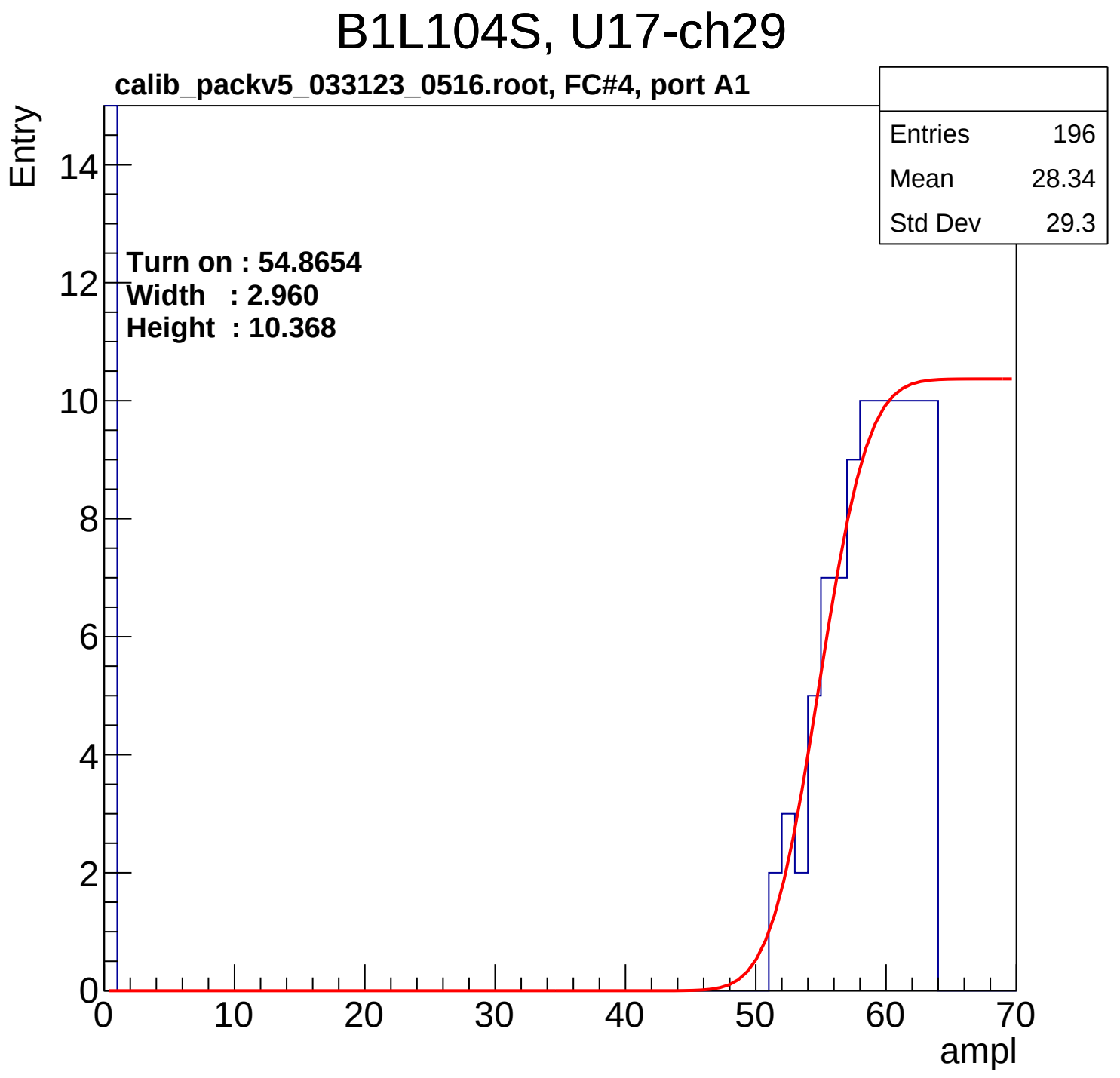
B1L104S, U17-ch29
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 28.34
Std Dev 29.3
Turn on : 54.8654
Width : 2.960
Height : 10.368
Entry
ampl
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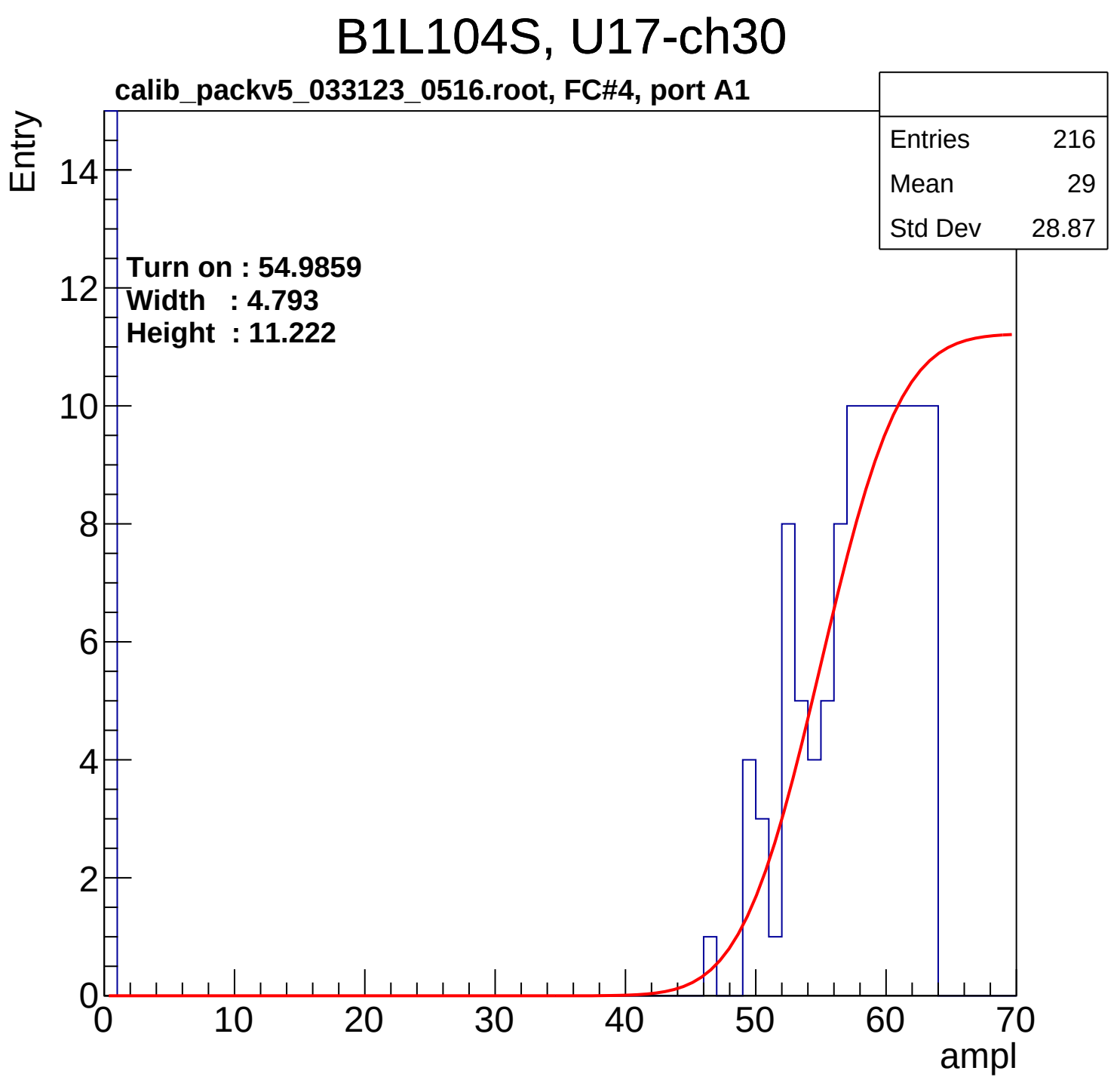
B1L104S, U17-ch30
calib_packv5_033123_0516.root, FC#4, port A1
Entries 216
Mean 29
Std Dev 28.87
Turn on : 54.9859
Width : 4.793
Height : 11.222
Entry
ampl
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6
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0
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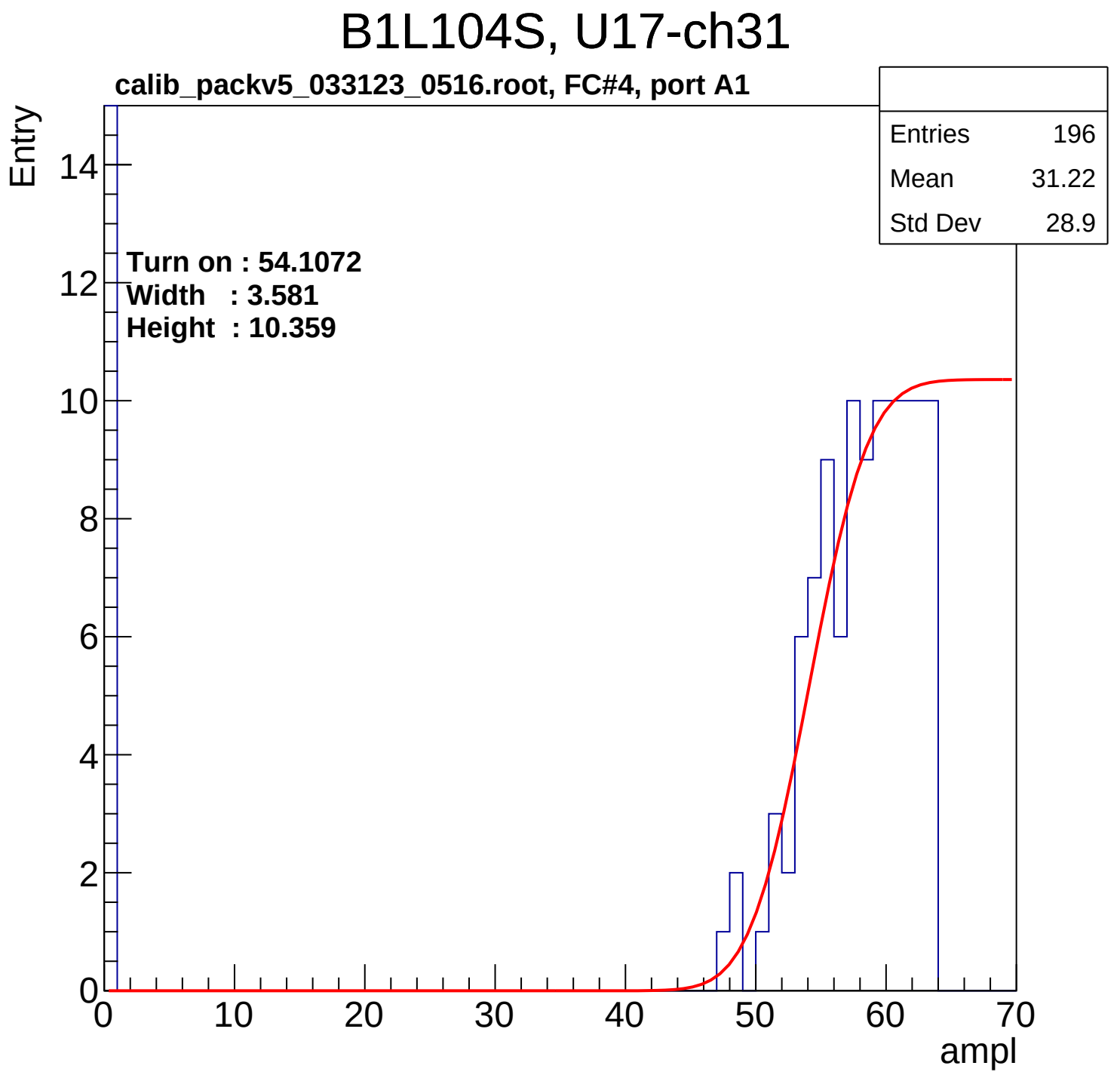
B1L104S, U17-ch31
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 31.22
Std Dev 28.9
Turn on : 54.1072
Width : 3.581
Height : 10.359
Entry
ampl
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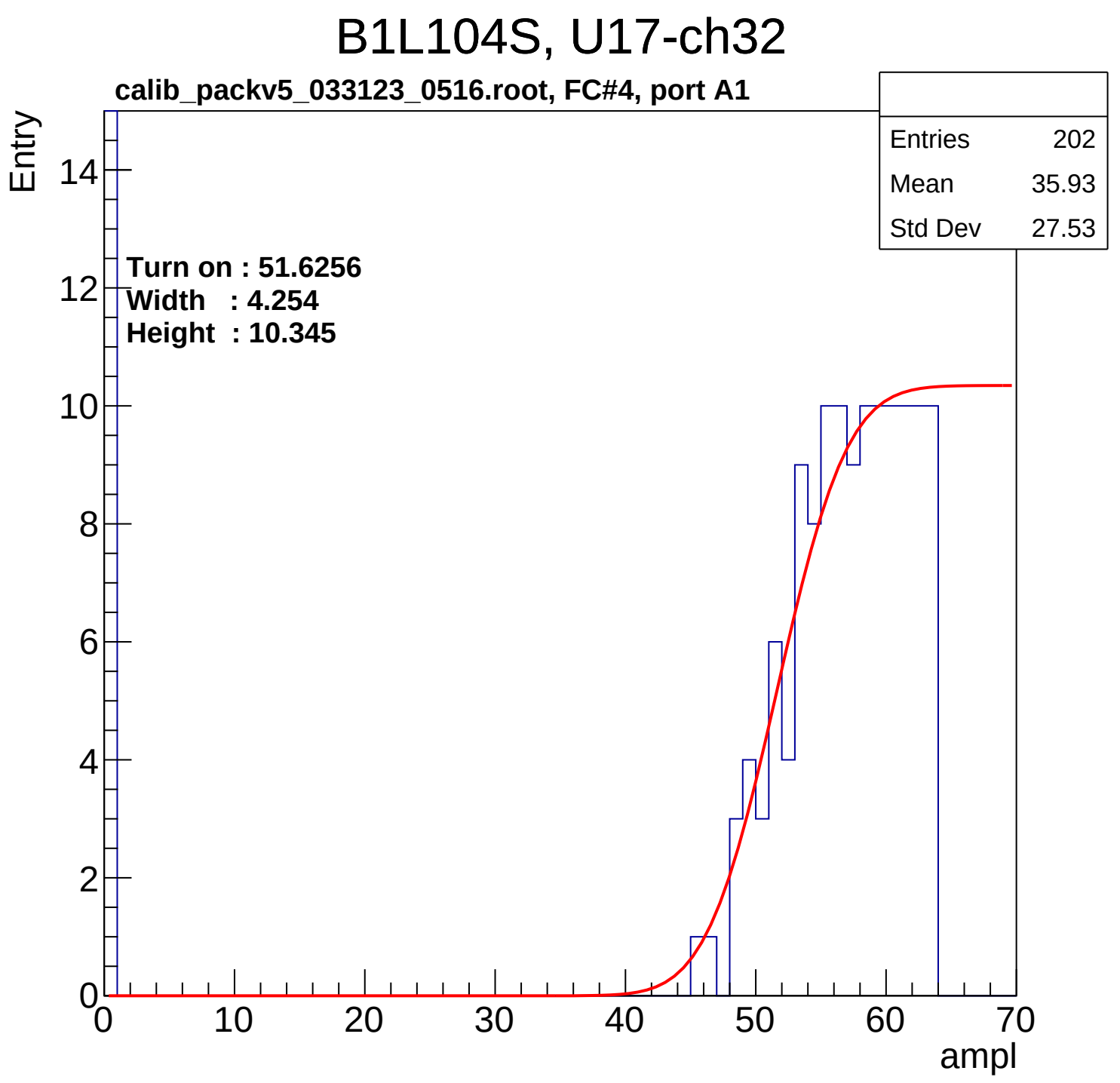
B1L104S, U17-ch32
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 35.93
Std Dev 27.53
Turn on : 51.6256
Width : 4.254
Height : 10.345
Entry
ampl
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2
4
6
8
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12
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0
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60
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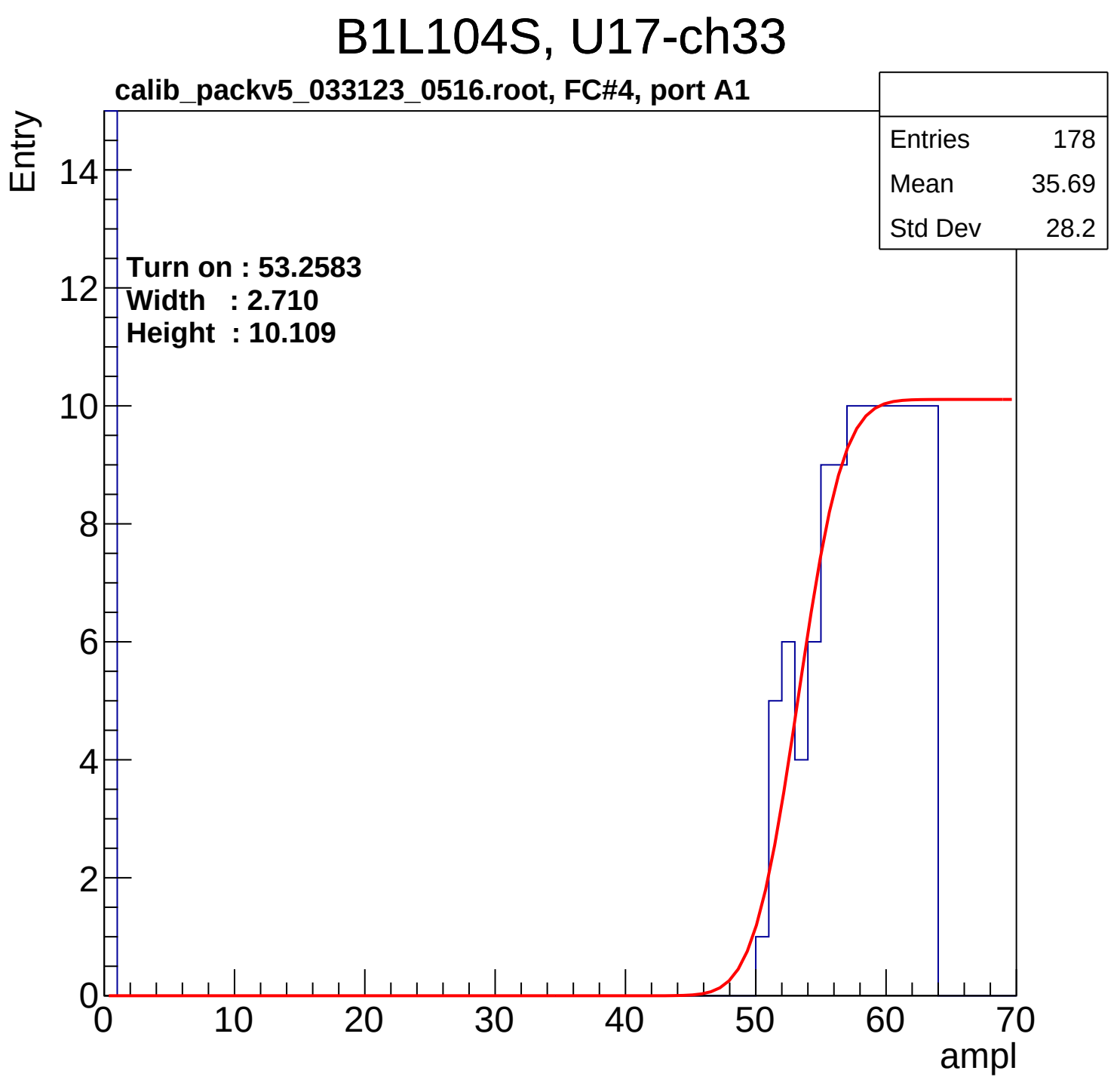
B1L104S, U17-ch33
calib_packv5_033123_0516.root, FC#4, port A1
Entries 178
Mean 35.69
Std Dev 28.2
Turn on : 53.2583
Width : 2.710
Height : 10.109
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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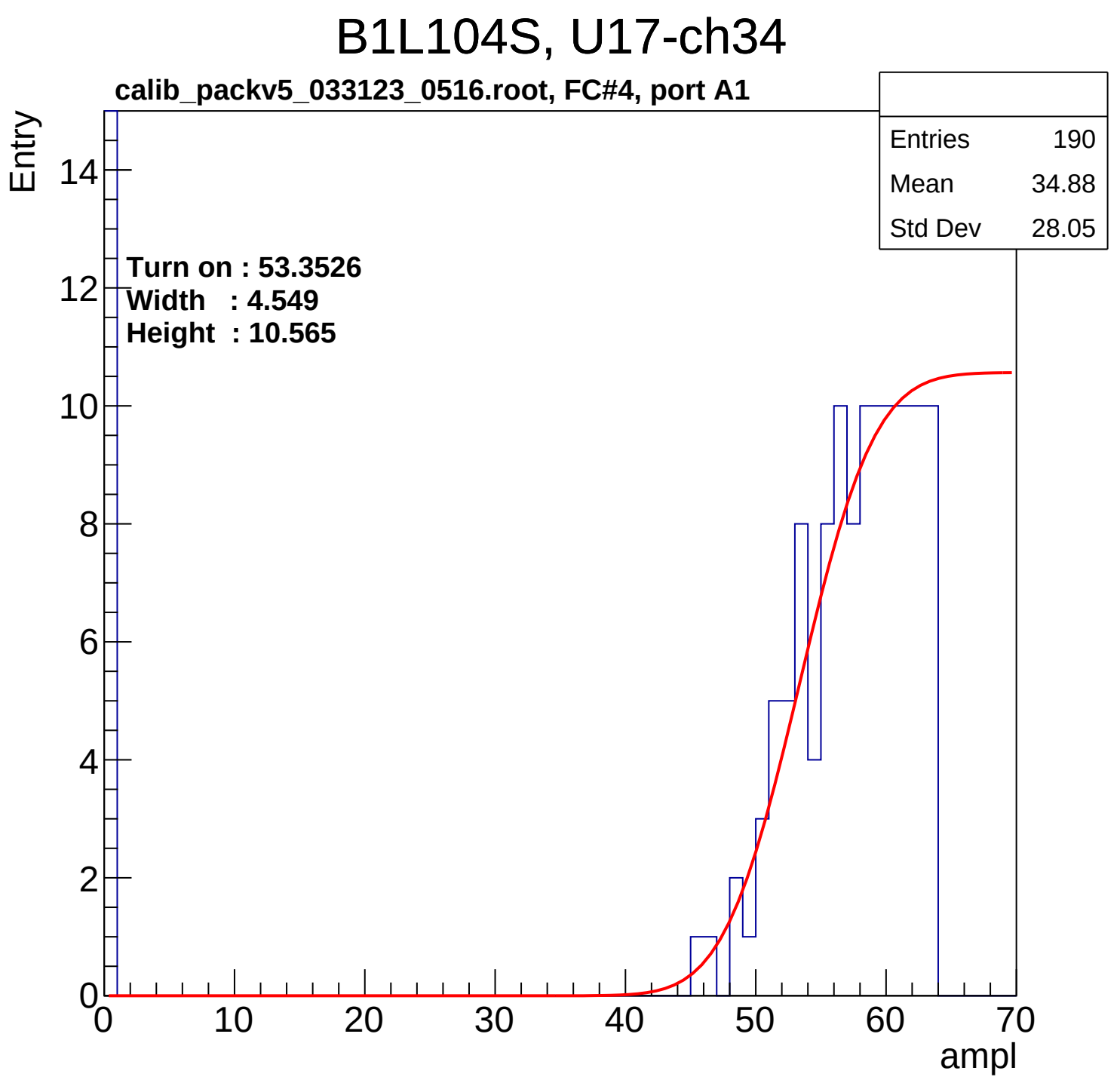
B1L104S, U17-ch34
calib_packv5_033123_0516.root, FC#4, port A1
Entries 190
Mean 34.88
Std Dev 28.05
Turn on : 53.3526
Width : 4.549
Height : 10.565
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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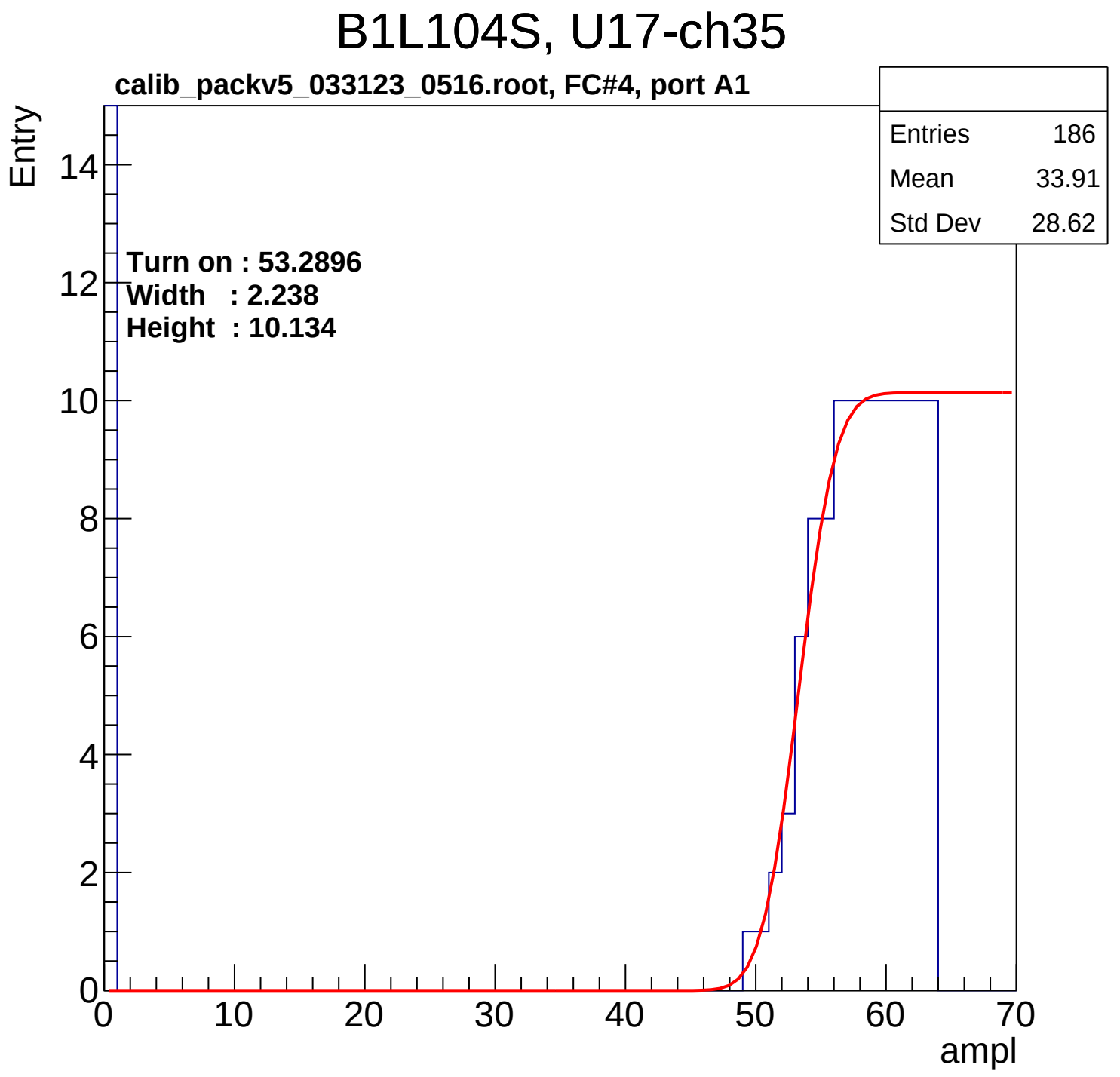
B1L104S, U17-ch35
calib_packv5_033123_0516.root, FC#4, port A1
Entries 186
Mean 33.91
Std Dev 28.62
Turn on : 53.2896
Width : 2.238
Height : 10.134
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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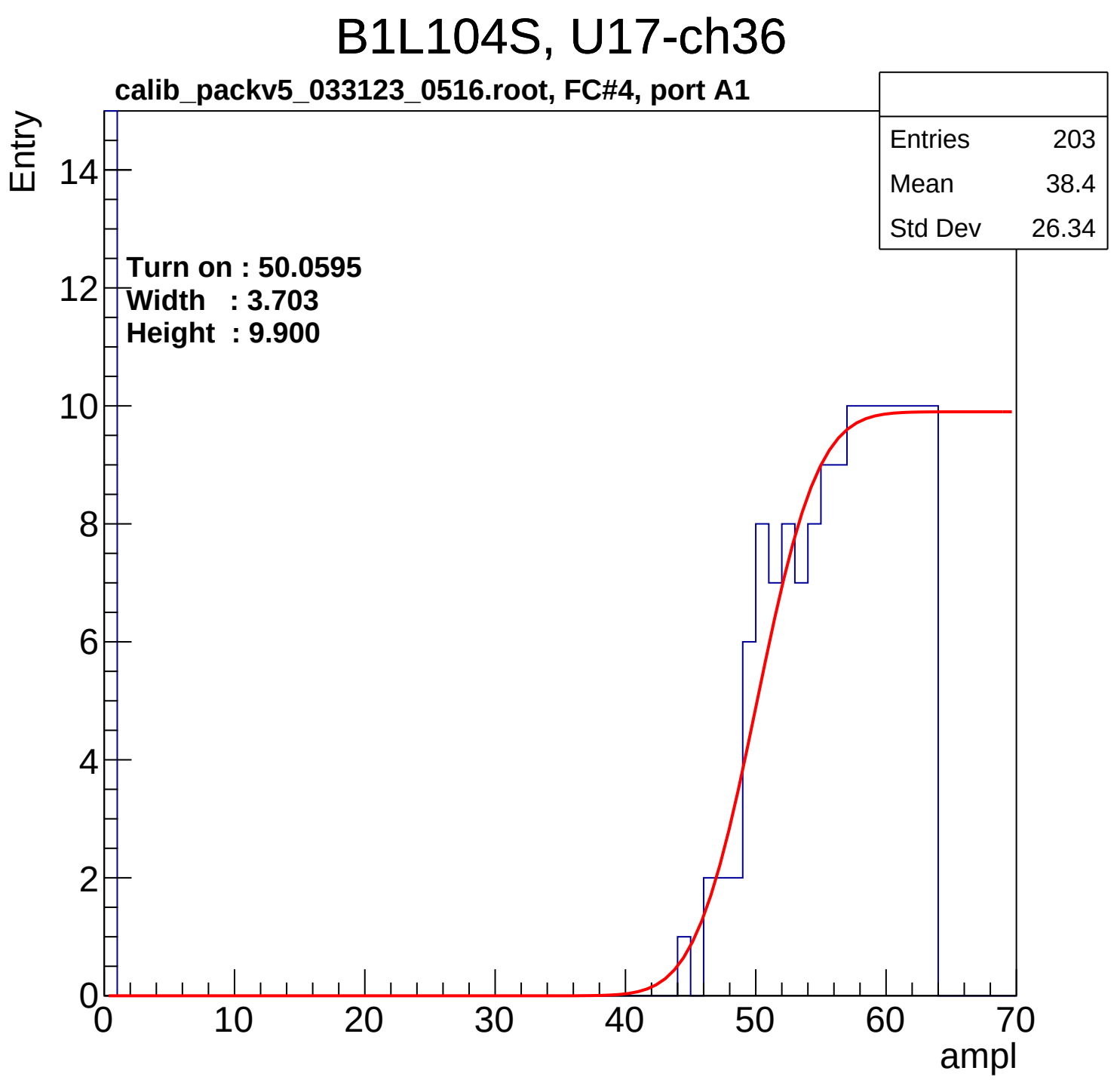
B1L104S, U17-ch36
calib_packv5_033123_0516.root, FC#4, port A1
Entries 203
Mean 38.4
Std Dev 26.34
Turn on : 50.0595
Width : 3.703
Height : 9.900
Entry
ampl
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2
4
6
8
10
12
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0
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60
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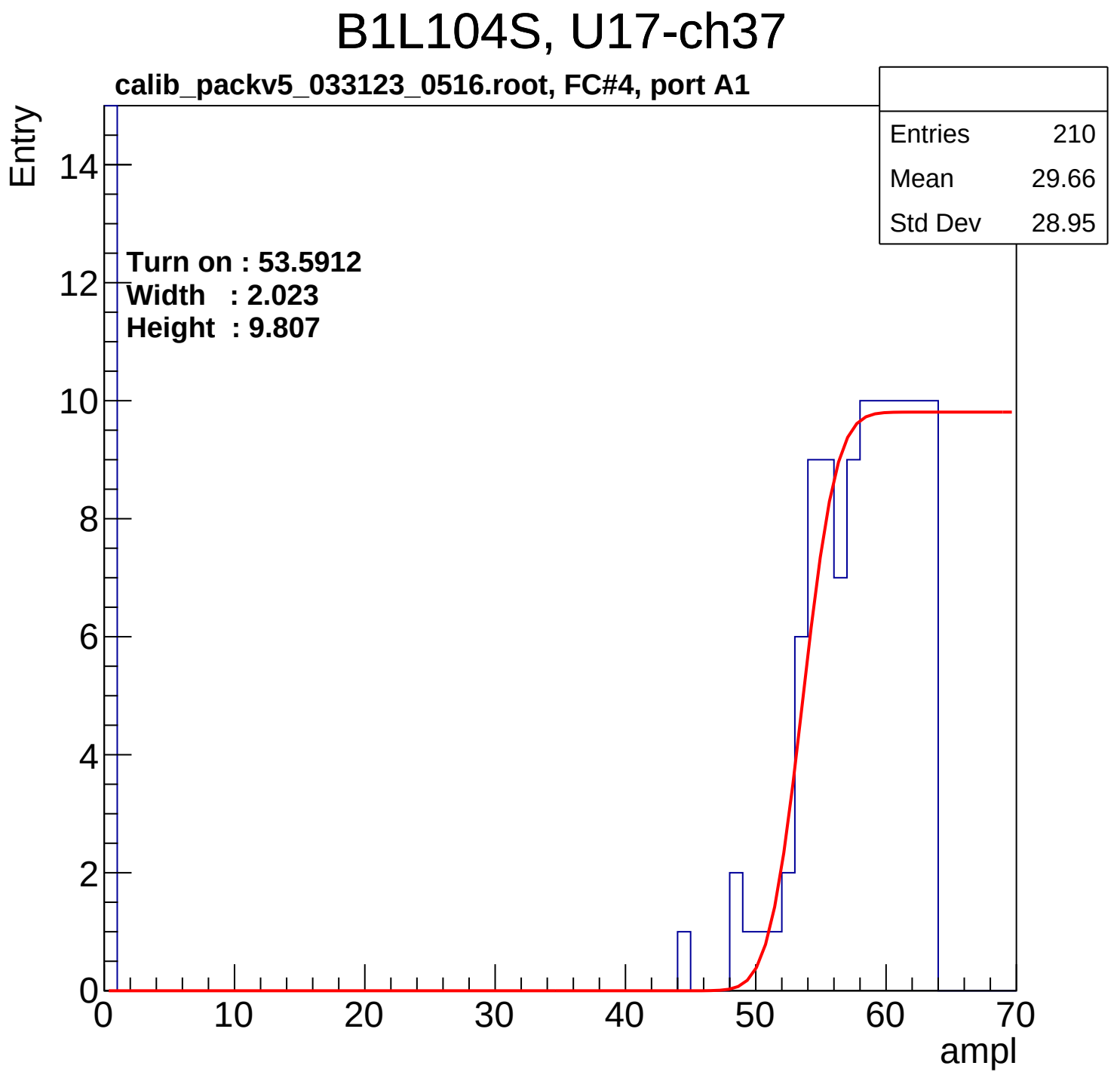
B1L104S, U17-ch37
calib_packv5_033123_0516.root, FC#4, port A1
Entries 210
Mean 29.66
Std Dev 28.95
Turn on : 53.5912
Width : 2.023
Height : 9.807
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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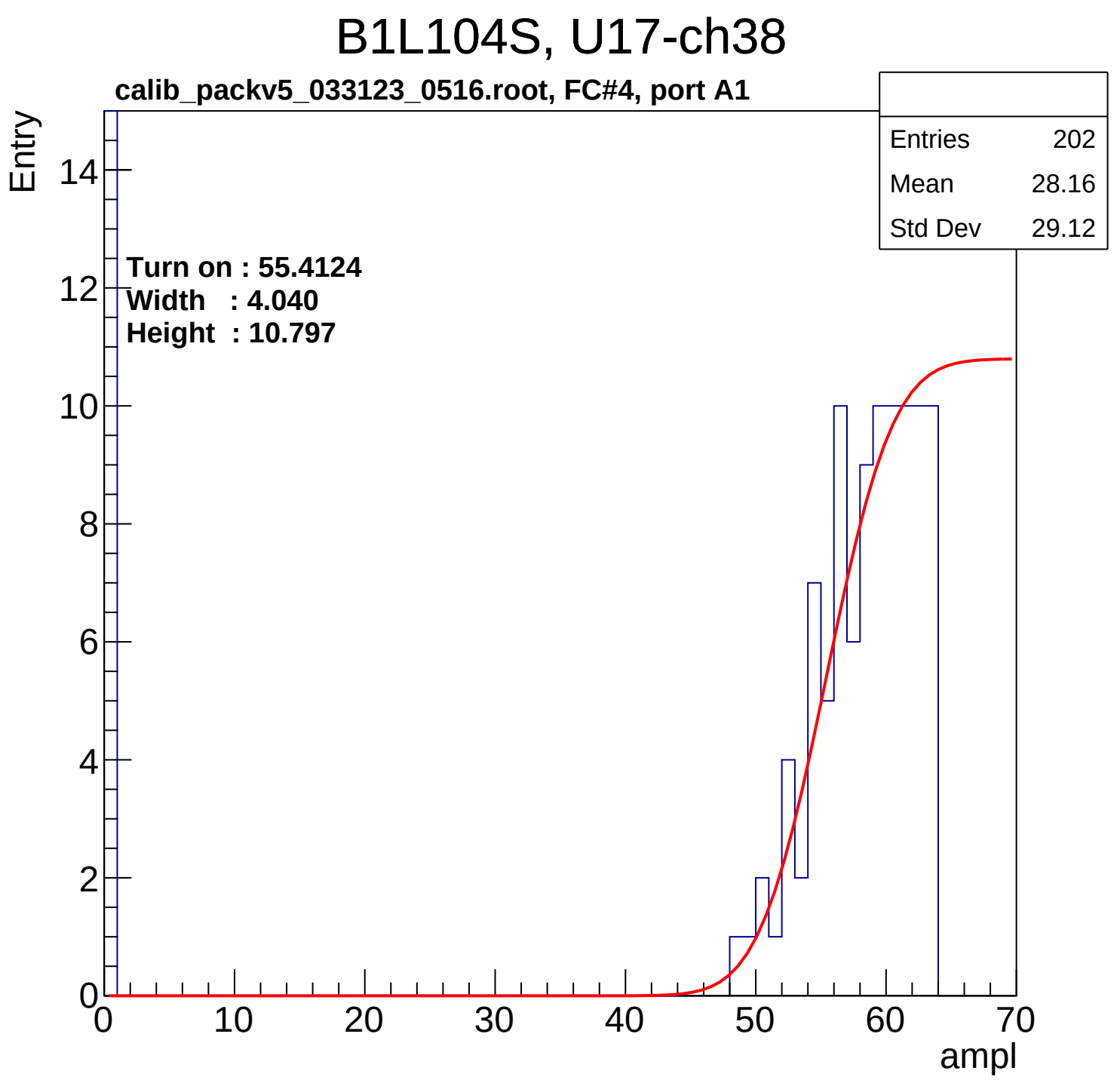
B1L104S, U17-ch38
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 28.16
Std Dev 29.12
Turn on : 55.4124
Width : 4.040
Height : 10.797
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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60
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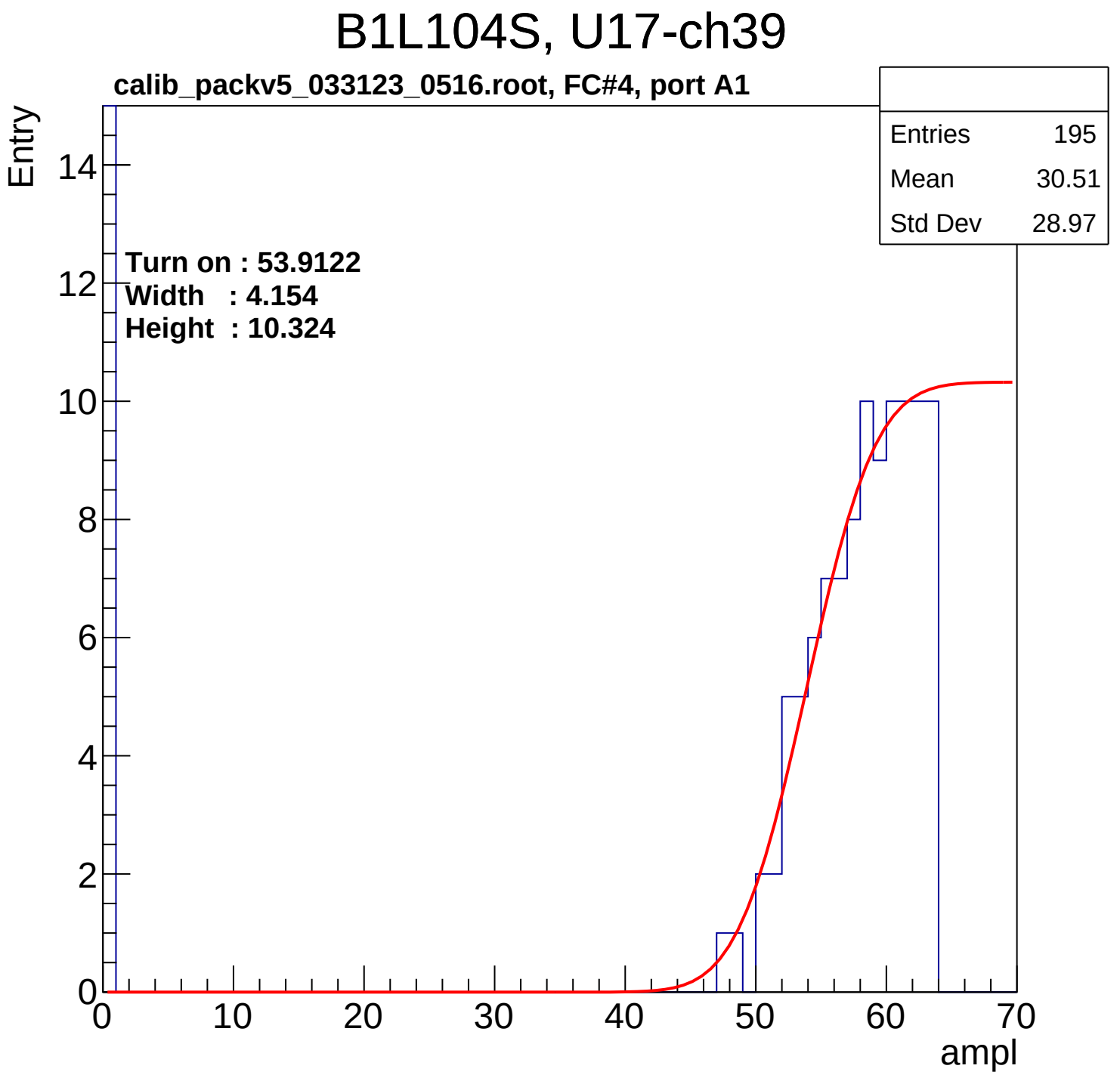
B1L104S, U17-ch39
calib_packv5_033123_0516.root, FC#4, port A1
Entries 195
Mean 30.51
Std Dev 28.97
Turn on : 53.9122
Width : 4.154
Height : 10.324
Entry
ampl
0
2
4
6
8
10
12
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0
10
20
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40
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60
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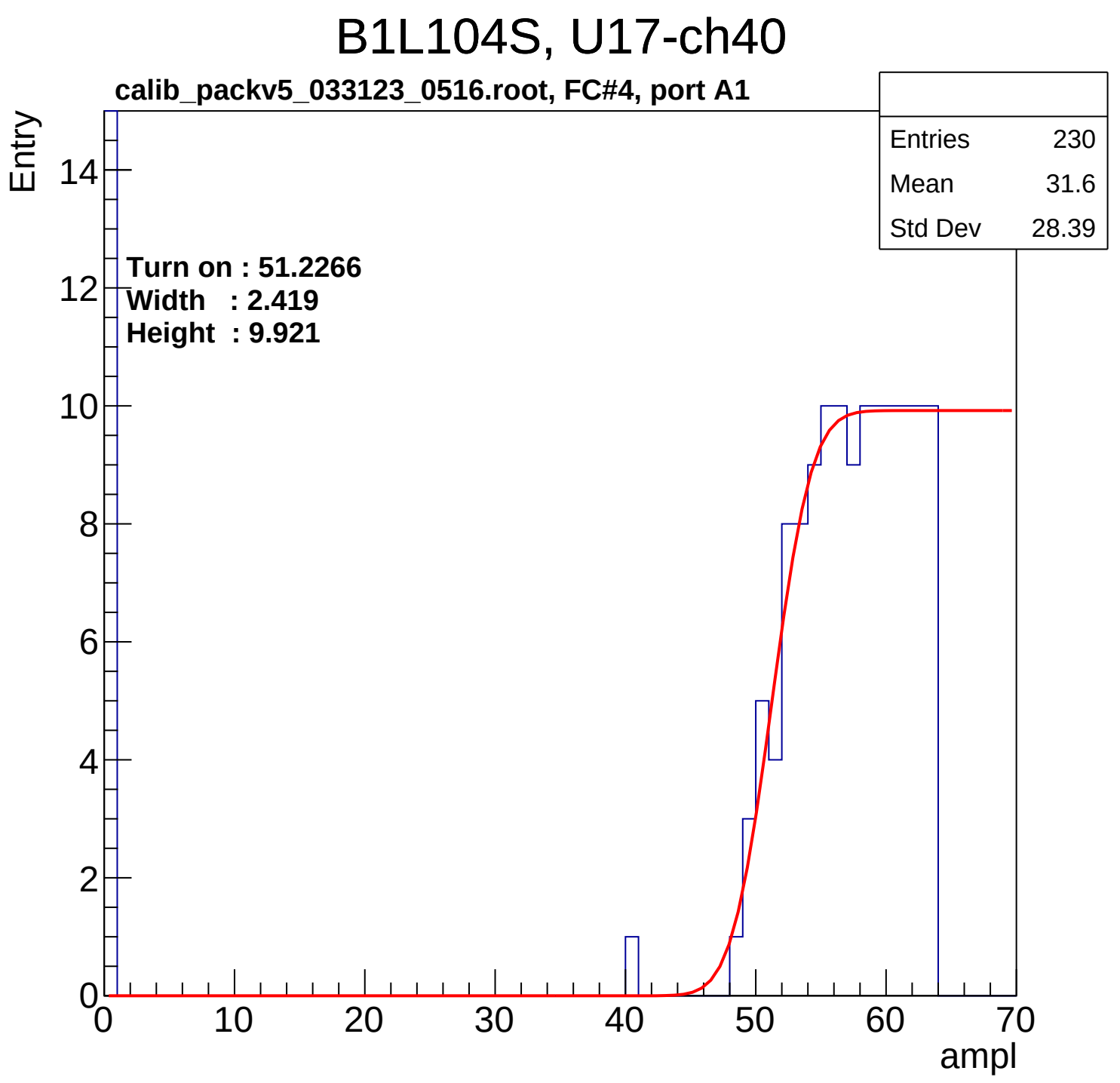
B1L104S, U17-ch40
calib_packv5_033123_0516.root, FC#4, port A1
Entries 230
Mean 31.6
Std Dev 28.39
Turn on : 51.2266
Width : 2.419
Height : 9.921
Entry
ampl
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2
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6
8
10
12
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0
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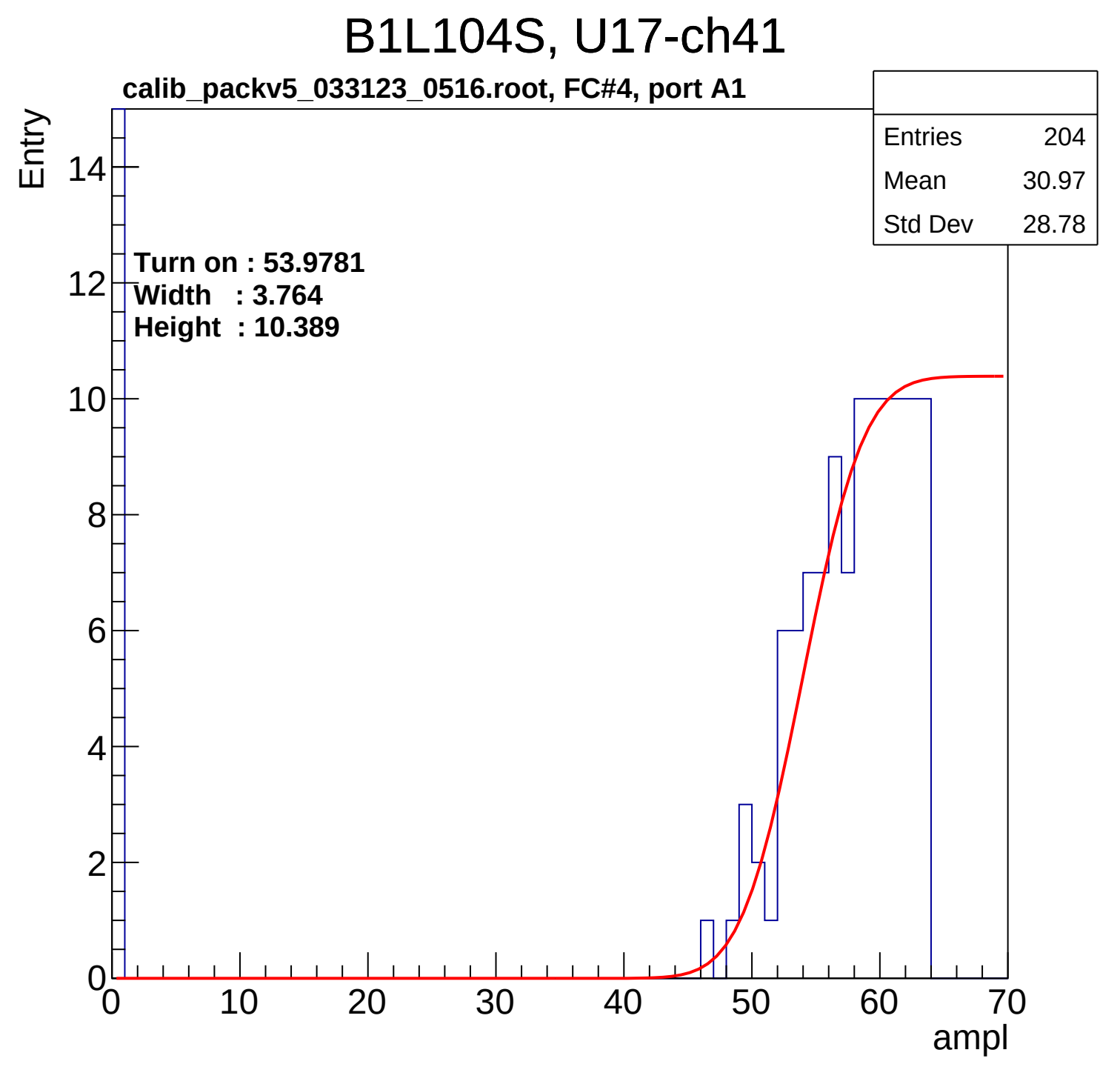
B1L104S, U17-ch41
calib_packv5_033123_0516.root, FC#4, port A1
Entries 204
Mean 30.97
Std Dev 28.78
Turn on : 53.9781
Width : 3.764
Height : 10.389
Entry
ampl
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2
4
6
8
10
12
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0
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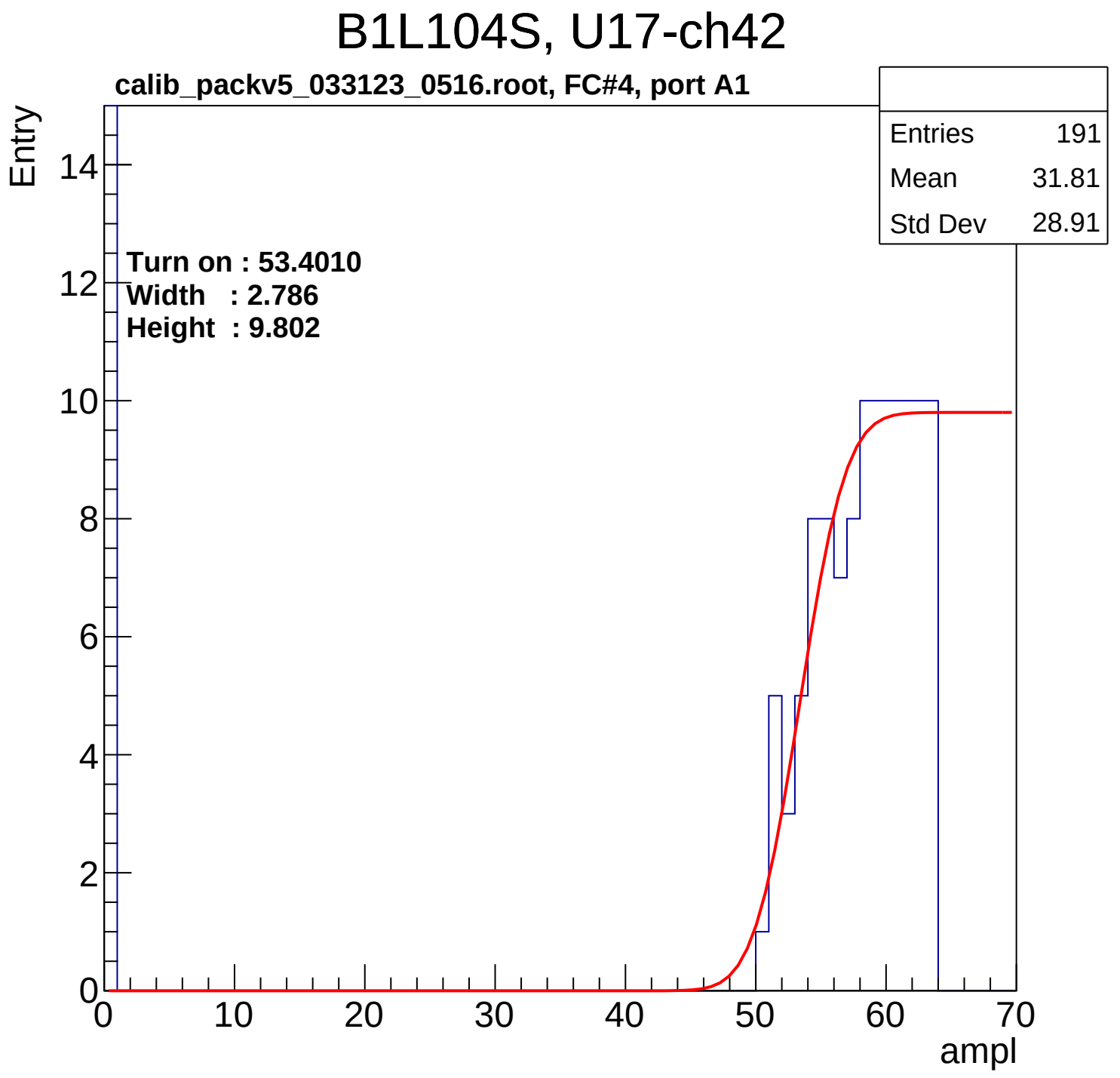
B1L104S, U17-ch42
calib_packv5_033123_0516.root, FC#4, port A1
Entries 191
Mean 31.81
Std Dev 28.91
Turn on : 53.4010
Width : 2.786
Height : 9.802
Entry
ampl
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6
8
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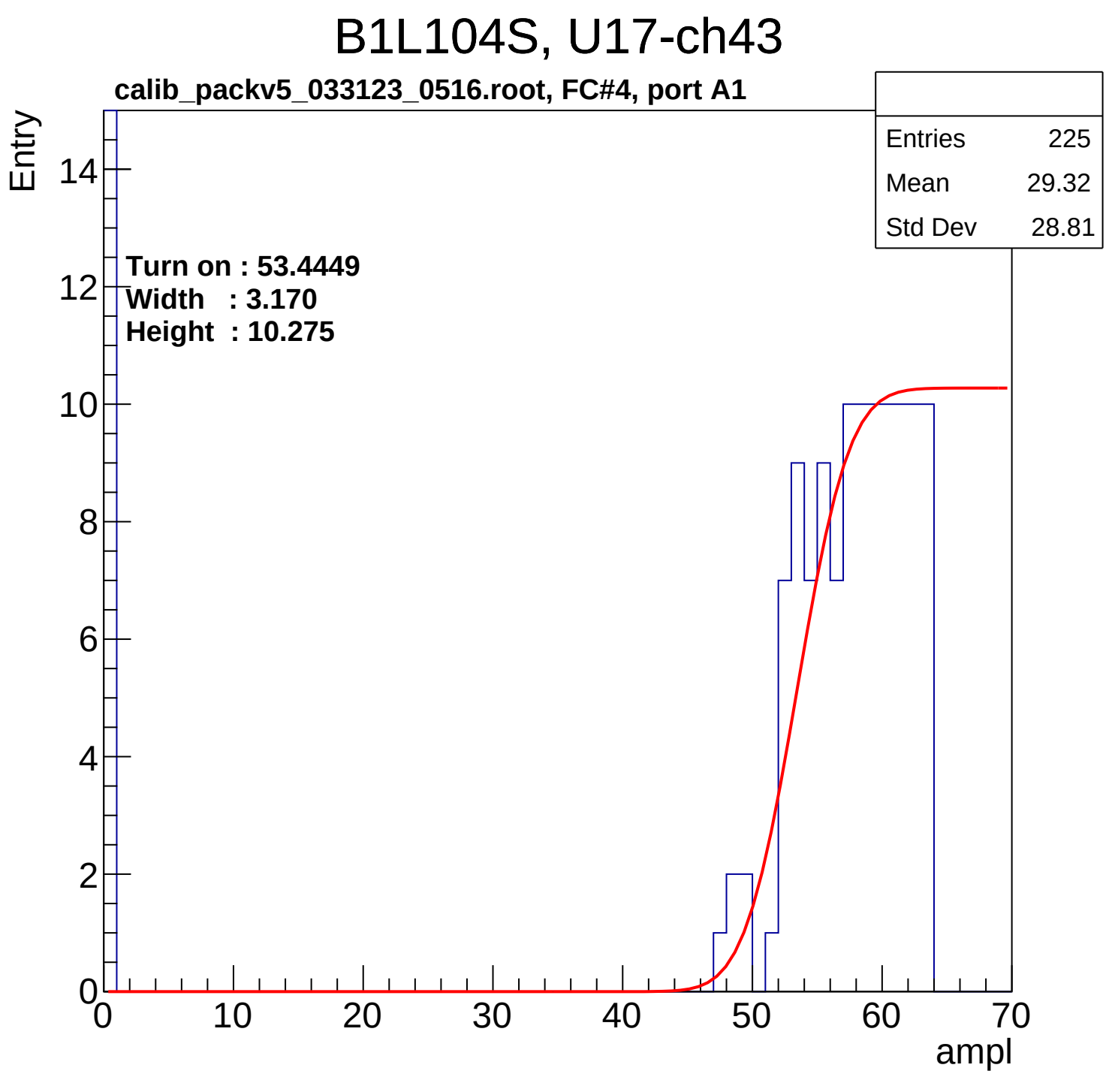
B1L104S, U17-ch43
calib_packv5_033123_0516.root, FC#4, port A1
Entries 225
Mean 29.32
Std Dev 28.81
Turn on : 53.4449
Width : 3.170
Height : 10.275
Entry
ampl
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6
8
10
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0
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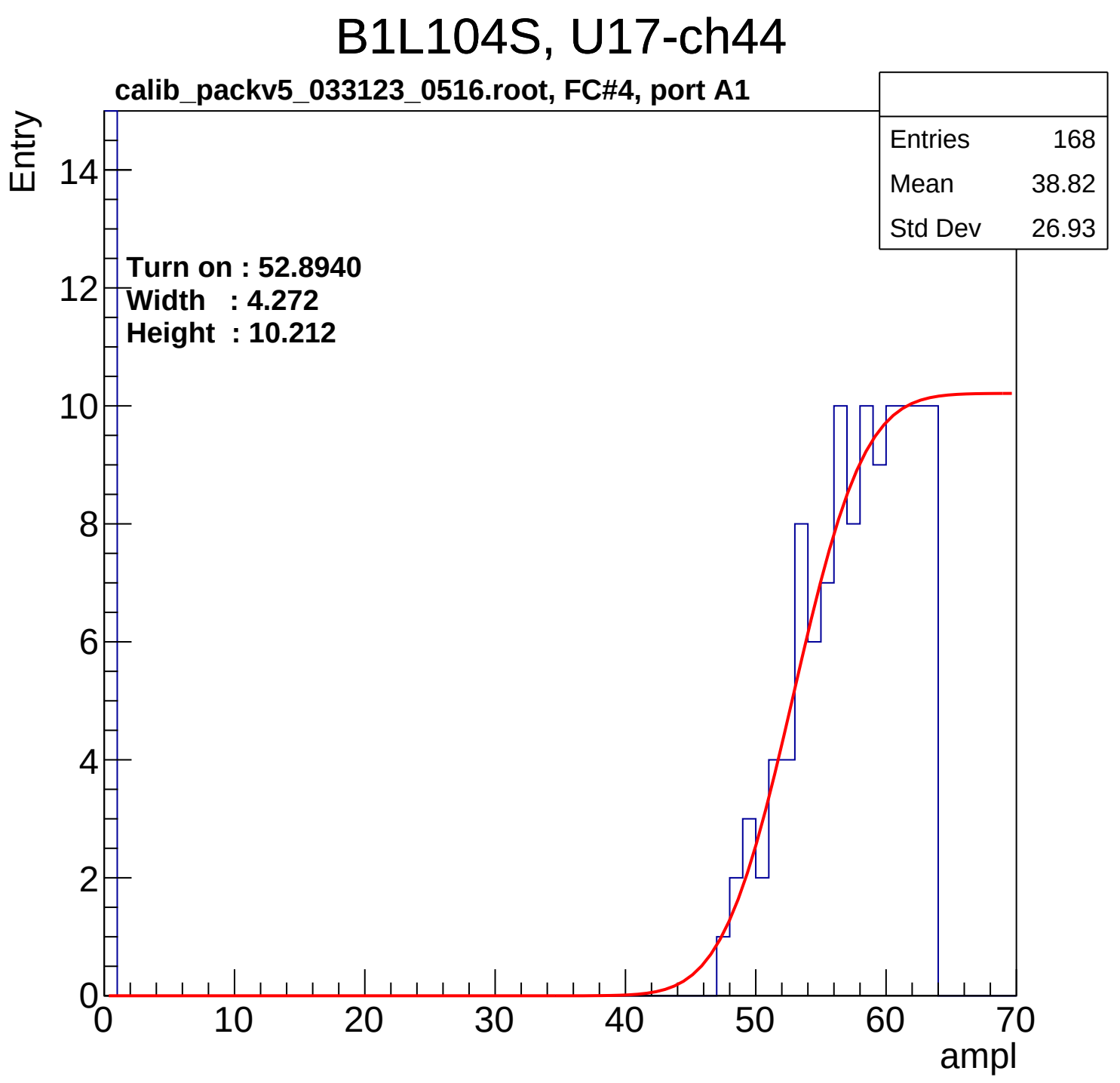
B1L104S, U17-ch44
calib_packv5_033123_0516.root, FC#4, port A1
Entries 168
Mean 38.82
Std Dev 26.93
Turn on : 52.8940
Width : 4.272
Height : 10.212
Entry
ampl
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6
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20
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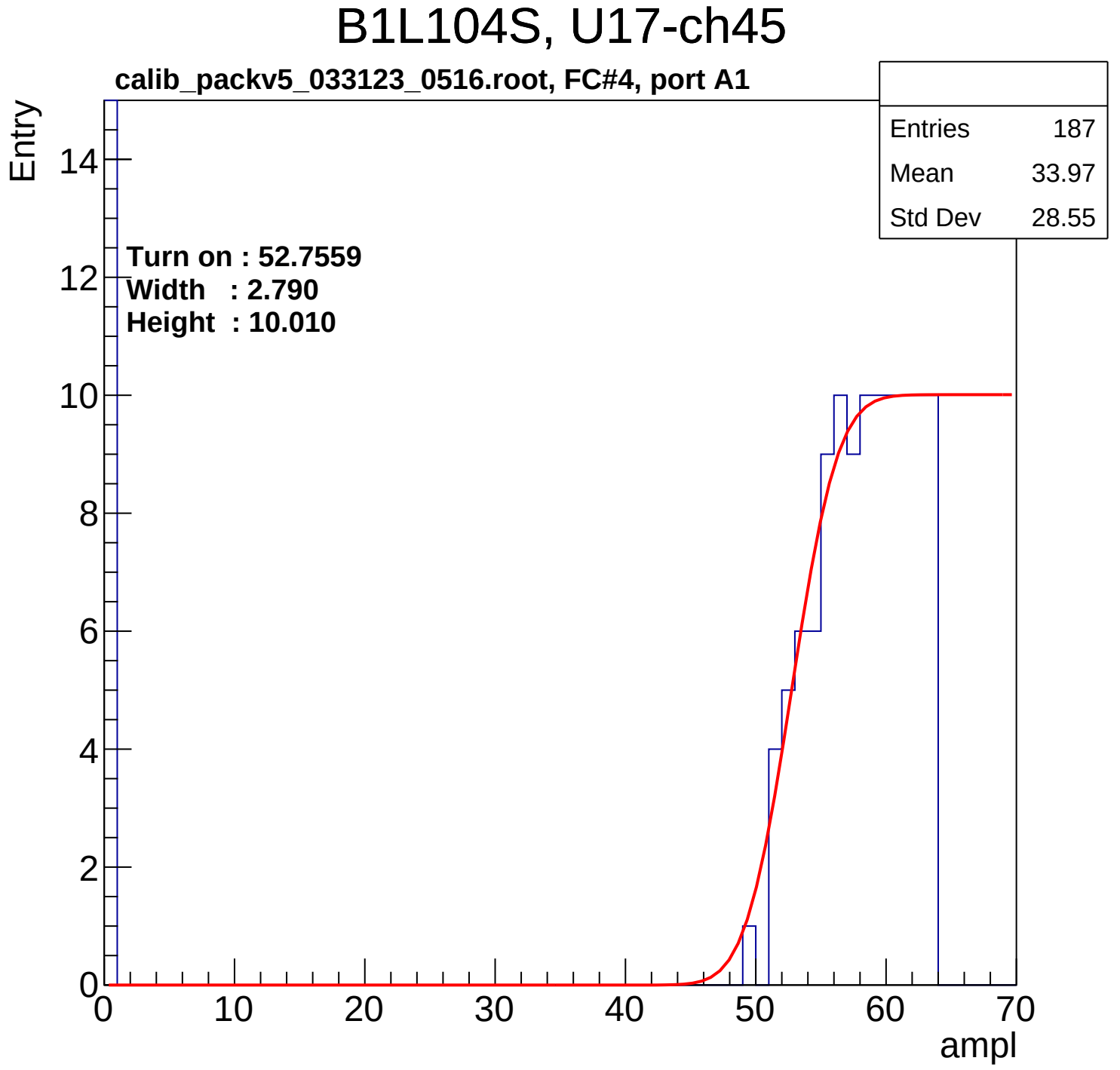
B1L104S, U17-ch45
calib_packv5_033123_0516.root, FC#4, port A1
Entries 187
Mean 33.97
Std Dev 28.55
Turn on : 52.7559
Width : 2.790
Height : 10.010
Entry
ampl
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6
8
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0
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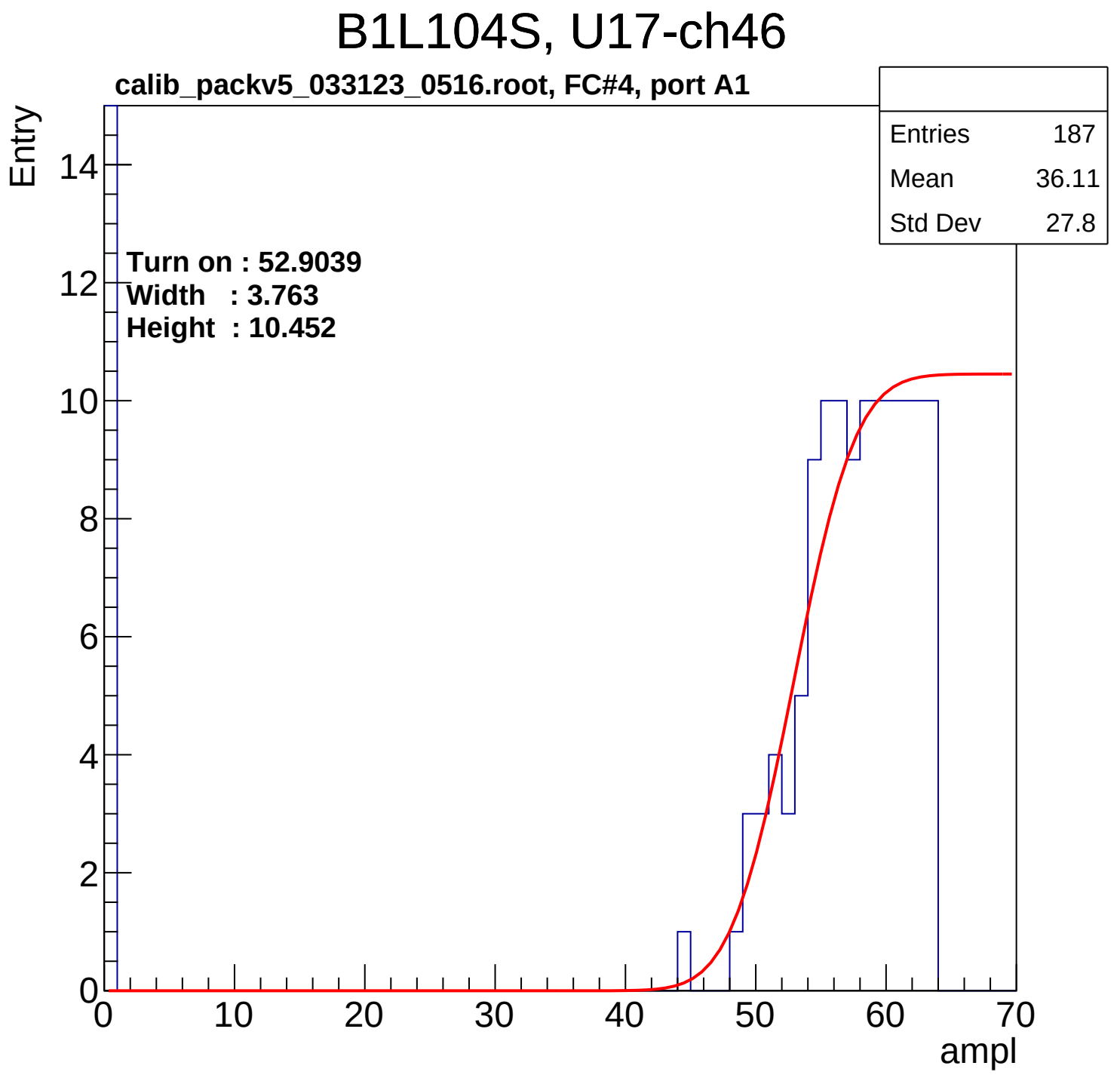
B1L104S, U17-ch46
calib_packv5_033123_0516.root, FC#4, port A1
Entries 187
Mean 36.11
Std Dev 27.8
Turn on : 52.9039
Width : 3.763
Height : 10.452
Entry
ampl
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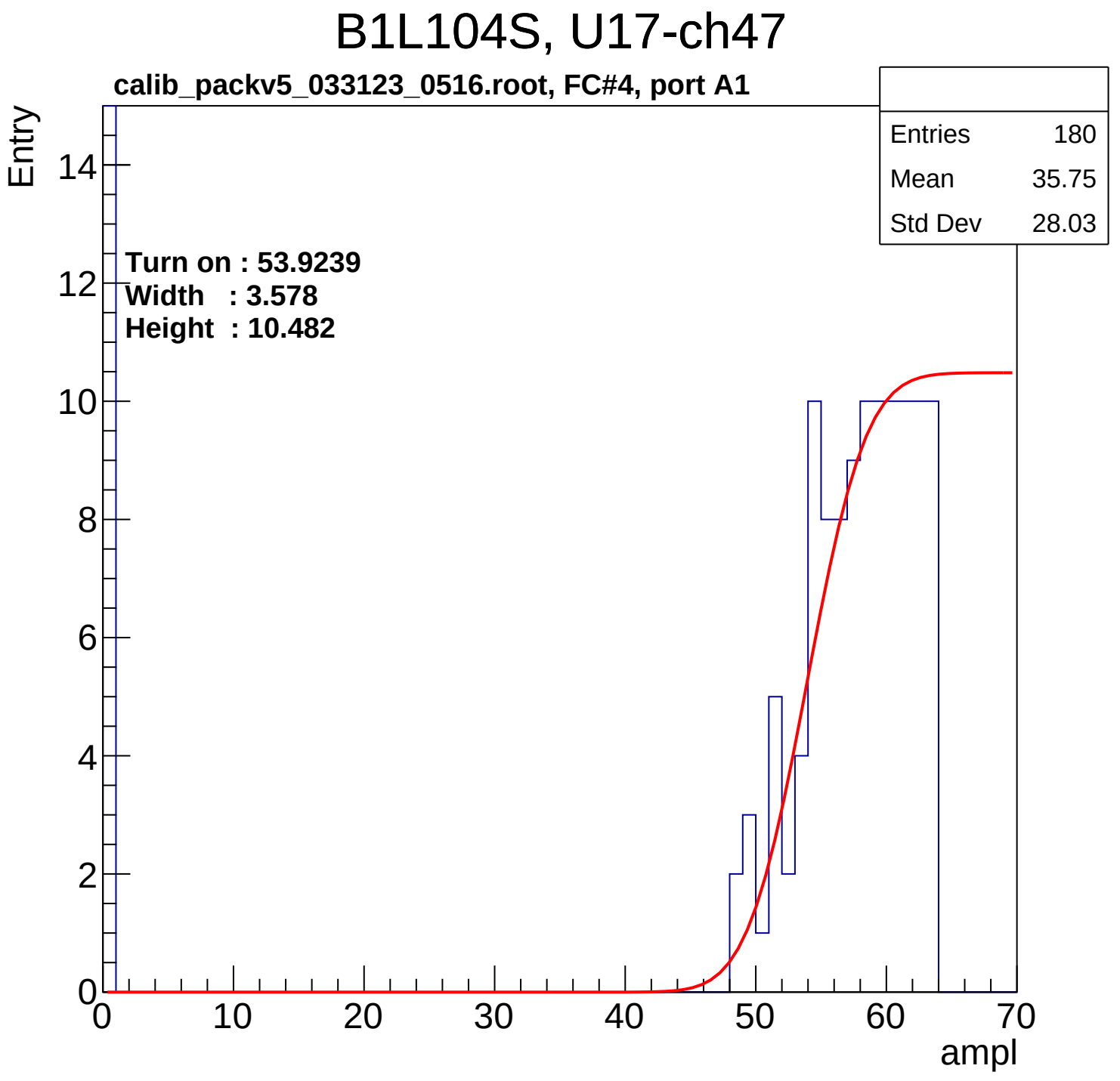
B1L104S, U17-ch47
calib_packv5_033123_0516.root, FC#4, port A1
Entries 180
Mean 35.75
Std Dev 28.03
Turn on : 53.9239
Width : 3.578
Height : 10.482
Entry
ampl
0
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4
6
8
10
12
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0
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60
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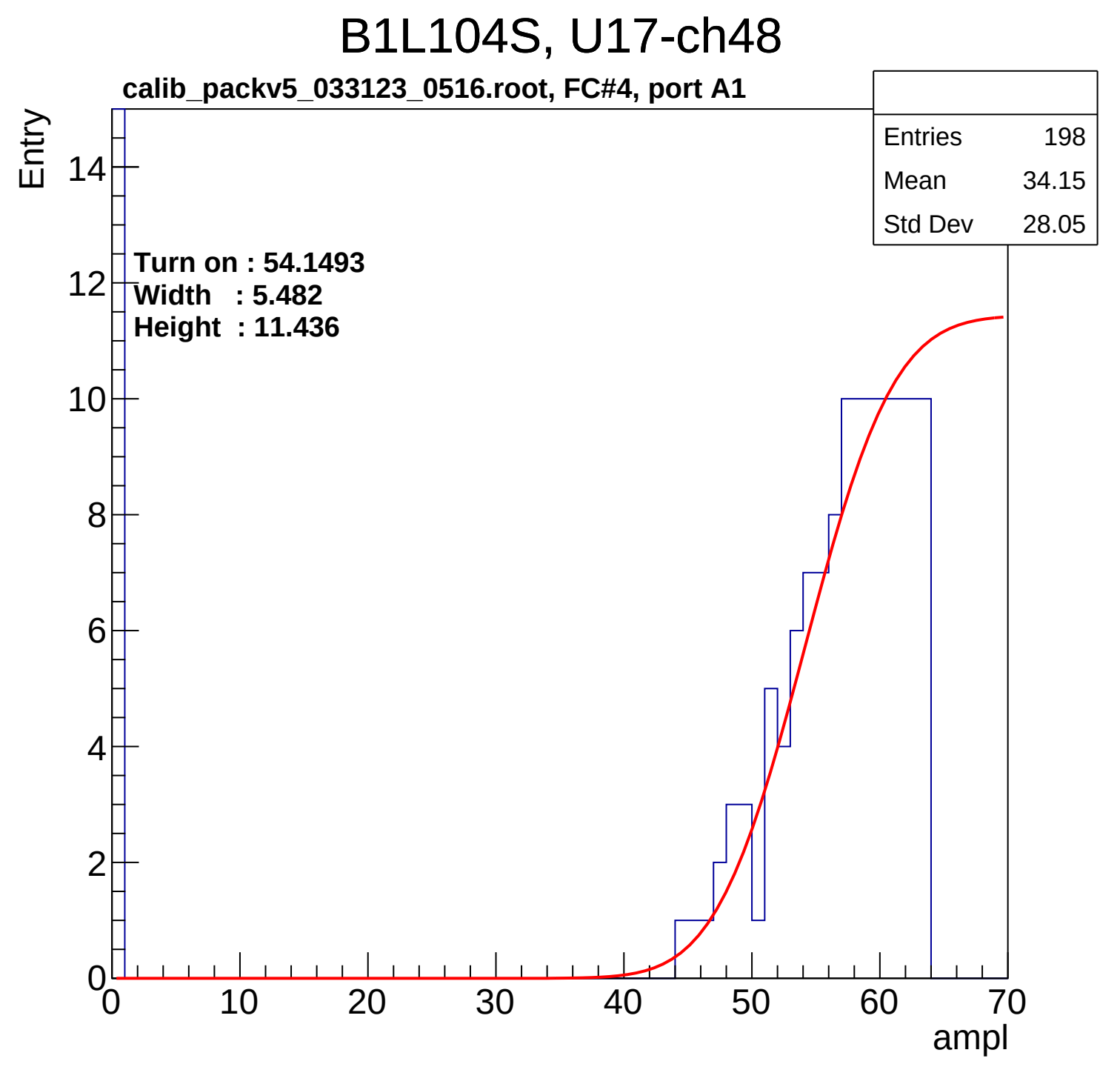
B1L104S, U17-ch48
calib_packv5_033123_0516.root, FC#4, port A1
Entries 198
Mean 34.15
Std Dev 28.05
Turn on : 54.1493
Width : 5.482
Height : 11.436
Entry
ampl
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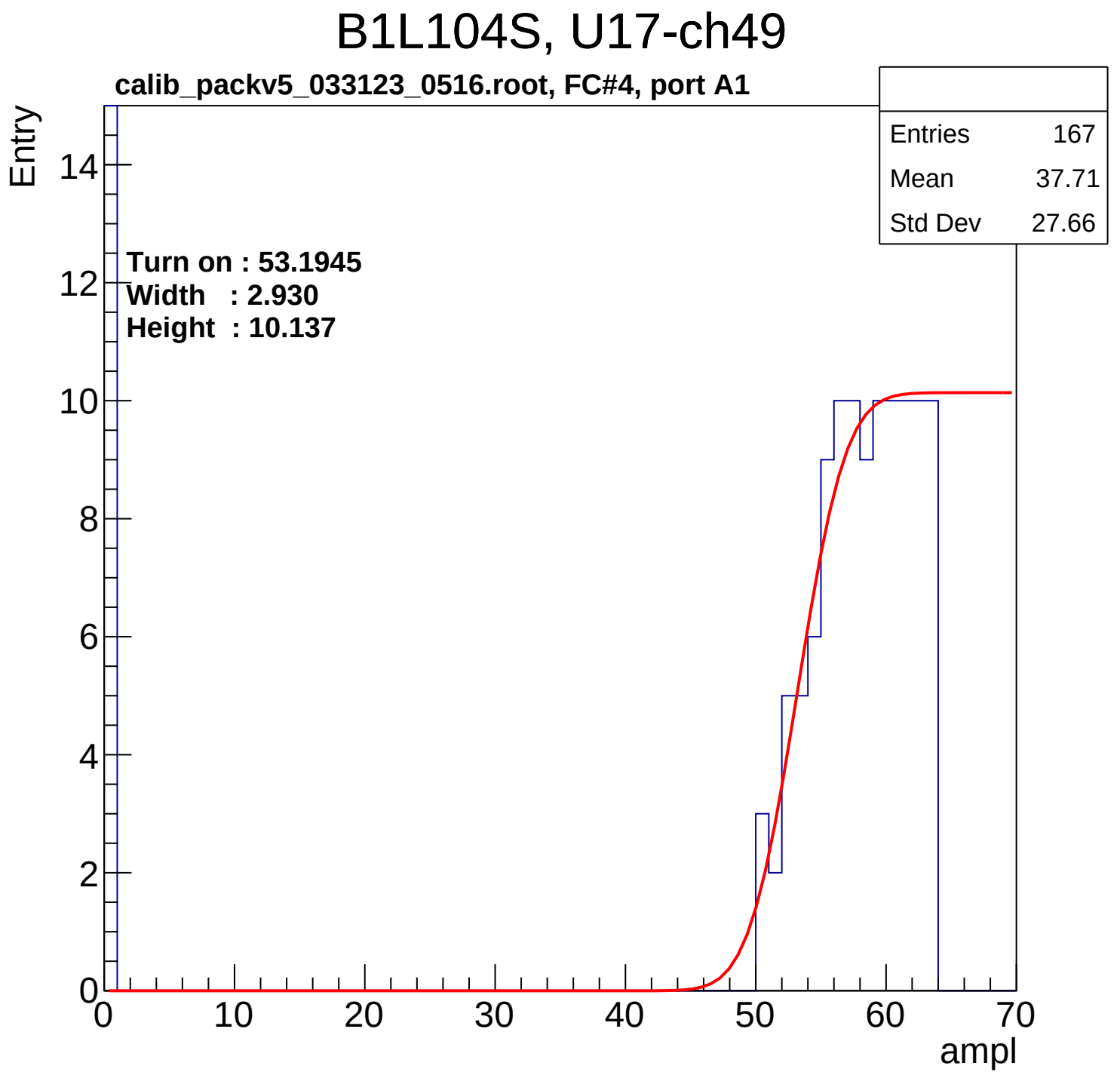
B1L104S, U17-ch49
calib_packv5_033123_0516.root, FC#4, port A1
Entries 167
Mean 37.71
Std Dev 27.66
Turn on : 53.1945
Width : 2.930
Height : 10.137
Entry
ampl
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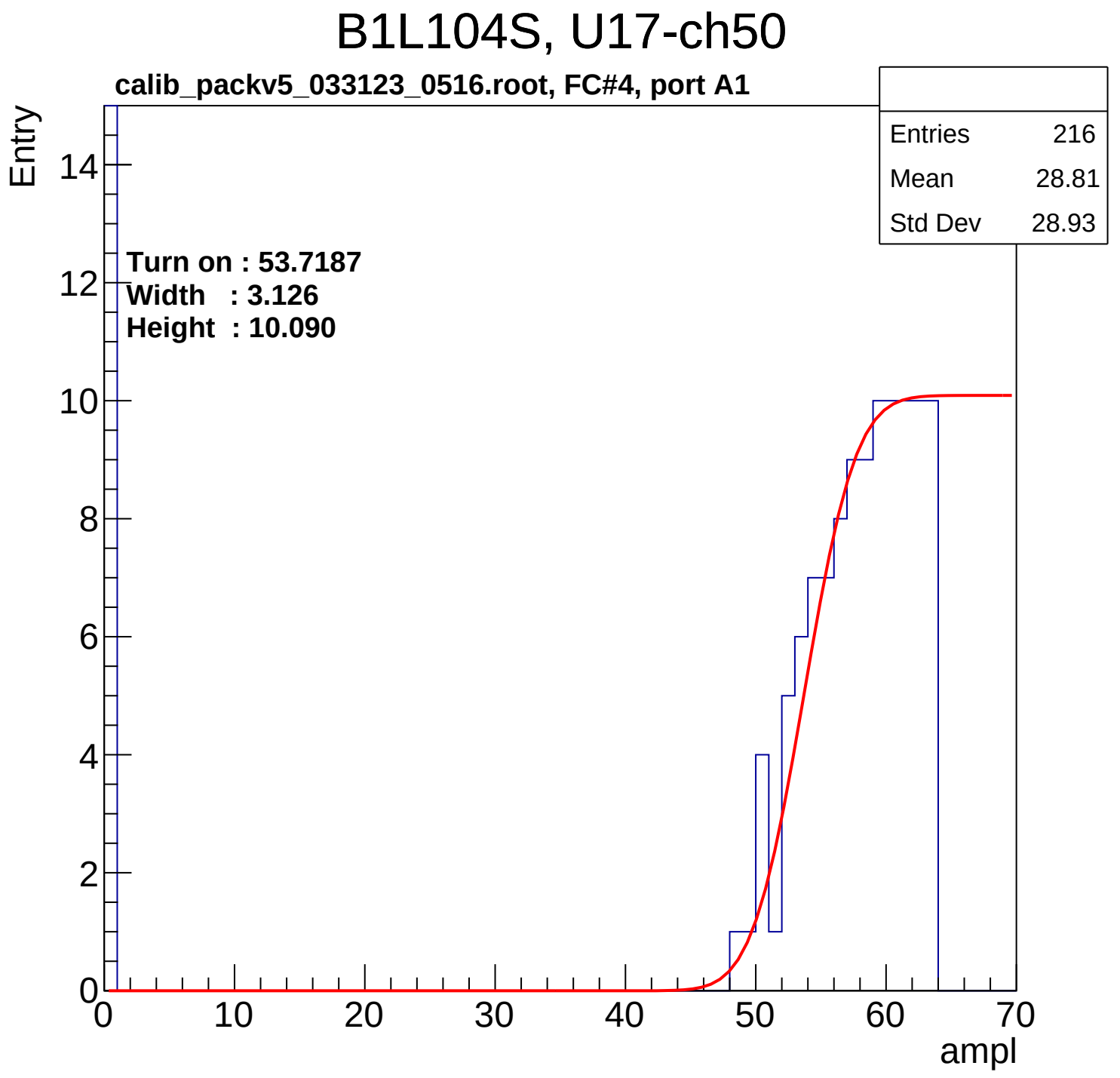
B1L104S, U17-ch50
calib_packv5_033123_0516.root, FC#4, port A1
Entries 216
Mean 28.81
Std Dev 28.93
Turn on : 53.7187
Width : 3.126
Height : 10.090
Entry
ampl
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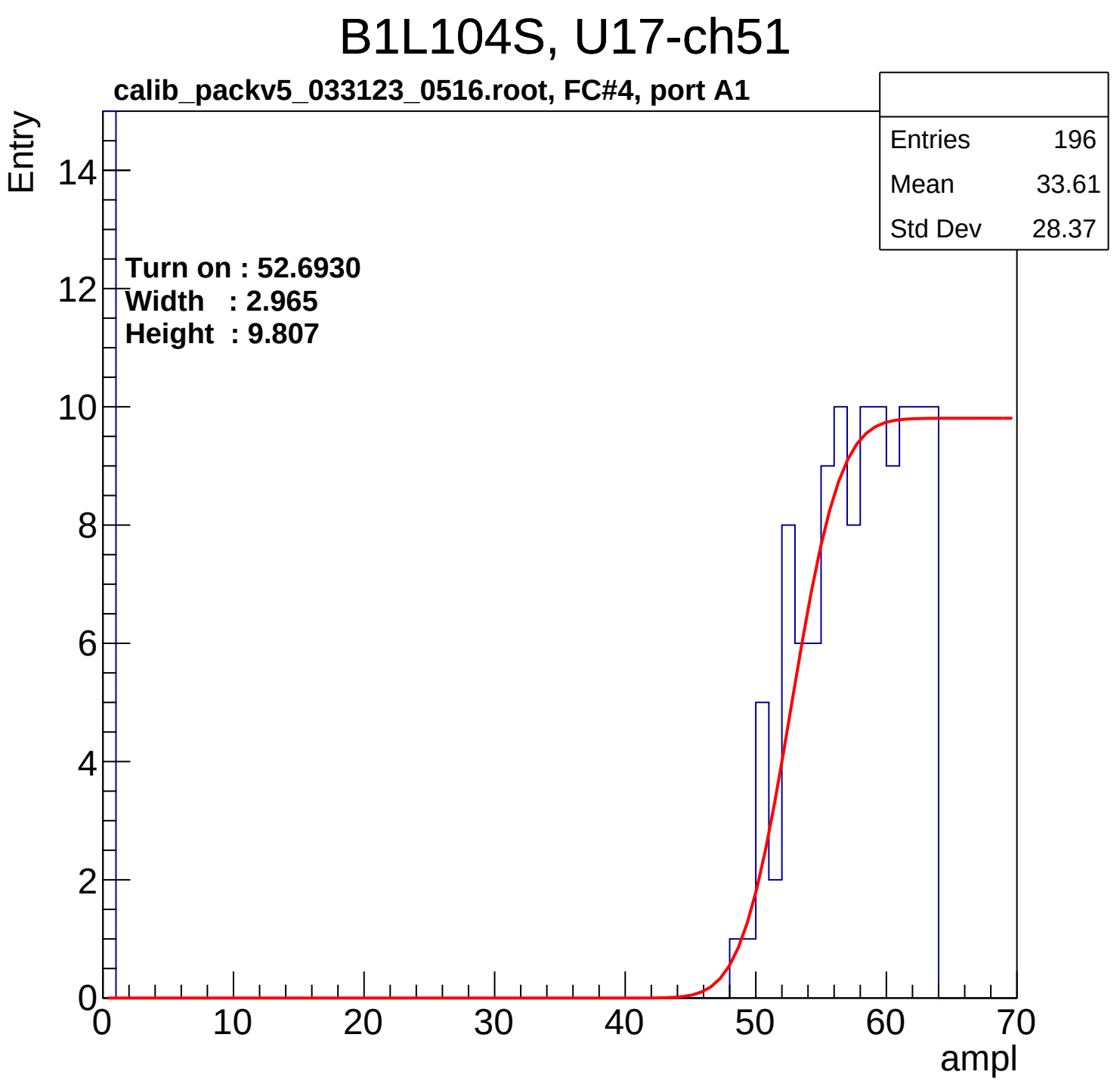
B1L104S, U17-ch51
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 33.61
Std Dev 28.37
Turn on : 52.6930
Width : 2.965
Height : 9.807
Entry
ampl
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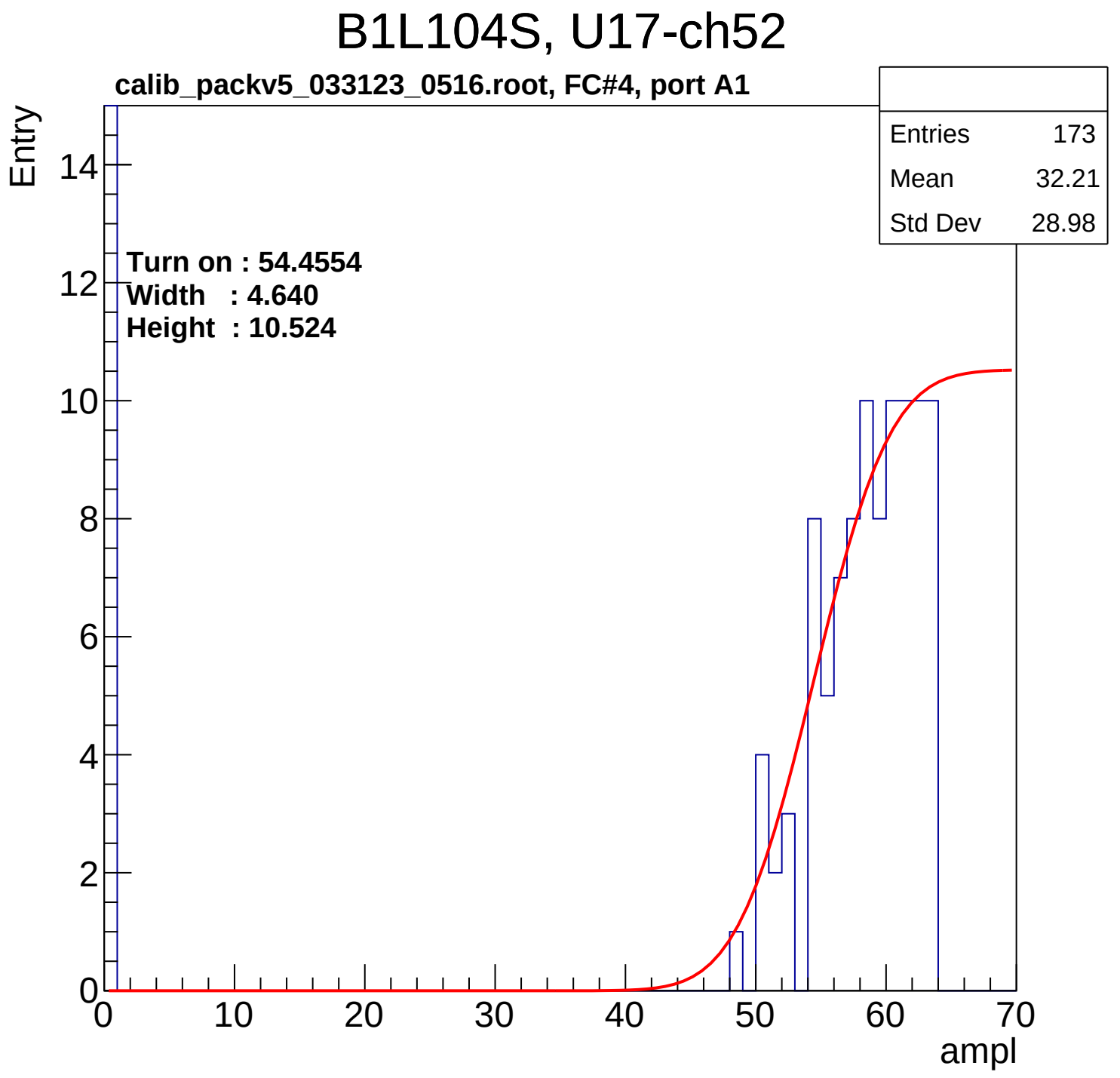
B1L104S, U17-ch52
calib_packv5_033123_0516.root, FC#4, port A1
Entries 173
Mean 32.21
Std Dev 28.98
Turn on : 54.4554
Width : 4.640
Height : 10.524
Entry
ampl
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8
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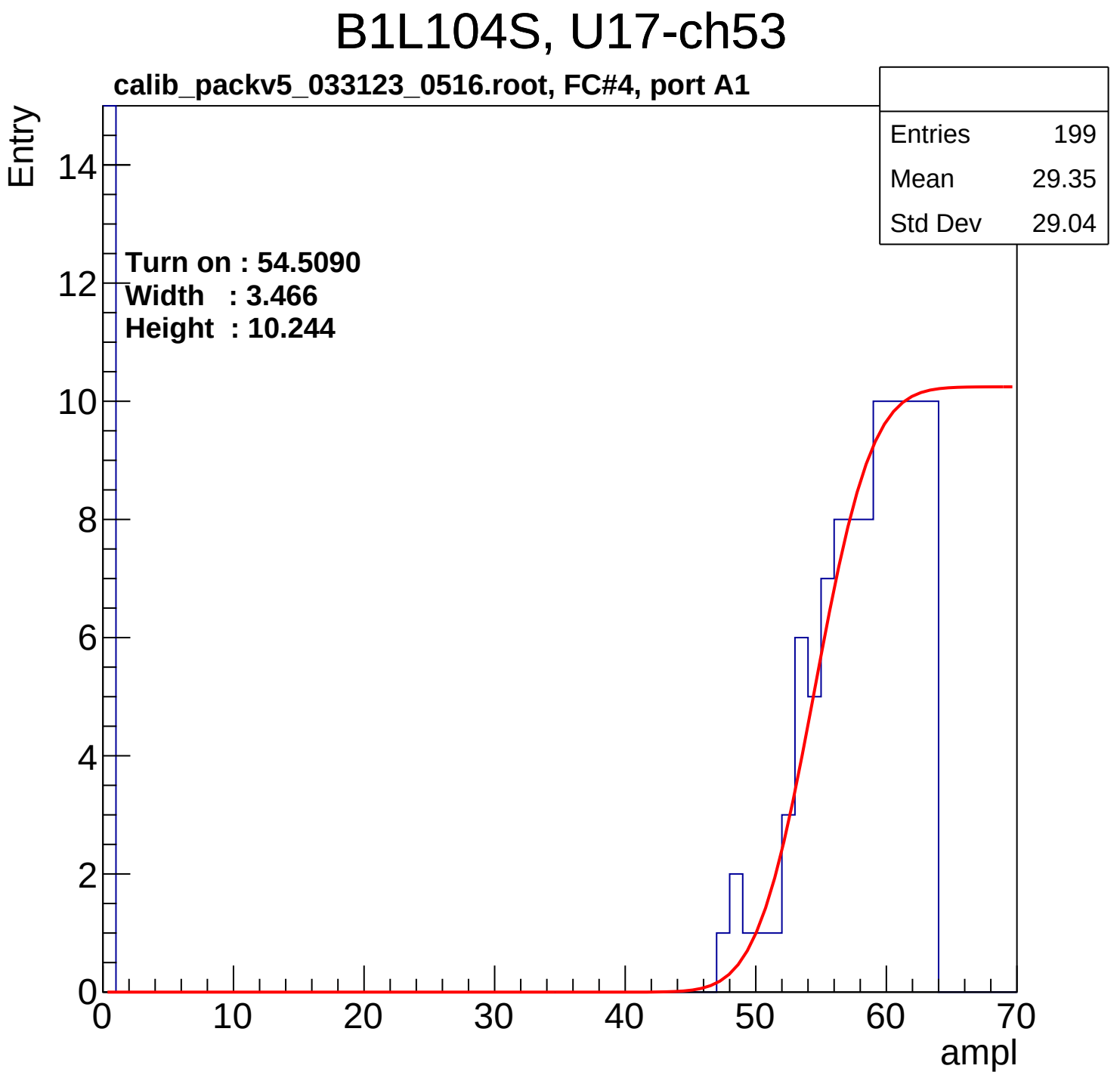
B1L104S, U17-ch53
calib_packv5_033123_0516.root, FC#4, port A1
Entries 199
Mean 29.35
Std Dev 29.04
Turn on : 54.5090
Width : 3.466
Height : 10.244
Entry
ampl
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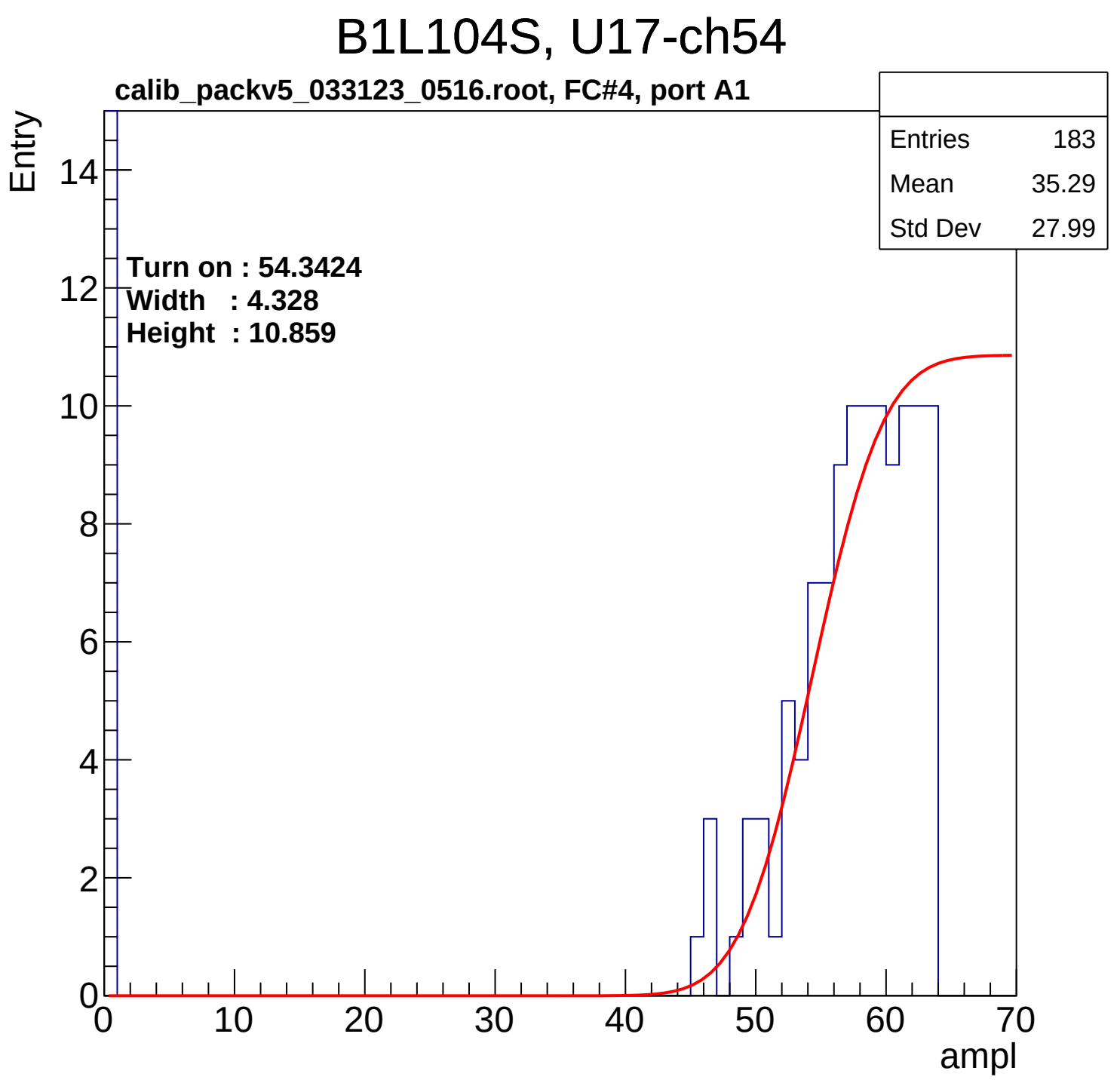
B1L104S, U17-ch54
calib_packv5_033123_0516.root, FC#4, port A1
Entries 183
Mean 35.29
Std Dev 27.99
Turn on : 54.3424
Width : 4.328
Height : 10.859
Entry
ampl
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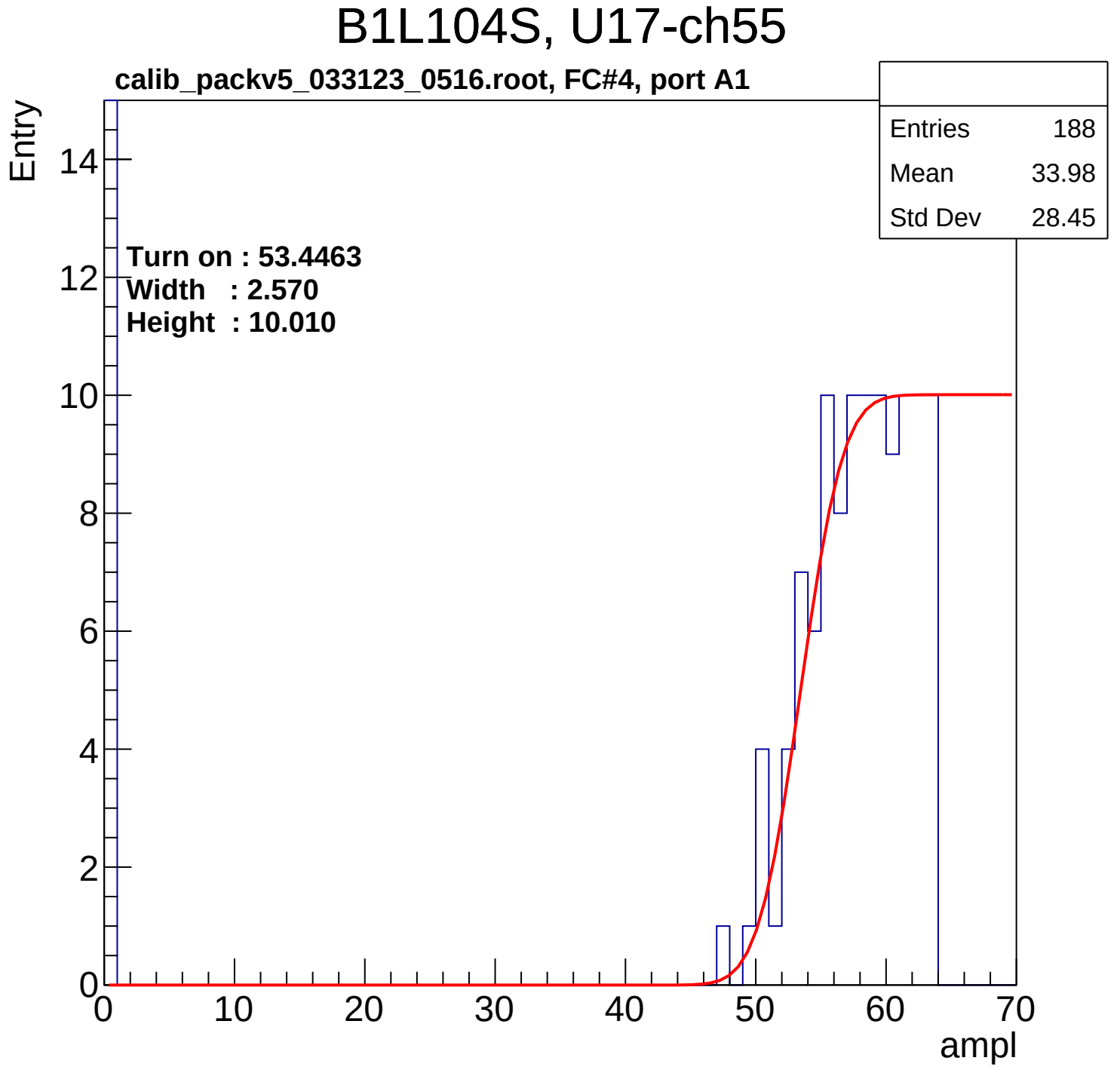
B1L104S, U17-ch55
calib_packv5_033123_0516.root, FC#4, port A1
Entries 188
Mean 33.98
Std Dev 28.45
Turn on : 53.4463
Width : 2.570
Height : 10.010
Entry
ampl
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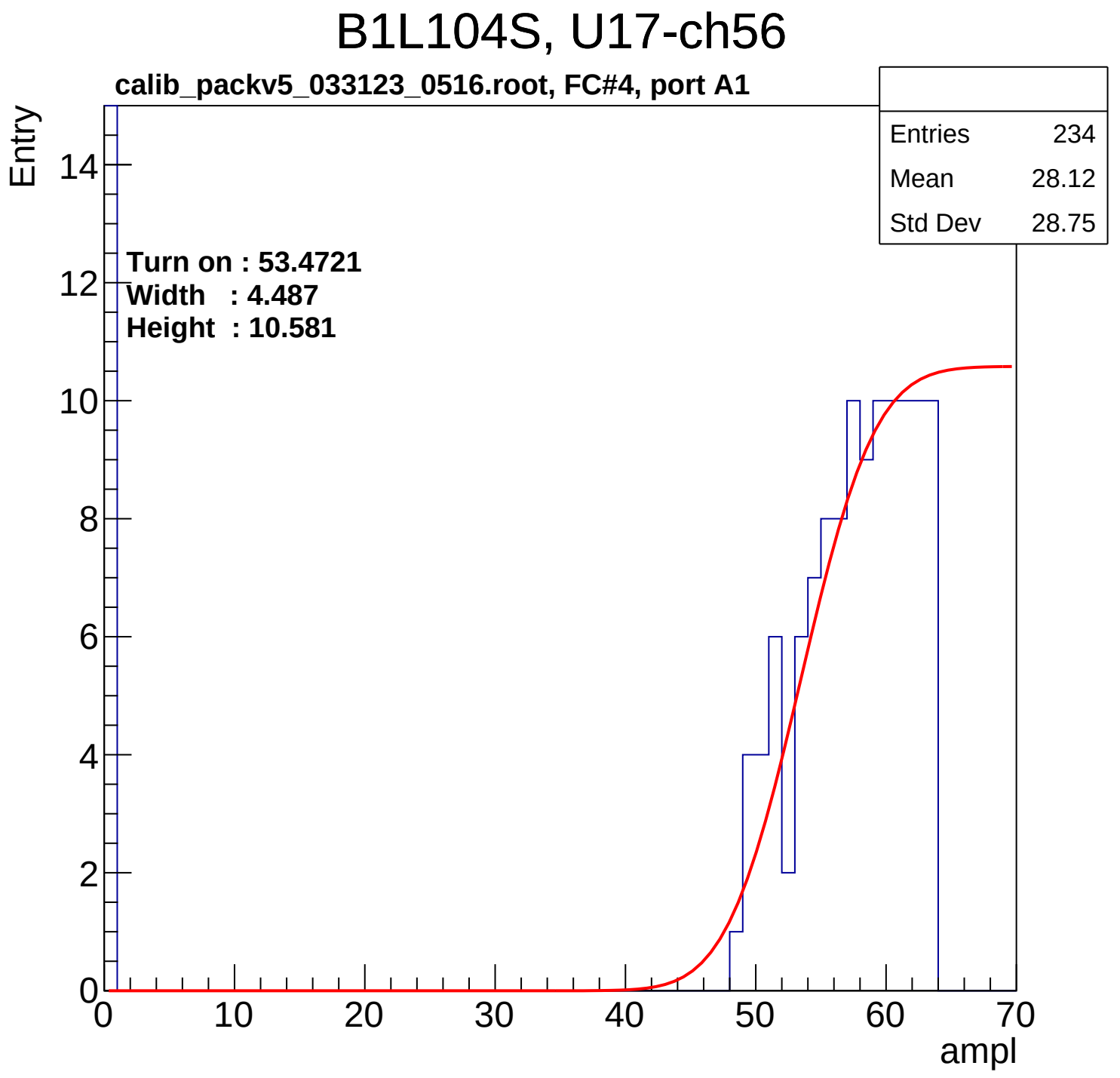
B1L104S, U17-ch56
calib_packv5_033123_0516.root, FC#4, port A1
Entries 234
Mean 28.12
Std Dev 28.75
Turn on : 53.4721
Width : 4.487
Height : 10.581
Entry
ampl
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4
6
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10
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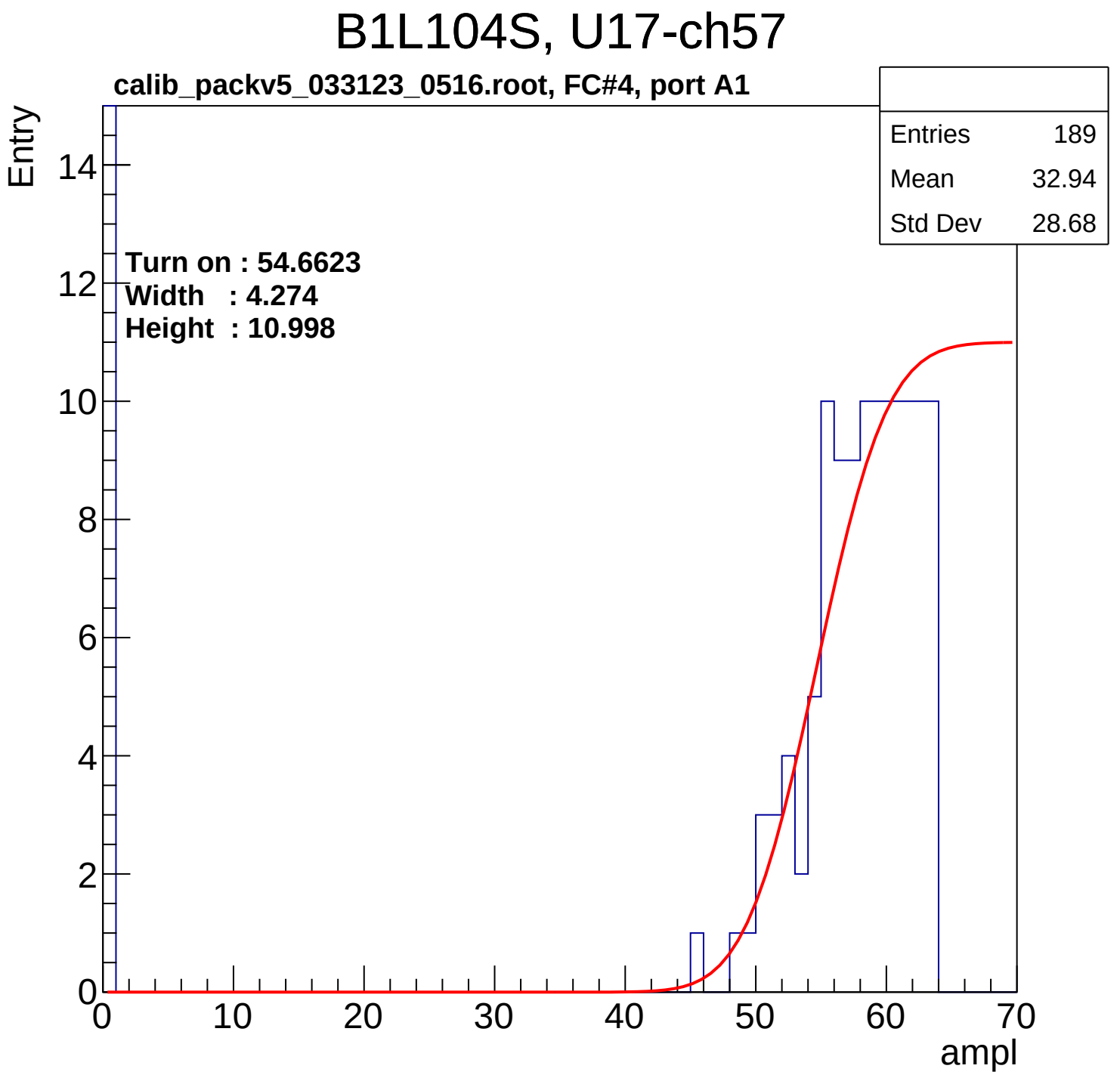
B1L104S, U17-ch57
calib_packv5_033123_0516.root, FC#4, port A1
Entries 189
Mean 32.94
Std Dev 28.68
Turn on : 54.6623
Width : 4.274
Height : 10.998
Entry
ampl
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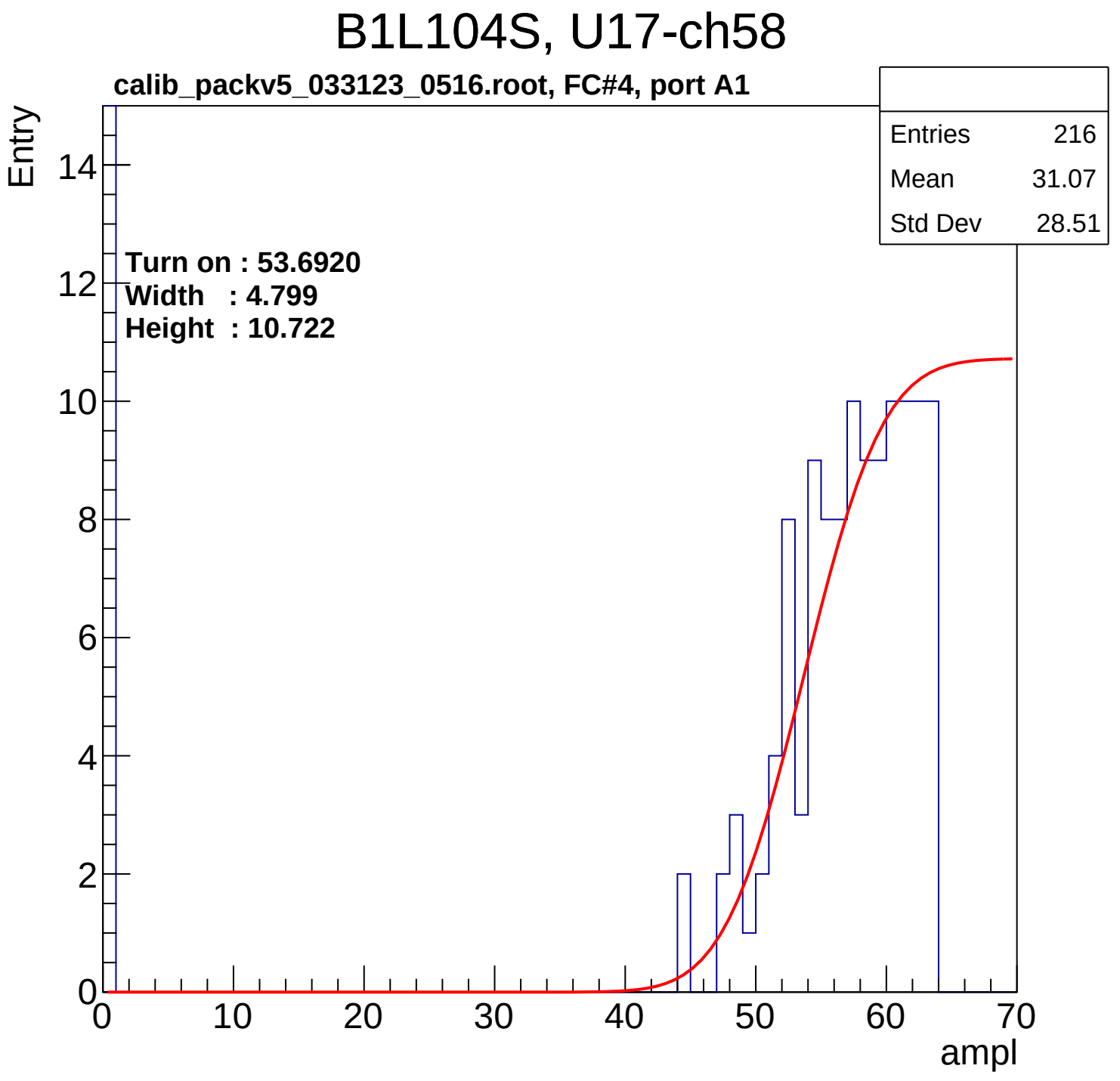
B1L104S, U17-ch58
calib_packv5_033123_0516.root, FC#4, port A1
Entries 216
Mean 31.07
Std Dev 28.51
Turn on : 53.6920
Width : 4.799
Height : 10.722
Entry
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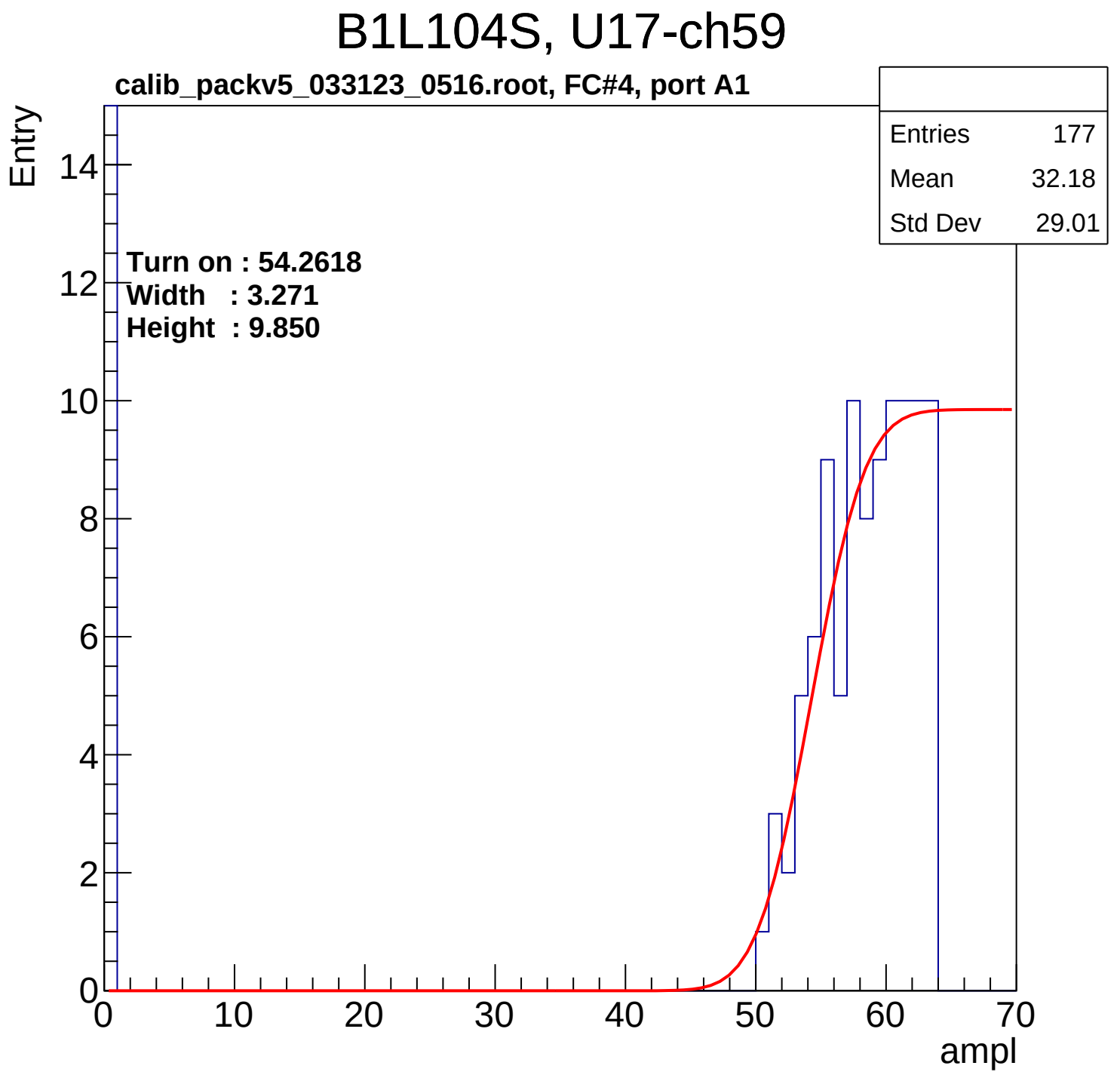
B1L104S, U17-ch59
calib_packv5_033123_0516.root, FC#4, port A1
Entries 177
Mean 32.18
Std Dev 29.01
Turn on : 54.2618
Width : 3.271
Height : 9.850
Entry
ampl
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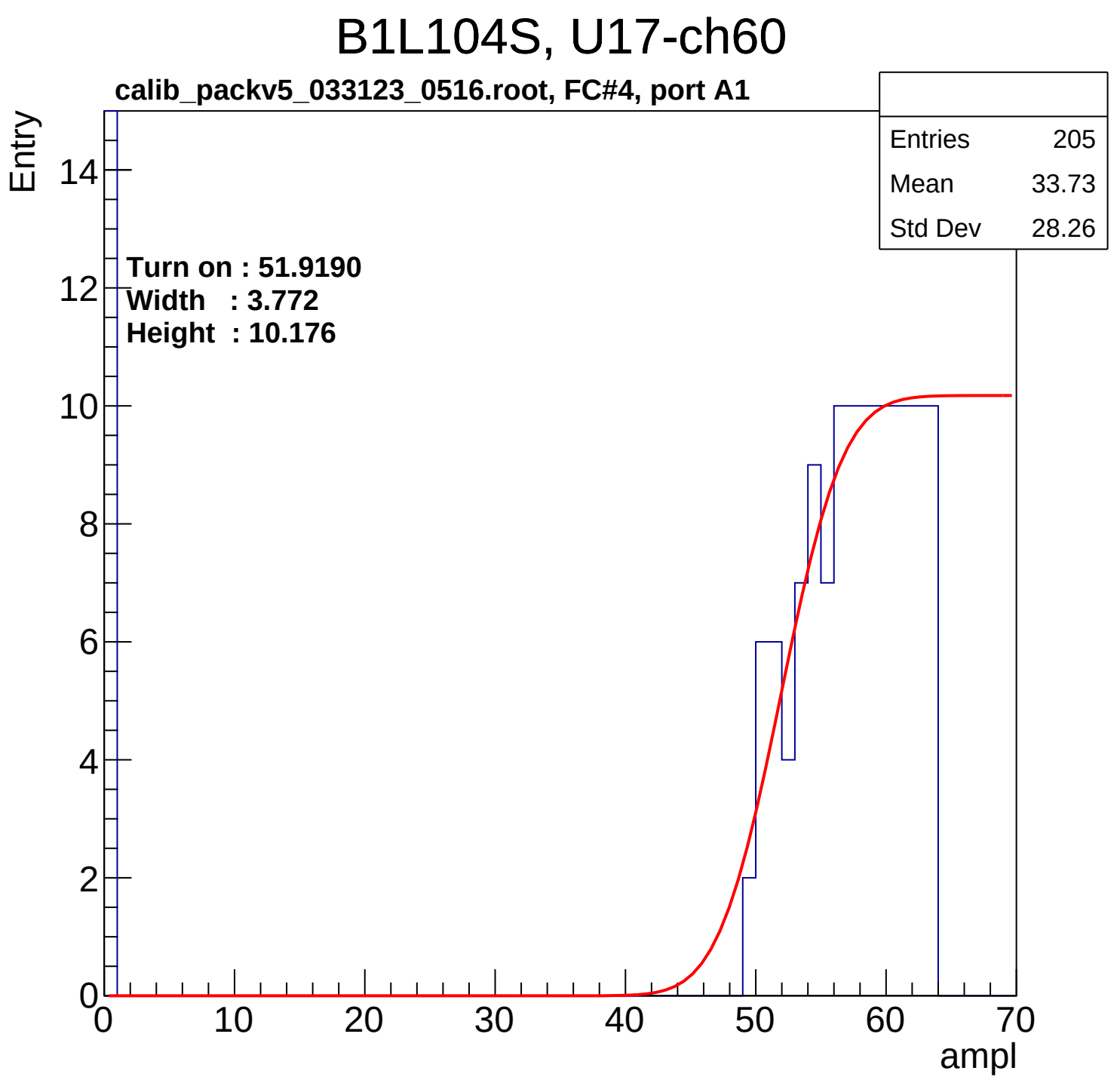
B1L104S, U17-ch60
calib_packv5_033123_0516.root, FC#4, port A1
Entries 205
Mean 33.73
Std Dev 28.26
Turn on : 51.9190
Width : 3.772
Height : 10.176
Entry
ampl
0
2
4
6
8
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12
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10
20
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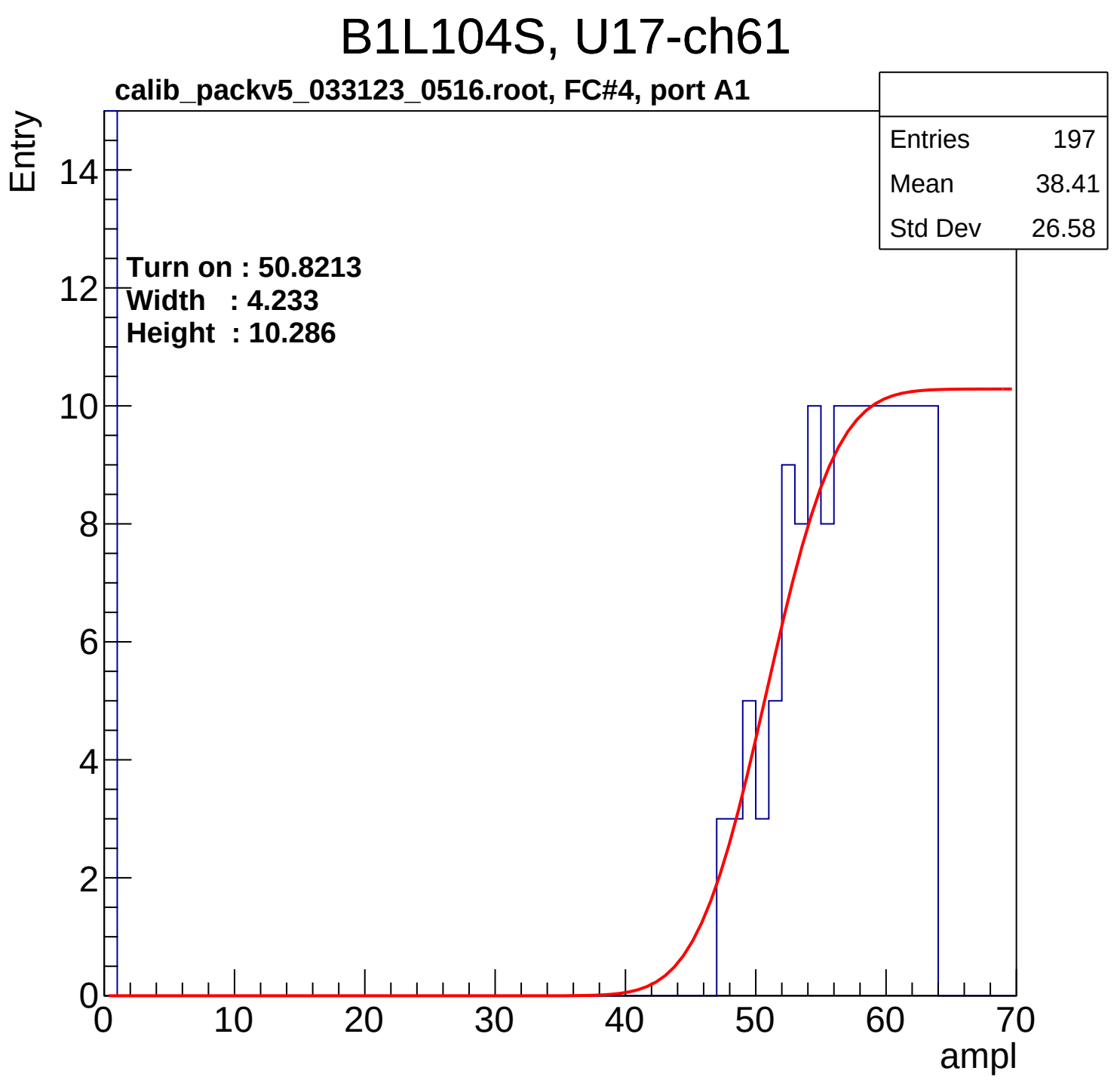
B1L104S, U17-ch61
calib_packv5_033123_0516.root, FC#4, port A1
Entries 197
Mean 38.41
Std Dev 26.58
Turn on : 50.8213
Width : 4.233
Height : 10.286
Entry
ampl
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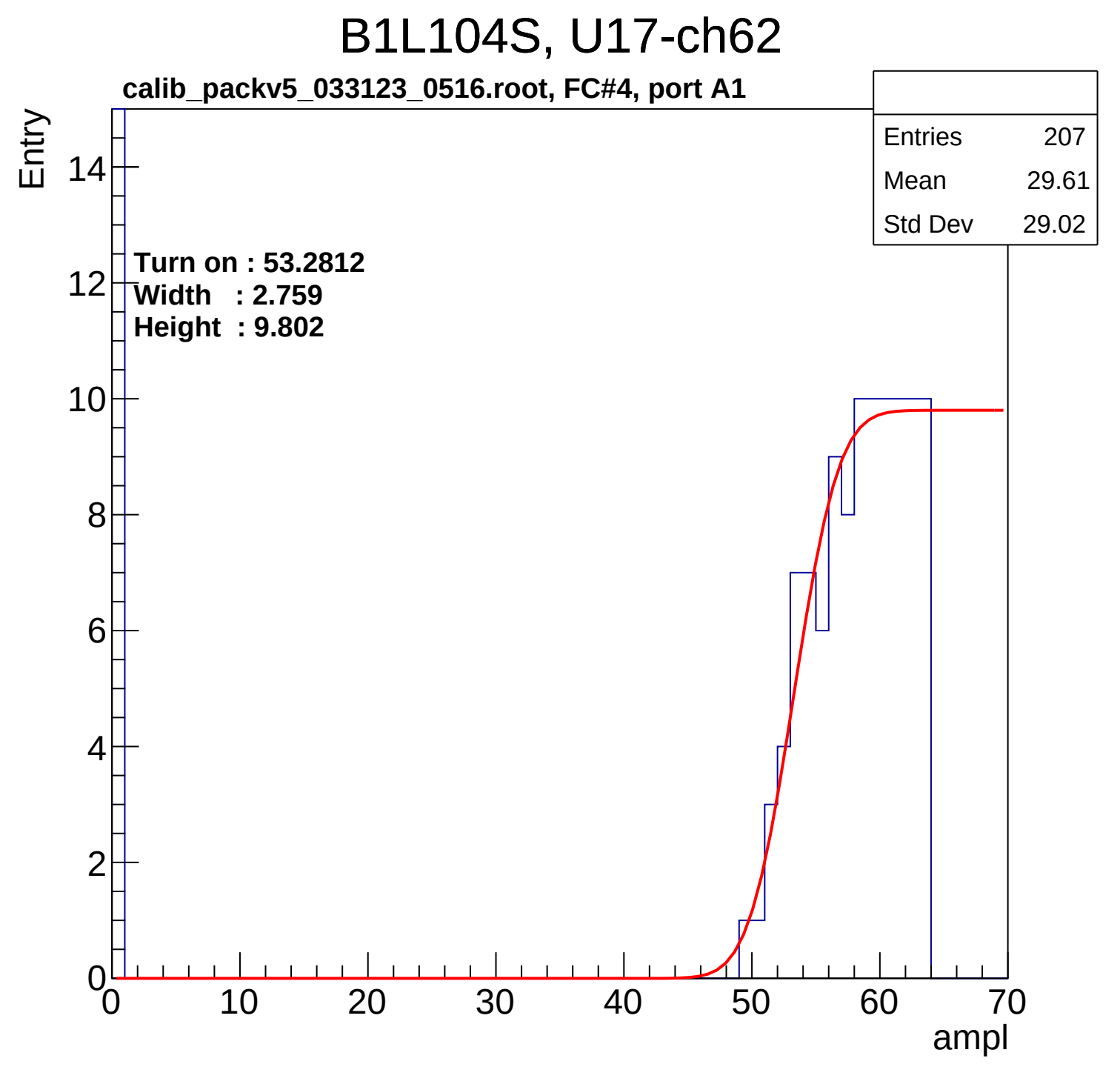
B1L104S, U17-ch62
calib_packv5_033123_0516.root, FC#4, port A1
Entries 207
Mean 29.61
Std Dev 29.02
Turn on : 53.2812
Width : 2.759
Height : 9.802
Entry
ampl
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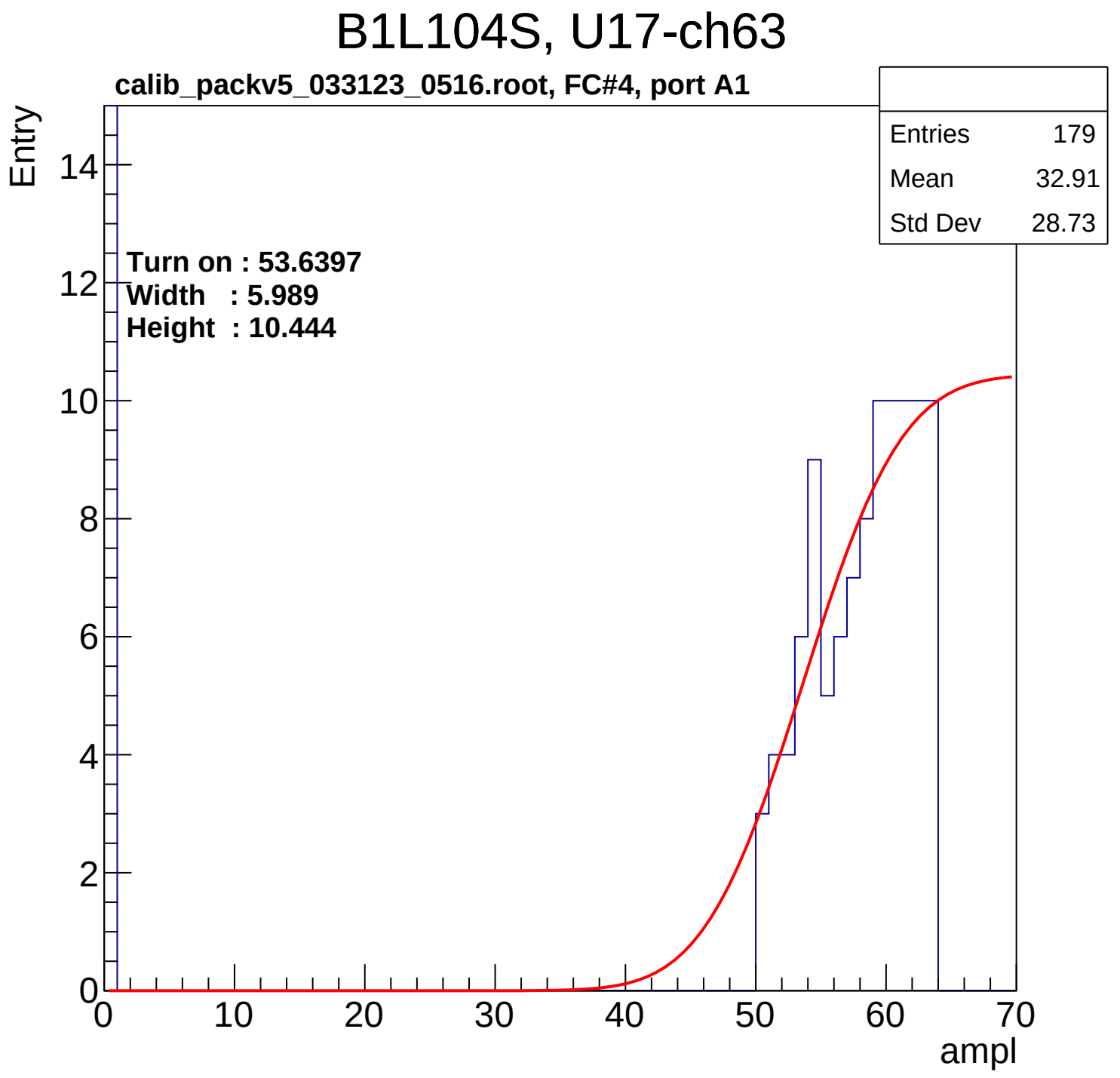
B1L104S, U17-ch63
calib_packv5_033123_0516.root, FC#4, port A1
Entries 179
Mean 32.91
Std Dev 28.73
Turn on : 53.6397
Width : 5.989
Height : 10.444
Entry
ampl
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4
6
8
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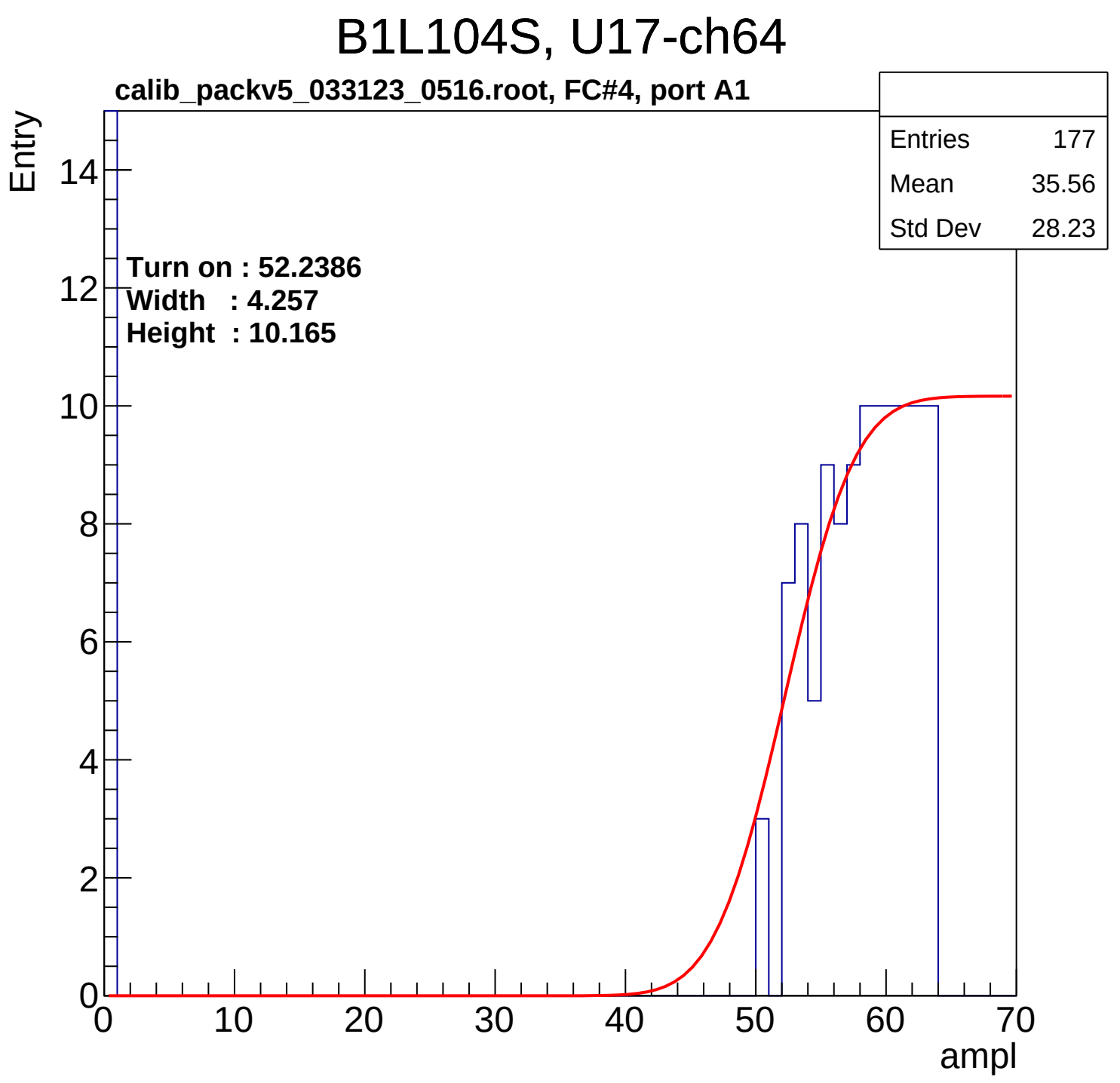
B1L104S, U17-ch64
calib_packv5_033123_0516.root, FC#4, port A1
Entries 177
Mean 35.56
Std Dev 28.23
Turn on : 52.2386
Width : 4.257
Height : 10.165
Entry
ampl
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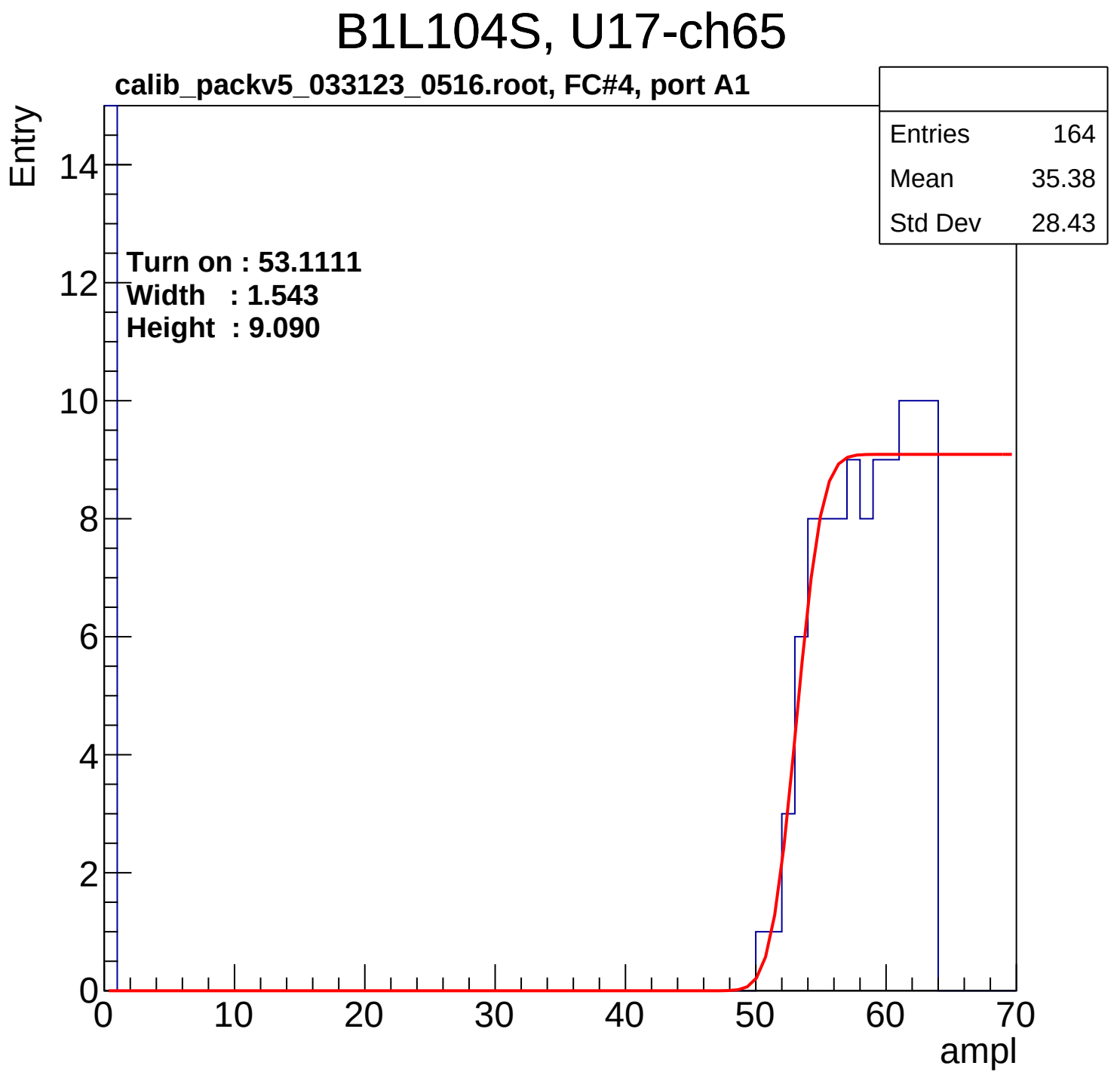
B1L104S, U17-ch65
calib_packv5_033123_0516.root, FC#4, port A1
Entries 164
Mean 35.38
Std Dev 28.43
Turn on : 53.1111
Width : 1.543
Height : 9.090
Entry
ampl
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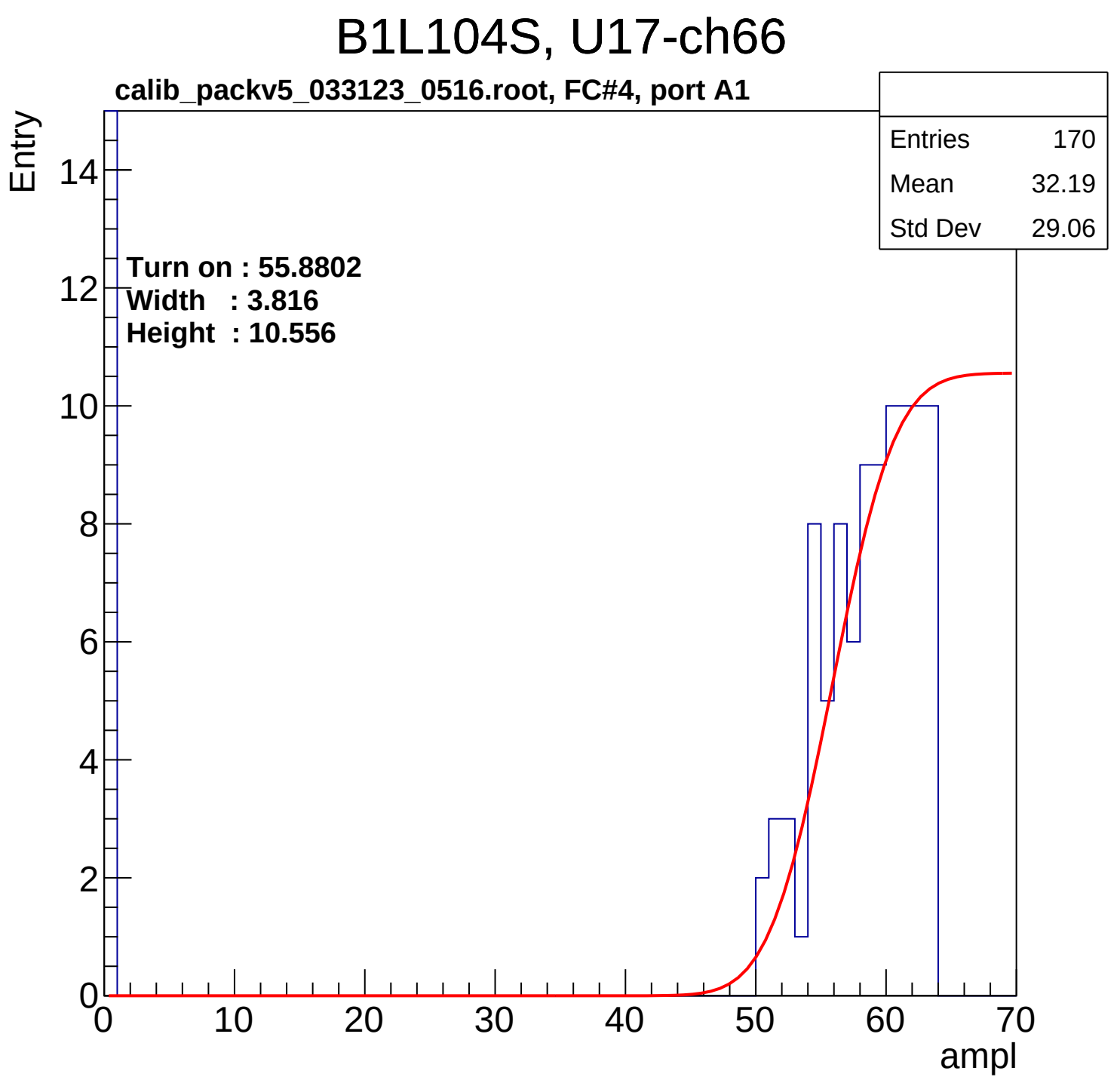
B1L104S, U17-ch66
calib_packv5_033123_0516.root, FC#4, port A1
Entries 170
Mean 32.19
Std Dev 29.06
Turn on : 55.8802
Width : 3.816
Height : 10.556
Entry
ampl
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8
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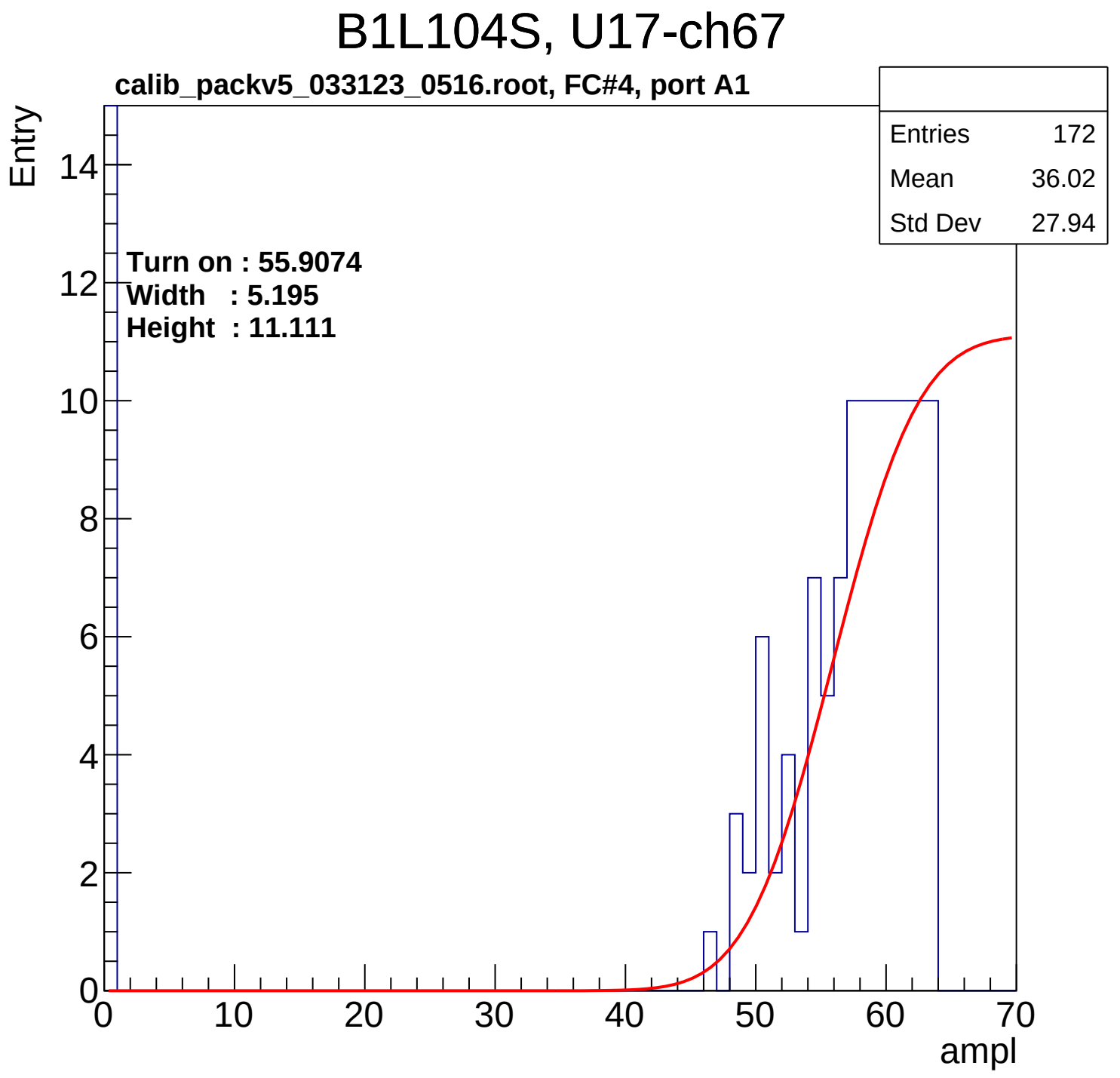
B1L104S, U17-ch67
calib_packv5_033123_0516.root, FC#4, port A1
Entries 172
Mean 36.02
Std Dev 27.94
Turn on : 55.9074
Width : 5.195
Height : 11.111
Entry
ampl
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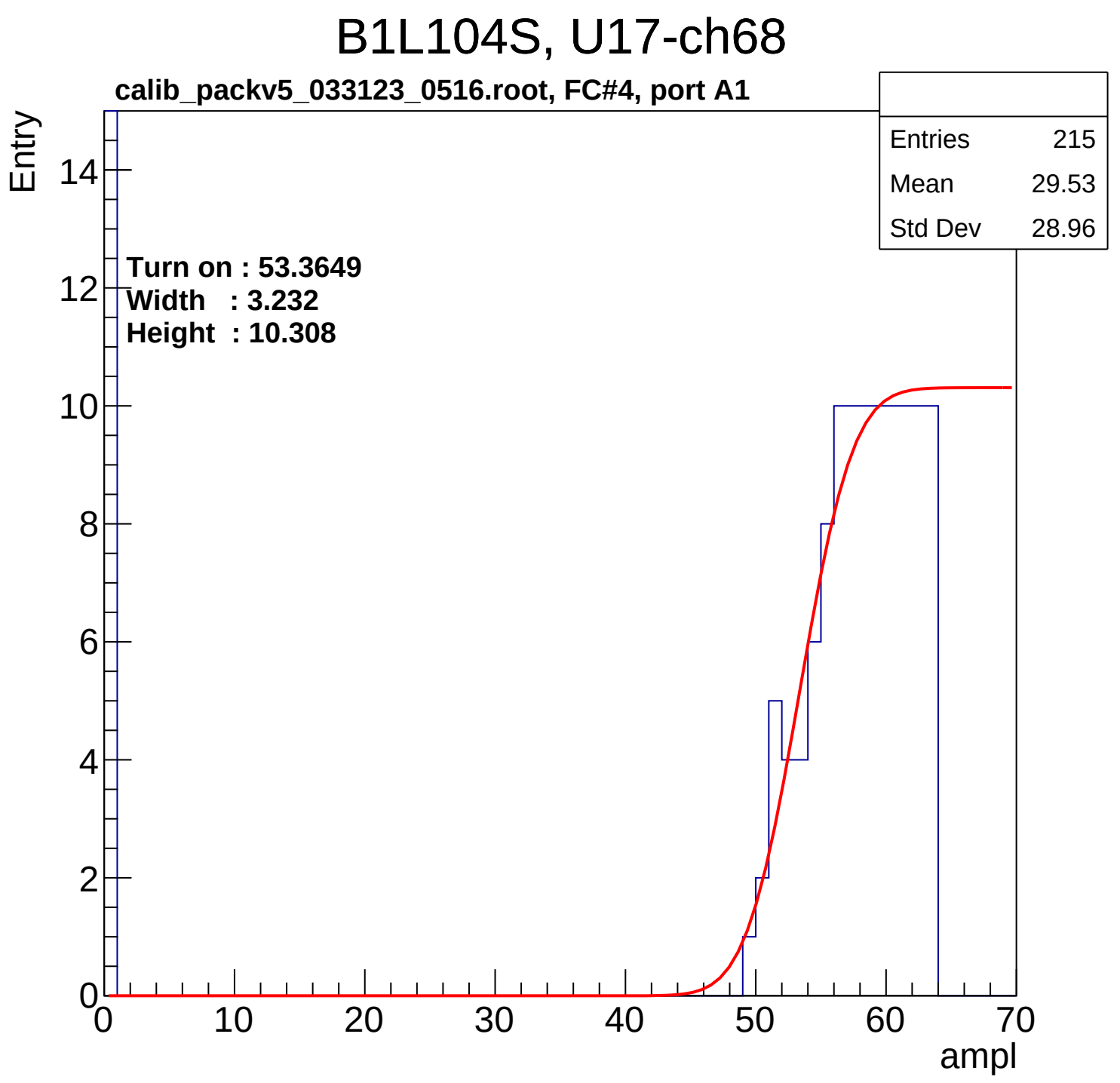
B1L104S, U17-ch68
calib_packv5_033123_0516.root, FC#4, port A1
Entries 215
Mean 29.53
Std Dev 28.96
Turn on : 53.3649
Width : 3.232
Height : 10.308
Entry
ampl
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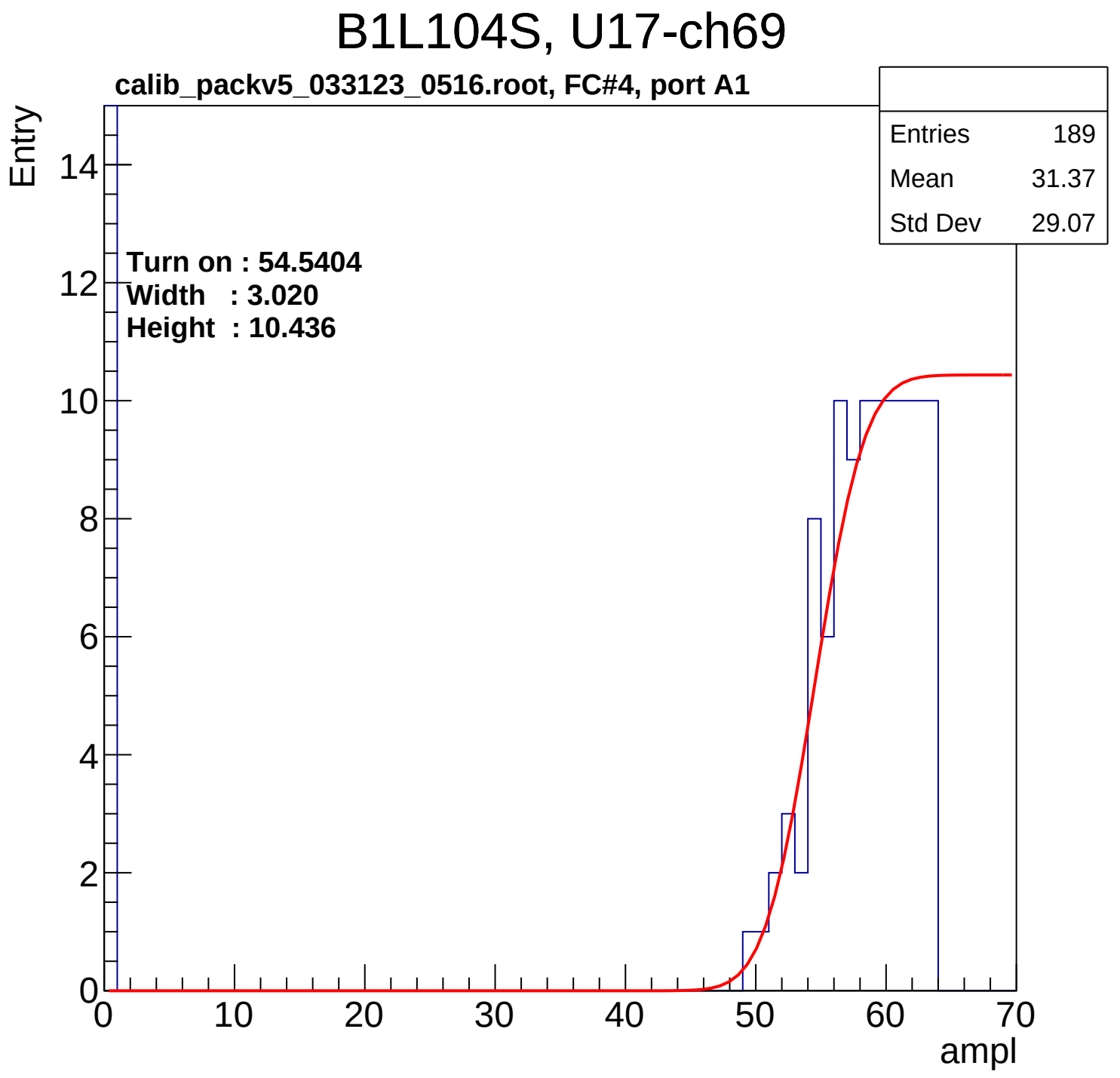
B1L104S, U17-ch69
calib_packv5_033123_0516.root, FC#4, port A1
Entries 189
Mean 31.37
Std Dev 29.07
Turn on : 54.5404
Width : 3.020
Height : 10.436
Entry
ampl
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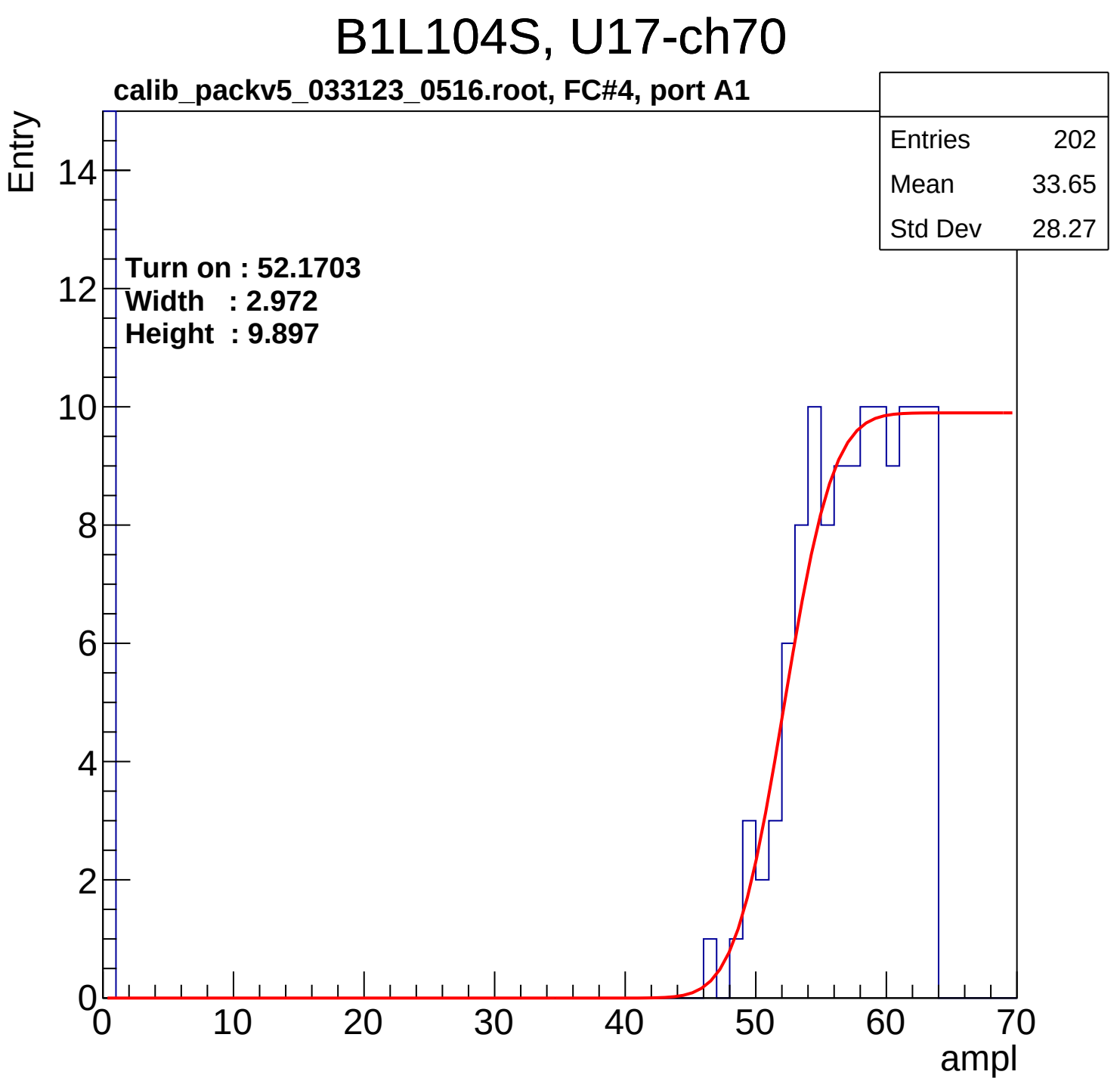
B1L104S, U17-ch70
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 33.65
Std Dev 28.27
Turn on : 52.1703
Width : 2.972
Height : 9.897
Entry
ampl
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2
4
6
8
10
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0
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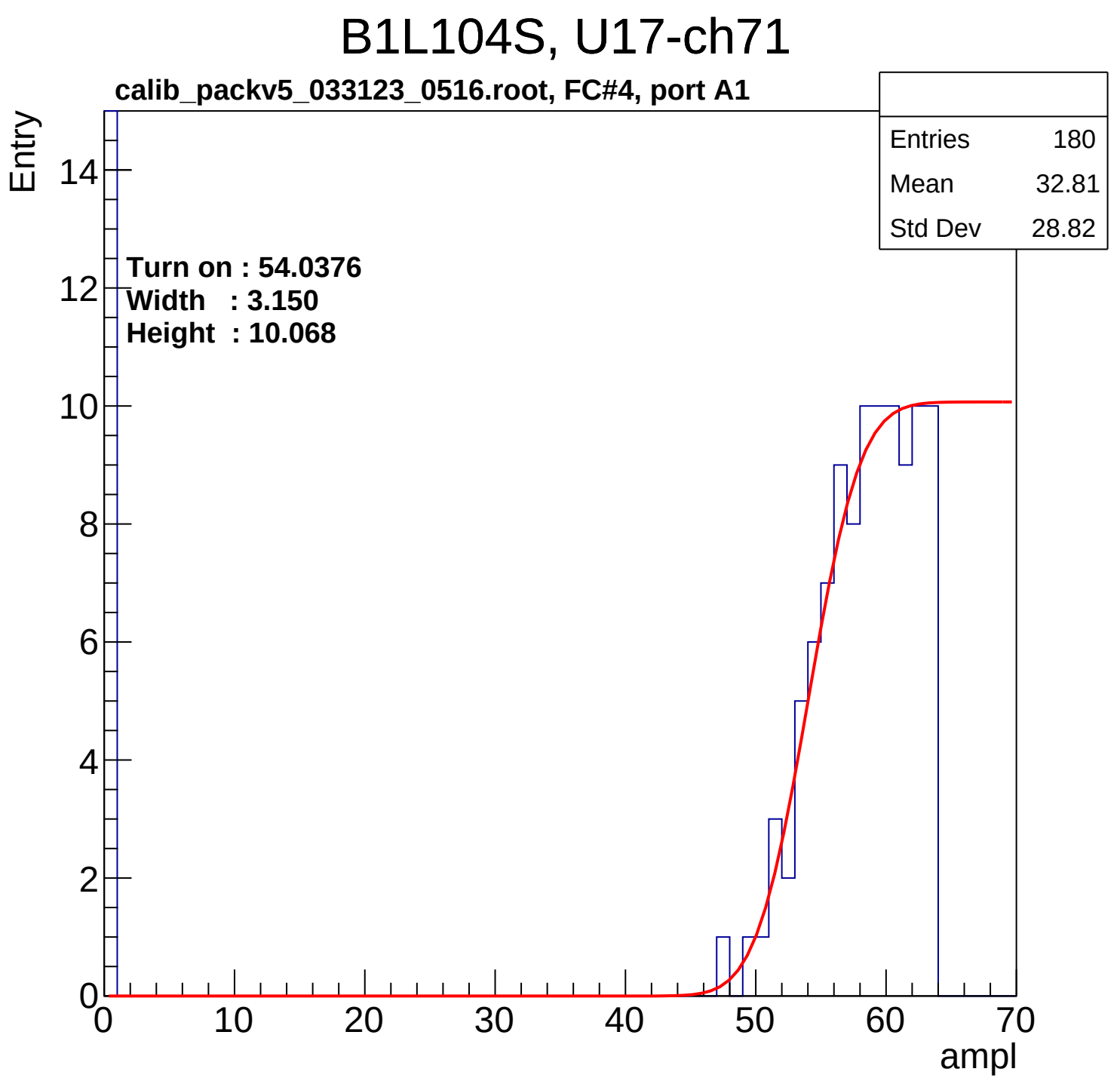
B1L104S, U17-ch71
calib_packv5_033123_0516.root, FC#4, port A1
Entries 180
Mean 32.81
Std Dev 28.82
Turn on : 54.0376
Width : 3.150
Height : 10.068
Entry
ampl
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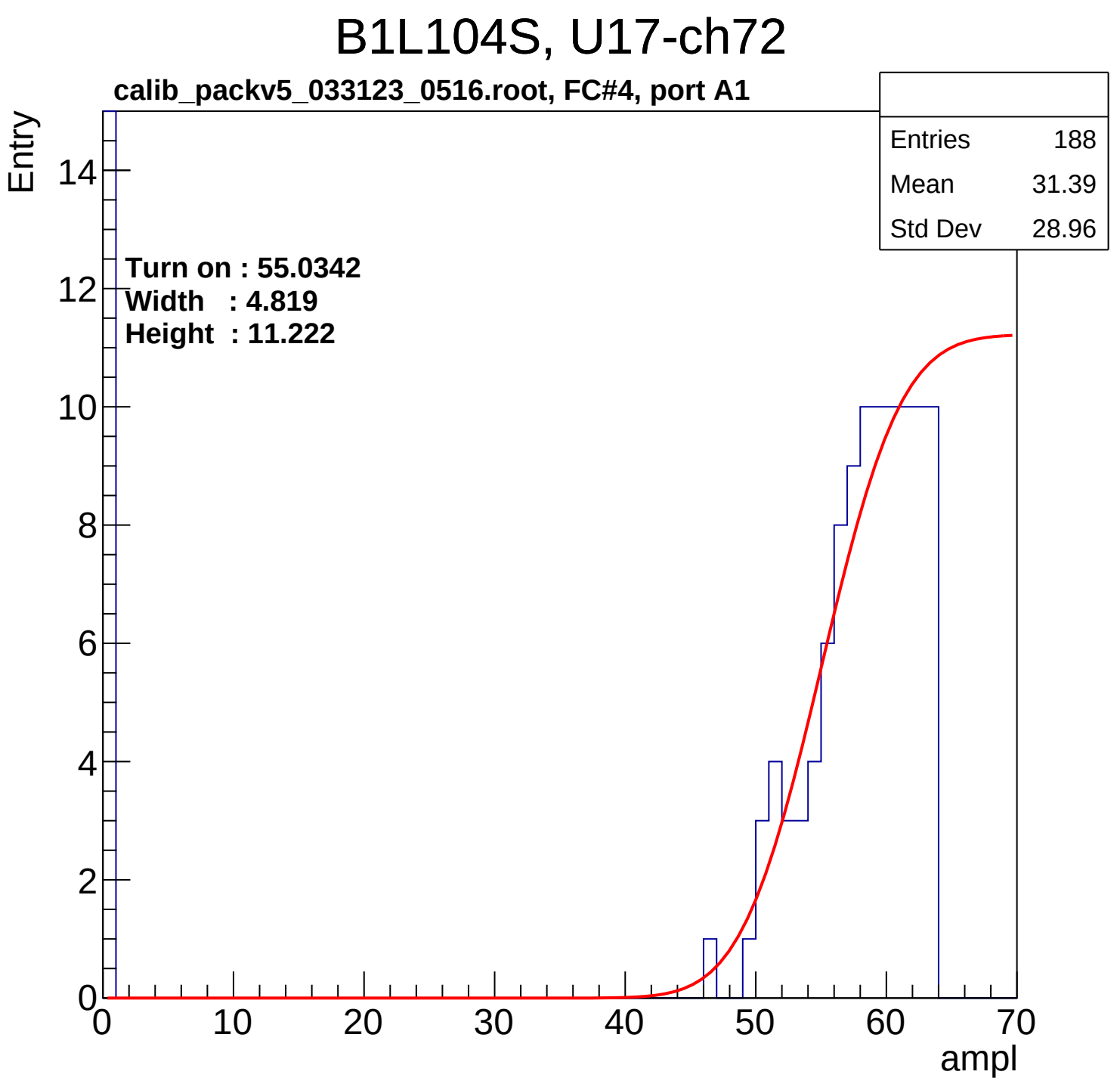
B1L104S, U17-ch72
calib_packv5_033123_0516.root, FC#4, port A1
Entries 188
Mean 31.39
Std Dev 28.96
Turn on : 55.0342
Width : 4.819
Height : 11.222
Entry
ampl
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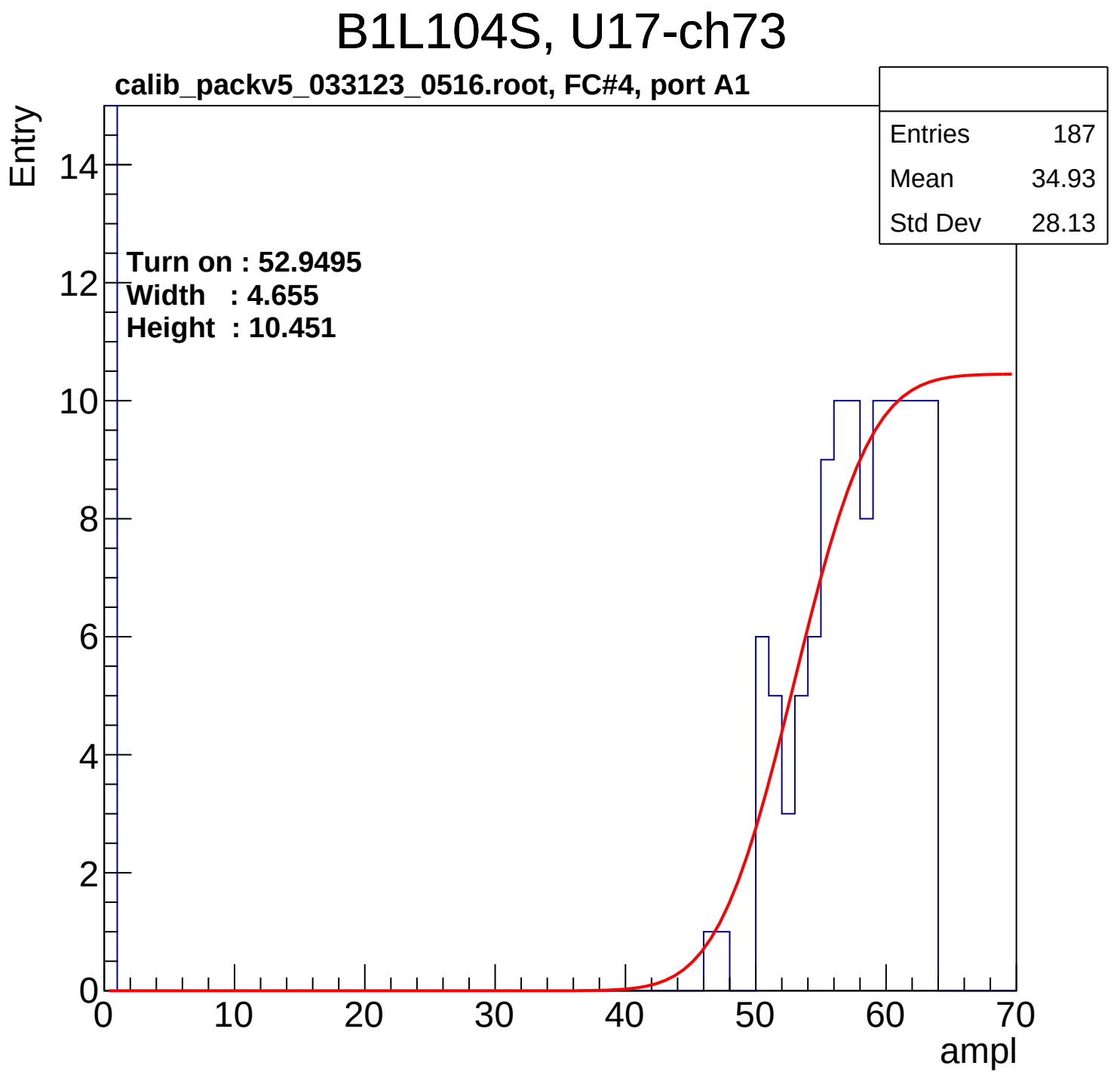
B1L104S, U17-ch73
calib_packv5_033123_0516.root, FC#4, port A1
Entries 187
Mean 34.93
Std Dev 28.13
Turn on : 52.9495
Width : 4.655
Height : 10.451
Entry
ampl
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8
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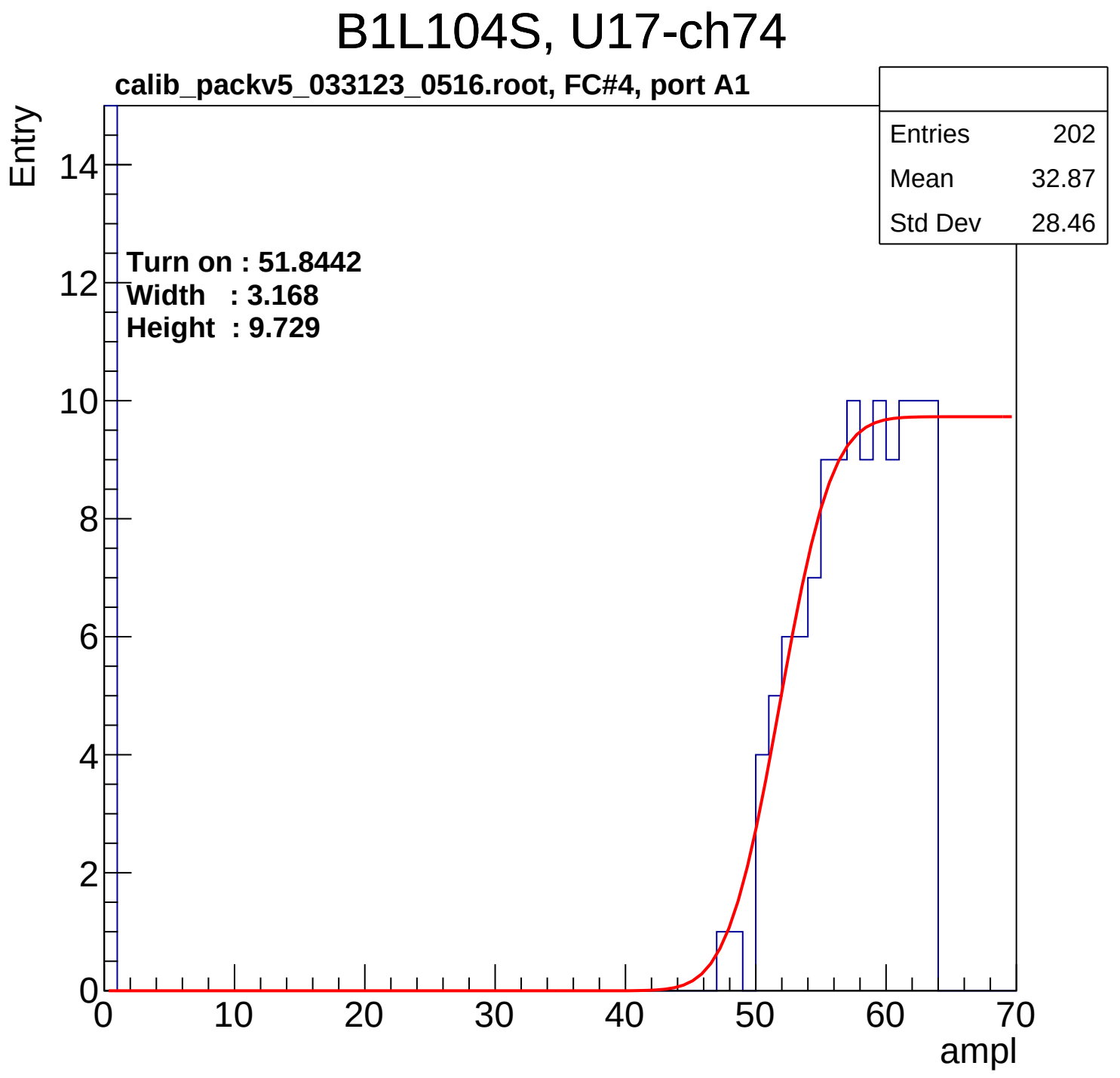
B1L104S, U17-ch74
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 32.87
Std Dev 28.46
Turn on : 51.8442
Width : 3.168
Height : 9.729
Entry
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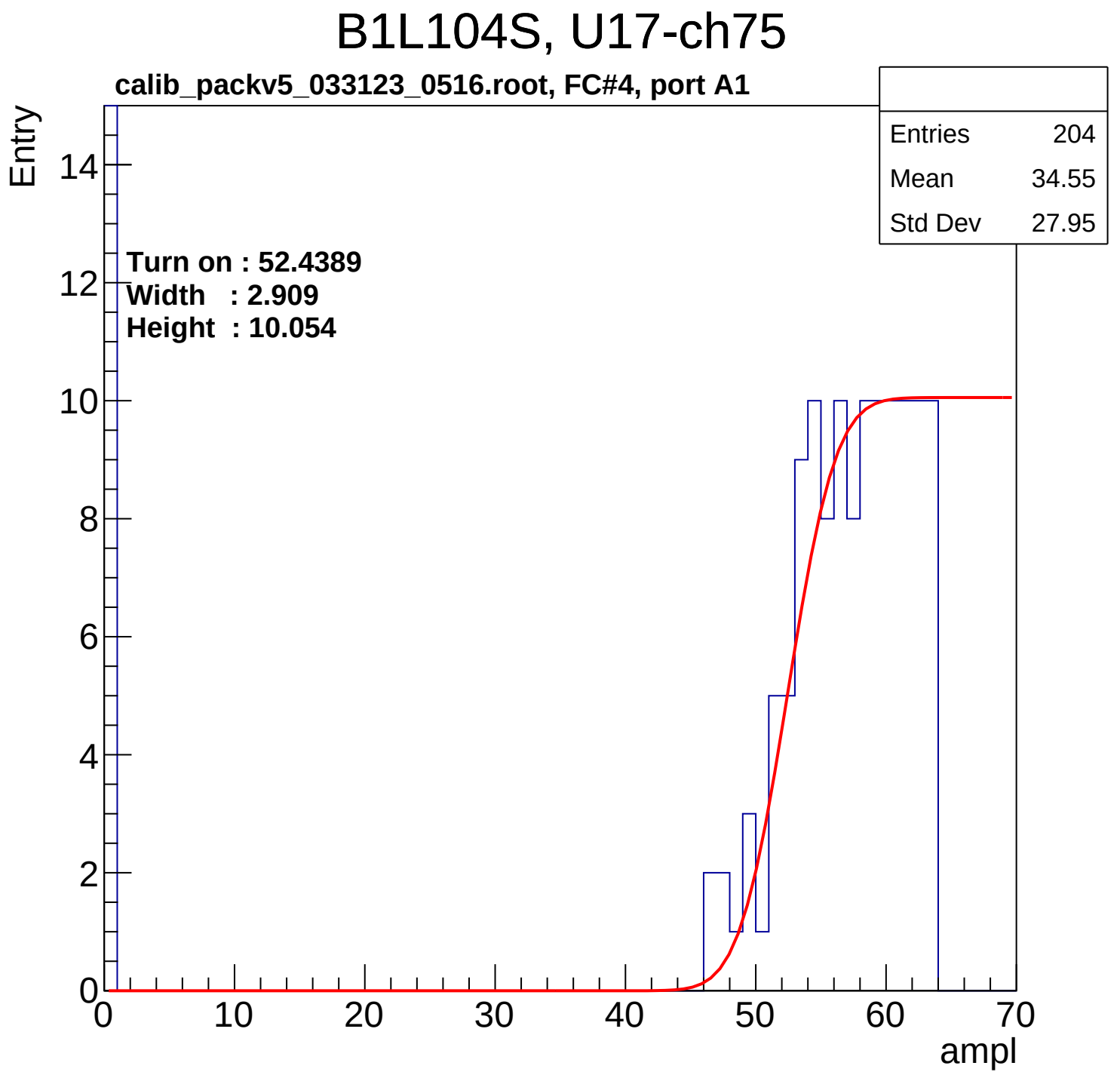
B1L104S, U17-ch75
calib_packv5_033123_0516.root, FC#4, port A1
Entries 204
Mean 34.55
Std Dev 27.95
Turn on : 52.4389
Width : 2.909
Height : 10.054
Entry
ampl
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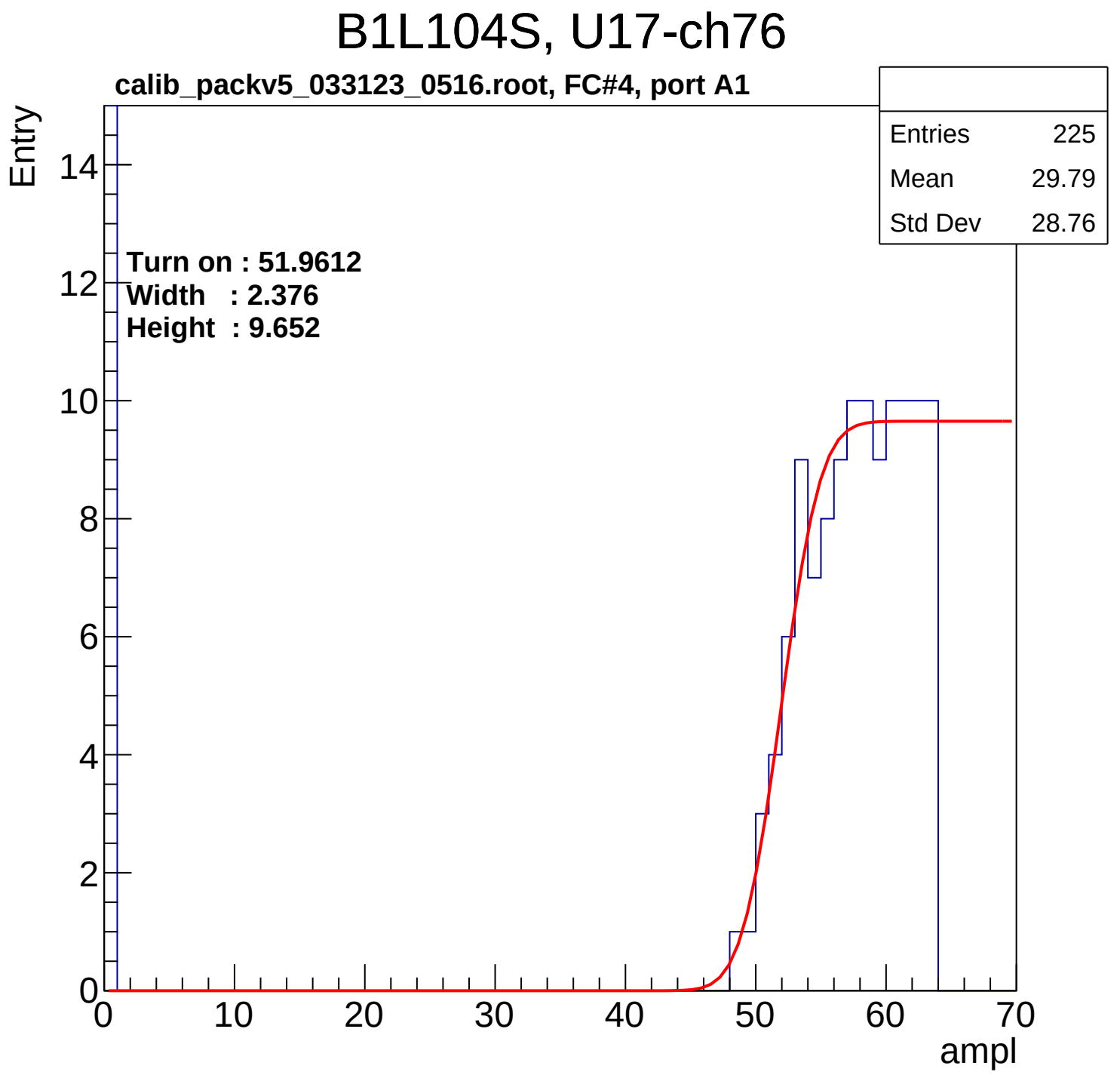
B1L104S, U17-ch76
calib_packv5_033123_0516.root, FC#4, port A1
Entries 225
Mean 29.79
Std Dev 28.76
Turn on : 51.9612
Width : 2.376
Height : 9.652
Entry
ampl
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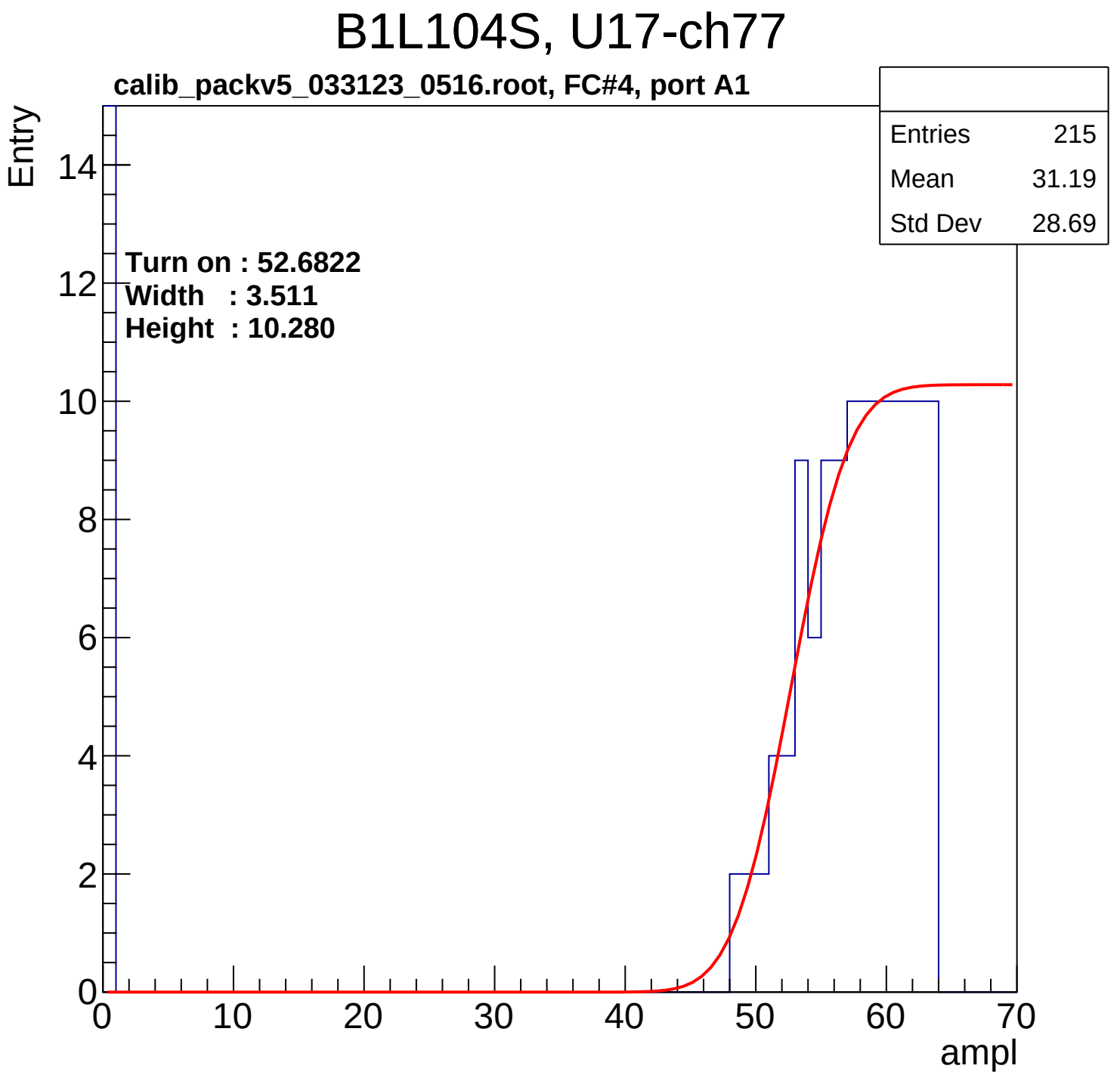
B1L104S, U17-ch77
calib_packv5_033123_0516.root, FC#4, port A1
Entries 215
Mean 31.19
Std Dev 28.69
Turn on : 52.6822
Width : 3.511
Height : 10.280
Entry
ampl
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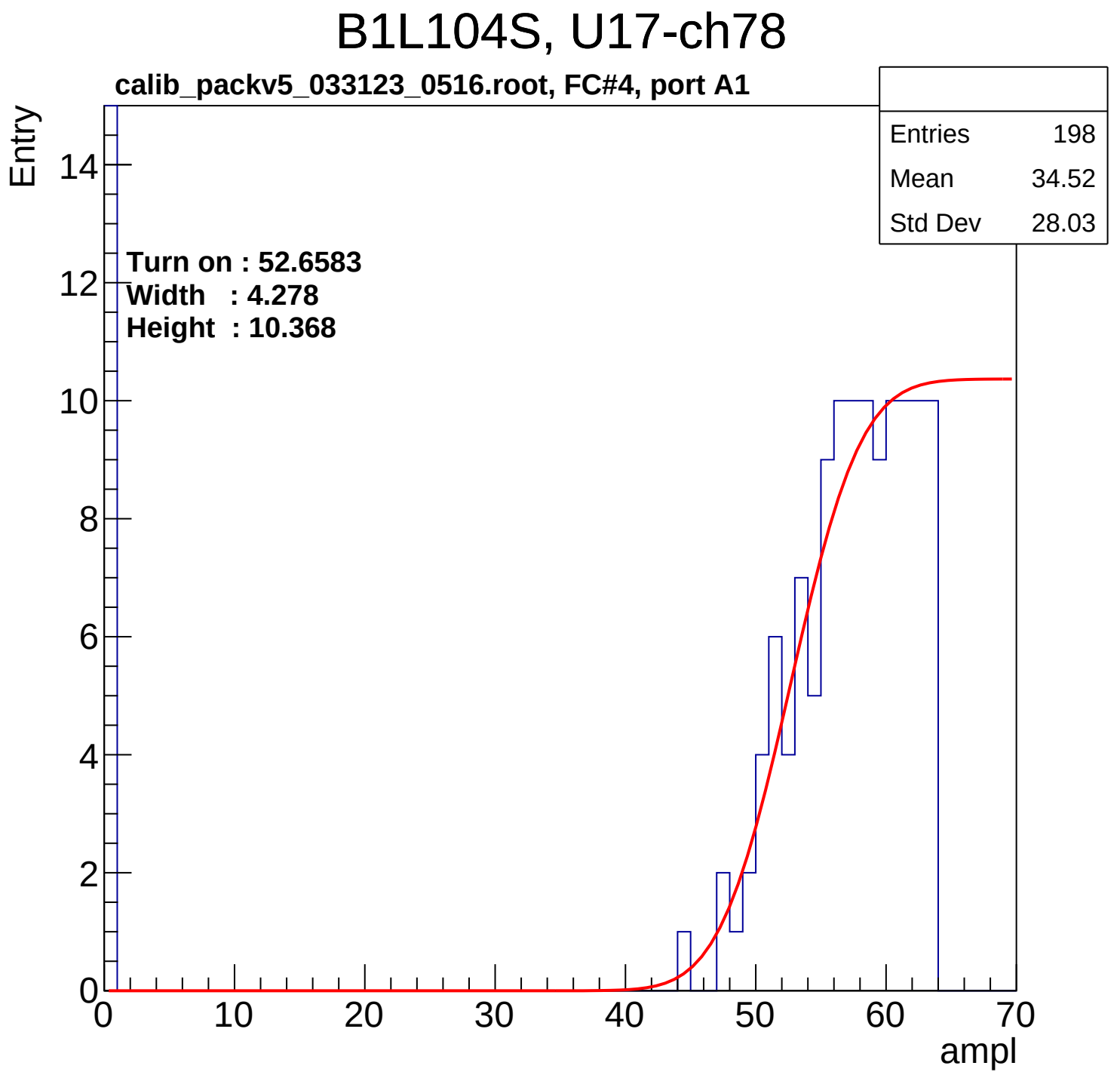
B1L104S, U17-ch78
calib_packv5_033123_0516.root, FC#4, port A1
Entries 198
Mean 34.52
Std Dev 28.03
Turn on : 52.6583
Width : 4.278
Height : 10.368
Entry
ampl
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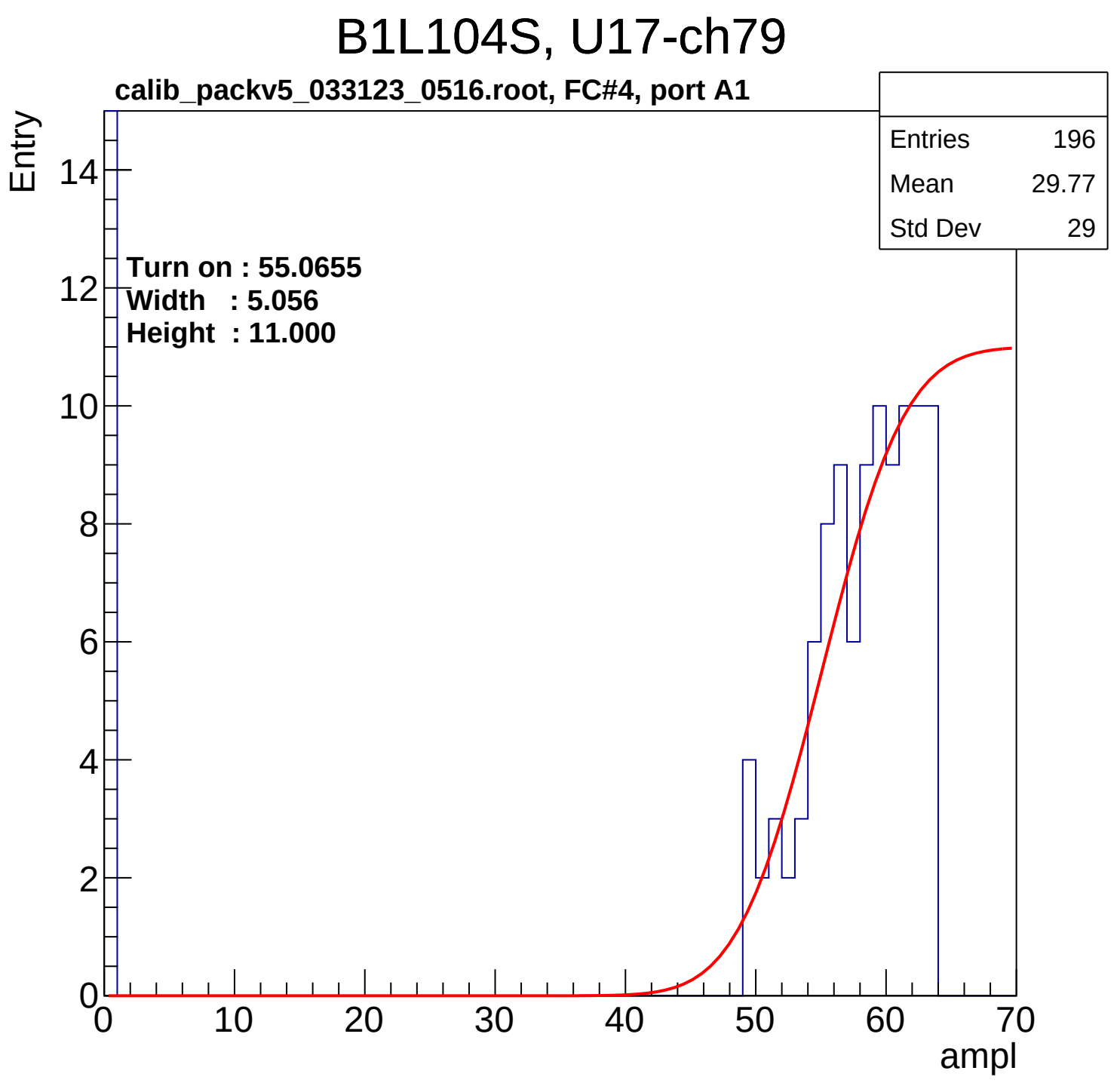
B1L104S, U17-ch79
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 29.77
Std Dev 29
Turn on : 55.0655
Width : 5.056
Height : 11.000
Entry
ampl
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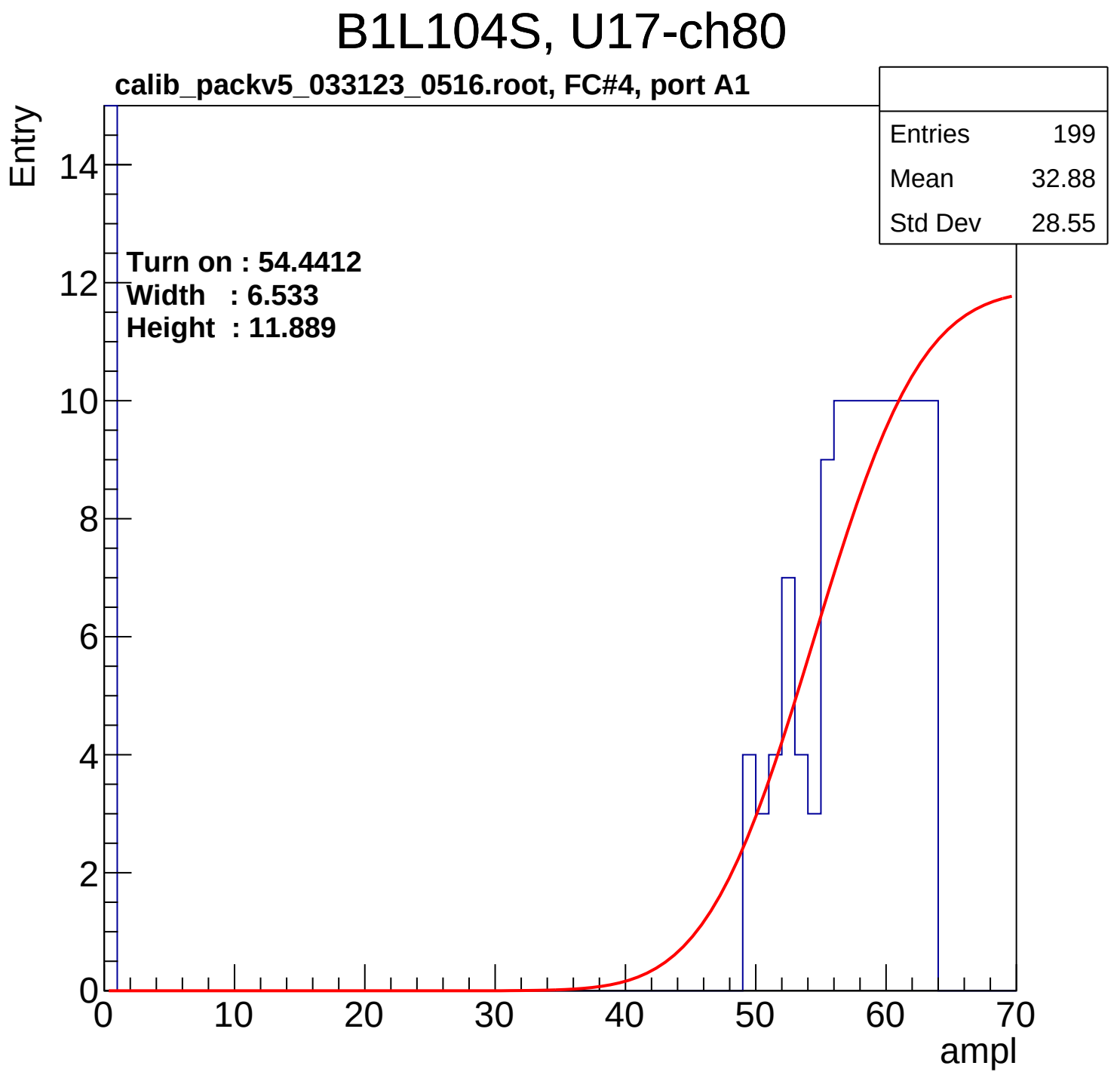
B1L104S, U17-ch80
calib_packv5_033123_0516.root, FC#4, port A1
Entries 199
Mean 32.88
Std Dev 28.55
Turn on : 54.4412
Width : 6.533
Height : 11.889
Entry
ampl
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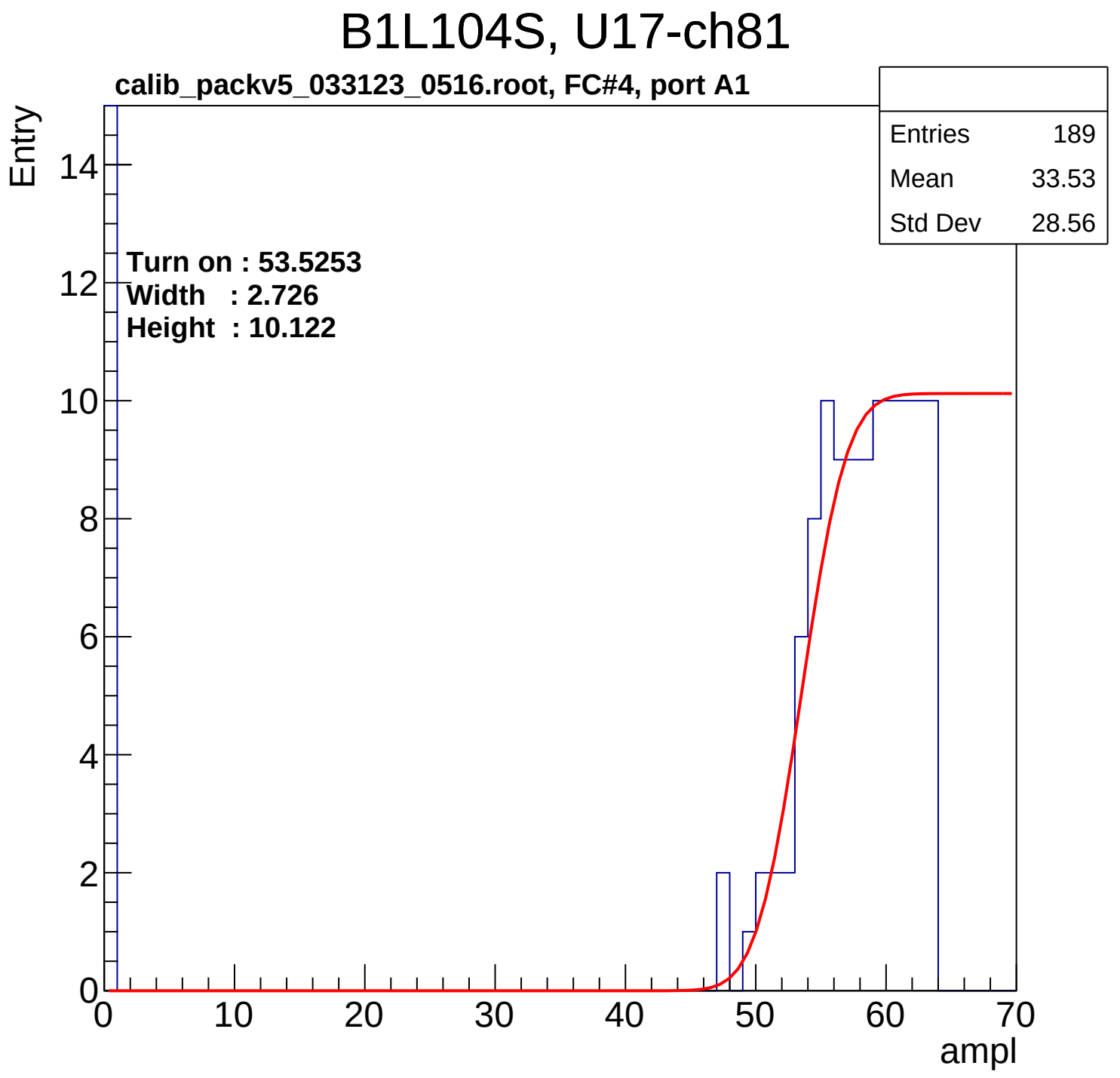
B1L104S, U17-ch81
calib_packv5_033123_0516.root, FC#4, port A1
Entries 189
Mean 33.53
Std Dev 28.56
Turn on : 53.5253
Width : 2.726
Height : 10.122
Entry
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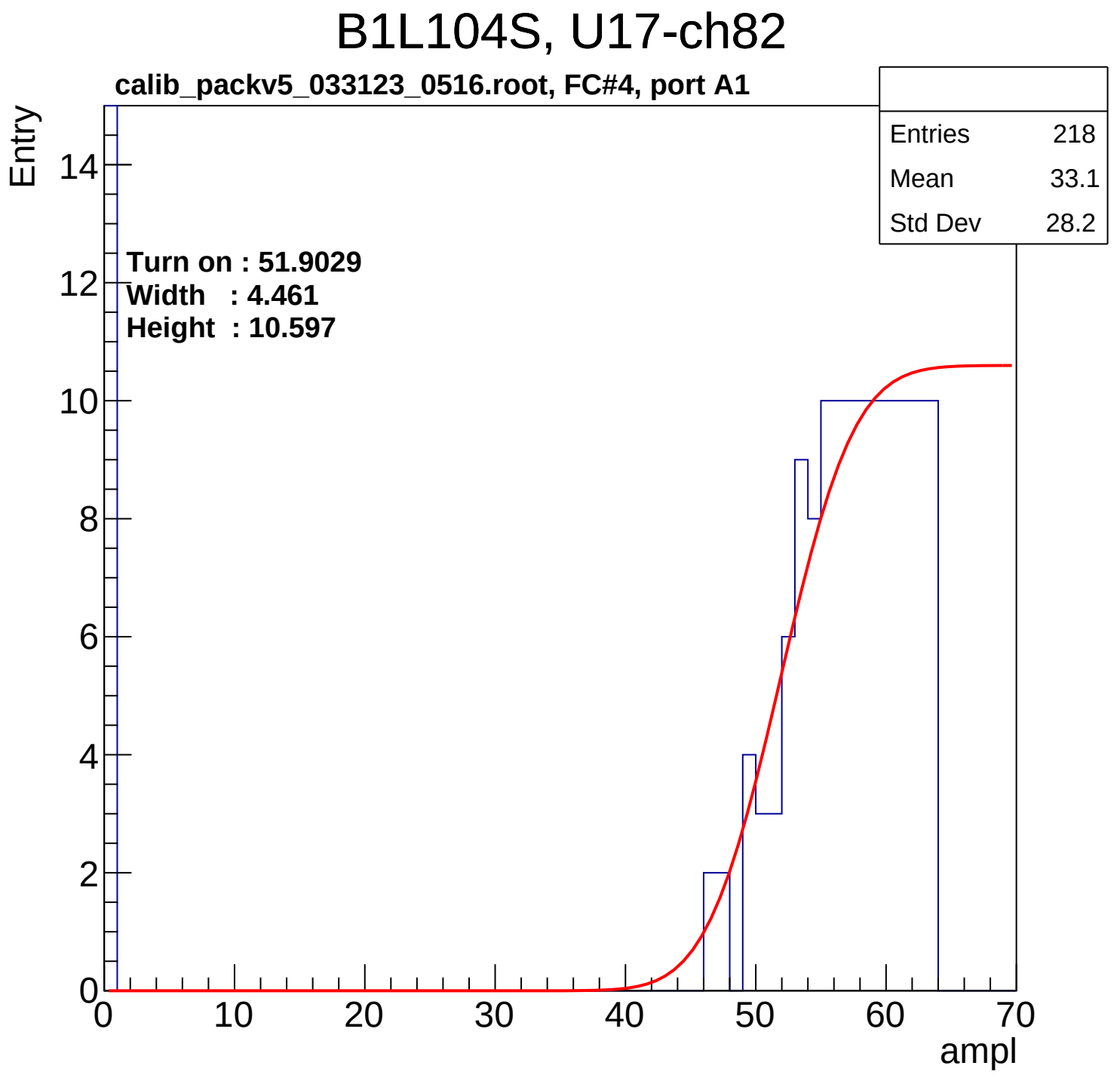
B1L104S, U17-ch82
calib_packv5_033123_0516.root, FC#4, port A1
Entries 218
Mean 33.1
Std Dev 28.2
Turn on : 51.9029
Width : 4.461
Height : 10.597
Entry
ampl
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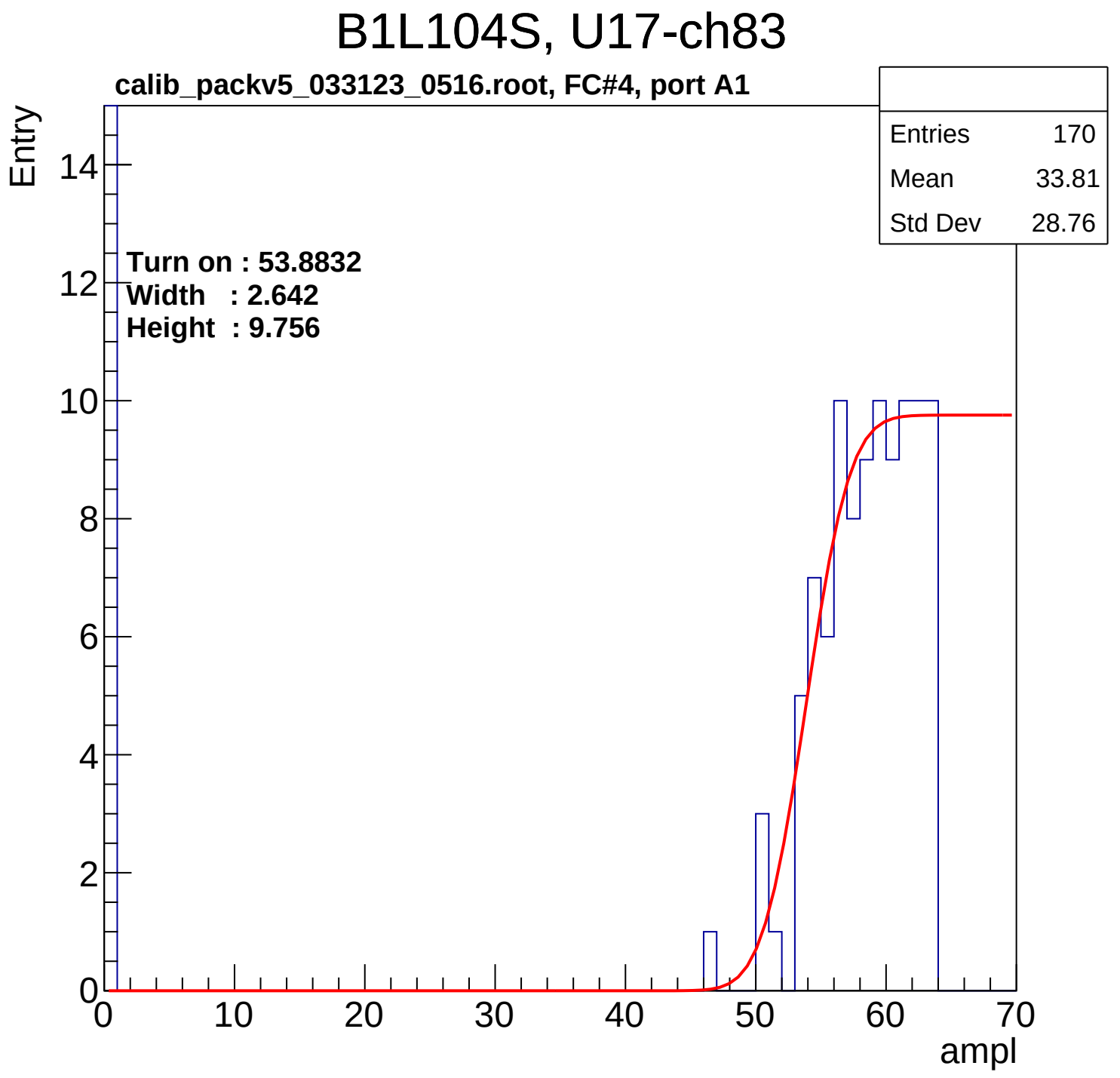
B1L104S, U17-ch83
calib_packv5_033123_0516.root, FC#4, port A1
Entries 170
Mean 33.81
Std Dev 28.76
Turn on : 53.8832
Width : 2.642
Height : 9.756
Entry
ampl
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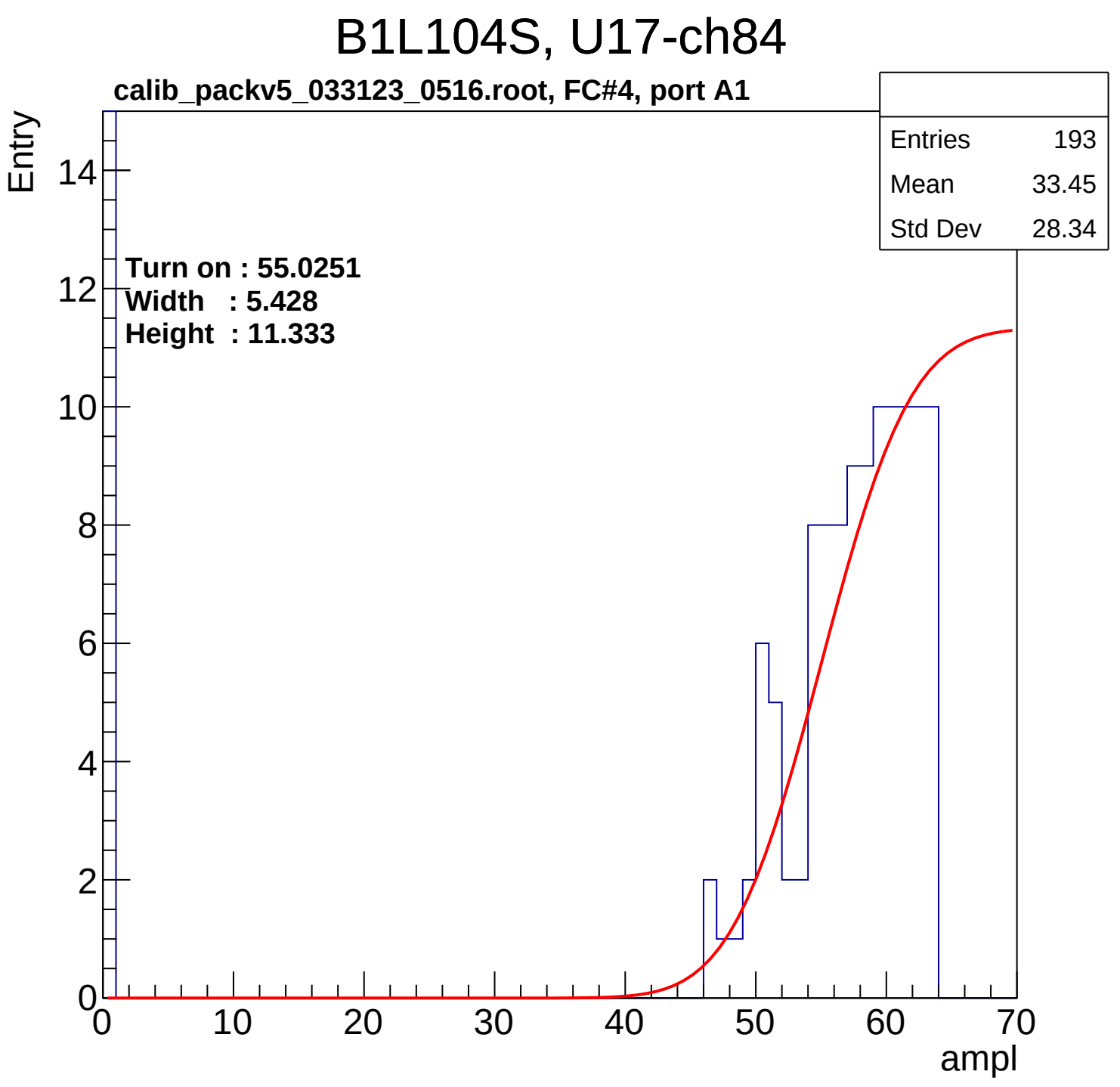
B1L104S, U17-ch84
calib_packv5_033123_0516.root, FC#4, port A1
Entries 193
Mean 33.45
Std Dev 28.34
Turn on : 55.0251
Width : 5.428
Height : 11.333
Entry
ampl
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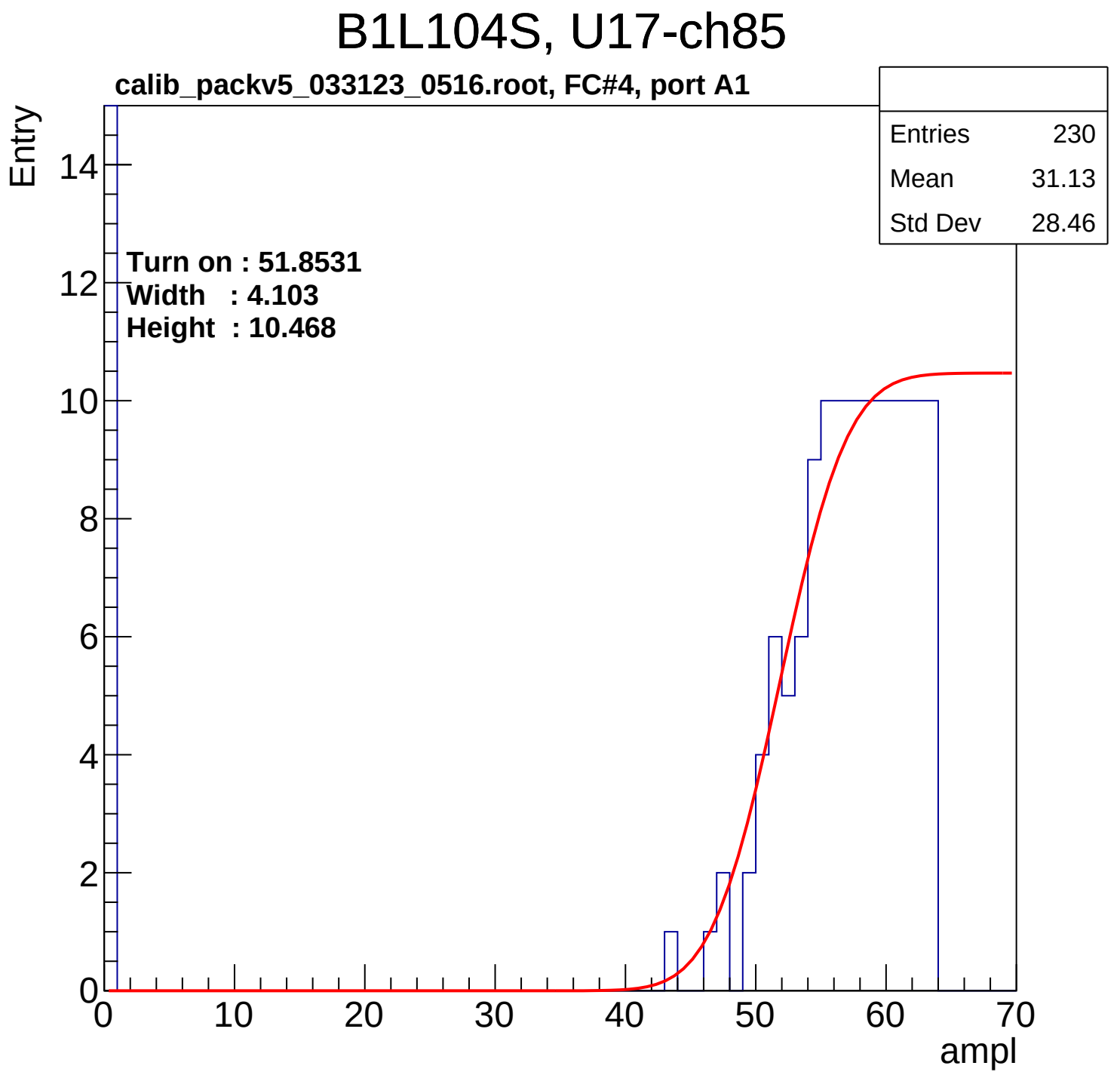
B1L104S, U17-ch85
calib_packv5_033123_0516.root, FC#4, port A1
Entries 230
Mean 31.13
Std Dev 28.46
Turn on : 51.8531
Width : 4.103
Height : 10.468
Entry
ampl
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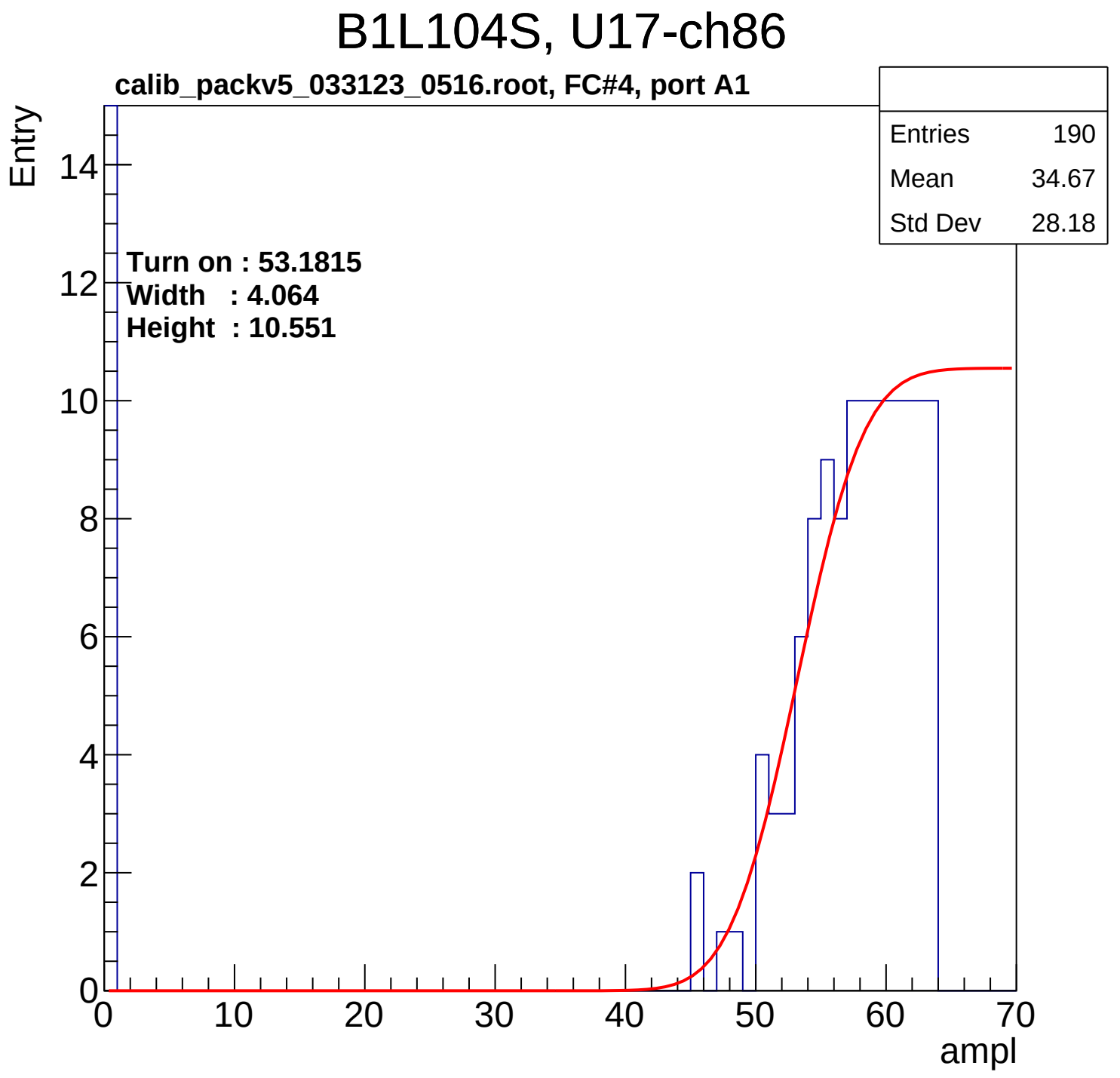
B1L104S, U17-ch86
calib_packv5_033123_0516.root, FC#4, port A1
Entries 190
Mean 34.67
Std Dev 28.18
Turn on : 53.1815
Width : 4.064
Height : 10.551
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ampl
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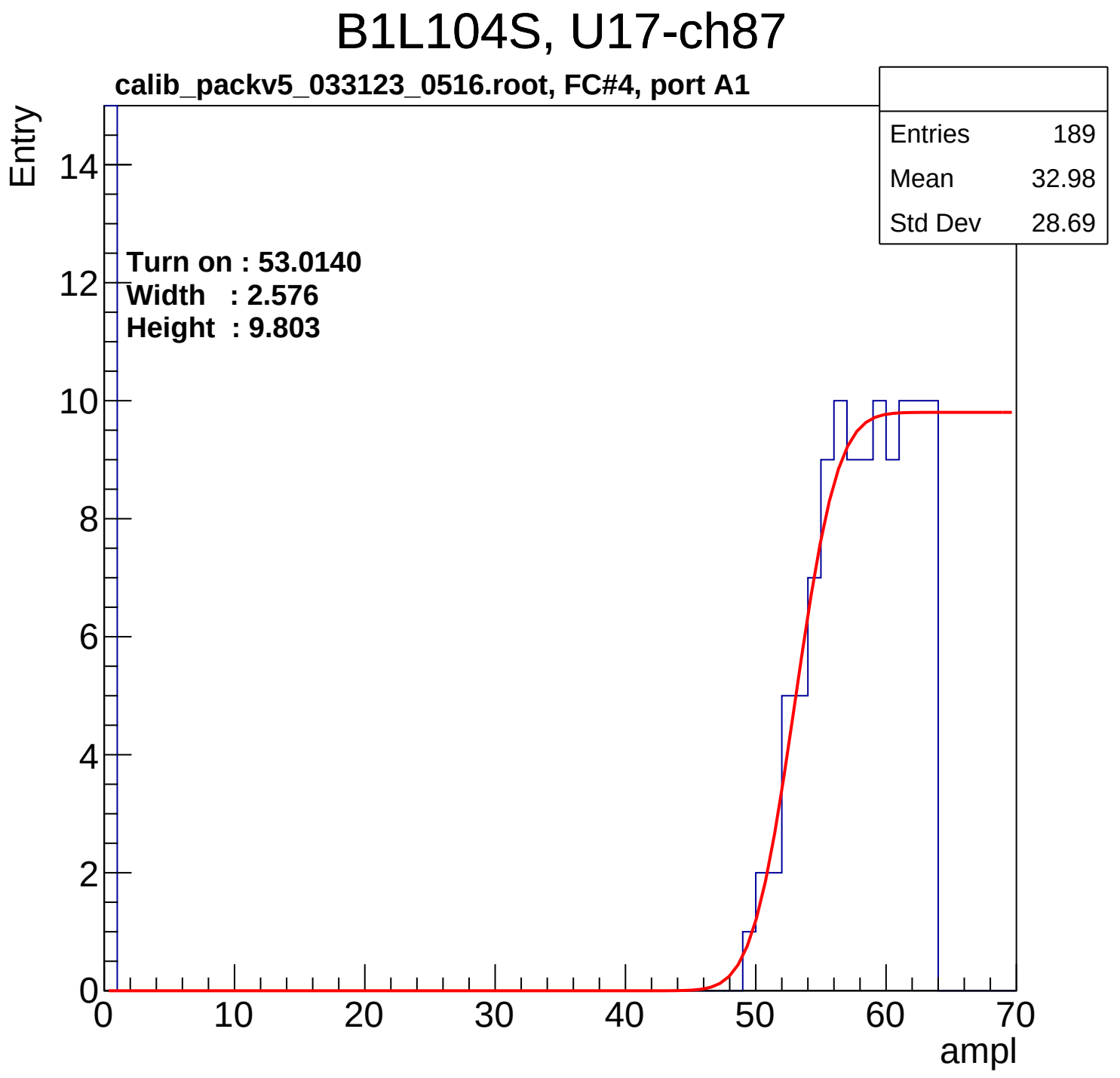
B1L104S, U17-ch87
calib_packv5_033123_0516.root, FC#4, port A1
Entries 189
Mean 32.98
Std Dev 28.69
Turn on : 53.0140
Width : 2.576
Height : 9.803
Entry
ampl
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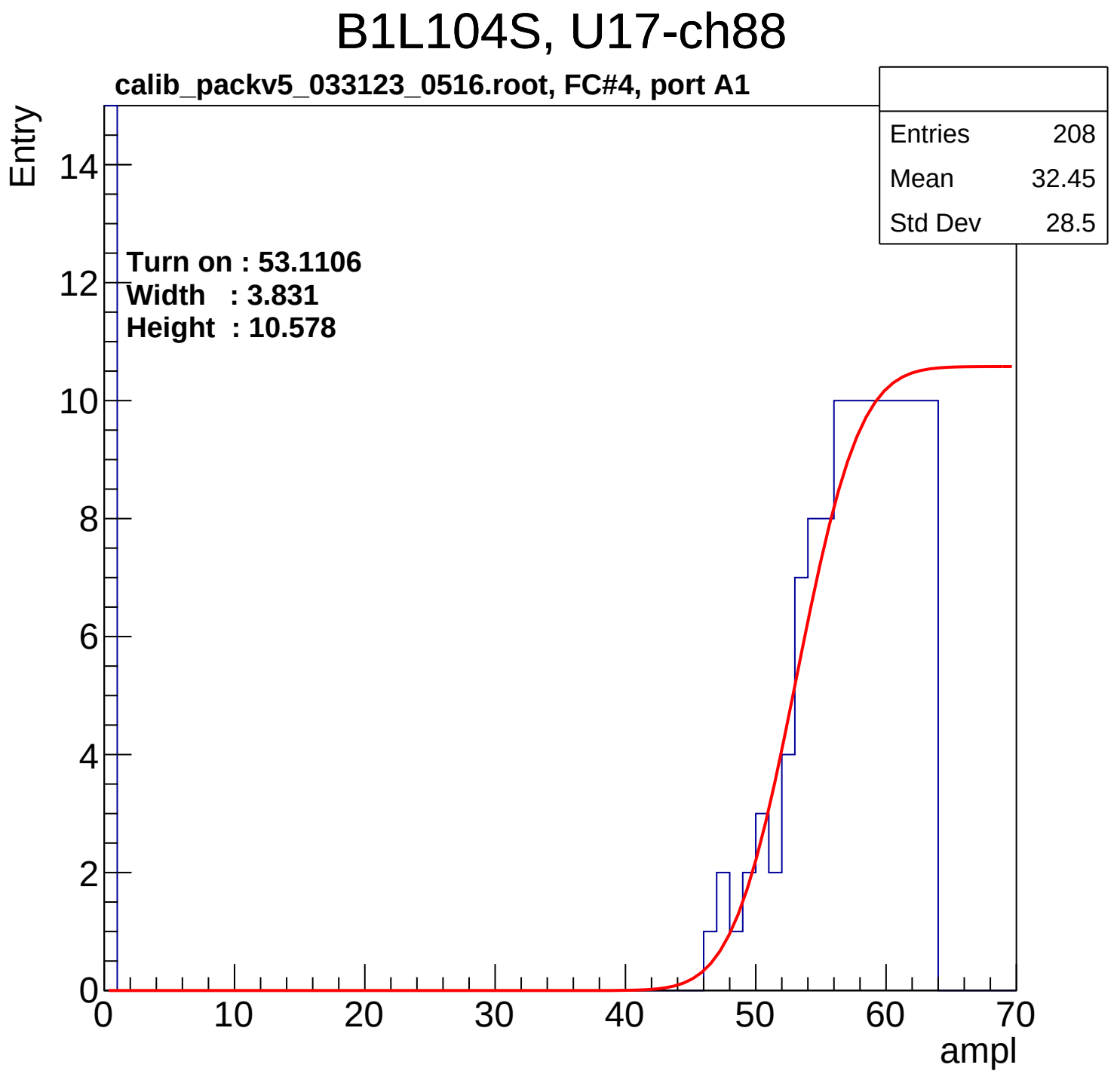
B1L104S, U17-ch88
calib_packv5_033123_0516.root, FC#4, port A1
Entries 208
Mean 32.45
Std Dev 28.5
Turn on : 53.1106
Width : 3.831
Height : 10.578
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ampl
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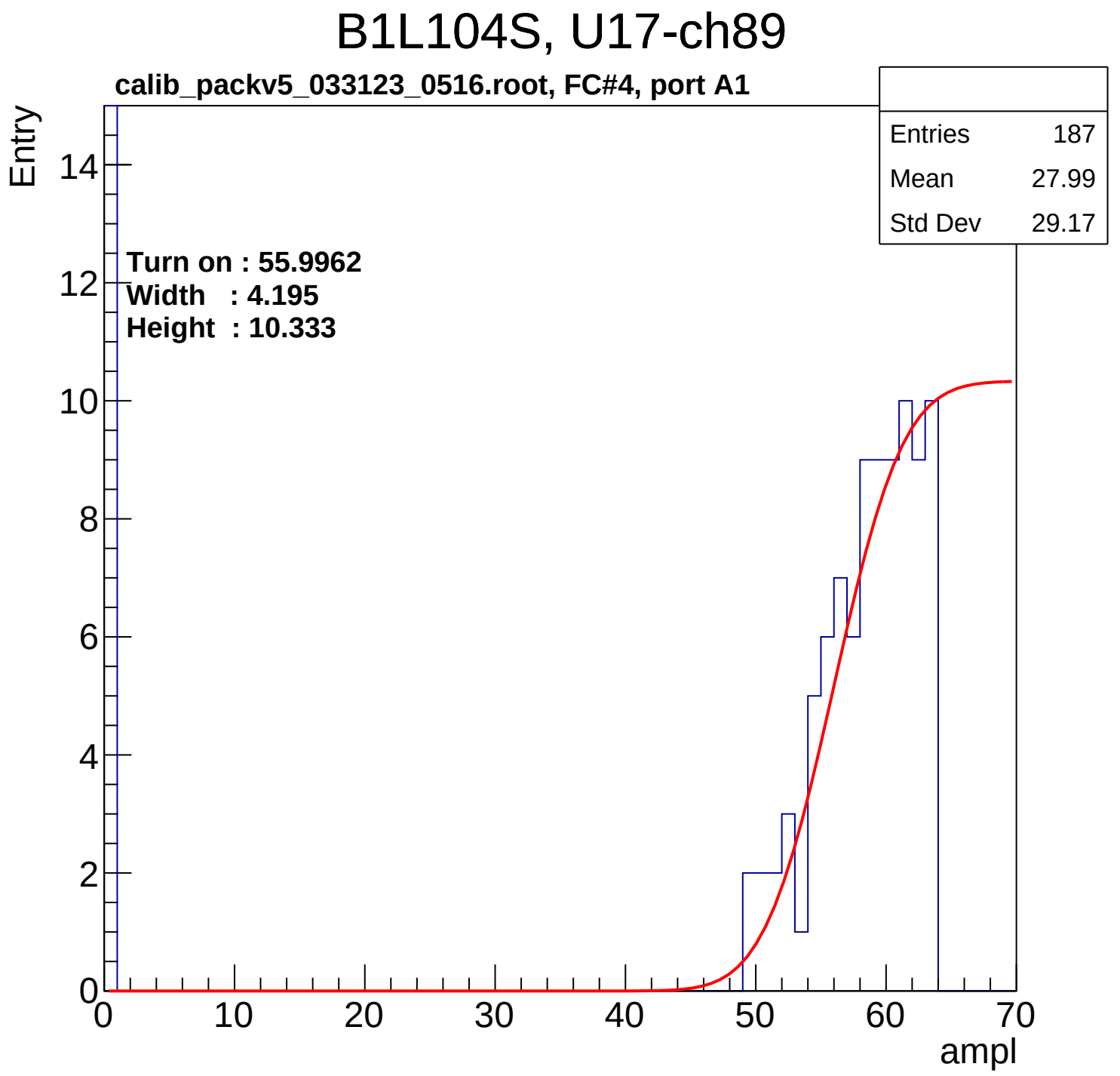
B1L104S, U17-ch89
calib_packv5_033123_0516.root, FC#4, port A1
Entries 187
Mean 27.99
Std Dev 29.17
Turn on : 55.9962
Width : 4.195
Height : 10.333
Entry
ampl
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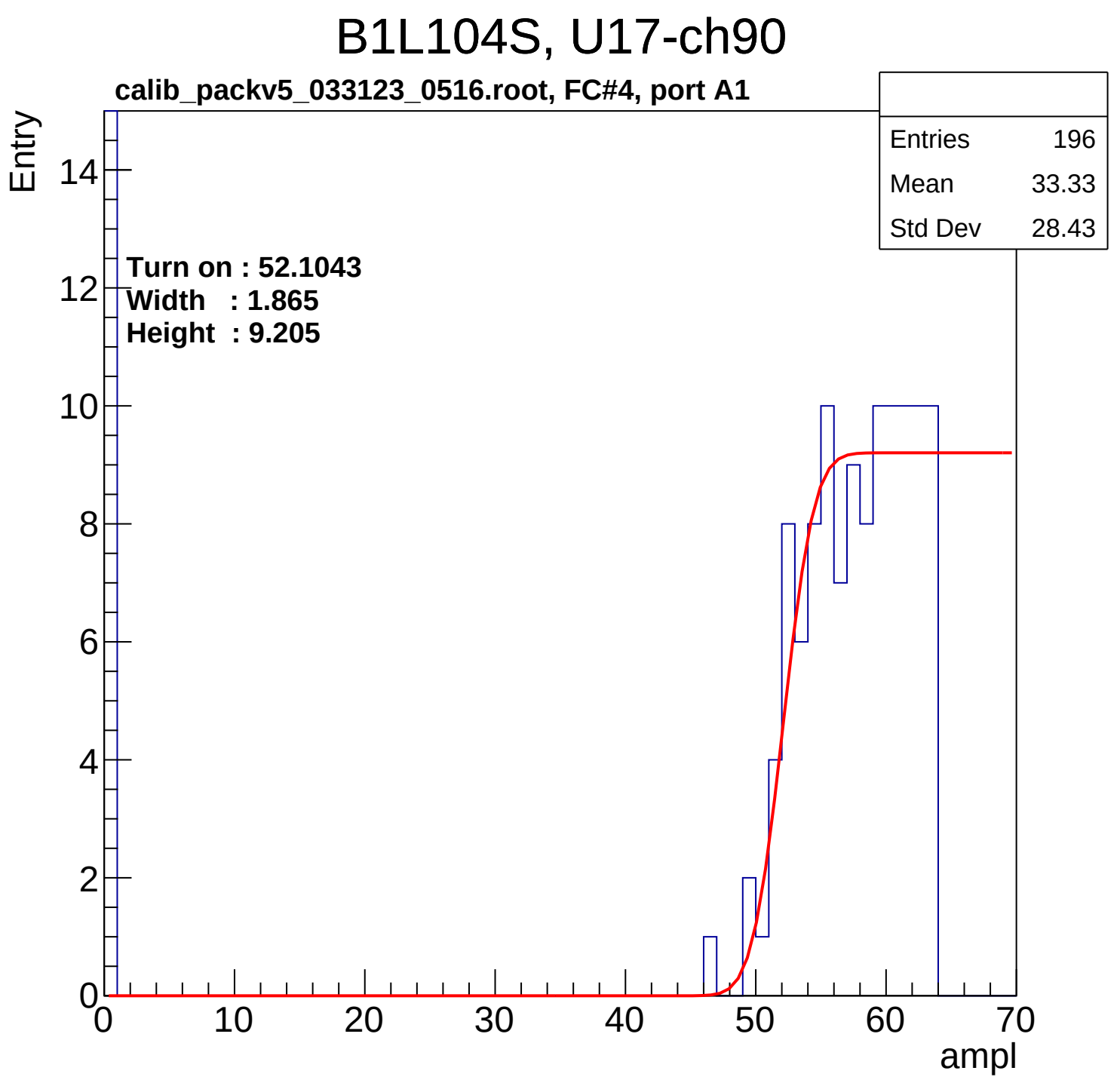
B1L104S, U17-ch90
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 33.33
Std Dev 28.43
Turn on : 52.1043
Width : 1.865
Height : 9.205
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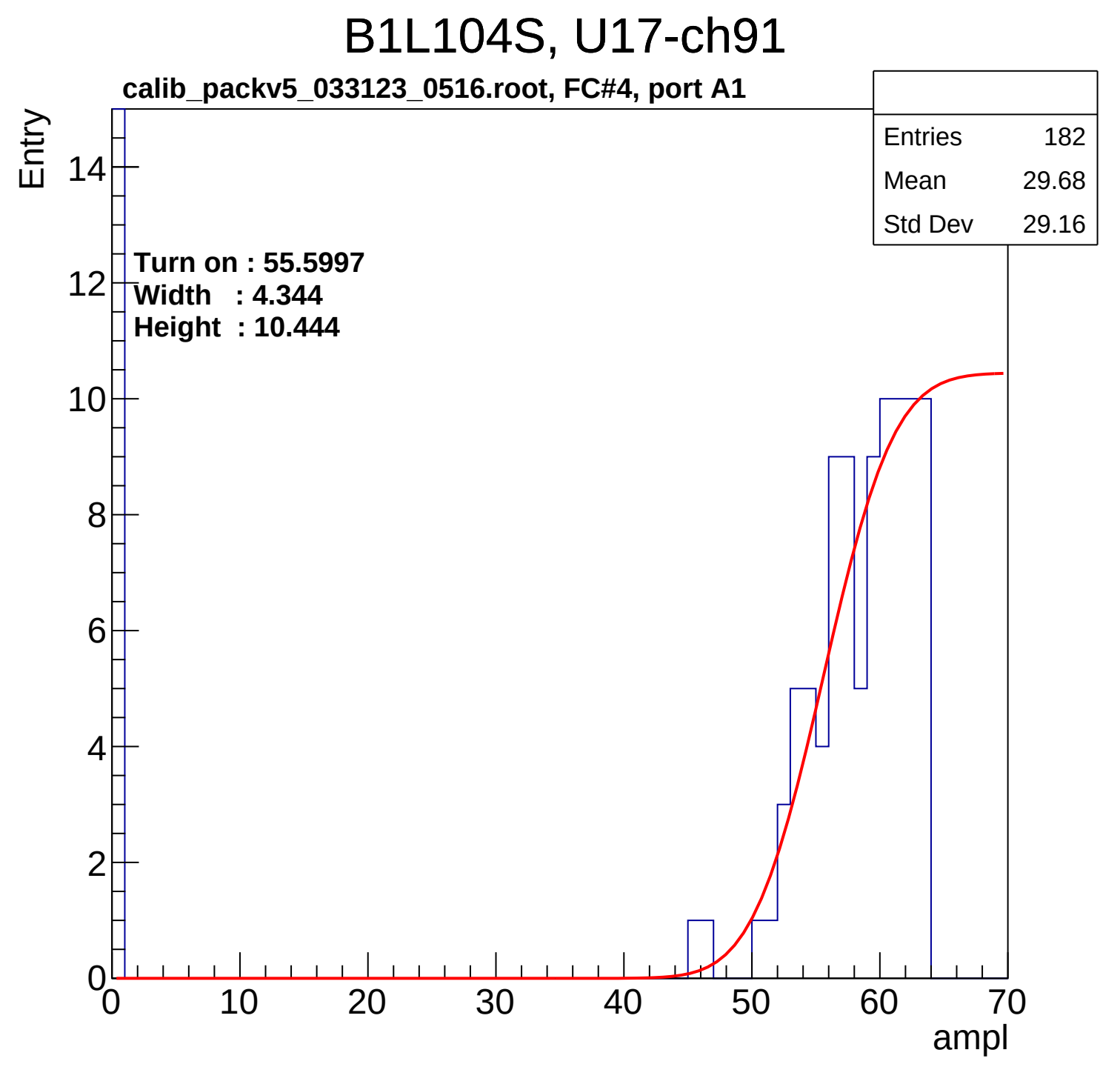
B1L104S, U17-ch91
calib_packv5_033123_0516.root, FC#4, port A1
Entries 182
Mean 29.68
Std Dev 29.16
Turn on : 55.5997
Width : 4.344
Height : 10.444
Entry
ampl
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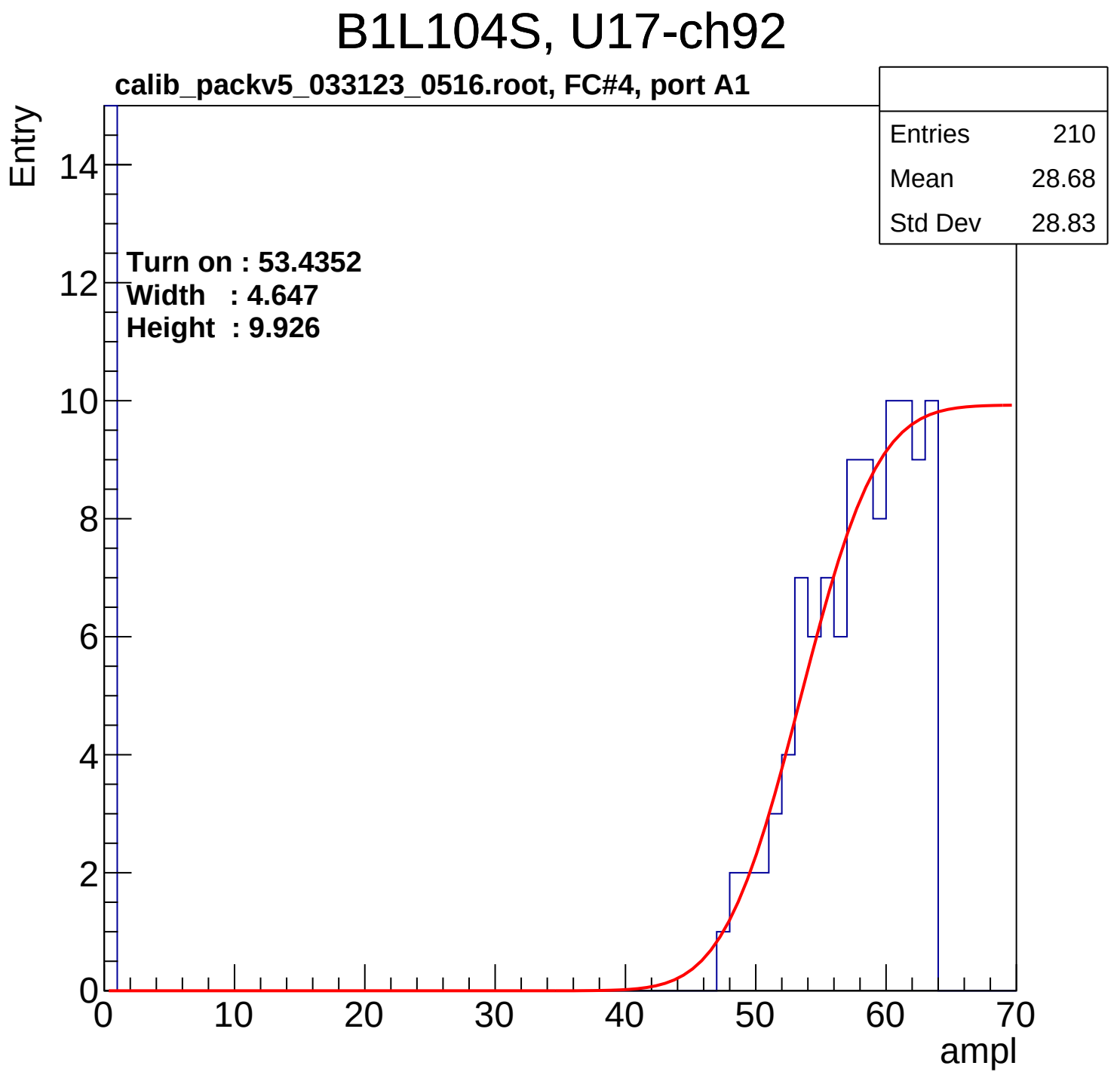
B1L104S, U17-ch92
calib_packv5_033123_0516.root, FC#4, port A1
Entries 210
Mean 28.68
Std Dev 28.83
Turn on : 53.4352
Width : 4.647
Height : 9.926
Entry
ampl
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2
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0
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60
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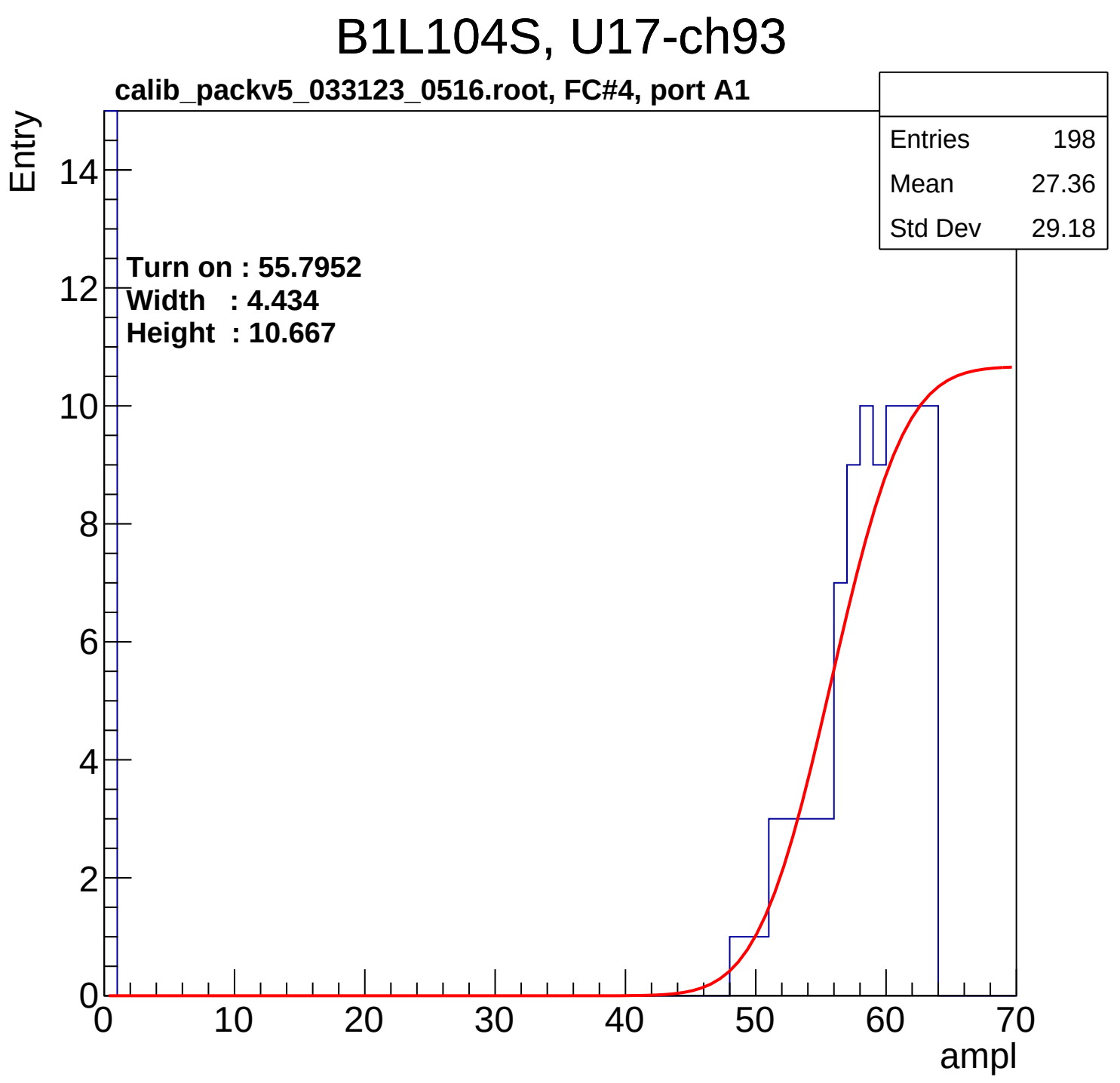
B1L104S, U17-ch93
calib_packv5_033123_0516.root, FC#4, port A1
Entries 198
Mean 27.36
Std Dev 29.18
Turn on : 55.7952
Width : 4.434
Height : 10.667
Entry
ampl
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2
4
6
8
10
12
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0
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20
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40
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60
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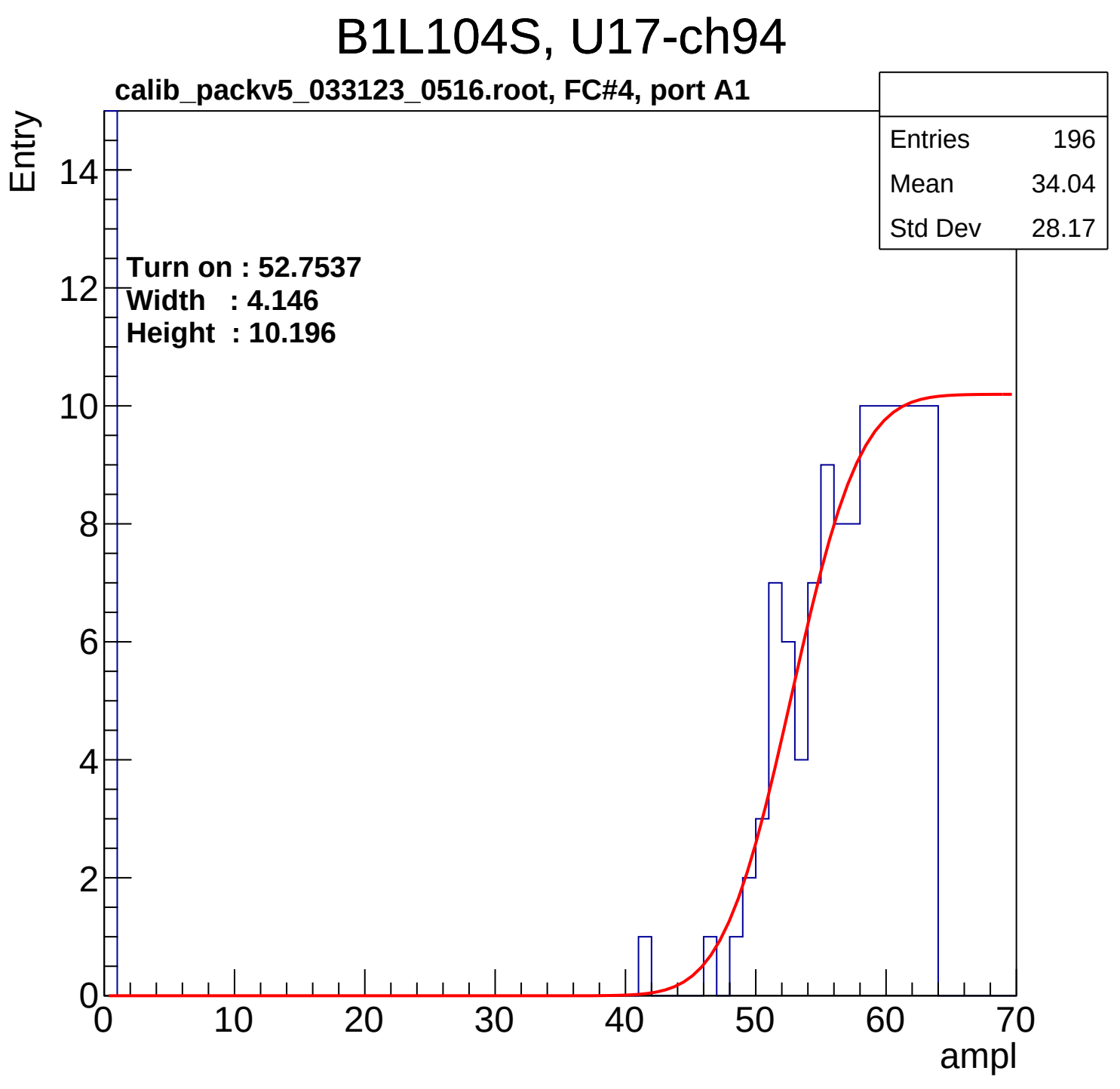
B1L104S, U17-ch94
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 34.04
Std Dev 28.17
Turn on : 52.7537
Width : 4.146
Height : 10.196
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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60
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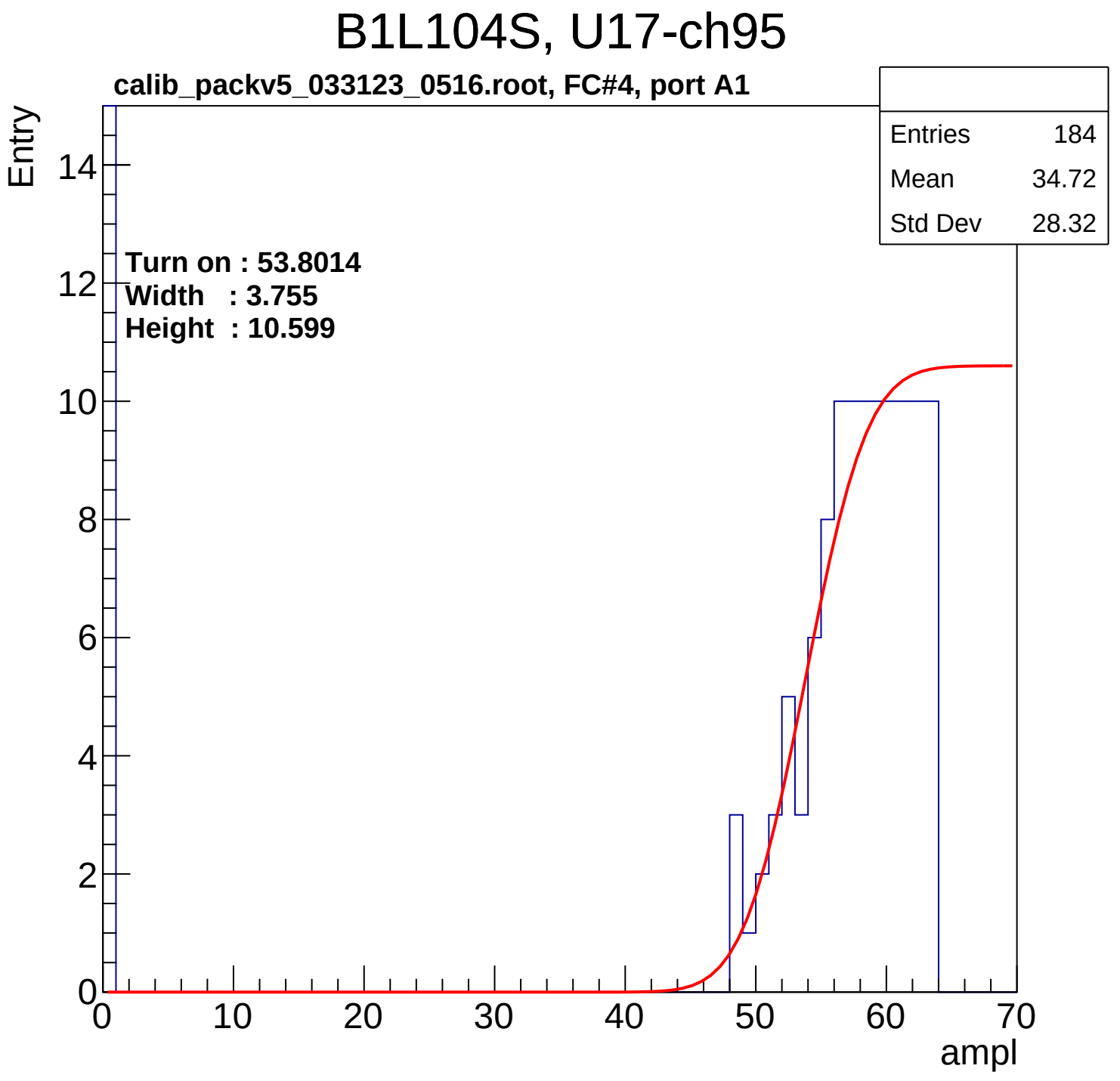
B1L104S, U17-ch95
calib_packv5_033123_0516.root, FC#4, port A1
Entries 184
Mean 34.72
Std Dev 28.32
Turn on : 53.8014
Width : 3.755
Height : 10.599
Entry
ampl
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2
4
6
8
10
12
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0
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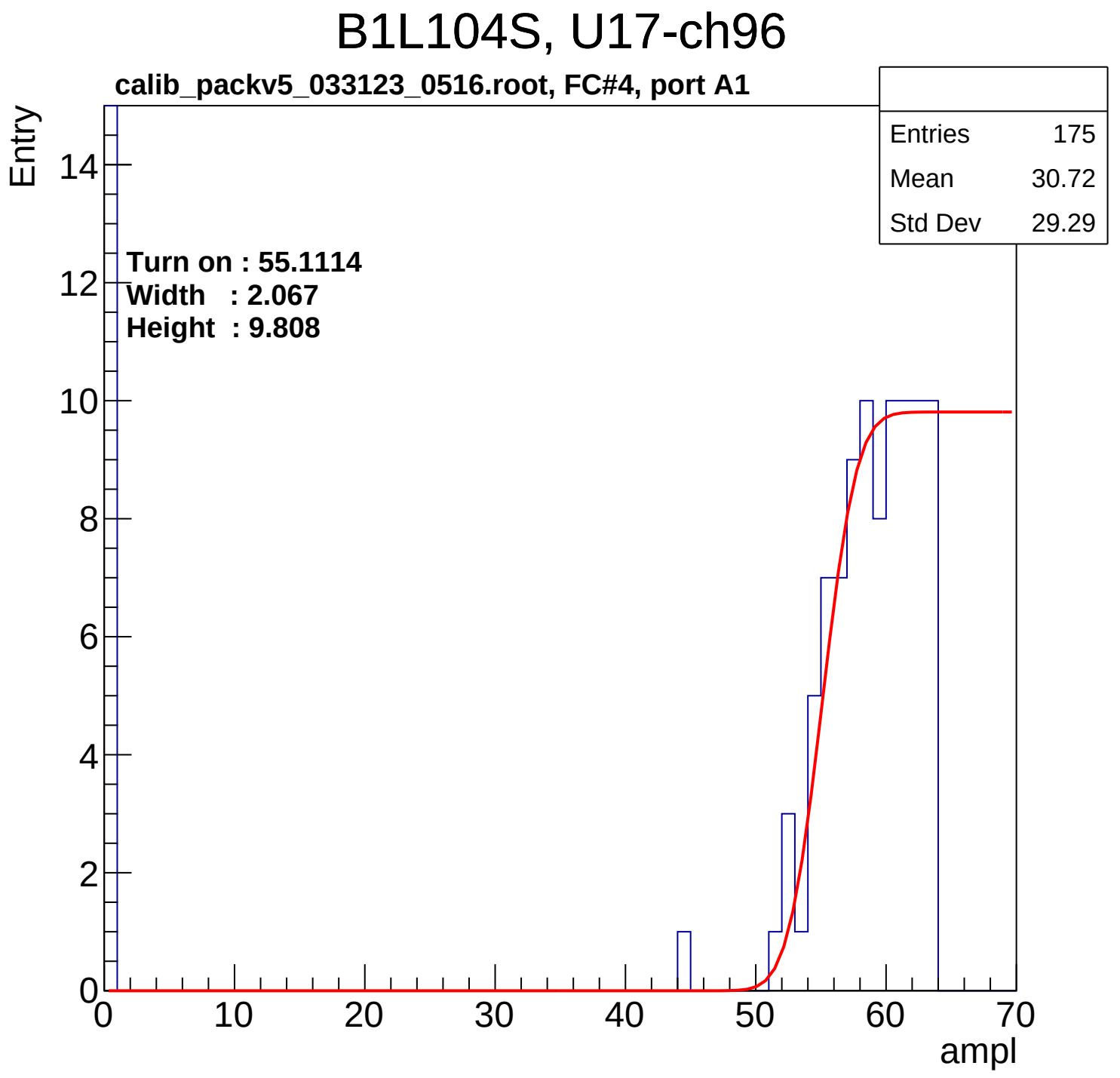
B1L104S, U17-ch96
calib_packv5_033123_0516.root, FC#4, port A1
Entries 175
Mean 30.72
Std Dev 29.29
Turn on : 55.1114
Width : 2.067
Height : 9.808
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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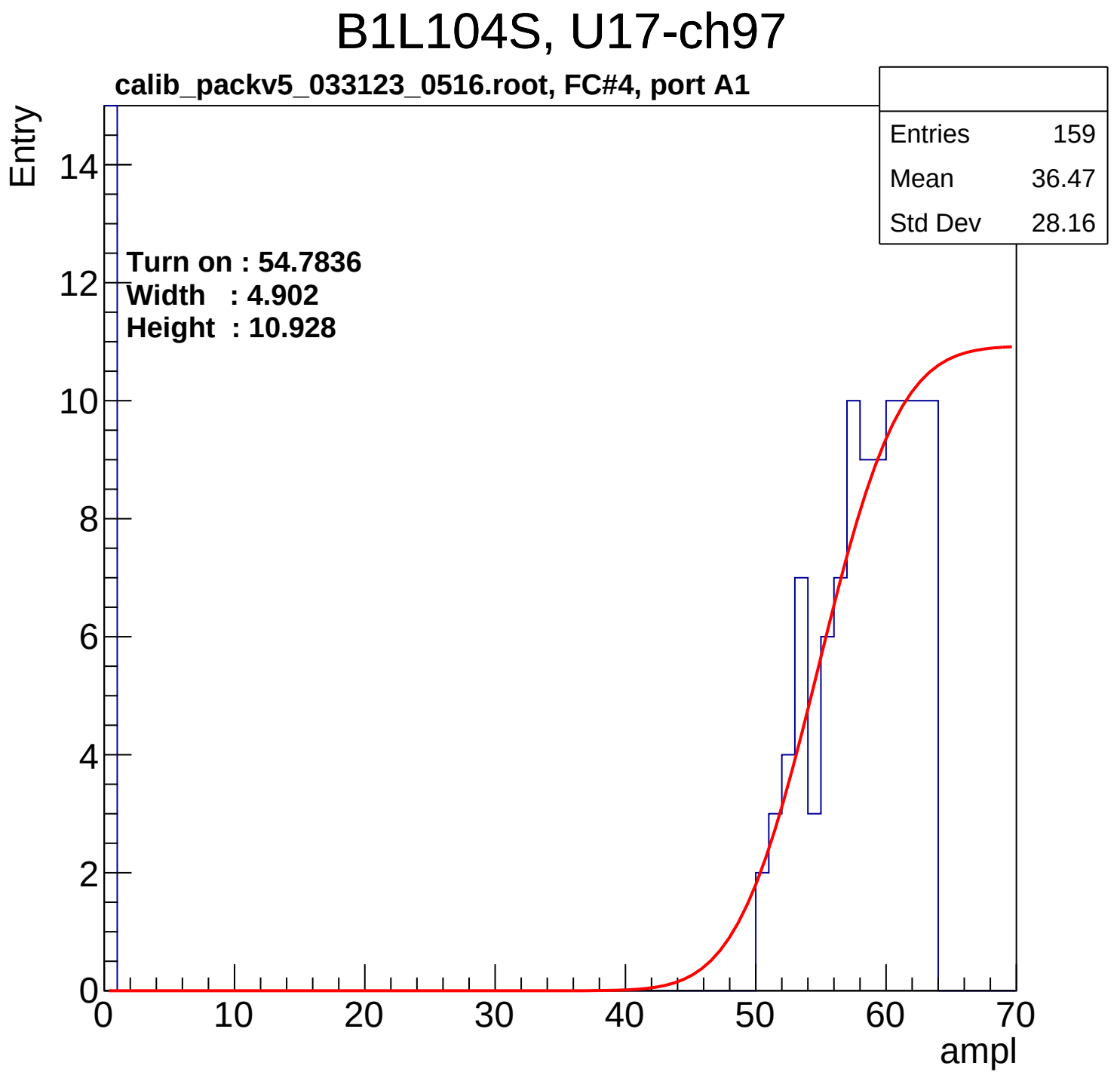
B1L104S, U17-ch97
calib_packv5_033123_0516.root, FC#4, port A1
Entries 159
Mean 36.47
Std Dev 28.16
Turn on : 54.7836
Width : 4.902
Height : 10.928
Entry
ampl
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2
4
6
8
10
12
14
0
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60
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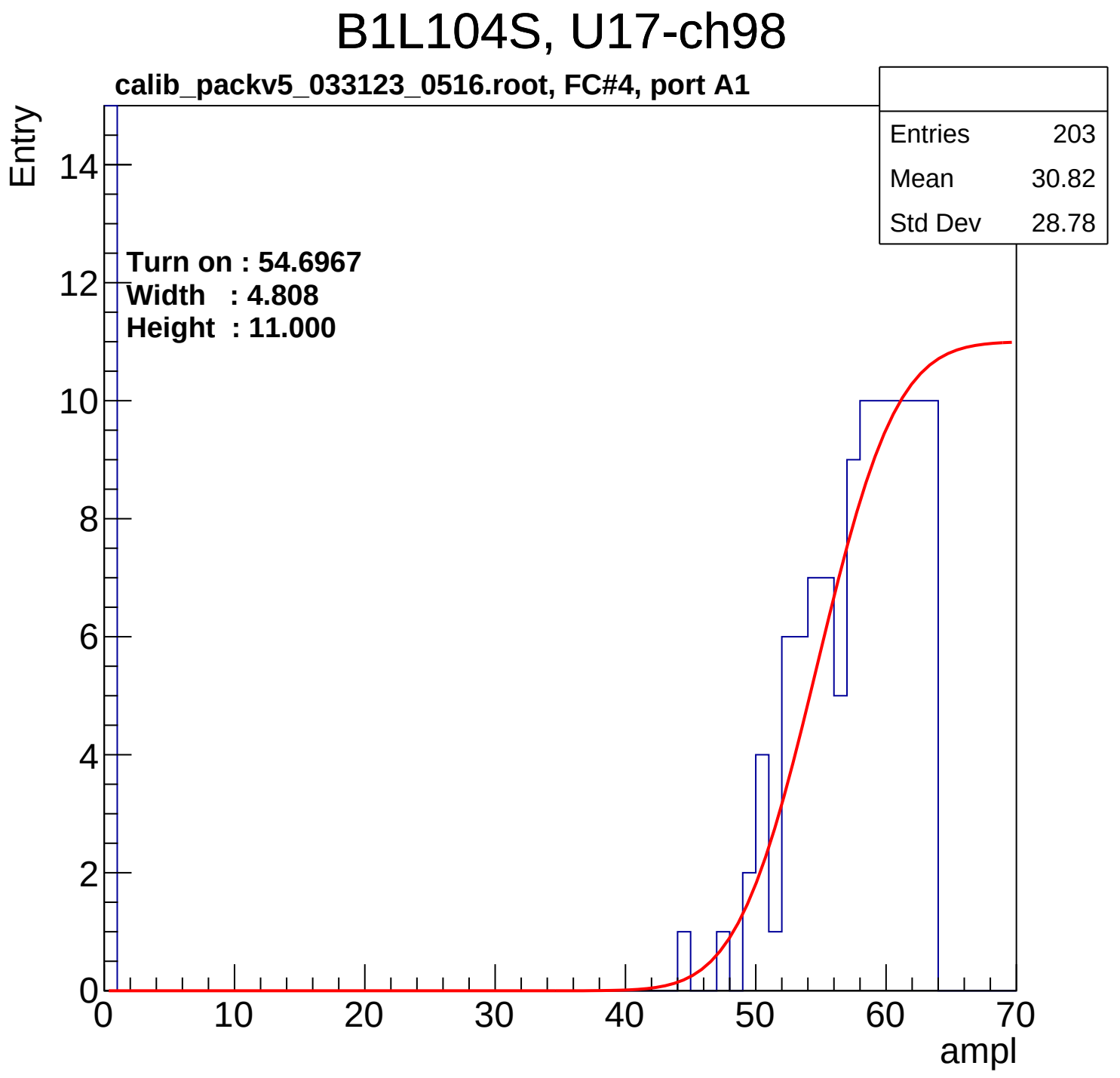
B1L104S, U17-ch98
calib_packv5_033123_0516.root, FC#4, port A1
Entries 203
Mean 30.82
Std Dev 28.78
Turn on : 54.6967
Width : 4.808
Height : 11.000
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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60
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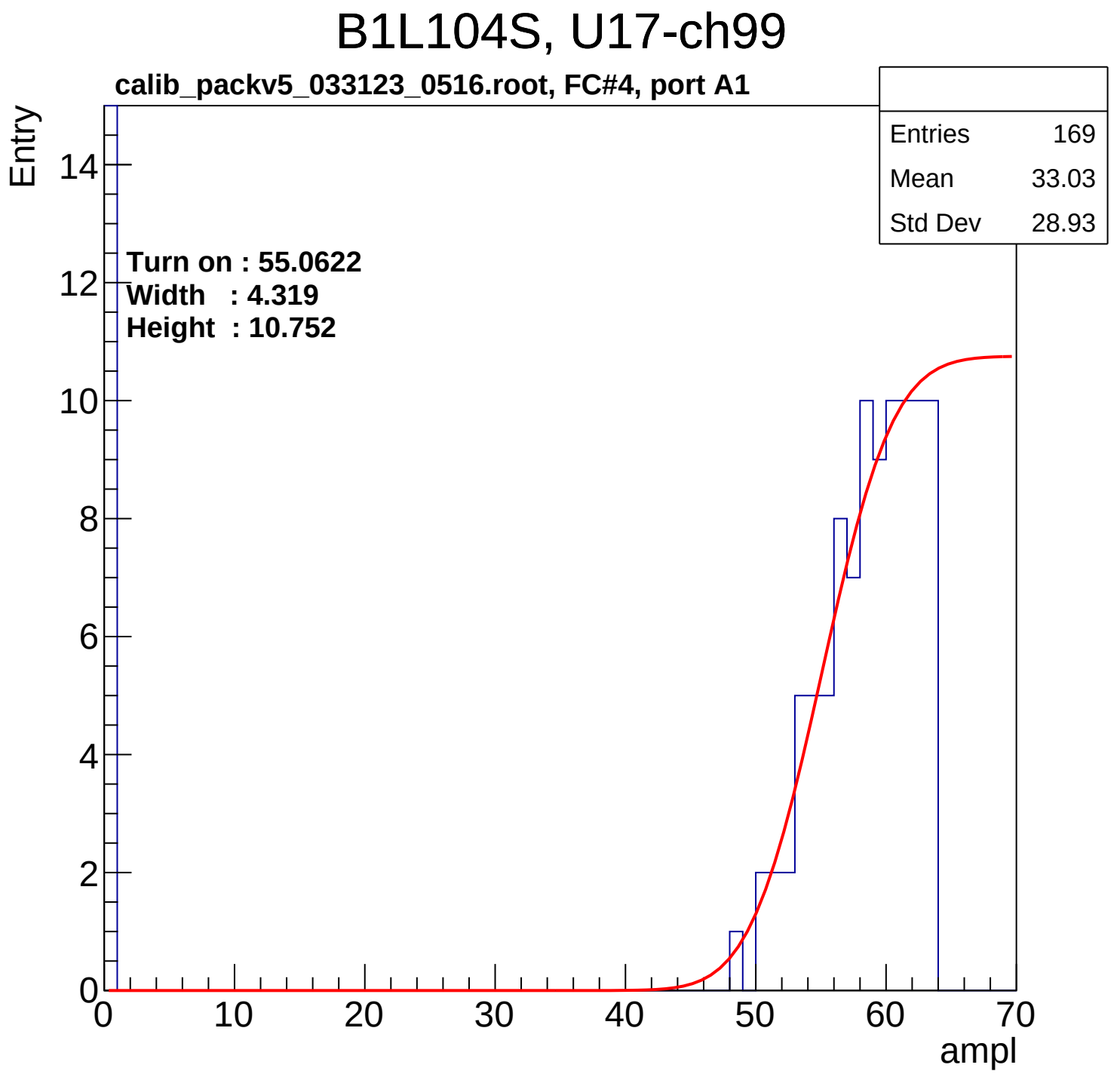
B1L104S, U17-ch99
calib_packv5_033123_0516.root, FC#4, port A1
Entries 169
Mean 33.03
Std Dev 28.93
Turn on : 55.0622
Width : 4.319
Height : 10.752
Entry
ampl
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4
6
8
10
12
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0
10
20
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60
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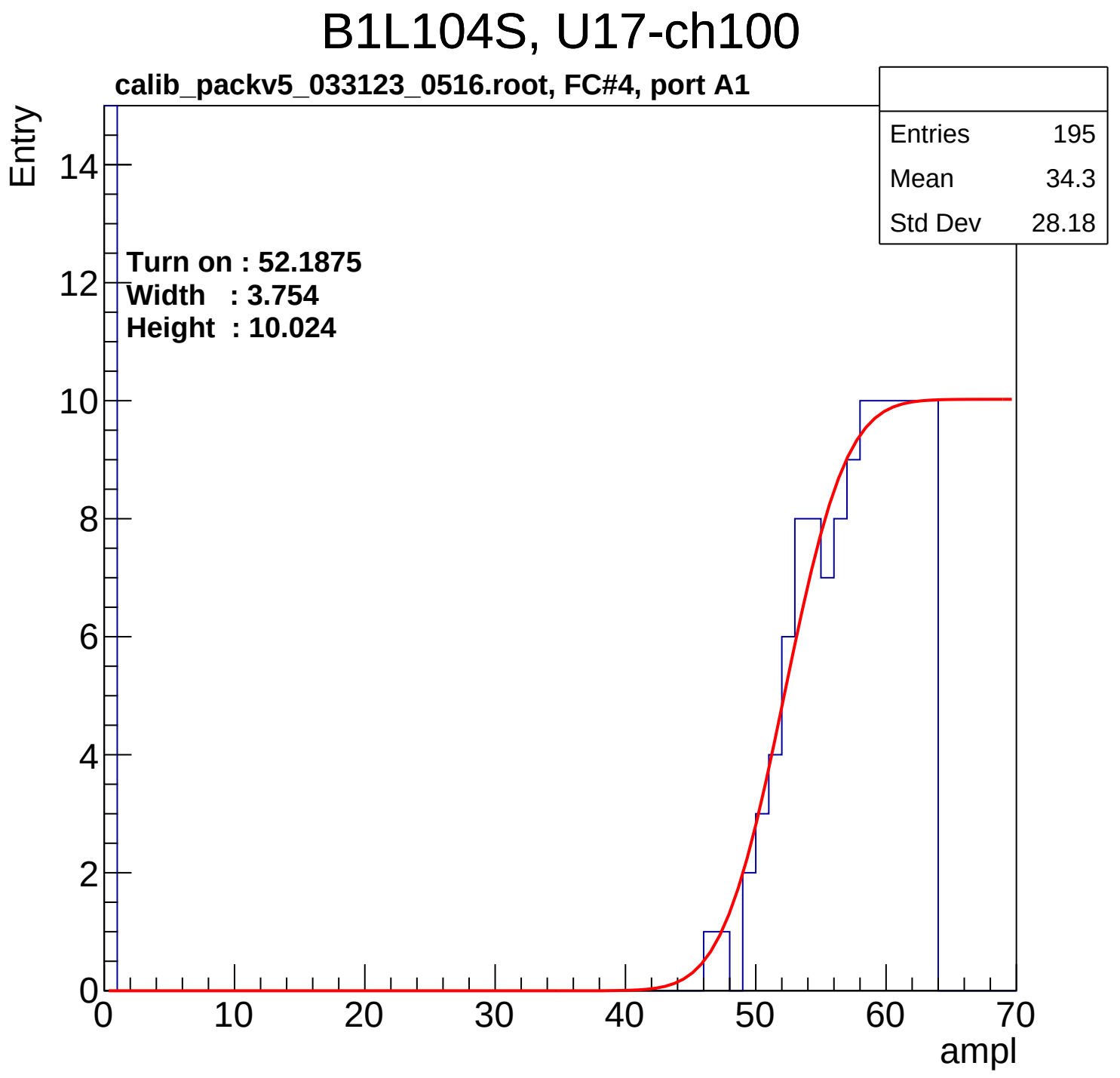
B1L104S, U17-ch100
calib_packv5_033123_0516.root, FC#4, port A1
Entries 195
Mean 34.3
Std Dev 28.18
Turn on : 52.1875
Width : 3.754
Height : 10.024
Entry
ampl
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6
8
10
12
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0
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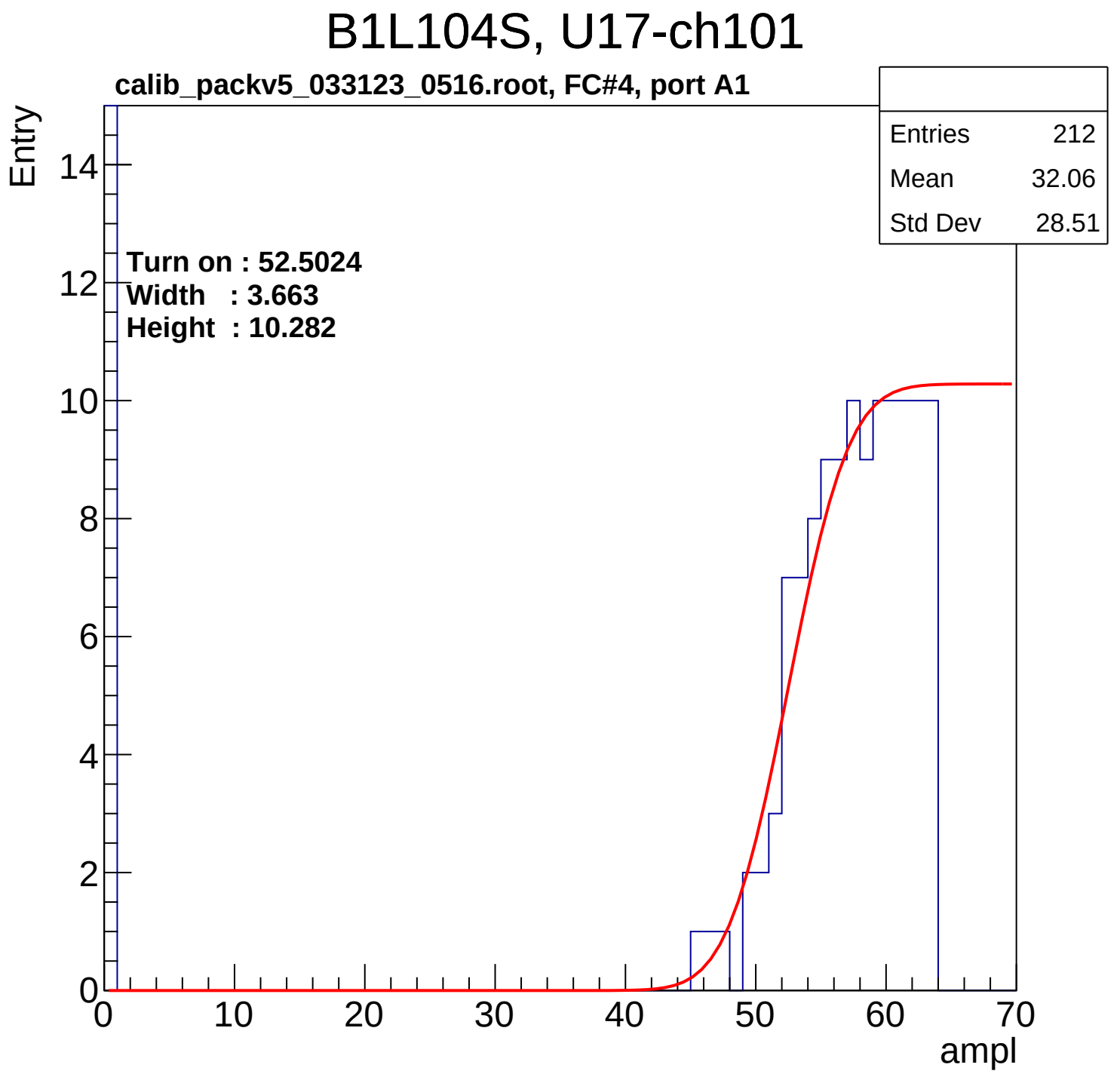
B1L104S, U17-ch101
calib_packv5_033123_0516.root, FC#4, port A1
Entries 212
Mean 32.06
Std Dev 28.51
Turn on : 52.5024
Width : 3.663
Height : 10.282
Entry
ampl
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6
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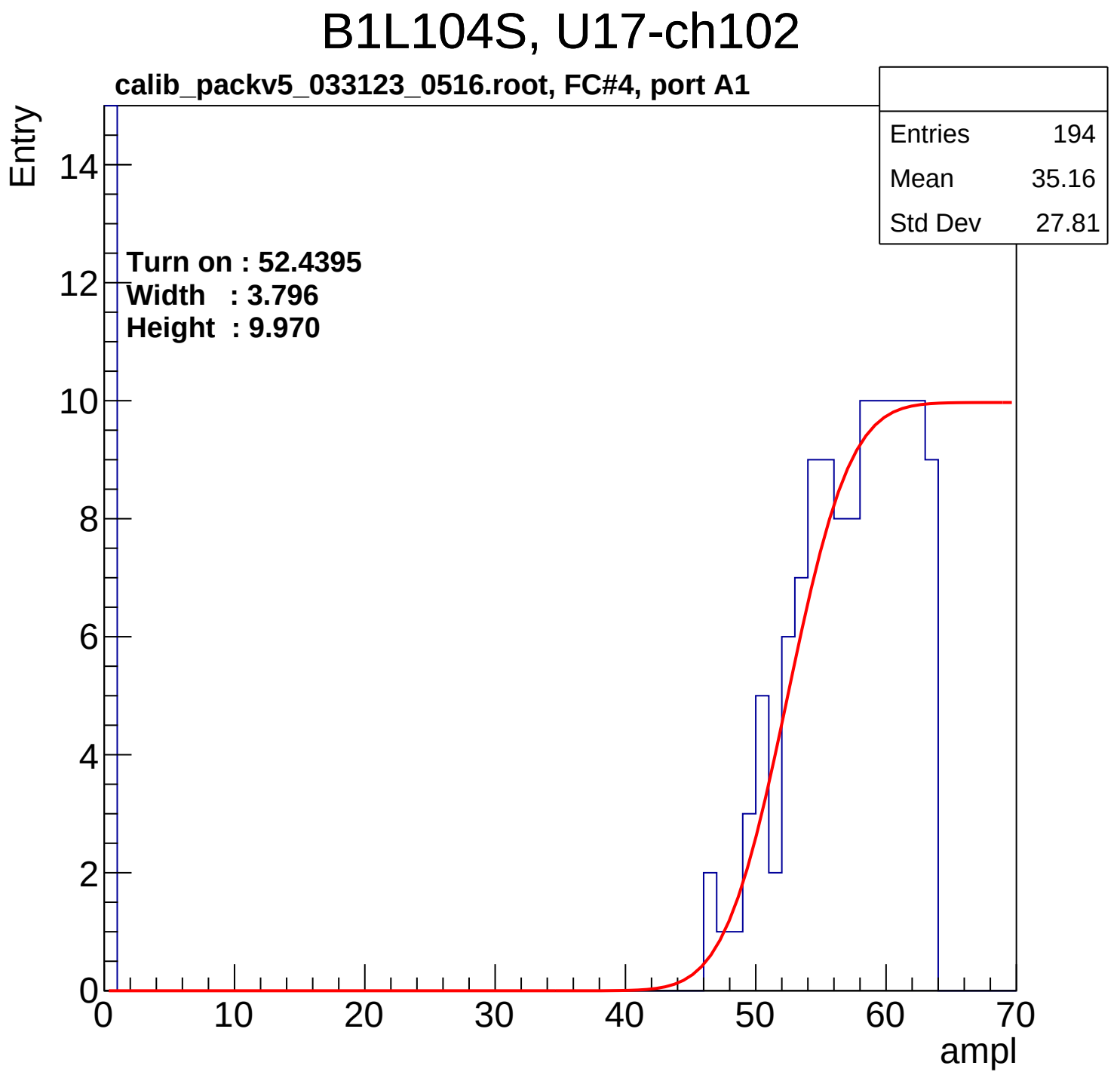
B1L104S, U17-ch102
calib_packv5_033123_0516.root, FC#4, port A1
Entries 194
Mean 35.16
Std Dev 27.81
Turn on : 52.4395
Width : 3.796
Height : 9.970
Entry
ampl
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2
4
6
8
10
12
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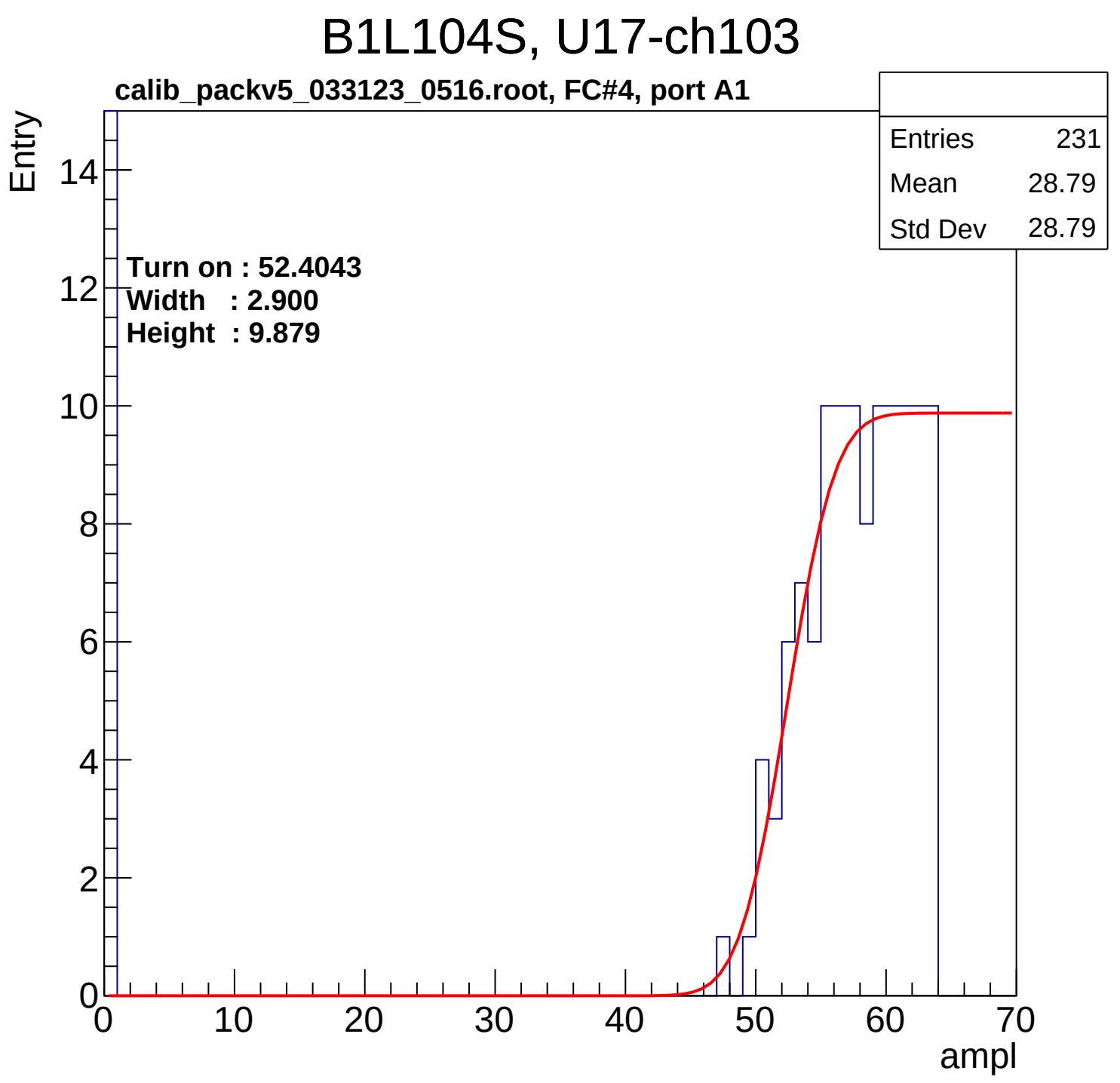
B1L104S, U17-ch103
calib_packv5_033123_0516.root, FC#4, port A1
Entries 231
Mean 28.79
Std Dev 28.79
Turn on : 52.4043
Width : 2.900
Height : 9.879
Entry
ampl
0
2
4
6
8
10
12
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0
10
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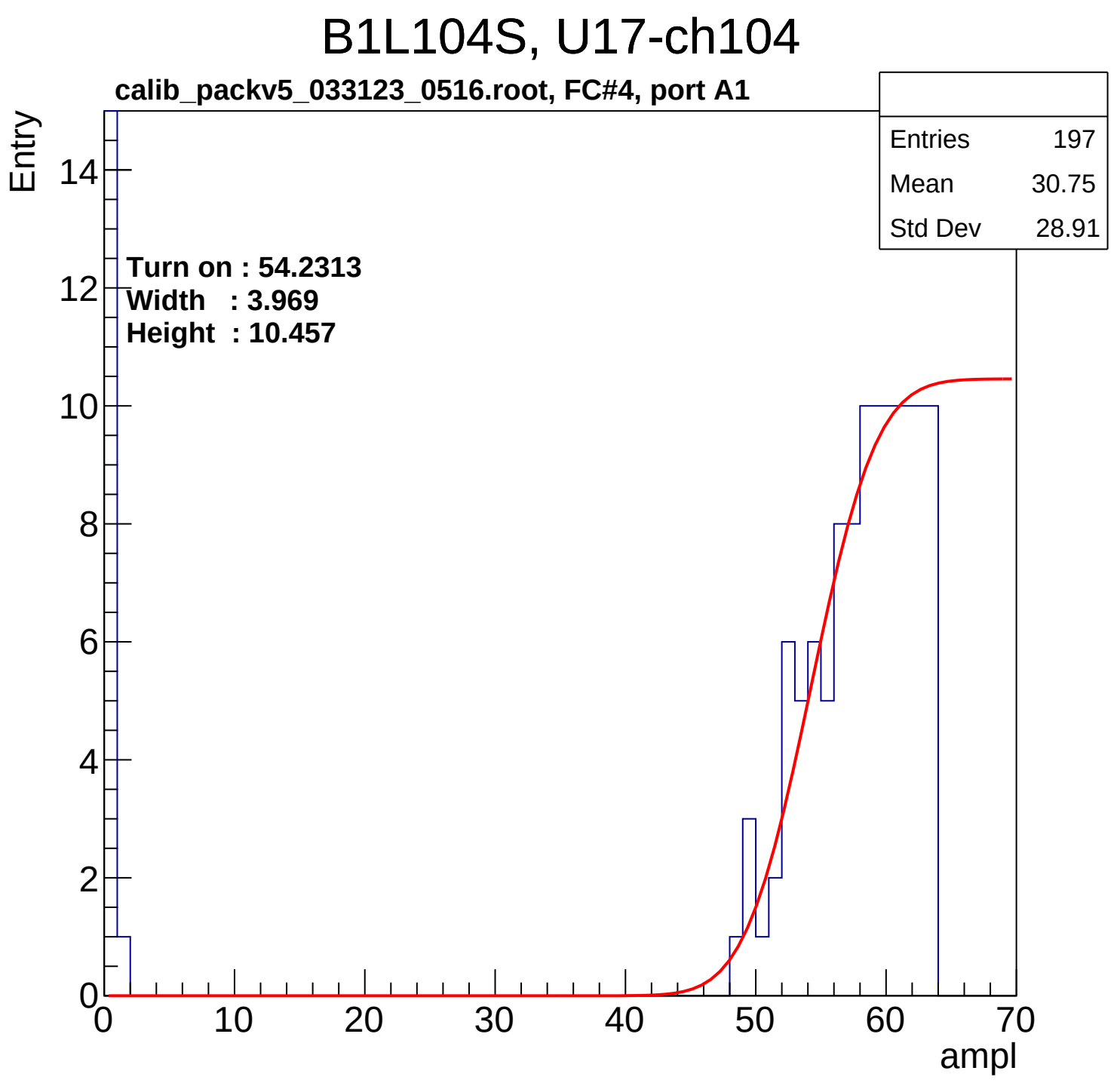
B1L104S, U17-ch104
calib_packv5_033123_0516.root, FC#4, port A1
Entries 197
Mean 30.75
Std Dev 28.91
Turn on : 54.2313
Width : 3.969
Height : 10.457
Entry
ampl
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6
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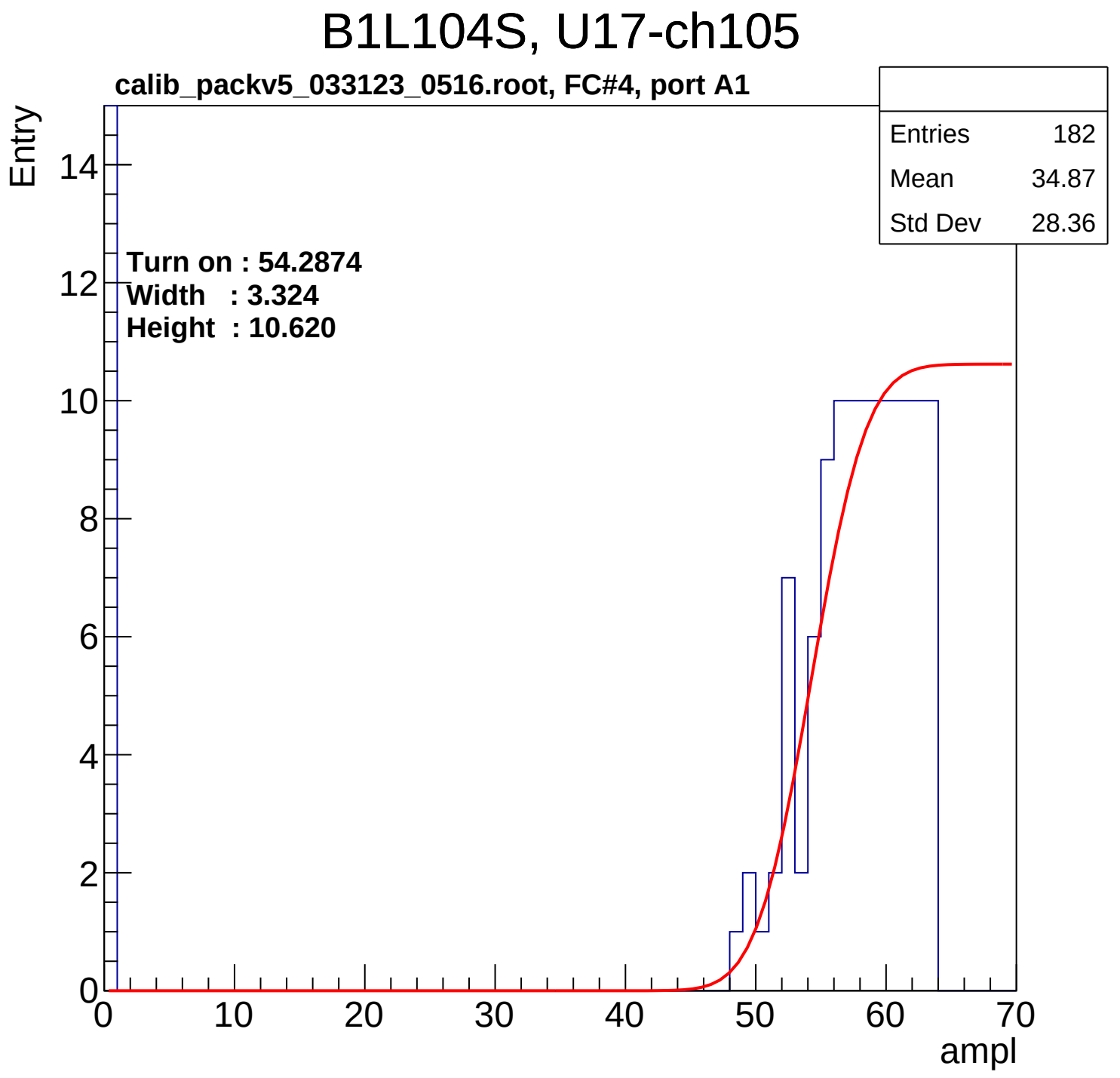
B1L104S, U17-ch105
calib_packv5_033123_0516.root, FC#4, port A1
Entries 182
Mean 34.87
Std Dev 28.36
Turn on : 54.2874
Width : 3.324
Height : 10.620
Entry
ampl
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4
6
8
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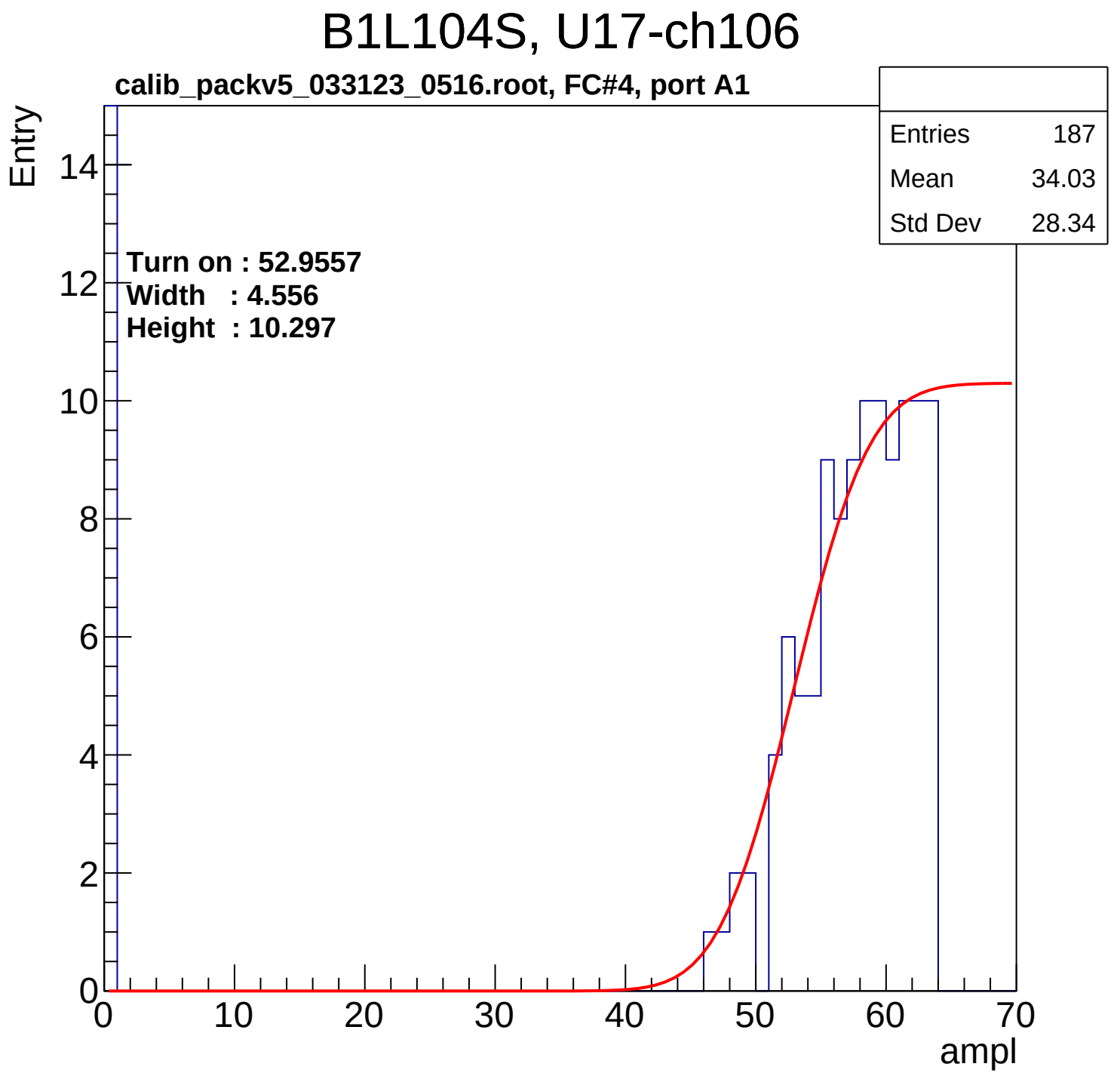
B1L104S, U17-ch106
calib_packv5_033123_0516.root, FC#4, port A1
Entries 187
Mean 34.03
Std Dev 28.34
Turn on : 52.9557
Width : 4.556
Height : 10.297
Entry
ampl
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10
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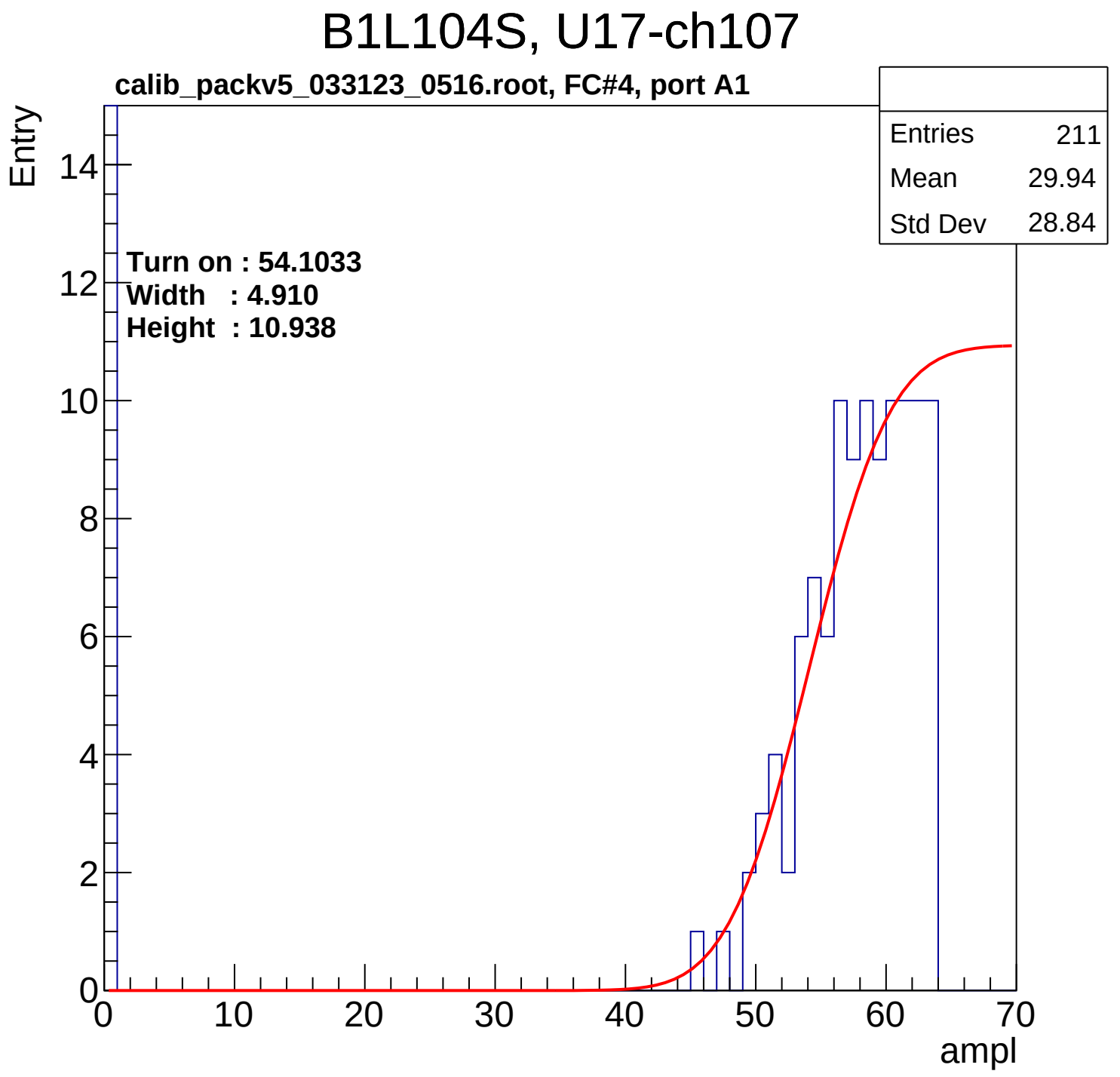
B1L104S, U17-ch107
calib_packv5_033123_0516.root, FC#4, port A1
Entries 211
Mean 29.94
Std Dev 28.84
Turn on : 54.1033
Width : 4.910
Height : 10.938
Entry
ampl
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6
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10
12
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60
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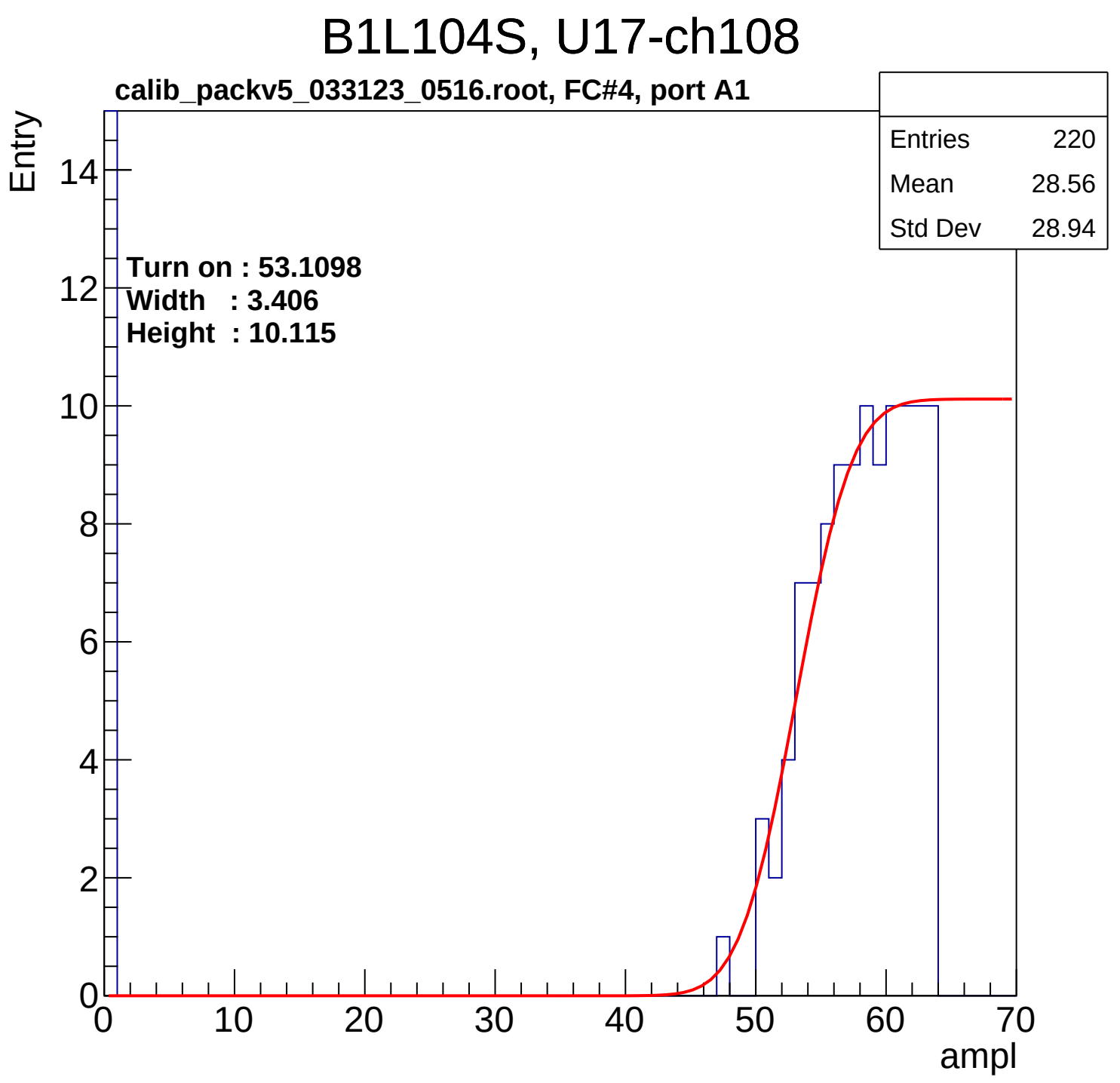
B1L104S, U17-ch108
calib_packv5_033123_0516.root, FC#4, port A1
Entries 220
Mean 28.56
Std Dev 28.94
Turn on : 53.1098
Width : 3.406
Height : 10.115
Entry
ampl
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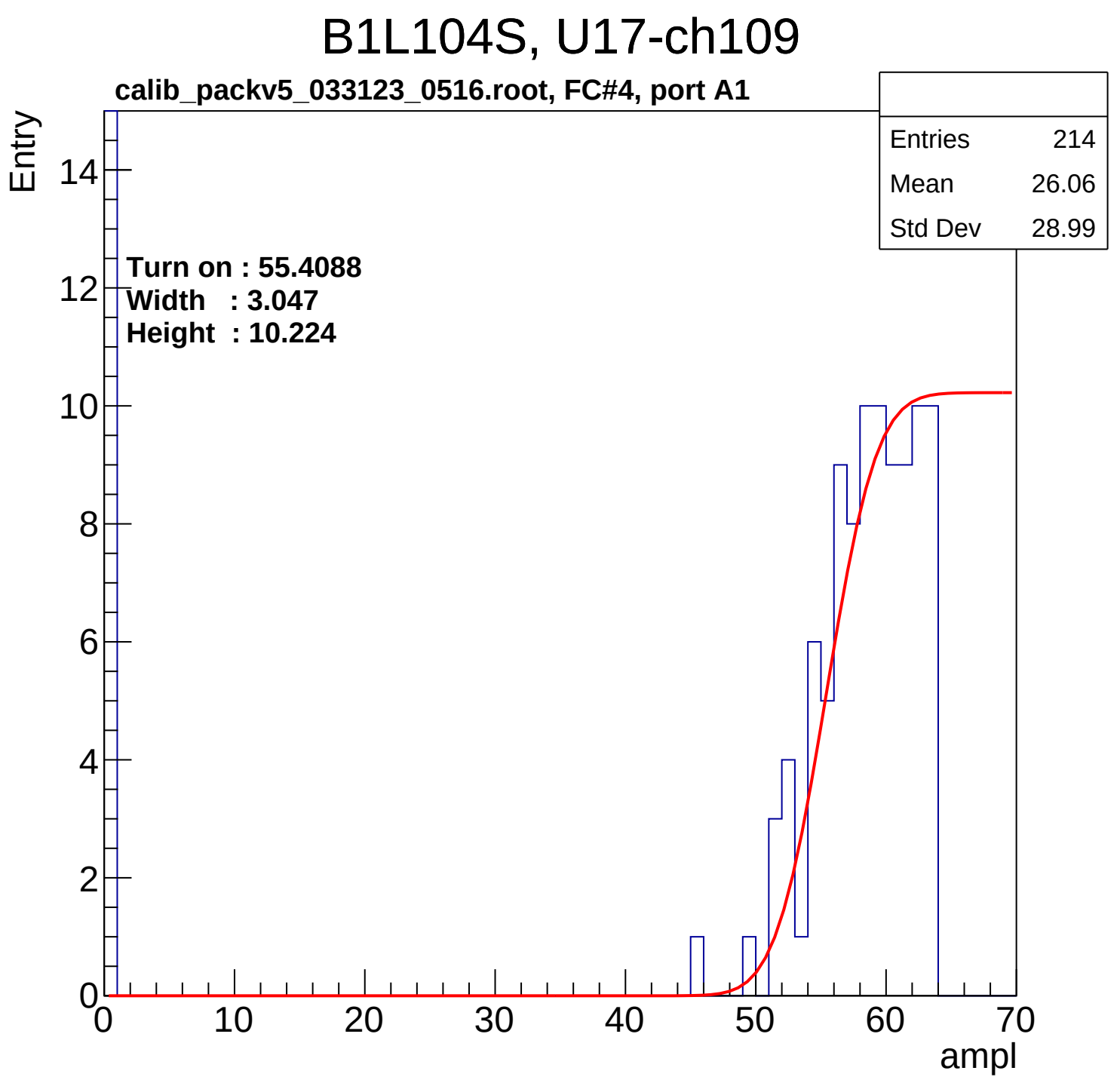
B1L104S, U17-ch109
calib_packv5_033123_0516.root, FC#4, port A1
Entries 214
Mean 26.06
Std Dev 28.99
Turn on : 55.4088
Width : 3.047
Height : 10.224
Entry
ampl
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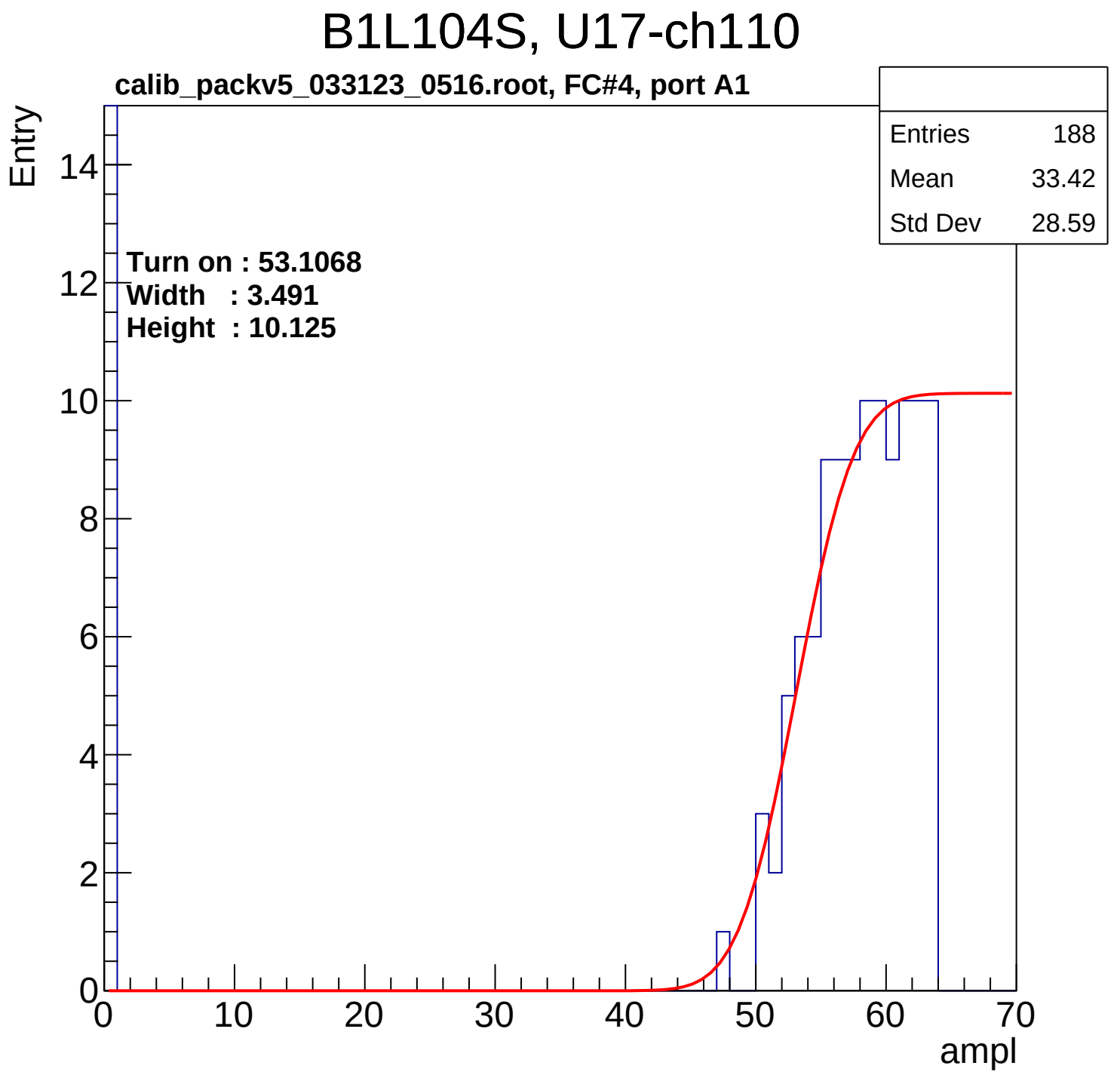
B1L104S, U17-ch110
calib_packv5_033123_0516.root, FC#4, port A1
Entries 188
Mean 33.42
Std Dev 28.59
Turn on : 53.1068
Width : 3.491
Height : 10.125
Entry
ampl
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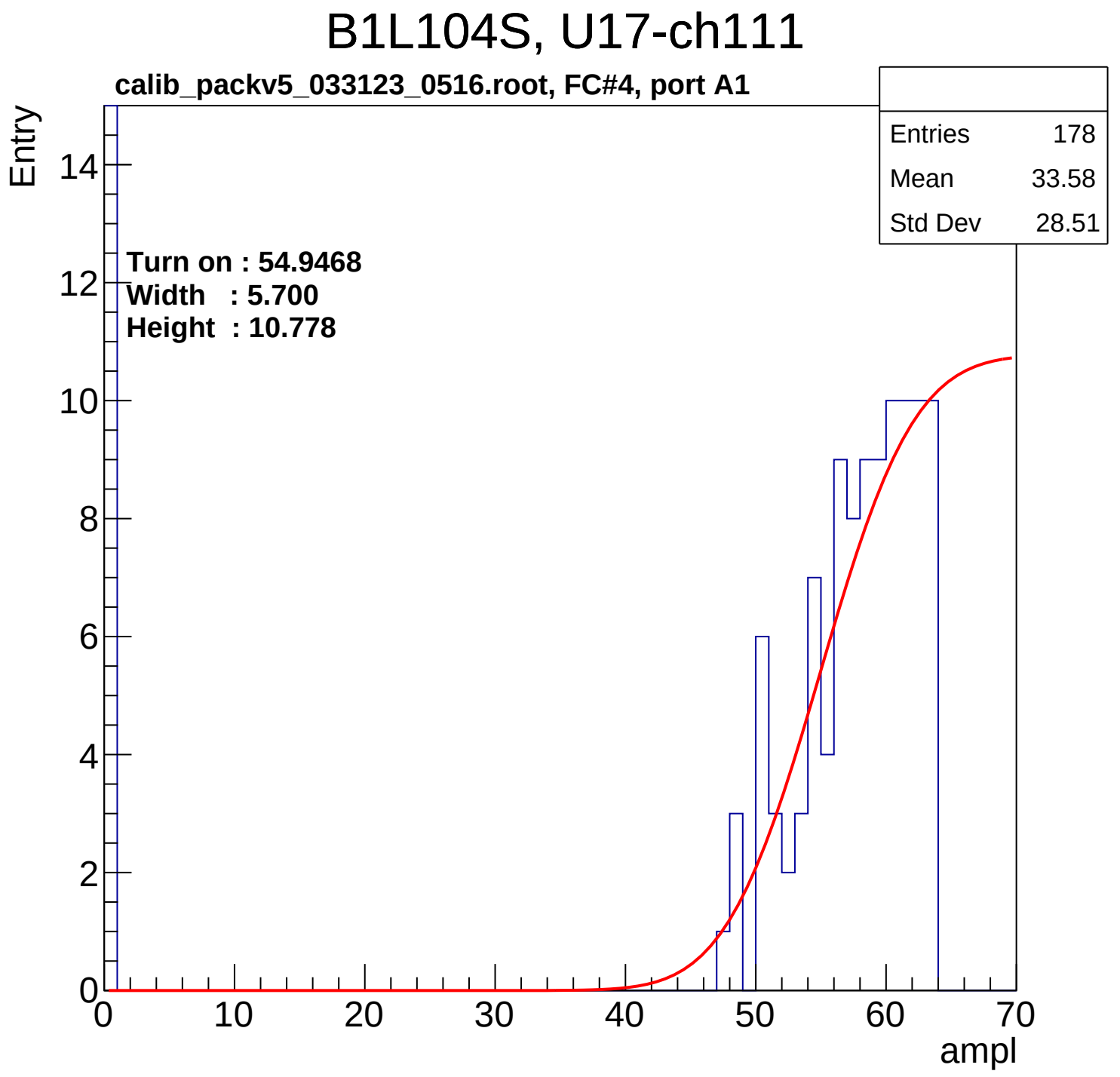
B1L104S, U17-ch111
calib_packv5_033123_0516.root, FC#4, port A1
Entries 178
Mean 33.58
Std Dev 28.51
Turn on : 54.9468
Width : 5.700
Height : 10.778
Entry
ampl
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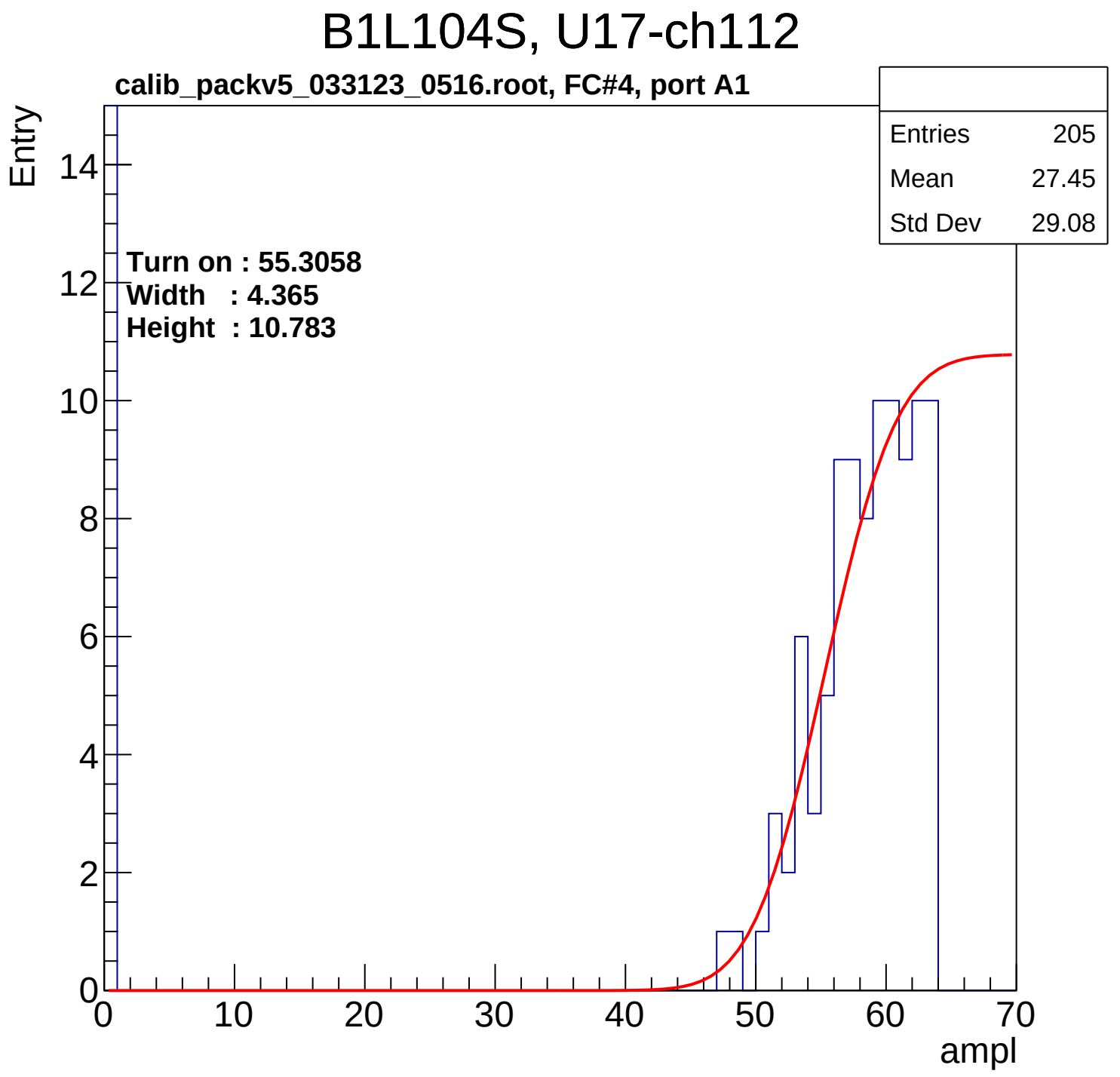
B1L104S, U17-ch112
calib_packv5_033123_0516.root, FC#4, port A1
Entries 205
Mean 27.45
Std Dev 29.08
Turn on : 55.3058
Width : 4.365
Height : 10.783
Entry
ampl
0
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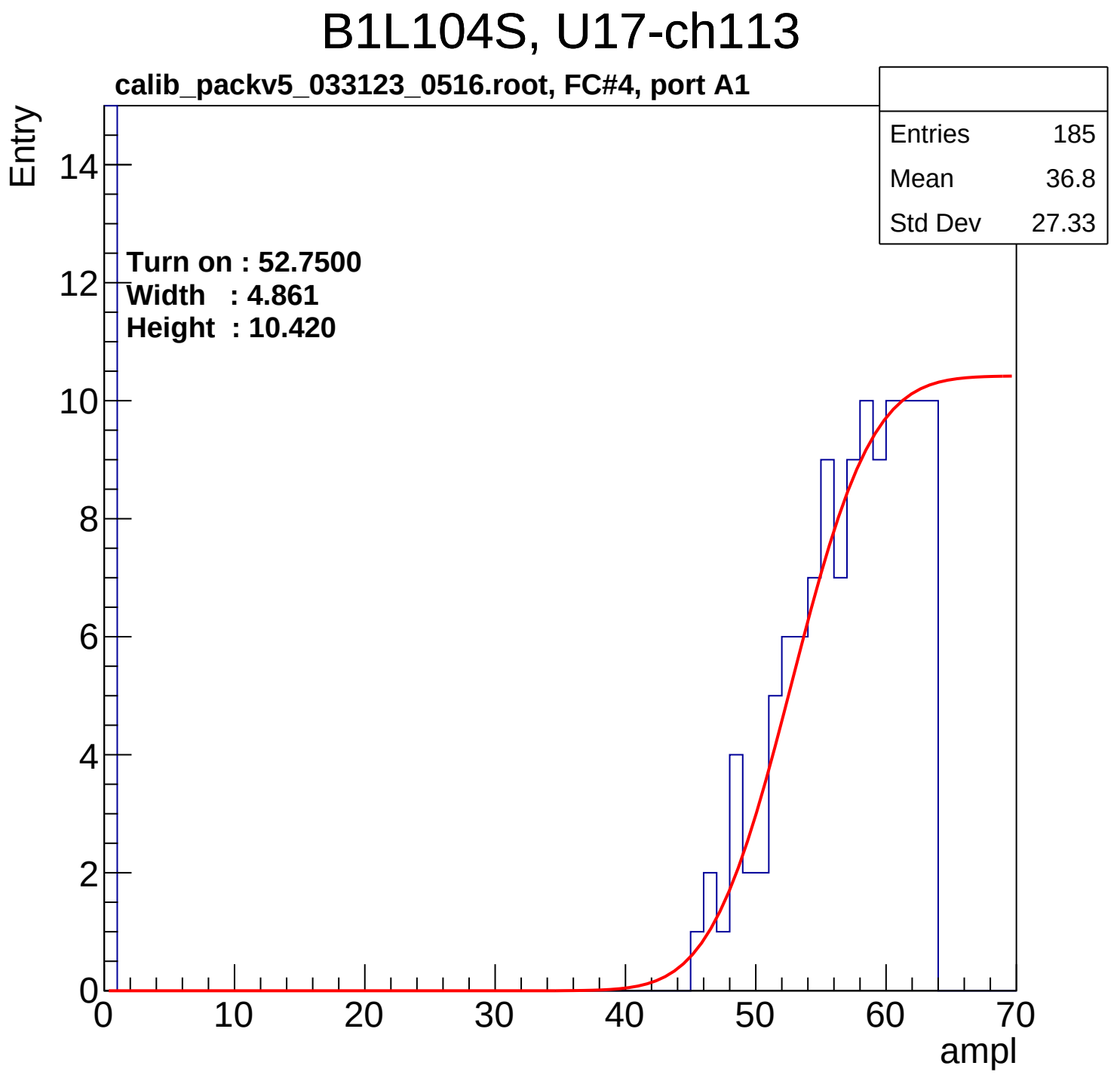
B1L104S, U17-ch113
calib_packv5_033123_0516.root, FC#4, port A1
Entries 185
Mean 36.8
Std Dev 27.33
Turn on : 52.7500
Width : 4.861
Height : 10.420
Entry
ampl
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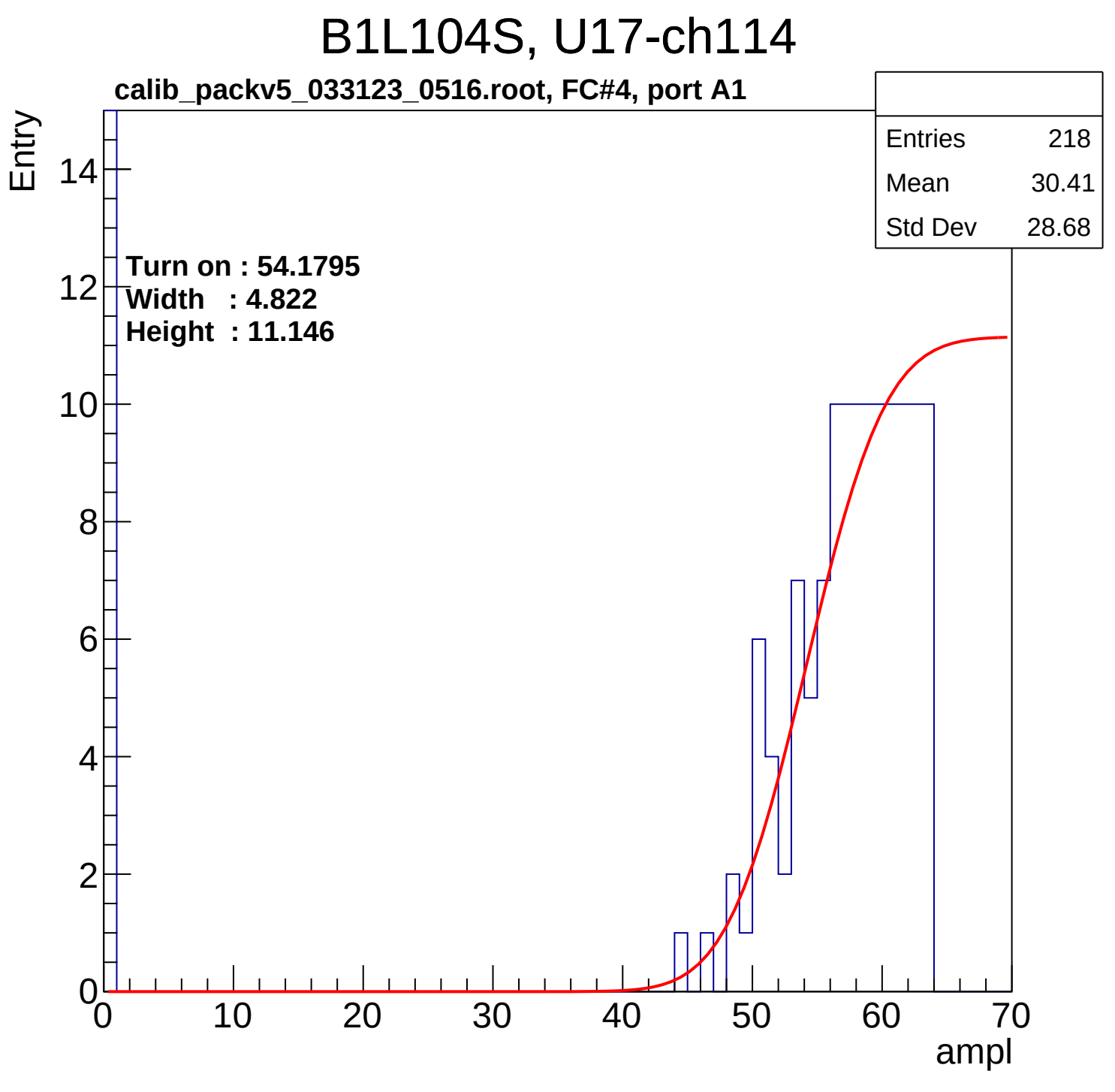
B1L104S, U17-ch114
calib_packv5_033123_0516.root, FC#4, port A1
Entries 218
Mean 30.41
Std Dev 28.68
Turn on : 54.1795
Width : 4.822
Height : 11.146
Entry
ampl
0
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6
8
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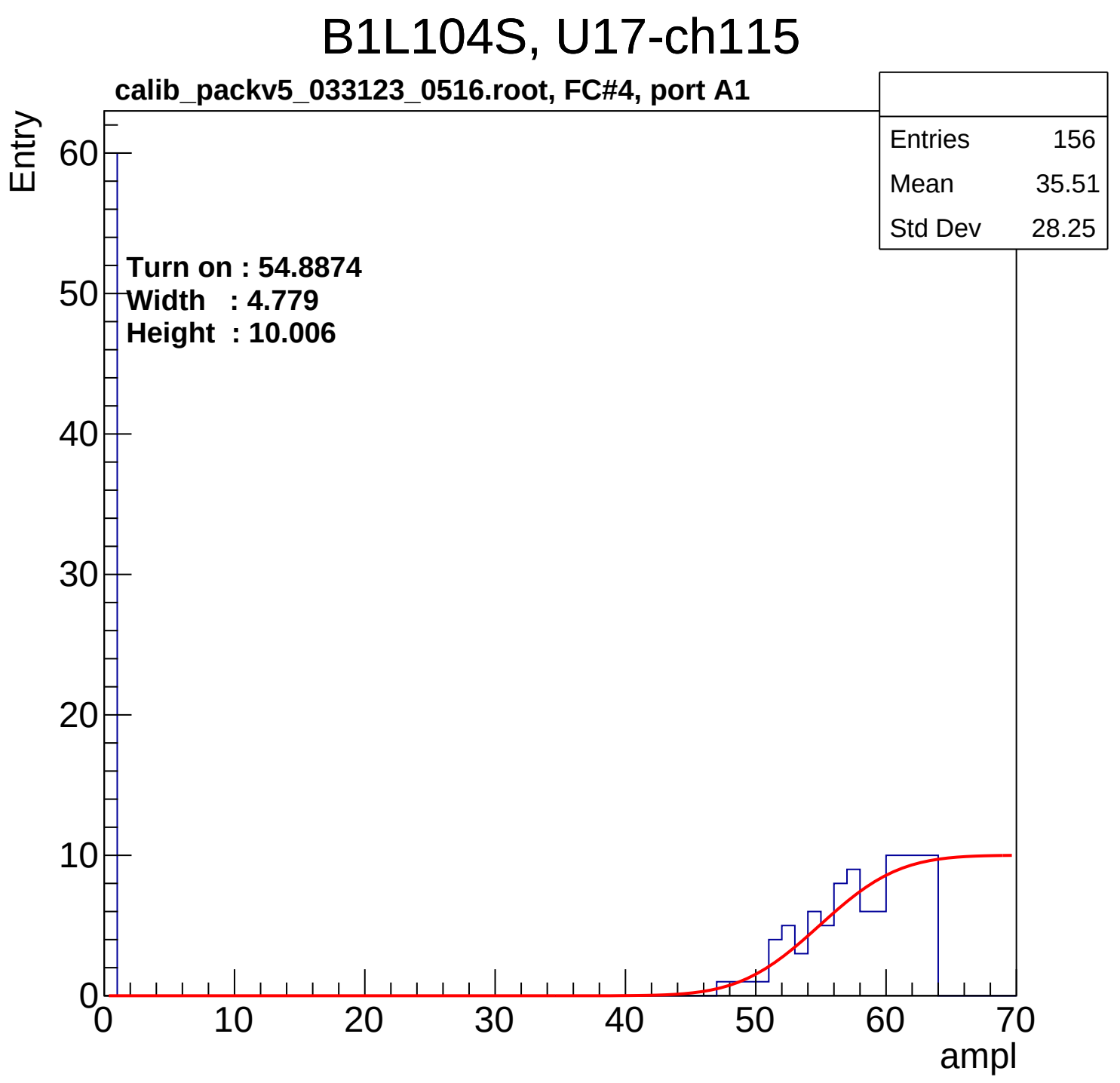
B1L104S, U17-ch115
calib_packv5_033123_0516.root, FC#4, port A1
Entries 156
Mean 35.51
Std Dev 28.25
Turn on : 54.8874
Width : 4.779
Height : 10.006
Entry
ampl
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40
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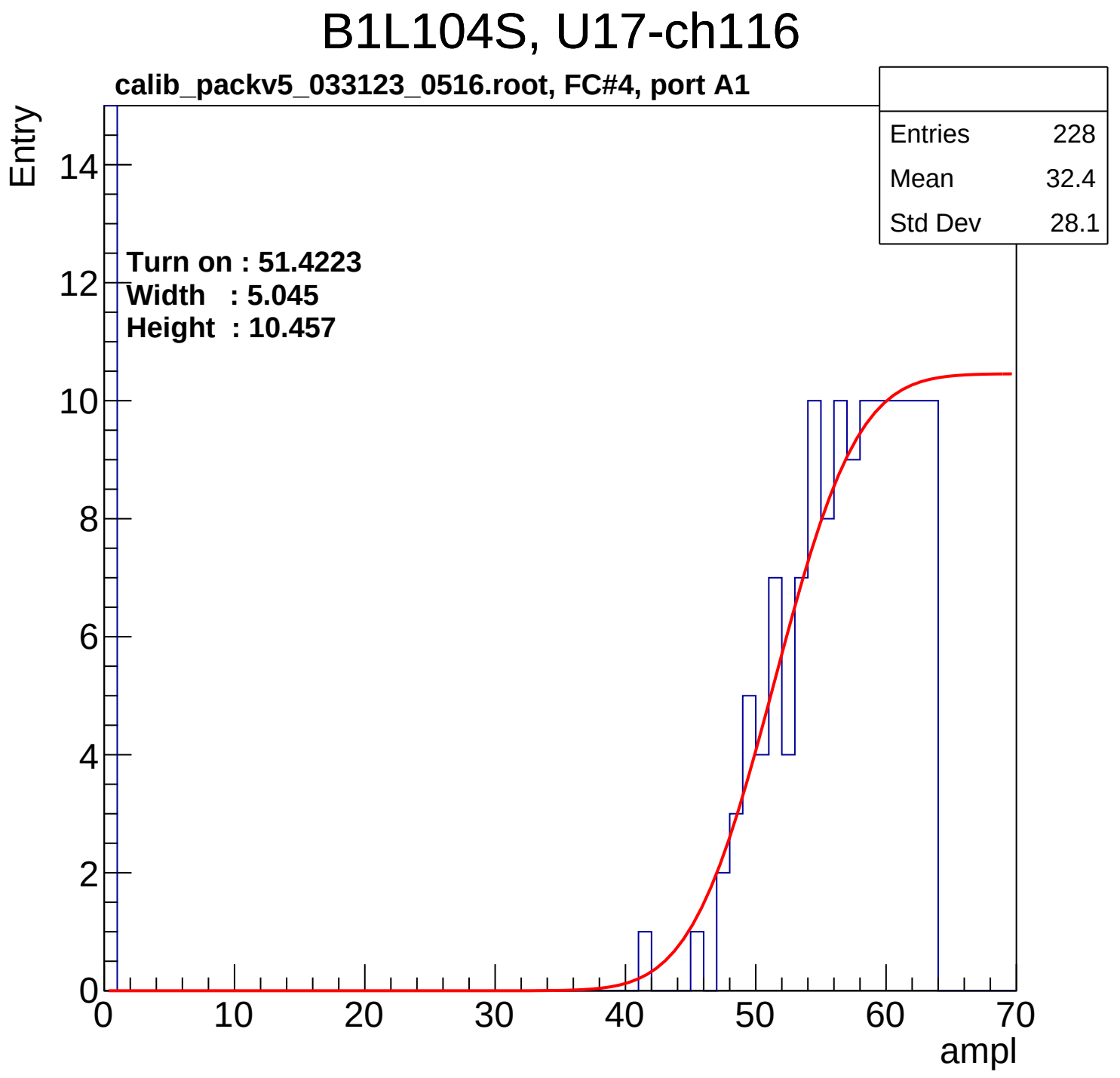
B1L104S, U17-ch116
calib_packv5_033123_0516.root, FC#4, port A1
Entries 228
Mean 32.4
Std Dev 28.1
Turn on : 51.4223
Width : 5.045
Height : 10.457
Entry
ampl
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4
6
8
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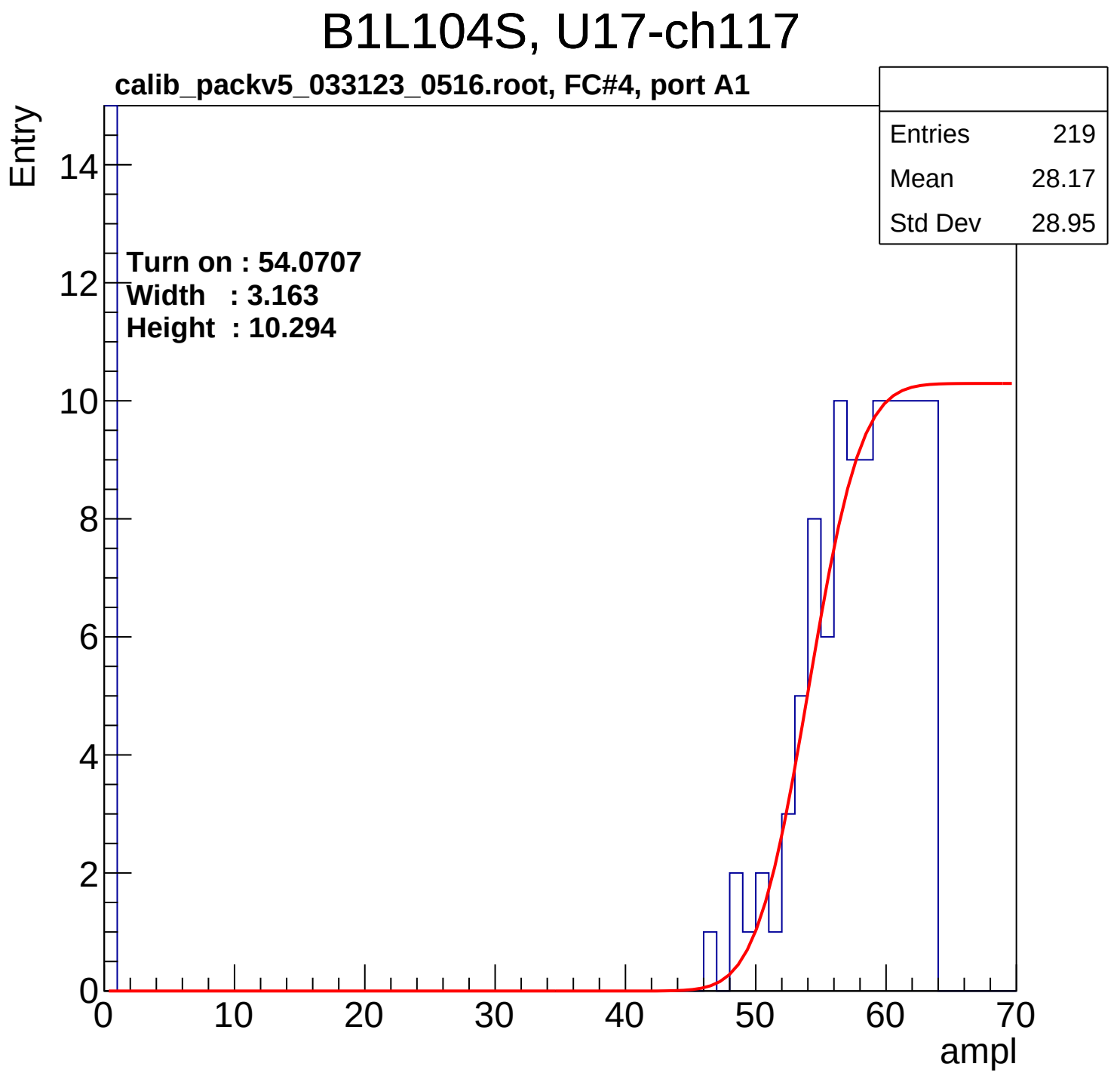
B1L104S, U17-ch117
calib_packv5_033123_0516.root, FC#4, port A1
Entries 219
Mean 28.17
Std Dev 28.95
Turn on : 54.0707
Width : 3.163
Height : 10.294
Entry
ampl
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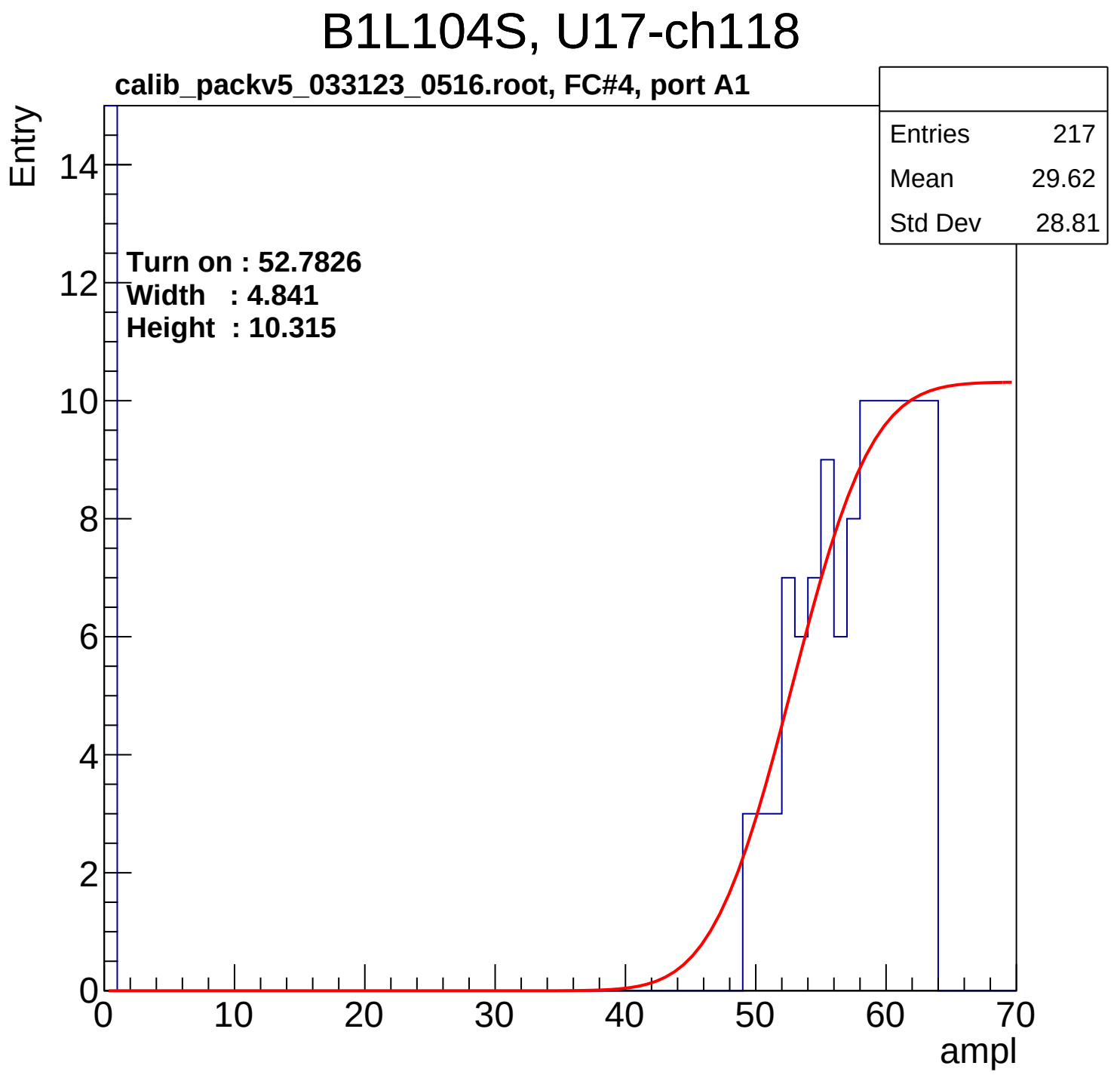
B1L104S, U17-ch118
calib_packv5_033123_0516.root, FC#4, port A1
Entries 217
Mean 29.62
Std Dev 28.81
Turn on : 52.7826
Width : 4.841
Height : 10.315
Entry
ampl
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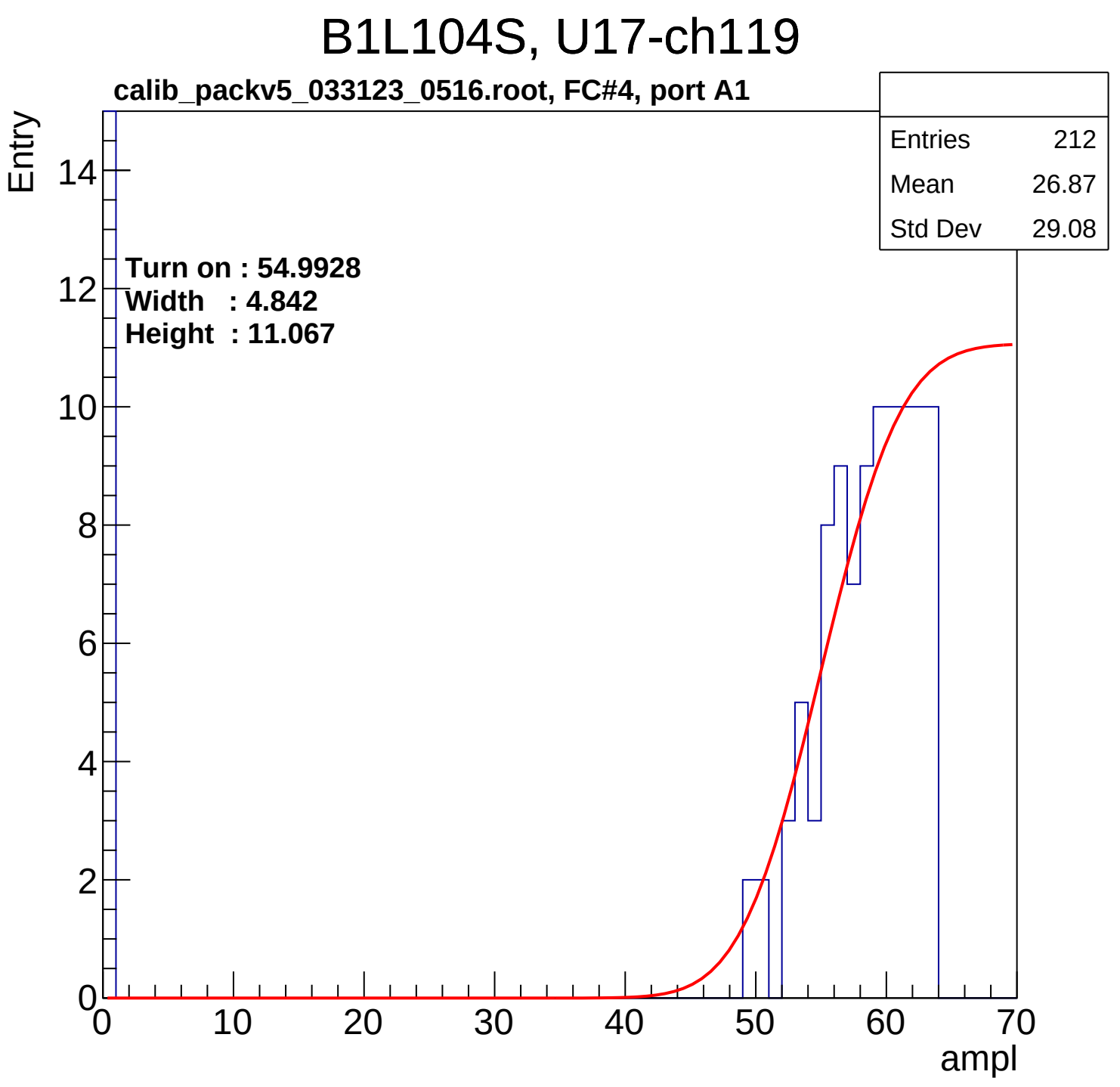
B1L104S, U17-ch119
calib_packv5_033123_0516.root, FC#4, port A1
Entries 212
Mean 26.87
Std Dev 29.08
Turn on : 54.9928
Width : 4.842
Height : 11.067
Entry
ampl
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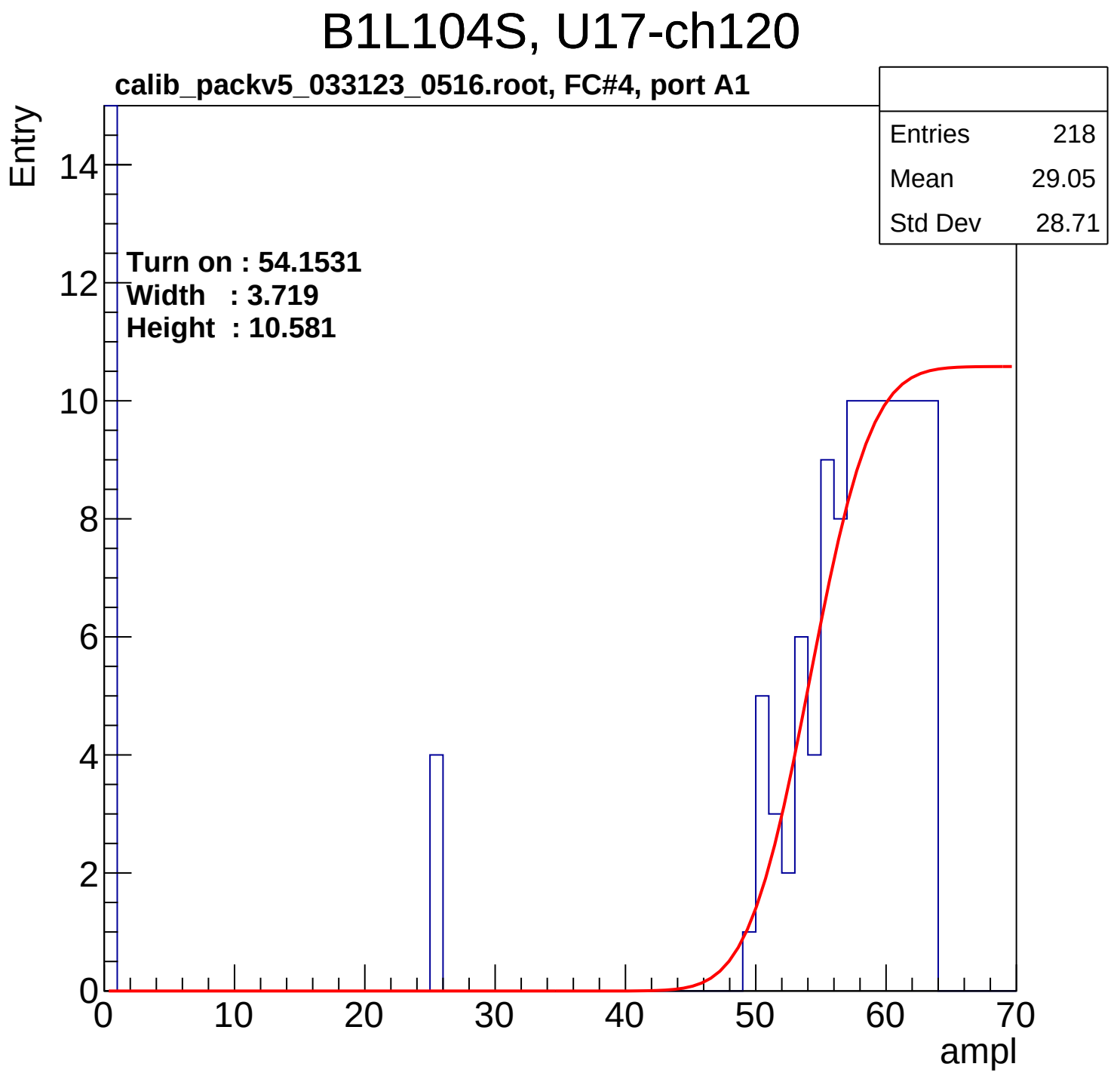
B1L104S, U17-ch120
calib_packv5_033123_0516.root, FC#4, port A1
Entries 218
Mean 29.05
Std Dev 28.71
Turn on : 54.1531
Width : 3.719
Height : 10.581
Entry
ampl
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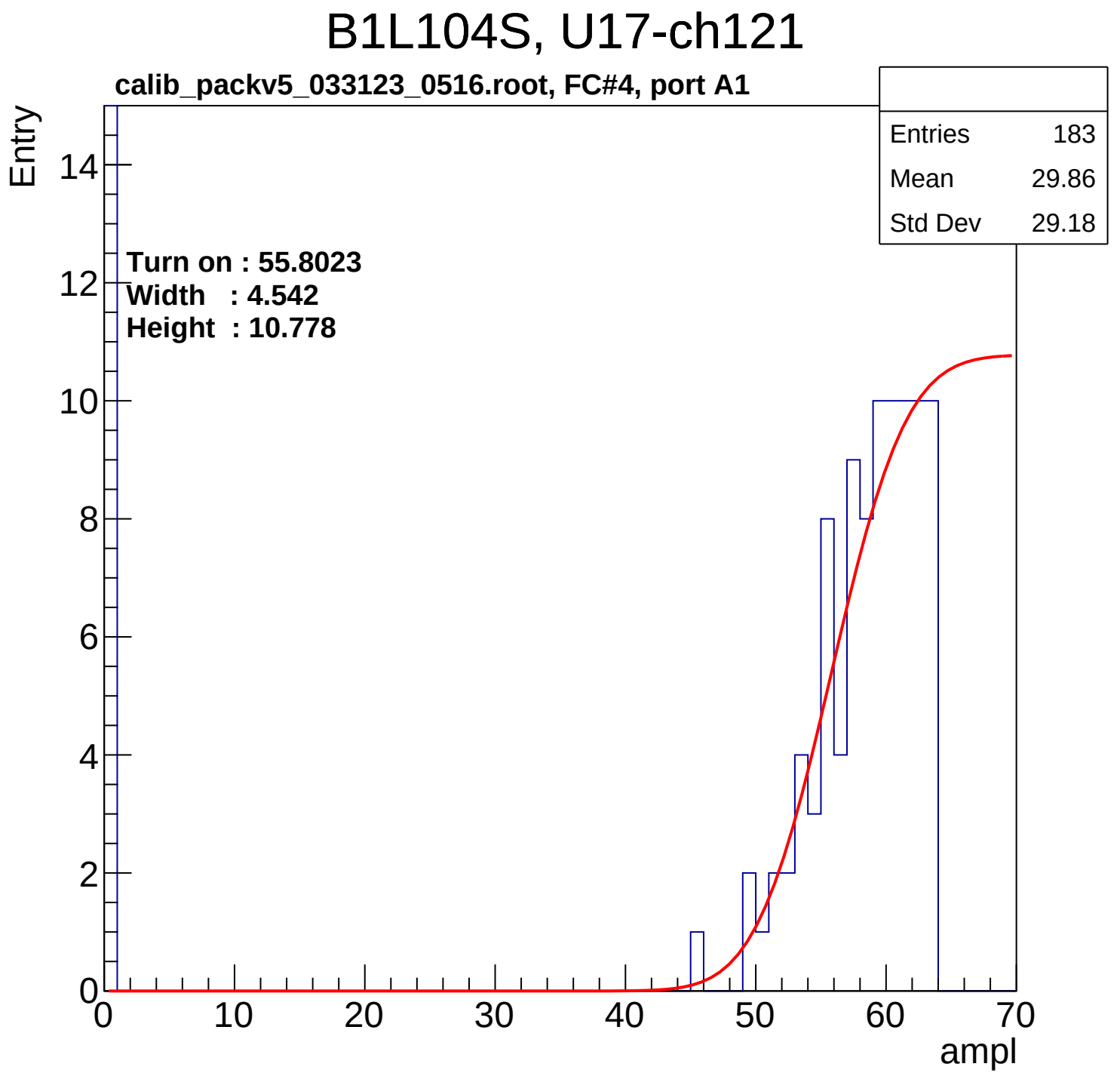
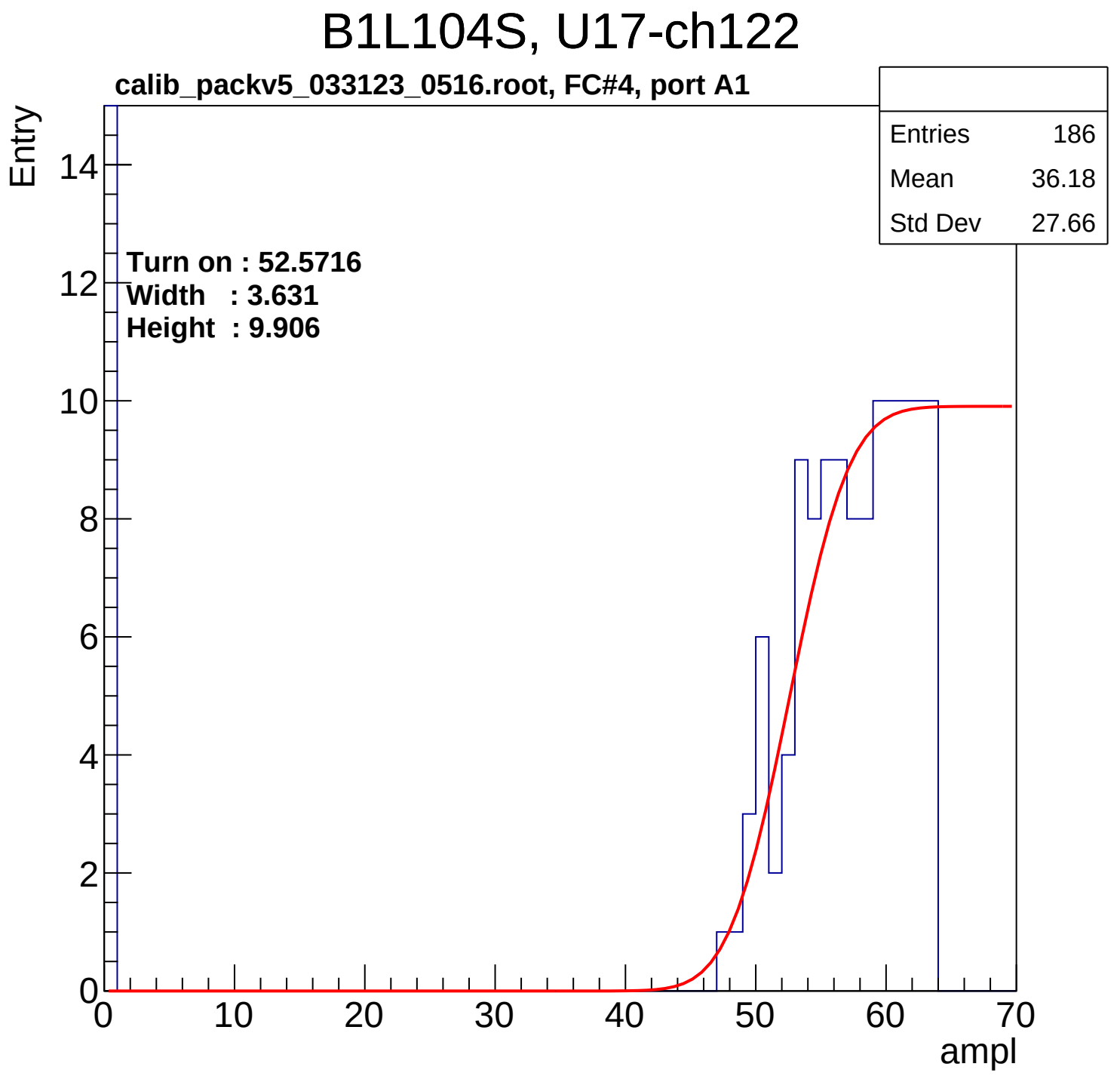
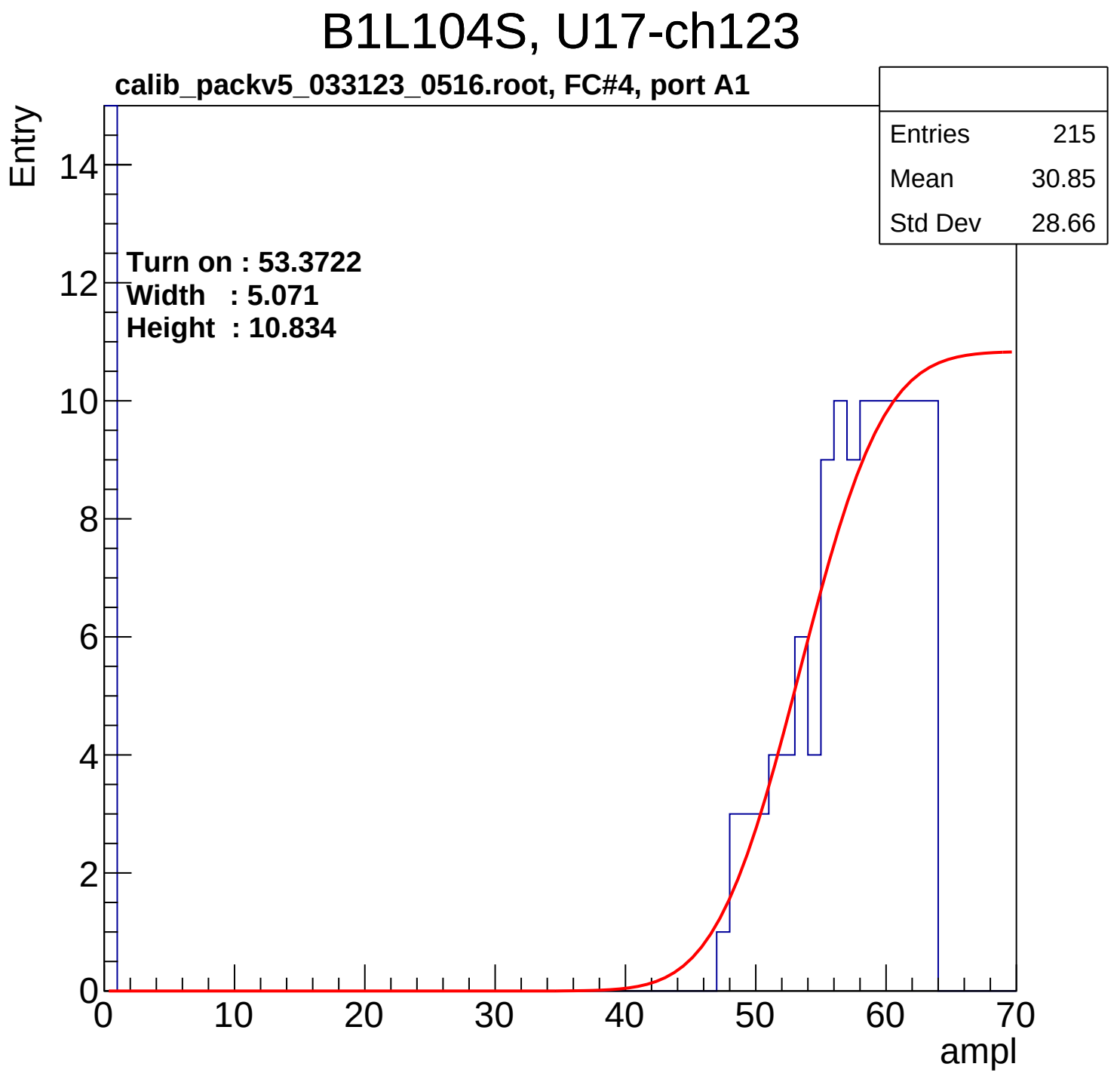
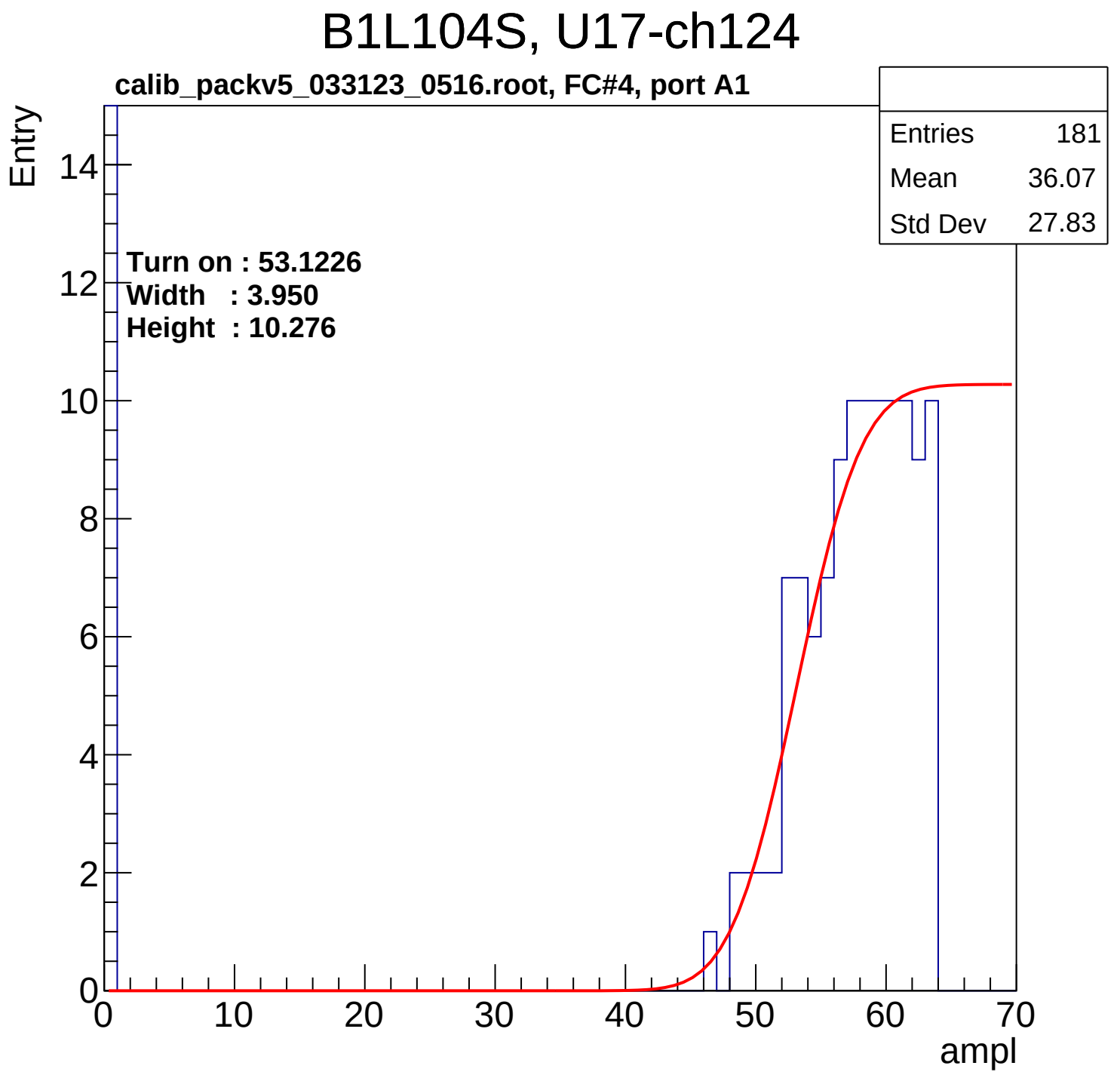
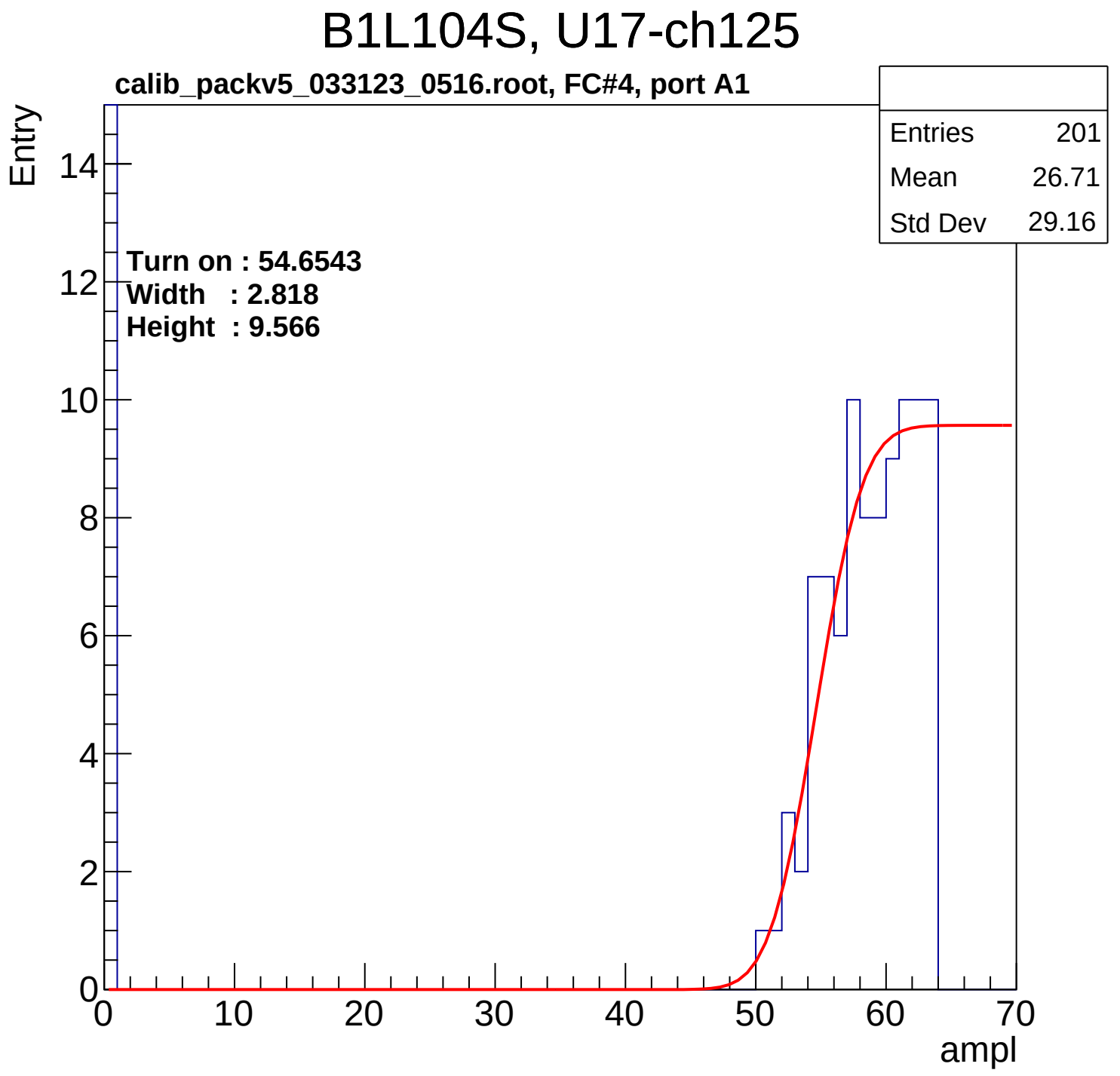
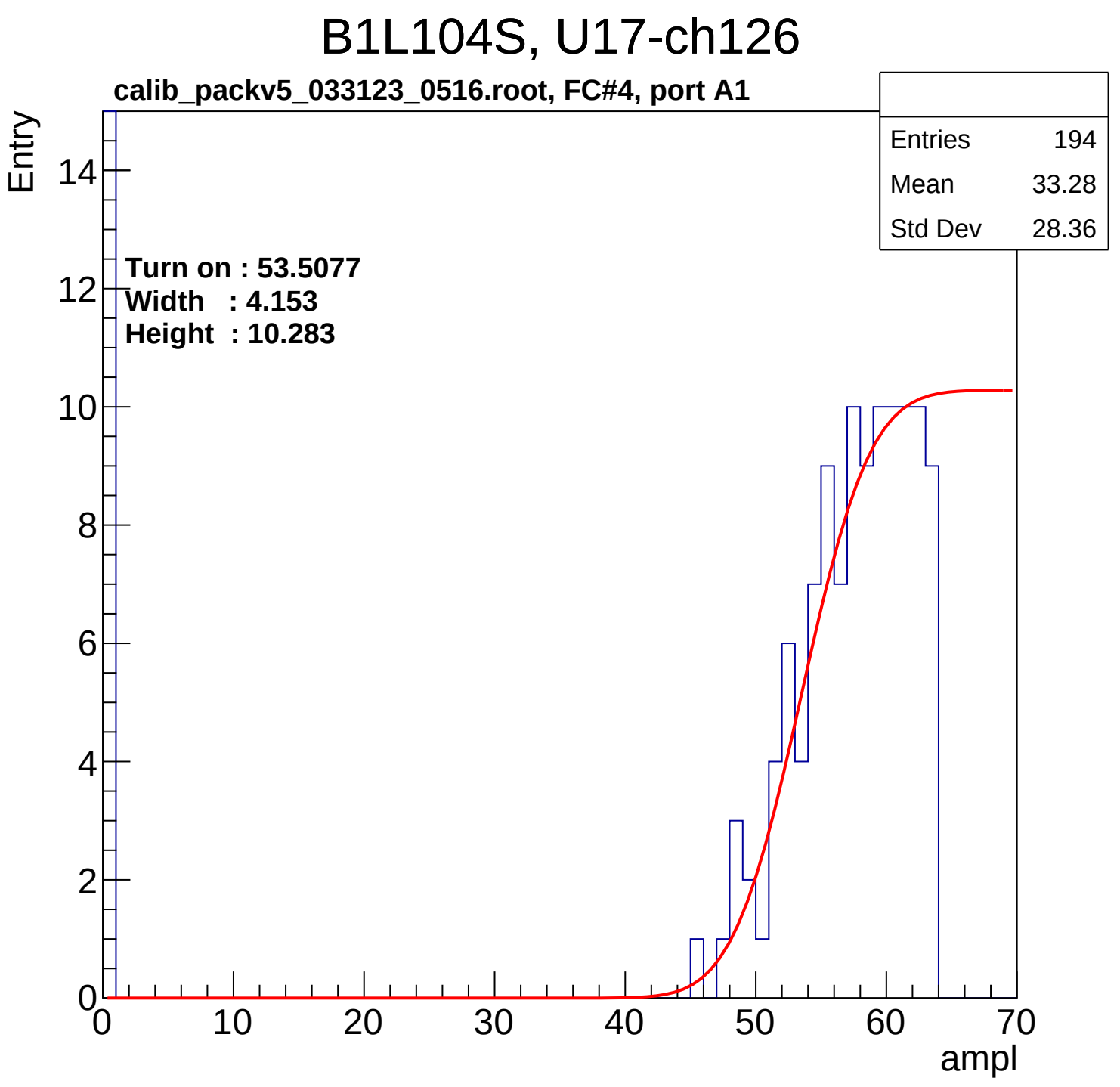

B1L104S, U17-ch121
calib_packv5_033123_0516.root, FC#4, port A1
Entries 183
Mean 29.86
Std Dev 29.18
Turn on : 55.8023
Width : 4.542
Height : 10.778
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U17-ch122
calib_packv5_033123_0516.root, FC#4, port A1
Entries 186
Mean 36.18
Std Dev 27.66
Turn on : 52.5716
Width : 3.631
Height : 9.906
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U17-ch123
calib_packv5_033123_0516.root, FC#4, port A1
Entries 215
Mean 30.85
Std Dev 28.66
Turn on : 53.3722
Width : 5.071
Height : 10.834
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U17-ch124
calib_packv5_033123_0516.root, FC#4, port A1
Entries 181
Mean 36.07
Std Dev 27.83
Turn on : 53.1226
Width : 3.950
Height : 10.276
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U17-ch125
calib_packv5_033123_0516.root, FC#4, port A1
Entries 201
Mean 26.71
Std Dev 29.16
Turn on : 54.6543
Width : 2.818
Height : 9.566
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U17-ch126
calib_packv5_033123_0516.root, FC#4, port A1
Entries 194
Mean 33.28
Std Dev 28.36
Turn on : 53.5077
Width : 4.153
Height : 10.283
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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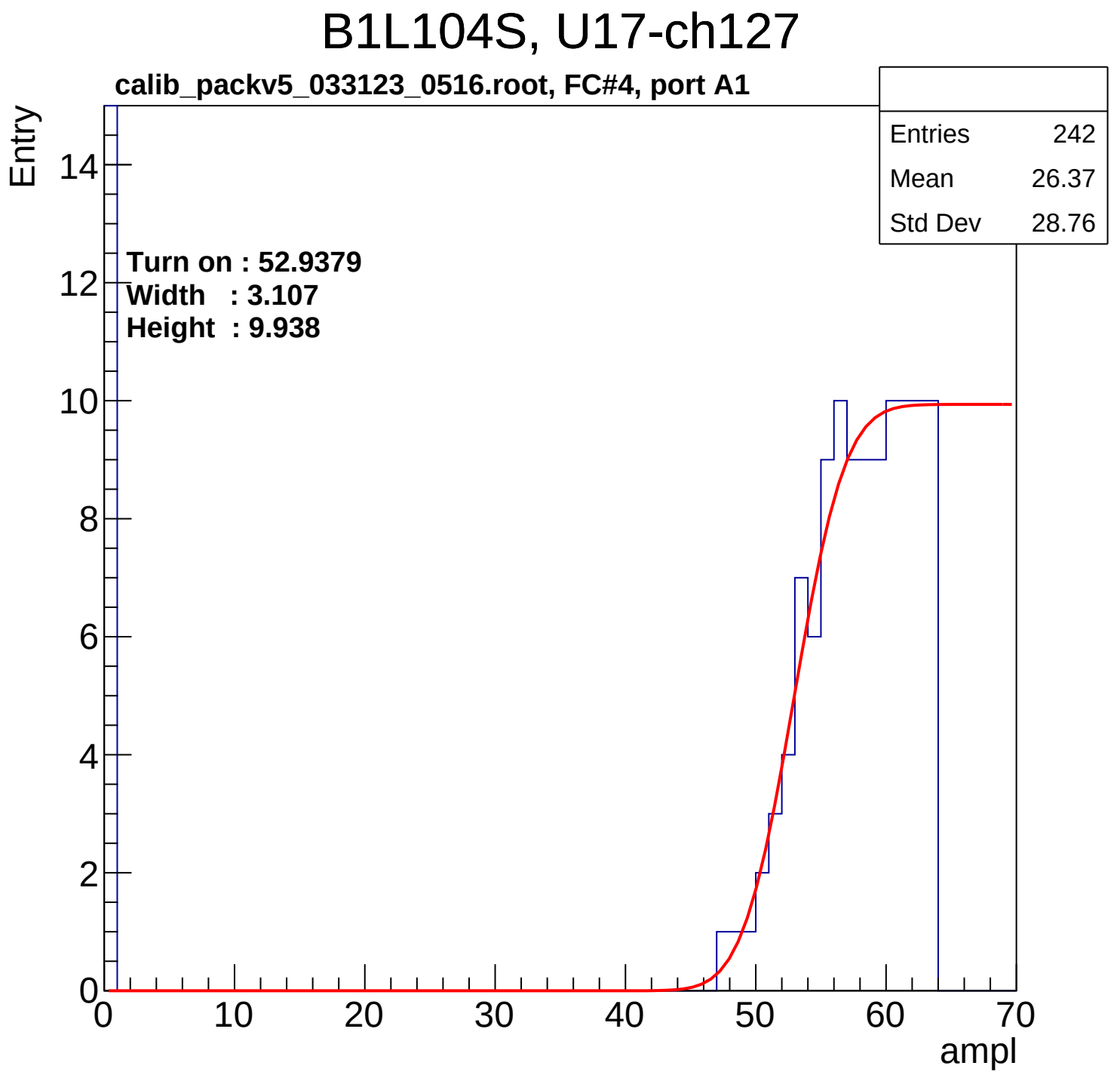
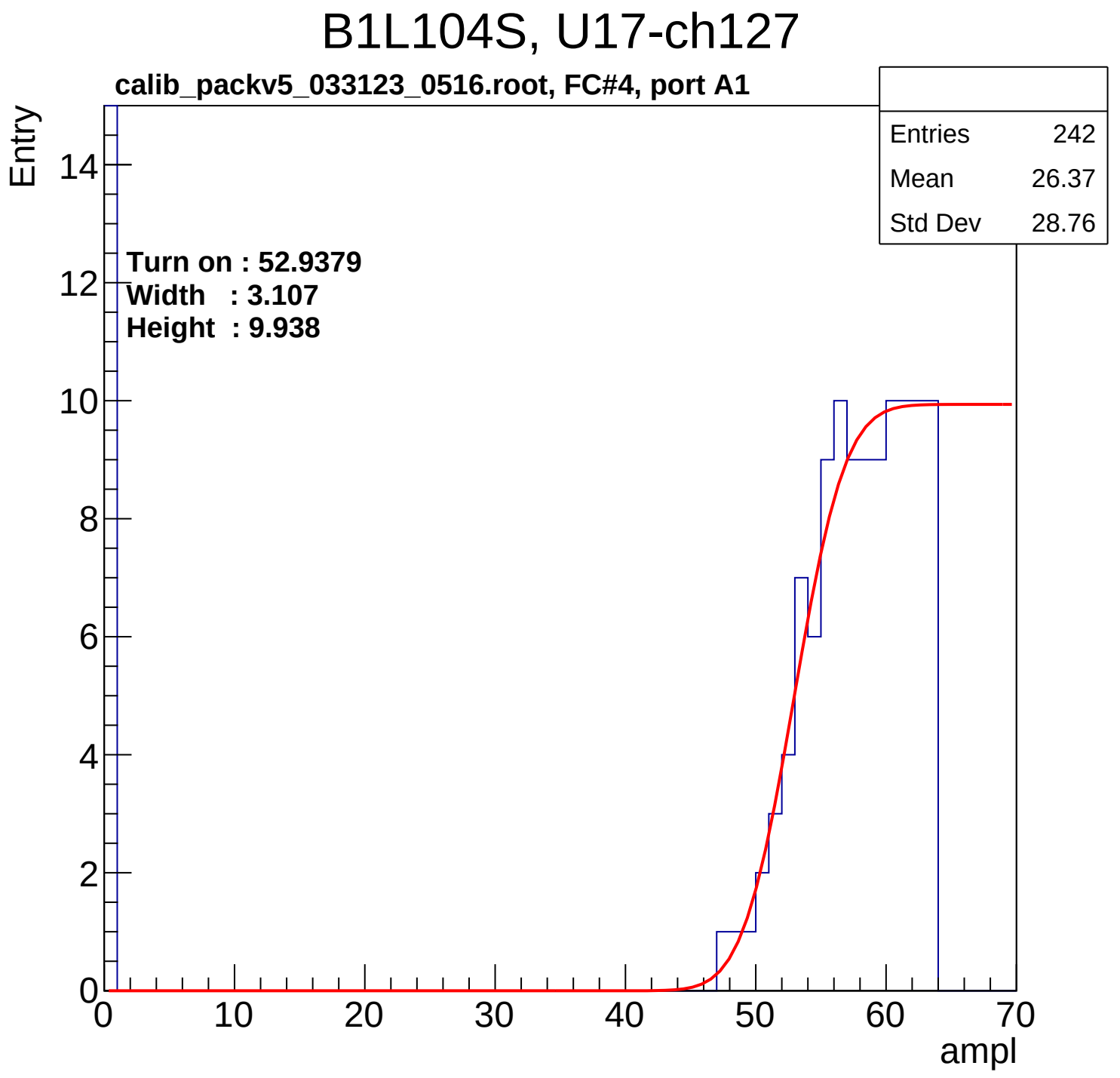

B1L104S, U17-ch127
calib_packv5_033123_0516.root, FC#4, port A1
Entries 242
Mean 26.37
Std Dev 28.76
Turn on : 52.9379
Width : 3.107
Height : 9.938
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U17-ch127
calib_packv5_033123_0516.root, FC#4, port A1
Entries 242
Mean 26.37
Std Dev 28.76
Turn on : 52.9379
Width : 3.107
Height : 9.938
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70