



# B0L101S, U15-ch0

calib\_packv5\_042523\_0143.root, FC#1, port C1

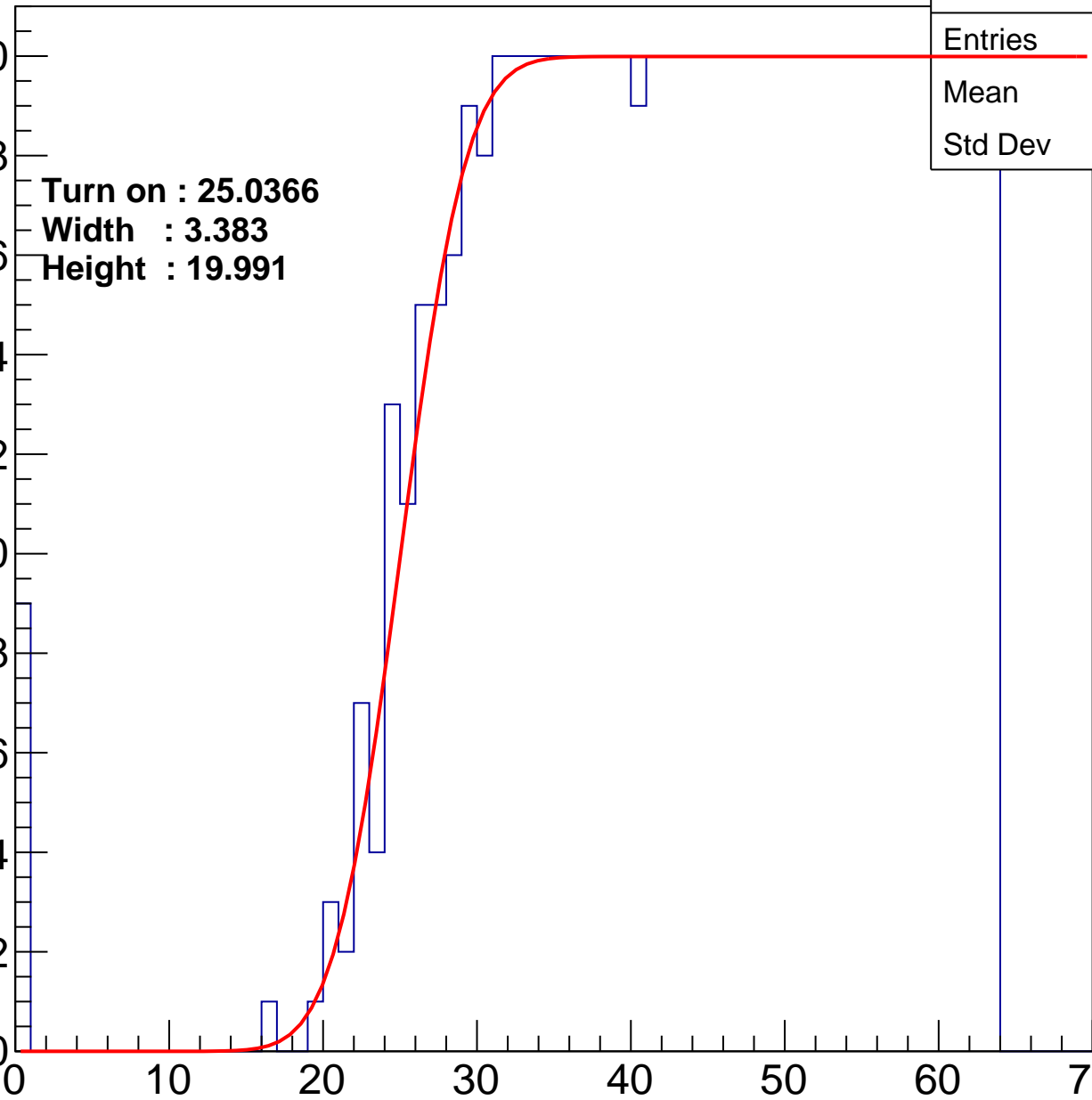
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 25.0366  
Width : 3.383  
Height : 19.991

Entries	793
Mean	43.23
Std Dev	12.42

ampl



# B0L101S, U15-ch1

calib\_packv5\_042523\_0143.root, FC#1, port C1

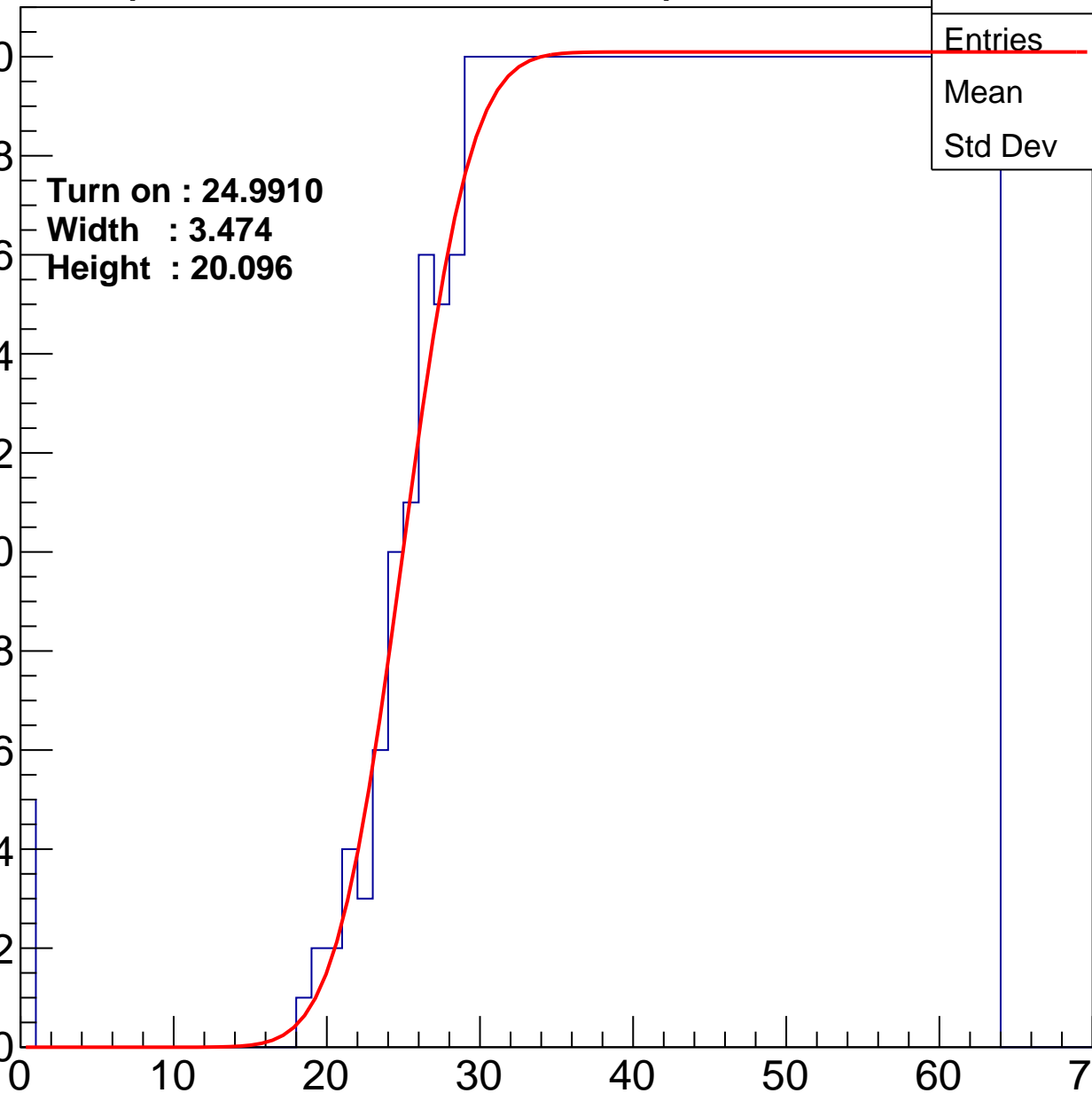
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 24.9910**  
**Width : 3.474**  
**Height : 20.096**

Entries	791
Mean	43.45
Std Dev	12.03

ampl



# B0L101S, U15-ch2

calib\_packv5\_042523\_0143.root, FC#1, port C1

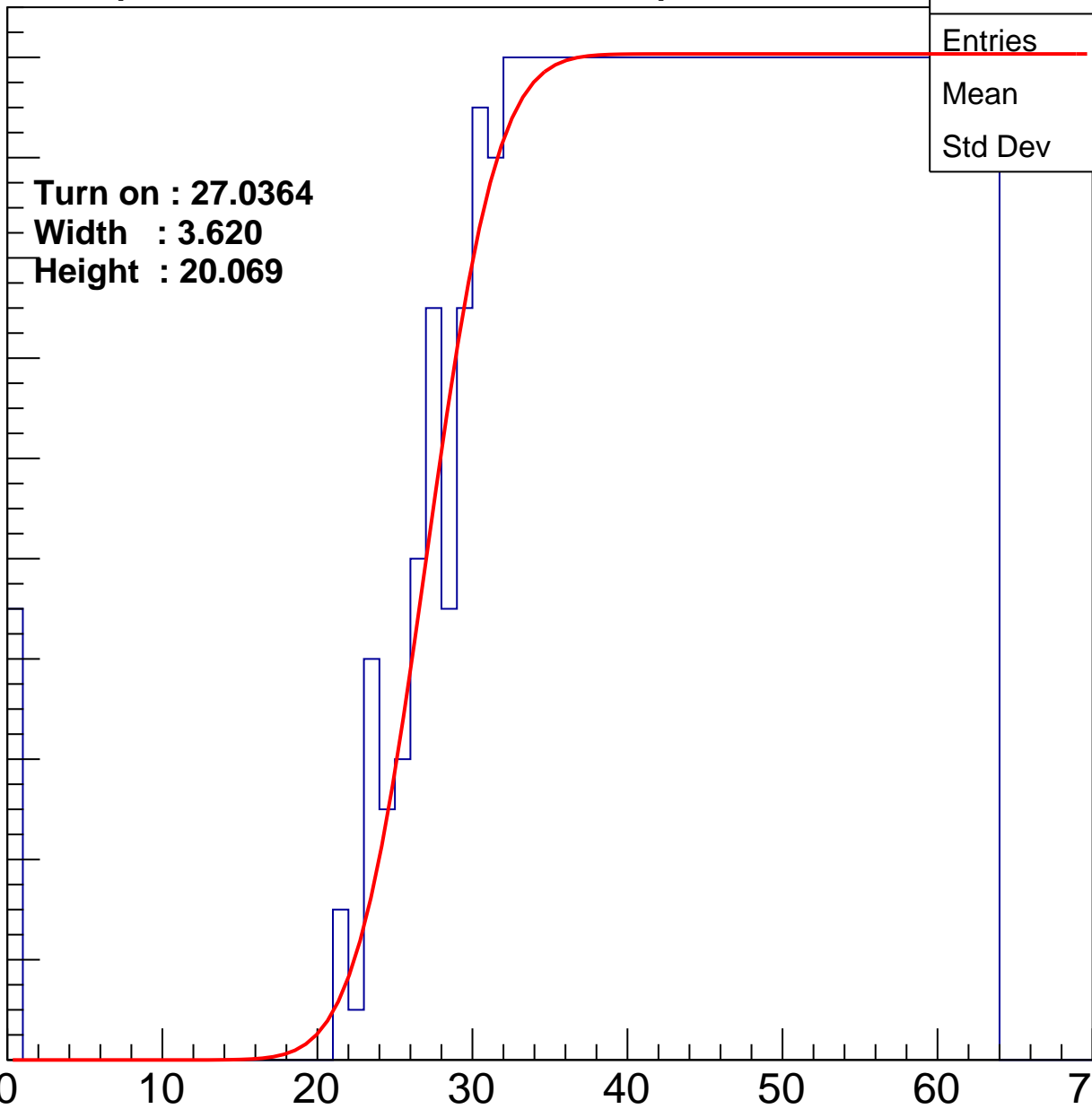
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 27.0364  
Width : 3.620  
Height : 20.069

Entries	758
Mean	44.09
Std Dev	12.02

ampl



# B0L101S, U15-ch3

calib\_packv5\_042523\_0143.root, FC#1, port C1

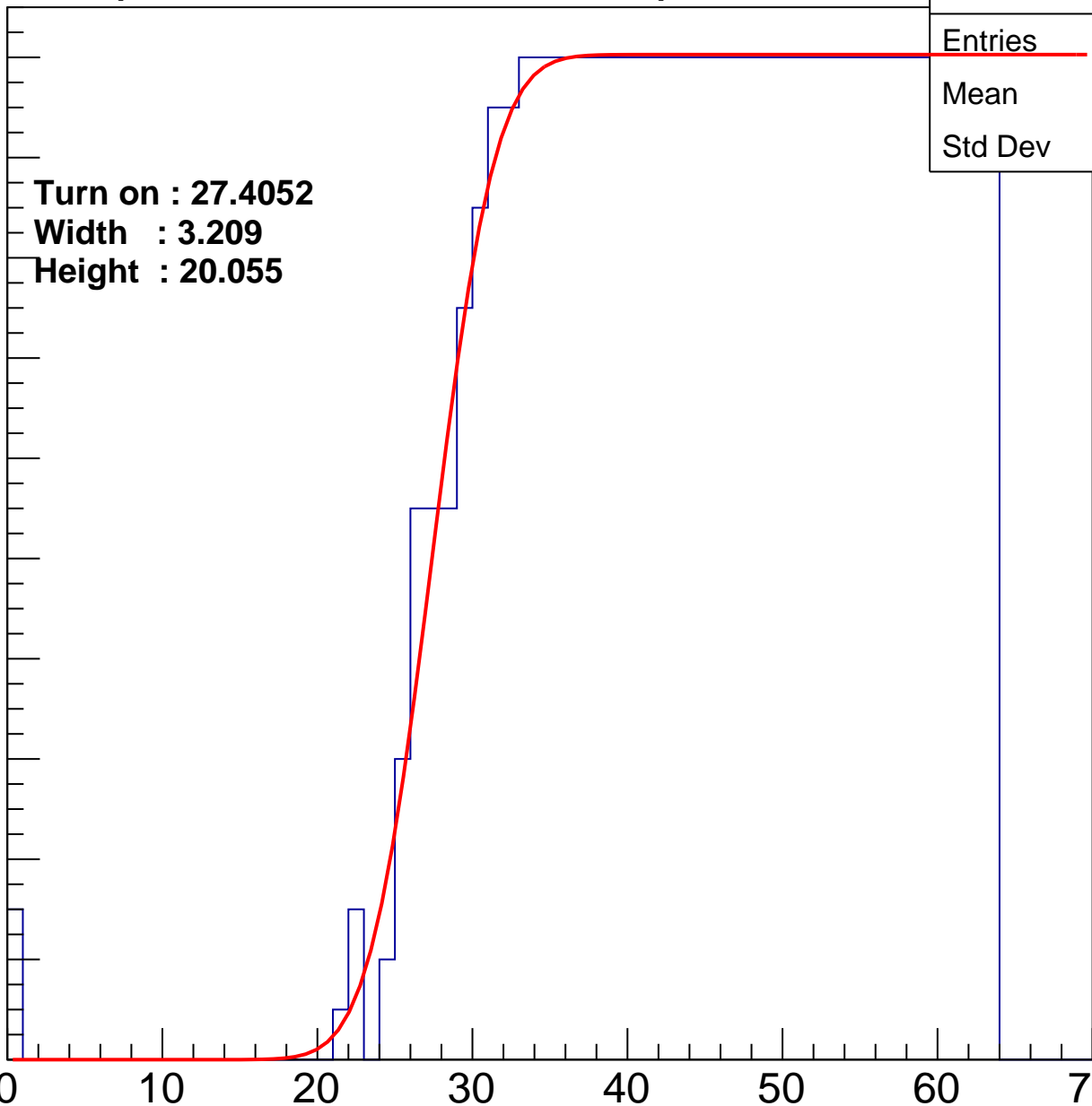
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 27.4052  
Width : 3.209  
Height : 20.055

Entries	738
Mean	44.82
Std Dev	11.16

ampl



# B0L101S, U15-ch4

calib\_packv5\_042523\_0143.root, FC#1, port C1

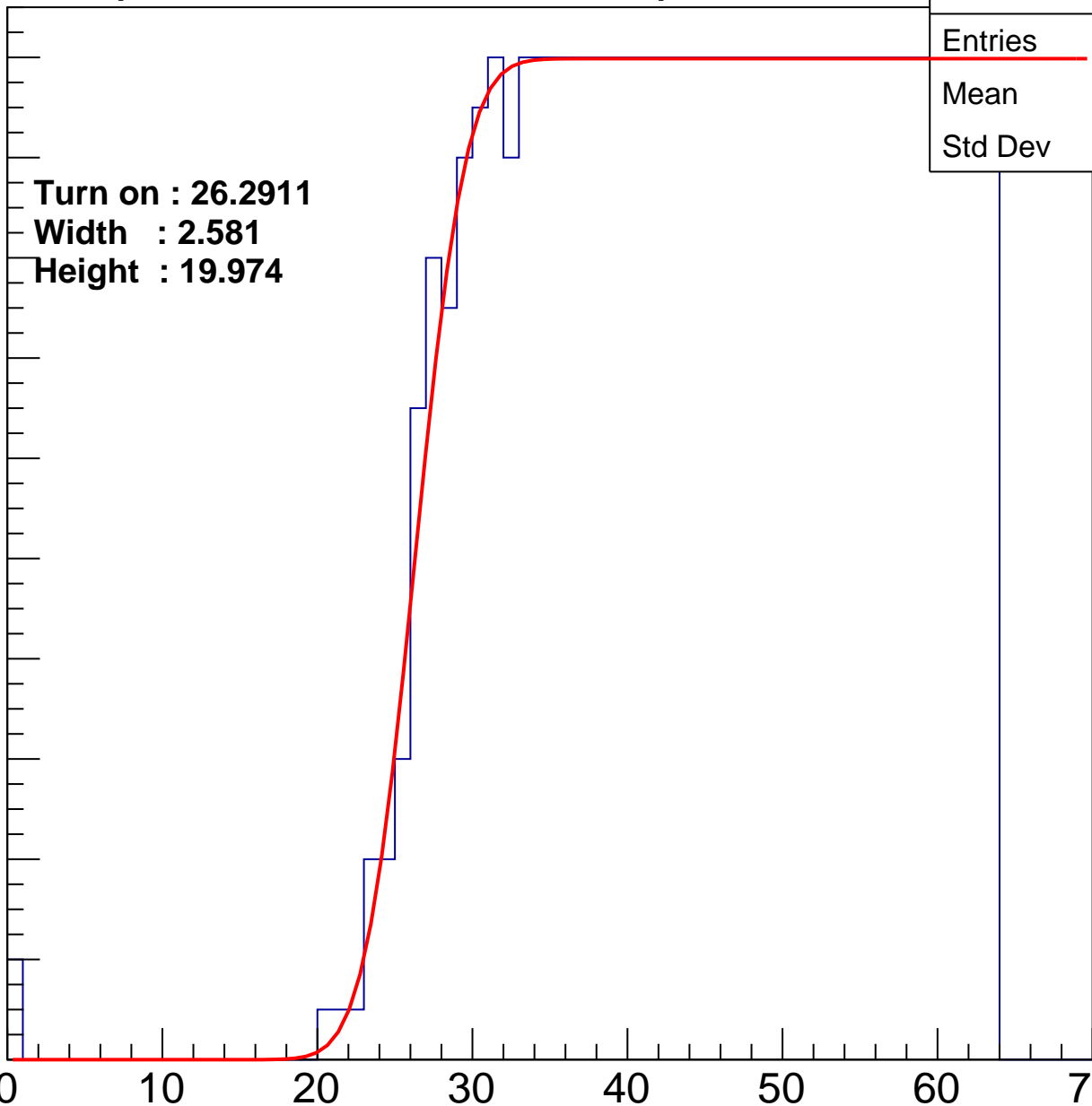
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 26.2911  
Width : 2.581  
Height : 19.974

Entries	758
Mean	44.38
Std Dev	11.3

ampl



# B0L101S, U15-ch5

calib\_packv5\_042523\_0143.root, FC#1, port C1

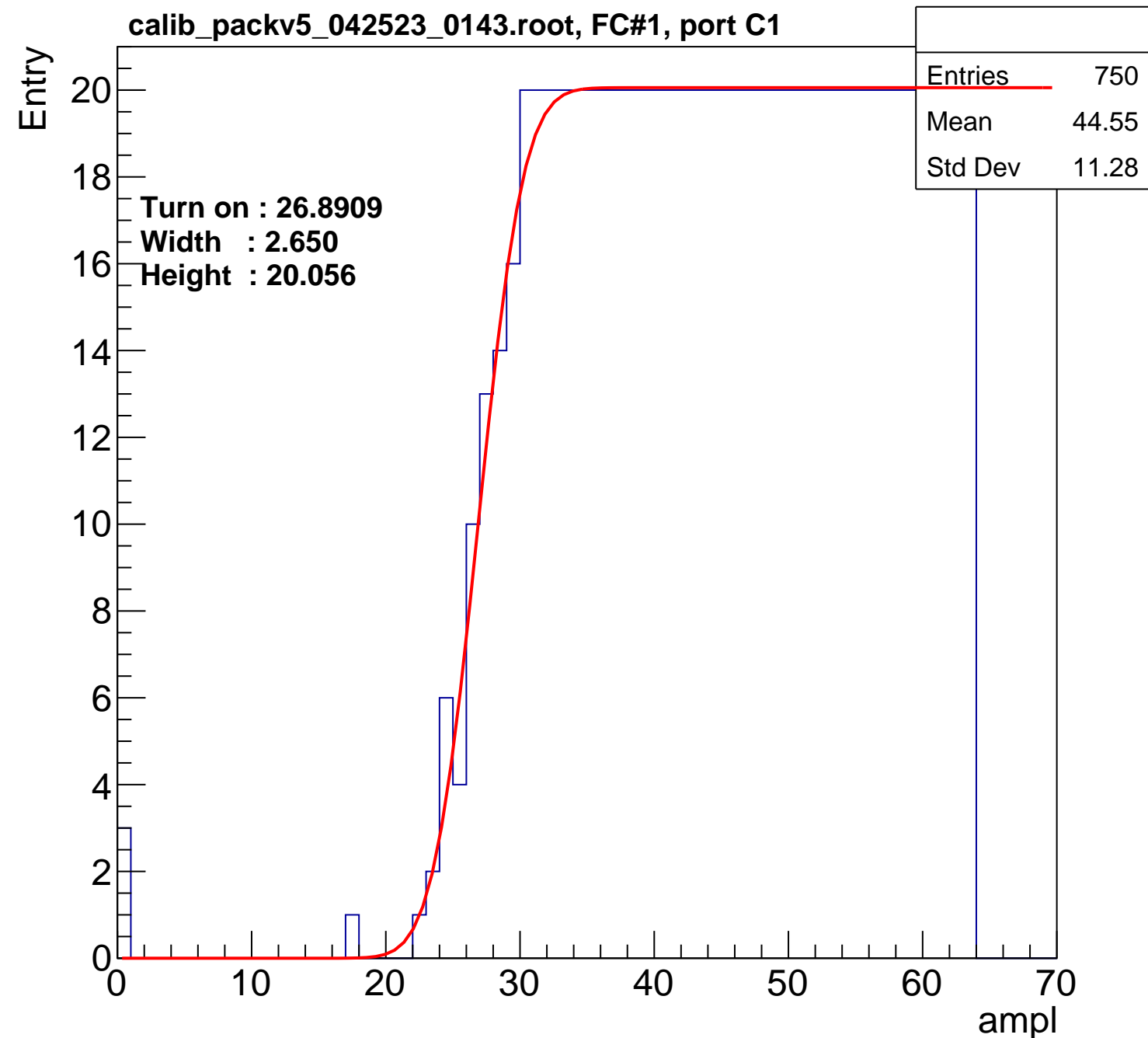
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 26.8909**  
**Width : 2.650**  
**Height : 20.056**

Entries	750
Mean	44.55
Std Dev	11.28

ampl



# B0L101S, U15-ch6

calib\_packv5\_042523\_0143.root, FC#1, port C1

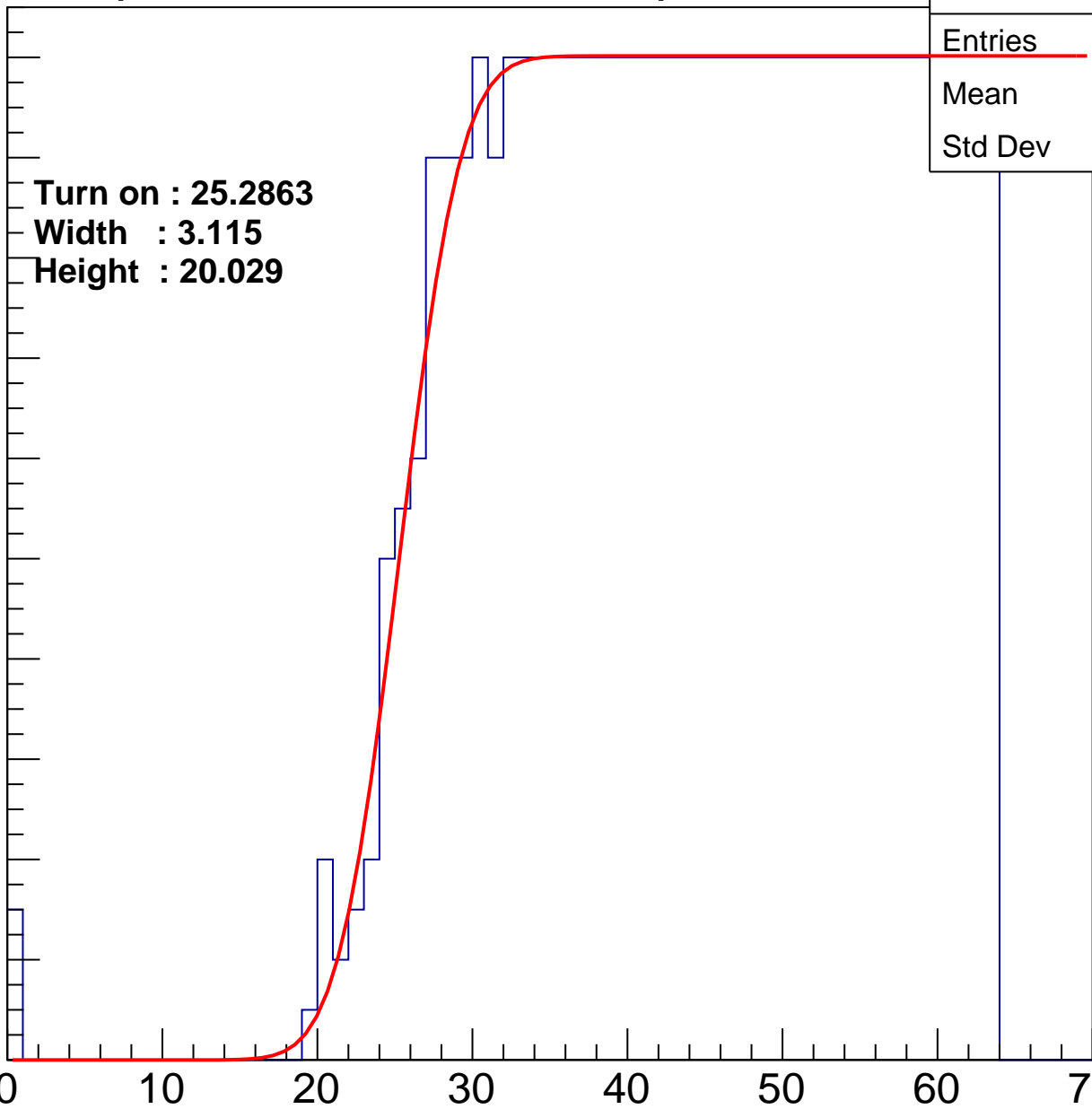
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 25.2863**  
**Width : 3.115**  
**Height : 20.029**

Entries	782
Mean	43.73
Std Dev	11.75

ampl





# B0L101S, U15-ch7

calib\_packv5\_042523\_0143.root, FC#1, port C1

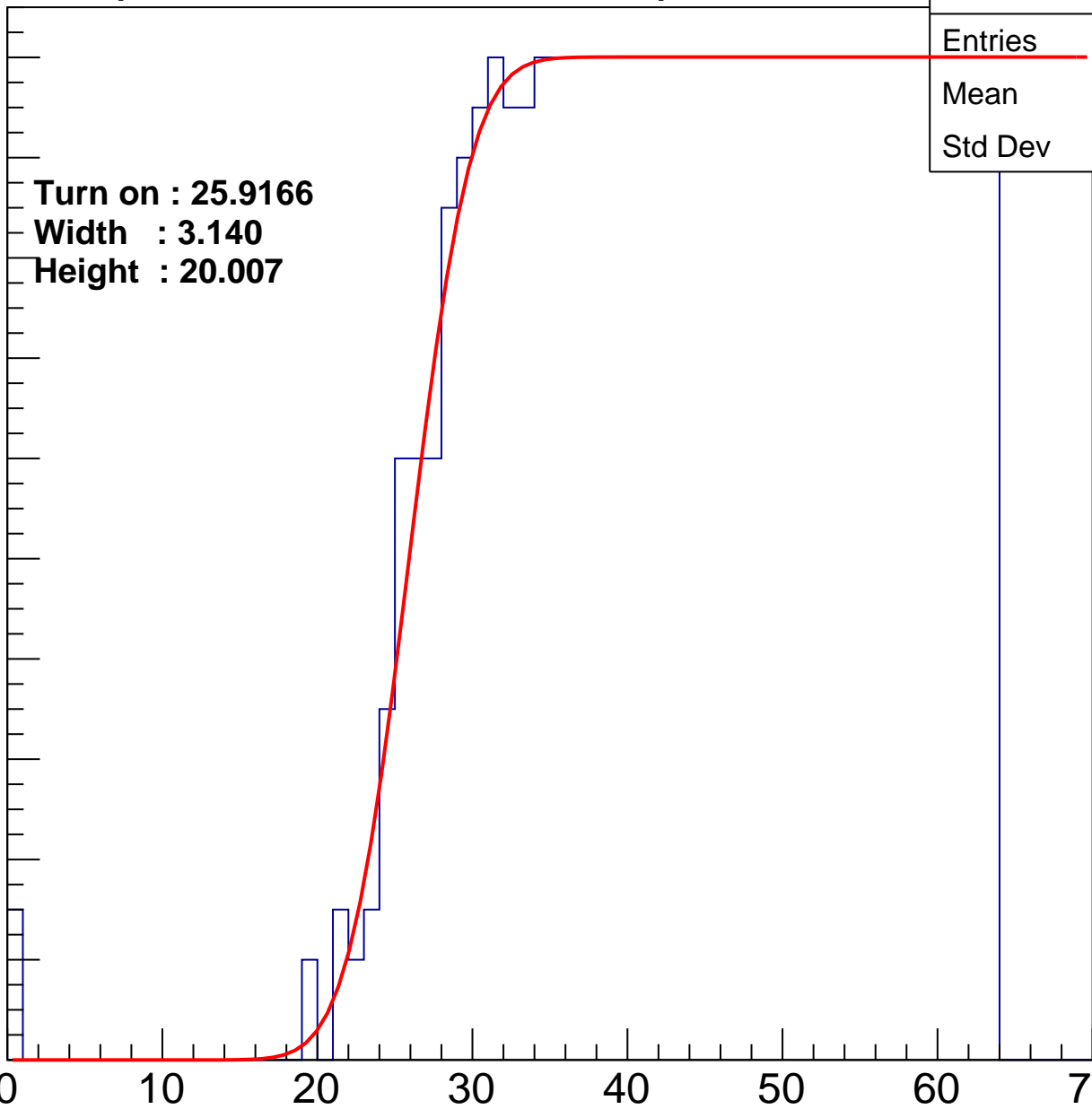
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 25.9166**  
**Width : 3.140**  
**Height : 20.007**

Entries	768
Mean	44.06
Std Dev	11.58

ampl



# B0L101S, U15-ch8

calib\_packv5\_042523\_0143.root, FC#1, port C1

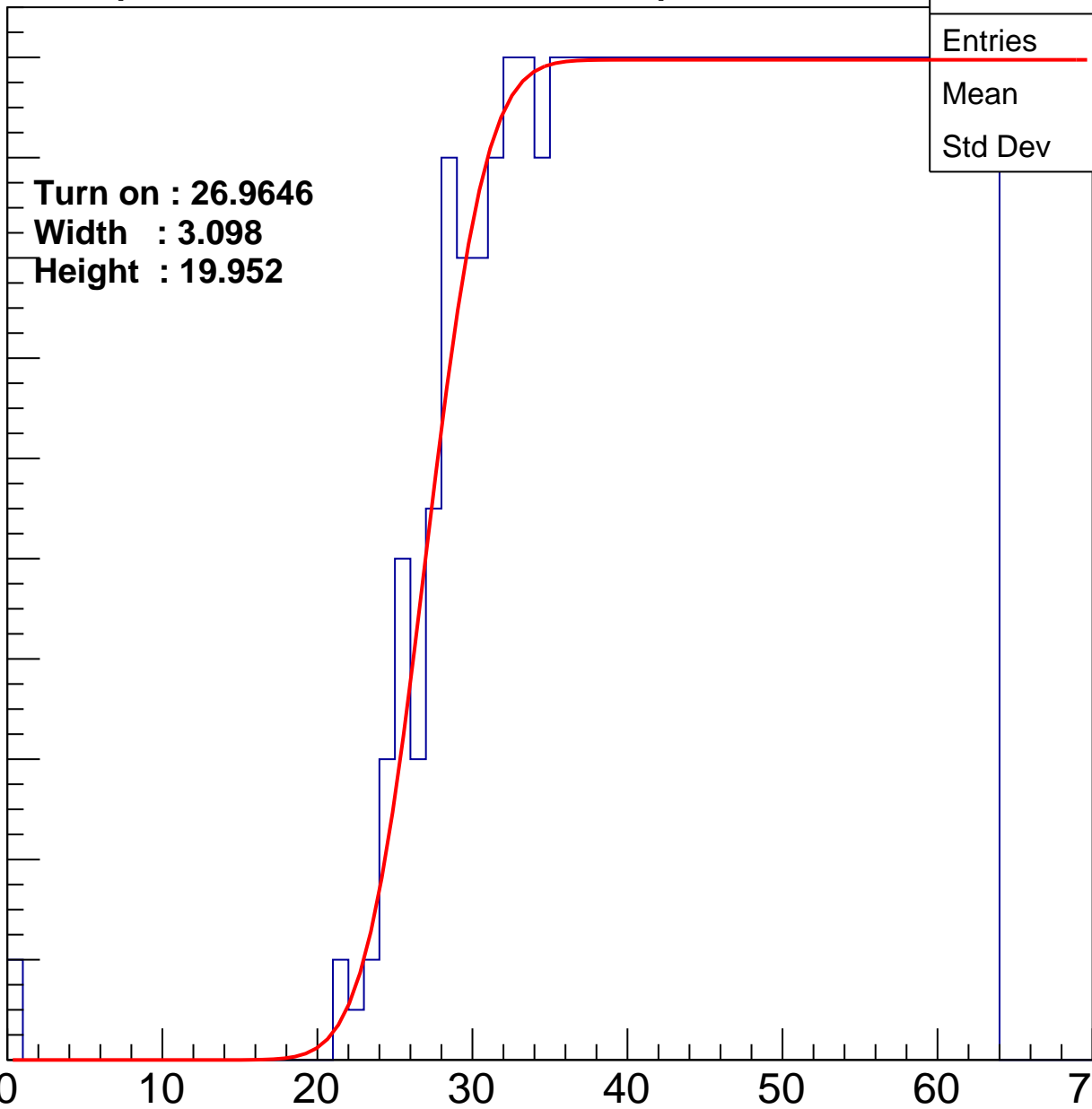
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 26.9646  
Width : 3.098  
Height : 19.952

Entries	746
Mean	44.63
Std Dev	11.21

ampl



# B0L101S, U15-ch9

calib\_packv5\_042523\_0143.root, FC#1, port C1

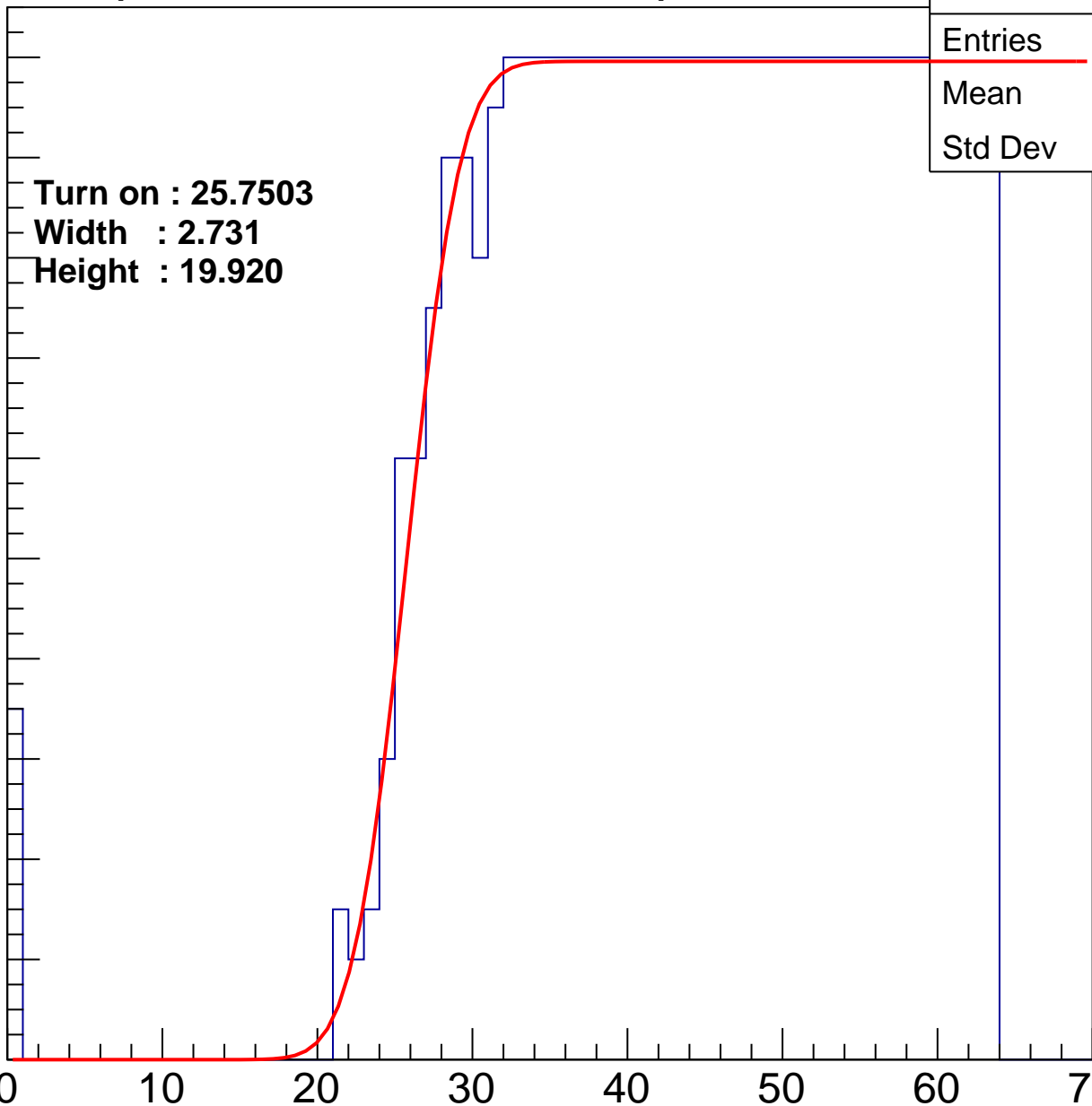
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 25.7503  
Width : 2.731  
Height : 19.920

Entries	771
Mean	43.88
Std Dev	11.93

ampl



# B0L101S, U15-ch10

calib\_packv5\_042523\_0143.root, FC#1, port C1

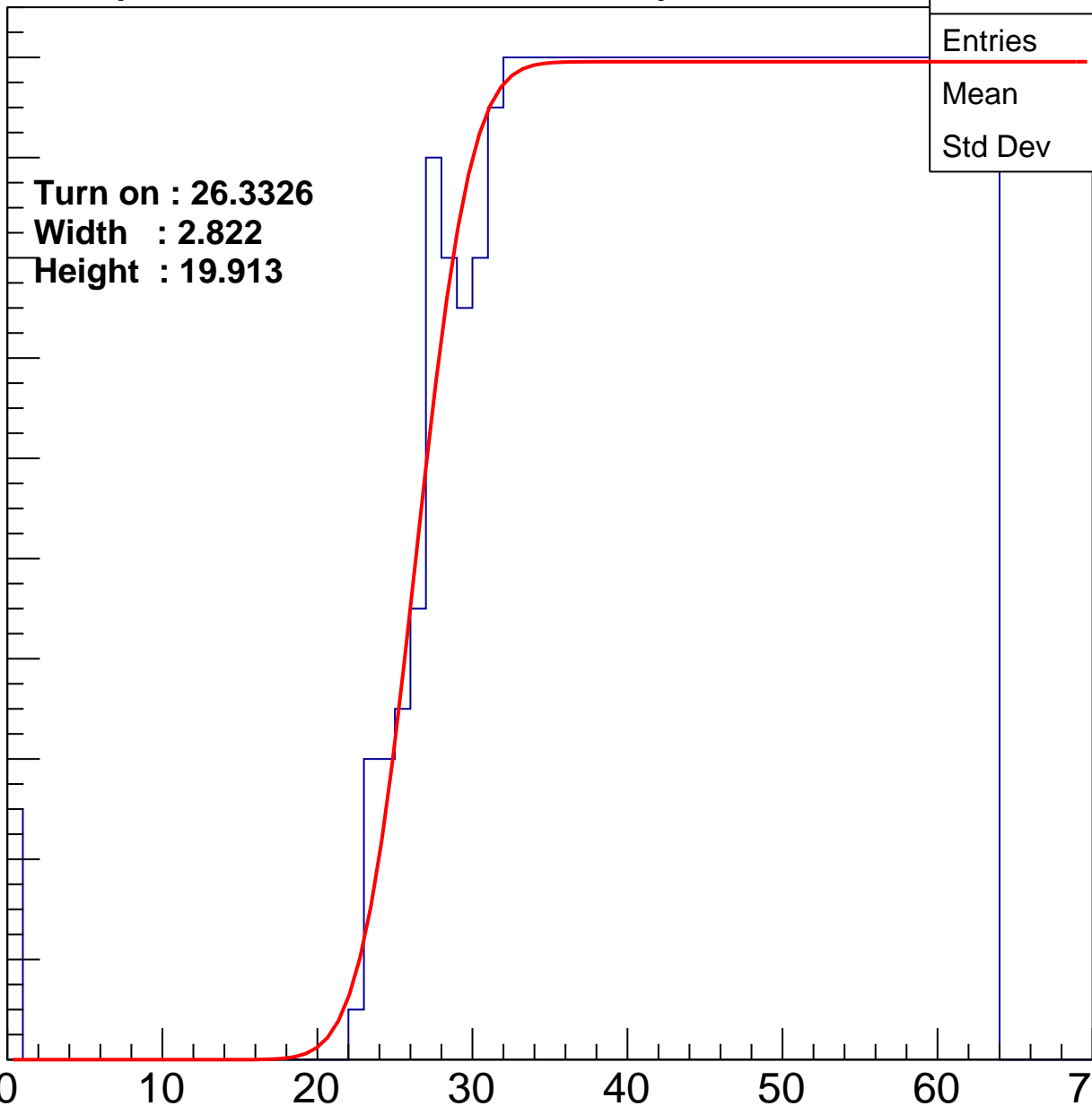
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 26.3326  
Width : 2.822  
Height : 19.913

Entries	758
Mean	44.26
Std Dev	11.6

ampl



# B0L101S, U15-ch11

calib\_packv5\_042523\_0143.root, FC#1, port C1

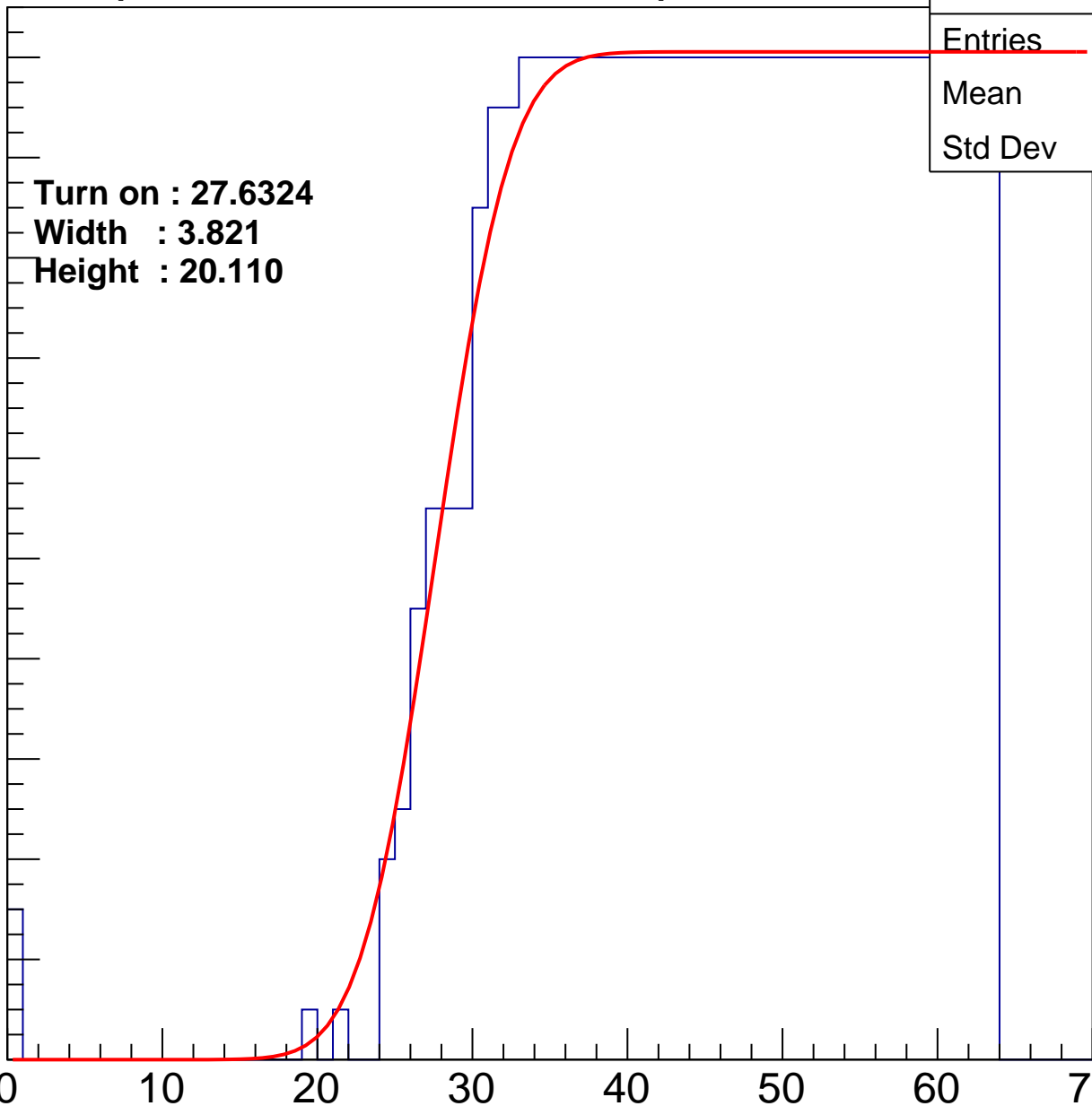
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 27.6324**  
**Width : 3.821**  
**Height : 20.110**

Entries	731
Mean	44.99
Std Dev	11.09

ampl



# B0L101S, U15-ch12

calib\_packv5\_042523\_0143.root, FC#1, port C1

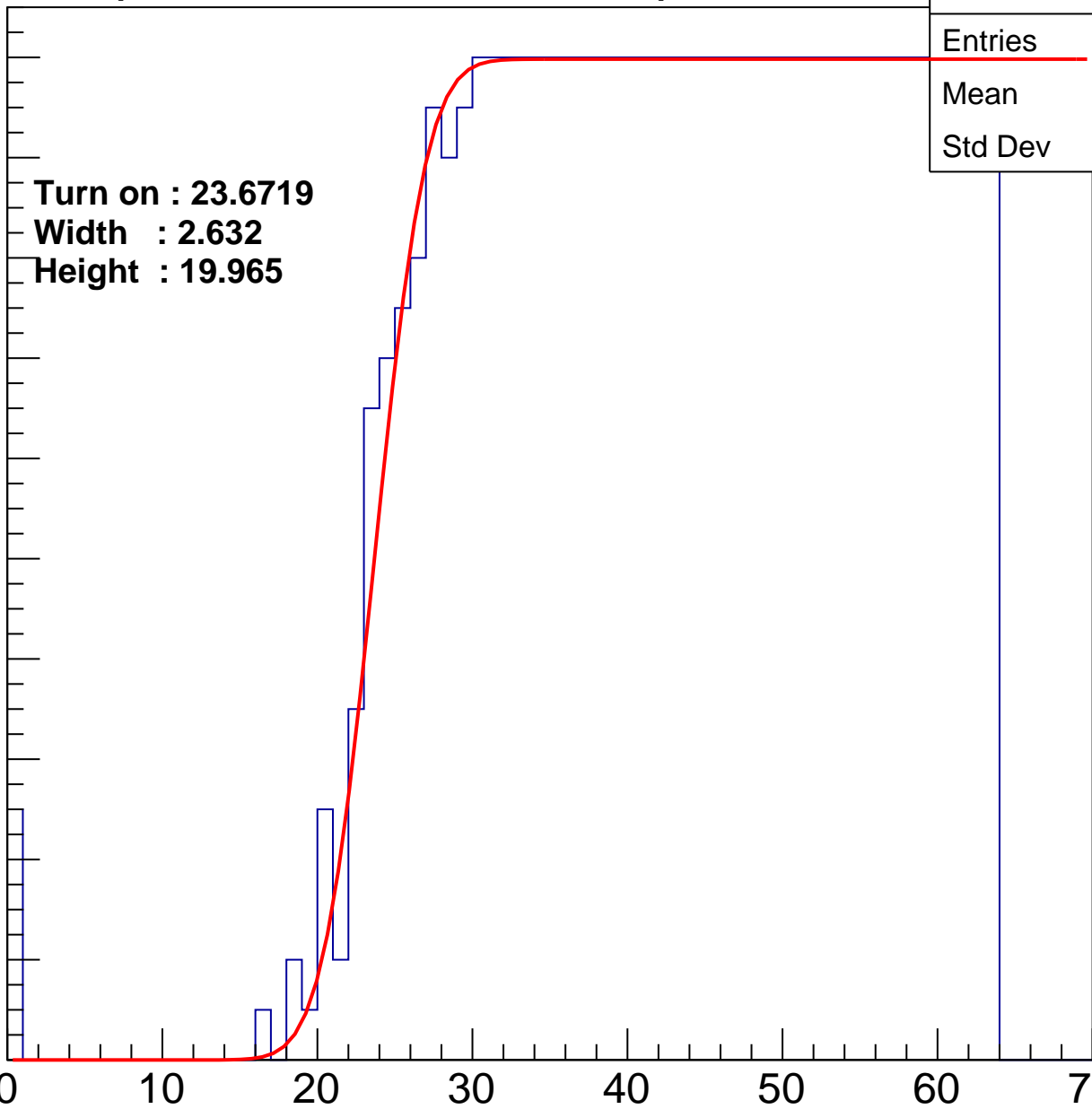
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 23.6719**  
**Width : 2.632**  
**Height : 19.965**

Entries	817
Mean	42.82
Std Dev	12.35

ampl



# B0L101S, U15-ch13

calib\_packv5\_042523\_0143.root, FC#1, port C1

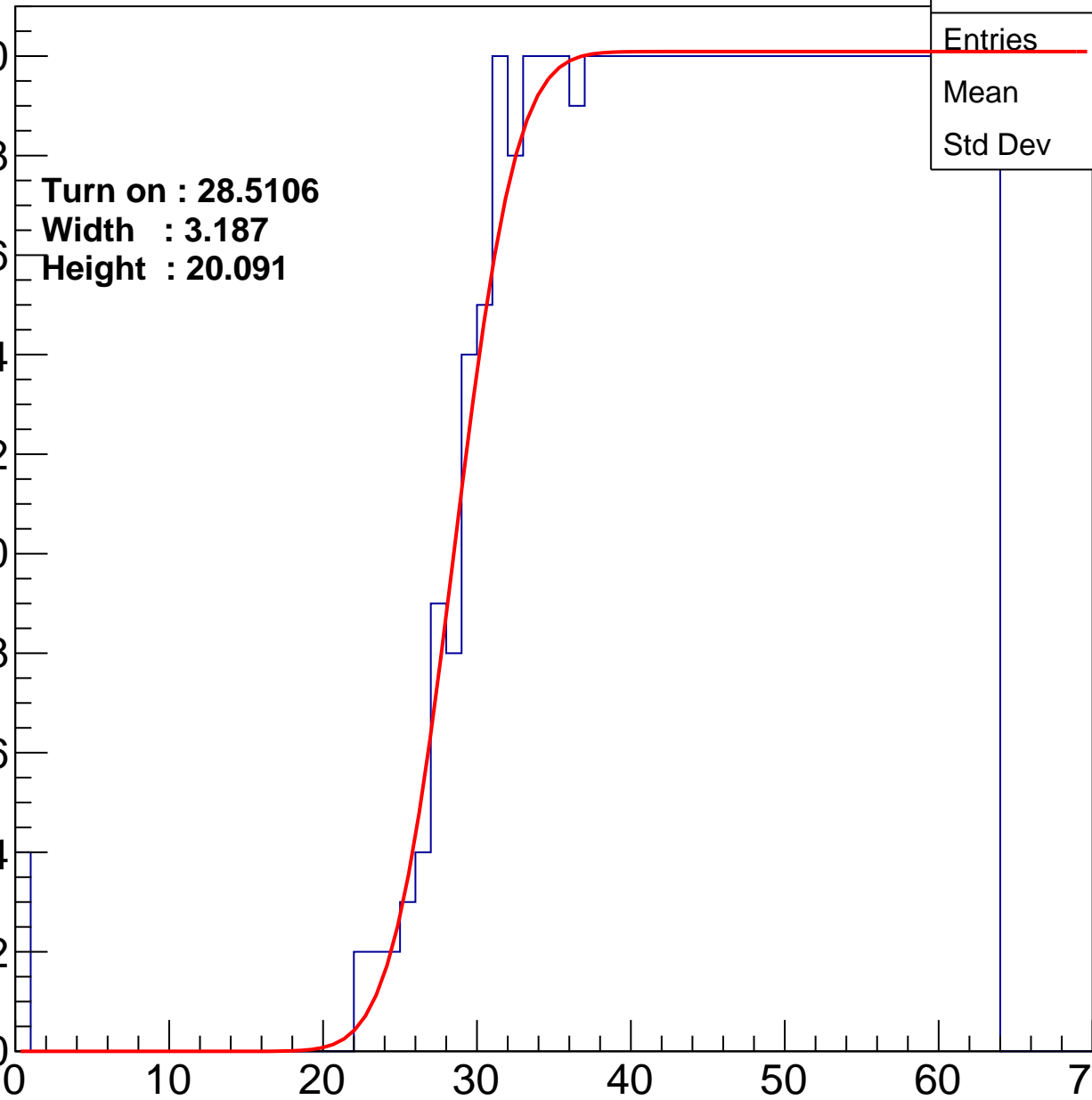
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 28.5106**  
**Width : 3.187**  
**Height : 20.091**

Entries	720
Mean	45.22
Std Dev	11.05

ampl



# B0L101S, U15-ch14

calib\_packv5\_042523\_0143.root, FC#1, port C1

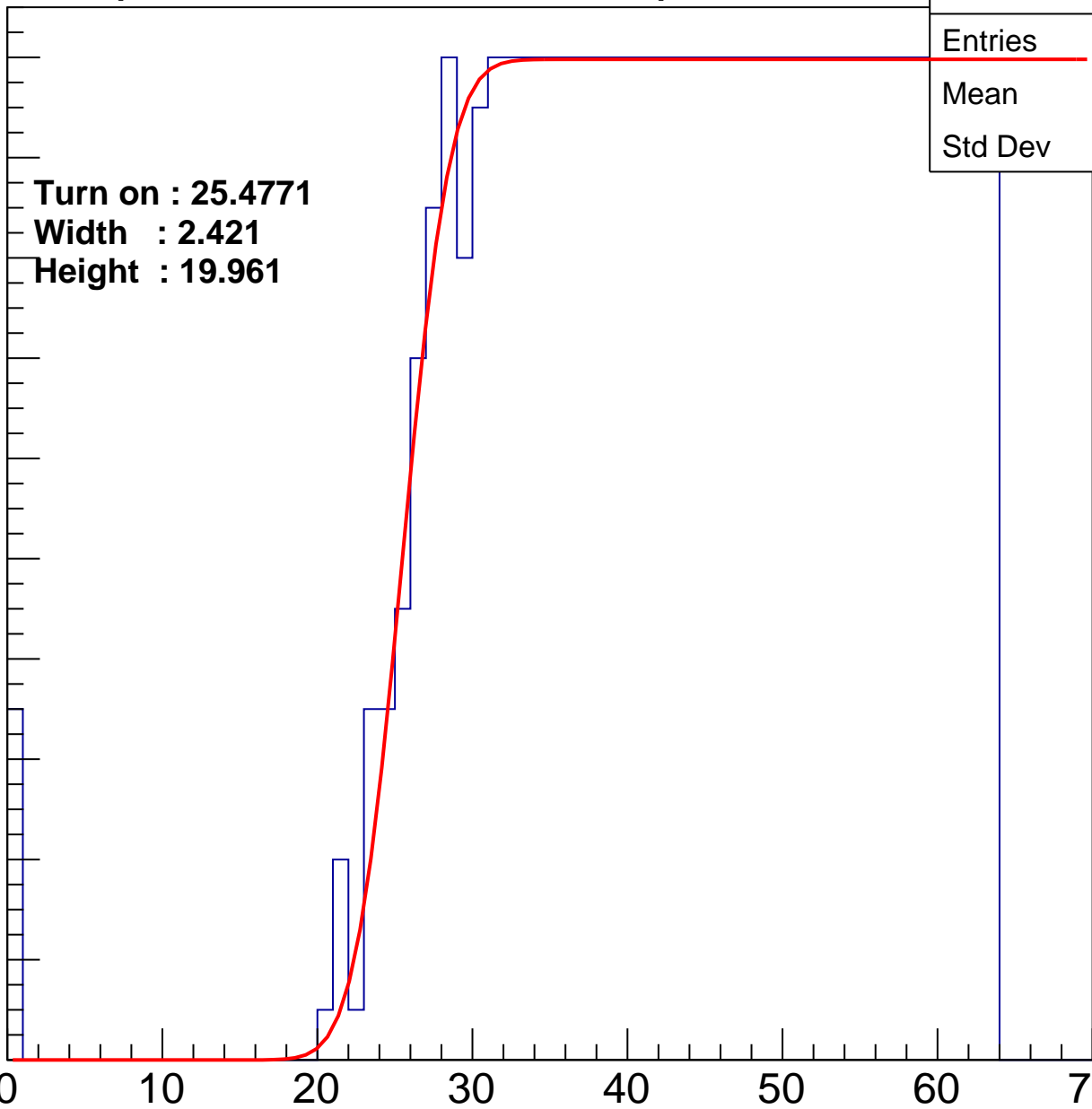
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 25.4771  
Width : 2.421  
Height : 19.961

Entries	782
Mean	43.63
Std Dev	12.04

ampl





# B0L101S, U15-ch15

calib\_packv5\_042523\_0143.root, FC#1, port C1

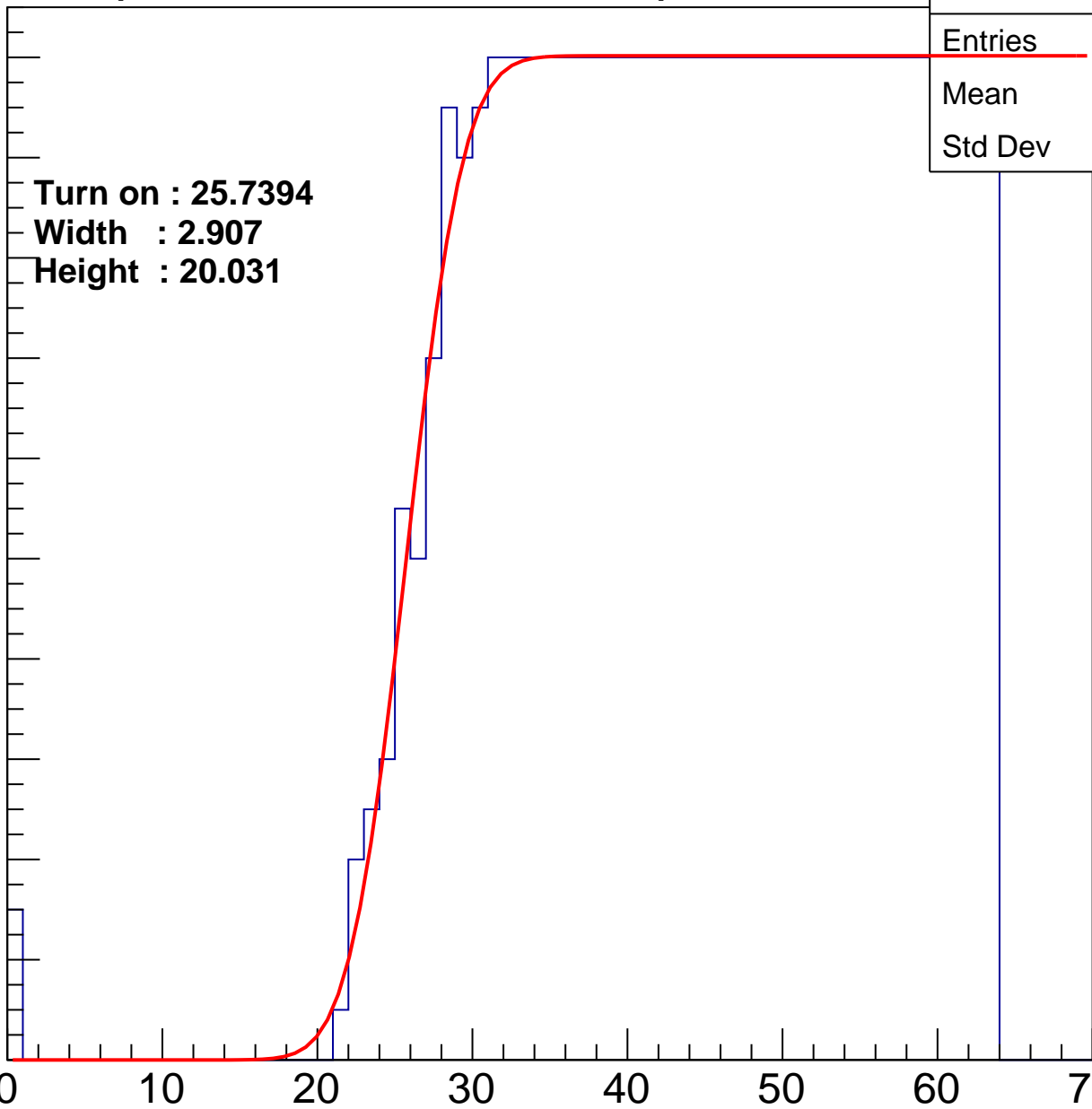
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 25.7394  
Width : 2.907  
Height : 20.031

Entries	770
Mean	44.06
Std Dev	11.54

ampl



# B0L101S, U15-ch16

calib\_packv5\_042523\_0143.root, FC#1, port C1

Entry

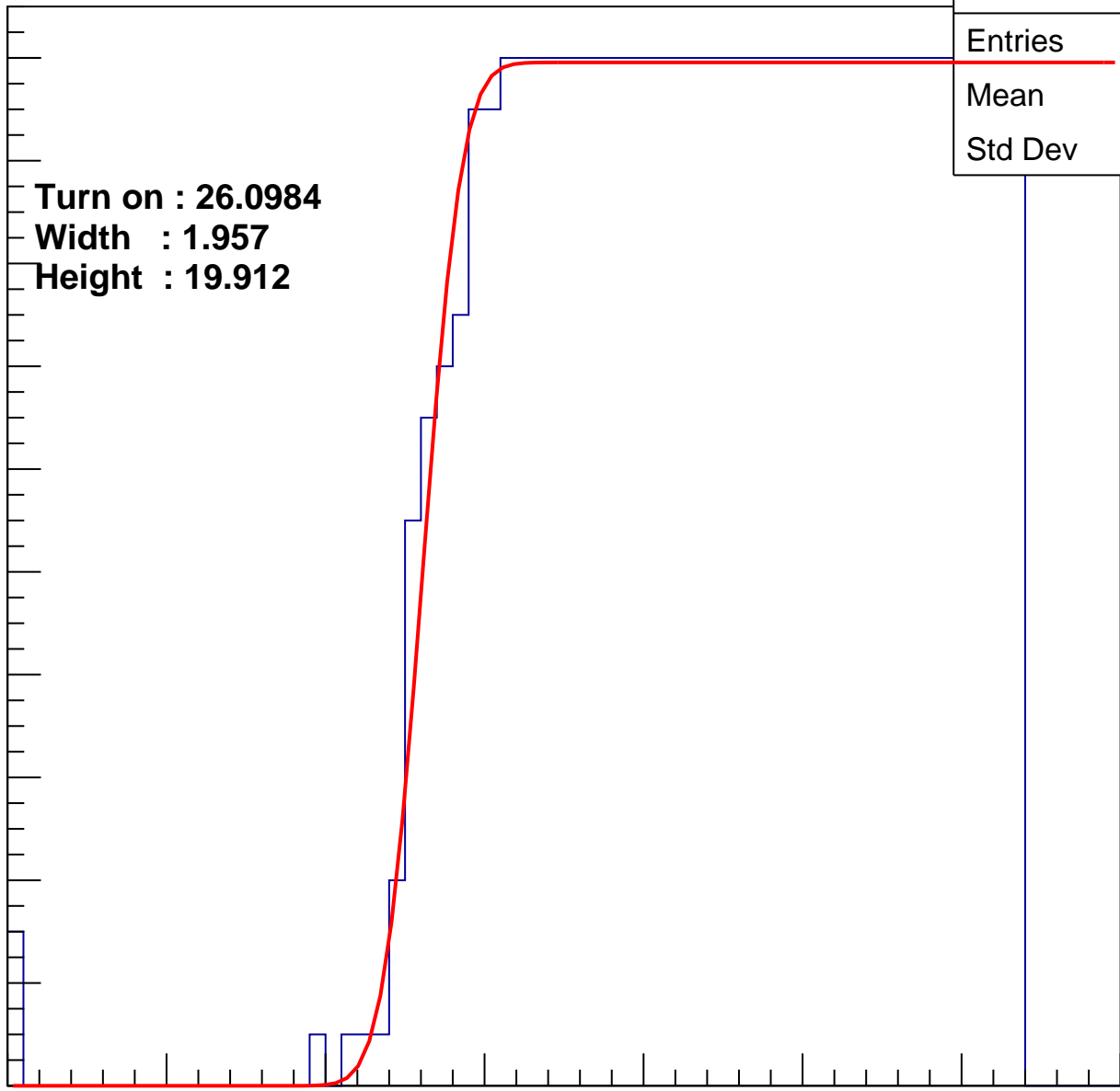
20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 26.0984**  
**Width : 1.957**  
**Height : 19.912**

Entries	762
Mean	44.27
Std Dev	11.41

ampl

0 10 20 30 40 50 60 70



# B0L101S, U15-ch17

calib\_packv5\_042523\_0143.root, FC#1, port C1

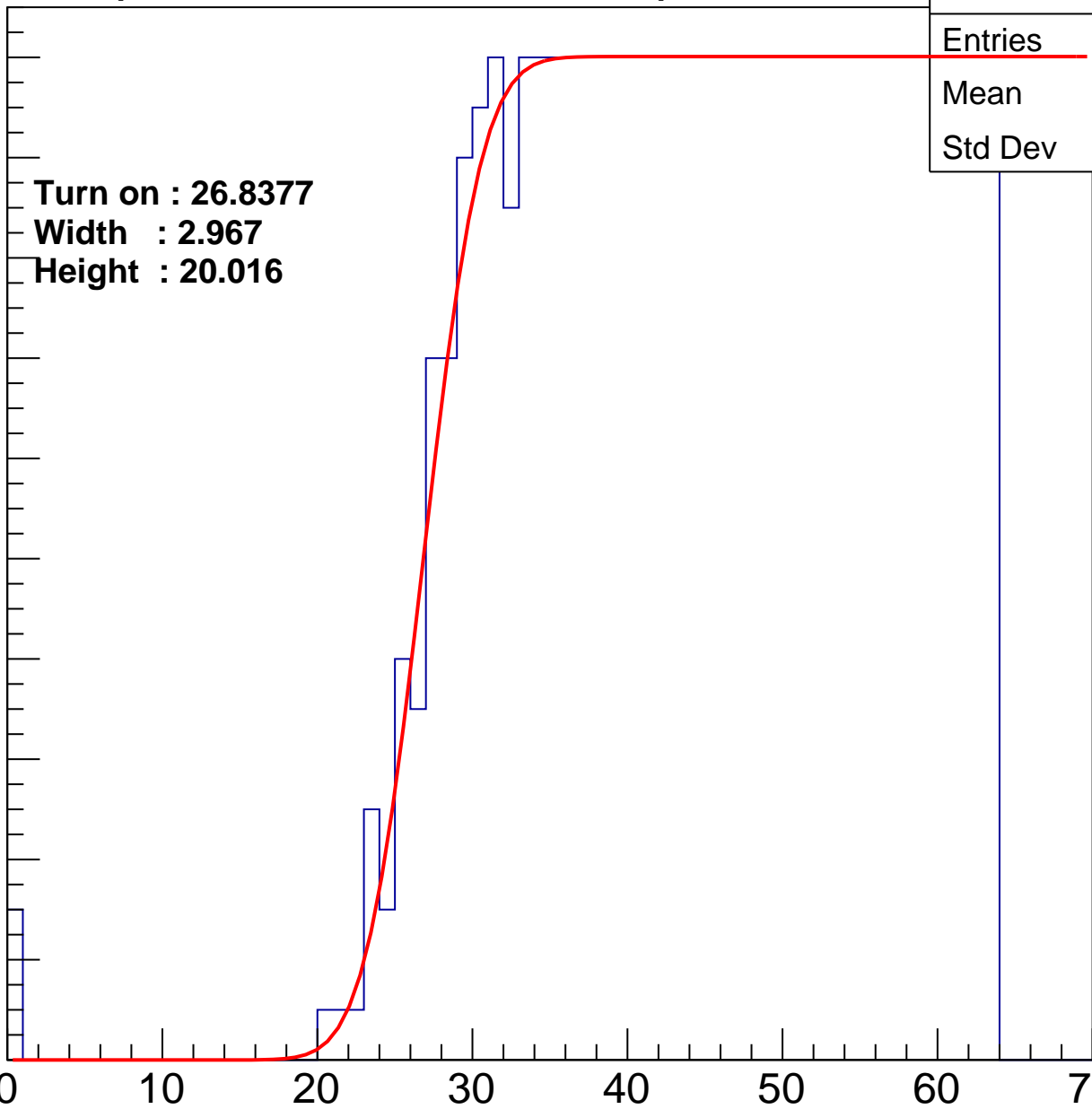
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 26.8377**  
**Width : 2.967**  
**Height : 20.016**

Entries	751
Mean	44.5
Std Dev	11.34

ampl



# B0L101S, U15-ch18

calib\_packv5\_042523\_0143.root, FC#1, port C1

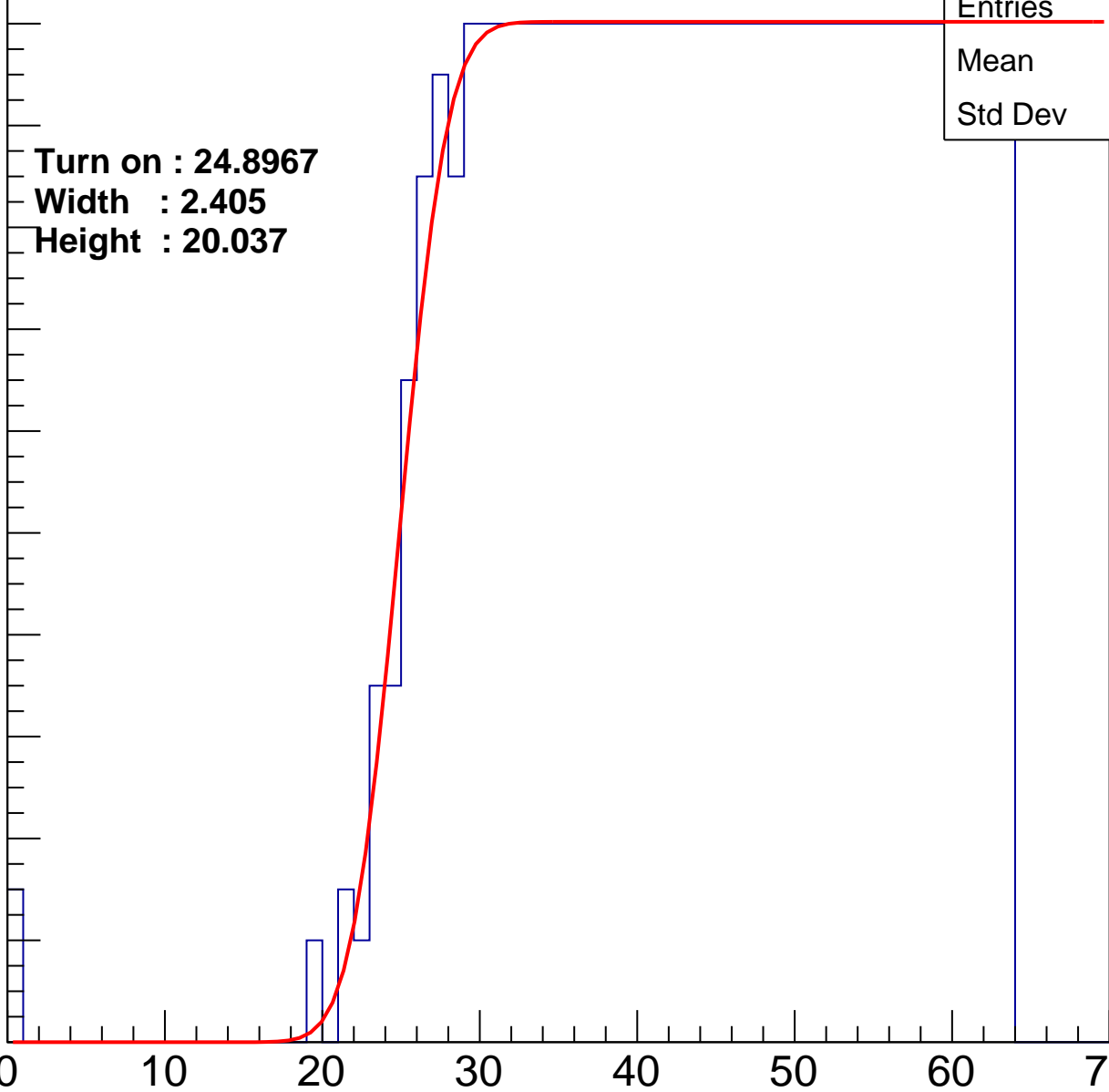
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 24.8967**  
**Width : 2.405**  
**Height : 20.037**

Entries	790
Mean	43.58
Std Dev	11.78

ampl



# B0L101S, U15-ch19

calib\_packv5\_042523\_0143.root, FC#1, port C1

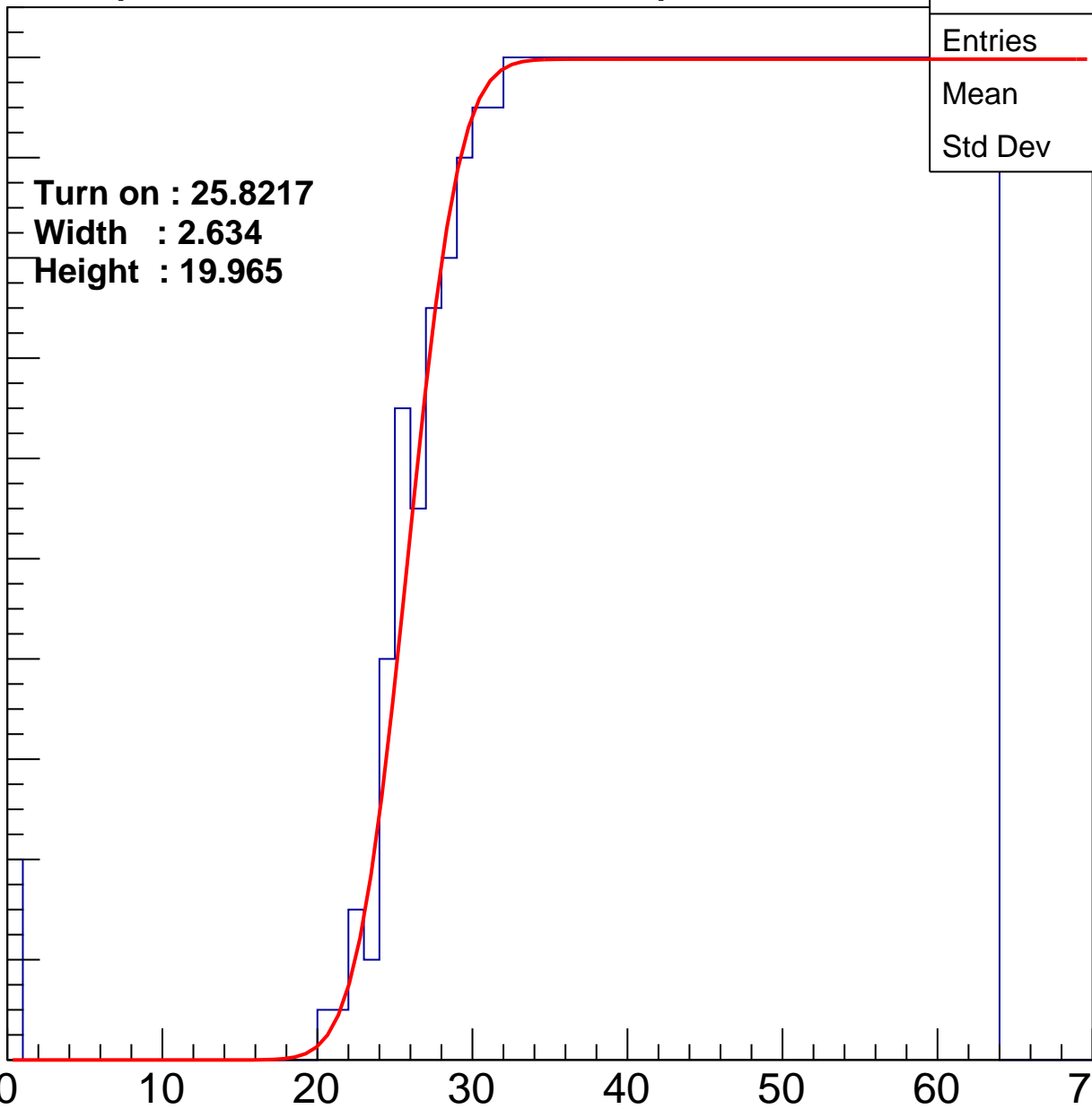
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 25.8217**  
**Width : 2.634**  
**Height : 19.965**

Entries	770
Mean	44.01
Std Dev	11.65

ampl



# B0L101S, U15-ch20

calib\_packv5\_042523\_0143.root, FC#1, port C1

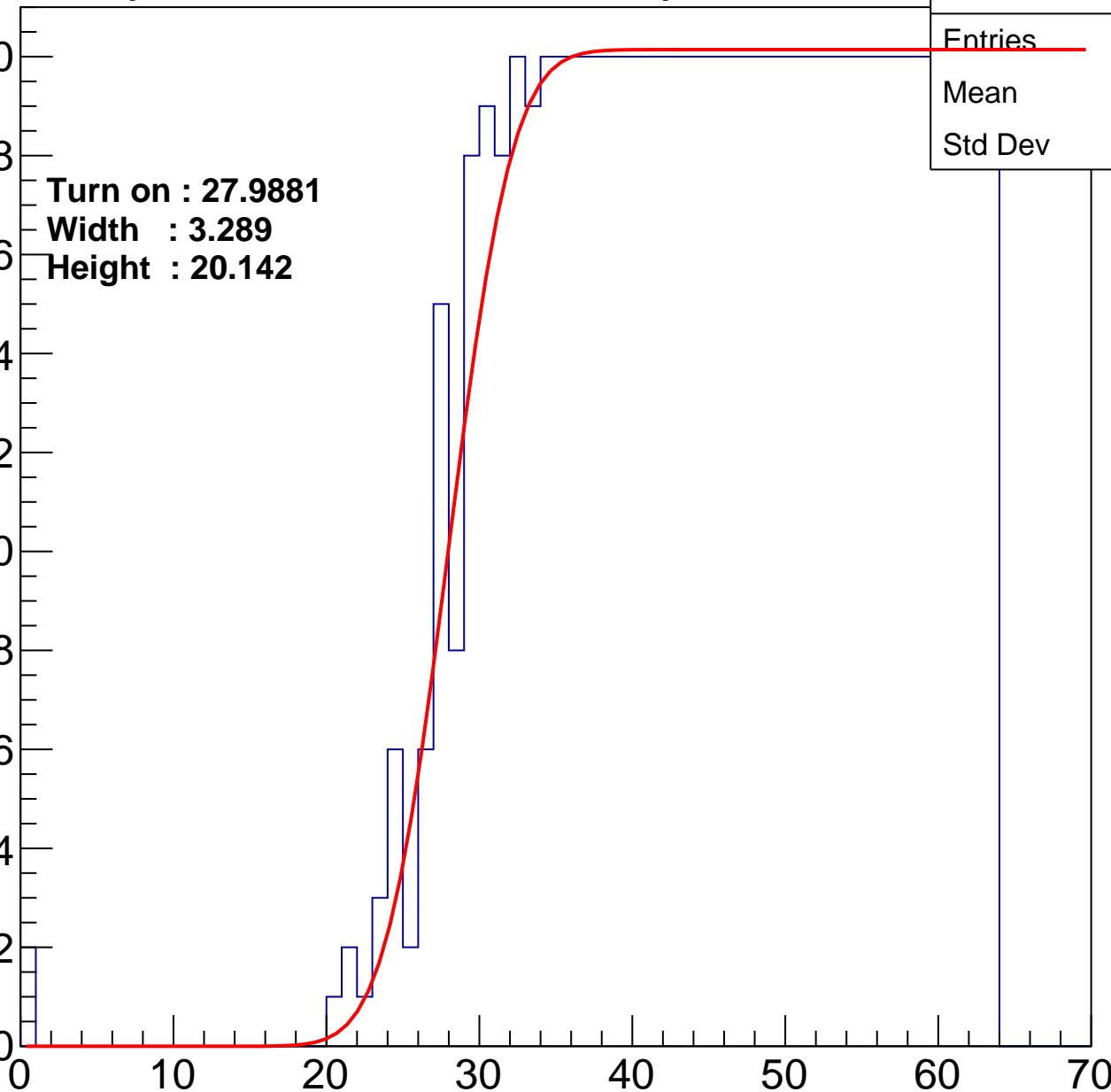
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 27.9881  
Width : 3.289  
Height : 20.142

Entries	740
Mean	44.8
Std Dev	11.11

ampl



# B0L101S, U15-ch21

calib\_packv5\_042523\_0143.root, FC#1, port C1

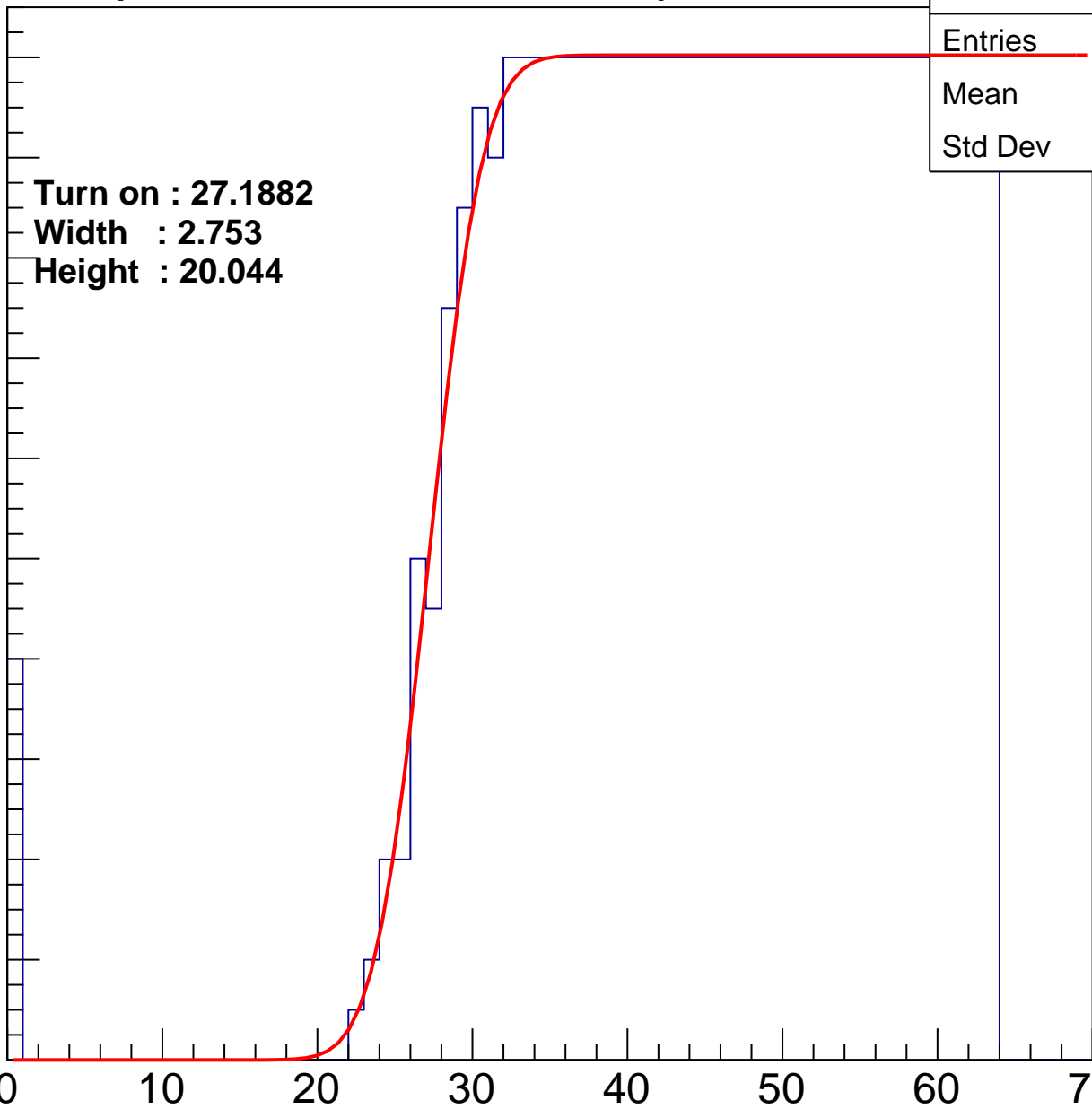
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 27.1882  
Width : 2.753  
Height : 20.044

Entries	747
Mean	44.46
Std Dev	11.71

ampl



# B0L101S, U15-ch22

calib\_packv5\_042523\_0143.root, FC#1, port C1

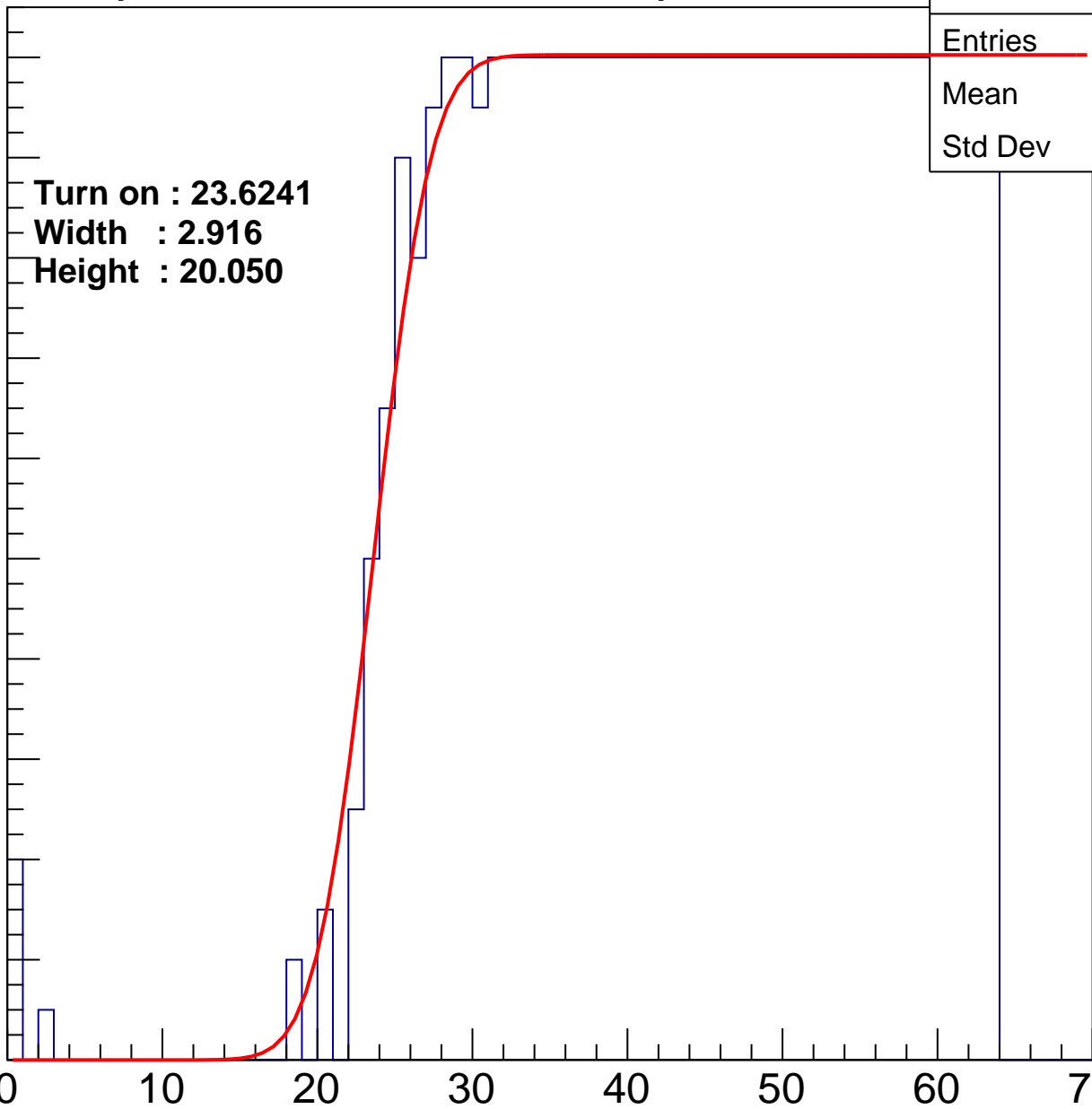
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 23.6241**  
**Width : 2.916**  
**Height : 20.050**

Entries	810
Mean	43.04
Std Dev	12.18

ampl





# B0L101S, U15-ch23

calib\_packv5\_042523\_0143.root, FC#1, port C1

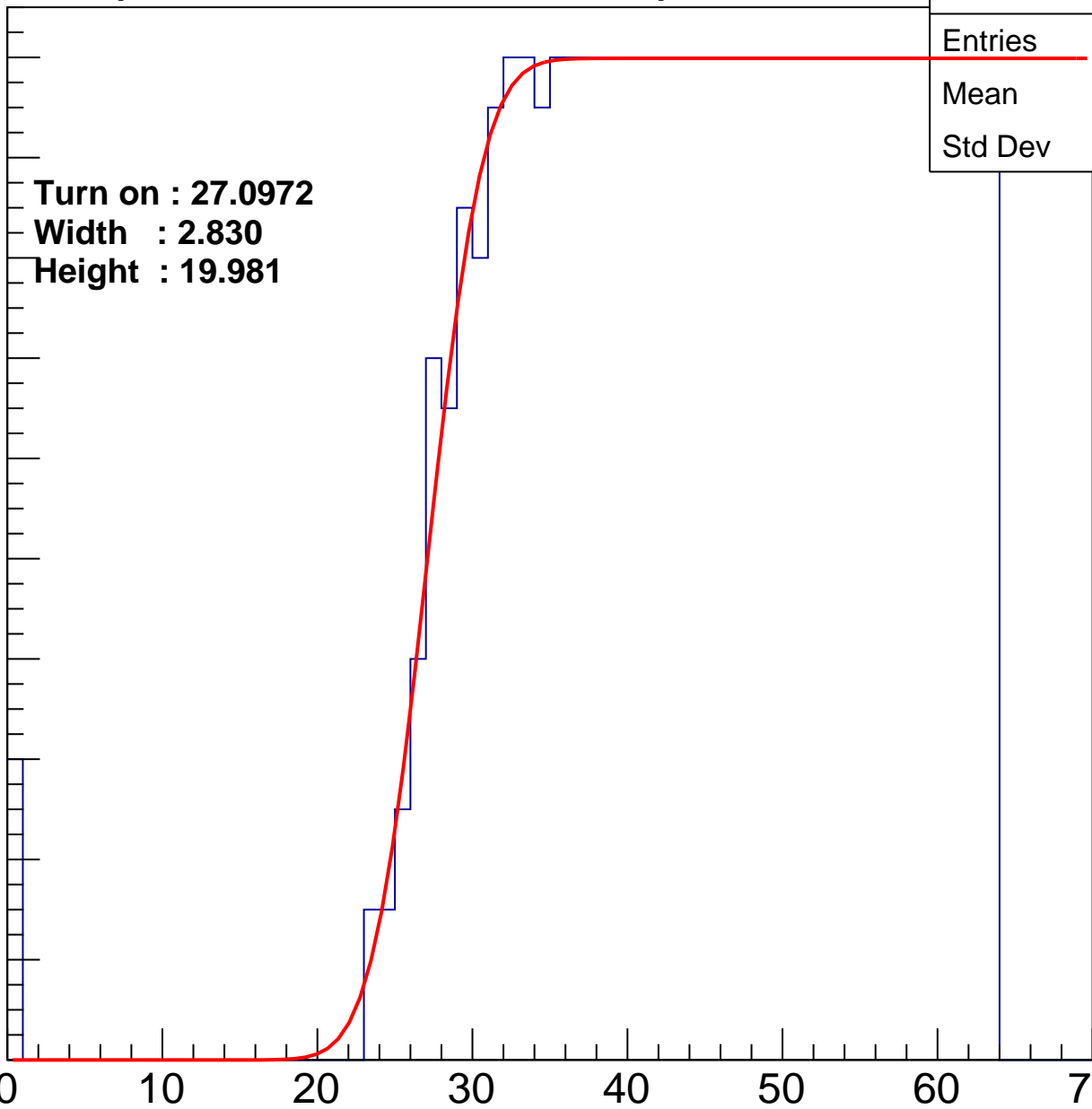
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 27.0972**  
**Width : 2.830**  
**Height : 19.981**

Entries	743
Mean	44.61
Std Dev	11.49

ampl



# B0L101S, U15-ch24

calib\_packv5\_042523\_0143.root, FC#1, port C1

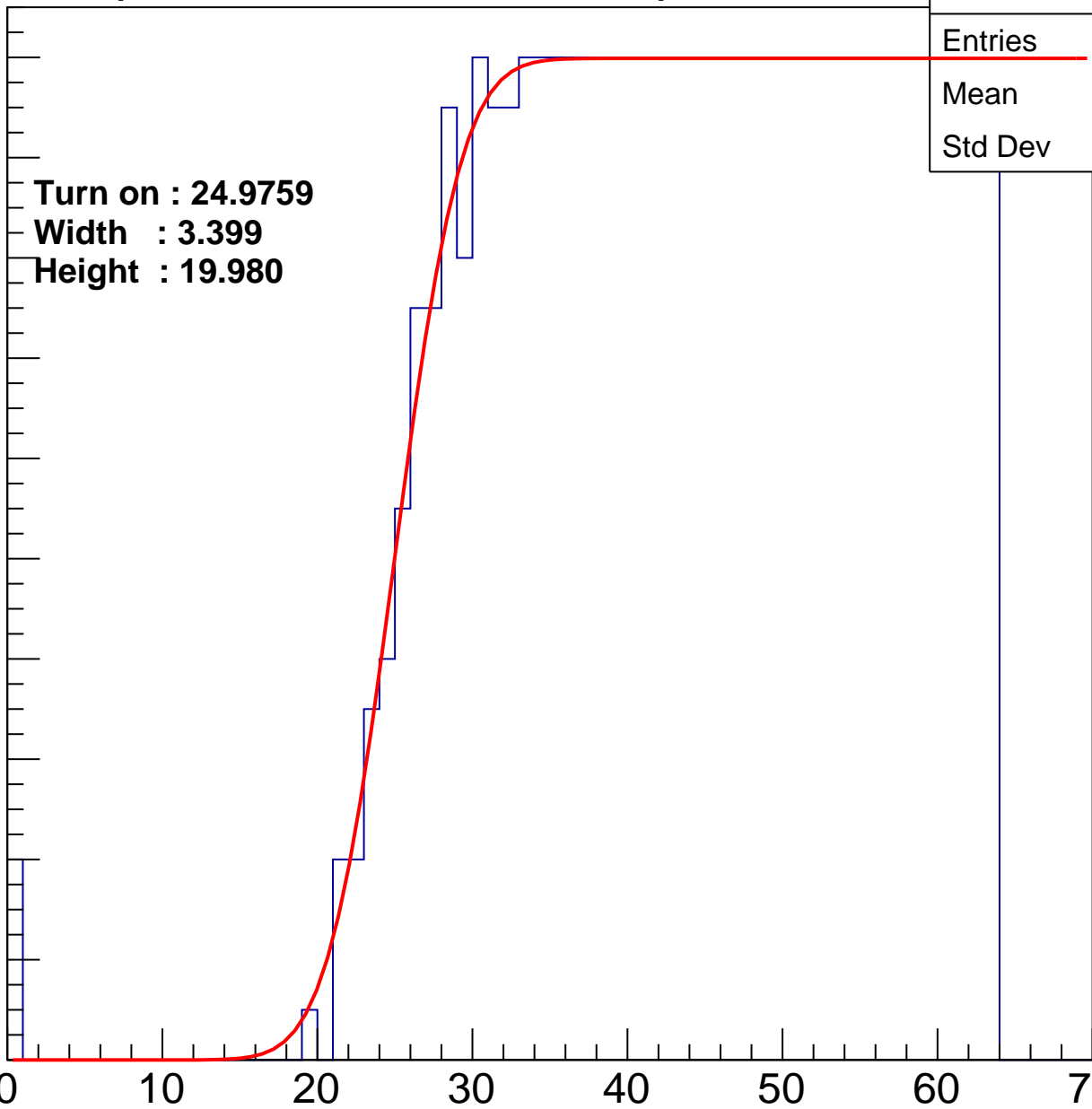
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 24.9759**  
**Width : 3.399**  
**Height : 19.980**

Entries	782
Mean	43.69
Std Dev	11.84

ampl



# B0L101S, U15-ch25

calib\_packv5\_042523\_0143.root, FC#1, port C1

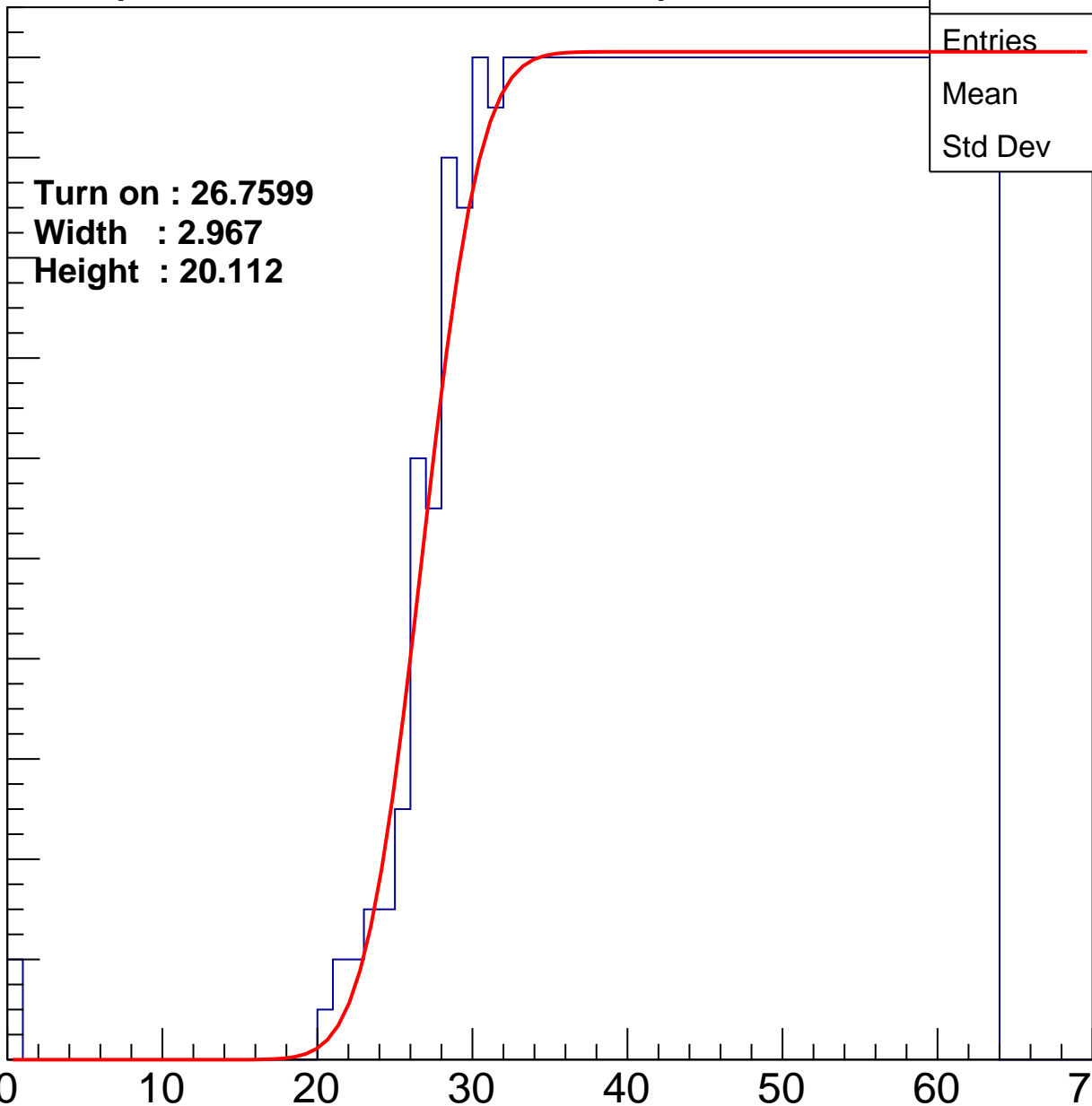
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 26.7599  
Width : 2.967  
Height : 20.112

Entries	755
Mean	44.46
Std Dev	11.26

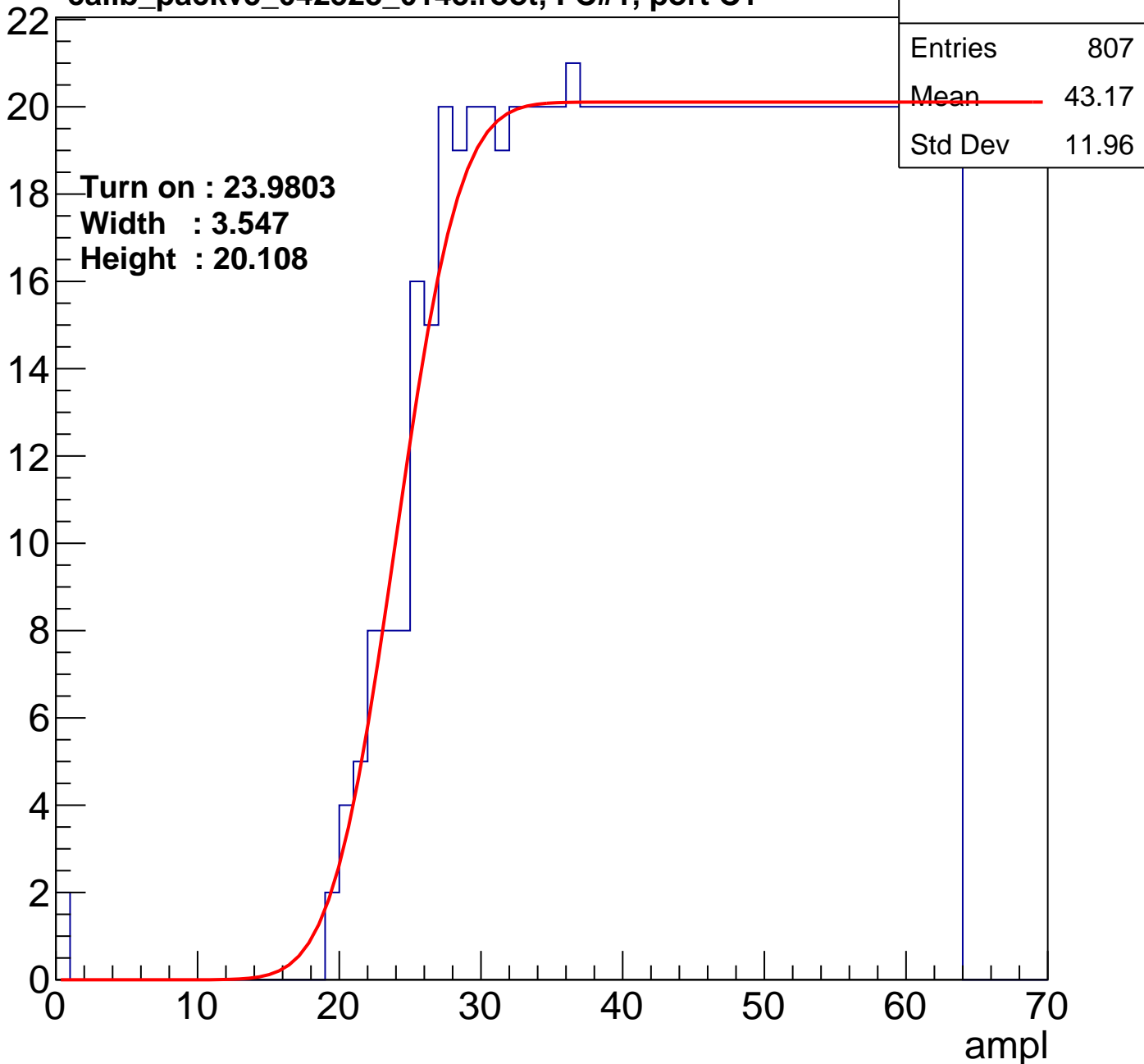
ampl



# B0L101S, U15-ch26

calib\_packv5\_042523\_0143.root, FC#1, port C1

Entry



# B0L101S, U15-ch27

calib\_packv5\_042523\_0143.root, FC#1, port C1

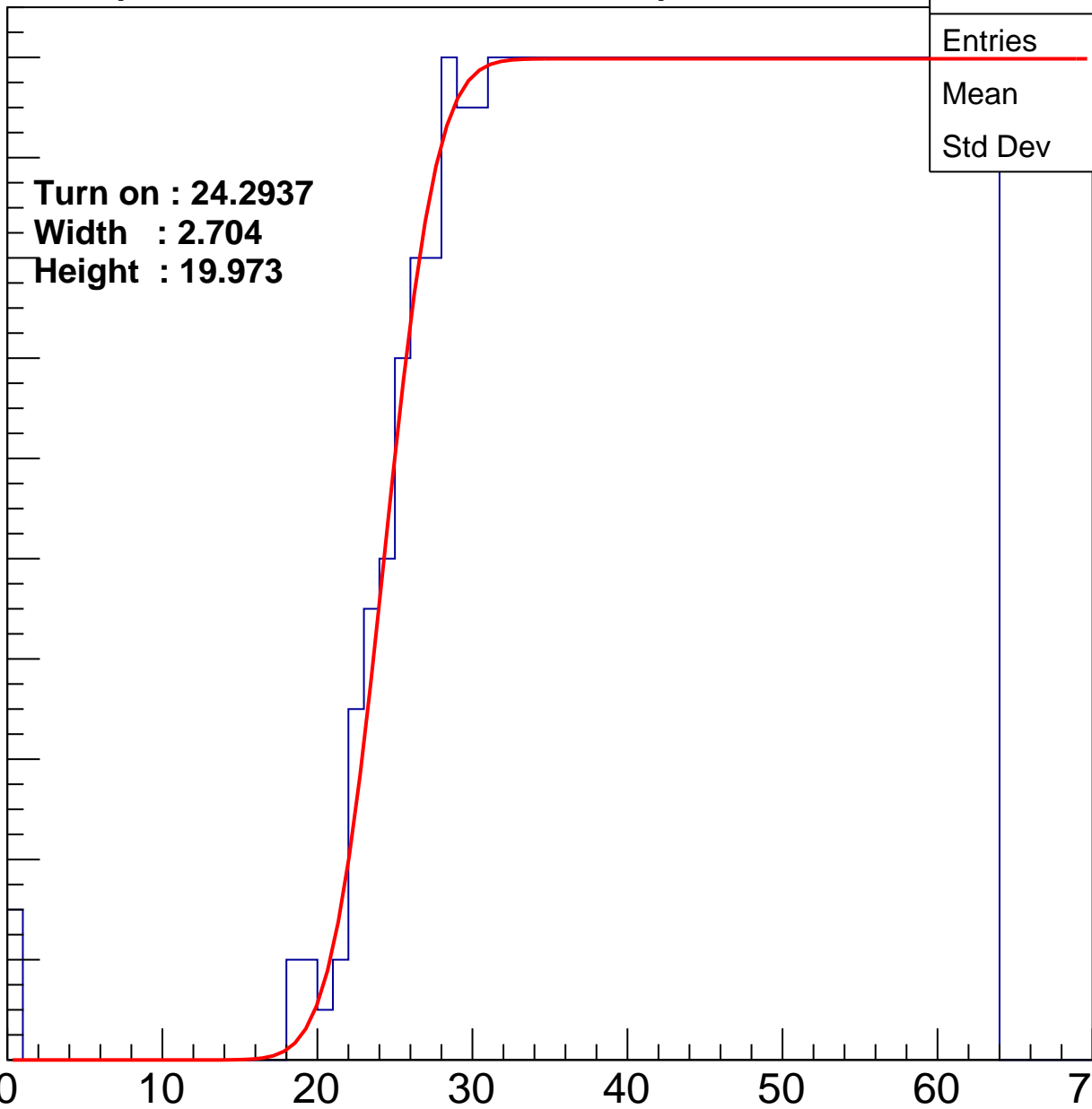
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 24.2937**  
**Width : 2.704**  
**Height : 19.973**

Entries	800
Mean	43.3
Std Dev	11.98

ampl



# B0L101S, U15-ch28

calib\_packv5\_042523\_0143.root, FC#1, port C1

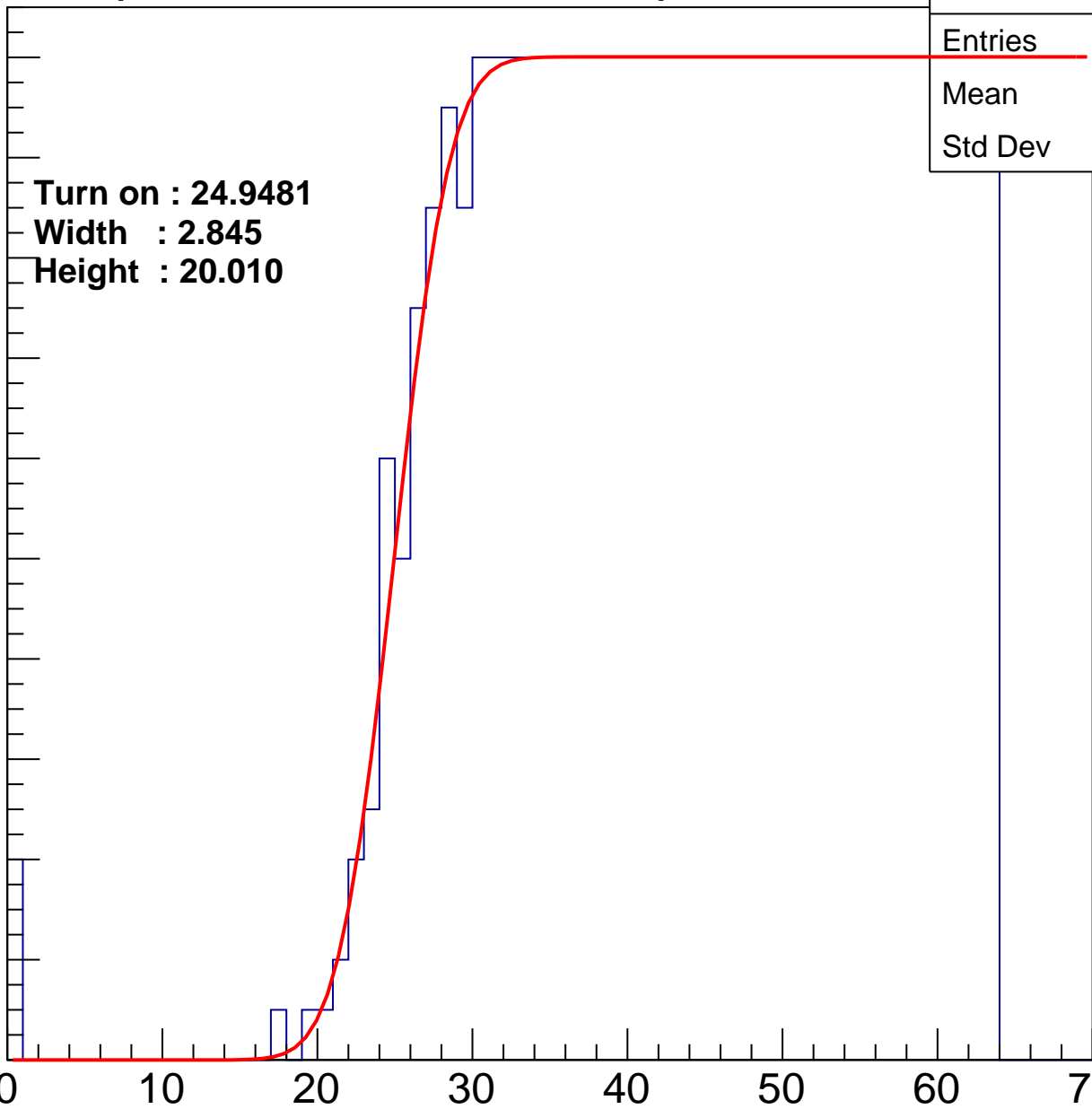
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 24.9481**  
**Width : 2.845**  
**Height : 20.010**

Entries	788
Mean	43.57
Std Dev	11.88

ampl



# B0L101S, U15-ch29

calib\_packv5\_042523\_0143.root, FC#1, port C1

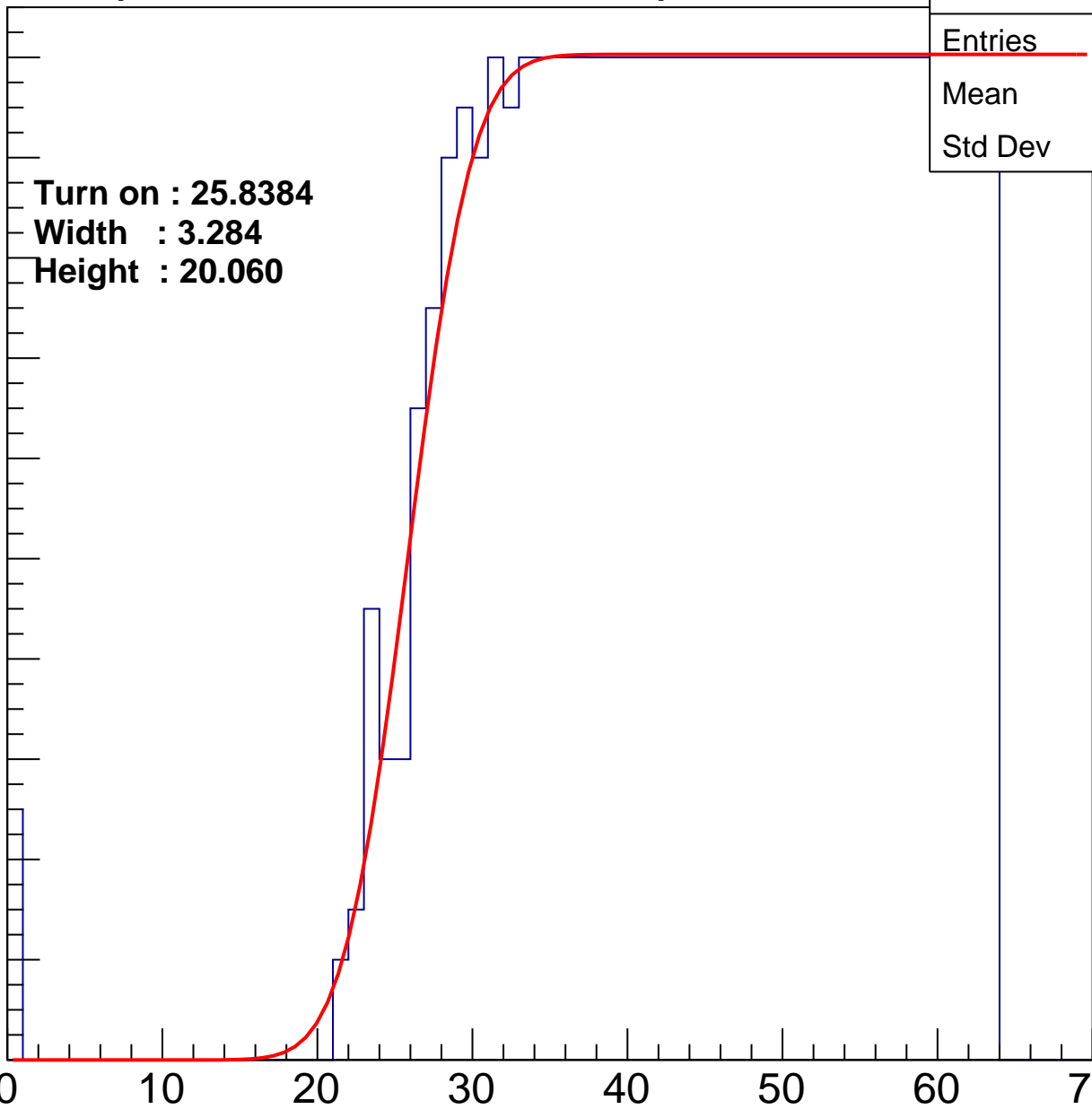
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 25.8384  
Width : 3.284  
Height : 20.060

Entries	773
Mean	43.9
Std Dev	11.78

ampl



# B0L101S, U15-ch30

calib\_packv5\_042523\_0143.root, FC#1, port C1

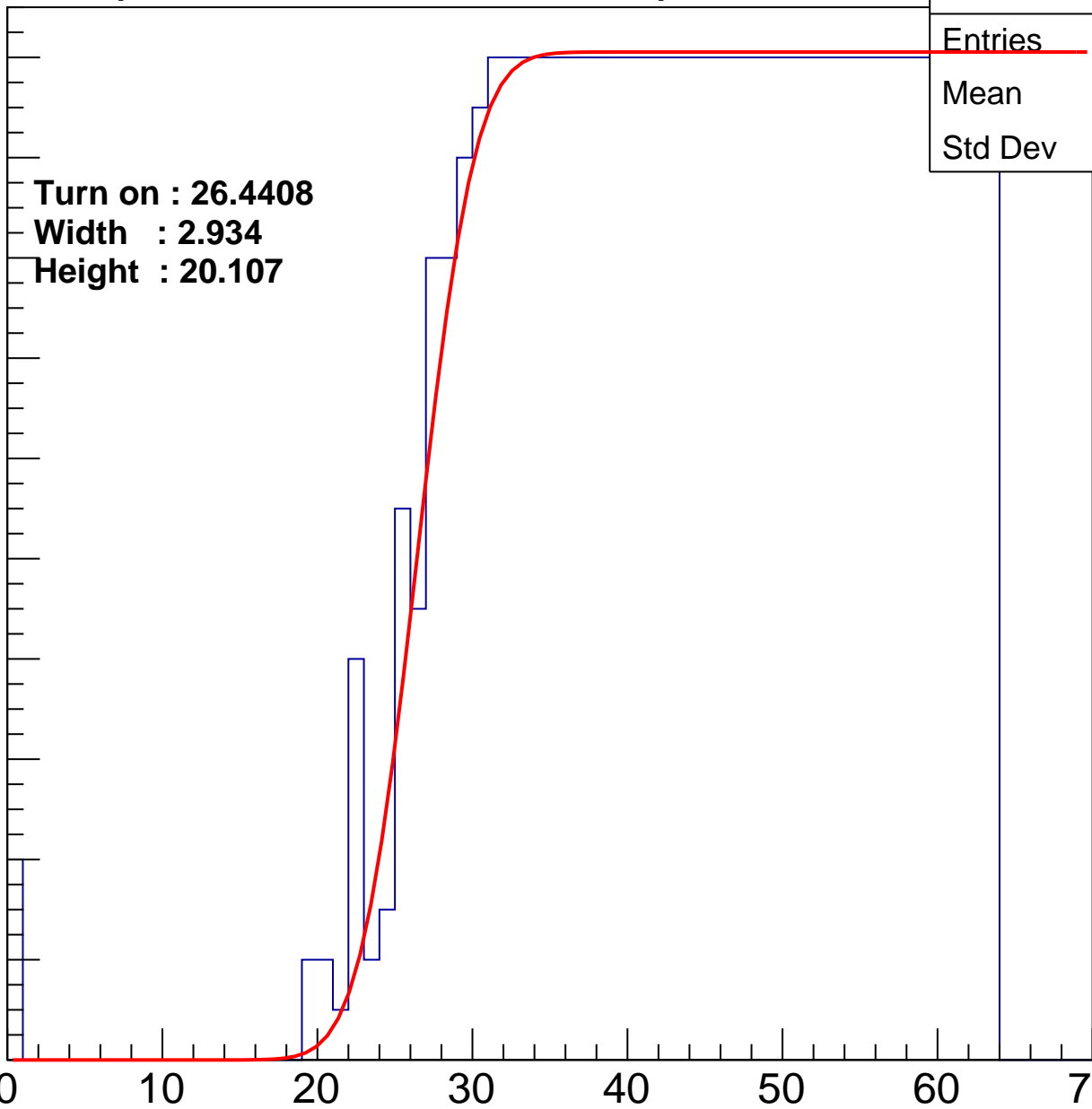
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 26.4408**  
**Width : 2.934**  
**Height : 20.107**

Entries	771
Mean	43.96
Std Dev	11.71

ampl





# B0L101S, U15-ch31

calib\_packv5\_042523\_0143.root, FC#1, port C1

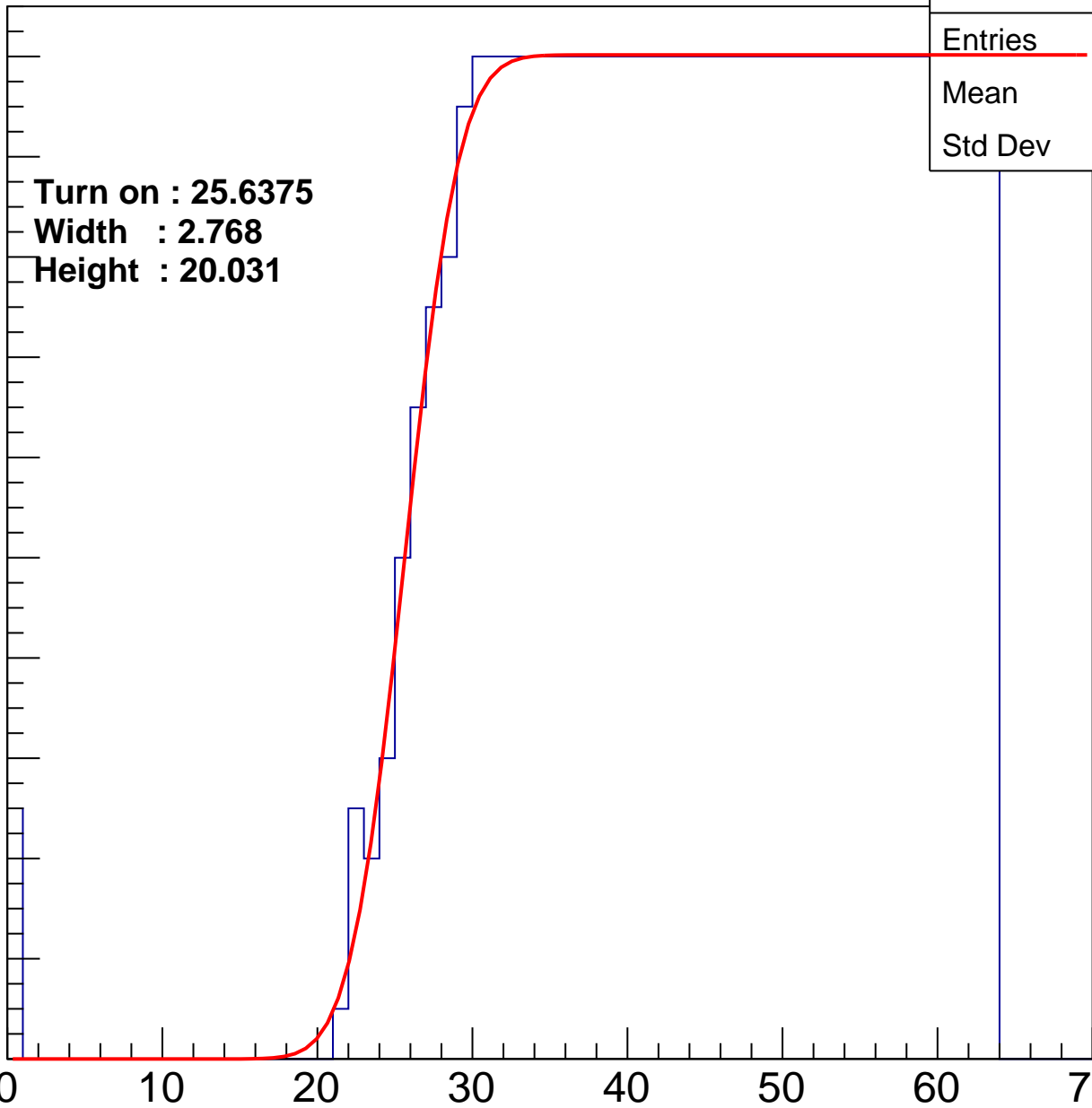
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 25.6375  
Width : 2.768  
Height : 20.031

Entries	774
Mean	43.9
Std Dev	11.76

ampl



# B0L101S, U15-ch32

calib\_packv5\_042523\_0143.root, FC#1, port C1

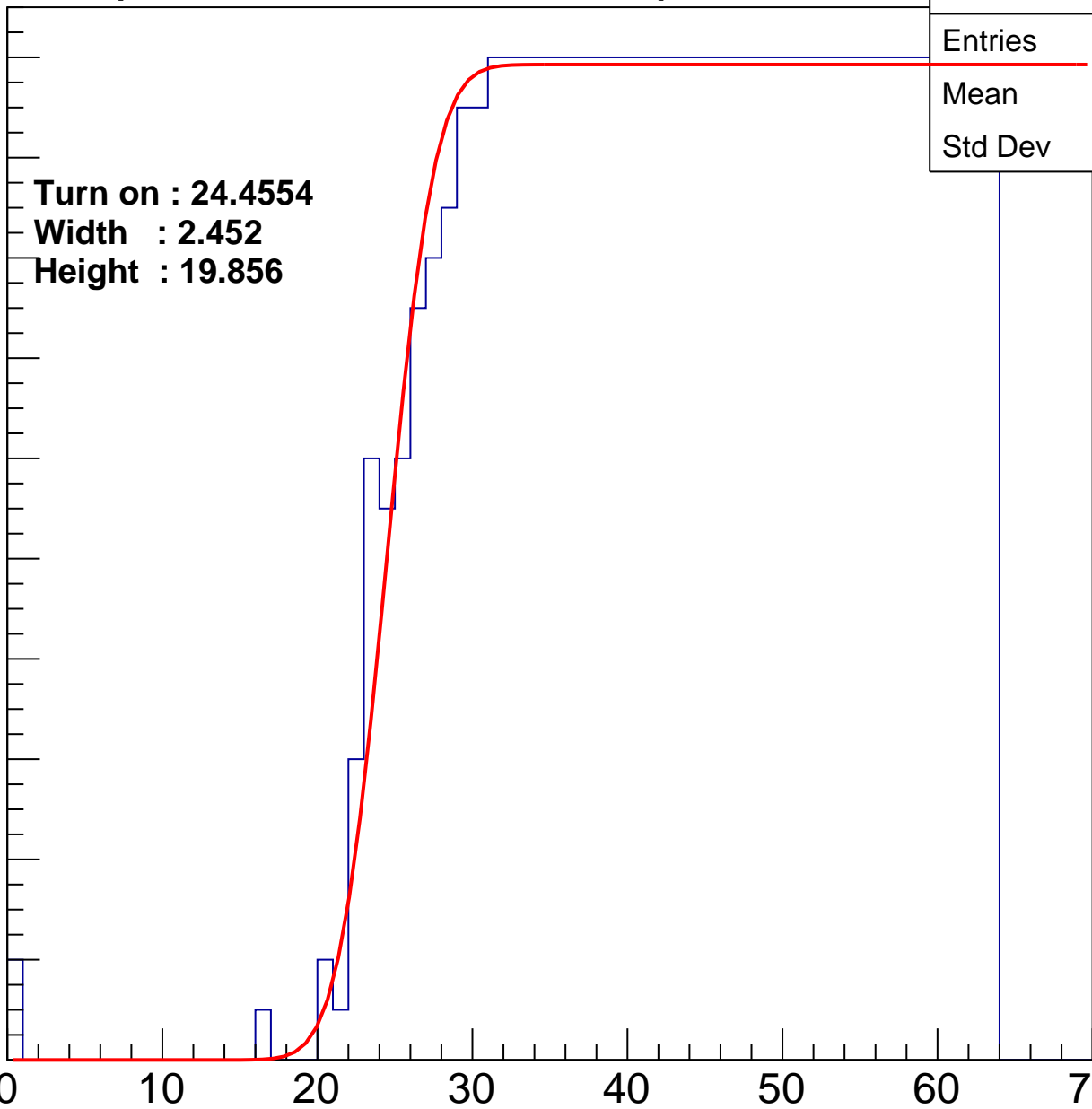
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 24.4554**  
**Width : 2.452**  
**Height : 19.856**

Entries	793
Mean	43.49
Std Dev	11.81

ampl



# B0L101S, U15-ch33

calib\_packv5\_042523\_0143.root, FC#1, port C1

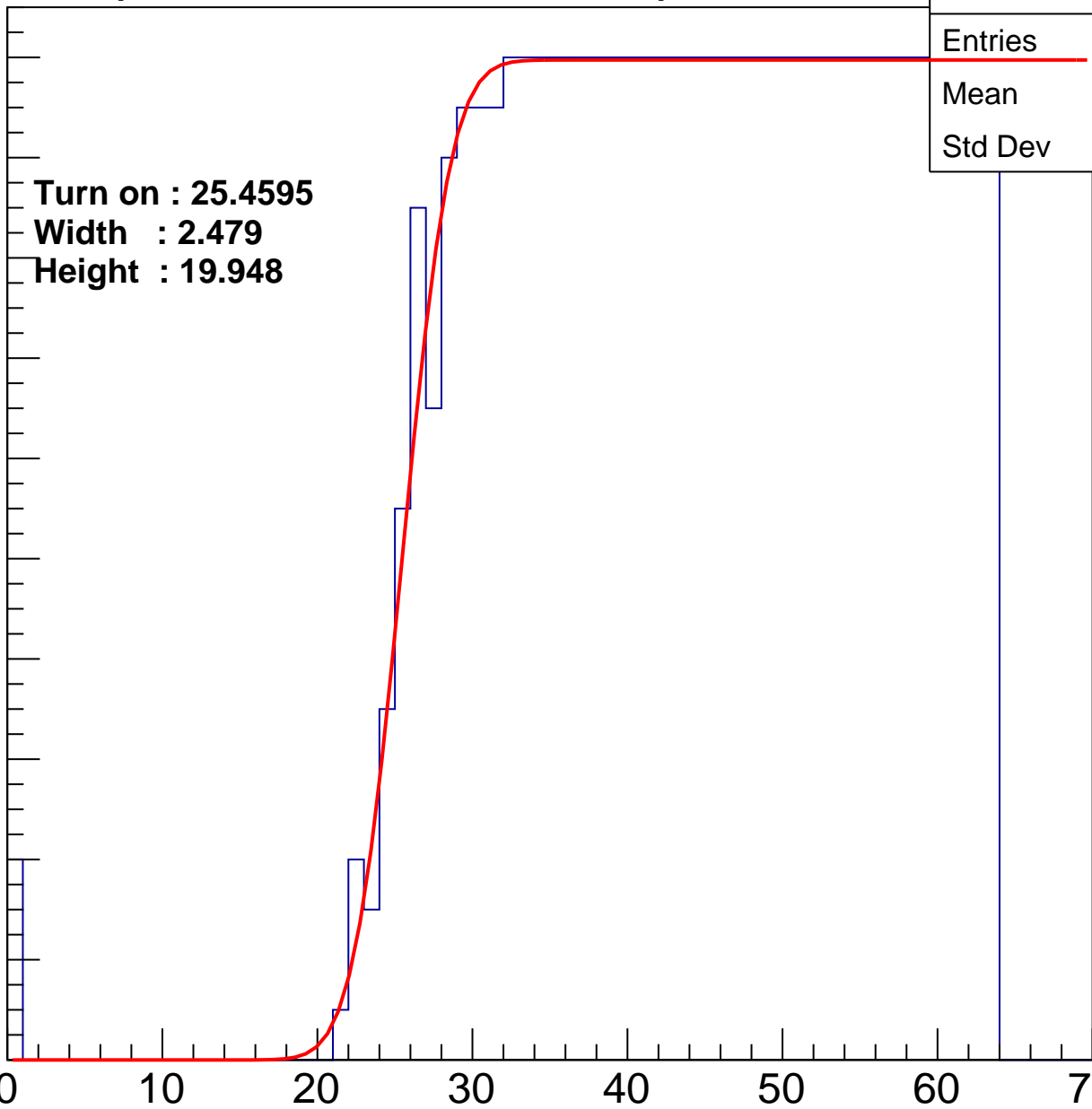
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 25.4595**  
**Width : 2.479**  
**Height : 19.948**

Entries	775
Mean	43.91
Std Dev	11.68

ampl



# B0L101S, U15-ch34

calib\_packv5\_042523\_0143.root, FC#1, port C1

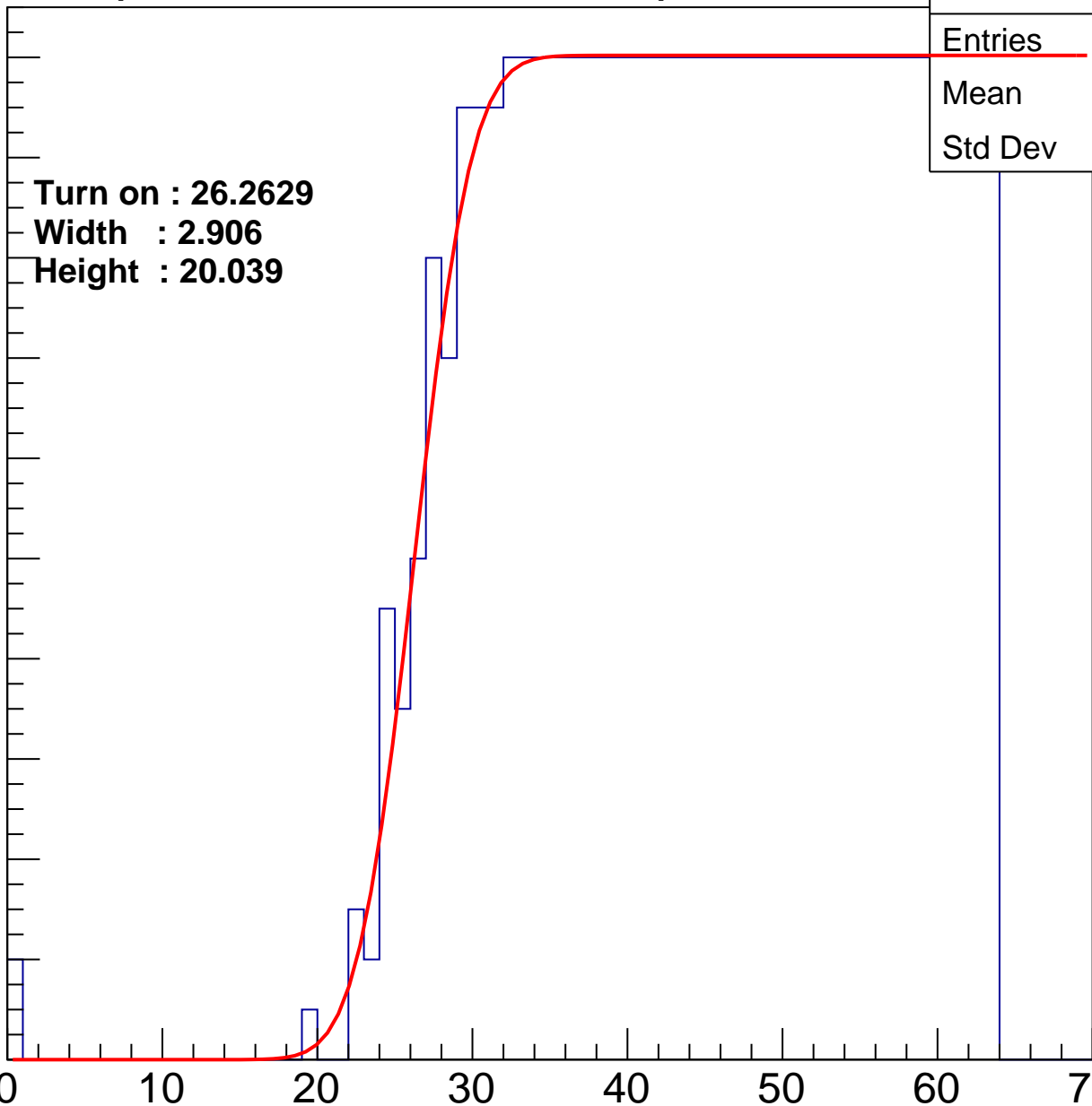
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 26.2629**  
**Width : 2.906**  
**Height : 20.039**

Entries	761
Mean	44.3
Std Dev	11.34

ampl



# B0L101S, U15-ch35

calib\_packv5\_042523\_0143.root, FC#1, port C1

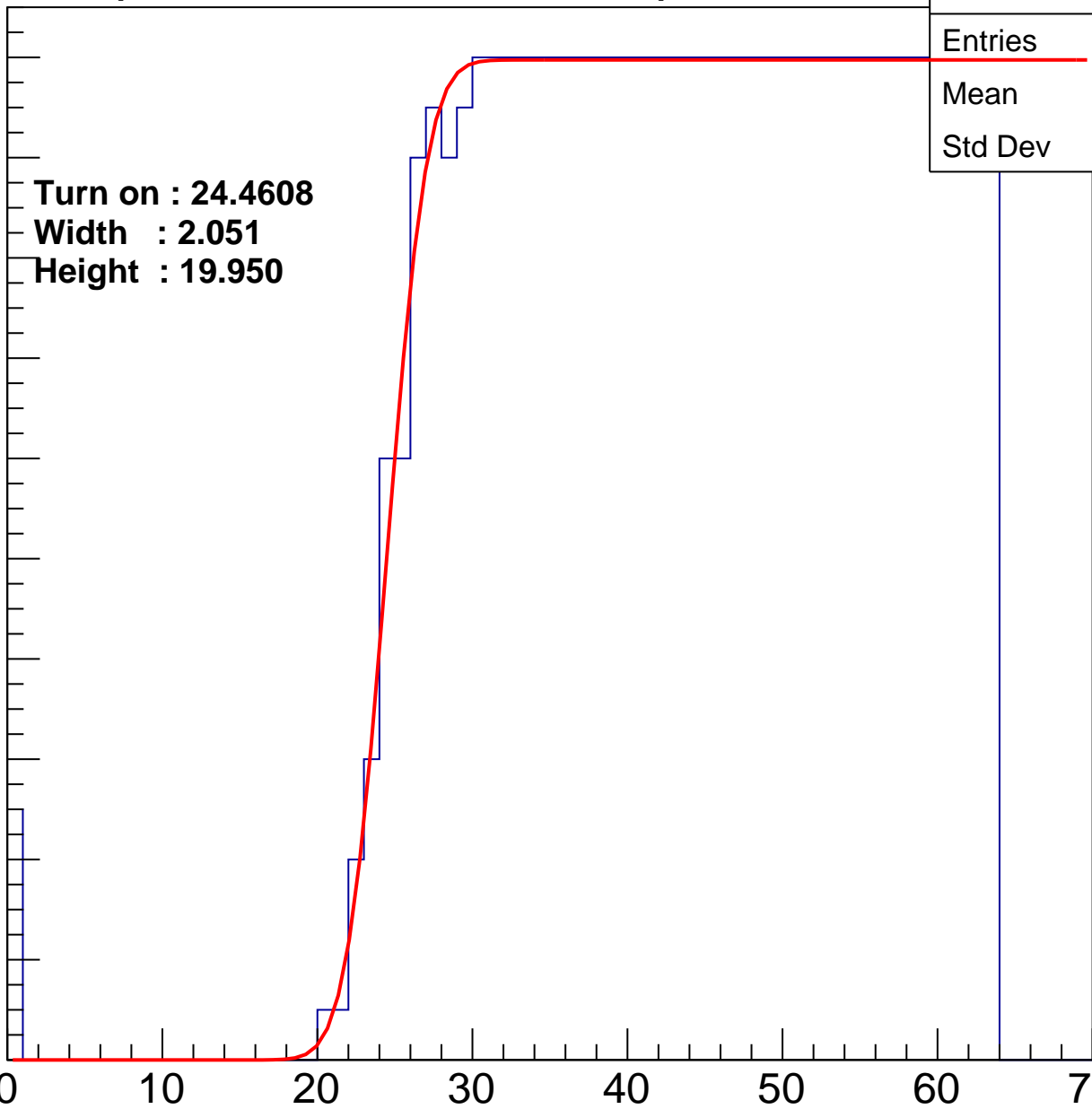
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 24.4608**  
**Width : 2.051**  
**Height : 19.950**

Entries	795
Mean	43.41
Std Dev	11.98

ampl



# B0L101S, U15-ch36

calib\_packv5\_042523\_0143.root, FC#1, port C1

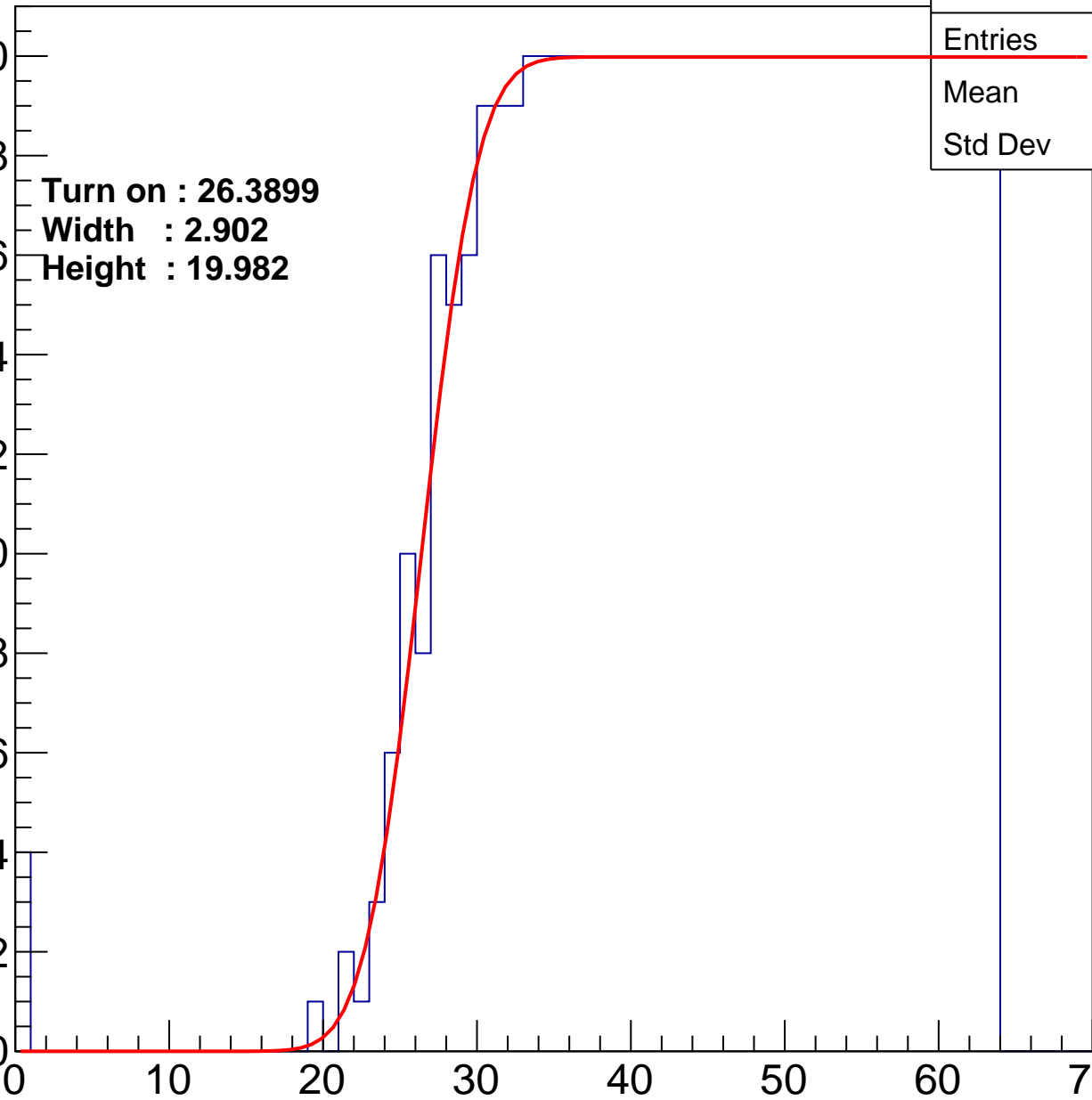
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 26.3899**  
**Width : 2.902**  
**Height : 19.982**

Entries	759
Mean	44.26
Std Dev	11.54

ampl



# B0L101S, U15-ch37

calib\_packv5\_042523\_0143.root, FC#1, port C1

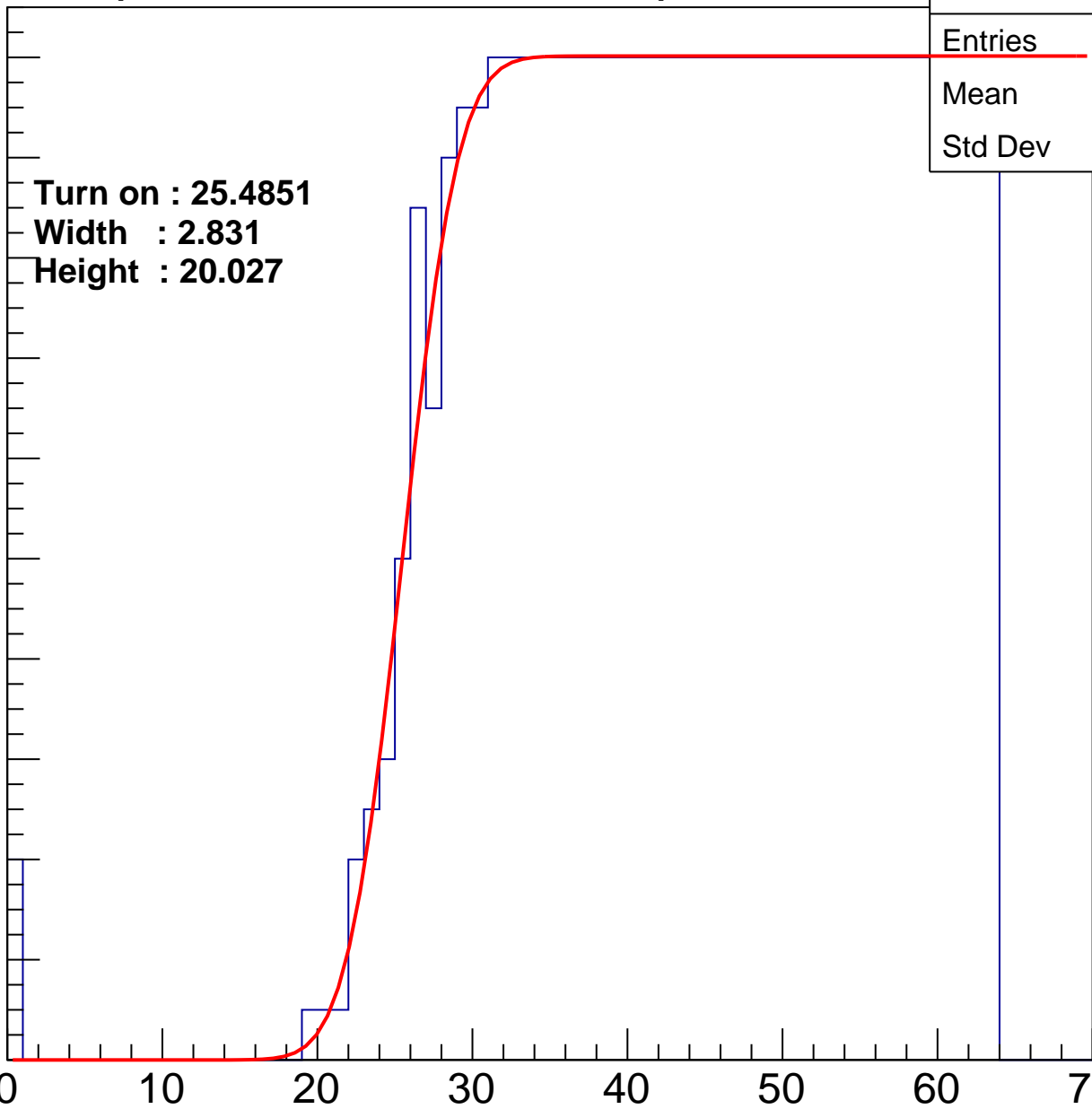
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 25.4851**  
**Width : 2.831**  
**Height : 20.027**

Entries	778
Mean	43.82
Std Dev	11.74

ampl



# B0L101S, U15-ch38

calib\_packv5\_042523\_0143.root, FC#1, port C1

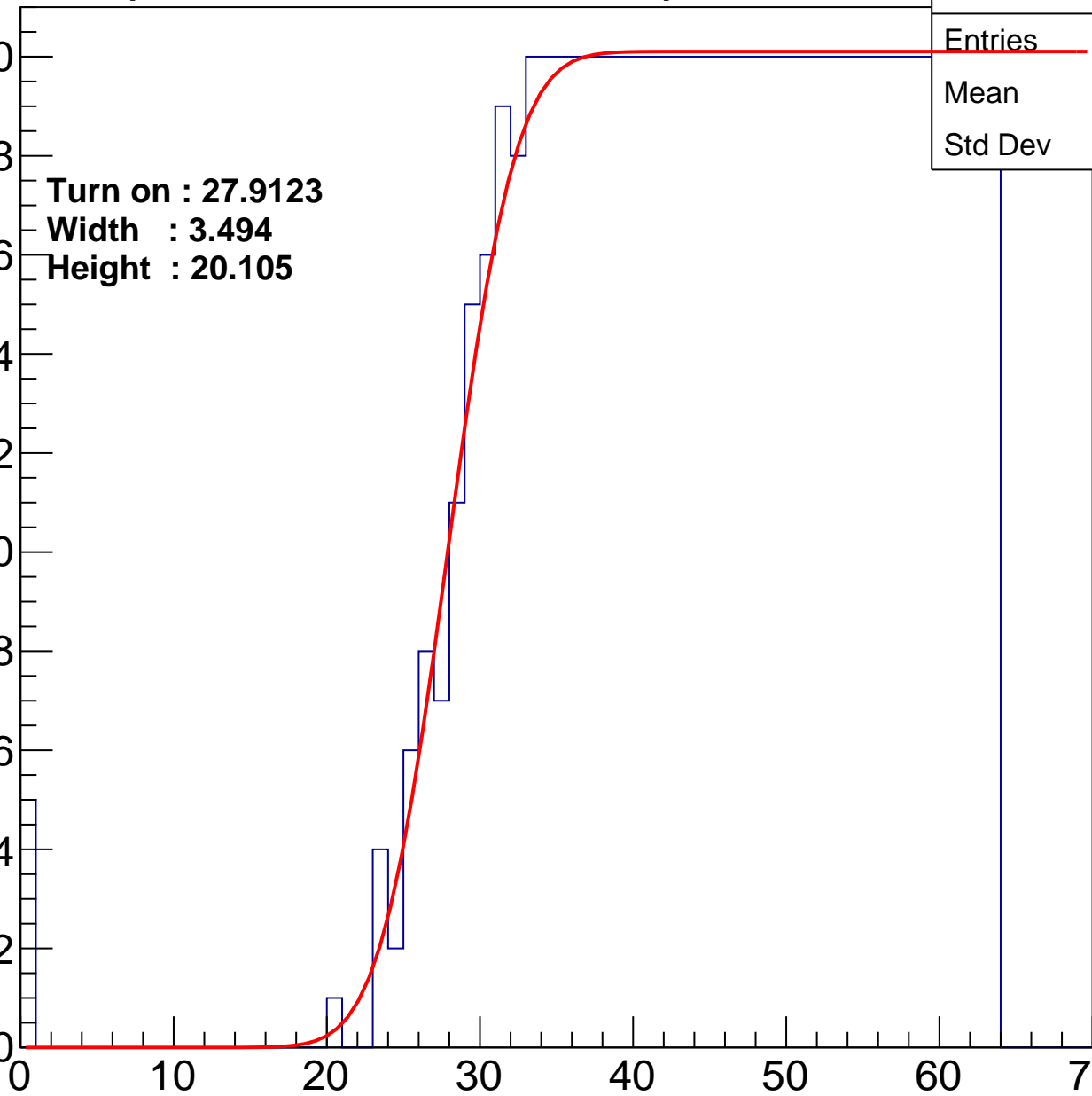
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 27.9123  
Width : 3.494  
Height : 20.105

Entries	732
Mean	44.88
Std Dev	11.31

ampl





# B0L101S, U15-ch39

calib\_packv5\_042523\_0143.root, FC#1, port C1

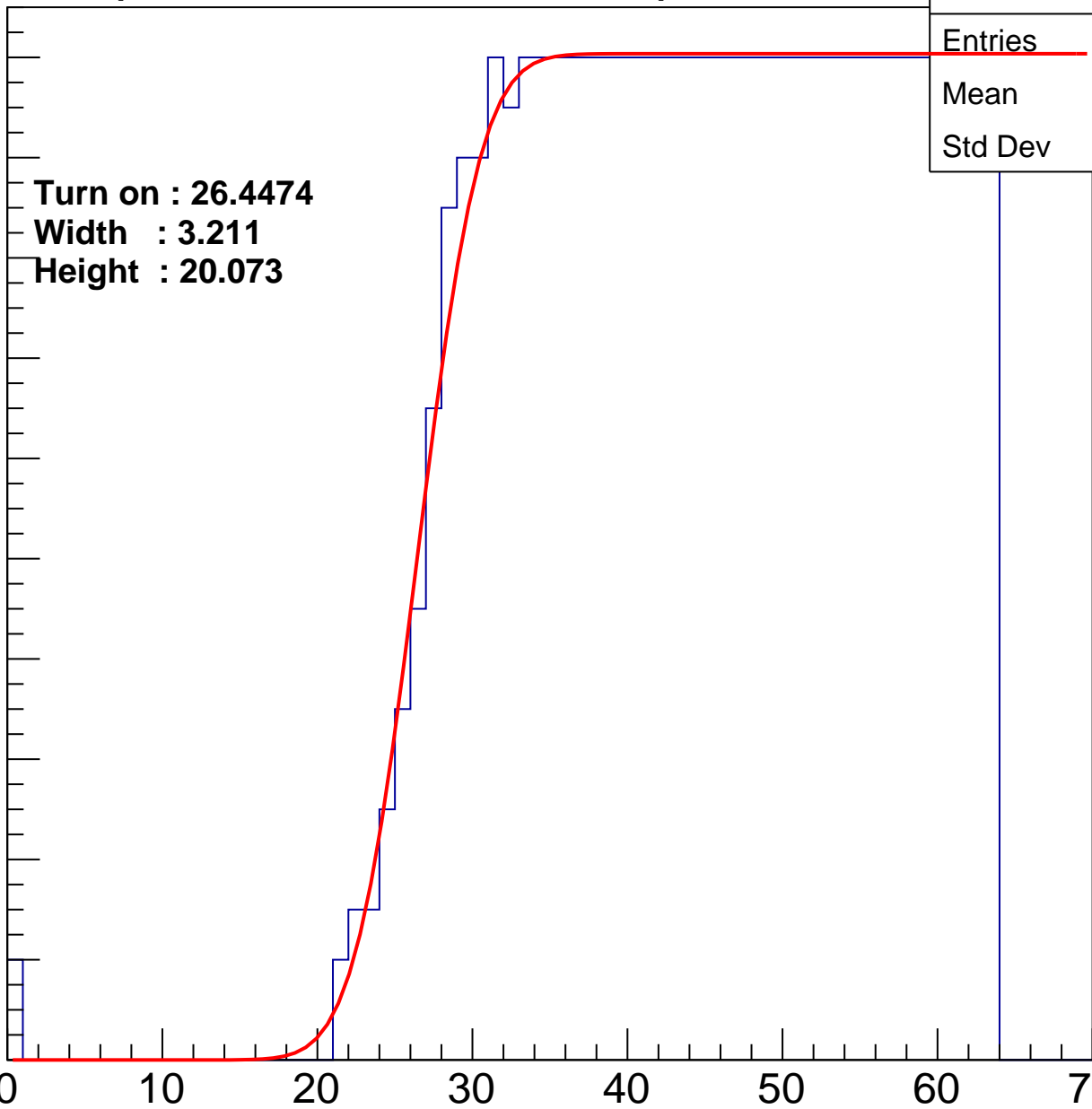
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 26.4474**  
**Width : 3.211**  
**Height : 20.073**

Entries	756
Mean	44.42
Std Dev	11.29

ampl



# B0L101S, U15-ch40

calib\_packv5\_042523\_0143.root, FC#1, port C1

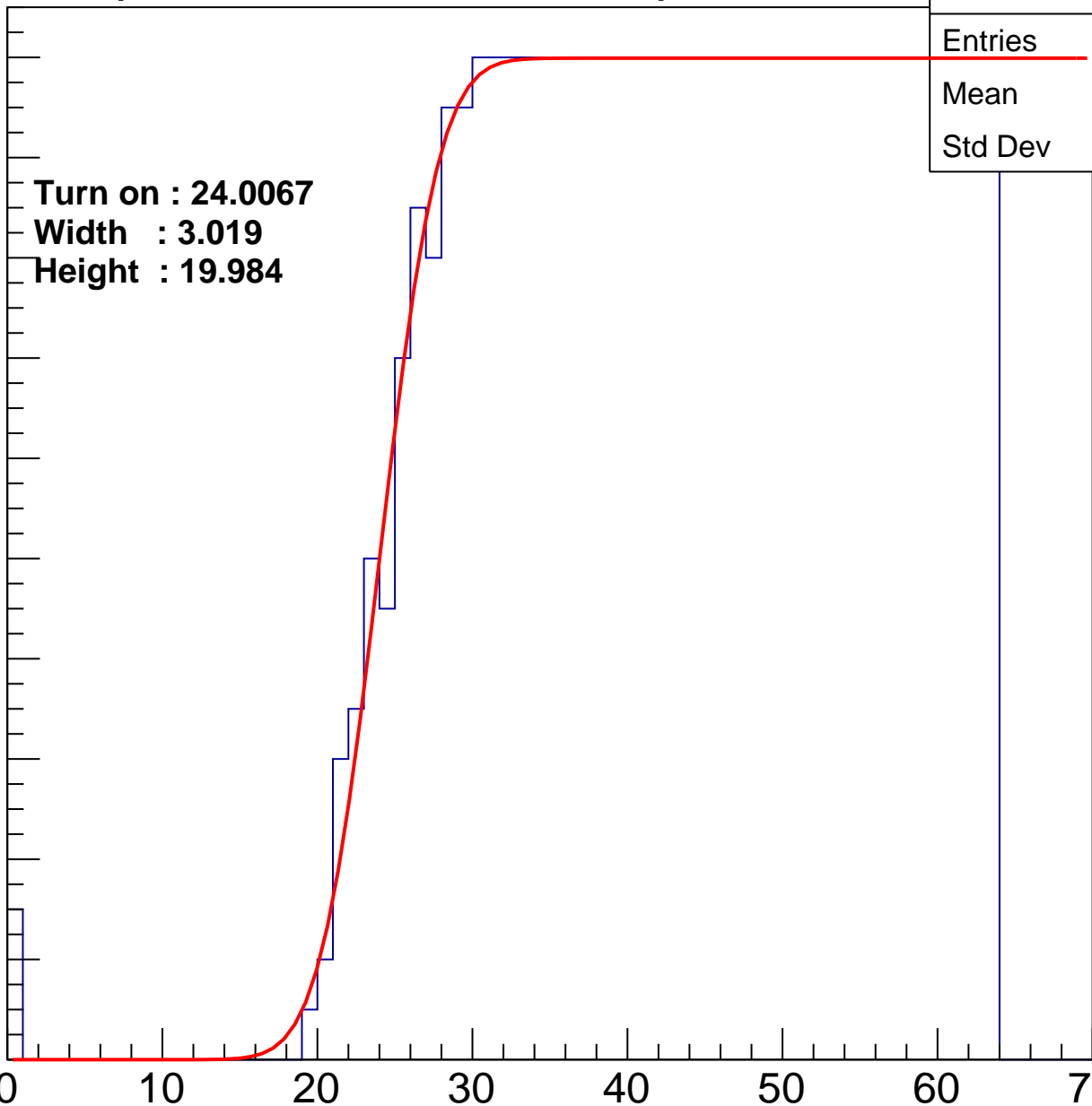
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 24.0067  
Width : 3.019  
Height : 19.984

Entries	803
Mean	43.23
Std Dev	12

ampl



# B0L101S, U15-ch41

calib\_packv5\_042523\_0143.root, FC#1, port C1

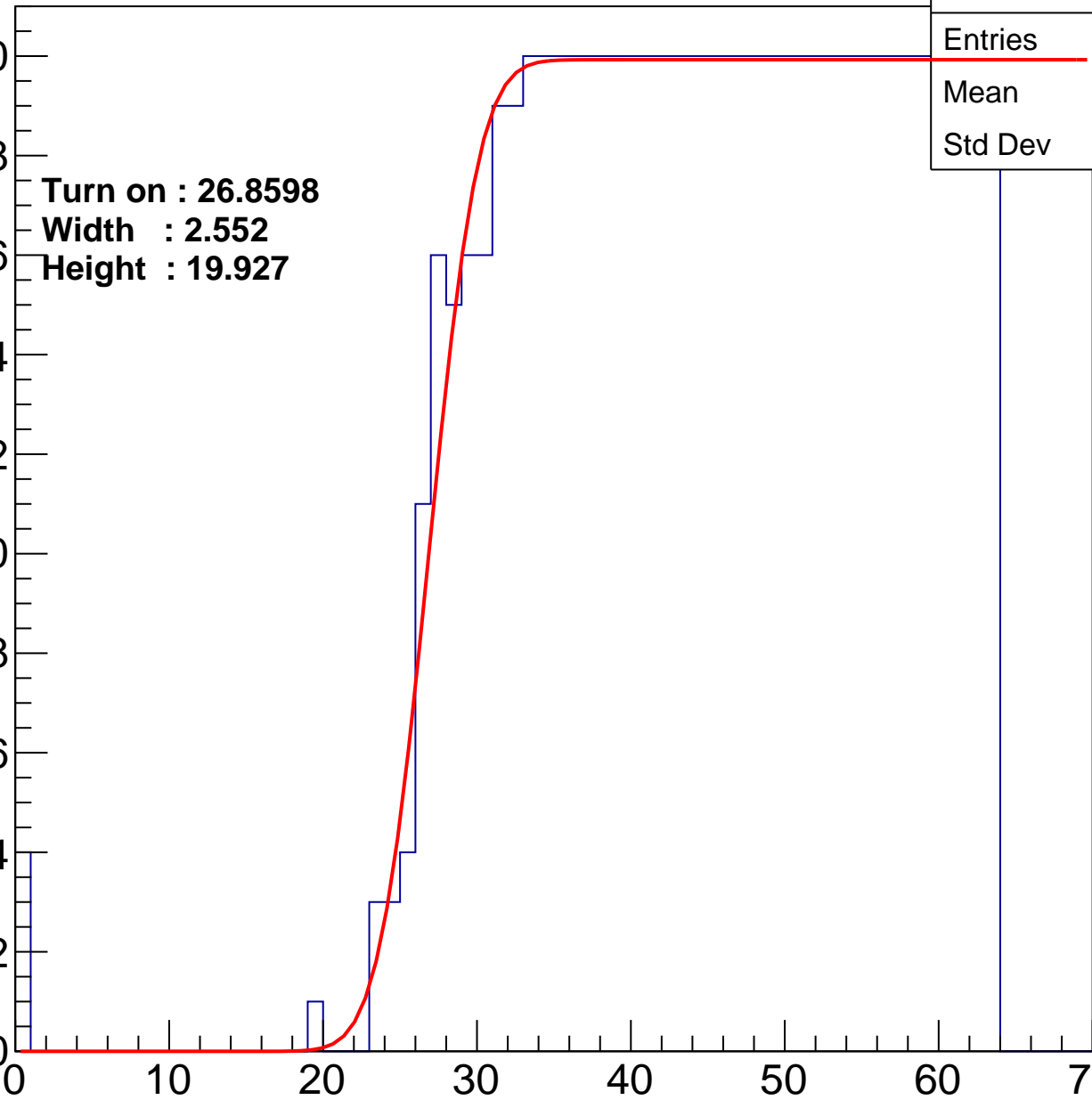
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 26.8598**  
**Width : 2.552**  
**Height : 19.927**

Entries	747
Mean	44.58
Std Dev	11.36

ampl



# B0L101S, U15-ch42

calib\_packv5\_042523\_0143.root, FC#1, port C1

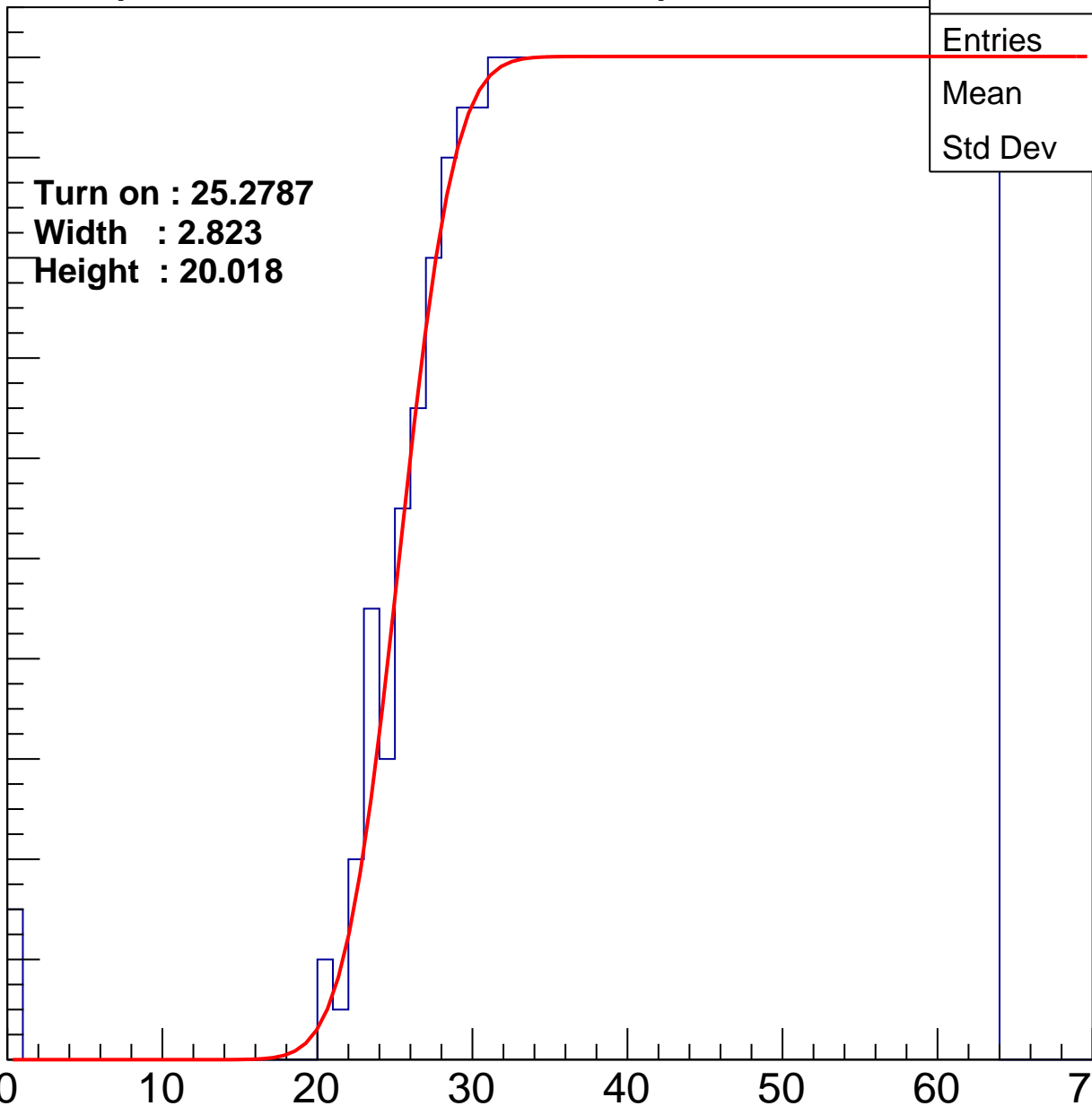
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 25.2787**  
**Width : 2.823**  
**Height : 20.018**

Entries	781
Mean	43.78
Std Dev	11.7

ampl



# B0L101S, U15-ch43

calib\_packv5\_042523\_0143.root, FC#1, port C1

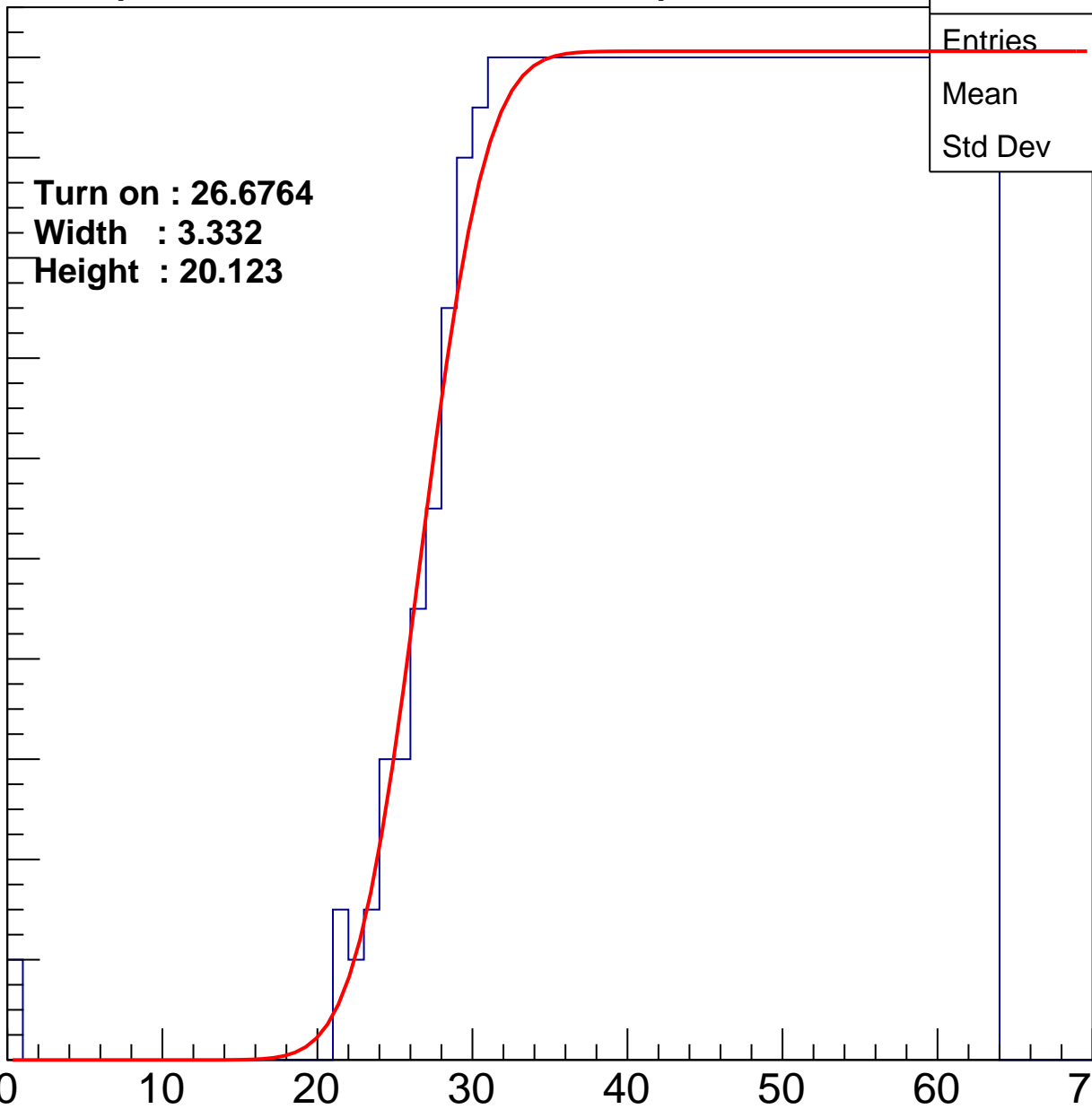
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 26.6764**  
**Width : 3.332**  
**Height : 20.123**

Entries	754
Mean	44.47
Std Dev	11.26

ampl



# B0L101S, U15-ch44

calib\_packv5\_042523\_0143.root, FC#1, port C1

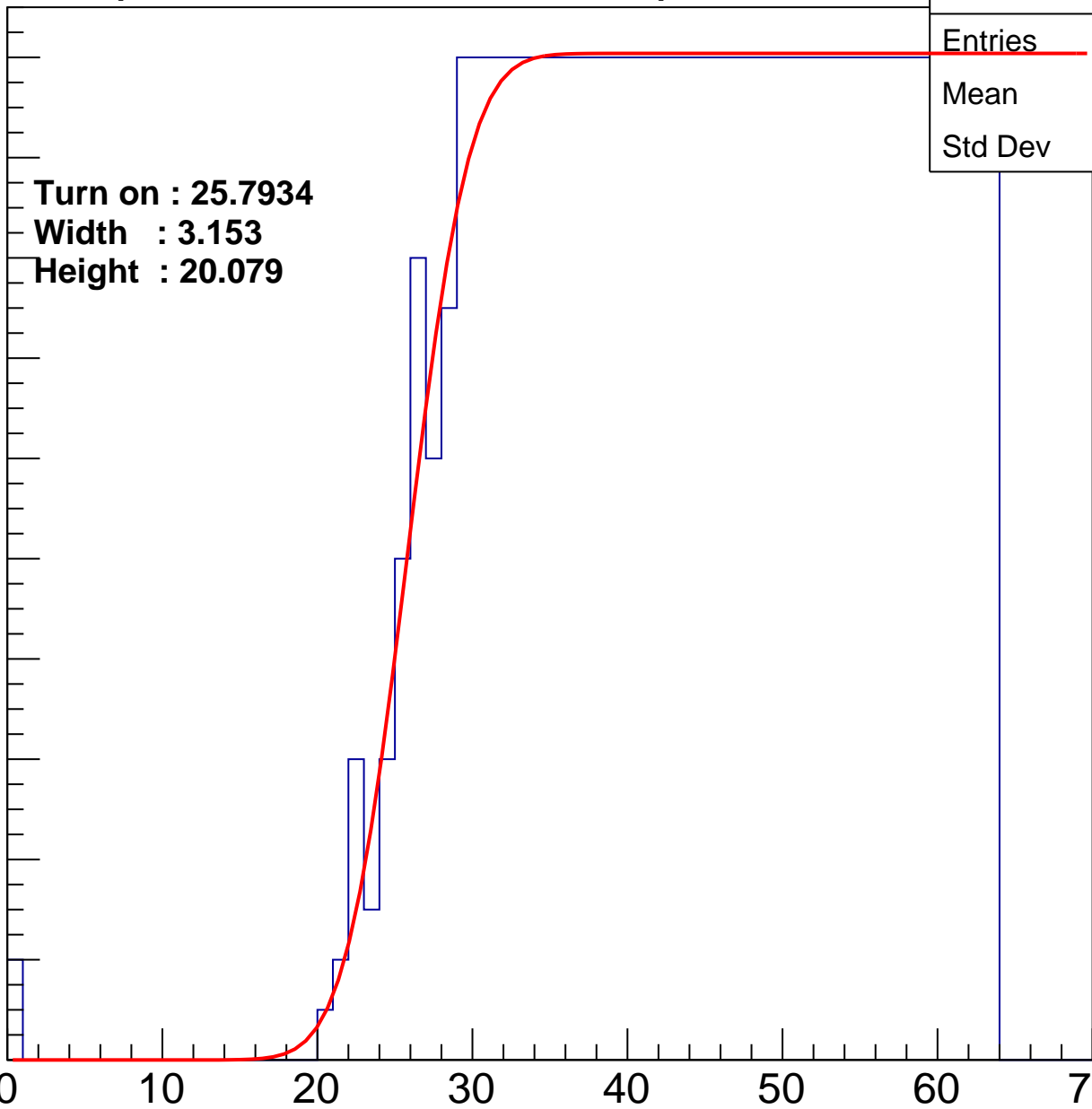
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 25.7934**  
**Width : 3.153**  
**Height : 20.079**

Entries	773
Mean	44.01
Std Dev	11.51

ampl



# B0L101S, U15-ch45

calib\_packv5\_042523\_0143.root, FC#1, port C1

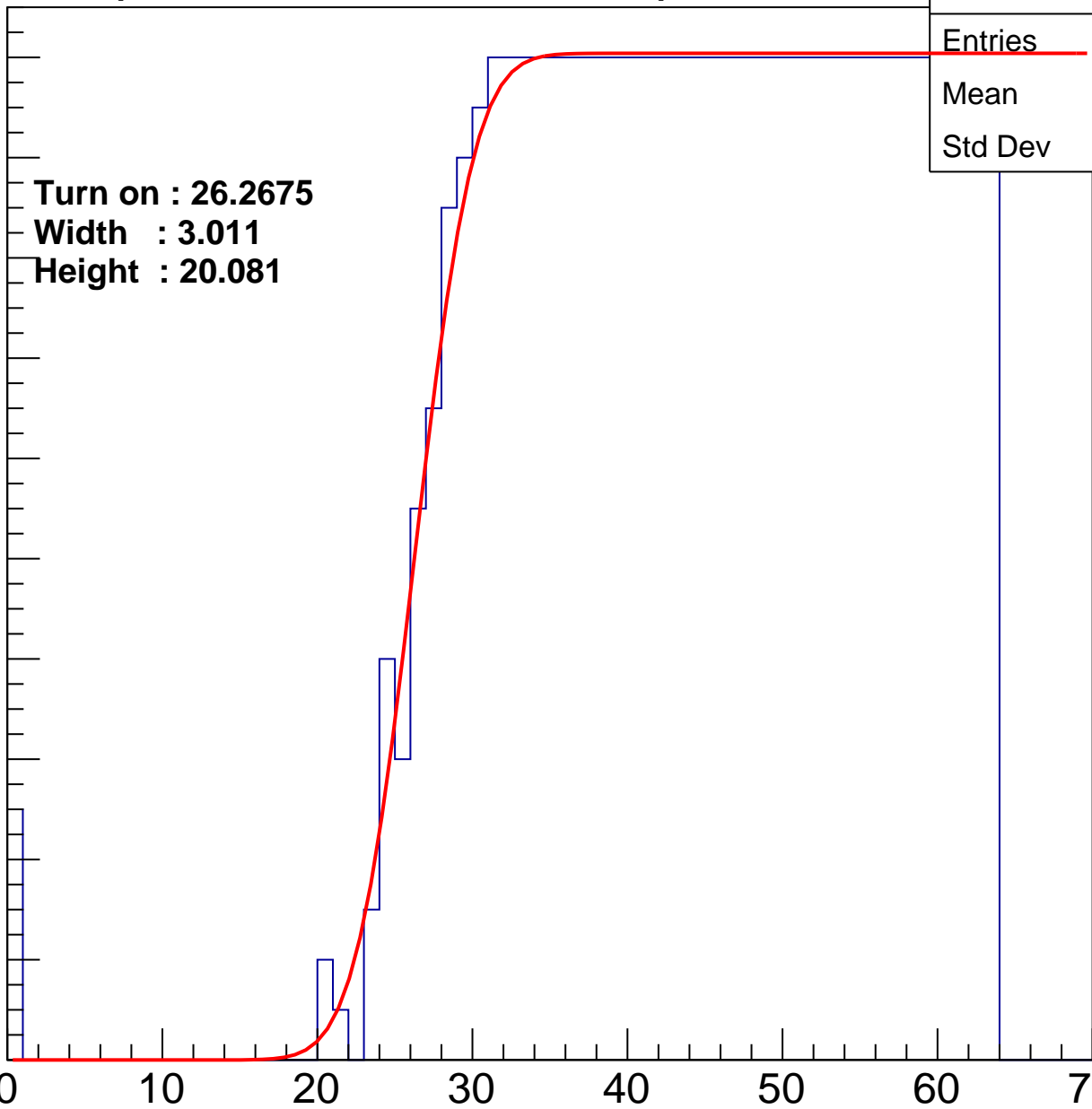
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 26.2675**  
**Width : 3.011**  
**Height : 20.081**

Entries	763
Mean	44.16
Std Dev	11.63

ampl



# B0L101S, U15-ch46

calib\_packv5\_042523\_0143.root, FC#1, port C1

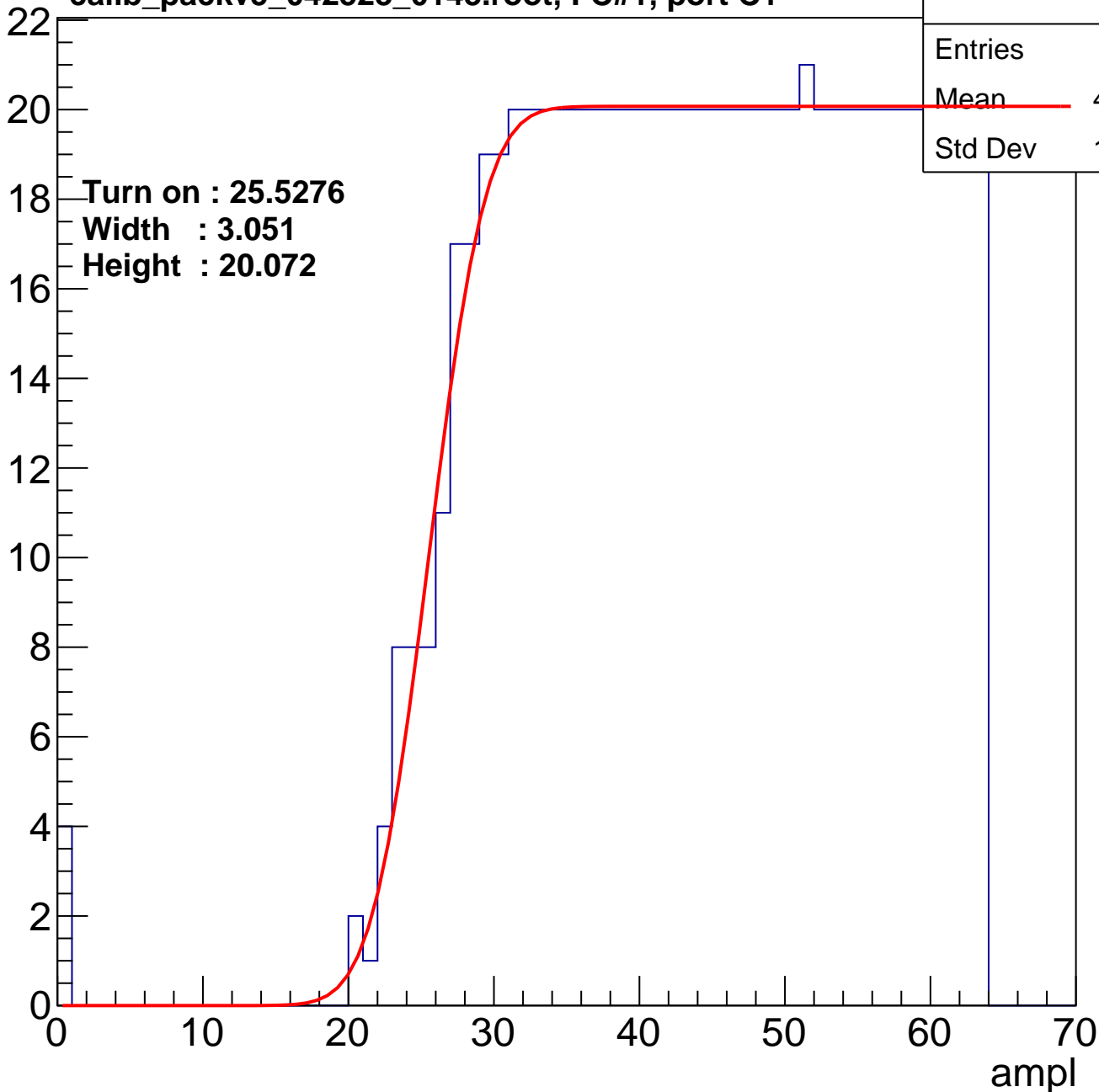
Entries	779
Mean	43.82
Std Dev	11.75

Turn on : 25.5276

Width : 3.051

Height : 20.072

Entry





# B0L101S, U15-ch47

calib\_packv5\_042523\_0143.root, FC#1, port C1

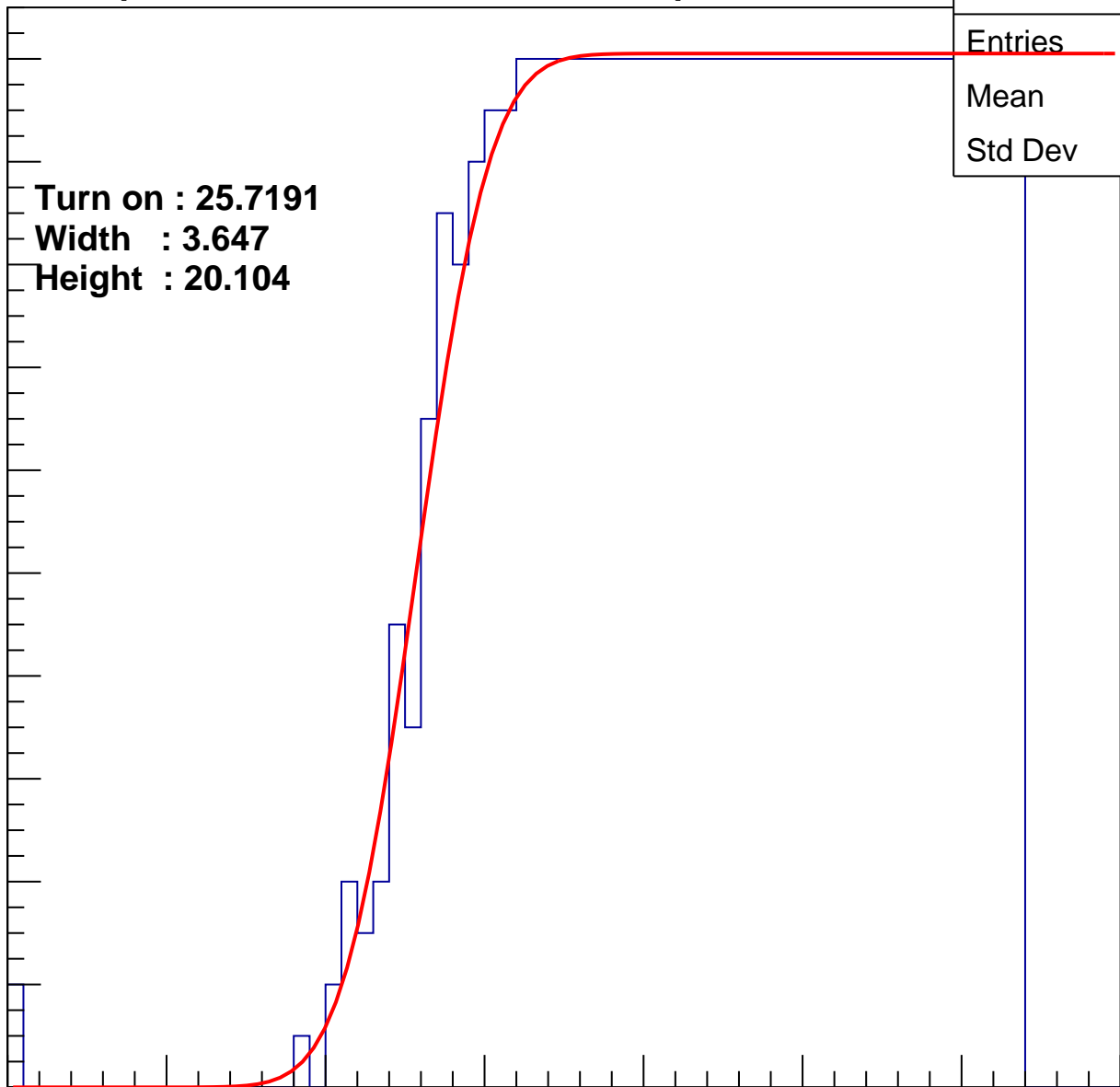
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 25.7191  
Width : 3.647  
Height : 20.104

Entries	774
Mean	43.95
Std Dev	11.58

ampl



# B0L101S, U15-ch48

calib\_packv5\_042523\_0143.root, FC#1, port C1

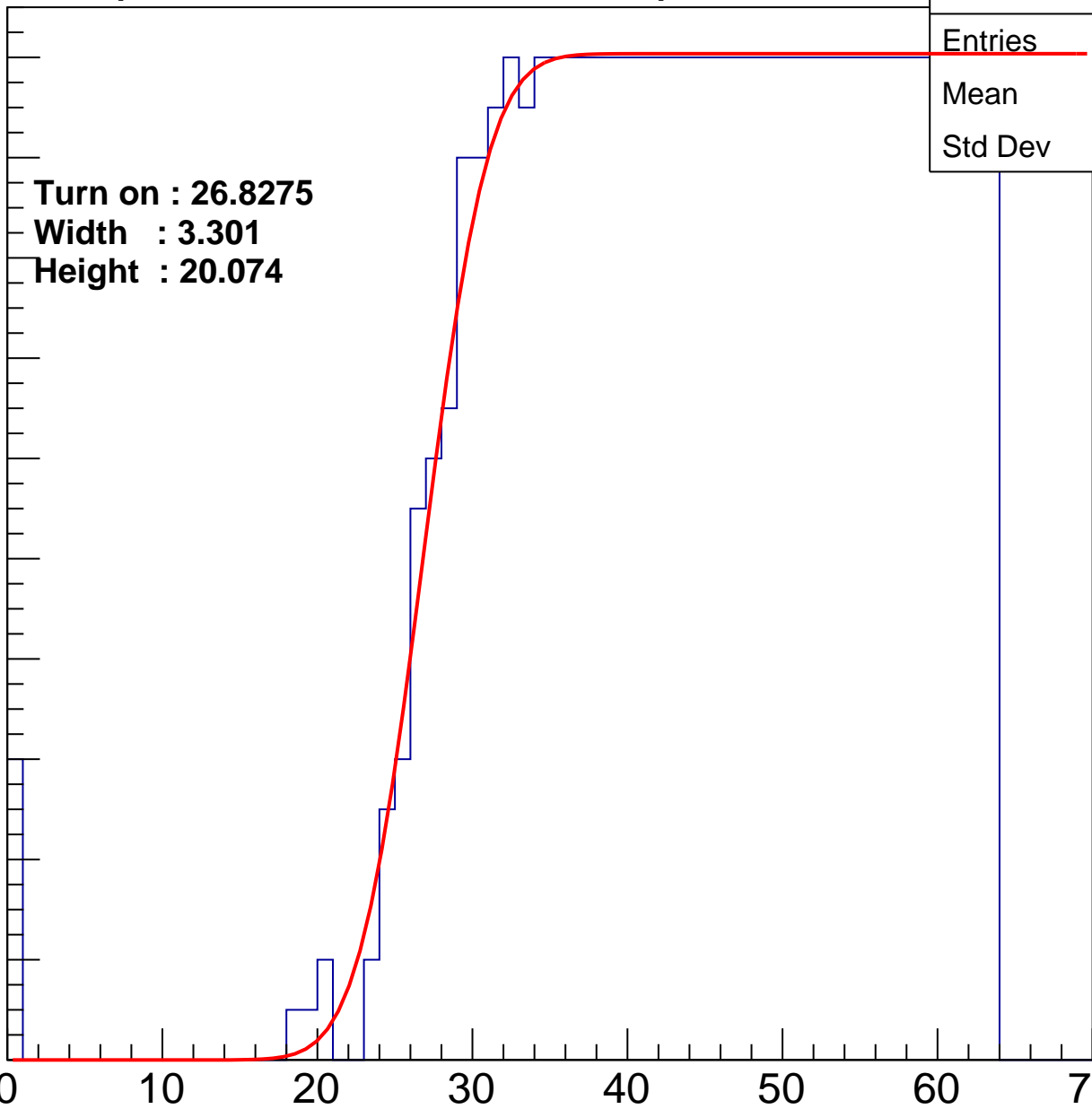
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 26.8275**  
**Width : 3.301**  
**Height : 20.074**

Entries	753
Mean	44.34
Std Dev	11.66

ampl



# B0L101S, U15-ch49

calib\_packv5\_042523\_0143.root, FC#1, port C1

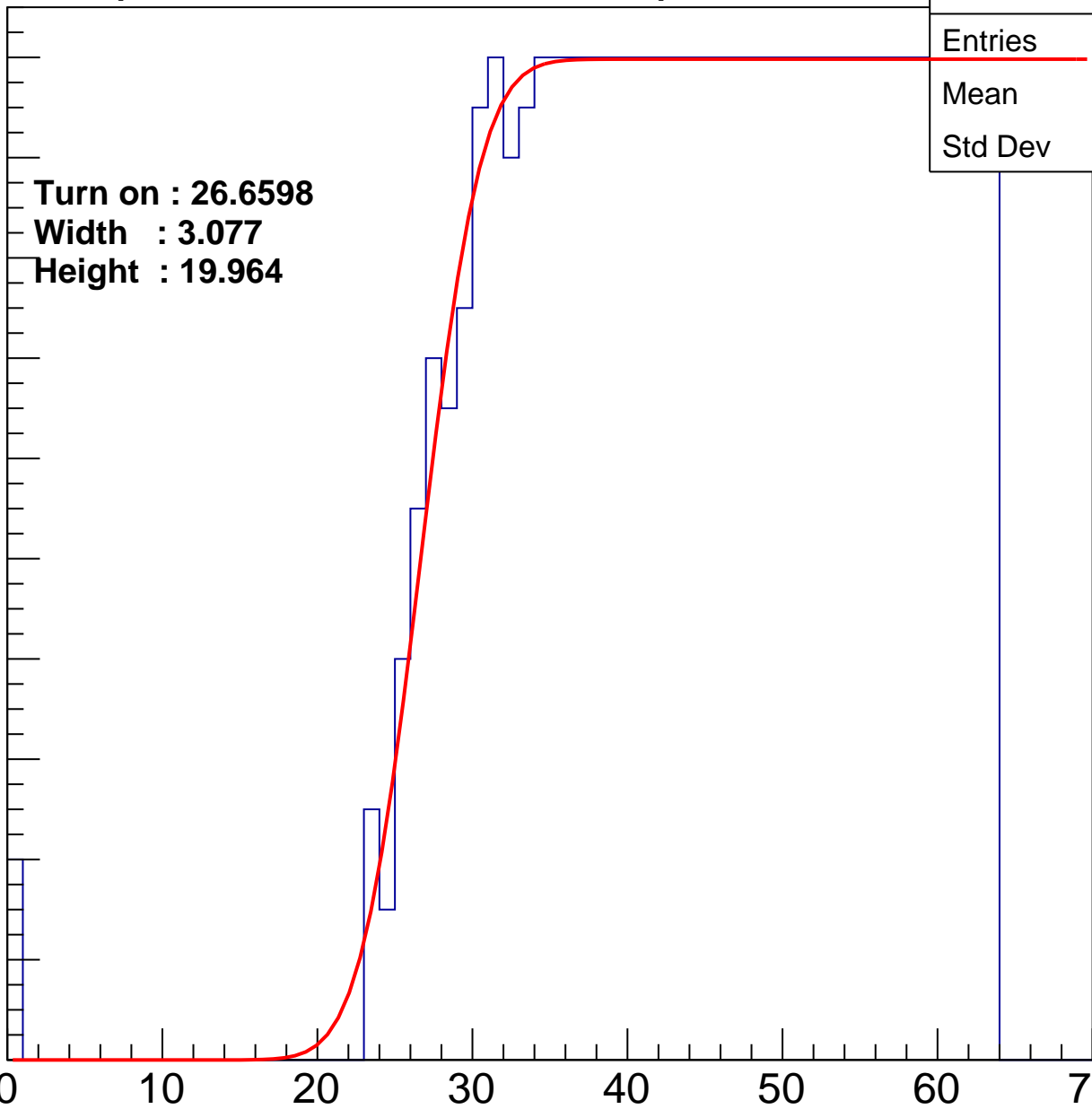
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 26.6598**  
**Width : 3.077**  
**Height : 19.964**

Entries	749
Mean	44.52
Std Dev	11.39

ampl



# B0L101S, U15-ch50

calib\_packv5\_042523\_0143.root, FC#1, port C1

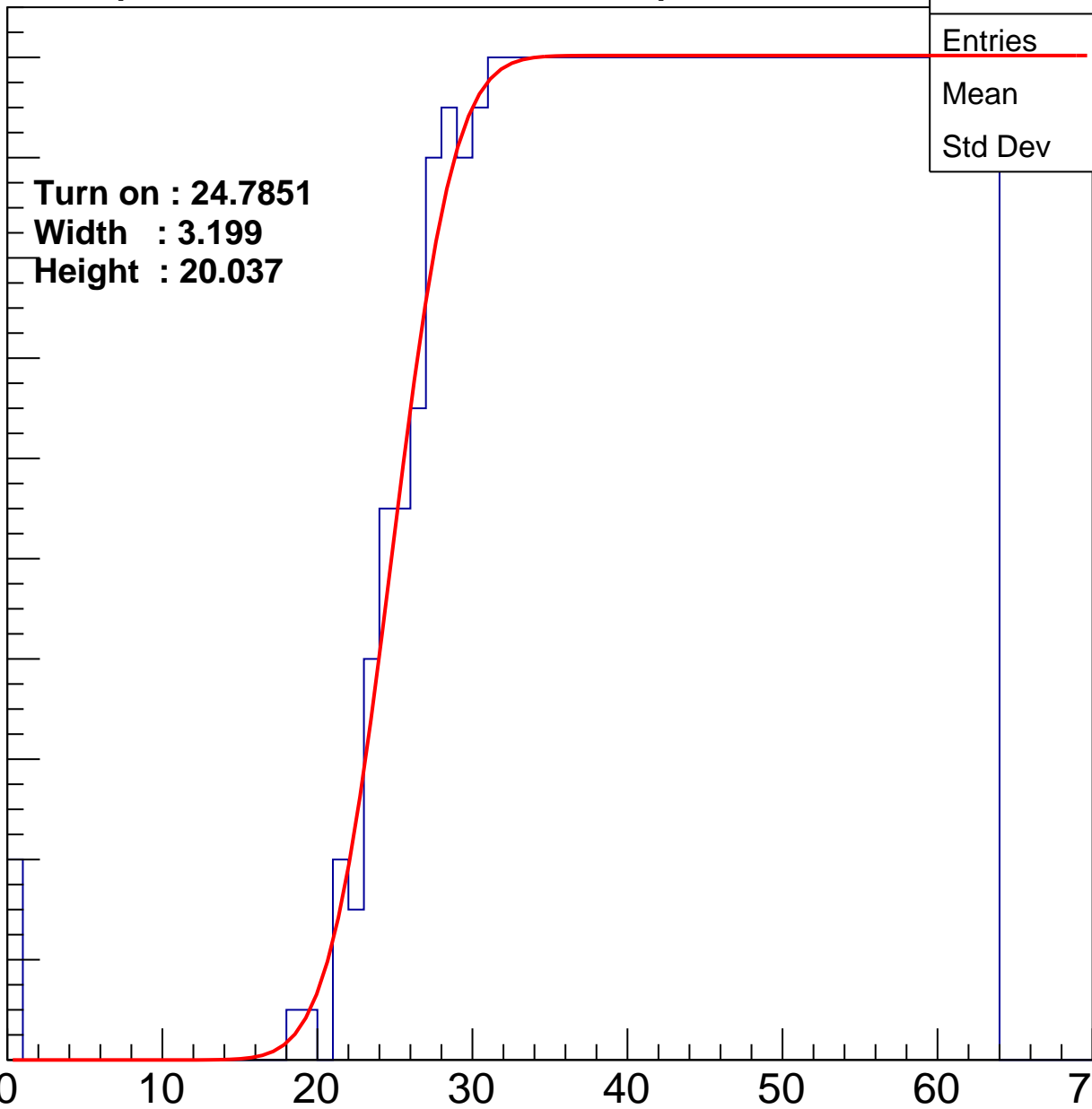
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 24.7851**  
**Width : 3.199**  
**Height : 20.037**

Entries	790
Mean	43.52
Std Dev	11.92

ampl



# B0L101S, U15-ch51

calib\_packv5\_042523\_0143.root, FC#1, port C1

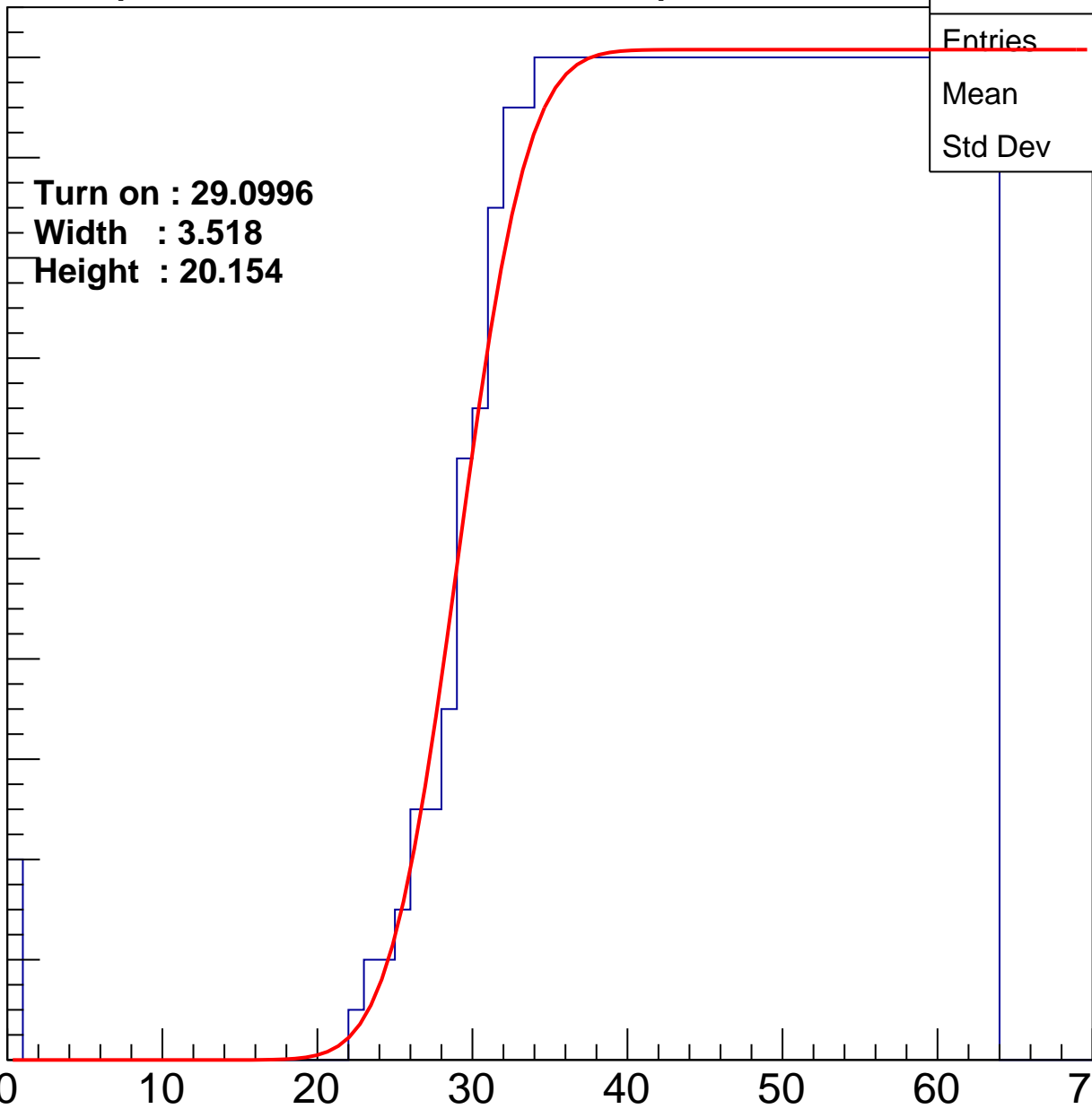
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 29.0996**  
**Width : 3.518**  
**Height : 20.154**

Entries	709
Mean	45.49
Std Dev	10.92

ampl



# B0L101S, U15-ch52

calib\_packv5\_042523\_0143.root, FC#1, port C1

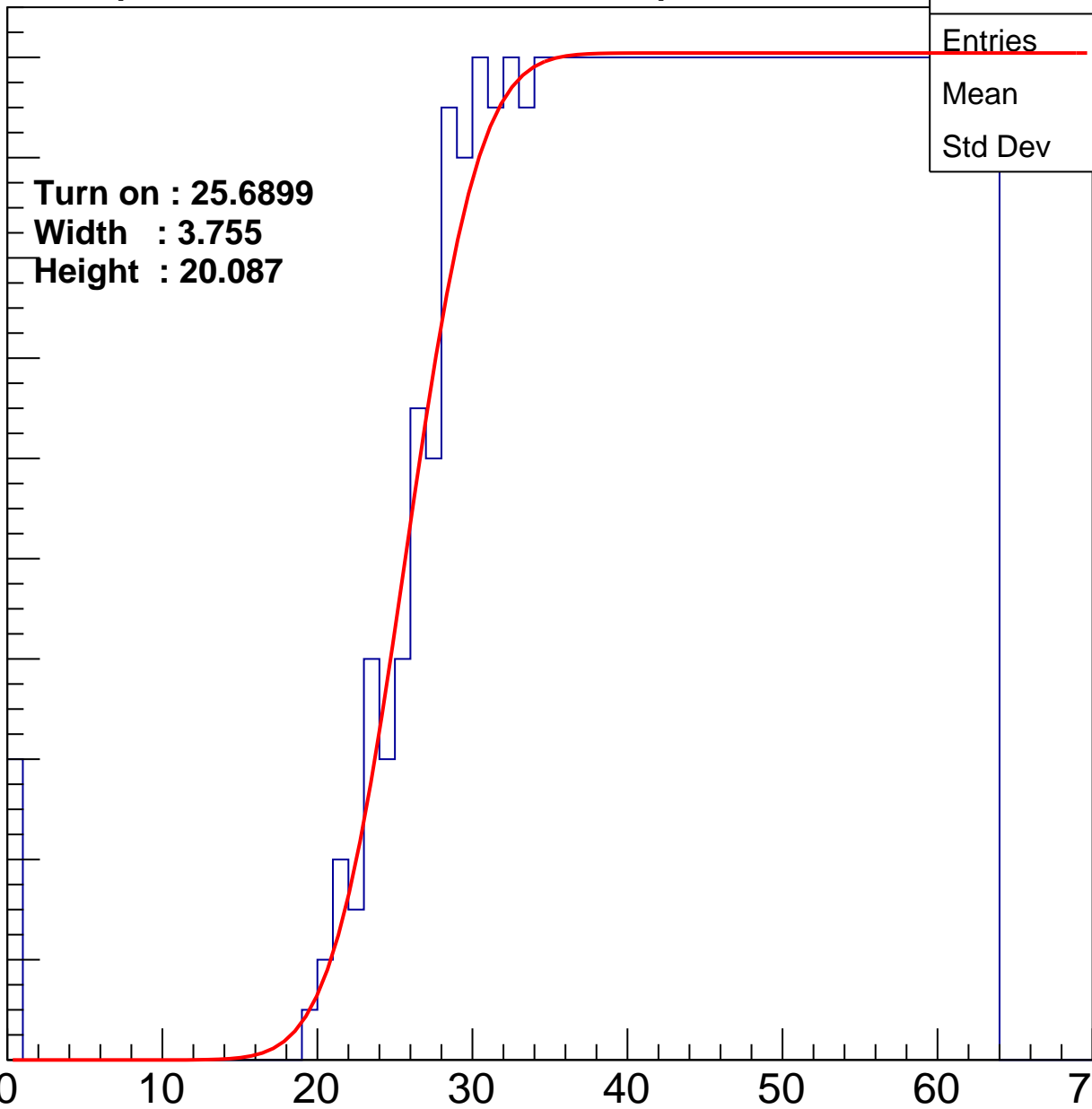
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 25.6899  
Width : 3.755  
Height : 20.087

Entries	778
Mean	43.71
Std Dev	11.98

ampl



# B0L101S, U15-ch53

calib\_packv5\_042523\_0143.root, FC#1, port C1

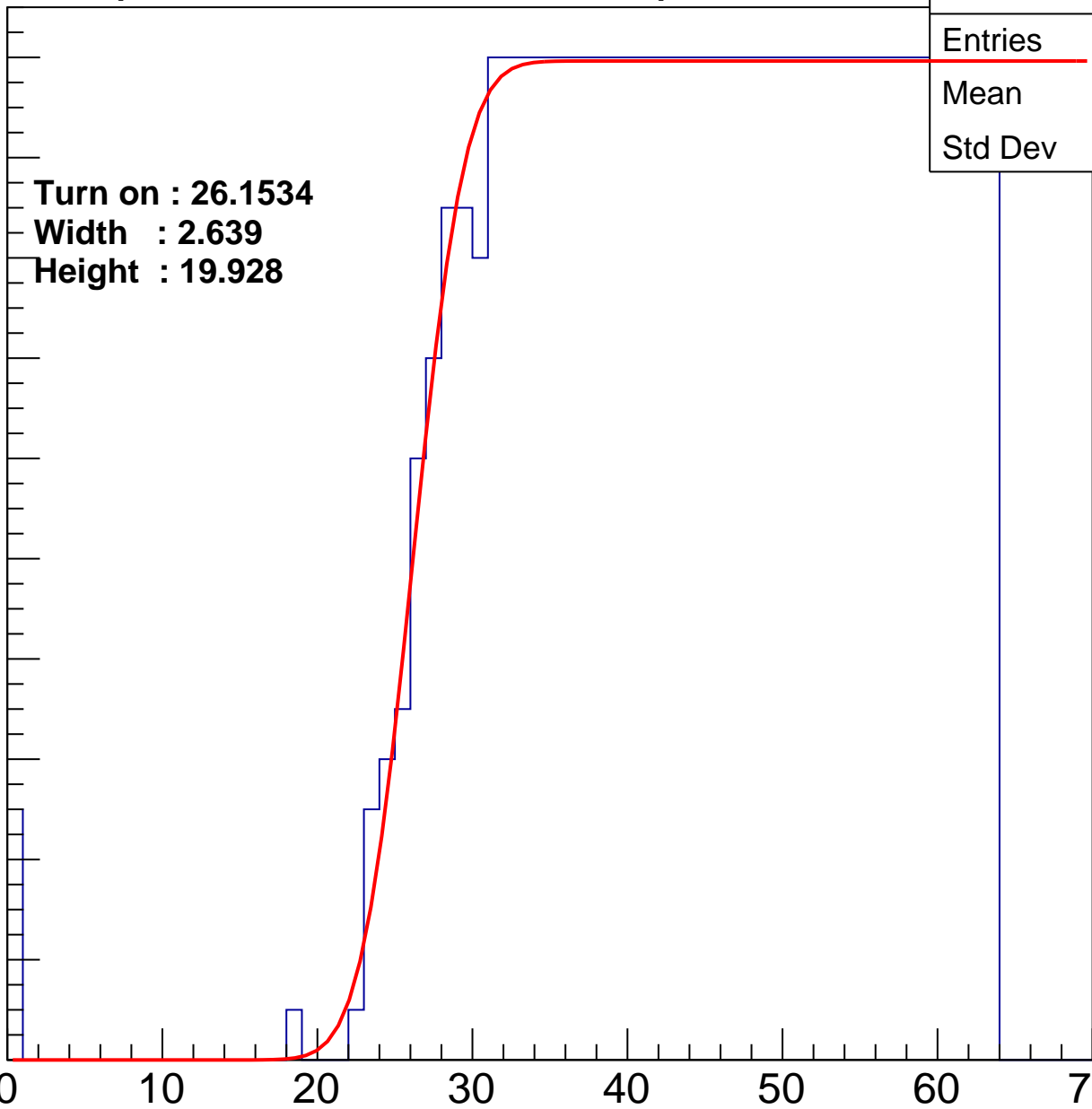
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 26.1534**  
**Width : 2.639**  
**Height : 19.928**

Entries	761
Mean	44.2
Std Dev	11.63

ampl



# B0L101S, U15-ch54

calib\_packv5\_042523\_0143.root, FC#1, port C1

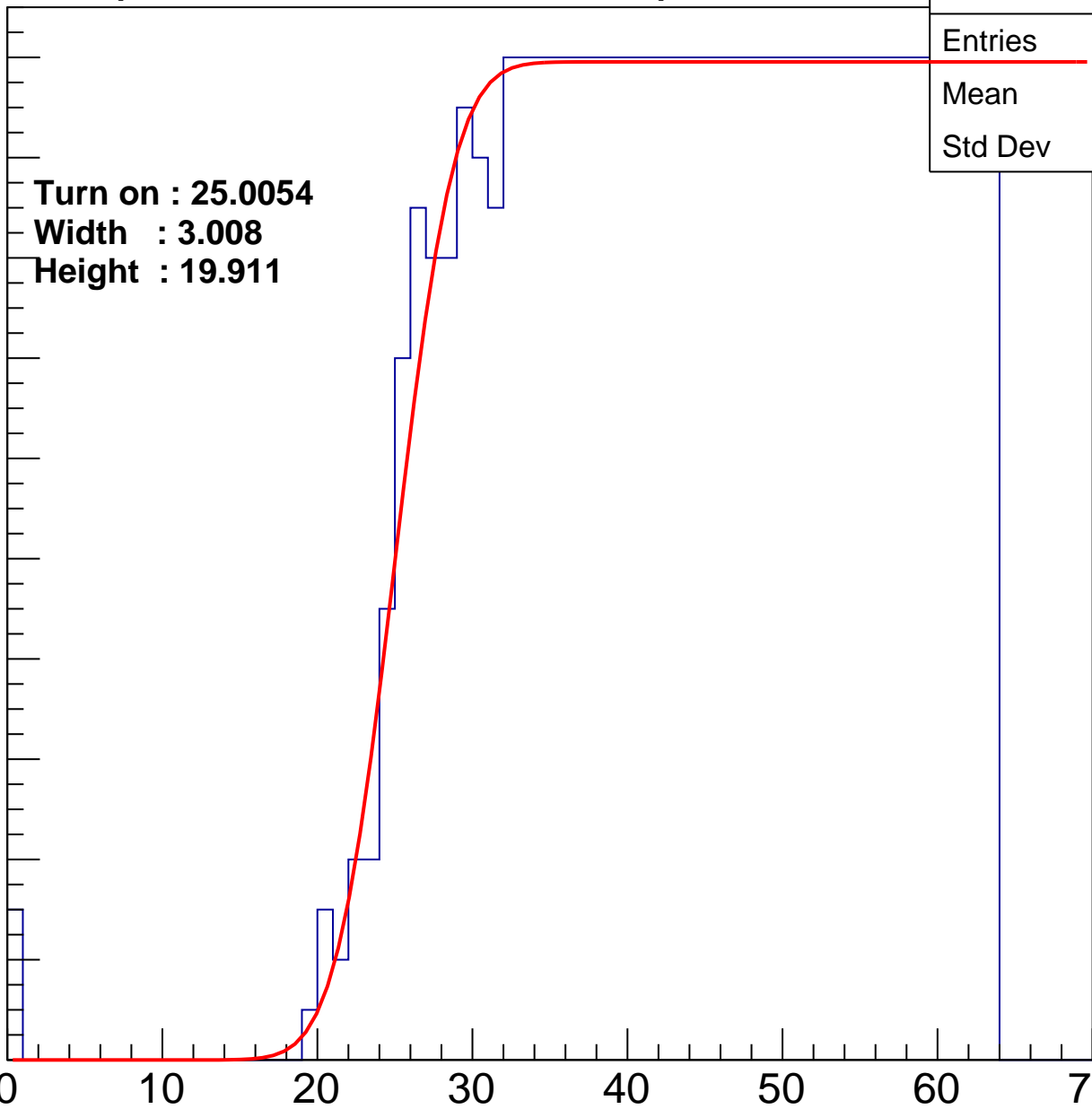
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 25.0054  
Width : 3.008  
Height : 19.911

Entries	783
Mean	43.69
Std Dev	11.79

ampl





# B0L101S, U15-ch55

calib\_packv5\_042523\_0143.root, FC#1, port C1

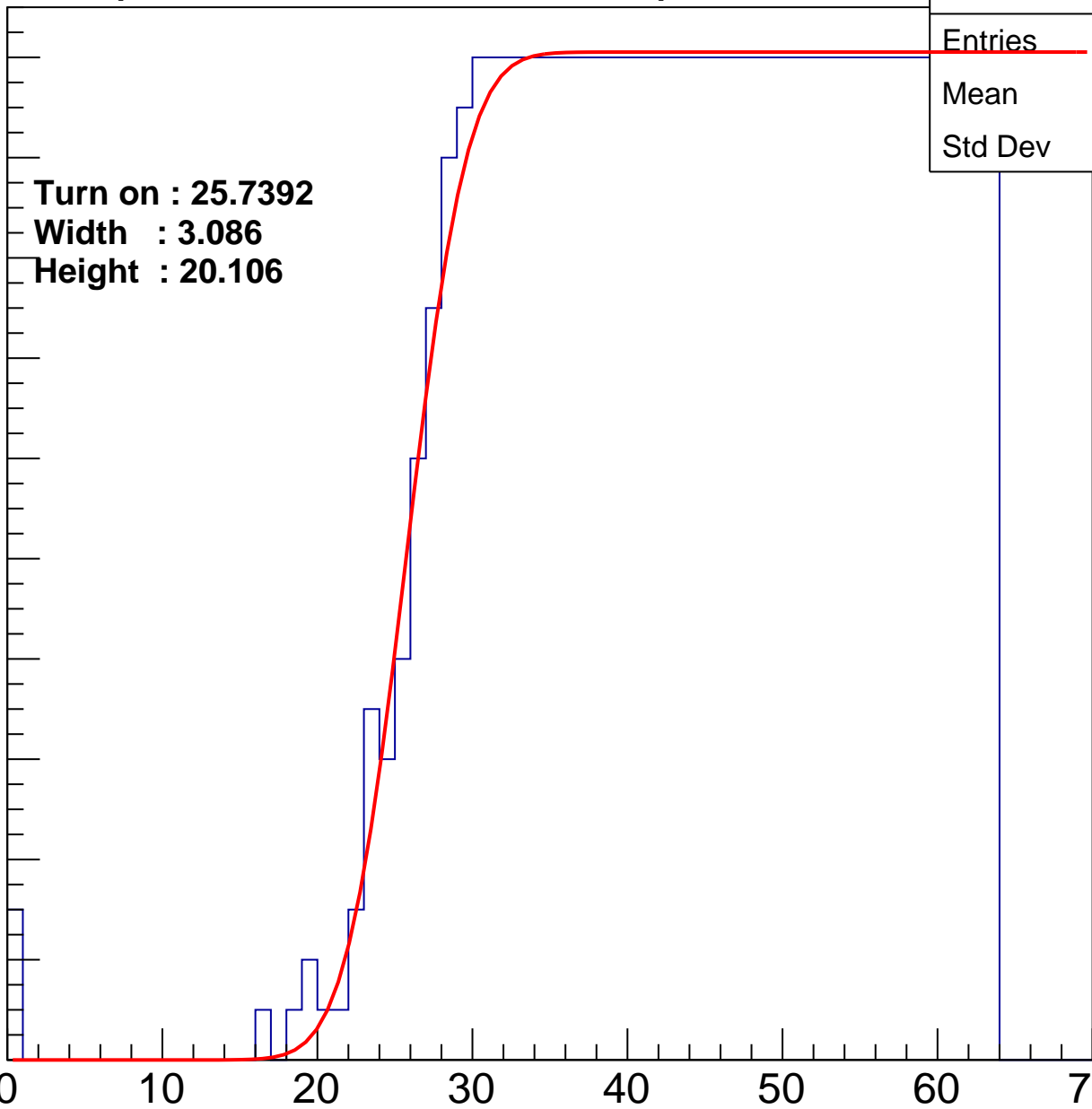
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 25.7392  
Width : 3.086  
Height : 20.106

Entries	777
Mean	43.86
Std Dev	11.69

ampl



# B0L101S, U15-ch56

calib\_packv5\_042523\_0143.root, FC#1, port C1

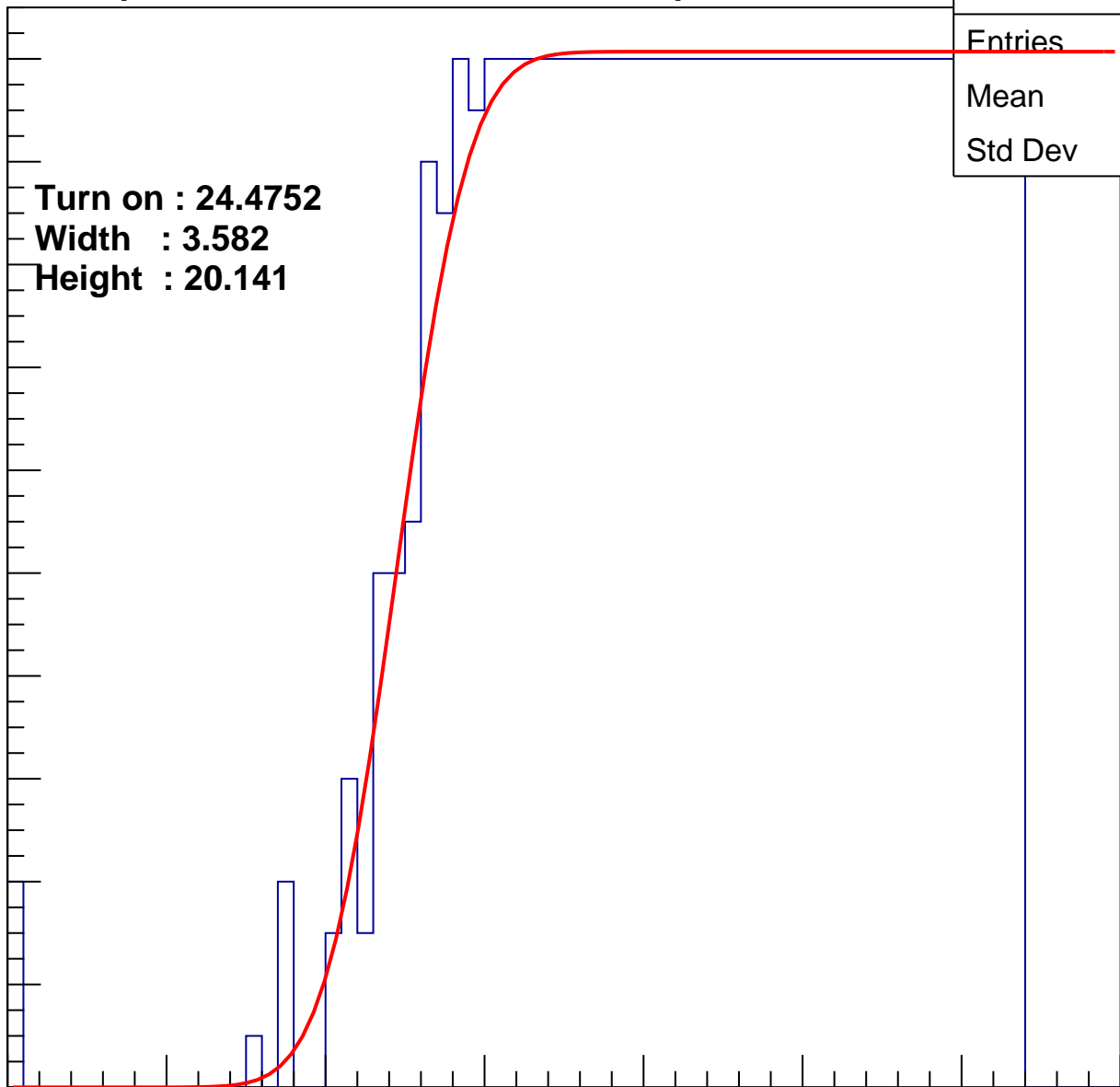
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 24.4752  
Width : 3.582  
Height : 20.141

Entries	806
Mean	43.1
Std Dev	12.17

ampl



# B0L101S, U15-ch57

calib\_packv5\_042523\_0143.root, FC#1, port C1

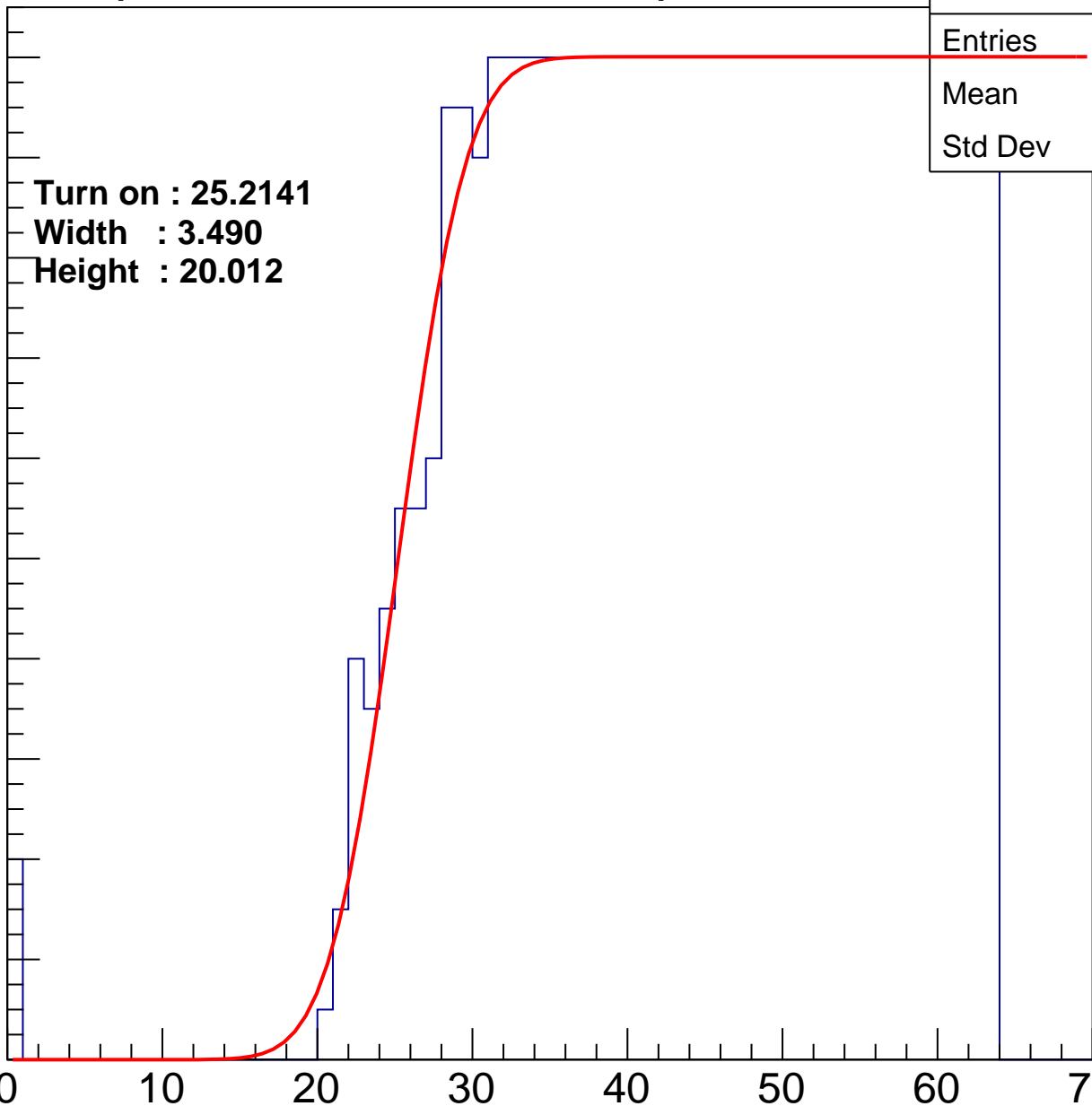
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 25.2141  
Width : 3.490  
Height : 20.012

Entries	782
Mean	43.69
Std Dev	11.85

ampl



# B0L101S, U15-ch58

calib\_packv5\_042523\_0143.root, FC#1, port C1

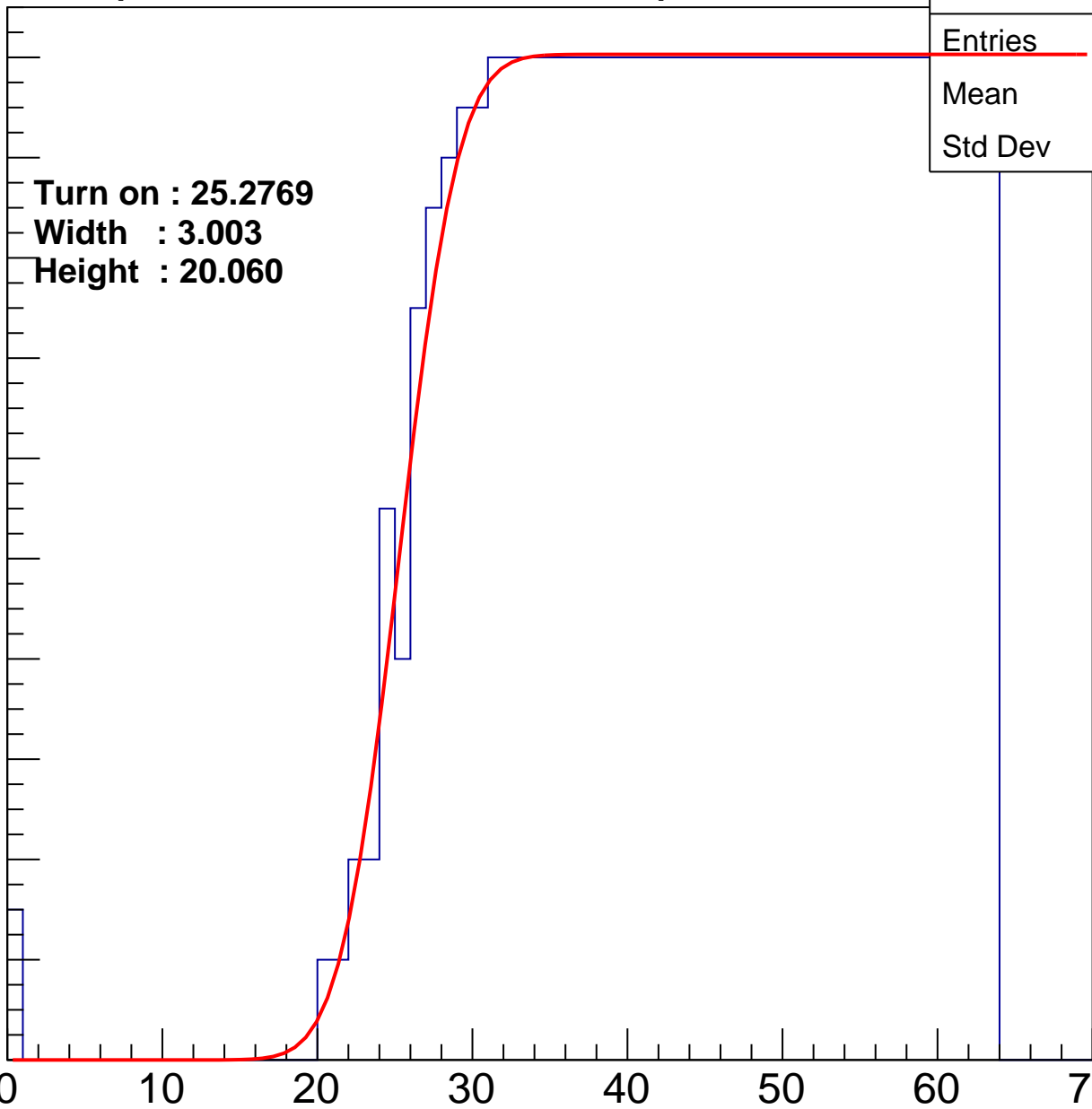
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 25.2769  
Width : 3.003  
Height : 20.060

Entries	782
Mean	43.76
Std Dev	11.7

ampl



# B0L101S, U15-ch59

calib\_packv5\_042523\_0143.root, FC#1, port C1

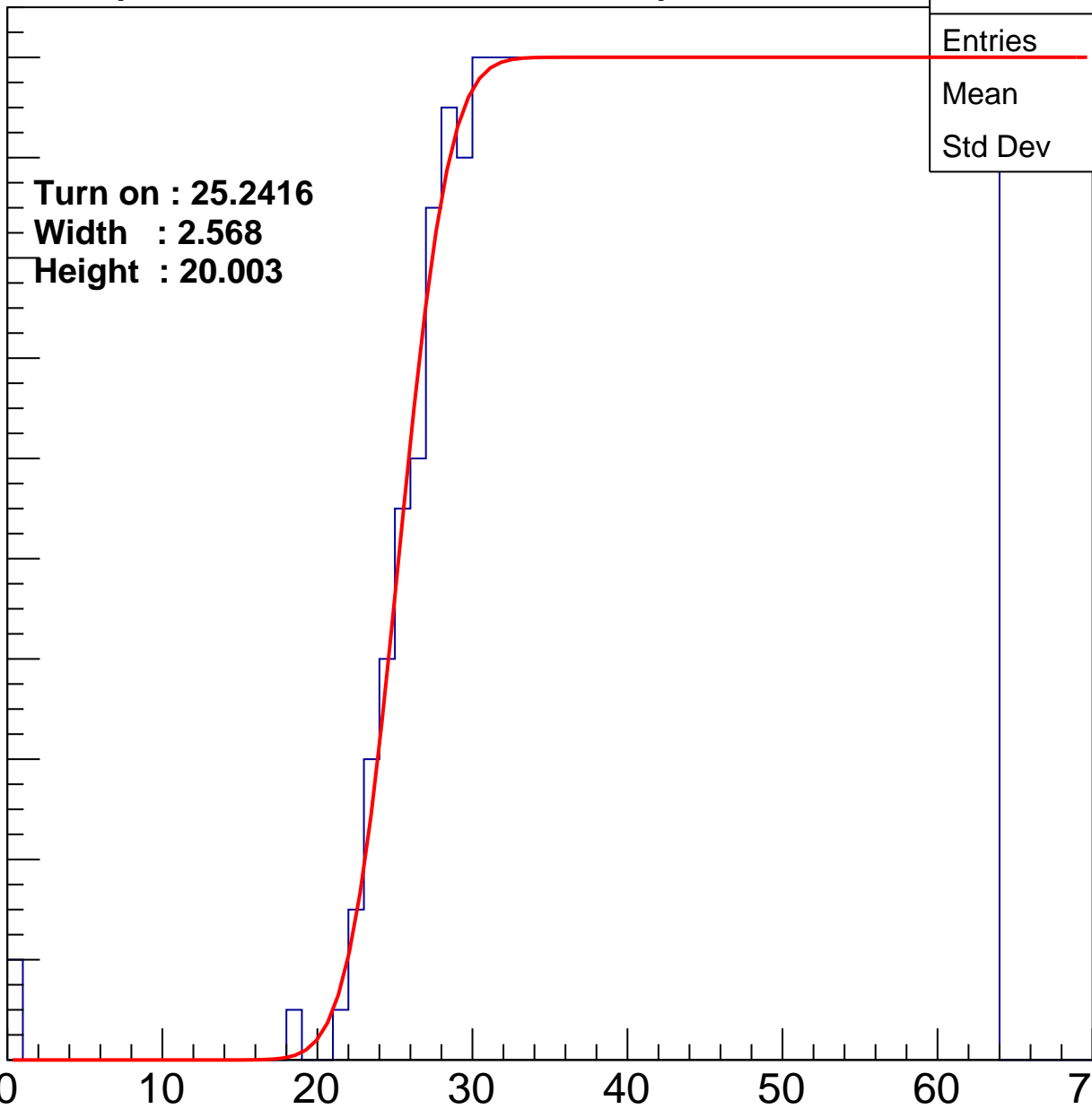
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 25.2416**  
**Width : 2.568**  
**Height : 20.003**

Entries	778
Mean	43.9
Std Dev	11.55

ampl



# B0L101S, U15-ch60

calib\_packv5\_042523\_0143.root, FC#1, port C1

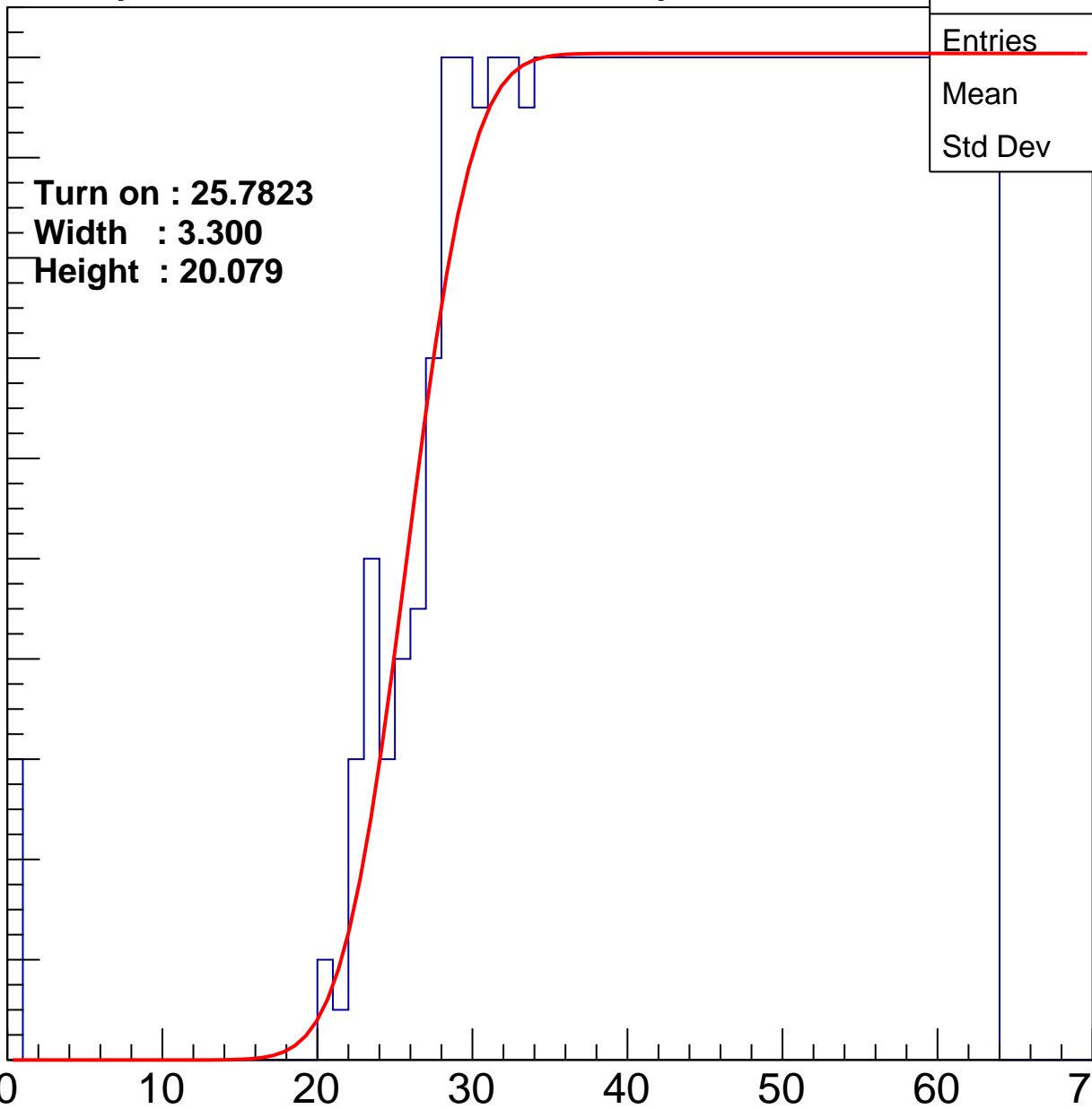
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 25.7823  
Width : 3.300  
Height : 20.079

Entries	780
Mean	43.69
Std Dev	11.97

ampl



# B0L101S, U15-ch61

calib\_packv5\_042523\_0143.root, FC#1, port C1

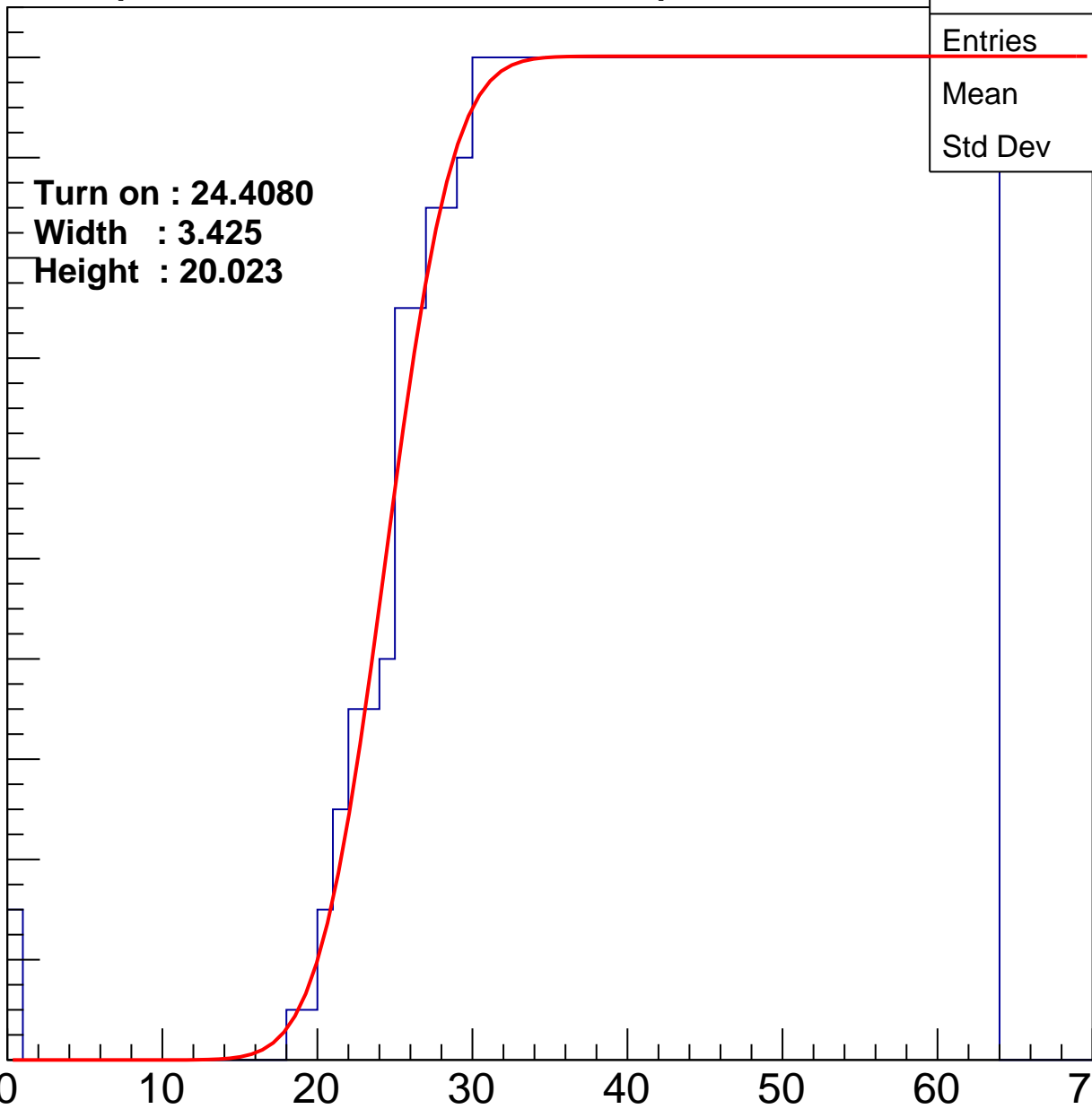
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 24.4080**  
**Width : 3.425**  
**Height : 20.023**

Entries	797
Mean	43.35
Std Dev	11.97

ampl



# B0L101S, U15-ch62

calib\_packv5\_042523\_0143.root, FC#1, port C1

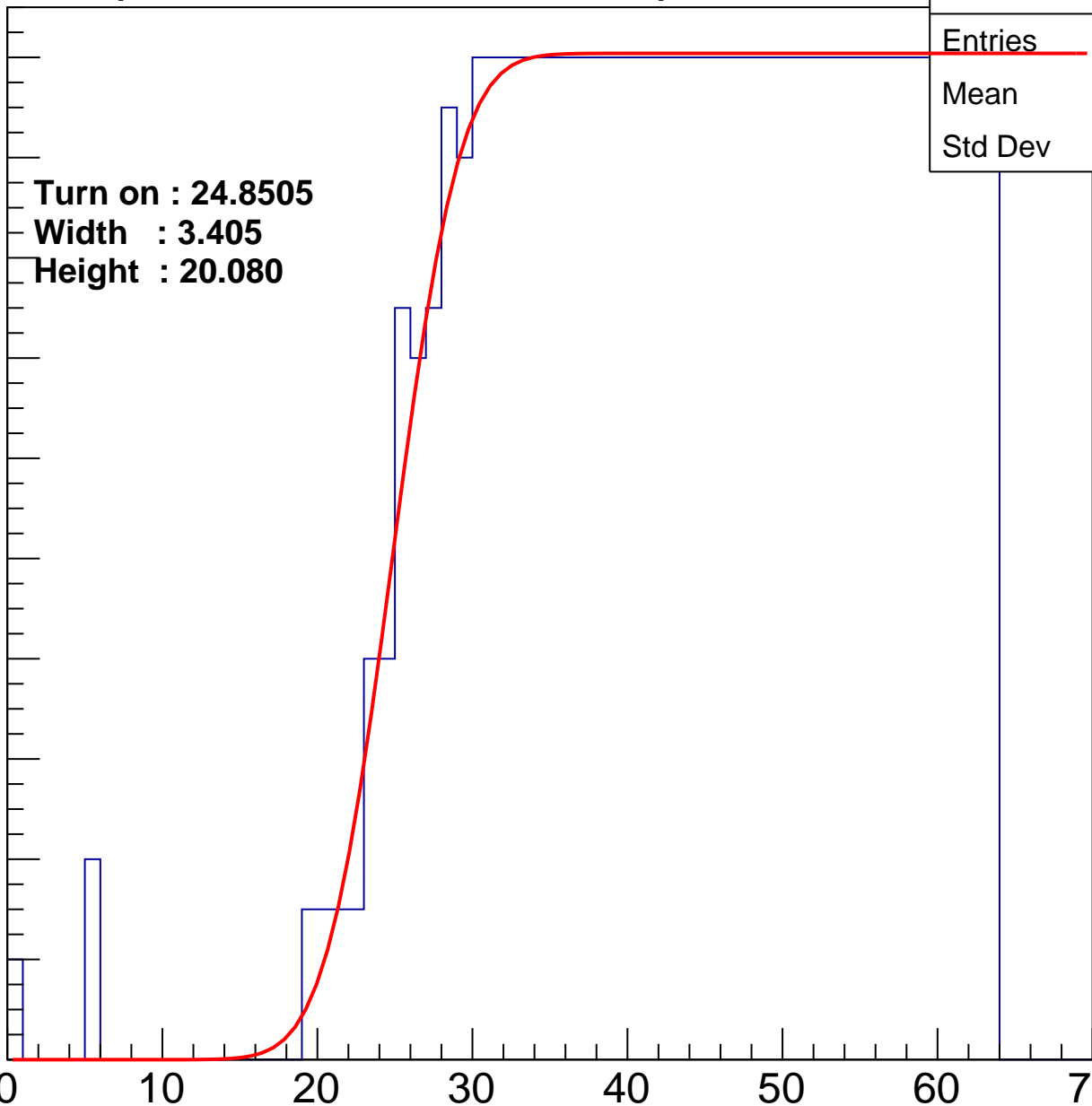
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 24.8505**  
**Width : 3.405**  
**Height : 20.080**

Entries	795
Mean	43.35
Std Dev	12.07

ampl





# B0L101S, U15-ch63

calib\_packv5\_042523\_0143.root, FC#1, port C1

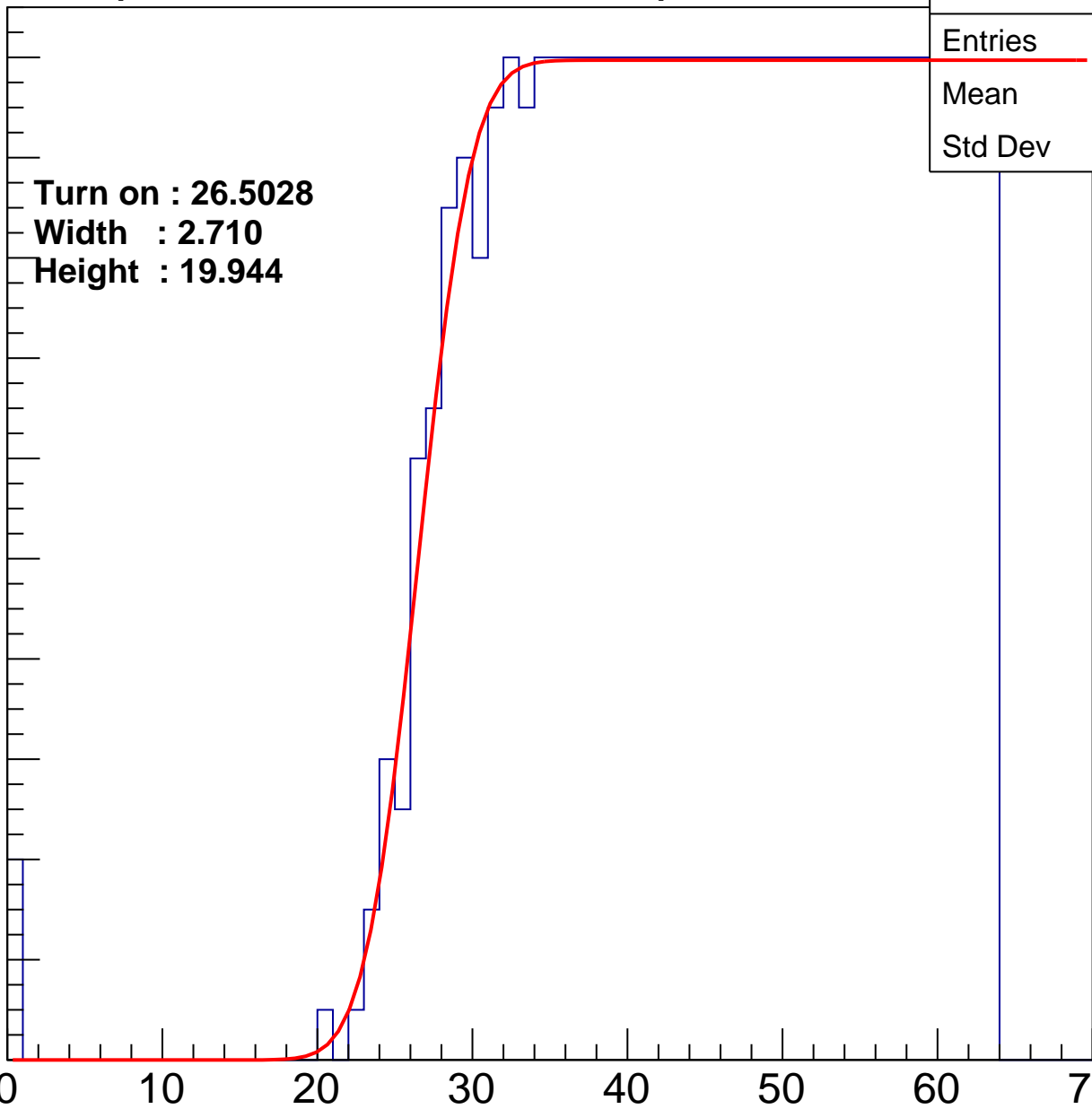
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 26.5028**  
**Width : 2.710**  
**Height : 19.944**

Entries	754
Mean	44.4
Std Dev	11.45

ampl



# B0L101S, U15-ch64

calib\_packv5\_042523\_0143.root, FC#1, port C1

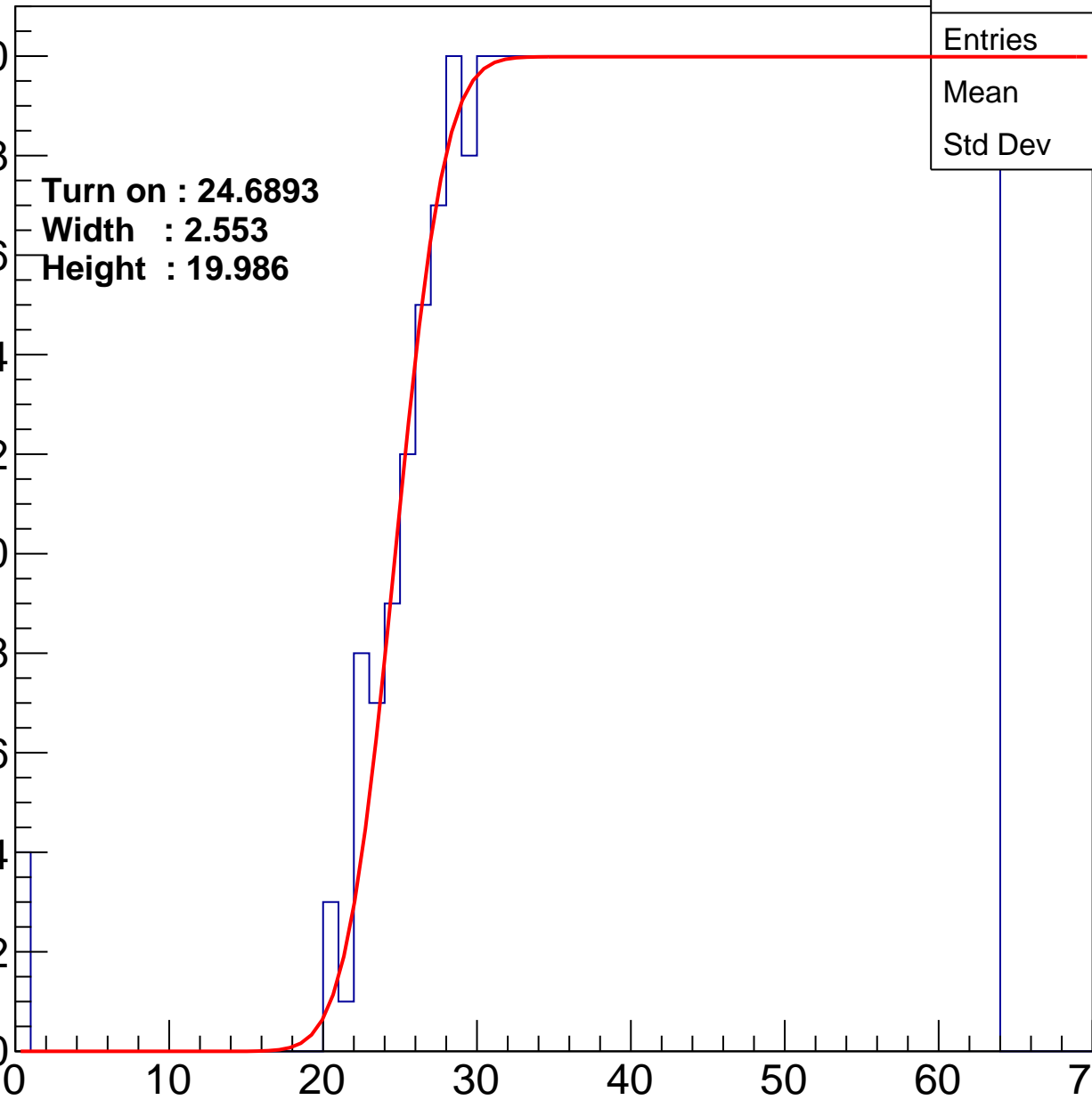
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 24.6893**  
**Width : 2.553**  
**Height : 19.986**

Entries	794
Mean	43.43
Std Dev	11.94

ampl



# B0L101S, U15-ch65

calib\_packv5\_042523\_0143.root, FC#1, port C1

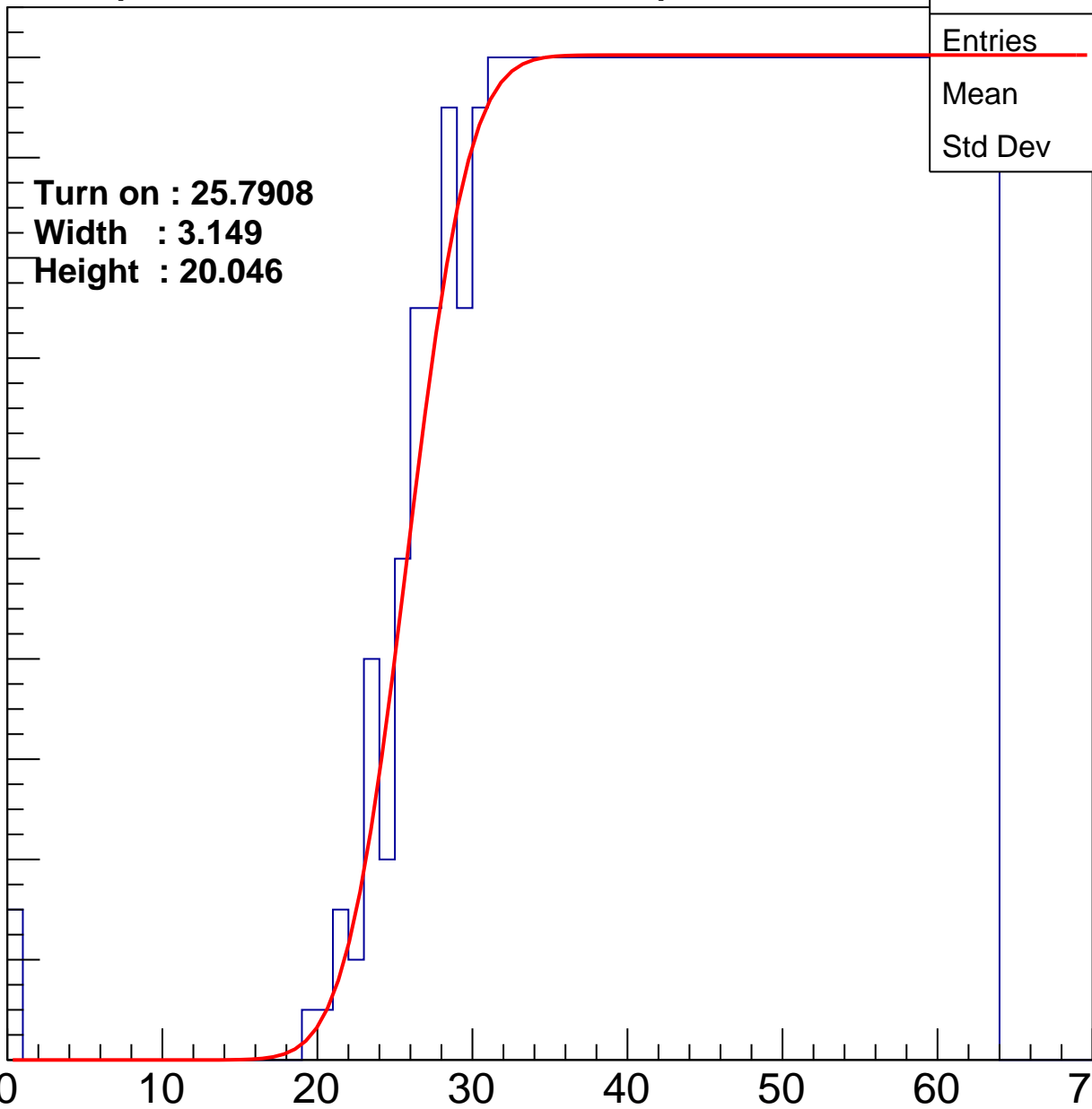
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 25.7908**  
**Width : 3.149**  
**Height : 20.046**

Entries	775
Mean	43.91
Std Dev	11.65

ampl



# B0L101S, U15-ch66

calib\_packv5\_042523\_0143.root, FC#1, port C1

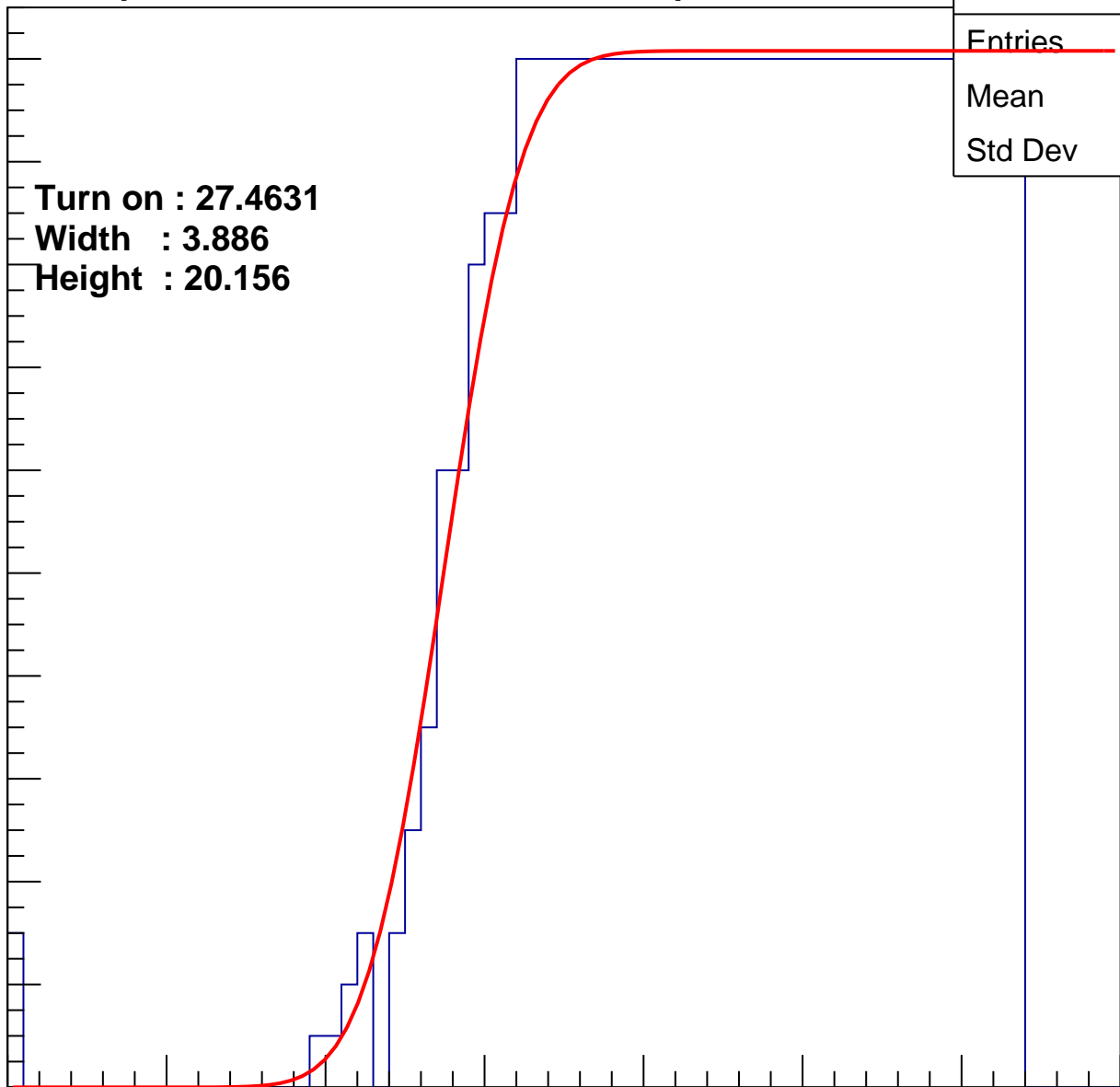
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 27.4631  
Width : 3.886  
Height : 20.156

Entries	739
Mean	44.77
Std Dev	11.22

ampl



# B0L101S, U15-ch67

calib\_packv5\_042523\_0143.root, FC#1, port C1

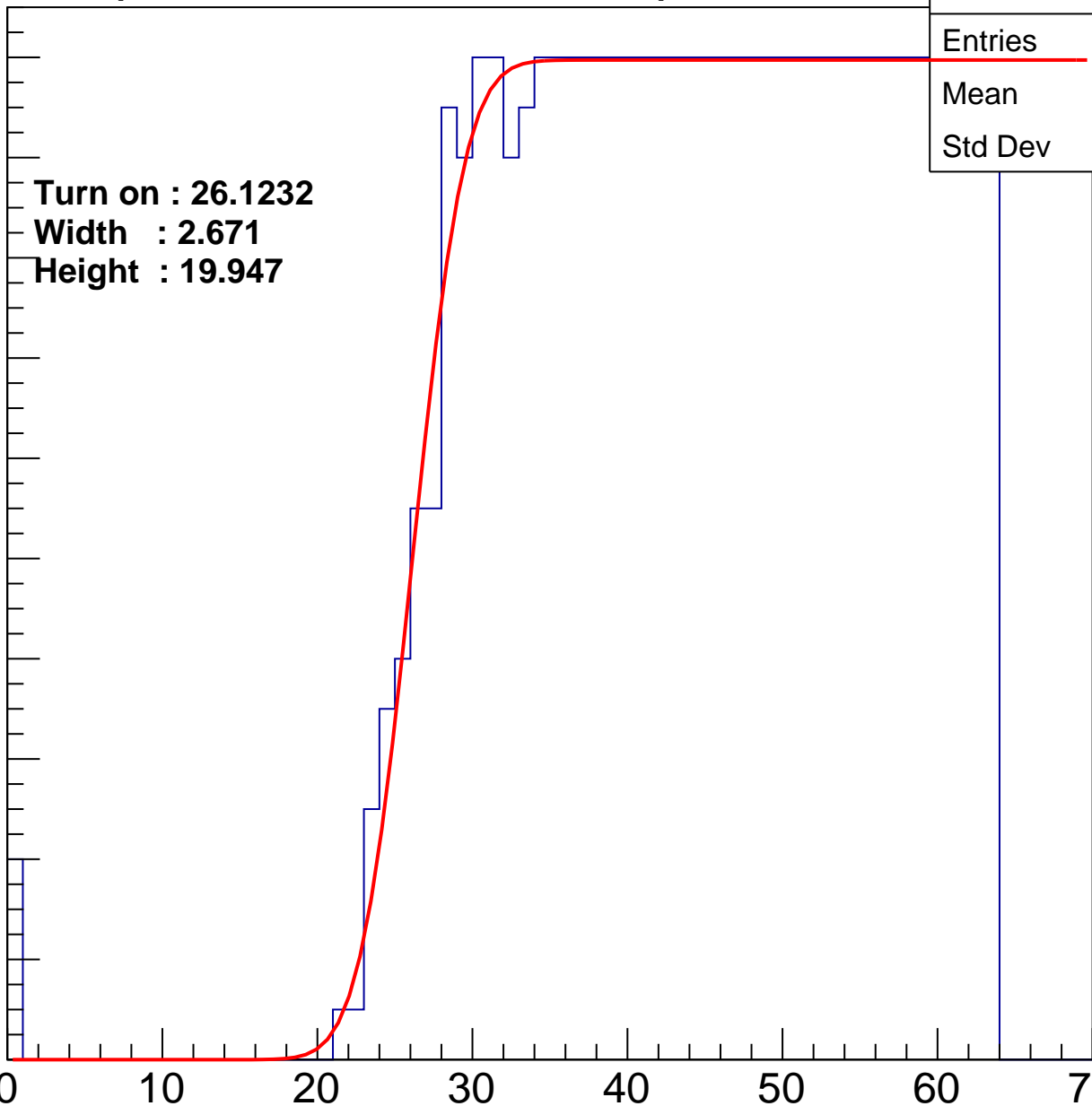
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 26.1232**  
**Width : 2.671**  
**Height : 19.947**

Entries	762
Mean	44.21
Std Dev	11.55

ampl



# B0L101S, U15-ch68

calib\_packv5\_042523\_0143.root, FC#1, port C1

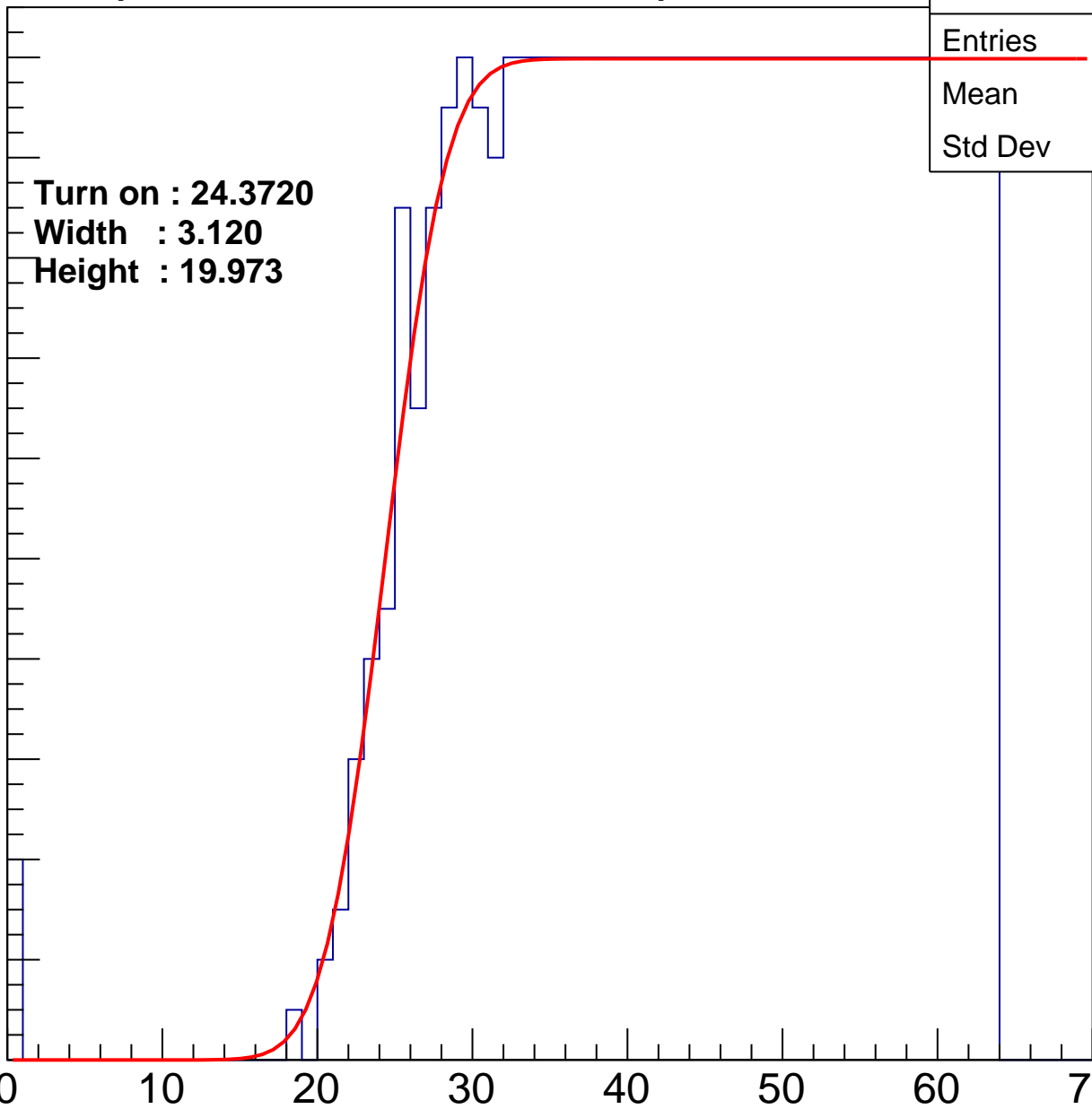
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 24.3720**  
**Width : 3.120**  
**Height : 19.973**

Entries	796
Mean	43.36
Std Dev	12

ampl



# B0L101S, U15-ch69

calib\_packv5\_042523\_0143.root, FC#1, port C1

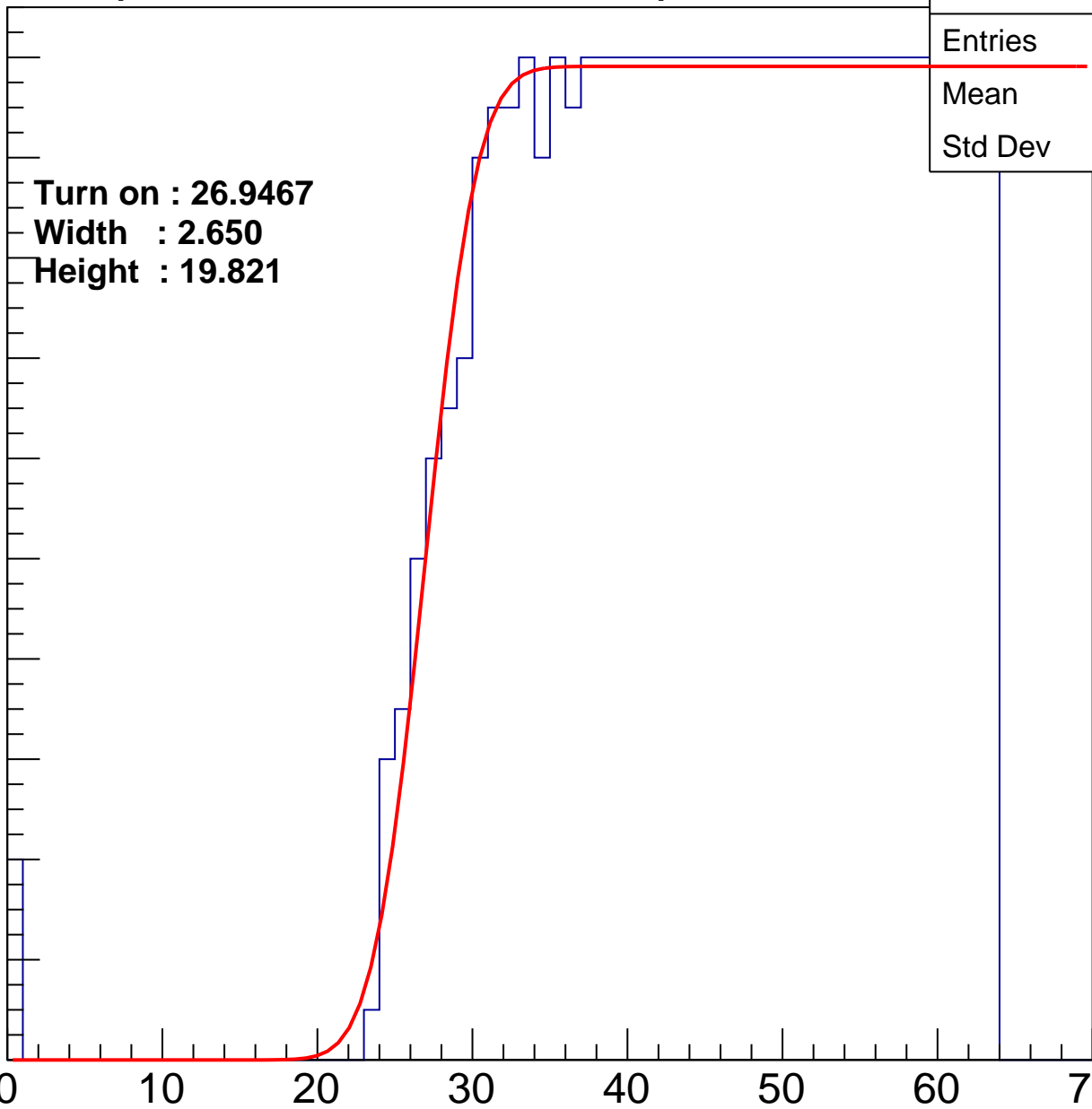
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 26.9467**  
**Width : 2.650**  
**Height : 19.821**

Entries	740
Mean	44.71
Std Dev	11.31

ampl



# B0L101S, U15-ch70

calib\_packv5\_042523\_0143.root, FC#1, port C1

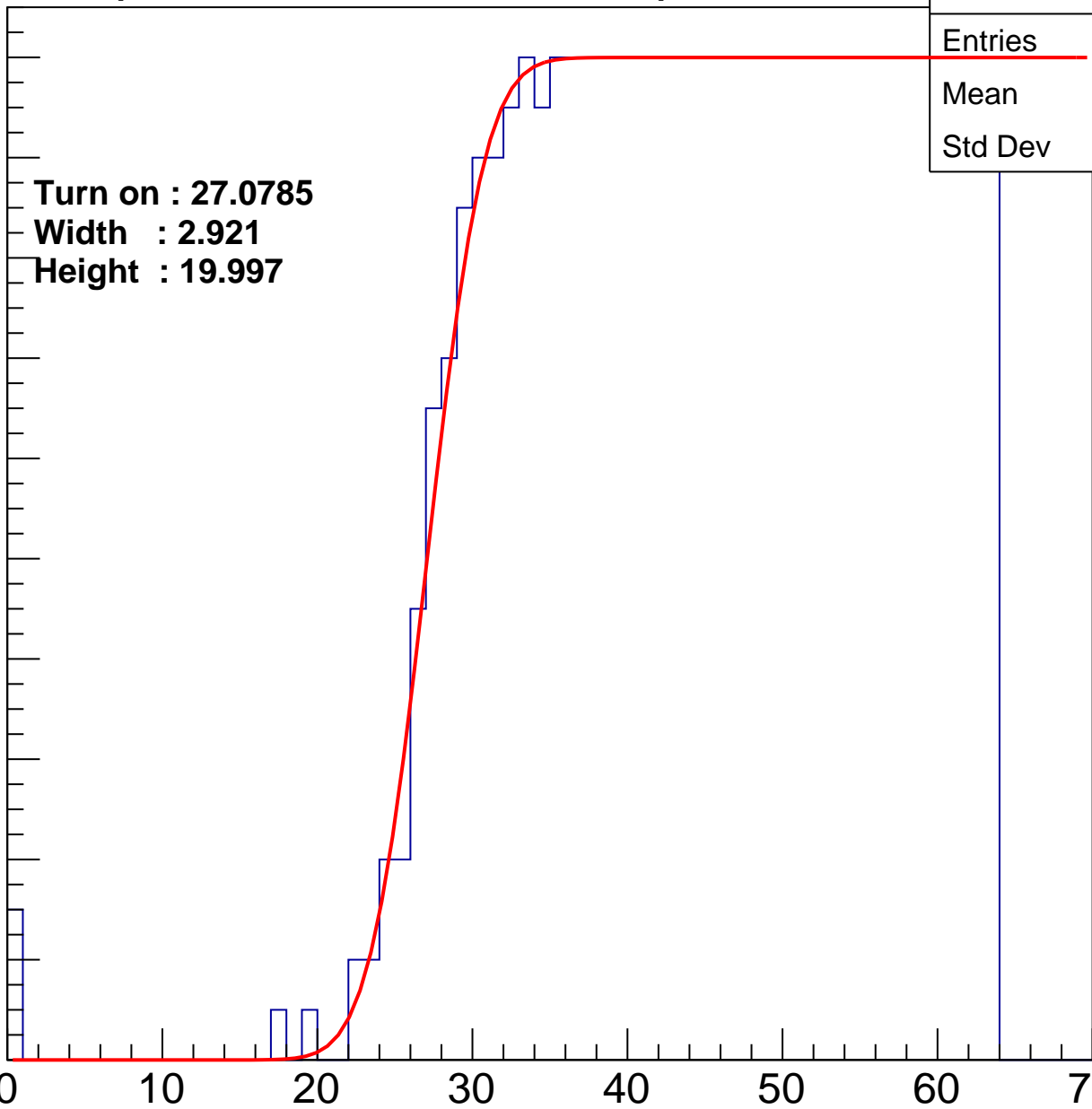
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 27.0785**  
**Width : 2.921**  
**Height : 19.997**

Entries	744
Mean	44.66
Std Dev	11.27

ampl





# B0L101S, U15-ch71

calib\_packv5\_042523\_0143.root, FC#1, port C1

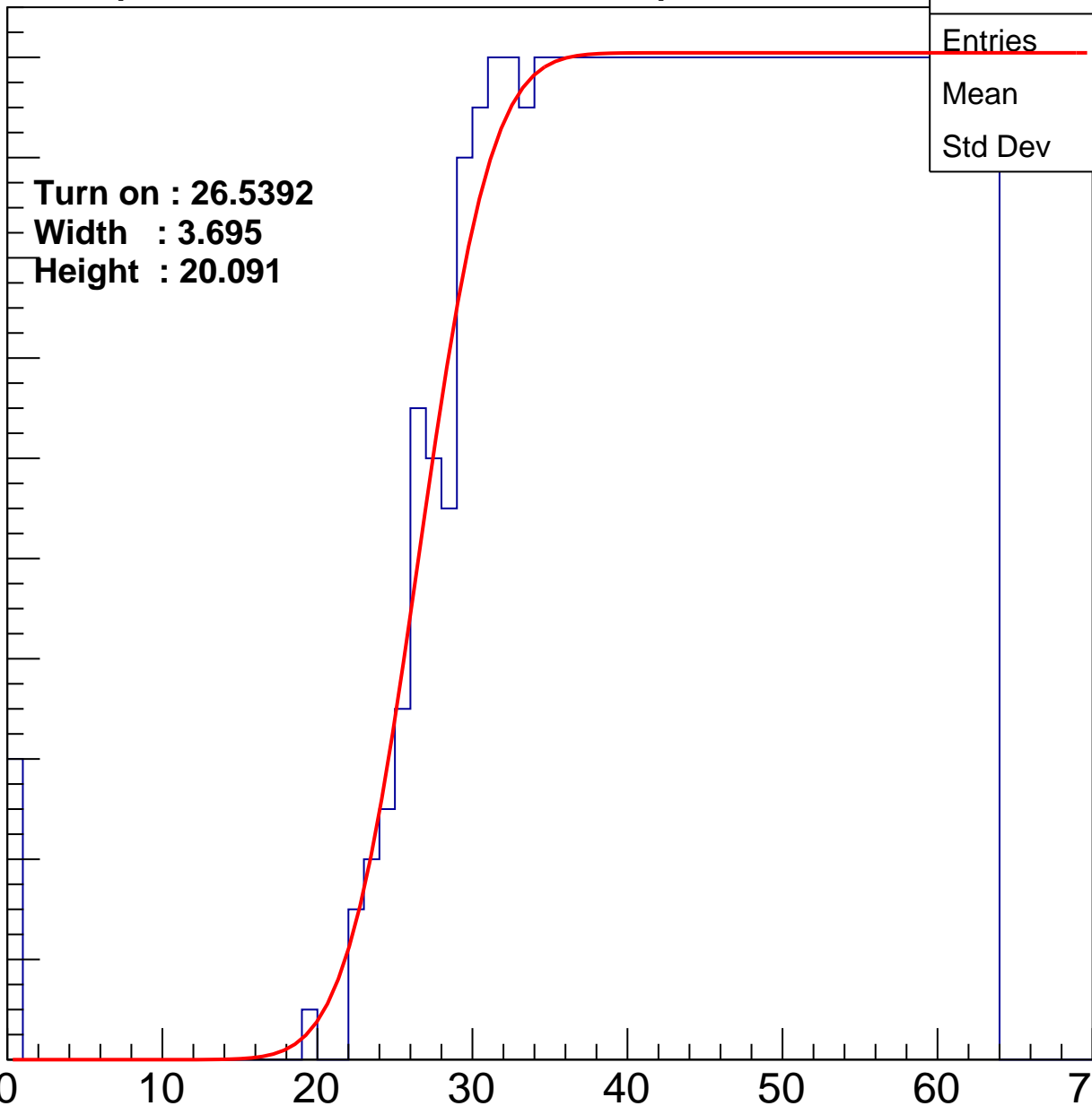
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 26.5392  
Width : 3.695  
Height : 20.091

Entries	758
Mean	44.22
Std Dev	11.71

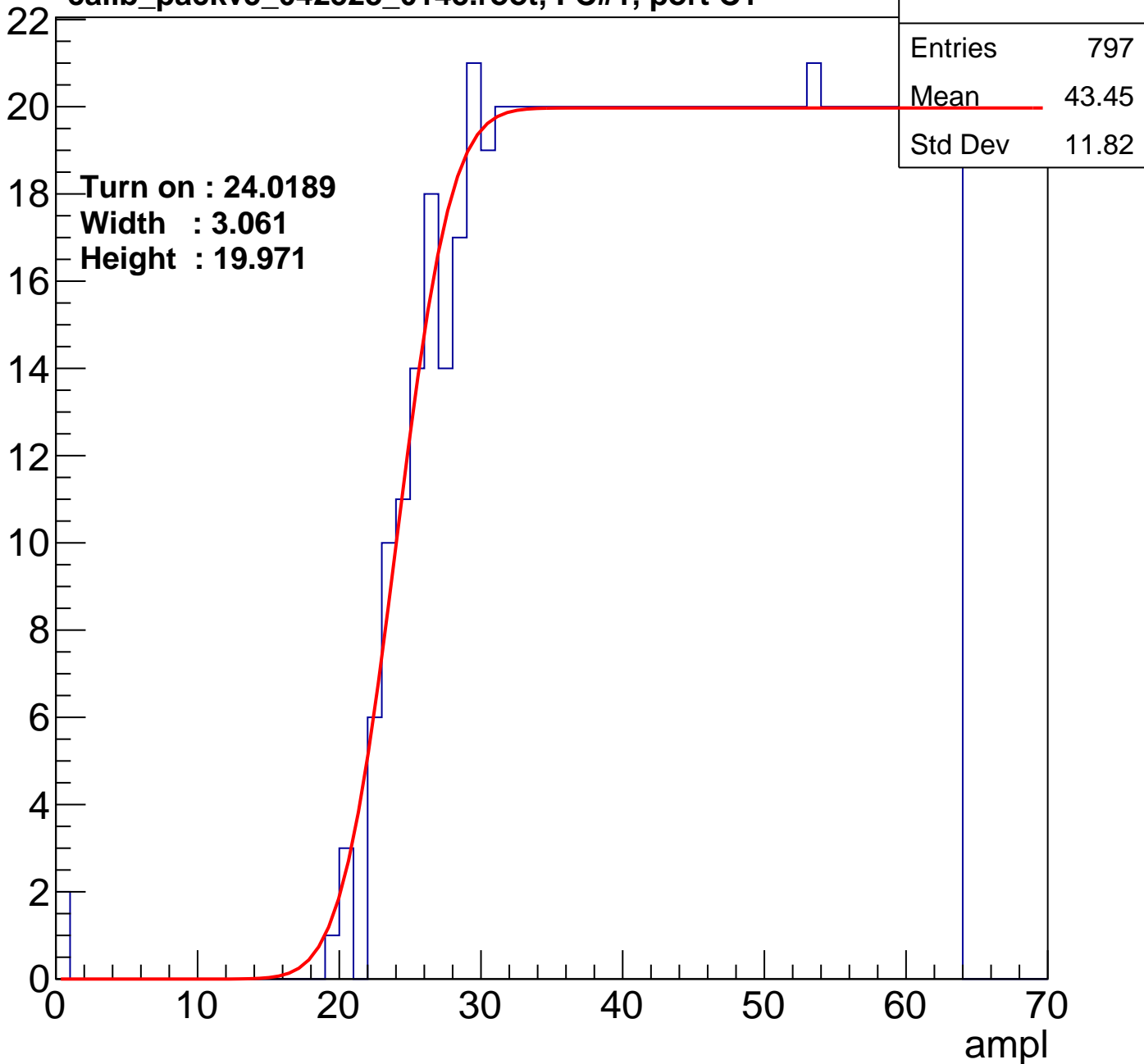
ampl



# B0L101S, U15-ch72

calib\_packv5\_042523\_0143.root, FC#1, port C1

Entry



# B0L101S, U15-ch73

calib\_packv5\_042523\_0143.root, FC#1, port C1

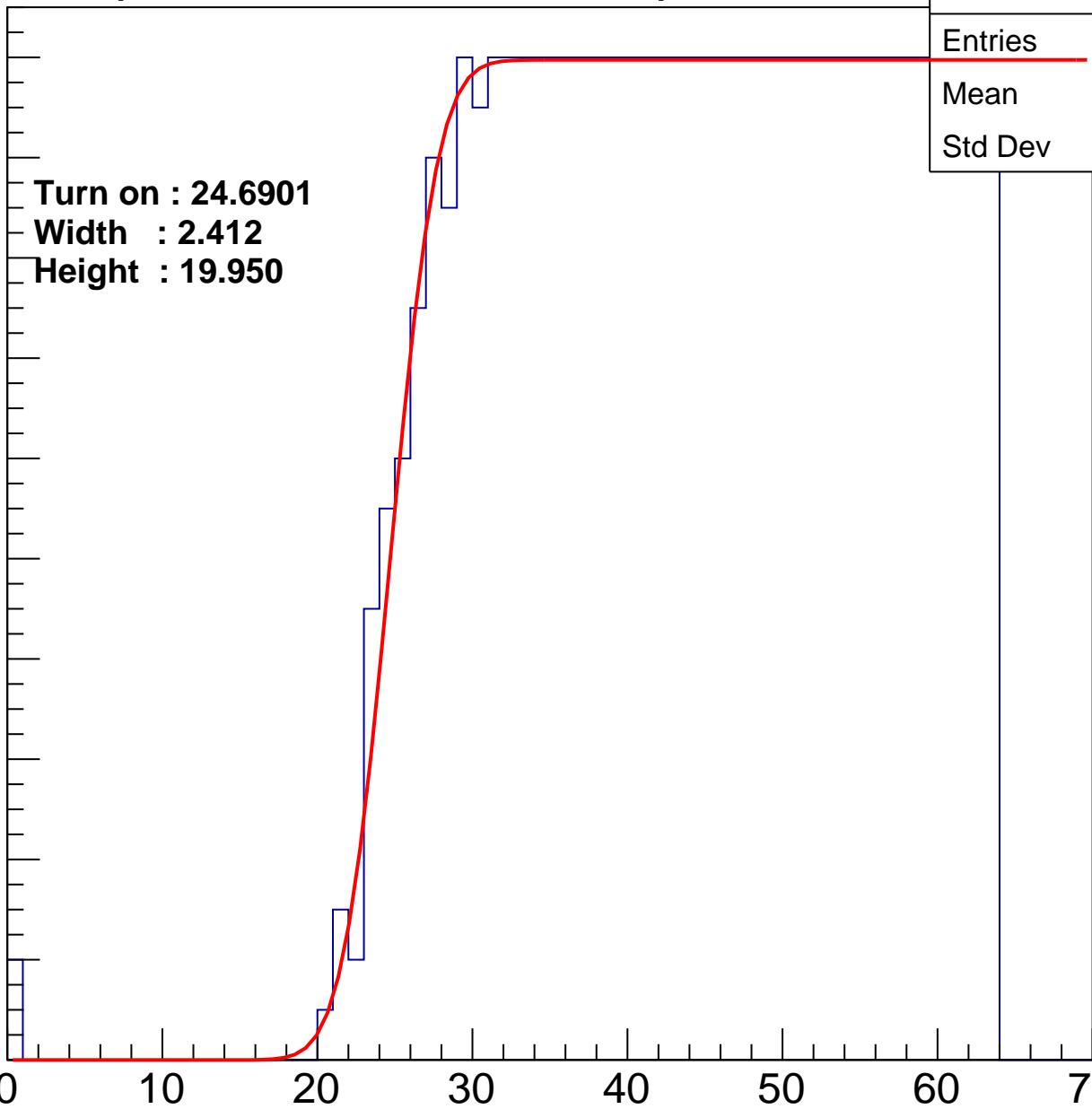
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 24.6901**  
**Width : 2.412**  
**Height : 19.950**

Entries	789
Mean	43.62
Std Dev	11.7

ampl



# B0L101S, U15-ch74

calib\_packv5\_042523\_0143.root, FC#1, port C1

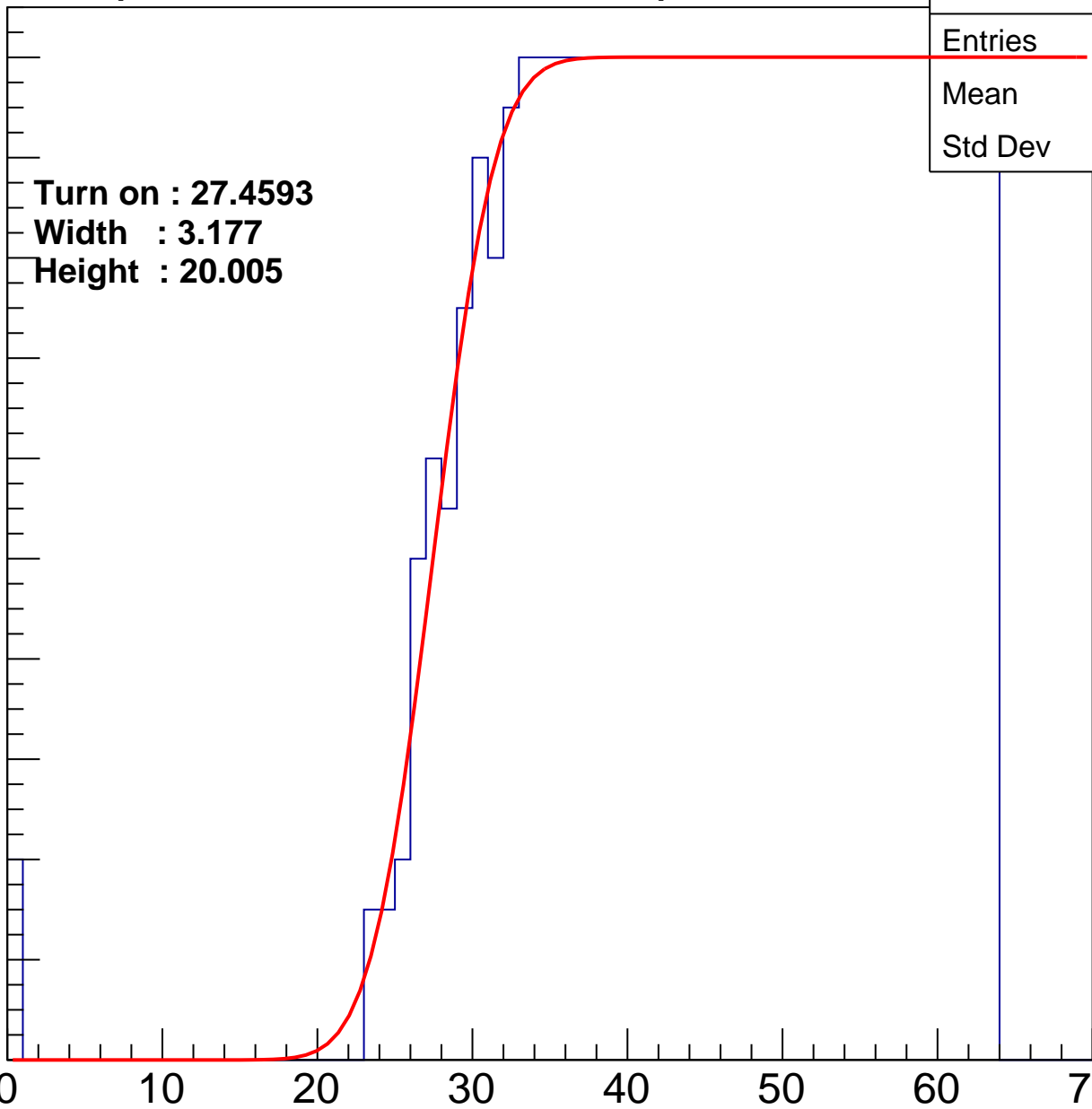
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 27.4593**  
**Width : 3.177**  
**Height : 20.005**

Entries	735
Mean	44.86
Std Dev	11.22

ampl



# B0L101S, U15-ch75

calib\_packv5\_042523\_0143.root, FC#1, port C1

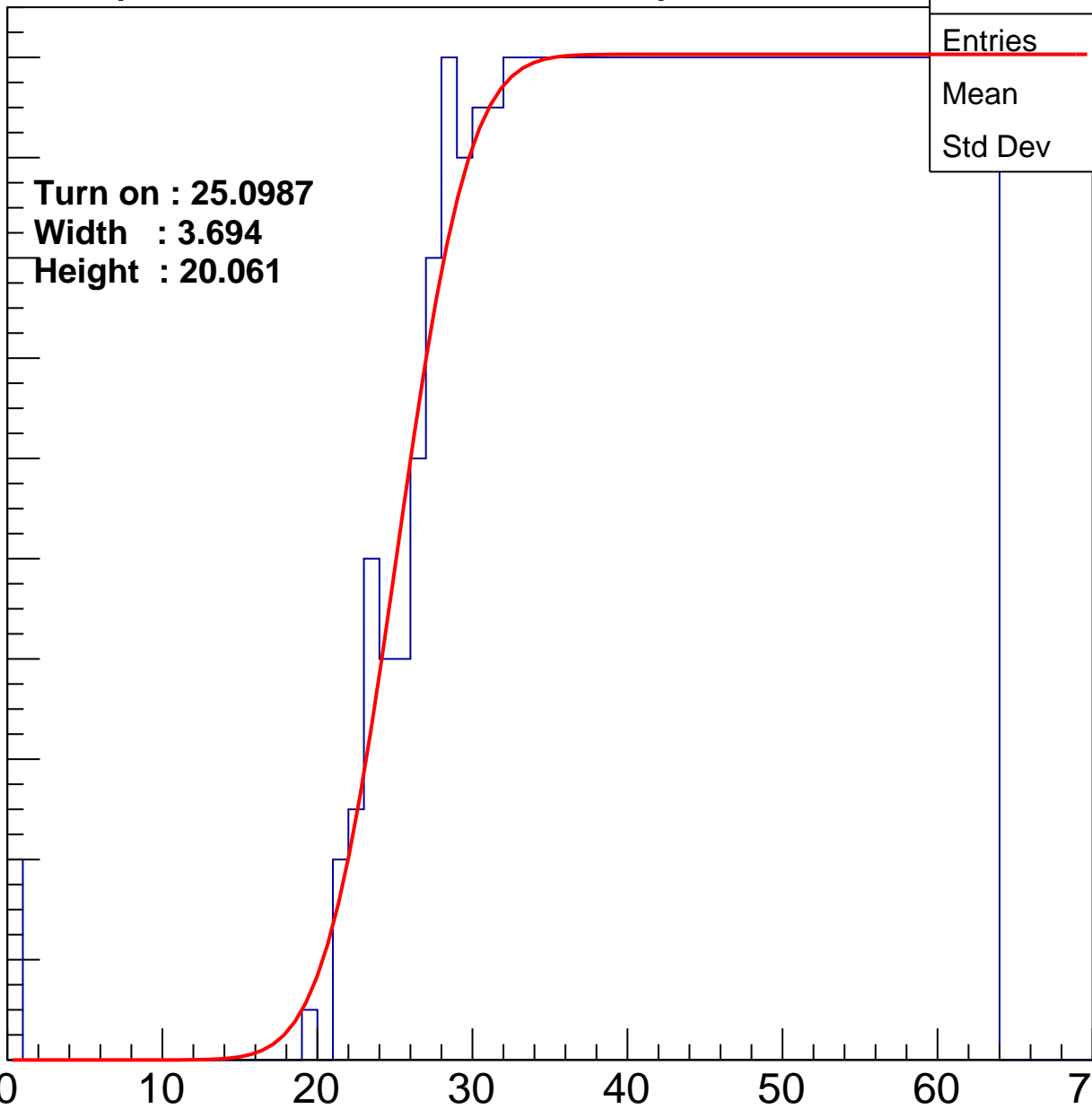
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 25.0987**  
**Width : 3.694**  
**Height : 20.061**

Entries	784
Mean	43.65
Std Dev	11.86

ampl



# B0L101S, U15-ch76

calib\_packv5\_042523\_0143.root, FC#1, port C1

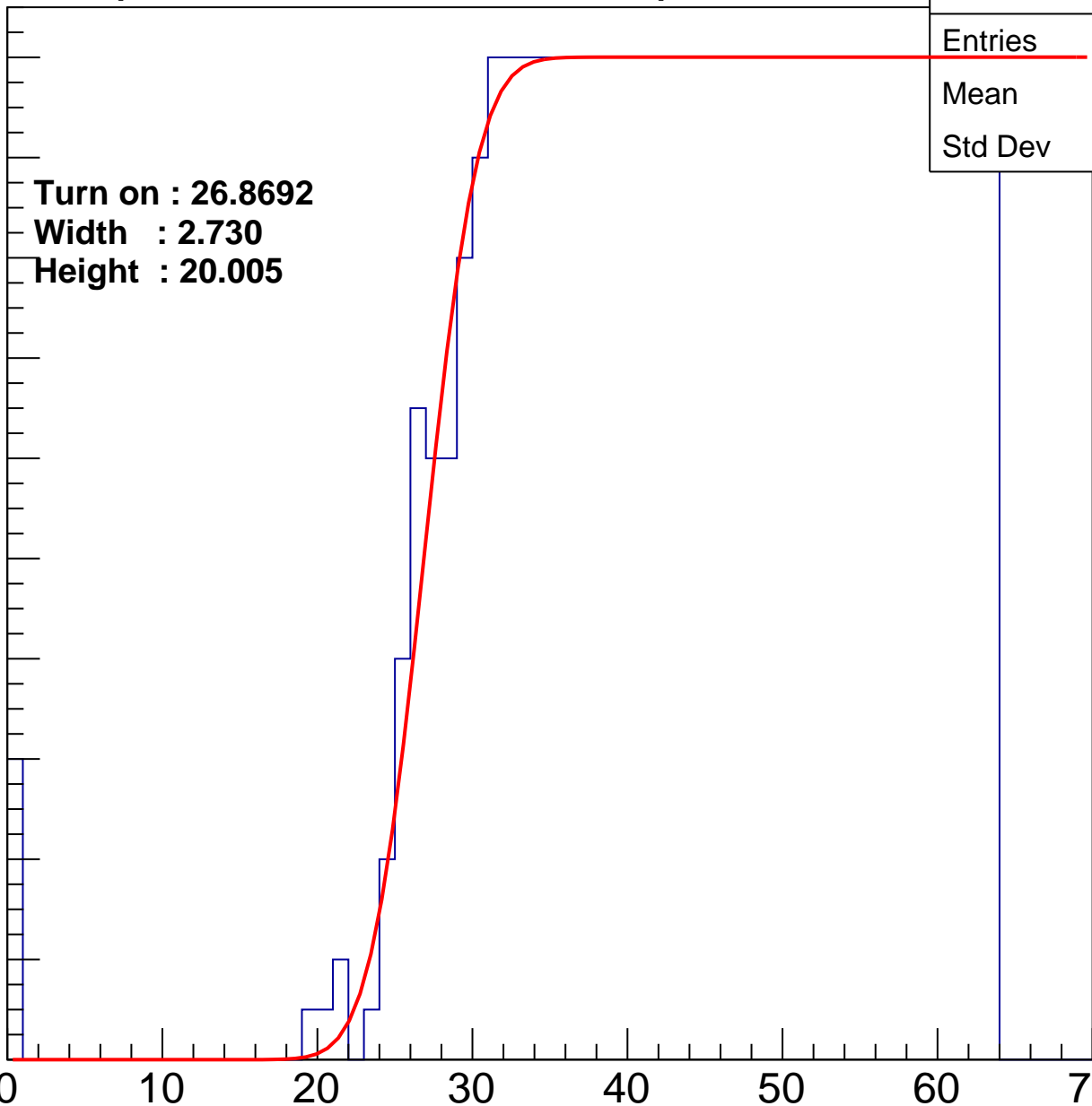
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 26.8692**  
**Width : 2.730**  
**Height : 20.005**

Entries	754
Mean	44.33
Std Dev	11.65

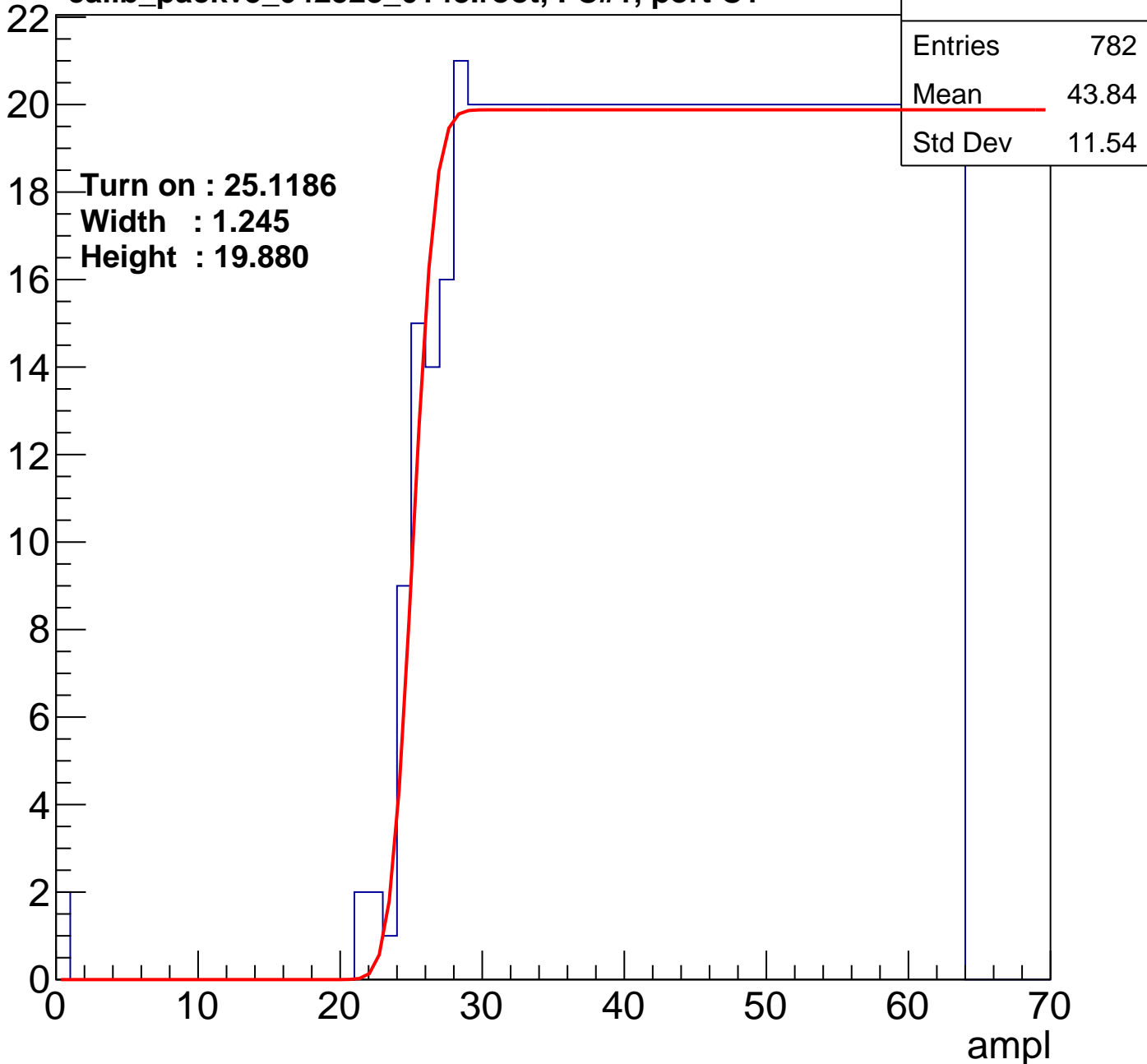
ampl



# B0L101S, U15-ch77

calib\_packv5\_042523\_0143.root, FC#1, port C1

Entry



# B0L101S, U15-ch78

calib\_packv5\_042523\_0143.root, FC#1, port C1

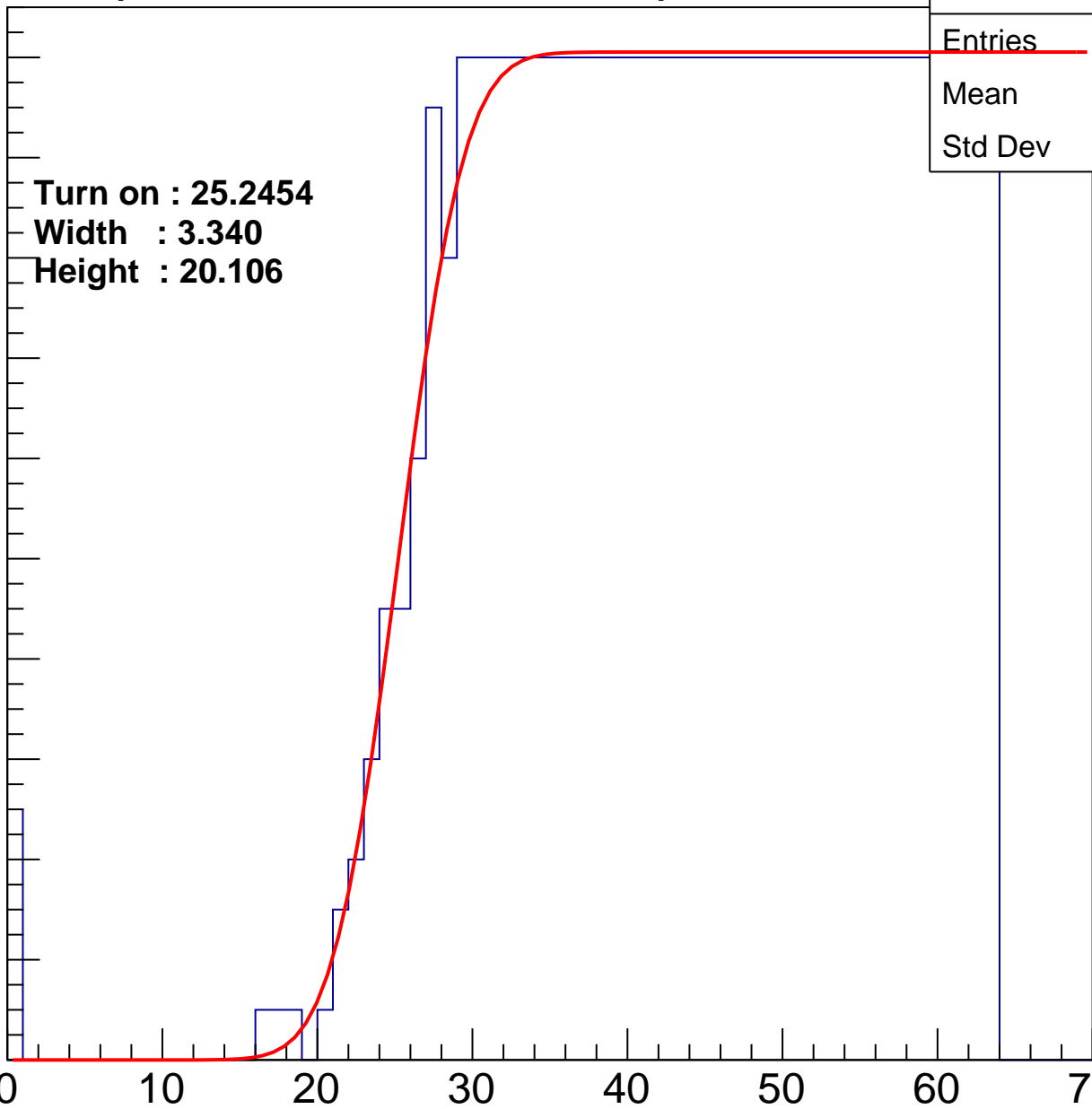
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 25.2454**  
**Width : 3.340**  
**Height : 20.106**

Entries	787
Mean	43.55
Std Dev	11.98

ampl





# B0L101S, U15-ch79

calib\_packv5\_042523\_0143.root, FC#1, port C1

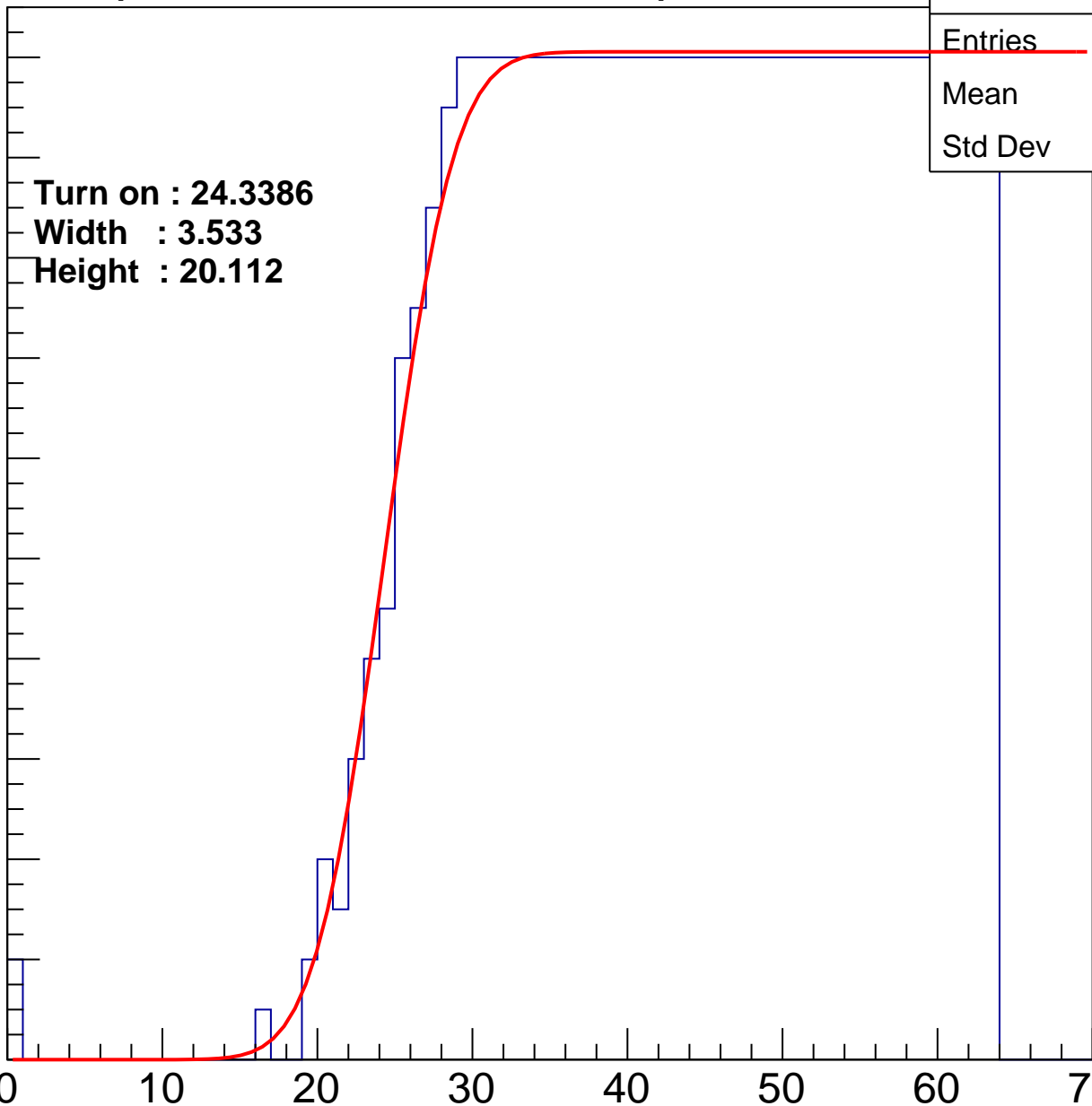
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 24.3386**  
**Width : 3.533**  
**Height : 20.112**

Entries	800
Mean	43.33
Std Dev	11.9

ampl



# B0L101S, U15-ch80

calib\_packv5\_042523\_0143.root, FC#1, port C1

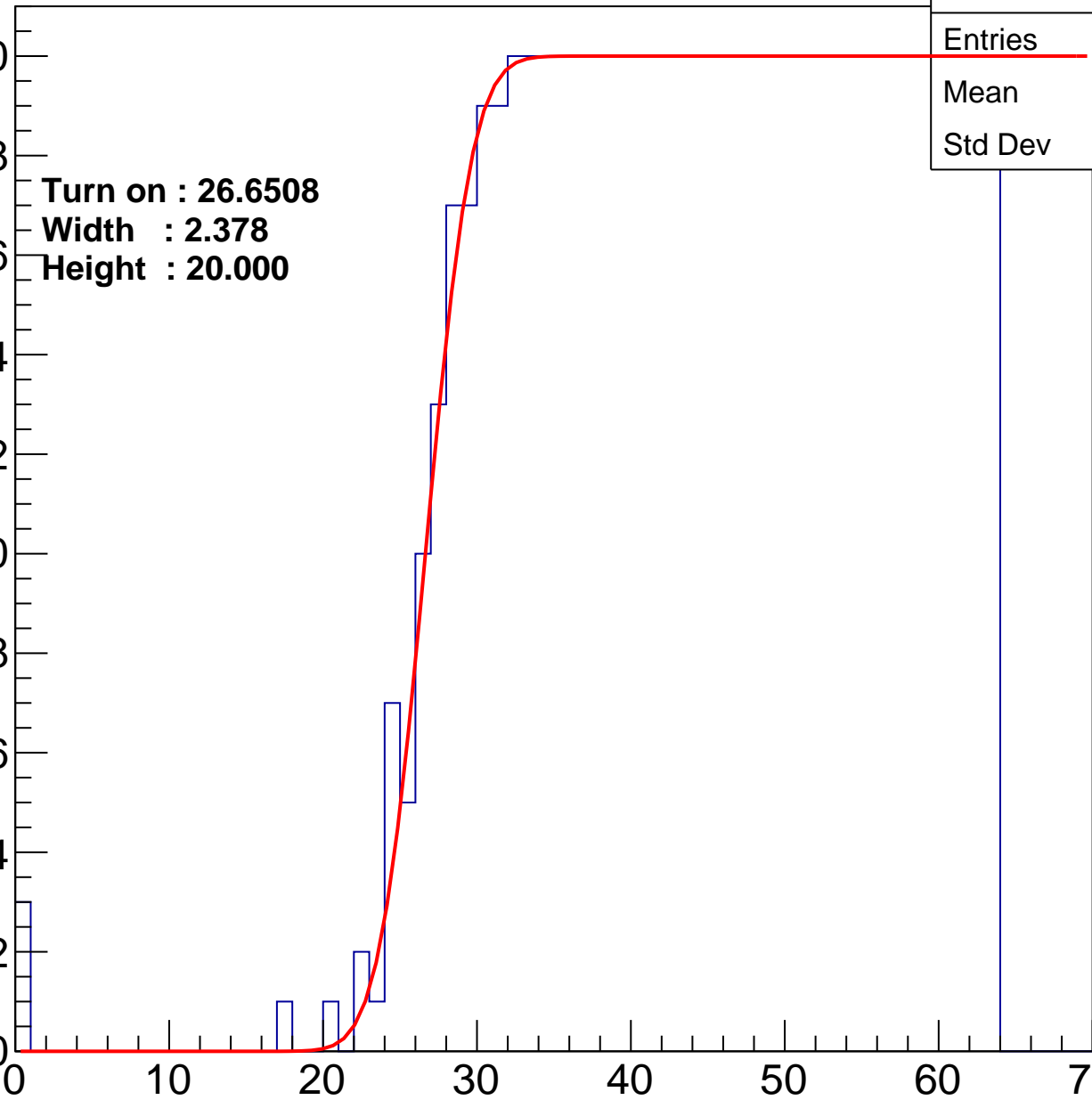
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 26.6508**  
**Width : 2.378**  
**Height : 20.000**

Entries	755
Mean	44.42
Std Dev	11.36

ampl



# B0L101S, U15-ch81

calib\_packv5\_042523\_0143.root, FC#1, port C1

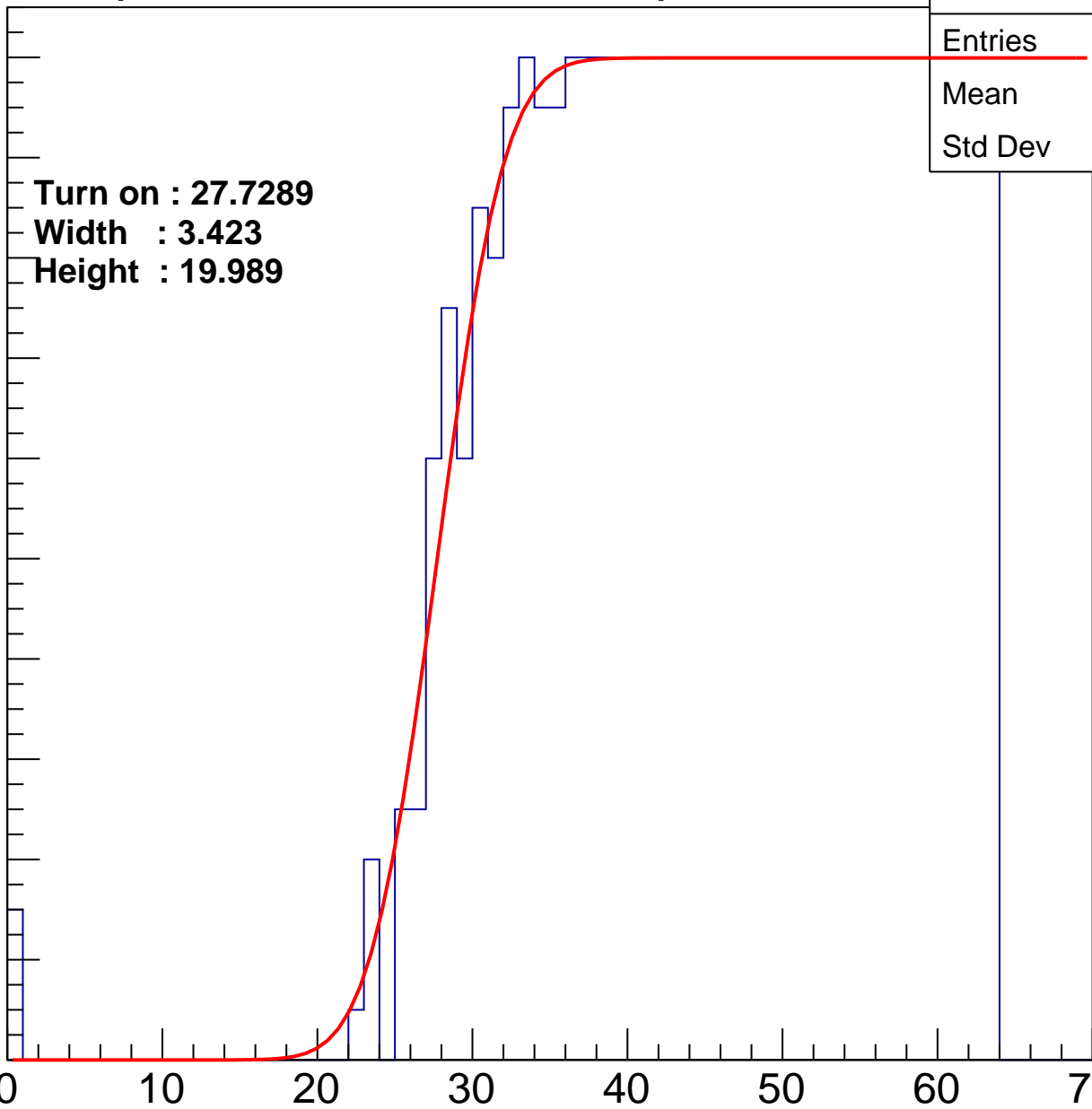
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 27.7289**  
**Width : 3.423**  
**Height : 19.989**

Entries	727
Mean	45.07
Std Dev	11.05

ampl



# B0L101S, U15-ch82

calib\_packv5\_042523\_0143.root, FC#1, port C1

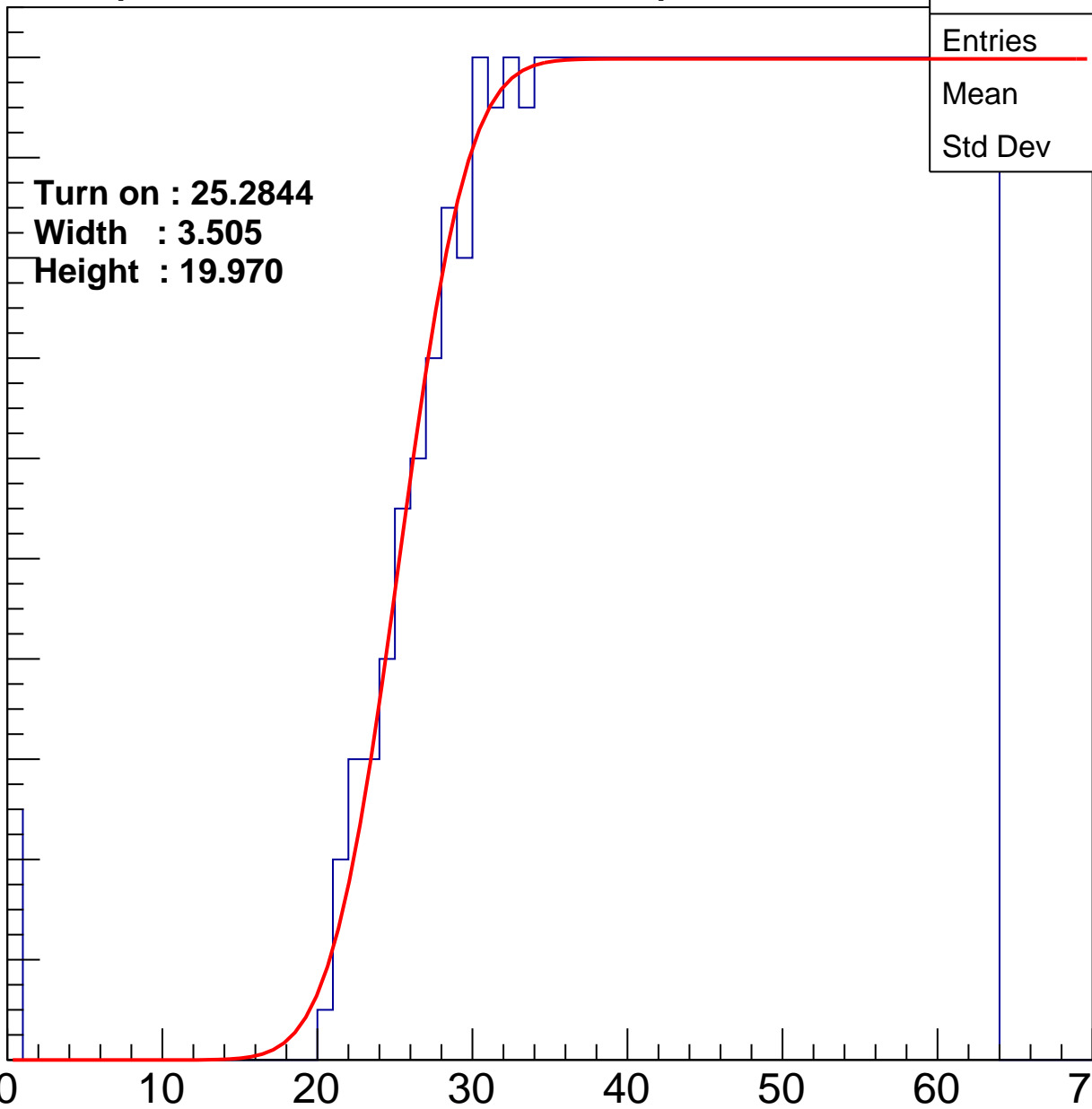
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 25.2844**  
**Width : 3.505**  
**Height : 19.970**

Entries	778
Mean	43.74
Std Dev	11.91

ampl



# B0L101S, U15-ch83

calib\_packv5\_042523\_0143.root, FC#1, port C1

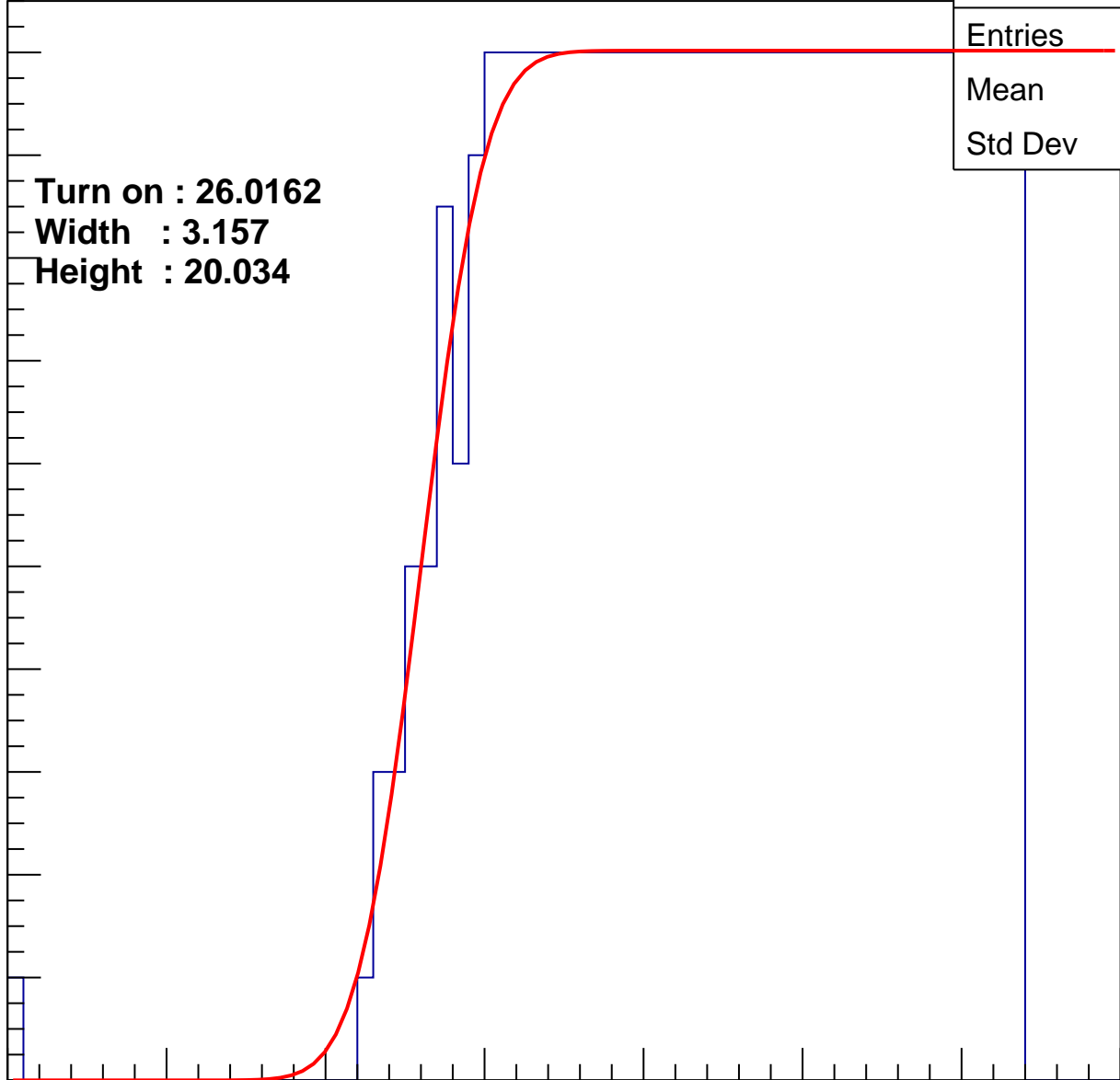
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 26.0162  
Width : 3.157  
Height : 20.034

Entries	763
Mean	44.26
Std Dev	11.36

ampl



# B0L101S, U15-ch84

calib\_packv5\_042523\_0143.root, FC#1, port C1

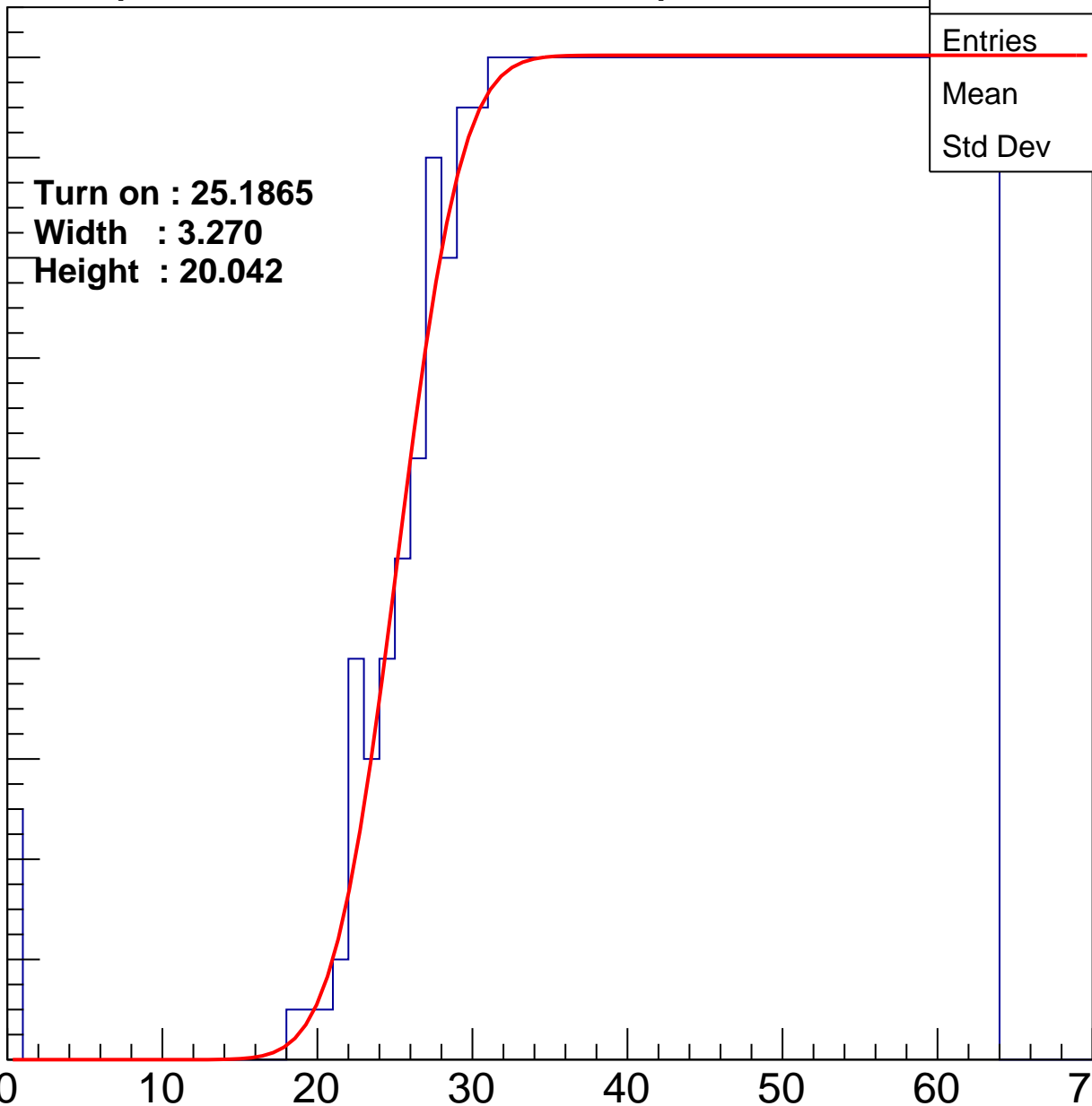
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 25.1865  
Width : 3.270  
Height : 20.042

Entries	786
Mean	43.56
Std Dev	11.98

ampl



# B0L101S, U15-ch85

calib\_packv5\_042523\_0143.root, FC#1, port C1

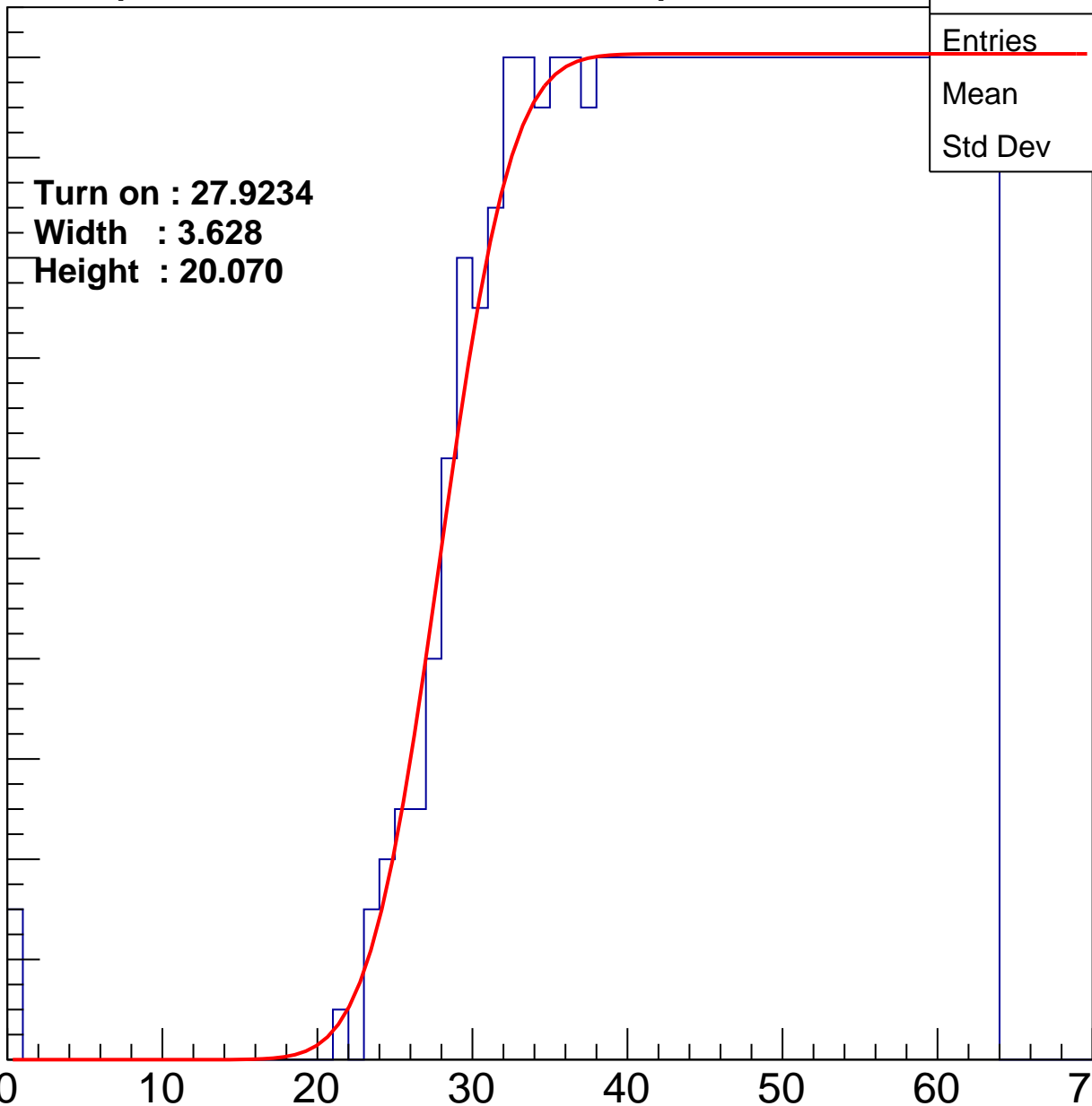
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 27.9234  
Width : 3.628  
Height : 20.070

Entries	727
Mean	45.07
Std Dev	11.06

ampl



# B0L101S, U15-ch86

calib\_packv5\_042523\_0143.root, FC#1, port C1

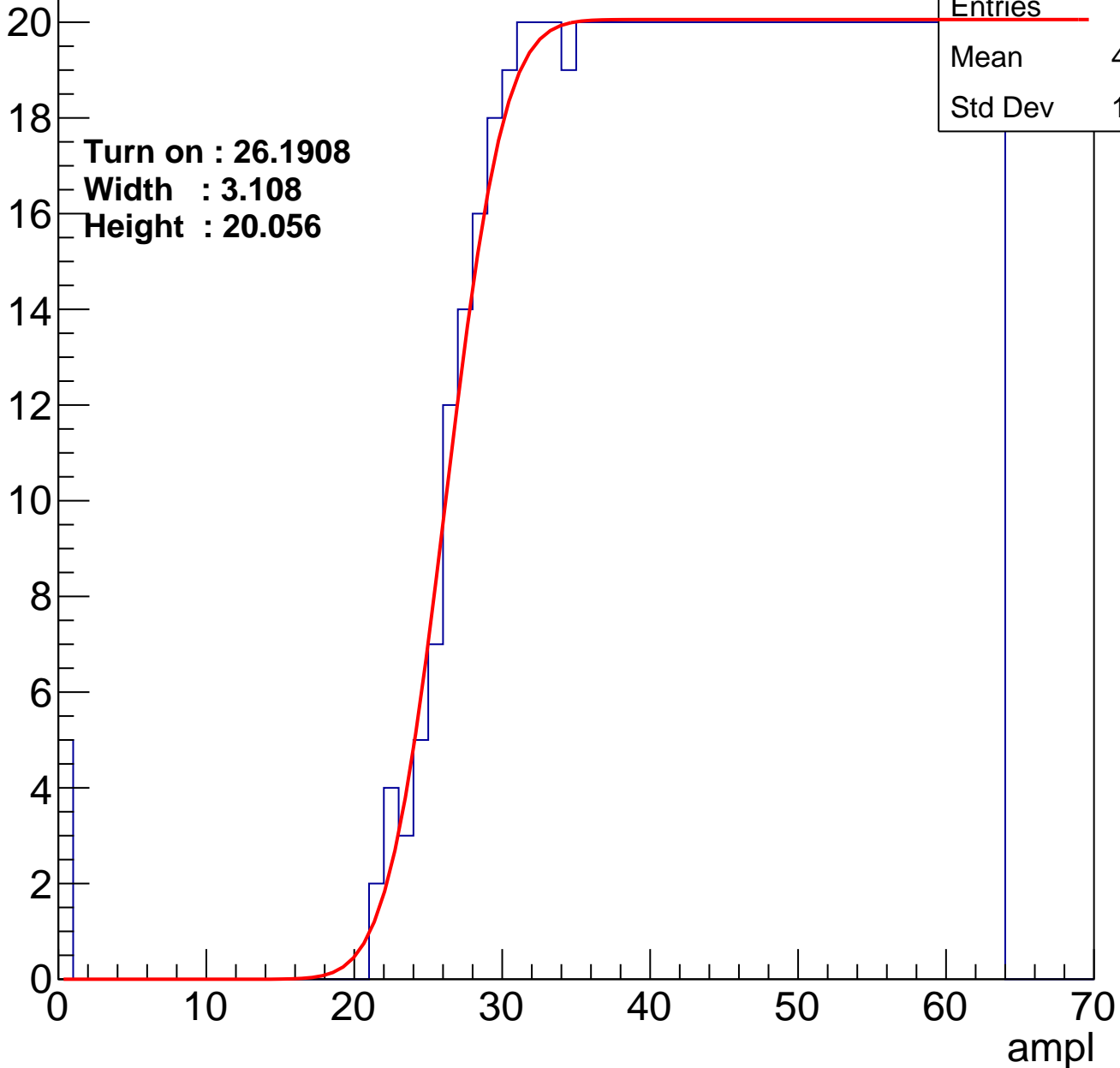
Entries	764
Mean	44.12
Std Dev	11.67

Turn on : 26.1908

Width : 3.108

Height : 20.056

Entry





# B0L101S, U15-ch87

calib\_packv5\_042523\_0143.root, FC#1, port C1

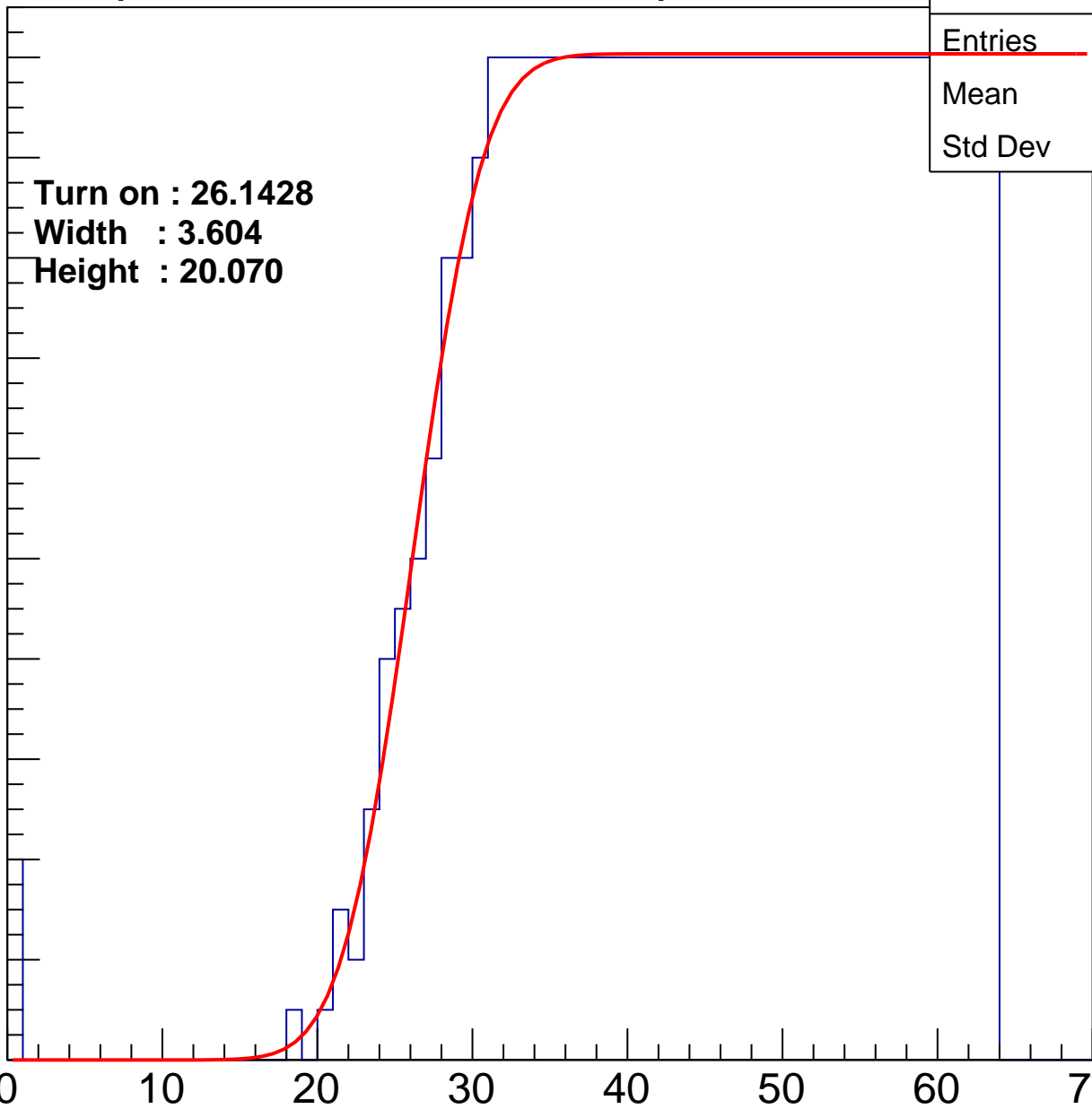
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 26.1428**  
**Width : 3.604**  
**Height : 20.070**

Entries	765
Mean	44.1
Std Dev	11.65

ampl



# B0L101S, U15-ch88

calib\_packv5\_042523\_0143.root, FC#1, port C1

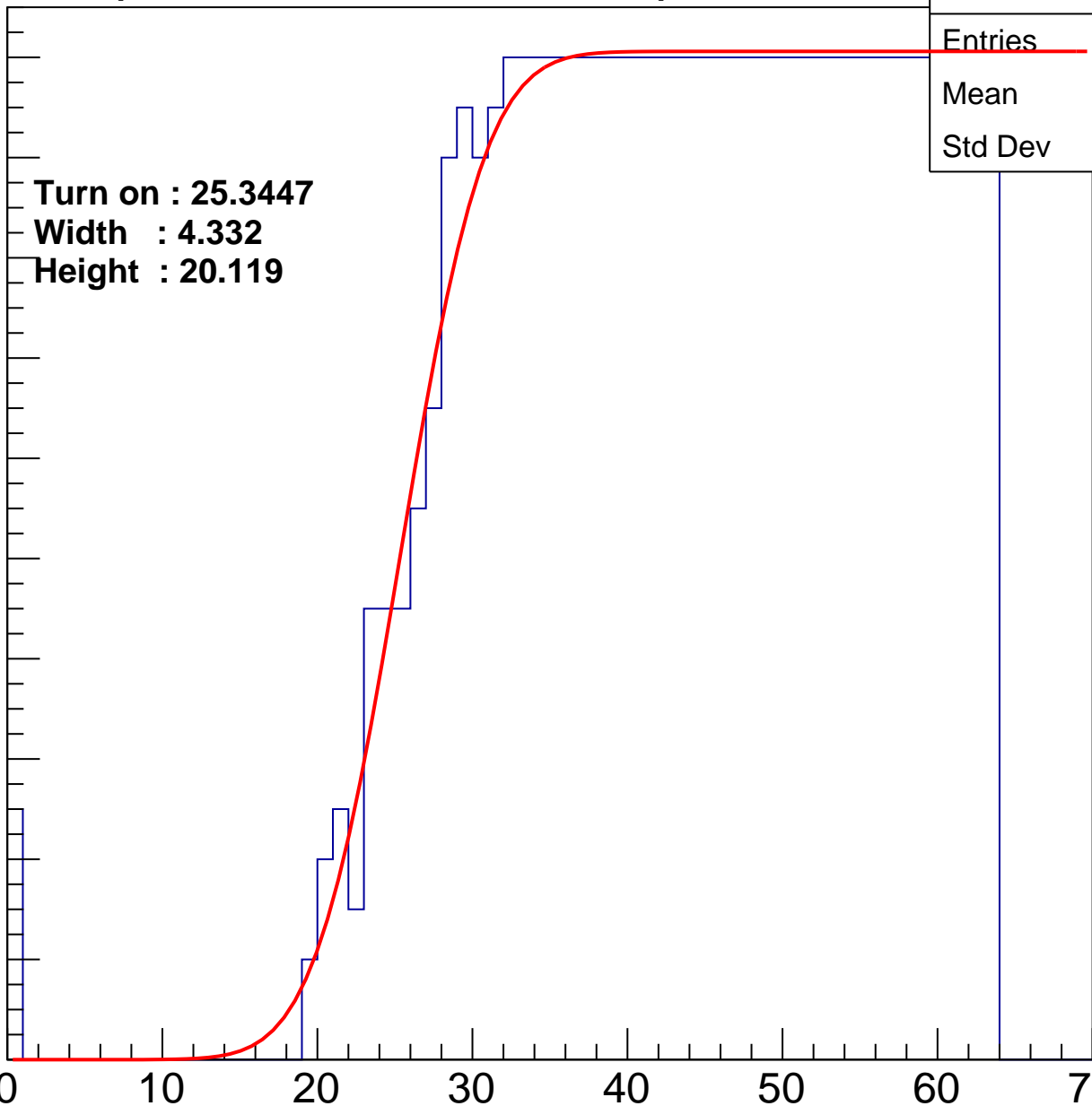
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 25.3447**  
**Width : 4.332**  
**Height : 20.119**

Entries	784
Mean	43.57
Std Dev	12.02

ampl



# B0L101S, U15-ch89

calib\_packv5\_042523\_0143.root, FC#1, port C1

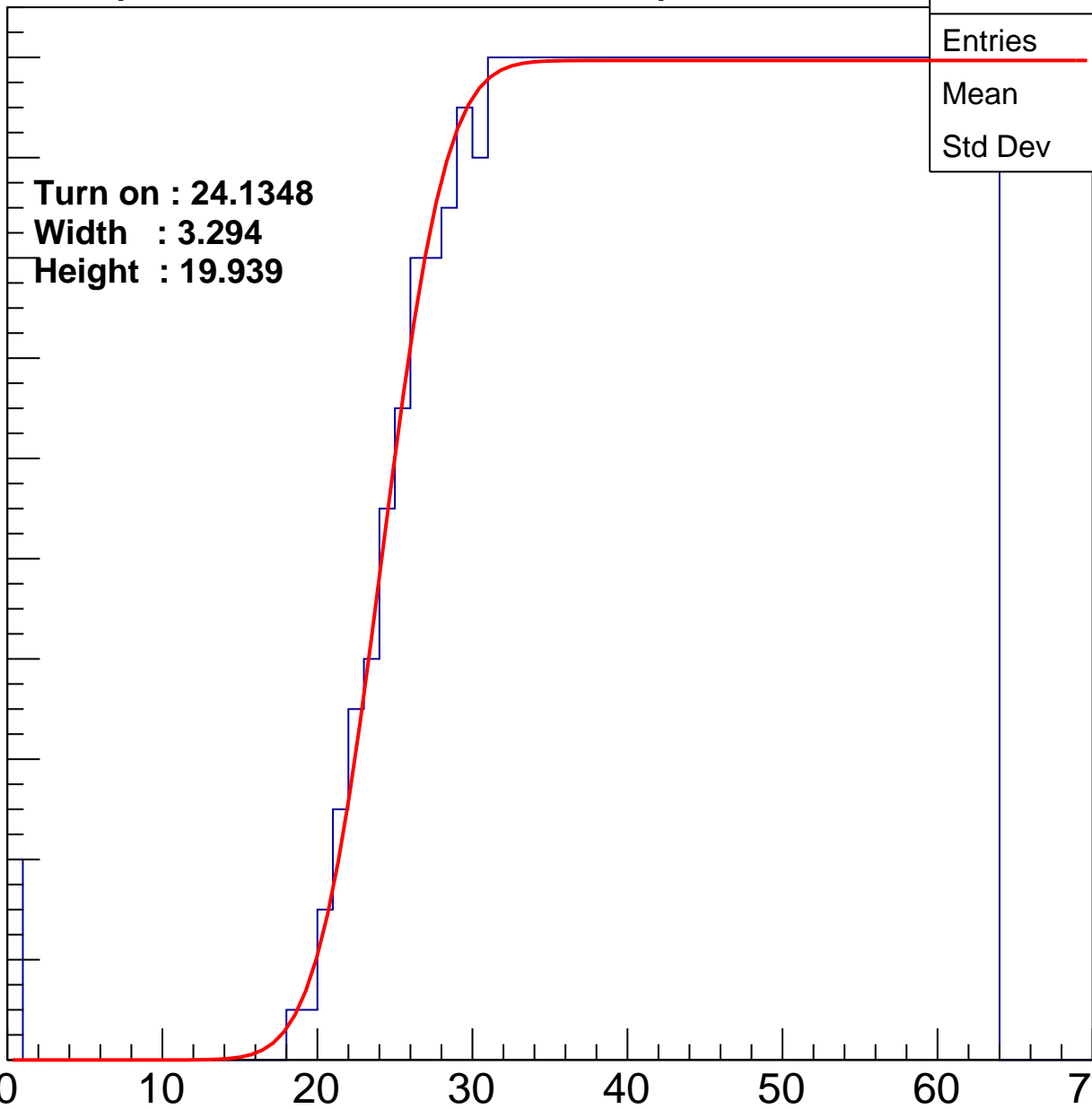
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 24.1348**  
**Width : 3.294**  
**Height : 19.939**

Entries	799
Mean	43.26
Std Dev	12.09

ampl

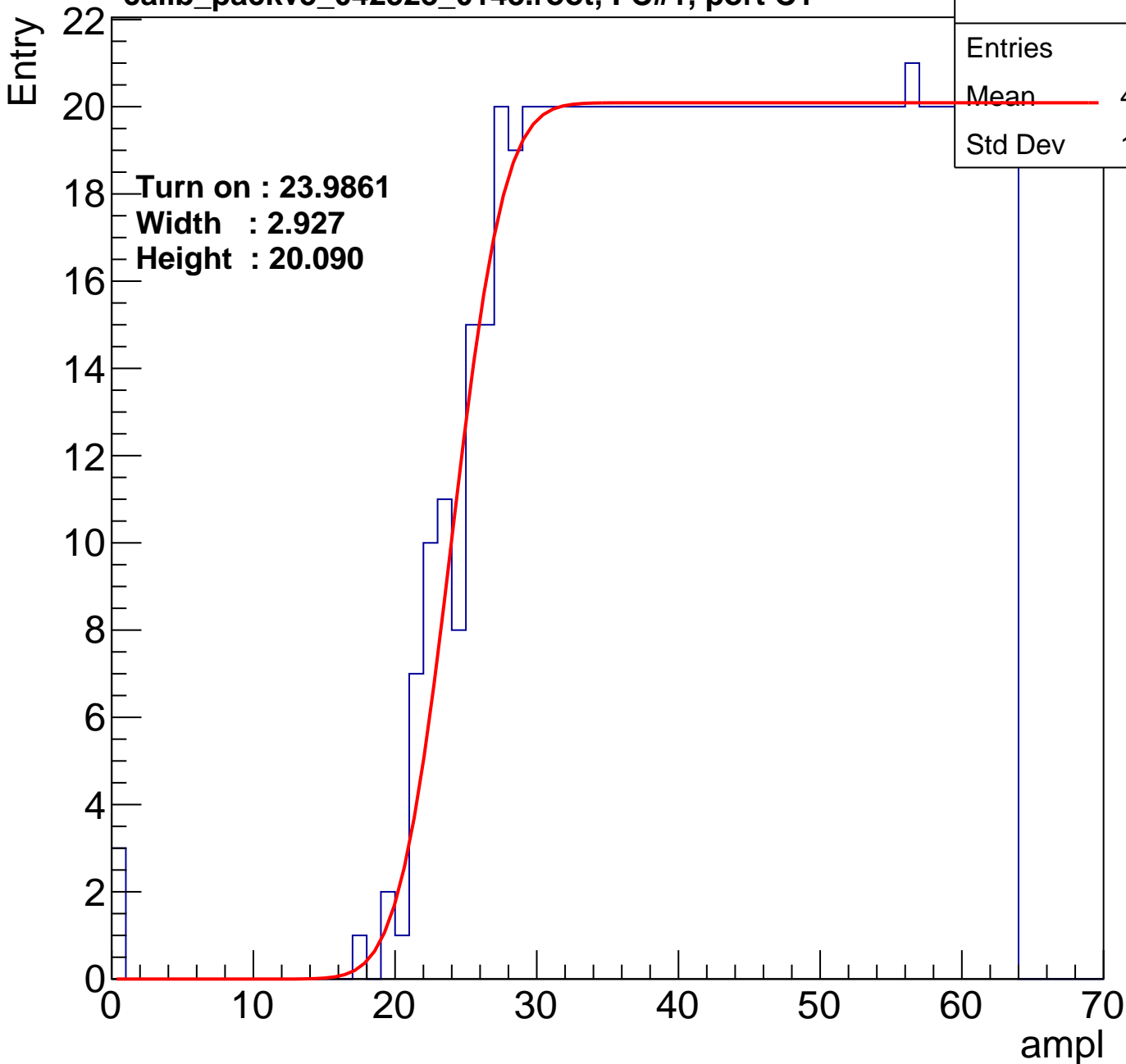


# B0L101S, U15-ch90

calib\_packv5\_042523\_0143.root, FC#1, port C1

Entries	814
Mean	43.05
Std Dev	12.13

Turn on : 23.9861  
Width : 2.927  
Height : 20.090



# B0L101S, U15-ch91

calib\_packv5\_042523\_0143.root, FC#1, port C1

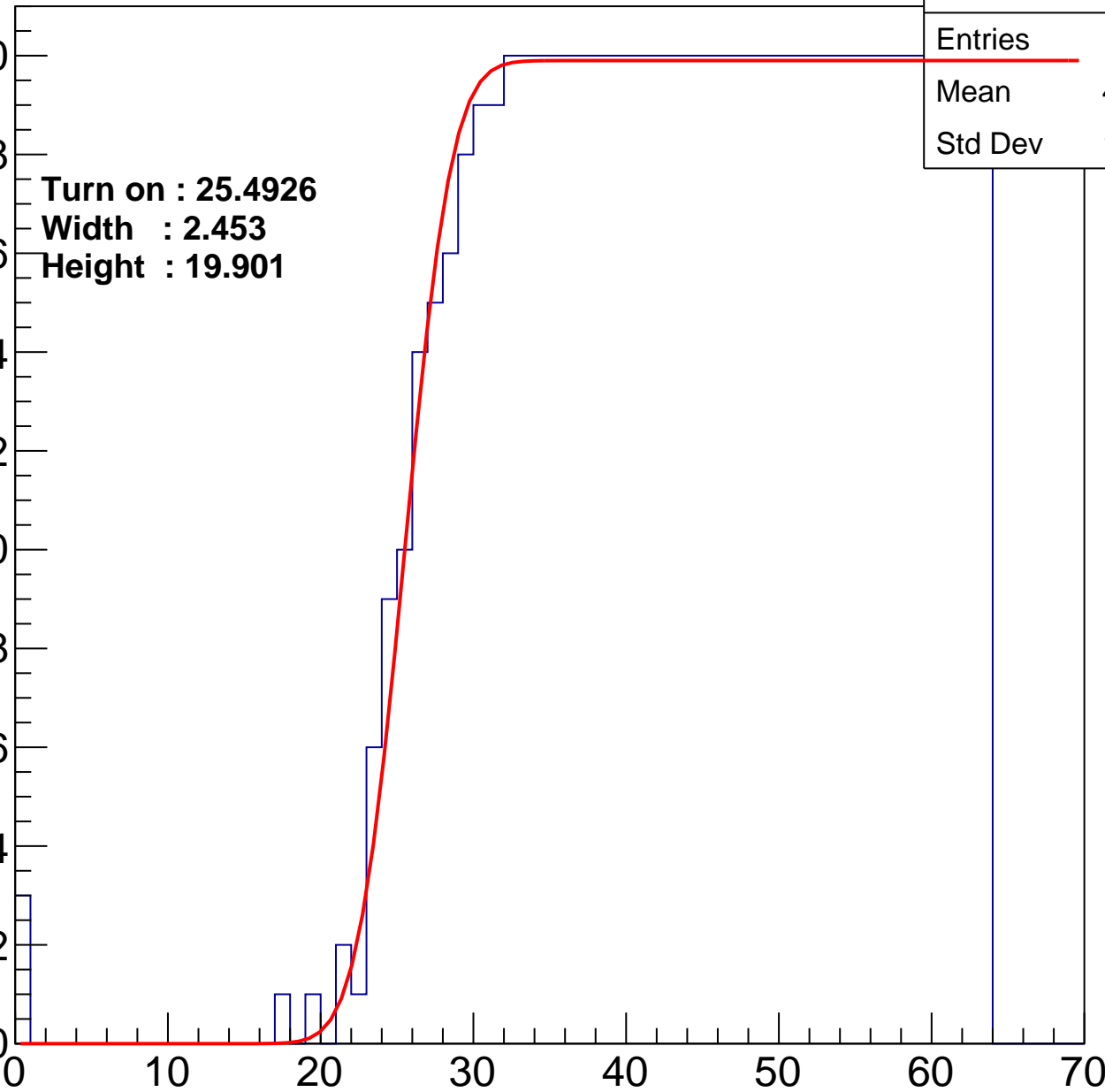
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 25.4926  
Width : 2.453  
Height : 19.901

Entries	774
Mean	43.93
Std Dev	11.64

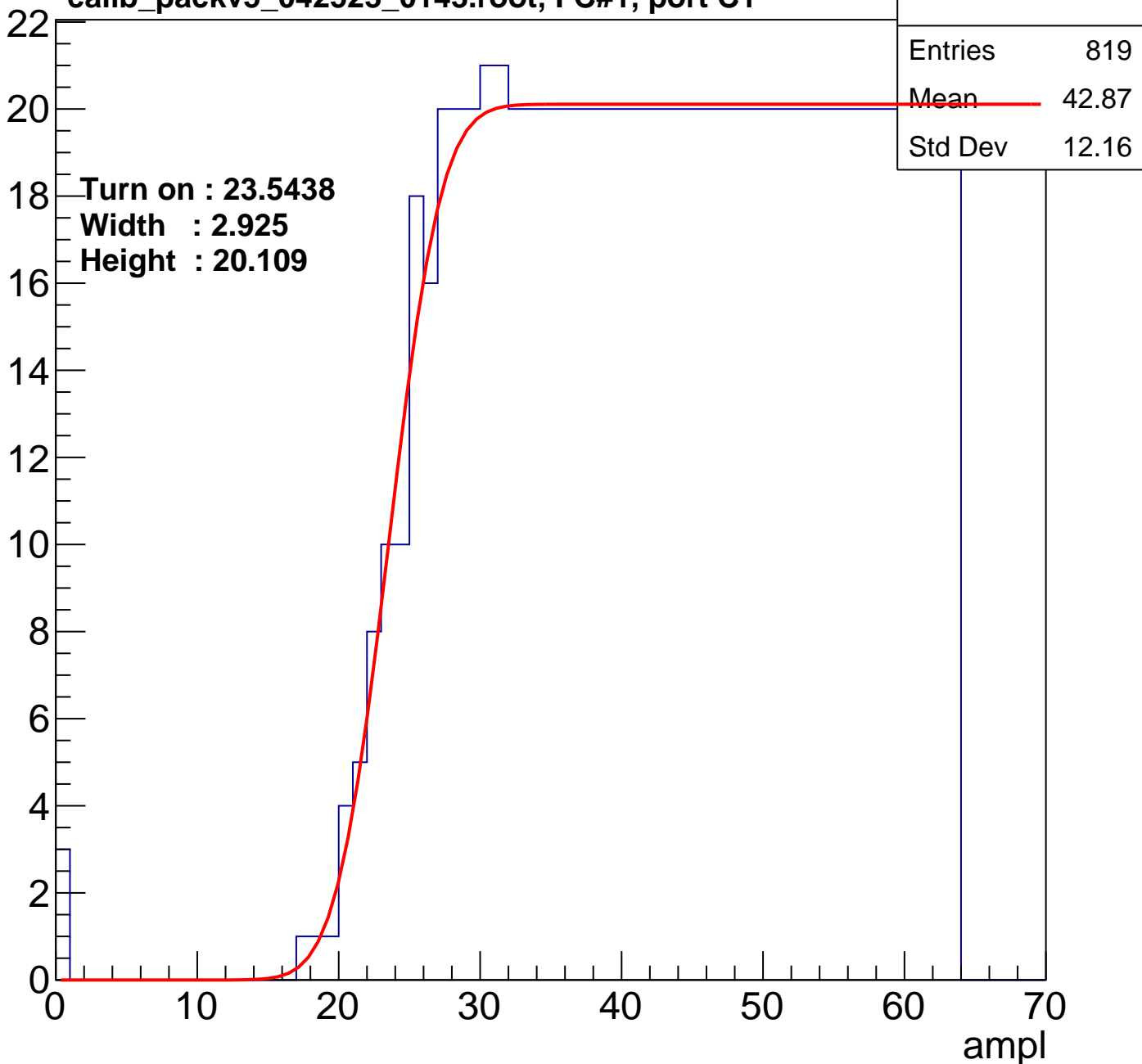
ampl



# B0L101S, U15-ch92

calib\_packv5\_042523\_0143.root, FC#1, port C1

Entry



# B0L101S, U15-ch93

calib\_packv5\_042523\_0143.root, FC#1, port C1

Entry

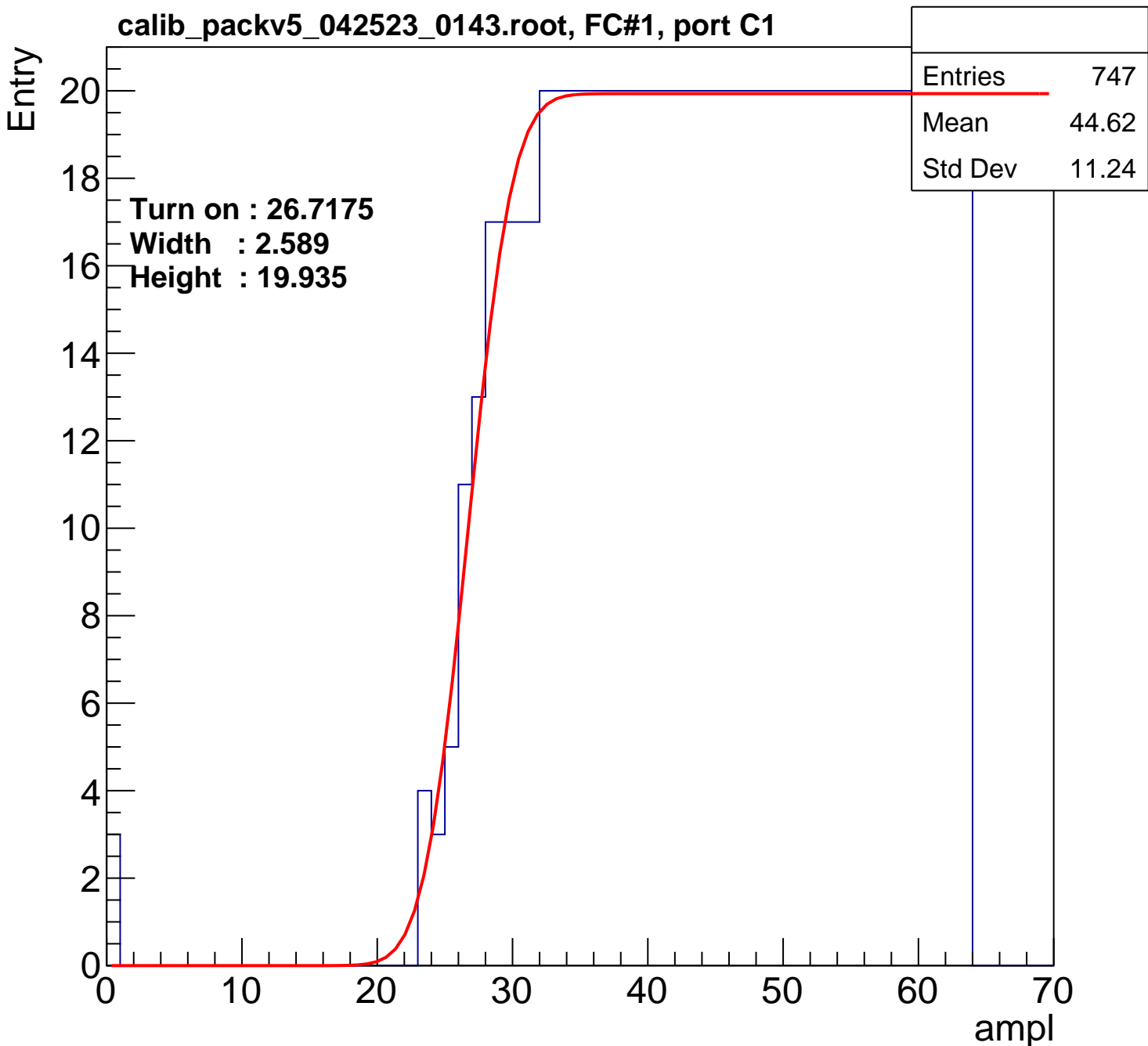
20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 26.7175**  
**Width : 2.589**  
**Height : 19.935**

Entries	747
Mean	44.62
Std Dev	11.24

ampl

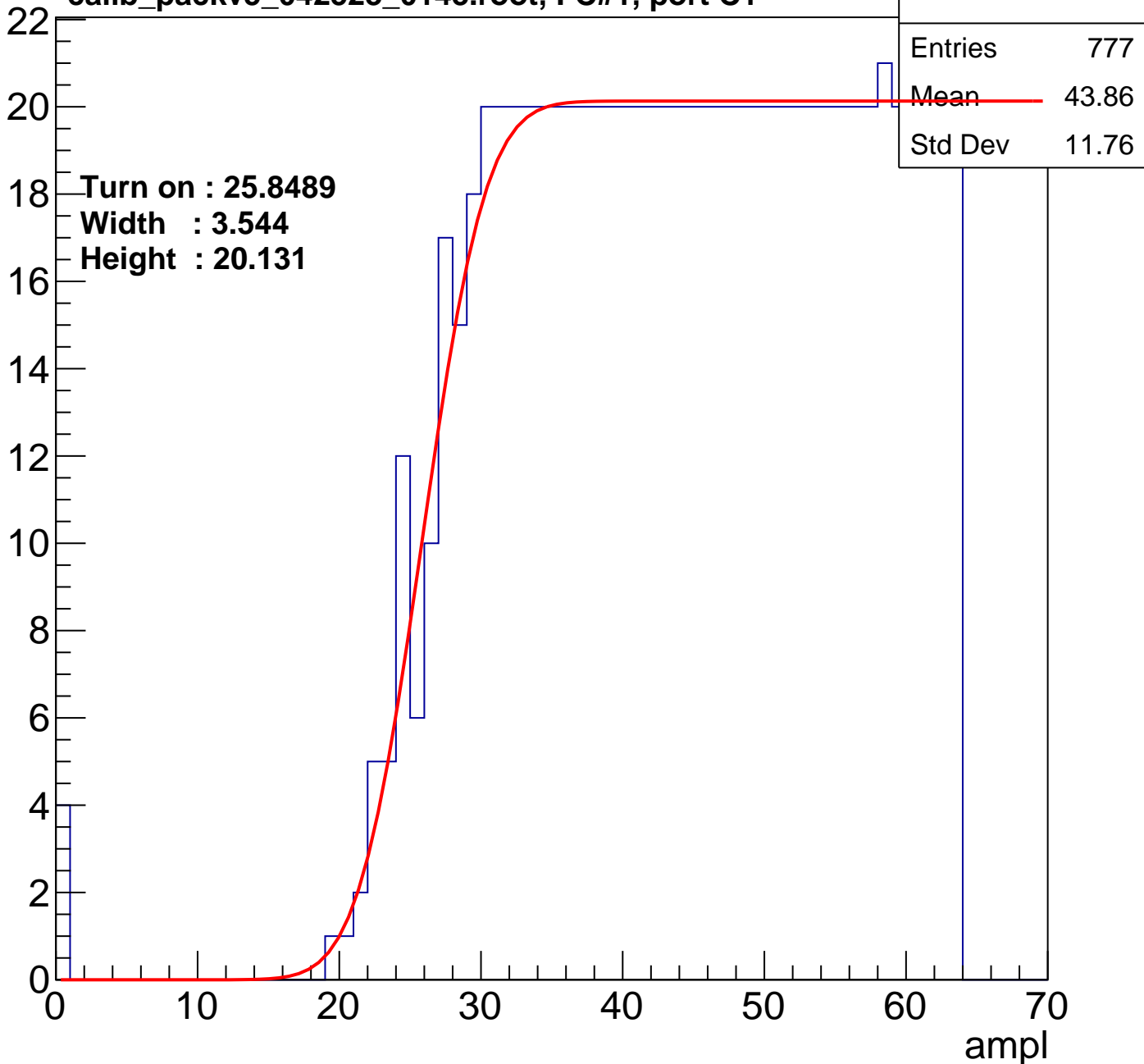
0 10 20 30 40 50 60 70



# B0L101S, U15-ch94

calib\_packv5\_042523\_0143.root, FC#1, port C1

Entry





# B0L101S, U15-ch95

calib\_packv5\_042523\_0143.root, FC#1, port C1

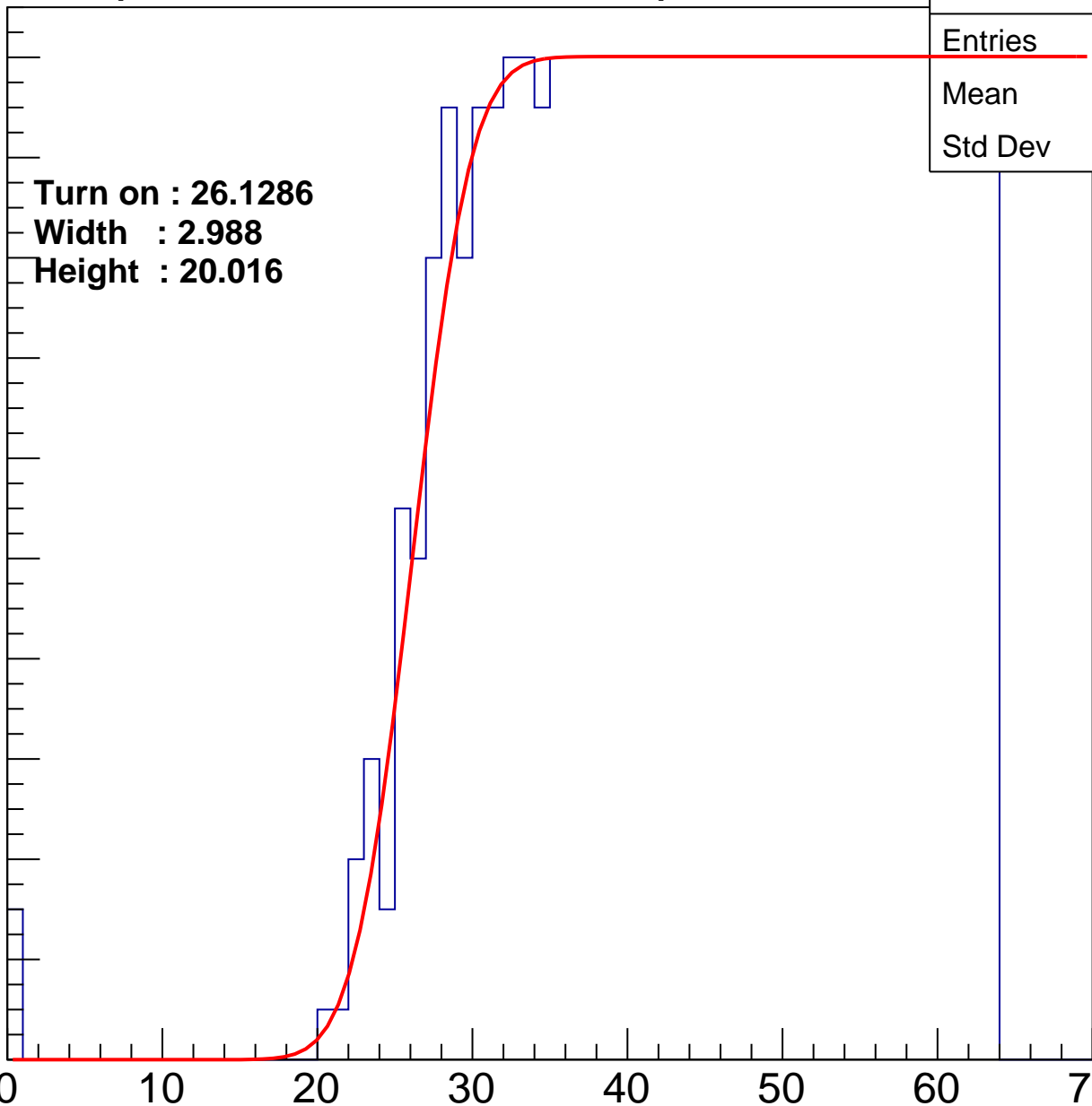
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 26.1286  
Width : 2.988  
Height : 20.016

Entries	767
Mean	44.1
Std Dev	11.54

ampl



# B0L101S, U15-ch96

calib\_packv5\_042523\_0143.root, FC#1, port C1

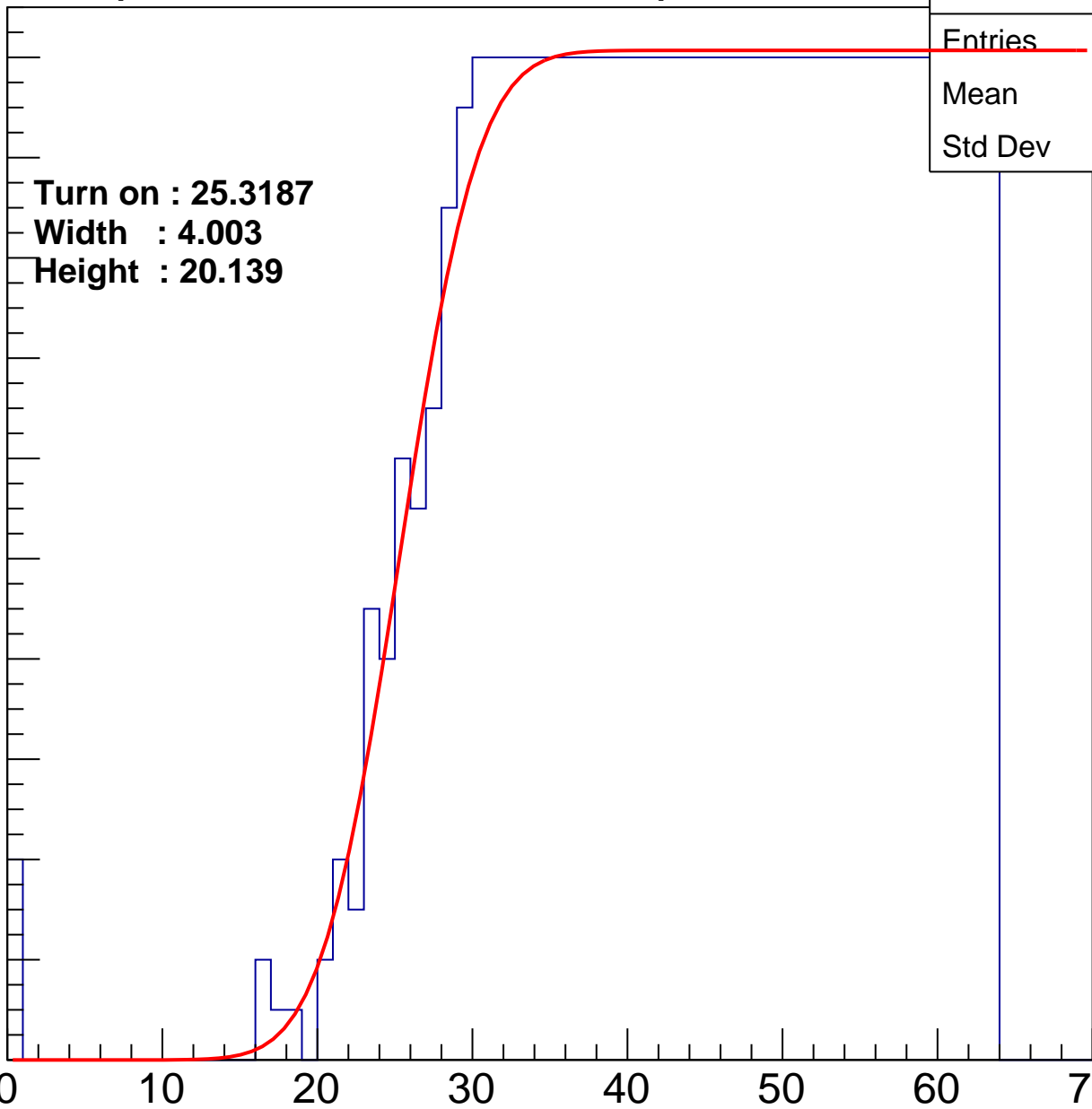
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 25.3187  
Width : 4.003  
Height : 20.139

Entries	786
Mean	43.56
Std Dev	11.96

ampl



# B0L101S, U15-ch97

calib\_packv5\_042523\_0143.root, FC#1, port C1

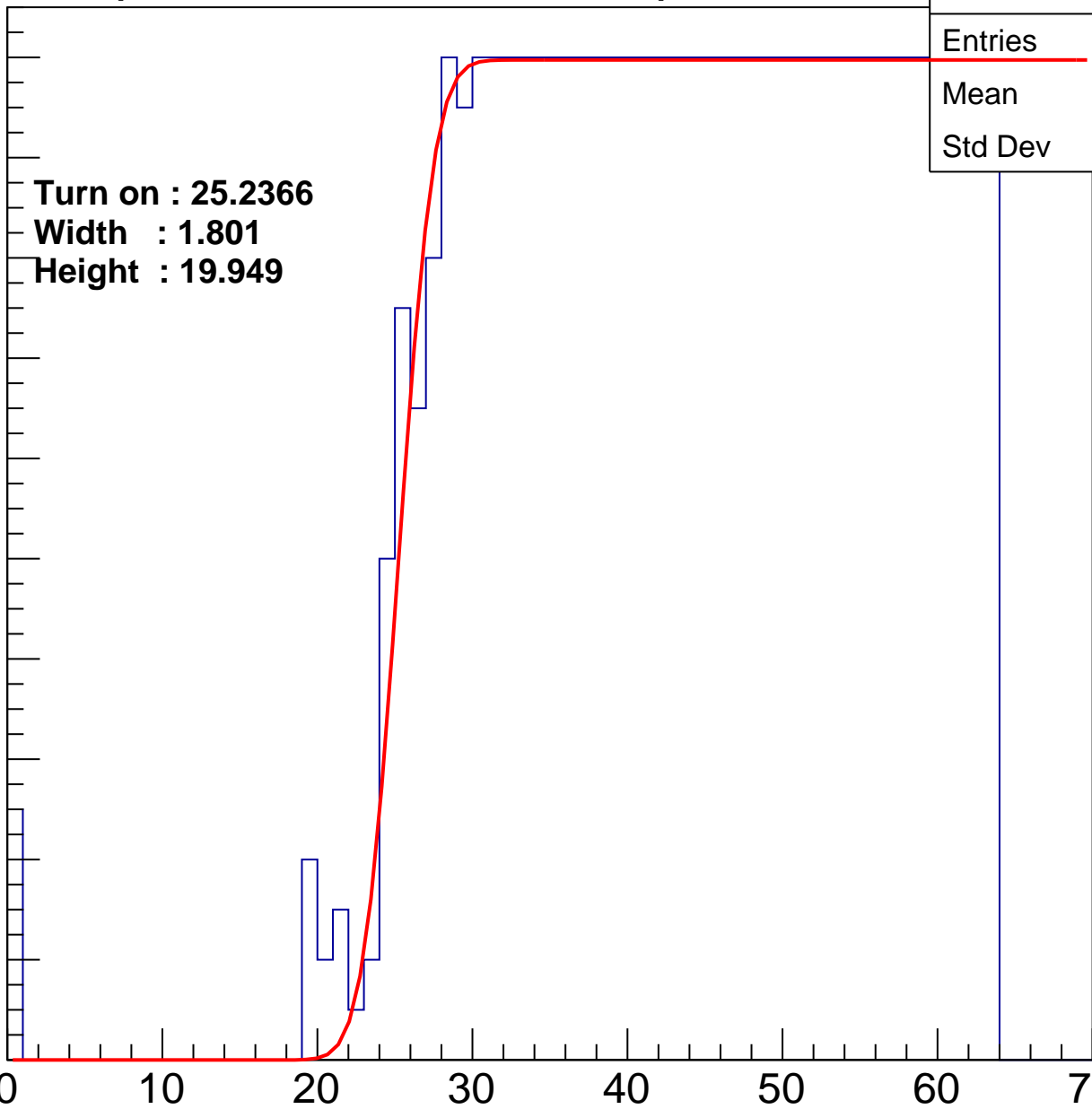
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 25.2366**  
**Width : 1.801**  
**Height : 19.949**

Entries	790
Mean	43.5
Std Dev	11.98

ampl



# B0L101S, U15-ch98

calib\_packv5\_042523\_0143.root, FC#1, port C1

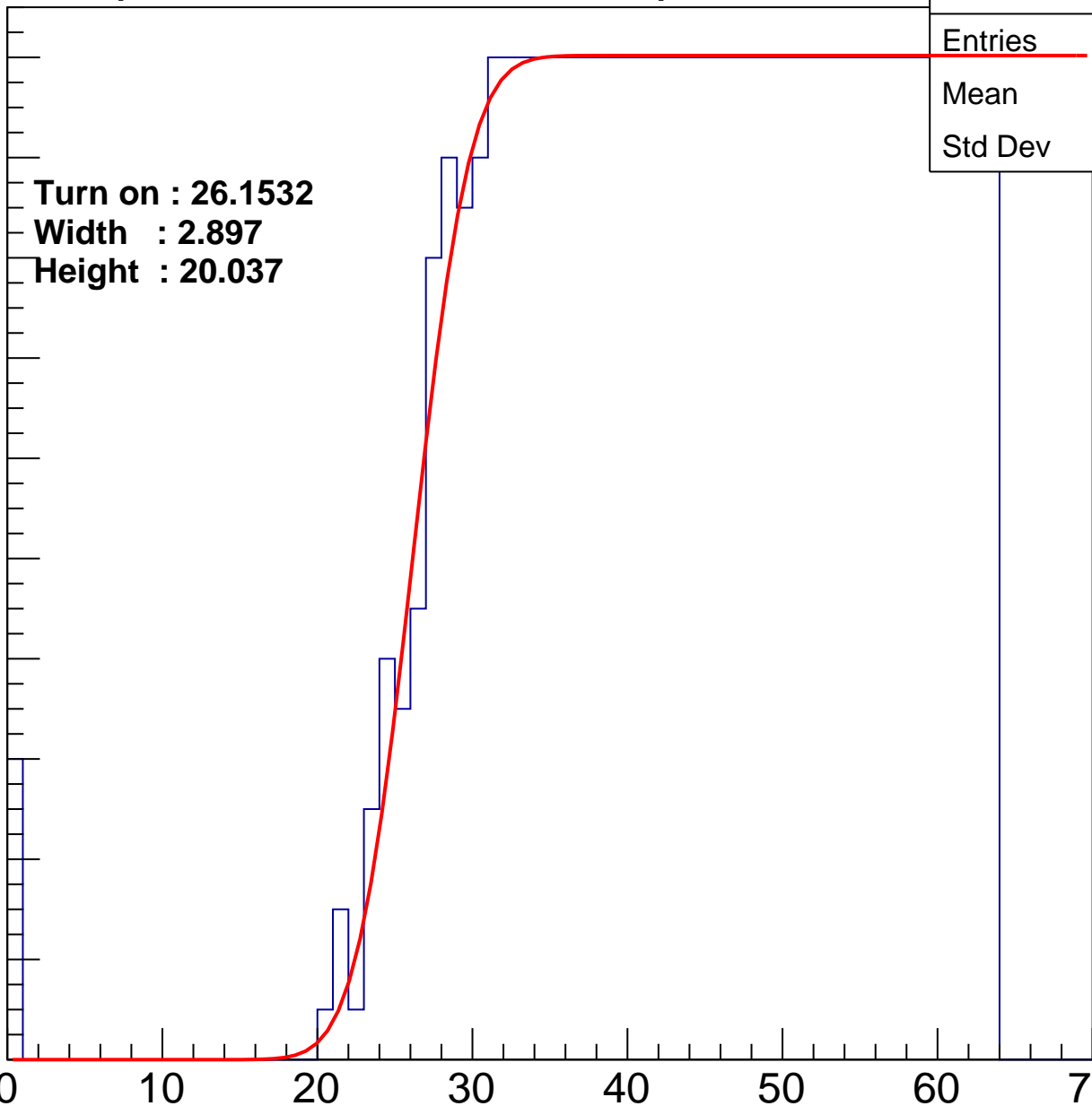
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 26.1532  
Width : 2.897  
Height : 20.037

Entries	769
Mean	43.97
Std Dev	11.82

ampl



# B0L101S, U15-ch99

calib\_packv5\_042523\_0143.root, FC#1, port C1

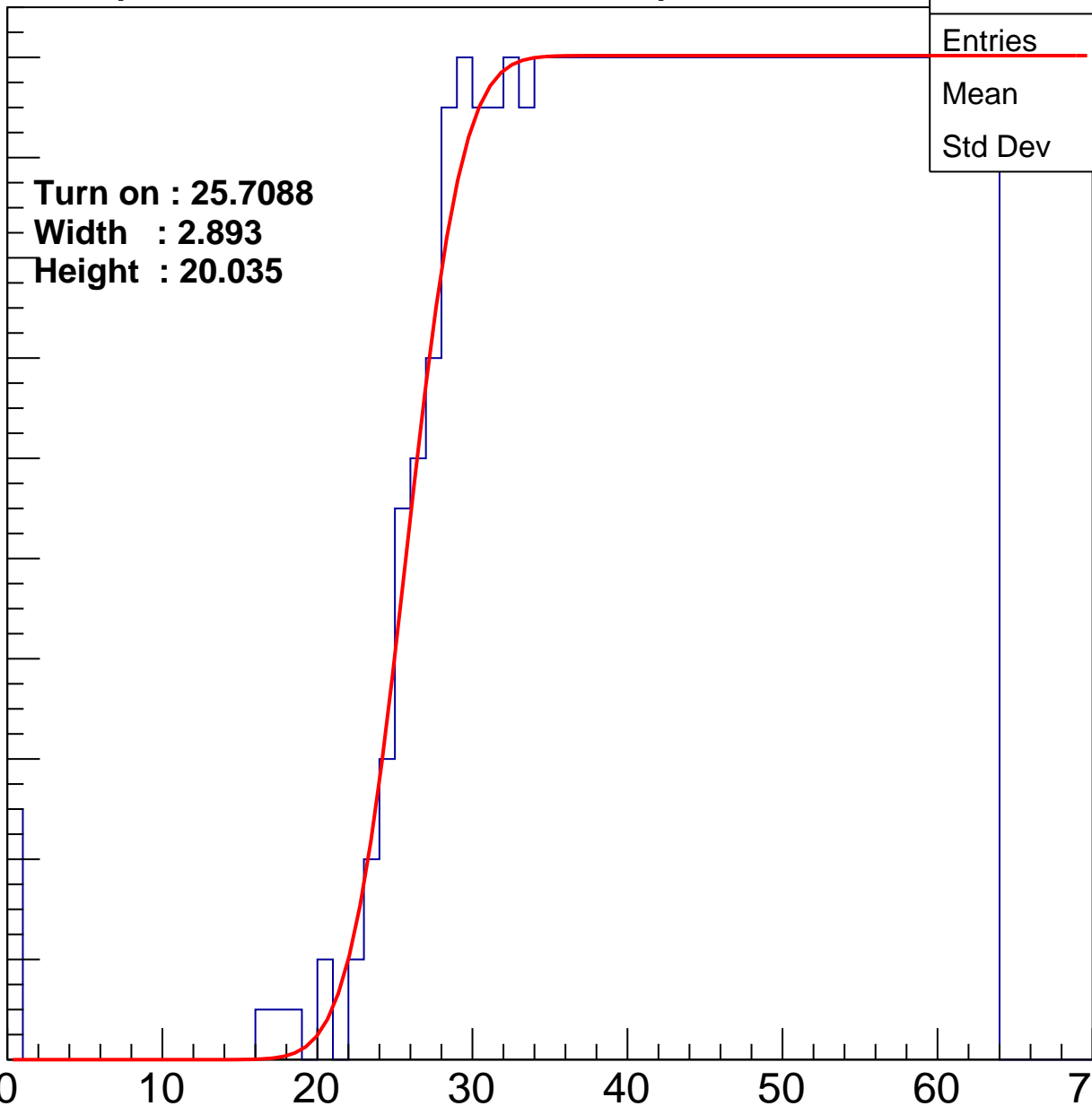
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 25.7088**  
**Width : 2.893**  
**Height : 20.035**

Entries	775
Mean	43.84
Std Dev	11.84

ampl



# B0L101S, U15-ch100

calib\_packv5\_042523\_0143.root, FC#1, port C1

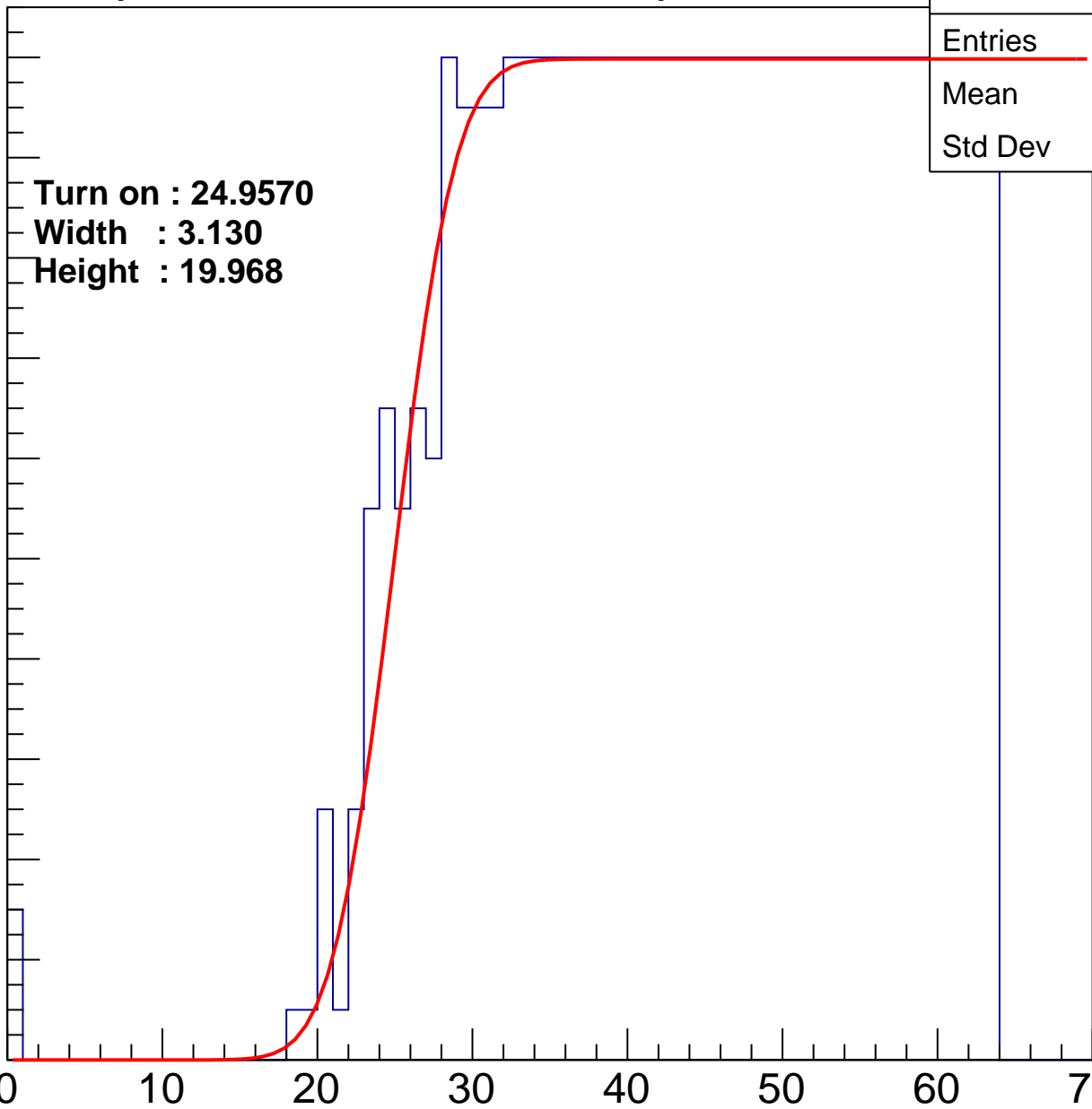
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 24.9570**  
**Width : 3.130**  
**Height : 19.968**

Entries	793
Mean	43.43
Std Dev	11.94

ampl



# B0L101S, U15-ch101

calib\_packv5\_042523\_0143.root, FC#1, port C1

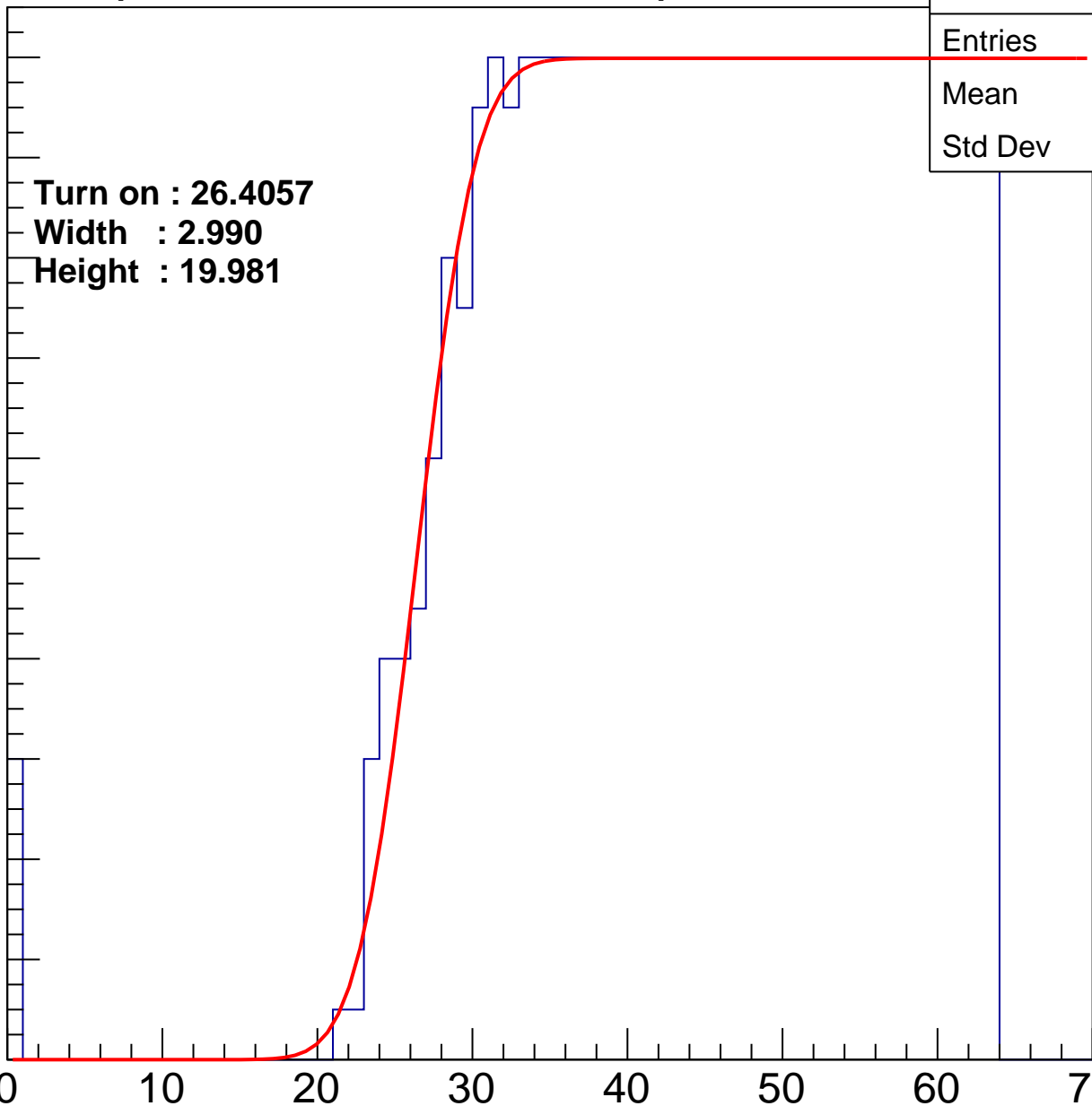
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 26.4057**  
**Width : 2.990**  
**Height : 19.981**

Entries	760
Mean	44.17
Std Dev	11.73

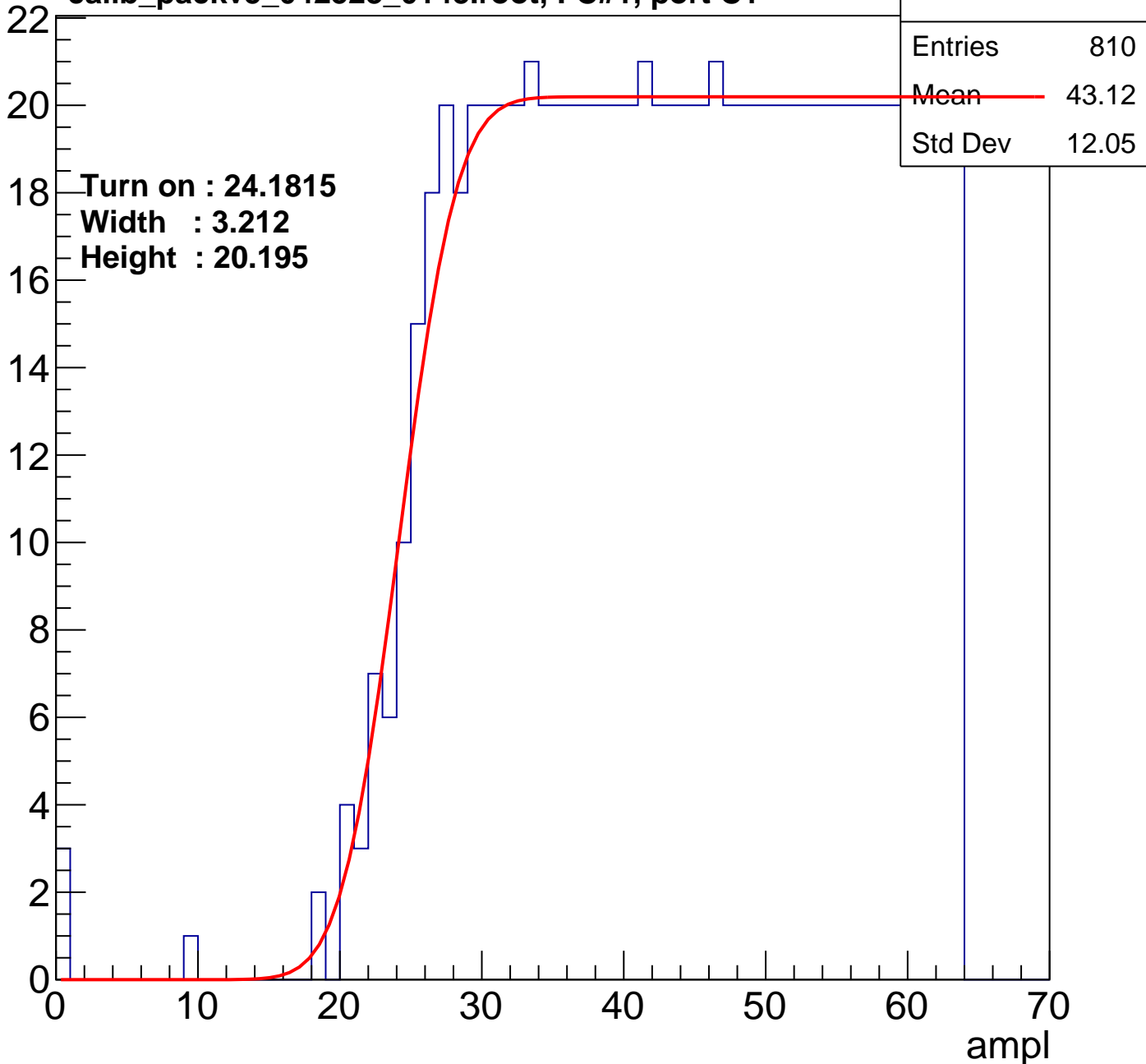
ampl



# B0L101S, U15-ch102

calib\_packv5\_042523\_0143.root, FC#1, port C1

Entry





# B0L101S, U15-ch103

calib\_packv5\_042523\_0143.root, FC#1, port C1

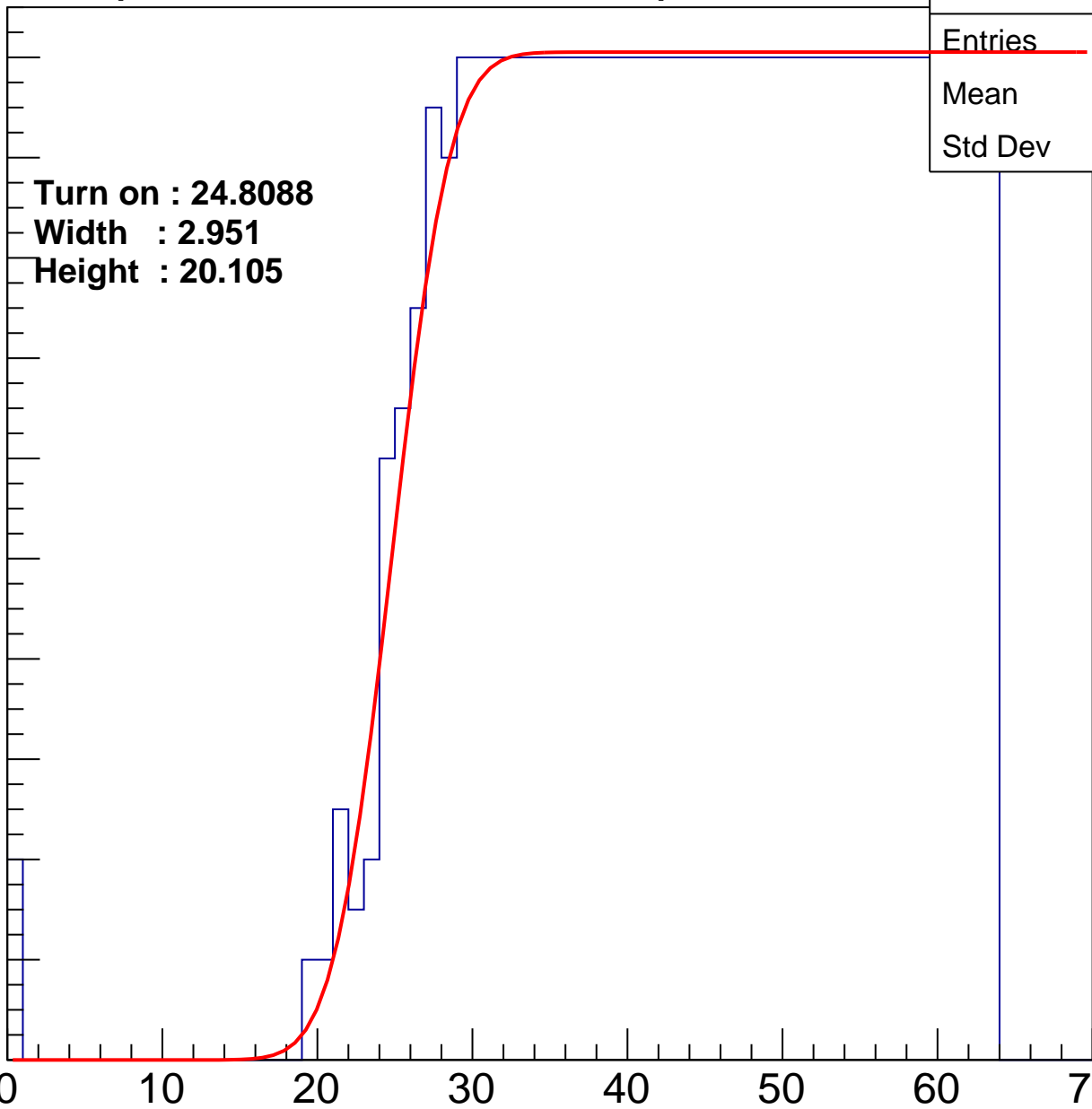
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 24.8088**  
**Width : 2.951**  
**Height : 20.105**

Entries	797
Mean	43.36
Std Dev	11.98

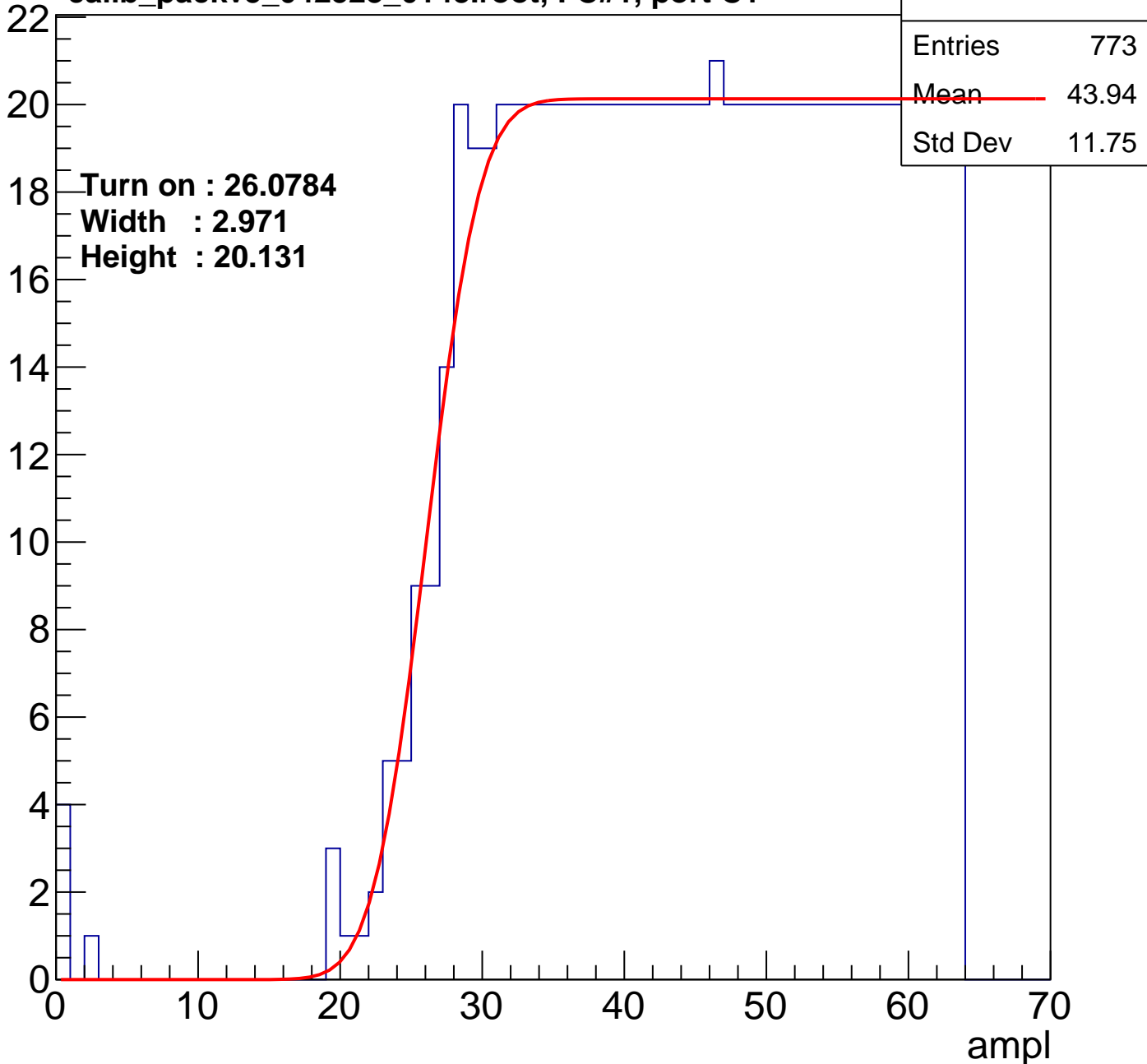
ampl



# B0L101S, U15-ch104

calib\_packv5\_042523\_0143.root, FC#1, port C1

Entry



# B0L101S, U15-ch105

calib\_packv5\_042523\_0143.root, FC#1, port C1

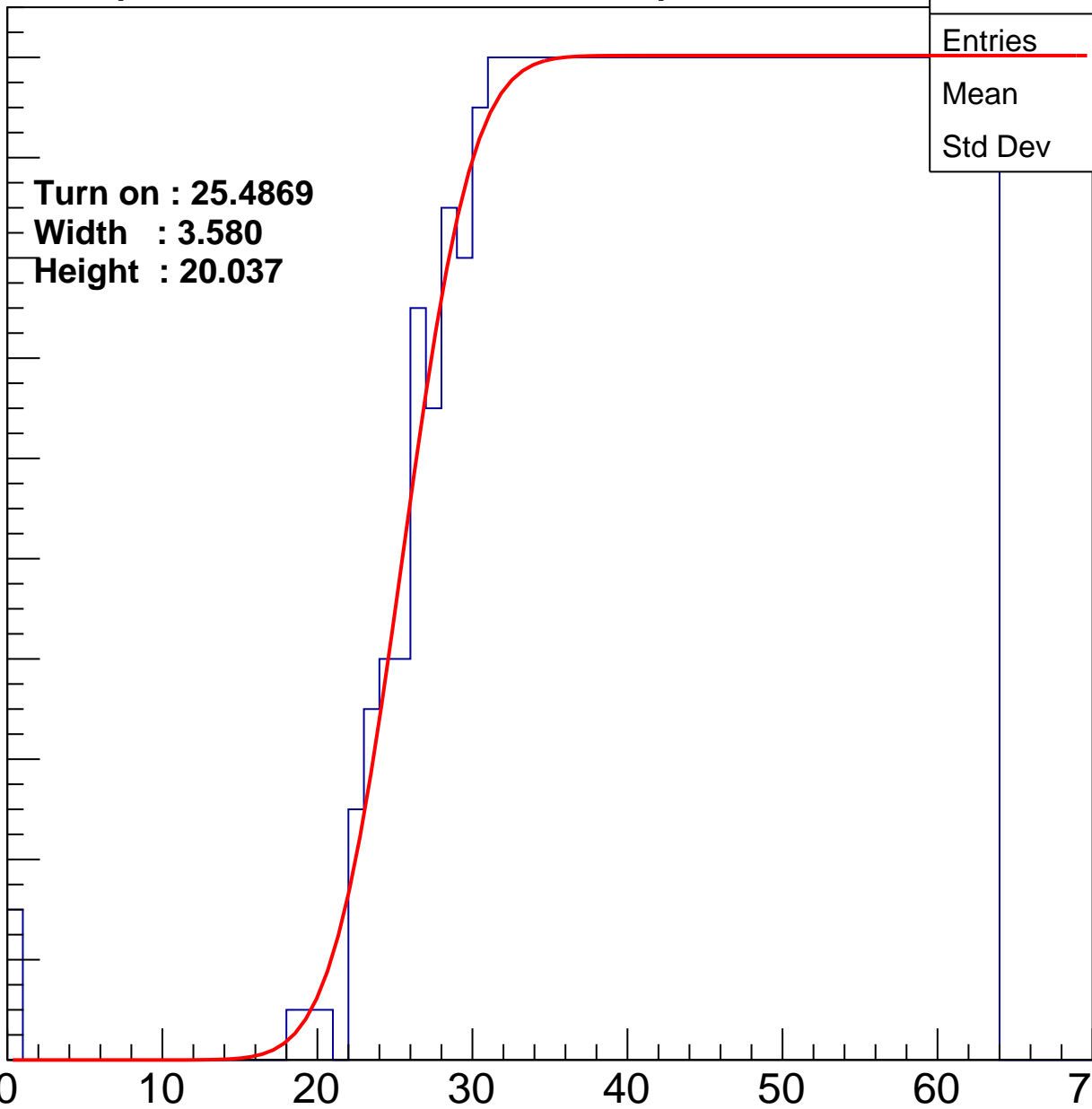
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 25.4869**  
**Width : 3.580**  
**Height : 20.037**

Entries	774
Mean	43.92
Std Dev	11.67

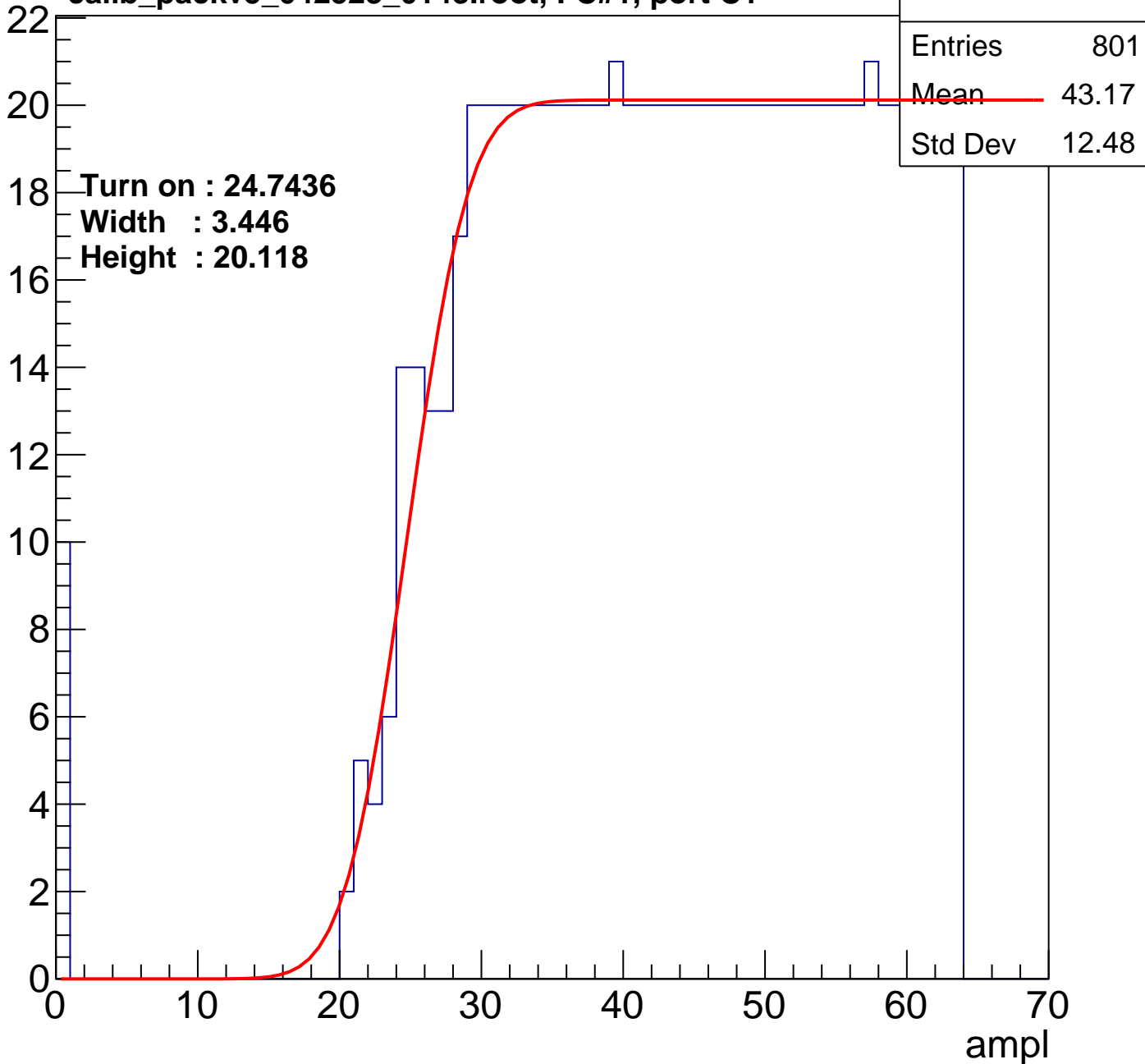
ampl



# B0L101S, U15-ch106

calib\_packv5\_042523\_0143.root, FC#1, port C1

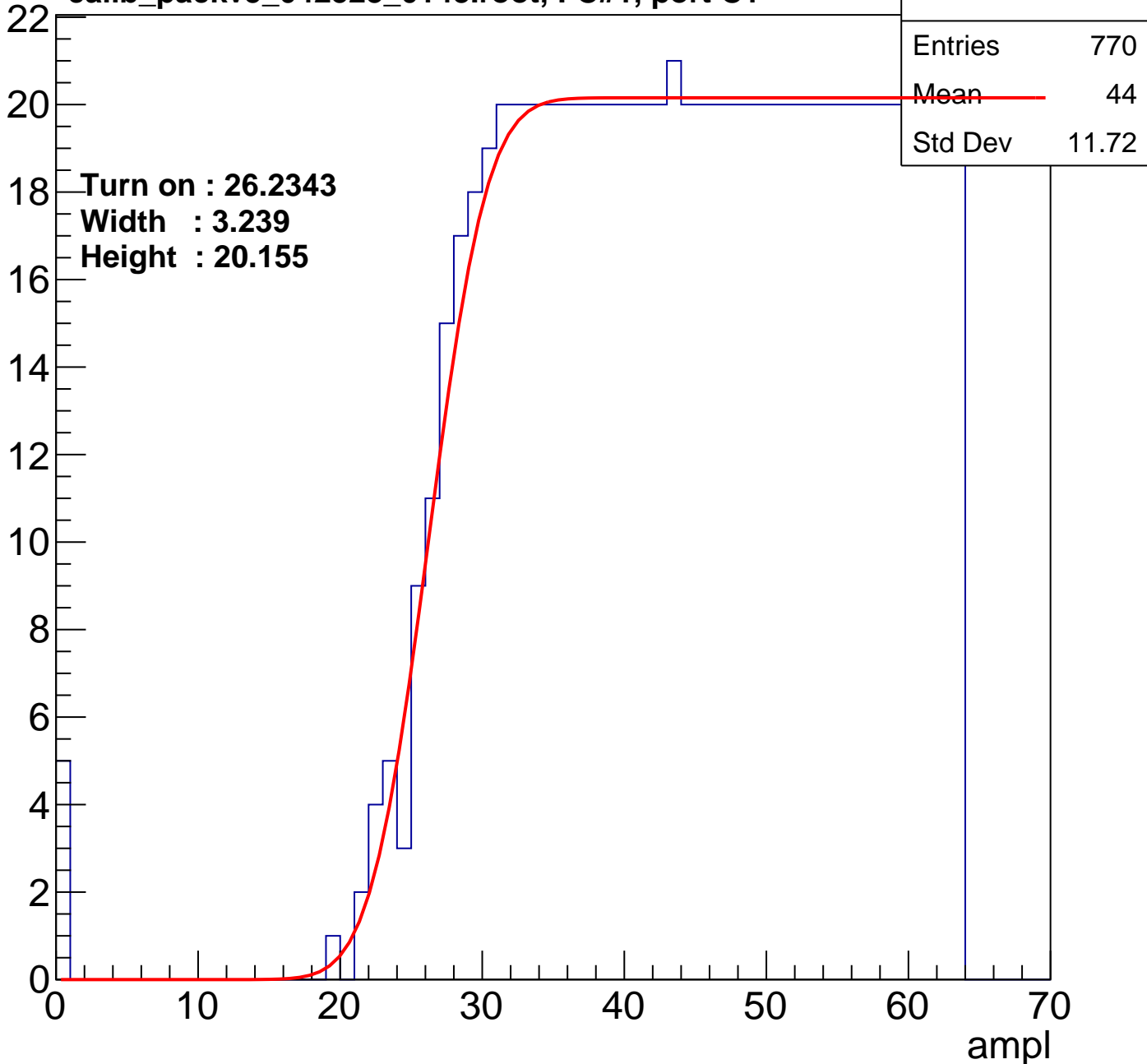
Entry



# B0L101S, U15-ch107

calib\_packv5\_042523\_0143.root, FC#1, port C1

Entry

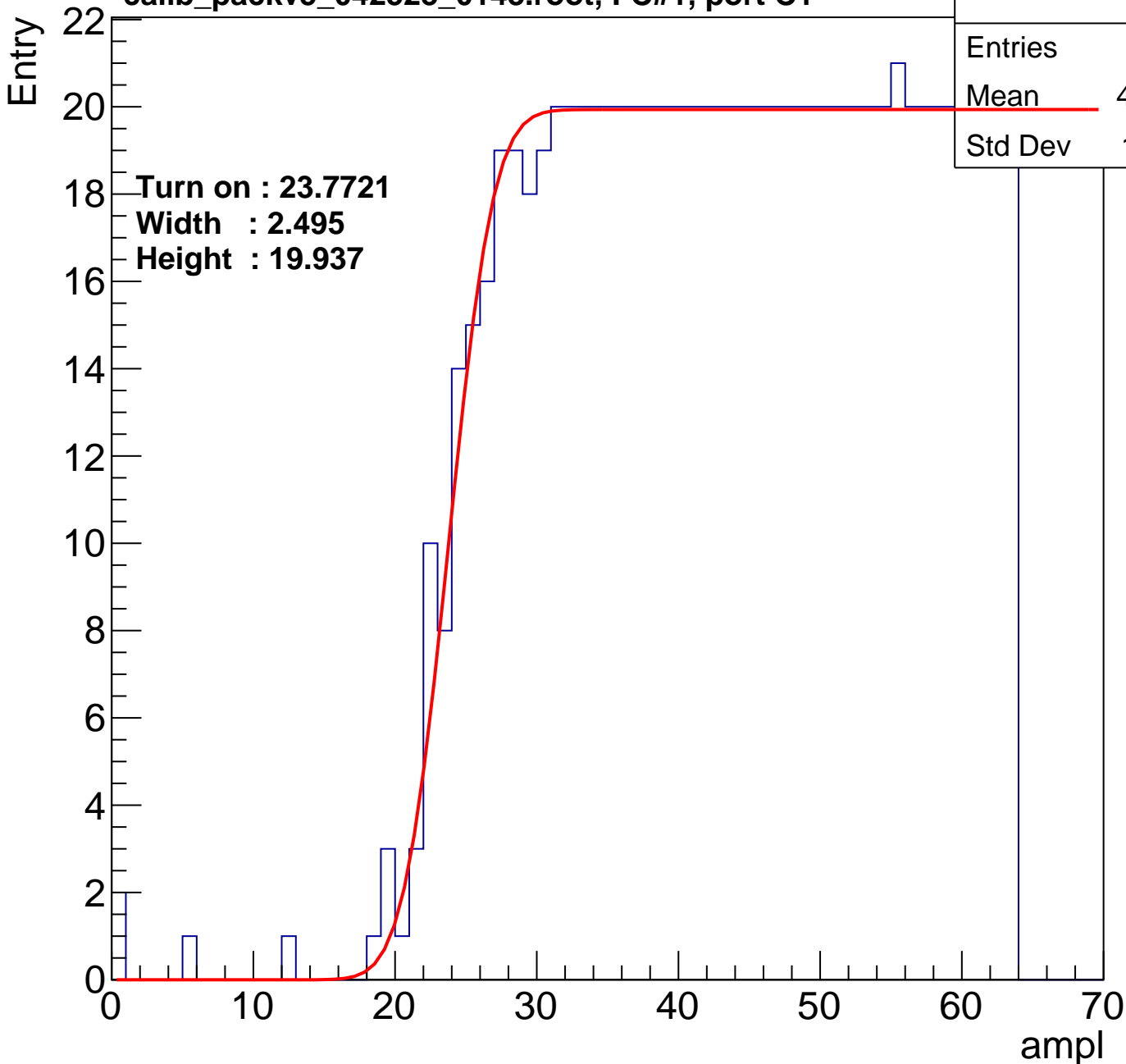


# B0L101S, U15-ch108

calib\_packv5\_042523\_0143.root, FC#1, port C1

Entries	811
Mean	43.06
Std Dev	12.11

Turn on : 23.7721  
Width : 2.495  
Height : 19.937



# B0L101S, U15-ch109

calib\_packv5\_042523\_0143.root, FC#1, port C1

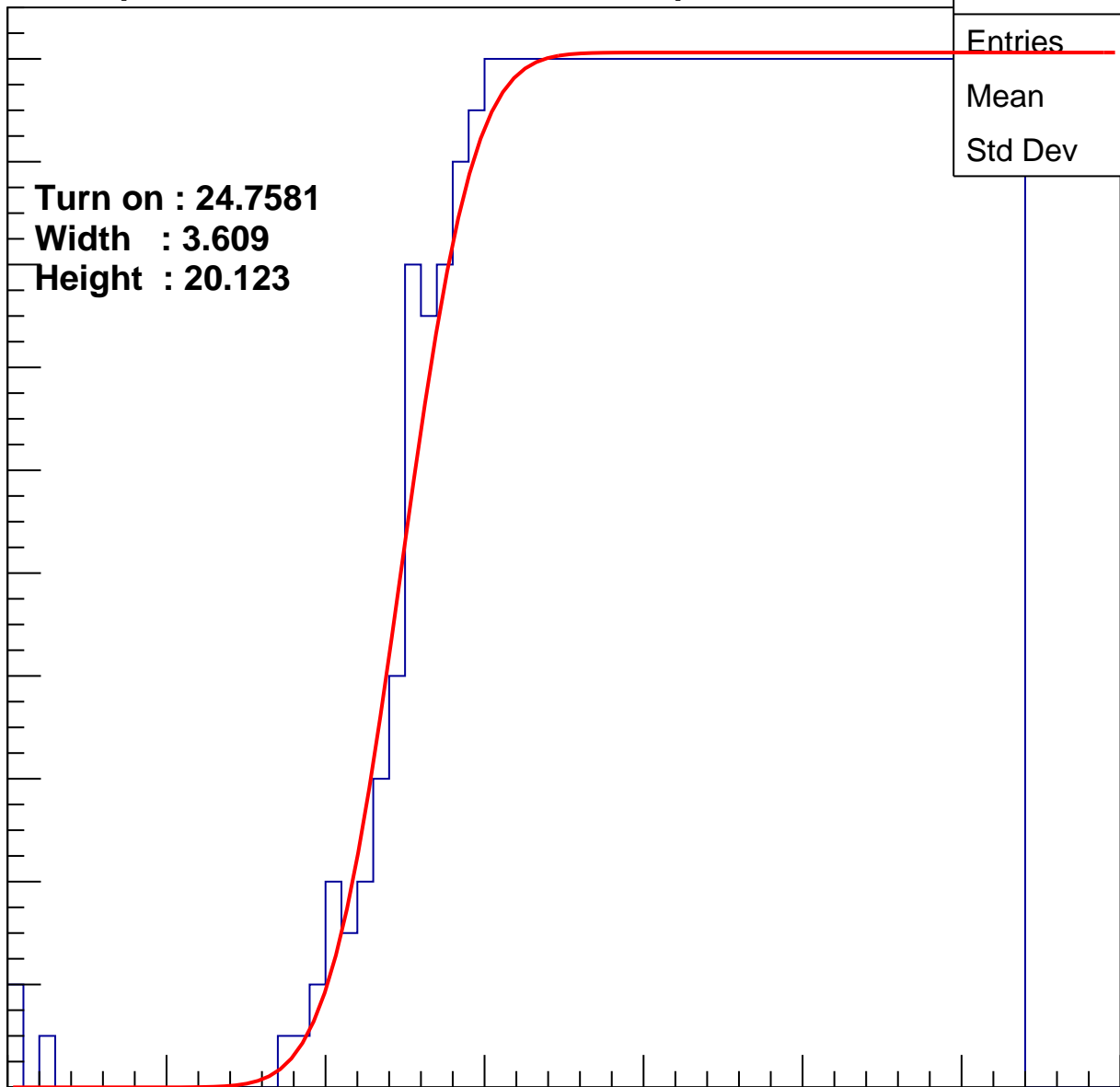
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 24.7581  
Width : 3.609  
Height : 20.123

Entries	796
Mean	43.38
Std Dev	11.94

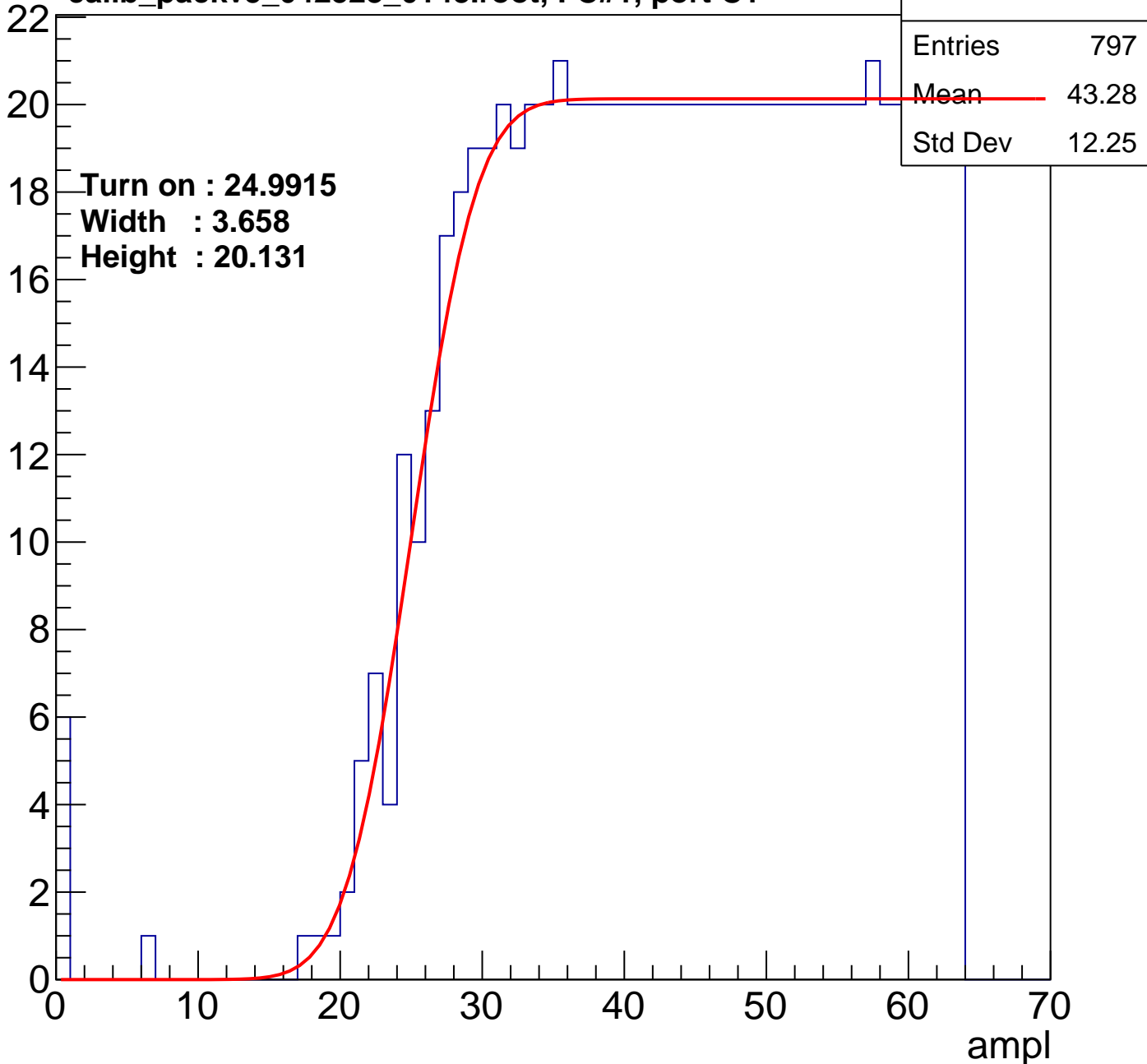
ampl



# B0L101S, U15-ch110

calib\_packv5\_042523\_0143.root, FC#1, port C1

Entry





# B0L101S, U15-ch111

calib\_packv5\_042523\_0143.root, FC#1, port C1

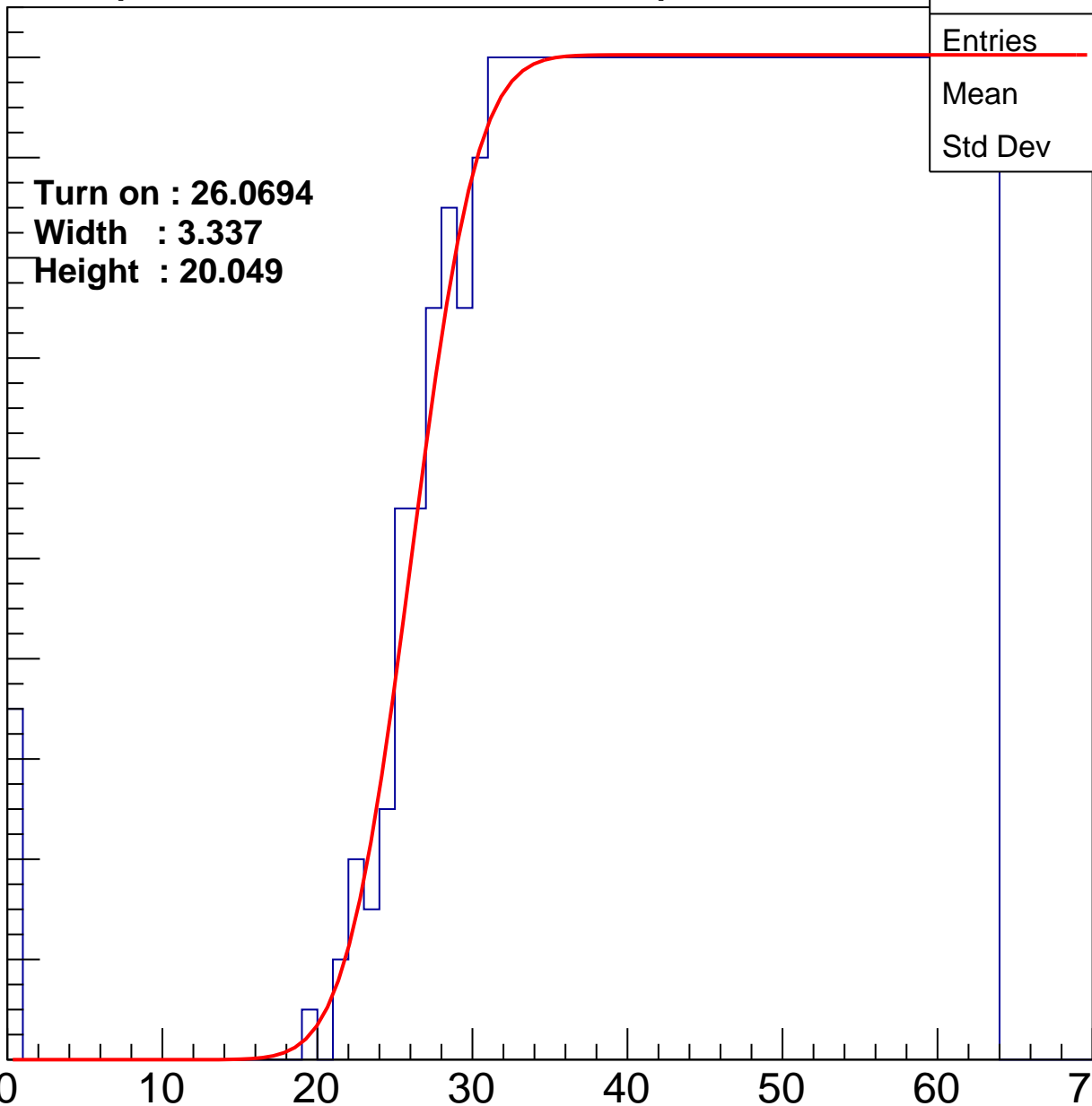
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 26.0694**  
**Width : 3.337**  
**Height : 20.049**

Entries	769
Mean	43.92
Std Dev	11.93

ampl



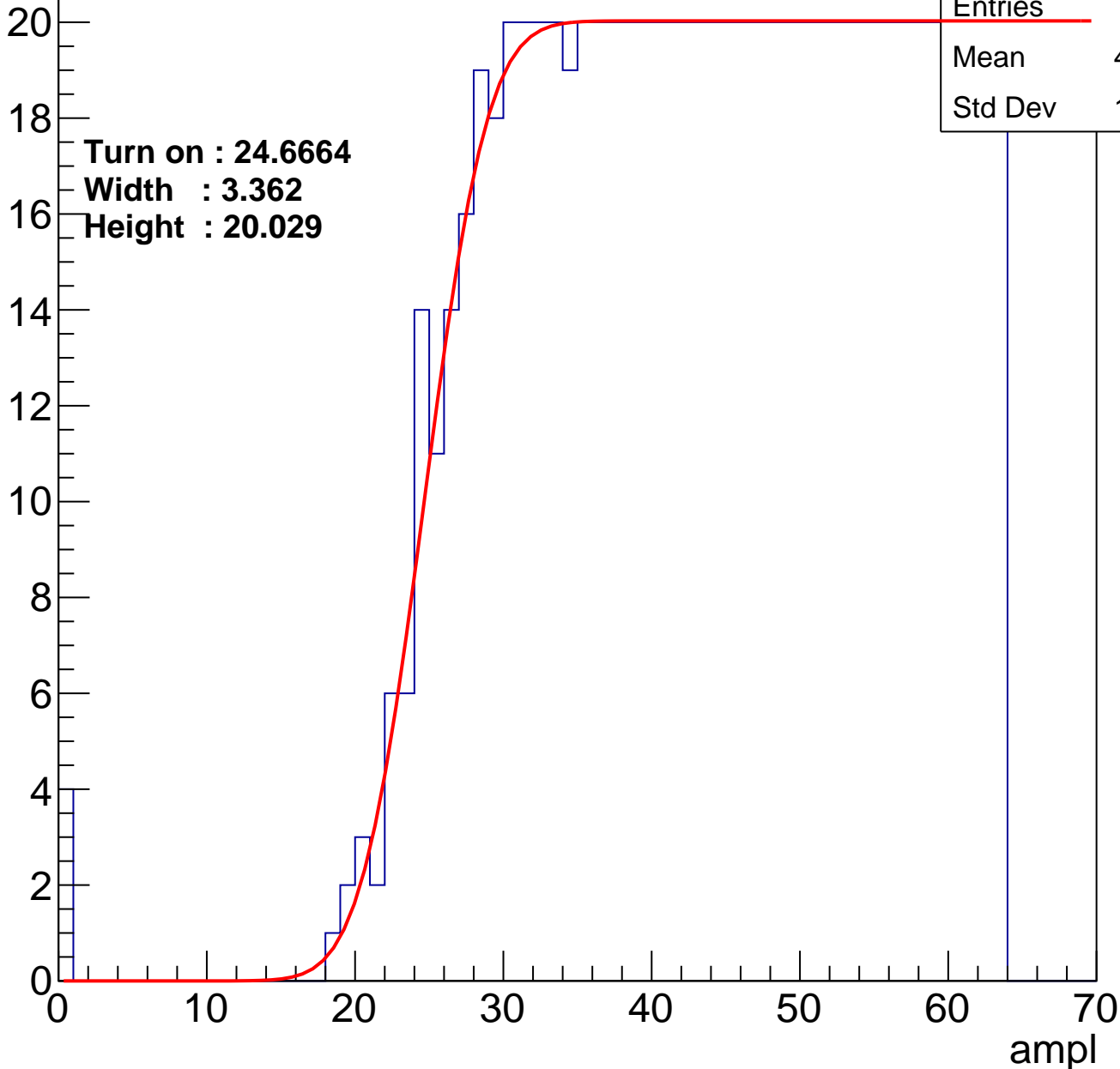
# B0L101S, U15-ch112

calib\_packv5\_042523\_0143.root, FC#1, port C1

Entries	795
Mean	43.36
Std Dev	12.02

Turn on : 24.6664  
Width : 3.362  
Height : 20.029

Entry



ampl

# B0L101S, U15-ch113

calib\_packv5\_042523\_0143.root, FC#1, port C1

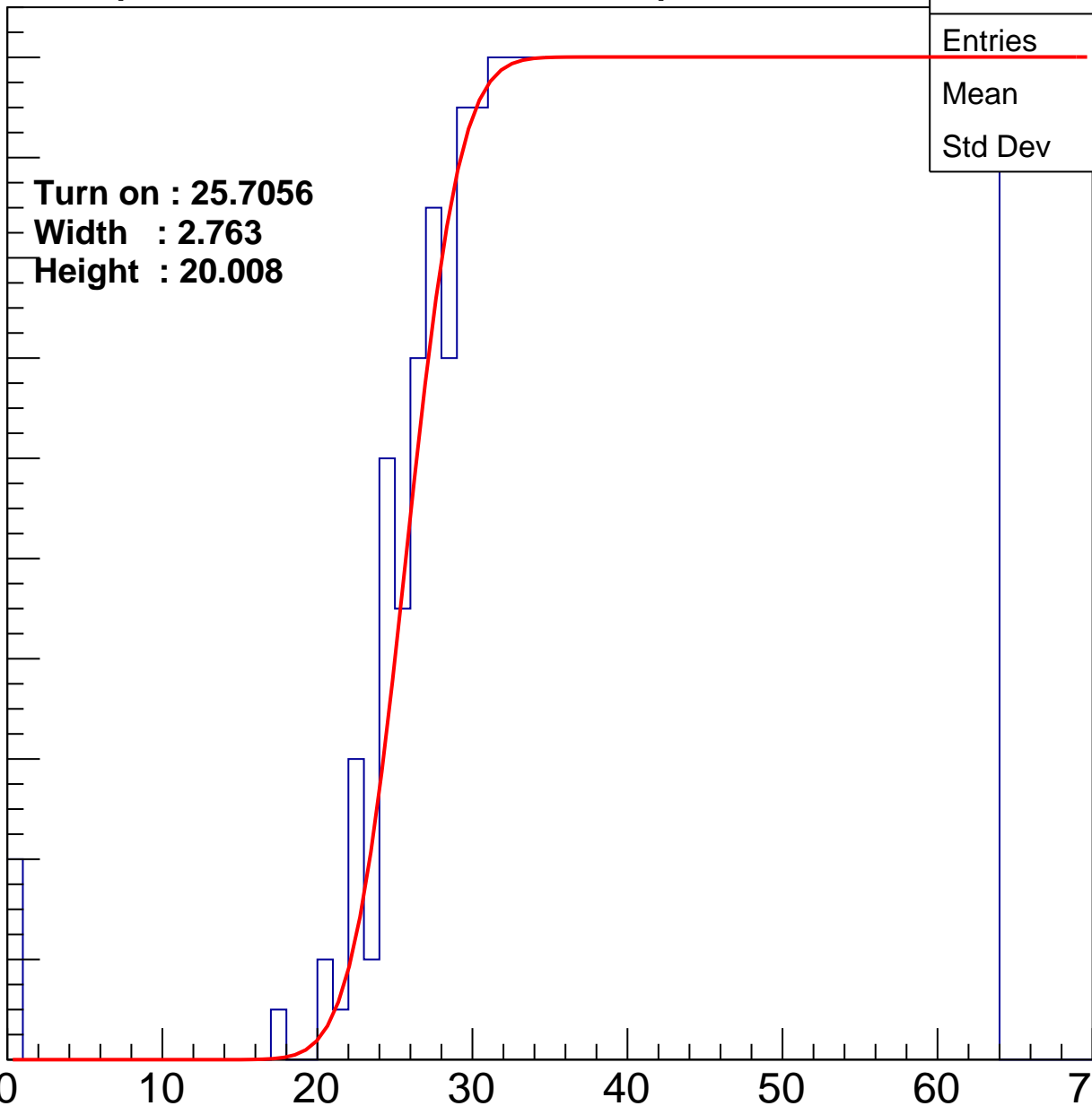
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 25.7056**  
**Width : 2.763**  
**Height : 20.008**

Entries	780
Mean	43.75
Std Dev	11.81

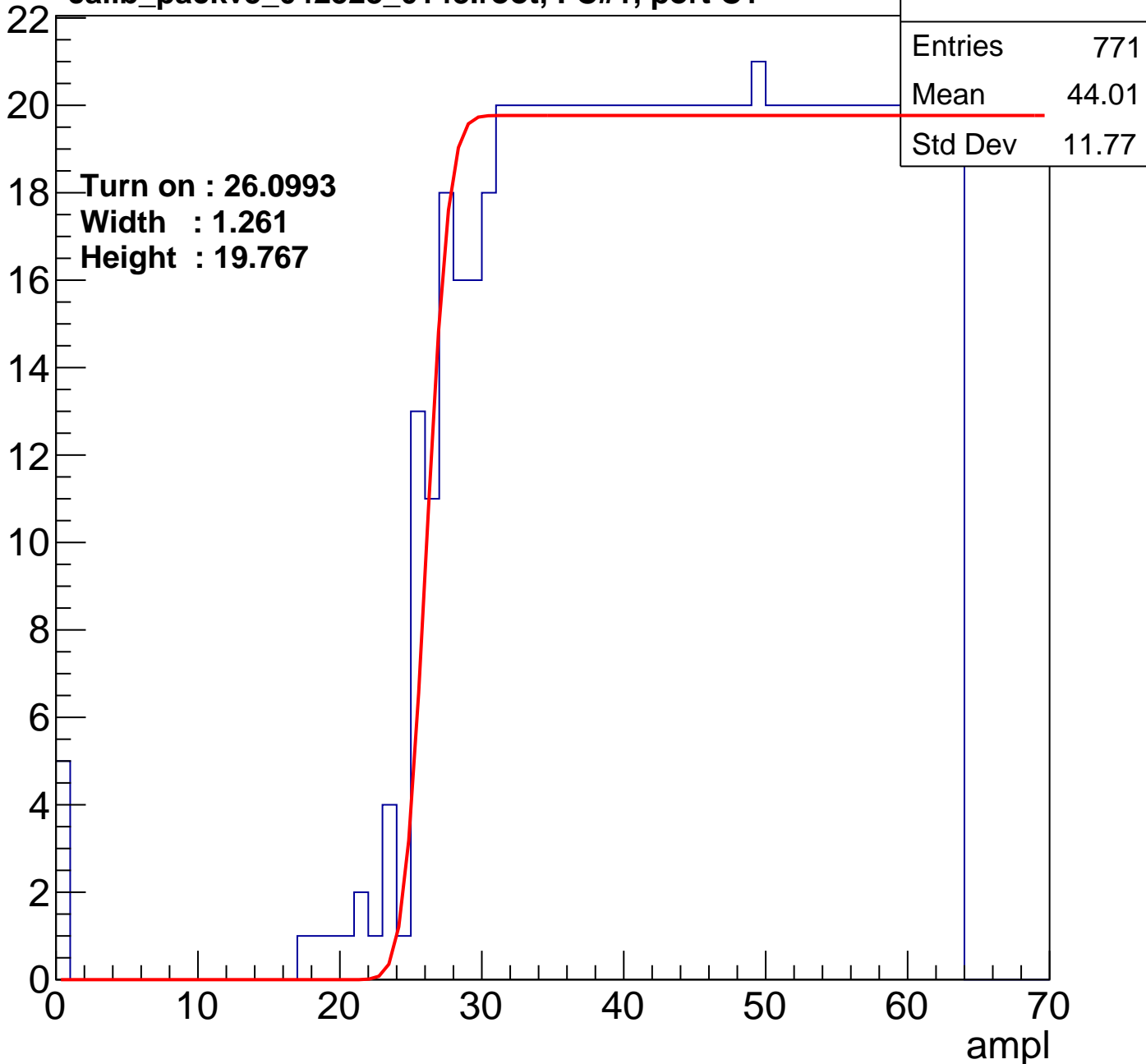
ampl



# B0L101S, U15-ch114

calib\_packv5\_042523\_0143.root, FC#1, port C1

Entry



# B0L101S, U15-ch115

calib\_packv5\_042523\_0143.root, FC#1, port C1

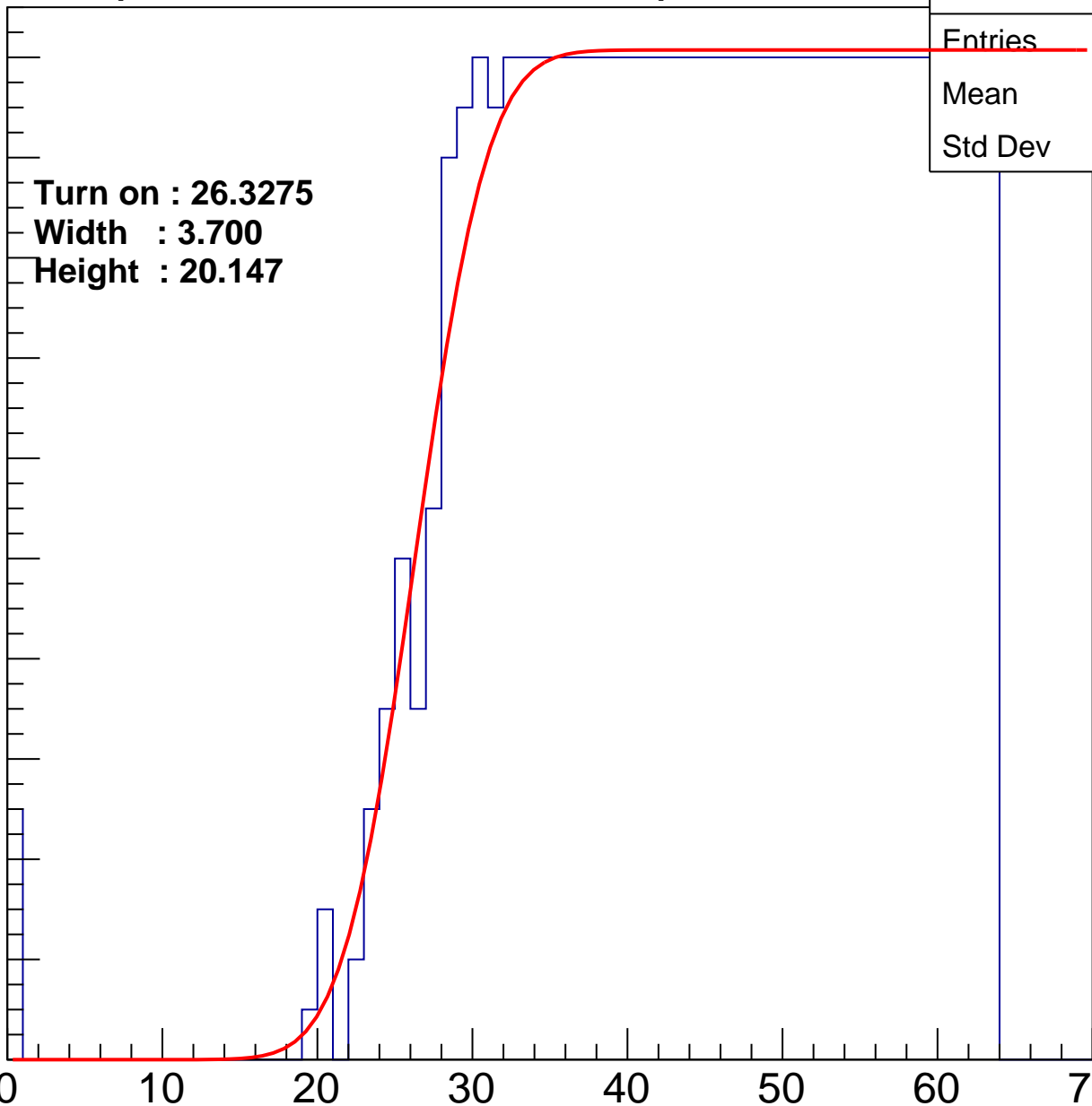
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 26.3275**  
**Width : 3.700**  
**Height : 20.147**

Entries	767
Mean	44.04
Std Dev	11.73

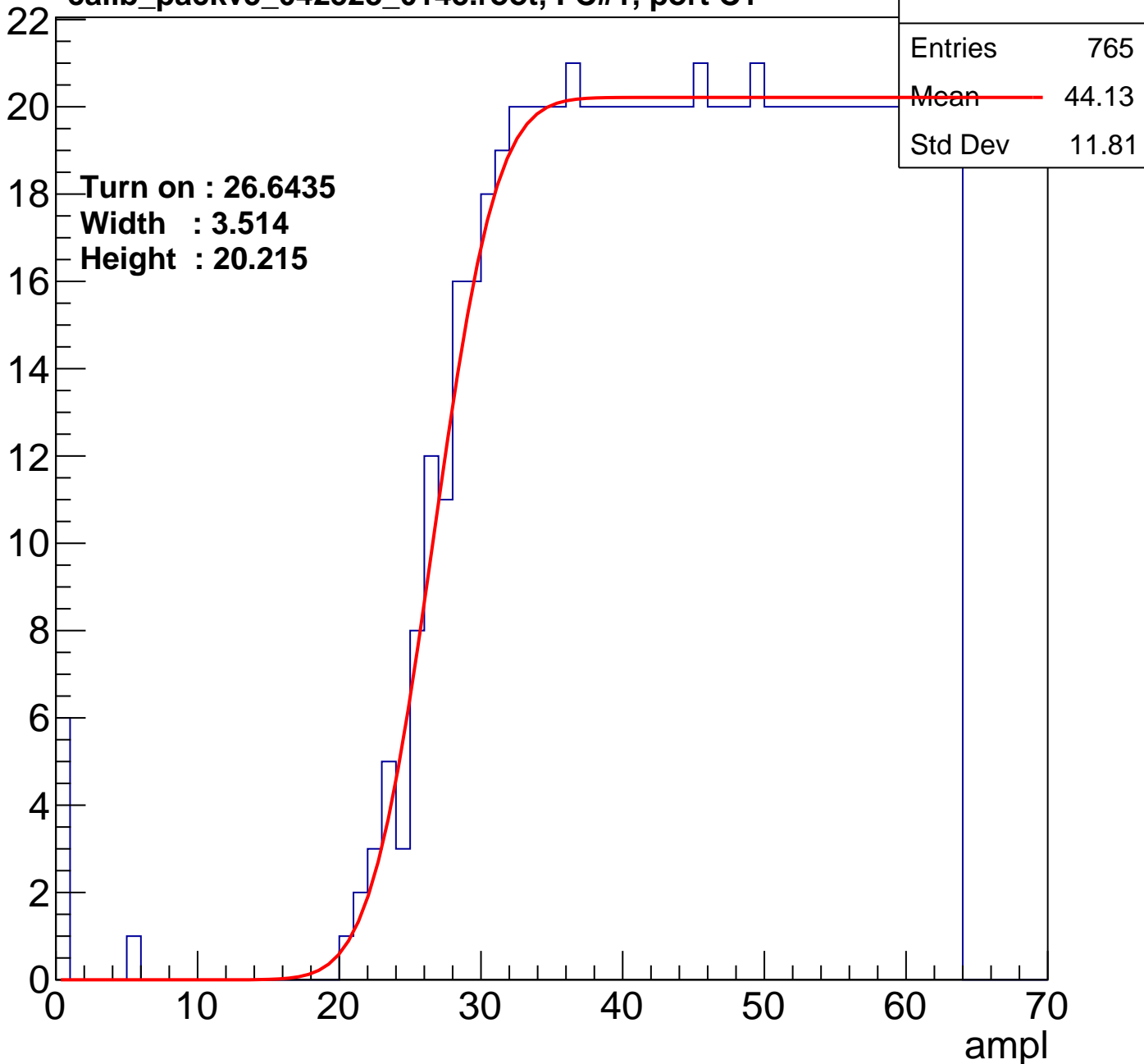
ampl



# B0L101S, U15-ch116

calib\_packv5\_042523\_0143.root, FC#1, port C1

Entry



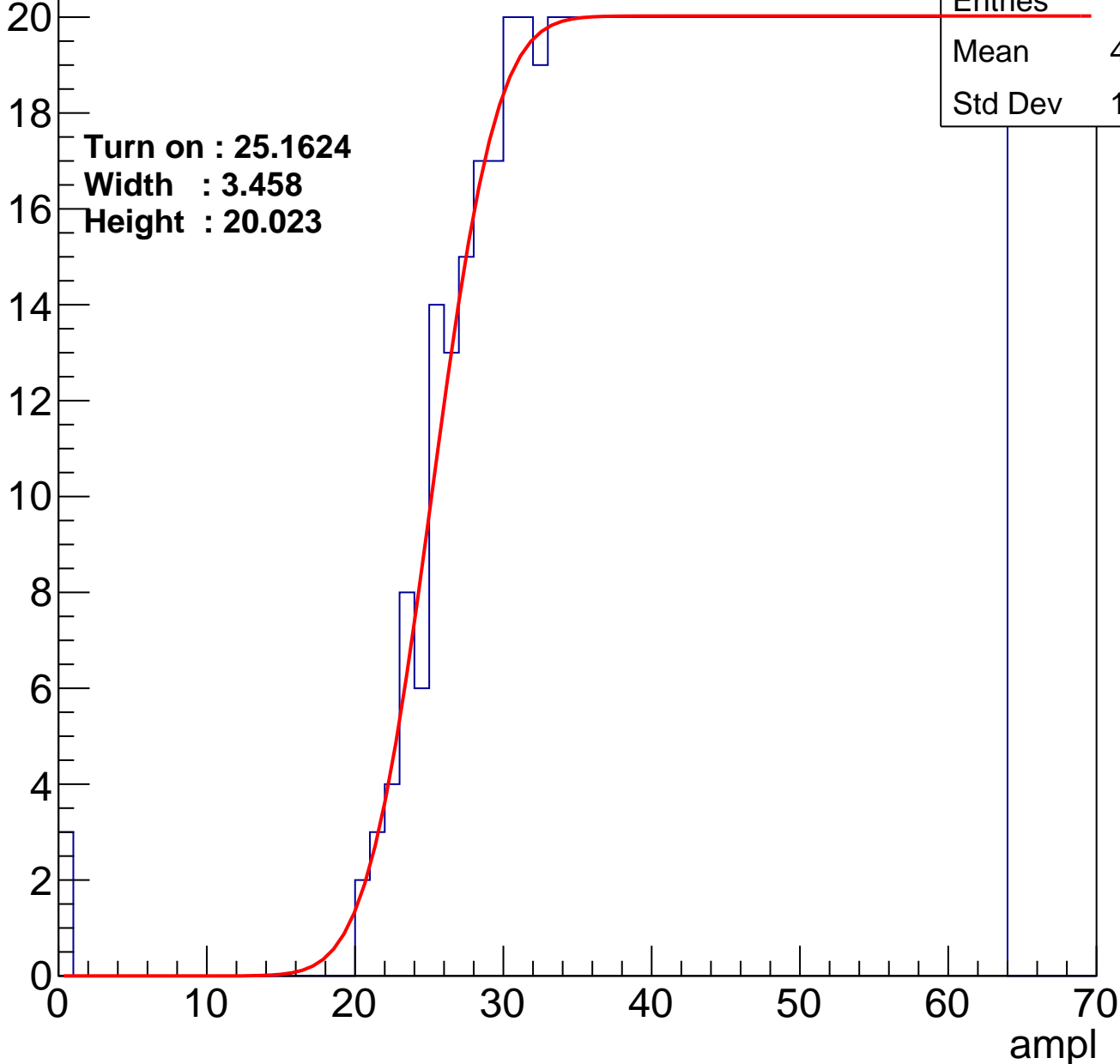
# B0L101S, U15-ch117

calib\_packv5\_042523\_0143.root, FC#1, port C1

Entries	781
Mean	43.75
Std Dev	11.74

Turn on : 25.1624  
Width : 3.458  
Height : 20.023

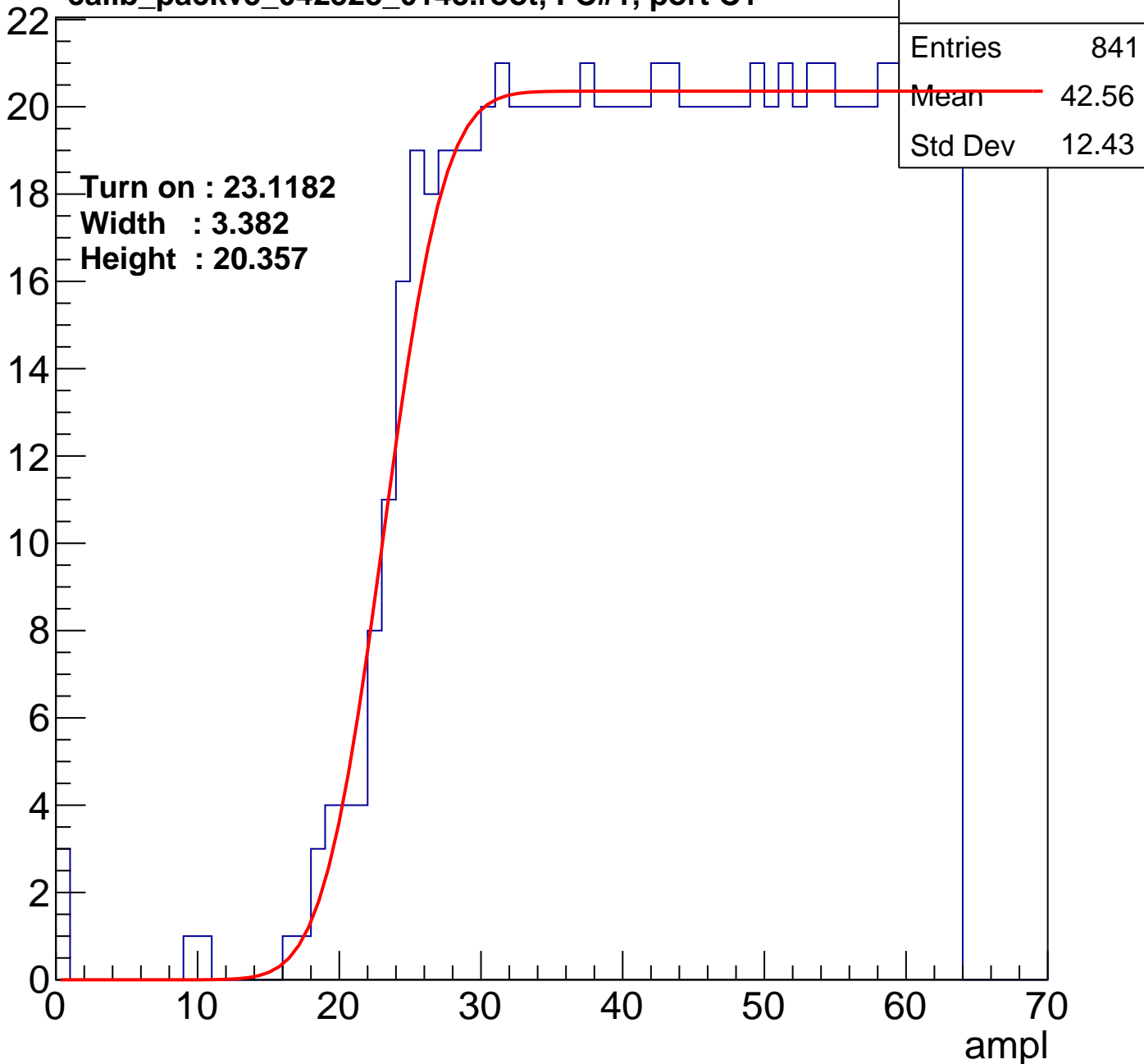
Entry



# B0L101S, U15-ch118

calib\_packv5\_042523\_0143.root, FC#1, port C1

Entry





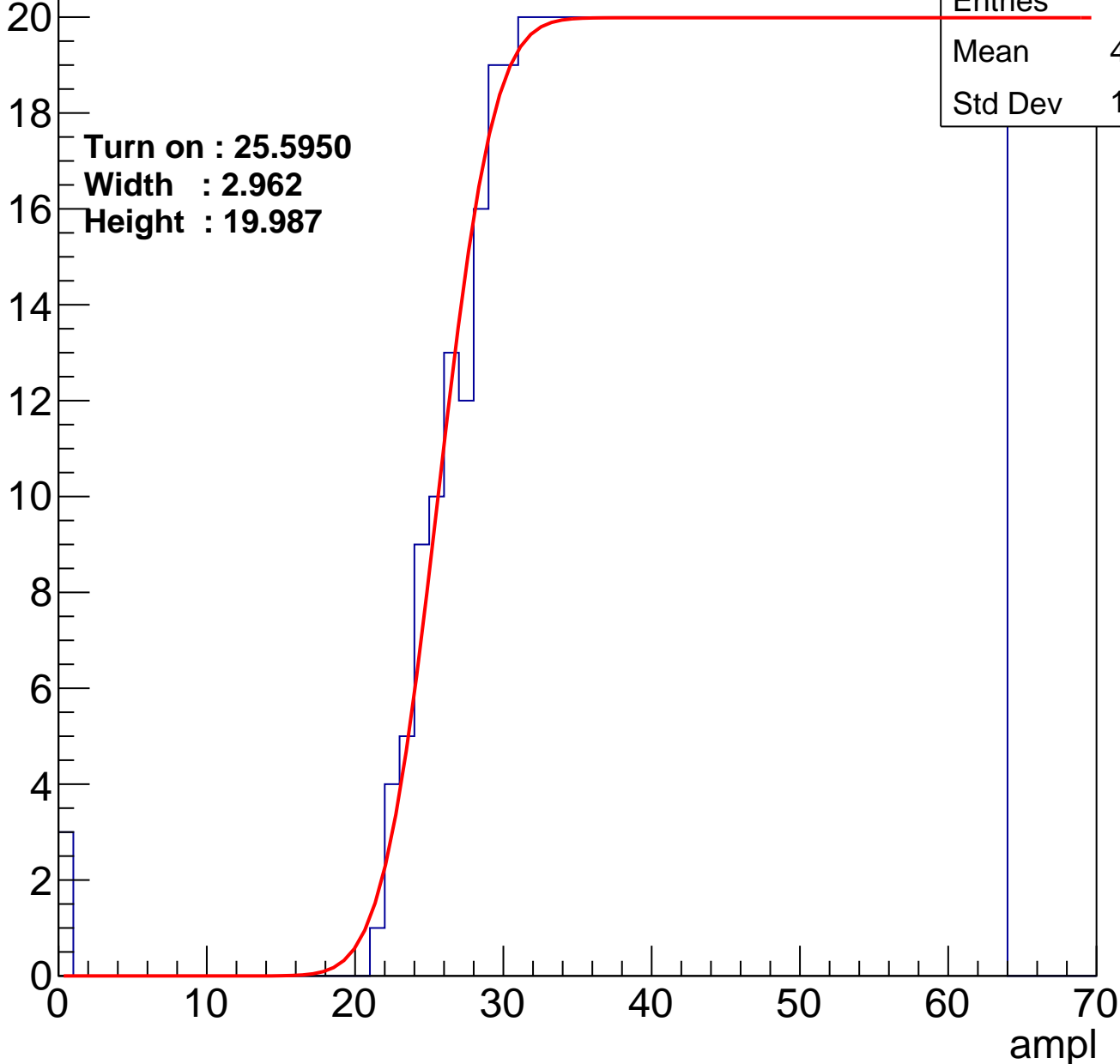
# B0L101S, U15-ch119

calib\_packv5\_042523\_0143.root, FC#1, port C1

Entries	771
Mean	44.02
Std Dev	11.57

**Turn on : 25.5950**  
**Width : 2.962**  
**Height : 19.987**

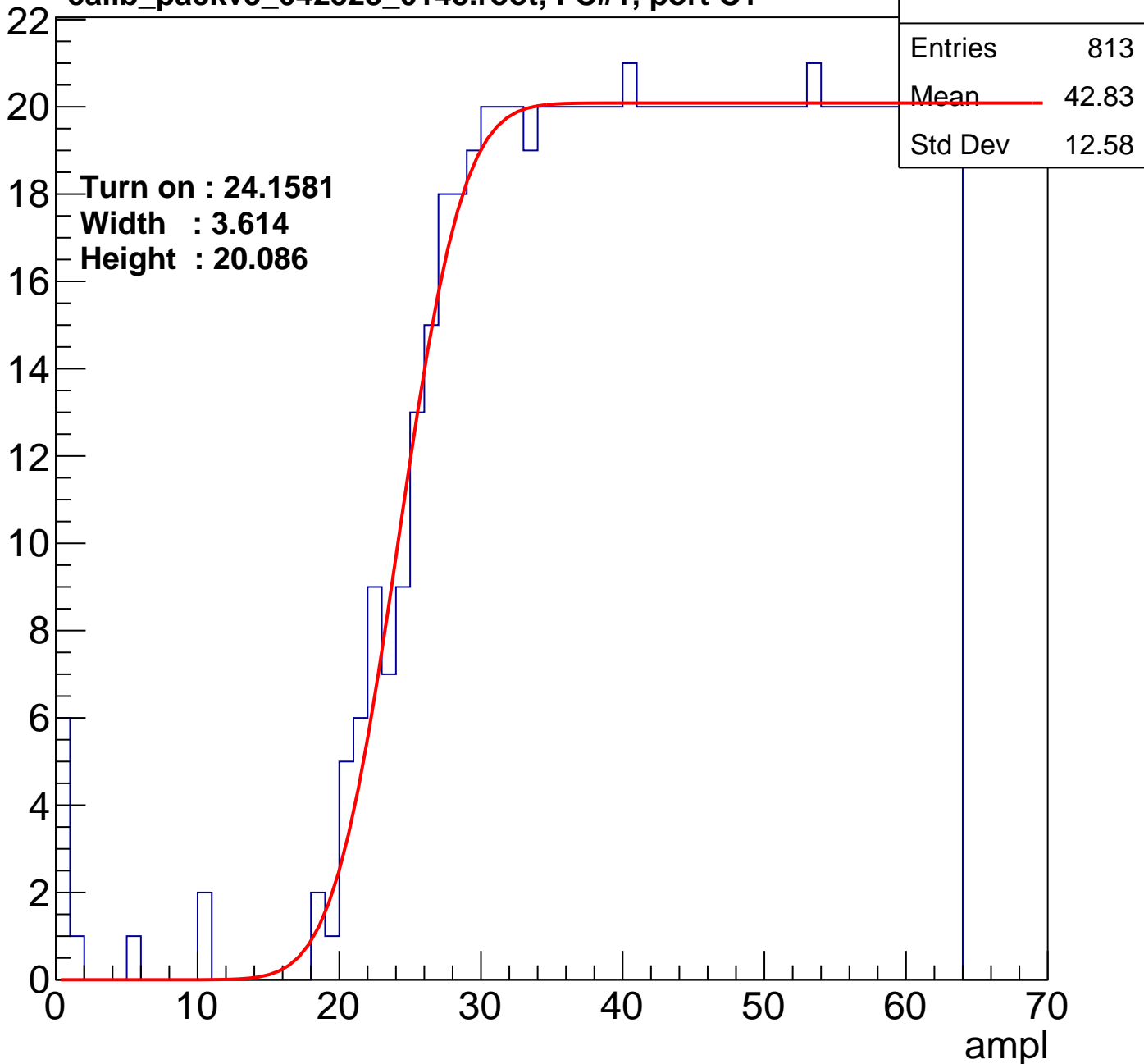
Entry



# B0L101S, U15-ch120

calib\_packv5\_042523\_0143.root, FC#1, port C1

Entry



# B0L101S, U15-ch121

calib\_packv5\_042523\_0143.root, FC#1, port C1

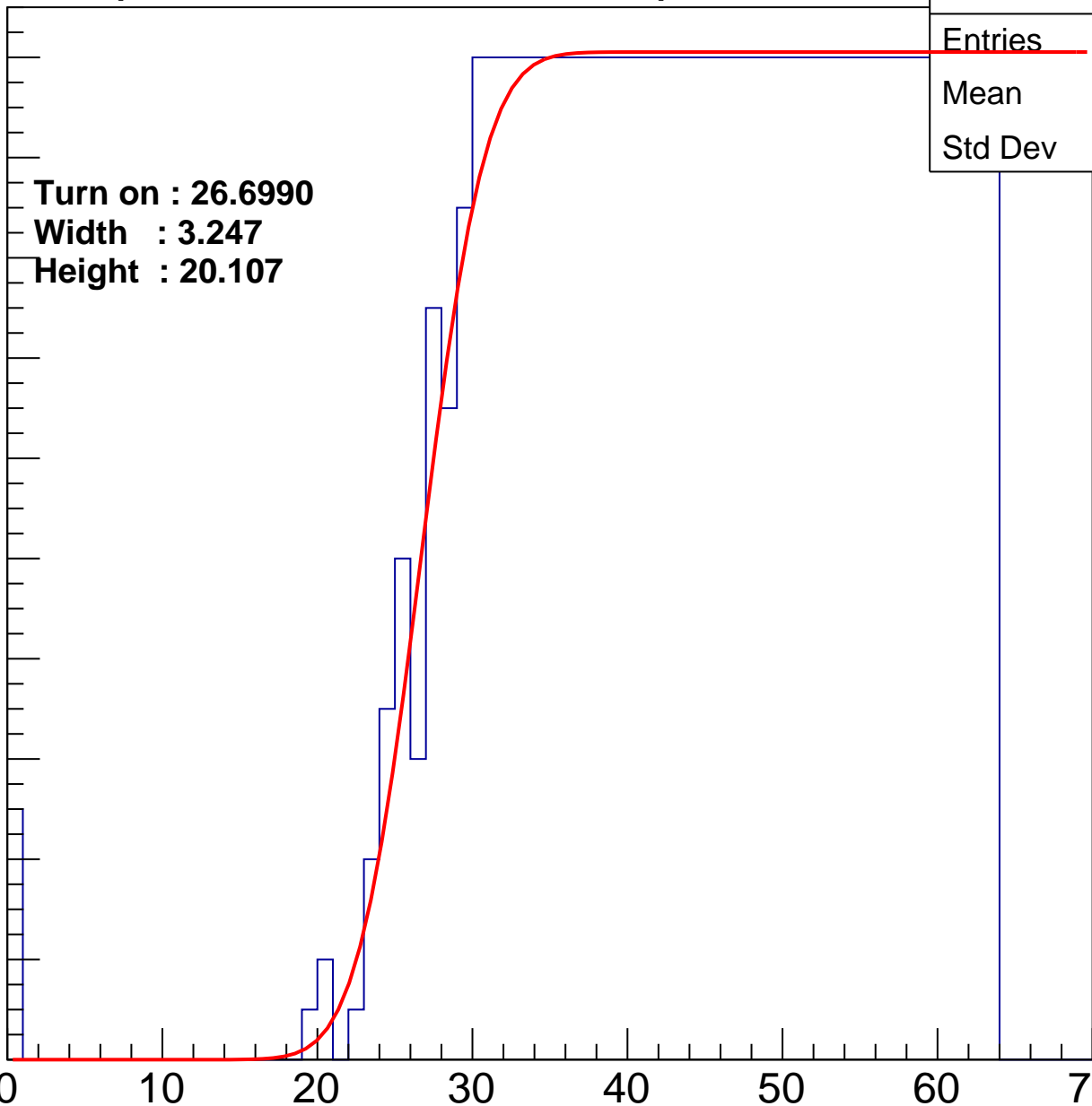
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 26.6990  
Width : 3.247  
Height : 20.107

Entries	761
Mean	44.19
Std Dev	11.65

ampl



# B0L101S, U15-ch122

calib\_packv5\_042523\_0143.root, FC#1, port C1

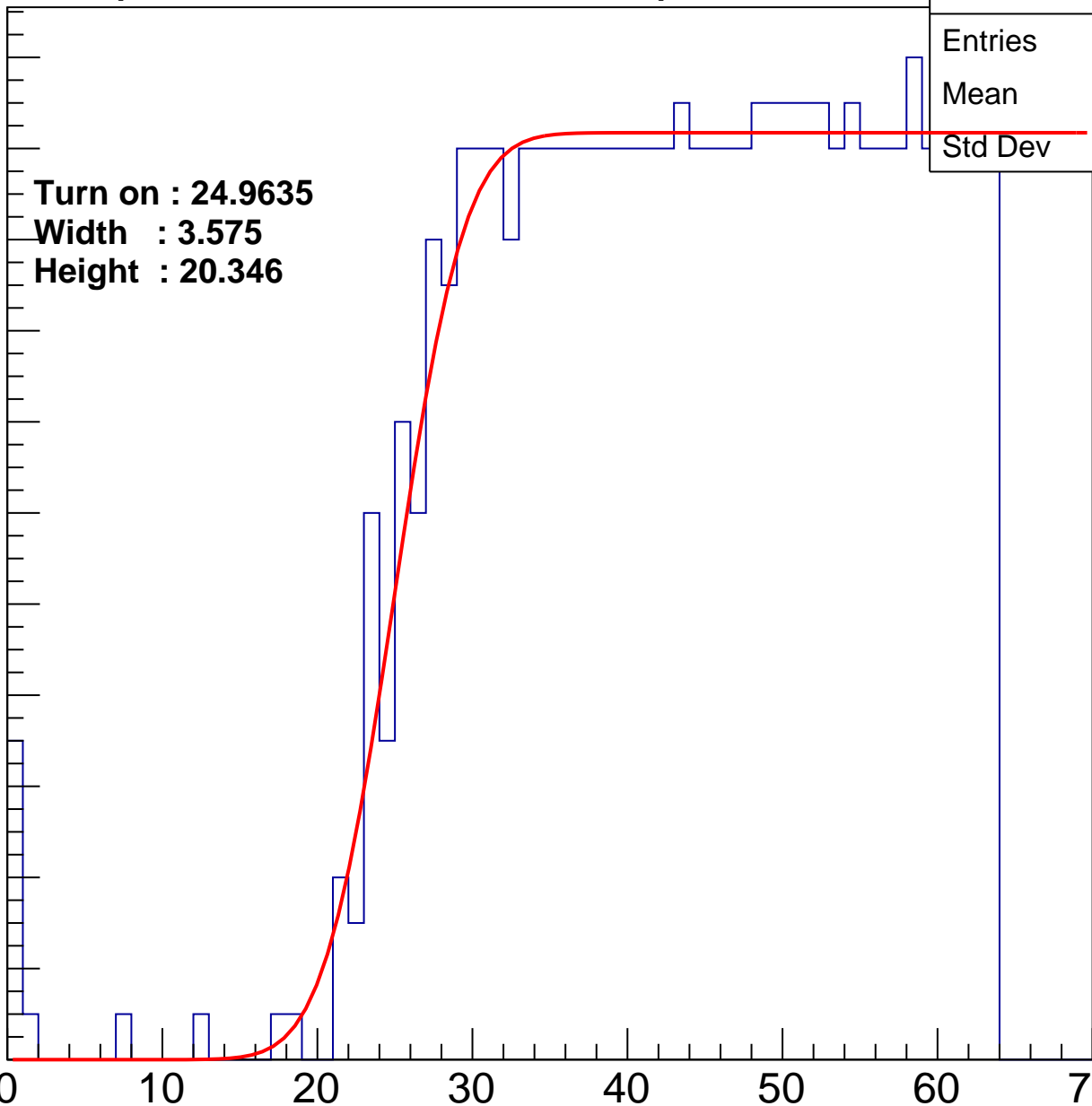
Entry

22  
20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 24.9635**  
**Width : 3.575**  
**Height : 20.346**

Entries	807
Mean	43.29
Std Dev	12.39

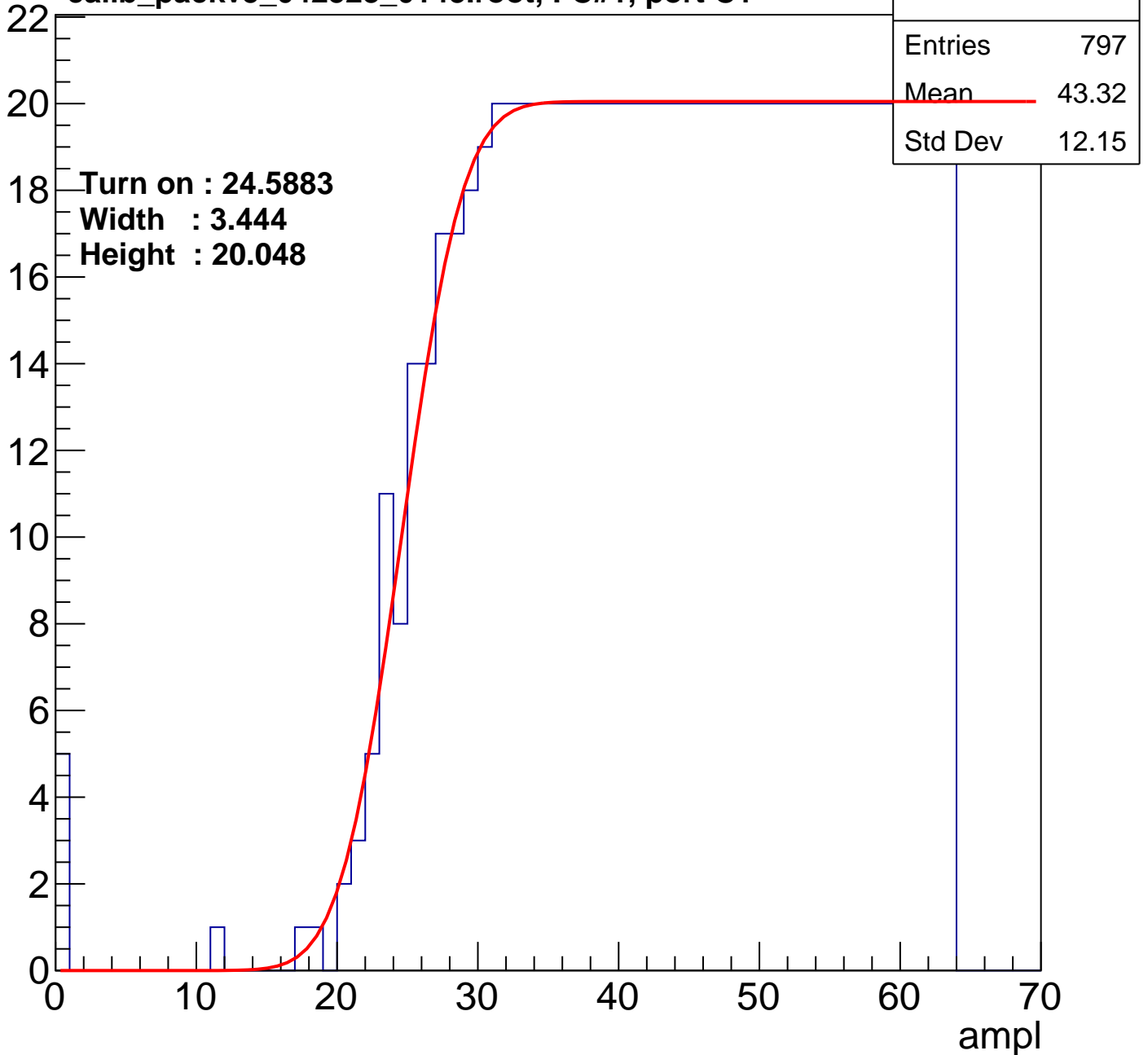
ampl



# B0L101S, U15-ch123

calib\_packv5\_042523\_0143.root, FC#1, port C1

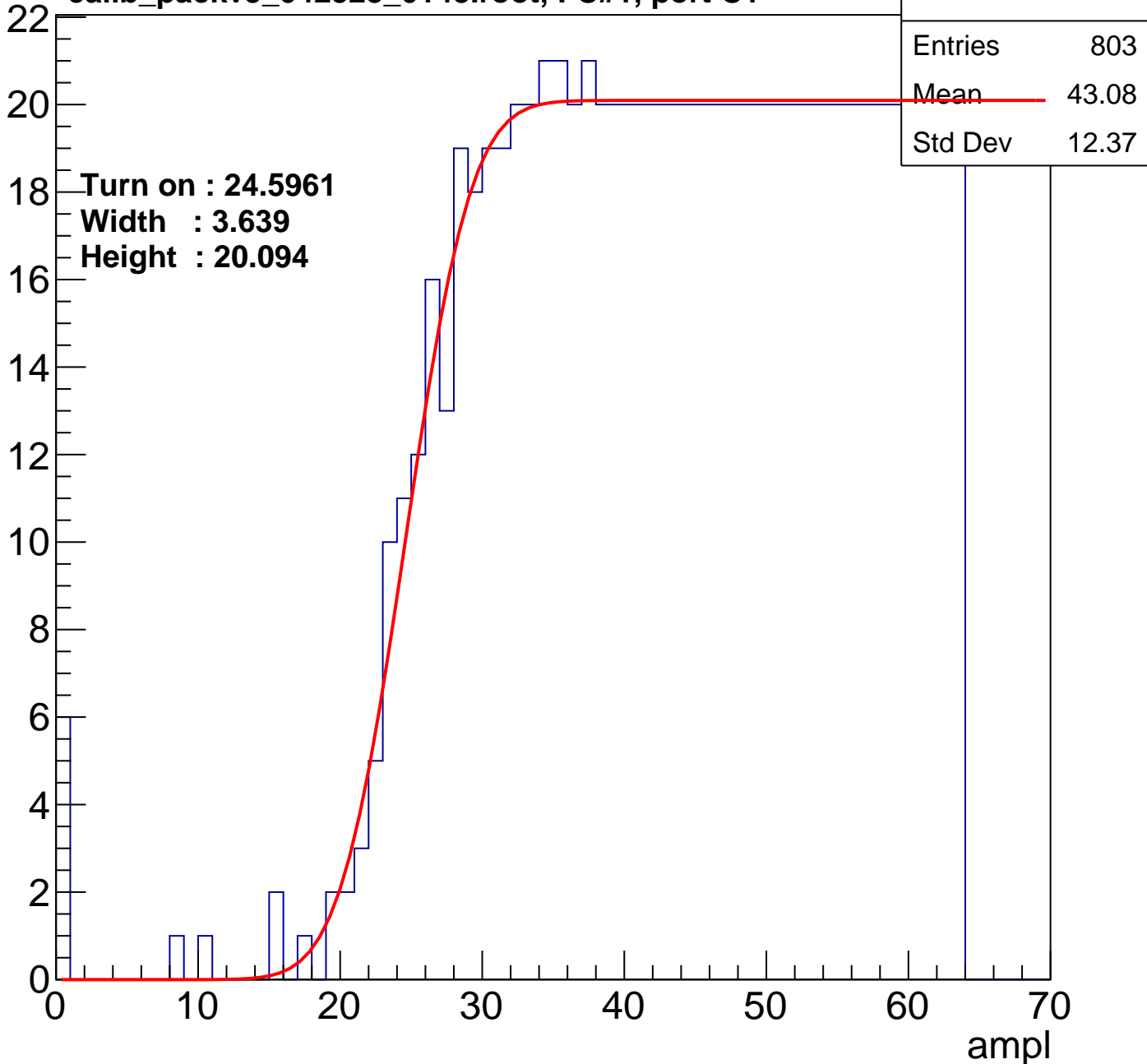
Entry



# B0L101S, U15-ch124

calib\_packv5\_042523\_0143.root, FC#1, port C1

Entry



# B0L101S, U15-ch125

calib\_packv5\_042523\_0143.root, FC#1, port C1

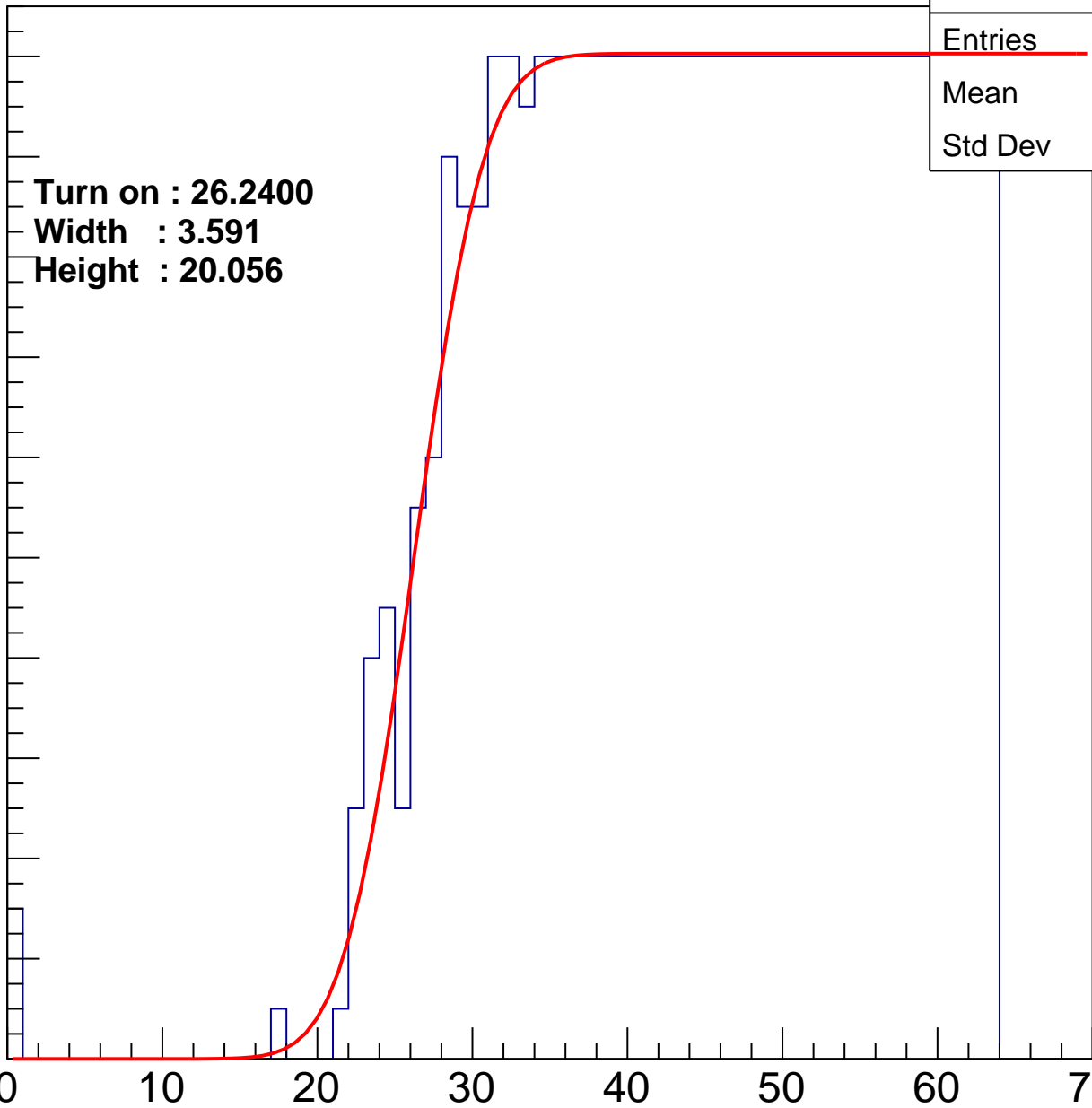
Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 26.2400**  
**Width : 3.591**  
**Height : 20.056**

Entries	766
Mean	44.1
Std Dev	11.59

ampl



# B0L101S, U15-ch126

calib\_packv5\_042523\_0143.root, FC#1, port C1

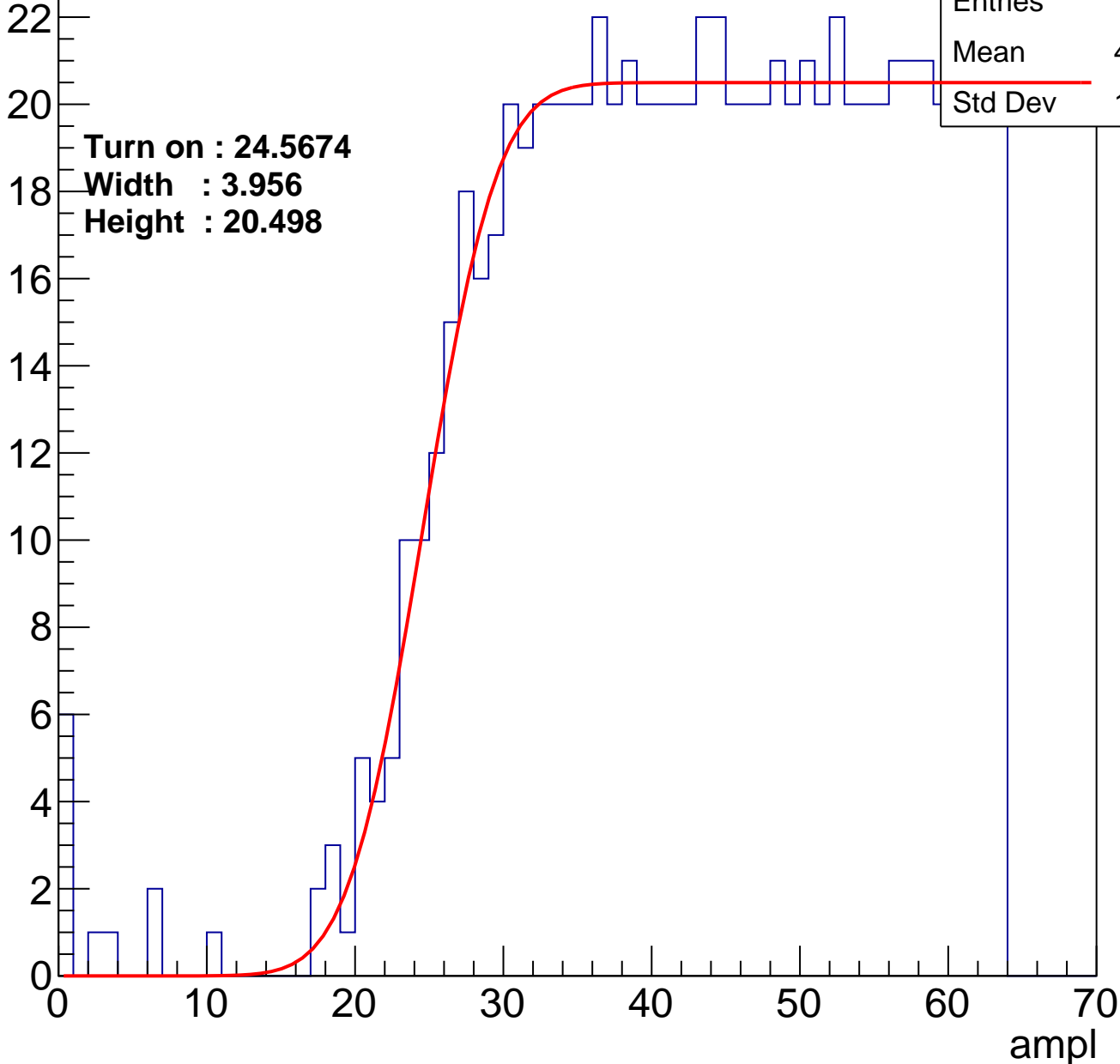
Entries	824
Mean	42.94
Std Dev	12.63

**Turn on : 24.5674**

**Width : 3.956**

**Height : 20.498**

Entry

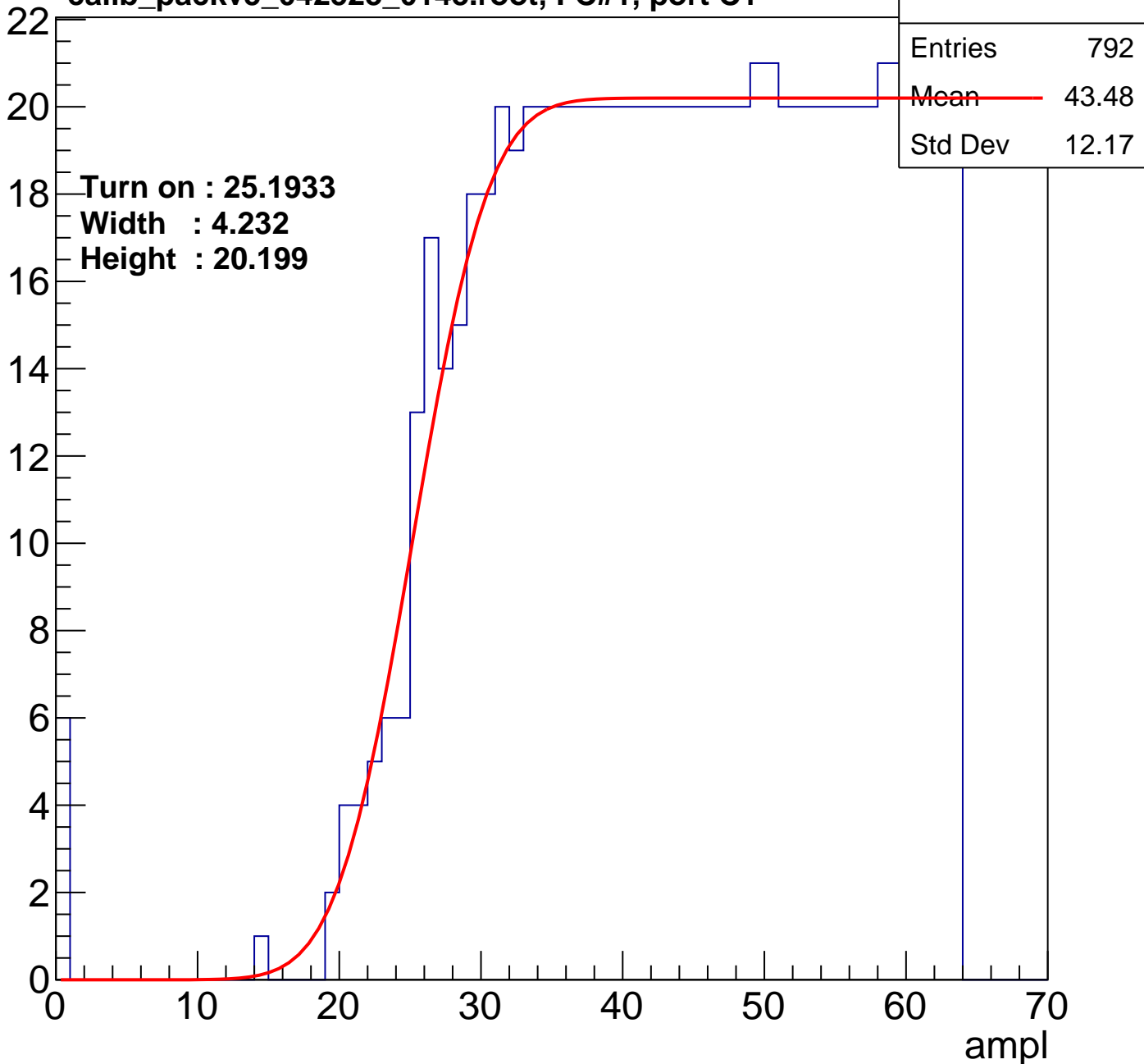




# B0L101S, U15-ch127

calib\_packv5\_042523\_0143.root, FC#1, port C1

Entry



# B0L101S, U15-ch127

calib\_packv5\_042523\_0143.root, FC#1, port C1

Entry

