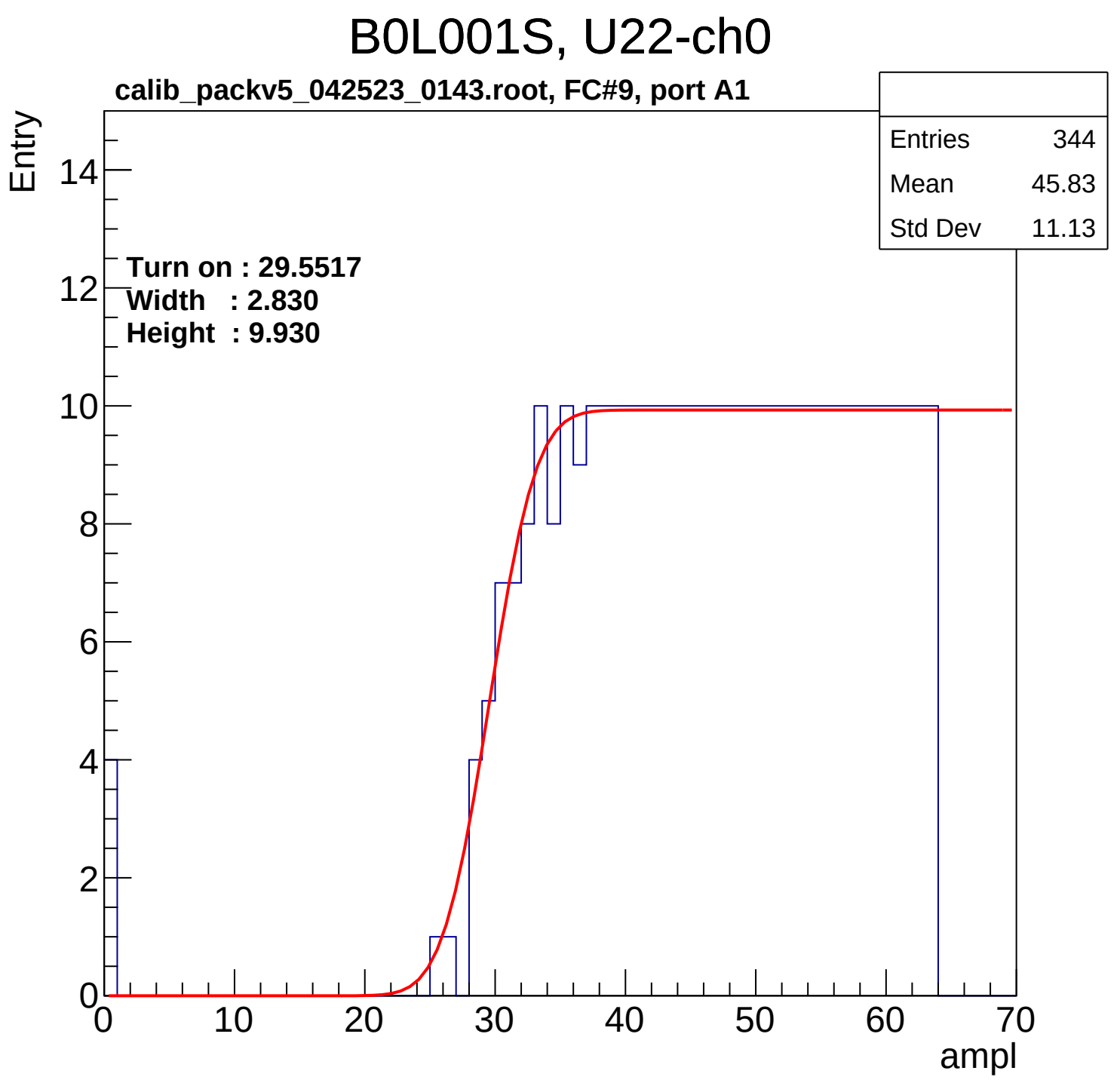
B0L001S, U22-ch0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 344
Mean 45.83
Std Dev 11.13
Turn on : 29.5517
Width : 2.830
Height : 9.930
Entry
ampl
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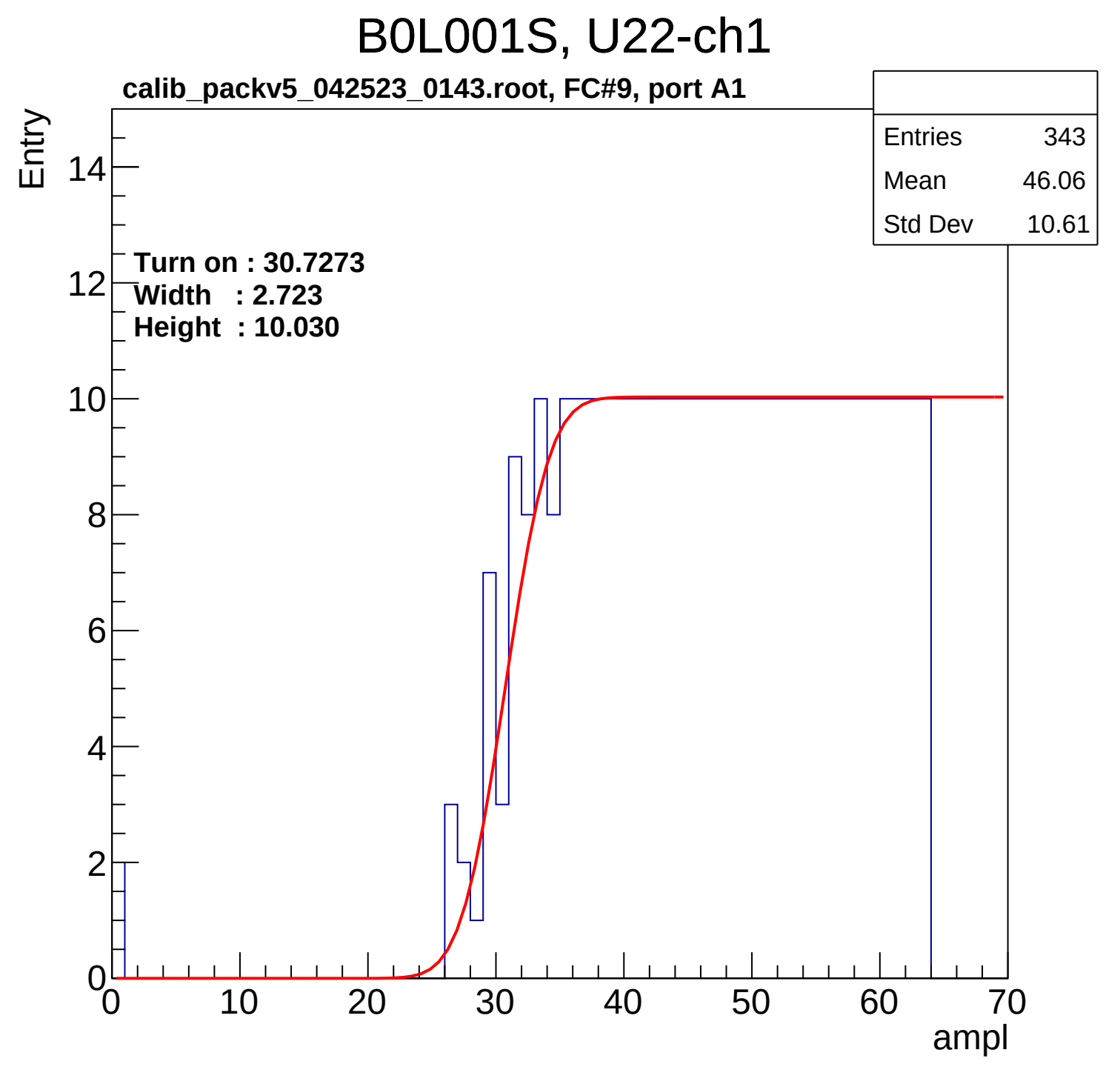
B0L001S, U22-ch1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 343
Mean 46.06
Std Dev 10.61
Turn on : 30.7273
Width : 2.723
Height : 10.030
Entry
ampl
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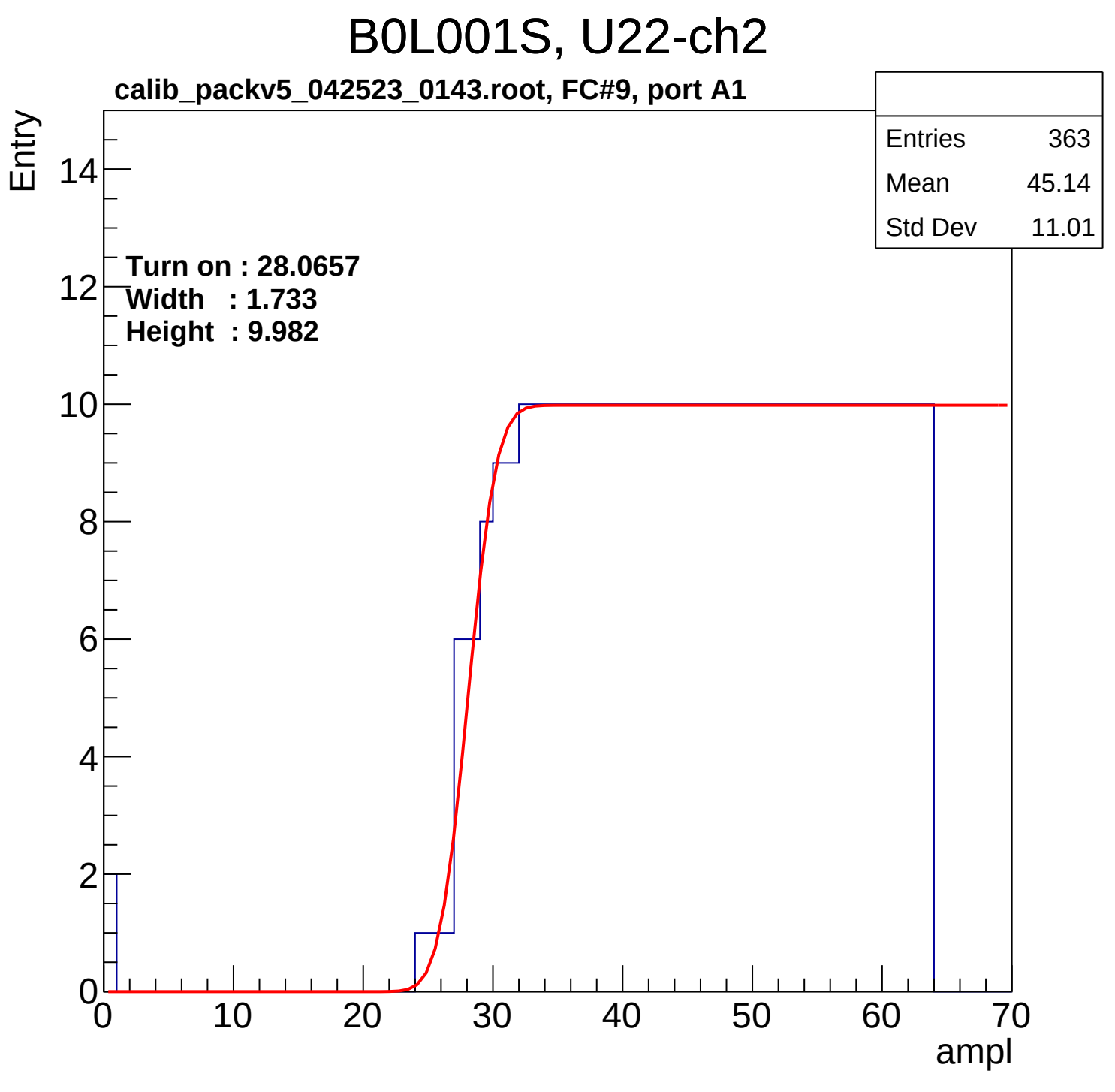
B0L001S, U22-ch2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.14
Std Dev 11.01
Turn on : 28.0657
Width : 1.733
Height : 9.982
Entry
ampl
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2
4
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0
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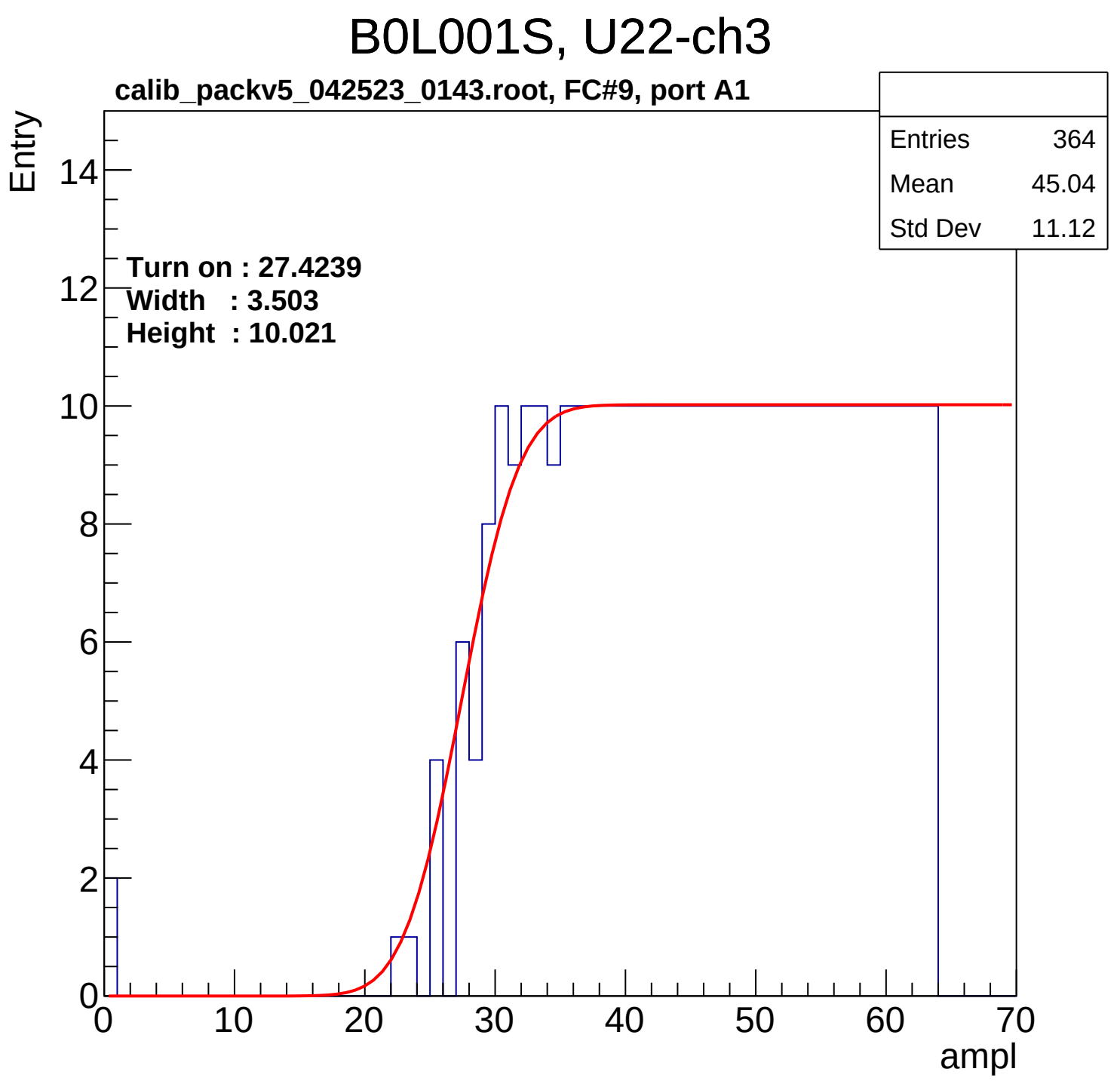
B0L001S, U22-ch3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 45.04
Std Dev 11.12
Turn on : 27.4239
Width : 3.503
Height : 10.021
Entry
ampl
0
2
4
6
8
10
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0
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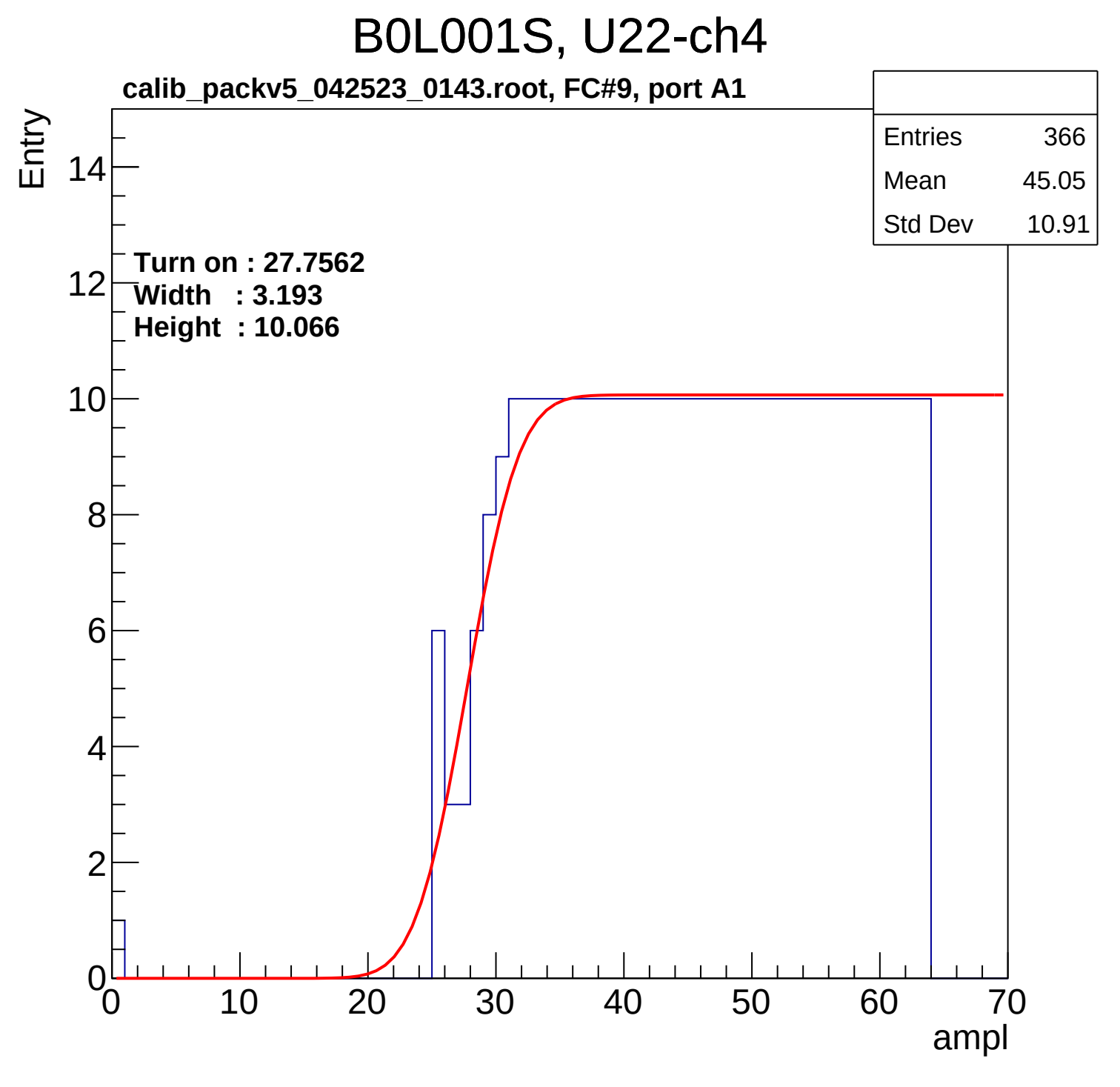
B0L001S, U22-ch4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 45.05
Std Dev 10.91
Turn on : 27.7562
Width : 3.193
Height : 10.066
Entry
ampl
0
2
4
6
8
10
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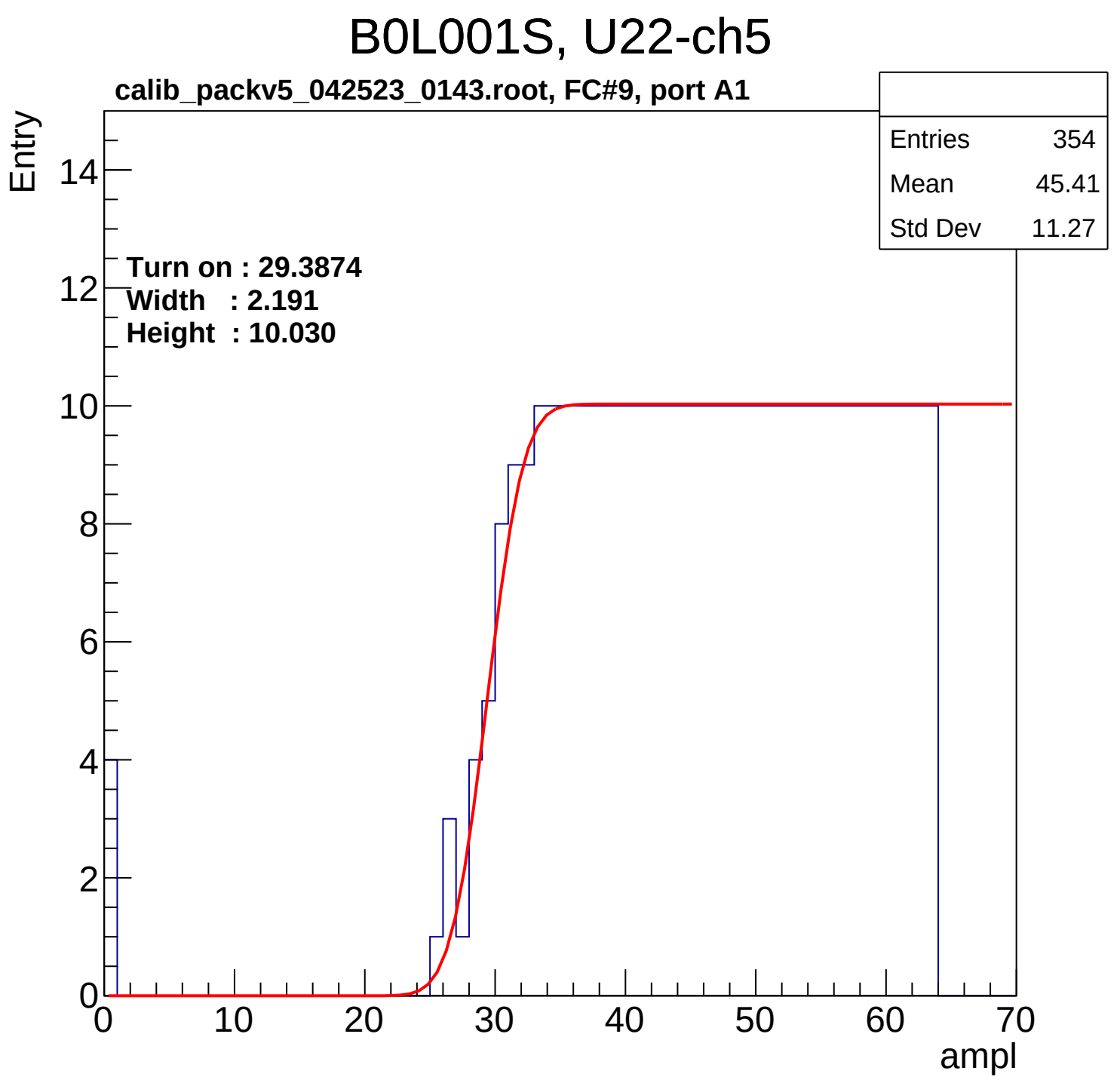
B0L001S, U22-ch5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.41
Std Dev 11.27
Turn on : 29.3874
Width : 2.191
Height : 10.030
Entry
ampl
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2
4
6
8
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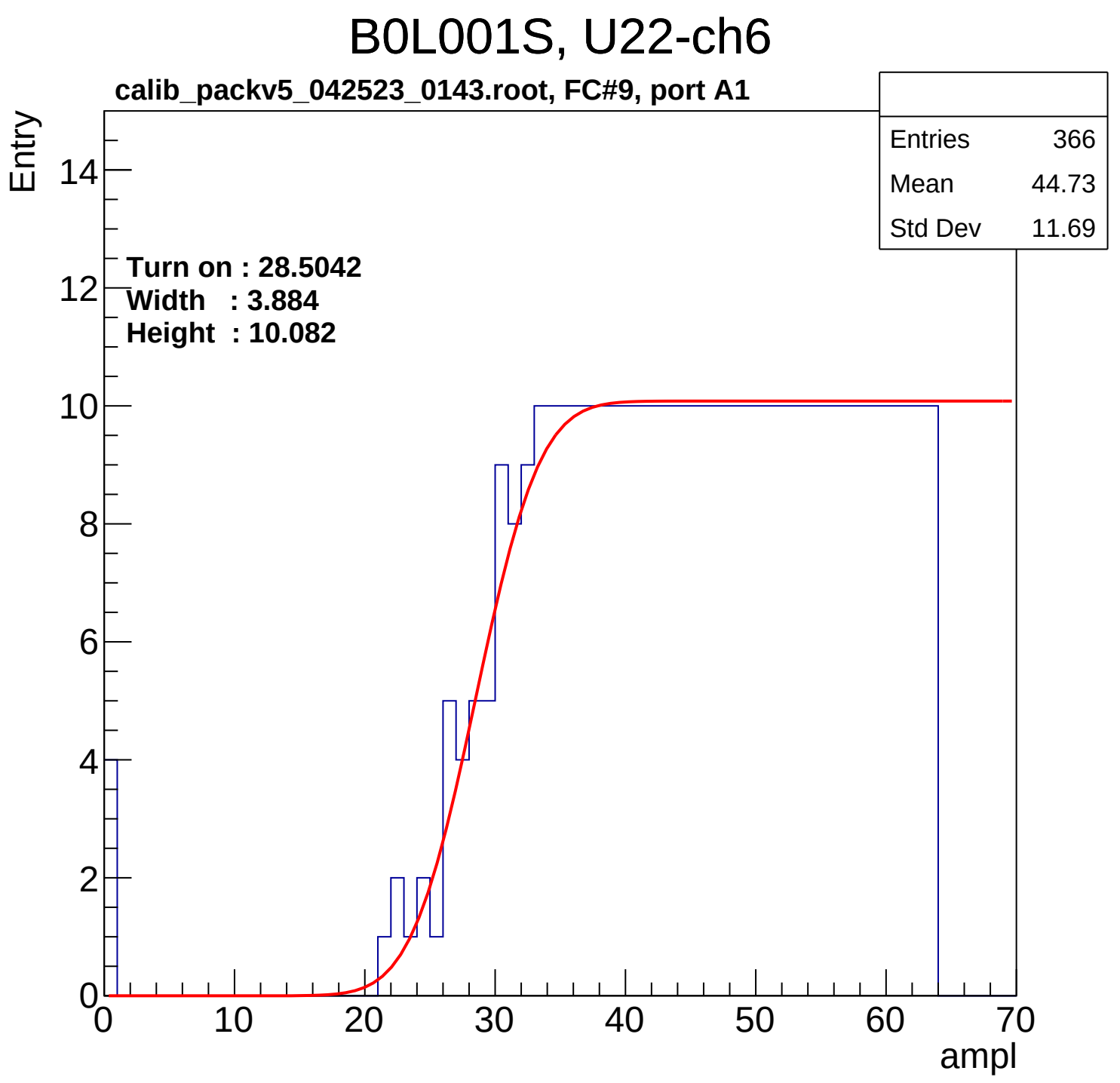
B0L001S, U22-ch6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.73
Std Dev 11.69
Turn on : 28.5042
Width : 3.884
Height : 10.082
Entry
ampl
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2
4
6
8
10
12
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0
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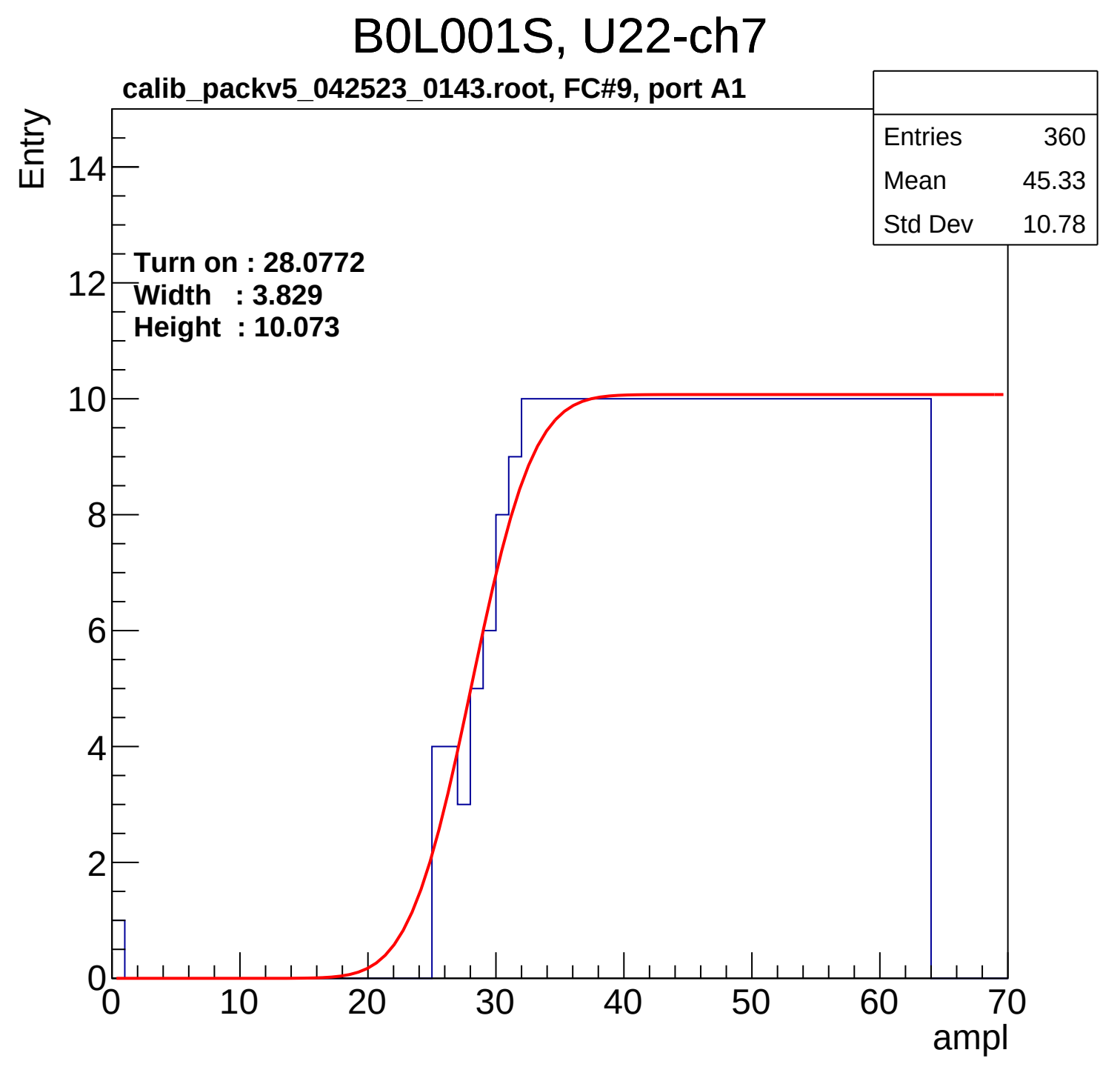
B0L001S, U22-ch7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.33
Std Dev 10.78
Turn on : 28.0772
Width : 3.829
Height : 10.073
Entry
ampl
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2
4
6
8
10
12
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0
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60
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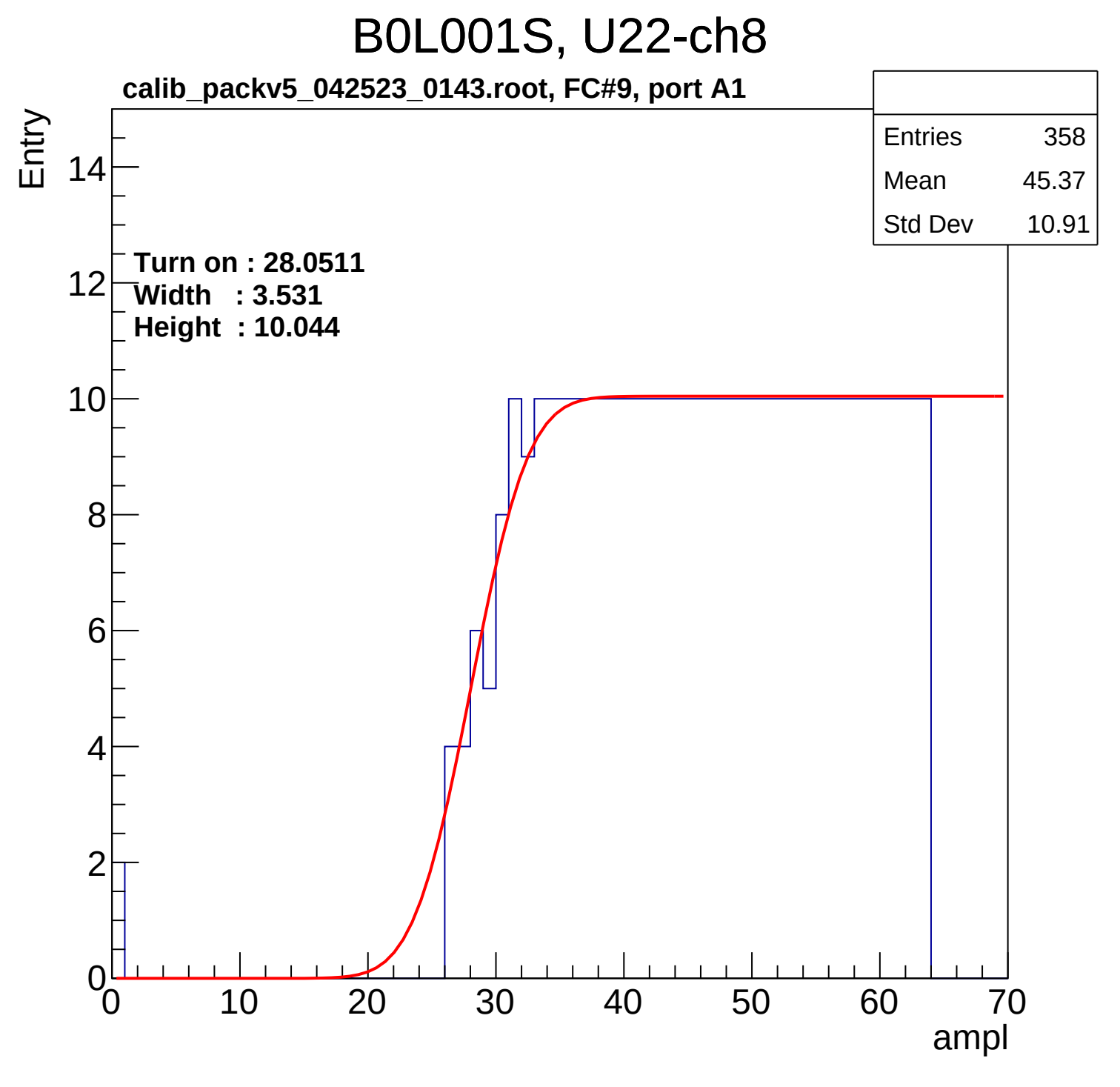
B0L001S, U22-ch8
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.37
Std Dev 10.91
Turn on : 28.0511
Width : 3.531
Height : 10.044
Entry
ampl
0
2
4
6
8
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0
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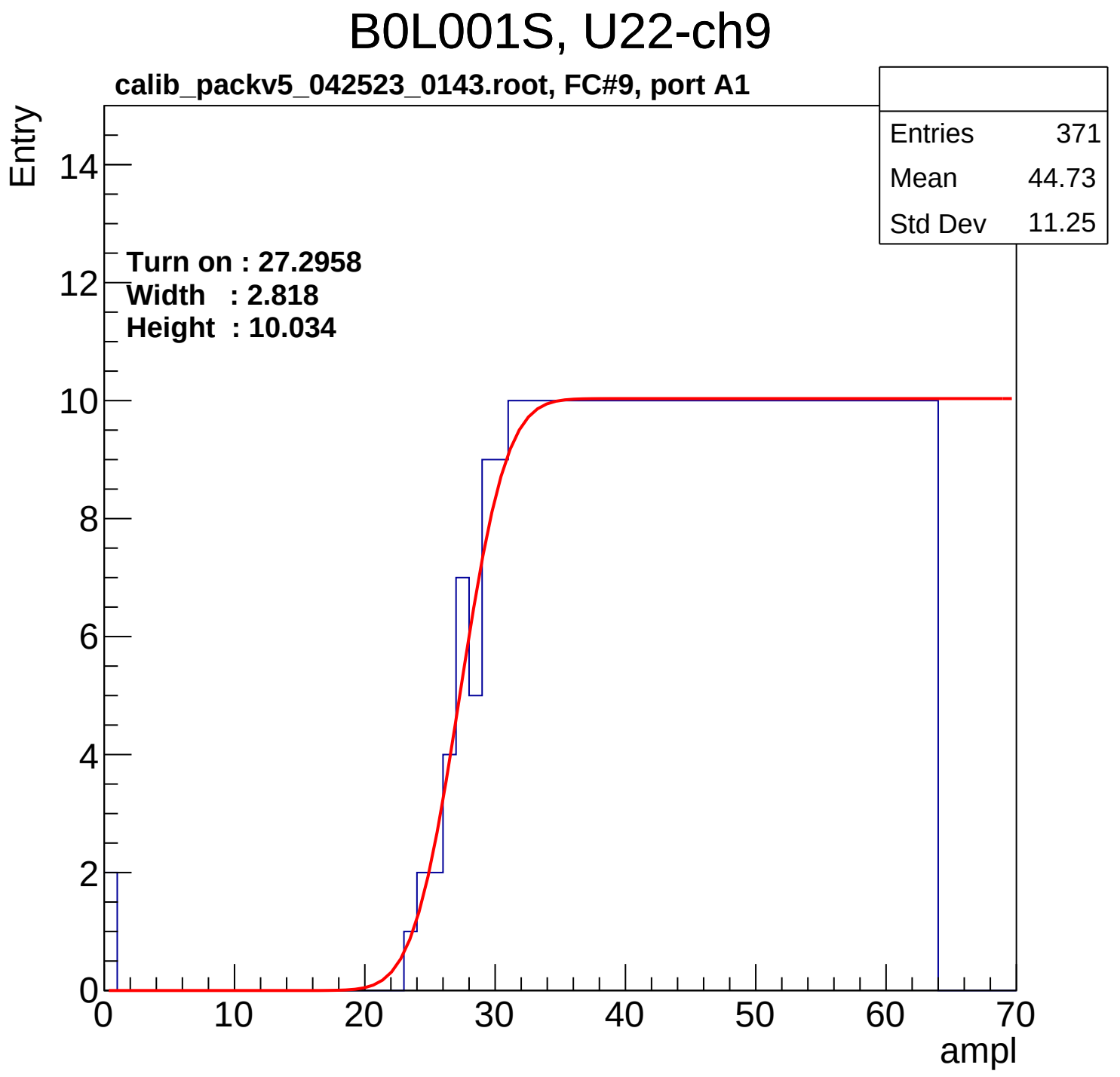
B0L001S, U22-ch9
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.73
Std Dev 11.25
Turn on : 27.2958
Width : 2.818
Height : 10.034
Entry
ampl
0
2
4
6
8
10
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0
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60
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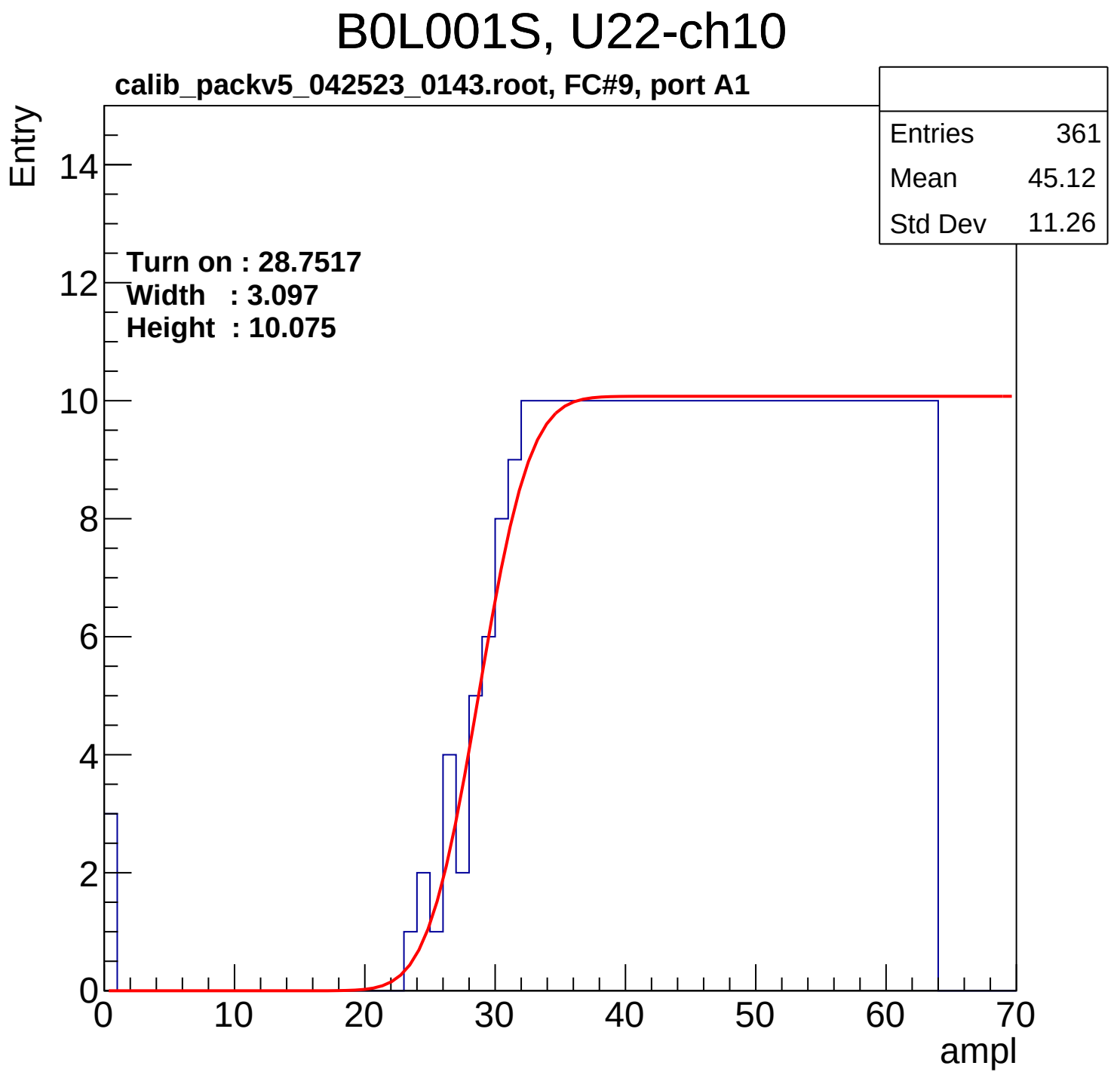
B0L001S, U22-ch10
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.12
Std Dev 11.26
Turn on : 28.7517
Width : 3.097
Height : 10.075
Entry
ampl
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6
8
10
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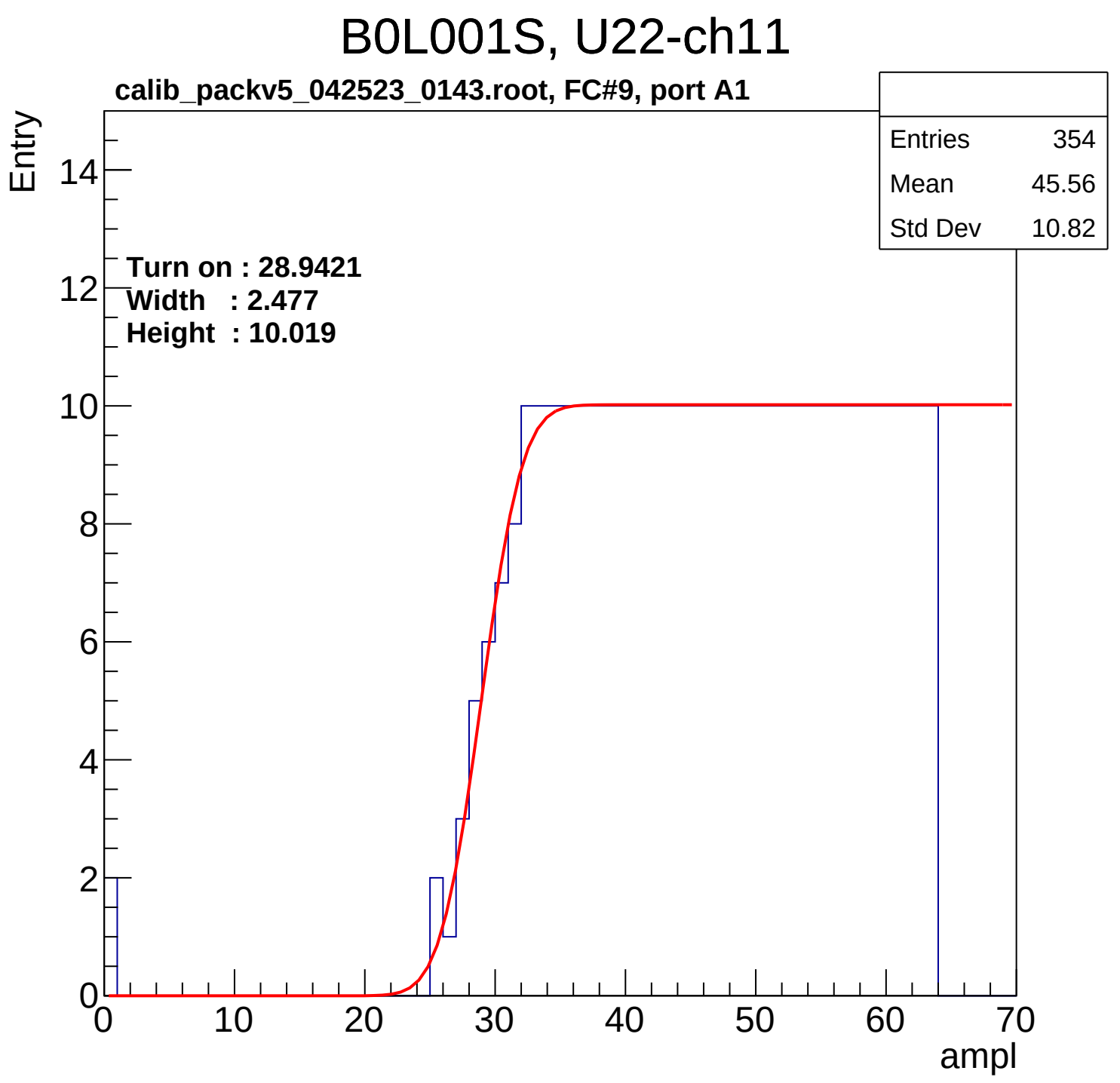
B0L001S, U22-ch11
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.56
Std Dev 10.82
Turn on : 28.9421
Width : 2.477
Height : 10.019
Entry
ampl
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4
6
8
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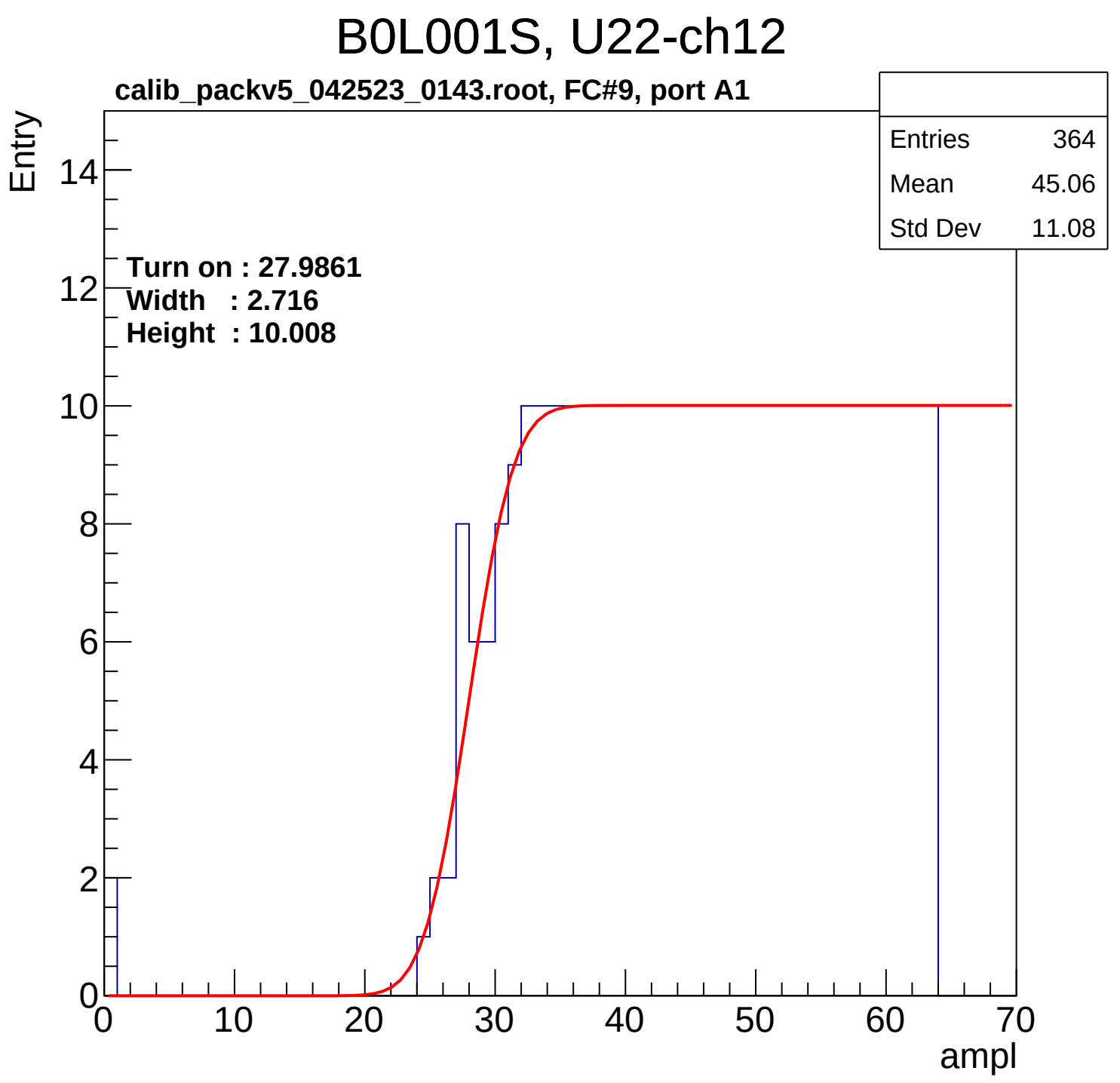
B0L001S, U22-ch12
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 45.06
Std Dev 11.08
Turn on : 27.9861
Width : 2.716
Height : 10.008
Entry
ampl
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6
8
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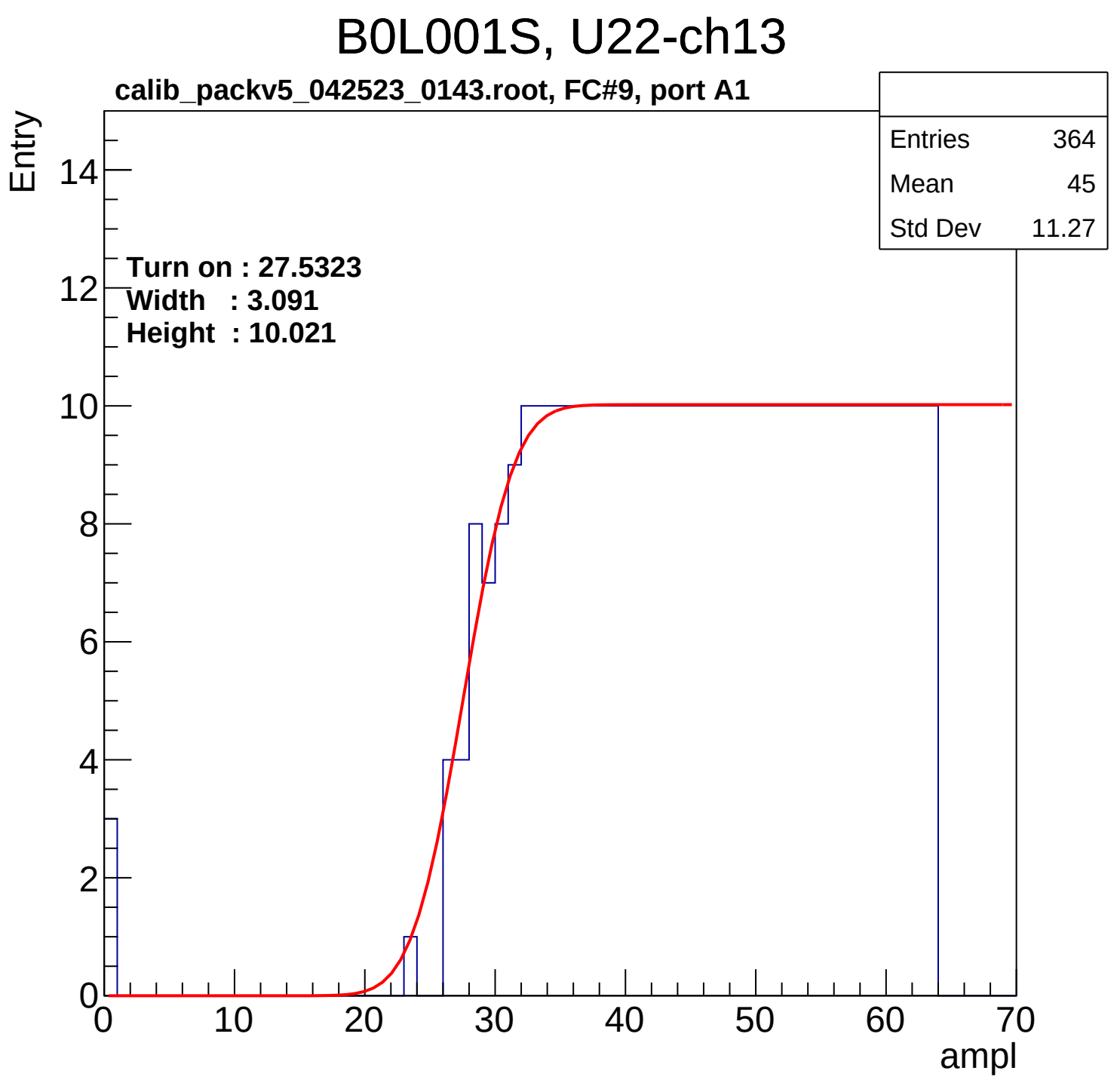
B0L001S, U22-ch13
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 45
Std Dev 11.27
Turn on : 27.5323
Width : 3.091
Height : 10.021
Entry
ampl
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4
6
8
10
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0
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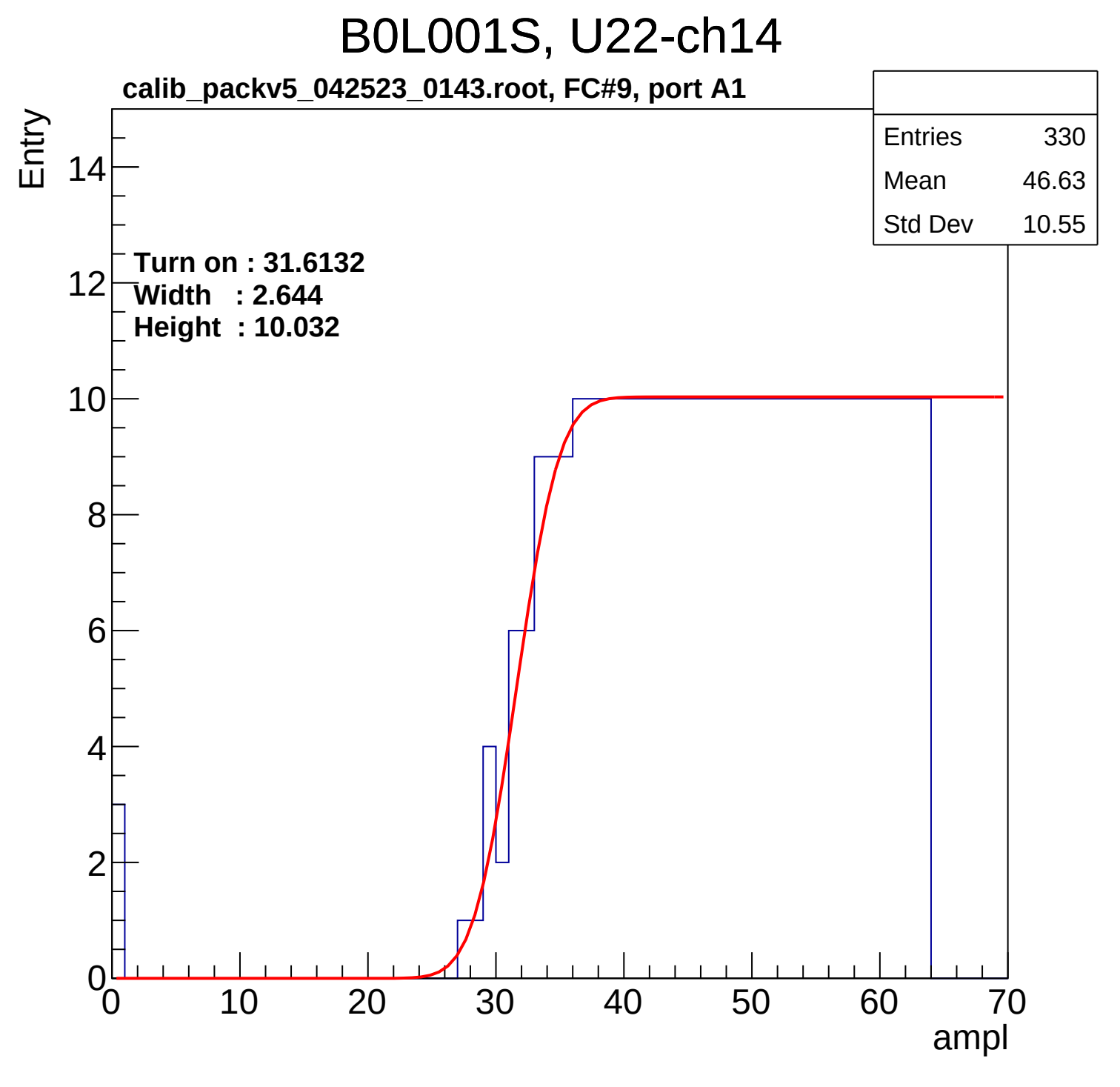
B0L001S, U22-ch14
calib_packv5_042523_0143.root, FC#9, port A1
Entries 330
Mean 46.63
Std Dev 10.55
Turn on : 31.6132
Width : 2.644
Height : 10.032
Entry
ampl
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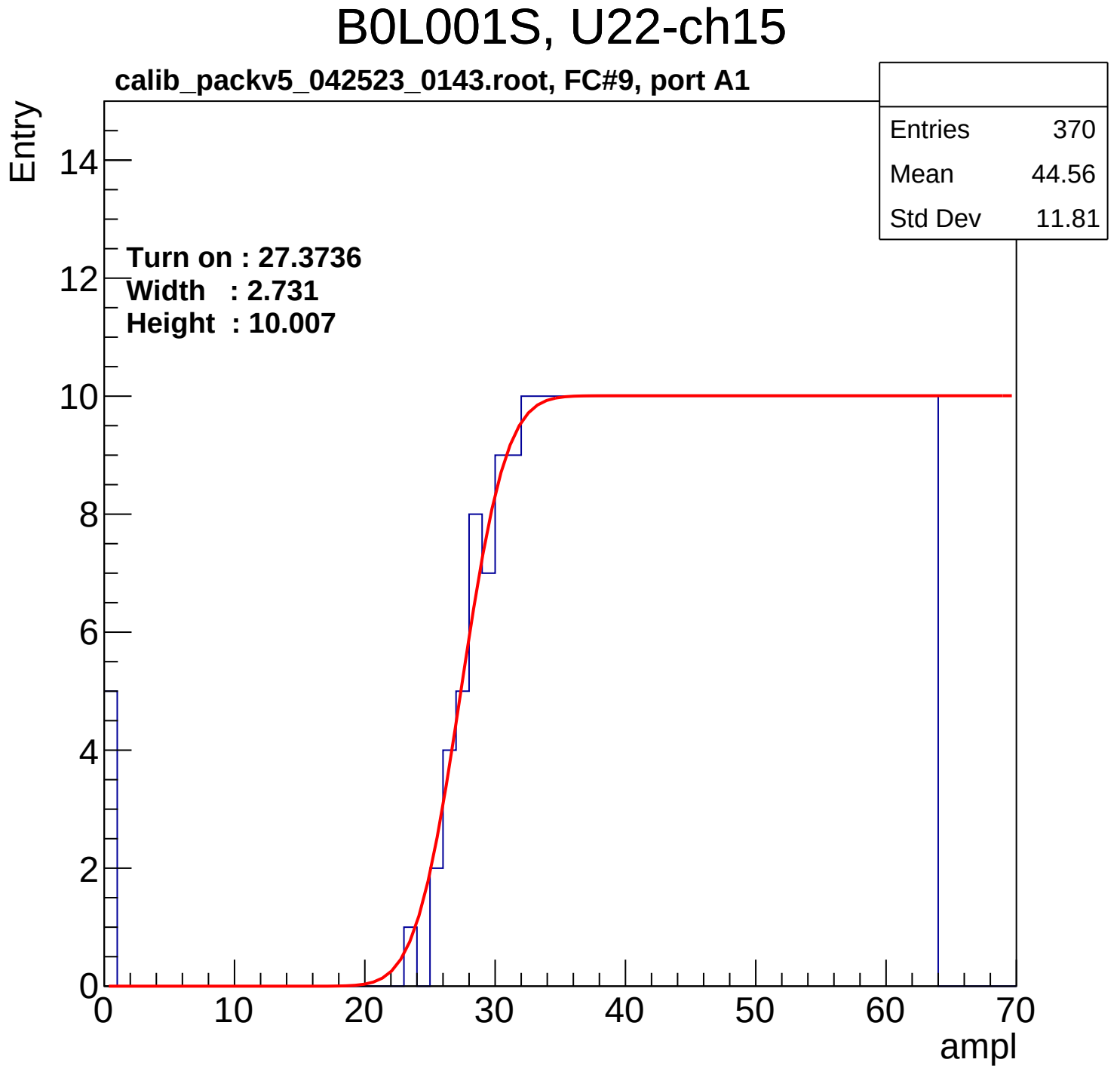
B0L001S, U22-ch15
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.56
Std Dev 11.81
Turn on : 27.3736
Width : 2.731
Height : 10.007
Entry
ampl
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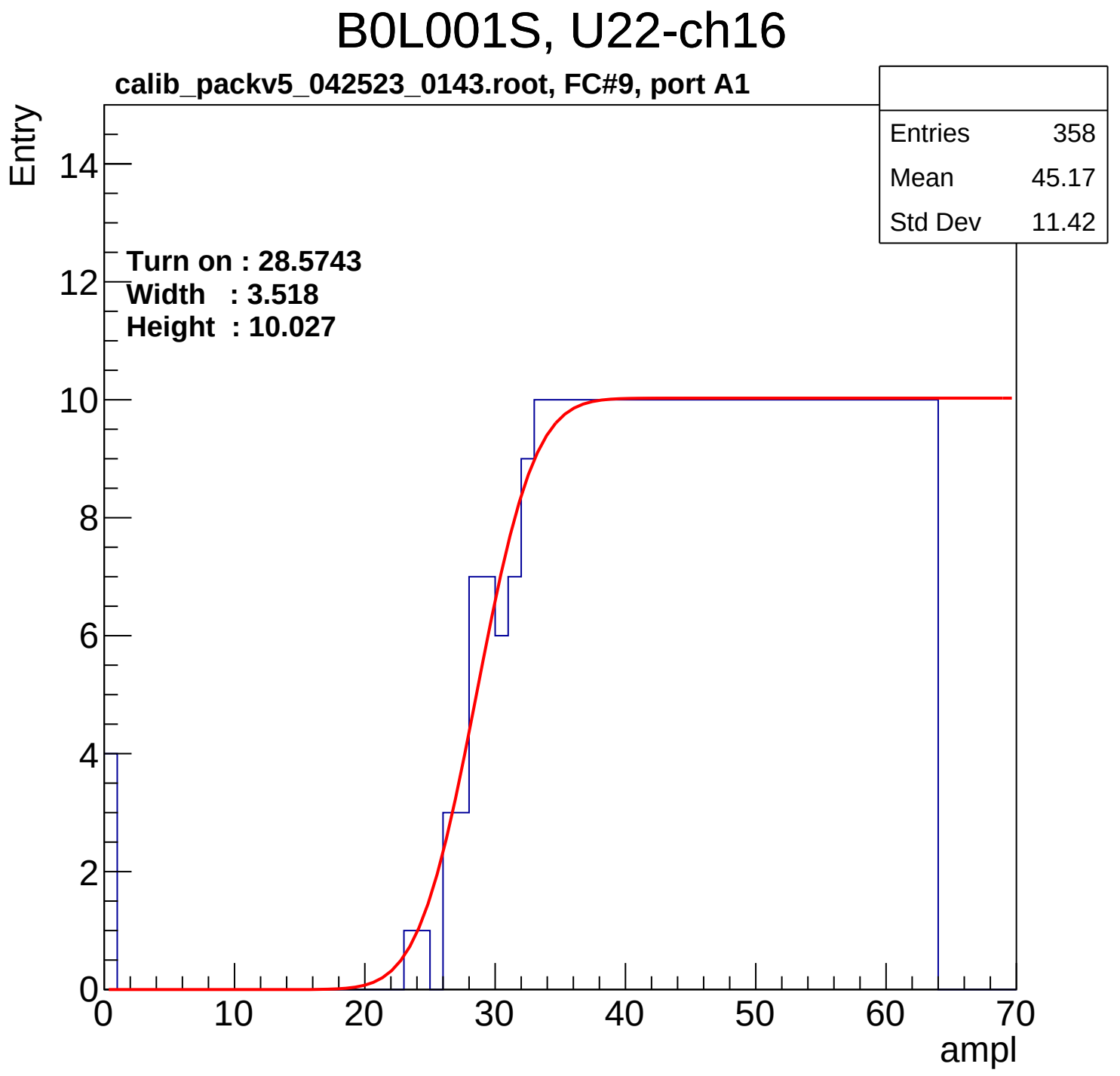
B0L001S, U22-ch16
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.17
Std Dev 11.42
Turn on : 28.5743
Width : 3.518
Height : 10.027
Entry
ampl
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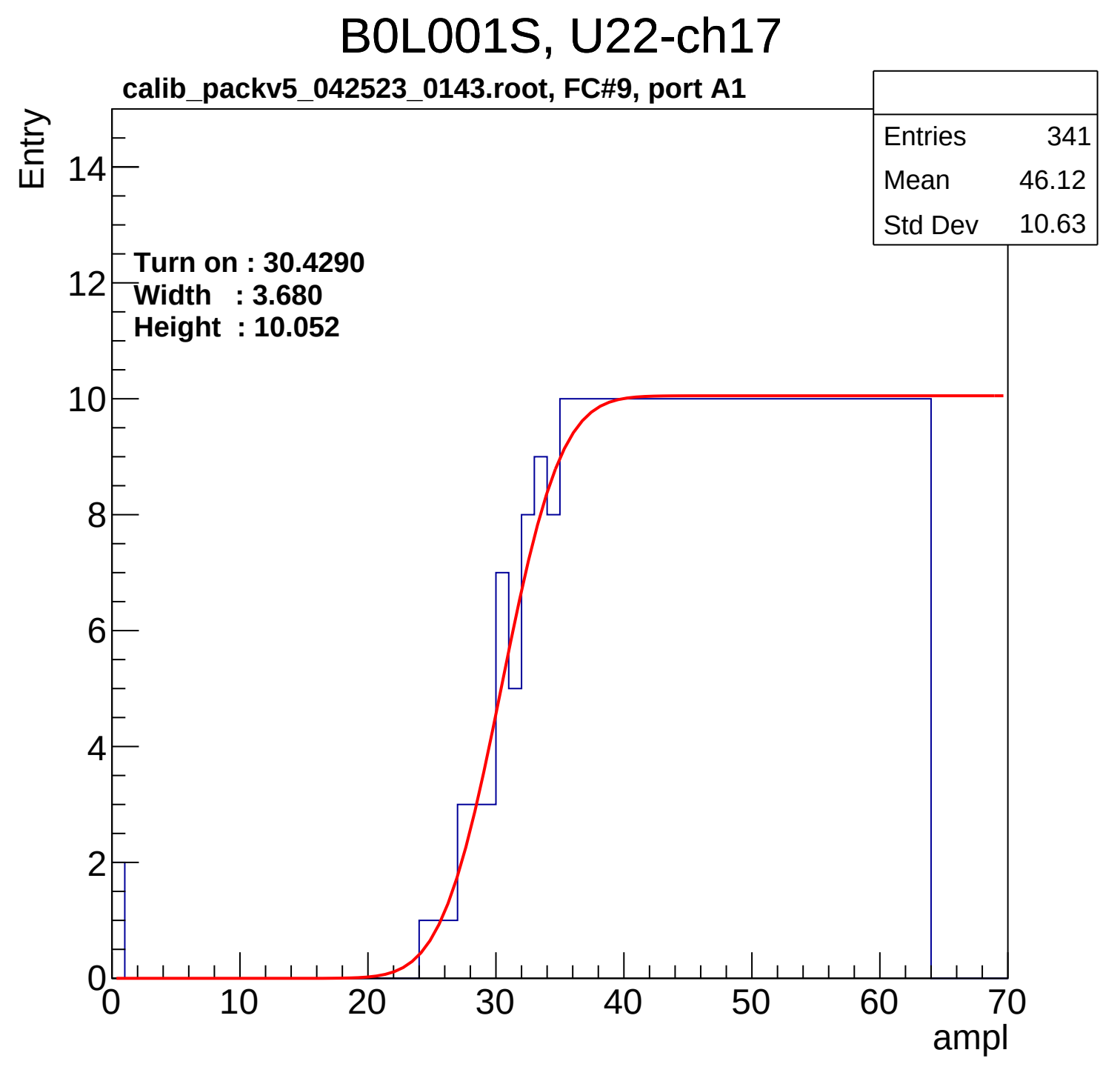
B0L001S, U22-ch17
calib_packv5_042523_0143.root, FC#9, port A1
Entries 341
Mean 46.12
Std Dev 10.63
Turn on : 30.4290
Width : 3.680
Height : 10.052
Entry
ampl
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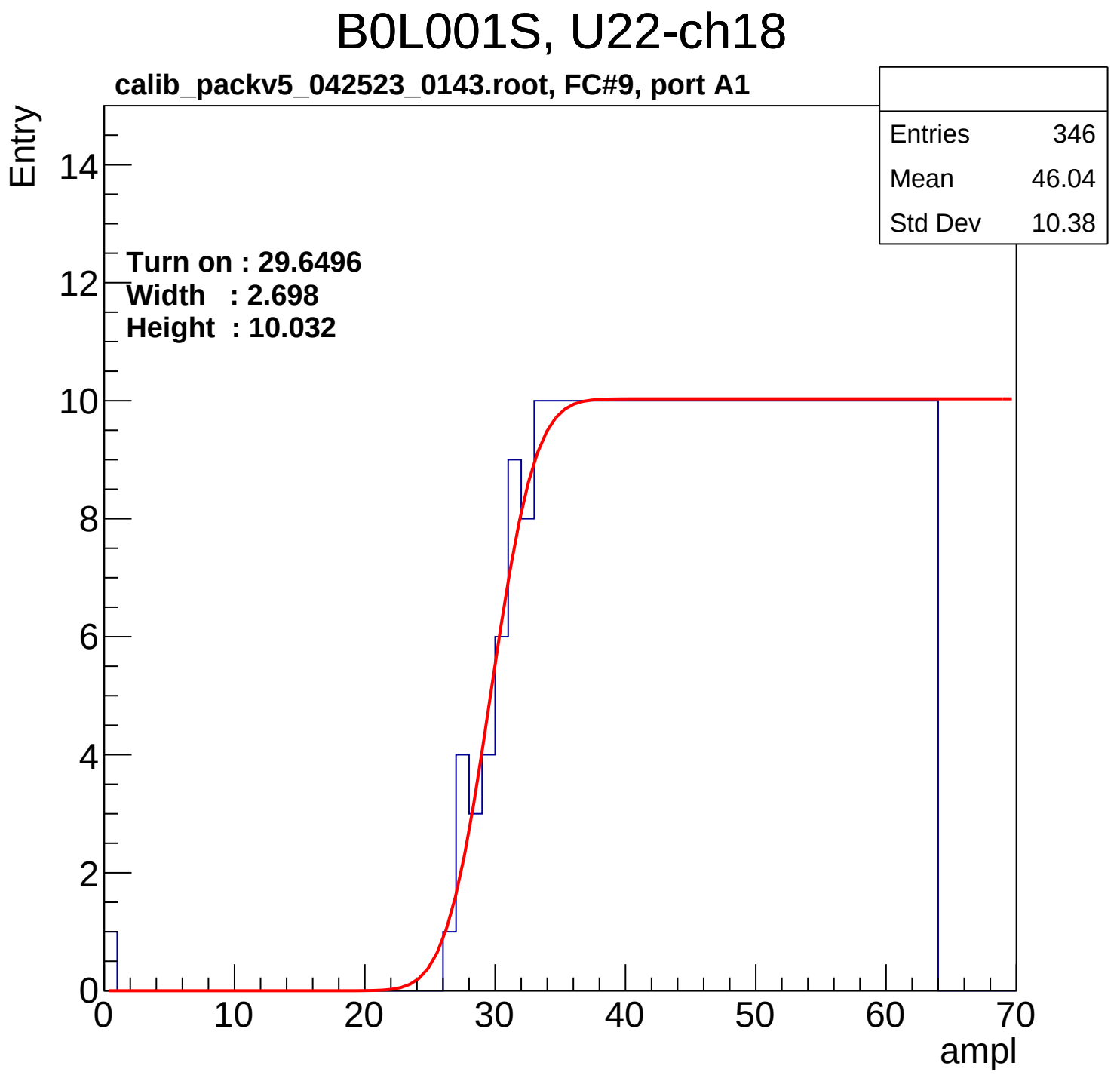
B0L001S, U22-ch18
calib_packv5_042523_0143.root, FC#9, port A1
Entries 346
Mean 46.04
Std Dev 10.38
Turn on : 29.6496
Width : 2.698
Height : 10.032
Entry
ampl
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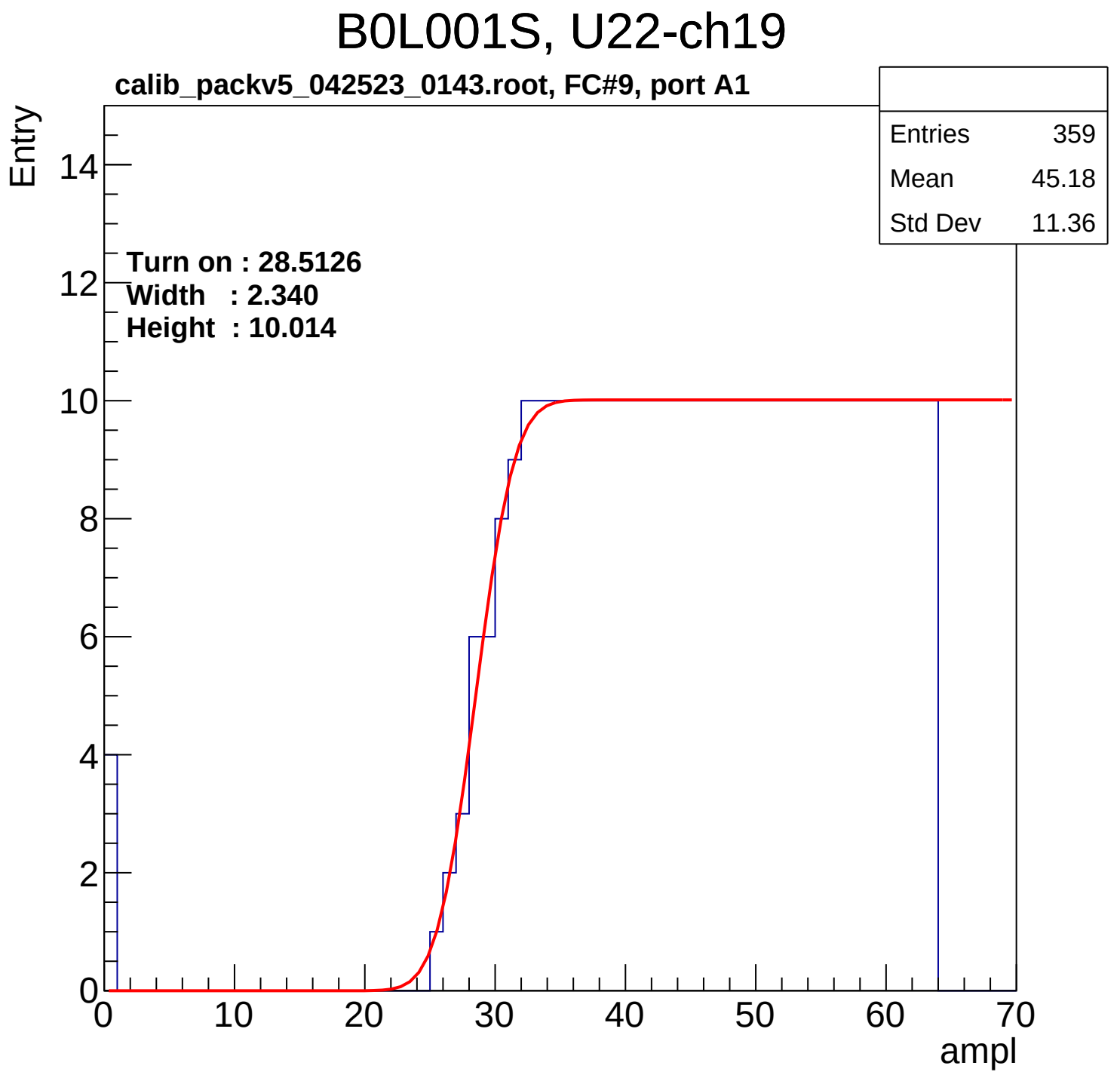
B0L001S, U22-ch19
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.18
Std Dev 11.36
Turn on : 28.5126
Width : 2.340
Height : 10.014
Entry
ampl
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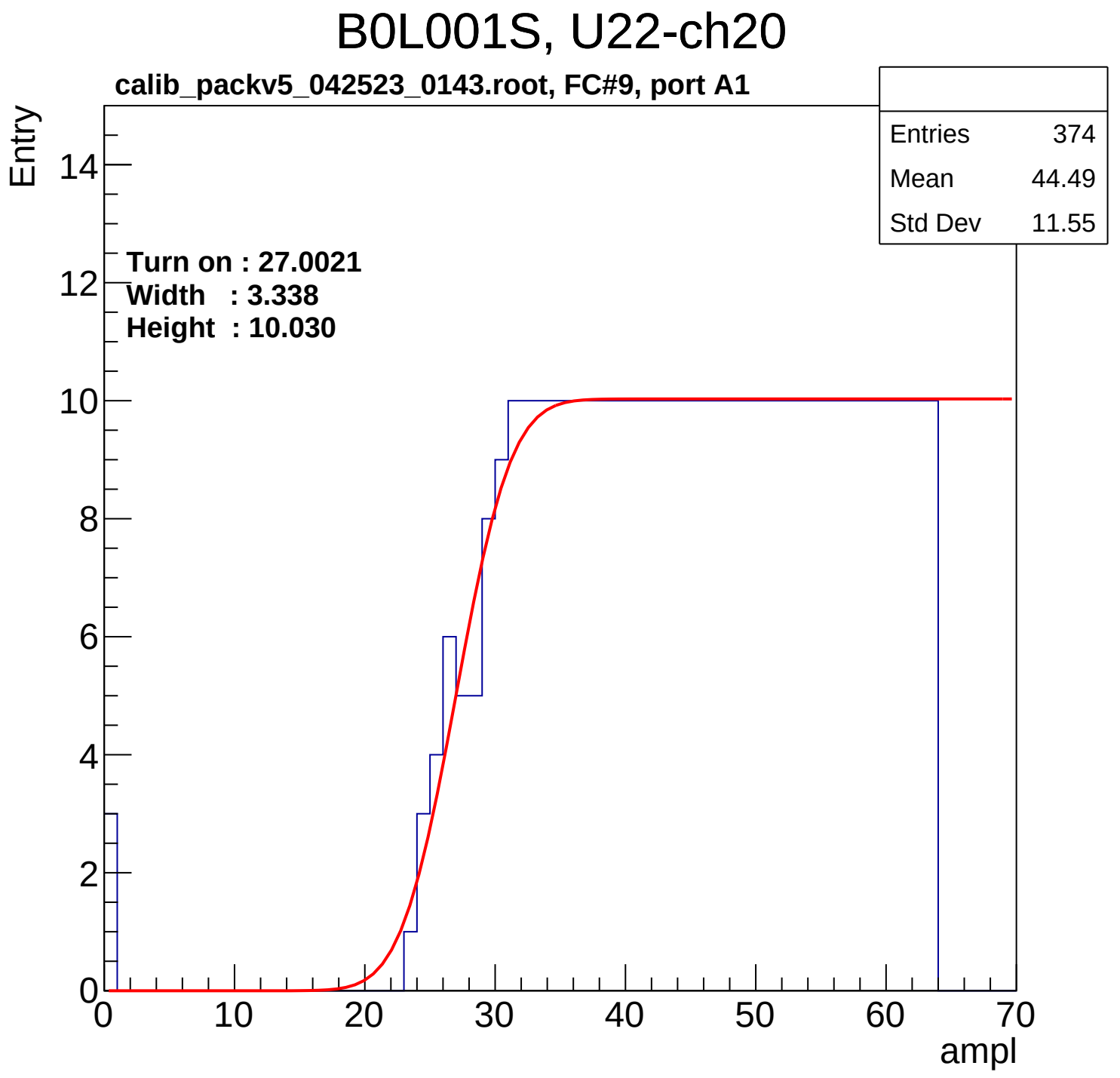
B0L001S, U22-ch20
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.49
Std Dev 11.55
Turn on : 27.0021
Width : 3.338
Height : 10.030
Entry
ampl
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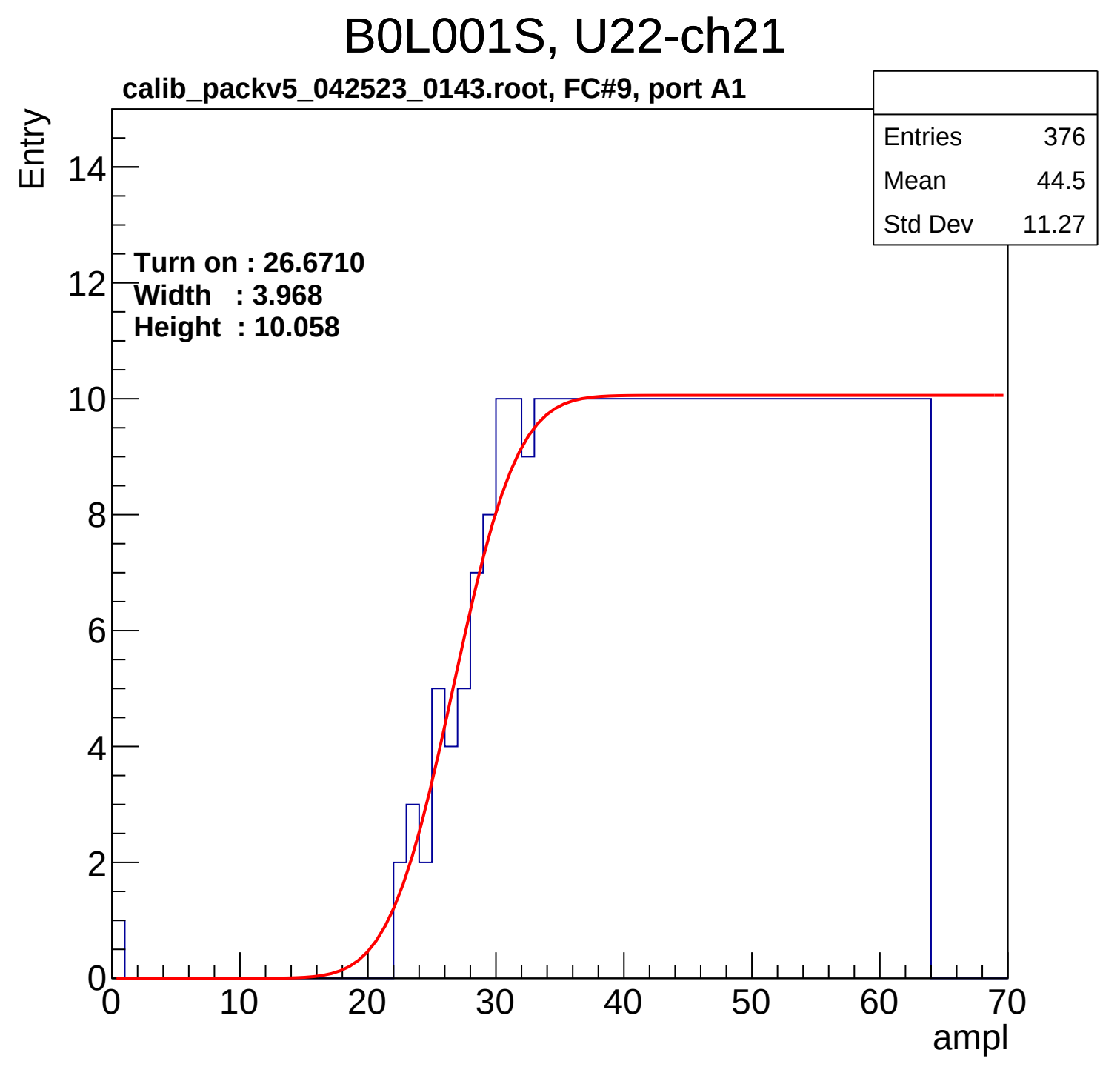
B0L001S, U22-ch21
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.5
Std Dev 11.27
Turn on : 26.6710
Width : 3.968
Height : 10.058
Entry
ampl
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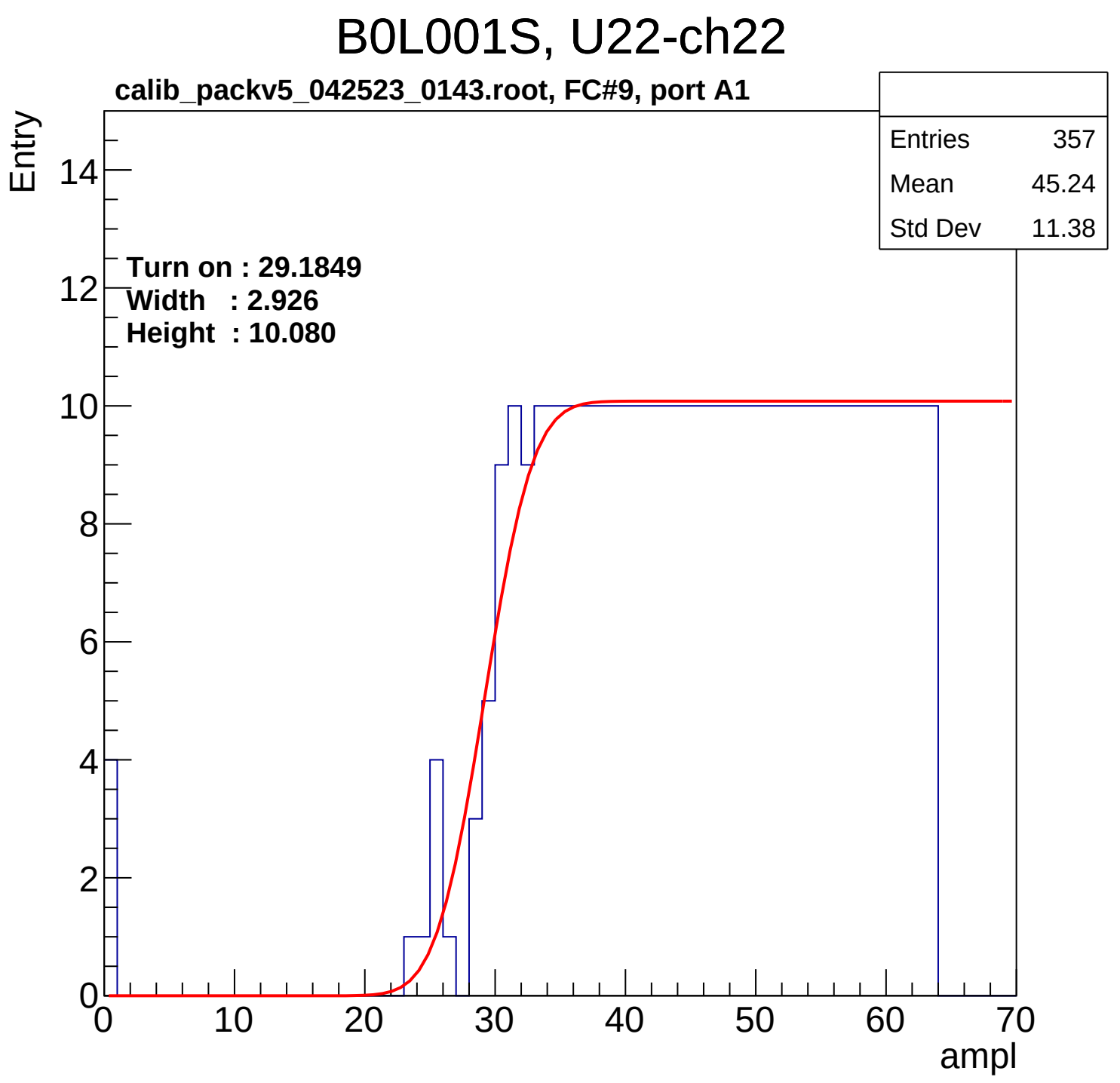
B0L001S, U22-ch22
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.24
Std Dev 11.38
Turn on : 29.1849
Width : 2.926
Height : 10.080
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ampl
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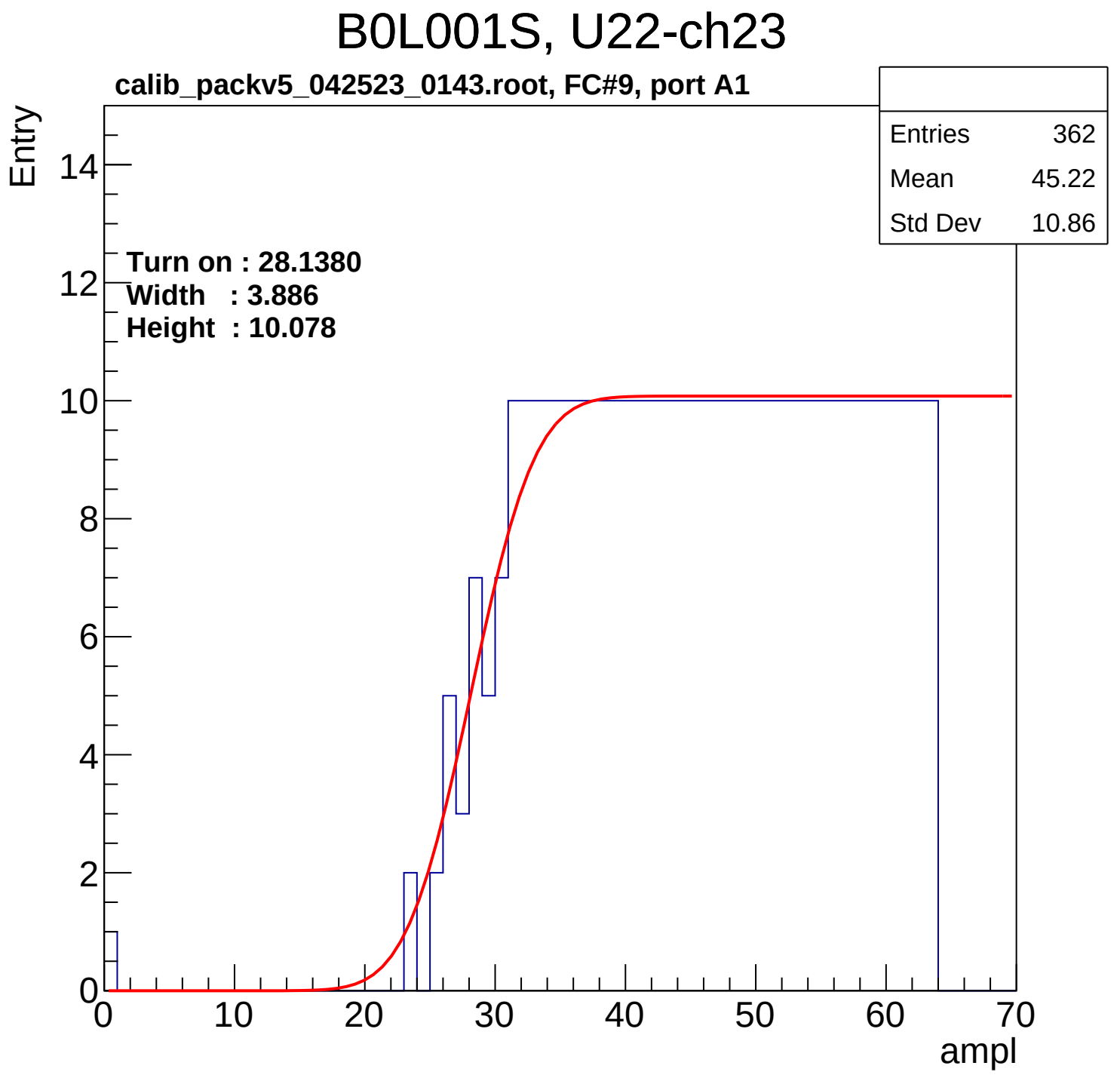
B0L001S, U22-ch23
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.22
Std Dev 10.86
Turn on : 28.1380
Width : 3.886
Height : 10.078
Entry
ampl
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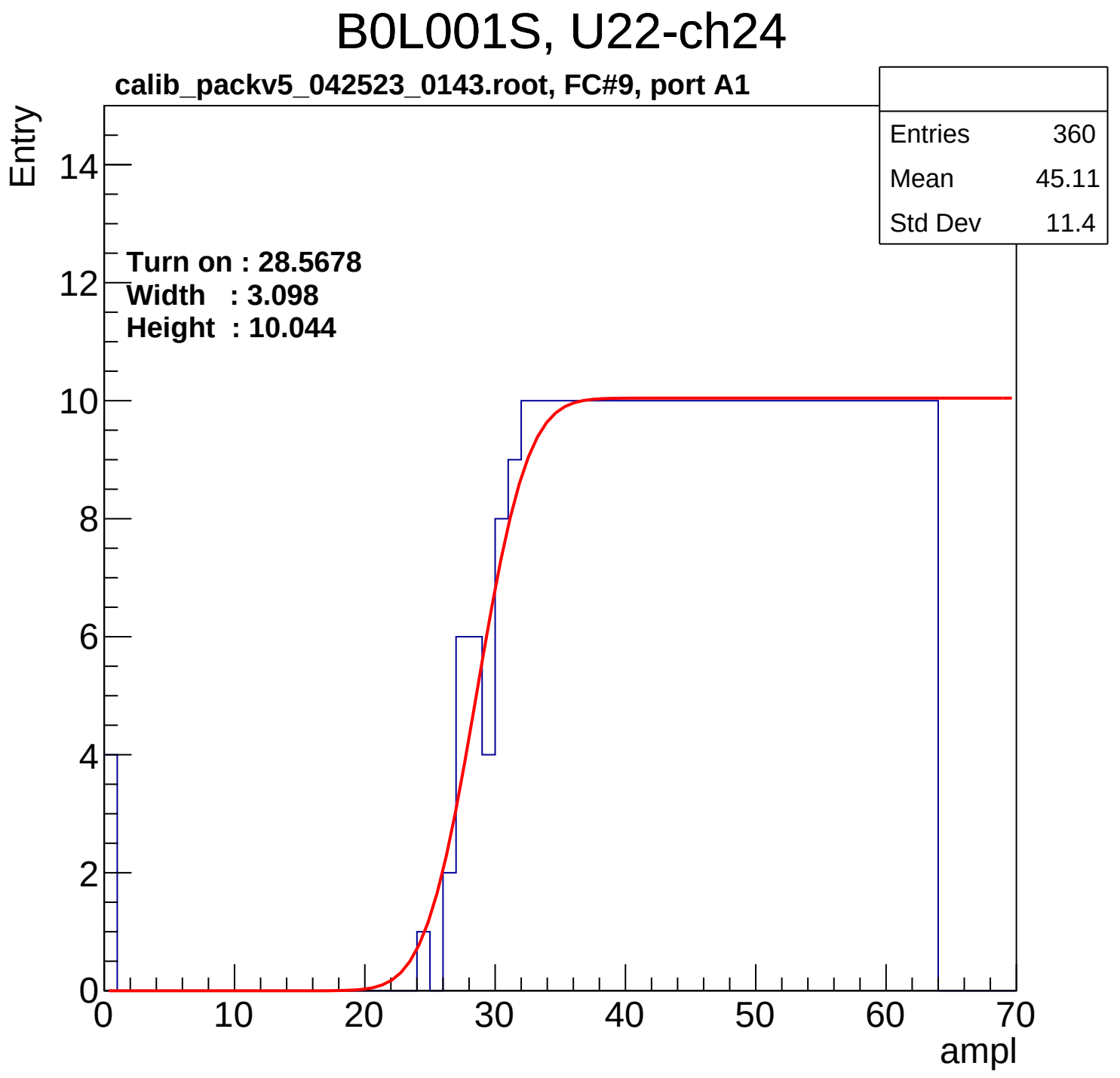
B0L001S, U22-ch24
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.11
Std Dev 11.4
Turn on : 28.5678
Width : 3.098
Height : 10.044
Entry
ampl
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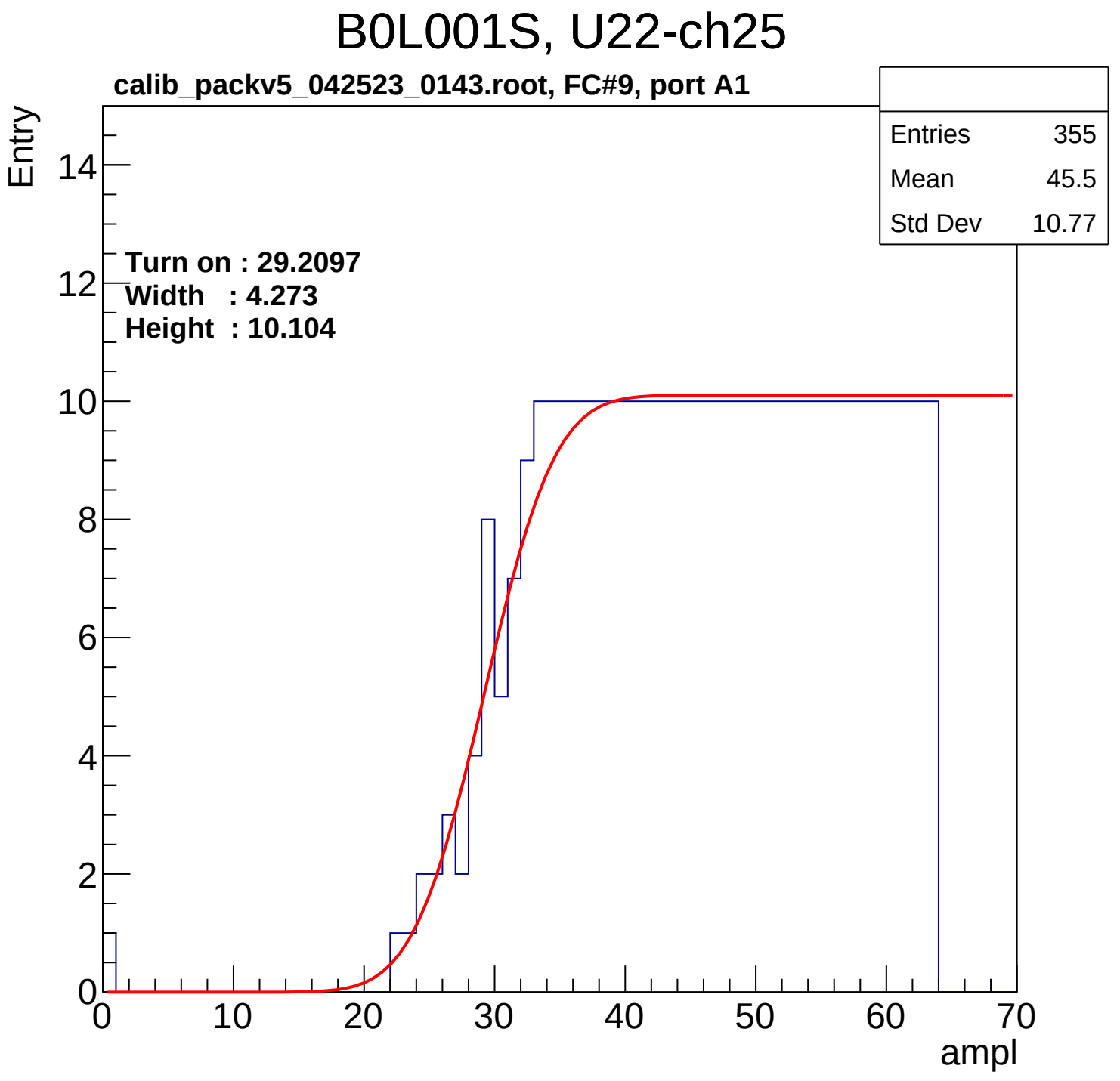
B0L001S, U22-ch25
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.5
Std Dev 10.77
Turn on : 29.2097
Width : 4.273
Height : 10.104
Entry
ampl
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6
8
10
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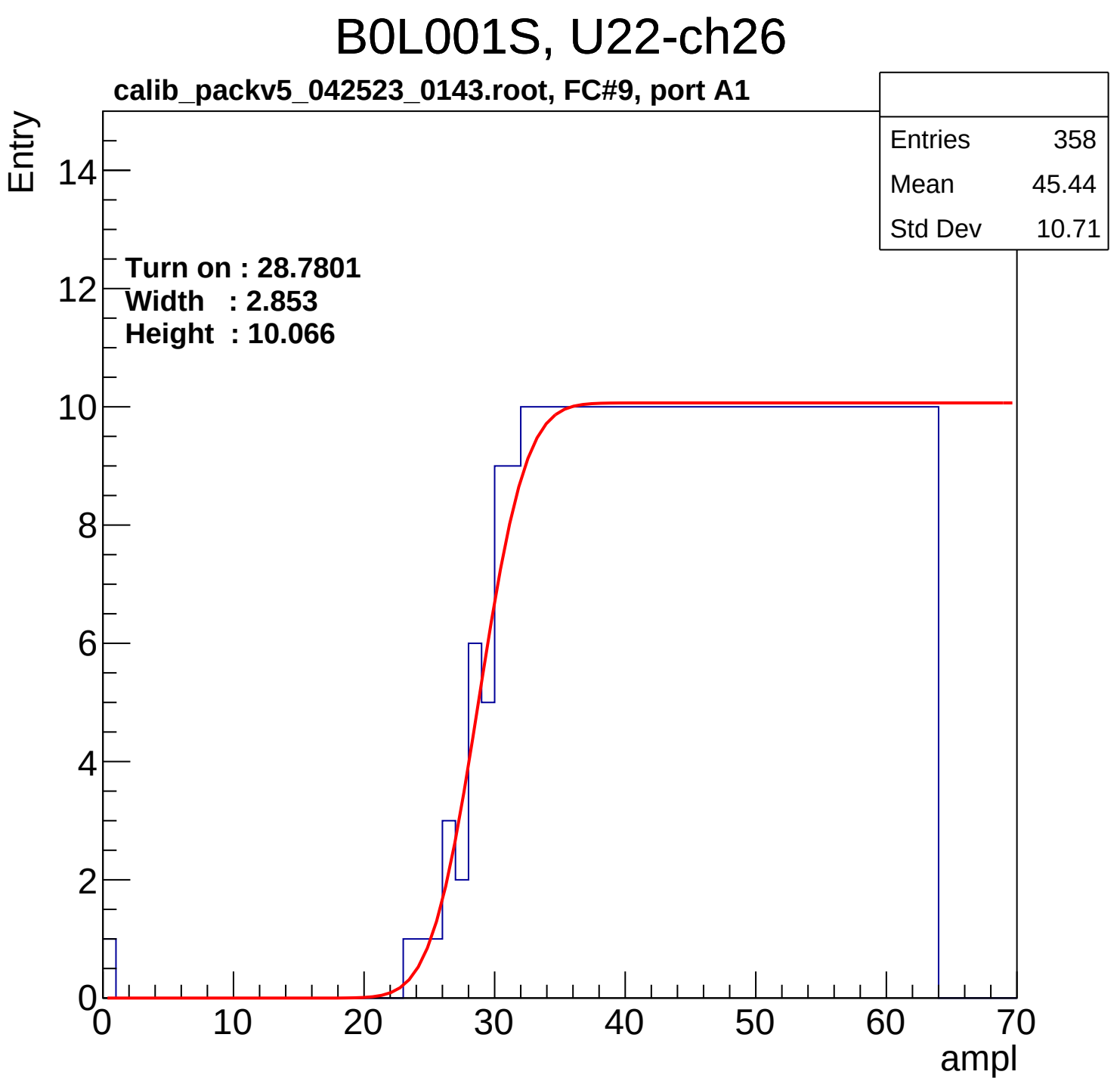
B0L001S, U22-ch26
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.44
Std Dev 10.71
Turn on : 28.7801
Width : 2.853
Height : 10.066
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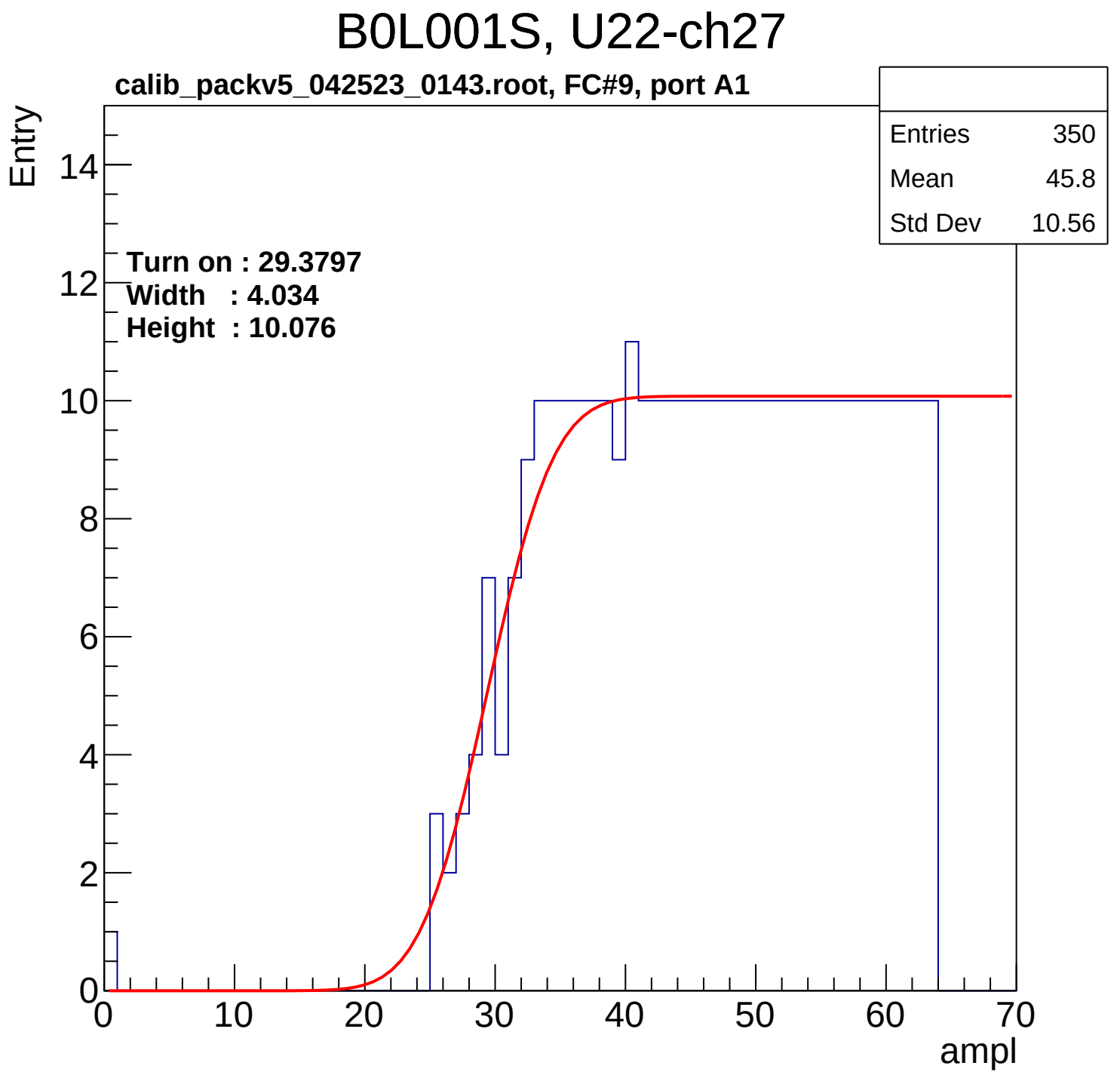
B0L001S, U22-ch27
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.8
Std Dev 10.56
Turn on : 29.3797
Width : 4.034
Height : 10.076
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ampl
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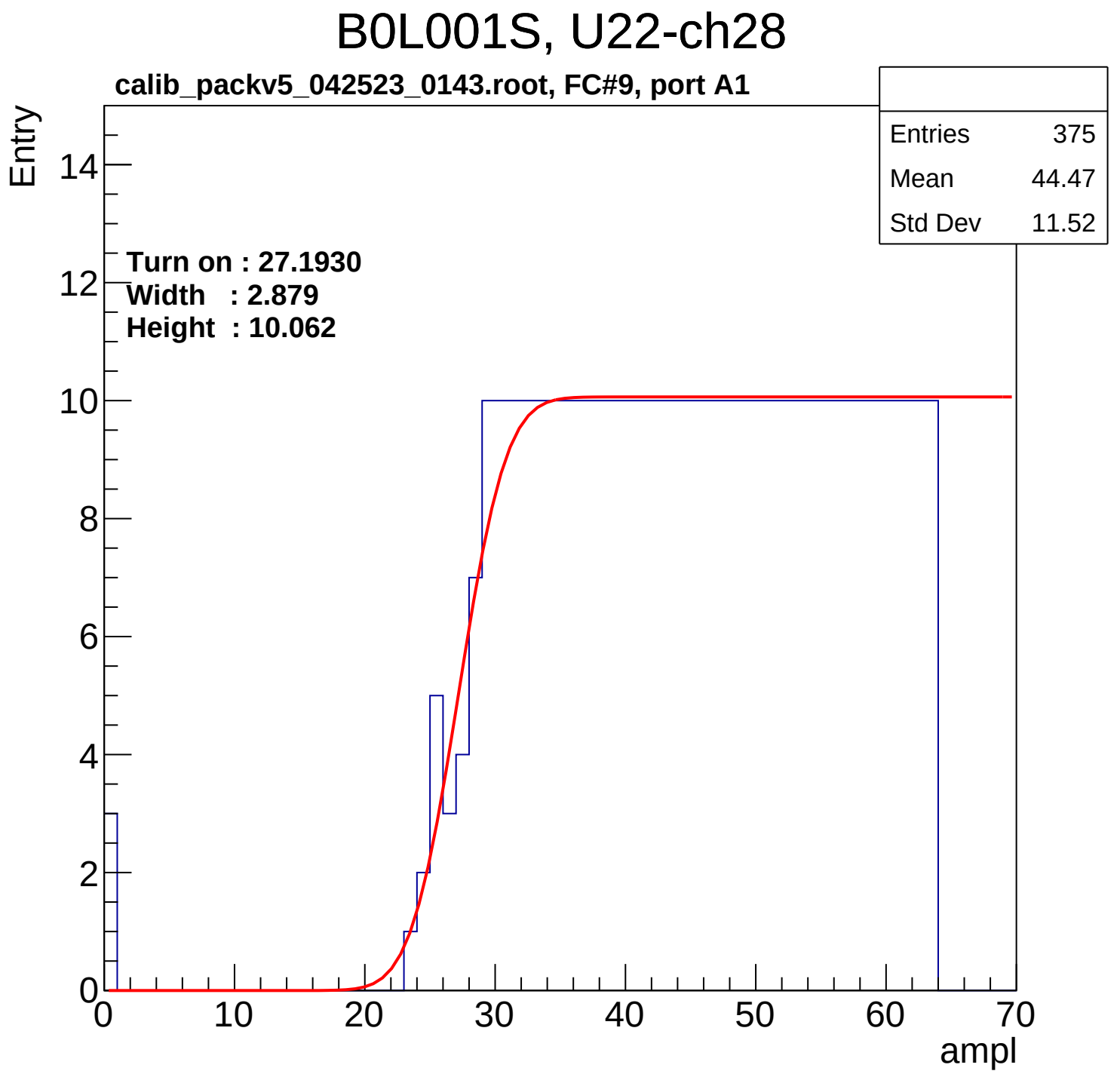
B0L001S, U22-ch28
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.47
Std Dev 11.52
Turn on : 27.1930
Width : 2.879
Height : 10.062
Entry
ampl
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4
6
8
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20
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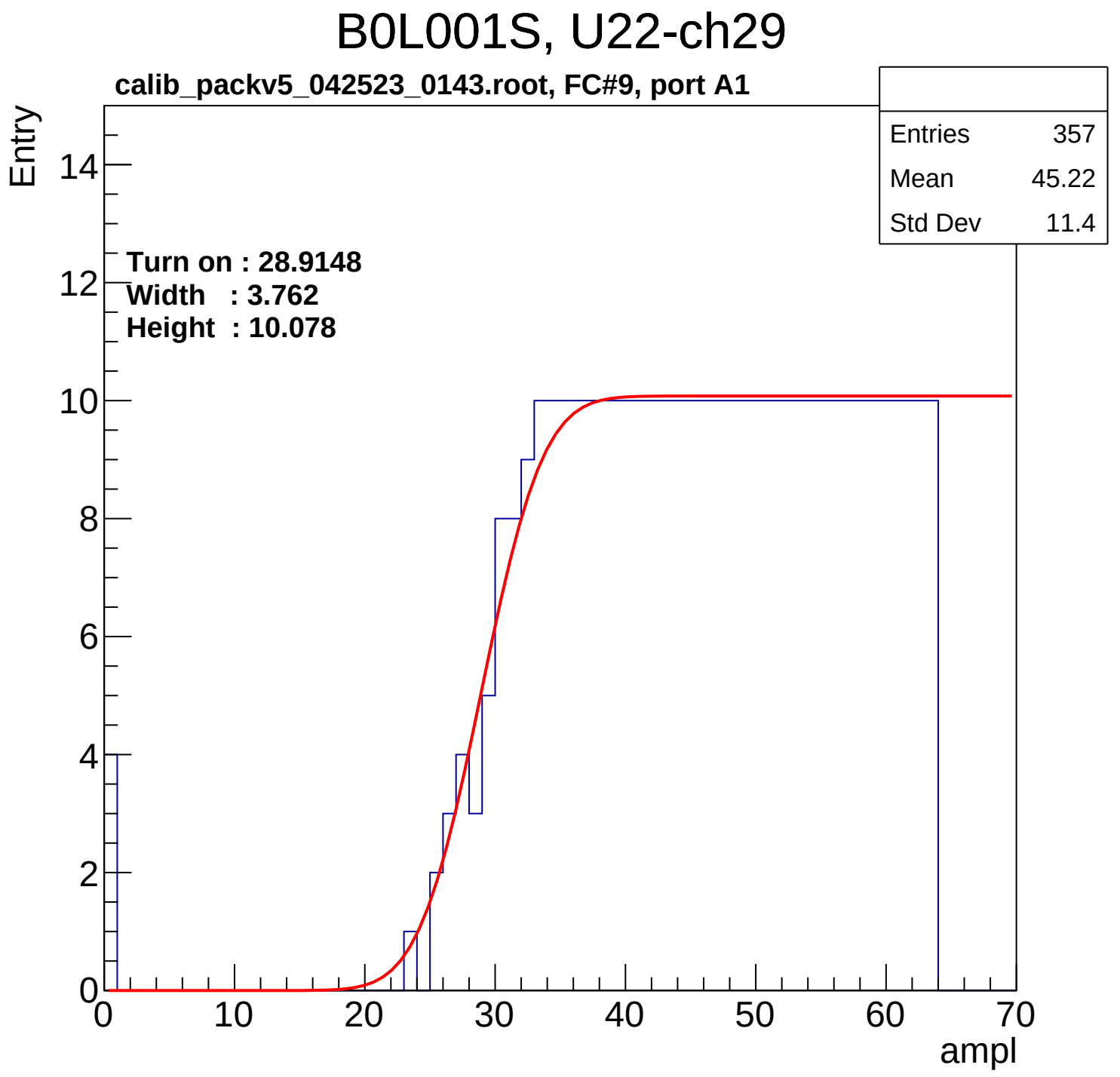
B0L001S, U22-ch29
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.22
Std Dev 11.4
Turn on : 28.9148
Width : 3.762
Height : 10.078
Entry
ampl
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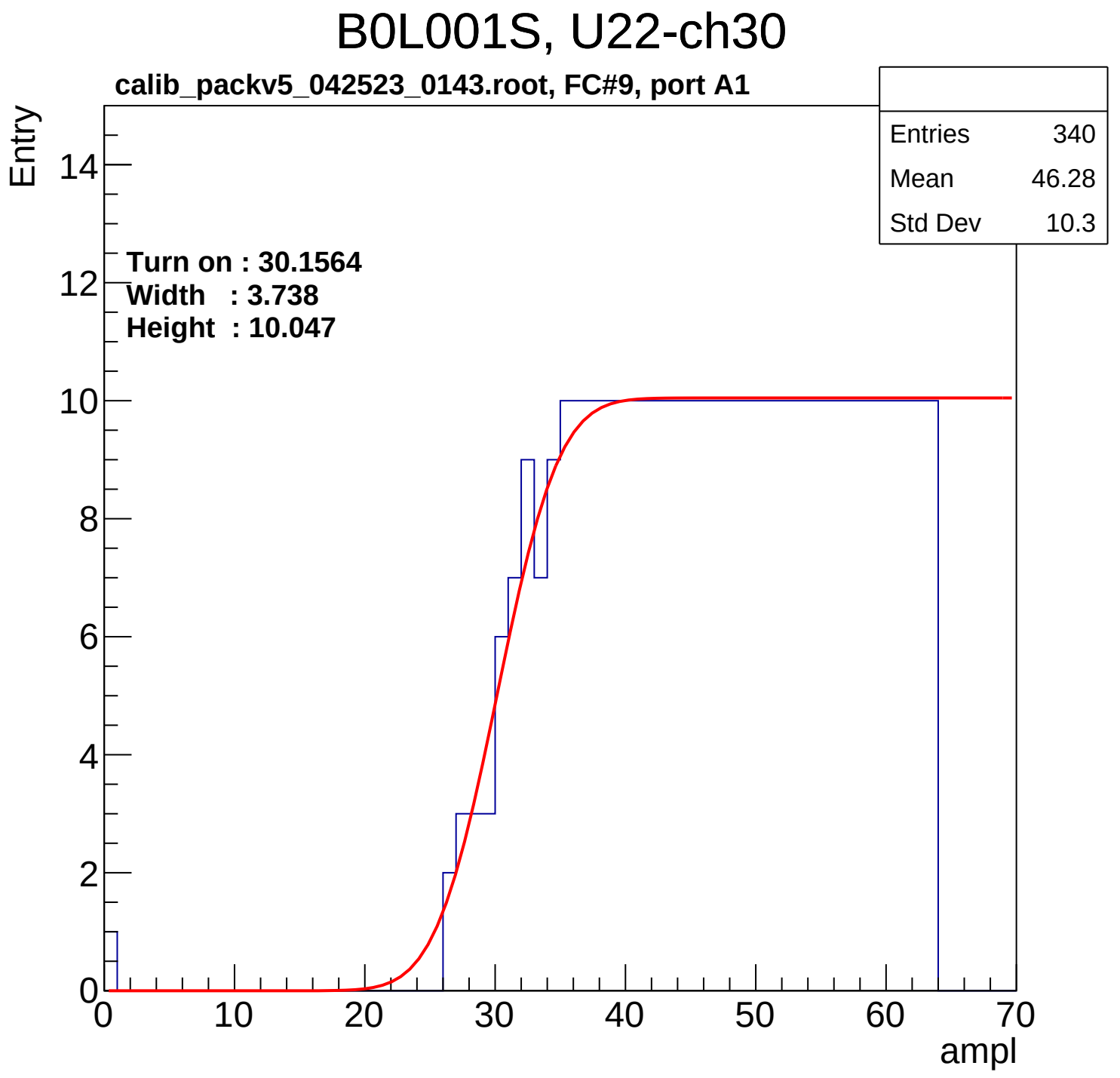
B0L001S, U22-ch30
calib_packv5_042523_0143.root, FC#9, port A1
Entries 340
Mean 46.28
Std Dev 10.3
Turn on : 30.1564
Width : 3.738
Height : 10.047
Entry
ampl
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2
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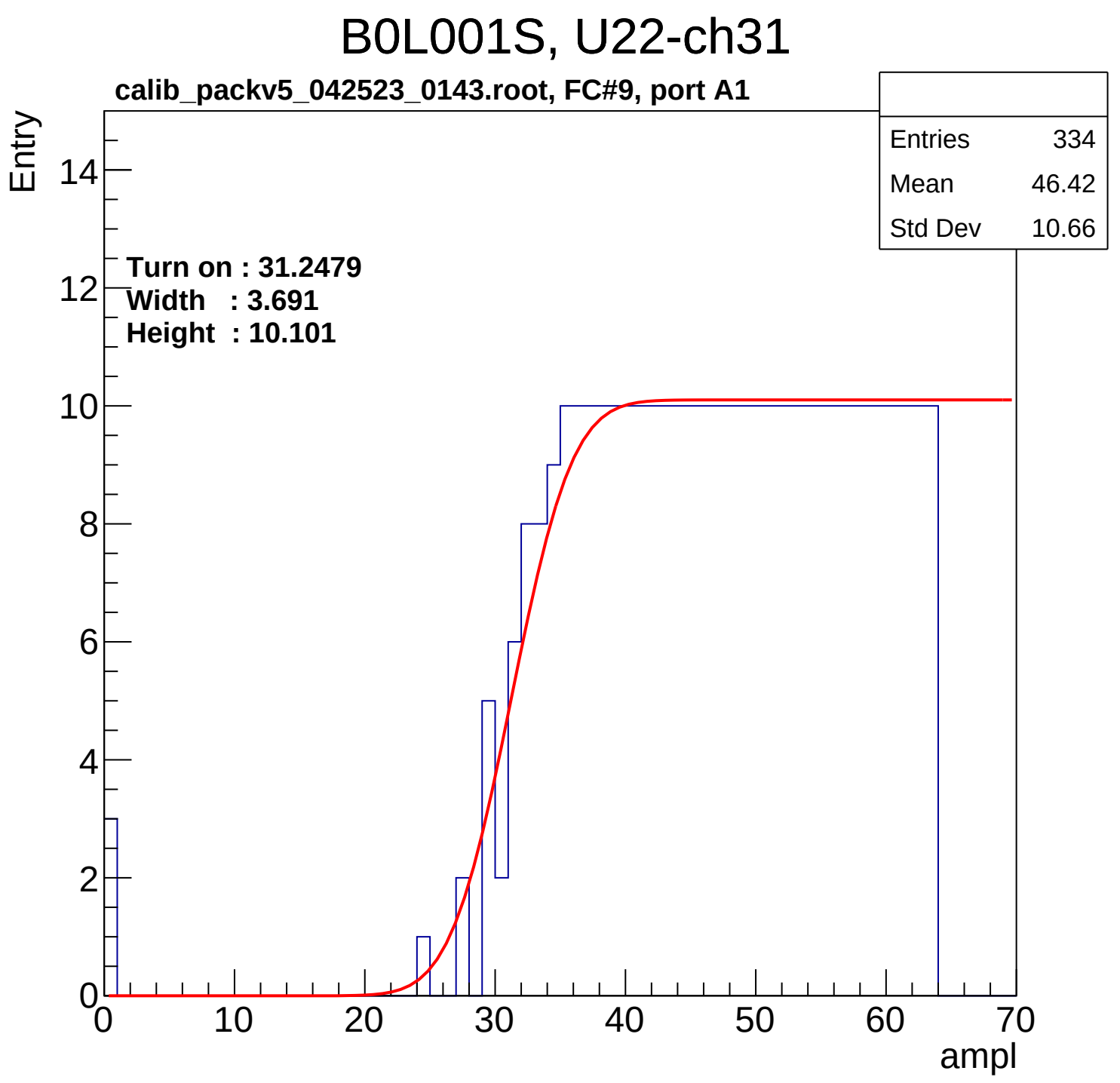
B0L001S, U22-ch31
calib_packv5_042523_0143.root, FC#9, port A1
Entries 334
Mean 46.42
Std Dev 10.66
Turn on : 31.2479
Width : 3.691
Height : 10.101
Entry
ampl
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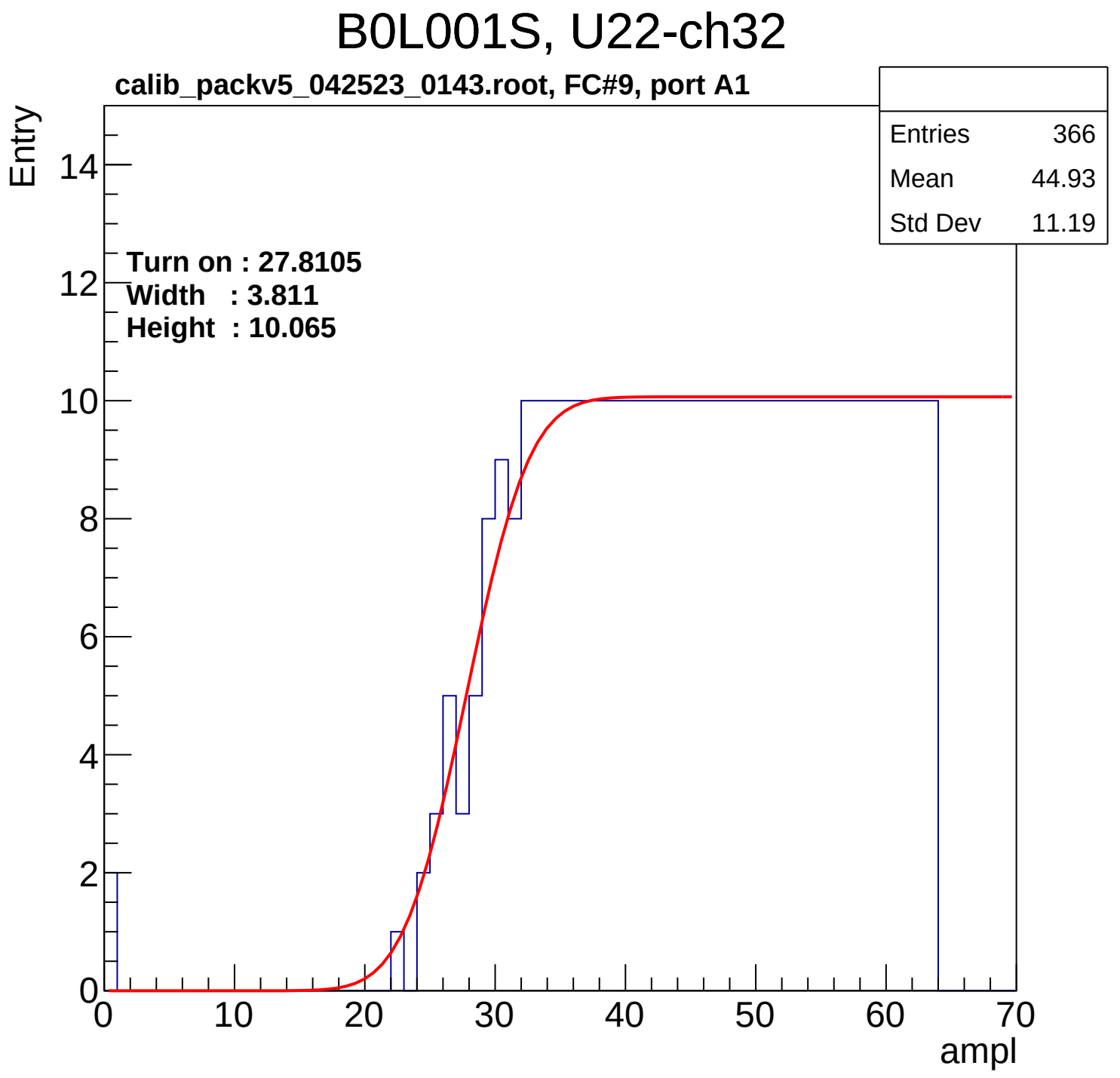
B0L001S, U22-ch32
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.93
Std Dev 11.19
Turn on : 27.8105
Width : 3.811
Height : 10.065
Entry
ampl
0
2
4
6
8
10
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0
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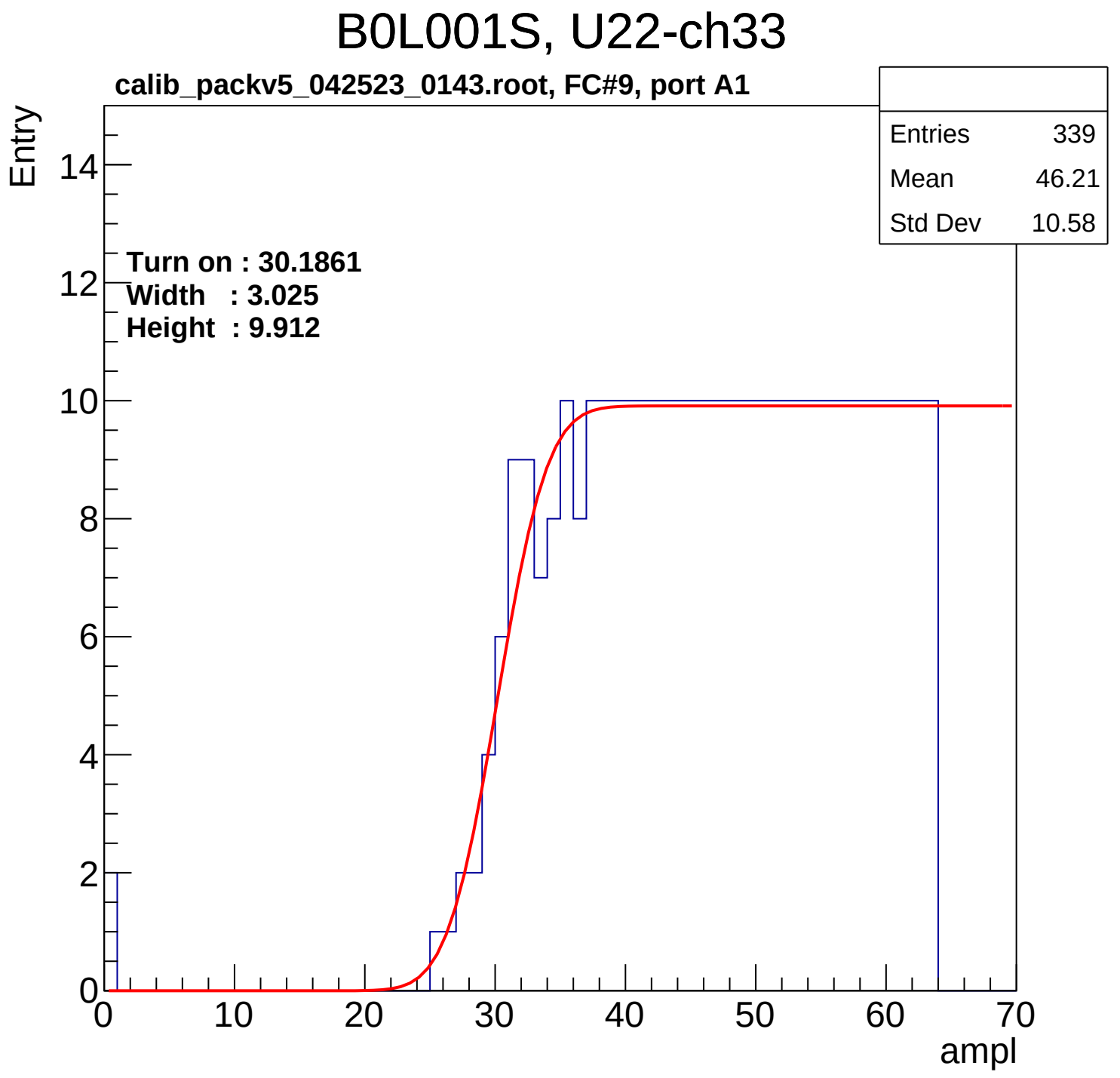
B0L001S, U22-ch33
calib_packv5_042523_0143.root, FC#9, port A1
Entries 339
Mean 46.21
Std Dev 10.58
Turn on : 30.1861
Width : 3.025
Height : 9.912
Entry
ampl
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4
6
8
10
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0
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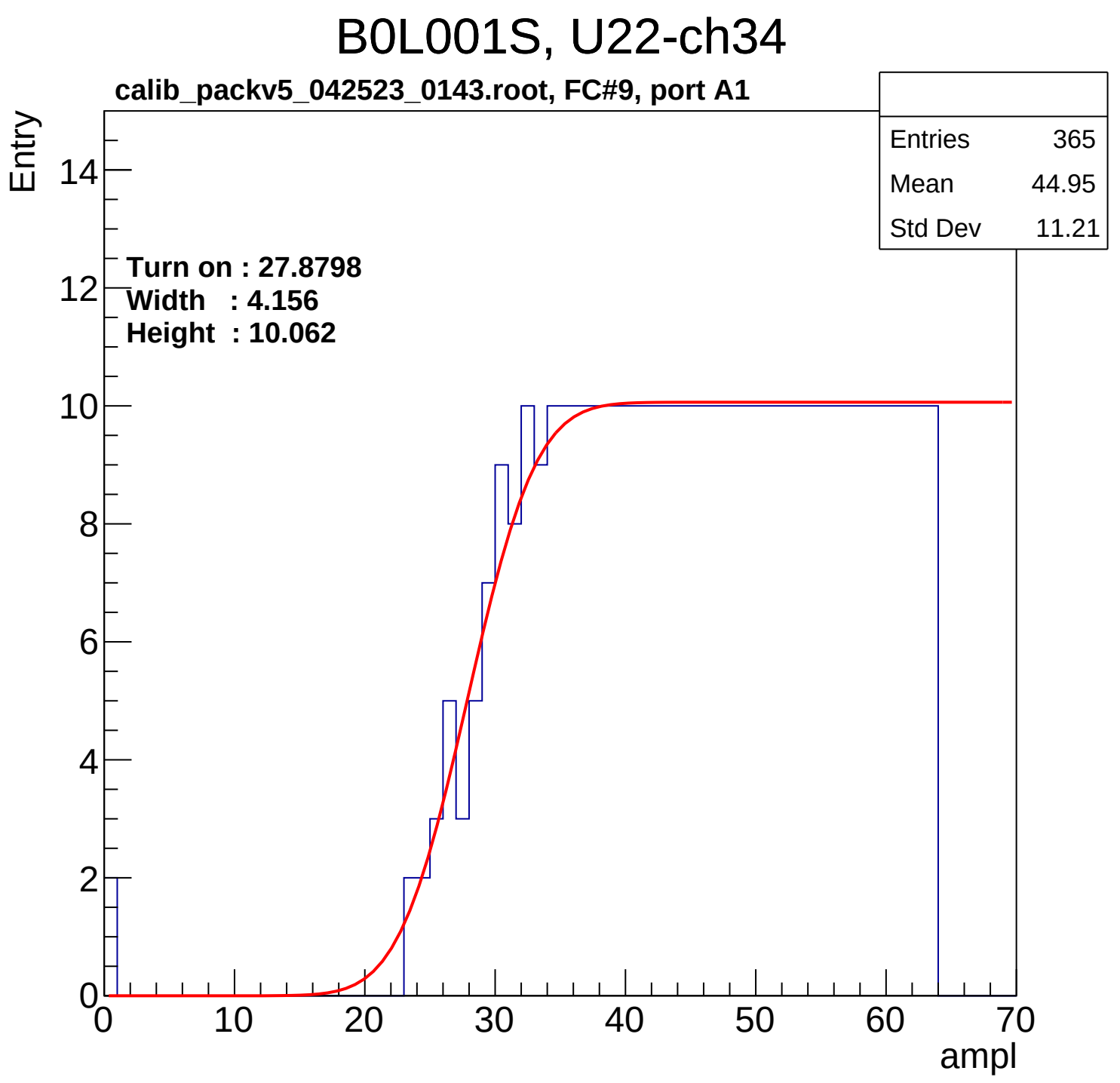
B0L001S, U22-ch34
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.95
Std Dev 11.21
Turn on : 27.8798
Width : 4.156
Height : 10.062
Entry
ampl
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6
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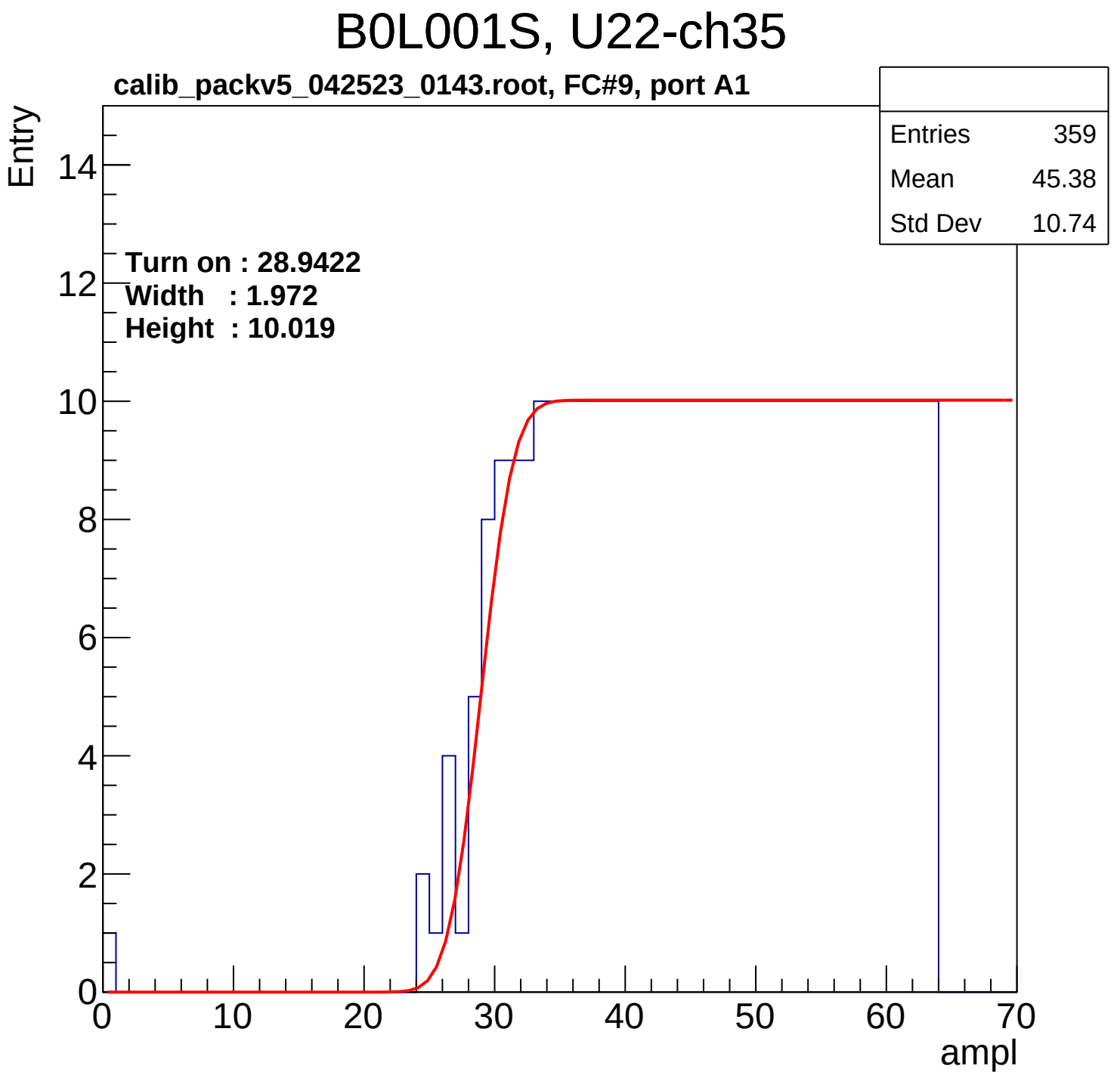
B0L001S, U22-ch35
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.38
Std Dev 10.74
Turn on : 28.9422
Width : 1.972
Height : 10.019
Entry
ampl
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6
8
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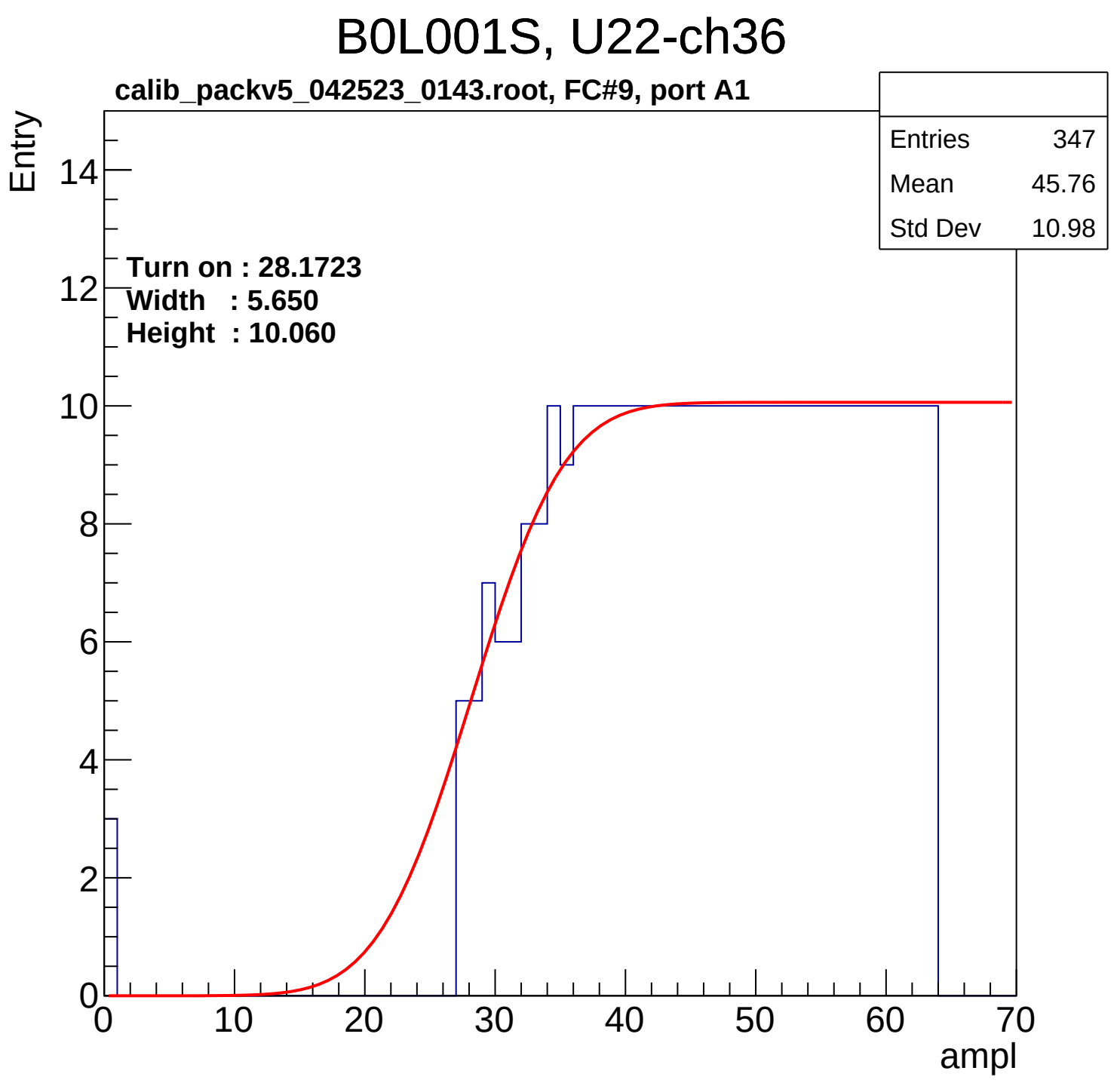
B0L001S, U22-ch36
calib_packv5_042523_0143.root, FC#9, port A1
Entries 347
Mean 45.76
Std Dev 10.98
Turn on : 28.1723
Width : 5.650
Height : 10.060
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
50
60
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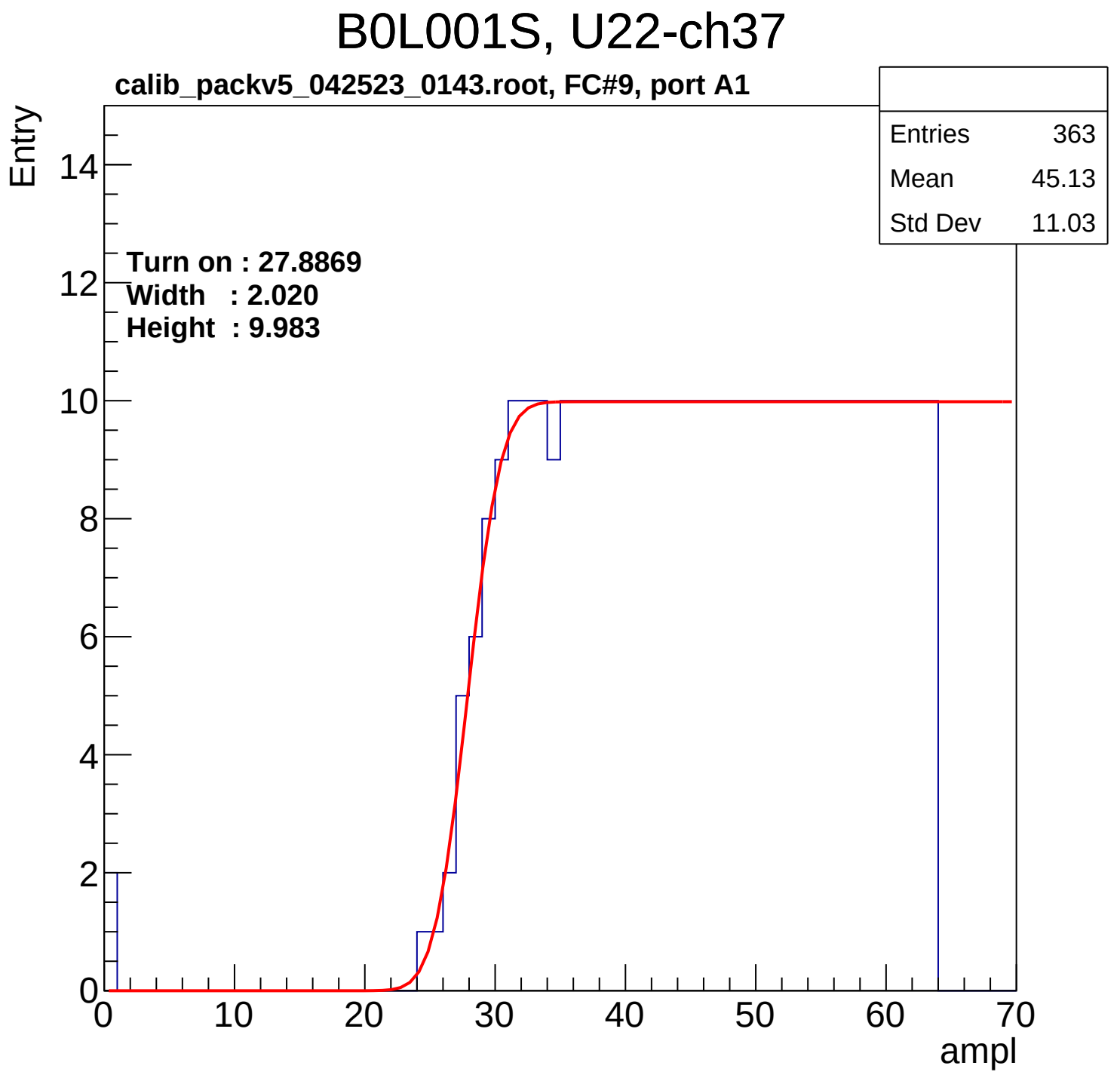
B0L001S, U22-ch37
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.13
Std Dev 11.03
Turn on : 27.8869
Width : 2.020
Height : 9.983
Entry
ampl
0
2
4
6
8
10
12
14
0
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40
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60
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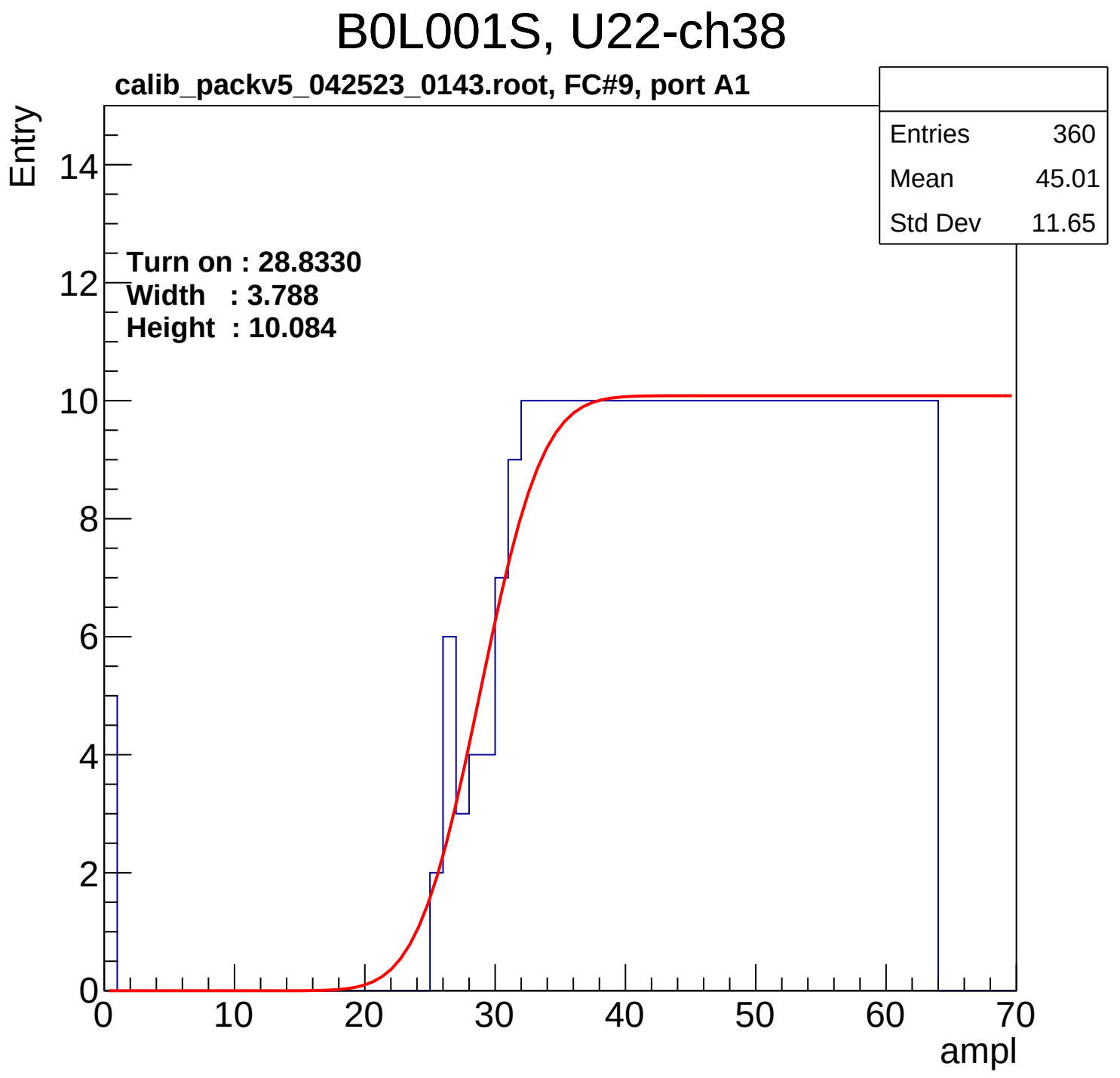
B0L001S, U22-ch38
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.01
Std Dev 11.65
Turn on : 28.8330
Width : 3.788
Height : 10.084
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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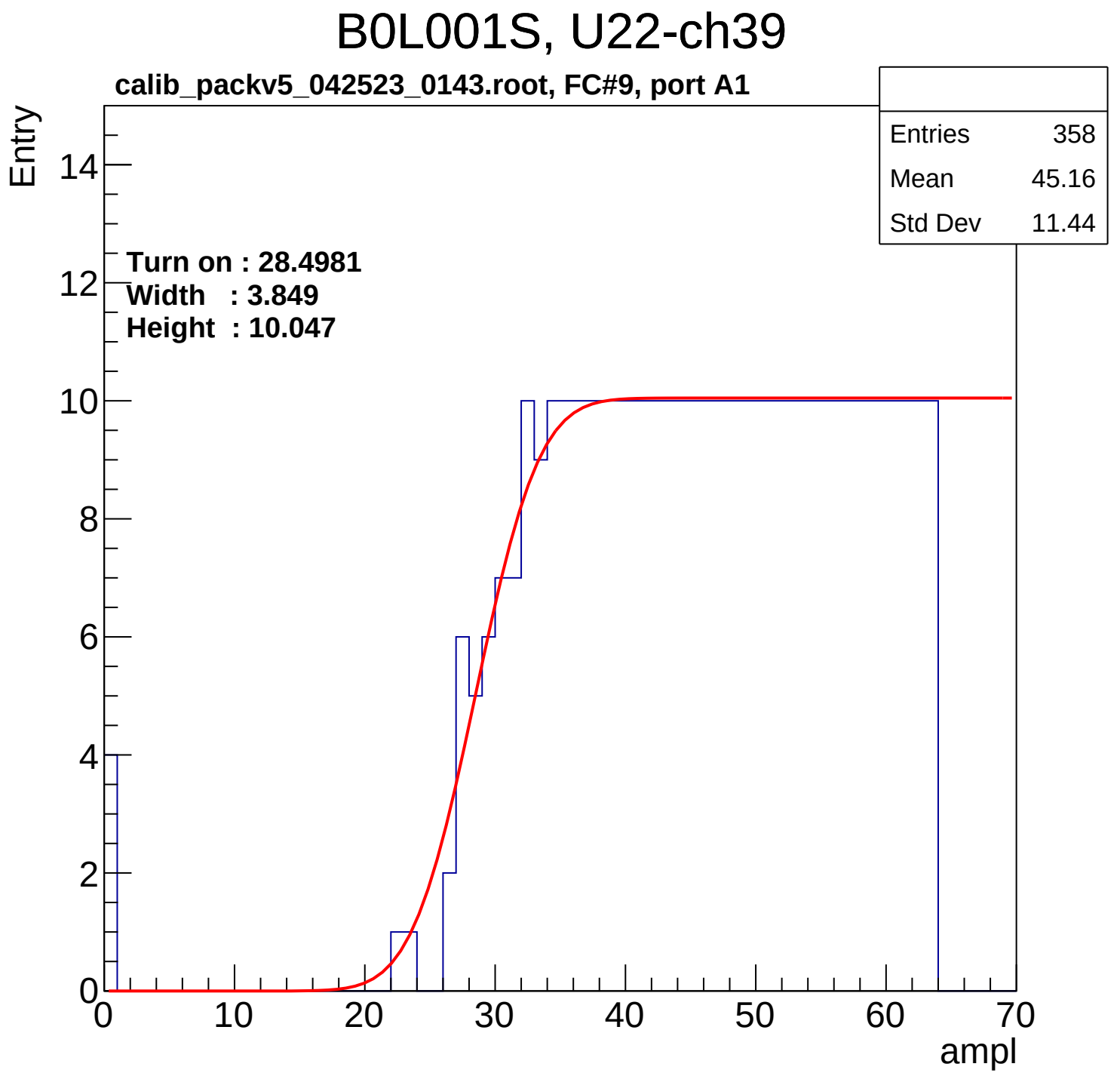
B0L001S, U22-ch39
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.16
Std Dev 11.44
Turn on : 28.4981
Width : 3.849
Height : 10.047
Entry
ampl
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6
8
10
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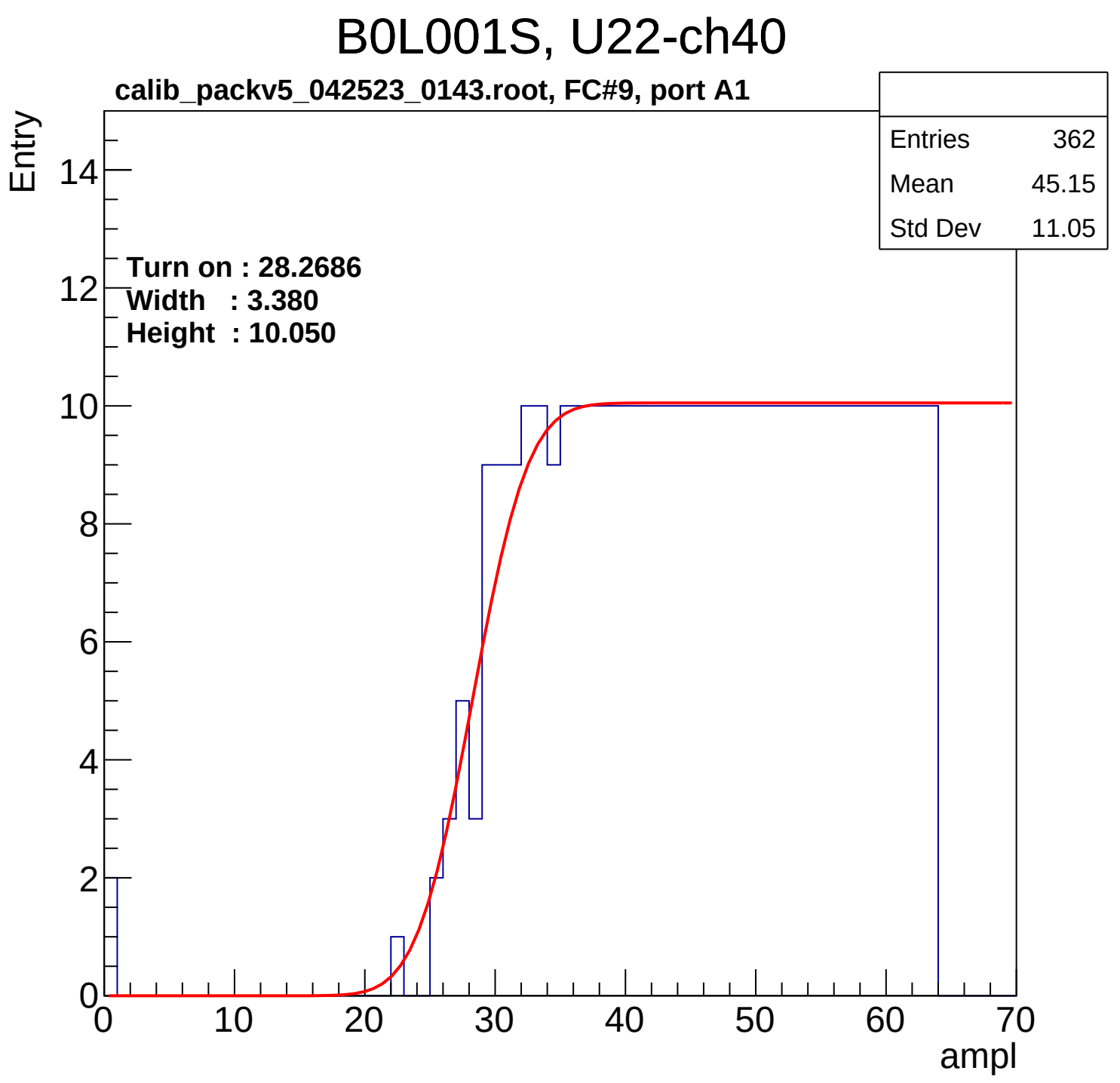
B0L001S, U22-ch40
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.15
Std Dev 11.05
Turn on : 28.2686
Width : 3.380
Height : 10.050
Entry
ampl
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6
8
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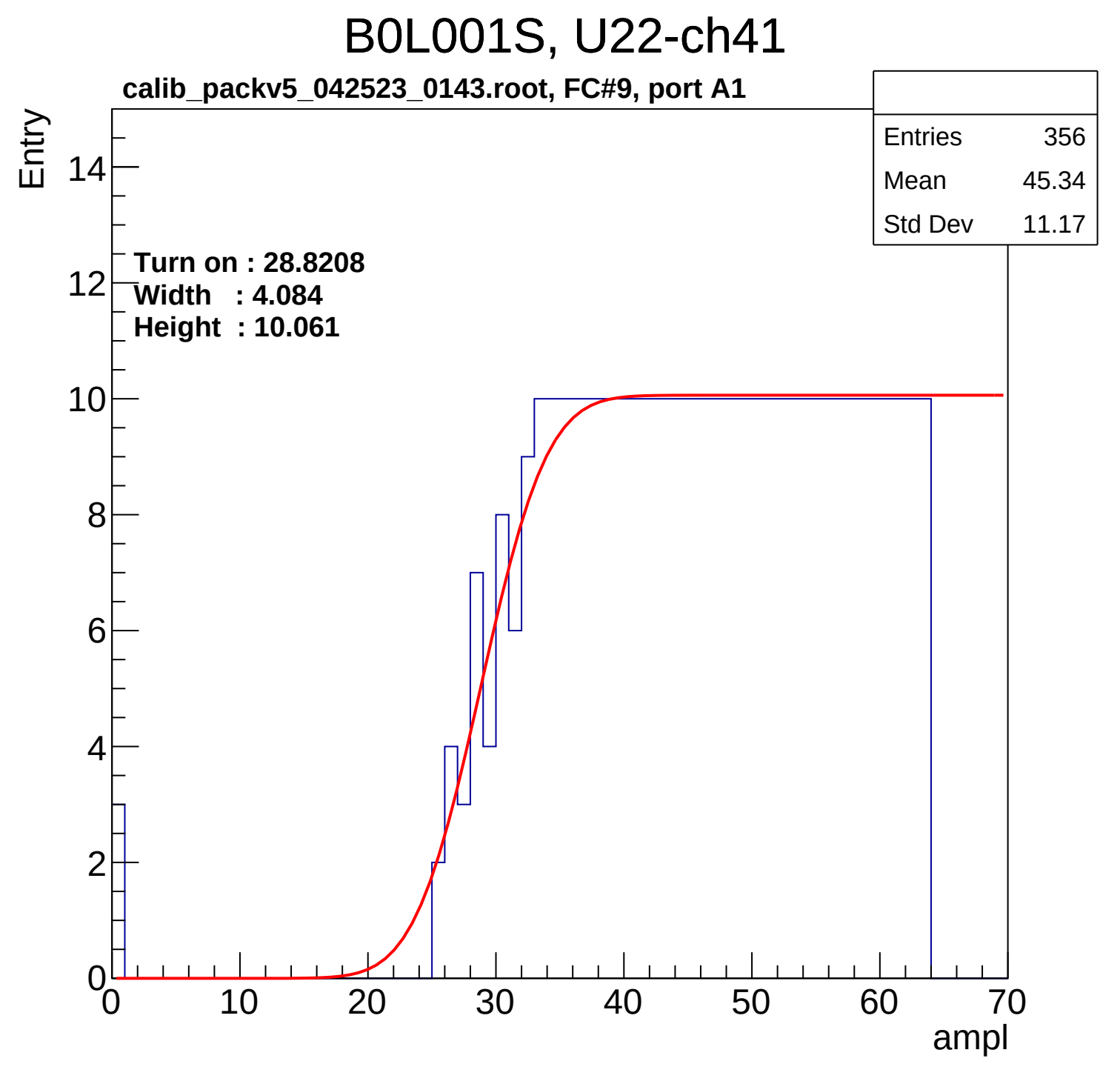
B0L001S, U22-ch41
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.34
Std Dev 11.17
Turn on : 28.8208
Width : 4.084
Height : 10.061
Entry
ampl
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2
4
6
8
10
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0
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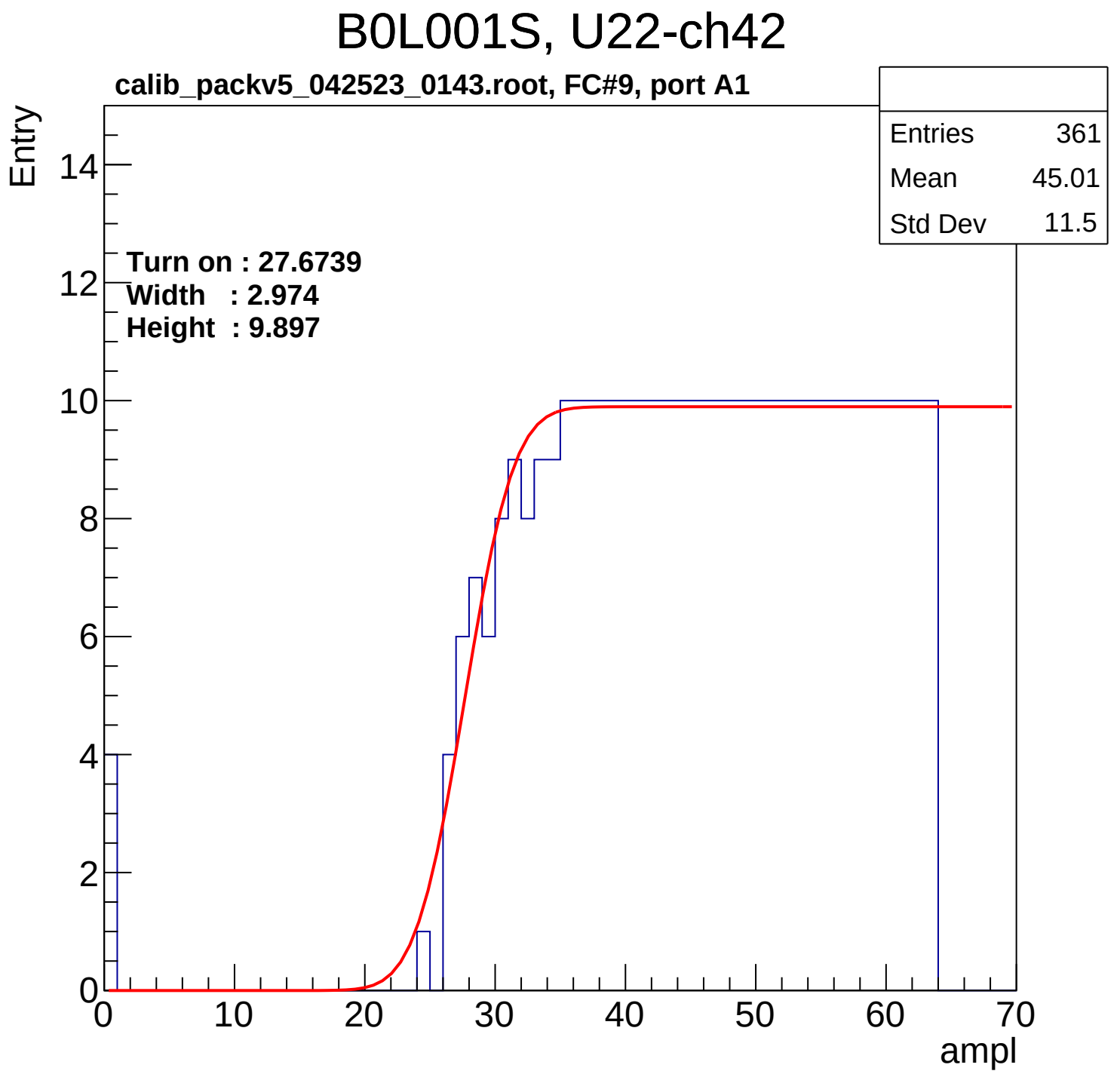
B0L001S, U22-ch42
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.01
Std Dev 11.5
Turn on : 27.6739
Width : 2.974
Height : 9.897
Entry
ampl
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2
4
6
8
10
12
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0
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40
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60
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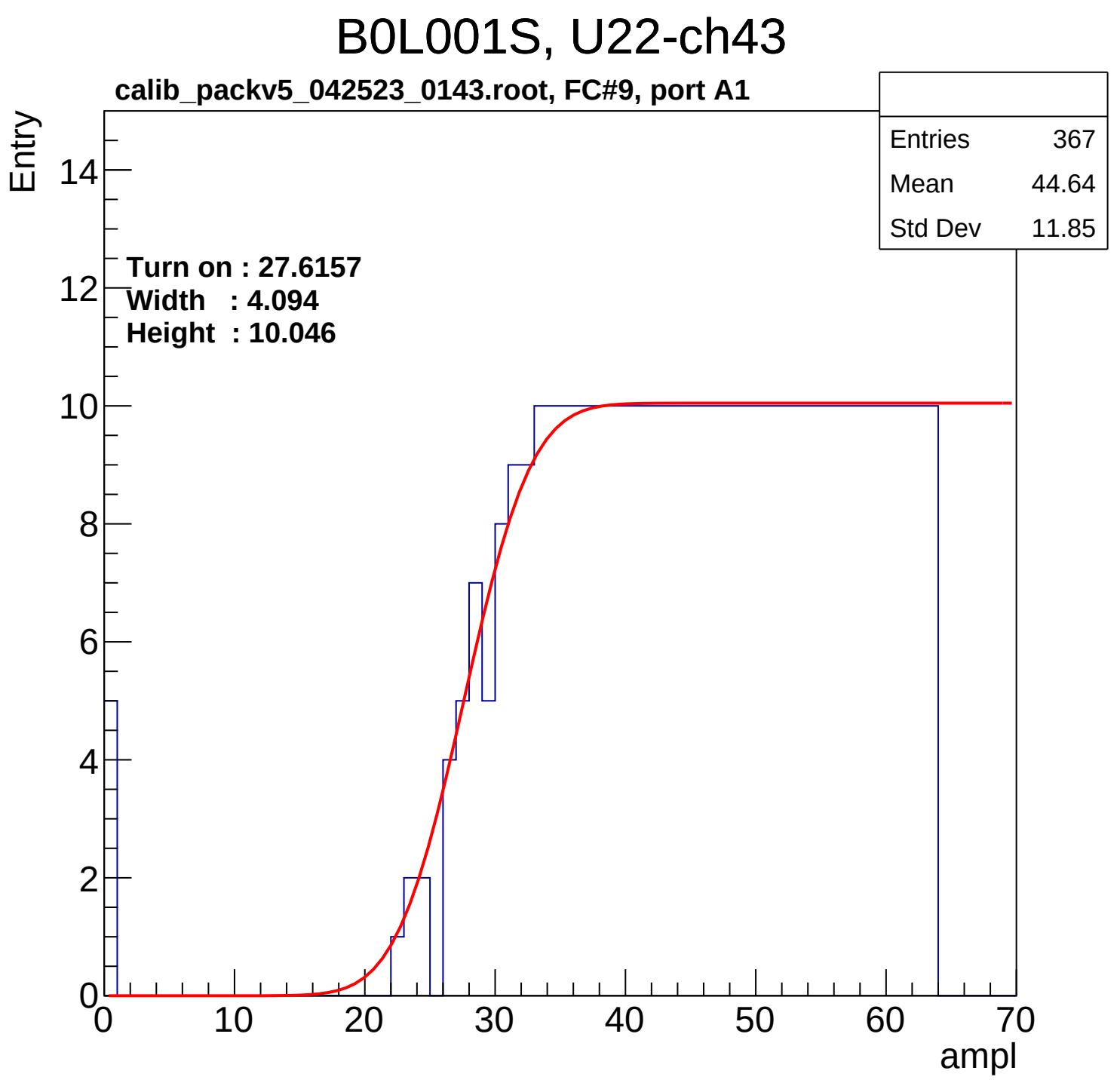
B0L001S, U22-ch43
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.64
Std Dev 11.85
Turn on : 27.6157
Width : 4.094
Height : 10.046
Entry
ampl
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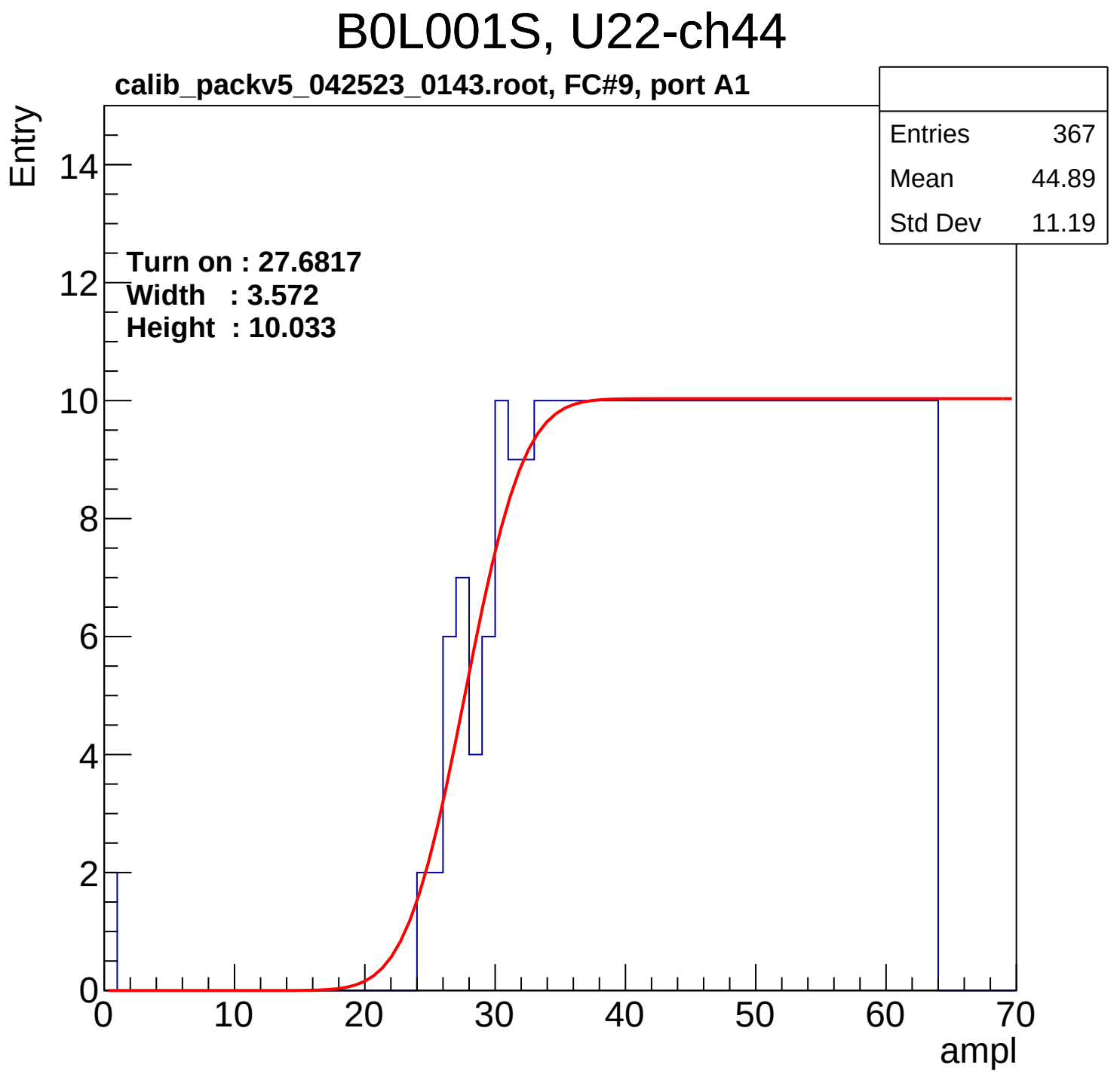
B0L001S, U22-ch44
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.89
Std Dev 11.19
Turn on : 27.6817
Width : 3.572
Height : 10.033
Entry
ampl
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8
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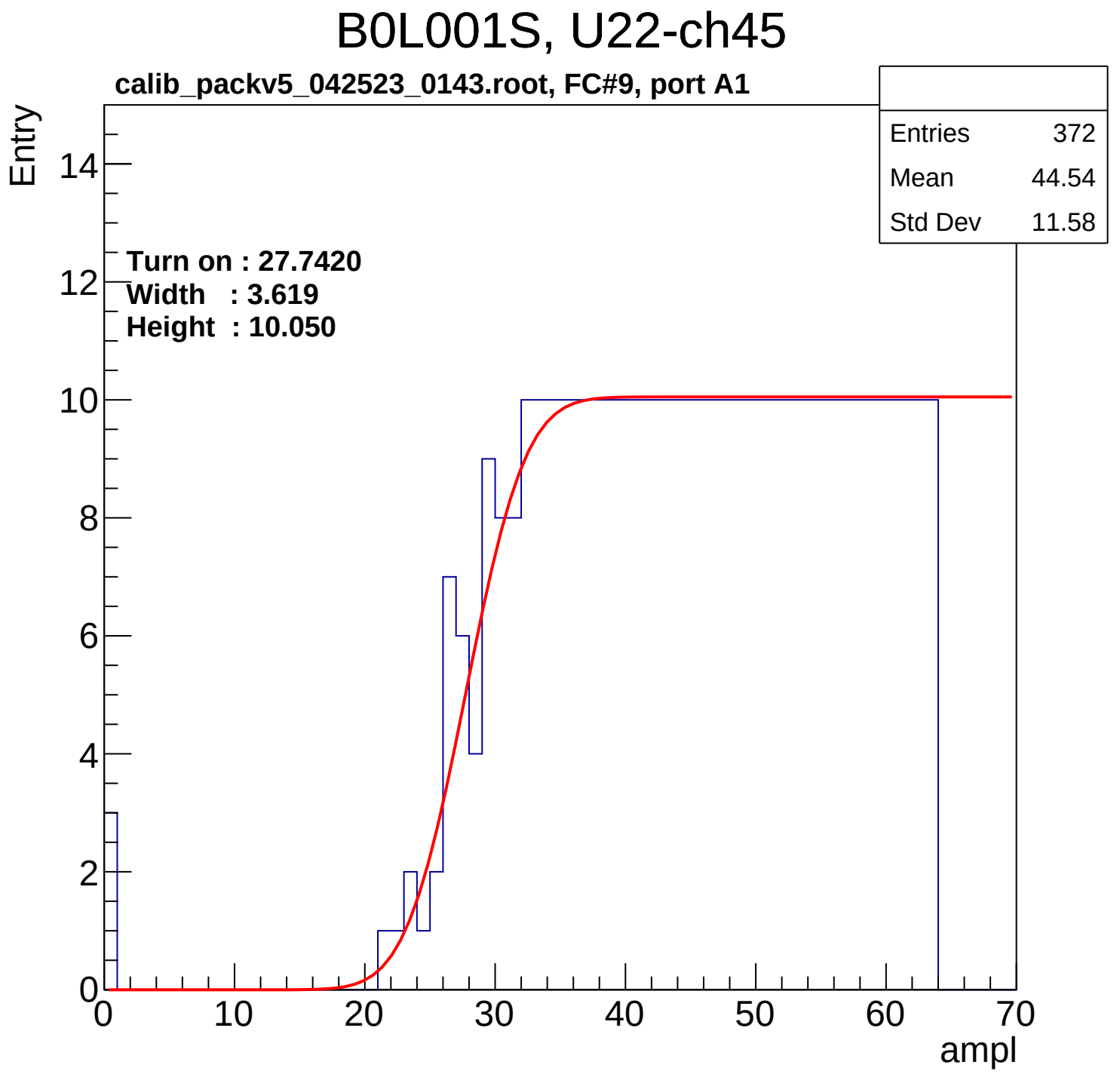
B0L001S, U22-ch45
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.54
Std Dev 11.58
Turn on : 27.7420
Width : 3.619
Height : 10.050
Entry
ampl
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6
8
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60
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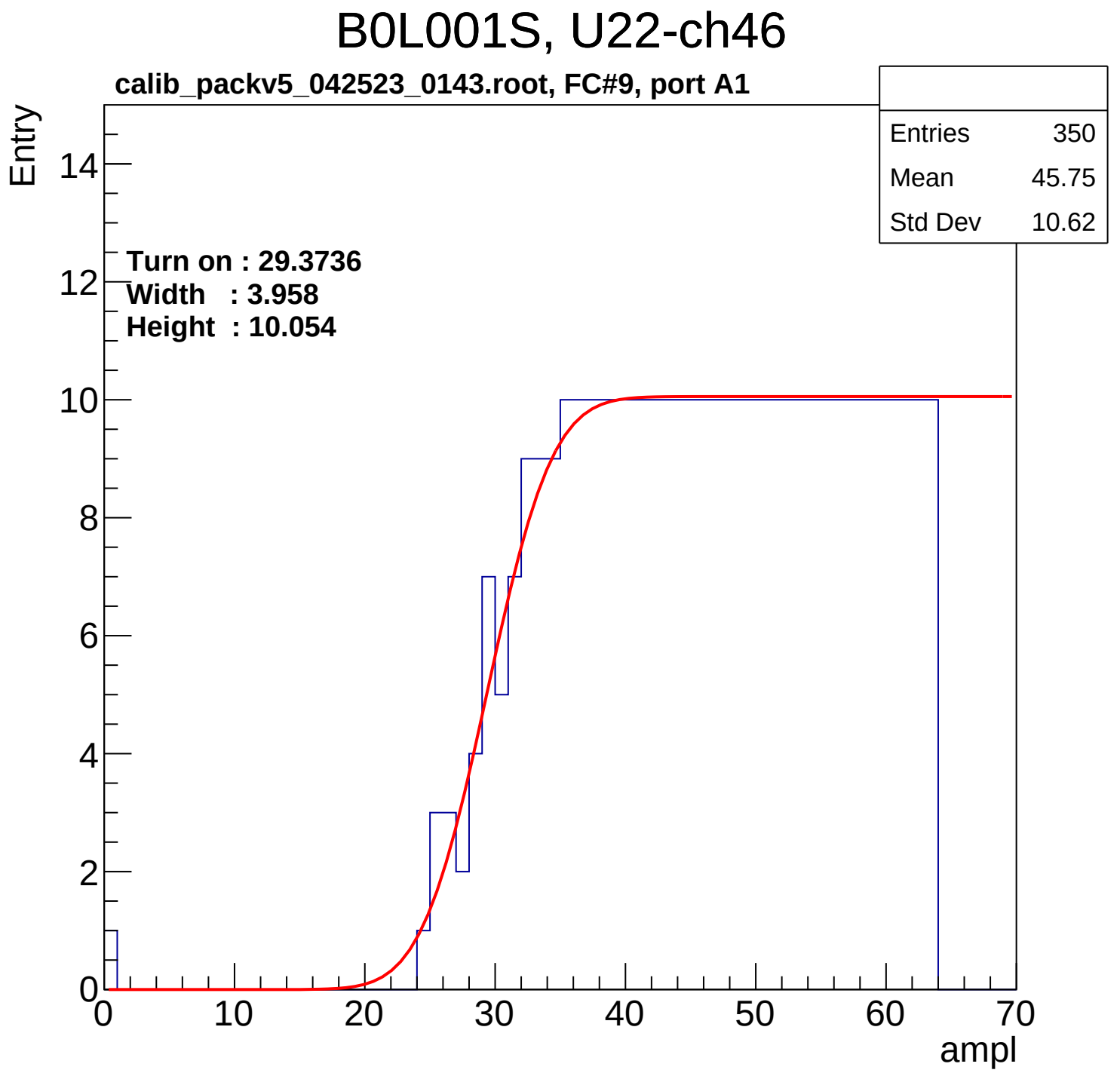
B0L001S, U22-ch46
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.75
Std Dev 10.62
Turn on : 29.3736
Width : 3.958
Height : 10.054
Entry
ampl
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6
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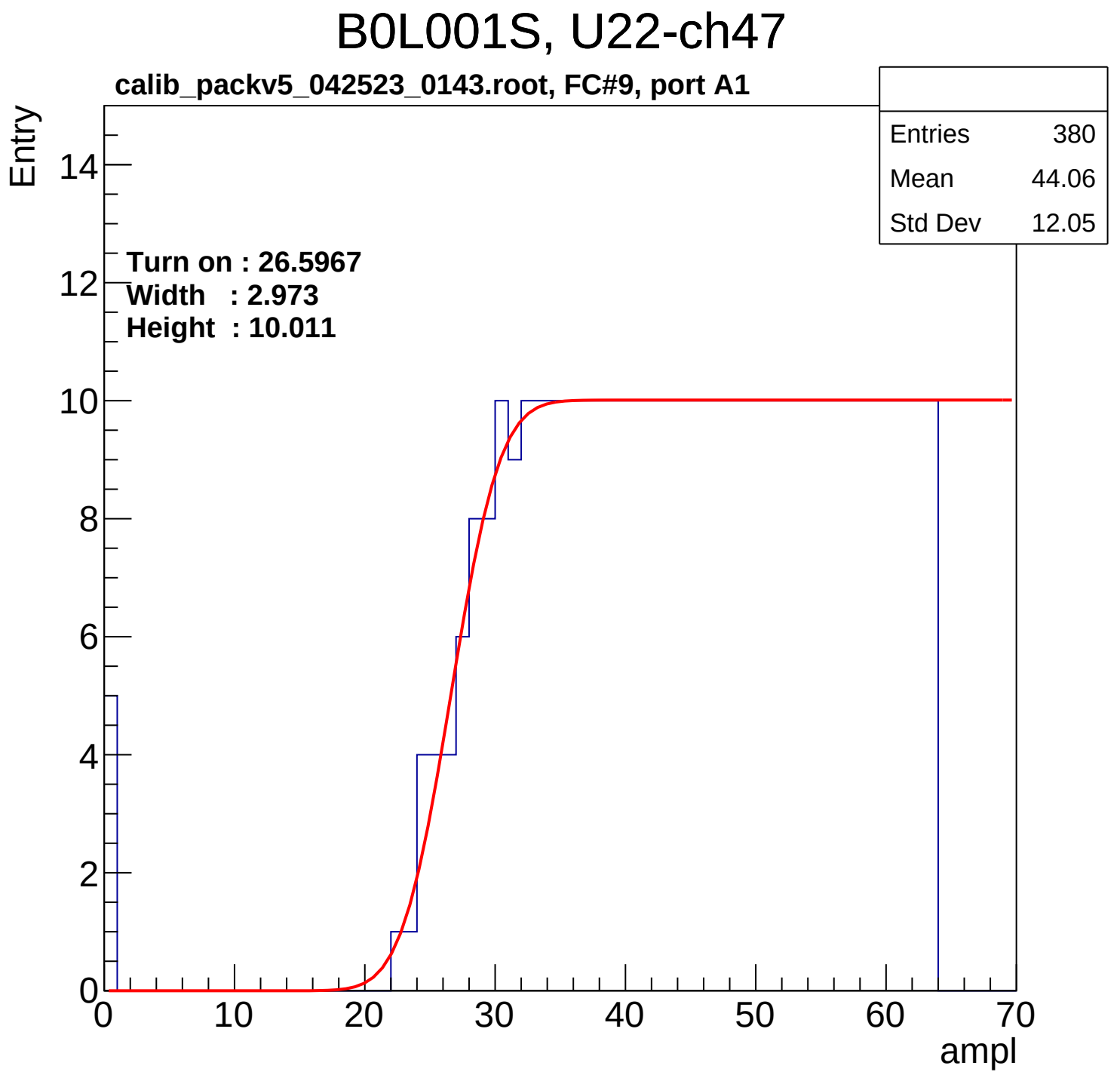
B0L001S, U22-ch47
calib_packv5_042523_0143.root, FC#9, port A1
Entries 380
Mean 44.06
Std Dev 12.05
Turn on : 26.5967
Width : 2.973
Height : 10.011
Entry
ampl
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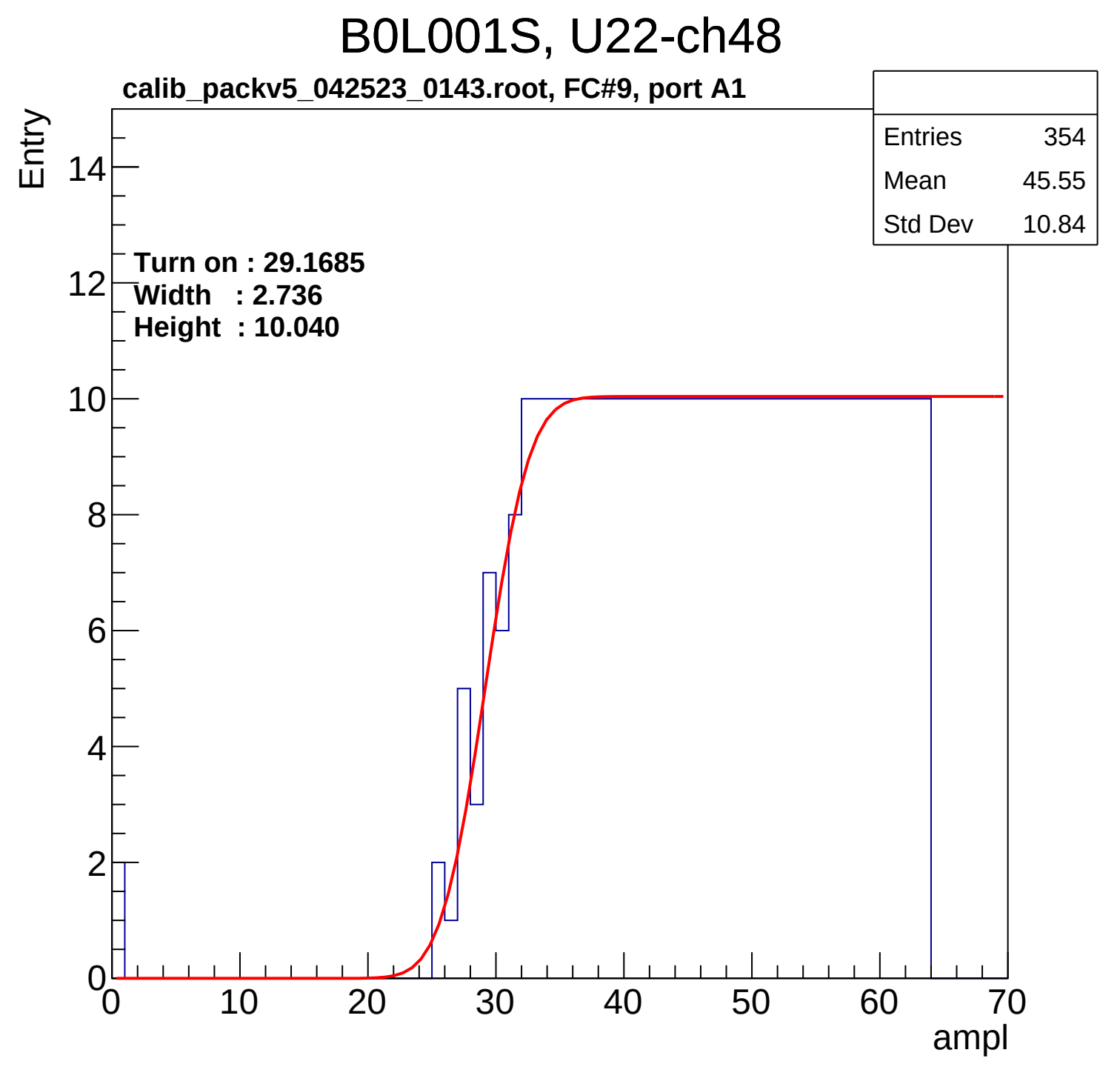
B0L001S, U22-ch48
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.55
Std Dev 10.84
Turn on : 29.1685
Width : 2.736
Height : 10.040
Entry
ampl
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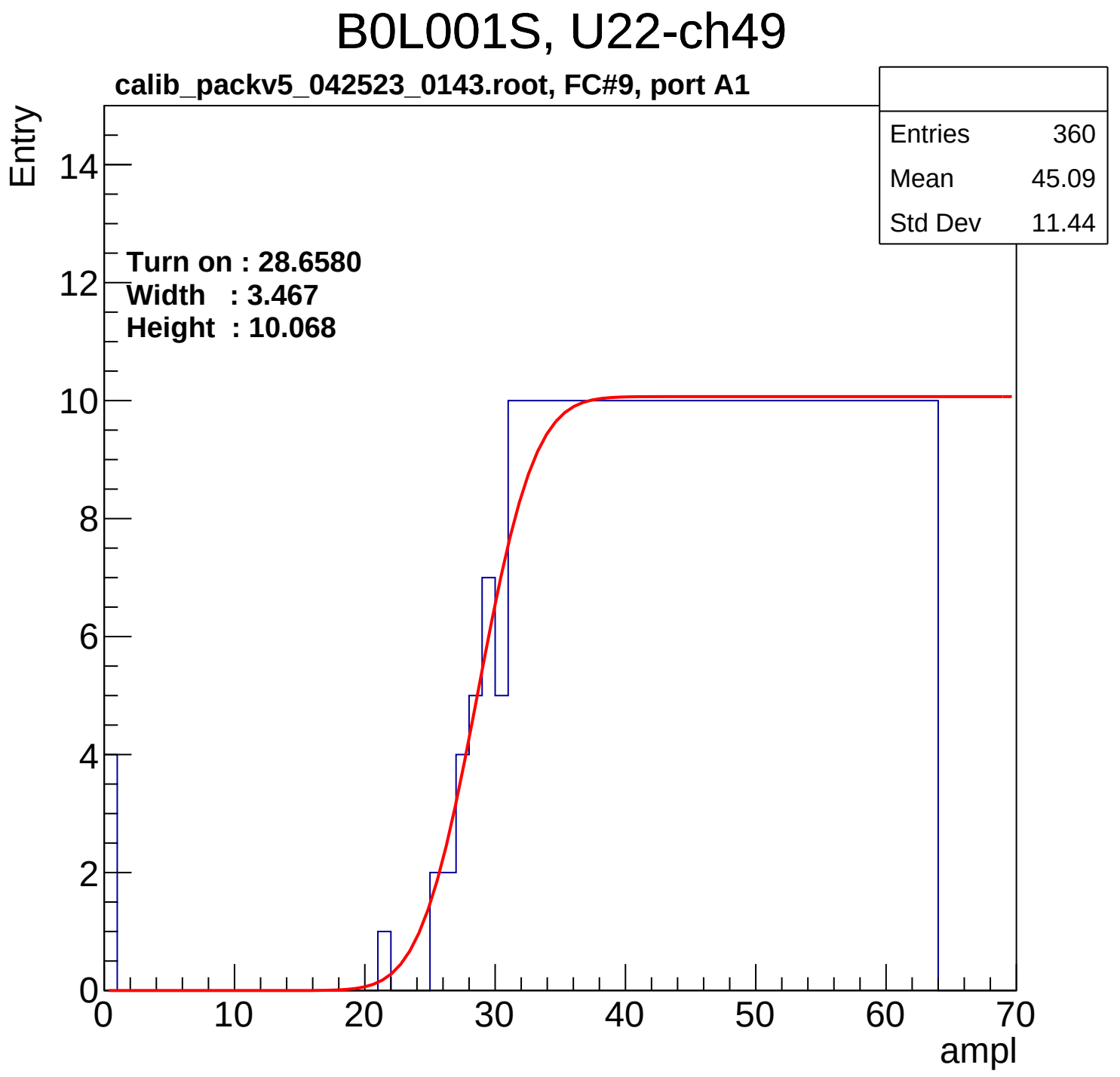
B0L001S, U22-ch49
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.09
Std Dev 11.44
Turn on : 28.6580
Width : 3.467
Height : 10.068
Entry
ampl
0
2
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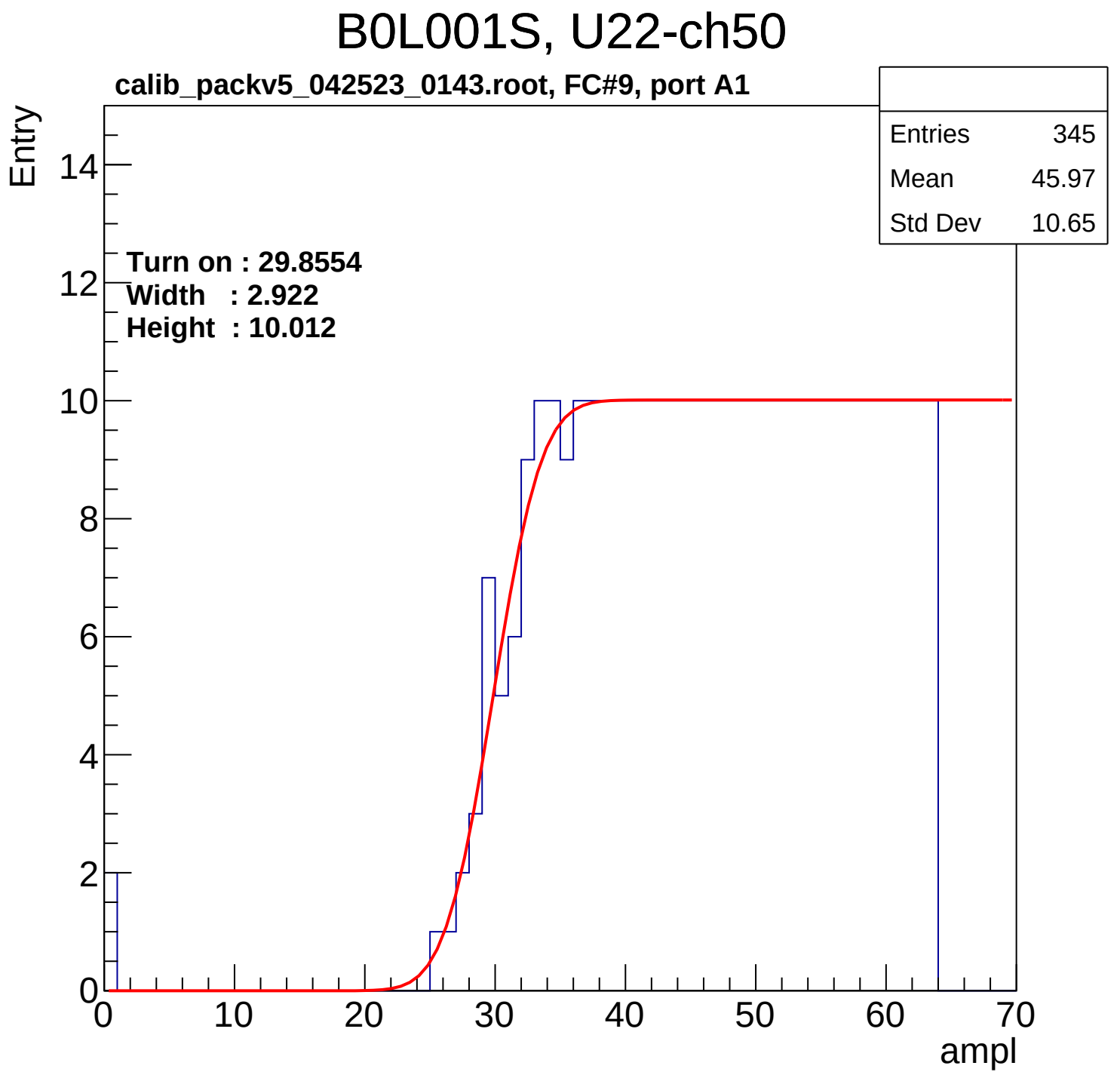
B0L001S, U22-ch50
calib_packv5_042523_0143.root, FC#9, port A1
Entries 345
Mean 45.97
Std Dev 10.65
Turn on : 29.8554
Width : 2.922
Height : 10.012
Entry
ampl
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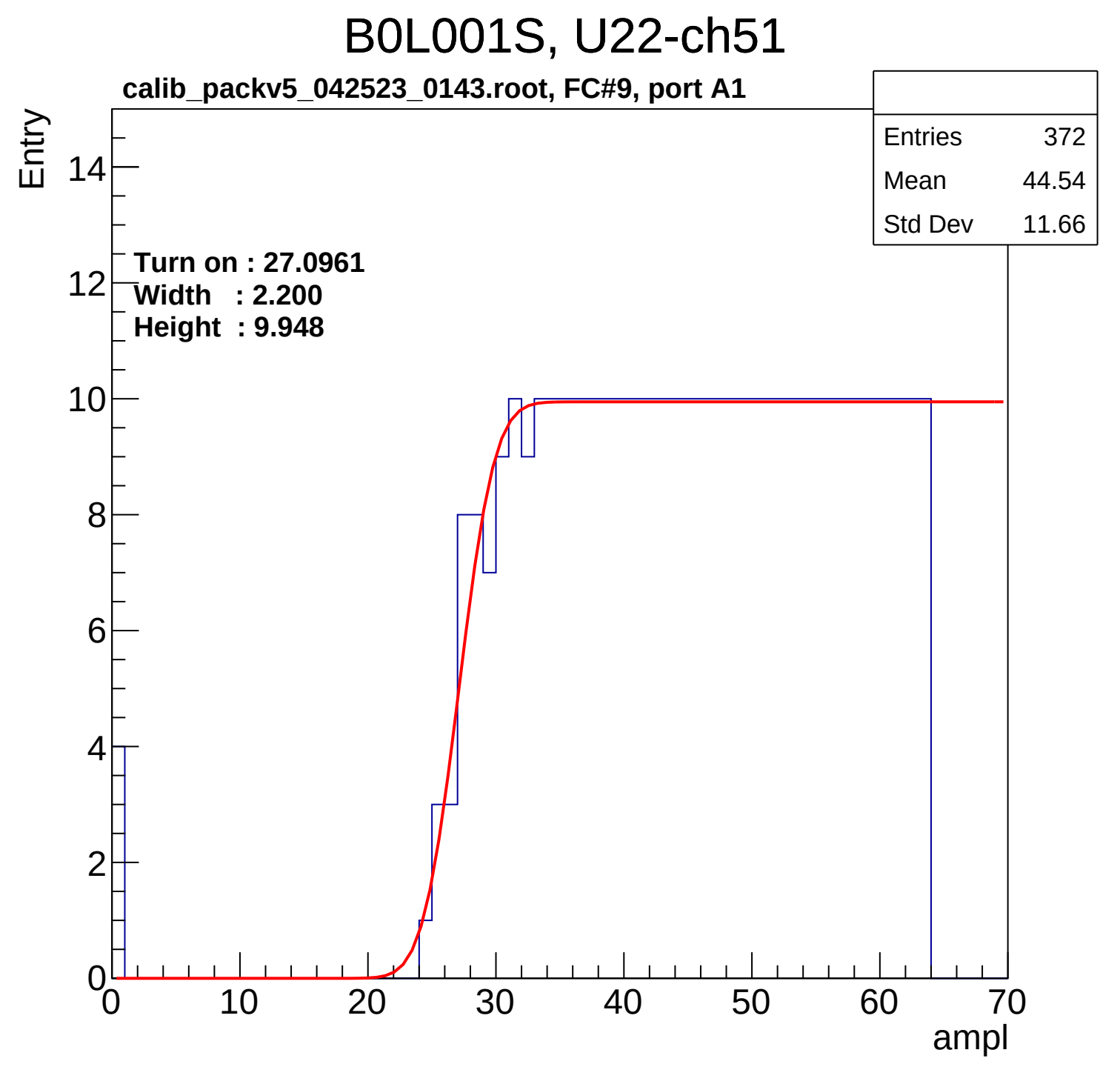
B0L001S, U22-ch51
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.54
Std Dev 11.66
Turn on : 27.0961
Width : 2.200
Height : 9.948
Entry
ampl
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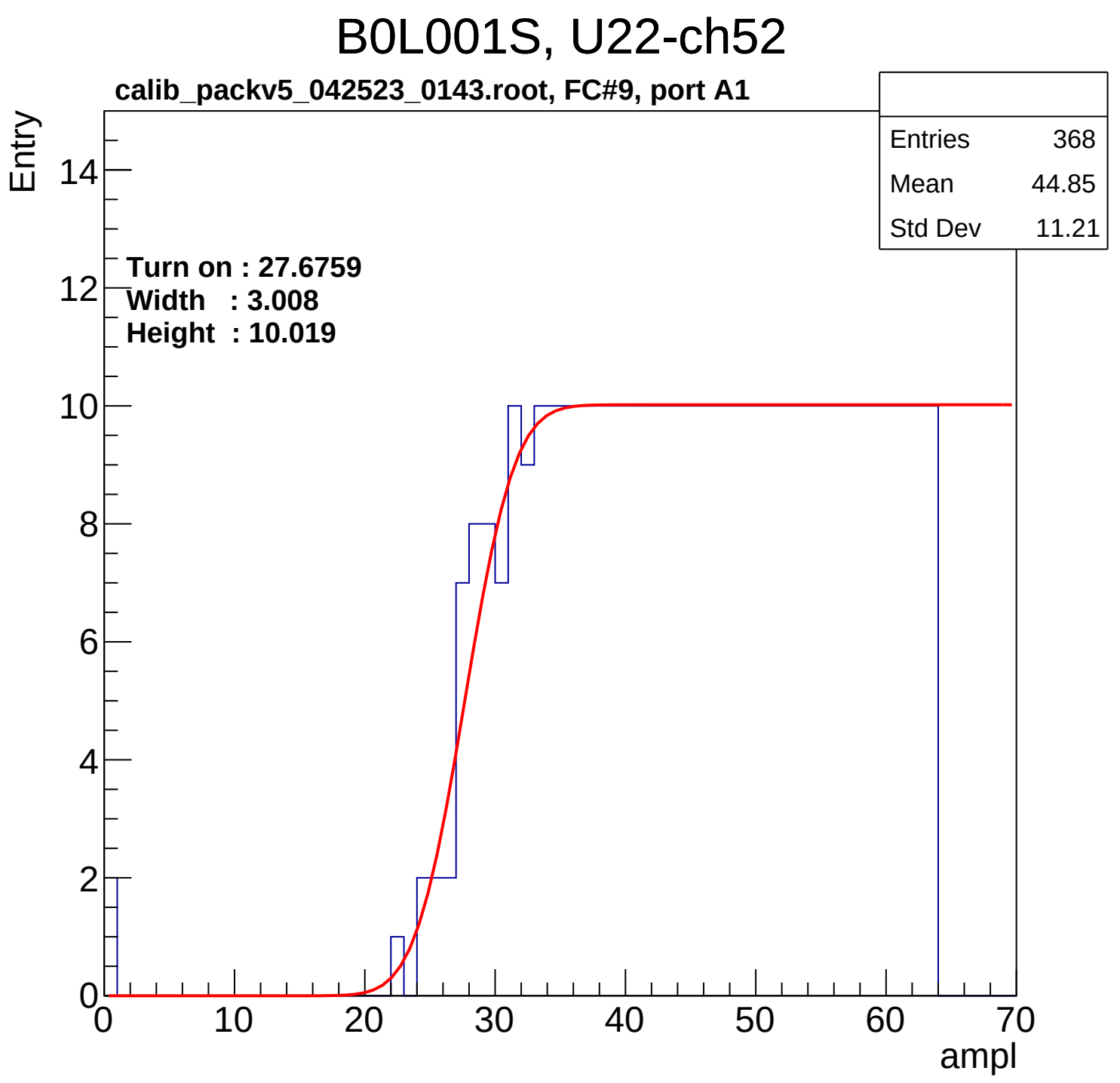
B0L001S, U22-ch52
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.85
Std Dev 11.21
Turn on : 27.6759
Width : 3.008
Height : 10.019
Entry
ampl
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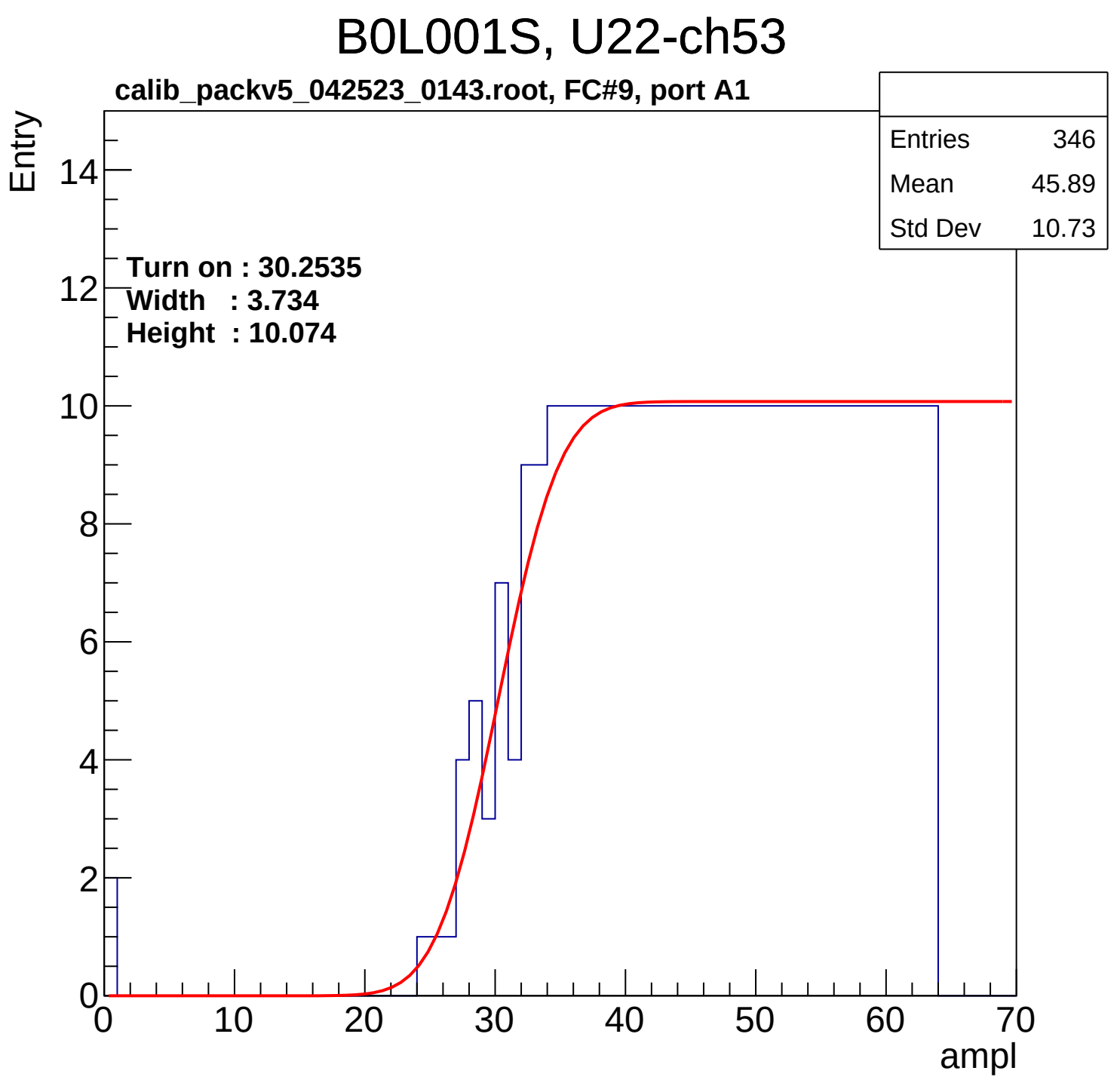
B0L001S, U22-ch53
calib_packv5_042523_0143.root, FC#9, port A1
Entries 346
Mean 45.89
Std Dev 10.73
Turn on : 30.2535
Width : 3.734
Height : 10.074
Entry
ampl
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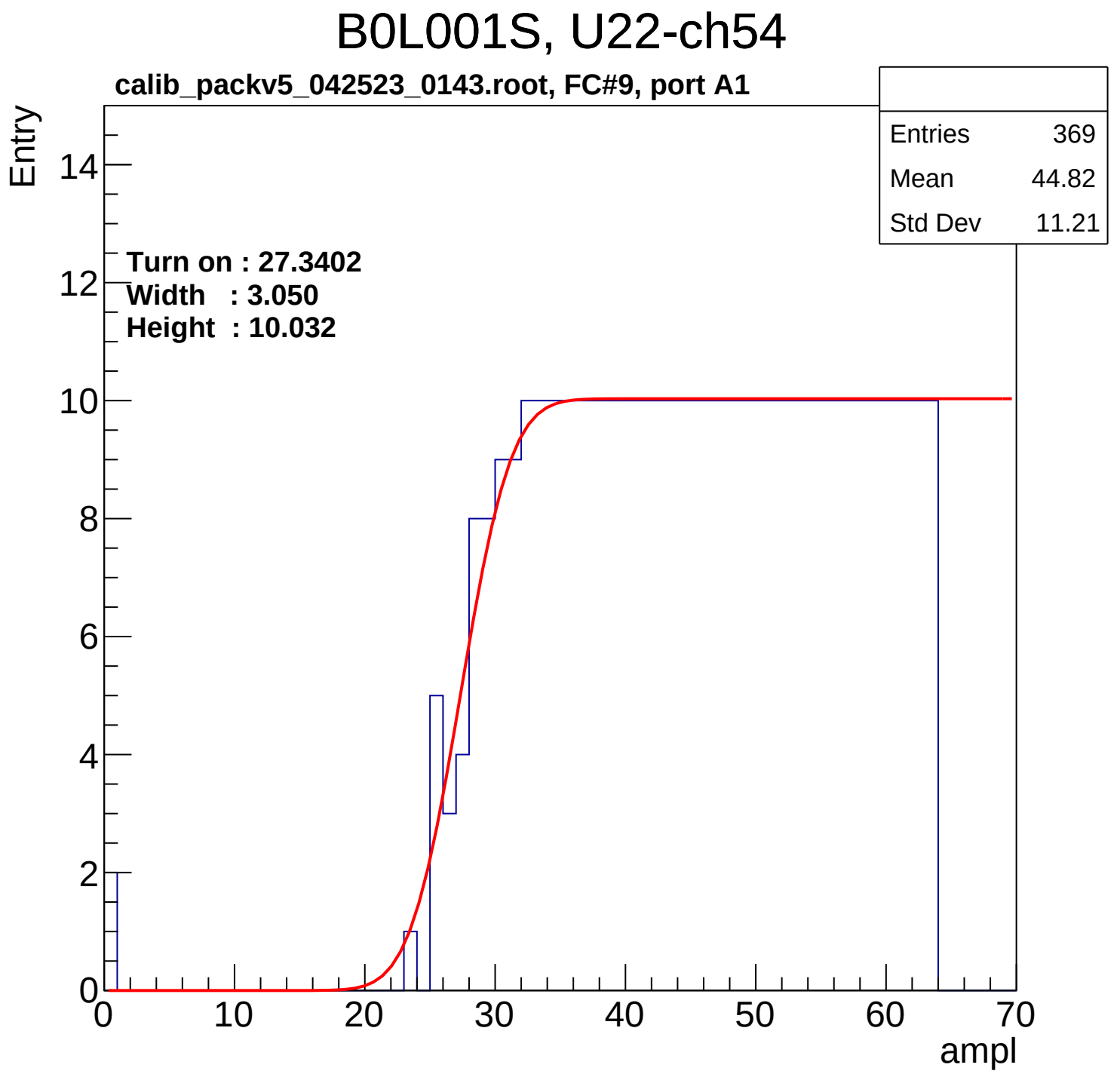
B0L001S, U22-ch54
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.82
Std Dev 11.21
Turn on : 27.3402
Width : 3.050
Height : 10.032
Entry
ampl
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6
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10
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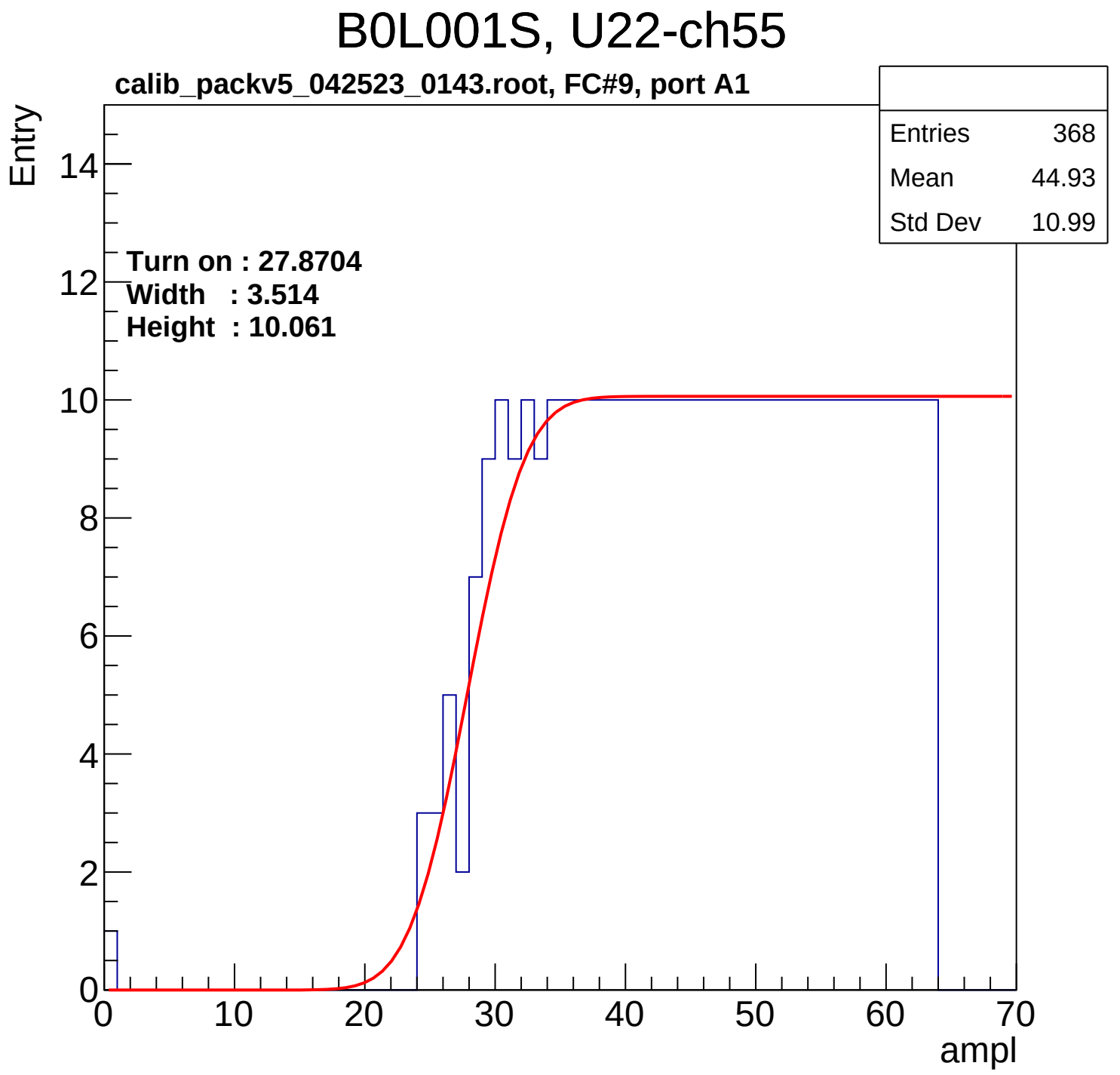
B0L001S, U22-ch55
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.93
Std Dev 10.99
Turn on : 27.8704
Width : 3.514
Height : 10.061
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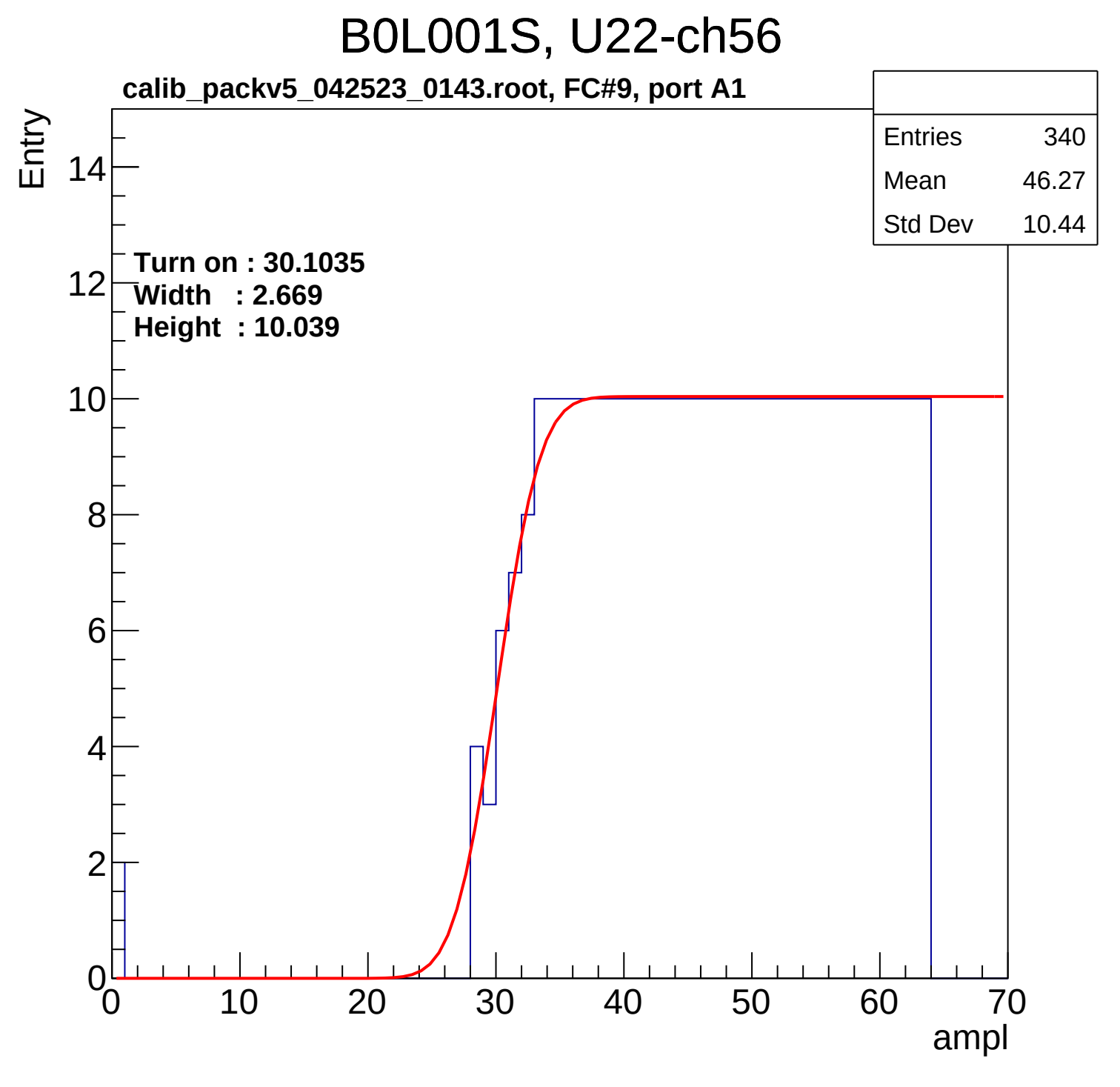
B0L001S, U22-ch56
calib_packv5_042523_0143.root, FC#9, port A1
Entries 340
Mean 46.27
Std Dev 10.44
Turn on : 30.1035
Width : 2.669
Height : 10.039
Entry
ampl
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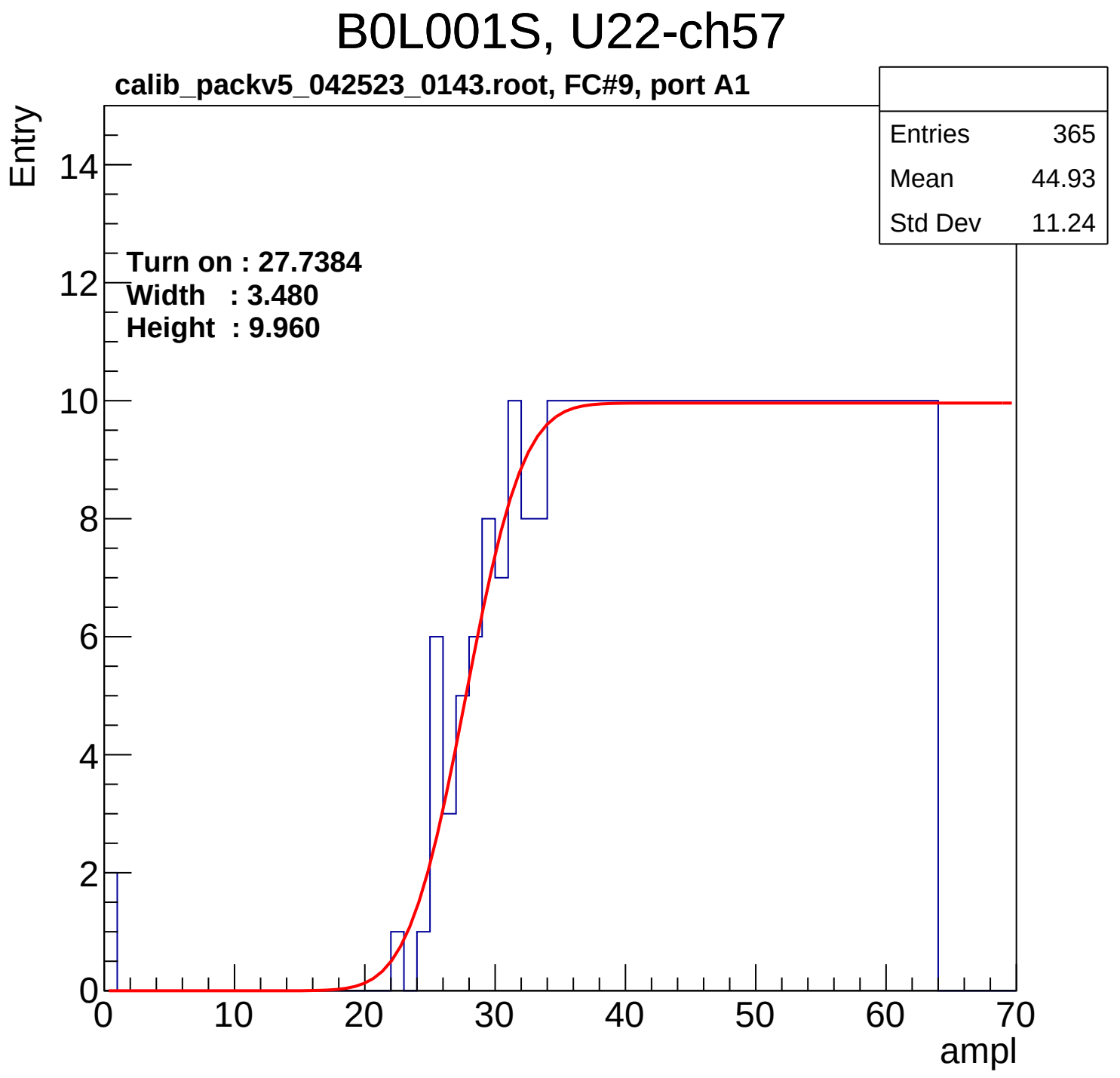
B0L001S, U22-ch57
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.93
Std Dev 11.24
Turn on : 27.7384
Width : 3.480
Height : 9.960
Entry
ampl
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6
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10
20
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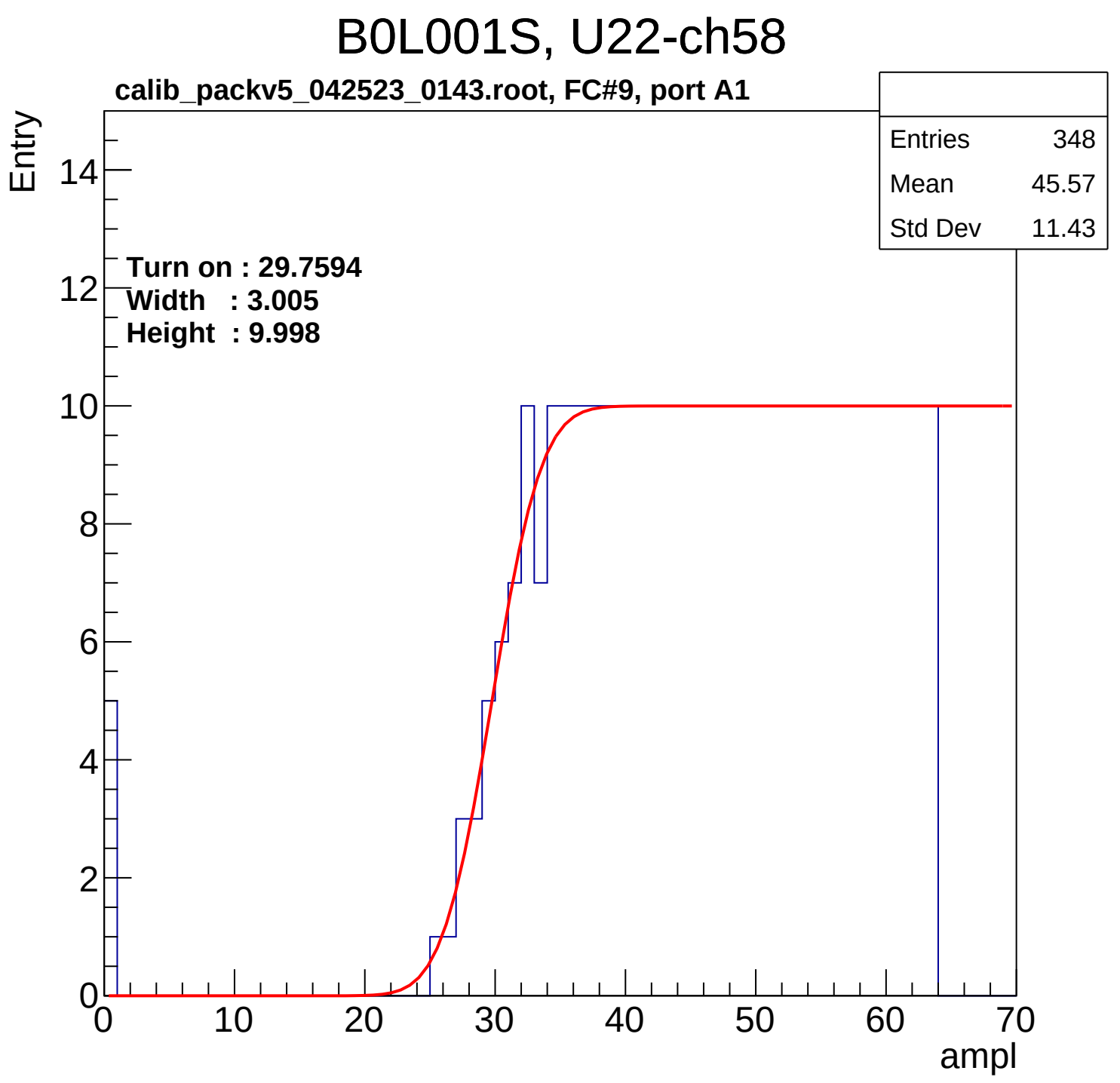
B0L001S, U22-ch58
calib_packv5_042523_0143.root, FC#9, port A1
Entries 348
Mean 45.57
Std Dev 11.43
Turn on : 29.7594
Width : 3.005
Height : 9.998
Entry
ampl
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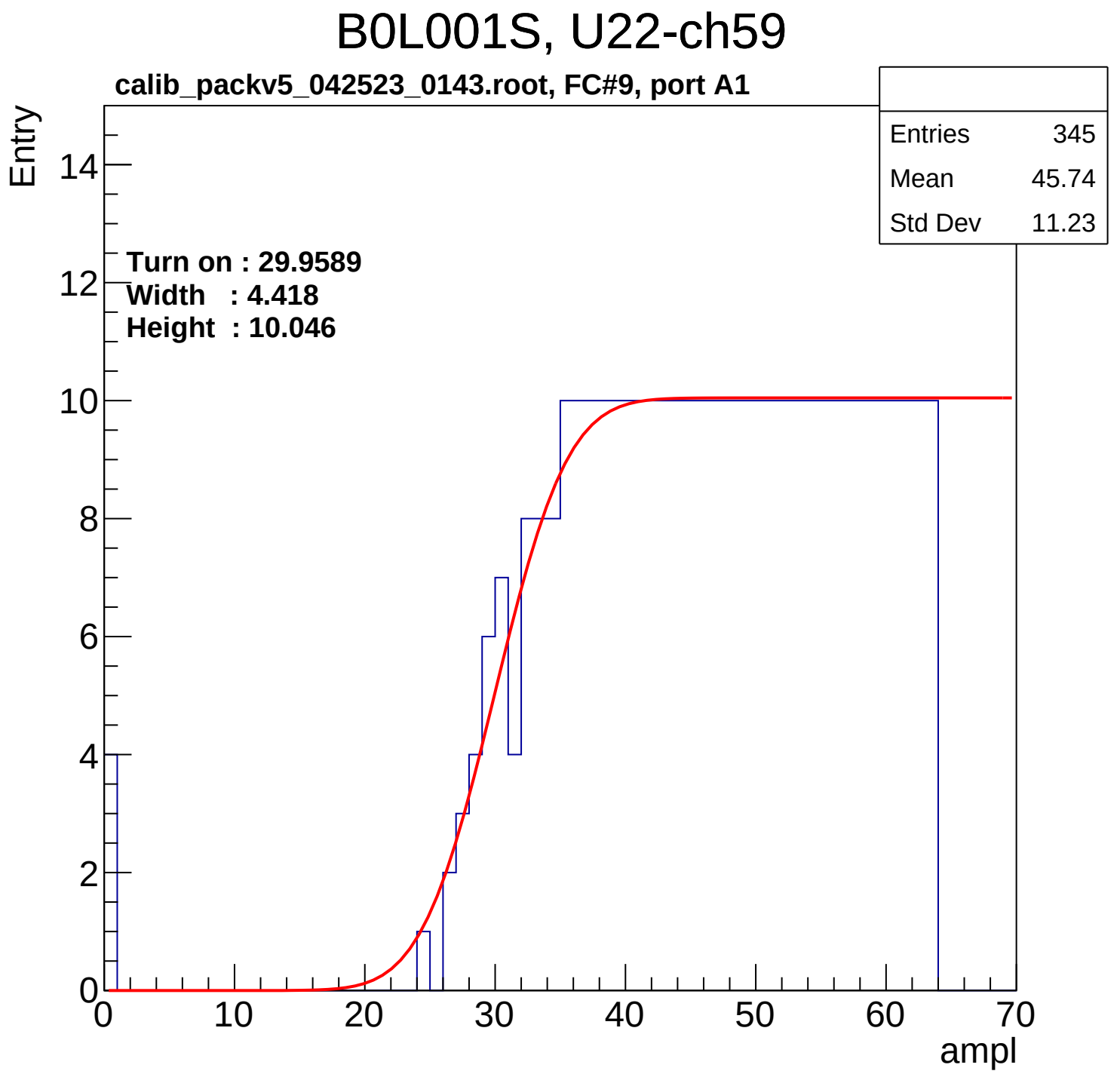
B0L001S, U22-ch59
calib_packv5_042523_0143.root, FC#9, port A1
Entries 345
Mean 45.74
Std Dev 11.23
Turn on : 29.9589
Width : 4.418
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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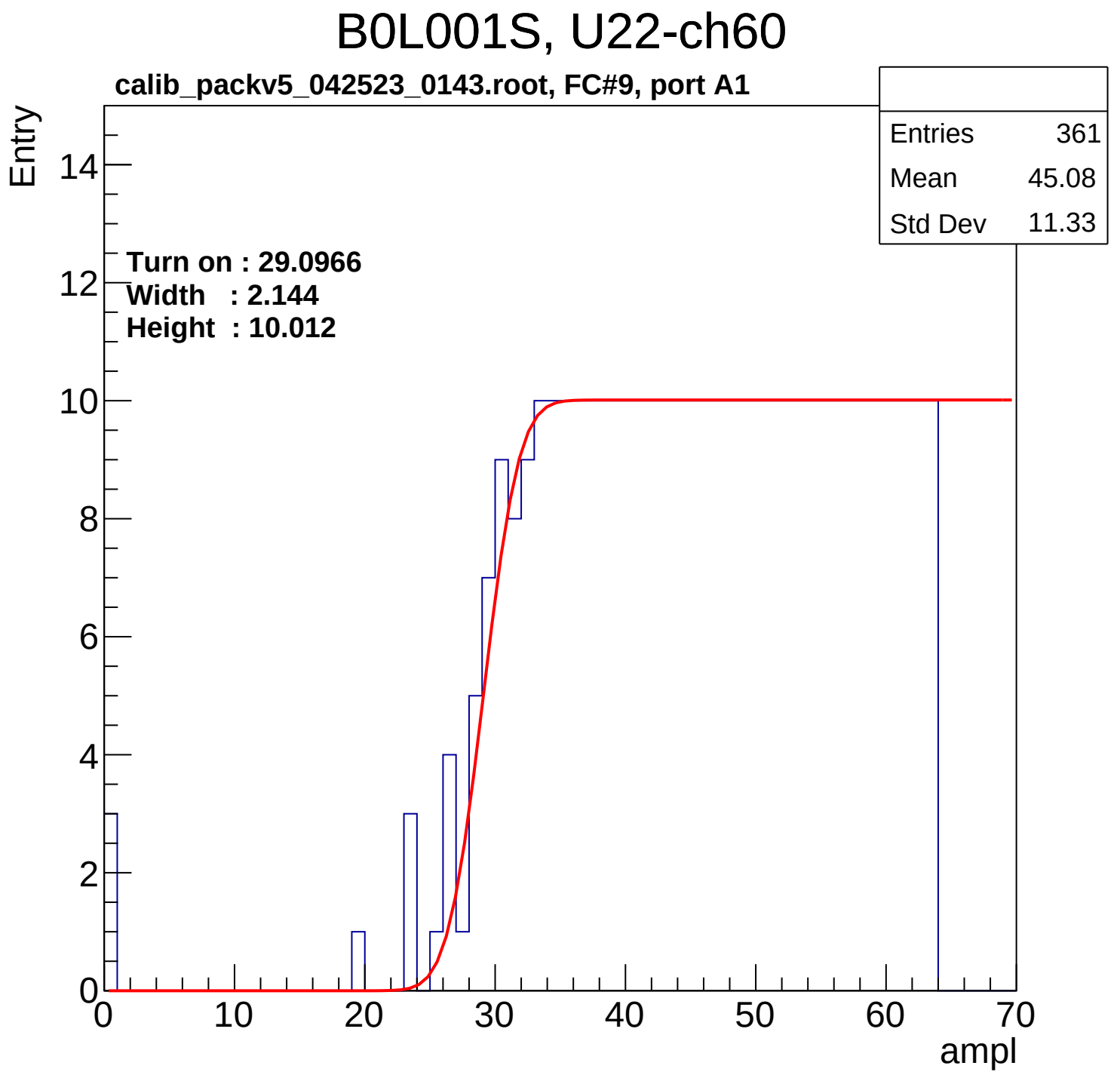
B0L001S, U22-ch60
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.08
Std Dev 11.33
Turn on : 29.0966
Width : 2.144
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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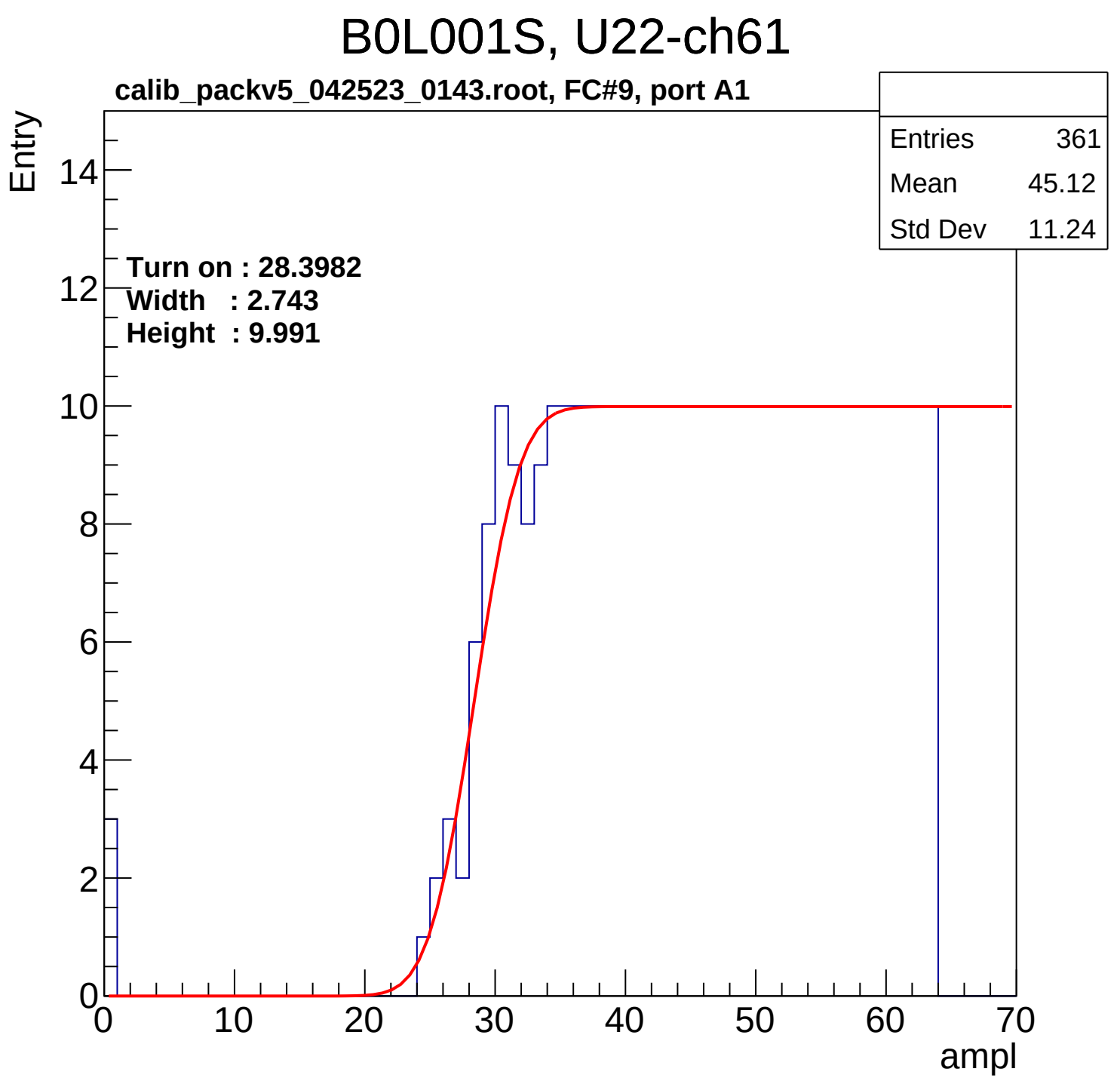
B0L001S, U22-ch61
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.12
Std Dev 11.24
Turn on : 28.3982
Width : 2.743
Height : 9.991
Entry
ampl
0
2
4
6
8
10
12
14
0
10
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60
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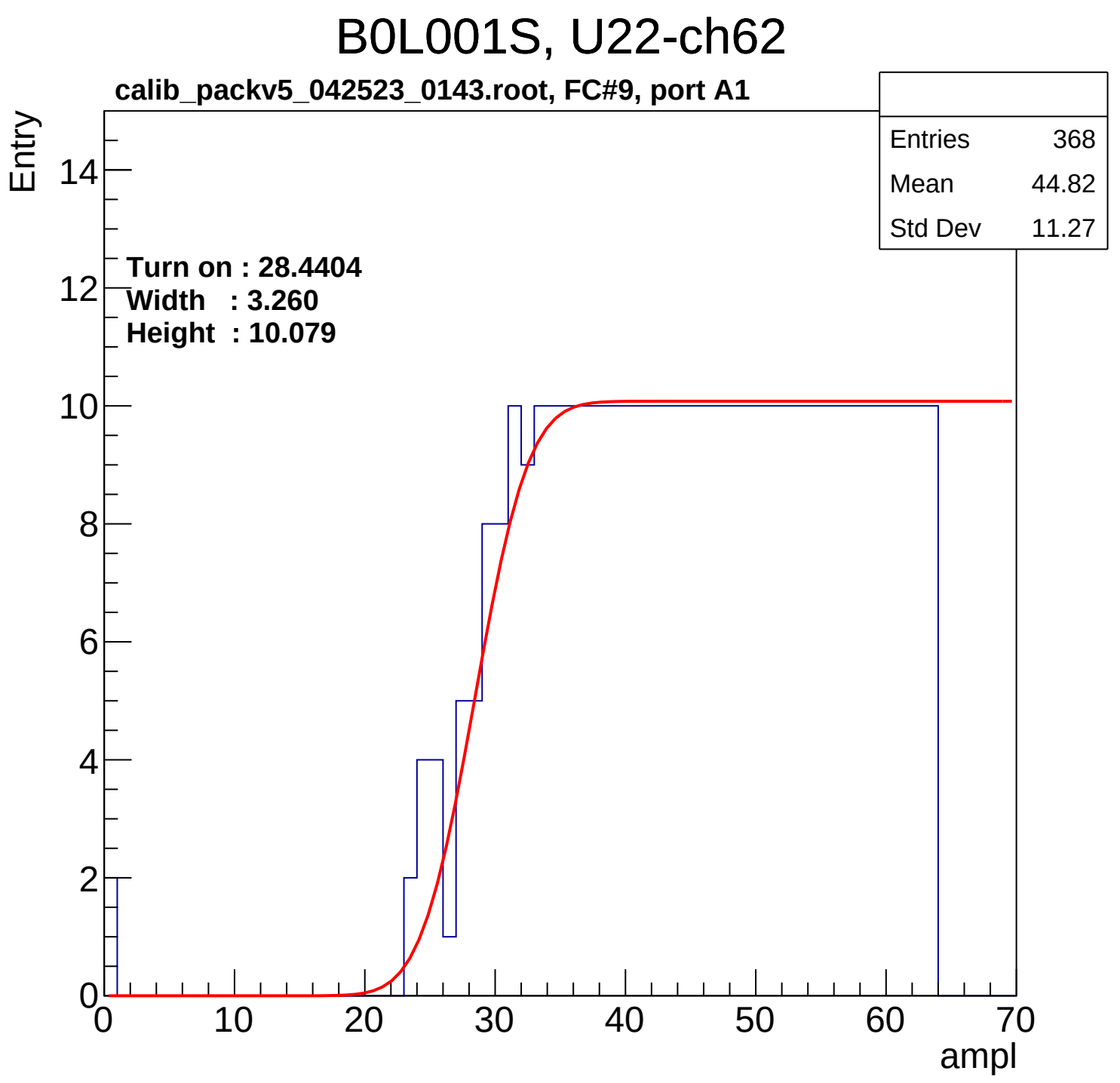
B0L001S, U22-ch62
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.82
Std Dev 11.27
Turn on : 28.4404
Width : 3.260
Height : 10.079
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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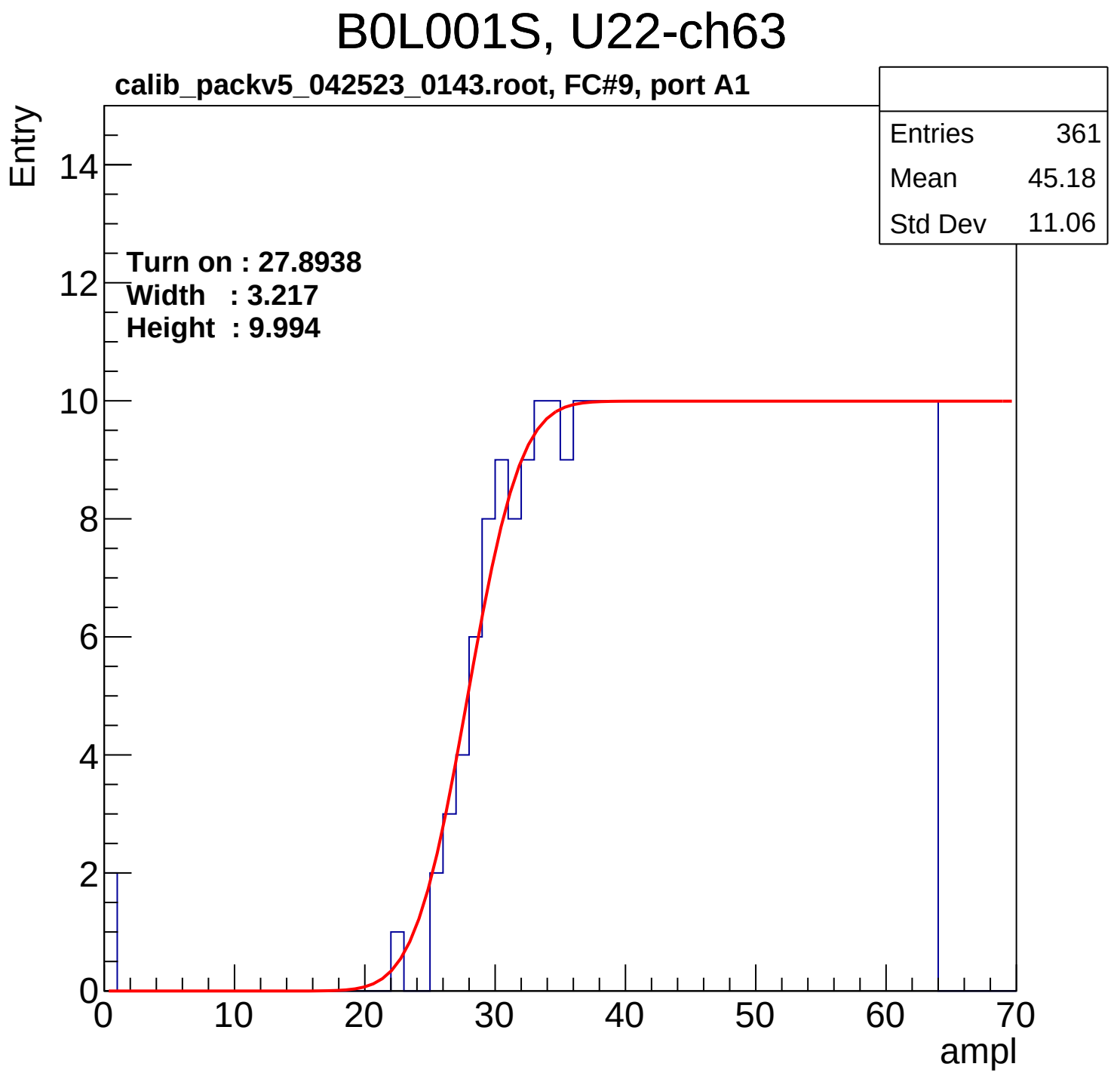
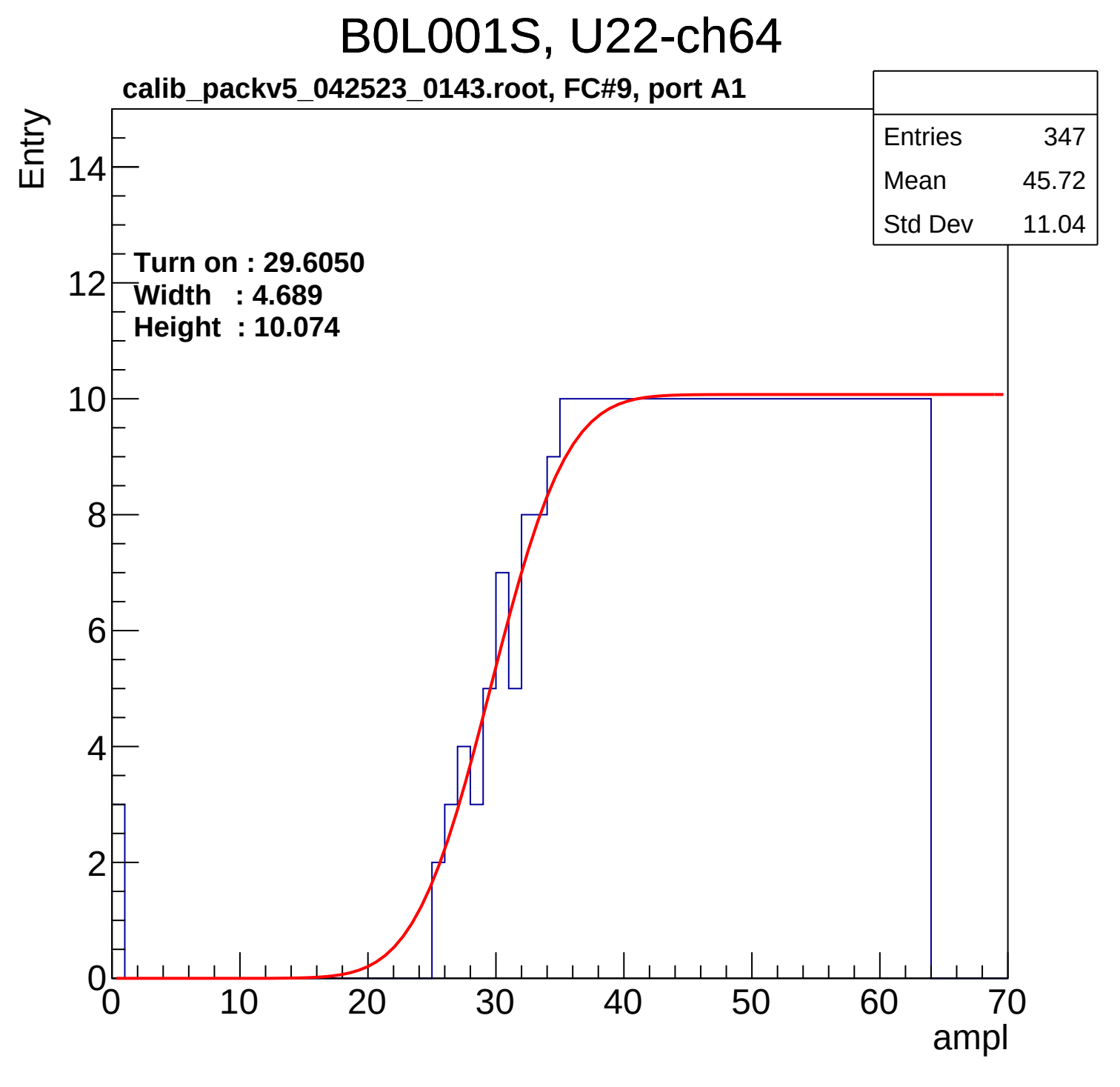

B0L001S, U22-ch63
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.18
Std Dev 11.06
Turn on : 27.8938
Width : 3.217
Height : 9.994
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U22-ch64
calib_packv5_042523_0143.root, FC#9, port A1
Entries 347
Mean 45.72
Std Dev 11.04
Turn on : 29.6050
Width : 4.689
Height : 10.074
Entry
ampl
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2
4
6
8
10
12
14
0
10
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60
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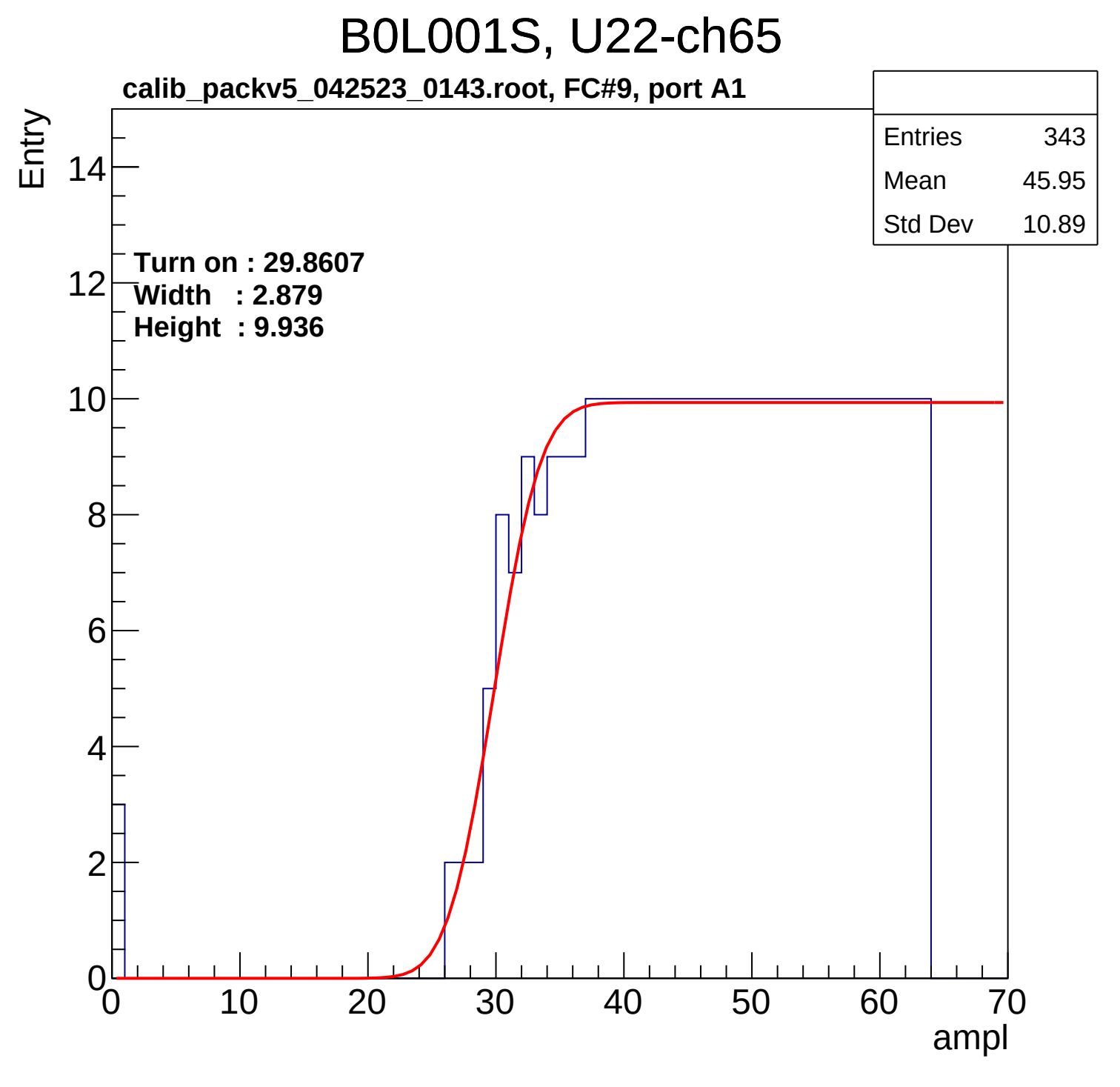
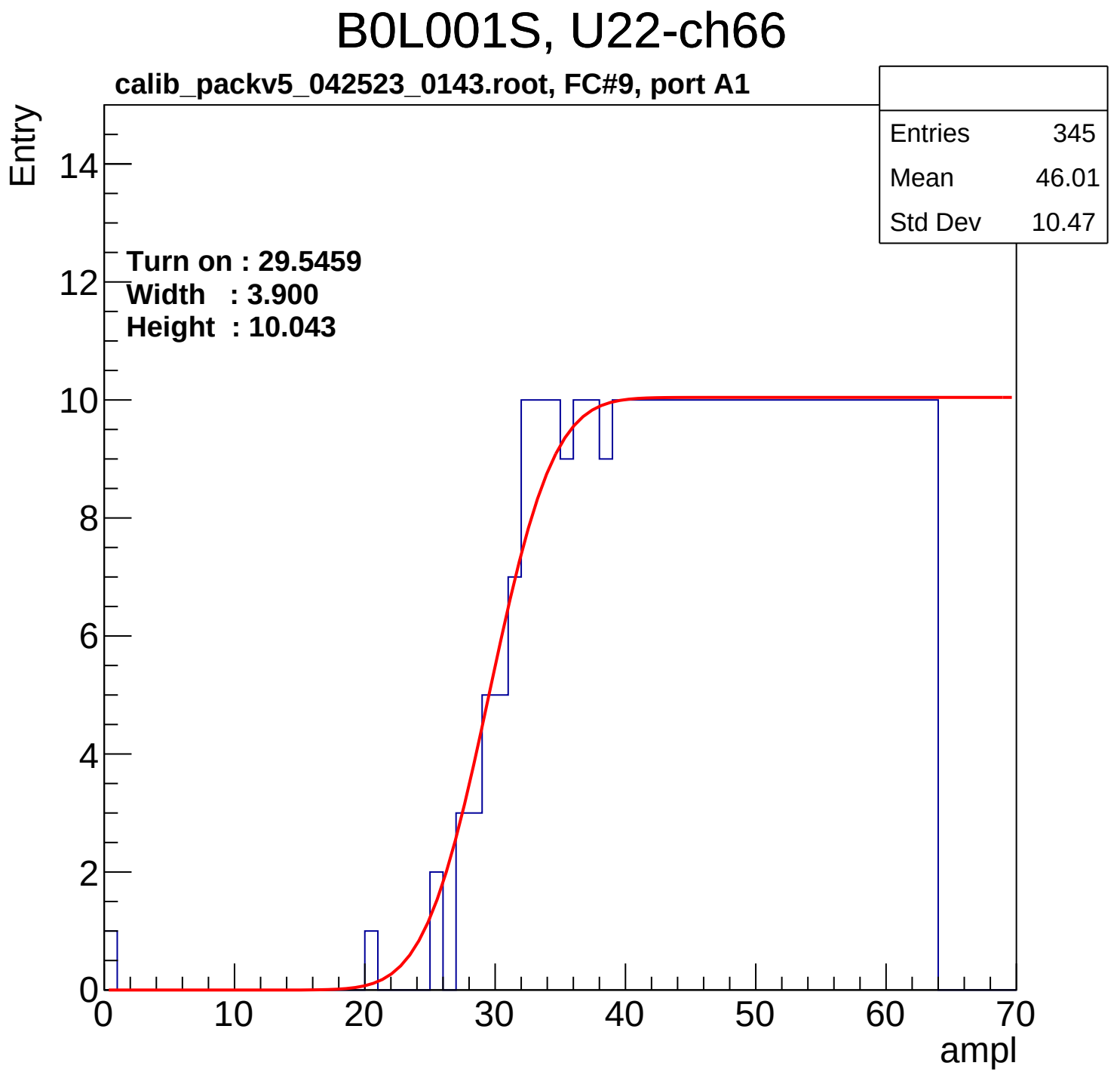

B0L001S, U22-ch65
calib_packv5_042523_0143.root, FC#9, port A1
Entries 343
Mean 45.95
Std Dev 10.89
Turn on : 29.8607
Width : 2.879
Height : 9.936
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U22-ch66
calib_packv5_042523_0143.root, FC#9, port A1
Entries 345
Mean 46.01
Std Dev 10.47
Turn on : 29.5459
Width : 3.900
Height : 10.043
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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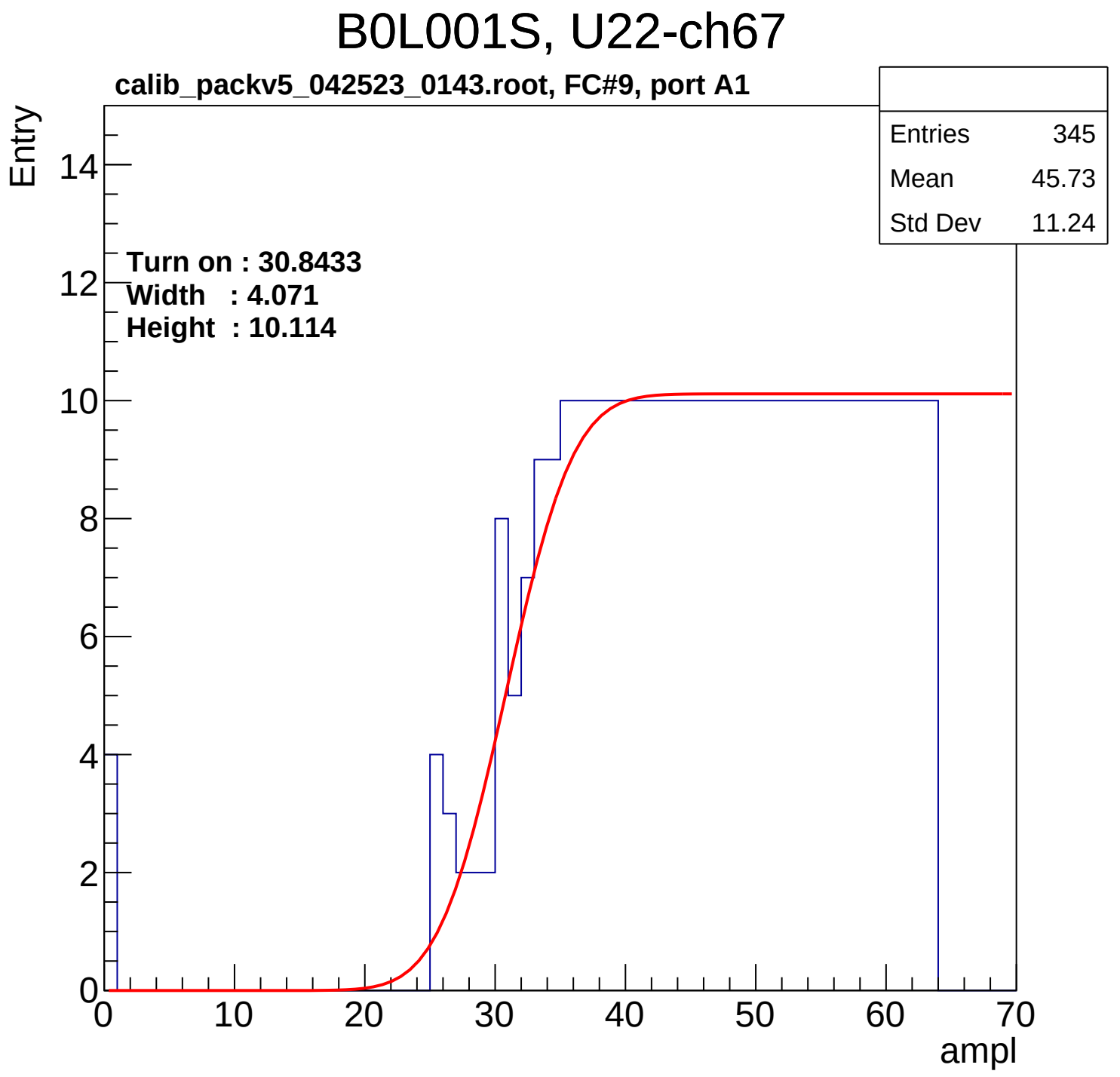
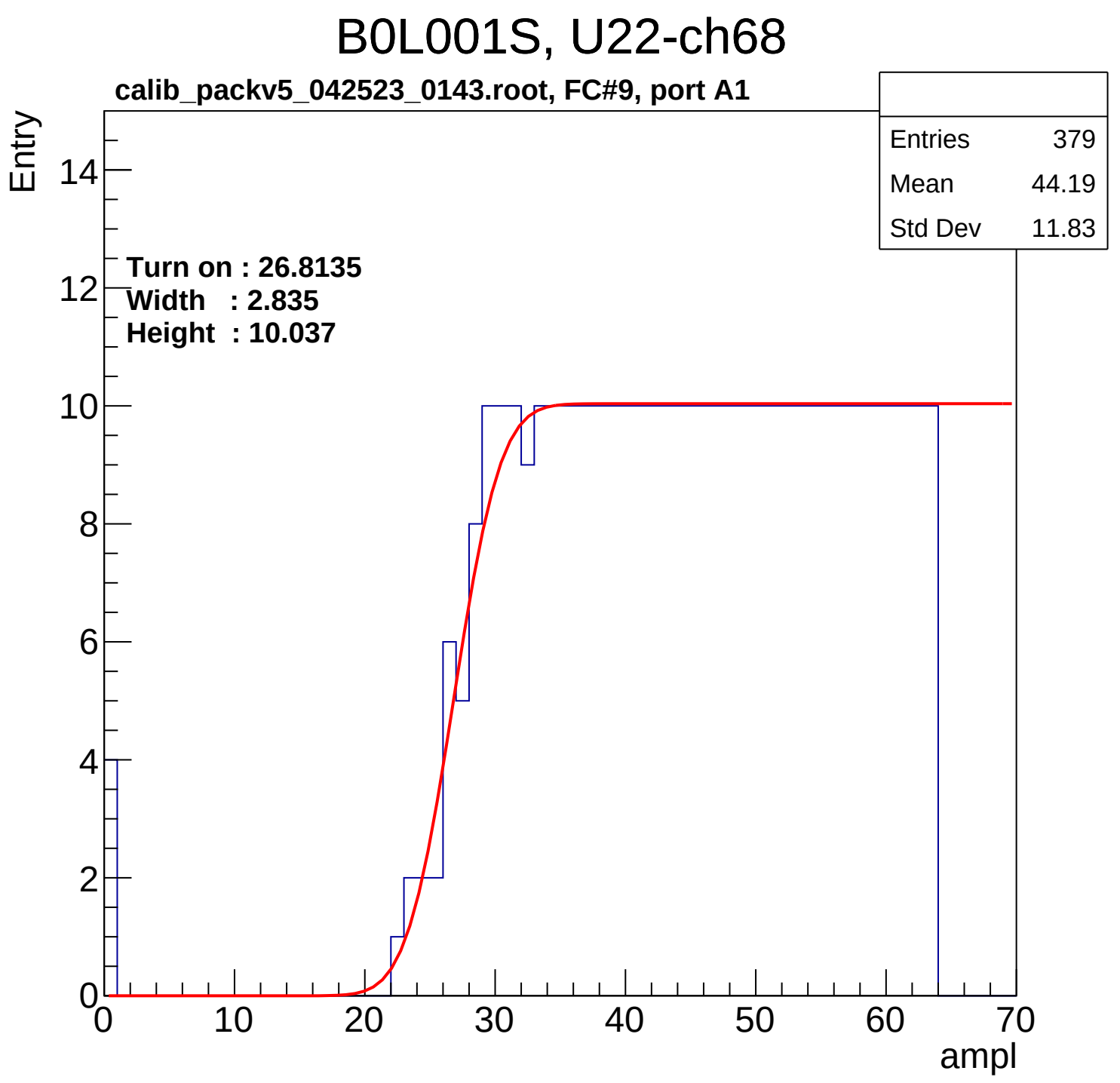

B0L001S, U22-ch67
calib_packv5_042523_0143.root, FC#9, port A1
Entries 345
Mean 45.73
Std Dev 11.24
Turn on : 30.8433
Width : 4.071
Height : 10.114
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U22-ch68
calib_packv5_042523_0143.root, FC#9, port A1
Entries 379
Mean 44.19
Std Dev 11.83
Turn on : 26.8135
Width : 2.835
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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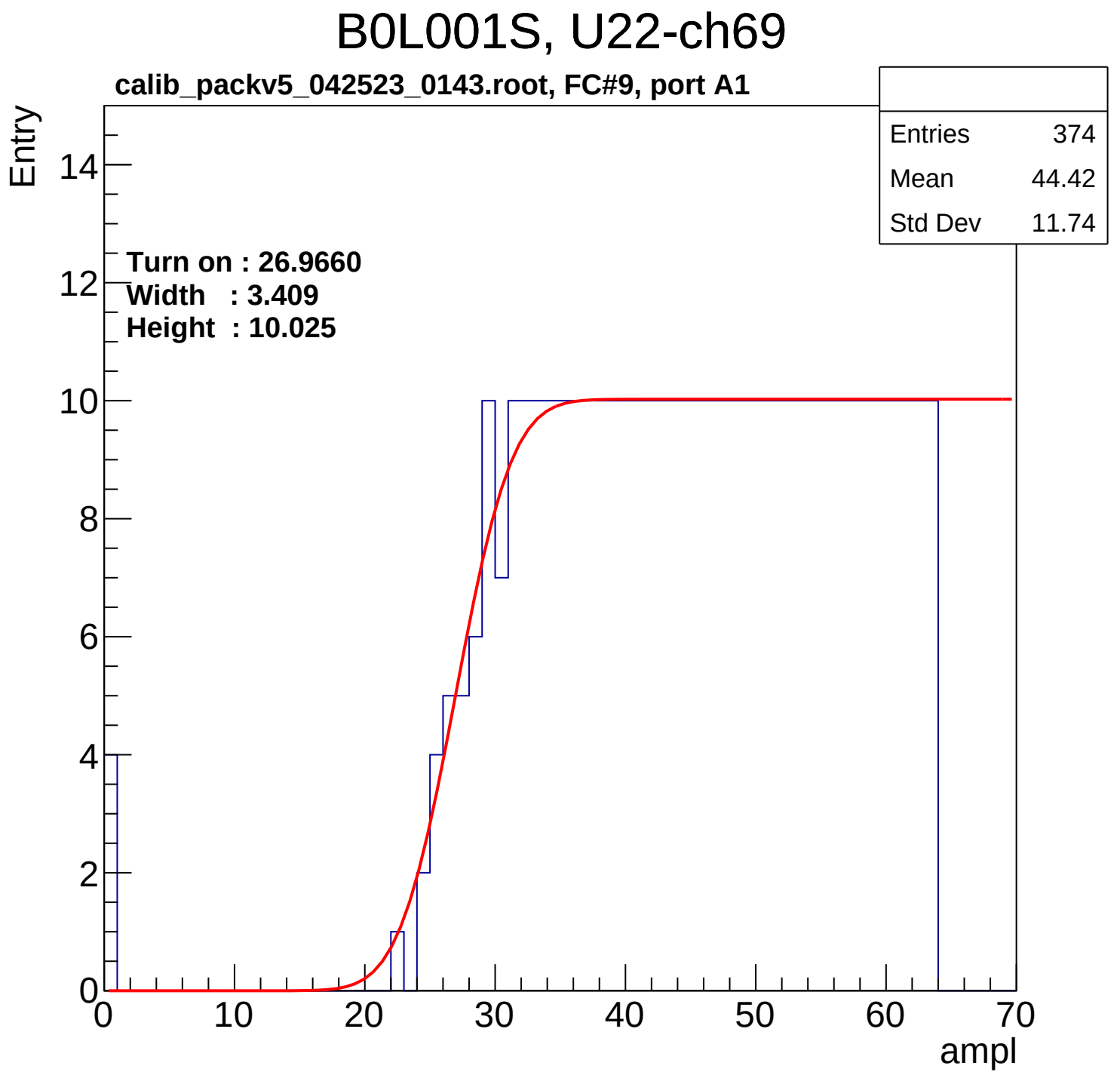
40
50
60
70


B0L001S, U22-ch69
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.42
Std Dev 11.74
Turn on : 26.9660
Width : 3.409
Height : 10.025
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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60
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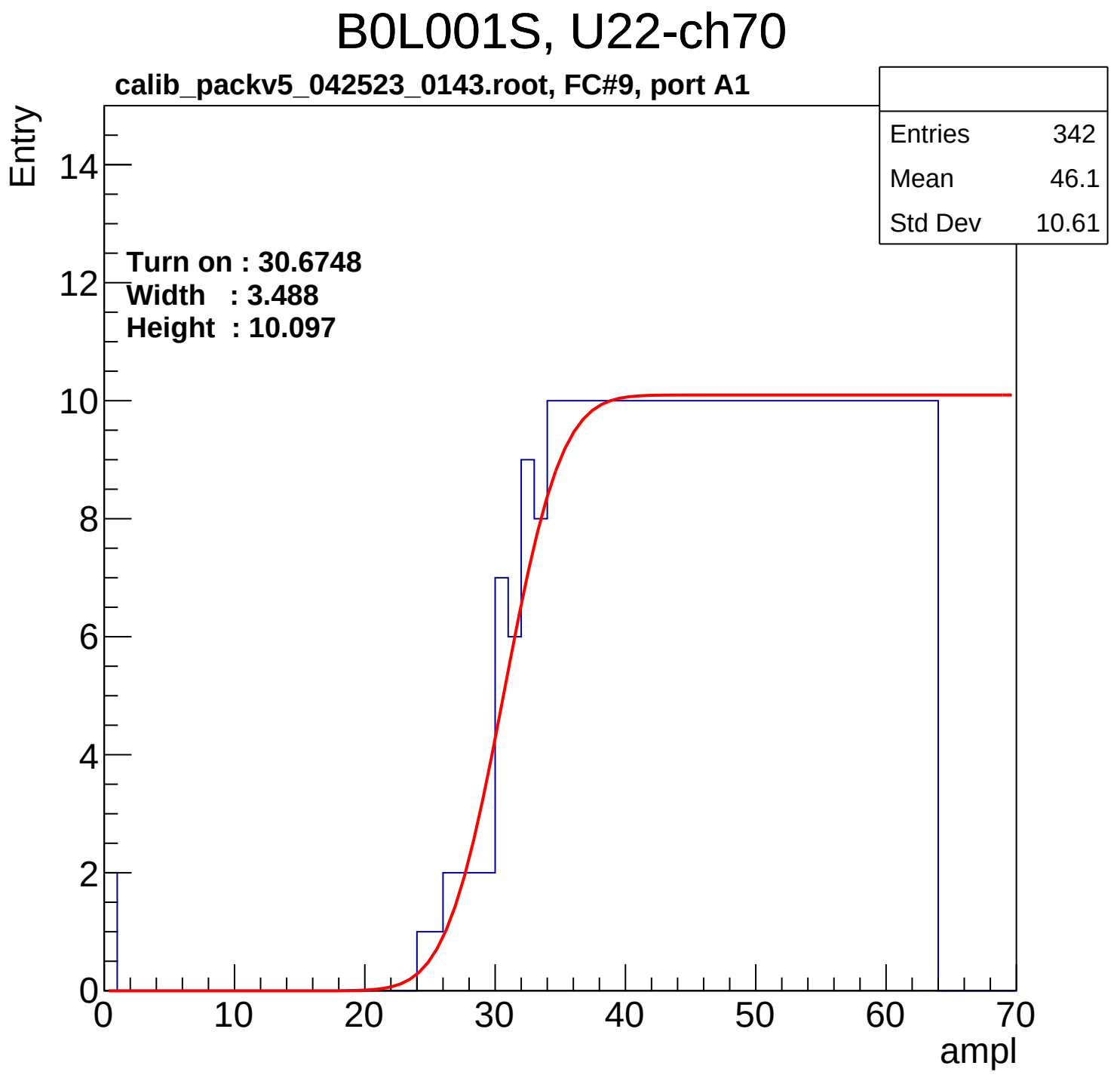
B0L001S, U22-ch70
calib_packv5_042523_0143.root, FC#9, port A1
Entries 342
Mean 46.1
Std Dev 10.61
Turn on : 30.6748
Width : 3.488
Height : 10.097
Entry
ampl
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2
4
6
8
10
12
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0
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20
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60
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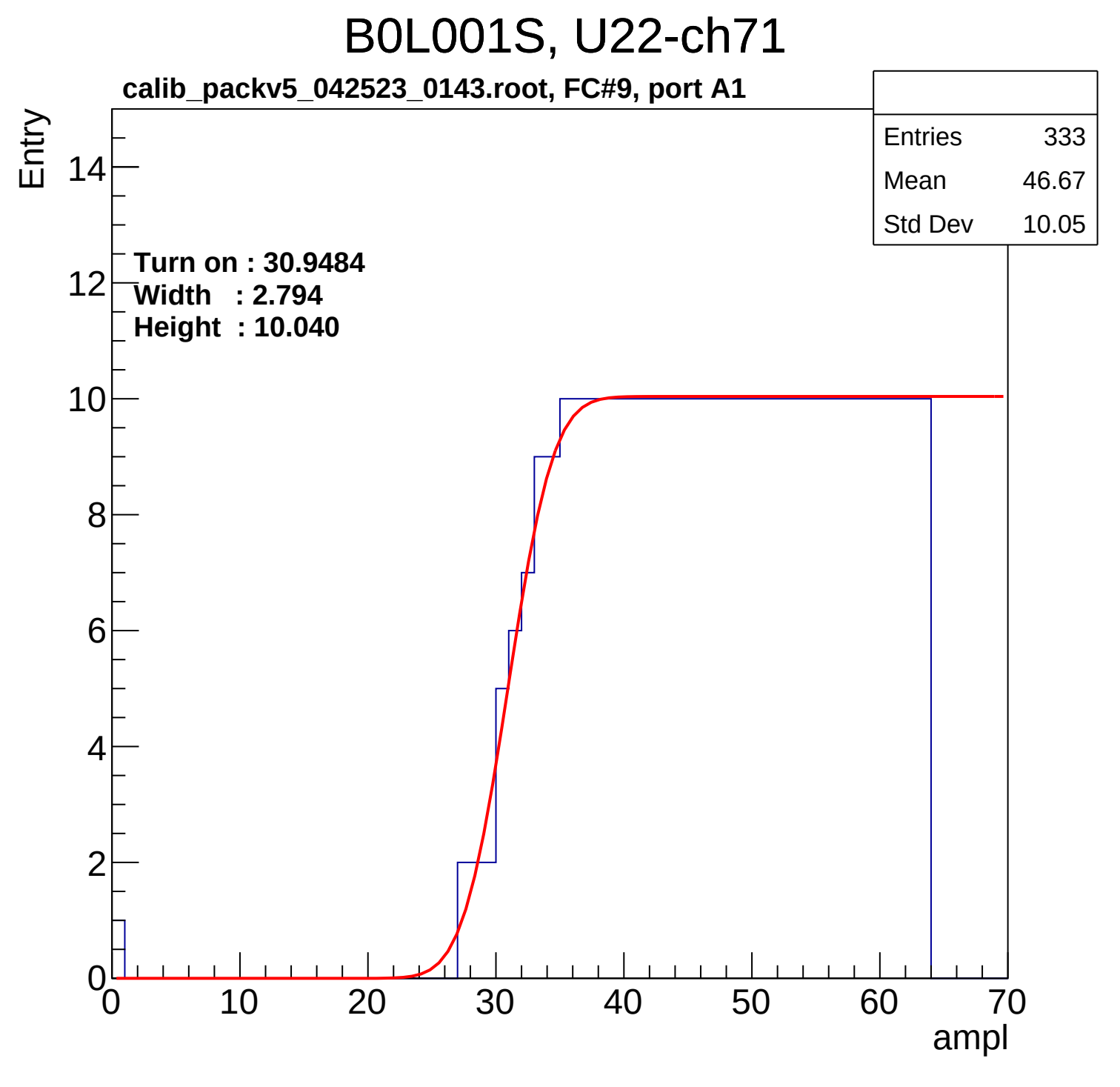
B0L001S, U22-ch71
calib_packv5_042523_0143.root, FC#9, port A1
Entries 333
Mean 46.67
Std Dev 10.05
Turn on : 30.9484
Width : 2.794
Height : 10.040
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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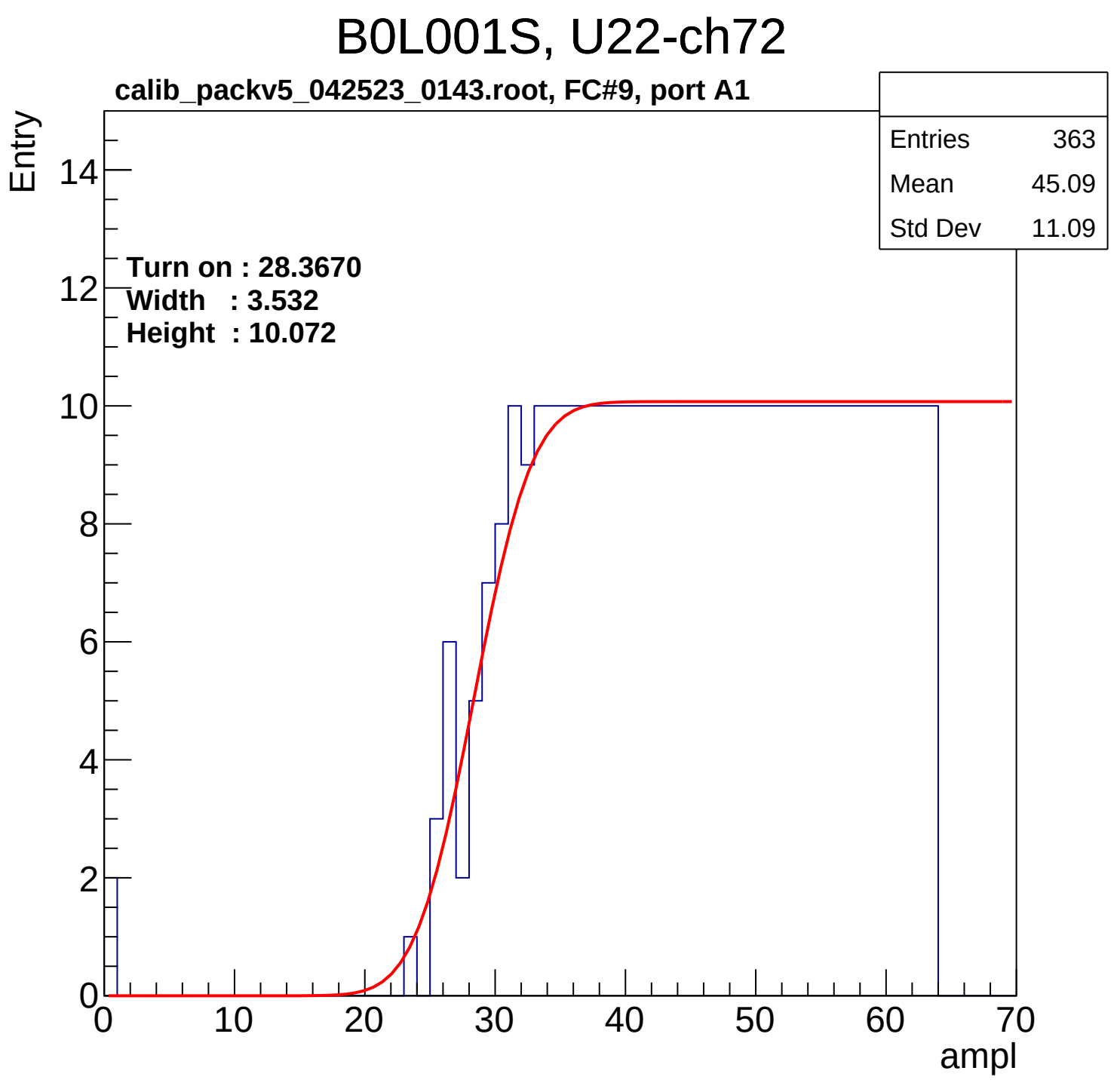
B0L001S, U22-ch72
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.09
Std Dev 11.09
Turn on : 28.3670
Width : 3.532
Height : 10.072
Entry
ampl
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2
4
6
8
10
12
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0
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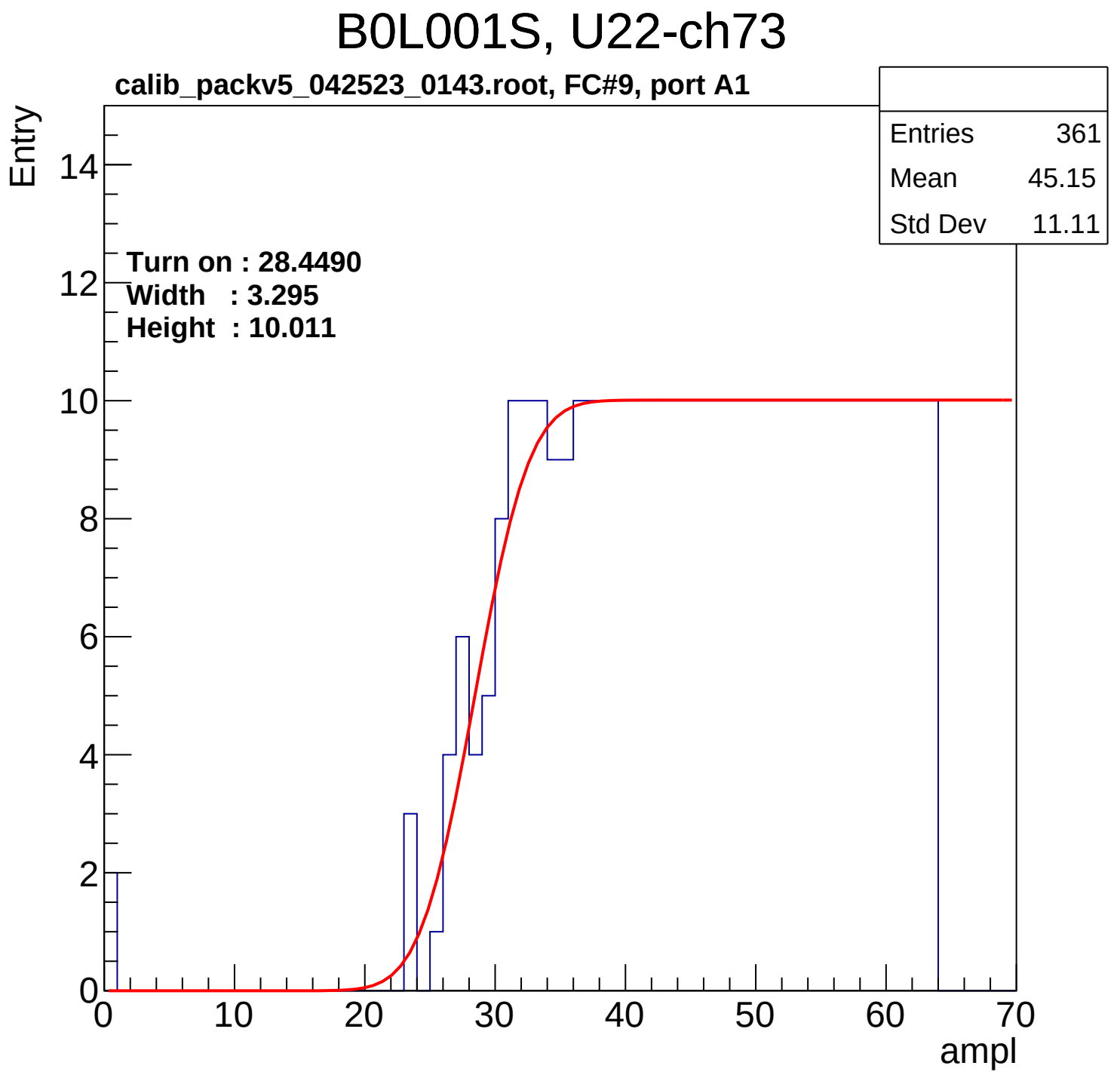
B0L001S, U22-ch73
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.15
Std Dev 11.11
Turn on : 28.4490
Width : 3.295
Height : 10.011
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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60
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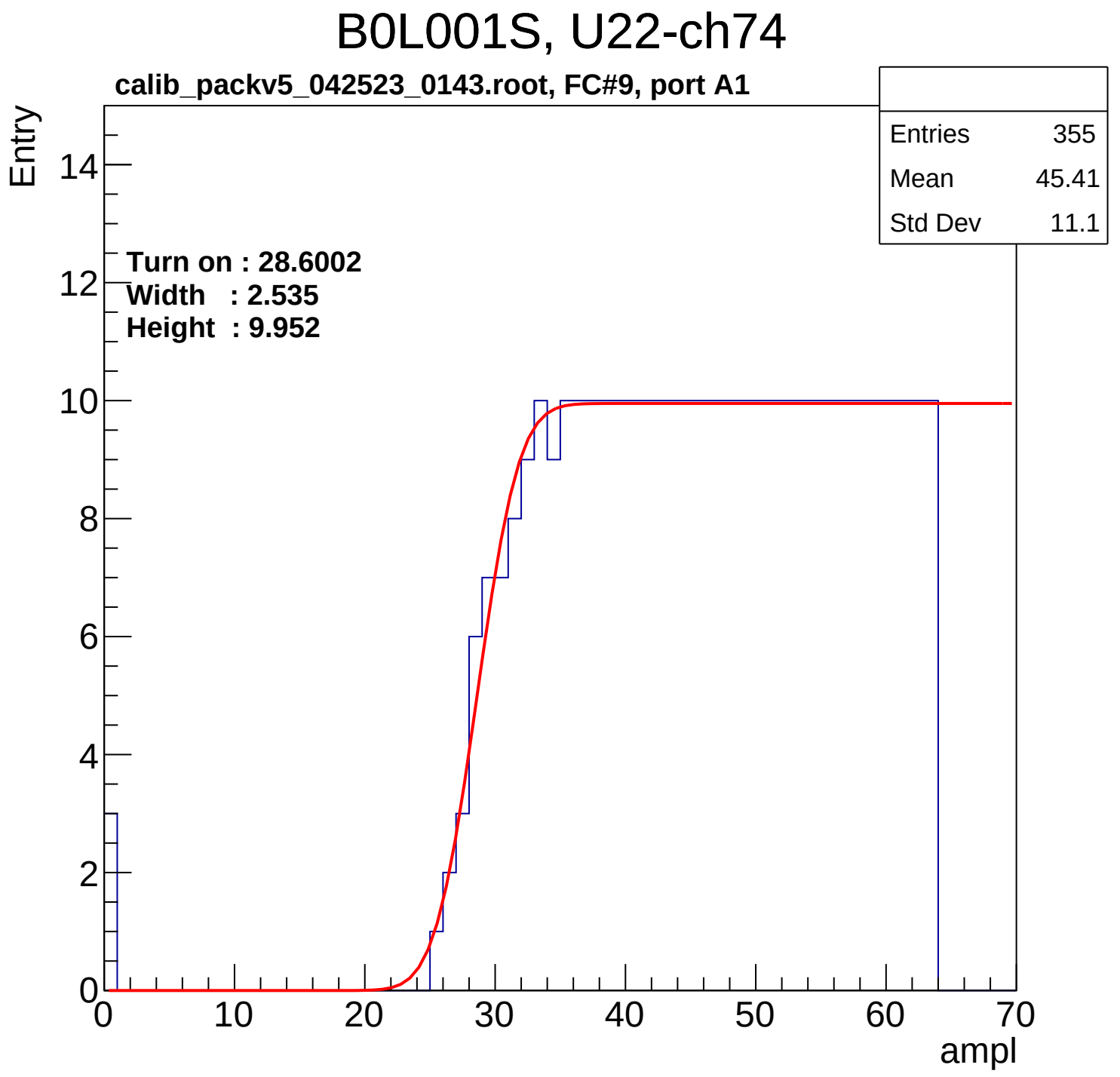
B0L001S, U22-ch74
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.41
Std Dev 11.1
Turn on : 28.6002
Width : 2.535
Height : 9.952
Entry
ampl
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2
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6
8
10
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0
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20
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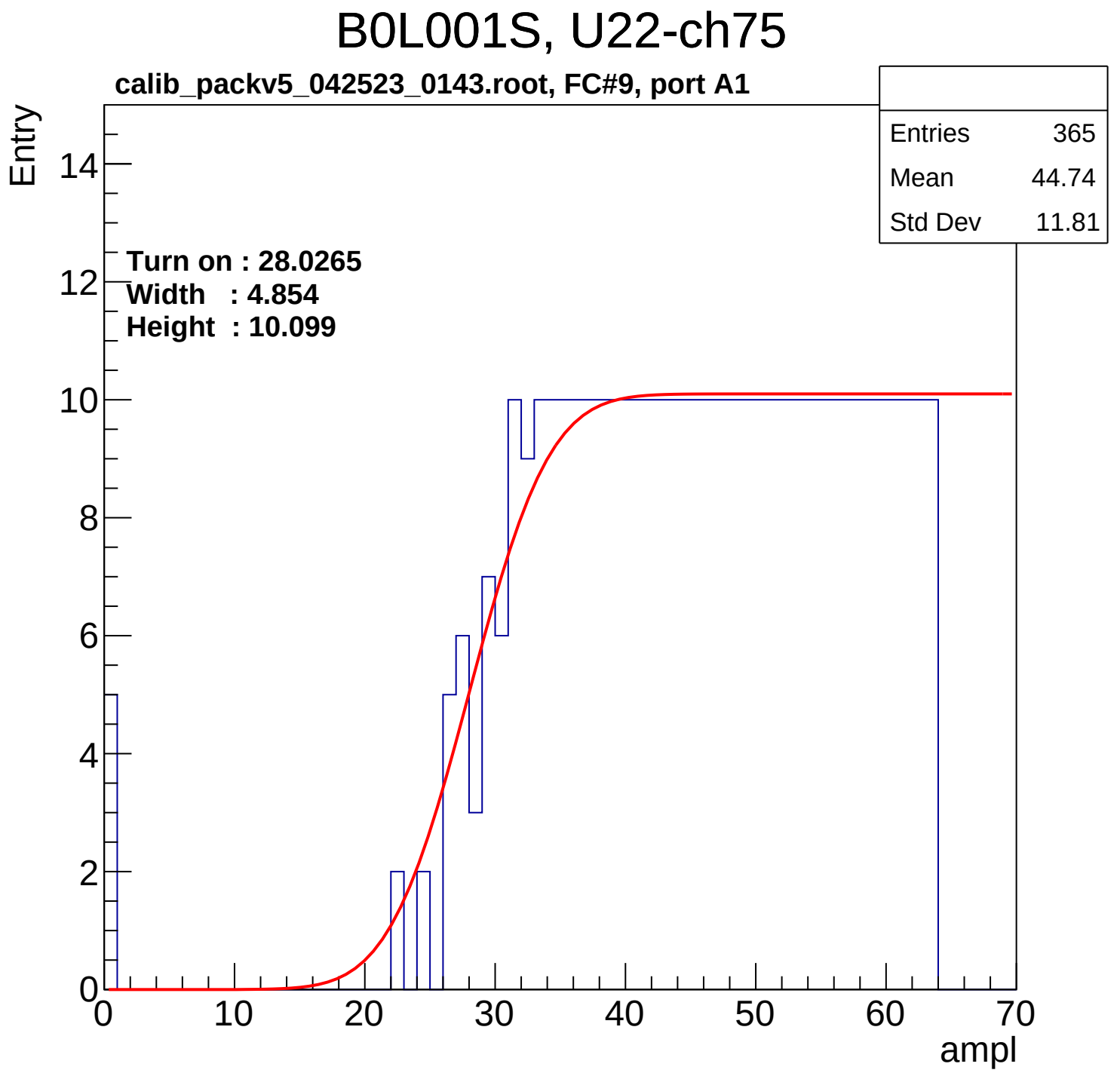
B0L001S, U22-ch75
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.74
Std Dev 11.81
Turn on : 28.0265
Width : 4.854
Height : 10.099
Entry
ampl
0
2
4
6
8
10
12
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0
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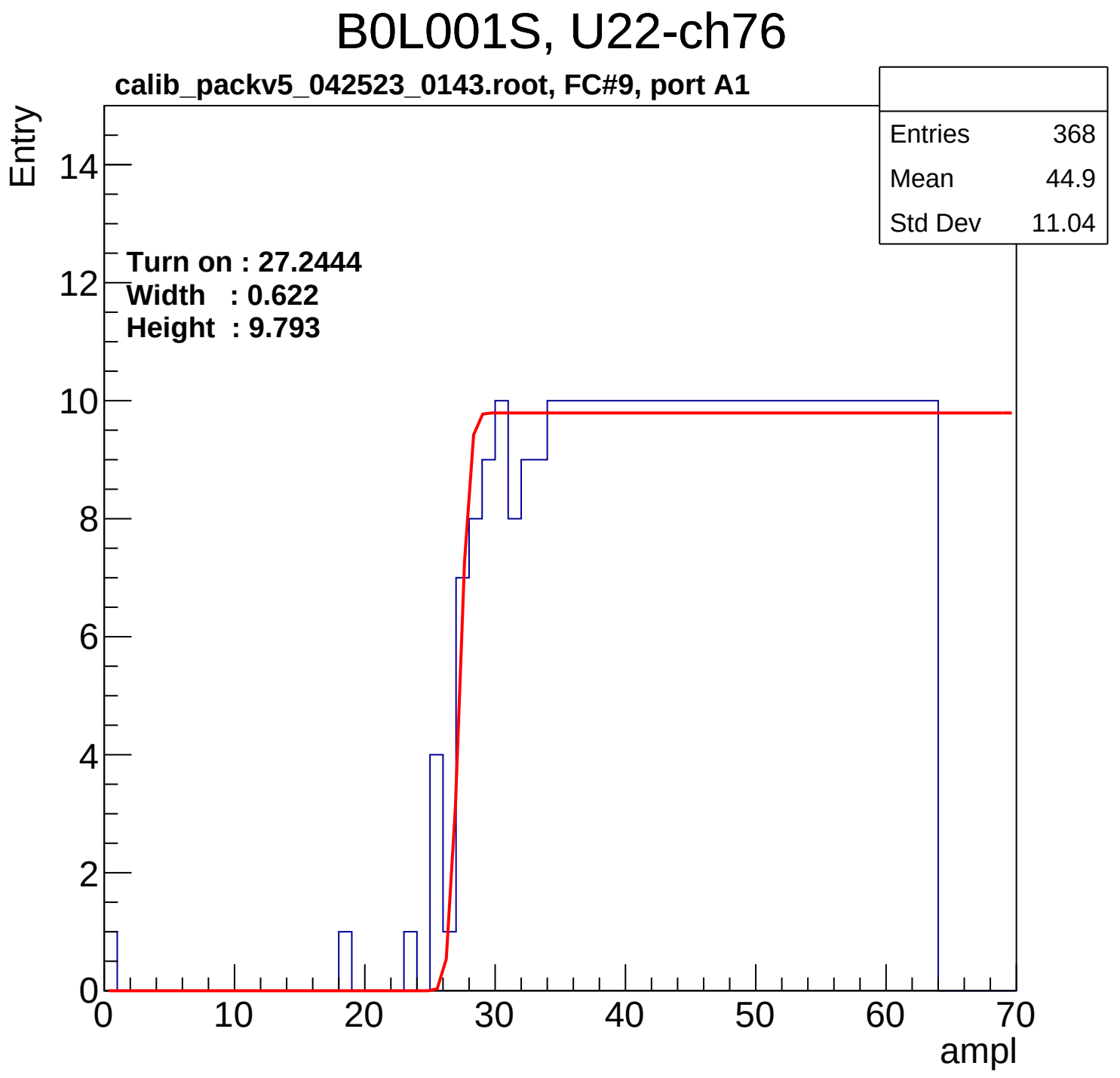
B0L001S, U22-ch76
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.9
Std Dev 11.04
Turn on : 27.2444
Width : 0.622
Height : 9.793
Entry
ampl
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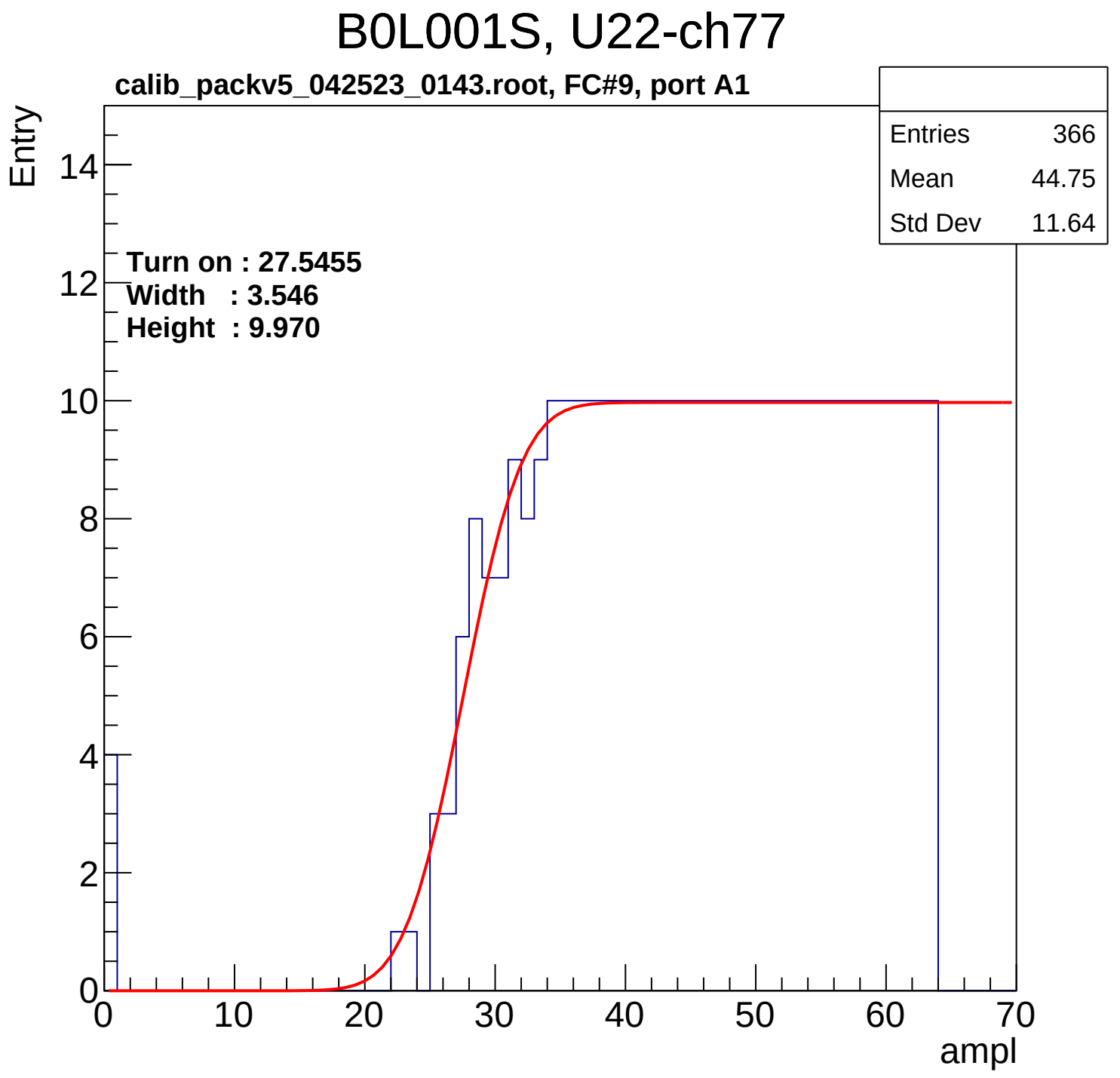
B0L001S, U22-ch77
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.75
Std Dev 11.64
Turn on : 27.5455
Width : 3.546
Height : 9.970
Entry
ampl
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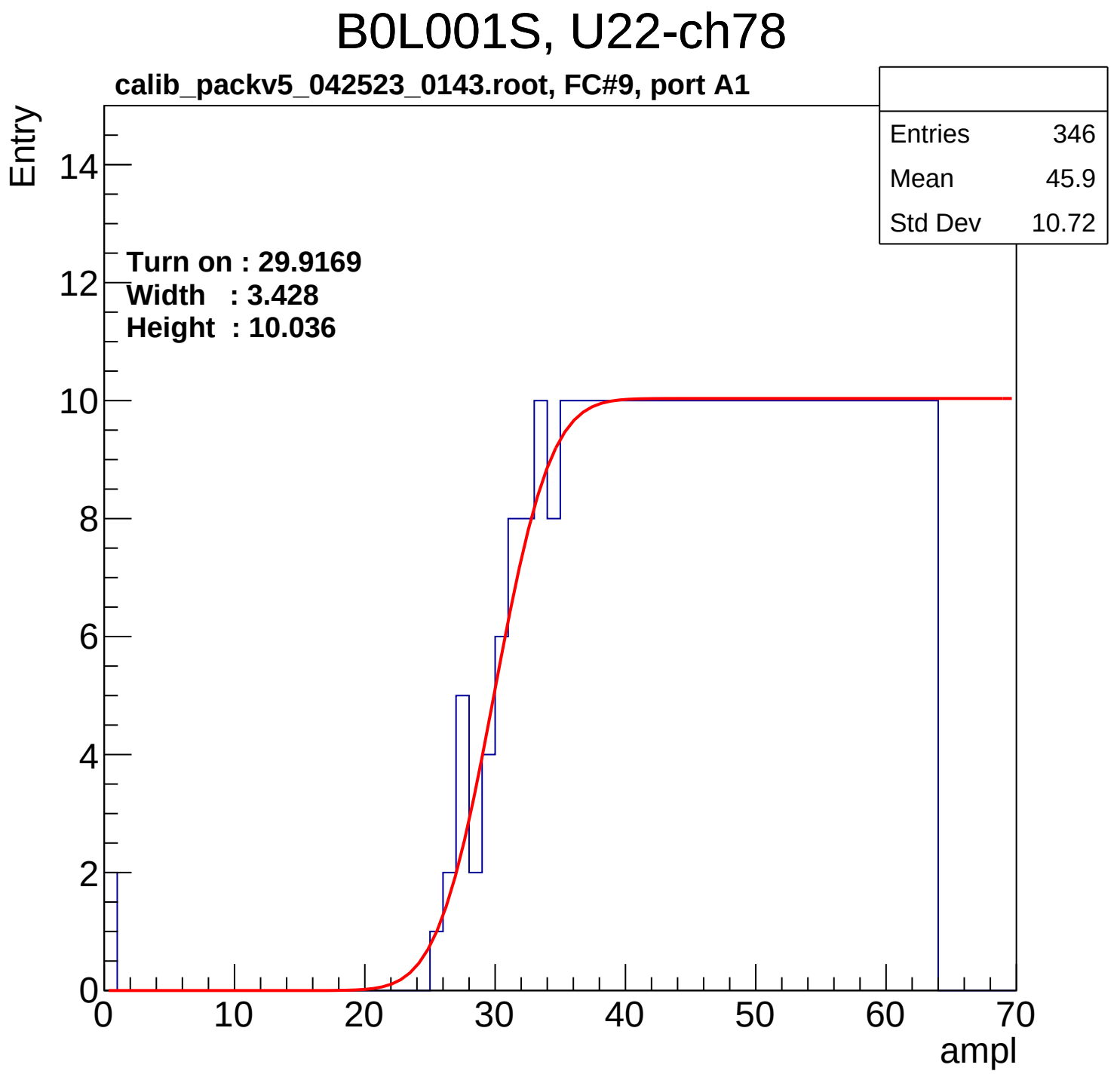
B0L001S, U22-ch78
calib_packv5_042523_0143.root, FC#9, port A1
Entries 346
Mean 45.9
Std Dev 10.72
Turn on : 29.9169
Width : 3.428
Height : 10.036
Entry
ampl
0
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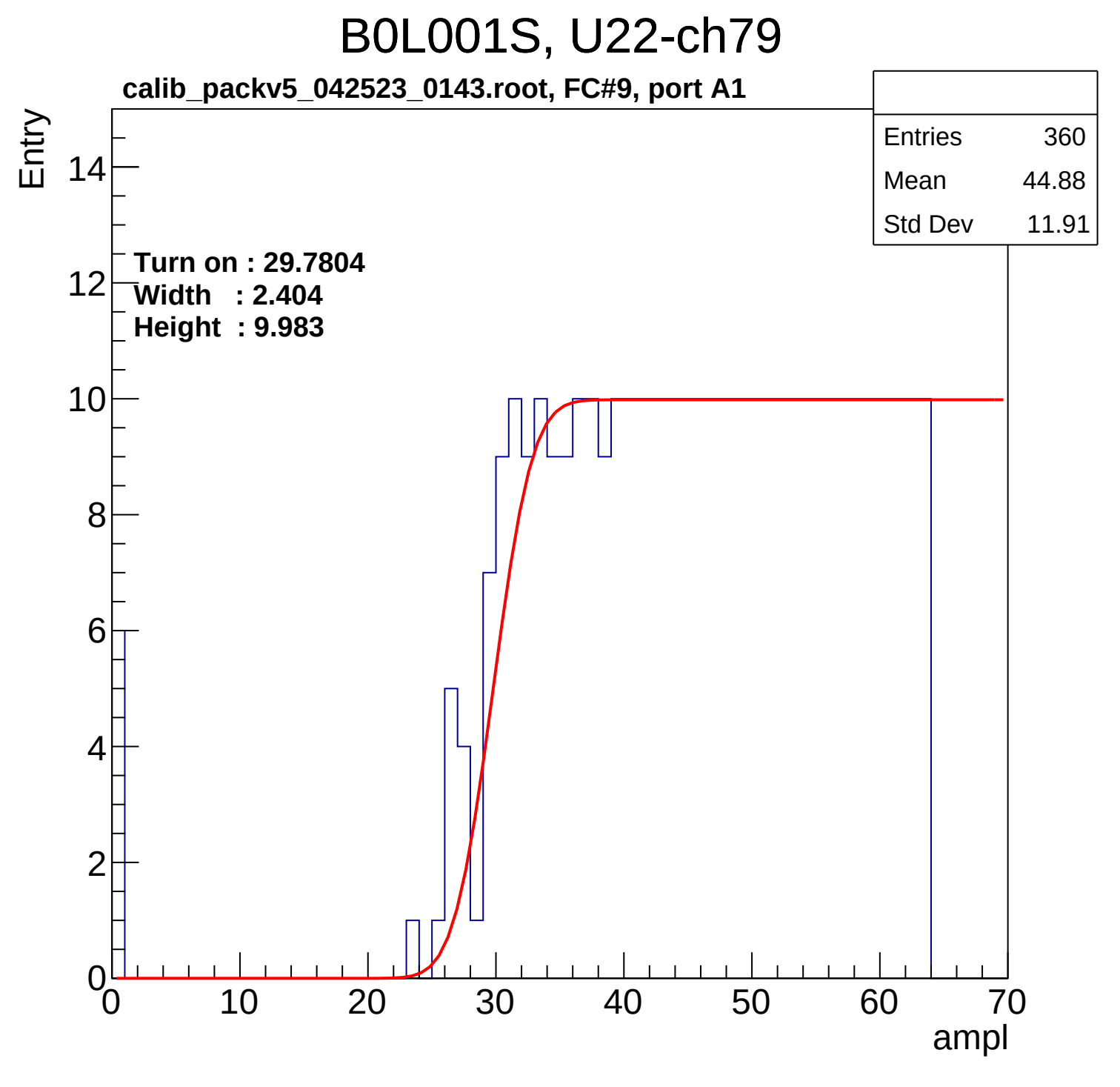
B0L001S, U22-ch79
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 44.88
Std Dev 11.91
Turn on : 29.7804
Width : 2.404
Height : 9.983
Entry
ampl
0
2
4
6
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10
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0
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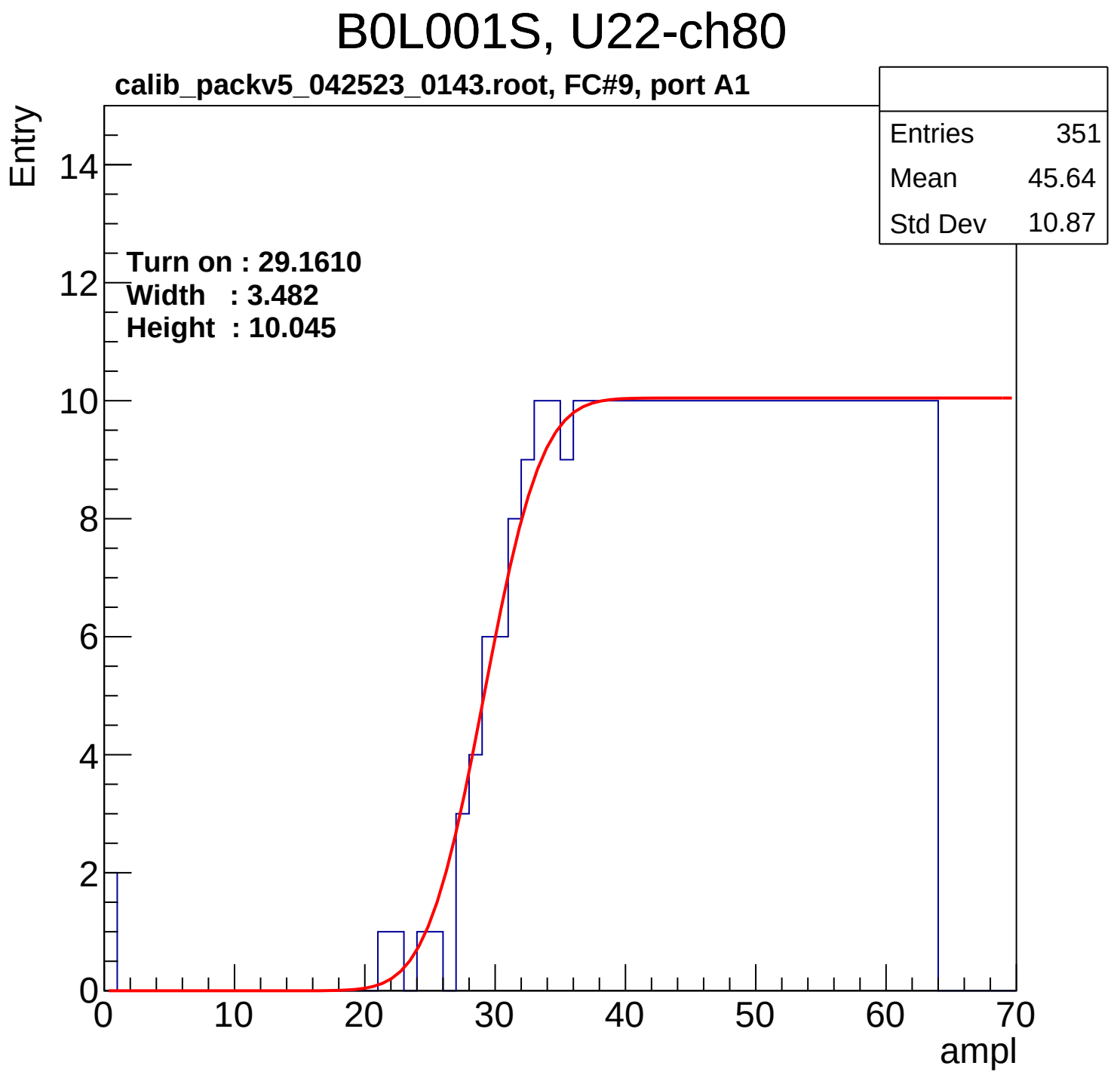
B0L001S, U22-ch80
calib_packv5_042523_0143.root, FC#9, port A1
Entries 351
Mean 45.64
Std Dev 10.87
Turn on : 29.1610
Width : 3.482
Height : 10.045
Entry
ampl
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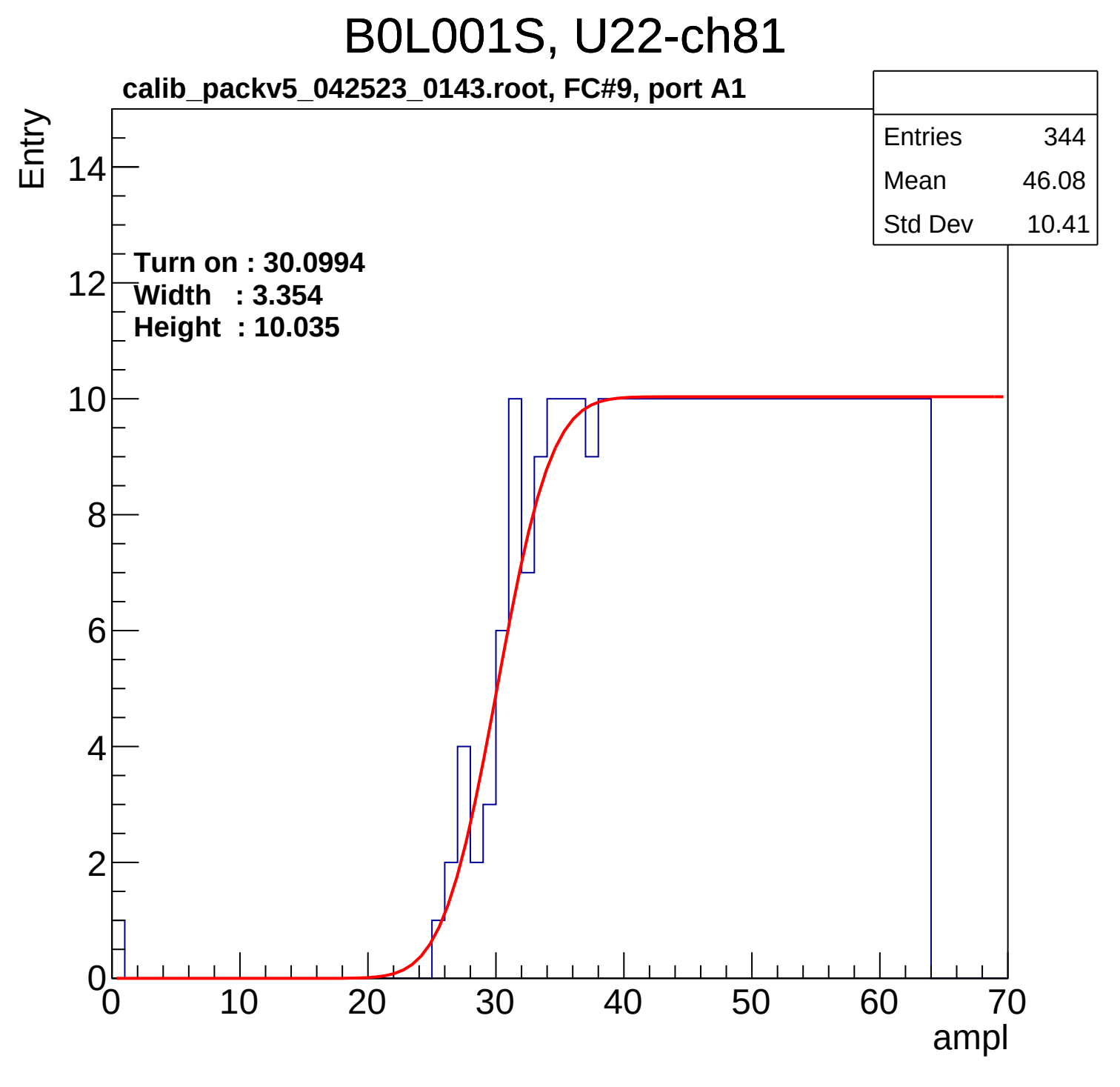
B0L001S, U22-ch81
calib_packv5_042523_0143.root, FC#9, port A1
Entries 344
Mean 46.08
Std Dev 10.41
Turn on : 30.0994
Width : 3.354
Height : 10.035
Entry
ampl
0
2
4
6
8
10
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0
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20
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40
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60
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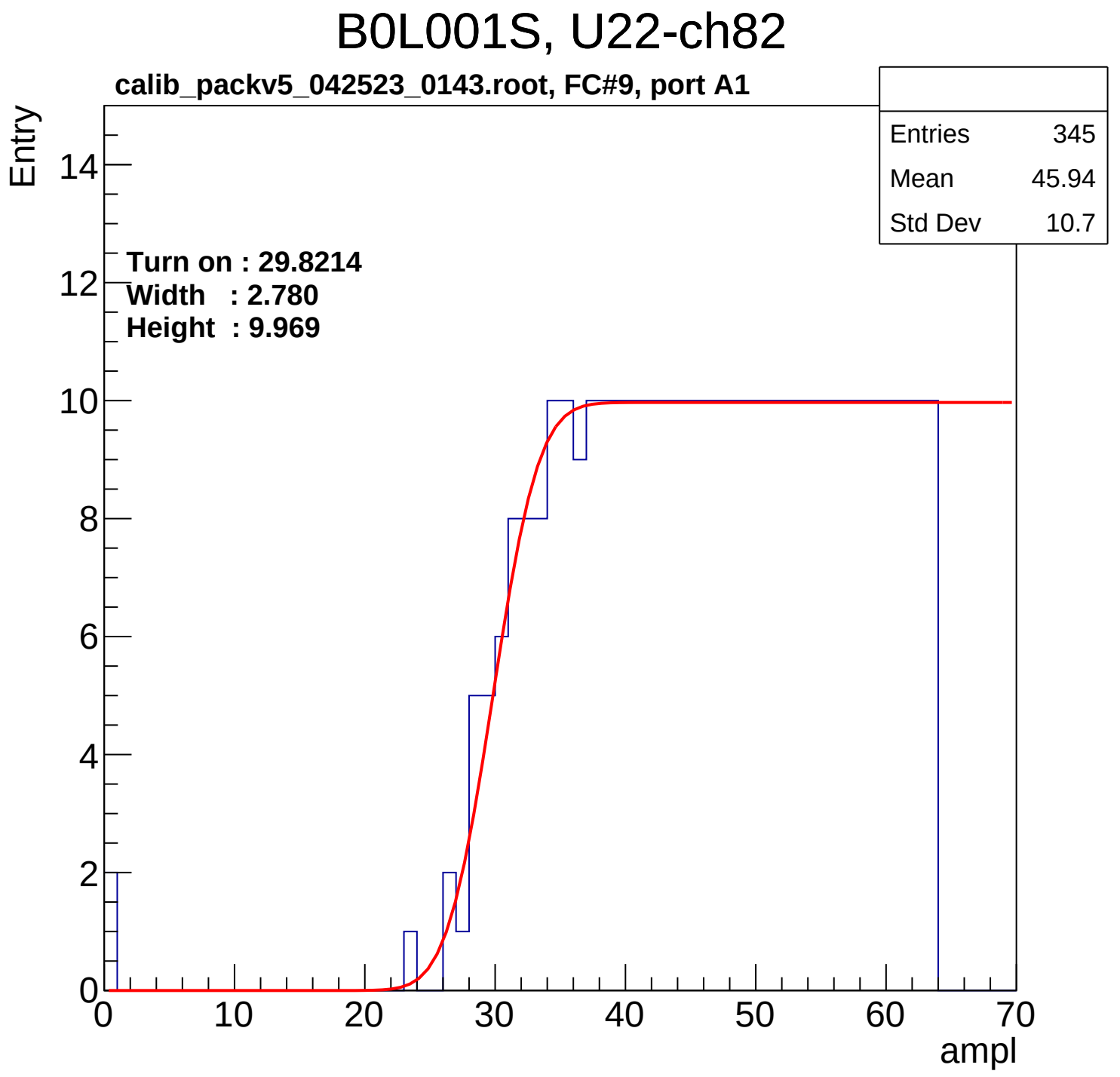
B0L001S, U22-ch82
calib_packv5_042523_0143.root, FC#9, port A1
Entries 345
Mean 45.94
Std Dev 10.7
Turn on : 29.8214
Width : 2.780
Height : 9.969
Entry
ampl
0
2
4
6
8
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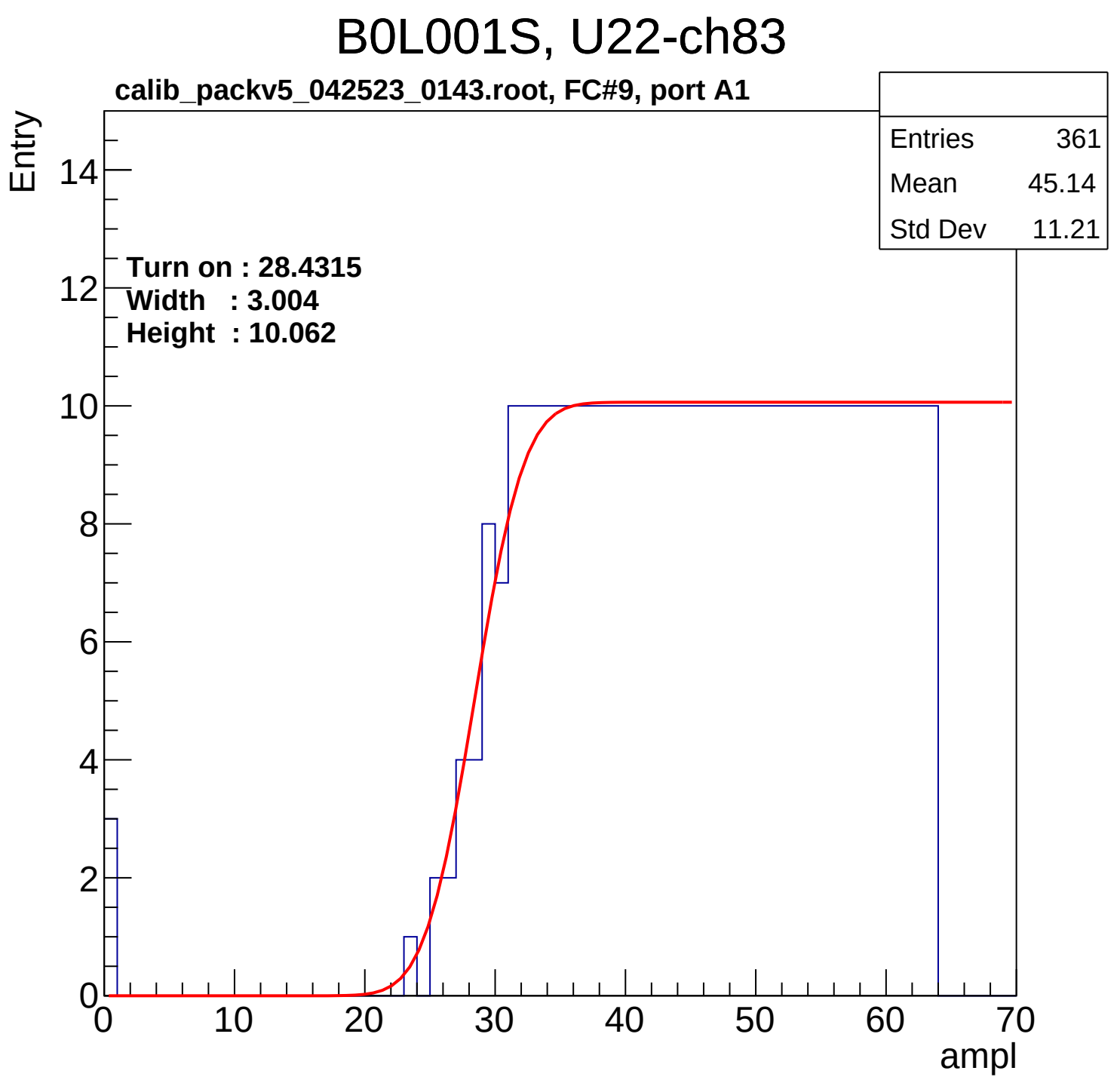
B0L001S, U22-ch83
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.14
Std Dev 11.21
Turn on : 28.4315
Width : 3.004
Height : 10.062
Entry
ampl
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2
4
6
8
10
12
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0
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60
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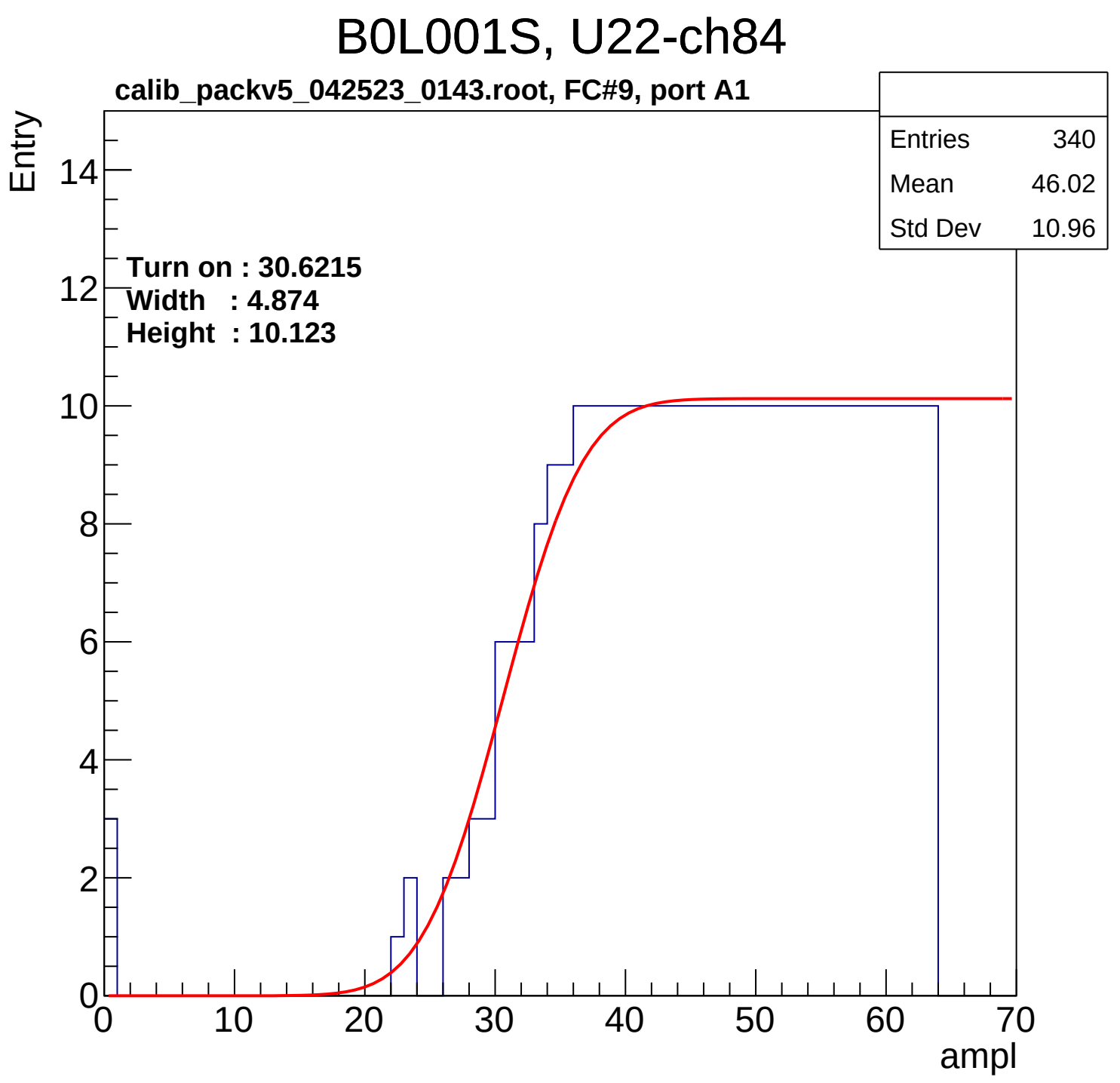
B0L001S, U22-ch84
calib_packv5_042523_0143.root, FC#9, port A1
Entries 340
Mean 46.02
Std Dev 10.96
Turn on : 30.6215
Width : 4.874
Height : 10.123
Entry
ampl
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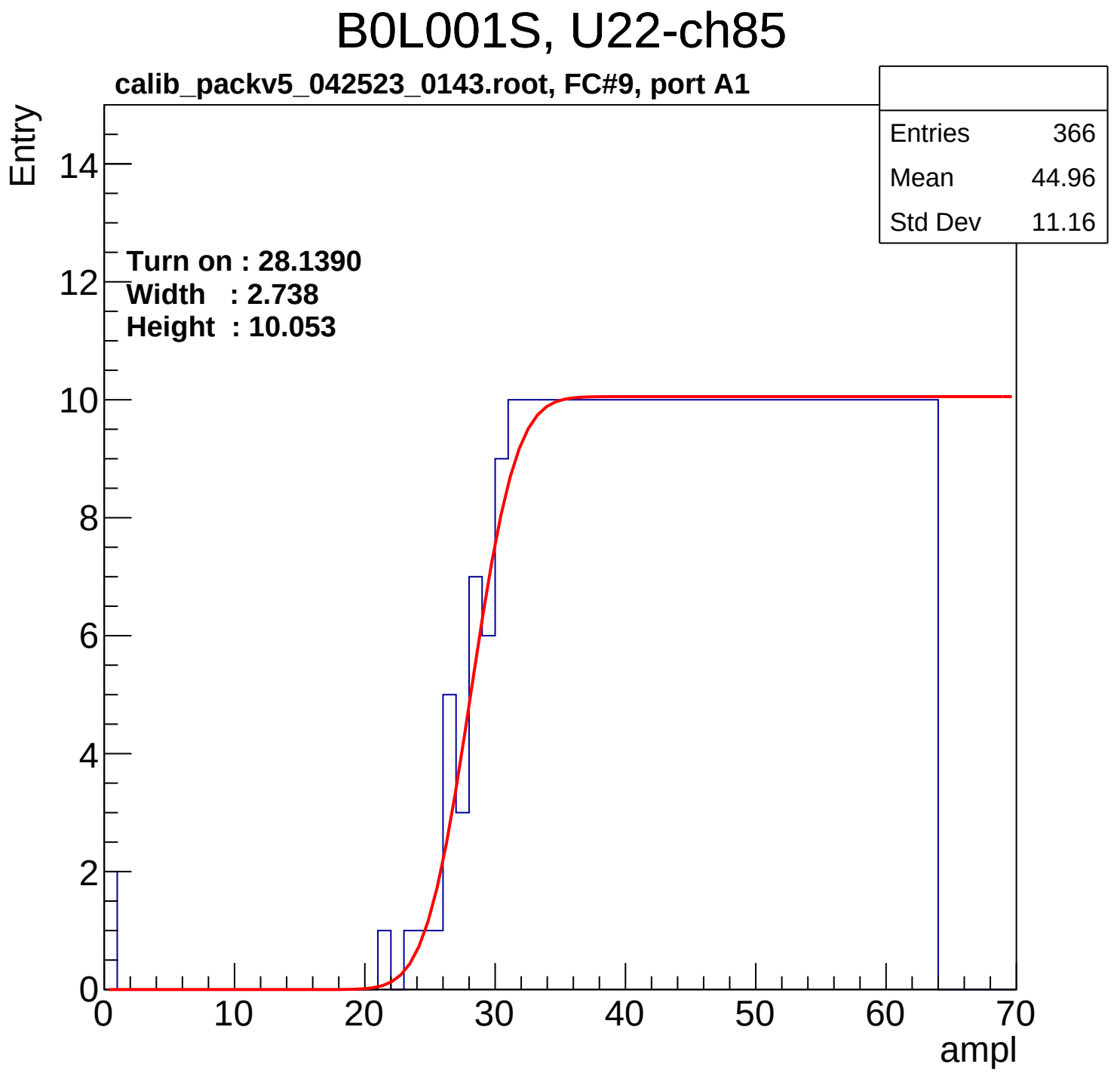
B0L001S, U22-ch85
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.96
Std Dev 11.16
Turn on : 28.1390
Width : 2.738
Height : 10.053
Entry
ampl
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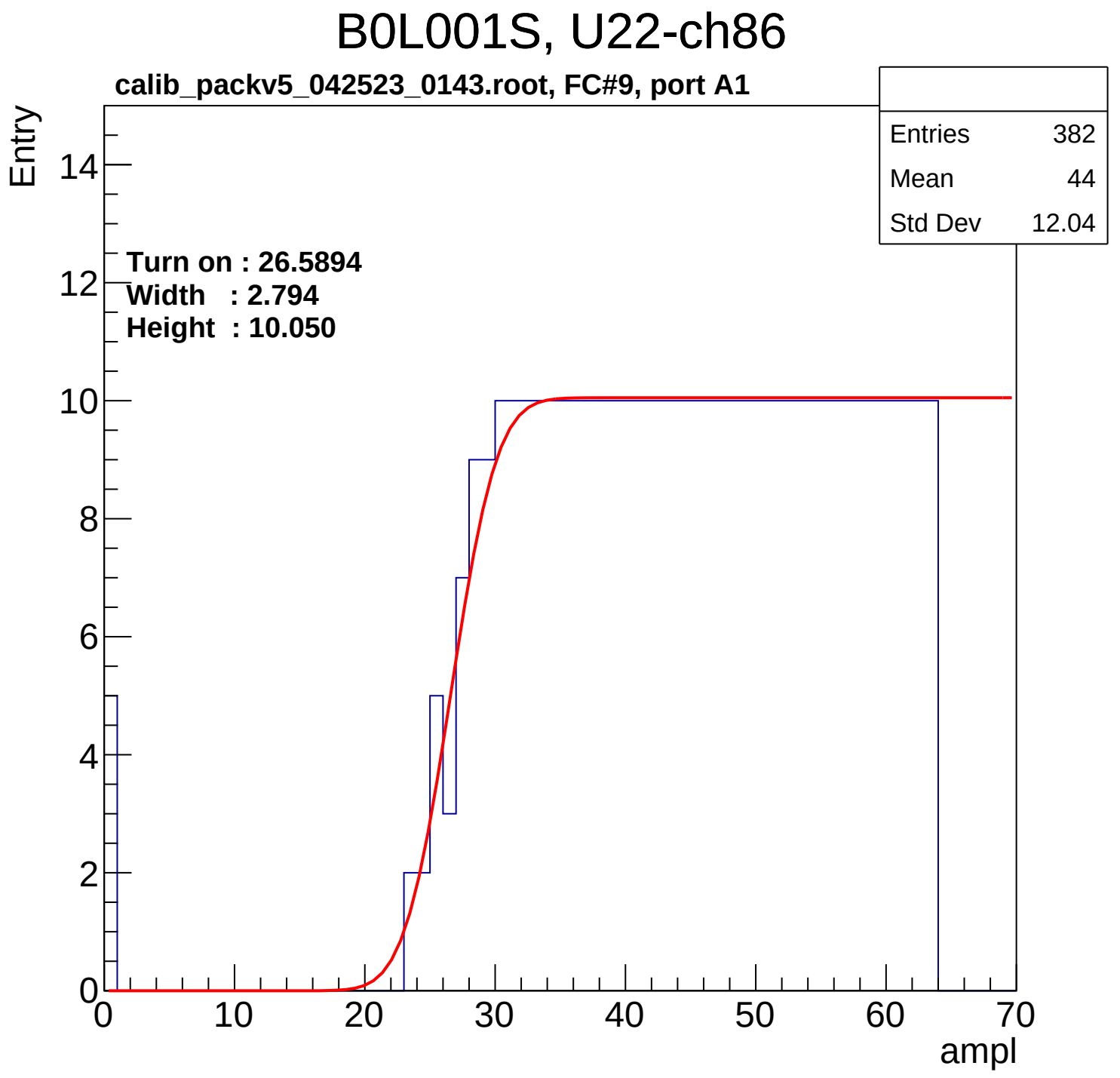
B0L001S, U22-ch86
calib_packv5_042523_0143.root, FC#9, port A1
Entries 382
Mean 44
Std Dev 12.04
Turn on : 26.5894
Width : 2.794
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
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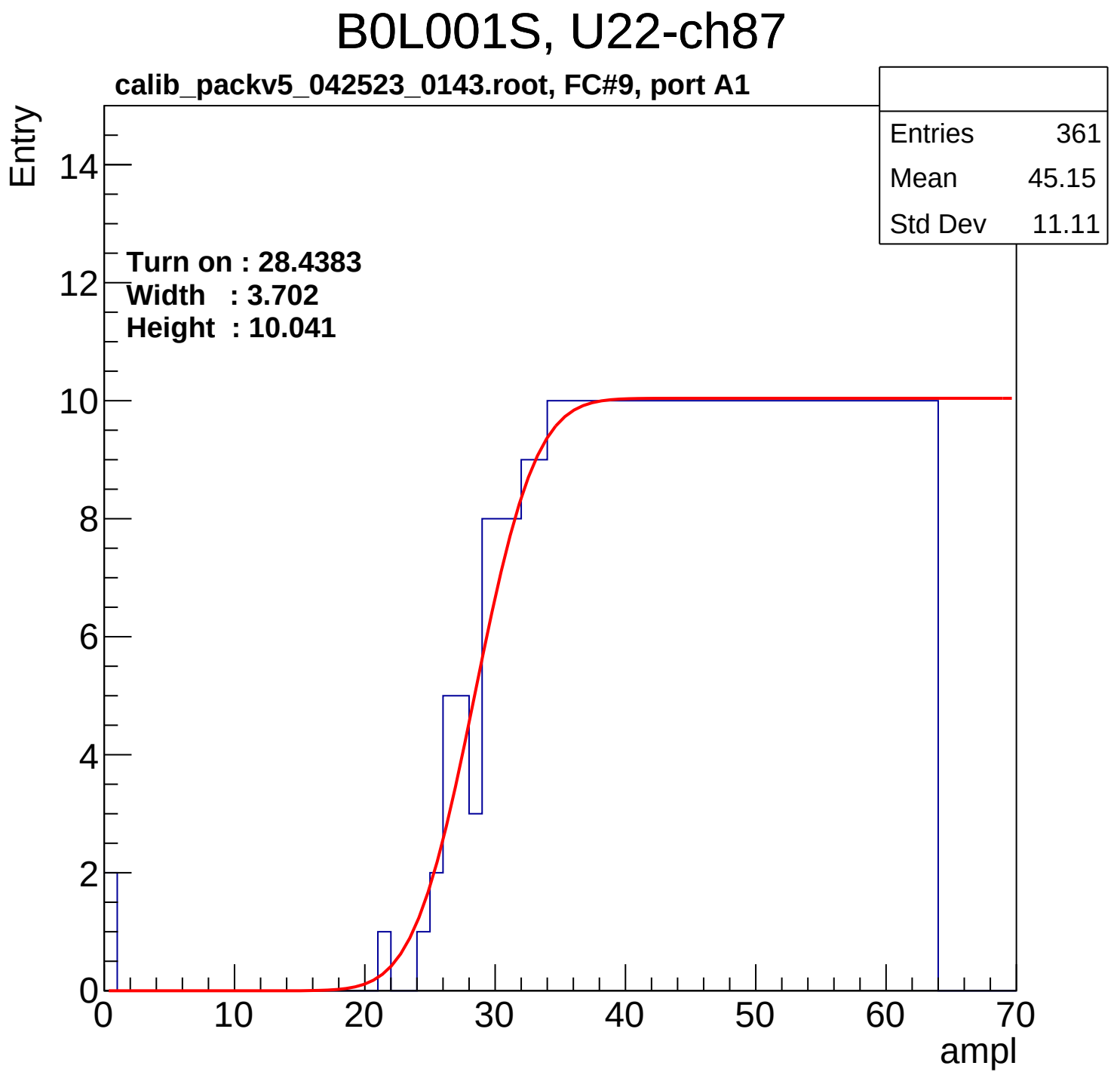
B0L001S, U22-ch87
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.15
Std Dev 11.11
Turn on : 28.4383
Width : 3.702
Height : 10.041
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ampl
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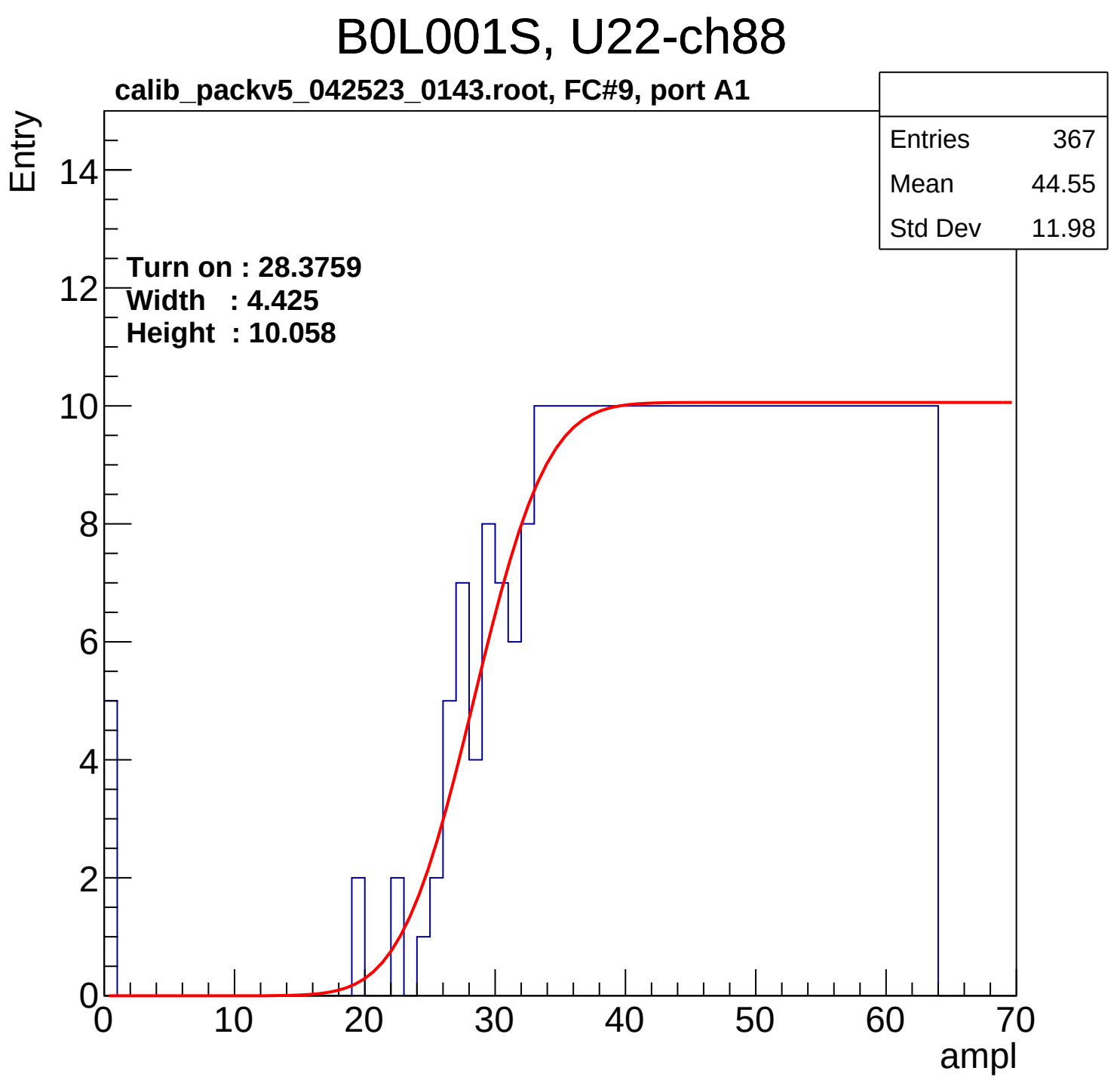
B0L001S, U22-ch88
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.55
Std Dev 11.98
Turn on : 28.3759
Width : 4.425
Height : 10.058
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ampl
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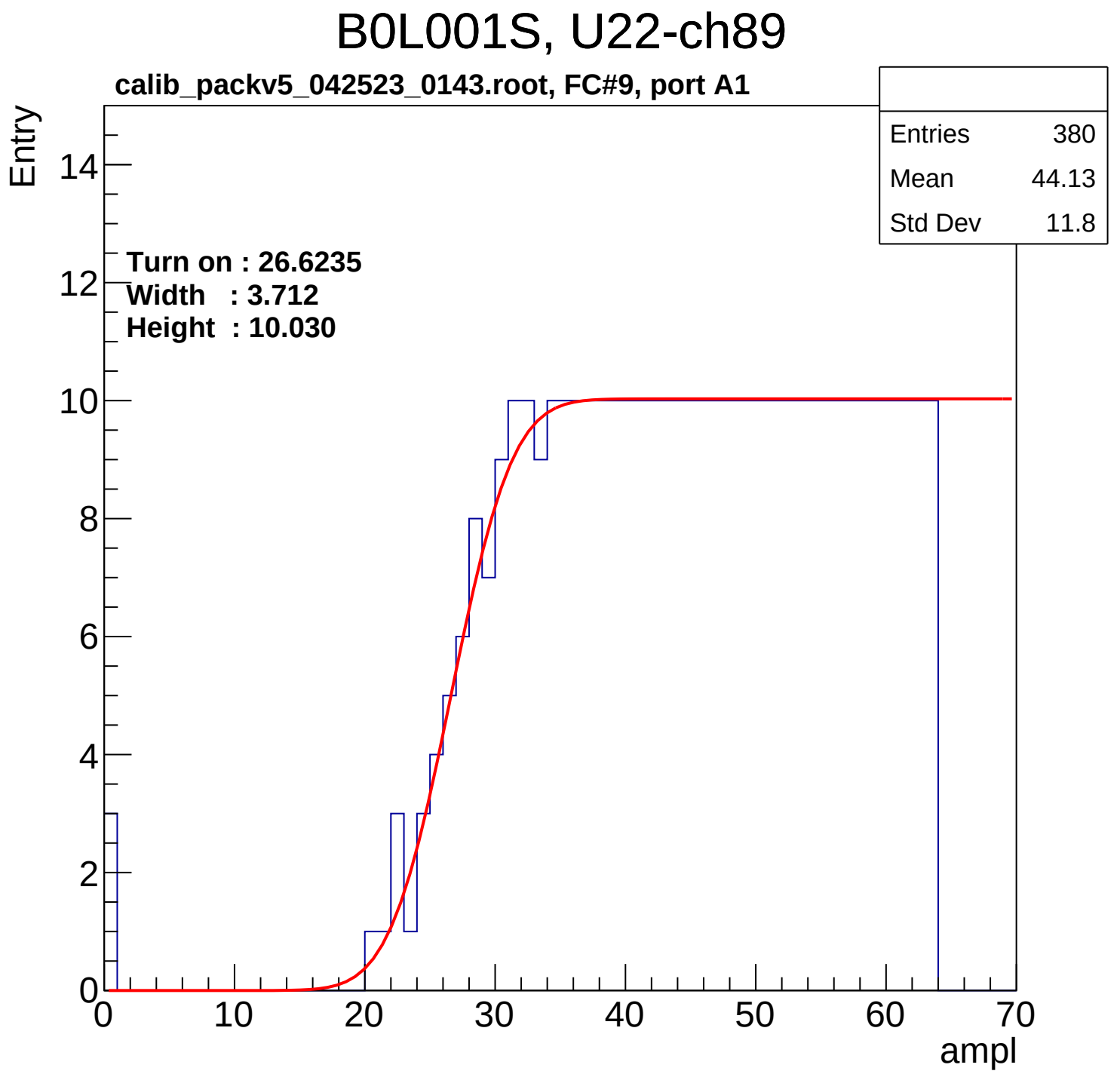
B0L001S, U22-ch89
calib_packv5_042523_0143.root, FC#9, port A1
Entries 380
Mean 44.13
Std Dev 11.8
Turn on : 26.6235
Width : 3.712
Height : 10.030
Entry
ampl
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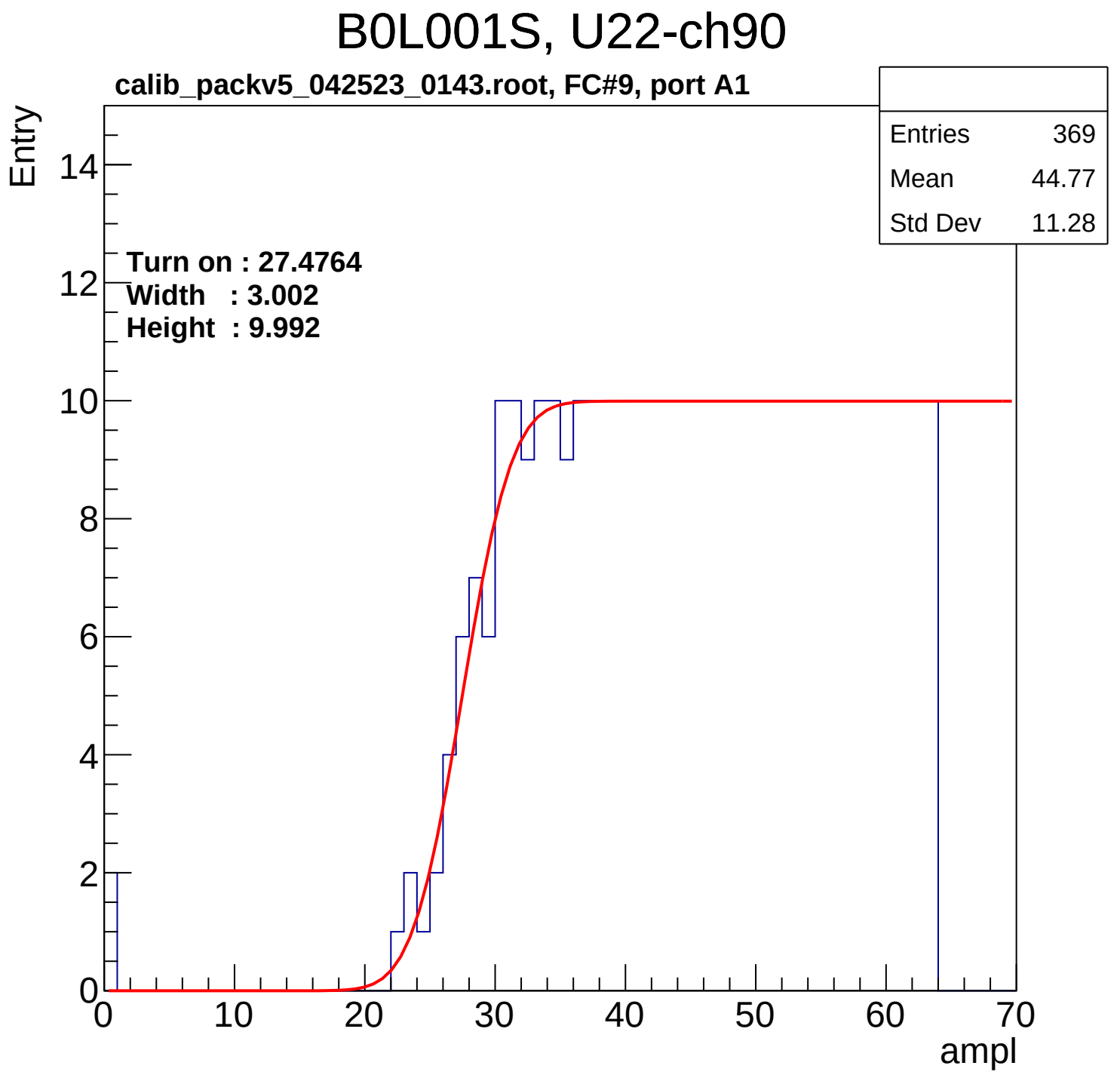
B0L001S, U22-ch90
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.77
Std Dev 11.28
Turn on : 27.4764
Width : 3.002
Height : 9.992
Entry
ampl
0
2
4
6
8
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12
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0
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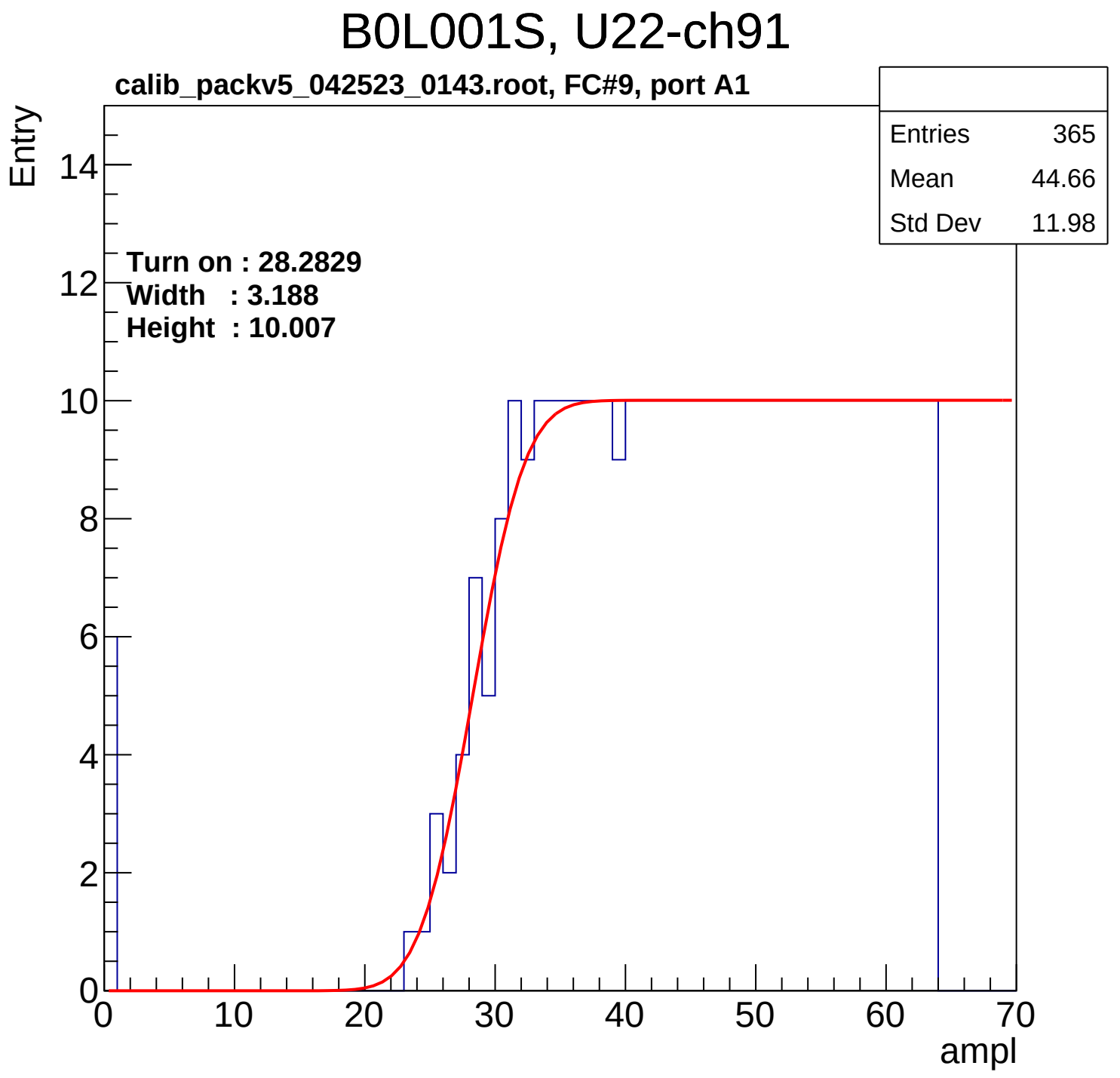
B0L001S, U22-ch91
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.66
Std Dev 11.98
Turn on : 28.2829
Width : 3.188
Height : 10.007
Entry
ampl
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2
4
6
8
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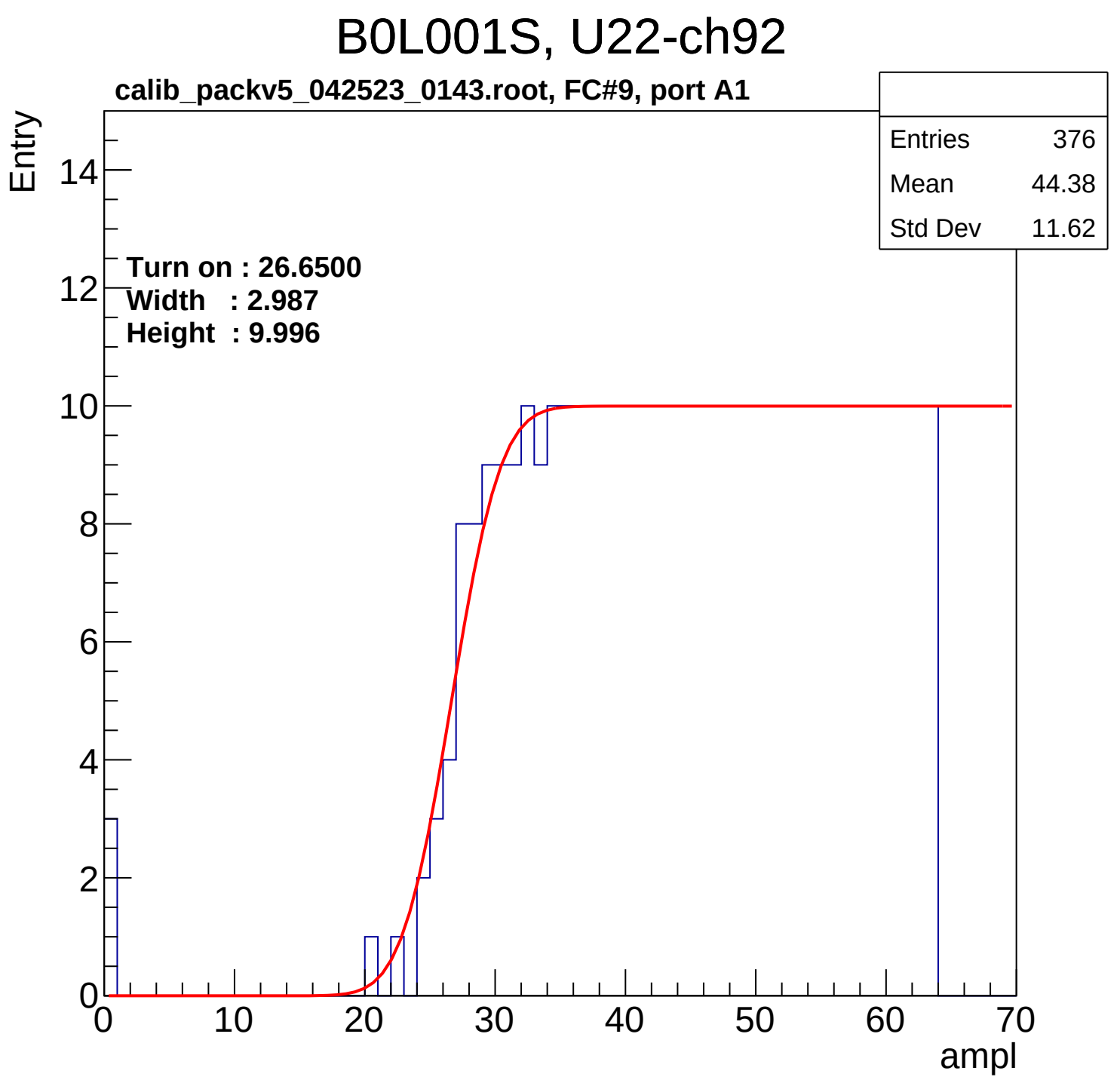
B0L001S, U22-ch92
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.38
Std Dev 11.62
Turn on : 26.6500
Width : 2.987
Height : 9.996
Entry
ampl
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2
4
6
8
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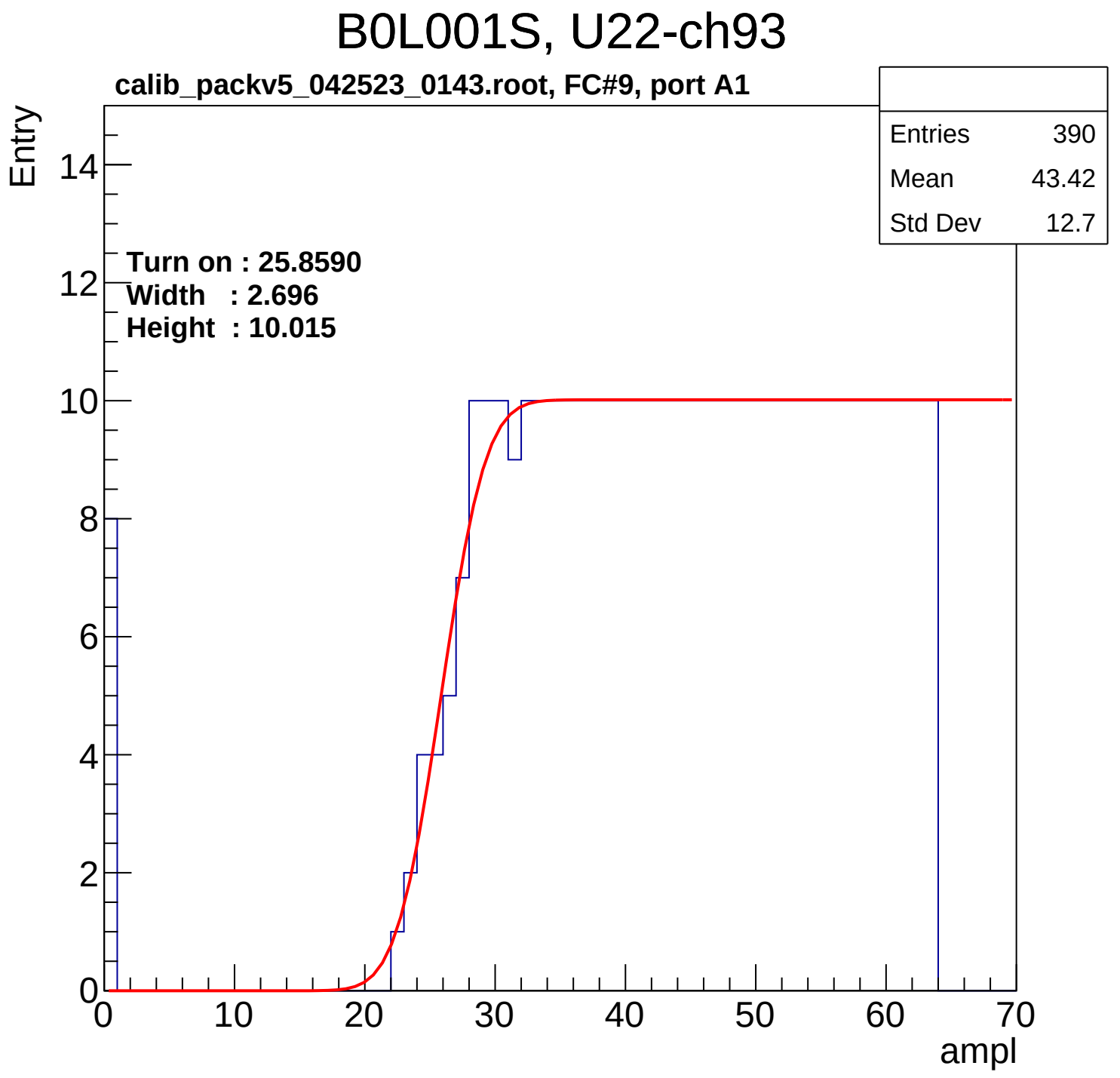
B0L001S, U22-ch93
calib_packv5_042523_0143.root, FC#9, port A1
Entries 390
Mean 43.42
Std Dev 12.7
Turn on : 25.8590
Width : 2.696
Height : 10.015
Entry
ampl
0
2
4
6
8
10
12
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0
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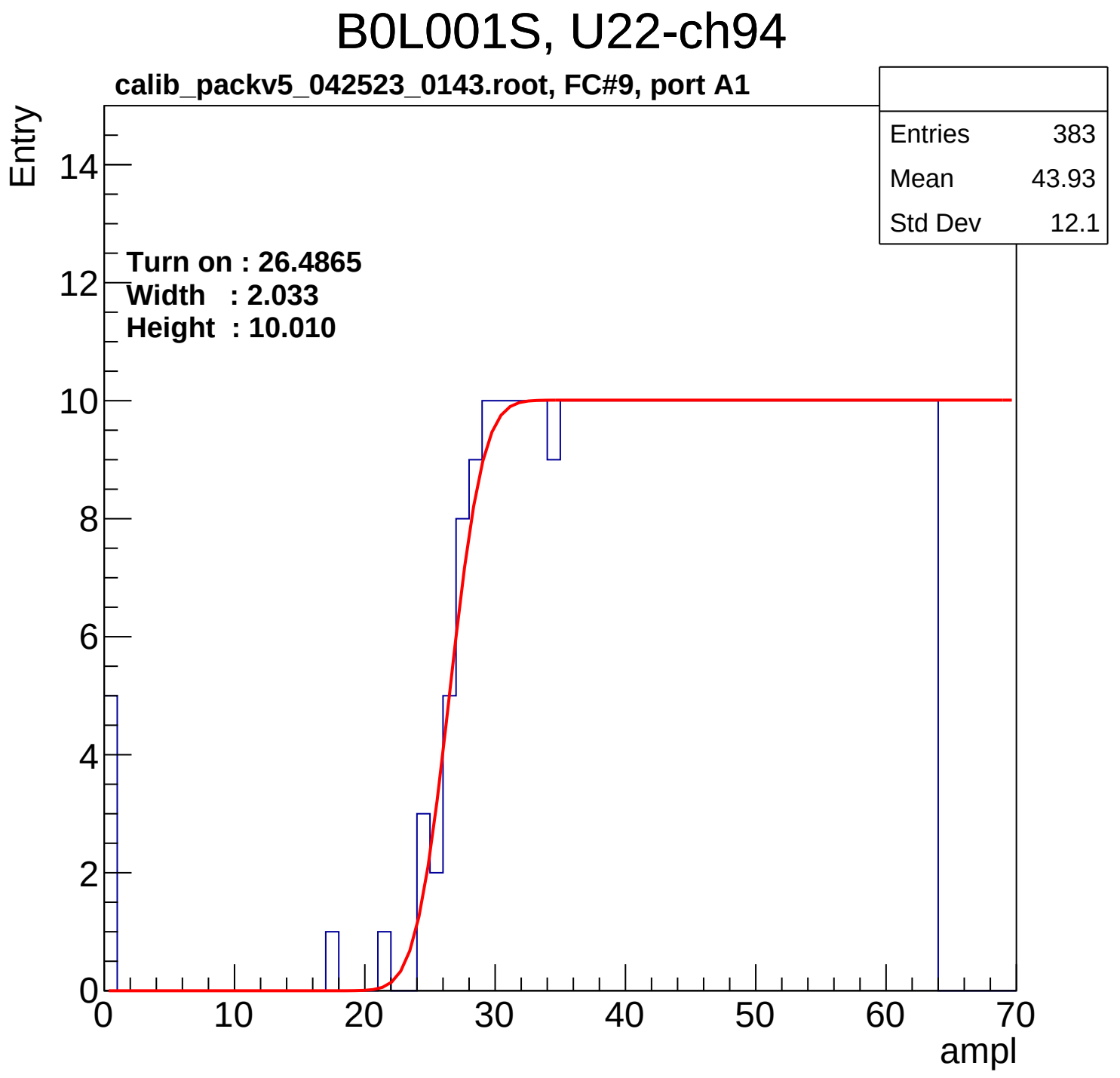
B0L001S, U22-ch94
calib_packv5_042523_0143.root, FC#9, port A1
Entries 383
Mean 43.93
Std Dev 12.1
Turn on : 26.4865
Width : 2.033
Height : 10.010
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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40
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60
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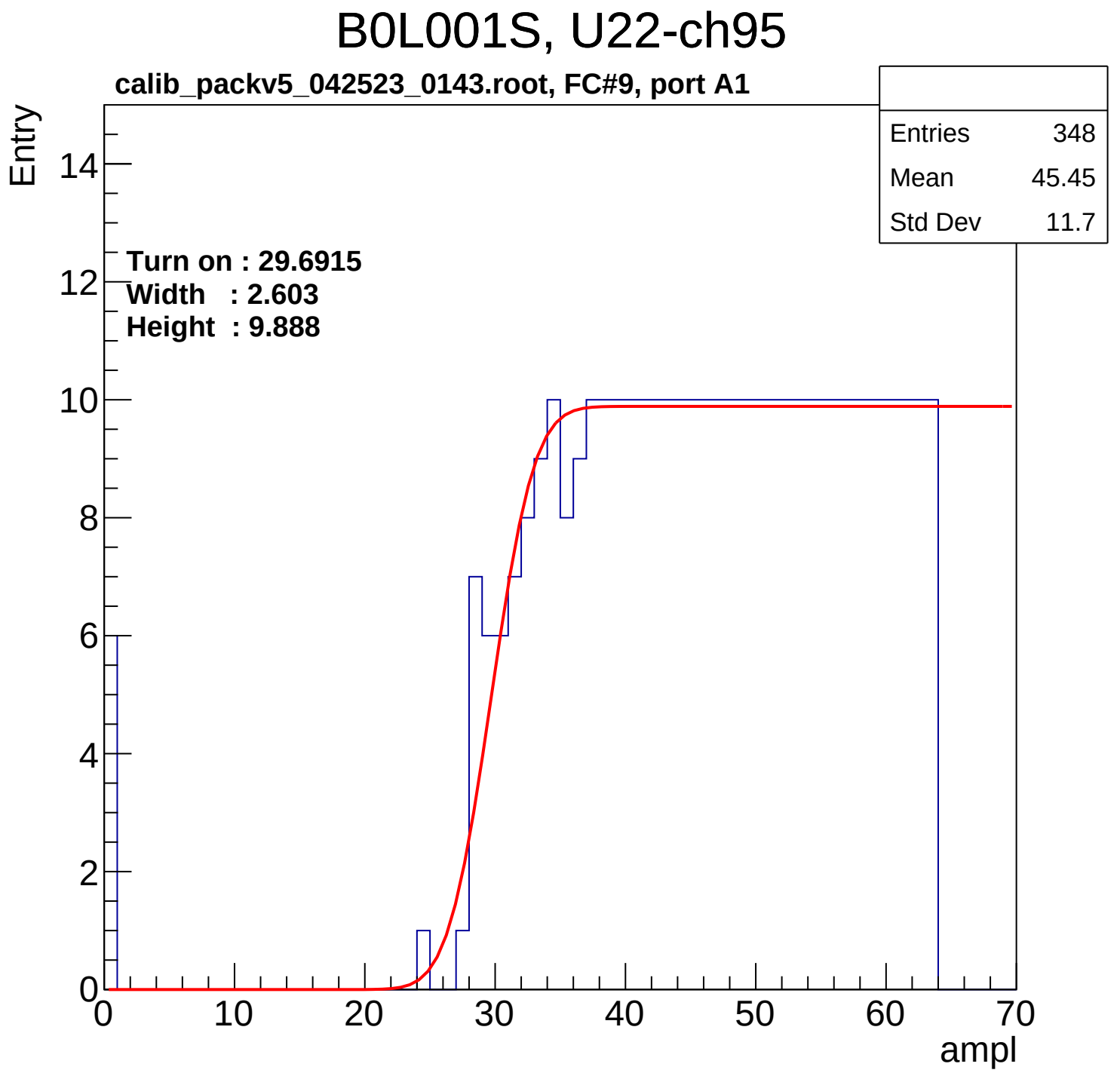
B0L001S, U22-ch95
calib_packv5_042523_0143.root, FC#9, port A1
Entries 348
Mean 45.45
Std Dev 11.7
Turn on : 29.6915
Width : 2.603
Height : 9.888
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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60
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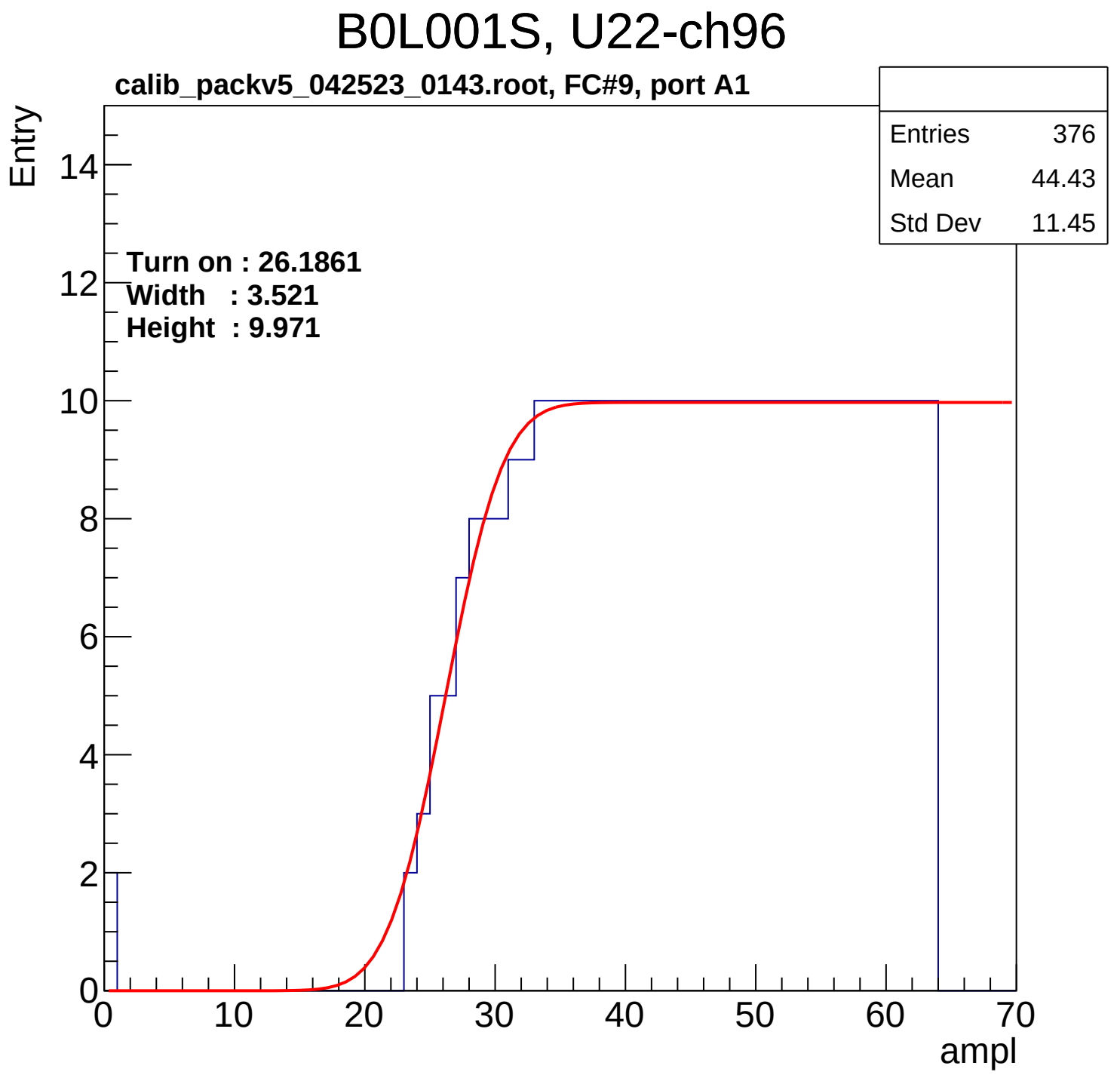
B0L001S, U22-ch96
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.43
Std Dev 11.45
Turn on : 26.1861
Width : 3.521
Height : 9.971
Entry
ampl
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2
4
6
8
10
12
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0
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20
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40
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60
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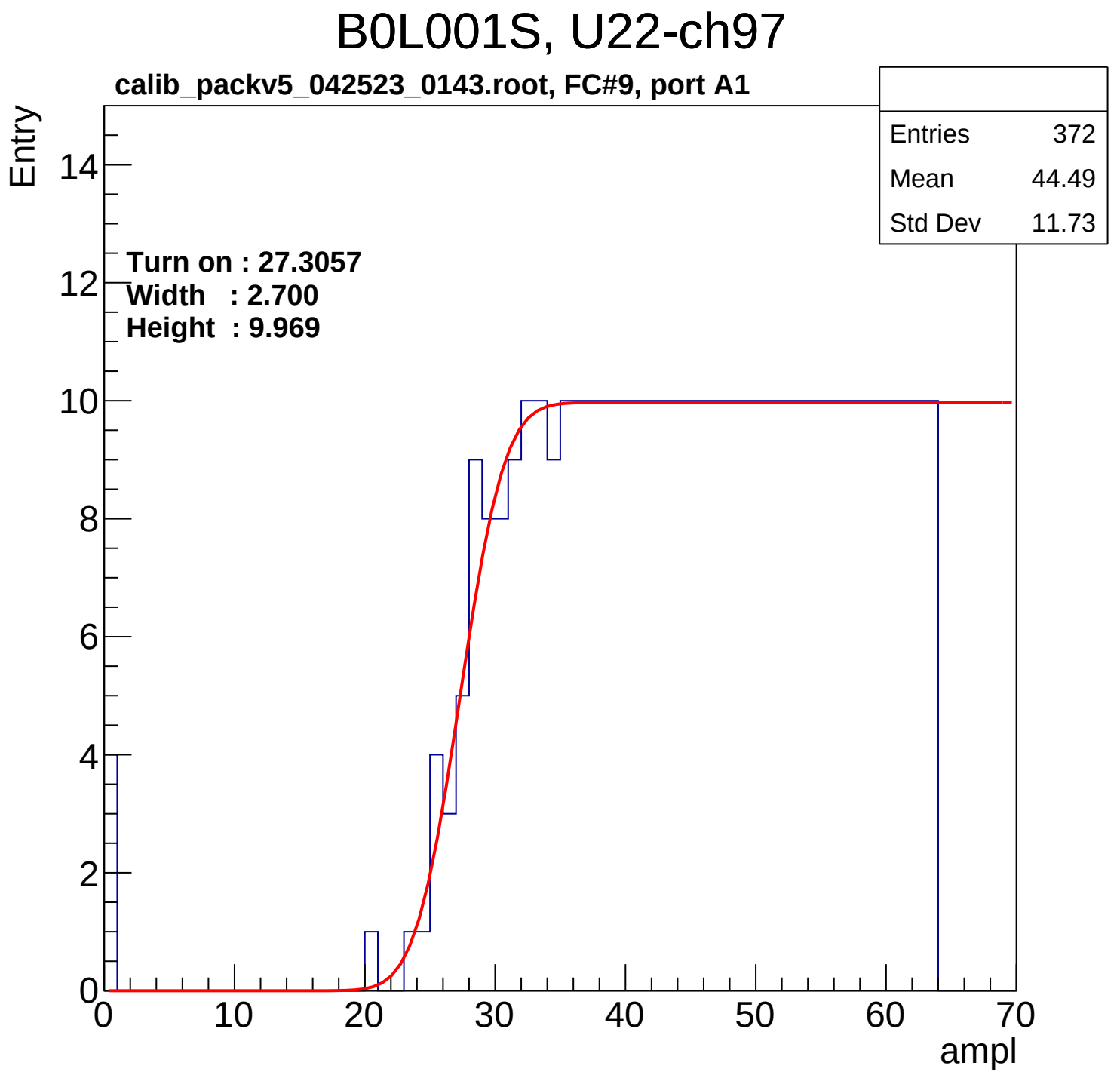
B0L001S, U22-ch97
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.49
Std Dev 11.73
Turn on : 27.3057
Width : 2.700
Height : 9.969
Entry
ampl
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6
8
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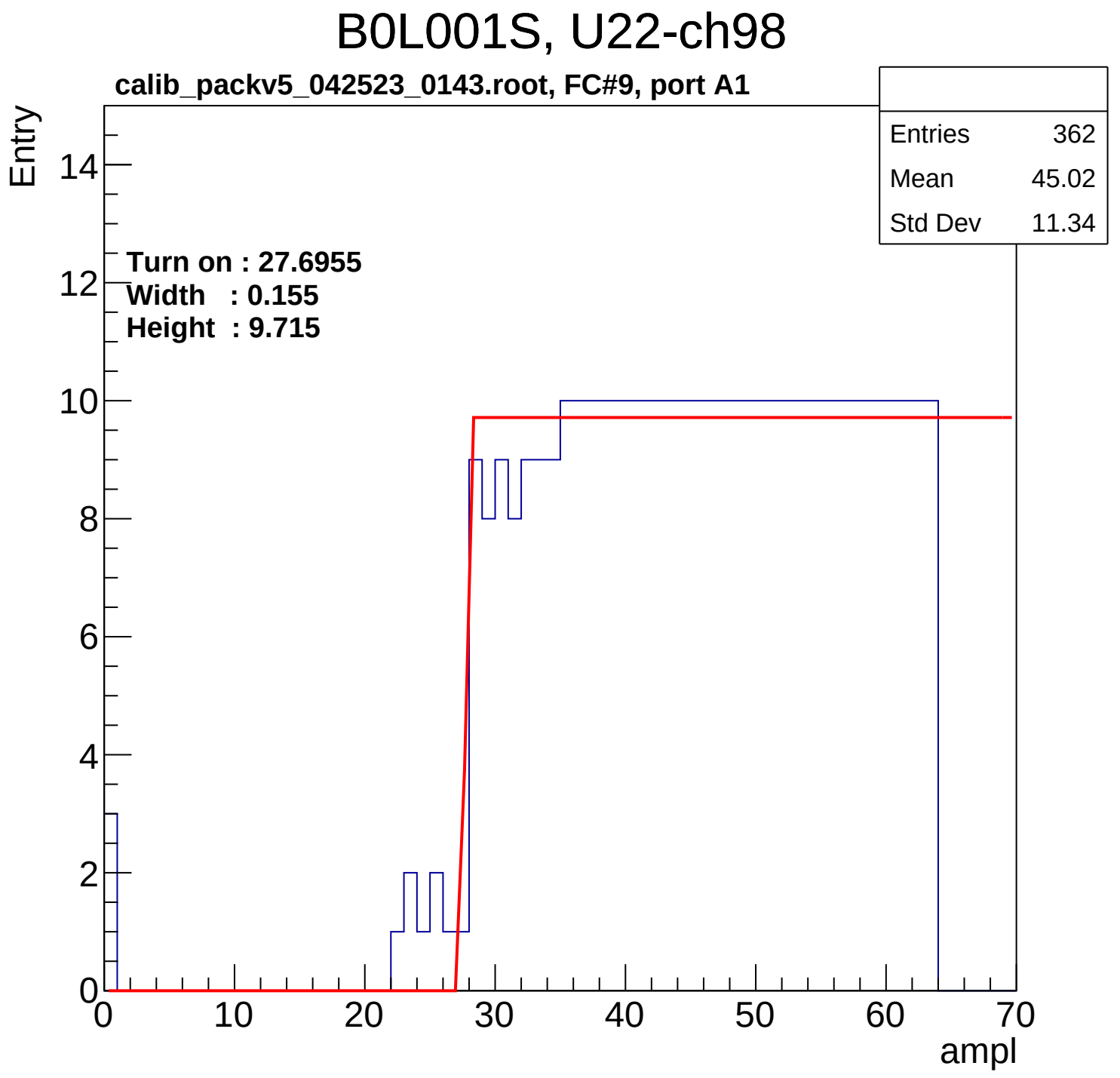
B0L001S, U22-ch98
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.02
Std Dev 11.34
Turn on : 27.6955
Width : 0.155
Height : 9.715
Entry
ampl
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6
8
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0
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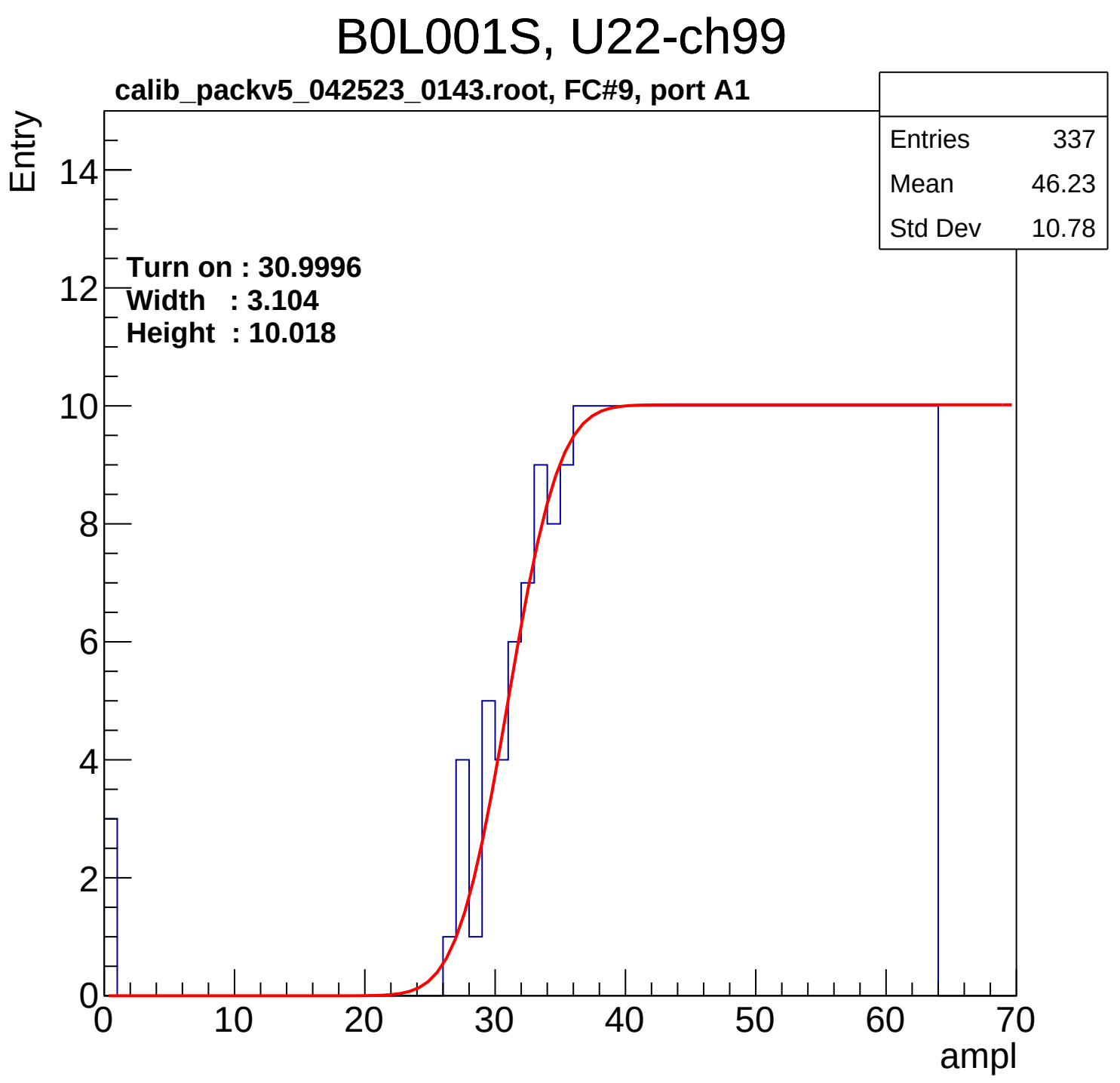
B0L001S, U22-ch99
calib_packv5_042523_0143.root, FC#9, port A1
Entries 337
Mean 46.23
Std Dev 10.78
Turn on : 30.9996
Width : 3.104
Height : 10.018
Entry
ampl
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6
8
10
12
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0
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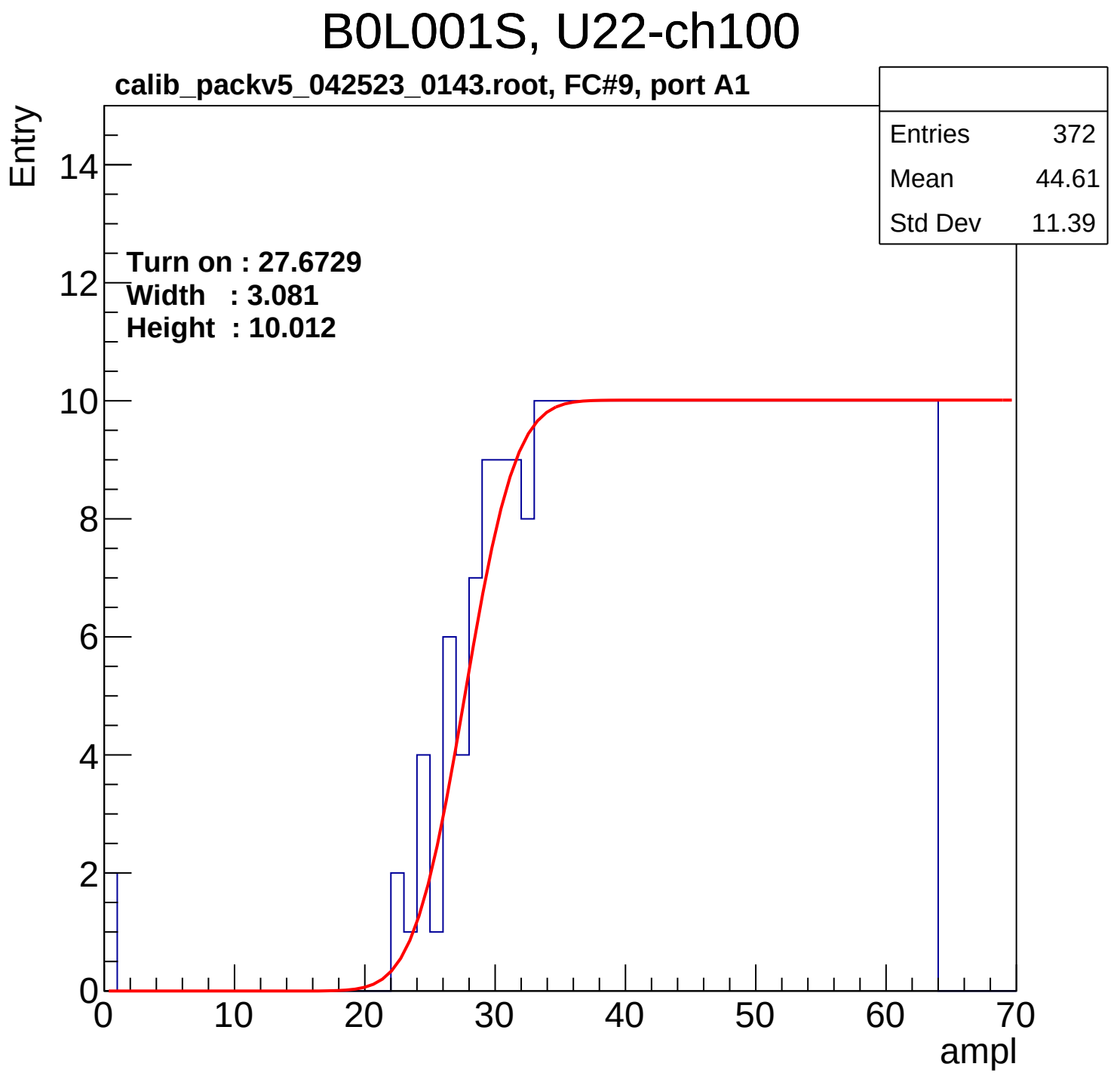
B0L001S, U22-ch100
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.61
Std Dev 11.39
Turn on : 27.6729
Width : 3.081
Height : 10.012
Entry
ampl
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4
6
8
10
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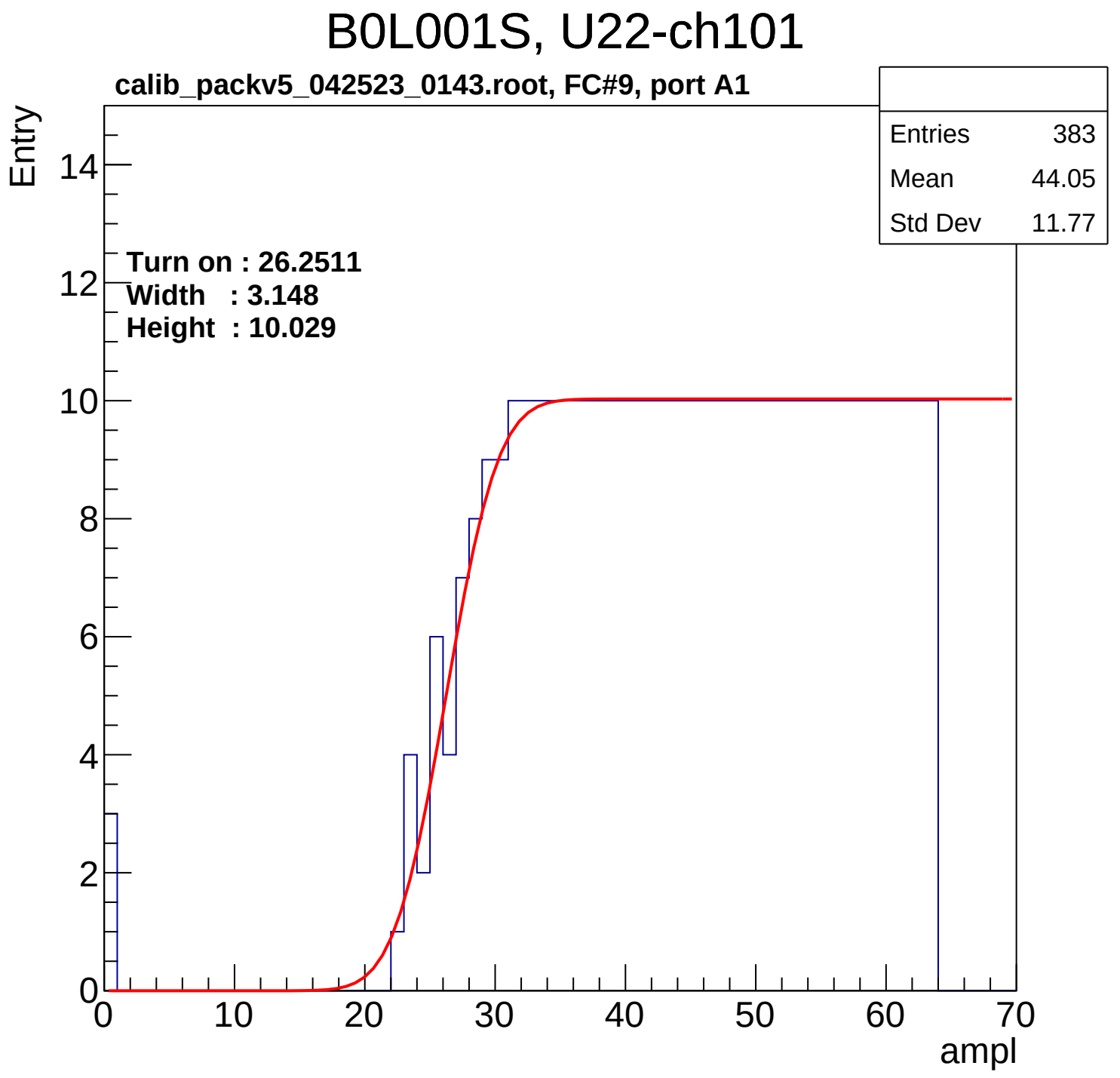
B0L001S, U22-ch101
calib_packv5_042523_0143.root, FC#9, port A1
Entries 383
Mean 44.05
Std Dev 11.77
Turn on : 26.2511
Width : 3.148
Height : 10.029
Entry
ampl
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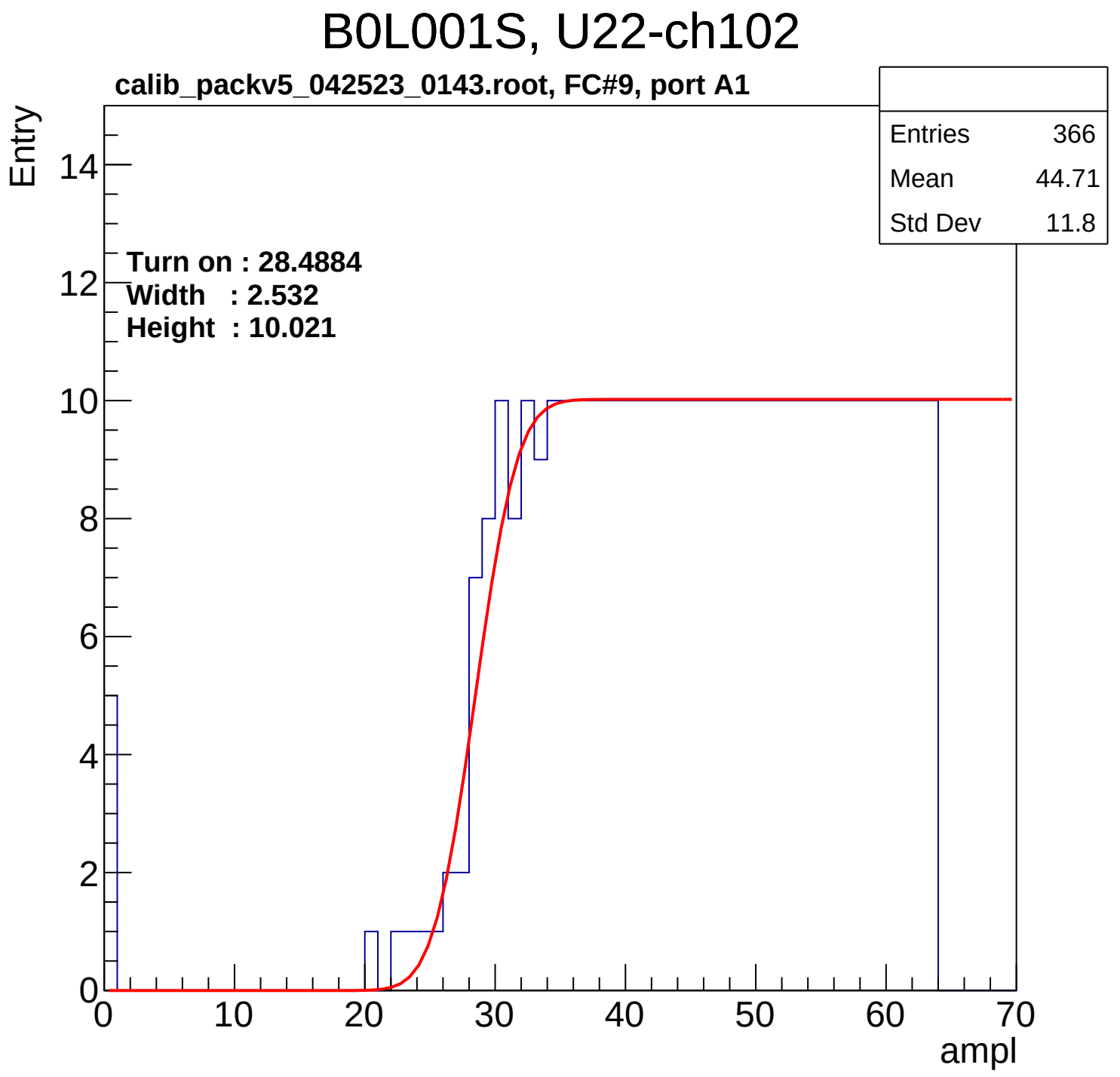
B0L001S, U22-ch102
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.71
Std Dev 11.8
Turn on : 28.4884
Width : 2.532
Height : 10.021
Entry
ampl
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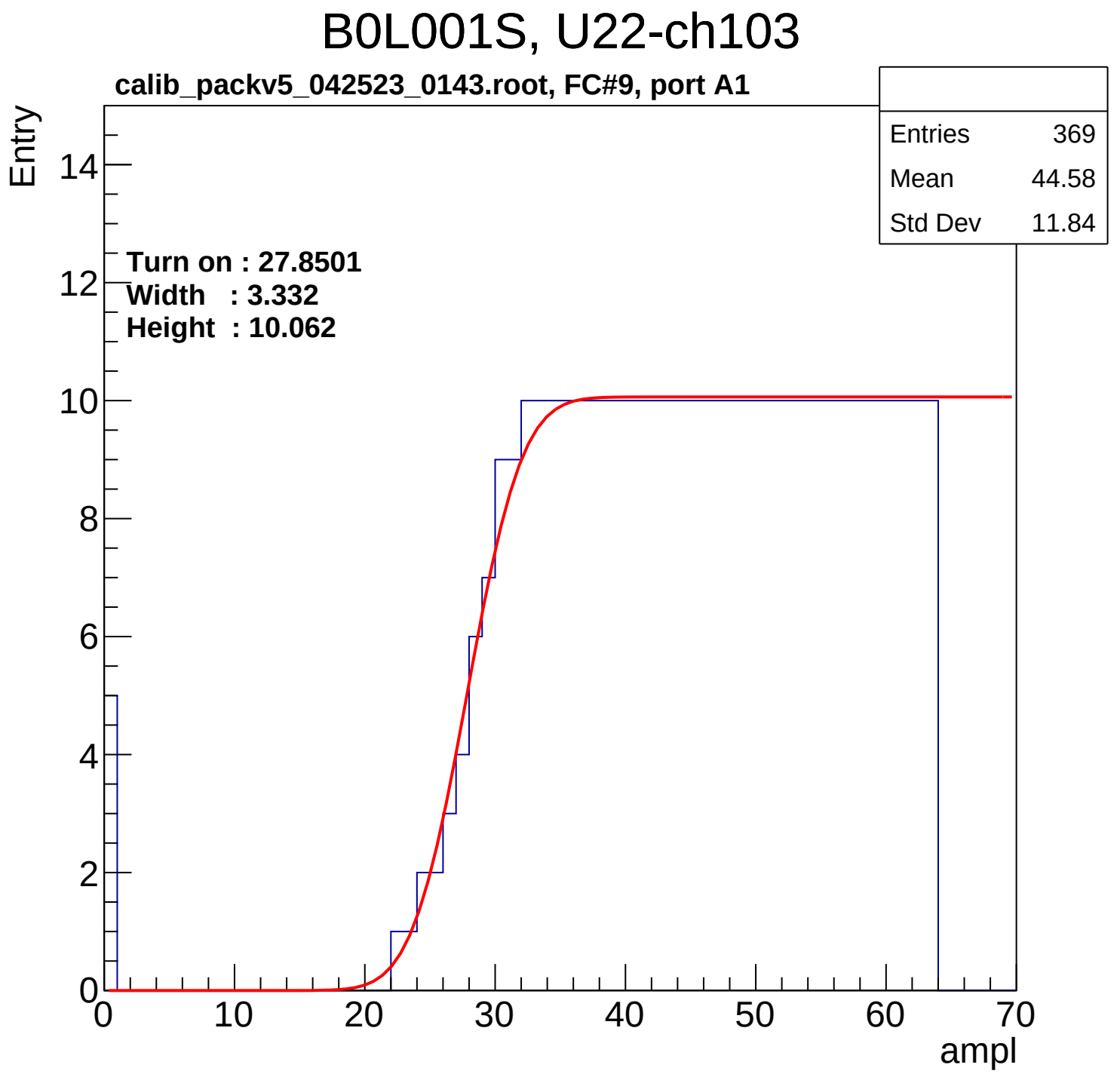
B0L001S, U22-ch103
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.58
Std Dev 11.84
Turn on : 27.8501
Width : 3.332
Height : 10.062
Entry
ampl
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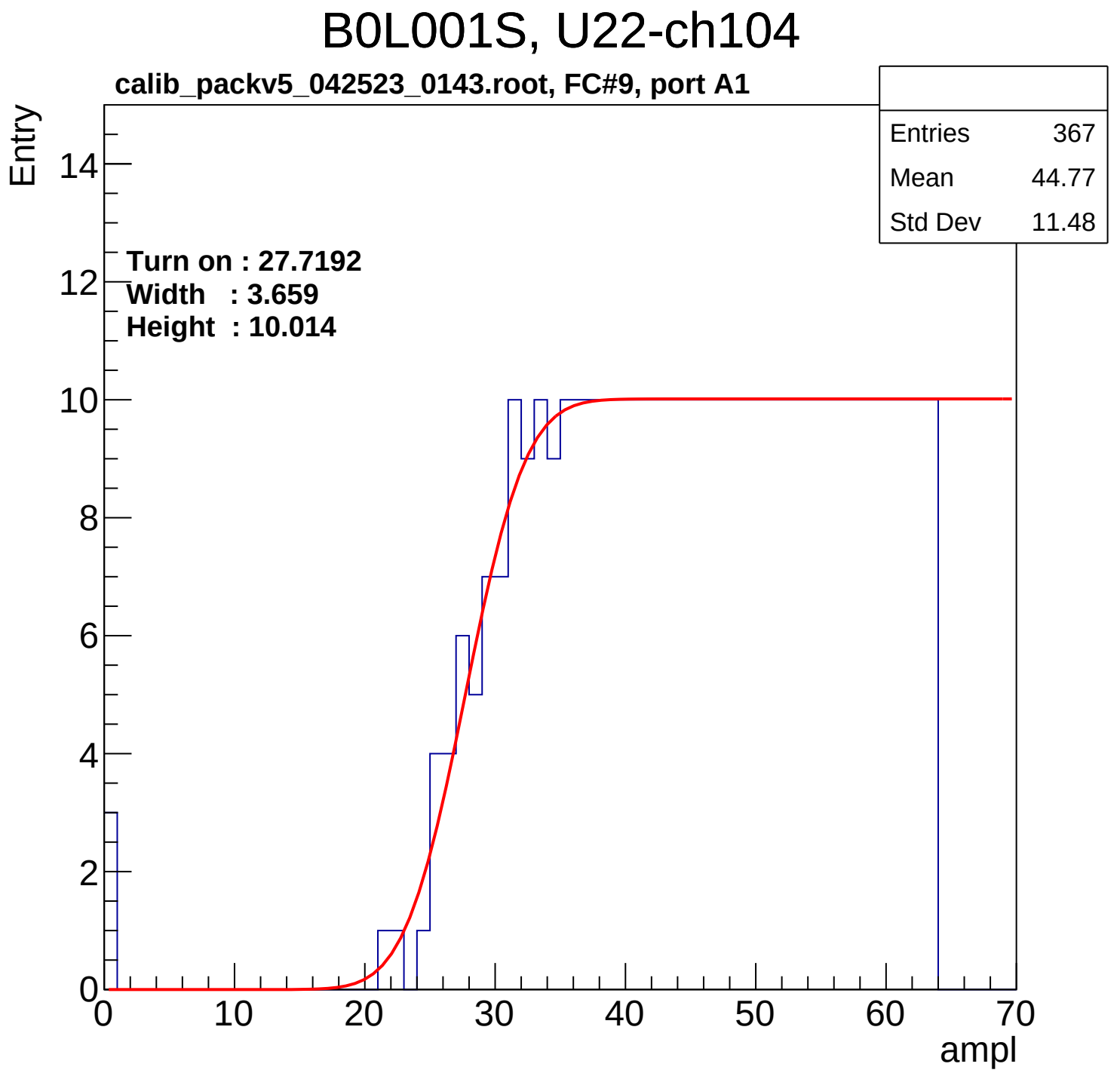
B0L001S, U22-ch104
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.77
Std Dev 11.48
Turn on : 27.7192
Width : 3.659
Height : 10.014
Entry
ampl
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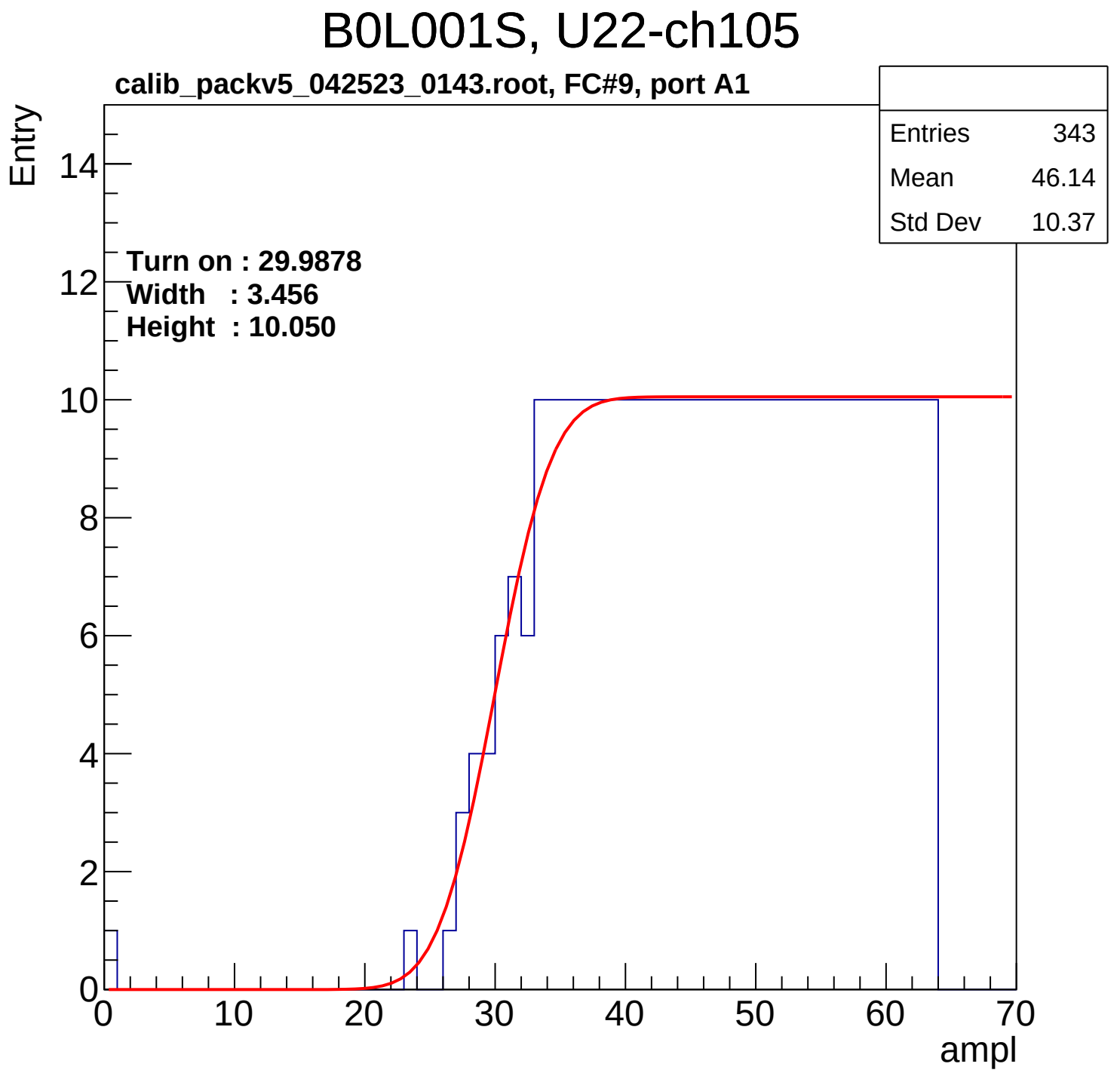
B0L001S, U22-ch105
calib_packv5_042523_0143.root, FC#9, port A1
Entries 343
Mean 46.14
Std Dev 10.37
Turn on : 29.9878
Width : 3.456
Height : 10.050
Entry
ampl
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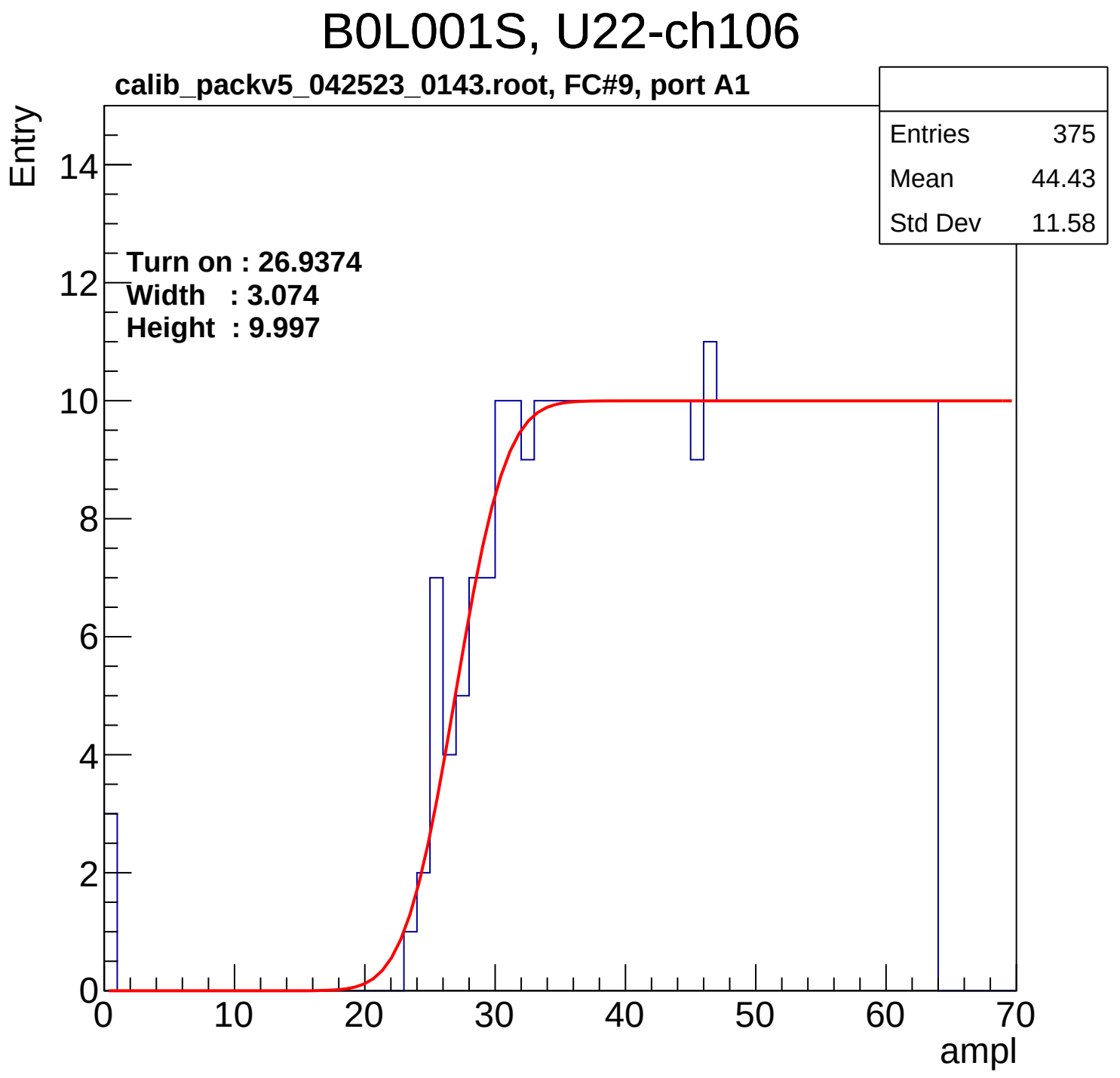
B0L001S, U22-ch106
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.43
Std Dev 11.58
Turn on : 26.9374
Width : 3.074
Height : 9.997
Entry
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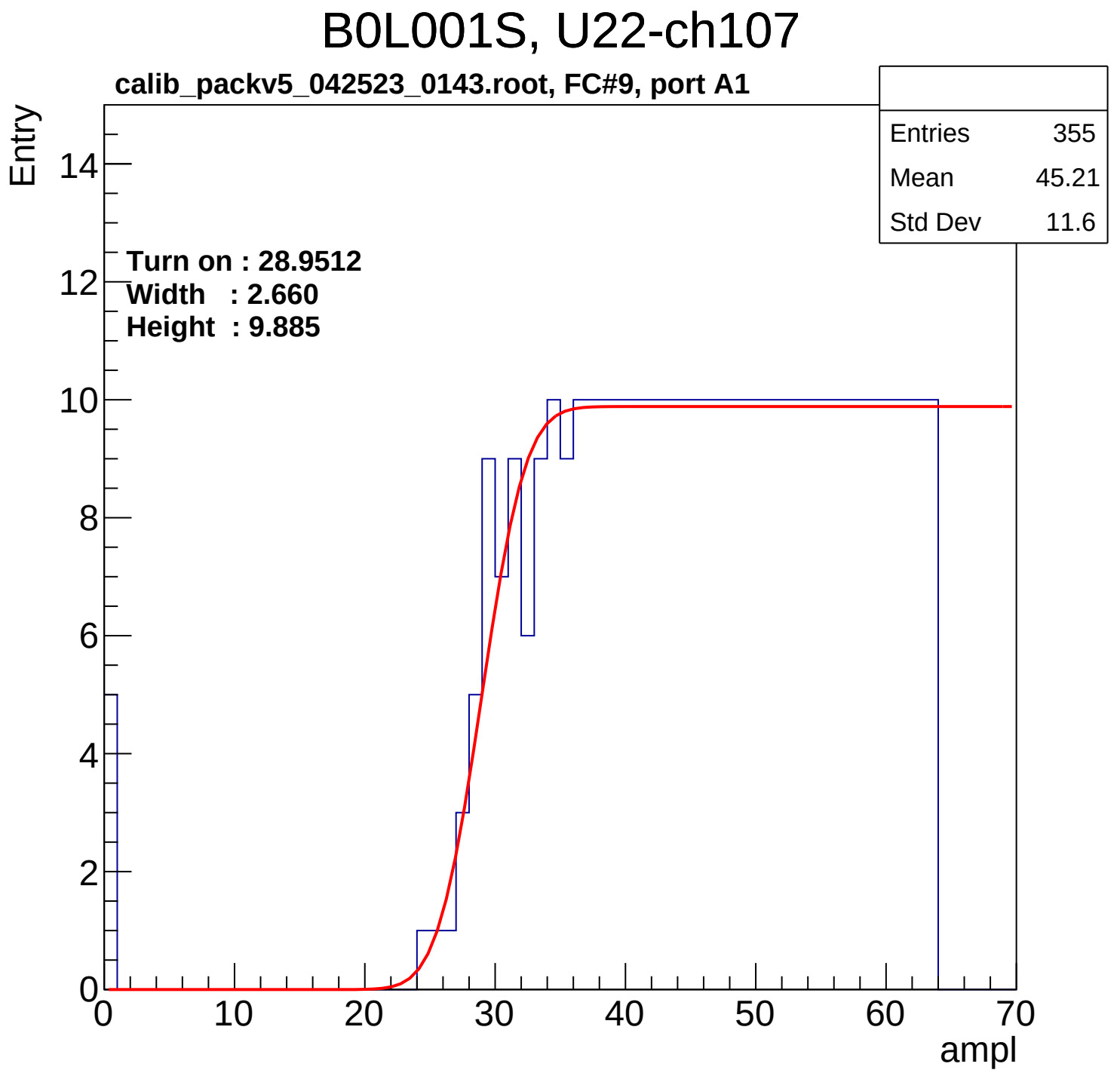
B0L001S, U22-ch107
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.21
Std Dev 11.6
Turn on : 28.9512
Width : 2.660
Height : 9.885
Entry
ampl
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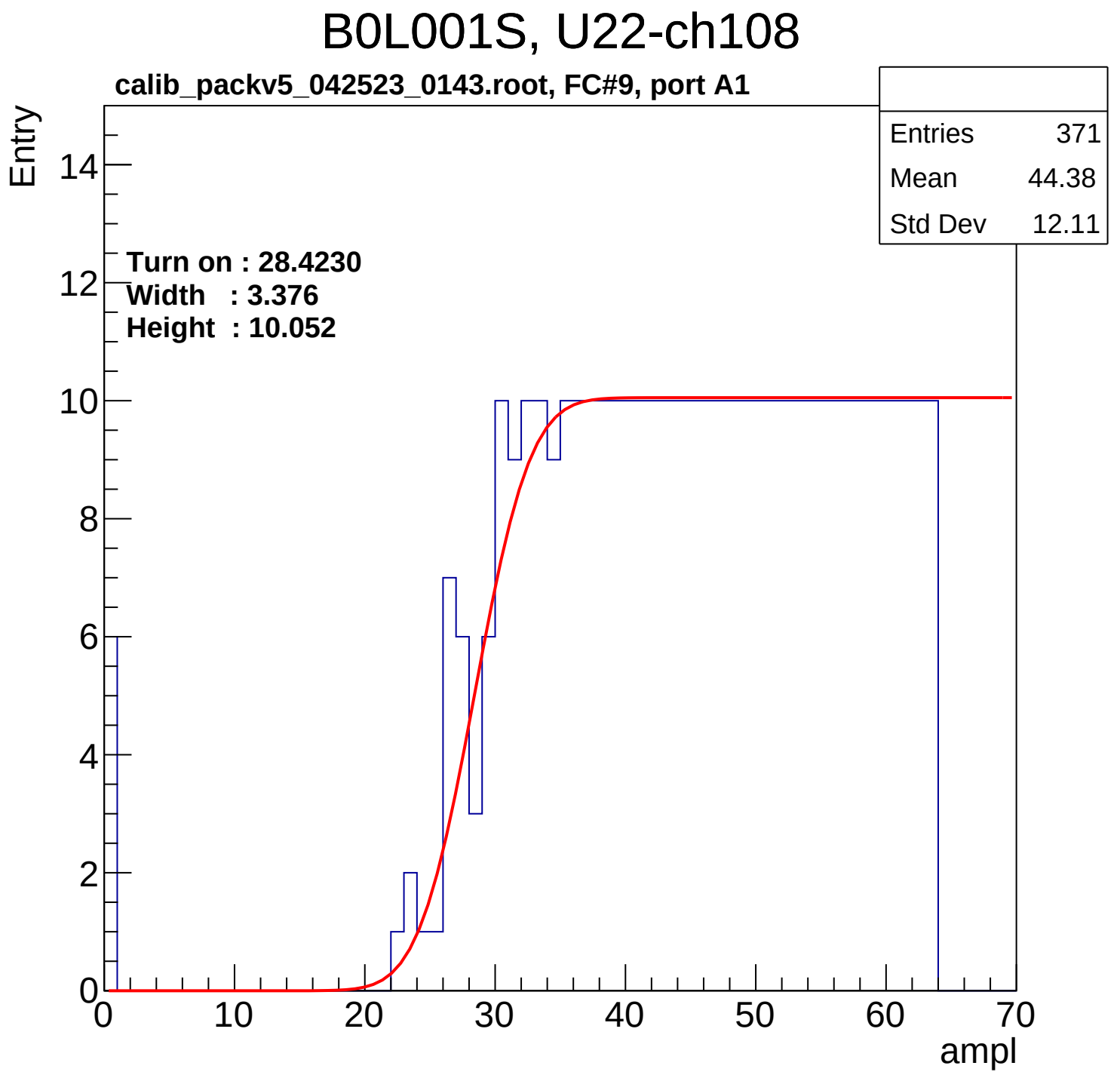
B0L001S, U22-ch108
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.38
Std Dev 12.11
Turn on : 28.4230
Width : 3.376
Height : 10.052
Entry
ampl
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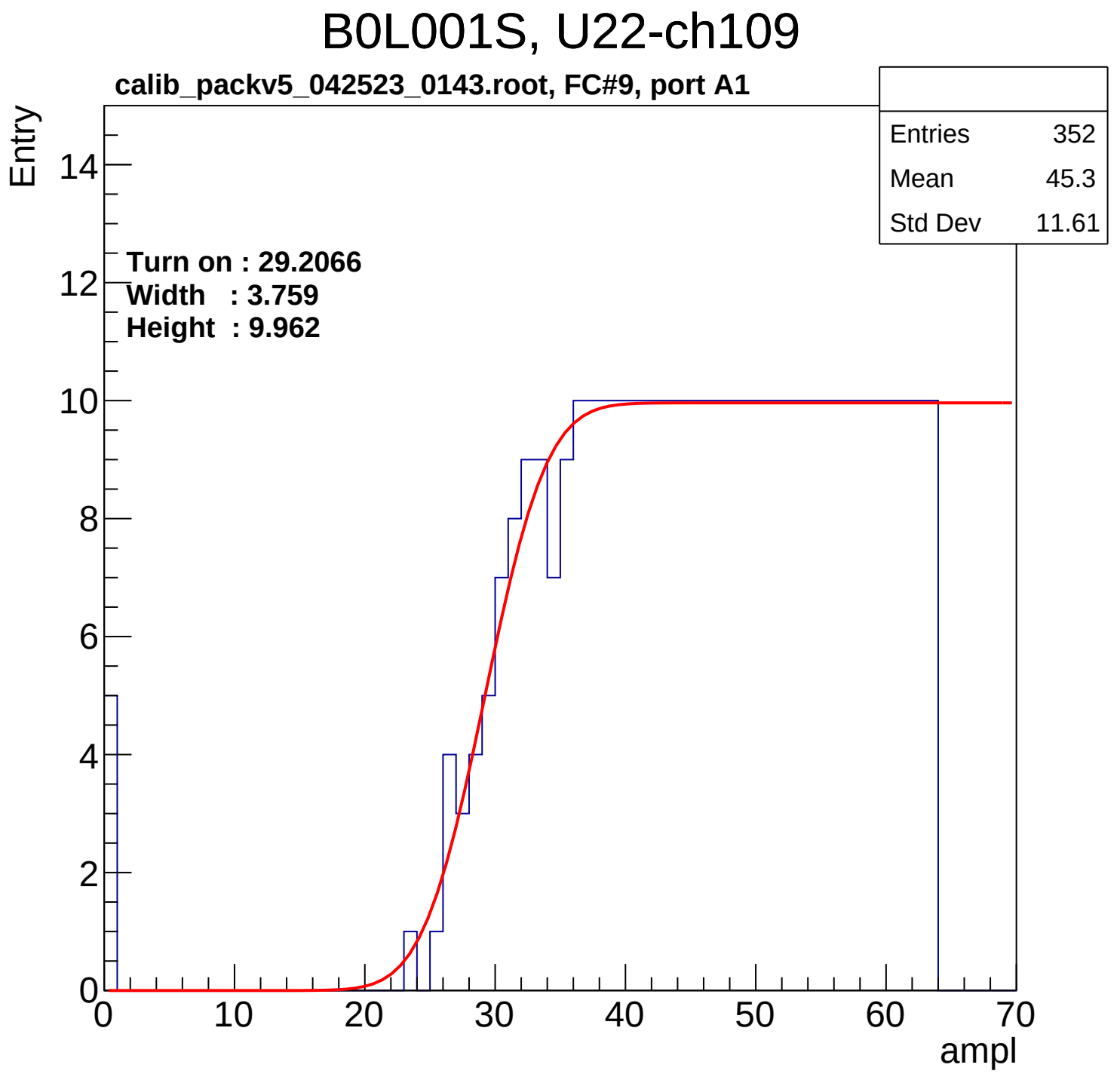
B0L001S, U22-ch109
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.3
Std Dev 11.61
Turn on : 29.2066
Width : 3.759
Height : 9.962
Entry
ampl
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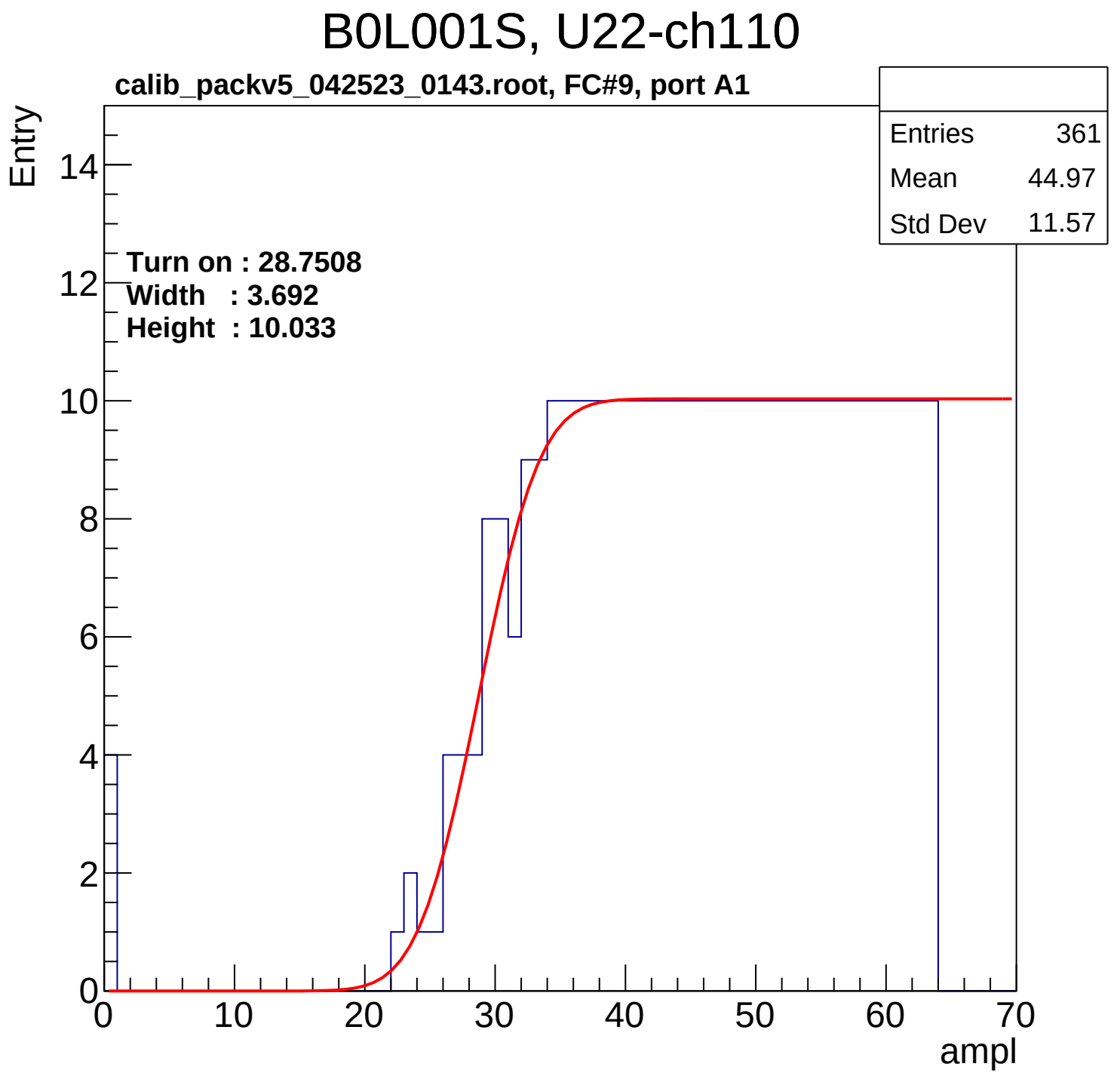
B0L001S, U22-ch110
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 44.97
Std Dev 11.57
Turn on : 28.7508
Width : 3.692
Height : 10.033
Entry
ampl
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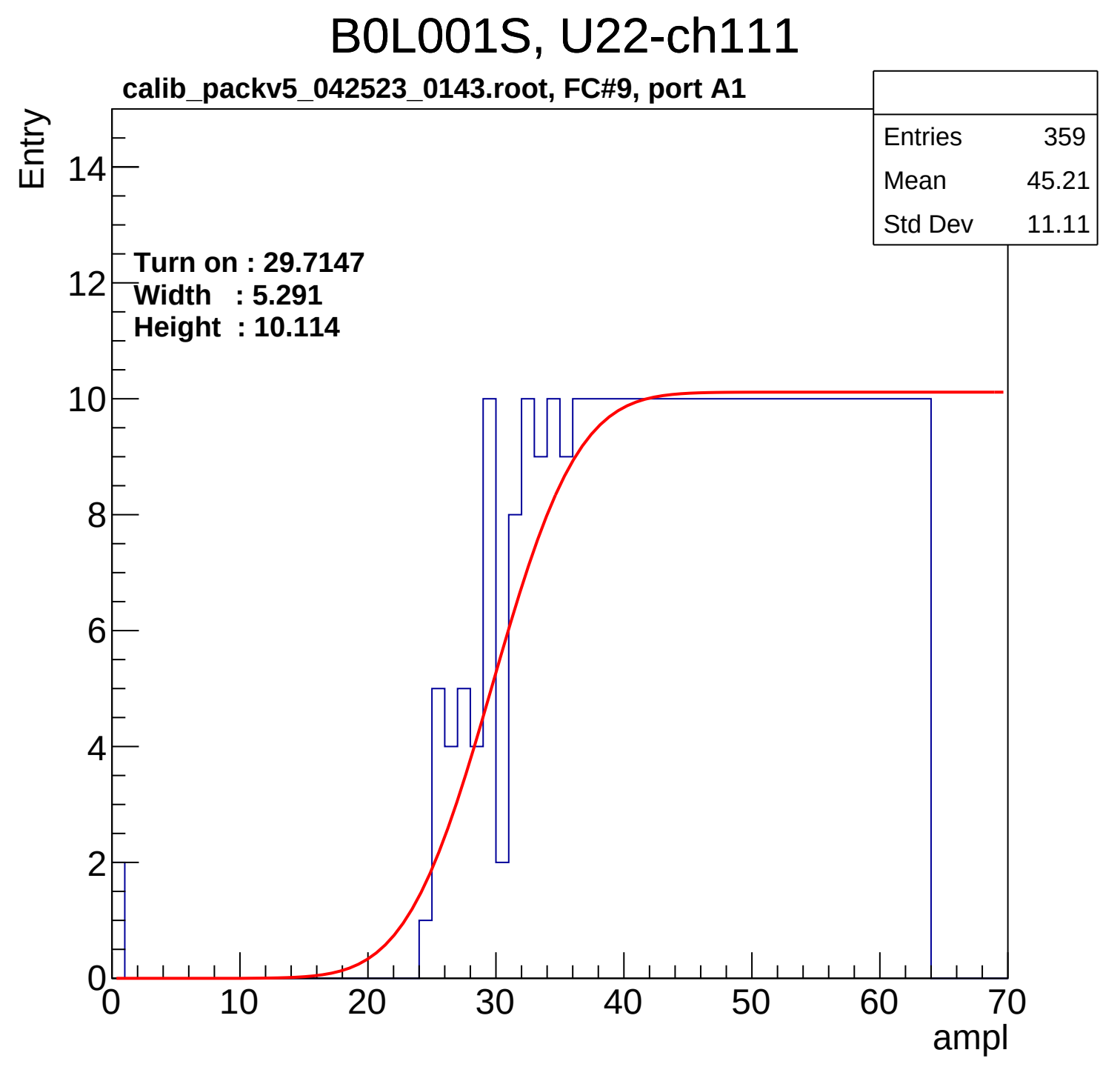
B0L001S, U22-ch111
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.21
Std Dev 11.11
Turn on : 29.7147
Width : 5.291
Height : 10.114
Entry
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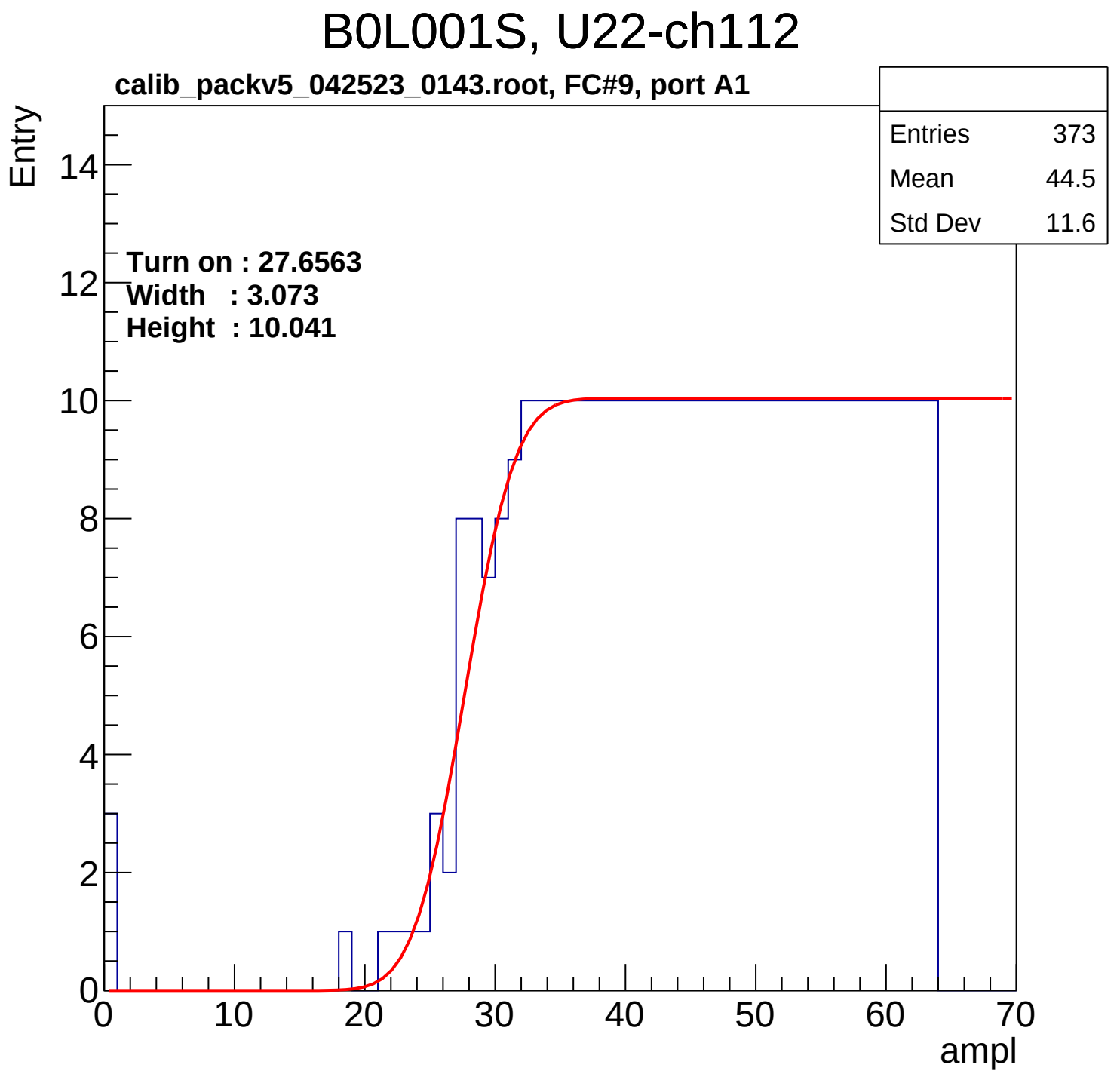
B0L001S, U22-ch112
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.5
Std Dev 11.6
Turn on : 27.6563
Width : 3.073
Height : 10.041
Entry
ampl
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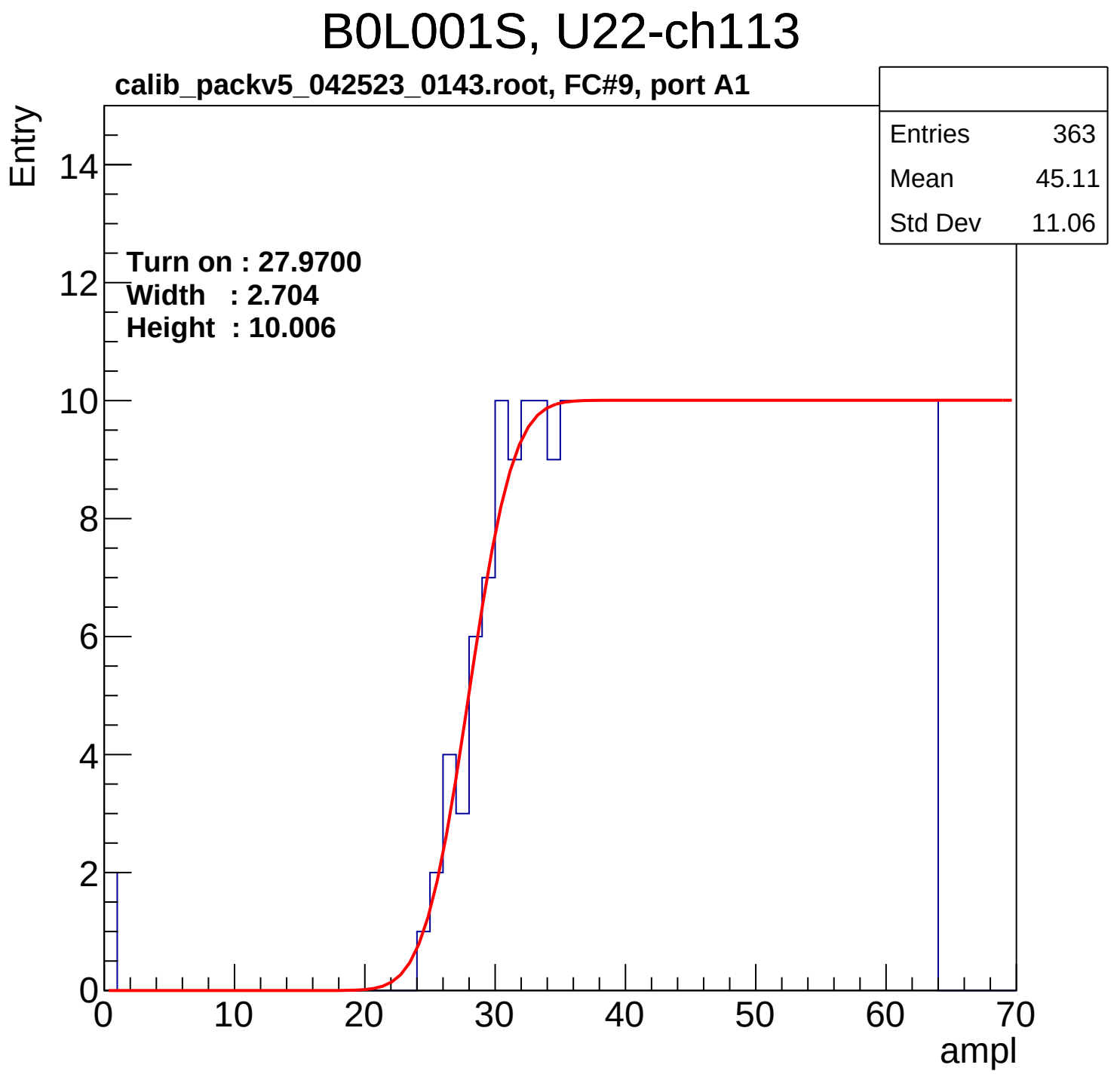
B0L001S, U22-ch113
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.11
Std Dev 11.06
Turn on : 27.9700
Width : 2.704
Height : 10.006
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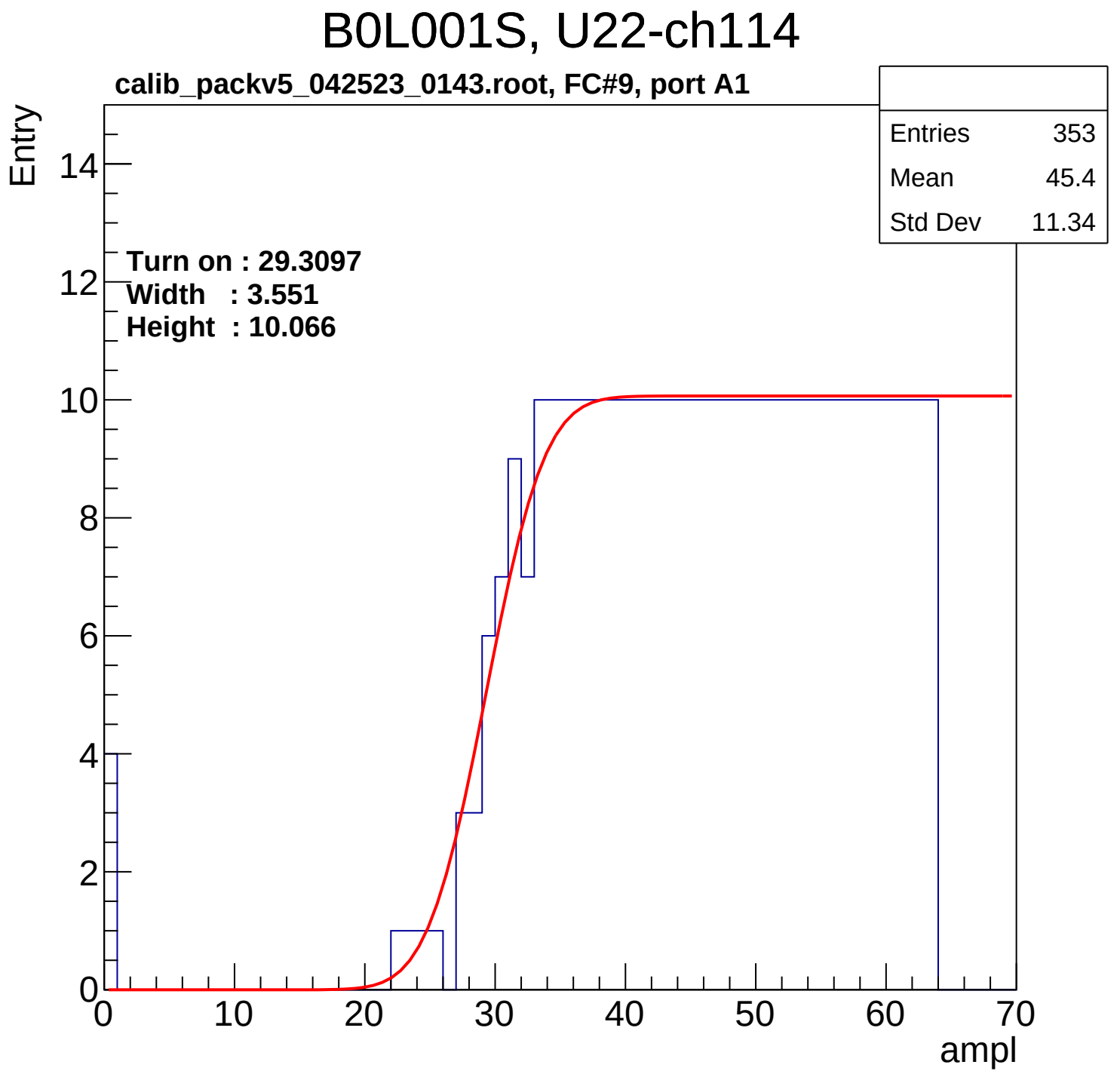
B0L001S, U22-ch114
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.4
Std Dev 11.34
Turn on : 29.3097
Width : 3.551
Height : 10.066
Entry
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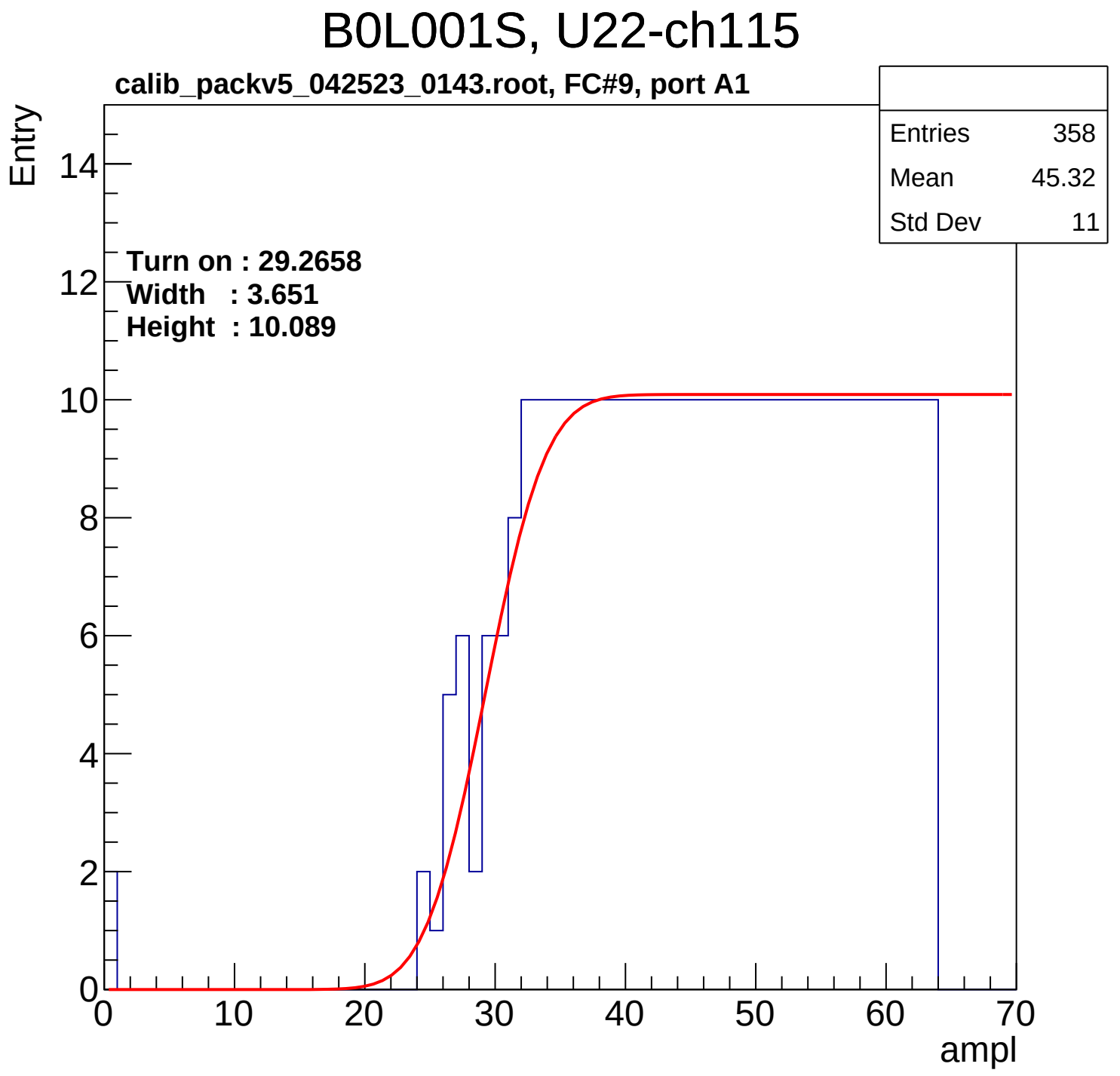
B0L001S, U22-ch115
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.32
Std Dev 11
Turn on : 29.2658
Width : 3.651
Height : 10.089
Entry
ampl
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6
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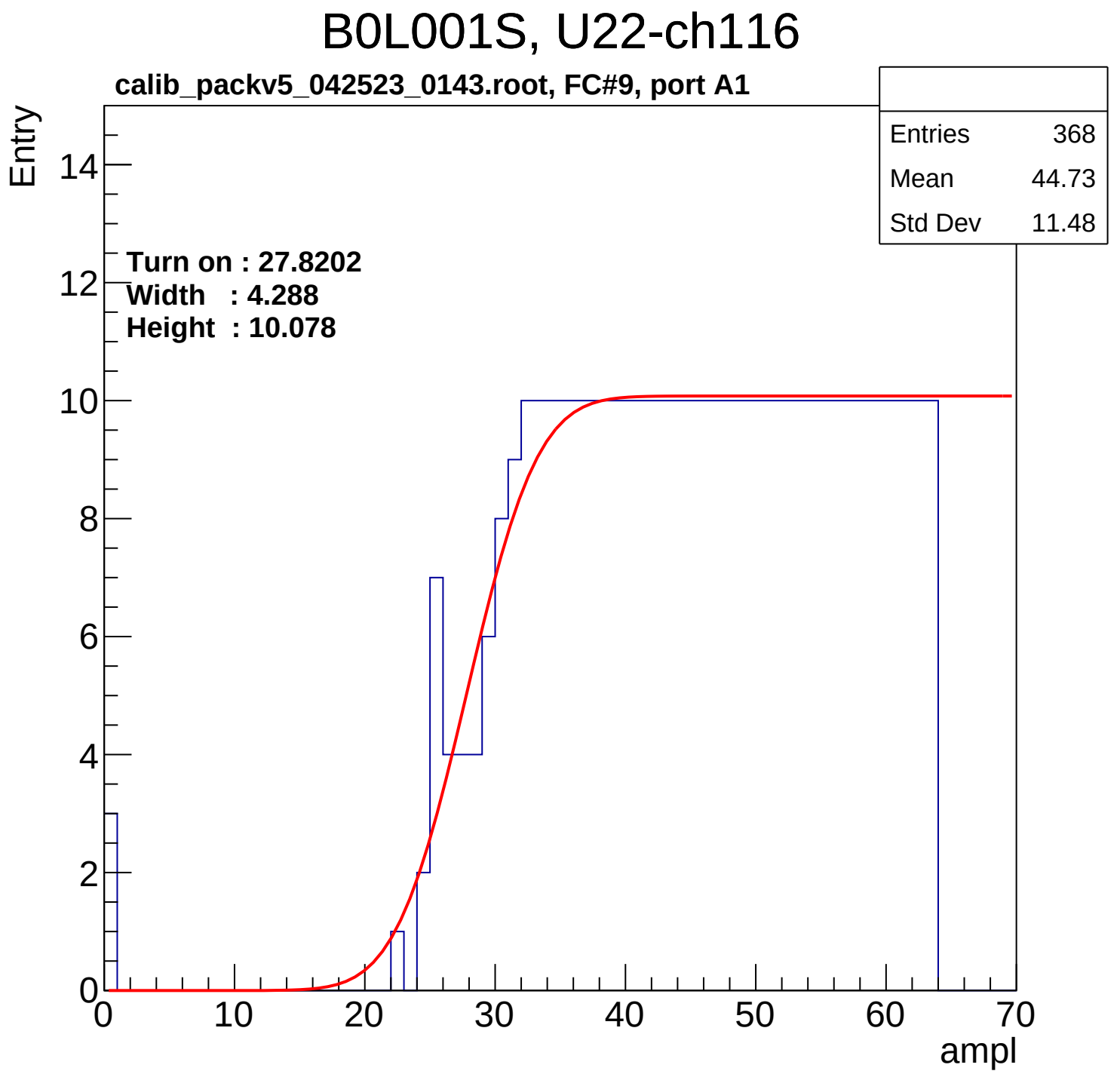
B0L001S, U22-ch116
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.73
Std Dev 11.48
Turn on : 27.8202
Width : 4.288
Height : 10.078
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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60
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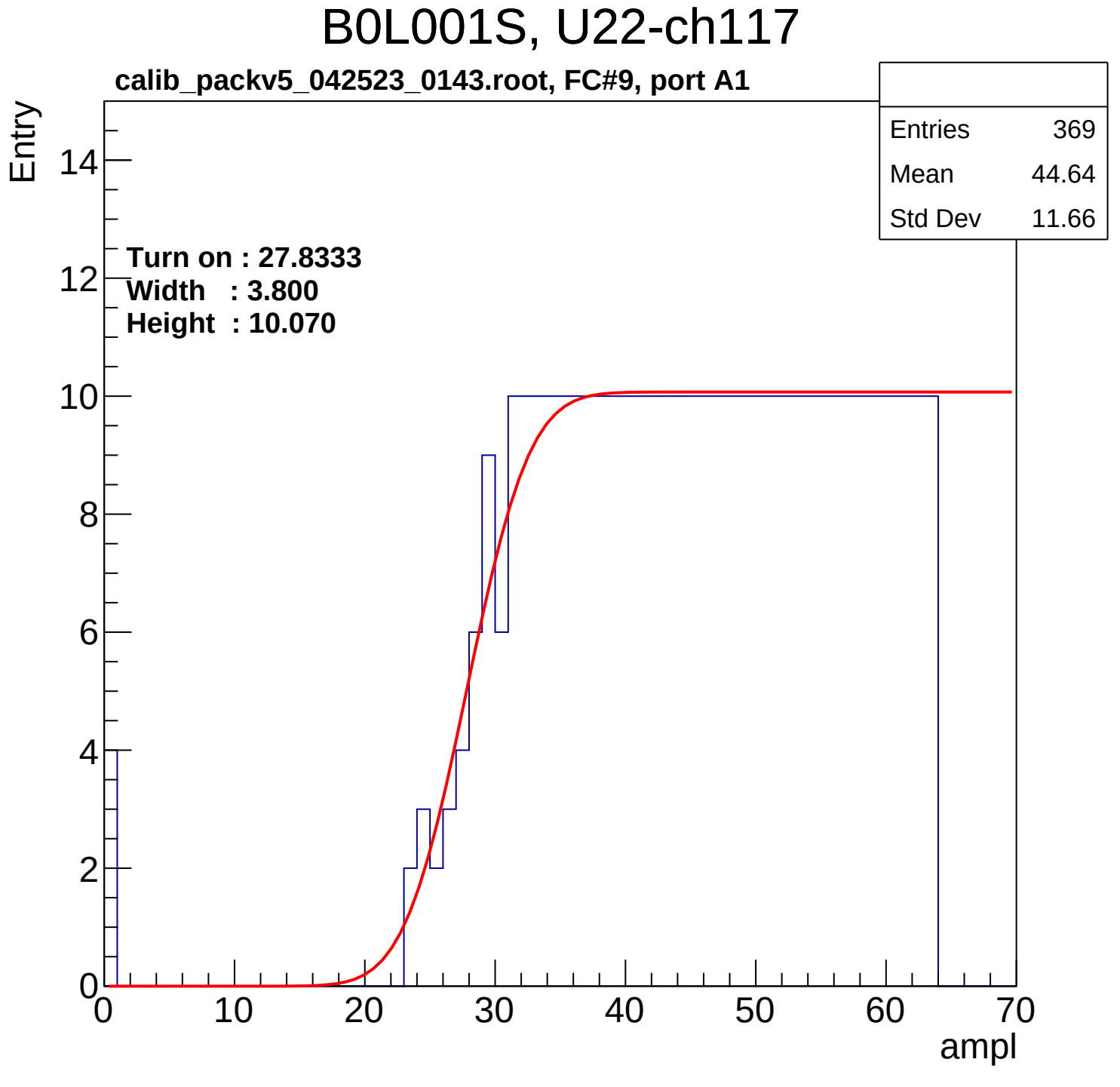
B0L001S, U22-ch117
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.64
Std Dev 11.66
Turn on : 27.8333
Width : 3.800
Height : 10.070
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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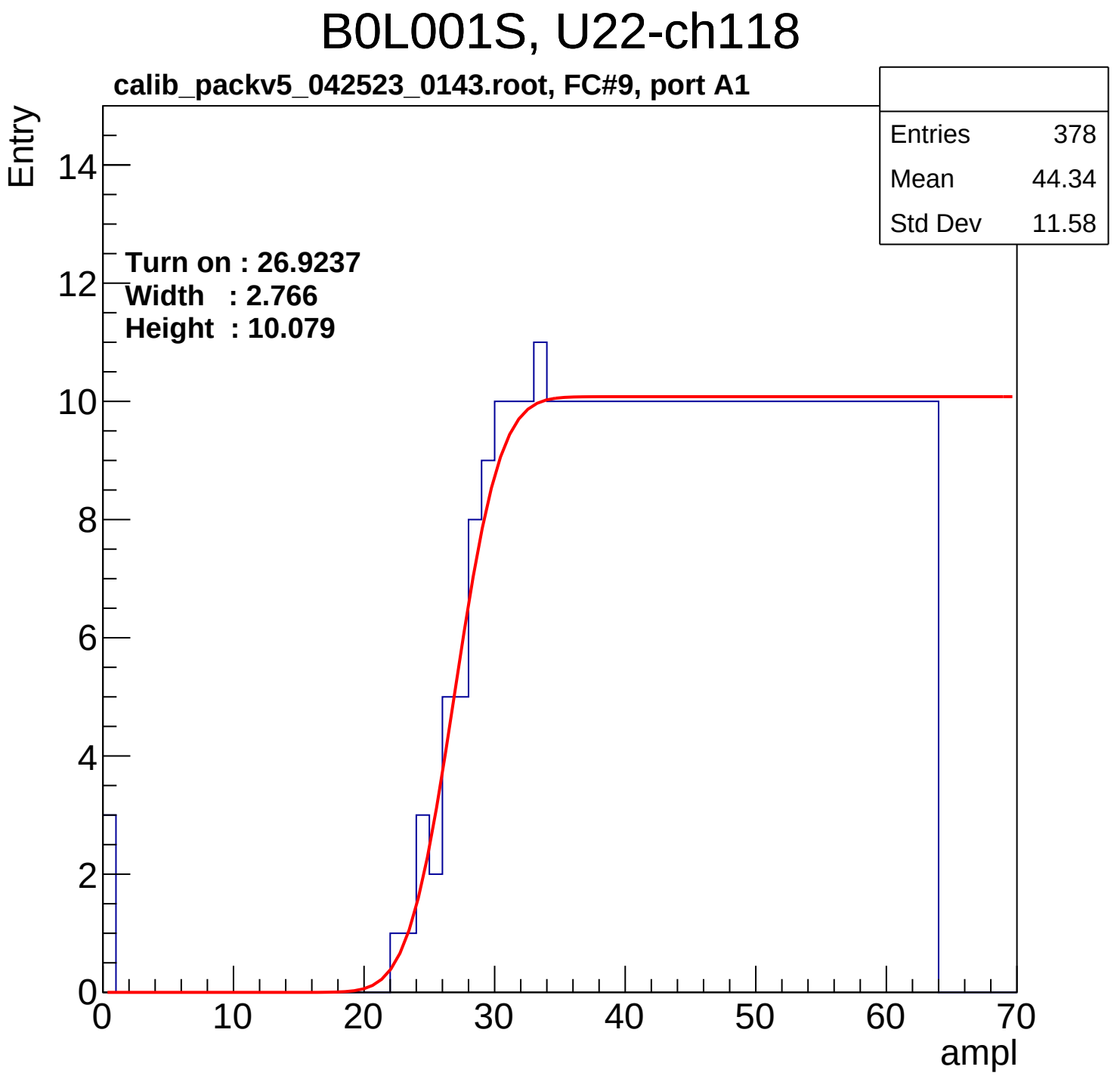
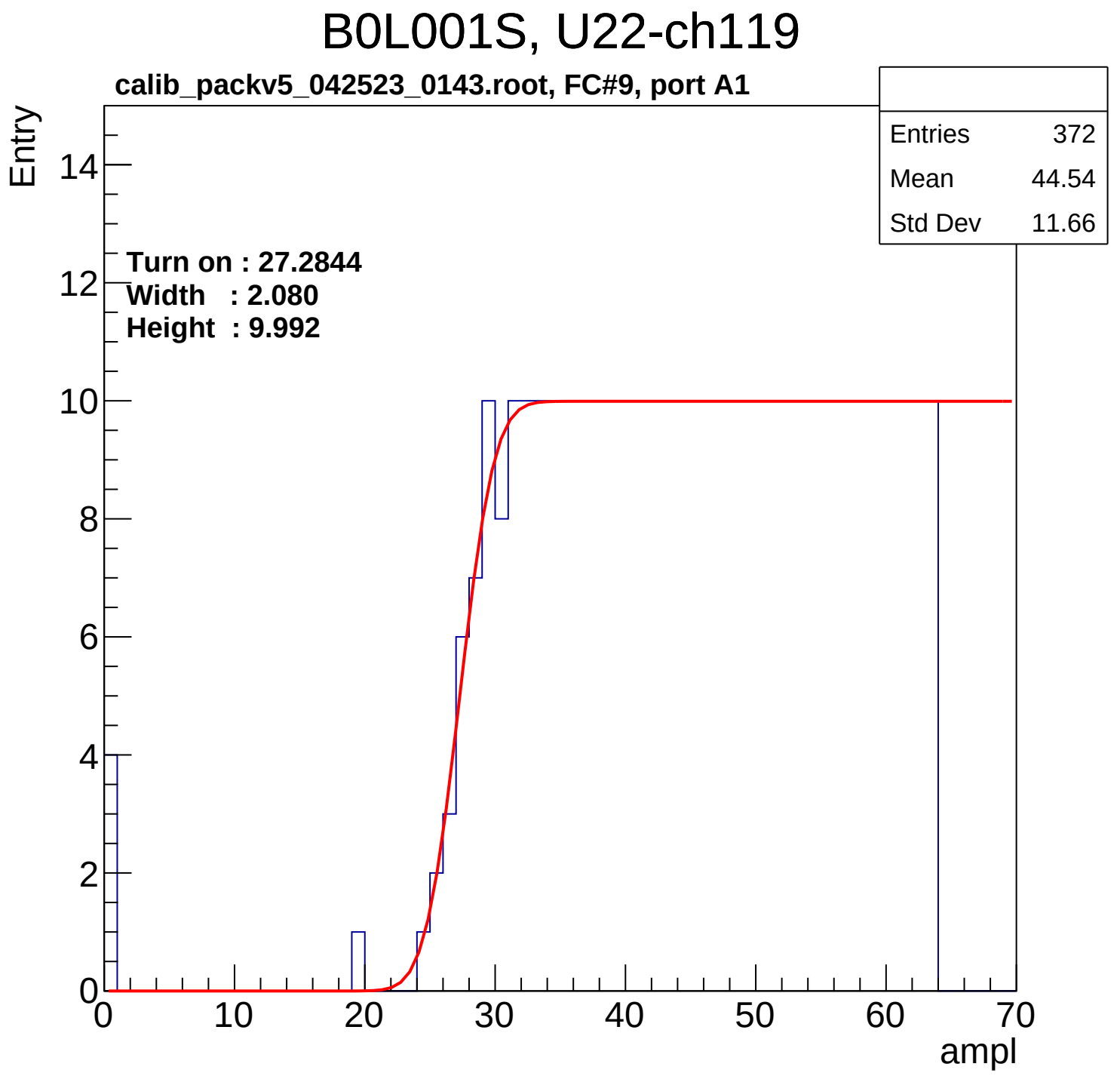
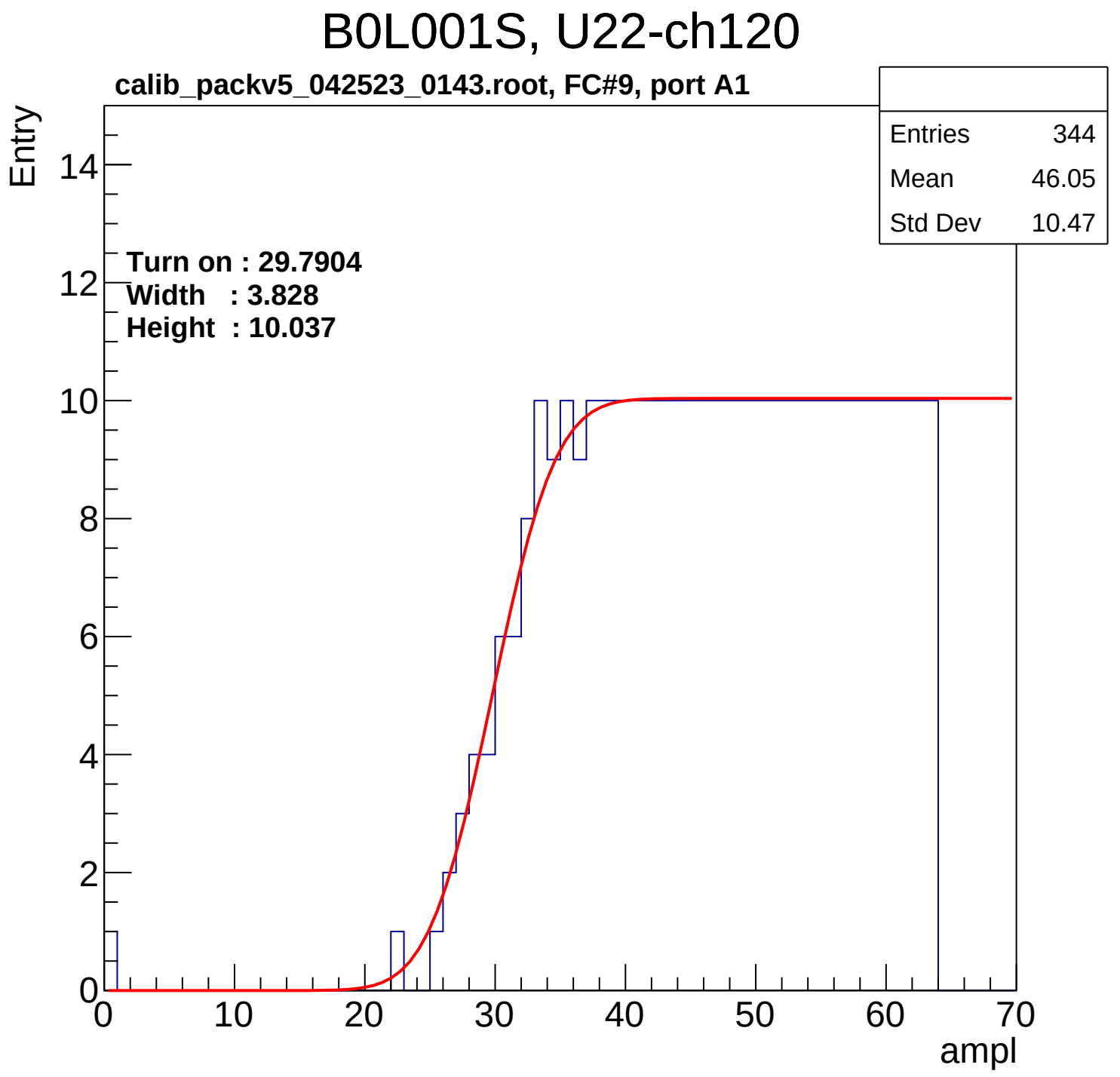
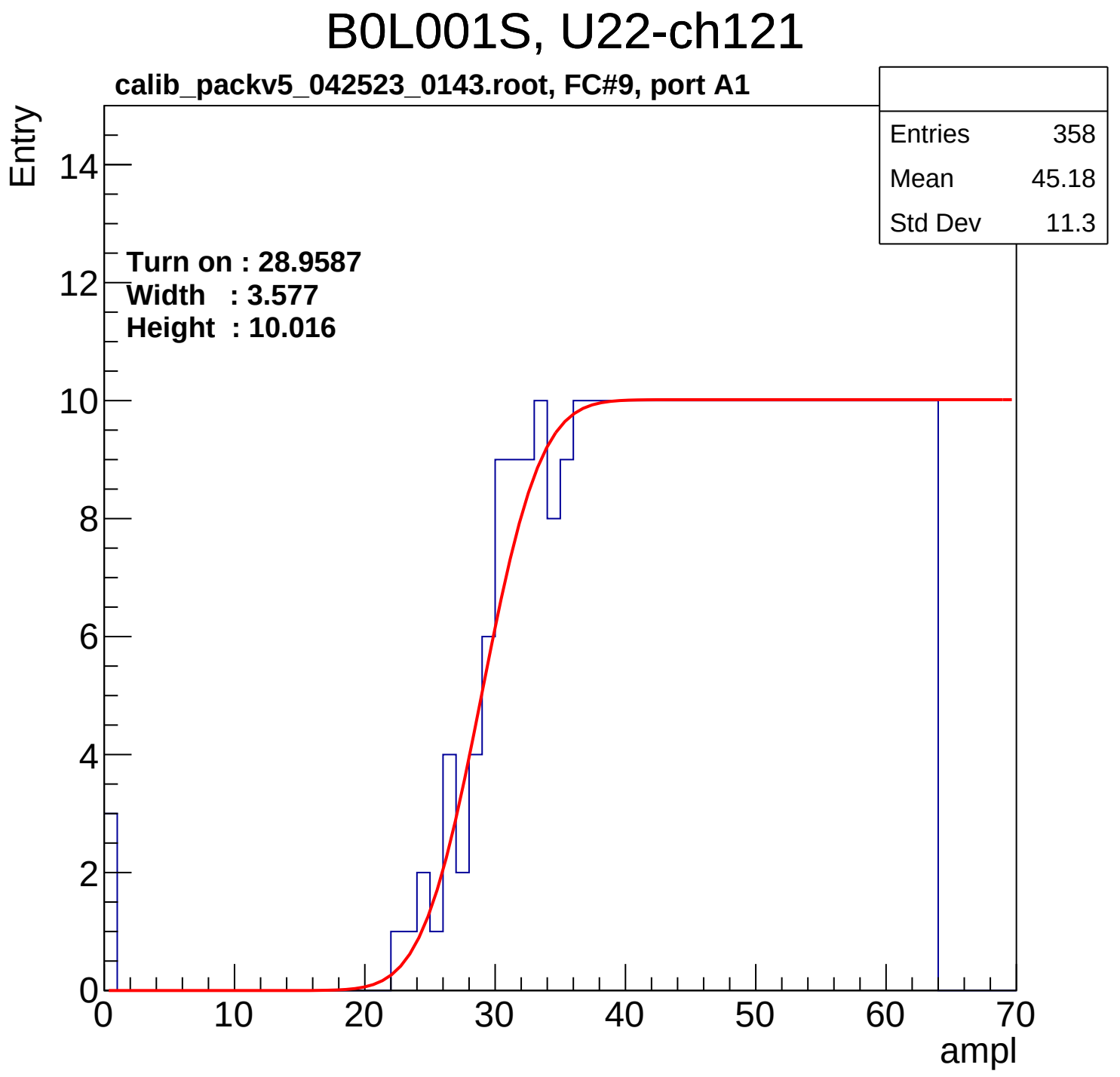
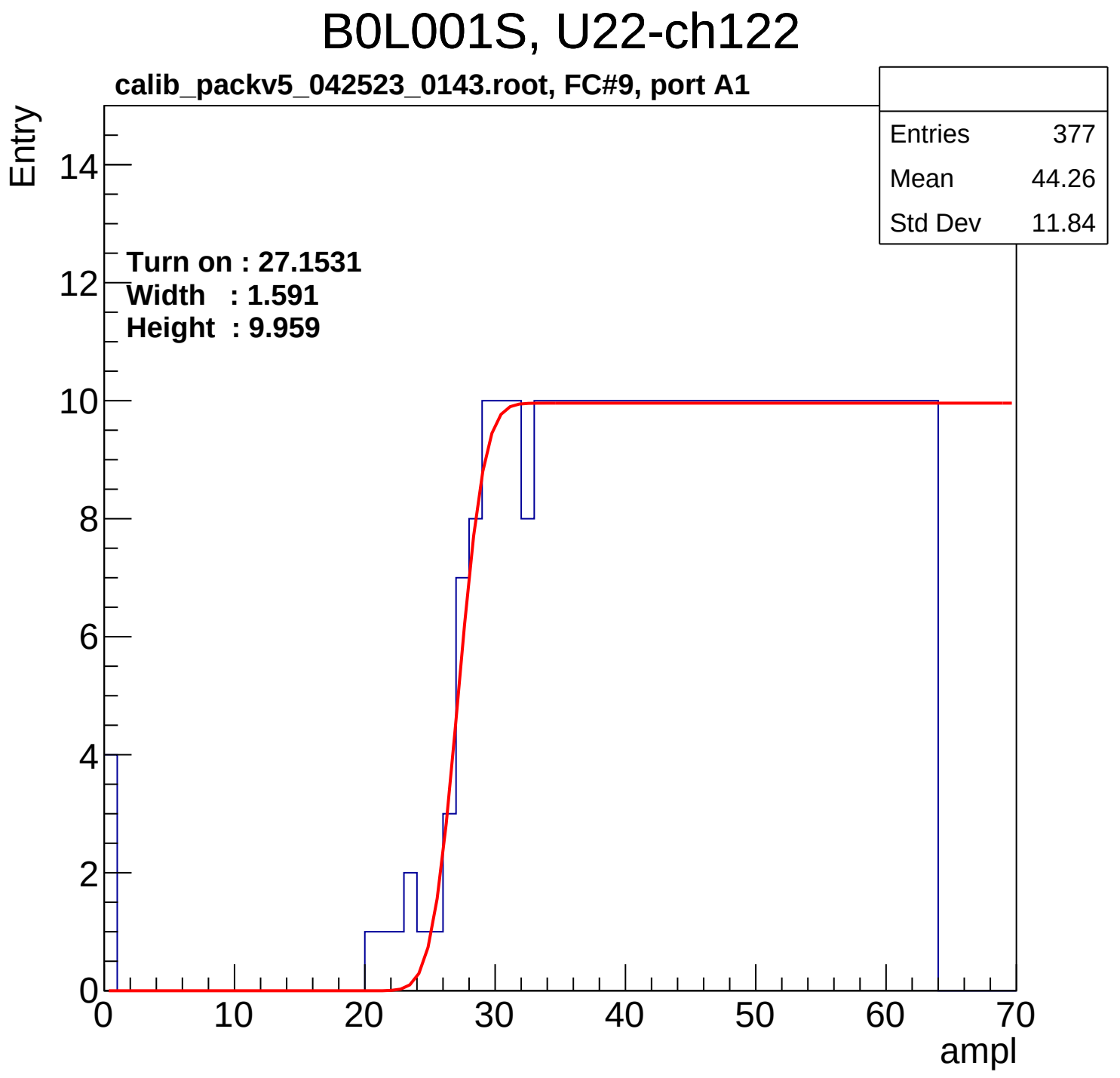
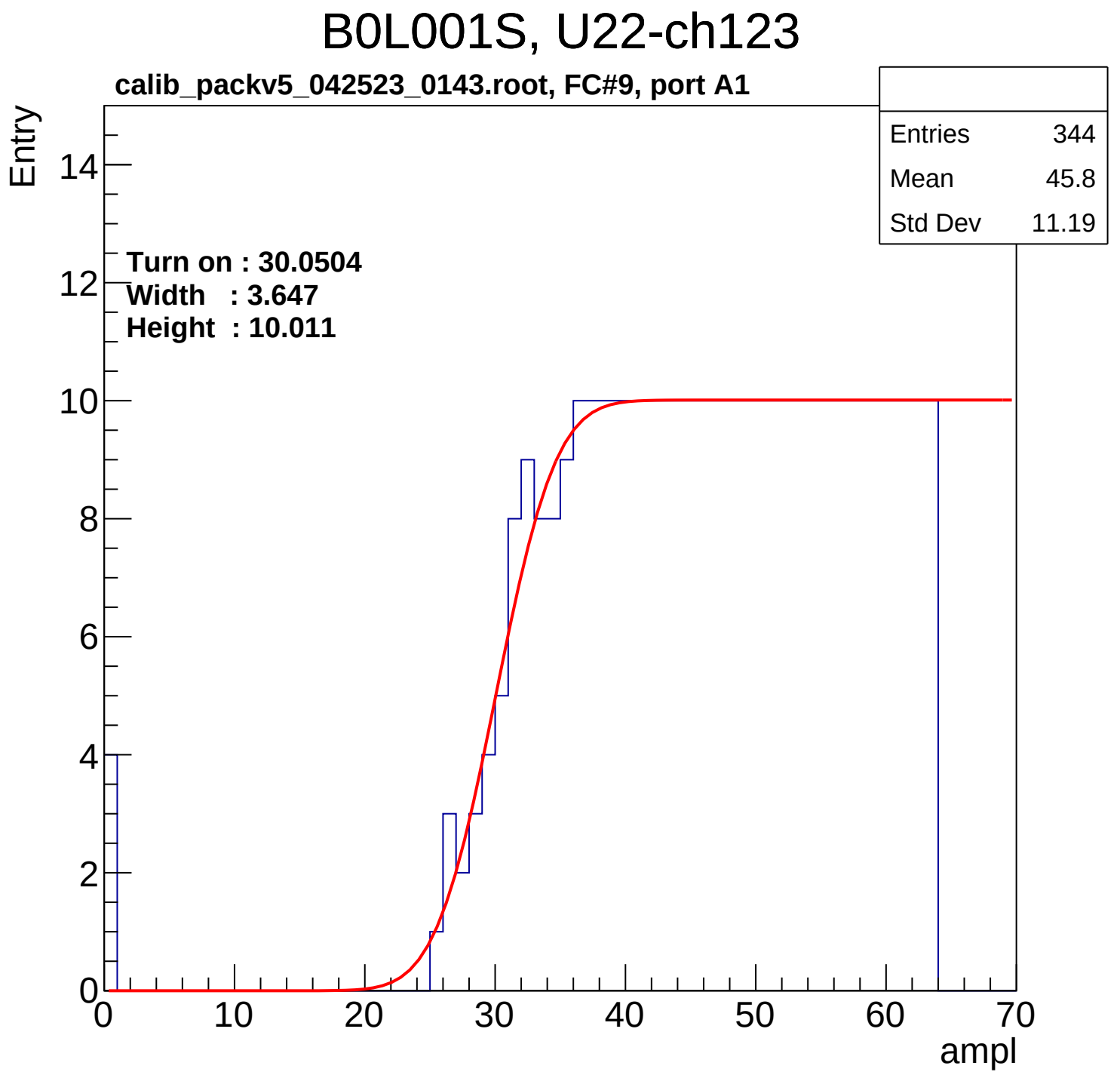

B0L001S, U22-ch118
calib_packv5_042523_0143.root, FC#9, port A1
Entries 378
Mean 44.34
Std Dev 11.58
Turn on : 26.9237
Width : 2.766
Height : 10.079
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

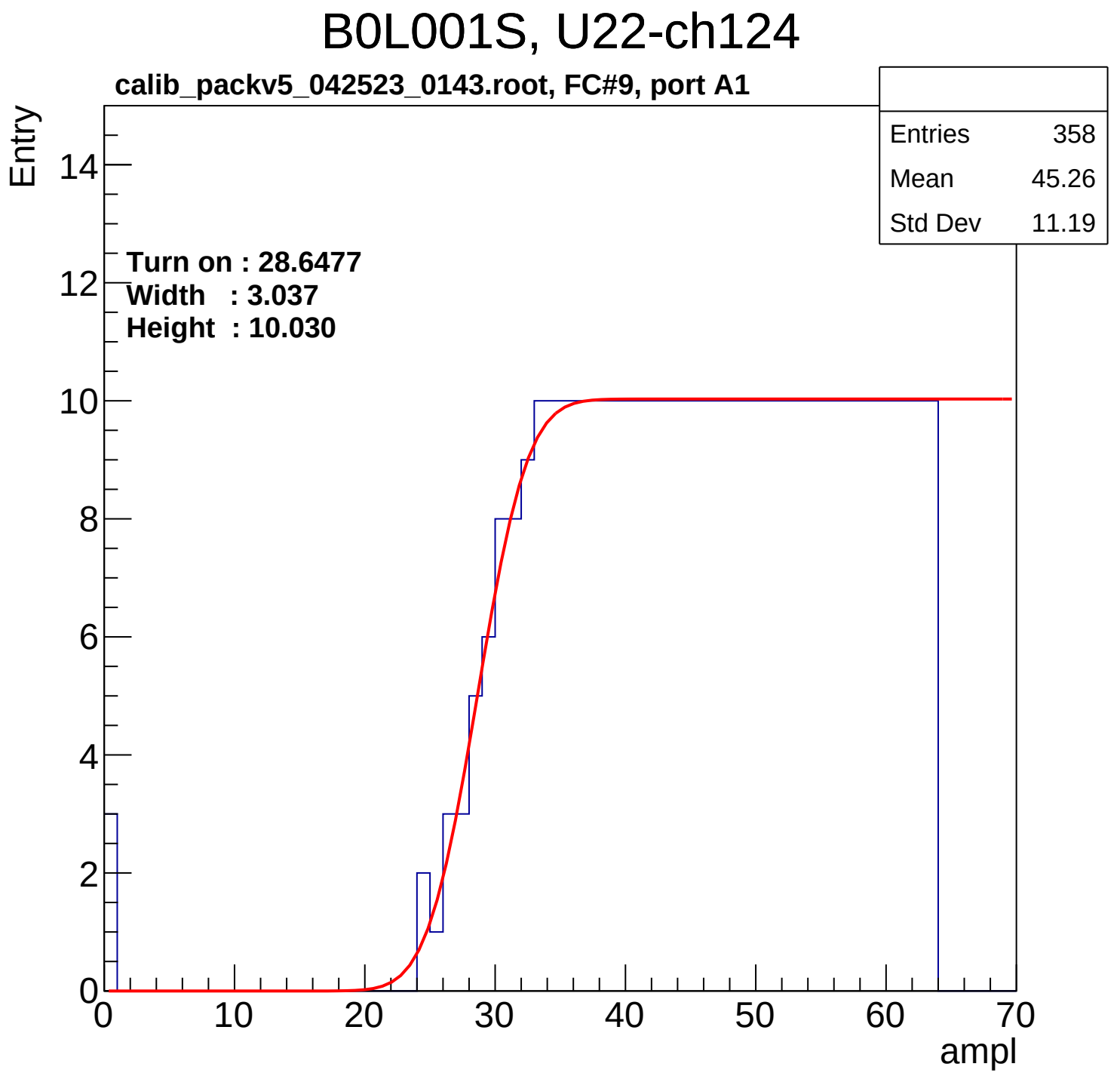

B0L001S, U22-ch119
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.54
Std Dev 11.66
Turn on : 27.2844
Width : 2.080
Height : 9.992
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

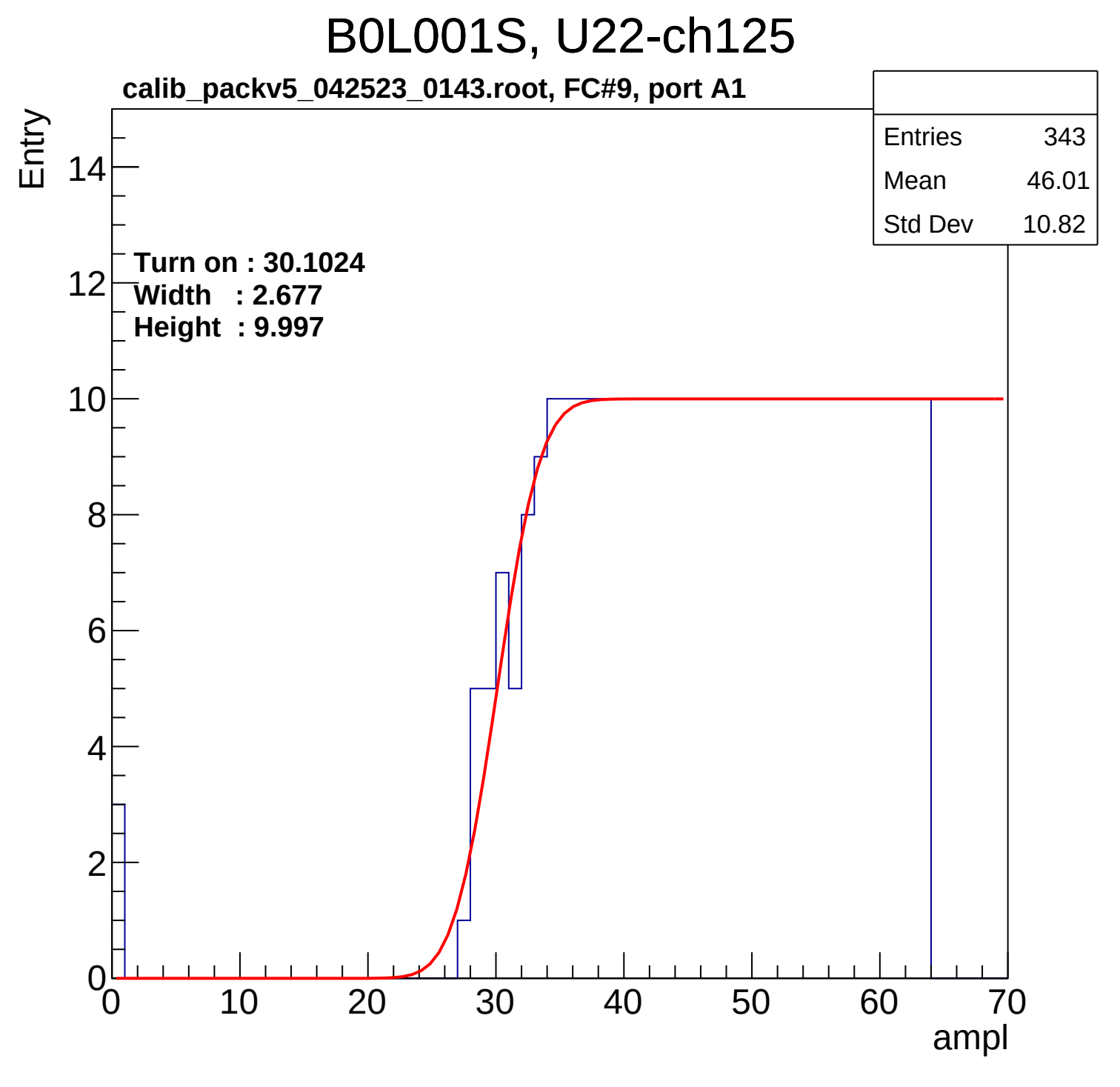

B0L001S, U22-ch120
calib_packv5_042523_0143.root, FC#9, port A1
Entries 344
Mean 46.05
Std Dev 10.47
Turn on : 29.7904
Width : 3.828
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

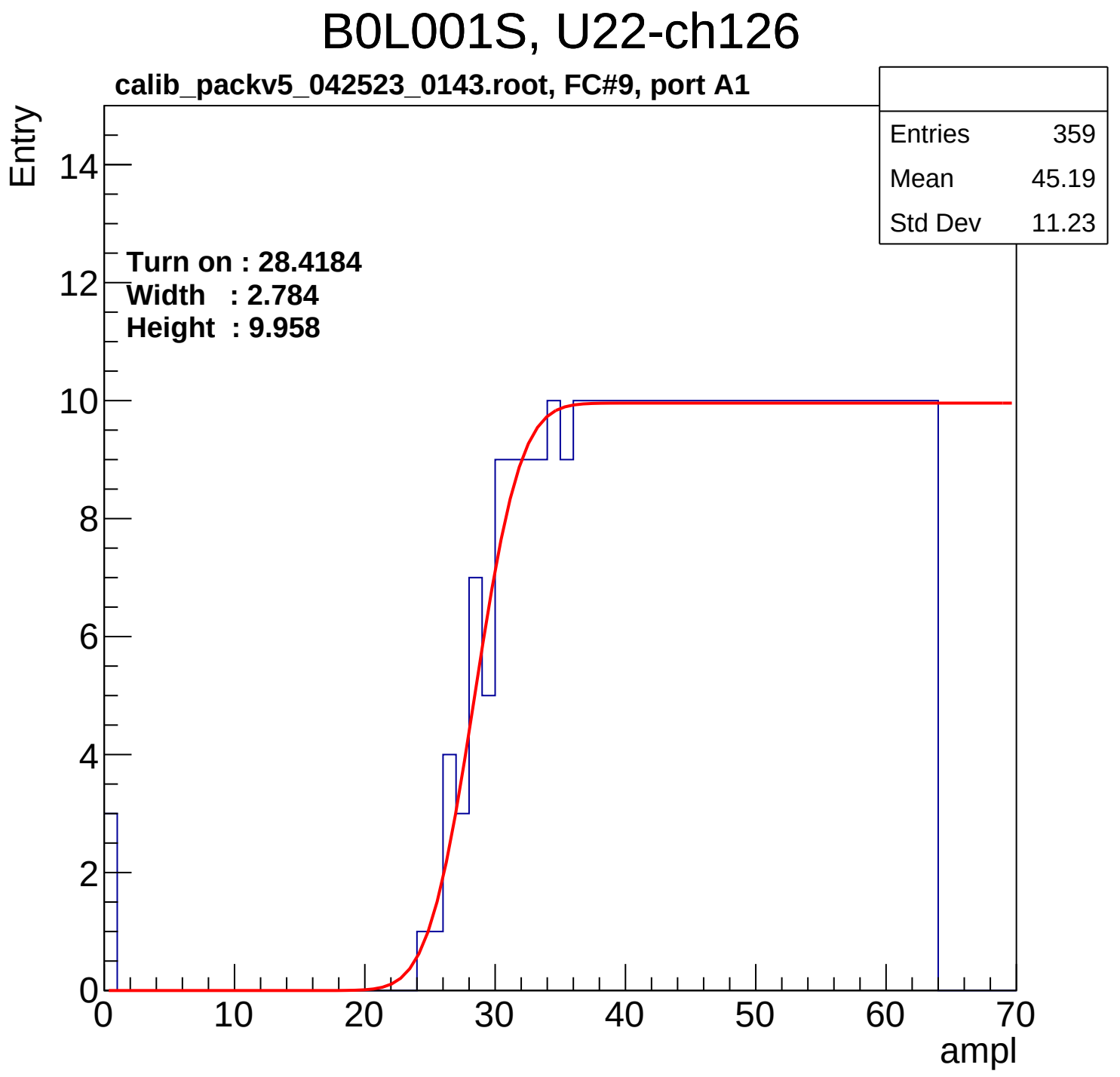

B0L001S, U22-ch121
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.18
Std Dev 11.3
Turn on : 28.9587
Width : 3.577
Height : 10.016
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

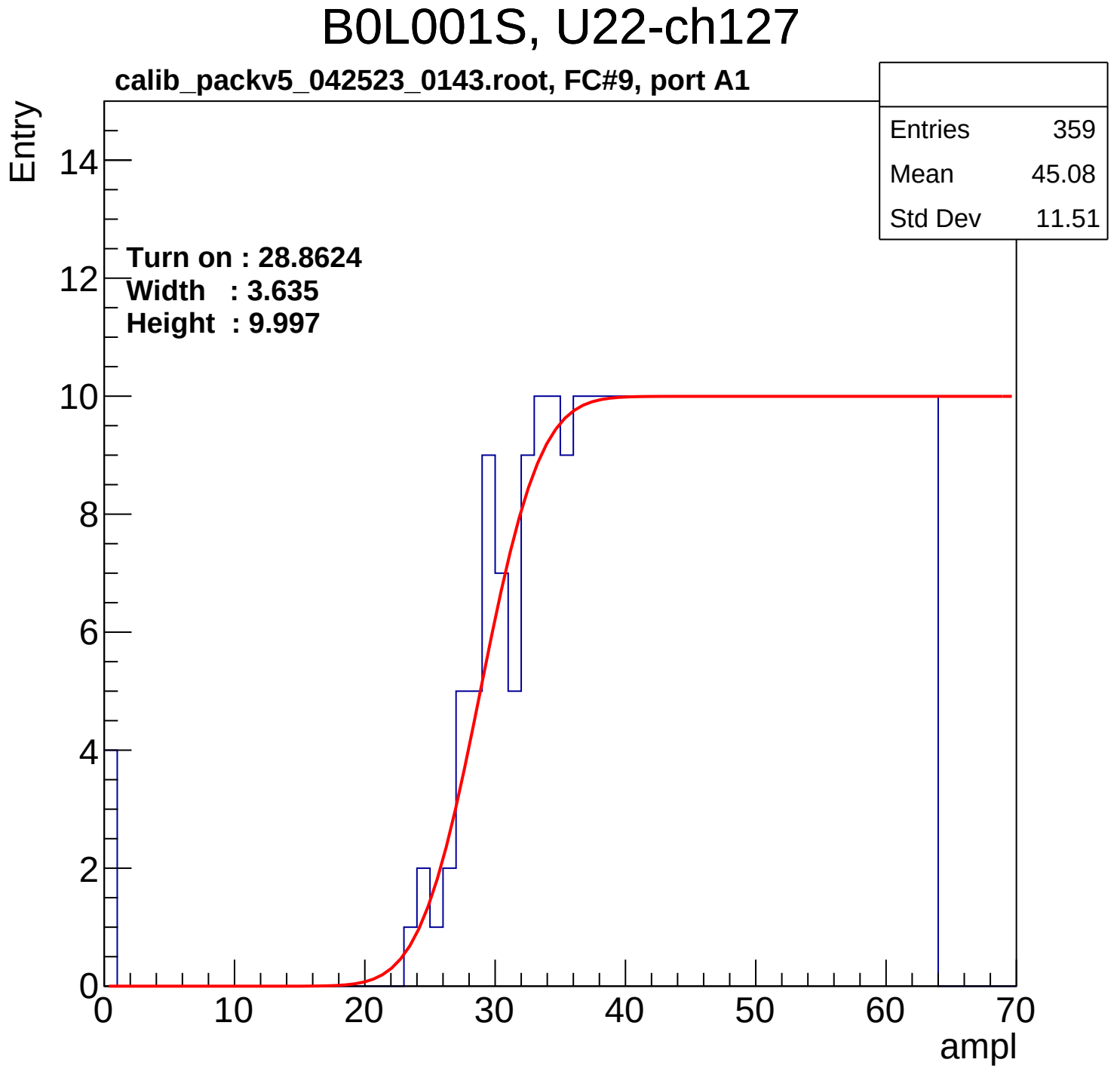

B0L001S, U22-ch122
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.26
Std Dev 11.84
Turn on : 27.1531
Width : 1.591
Height : 9.959
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

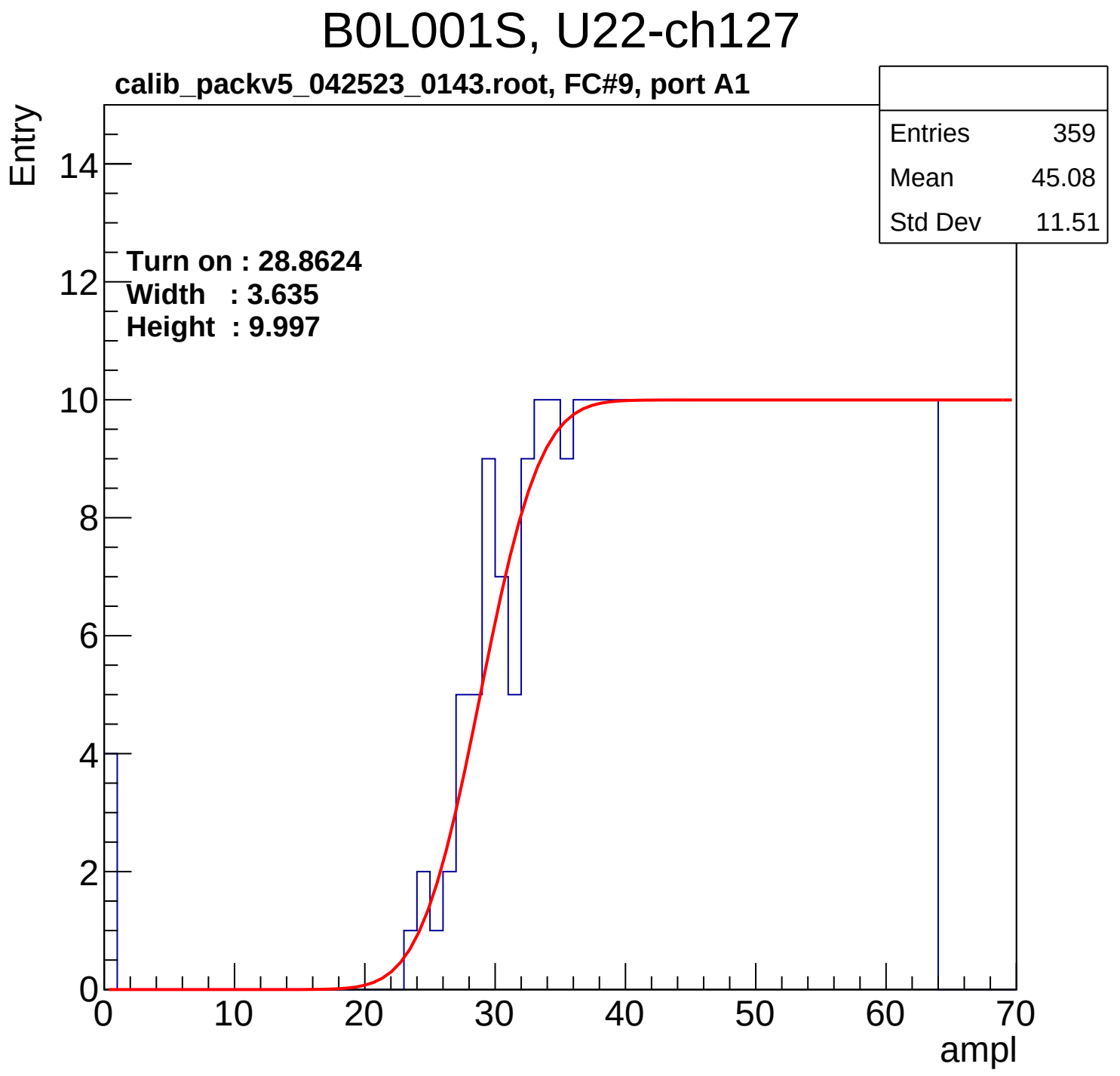

B0L001S, U22-ch123
calib_packv5_042523_0143.root, FC#9, port A1
Entries 344
Mean 45.8
Std Dev 11.19
Turn on : 30.0504
Width : 3.647
Height : 10.011
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U22-ch124
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.26
Std Dev 11.19
Turn on : 28.6477
Width : 3.037
Height : 10.030
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U22-ch125
calib_packv5_042523_0143.root, FC#9, port A1
Entries 343
Mean 46.01
Std Dev 10.82
Turn on : 30.1024
Width : 2.677
Height : 9.997
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U22-ch126
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.19
Std Dev 11.23
Turn on : 28.4184
Width : 2.784
Height : 9.958
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U22-ch127
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.08
Std Dev 11.51
Turn on : 28.8624
Width : 3.635
Height : 9.997
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U22-ch127
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.08
Std Dev 11.51
Turn on : 28.8624
Width : 3.635
Height : 9.997
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70