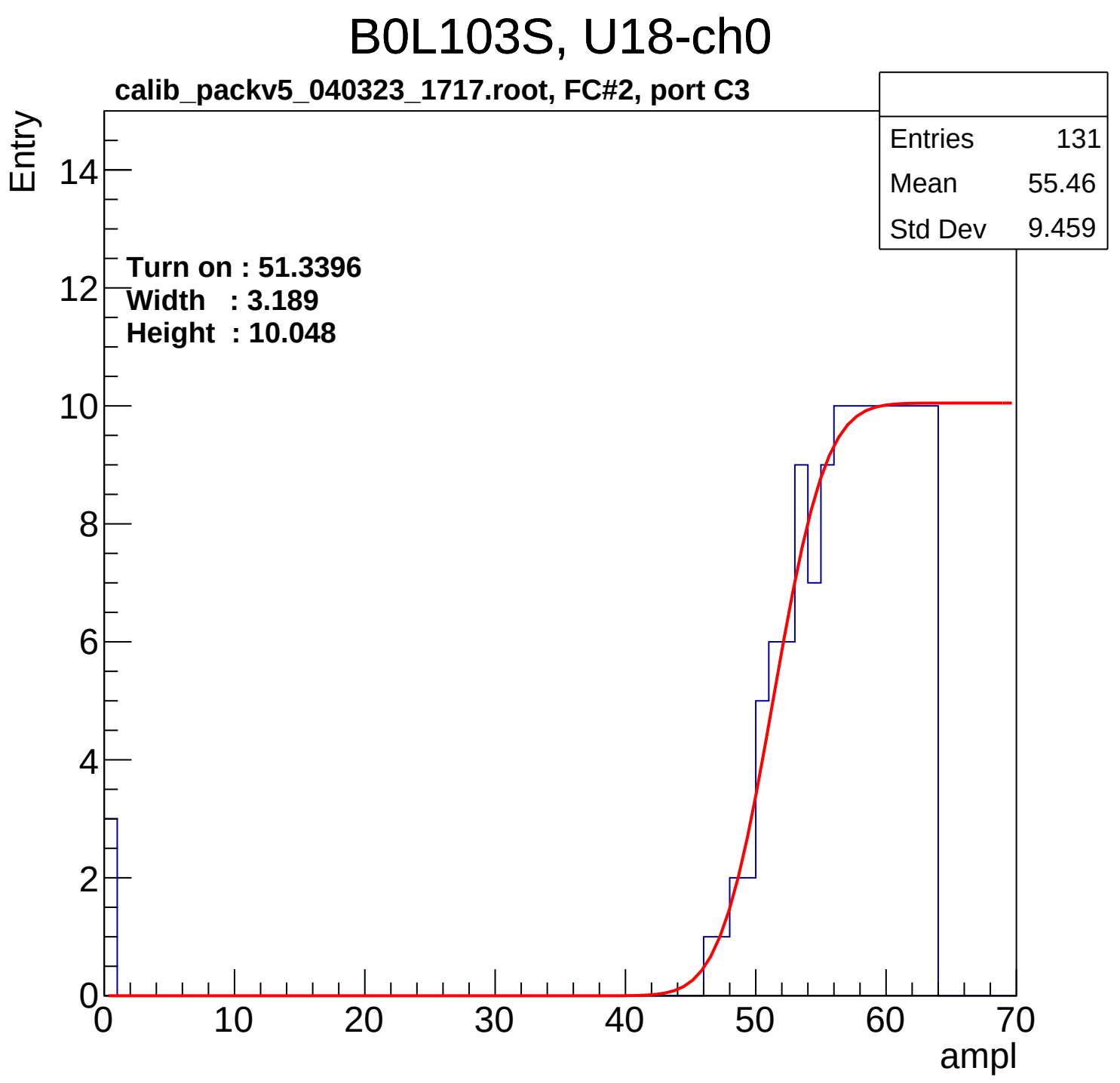
B0L103S, U18-ch0
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 55.46
Std Dev 9.459
Turn on : 51.3396
Width : 3.189
Height : 10.048
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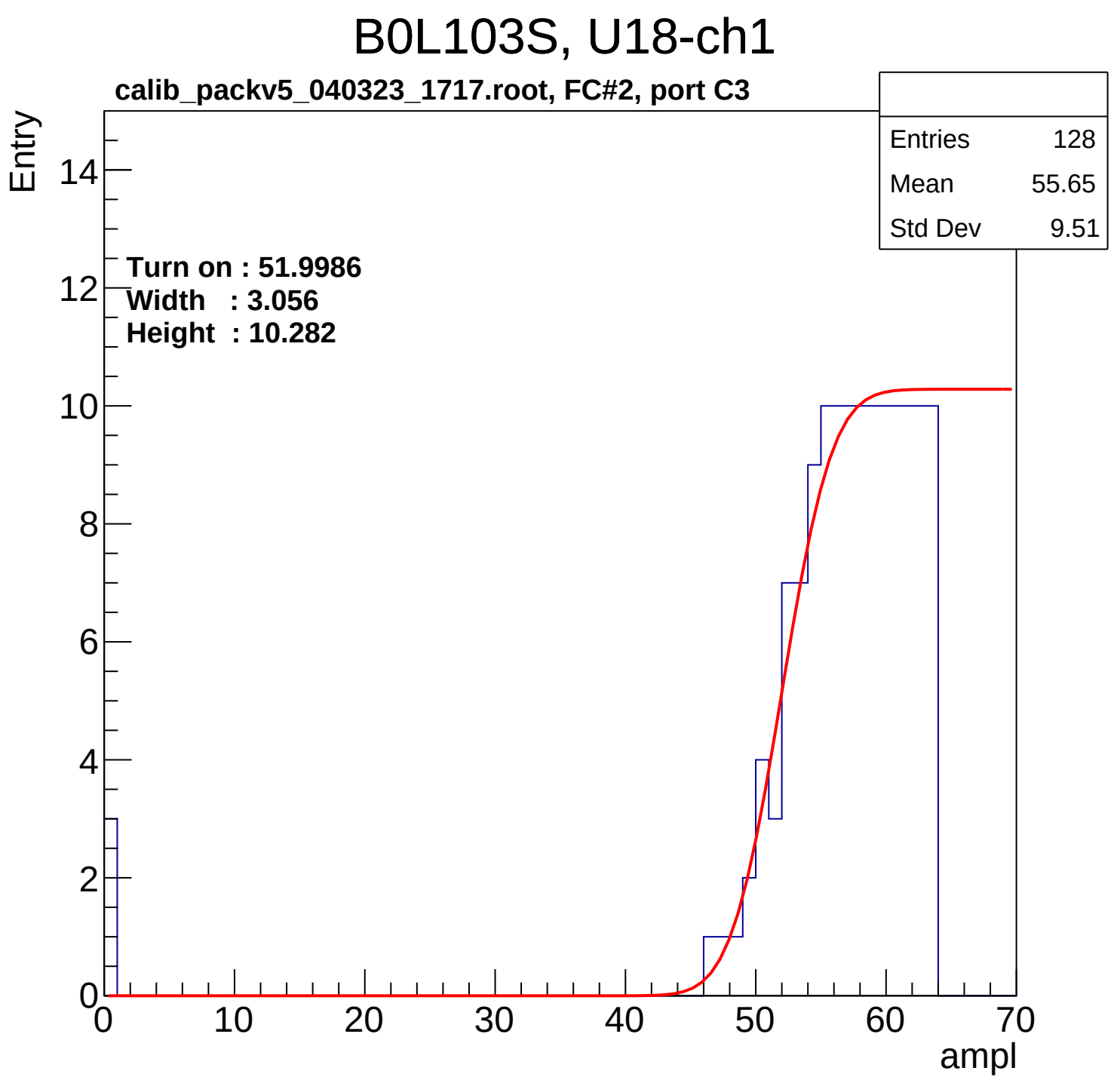
B0L103S, U18-ch1
calib_packv5_040323_1717.root, FC#2, port C3
Entries 128
Mean 55.65
Std Dev 9.51
Turn on : 51.9986
Width : 3.056
Height : 10.282
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ampl
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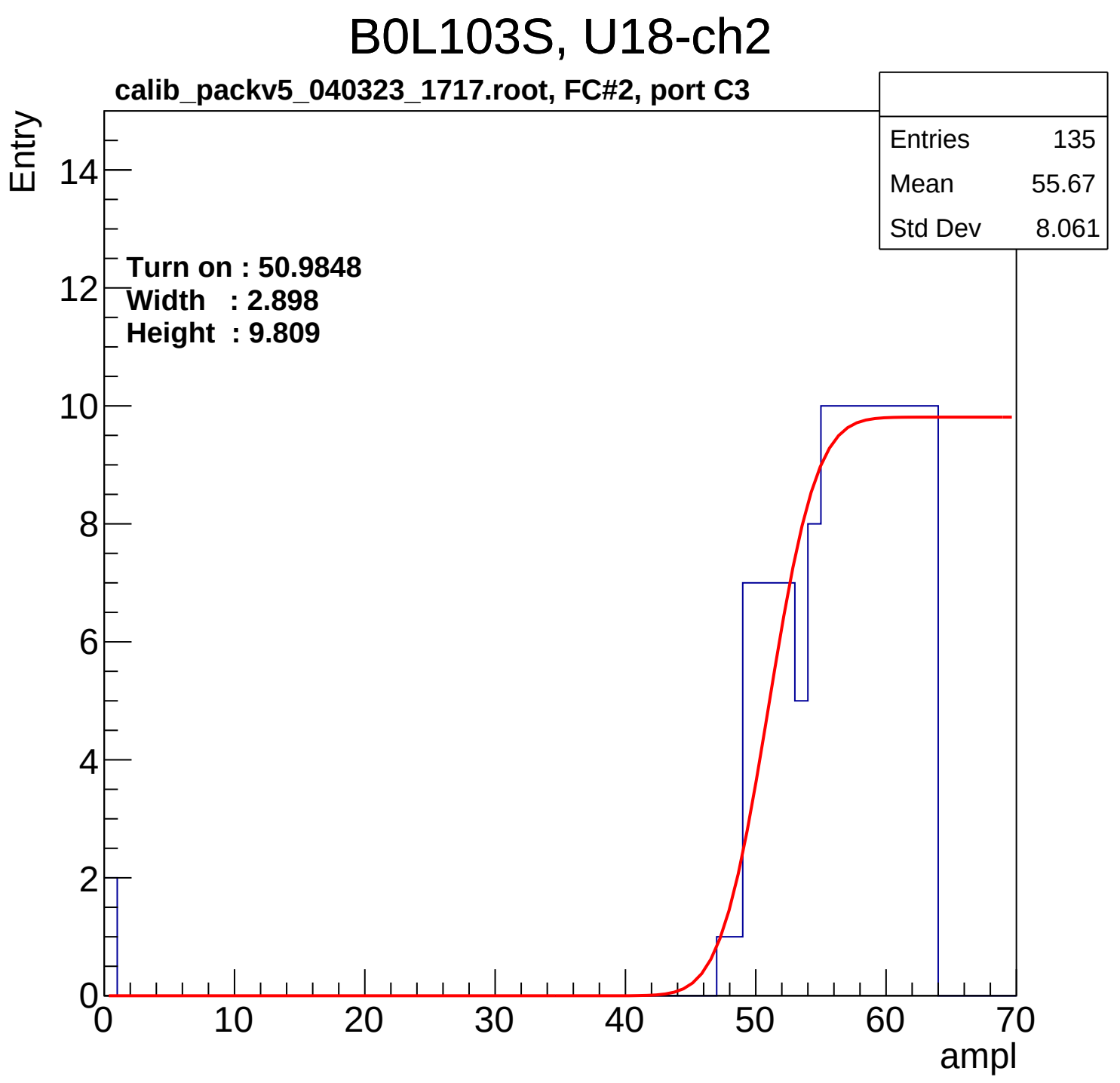
B0L103S, U18-ch2
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 55.67
Std Dev 8.061
Turn on : 50.9848
Width : 2.898
Height : 9.809
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ampl
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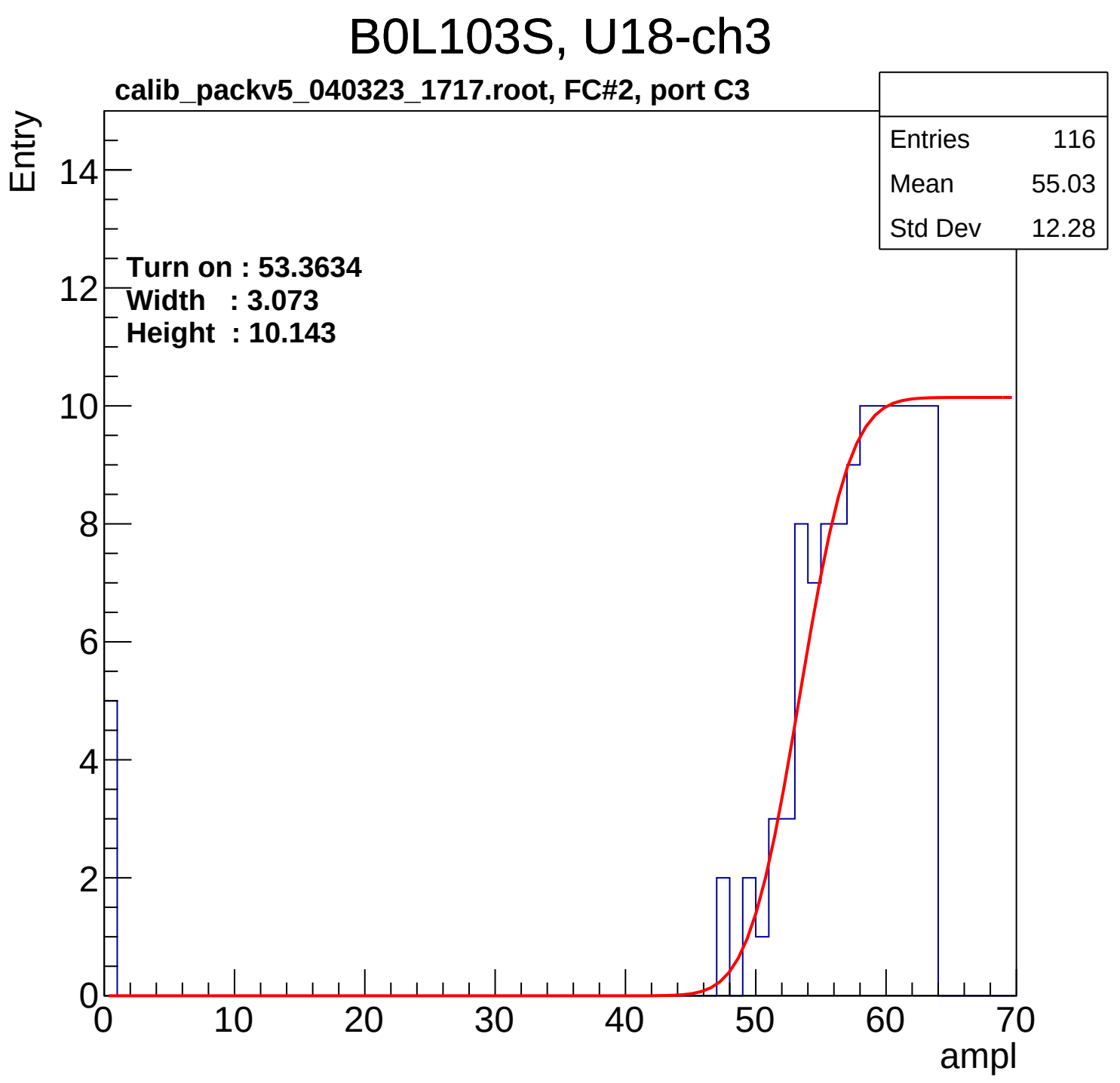
B0L103S, U18-ch3
calib_packv5_040323_1717.root, FC#2, port C3
Entries 116
Mean 55.03
Std Dev 12.28
Turn on : 53.3634
Width : 3.073
Height : 10.143
Entry
ampl
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2
4
6
8
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0
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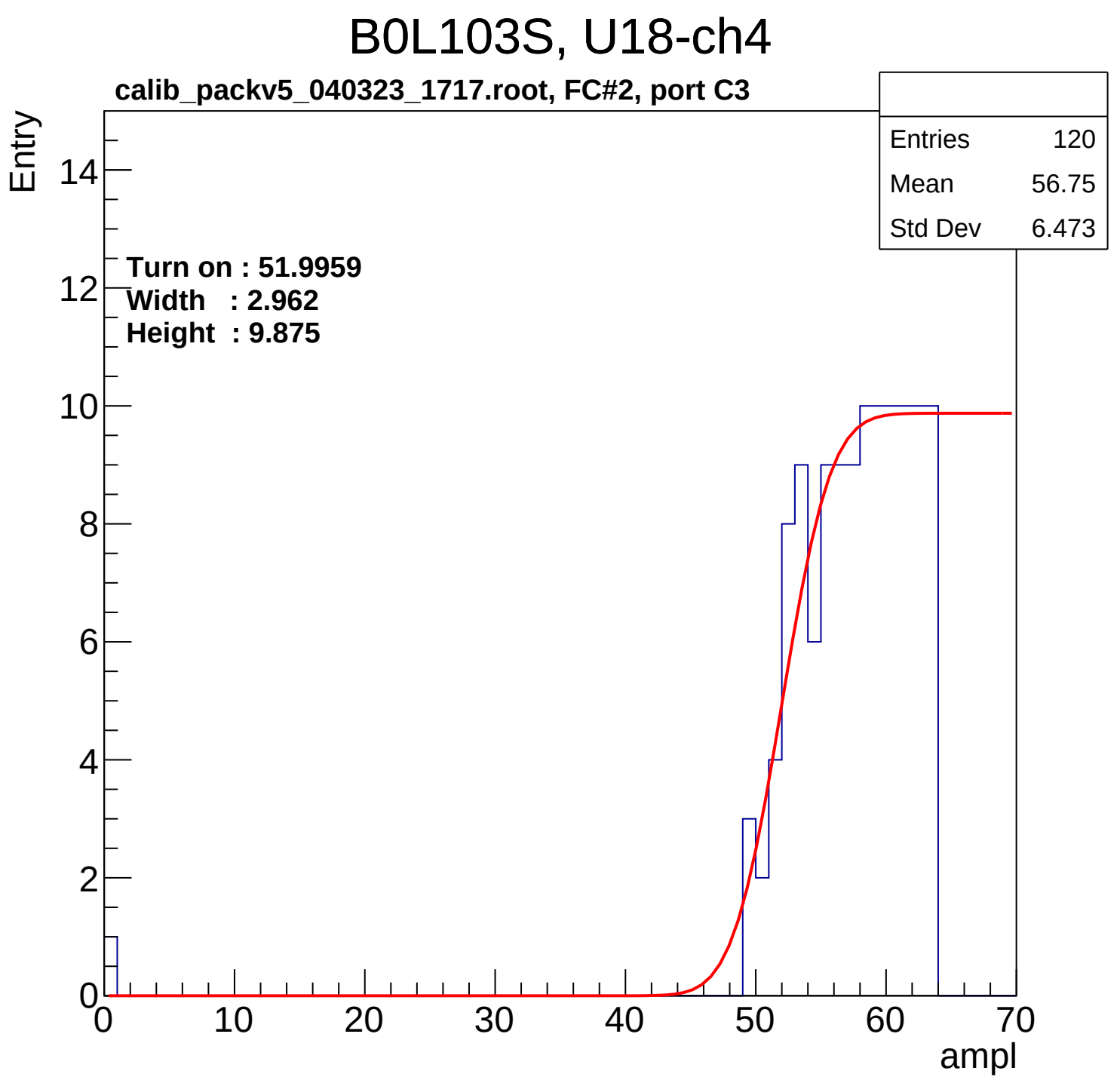
B0L103S, U18-ch4
calib_packv5_040323_1717.root, FC#2, port C3
Entries 120
Mean 56.75
Std Dev 6.473
Turn on : 51.9959
Width : 2.962
Height : 9.875
Entry
ampl
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8
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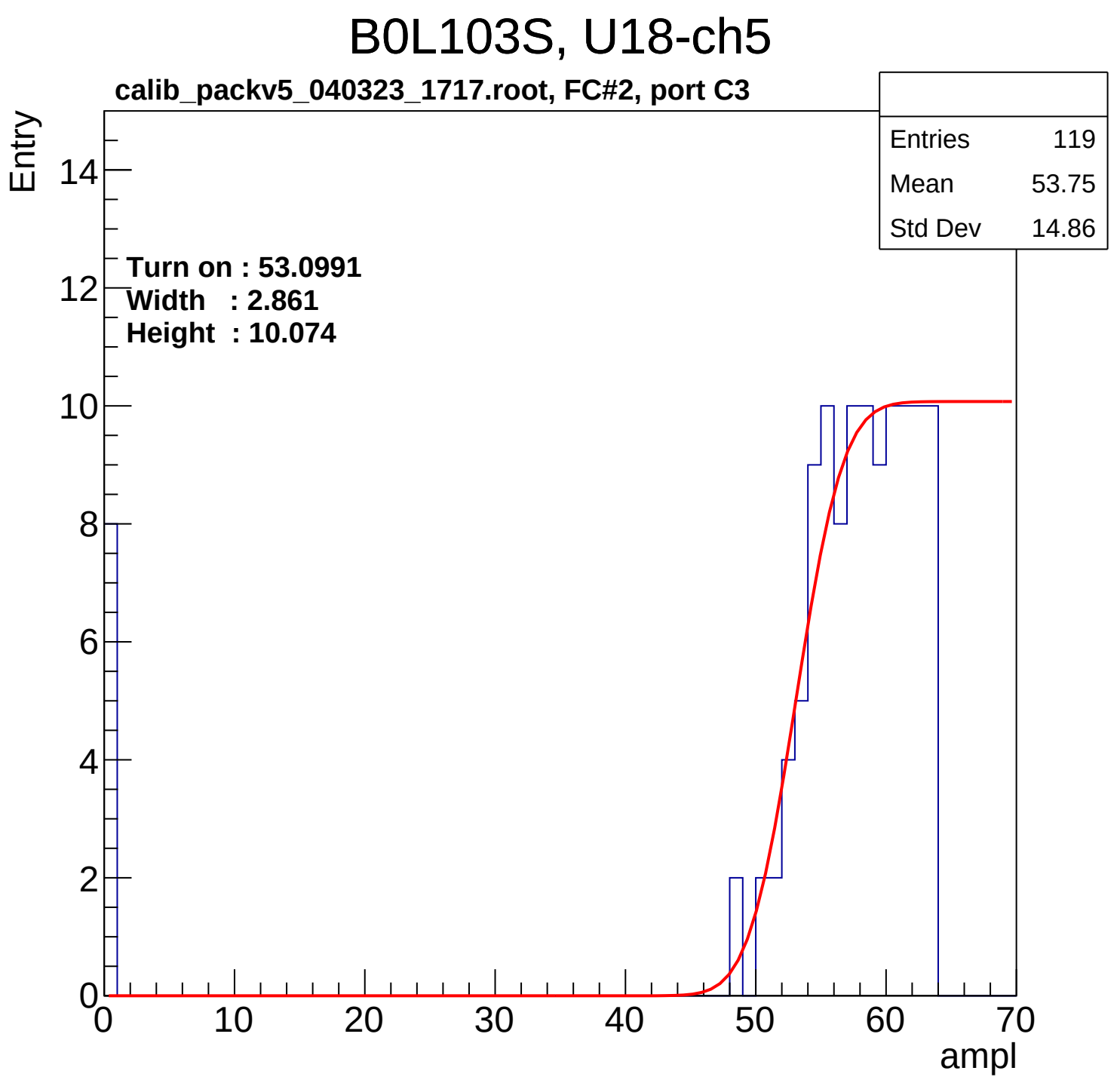
B0L103S, U18-ch5
calib_packv5_040323_1717.root, FC#2, port C3
Entries 119
Mean 53.75
Std Dev 14.86
Turn on : 53.0991
Width : 2.861
Height : 10.074
Entry
ampl
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2
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6
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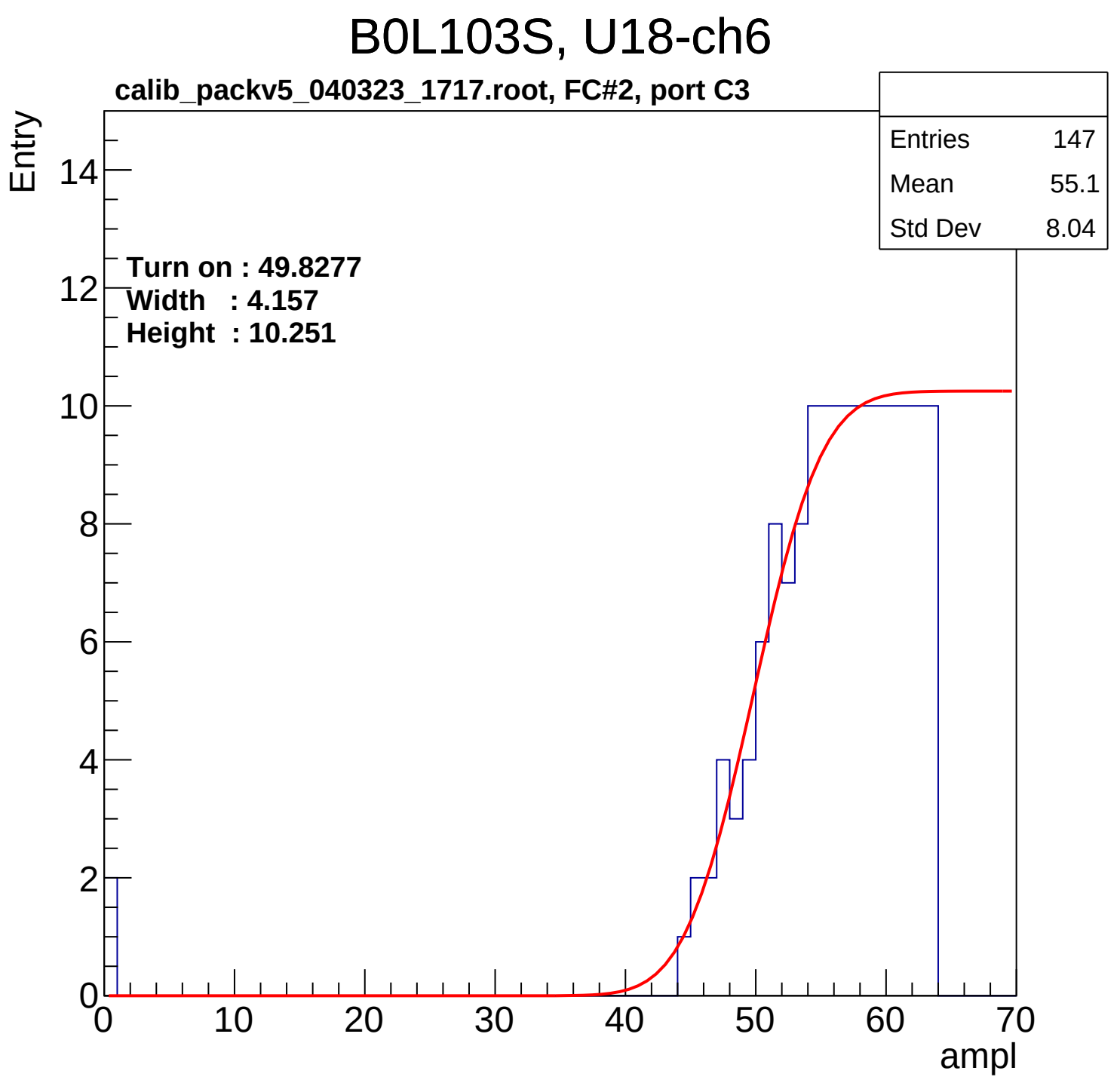
B0L103S, U18-ch6
calib_packv5_040323_1717.root, FC#2, port C3
Entries 147
Mean 55.1
Std Dev 8.04
Turn on : 49.8277
Width : 4.157
Height : 10.251
Entry
ampl
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6
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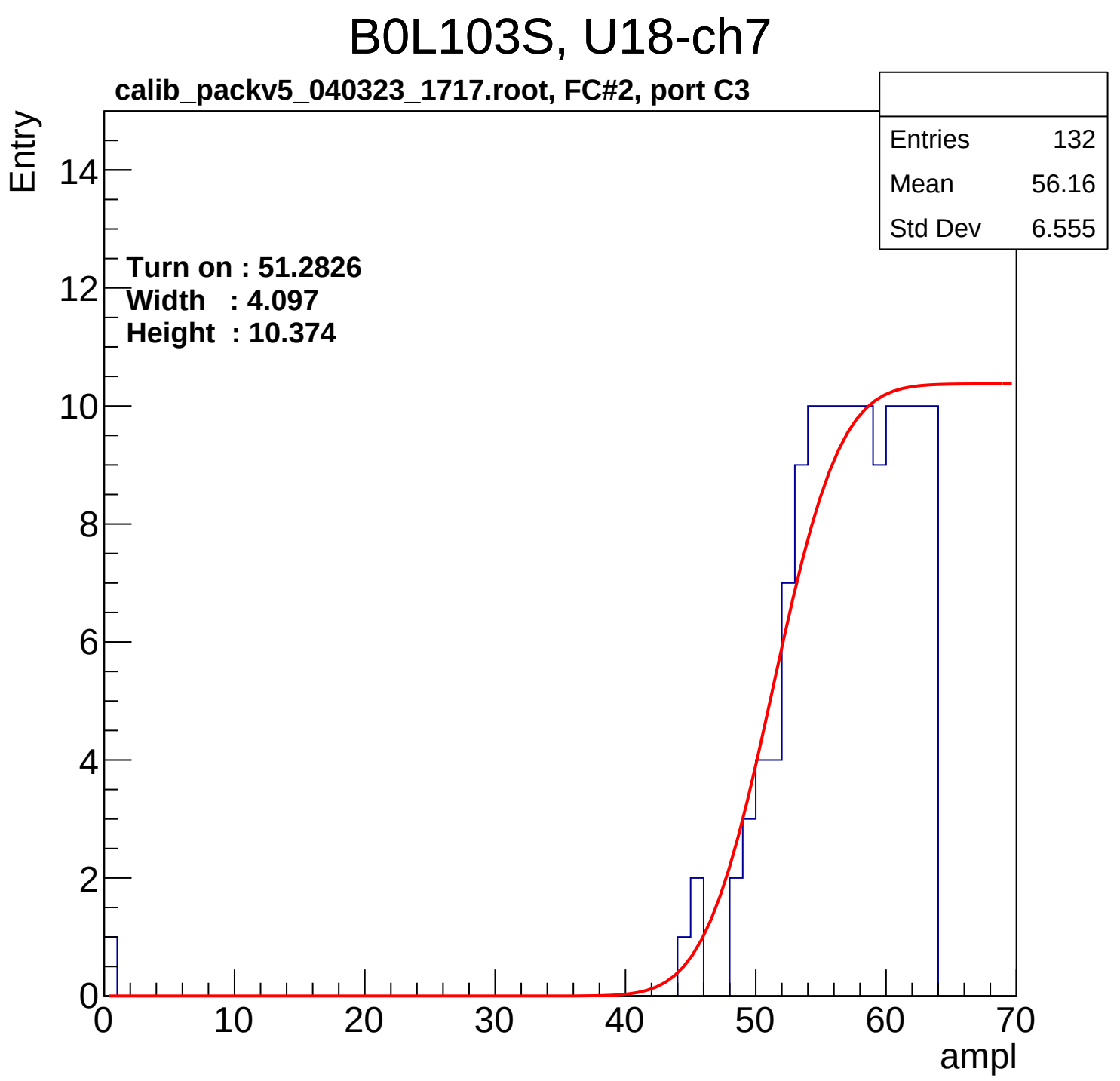
B0L103S, U18-ch7
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 56.16
Std Dev 6.555
Turn on : 51.2826
Width : 4.097
Height : 10.374
Entry
ampl
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2
4
6
8
10
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60
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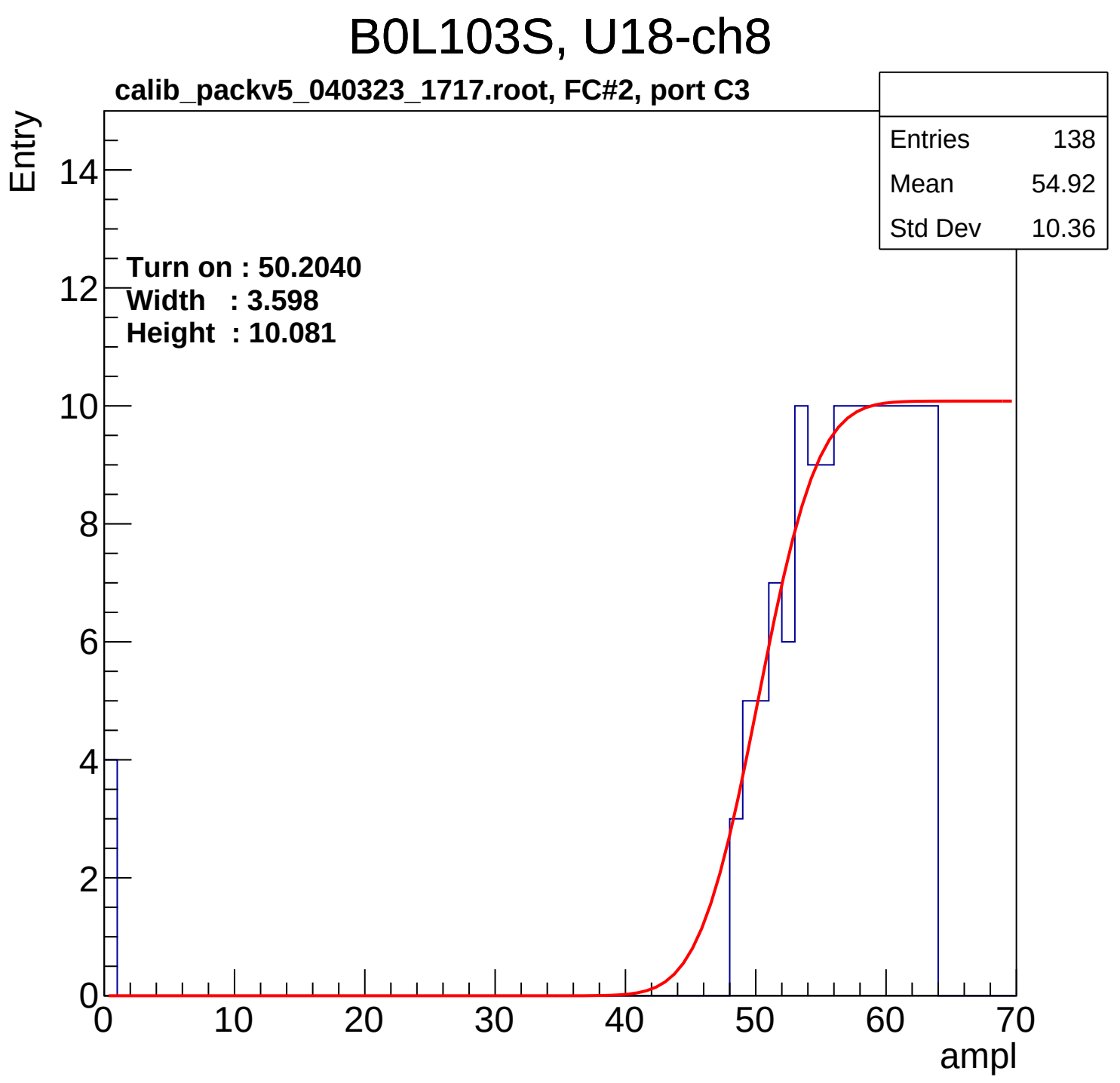
B0L103S, U18-ch8
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 54.92
Std Dev 10.36
Turn on : 50.2040
Width : 3.598
Height : 10.081
Entry
ampl
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8
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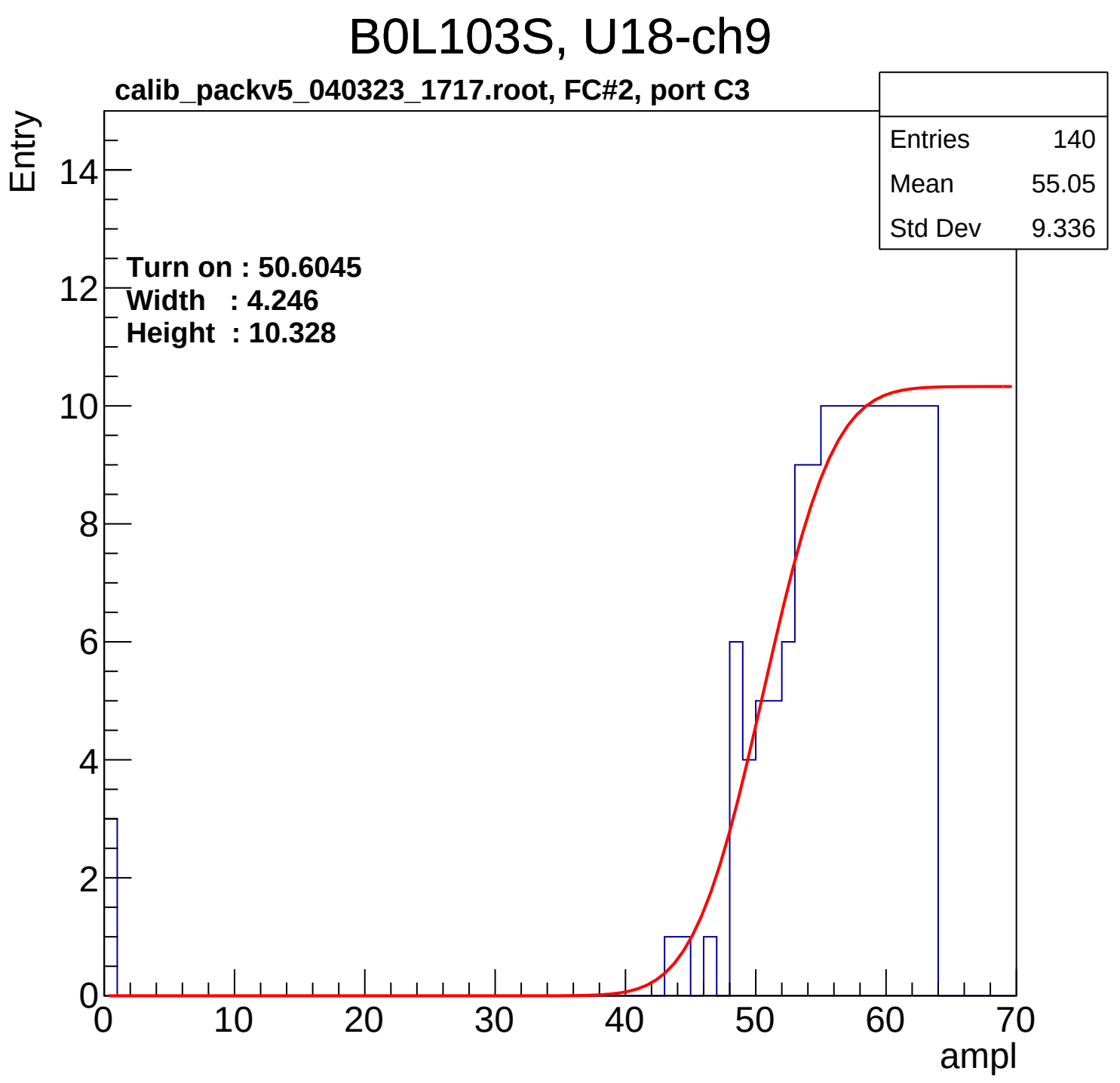
B0L103S, U18-ch9
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 55.05
Std Dev 9.336
Turn on : 50.6045
Width : 4.246
Height : 10.328
Entry
ampl
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2
4
6
8
10
12
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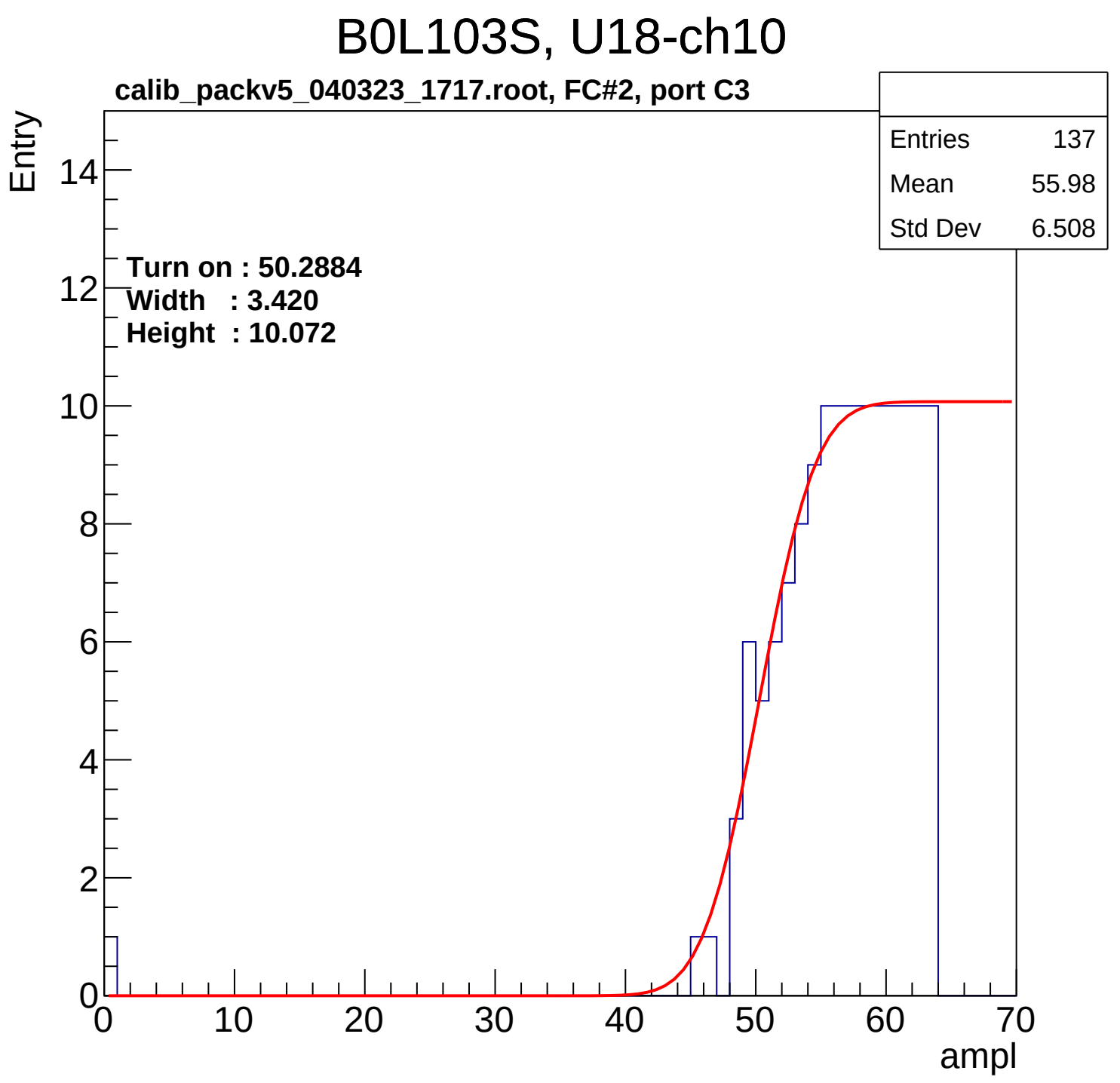
B0L103S, U18-ch10
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 55.98
Std Dev 6.508
Turn on : 50.2884
Width : 3.420
Height : 10.072
Entry
ampl
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6
8
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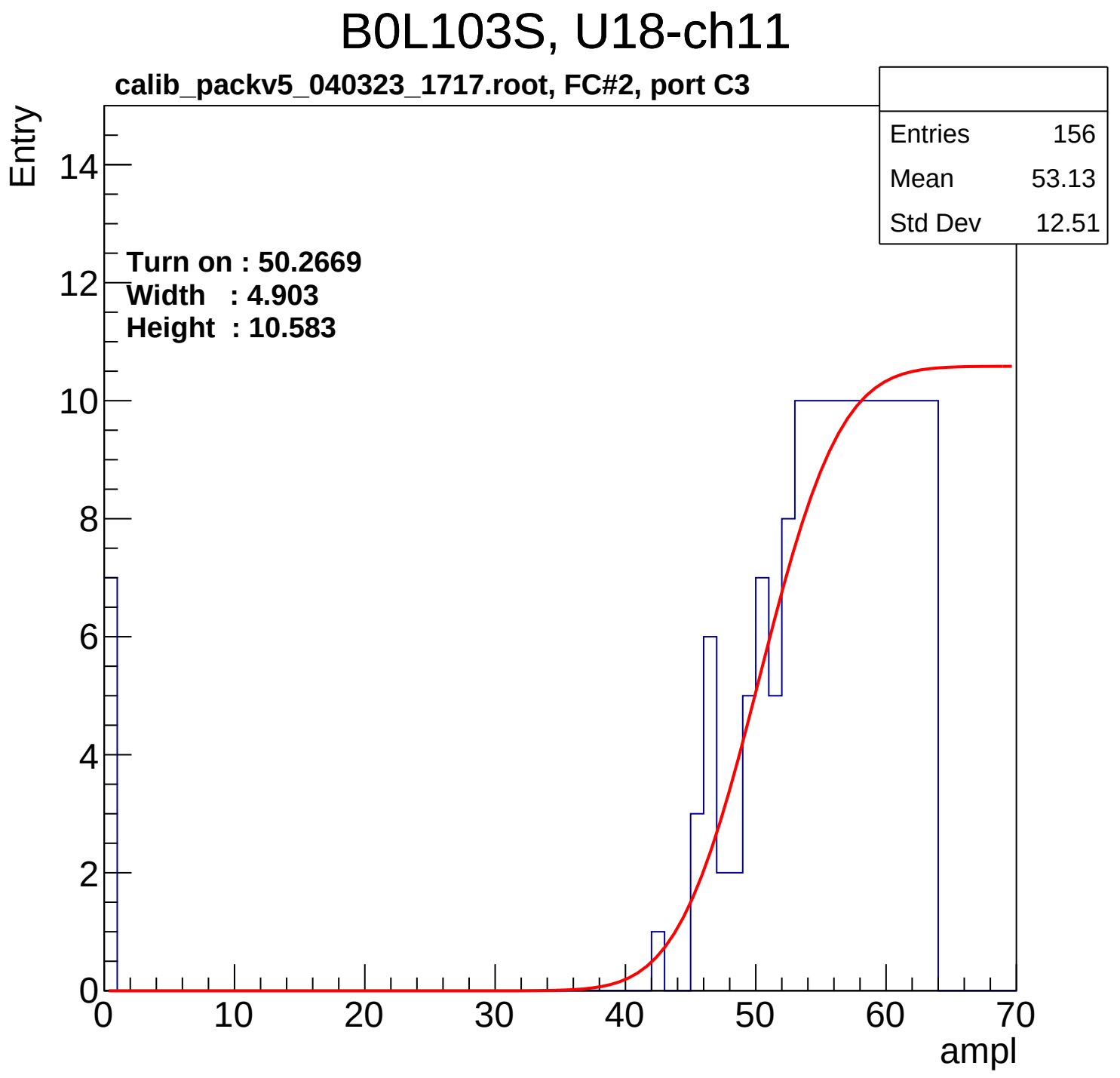
B0L103S, U18-ch11
calib_packv5_040323_1717.root, FC#2, port C3
Entries 156
Mean 53.13
Std Dev 12.51
Turn on : 50.2669
Width : 4.903
Height : 10.583
Entry
ampl
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6
8
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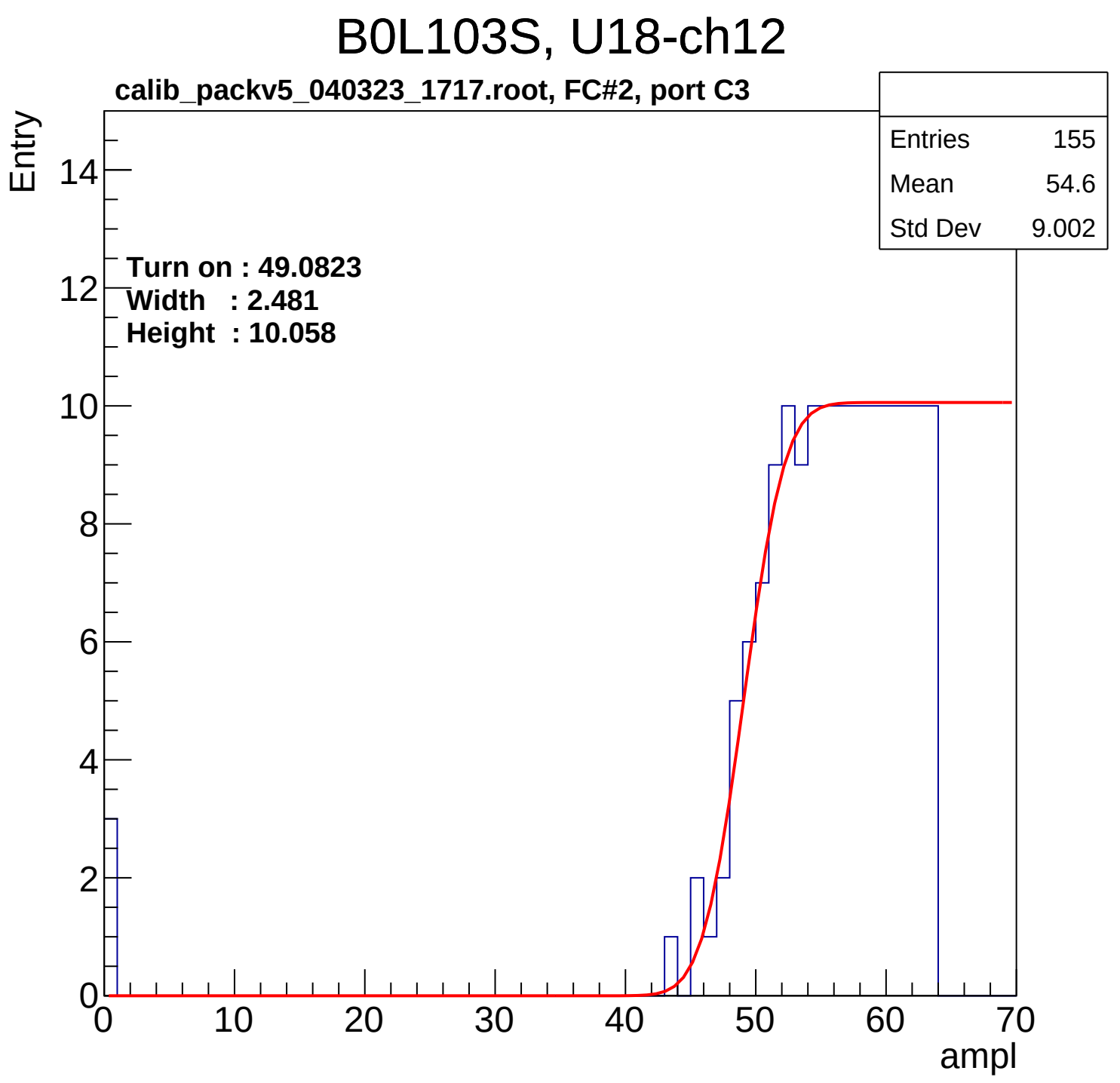
B0L103S, U18-ch12
calib_packv5_040323_1717.root, FC#2, port C3
Entries 155
Mean 54.6
Std Dev 9.002
Turn on : 49.0823
Width : 2.481
Height : 10.058
Entry
ampl
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6
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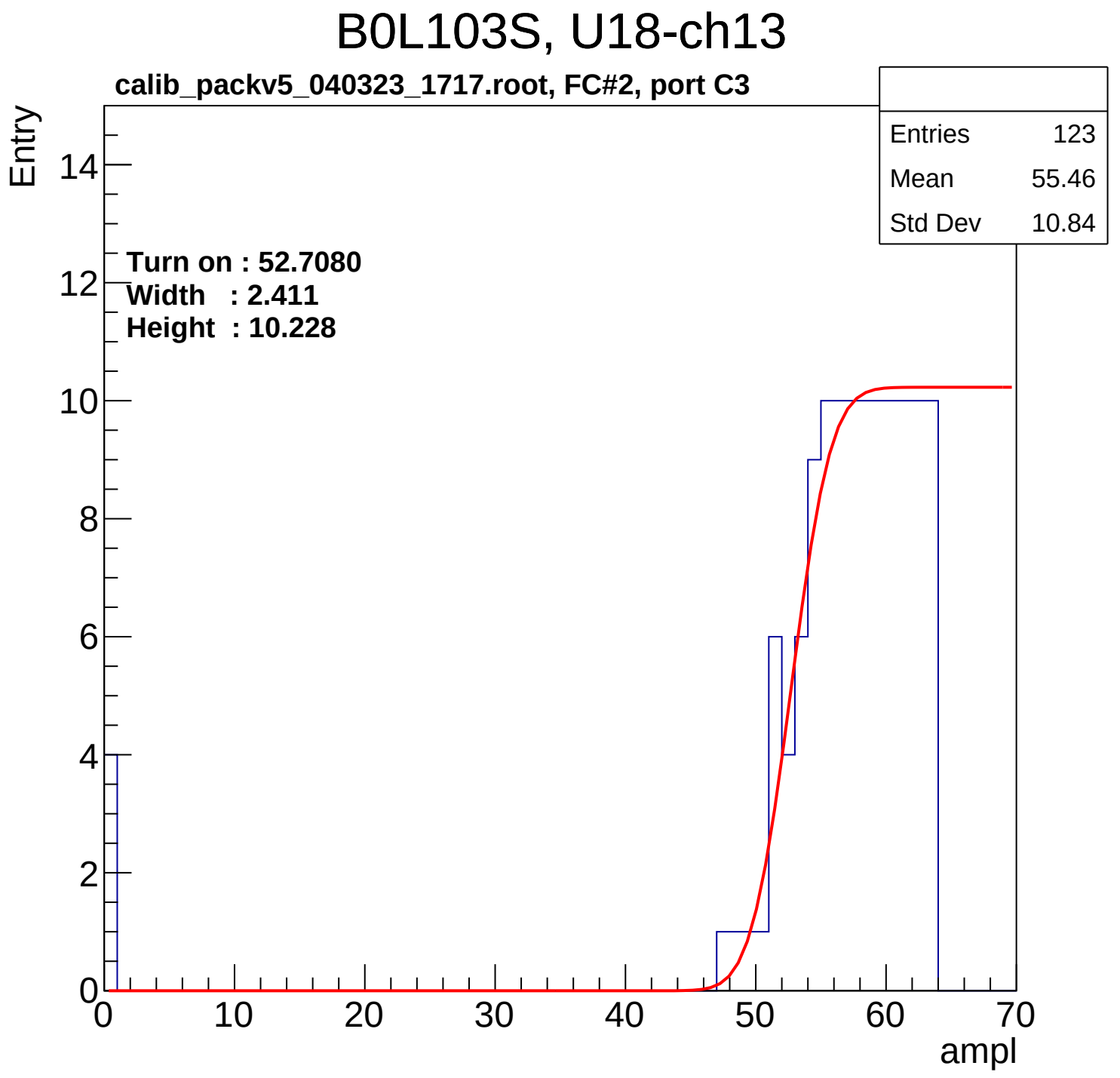
B0L103S, U18-ch13
calib_packv5_040323_1717.root, FC#2, port C3
Entries 123
Mean 55.46
Std Dev 10.84
Turn on : 52.7080
Width : 2.411
Height : 10.228
Entry
ampl
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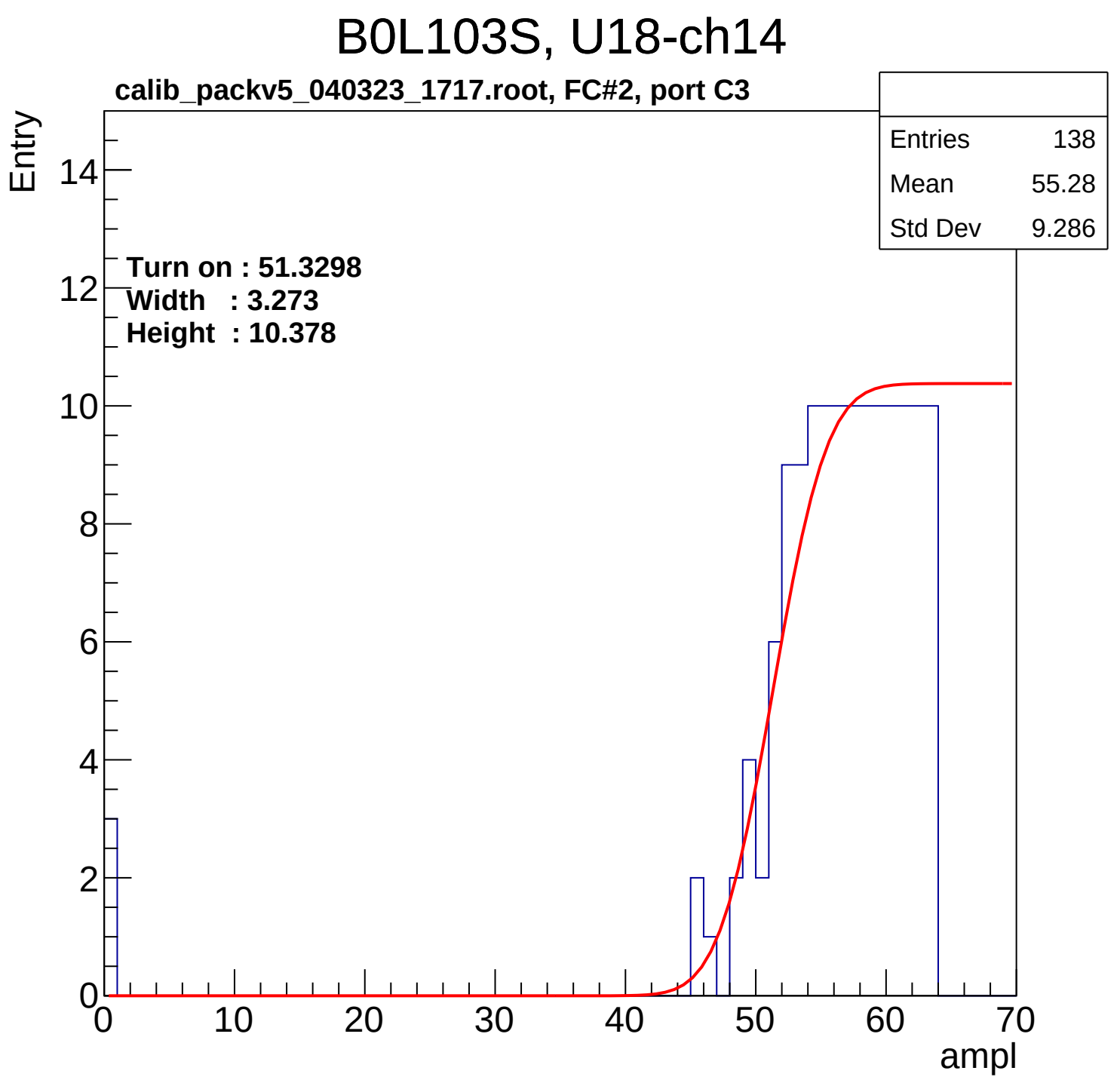
B0L103S, U18-ch14
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 55.28
Std Dev 9.286
Turn on : 51.3298
Width : 3.273
Height : 10.378
Entry
ampl
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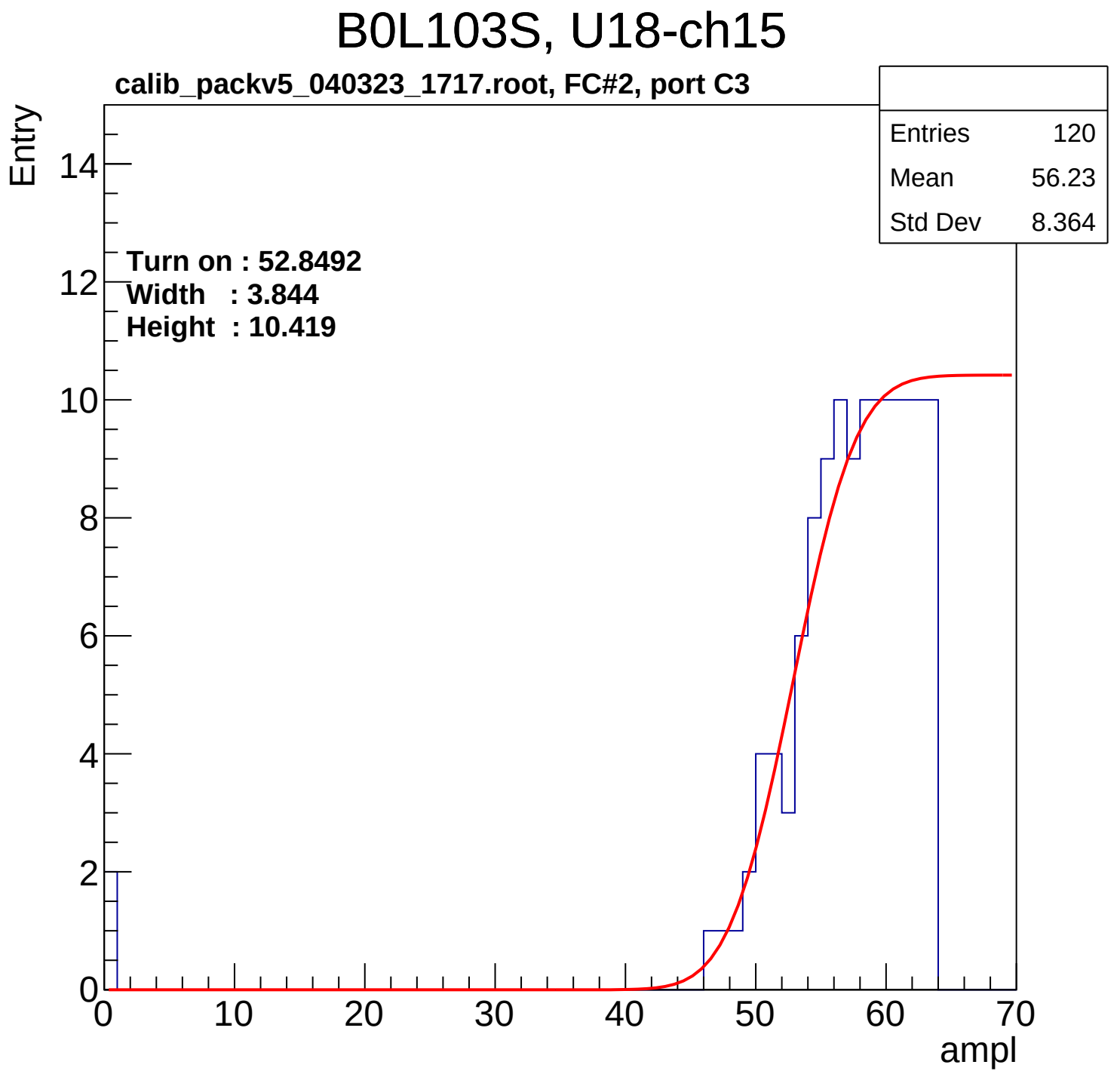
B0L103S, U18-ch15
calib_packv5_040323_1717.root, FC#2, port C3
Entries 120
Mean 56.23
Std Dev 8.364
Turn on : 52.8492
Width : 3.844
Height : 10.419
Entry
ampl
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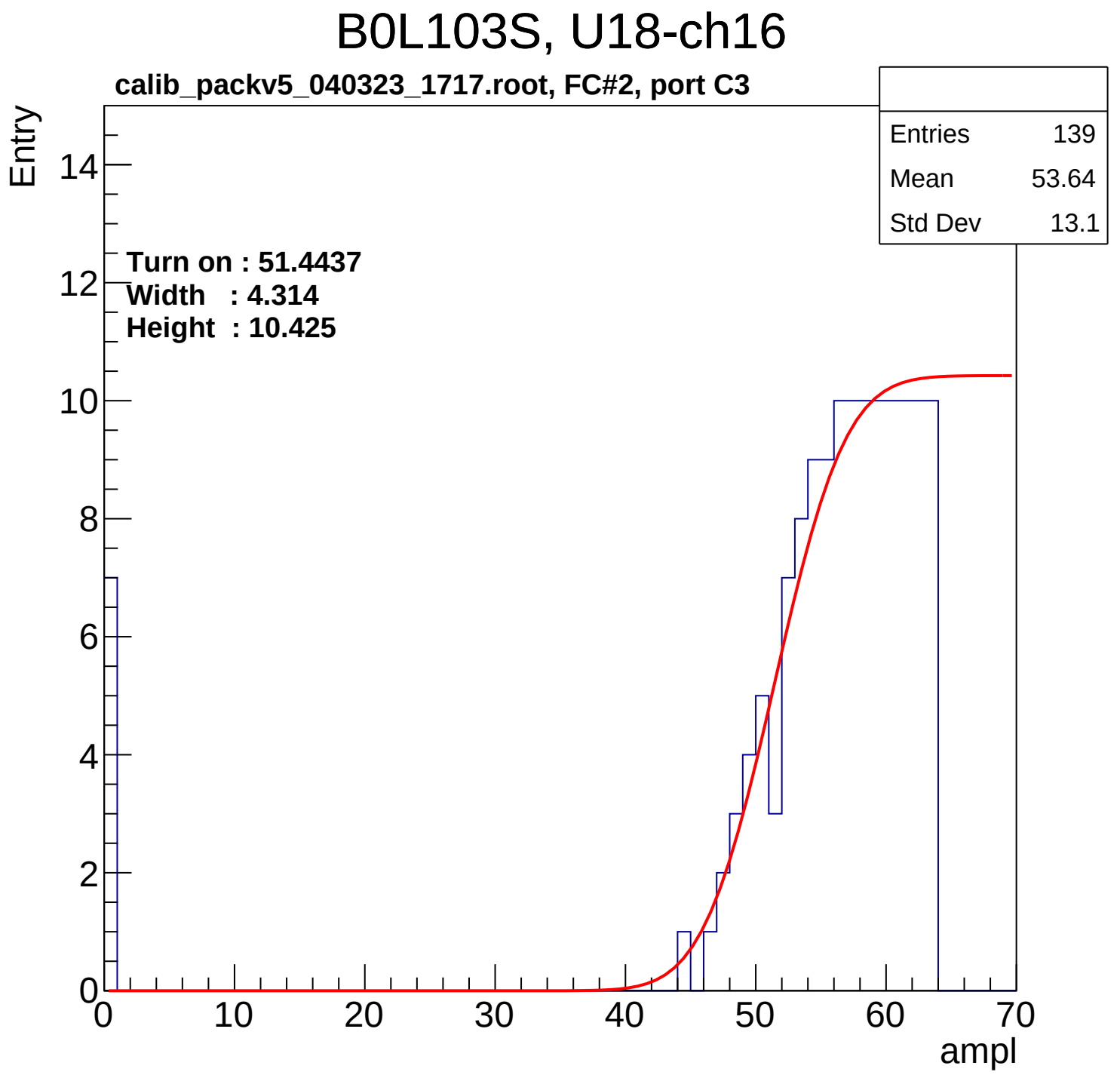
B0L103S, U18-ch16
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 53.64
Std Dev 13.1
Turn on : 51.4437
Width : 4.314
Height : 10.425
Entry
ampl
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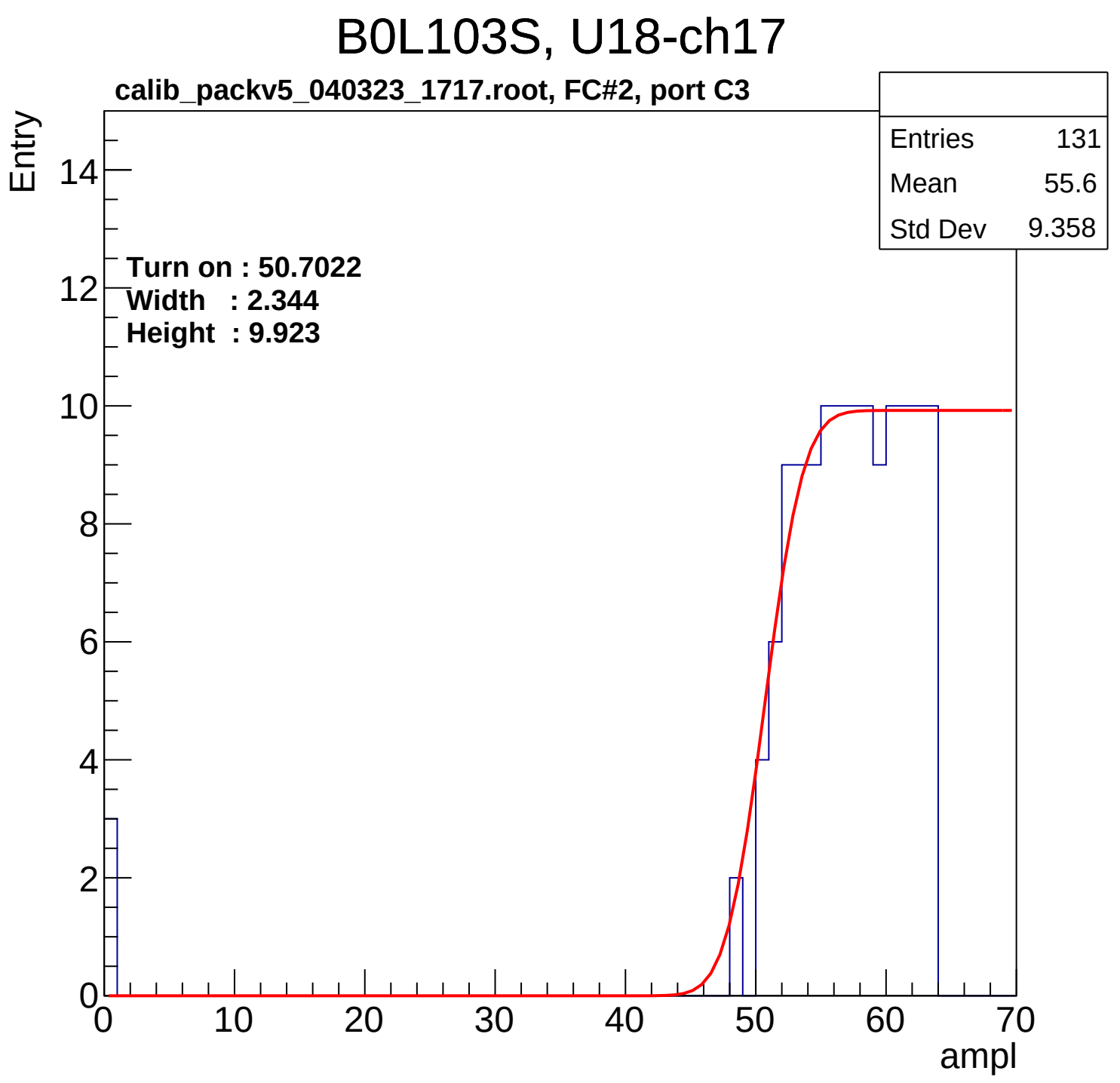
B0L103S, U18-ch17
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 55.6
Std Dev 9.358
Turn on : 50.7022
Width : 2.344
Height : 9.923
Entry
ampl
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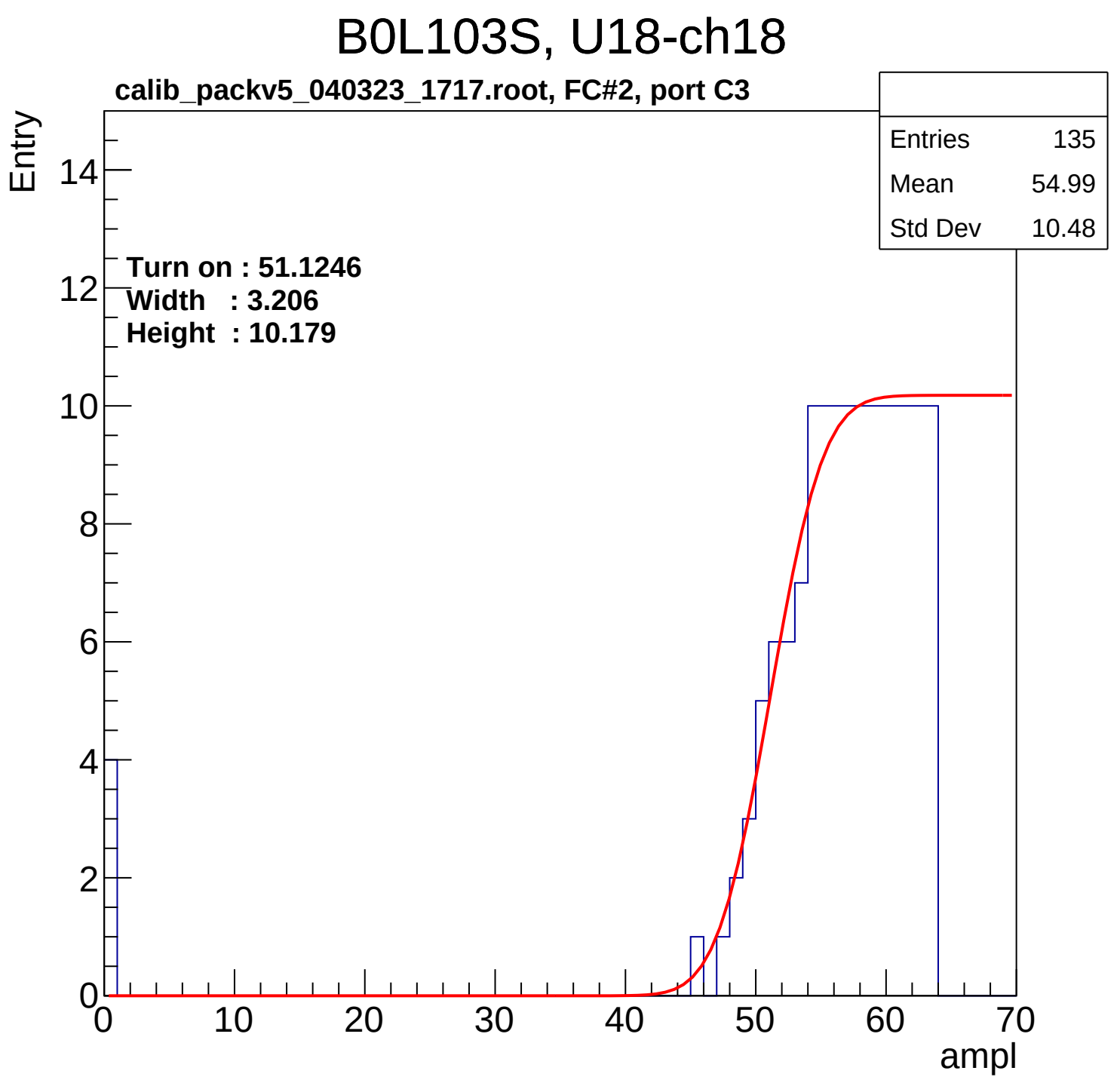
B0L103S, U18-ch18
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 54.99
Std Dev 10.48
Turn on : 51.1246
Width : 3.206
Height : 10.179
Entry
ampl
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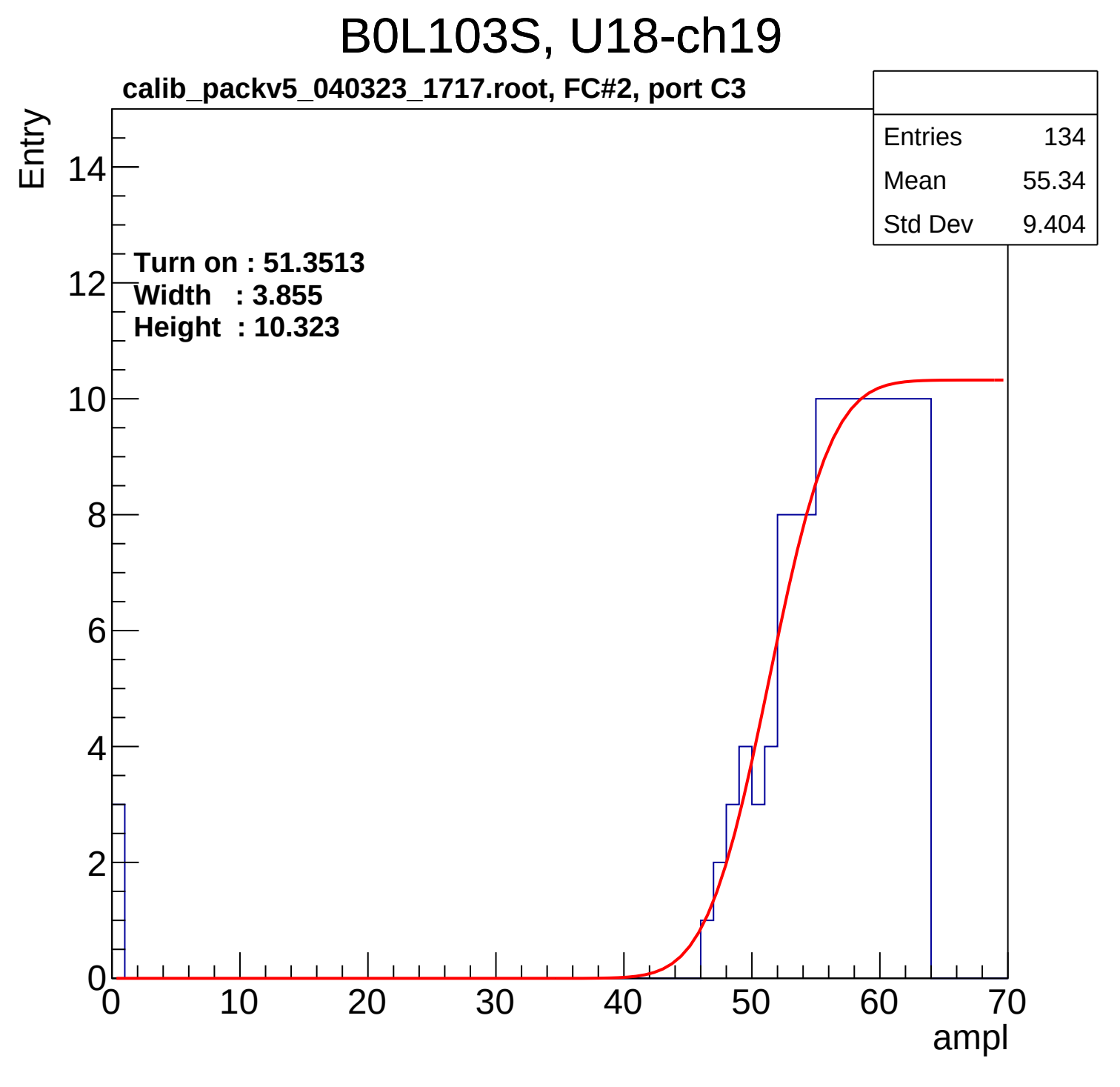
B0L103S, U18-ch19
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 55.34
Std Dev 9.404
Turn on : 51.3513
Width : 3.855
Height : 10.323
Entry
ampl
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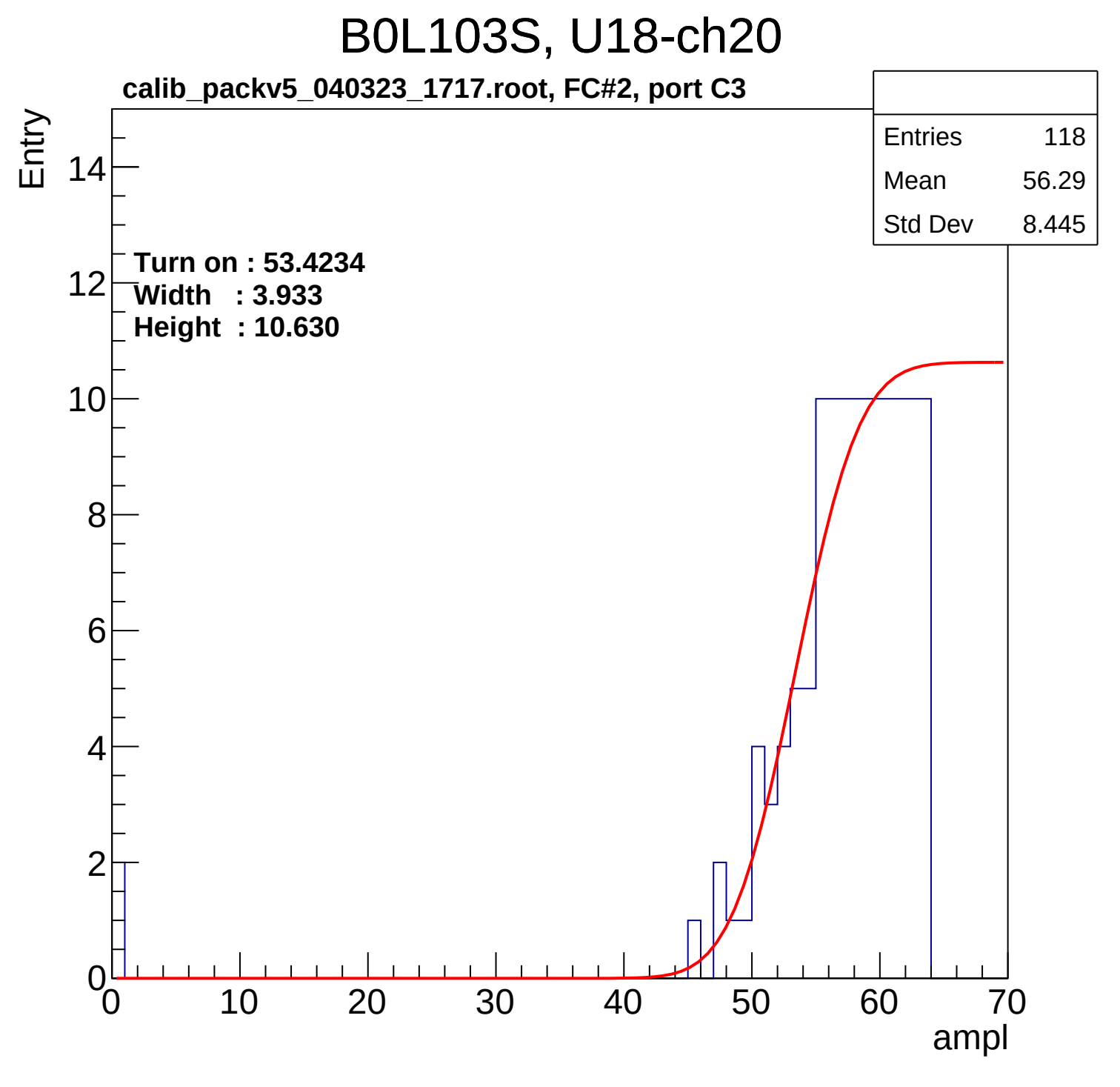
B0L103S, U18-ch20
calib_packv5_040323_1717.root, FC#2, port C3
Entries 118
Mean 56.29
Std Dev 8.445
Turn on : 53.4234
Width : 3.933
Height : 10.630
Entry
ampl
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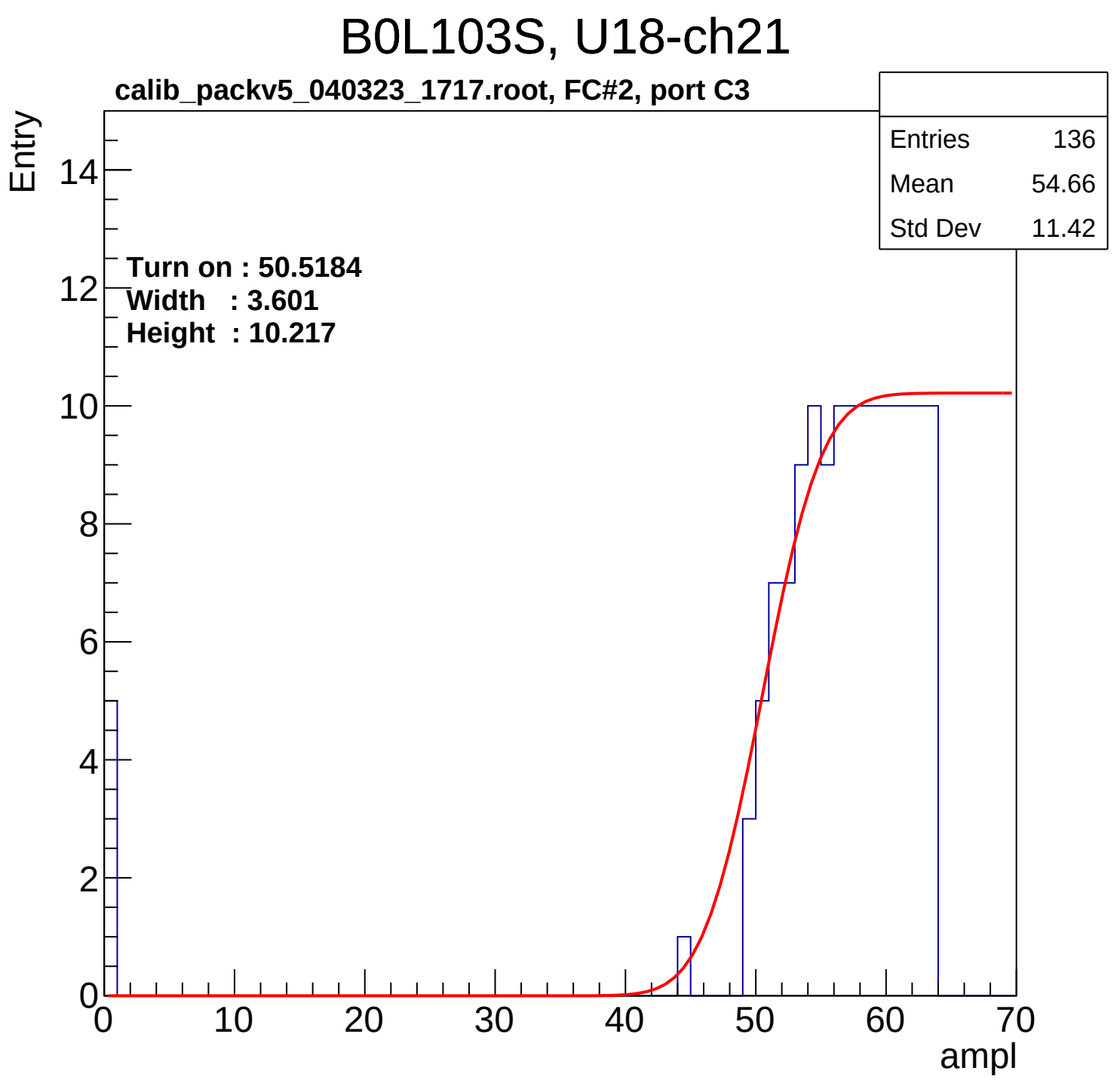
B0L103S, U18-ch21
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 54.66
Std Dev 11.42
Turn on : 50.5184
Width : 3.601
Height : 10.217
Entry
ampl
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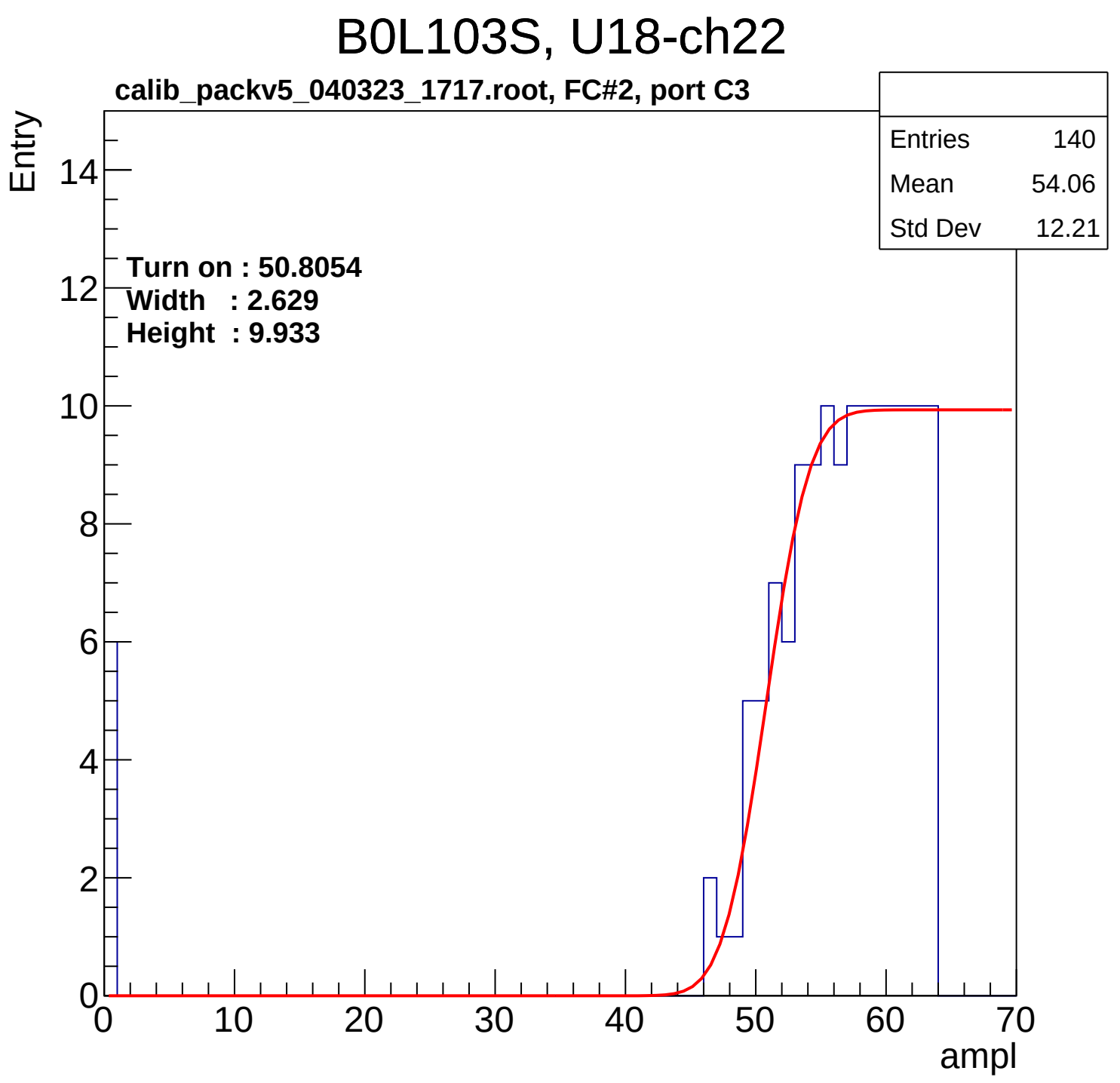
B0L103S, U18-ch22
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 54.06
Std Dev 12.21
Turn on : 50.8054
Width : 2.629
Height : 9.933
Entry
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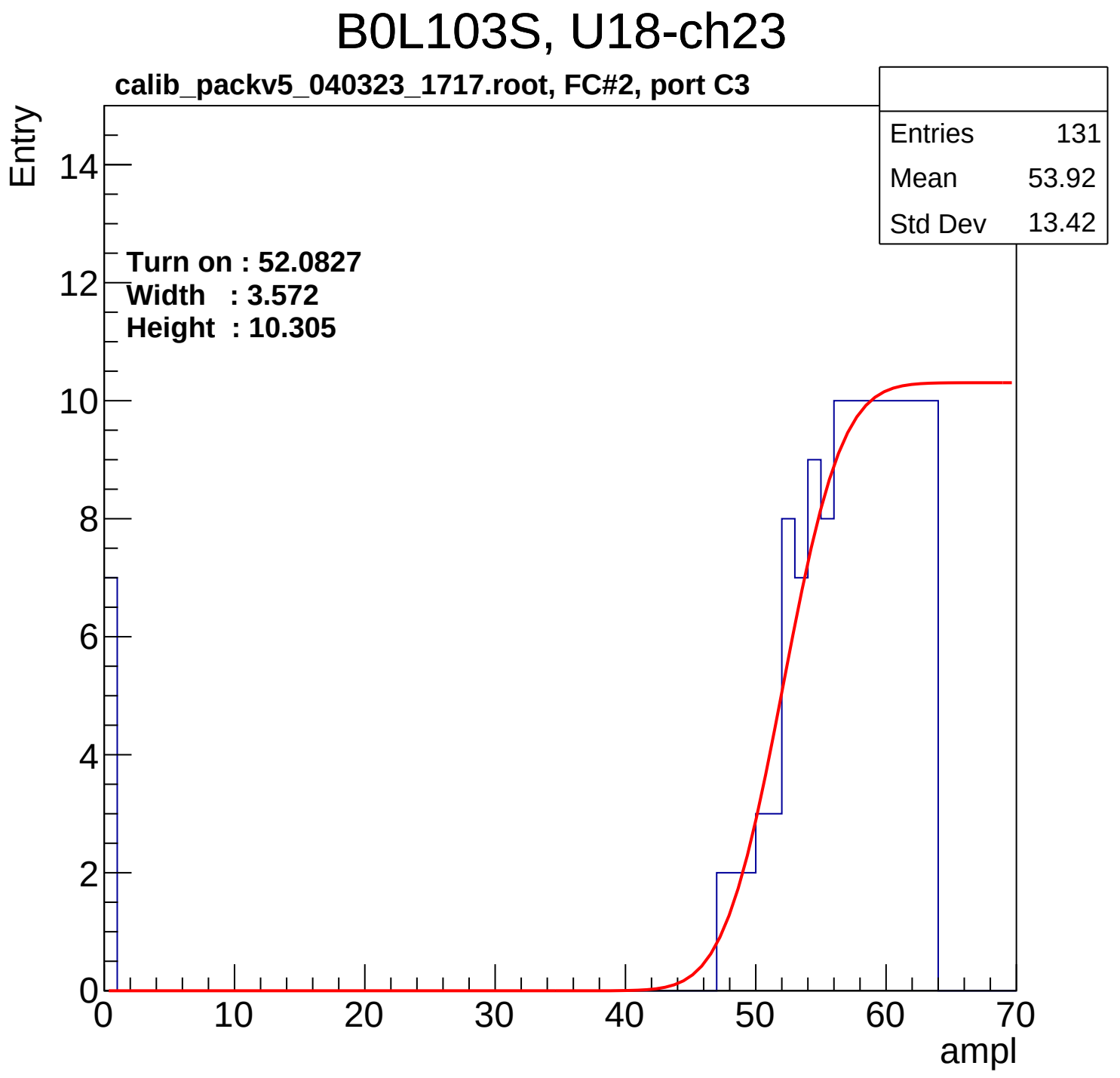
B0L103S, U18-ch23
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 53.92
Std Dev 13.42
Turn on : 52.0827
Width : 3.572
Height : 10.305
Entry
ampl
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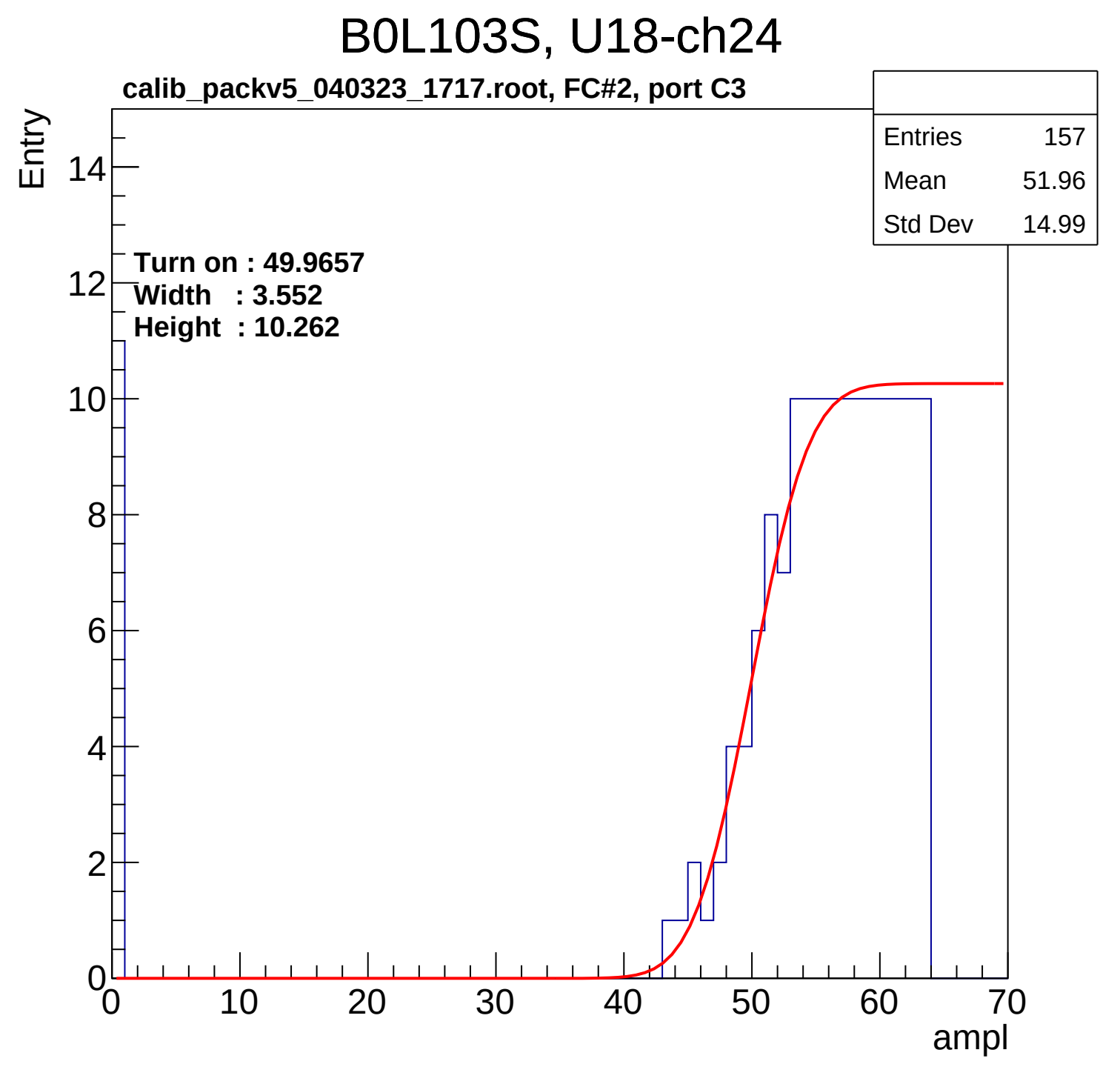
B0L103S, U18-ch24
calib_packv5_040323_1717.root, FC#2, port C3
Entries 157
Mean 51.96
Std Dev 14.99
Turn on : 49.9657
Width : 3.552
Height : 10.262
Entry
ampl
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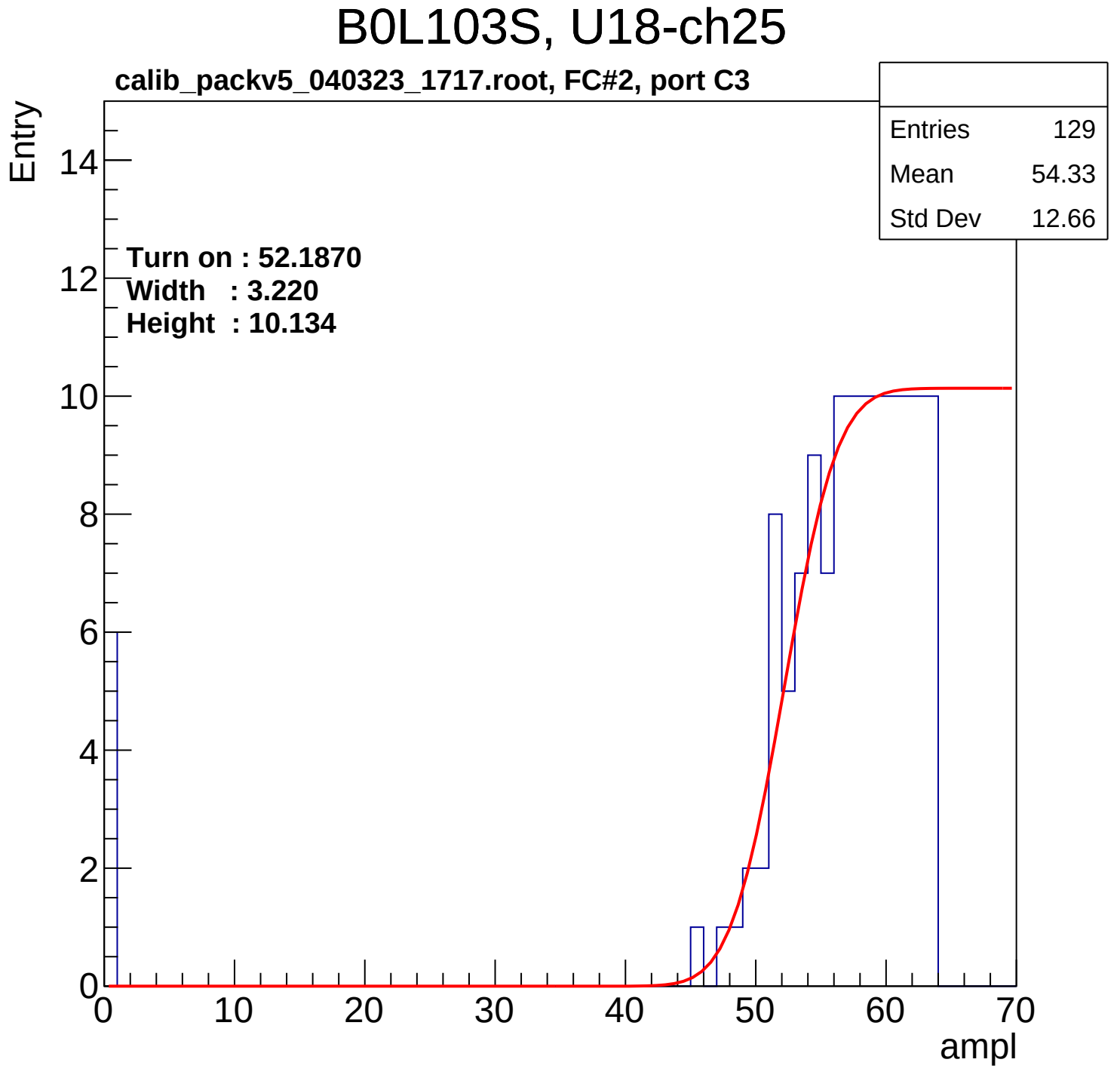
B0L103S, U18-ch25
calib_packv5_040323_1717.root, FC#2, port C3
Entries 129
Mean 54.33
Std Dev 12.66
Turn on : 52.1870
Width : 3.220
Height : 10.134
Entry
ampl
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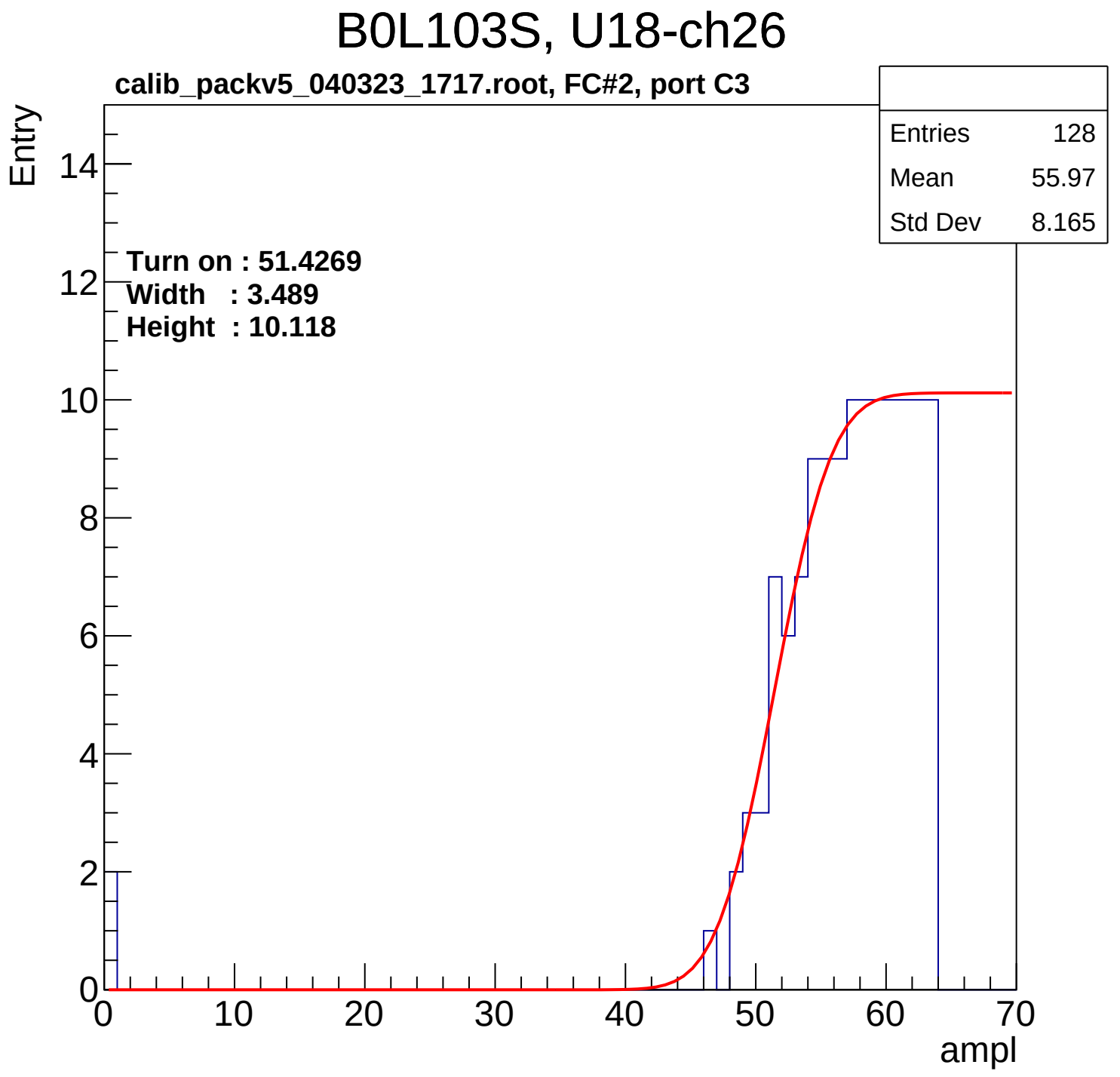
B0L103S, U18-ch26
calib_packv5_040323_1717.root, FC#2, port C3
Entries 128
Mean 55.97
Std Dev 8.165
Turn on : 51.4269
Width : 3.489
Height : 10.118
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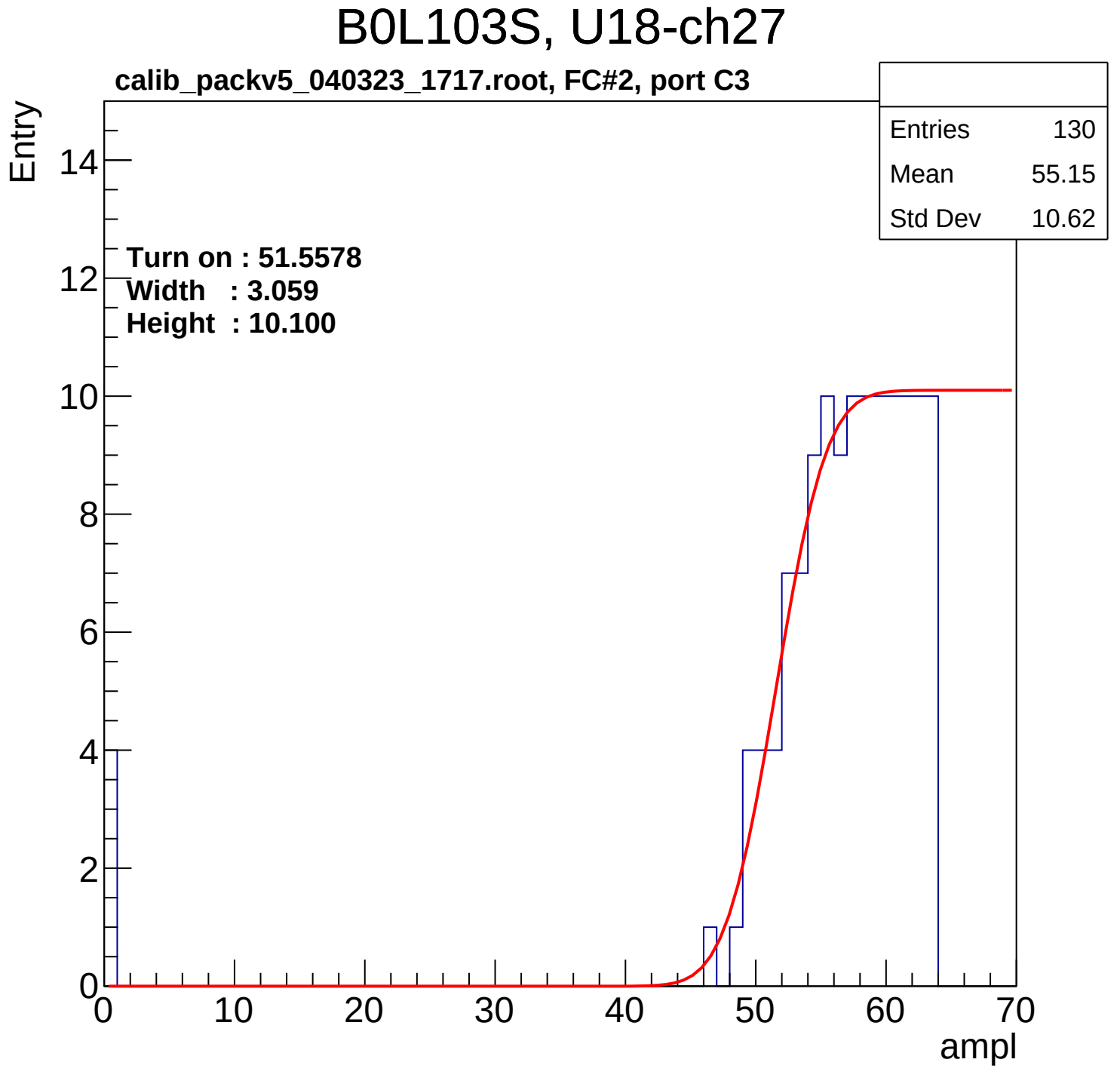
B0L103S, U18-ch27
calib_packv5_040323_1717.root, FC#2, port C3
Entries 130
Mean 55.15
Std Dev 10.62
Turn on : 51.5578
Width : 3.059
Height : 10.100
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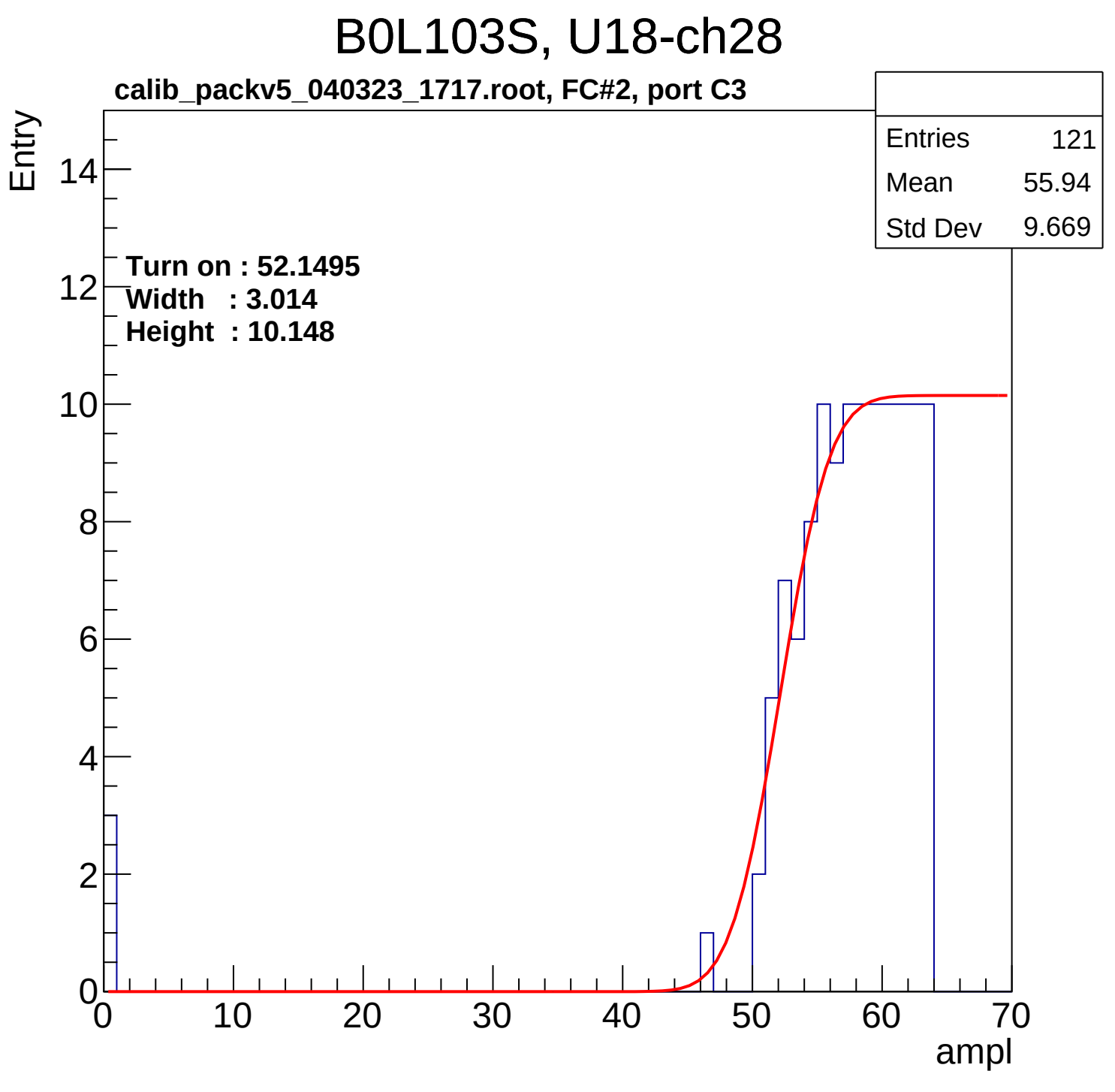
B0L103S, U18-ch28
calib_packv5_040323_1717.root, FC#2, port C3
Entries 121
Mean 55.94
Std Dev 9.669
Turn on : 52.1495
Width : 3.014
Height : 10.148
Entry
ampl
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4
6
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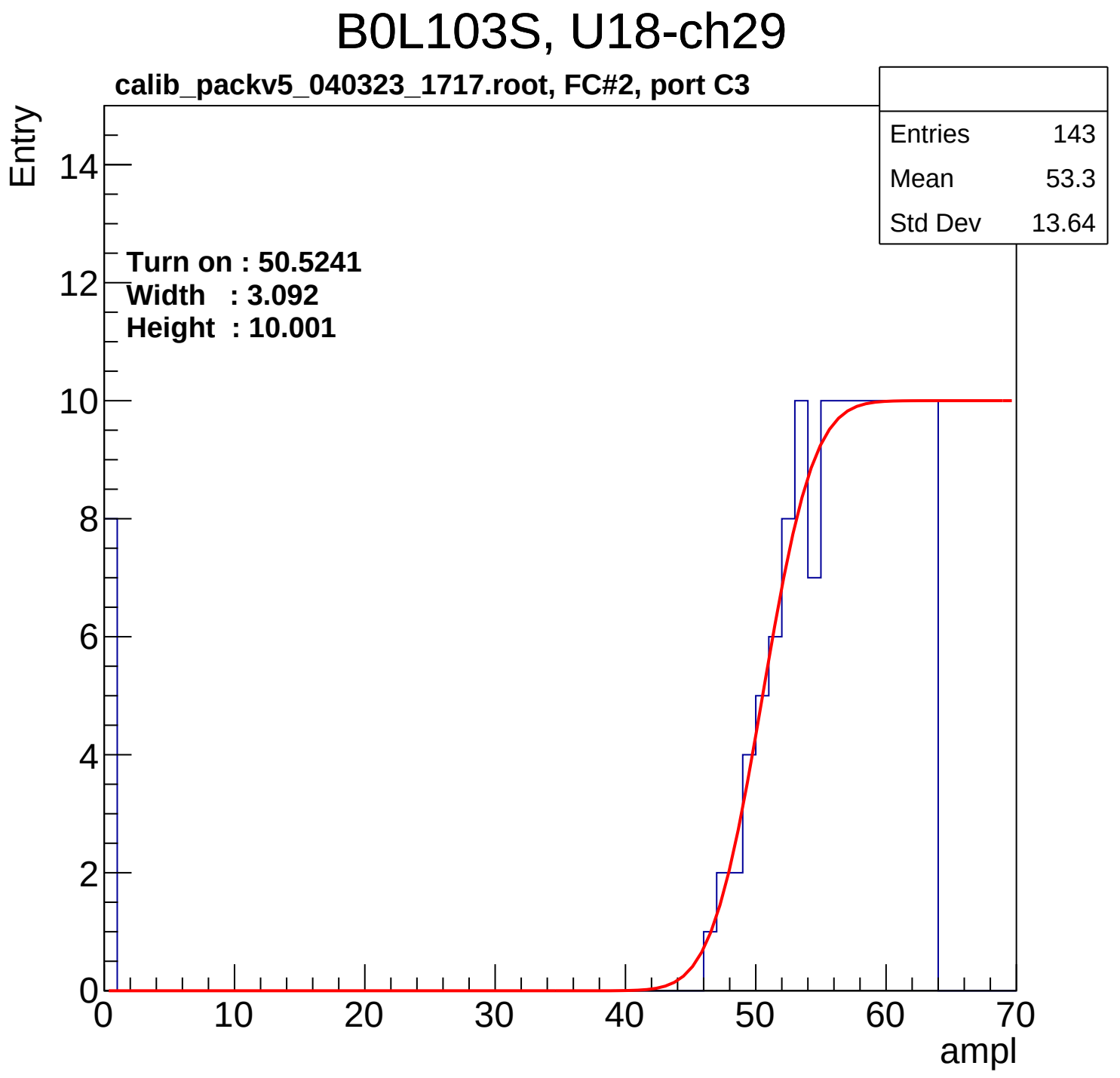
B0L103S, U18-ch29
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 53.3
Std Dev 13.64
Turn on : 50.5241
Width : 3.092
Height : 10.001
Entry
ampl
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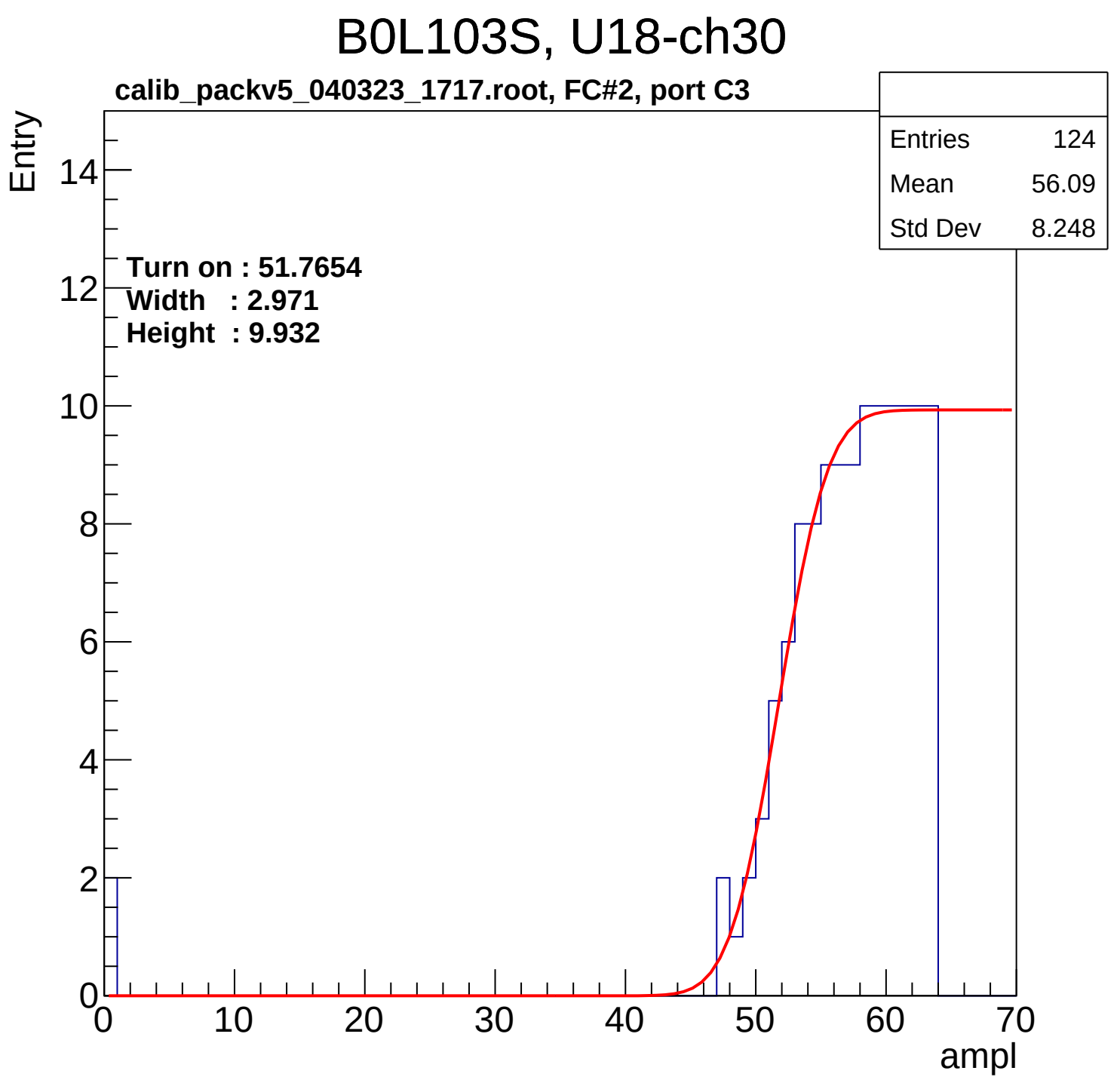
B0L103S, U18-ch30
calib_packv5_040323_1717.root, FC#2, port C3
Entries 124
Mean 56.09
Std Dev 8.248
Turn on : 51.7654
Width : 2.971
Height : 9.932
Entry
ampl
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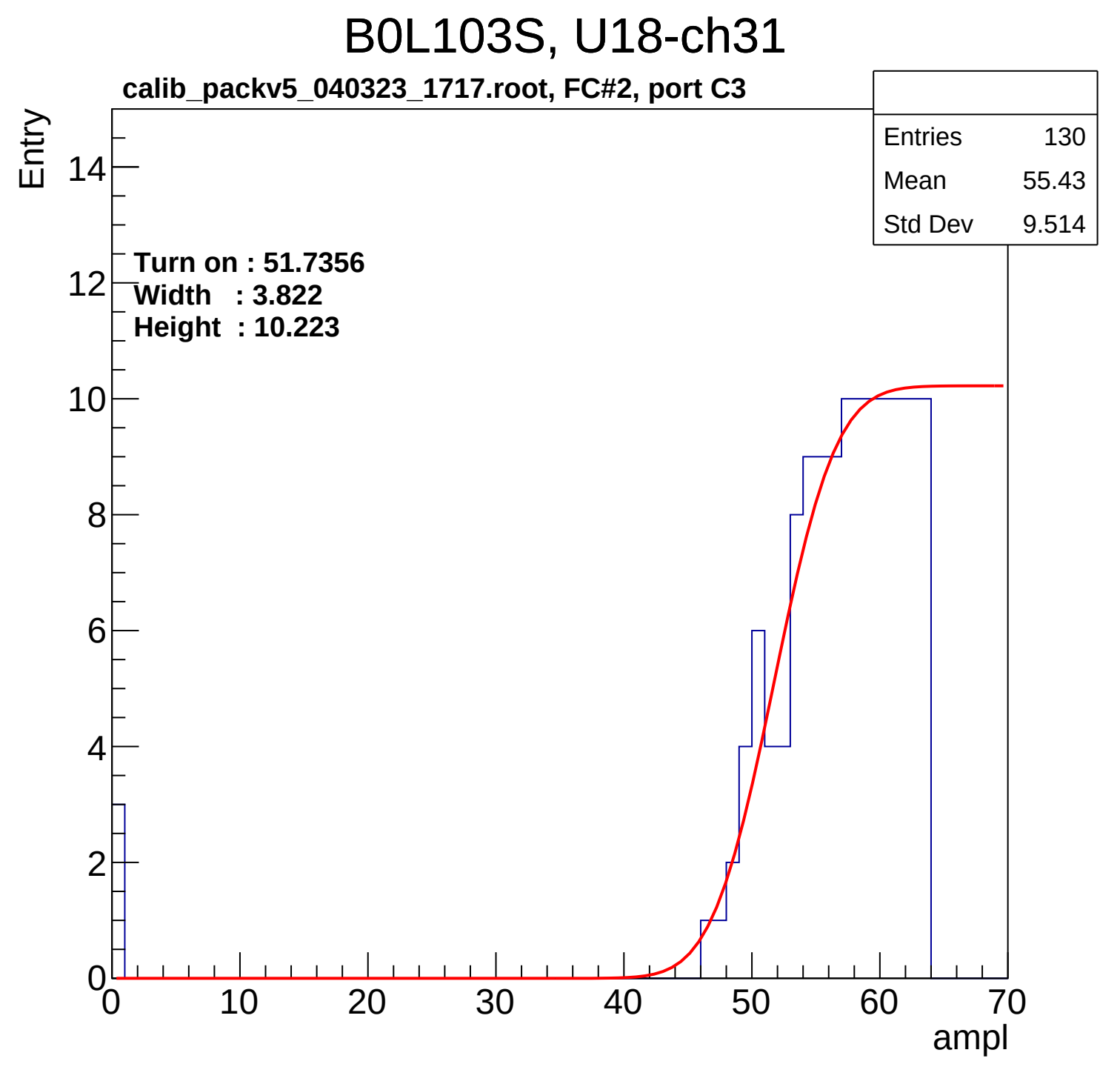
B0L103S, U18-ch31
calib_packv5_040323_1717.root, FC#2, port C3
Entries 130
Mean 55.43
Std Dev 9.514
Turn on : 51.7356
Width : 3.822
Height : 10.223
Entry
ampl
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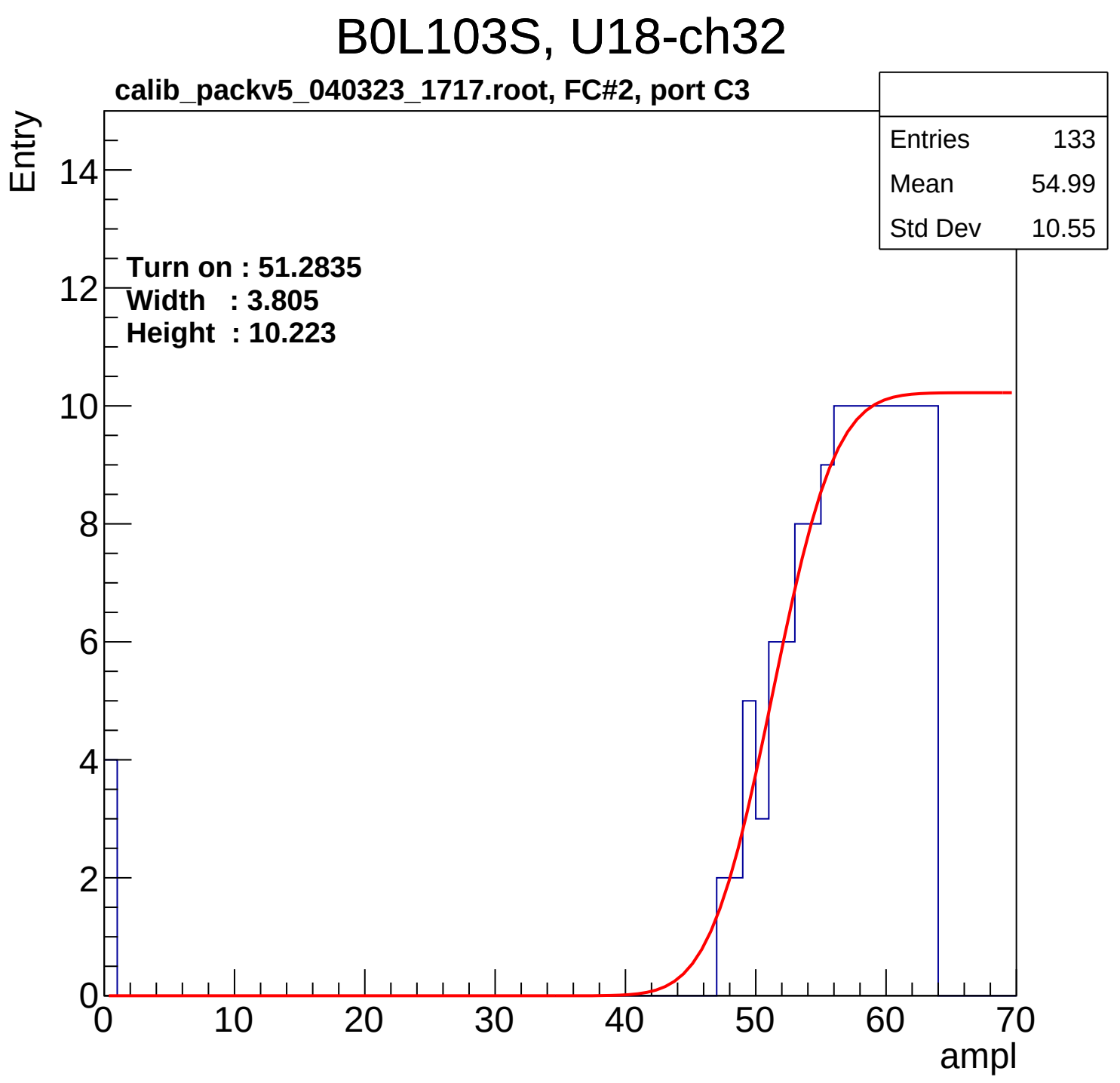
B0L103S, U18-ch32
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 54.99
Std Dev 10.55
Turn on : 51.2835
Width : 3.805
Height : 10.223
Entry
ampl
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2
4
6
8
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12
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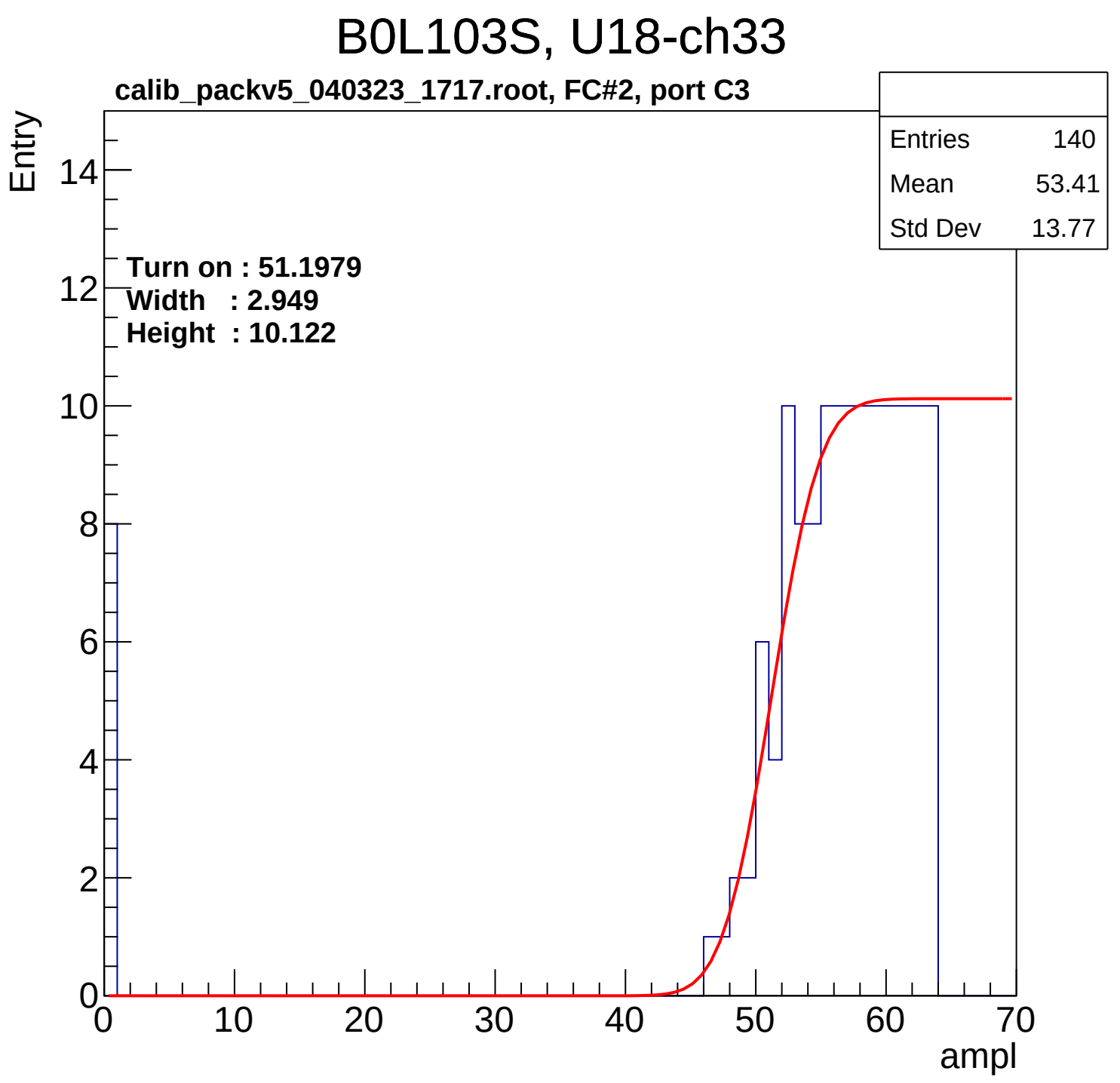
B0L103S, U18-ch33
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 53.41
Std Dev 13.77
Turn on : 51.1979
Width : 2.949
Height : 10.122
Entry
ampl
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2
4
6
8
10
12
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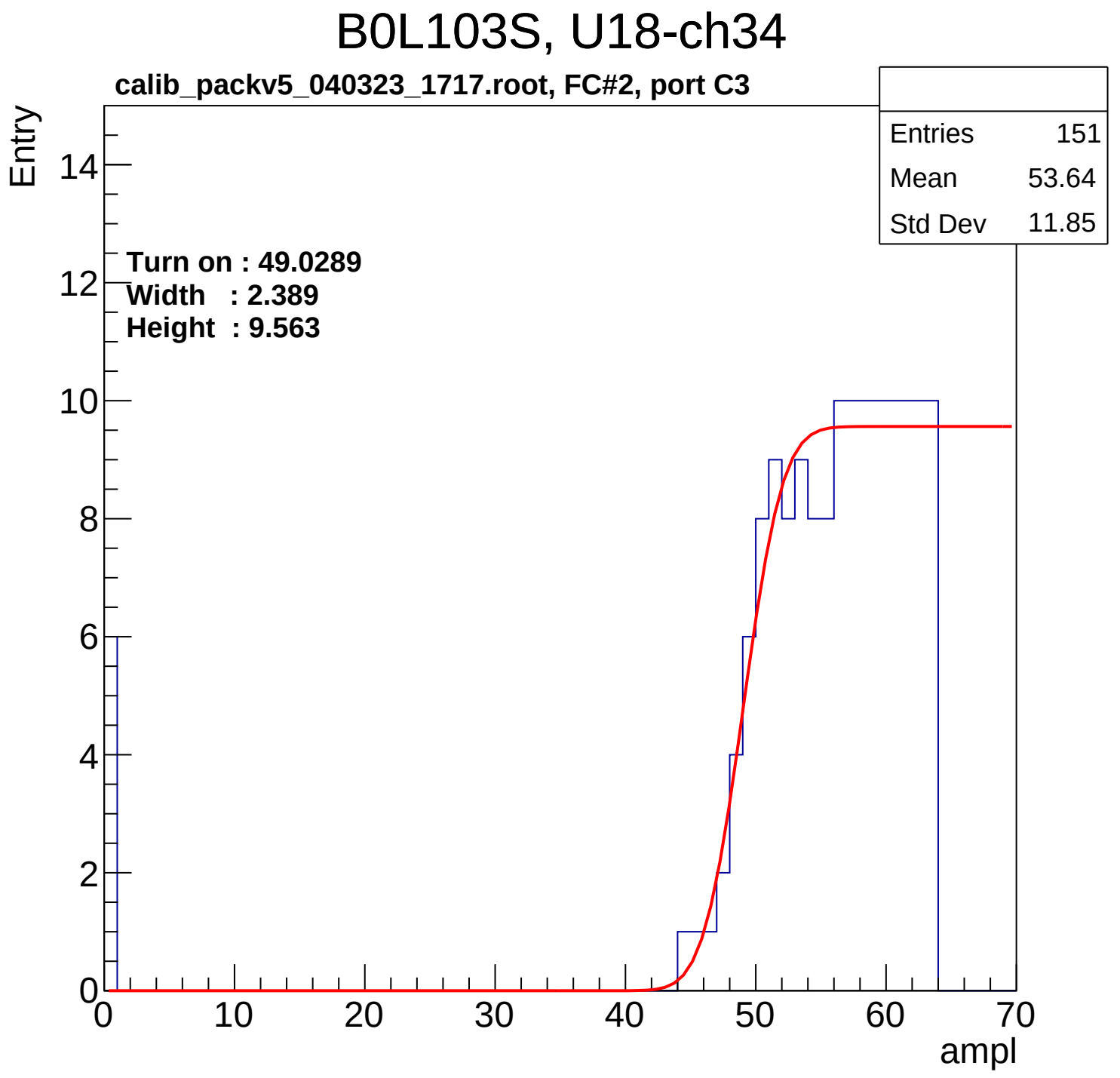
B0L103S, U18-ch34
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 53.64
Std Dev 11.85
Turn on : 49.0289
Width : 2.389
Height : 9.563
Entry
ampl
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6
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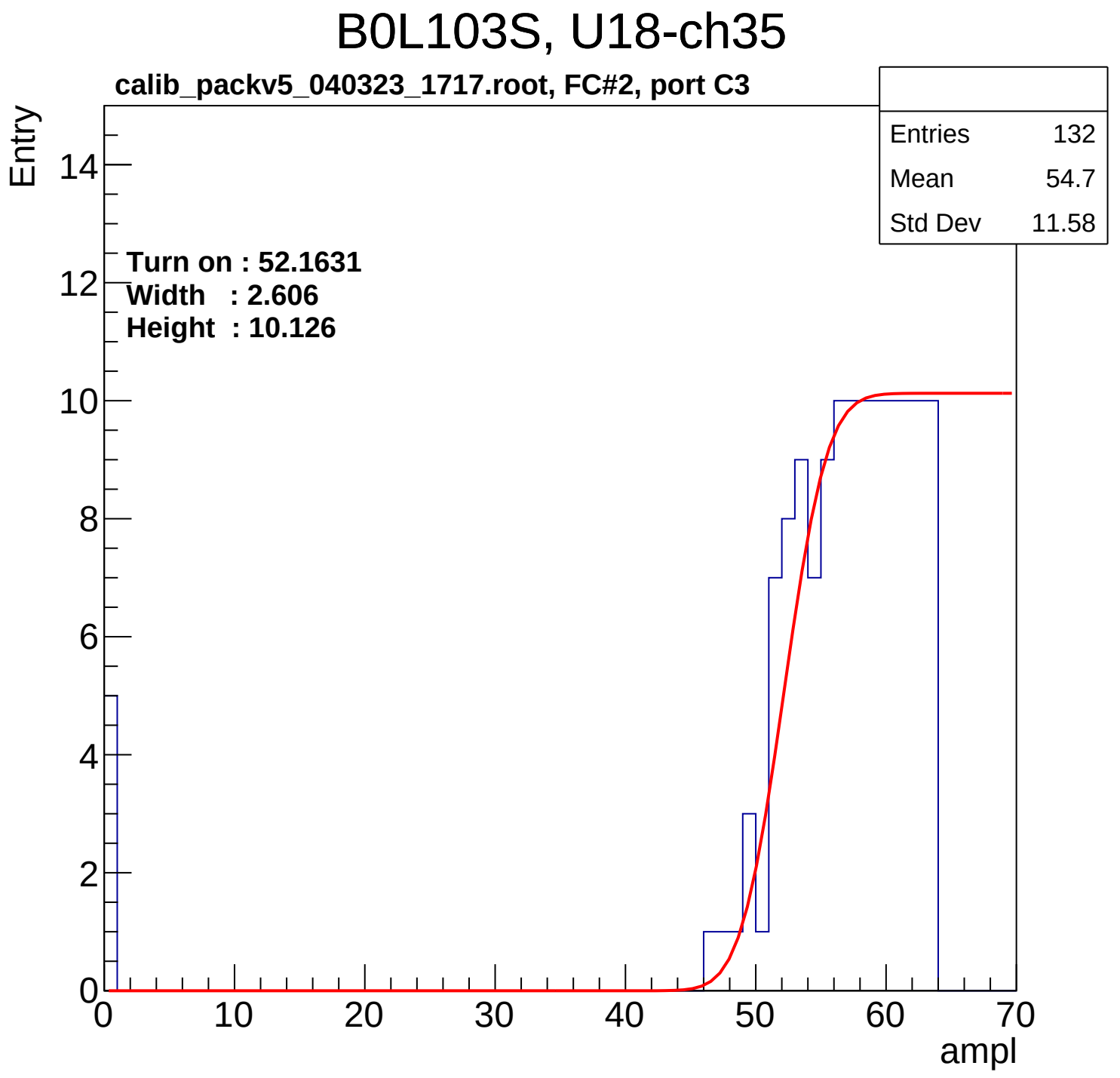
B0L103S, U18-ch35
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 54.7
Std Dev 11.58
Turn on : 52.1631
Width : 2.606
Height : 10.126
Entry
ampl
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6
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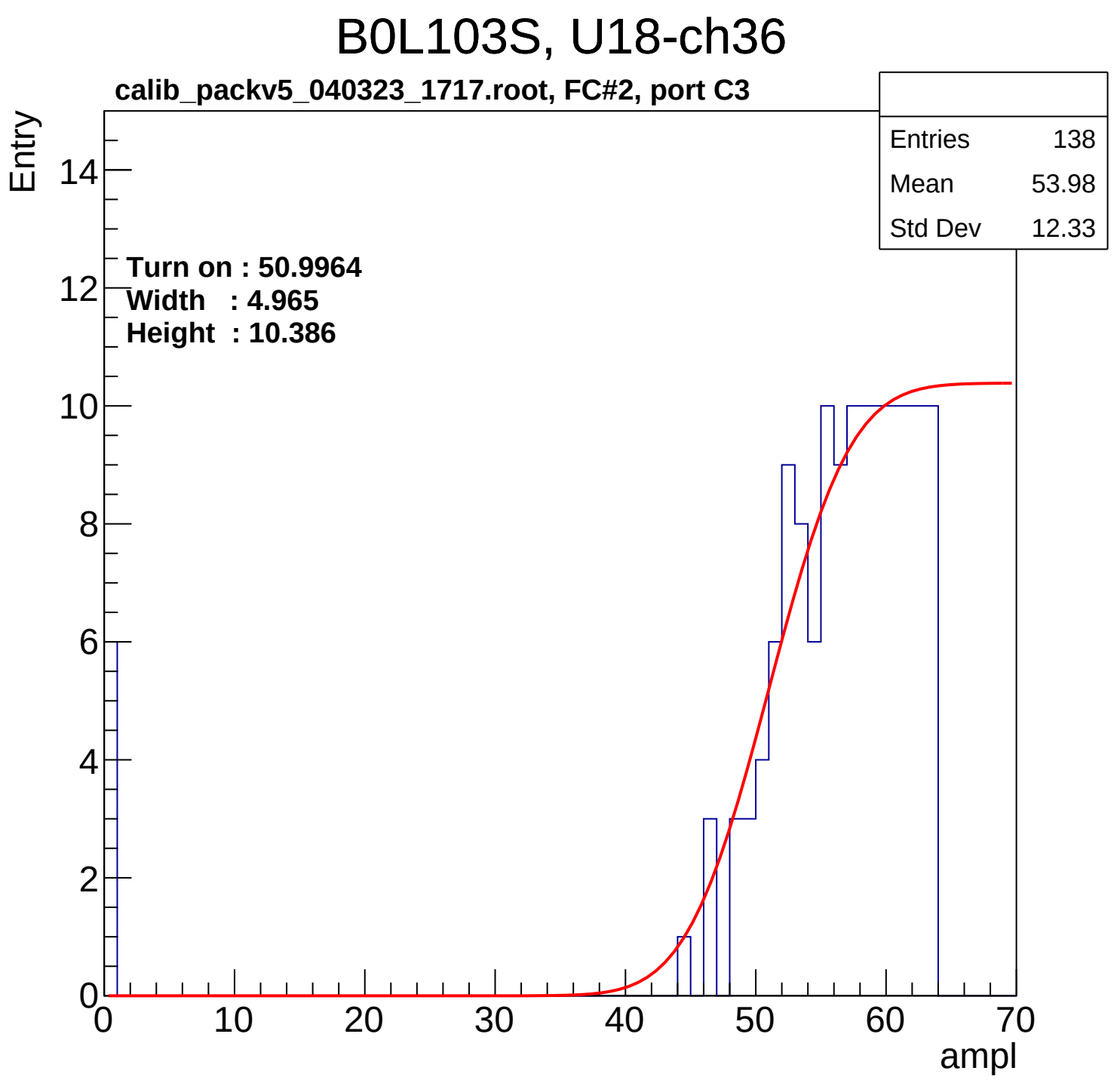
B0L103S, U18-ch36
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 53.98
Std Dev 12.33
Turn on : 50.9964
Width : 4.965
Height : 10.386
Entry
ampl
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4
6
8
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12
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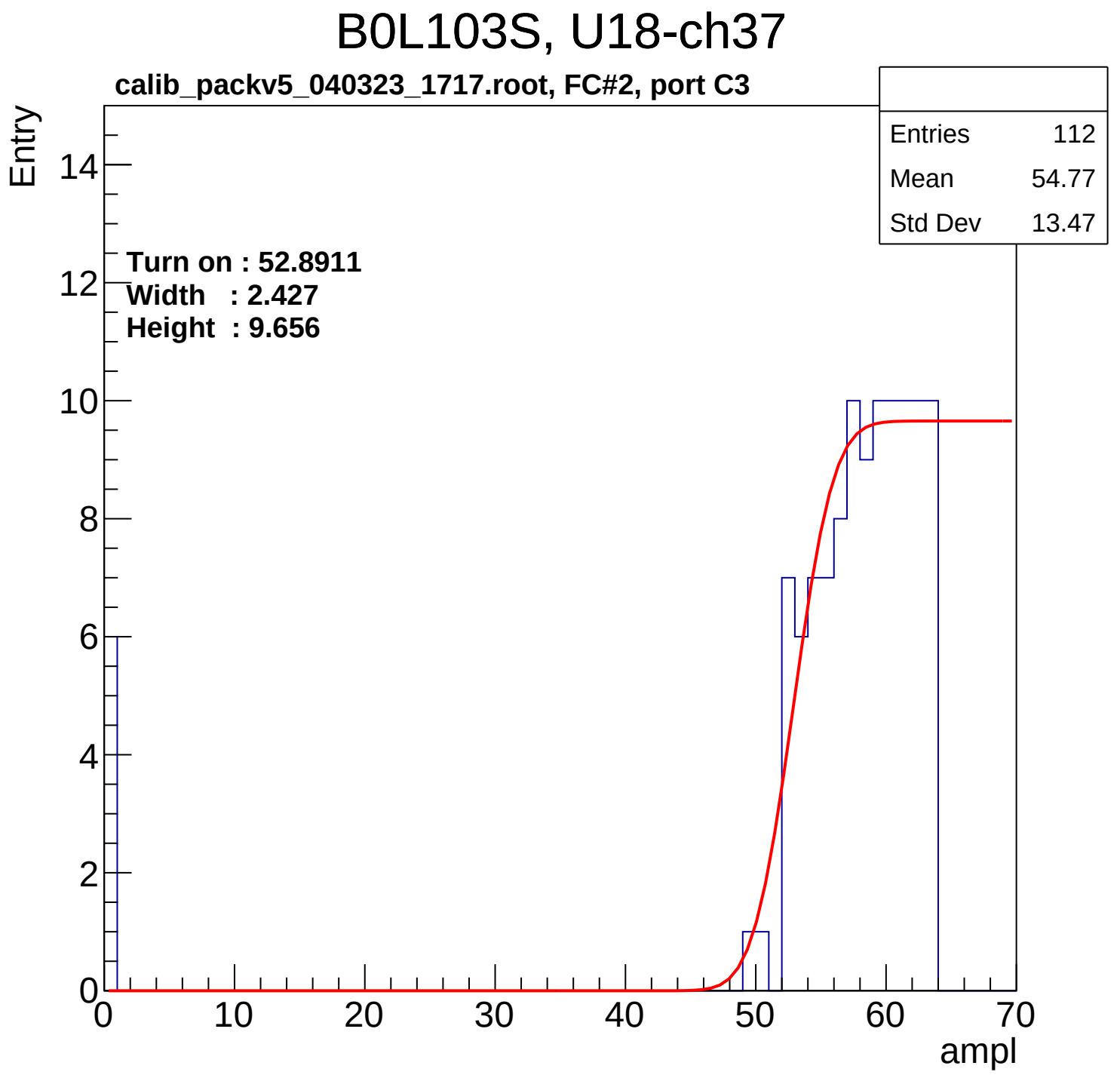
B0L103S, U18-ch37
calib_packv5_040323_1717.root, FC#2, port C3
Entries 112
Mean 54.77
Std Dev 13.47
Turn on : 52.8911
Width : 2.427
Height : 9.656
Entry
ampl
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6
8
10
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0
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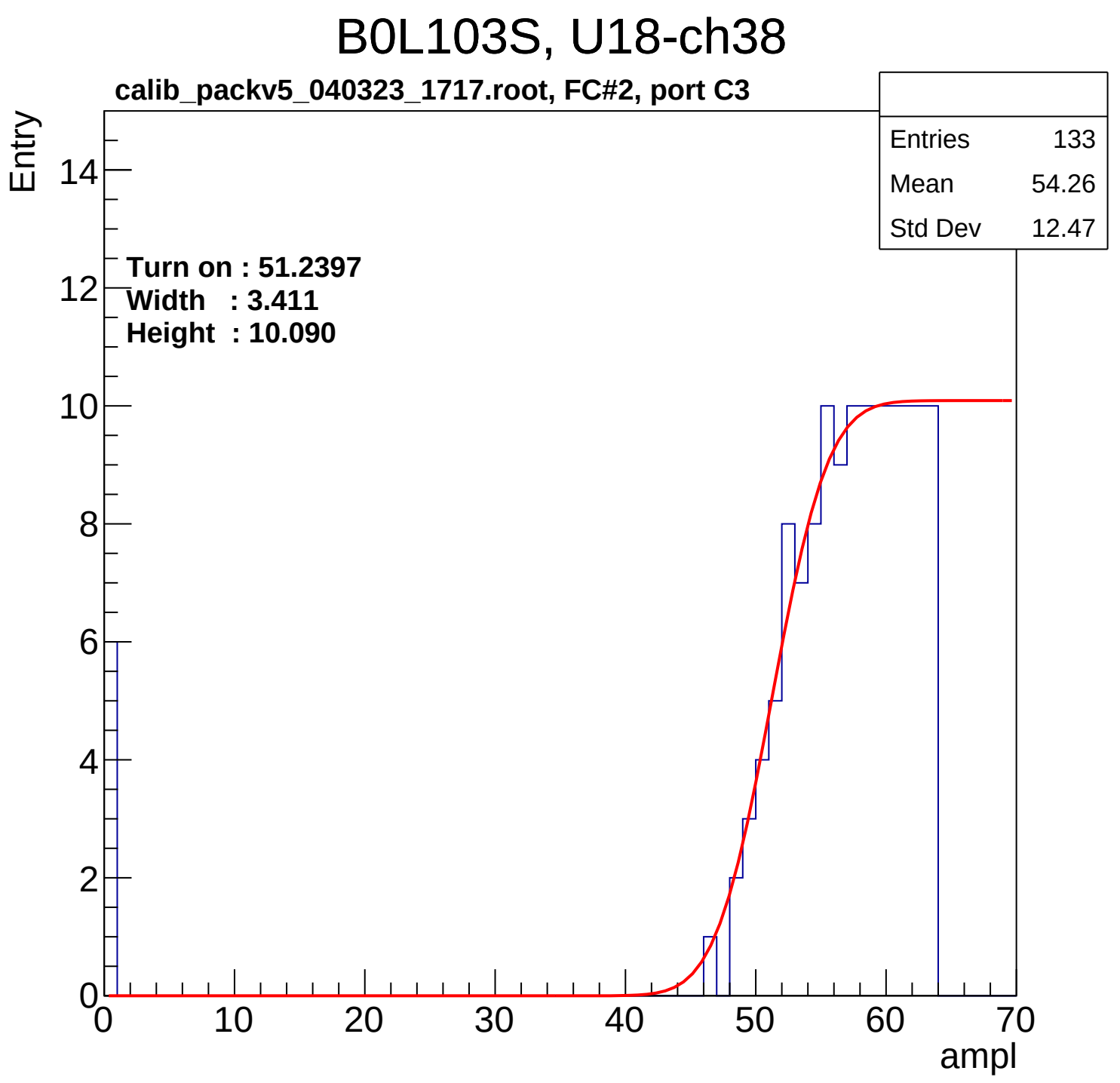
B0L103S, U18-ch38
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 54.26
Std Dev 12.47
Turn on : 51.2397
Width : 3.411
Height : 10.090
Entry
ampl
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6
8
10
12
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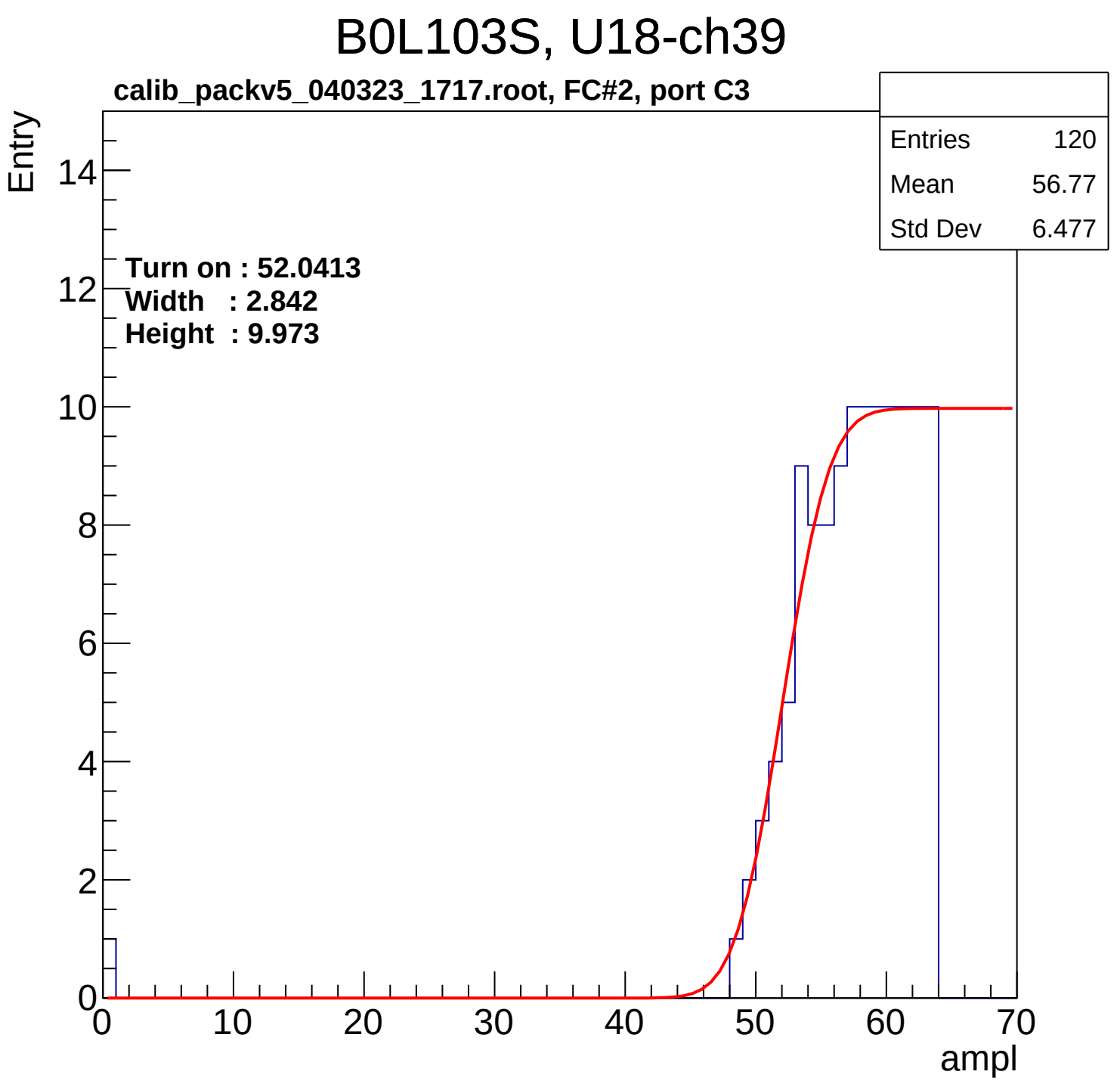
B0L103S, U18-ch39
calib_packv5_040323_1717.root, FC#2, port C3
Entries 120
Mean 56.77
Std Dev 6.477
Turn on : 52.0413
Width : 2.842
Height : 9.973
Entry
ampl
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6
8
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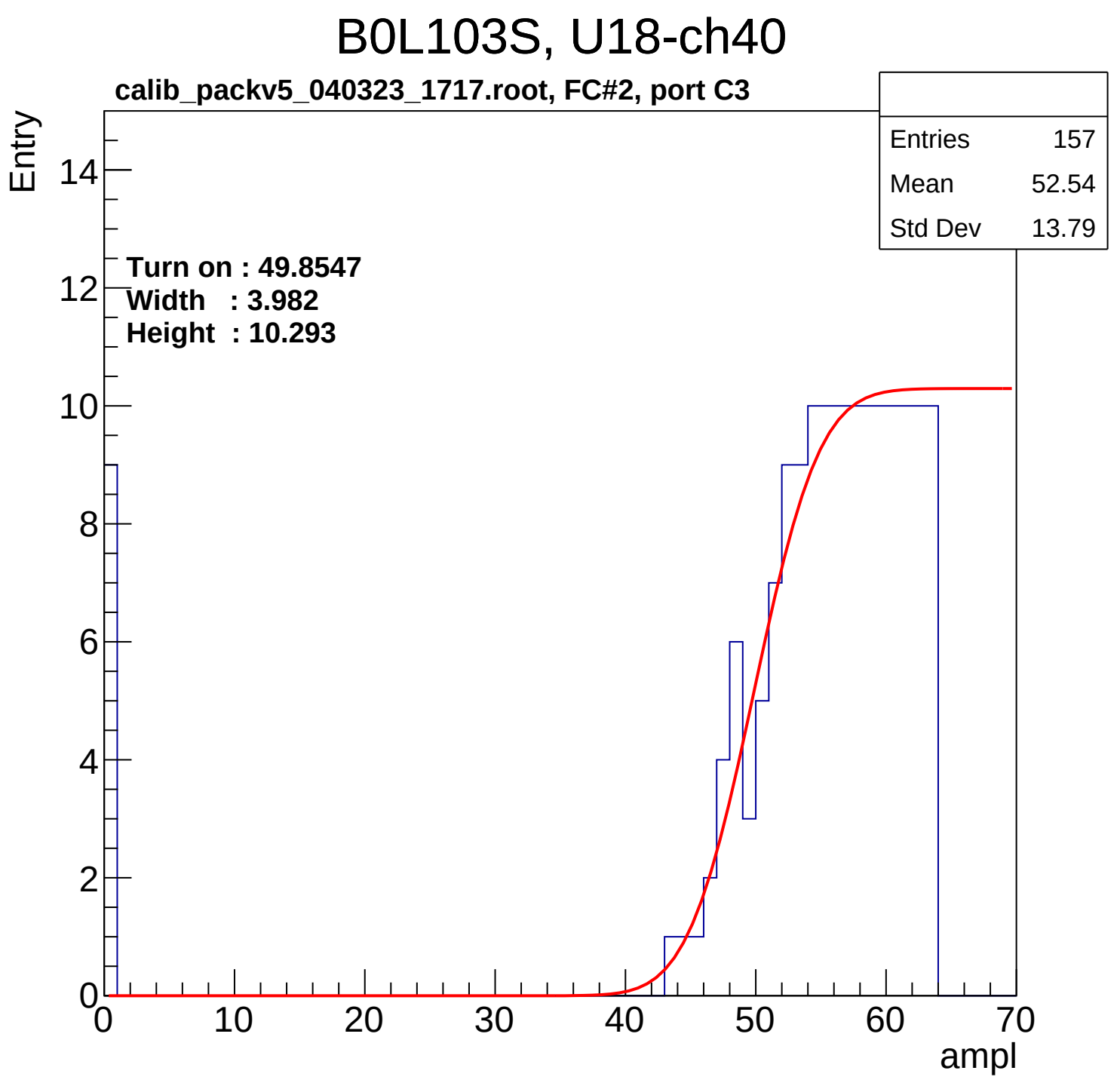
B0L103S, U18-ch40
calib_packv5_040323_1717.root, FC#2, port C3
Entries 157
Mean 52.54
Std Dev 13.79
Turn on : 49.8547
Width : 3.982
Height : 10.293
Entry
ampl
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8
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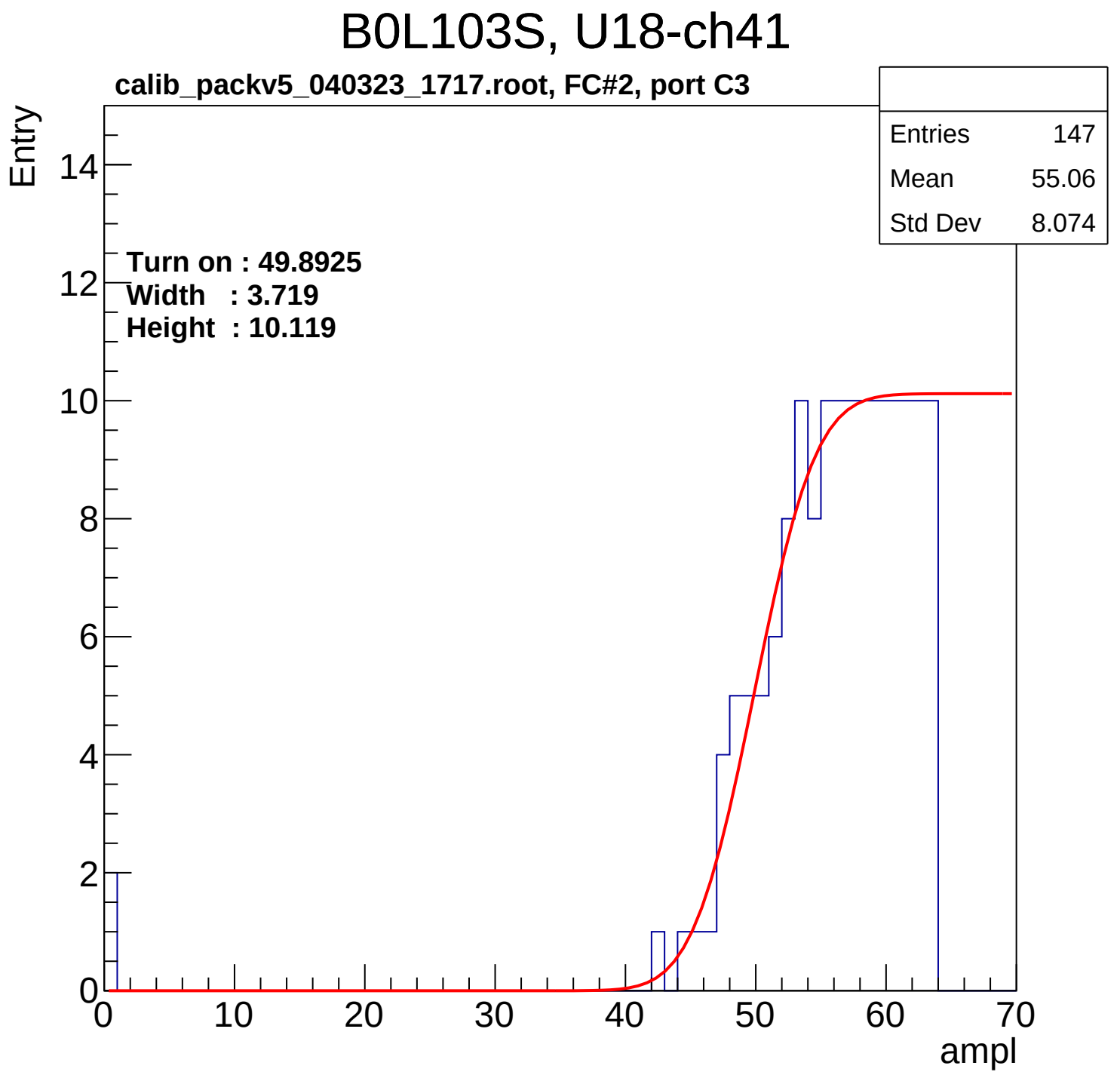
B0L103S, U18-ch41
calib_packv5_040323_1717.root, FC#2, port C3
Entries 147
Mean 55.06
Std Dev 8.074
Turn on : 49.8925
Width : 3.719
Height : 10.119
Entry
ampl
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6
8
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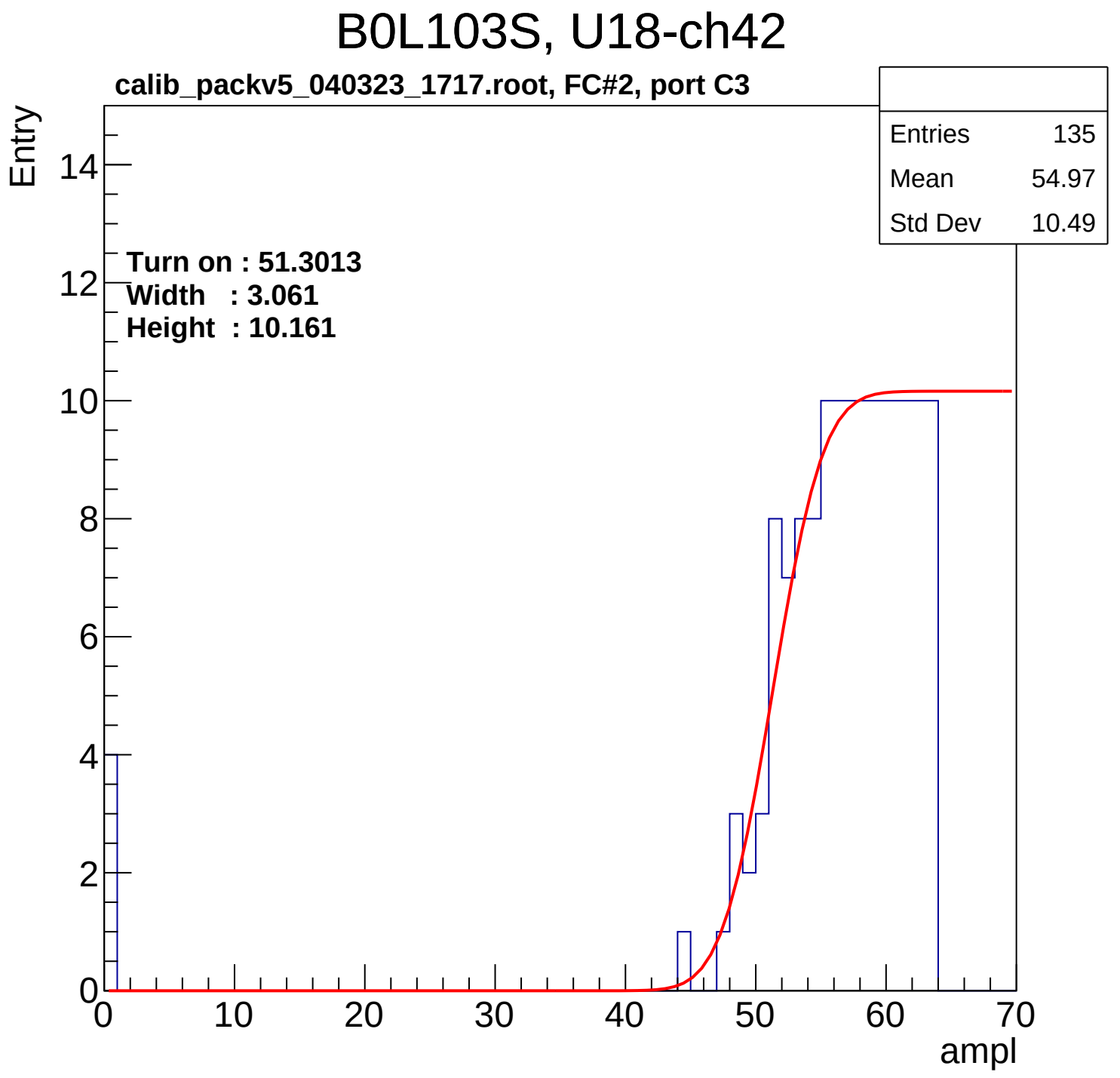
B0L103S, U18-ch42
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 54.97
Std Dev 10.49
Turn on : 51.3013
Width : 3.061
Height : 10.161
Entry
ampl
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6
8
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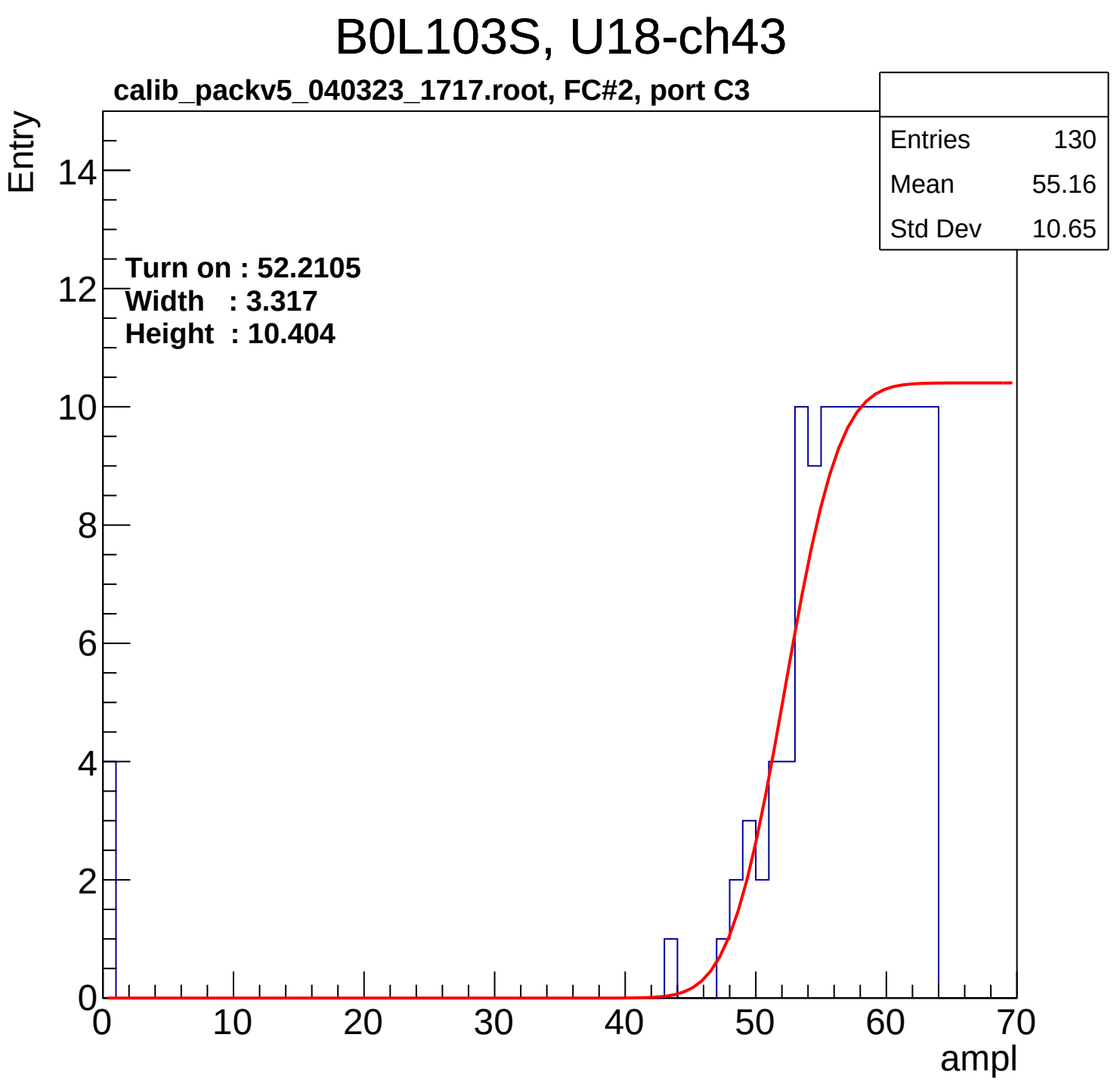
B0L103S, U18-ch43
calib_packv5_040323_1717.root, FC#2, port C3
Entries 130
Mean 55.16
Std Dev 10.65
Turn on : 52.2105
Width : 3.317
Height : 10.404
Entry
ampl
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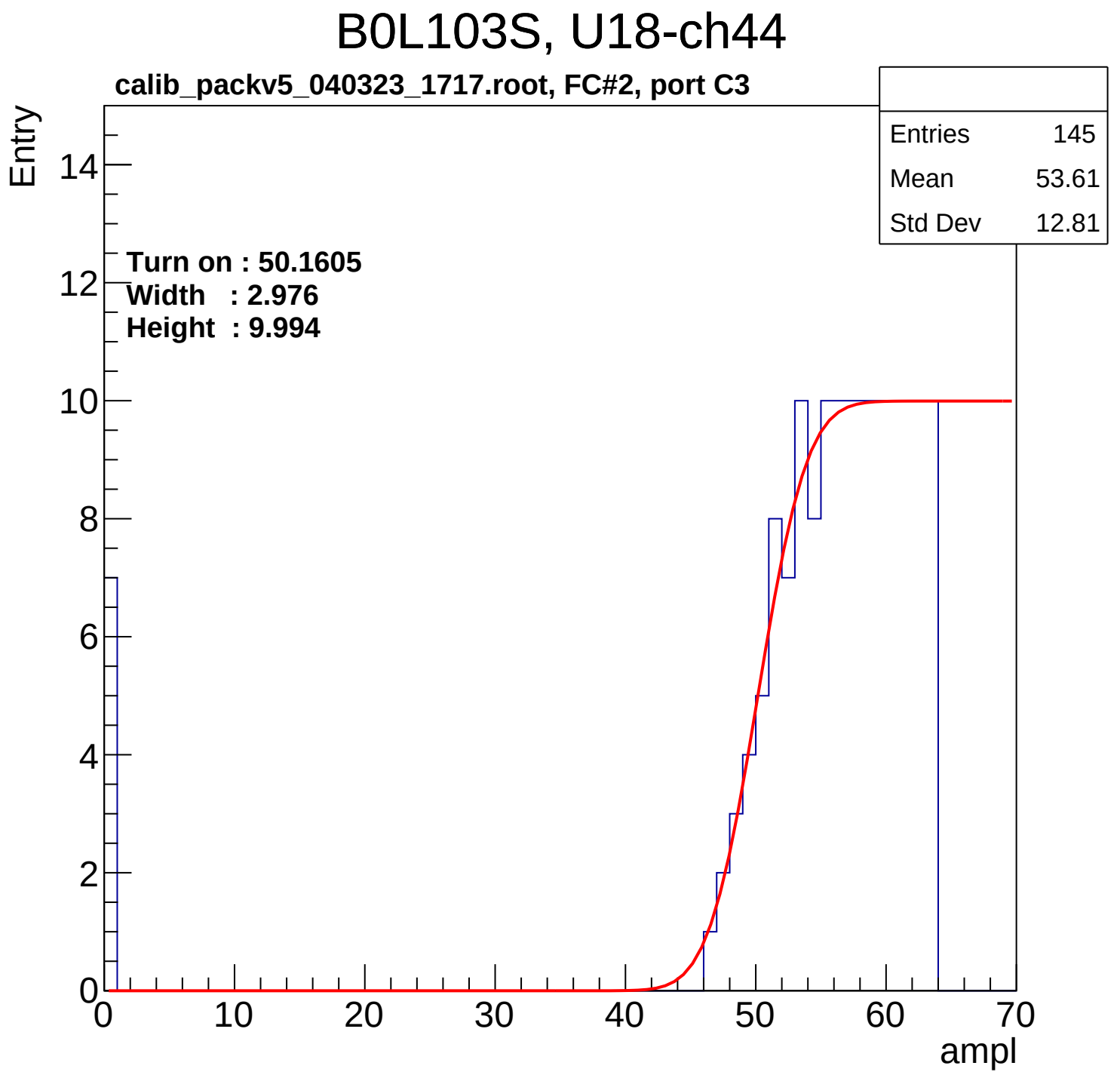
B0L103S, U18-ch44
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 53.61
Std Dev 12.81
Turn on : 50.1605
Width : 2.976
Height : 9.994
Entry
ampl
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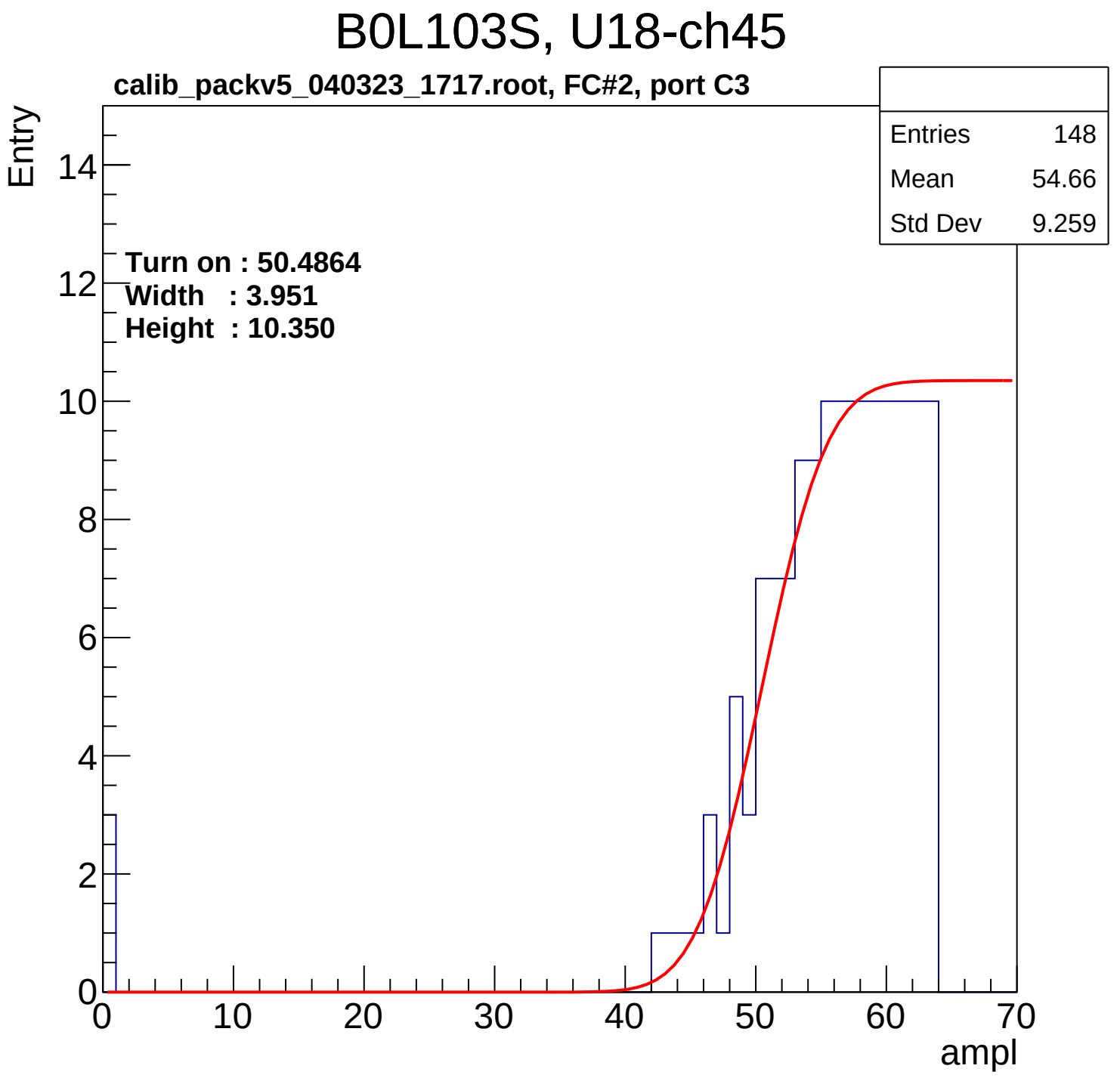
B0L103S, U18-ch45
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 54.66
Std Dev 9.259
Turn on : 50.4864
Width : 3.951
Height : 10.350
Entry
ampl
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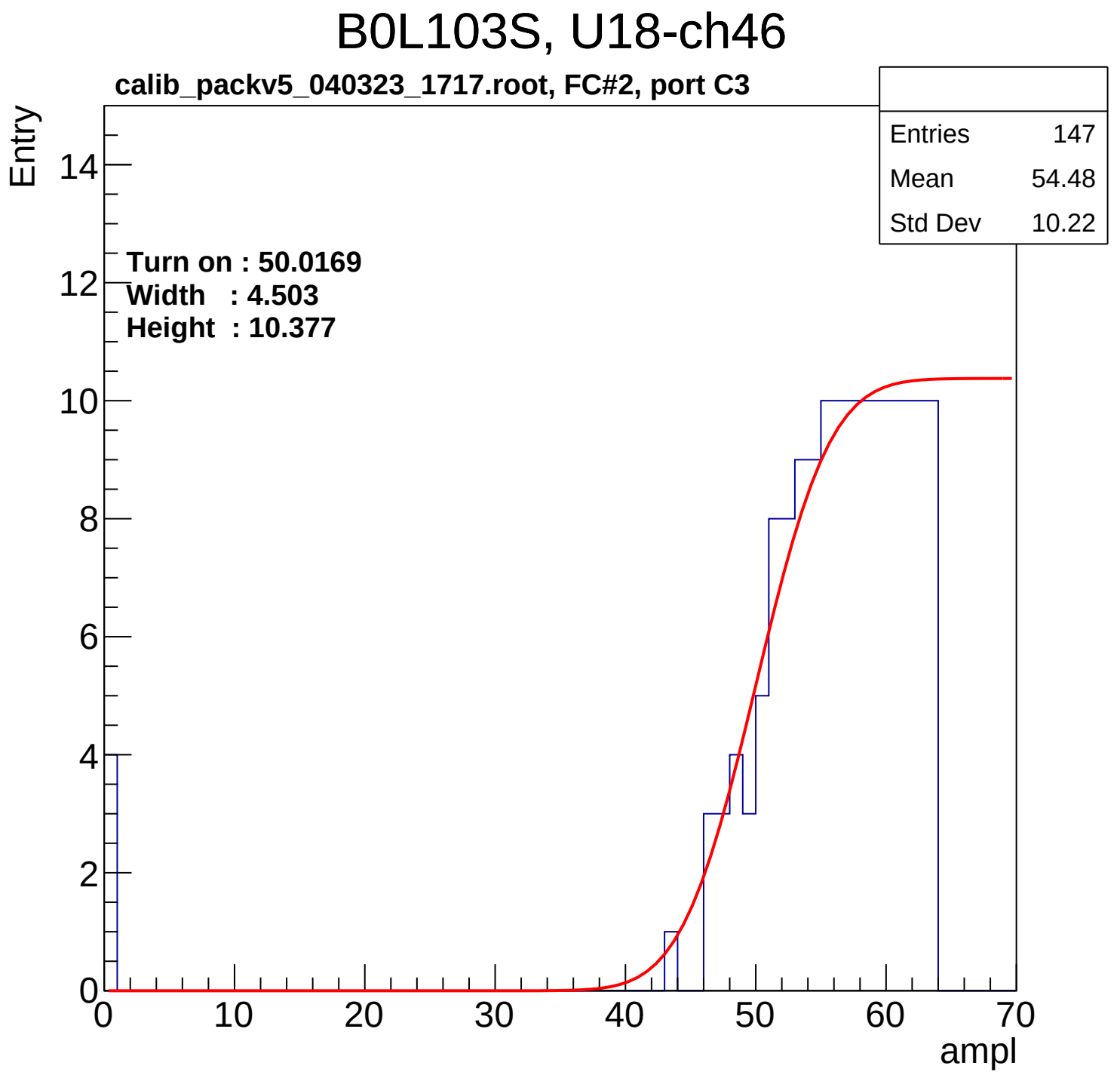
B0L103S, U18-ch46
calib_packv5_040323_1717.root, FC#2, port C3
Entries 147
Mean 54.48
Std Dev 10.22
Turn on : 50.0169
Width : 4.503
Height : 10.377
Entry
ampl
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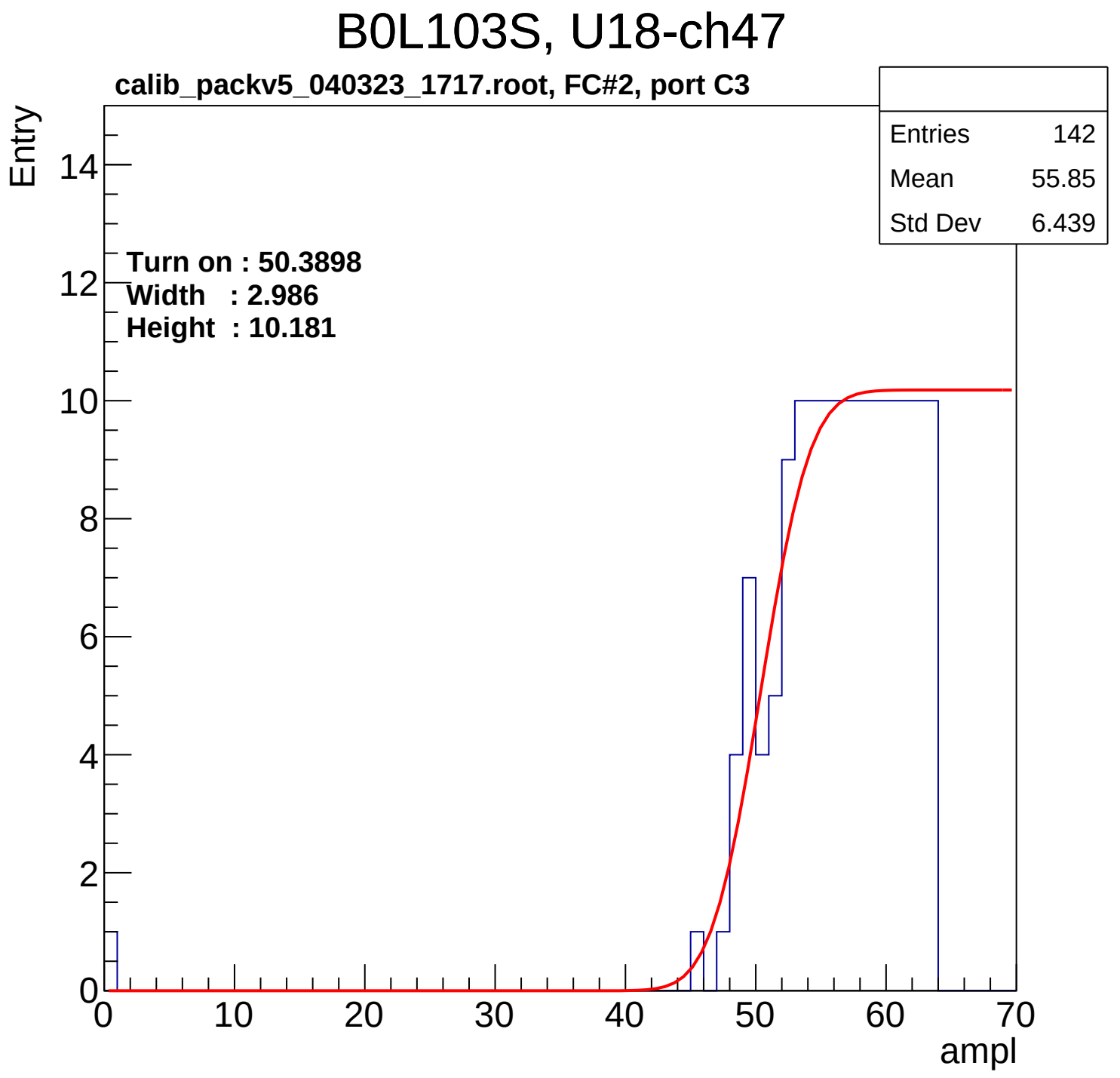
B0L103S, U18-ch47
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 55.85
Std Dev 6.439
Turn on : 50.3898
Width : 2.986
Height : 10.181
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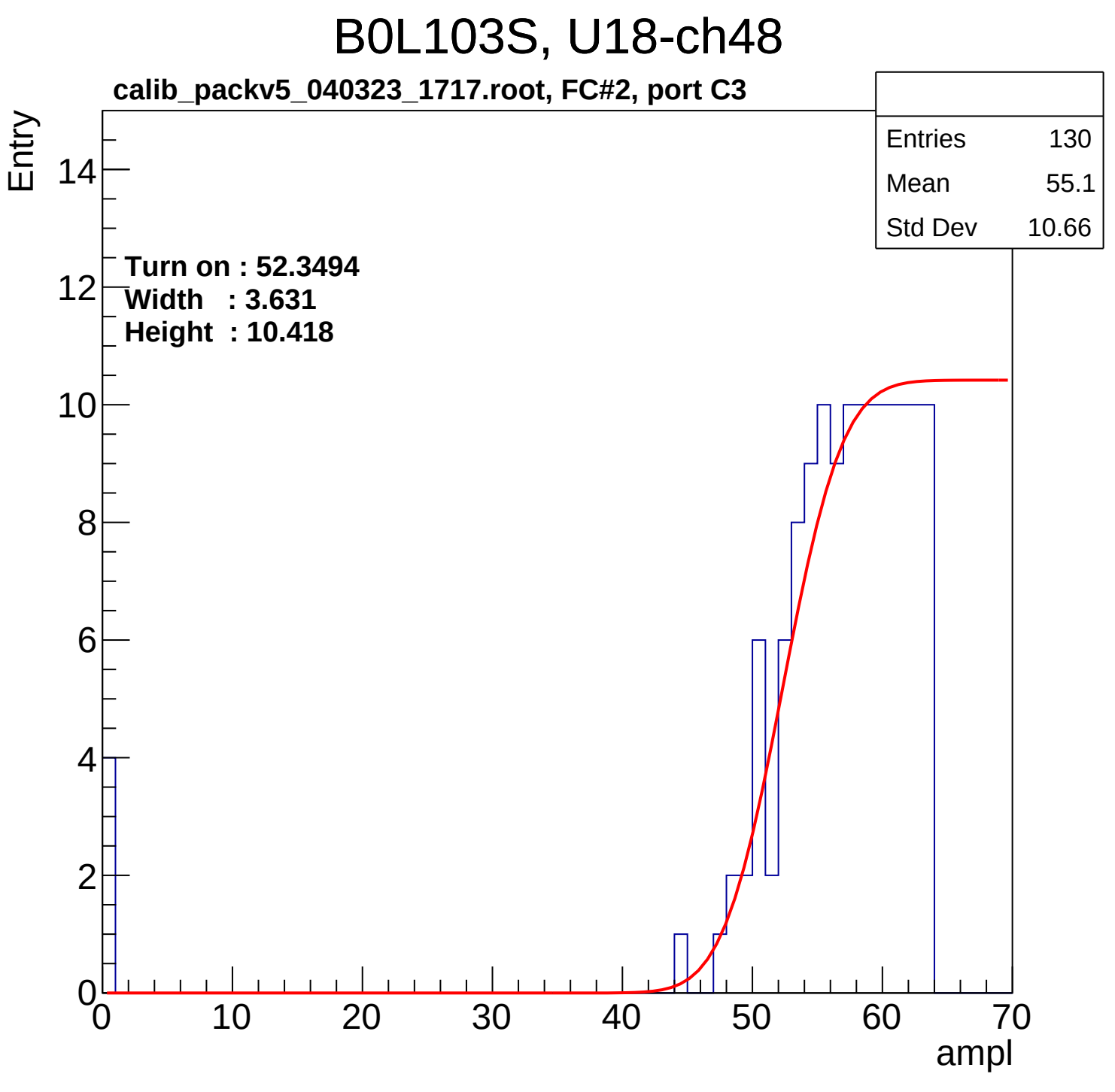
B0L103S, U18-ch48
calib_packv5_040323_1717.root, FC#2, port C3
Entries 130
Mean 55.1
Std Dev 10.66
Turn on : 52.3494
Width : 3.631
Height : 10.418
Entry
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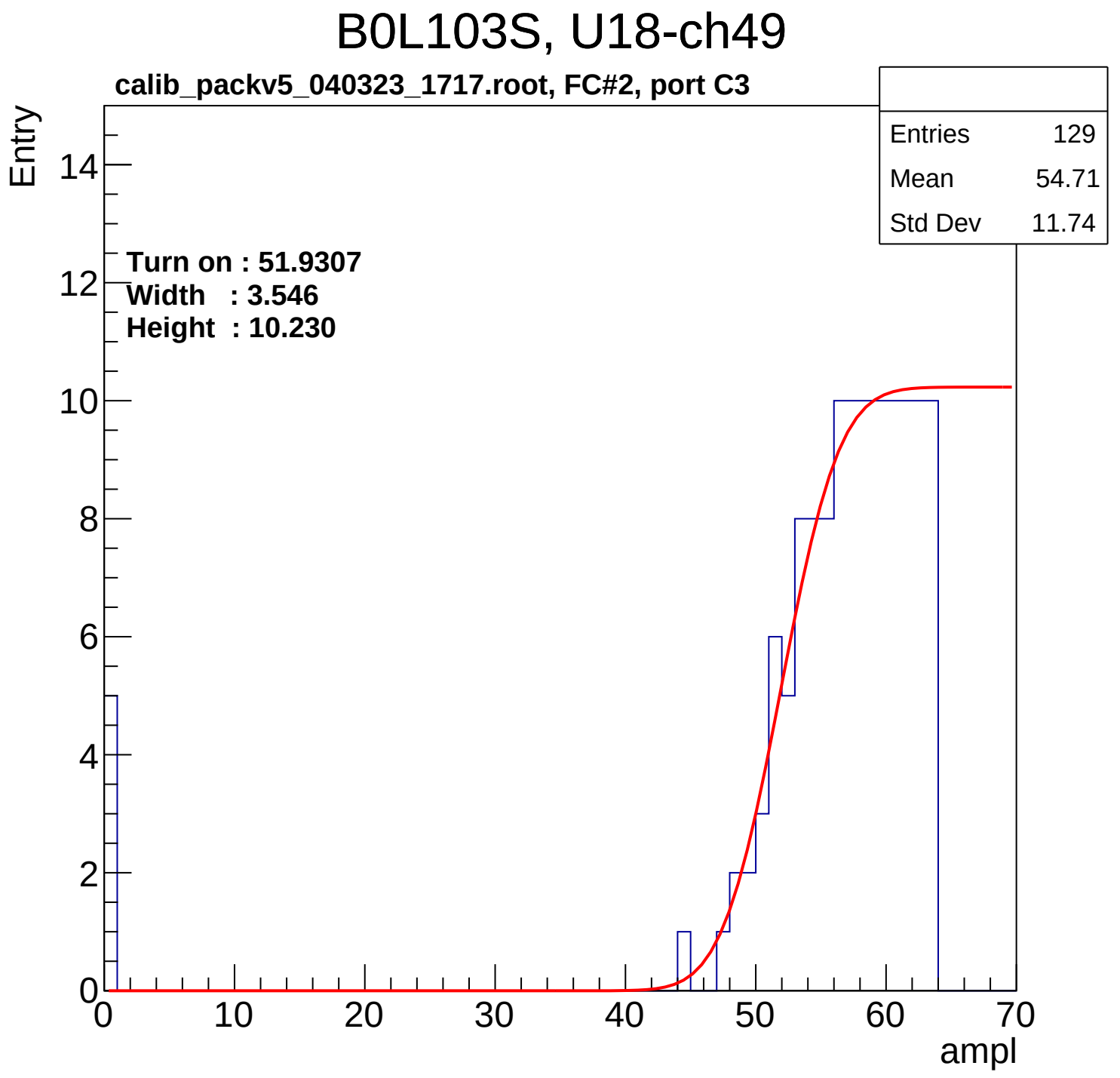
B0L103S, U18-ch49
calib_packv5_040323_1717.root, FC#2, port C3
Entries 129
Mean 54.71
Std Dev 11.74
Turn on : 51.9307
Width : 3.546
Height : 10.230
Entry
ampl
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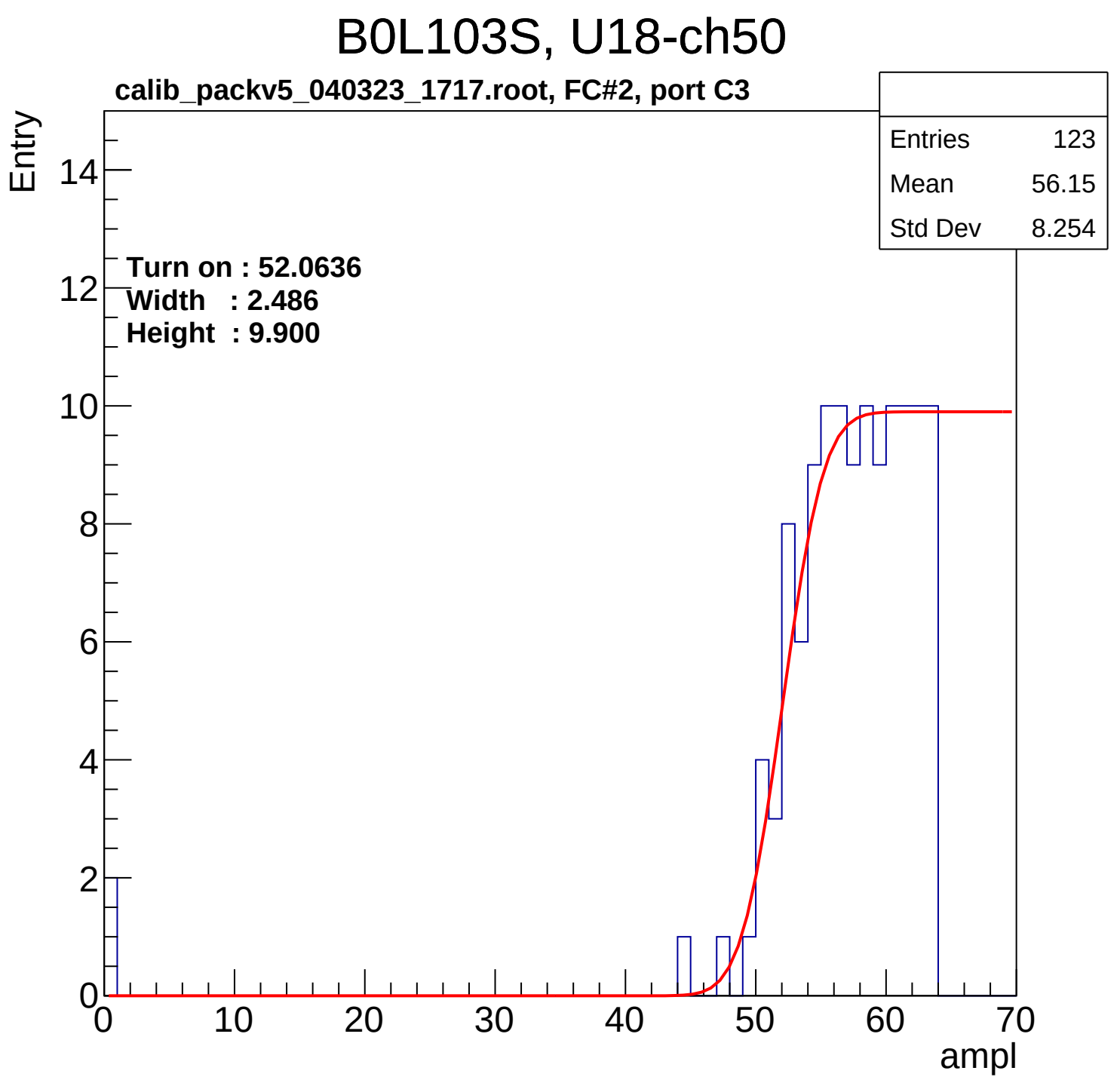
B0L103S, U18-ch50
calib_packv5_040323_1717.root, FC#2, port C3
Entries 123
Mean 56.15
Std Dev 8.254
Turn on : 52.0636
Width : 2.486
Height : 9.900
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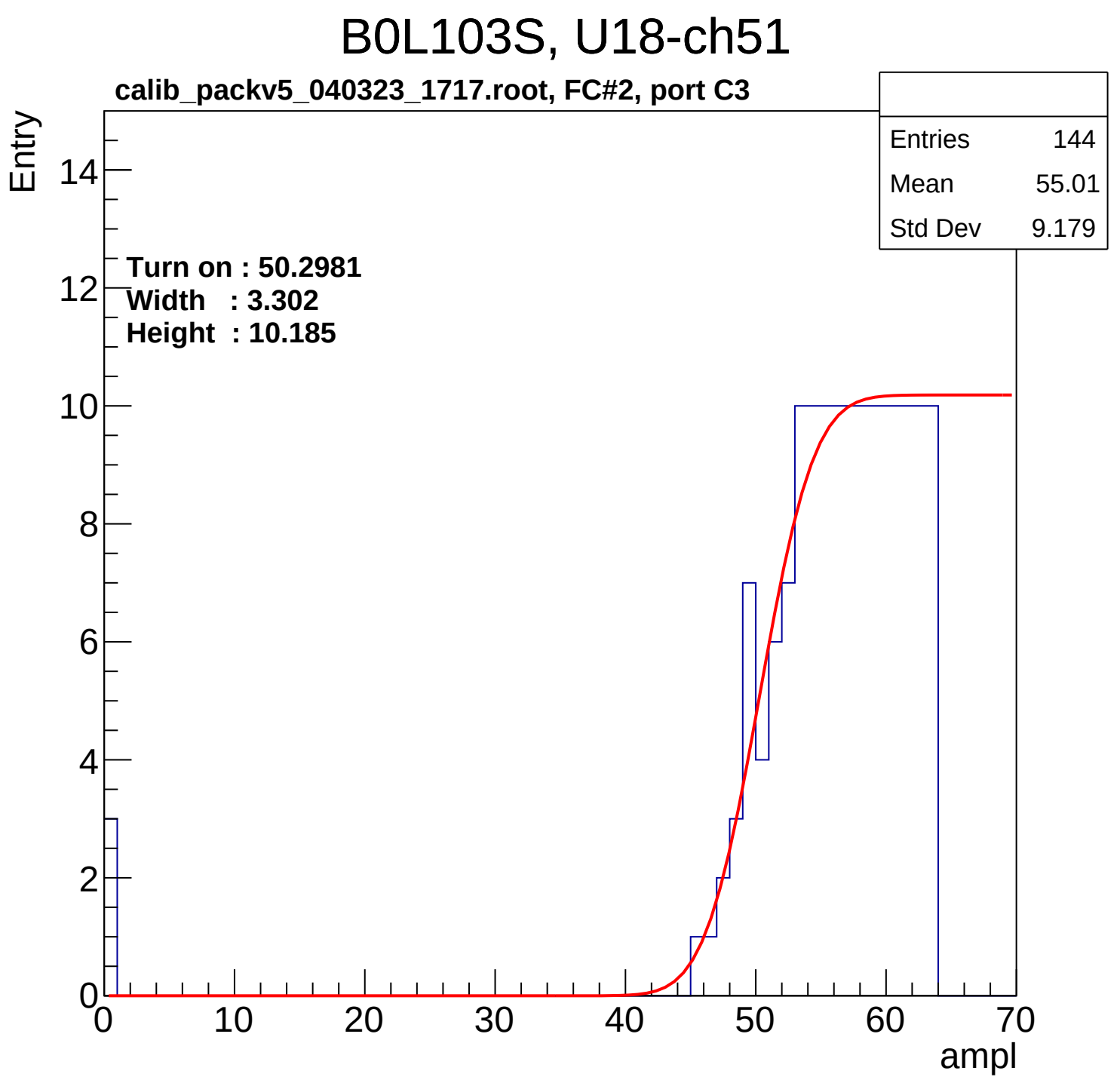
B0L103S, U18-ch51
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 55.01
Std Dev 9.179
Turn on : 50.2981
Width : 3.302
Height : 10.185
Entry
ampl
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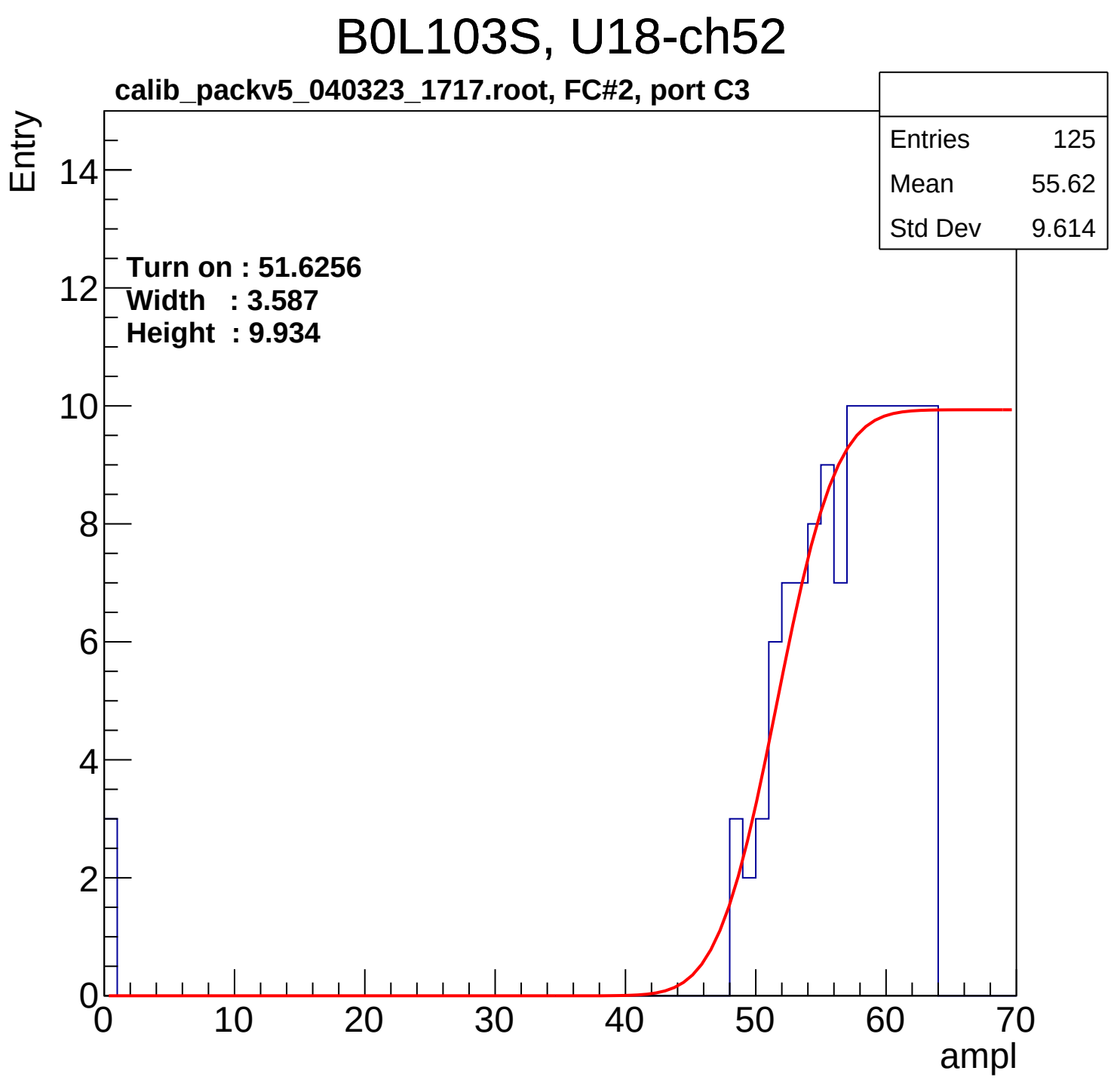
B0L103S, U18-ch52
calib_packv5_040323_1717.root, FC#2, port C3
Entries 125
Mean 55.62
Std Dev 9.614
Turn on : 51.6256
Width : 3.587
Height : 9.934
Entry
ampl
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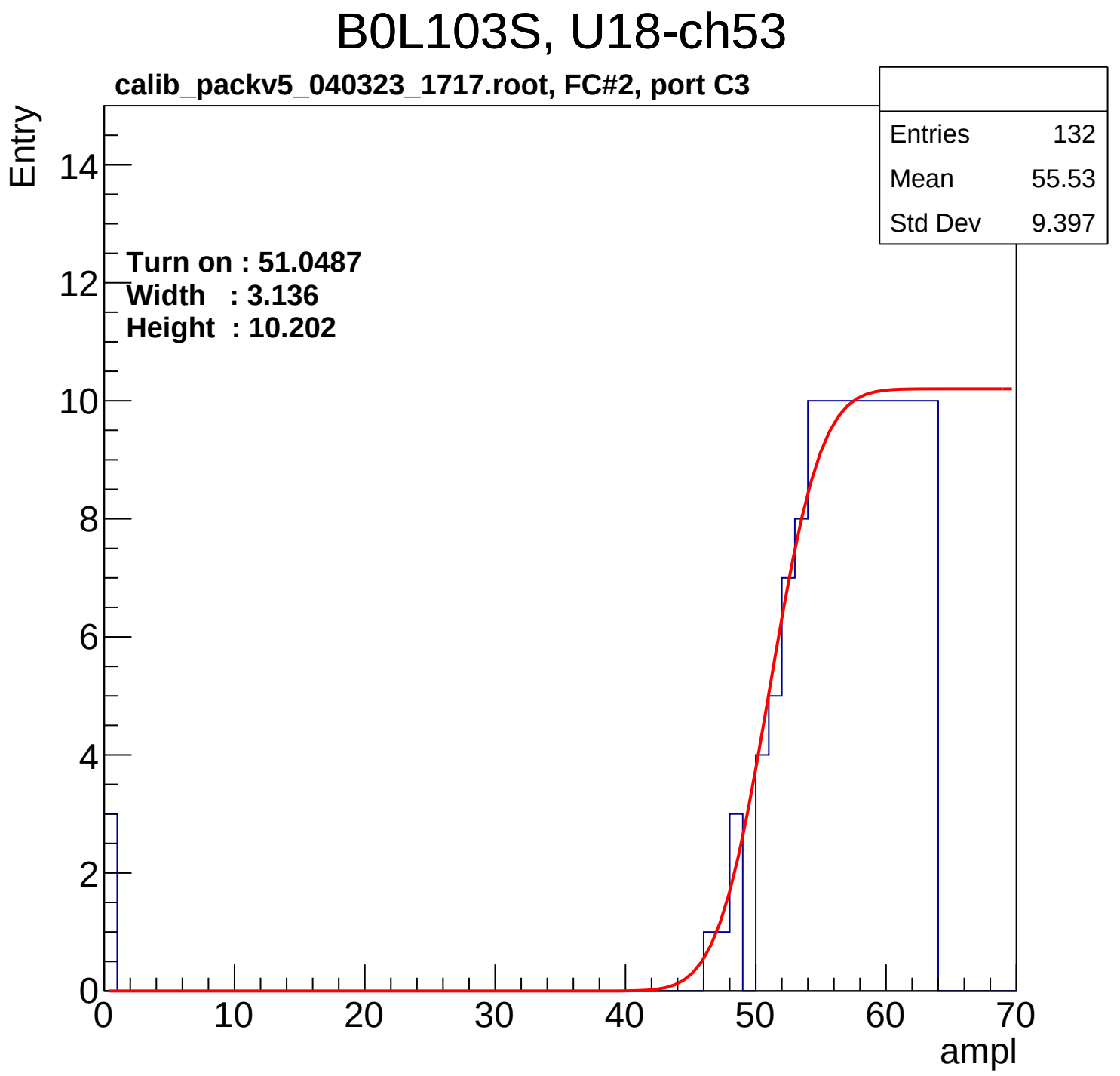
B0L103S, U18-ch53
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 55.53
Std Dev 9.397
Turn on : 51.0487
Width : 3.136
Height : 10.202
Entry
ampl
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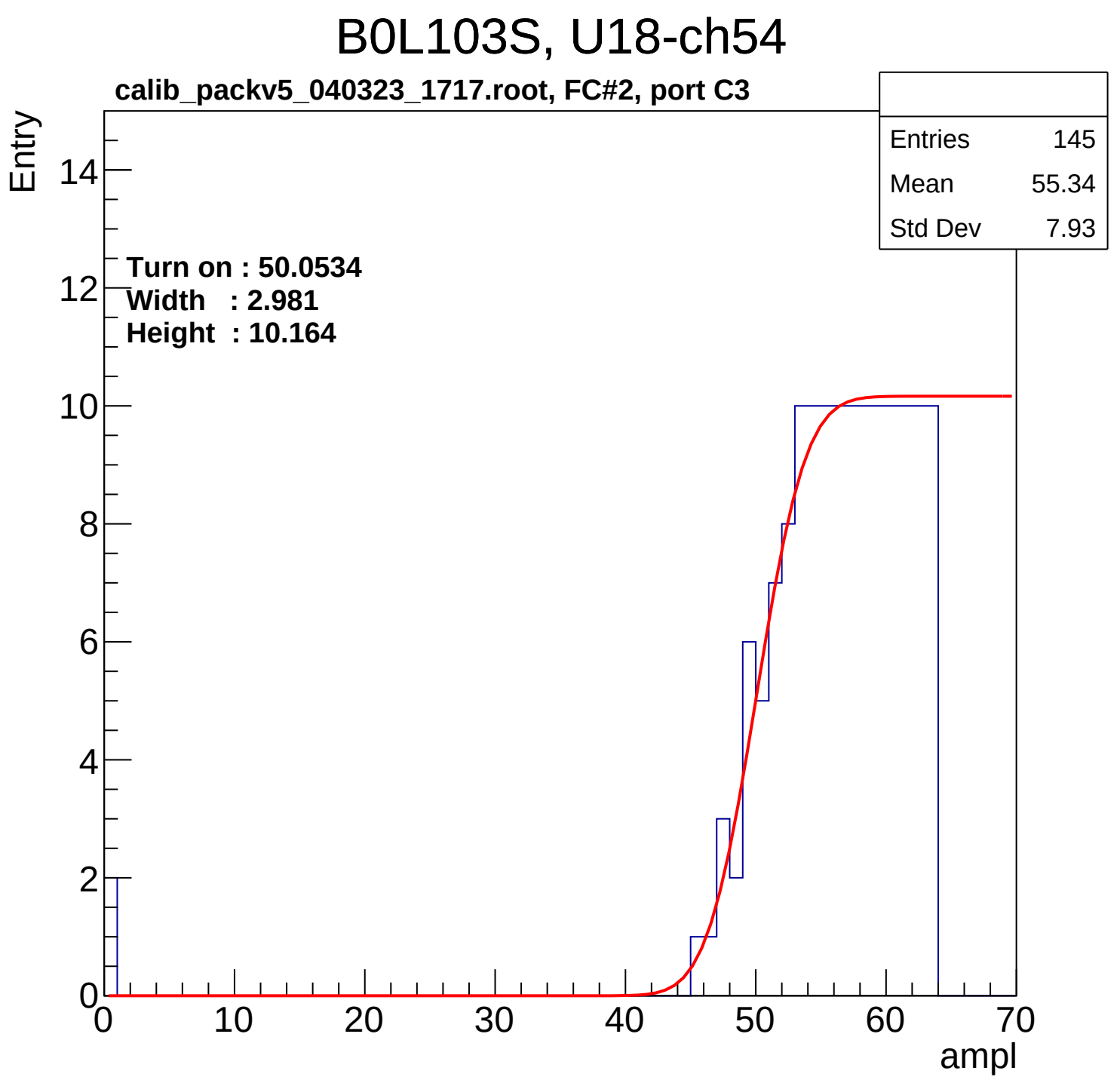
B0L103S, U18-ch54
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 55.34
Std Dev 7.93
Turn on : 50.0534
Width : 2.981
Height : 10.164
Entry
ampl
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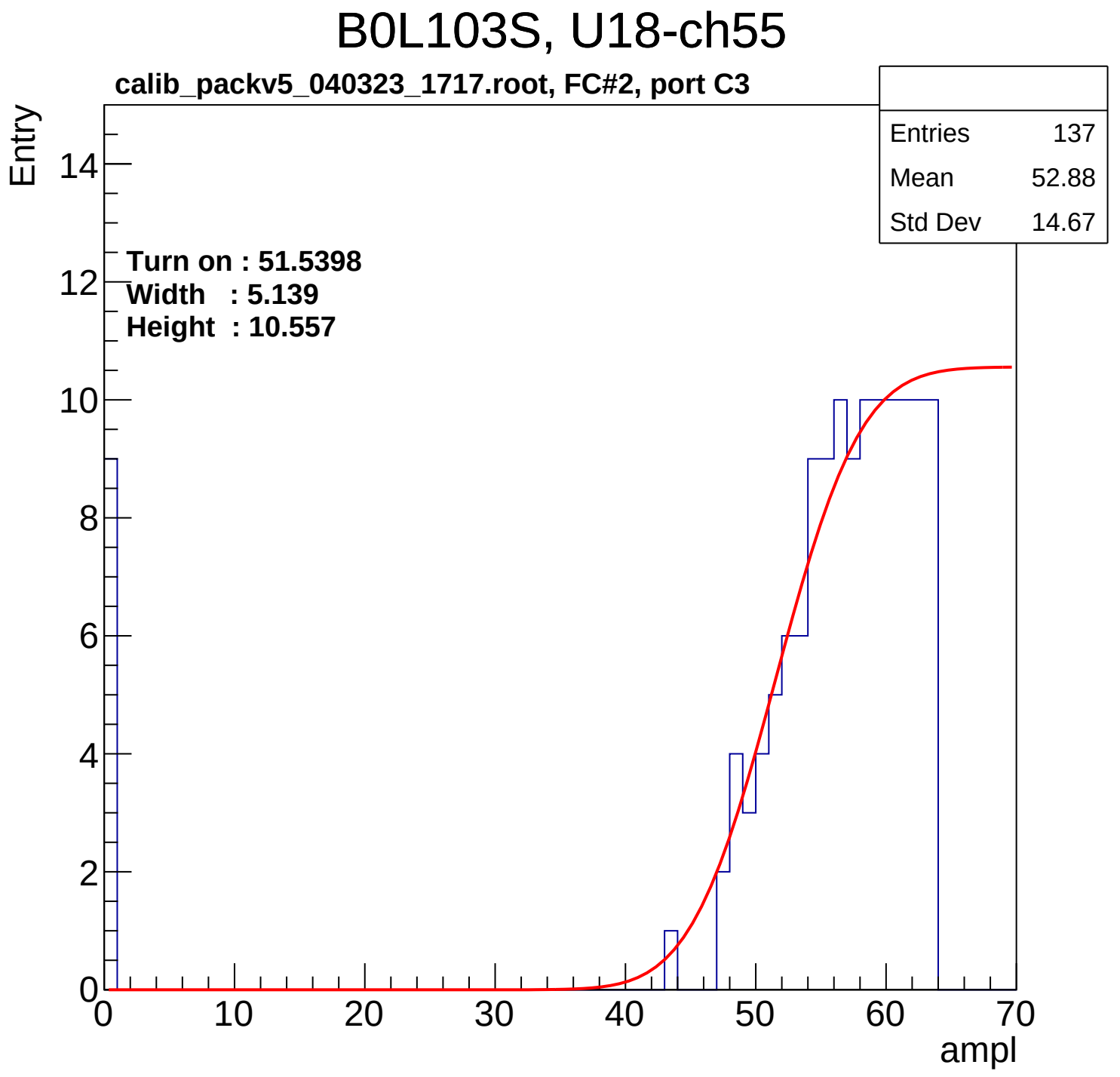
B0L103S, U18-ch55
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 52.88
Std Dev 14.67
Turn on : 51.5398
Width : 5.139
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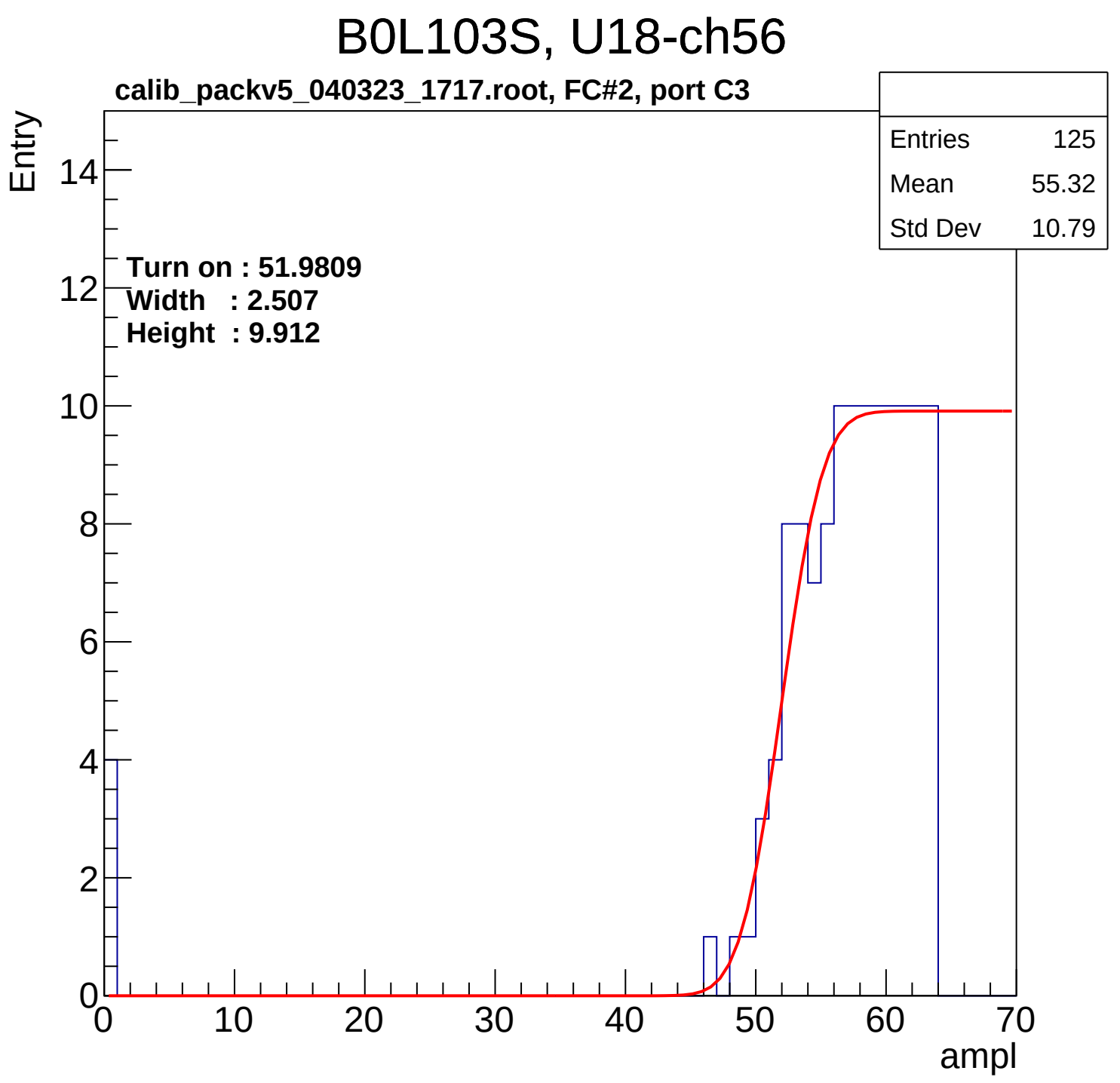
B0L103S, U18-ch56
calib_packv5_040323_1717.root, FC#2, port C3
Entries 125
Mean 55.32
Std Dev 10.79
Turn on : 51.9809
Width : 2.507
Height : 9.912
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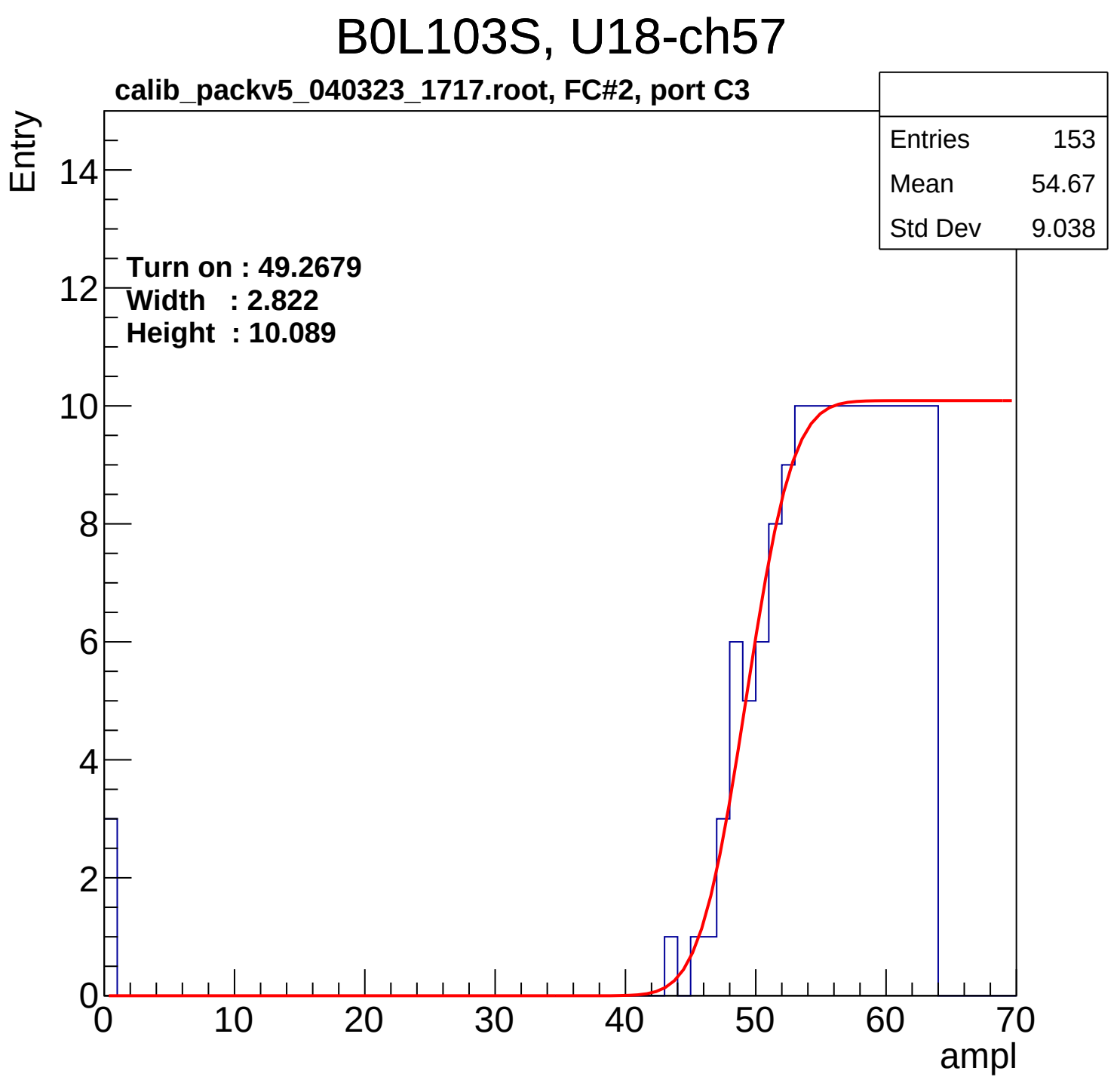
B0L103S, U18-ch57
calib_packv5_040323_1717.root, FC#2, port C3
Entries 153
Mean 54.67
Std Dev 9.038
Turn on : 49.2679
Width : 2.822
Height : 10.089
Entry
ampl
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4
6
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12
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20
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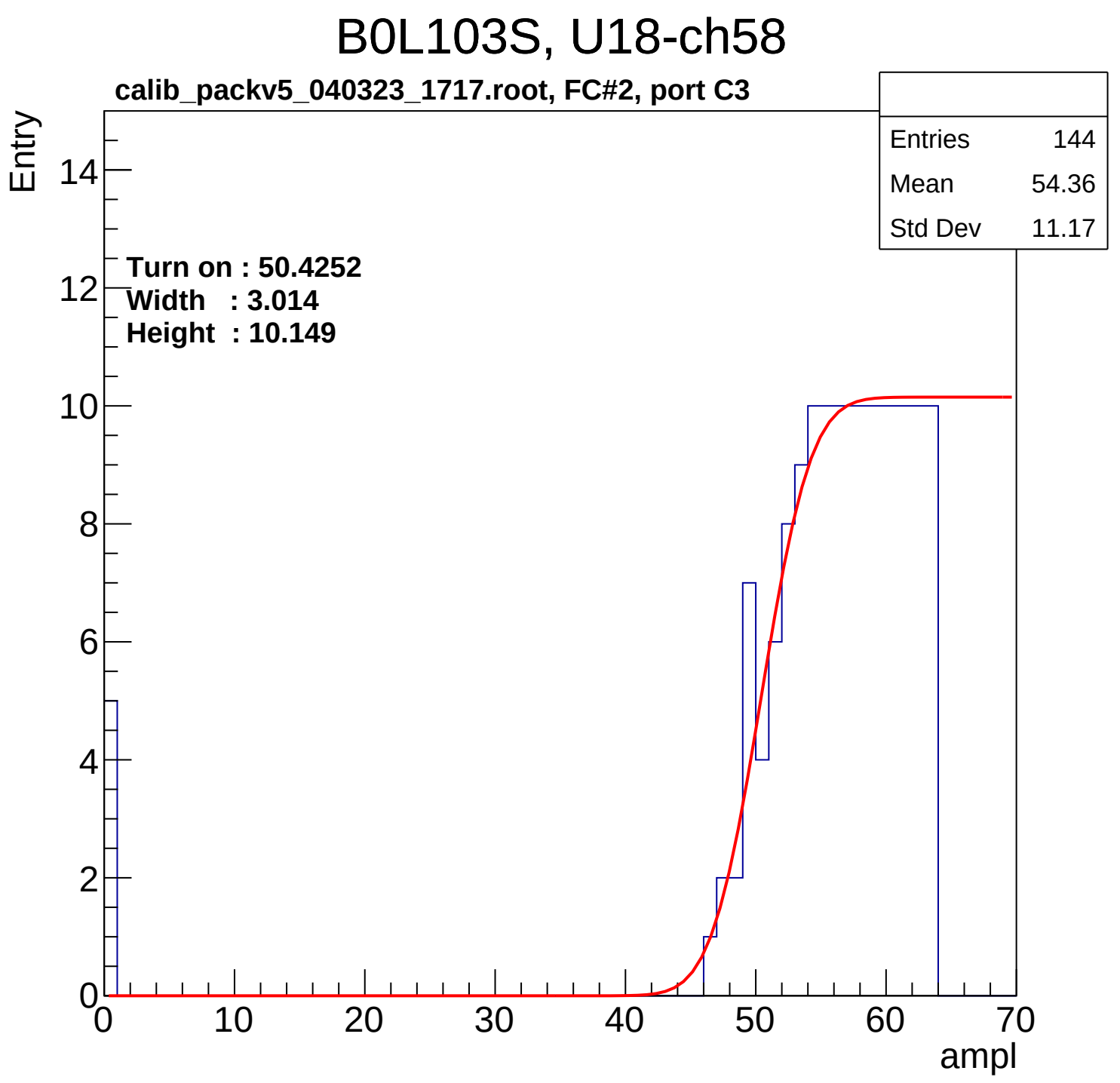
B0L103S, U18-ch58
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 54.36
Std Dev 11.17
Turn on : 50.4252
Width : 3.014
Height : 10.149
Entry
ampl
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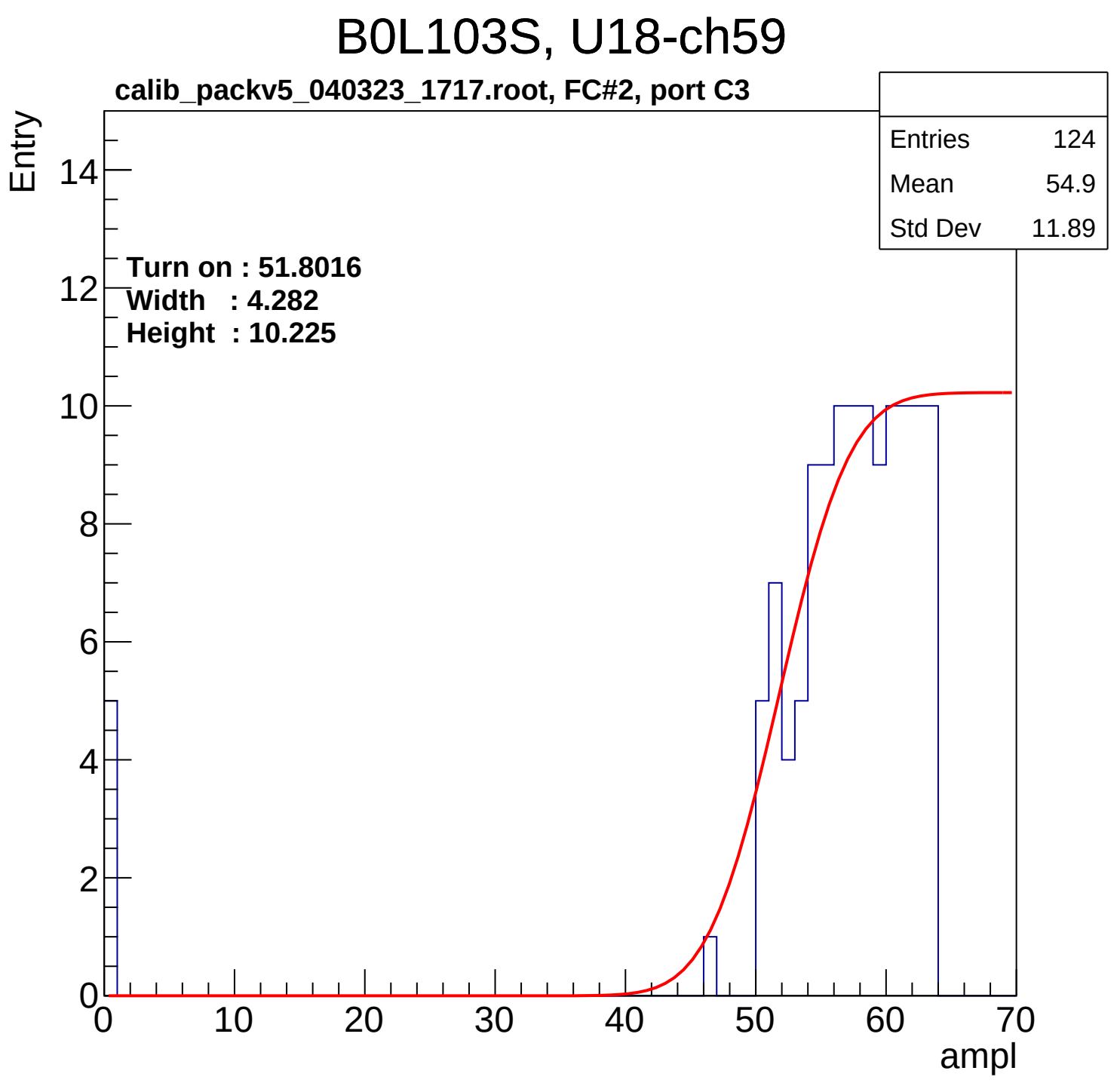
B0L103S, U18-ch59
calib_packv5_040323_1717.root, FC#2, port C3
Entries 124
Mean 54.9
Std Dev 11.89
Turn on : 51.8016
Width : 4.282
Height : 10.225
Entry
ampl
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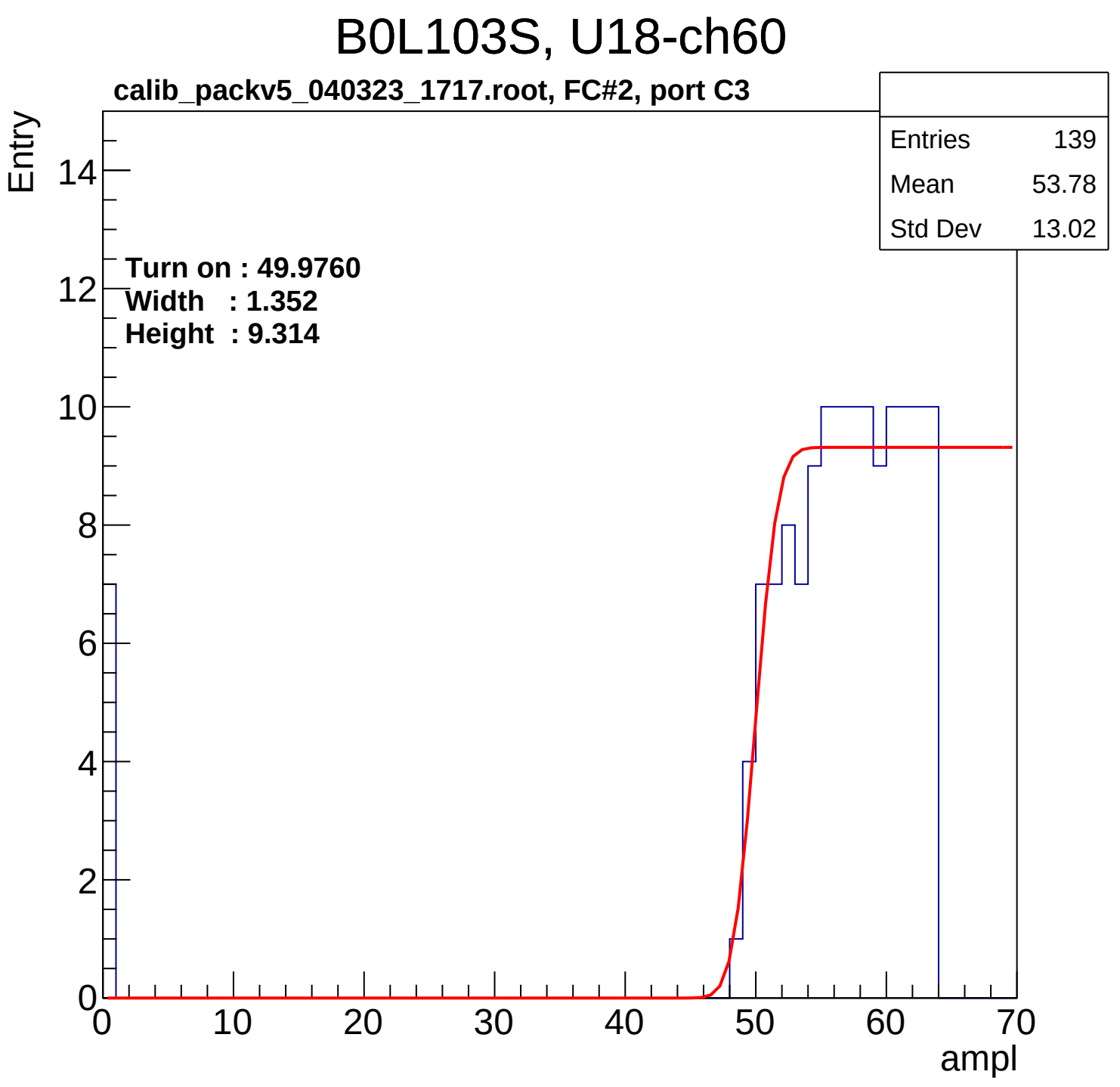
B0L103S, U18-ch60
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 53.78
Std Dev 13.02
Turn on : 49.9760
Width : 1.352
Height : 9.314
Entry
ampl
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4
6
8
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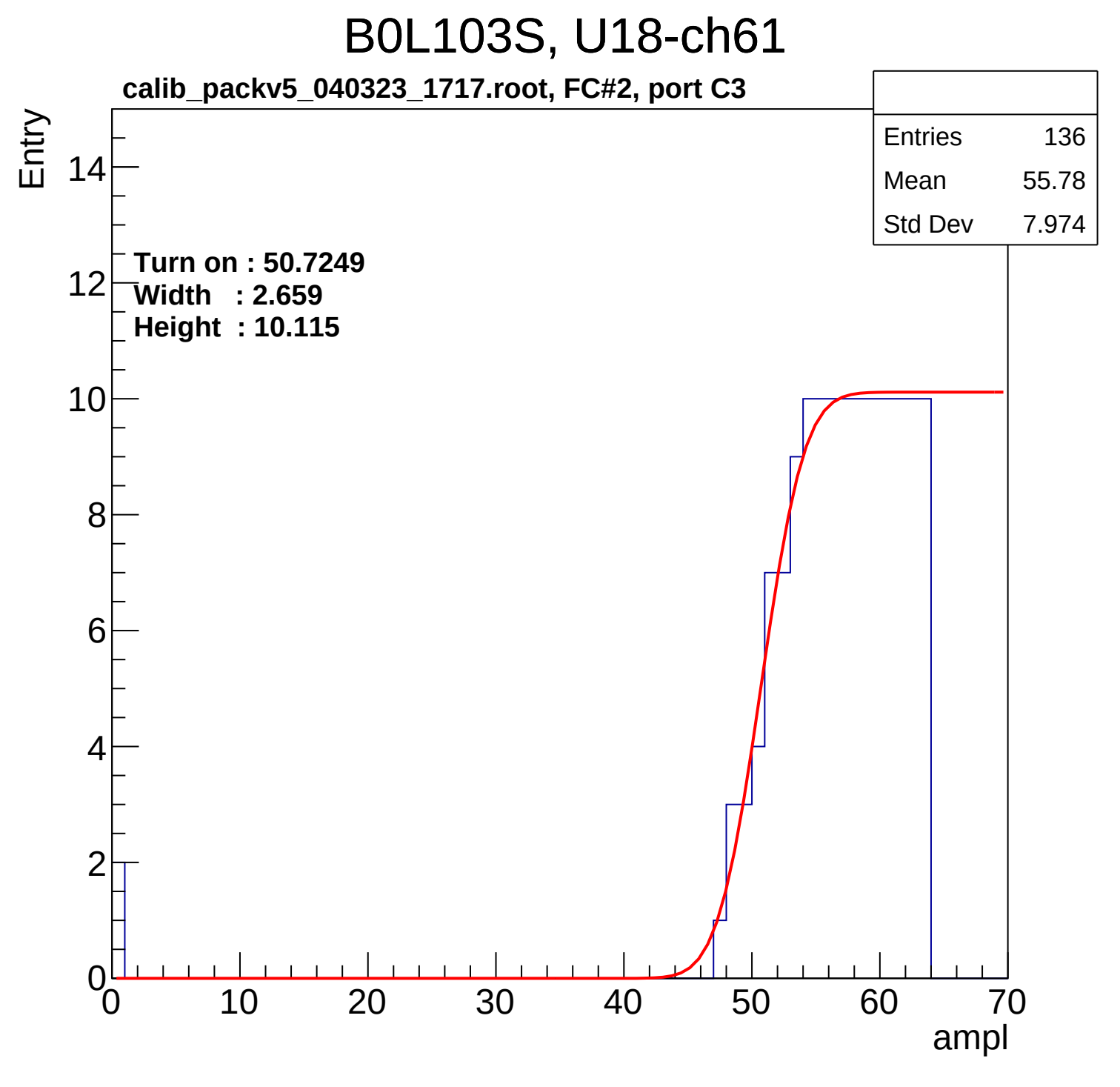
B0L103S, U18-ch61
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 55.78
Std Dev 7.974
Turn on : 50.7249
Width : 2.659
Height : 10.115
Entry
ampl
0
2
4
6
8
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12
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0
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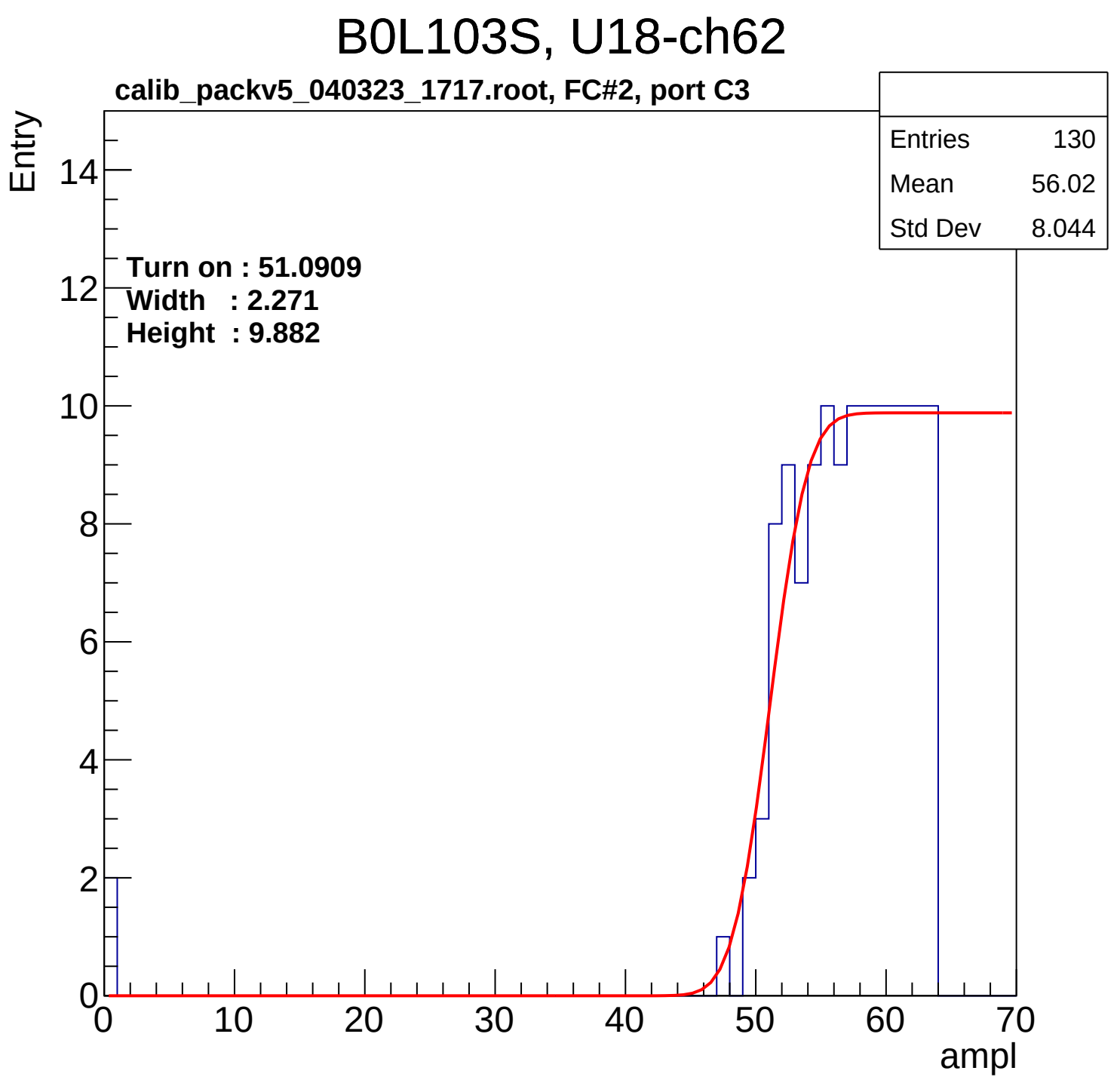
B0L103S, U18-ch62
calib_packv5_040323_1717.root, FC#2, port C3
Entries 130
Mean 56.02
Std Dev 8.044
Turn on : 51.0909
Width : 2.271
Height : 9.882
Entry
ampl
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2
4
6
8
10
12
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0
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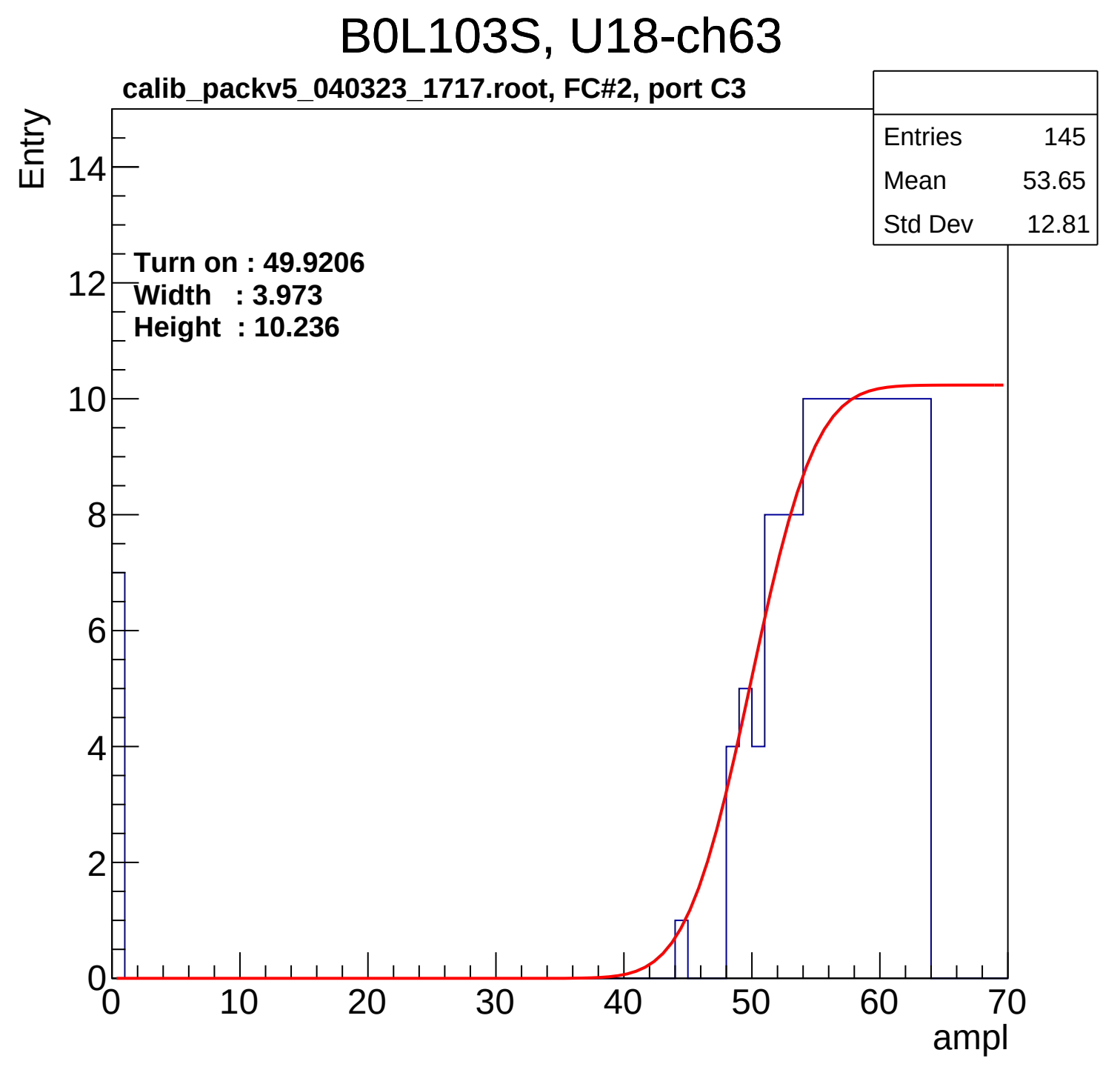
B0L103S, U18-ch63
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 53.65
Std Dev 12.81
Turn on : 49.9206
Width : 3.973
Height : 10.236
Entry
ampl
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2
4
6
8
10
12
14
0
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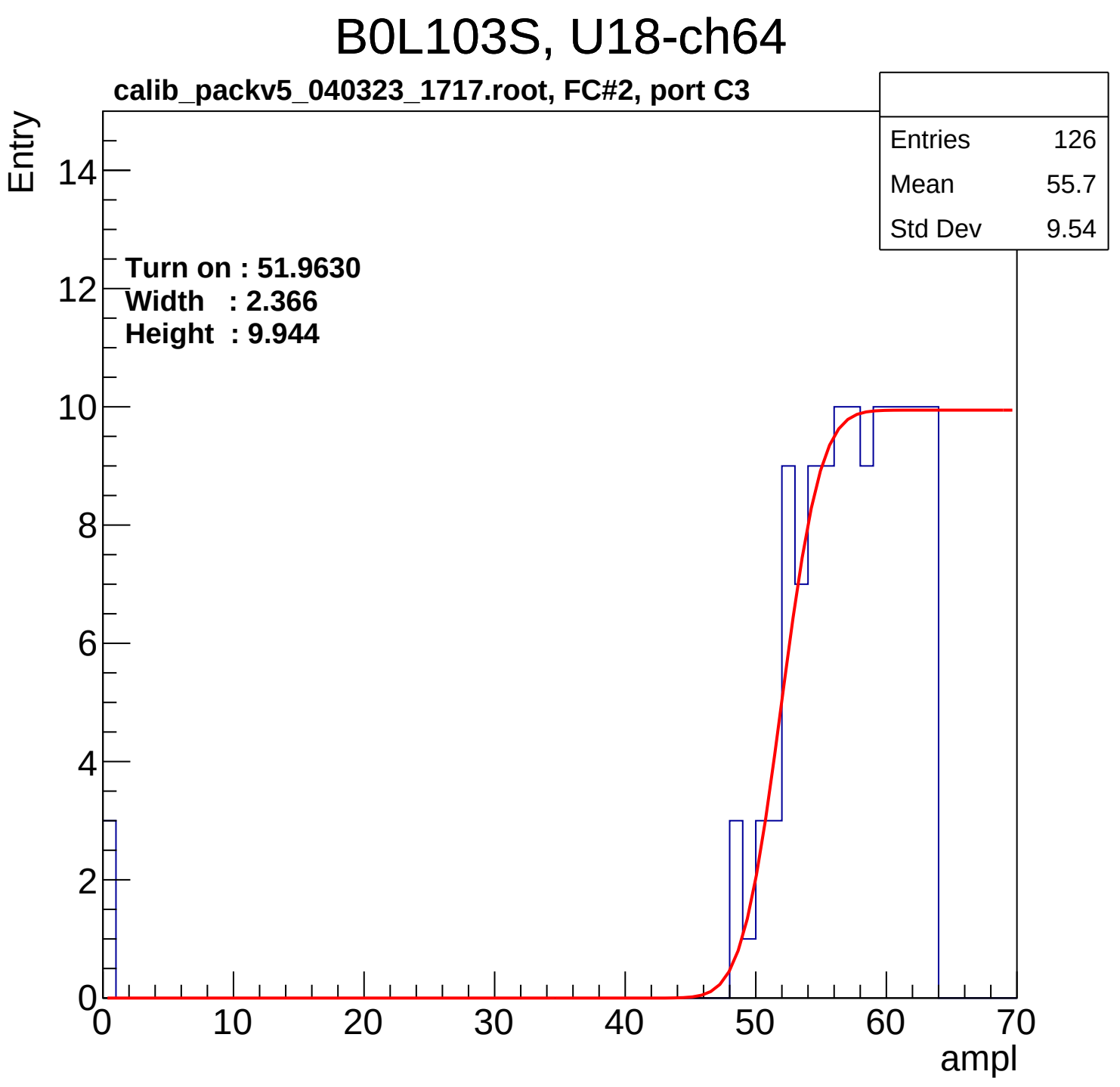
B0L103S, U18-ch64
calib_packv5_040323_1717.root, FC#2, port C3
Entries 126
Mean 55.7
Std Dev 9.54
Turn on : 51.9630
Width : 2.366
Height : 9.944
Entry
ampl
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2
4
6
8
10
12
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0
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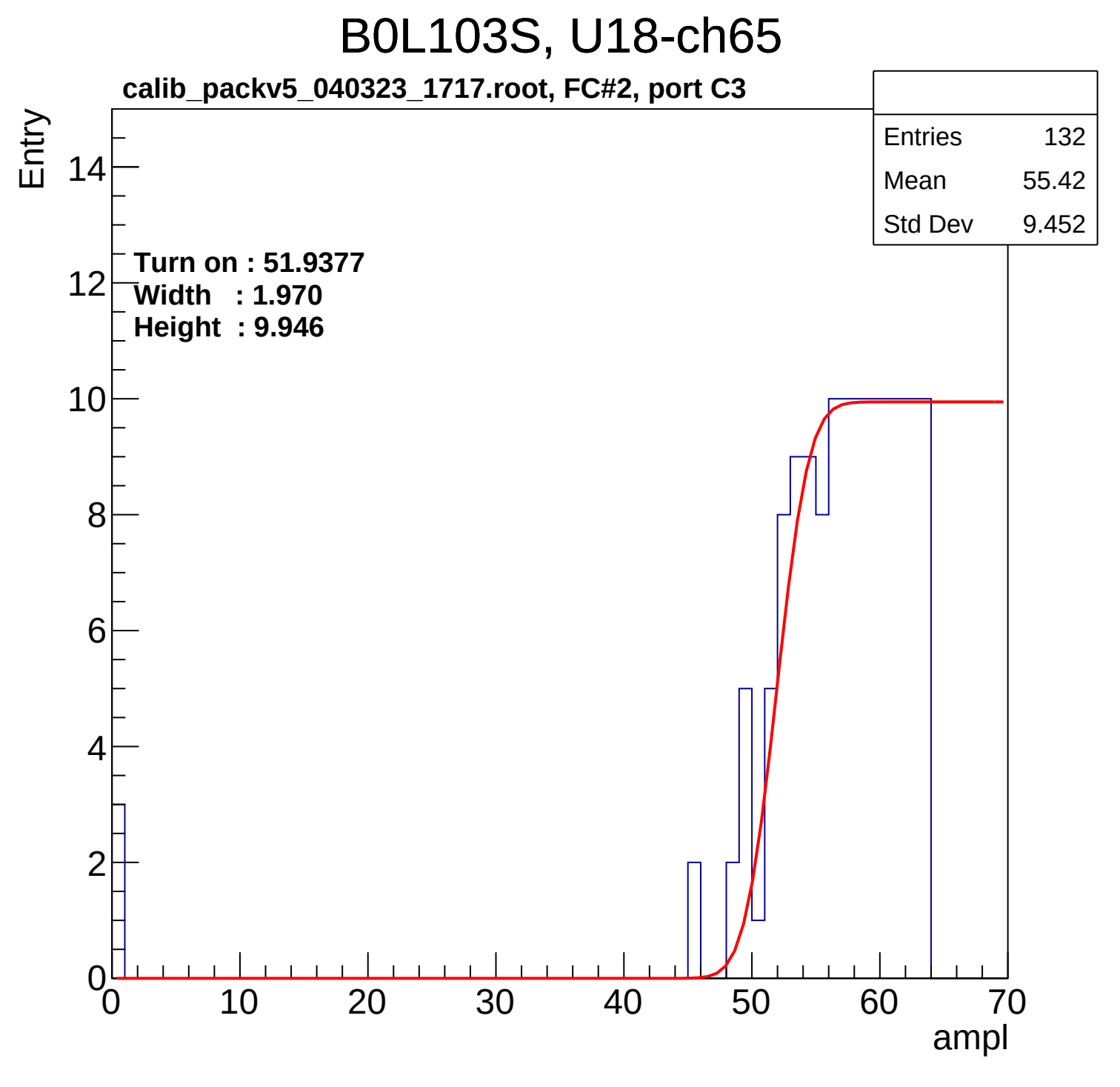
B0L103S, U18-ch65
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 55.42
Std Dev 9.452
Turn on : 51.9377
Width : 1.970
Height : 9.946
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
50
60
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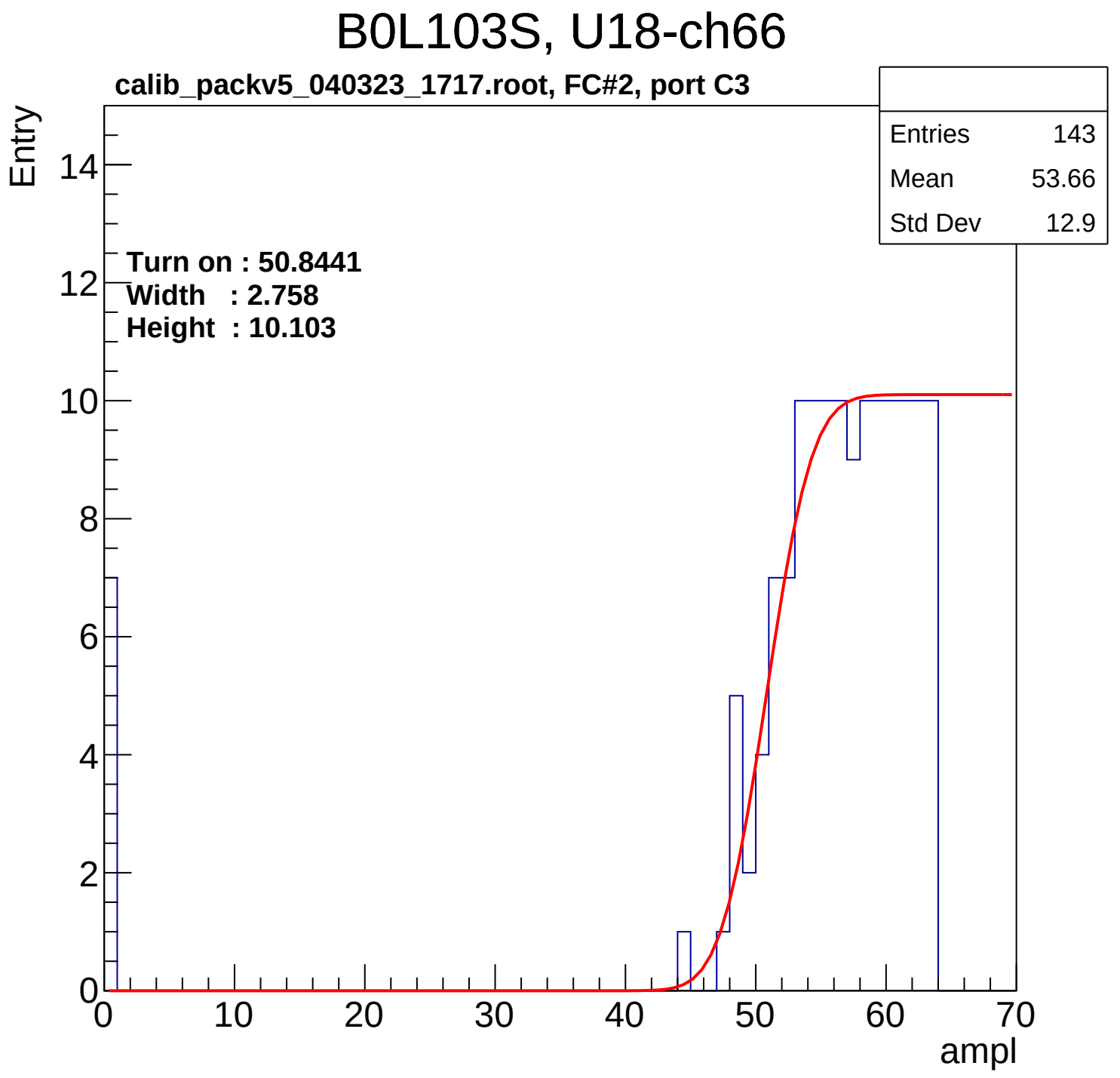
B0L103S, U18-ch66
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 53.66
Std Dev 12.9
Turn on : 50.8441
Width : 2.758
Height : 10.103
Entry
ampl
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2
4
6
8
10
12
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0
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60
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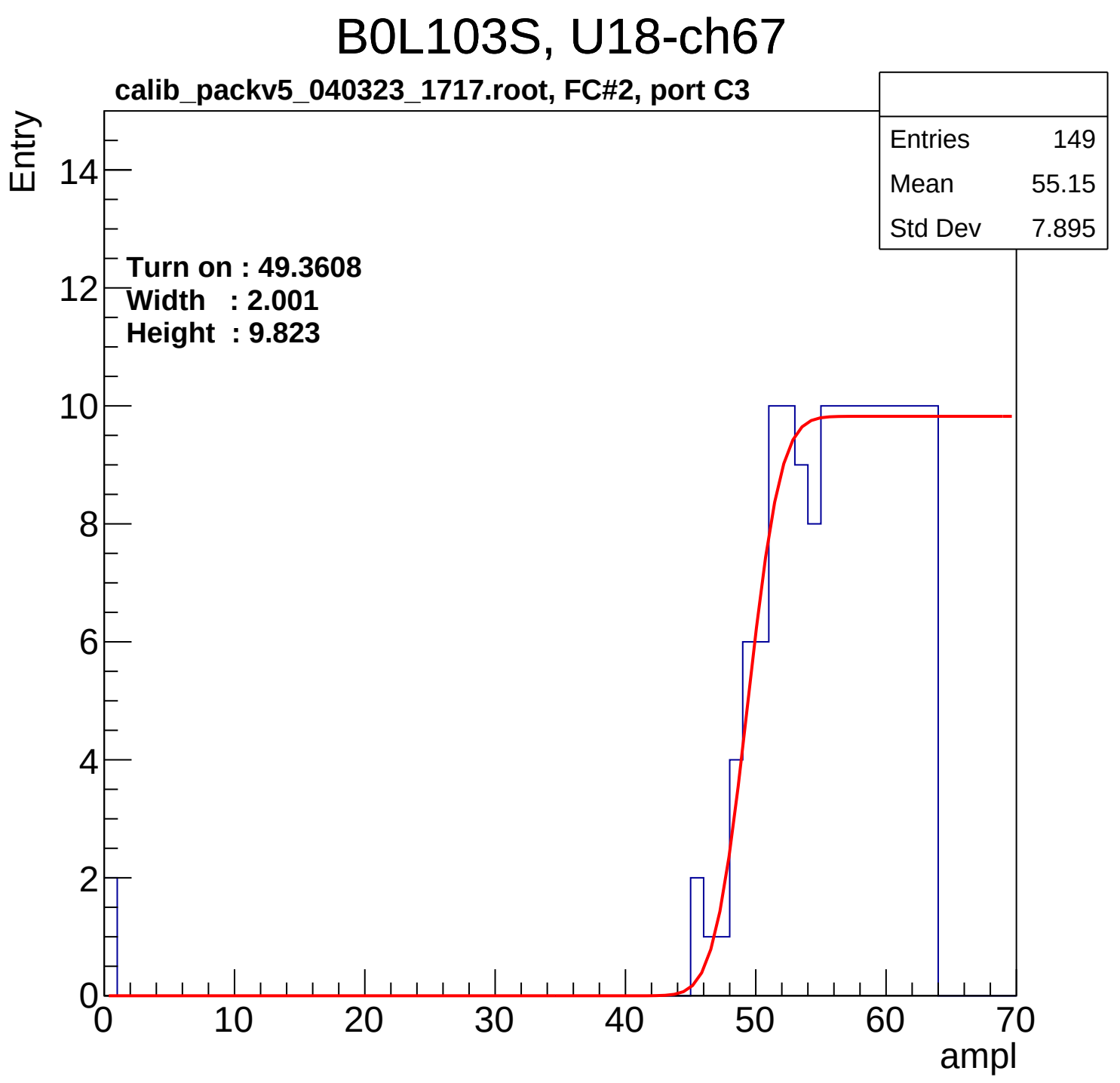
B0L103S, U18-ch67
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 55.15
Std Dev 7.895
Turn on : 49.3608
Width : 2.001
Height : 9.823
Entry
ampl
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2
4
6
8
10
12
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0
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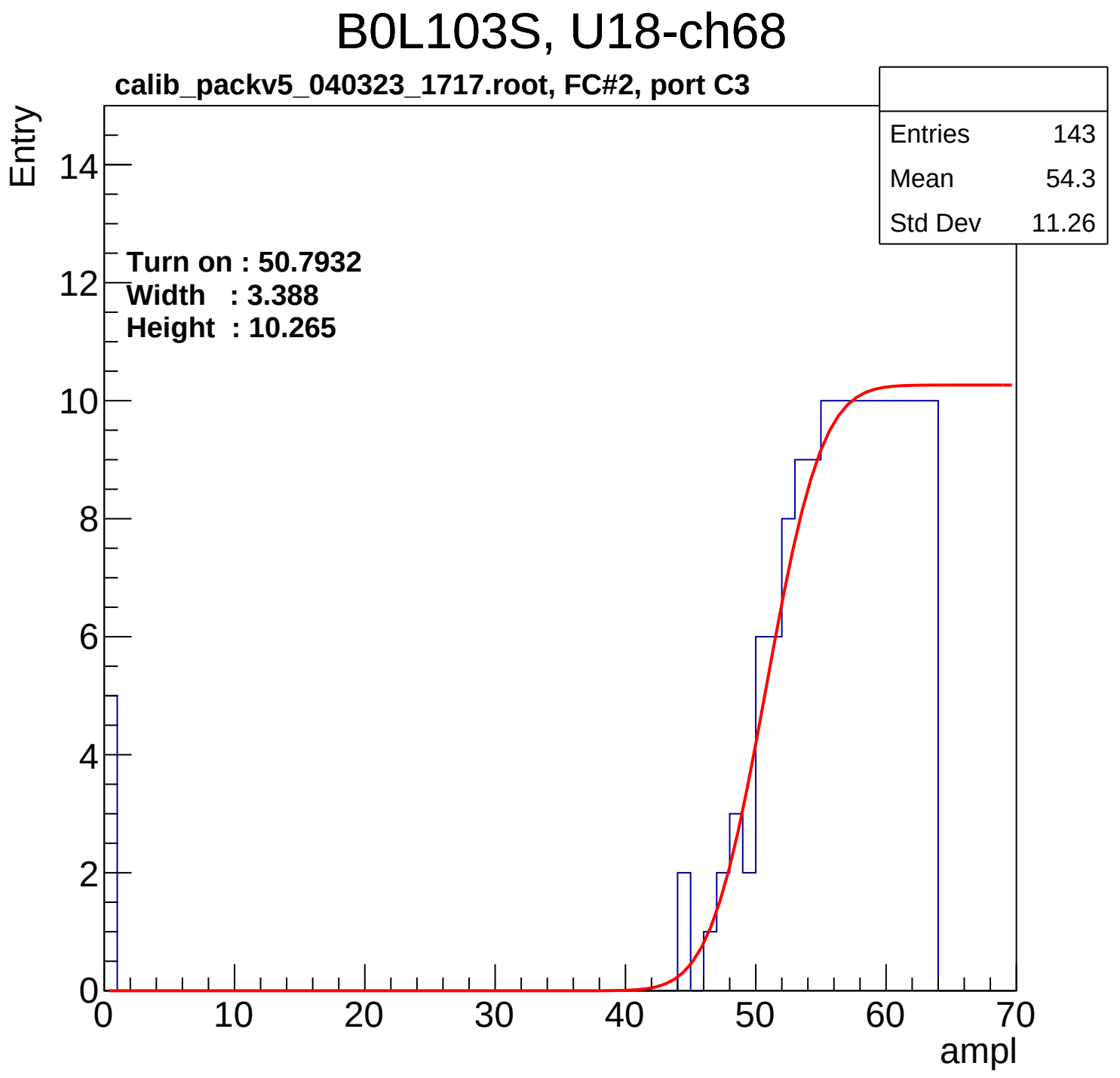
B0L103S, U18-ch68
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 54.3
Std Dev 11.26
Turn on : 50.7932
Width : 3.388
Height : 10.265
Entry
ampl
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4
6
8
10
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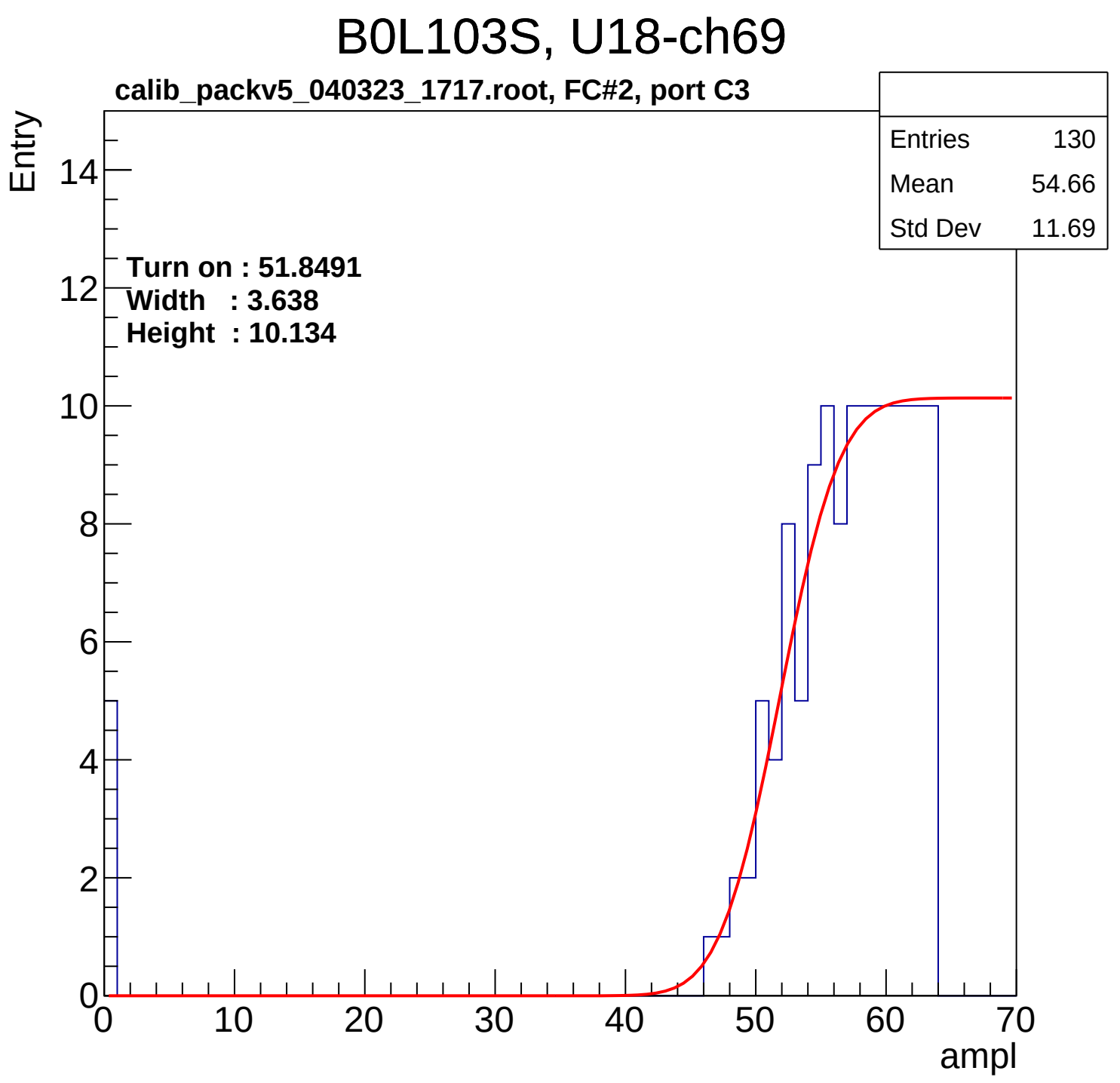
B0L103S, U18-ch69
calib_packv5_040323_1717.root, FC#2, port C3
Entries 130
Mean 54.66
Std Dev 11.69
Turn on : 51.8491
Width : 3.638
Height : 10.134
Entry
ampl
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4
6
8
10
12
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0
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20
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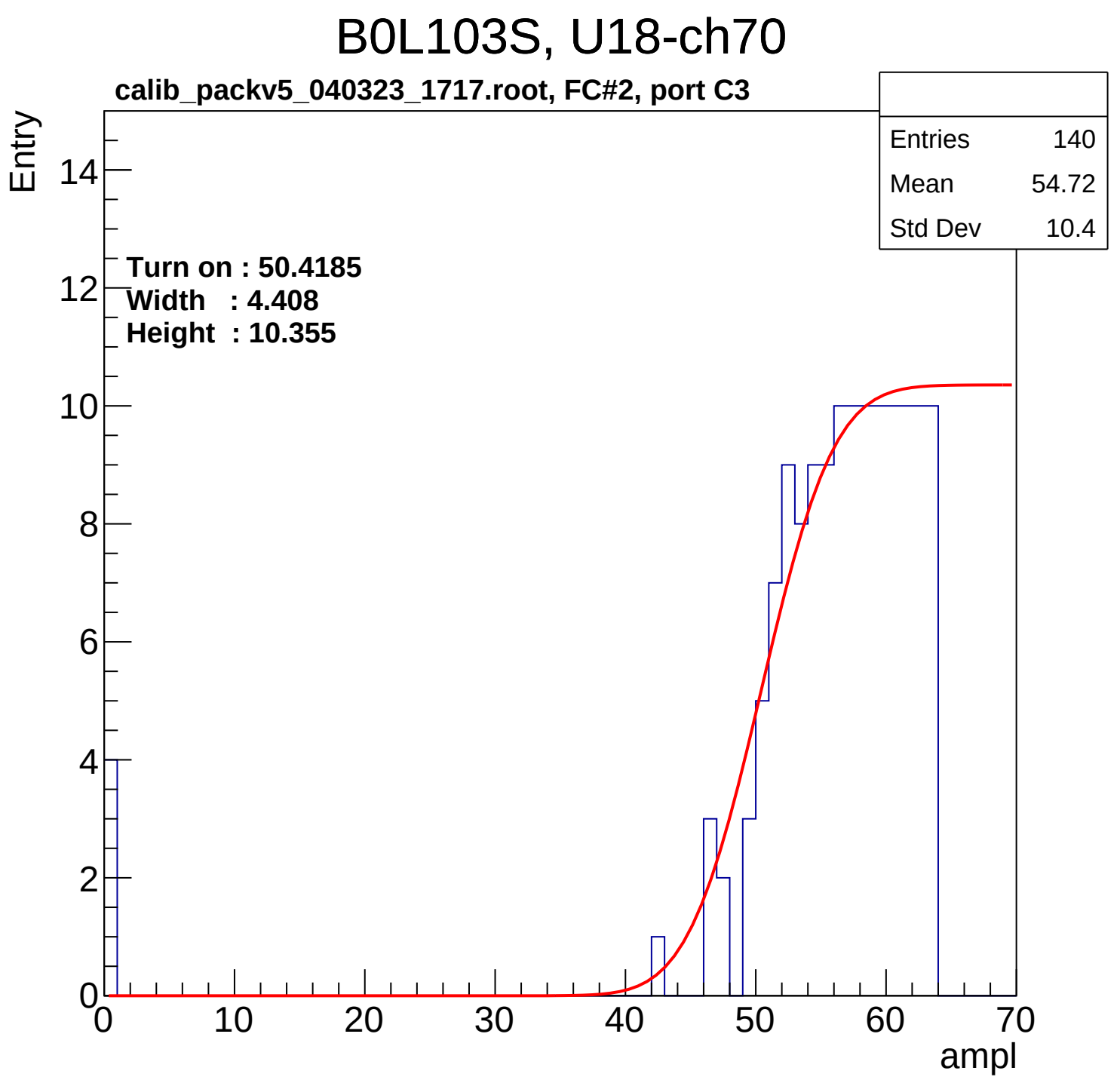
B0L103S, U18-ch70
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 54.72
Std Dev 10.4
Turn on : 50.4185
Width : 4.408
Height : 10.355
Entry
ampl
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6
8
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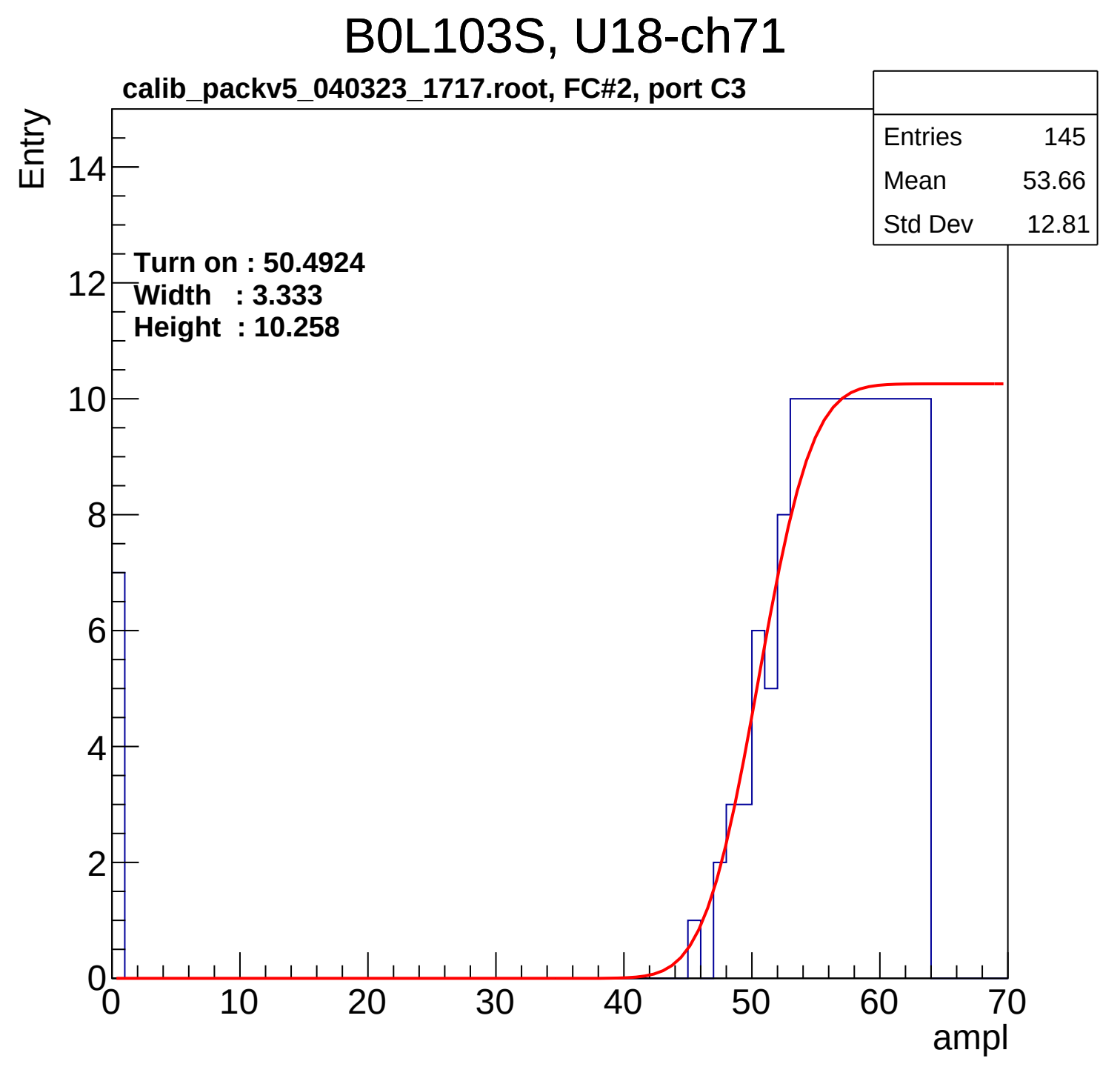
B0L103S, U18-ch71
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 53.66
Std Dev 12.81
Turn on : 50.4924
Width : 3.333
Height : 10.258
Entry
ampl
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4
6
8
10
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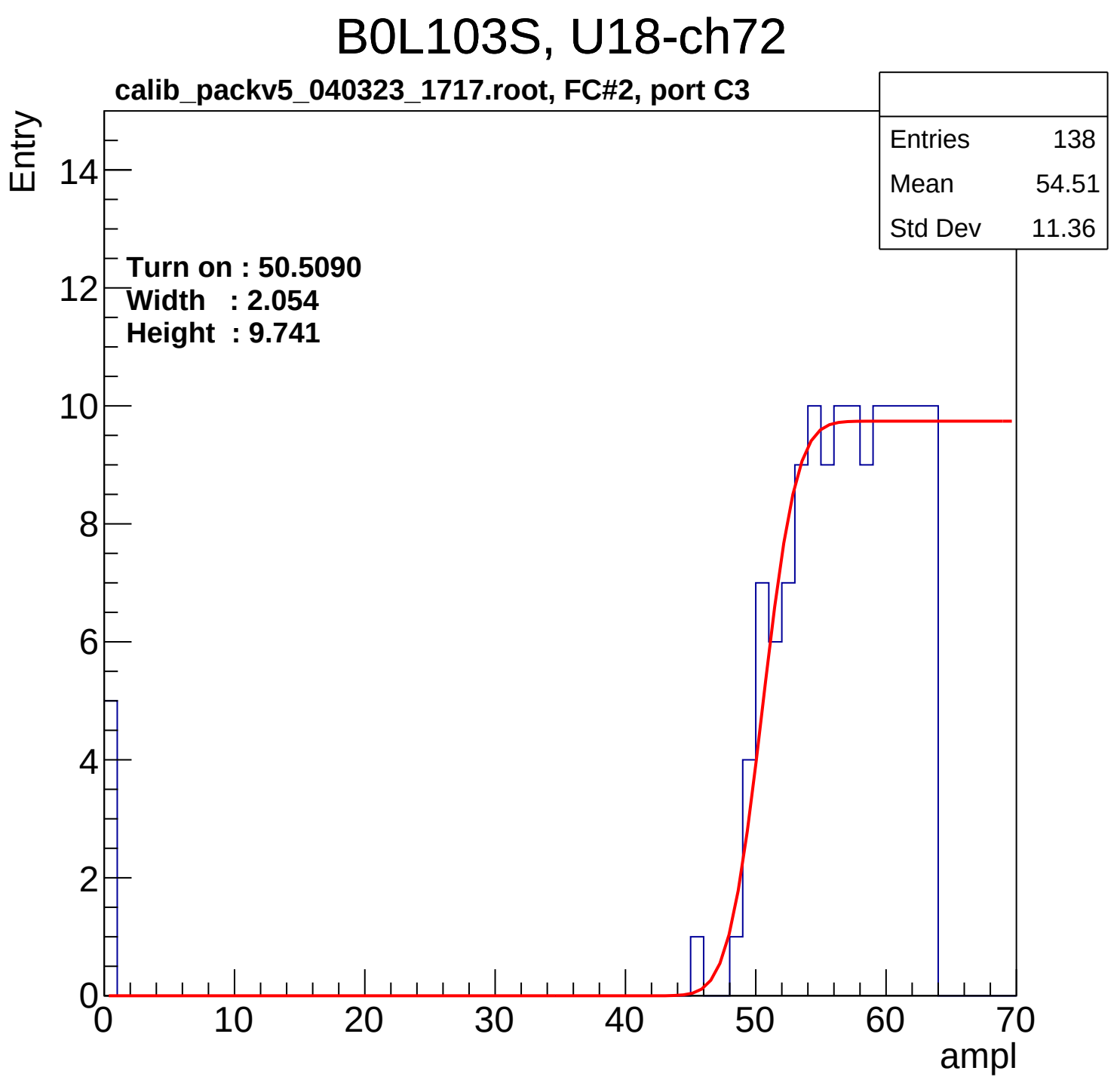
B0L103S, U18-ch72
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 54.51
Std Dev 11.36
Turn on : 50.5090
Width : 2.054
Height : 9.741
Entry
ampl
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6
8
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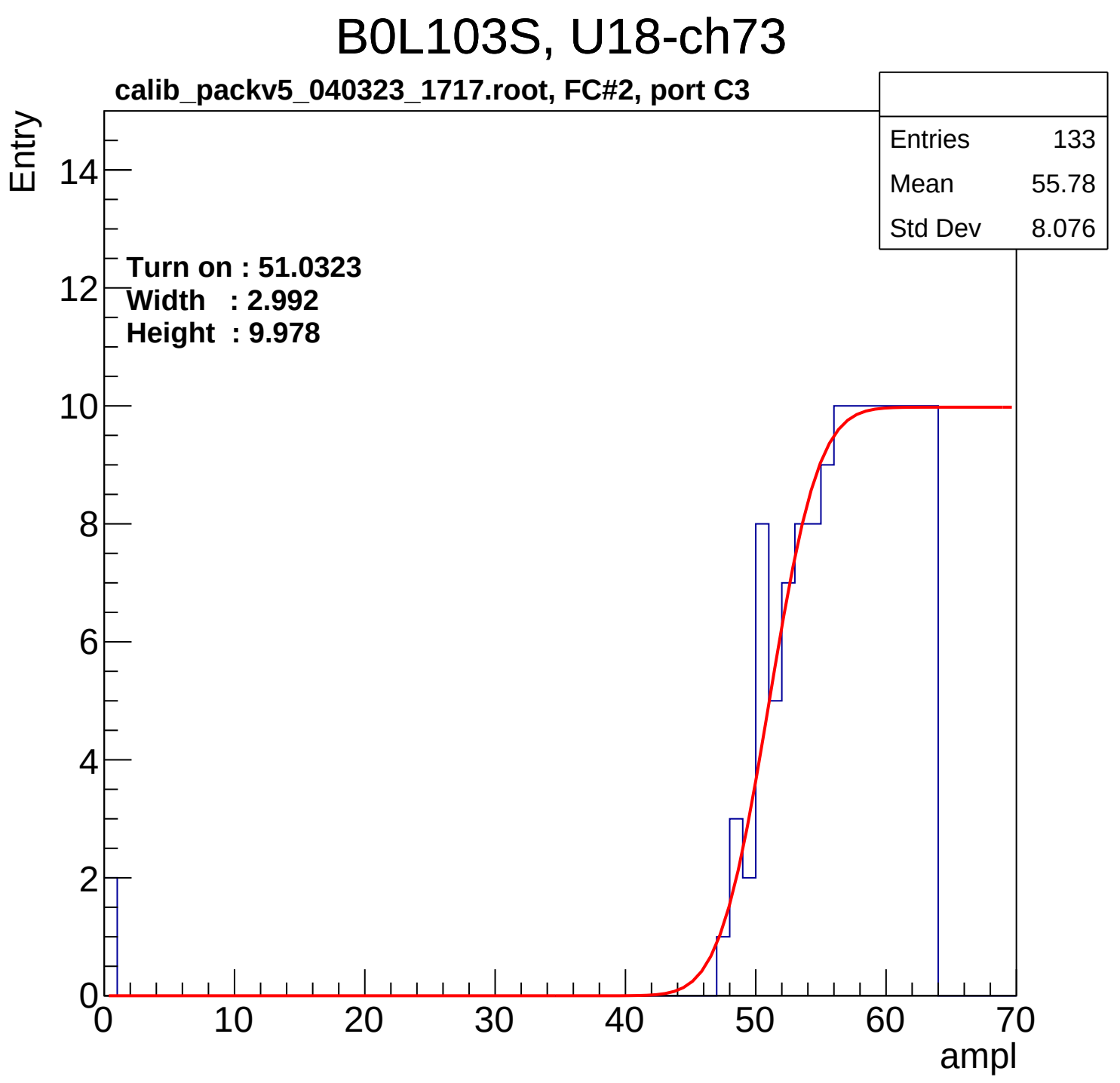
B0L103S, U18-ch73
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 55.78
Std Dev 8.076
Turn on : 51.0323
Width : 2.992
Height : 9.978
Entry
ampl
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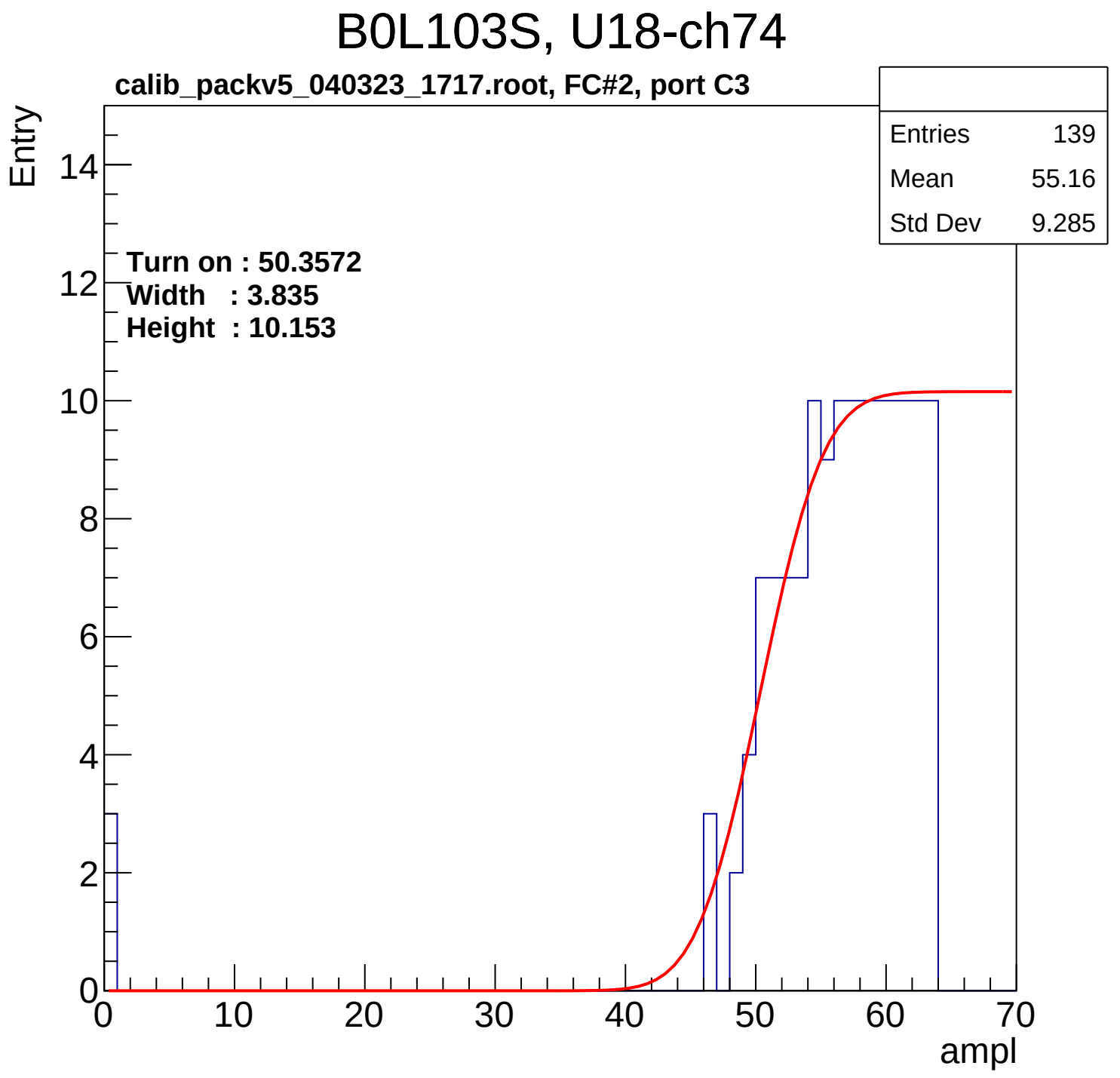
B0L103S, U18-ch74
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 55.16
Std Dev 9.285
Turn on : 50.3572
Width : 3.835
Height : 10.153
Entry
ampl
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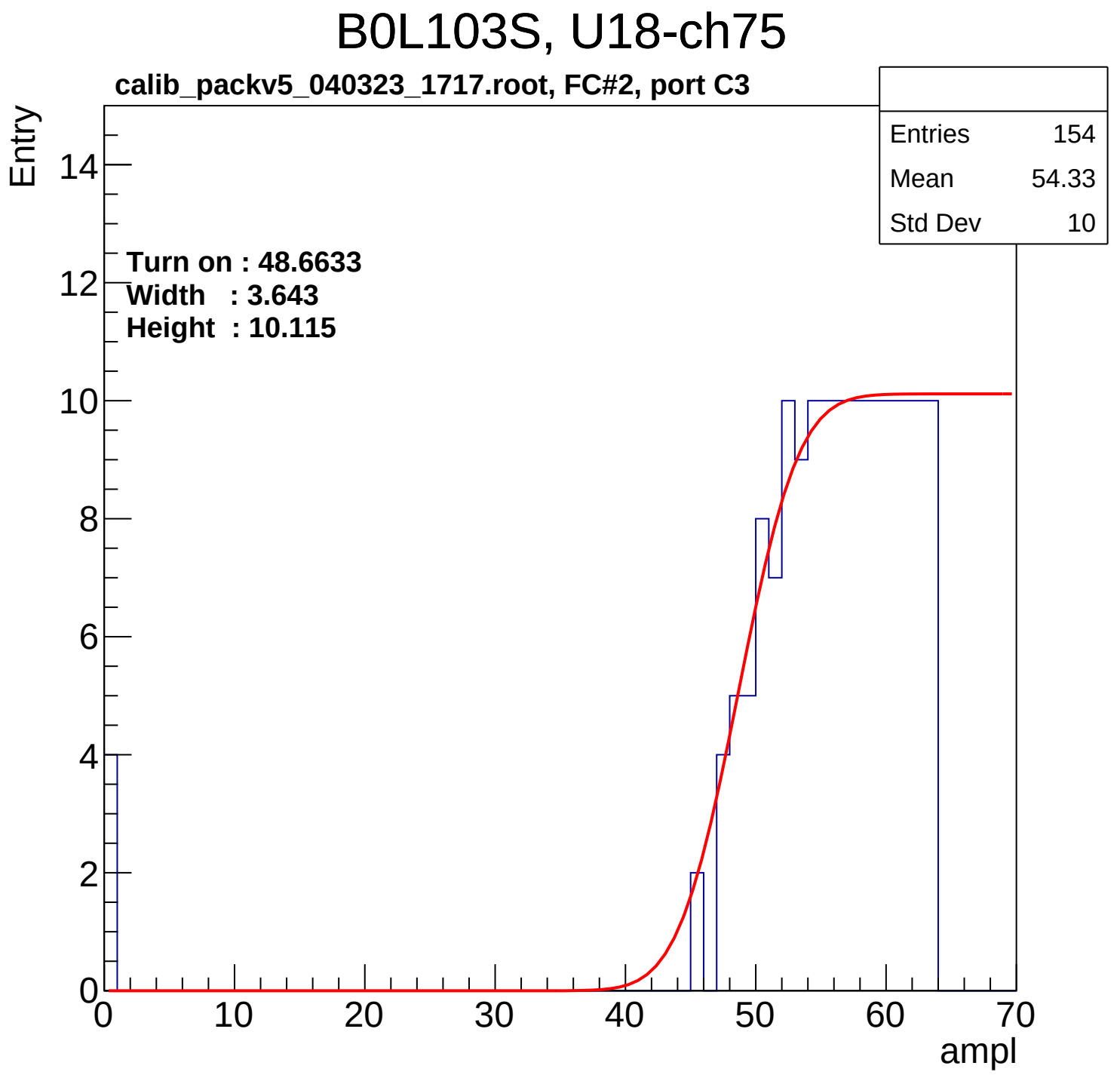
B0L103S, U18-ch75
calib_packv5_040323_1717.root, FC#2, port C3
Entries 154
Mean 54.33
Std Dev 10
Turn on : 48.6633
Width : 3.643
Height : 10.115
Entry
ampl
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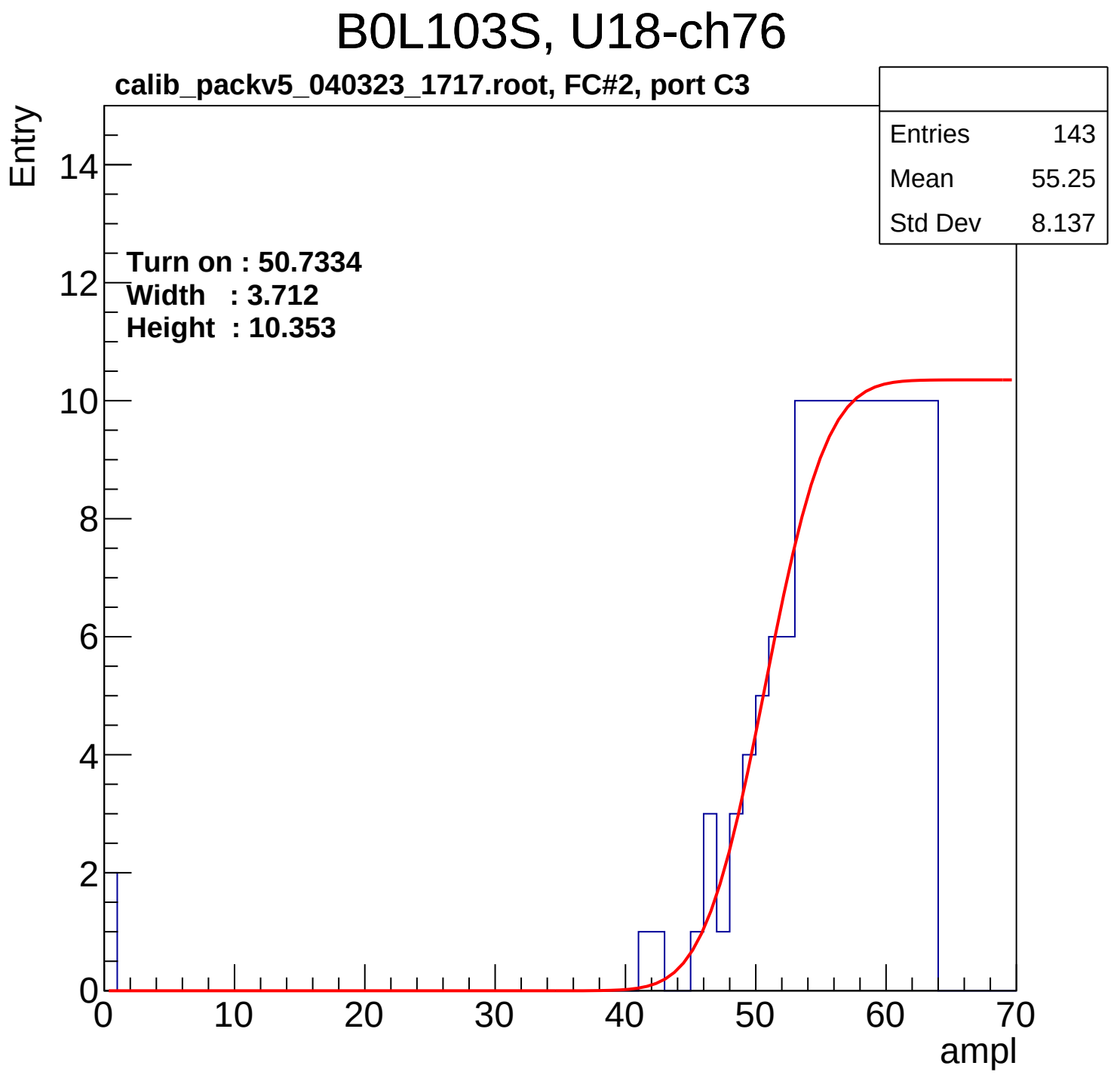
B0L103S, U18-ch76
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 55.25
Std Dev 8.137
Turn on : 50.7334
Width : 3.712
Height : 10.353
Entry
ampl
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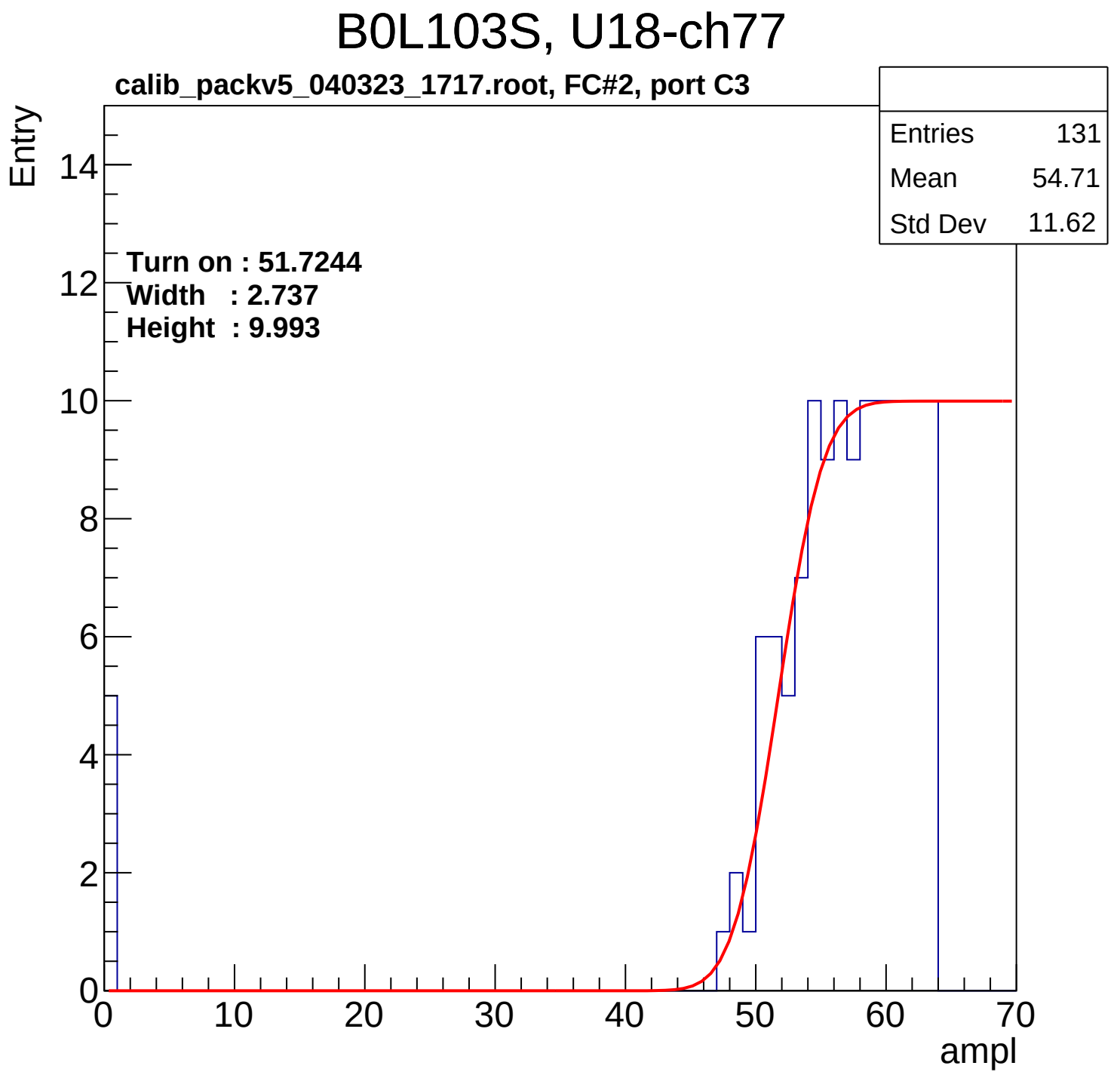
B0L103S, U18-ch77
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 54.71
Std Dev 11.62
Turn on : 51.7244
Width : 2.737
Height : 9.993
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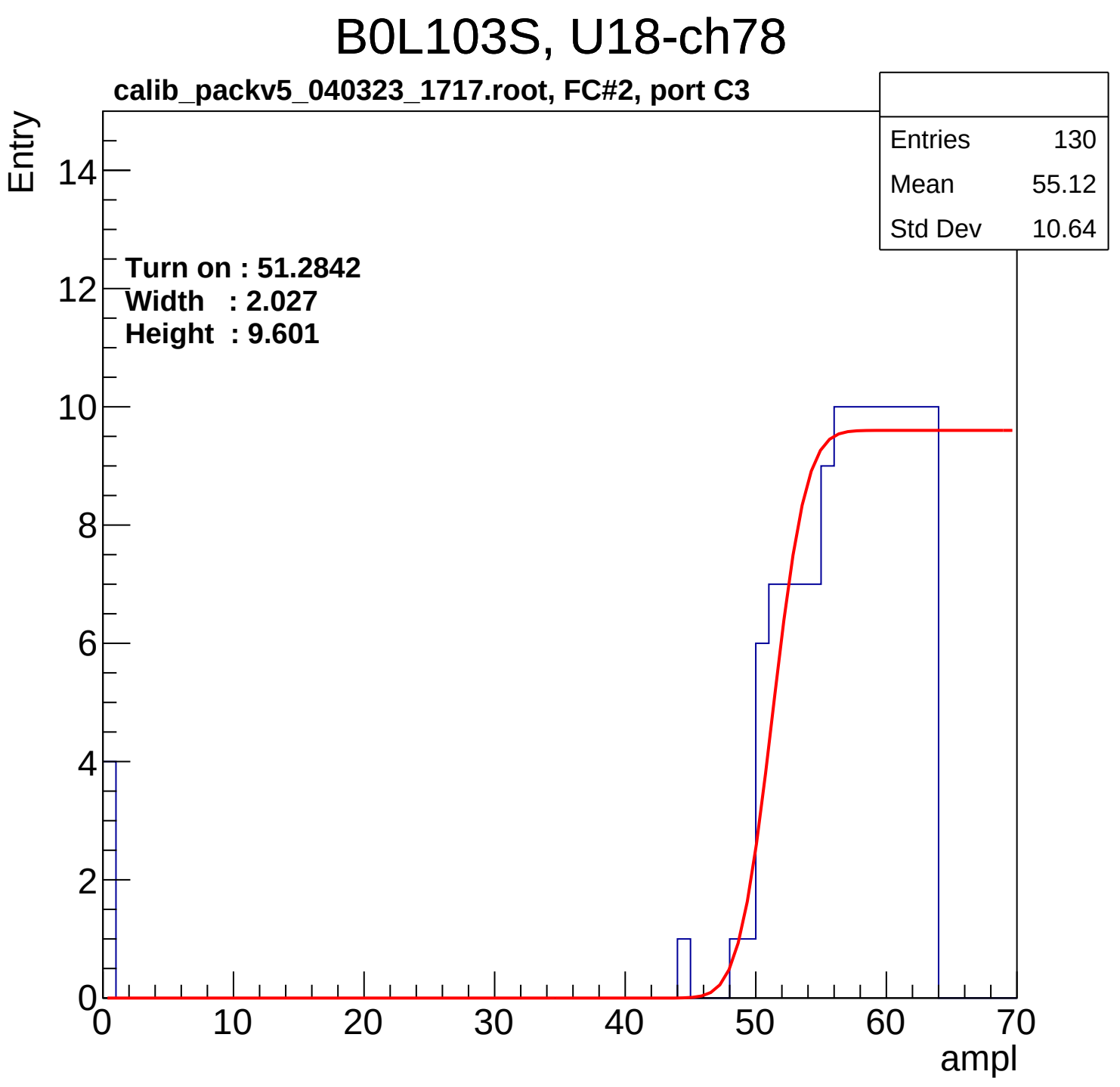
B0L103S, U18-ch78
calib_packv5_040323_1717.root, FC#2, port C3
Entries 130
Mean 55.12
Std Dev 10.64
Turn on : 51.2842
Width : 2.027
Height : 9.601
Entry
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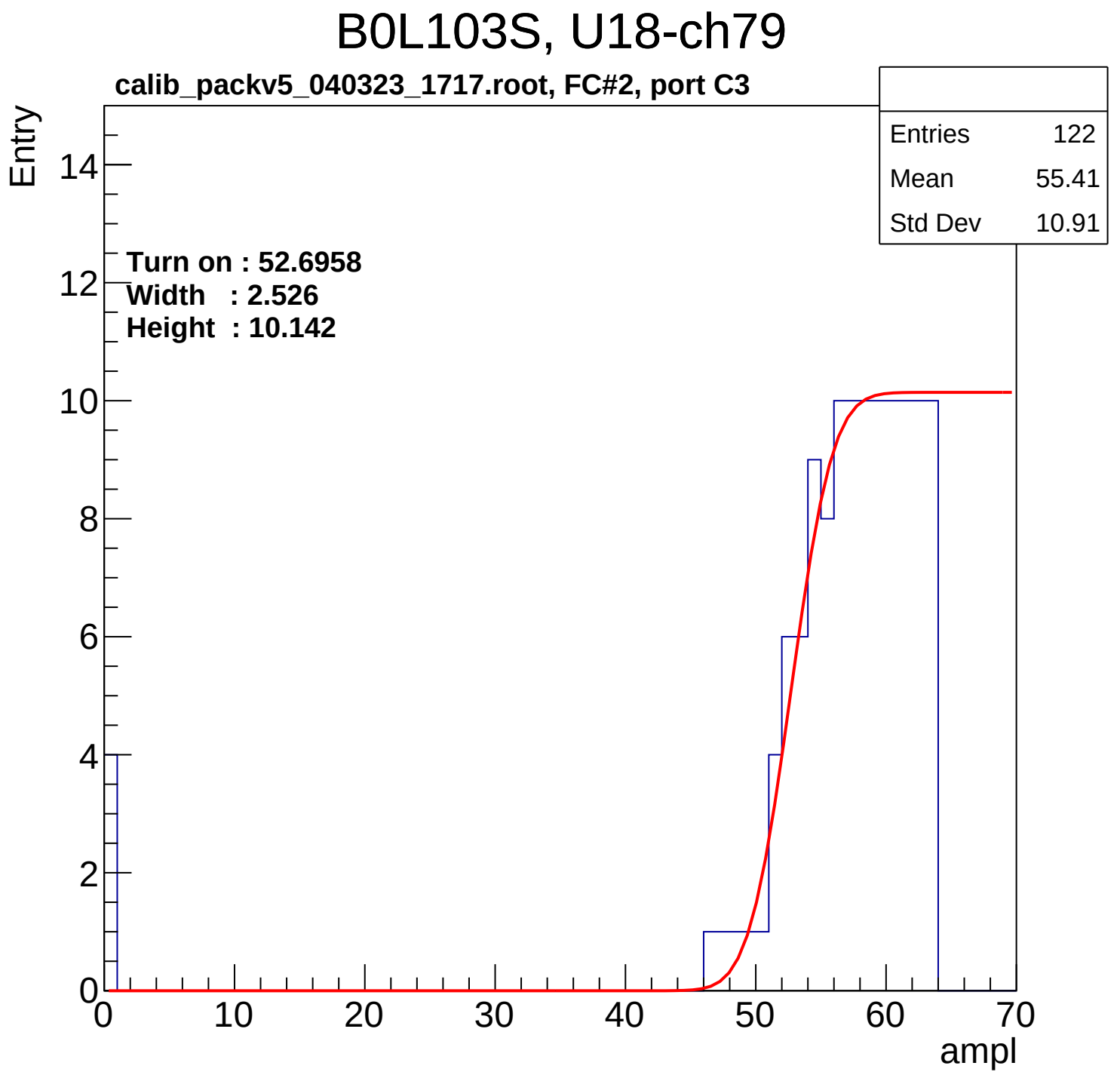
B0L103S, U18-ch79
calib_packv5_040323_1717.root, FC#2, port C3
Entries 122
Mean 55.41
Std Dev 10.91
Turn on : 52.6958
Width : 2.526
Height : 10.142
Entry
ampl
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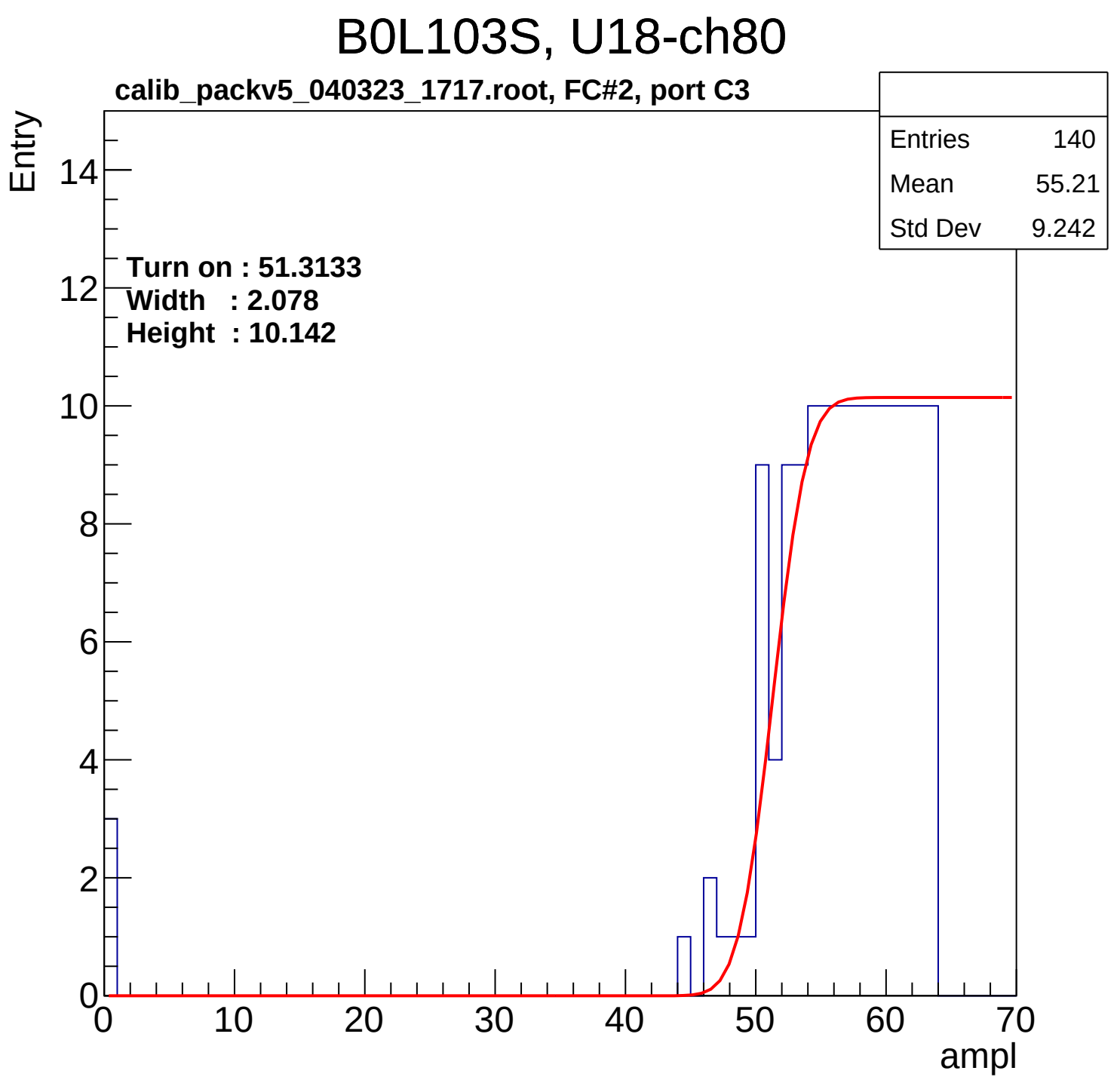
B0L103S, U18-ch80
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 55.21
Std Dev 9.242
Turn on : 51.3133
Width : 2.078
Height : 10.142
Entry
ampl
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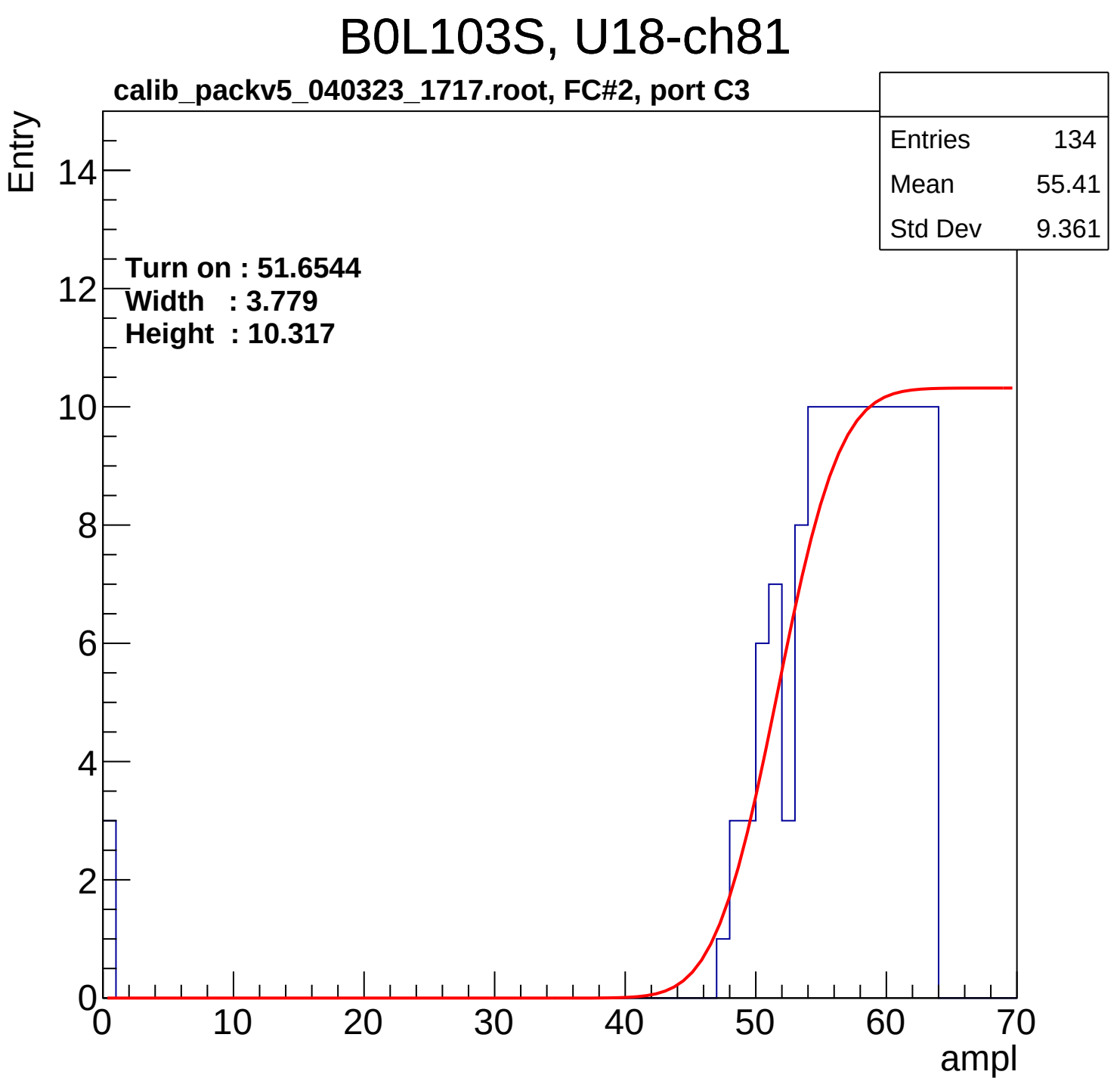
B0L103S, U18-ch81
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 55.41
Std Dev 9.361
Turn on : 51.6544
Width : 3.779
Height : 10.317
Entry
ampl
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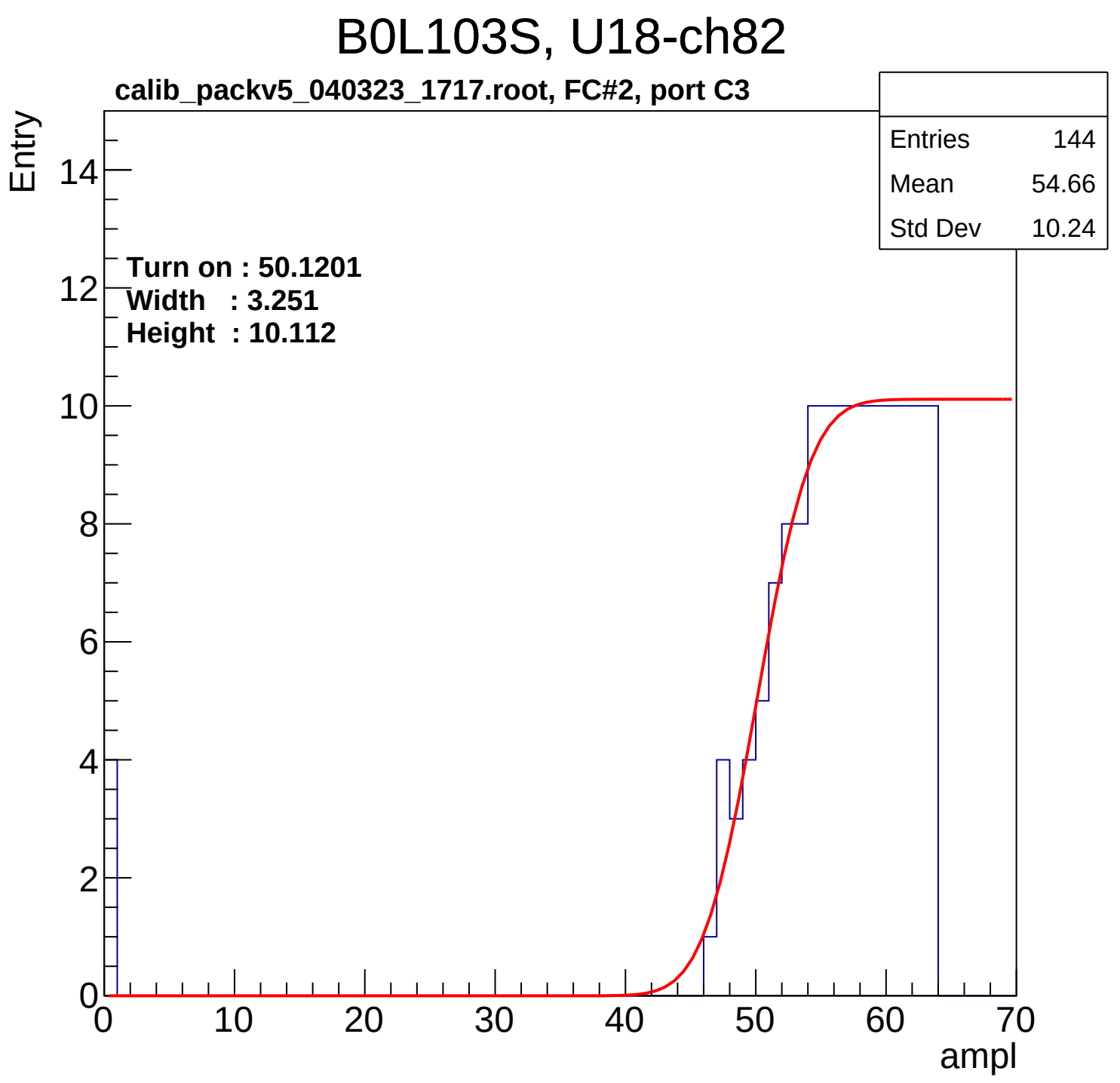
B0L103S, U18-ch82
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 54.66
Std Dev 10.24
Turn on : 50.1201
Width : 3.251
Height : 10.112
Entry
ampl
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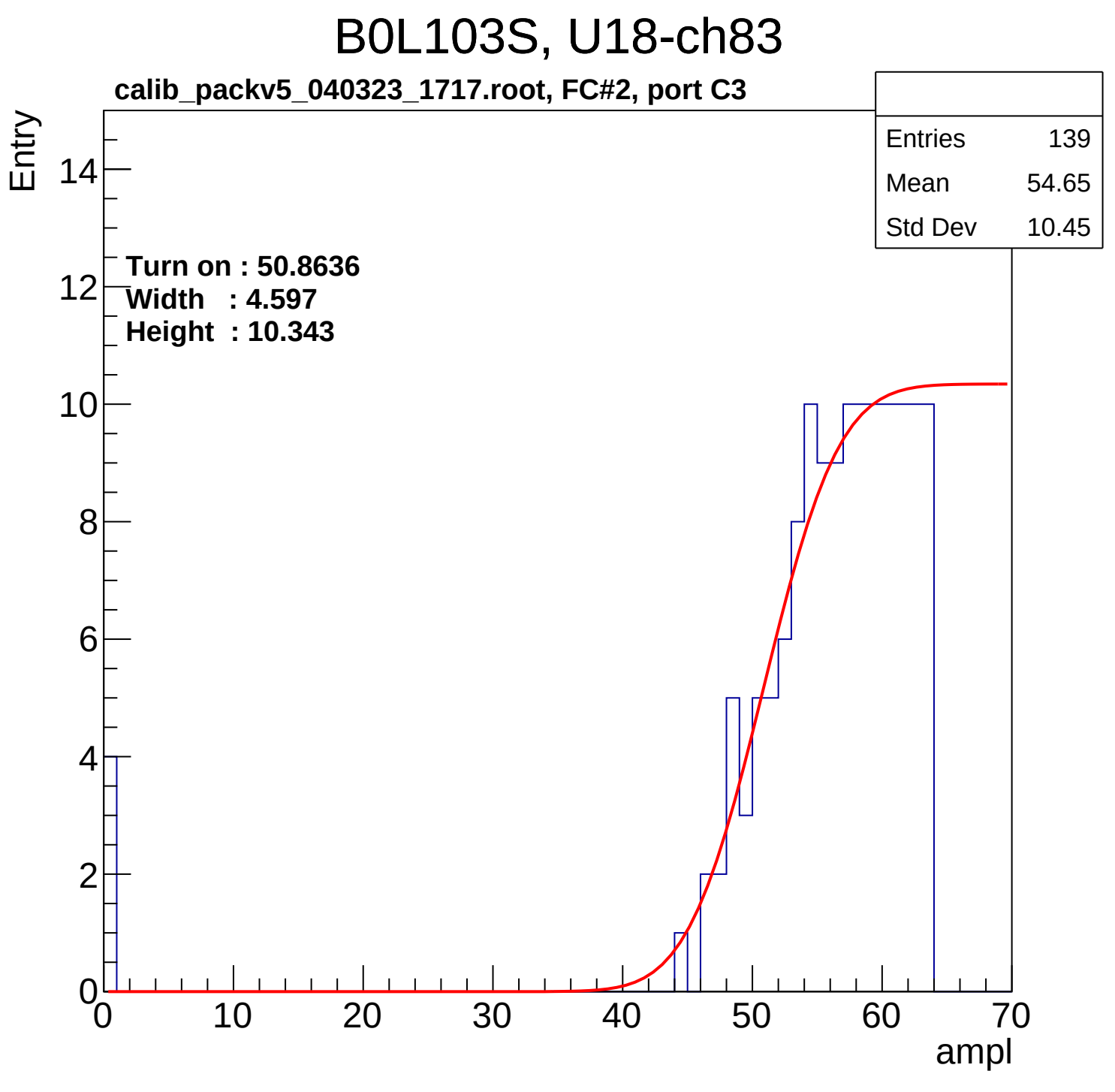
B0L103S, U18-ch83
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 54.65
Std Dev 10.45
Turn on : 50.8636
Width : 4.597
Height : 10.343
Entry
ampl
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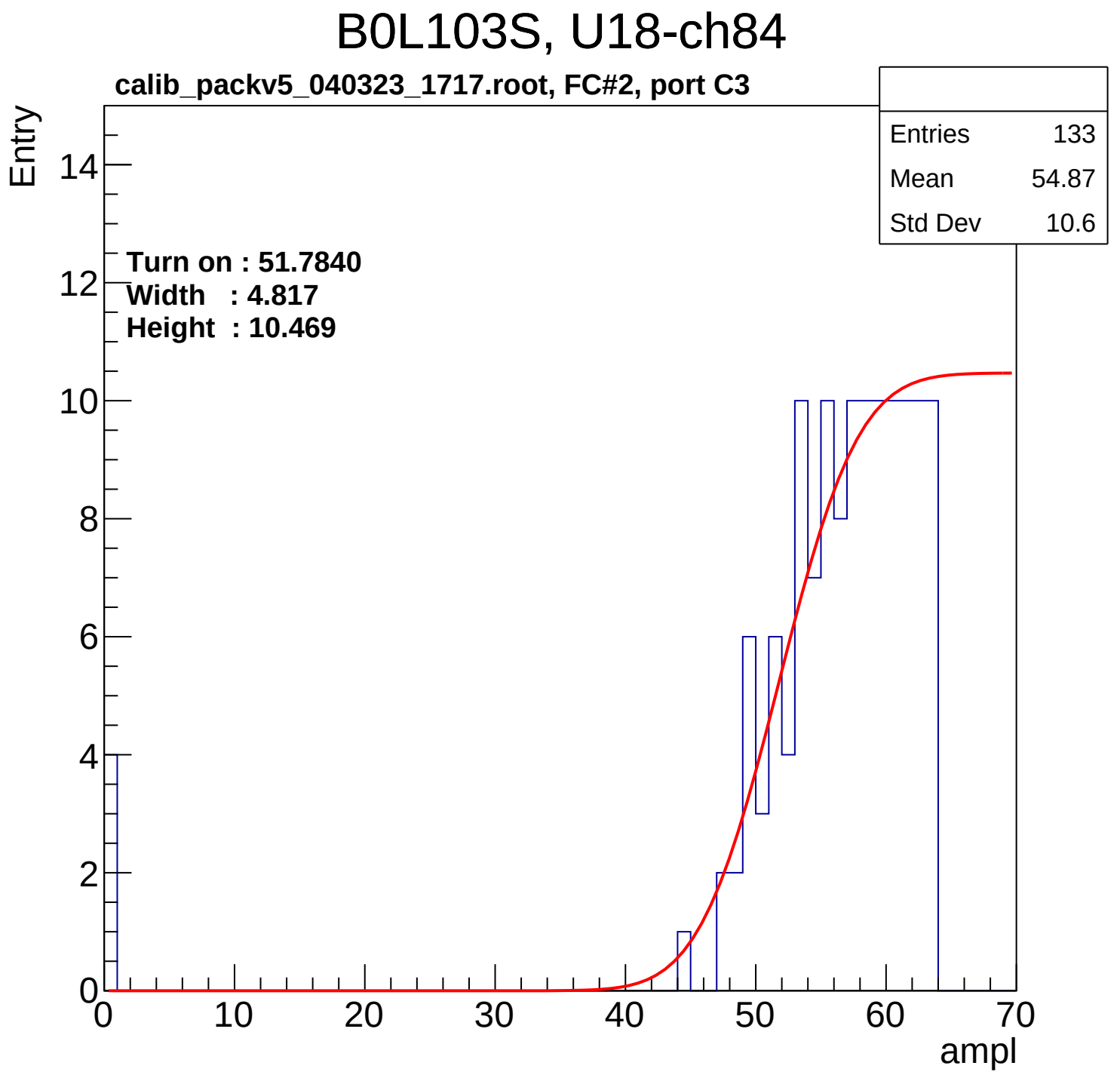
B0L103S, U18-ch84
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 54.87
Std Dev 10.6
Turn on : 51.7840
Width : 4.817
Height : 10.469
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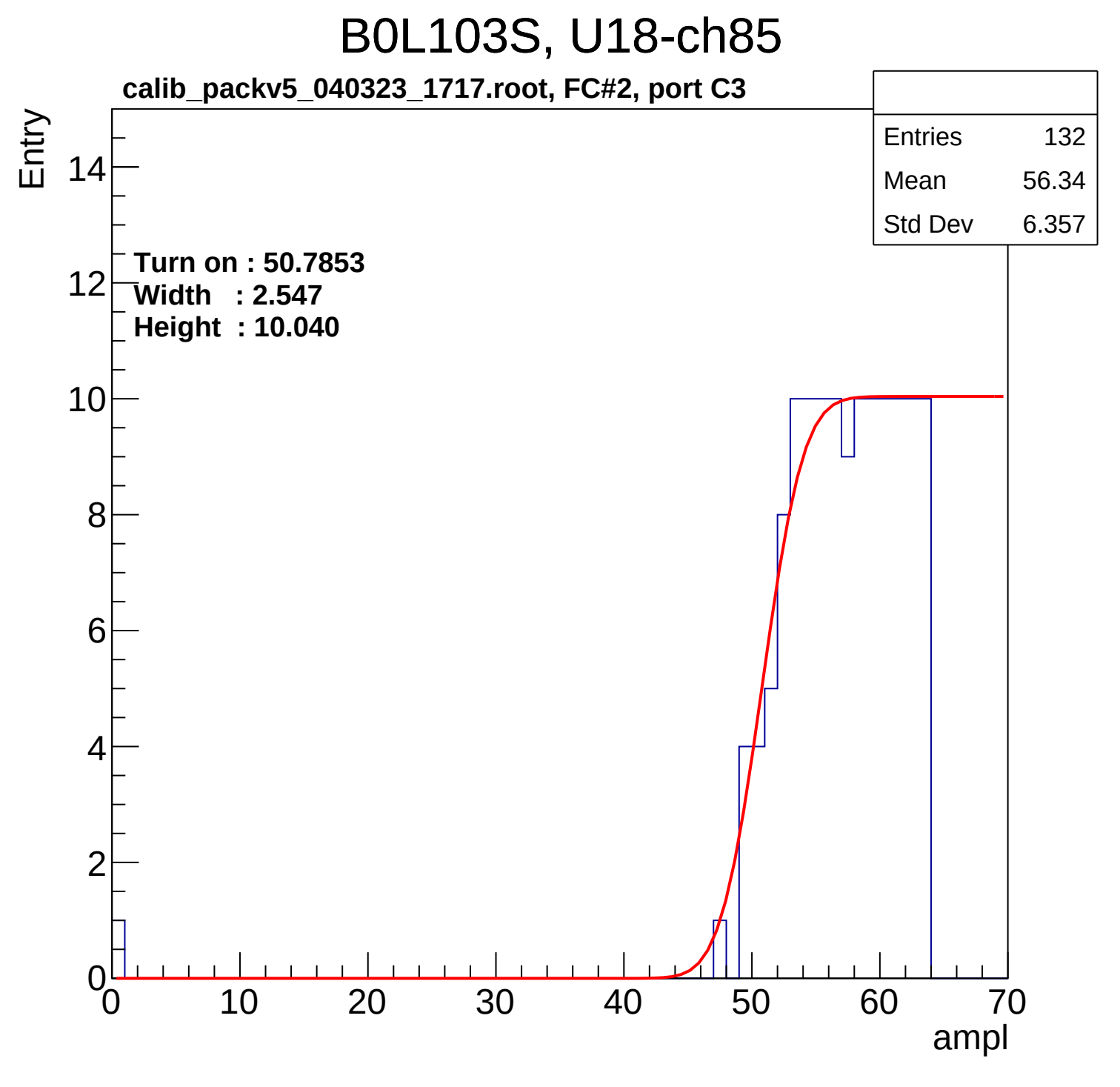
B0L103S, U18-ch85
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 56.34
Std Dev 6.357
Turn on : 50.7853
Width : 2.547
Height : 10.040
Entry
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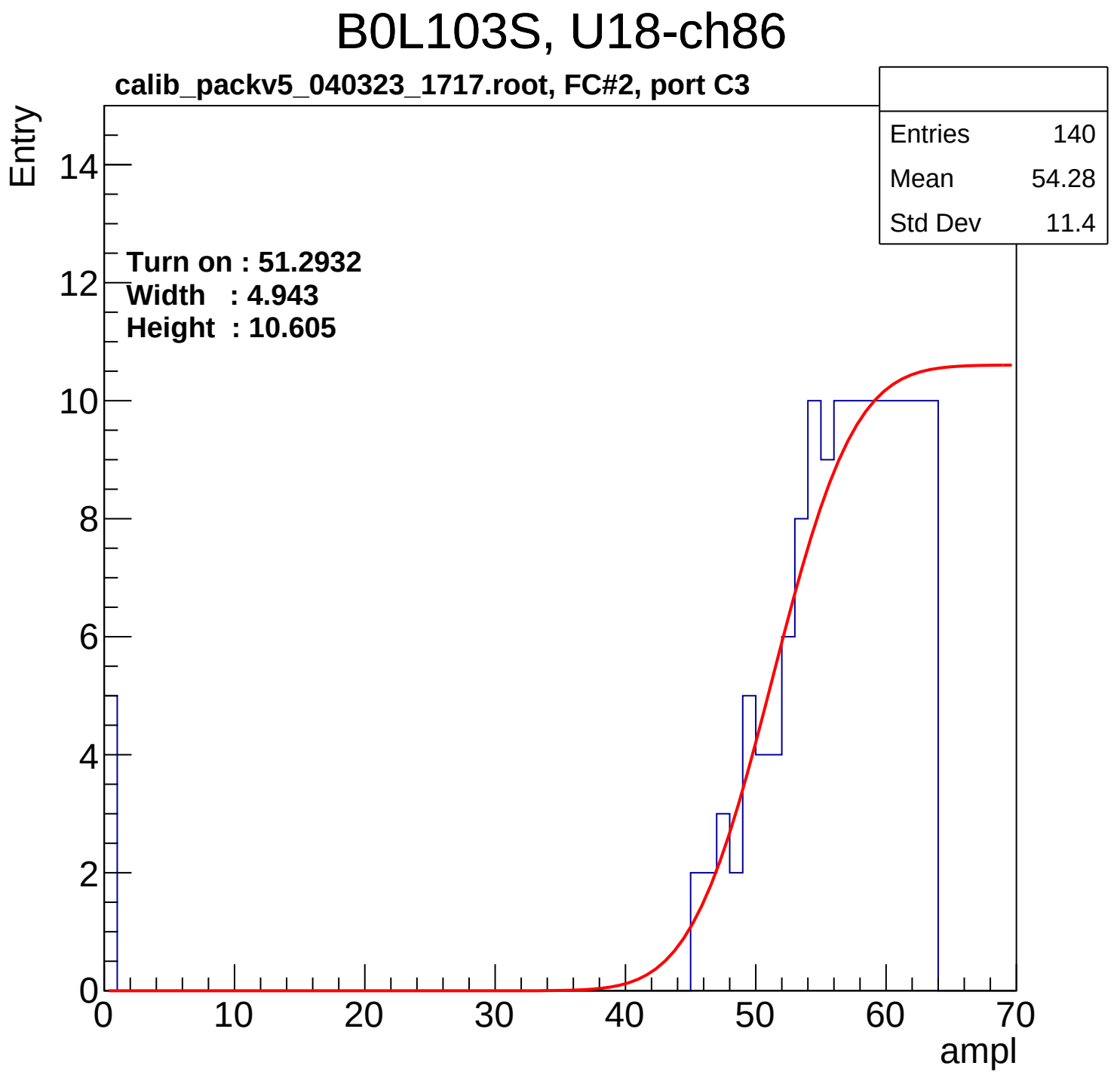
B0L103S, U18-ch86
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 54.28
Std Dev 11.4
Turn on : 51.2932
Width : 4.943
Height : 10.605
Entry
ampl
0
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4
6
8
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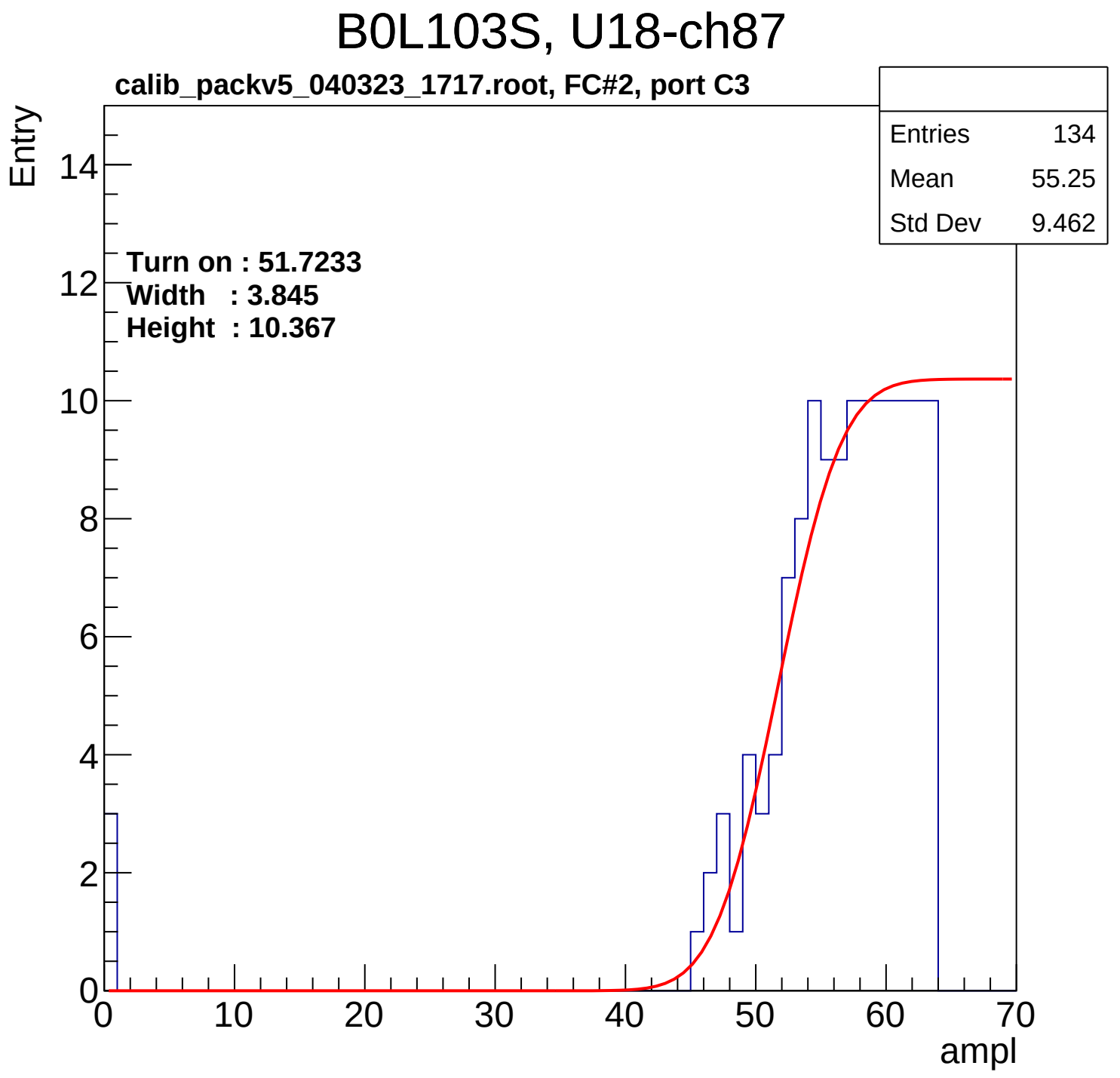
B0L103S, U18-ch87
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 55.25
Std Dev 9.462
Turn on : 51.7233
Width : 3.845
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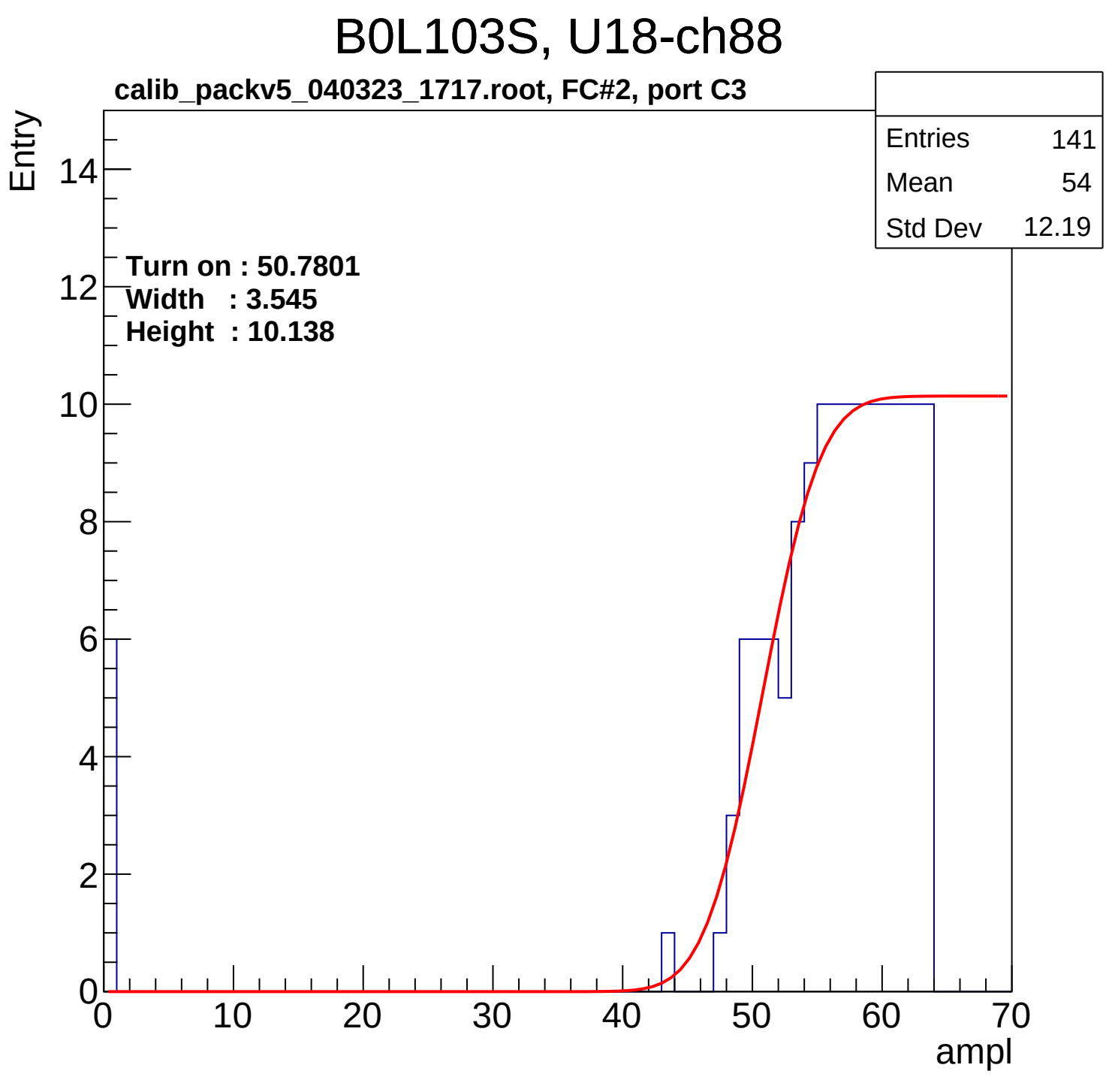
B0L103S, U18-ch88
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 54
Std Dev 12.19
Turn on : 50.7801
Width : 3.545
Height : 10.138
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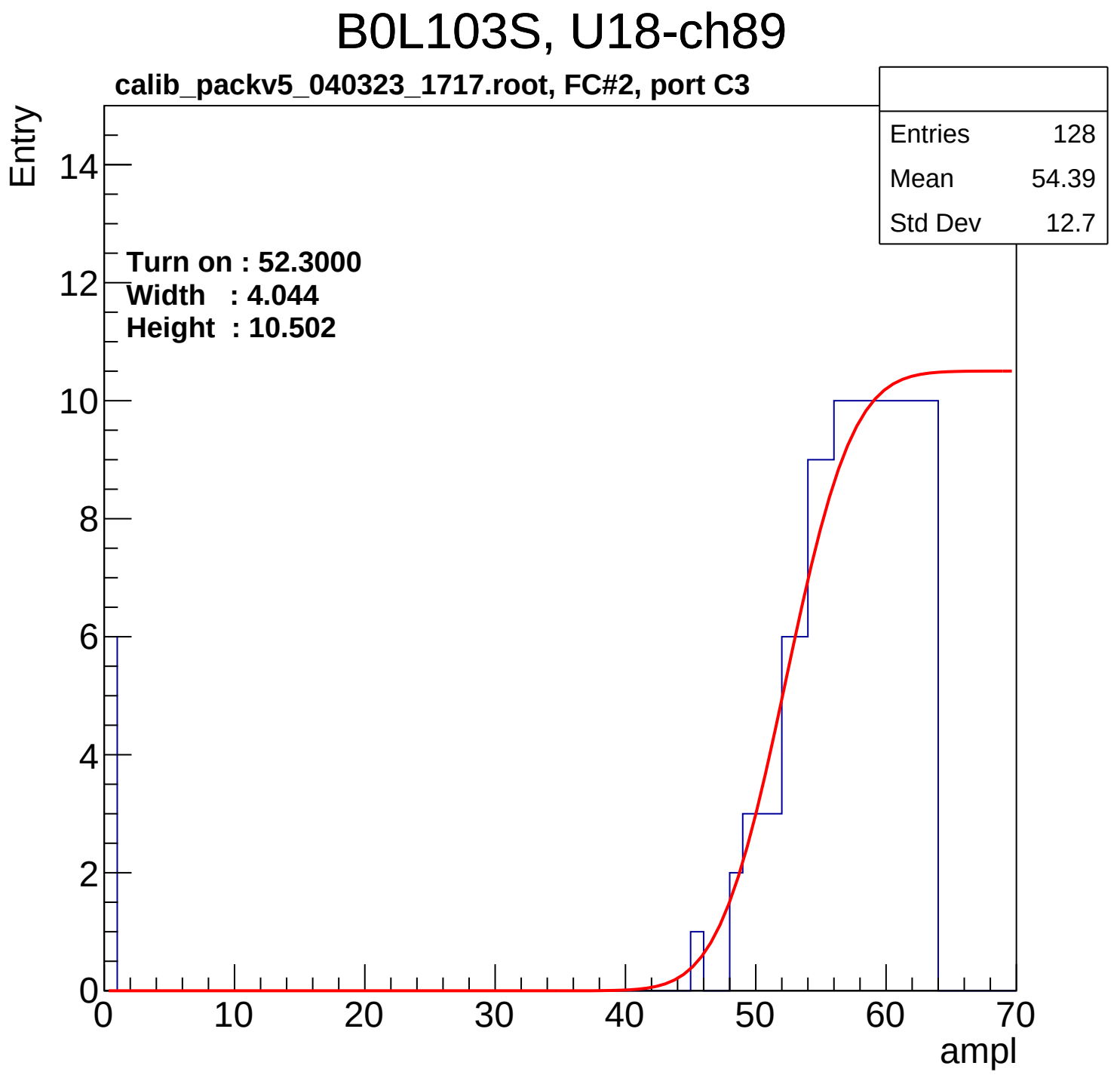
B0L103S, U18-ch89
calib_packv5_040323_1717.root, FC#2, port C3
Entries 128
Mean 54.39
Std Dev 12.7
Turn on : 52.3000
Width : 4.044
Height : 10.502
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ampl
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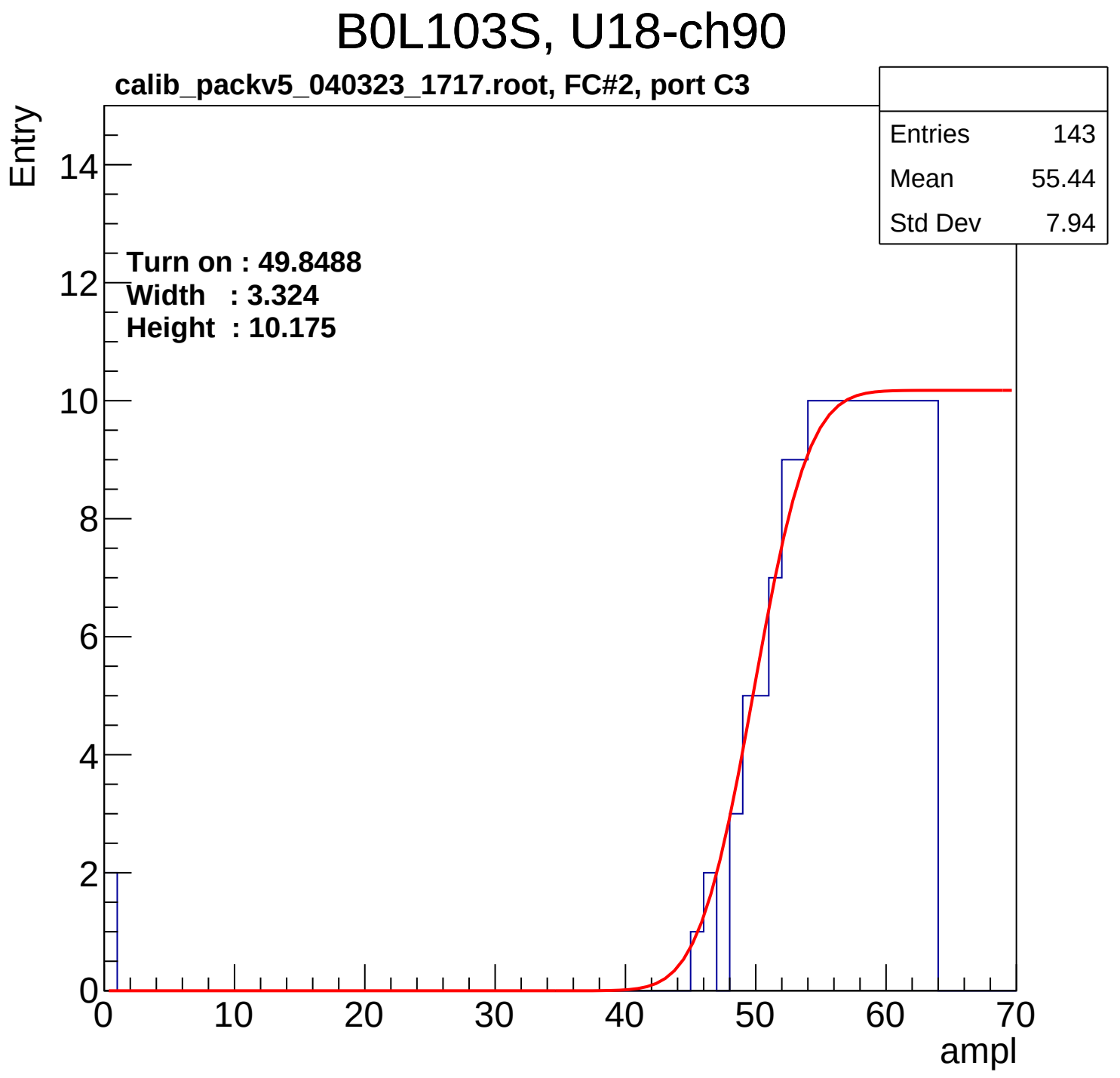
B0L103S, U18-ch90
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 55.44
Std Dev 7.94
Turn on : 49.8488
Width : 3.324
Height : 10.175
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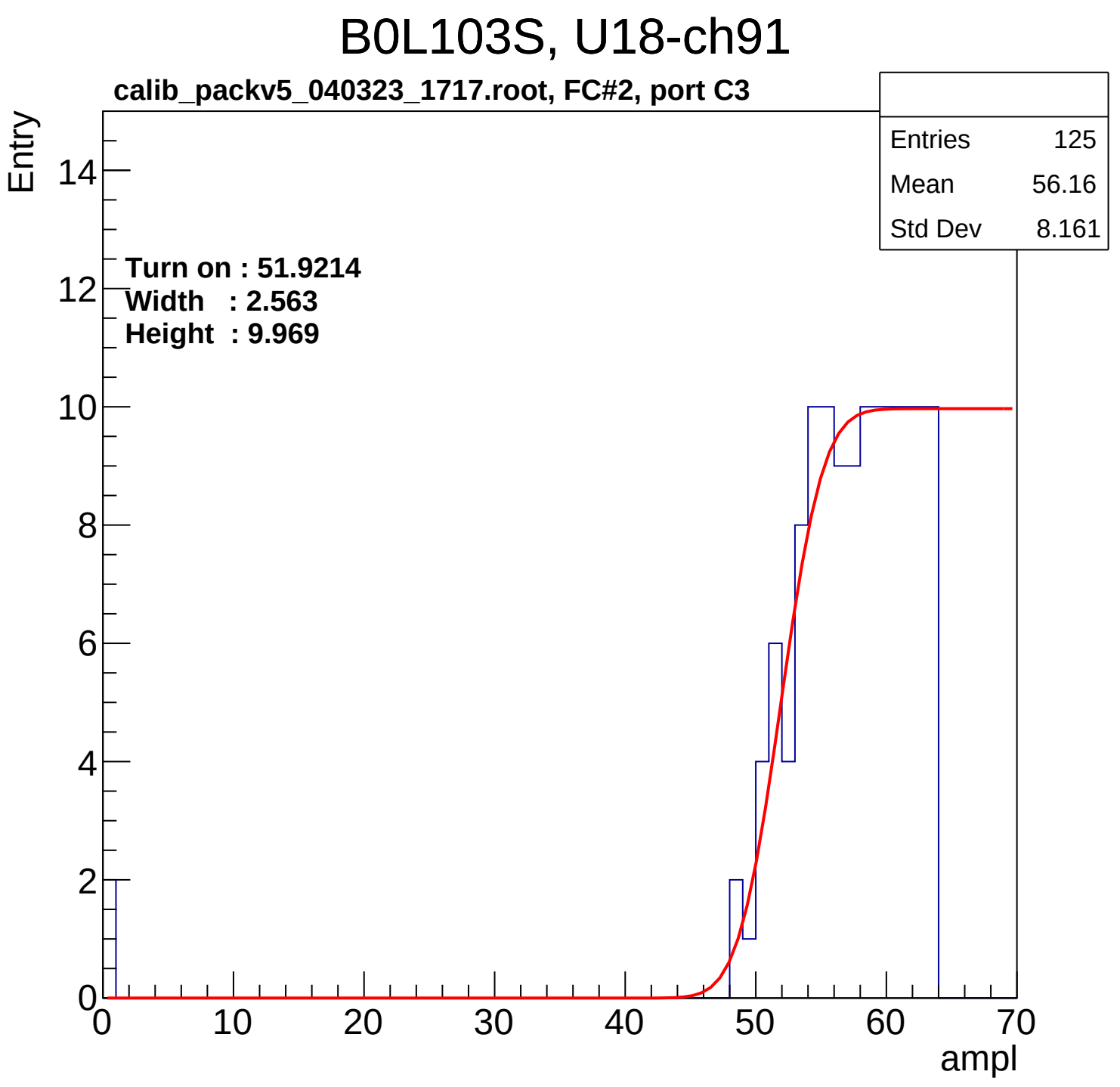
B0L103S, U18-ch91
calib_packv5_040323_1717.root, FC#2, port C3
Entries 125
Mean 56.16
Std Dev 8.161
Turn on : 51.9214
Width : 2.563
Height : 9.969
Entry
ampl
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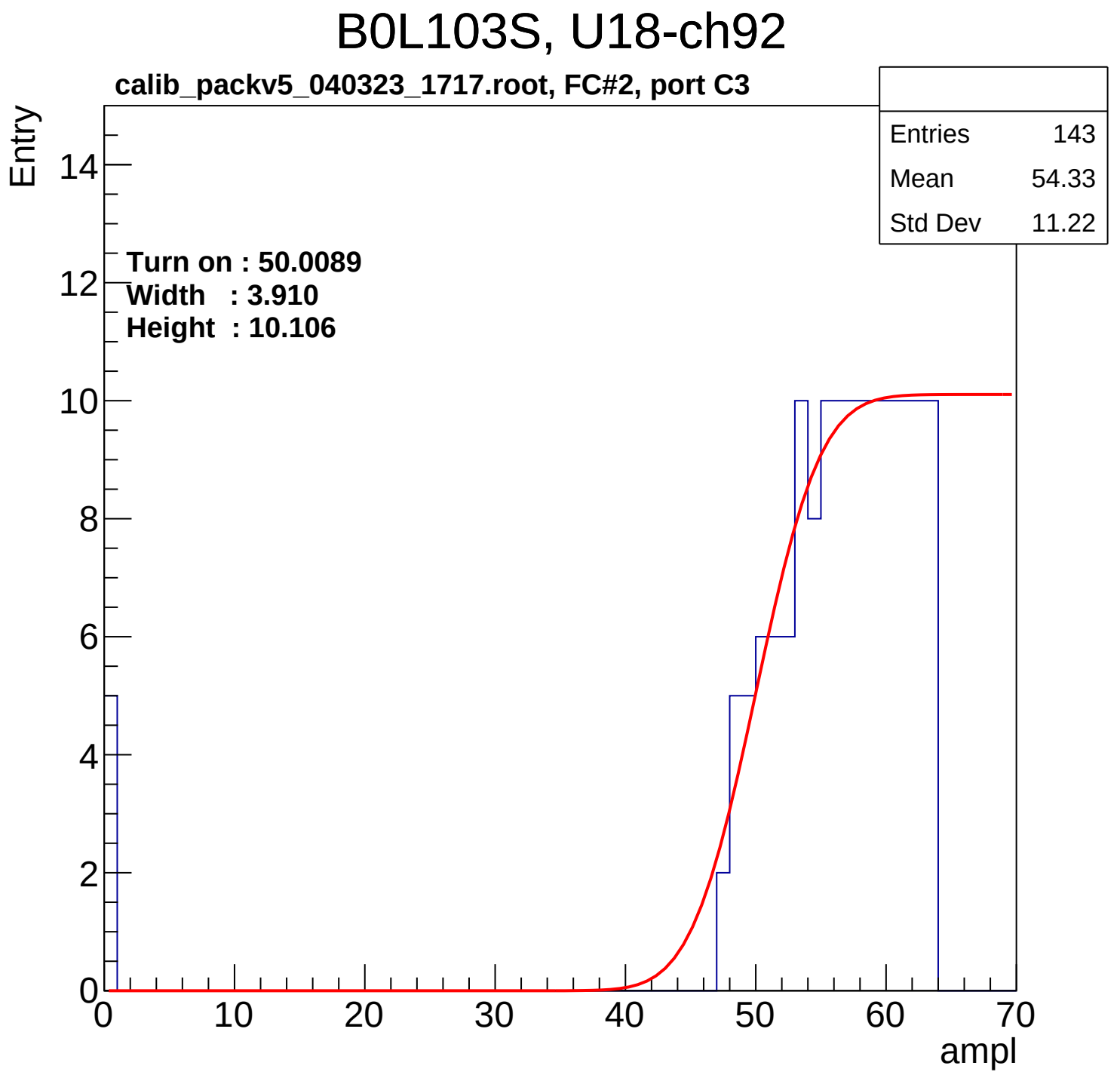
B0L103S, U18-ch92
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 54.33
Std Dev 11.22
Turn on : 50.0089
Width : 3.910
Height : 10.106
Entry
ampl
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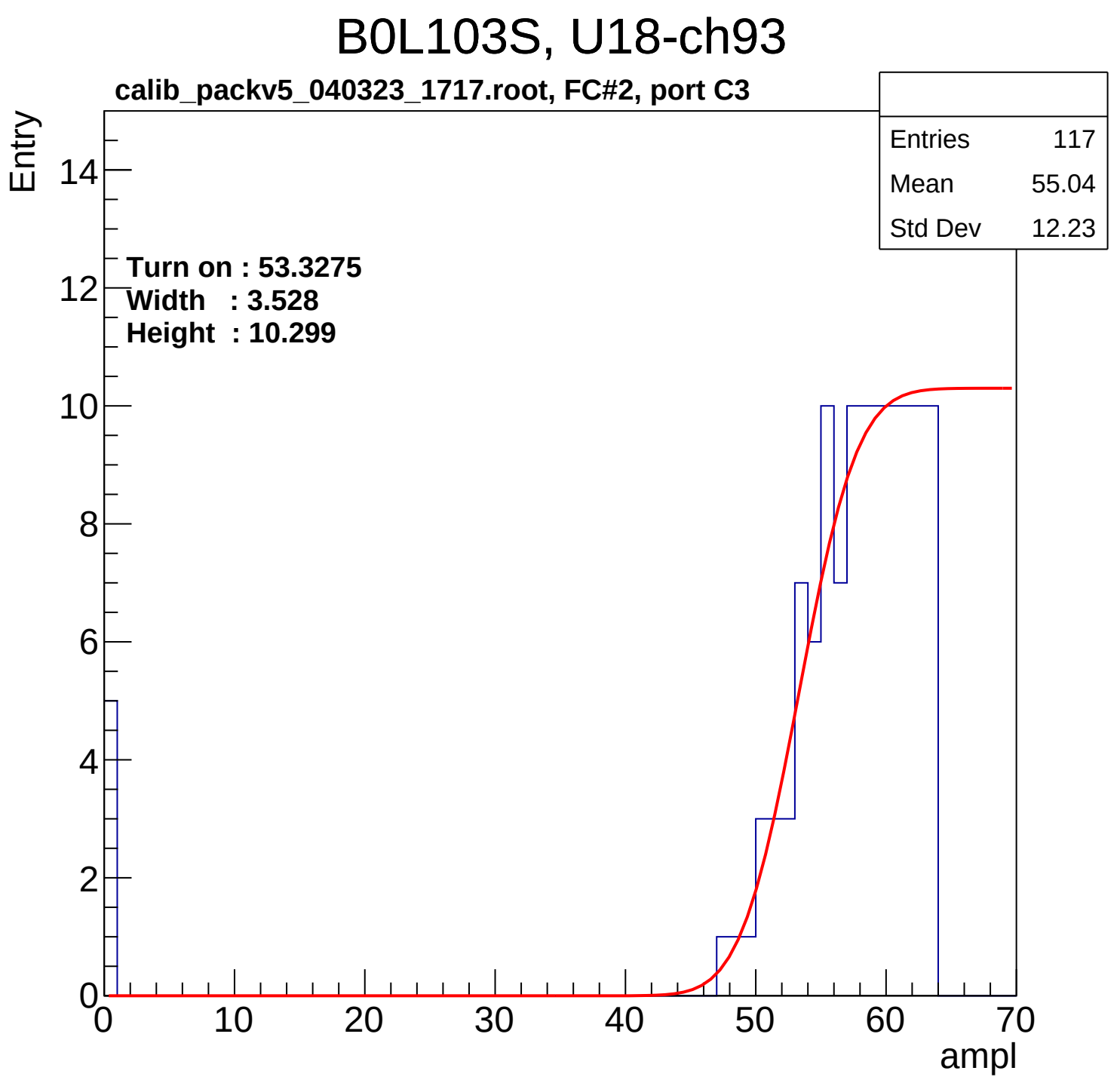
B0L103S, U18-ch93
calib_packv5_040323_1717.root, FC#2, port C3
Entries 117
Mean 55.04
Std Dev 12.23
Turn on : 53.3275
Width : 3.528
Height : 10.299
Entry
ampl
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6
8
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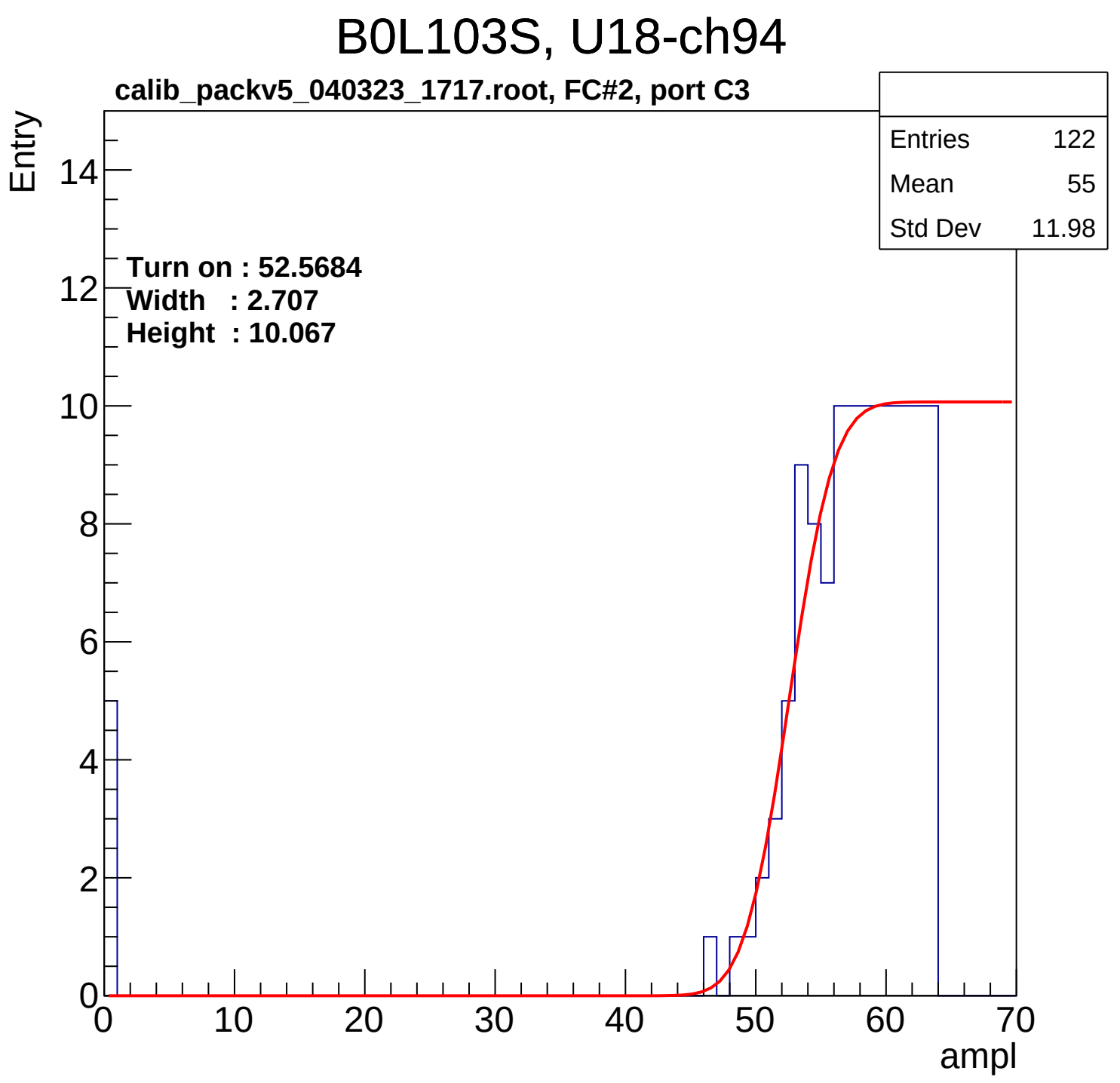
B0L103S, U18-ch94
calib_packv5_040323_1717.root, FC#2, port C3
Entries 122
Mean 55
Std Dev 11.98
Turn on : 52.5684
Width : 2.707
Height : 10.067
Entry
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4
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8
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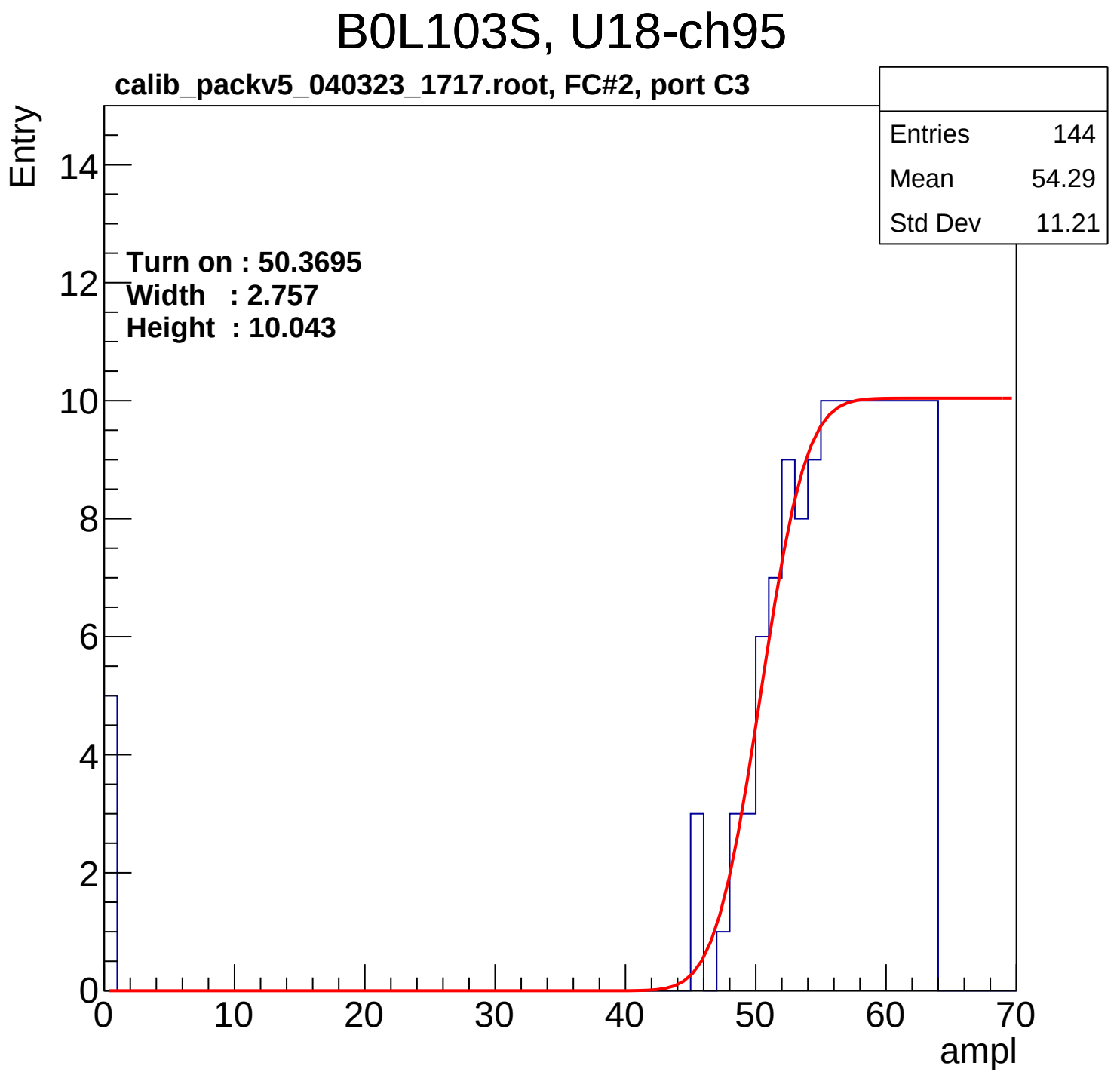
B0L103S, U18-ch95
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 54.29
Std Dev 11.21
Turn on : 50.3695
Width : 2.757
Height : 10.043
Entry
ampl
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8
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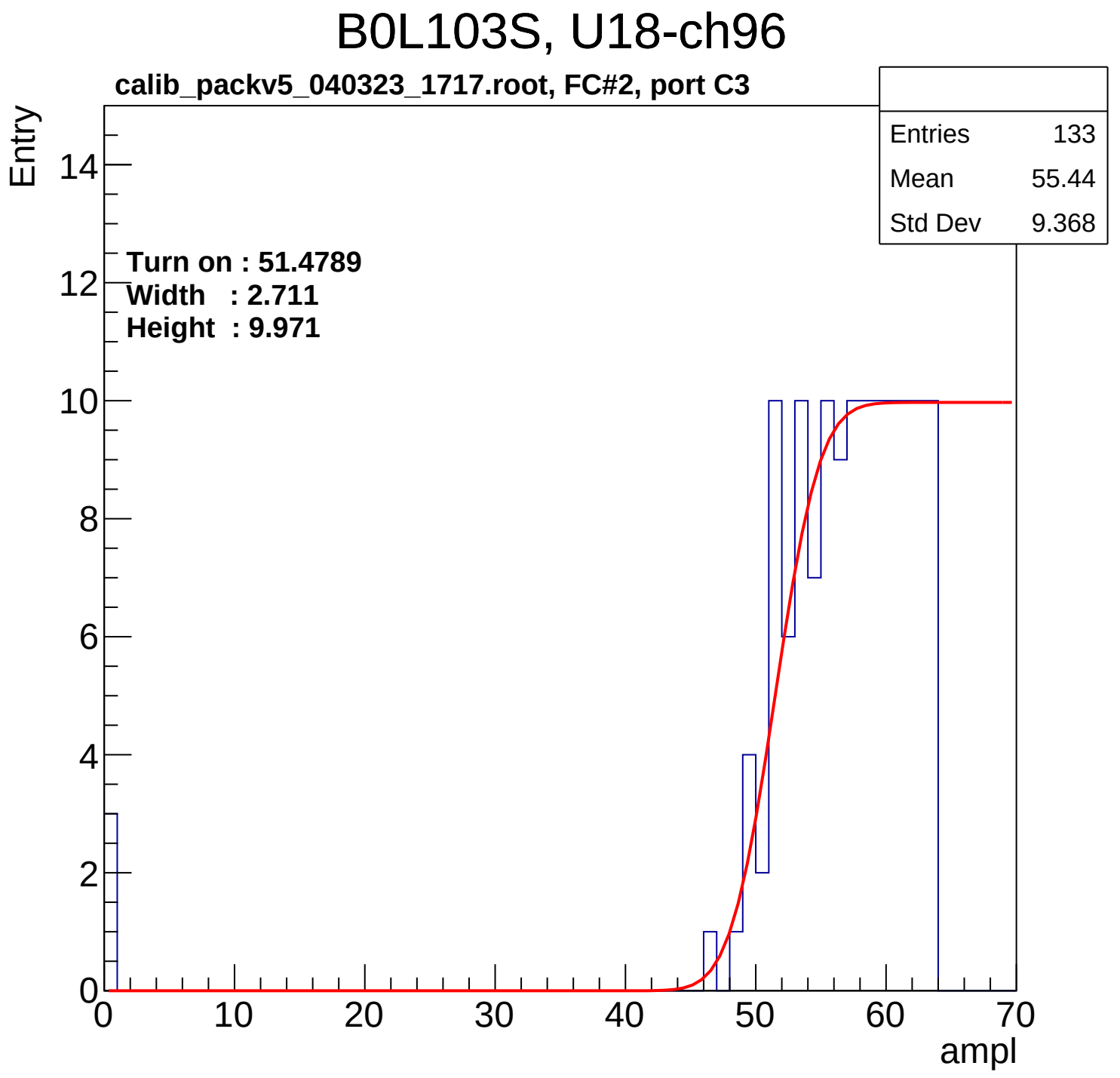
B0L103S, U18-ch96
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 55.44
Std Dev 9.368
Turn on : 51.4789
Width : 2.711
Height : 9.971
Entry
ampl
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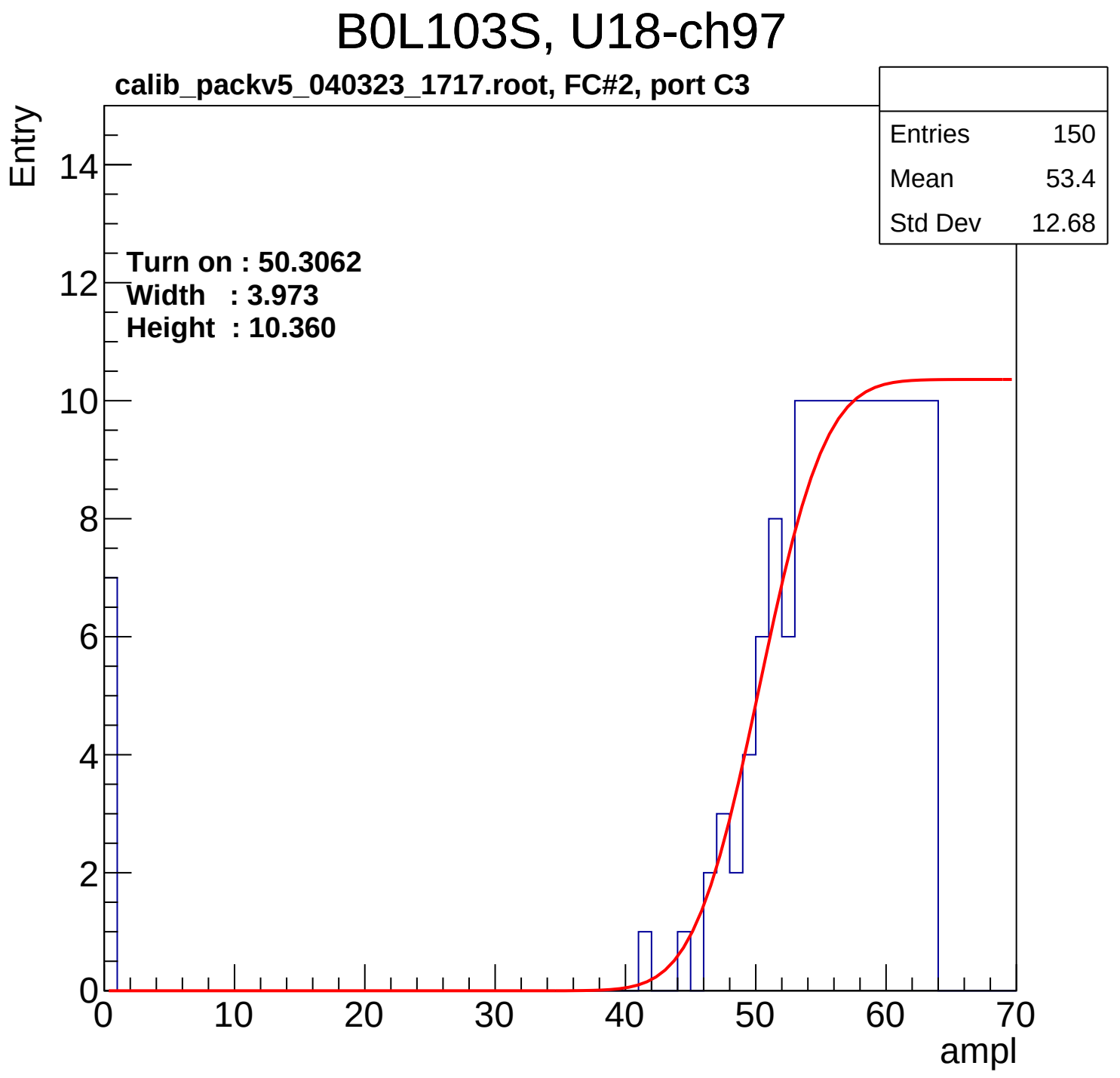
B0L103S, U18-ch97
calib_packv5_040323_1717.root, FC#2, port C3
Entries 150
Mean 53.4
Std Dev 12.68
Turn on : 50.3062
Width : 3.973
Height : 10.360
Entry
ampl
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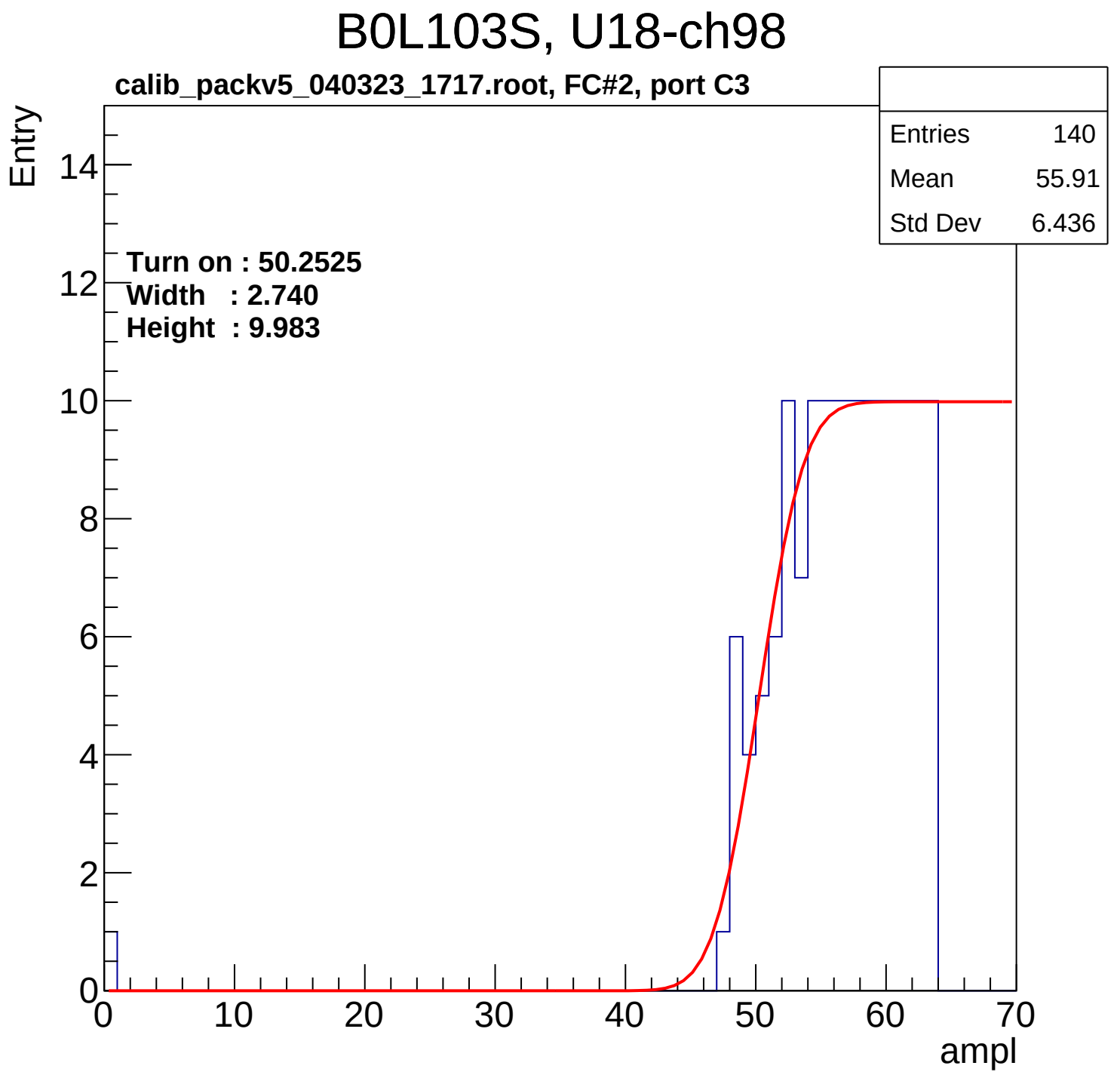
B0L103S, U18-ch98
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 55.91
Std Dev 6.436
Turn on : 50.2525
Width : 2.740
Height : 9.983
Entry
ampl
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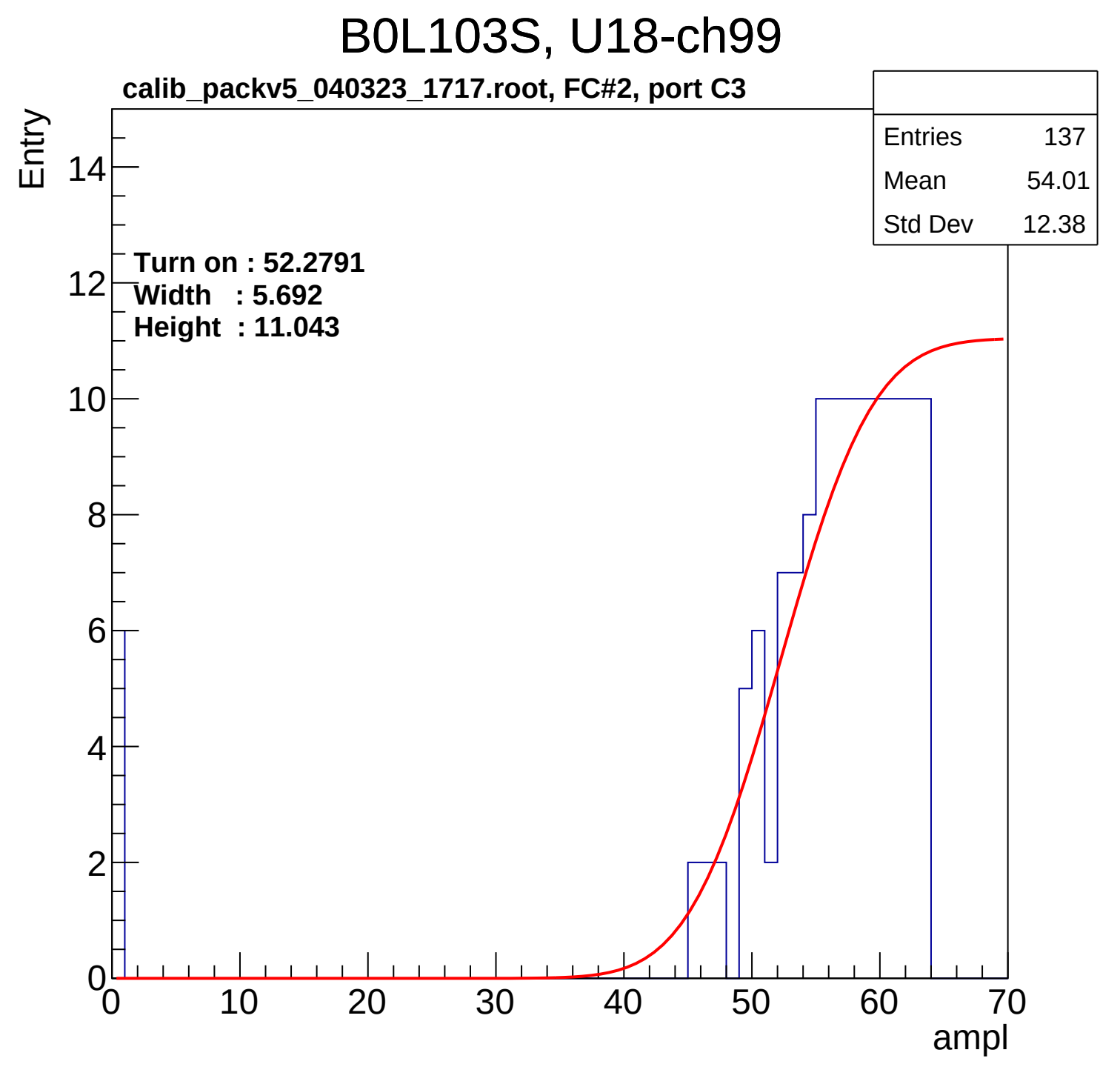
B0L103S, U18-ch99
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 54.01
Std Dev 12.38
Turn on : 52.2791
Width : 5.692
Height : 11.043
Entry
ampl
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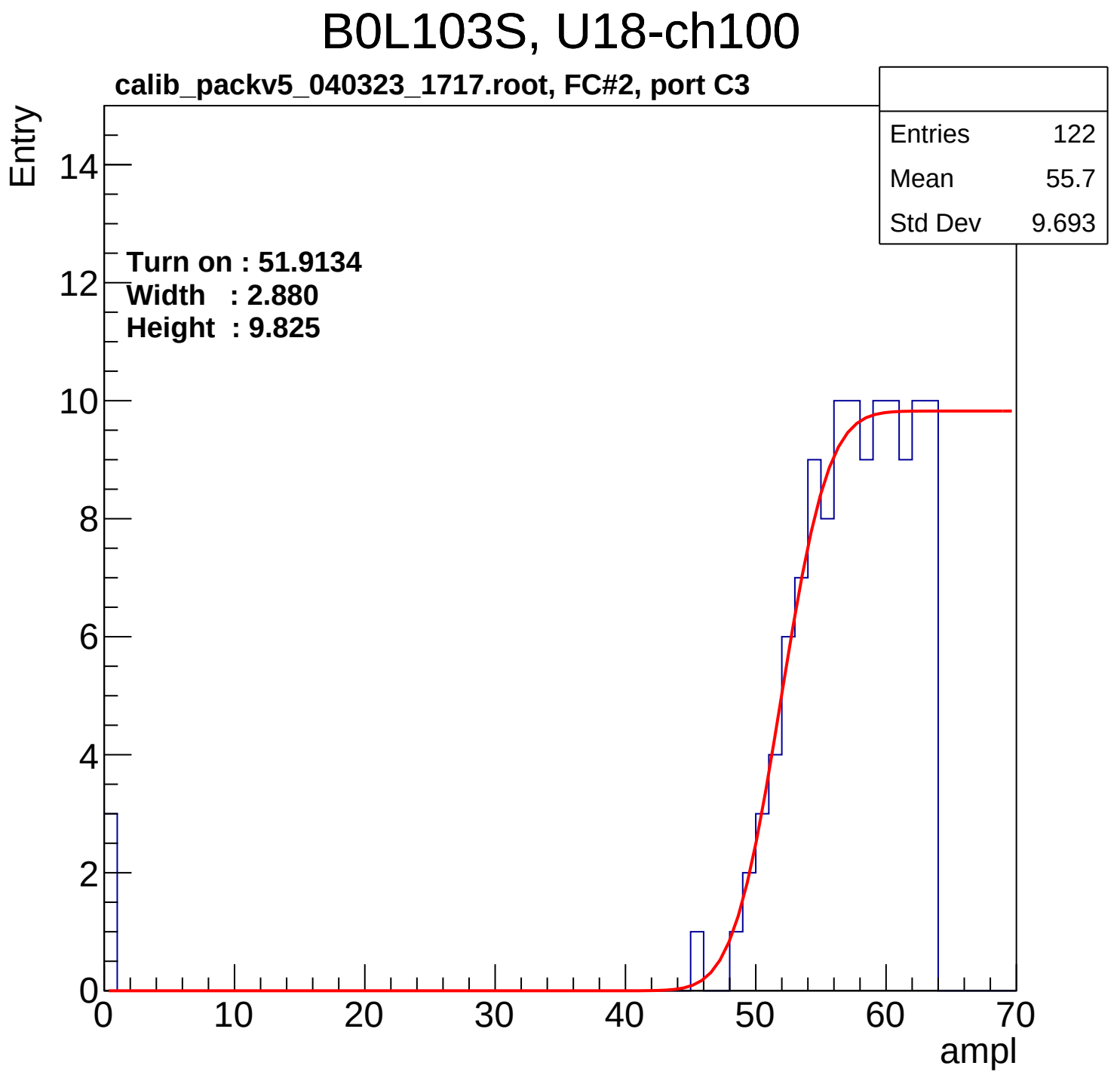
B0L103S, U18-ch100
calib_packv5_040323_1717.root, FC#2, port C3
Entries 122
Mean 55.7
Std Dev 9.693
Turn on : 51.9134
Width : 2.880
Height : 9.825
Entry
ampl
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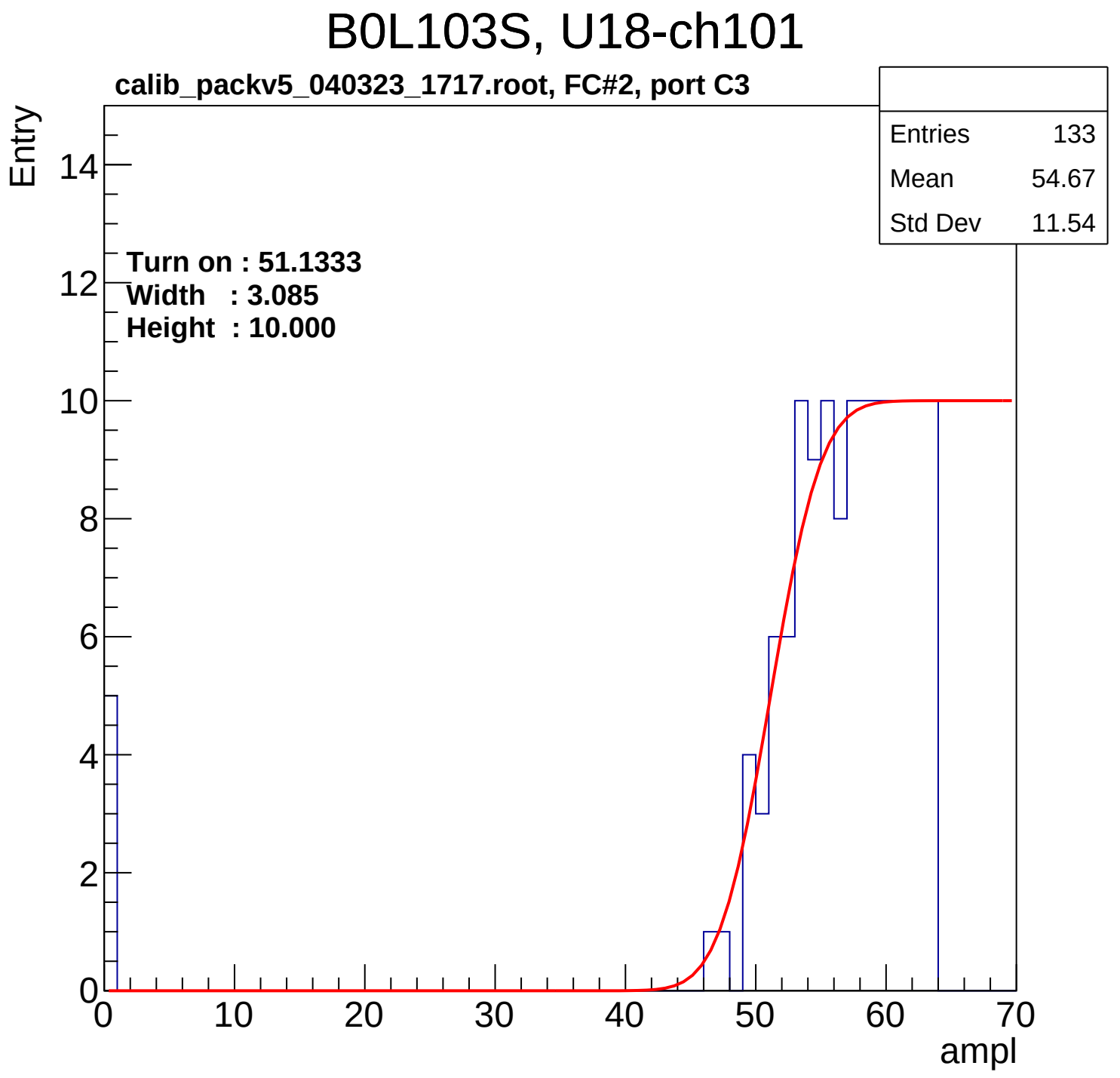
B0L103S, U18-ch101
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 54.67
Std Dev 11.54
Turn on : 51.1333
Width : 3.085
Height : 10.000
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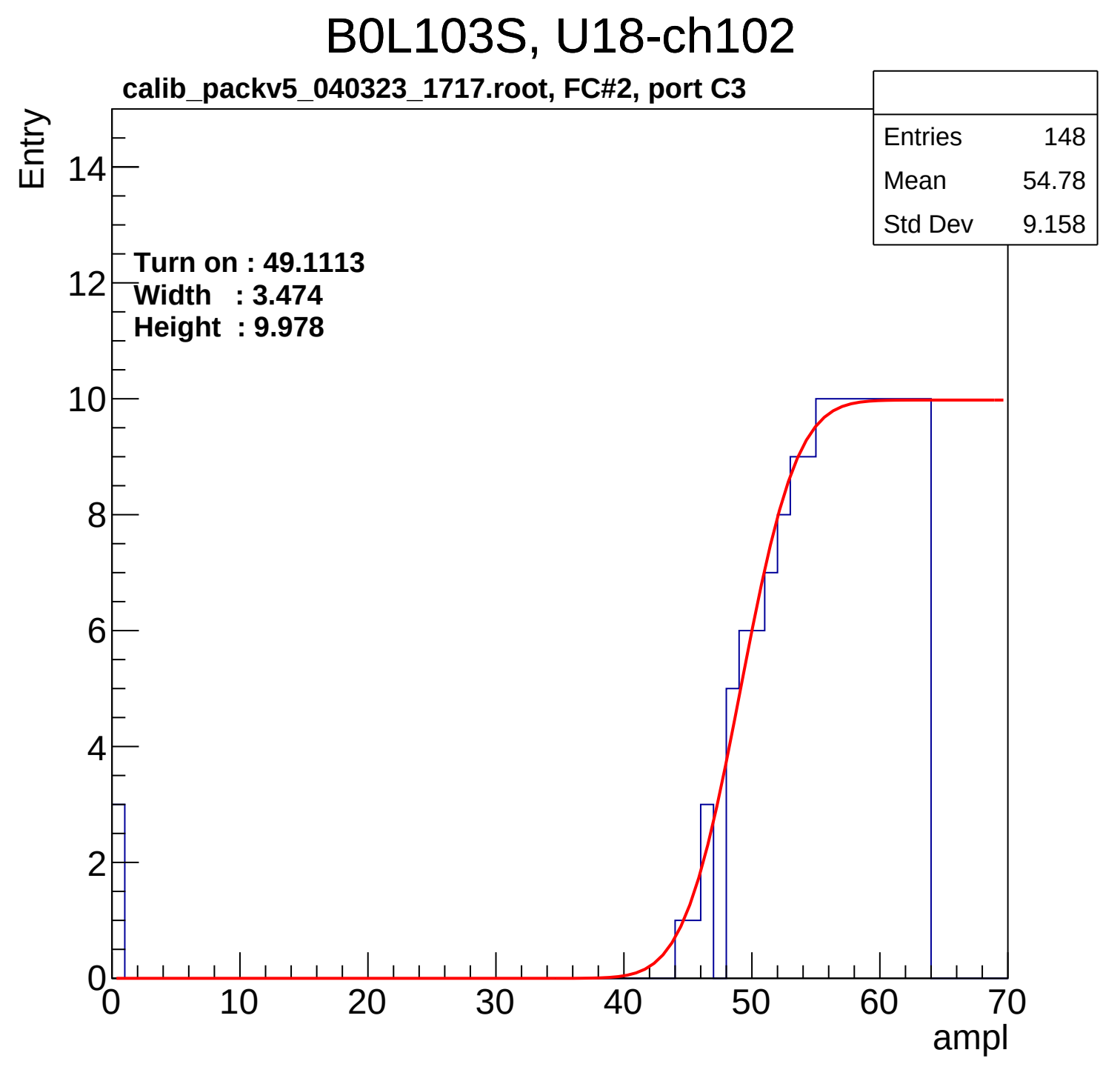
B0L103S, U18-ch102
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 54.78
Std Dev 9.158
Turn on : 49.1113
Width : 3.474
Height : 9.978
Entry
ampl
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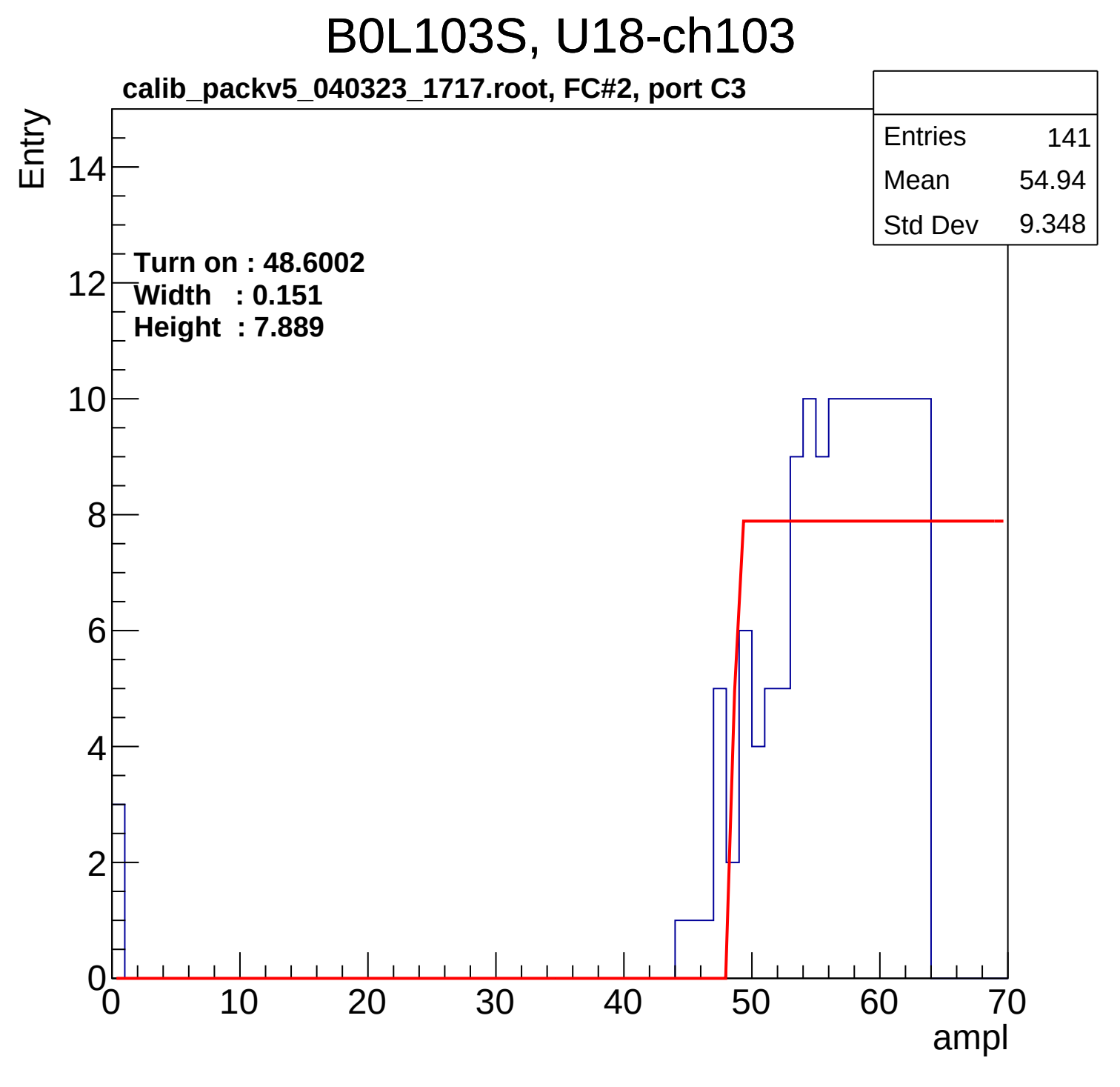
B0L103S, U18-ch103
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 54.94
Std Dev 9.348
Turn on : 48.6002
Width : 0.151
Height : 7.889
Entry
ampl
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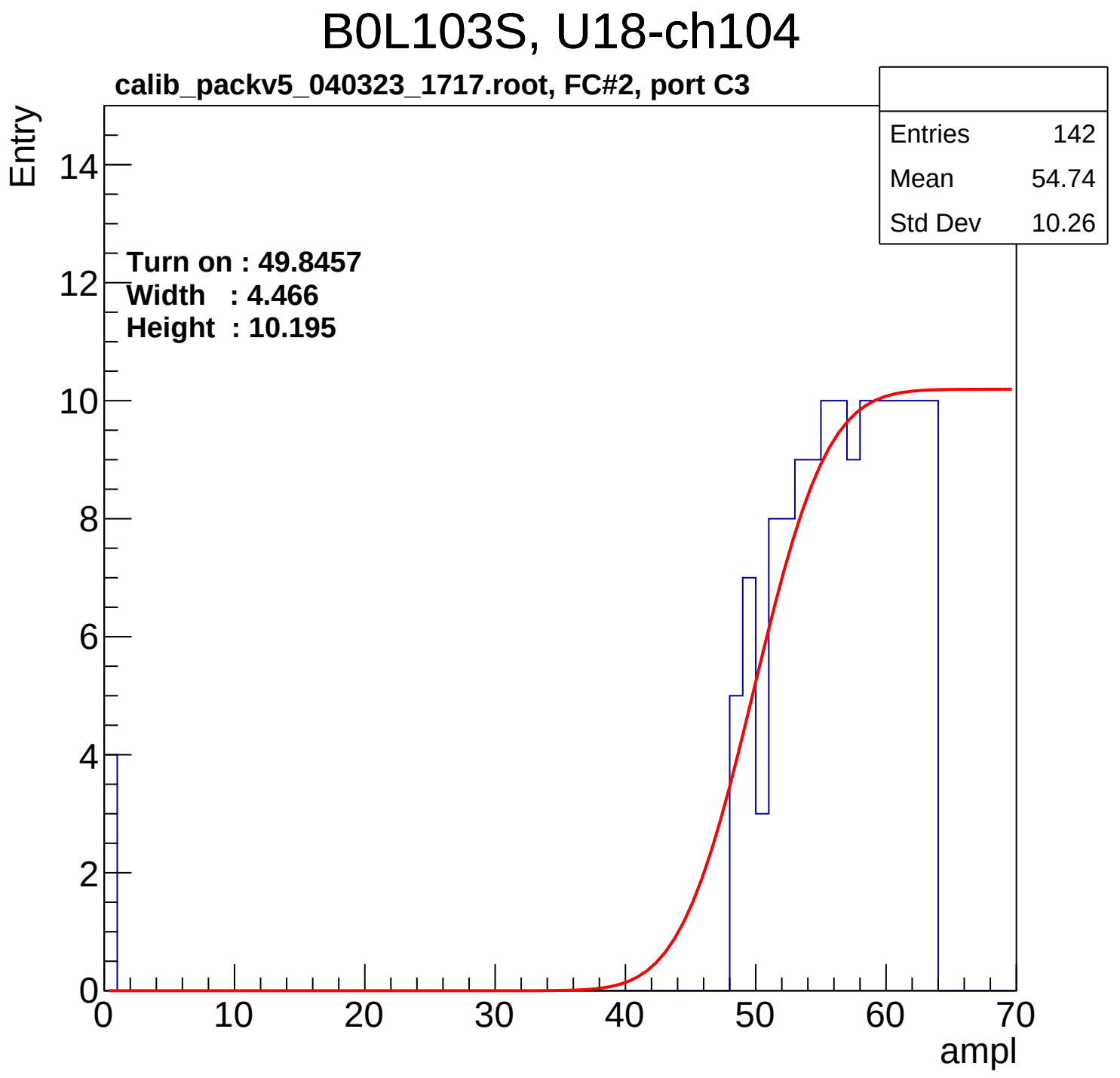
B0L103S, U18-ch104
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 54.74
Std Dev 10.26
Turn on : 49.8457
Width : 4.466
Height : 10.195
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ampl
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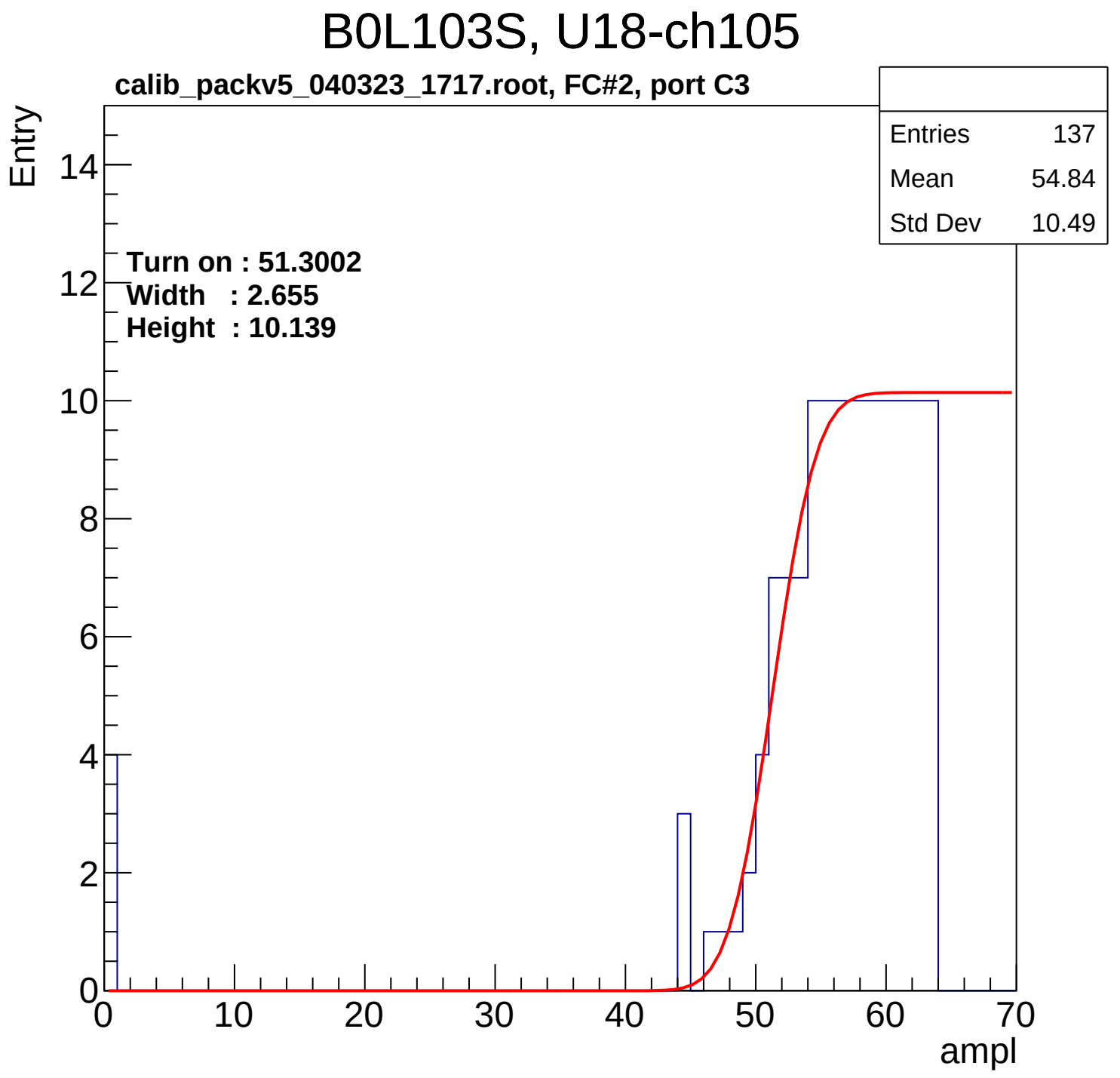
B0L103S, U18-ch105
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 54.84
Std Dev 10.49
Turn on : 51.3002
Width : 2.655
Height : 10.139
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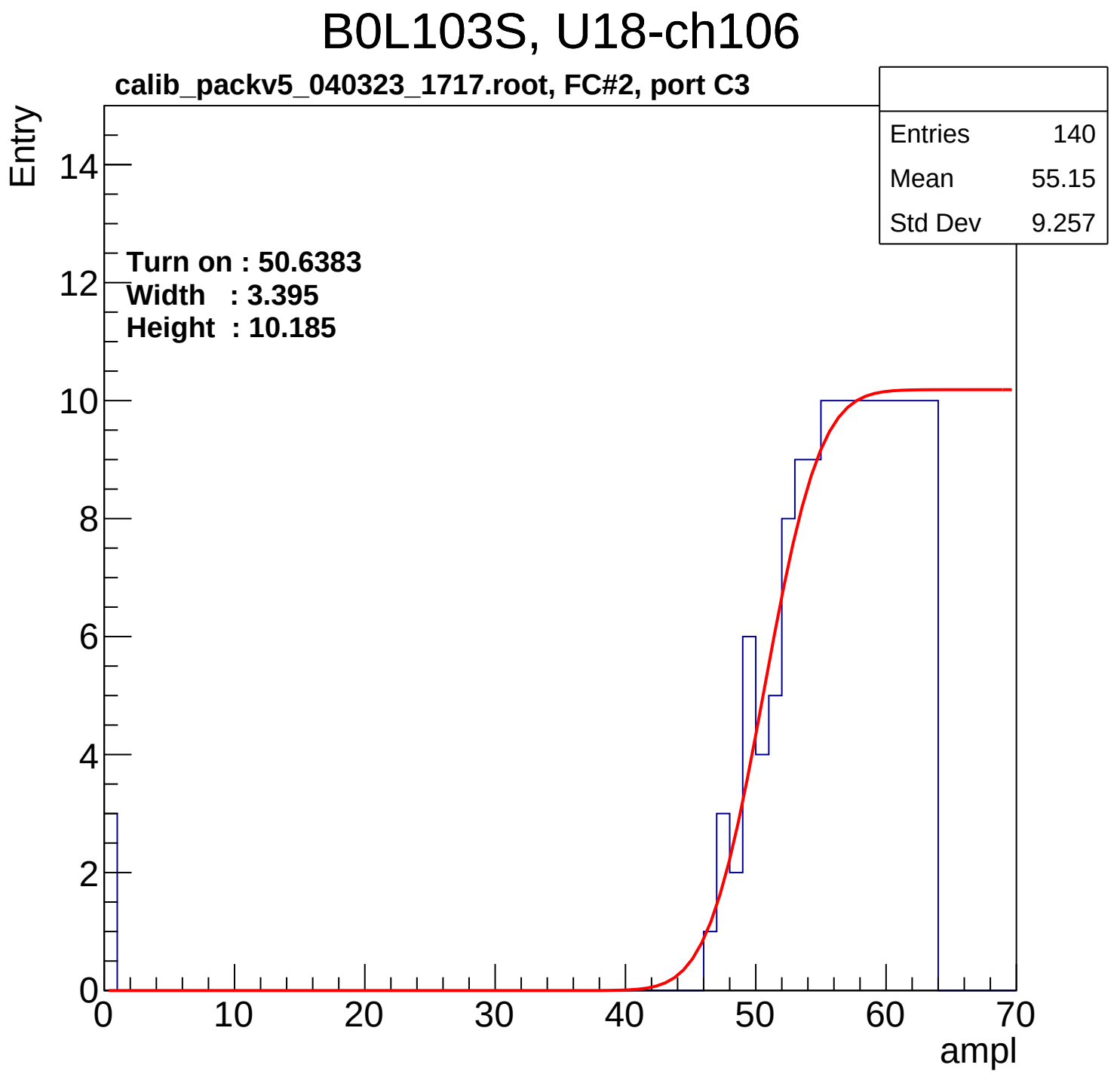
B0L103S, U18-ch106
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 55.15
Std Dev 9.257
Turn on : 50.6383
Width : 3.395
Height : 10.185
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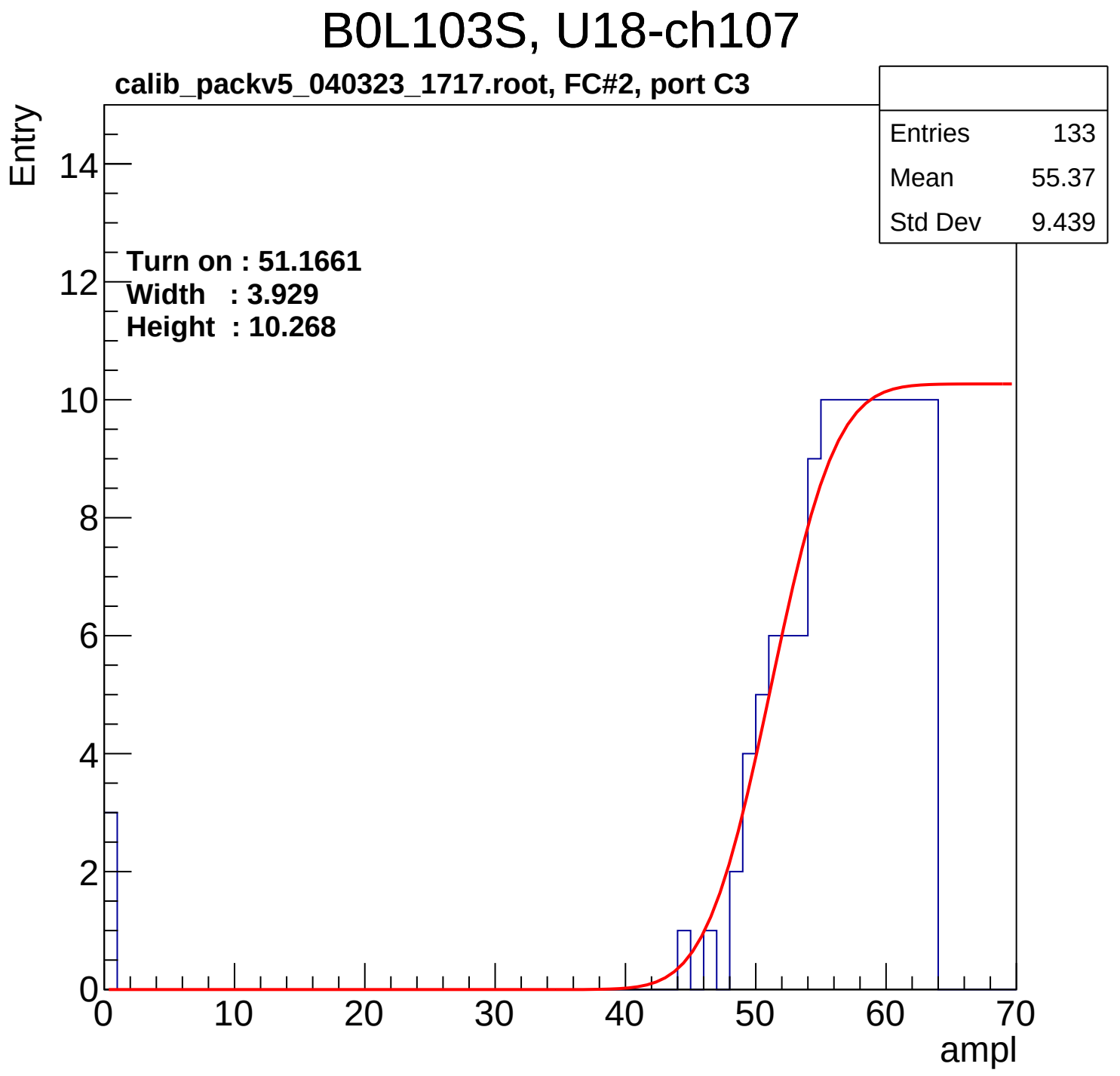
B0L103S, U18-ch107
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 55.37
Std Dev 9.439
Turn on : 51.1661
Width : 3.929
Height : 10.268
Entry
ampl
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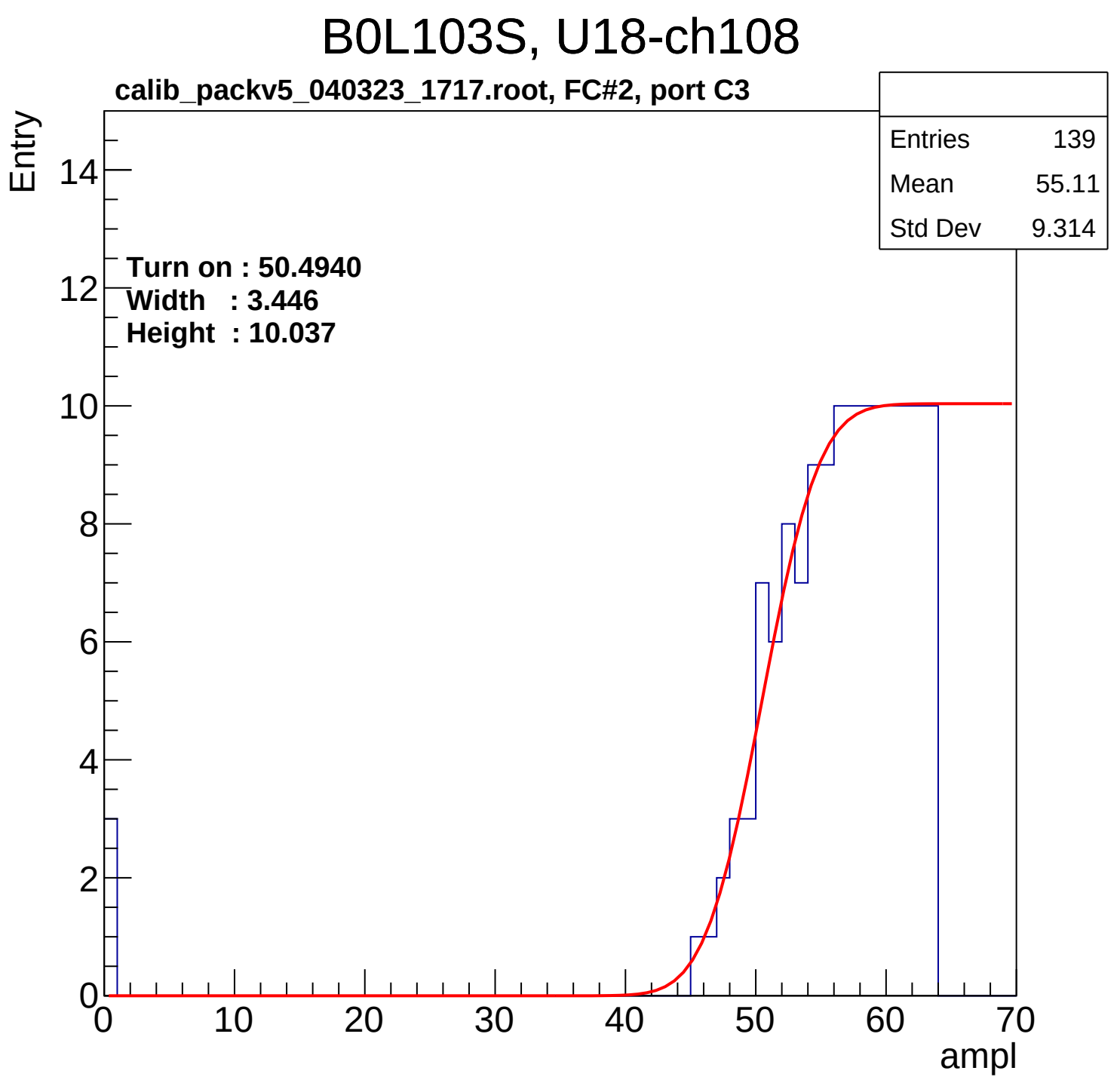
B0L103S, U18-ch108
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 55.11
Std Dev 9.314
Turn on : 50.4940
Width : 3.446
Height : 10.037
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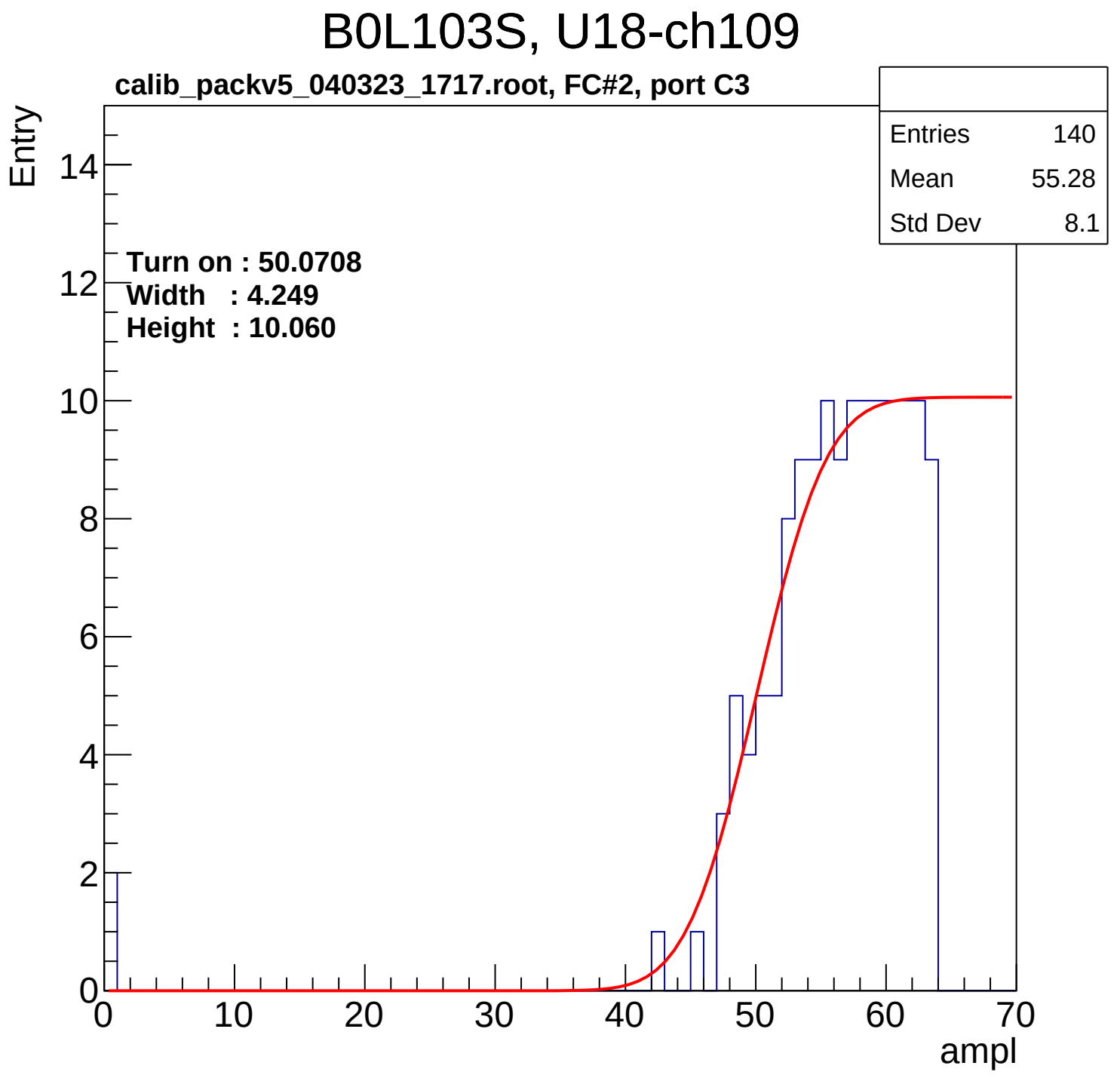
B0L103S, U18-ch109
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 55.28
Std Dev 8.1
Turn on : 50.0708
Width : 4.249
Height : 10.060
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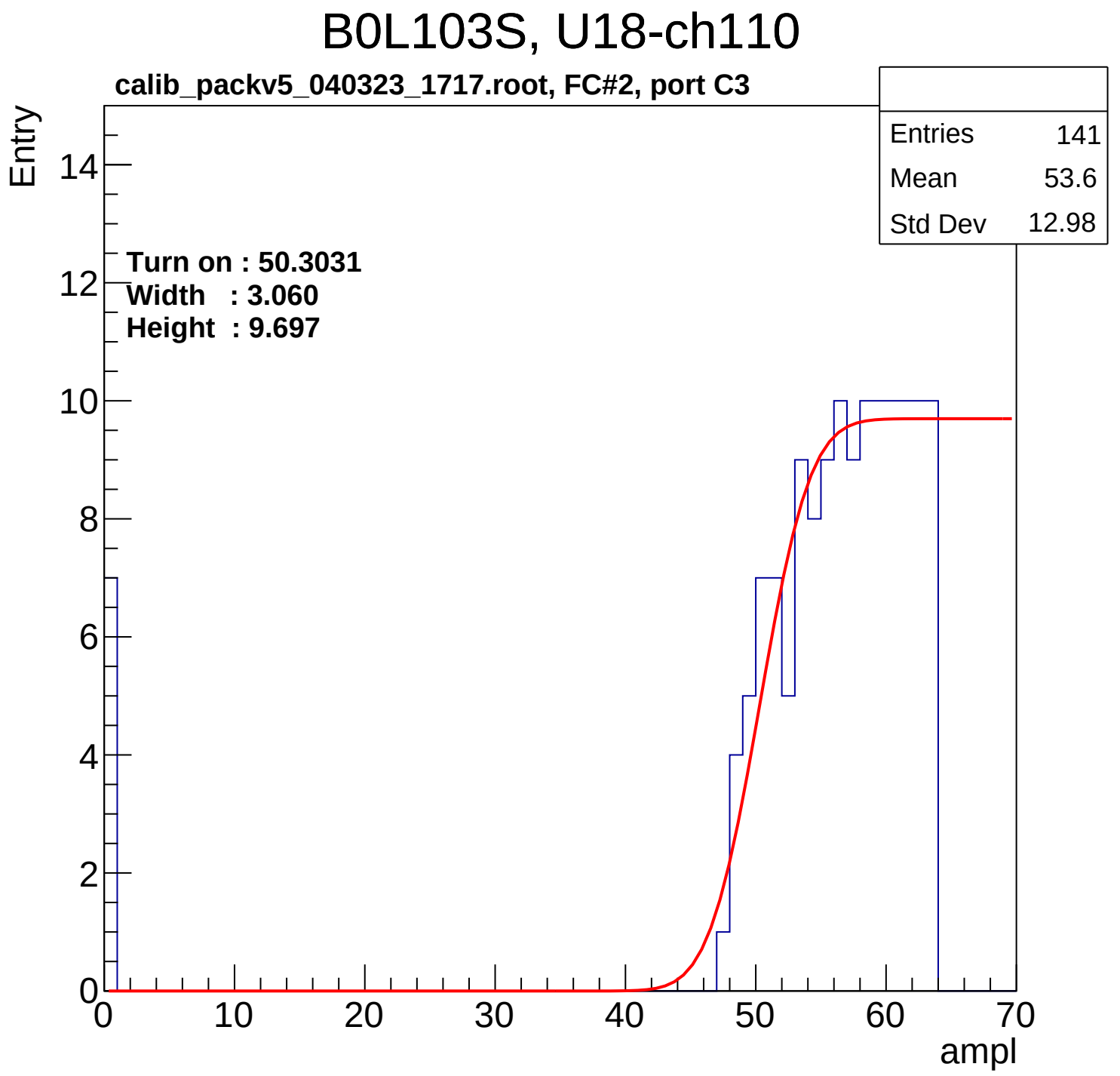
B0L103S, U18-ch110
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 53.6
Std Dev 12.98
Turn on : 50.3031
Width : 3.060
Height : 9.697
Entry
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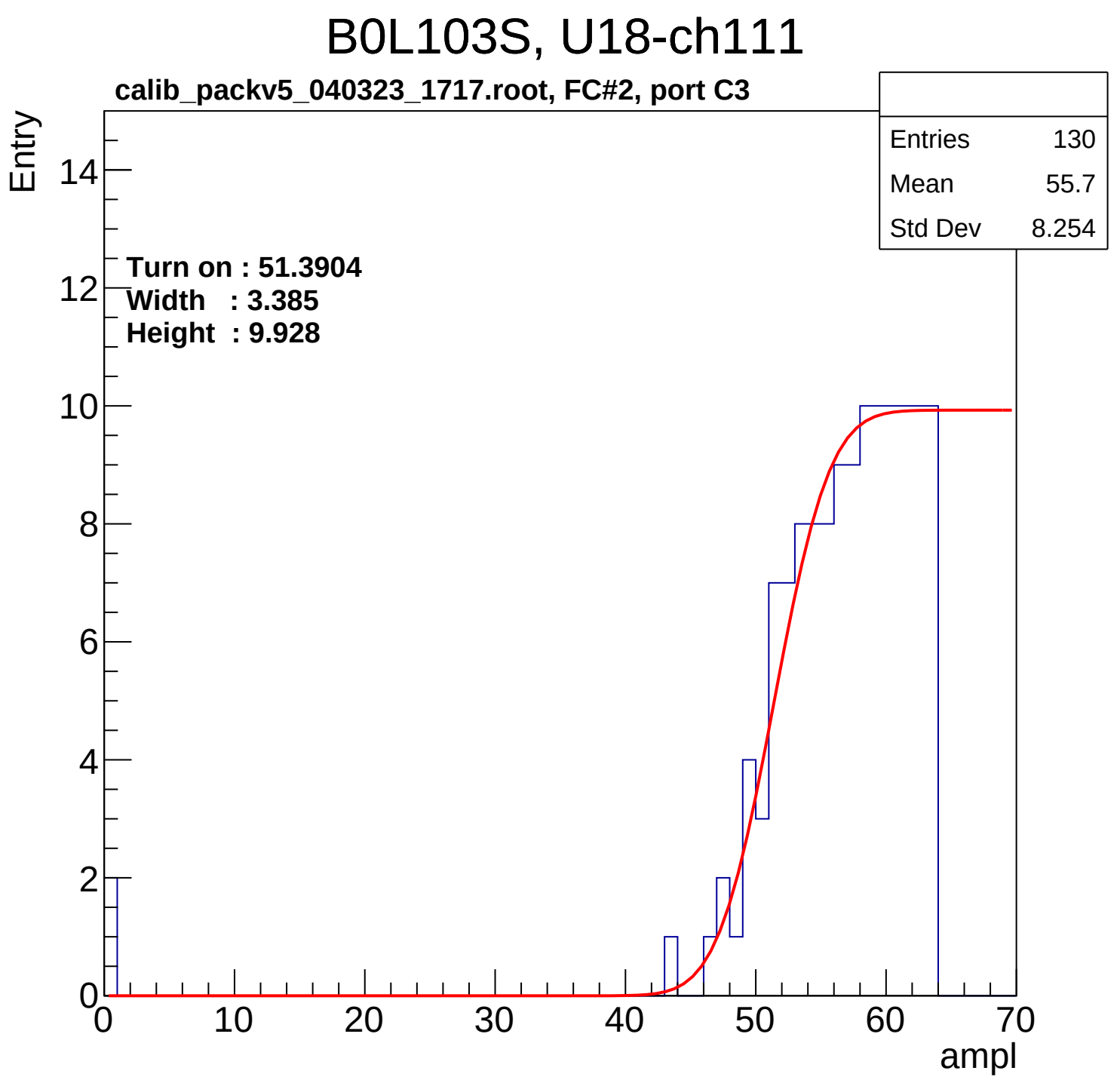
B0L103S, U18-ch111
calib_packv5_040323_1717.root, FC#2, port C3
Entries 130
Mean 55.7
Std Dev 8.254
Turn on : 51.3904
Width : 3.385
Height : 9.928
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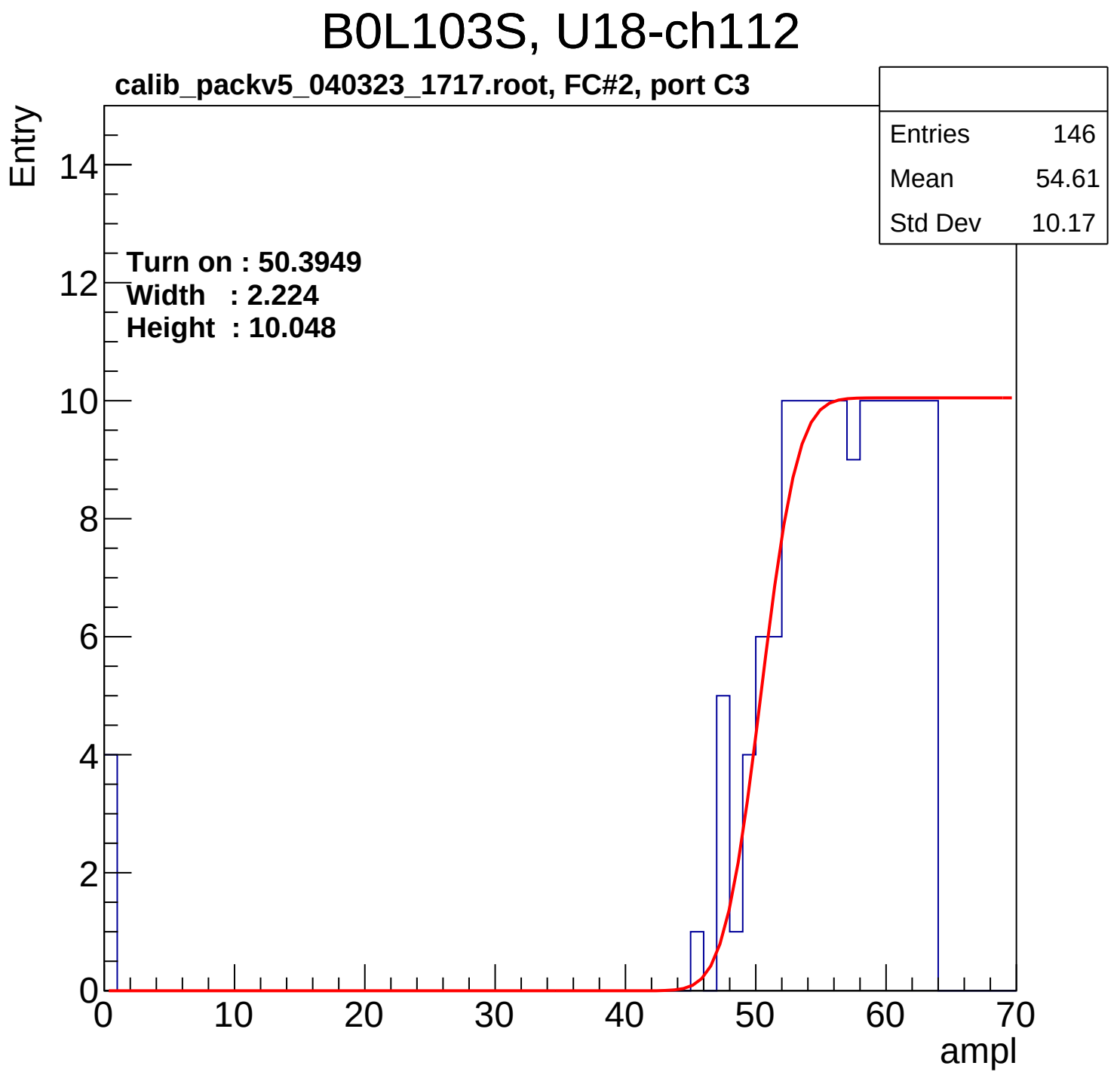
B0L103S, U18-ch112
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 54.61
Std Dev 10.17
Turn on : 50.3949
Width : 2.224
Height : 10.048
Entry
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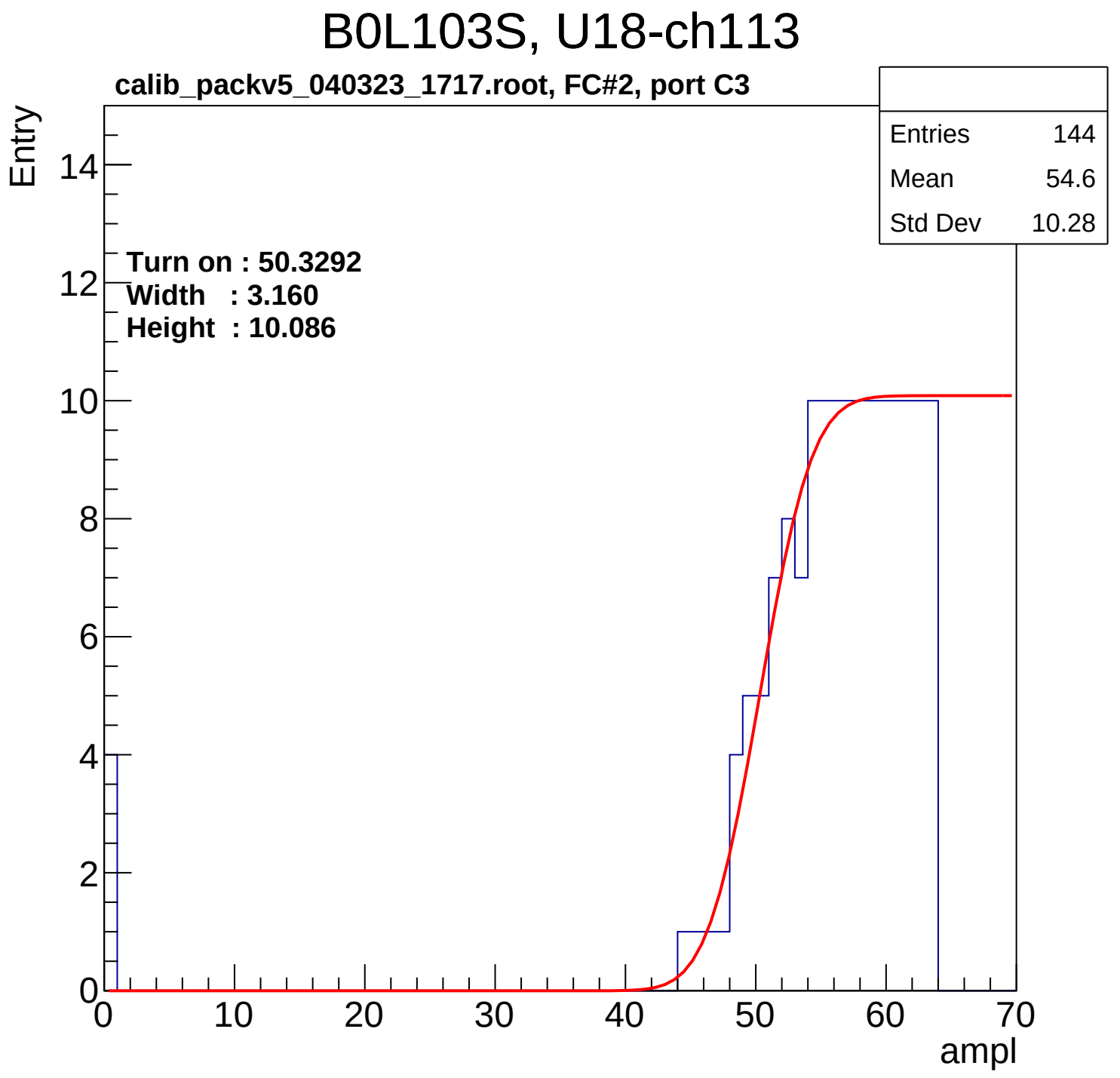
B0L103S, U18-ch113
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 54.6
Std Dev 10.28
Turn on : 50.3292
Width : 3.160
Height : 10.086
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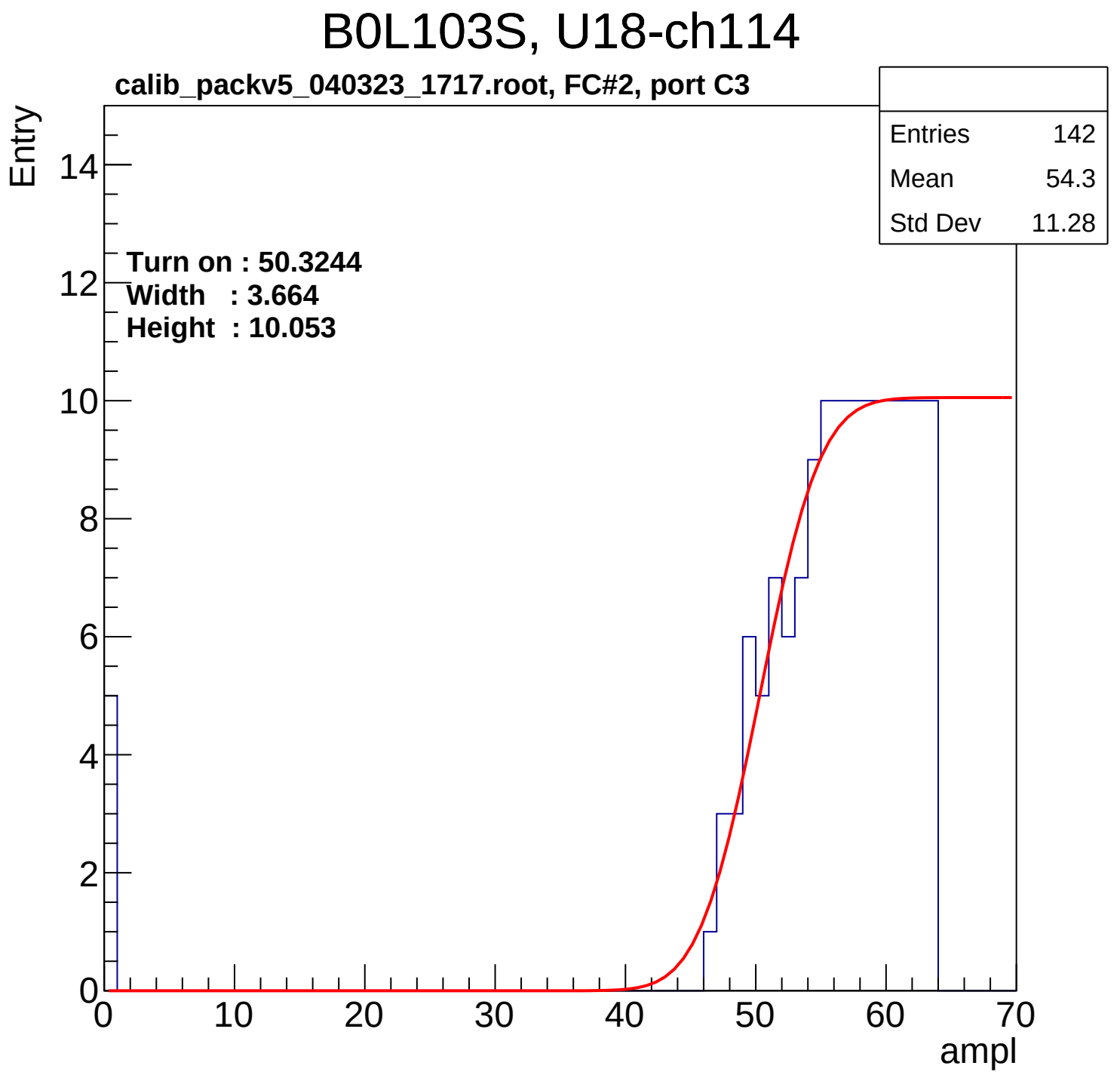
B0L103S, U18-ch114
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 54.3
Std Dev 11.28
Turn on : 50.3244
Width : 3.664
Height : 10.053
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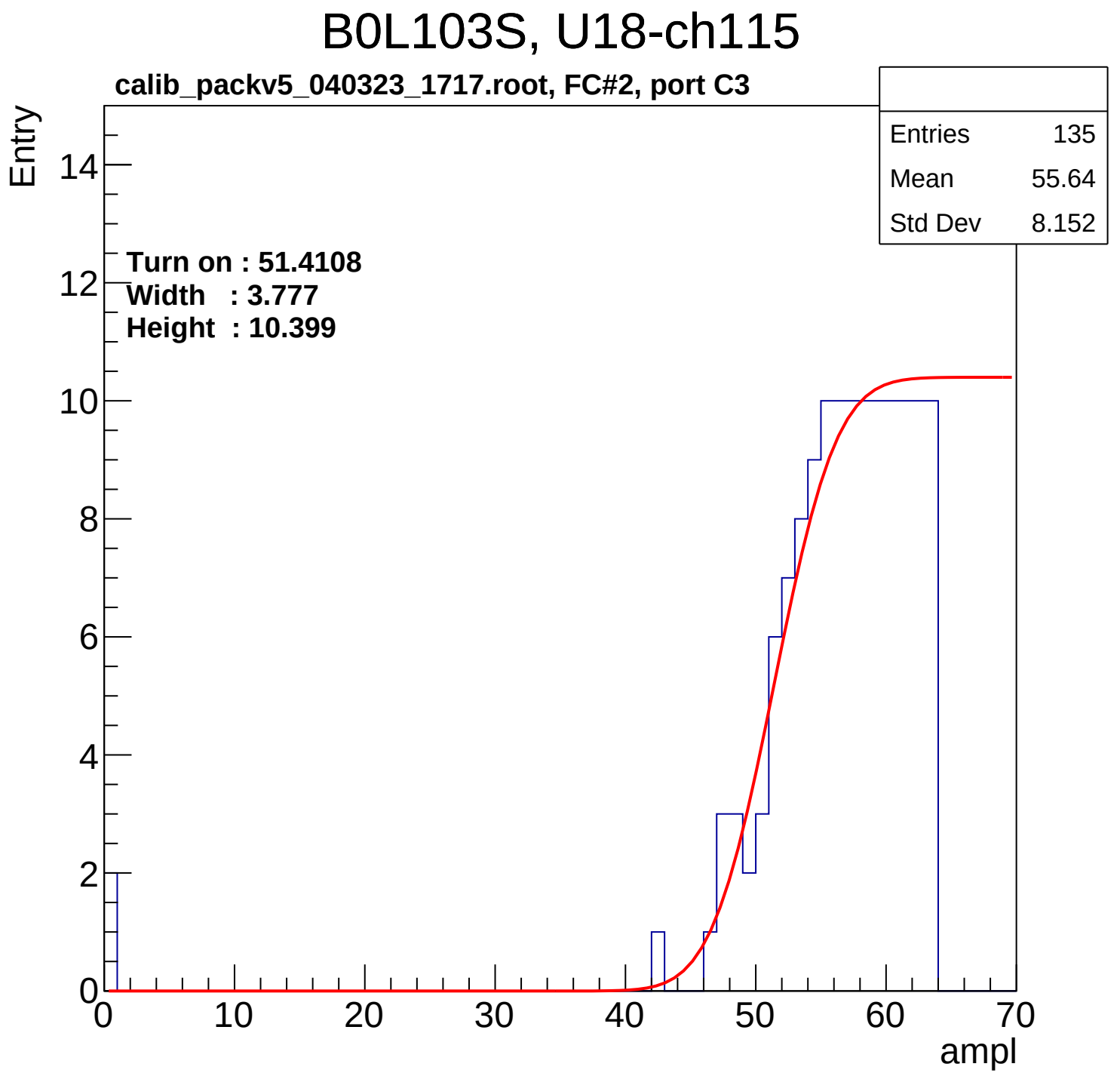
B0L103S, U18-ch115
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 55.64
Std Dev 8.152
Turn on : 51.4108
Width : 3.777
Height : 10.399
Entry
ampl
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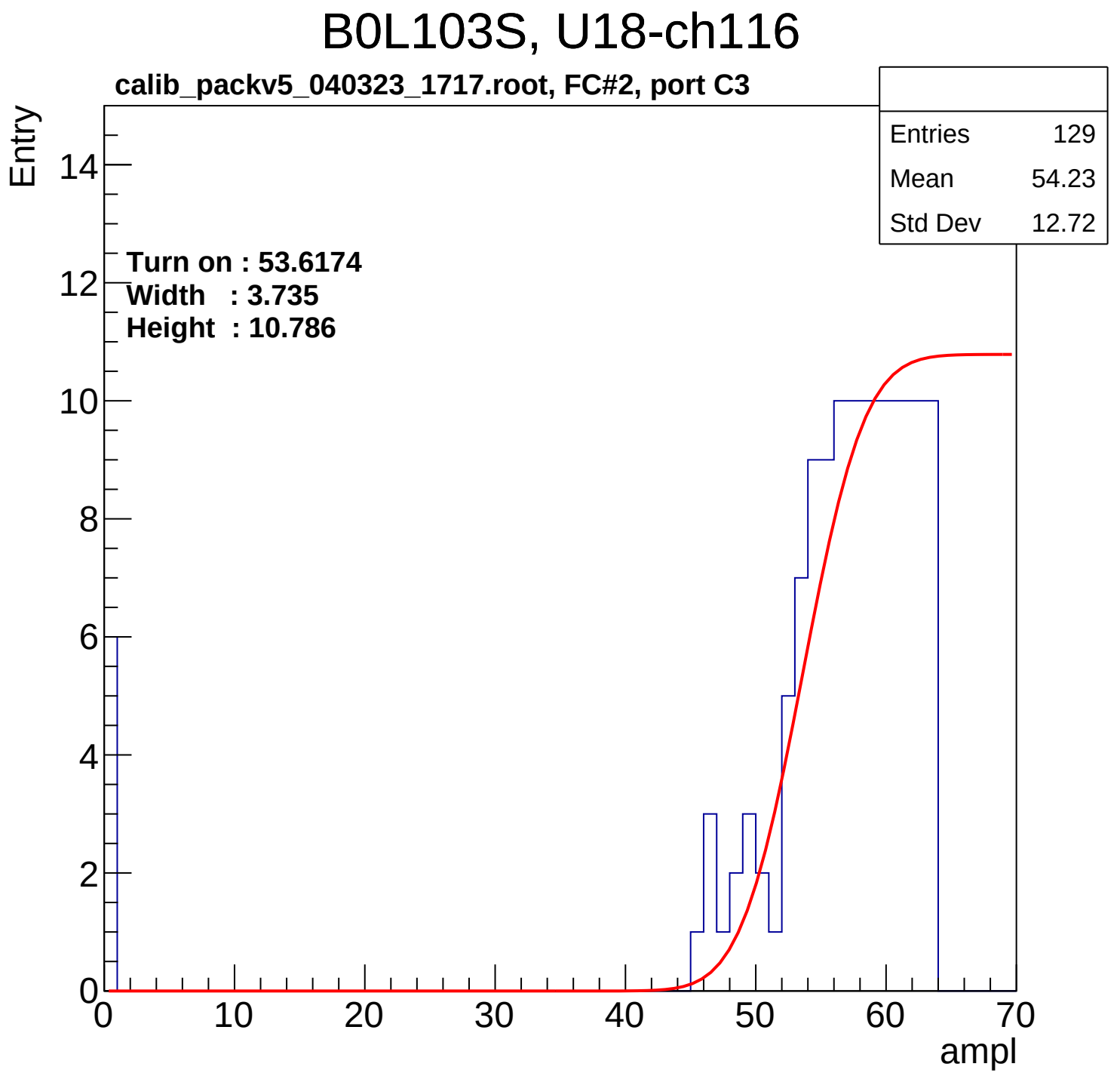
B0L103S, U18-ch116
calib_packv5_040323_1717.root, FC#2, port C3
Entries 129
Mean 54.23
Std Dev 12.72
Turn on : 53.6174
Width : 3.735
Height : 10.786
Entry
ampl
0
2
4
6
8
10
12
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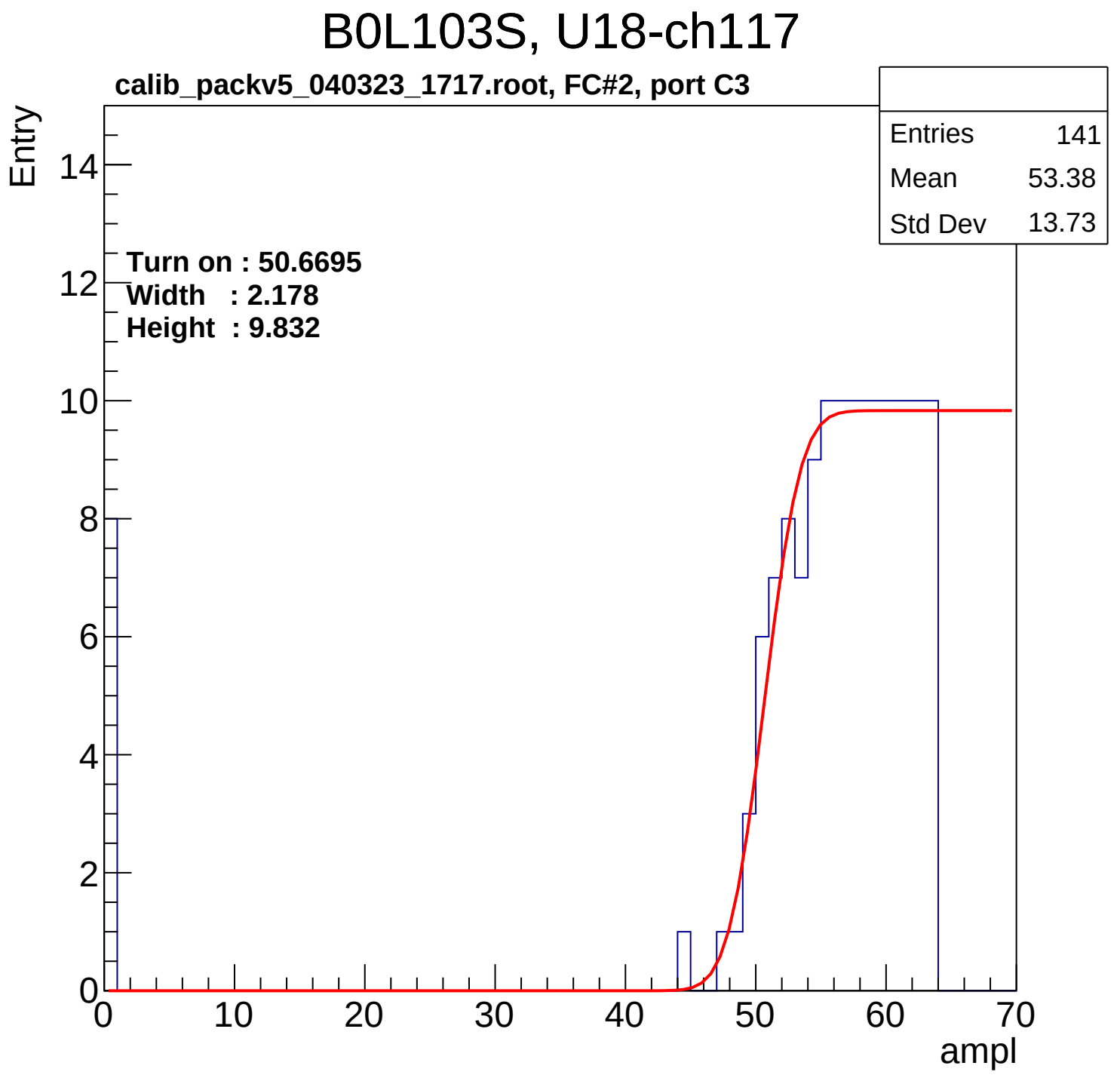
B0L103S, U18-ch117
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 53.38
Std Dev 13.73
Turn on : 50.6695
Width : 2.178
Height : 9.832
Entry
ampl
0
2
4
6
8
10
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0
10
20
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60
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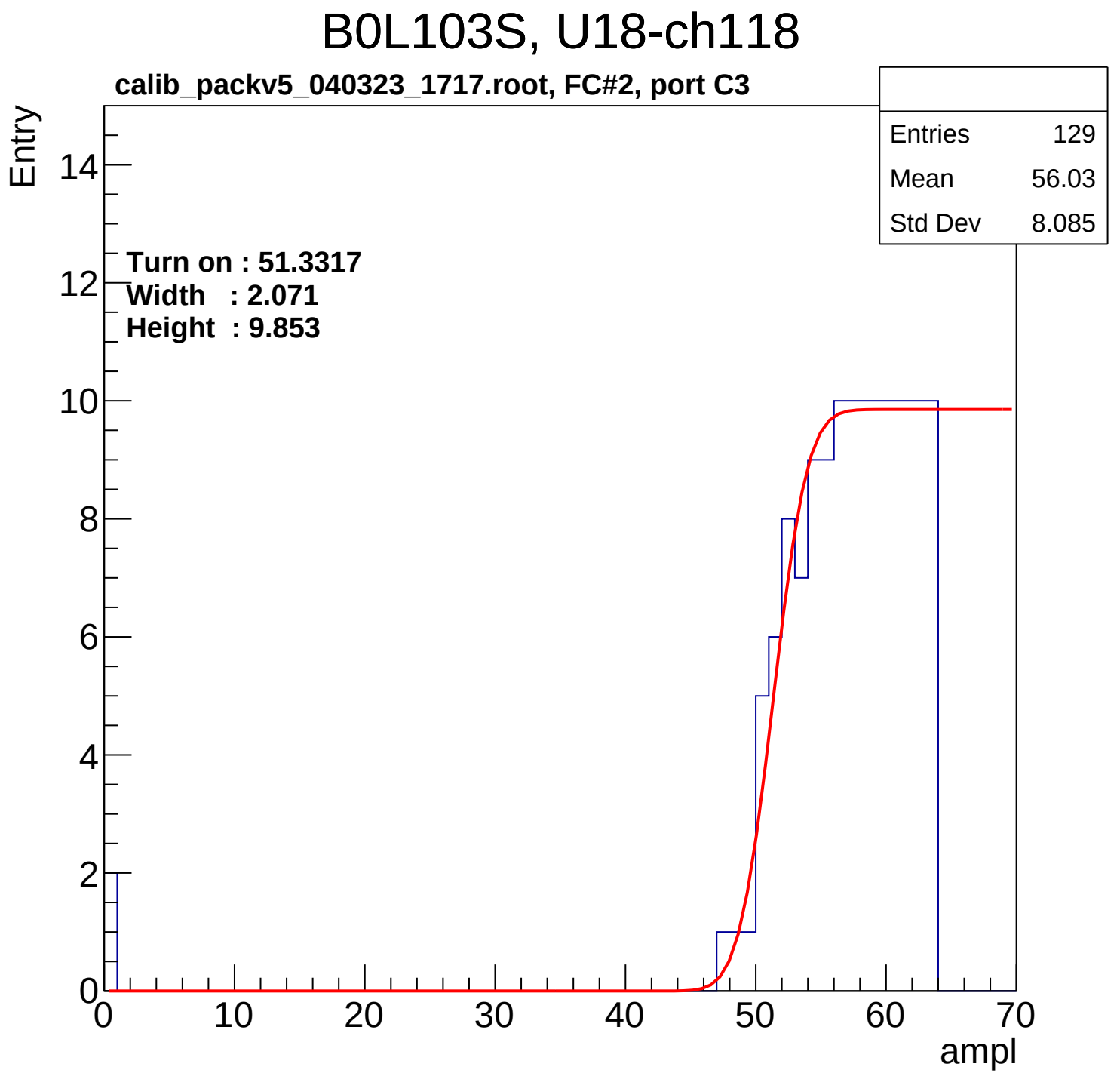
B0L103S, U18-ch118
calib_packv5_040323_1717.root, FC#2, port C3
Entries 129
Mean 56.03
Std Dev 8.085
Turn on : 51.3317
Width : 2.071
Height : 9.853
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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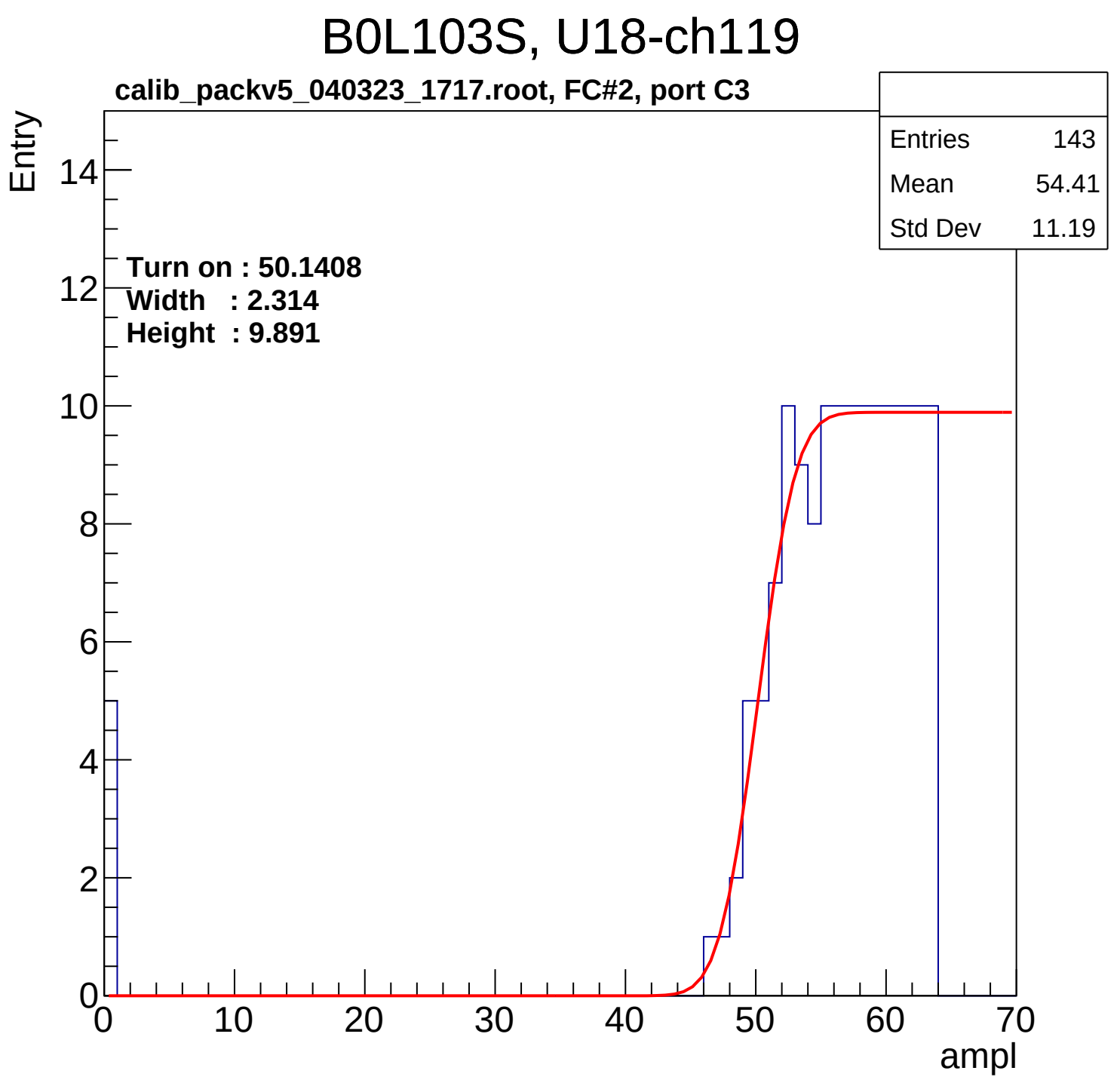
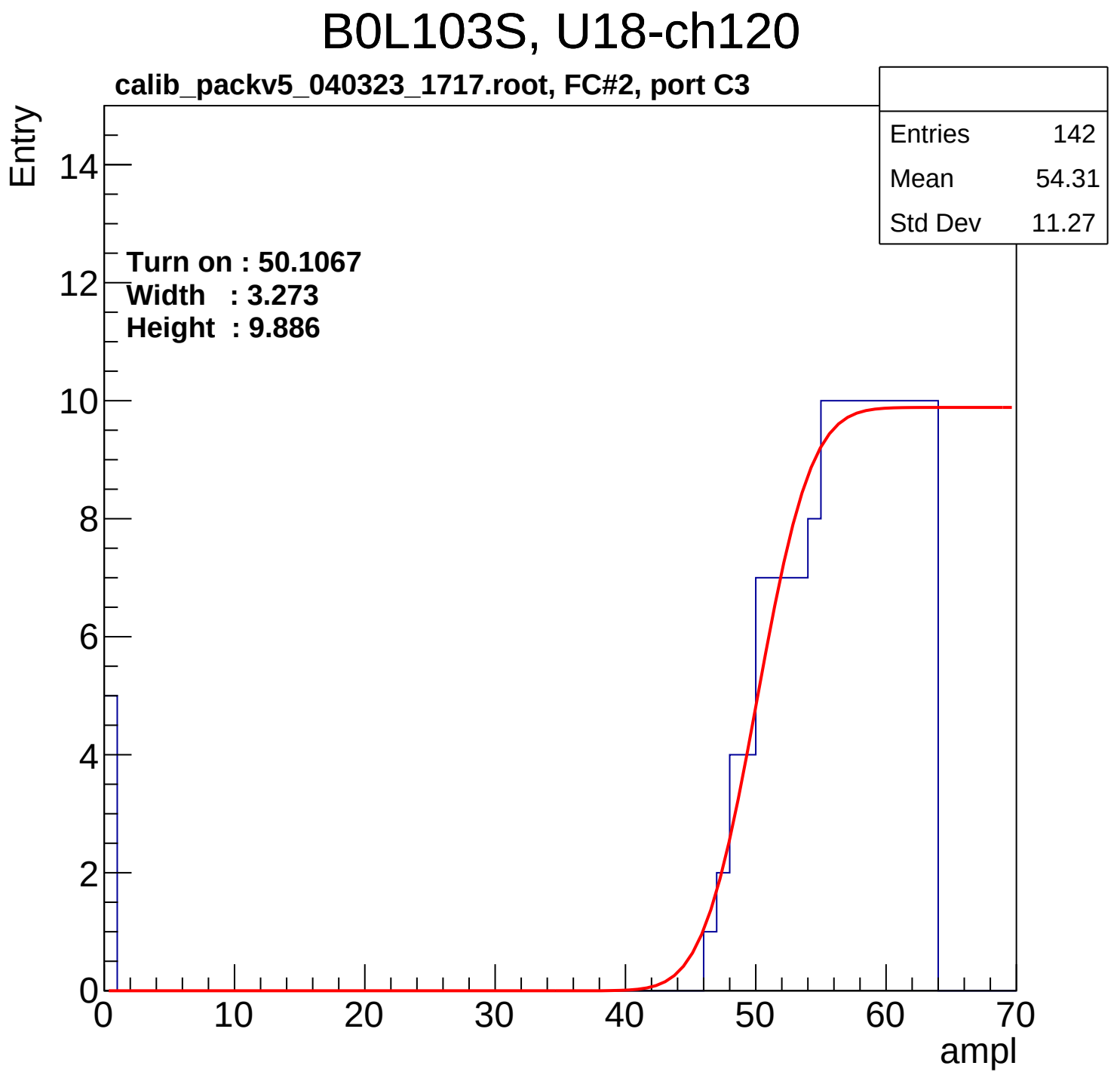

B0L103S, U18-ch119
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 54.41
Std Dev 11.19
Turn on : 50.1408
Width : 2.314
Height : 9.891
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U18-ch120
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 54.31
Std Dev 11.27
Turn on : 50.1067
Width : 3.273
Height : 9.886
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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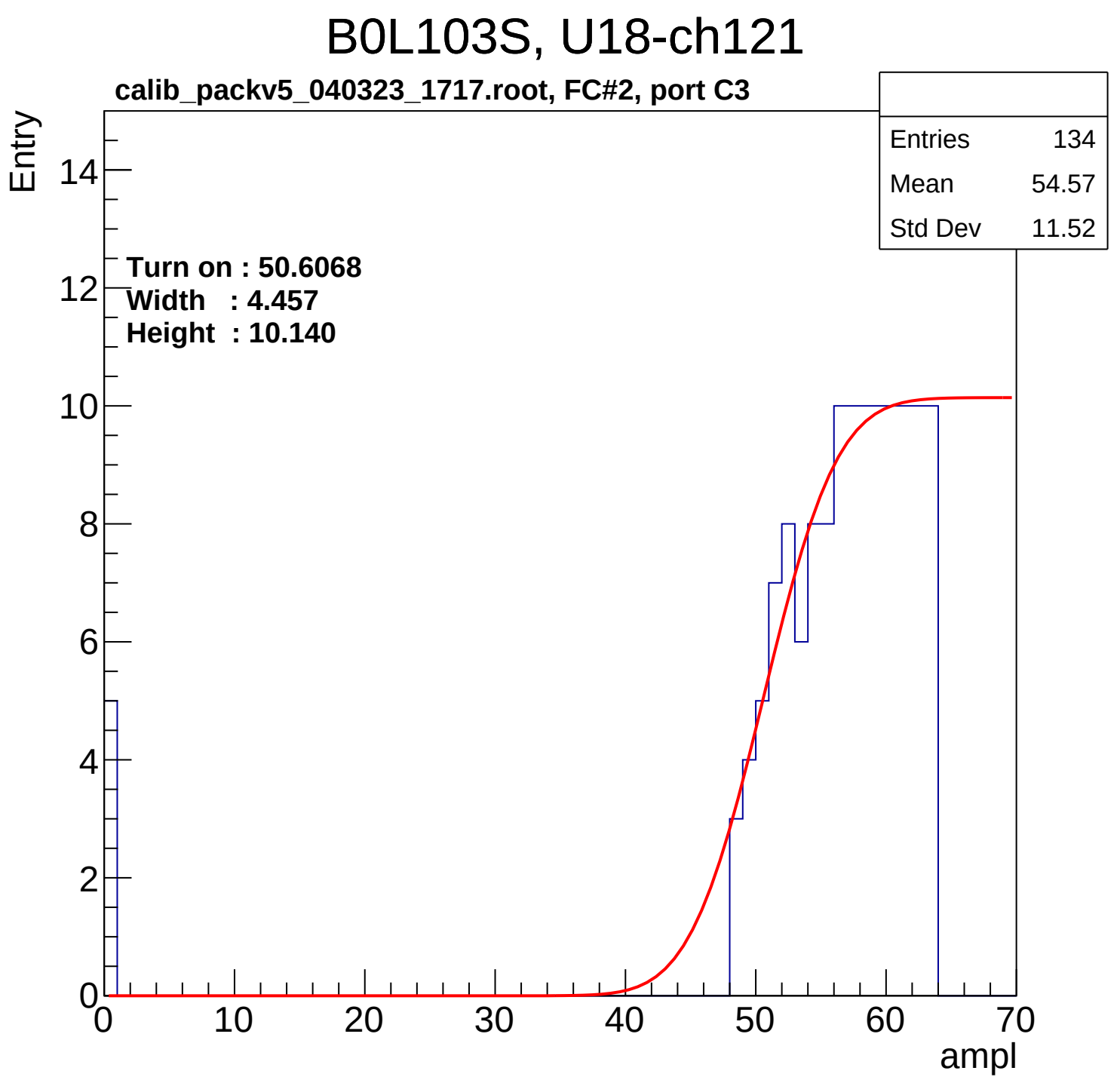
B0L103S, U18-ch121
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 54.57
Std Dev 11.52
Turn on : 50.6068
Width : 4.457
Height : 10.140
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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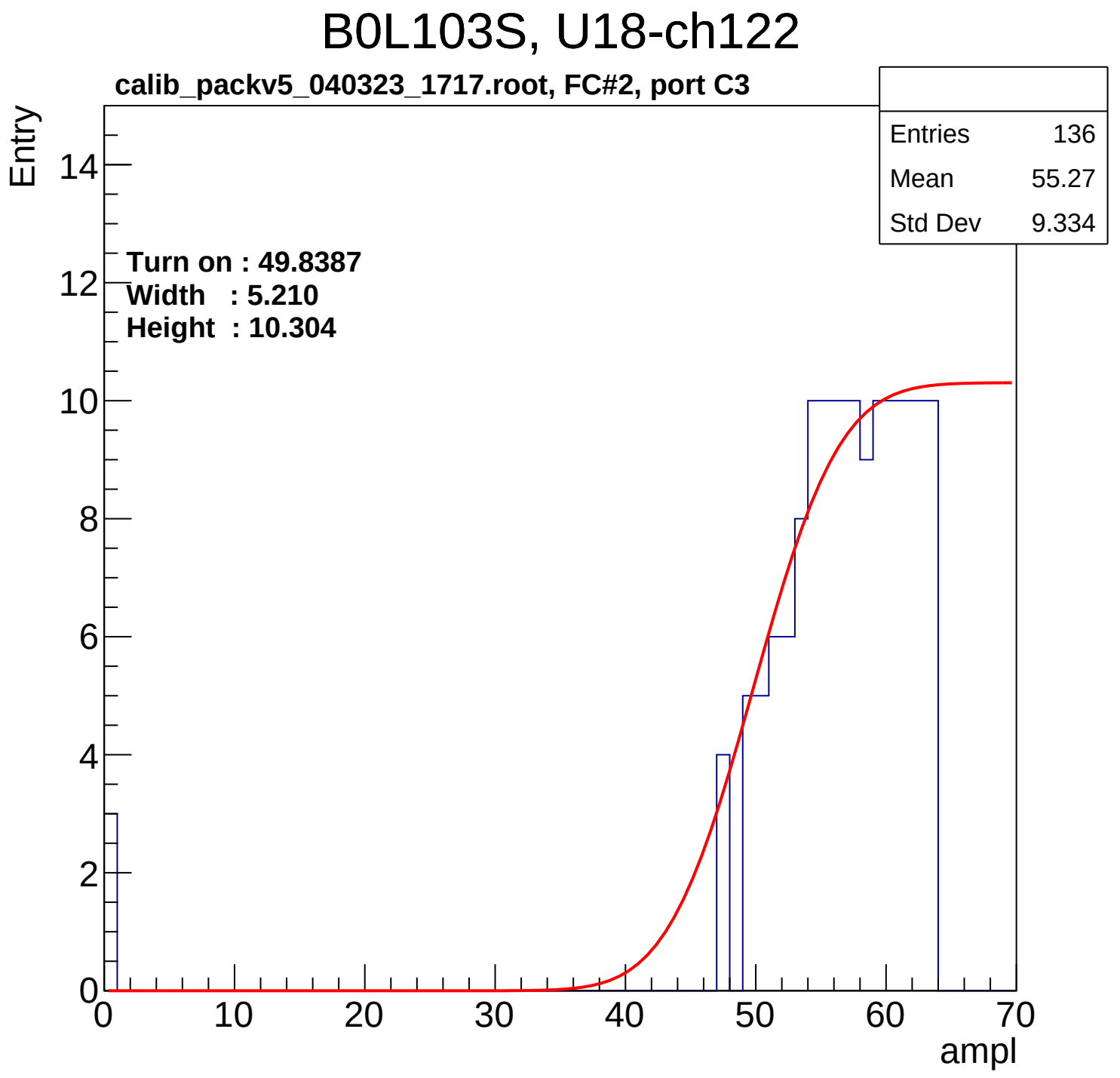
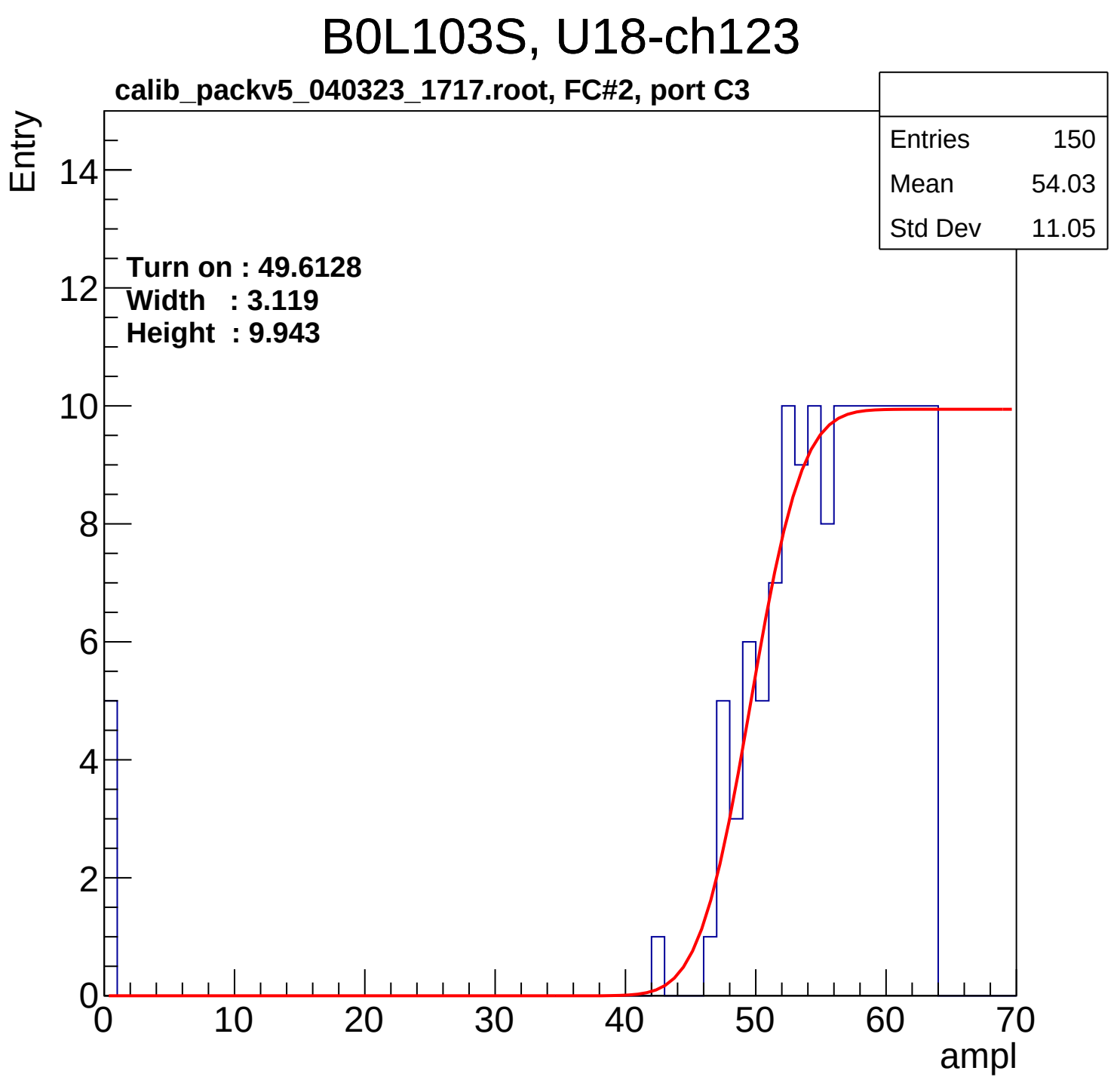
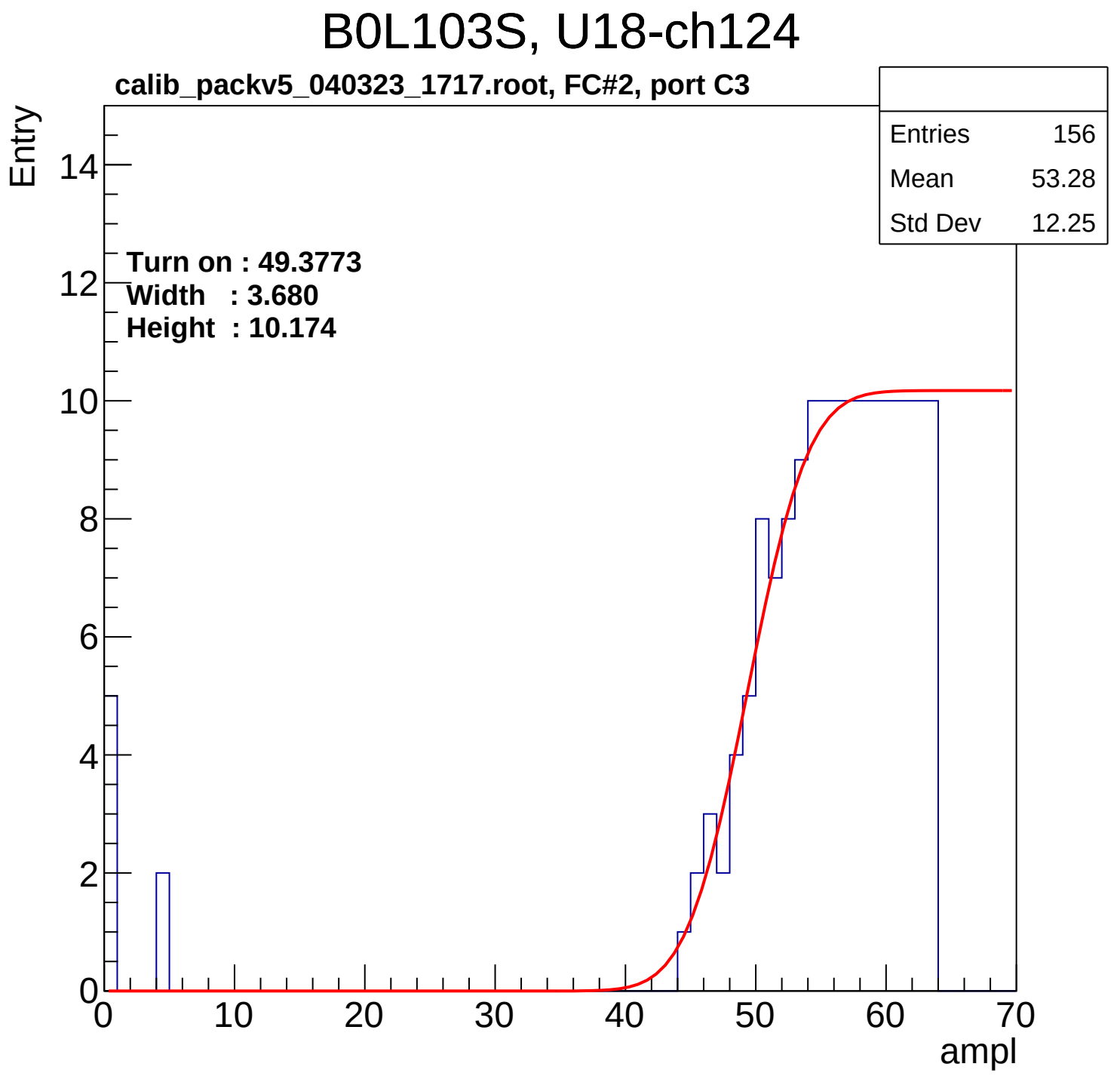

B0L103S, U18-ch122
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 55.27
Std Dev 9.334
Turn on : 49.8387
Width : 5.210
Height : 10.304
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U18-ch123
calib_packv5_040323_1717.root, FC#2, port C3
Entries 150
Mean 54.03
Std Dev 11.05
Turn on : 49.6128
Width : 3.119
Height : 9.943
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U18-ch124
calib_packv5_040323_1717.root, FC#2, port C3
Entries 156
Mean 53.28
Std Dev 12.25
Turn on : 49.3773
Width : 3.680
Height : 10.174
Entry
ampl
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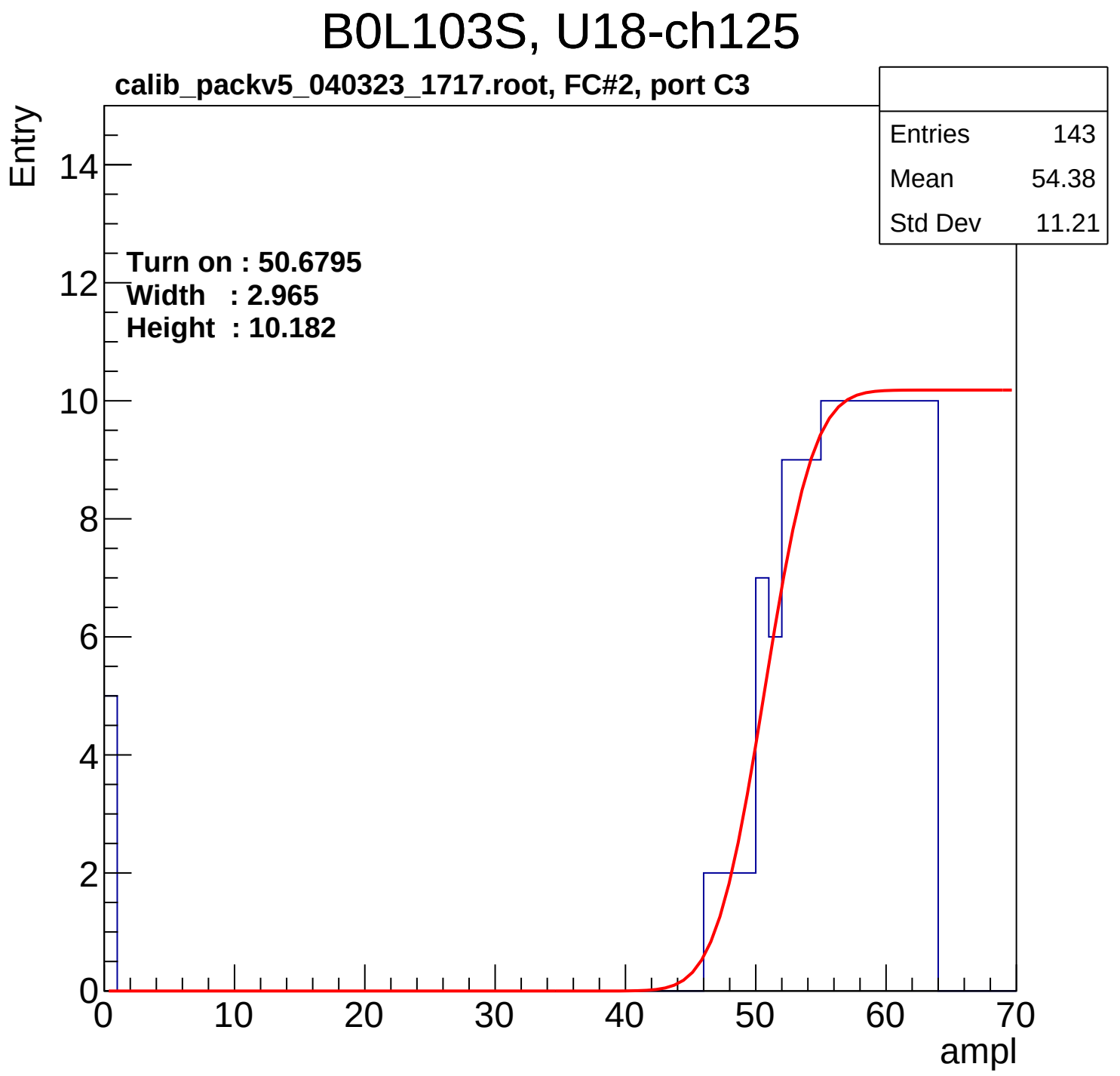
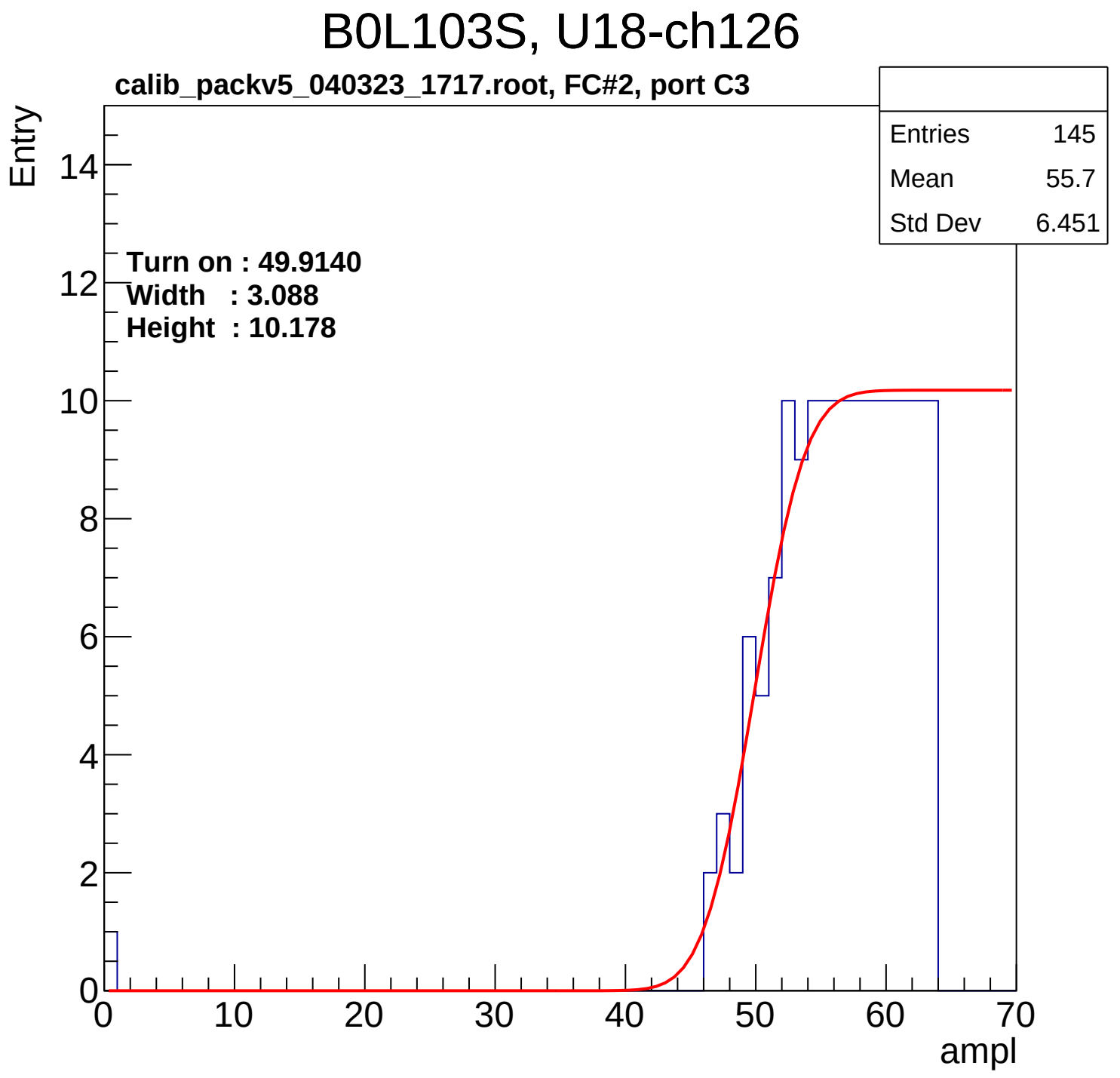
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U18-ch125
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 54.38
Std Dev 11.21
Turn on : 50.6795
Width : 2.965
Height : 10.182
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U18-ch126
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 55.7
Std Dev 6.451
Turn on : 49.9140
Width : 3.088
Height : 10.178
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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40
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60
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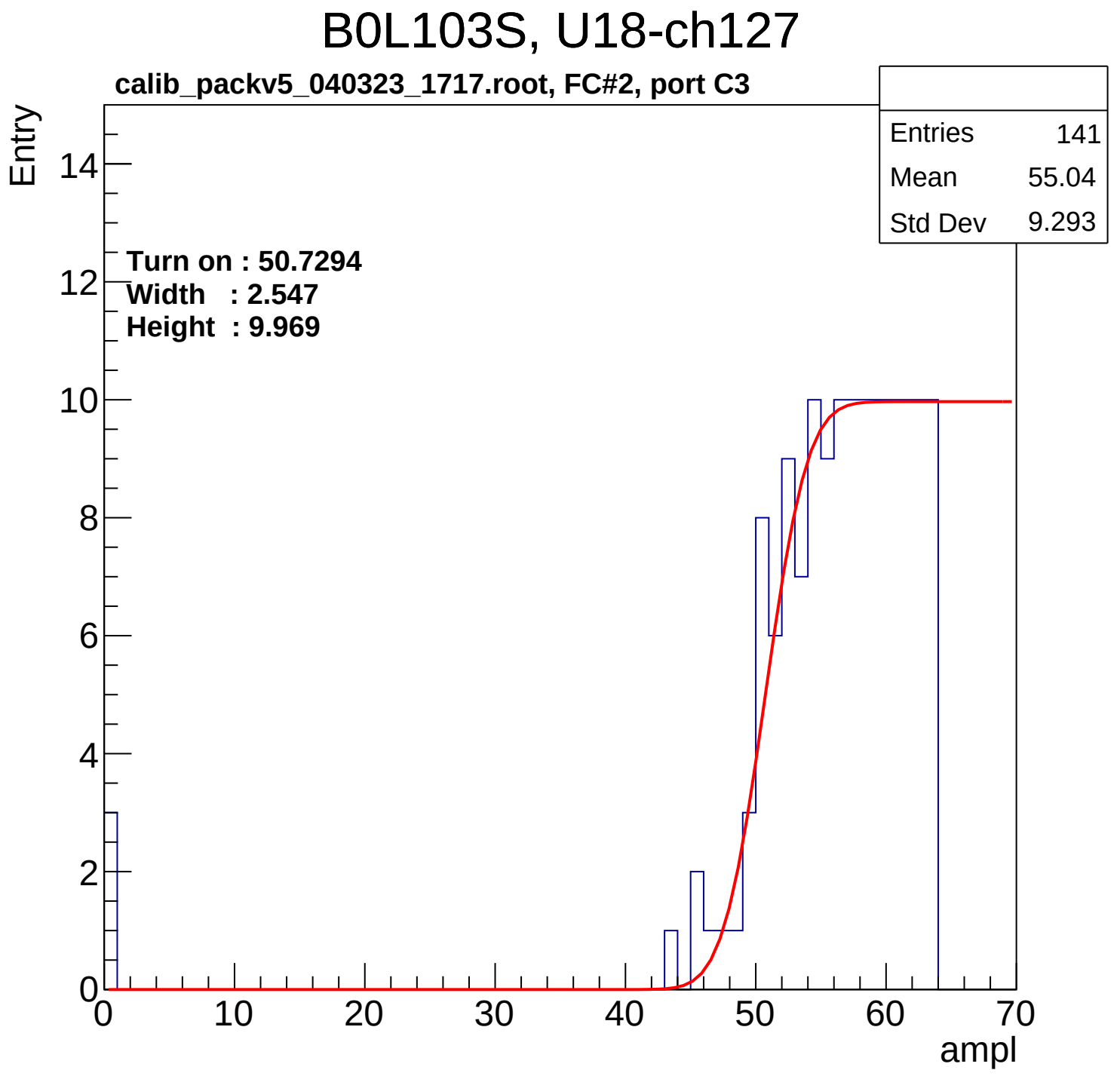
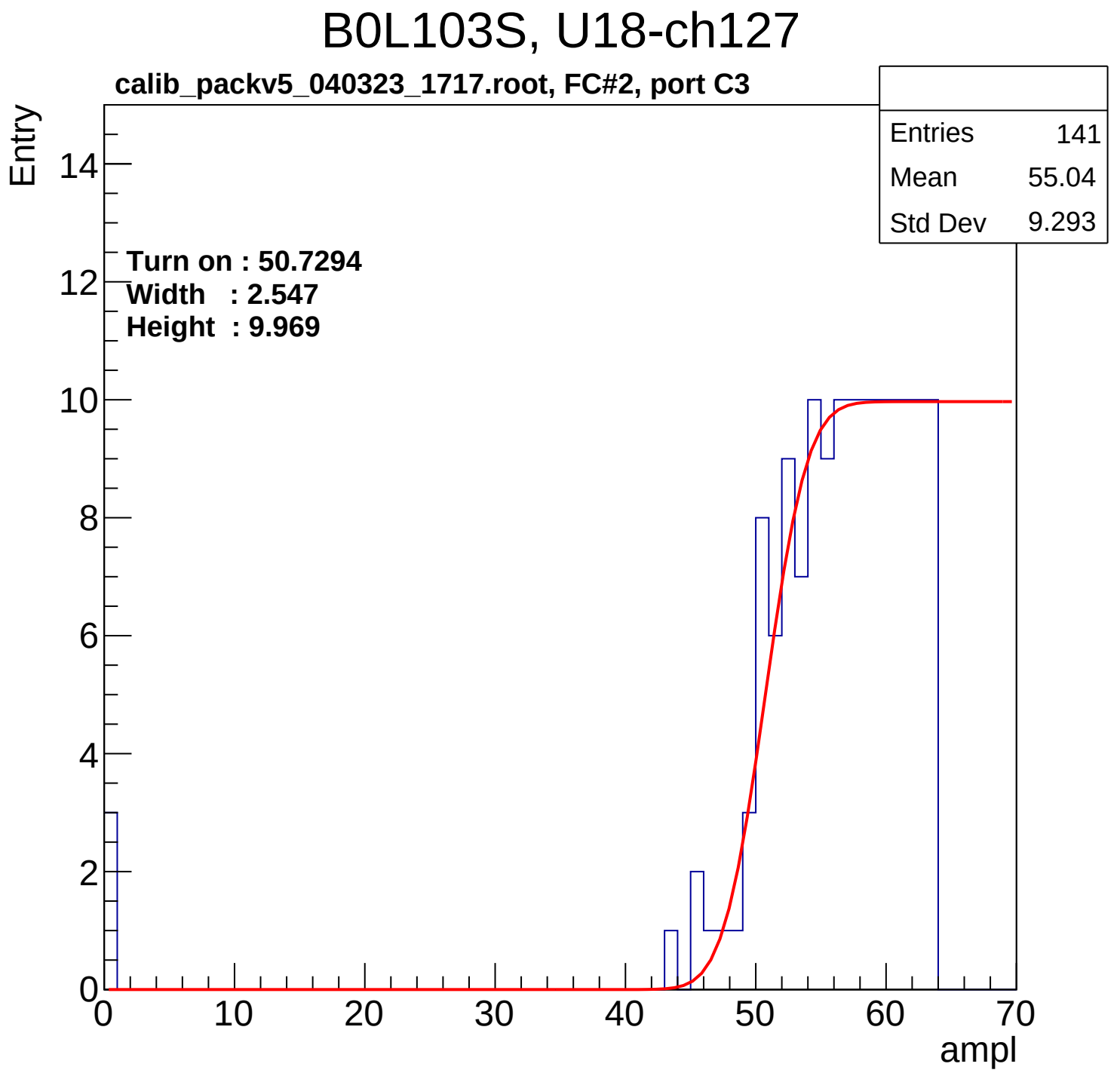

B0L103S, U18-ch127
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 55.04
Std Dev 9.293
Turn on : 50.7294
Width : 2.547
Height : 9.969
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U18-ch127
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 55.04
Std Dev 9.293
Turn on : 50.7294
Width : 2.547
Height : 9.969
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70