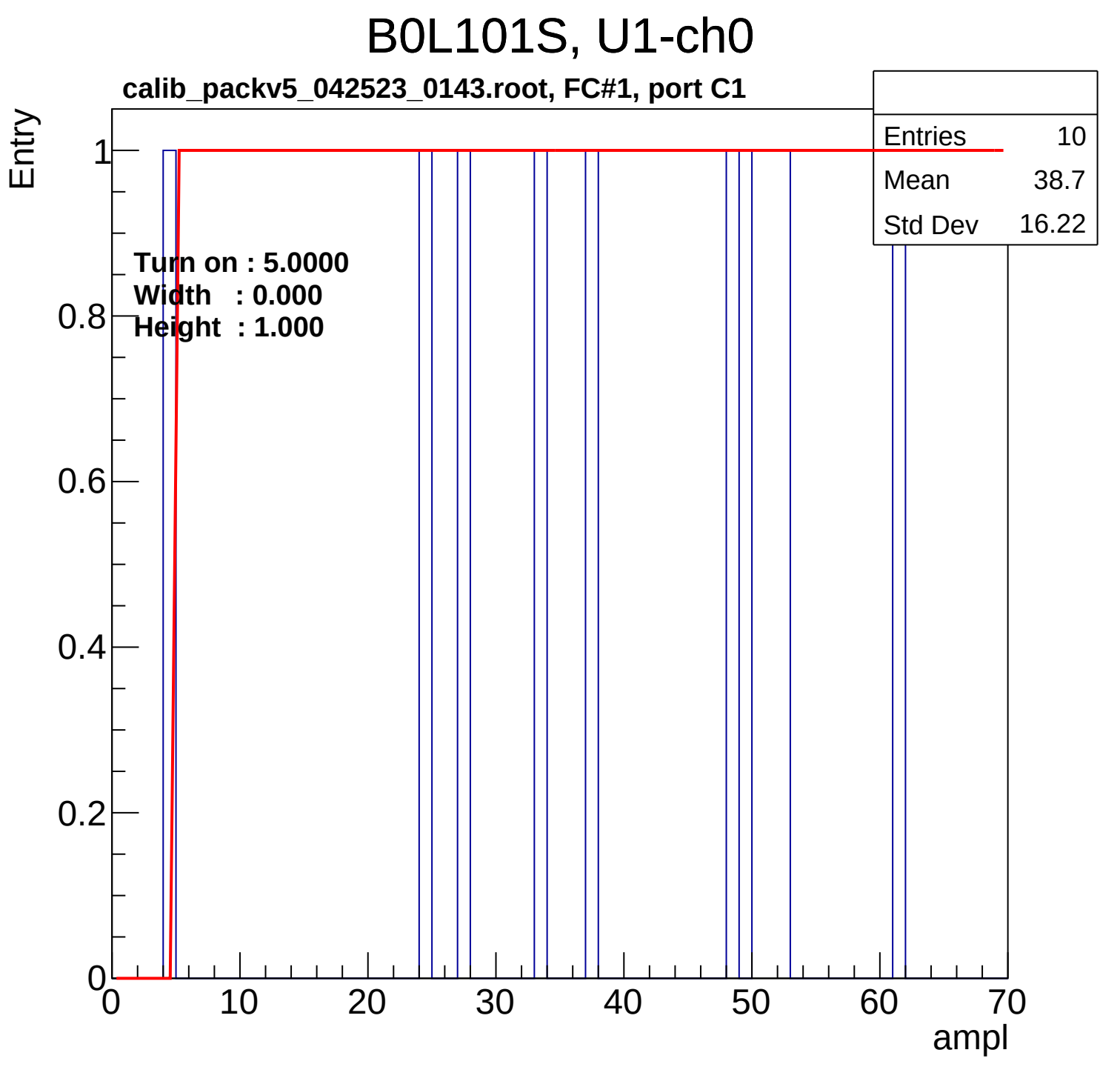
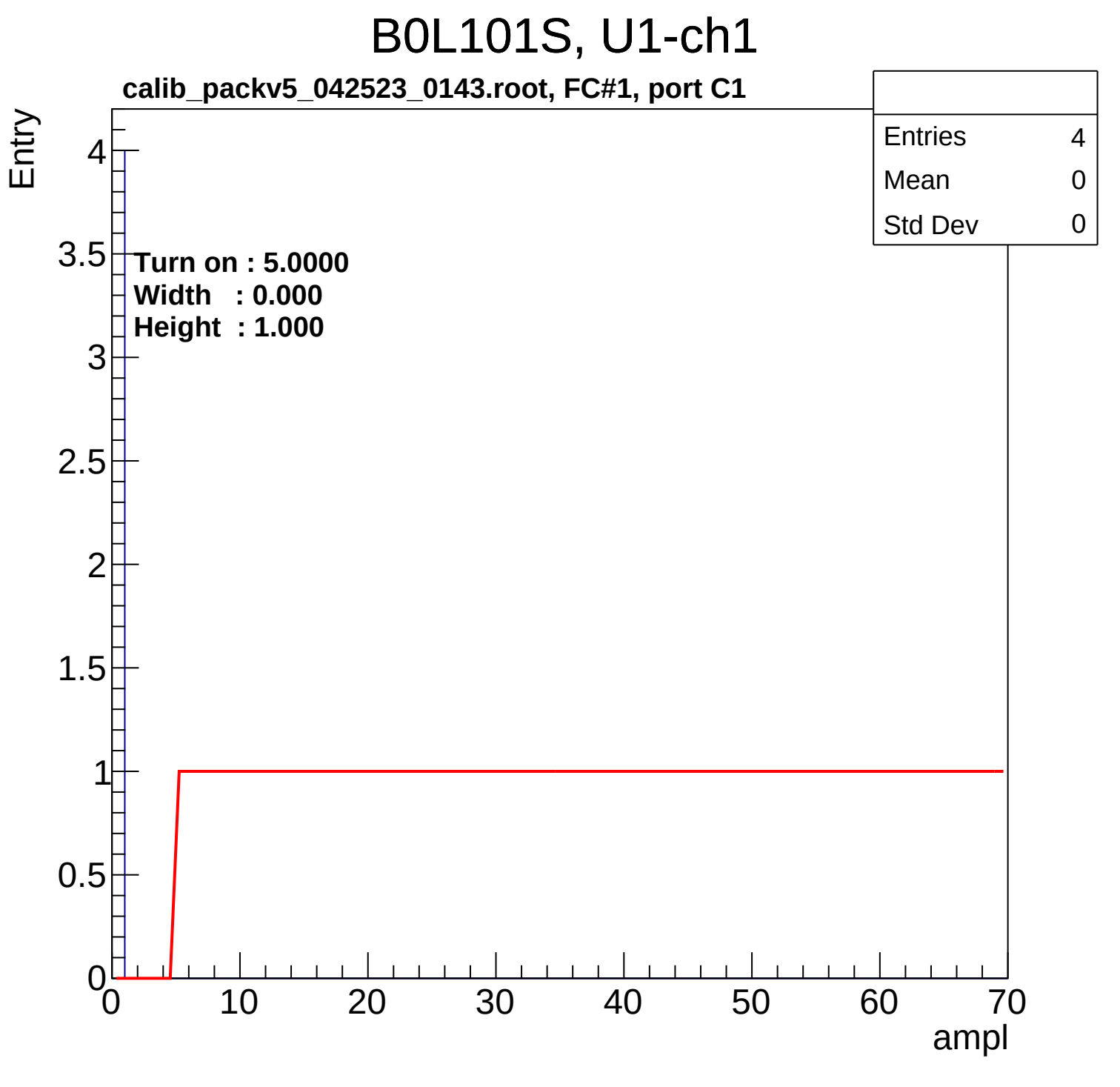
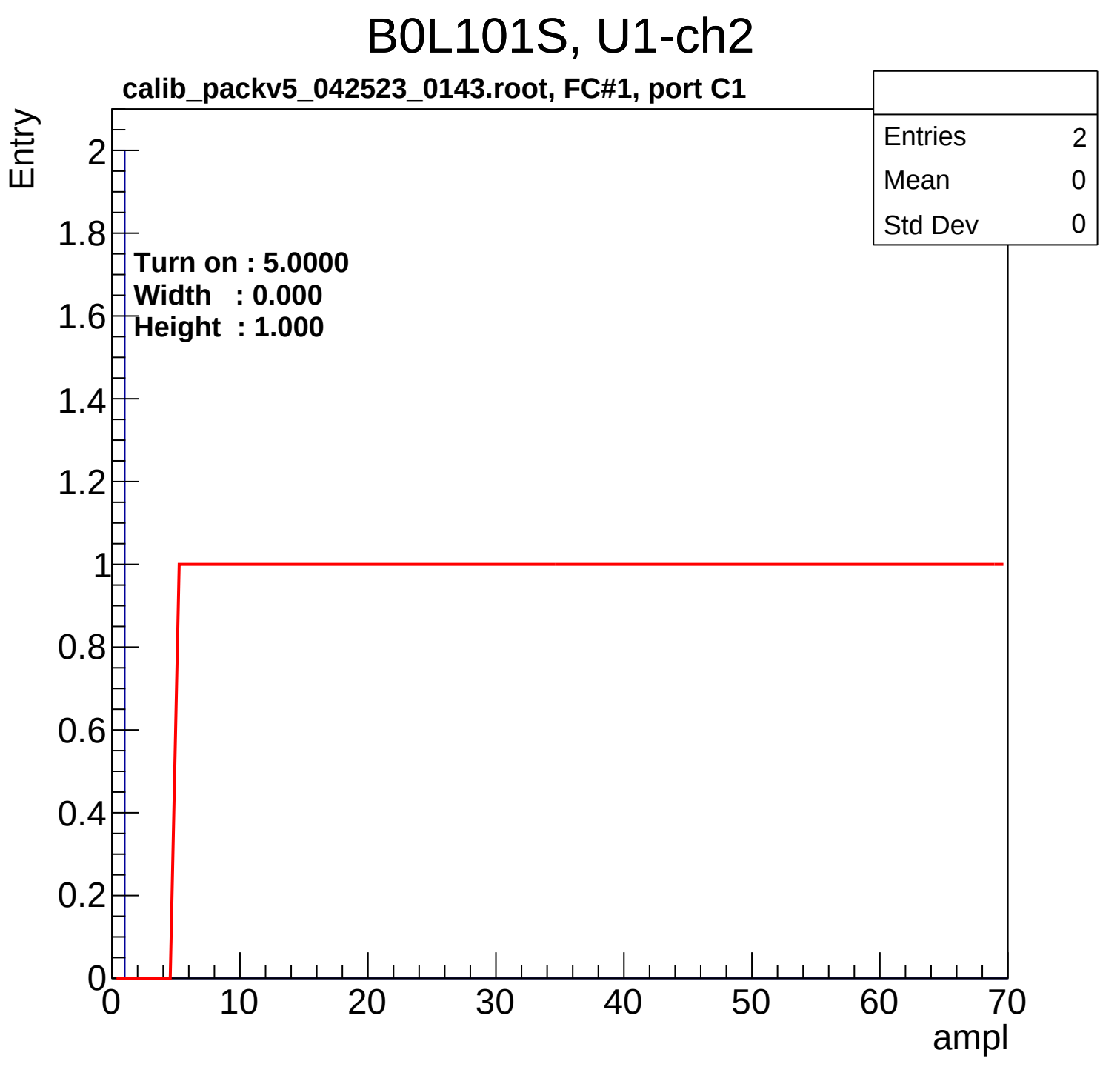
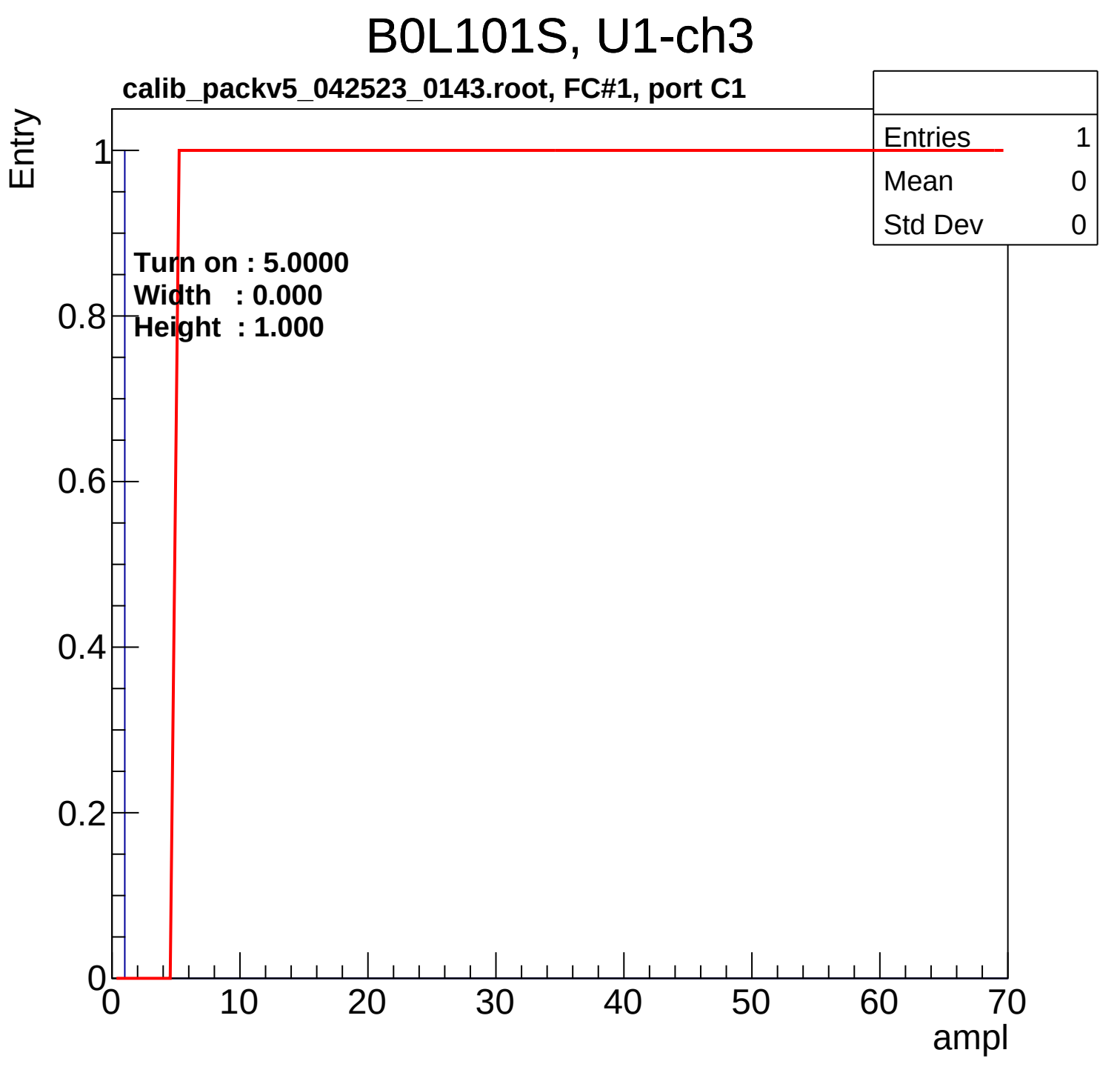
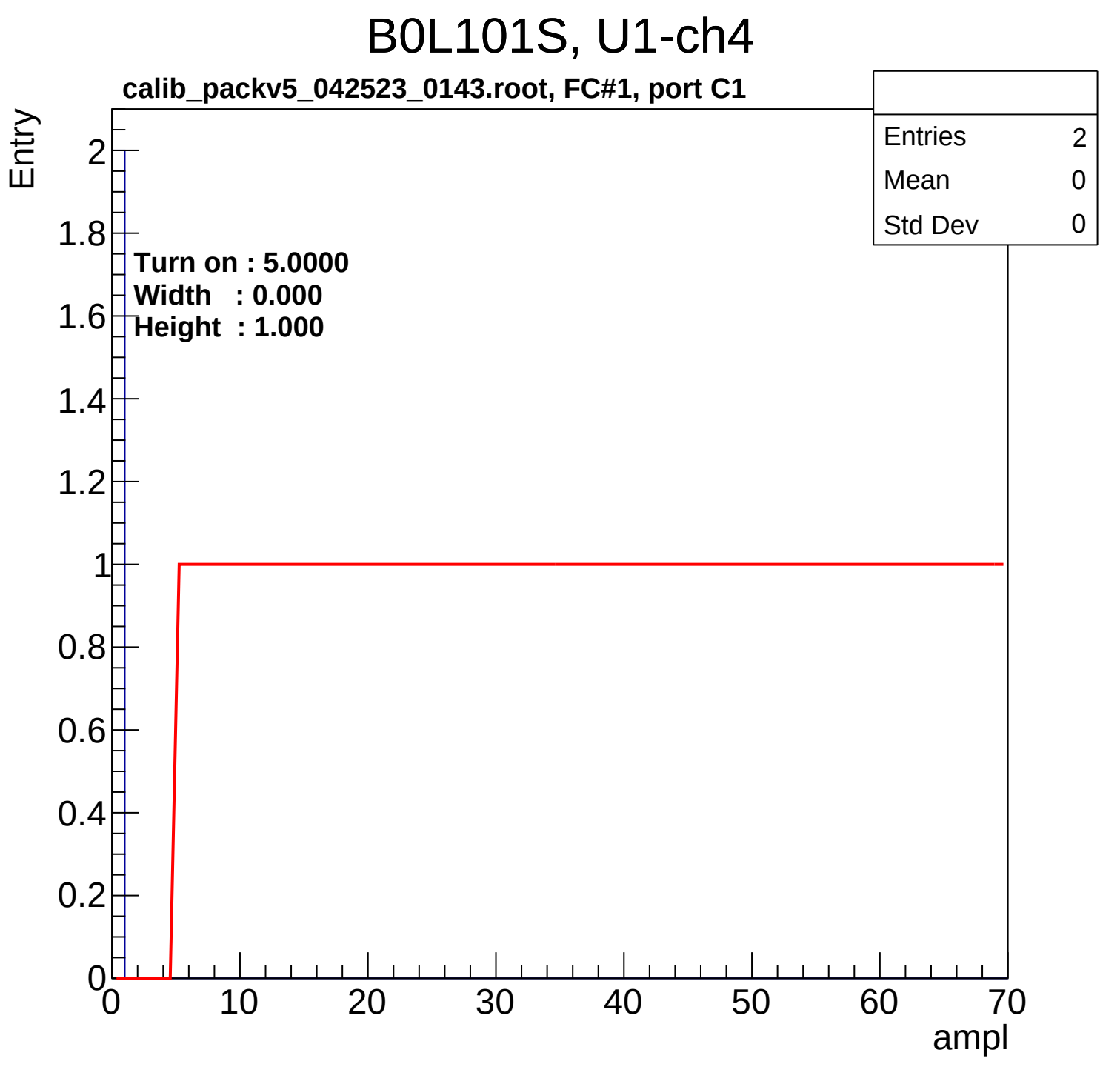
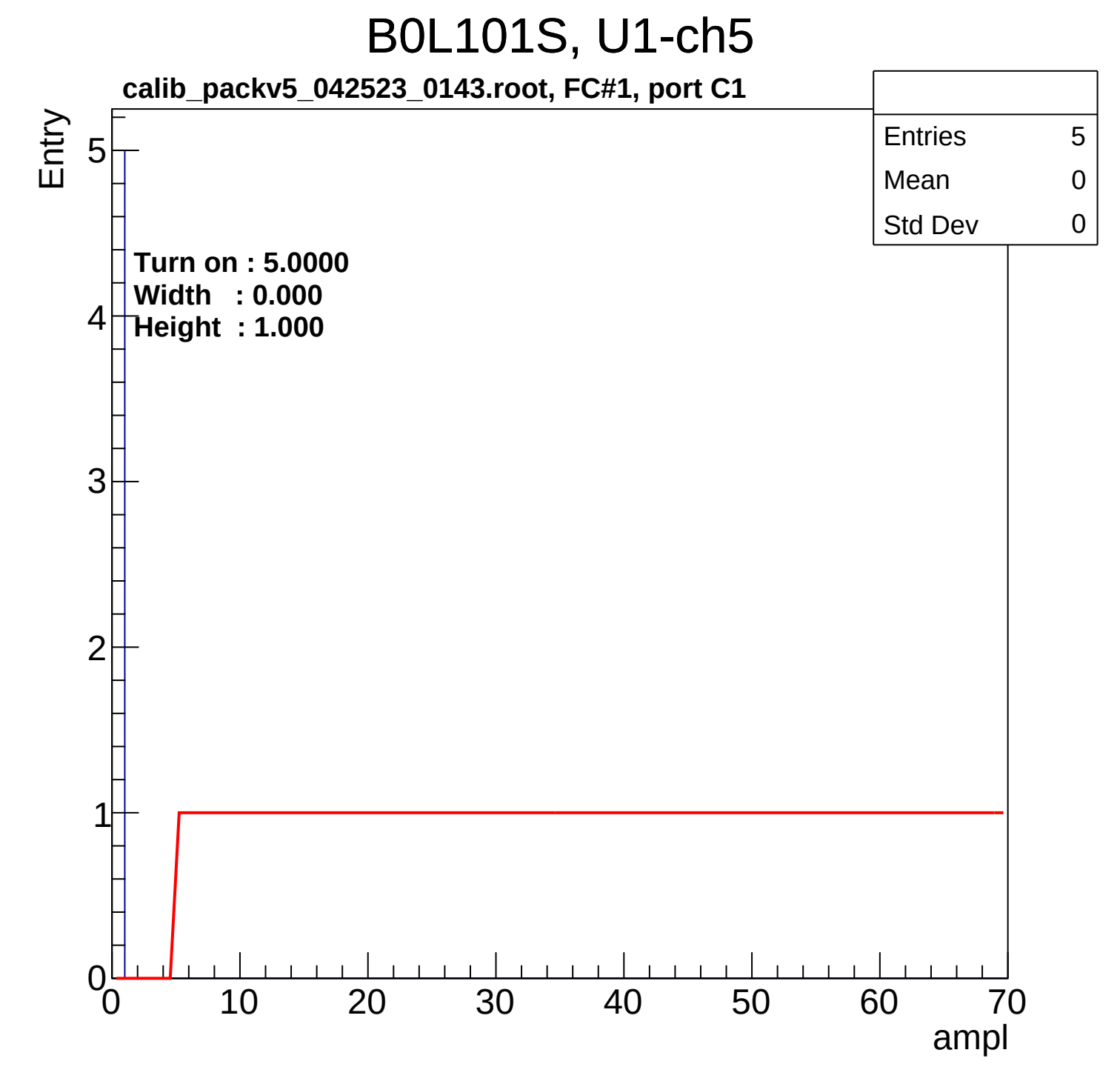

B0L101S, U1-ch0
calib_packv5_042523_0143.root, FC#1, port C1
Entries 10
Mean 38.7
Std Dev 16.22
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

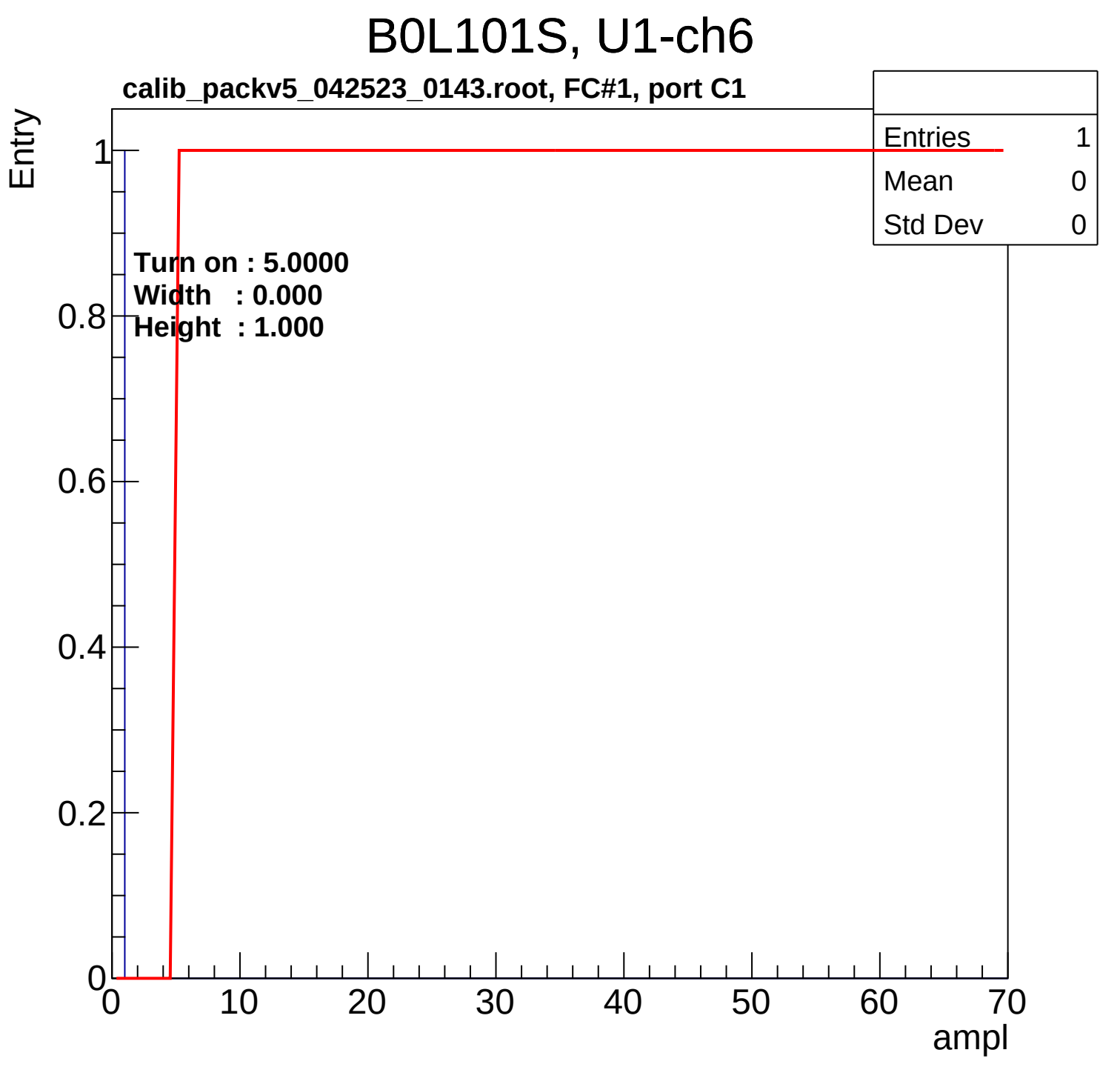

B0L101S, U1-ch1
calib_packv5_042523_0143.root, FC#1, port C1
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

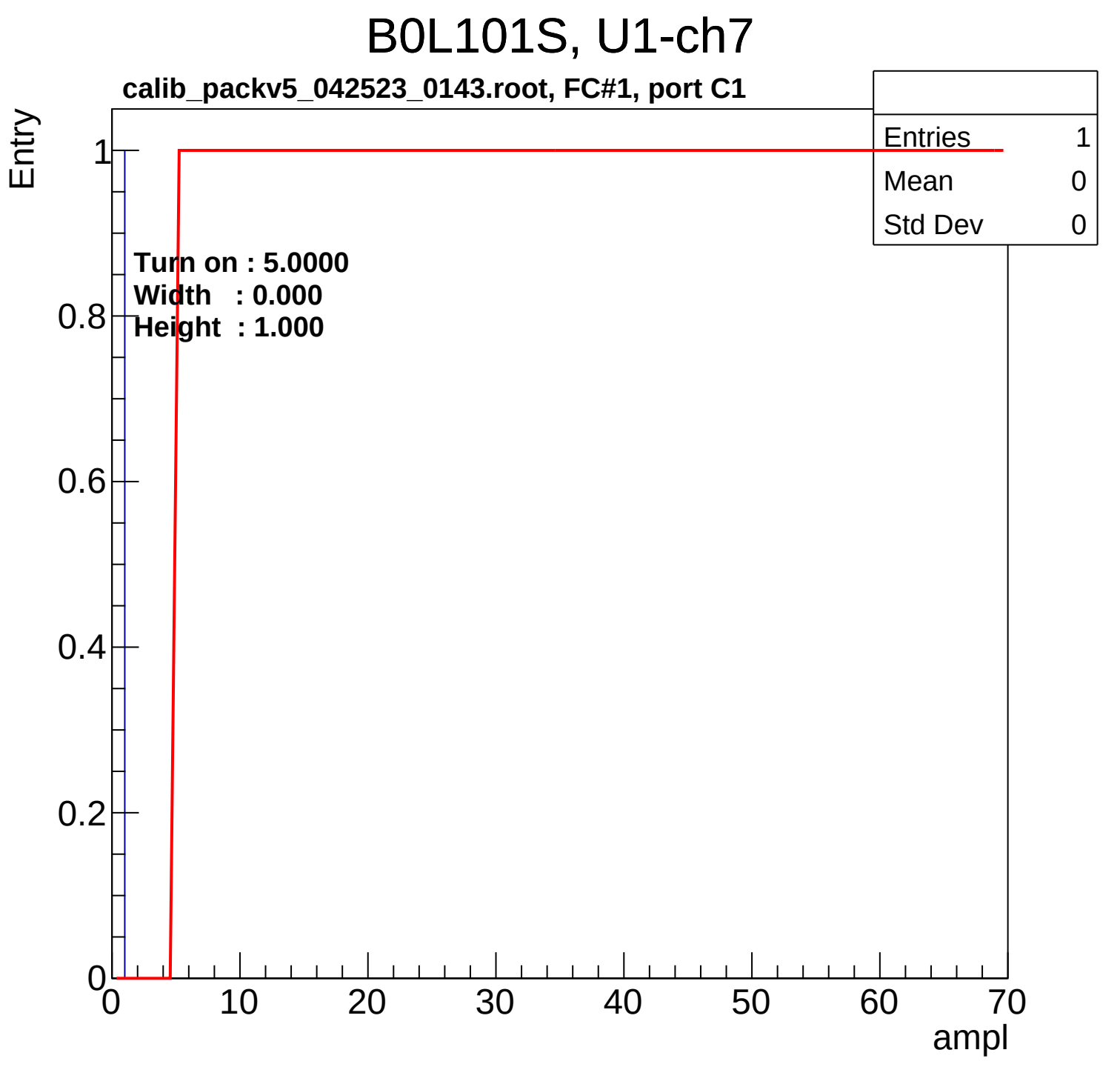

B0L101S, U1-ch2
calib_packv5_042523_0143.root, FC#1, port C1
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

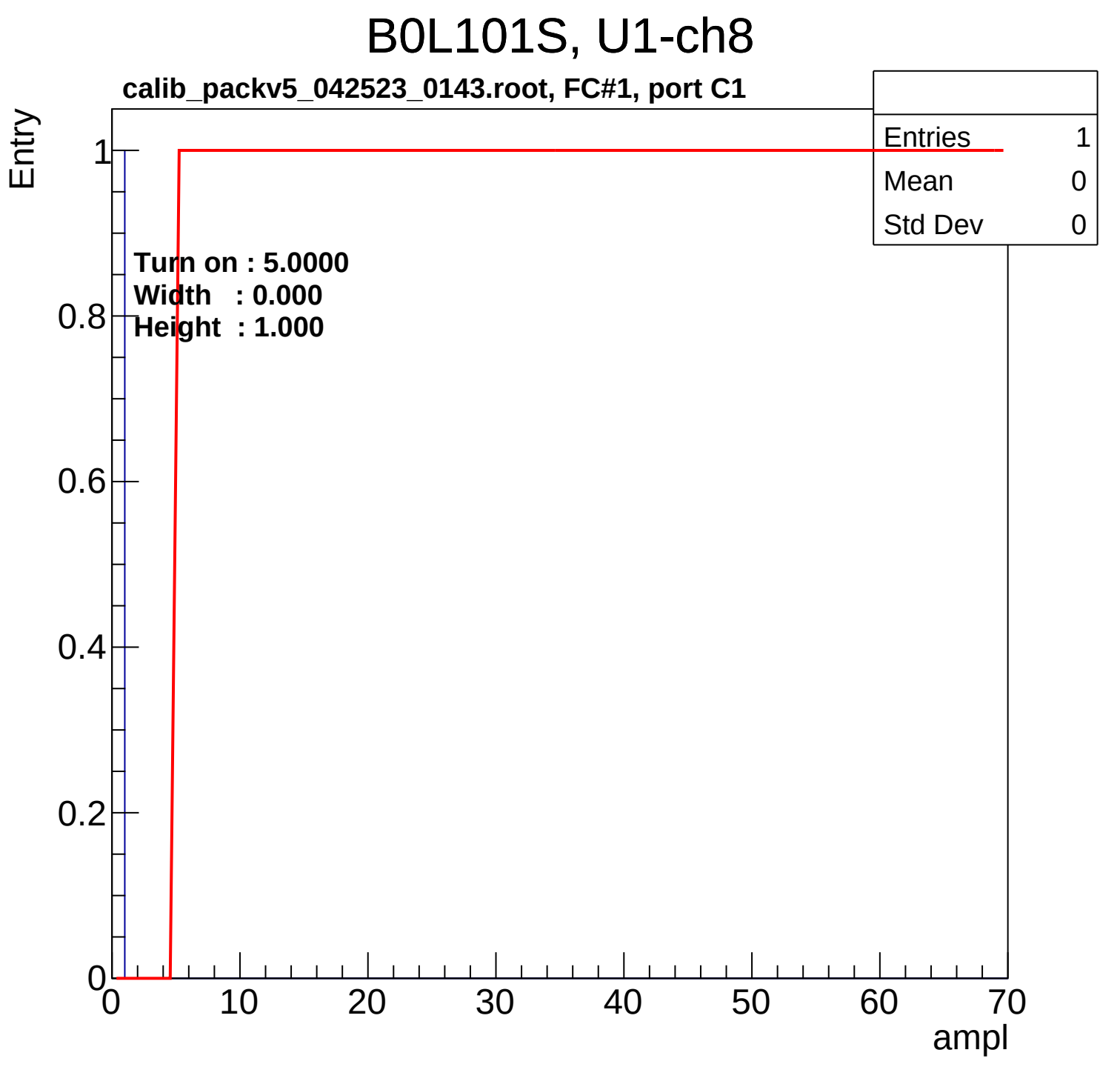

B0L101S, U1-ch3
calib_packv5_042523_0143.root, FC#1, port C1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

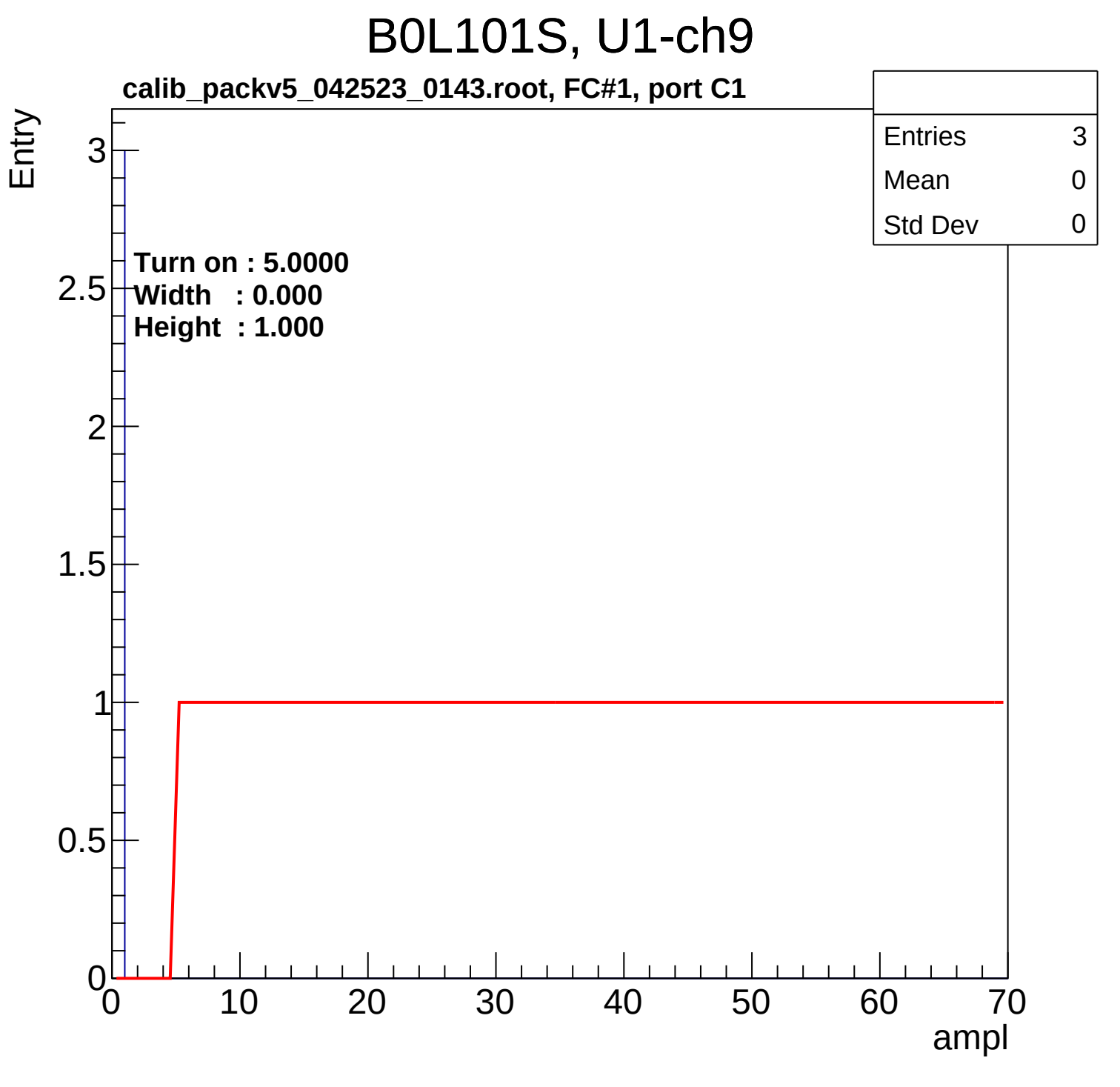

B0L101S, U1-ch4
calib_packv5_042523_0143.root, FC#1, port C1
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

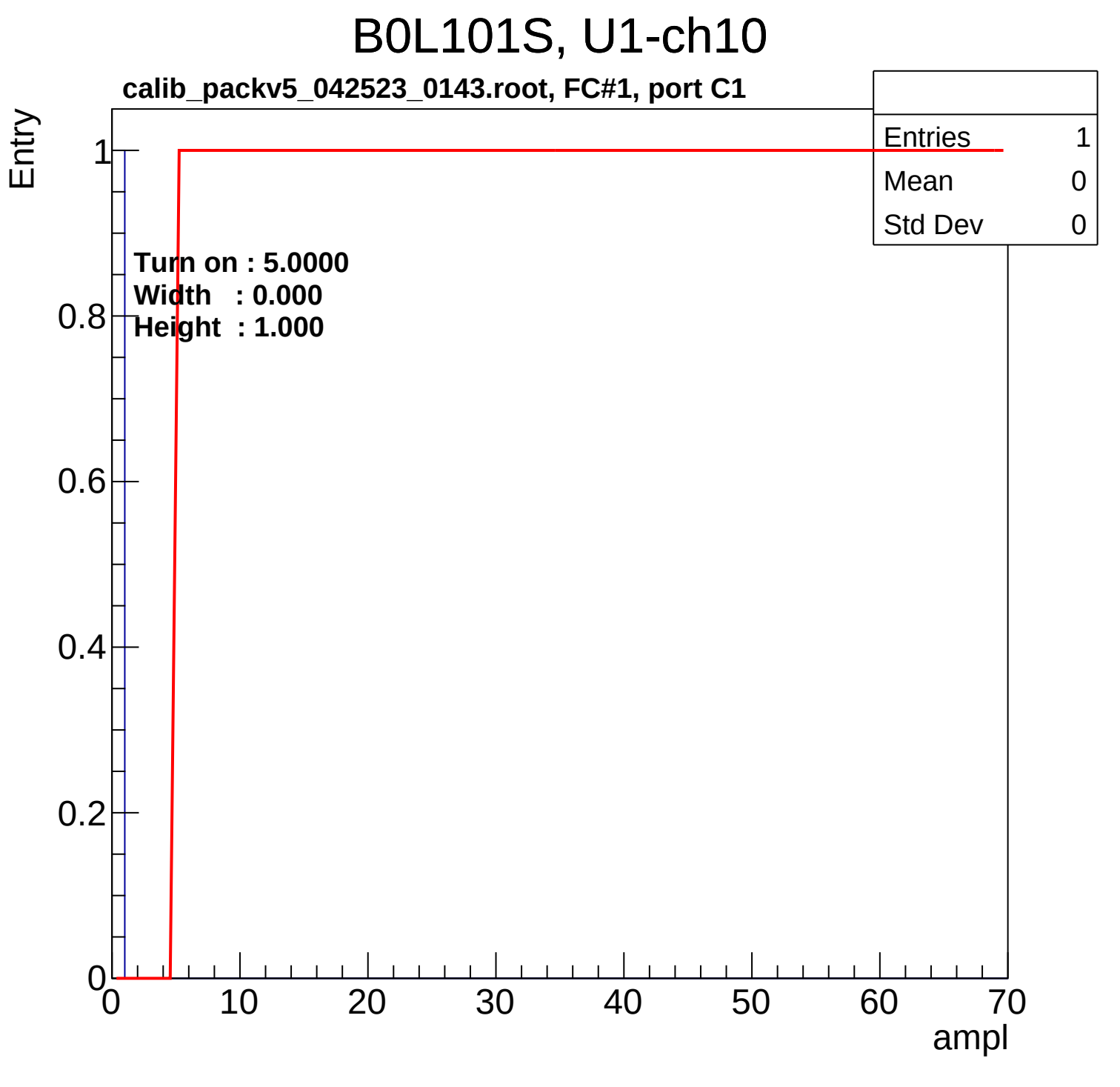

B0L101S, U1-ch5
calib_packv5_042523_0143.root, FC#1, port C1
Entries 5
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

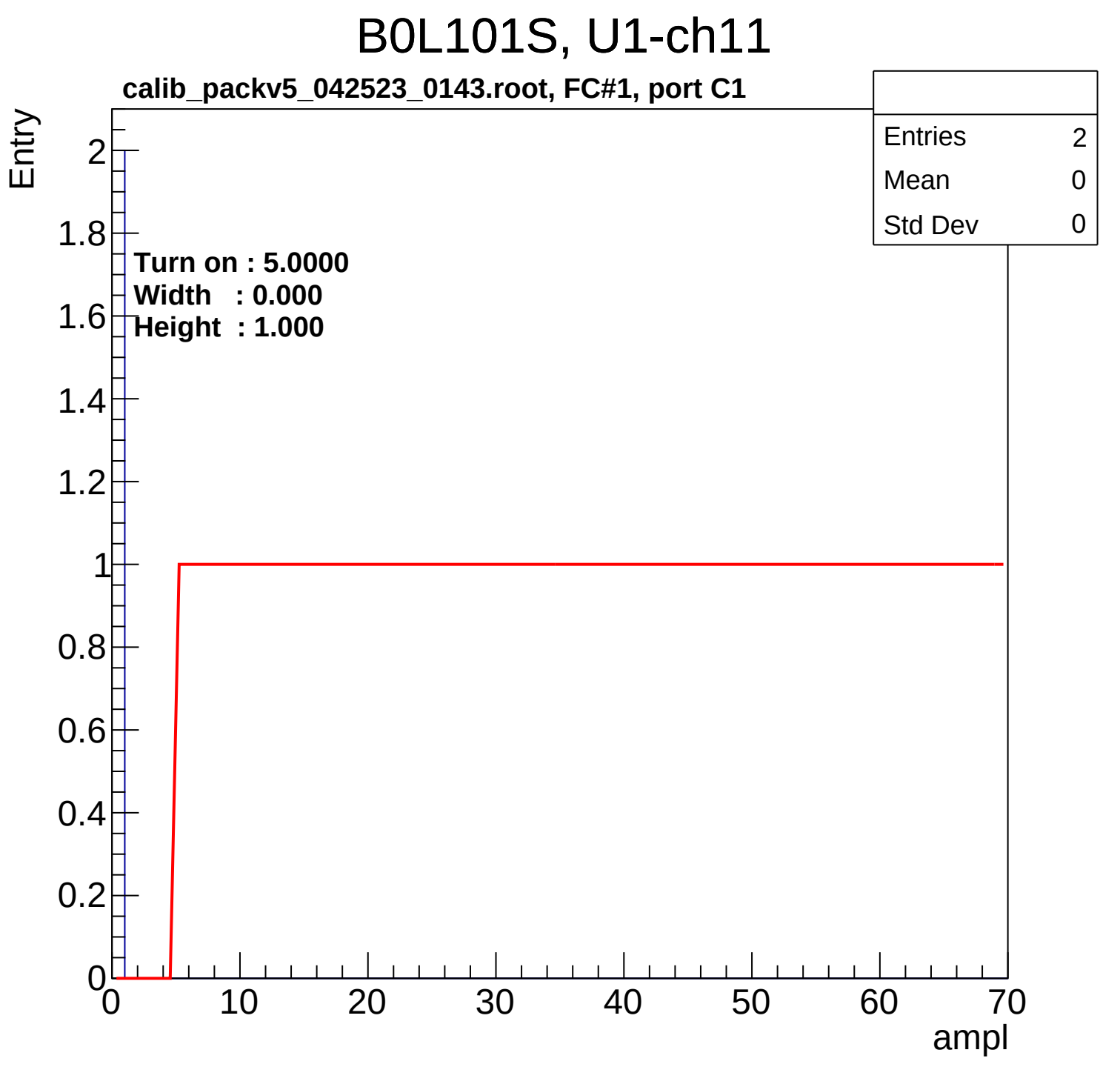

B0L101S, U1-ch6
calib_packv5_042523_0143.root, FC#1, port C1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

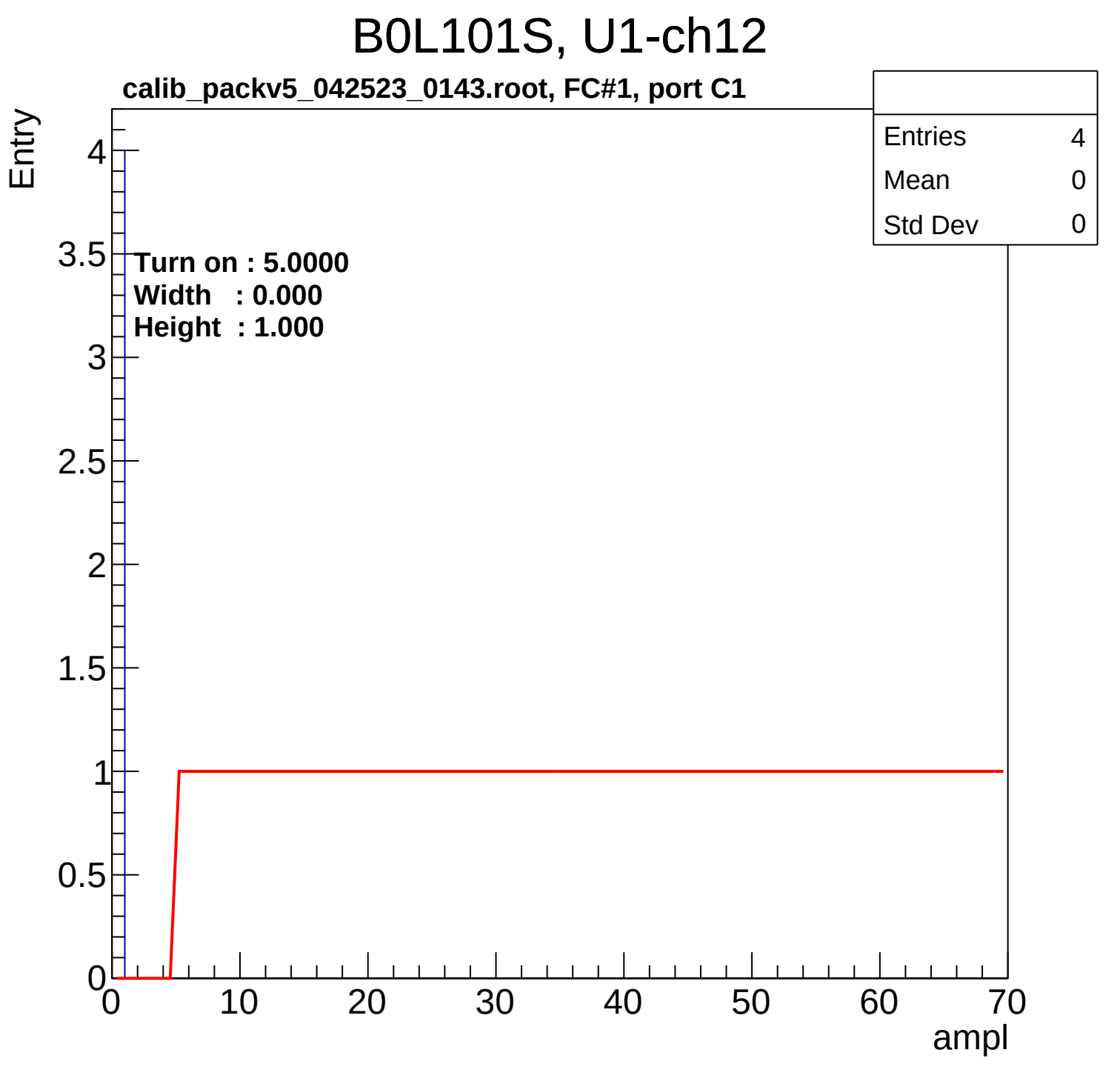

B0L101S, U1-ch7
calib_packv5_042523_0143.root, FC#1, port C1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

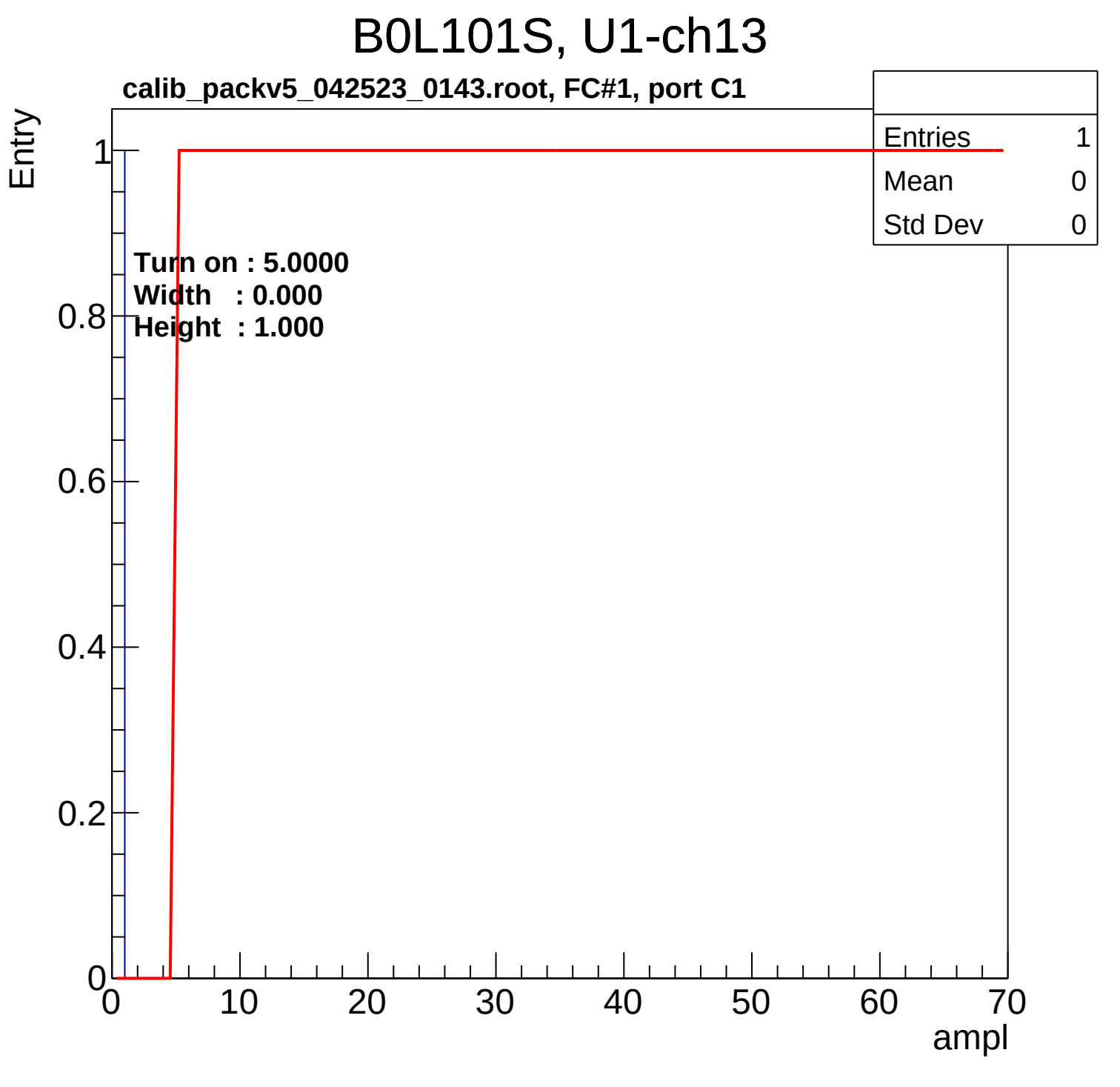

B0L101S, U1-ch8
calib_packv5_042523_0143.root, FC#1, port C1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

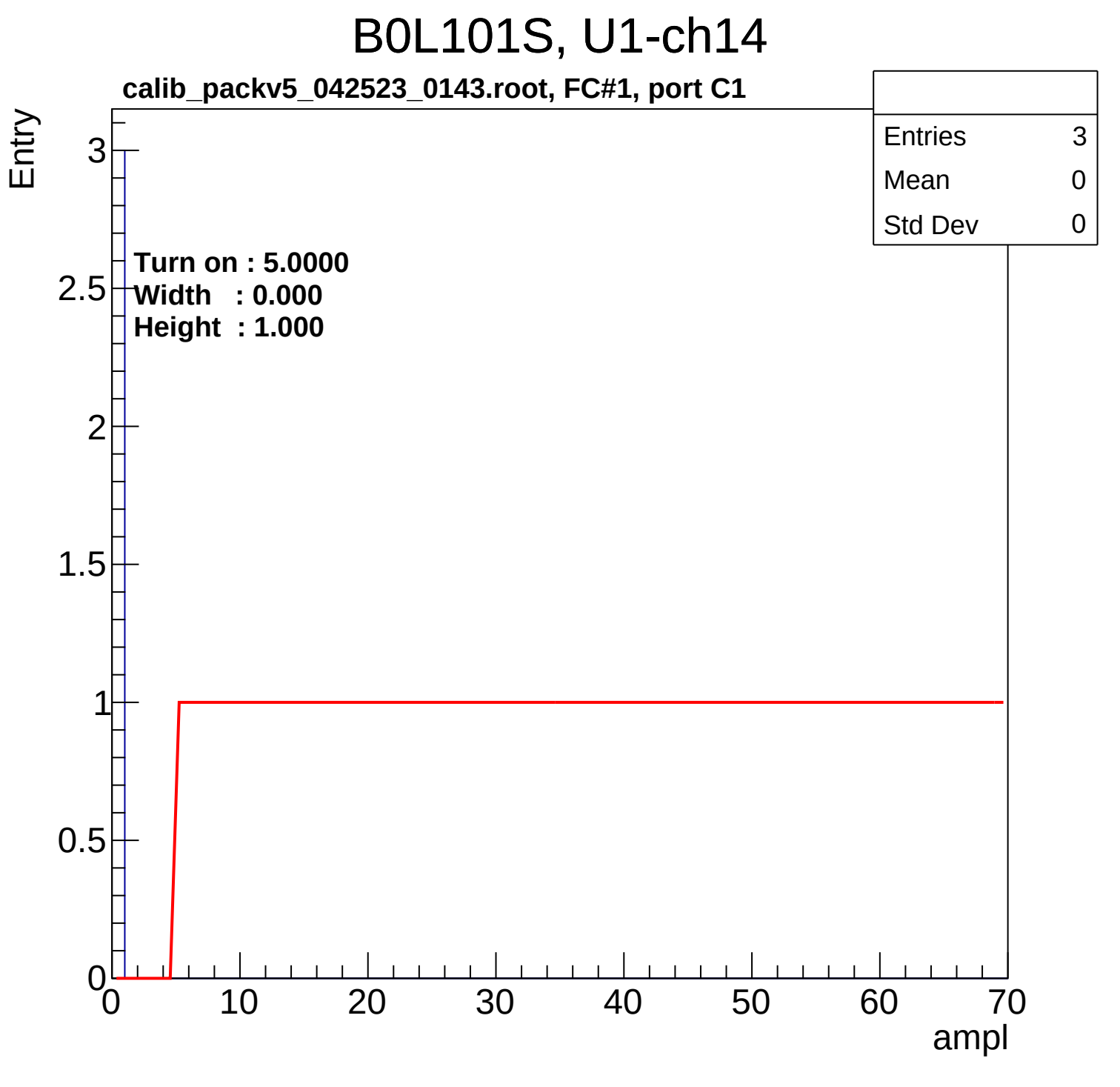

B0L101S, U1-ch9
calib_packv5_042523_0143.root, FC#1, port C1
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

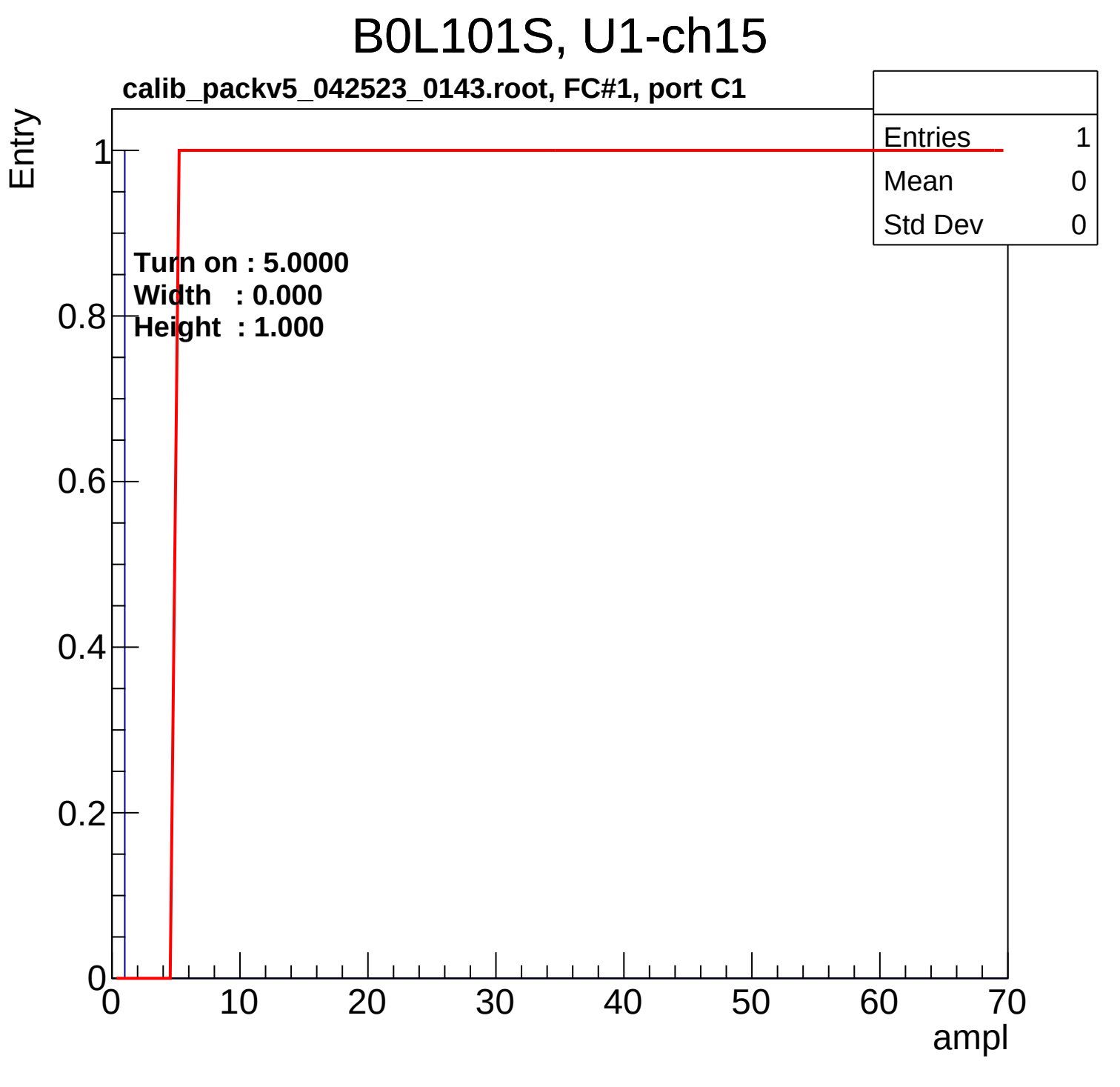

B0L101S, U1-ch10
calib_packv5_042523_0143.root, FC#1, port C1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

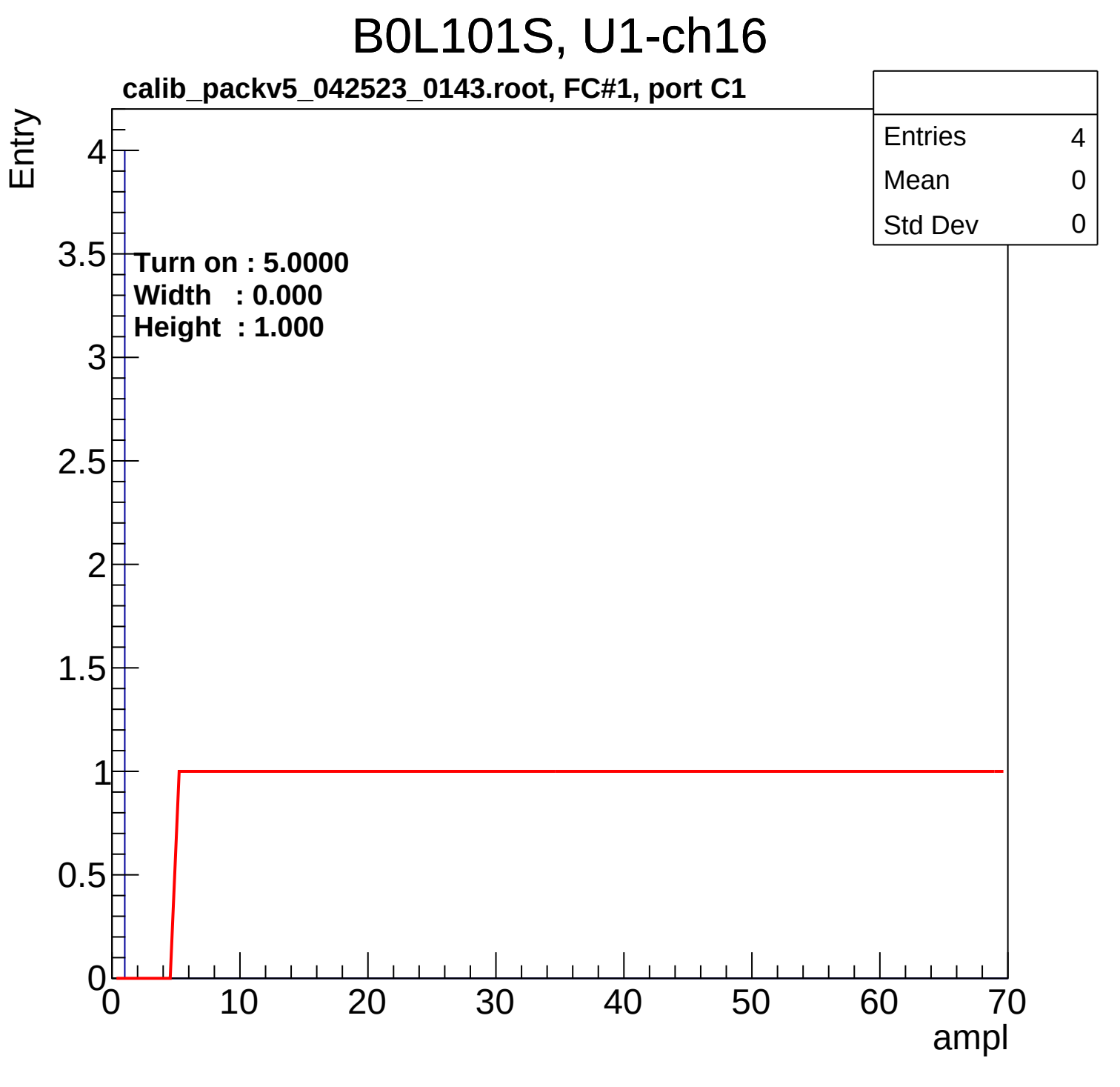

B0L101S, U1-ch11
calib_packv5_042523_0143.root, FC#1, port C1
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

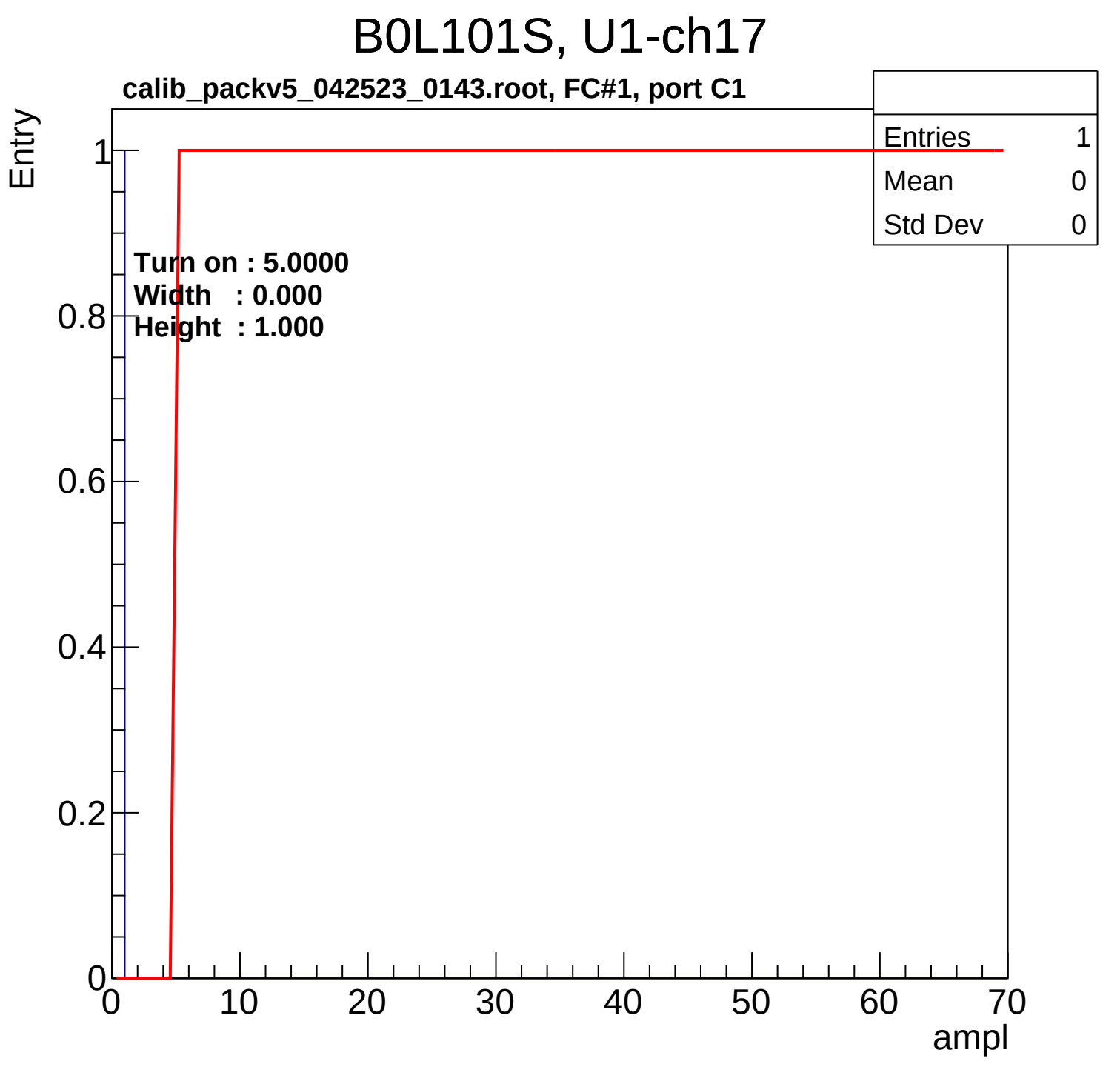

B0L101S, U1-ch12
calib_packv5_042523_0143.root, FC#1, port C1
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

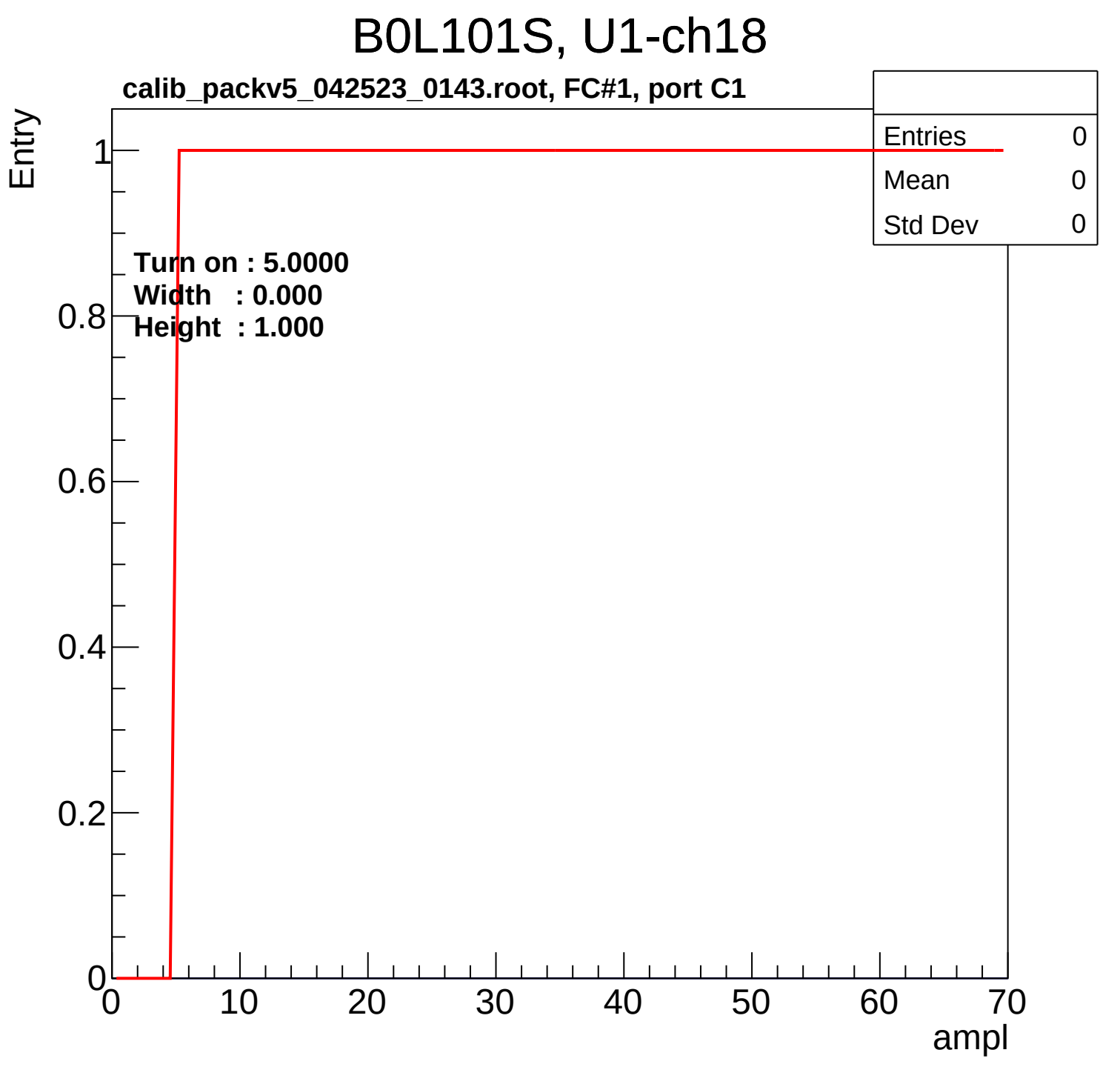

B0L101S, U1-ch13
calib_packv5_042523_0143.root, FC#1, port C1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

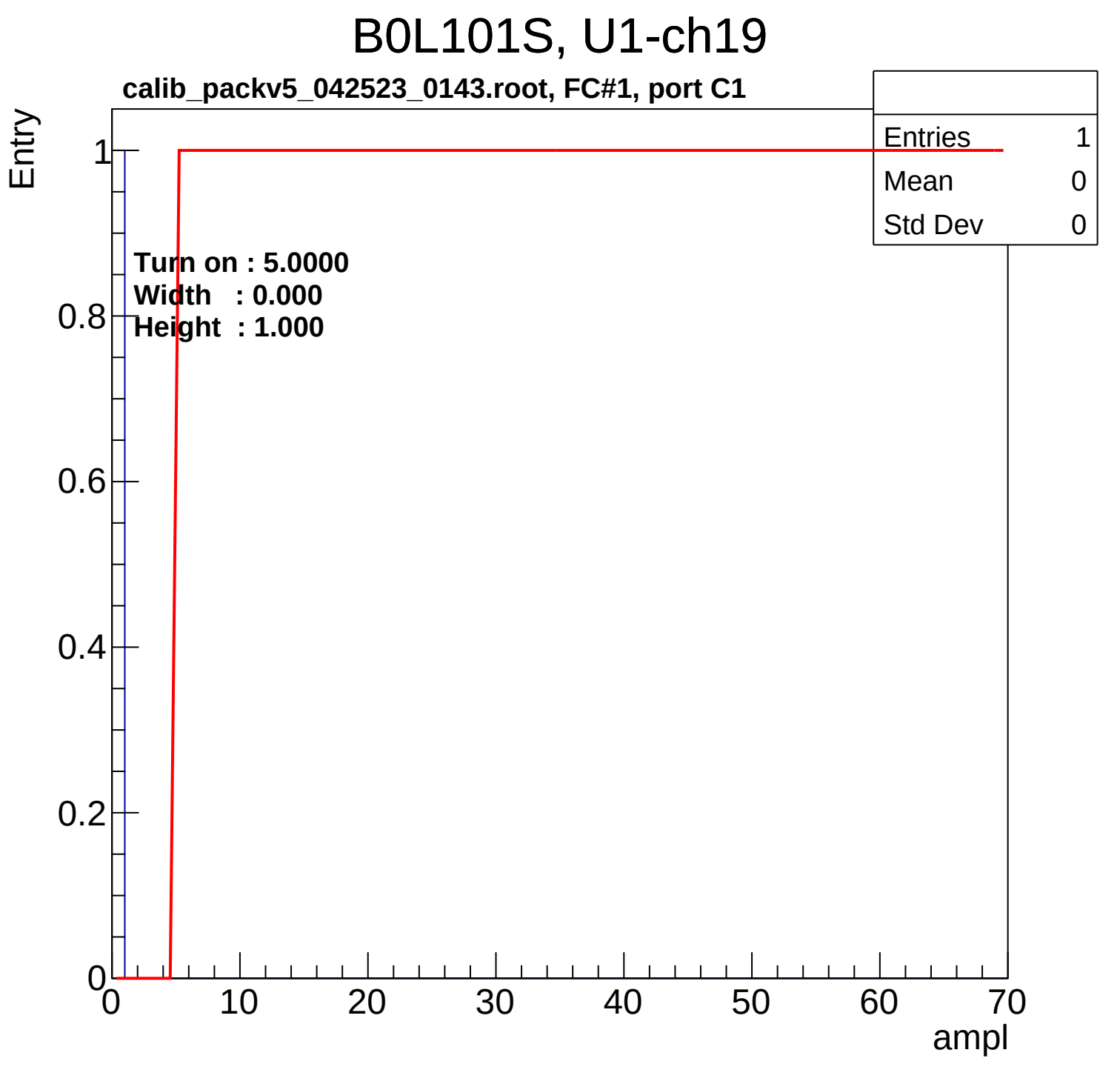

B0L101S, U1-ch14
calib_packv5_042523_0143.root, FC#1, port C1
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

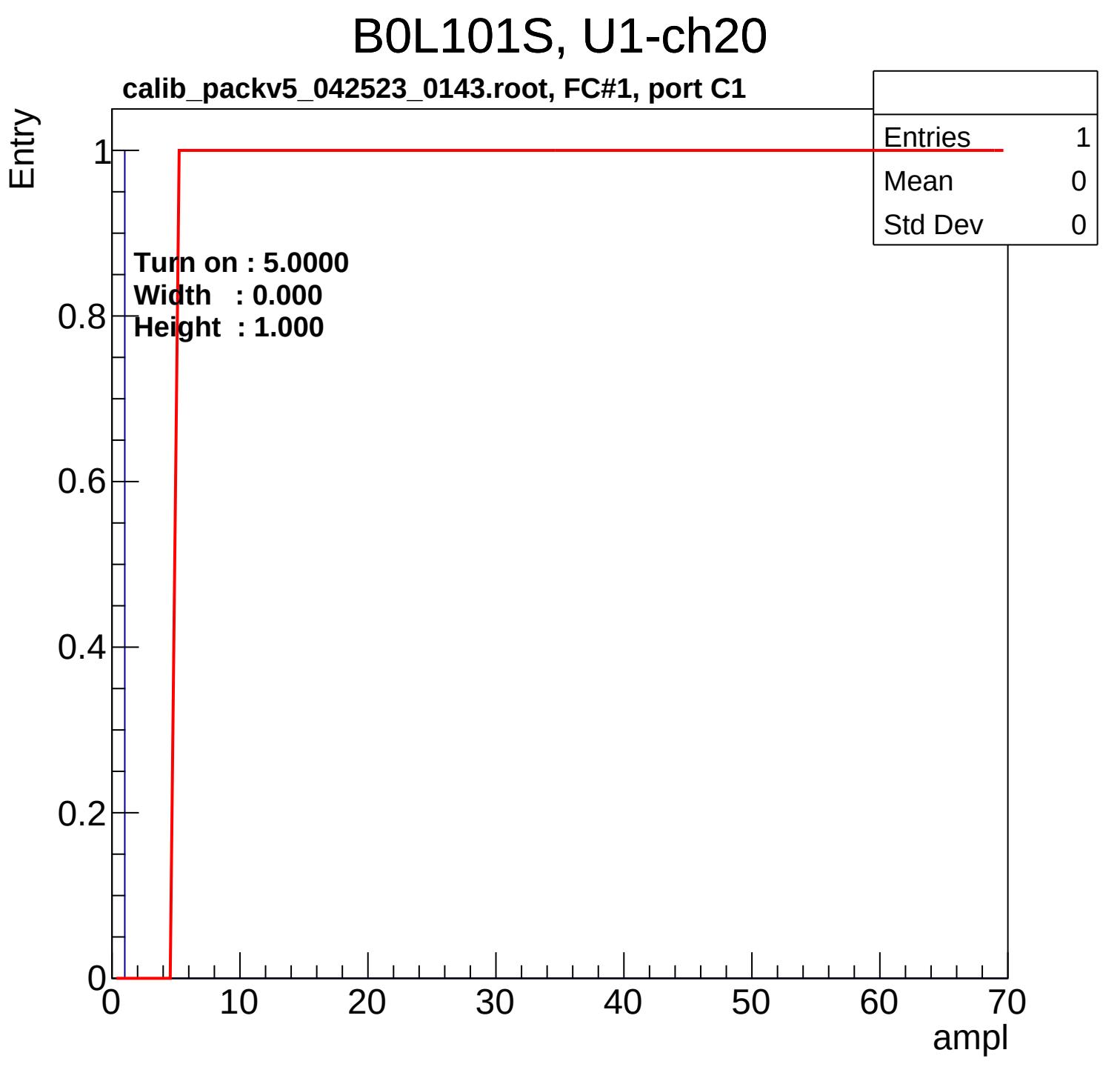

B0L101S, U1-ch15
calib_packv5_042523_0143.root, FC#1, port C1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

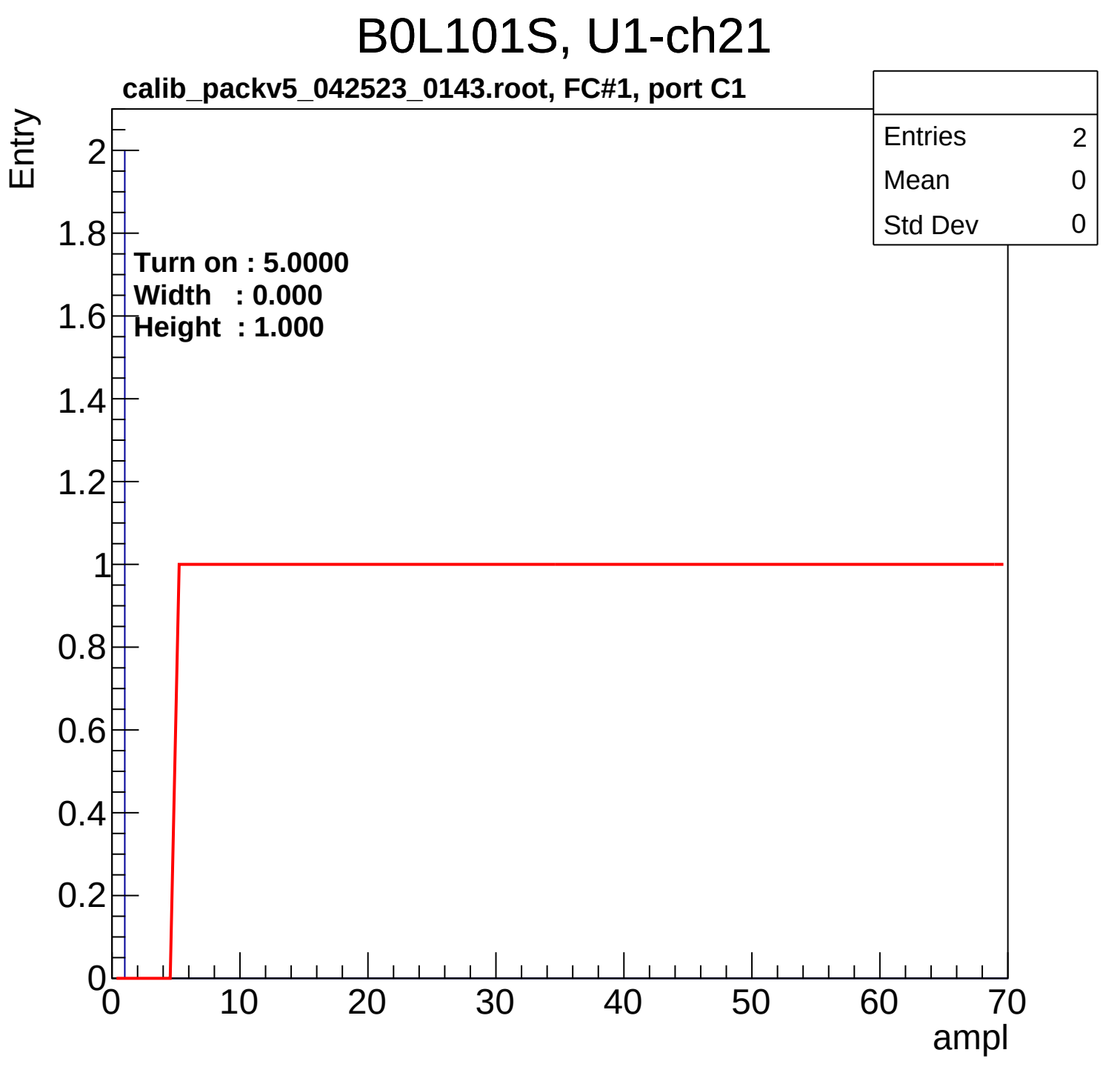

B0L101S, U1-ch16
calib_packv5_042523_0143.root, FC#1, port C1
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

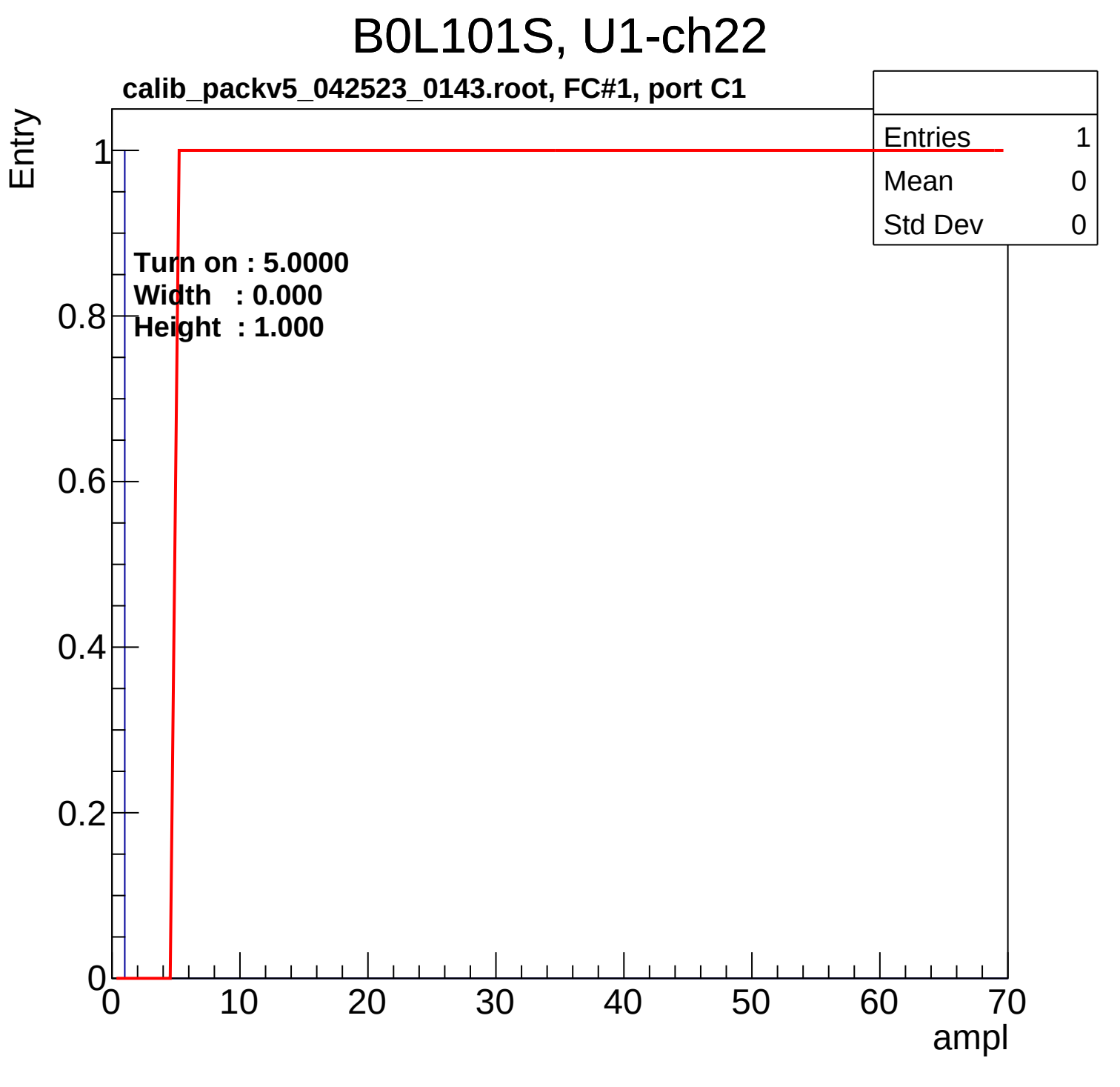

B0L101S, U1-ch17
calib_packv5_042523_0143.root, FC#1, port C1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

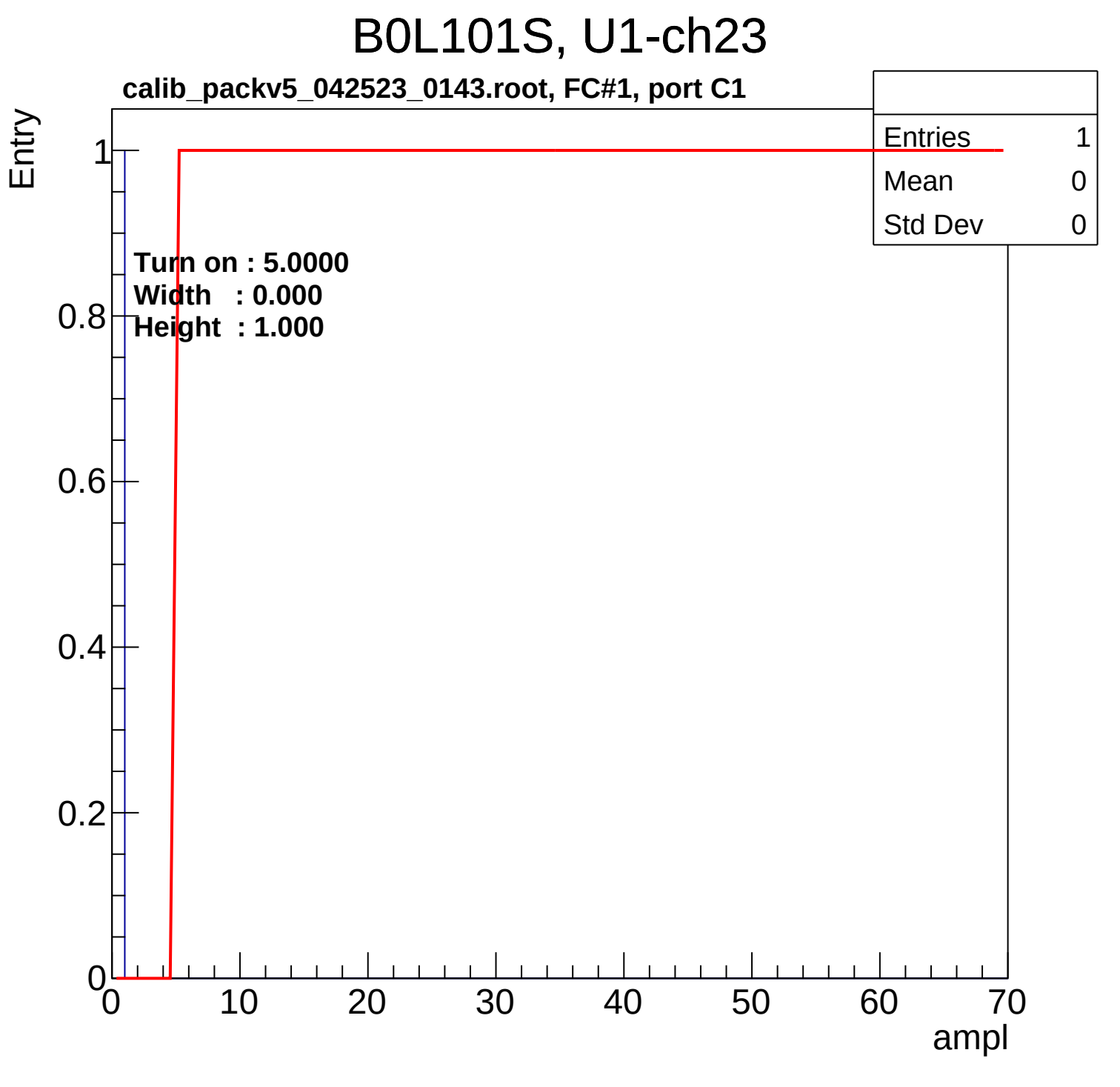

B0L101S, U1-ch18
calib_packv5_042523_0143.root, FC#1, port C1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

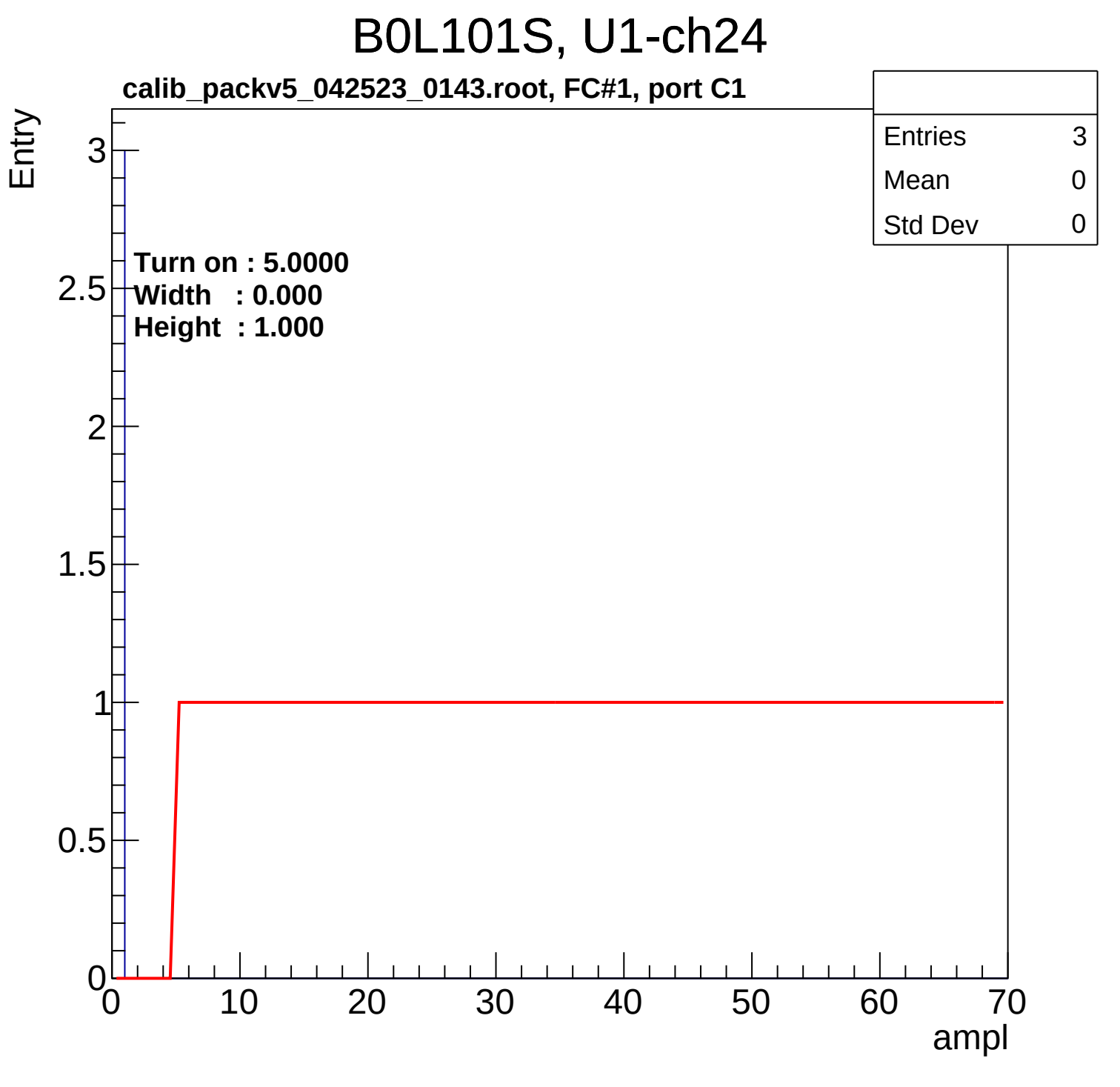

B0L101S, U1-ch19
calib_packv5_042523_0143.root, FC#1, port C1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

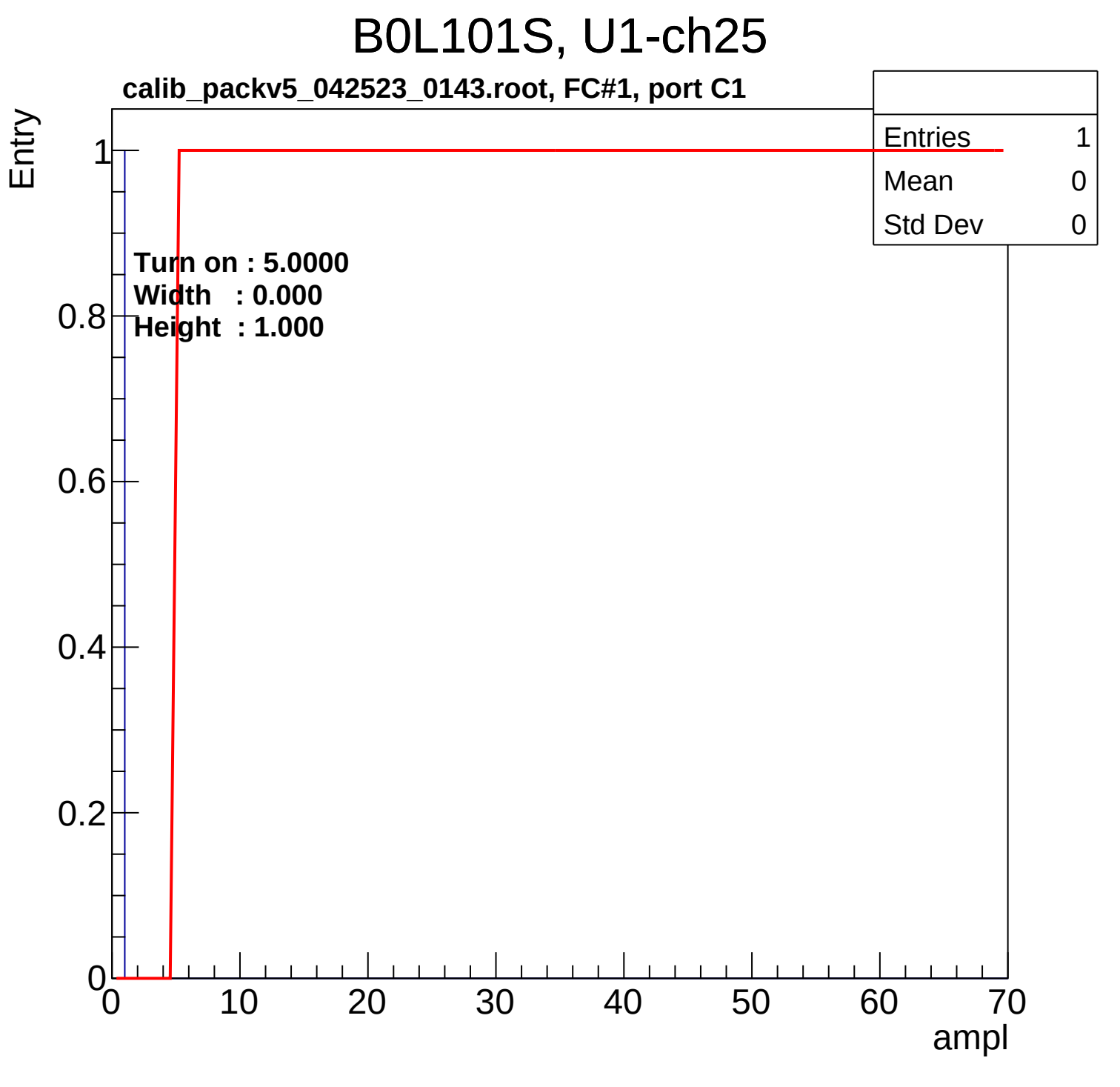

B0L101S, U1-ch20
calib_packv5_042523_0143.root, FC#1, port C1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

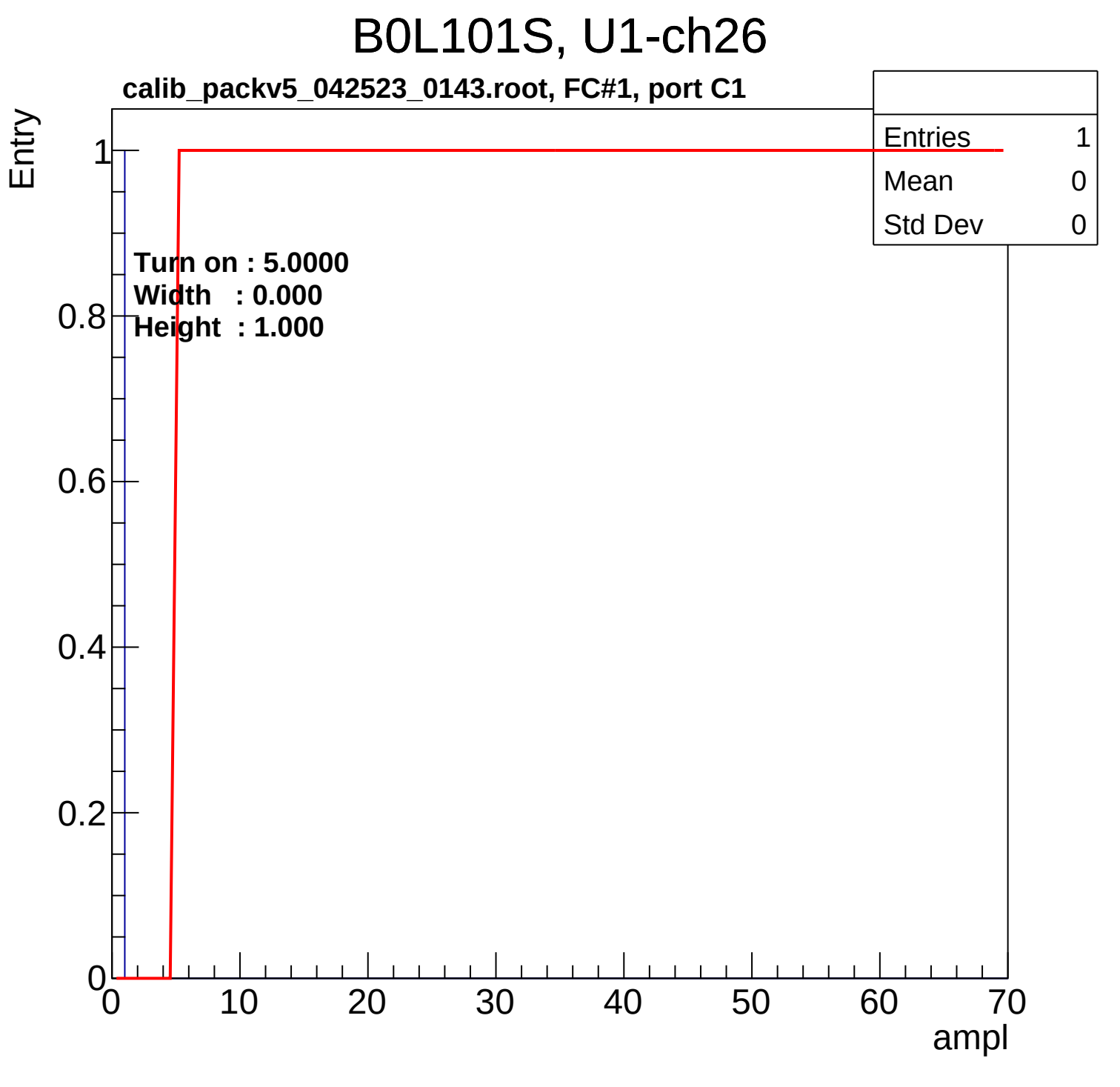

B0L101S, U1-ch21
calib_packv5_042523_0143.root, FC#1, port C1
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

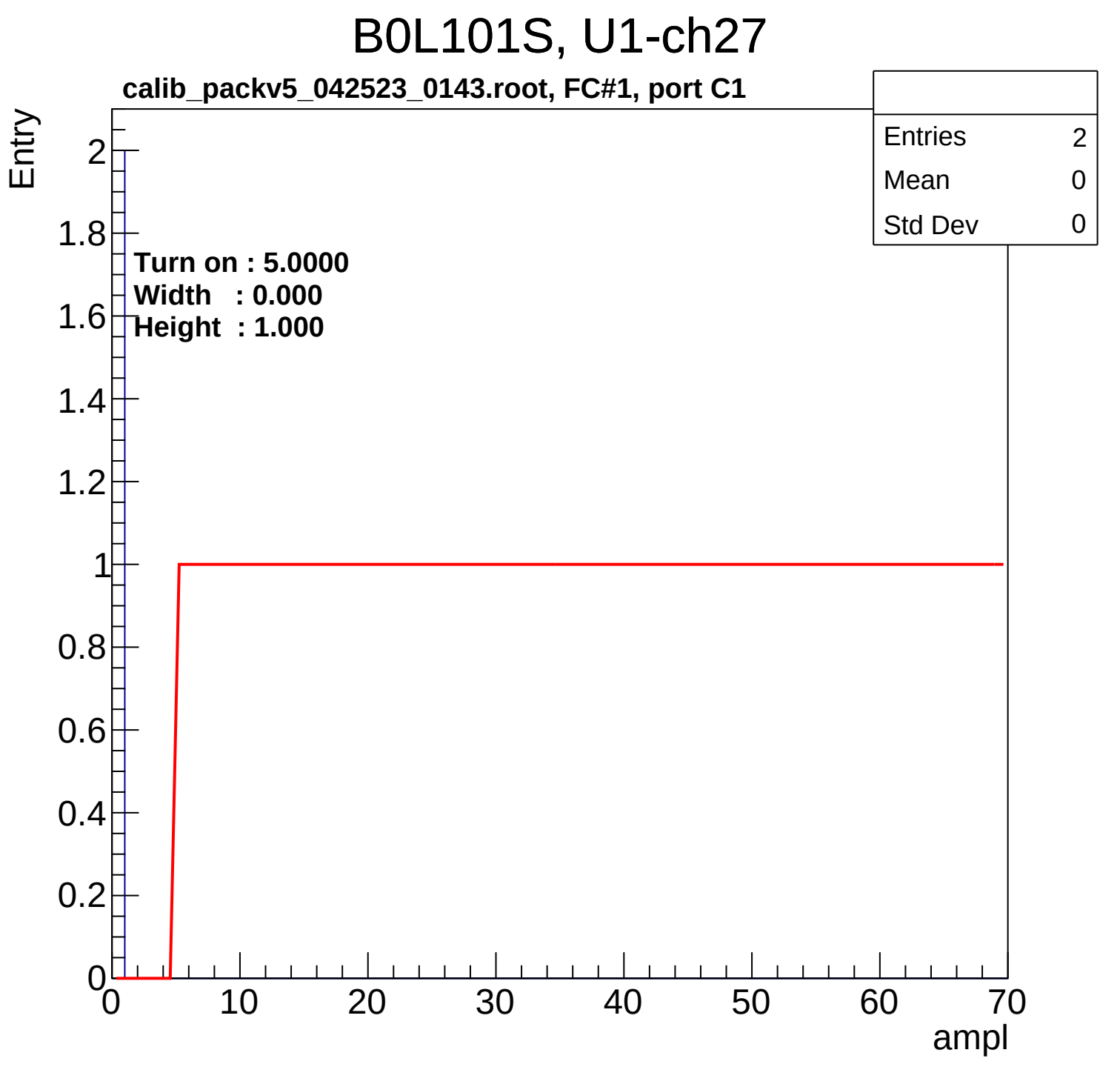

B0L101S, U1-ch22
calib_packv5_042523_0143.root, FC#1, port C1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

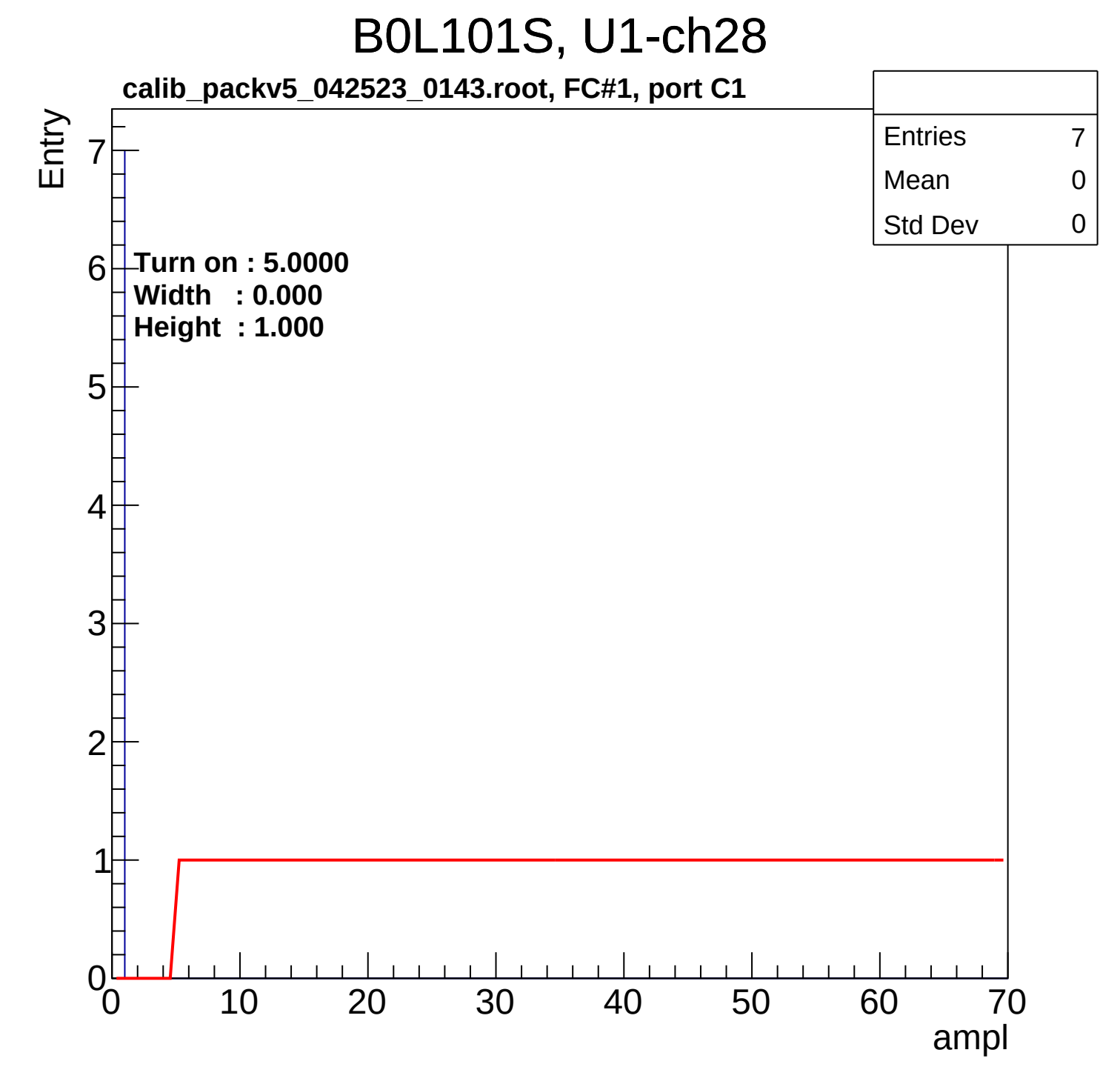

B0L101S, U1-ch23
calib_packv5_042523_0143.root, FC#1, port C1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

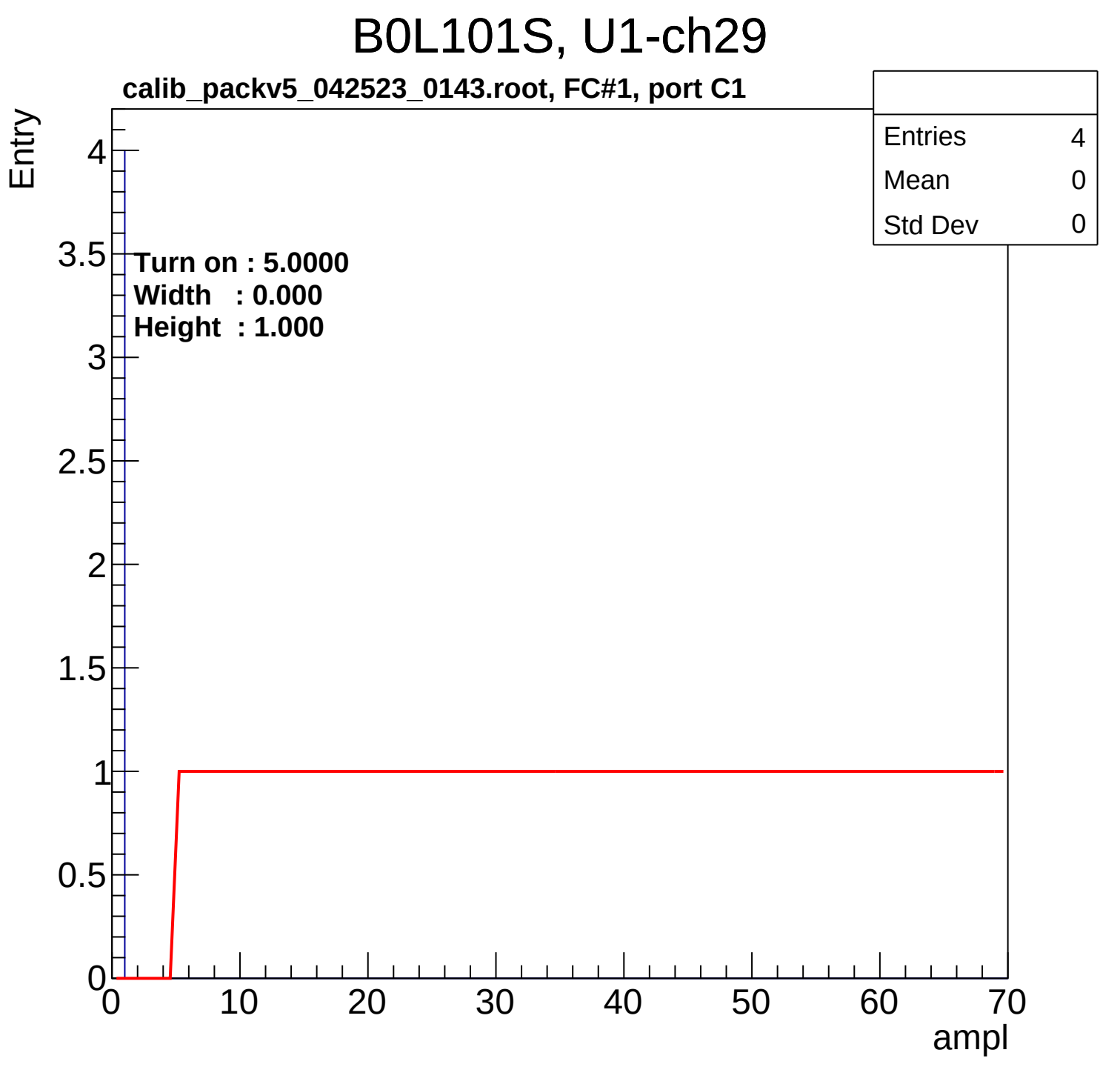

B0L101S, U1-ch24
calib_packv5_042523_0143.root, FC#1, port C1
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

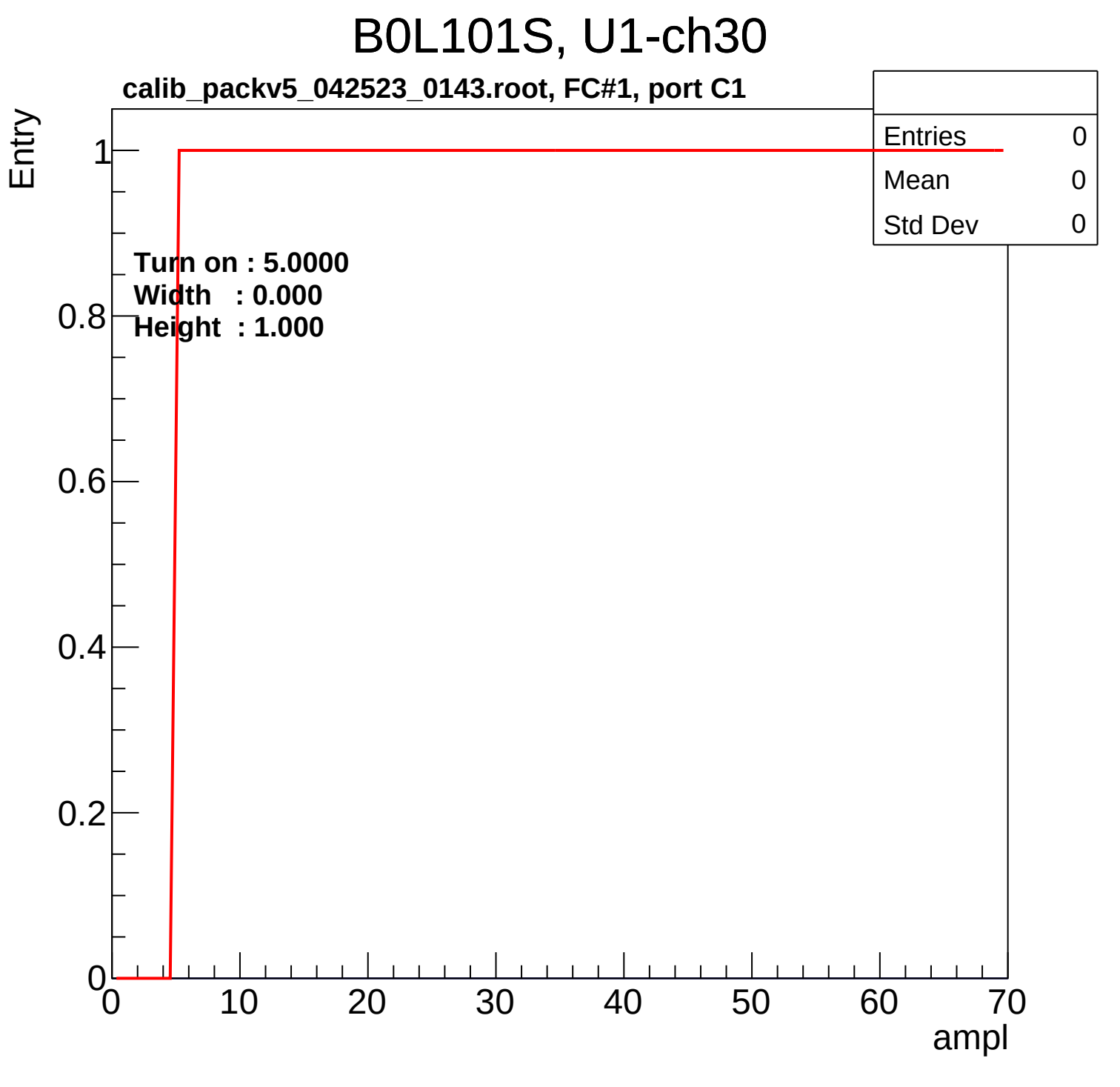

B0L101S, U1-ch25
calib_packv5_042523_0143.root, FC#1, port C1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

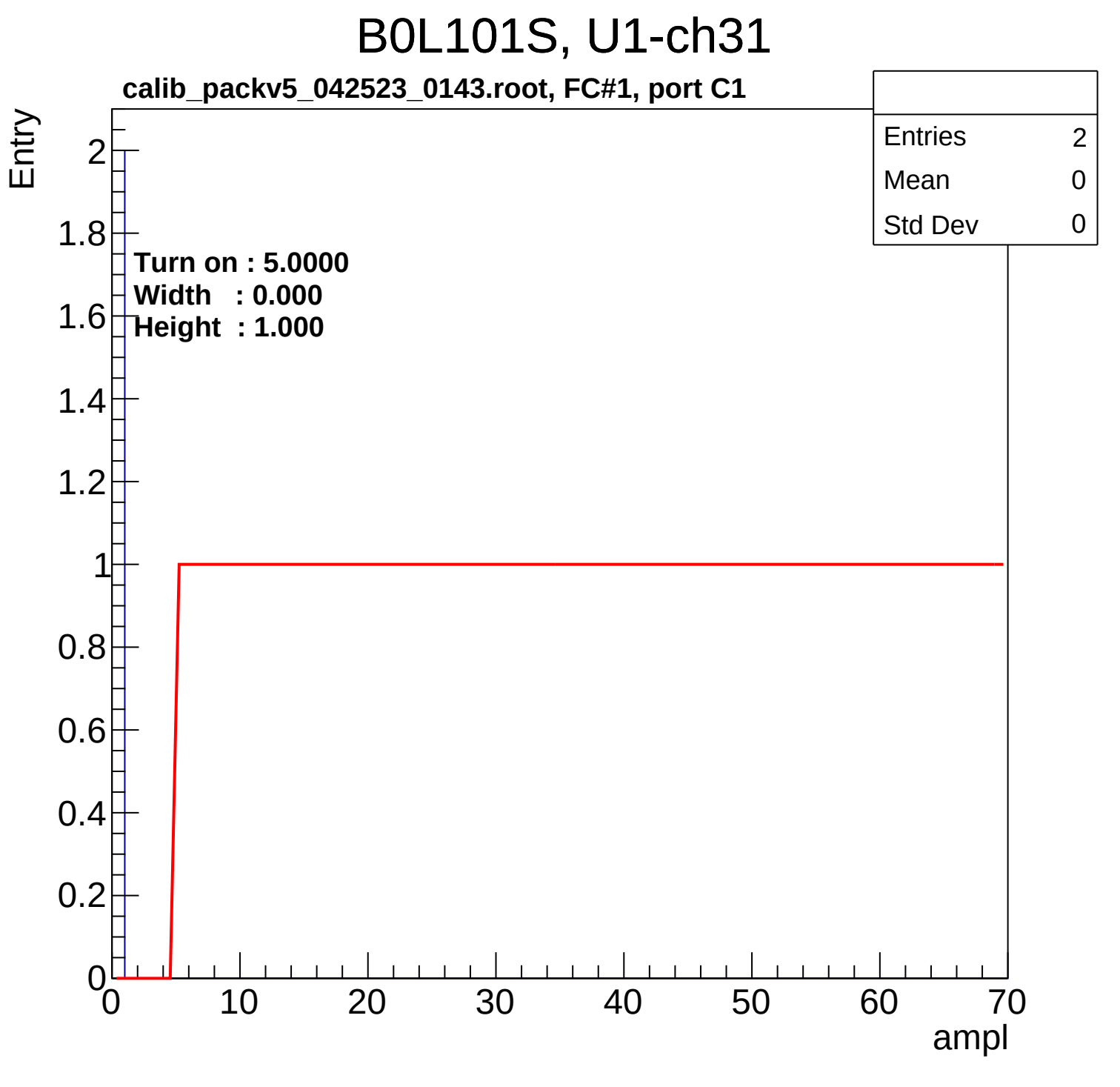

B0L101S, U1-ch26
calib_packv5_042523_0143.root, FC#1, port C1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

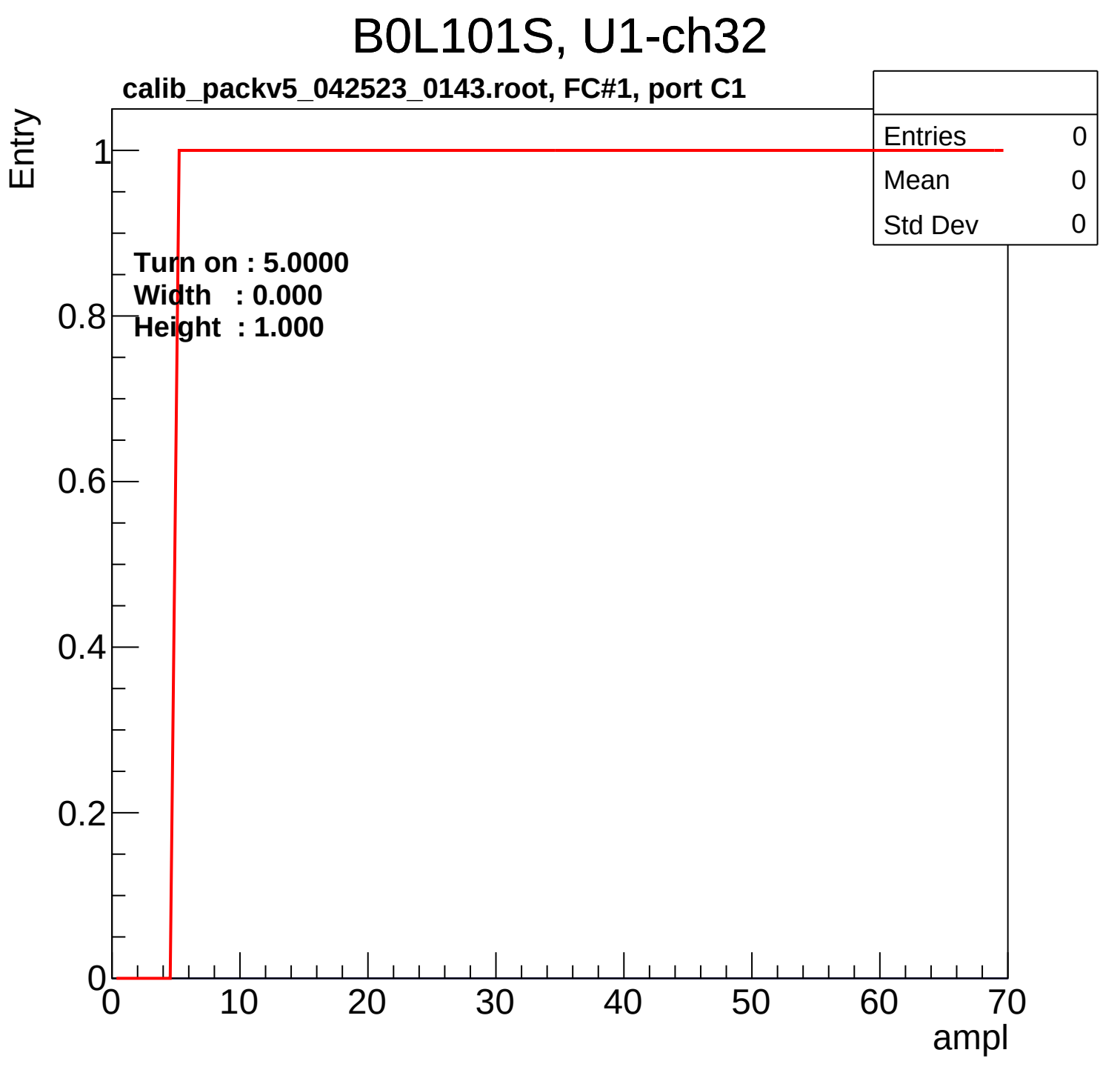

B0L101S, U1-ch27
calib_packv5_042523_0143.root, FC#1, port C1
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

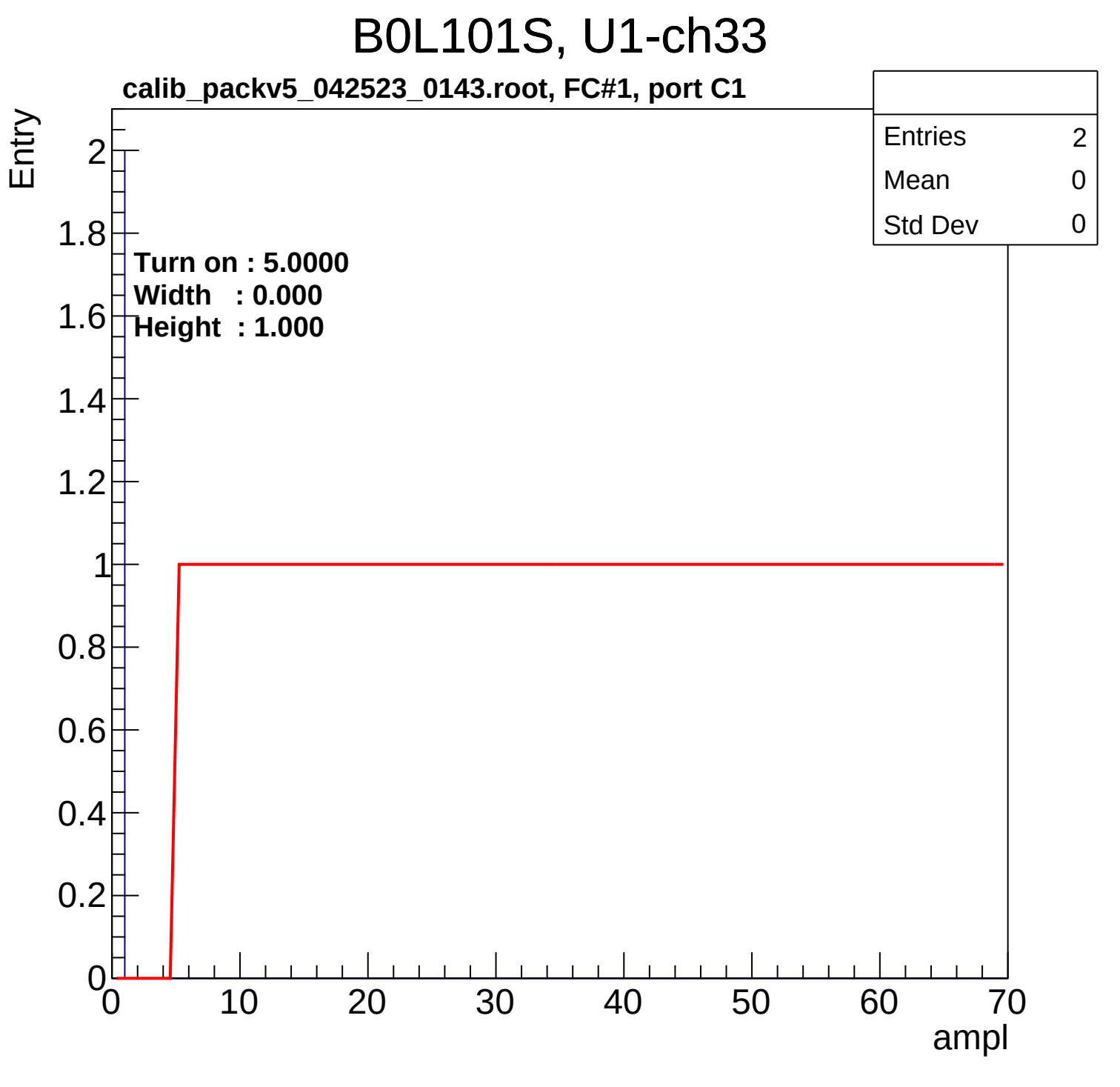

B0L101S, U1-ch28
calib_packv5_042523_0143.root, FC#1, port C1
Entries 7
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

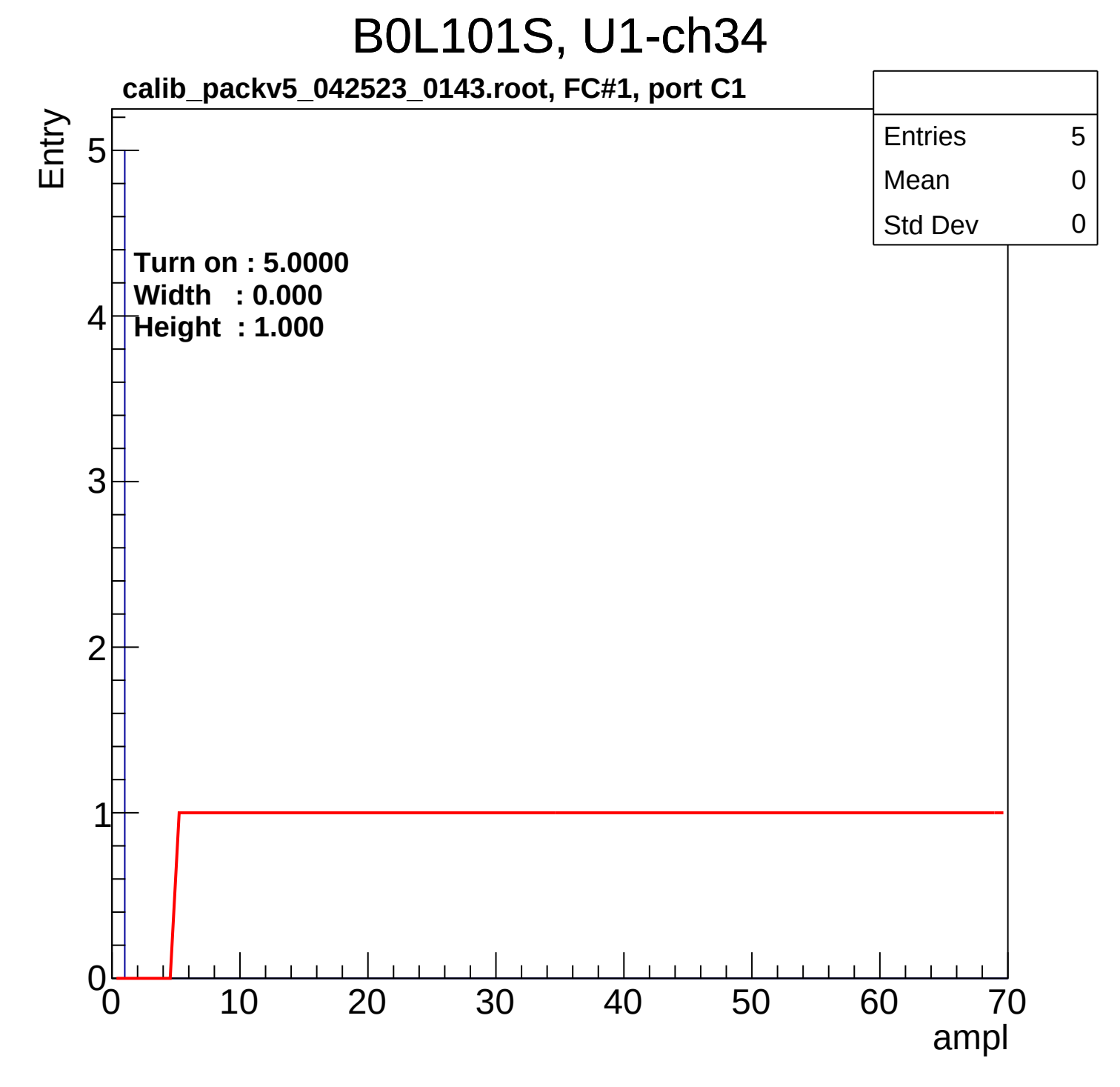

B0L101S, U1-ch29
calib_packv5_042523_0143.root, FC#1, port C1
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

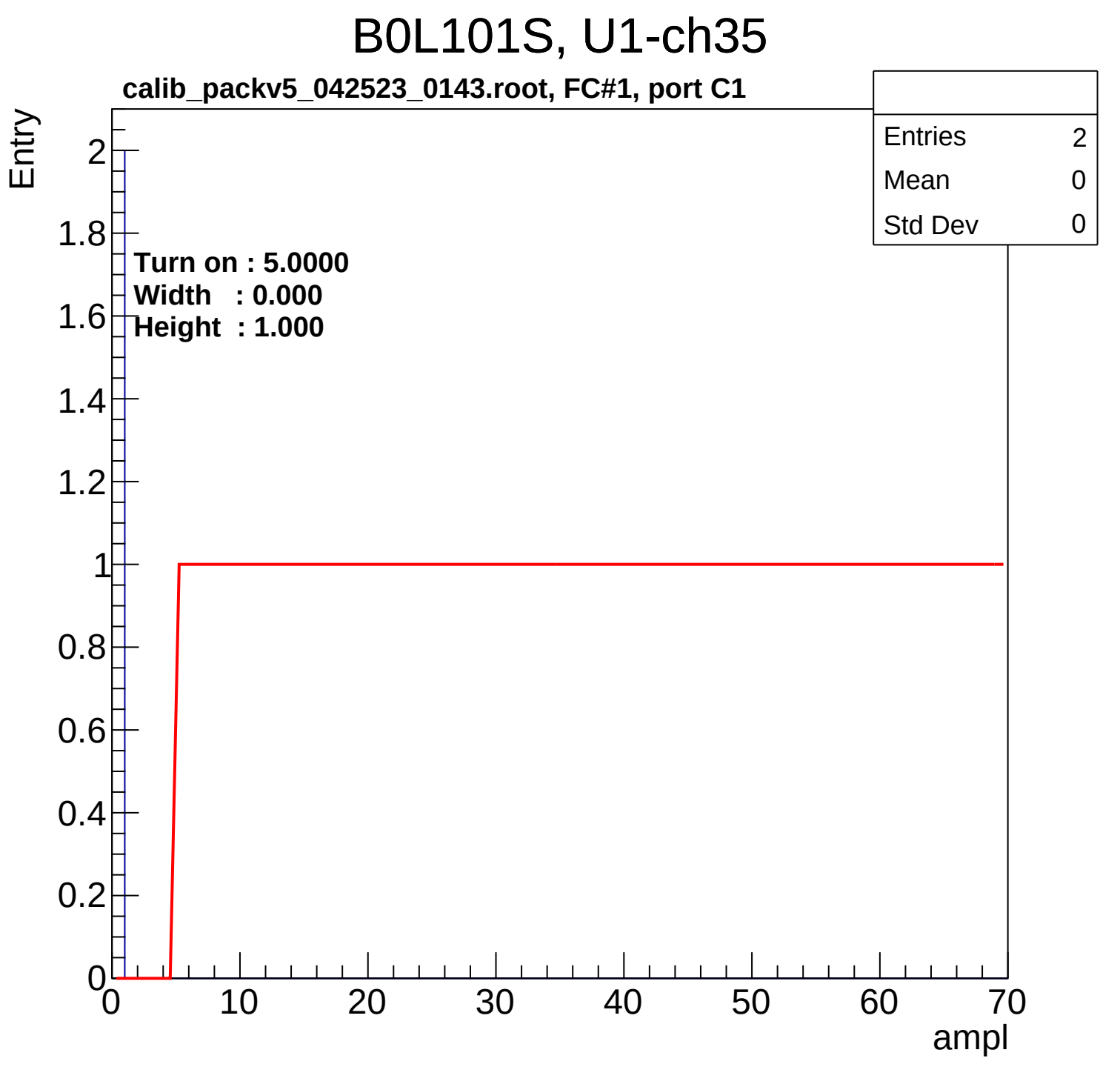

B0L101S, U1-ch30
calib_packv5_042523_0143.root, FC#1, port C1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

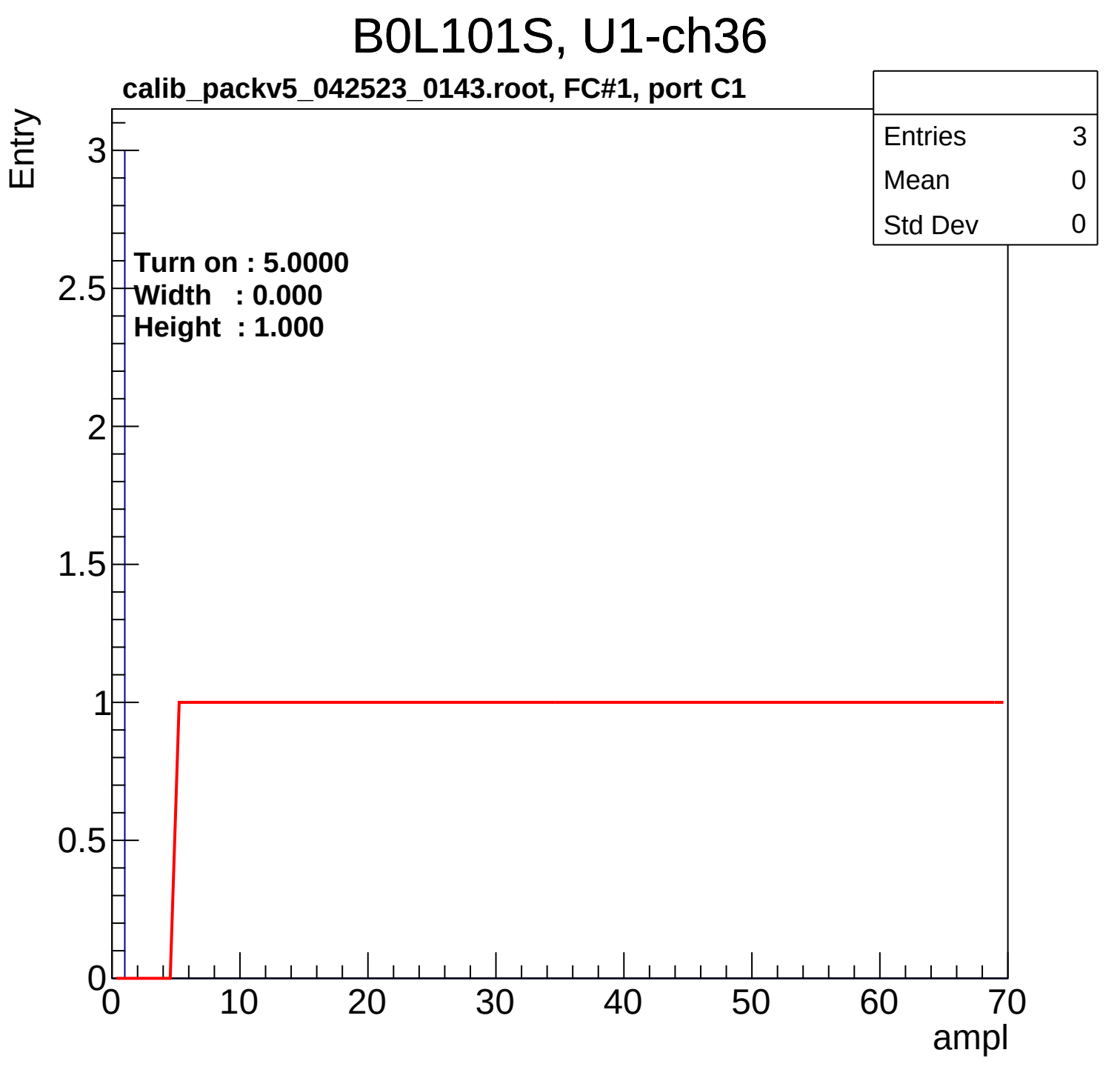

B0L101S, U1-ch31
calib_packv5_042523_0143.root, FC#1, port C1
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

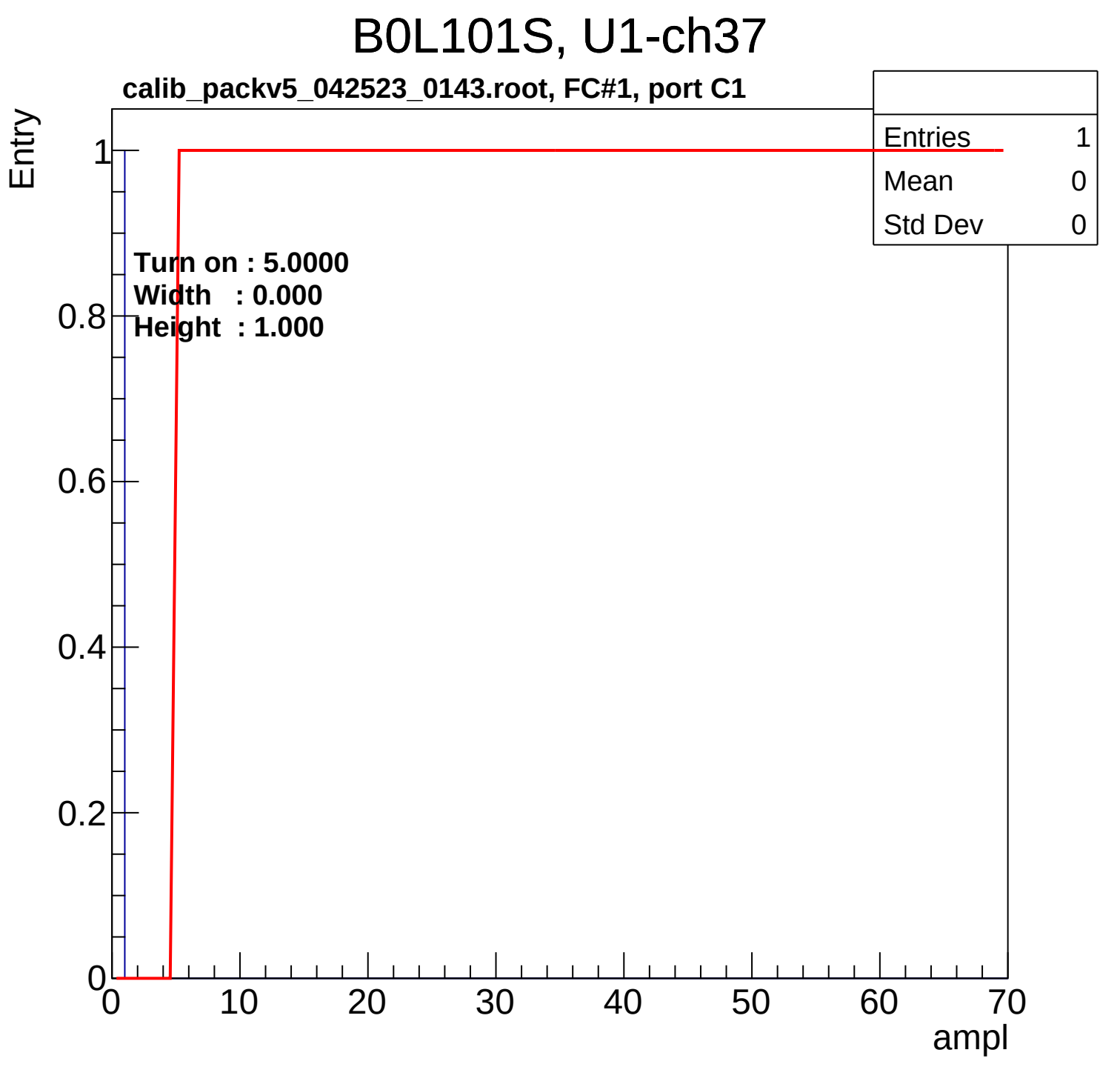

B0L101S, U1-ch32
calib_packv5_042523_0143.root, FC#1, port C1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

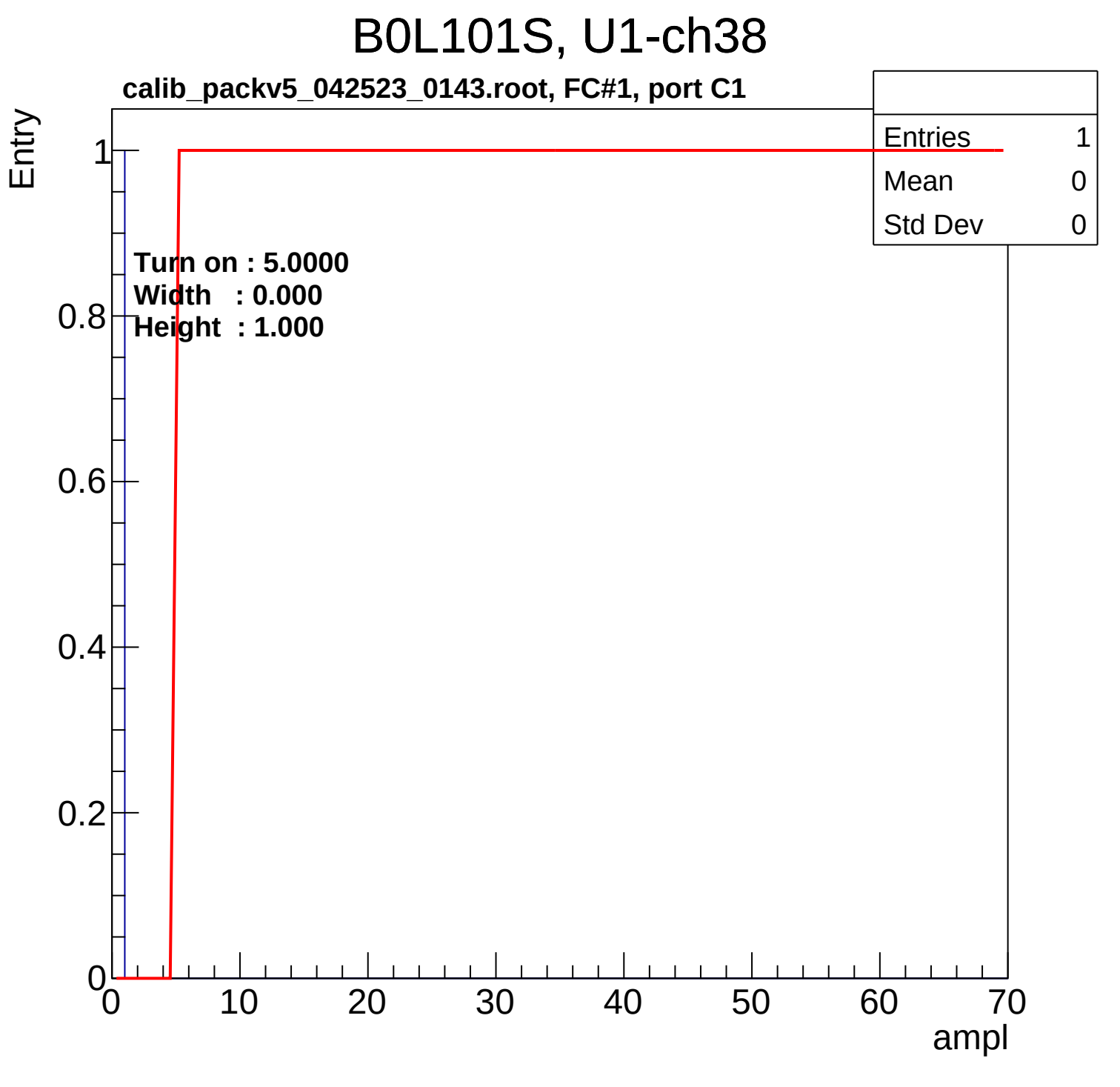

B0L101S, U1-ch33
calib_packv5_042523_0143.root, FC#1, port C1
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

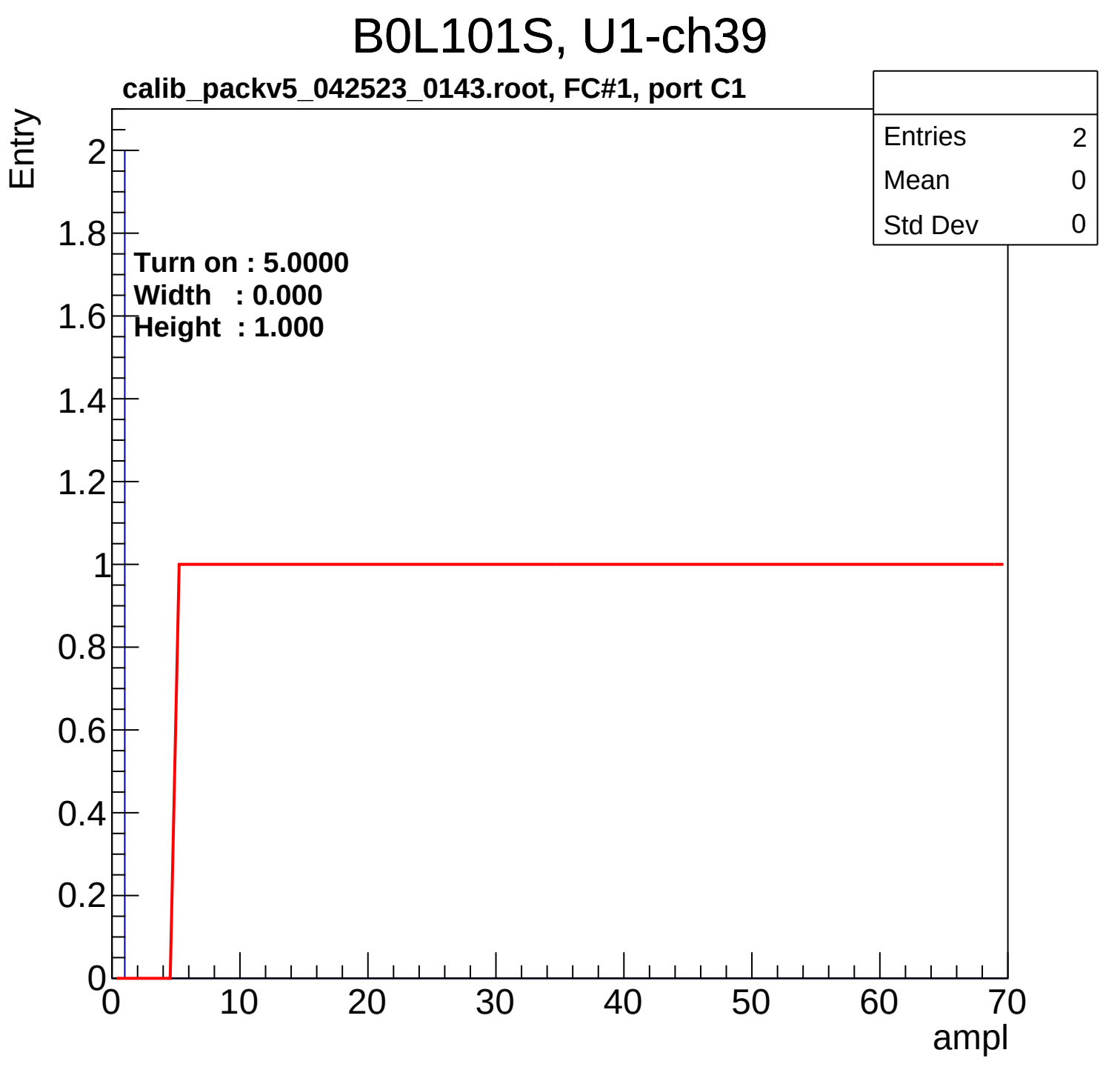

B0L101S, U1-ch34
calib_packv5_042523_0143.root, FC#1, port C1
Entries 5
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

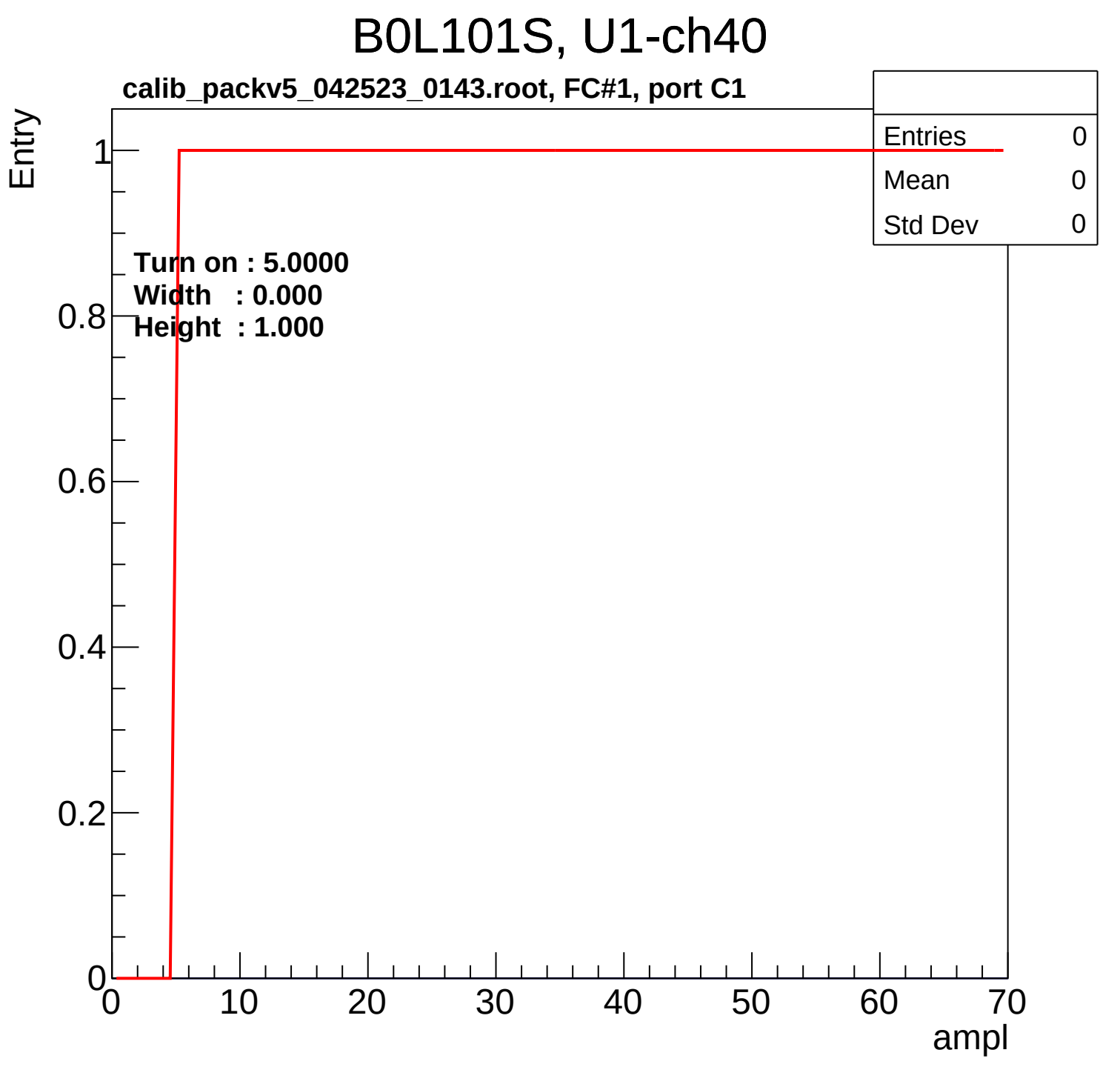

B0L101S, U1-ch35
calib_packv5_042523_0143.root, FC#1, port C1
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

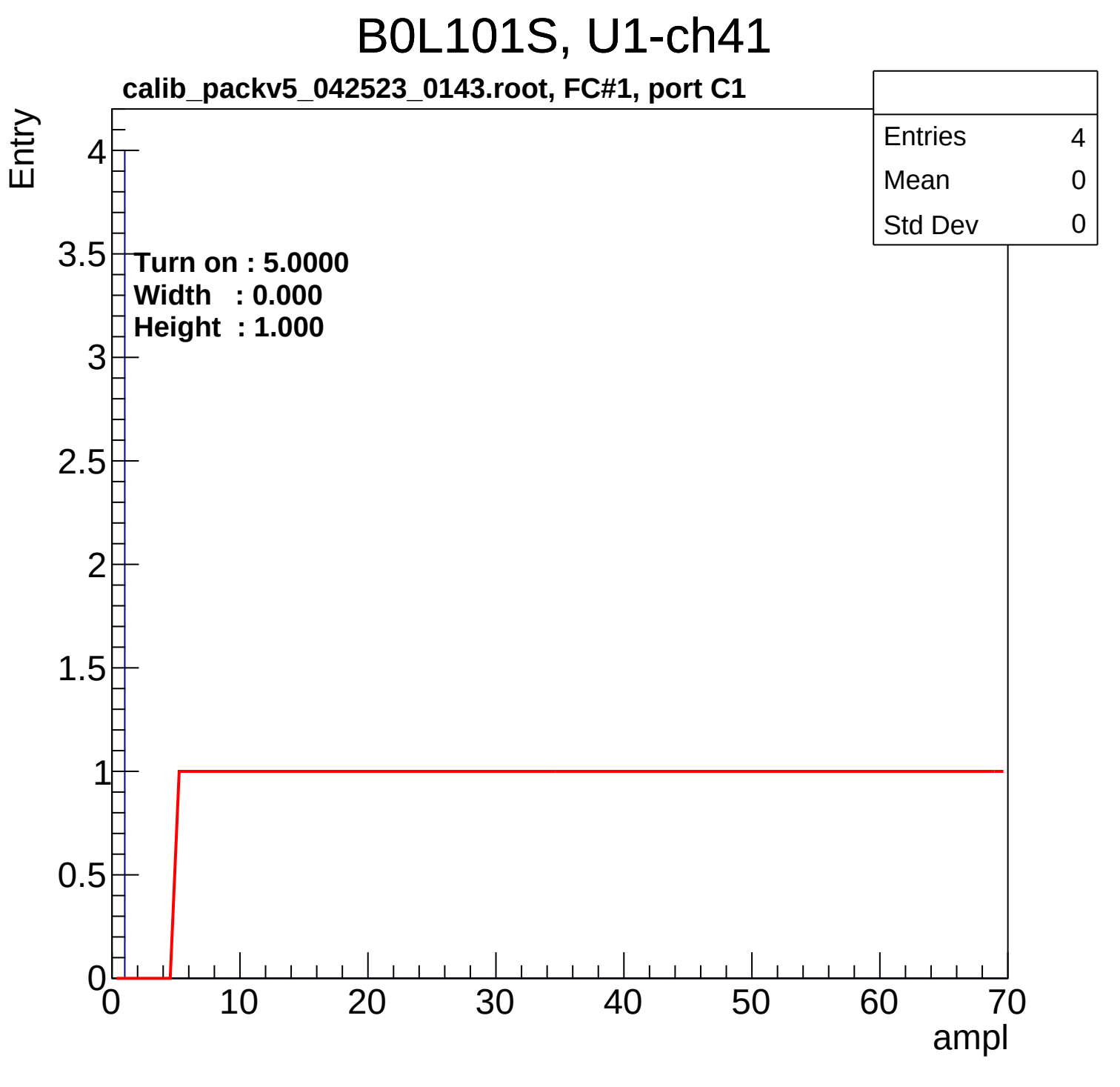

B0L101S, U1-ch36
calib_packv5_042523_0143.root, FC#1, port C1
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

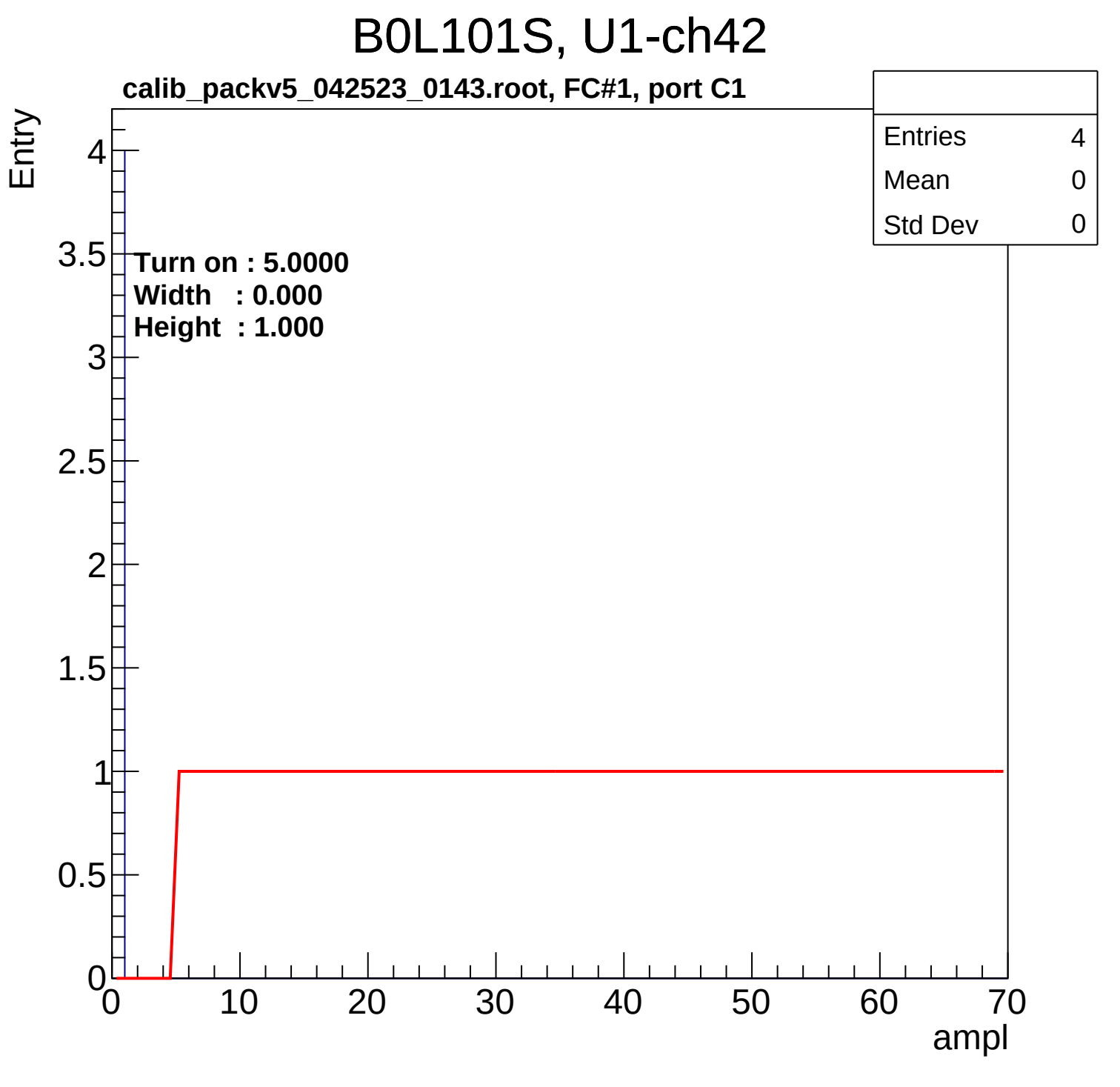

B0L101S, U1-ch37
calib_packv5_042523_0143.root, FC#1, port C1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

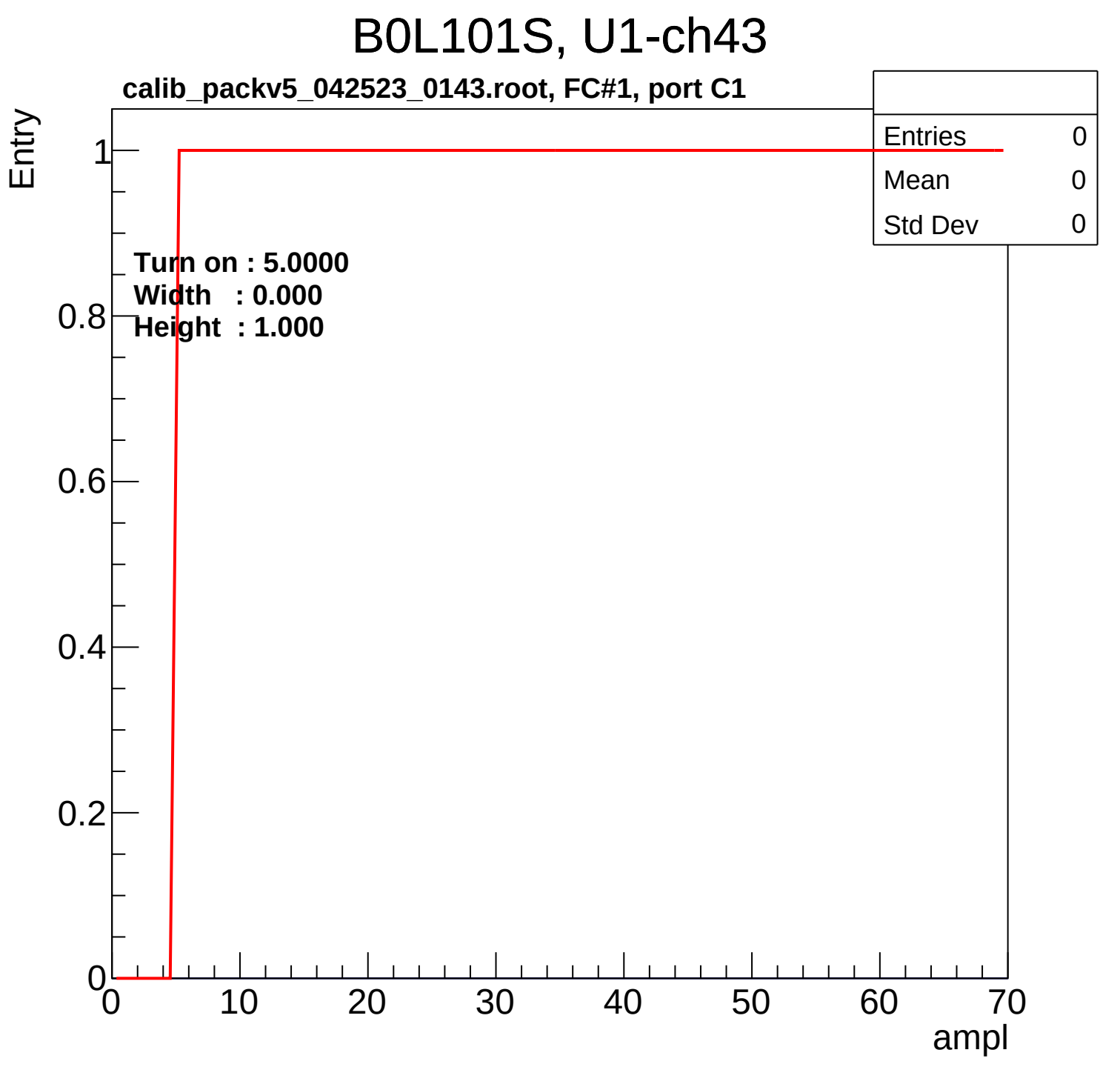

B0L101S, U1-ch38
calib_packv5_042523_0143.root, FC#1, port C1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

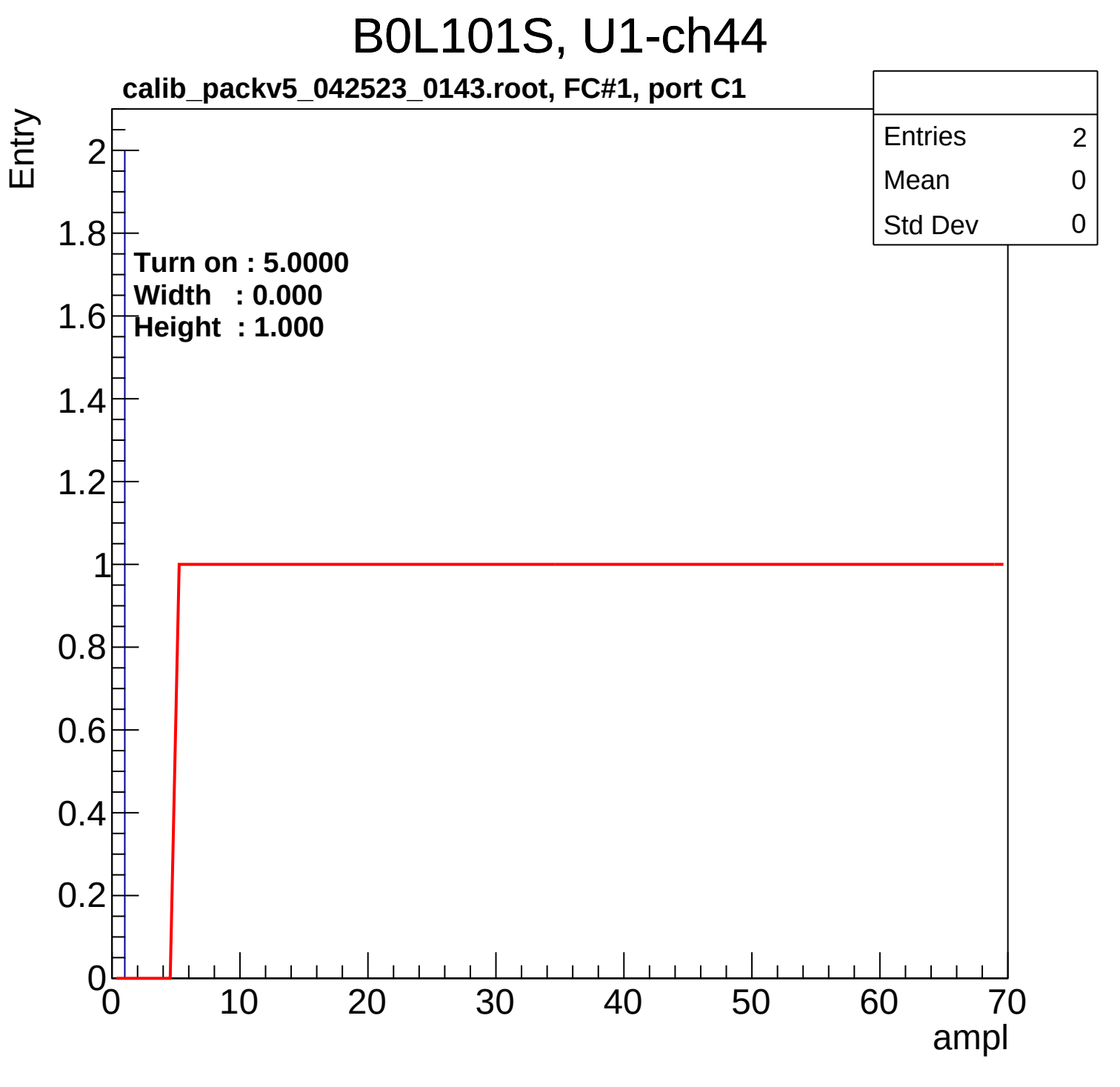

B0L101S, U1-ch39
calib_packv5_042523_0143.root, FC#1, port C1
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

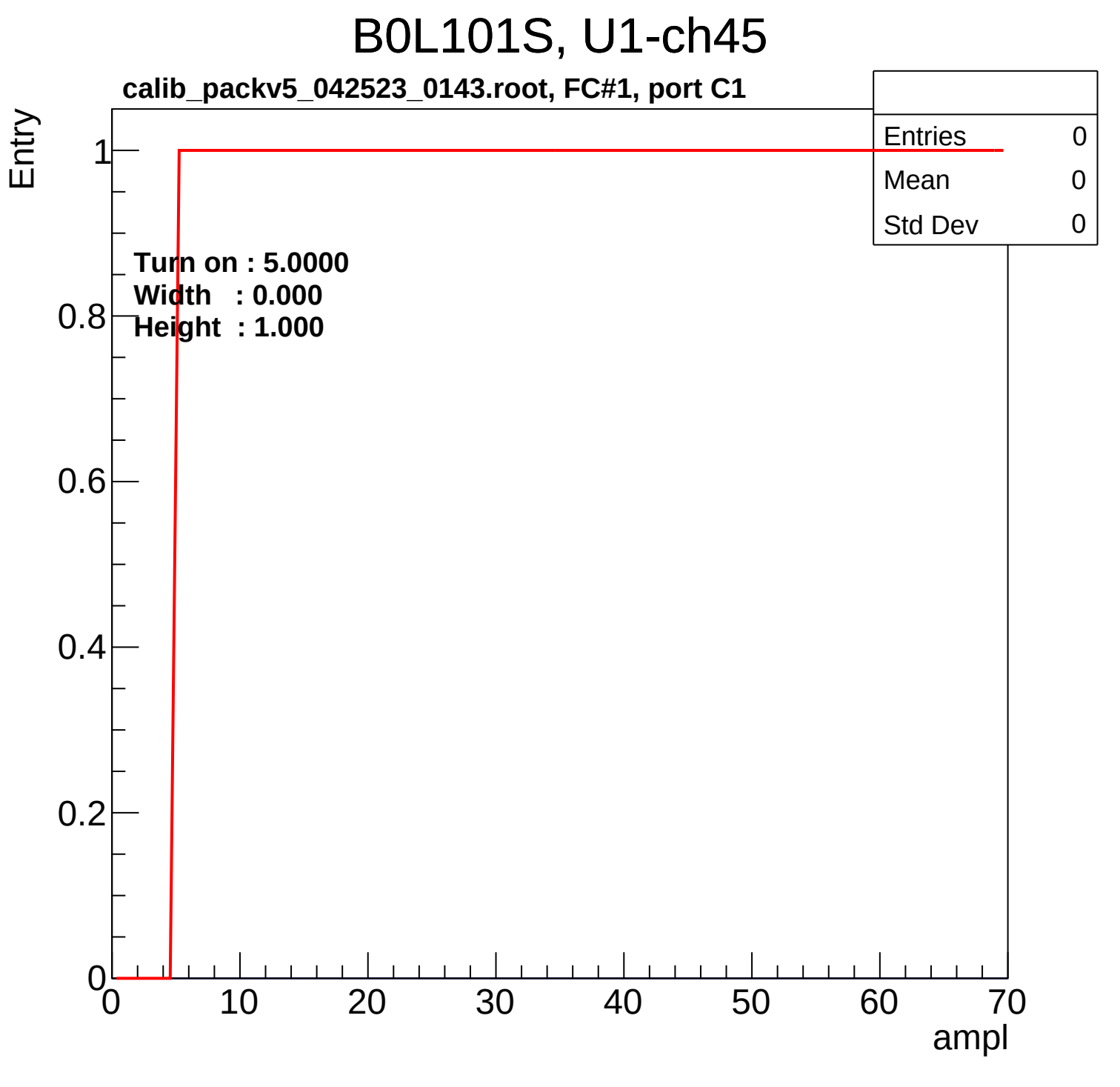

B0L101S, U1-ch40
calib_packv5_042523_0143.root, FC#1, port C1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

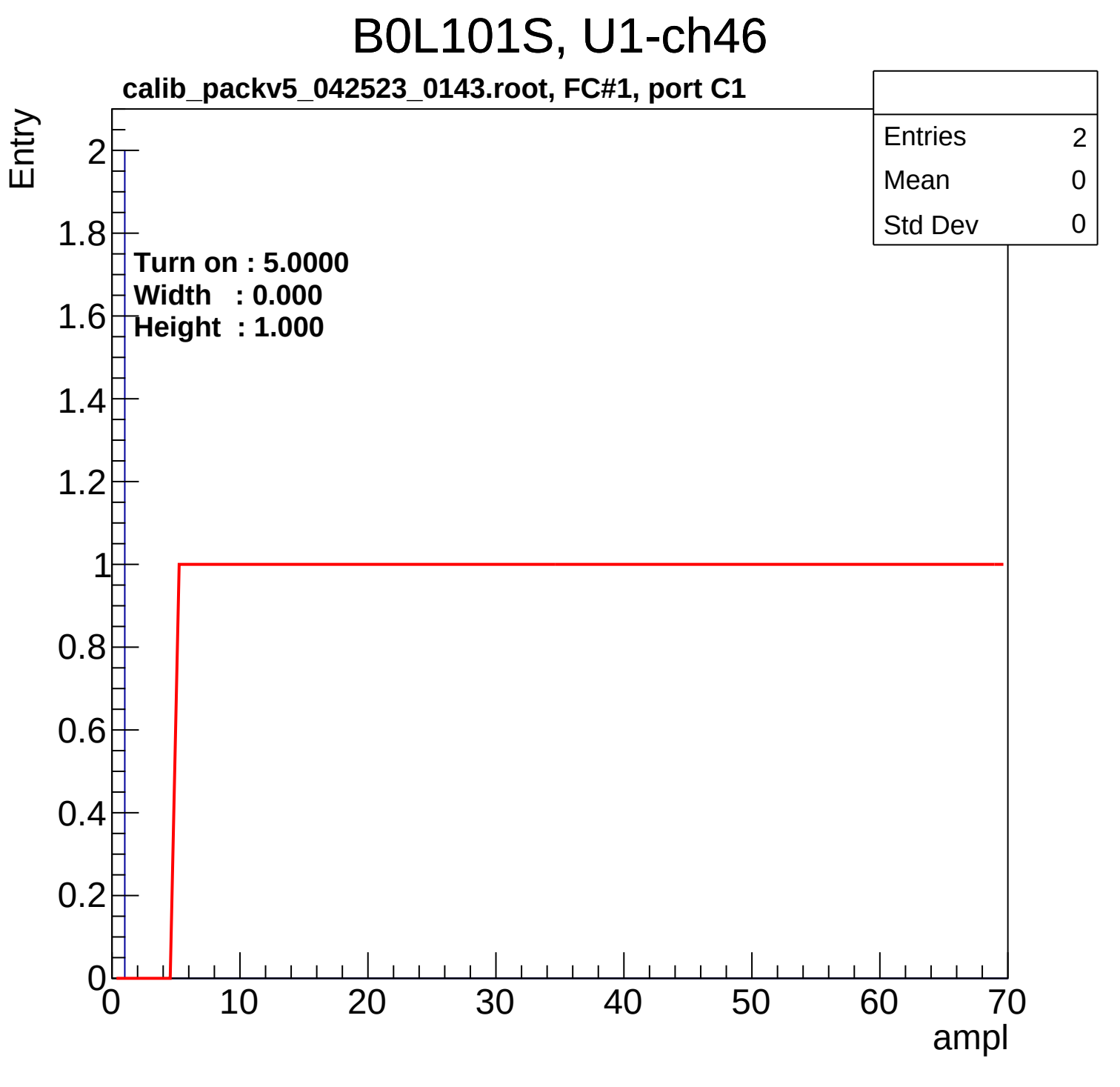

B0L101S, U1-ch41
calib_packv5_042523_0143.root, FC#1, port C1
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

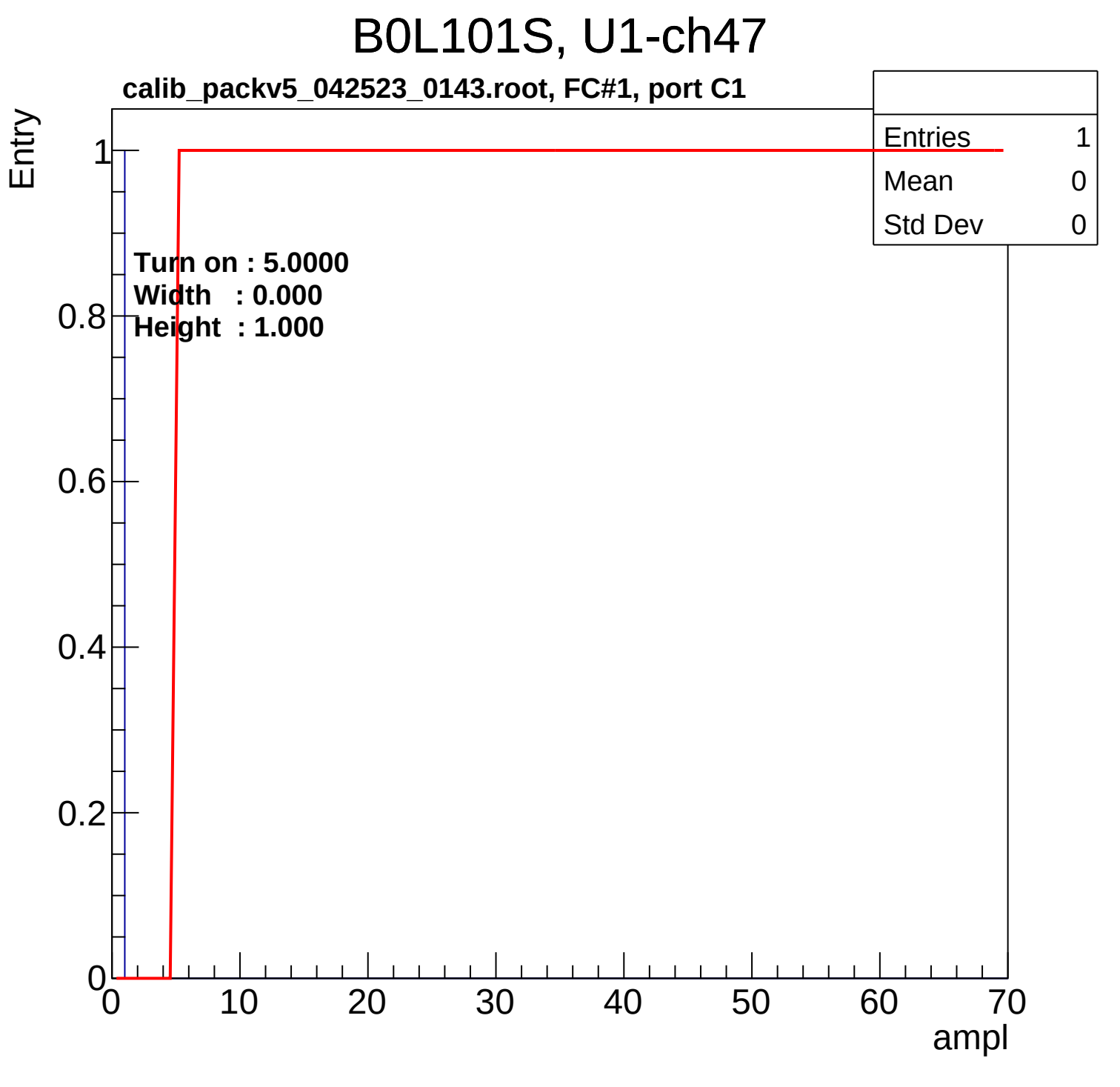

B0L101S, U1-ch42
calib_packv5_042523_0143.root, FC#1, port C1
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

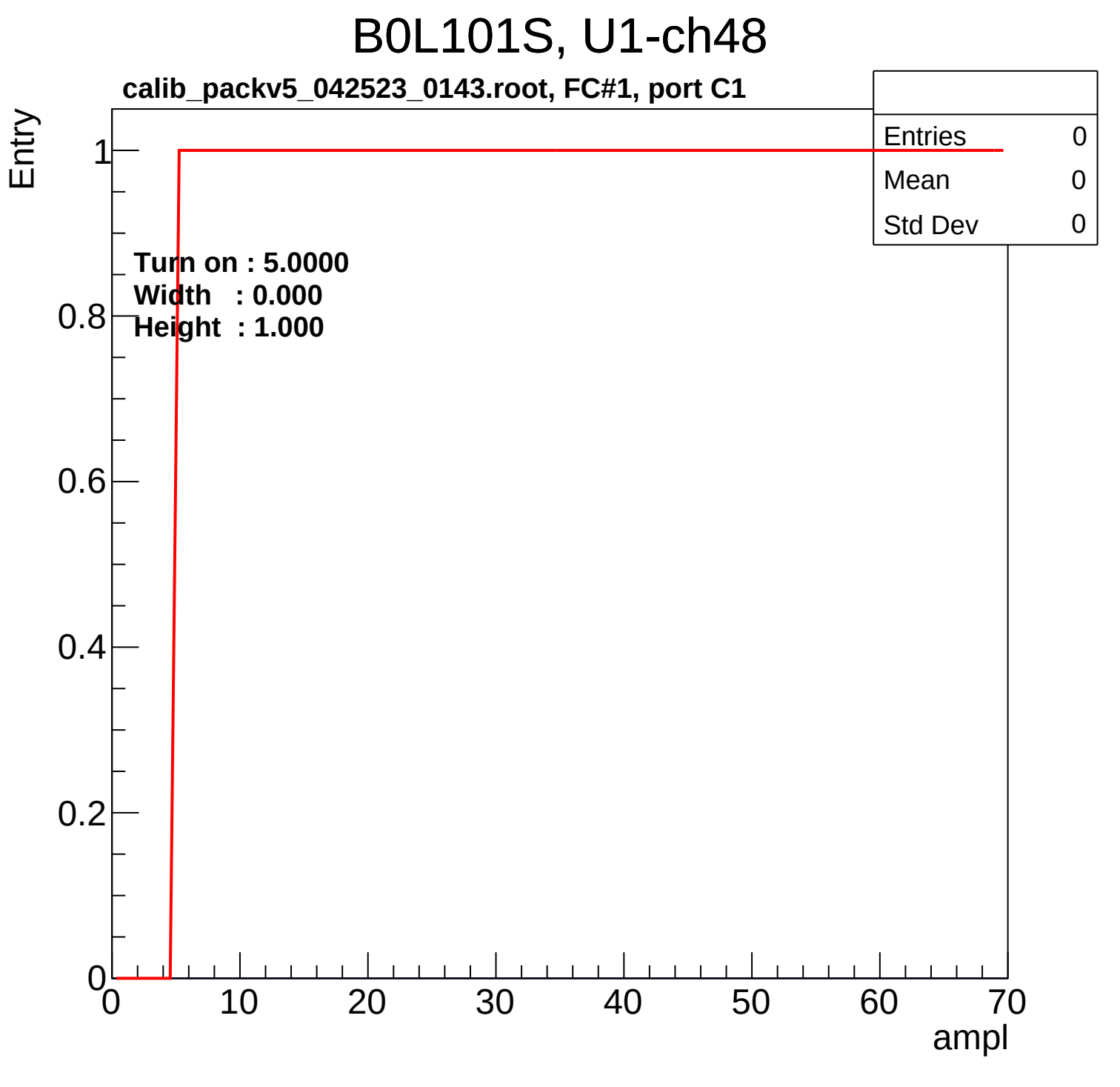

B0L101S, U1-ch43
calib_packv5_042523_0143.root, FC#1, port C1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

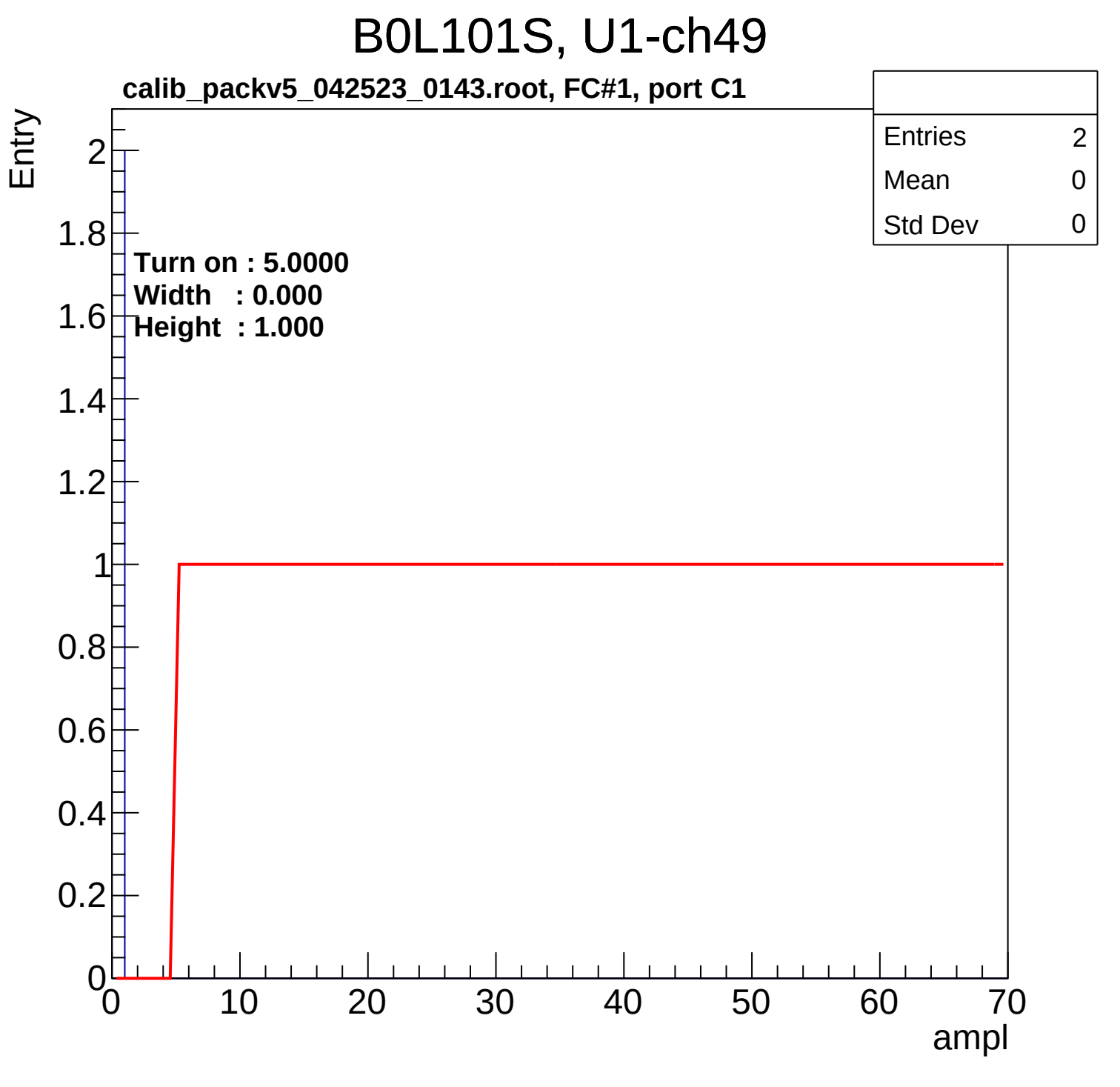

B0L101S, U1-ch44
calib_packv5_042523_0143.root, FC#1, port C1
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

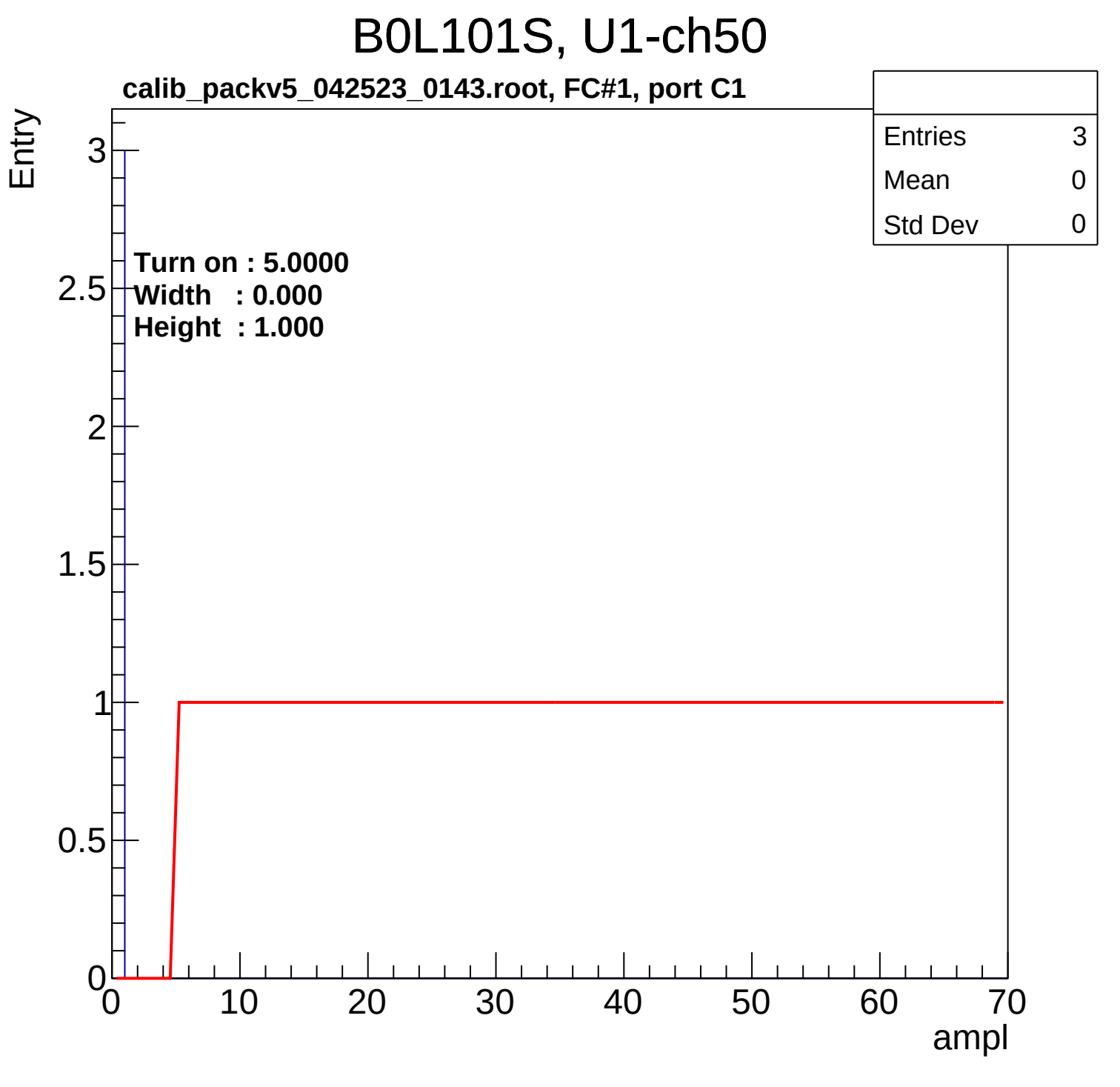

B0L101S, U1-ch45
calib_packv5_042523_0143.root, FC#1, port C1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

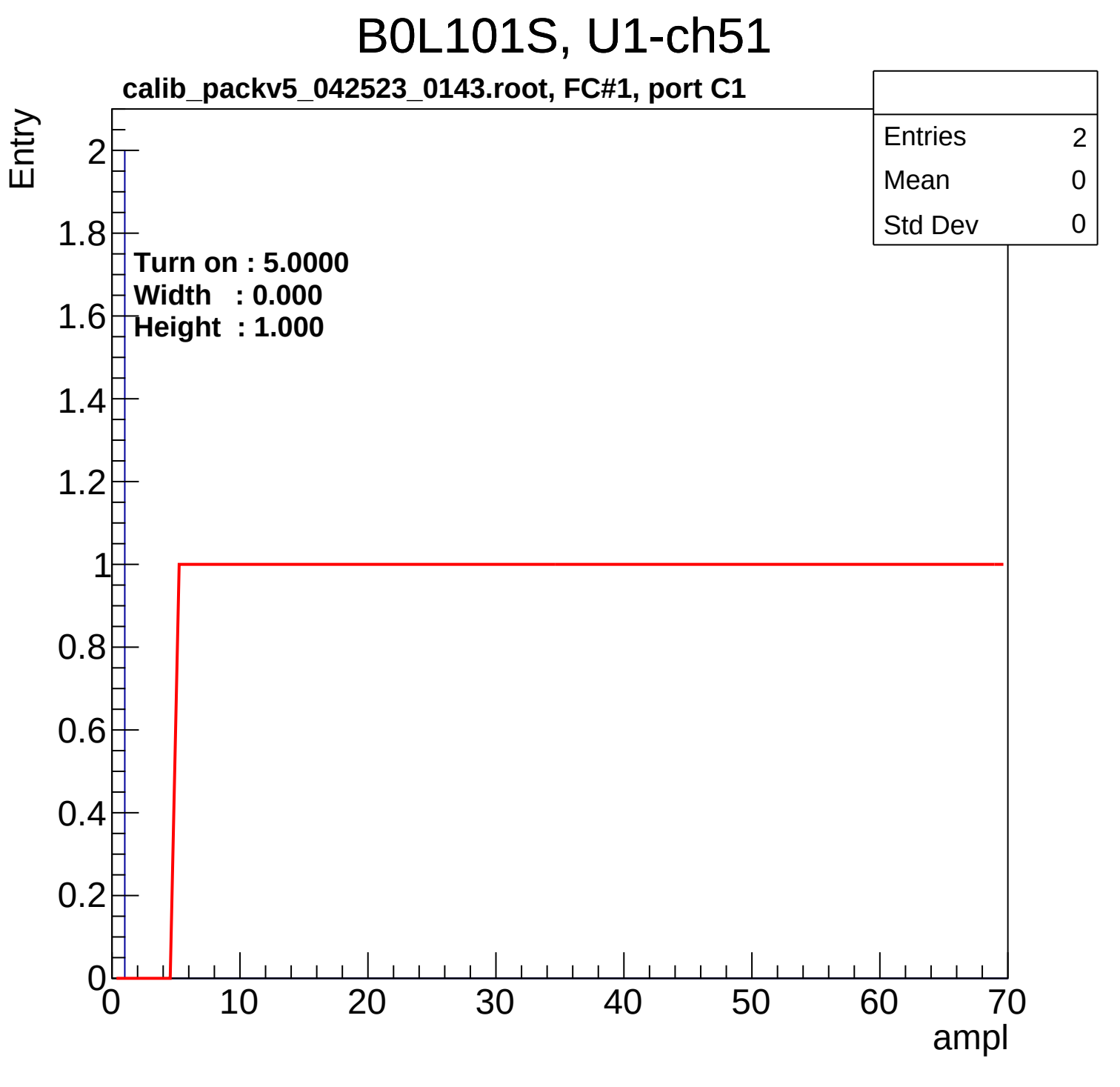

B0L101S, U1-ch46
calib_packv5_042523_0143.root, FC#1, port C1
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

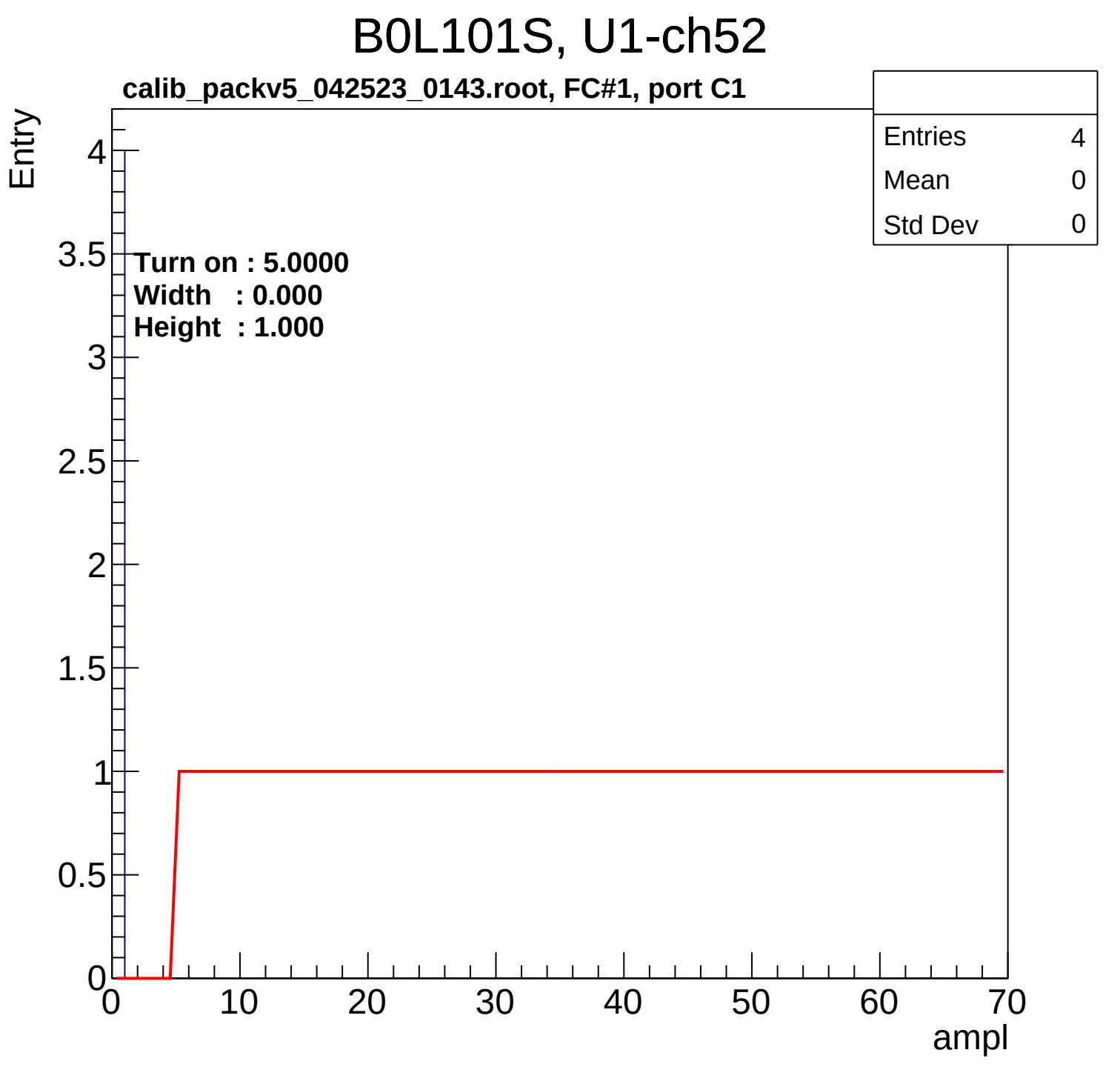

B0L101S, U1-ch47
calib_packv5_042523_0143.root, FC#1, port C1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

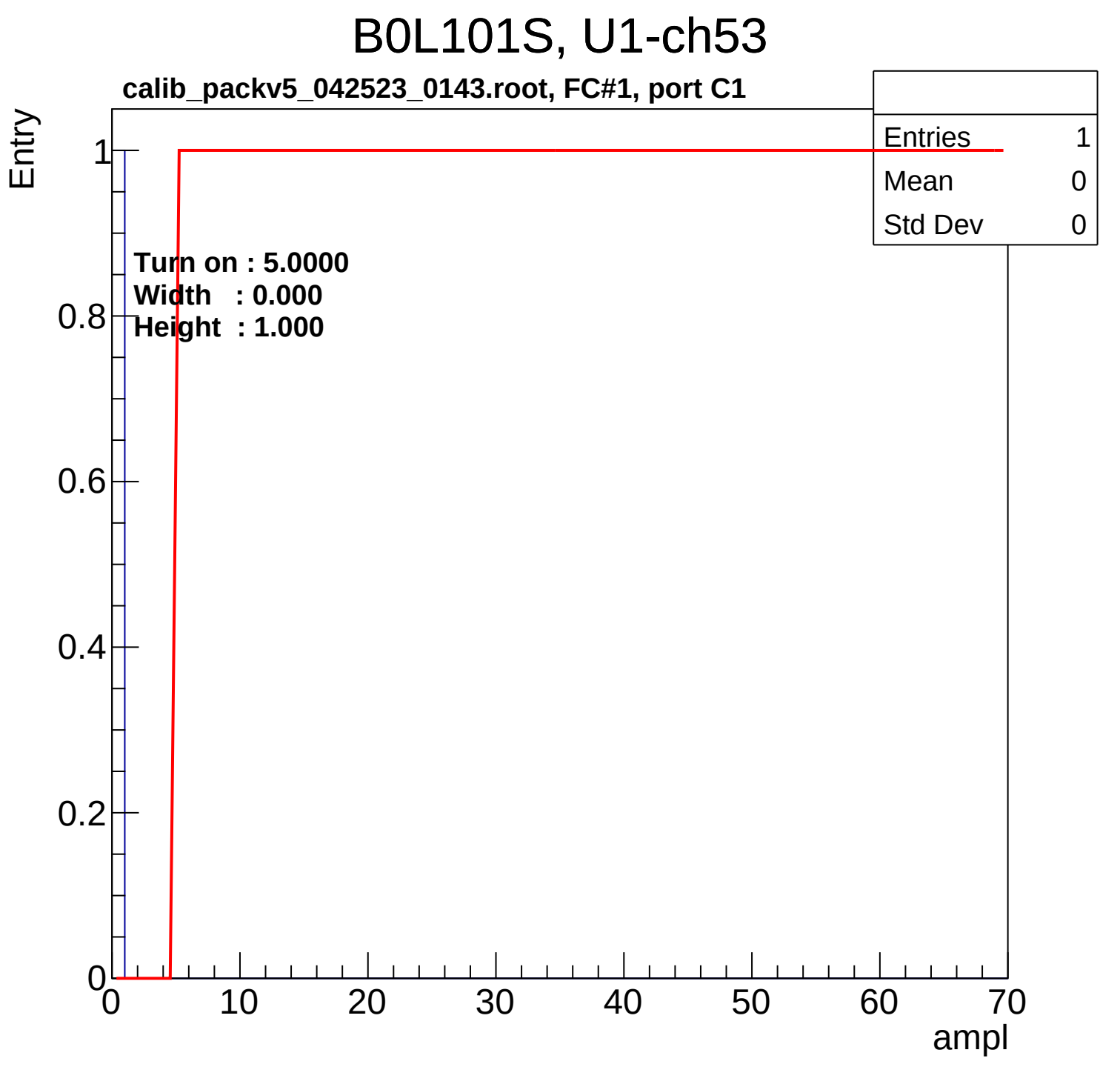

B0L101S, U1-ch48
calib_packv5_042523_0143.root, FC#1, port C1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

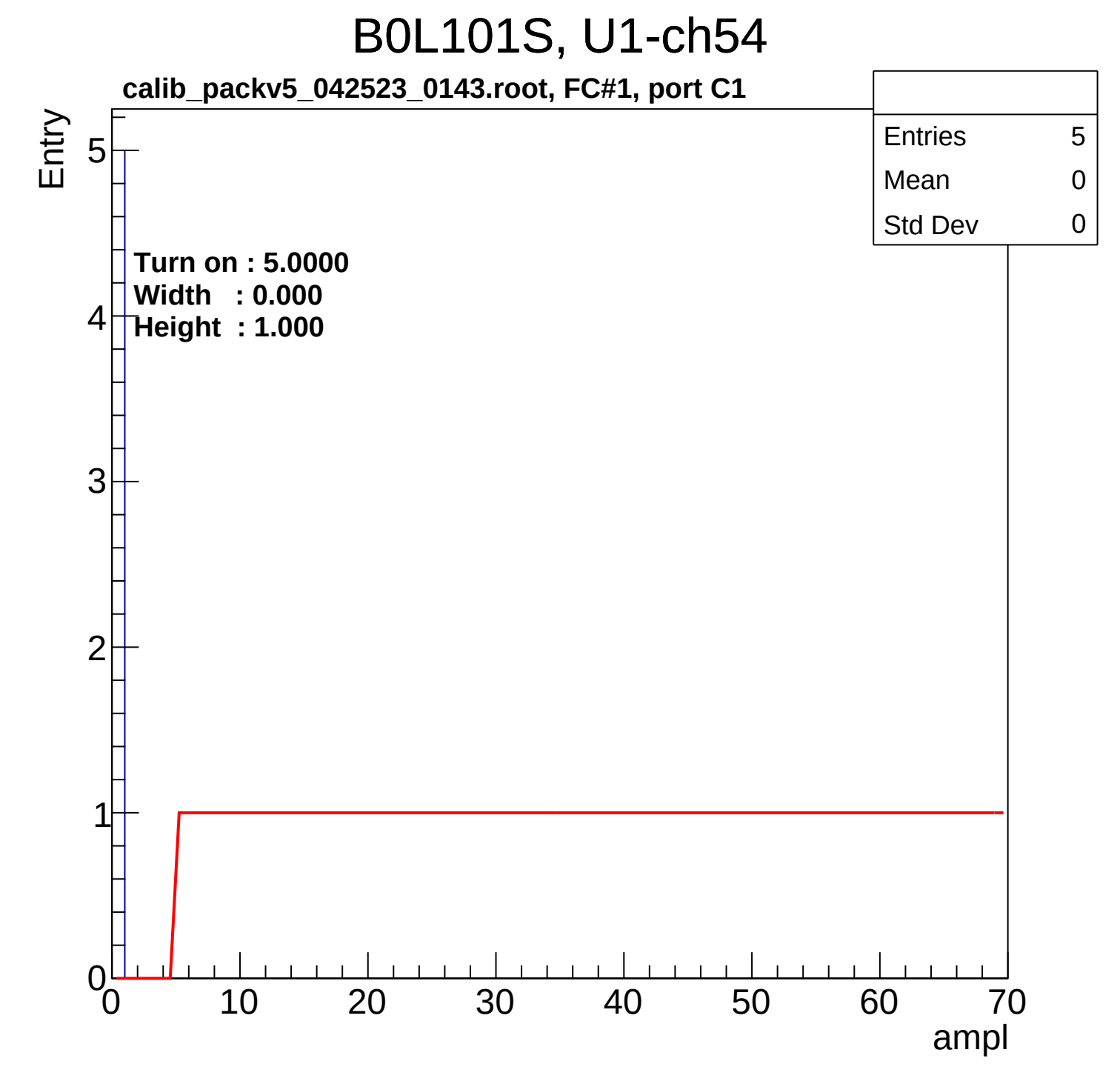

B0L101S, U1-ch49
calib_packv5_042523_0143.root, FC#1, port C1
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

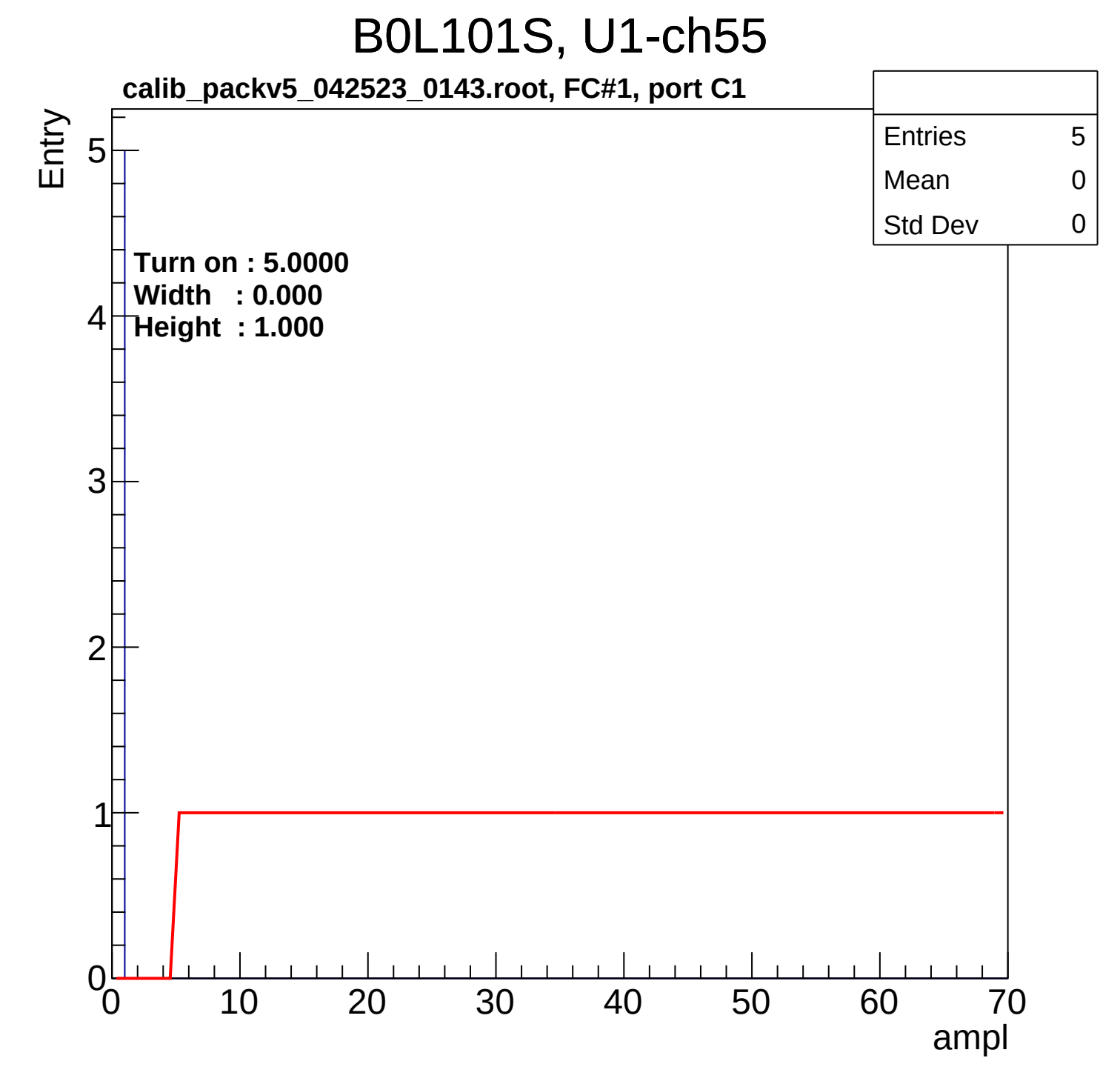

B0L101S, U1-ch50
calib_packv5_042523_0143.root, FC#1, port C1
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

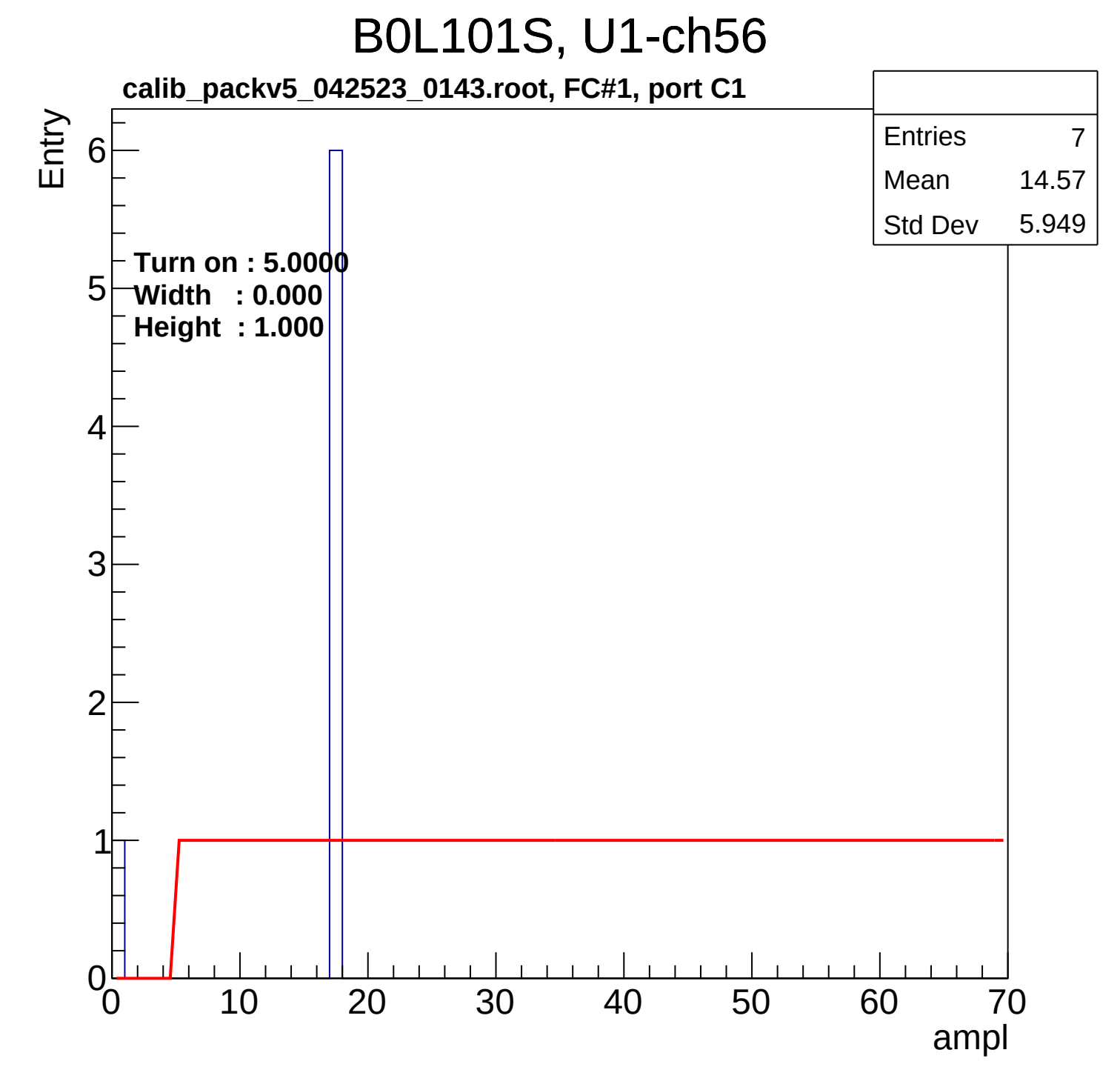

B0L101S, U1-ch51
calib_packv5_042523_0143.root, FC#1, port C1
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

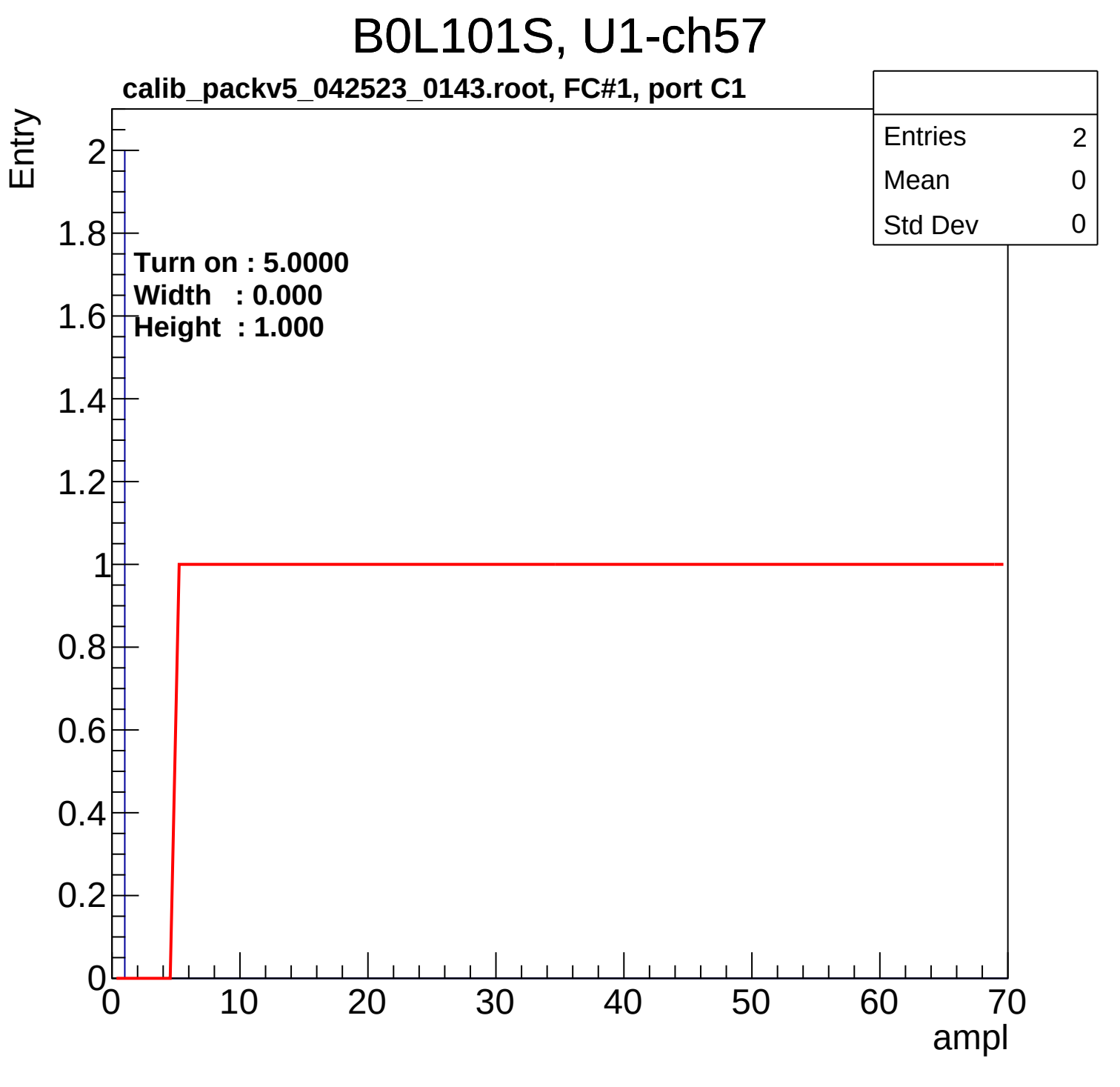

B0L101S, U1-ch52
calib_packv5_042523_0143.root, FC#1, port C1
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

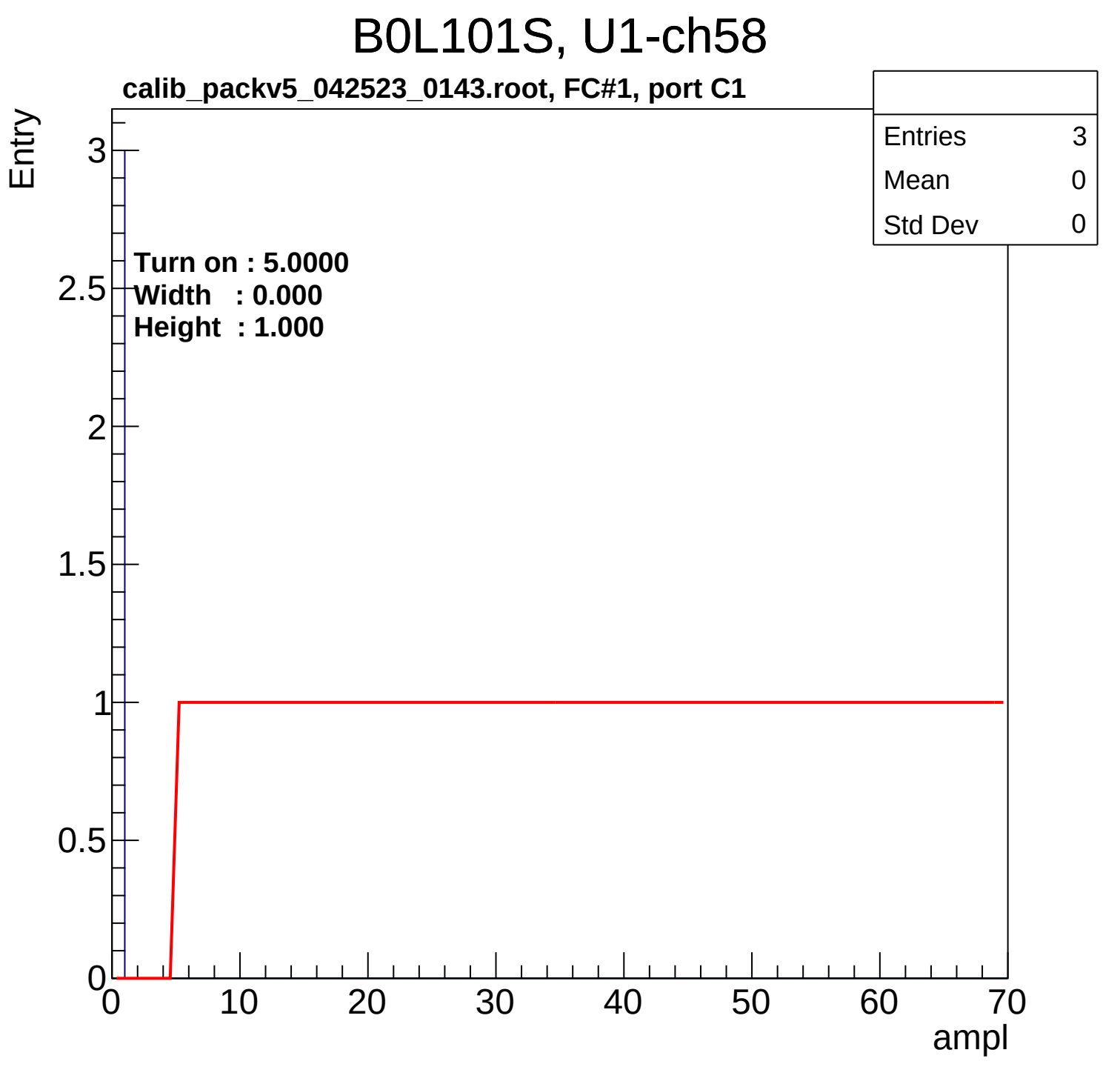

B0L101S, U1-ch53
calib_packv5_042523_0143.root, FC#1, port C1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

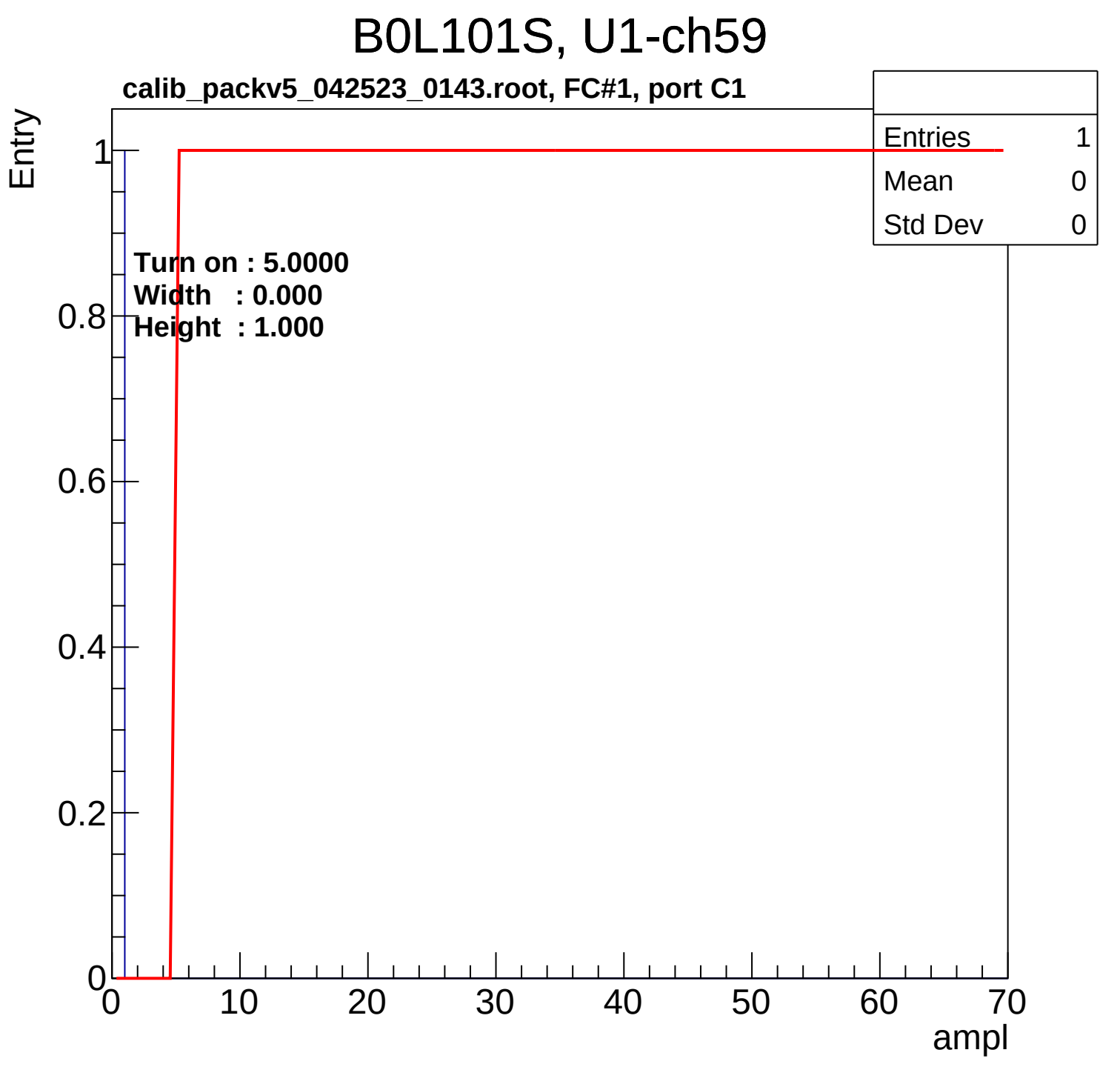

B0L101S, U1-ch54
calib_packv5_042523_0143.root, FC#1, port C1
Entries 5
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

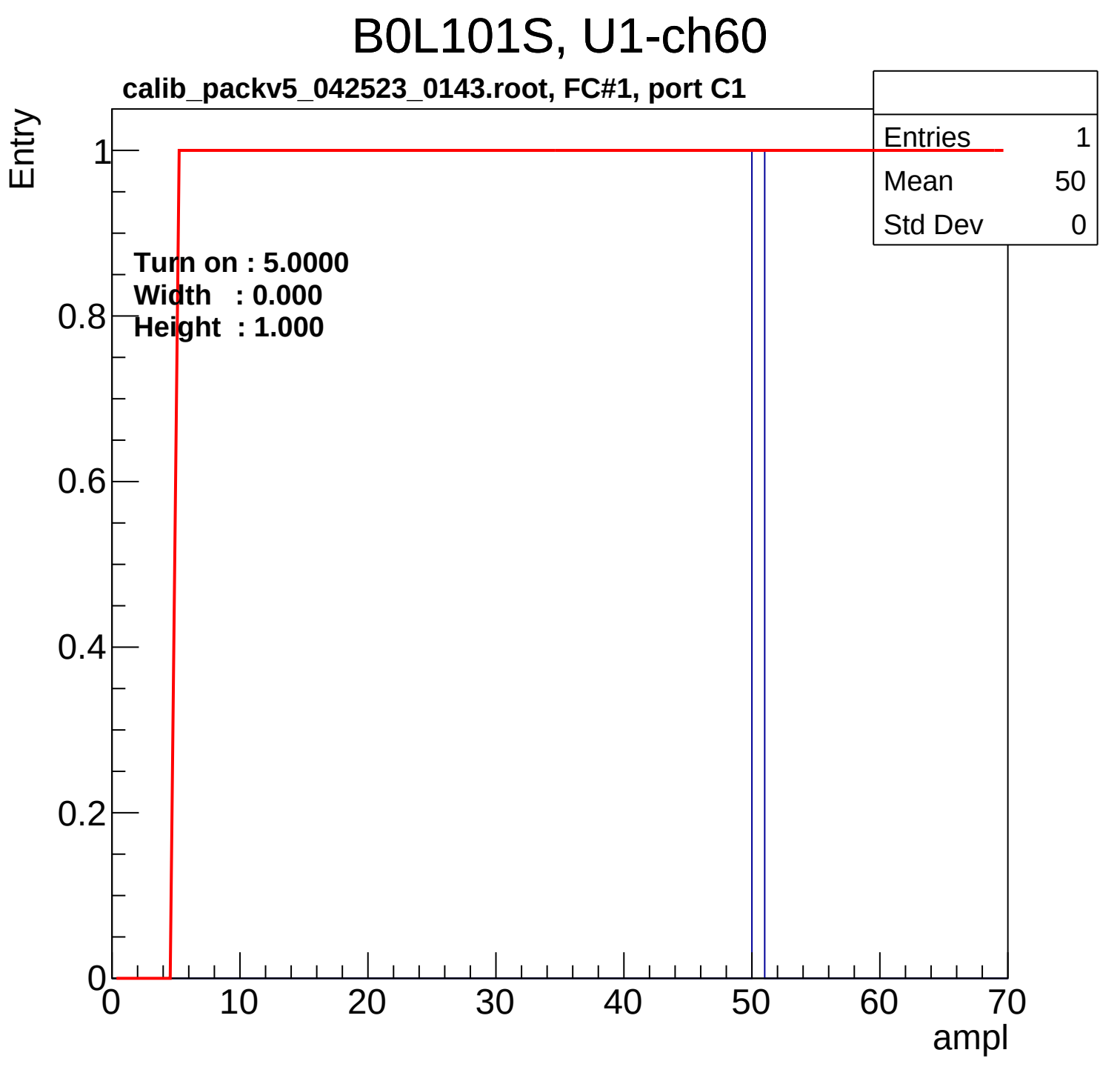

B0L101S, U1-ch55
calib_packv5_042523_0143.root, FC#1, port C1
Entries 5
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

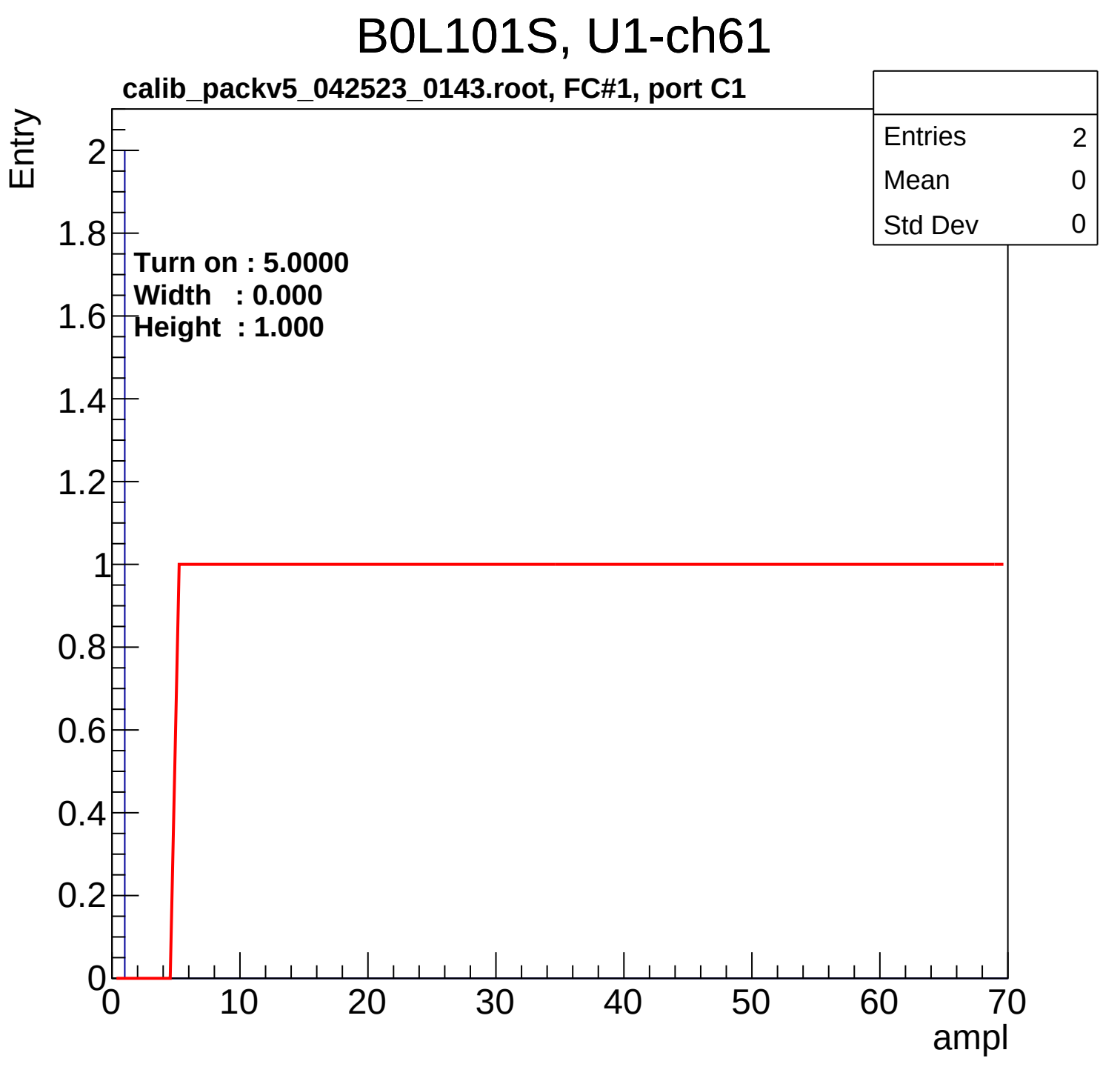

B0L101S, U1-ch56
calib_packv5_042523_0143.root, FC#1, port C1
Entries 7
Mean 14.57
Std Dev 5.949
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

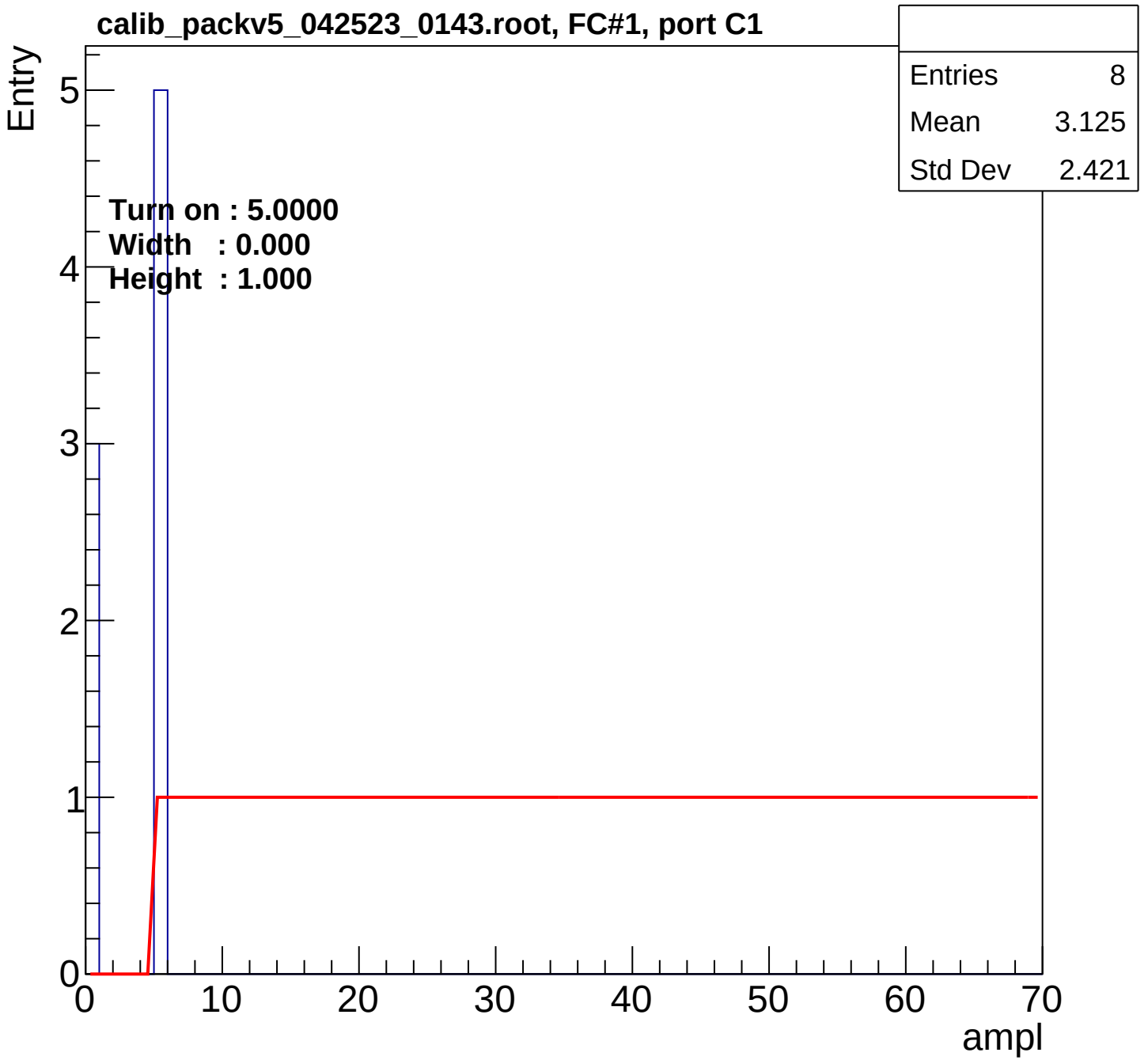

B0L101S, U1-ch57
calib_packv5_042523_0143.root, FC#1, port C1
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

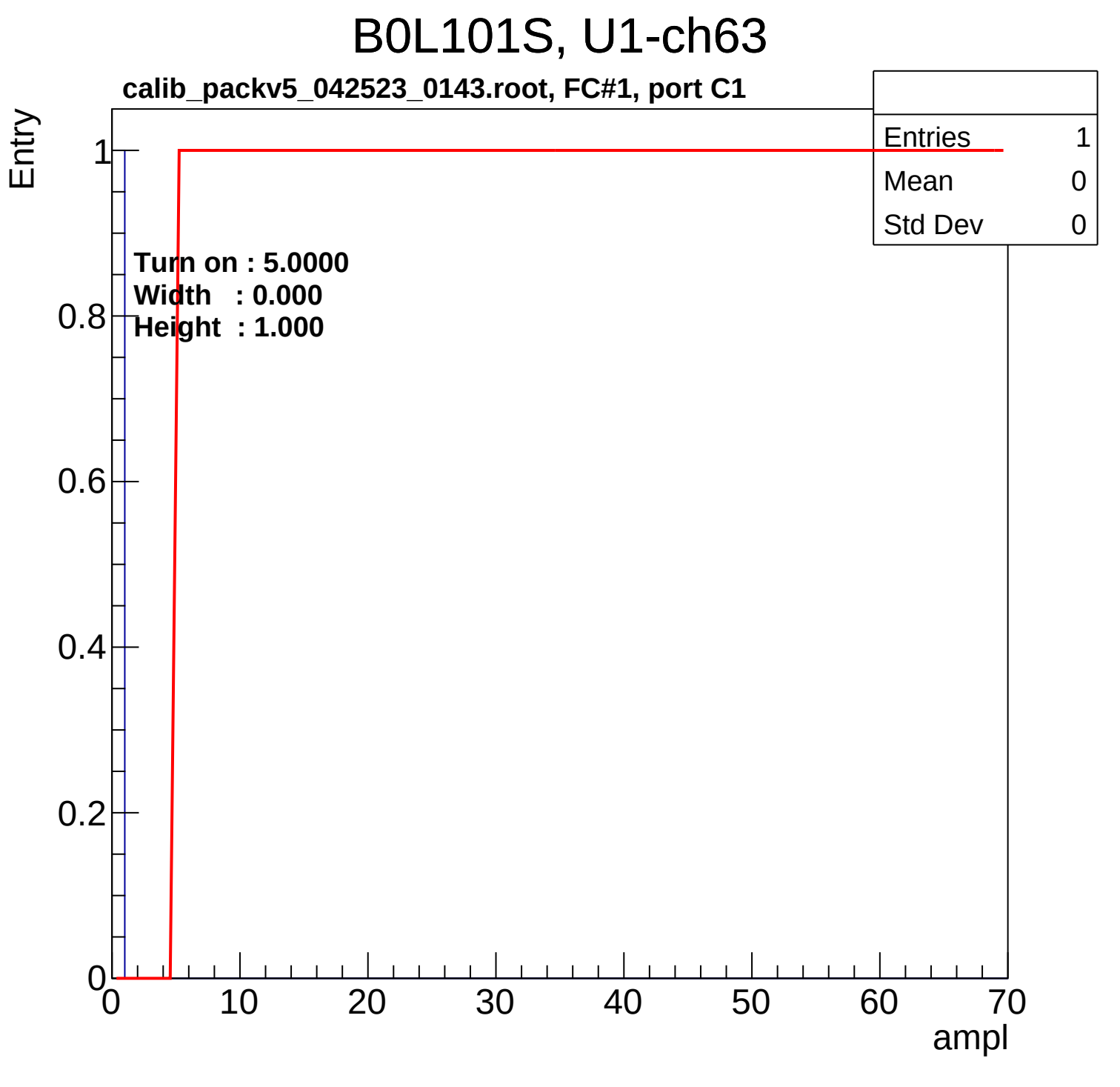

B0L101S, U1-ch58
calib_packv5_042523_0143.root, FC#1, port C1
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

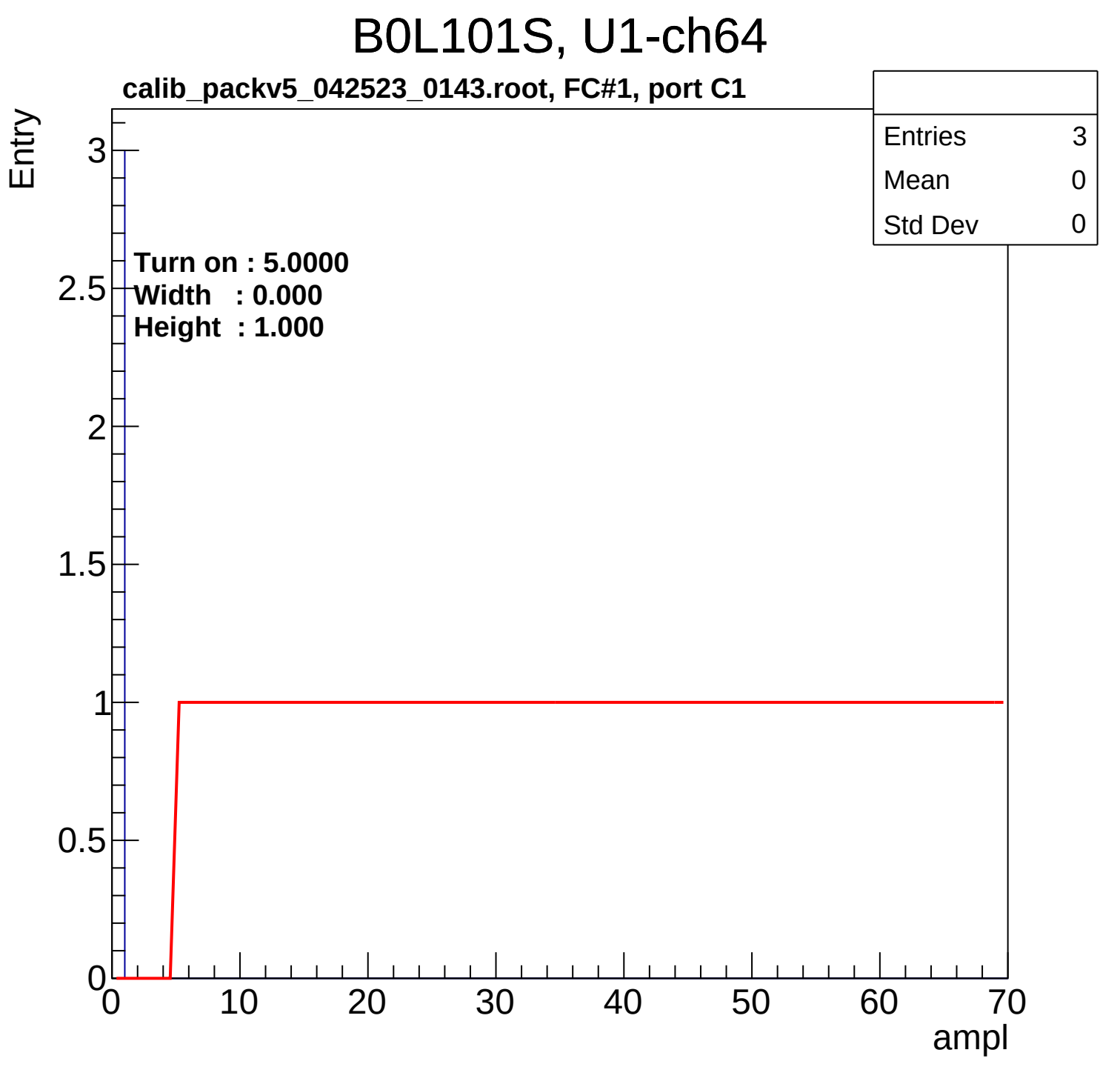

B0L101S, U1-ch59
calib_packv5_042523_0143.root, FC#1, port C1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

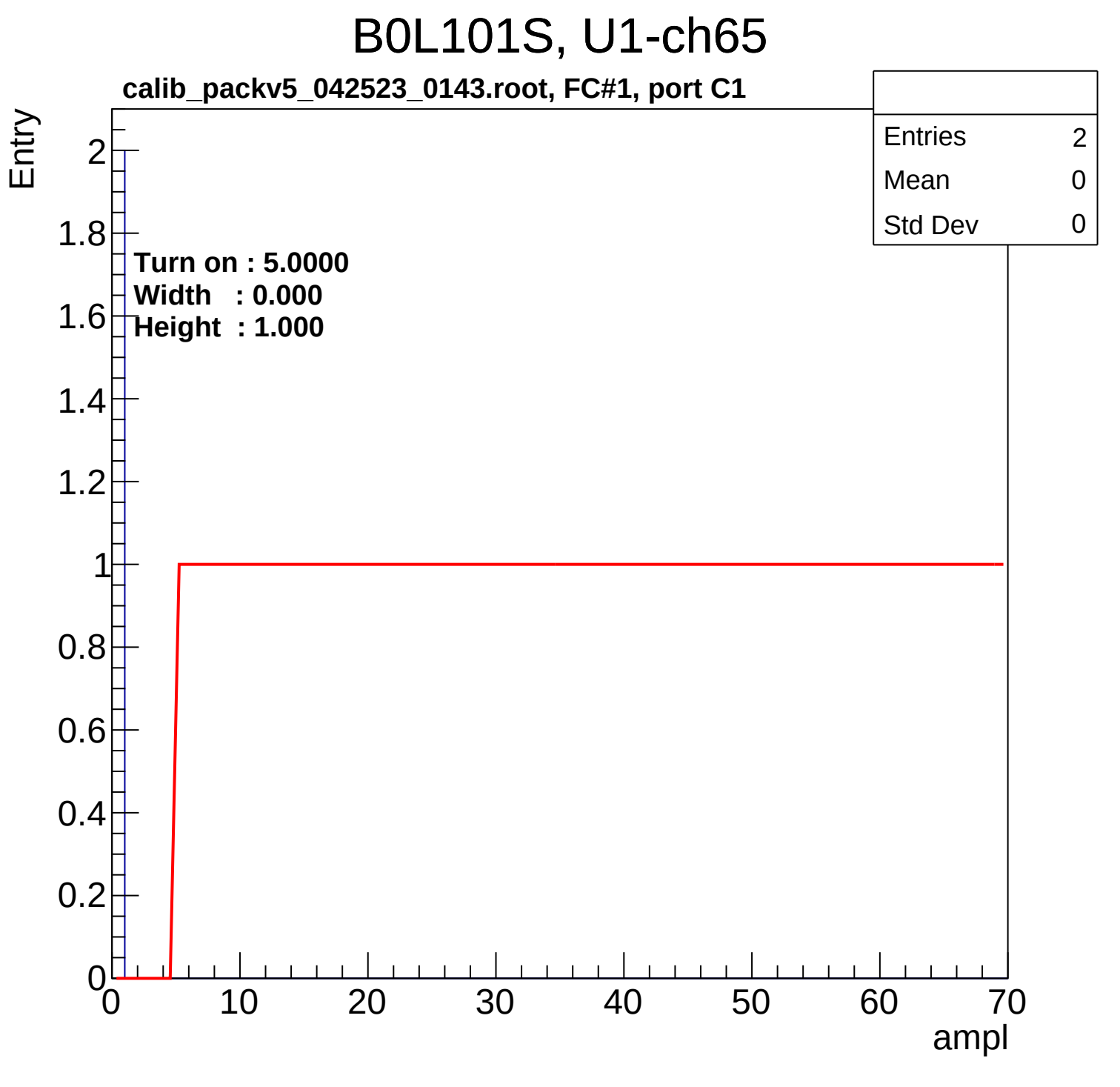

B0L101S, U1-ch60
calib_packv5_042523_0143.root, FC#1, port C1
Entries 1
Mean 50
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

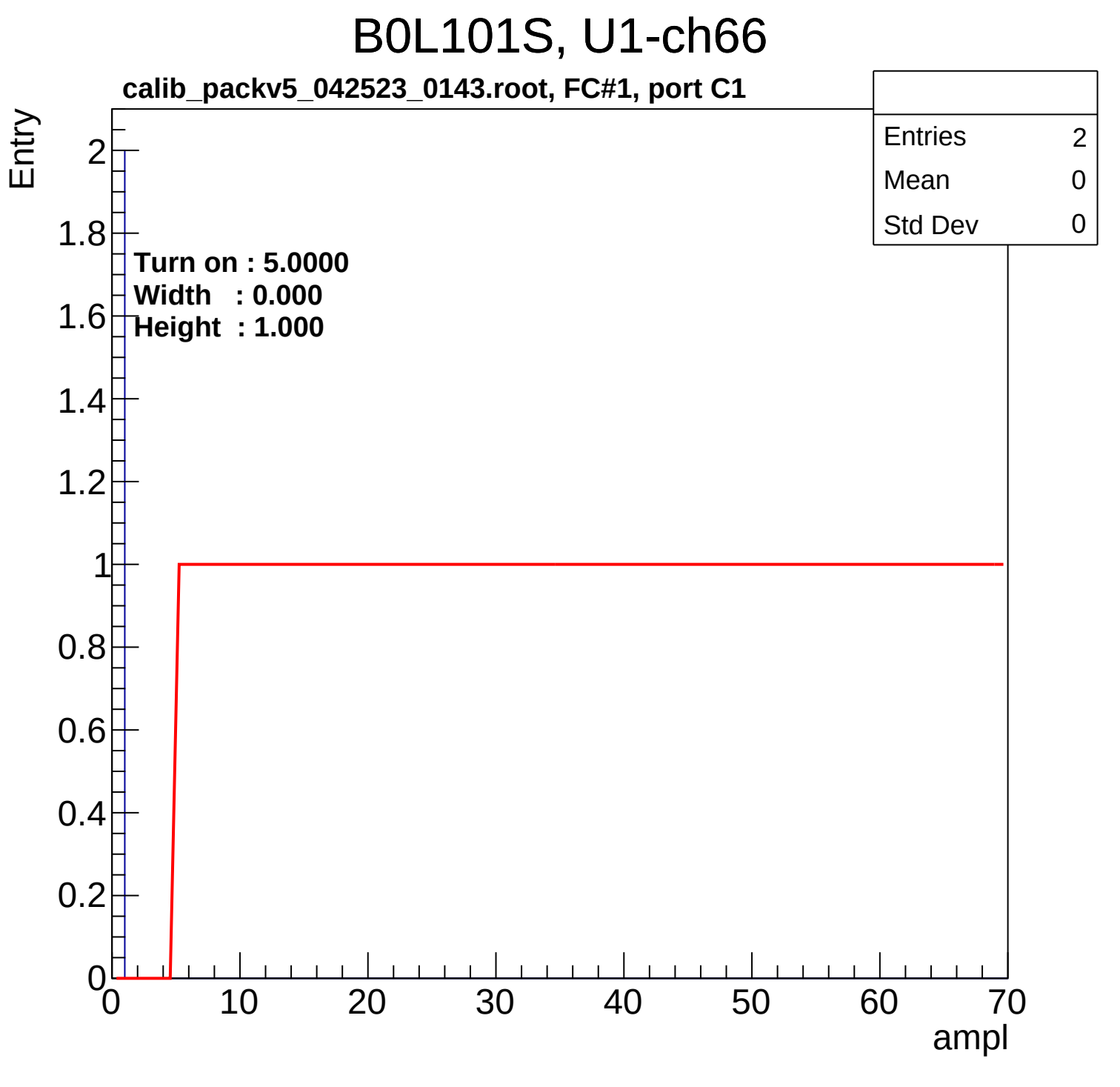

B0L101S, U1-ch61
calib_packv5_042523_0143.root, FC#1, port C1
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

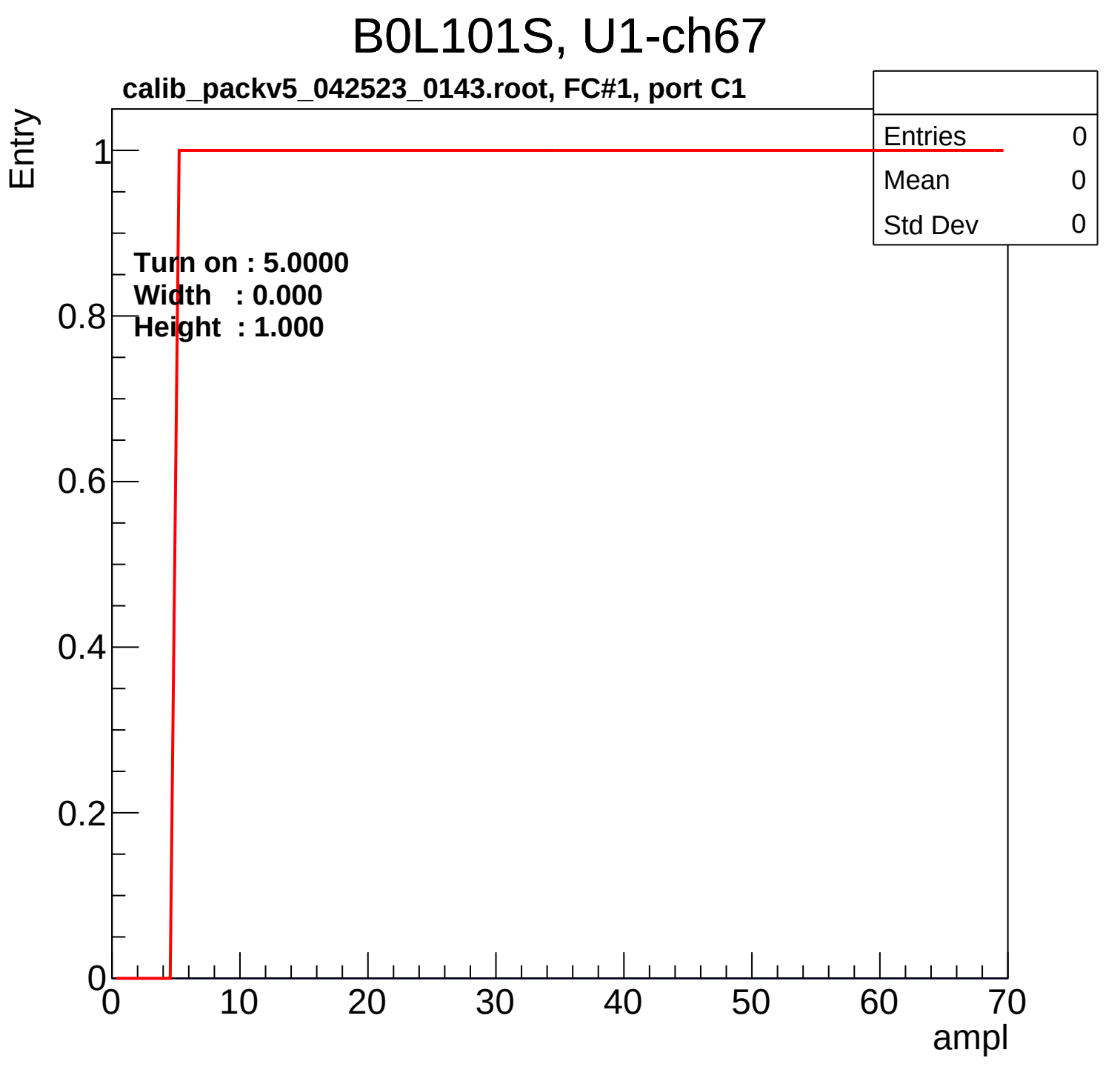

B0L101S, U1-ch62
calib_packv5_042523_0143.root, FC#1, port C1
Entries 8
Mean 3.125
Std Dev 2.421
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

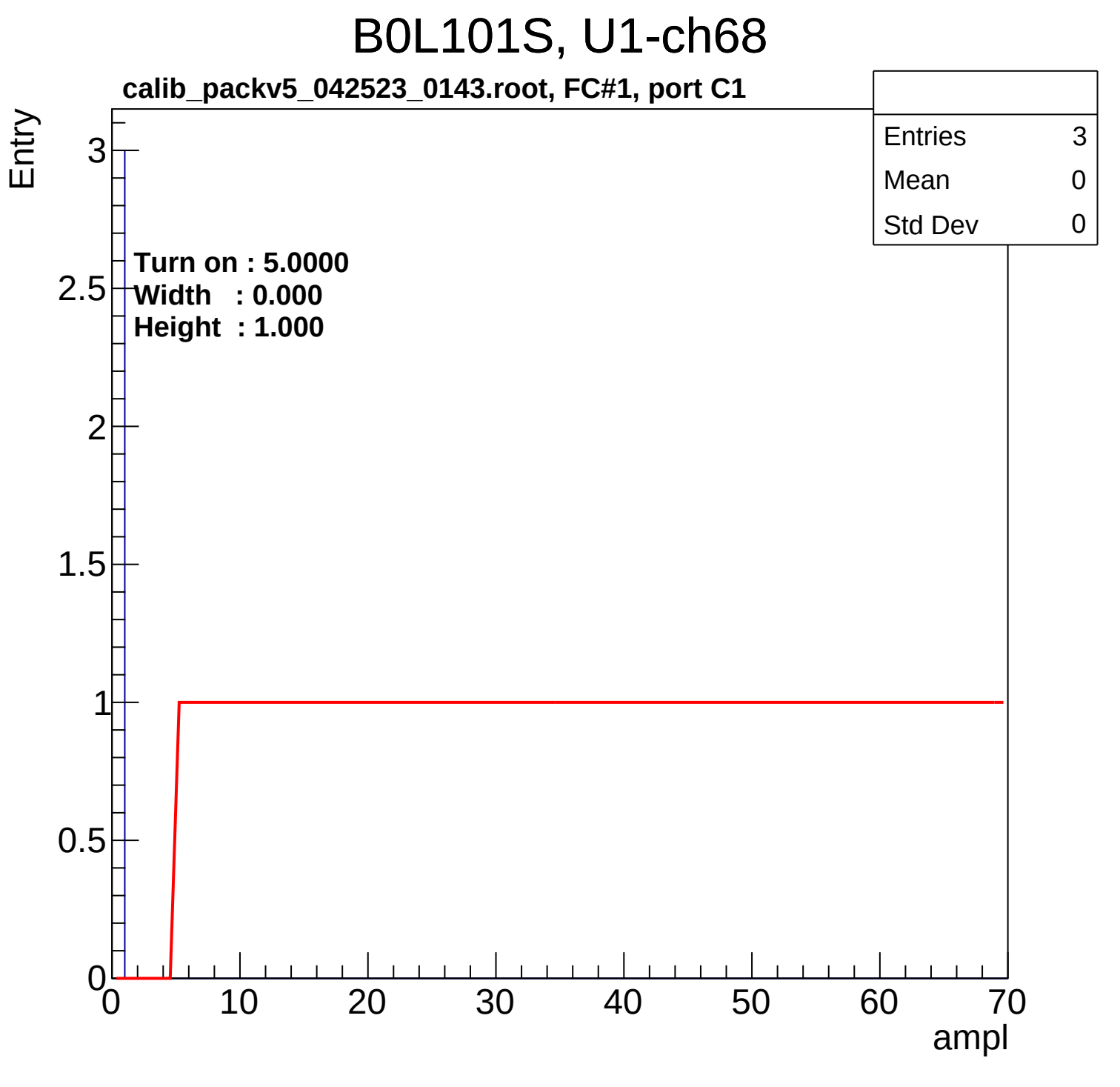

B0L101S, U1-ch63
calib_packv5_042523_0143.root, FC#1, port C1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

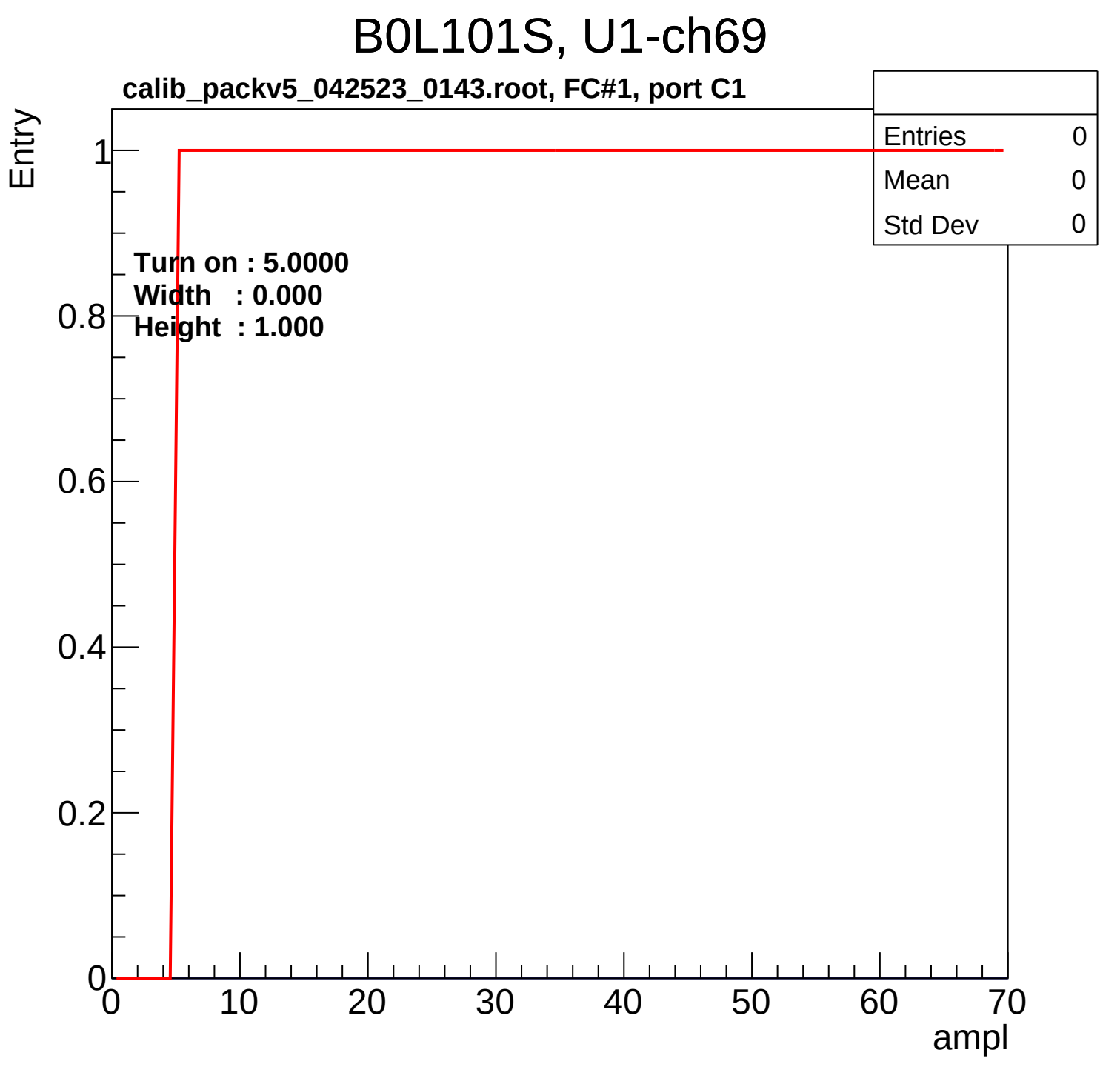

B0L101S, U1-ch64
calib_packv5_042523_0143.root, FC#1, port C1
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

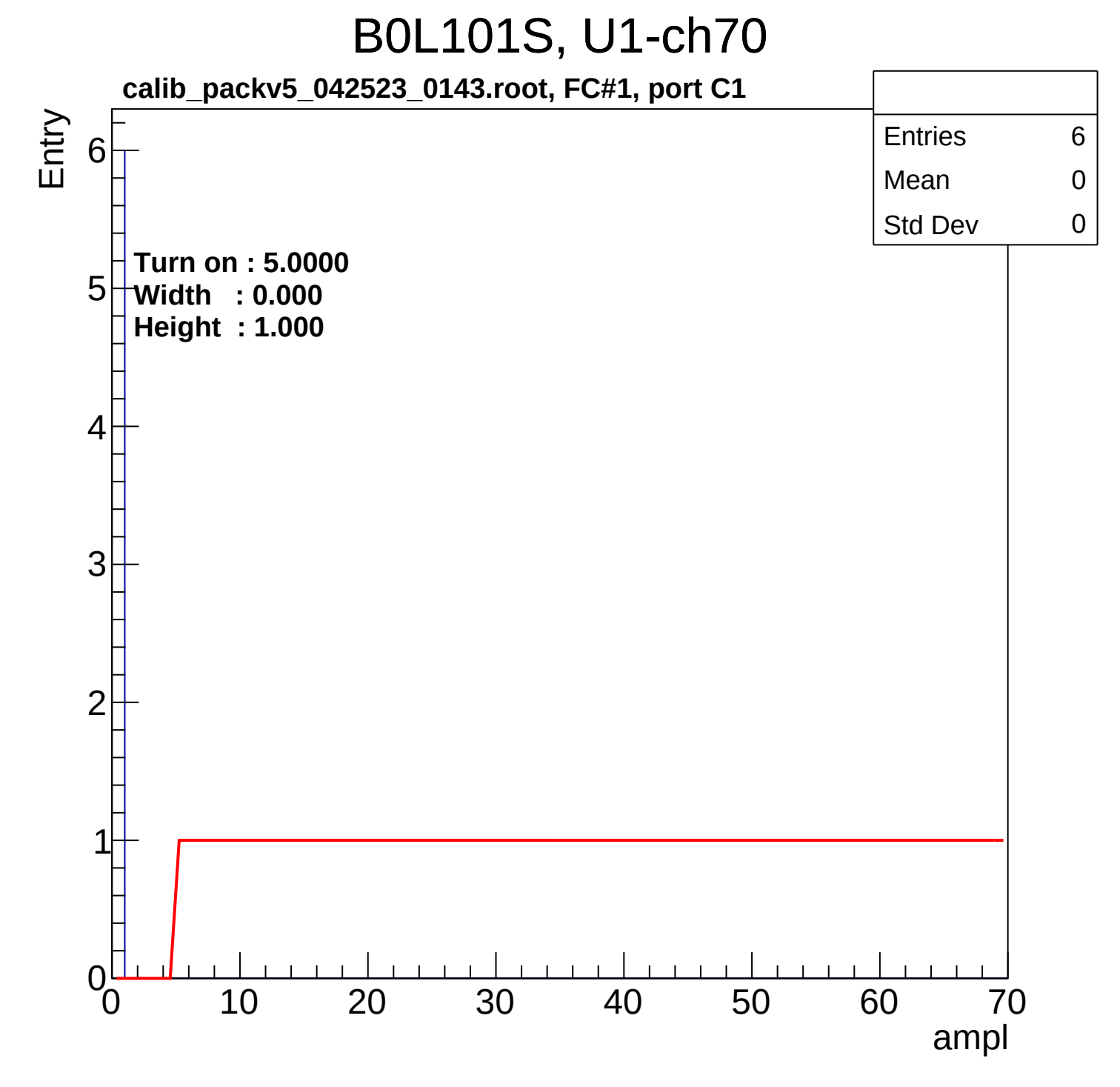

B0L101S, U1-ch65
calib_packv5_042523_0143.root, FC#1, port C1
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

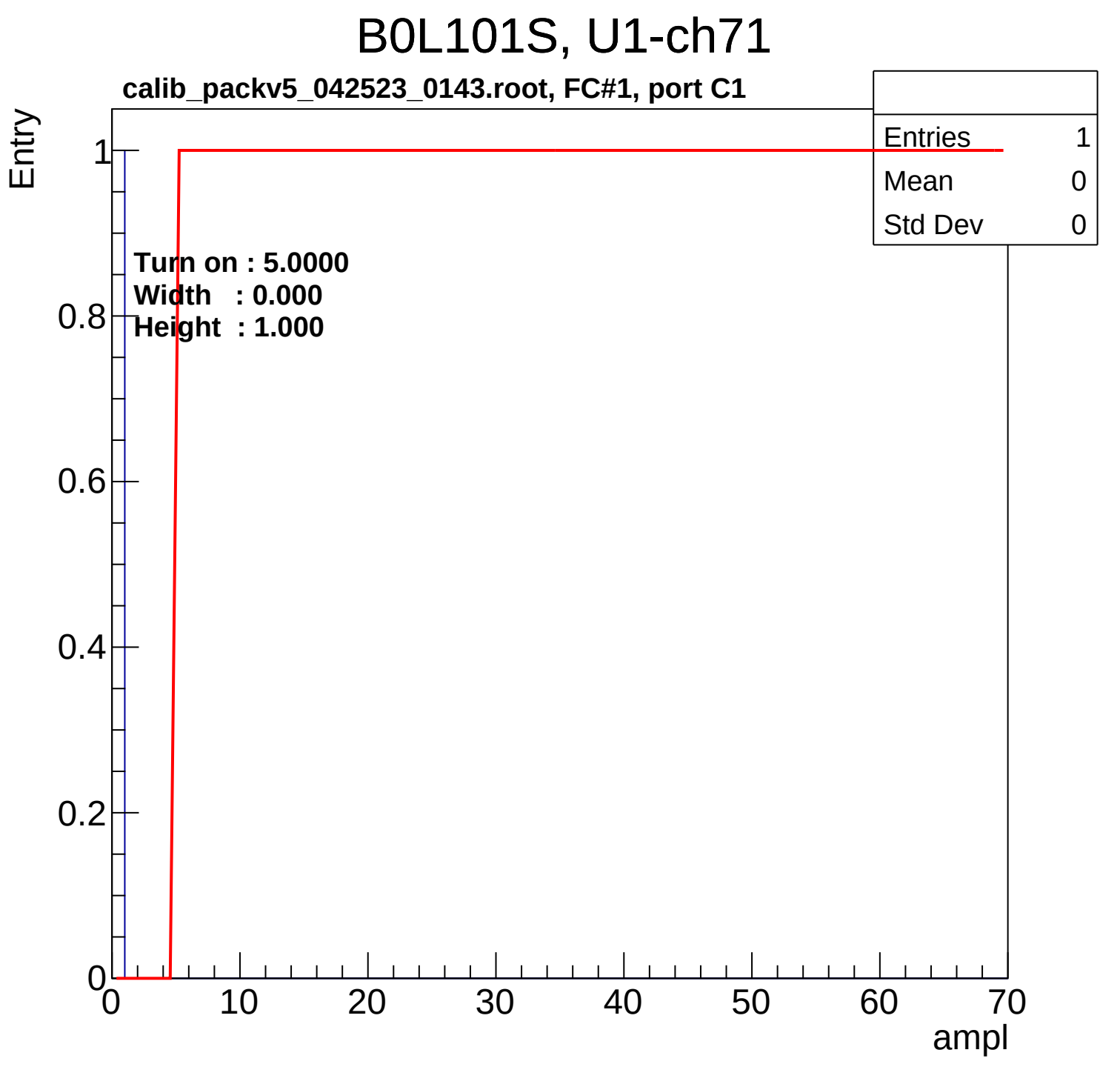

B0L101S, U1-ch66
calib_packv5_042523_0143.root, FC#1, port C1
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

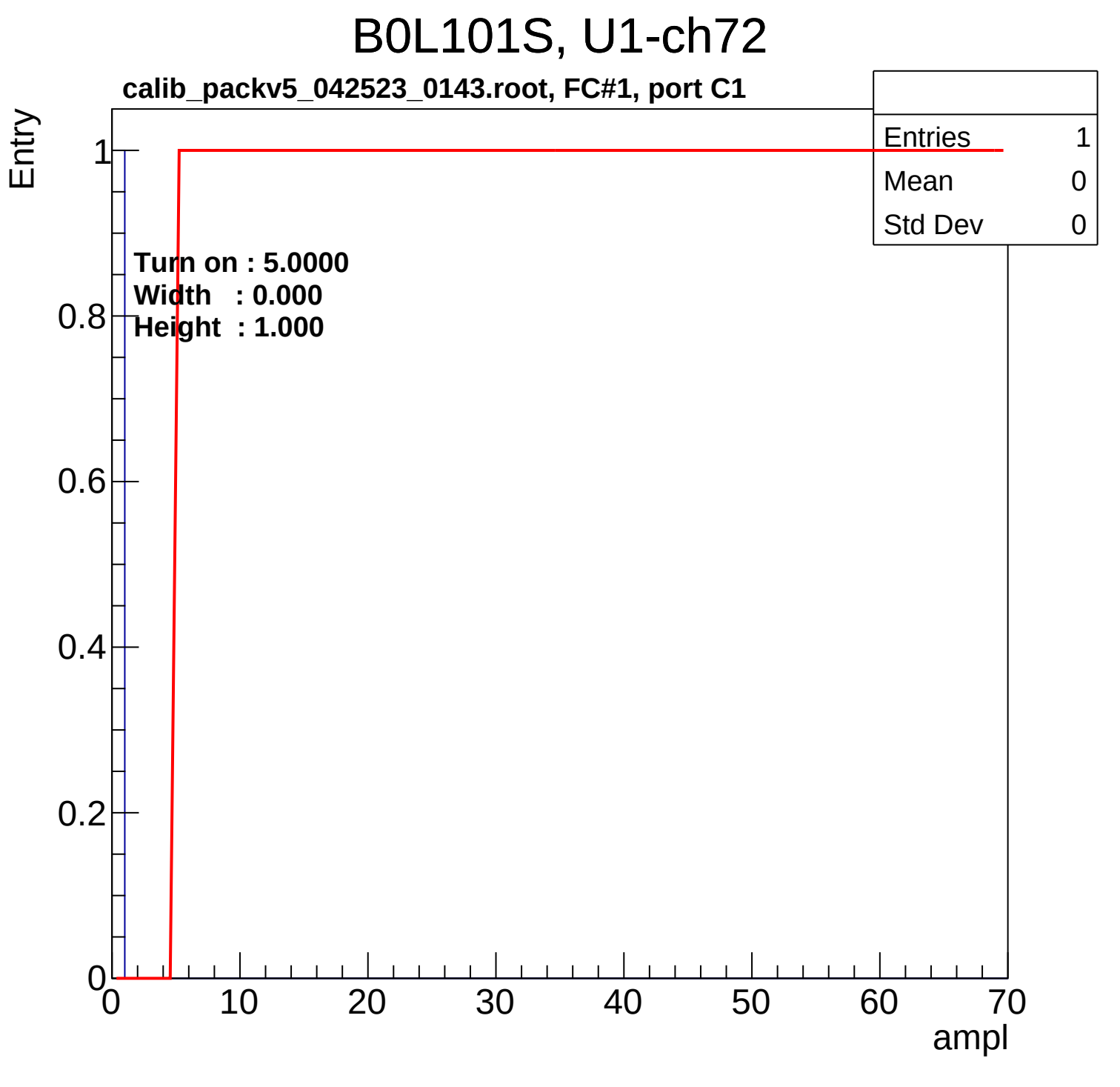

B0L101S, U1-ch67
calib_packv5_042523_0143.root, FC#1, port C1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

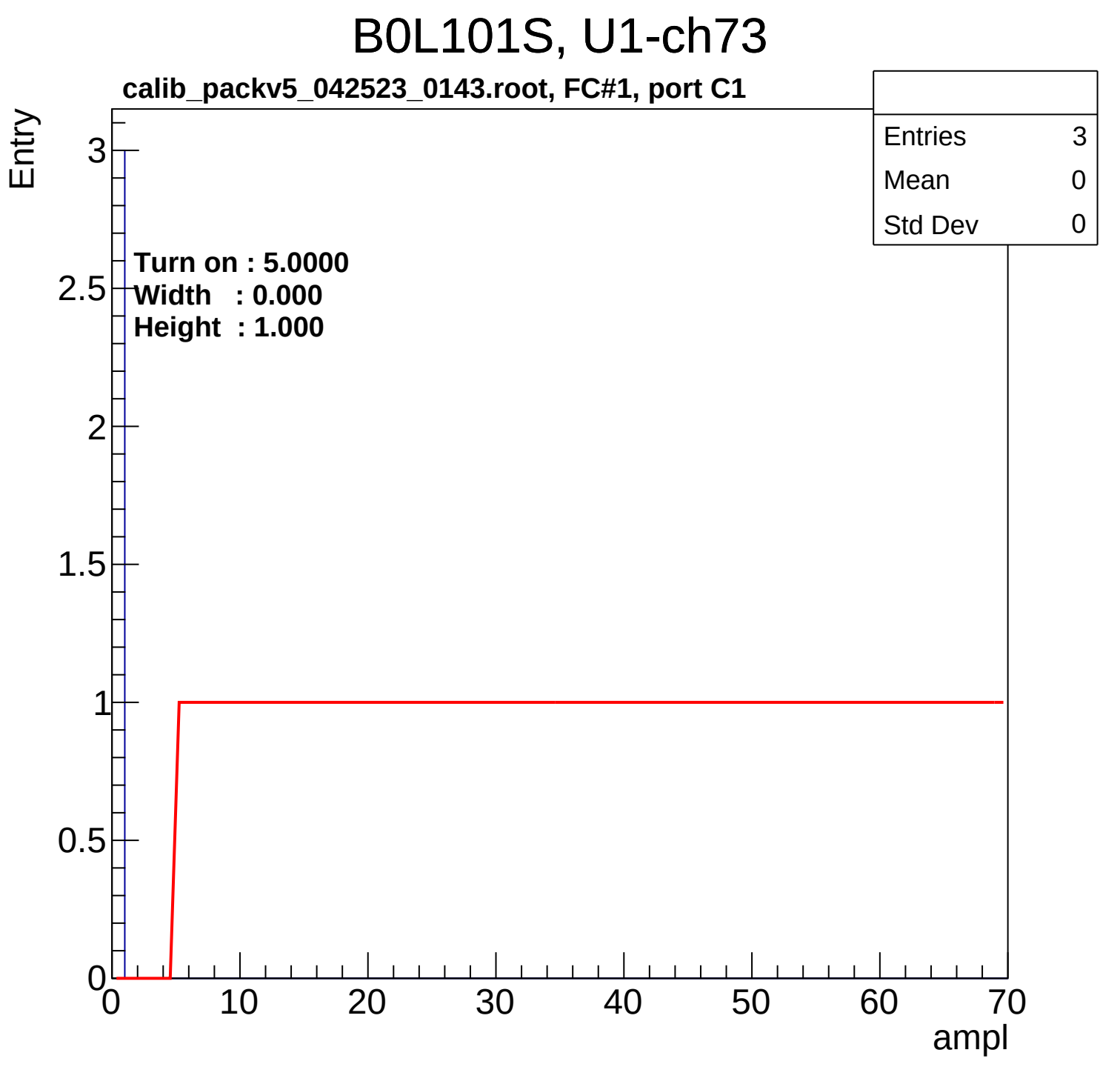

B0L101S, U1-ch68
calib_packv5_042523_0143.root, FC#1, port C1
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

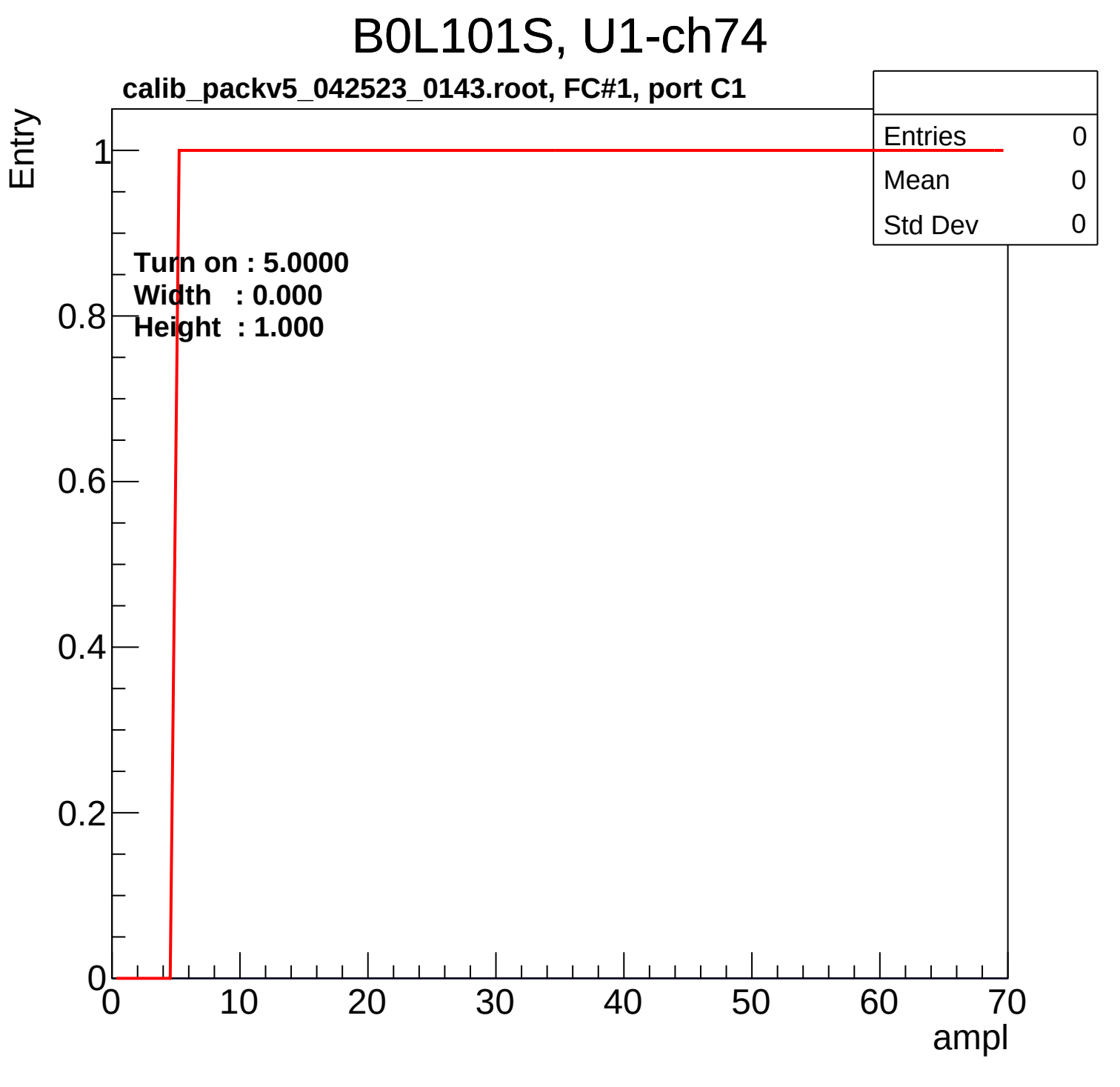

B0L101S, U1-ch69
calib_packv5_042523_0143.root, FC#1, port C1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

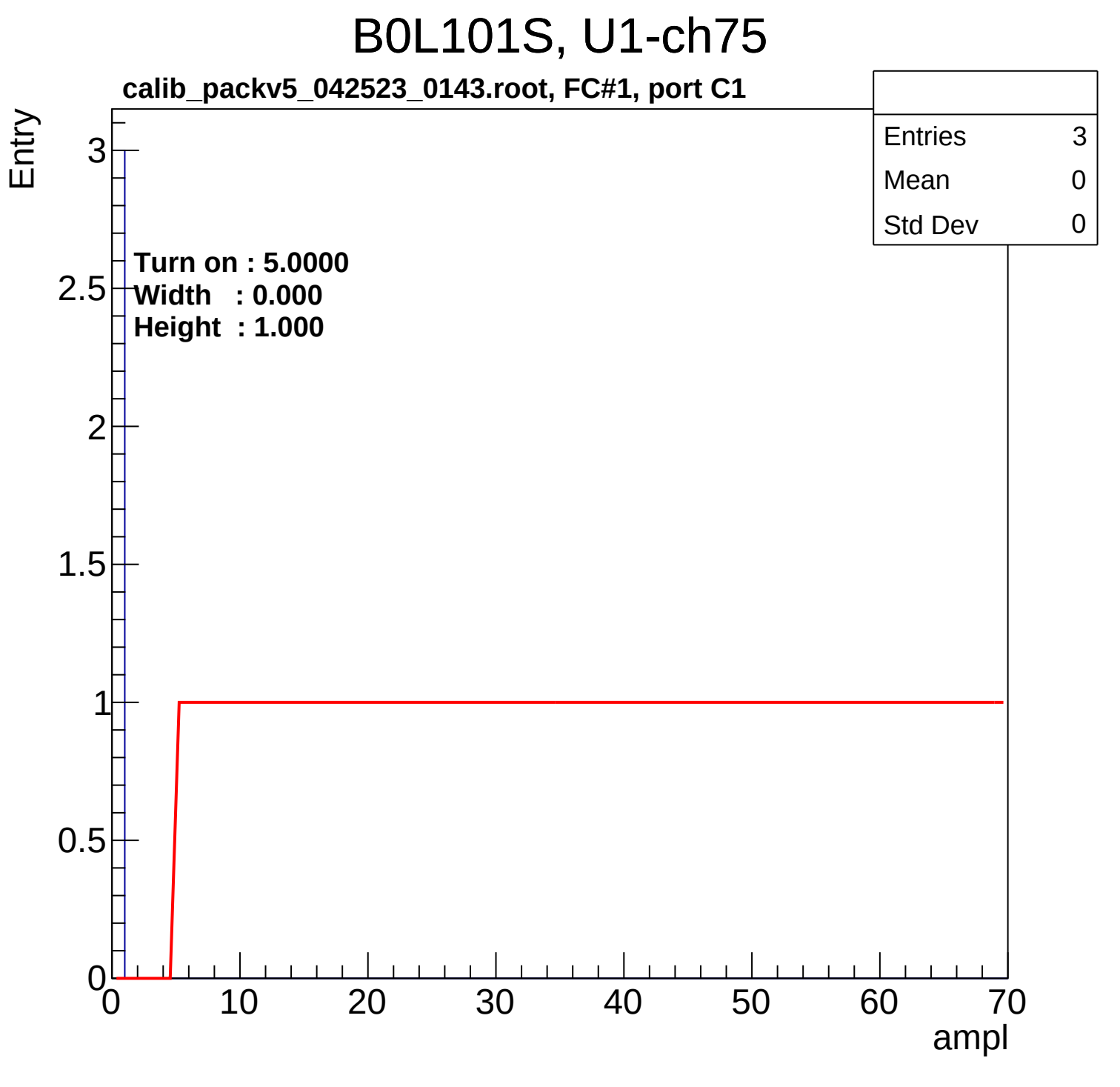

B0L101S, U1-ch70
calib_packv5_042523_0143.root, FC#1, port C1
Entries 6
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

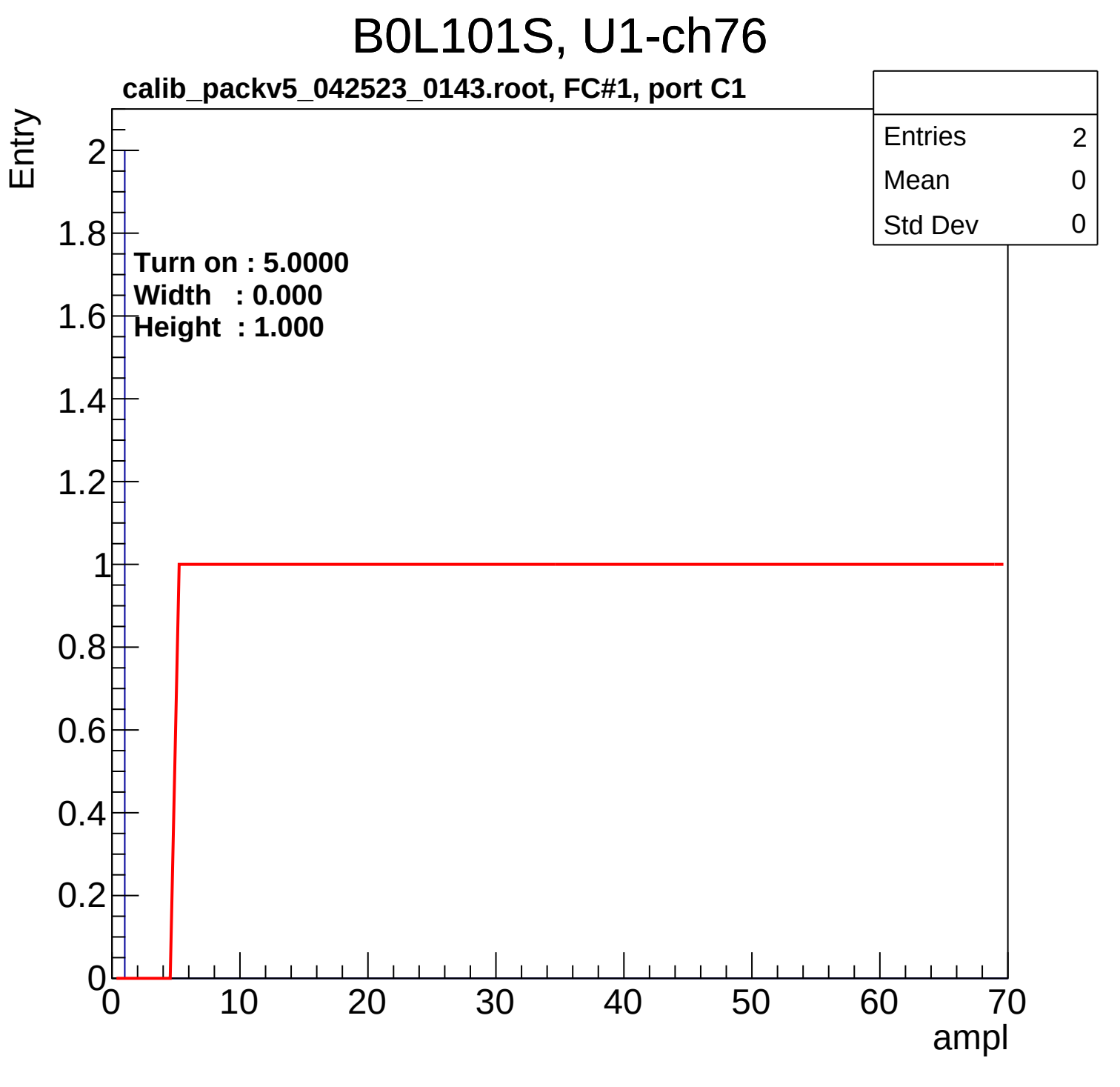

B0L101S, U1-ch71
calib_packv5_042523_0143.root, FC#1, port C1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

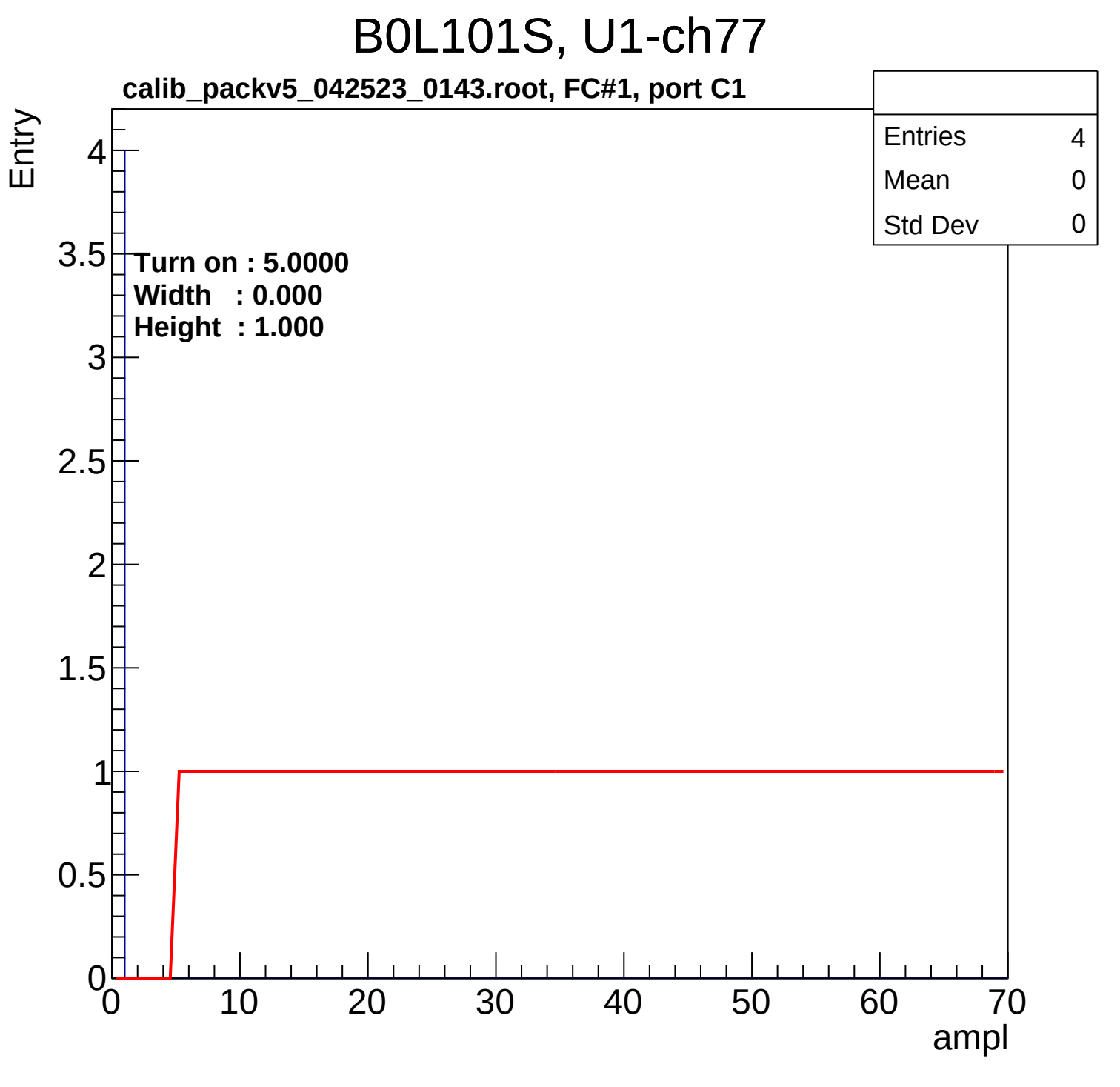

B0L101S, U1-ch72
calib_packv5_042523_0143.root, FC#1, port C1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

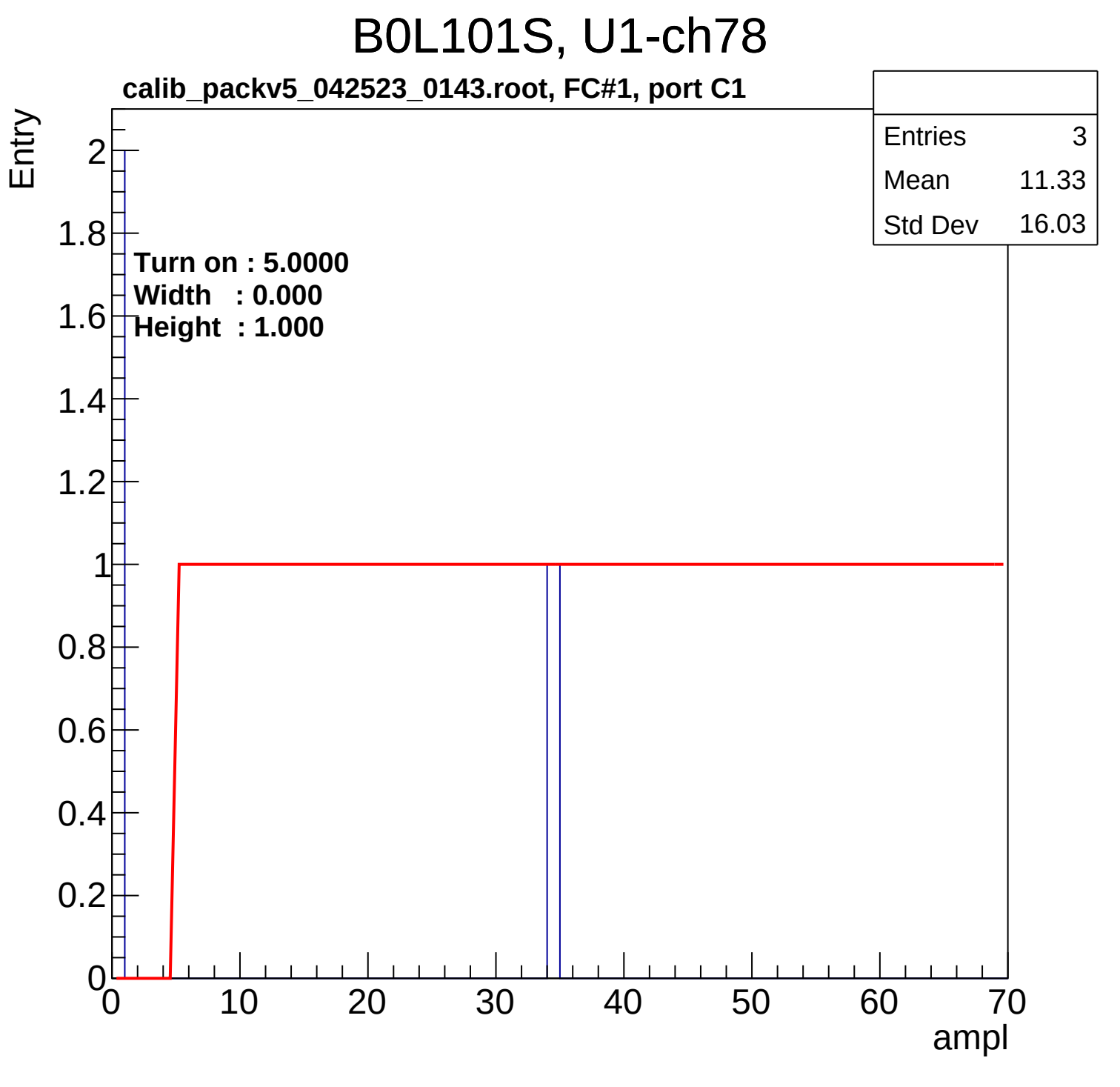

B0L101S, U1-ch73
calib_packv5_042523_0143.root, FC#1, port C1
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

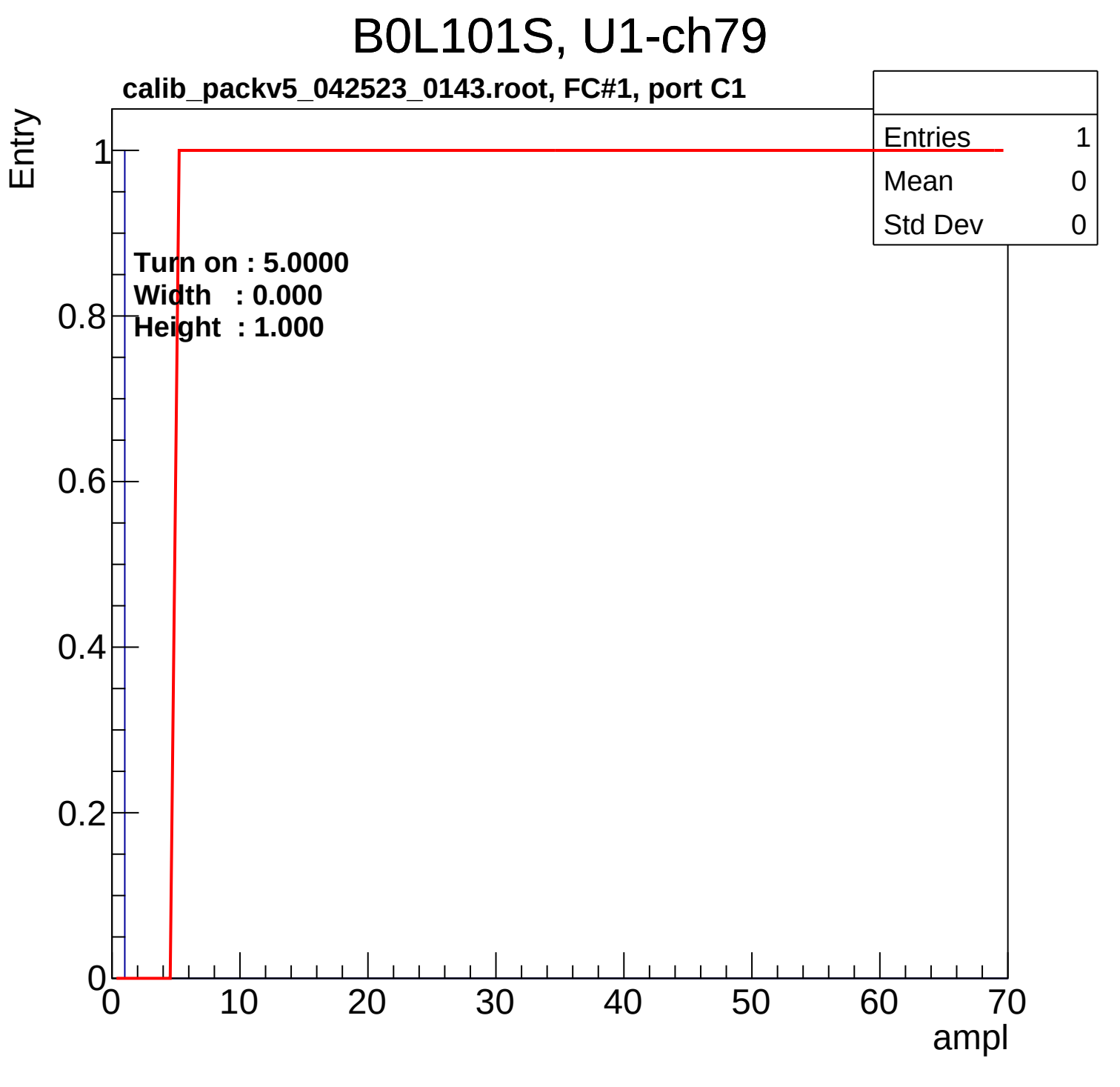

B0L101S, U1-ch74
calib_packv5_042523_0143.root, FC#1, port C1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

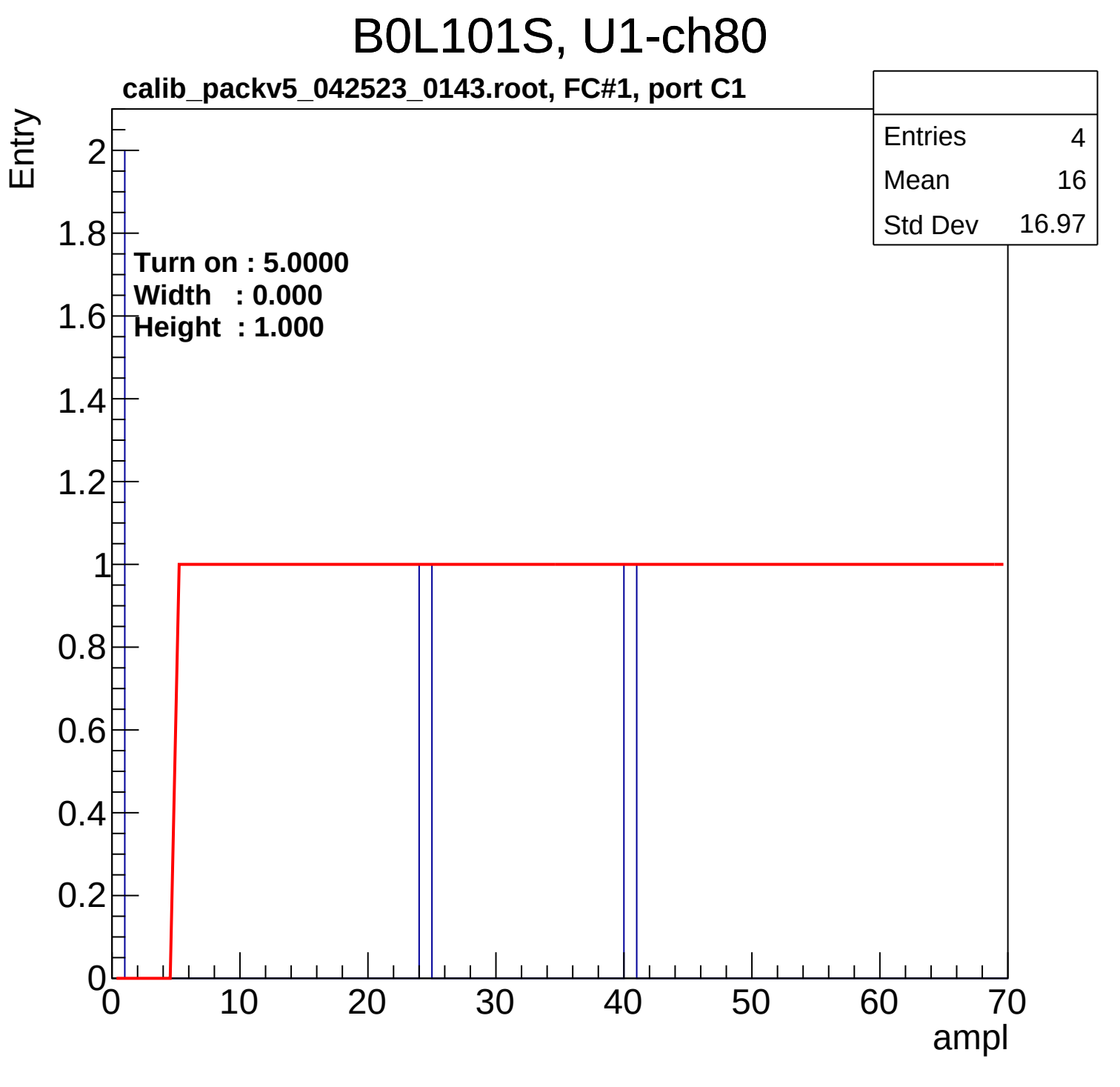

B0L101S, U1-ch75
calib_packv5_042523_0143.root, FC#1, port C1
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

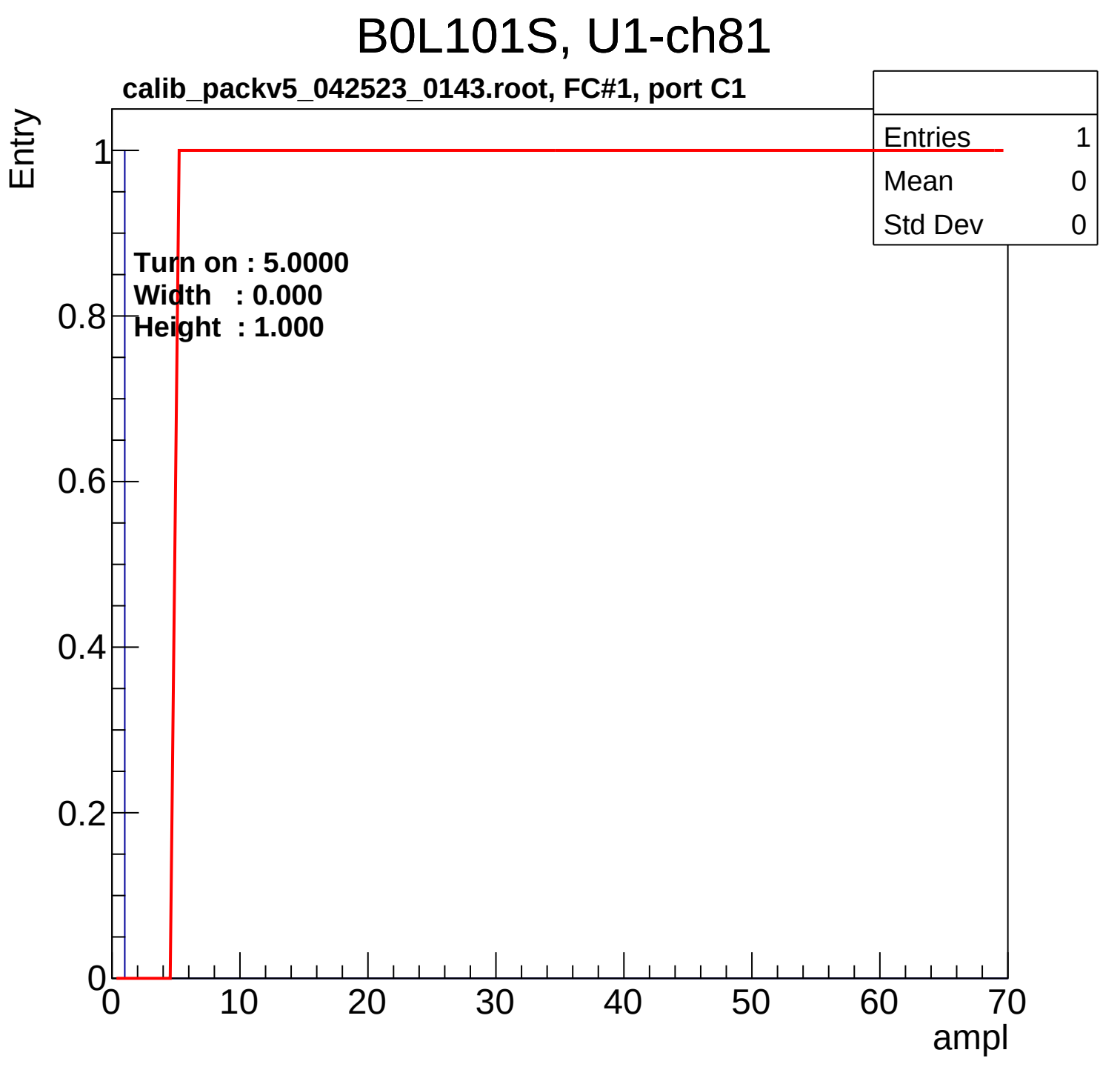

B0L101S, U1-ch76
calib_packv5_042523_0143.root, FC#1, port C1
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

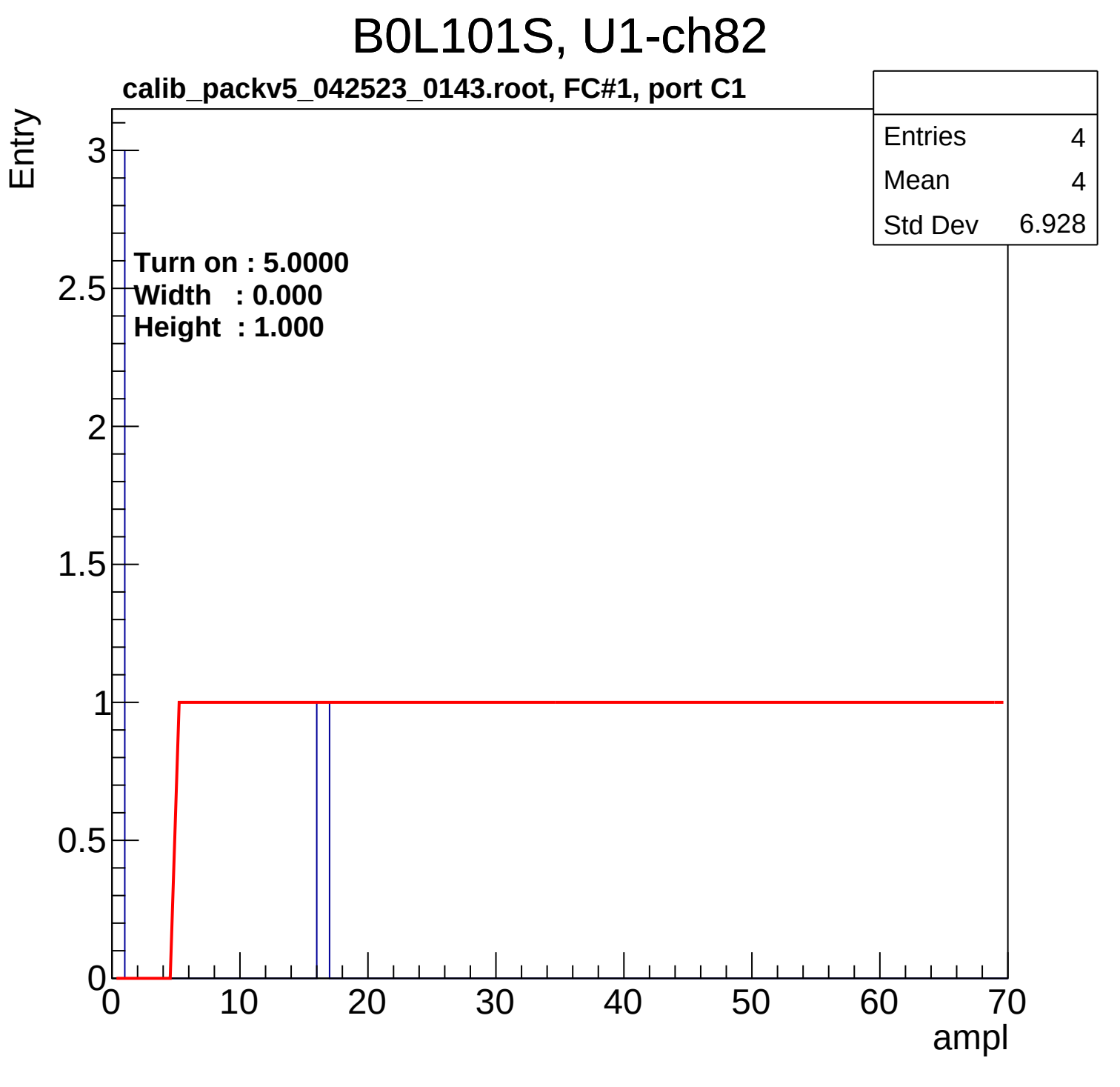

B0L101S, U1-ch77
calib_packv5_042523_0143.root, FC#1, port C1
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

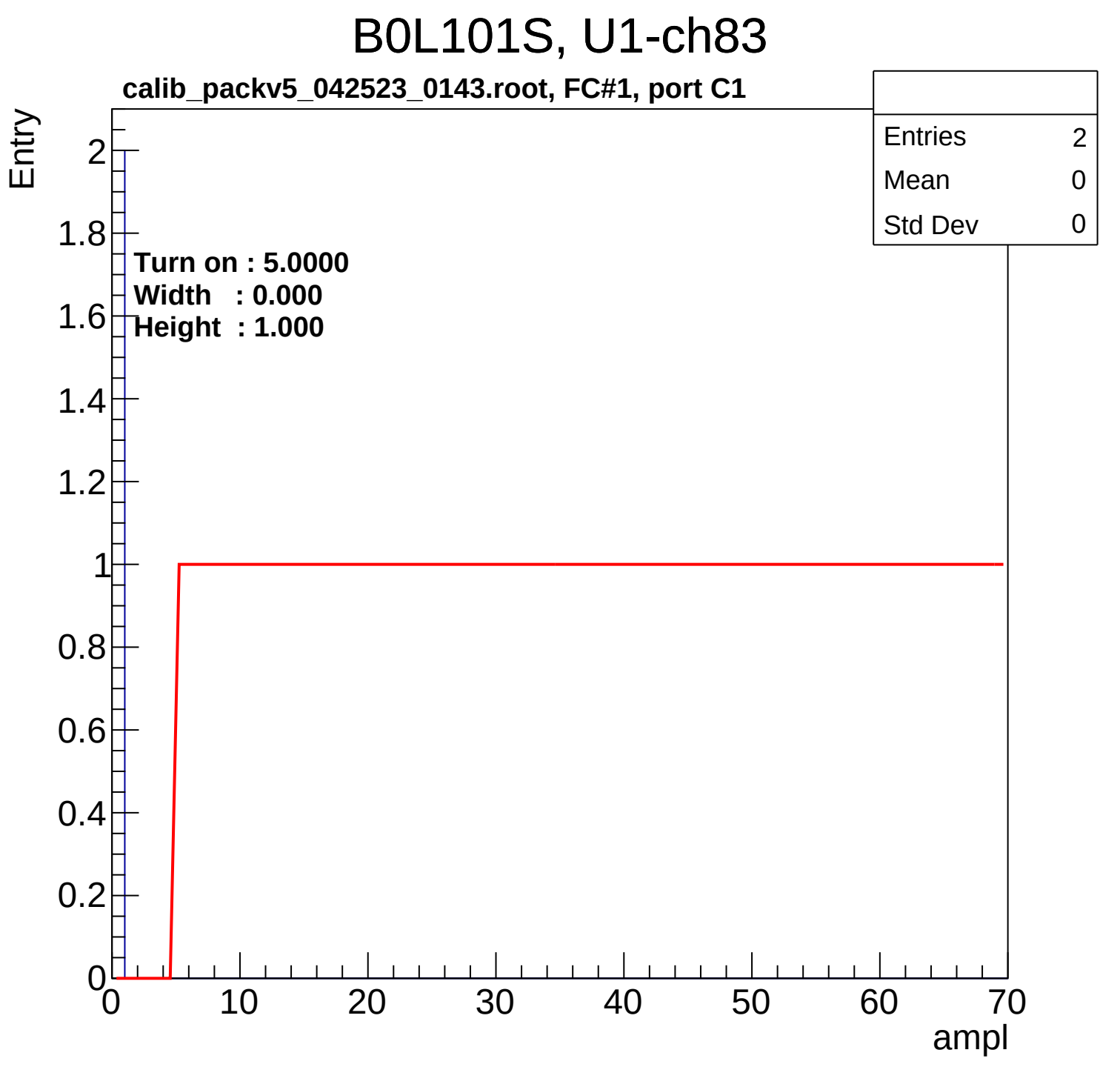

B0L101S, U1-ch78
calib_packv5_042523_0143.root, FC#1, port C1
Entries 3
Mean 11.33
Std Dev 16.03
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

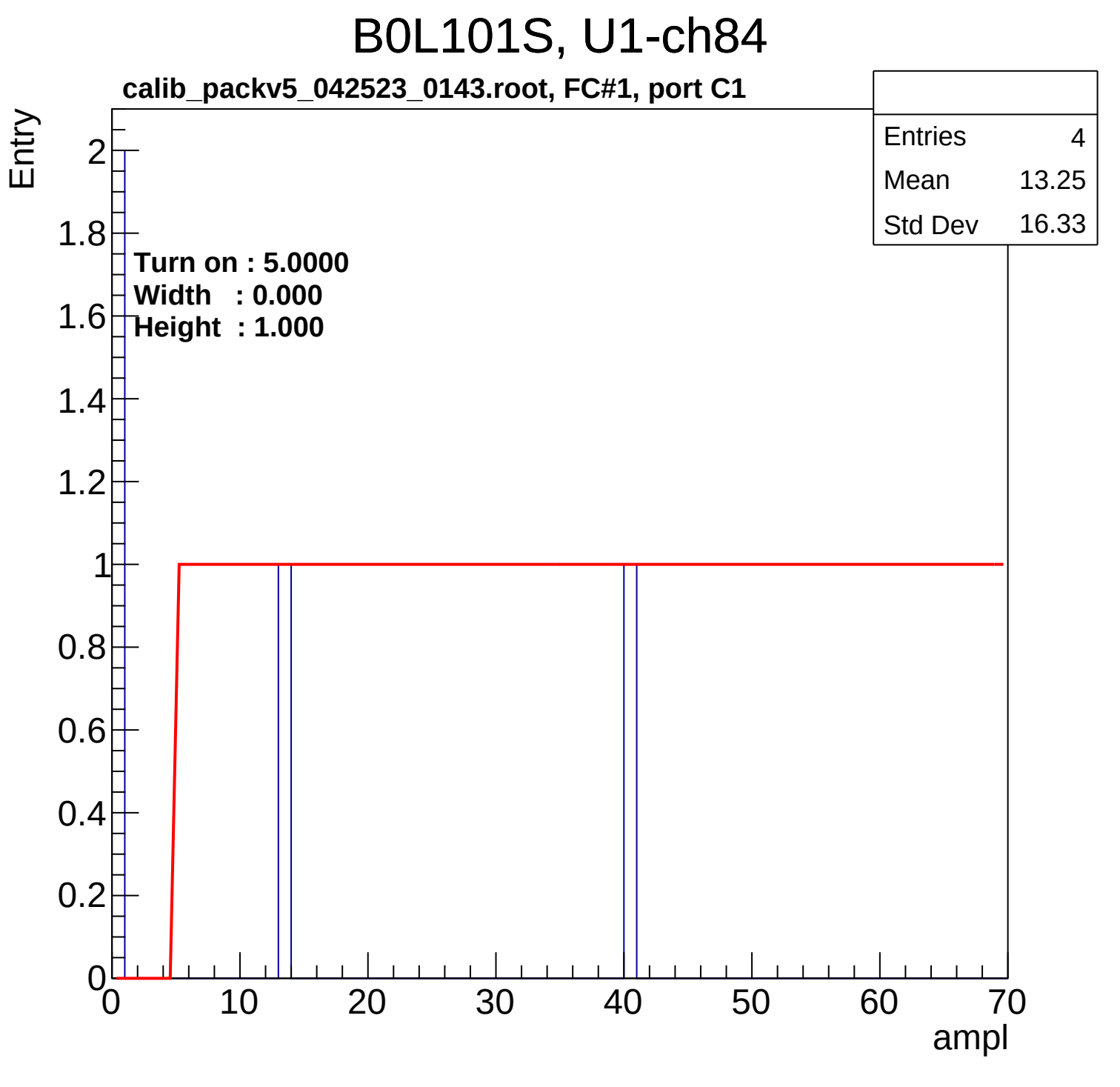

B0L101S, U1-ch79
calib_packv5_042523_0143.root, FC#1, port C1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

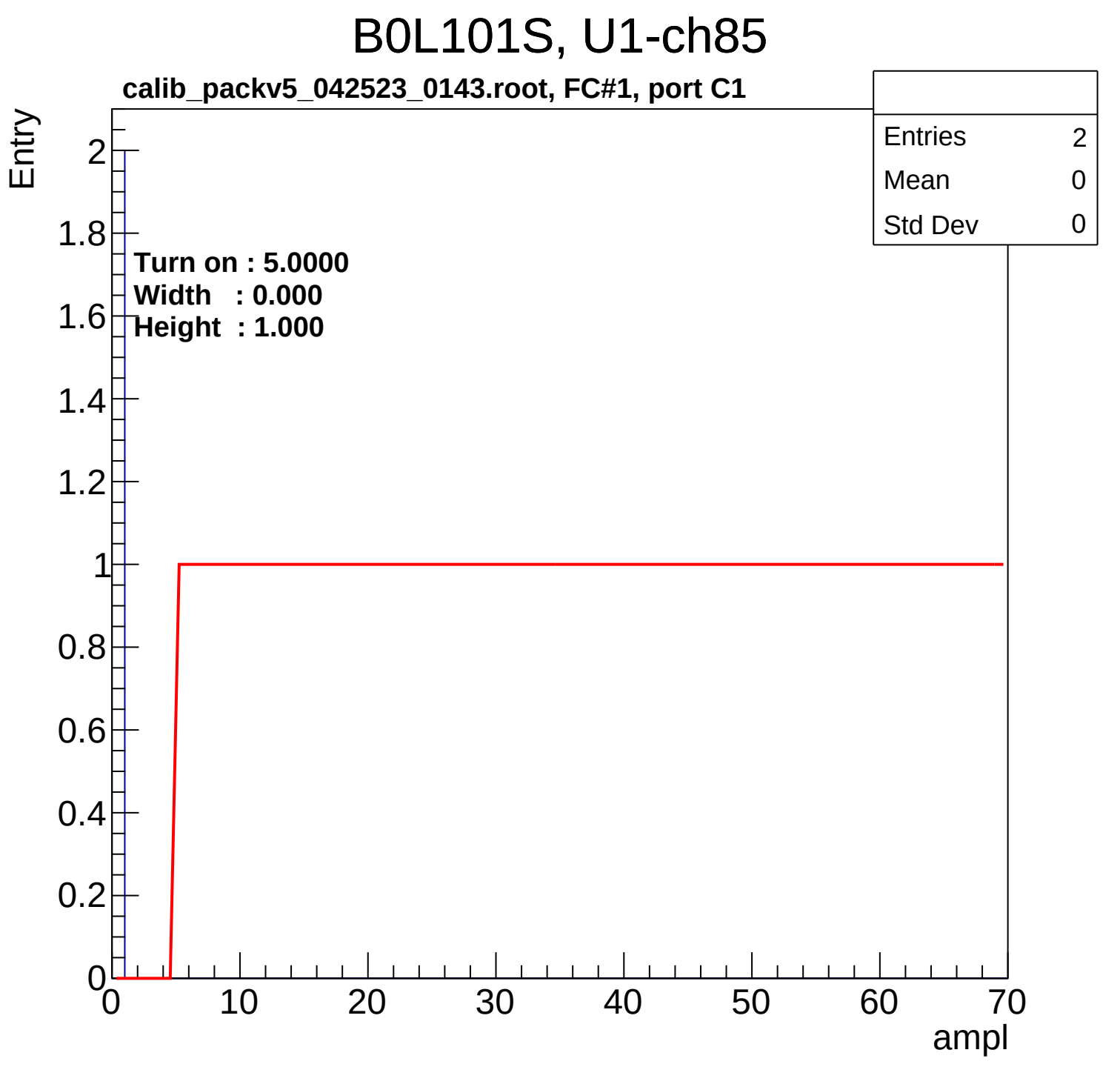

B0L101S, U1-ch80
calib_packv5_042523_0143.root, FC#1, port C1
Entries 4
Mean 16
Std Dev 16.97
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

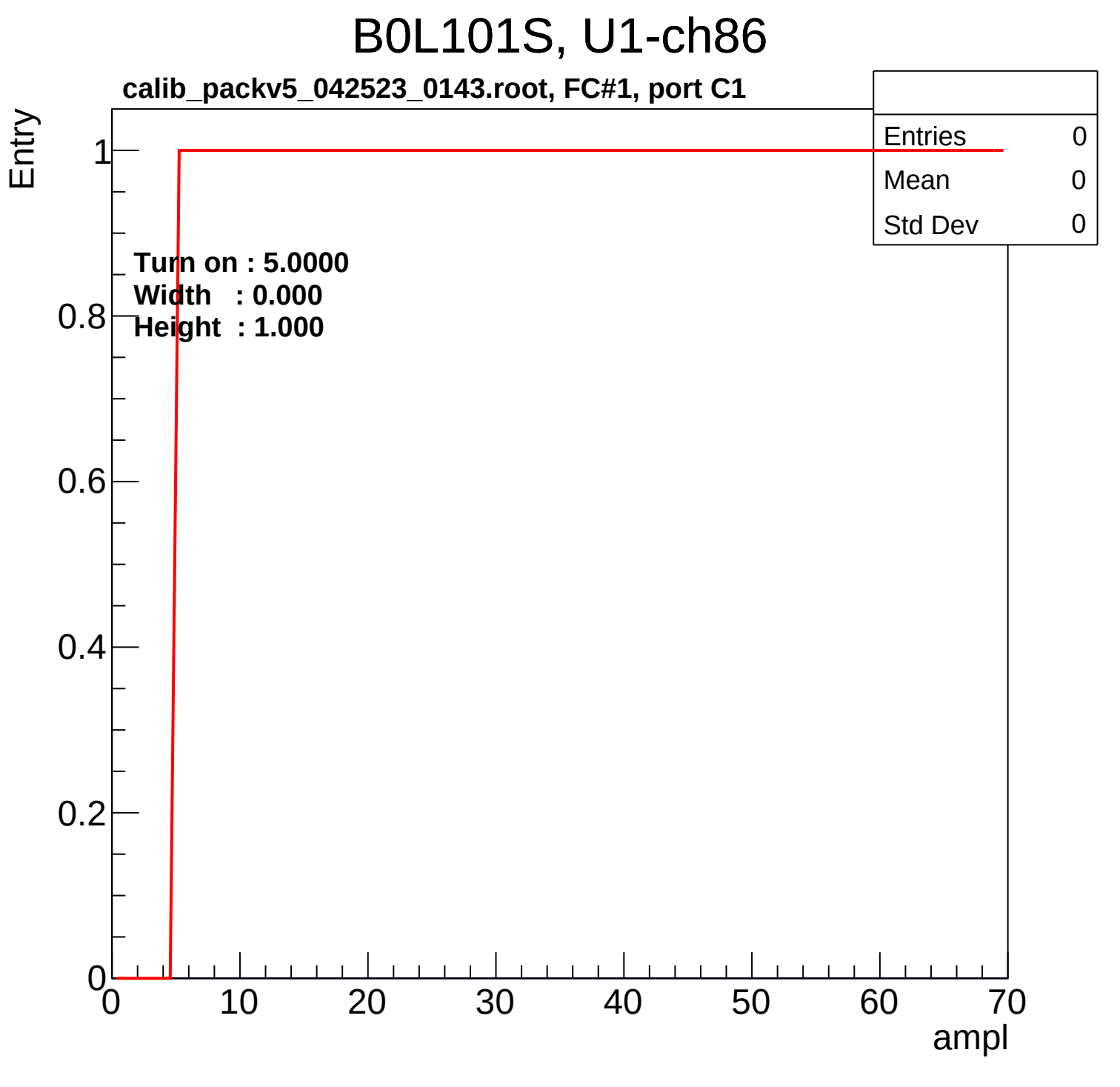

B0L101S, U1-ch81
calib_packv5_042523_0143.root, FC#1, port C1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

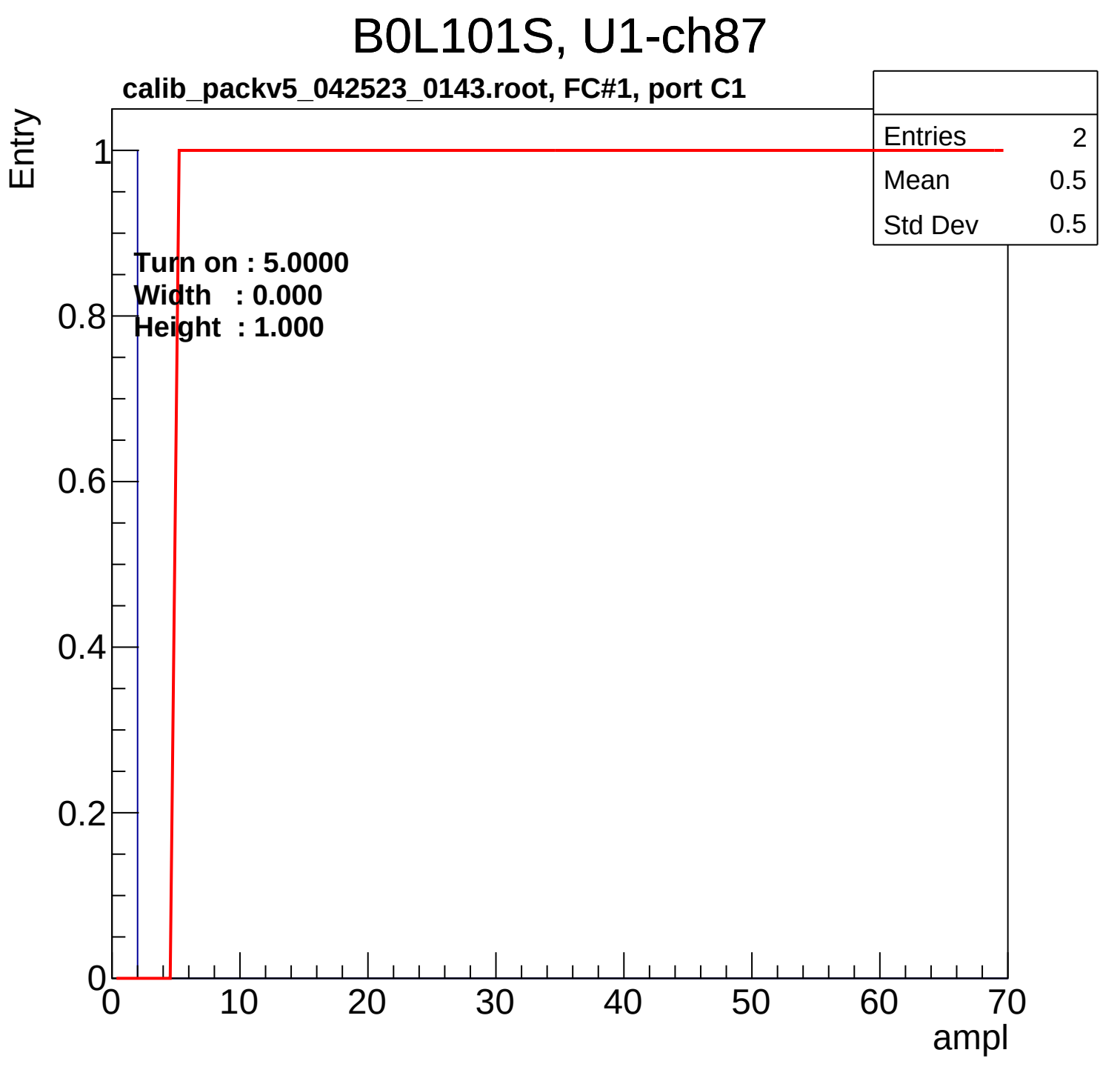

B0L101S, U1-ch82
calib_packv5_042523_0143.root, FC#1, port C1
Entries 4
Mean 4
Std Dev 6.928
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

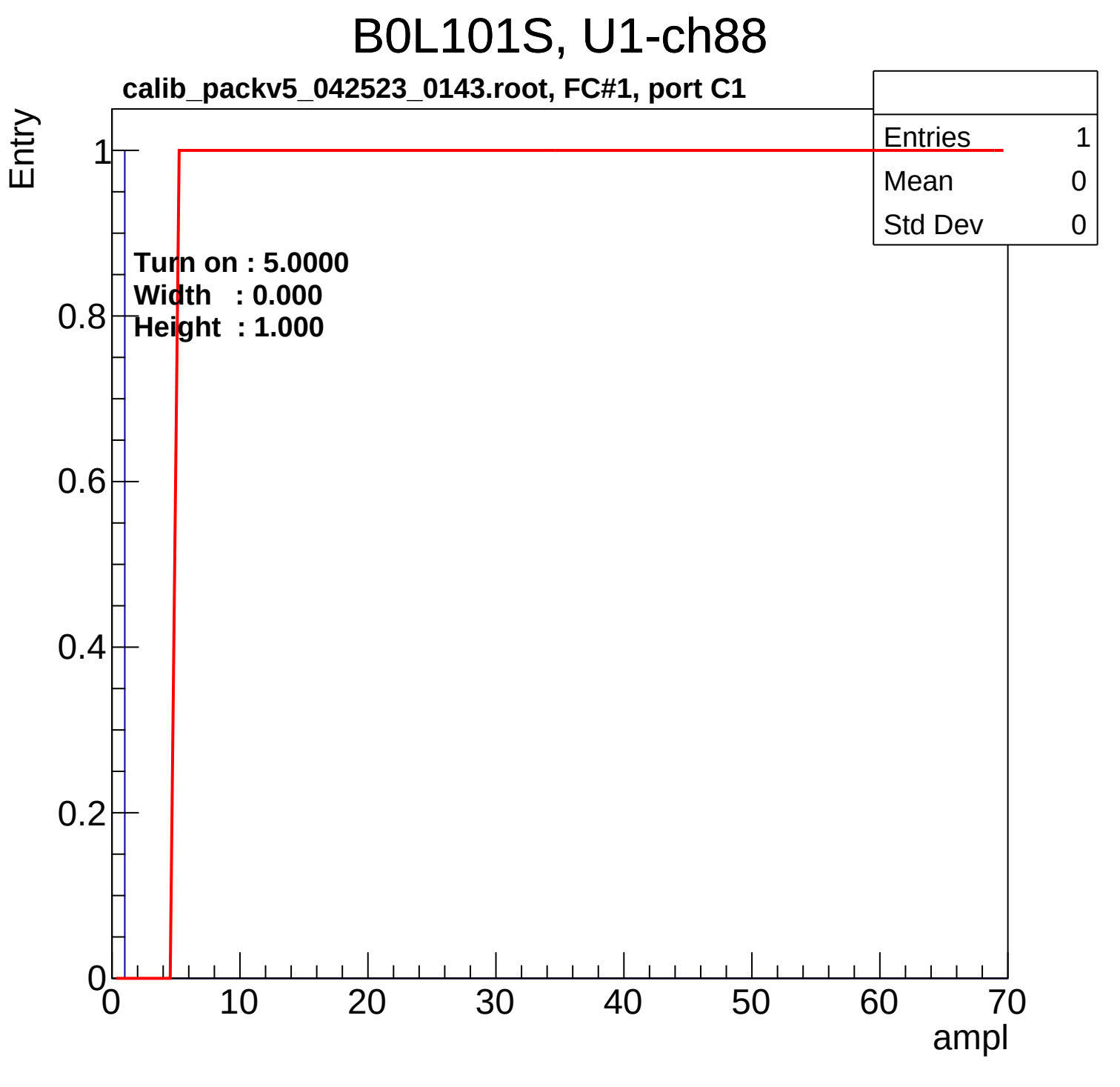

B0L101S, U1-ch83
calib_packv5_042523_0143.root, FC#1, port C1
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

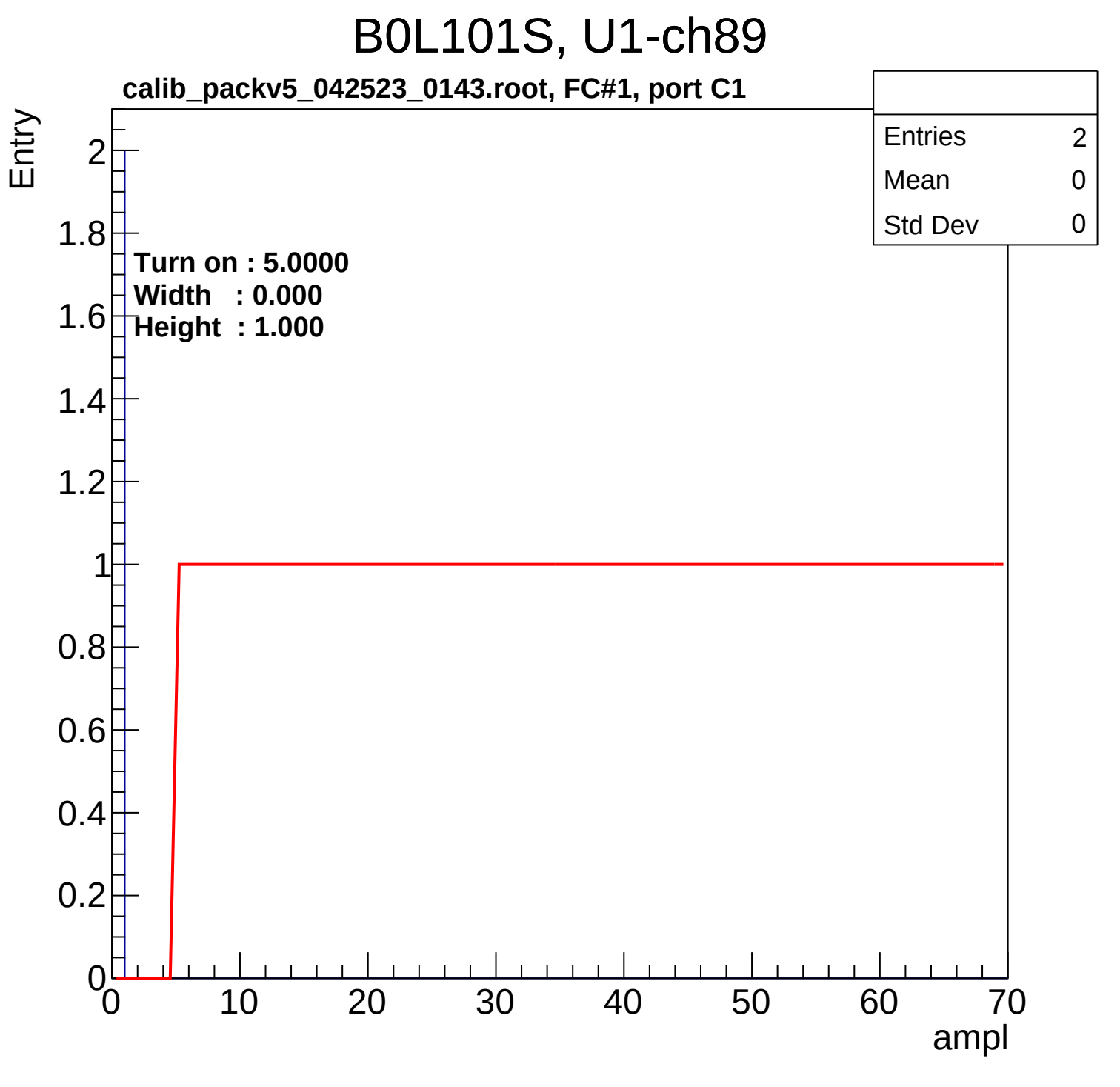

B0L101S, U1-ch84
calib_packv5_042523_0143.root, FC#1, port C1
Entries 4
Mean 13.25
Std Dev 16.33
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

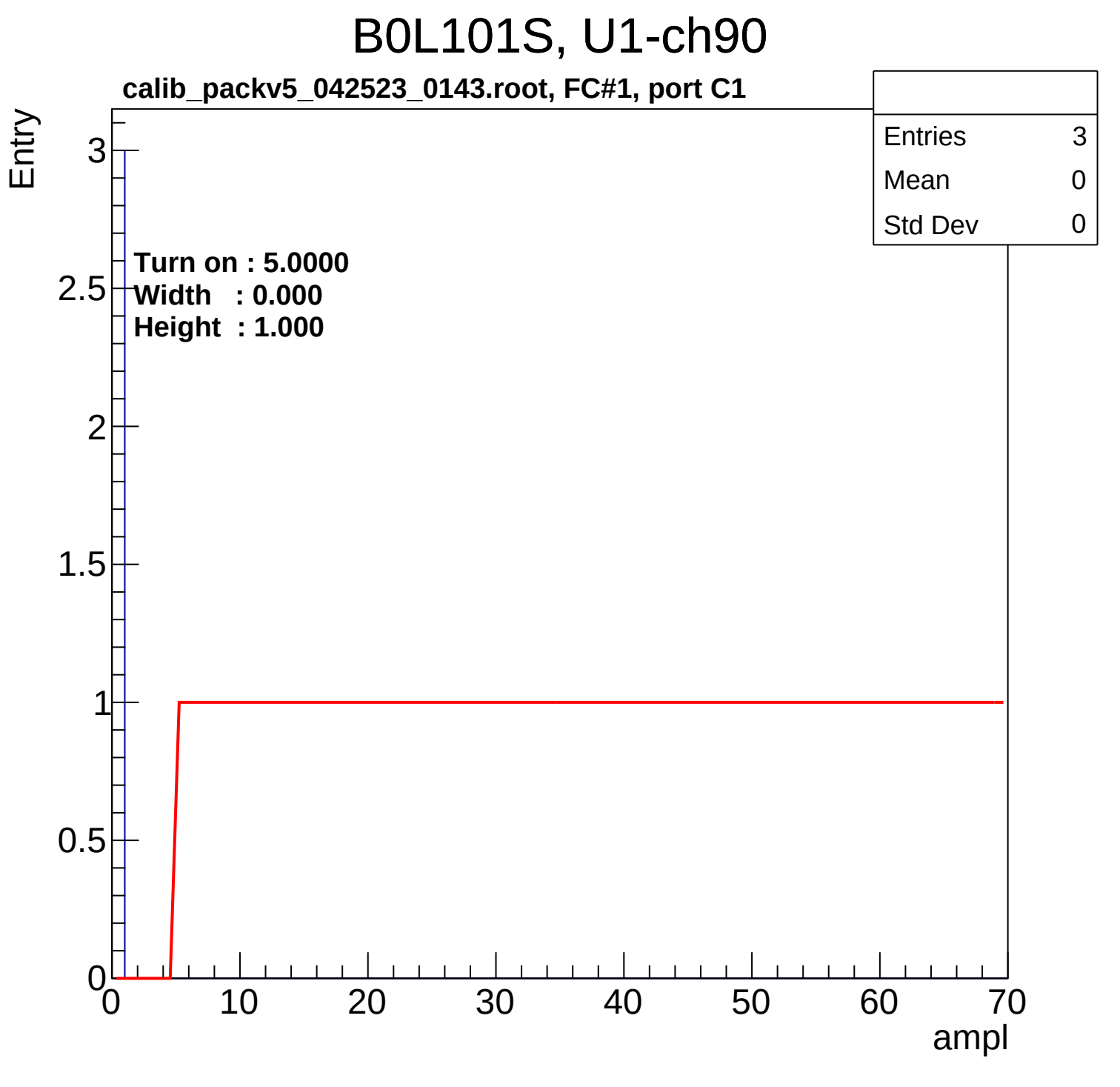

B0L101S, U1-ch85
calib_packv5_042523_0143.root, FC#1, port C1
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

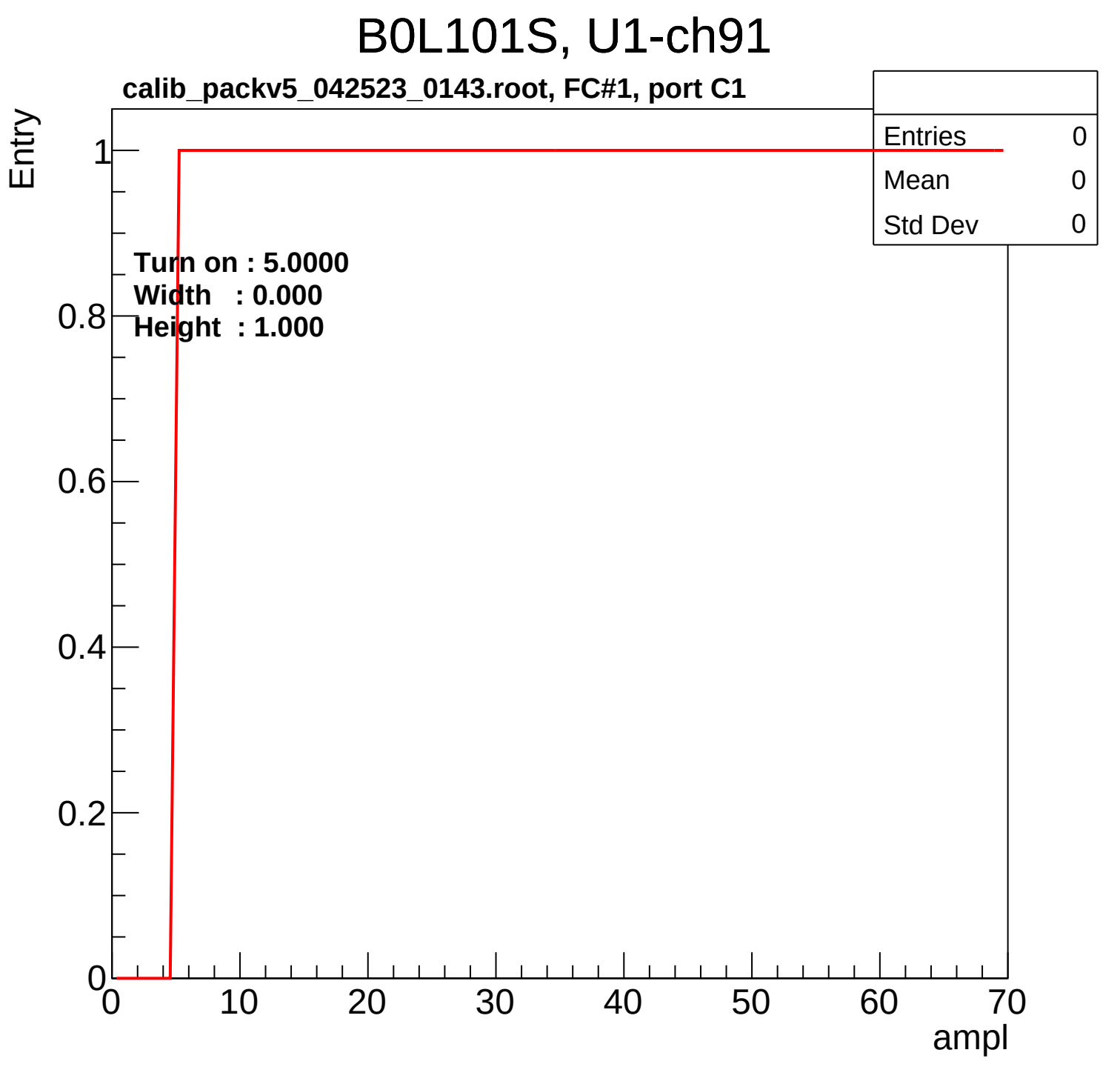

B0L101S, U1-ch86
calib_packv5_042523_0143.root, FC#1, port C1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

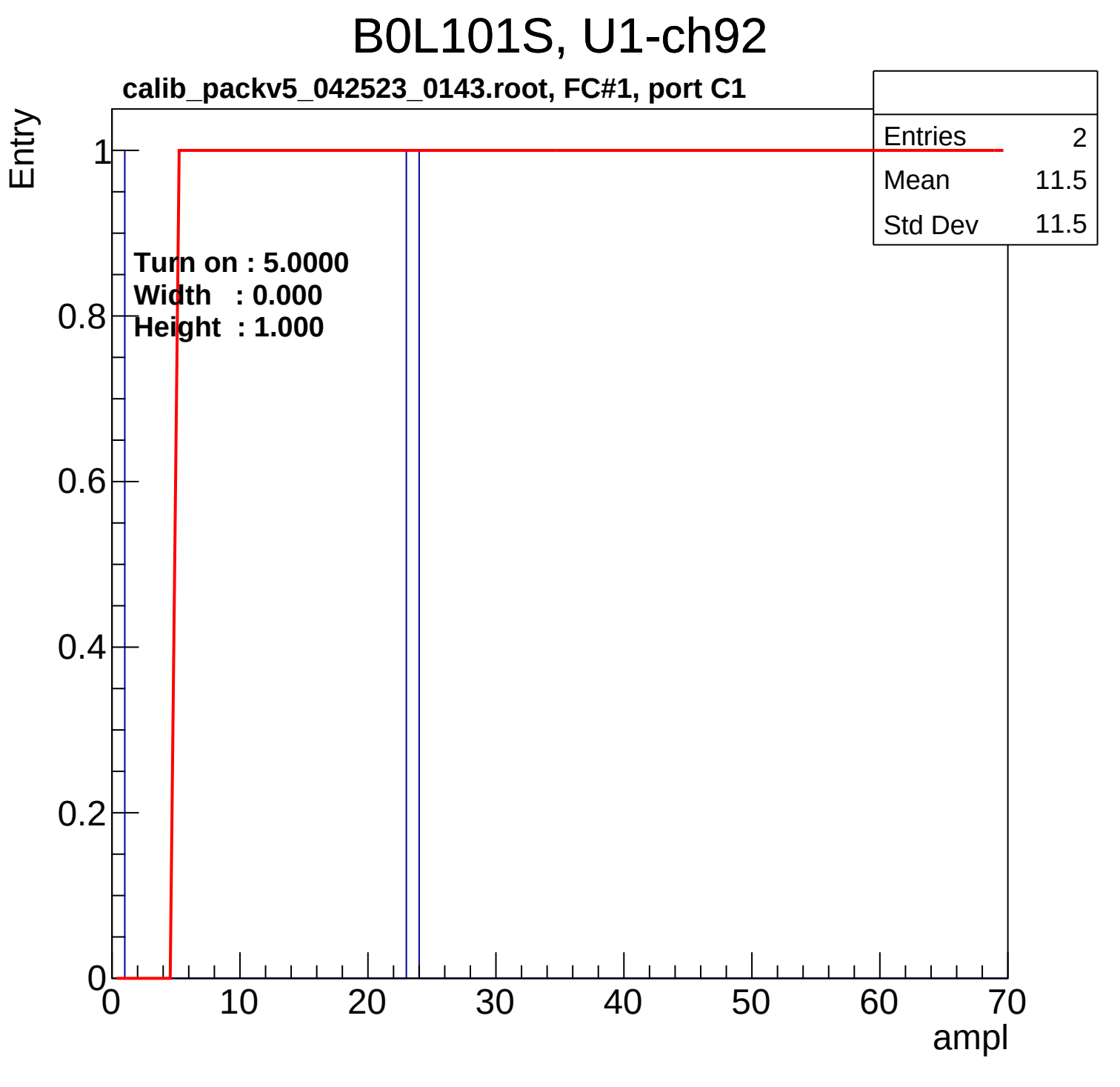

B0L101S, U1-ch87
calib_packv5_042523_0143.root, FC#1, port C1
Entries 2
Mean 0.5
Std Dev 0.5
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

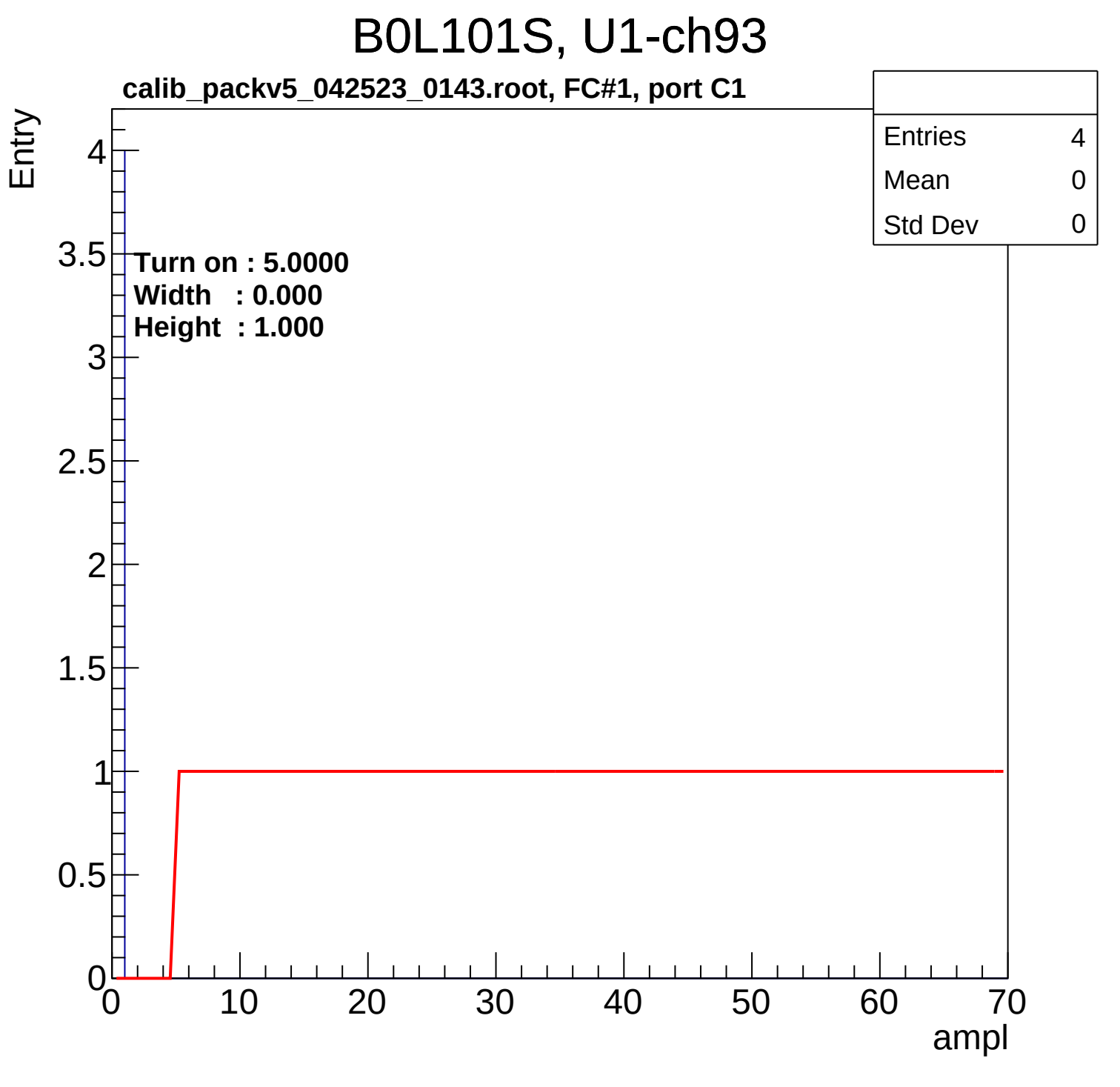

B0L101S, U1-ch88
calib_packv5_042523_0143.root, FC#1, port C1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

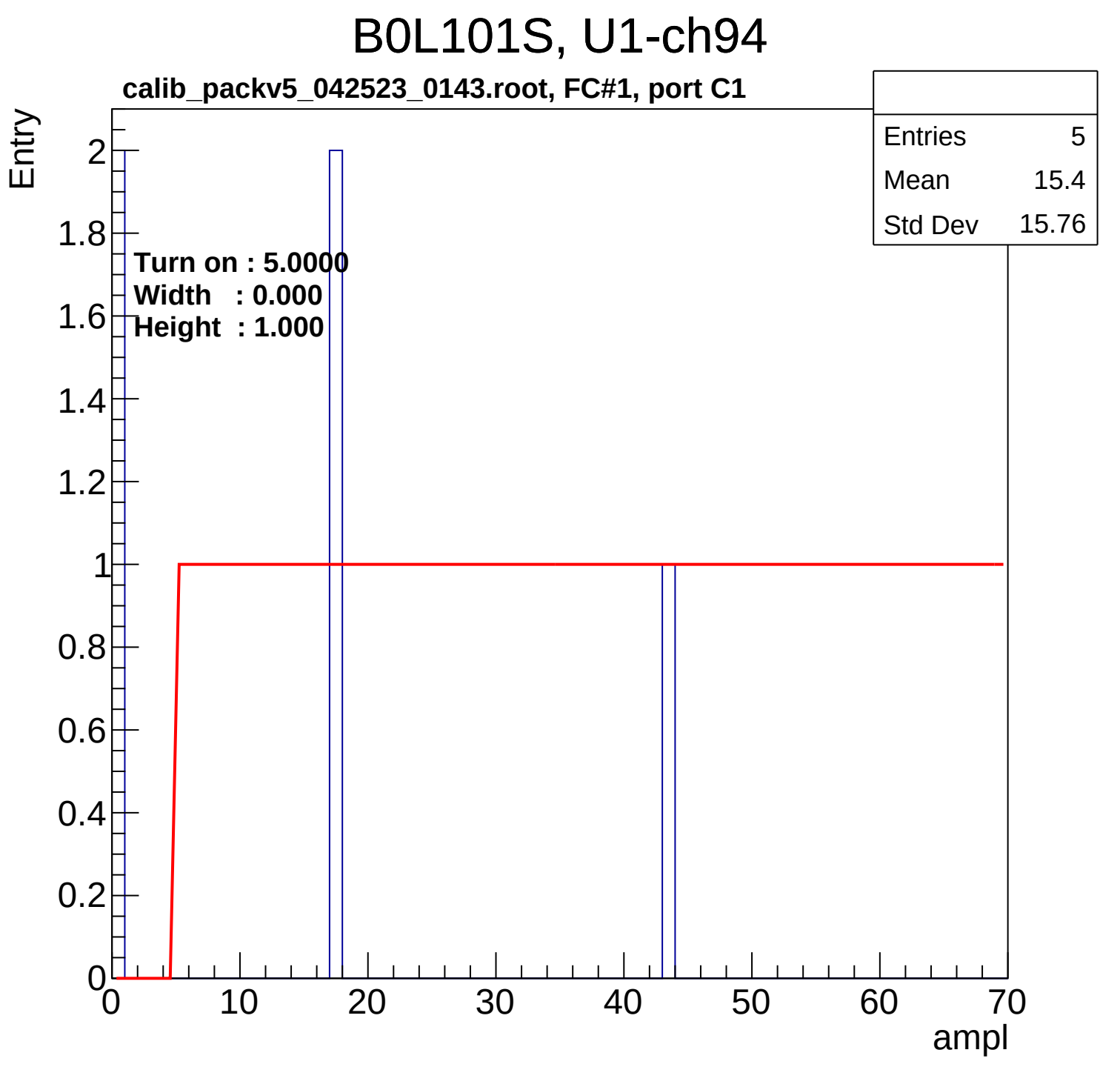

B0L101S, U1-ch89
calib_packv5_042523_0143.root, FC#1, port C1
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

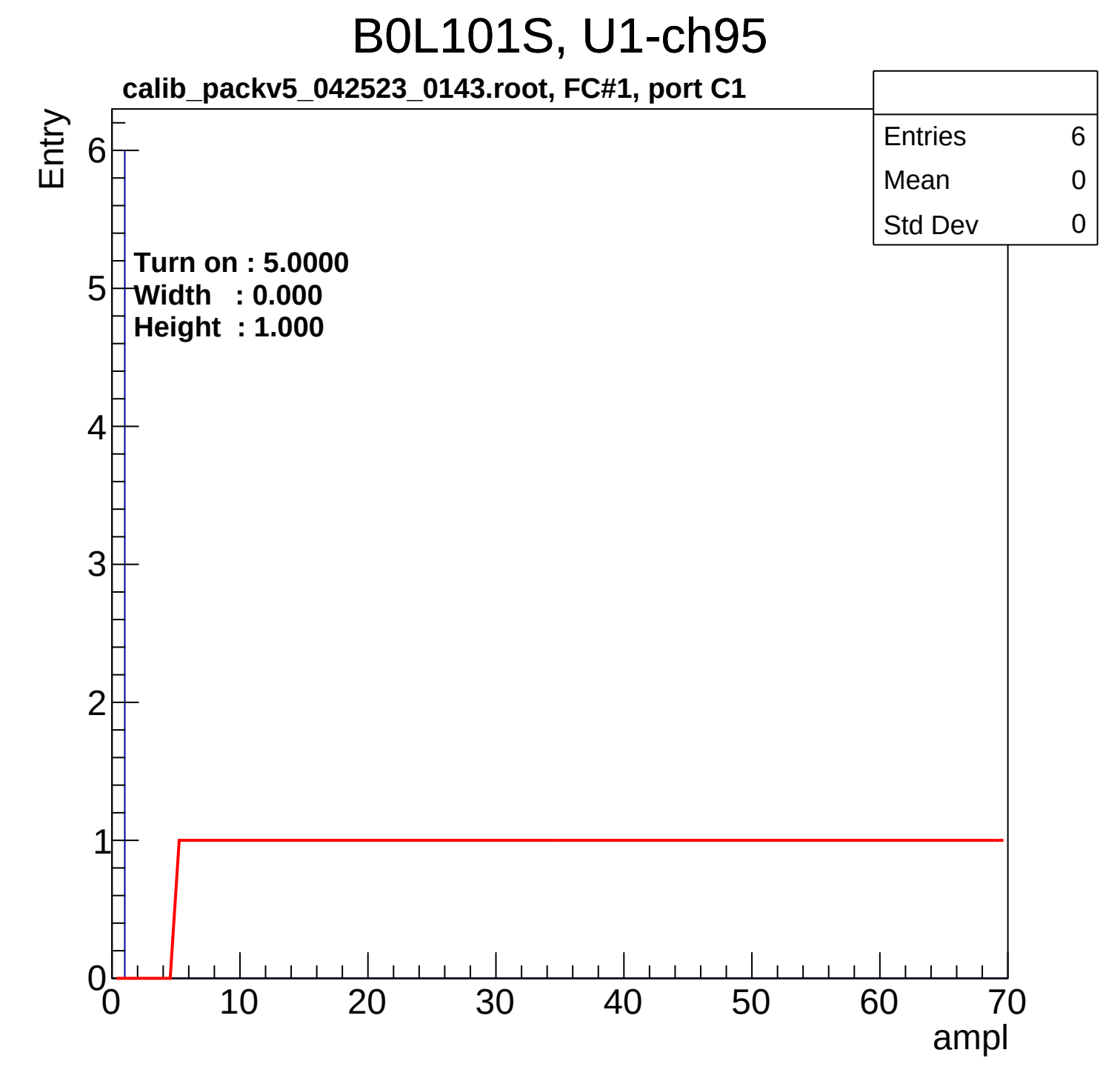

B0L101S, U1-ch90
calib_packv5_042523_0143.root, FC#1, port C1
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

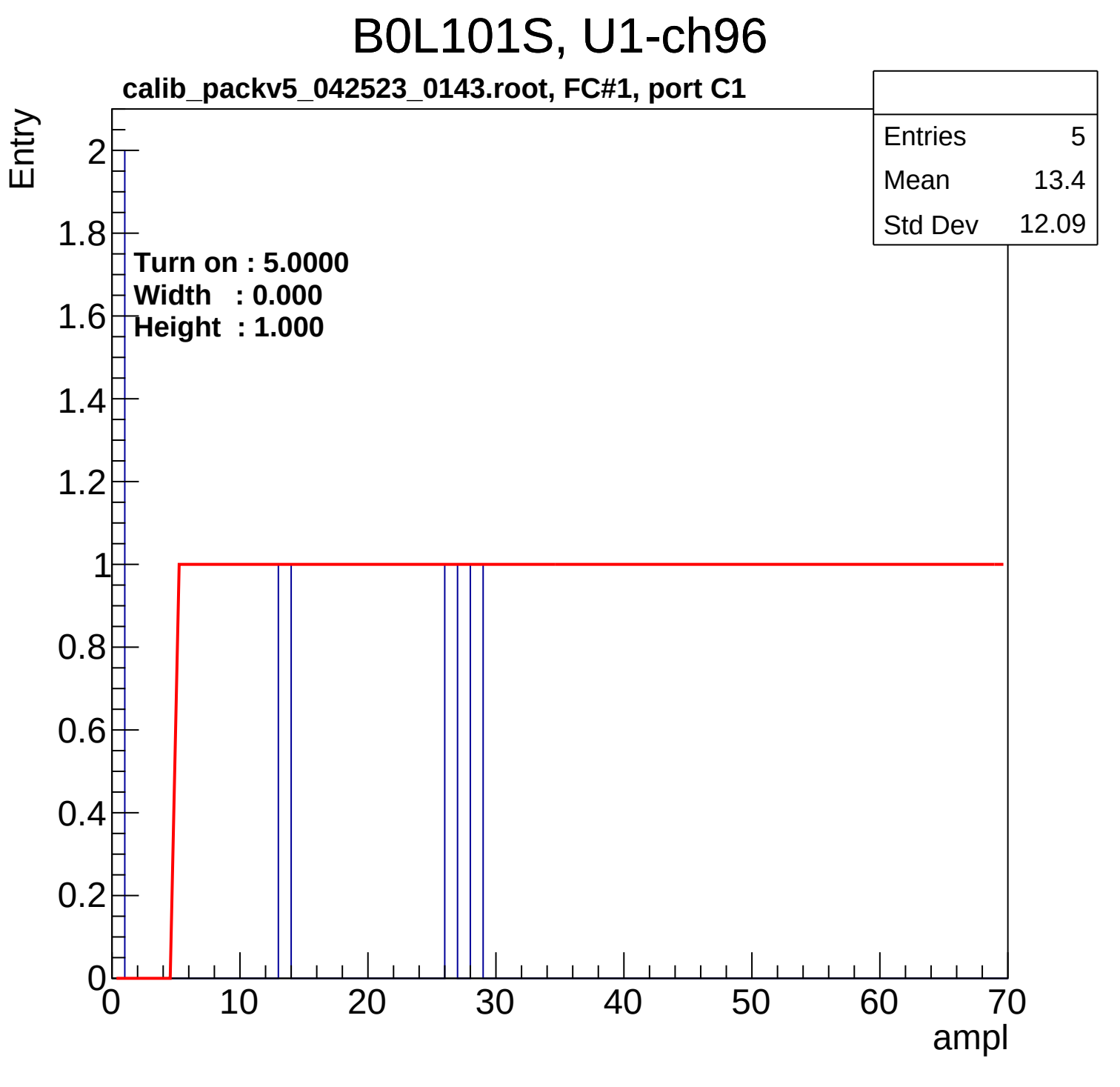

B0L101S, U1-ch91
calib_packv5_042523_0143.root, FC#1, port C1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

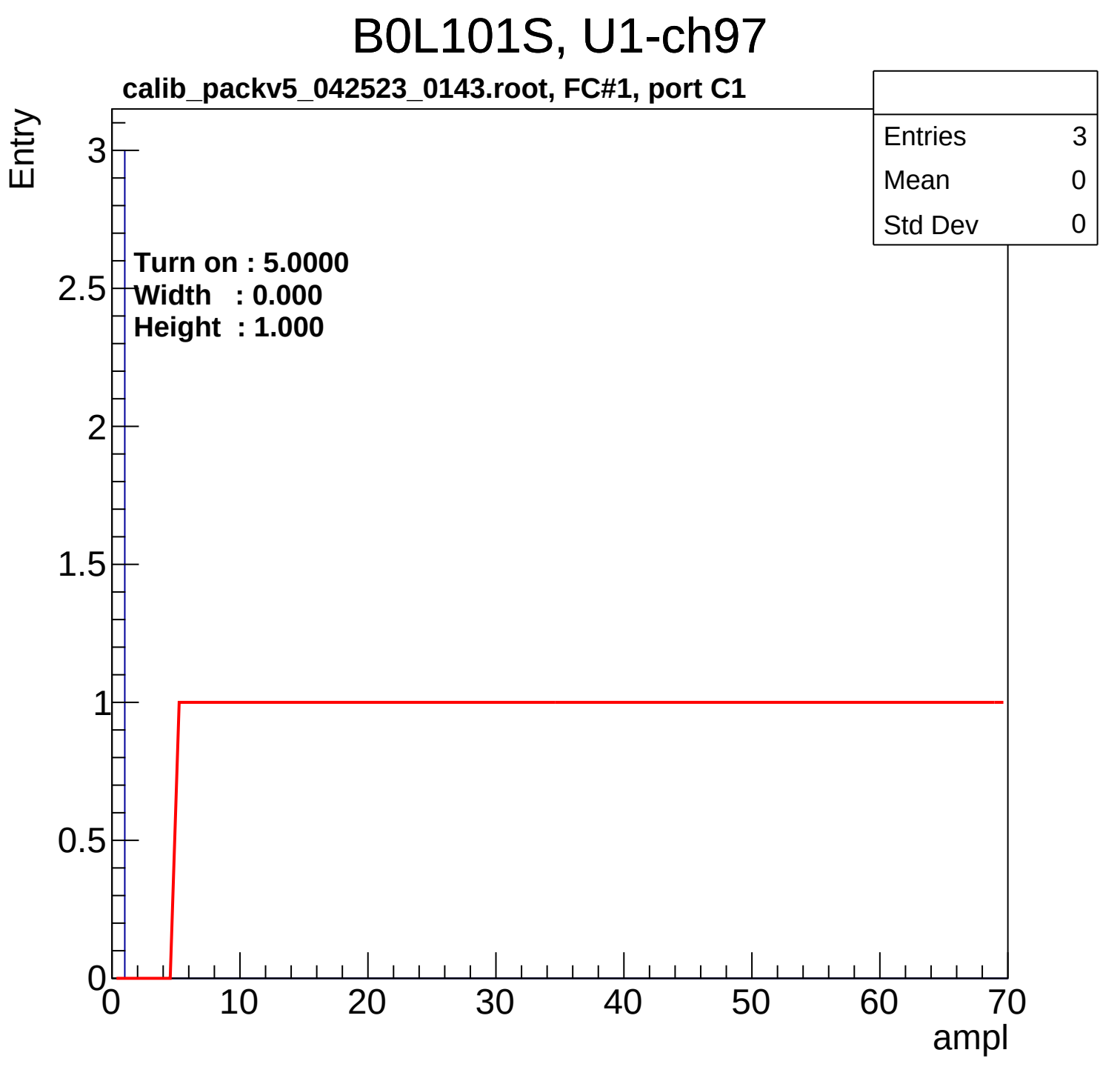

B0L101S, U1-ch92
calib_packv5_042523_0143.root, FC#1, port C1
Entries 2
Mean 11.5
Std Dev 11.5
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

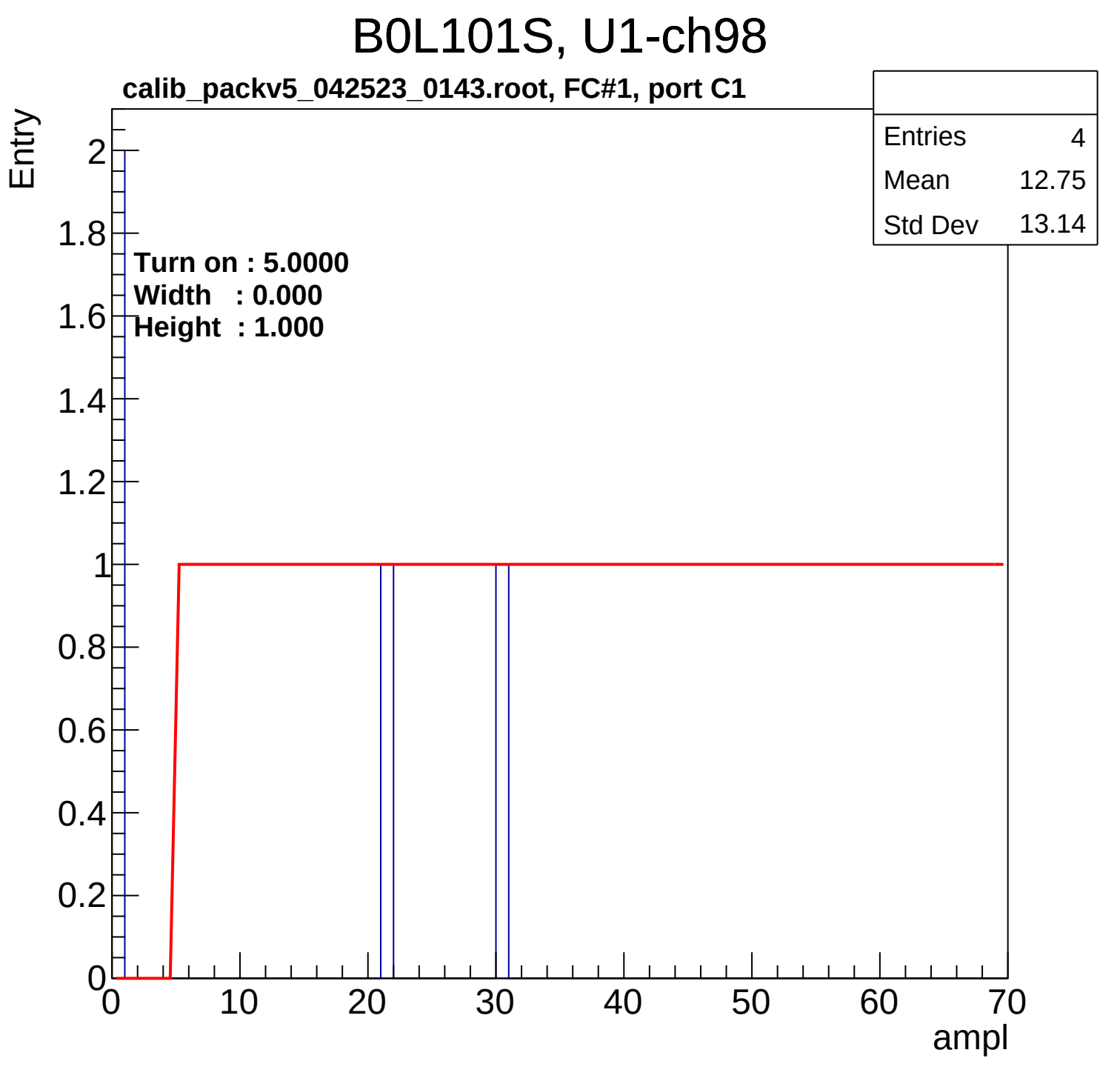

B0L101S, U1-ch93
calib_packv5_042523_0143.root, FC#1, port C1
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

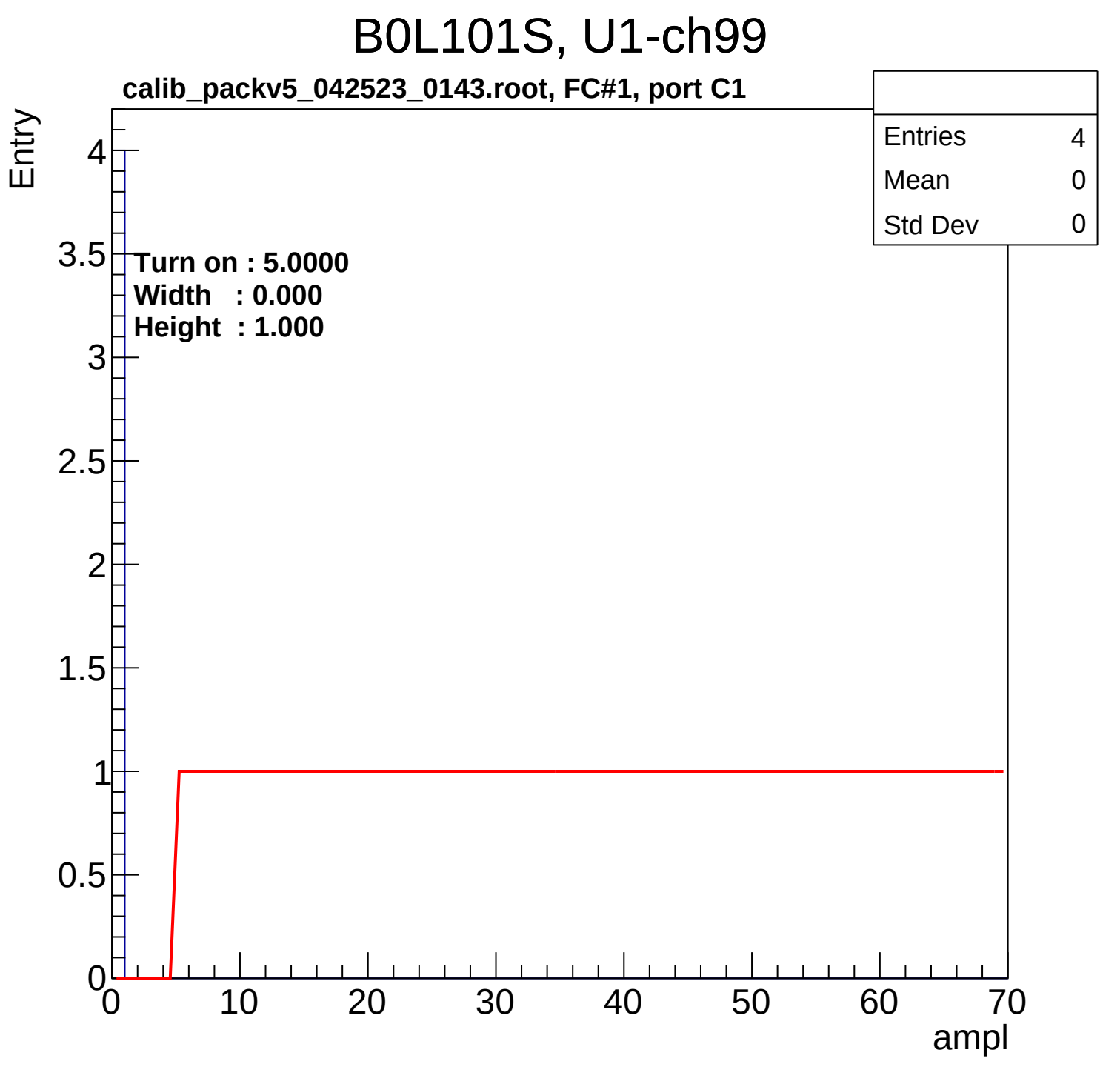

B0L101S, U1-ch94
calib_packv5_042523_0143.root, FC#1, port C1
Entries 5
Mean 15.4
Std Dev 15.76
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

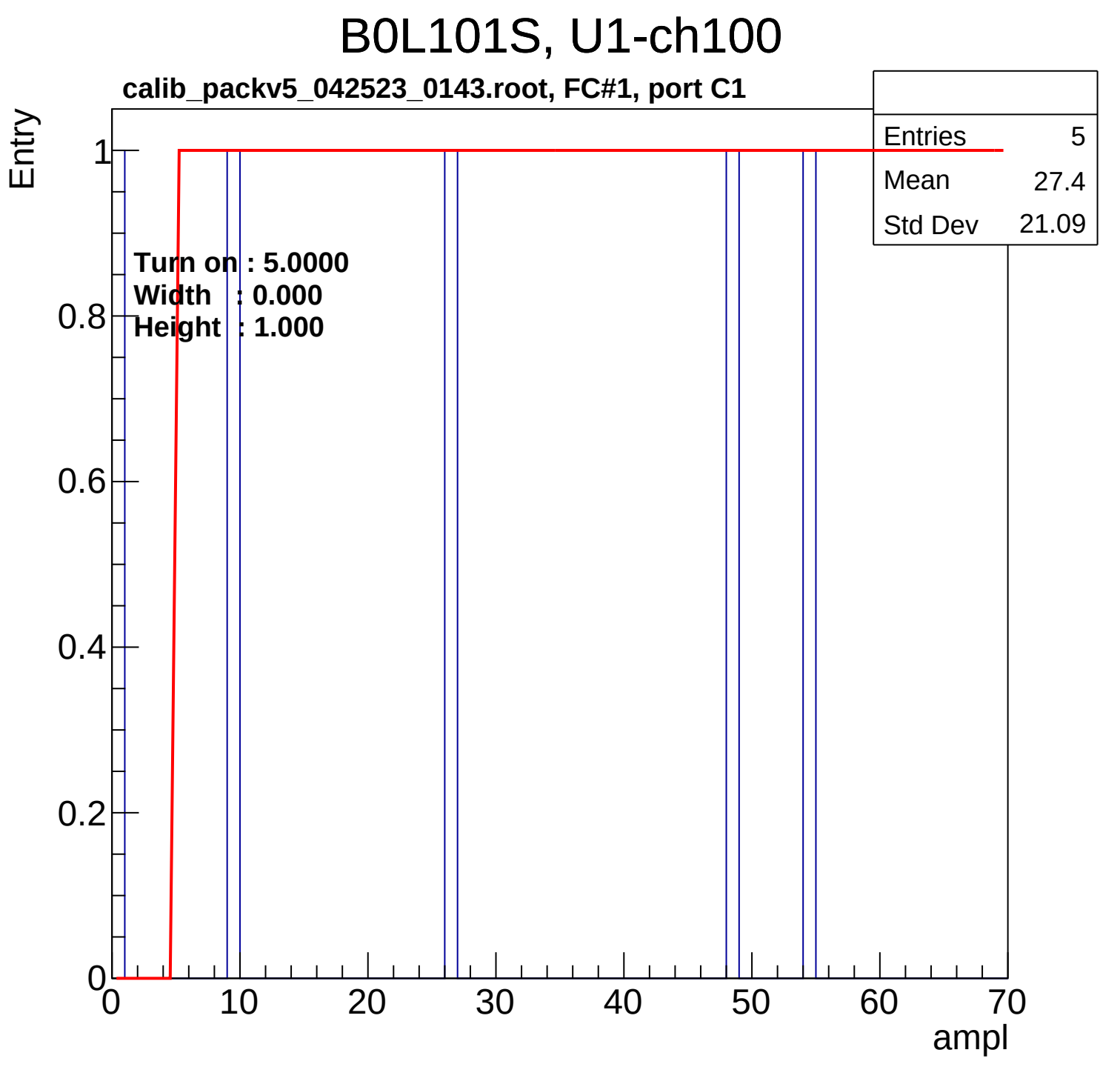

B0L101S, U1-ch95
calib_packv5_042523_0143.root, FC#1, port C1
Entries 6
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

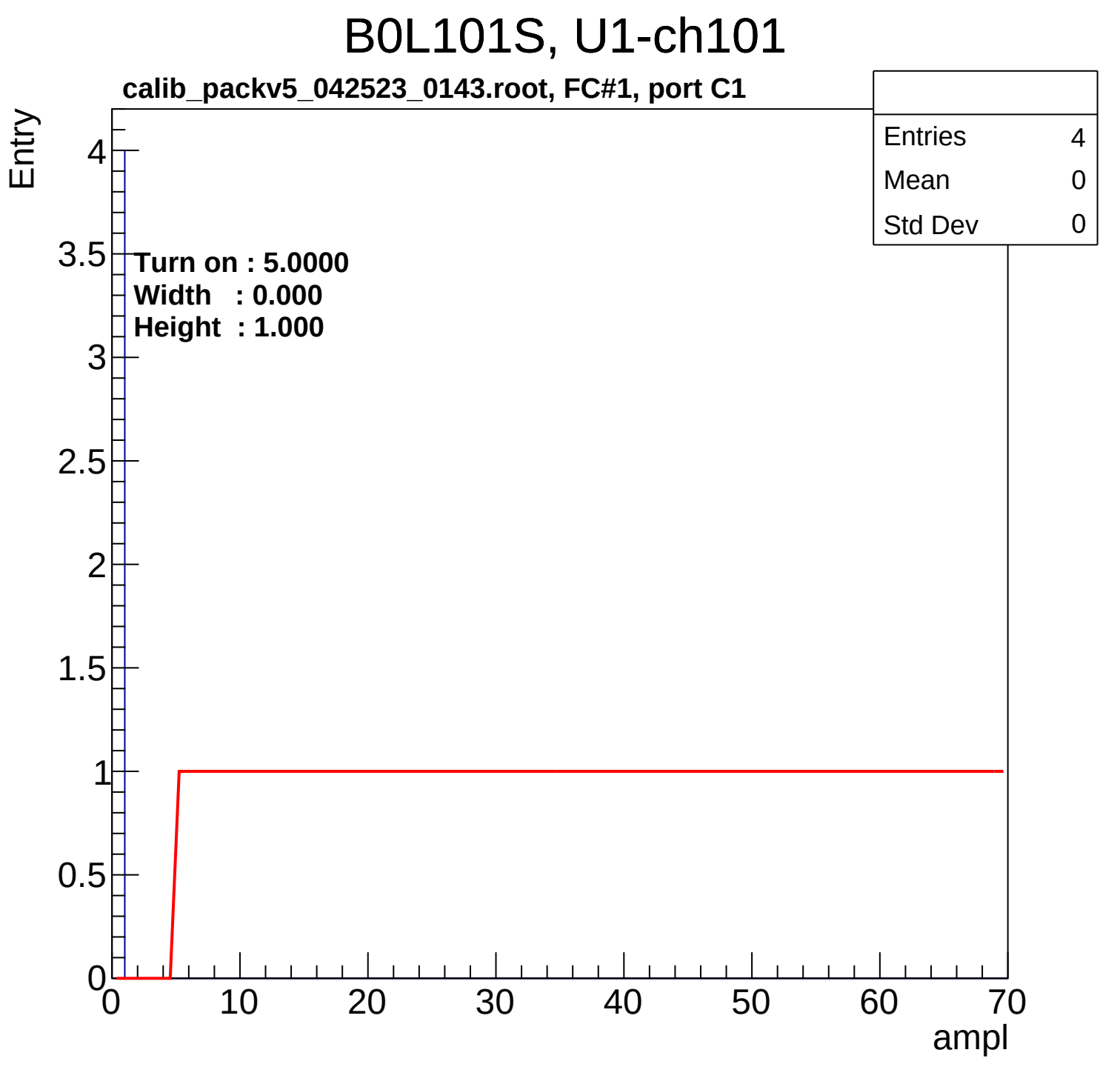

B0L101S, U1-ch96
calib_packv5_042523_0143.root, FC#1, port C1
Entries 5
Mean 13.4
Std Dev 12.09
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

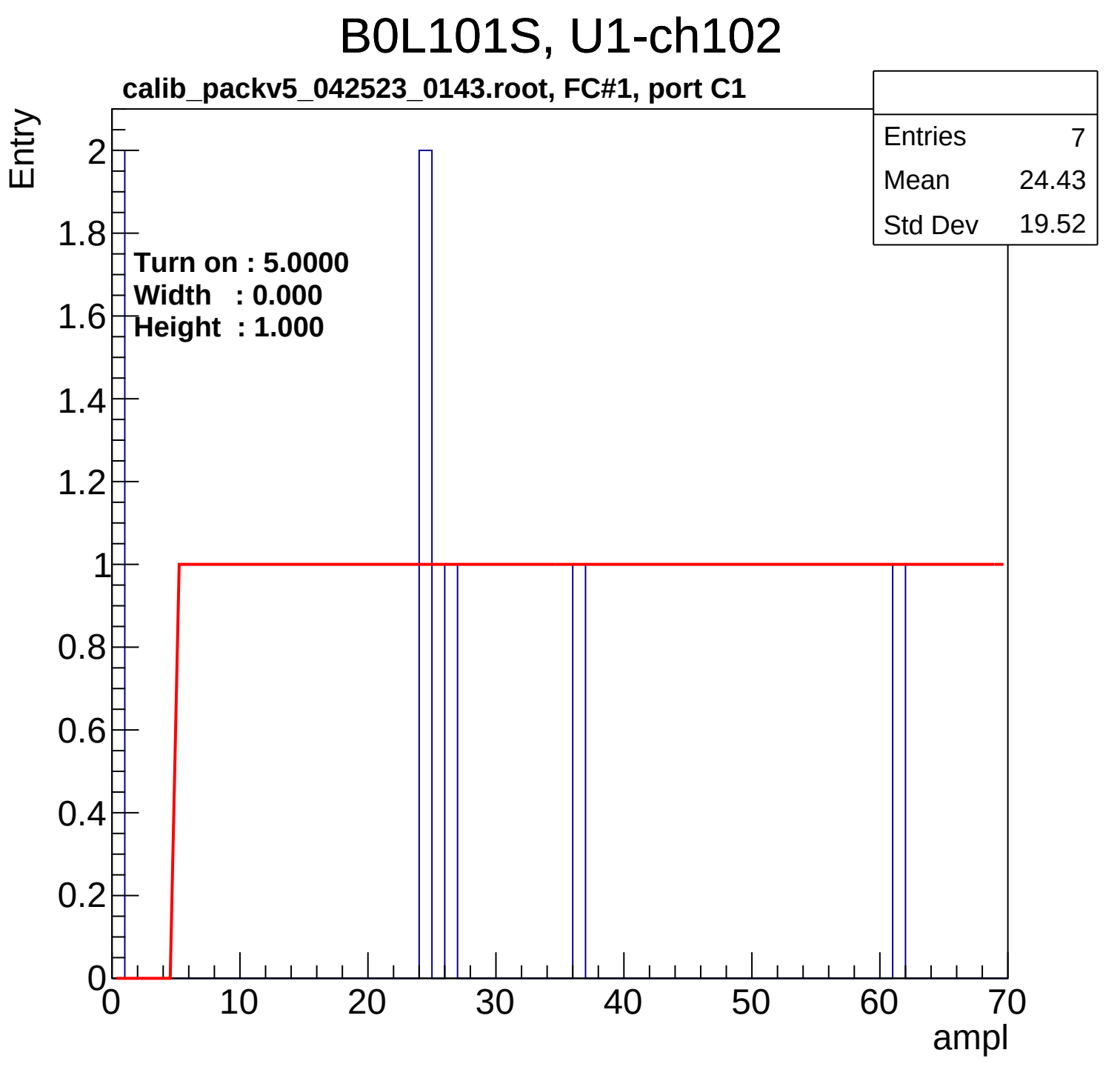

B0L101S, U1-ch97
calib_packv5_042523_0143.root, FC#1, port C1
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

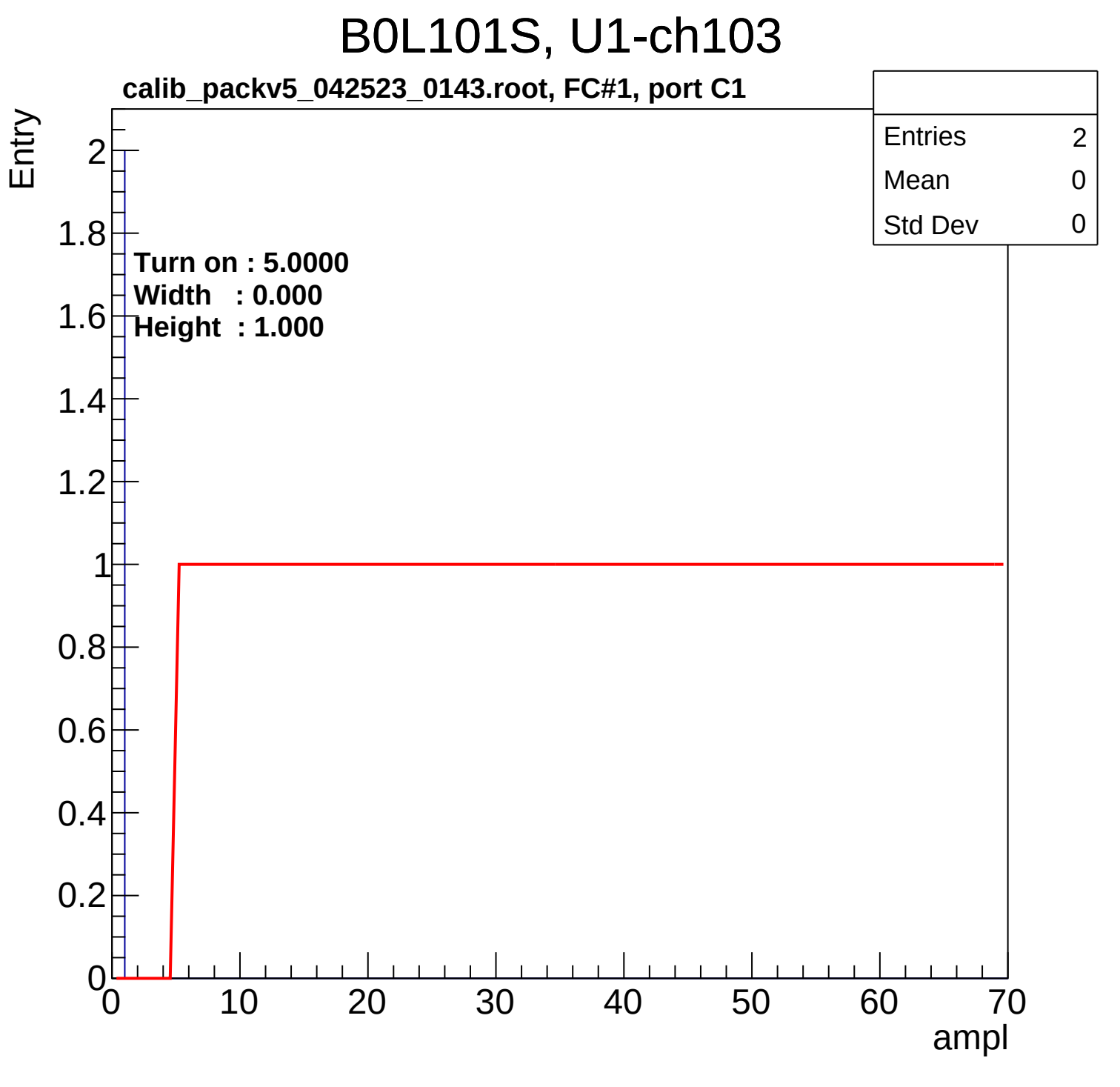

B0L101S, U1-ch98
calib_packv5_042523_0143.root, FC#1, port C1
Entries 4
Mean 12.75
Std Dev 13.14
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

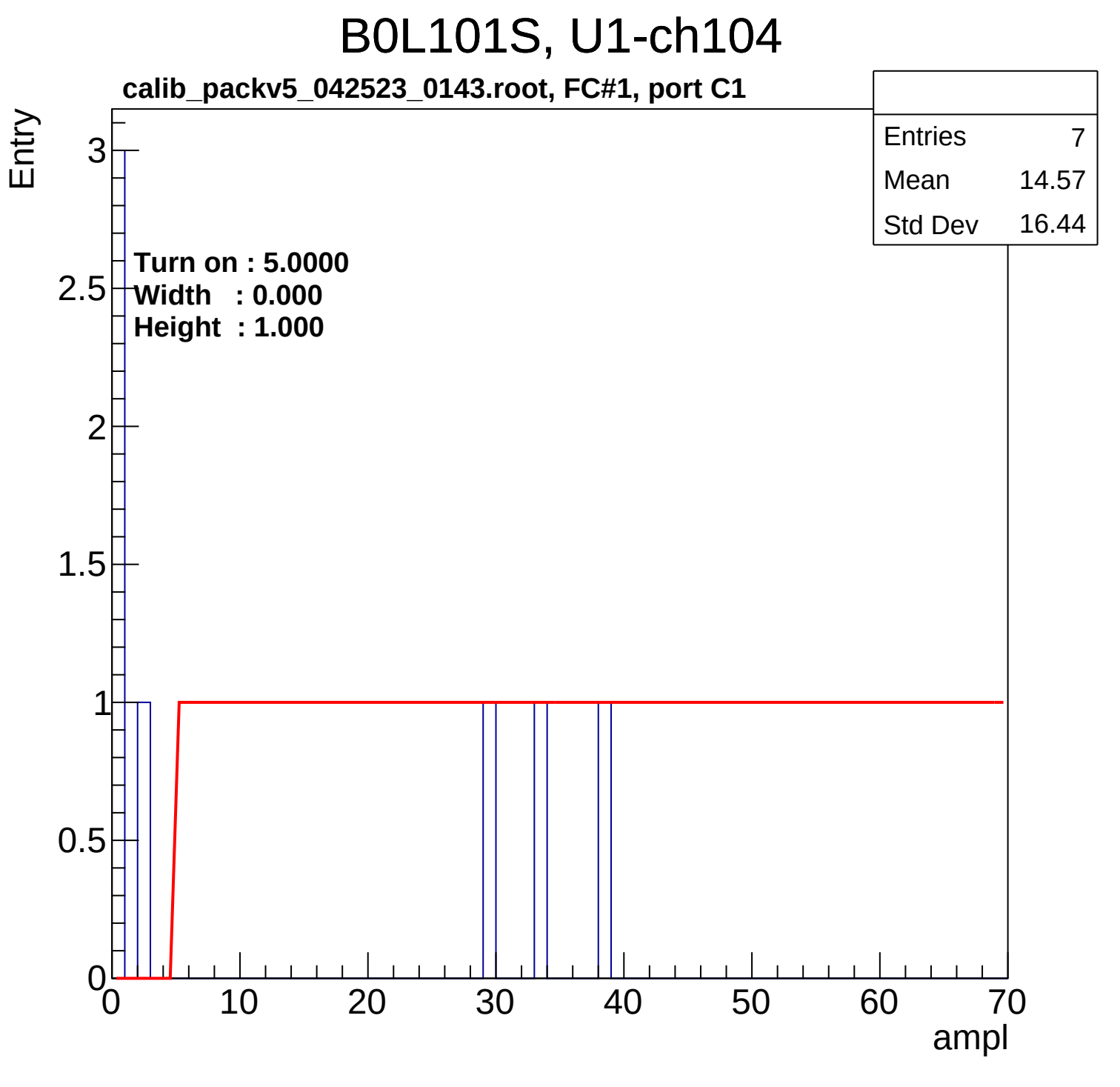

B0L101S, U1-ch99
calib_packv5_042523_0143.root, FC#1, port C1
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

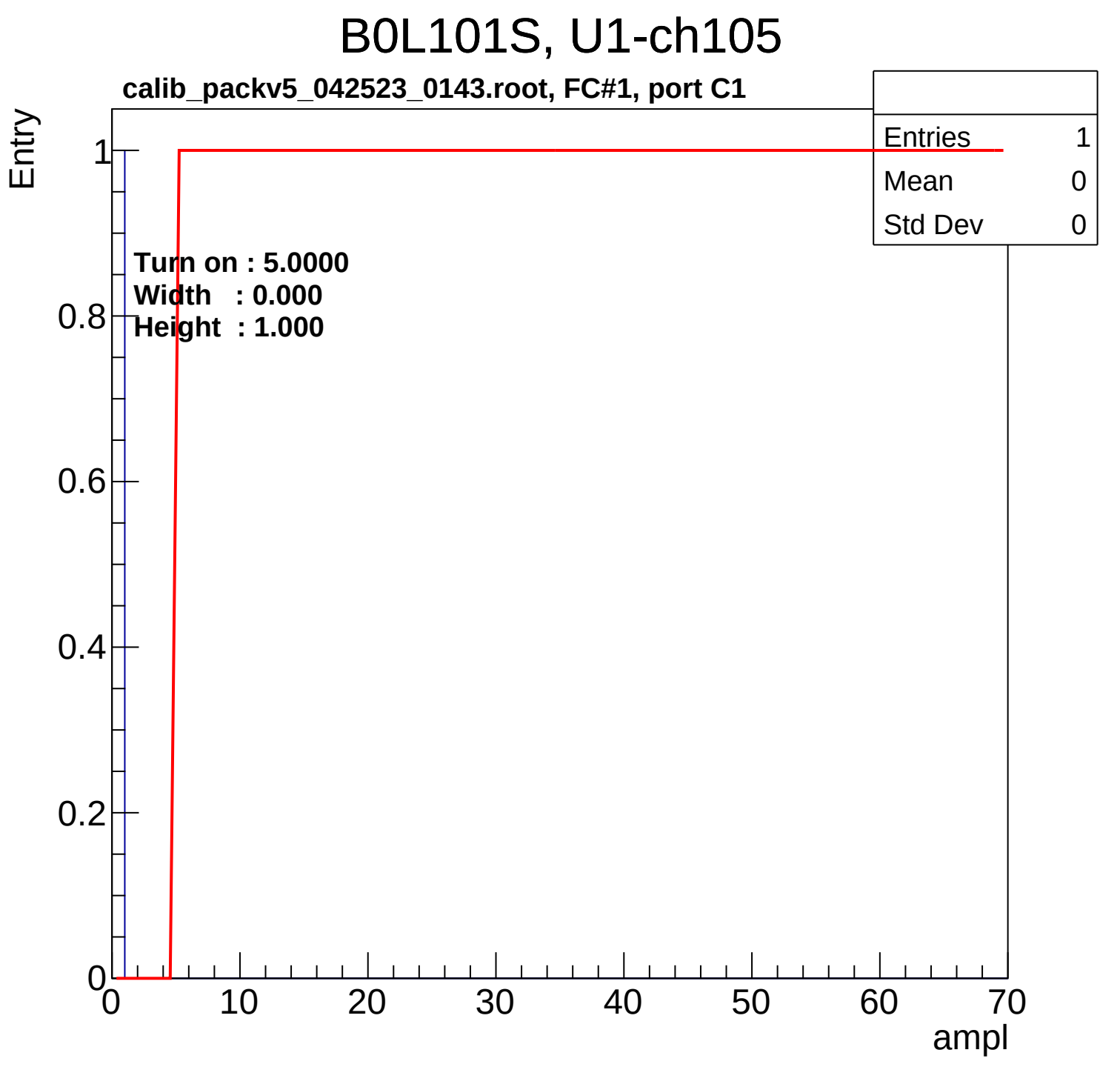

B0L101S, U1-ch100
calib_packv5_042523_0143.root, FC#1, port C1
Entries 5
Mean 27.4
Std Dev 21.09
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

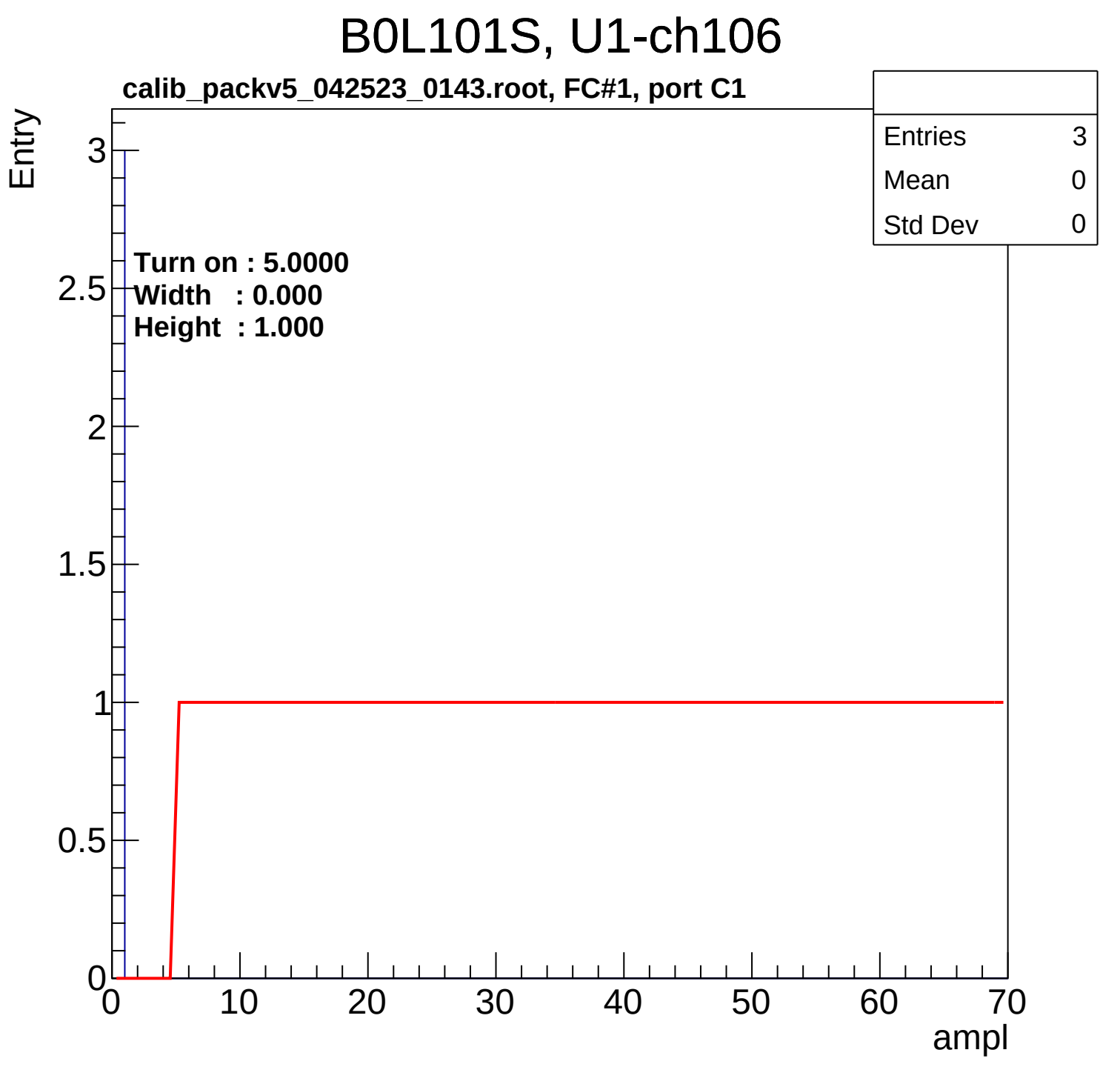

B0L101S, U1-ch101
calib_packv5_042523_0143.root, FC#1, port C1
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

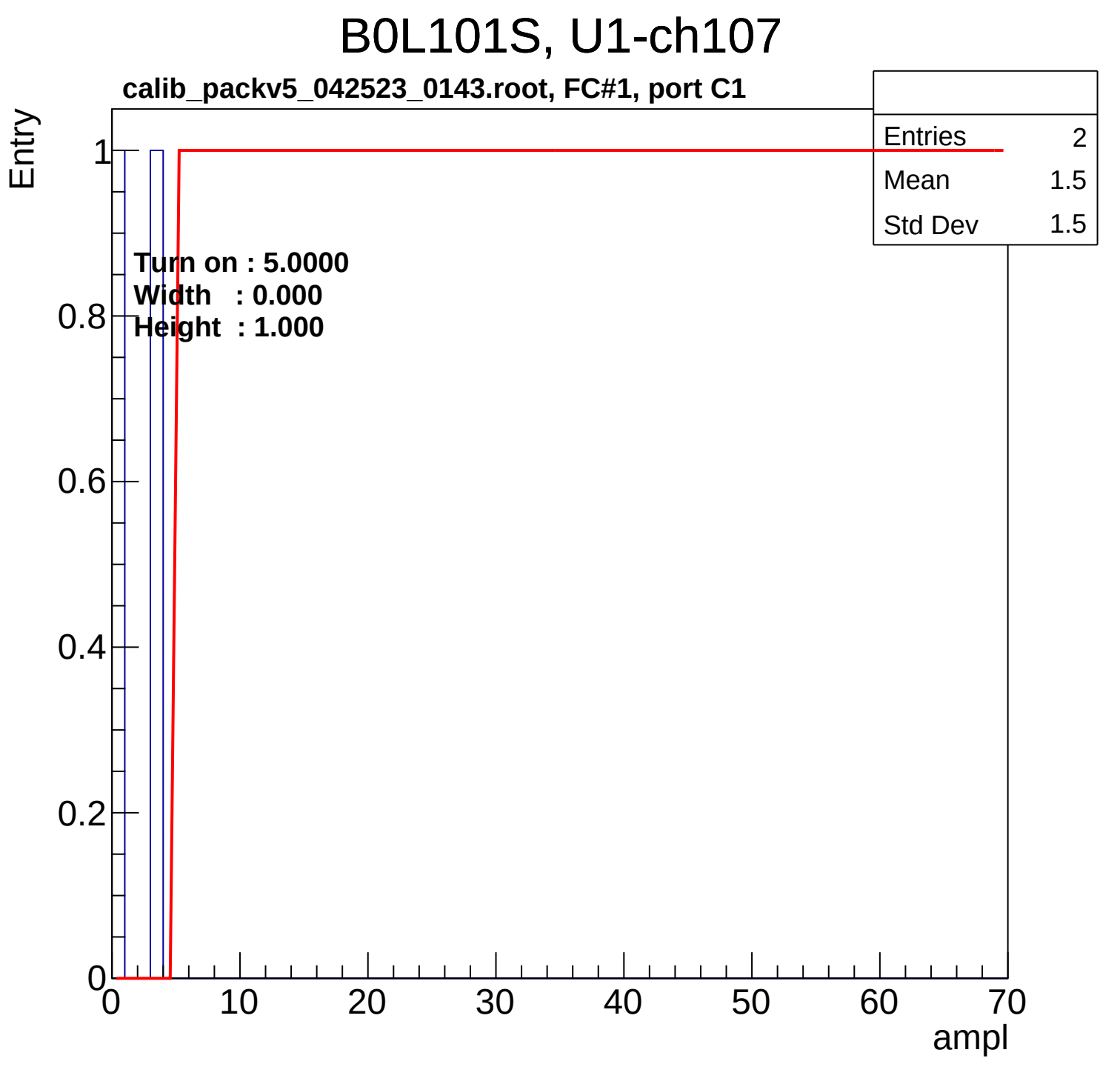

B0L101S, U1-ch102
calib_packv5_042523_0143.root, FC#1, port C1
Entries 7
Mean 24.43
Std Dev 19.52
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

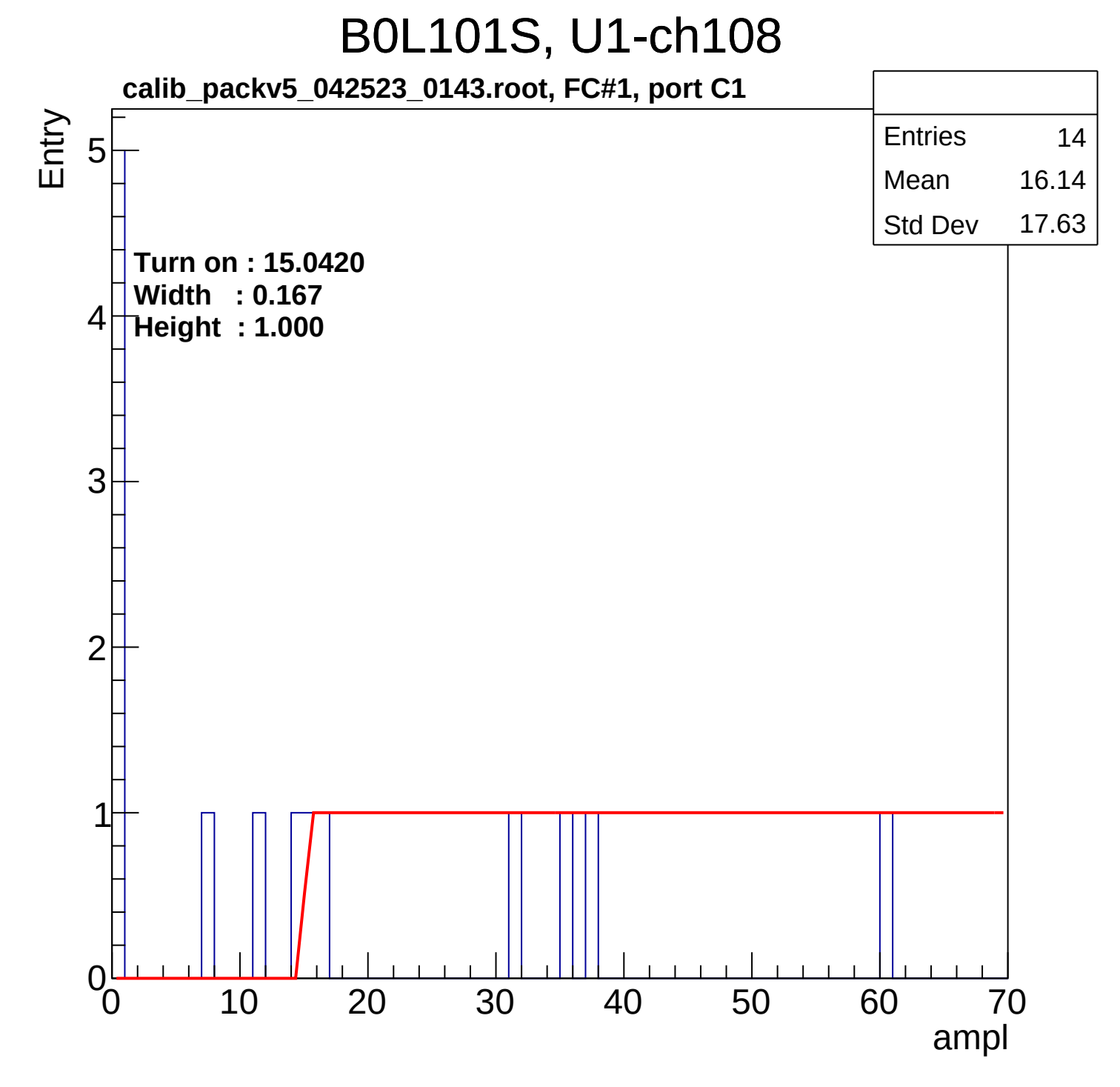

B0L101S, U1-ch103
calib_packv5_042523_0143.root, FC#1, port C1
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

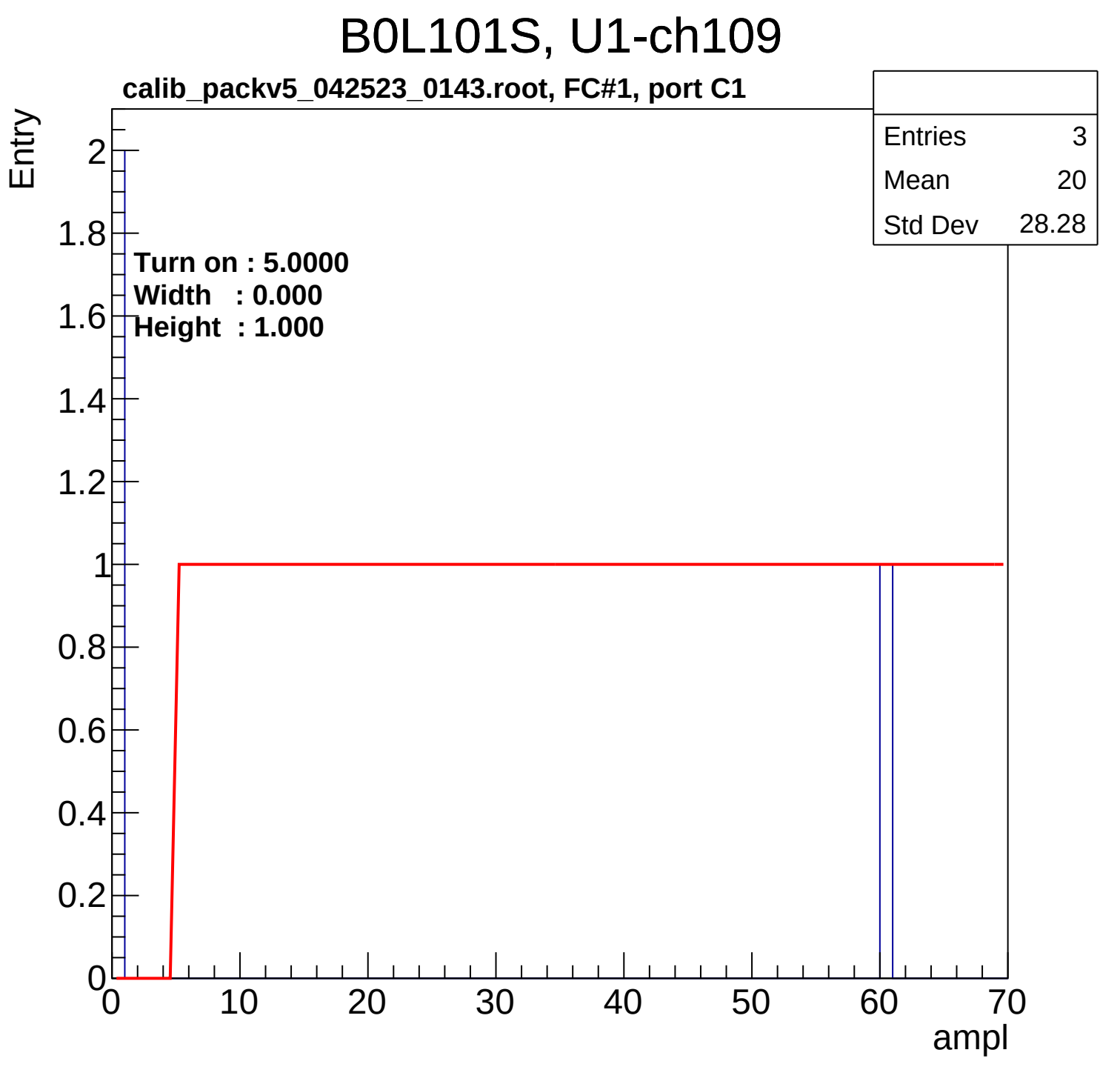

B0L101S, U1-ch104
calib_packv5_042523_0143.root, FC#1, port C1
Entries 7
Mean 14.57
Std Dev 16.44
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

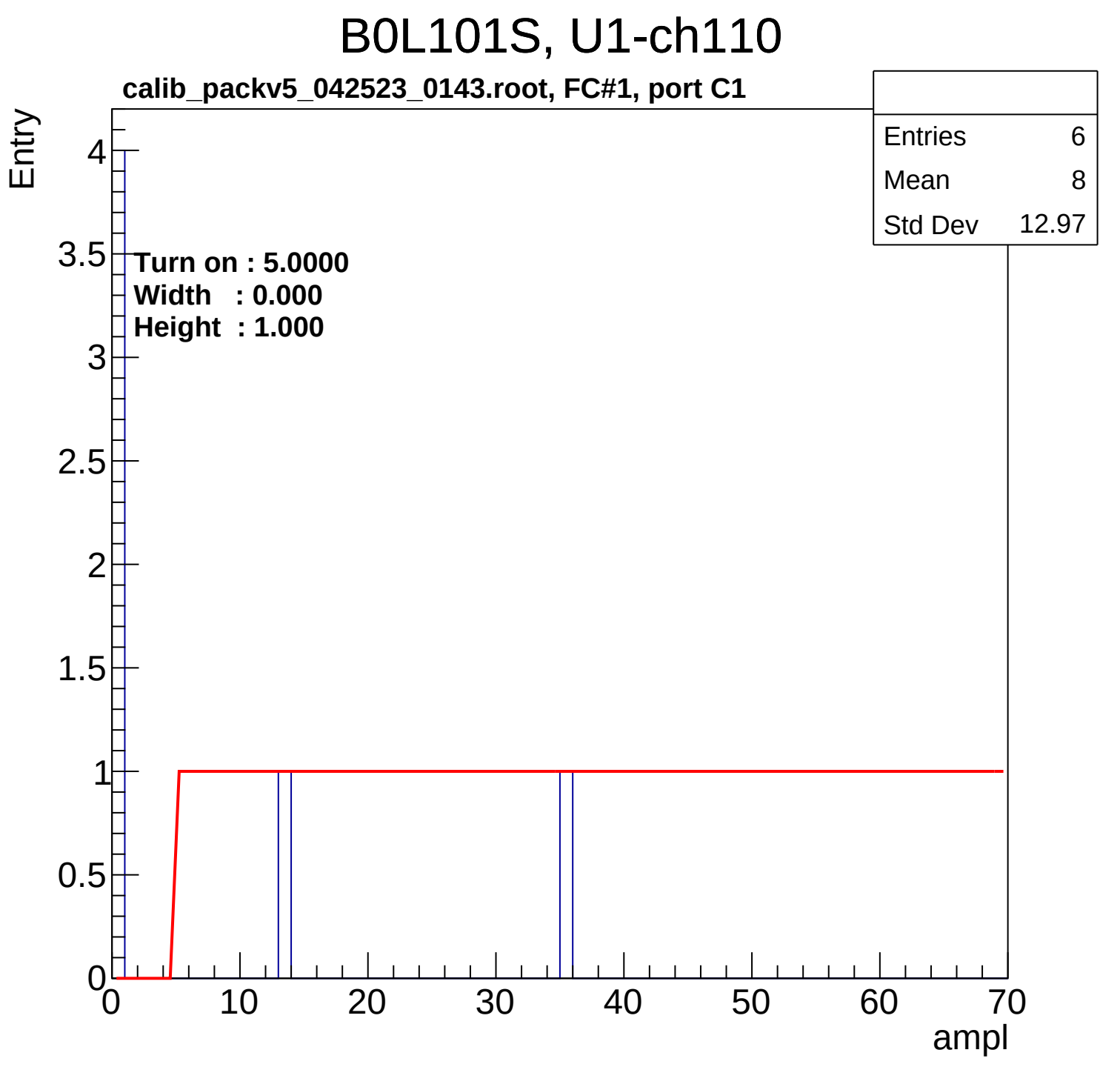

B0L101S, U1-ch105
calib_packv5_042523_0143.root, FC#1, port C1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

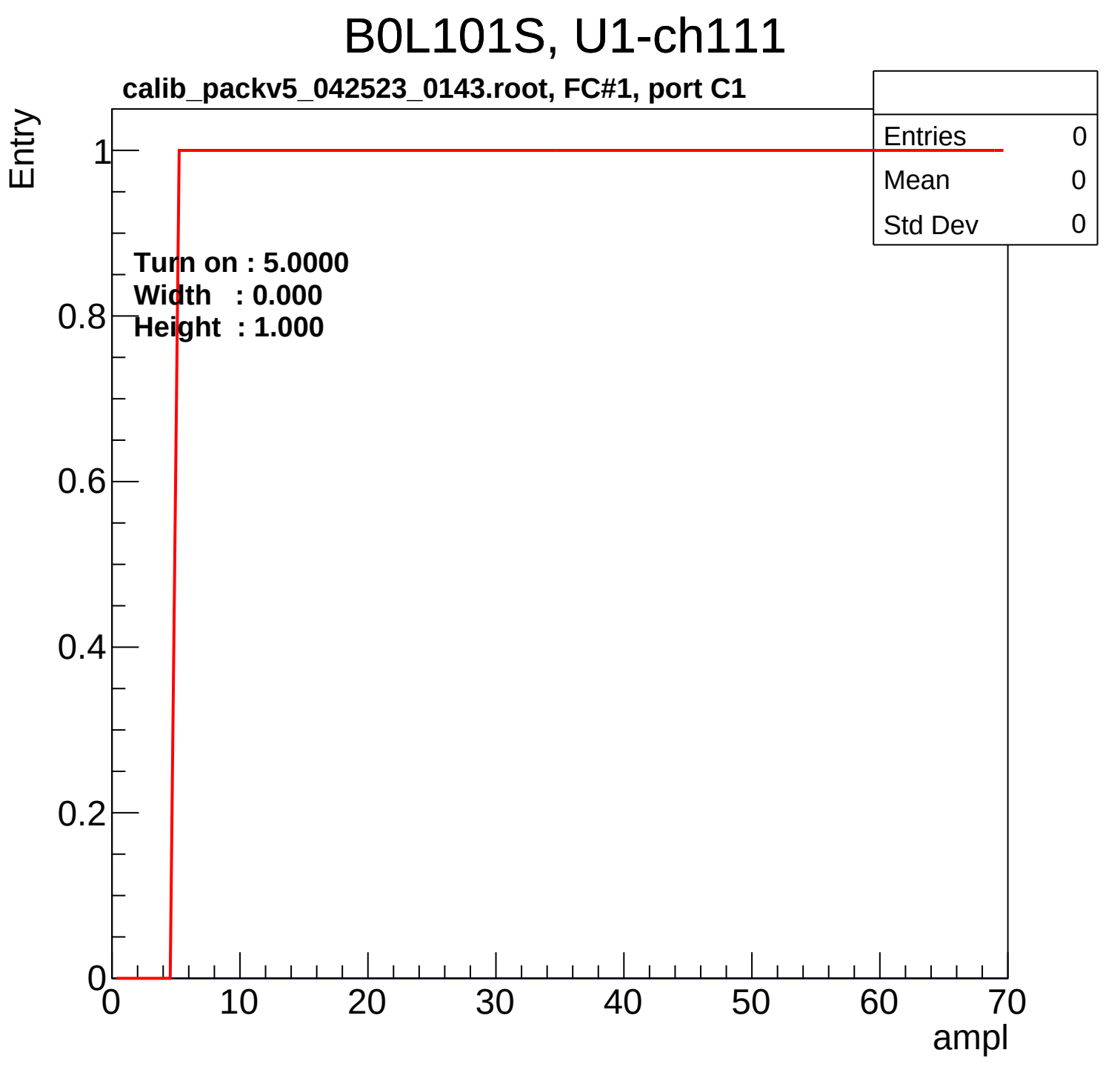

B0L101S, U1-ch106
calib_packv5_042523_0143.root, FC#1, port C1
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

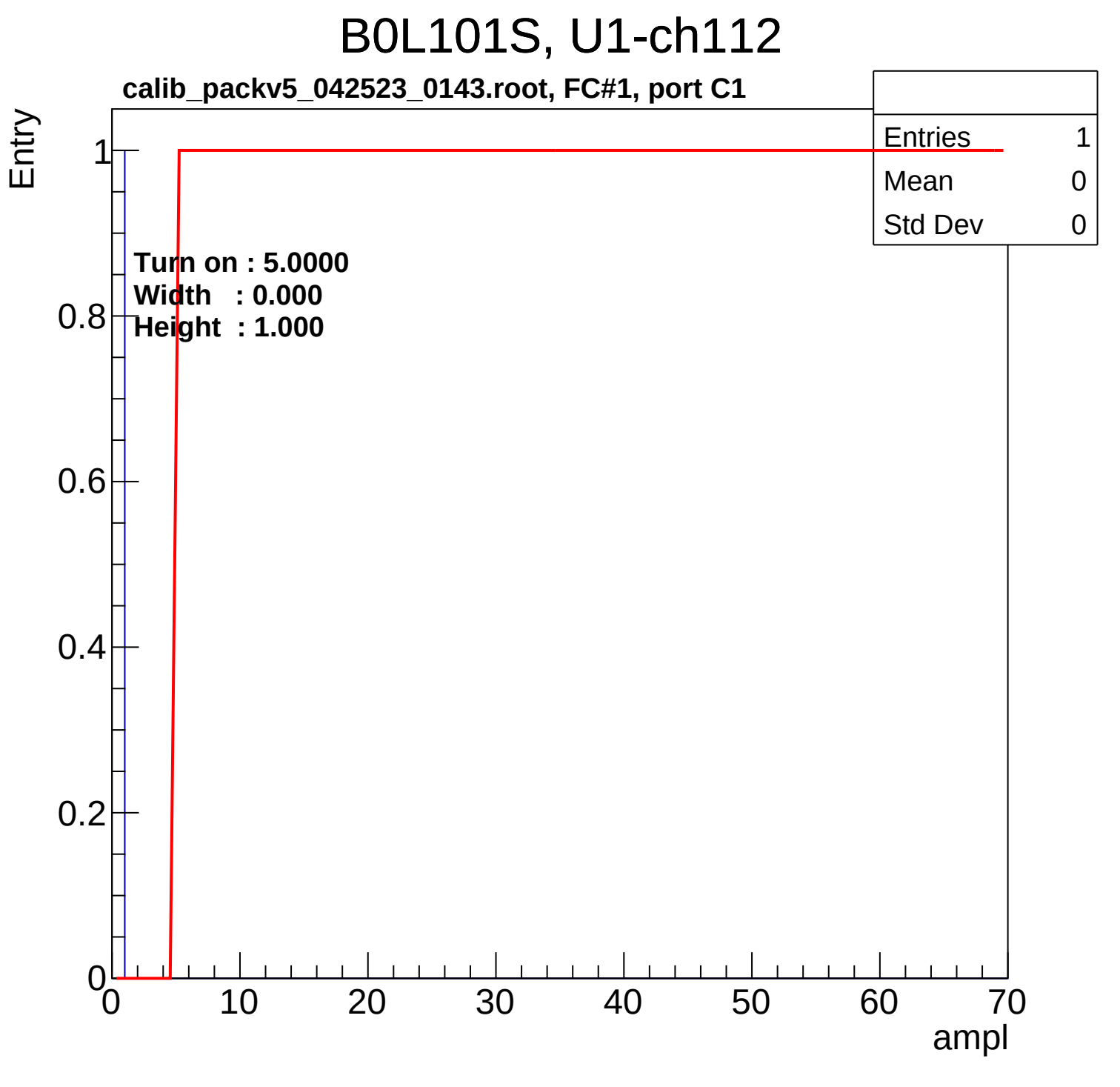

B0L101S, U1-ch107
calib_packv5_042523_0143.root, FC#1, port C1
Entries 2
Mean 1.5
Std Dev 1.5
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

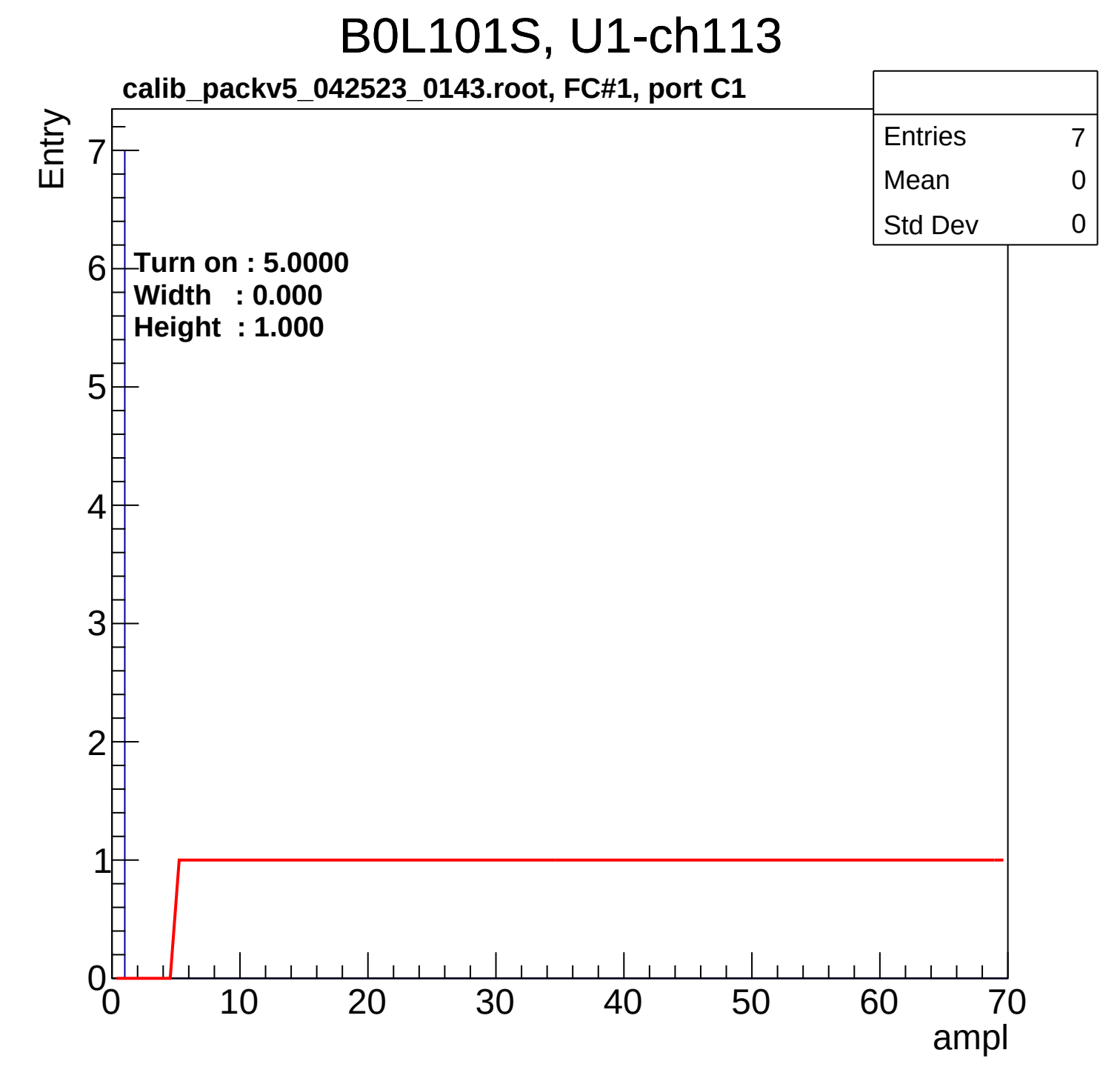

B0L101S, U1-ch108
calib_packv5_042523_0143.root, FC#1, port C1
Entries 14
Mean 16.14
Std Dev 17.63
Turn on : 15.0420
Width : 0.167
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

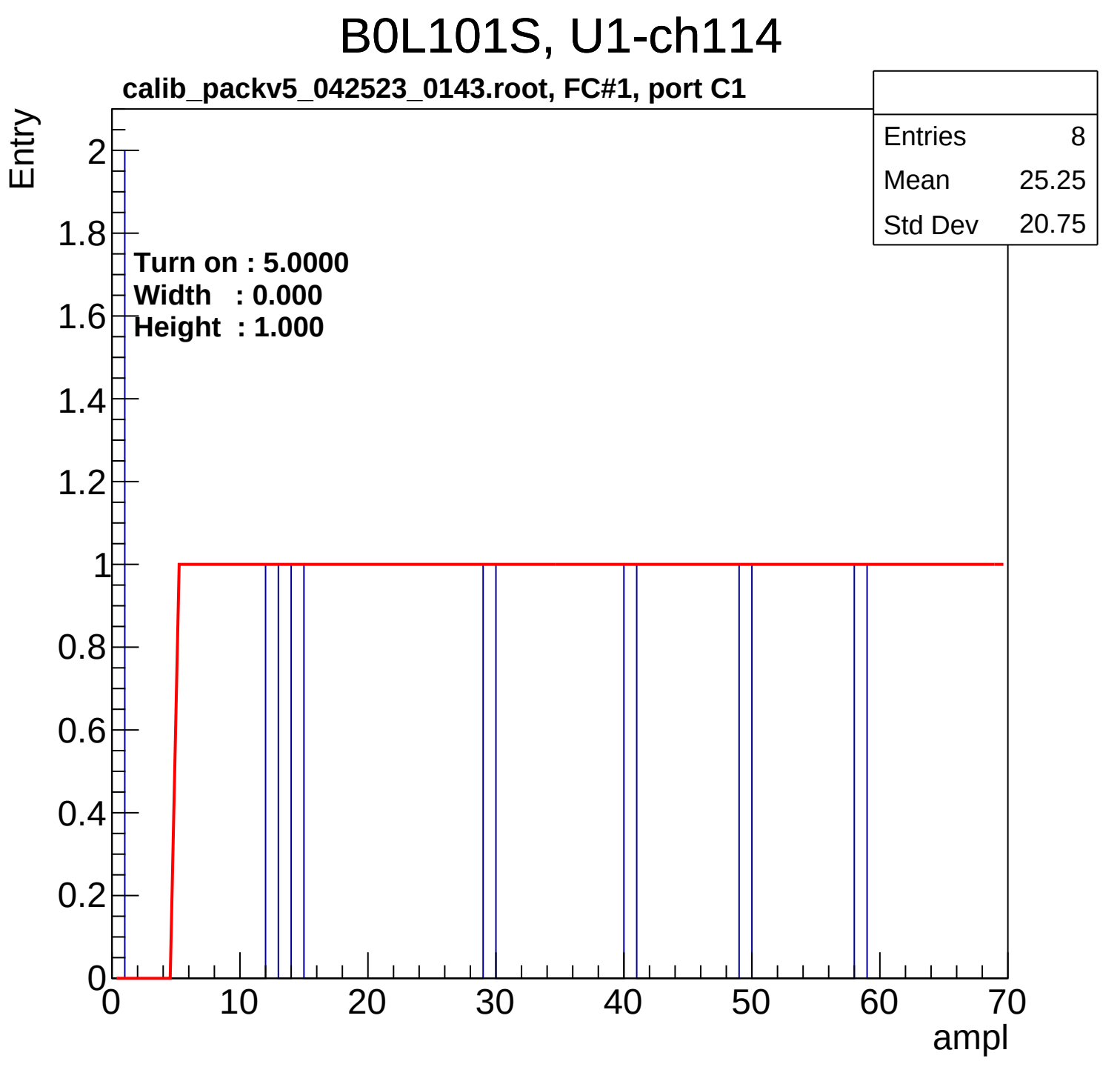

B0L101S, U1-ch109
calib_packv5_042523_0143.root, FC#1, port C1
Entries 3
Mean 20
Std Dev 28.28
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

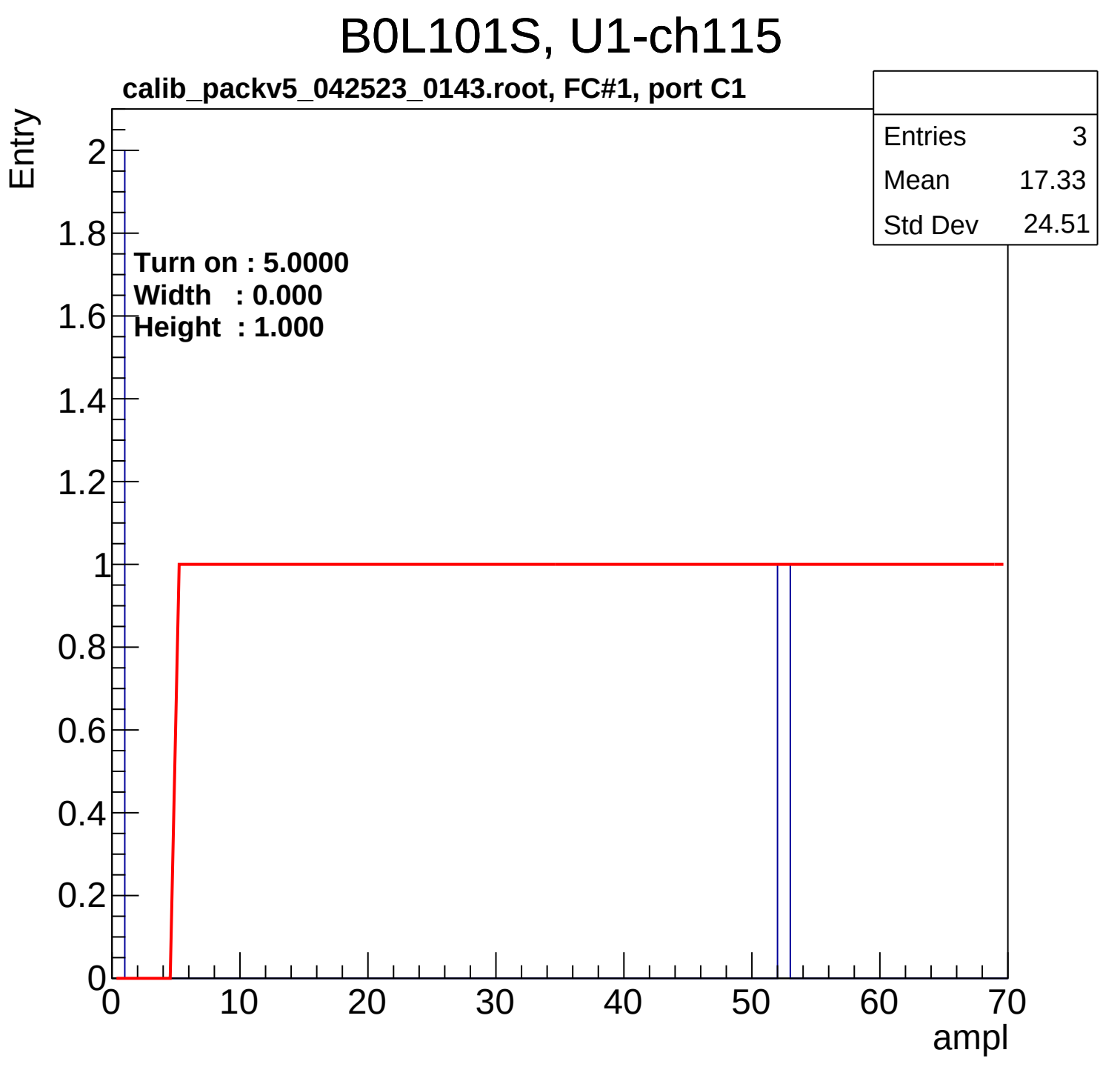

B0L101S, U1-ch110
calib_packv5_042523_0143.root, FC#1, port C1
Entries 6
Mean 8
Std Dev 12.97
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

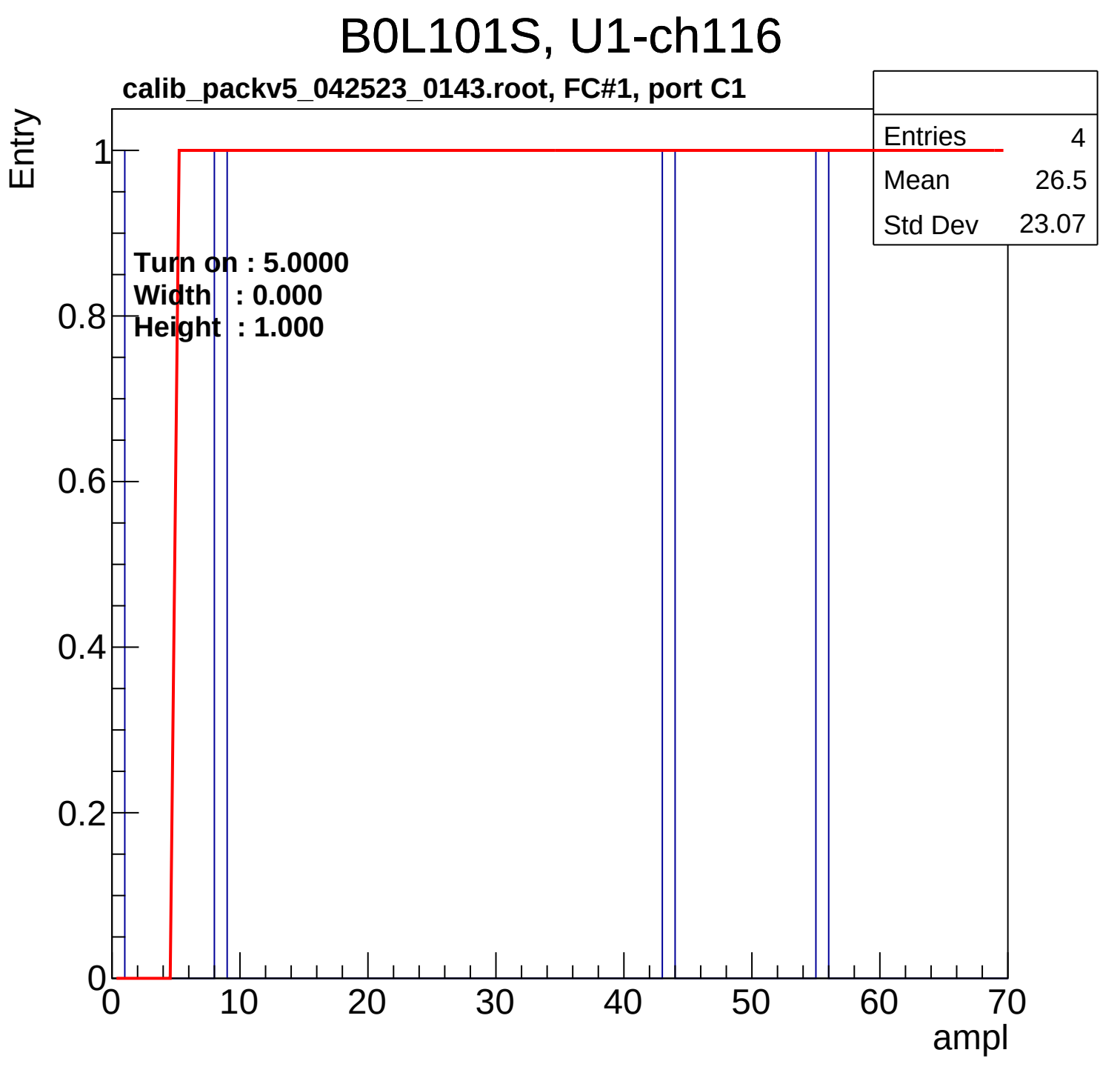

B0L101S, U1-ch111
calib_packv5_042523_0143.root, FC#1, port C1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

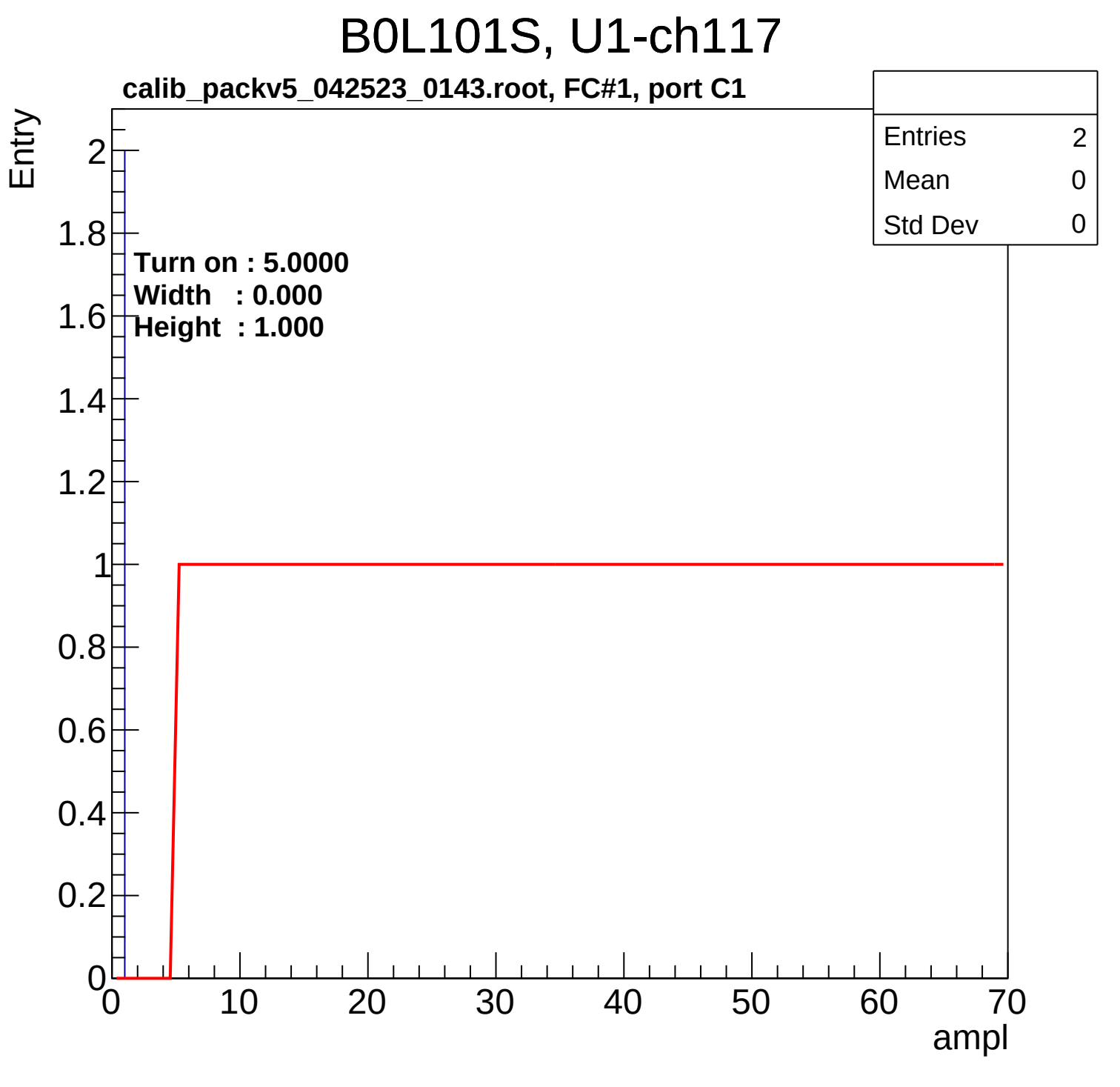

B0L101S, U1-ch112
calib_packv5_042523_0143.root, FC#1, port C1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

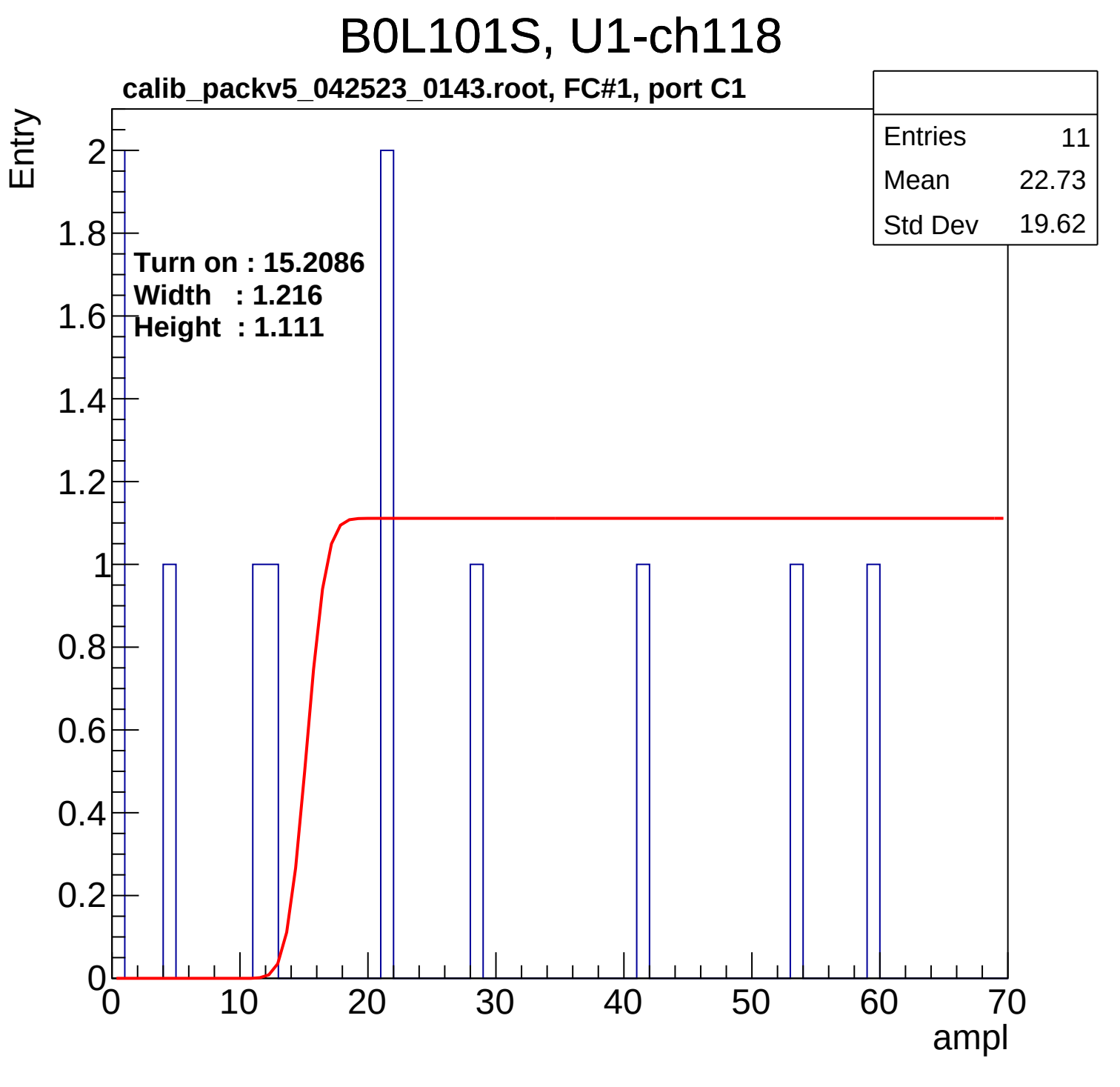

B0L101S, U1-ch113
calib_packv5_042523_0143.root, FC#1, port C1
Entries 7
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

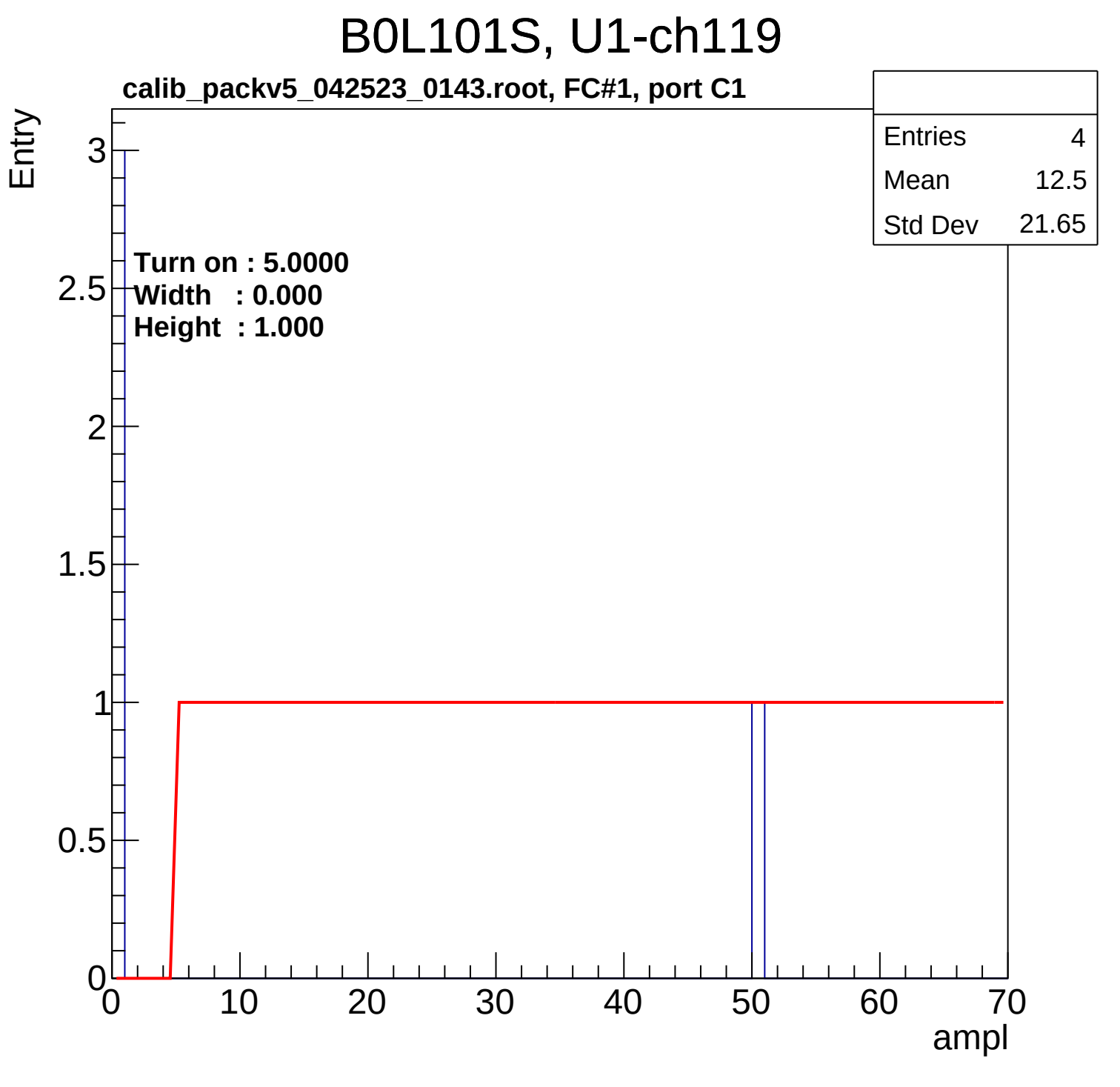

B0L101S, U1-ch114
calib_packv5_042523_0143.root, FC#1, port C1
Entries 8
Mean 25.25
Std Dev 20.75
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

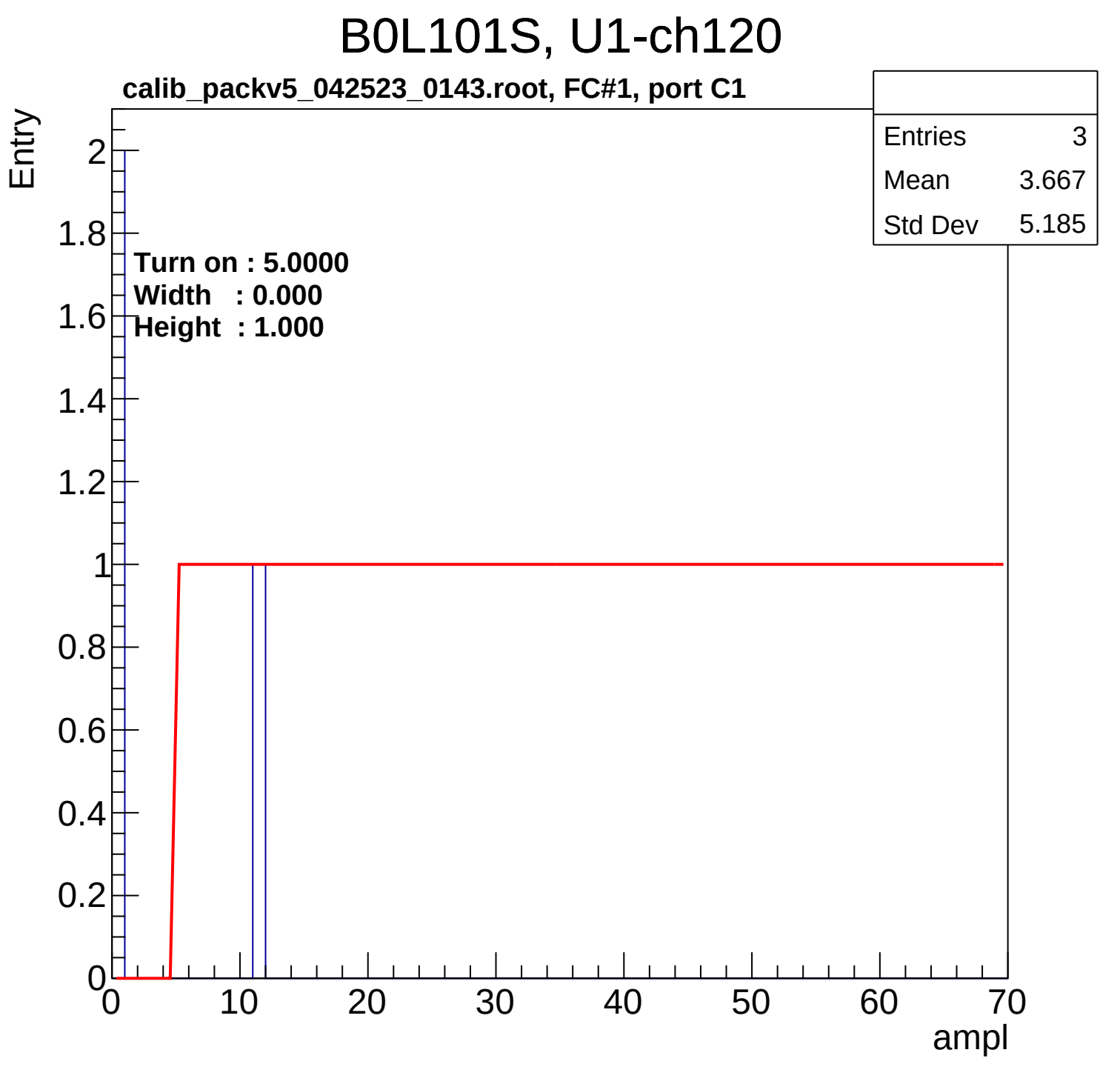

B0L101S, U1-ch115
calib_packv5_042523_0143.root, FC#1, port C1
Entries 3
Mean 17.33
Std Dev 24.51
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

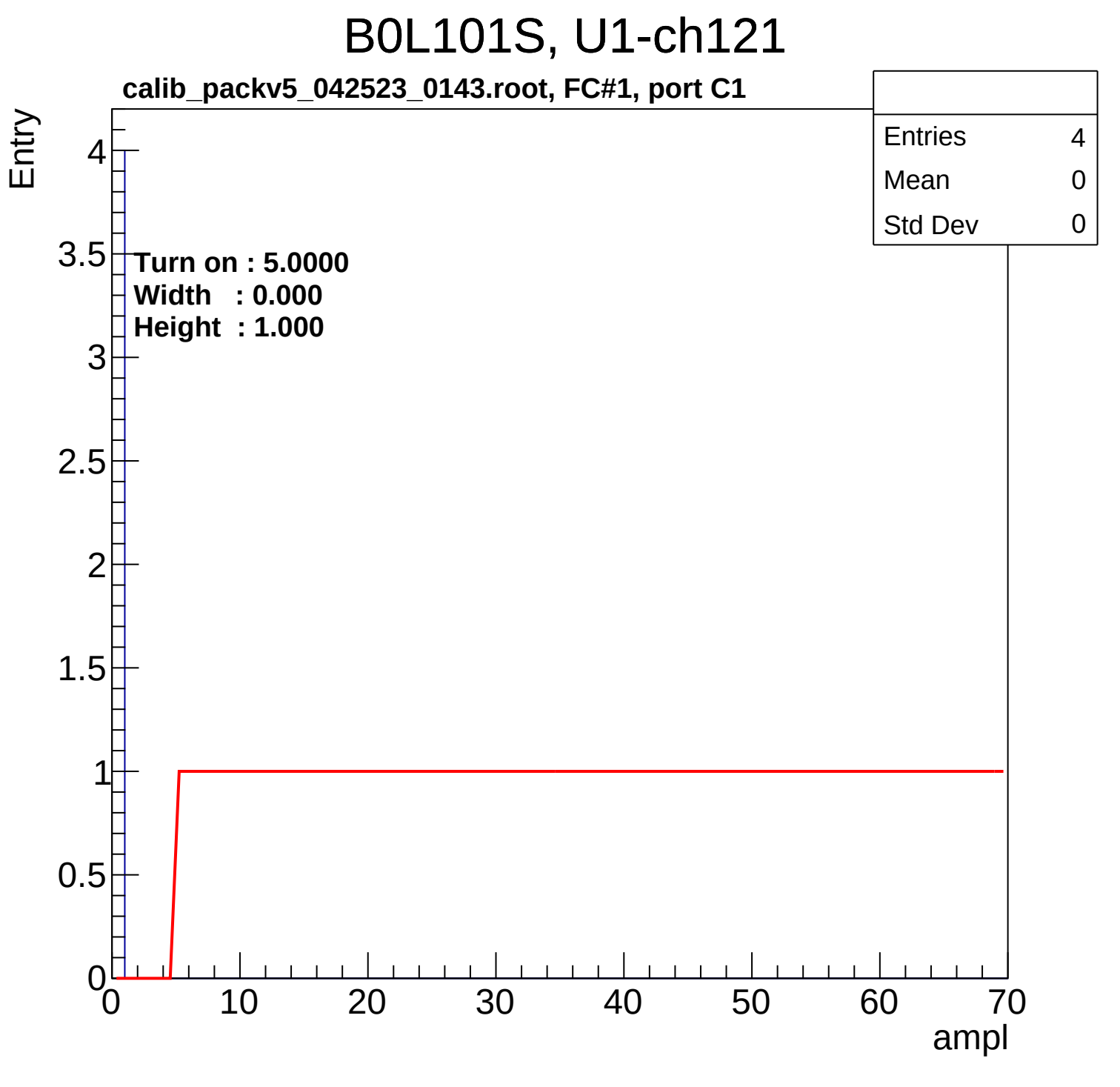

B0L101S, U1-ch116
calib_packv5_042523_0143.root, FC#1, port C1
Entries 4
Mean 26.5
Std Dev 23.07
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

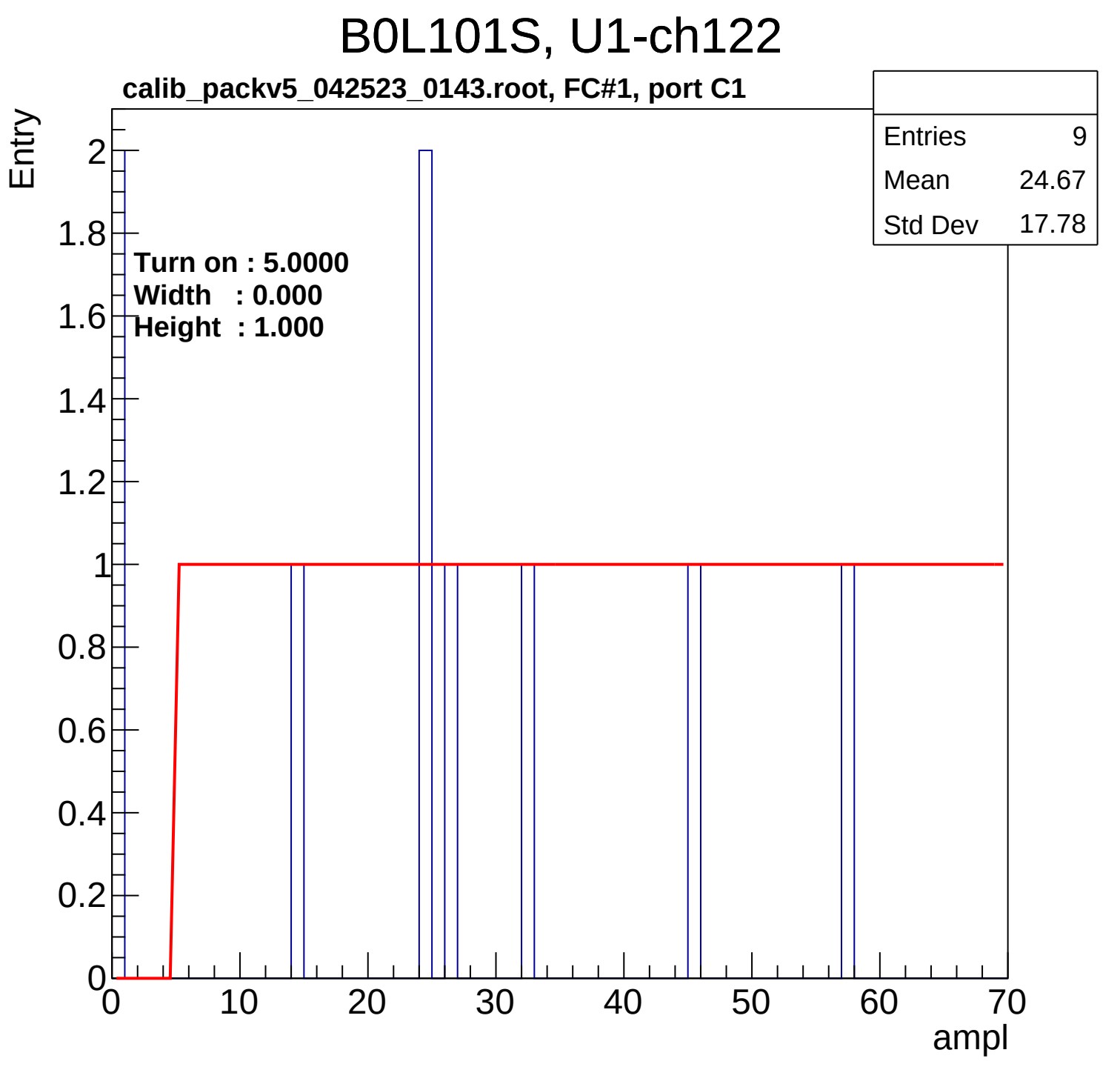

B0L101S, U1-ch117
calib_packv5_042523_0143.root, FC#1, port C1
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

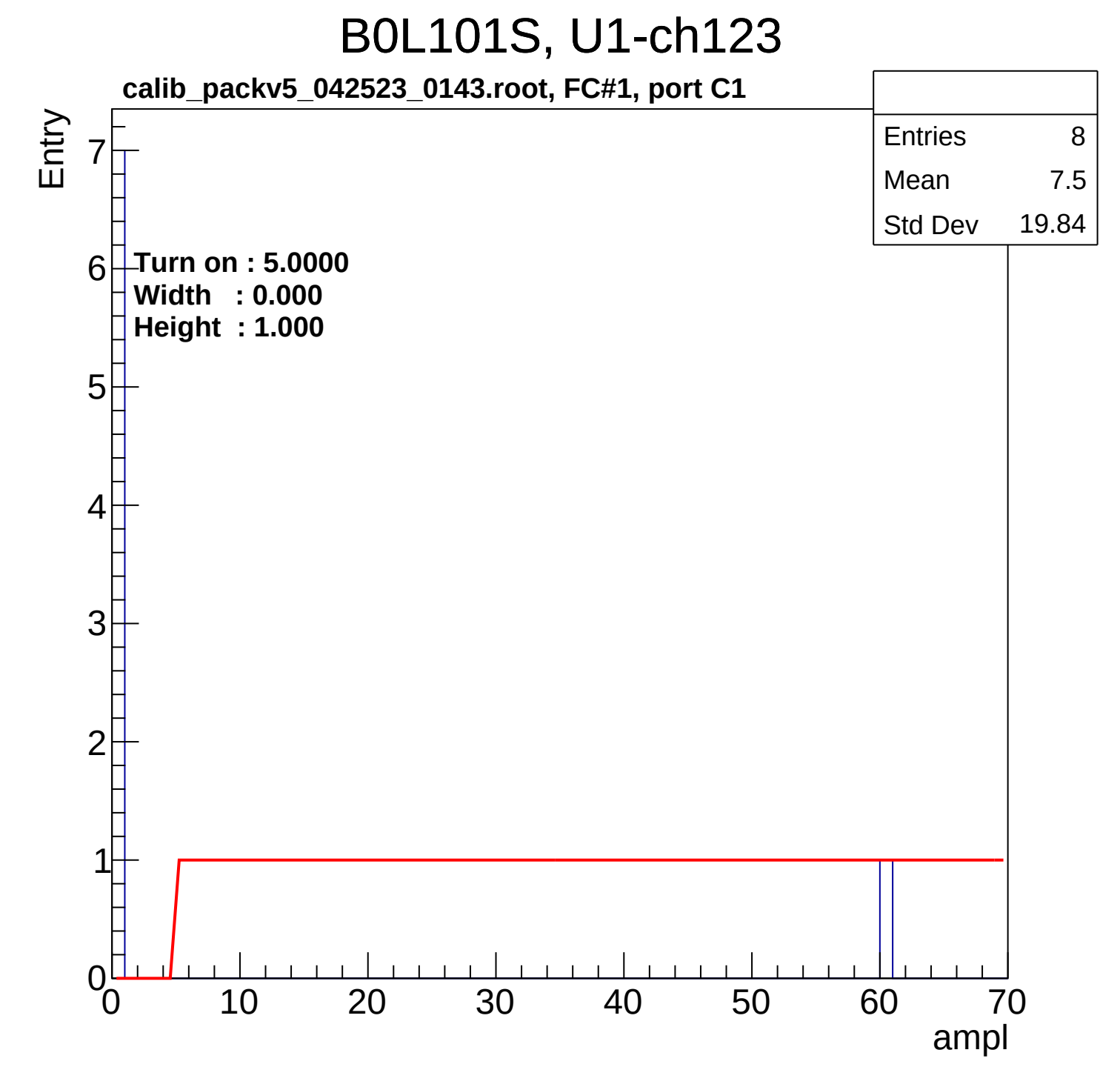

B0L101S, U1-ch118
calib_packv5_042523_0143.root, FC#1, port C1
Entries 11
Mean 22.73
Std Dev 19.62
Turn on : 15.2086
Width : 1.216
Height : 1.111
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

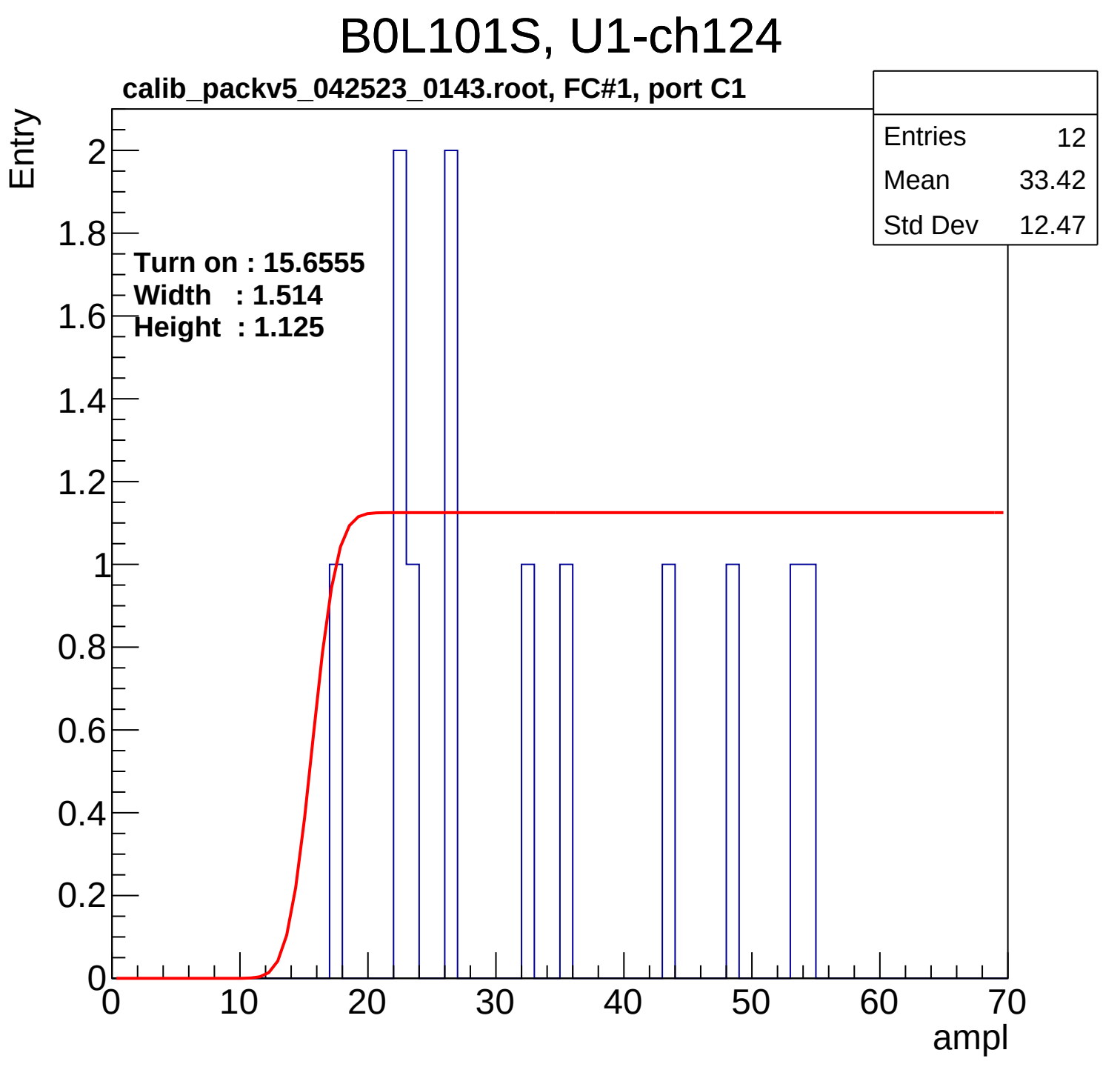

B0L101S, U1-ch119
calib_packv5_042523_0143.root, FC#1, port C1
Entries 4
Mean 12.5
Std Dev 21.65
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

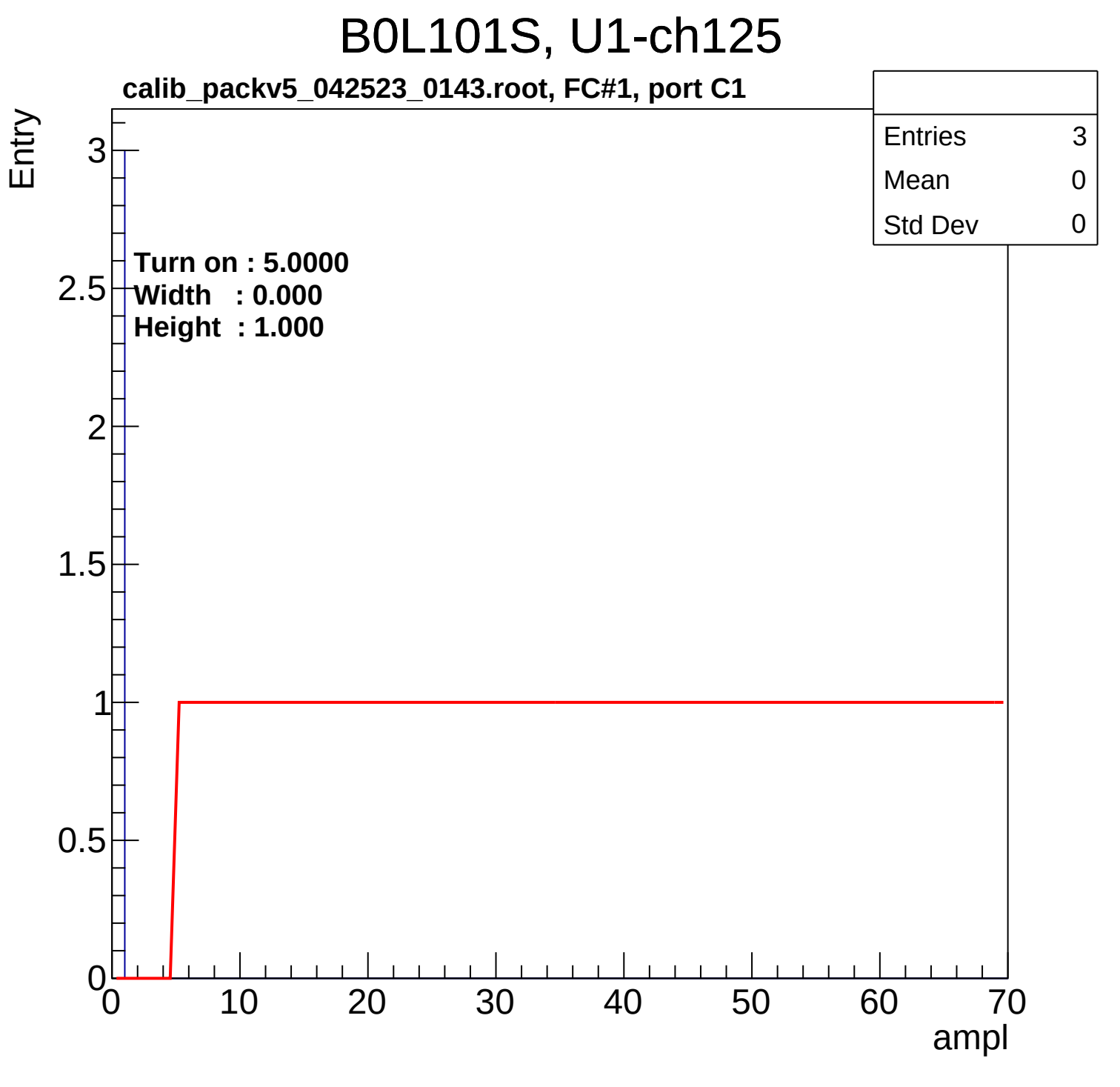

B0L101S, U1-ch120
calib_packv5_042523_0143.root, FC#1, port C1
Entries 3
Mean 3.667
Std Dev 5.185
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

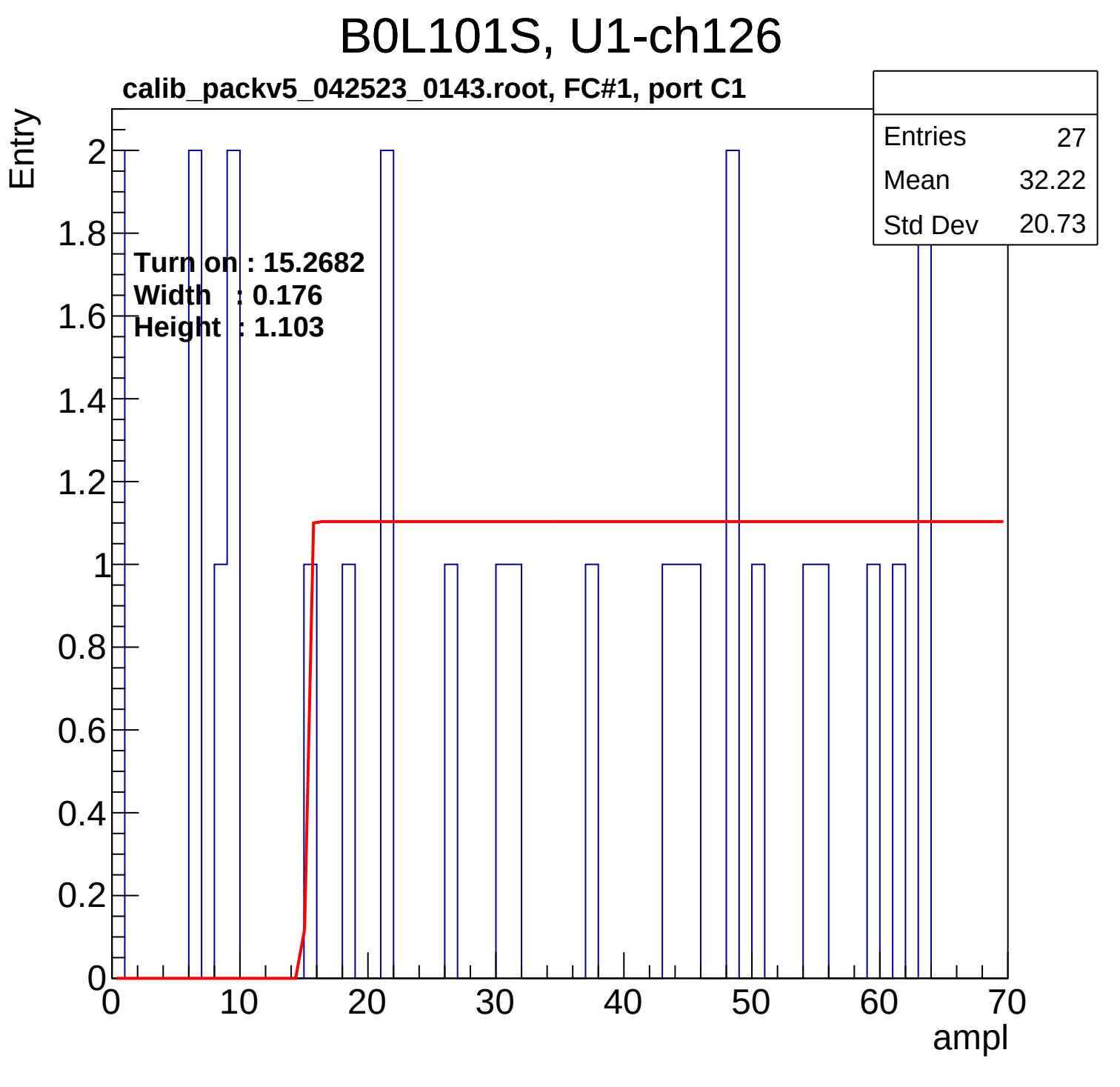

B0L101S, U1-ch121
calib_packv5_042523_0143.root, FC#1, port C1
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

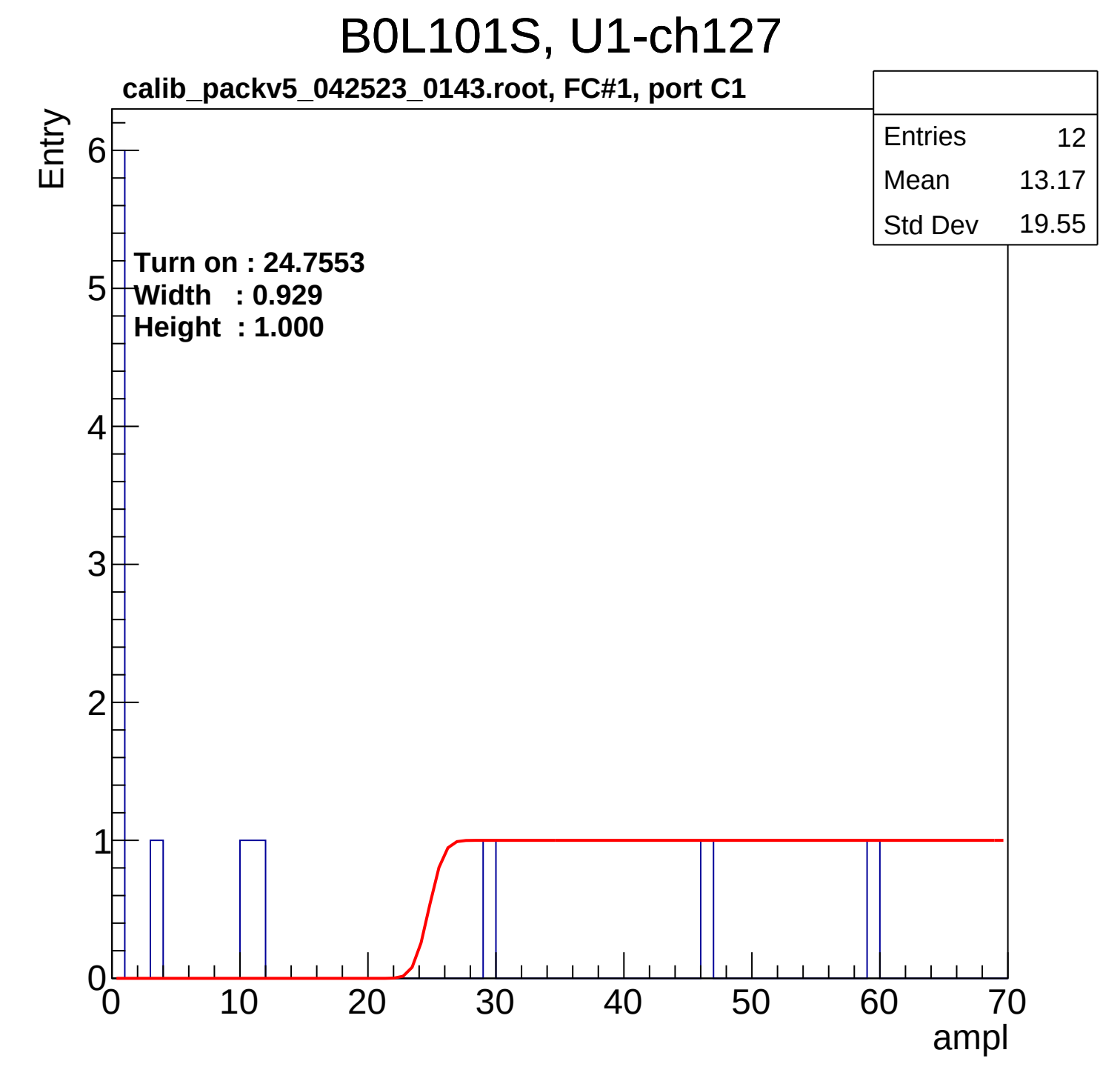

B0L101S, U1-ch122
calib_packv5_042523_0143.root, FC#1, port C1
Entries 9
Mean 24.67
Std Dev 17.78
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

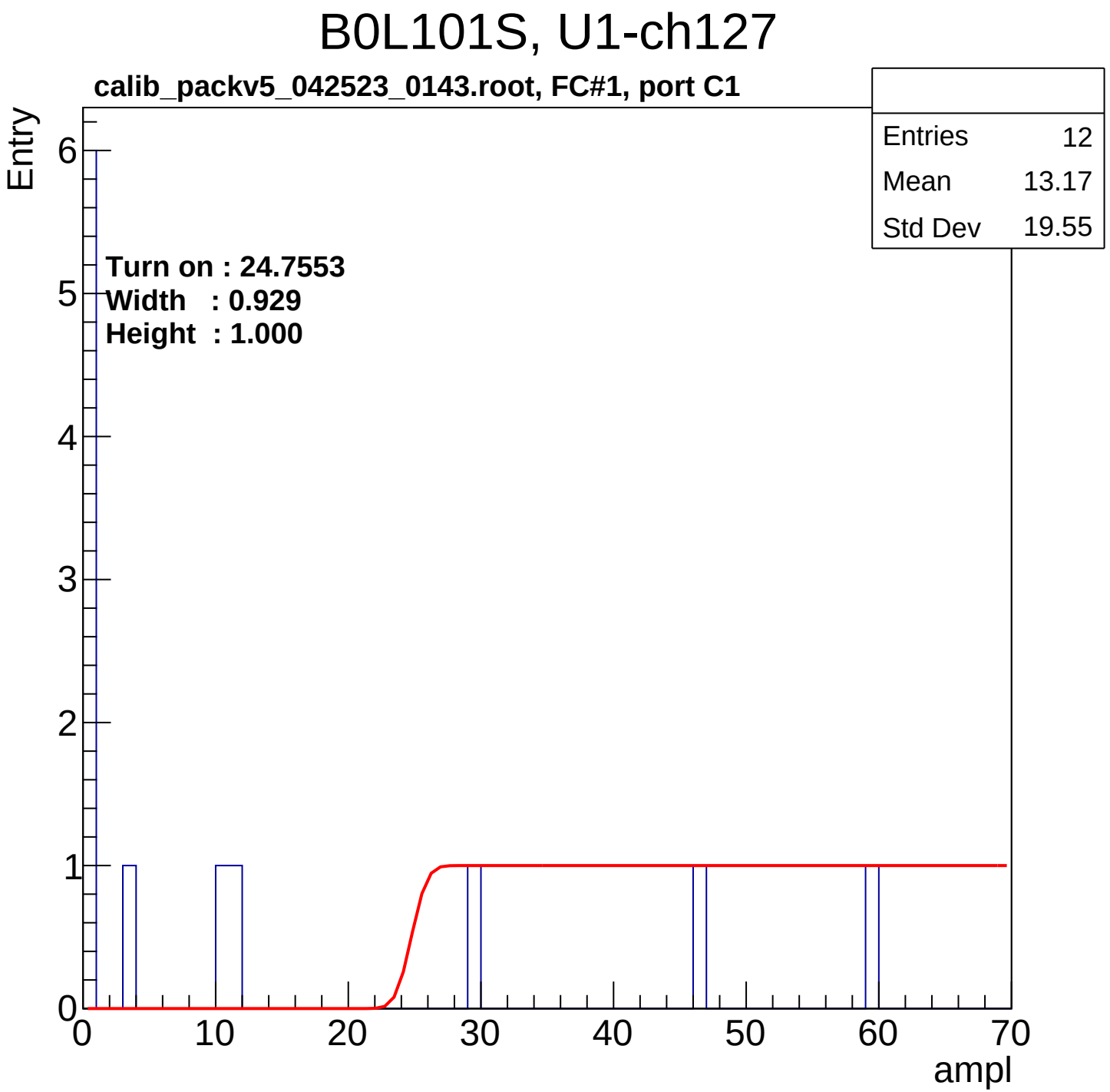

B0L101S, U1-ch123
calib_packv5_042523_0143.root, FC#1, port C1
Entries 8
Mean 7.5
Std Dev 19.84
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B0L101S, U1-ch124
calib_packv5_042523_0143.root, FC#1, port C1
Entries 12
Mean 33.42
Std Dev 12.47
Turn on : 15.6555
Width : 1.514
Height : 1.125
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L101S, U1-ch125
calib_packv5_042523_0143.root, FC#1, port C1
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B0L101S, U1-ch126
calib_packv5_042523_0143.root, FC#1, port C1
Entries 27
Mean 32.22
Std Dev 20.73
Turn on : 15.2682
Width : 0.176
Height : 1.103
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L101S, U1-ch127
calib_packv5_042523_0143.root, FC#1, port C1
Entries 12
Mean 13.17
Std Dev 19.55
Turn on : 24.7553
Width : 0.929
Height : 1.000
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B0L101S, U1-ch127
calib_packv5_042523_0143.root, FC#1, port C1
Entries 12
Mean 13.17
Std Dev 19.55
Turn on : 24.7553
Width : 0.929
Height : 1.000
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70