



# B1L101S, U7-ch0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	388
Mean	43.53
Std Dev	12.58

**Turn on : 26.7075**

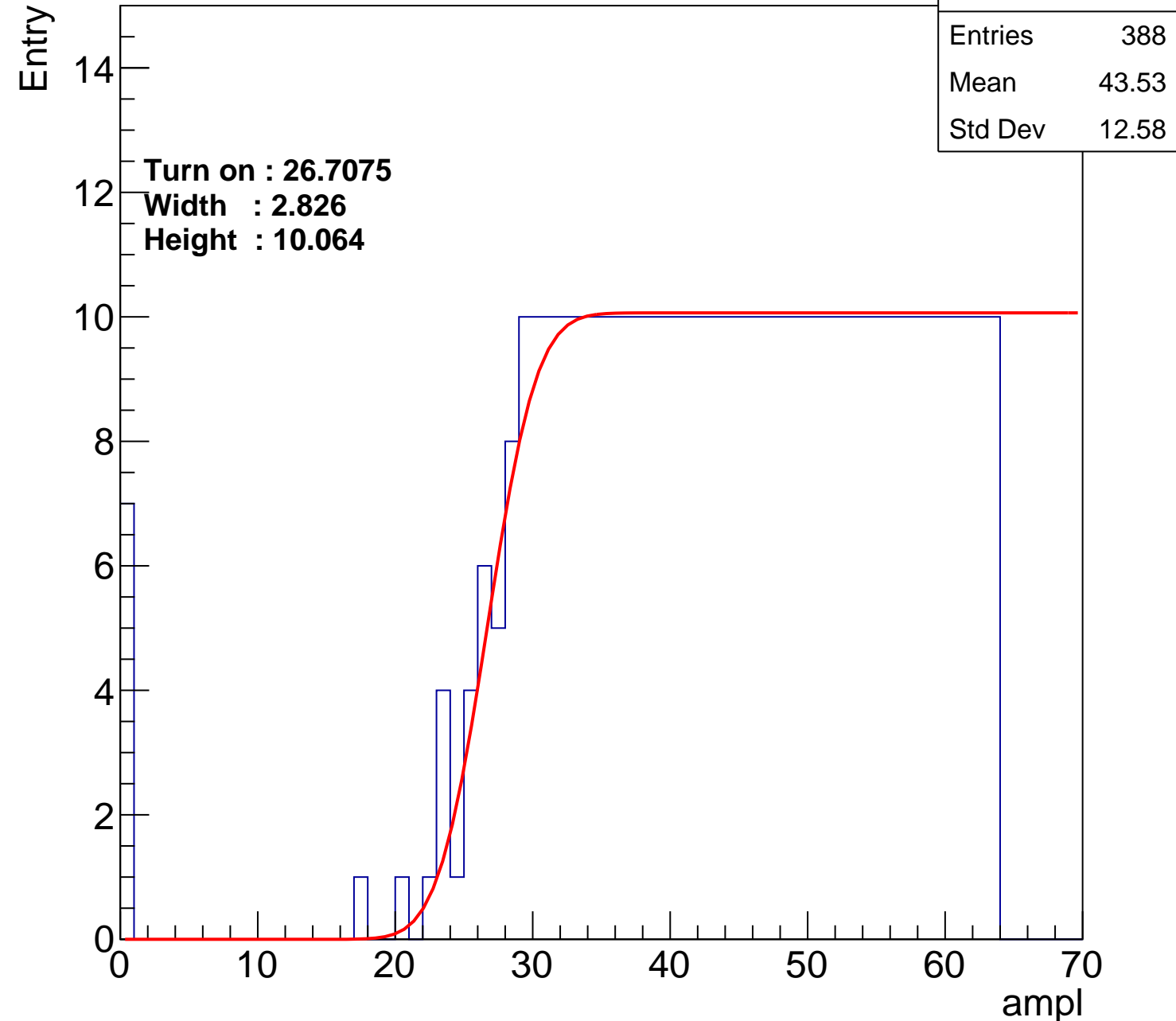
**Width : 2.826**

**Height : 10.064**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	375
Mean	44.51
Std Dev	11.39

Turn on : 26.9328

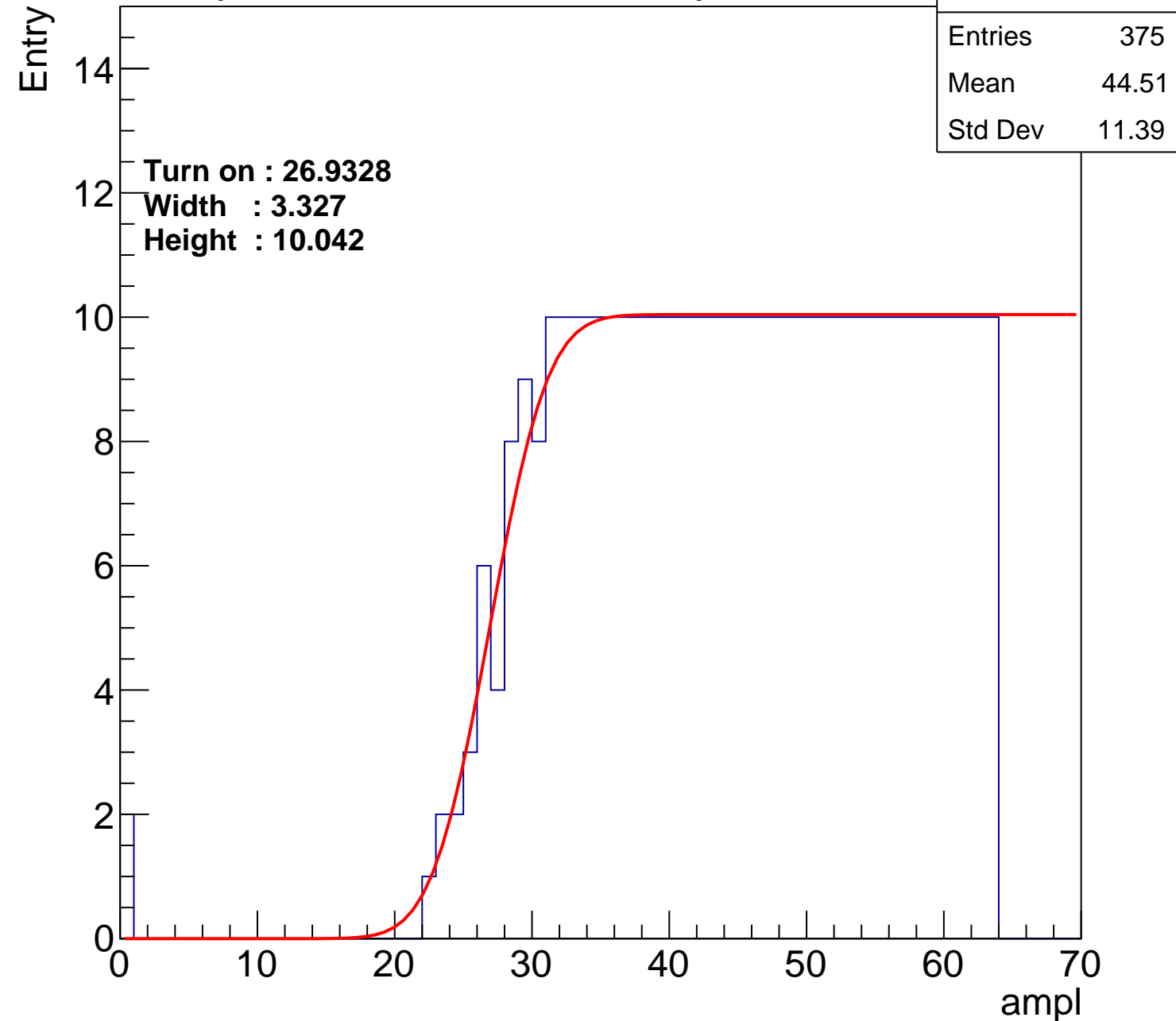
Width : 3.327

Height : 10.042

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	366
Mean	44.81
Std Dev	11.48

Turn on : 27.3930

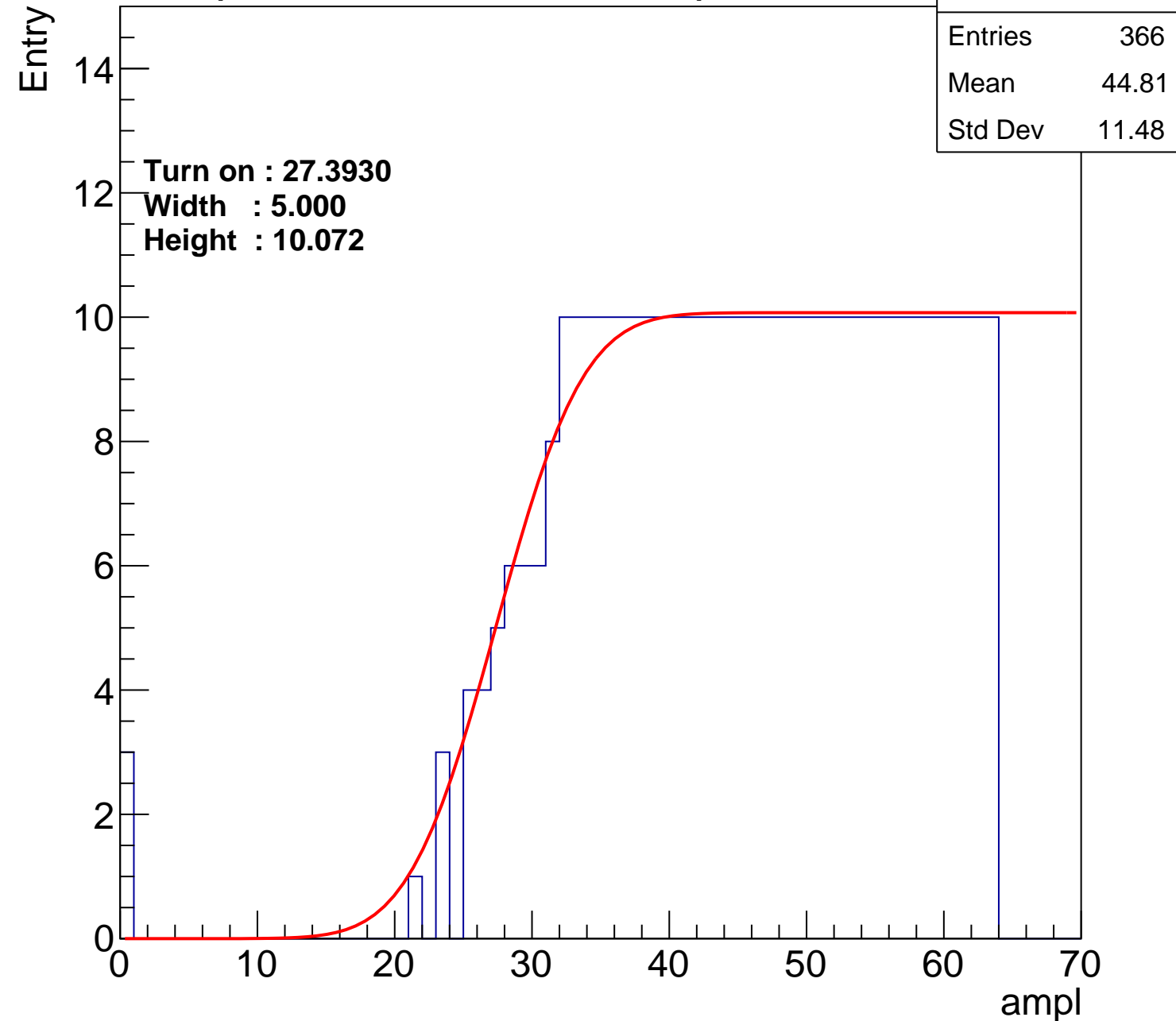
Width : 5.000

Height : 10.072

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	350
Mean	45.55
Std Dev	11.26

Turn on : 30.1295

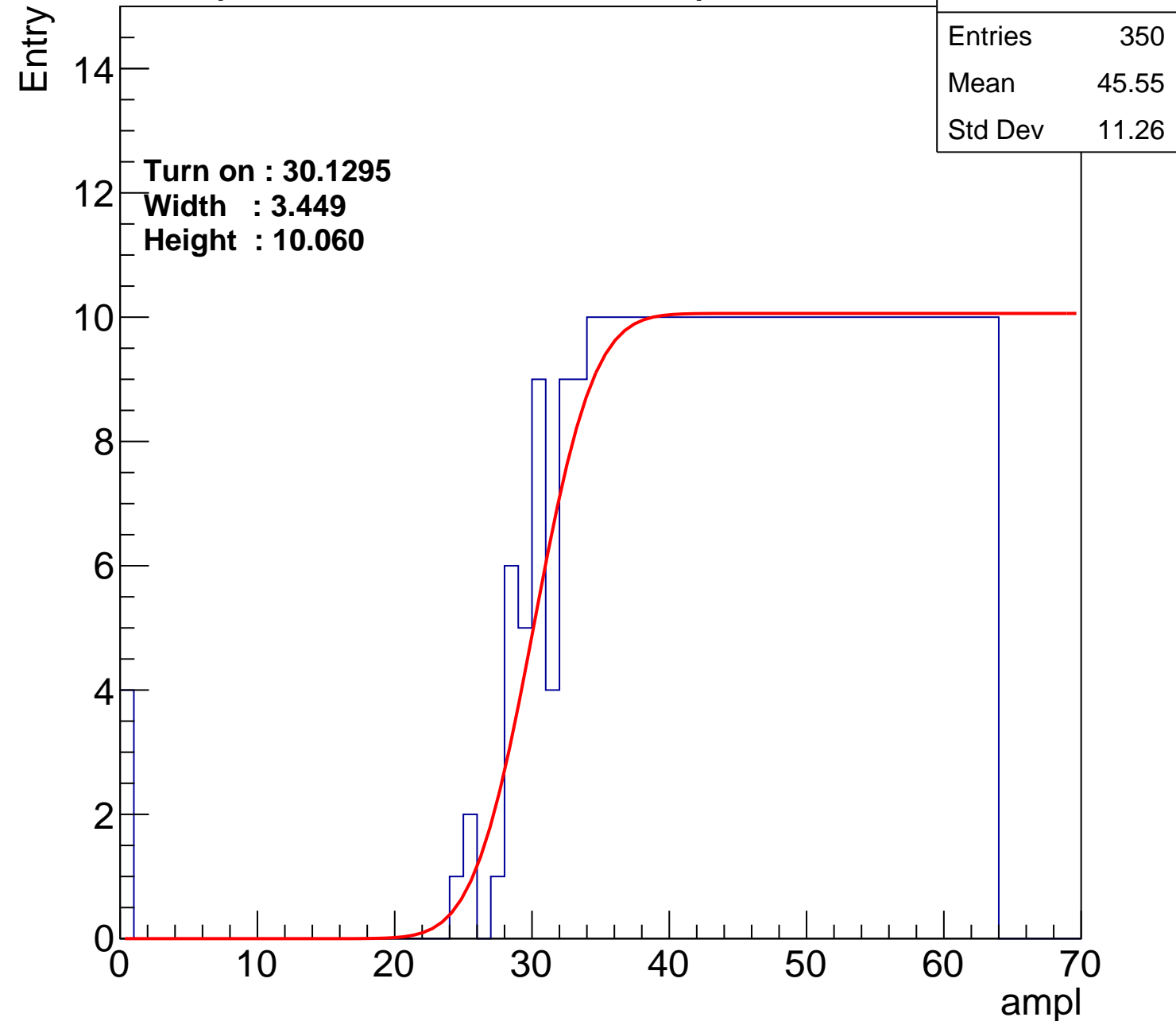
Width : 3.449

Height : 10.060

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch4

calib\_packv5\_042523\_0143.root, FC#0, port D2

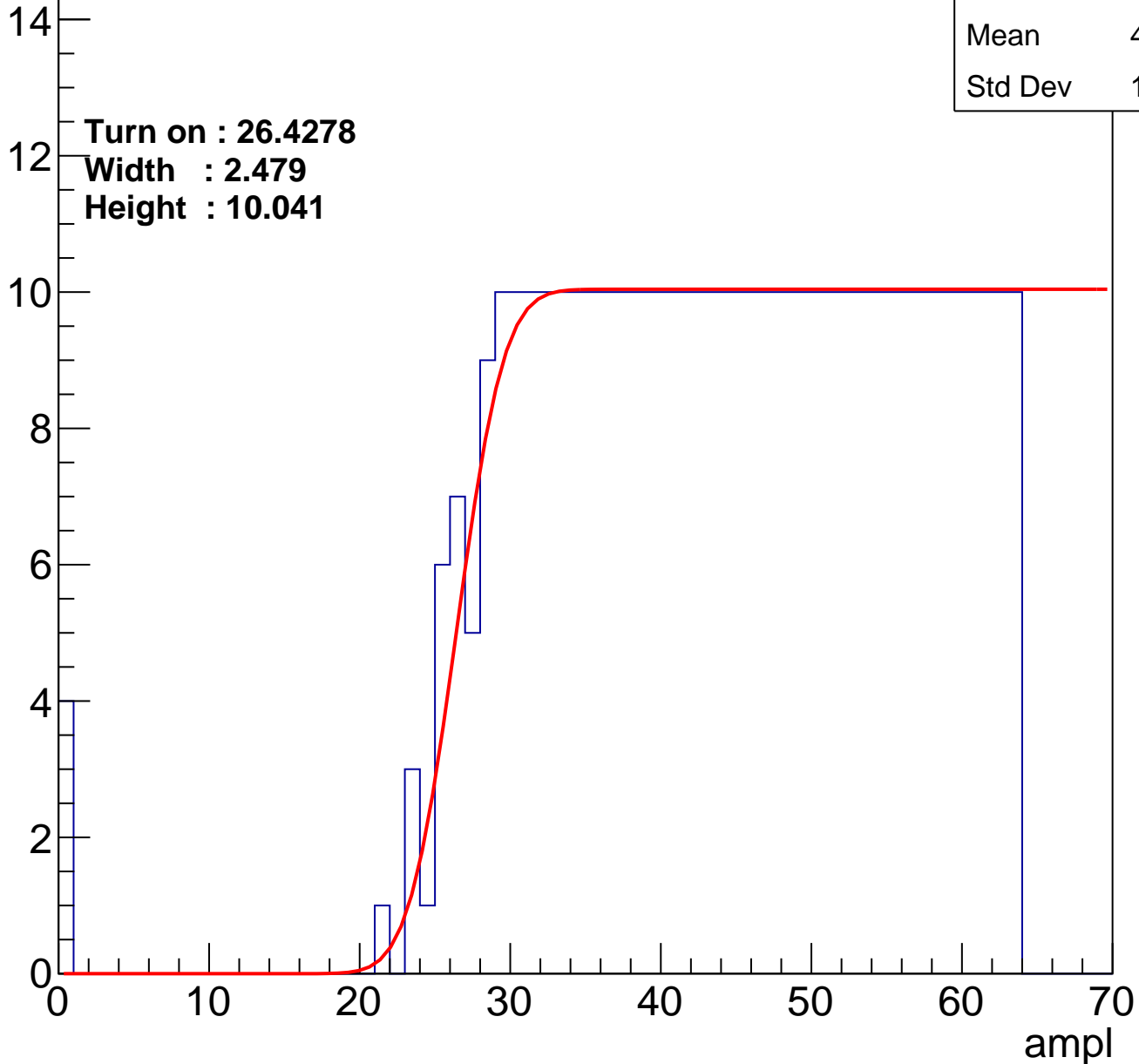
Entries	386
Mean	43.87
Std Dev	11.97

Turn on : 26.4278

Width : 2.479

Height : 10.041

Entry



# B1L101S, U7-ch5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	382
Mean	44.26
Std Dev	11.34

Turn on : 26.1780

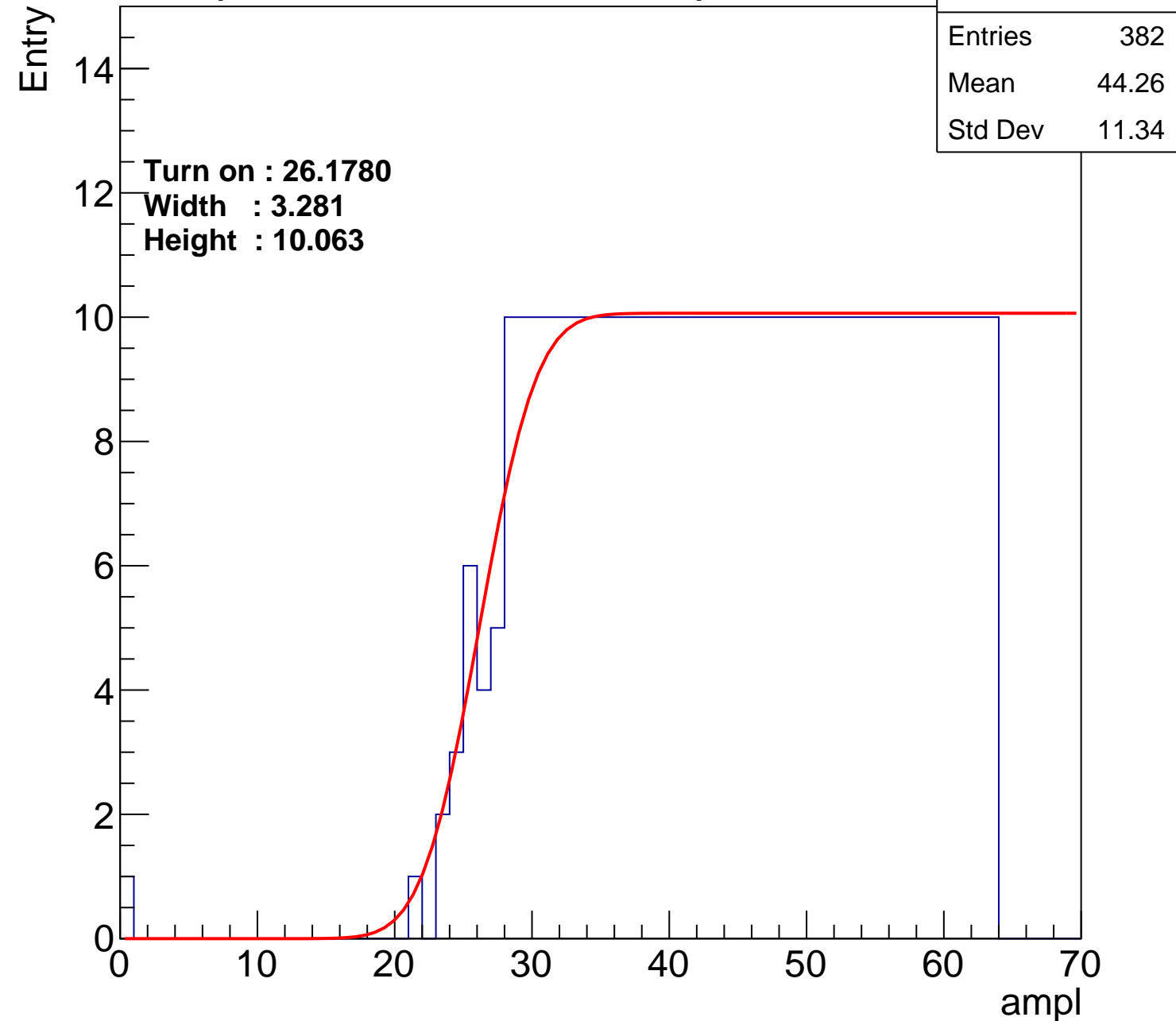
Width : 3.281

Height : 10.063

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	382
Mean	44.05
Std Dev	11.9

Turn on : 26.1452

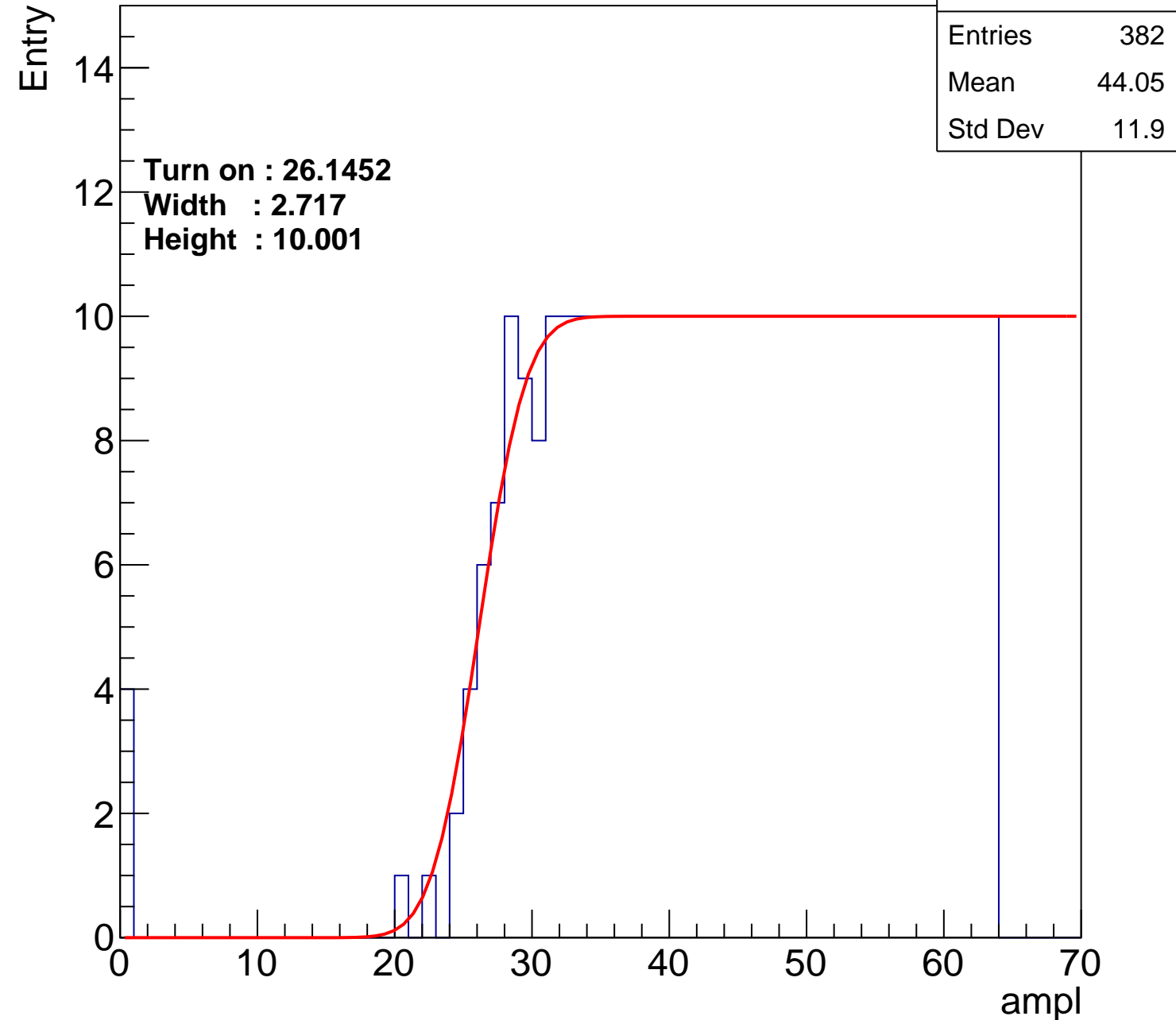
Width : 2.717

Height : 10.001

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U7-ch7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	382
Mean	43.86
Std Dev	12.39

**Turn on : 26.8316**

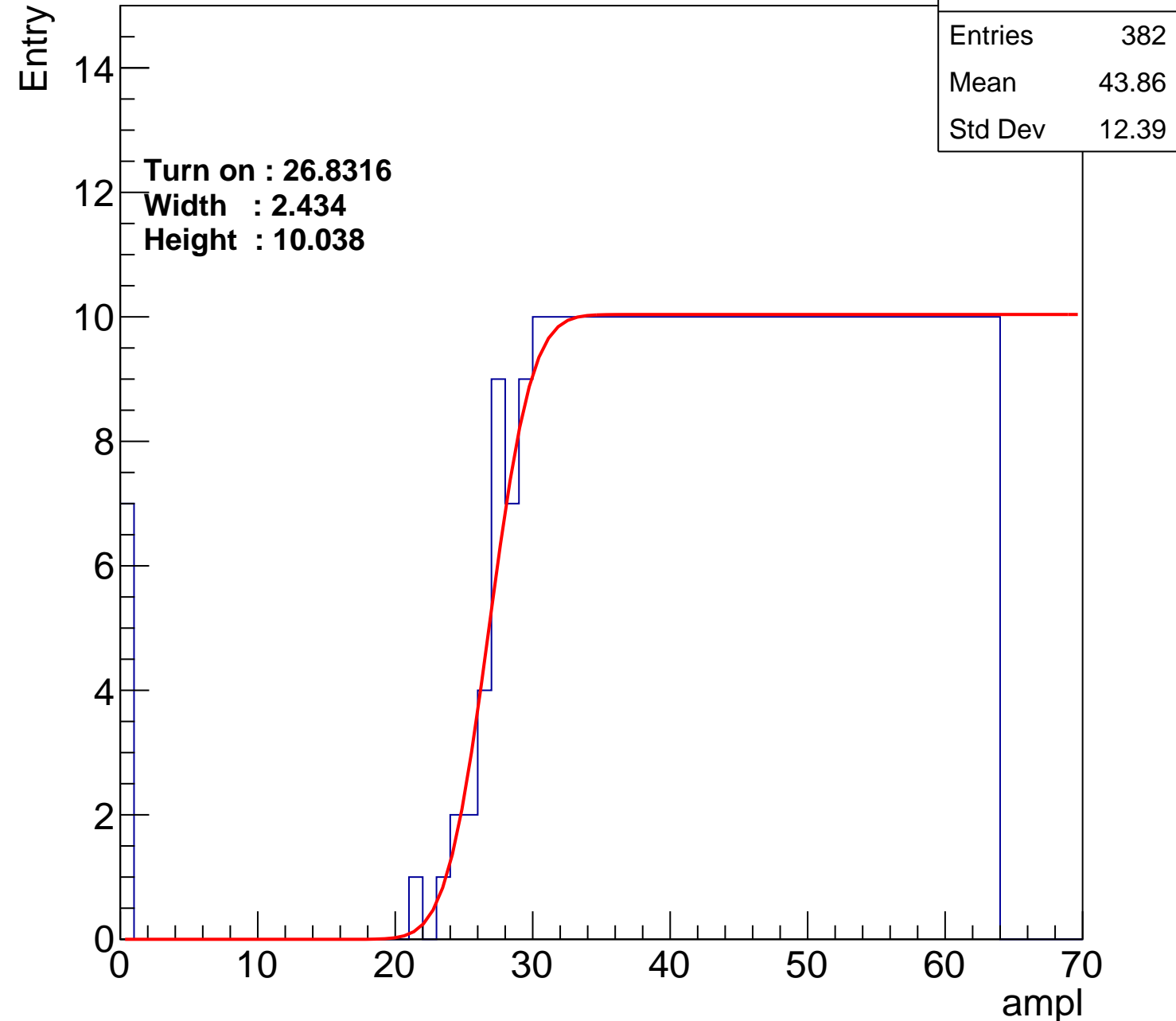
**Width : 2.434**

**Height : 10.038**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch8

calib\_packv5\_042523\_0143.root, FC#0, port D2

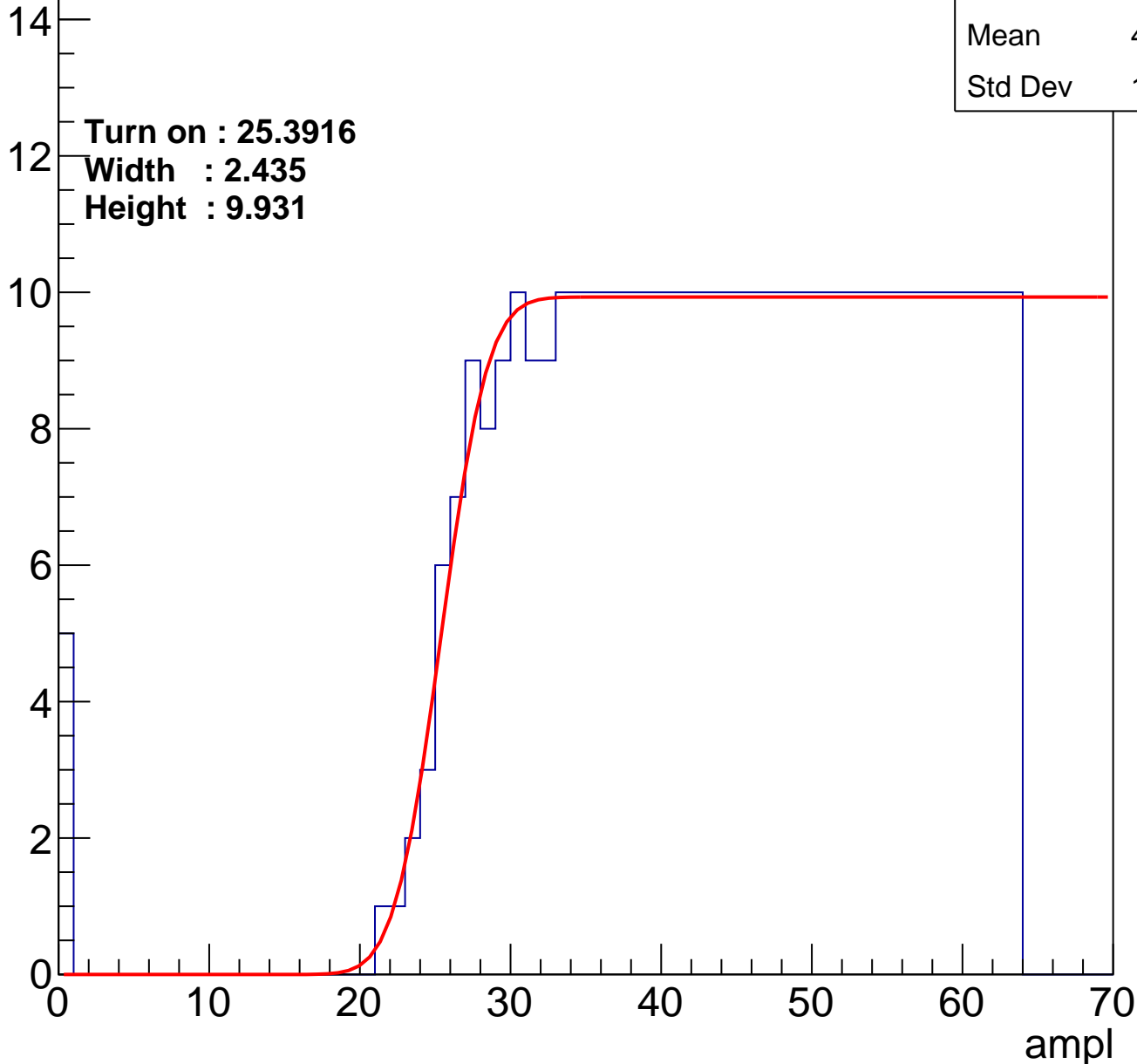
Entries	389
Mean	43.62
Std Dev	12.25

Turn on : 25.3916

Width : 2.435

Height : 9.931

Entry



# B1L101S, U7-ch9

calib\_packv5\_042523\_0143.root, FC#0, port D2

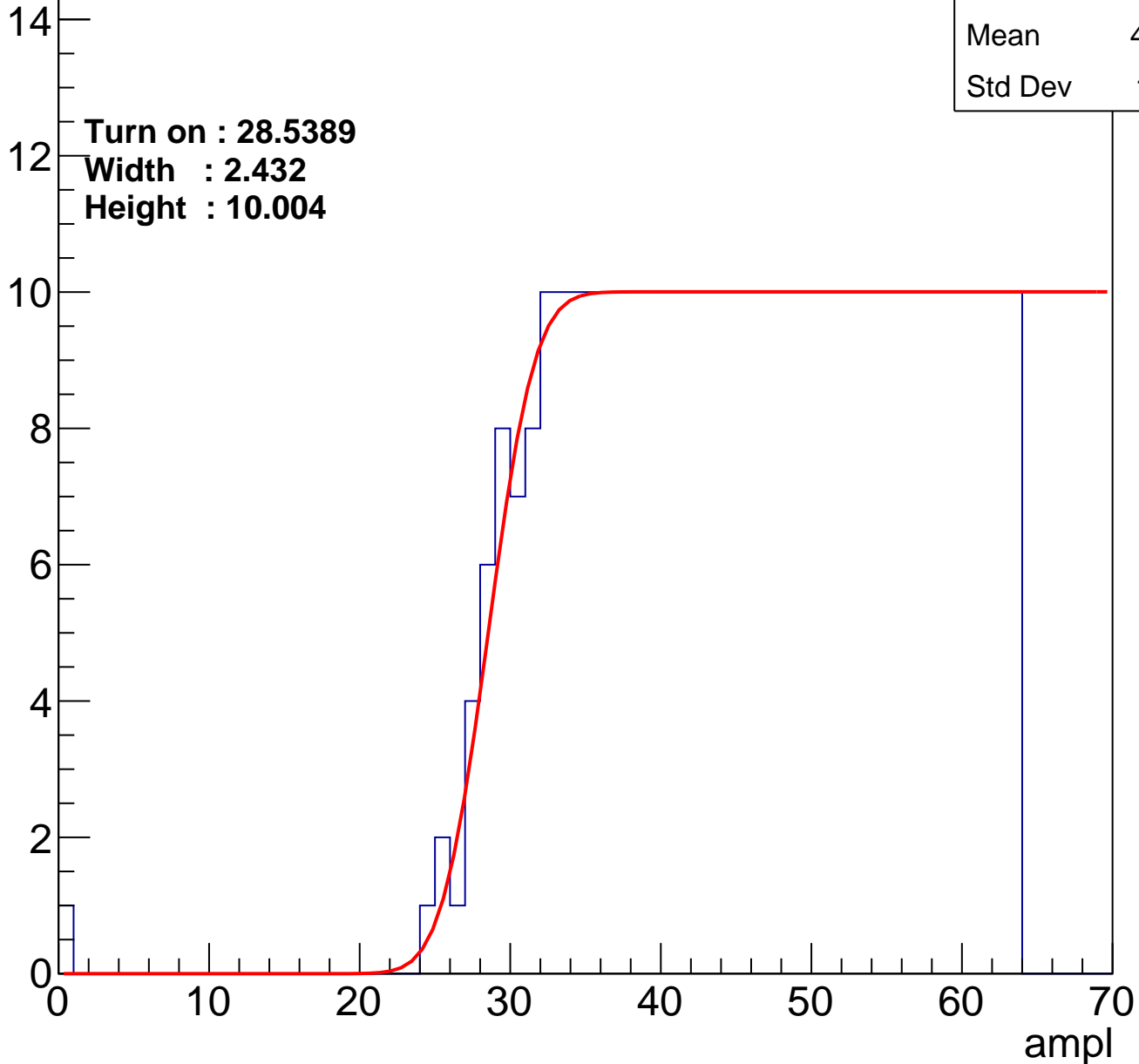
Entries	358
Mean	45.44
Std Dev	10.71

Turn on : 28.5389

Width : 2.432

Height : 10.004

Entry



# B1L101S, U7-ch10

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	378
Mean	43.97
Std Dev	12.5

Turn on : 27.1075

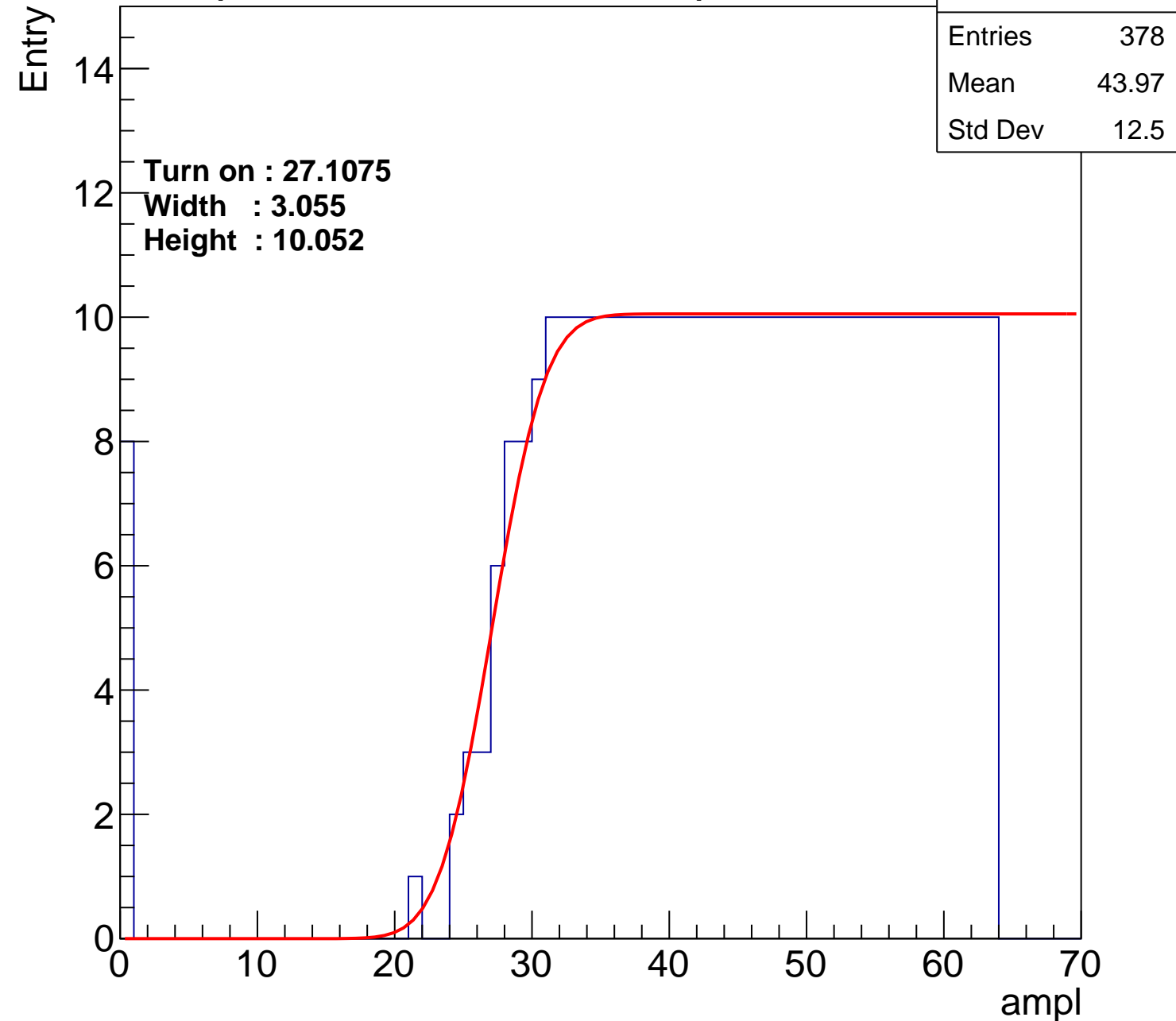
Width : 3.055

Height : 10.052

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch11

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	372
Mean	44.44
Std Dev	11.83

Turn on : 28.2081

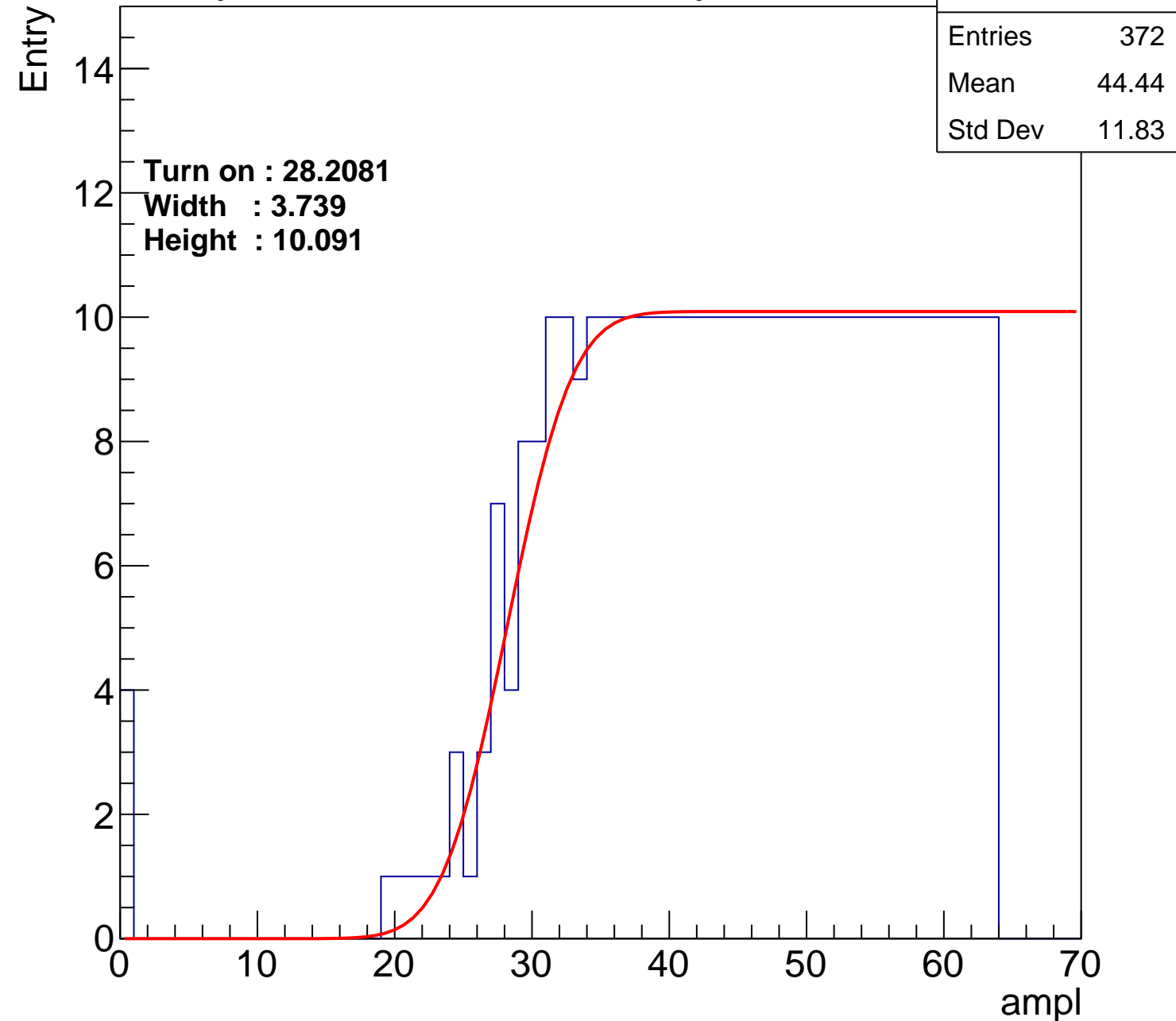
Width : 3.739

Height : 10.091

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch12

calib\_packv5\_042523\_0143.root, FC#0, port D2

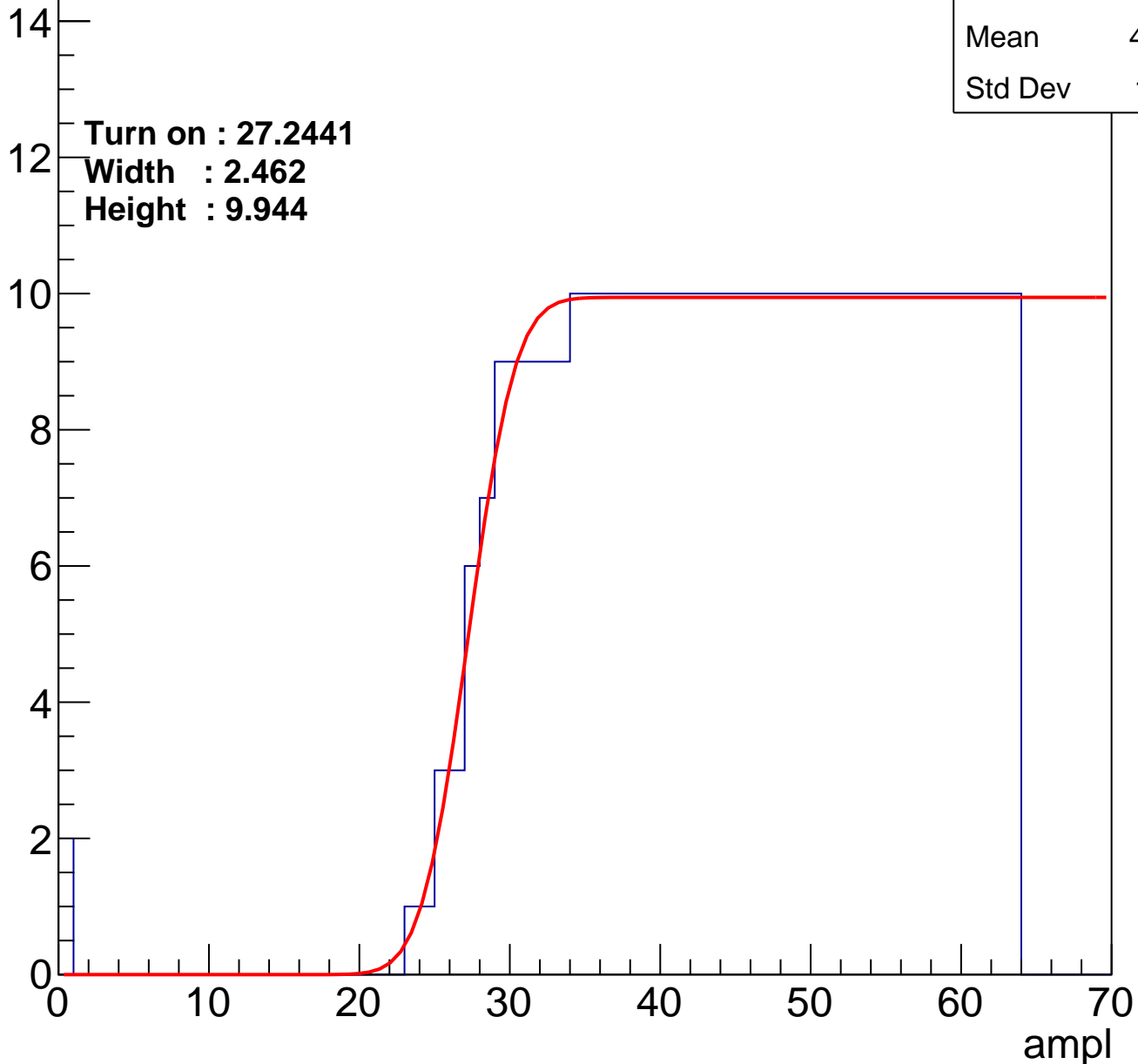
Entries	368
Mean	44.85
Std Dev	11.21

**Turn on : 27.2441**

**Width : 2.462**

**Height : 9.944**

Entry



# B1L101S, U7-ch13

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	374
Mean	44.44
Std Dev	11.7

Turn on : 26.9228

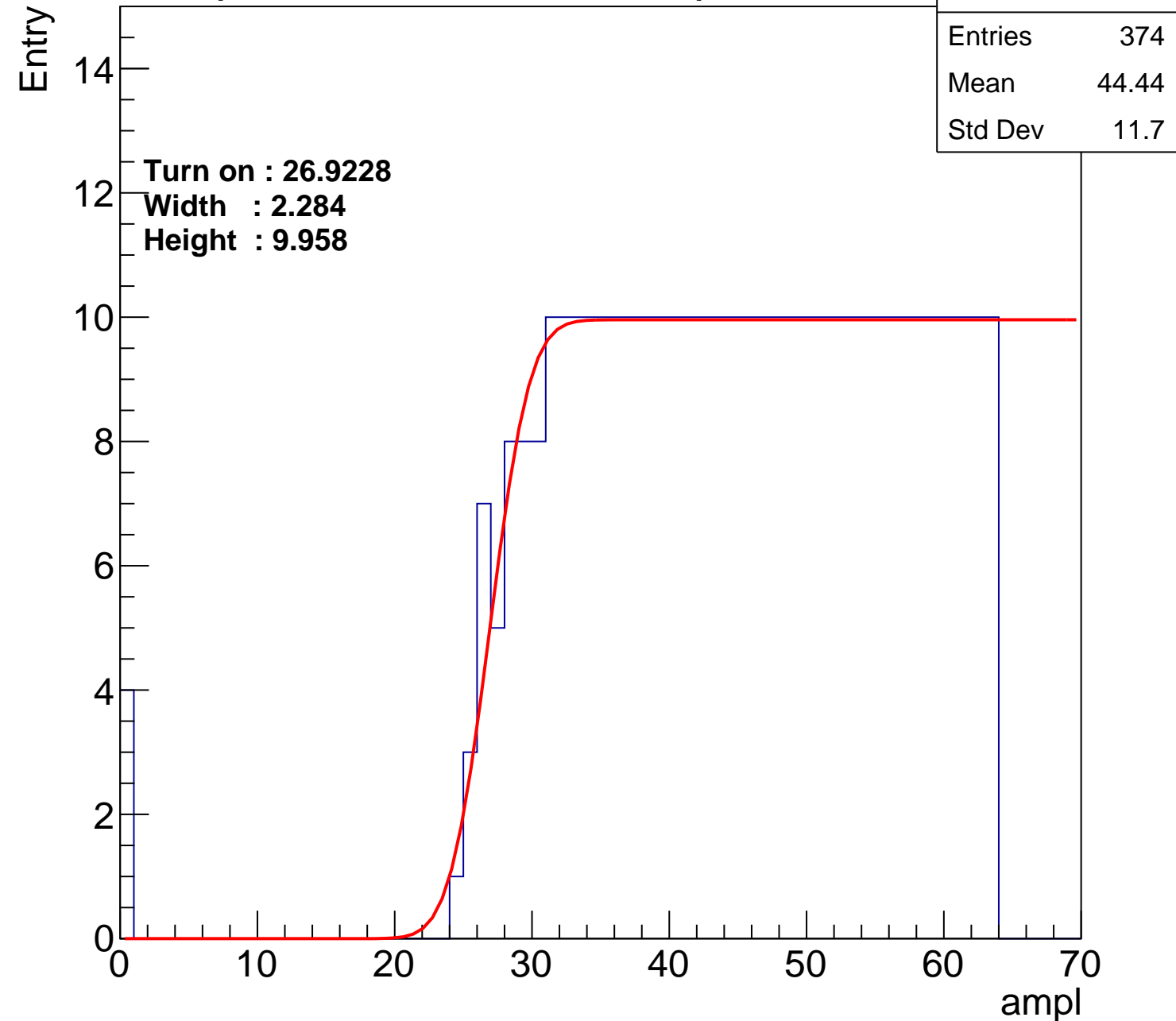
Width : 2.284

Height : 9.958

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch14

calib\_packv5\_042523\_0143.root, FC#0, port D2

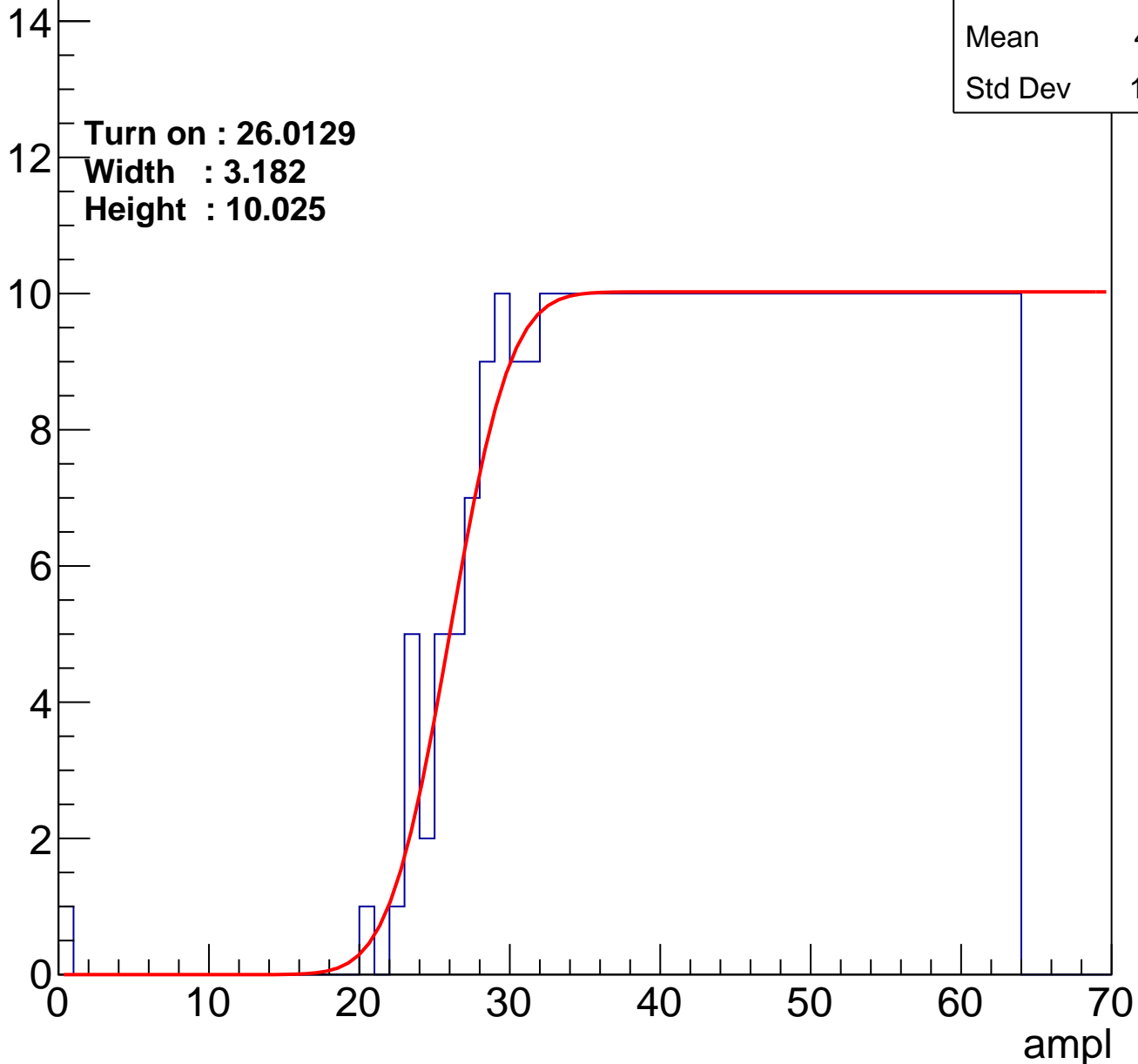
Entries	384
Mean	44.11
Std Dev	11.47

Turn on : 26.0129

Width : 3.182

Height : 10.025

Entry





# B1L101S, U7-ch15

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	374
Mean	44.53
Std Dev	11.49

Turn on : 26.8871

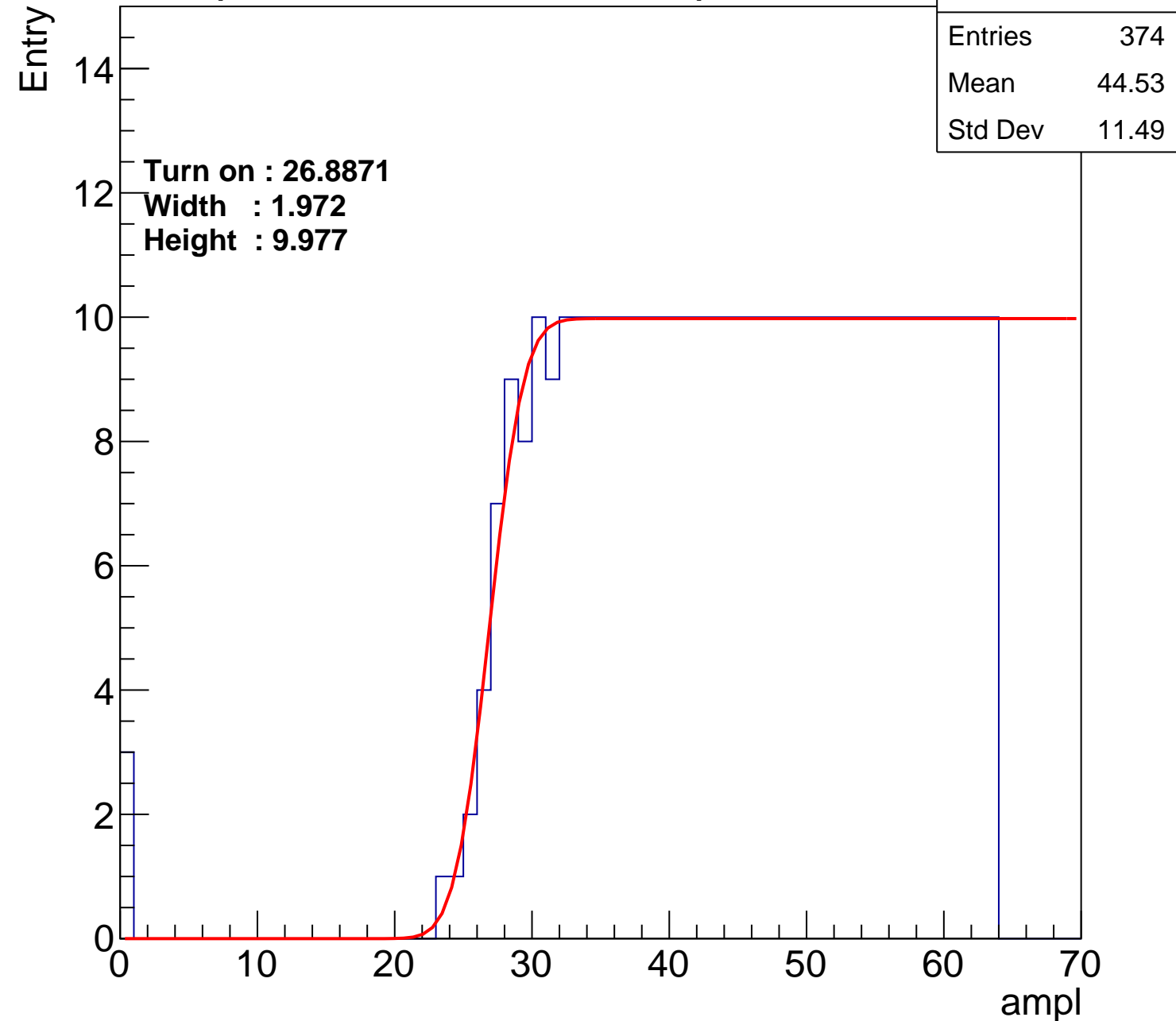
Width : 1.972

Height : 9.977

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch16

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	370
Mean	44.39
Std Dev	12.23

**Turn on : 28.2155**

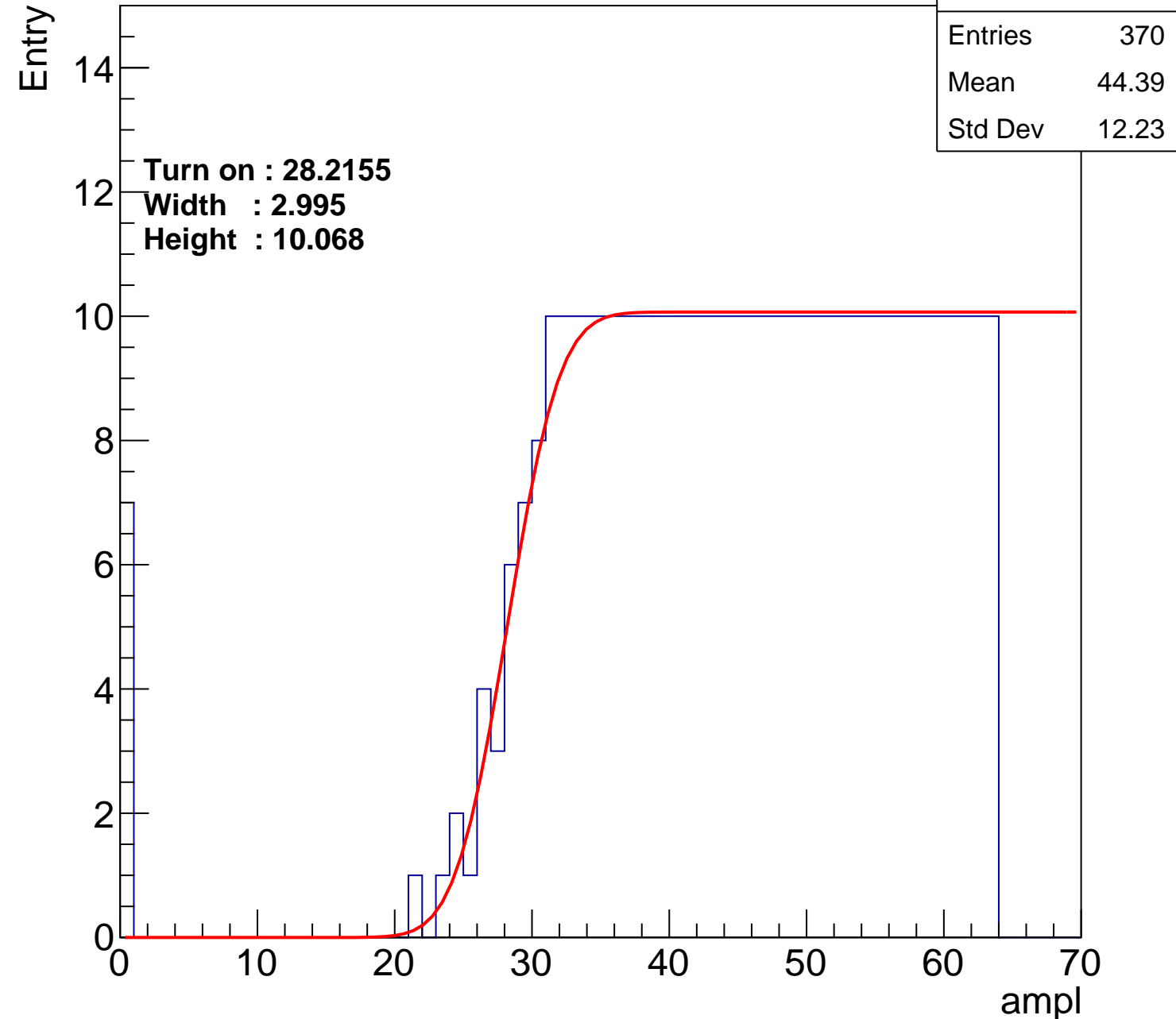
**Width : 2.995**

**Height : 10.068**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch17

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	364
Mean	44.99
Std Dev	11.3

**Turn on : 28.0782**

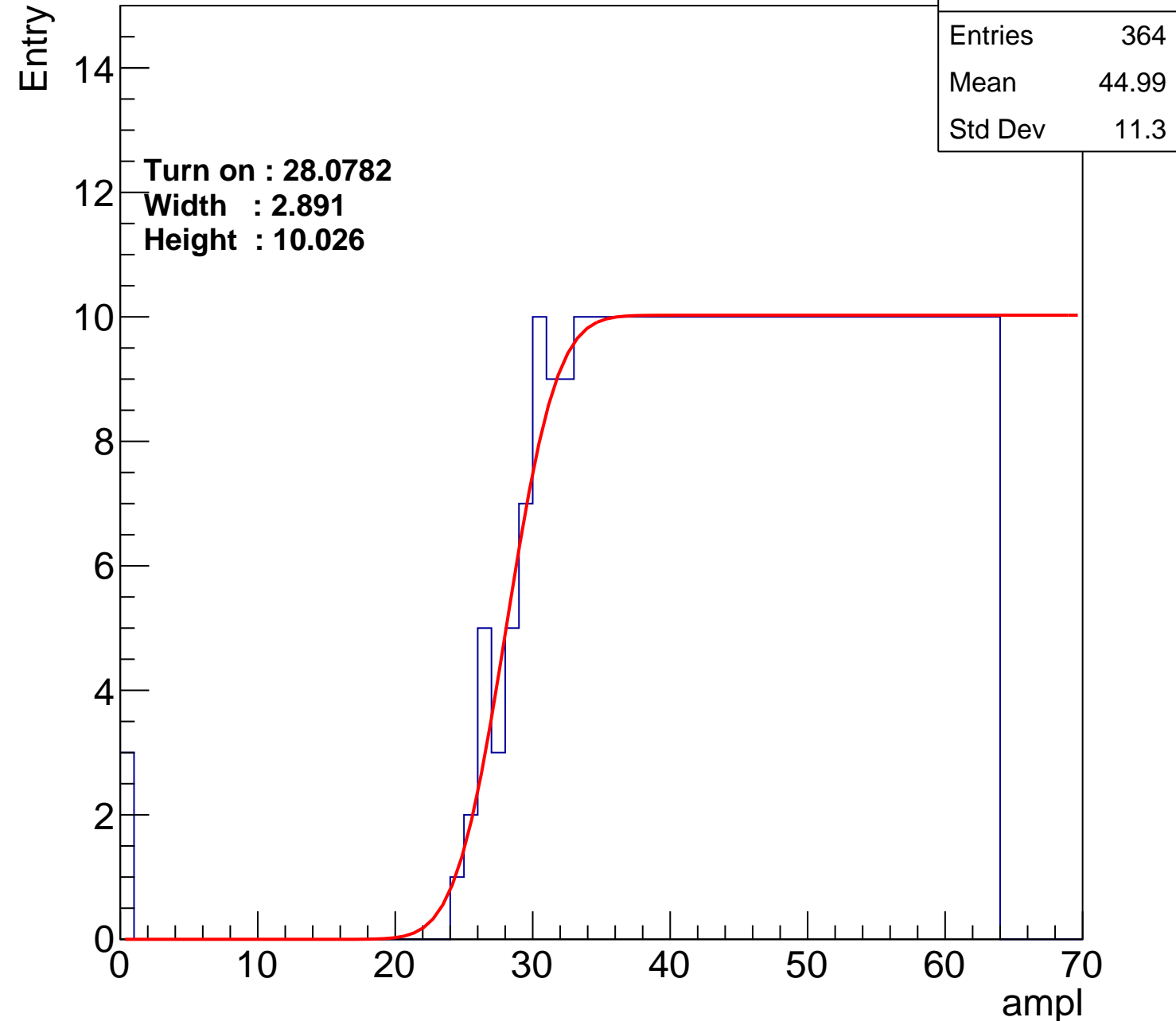
**Width : 2.891**

**Height : 10.026**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch18

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	389
Mean	43.85
Std Dev	11.64

Turn on : 25.6668

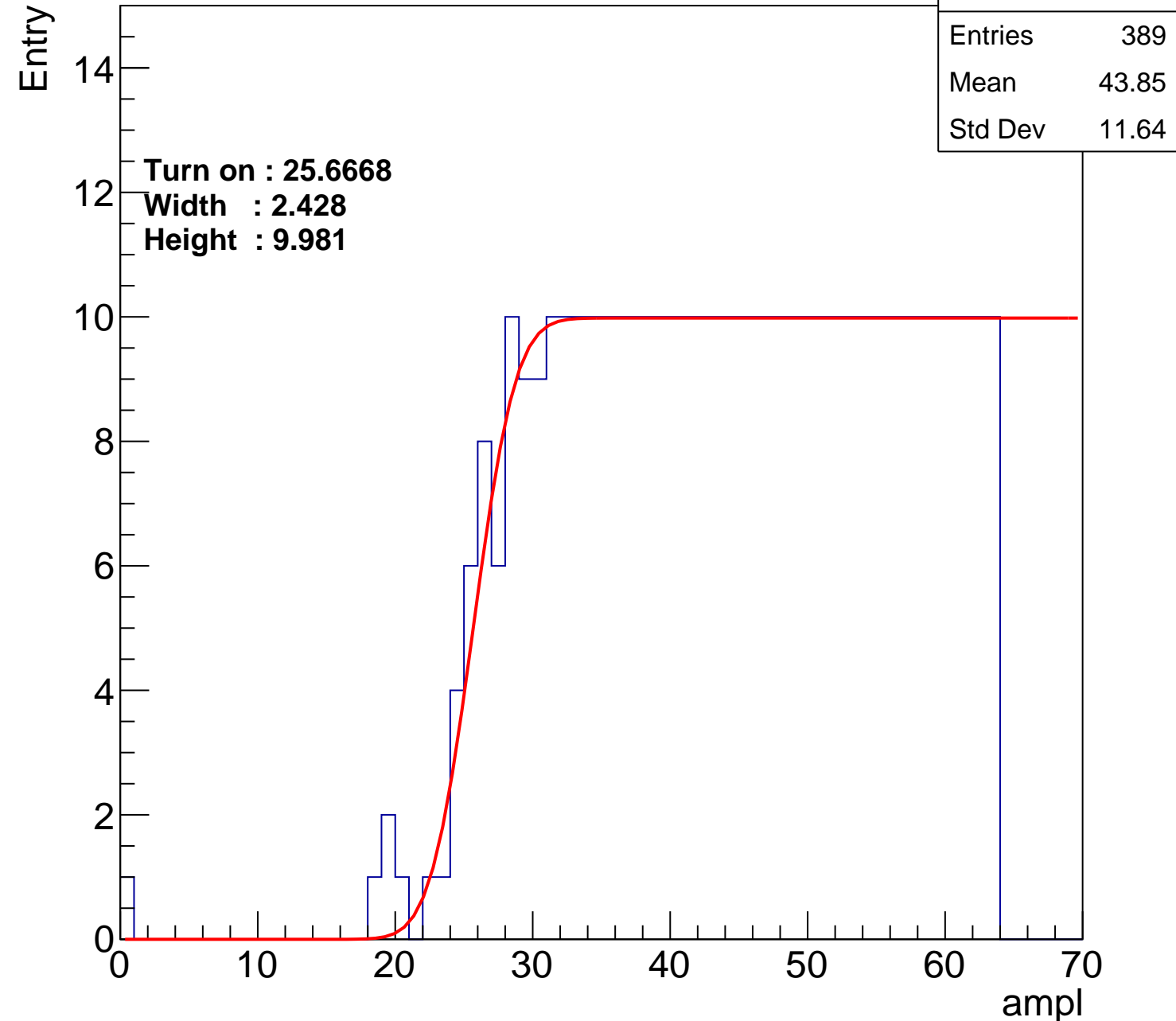
Width : 2.428

Height : 9.981

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch19

calib\_packv5\_042523\_0143.root, FC#0, port D2

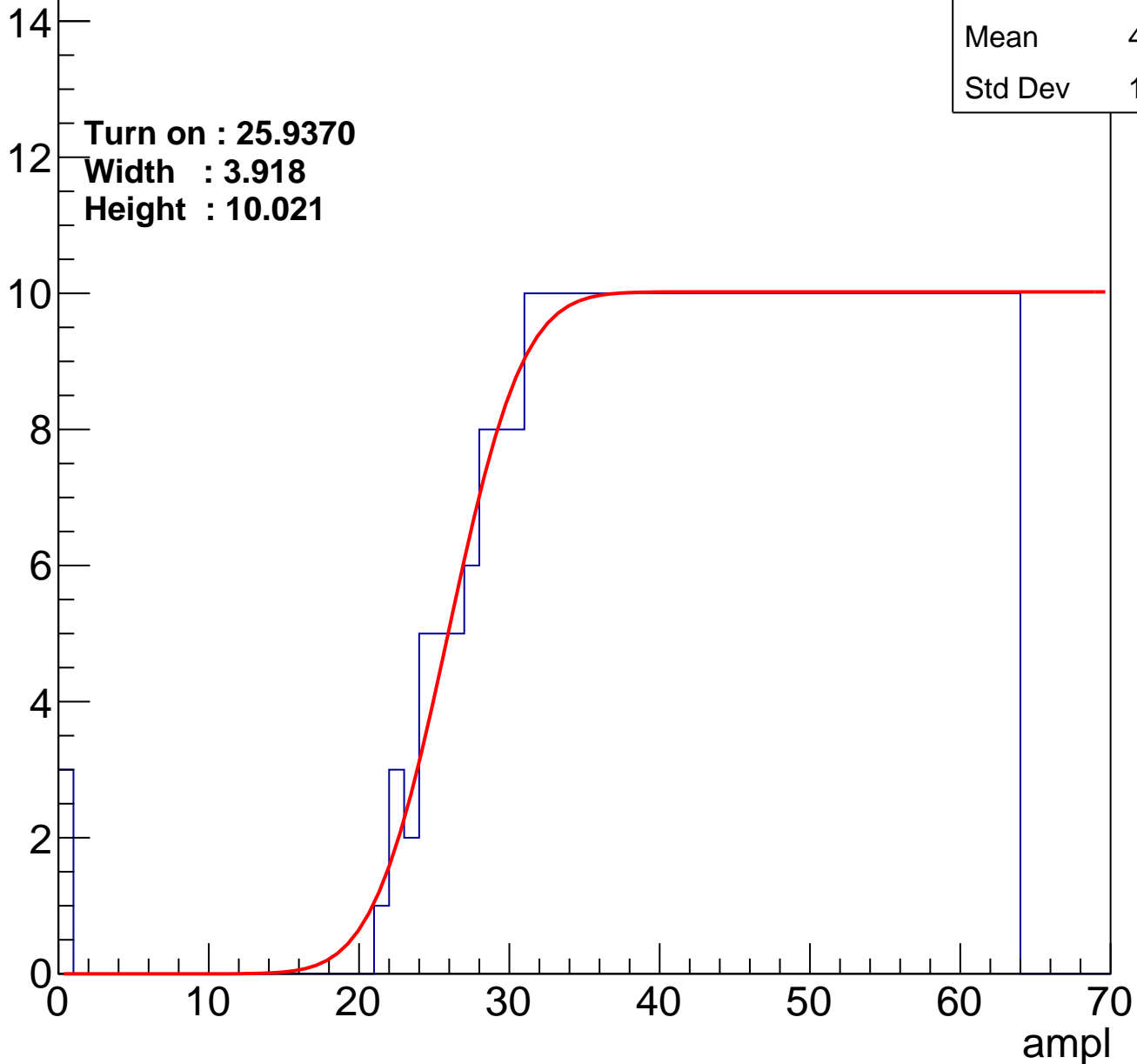
Entries	384
Mean	43.95
Std Dev	11.87

Turn on : 25.9370

Width : 3.918

Height : 10.021

Entry



# B1L101S, U7-ch20

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	406
Mean	42.96
Std Dev	12.27

Turn on : 23.6458

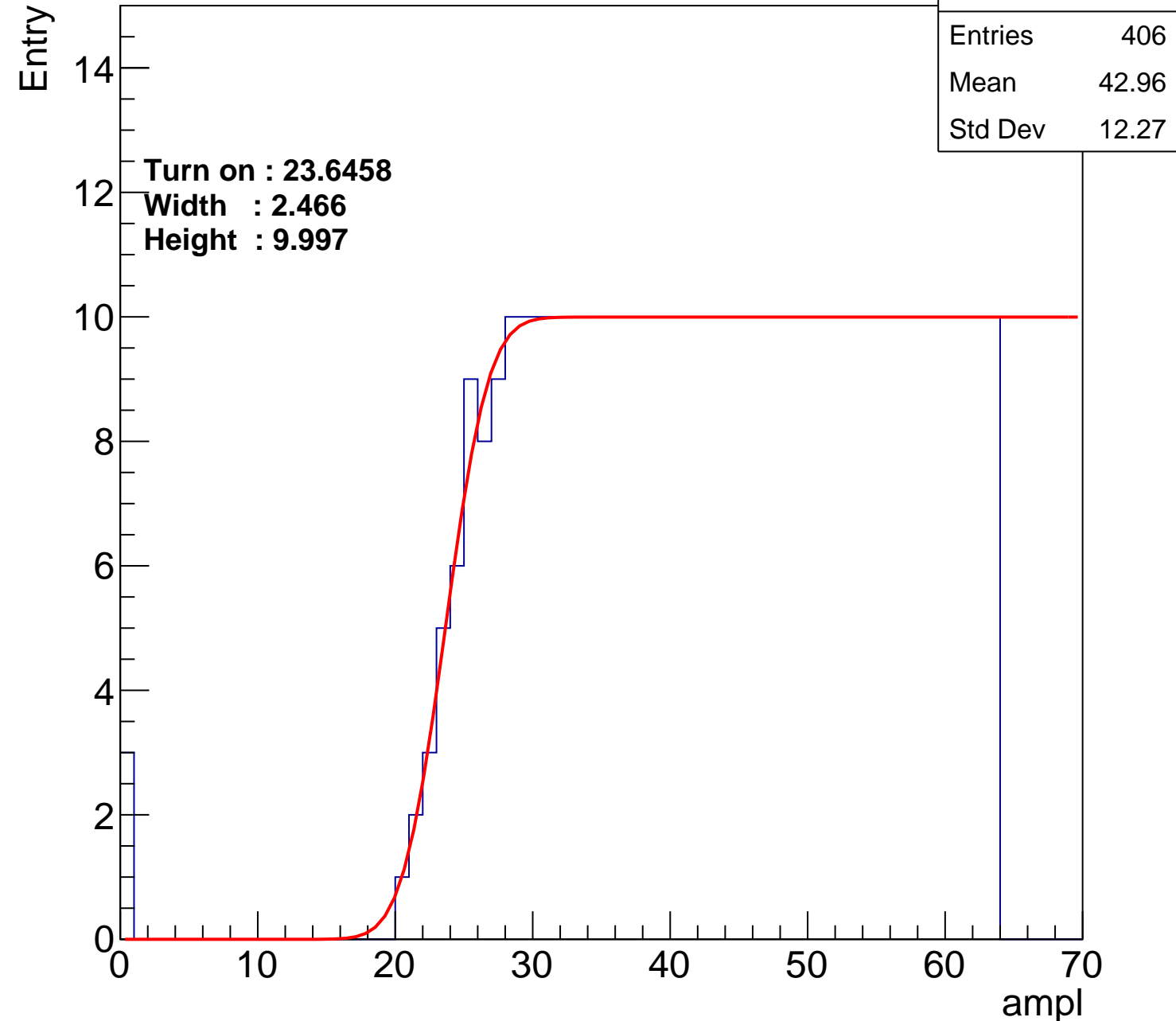
Width : 2.466

Height : 9.997

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch21

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	353
Mean	45.71
Std Dev	10.53

Turn on : 28.6530

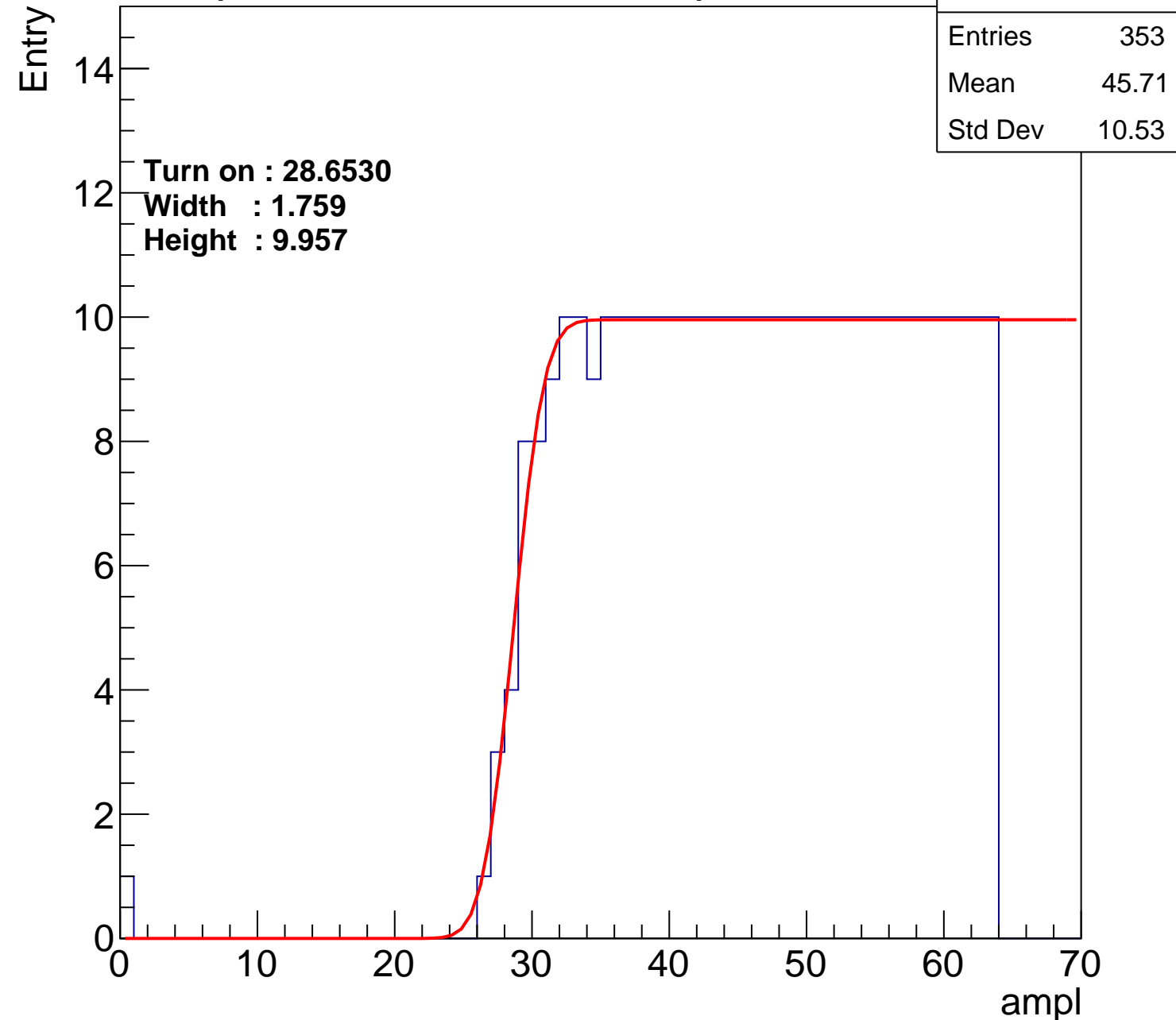
Width : 1.759

Height : 9.957

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch22

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	387
Mean	43.71
Std Dev	12.22

Turn on : 26.0061

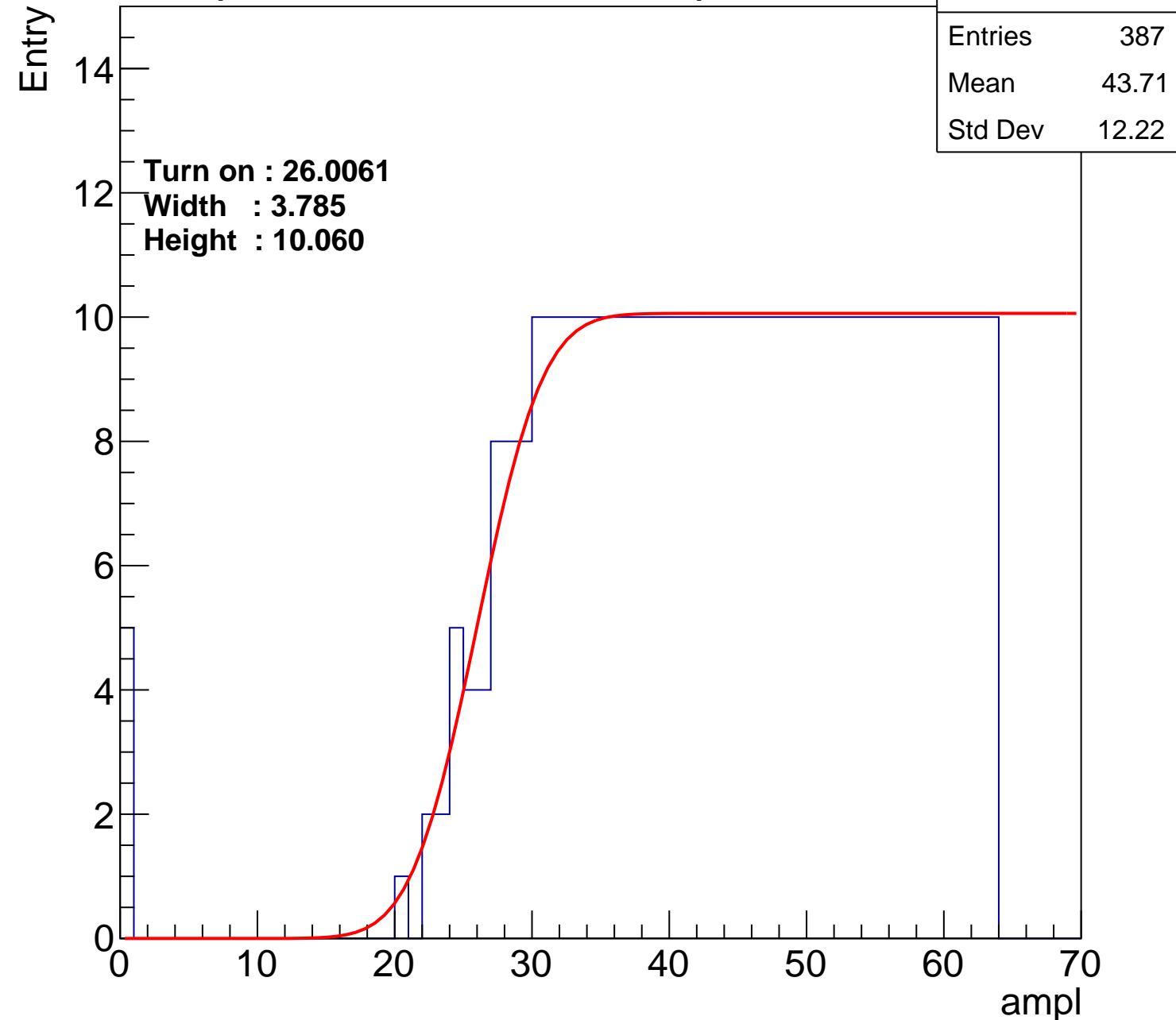
Width : 3.785

Height : 10.060

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U7-ch23

**calib\_packv5\_042523\_0143.root, FC#0, port D2**

Entries	364
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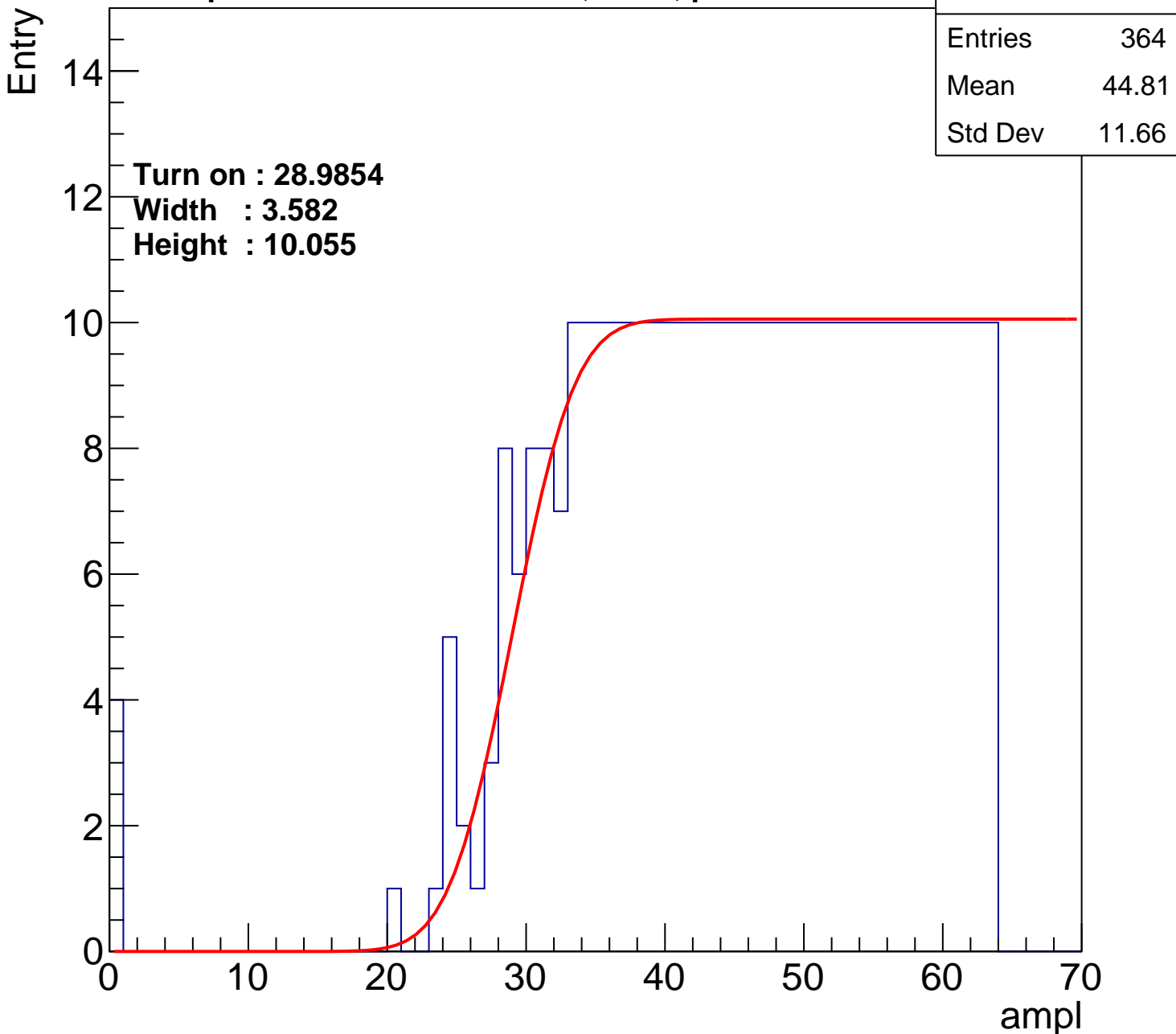
Mean	44.81
------	-------

Std Dev	11.66
---------	-------

**Turn on : 28.9854**

**Width : 3.582**

**Height : 10.055**



# B1L101S, U7-ch24

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	399
Mean	43.32
Std Dev	12.09

Turn on : 24.7484

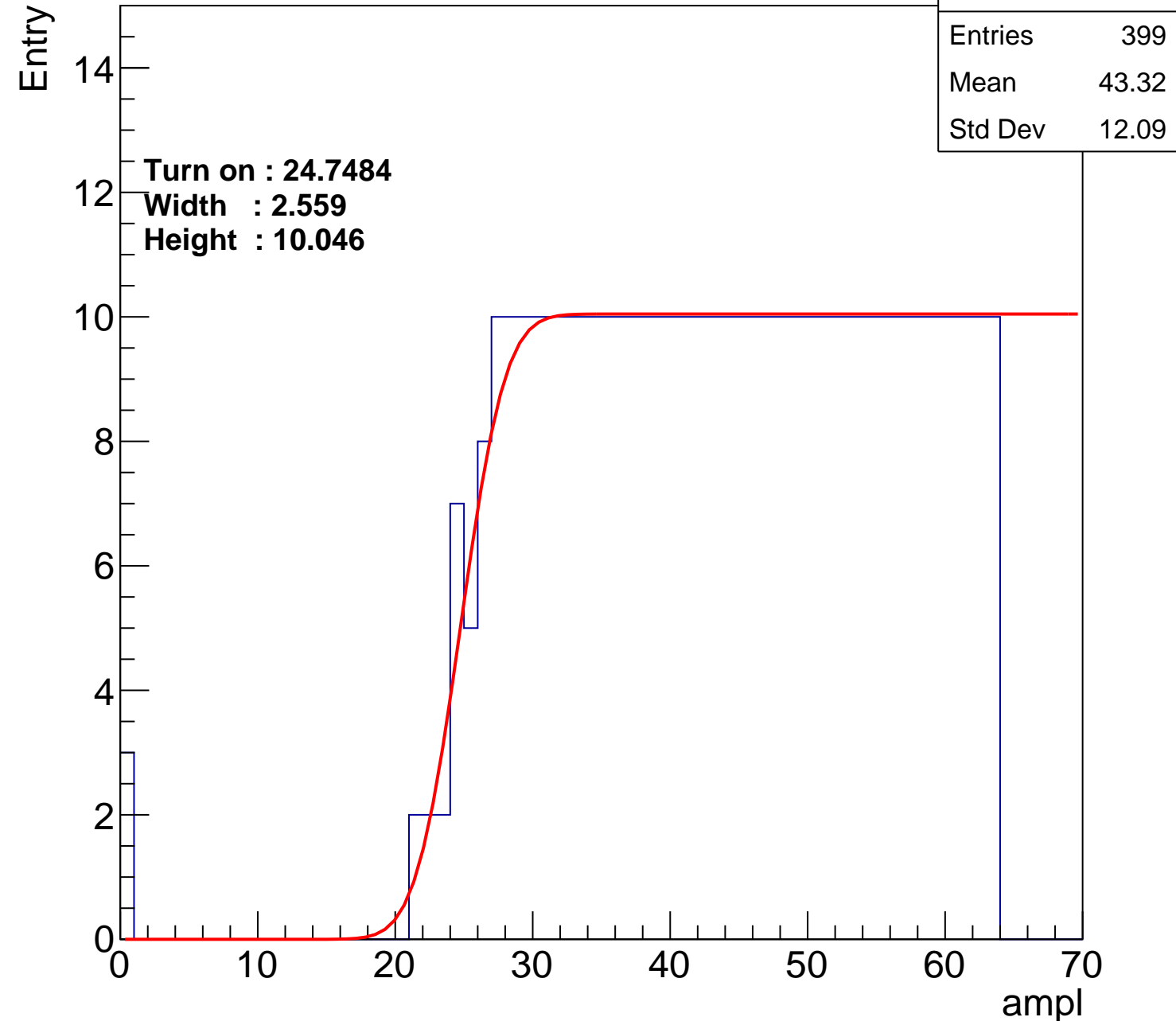
Width : 2.559

Height : 10.046

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch25

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	378
Mean	44.17
Std Dev	11.99

Turn on : 25.7005

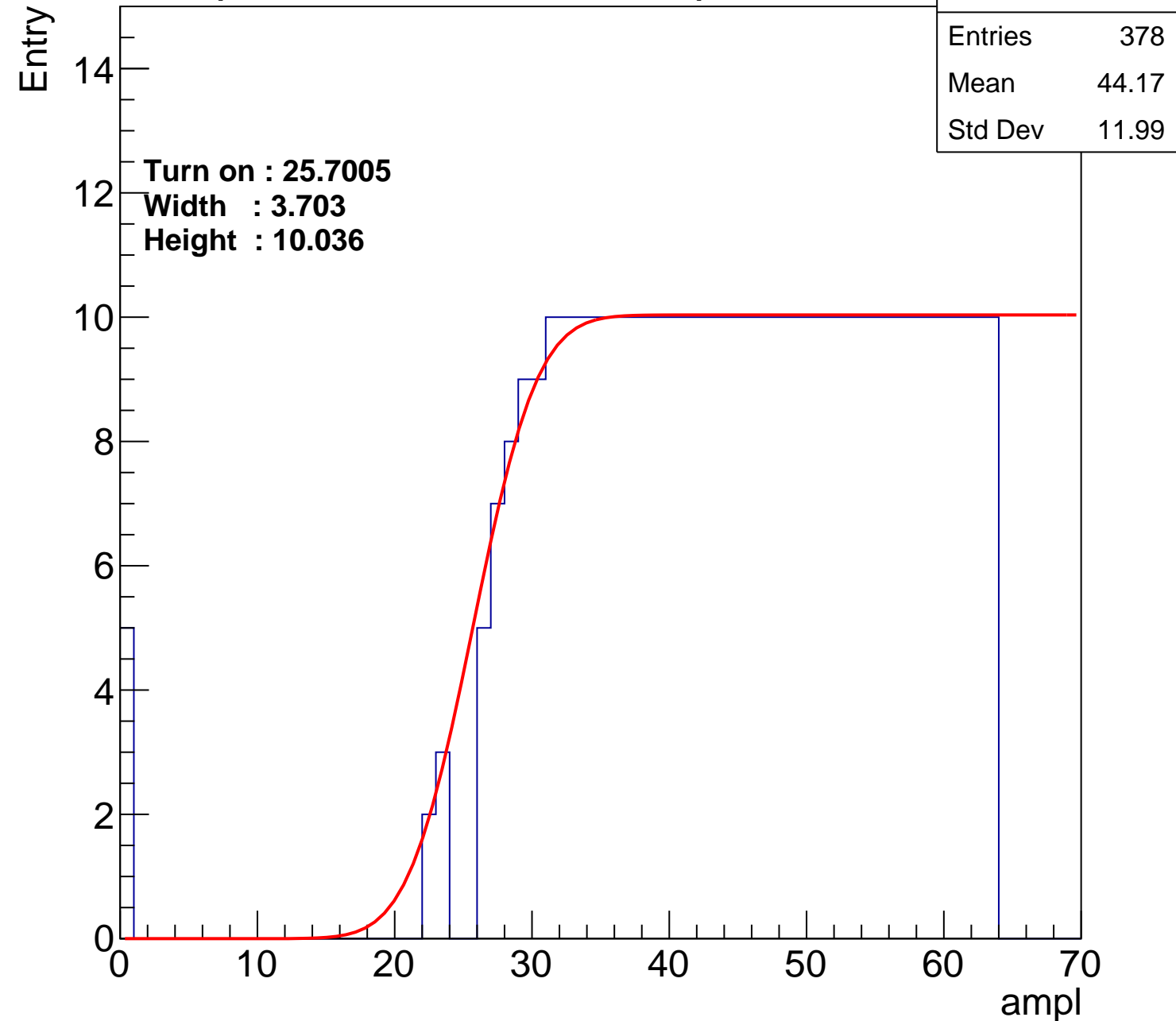
Width : 3.703

Height : 10.036

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch26

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	366
Mean	44.81
Std Dev	11.55

Turn on : 27.8085

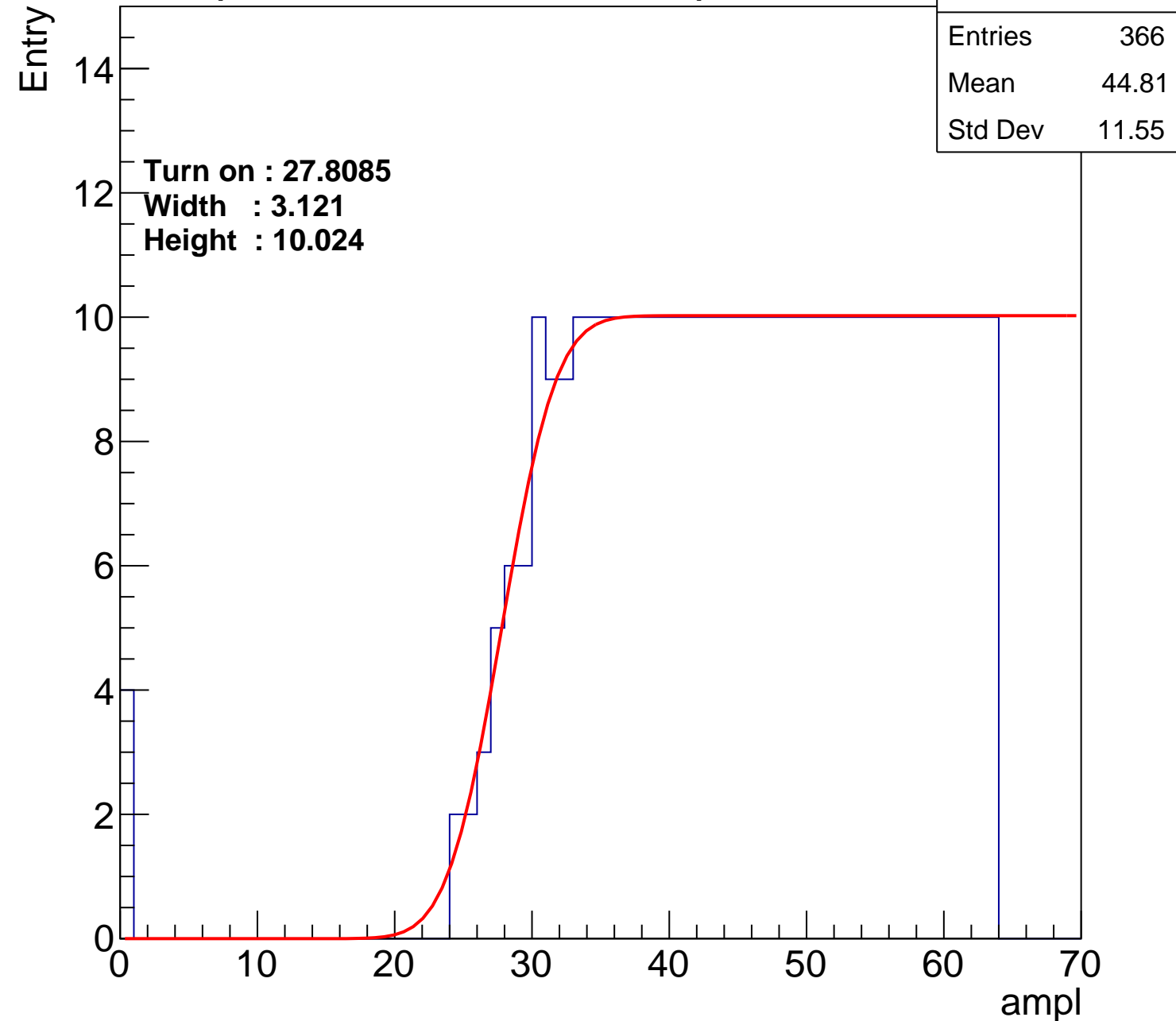
Width : 3.121

Height : 10.024

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch27

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	359
Mean	45.22
Std Dev	11.2

**Turn on : 28.2781**

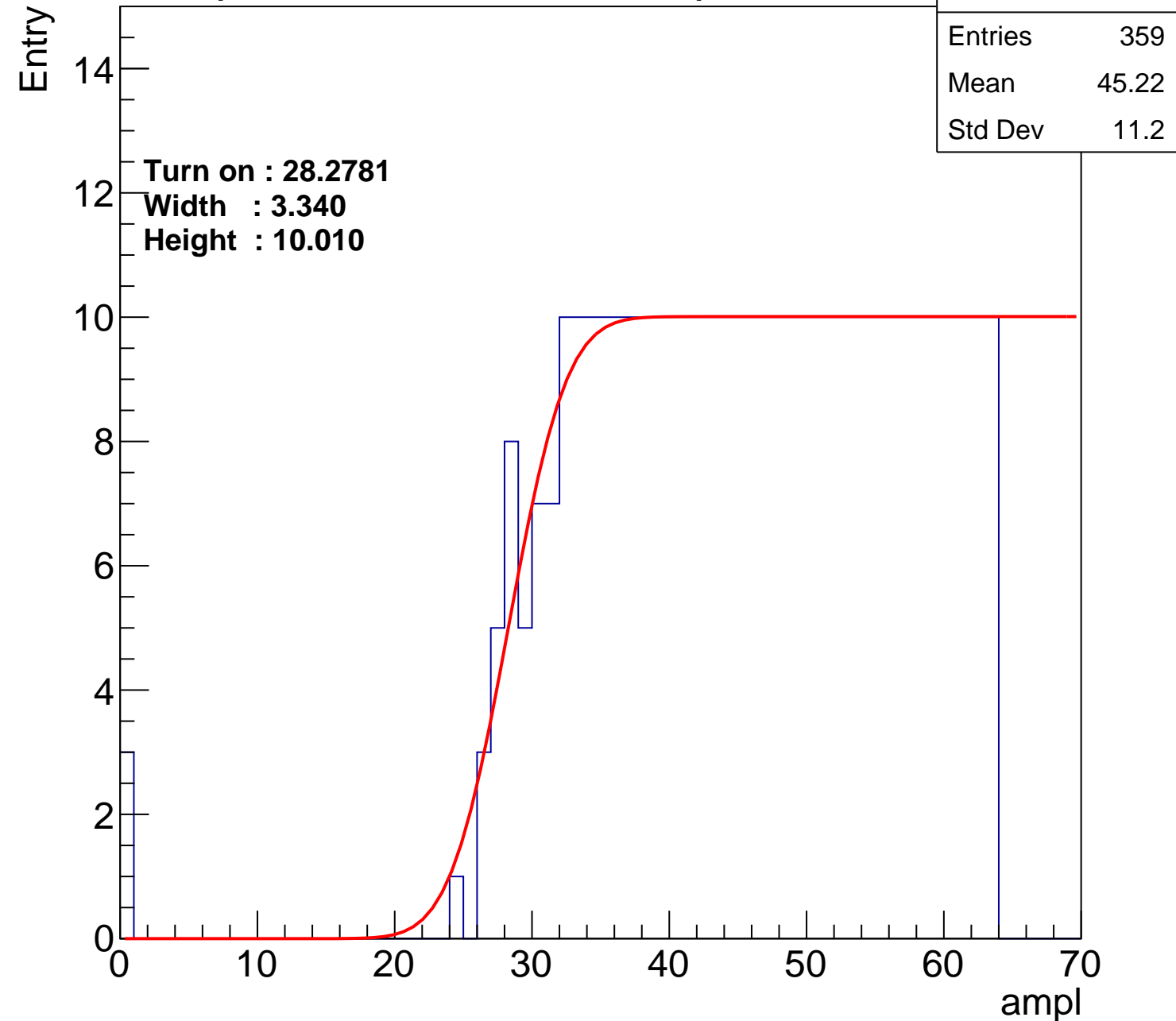
**Width : 3.340**

**Height : 10.010**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch28

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	365
Mean	44.88
Std Dev	11.5

Turn on : 27.9964

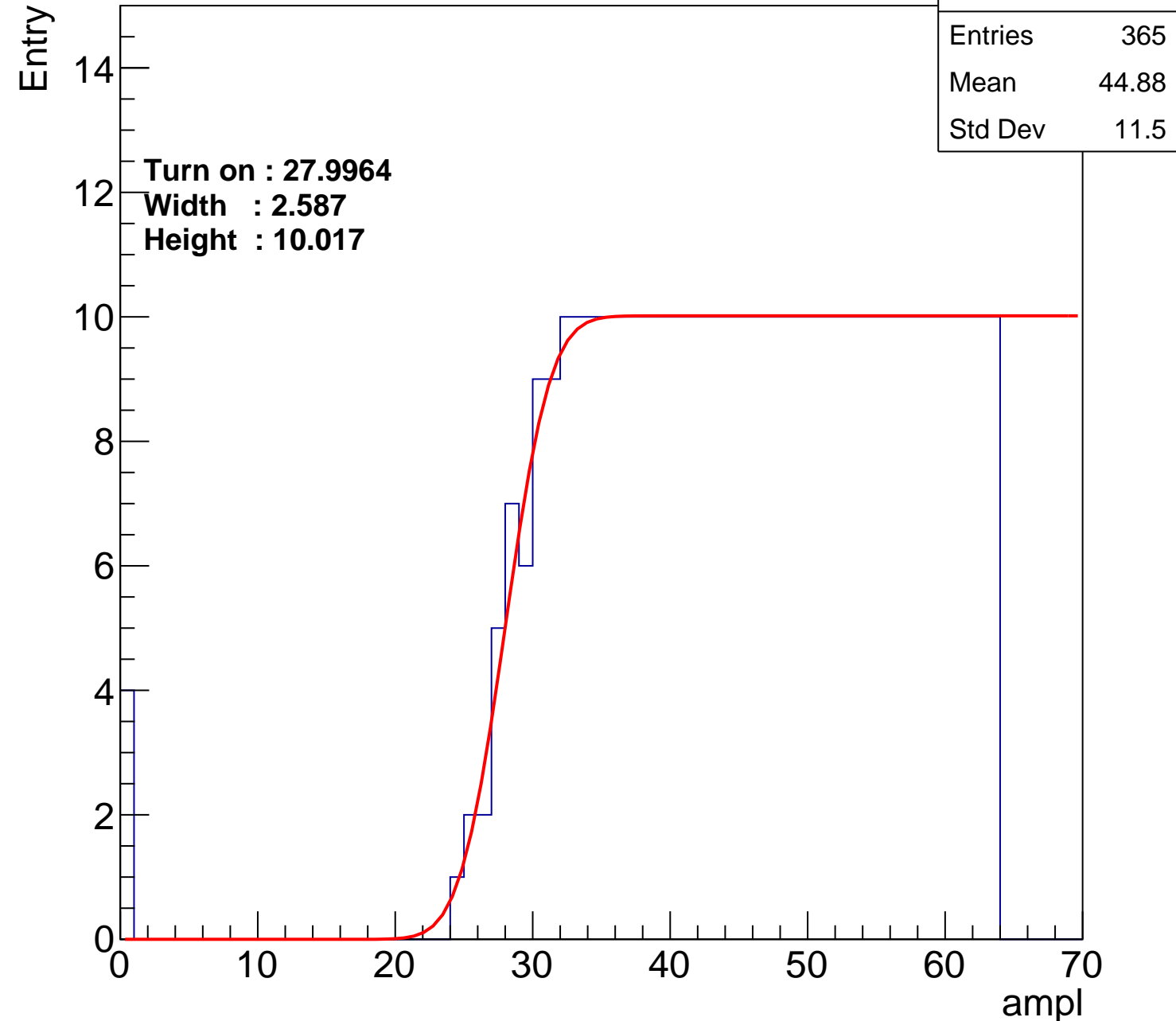
Width : 2.587

Height : 10.017

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch29

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	370
Mean	44.7
Std Dev	11.44

Turn on : 27.6088

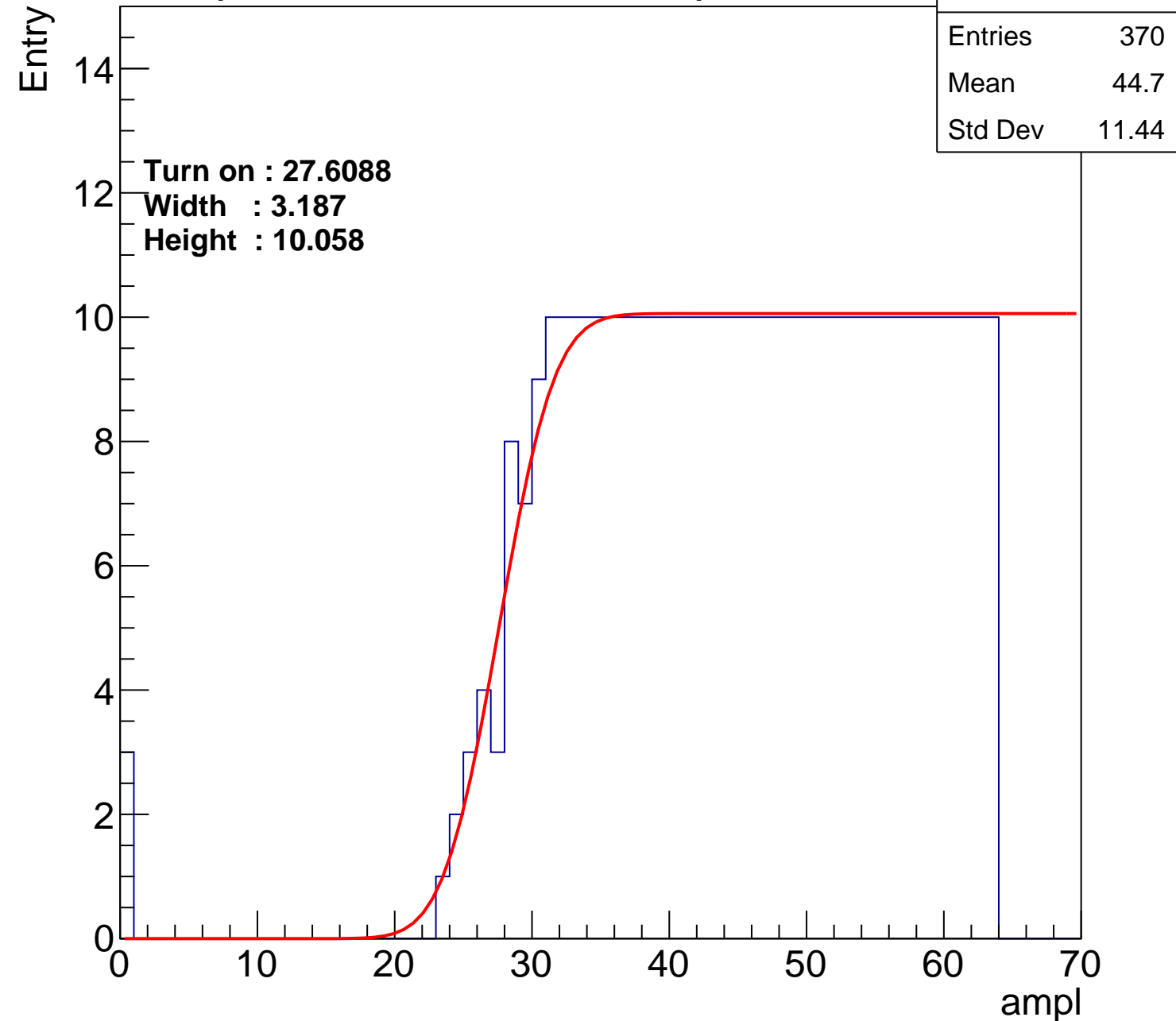
Width : 3.187

Height : 10.058

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch30

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	368
Mean	44.81
Std Dev	11.28

Turn on : 27.8268

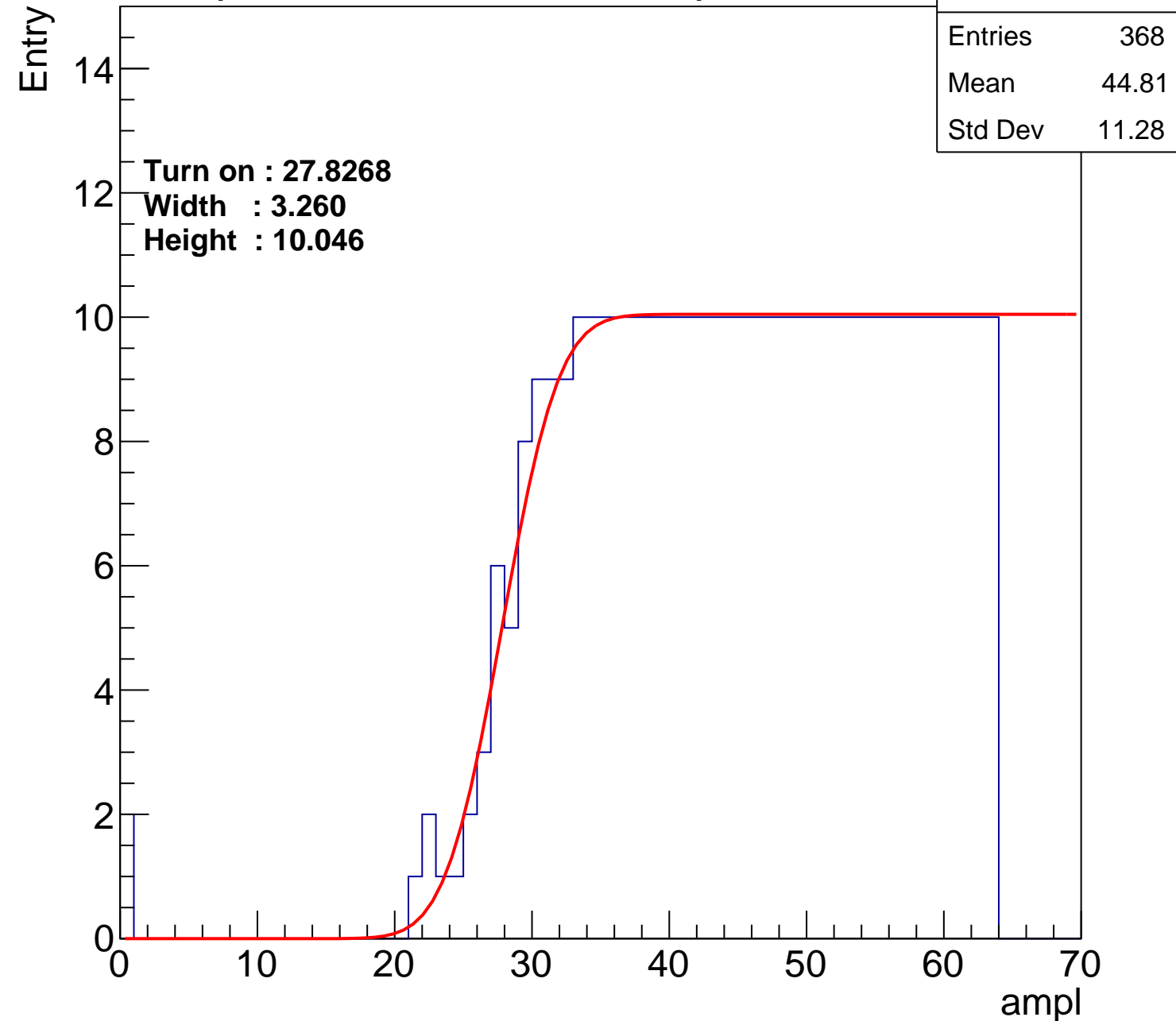
Width : 3.260

Height : 10.046

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U7-ch31

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	369
Mean	44.83
Std Dev	11.2

Turn on : 27.5624

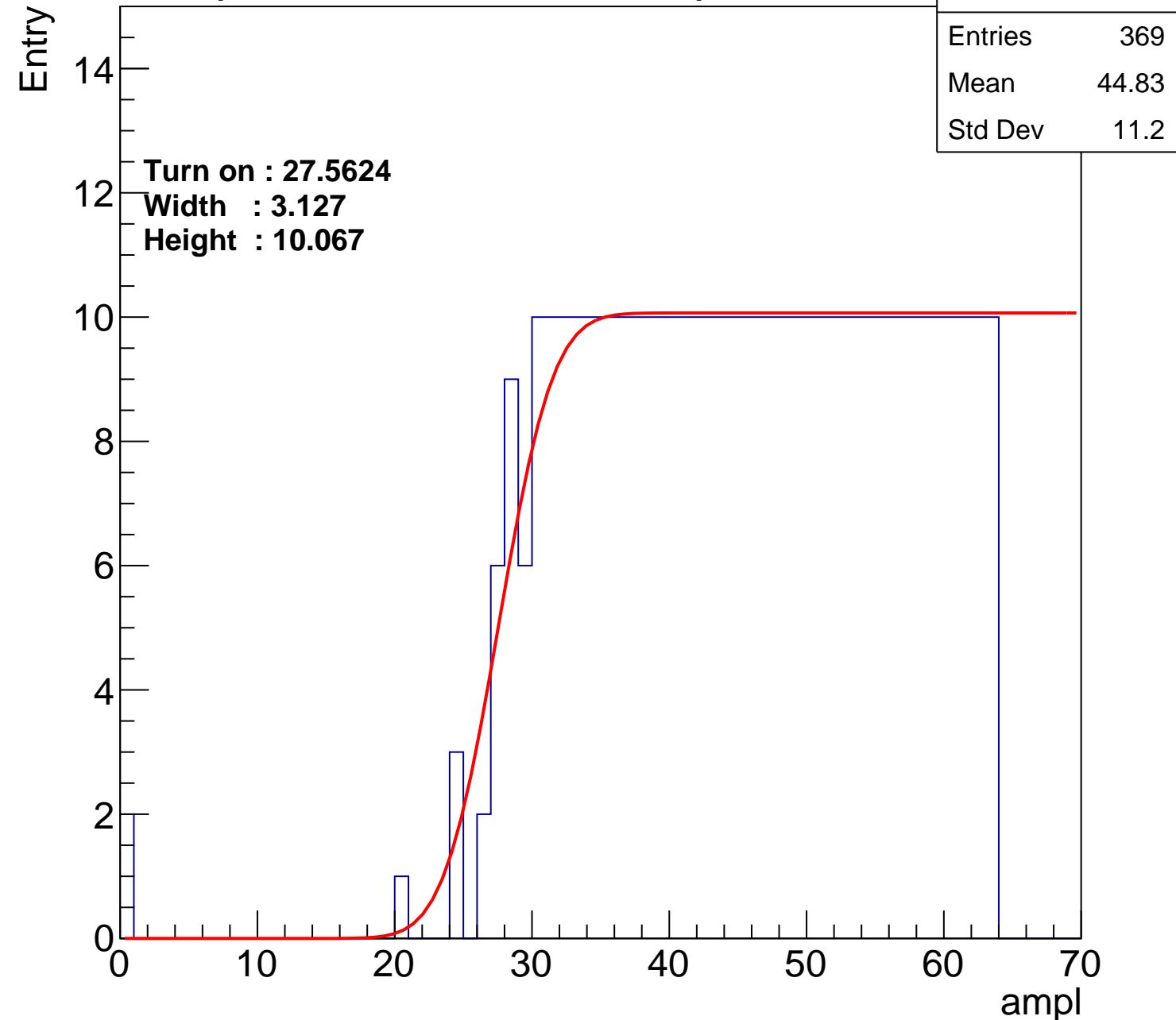
Width : 3.127

Height : 10.067

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch32

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	355
Mean	45.37
Std Dev	11.17

**Turn on : 28.1748**

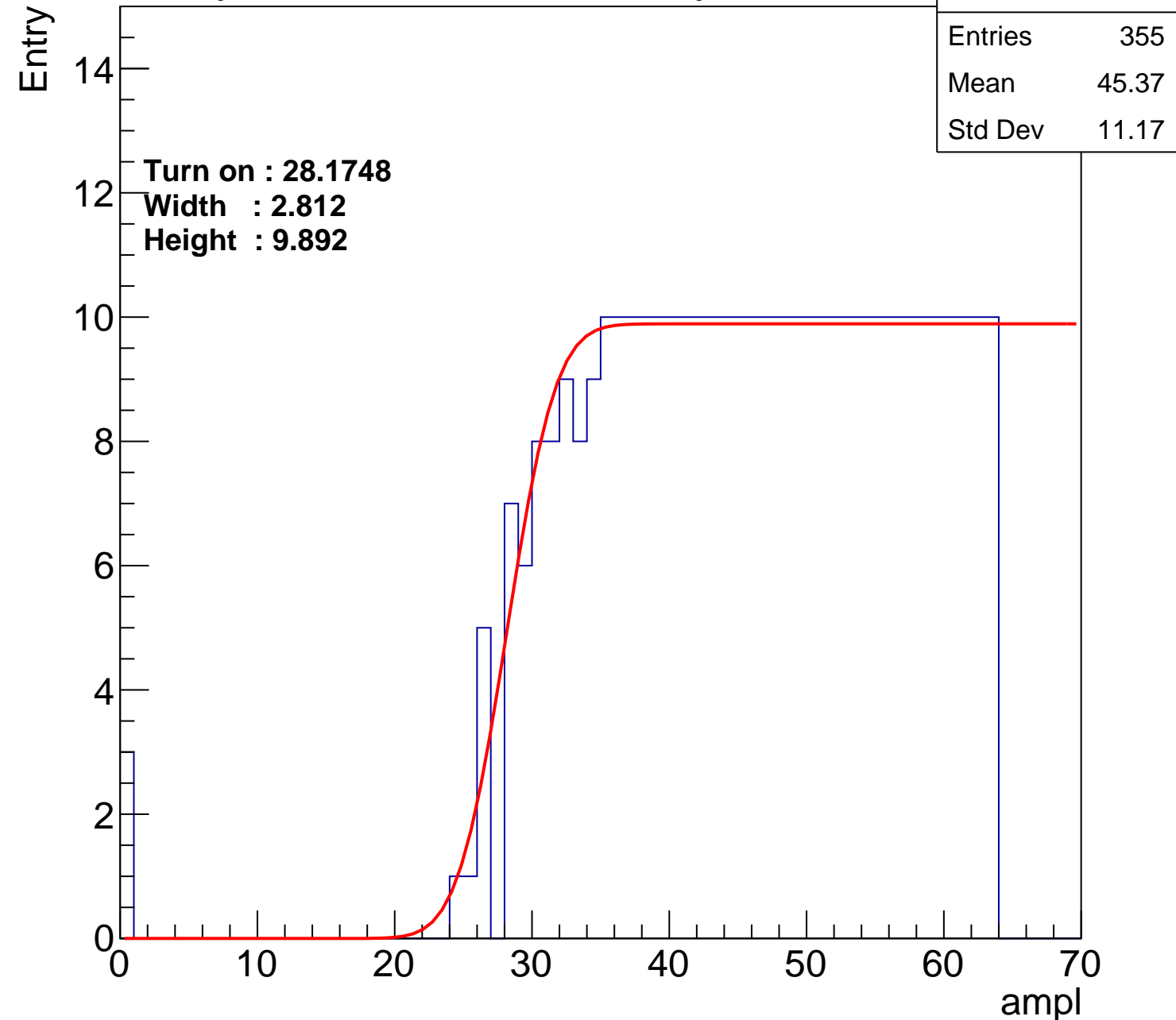
**Width : 2.812**

**Height : 9.892**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch33

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	380
Mean	44.26
Std Dev	11.51

Turn on : 25.8332

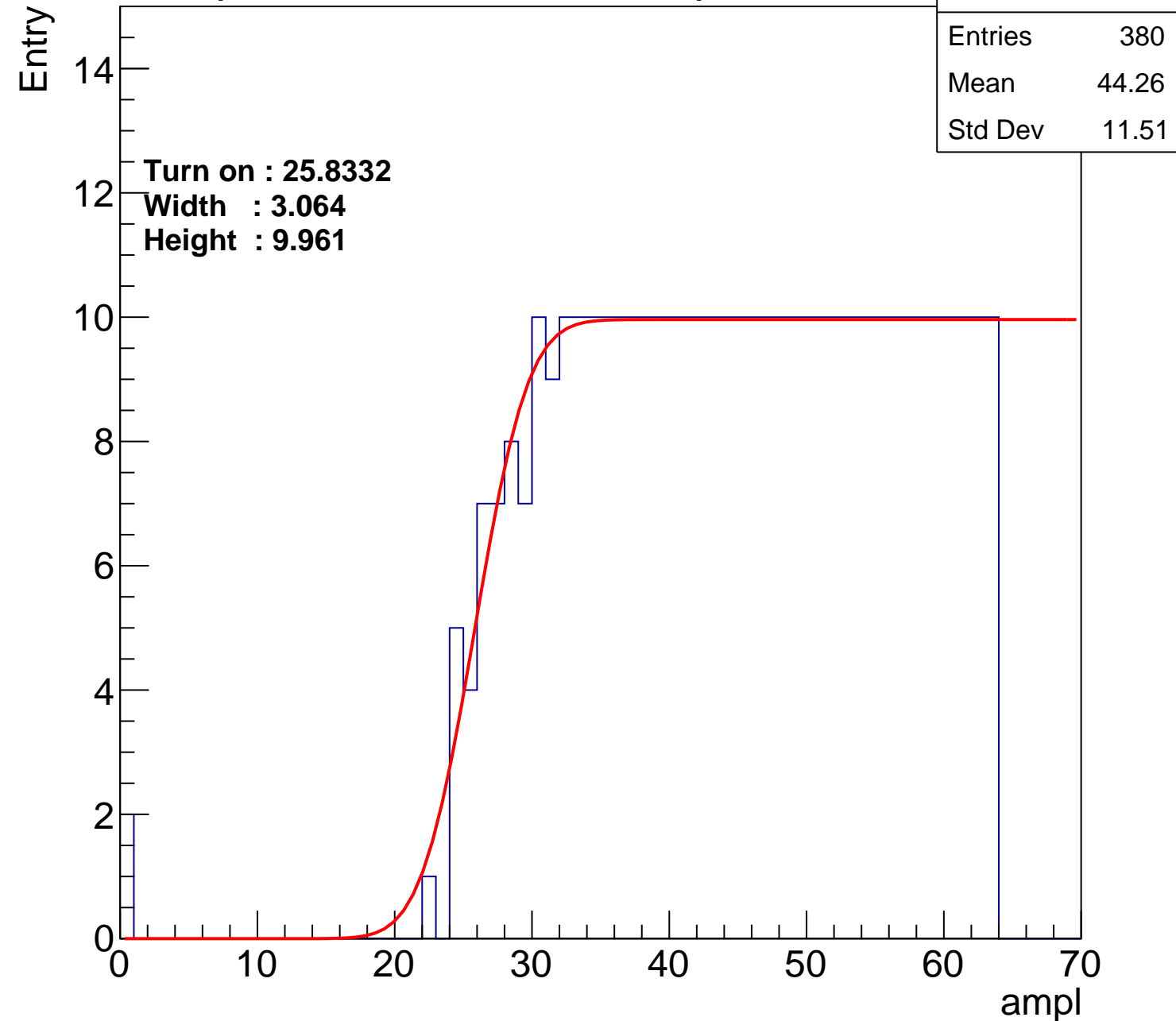
Width : 3.064

Height : 9.961

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch34

calib\_packv5\_042523\_0143.root, FC#0, port D2

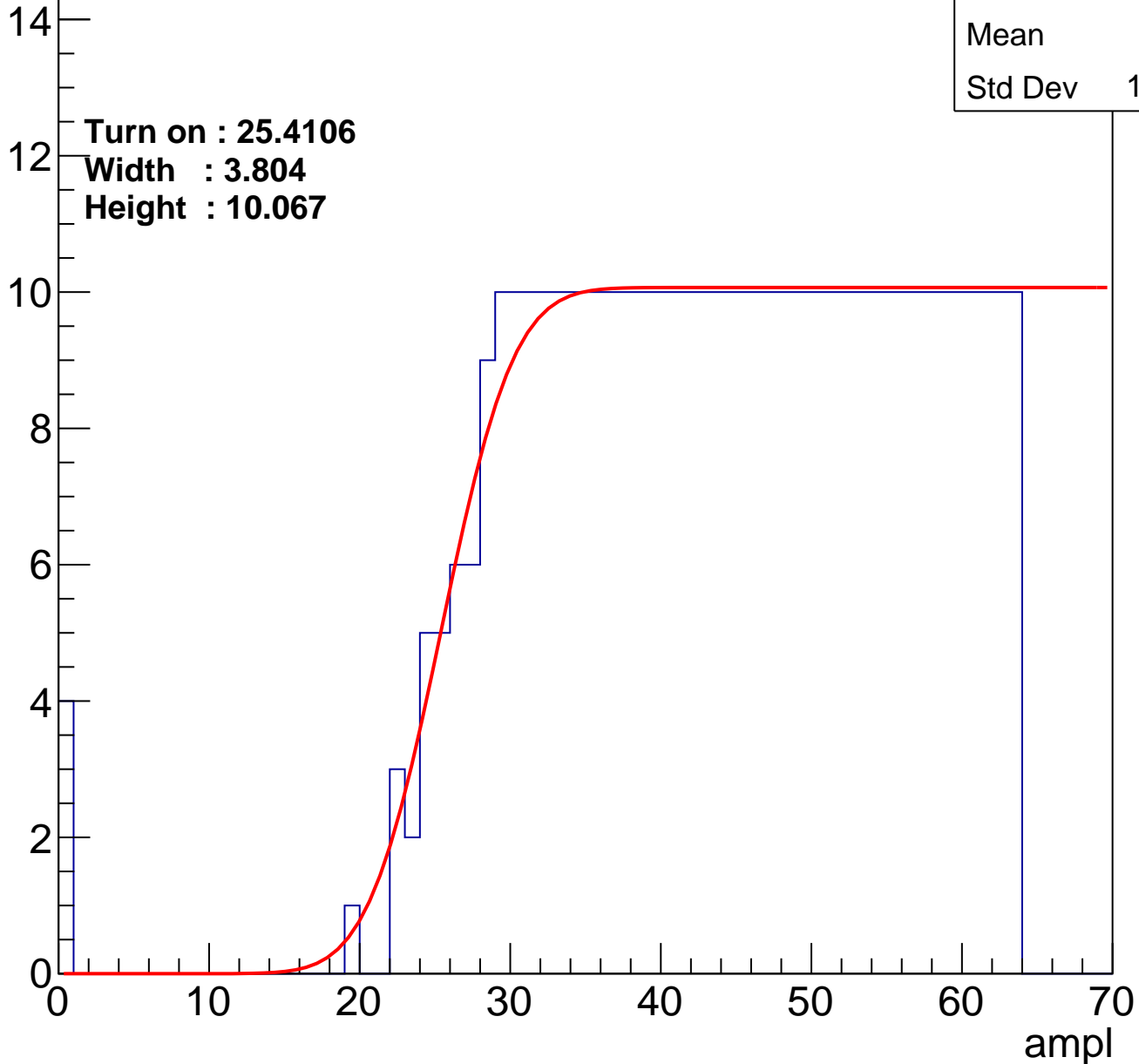
Entries	391
Mean	43.6
Std Dev	12.13

Turn on : 25.4106

Width : 3.804

Height : 10.067

Entry



# B1L101S, U7-ch35

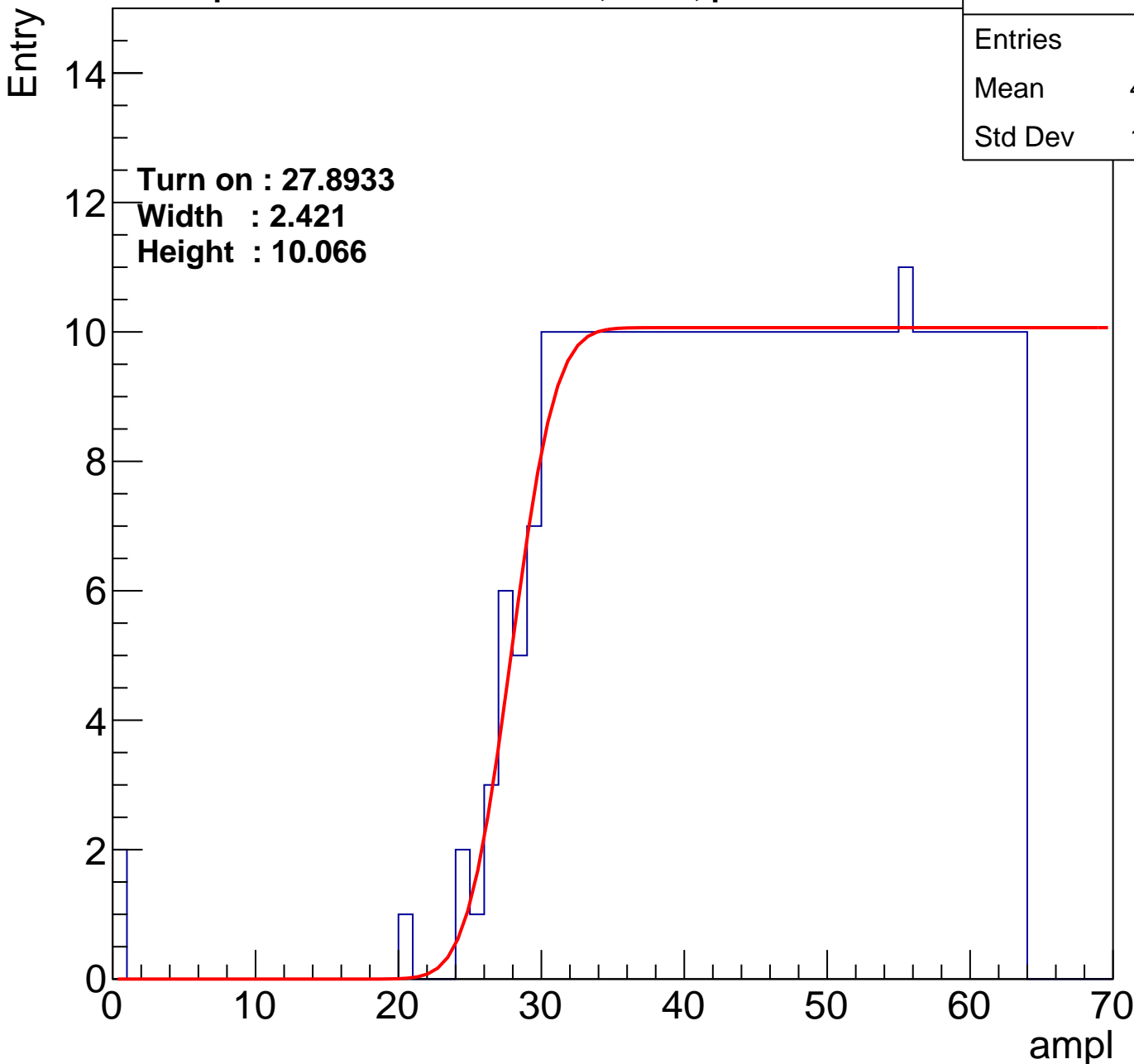
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	368
Mean	44.95
Std Dev	11.16

Turn on : 27.8933

Width : 2.421

Height : 10.066



# B1L101S, U7-ch36

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	384
Mean	44.1
Std Dev	11.49

**Turn on : 25.9497**

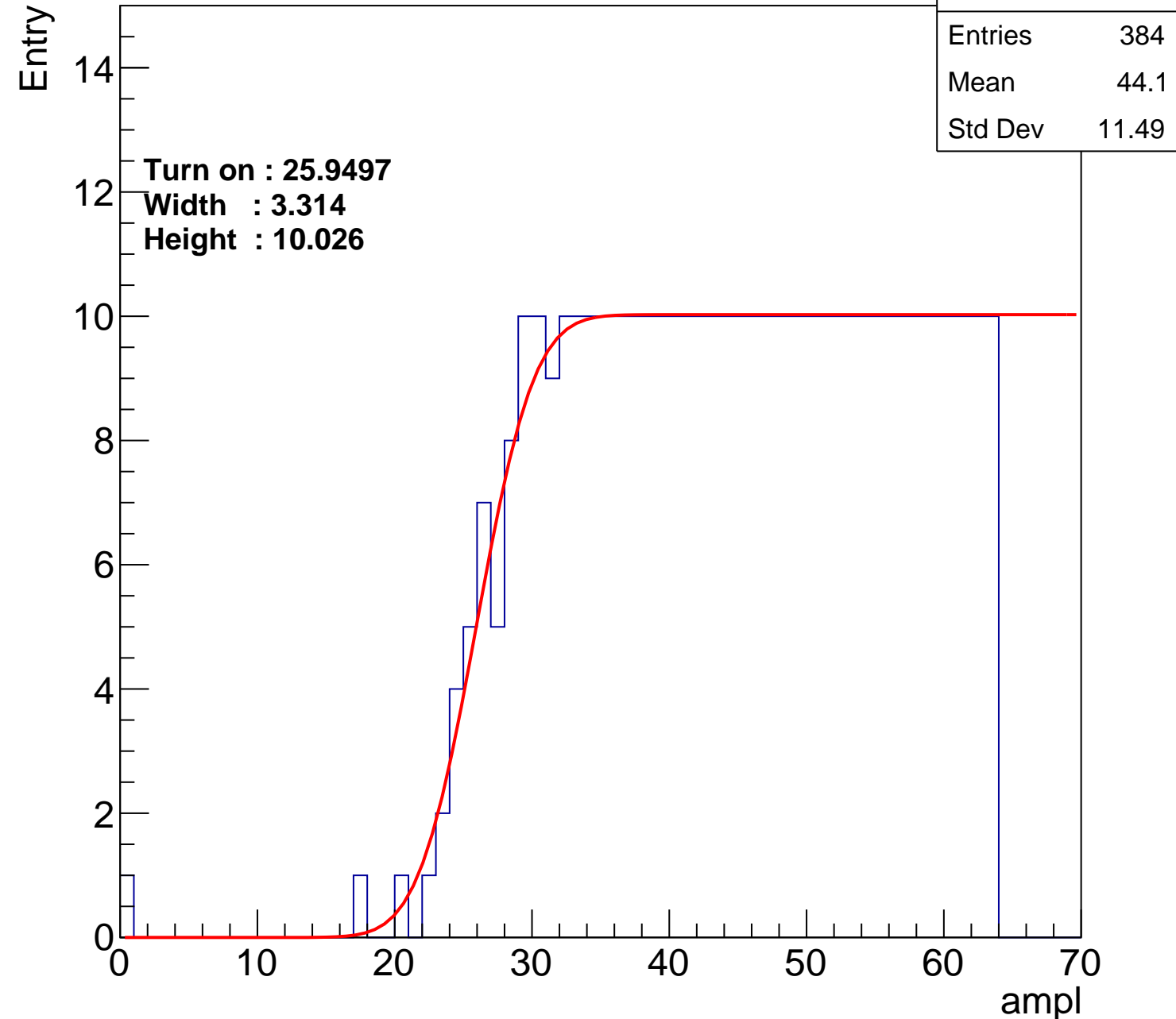
**Width : 3.314**

**Height : 10.026**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch37

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	380
Mean	44.16
Std Dev	11.83

**Turn on : 26.0645**

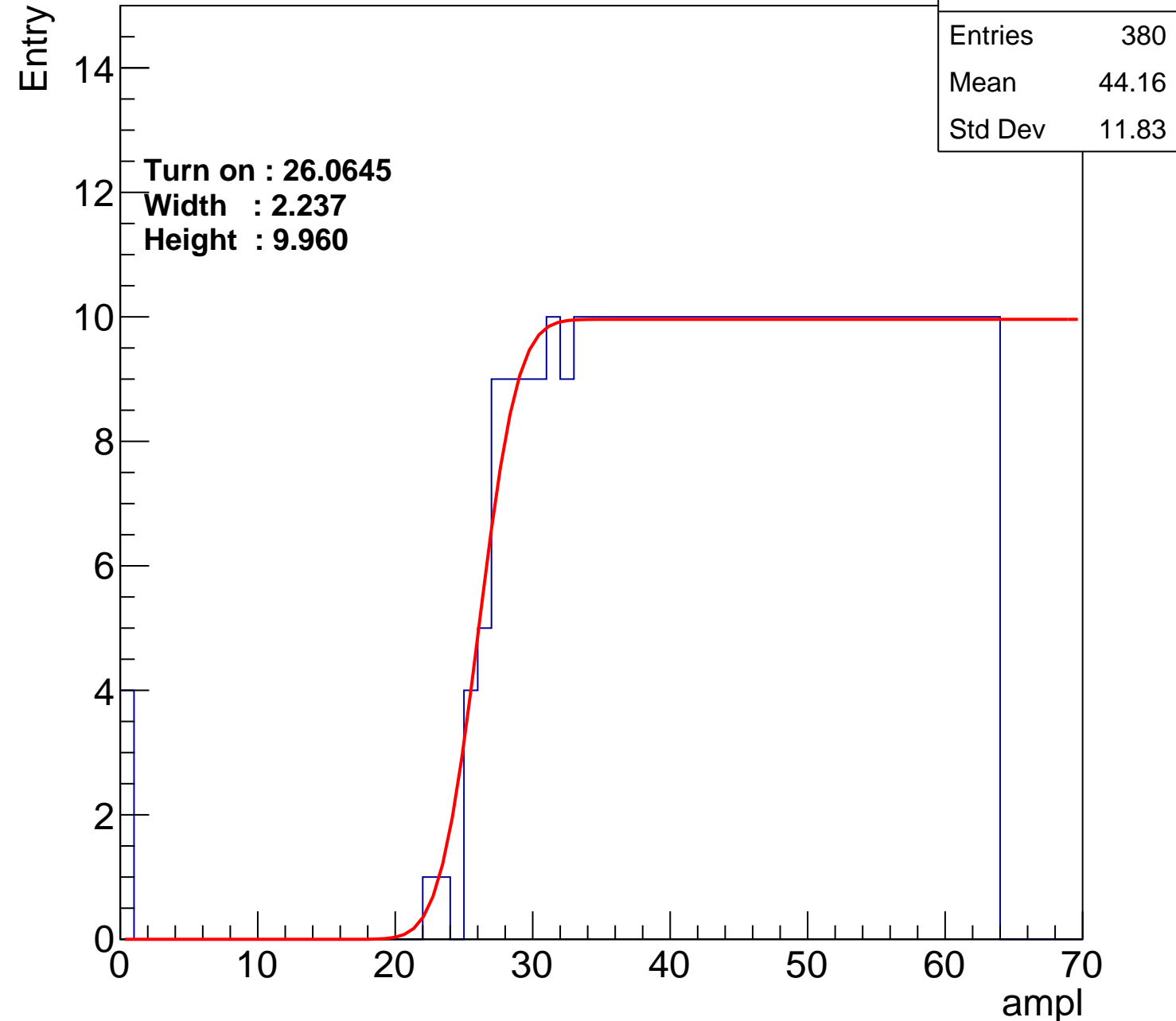
**Width : 2.237**

**Height : 9.960**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch38

calib\_packv5\_042523\_0143.root, FC#0, port D2

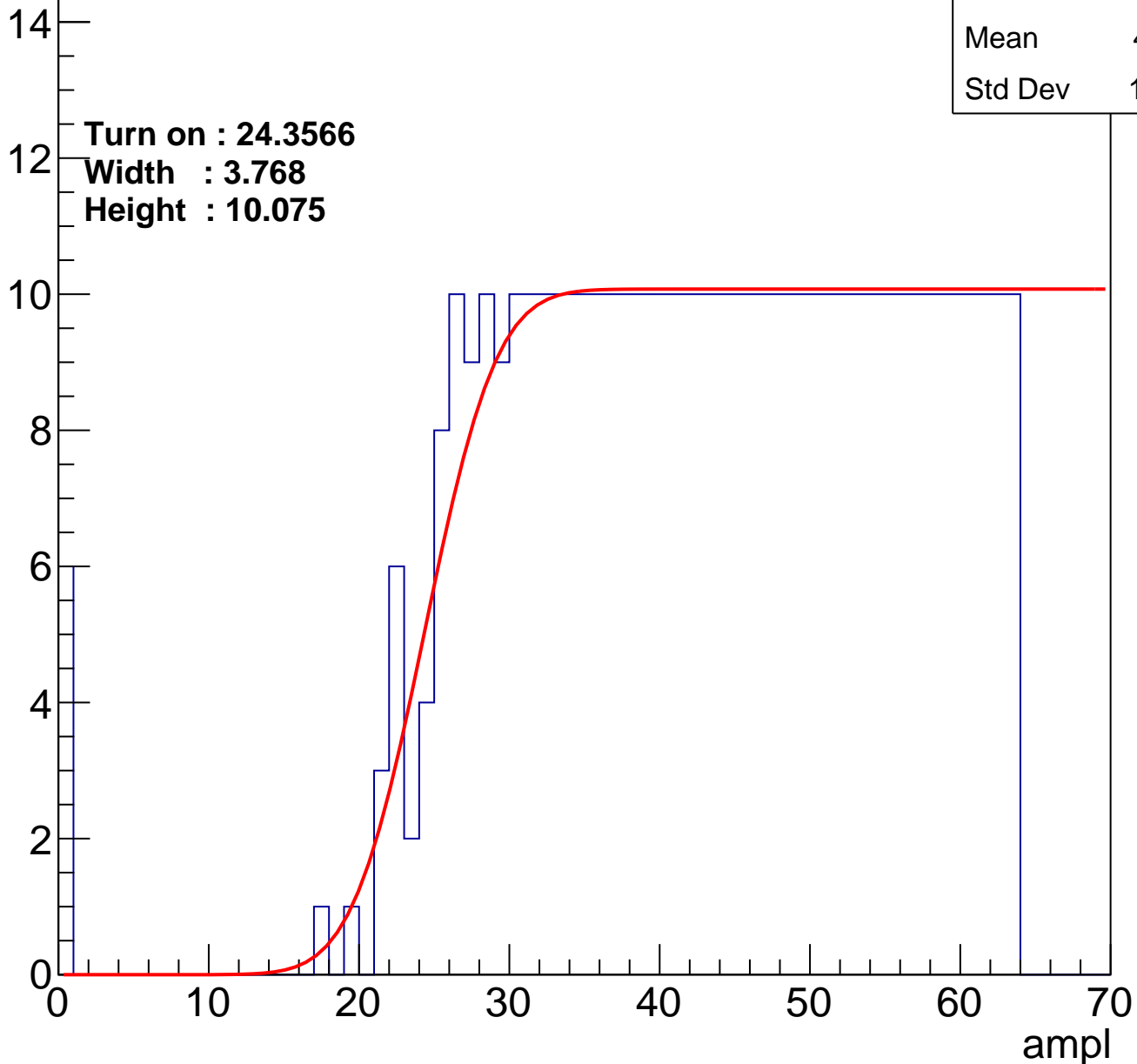
Entries	409
Mean	42.61
Std Dev	12.83

Turn on : 24.3566

Width : 3.768

Height : 10.075

Entry





# B1L101S, U7-ch39

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	390
Mean	43.8
Std Dev	11.73

Turn on : 25.7140

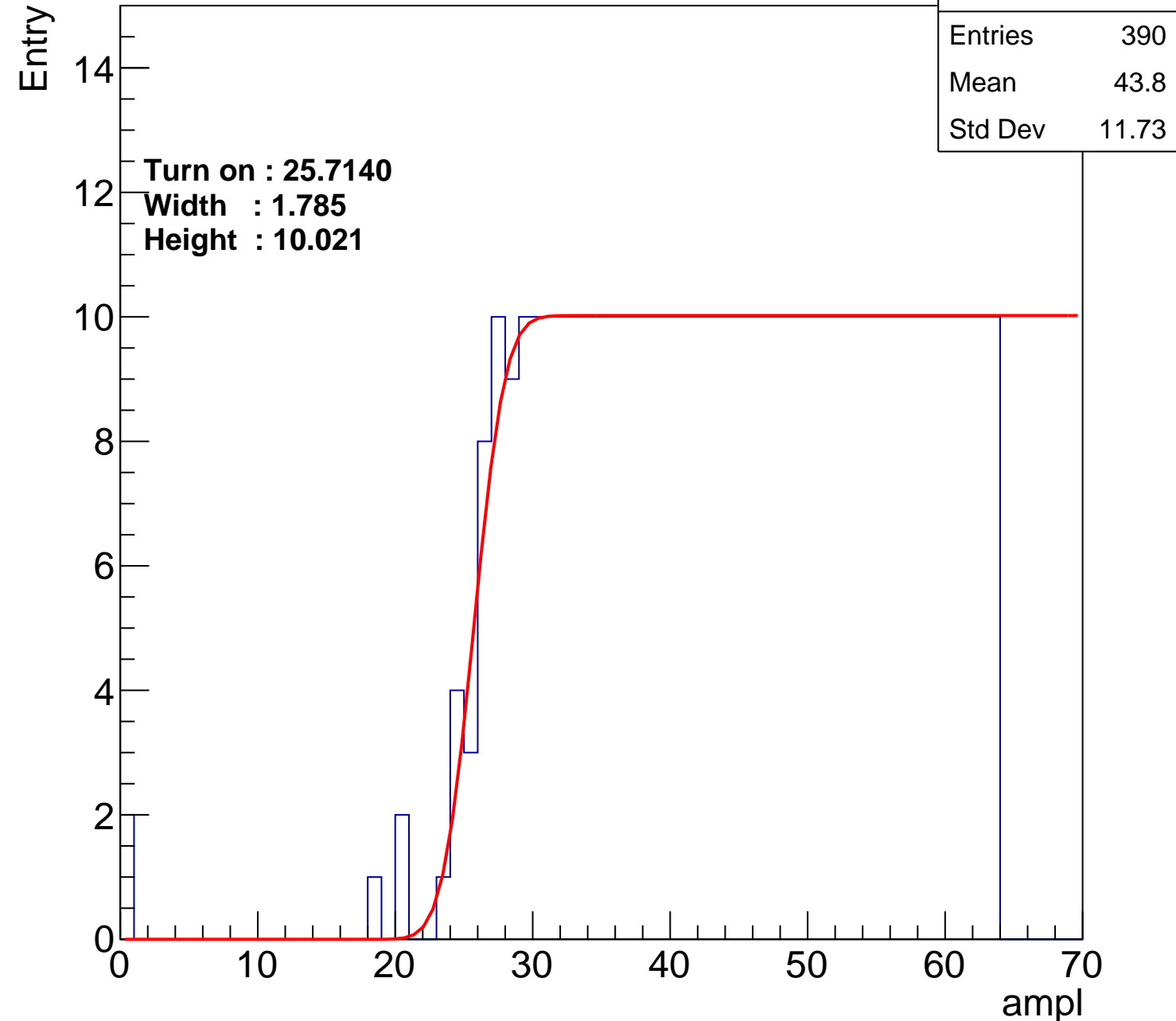
Width : 1.785

Height : 10.021

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch40

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	381
Mean	44.02
Std Dev	12.06

**Turn on : 26.3754**

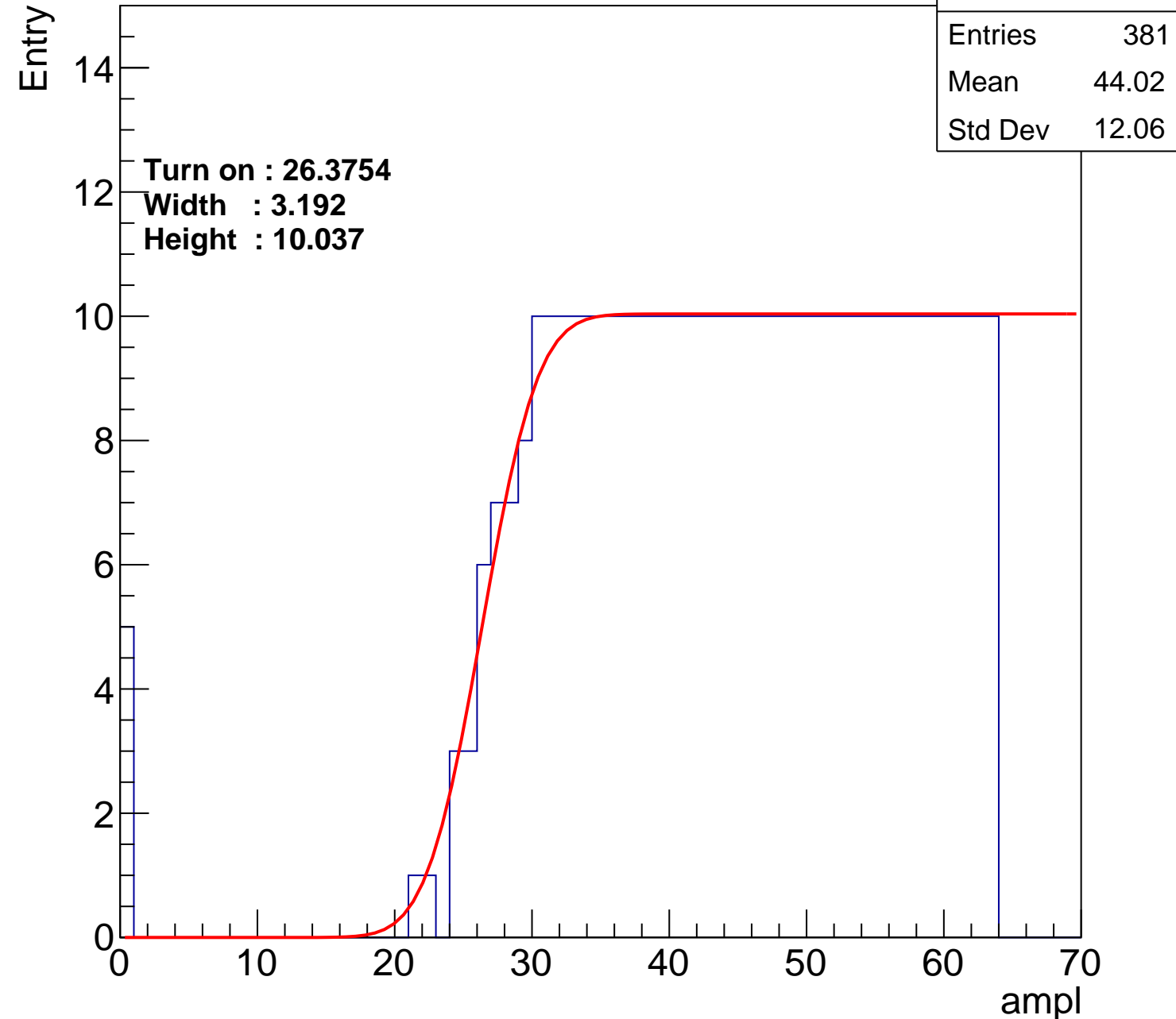
**Width : 3.192**

**Height : 10.037**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch41

calib\_packv5\_042523\_0143.root, FC#0, port D2

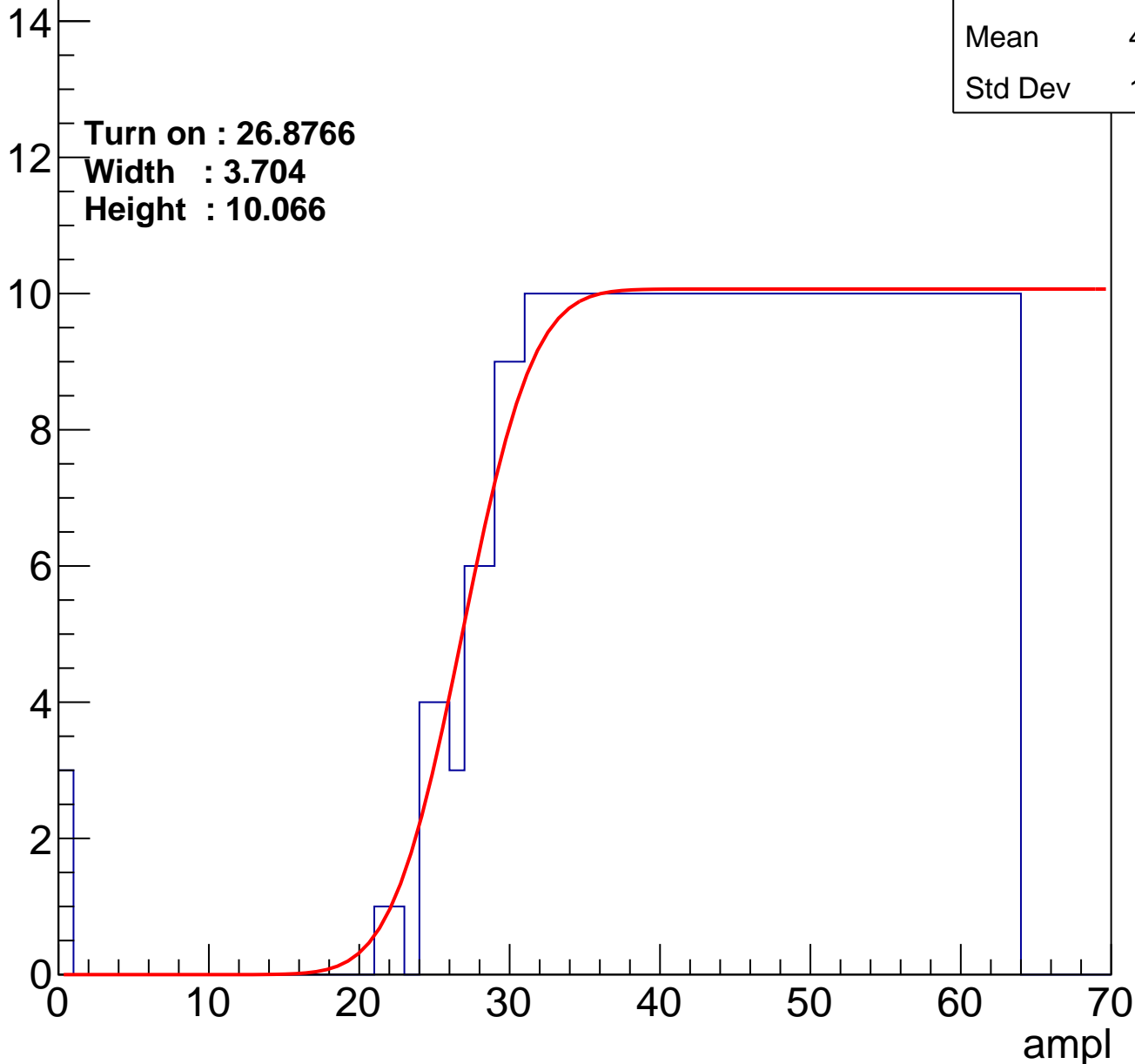
Entries	376
Mean	44.38
Std Dev	11.62

**Turn on : 26.8766**

**Width : 3.704**

**Height : 10.066**

Entry



# B1L101S, U7-ch42

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	390
Mean	43.87
Std Dev	11.54

Turn on : 25.0788

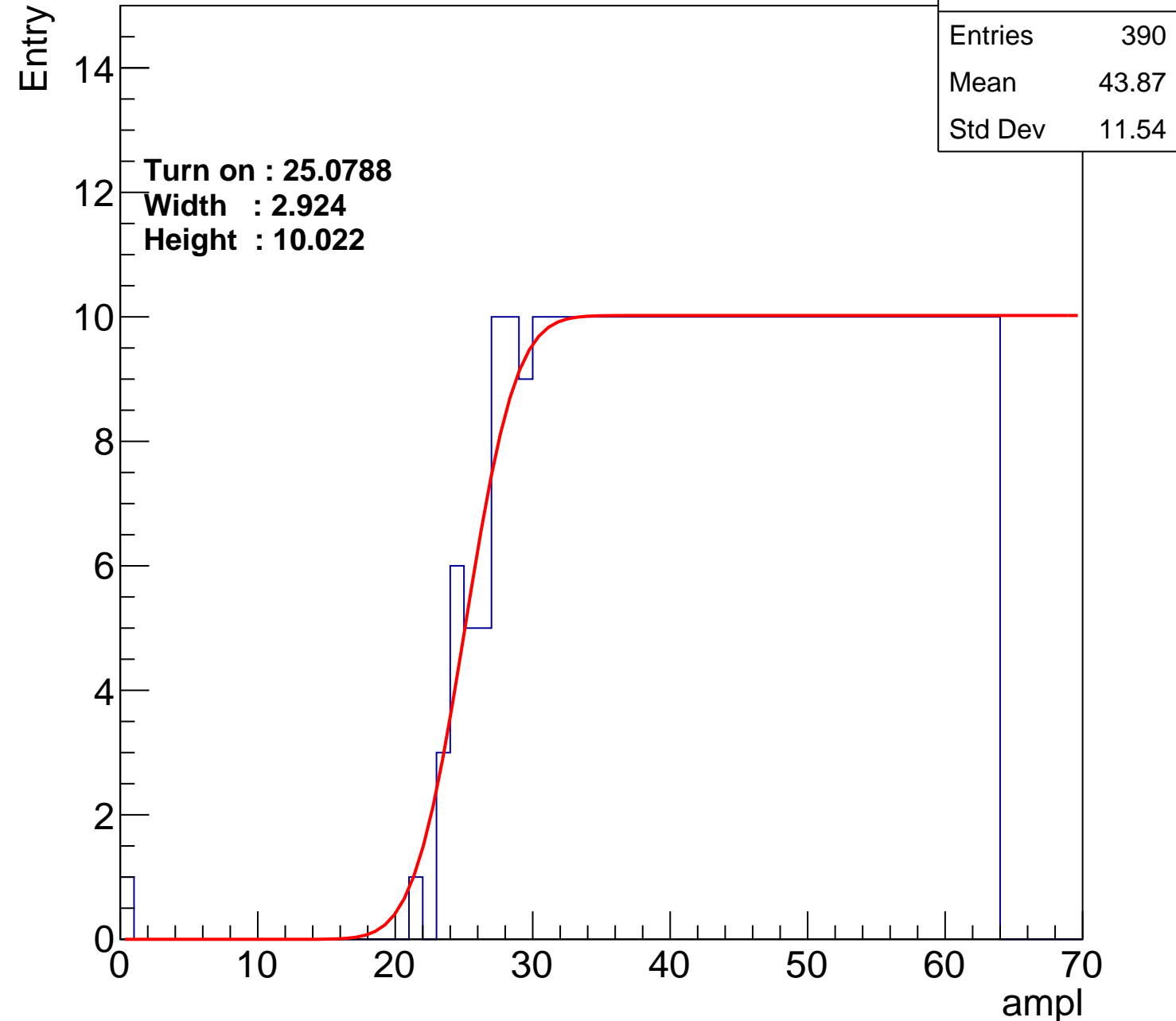
Width : 2.924

Height : 10.022

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch43

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	388
Mean	43.91
Std Dev	11.58

**Turn on : 25.9750**

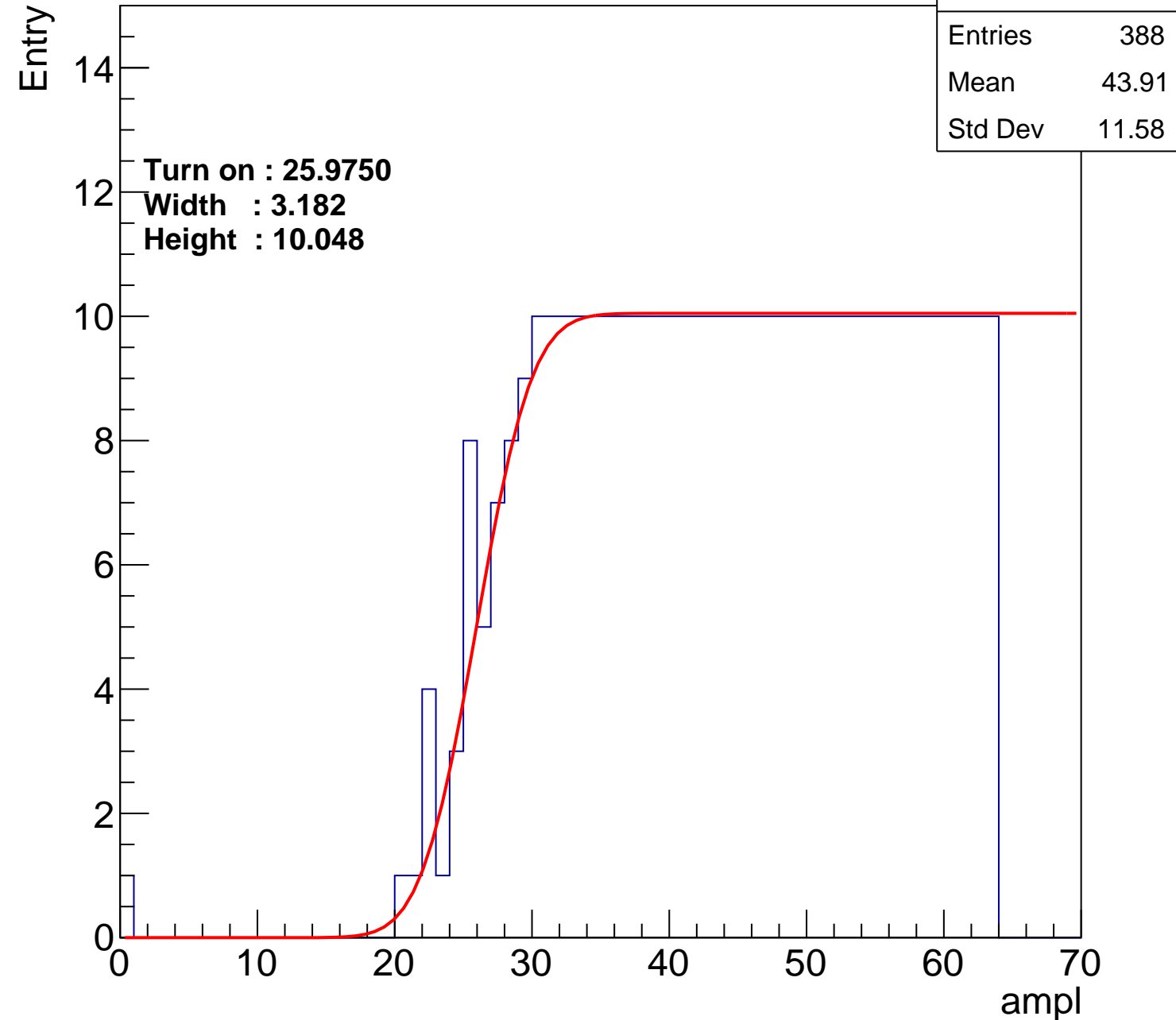
**Width : 3.182**

**Height : 10.048**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch44

calib\_packv5\_042523\_0143.root, FC#0, port D2

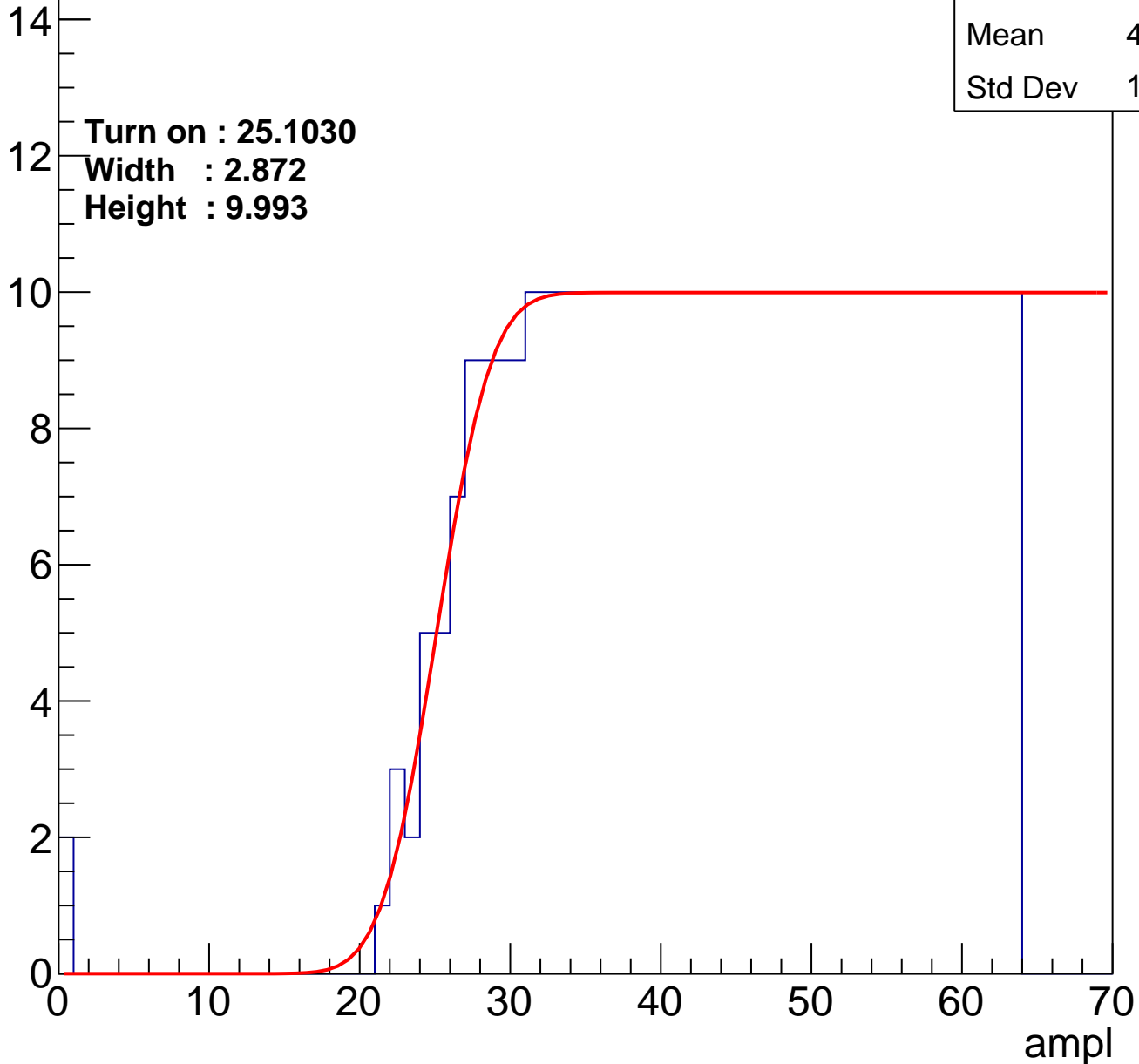
Entries	391
Mean	43.72
Std Dev	11.79

**Turn on : 25.1030**

**Width : 2.872**

**Height : 9.993**

Entry



# B1L101S, U7-ch45

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	375
Mean	44.42
Std Dev	11.61

Turn on : 27.1675

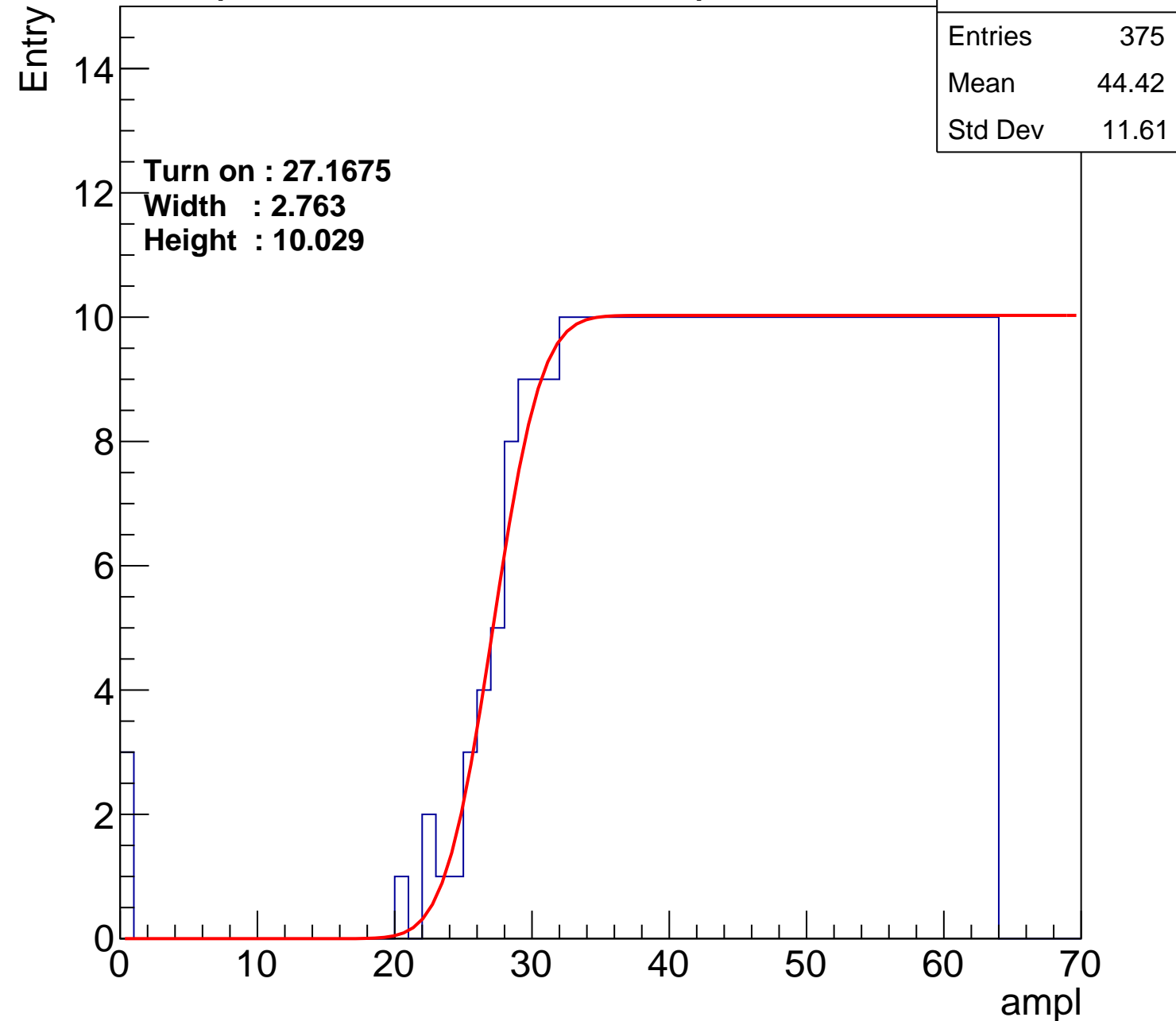
Width : 2.763

Height : 10.029

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch46

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	371
Mean	44.67
Std Dev	11.35

Turn on : 27.5926

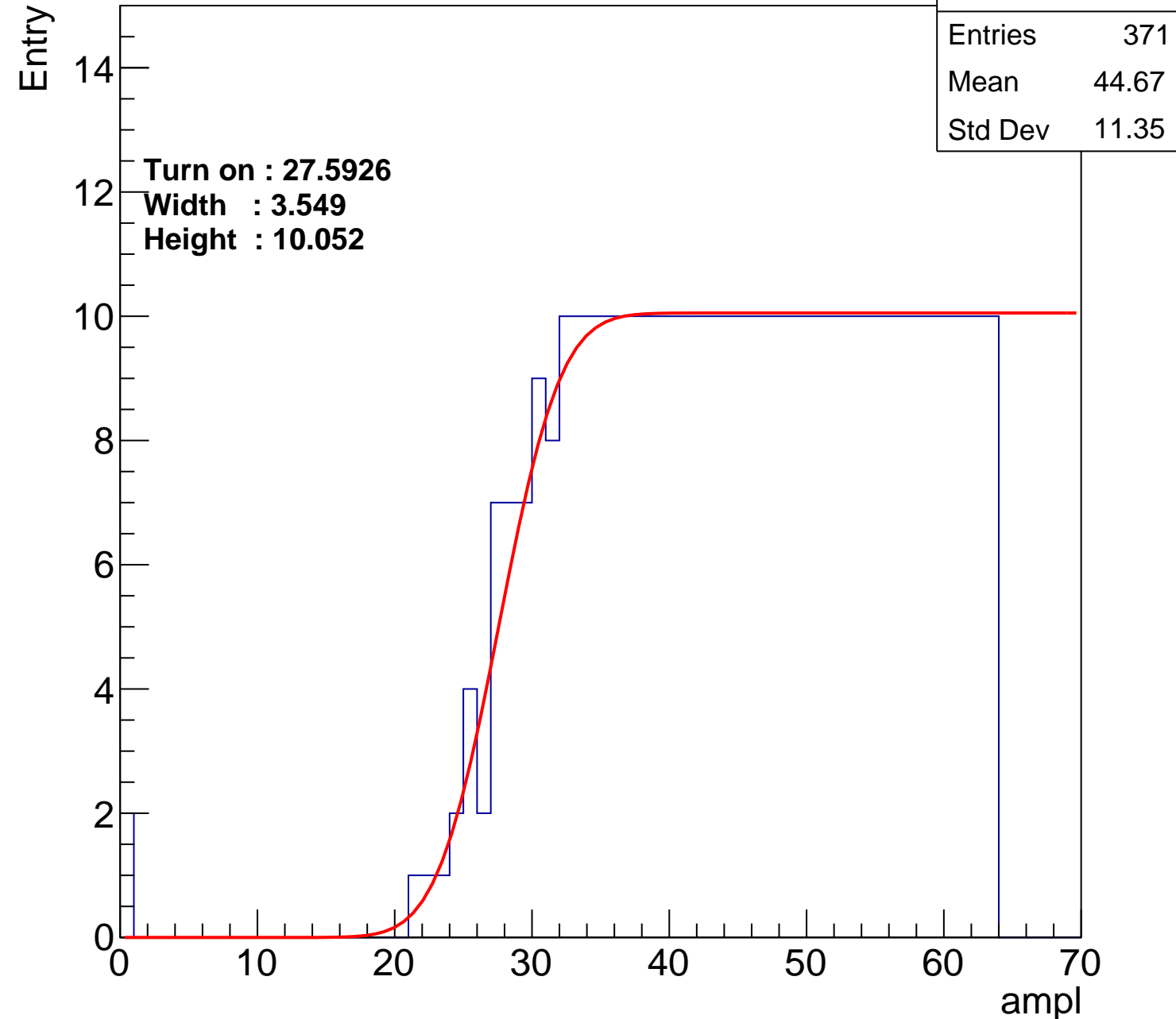
Width : 3.549

Height : 10.052

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U7-ch47

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	381
Mean	44.11
Std Dev	11.85

Turn on : 26.0596

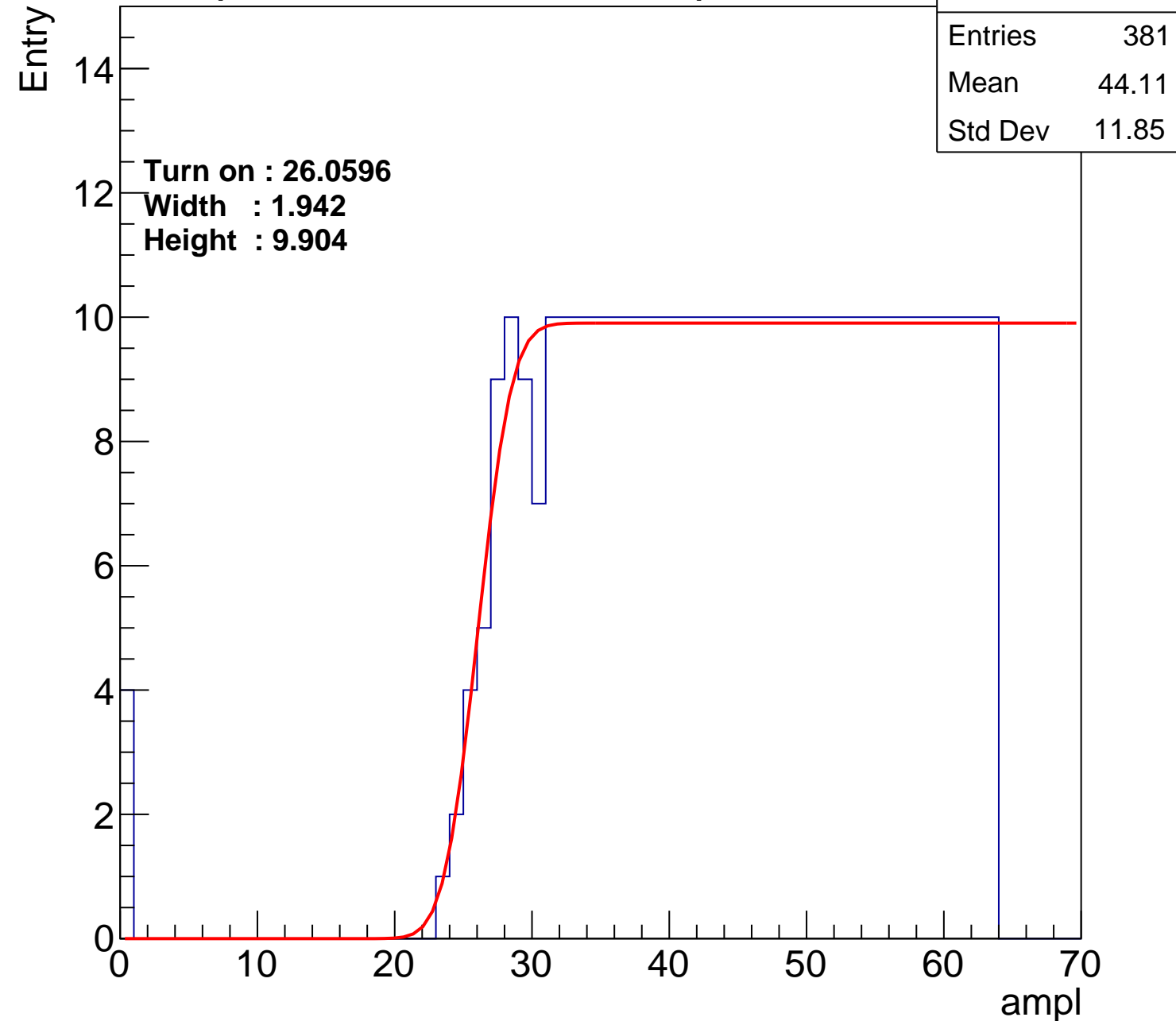
Width : 1.942

Height : 9.904

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch48

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	380
Mean	44.14
Std Dev	11.87

Turn on : 26.6131

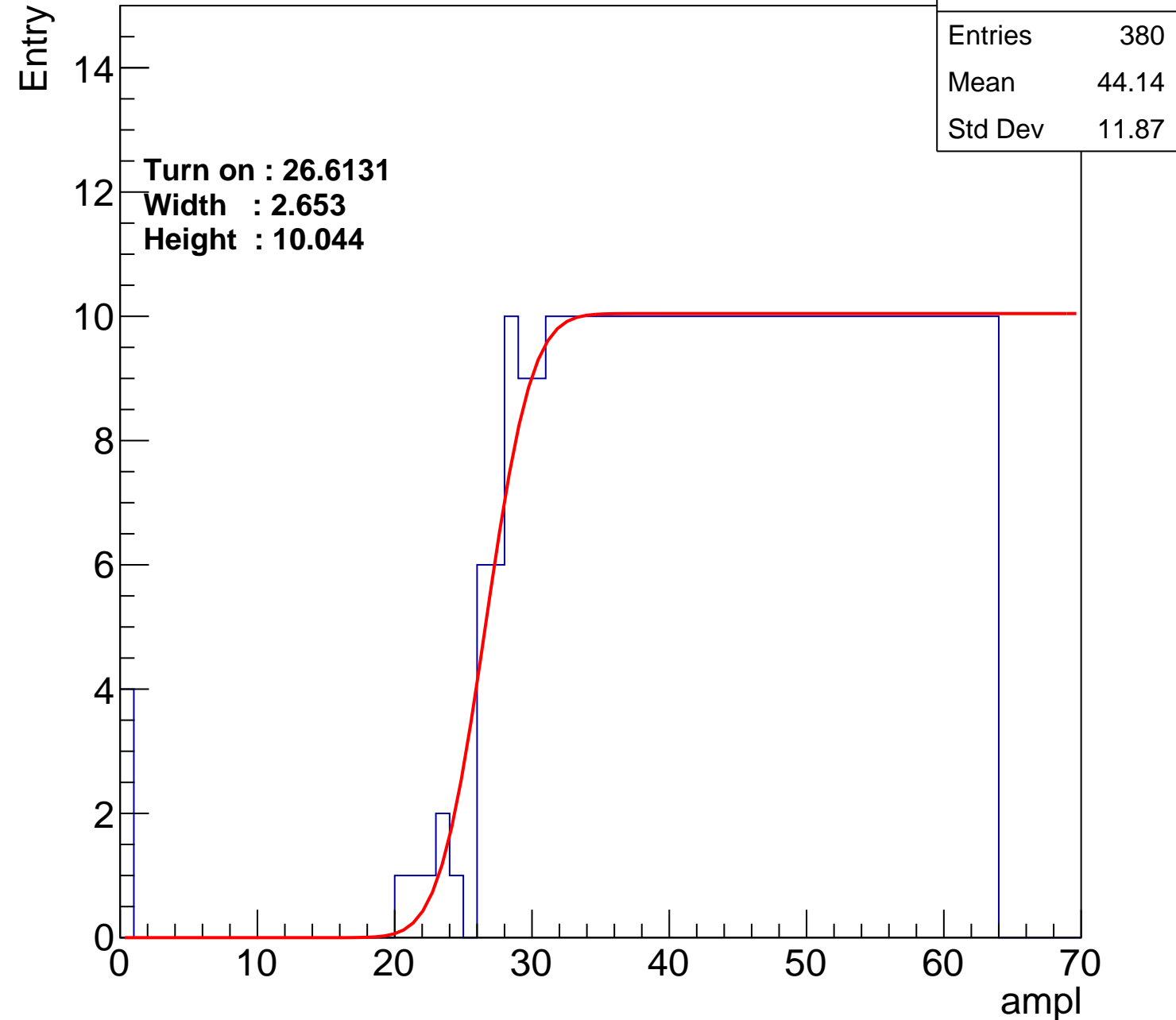
Width : 2.653

Height : 10.044

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch49

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	369
Mean	44.79
Std Dev	11.25

**Turn on : 27.3727**

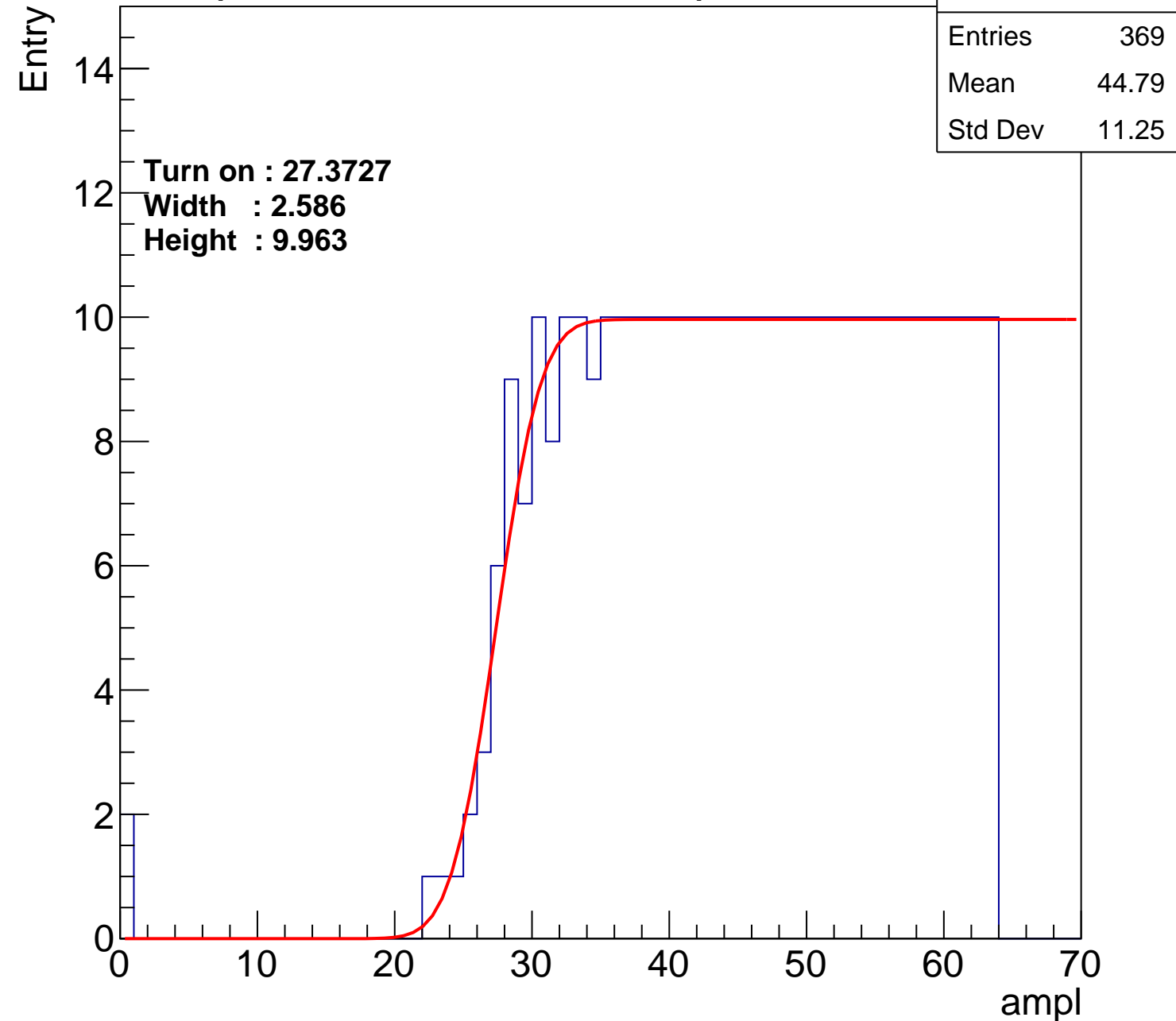
**Width : 2.586**

**Height : 9.963**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch50

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	372
Mean	44.57
Std Dev	11.53

**Turn on : 27.4067**

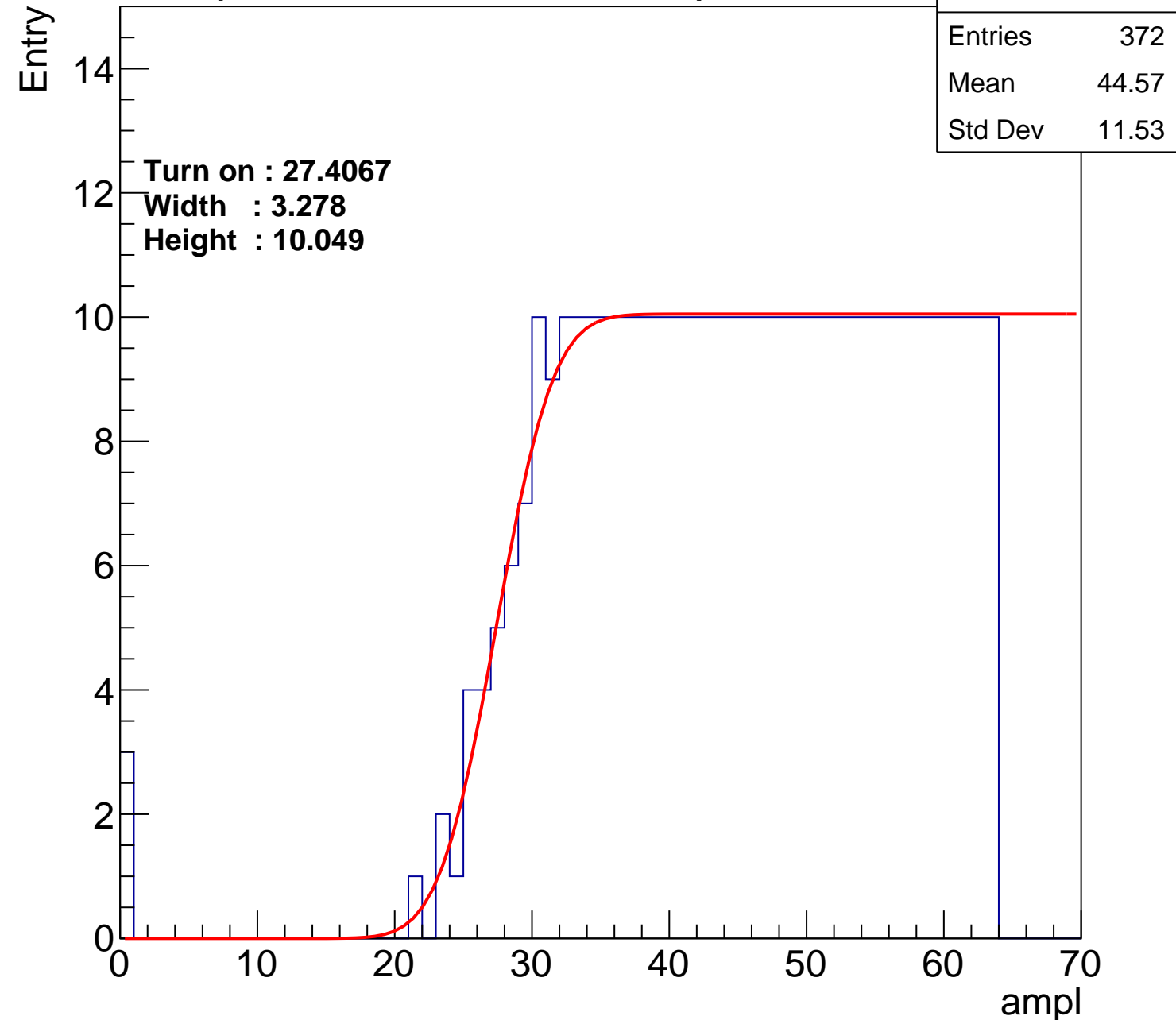
**Width : 3.278**

**Height : 10.049**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch51

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	362
Mean	45.13
Std Dev	11.09

Turn on : 28.0377

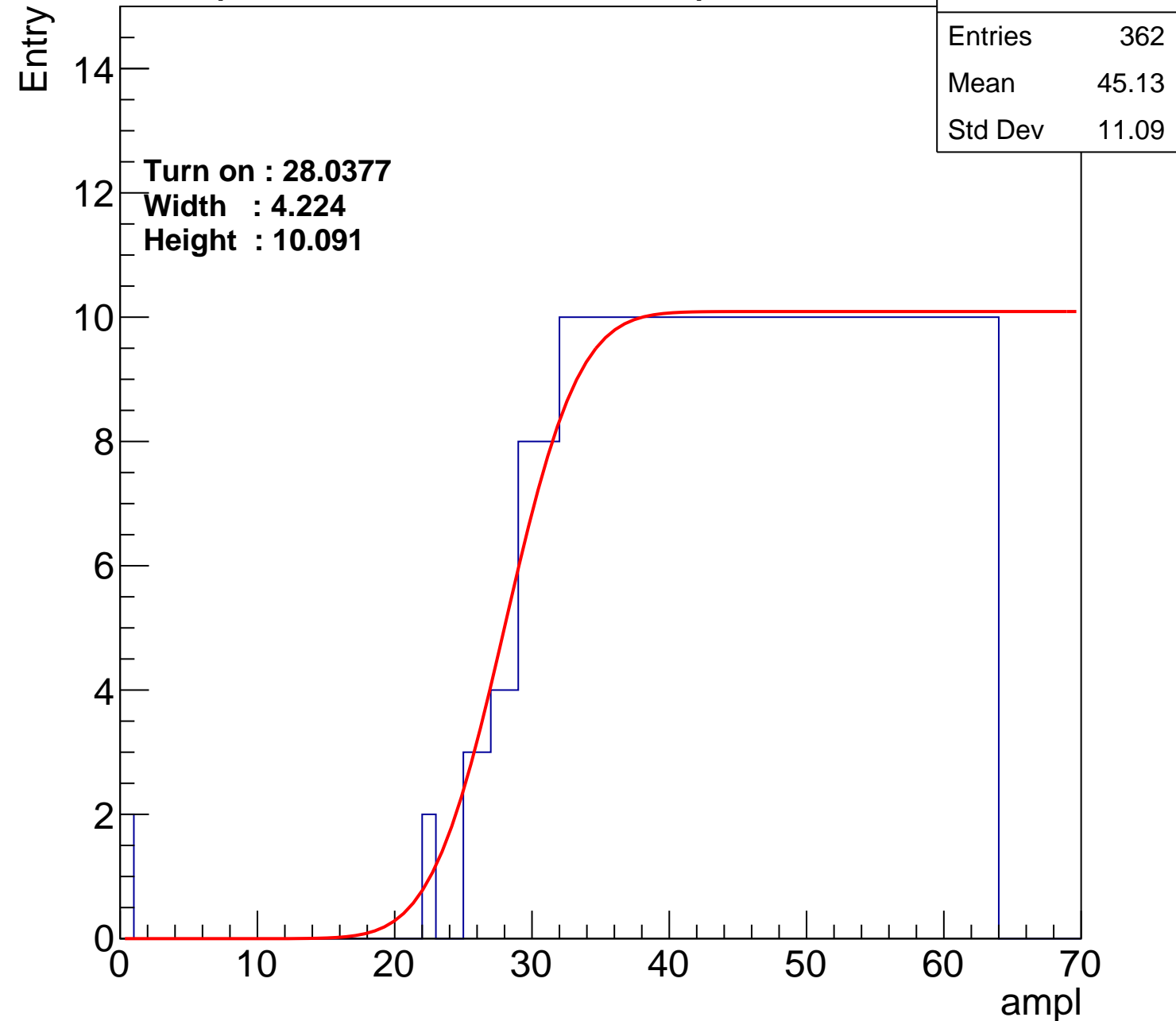
Width : 4.224

Height : 10.091

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch52

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	372
Mean	44.42
Std Dev	11.93

**Turn on : 27.6775**

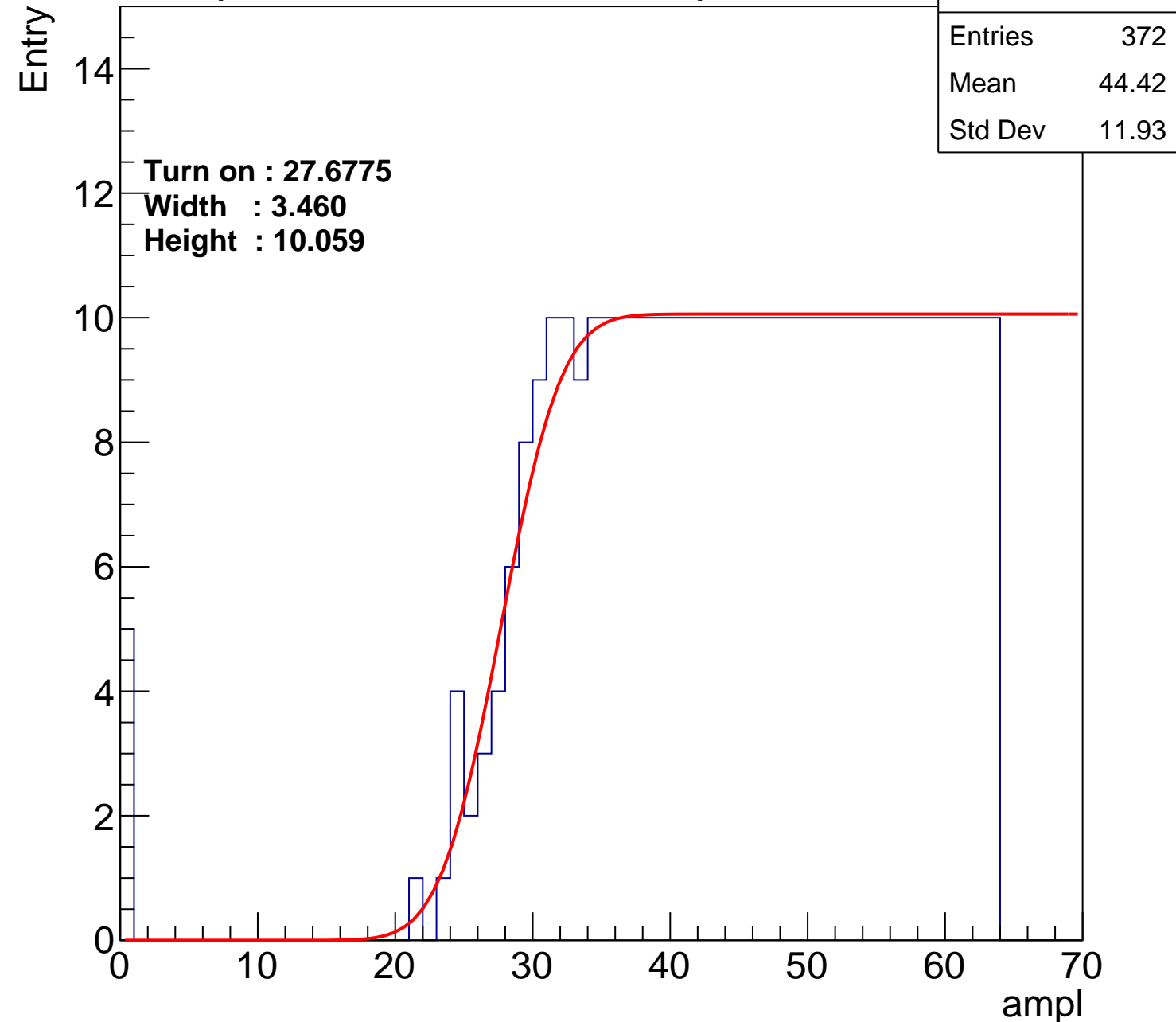
**Width : 3.460**

**Height : 10.059**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch53

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	378
Mean	44.33
Std Dev	11.51

Turn on : 26.8033

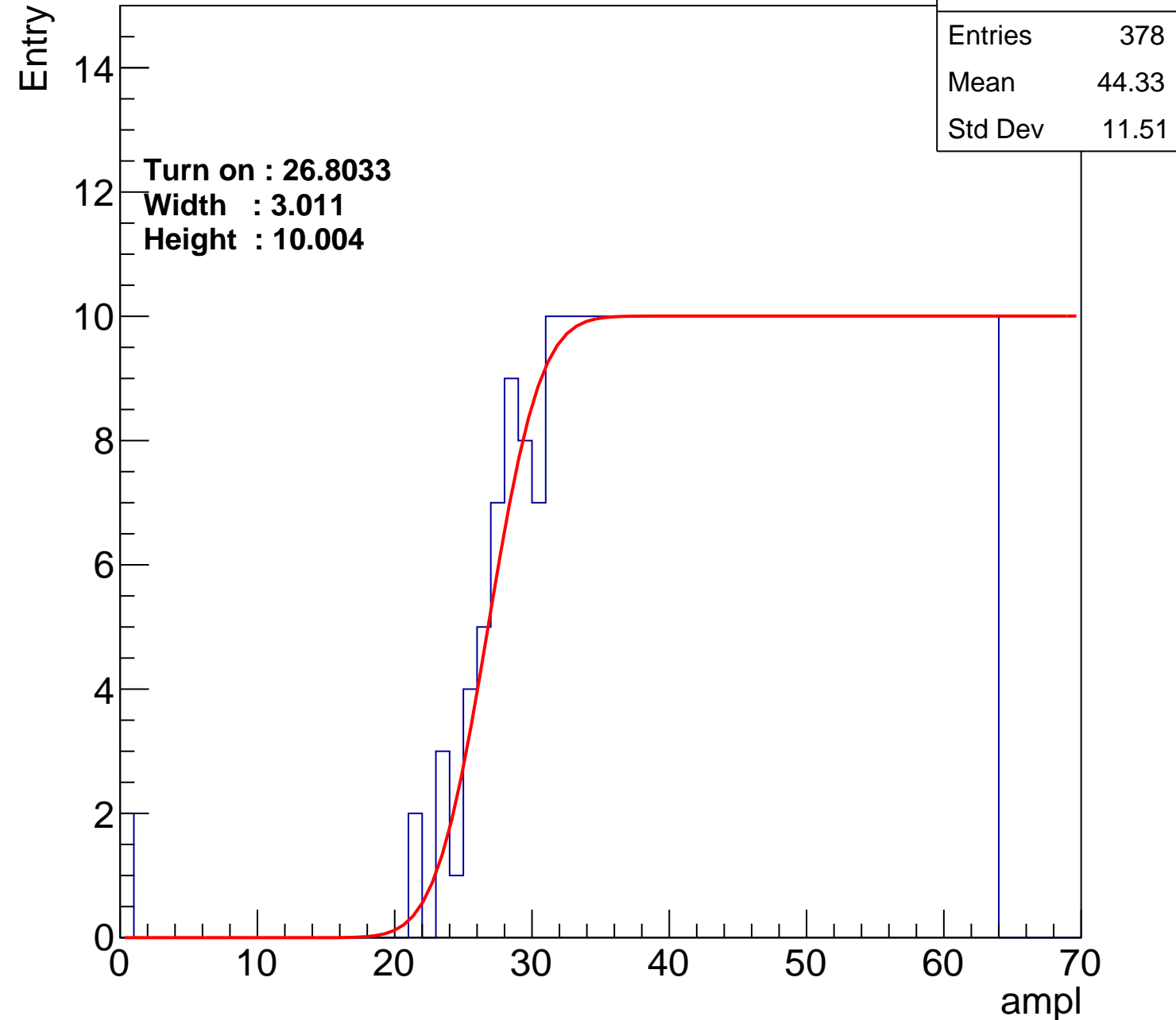
Width : 3.011

Height : 10.004

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch54

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	368
Mean	44.94
Std Dev	10.97

Turn on : 27.7054

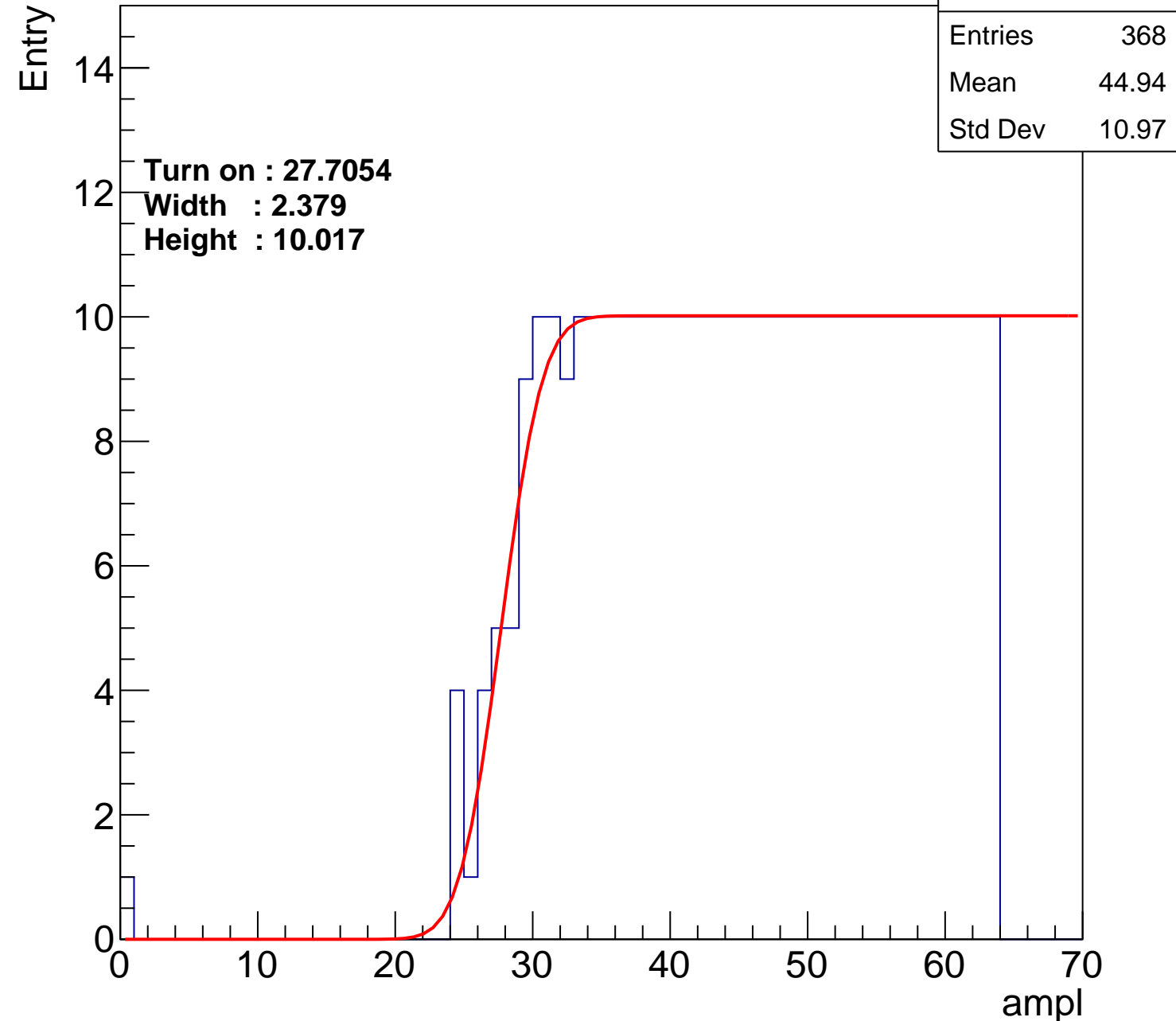
Width : 2.379

Height : 10.017

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U7-ch55

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	384
Mean	43.99
Std Dev	11.88

**Turn on : 25.7505**

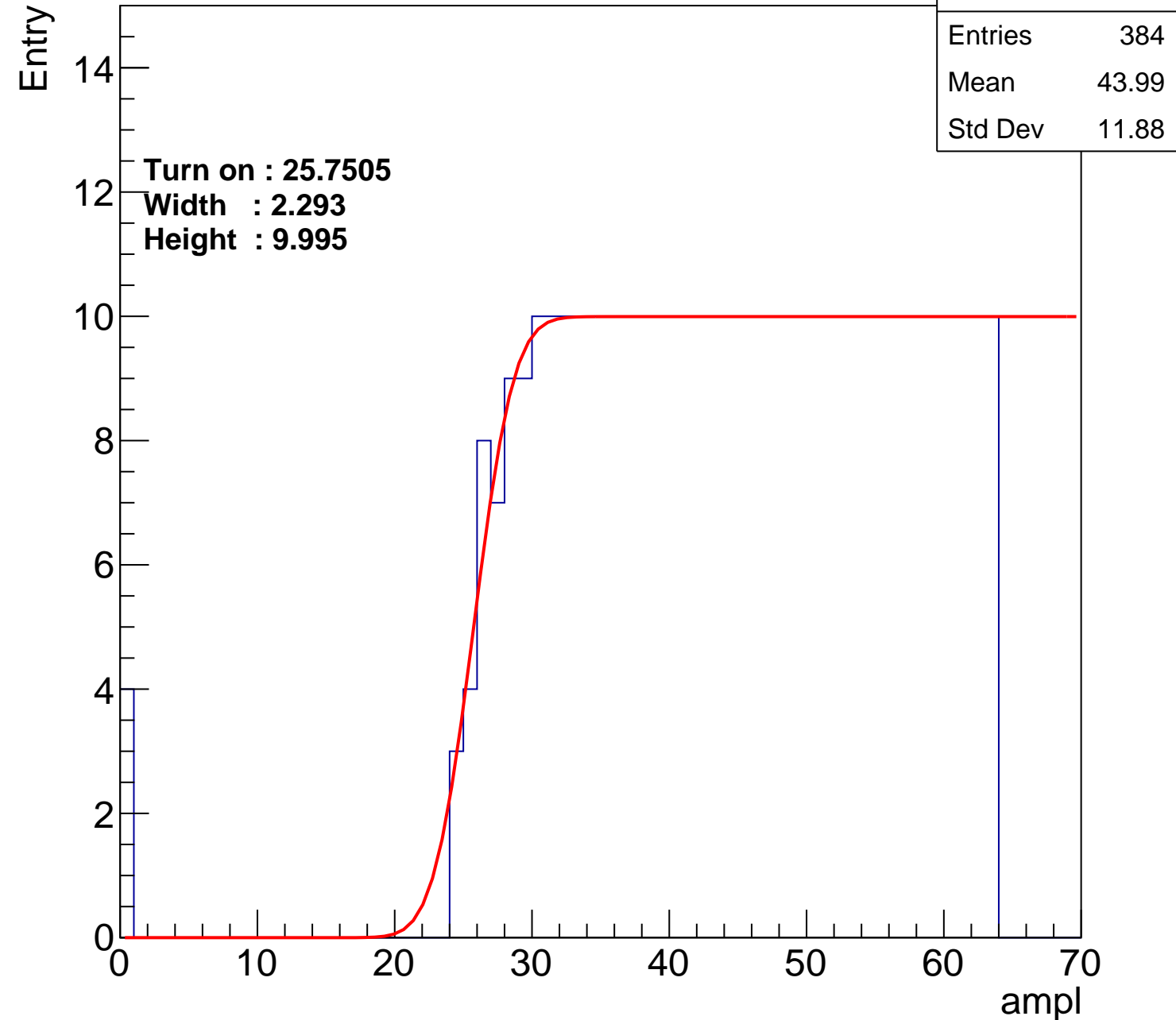
**Width : 2.293**

**Height : 9.995**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch56

calib\_packv5\_042523\_0143.root, FC#0, port D2

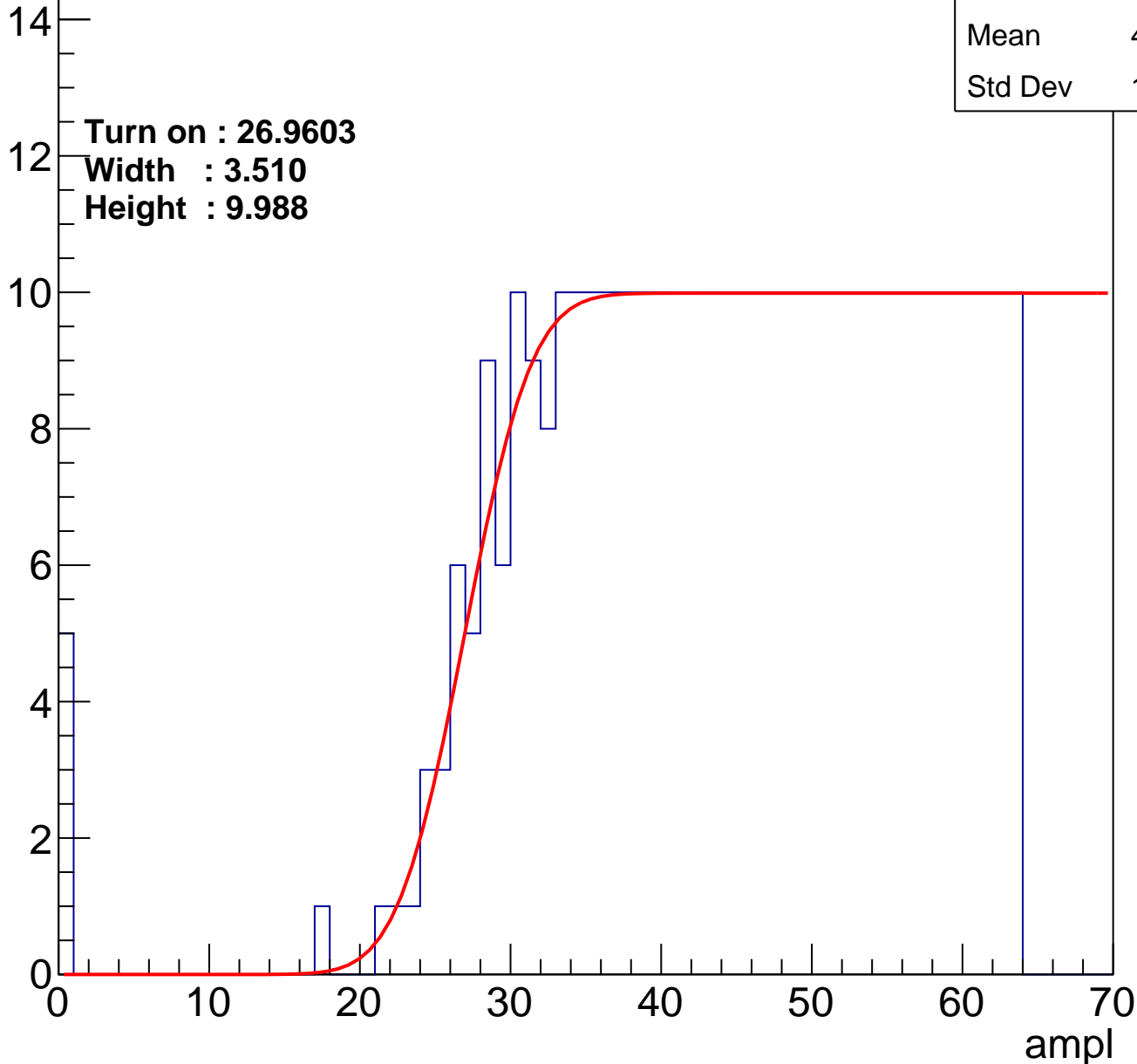
Entries	378
Mean	44.08
Std Dev	12.13

Turn on : 26.9603

Width : 3.510

Height : 9.988

Entry



# B1L101S, U7-ch57

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	389
Mean	43.76
Std Dev	11.9

Turn on : 24.6519

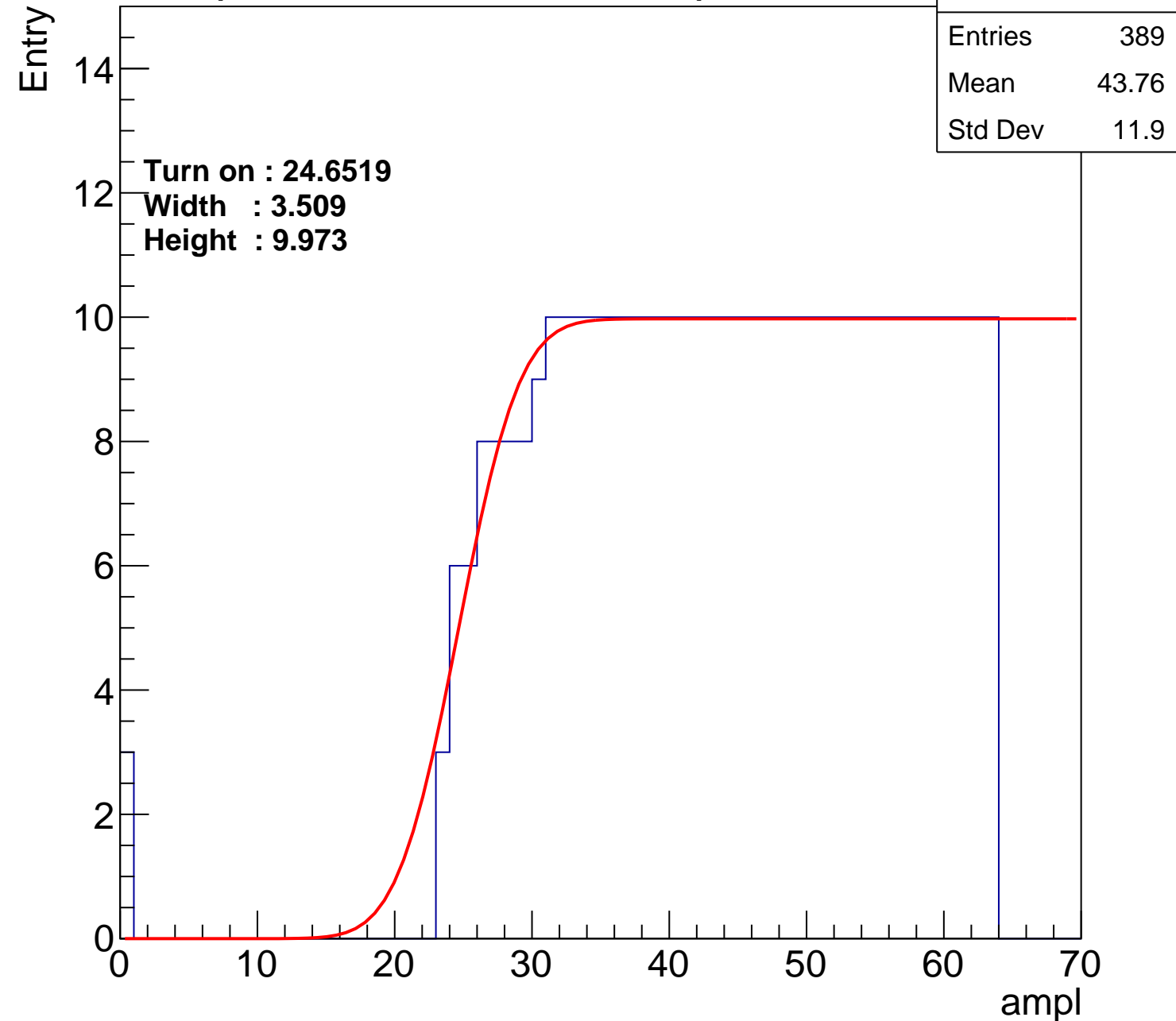
Width : 3.509

Height : 9.973

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch58

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	411
Mean	42.72
Std Dev	12.41

**Turn on : 23.2095**

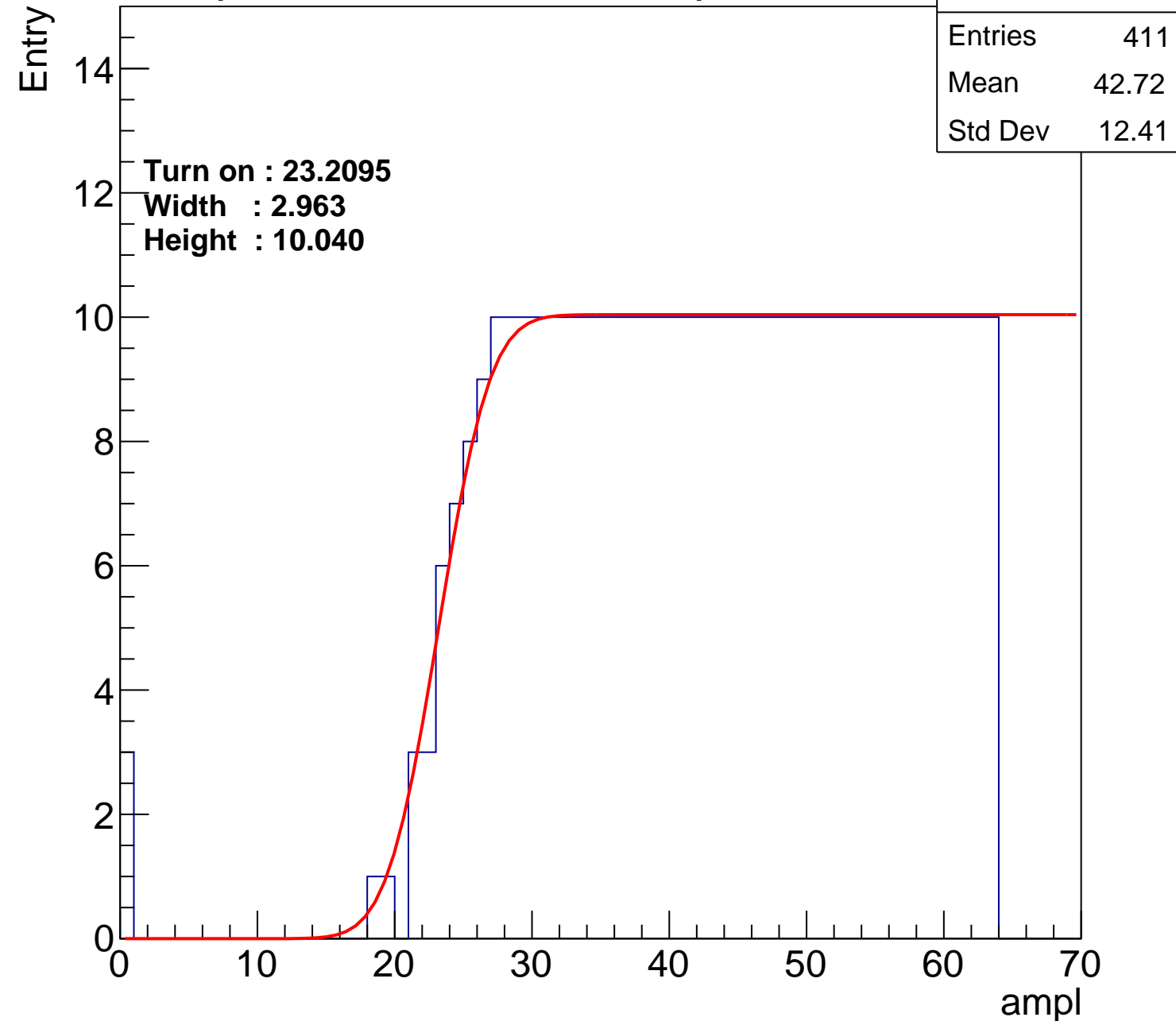
**Width : 2.963**

**Height : 10.040**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch59

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	380
Mean	44
Std Dev	12.21

Turn on : 27.1966

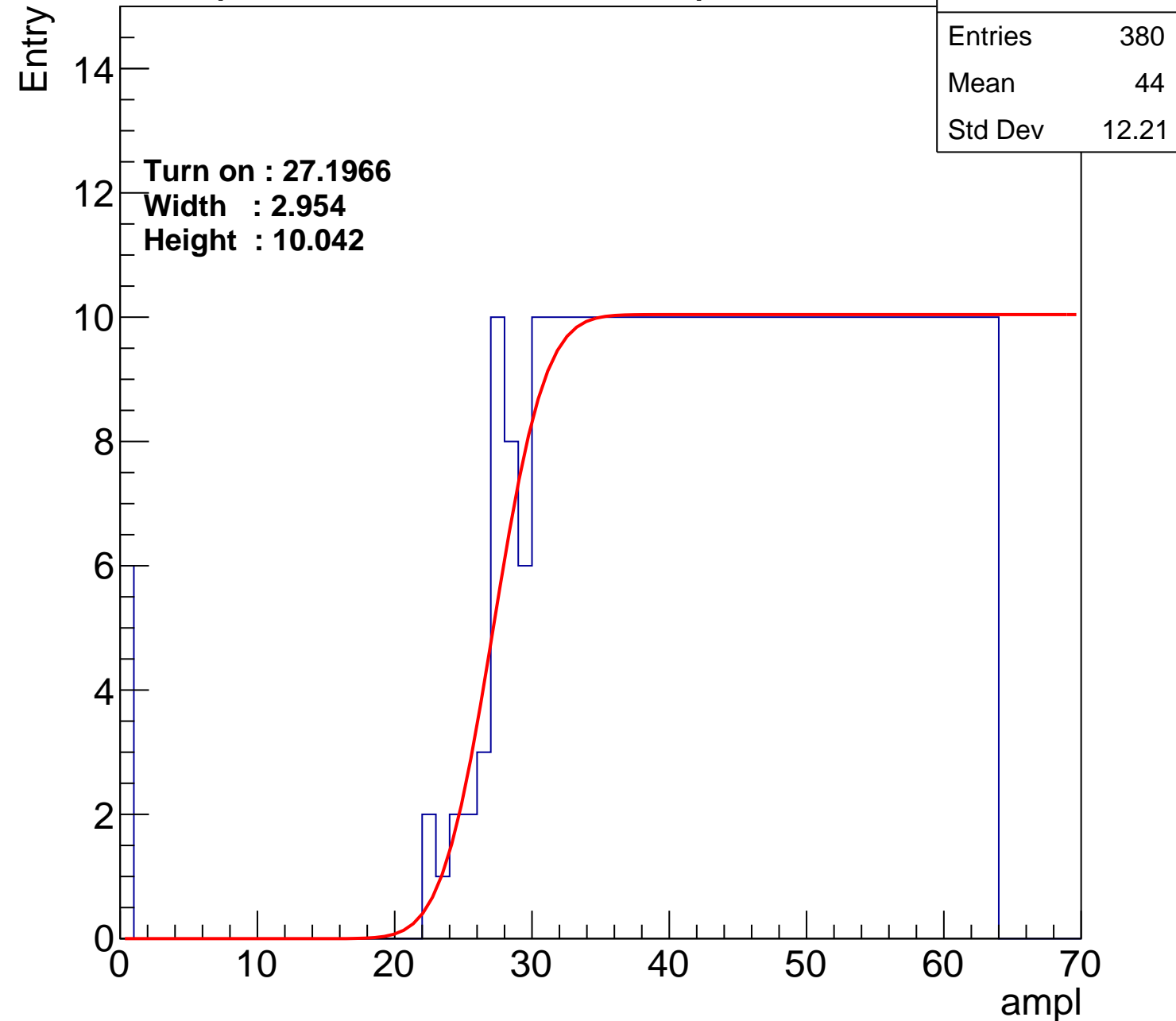
Width : 2.954

Height : 10.042

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch60

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	384
Mean	44.09
Std Dev	11.58

Turn on : 26.1282

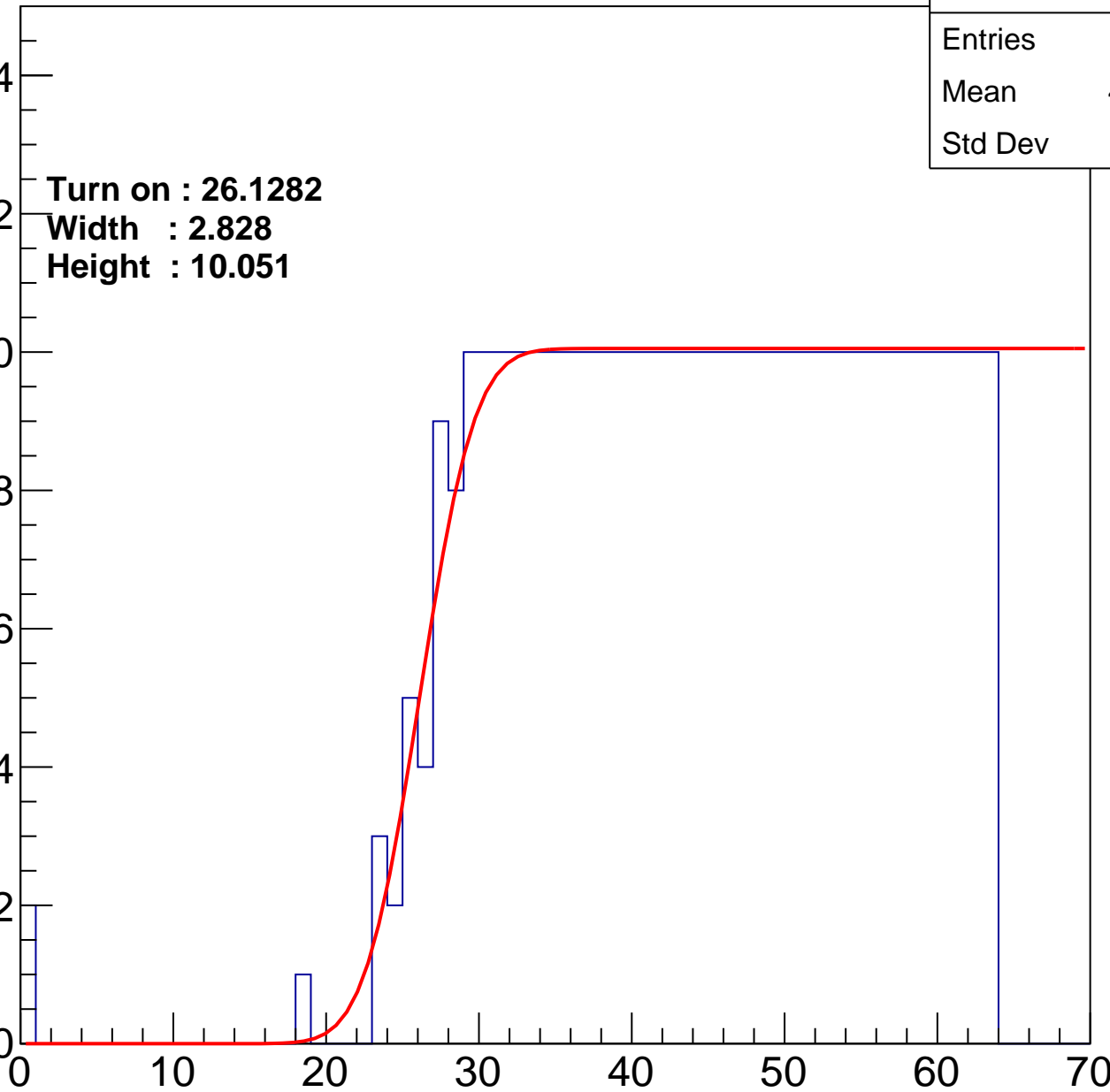
Width : 2.828

Height : 10.051

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch61

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	348
Mean	45.83
Std Dev	10.72

Turn on : 29.8134

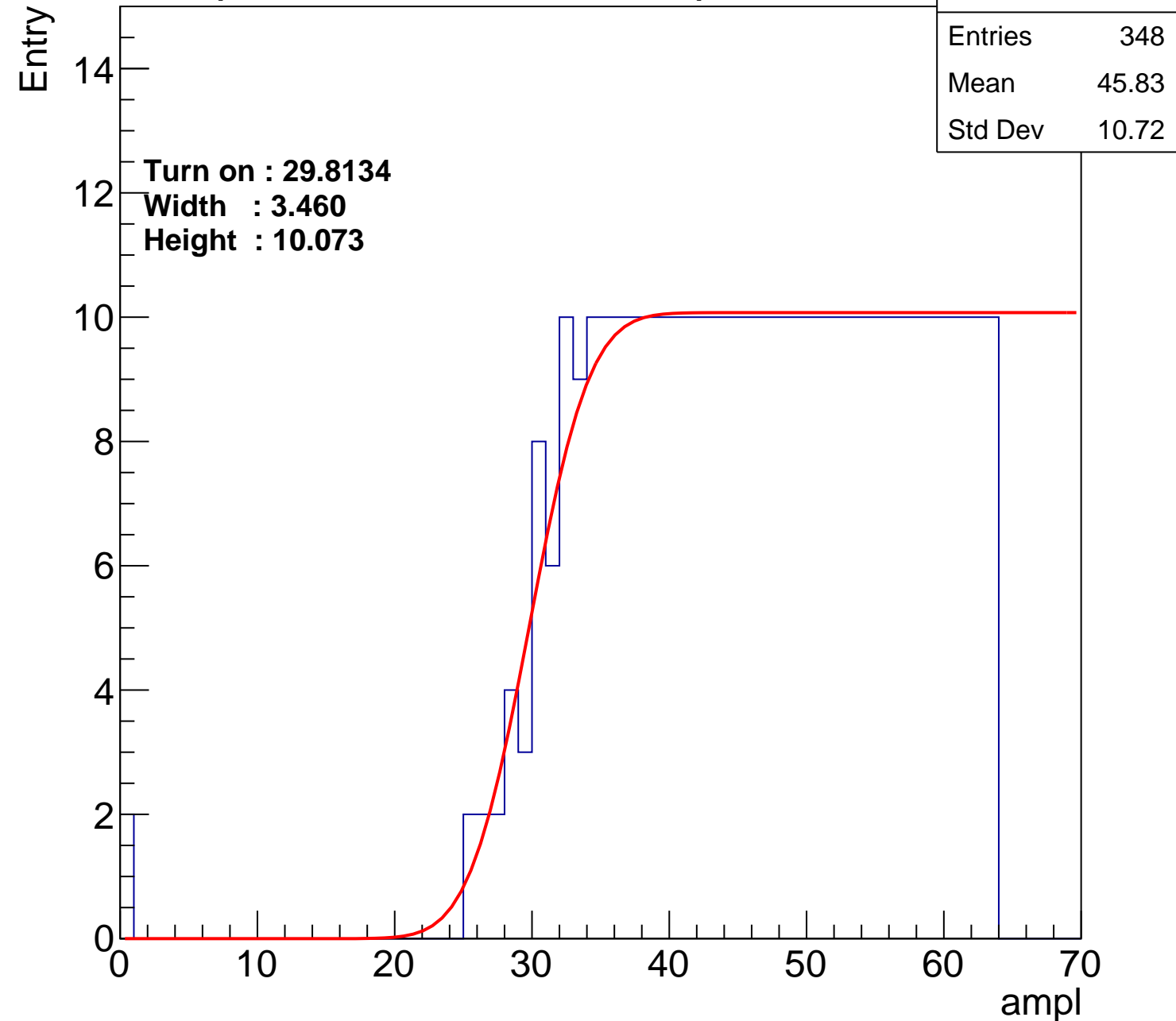
Width : 3.460

Height : 10.073

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch62

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	376
Mean	44.24
Std Dev	11.98

**Turn on : 26.9167**

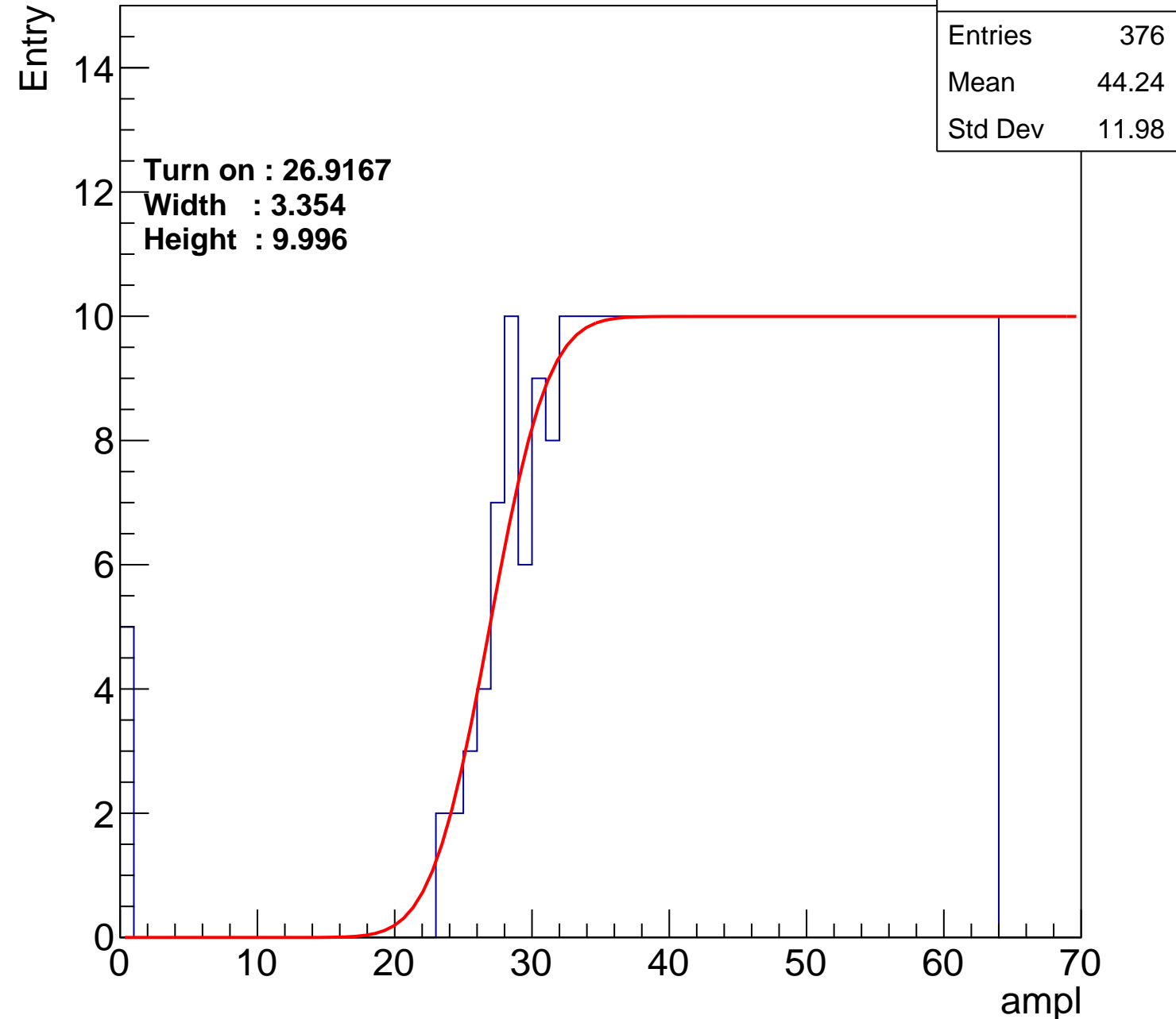
**Width : 3.354**

**Height : 9.996**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U7-ch63

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	370
Mean	44.79
Std Dev	11.21

Turn on : 27.1632

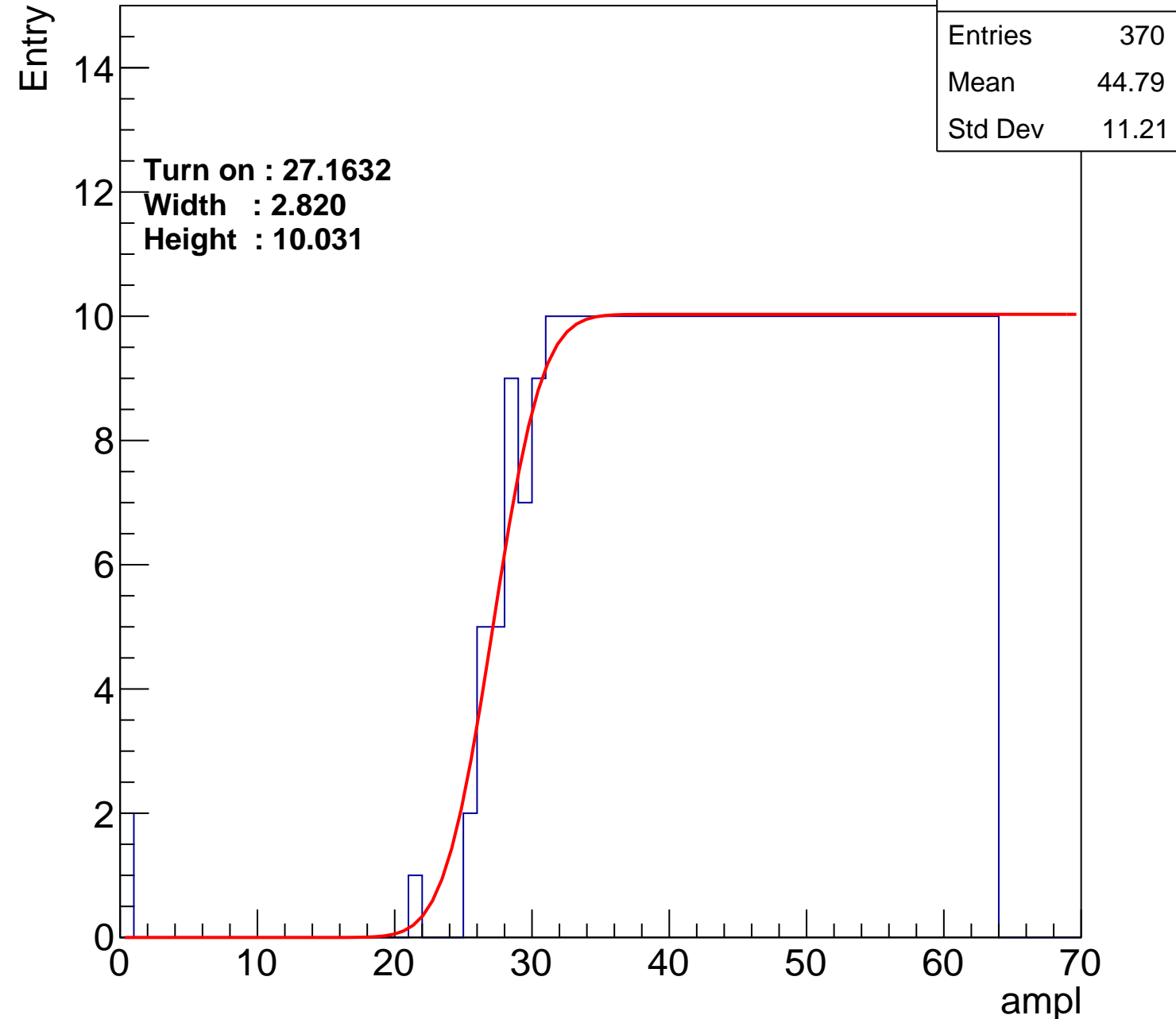
Width : 2.820

Height : 10.031

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch64

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	377
Mean	44.14
Std Dev	12.15

Turn on : 26.5836

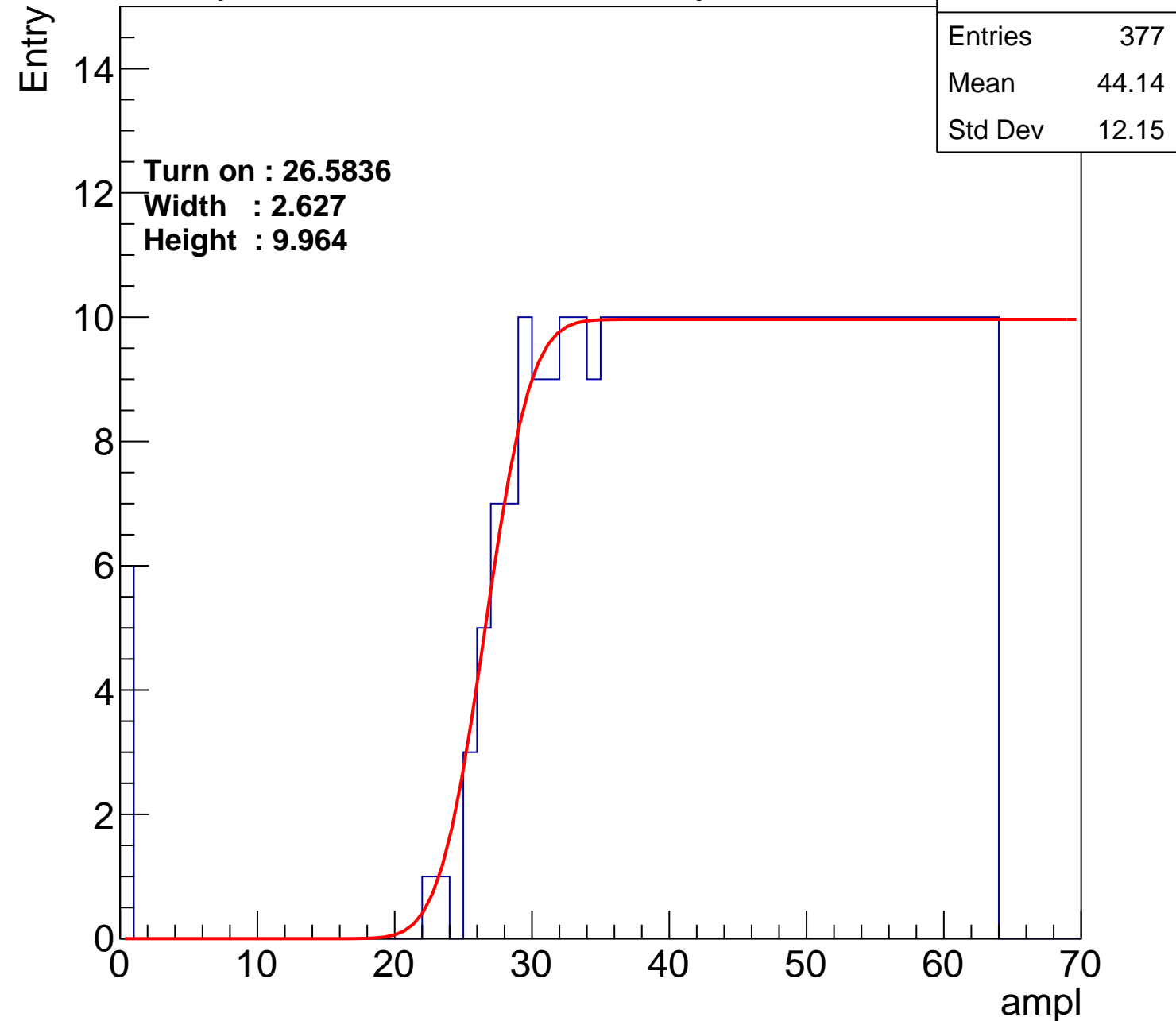
Width : 2.627

Height : 9.964

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch65

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	366
Mean	44.8
Std Dev	11.56

Turn on : 27.4521

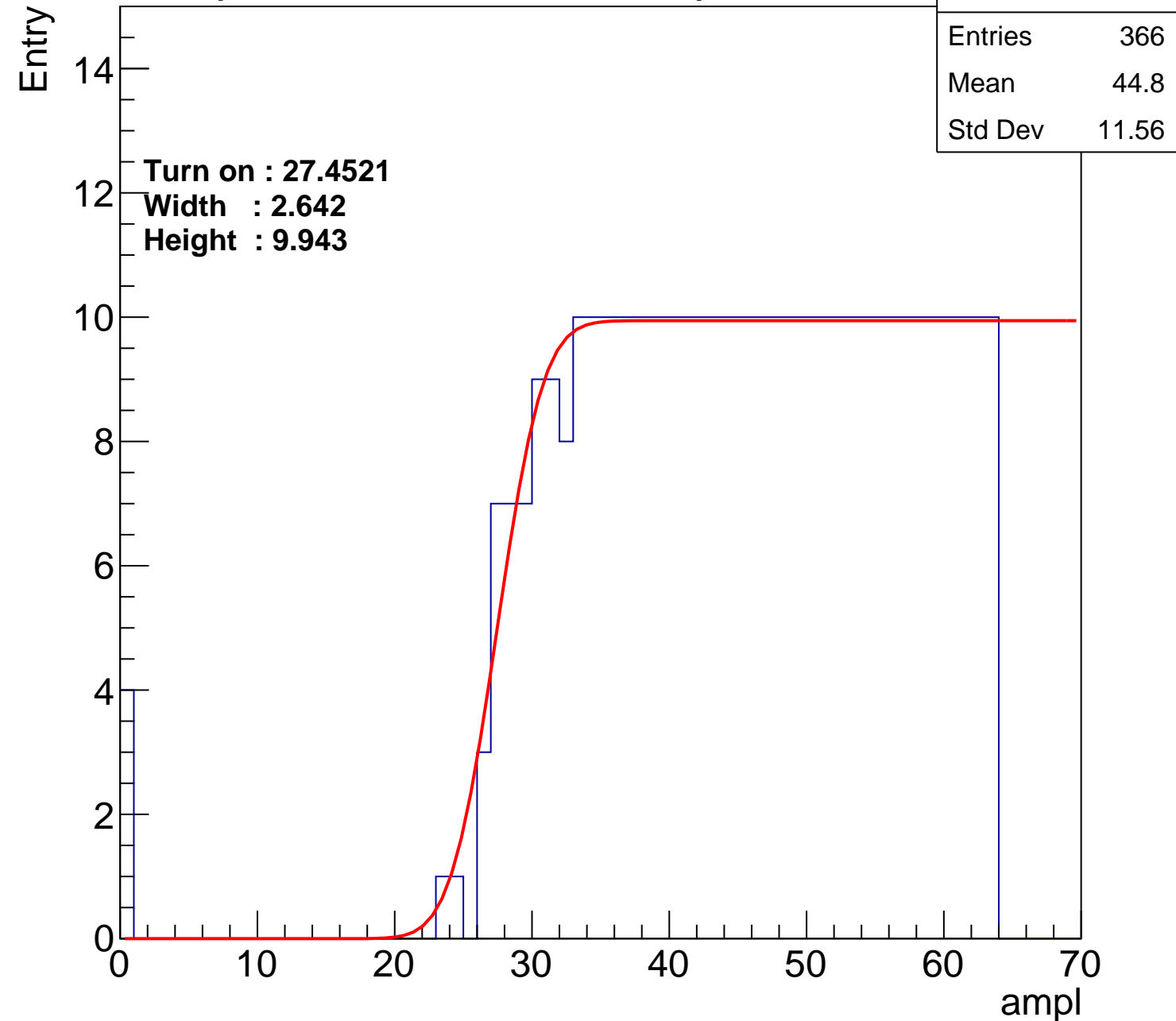
Width : 2.642

Height : 9.943

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch66

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	384
Mean	43.86
Std Dev	12.15

**Turn on : 26.8103**

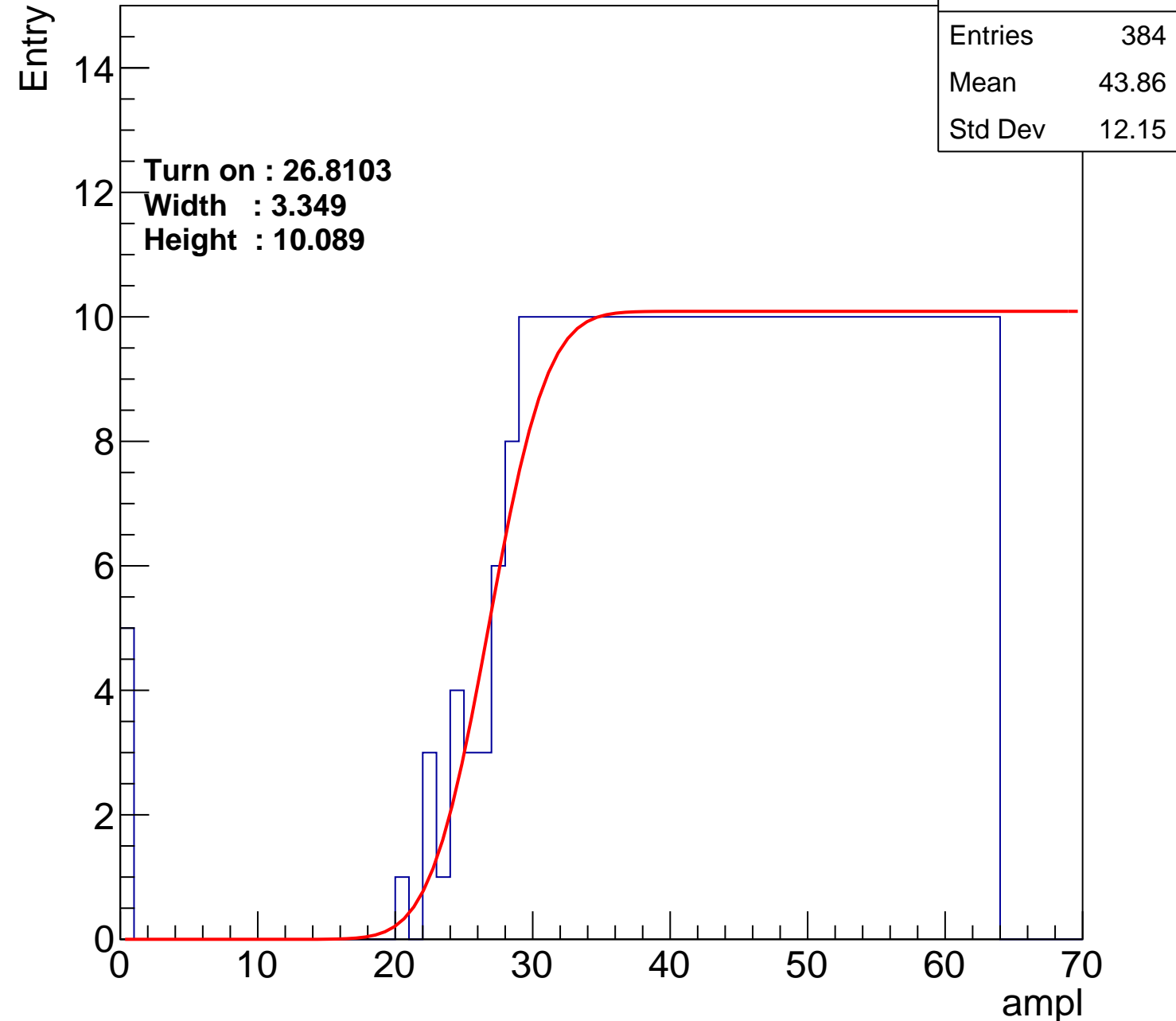
**Width : 3.349**

**Height : 10.089**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch67

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	381
Mean	44.15
Std Dev	11.71

**Turn on : 26.1909**

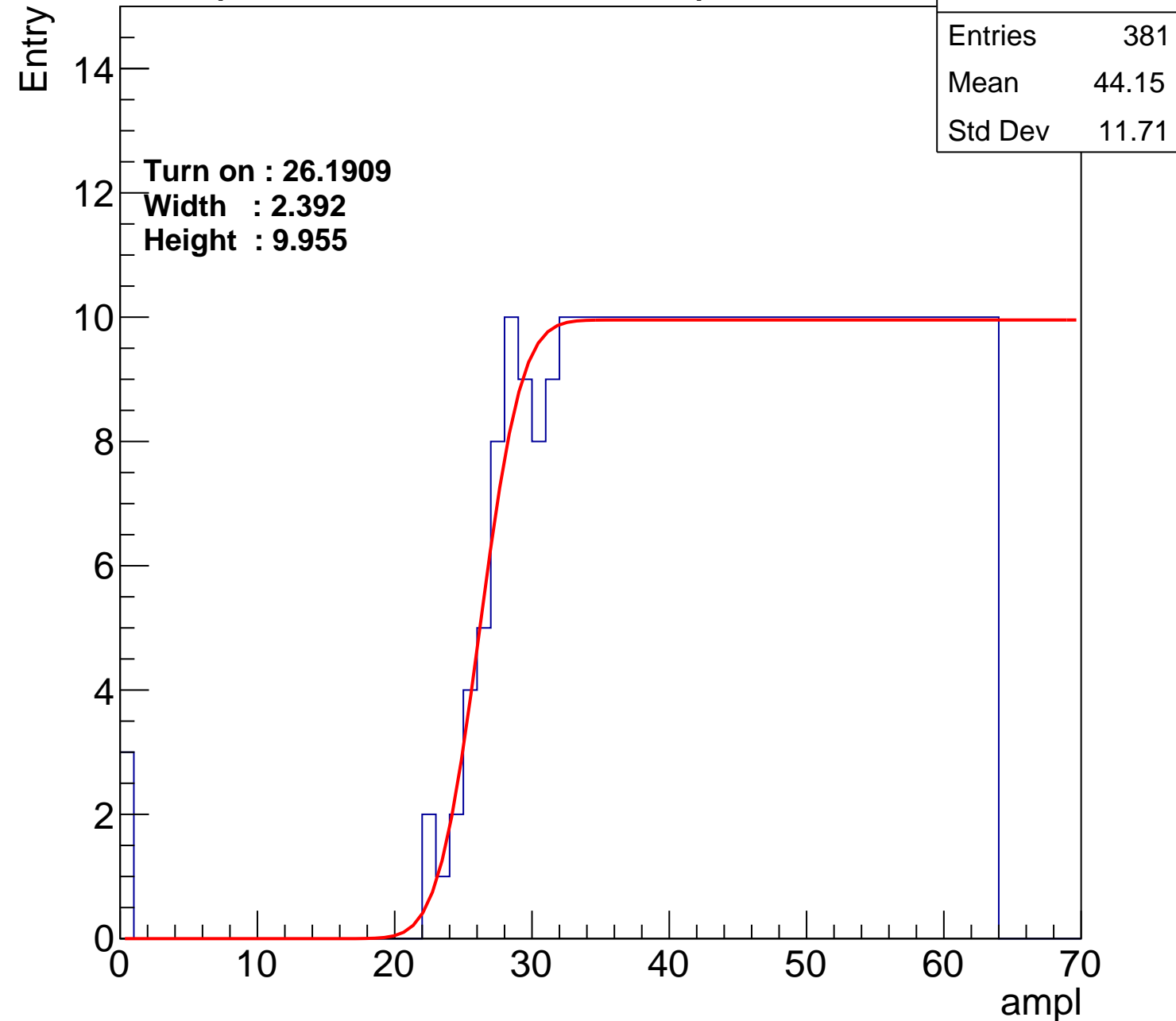
**Width : 2.392**

**Height : 9.955**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch68

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	361
Mean	45.07
Std Dev	11.32

**Turn on : 28.6559**

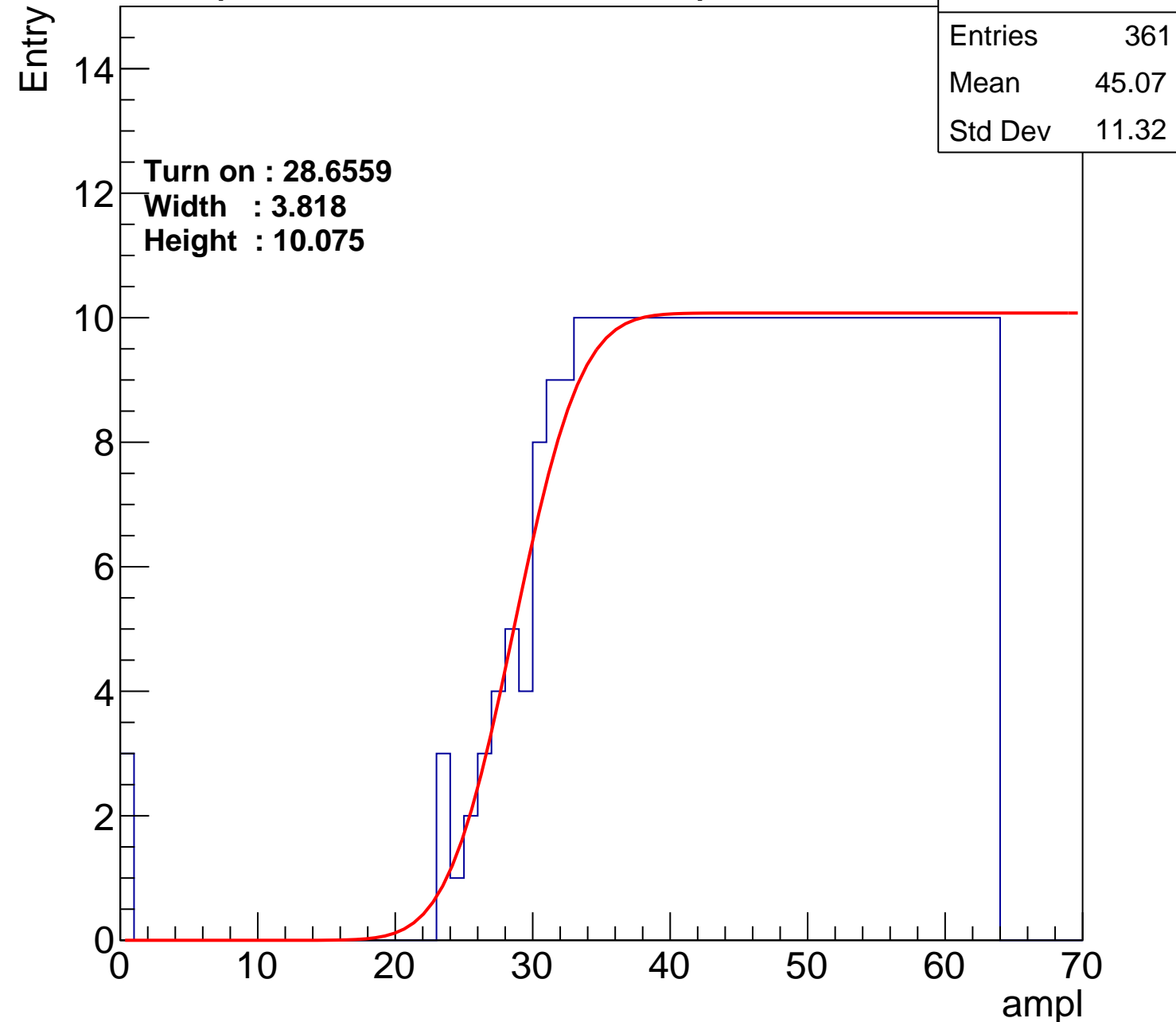
**Width : 3.818**

**Height : 10.075**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch69

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	373
Mean	44.63
Std Dev	11.24

Turn on : 27.8546

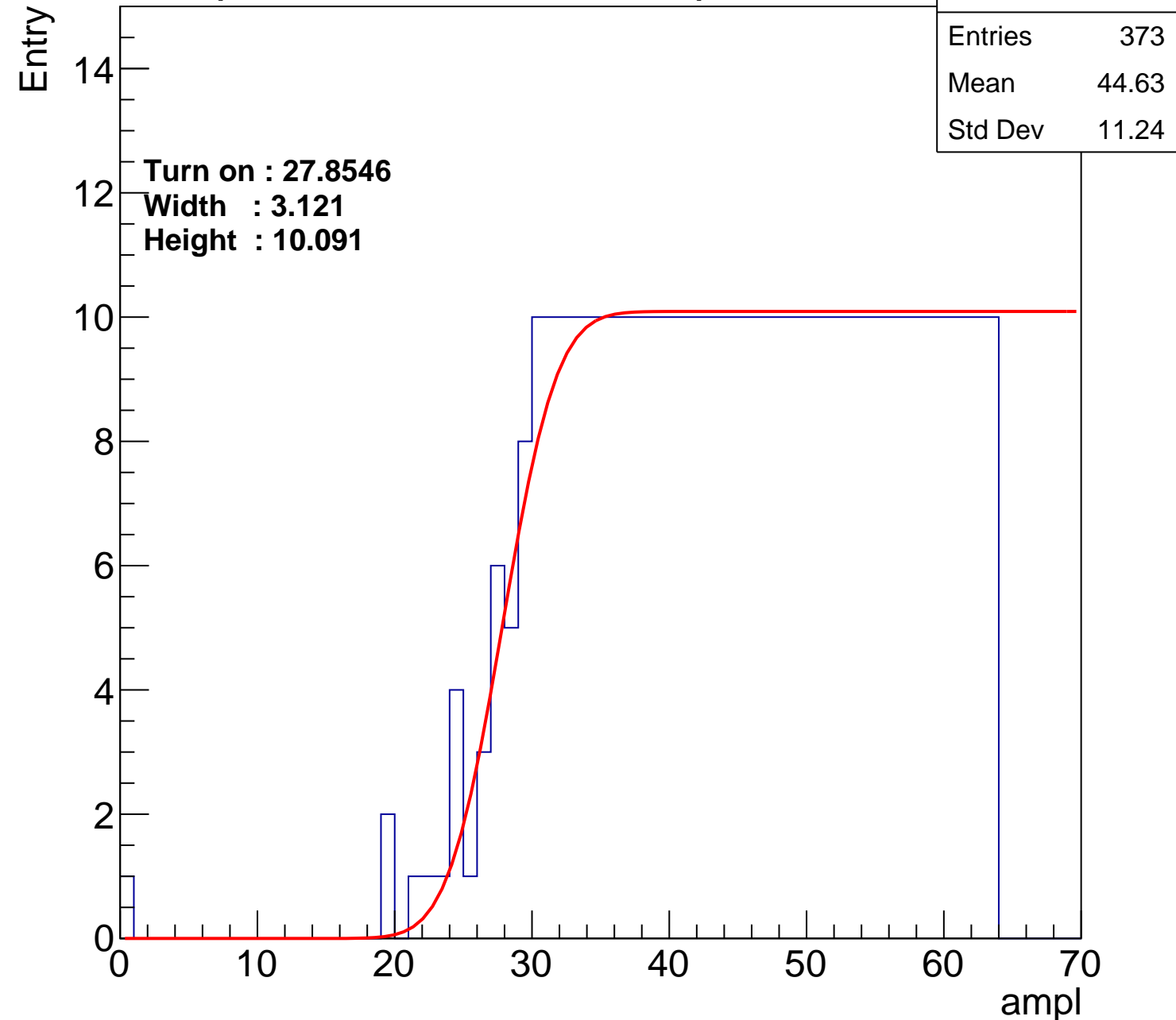
Width : 3.121

Height : 10.091

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch70

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	398
Mean	43.21
Std Dev	12.35

Turn on : 24.8077

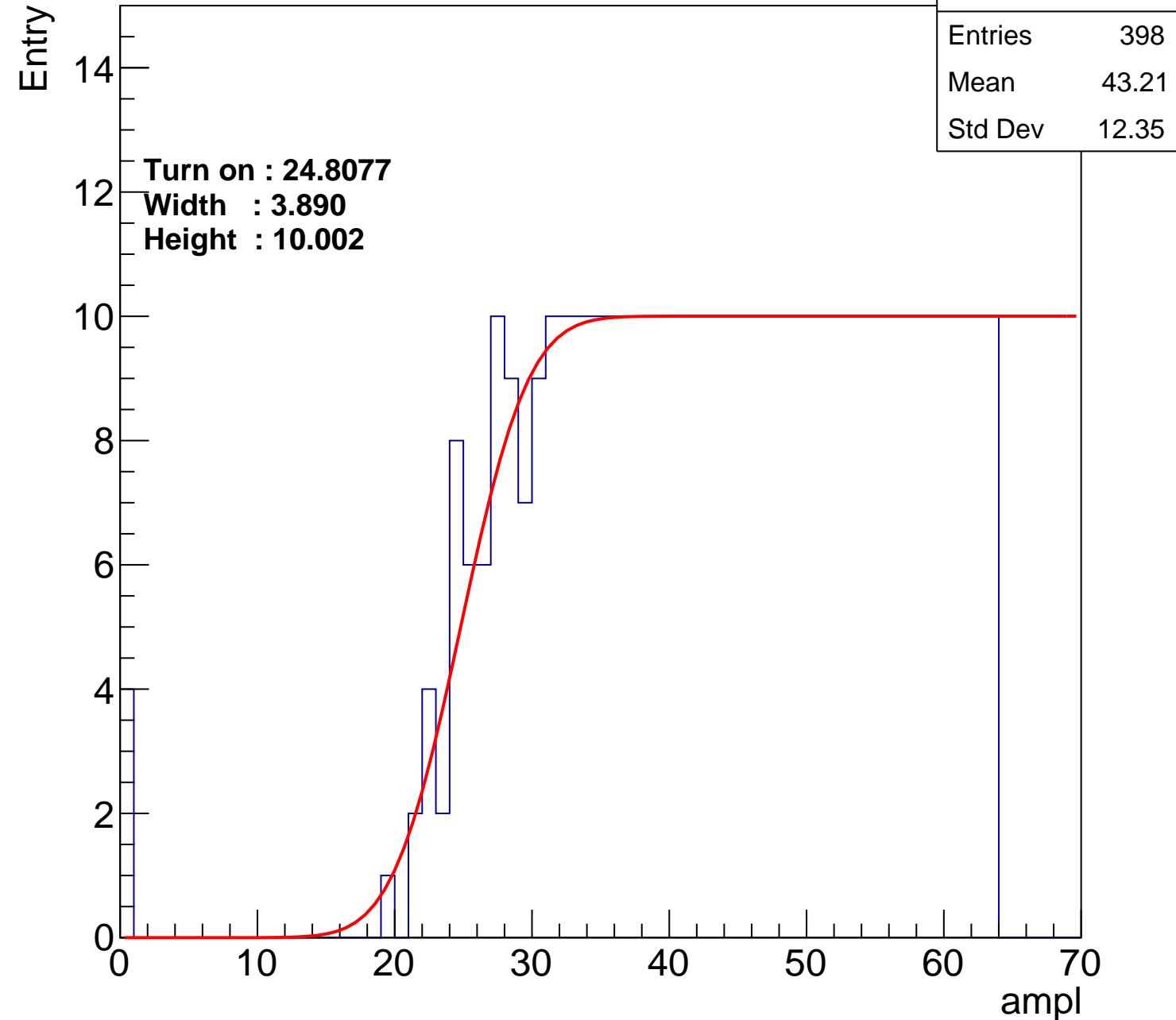
Width : 3.890

Height : 10.002

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U7-ch71

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	365
Mean	44.89
Std Dev	11.49

Turn on : 28.9196

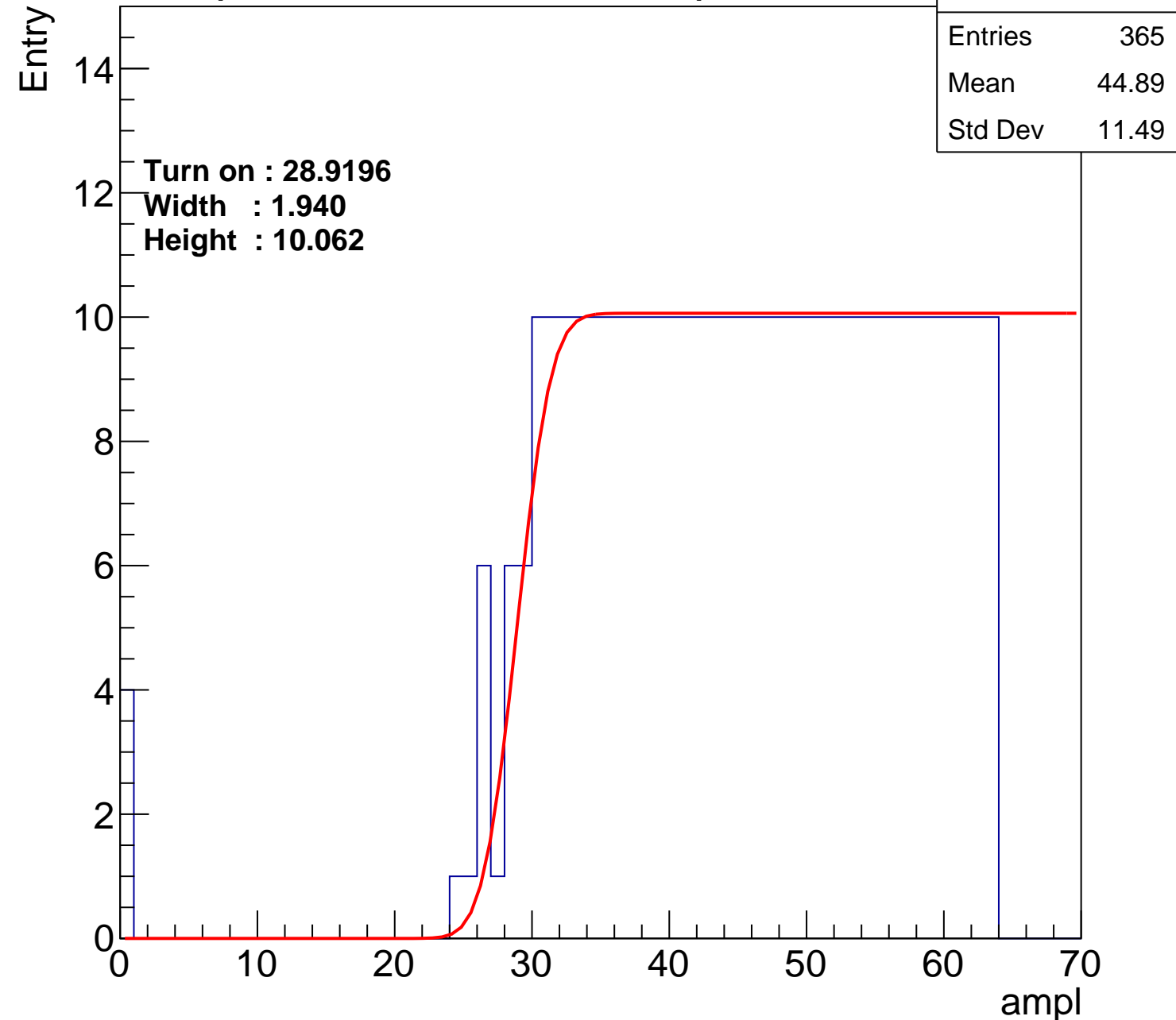
Width : 1.940

Height : 10.062

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch72

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	375
Mean	44.3
Std Dev	11.94

Turn on : 27.1158

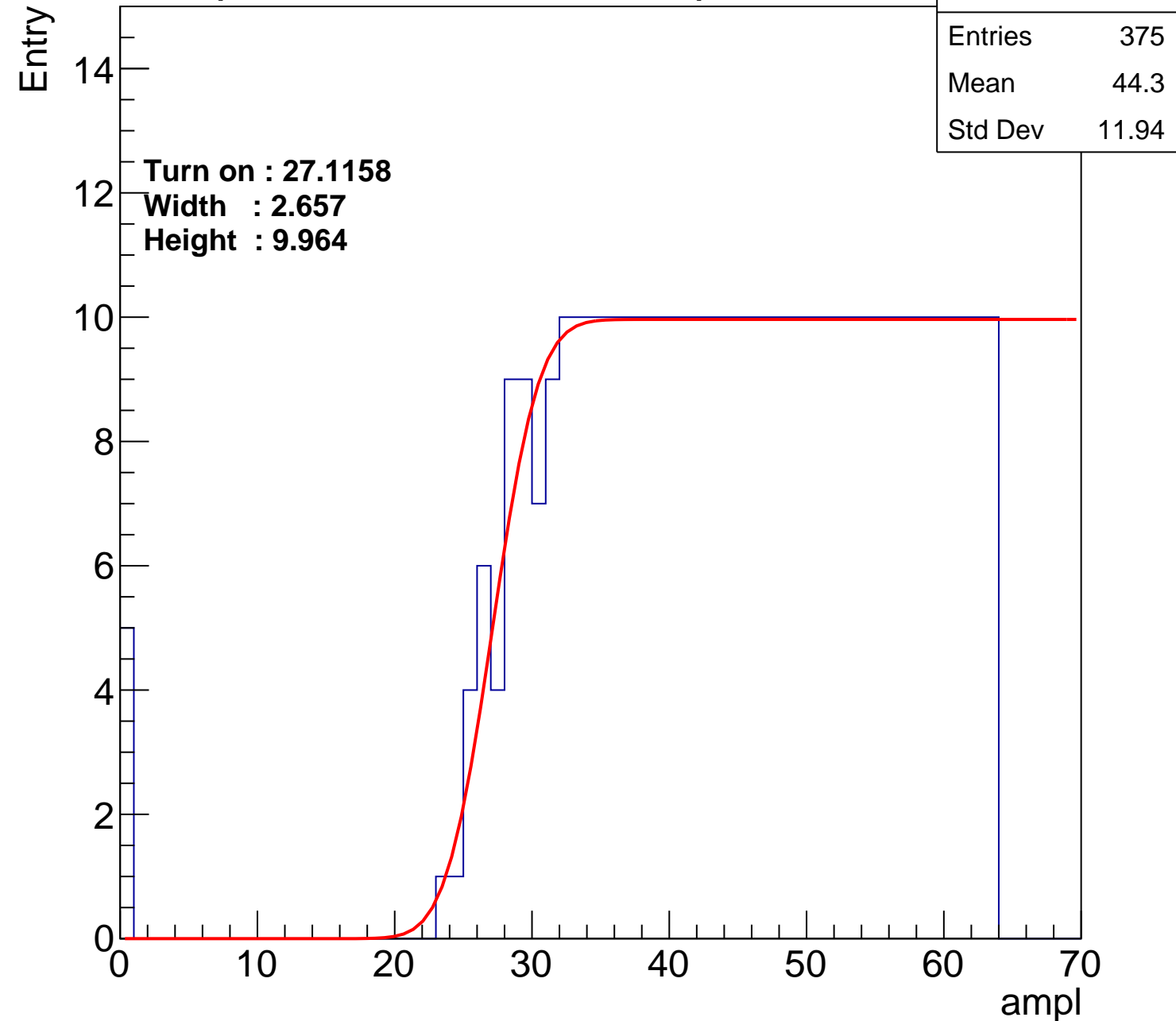
Width : 2.657

Height : 9.964

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch73

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	371
Mean	44.62
Std Dev	11.49

Turn on : 27.4258

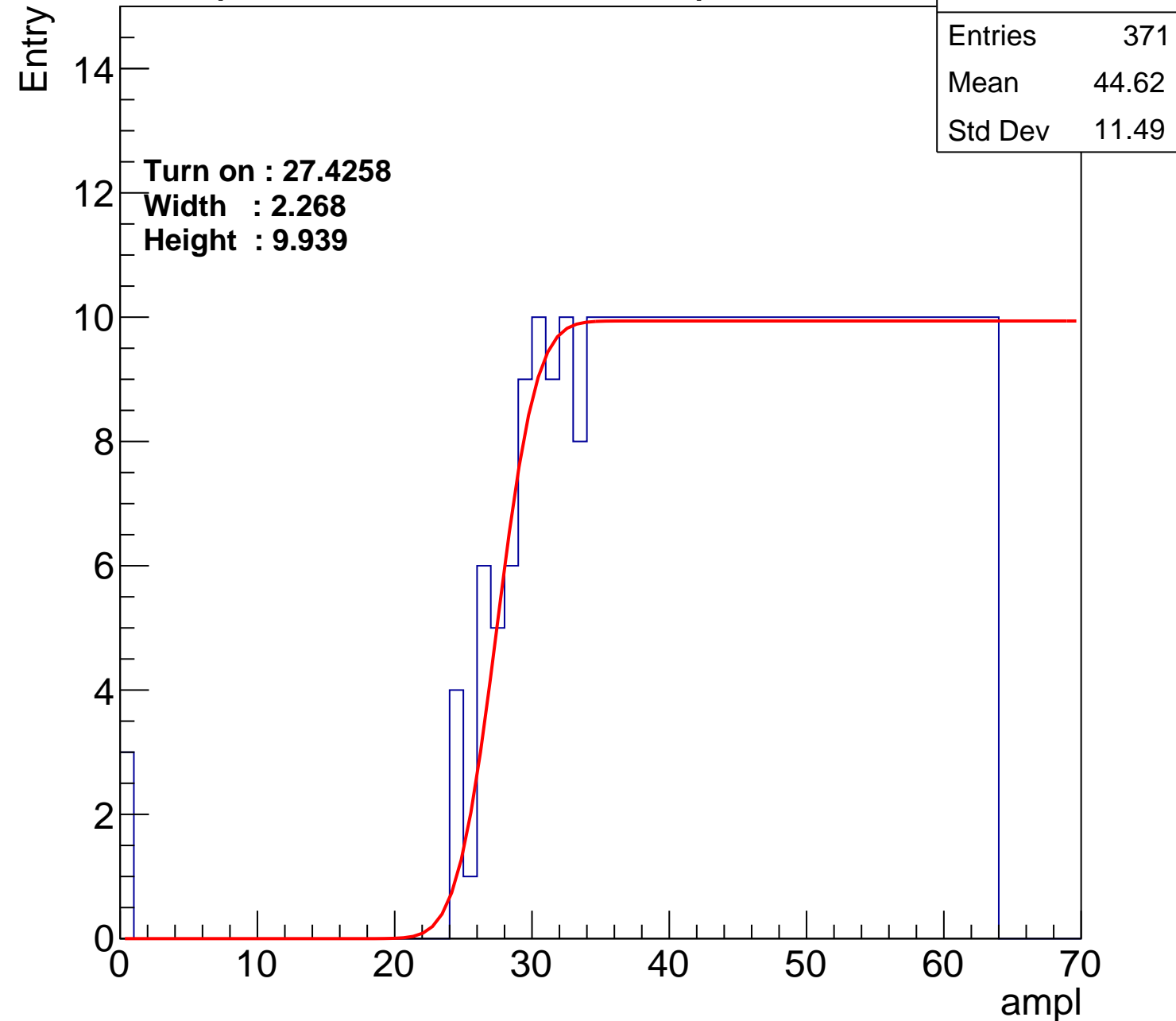
Width : 2.268

Height : 9.939

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch74

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	390
Mean	43.66
Std Dev	12.08

Turn on : 25.3788

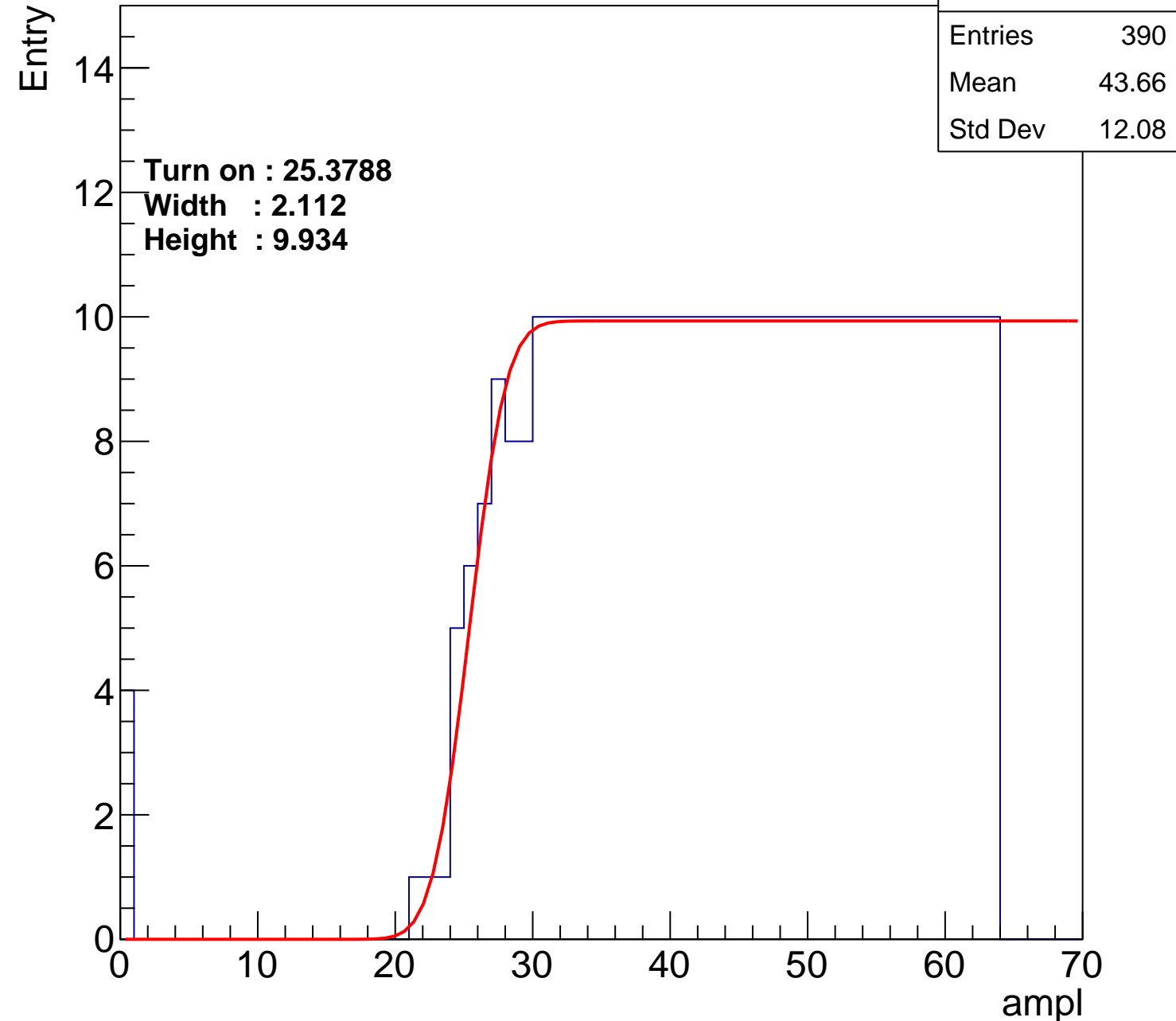
Width : 2.112

Height : 9.934

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch75

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	356
Mean	45.32
Std Dev	11.2

Turn on : 28.7290

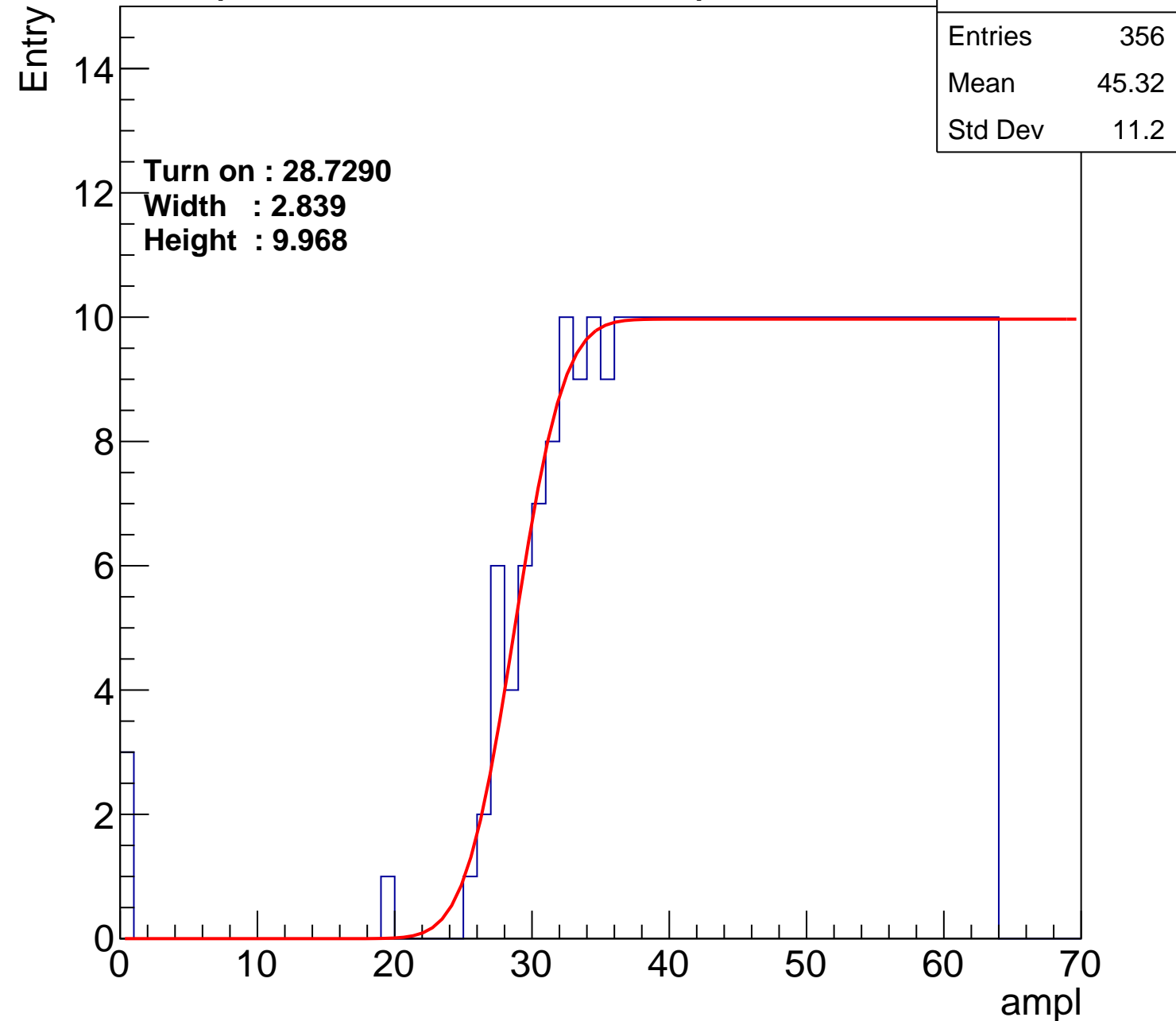
Width : 2.839

Height : 9.968

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch76

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	382
Mean	43.97
Std Dev	12.09

Turn on : 26.1655

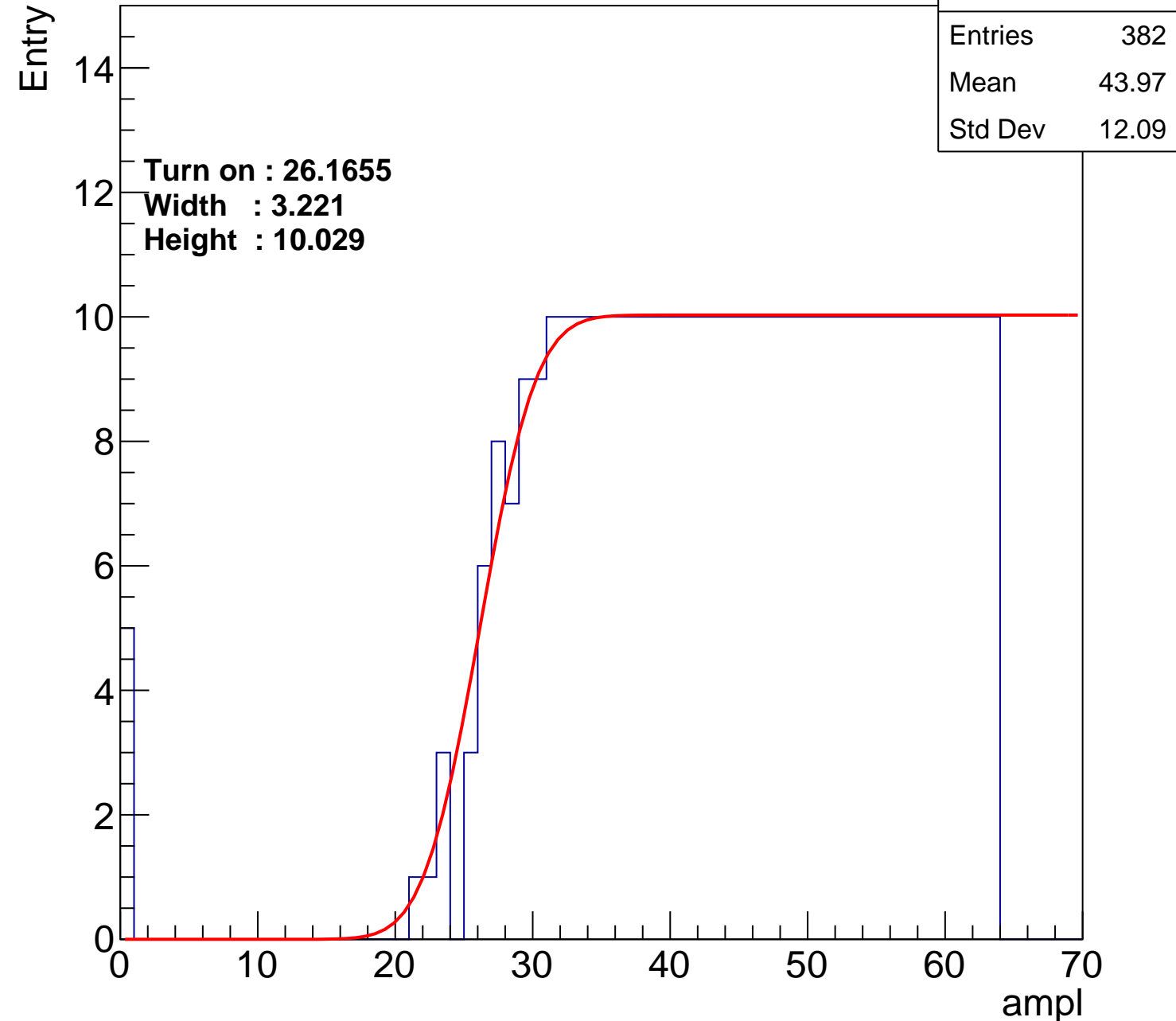
Width : 3.221

Height : 10.029

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch77

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	361
Mean	45.14
Std Dev	11.22

Turn on : 28.2361

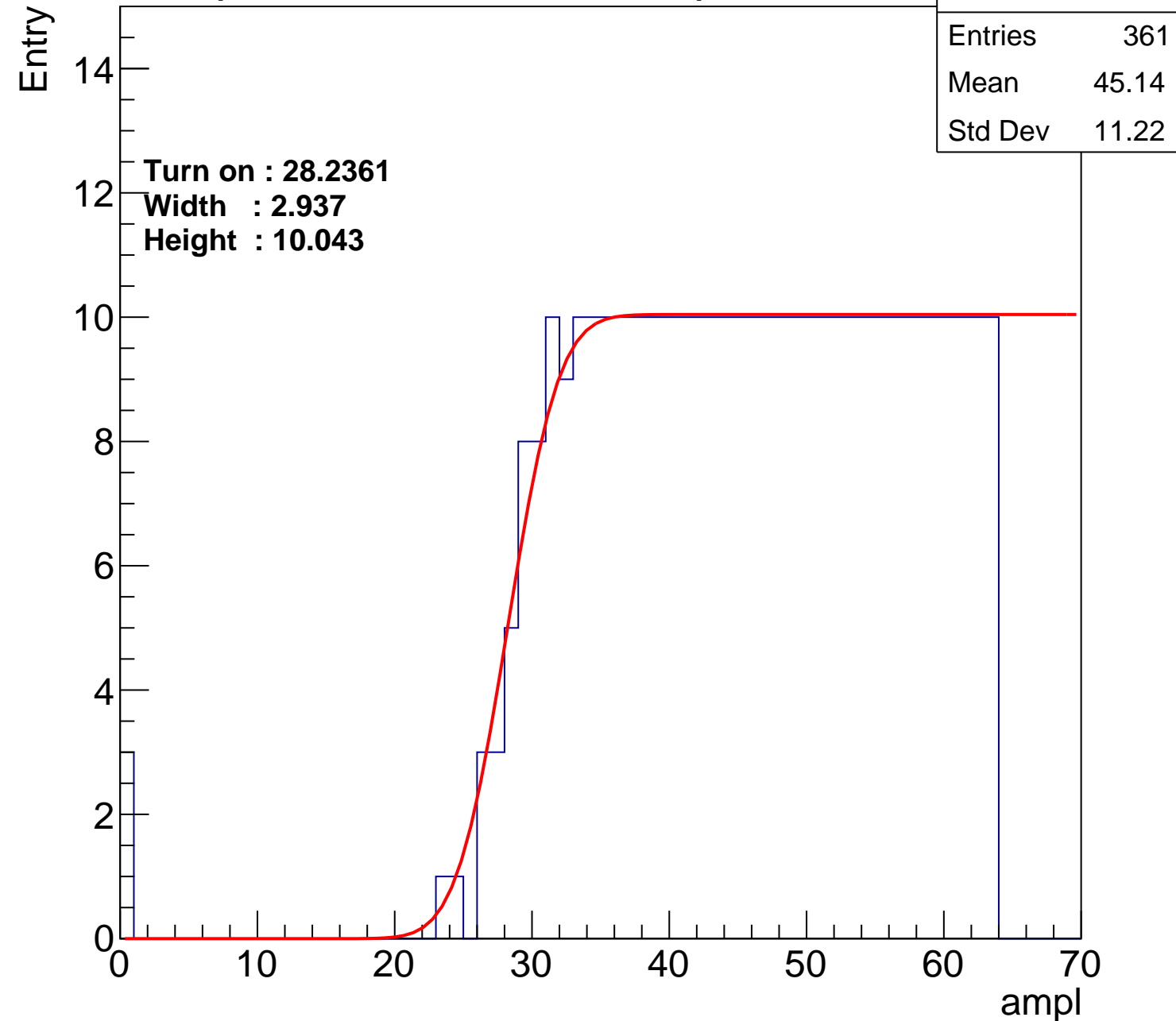
Width : 2.937

Height : 10.043

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch78

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	367
Mean	44.9
Std Dev	11.19

Turn on : 27.2682

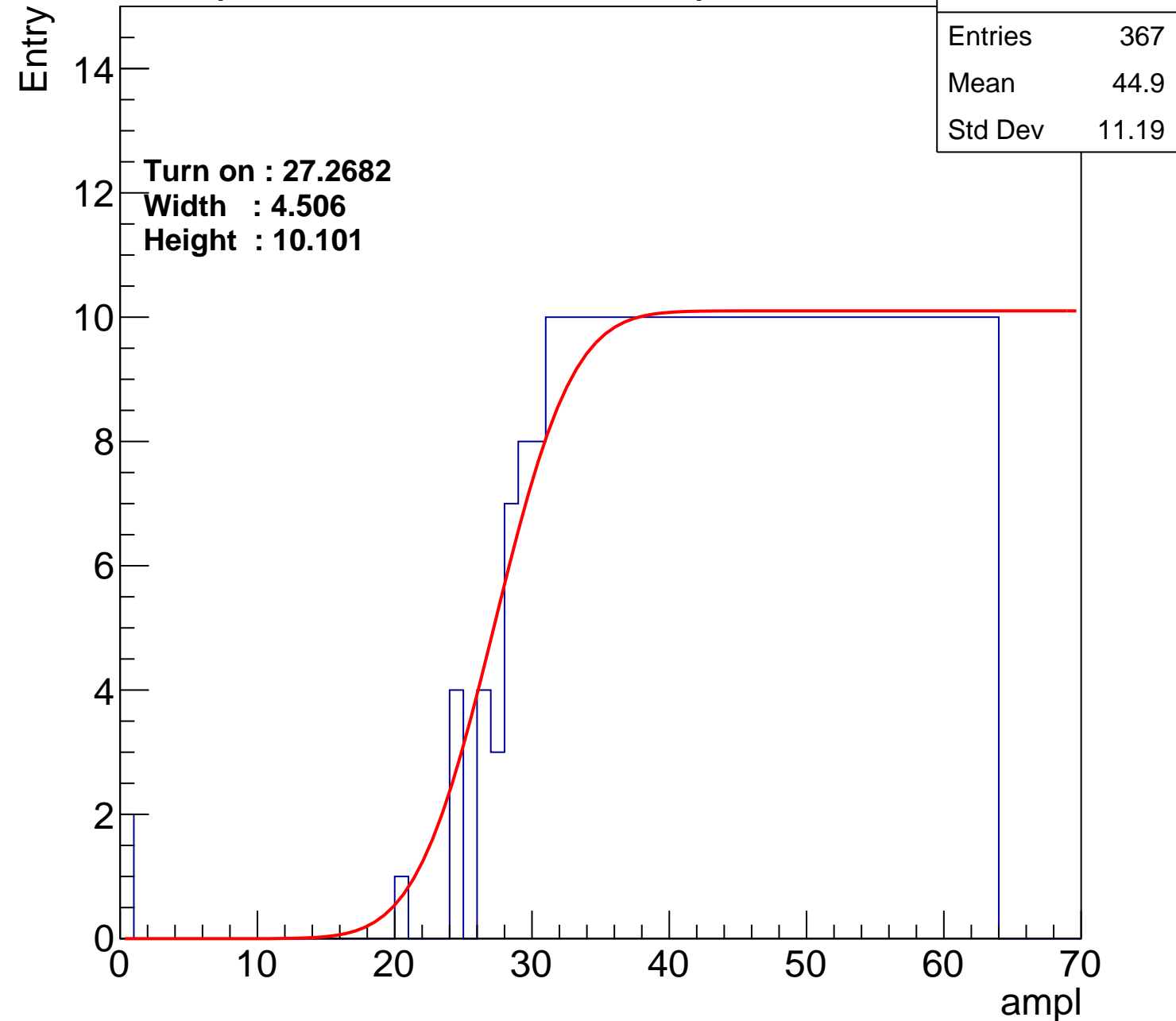
Width : 4.506

Height : 10.101

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U7-ch79

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	394
Mean	43.38
Std Dev	12.37

Turn on : 25.0598

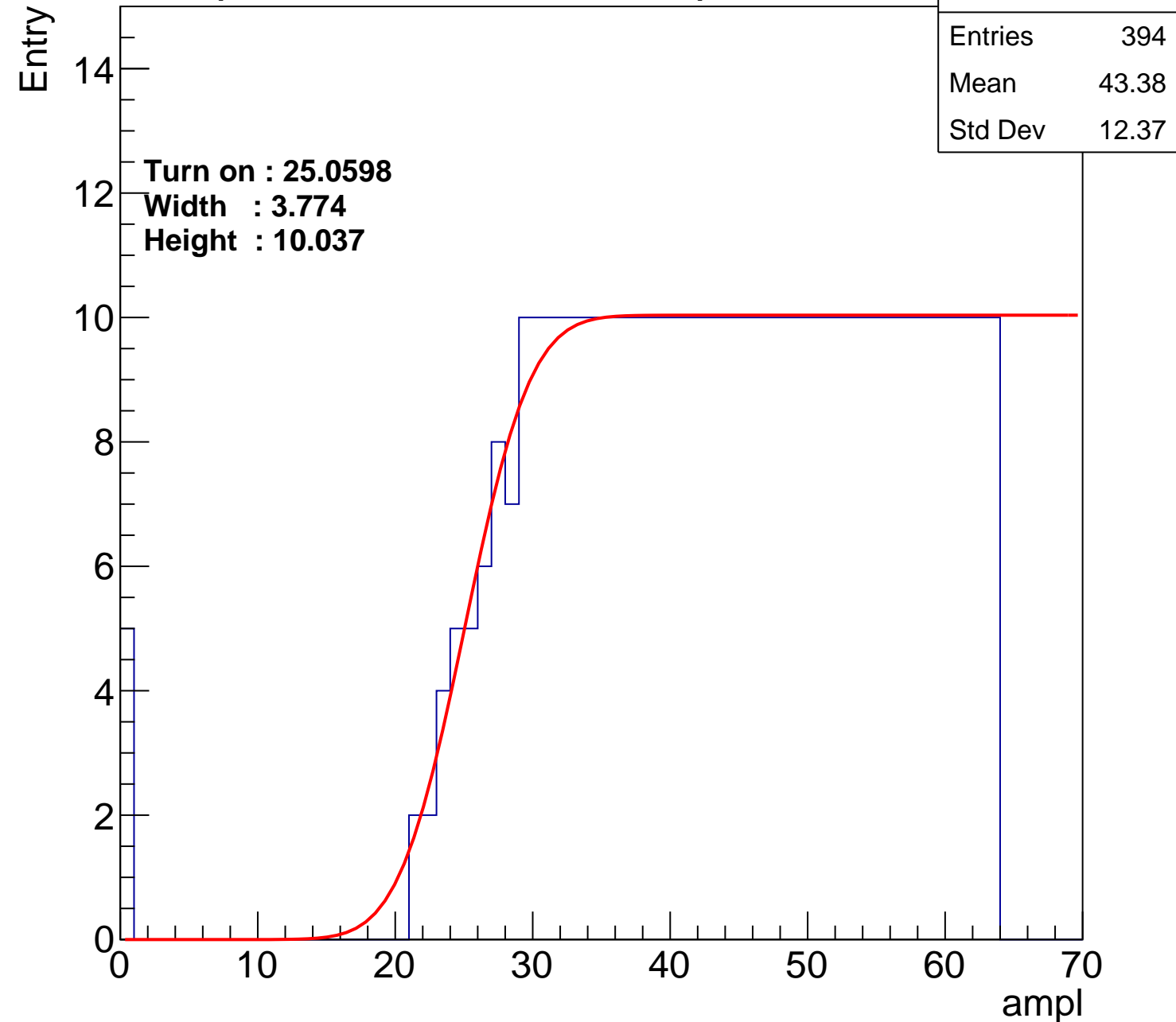
Width : 3.774

Height : 10.037

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch80

calib\_packv5\_042523\_0143.root, FC#0, port D2

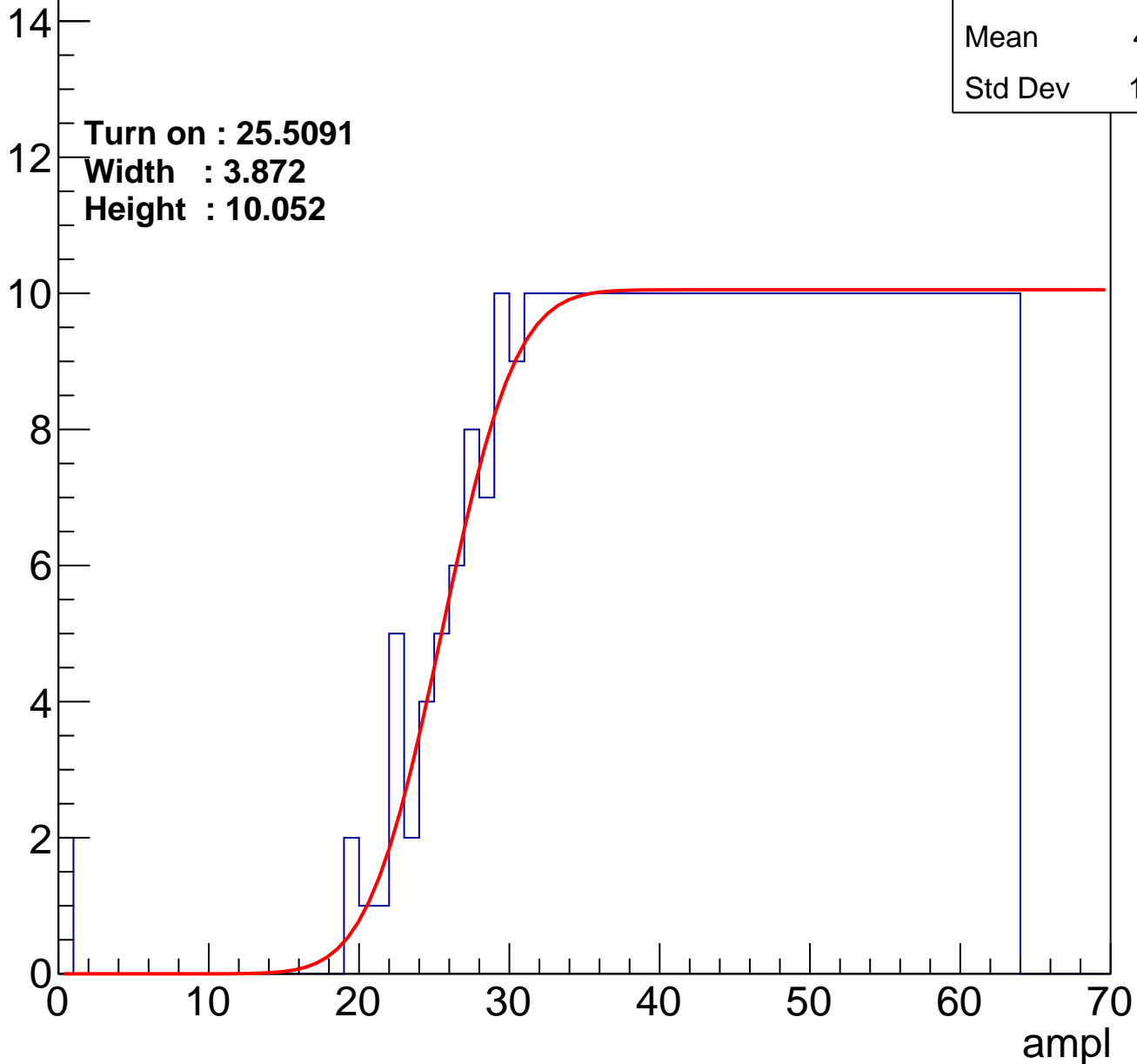
Entries	392
Mean	43.61
Std Dev	11.93

Turn on : 25.5091

Width : 3.872

Height : 10.052

Entry



# B1L101S, U7-ch81

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	384
Mean	43.95
Std Dev	11.88

**Turn on : 26.4155**

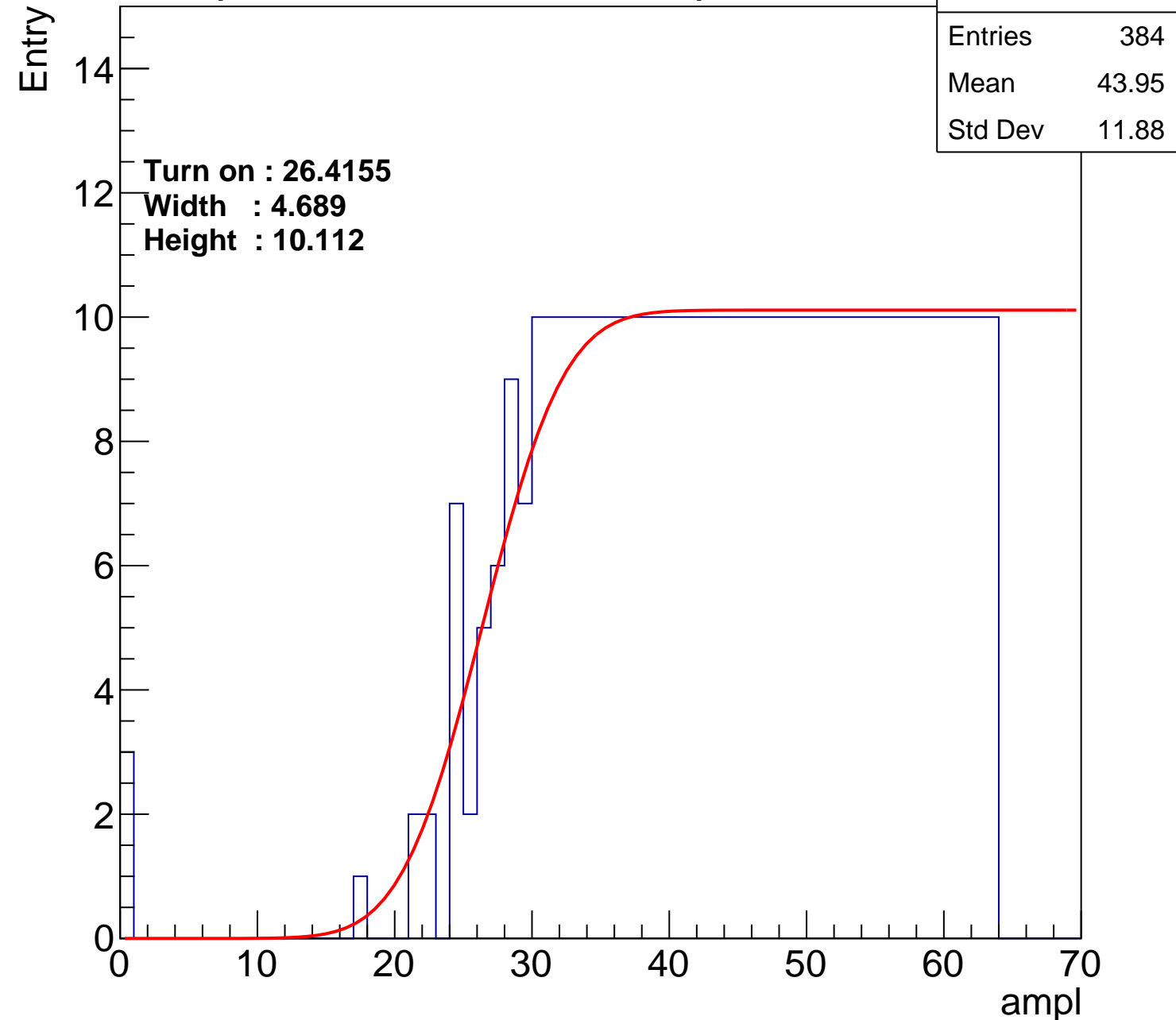
**Width : 4.689**

**Height : 10.112**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch82

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	379
Mean	44.26
Std Dev	11.65

Turn on : 26.5774

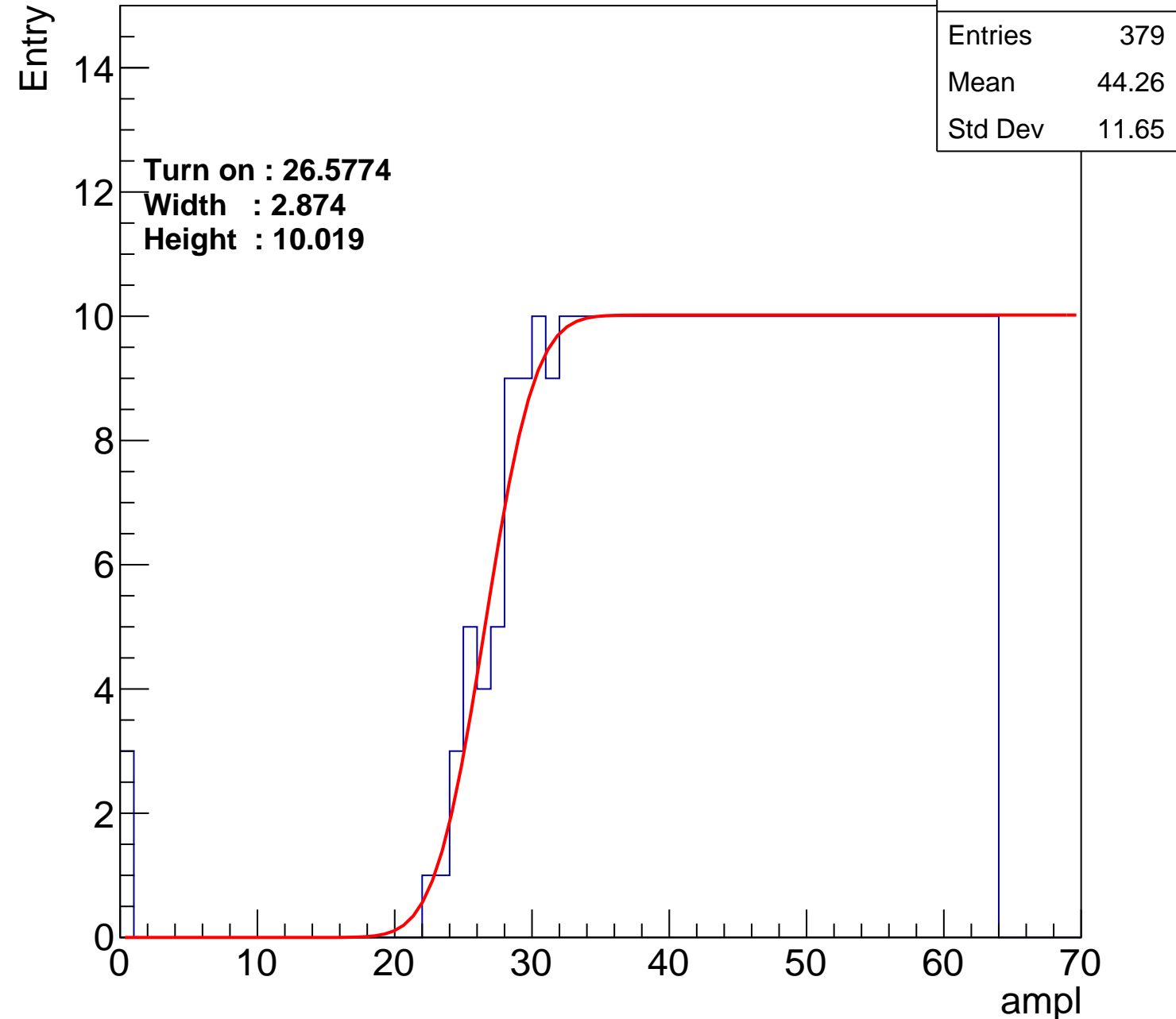
Width : 2.874

Height : 10.019

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch83

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	379
Mean	44.26
Std Dev	11.66

Turn on : 26.4986

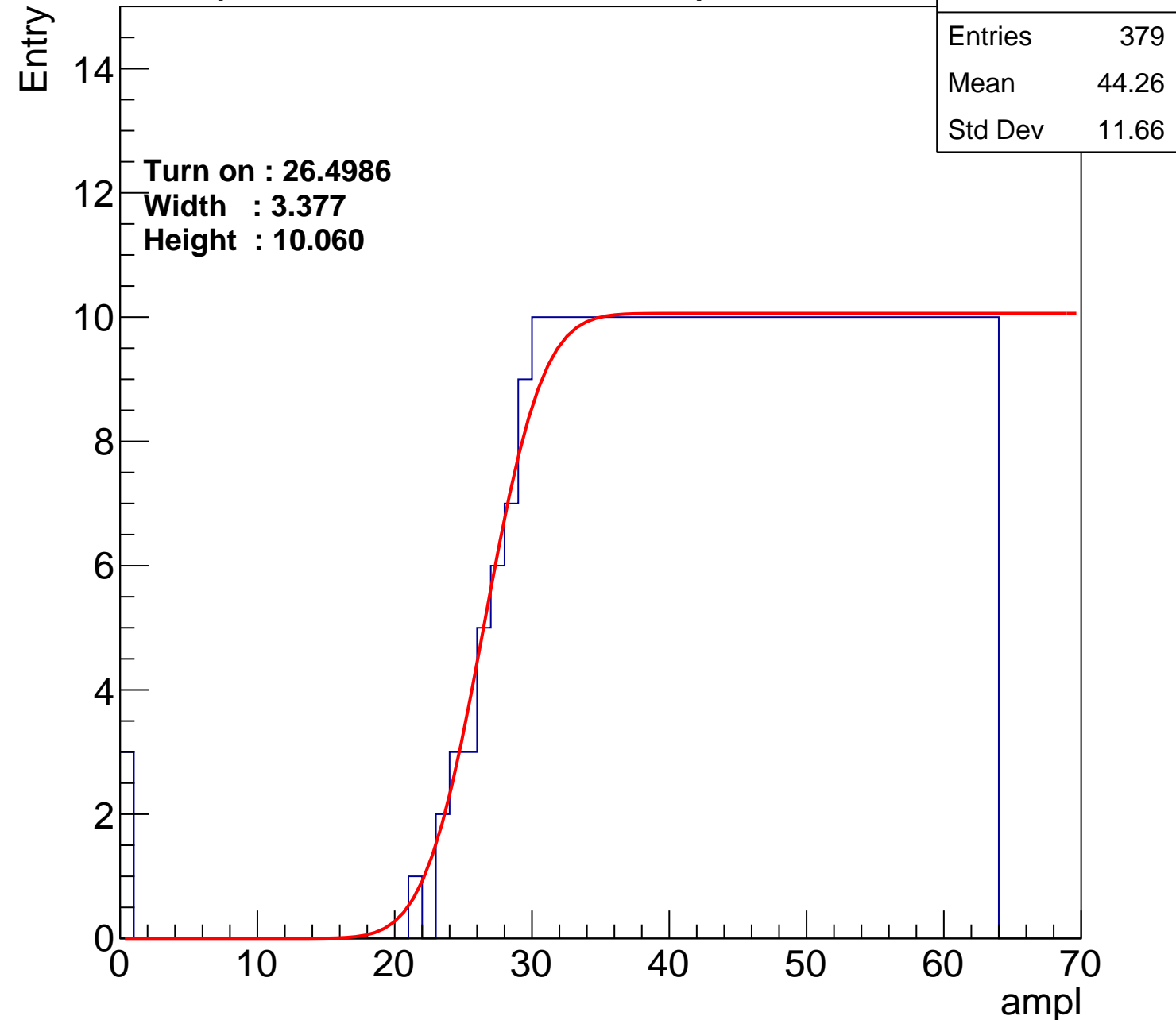
Width : 3.377

Height : 10.060

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch84

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	371
Mean	44.47
Std Dev	11.88

**Turn on : 27.2557**

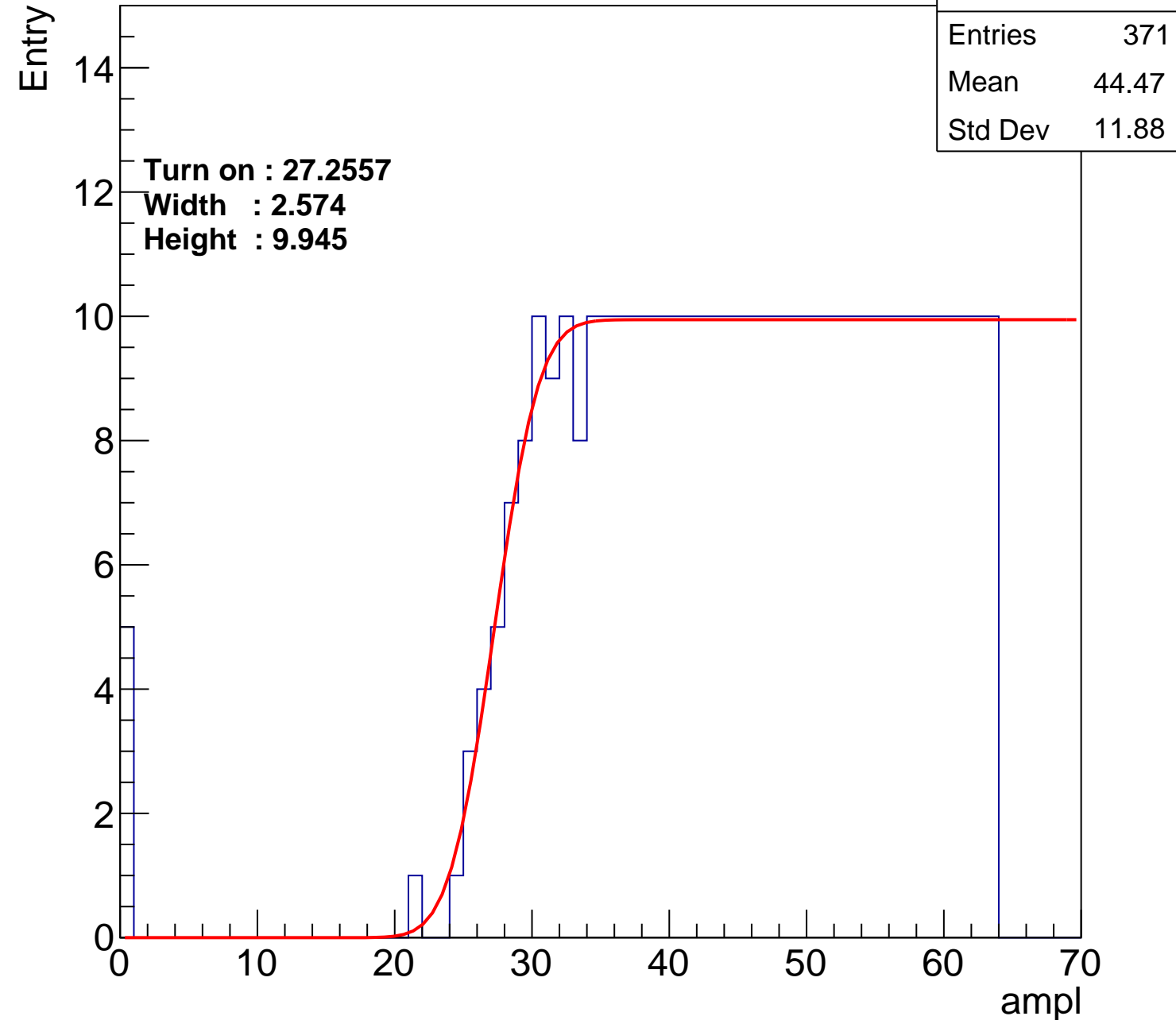
**Width : 2.574**

**Height : 9.945**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch85

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	364
Mean	45.01
Std Dev	11.17

Turn on : 28.0576

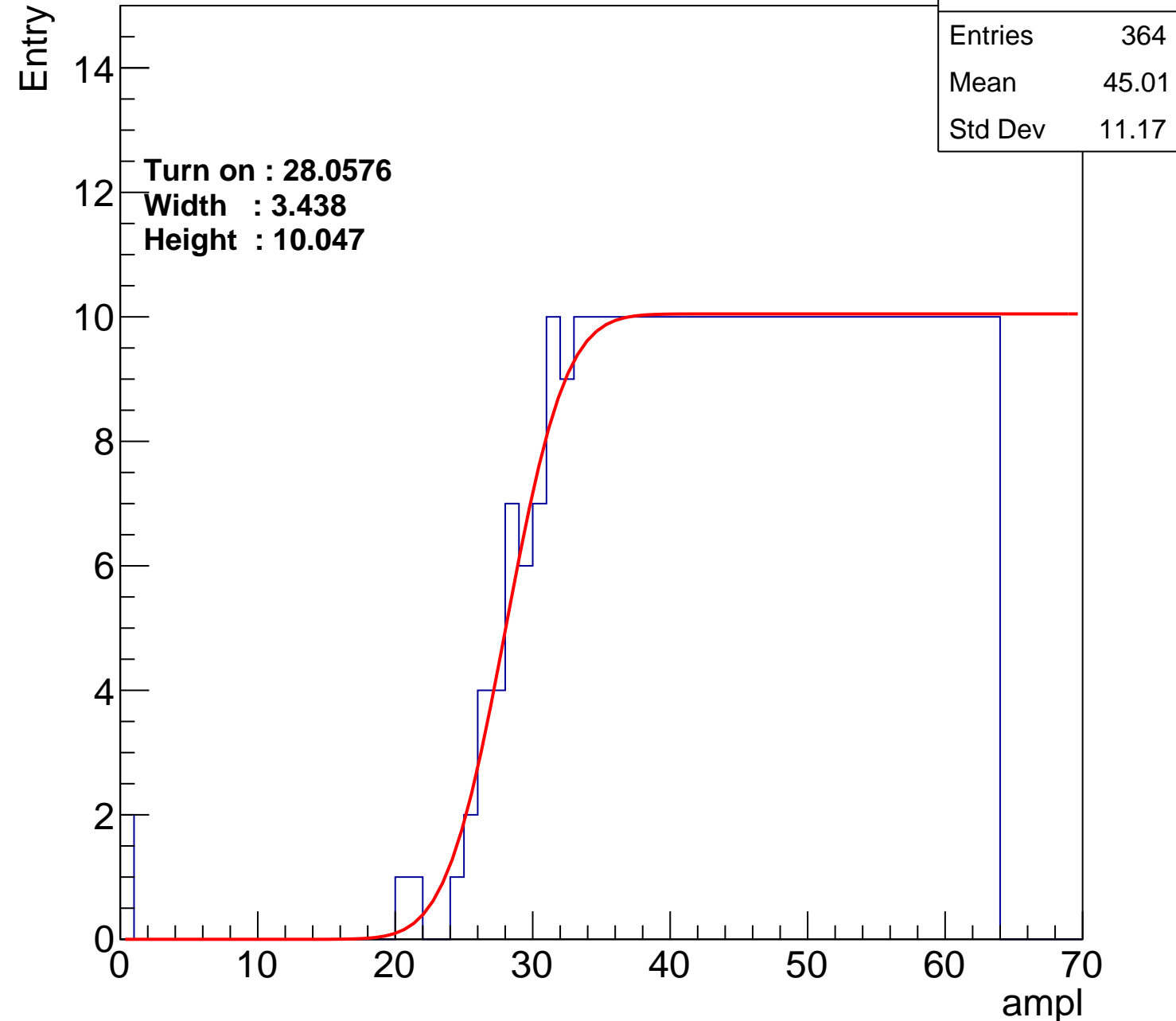
Width : 3.438

Height : 10.047

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch86

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	389
Mean	43.68
Std Dev	12.1

Turn on : 25.7503

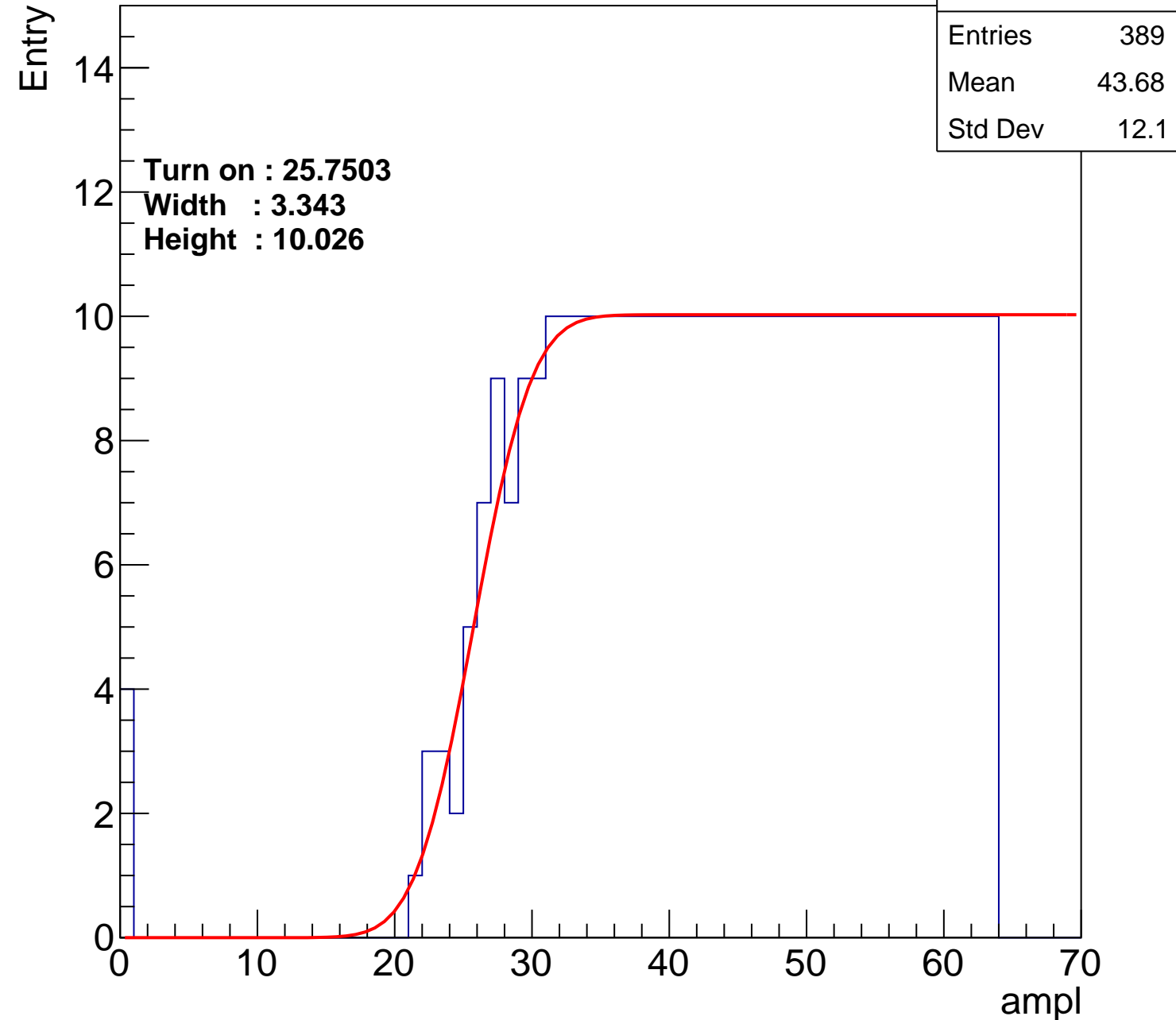
Width : 3.343

Height : 10.026

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U7-ch87

calib\_packv5\_042523\_0143.root, FC#0, port D2

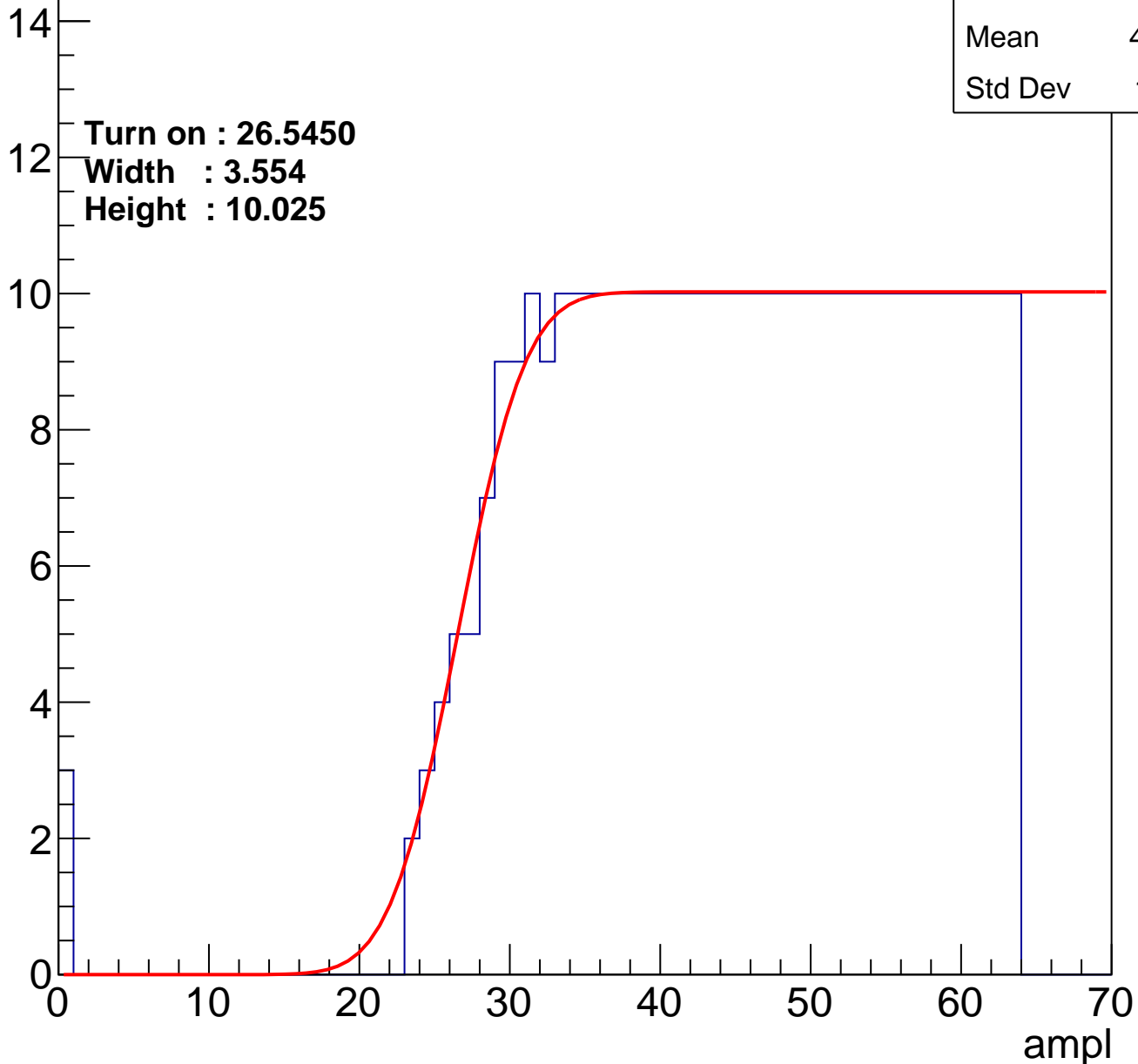
Entries	376
Mean	44.38
Std Dev	11.61

Turn on : 26.5450

Width : 3.554

Height : 10.025

Entry



# B1L101S, U7-ch88

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	398
Mean	43.38
Std Dev	11.98

Turn on : 24.6775

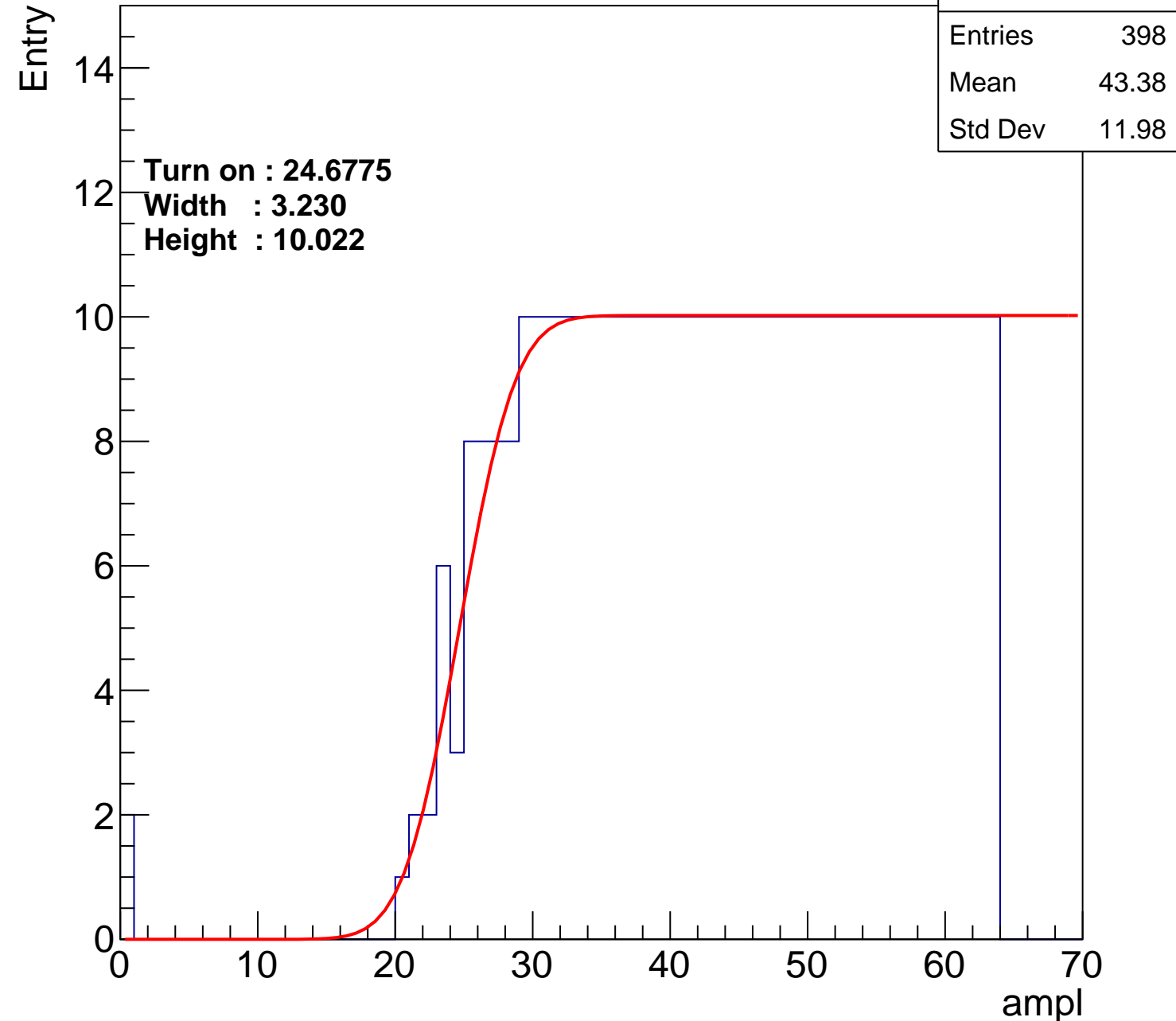
Width : 3.230

Height : 10.022

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch89

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	376
Mean	44.36
Std Dev	11.74

**Turn on : 27.0772**

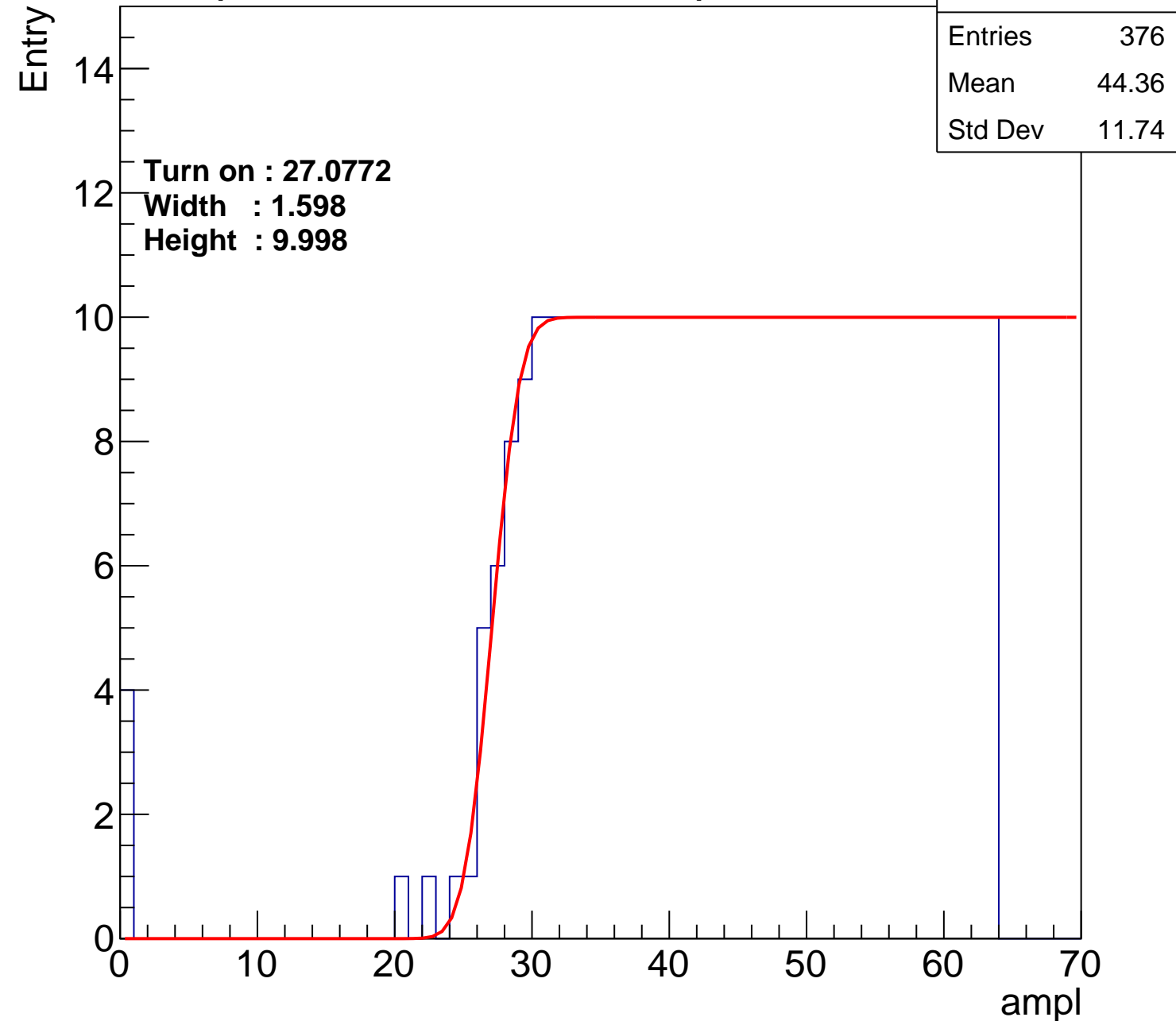
**Width : 1.598**

**Height : 9.998**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch90

calib\_packv5\_042523\_0143.root, FC#0, port D2

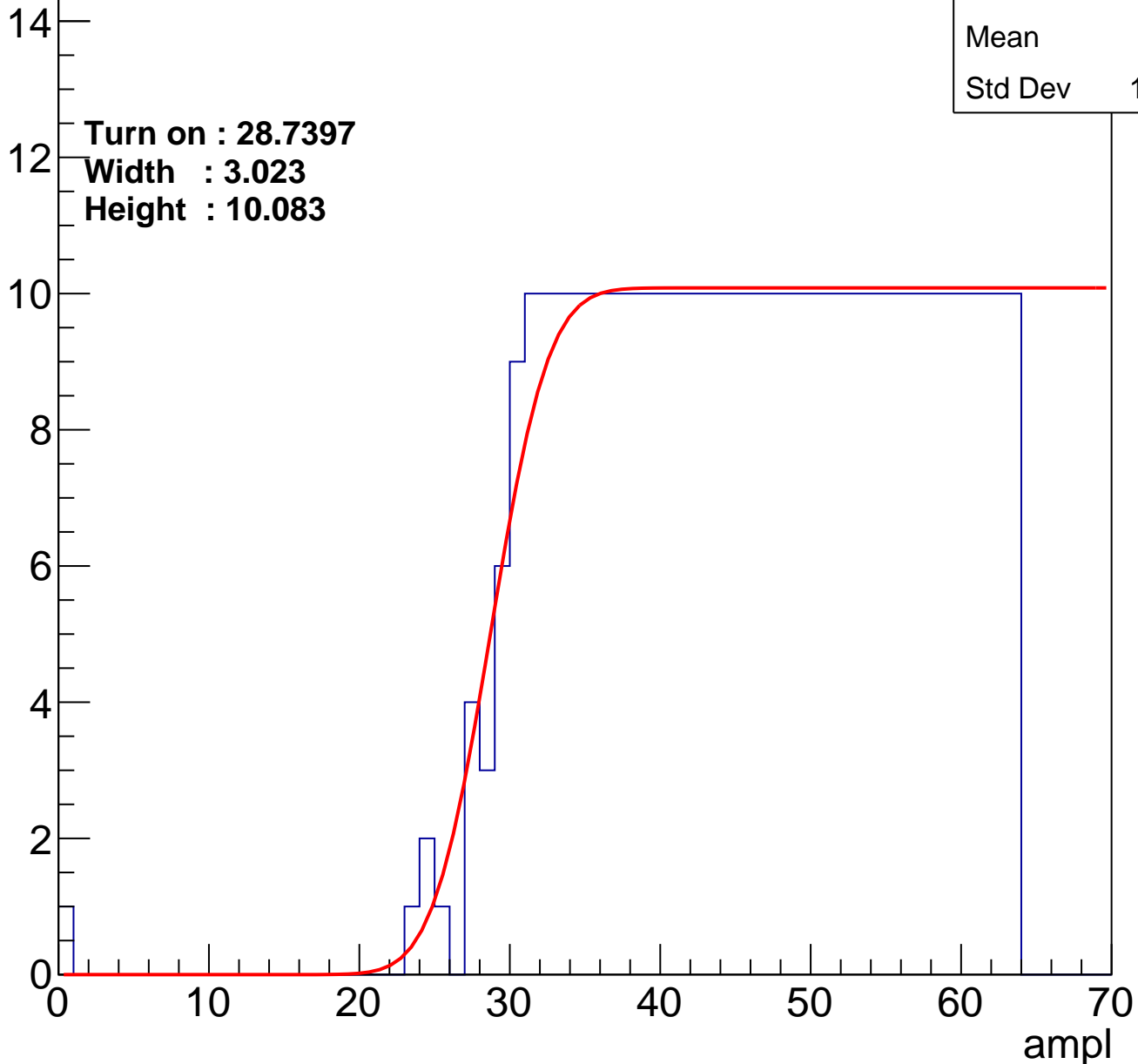
Entries	357
Mean	45.5
Std Dev	10.67

Turn on : 28.7397

Width : 3.023

Height : 10.083

Entry



# B1L101S, U7-ch91

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	384
Mean	43.99
Std Dev	11.8

Turn on : 25.9233

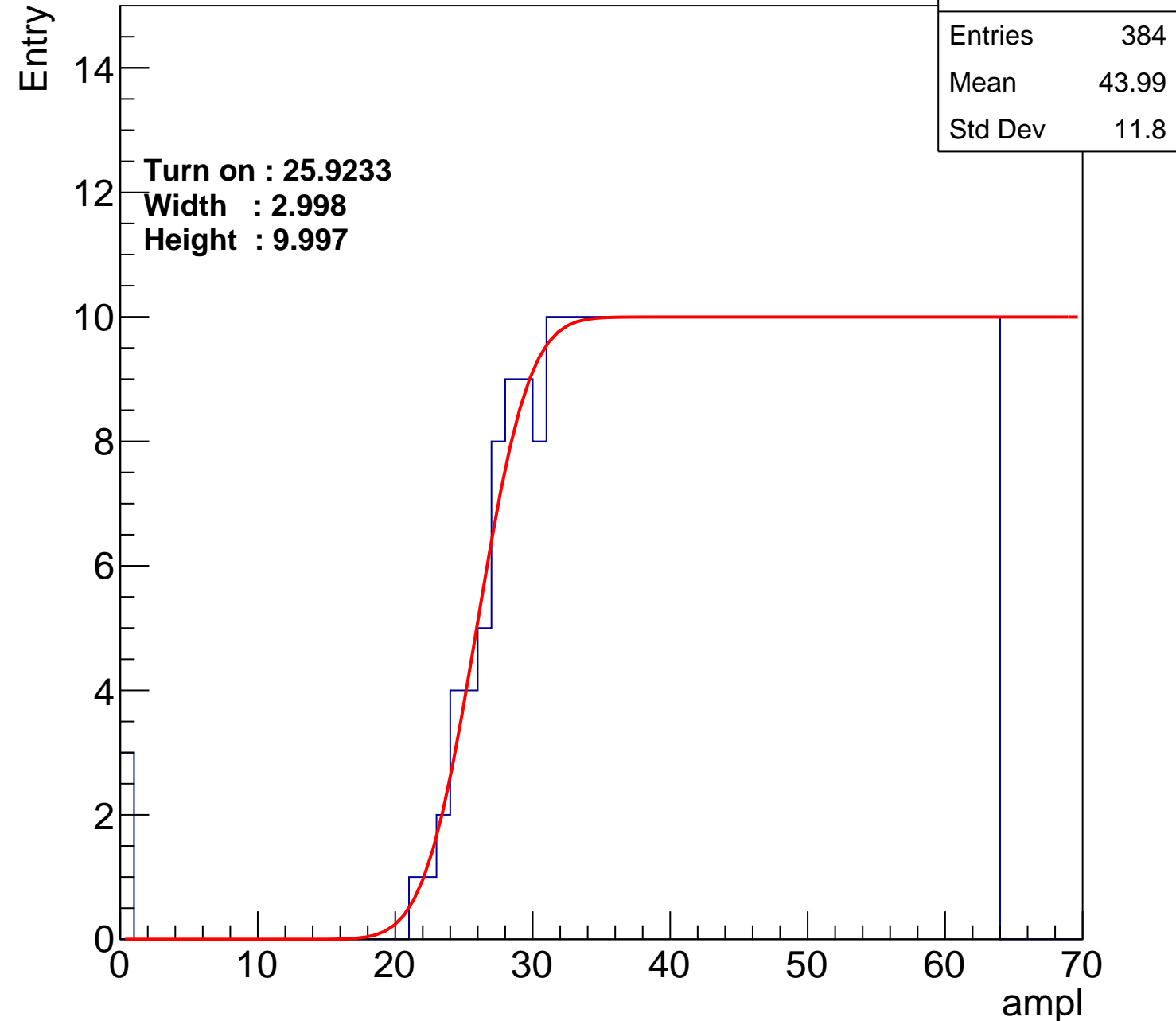
Width : 2.998

Height : 9.997

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch92

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	376
Mean	44.34
Std Dev	11.69

Turn on : 26.1546

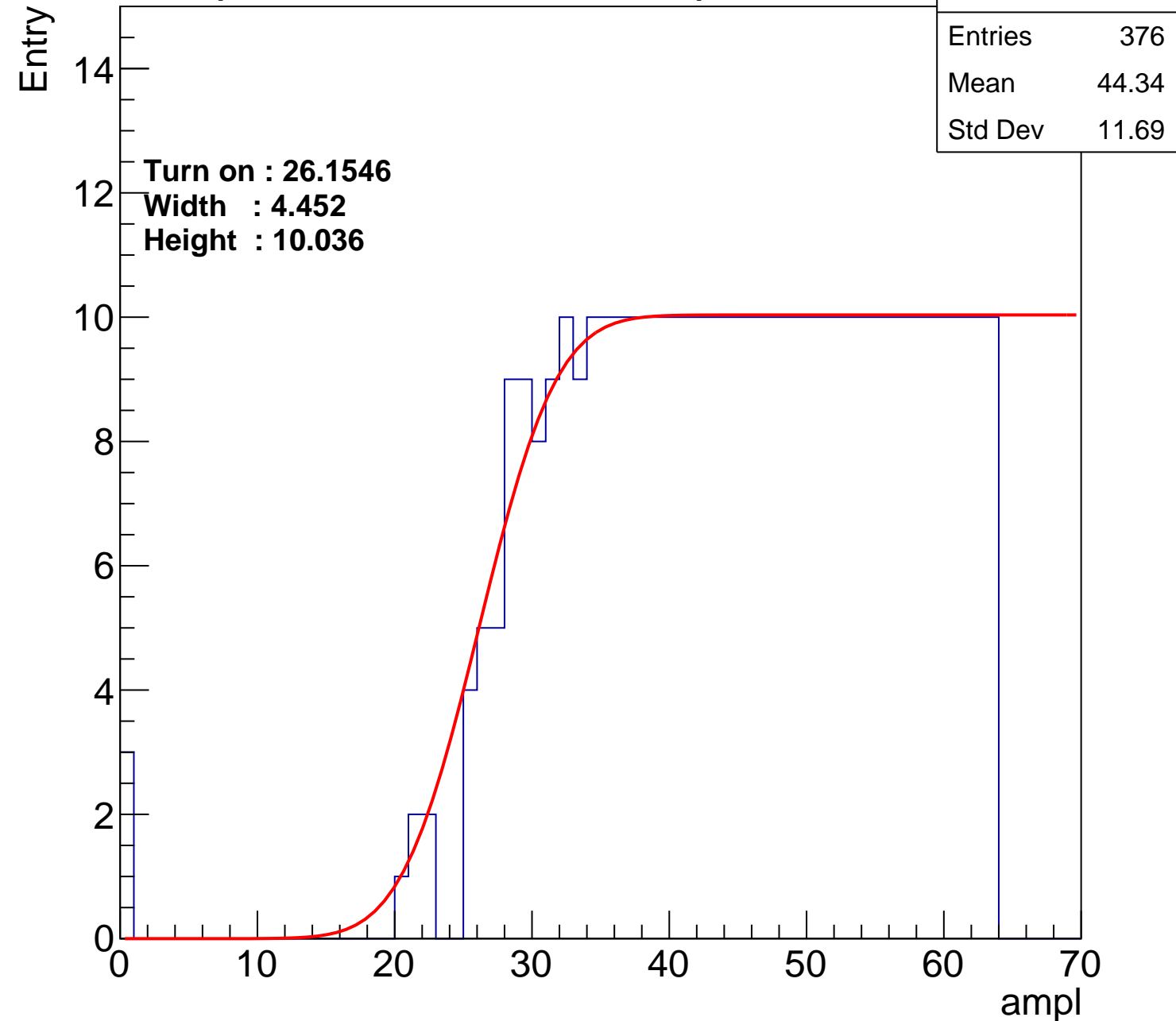
Width : 4.452

Height : 10.036

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch93

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	356
Mean	45.2
Std Dev	11.57

Turn on : 29.4848

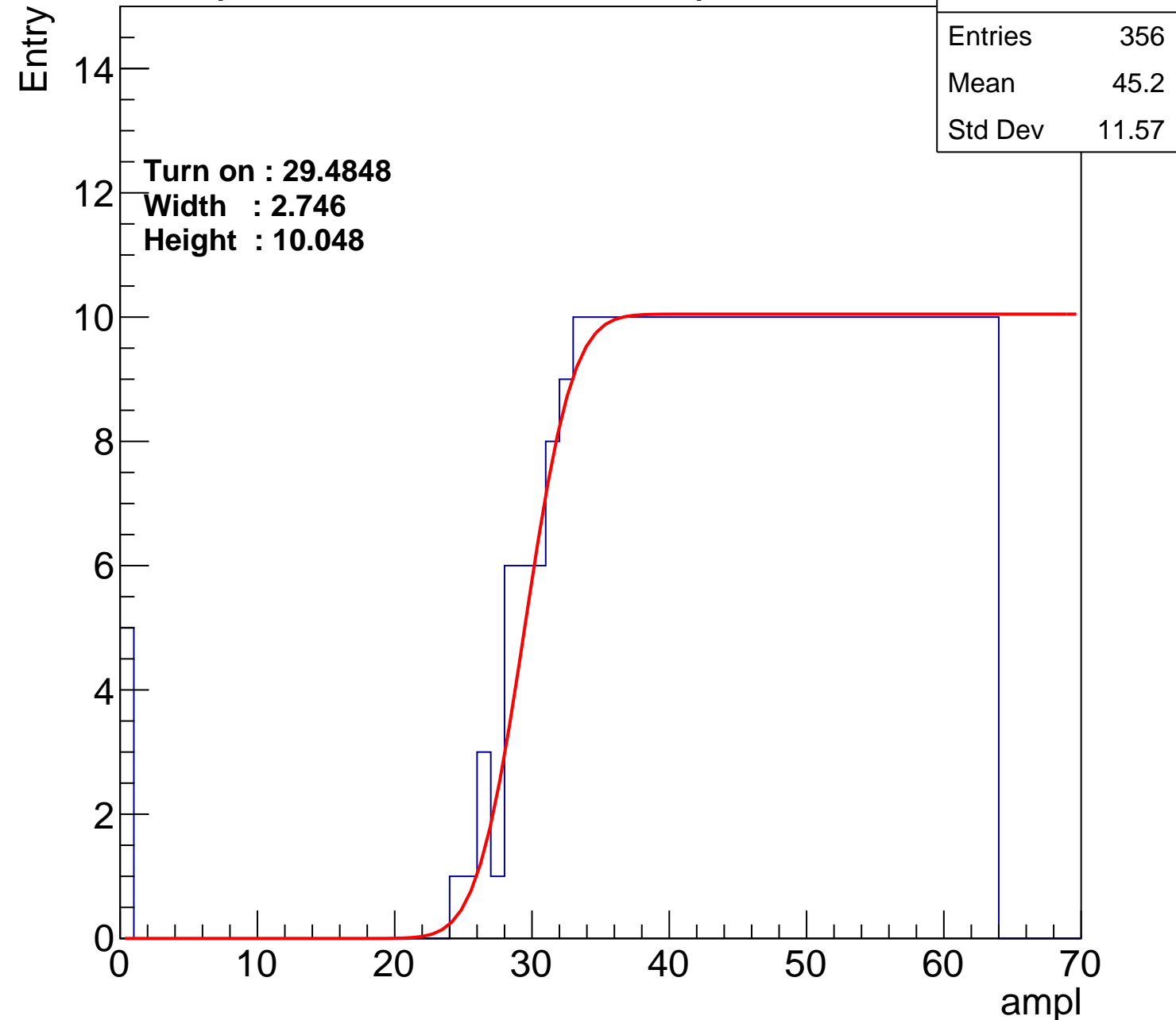
Width : 2.746

Height : 10.048

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch94

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	373
Mean	44.51
Std Dev	11.65

Turn on : 27.1337

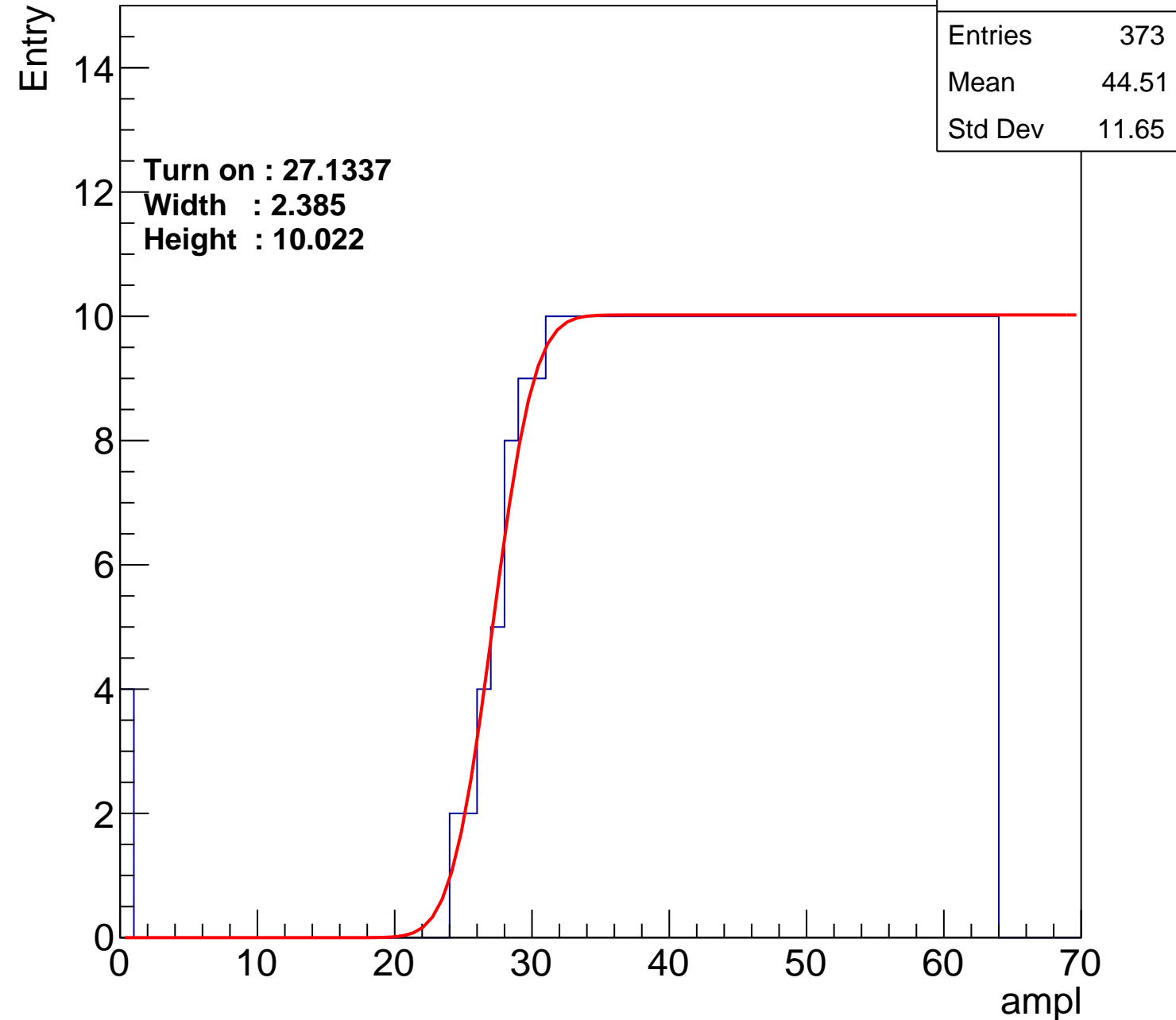
Width : 2.385

Height : 10.022

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U7-ch95

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	380
Mean	44.36
Std Dev	11.28

**Turn on : 26.0253**

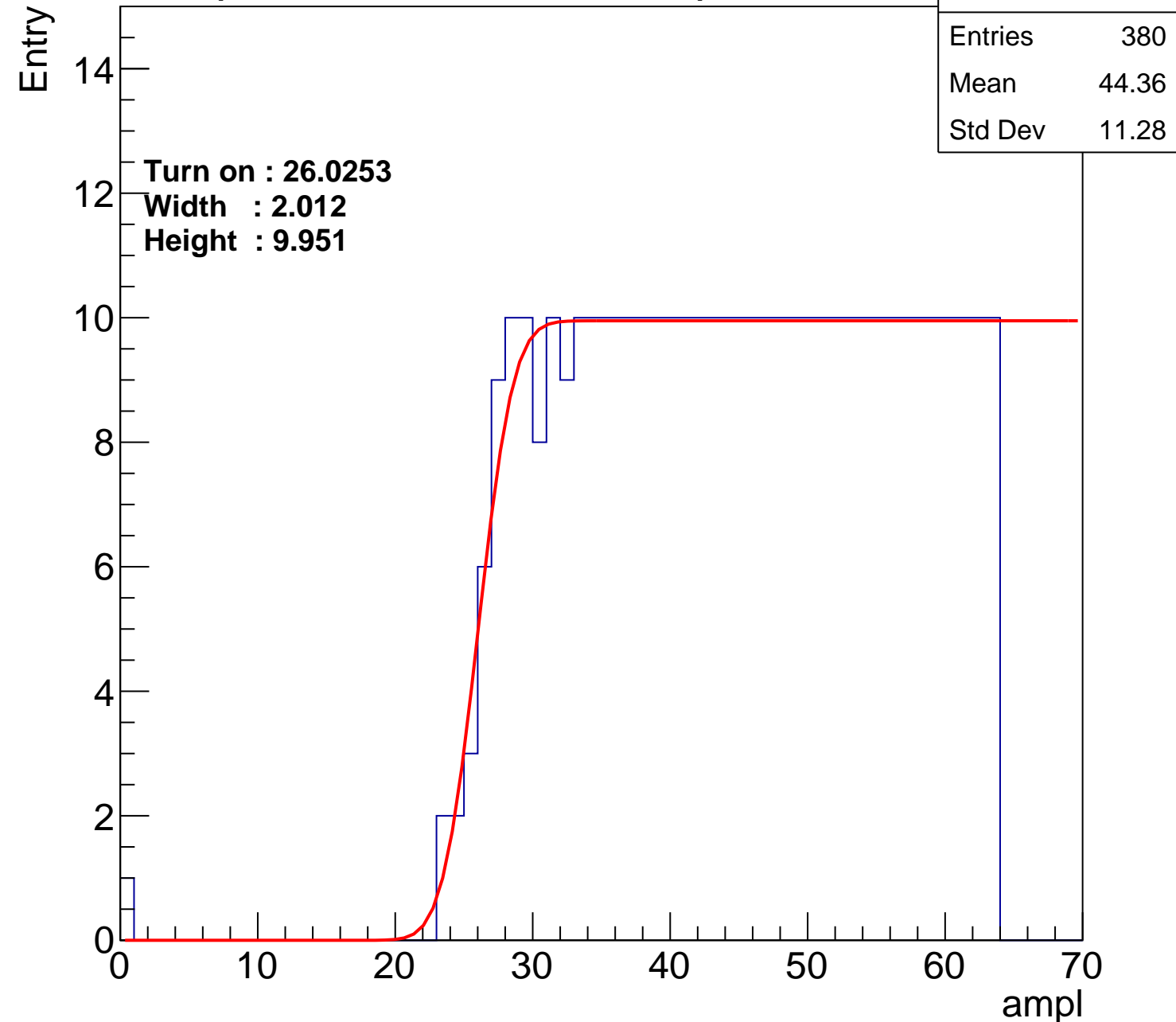
**Width : 2.012**

**Height : 9.951**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch96

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	368
Mean	44.86
Std Dev	11.19

Turn on : 27.9910

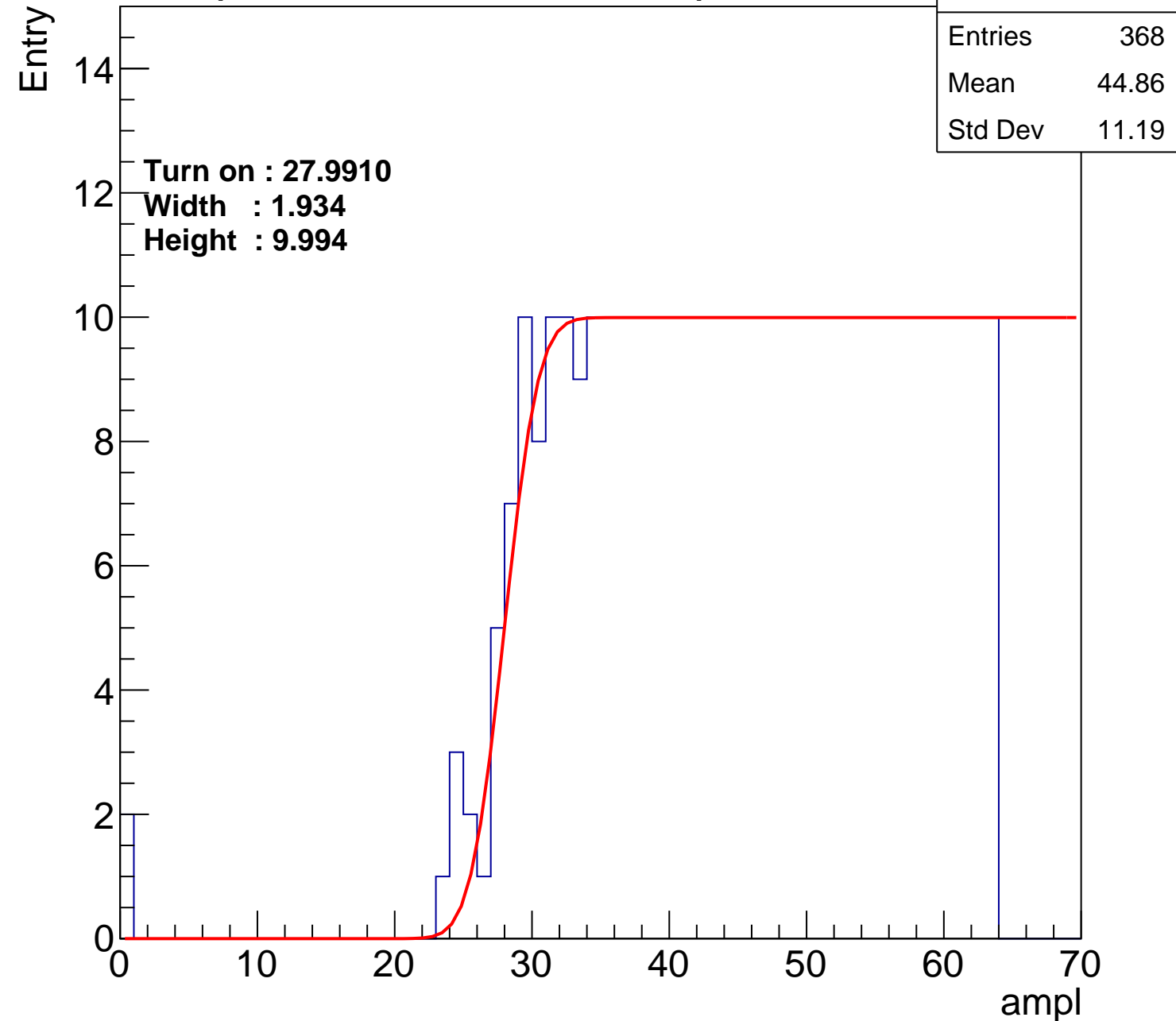
Width : 1.934

Height : 9.994

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch97

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	368
Mean	44.77
Std Dev	11.43

Turn on : 27.5978

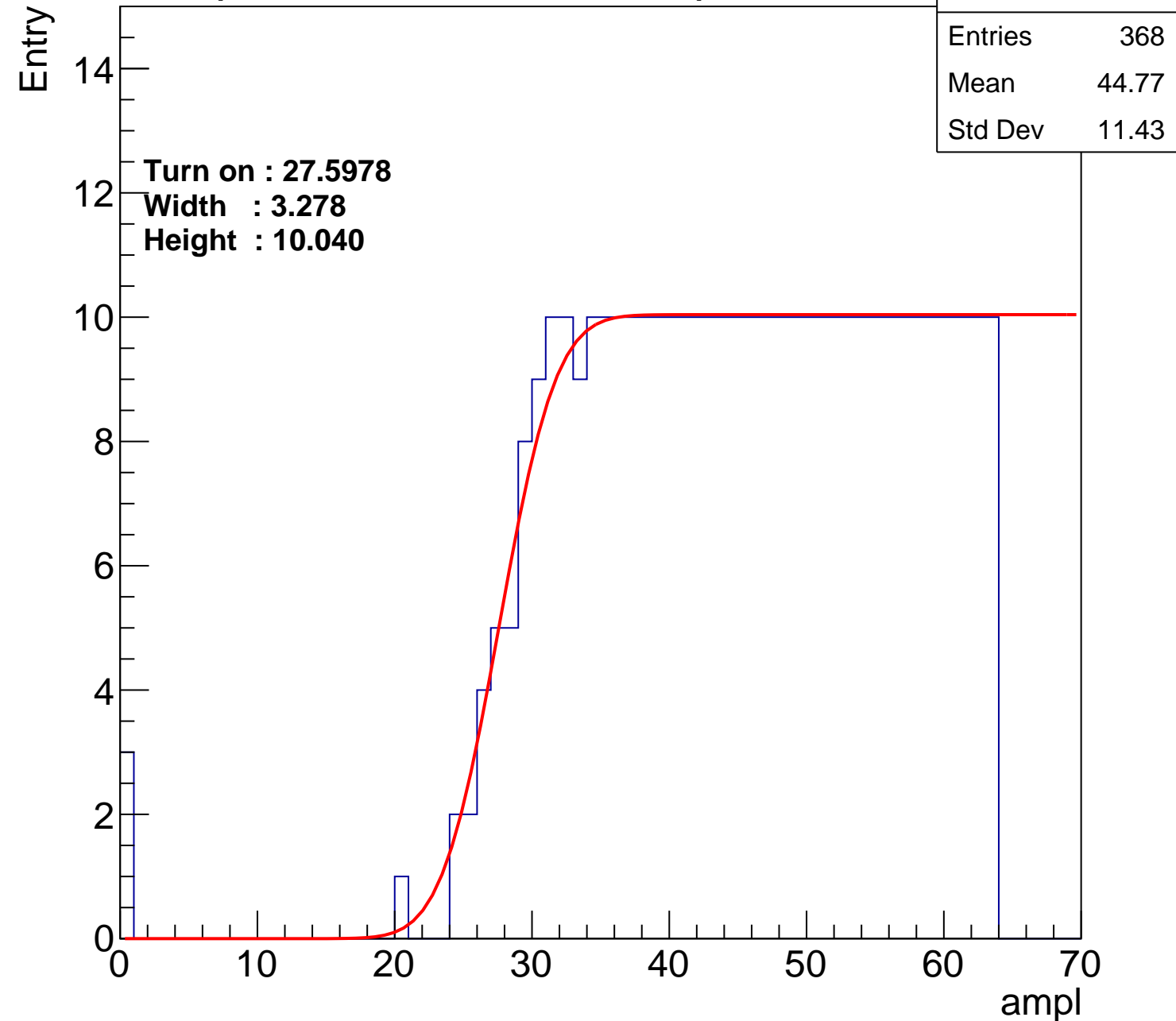
Width : 3.278

Height : 10.040

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch98

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	399
Mean	43.35
Std Dev	11.97

**Turn on : 24.3424**

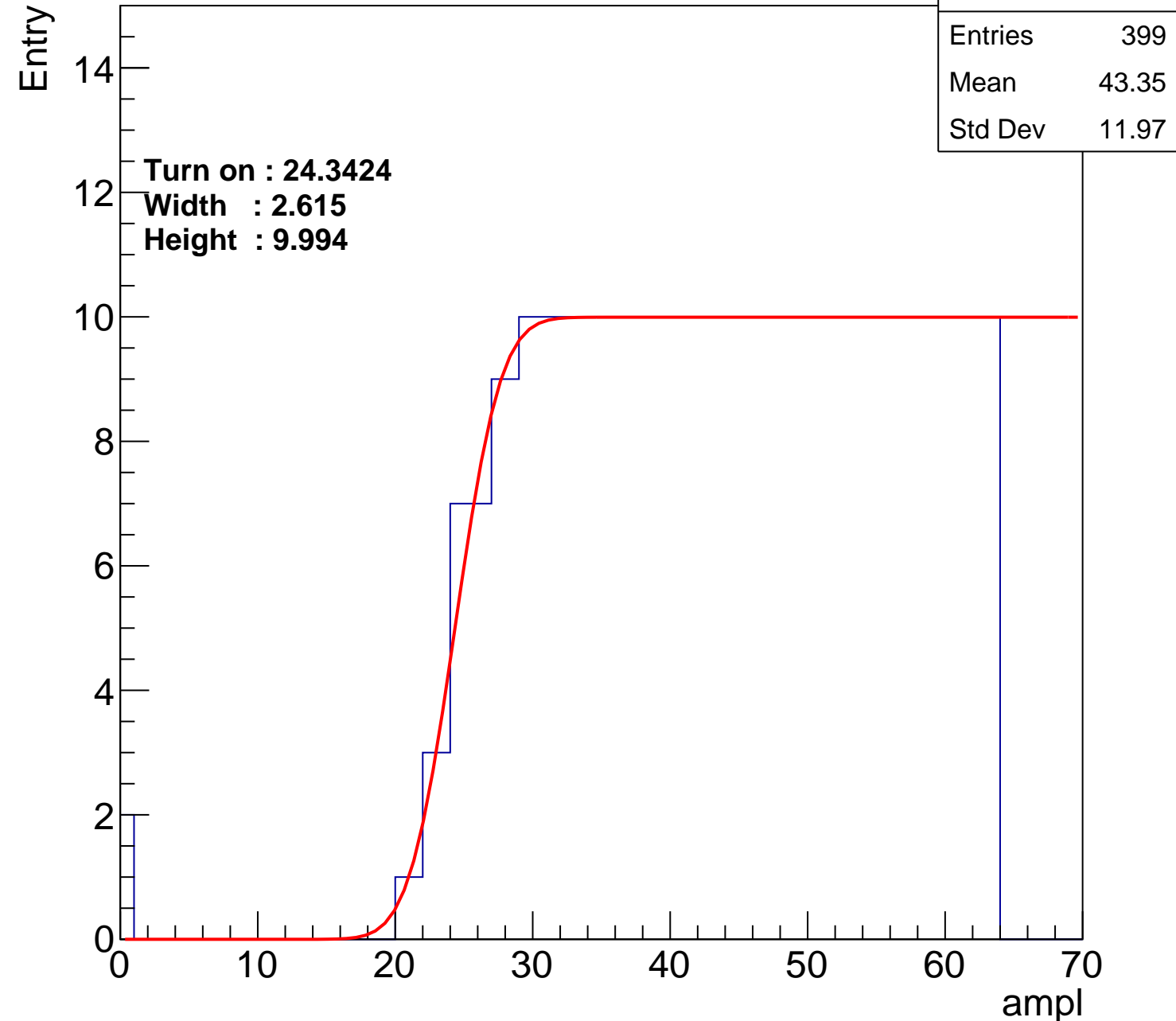
**Width : 2.615**

**Height : 9.994**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch99

calib\_packv5\_042523\_0143.root, FC#0, port D2

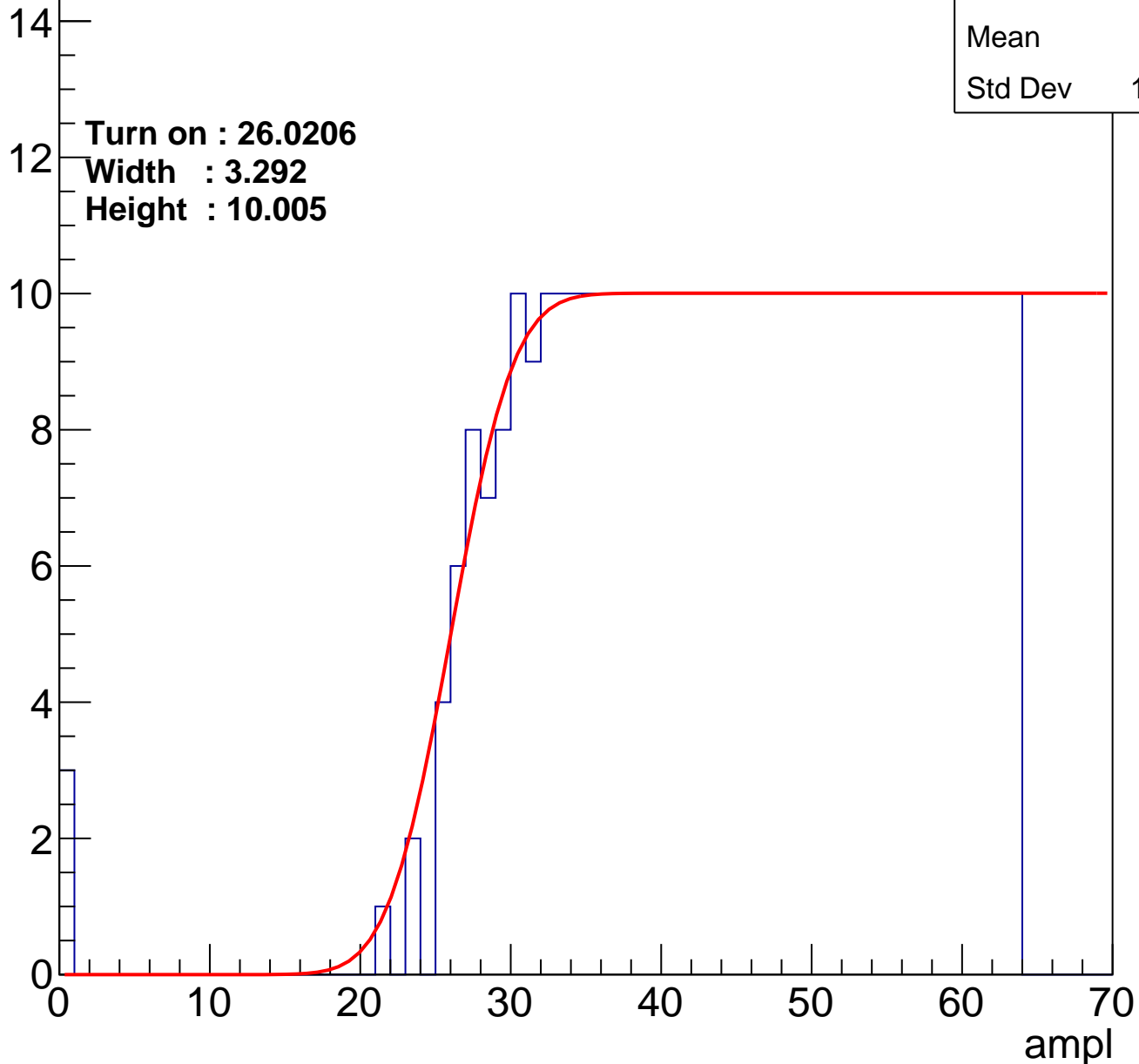
Entries	378
Mean	44.3
Std Dev	11.63

Turn on : 26.0206

Width : 3.292

Height : 10.005

Entry



# B1L101S, U7-ch100

calib\_packv5\_042523\_0143.root, FC#0, port D2

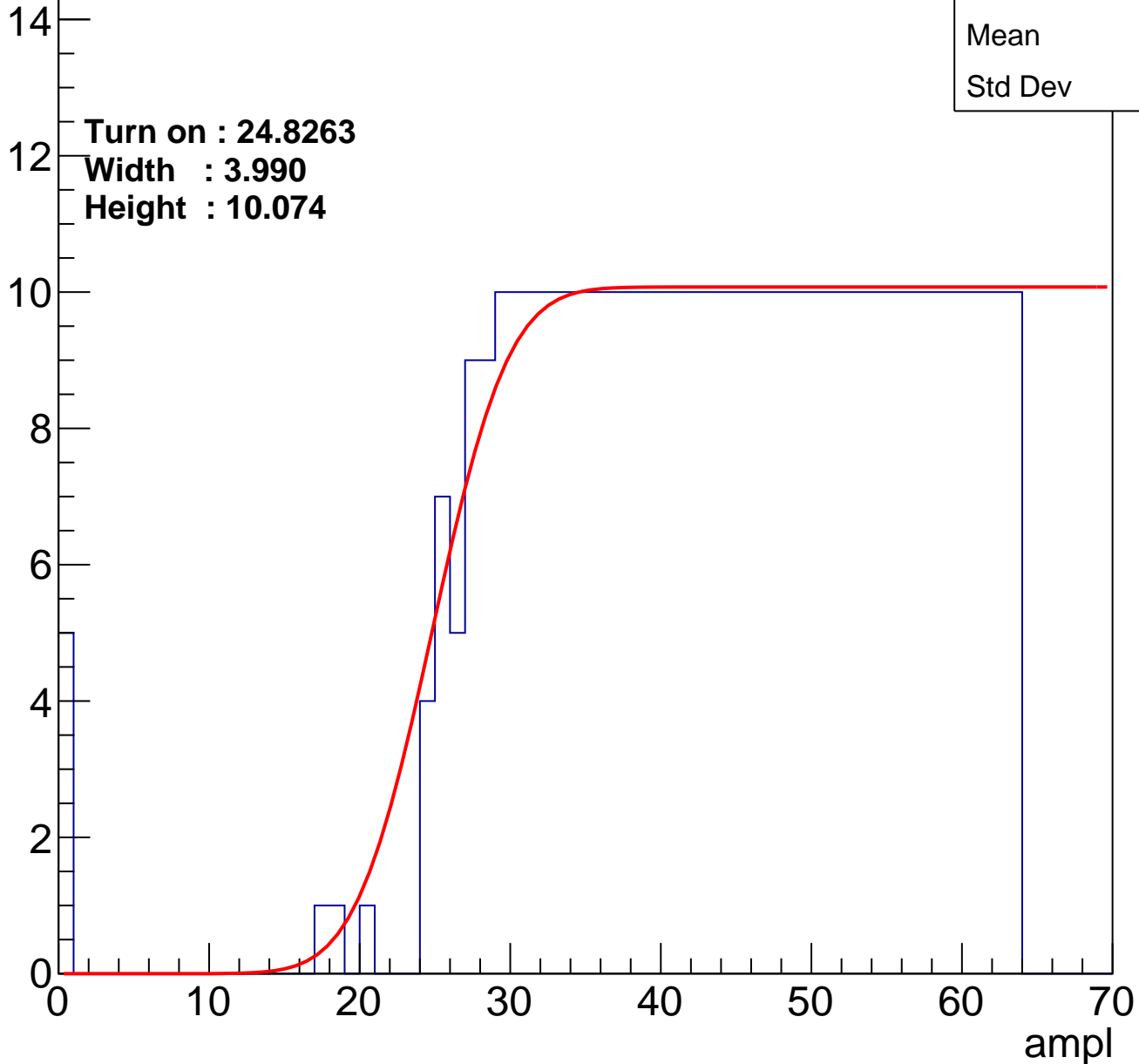
Entries	392
Mean	43.5
Std Dev	12.3

Turn on : 24.8263

Width : 3.990

Height : 10.074

Entry



# B1L101S, U7-ch101

calib\_packv5\_042523\_0143.root, FC#0, port D2

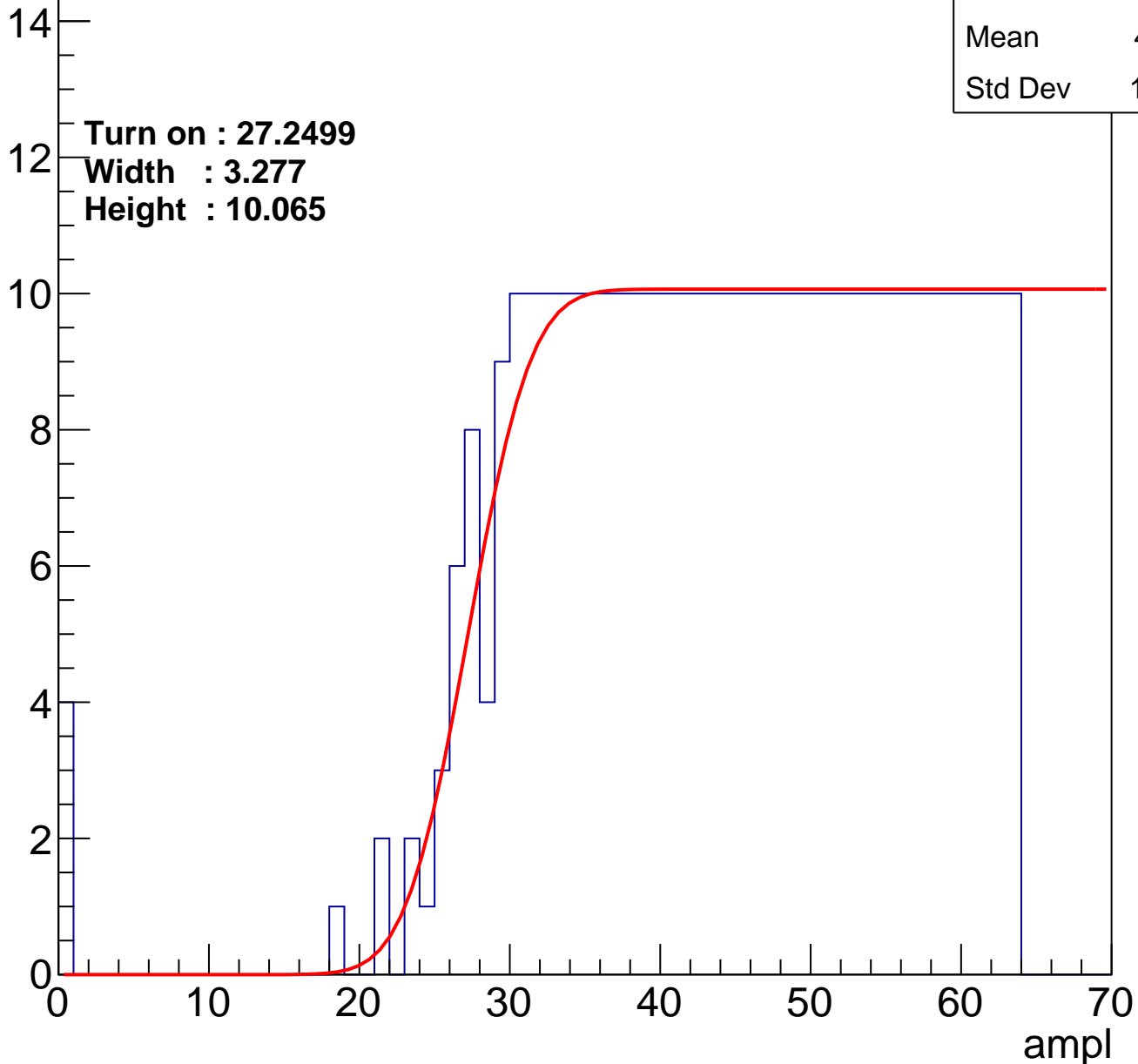
Entries	380
Mean	44.11
Std Dev	11.92

Turn on : 27.2499

Width : 3.277

Height : 10.065

Entry



# B1L101S, U7-ch102

calib\_packv5\_042523\_0143.root, FC#0, port D2

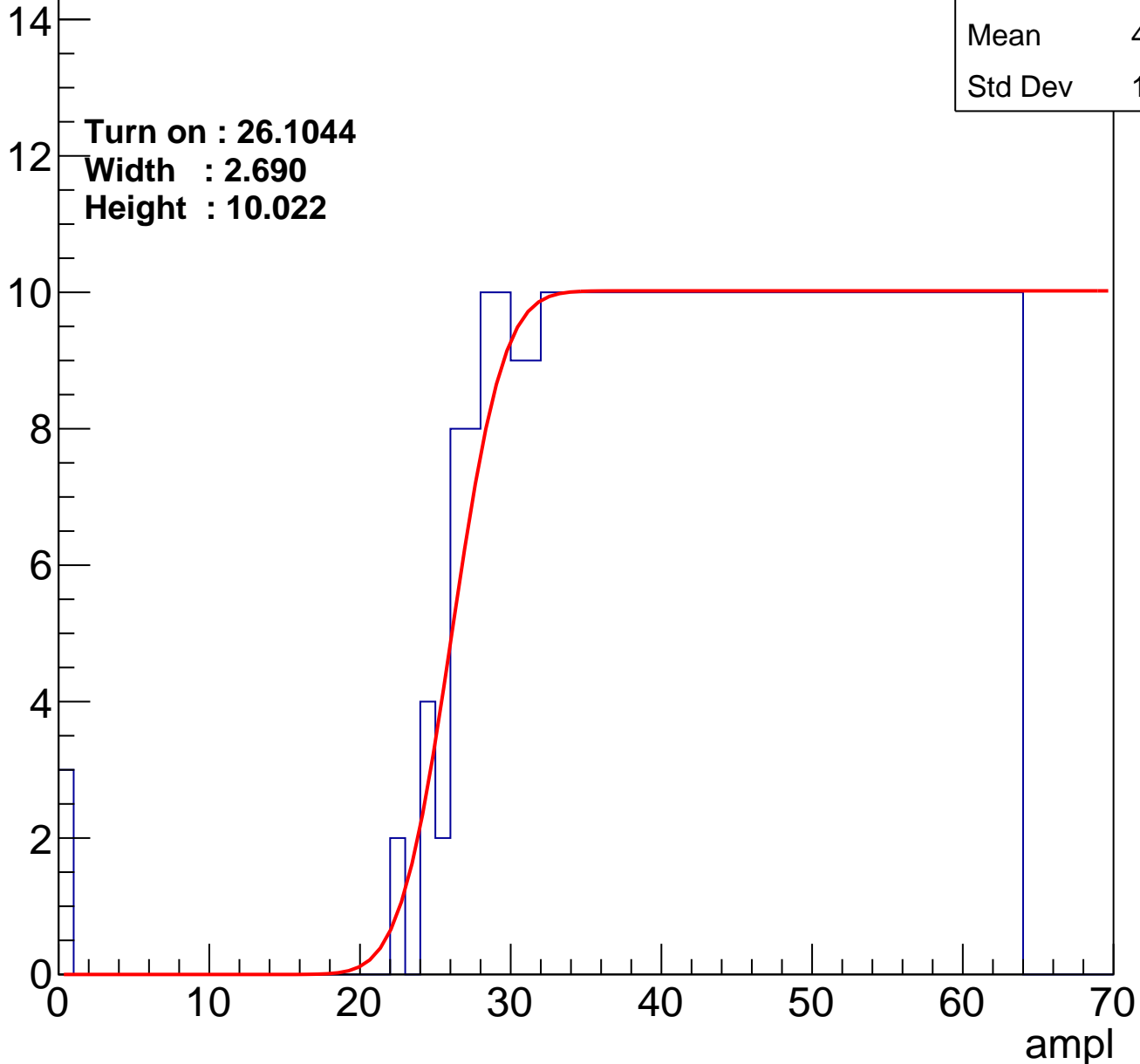
Entries	385
Mean	43.98
Std Dev	11.77

Turn on : 26.1044

Width : 2.690

Height : 10.022

Entry





# B1L101S, U7-ch103

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	365
Mean	44.91
Std Dev	11.36

**Turn on : 27.9490**

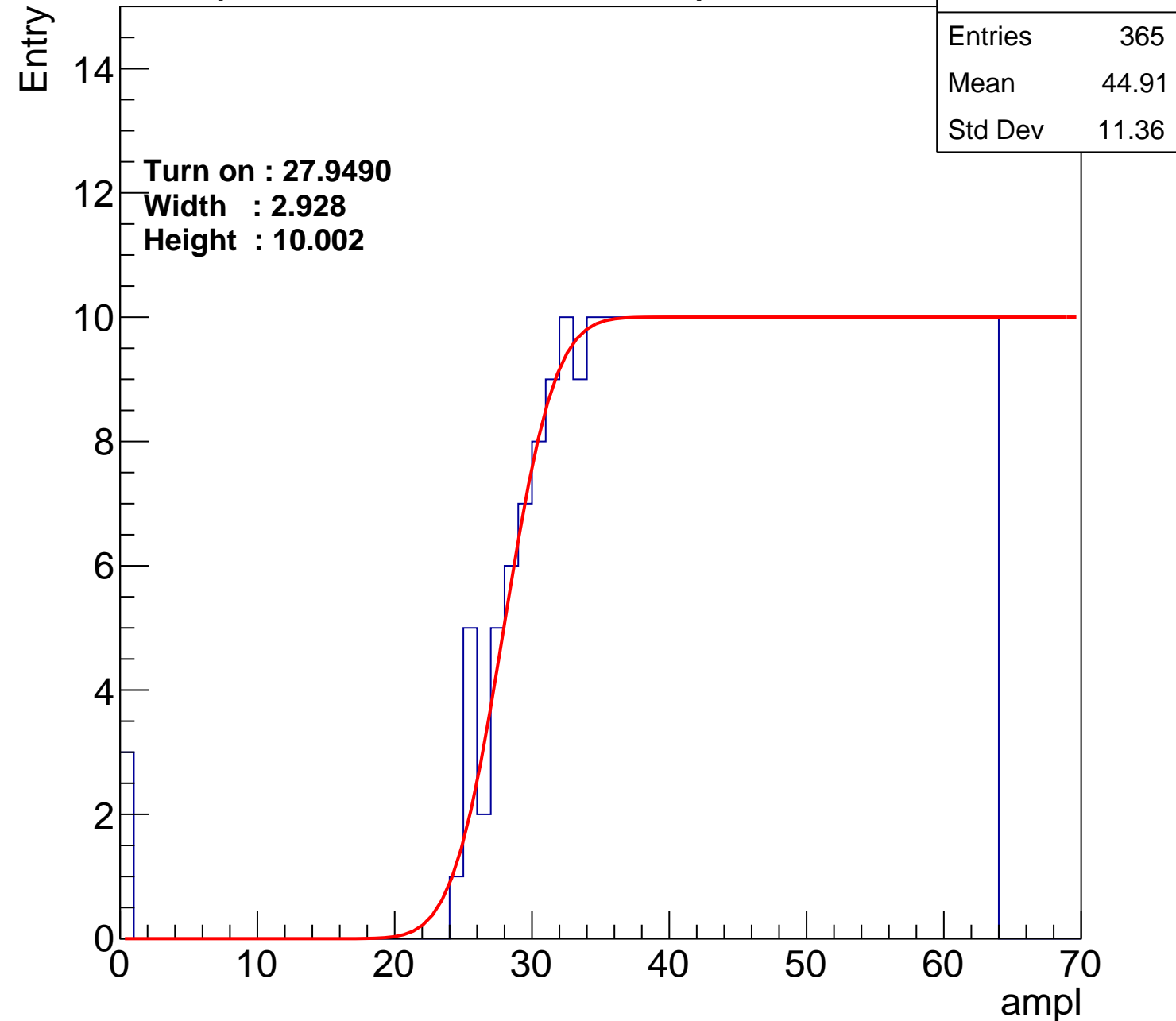
**Width : 2.928**

**Height : 10.002**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch104

calib\_packv5\_042523\_0143.root, FC#0, port D2

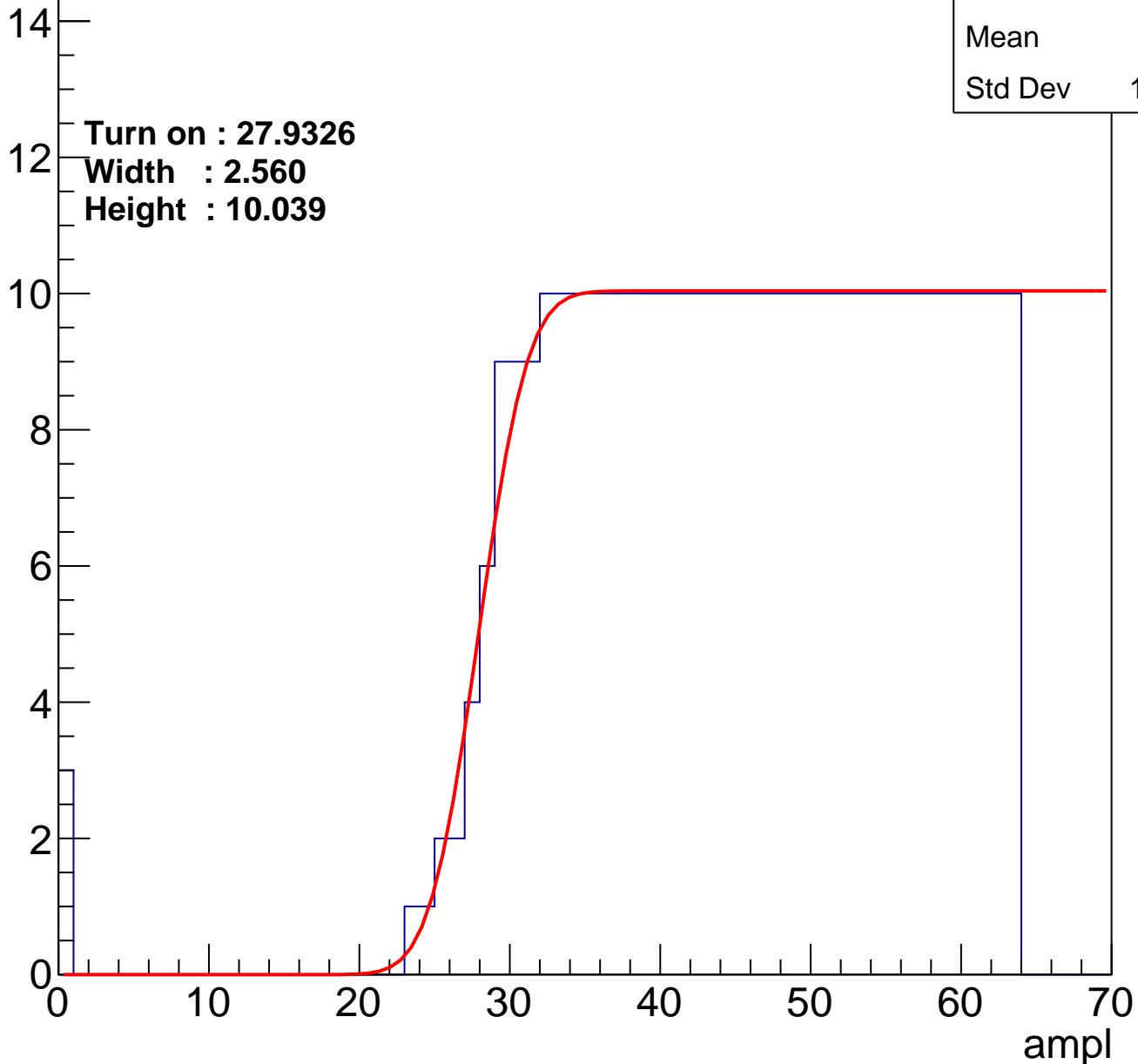
Entries	366
Mean	44.9
Std Dev	11.32

Turn on : 27.9326

Width : 2.560

Height : 10.039

Entry



# B1L101S, U7-ch105

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	371
Mean	44.7
Std Dev	11.29

**Turn on : 27.4787**

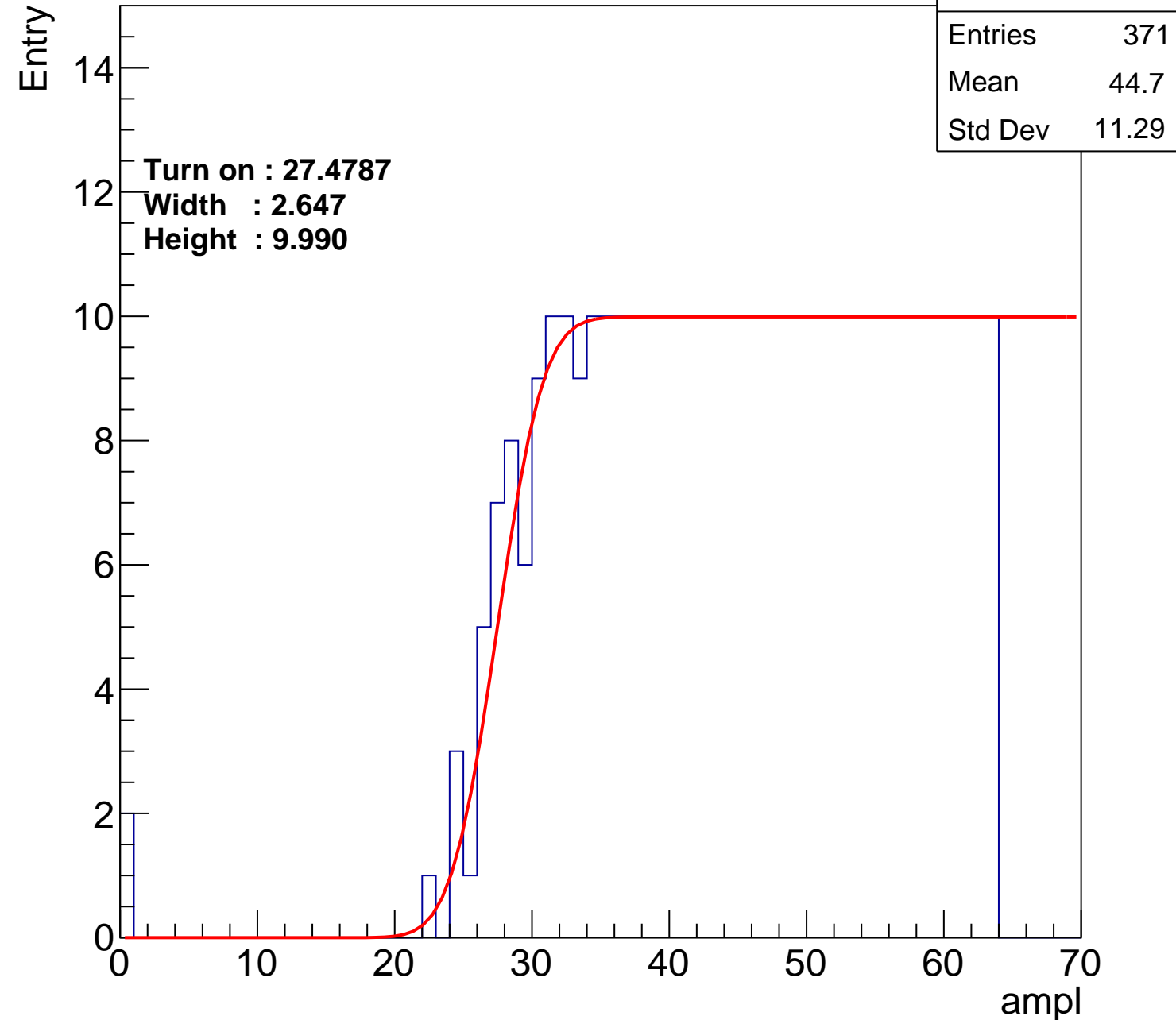
**Width : 2.647**

**Height : 9.990**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch106

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	390
Mean	43.52
Std Dev	12.43

Turn on : 25.7751

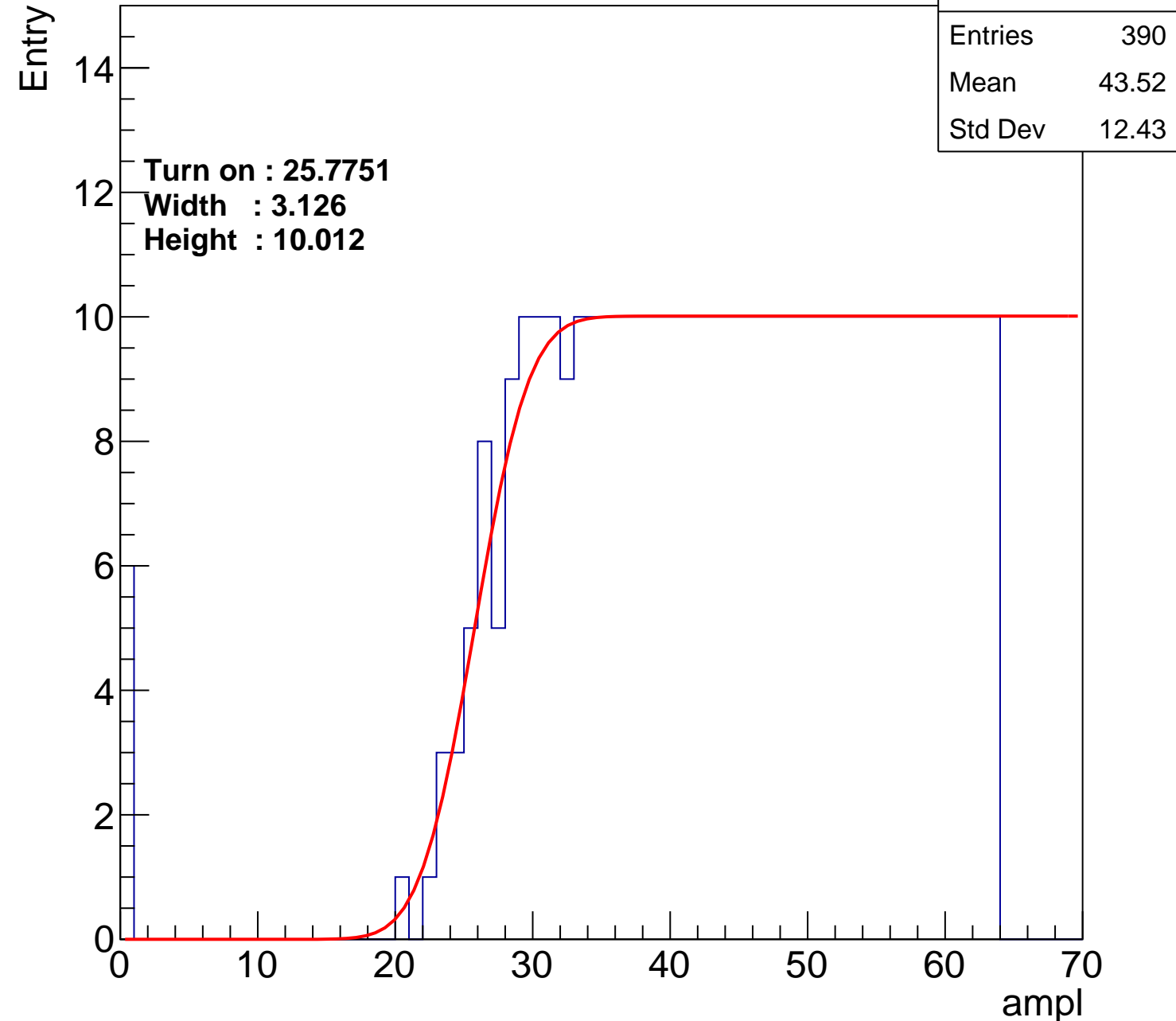
Width : 3.126

Height : 10.012

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch107

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	381
Mean	44.17
Std Dev	11.68

Turn on : 26.3989

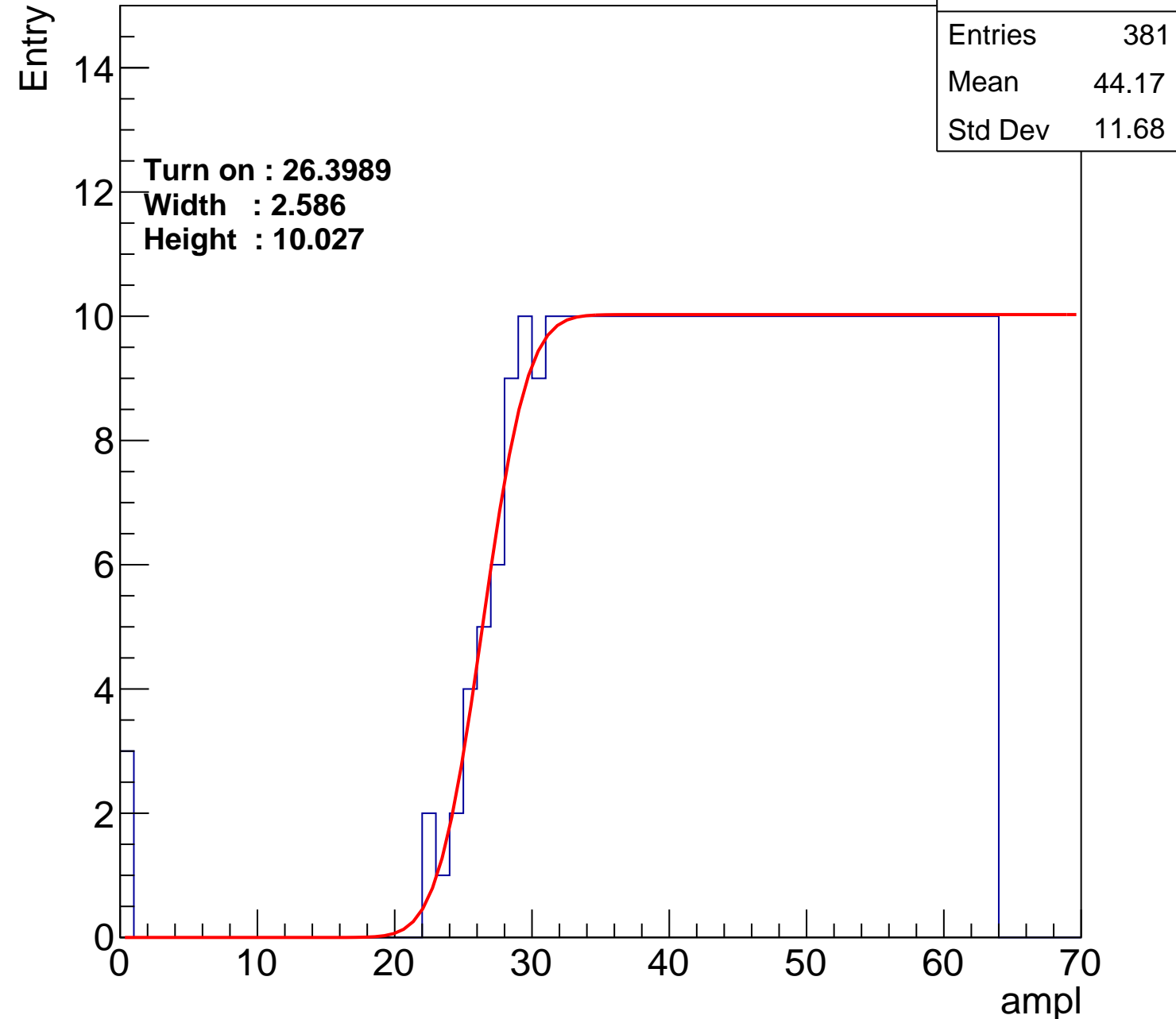
Width : 2.586

Height : 10.027

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch108

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	375
Mean	44.47
Std Dev	11.51

Turn on : 26.8333

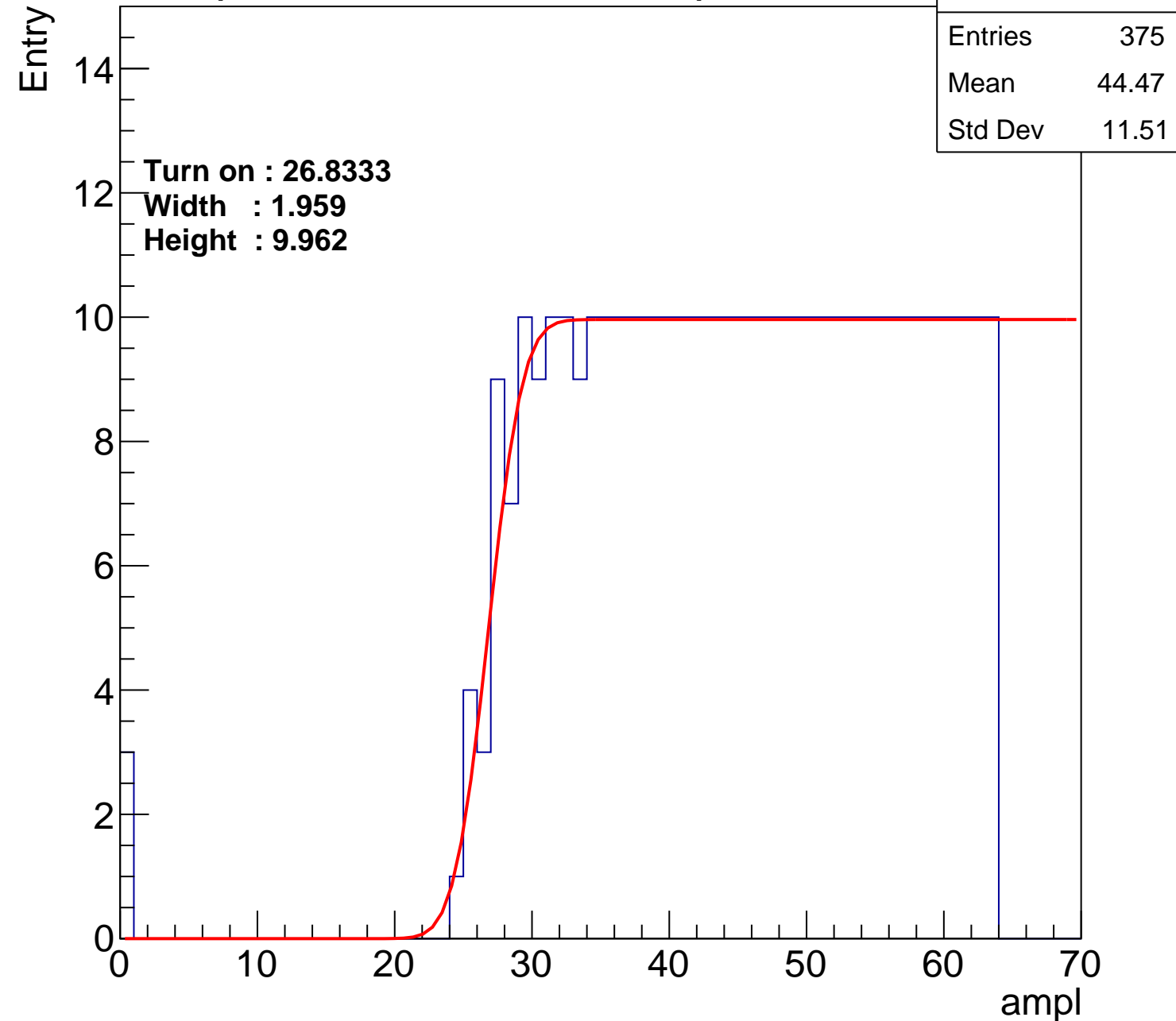
Width : 1.959

Height : 9.962

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch109

calib\_packv5\_042523\_0143.root, FC#0, port D2

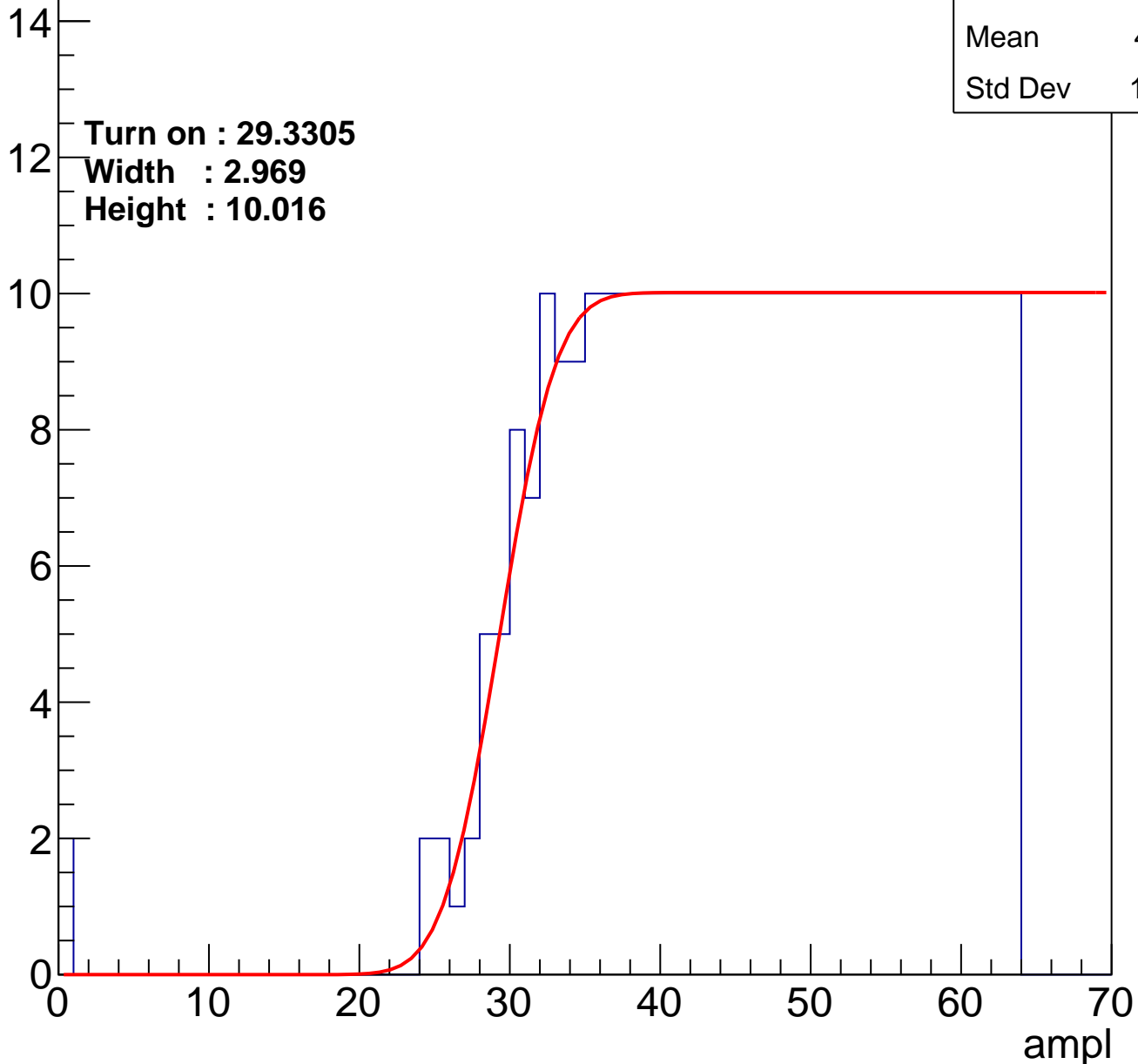
Entries	352
Mean	45.61
Std Dev	10.86

**Turn on : 29.3305**

**Width : 2.969**

**Height : 10.016**

Entry



# B1L101S, U7-ch110

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	394
Mean	43.62
Std Dev	11.73

Turn on : 24.9006

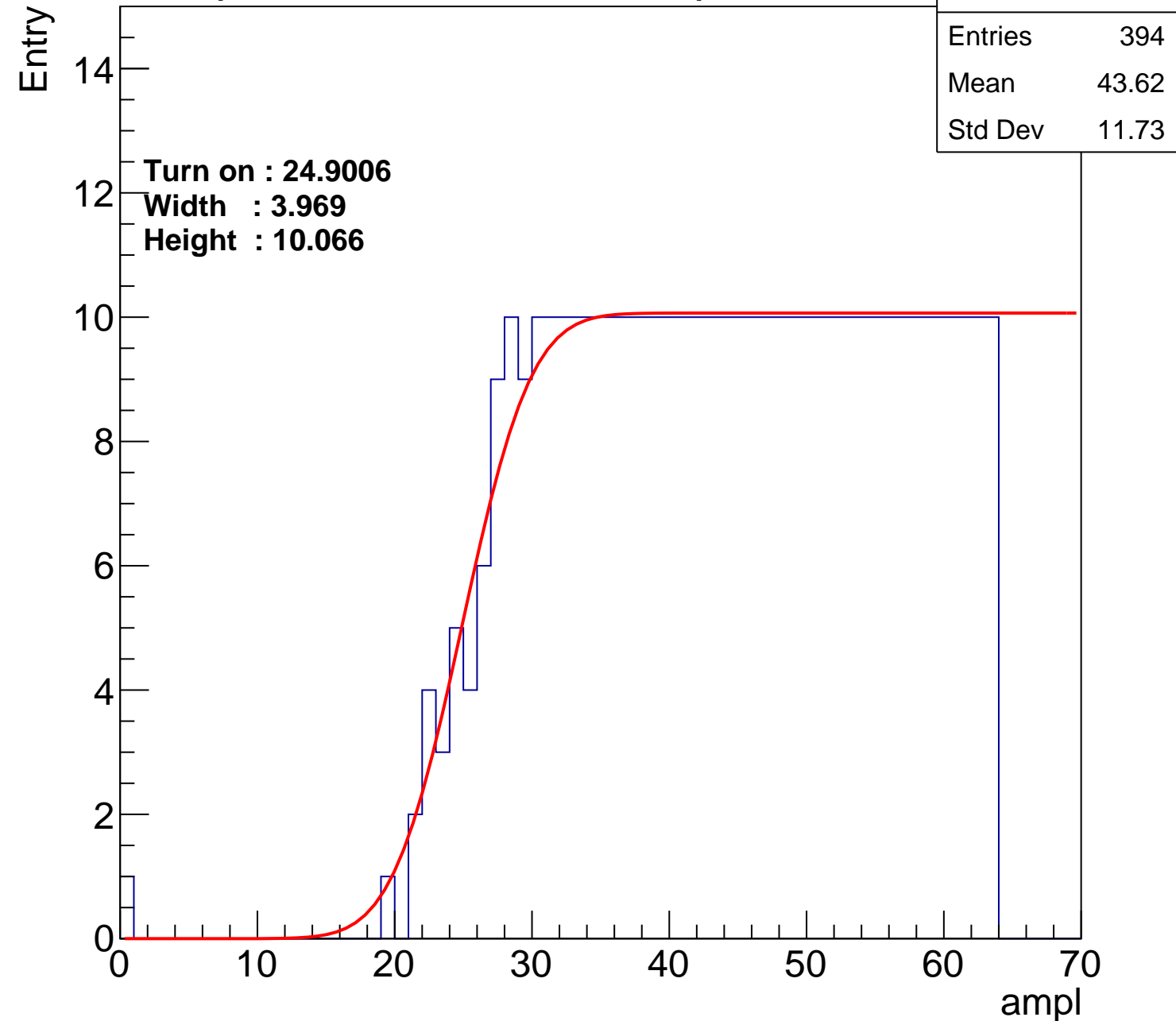
Width : 3.969

Height : 10.066

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U7-ch111

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	368
Mean	44.91
Std Dev	11.04

**Turn on : 27.9898**

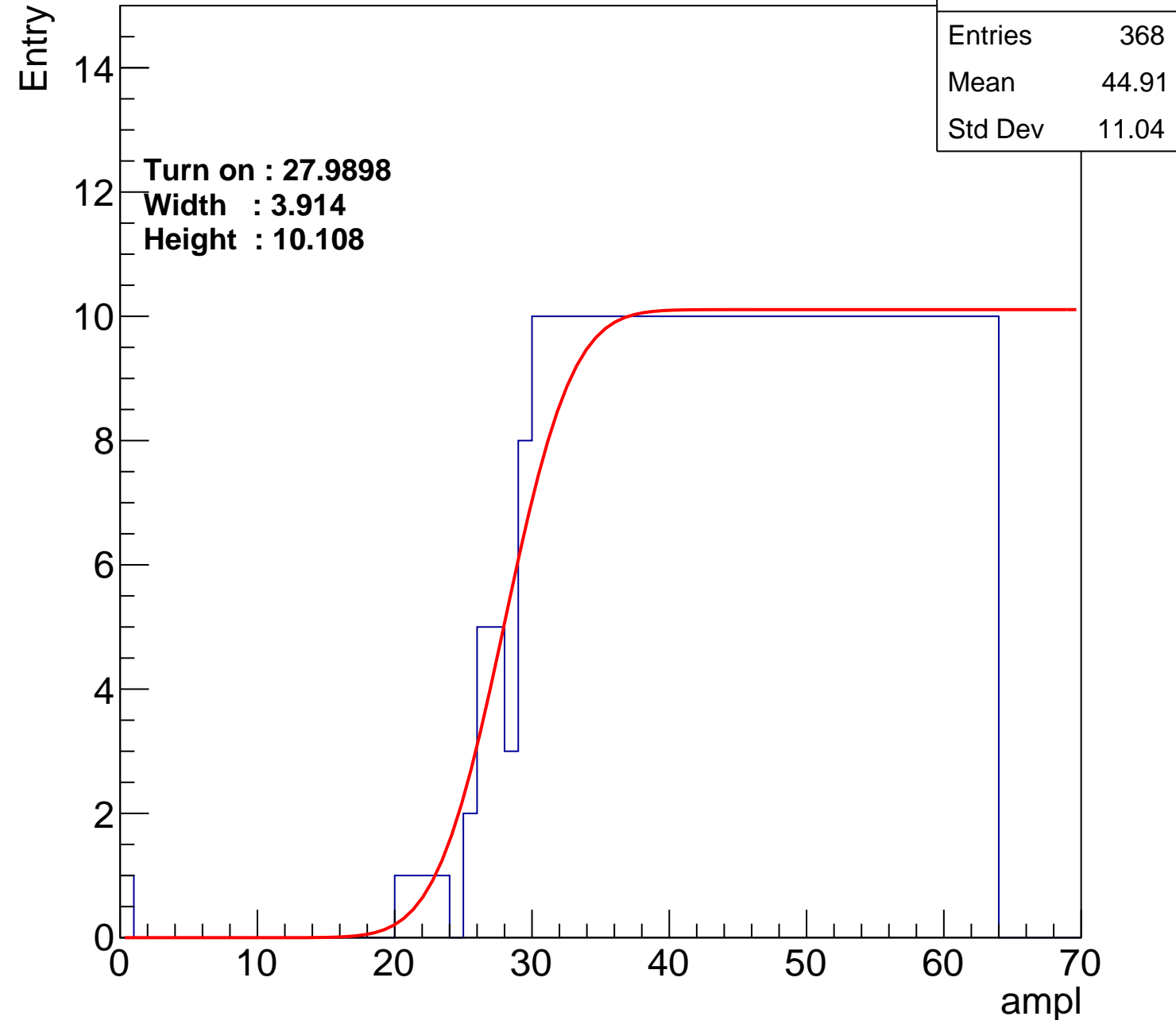
**Width : 3.914**

**Height : 10.108**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch112

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	371
Mean	44.59
Std Dev	11.63

Turn on : 27.2505

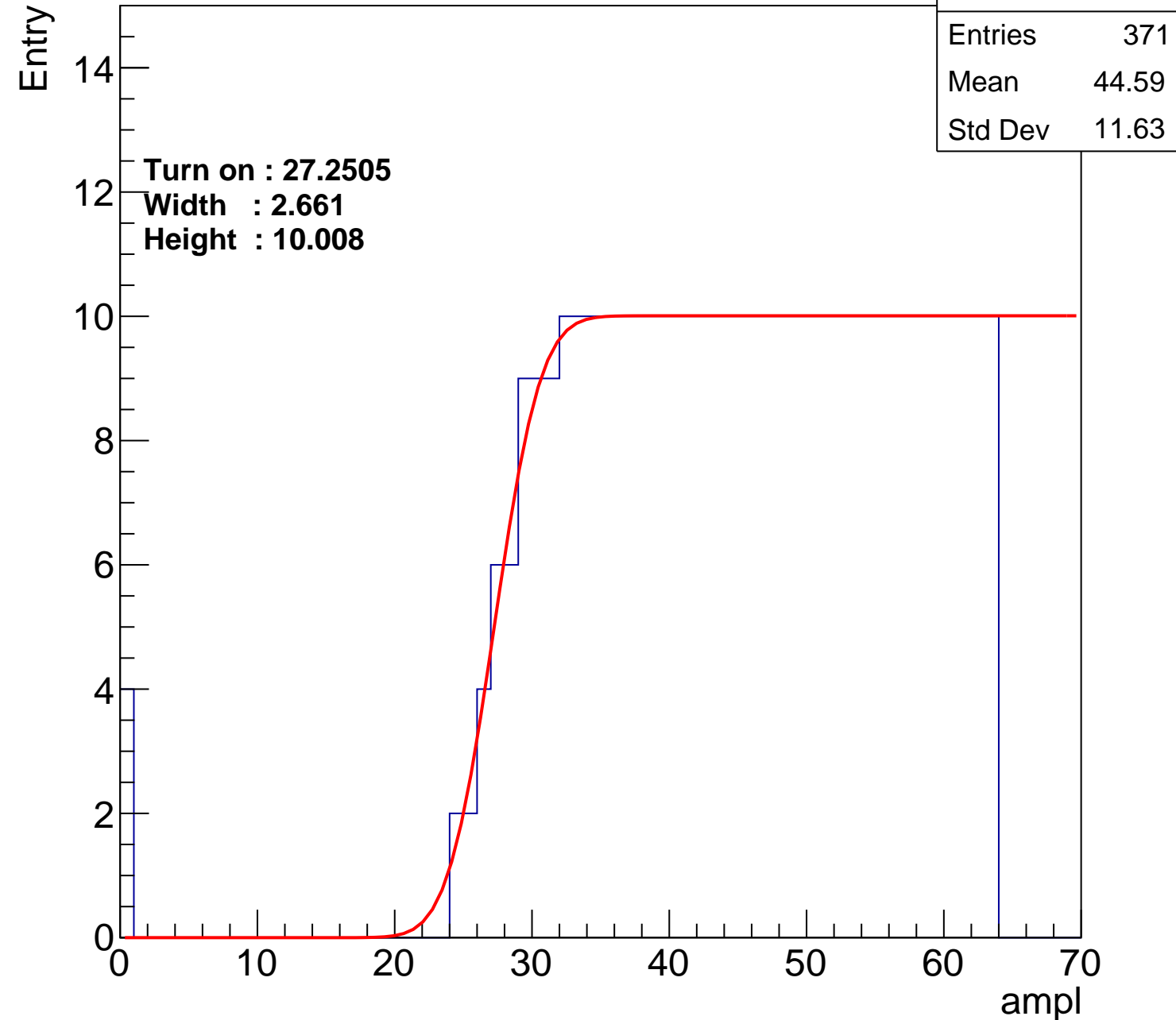
Width : 2.661

Height : 10.008

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch113

calib\_packv5\_042523\_0143.root, FC#0, port D2

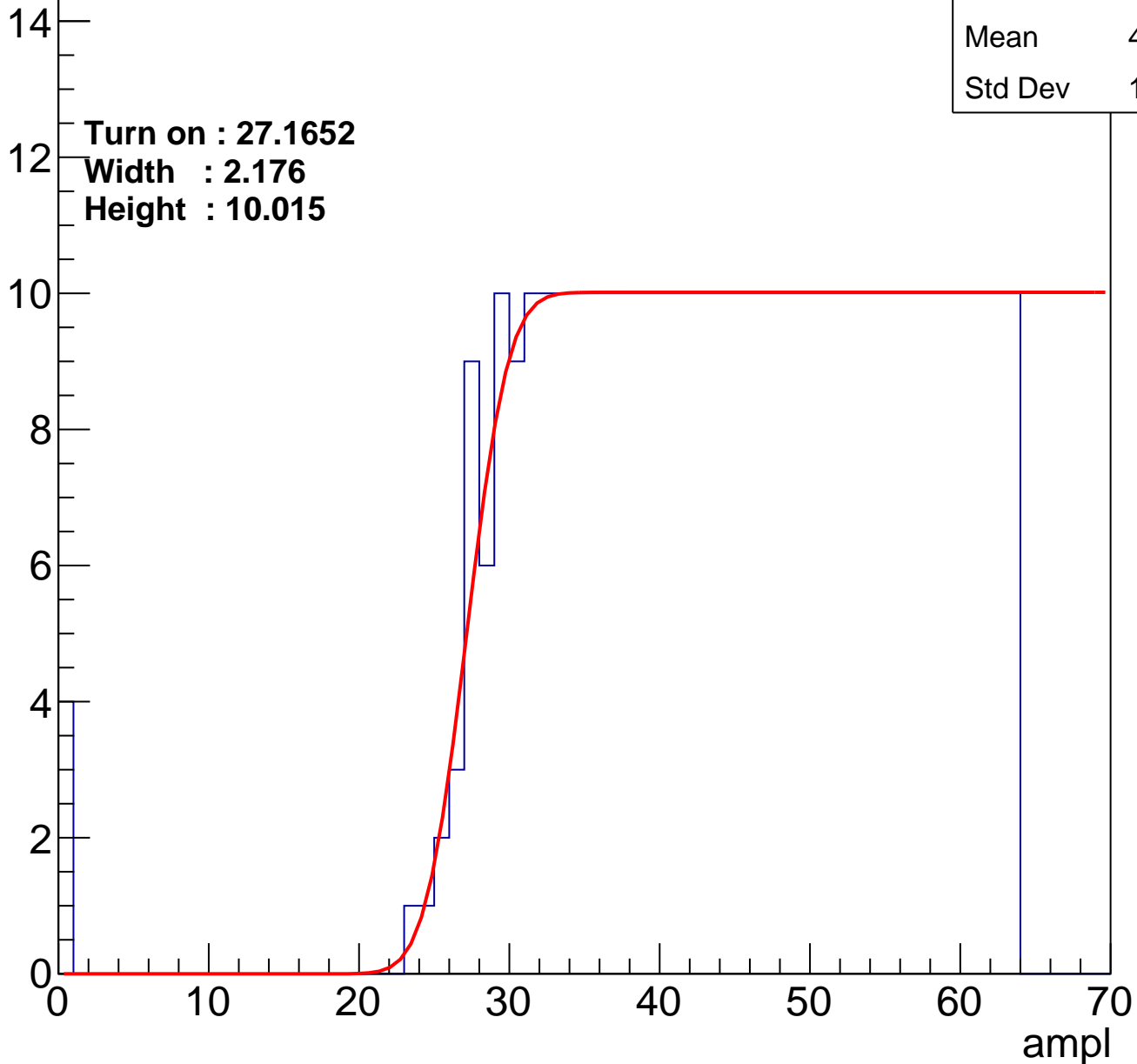
Entries	375
Mean	44.42
Std Dev	11.69

Turn on : 27.1652

Width : 2.176

Height : 10.015

Entry



# B1L101S, U7-ch114

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	381
Mean	44.17
Std Dev	11.67

Turn on : 25.8897

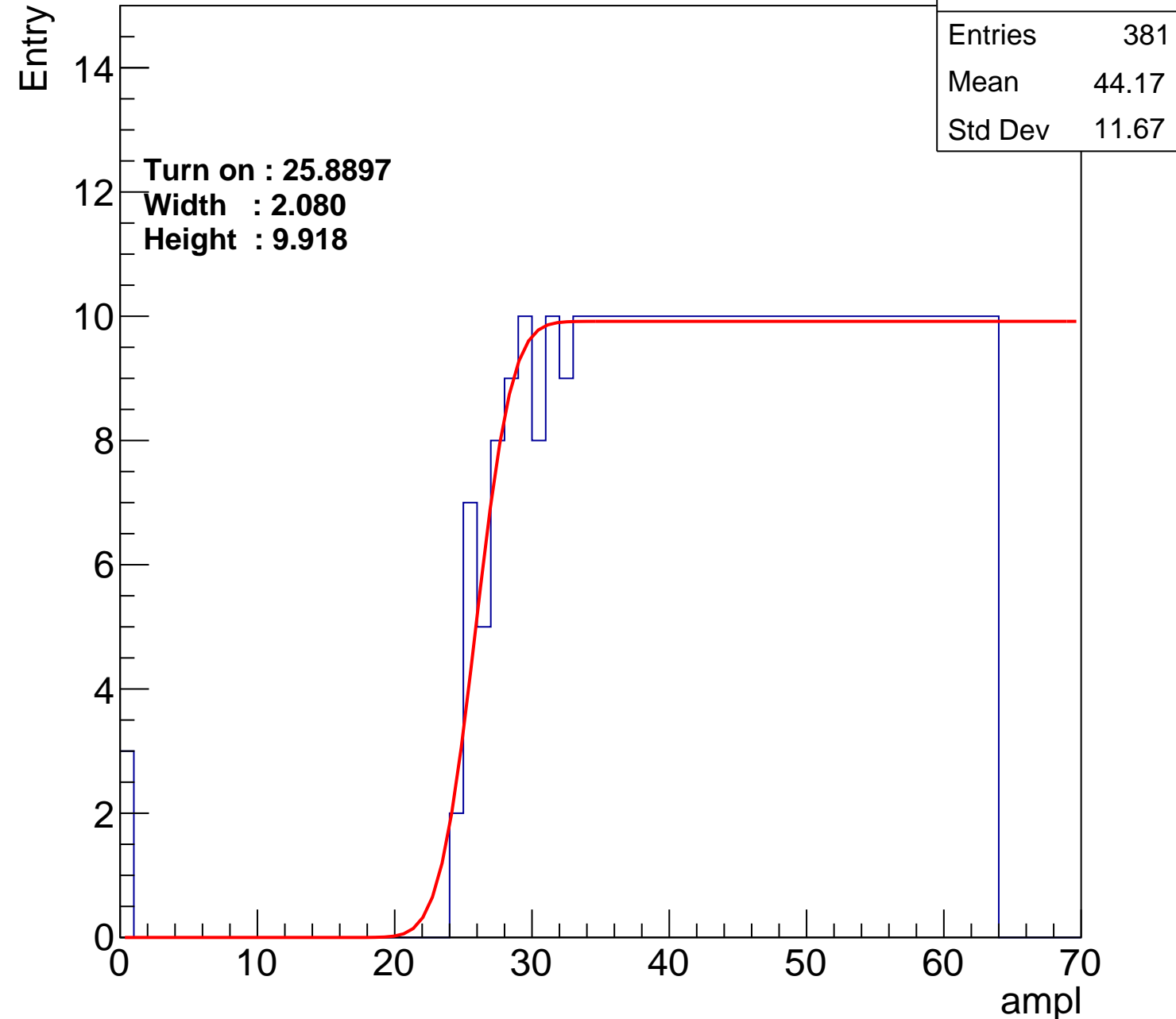
Width : 2.080

Height : 9.918

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch115

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	375
Mean	44.43
Std Dev	11.59

Turn on : 27.2950

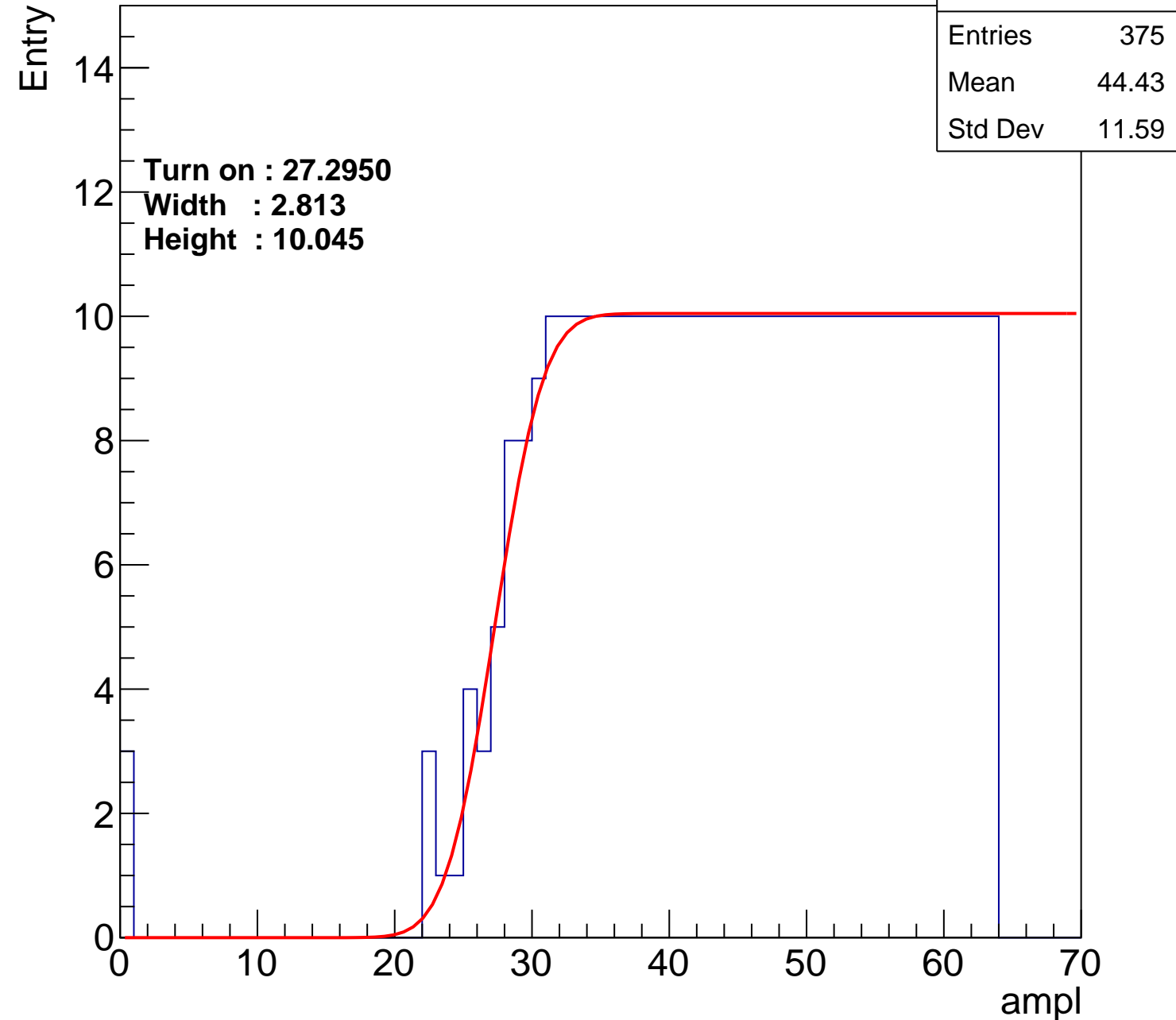
Width : 2.813

Height : 10.045

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch116

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	386
Mean	43.81
Std Dev	12.06

Turn on : 26.1889

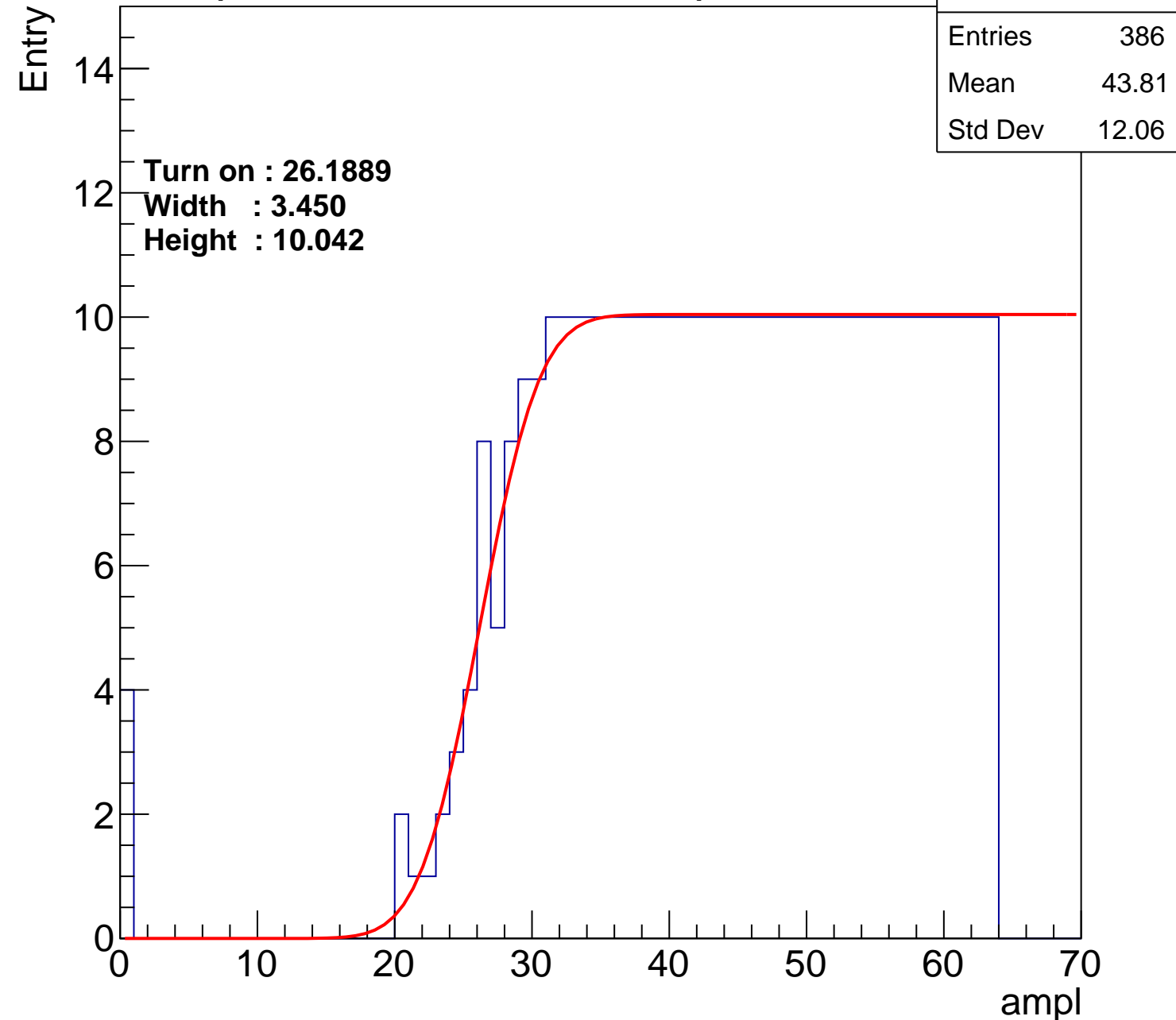
Width : 3.450

Height : 10.042

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch117

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	398
Mean	43.17
Std Dev	12.54

Turn on : 24.5867

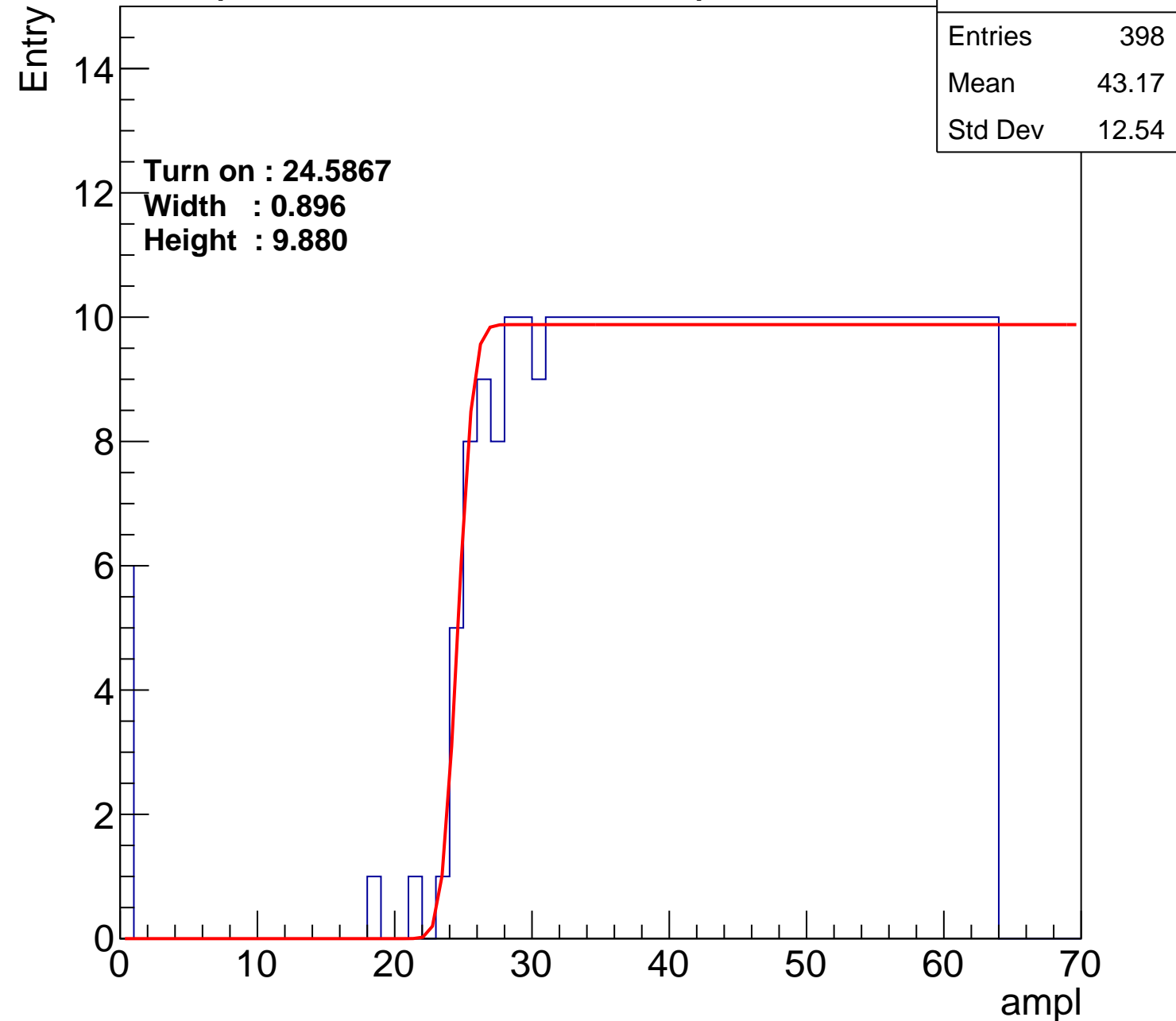
Width : 0.896

Height : 9.880

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch118

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	378
Mean	44.01
Std Dev	12.37

Turn on : 26.7525

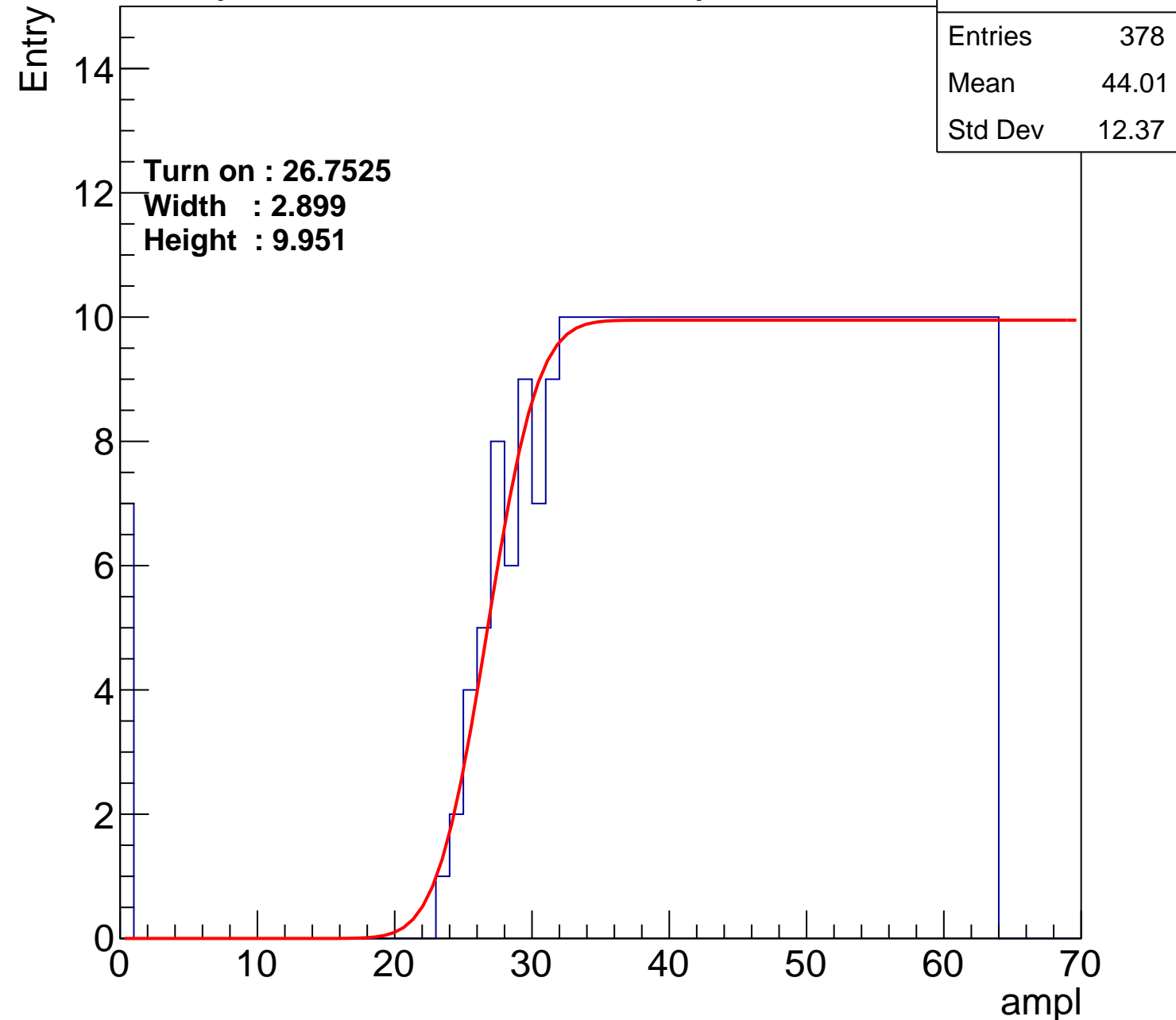
Width : 2.899

Height : 9.951

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U7-ch119

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	375
Mean	44.43
Std Dev	11.59

Turn on : 27.3276

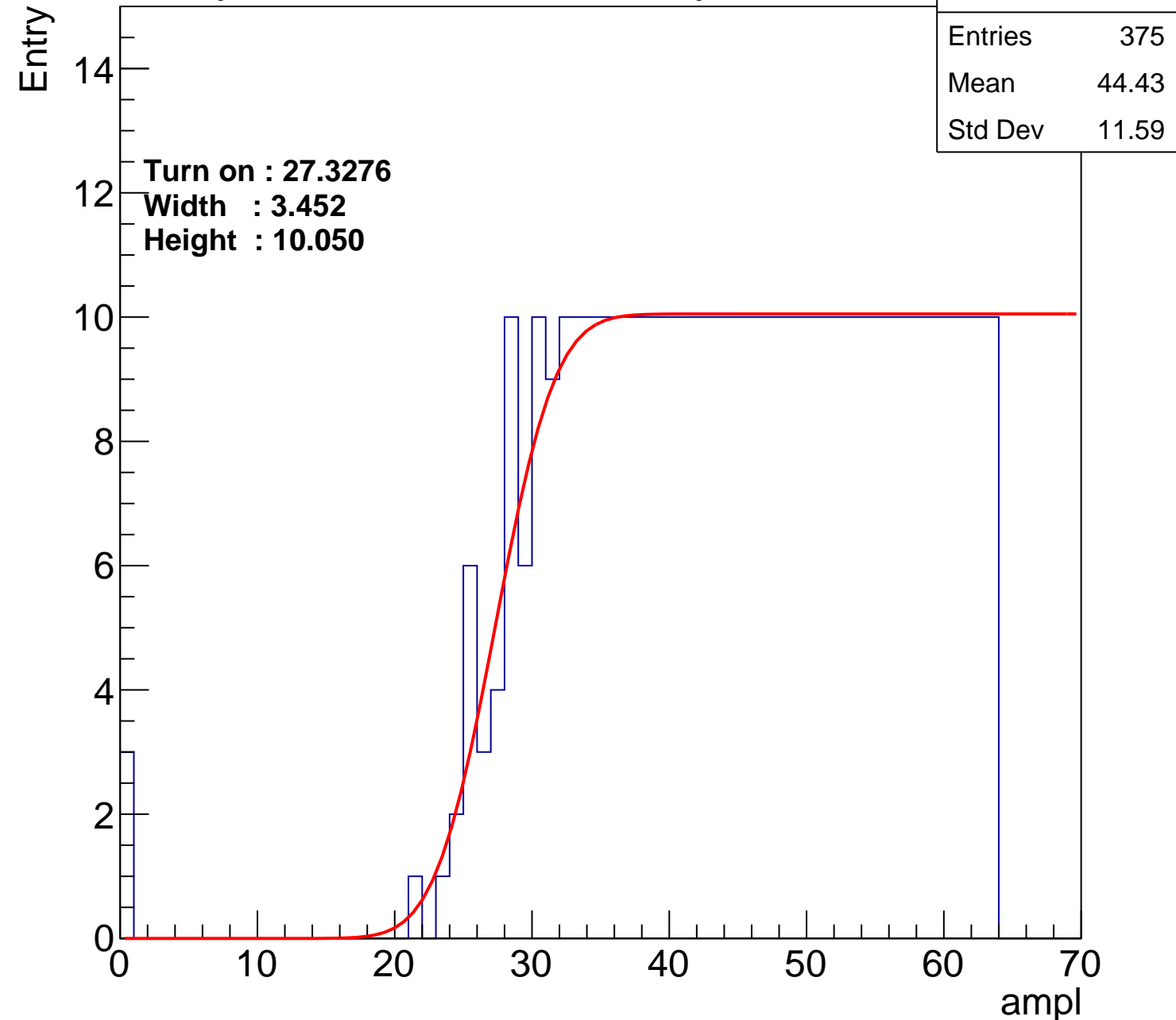
Width : 3.452

Height : 10.050

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch120

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	375
Mean	44.2
Std Dev	12.18

Turn on : 27.3825

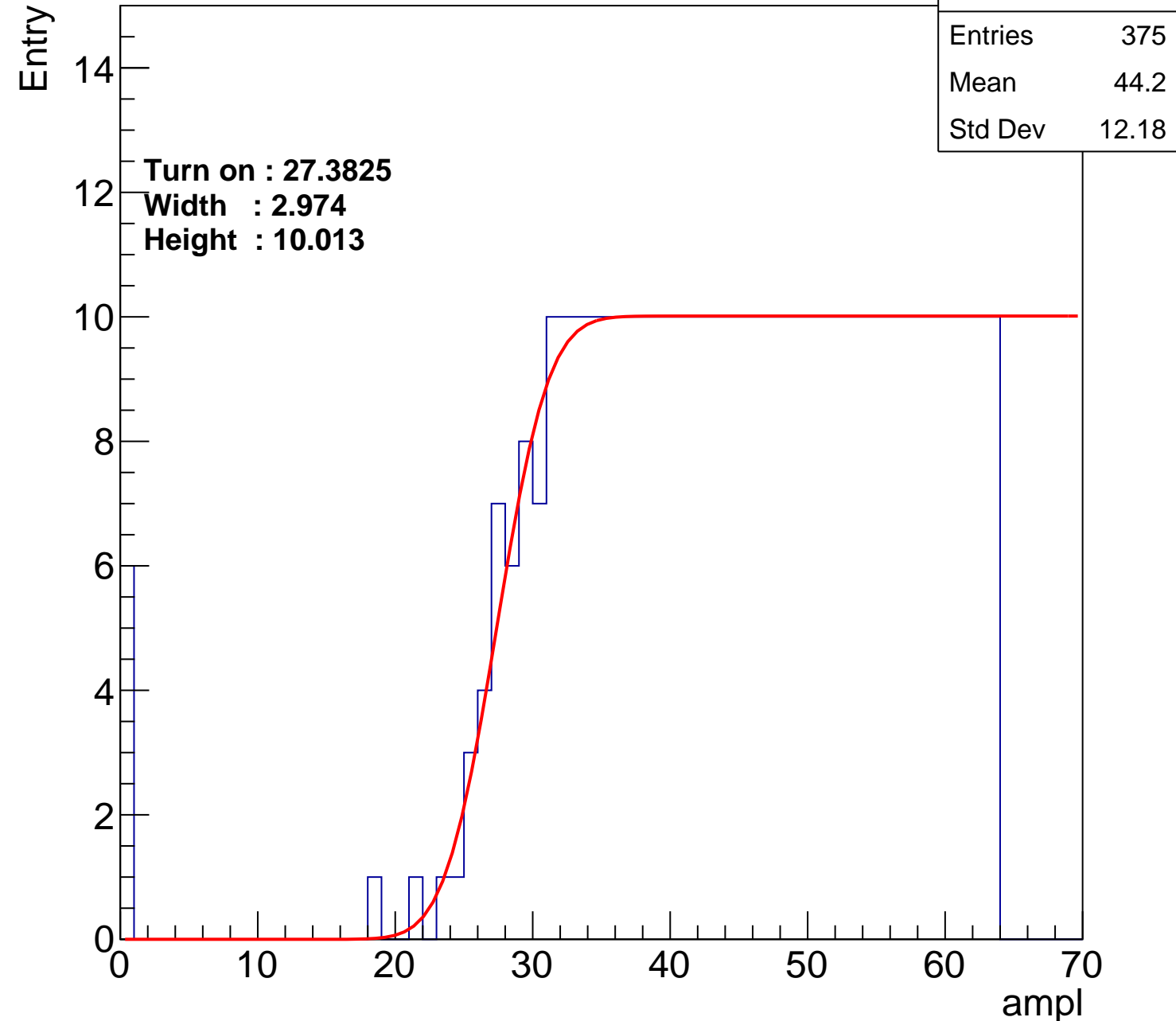
Width : 2.974

Height : 10.013

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch121

calib\_packv5\_042523\_0143.root, FC#0, port D2

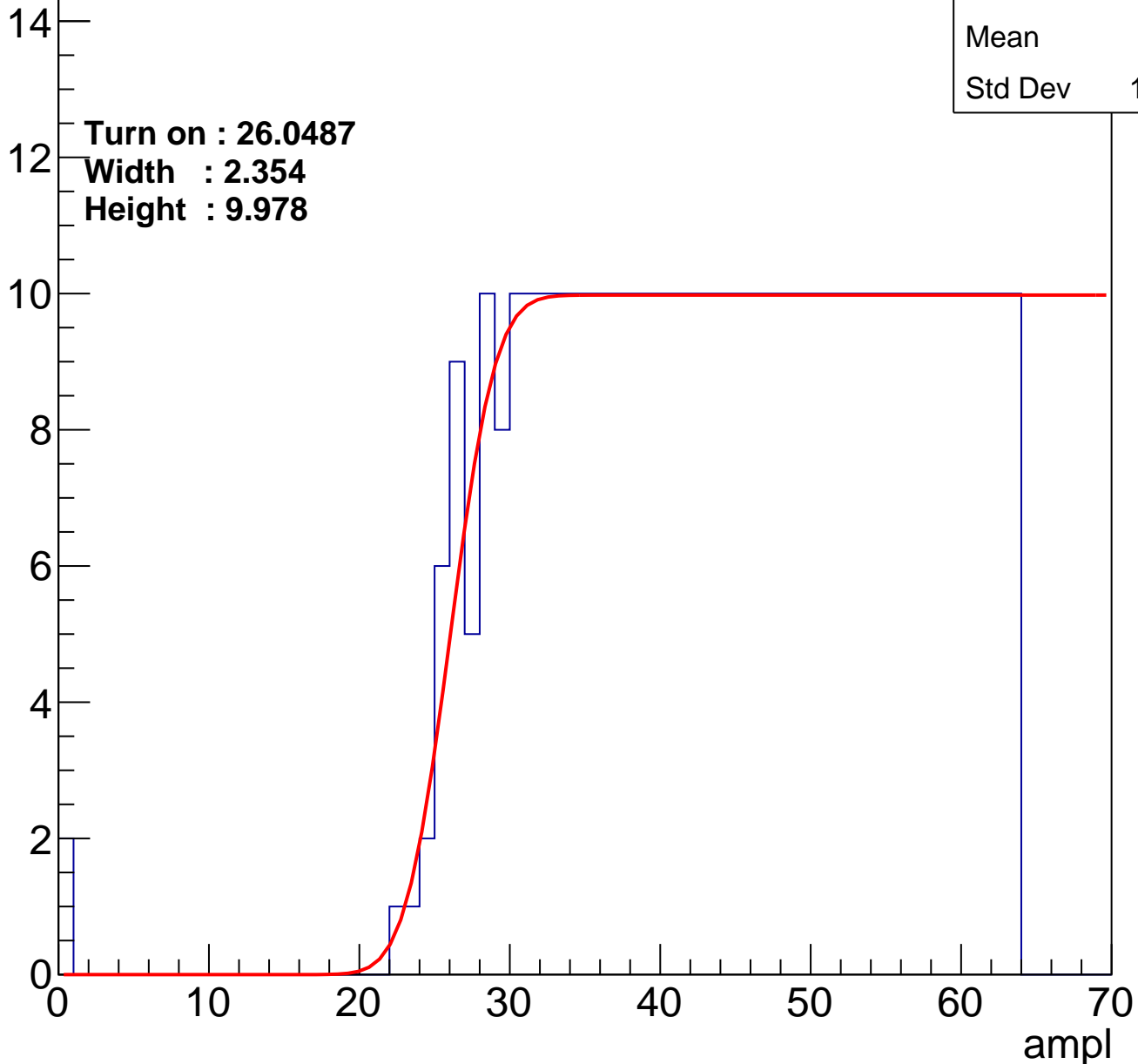
Entries	384
Mean	44.1
Std Dev	11.56

**Turn on : 26.0487**

**Width : 2.354**

**Height : 9.978**

Entry



# B1L101S, U7-ch122

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	387
Mean	43.74
Std Dev	12.18

Turn on : 25.7356

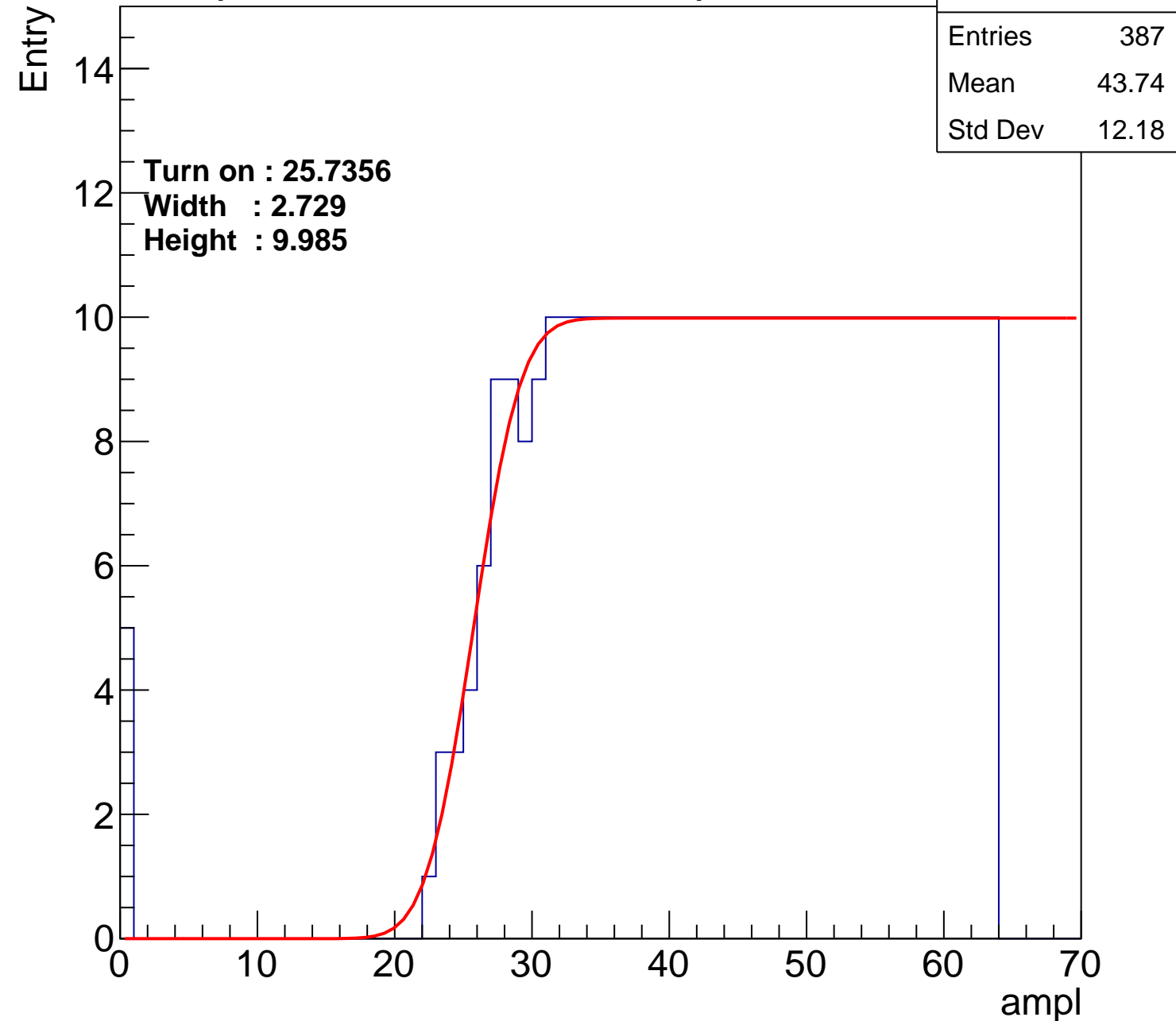
Width : 2.729

Height : 9.985

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch123

calib\_packv5\_042523\_0143.root, FC#0, port D2

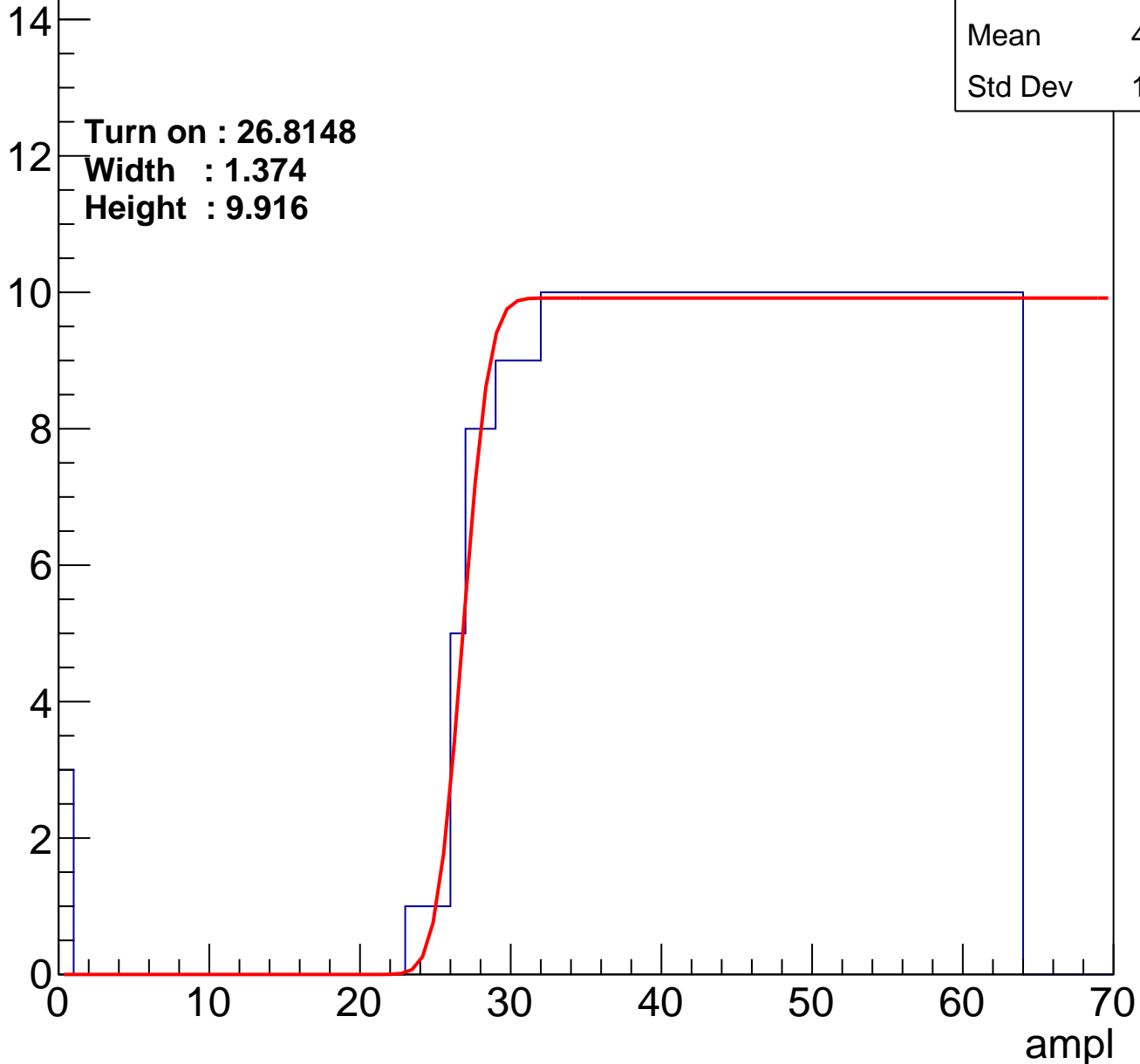
Entries	374
Mean	44.52
Std Dev	11.49

**Turn on : 26.8148**

**Width : 1.374**

**Height : 9.916**

Entry



# B1L101S, U7-ch124

calib\_packv5\_042523\_0143.root, FC#0, port D2

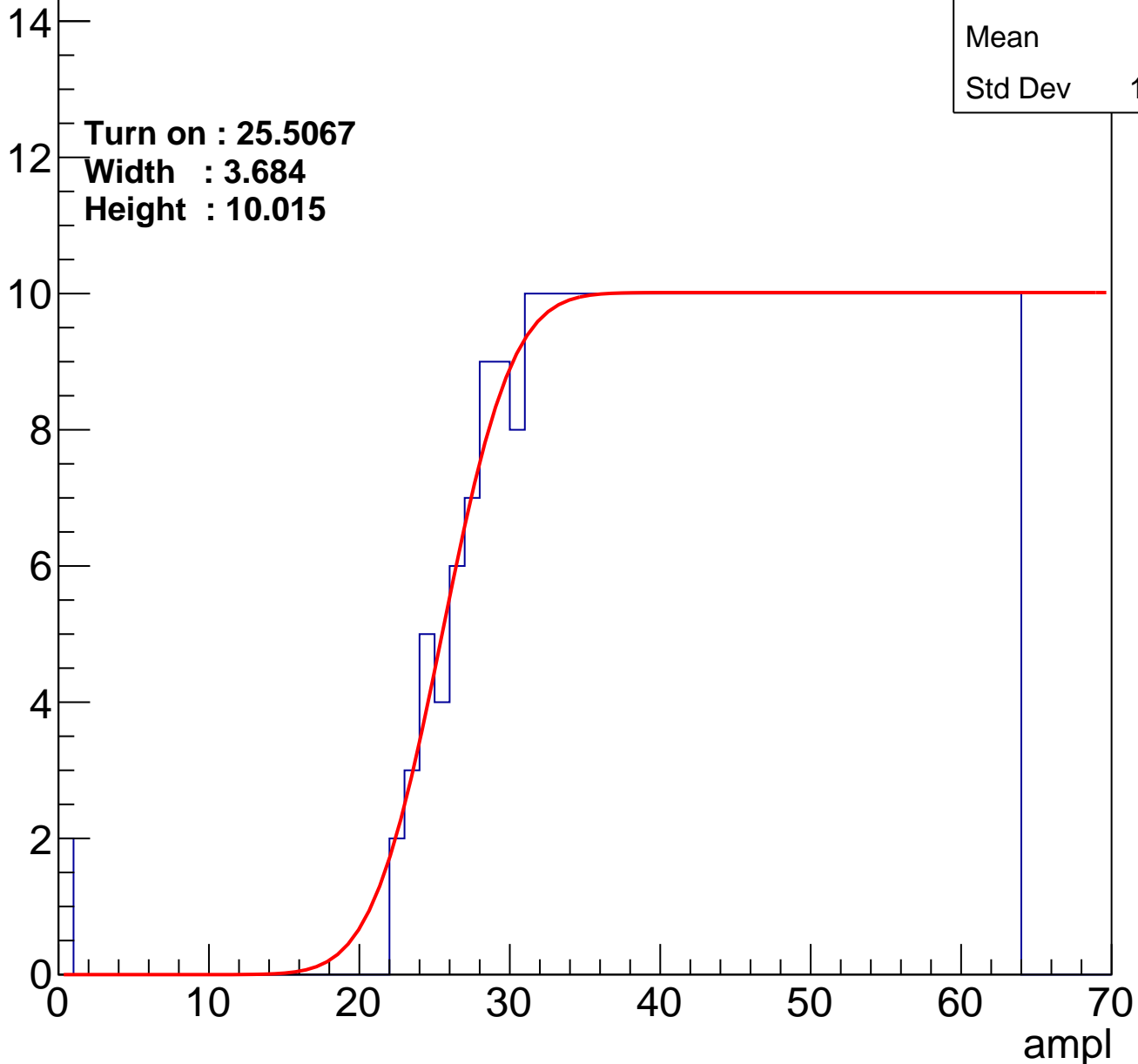
Entries	385
Mean	44
Std Dev	11.66

Turn on : 25.5067

Width : 3.684

Height : 10.015

Entry



# B1L101S, U7-ch125

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	367
Mean	44.79
Std Dev	11.44

Turn on : 28.0367

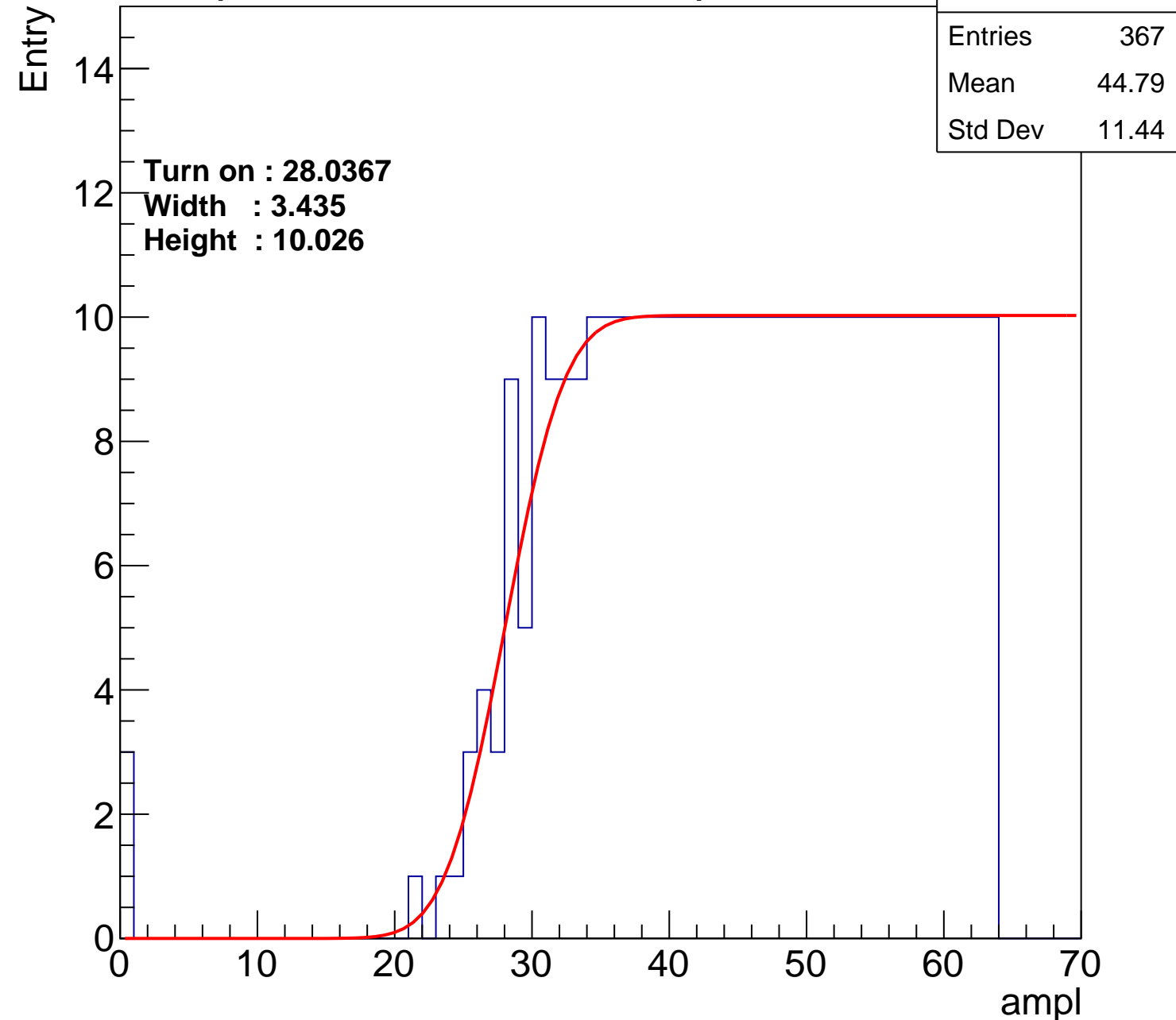
Width : 3.435

Height : 10.026

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch126

calib\_packv5\_042523\_0143.root, FC#0, port D2

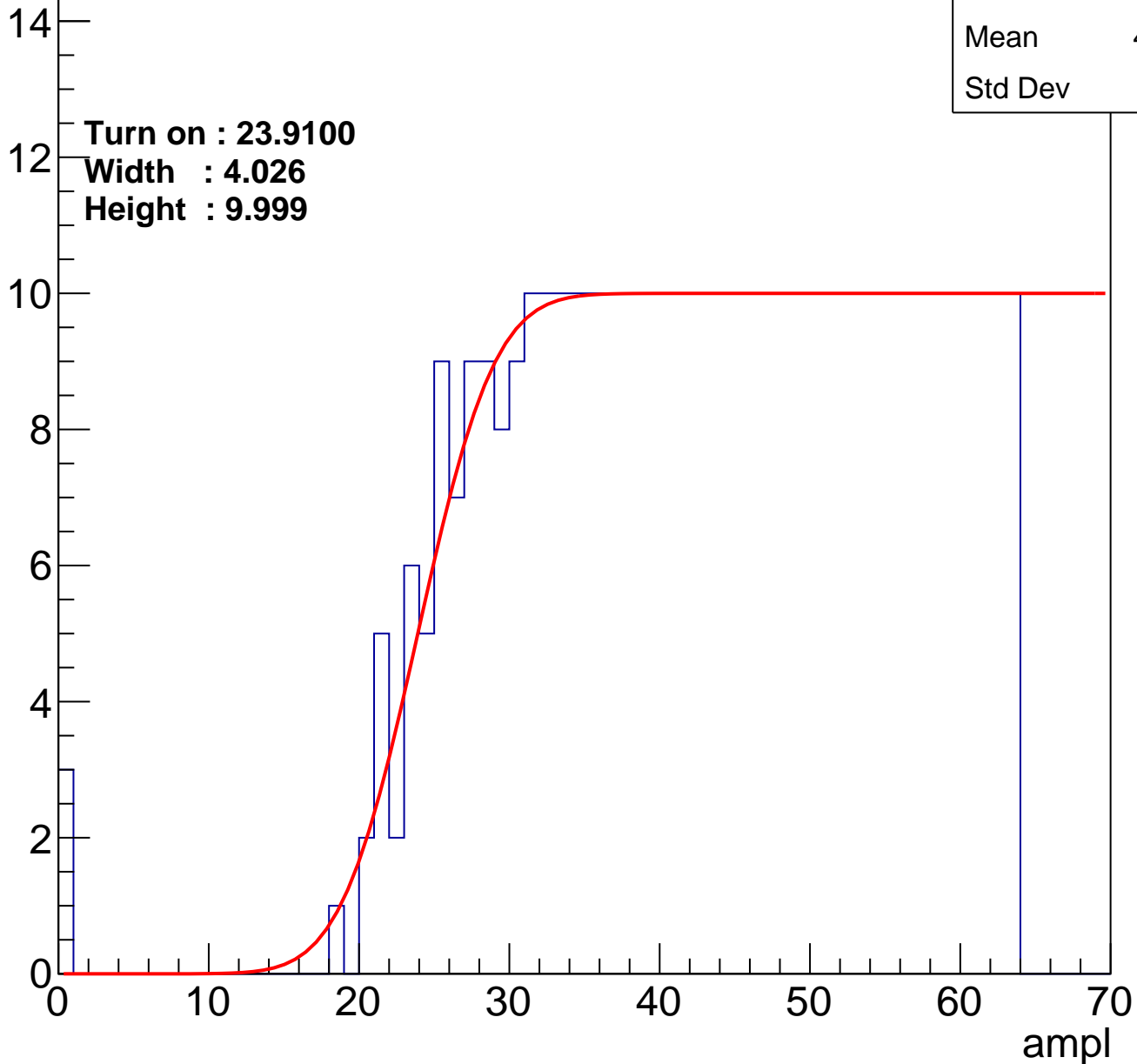
Entries	405
Mean	42.91
Std Dev	12.4

Turn on : 23.9100

Width : 4.026

Height : 9.999

Entry





# B1L101S, U7-ch127

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	380
Mean	44.14
Std Dev	11.78

**Turn on : 26.5941**

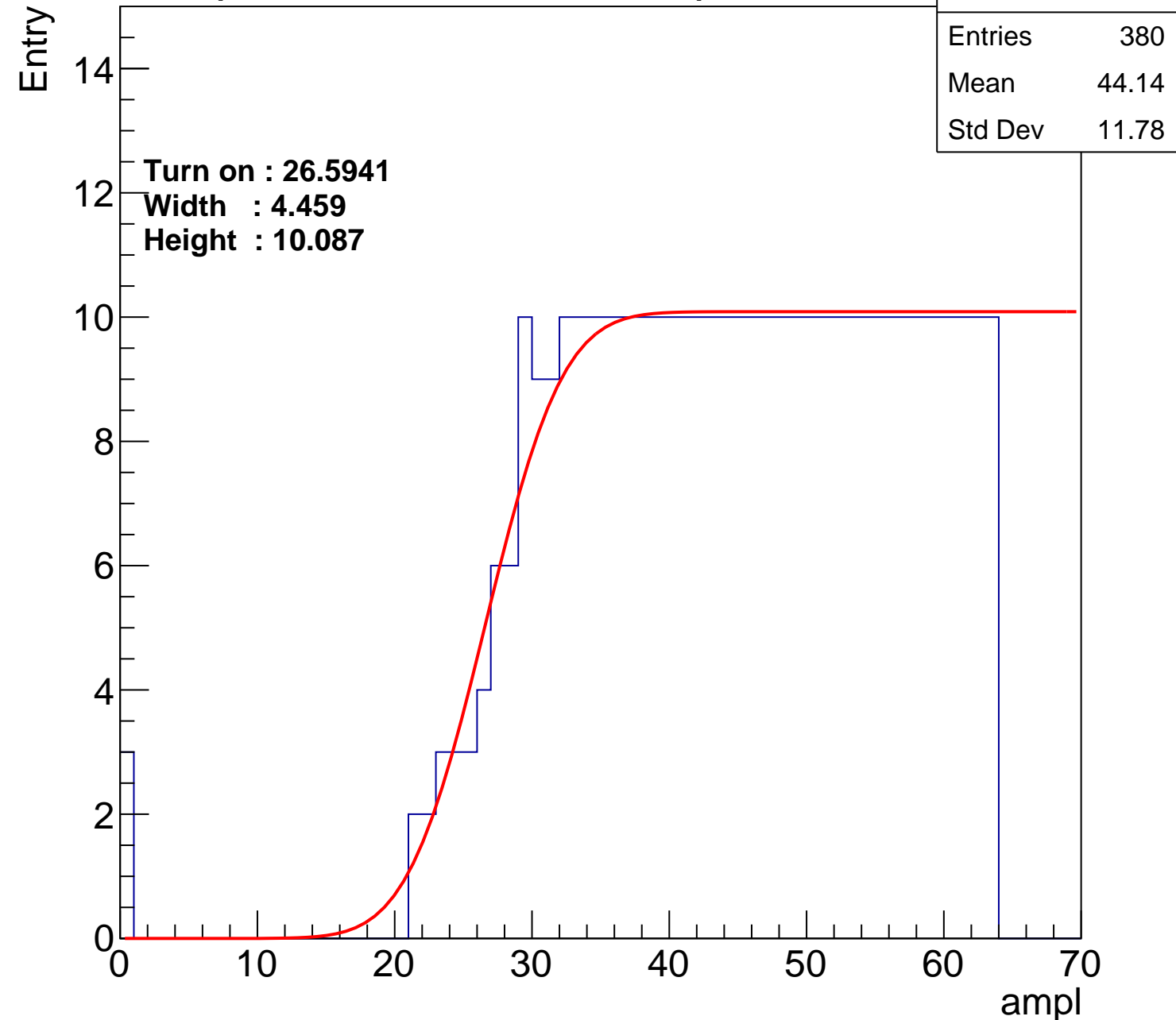
**Width : 4.459**

**Height : 10.087**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U7-ch127

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	380
Mean	44.14
Std Dev	11.78

Turn on : 26.5941

Width : 4.459

Height : 10.087

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

