



# B1L100S, U13-ch0

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	388
Mean	43.79
Std Dev	11.98

Turn on : 25.5111

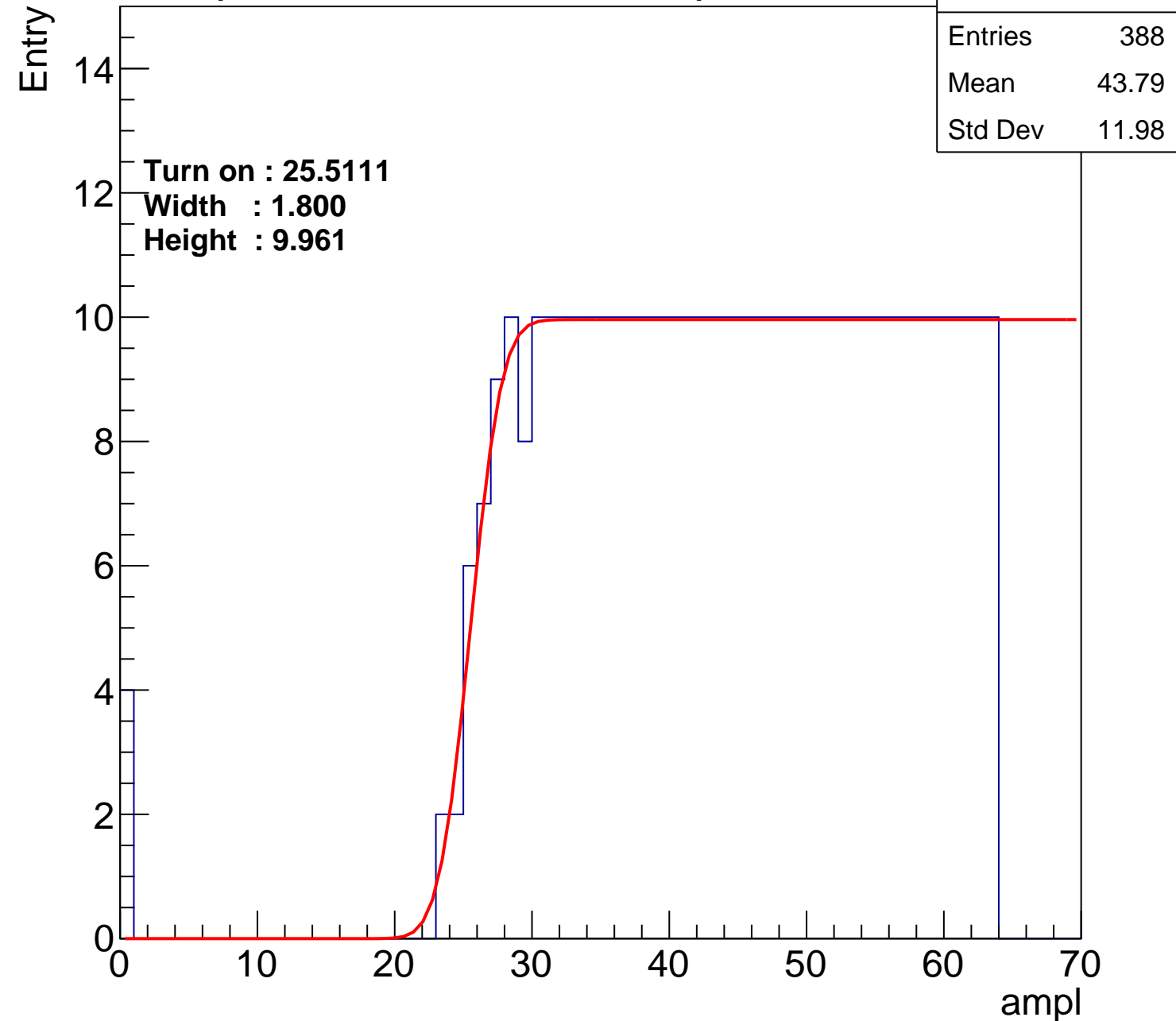
Width : 1.800

Height : 9.961

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch1

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	364
Mean	44.99
Std Dev	11.29

Turn on : 27.8556

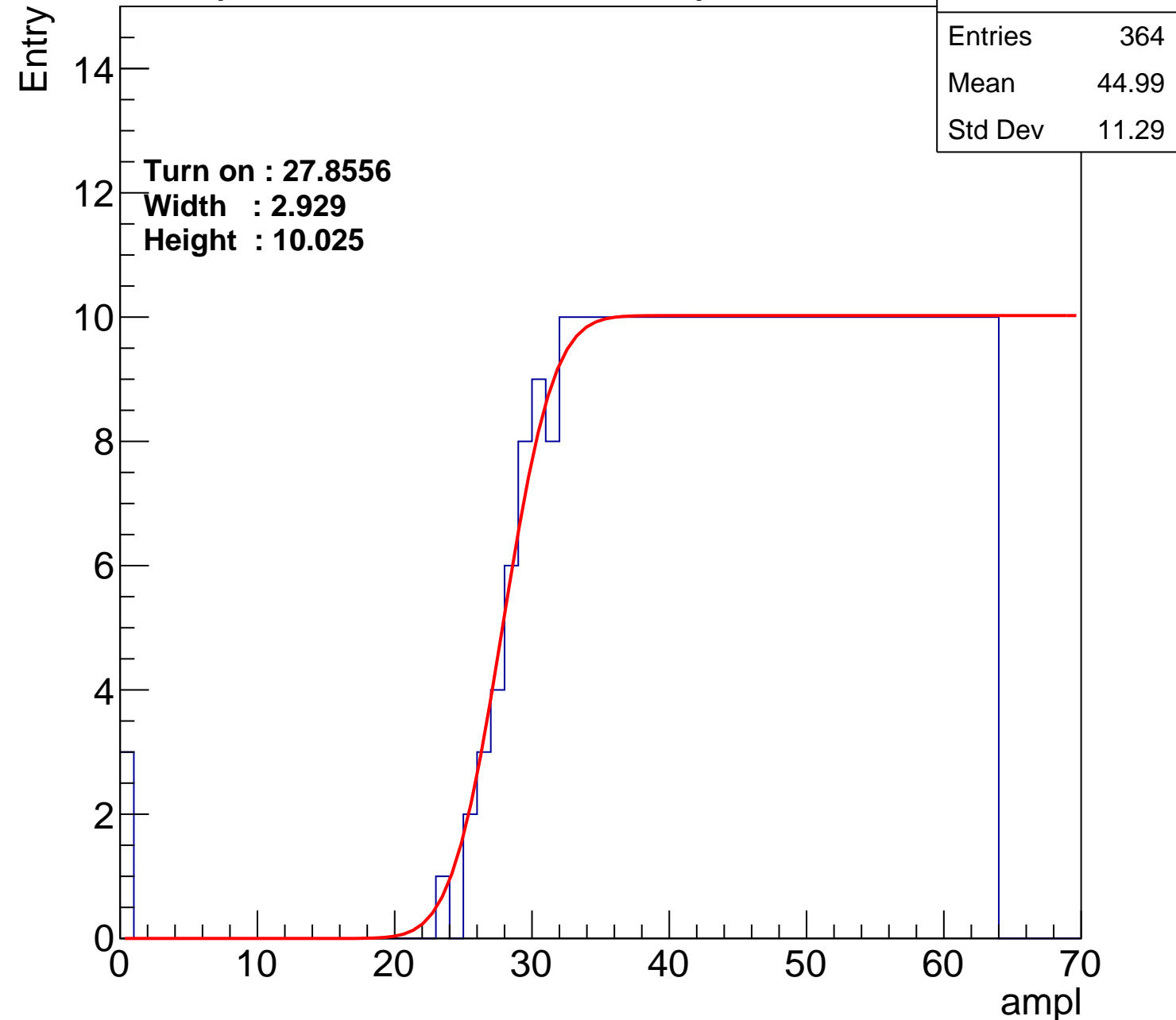
Width : 2.929

Height : 10.025

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch2

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	385
Mean	44.02
Std Dev	11.64

**Turn on : 26.4182**

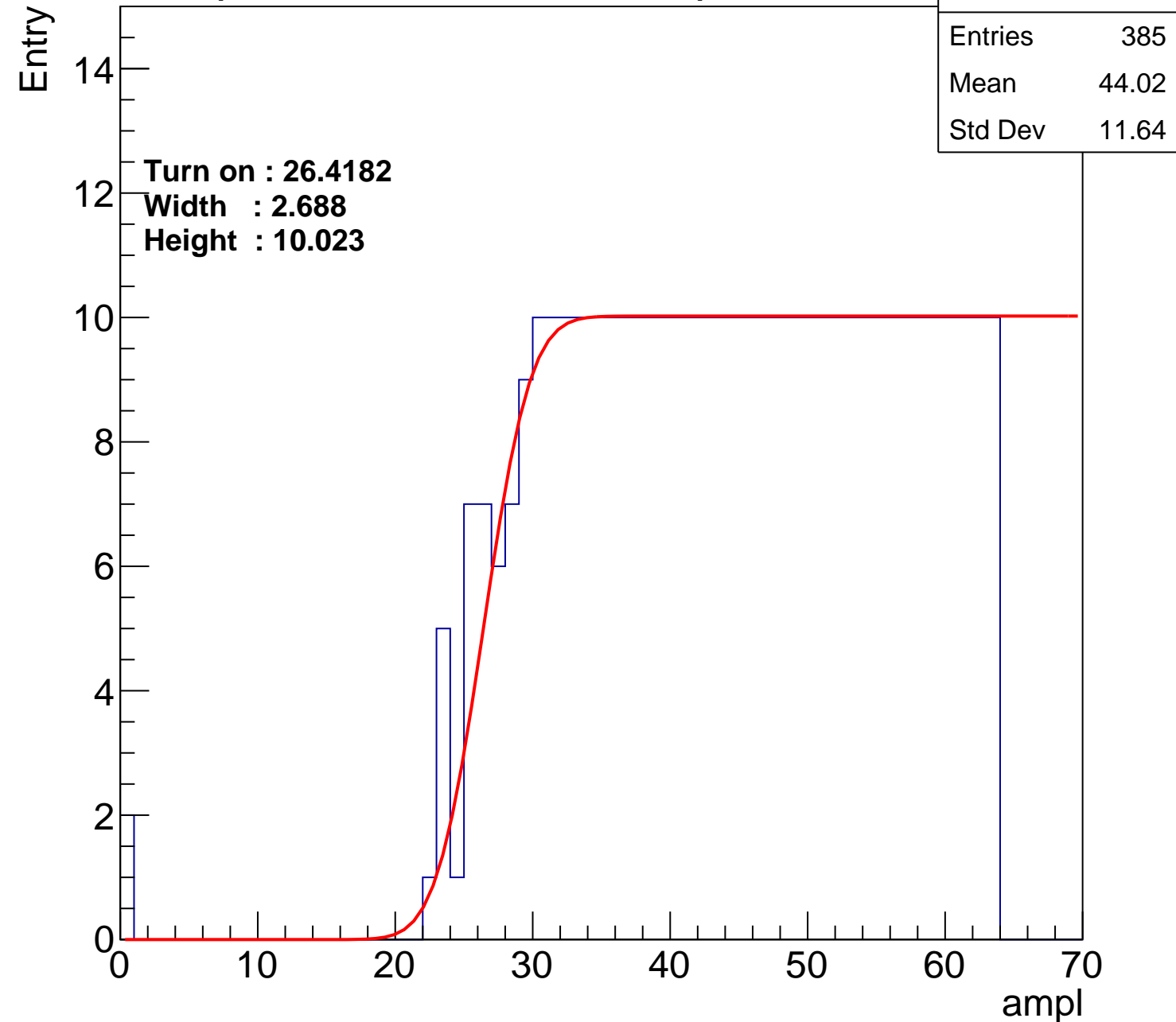
**Width : 2.688**

**Height : 10.023**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch3

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	367
Mean	44.89
Std Dev	11.2

Turn on : 28.2194

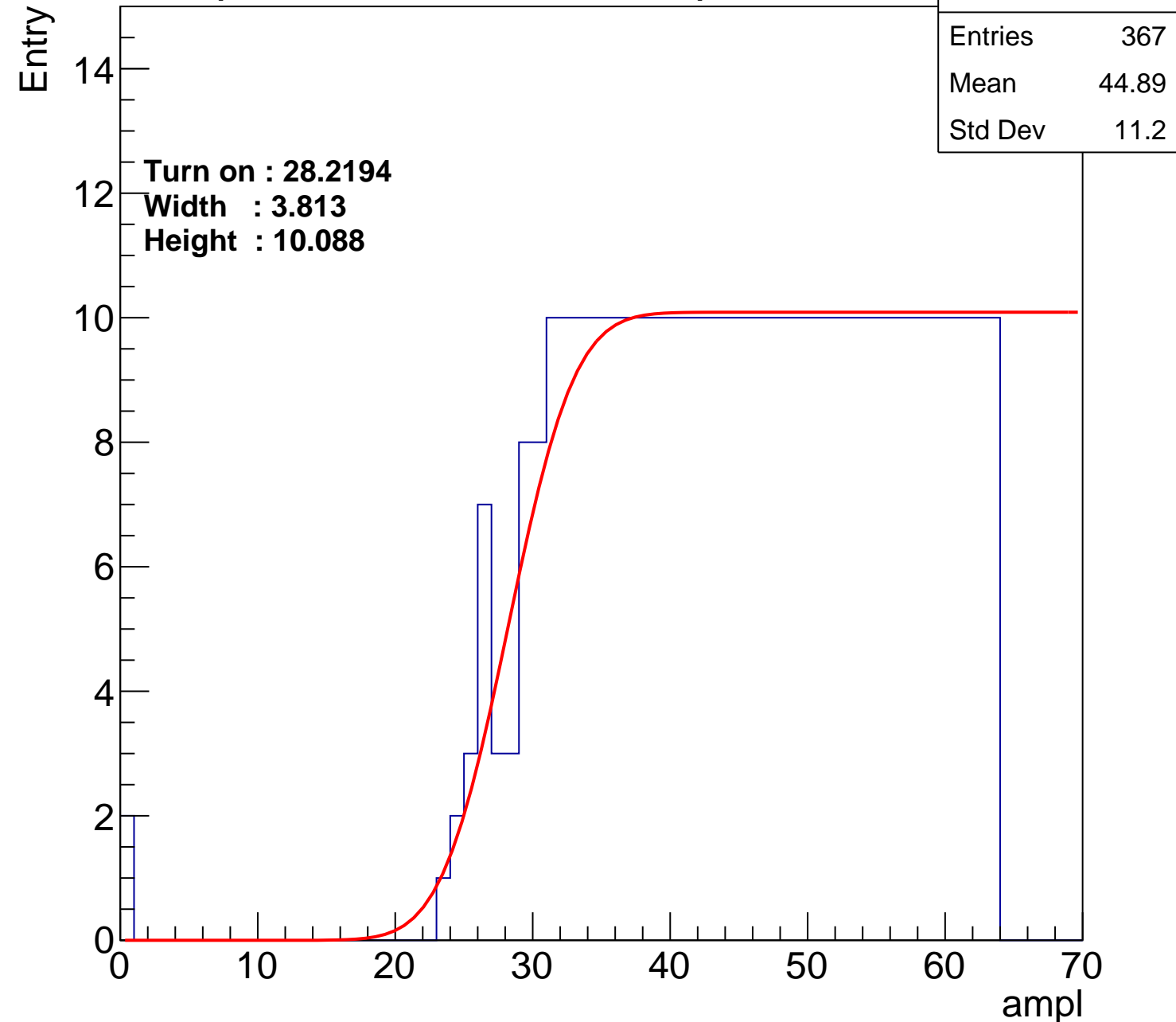
Width : 3.813

Height : 10.088

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch4

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	373
Mean	44.5
Std Dev	11.58

Turn on : 26.7468

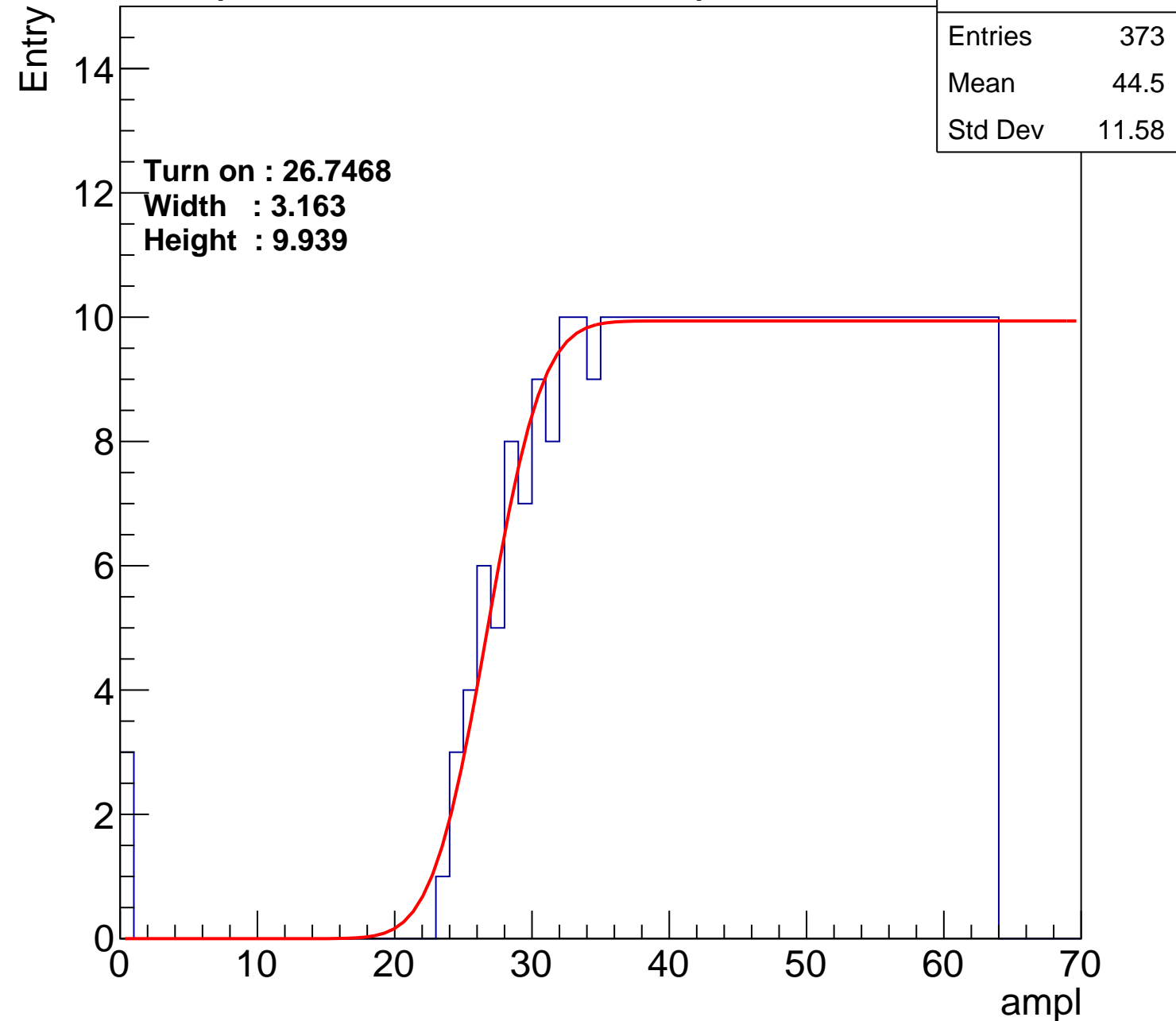
Width : 3.163

Height : 9.939

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch5

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	359
Mean	45.28
Std Dev	11

**Turn on : 28.9764**

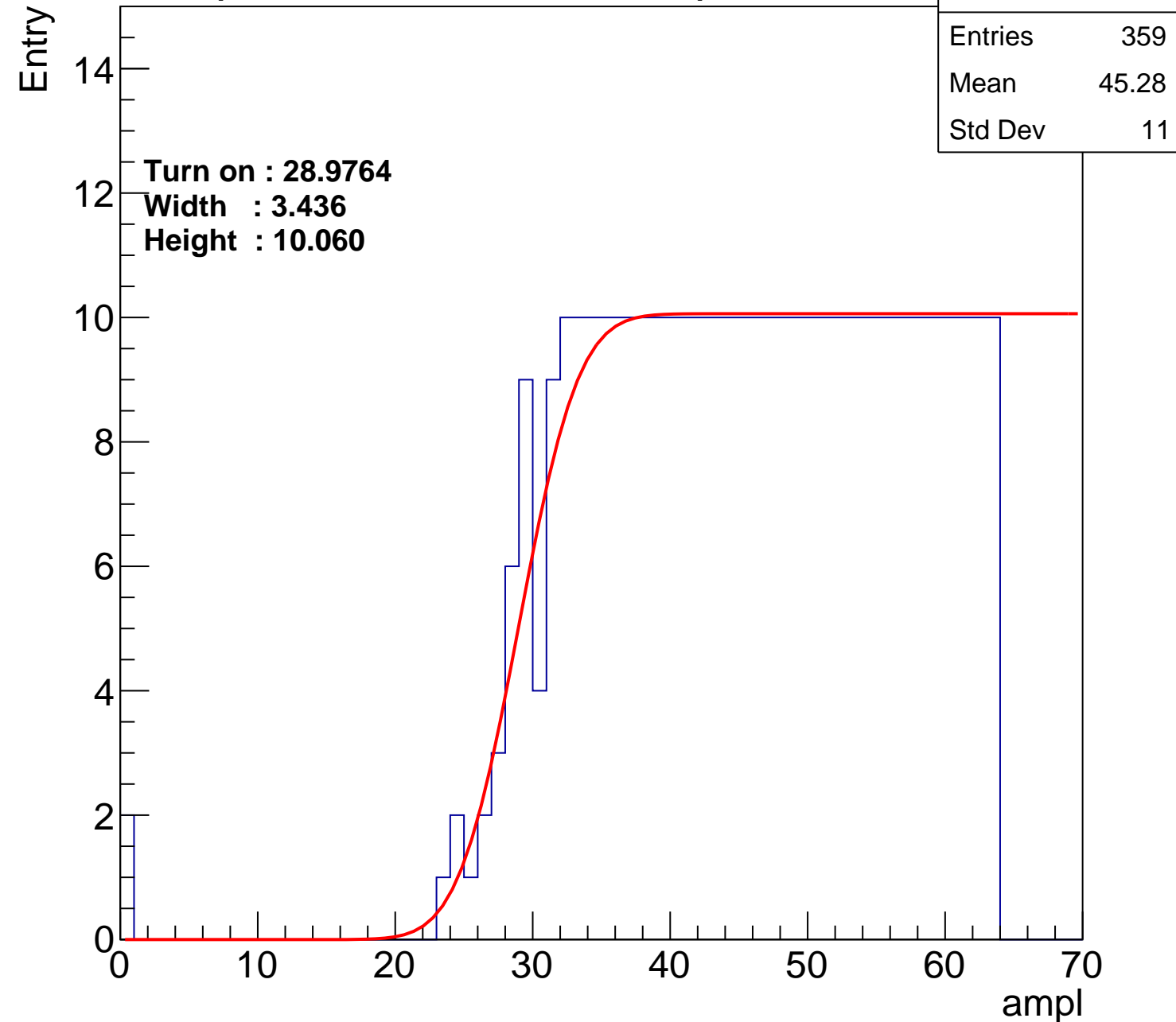
**Width : 3.436**

**Height : 10.060**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch6

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	386
Mean	43.92
Std Dev	11.82

**Turn on : 26.3979**

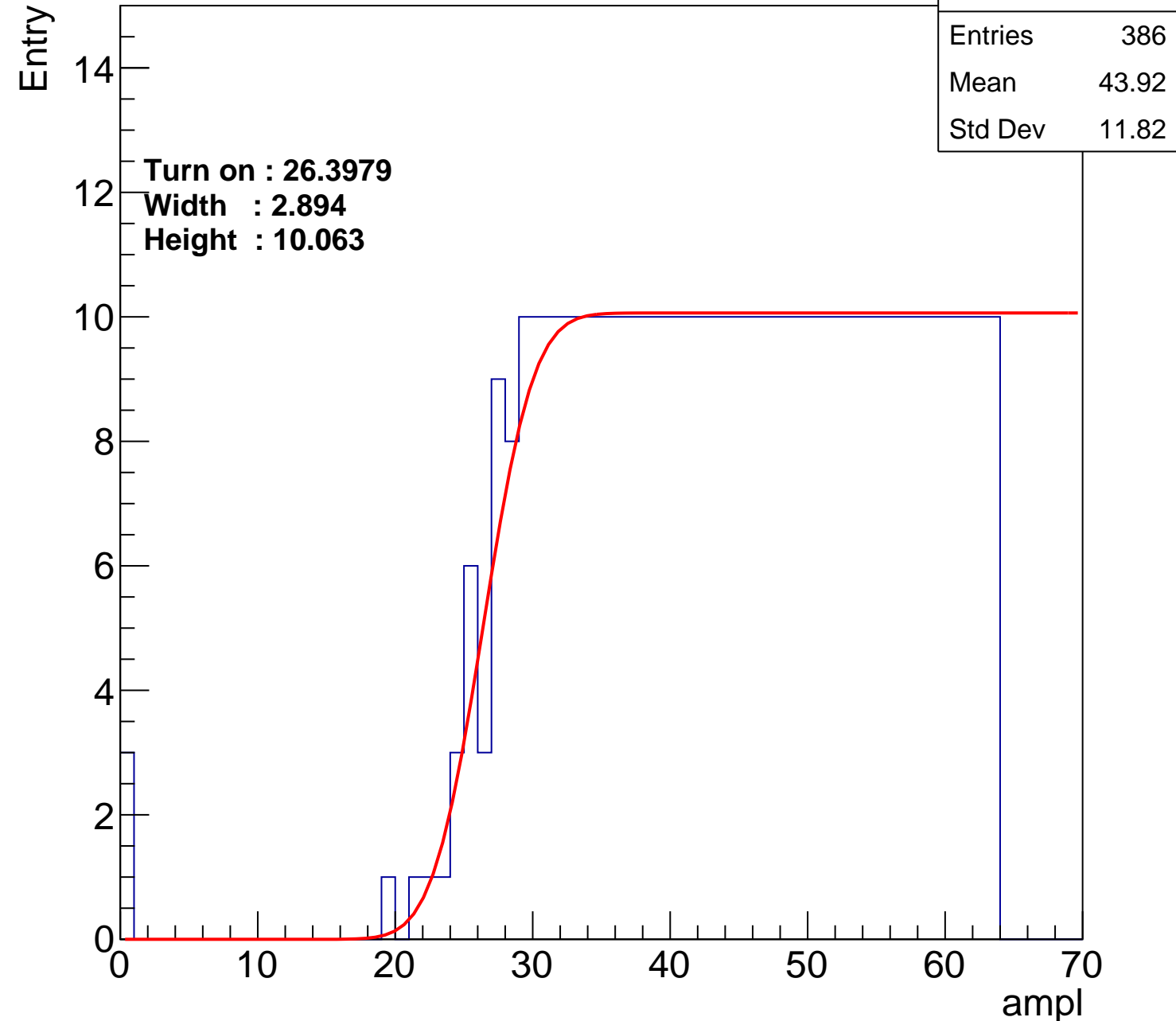
**Width : 2.894**

**Height : 10.063**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U13-ch7

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	374
Mean	44.63
Std Dev	11.16

**Turn on : 26.9844**

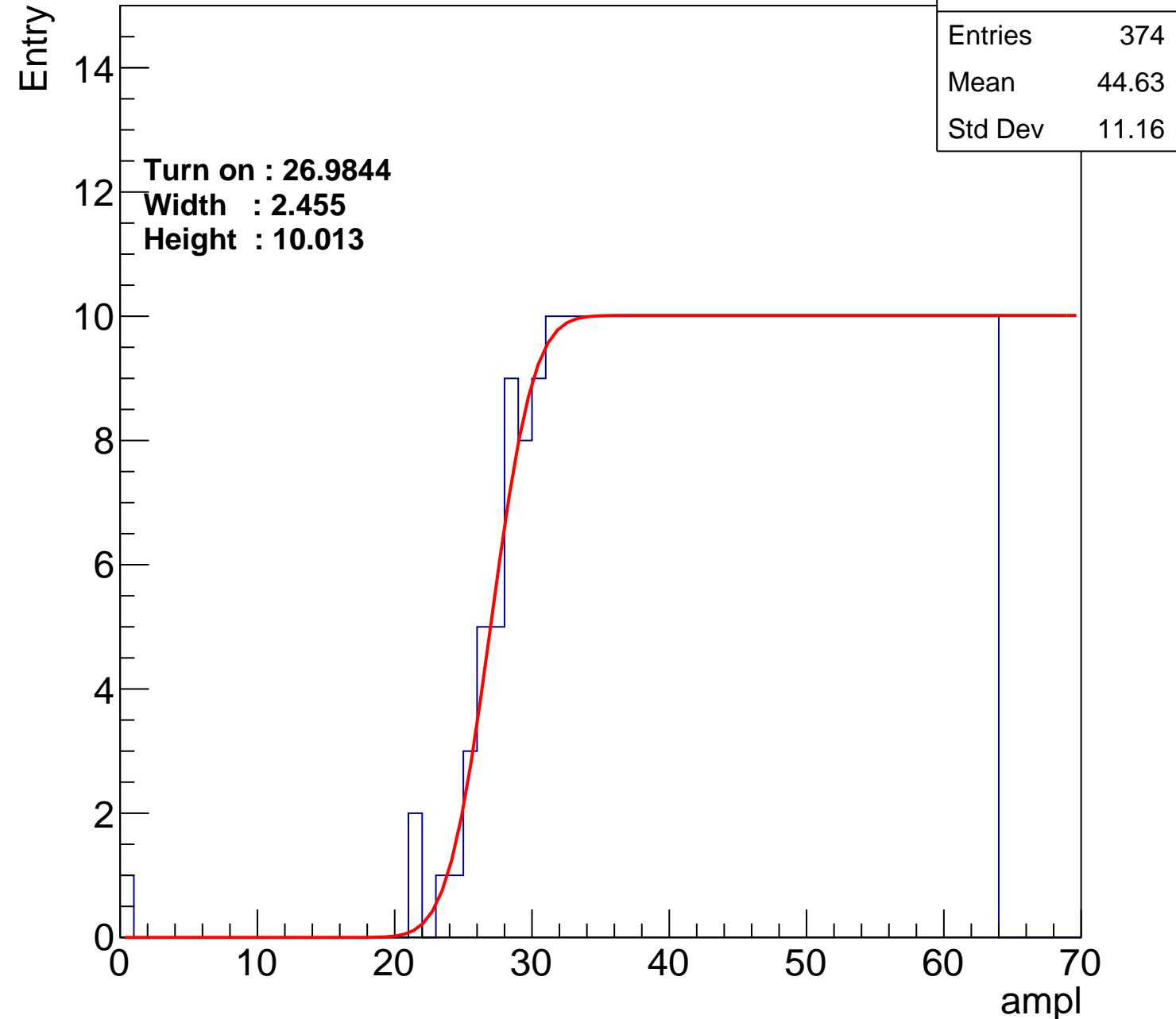
**Width : 2.455**

**Height : 10.013**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch8

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	379
Mean	44.14
Std Dev	11.91

Turn on : 27.0587

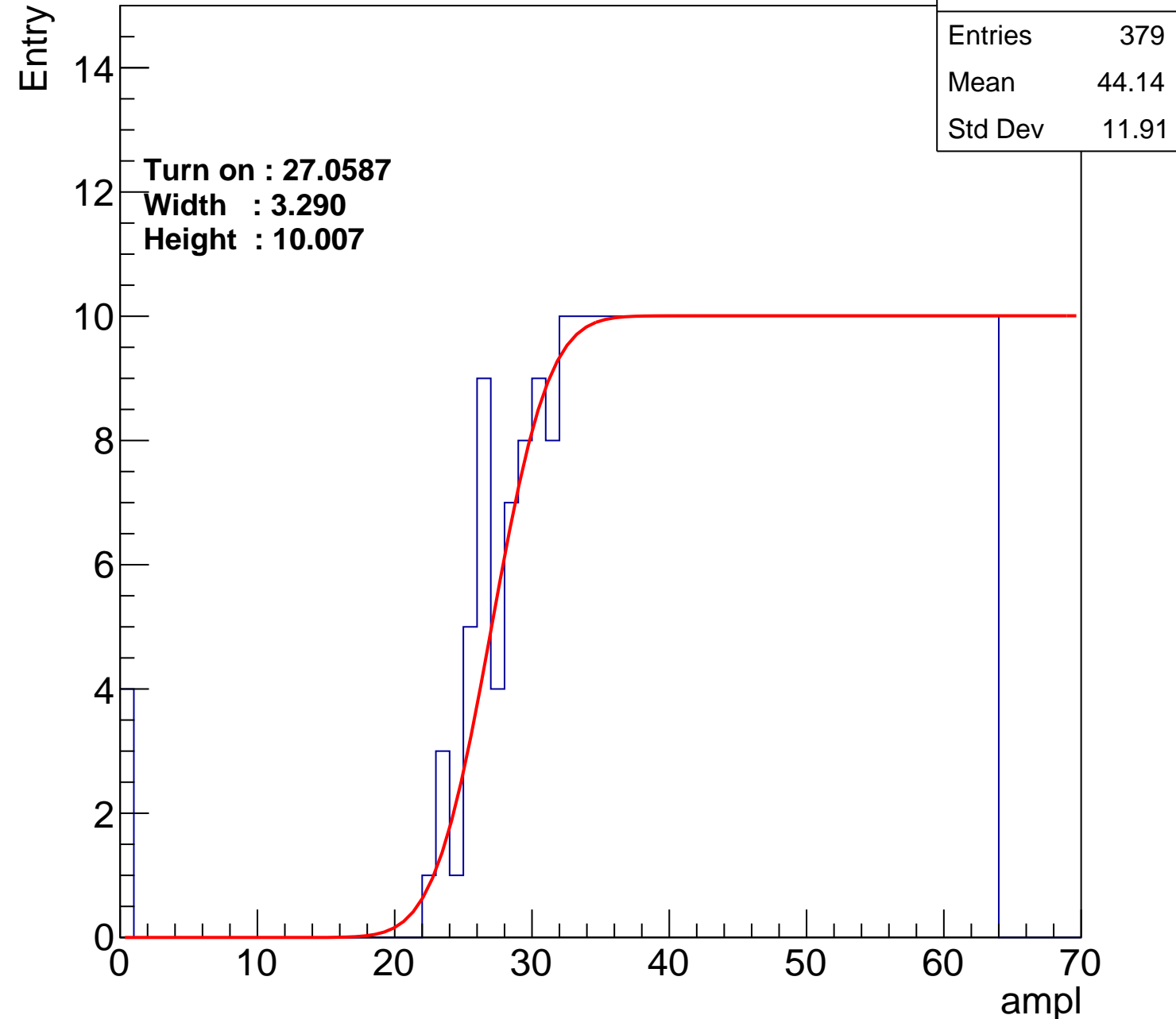
Width : 3.290

Height : 10.007

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch9

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	362
Mean	45.05
Std Dev	11.3

Turn on : 28.4148

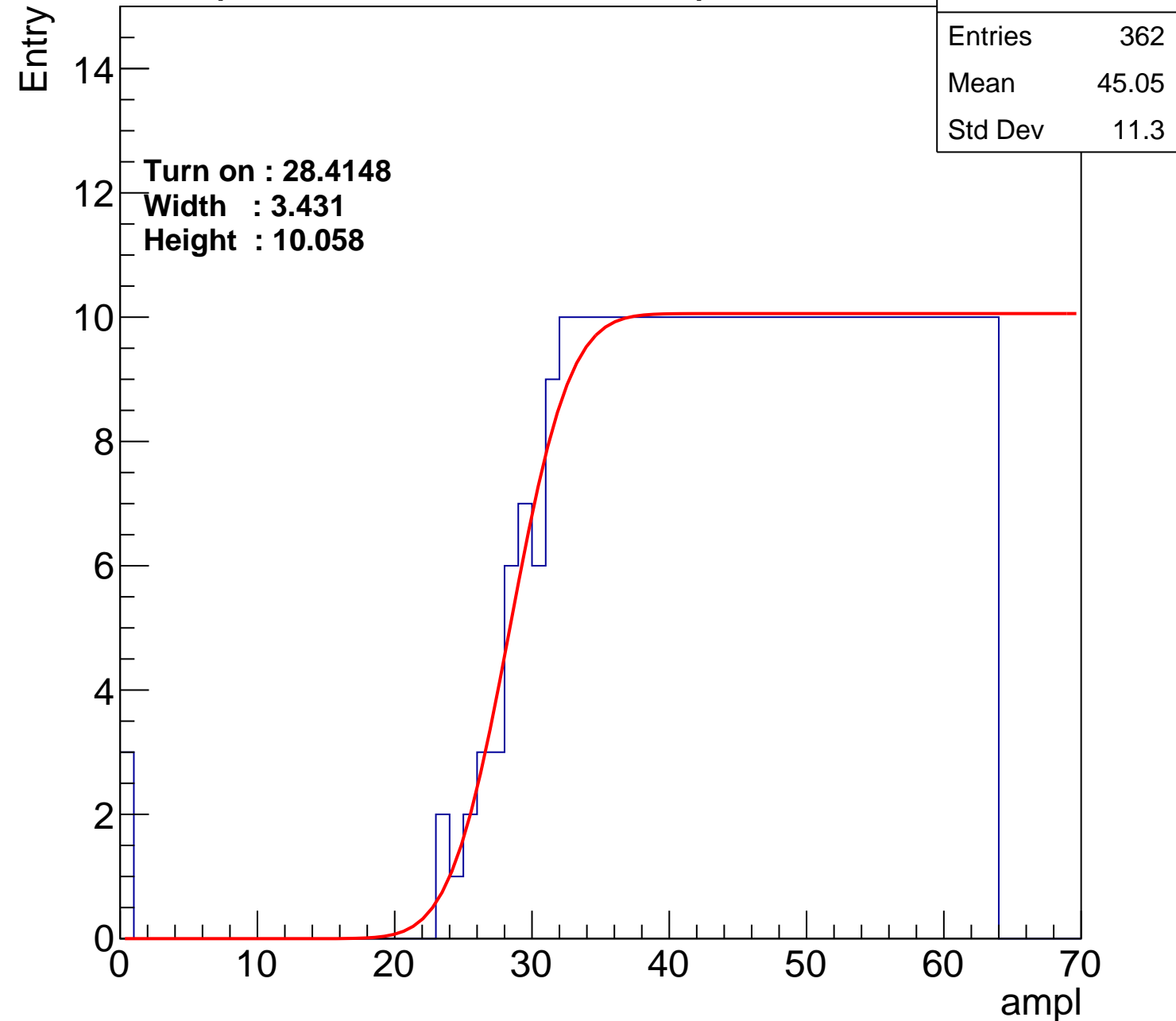
Width : 3.431

Height : 10.058

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



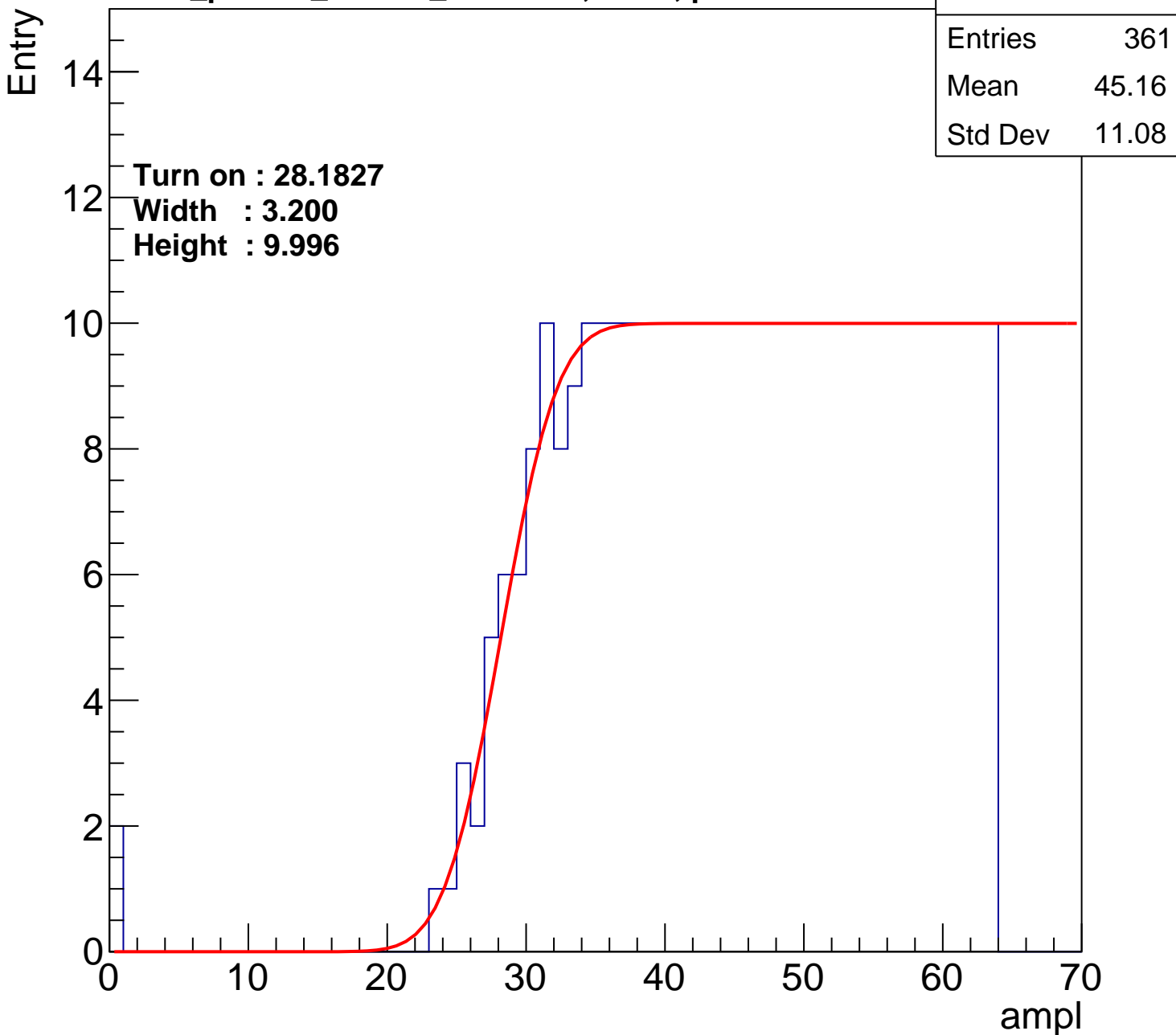
**calib\_packv5\_042523\_0143.root, FC#4, port A2**

**calib\_packv5\_042523\_0143.root, FC#4, port A2**

Entries	361
Mean	45.16
Std Dev	11.08

**Width : 3.200**

**Height : 9.996**



# B1L100S, U13-ch11

calib\_packv5\_042523\_0143.root, FC#4, port A2

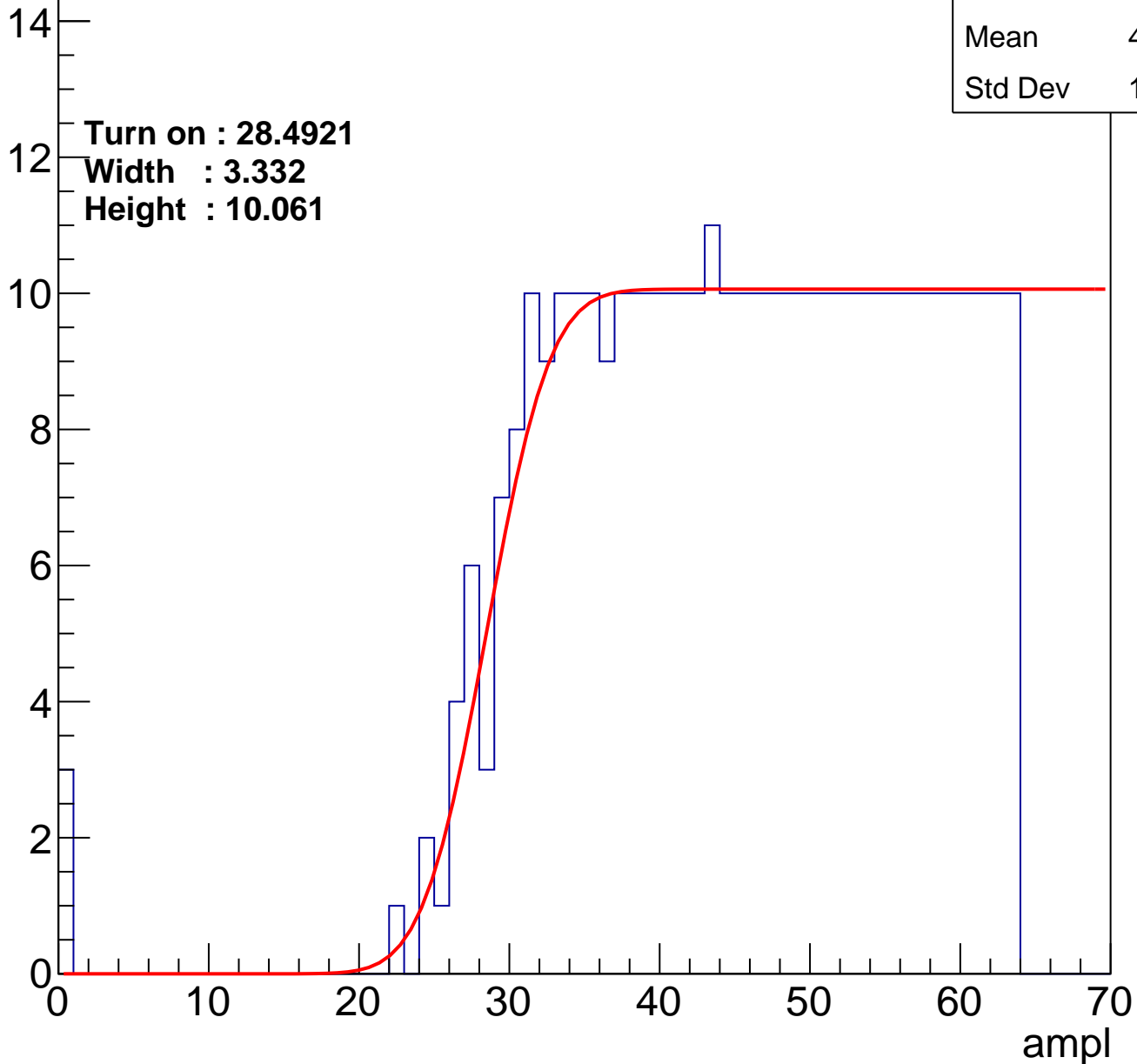
Entries	364
Mean	44.98
Std Dev	11.33

Turn on : 28.4921

Width : 3.332

Height : 10.061

Entry



# B1L100S, U13-ch12

calib\_packv5\_042523\_0143.root, FC#4, port A2

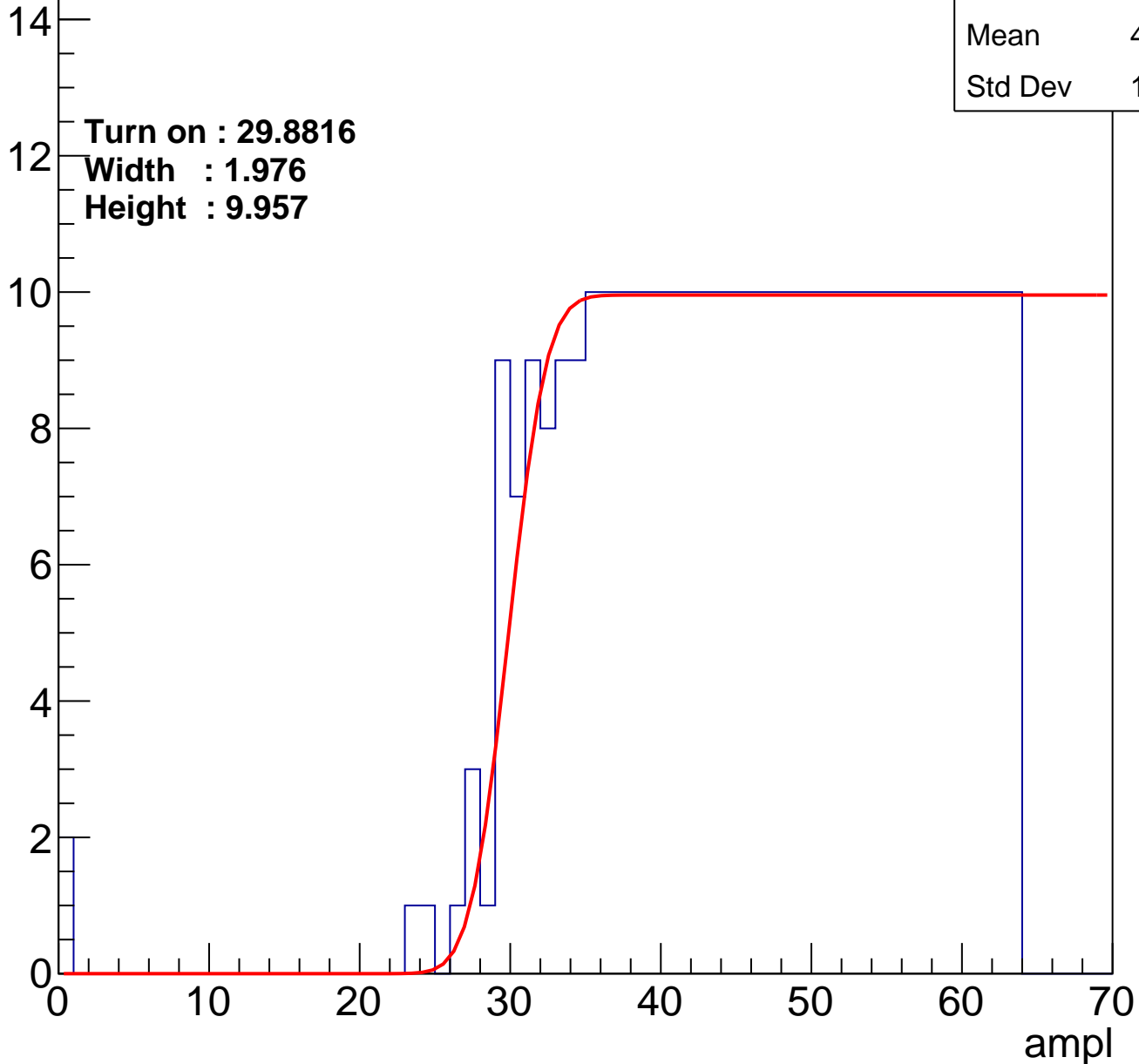
Entries	350
Mean	45.72
Std Dev	10.79

Turn on : 29.8816

Width : 1.976

Height : 9.957

Entry



# B1L100S, U13-ch13

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	368
Mean	44.95
Std Dev	10.97

Turn on : 27.5302

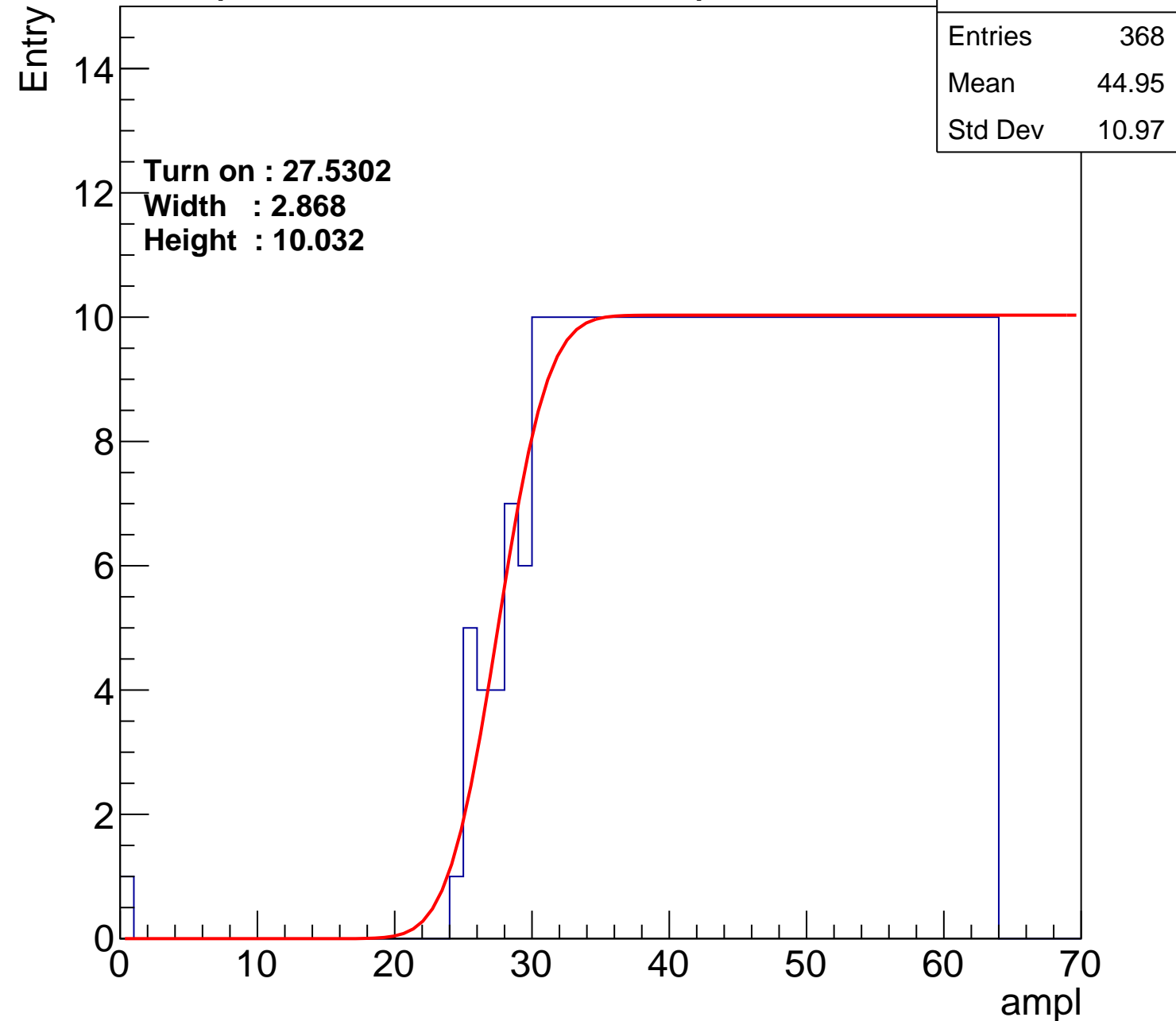
Width : 2.868

Height : 10.032

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch14

calib\_packv5\_042523\_0143.root, FC#4, port A2

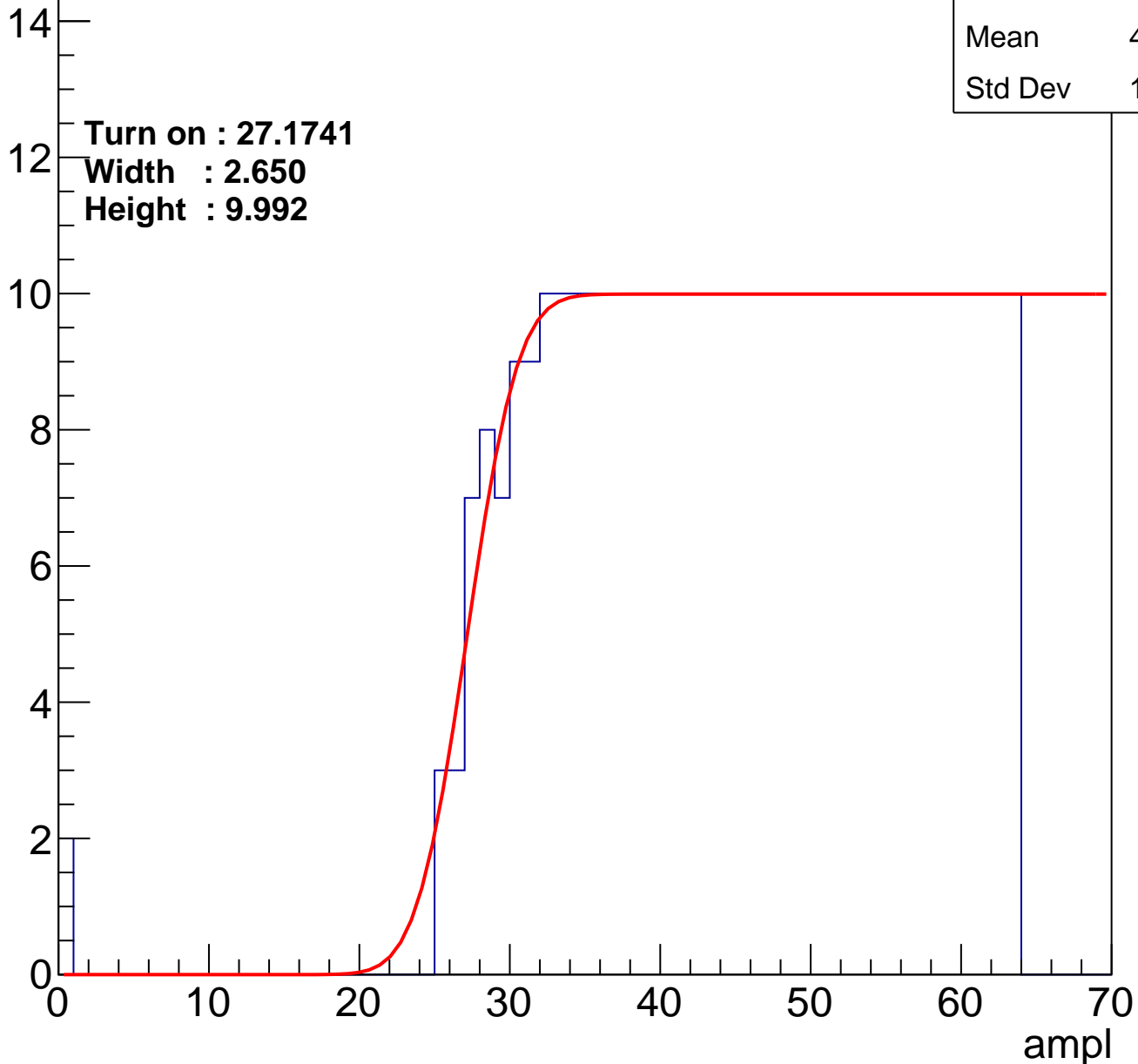
Entries	368
Mean	44.89
Std Dev	11.15

Turn on : 27.1741

Width : 2.650

Height : 9.992

Entry





# B1L100S, U13-ch15

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	369
Mean	44.81
Std Dev	11.23

Turn on : 27.1678

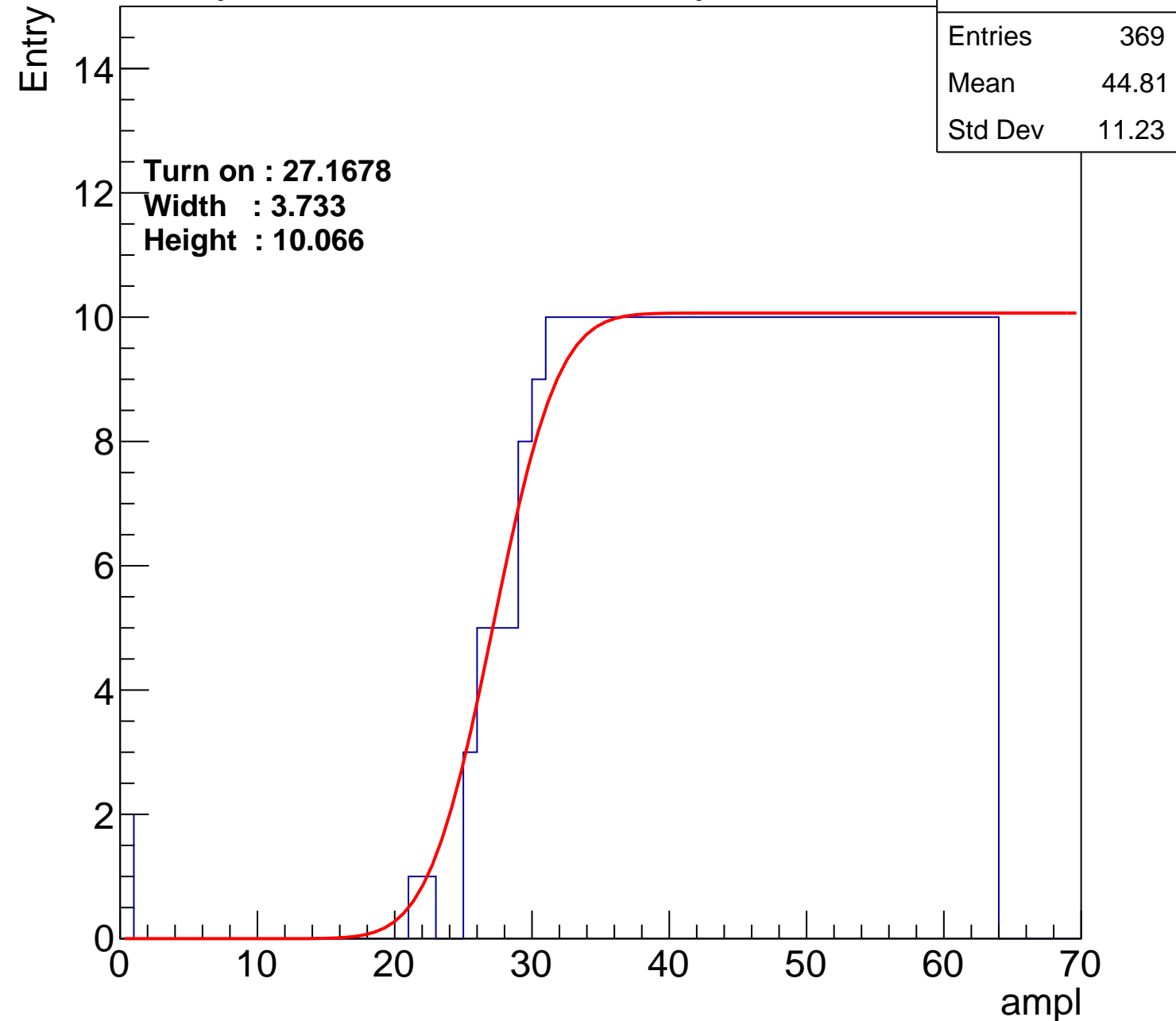
Width : 3.733

Height : 10.066

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch16

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	373
Mean	44.61
Std Dev	11.33

Turn on : 26.9915

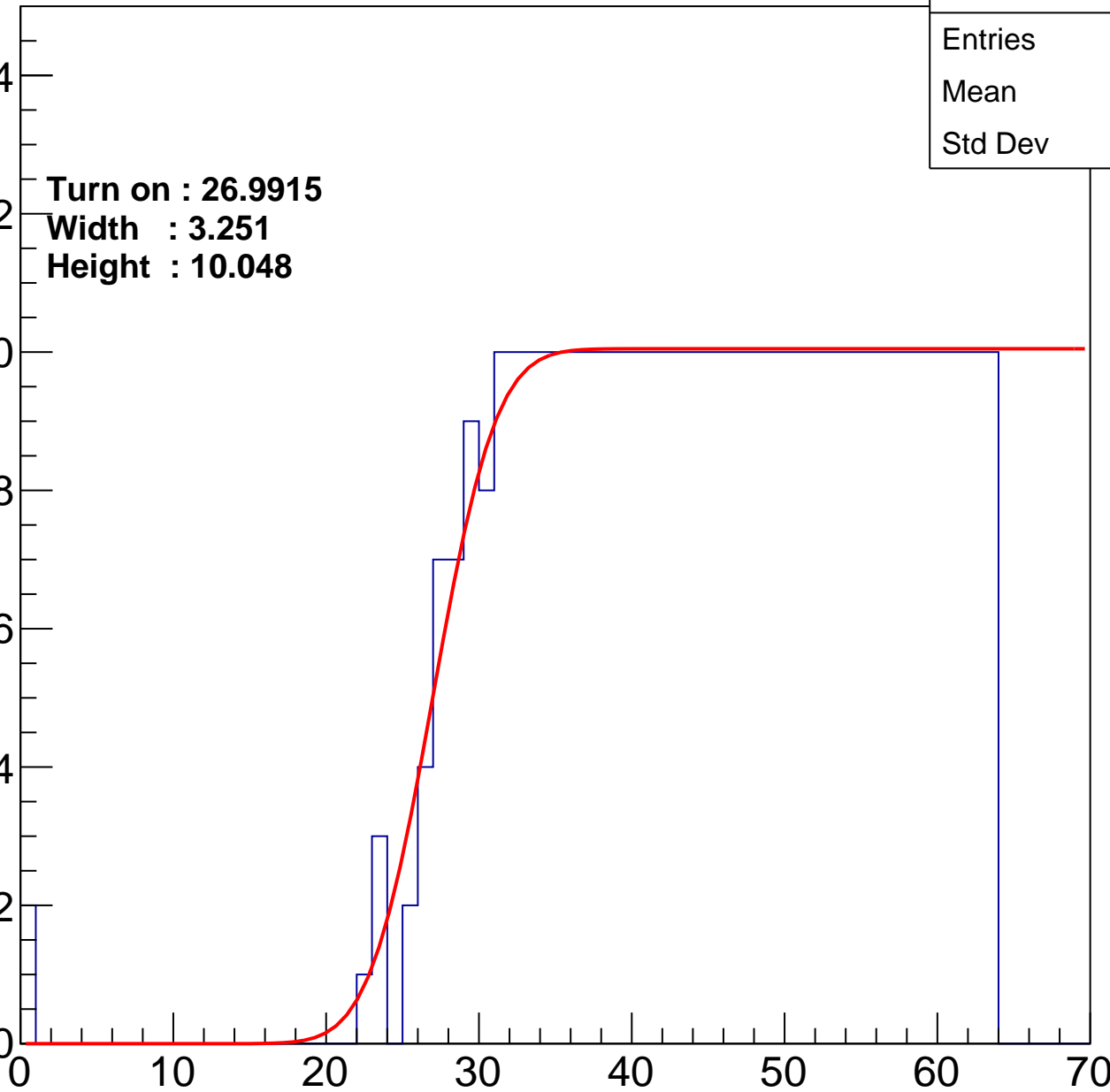
Width : 3.251

Height : 10.048

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch17

calib\_packv5\_042523\_0143.root, FC#4, port A2

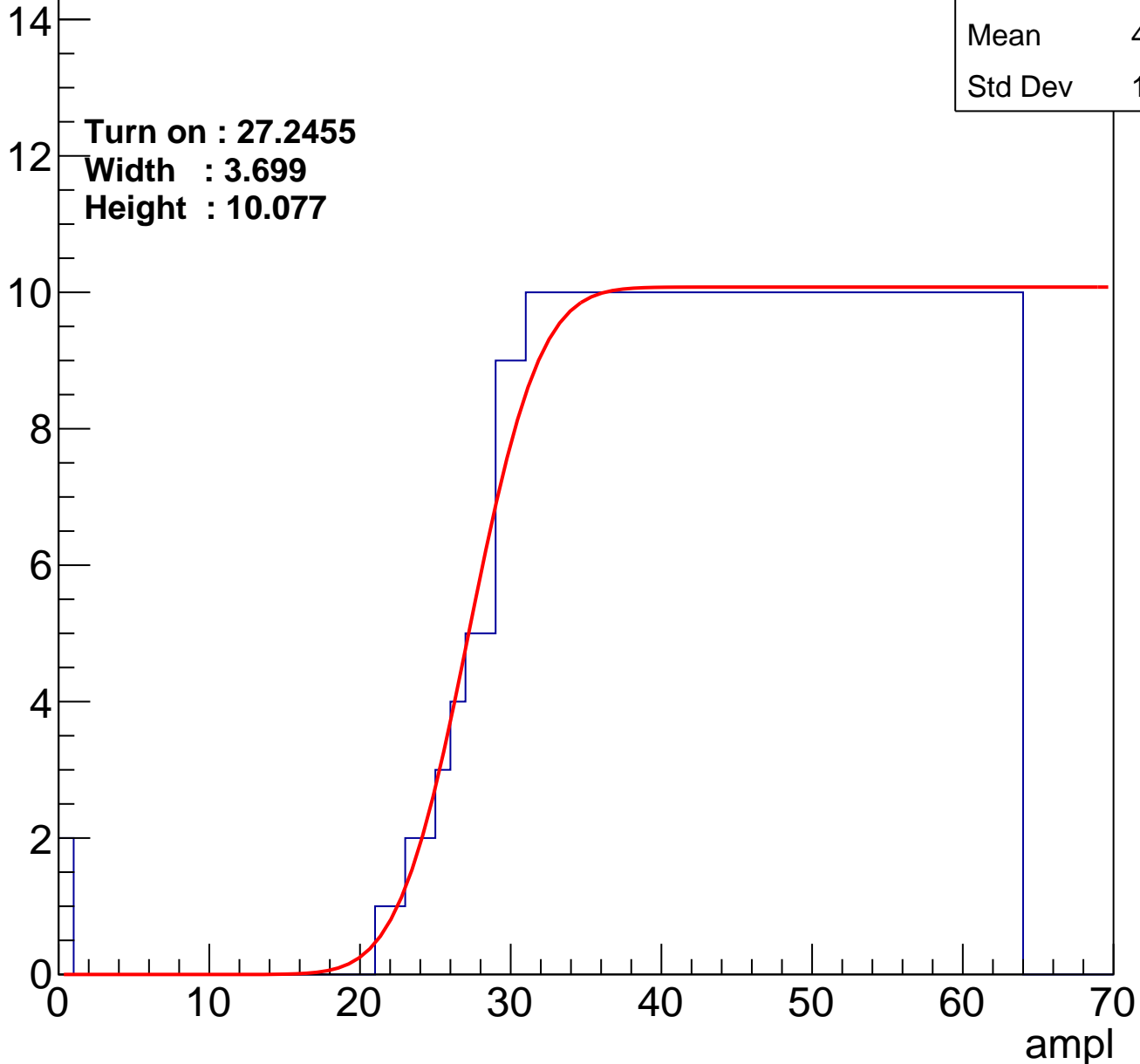
Entries	373
Mean	44.59
Std Dev	11.37

Turn on : 27.2455

Width : 3.699

Height : 10.077

Entry



# B1L100S, U13-ch18

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	357
Mean	45.37
Std Dev	10.97

Turn on : 28.8412

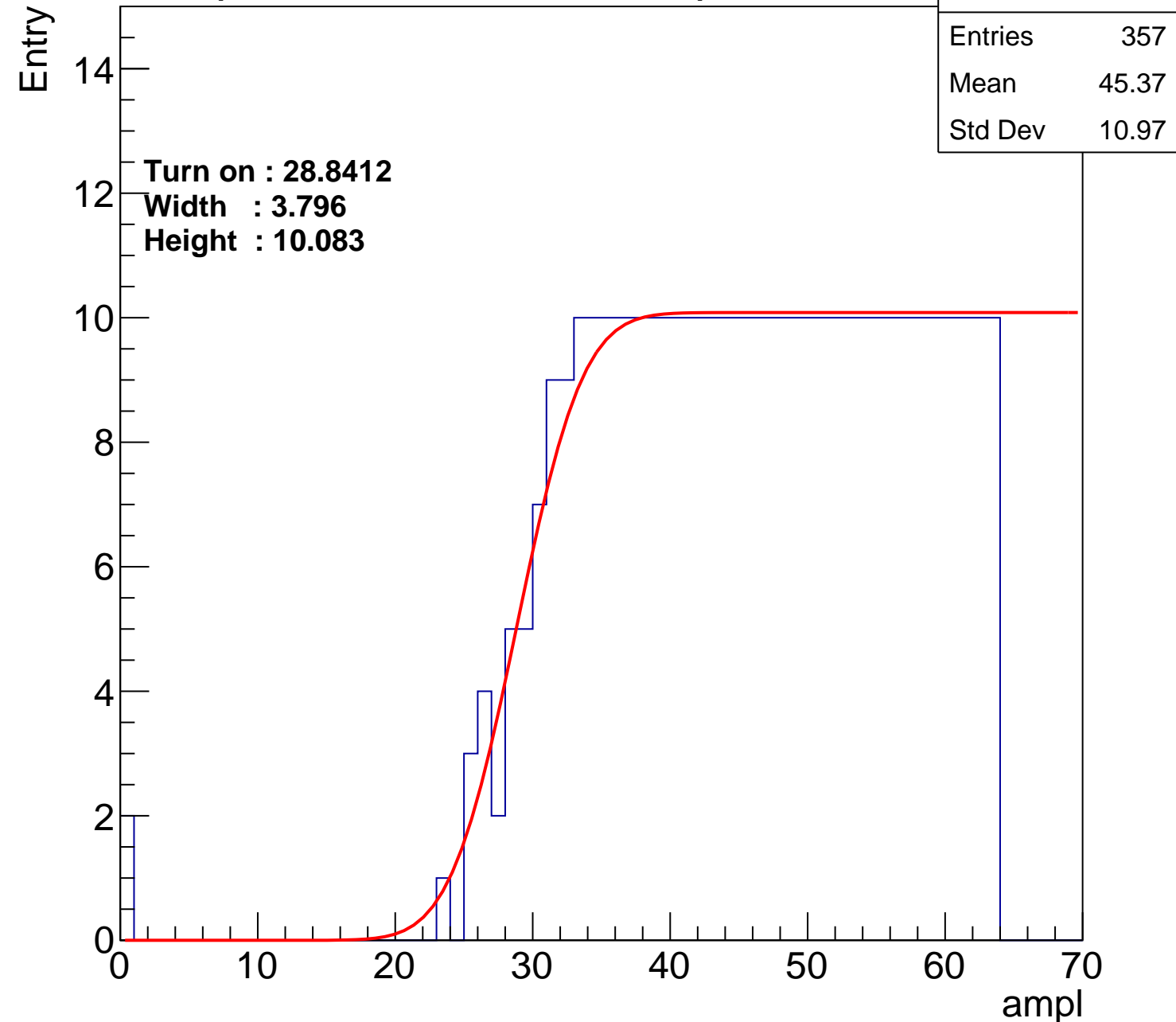
Width : 3.796

Height : 10.083

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch19

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	369
Mean	44.87
Std Dev	11.04

Turn on : 27.7904

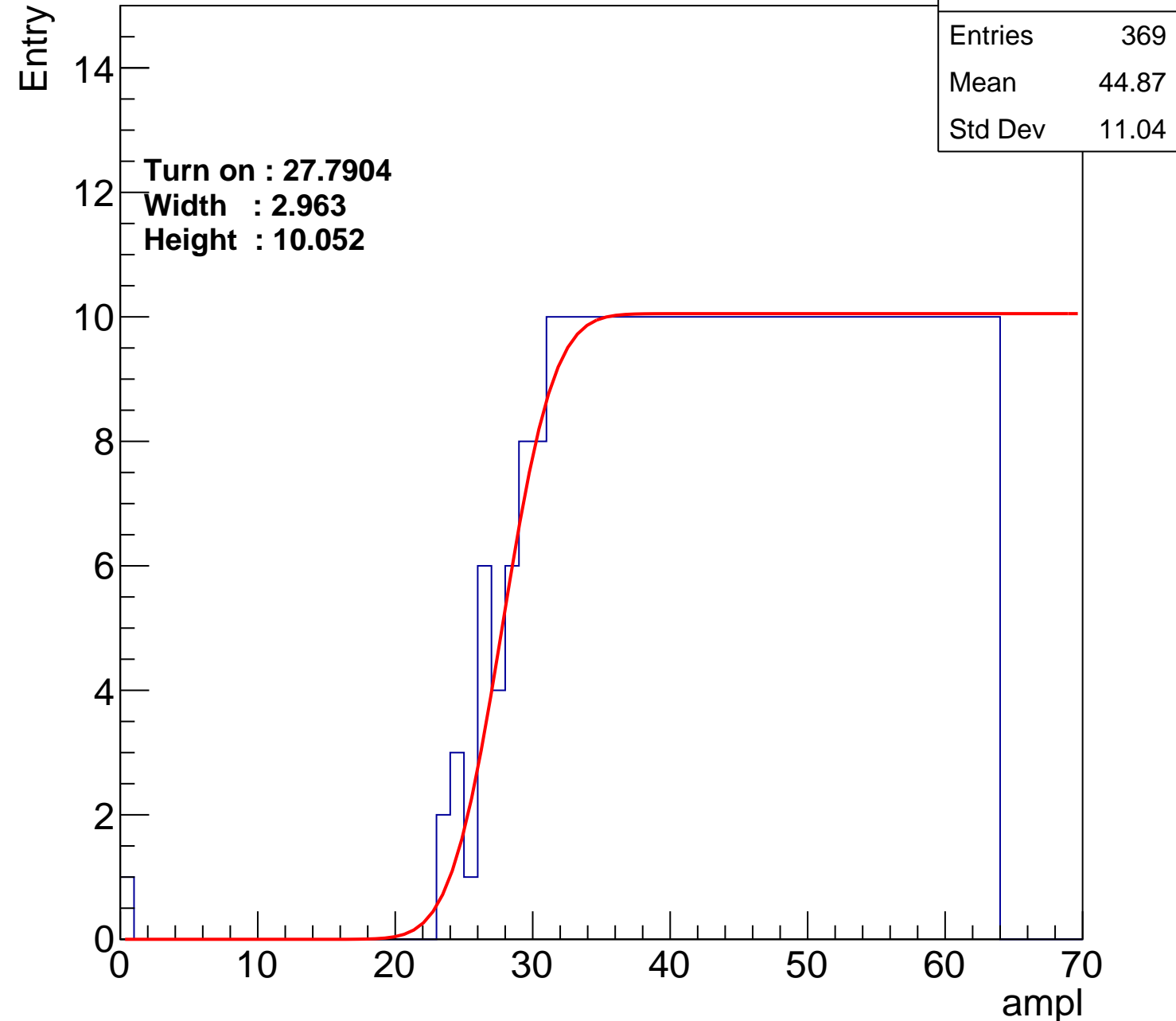
Width : 2.963

Height : 10.052

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch20

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	359
Mean	45.38
Std Dev	10.75

Turn on : 28.3931

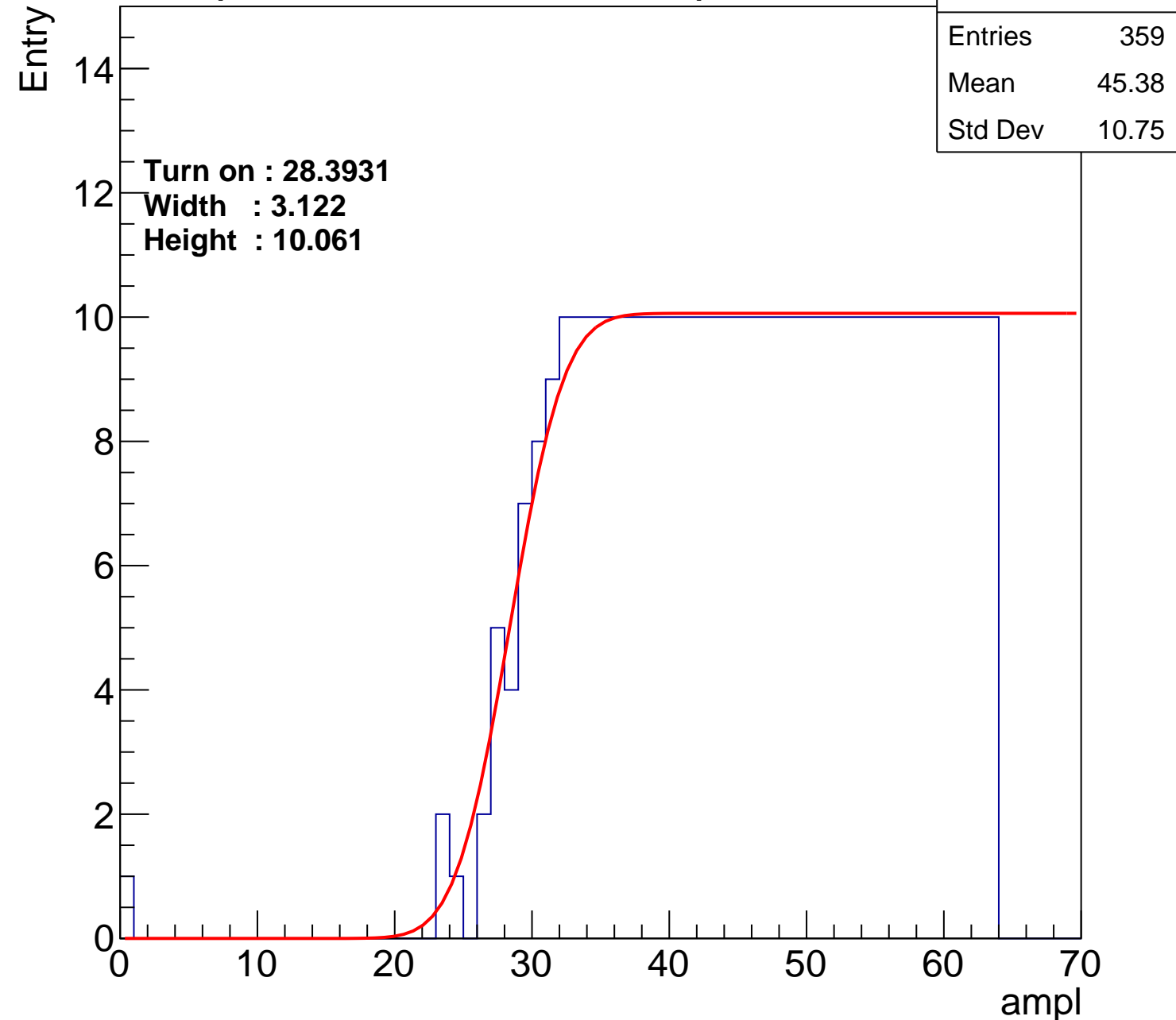
Width : 3.122

Height : 10.061

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch21

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	358
Mean	45.46
Std Dev	10.68

Turn on : 28.3488

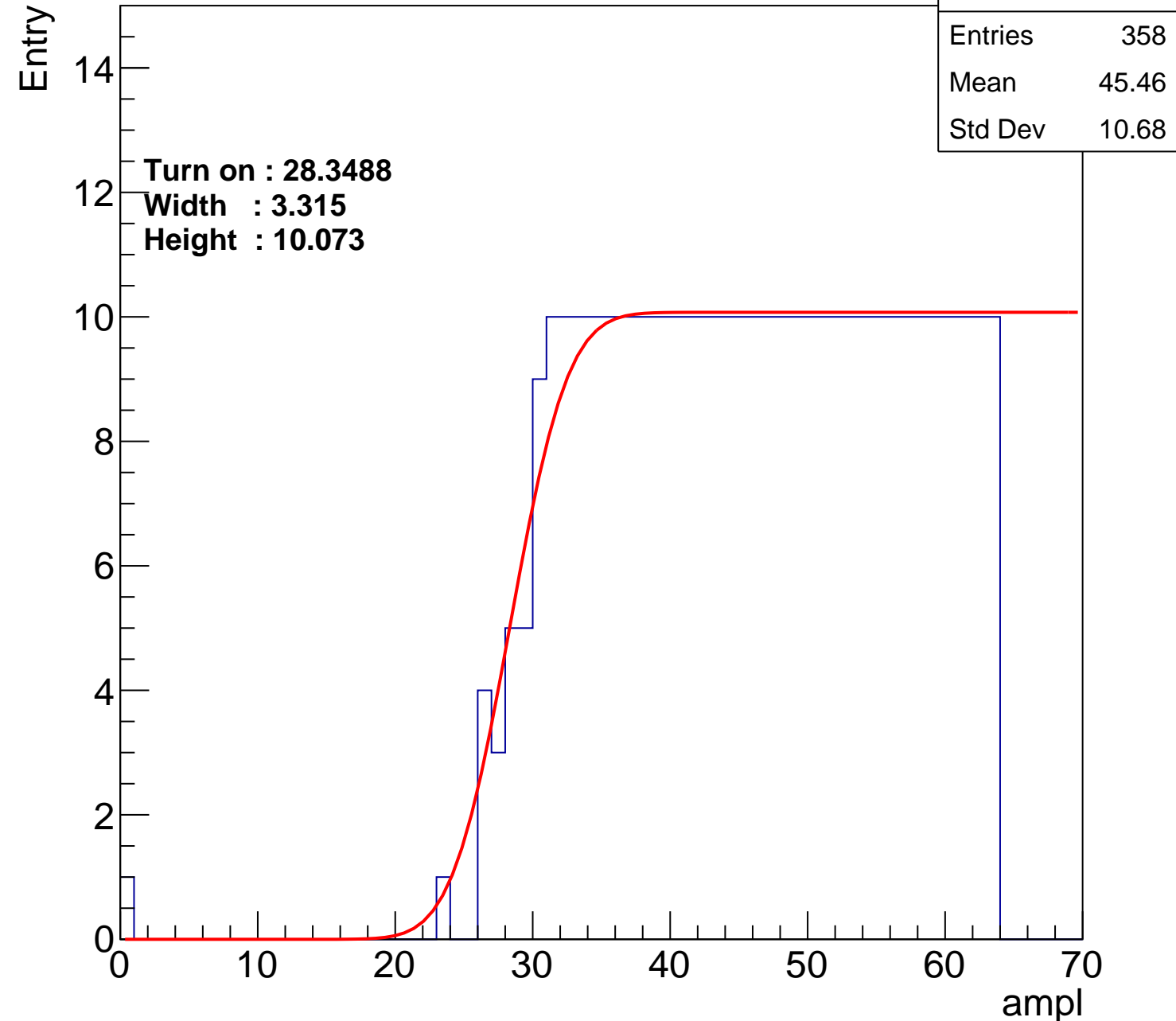
Width : 3.315

Height : 10.073

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch22

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	364
Mean	45.12
Std Dev	10.9

Turn on : 27.5718

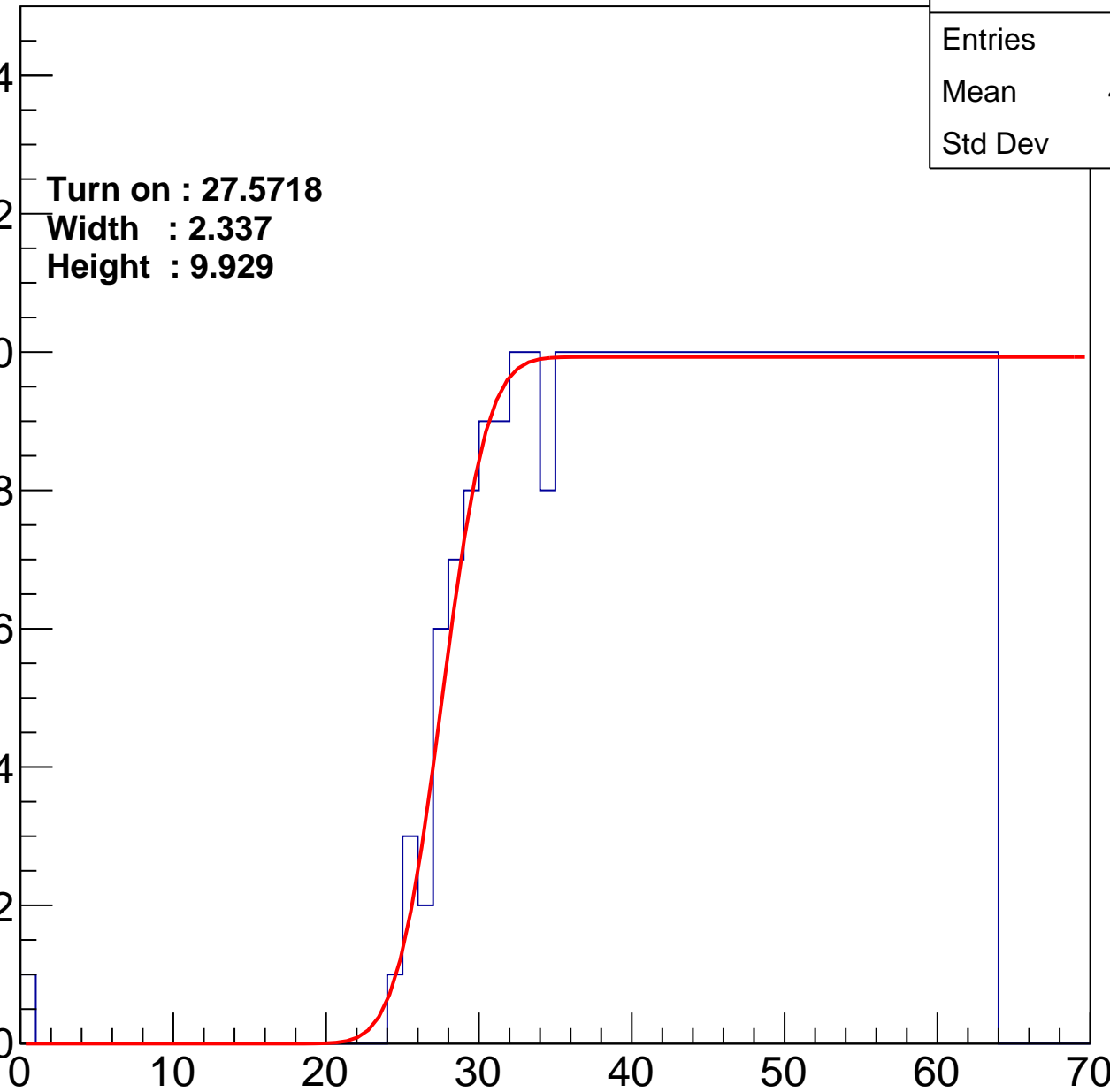
Width : 2.337

Height : 9.929

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U13-ch23

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	363
Mean	45.04
Std Dev	11.27

Turn on : 28.1033

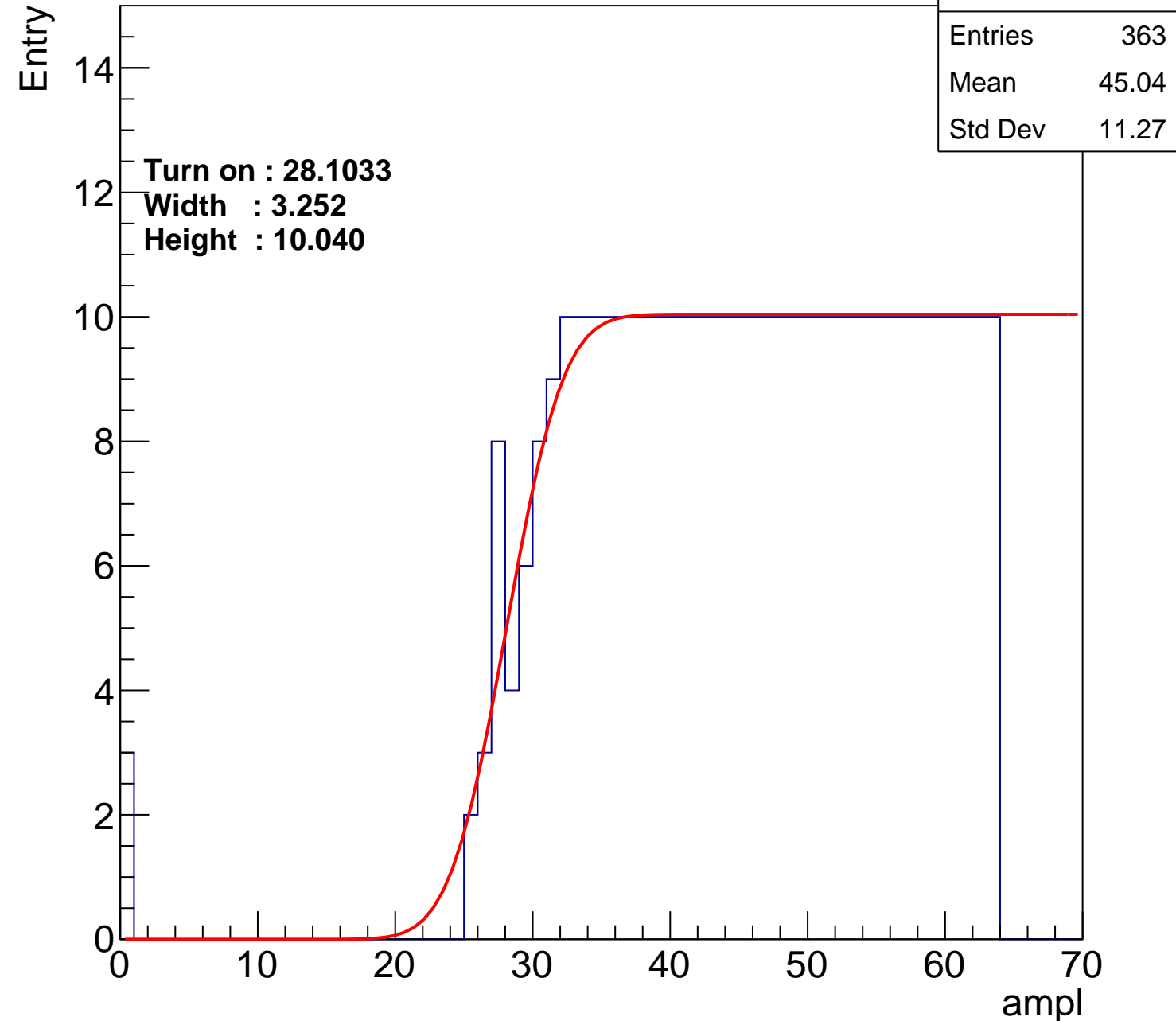
Width : 3.252

Height : 10.040

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch24

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	376
Mean	44.57
Std Dev	11.15

Turn on : 26.8338

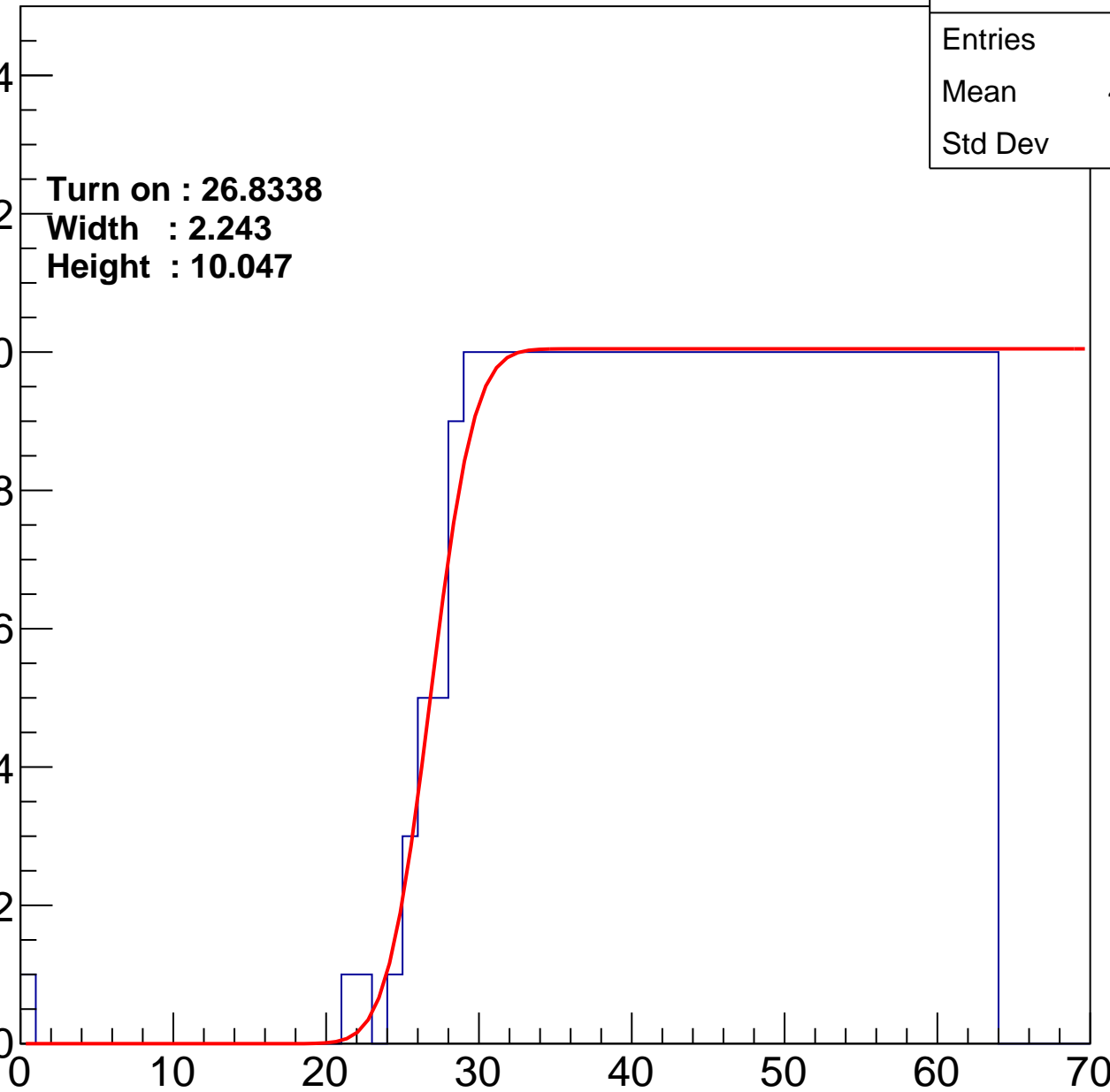
Width : 2.243

Height : 10.047

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



**calib\_packv5\_042523\_0143.root, FC#4, port A2**

**calib\_packv5\_042523\_0143.root, FC#4, port A2**

Turn on : 29.4058  
Width : 2.911  
Height : 10.055



# B1L100S, U13-ch26

calib\_packv5\_042523\_0143.root, FC#4, port A2

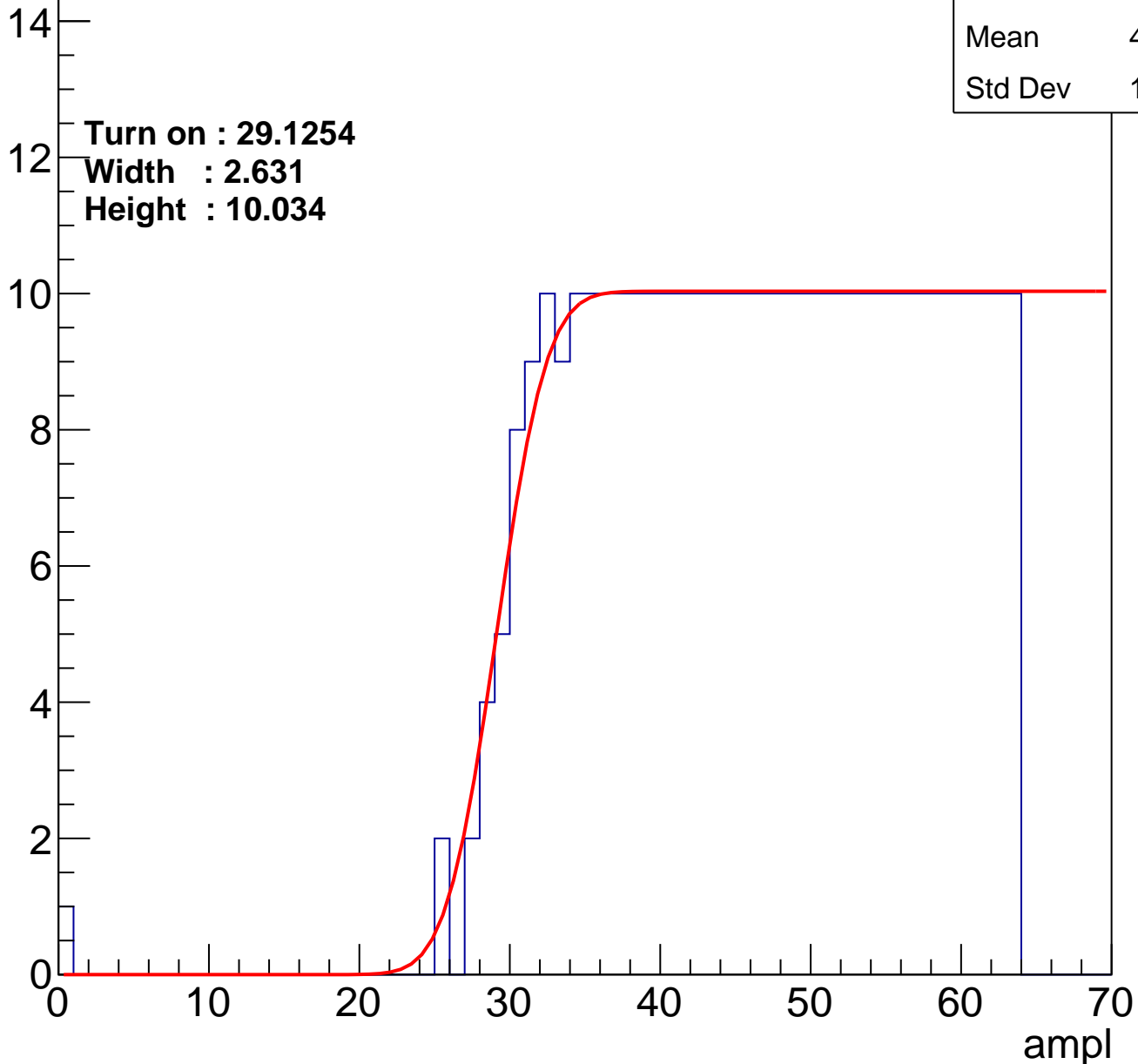
Entries	350
Mean	45.85
Std Dev	10.47

Turn on : 29.1254

Width : 2.631

Height : 10.034

Entry



# B1L100S, U13-ch27

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	357
Mean	45.47
Std Dev	10.71

Turn on : 28.5194

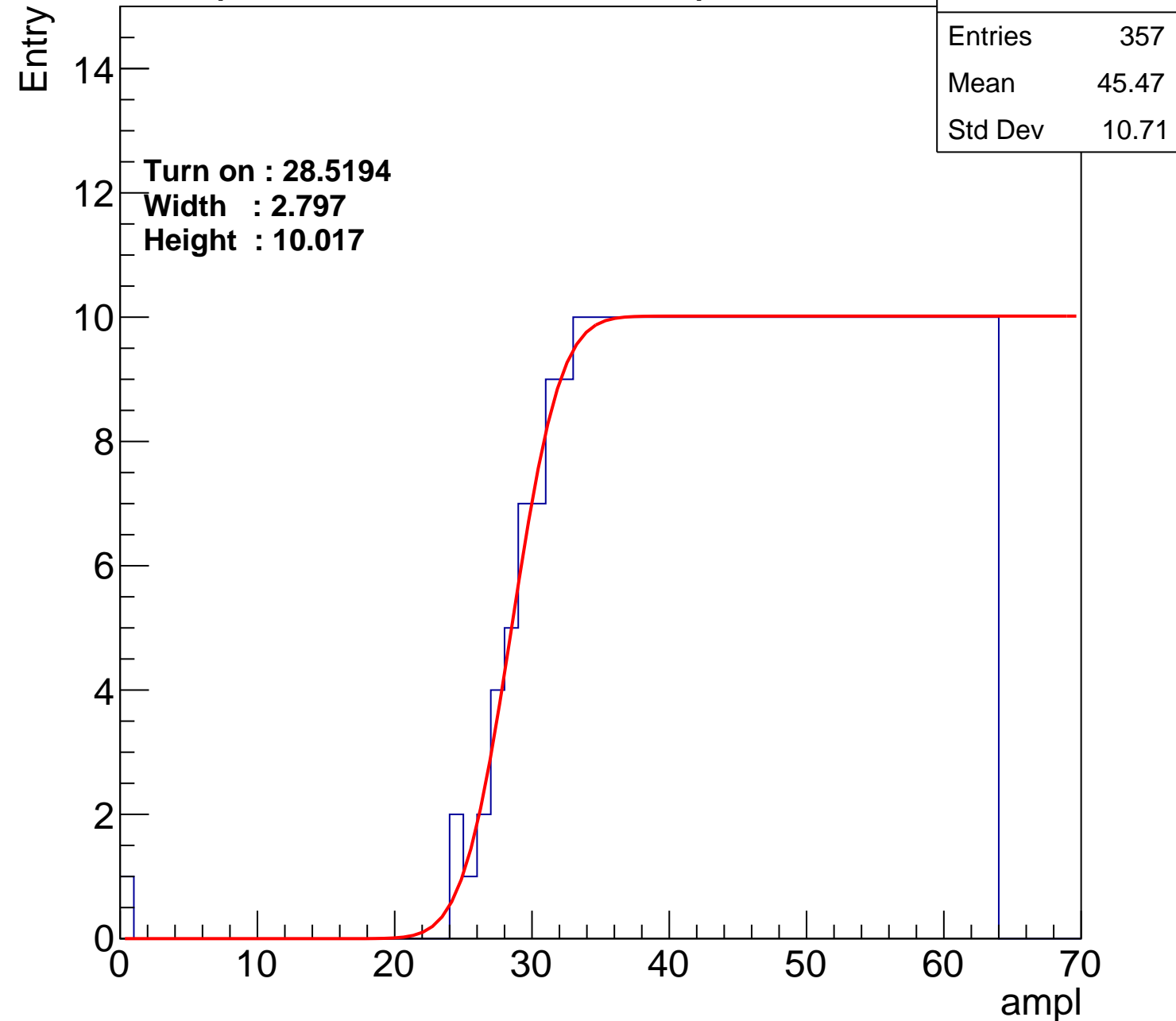
Width : 2.797

Height : 10.017

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch28

calib\_packv5\_042523\_0143.root, FC#4, port A2

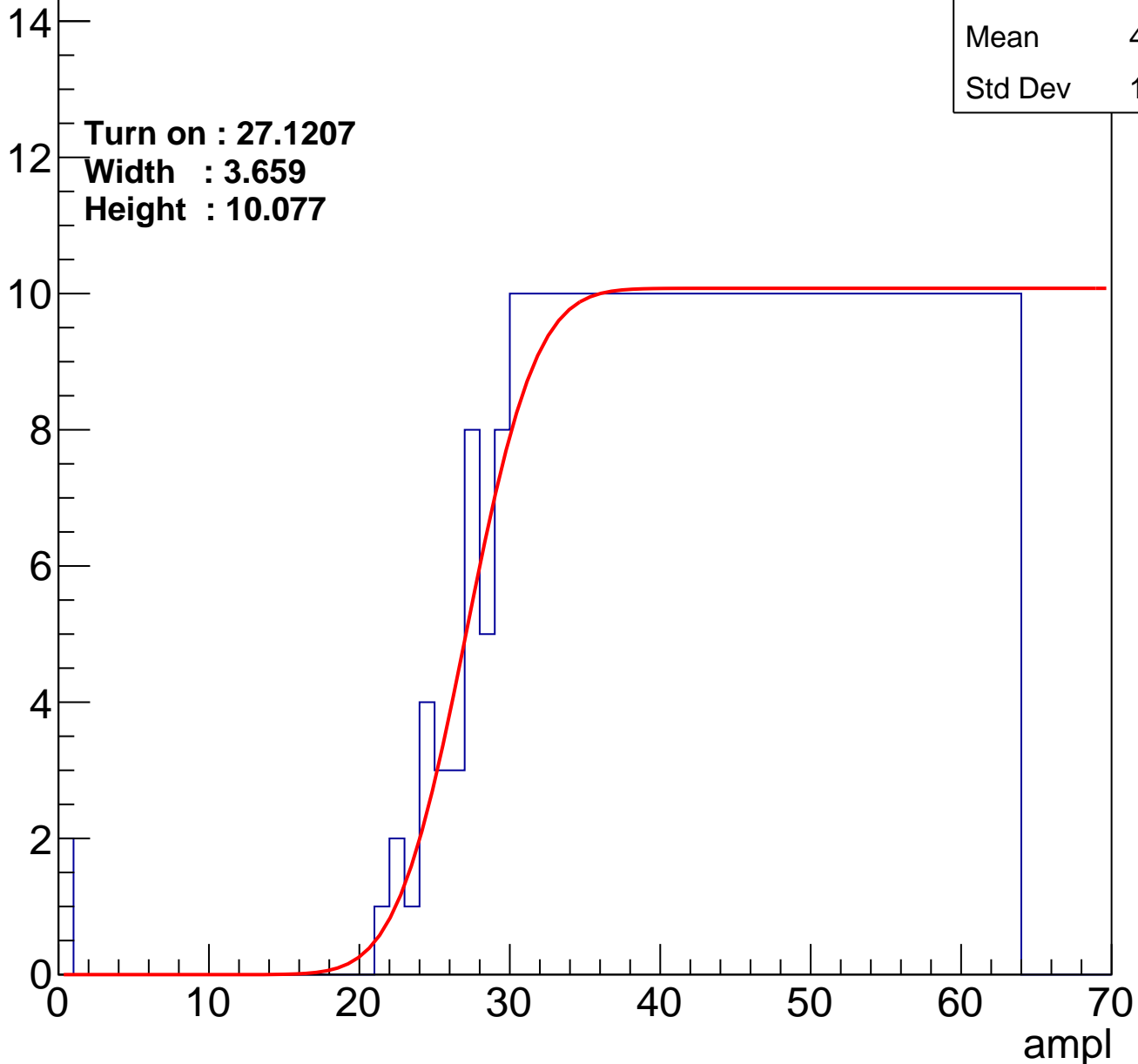
Entries	377
Mean	44.39
Std Dev	11.48

Turn on : 27.1207

Width : 3.659

Height : 10.077

Entry



# B1L100S, U13-ch29

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	367
Mean	44.87
Std Dev	11.22

Turn on : 27.4791

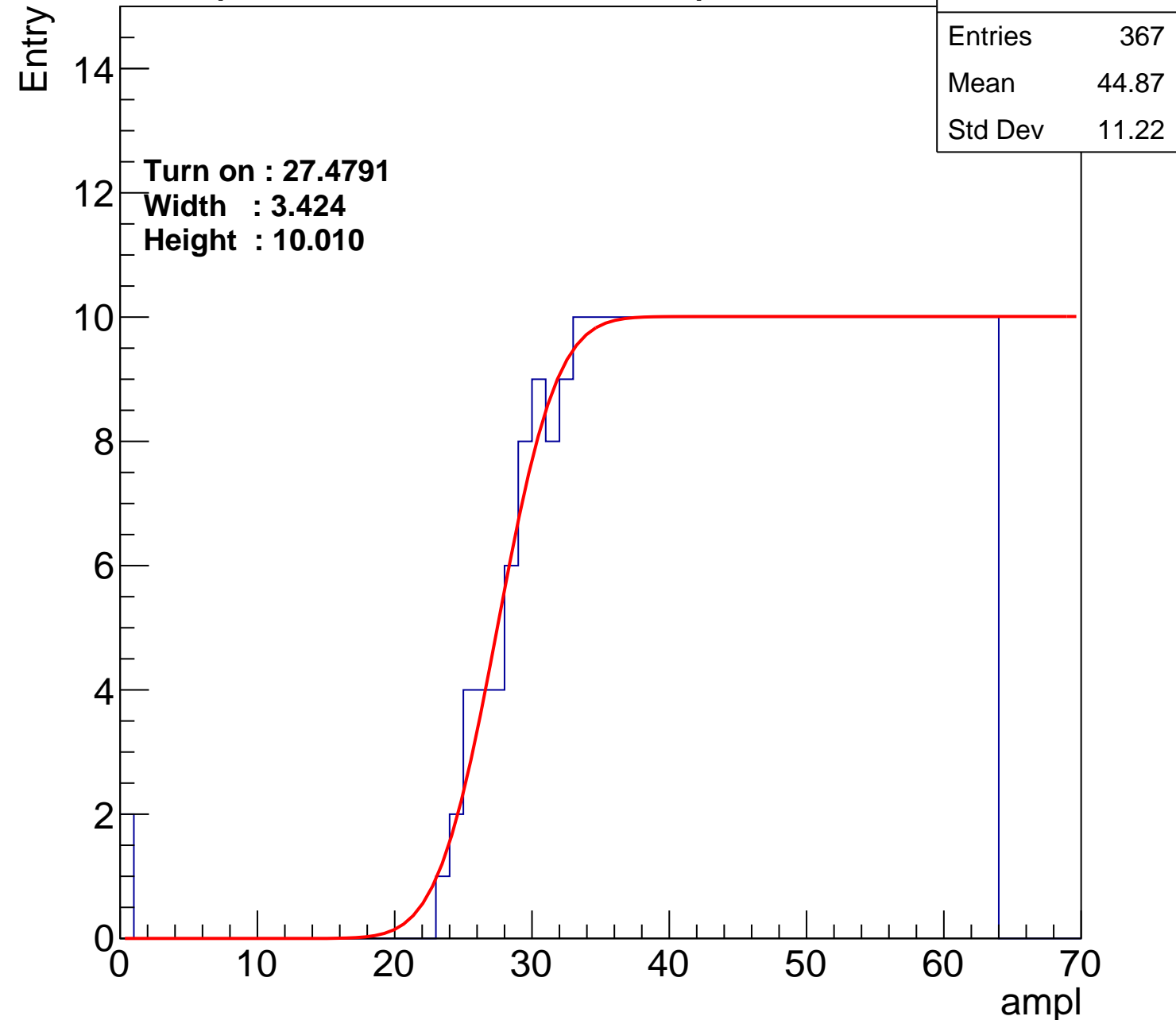
Width : 3.424

Height : 10.010

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch30

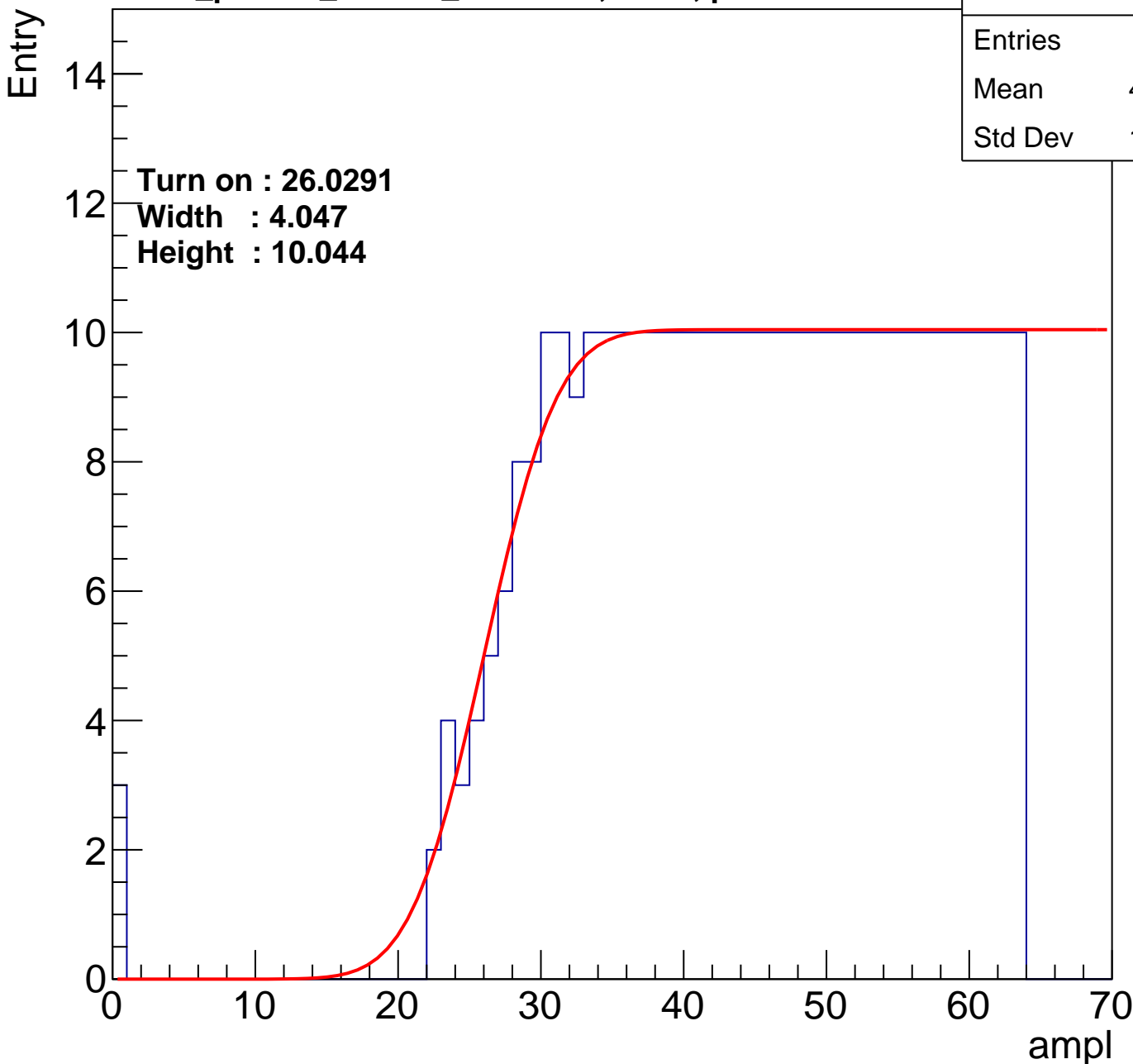
**calib\_packv5\_042523\_0143.root, FC#4, port A2**

Entries	382
Mean	44.07
Std Dev	11.79

**Turn on : 26.0291**

**Width : 4.047**

**Height : 10.044**





# B1L100S, U13-ch31

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	373
Mean	44.69
Std Dev	11.12

Turn on : 26.8170

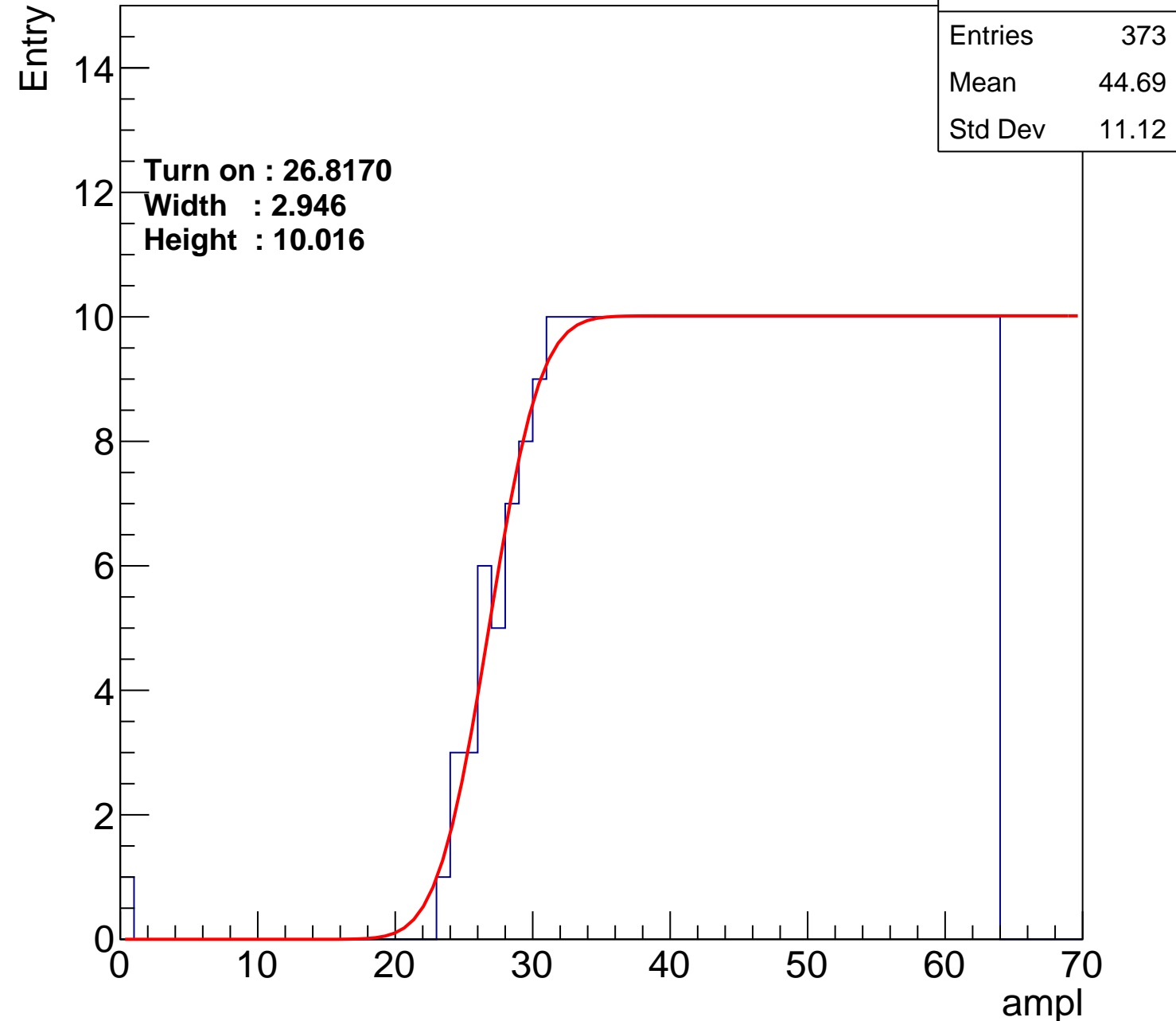
Width : 2.946

Height : 10.016

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch32

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	372
Mean	44.65
Std Dev	11.33

Turn on : 27.7245

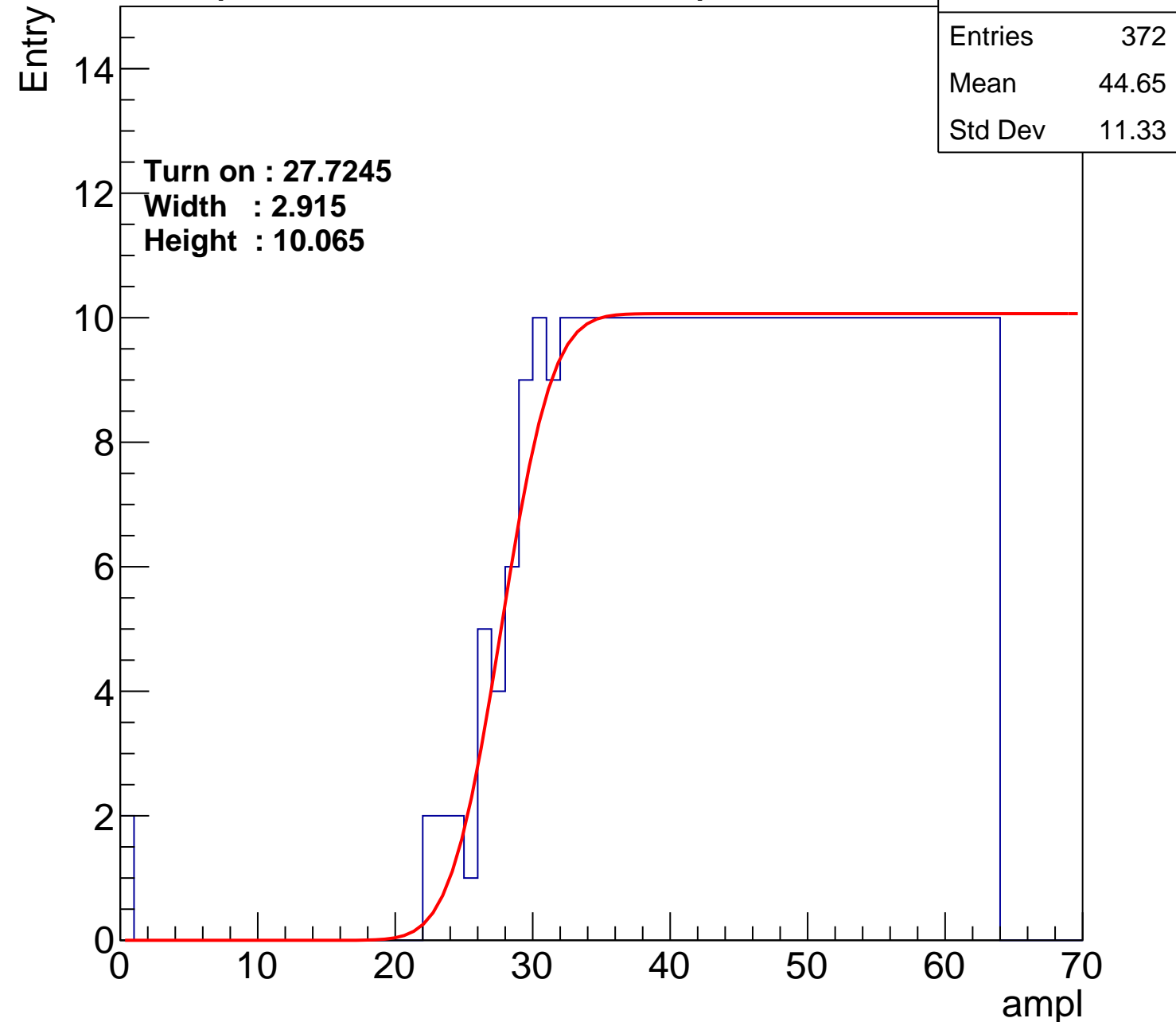
Width : 2.915

Height : 10.065

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch33

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	384
Mean	44.12
Std Dev	11.45

Turn on : 25.5269

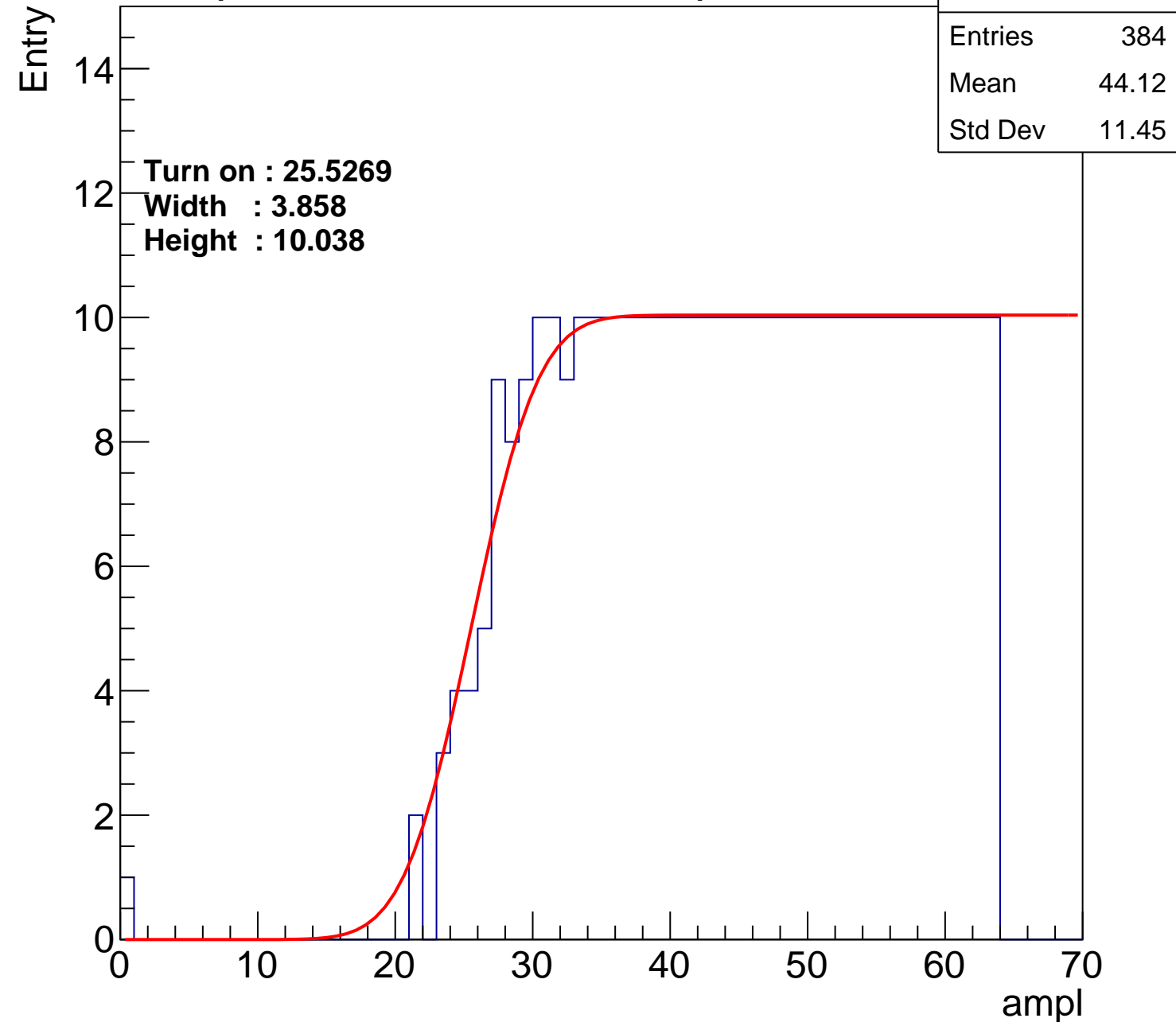
Width : 3.858

Height : 10.038

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch34

calib\_packv5\_042523\_0143.root, FC#4, port A2

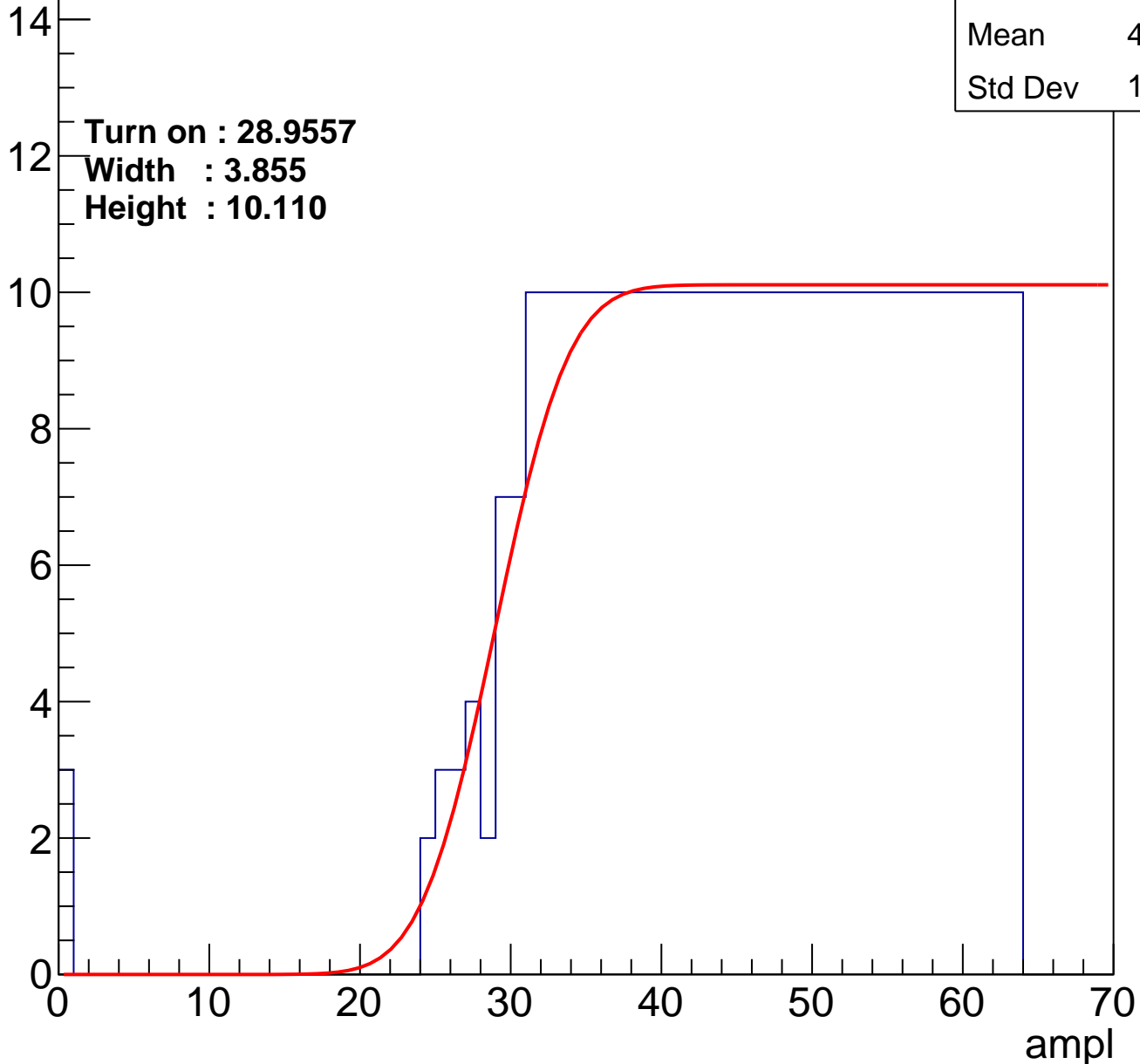
Entries	361
Mean	45.12
Std Dev	11.25

**Turn on : 28.9557**

**Width : 3.855**

**Height : 10.110**

Entry



# B1L100S, U13-ch35

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	347
Mean	45.63
Std Dev	11.39

Turn on : 29.8498

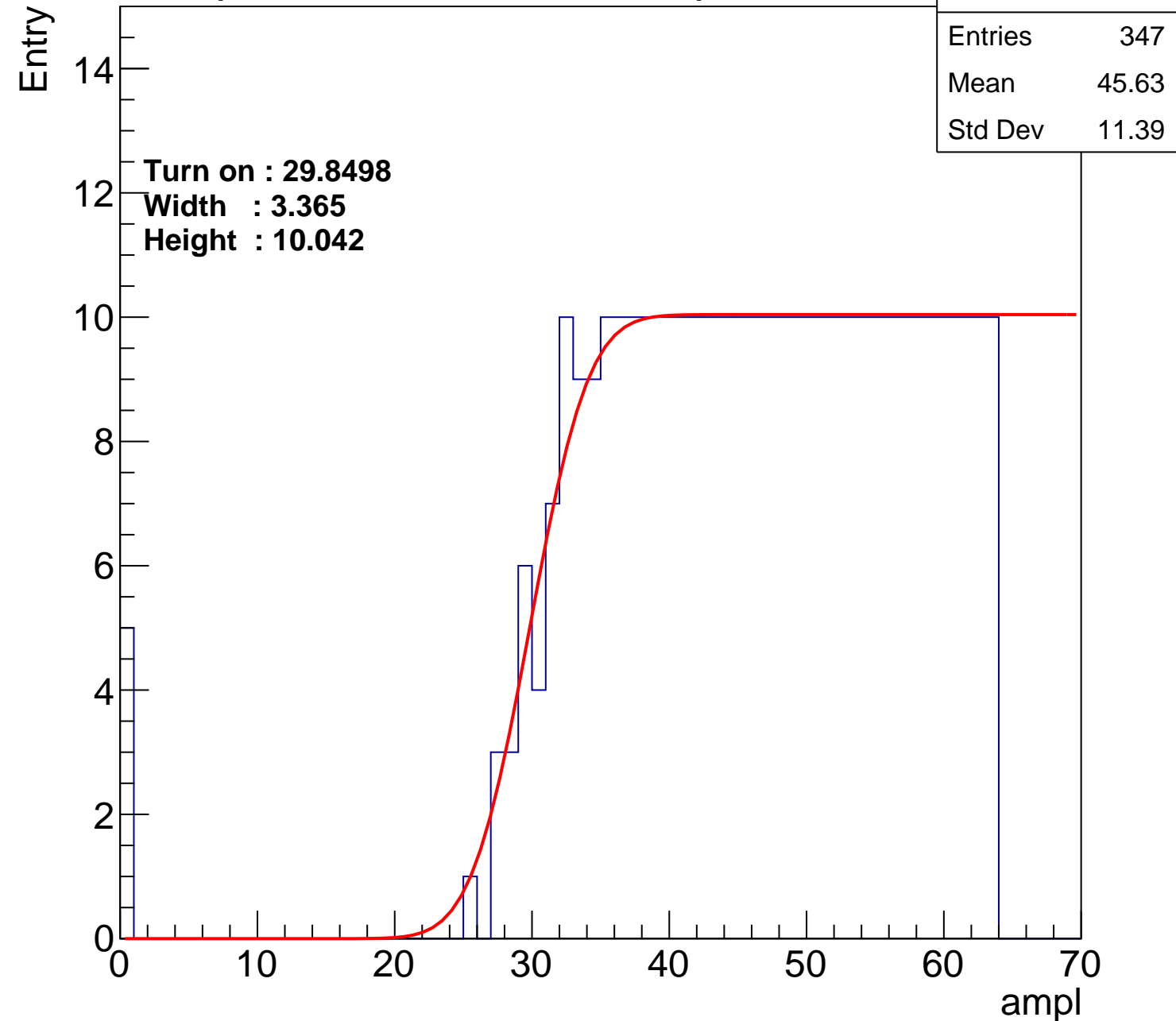
Width : 3.365

Height : 10.042

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch36

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	361
Mean	45.26
Std Dev	10.83

Turn on : 28.1745

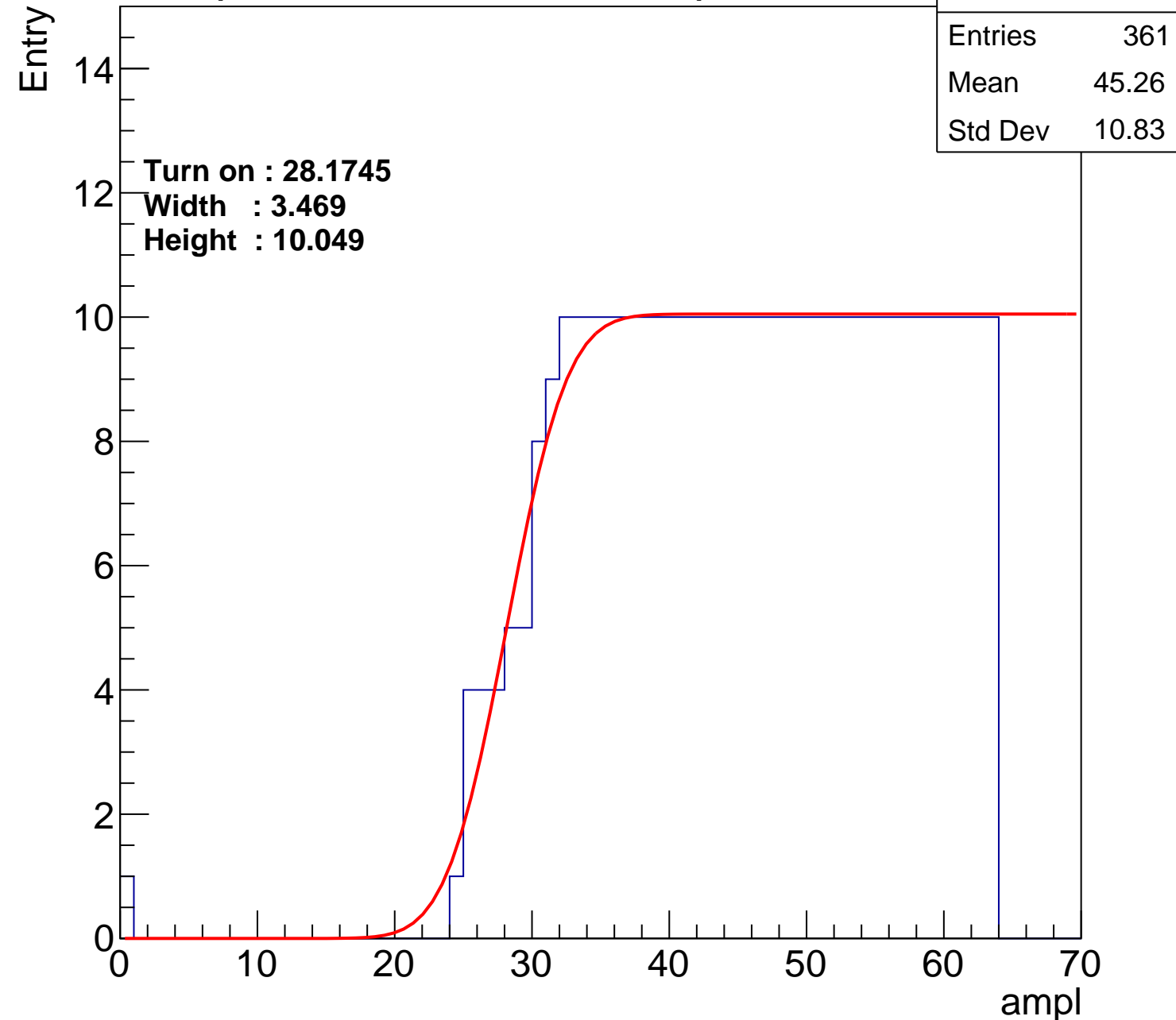
Width : 3.469

Height : 10.049

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch37

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	373
Mean	44.63
Std Dev	11.3

Turn on : 27.4032

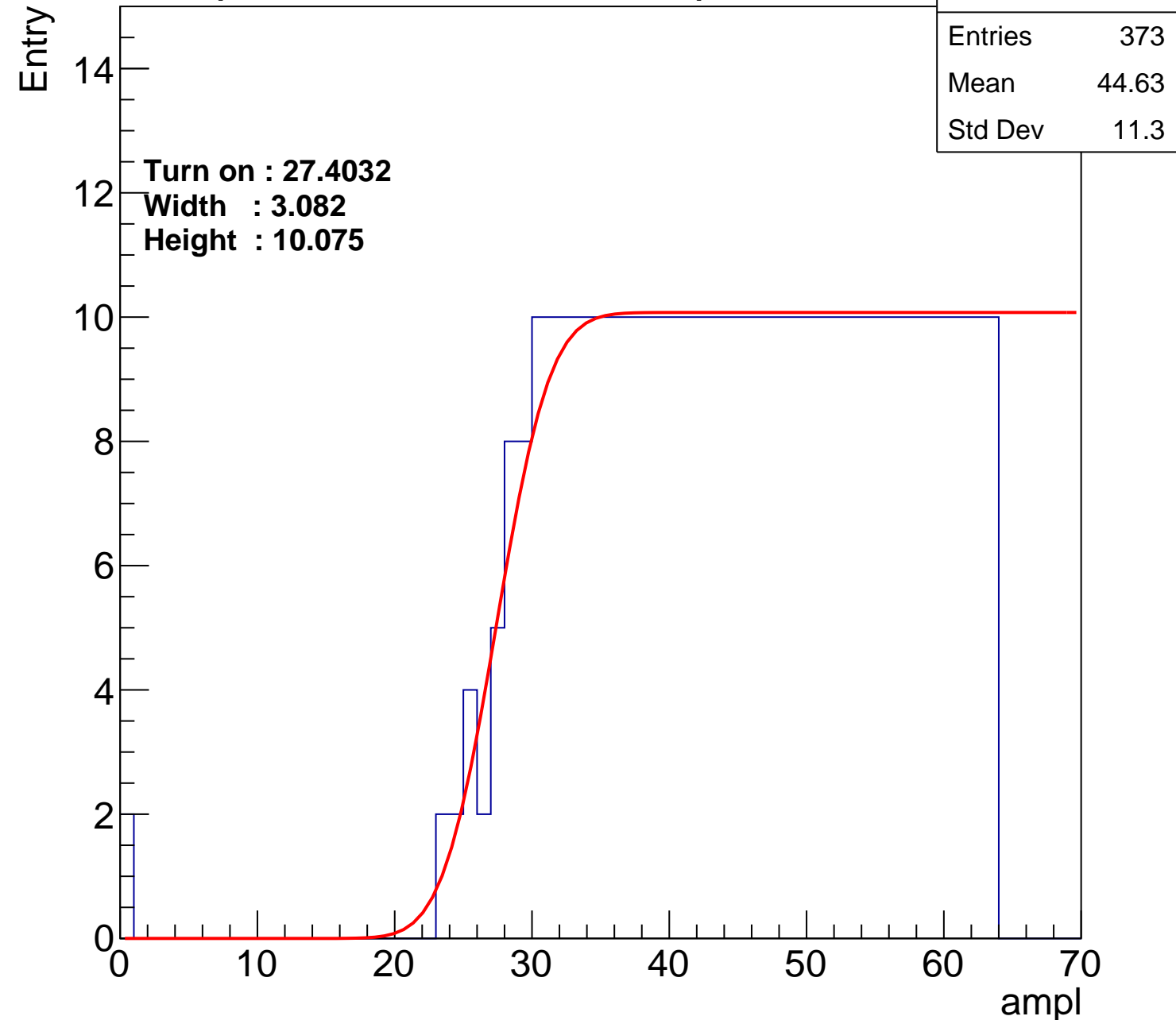
Width : 3.082

Height : 10.075

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch38

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	346
Mean	45.92
Std Dev	10.69

Turn on : 29.6568

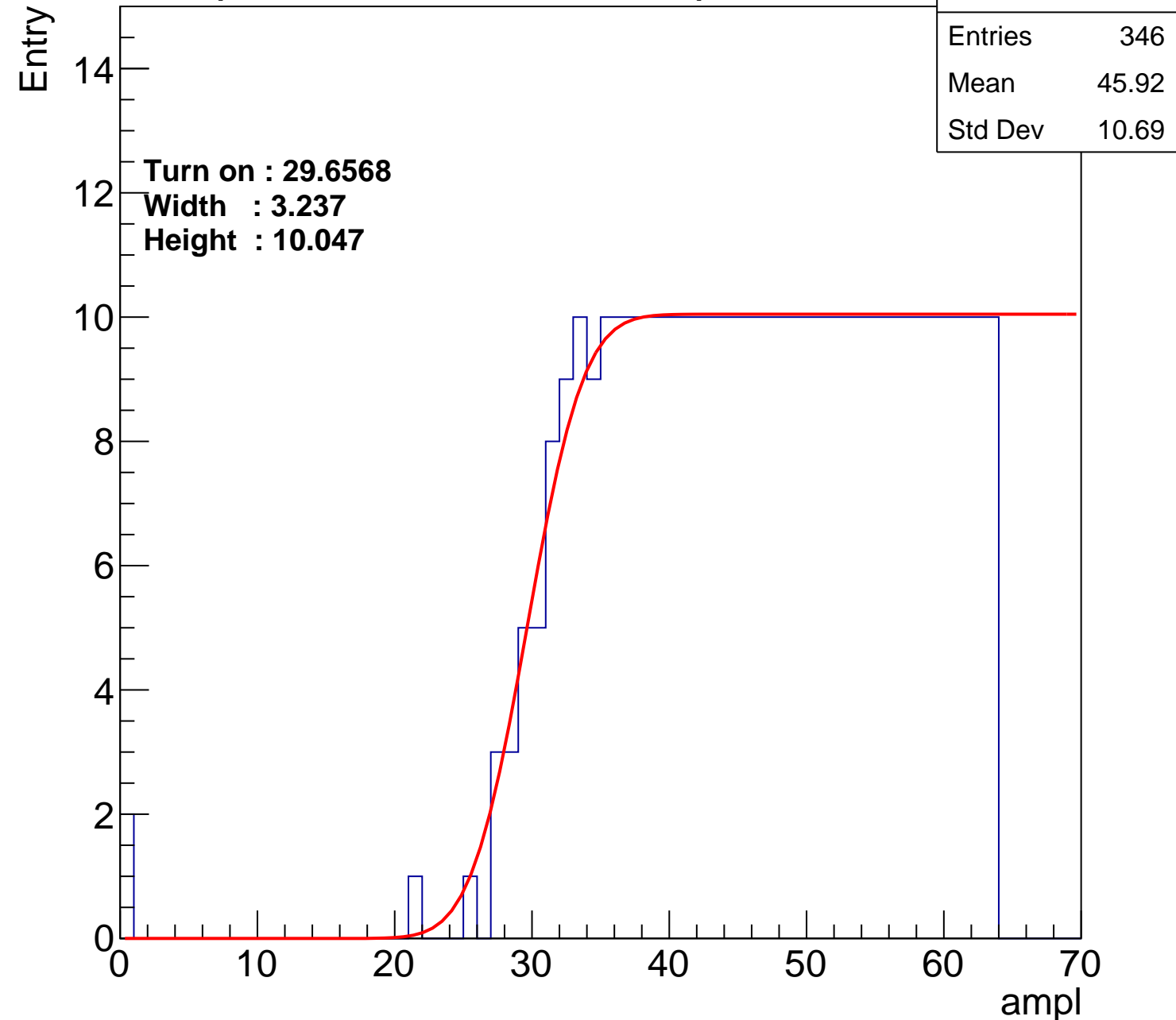
Width : 3.237

Height : 10.047

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U13-ch39

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	375
Mean	44.36
Std Dev	11.79

**Turn on : 27.2695**

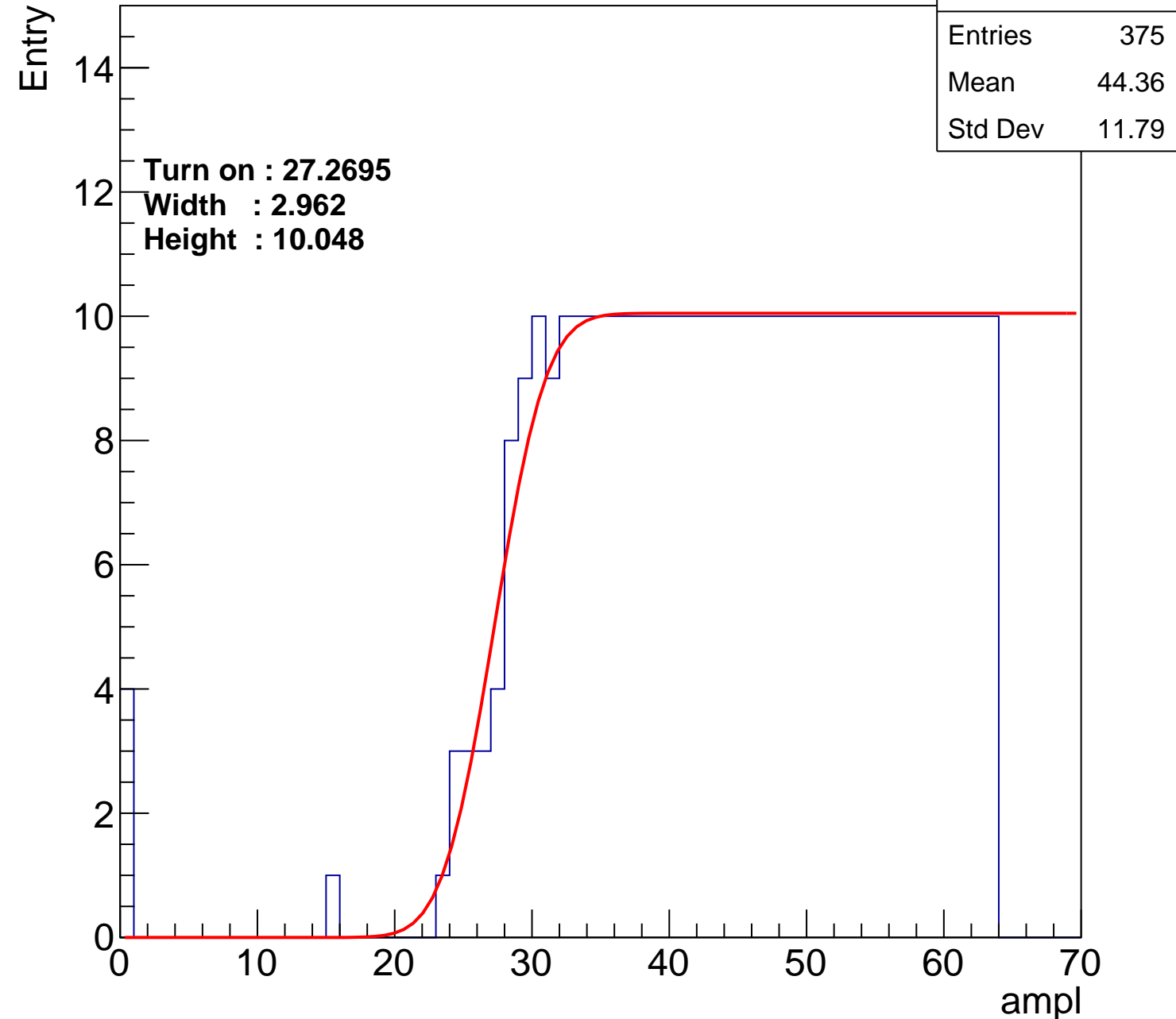
**Width : 2.962**

**Height : 10.048**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch40

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	363
Mean	45.16
Std Dev	10.89

Turn on : 27.7228

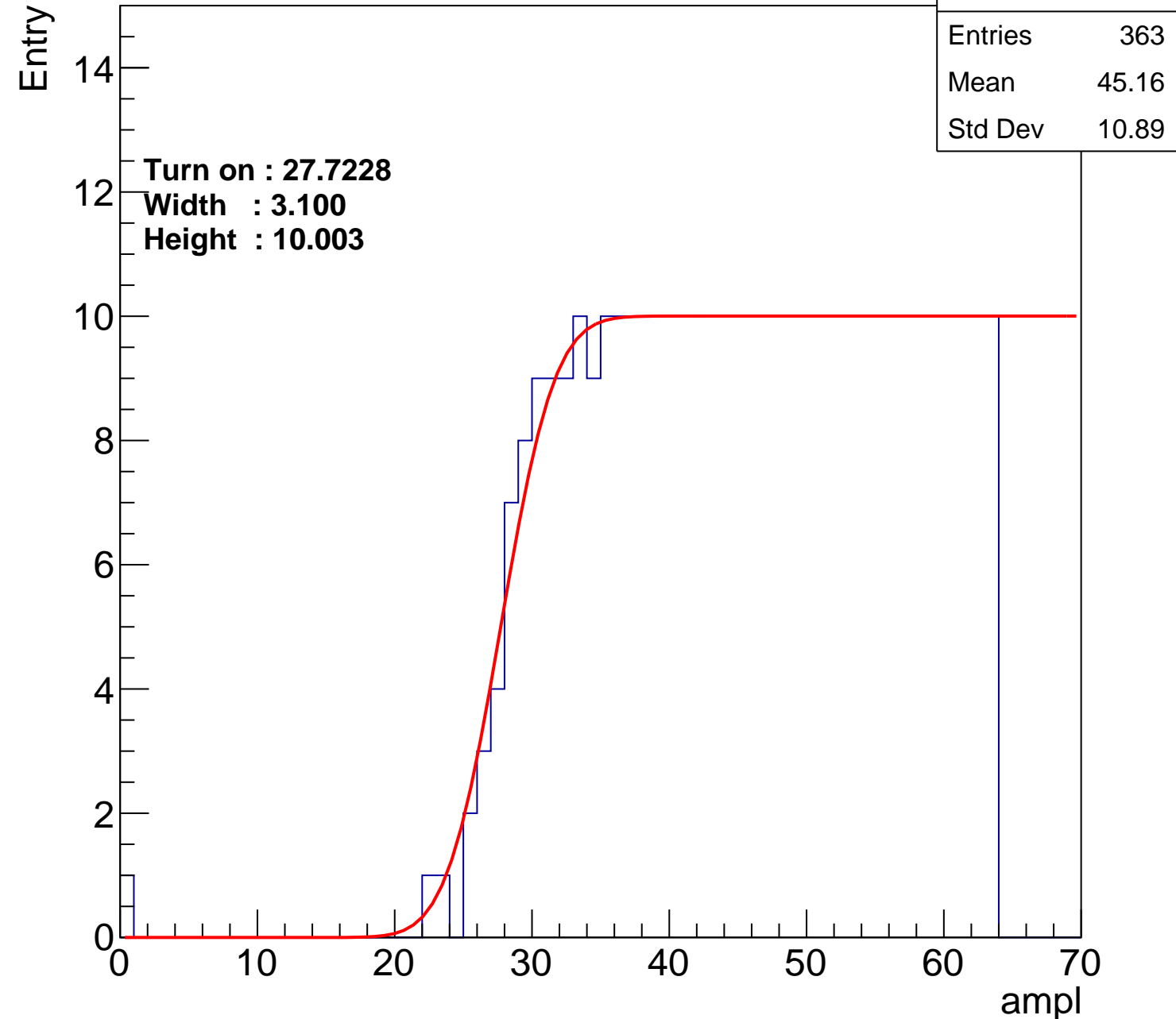
Width : 3.100

Height : 10.003

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch41

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	371
Mean	44.78
Std Dev	11.07

Turn on : 27.4962

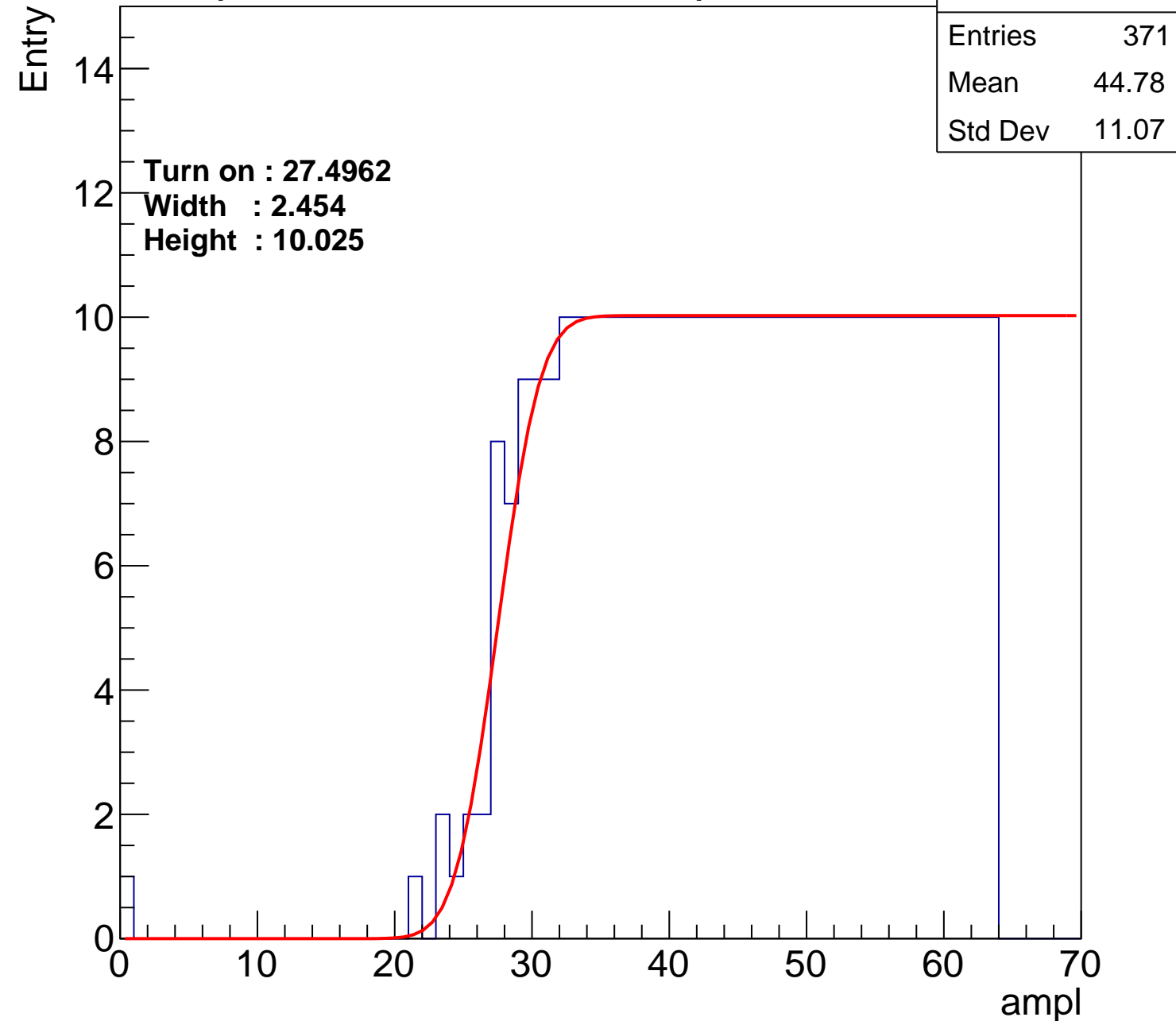
Width : 2.454

Height : 10.025

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch42

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	377
Mean	44.27
Std Dev	11.81

Turn on : 27.5049

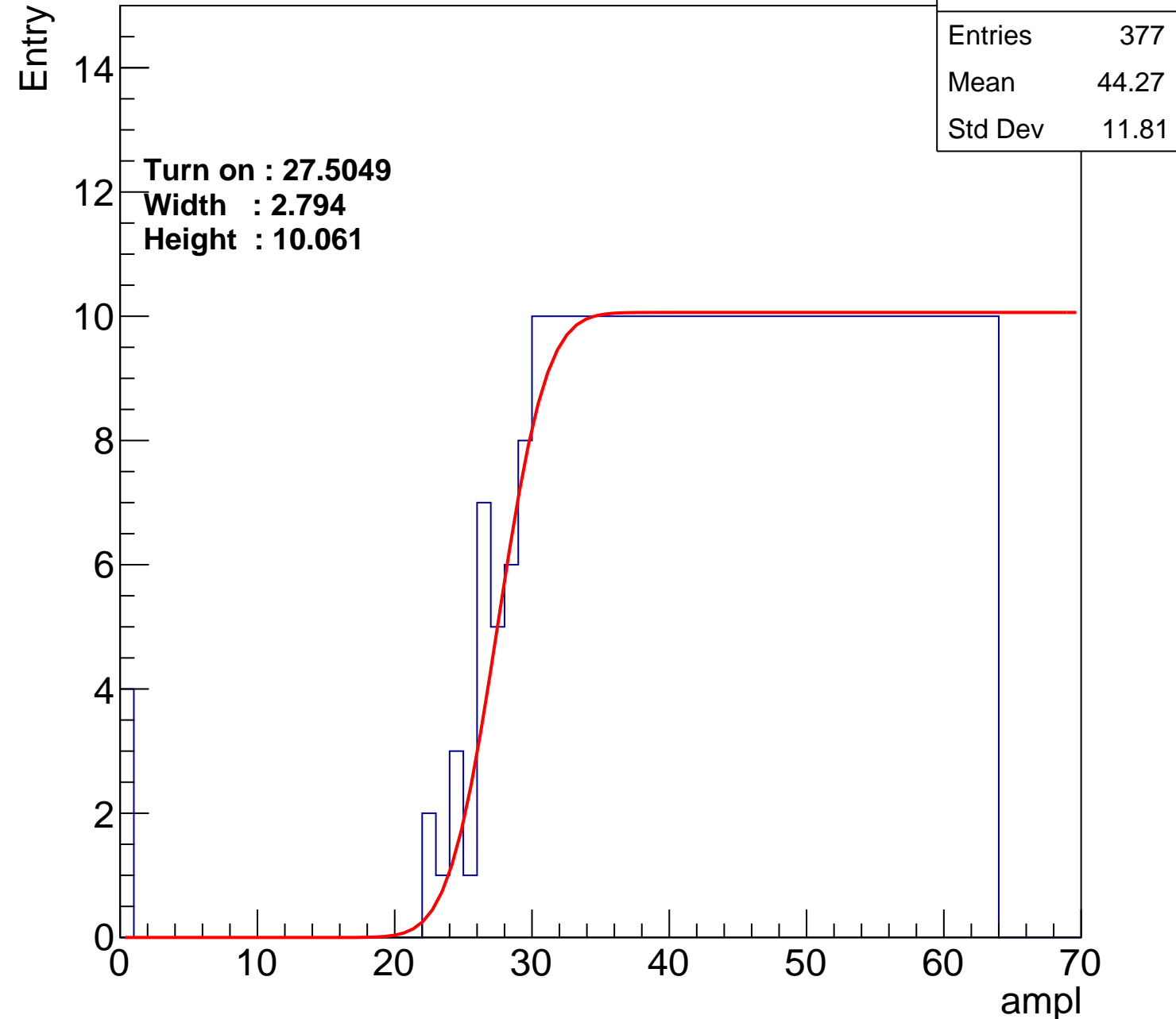
Width : 2.794

Height : 10.061

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch43

calib\_packv5\_042523\_0143.root, FC#4, port A2

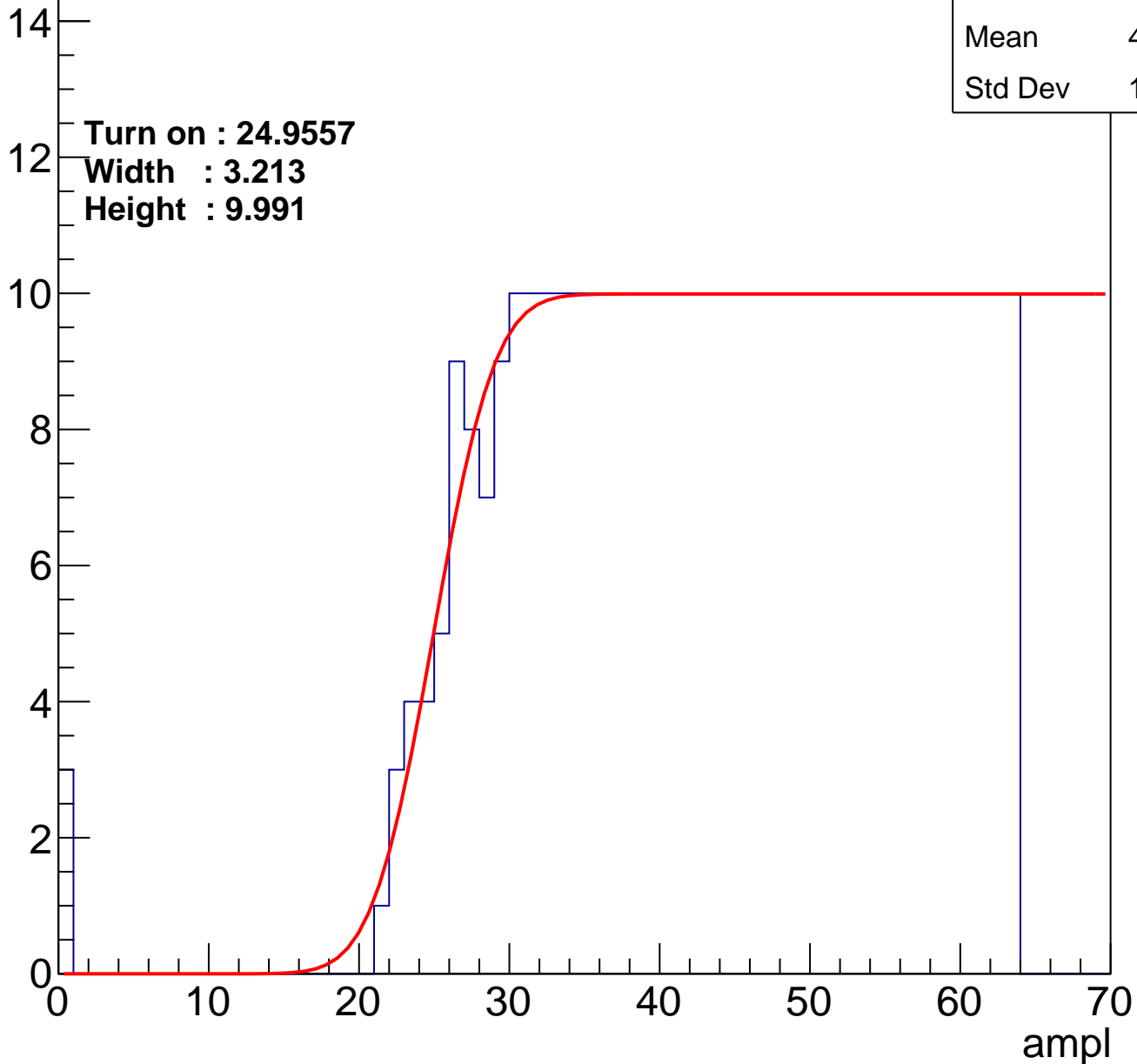
Entries	393
Mean	43.55
Std Dev	12.02

Turn on : 24.9557

Width : 3.213

Height : 9.991

Entry



# B1L100S, U13-ch44

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	366
Mean	44.92
Std Dev	11.3

**Turn on : 27.6655**

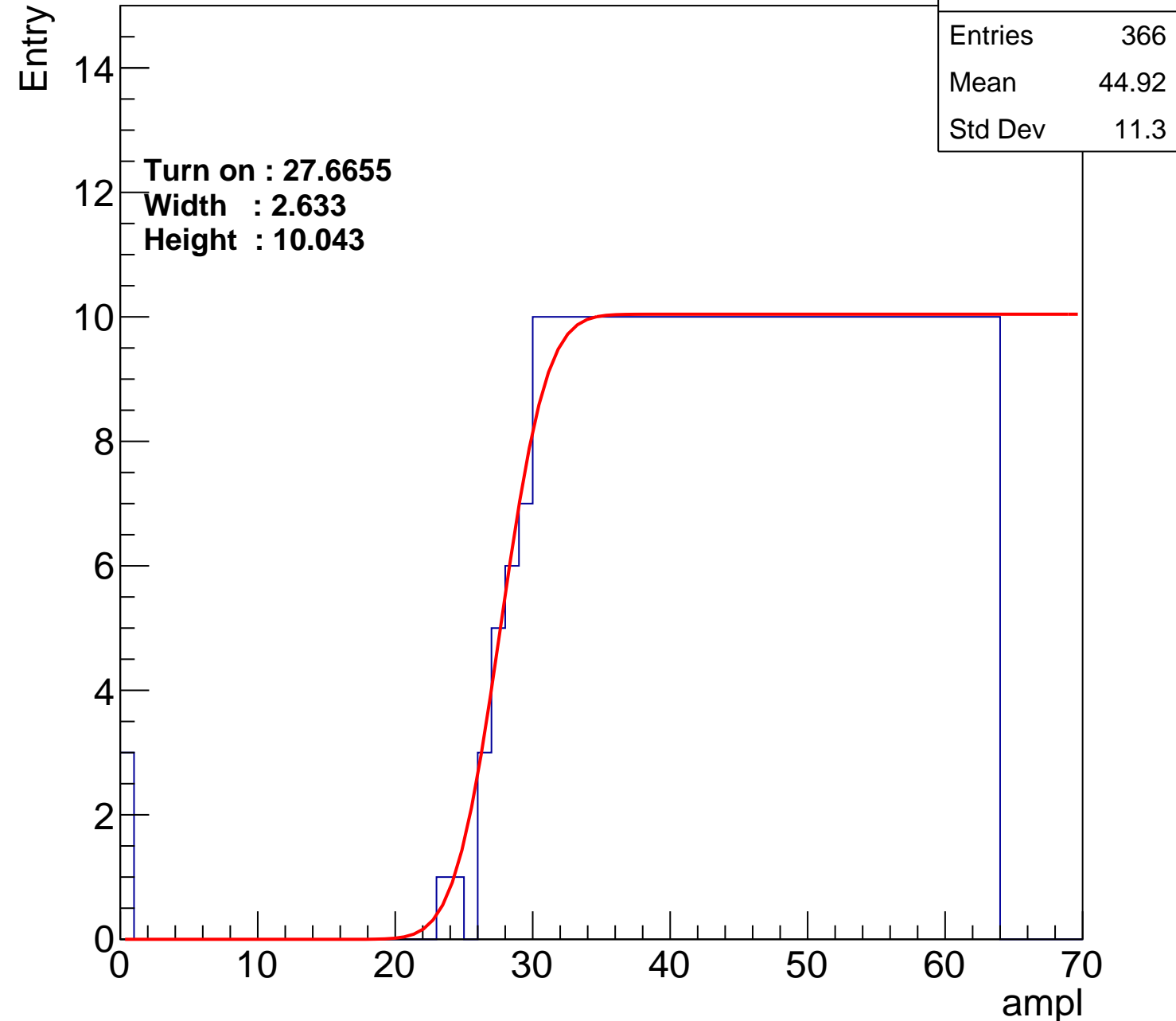
**Width : 2.633**

**Height : 10.043**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch45

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	369
Mean	44.86
Std Dev	11.05

Turn on : 27.2814

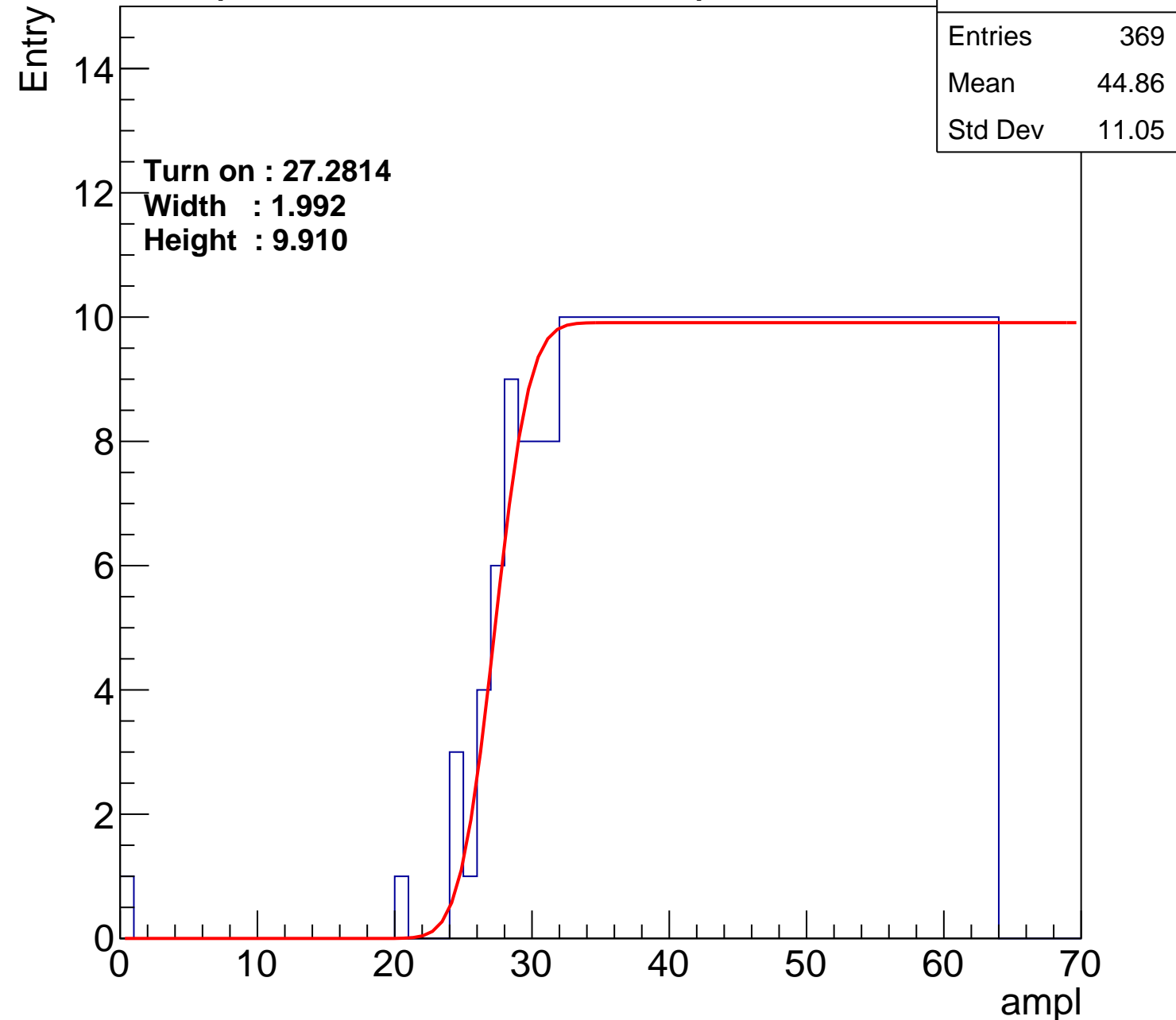
Width : 1.992

Height : 9.910

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch46

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	367
Mean	44.77
Std Dev	11.48

Turn on : 27.5836

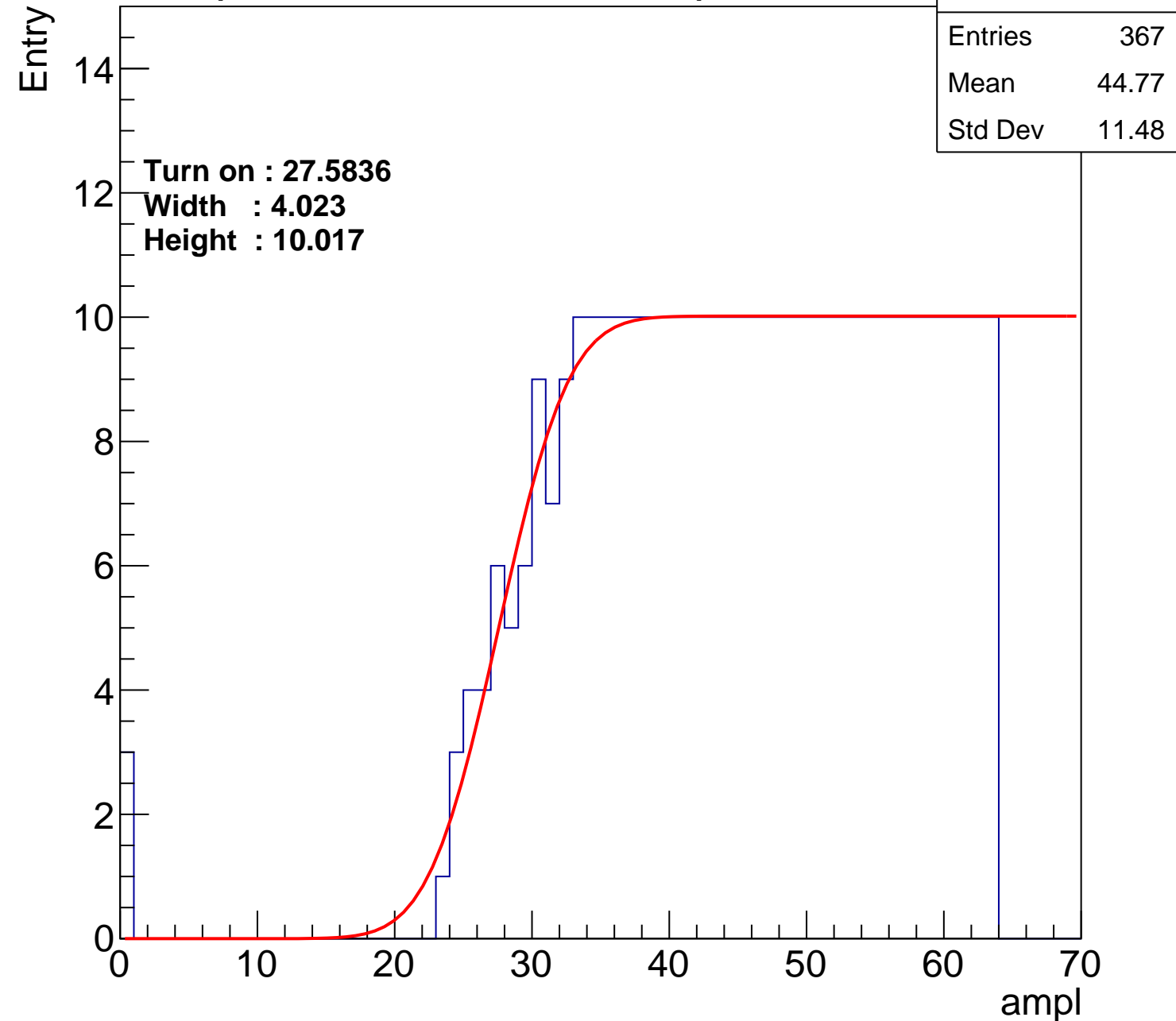
Width : 4.023

Height : 10.017

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U13-ch47

calib\_packv5\_042523\_0143.root, FC#4, port A2

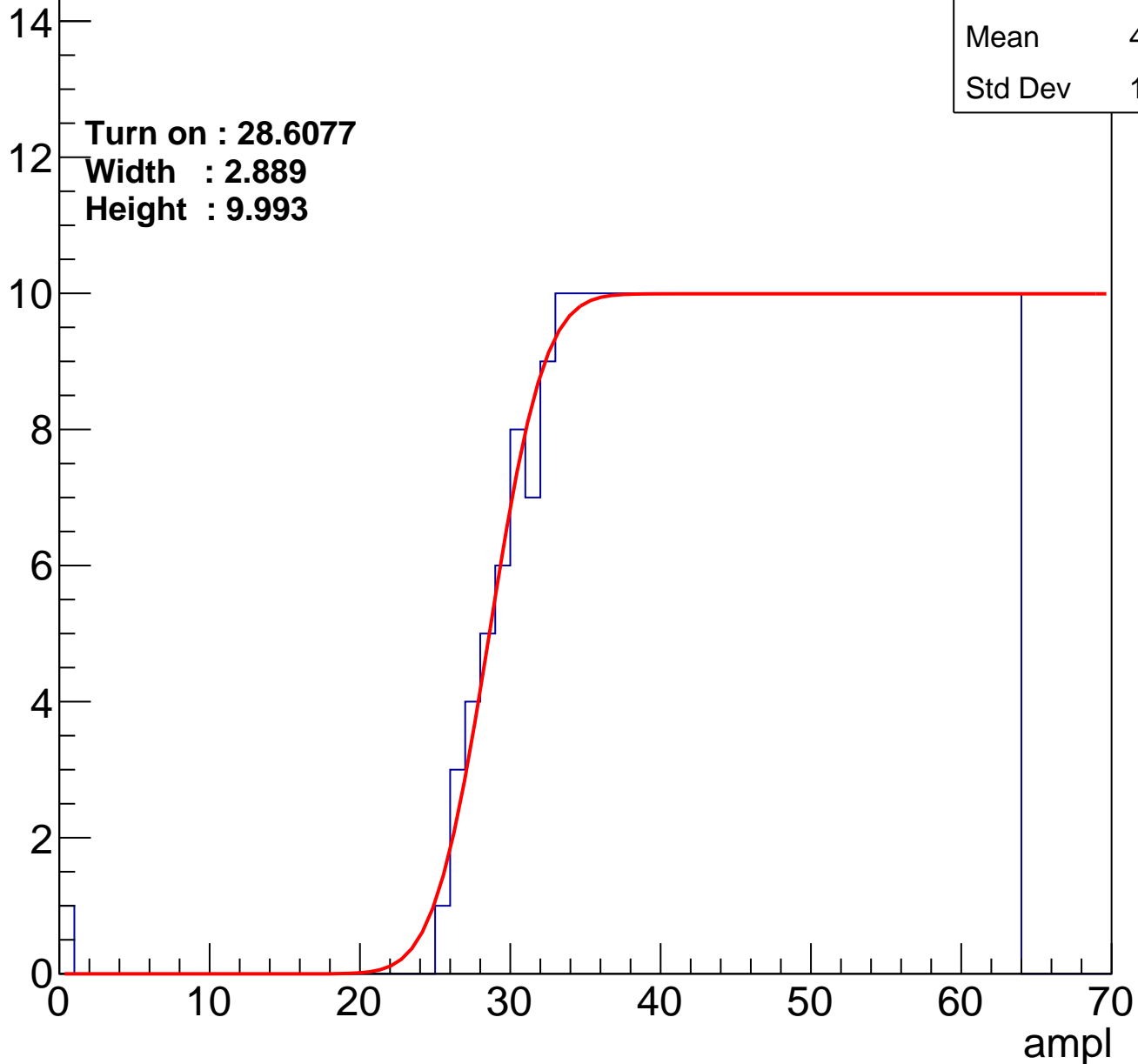
Entries	354
Mean	45.62
Std Dev	10.62

**Turn on : 28.6077**

**Width : 2.889**

**Height : 9.993**

Entry



# B1L100S, U13-ch48

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	356
Mean	45.44
Std Dev	10.91

Turn on : 28.6668

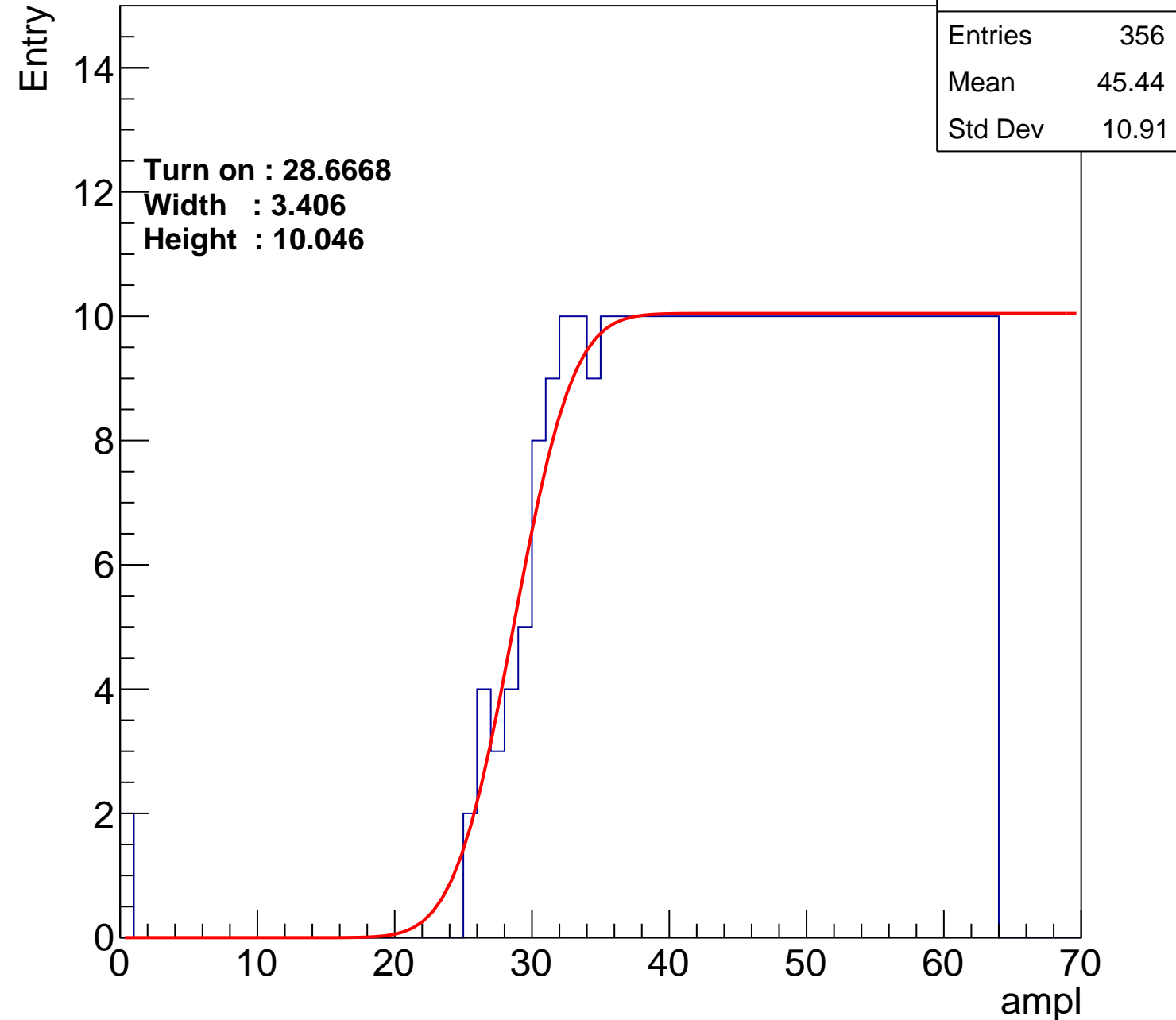
Width : 3.406

Height : 10.046

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch49

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	362
Mean	45.15
Std Dev	11.04

Turn on : 27.8706

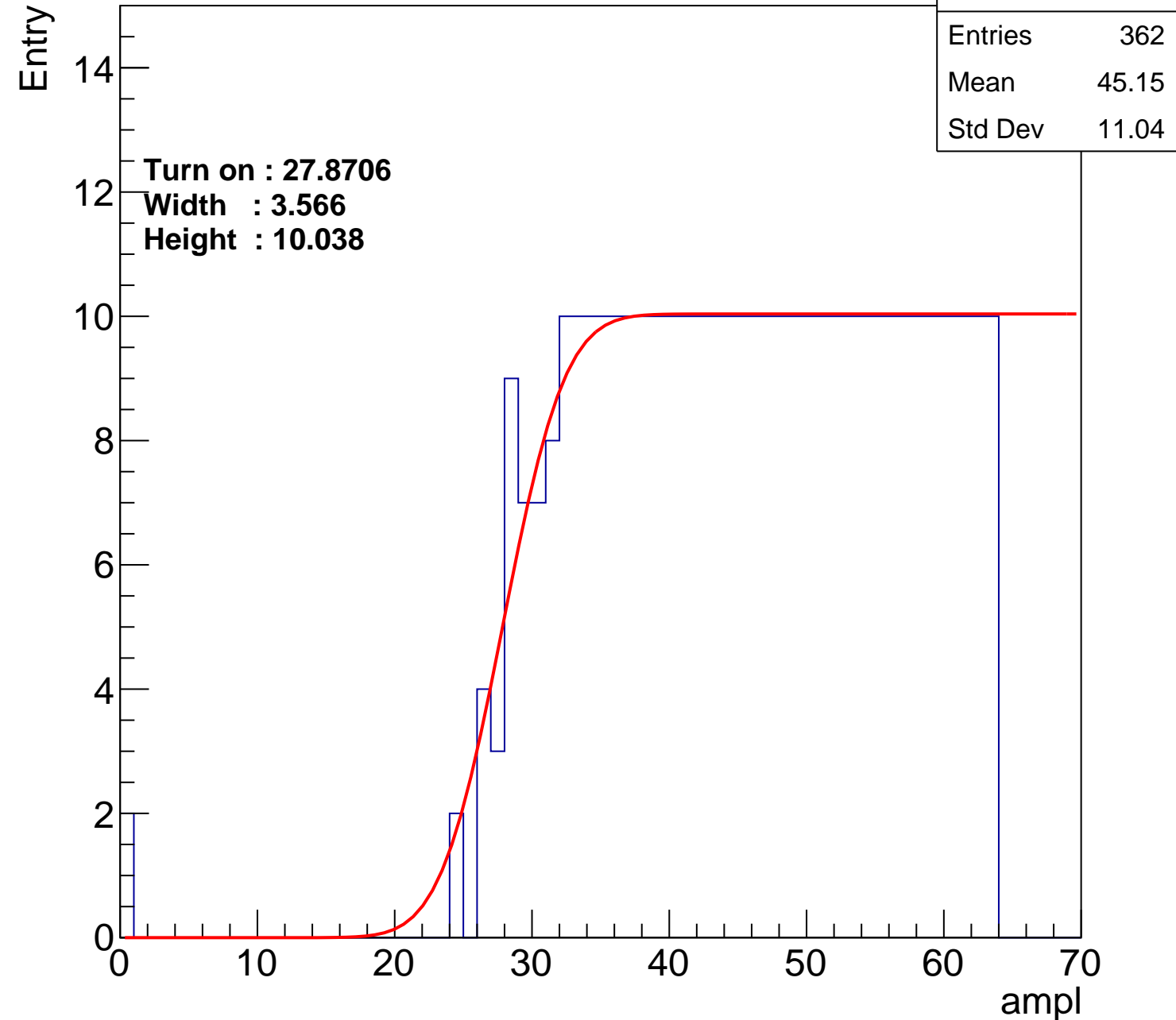
Width : 3.566

Height : 10.038

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch50

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	358
Mean	45.21
Std Dev	11.28

Turn on : 29.2819

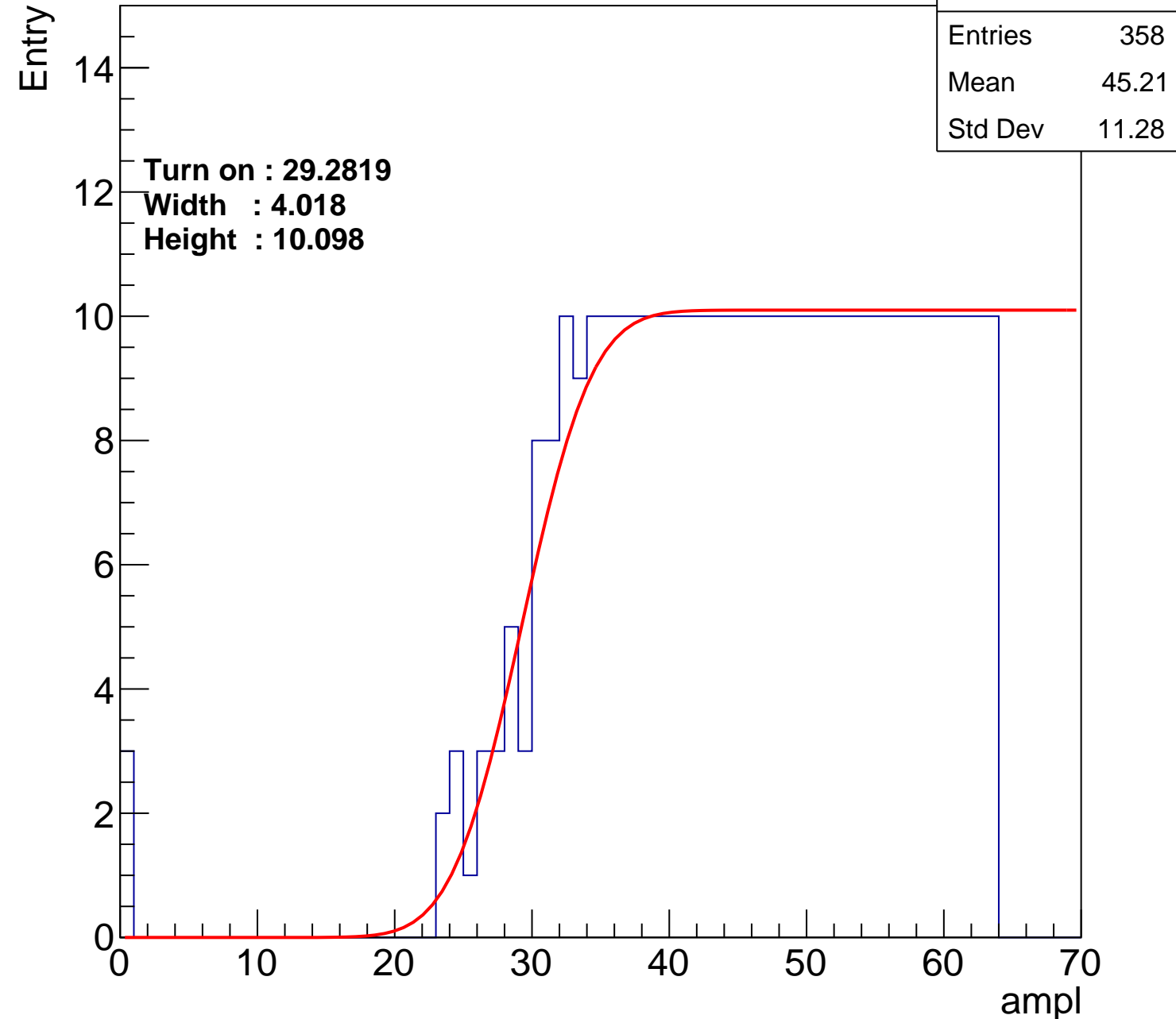
Width : 4.018

Height : 10.098

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch51

calib\_packv5\_042523\_0143.root, FC#4, port A2

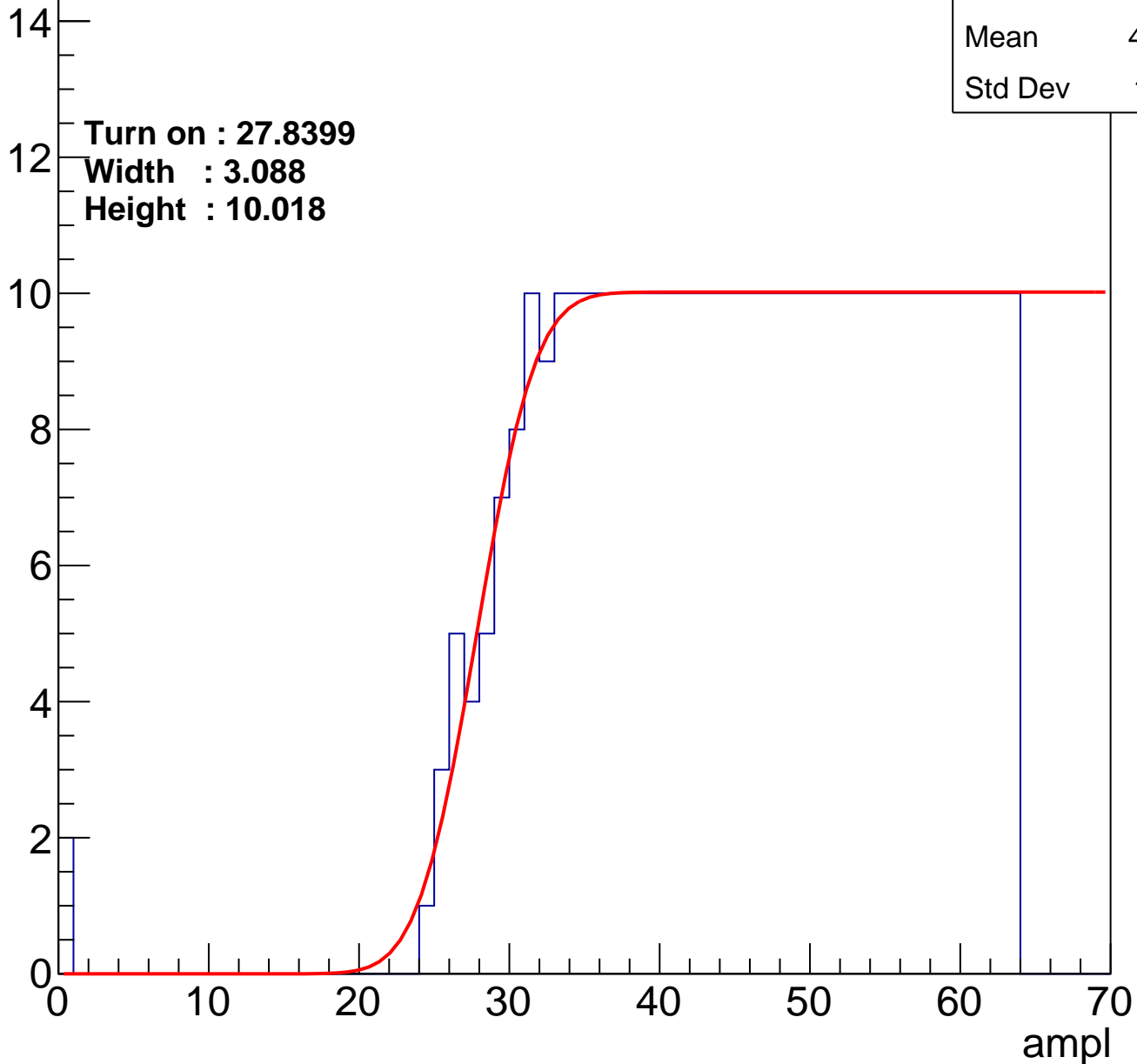
Entries	364
Mean	45.05
Std Dev	11.11

Turn on : 27.8399

Width : 3.088

Height : 10.018

Entry



# B1L100S, U13-ch52

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	365
Mean	45.13
Std Dev	10.82

Turn on : 27.5320

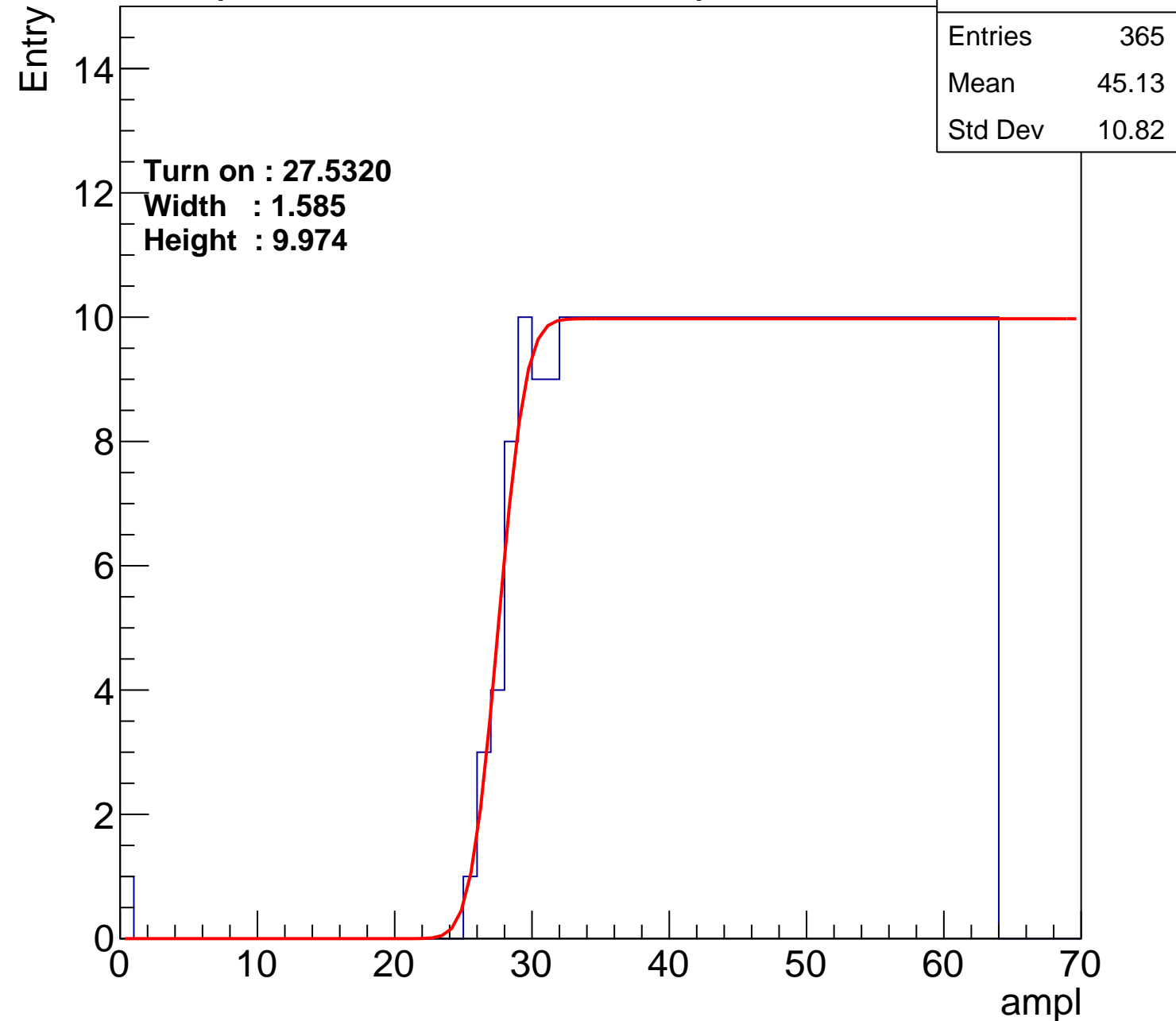
Width : 1.585

Height : 9.974

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch53

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	341
Mean	46.16
Std Dev	10.56

Turn on : 30.1697

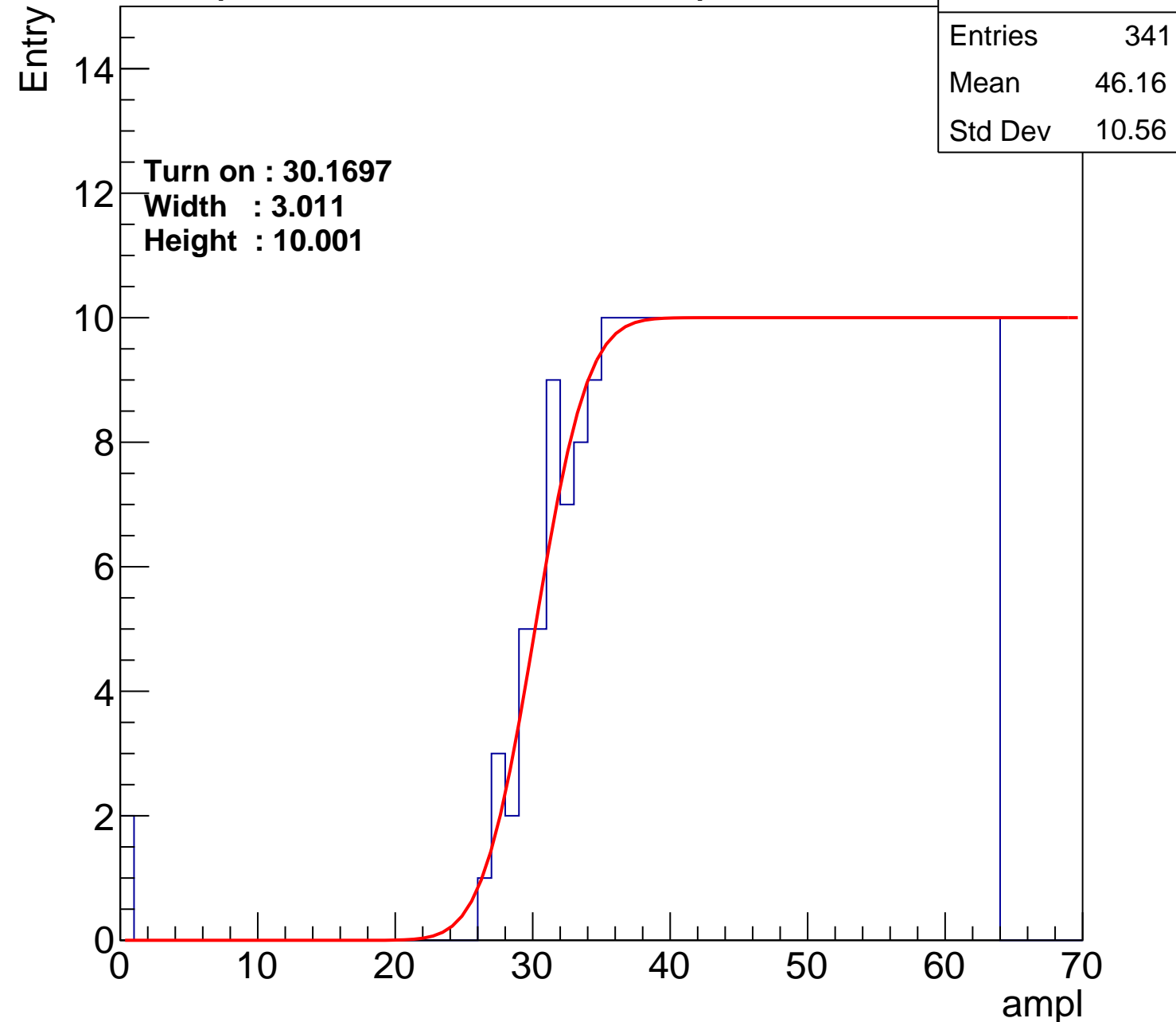
Width : 3.011

Height : 10.001

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch54

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	370
Mean	44.82
Std Dev	11.06

Turn on : 27.5045

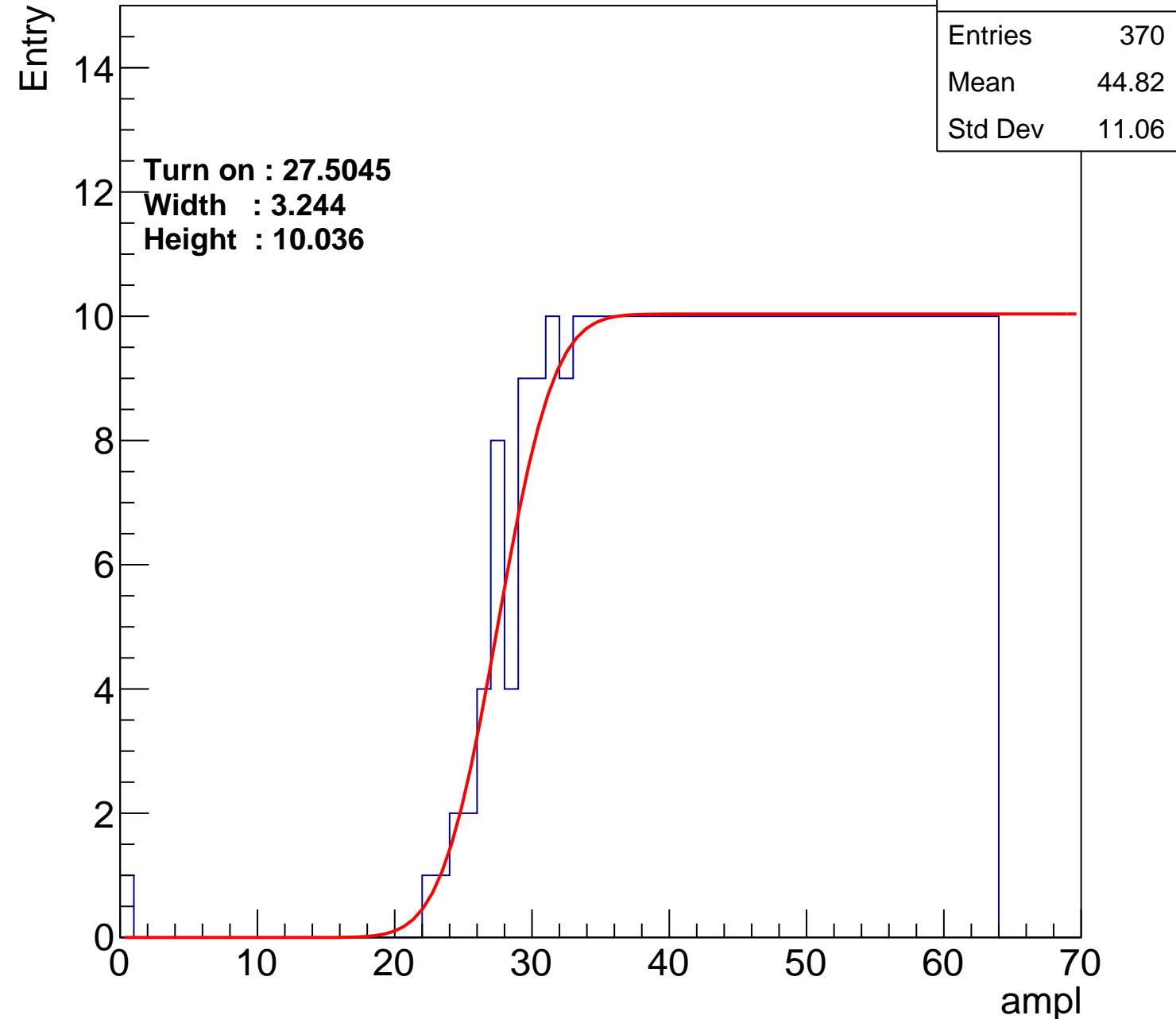
Width : 3.244

Height : 10.036

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U13-ch55

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	382
Mean	44.08
Std Dev	11.78

Turn on : 26.4719

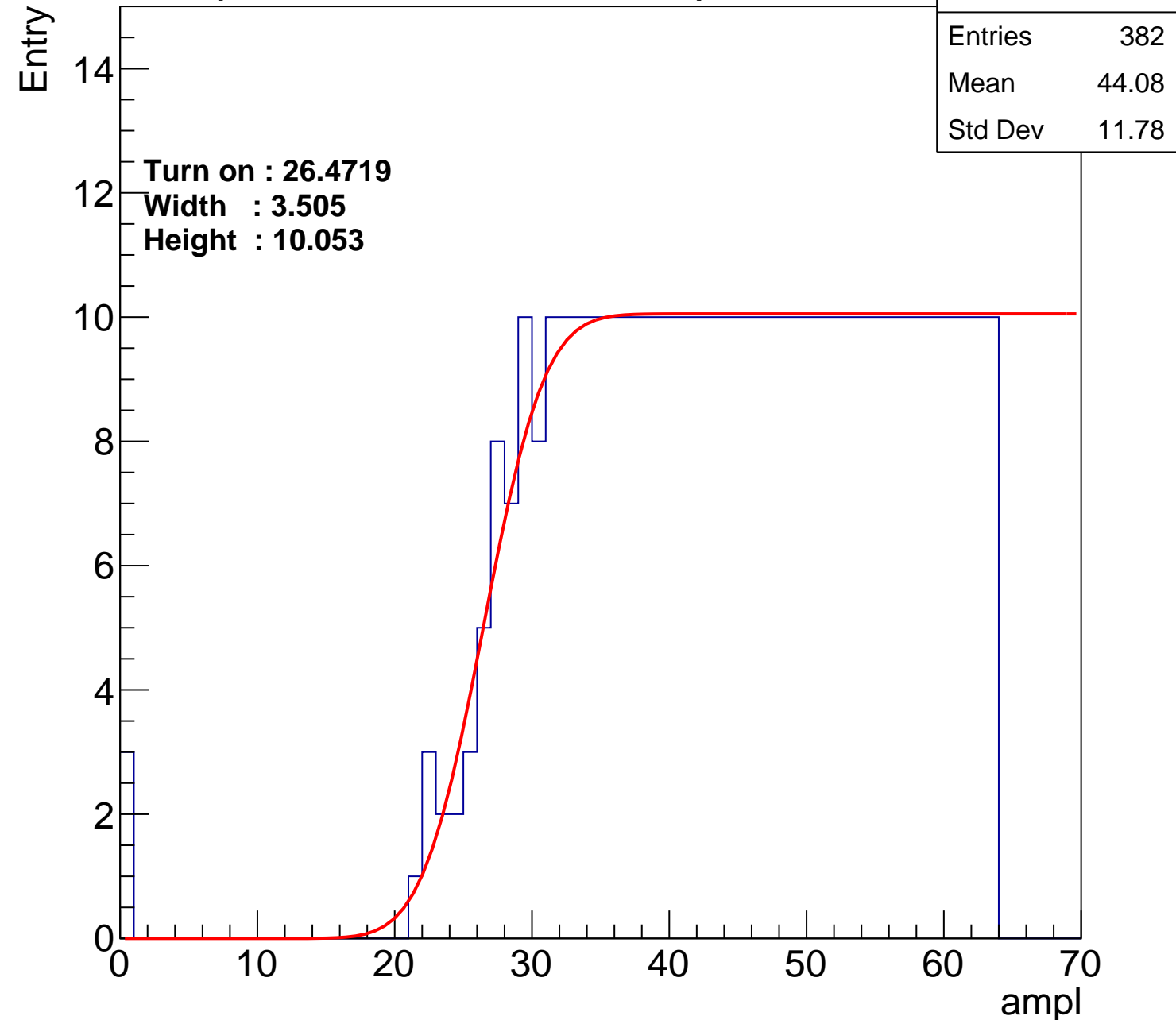
Width : 3.505

Height : 10.053

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch56

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	336
Mean	46.24
Std Dev	10.84

Turn on : 31.5257

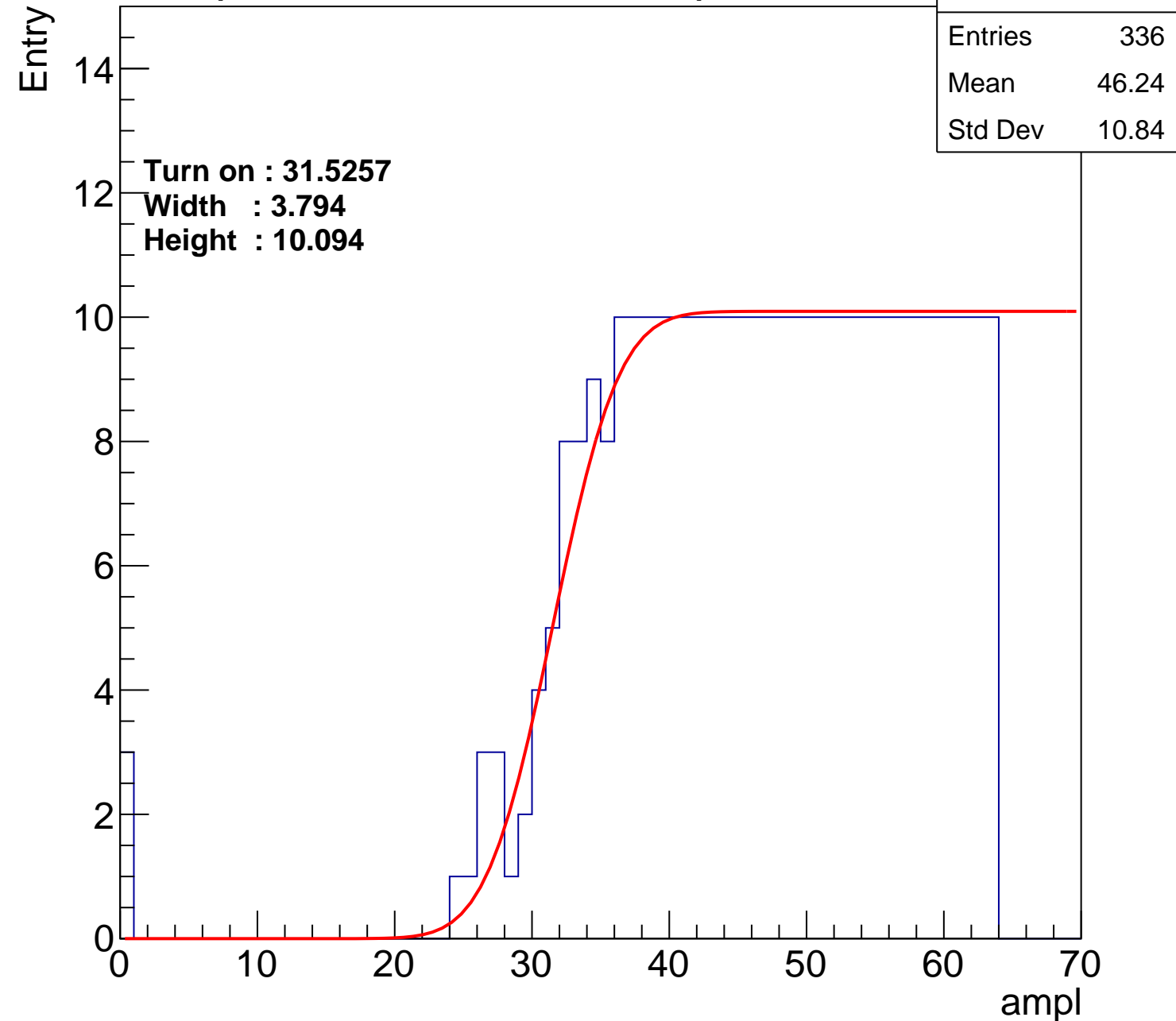
Width : 3.794

Height : 10.094

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch57

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	376
Mean	44.52
Std Dev	11.23

Turn on : 26.6764

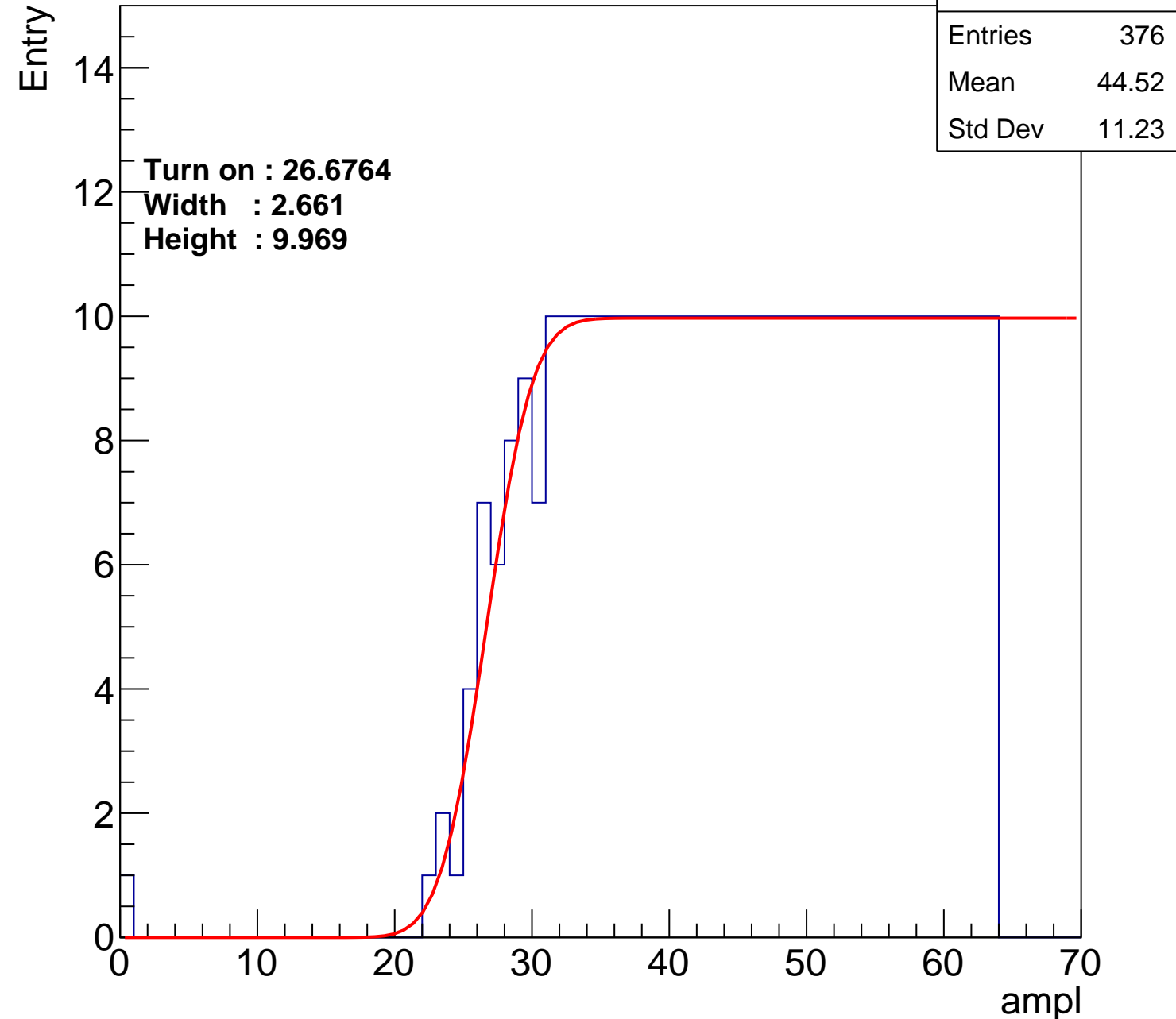
Width : 2.661

Height : 9.969

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch58

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	368
Mean	44.89
Std Dev	11.07

Turn on : 27.8210

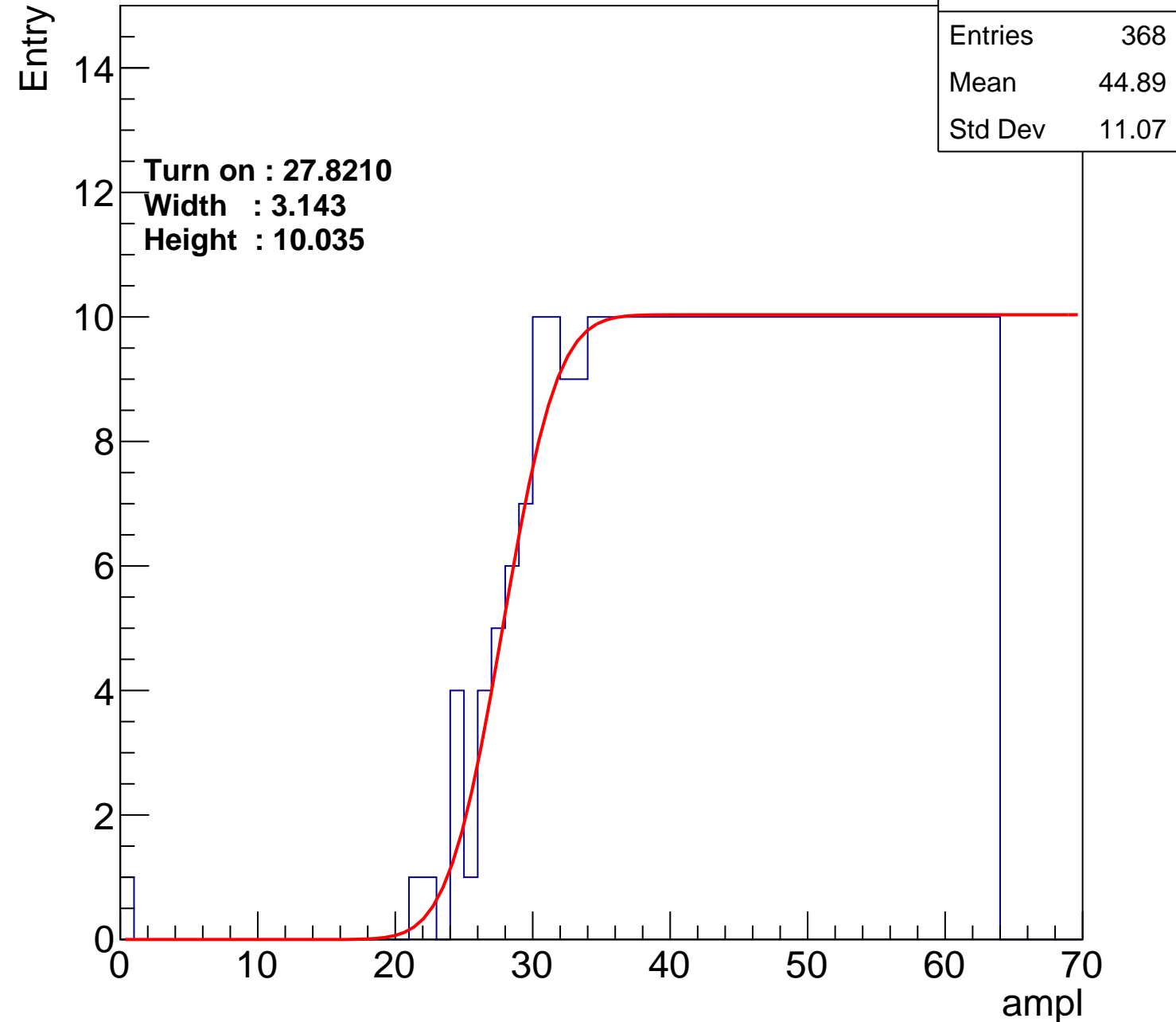
Width : 3.143

Height : 10.035

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch59

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	369
Mean	44.89
Std Dev	11.01

Turn on : 27.6166

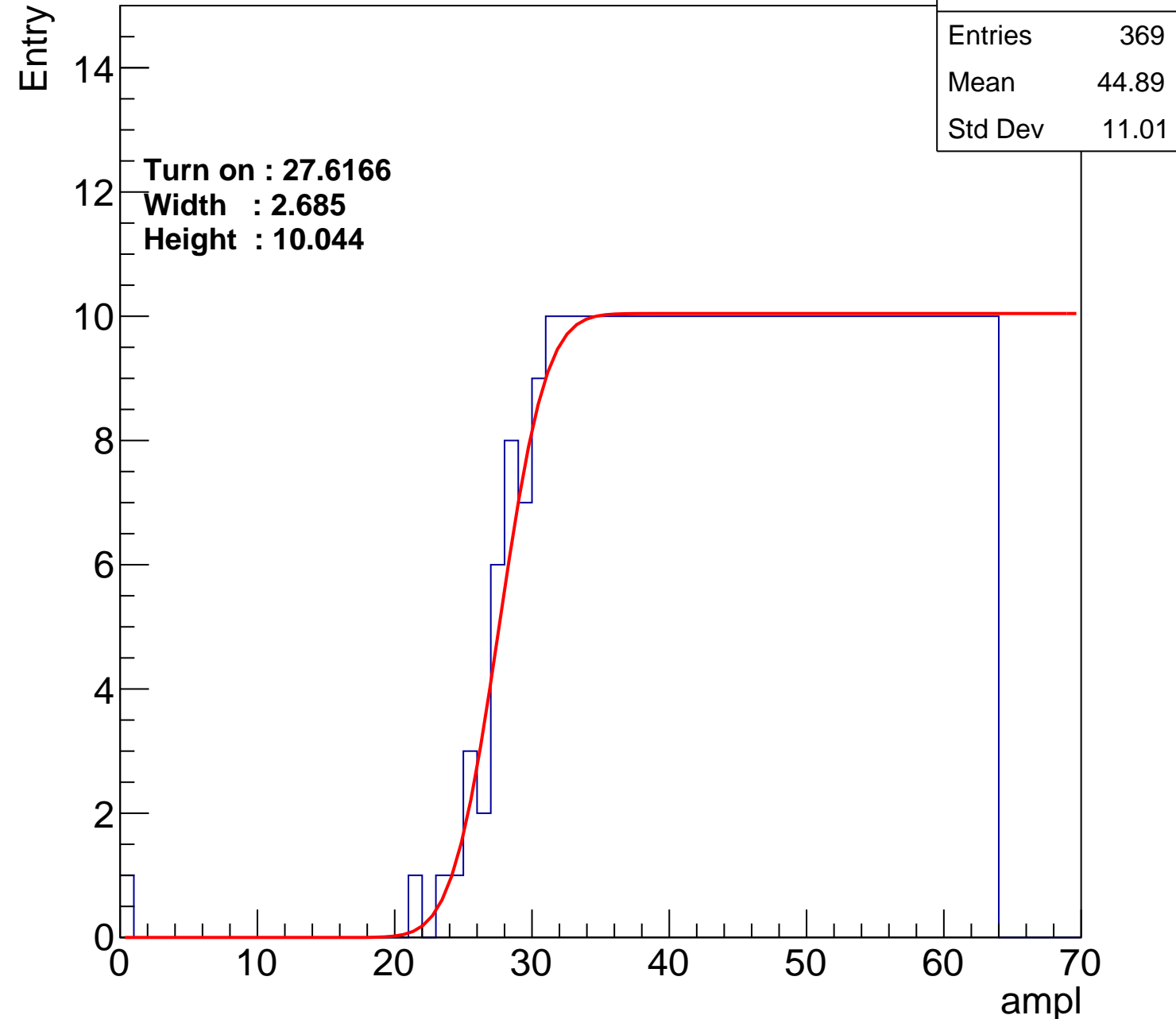
Width : 2.685

Height : 10.044

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch60

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	365
Mean	44.98
Std Dev	11.17

Turn on : 28.1376

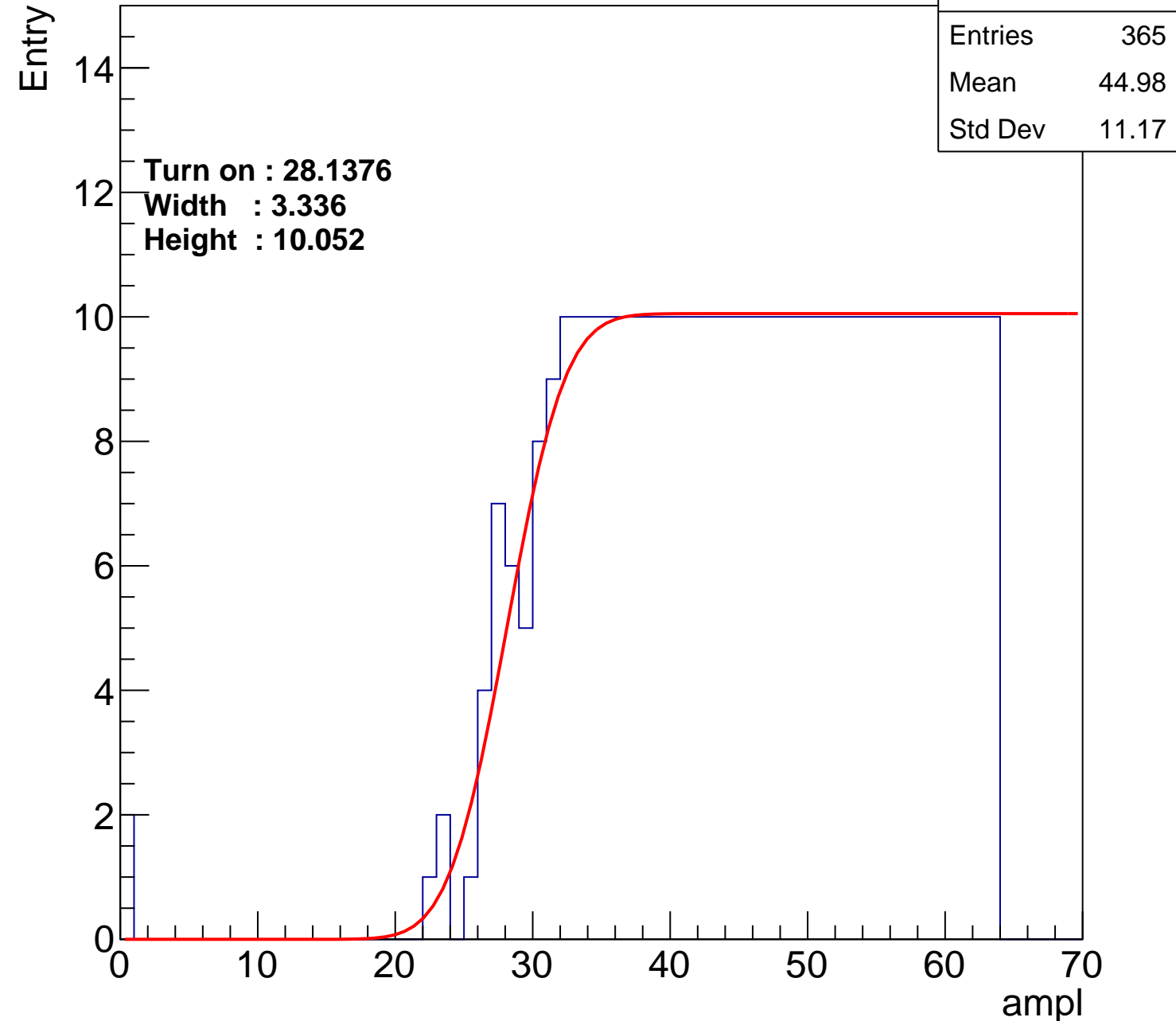
Width : 3.336

Height : 10.052

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch61

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	364
Mean	45.09
Std Dev	10.95

**Turn on : 27.9253**

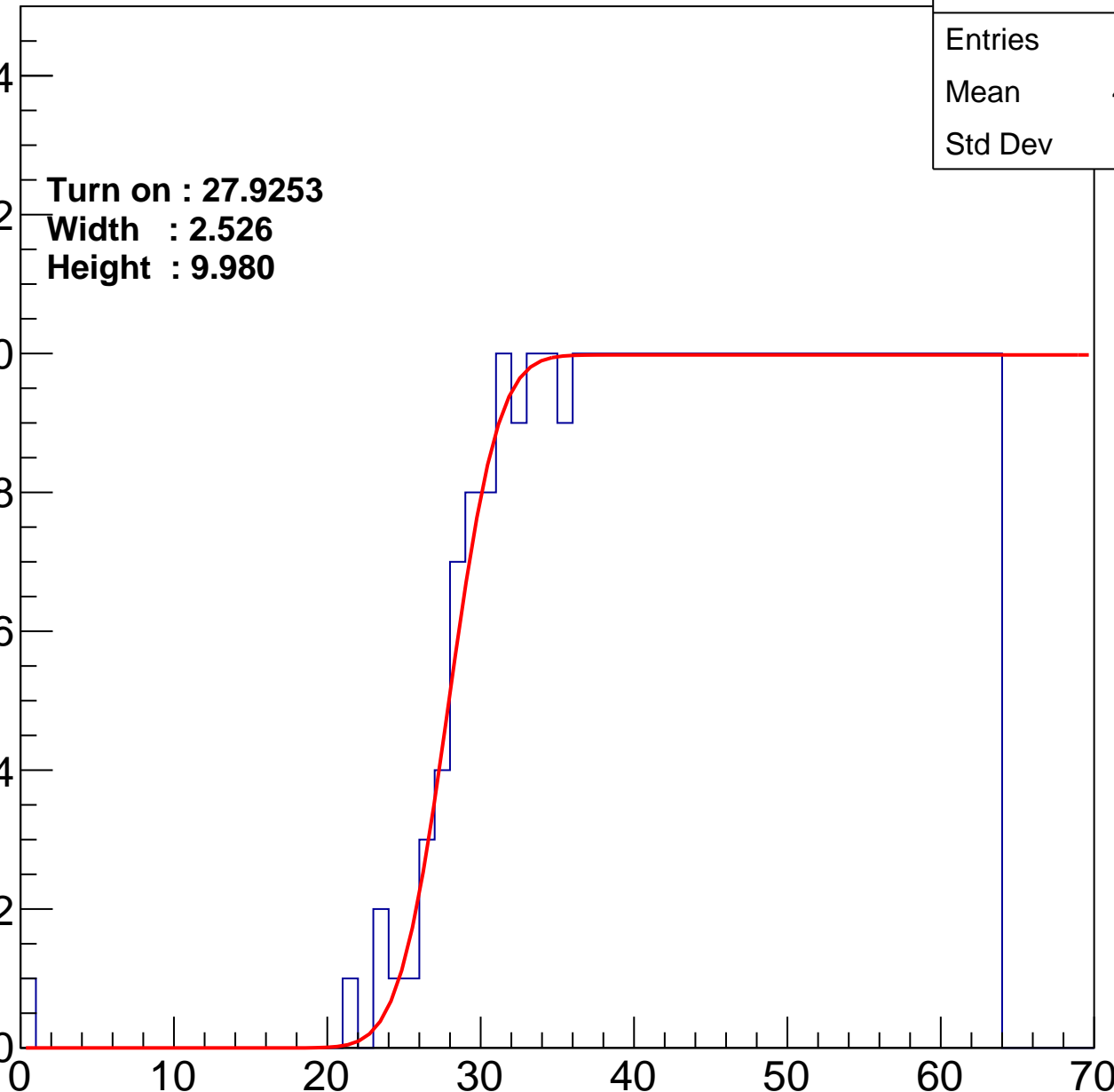
**Width : 2.526**

**Height : 9.980**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch62

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	381
Mean	44.1
Std Dev	11.79

**Turn on : 26.6067**

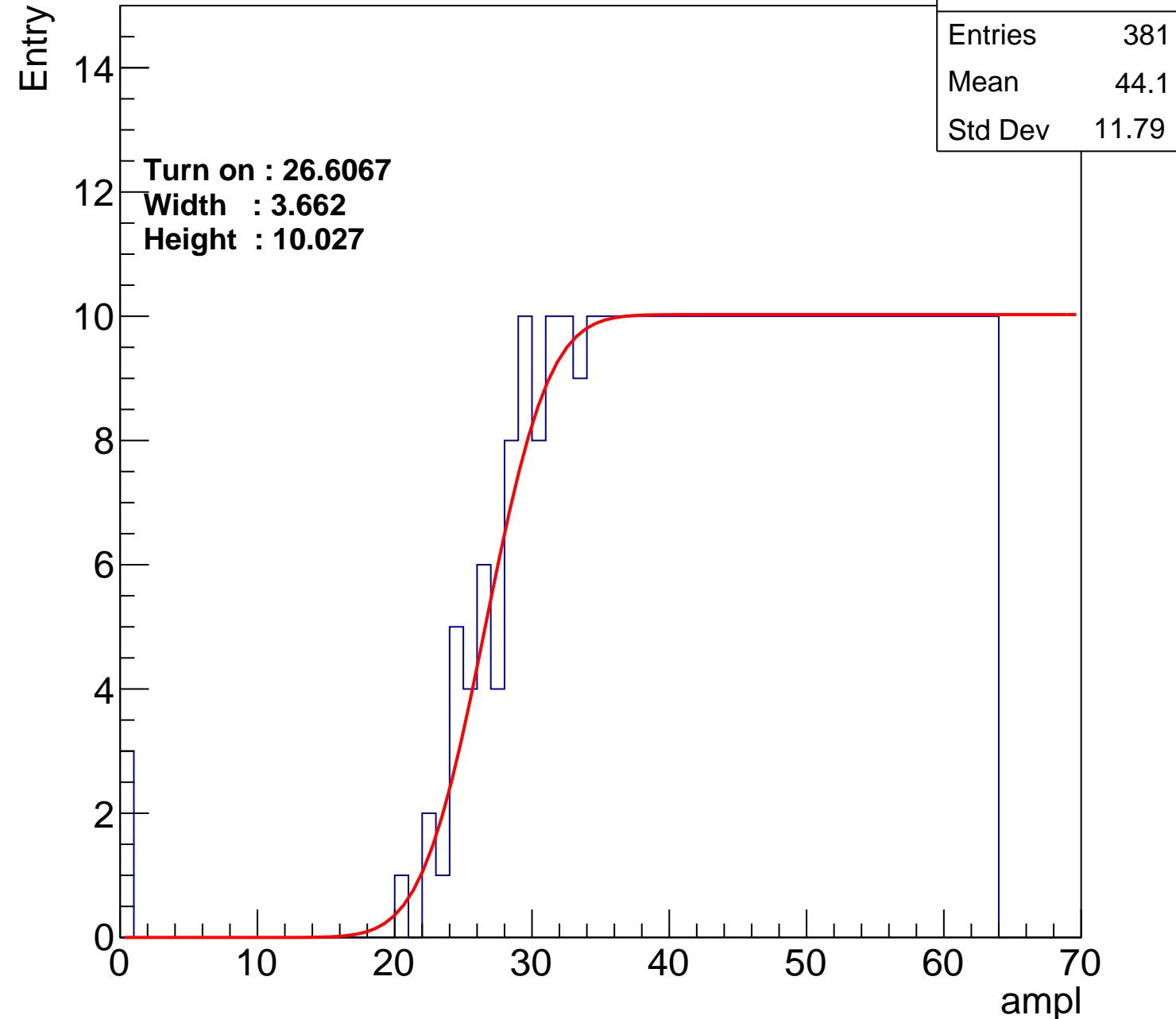
**Width : 3.662**

**Height : 10.027**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U13-ch63

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	356
Mean	45.34
Std Dev	11.16

Turn on : 28.5059

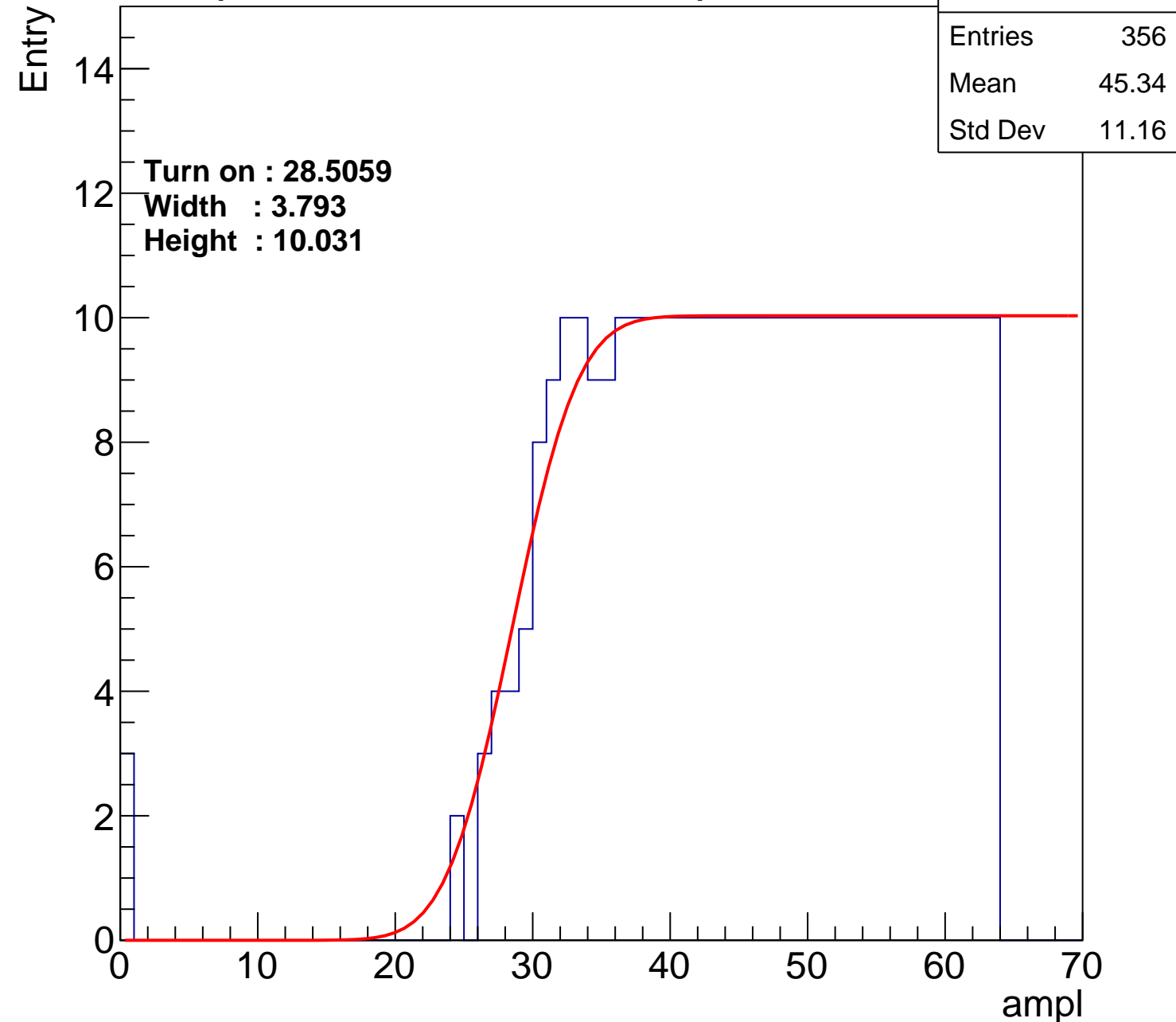
Width : 3.793

Height : 10.031

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch64

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	363
Mean	45.18
Std Dev	10.86

Turn on : 27.8943

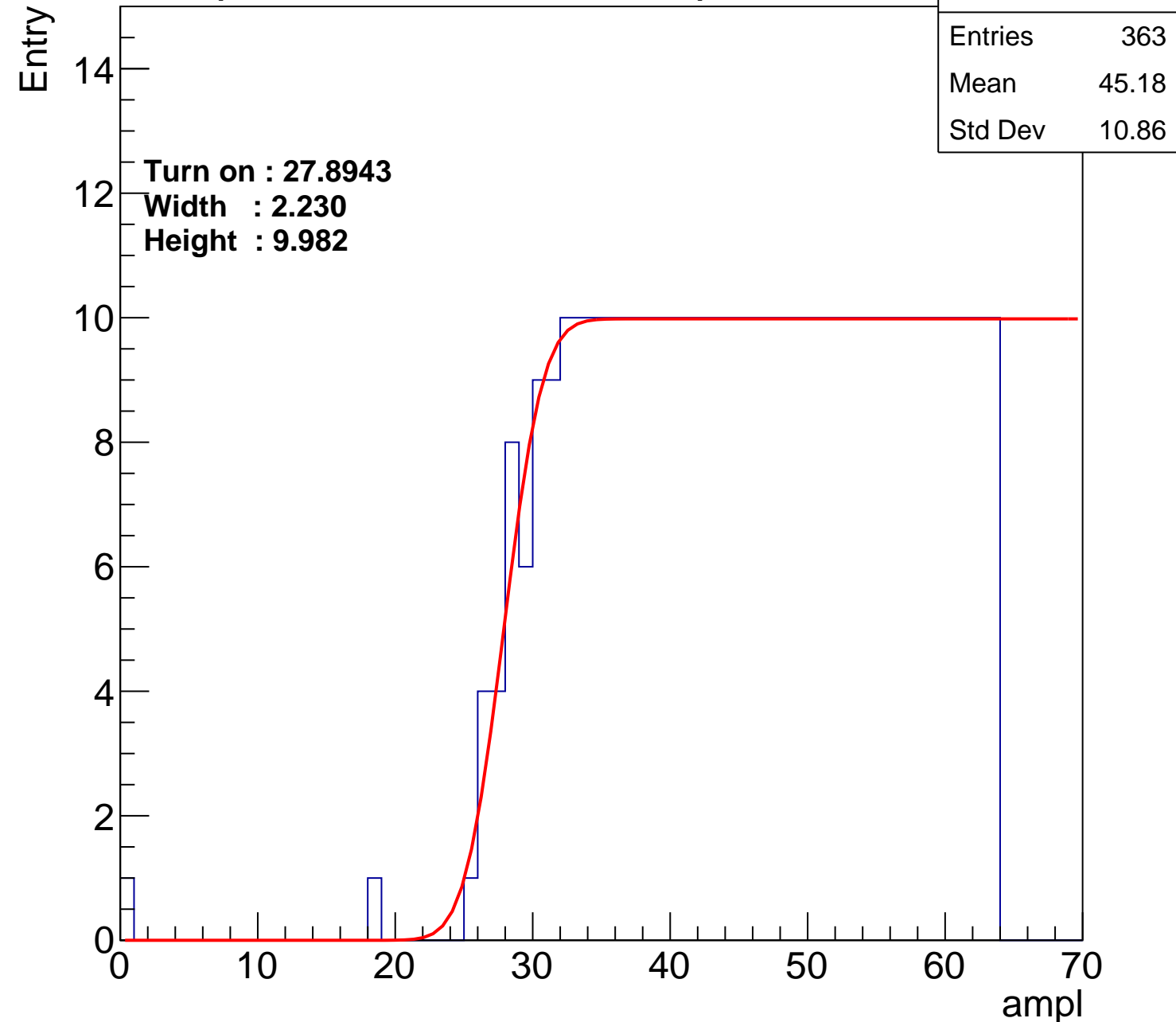
Width : 2.230

Height : 9.982

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch65

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	362
Mean	45.23
Std Dev	10.83

Turn on : 27.7928

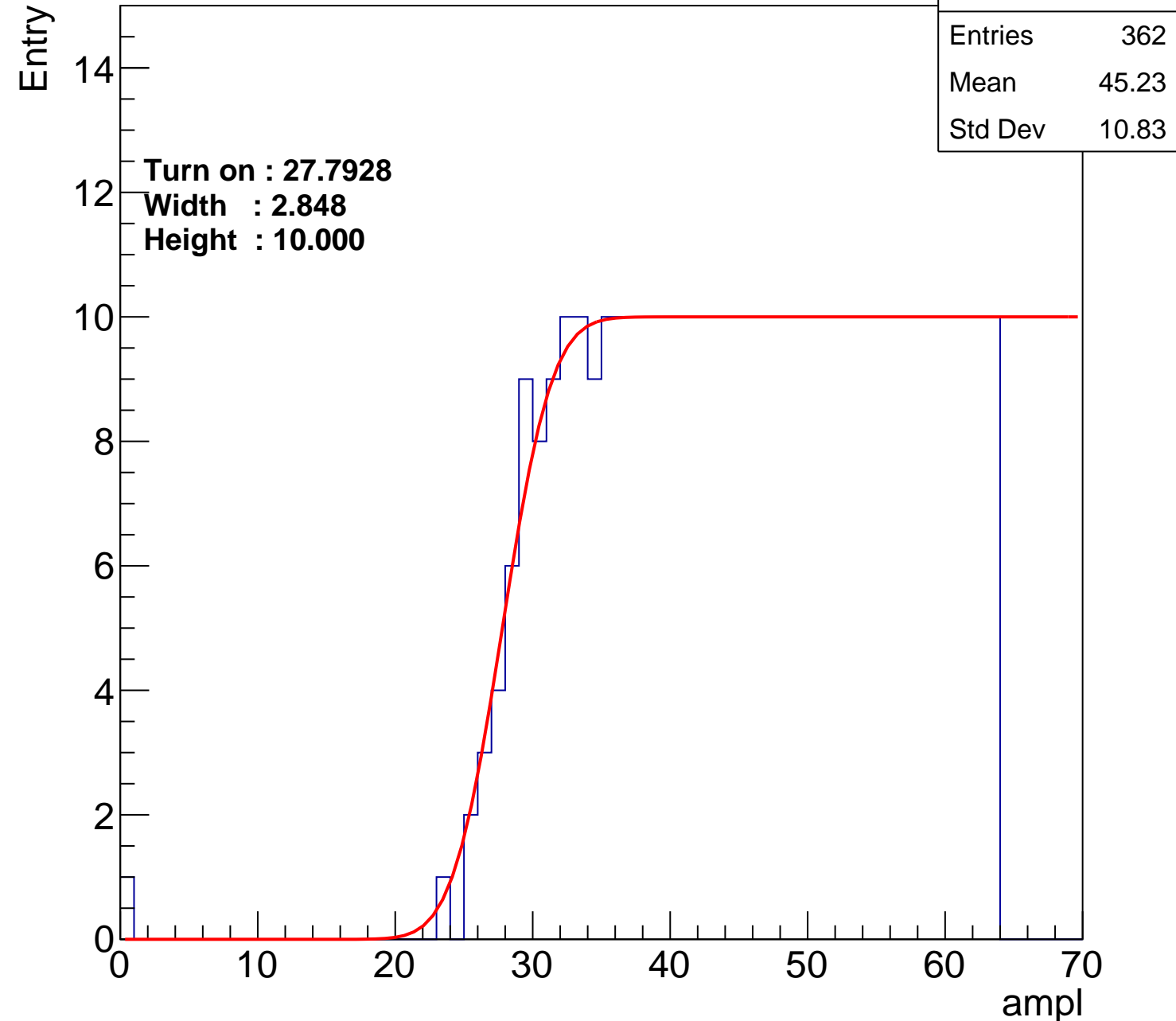
Width : 2.848

Height : 10.000

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch66

calib\_packv5\_042523\_0143.root, FC#4, port A2

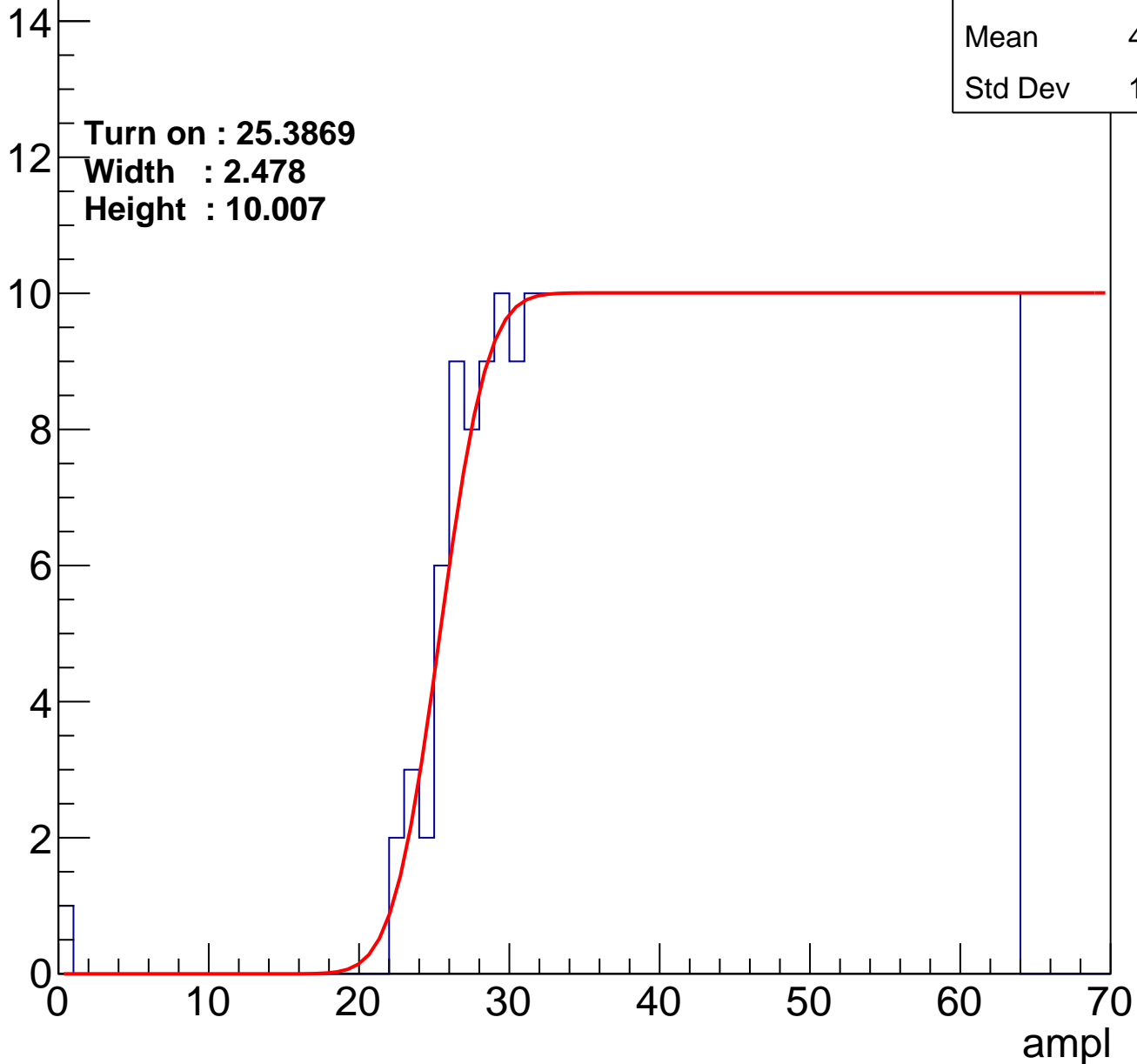
Entries	389
Mean	43.92
Std Dev	11.52

Turn on : 25.3869

Width : 2.478

Height : 10.007

Entry



# B1L100S, U13-ch67

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	358
Mean	45.15
Std Dev	11.45

Turn on : 29.2851

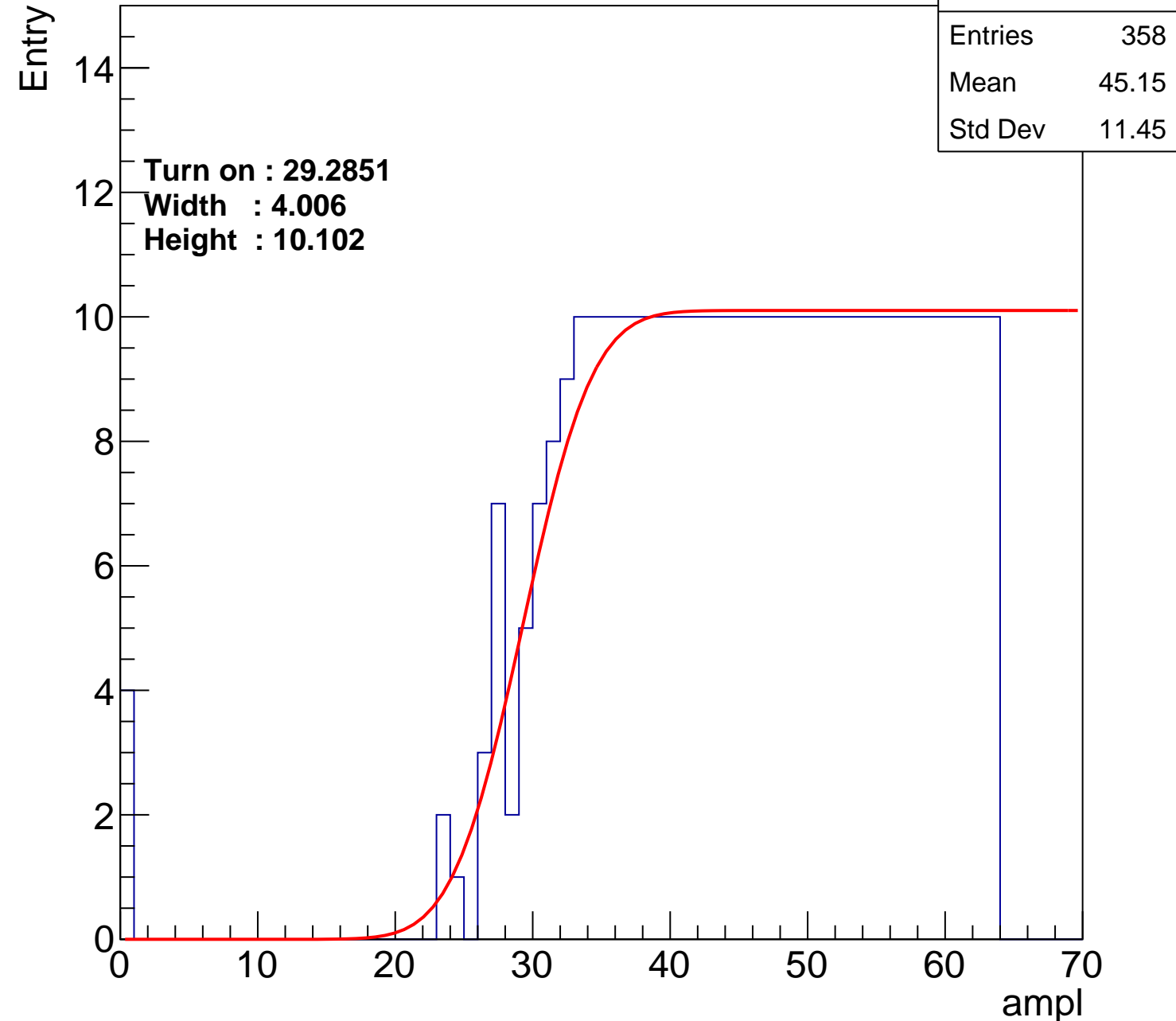
Width : 4.006

Height : 10.102

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch68

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	386
Mean	43.78
Std Dev	12.17

Turn on : 26.5158

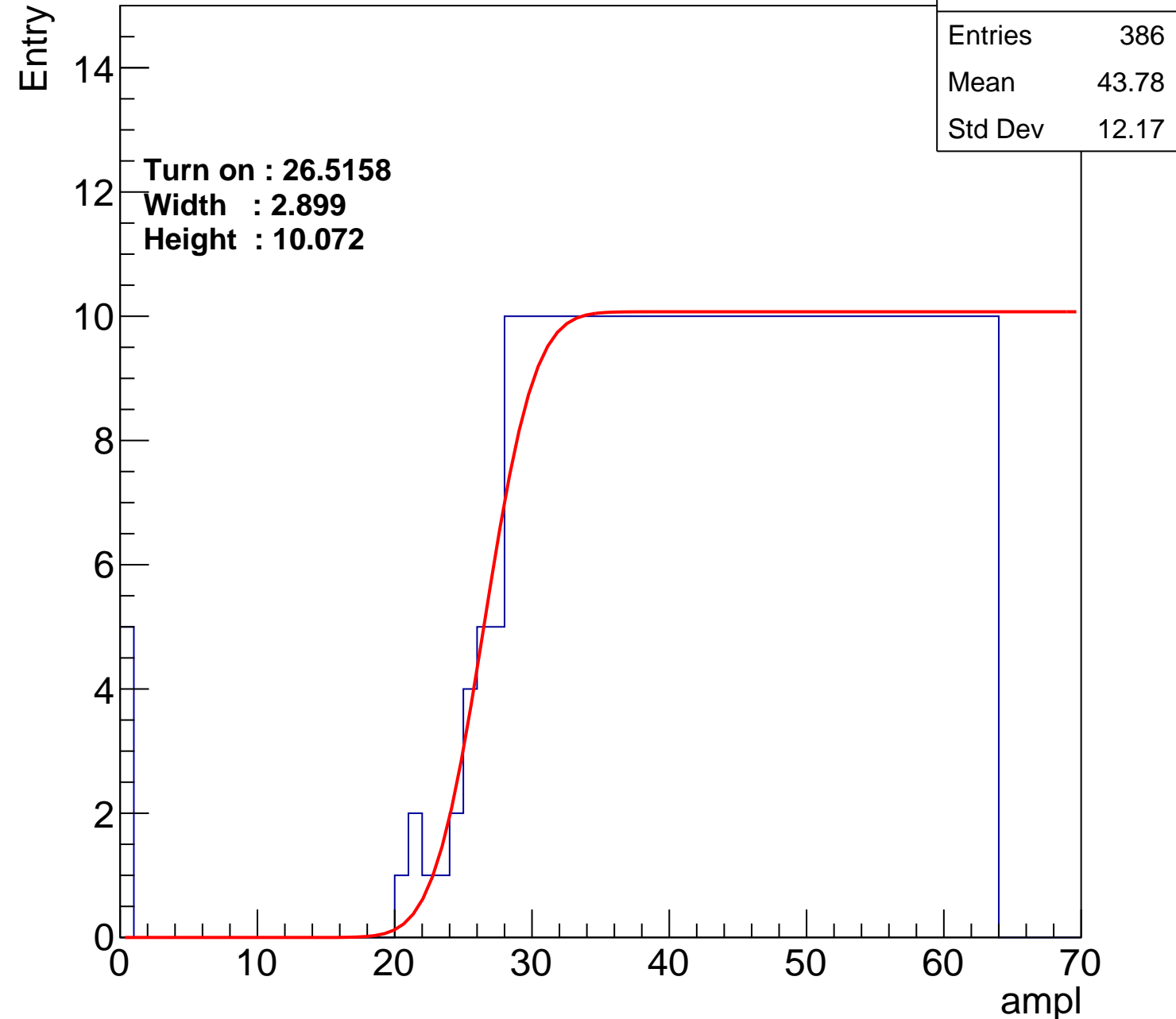
Width : 2.899

Height : 10.072

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch69

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	357
Mean	45.23
Std Dev	11.29

**Turn on : 28.5457**

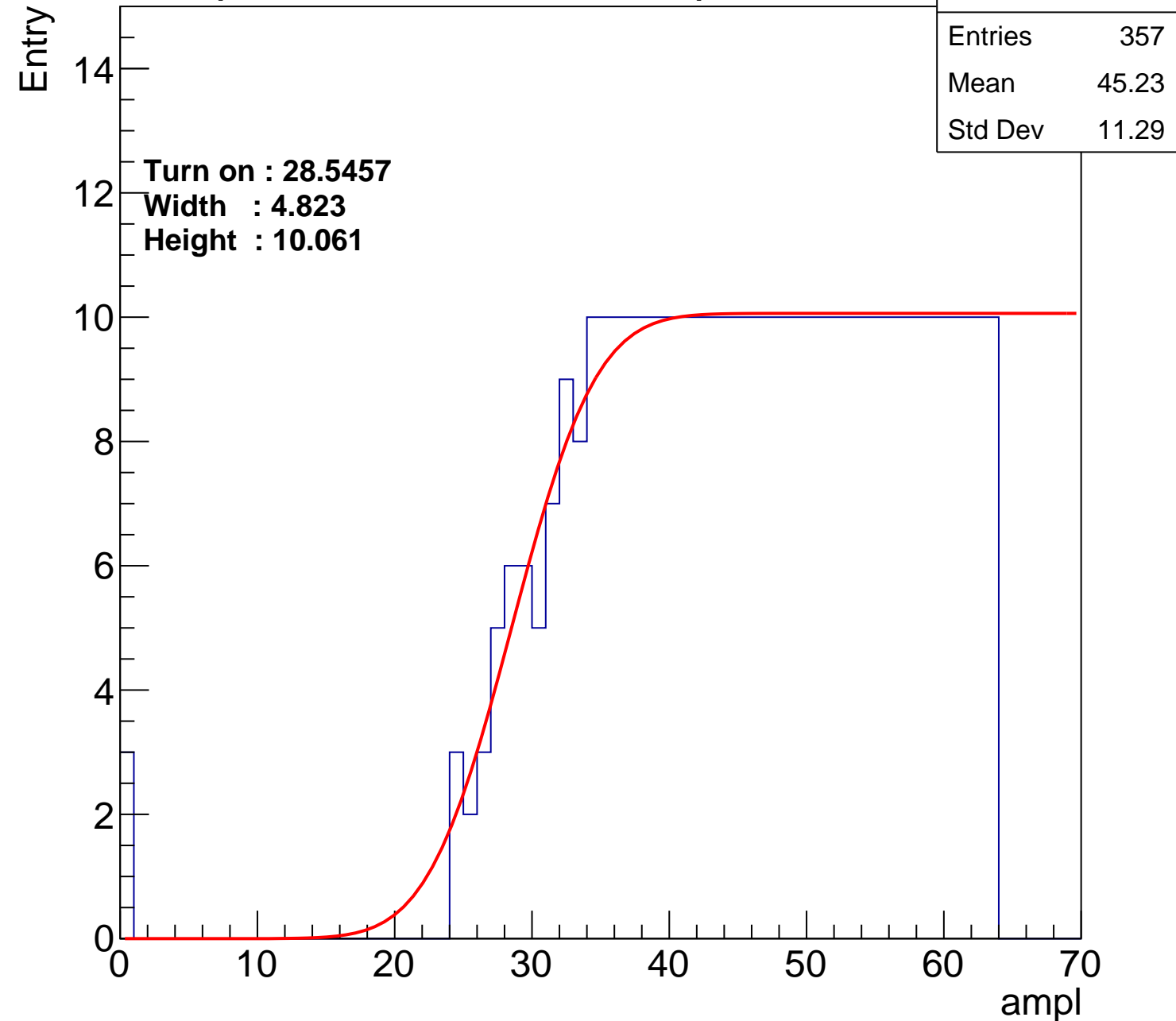
**Width : 4.823**

**Height : 10.061**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch70

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	372
Mean	44.66
Std Dev	11.3

Turn on : 27.3823

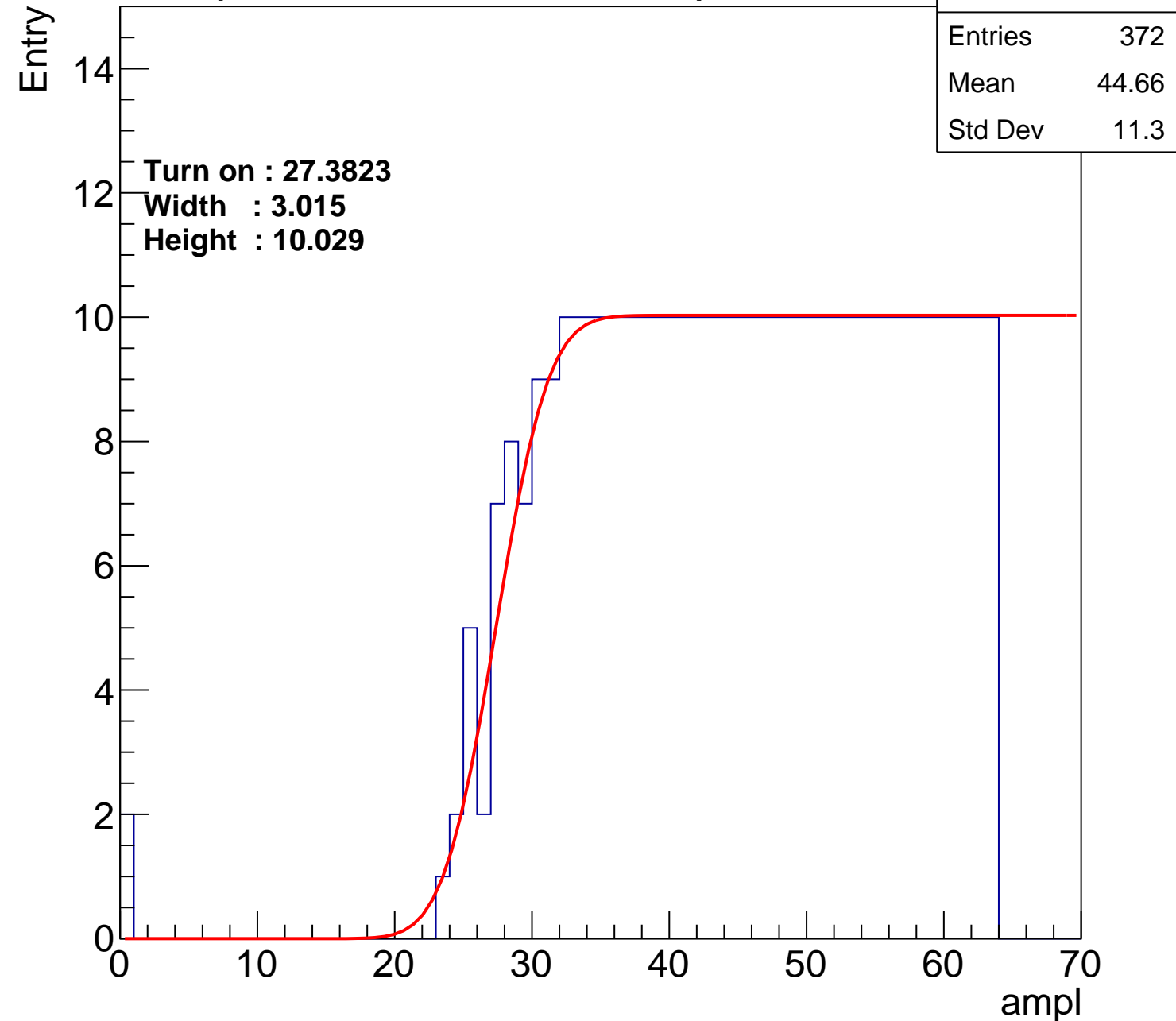
Width : 3.015

Height : 10.029

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U13-ch71

calib\_packv5\_042523\_0143.root, FC#4, port A2

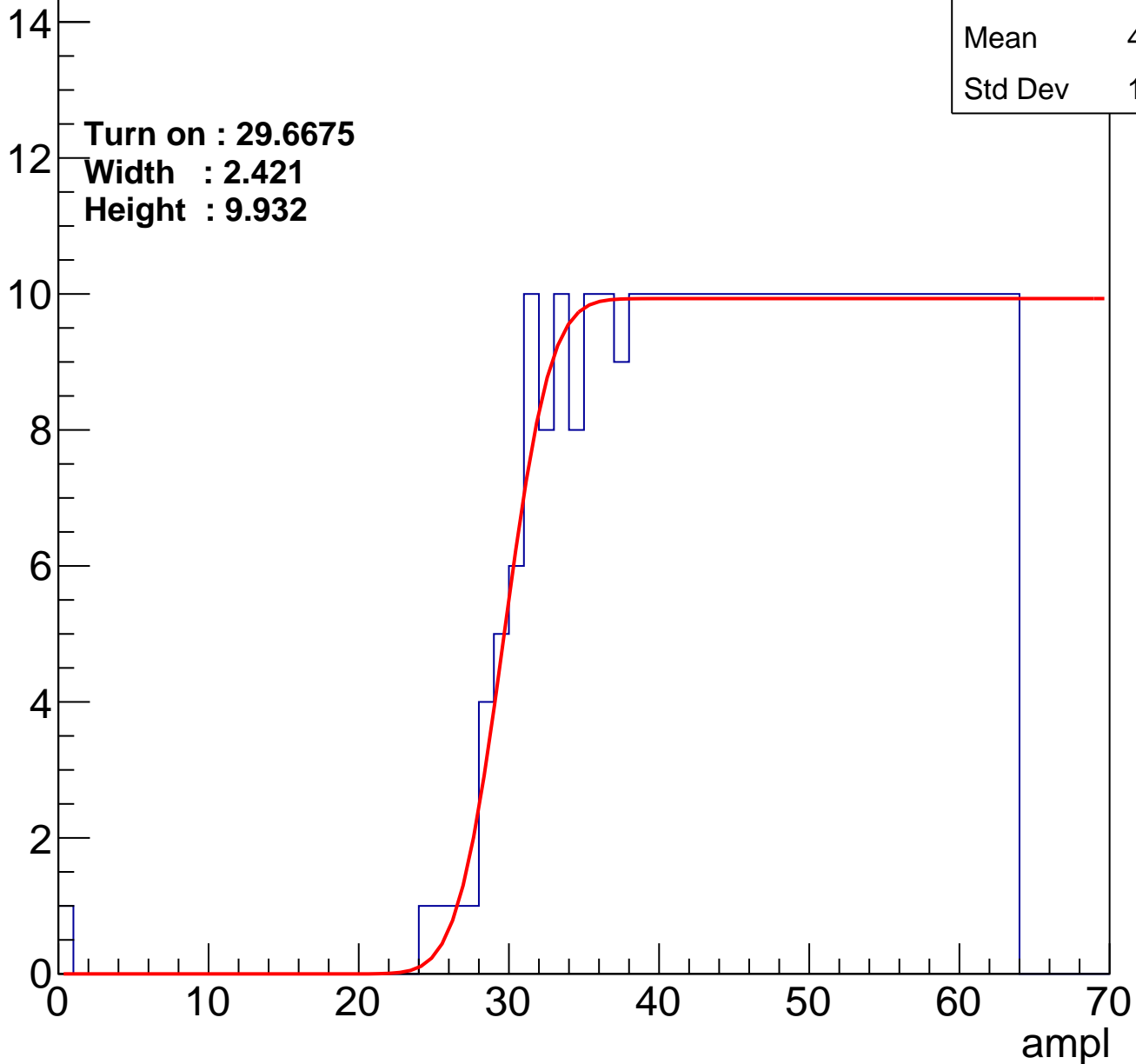
Entry

Entries	345
Mean	46.03
Std Dev	10.44

Turn on : 29.6675

Width : 2.421

Height : 9.932



# B1L100S, U13-ch72

calib\_packv5\_042523\_0143.root, FC#4, port A2

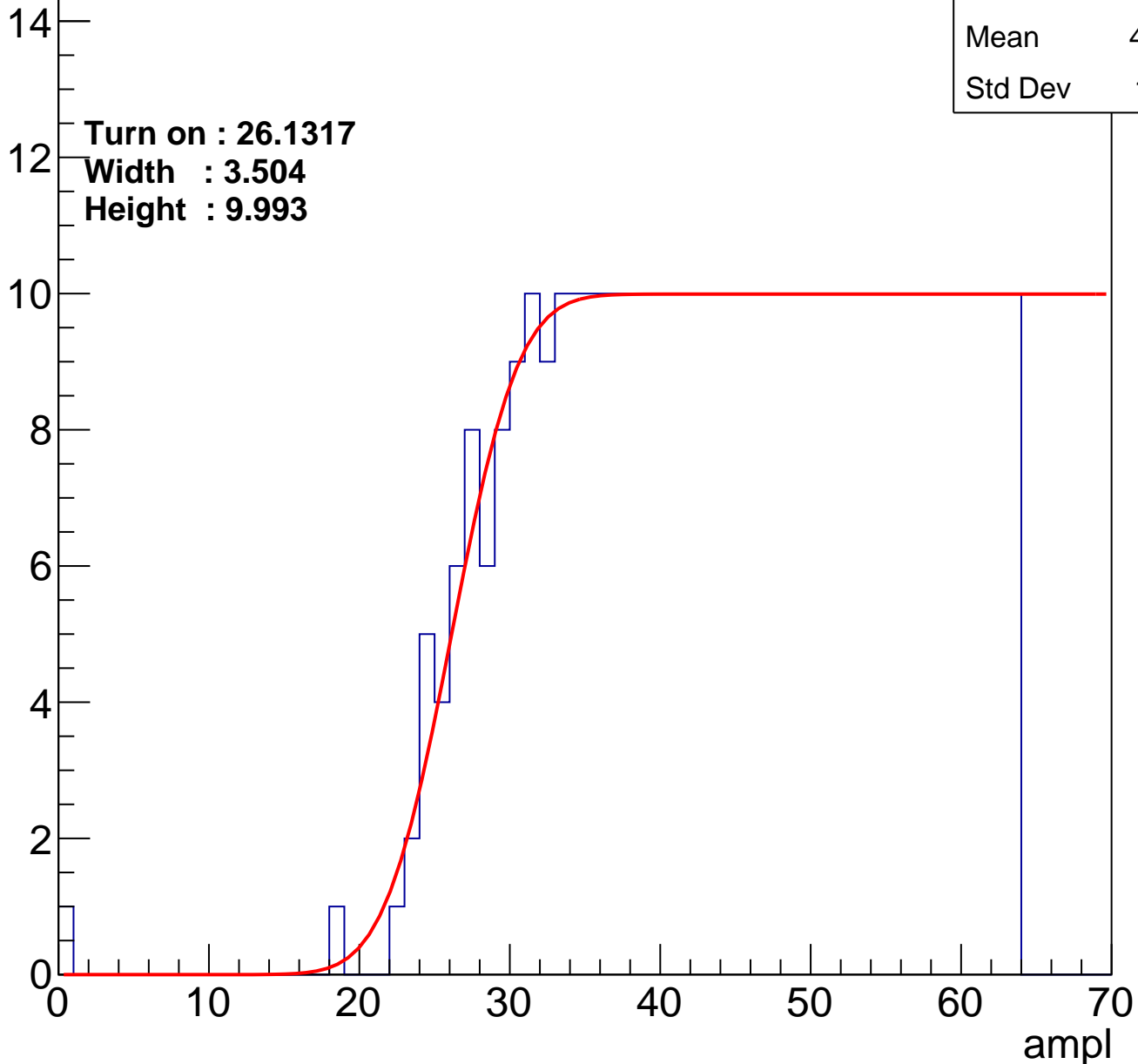
Entries	380
Mean	44.28
Std Dev	11.41

Turn on : 26.1317

Width : 3.504

Height : 9.993

Entry



# B1L100S, U13-ch73

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	367
Mean	44.98
Std Dev	10.97

**Turn on : 27.5047**

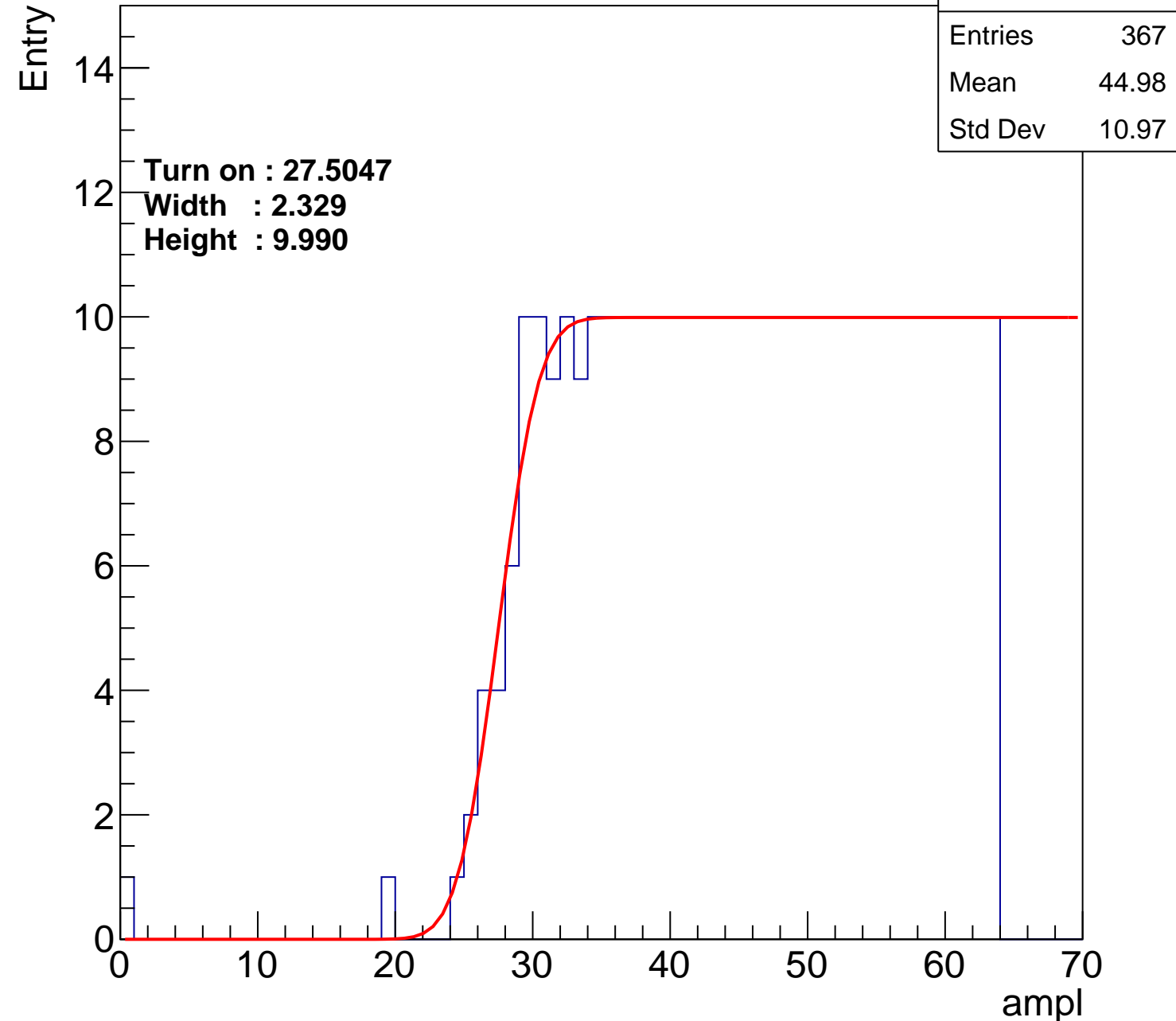
**Width : 2.329**

**Height : 9.990**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch74

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	363
Mean	45.1
Std Dev	11.09

Turn on : 28.7483

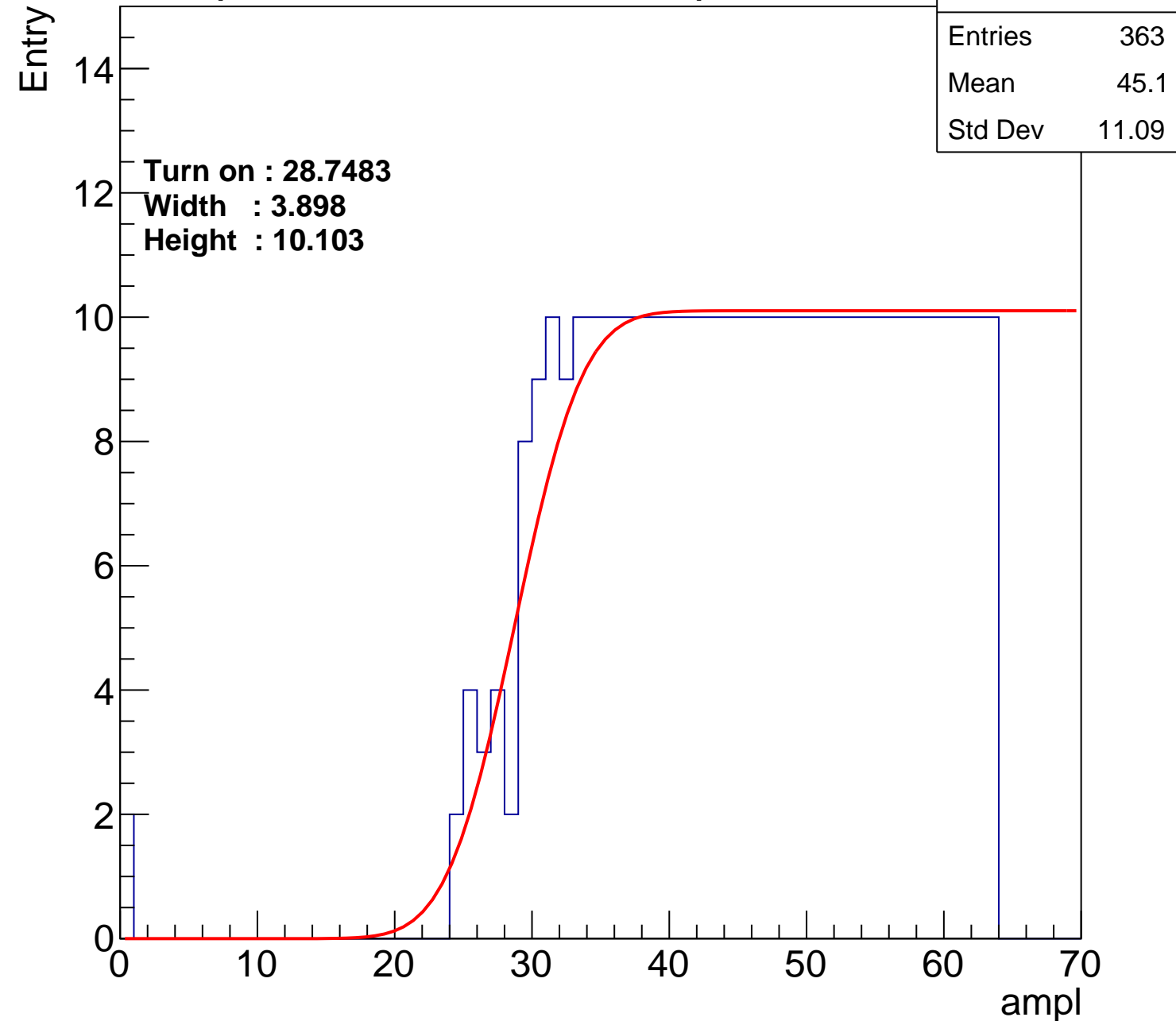
Width : 3.898

Height : 10.103

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch75

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	365
Mean	45.08
Std Dev	10.92

Turn on : 28.0438

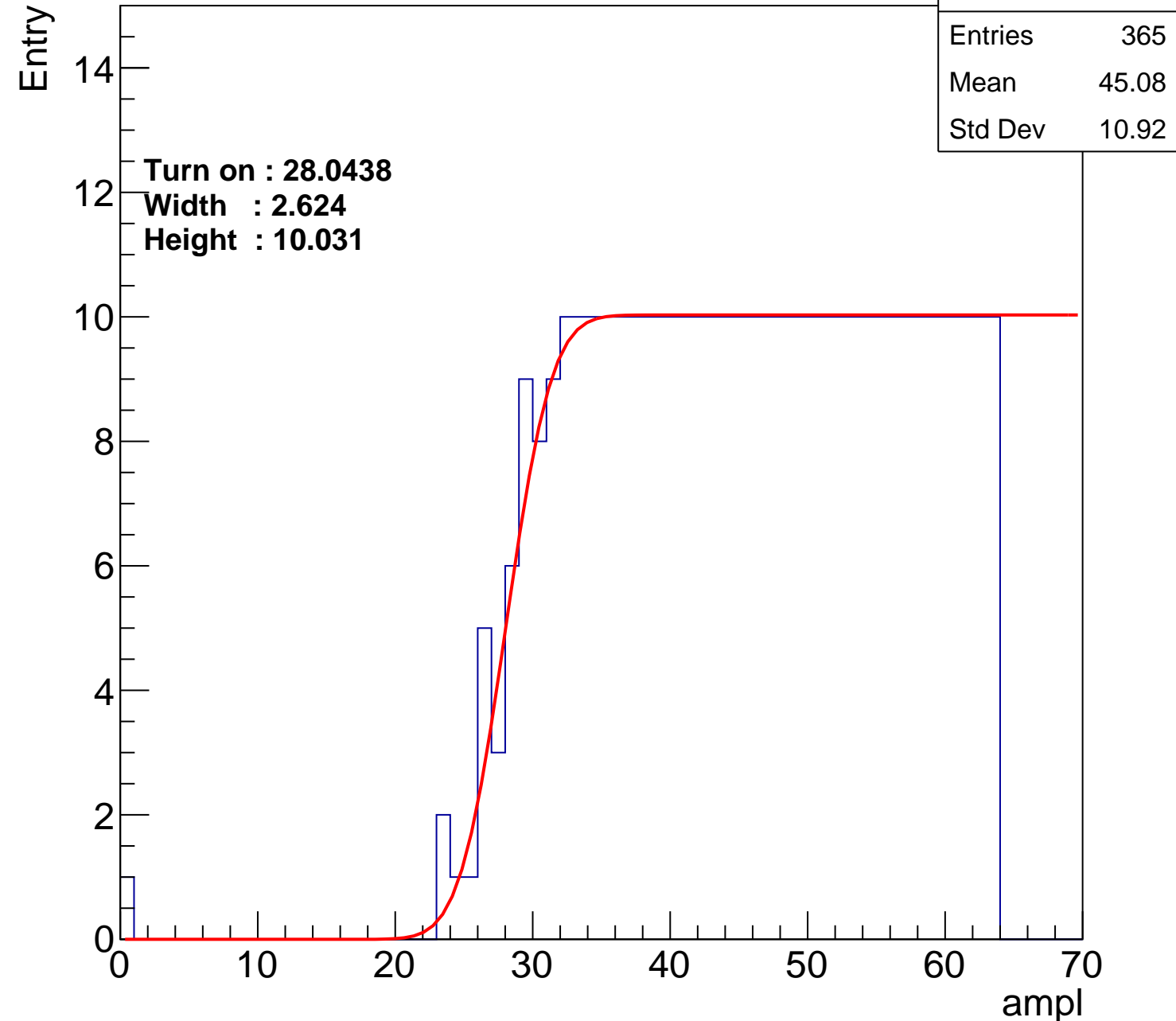
Width : 2.624

Height : 10.031

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch76

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	359
Mean	45.18
Std Dev	11.36

Turn on : 28.9221

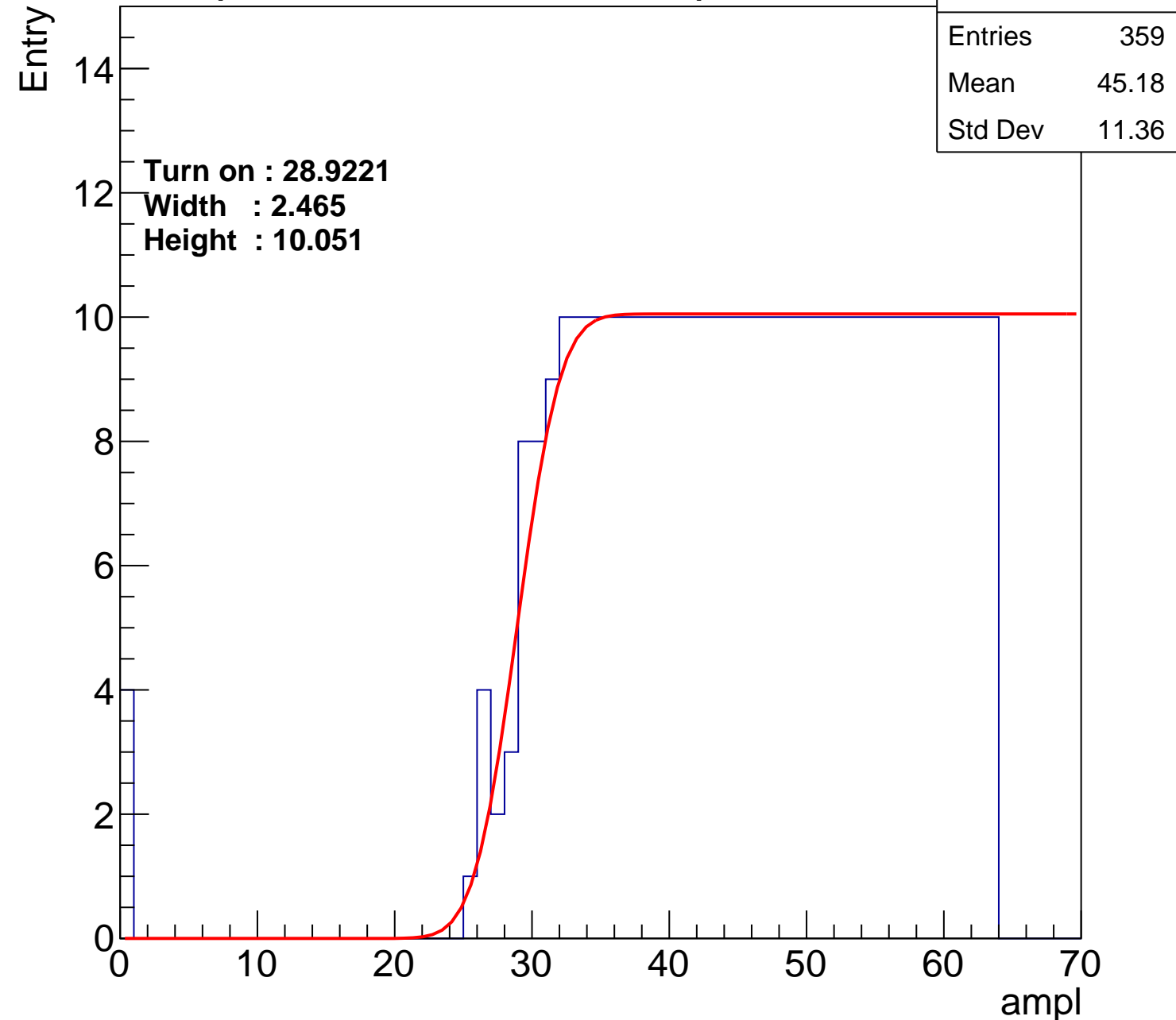
Width : 2.465

Height : 10.051

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch77

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	384
Mean	43.92
Std Dev	11.98

Turn on : 25.9369

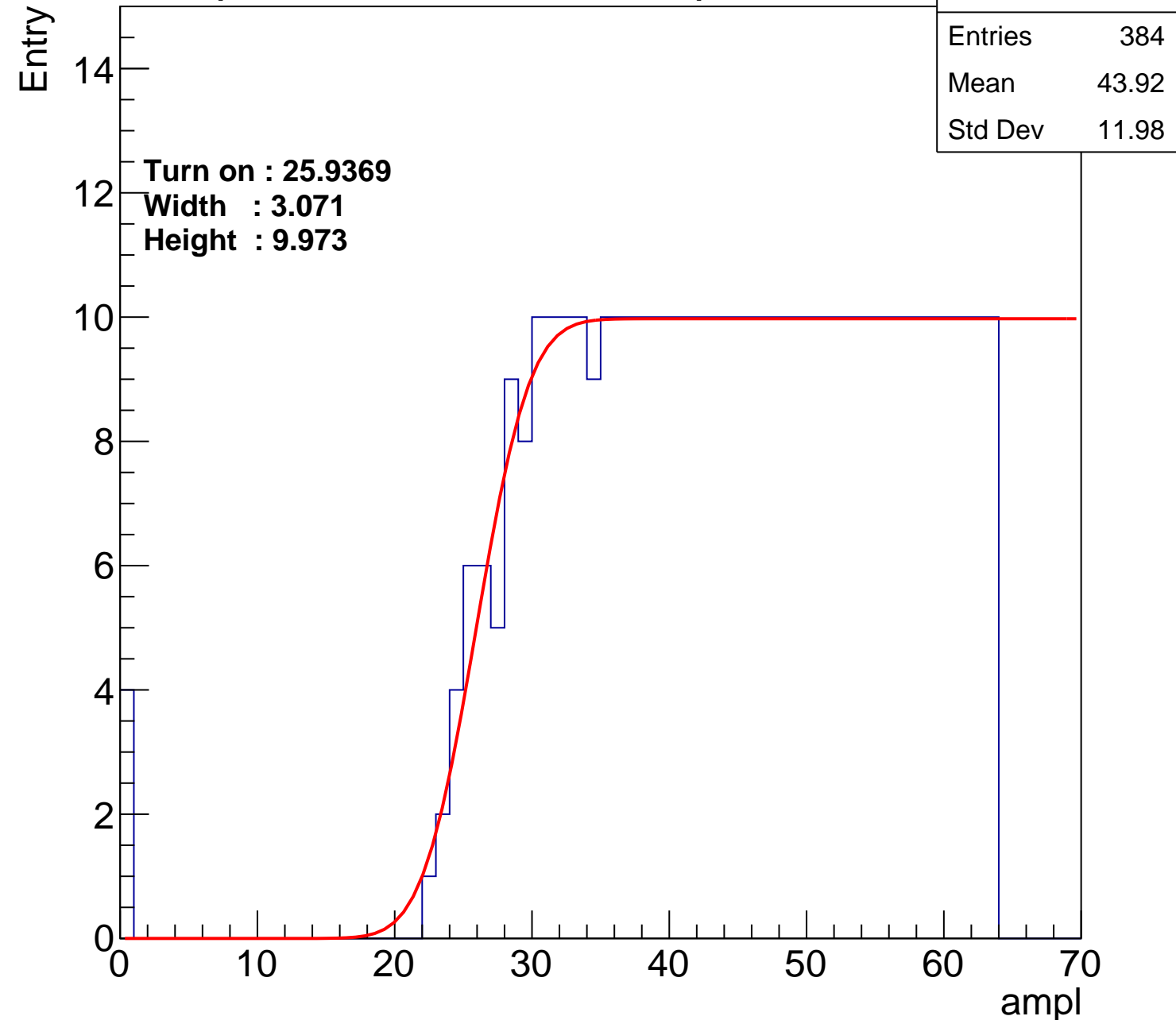
Width : 3.071

Height : 9.973

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch78

calib\_packv5\_042523\_0143.root, FC#4, port A2

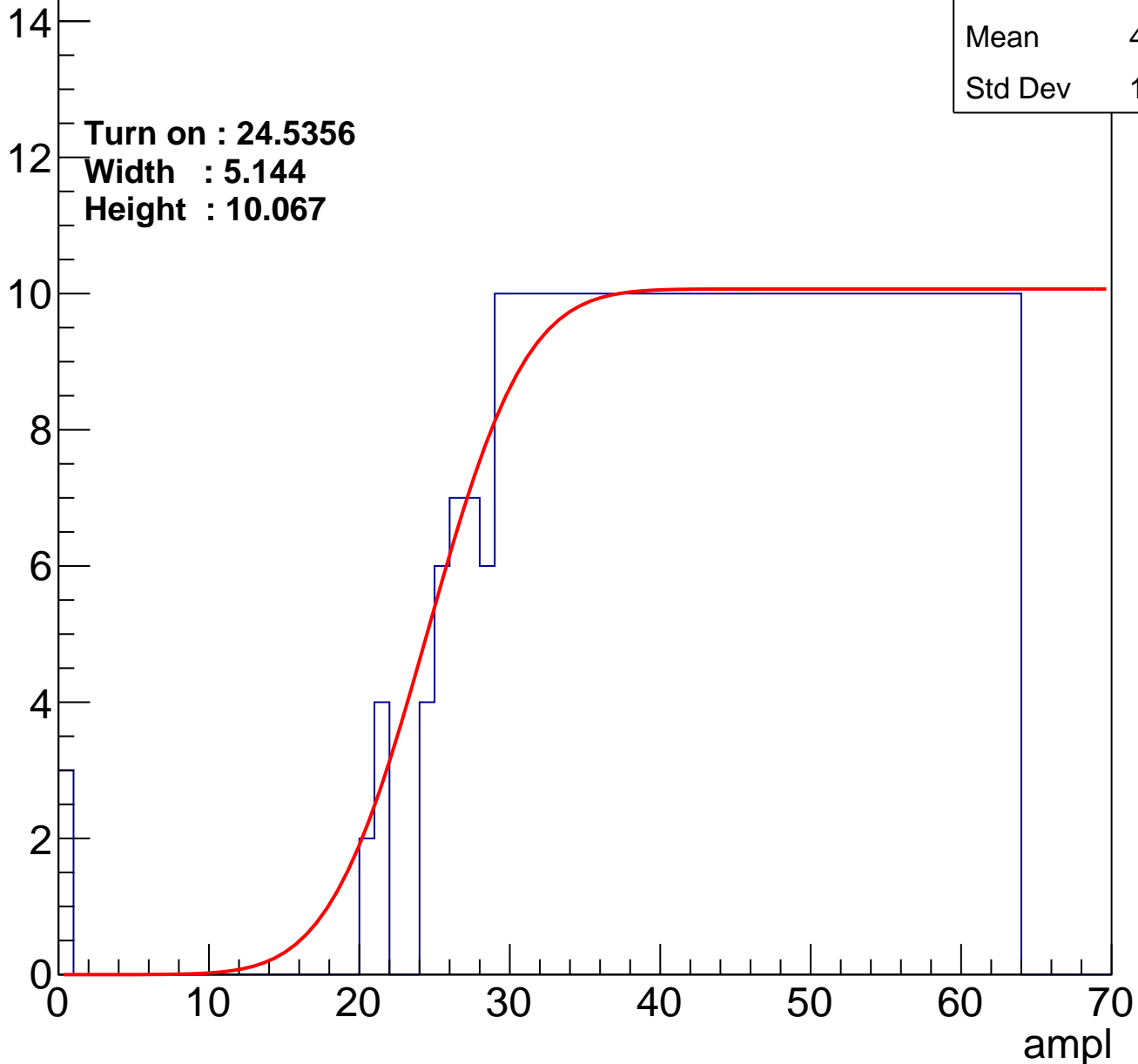
Entries	389
Mean	43.72
Std Dev	11.97

Turn on : 24.5356

Width : 5.144

Height : 10.067

Entry





# B1L100S, U13-ch79

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	359
Mean	45.29
Std Dev	10.99

**Turn on : 28.3087**

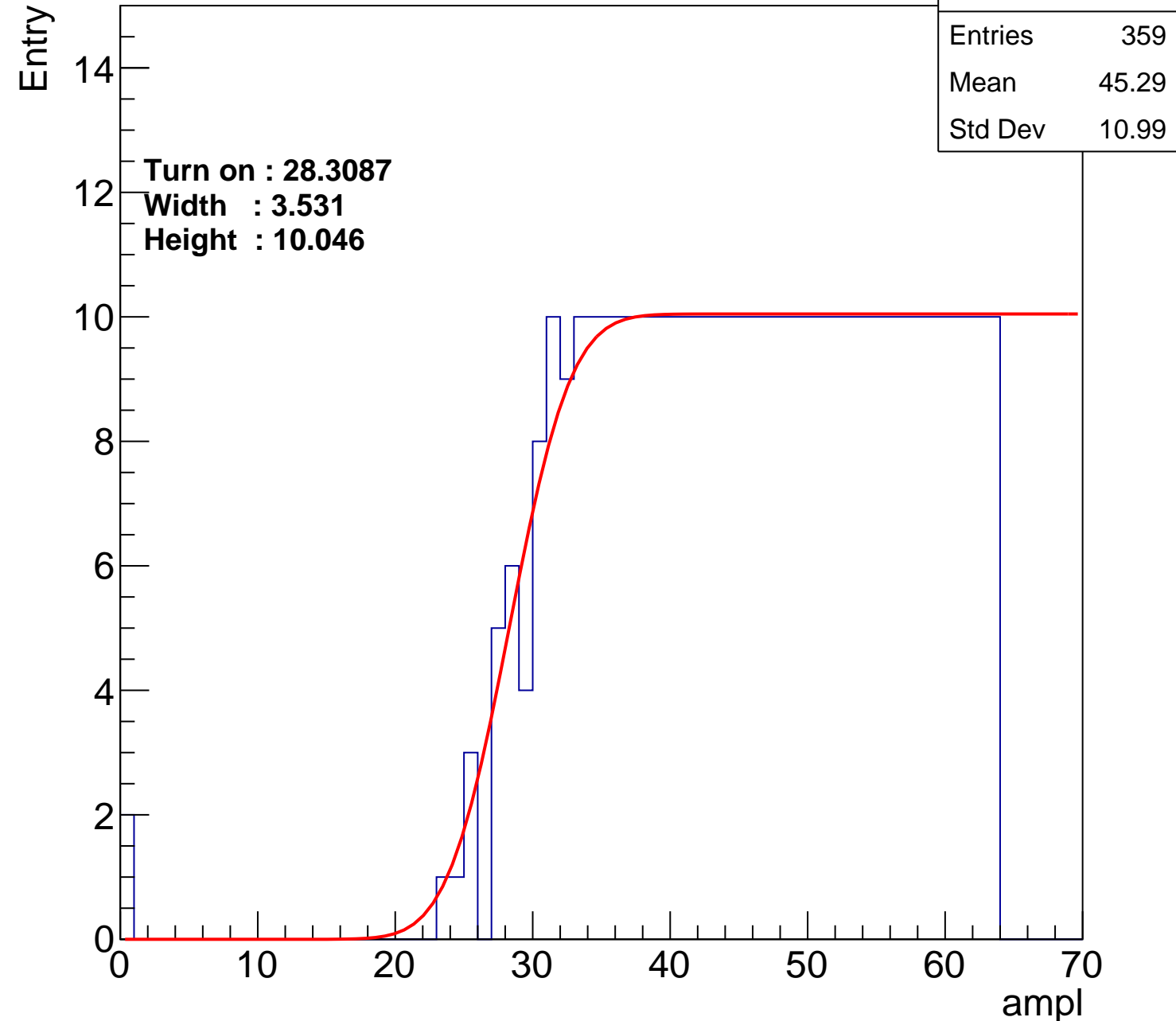
**Width : 3.531**

**Height : 10.046**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch80

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	357
Mean	45.42
Std Dev	10.77

**Turn on : 27.9795**

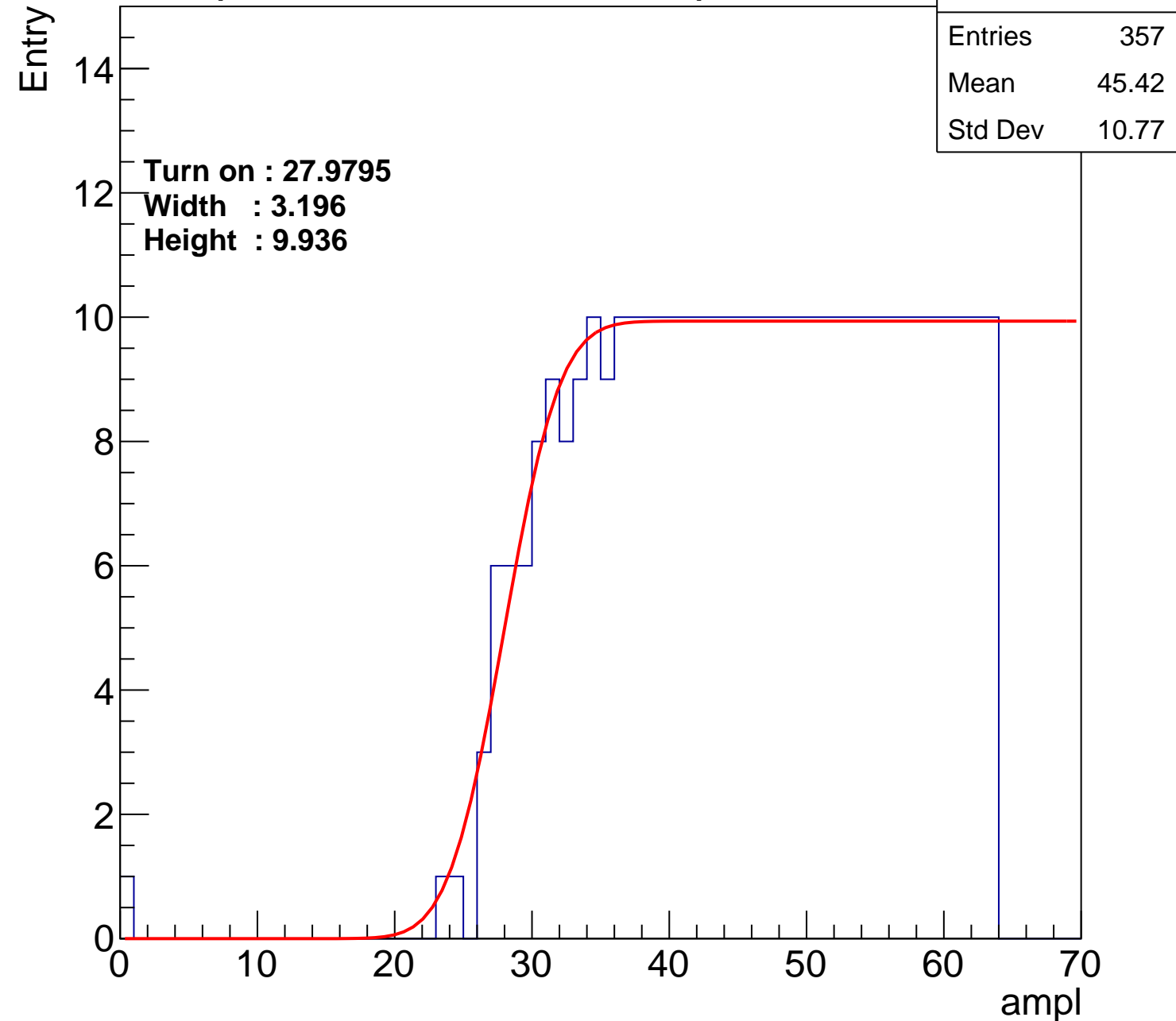
**Width : 3.196**

**Height : 9.936**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch81

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	386
Mean	43.95
Std Dev	11.69

Turn on : 25.8028

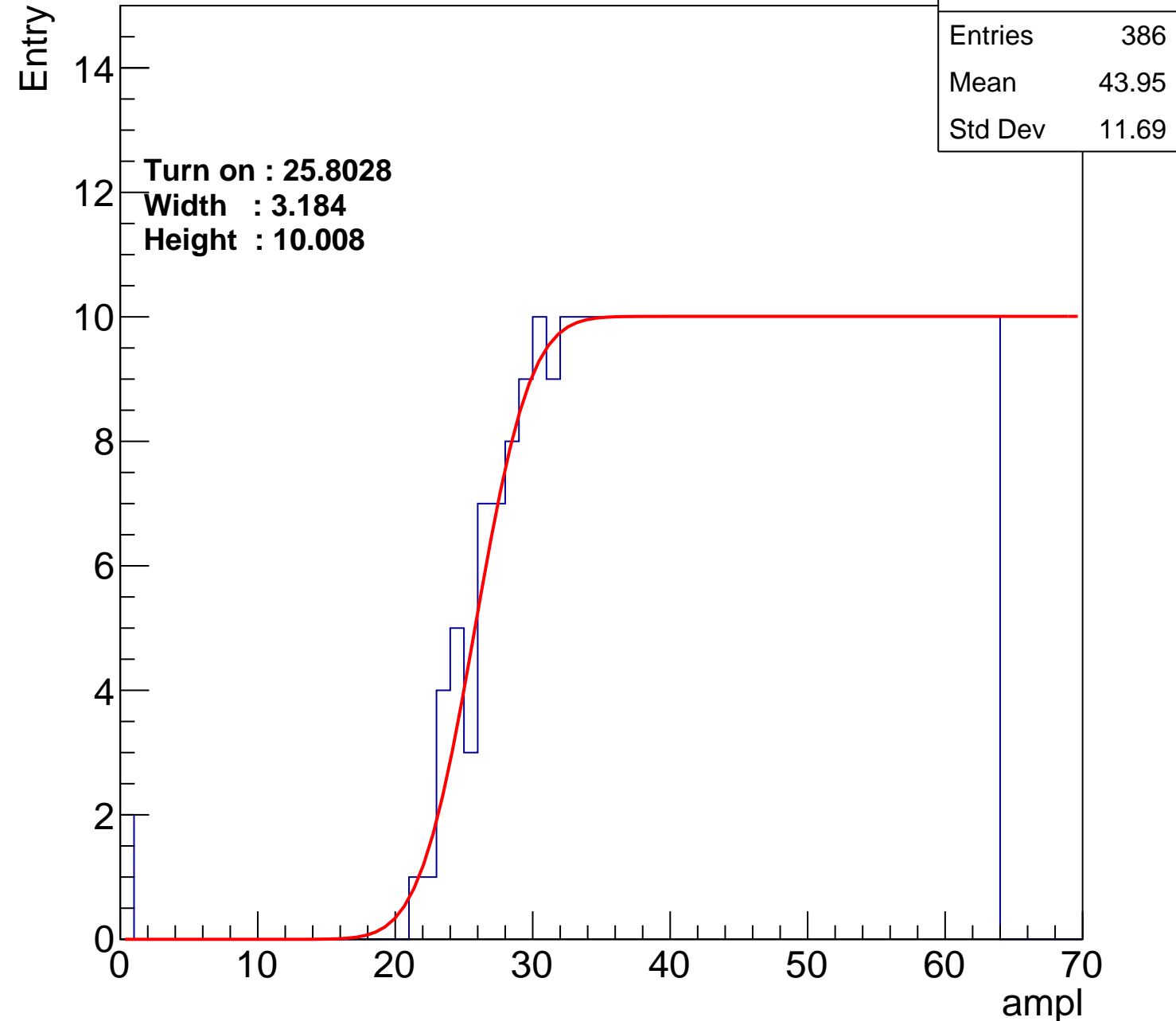
Width : 3.184

Height : 10.008

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch82

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	369
Mean	44.74
Std Dev	11.42

Turn on : 27.2844

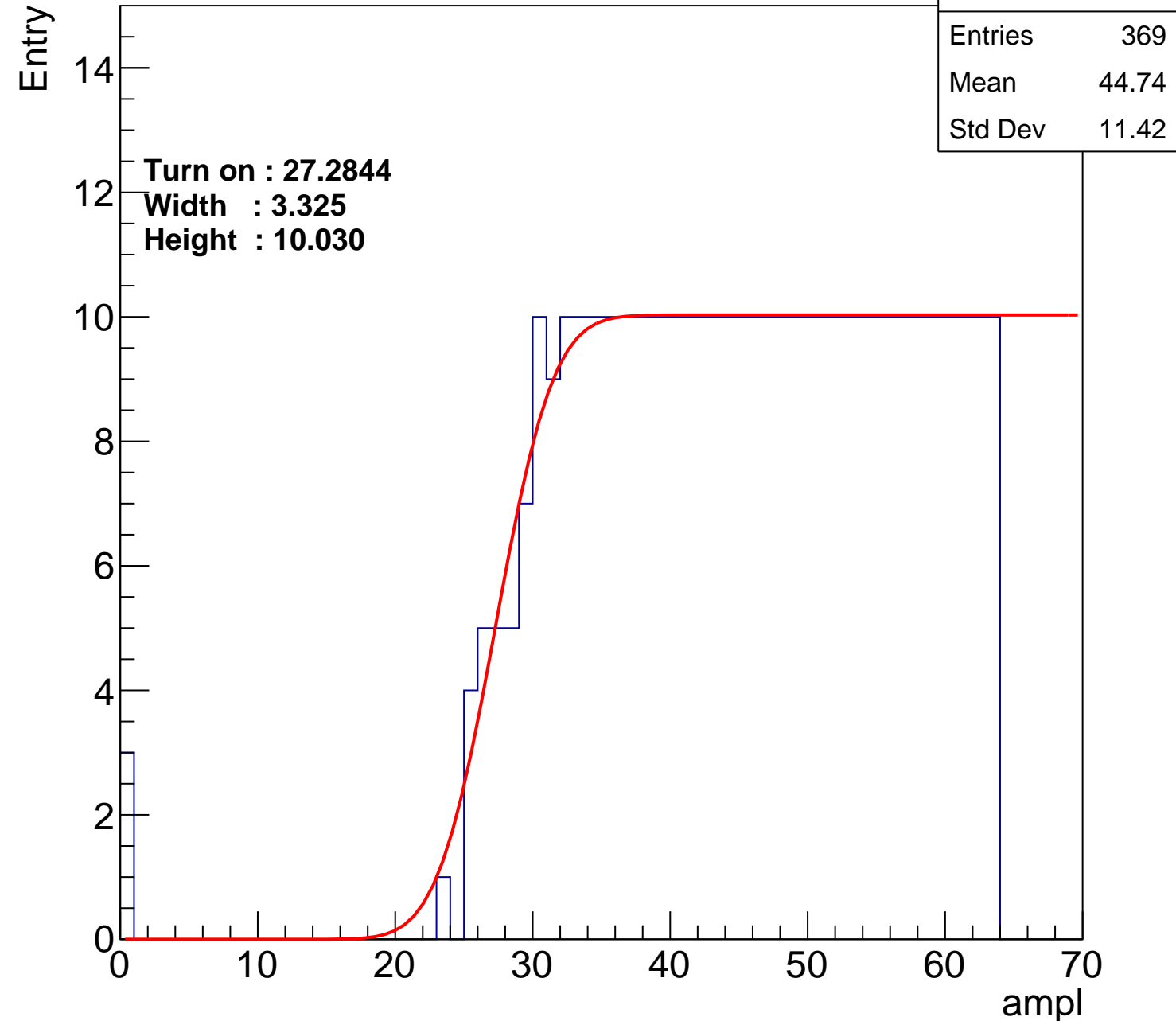
Width : 3.325

Height : 10.030

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch83

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	372
Mean	44.67
Std Dev	11.29

Turn on : 27.0339

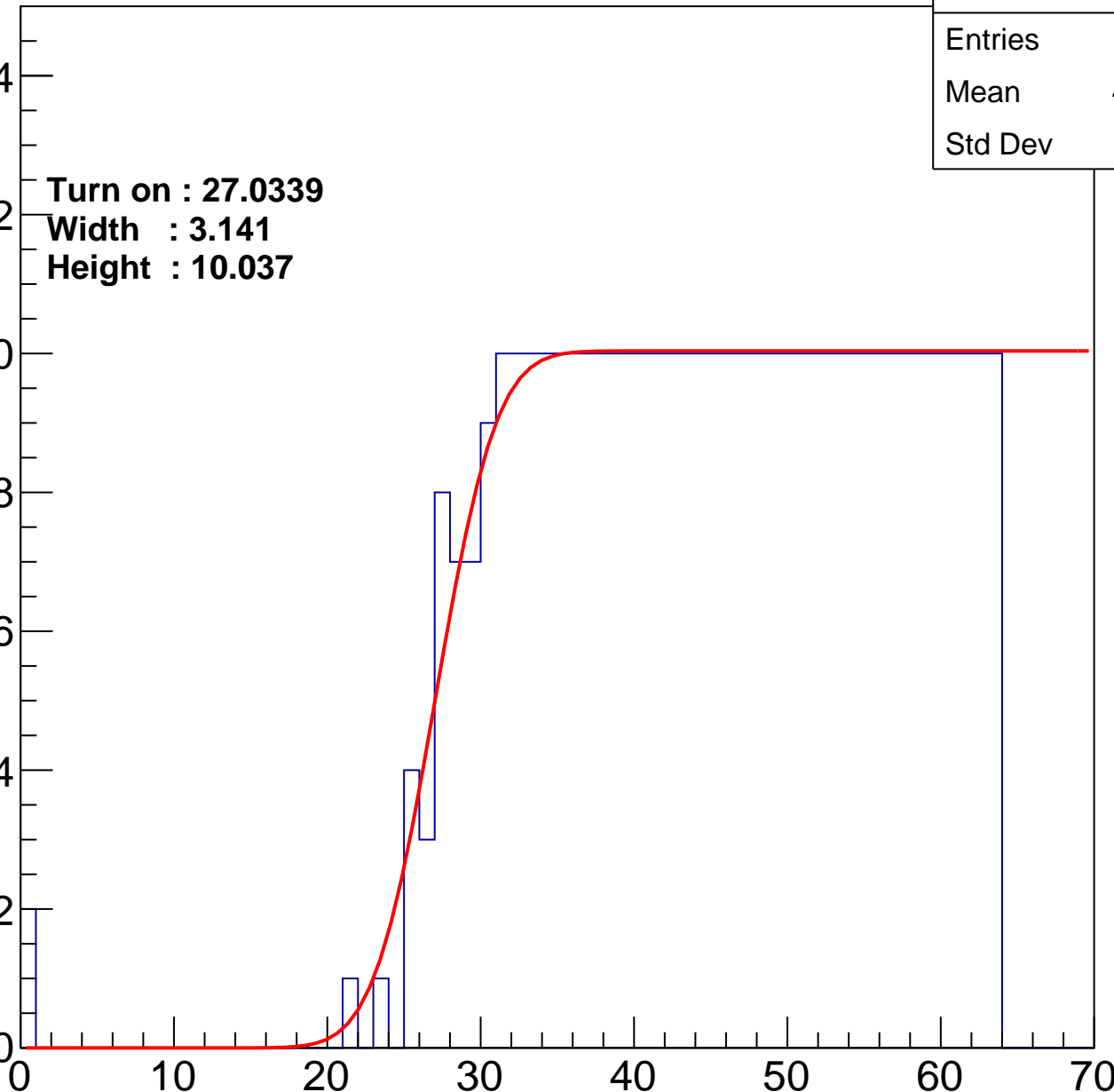
Width : 3.141

Height : 10.037

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch84

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	385
Mean	43.83
Std Dev	12.07

Turn on : 26.0291

Width : 4.318

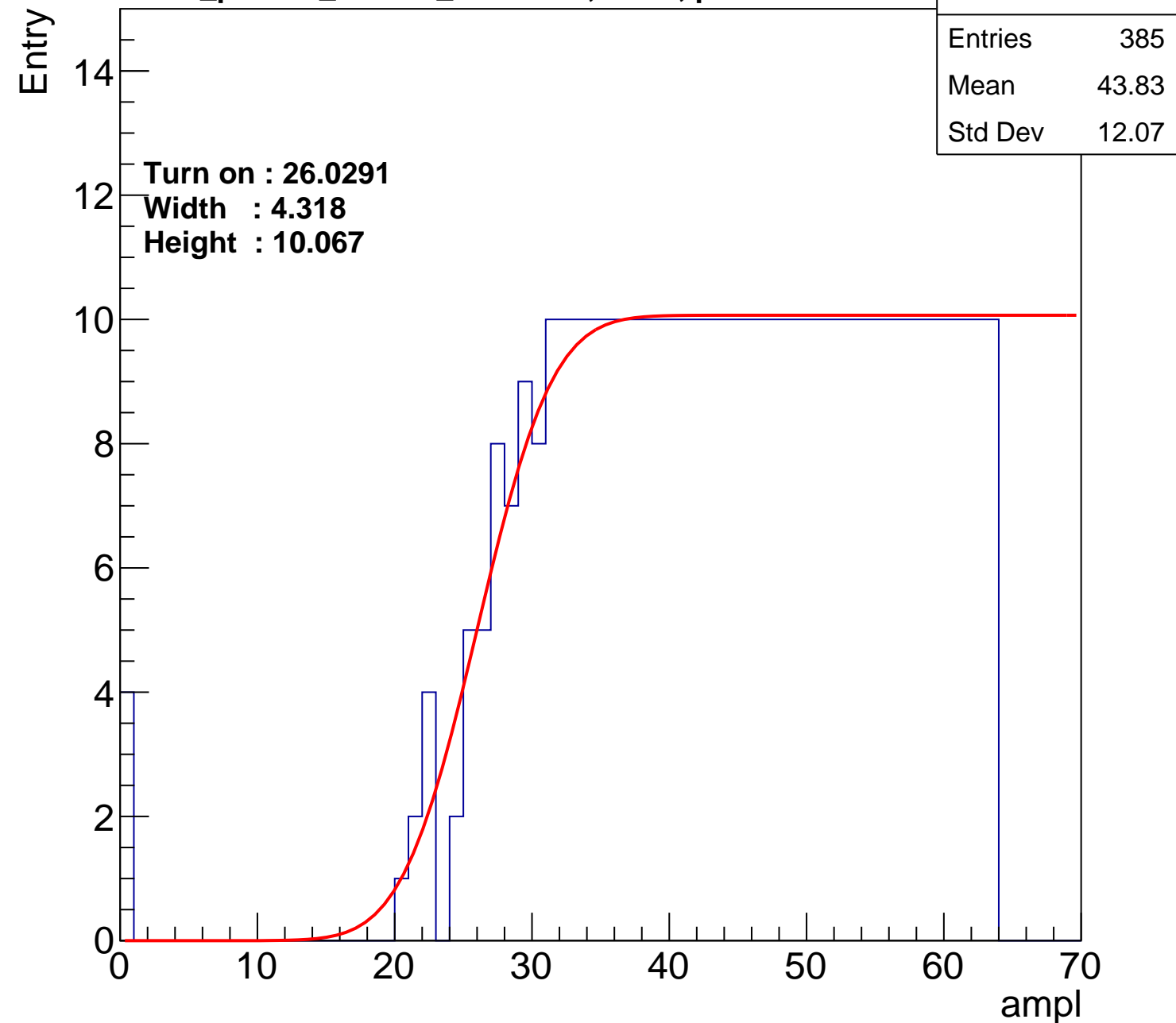
Height : 10.067

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L100S, U13-ch85

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	391
Mean	43.61
Std Dev	12.05

Turn on : 25.6555

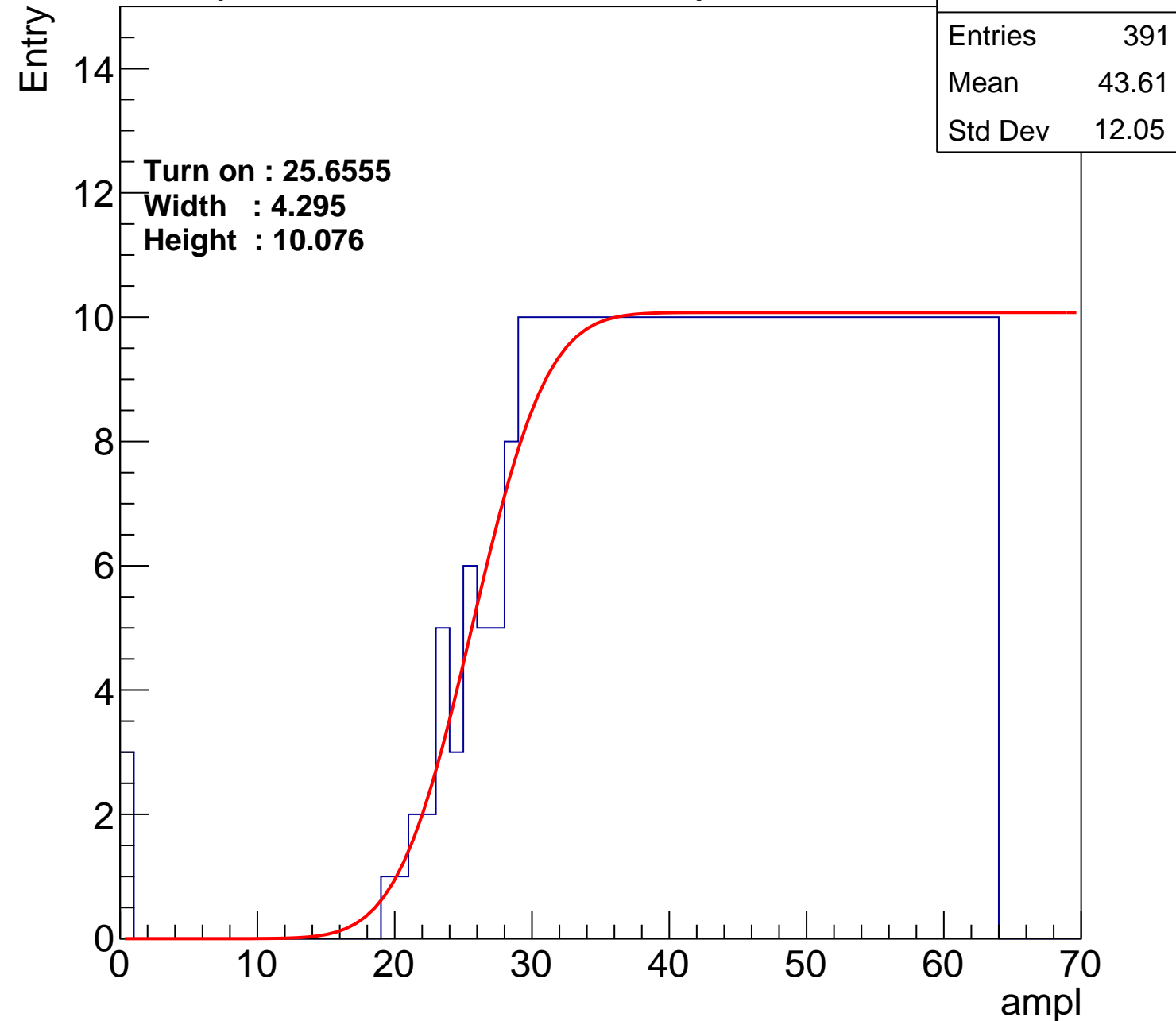
Width : 4.295

Height : 10.076

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch86

calib\_packv5\_042523\_0143.root, FC#4, port A2

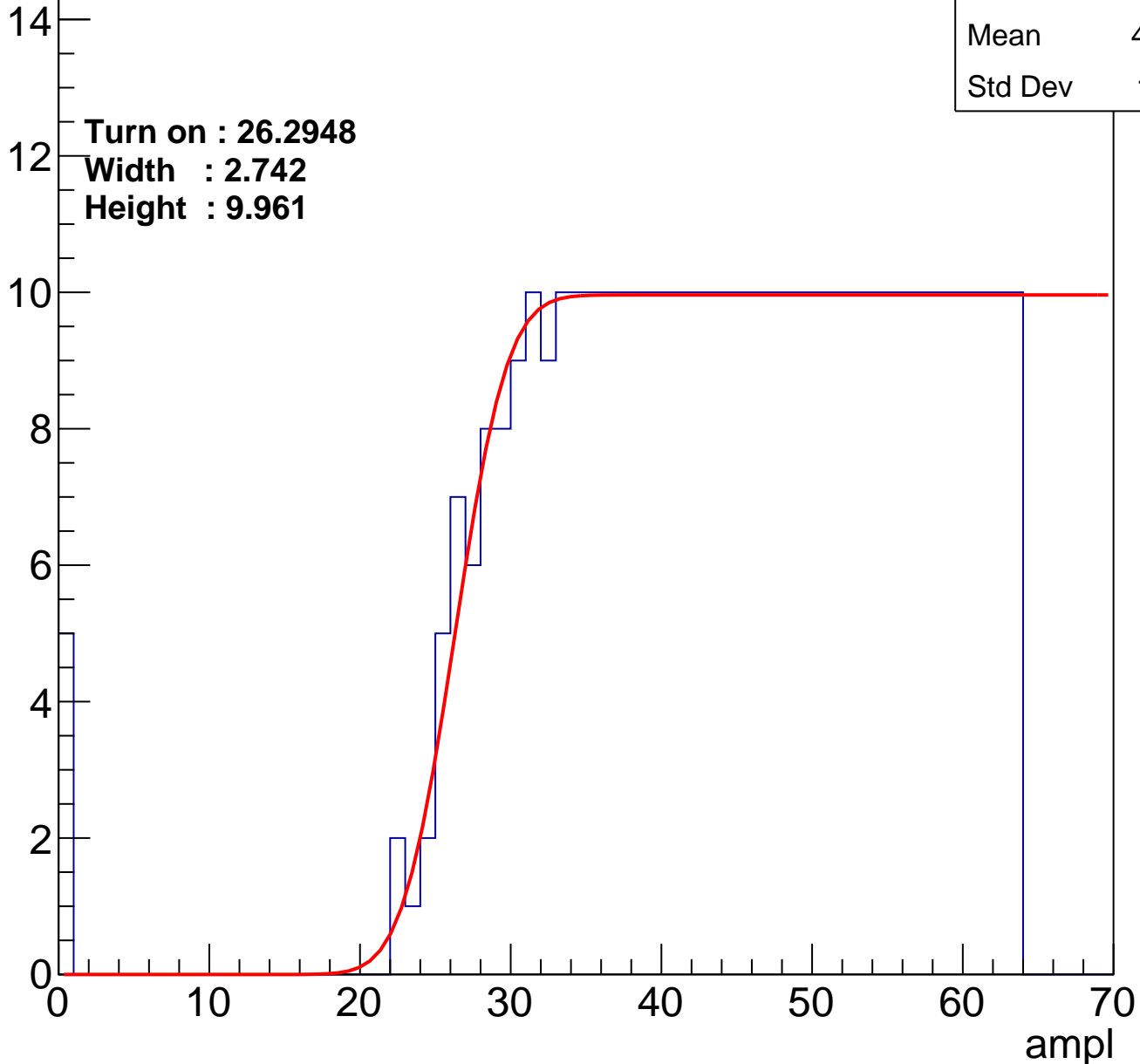
Entries	382
Mean	43.95
Std Dev	12.11

Turn on : 26.2948

Width : 2.742

Height : 9.961

Entry





# B1L100S, U13-ch87

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	386
Mean	43.66
Std Dev	12.49

Turn on : 26.3651

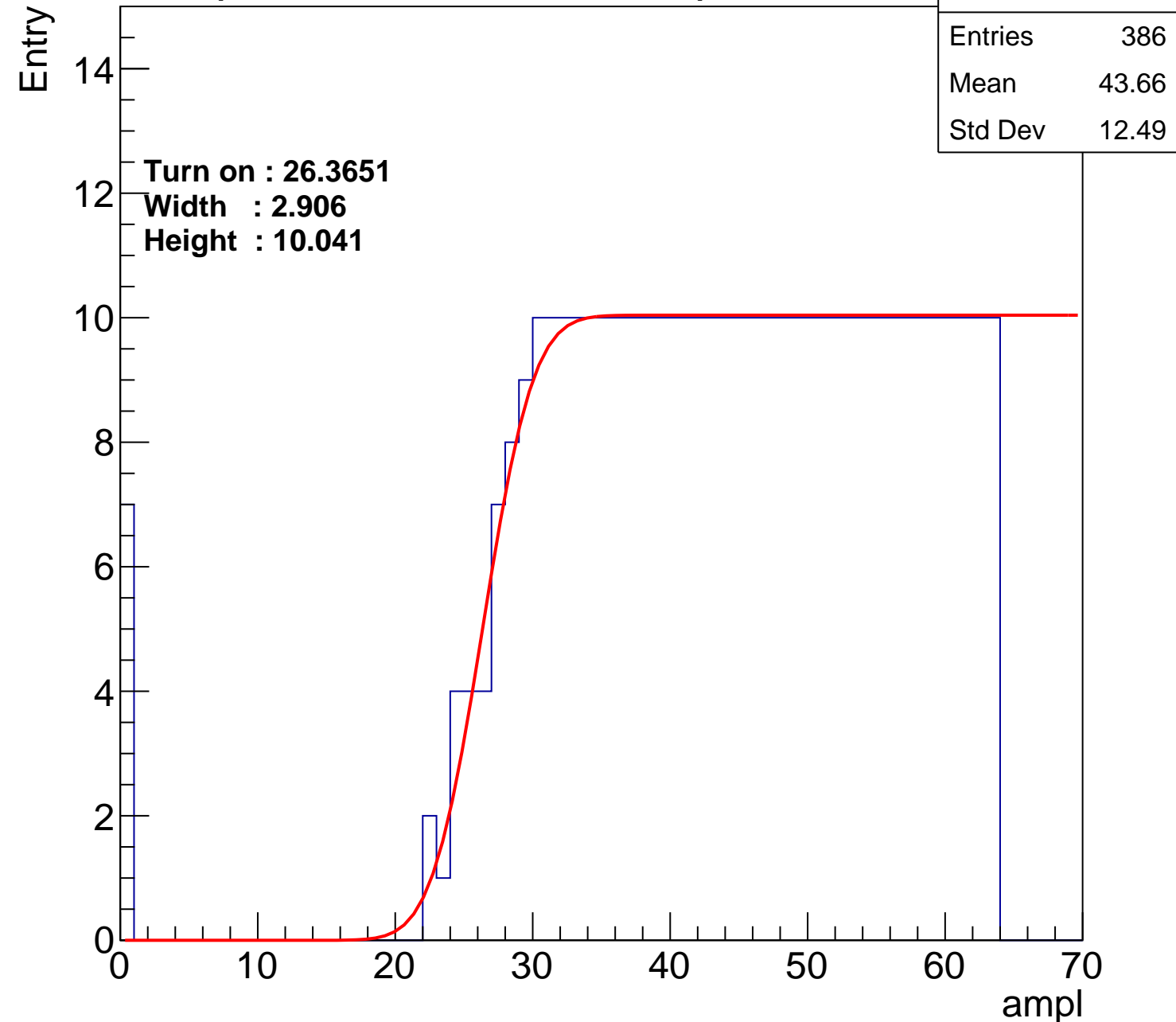
Width : 2.906

Height : 10.041

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch88

calib\_packv5\_042523\_0143.root, FC#4, port A2

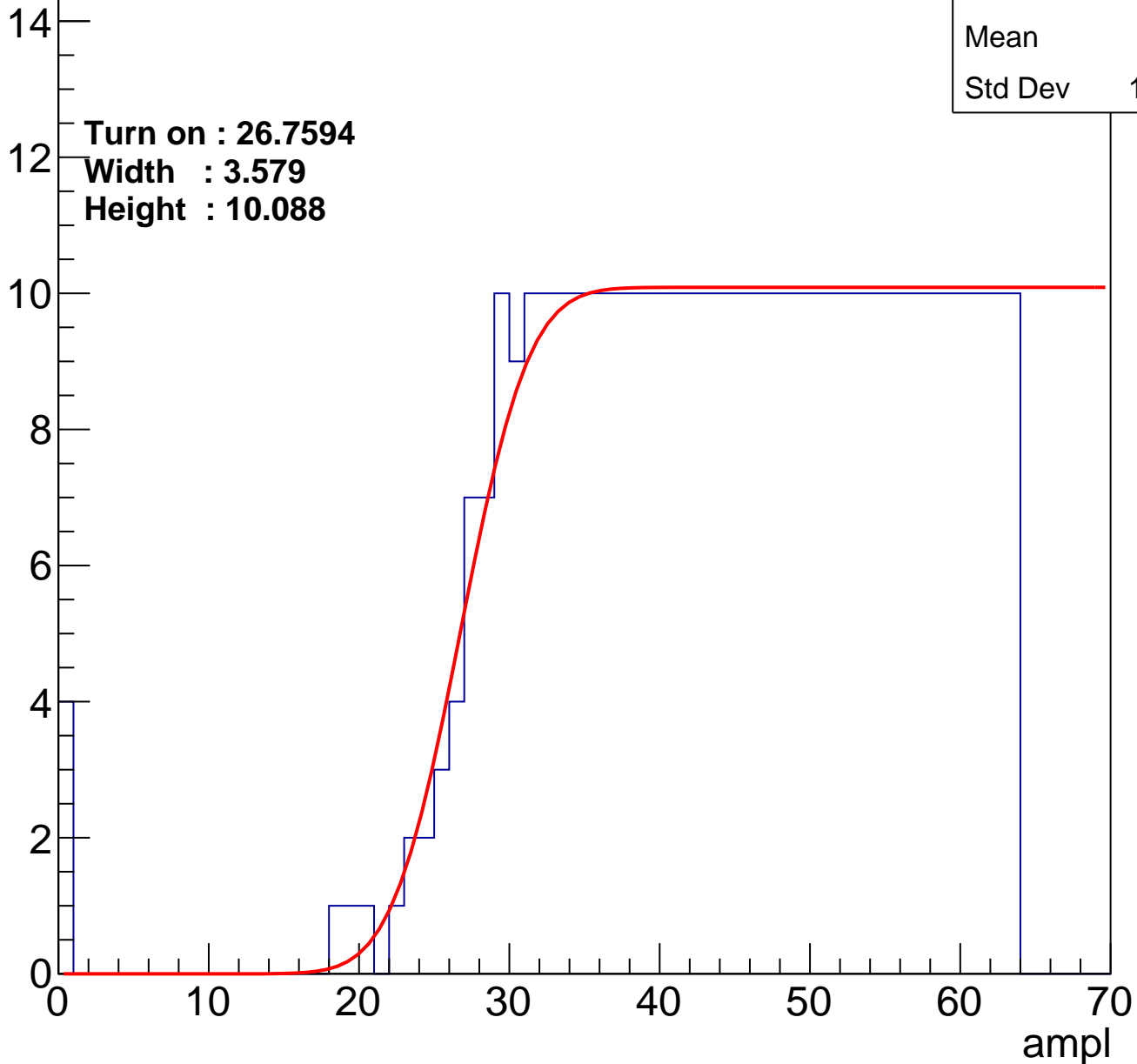
Entries	382
Mean	44
Std Dev	11.99

Turn on : 26.7594

Width : 3.579

Height : 10.088

Entry



# B1L100S, U13-ch89

calib\_packv5\_042523\_0143.root, FC#4, port A2

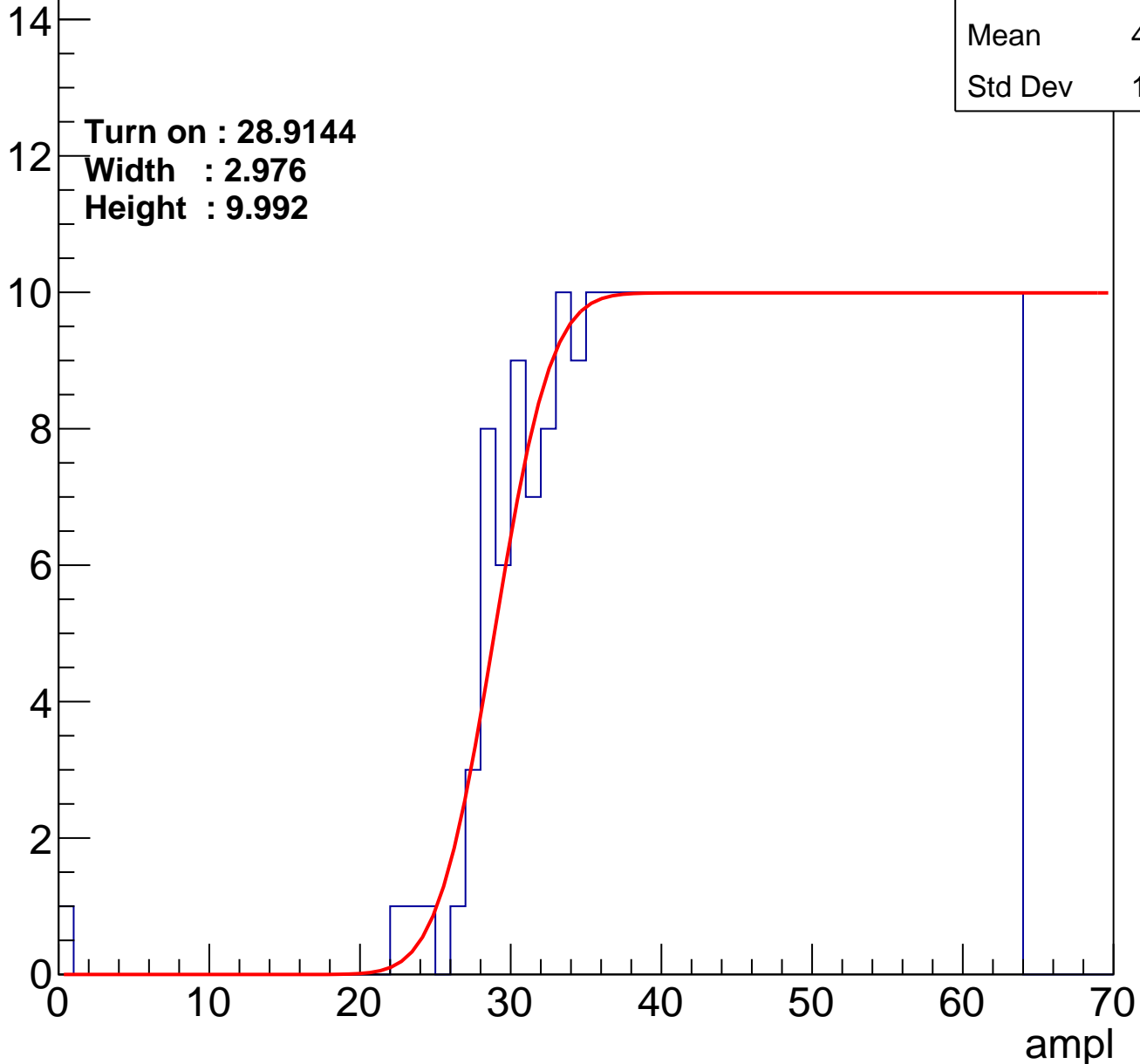
Entries	355
Mean	45.53
Std Dev	10.72

**Turn on : 28.9144**

**Width : 2.976**

**Height : 9.992**

Entry



# B1L100S, U13-ch90

calib\_packv5\_042523\_0143.root, FC#4, port A2

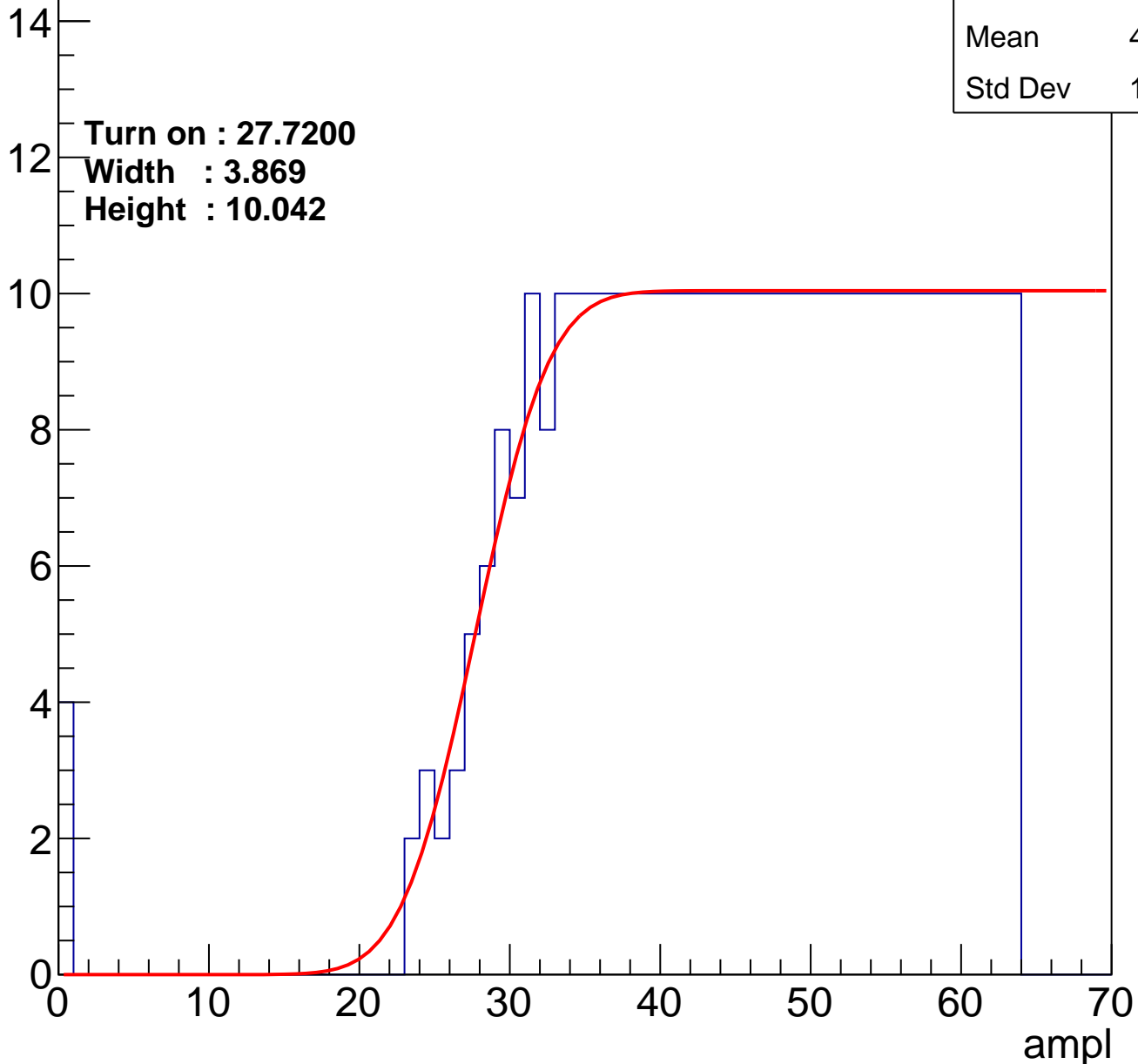
Entries	368
Mean	44.67
Std Dev	11.67

Turn on : 27.7200

Width : 3.869

Height : 10.042

Entry



# B1L100S, U13-ch91

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	366
Mean	45
Std Dev	11

Turn on : 27.6207

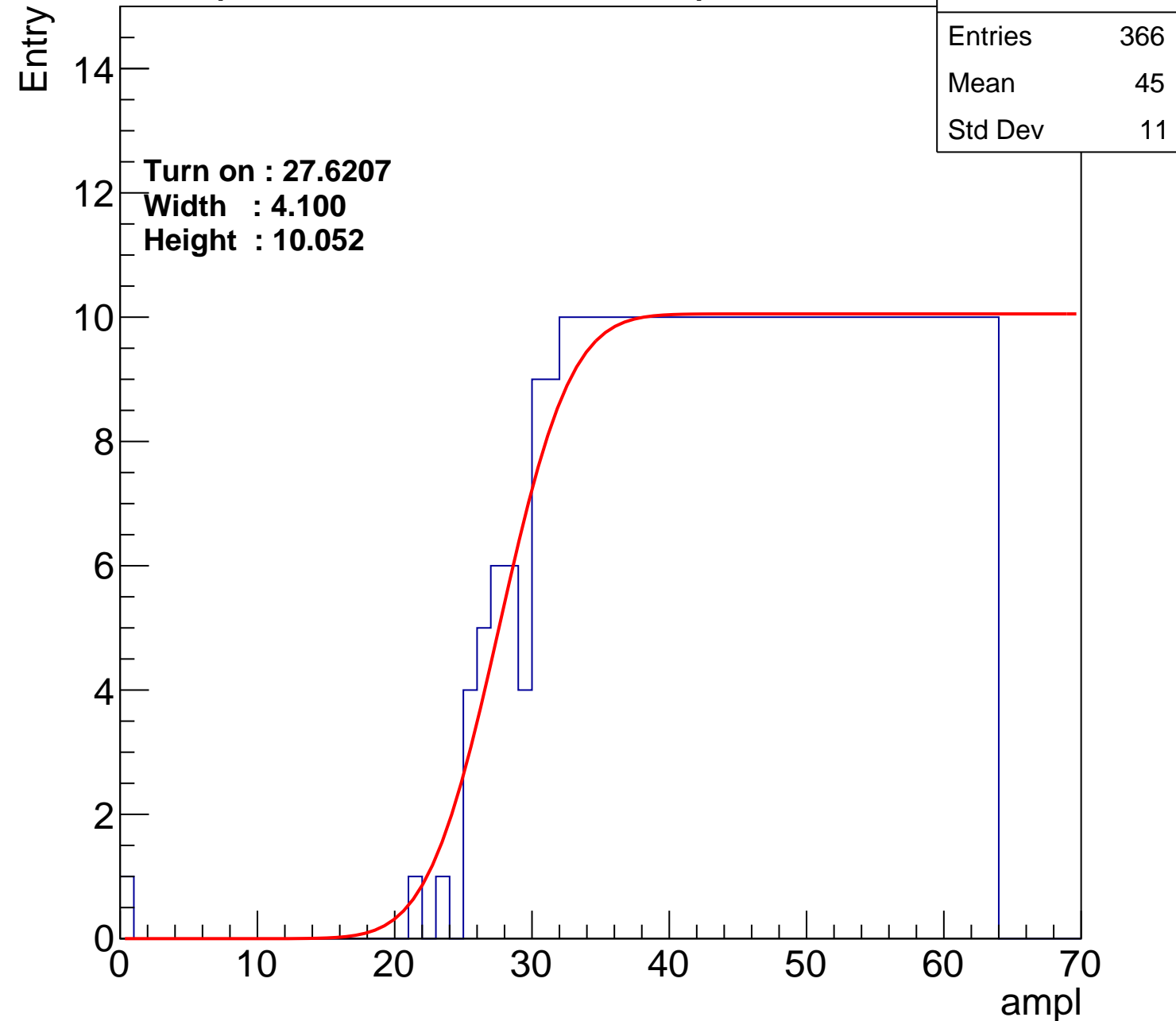
Width : 4.100

Height : 10.052

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch92

calib\_packv5\_042523\_0143.root, FC#4, port A2

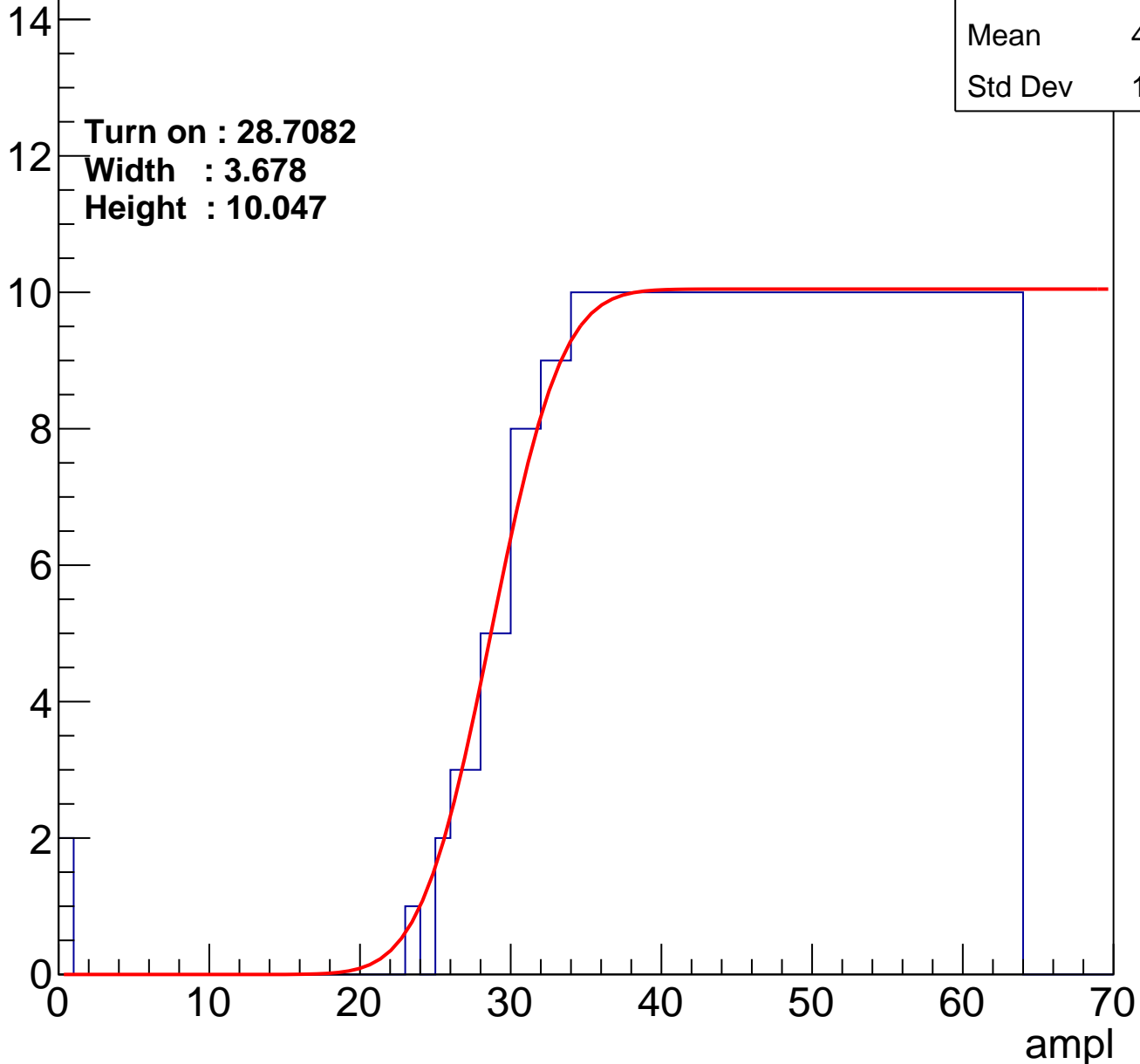
Entries	355
Mean	45.46
Std Dev	10.93

**Turn on : 28.7082**

**Width : 3.678**

**Height : 10.047**

Entry



# B1L100S, U13-ch93

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	371
Mean	44.79
Std Dev	11.06

Turn on : 27.0278

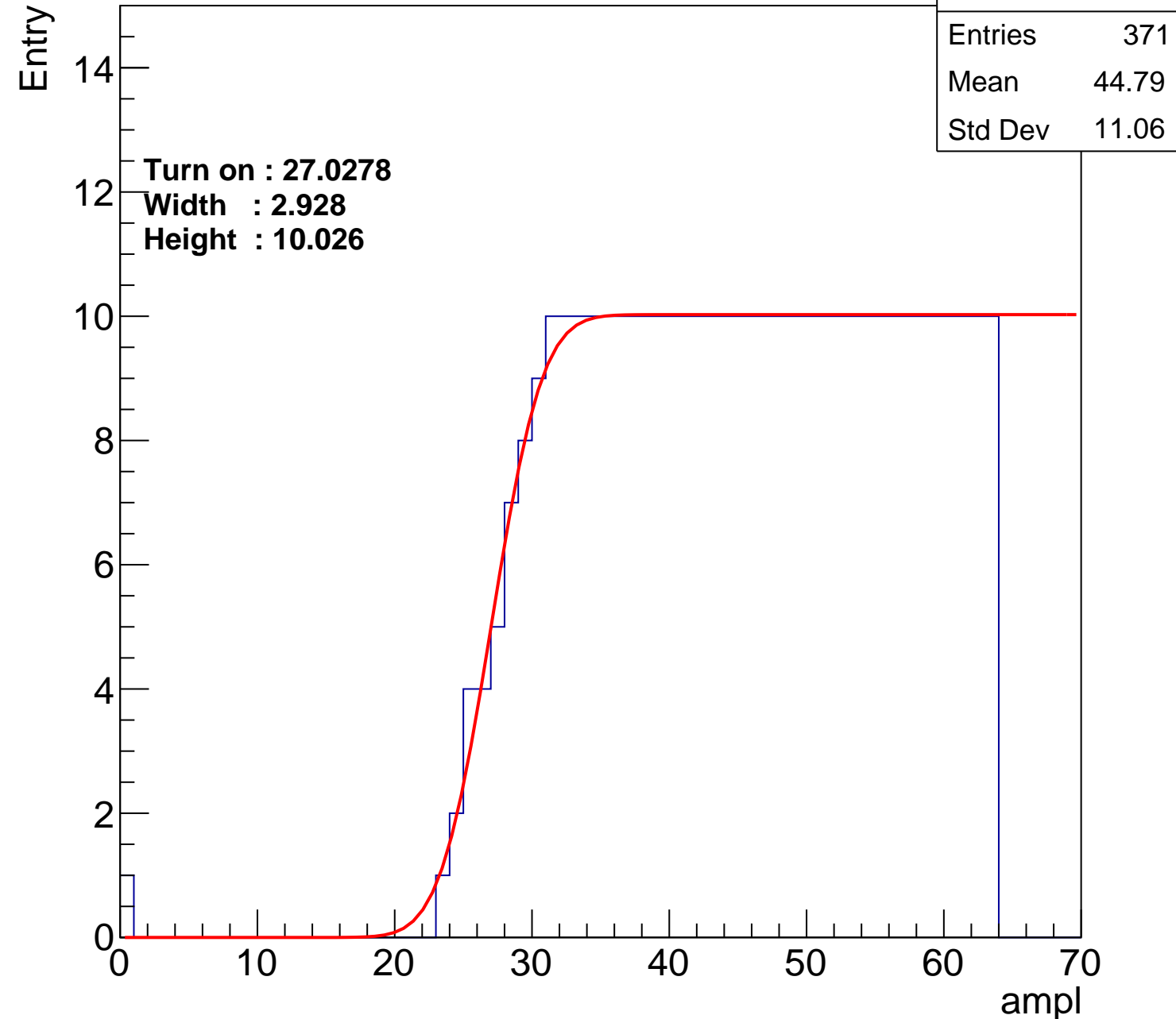
Width : 2.928

Height : 10.026

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch94

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	370
Mean	44.64
Std Dev	11.53

Turn on : 27.3567

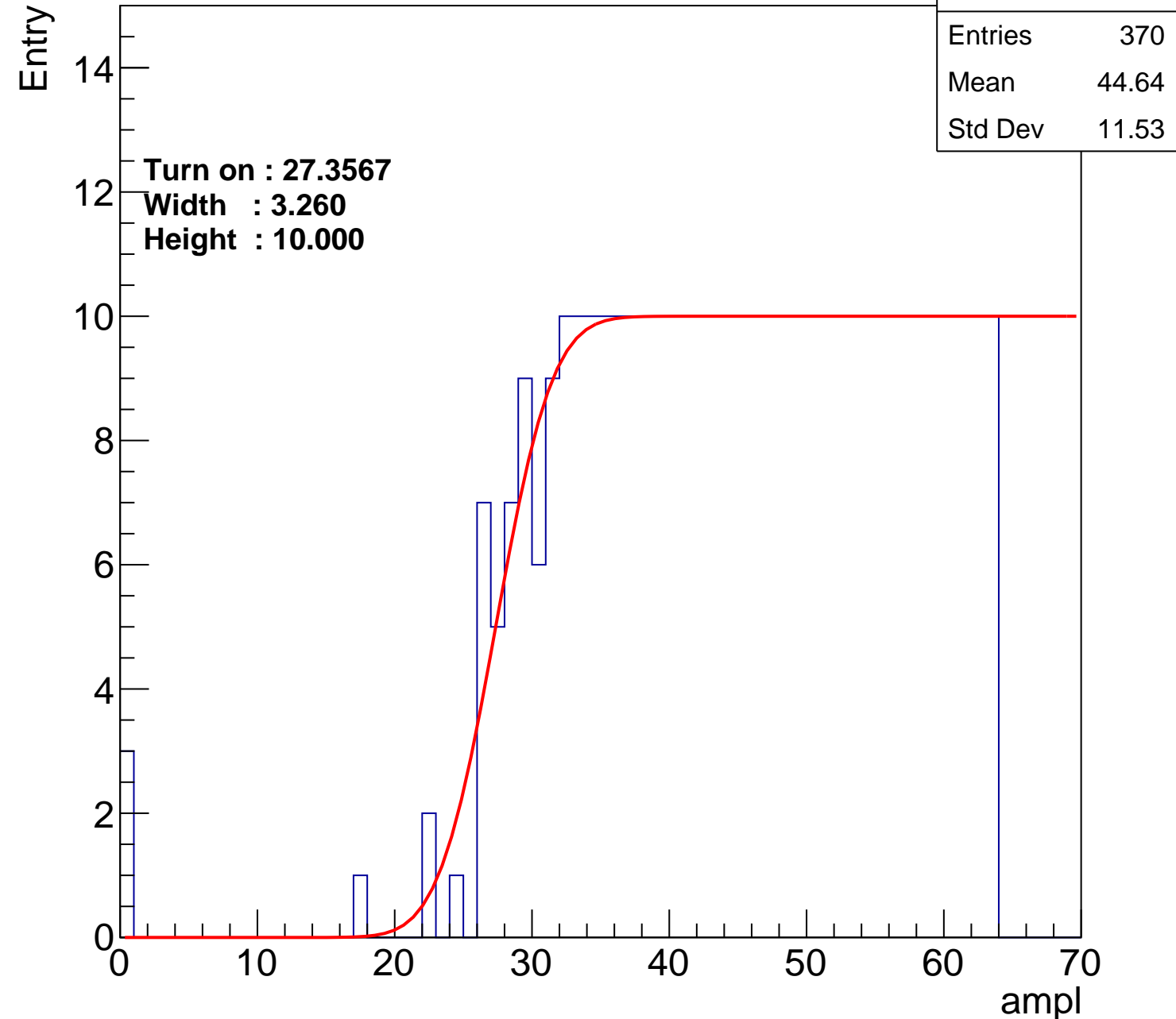
Width : 3.260

Height : 10.000

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U13-ch95

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	351
Mean	45.74
Std Dev	10.6

**Turn on : 29.2329**

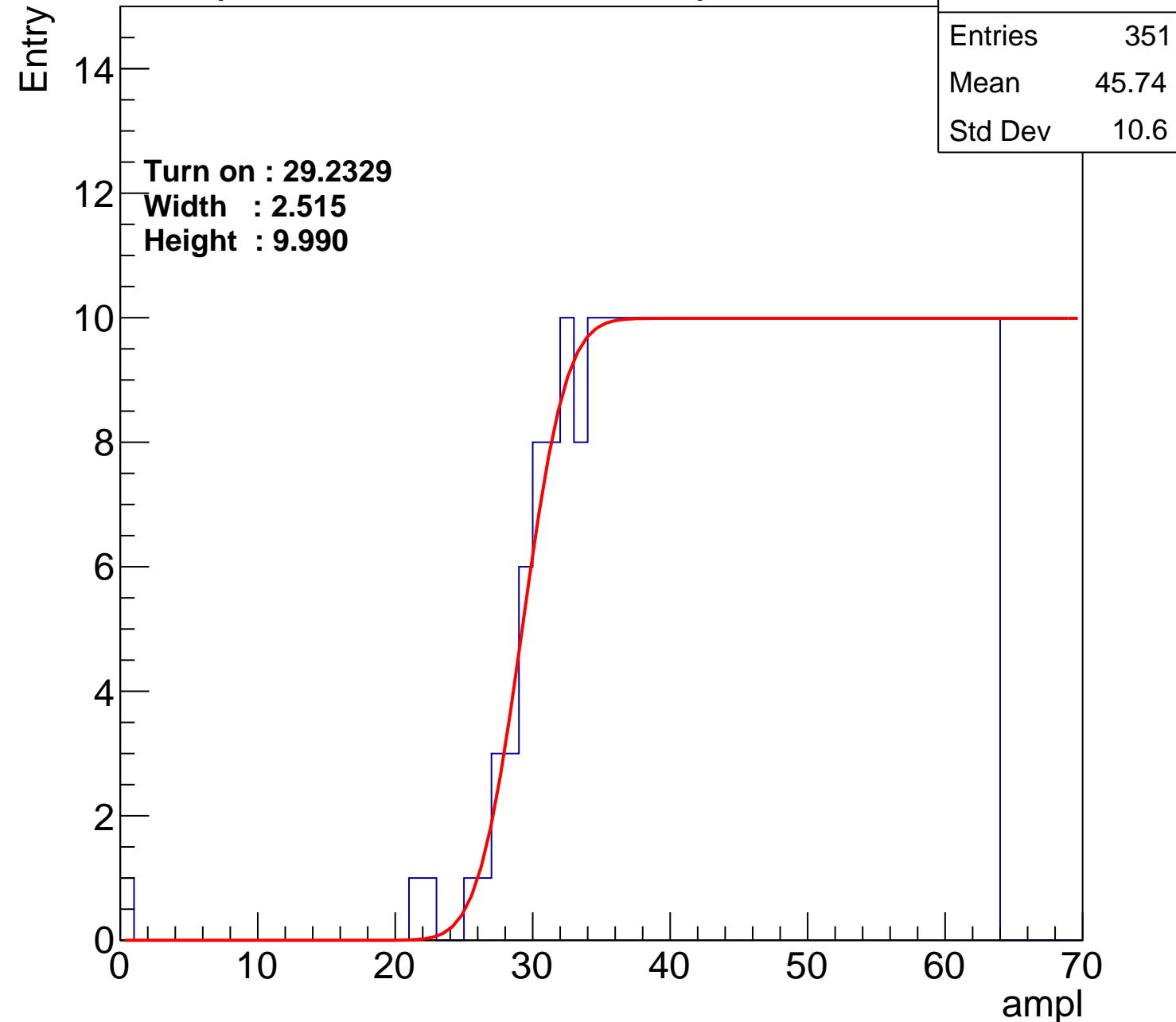
**Width : 2.515**

**Height : 9.990**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch96

calib\_packv5\_042523\_0143.root, FC#4, port A2

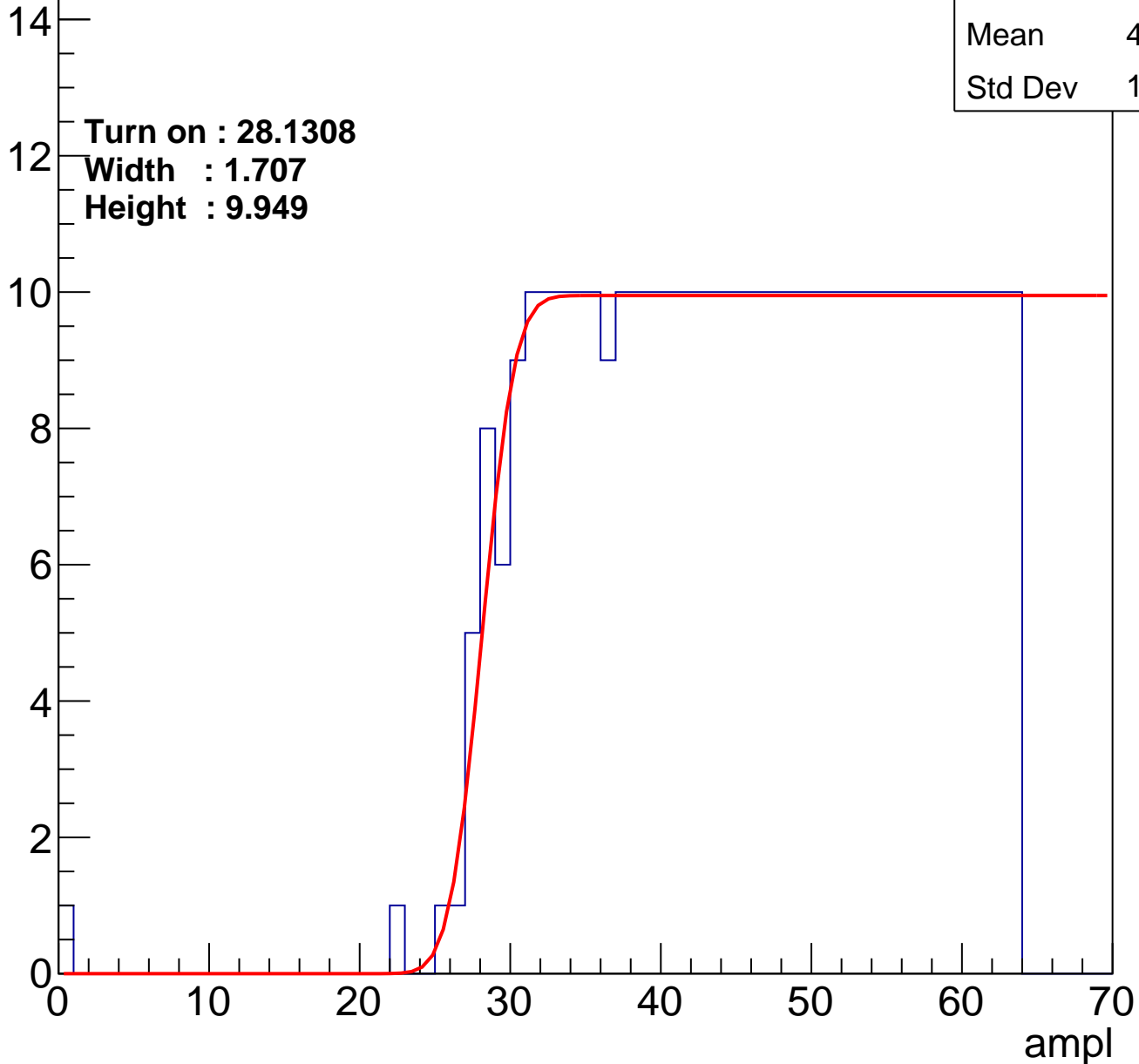
Entries	361
Mean	45.29
Std Dev	10.78

**Turn on : 28.1308**

**Width : 1.707**

**Height : 9.949**

Entry



# B1L100S, U13-ch97

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	381
Mean	43.98
Std Dev	12.1

Turn on : 26.4789

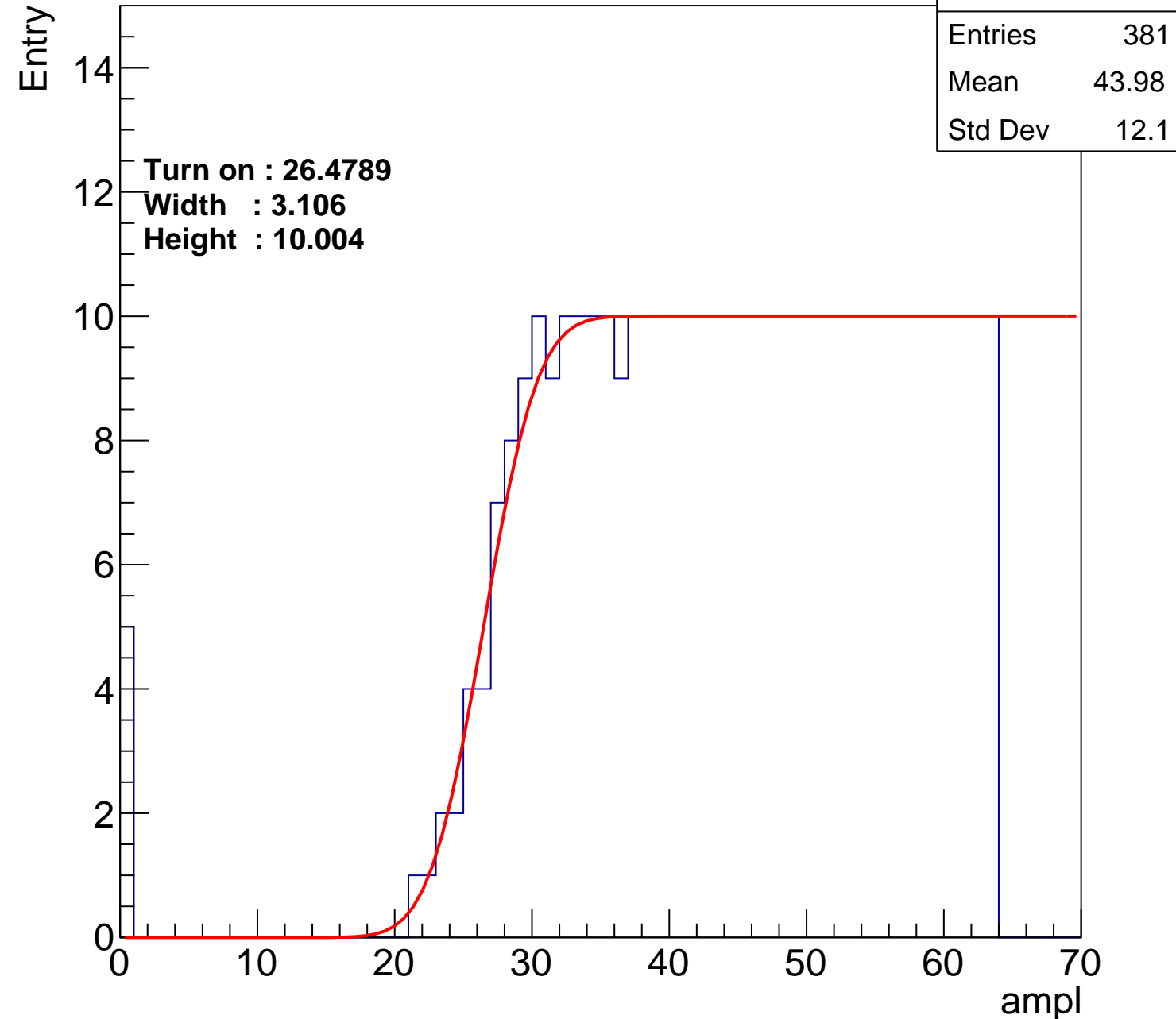
Width : 3.106

Height : 10.004

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch98

calib\_packv5\_042523\_0143.root, FC#4, port A2

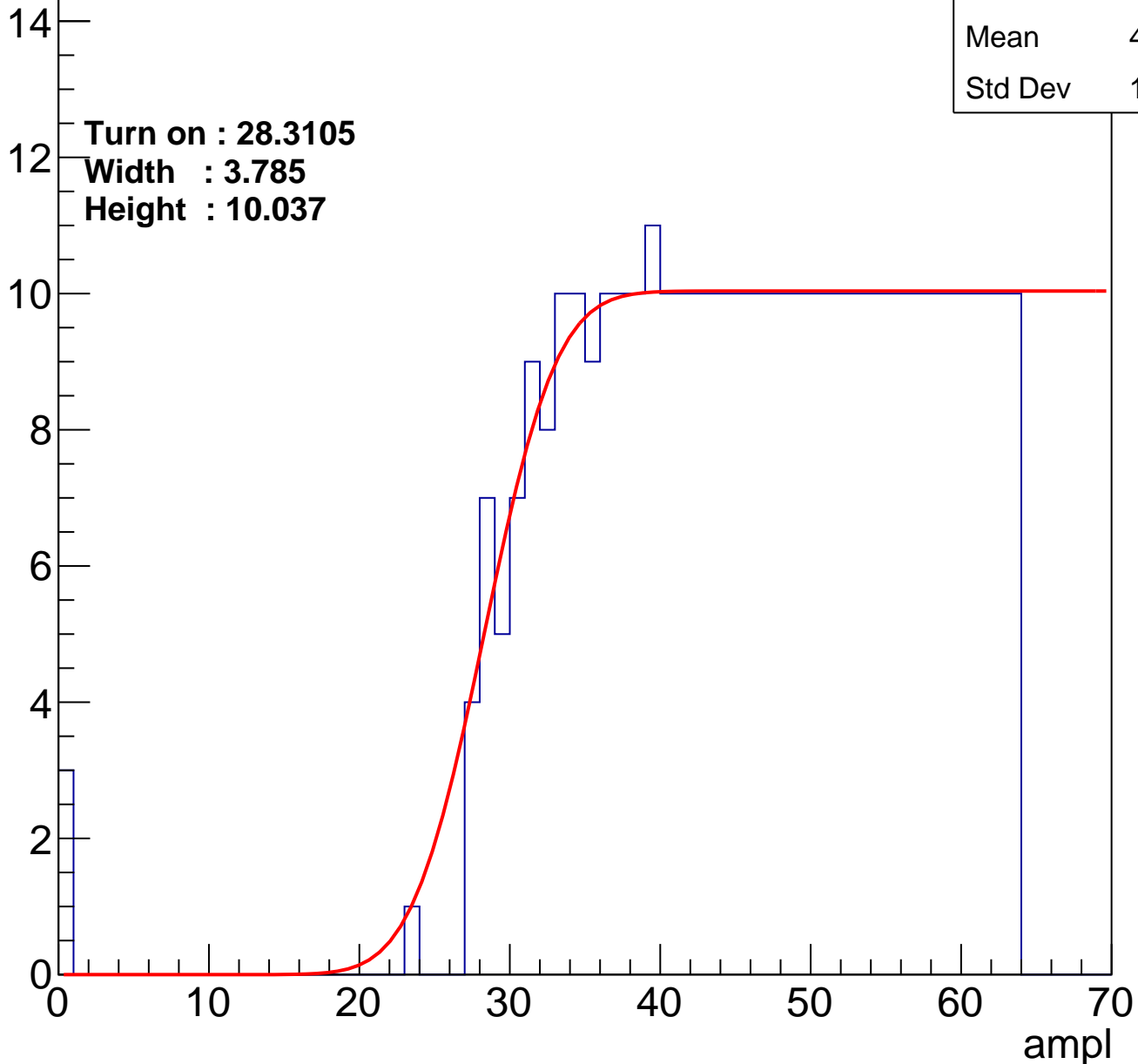
Entries	354
Mean	45.48
Std Dev	11.06

Turn on : 28.3105

Width : 3.785

Height : 10.037

Entry



# B1L100S, U13-ch99

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	386
Mean	43.89
Std Dev	11.86

Turn on : 26.0050

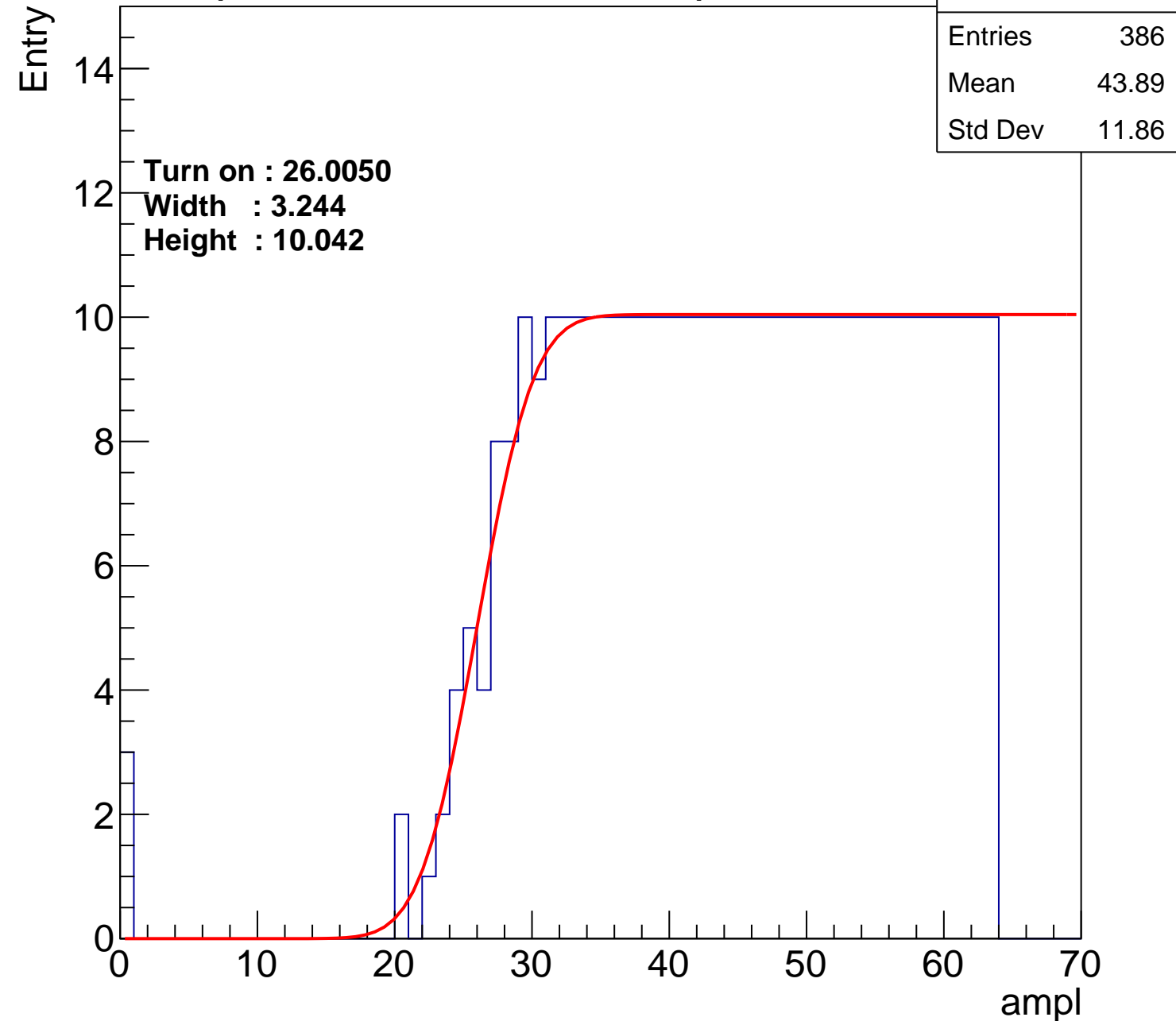
Width : 3.244

Height : 10.042

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch100

calib\_packv5\_042523\_0143.root, FC#4, port A2

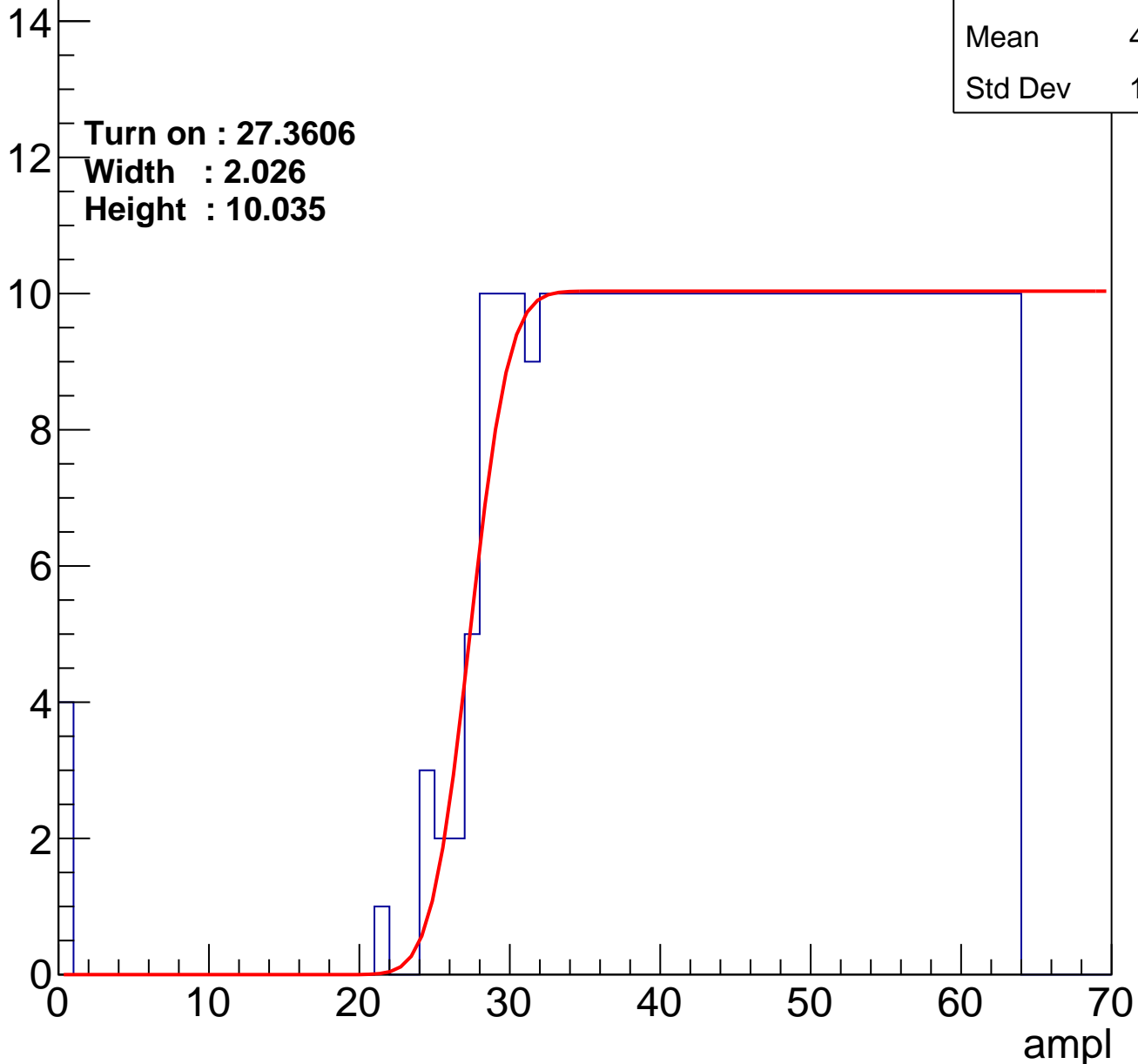
Entries	376
Mean	44.36
Std Dev	11.73

Turn on : 27.3606

Width : 2.026

Height : 10.035

Entry



# B1L100S, U13-ch101

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	365
Mean	44.95
Std Dev	11.2

Turn on : 27.5722

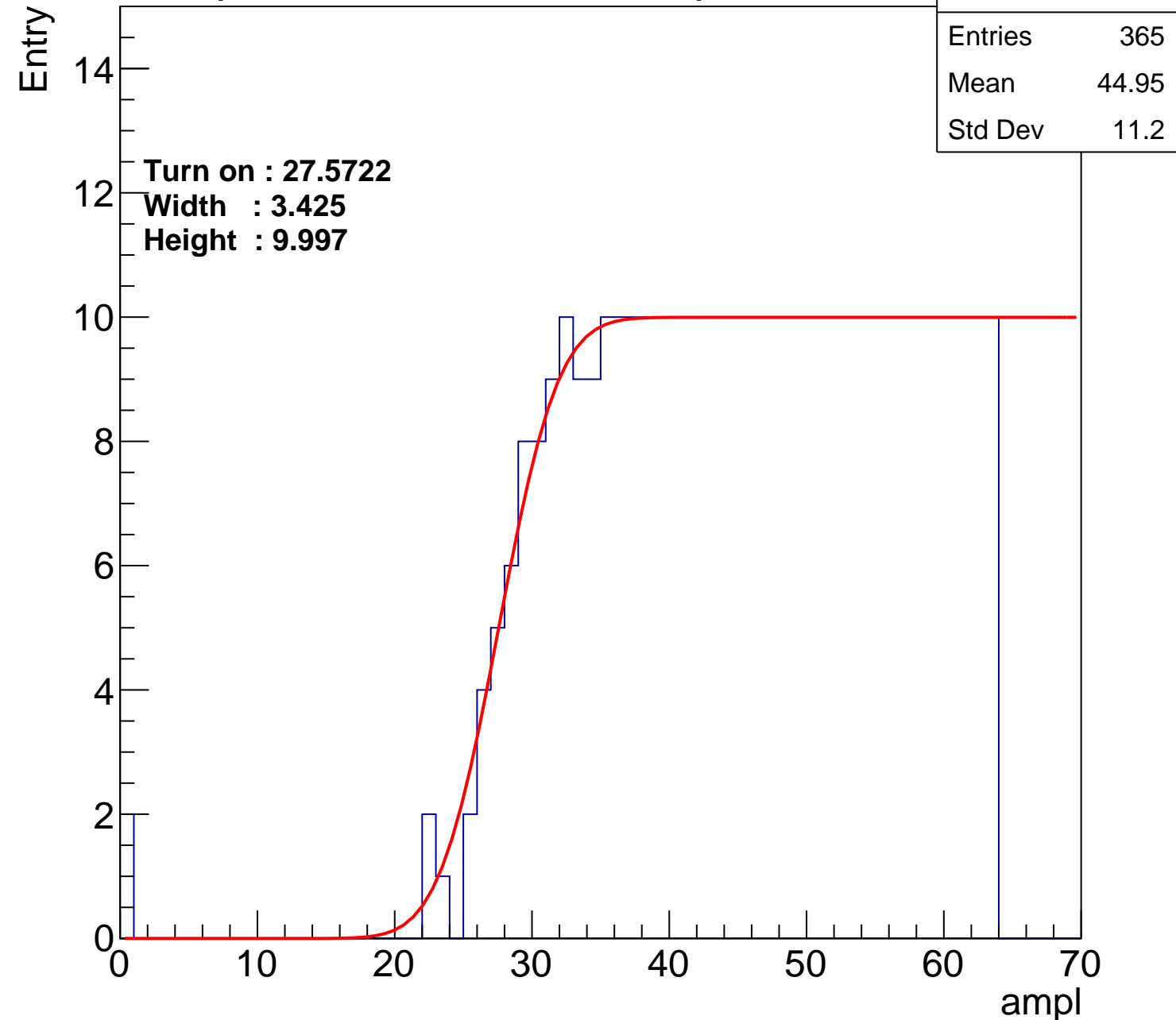
Width : 3.425

Height : 9.997

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch102

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	356
Mean	45.31
Std Dev	11.3

Turn on : 29.0002

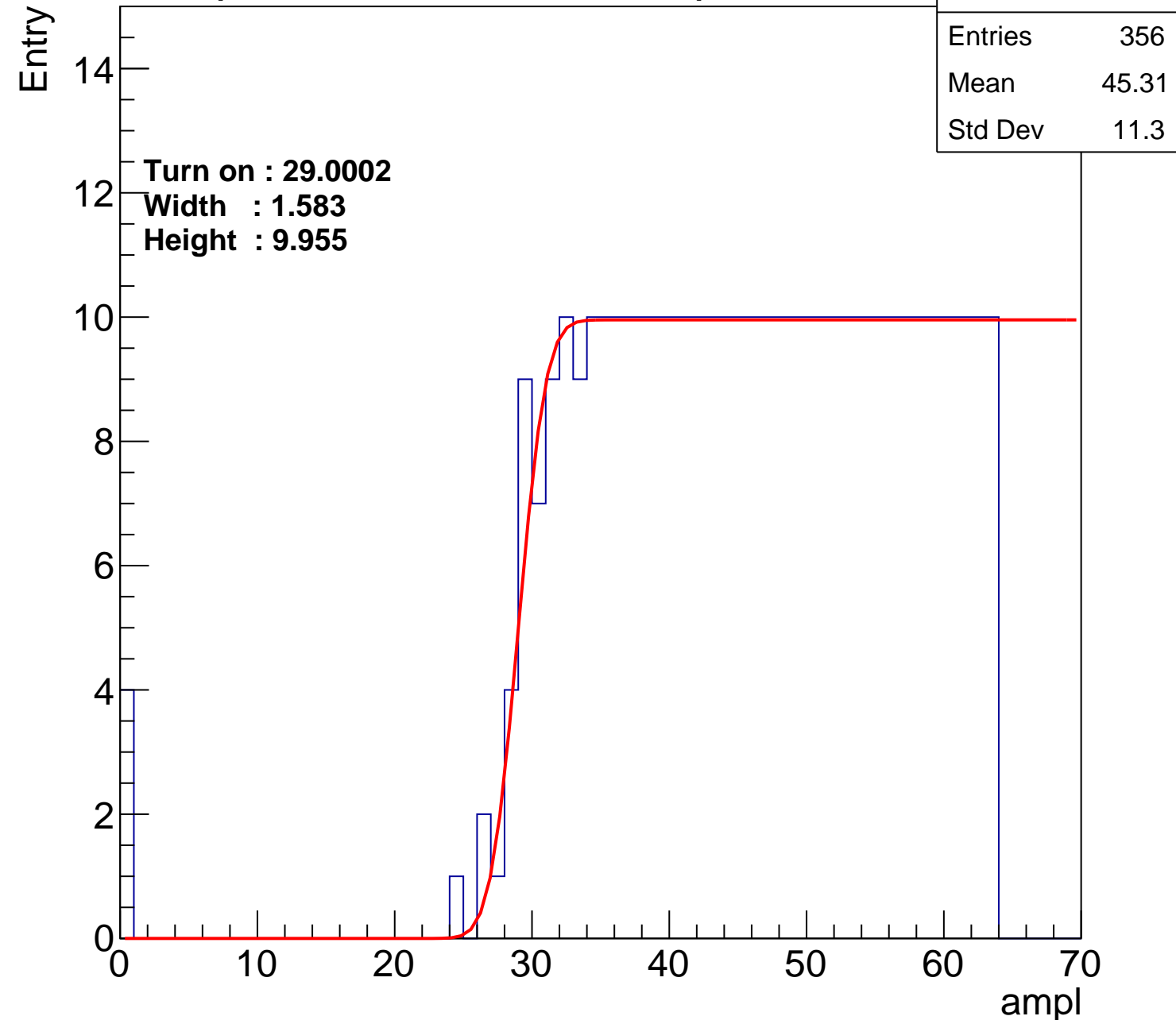
Width : 1.583

Height : 9.955

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U13-ch103

**calib\_packv5\_042523\_0143.root, FC#4, port A2**

Entries	349
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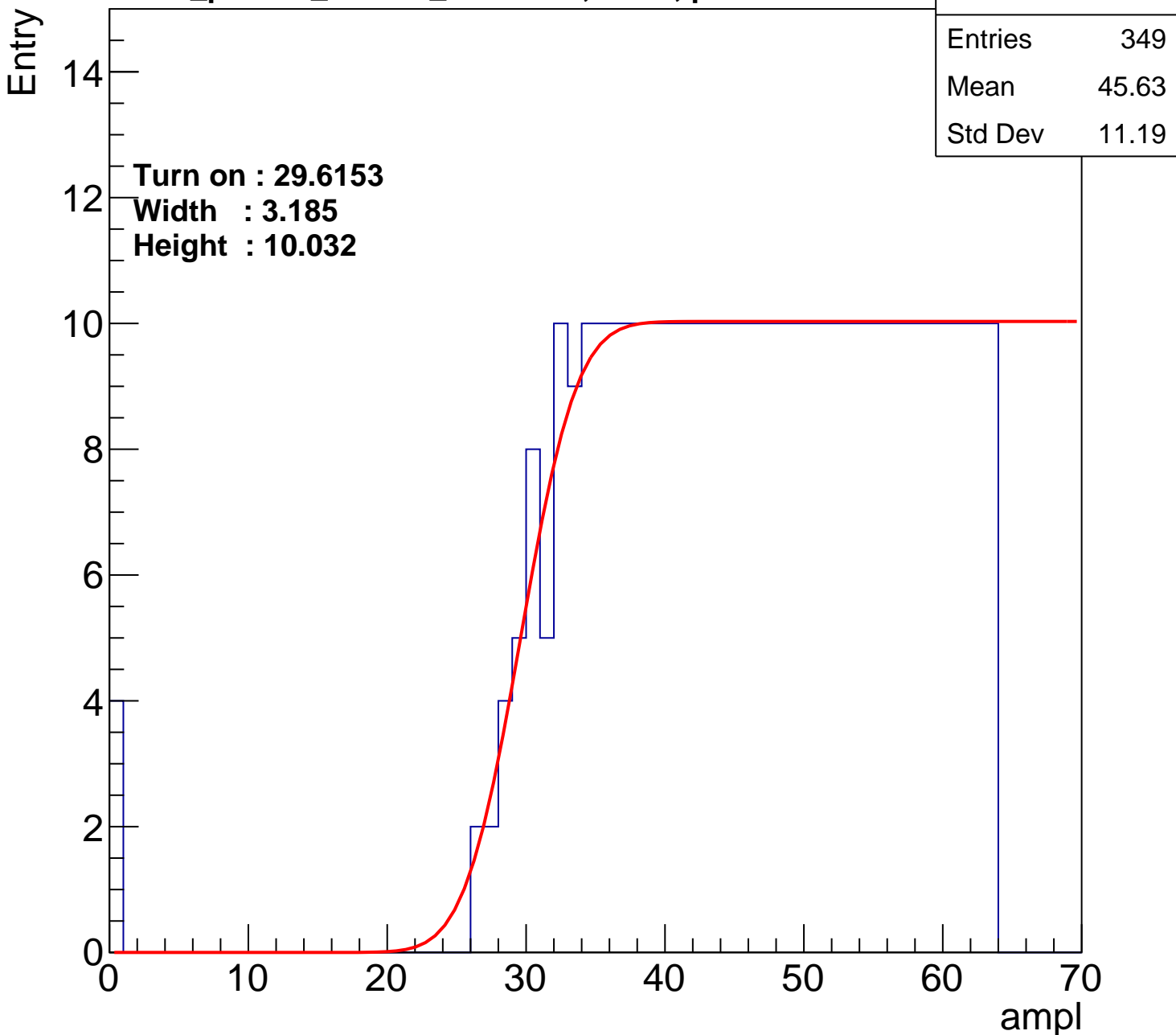
Mean	45.63
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Std Dev	11.19
---------	-------

**Turn on : 29.6153**

**Width : 3.185**

**Height : 10.032**



# B1L100S, U13-ch104

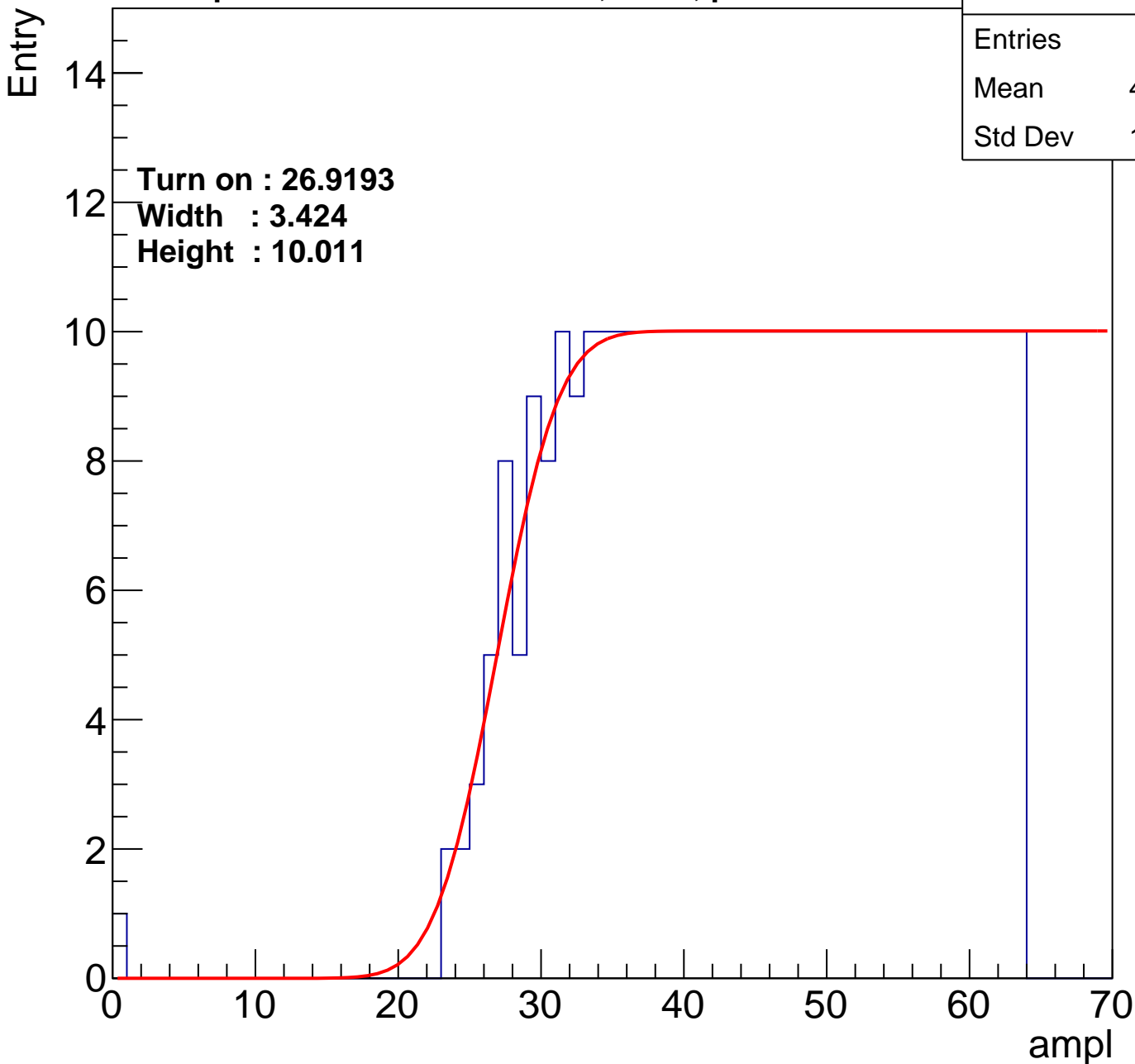
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	372
Mean	44.72
Std Dev	11.13

Turn on : 26.9193

Width : 3.424

Height : 10.011



# B1L100S, U13-ch105

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	368
Mean	44.88
Std Dev	11.07

Turn on : 27.6380

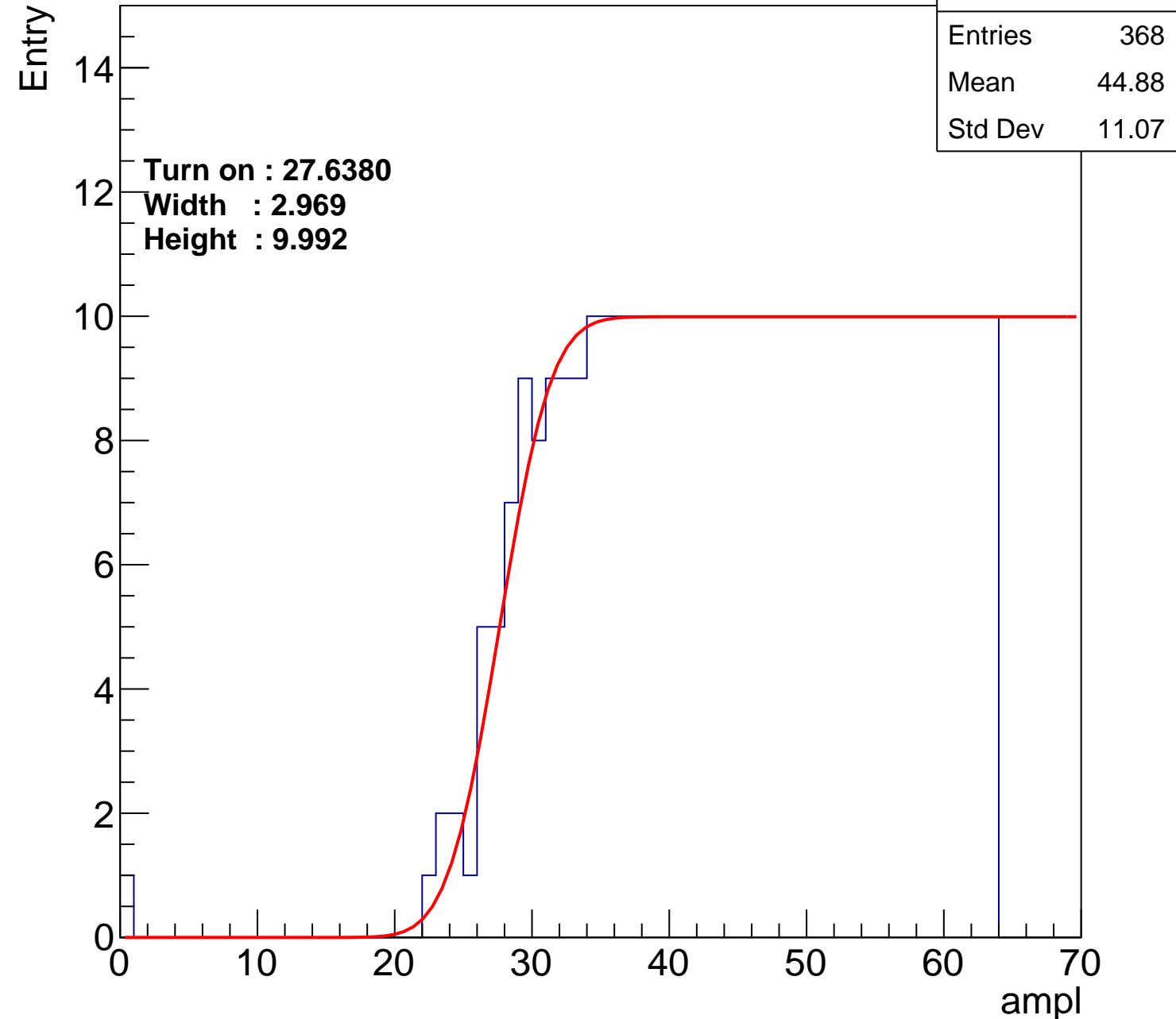
Width : 2.969

Height : 9.992

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch106

calib\_packv5\_042523\_0143.root, FC#4, port A2

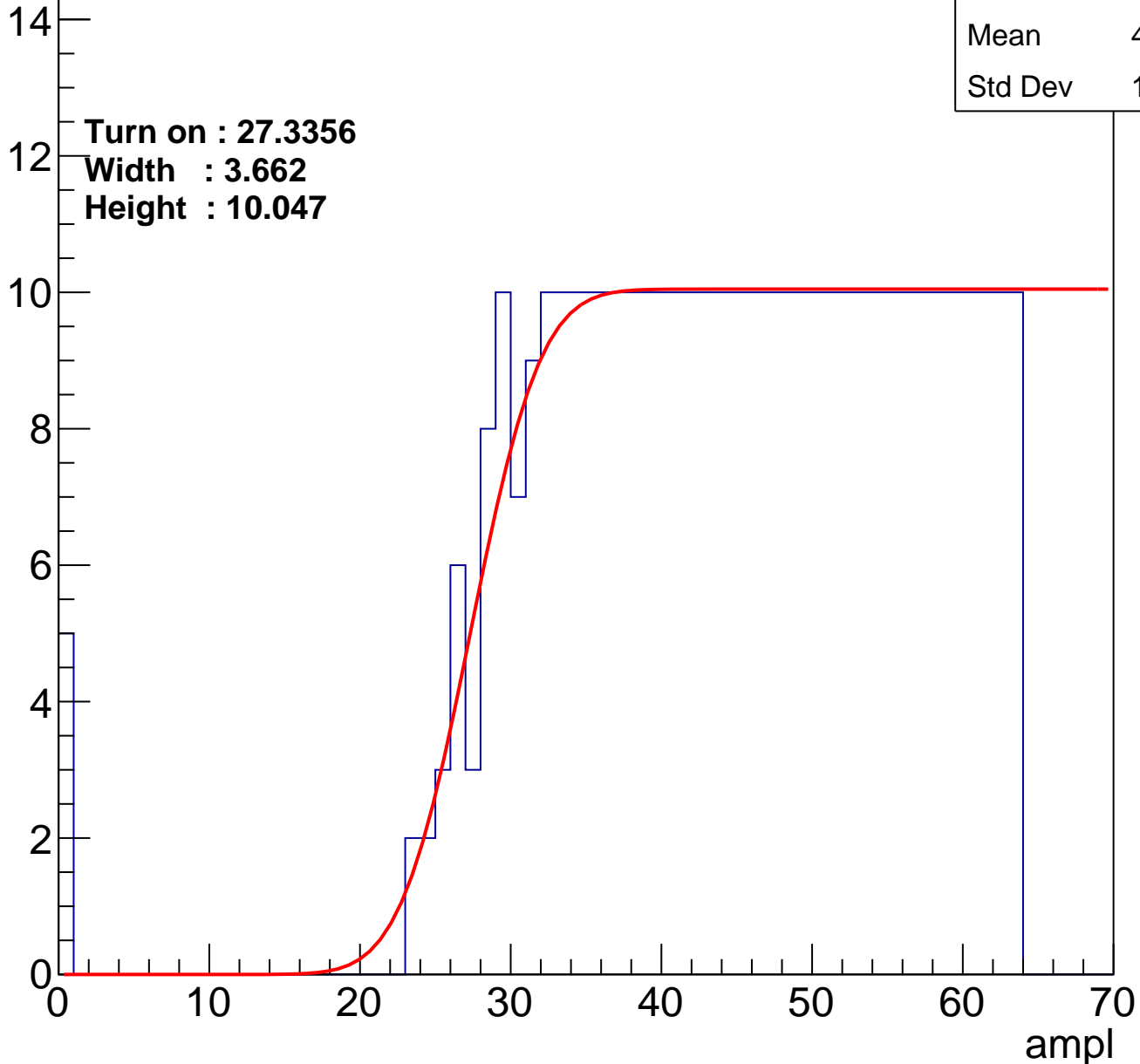
Entries	375
Mean	44.29
Std Dev	11.96

Turn on : 27.3356

Width : 3.662

Height : 10.047

Entry



# B1L100S, U13-ch107

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	381
Mean	44.34
Std Dev	11.25

**Turn on : 25.8190**

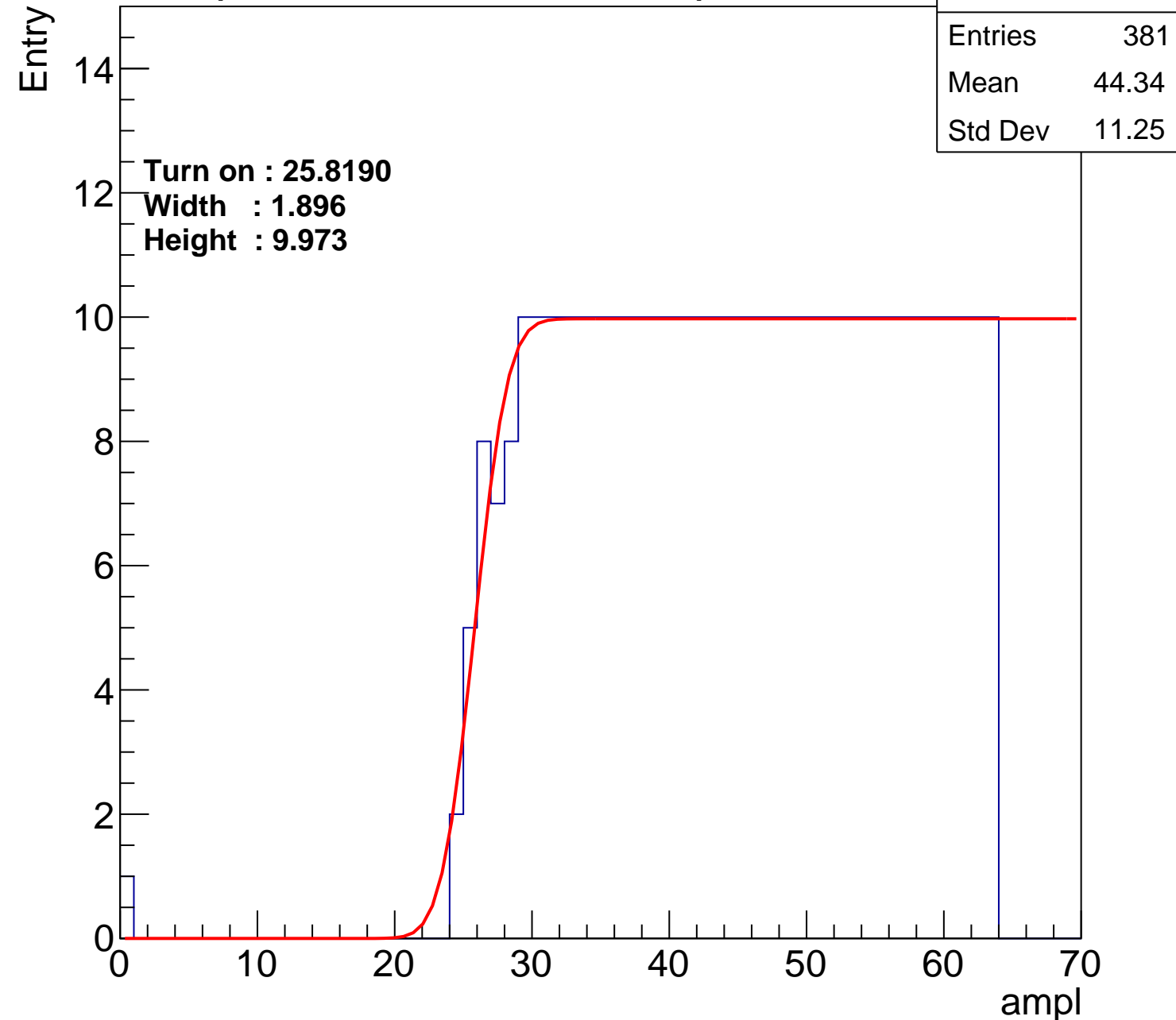
**Width : 1.896**

**Height : 9.973**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch108

calib\_packv5\_042523\_0143.root, FC#4, port A2

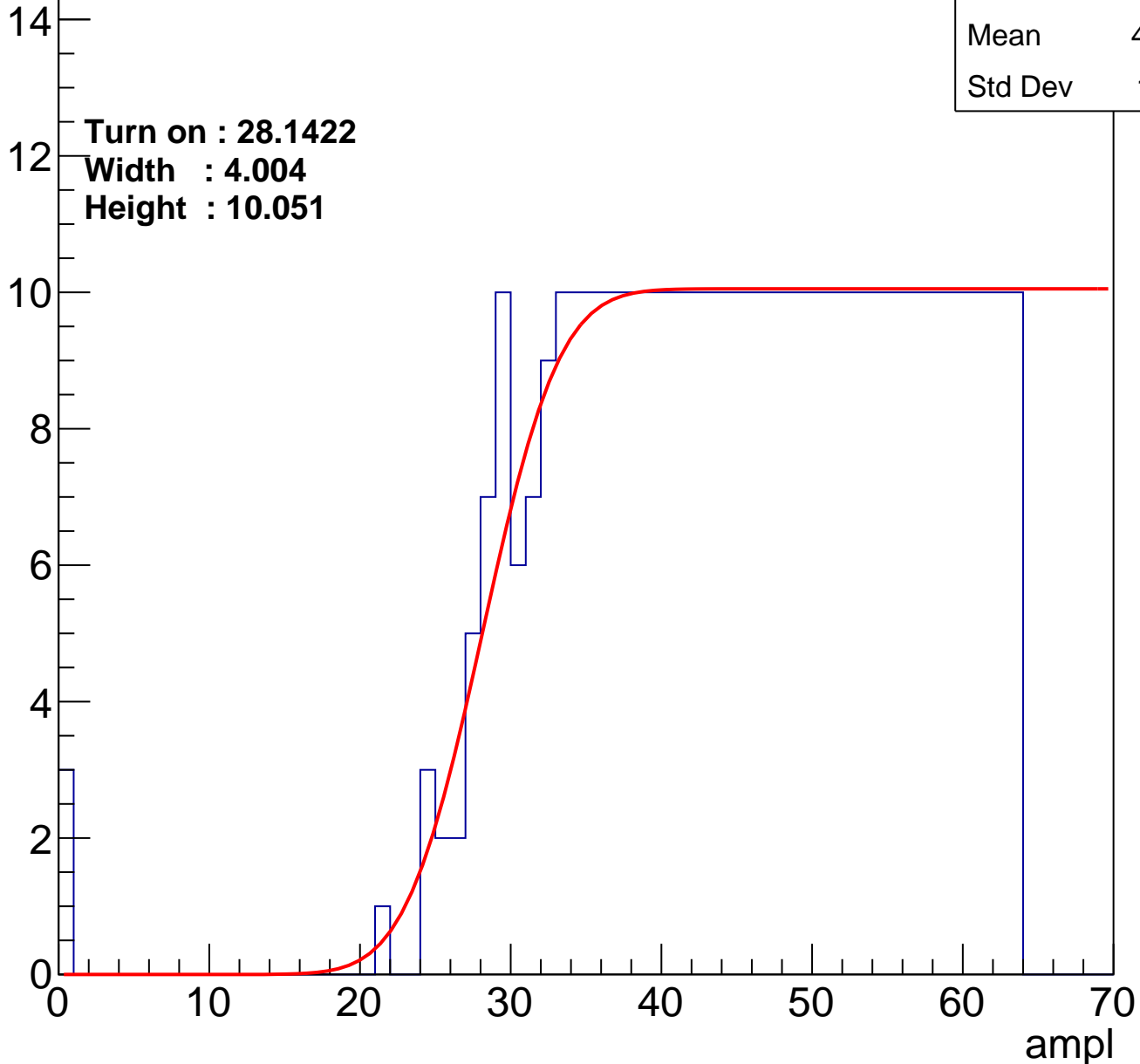
Entries	365
Mean	44.88
Std Dev	11.41

Turn on : 28.1422

Width : 4.004

Height : 10.051

Entry



# B1L100S, U13-ch109

calib\_packv5\_042523\_0143.root, FC#4, port A2

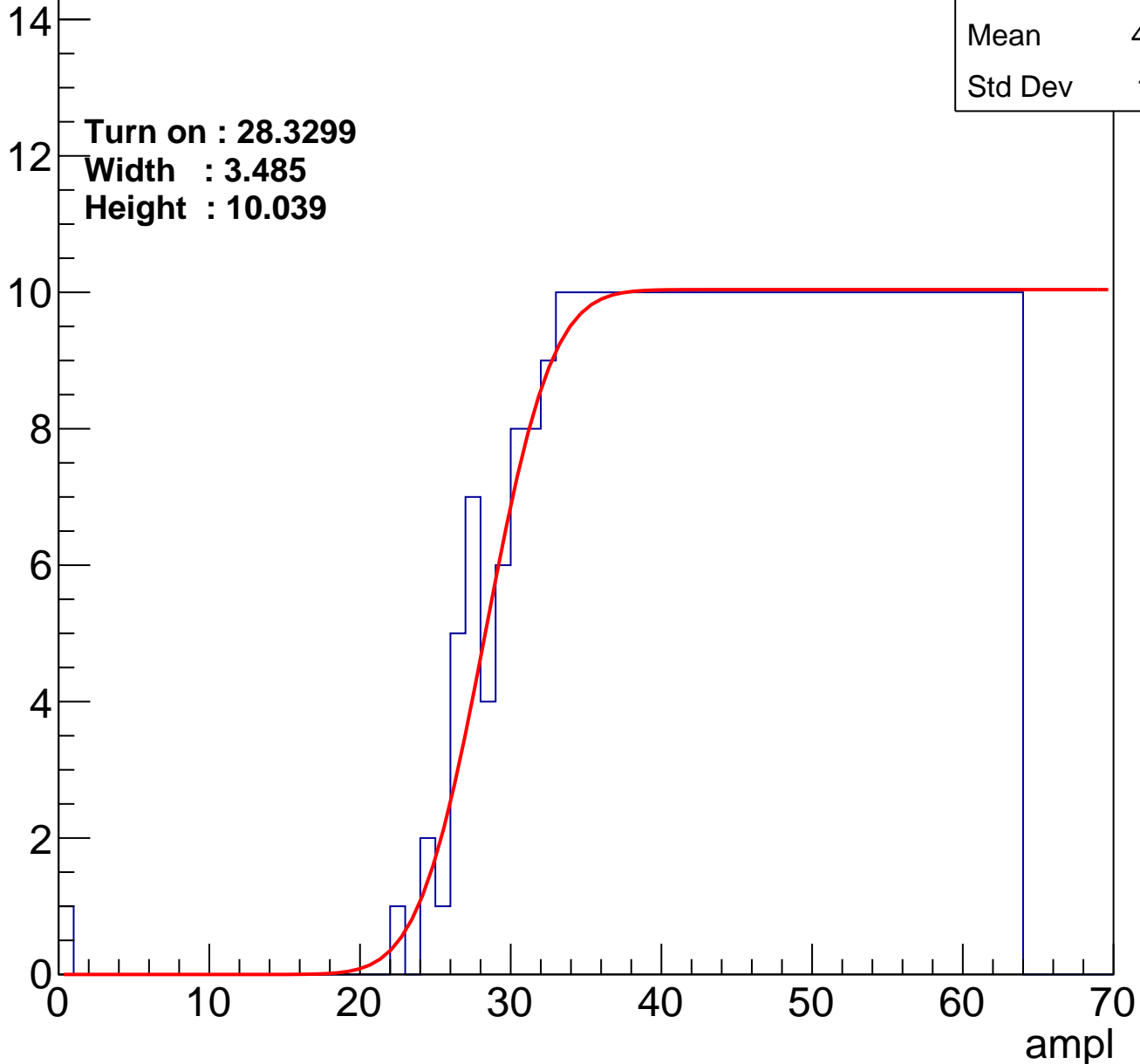
Entries	362
Mean	45.18
Std Dev	10.91

Turn on : 28.3299

Width : 3.485

Height : 10.039

Entry



# B1L100S, U13-ch110

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	367
Mean	44.95
Std Dev	11.11

Turn on : 27.4231

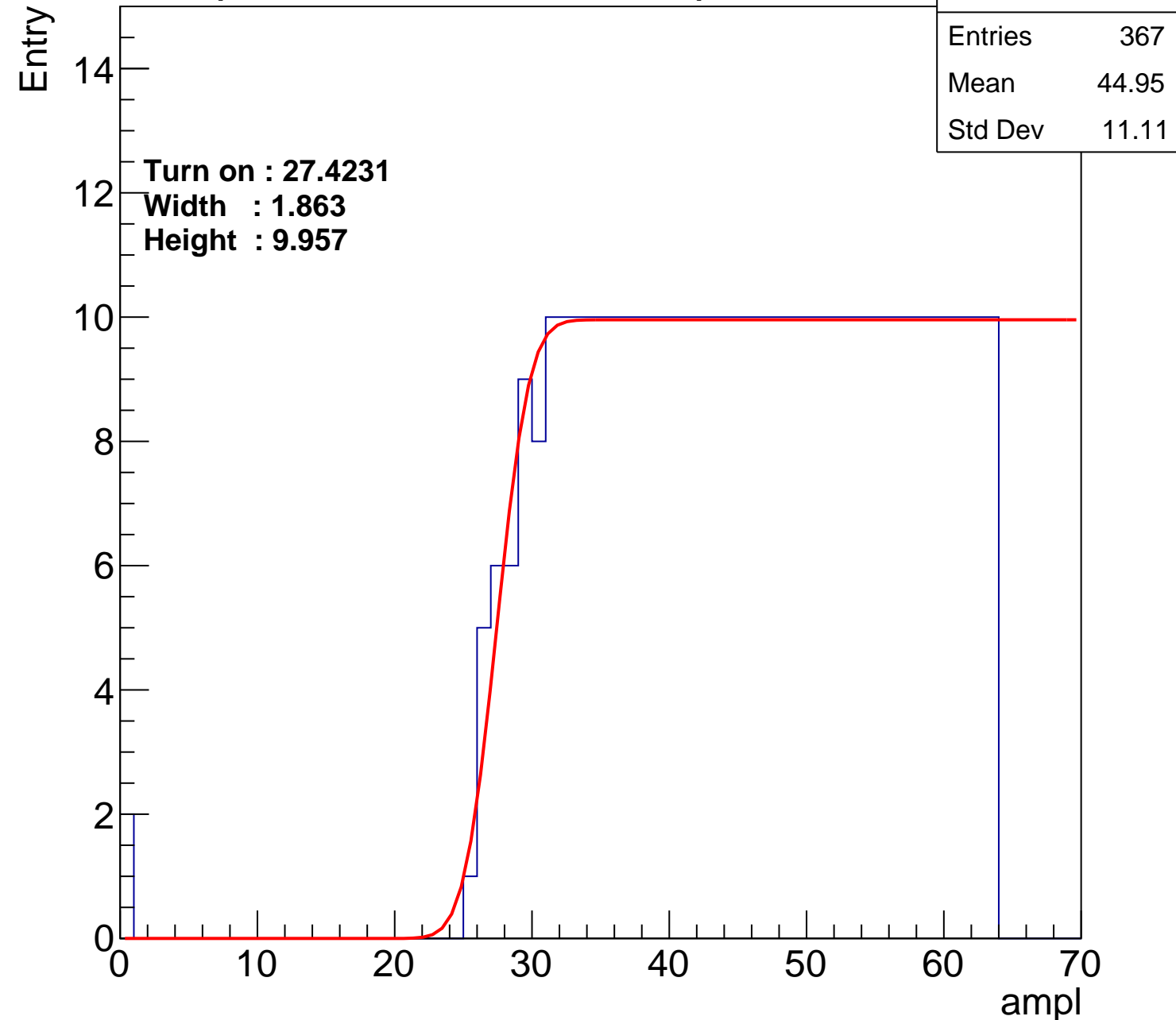
Width : 1.863

Height : 9.957

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U13-ch111

calib\_packv5\_042523\_0143.root, FC#4, port A2

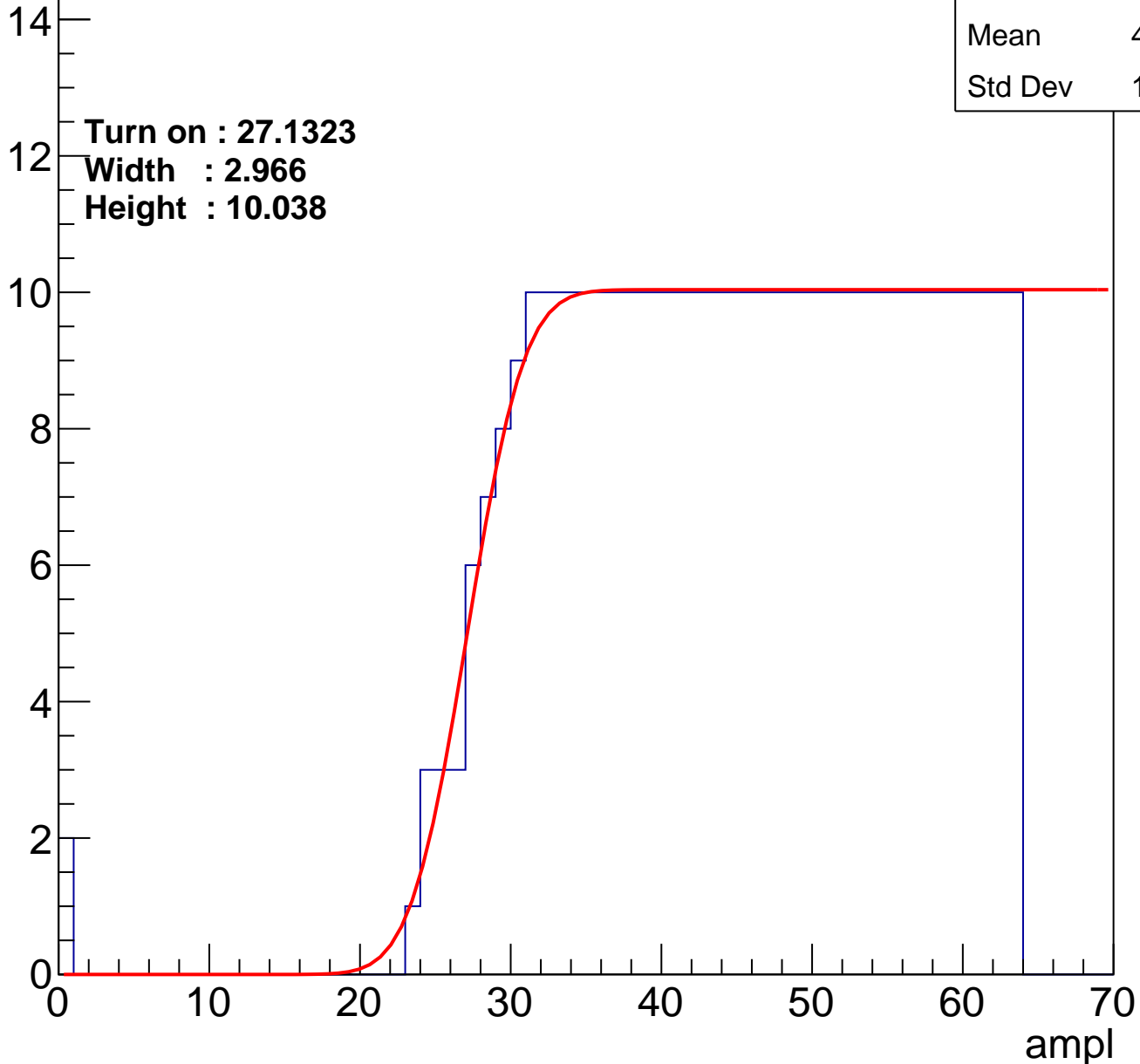
Entries	372
Mean	44.67
Std Dev	11.29

**Turn on : 27.1323**

**Width : 2.966**

**Height : 10.038**

Entry



# B1L100S, U13-ch112

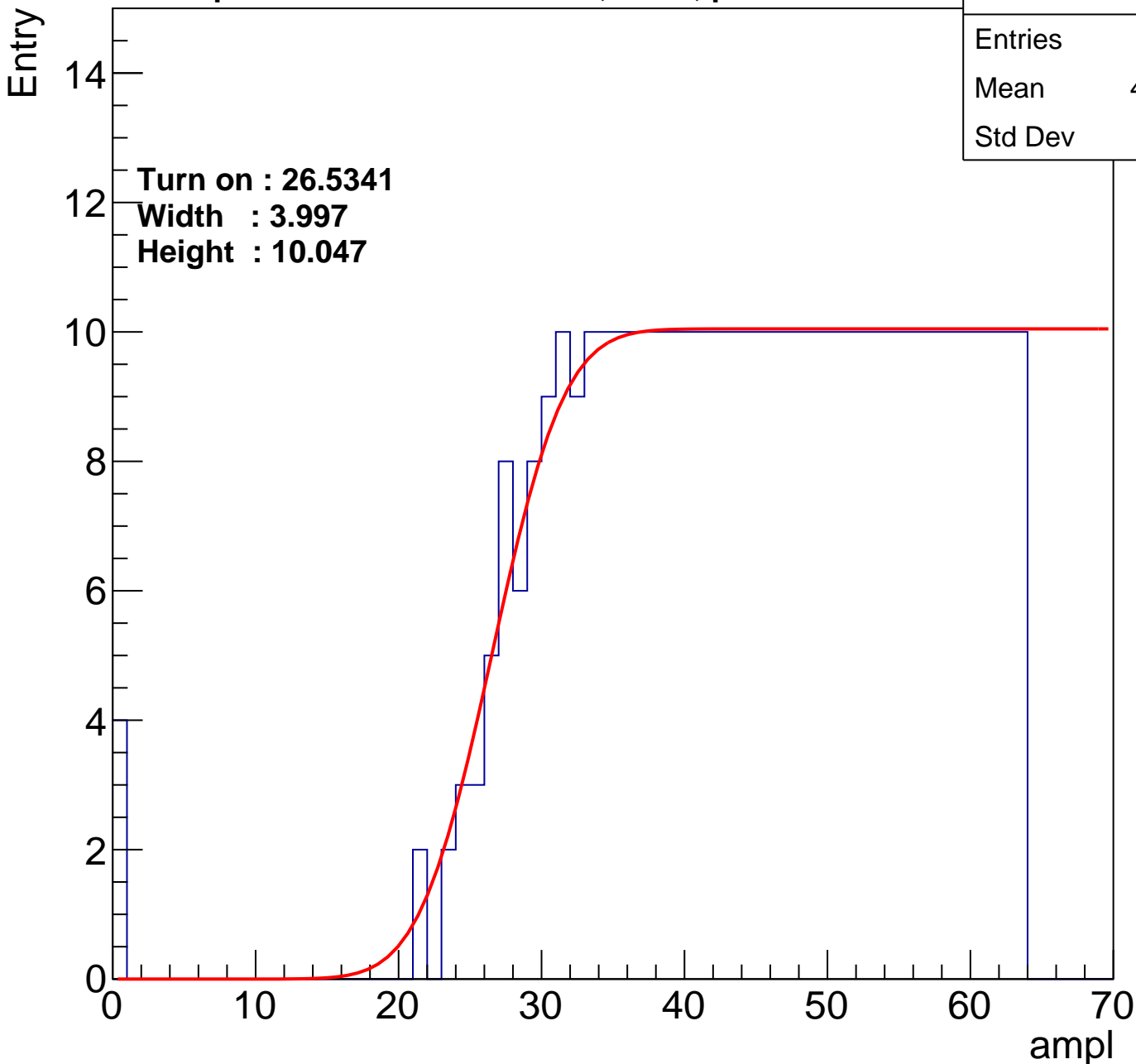
calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	379
Mean	44.14
Std Dev	11.91

Turn on : 26.5341

Width : 3.997

Height : 10.047



# B1L100S, U13-ch113

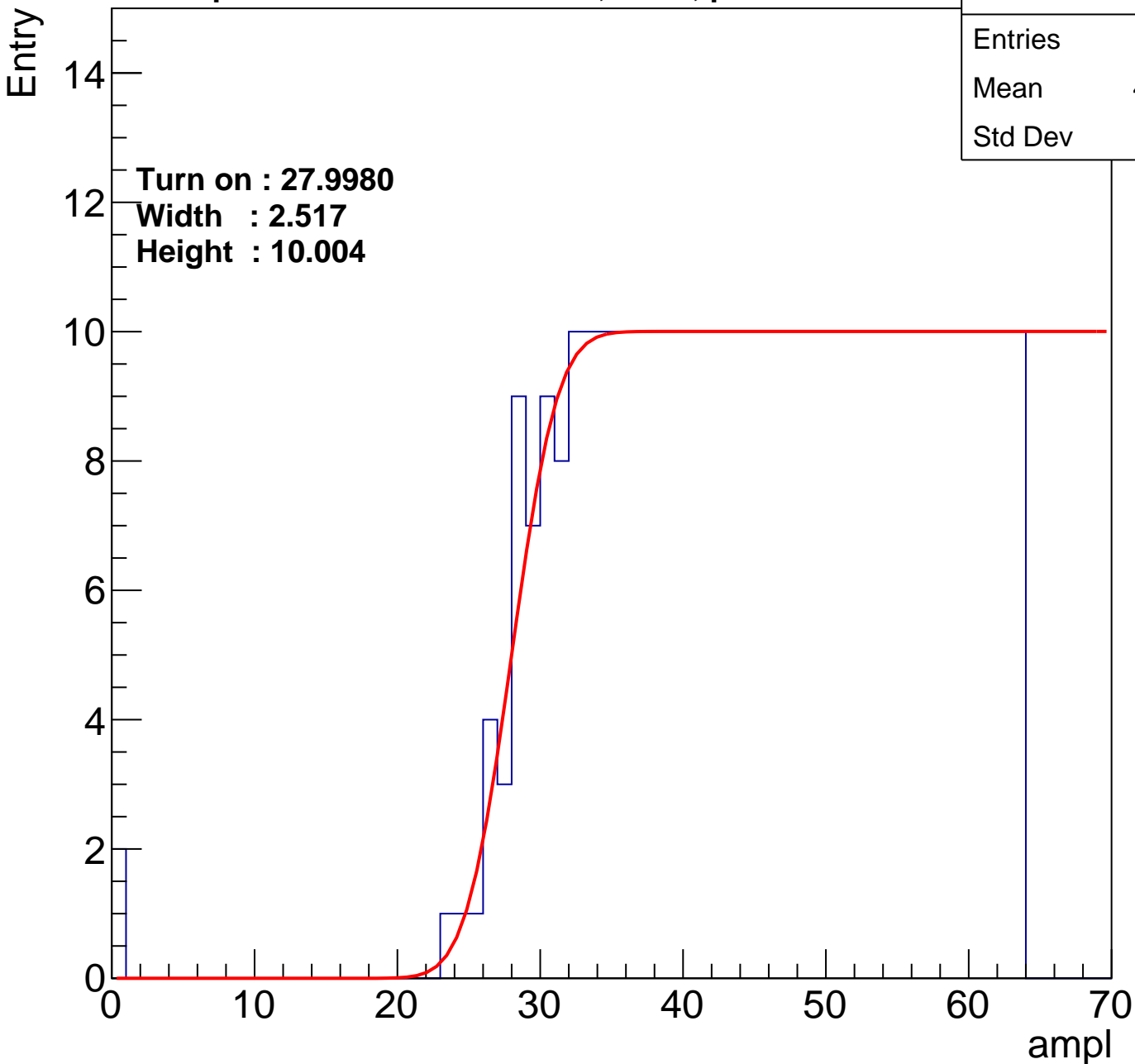
**calib\_packv5\_042523\_0143.root, FC#4, port A2**

**Turn on : 27.9980**

**Width : 2.517**

**Height : 10.004**

Entries	365
Mean	45.01
Std Dev	11.11



# B1L100S, U13-ch114

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	363
Mean	44.96
Std Dev	11.48

Turn on : 29.1573

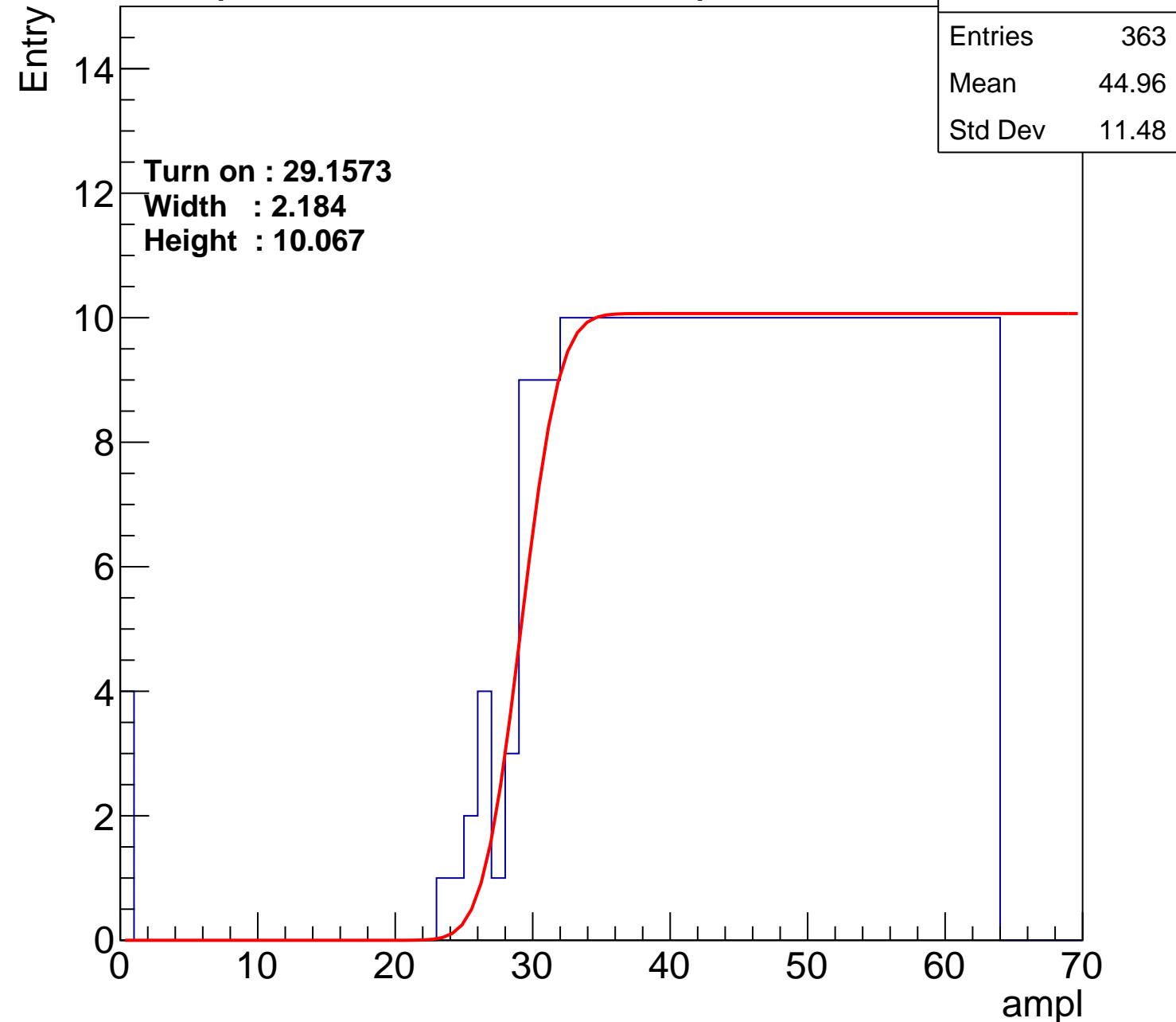
Width : 2.184

Height : 10.067

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch115

calib\_packv5\_042523\_0143.root, FC#4, port A2

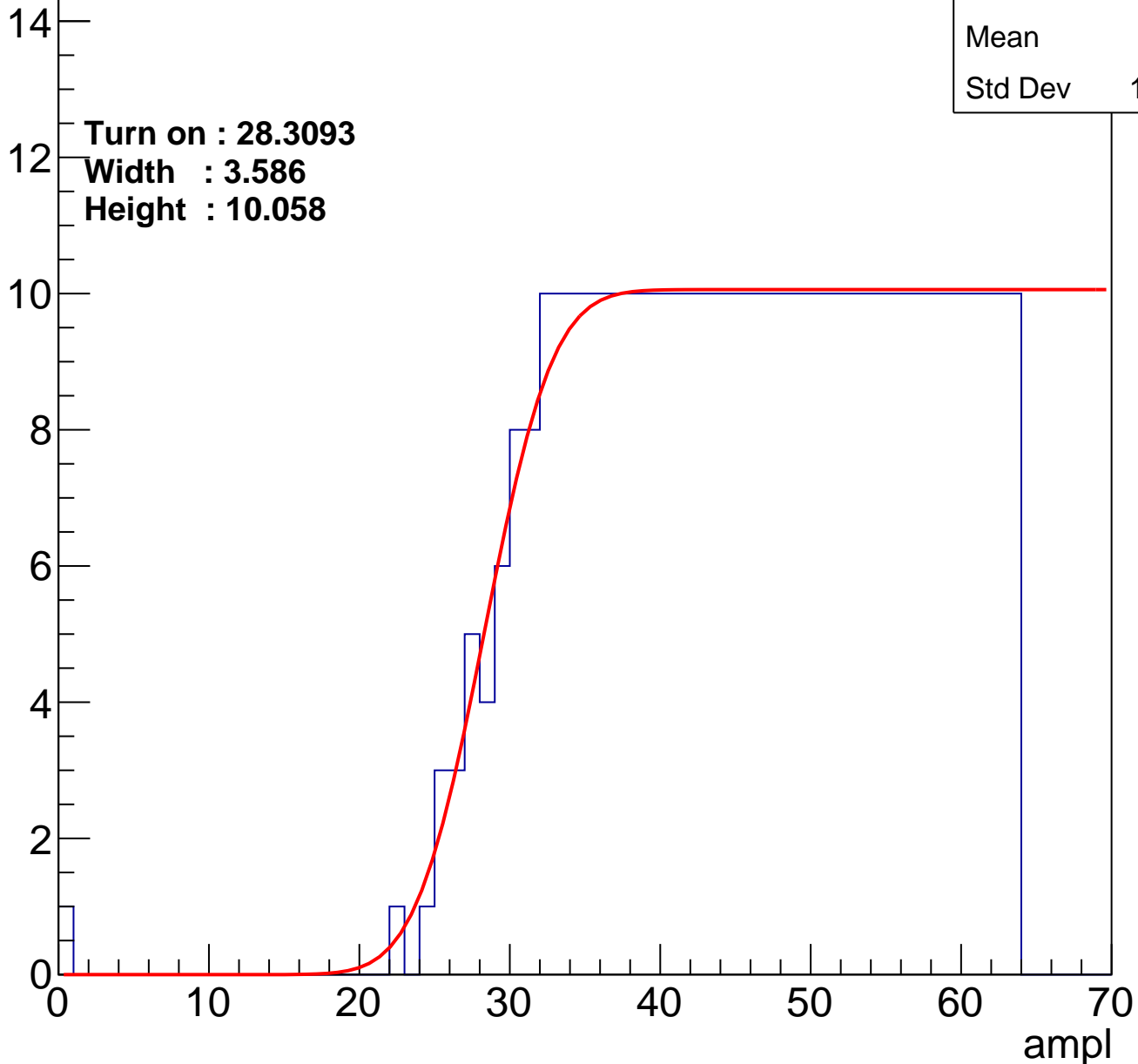
Entries	360
Mean	45.3
Std Dev	10.83

Turn on : 28.3093

Width : 3.586

Height : 10.058

Entry



# B1L100S, U13-ch116

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	379
Mean	44.15
Std Dev	11.89

Turn on : 27.3424

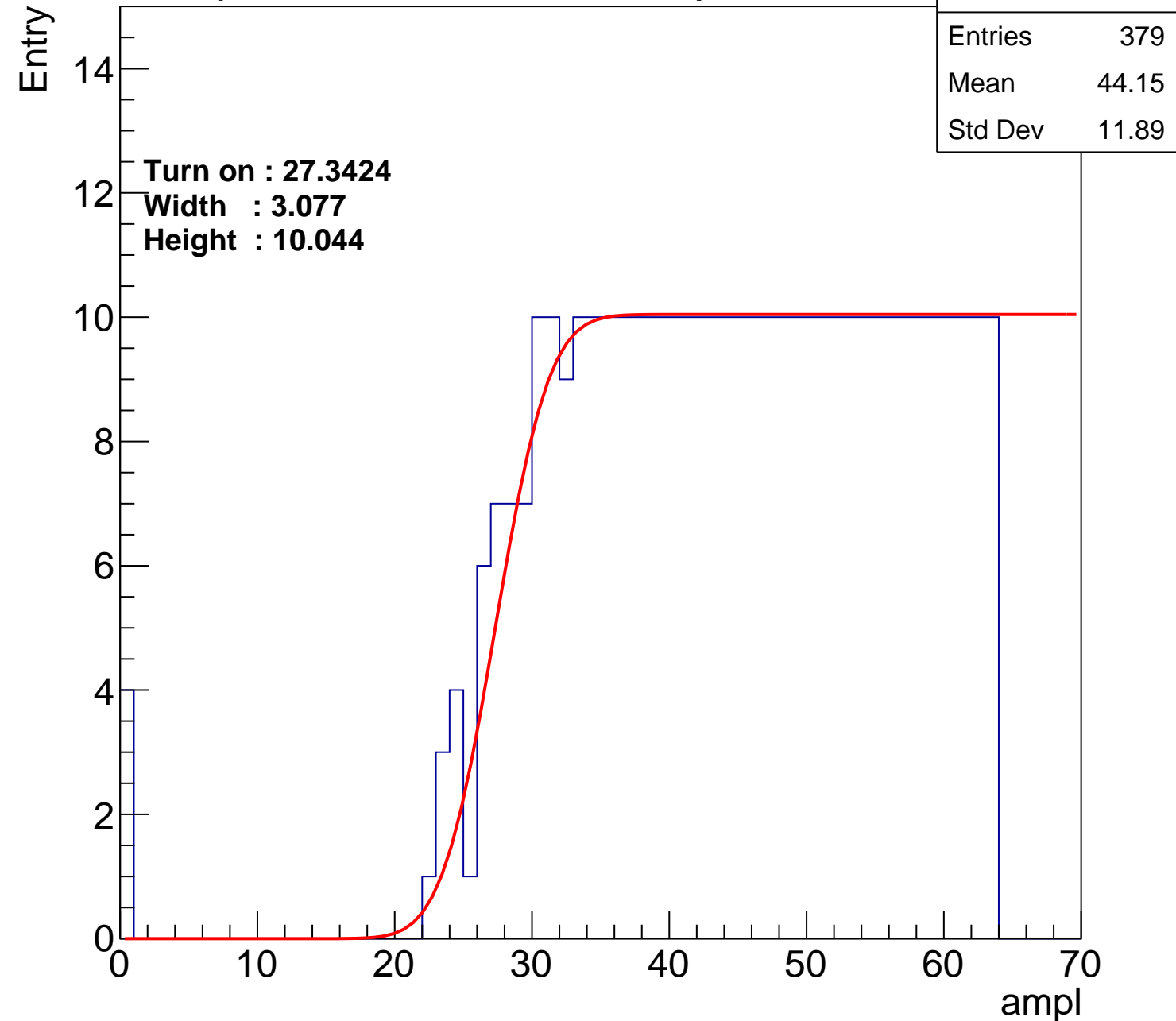
Width : 3.077

Height : 10.044

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch117

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	358
Mean	45.24
Std Dev	11.21

Turn on : 28.6593

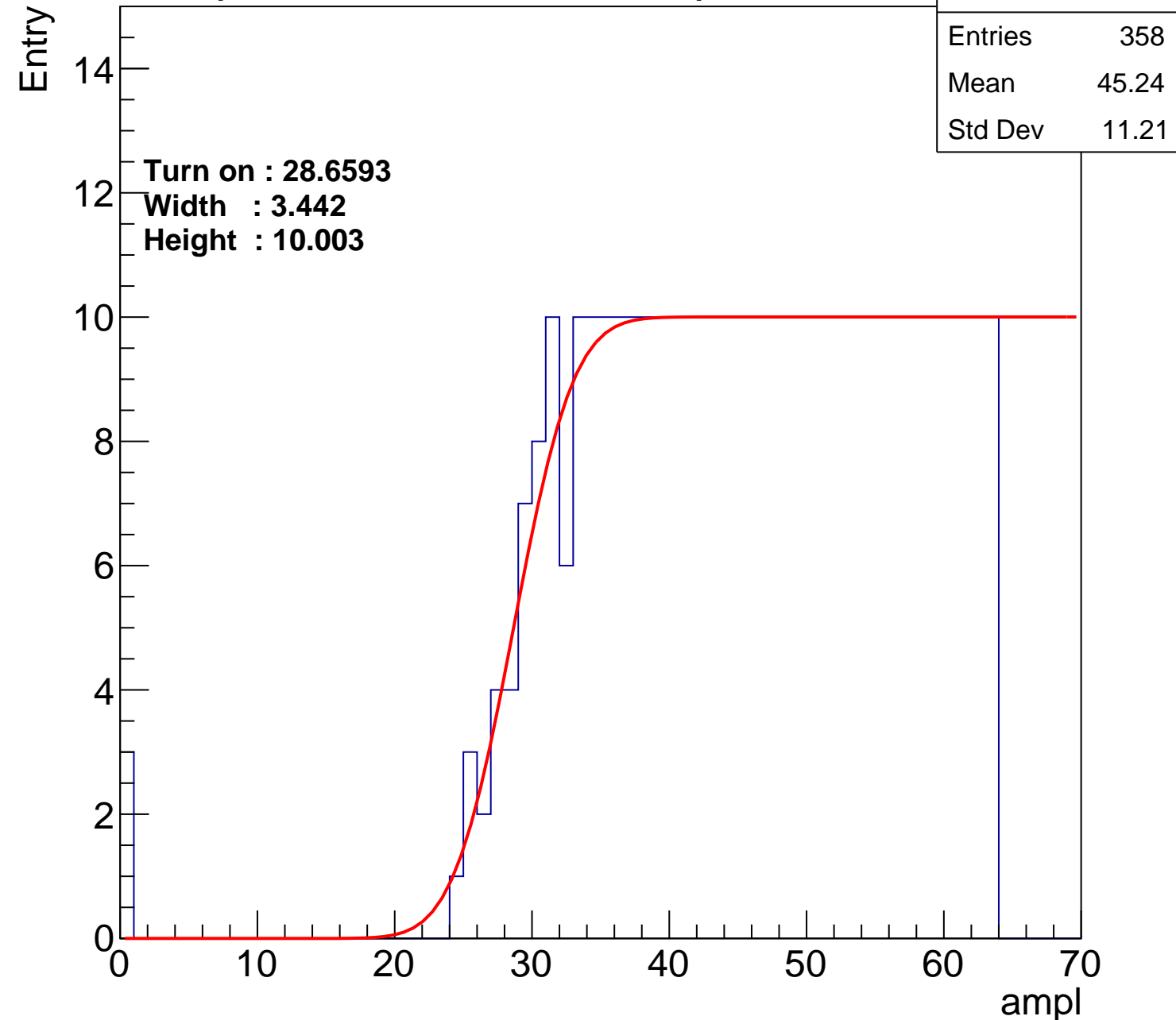
Width : 3.442

Height : 10.003

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch118

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	362
Mean	45.1
Std Dev	11.12

Turn on : 28.1205

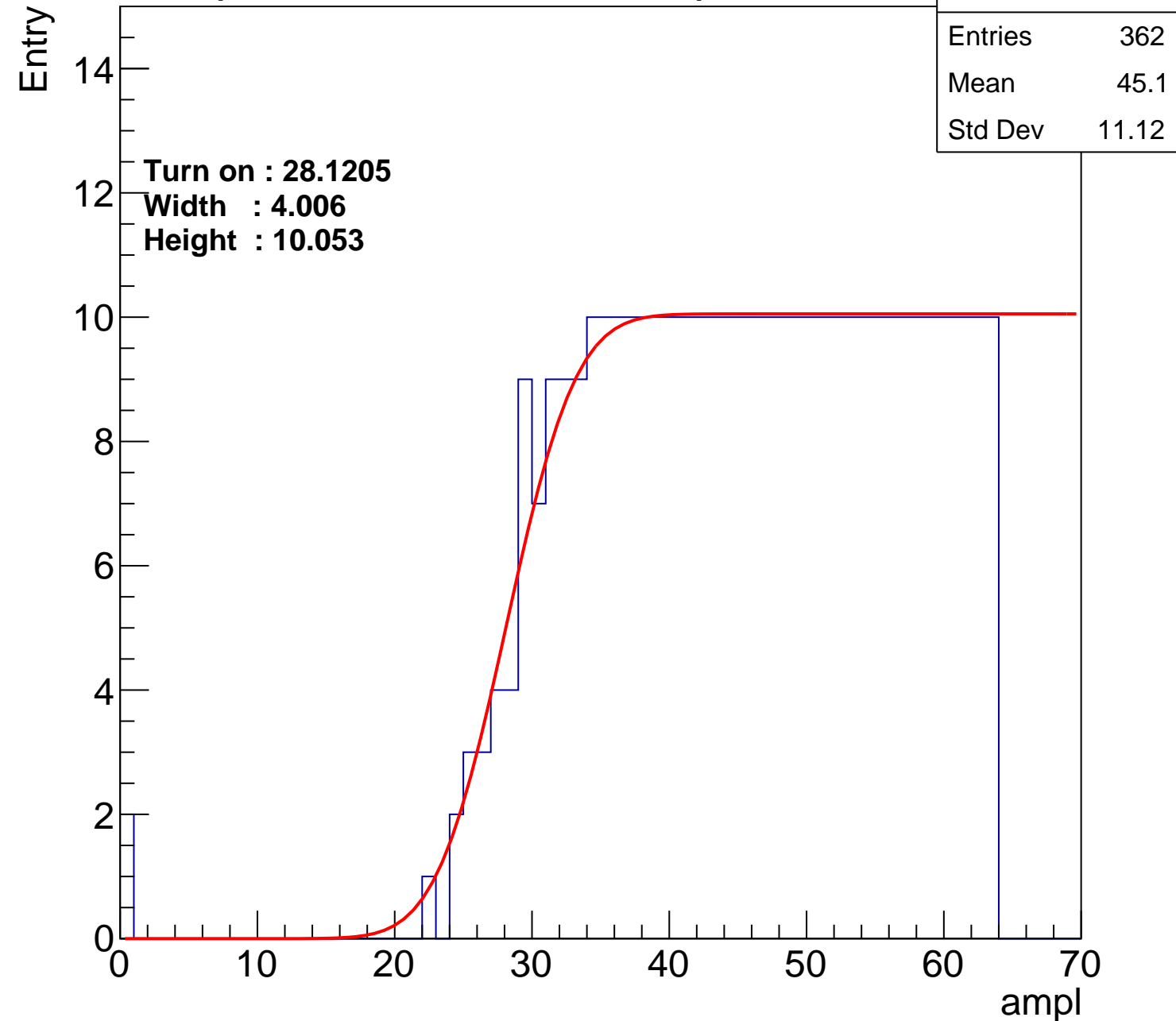
Width : 4.006

Height : 10.053

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L100S, U13-ch119

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	375
Mean	44.45
Std Dev	11.56

**Turn on : 26.8046**

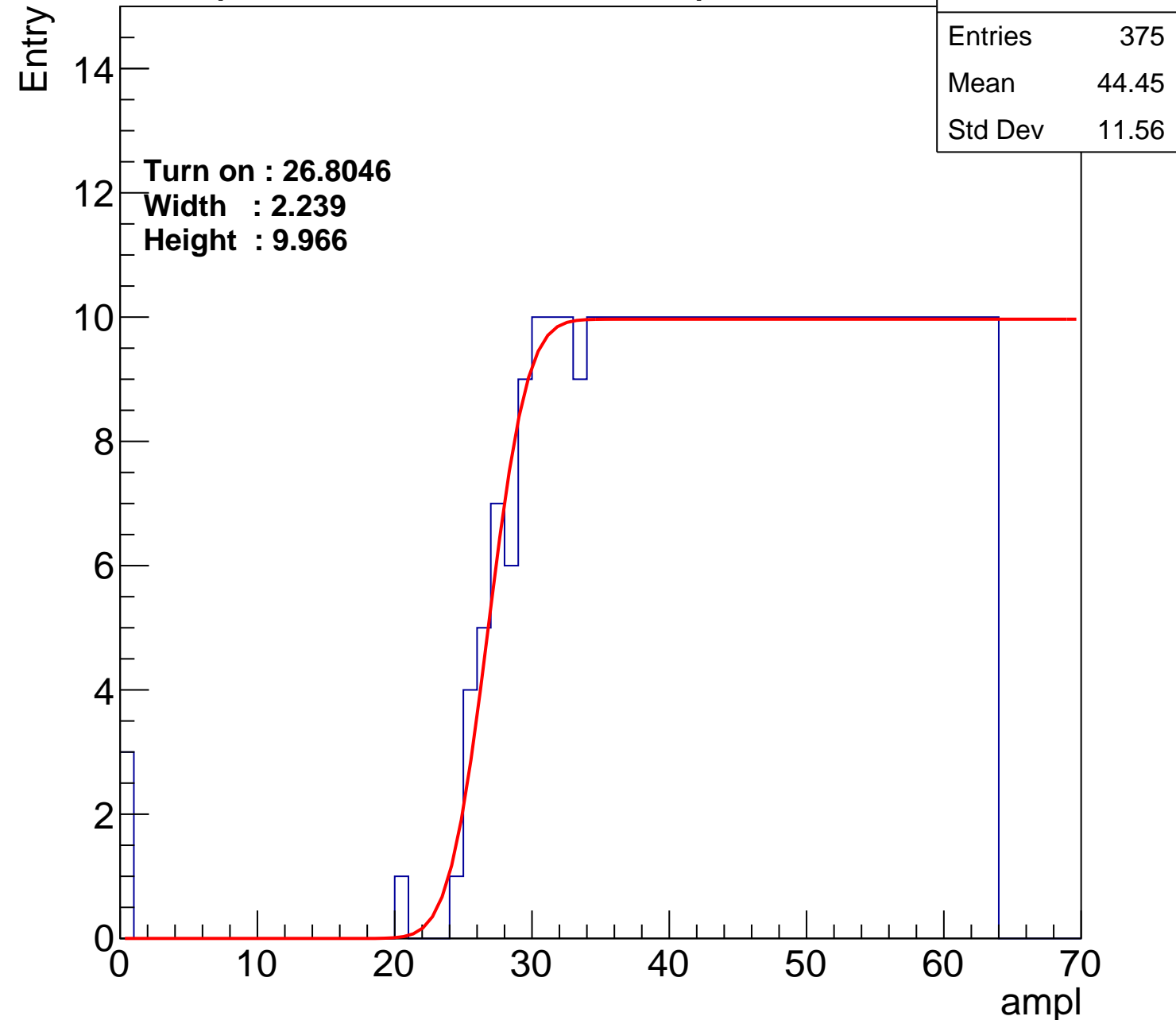
**Width : 2.239**

**Height : 9.966**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch120

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	368
Mean	44.84
Std Dev	11.23

**Turn on : 27.6660**

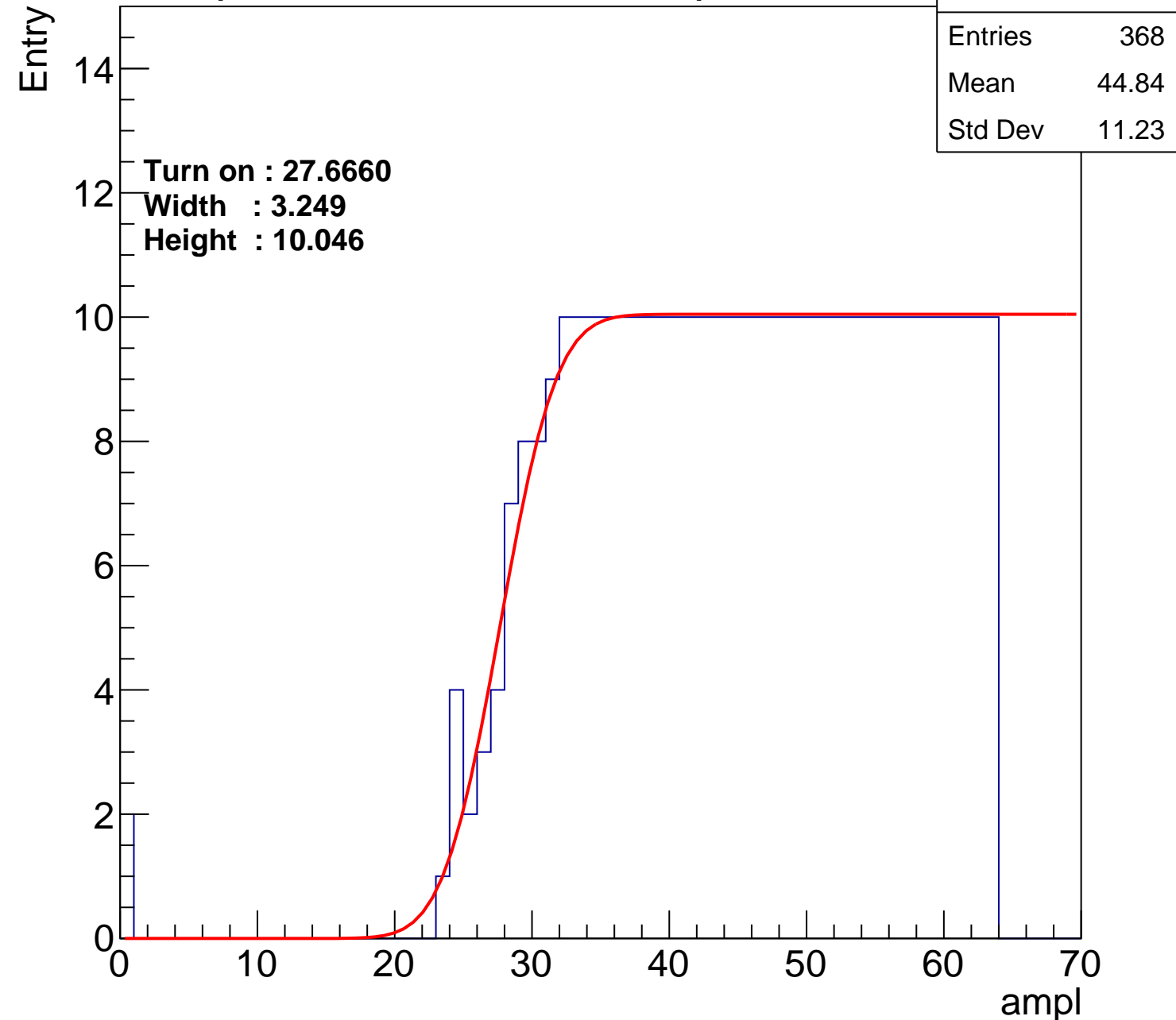
**Width : 3.249**

**Height : 10.046**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch121

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	367
Mean	44.98
Std Dev	10.97

Turn on : 27.3175

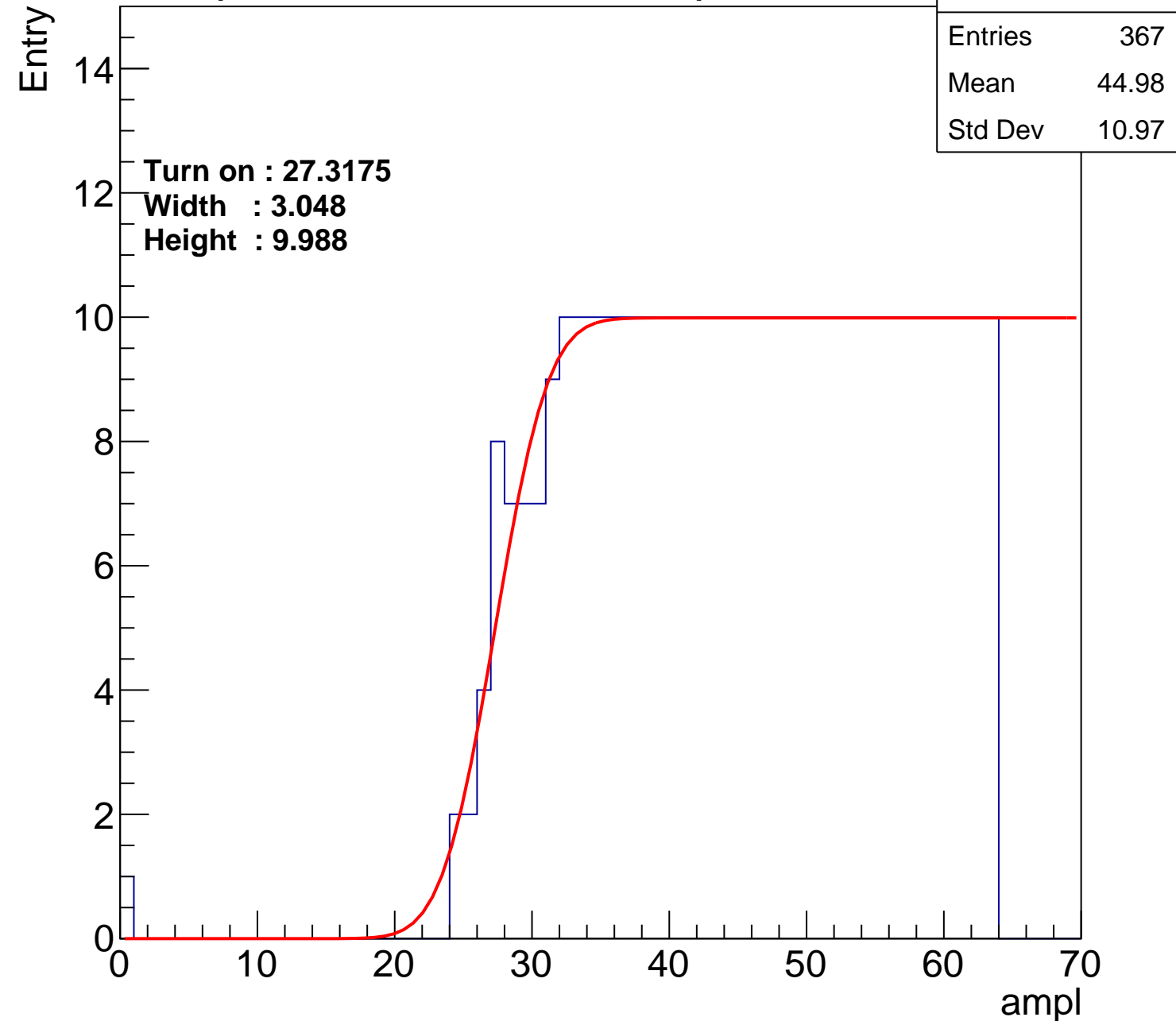
Width : 3.048

Height : 9.988

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch122

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	370
Mean	44.54
Std Dev	11.76

**Turn on : 28.7087**

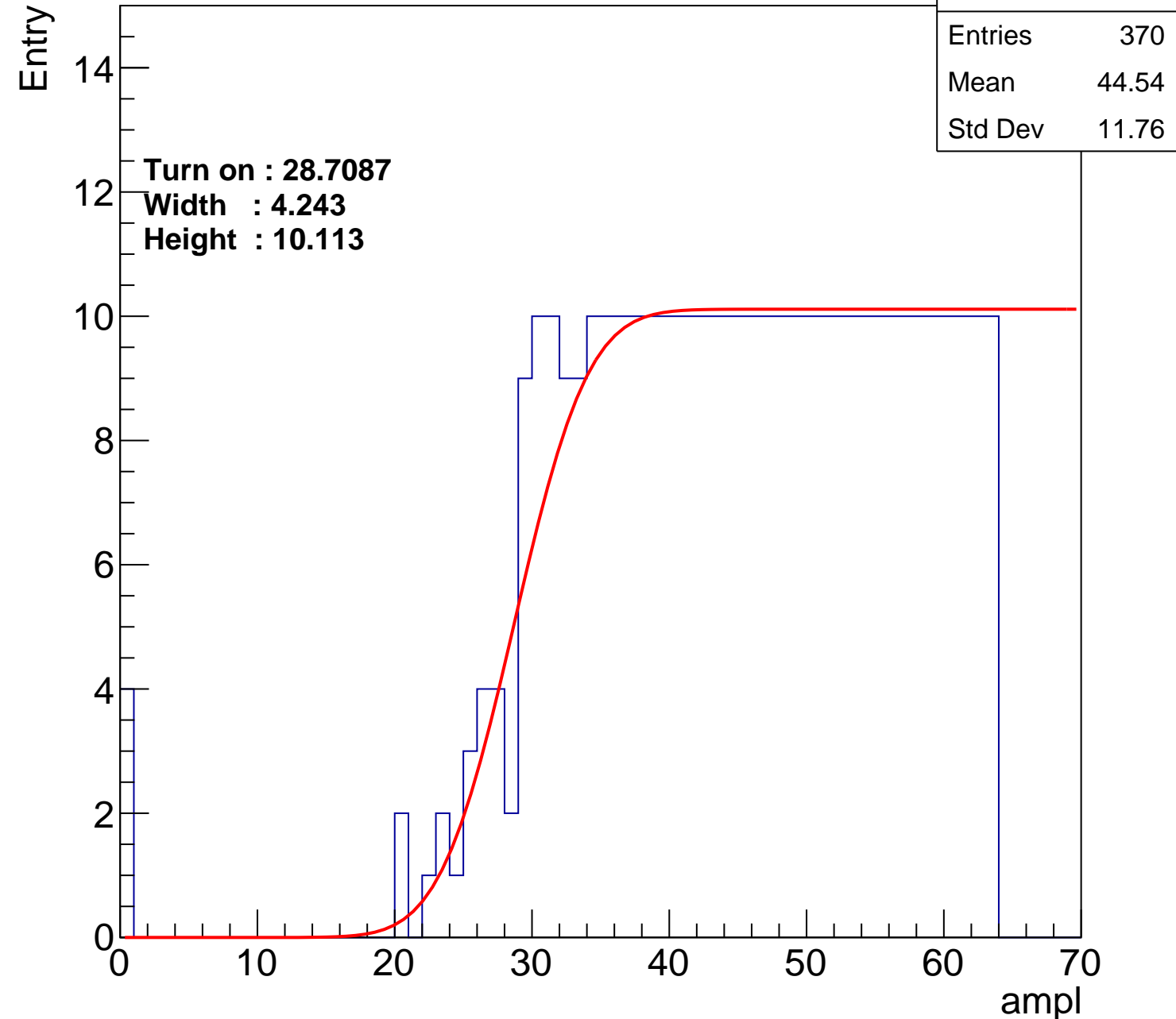
**Width : 4.243**

**Height : 10.113**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch123

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	361
Mean	45.16
Std Dev	11.1

**Turn on : 28.4580**

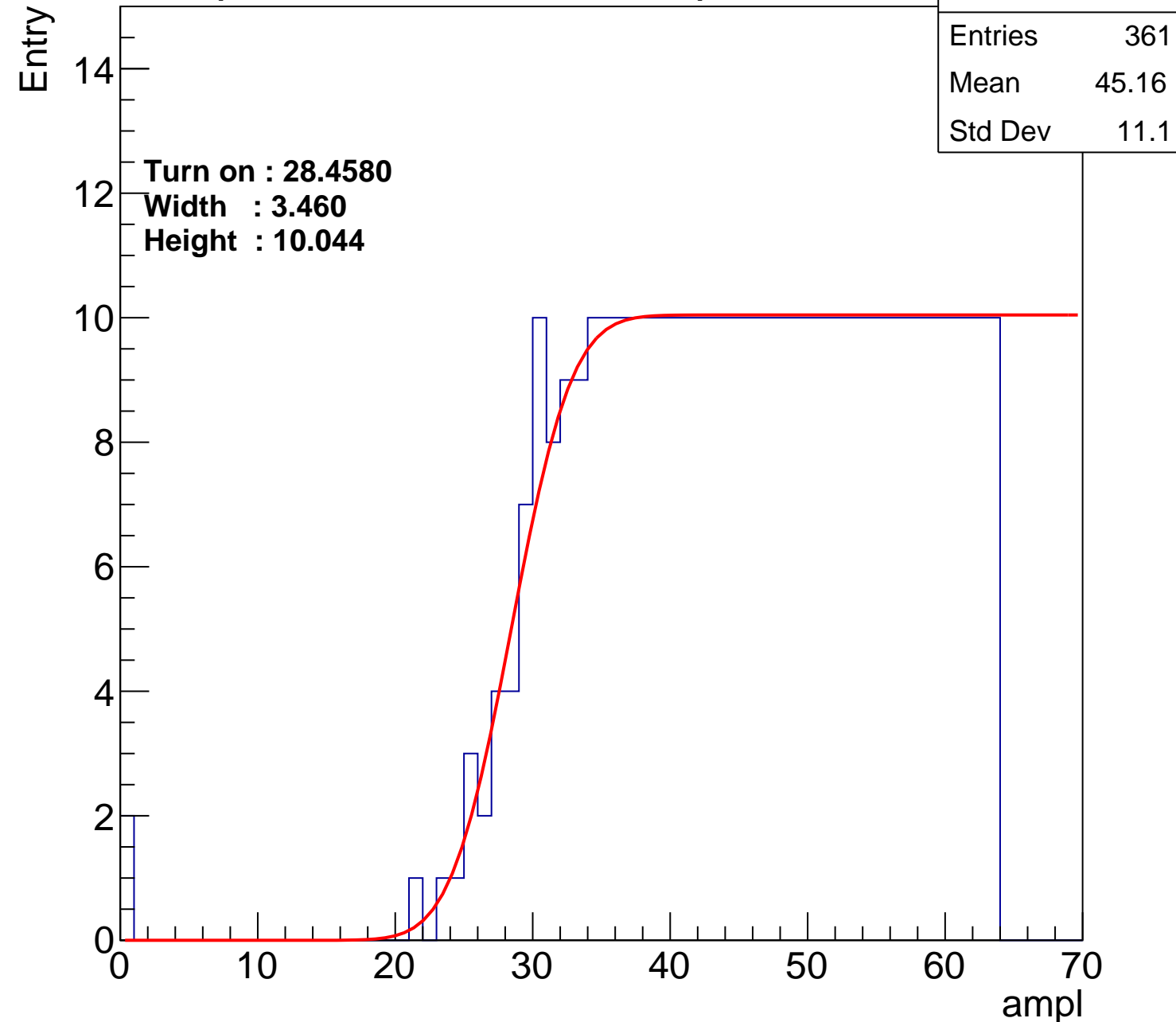
**Width : 3.460**

**Height : 10.044**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch124

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	367
Mean	44.83
Std Dev	11.31

Turn on : 27.6947

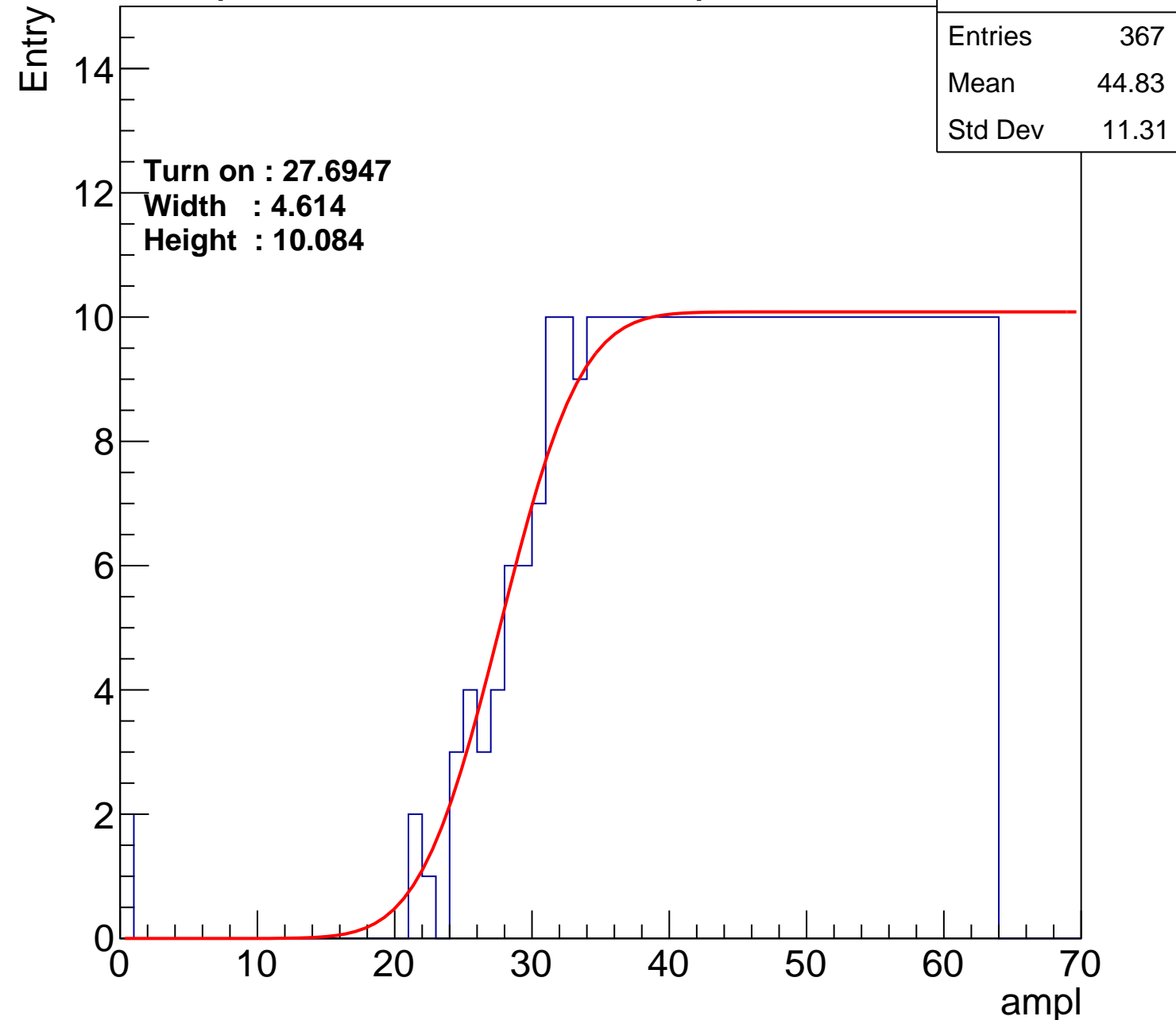
Width : 4.614

Height : 10.084

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch125

calib\_packv5\_042523\_0143.root, FC#4, port A2

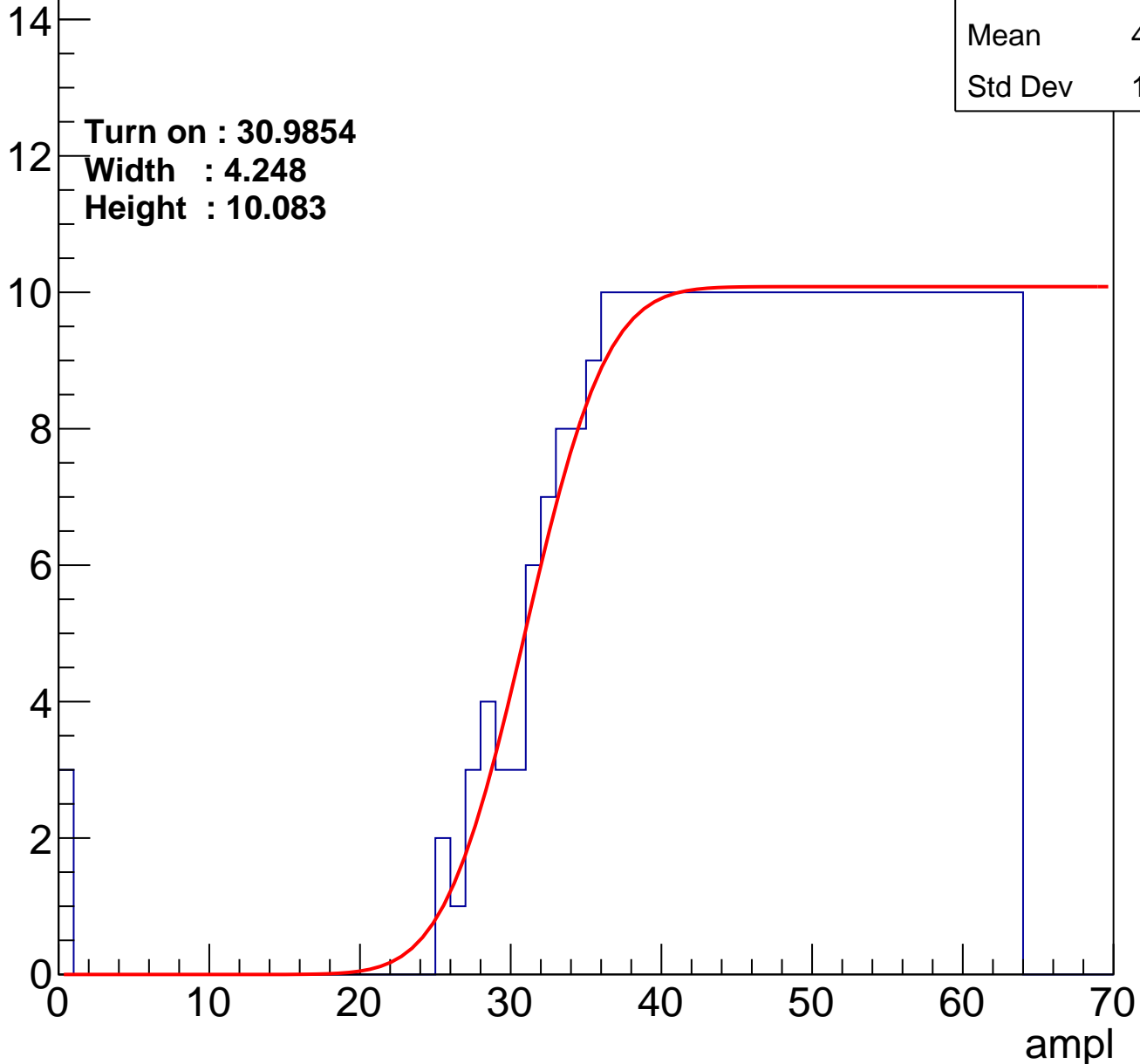
Entries	337
Mean	46.19
Std Dev	10.85

Turn on : 30.9854

Width : 4.248

Height : 10.083

Entry



# B1L100S, U13-ch126

calib\_packv5\_042523\_0143.root, FC#4, port A2

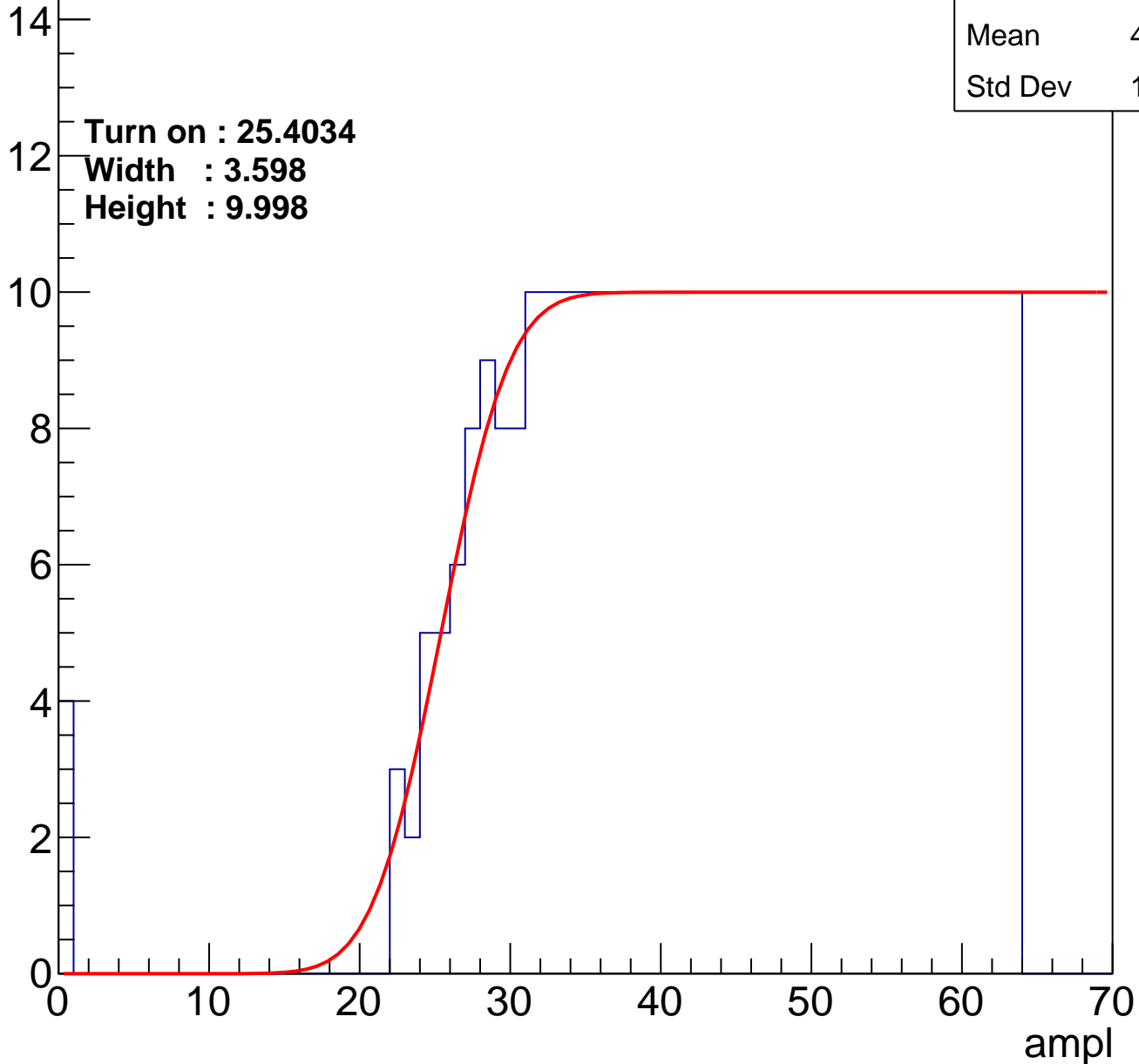
Entries	388
Mean	43.72
Std Dev	12.09

Turn on : 25.4034

Width : 3.598

Height : 9.998

Entry





# B1L100S, U13-ch127

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	369
Mean	44.85
Std Dev	11.06

Turn on : 27.4393

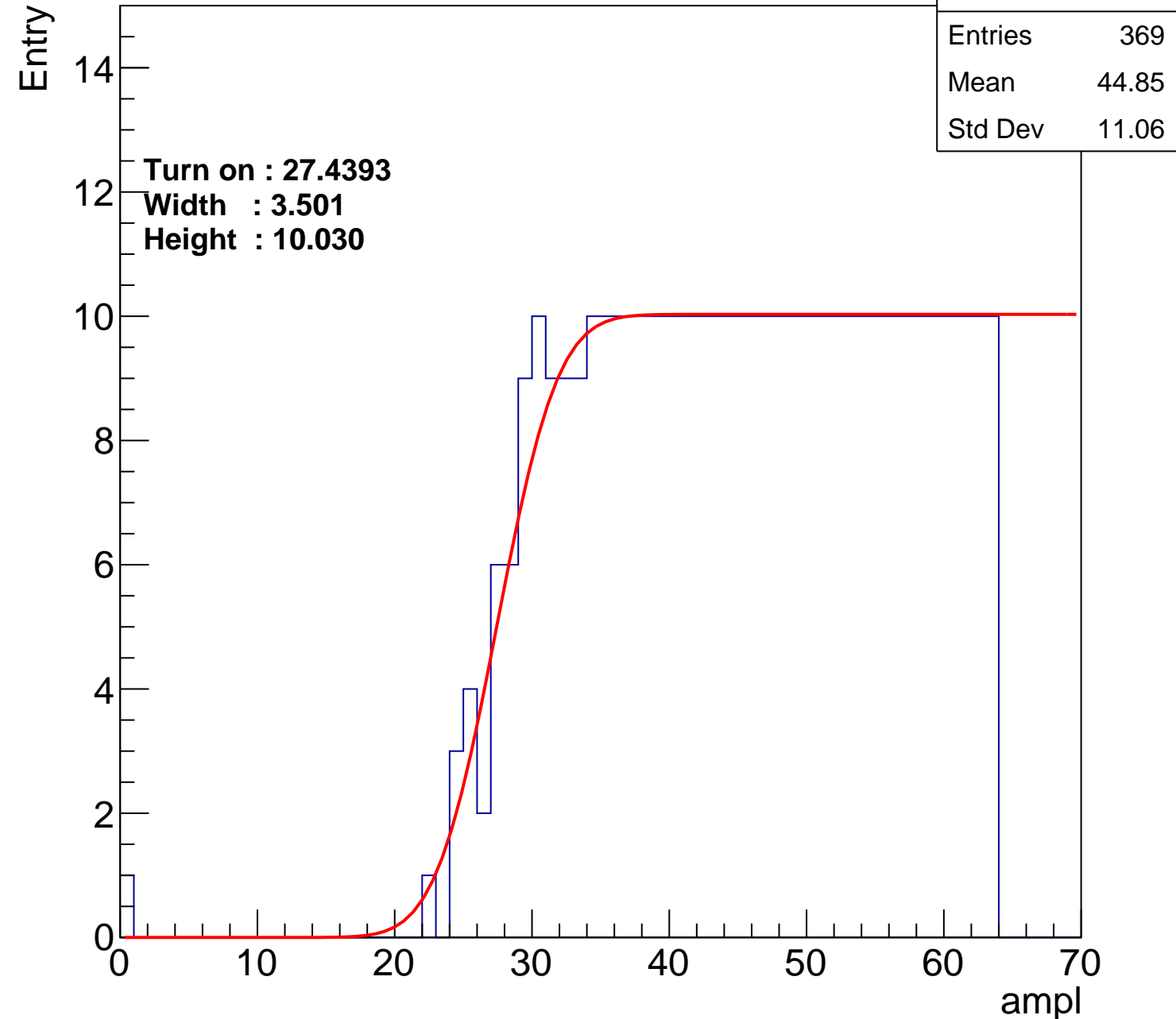
Width : 3.501

Height : 10.030

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L100S, U13-ch127

calib\_packv5\_042523\_0143.root, FC#4, port A2

Entries	369
Mean	44.85
Std Dev	11.06

Turn on : 27.4393

Width : 3.501

Height : 10.030

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

