



# B0L001S, U6-ch0, adc0

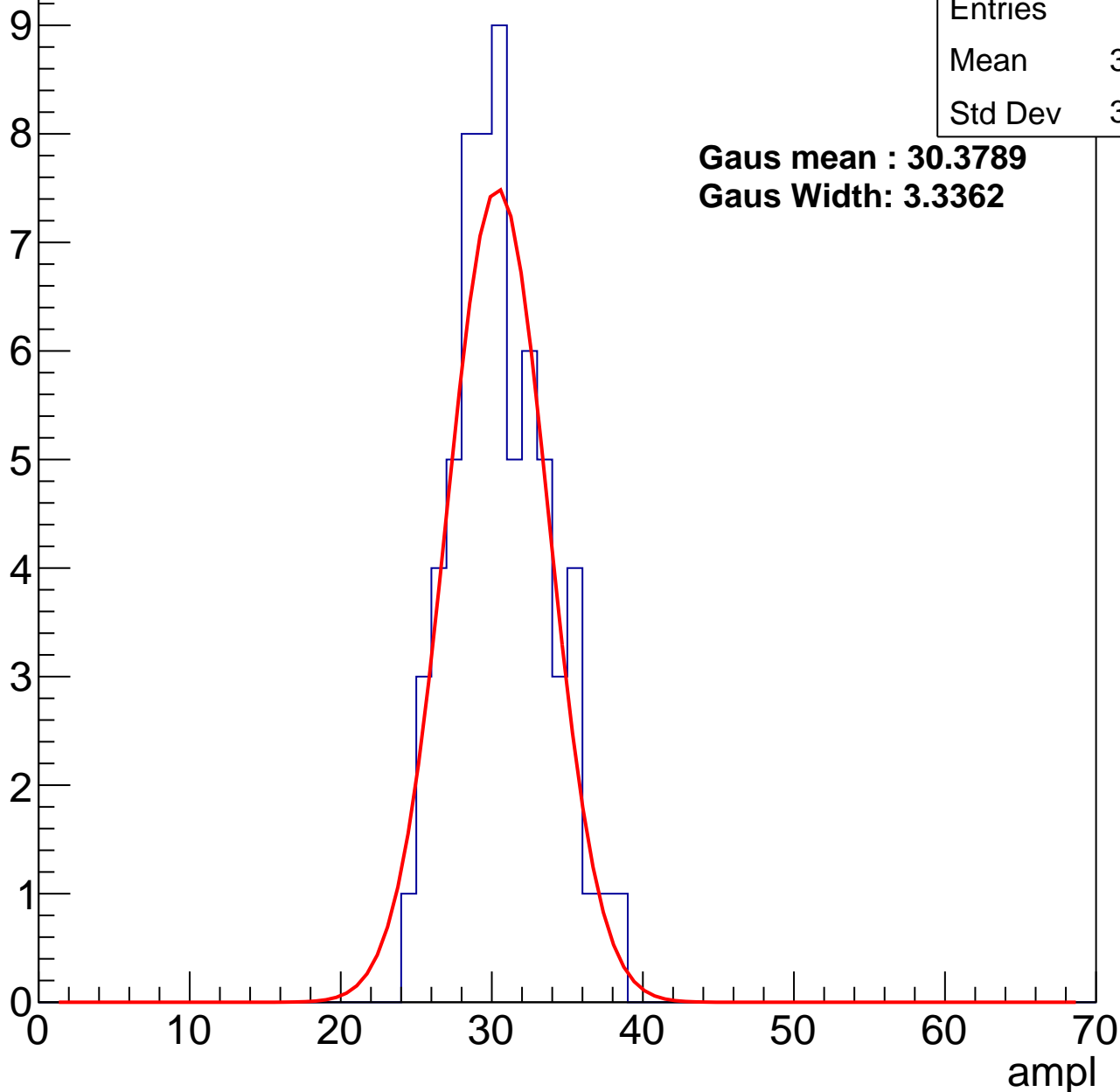
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	30.14
Std Dev	3.137

**Gaus mean : 30.3789**

**Gaus Width: 3.3362**



# B0L001S, U6-ch0, adc1

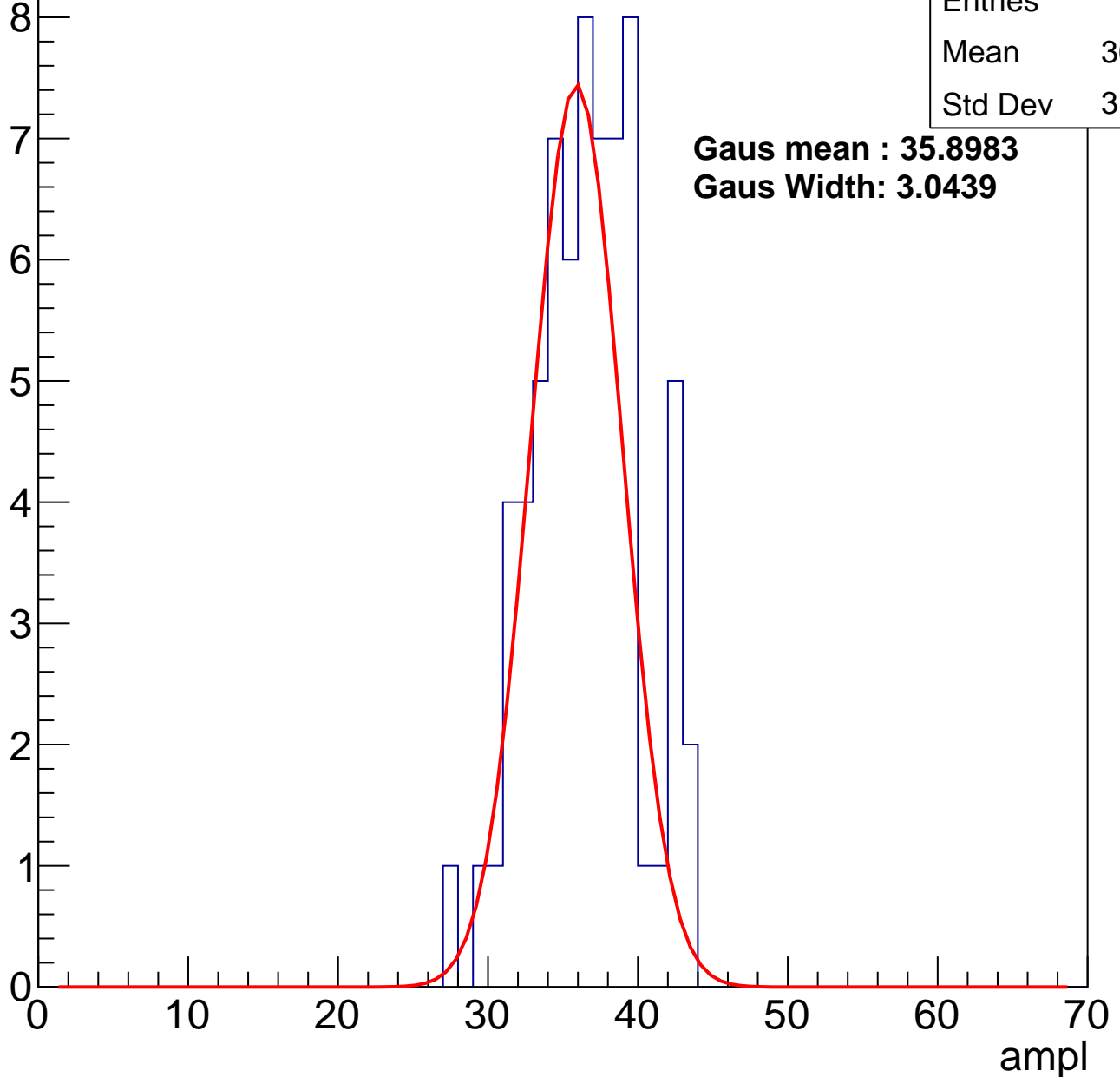
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	36.07
Std Dev	3.503

**Gaus mean : 35.8983**

**Gaus Width: 3.0439**



# B0L001S, U6-ch0, adc2

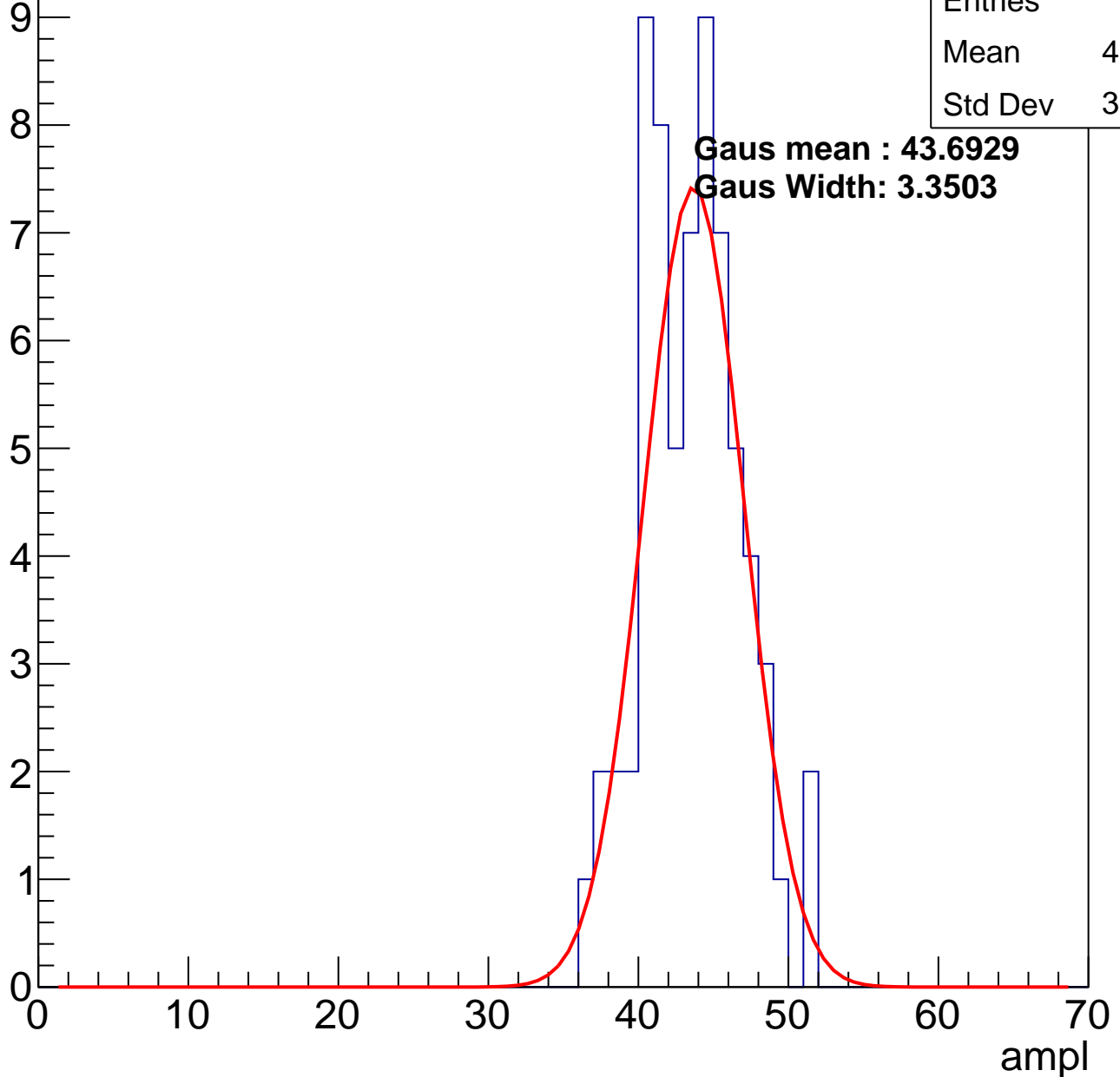
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	43.09
Std Dev	3.245

**Gaus mean : 43.6929**

**Gaus Width: 3.3503**

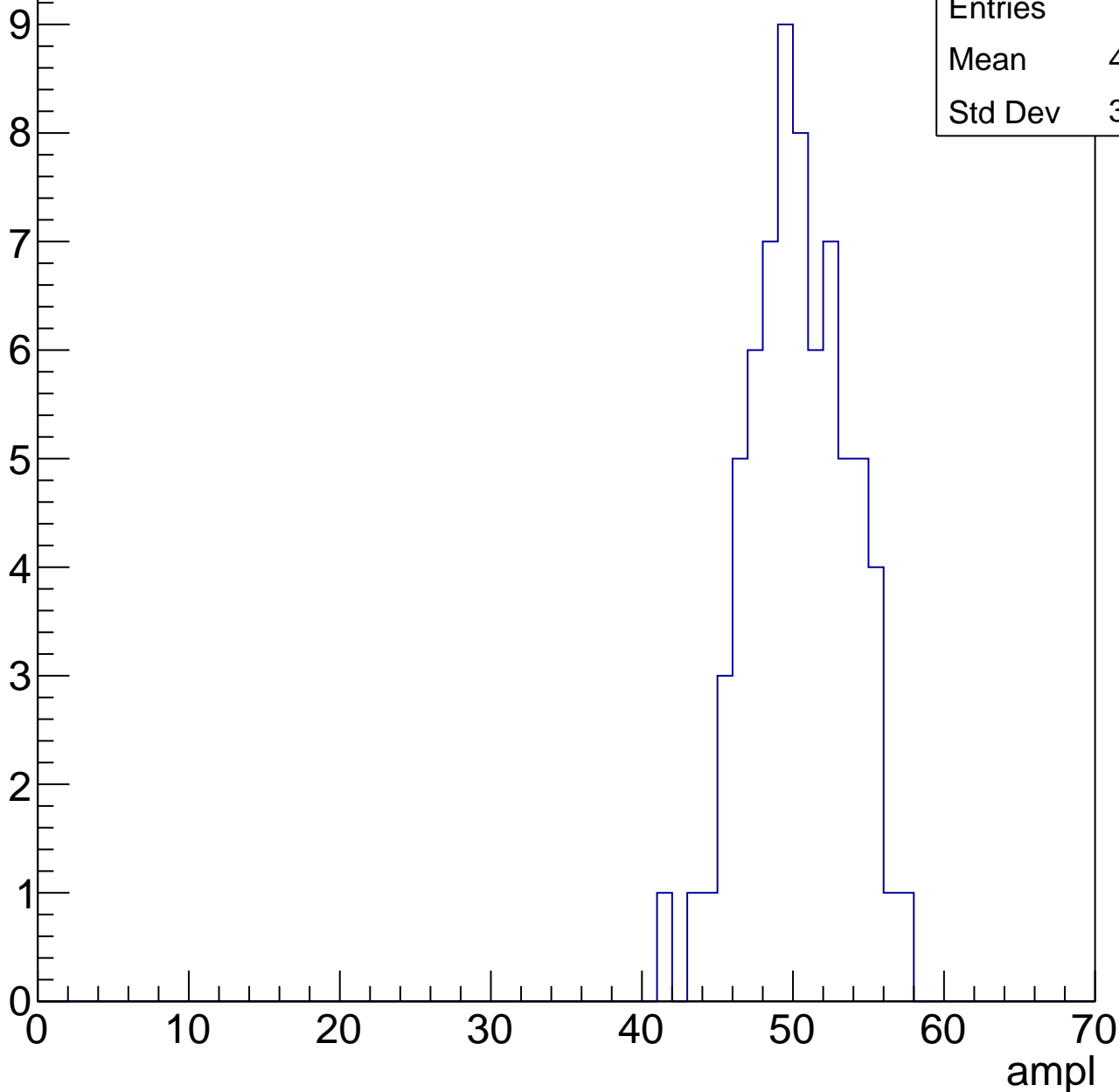


# B0L001S, U6-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

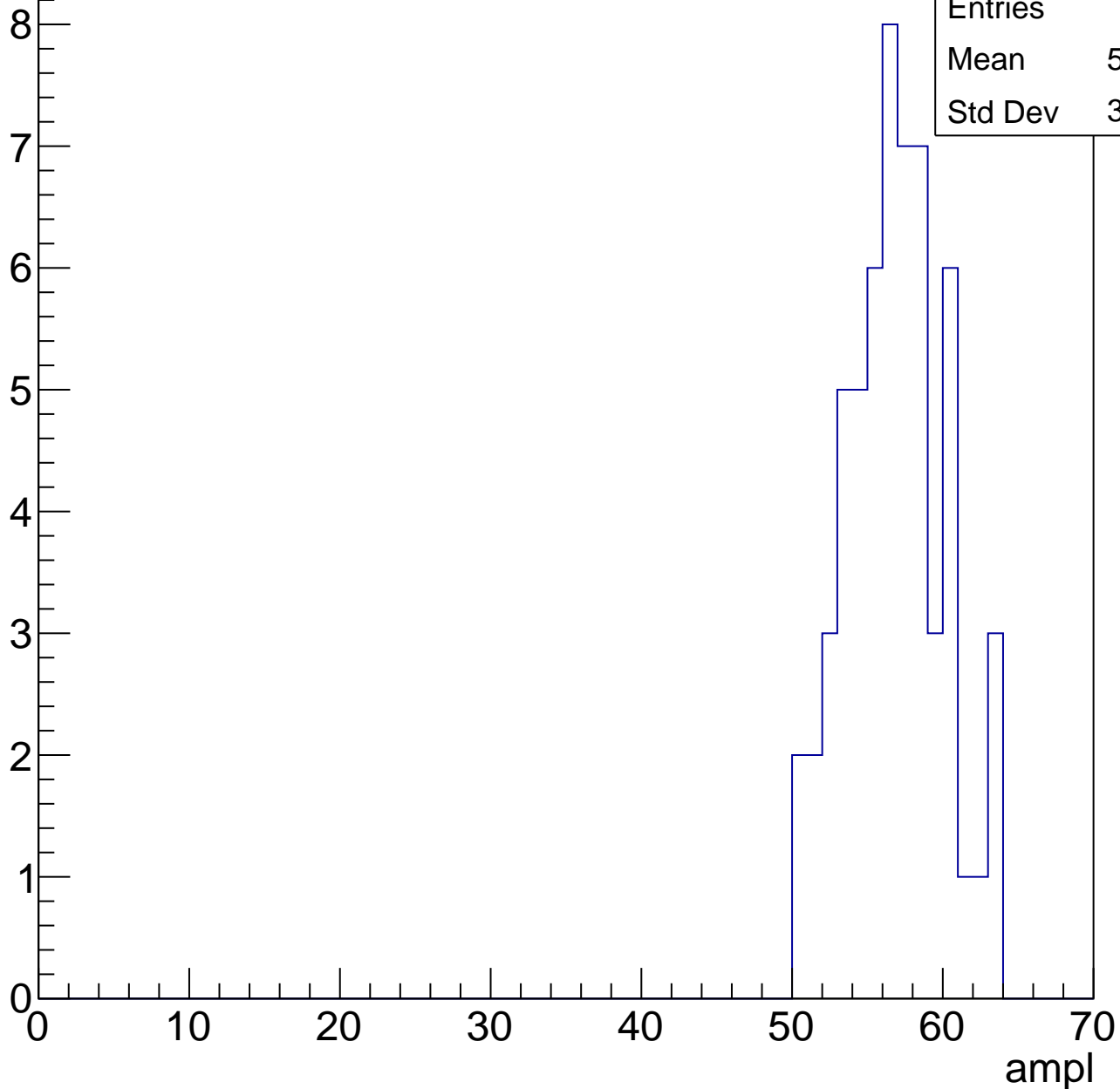
Entries	70
Mean	49.86
Std Dev	3.283



# B0L001S, U6-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

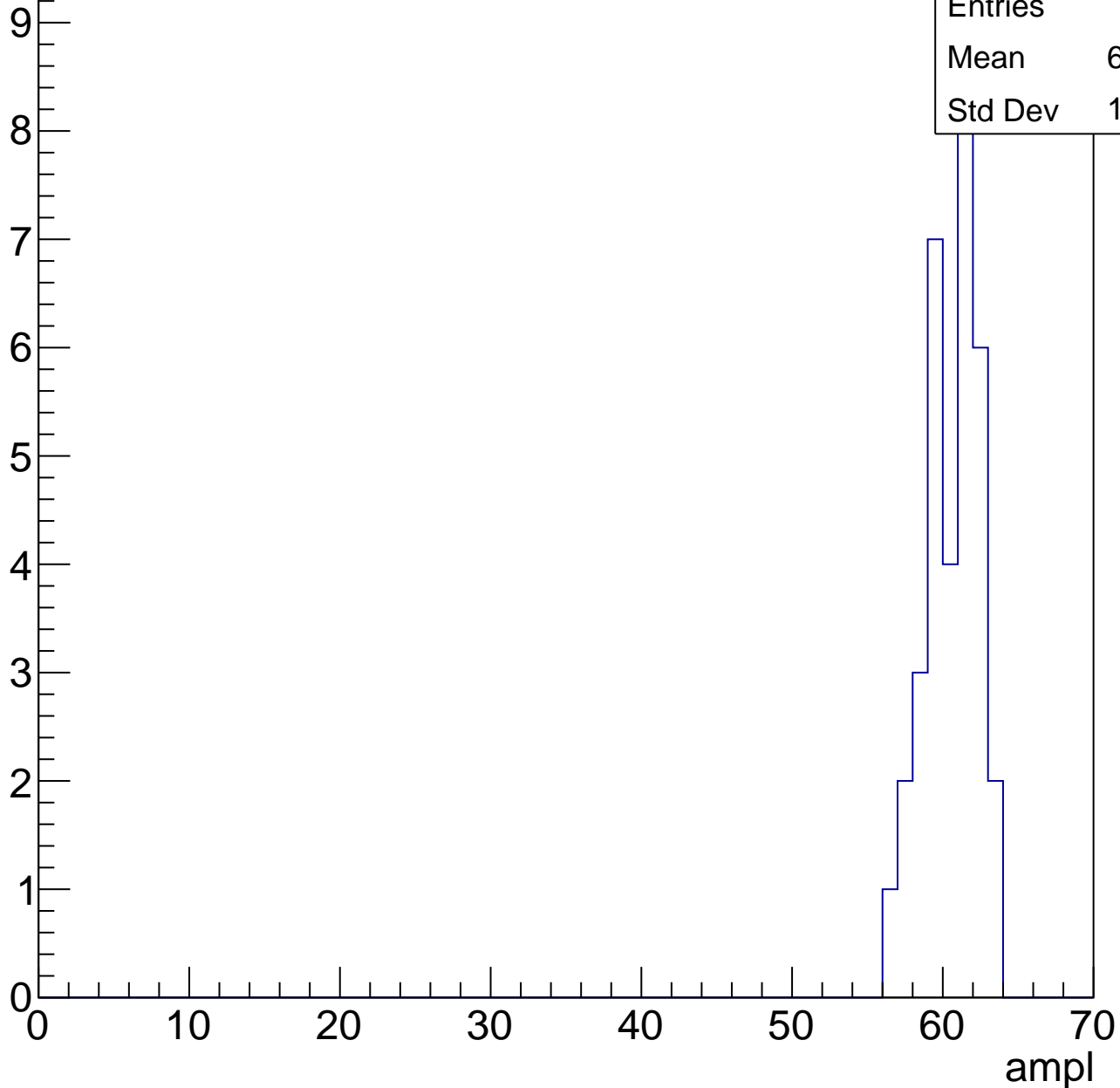


Entries	59
Mean	56.36
Std Dev	3.188

# B0L001S, U6-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

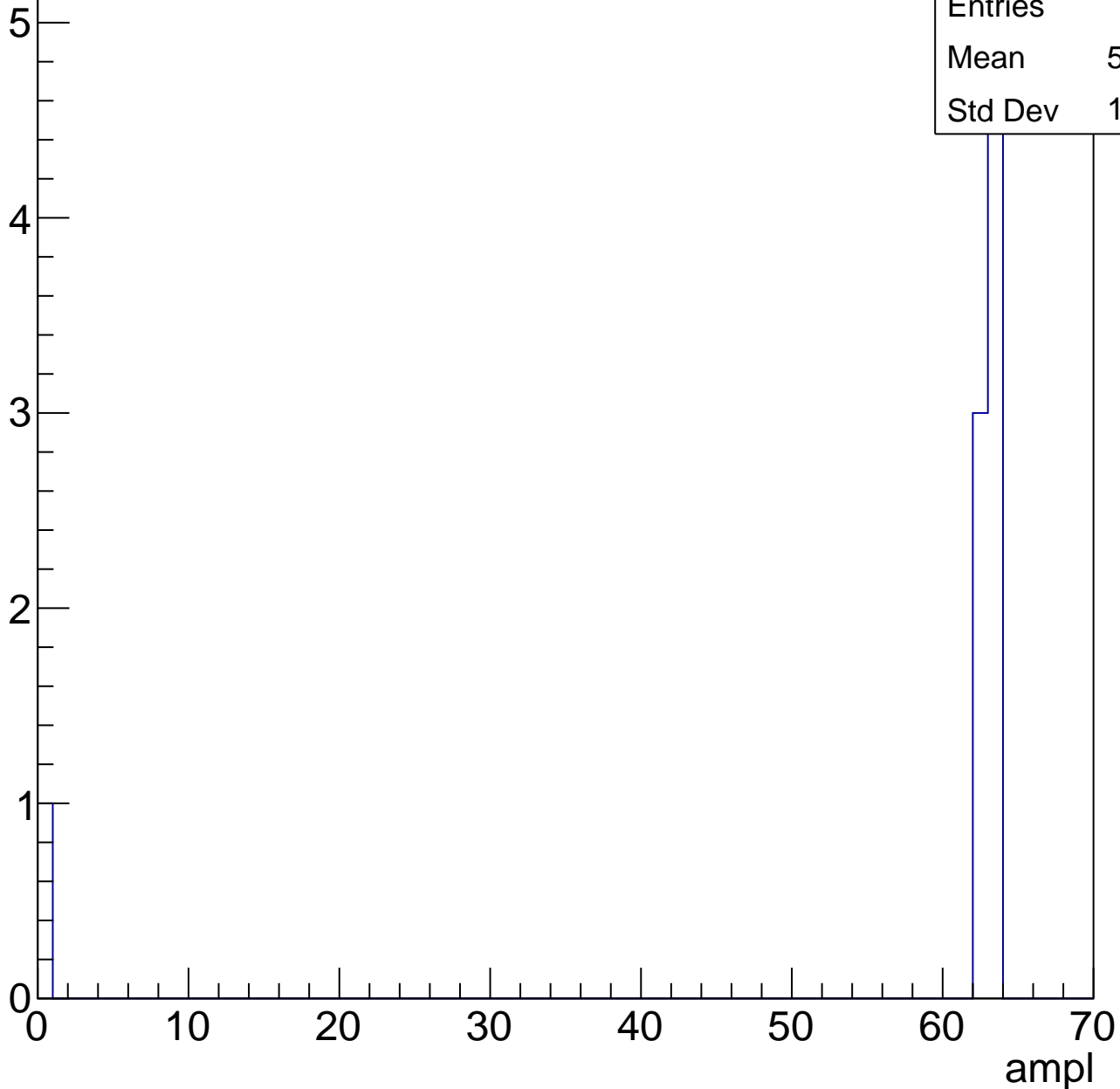


# B0L001S, U6-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	9
Mean	55.67
Std Dev	19.69





# B0L001S, U6-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U6-ch1, adc0

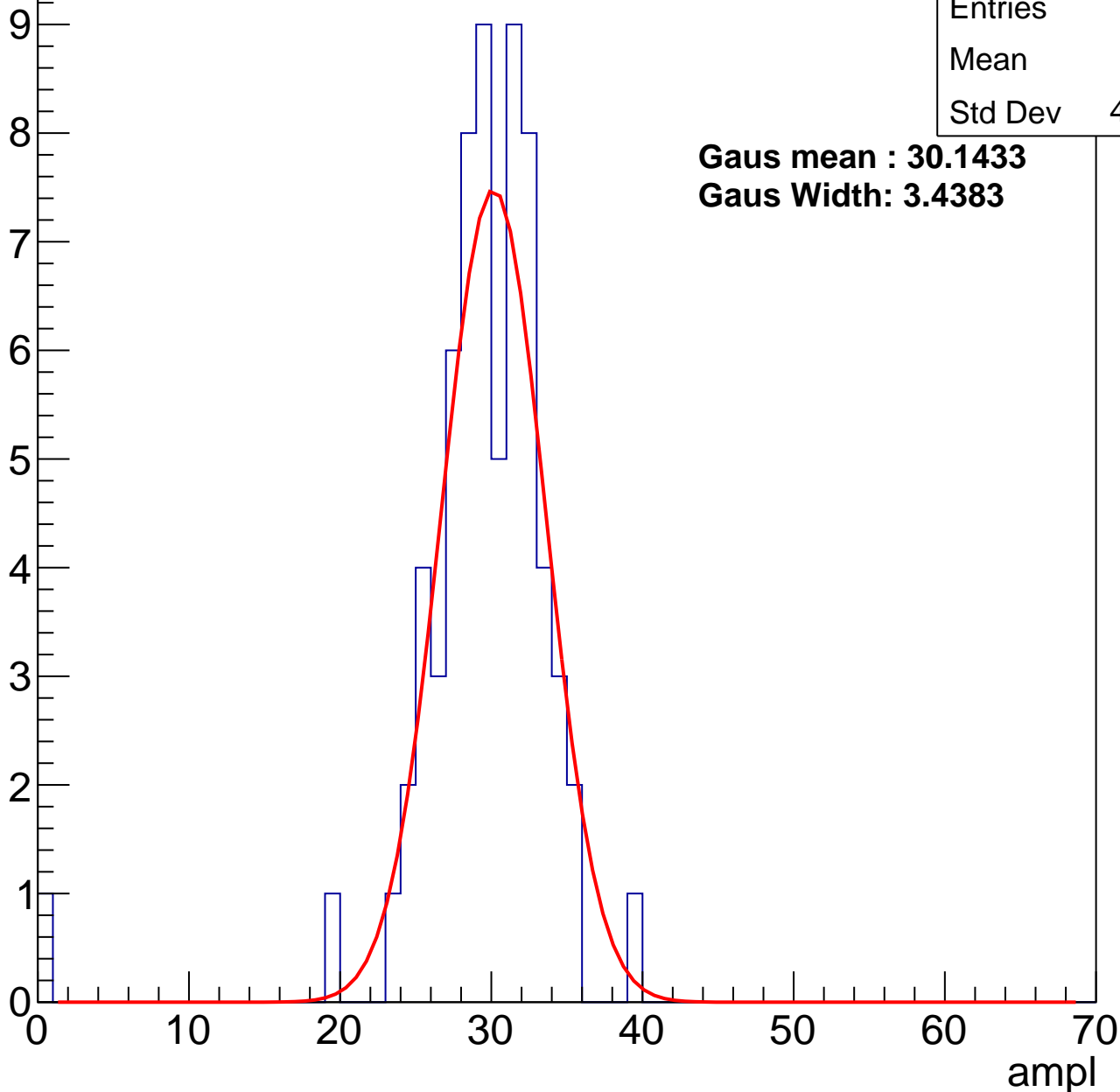
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	29
Std Dev	4.847

**Gaus mean : 30.1433**

**Gaus Width: 3.4383**

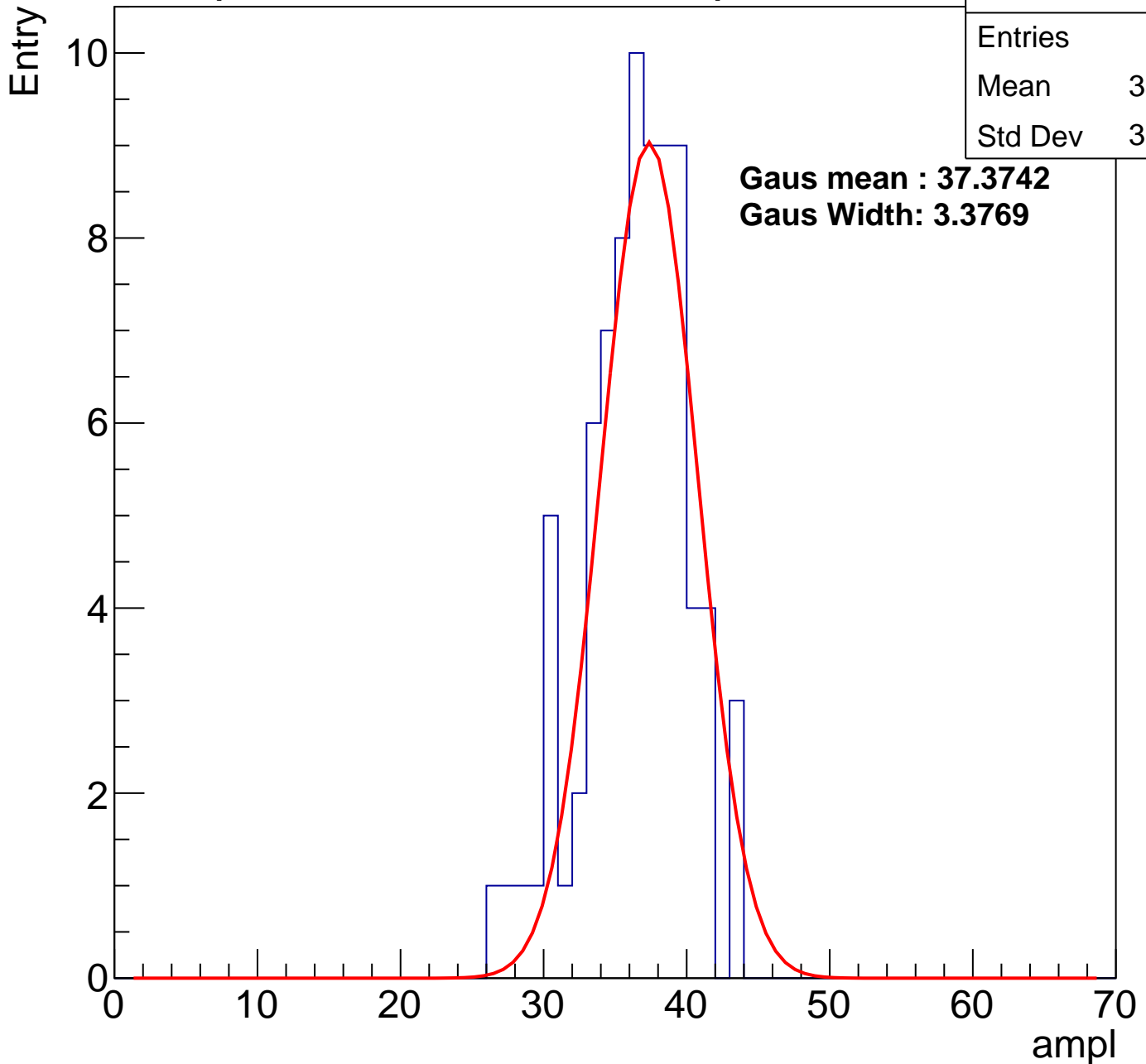


# B0L001S, U6-ch1, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	81
Mean	35.93
Std Dev	3.613

**Gaus mean : 37.3742**  
**Gaus Width: 3.3769**



# B0L001S, U6-ch1, adc2

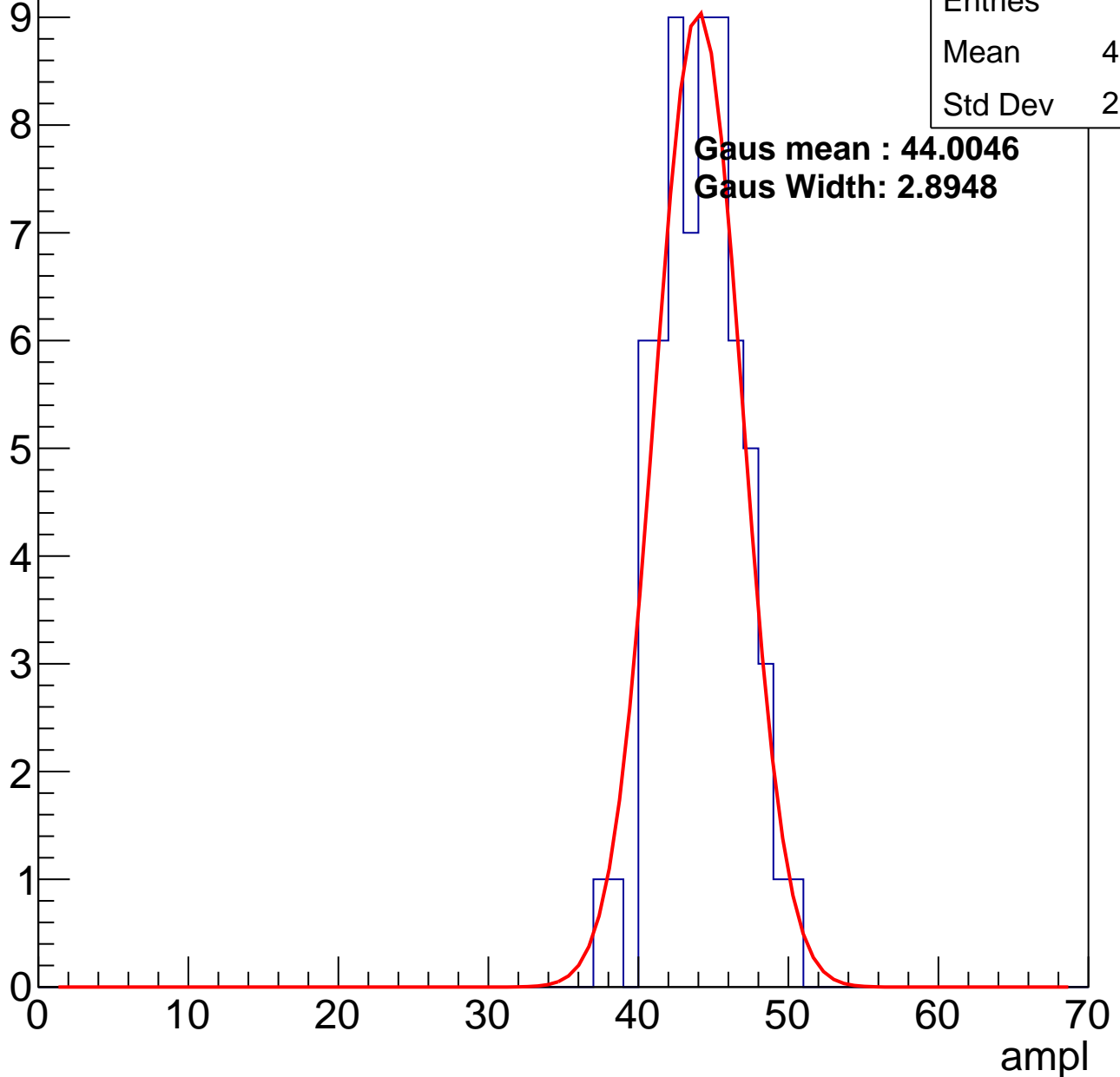
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	43.67
Std Dev	2.675

**Gaus mean : 44.0046**

**Gaus Width: 2.8948**

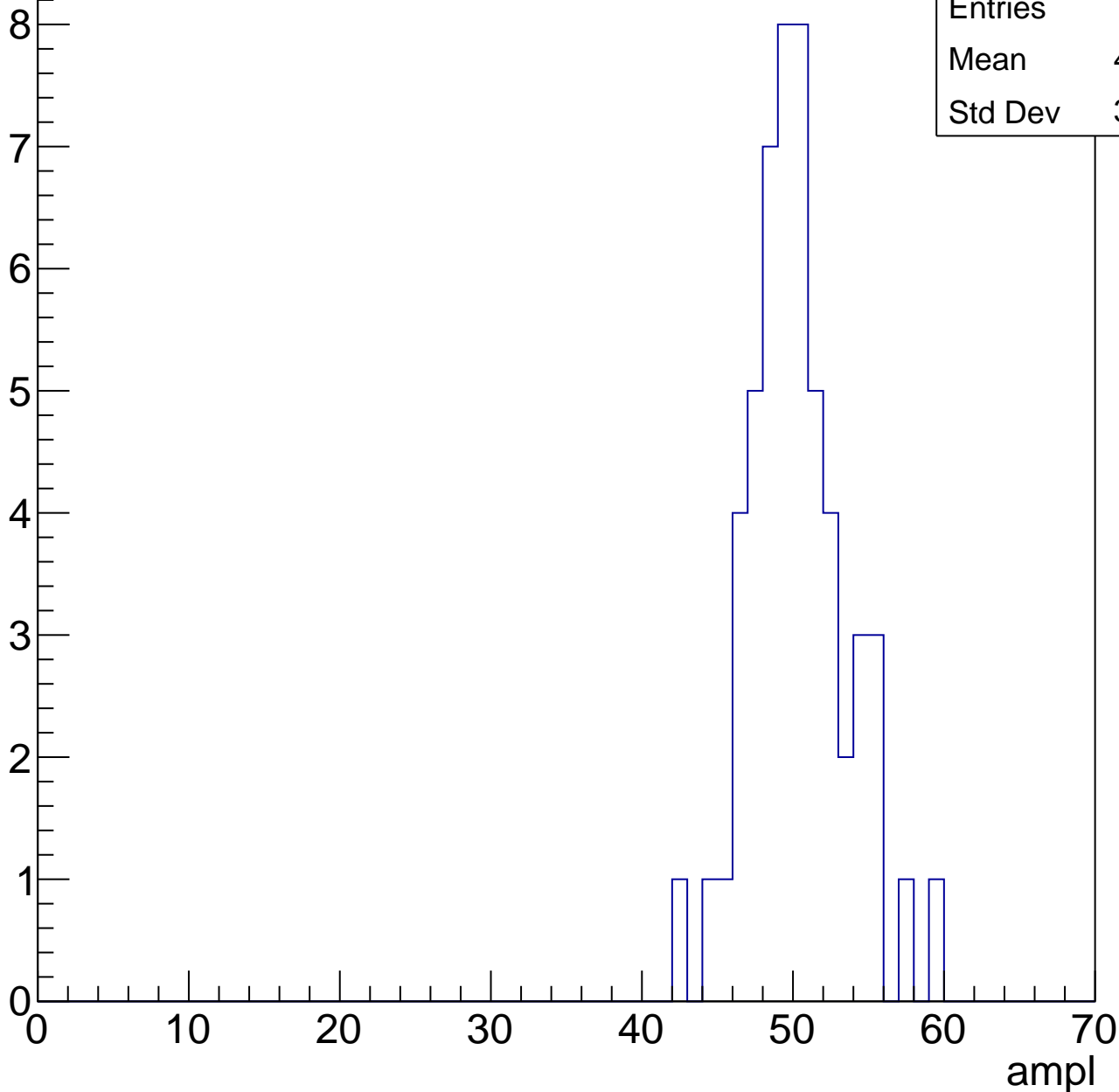


# B0L001S, U6-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

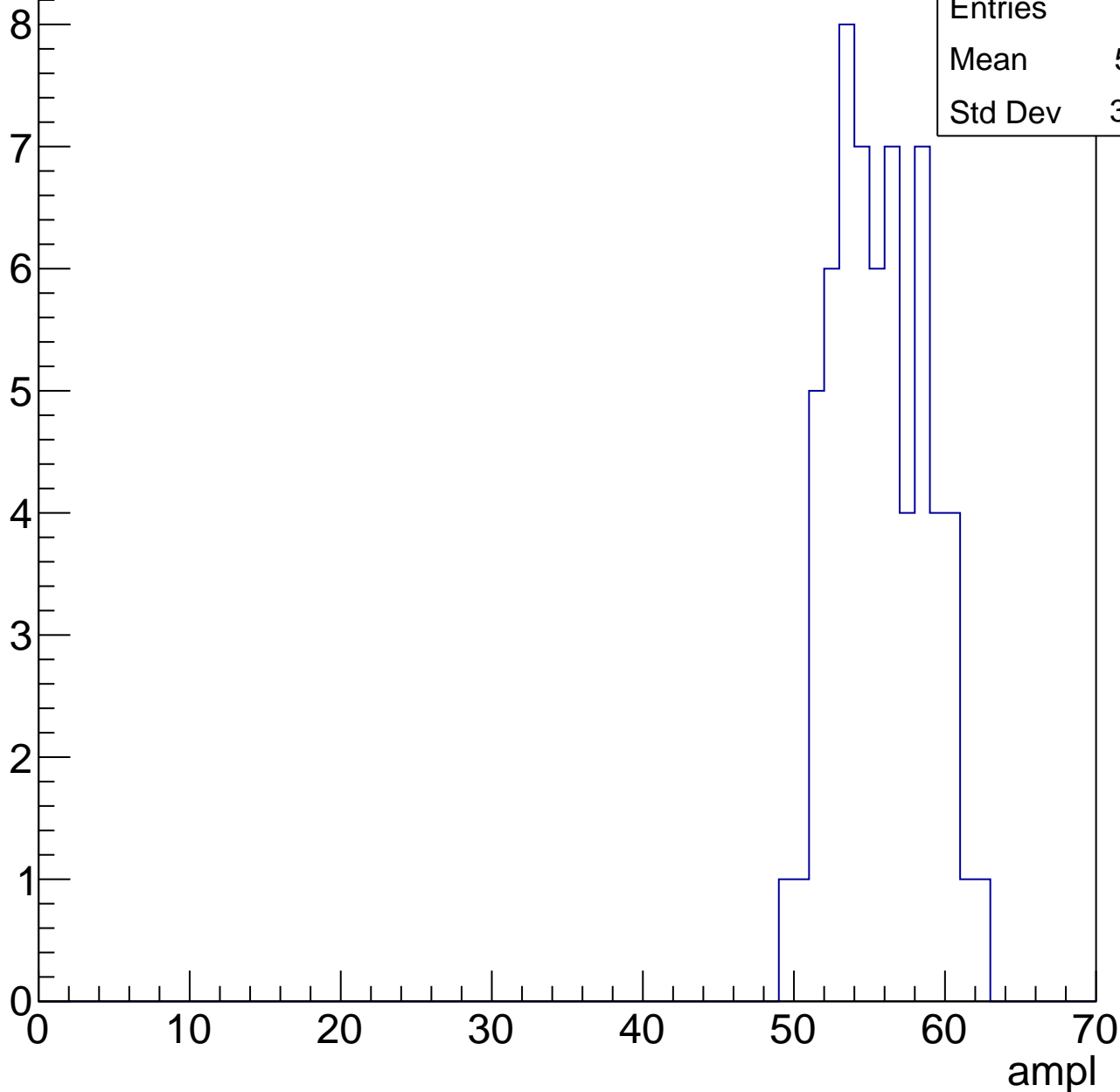
Entries	54
Mean	49.81
Std Dev	3.221



# B0L001S, U6-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

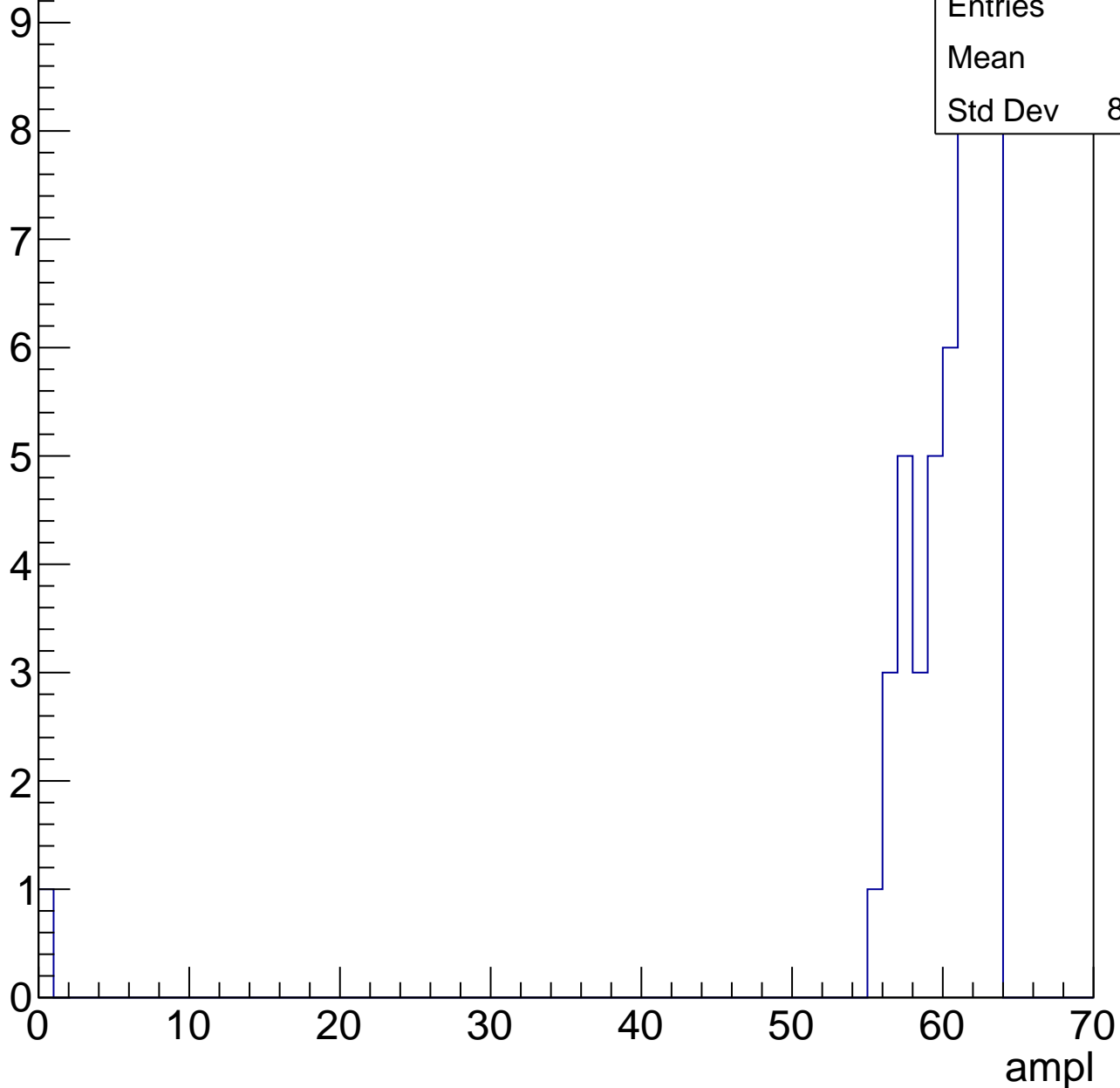


Entries	62
Mean	55.21
Std Dev	3.022

# B0L001S, U6-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



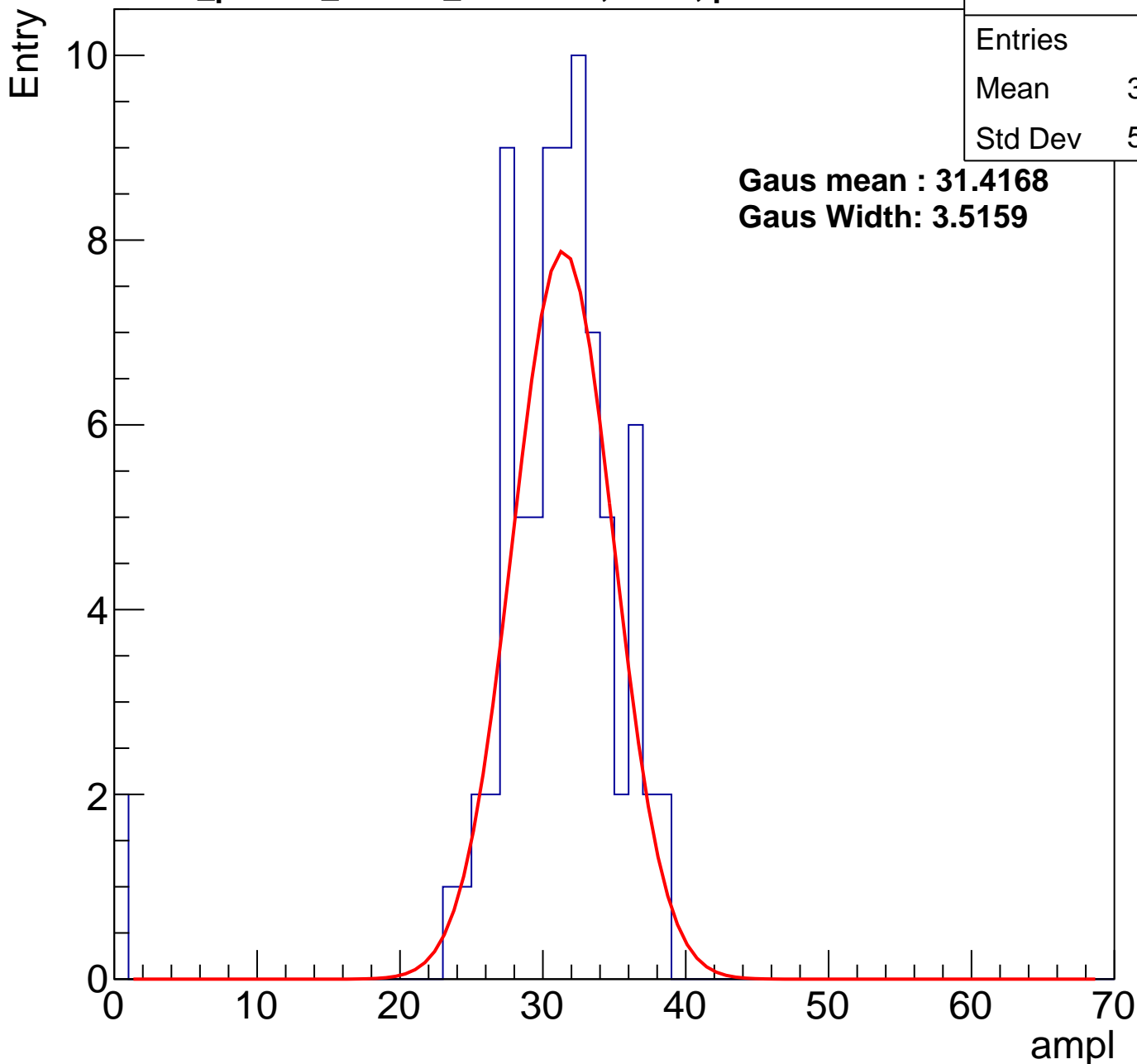
# B0L001S, U6-ch2, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	79
Mean	30.16
Std Dev	5.905

**Gaus mean : 31.4168**

**Gaus Width: 3.5159**



# B0L001S, U6-ch2, adc1

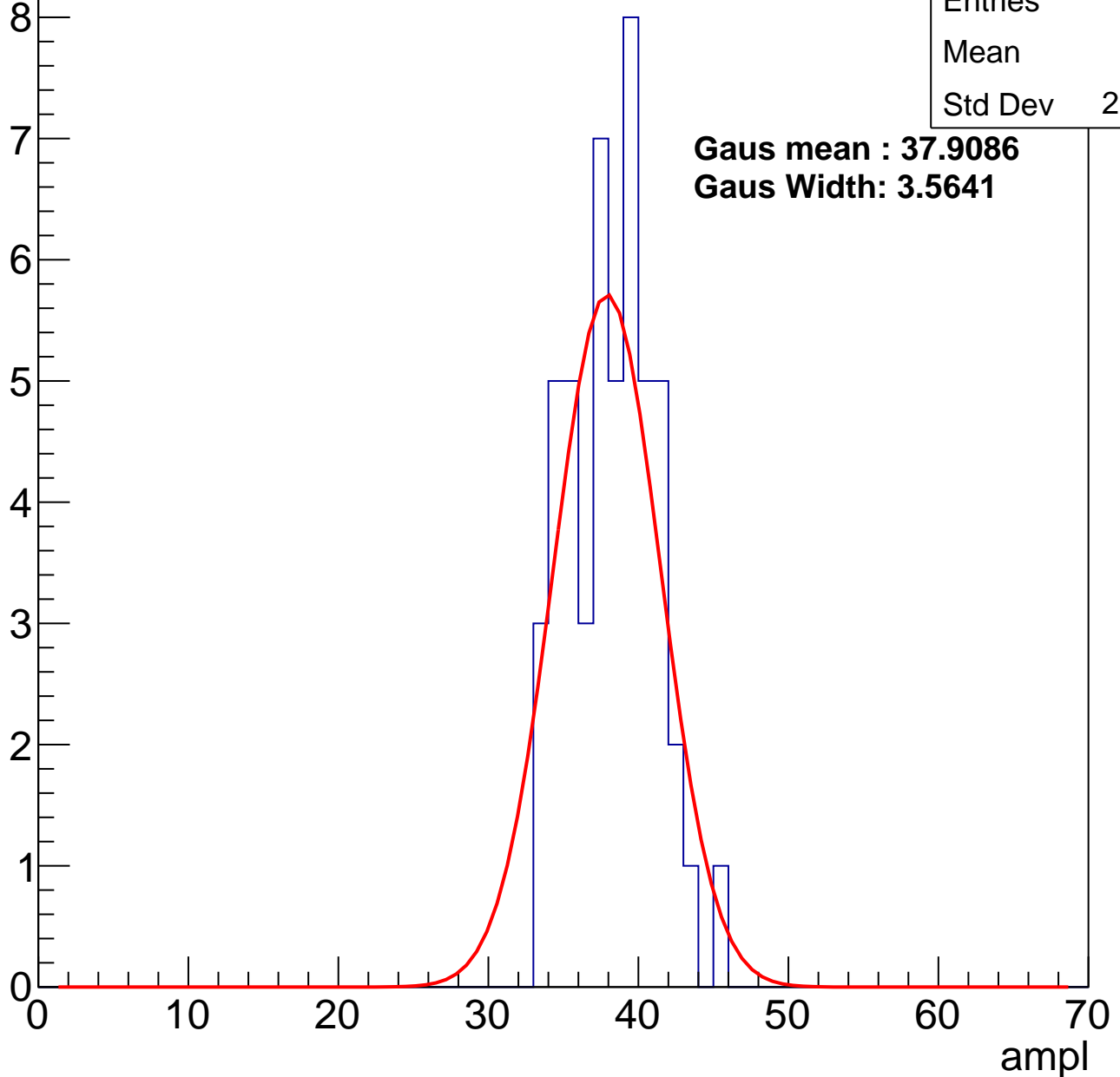
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	37.8
Std Dev	2.814

**Gaus mean : 37.9086**

**Gaus Width: 3.5641**



# B0L001S, U6-ch2, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	66
Mean	42.98
Std Dev	3.57

**Gaus mean : 43.9635**

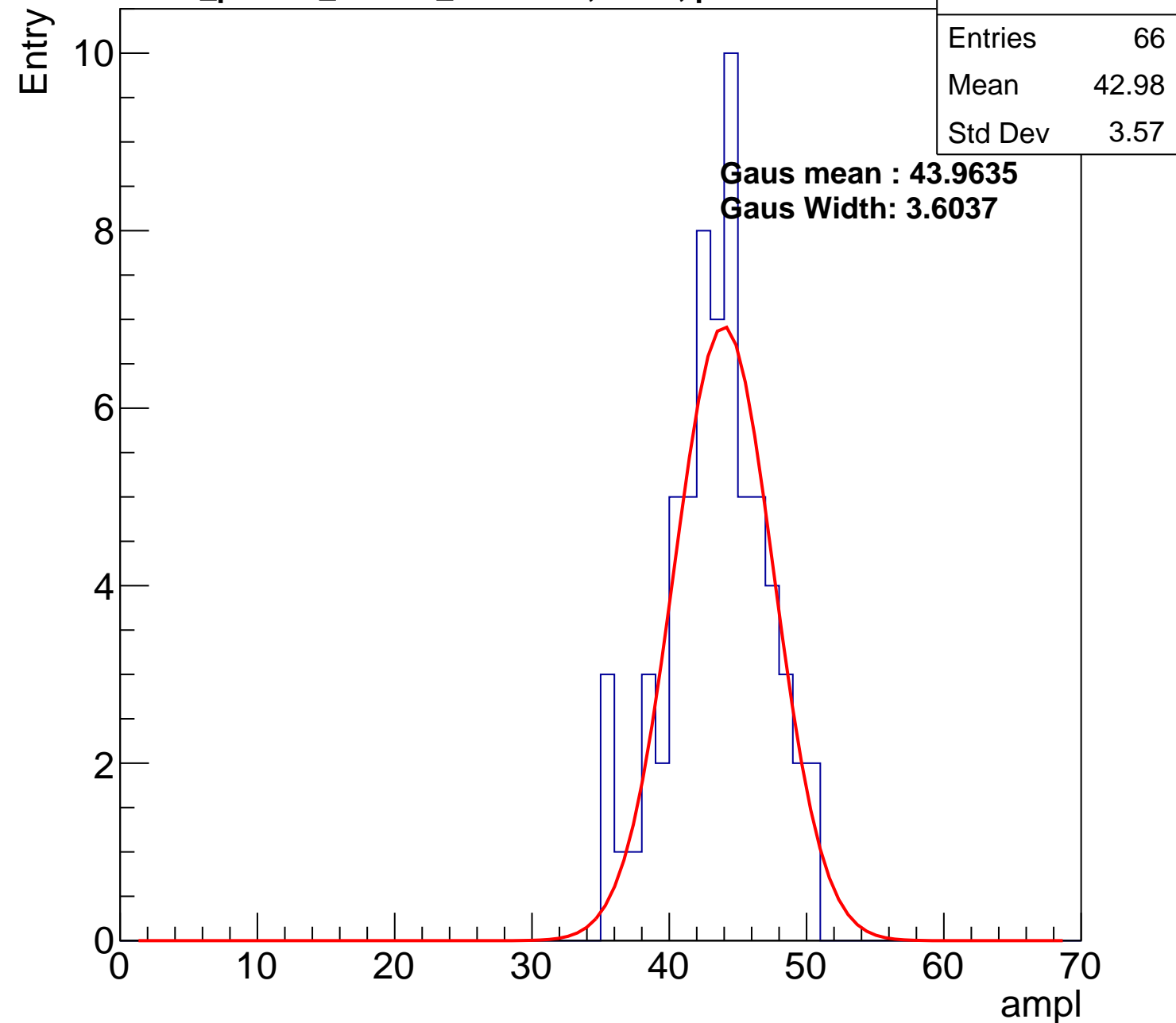
**Gaus Width: 3.6037**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

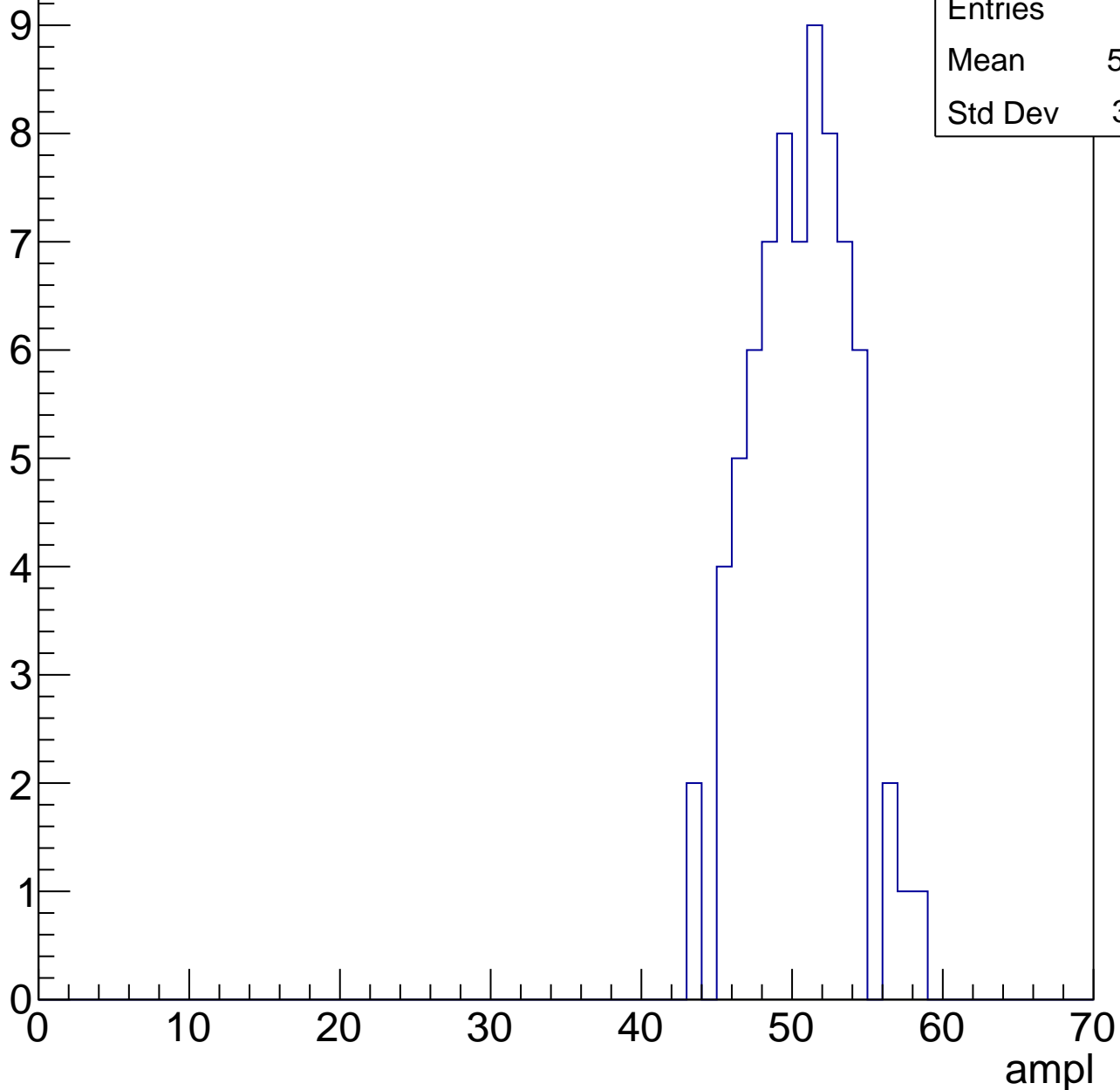


# B0L001S, U6-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

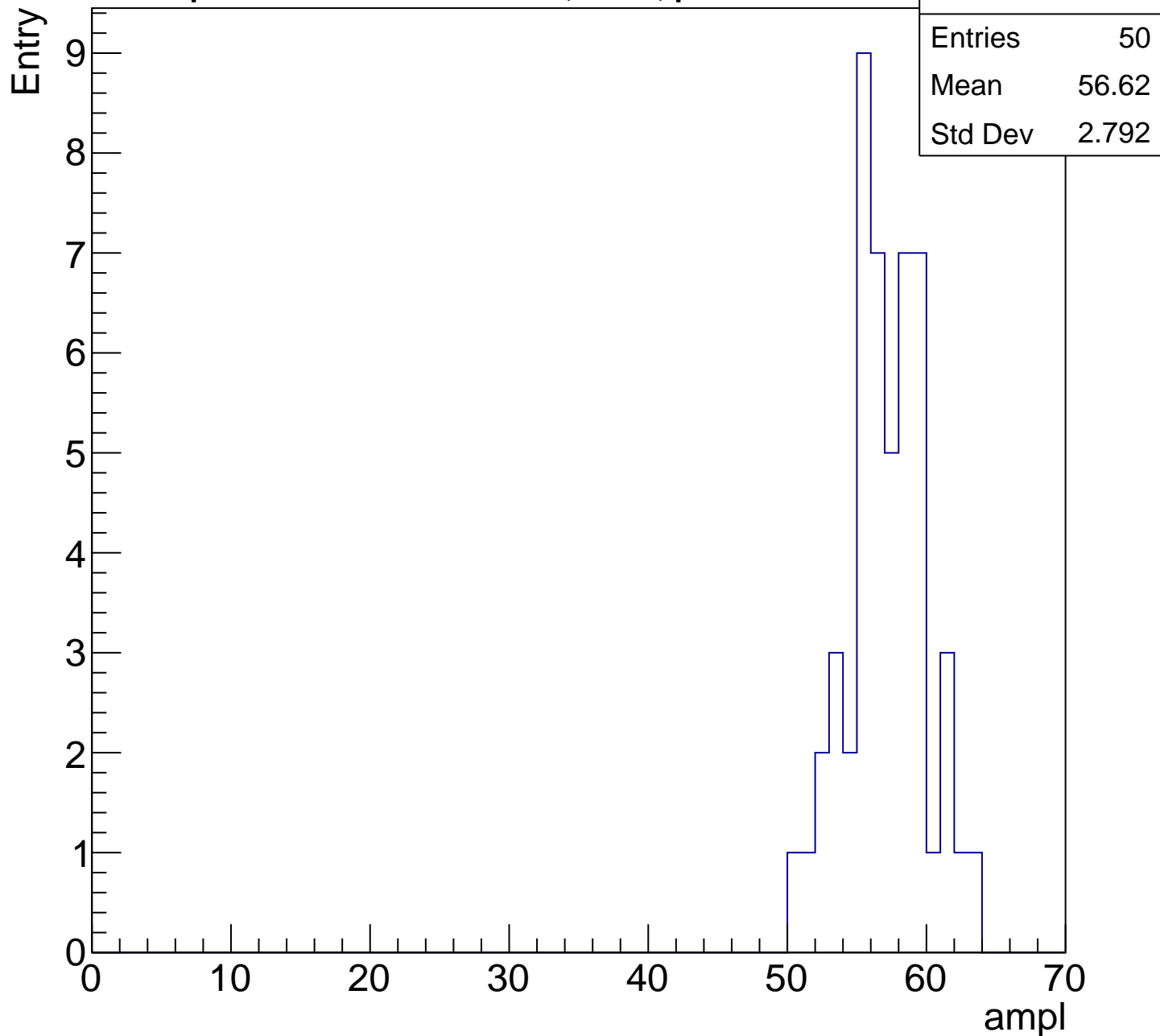
Entry

Entries	73
Mean	50.04
Std Dev	3.211



# B0L001S, U6-ch2, adc4

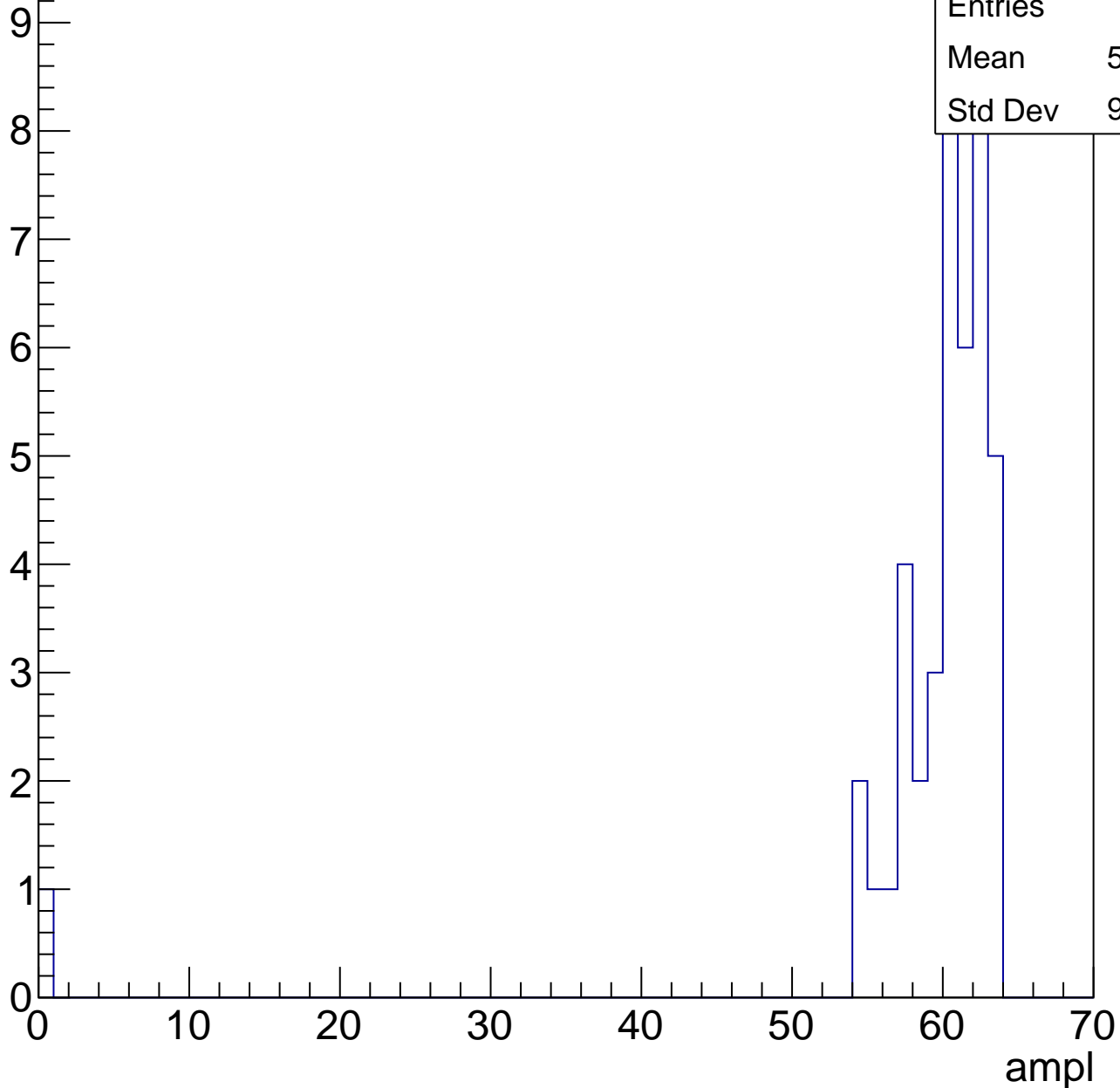
calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U6-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

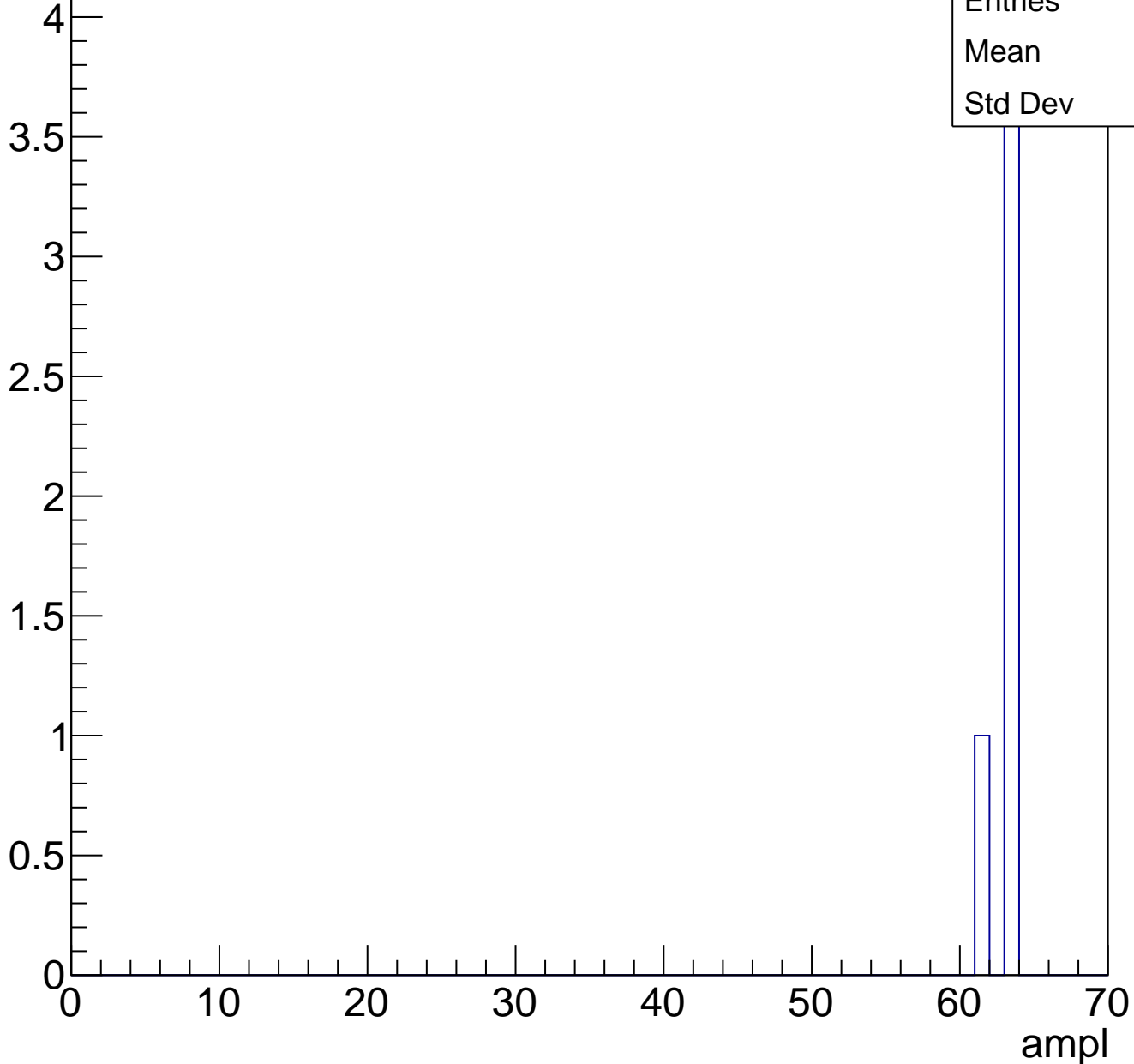
Entry



# B0L001S, U6-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

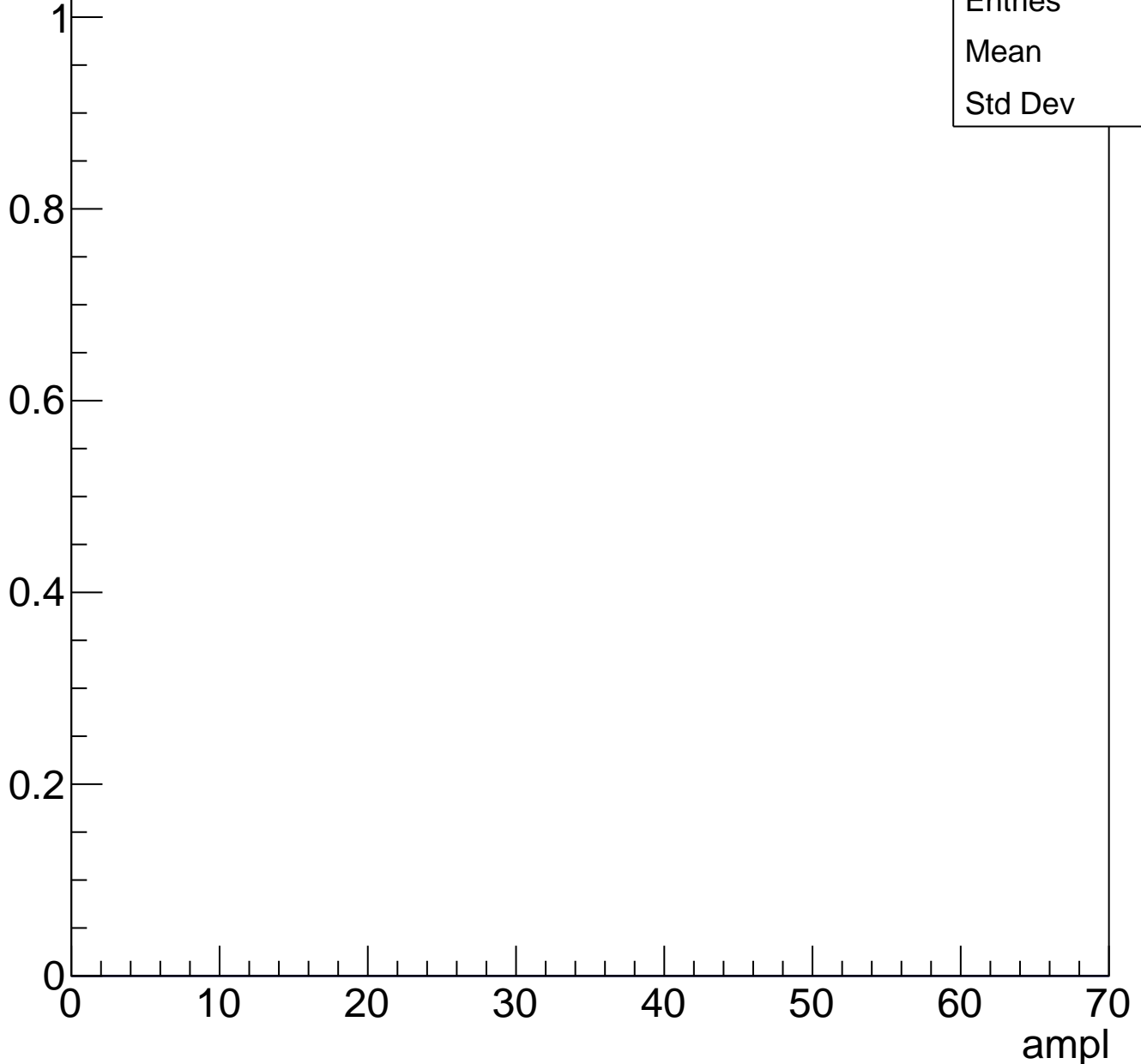




# B0L001S, U6-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U6-ch3, adc0

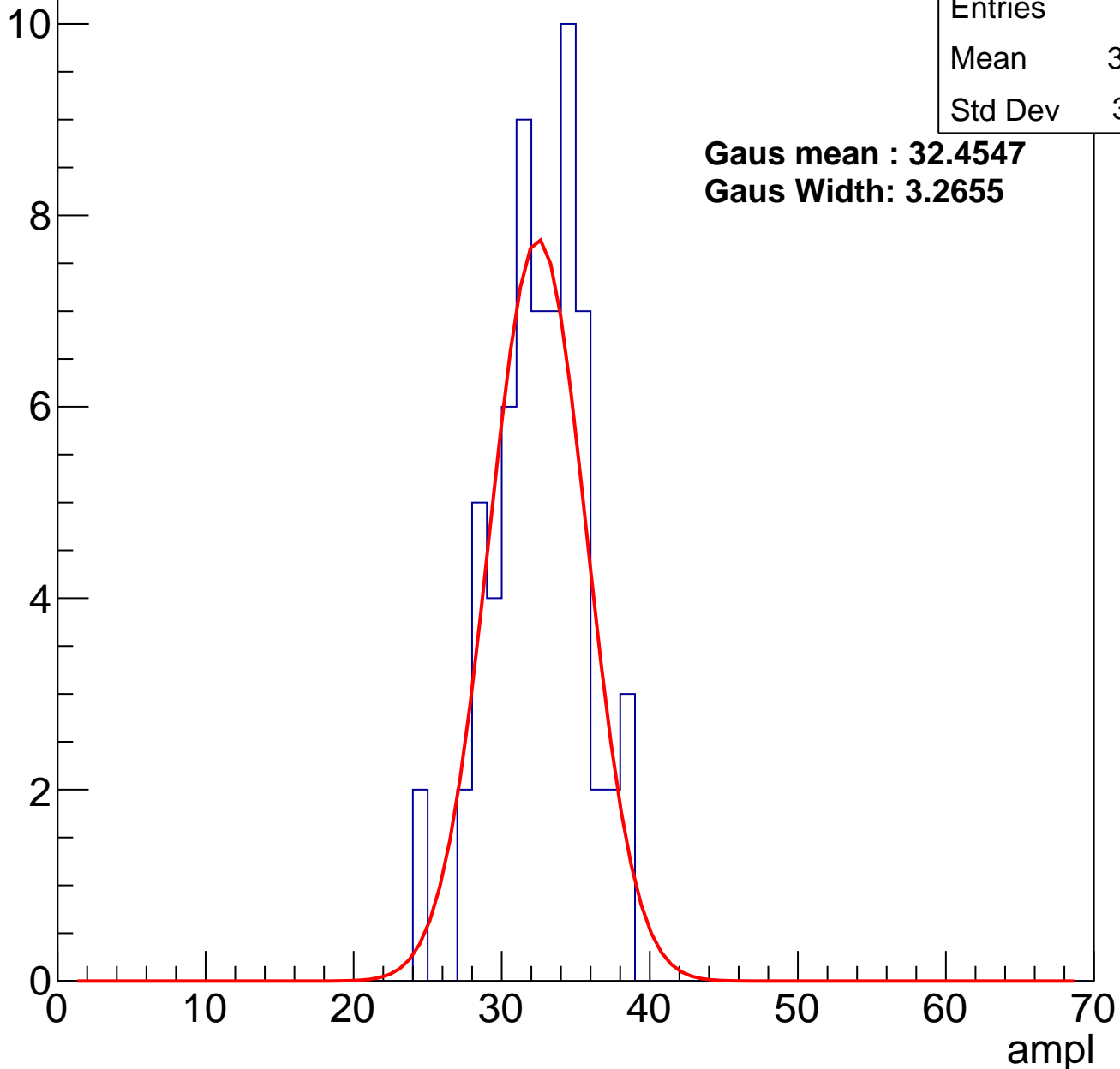
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	66
Mean	32.08
Std Dev	3.081

**Gaus mean : 32.4547**

**Gaus Width: 3.2655**

Entry



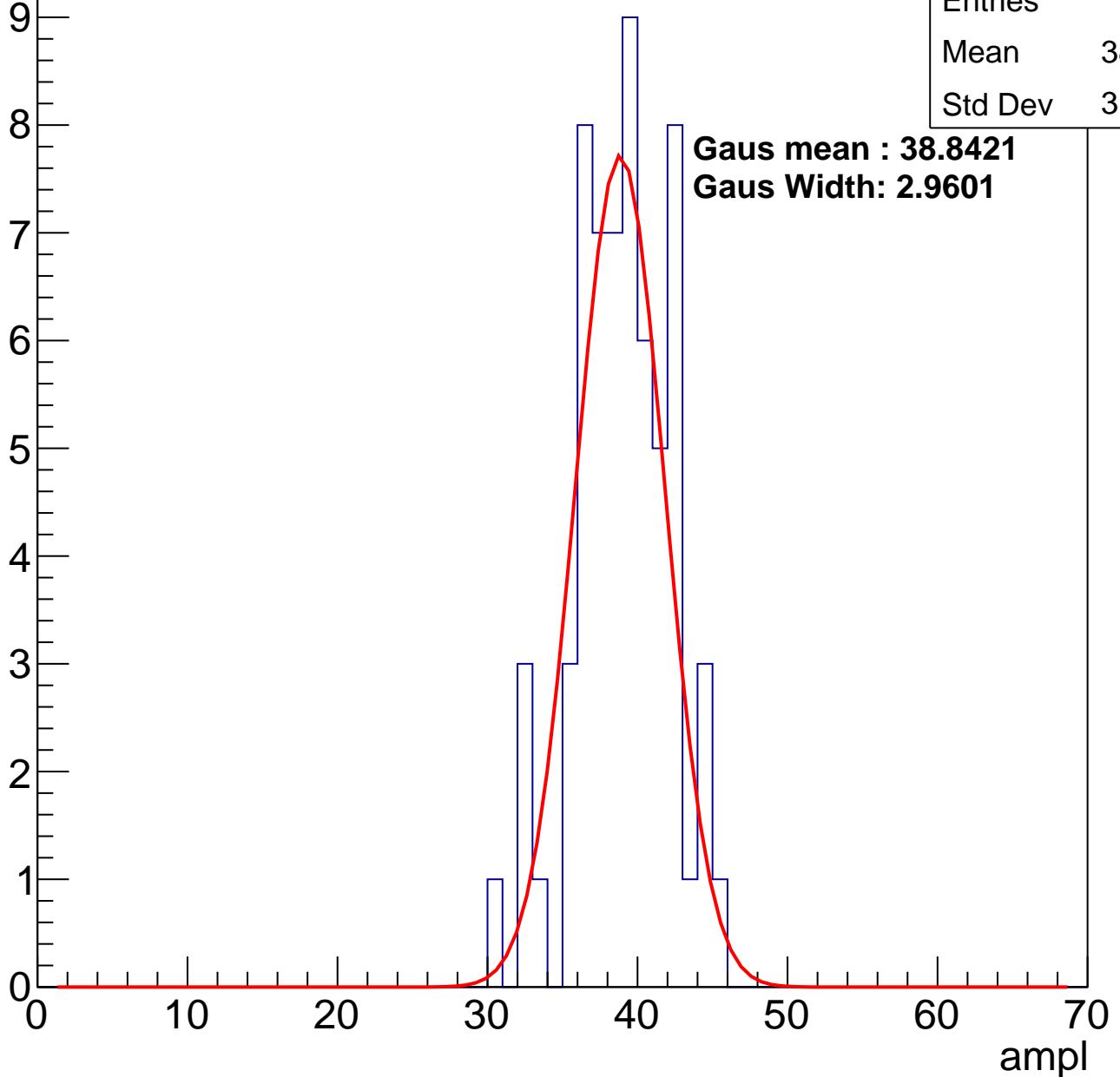
# B0L001S, U6-ch3, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	38.56
Std Dev	3.166

**Gaus mean : 38.8421**  
**Gaus Width: 2.9601**



# B0L001S, U6-ch3, adc2

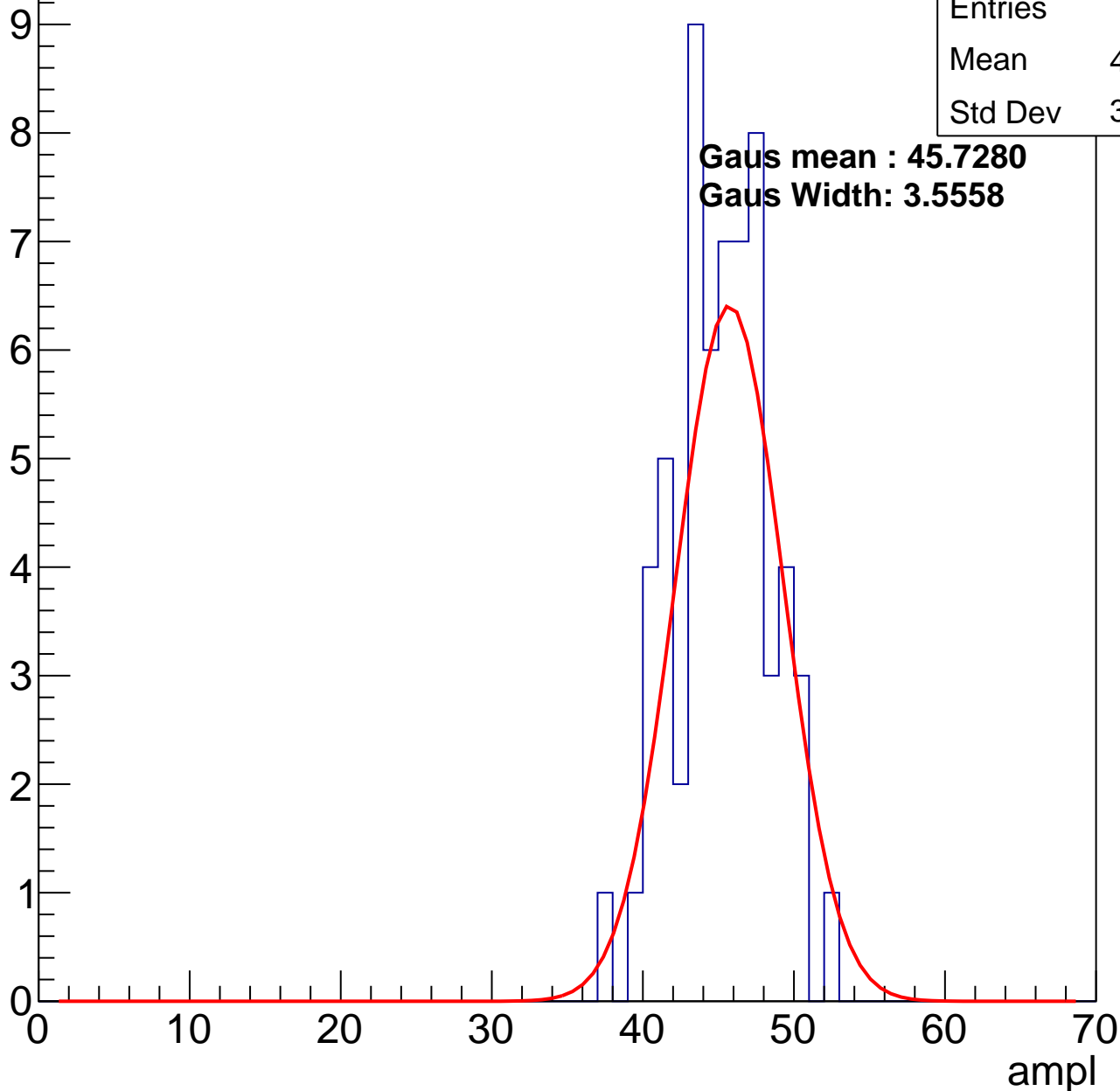
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	44.77
Std Dev	3.112

**Gaus mean : 45.7280**

**Gaus Width: 3.5558**

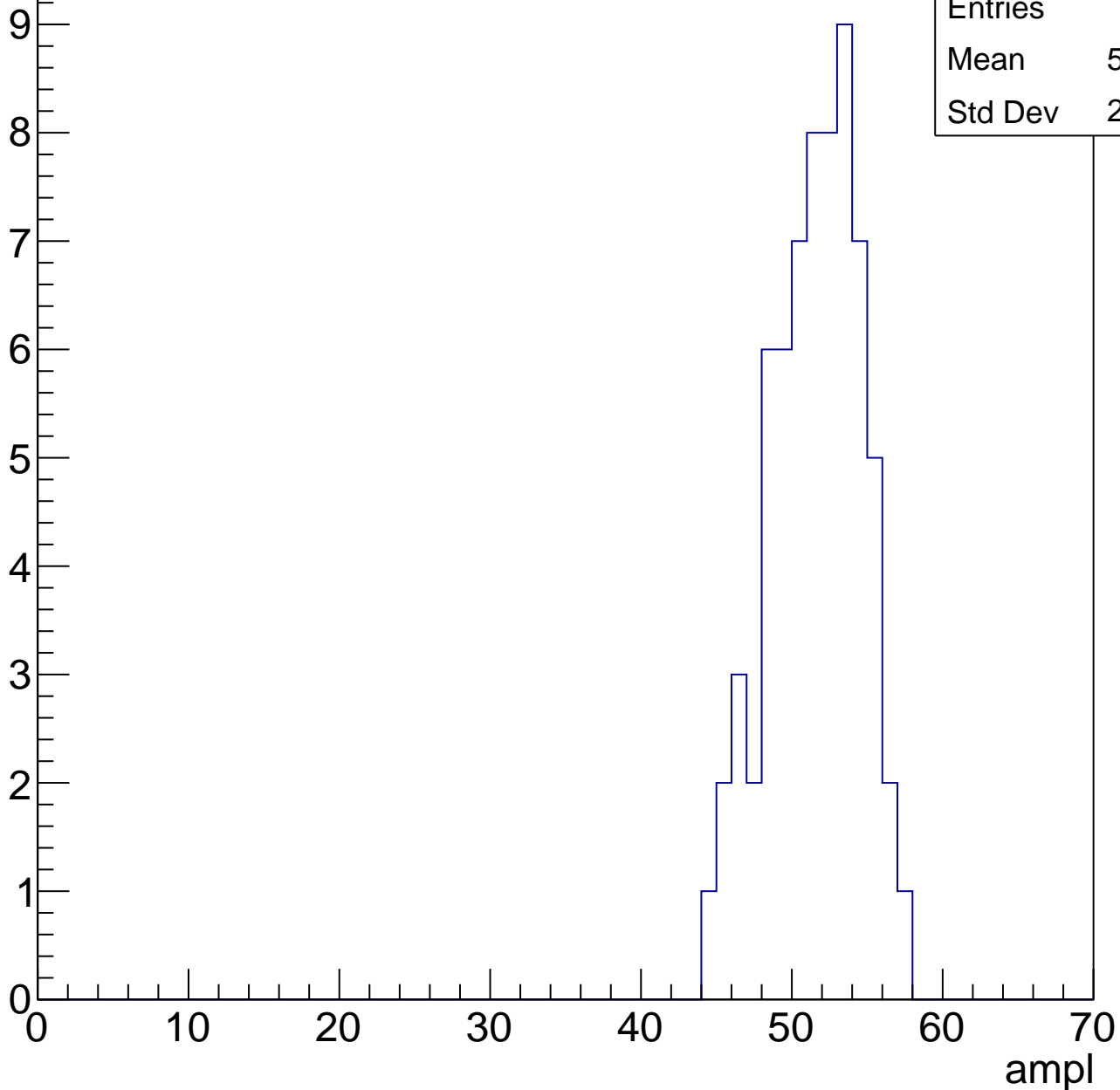


# B0L001S, U6-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	51.06
Std Dev	2.957



# B0L001S, U6-ch3, adc4

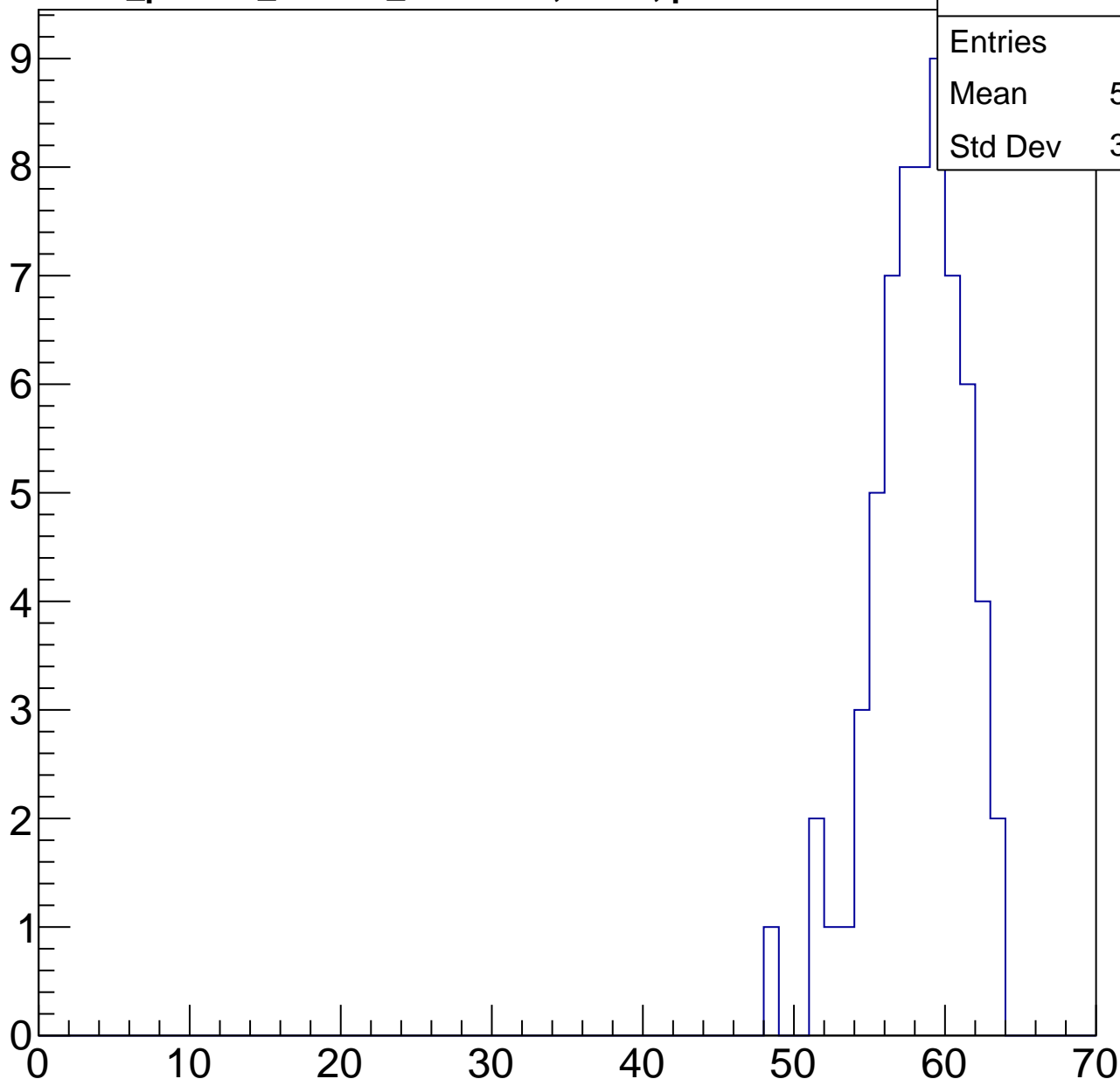
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	64
Mean	57.73
Std Dev	3.032

ampl

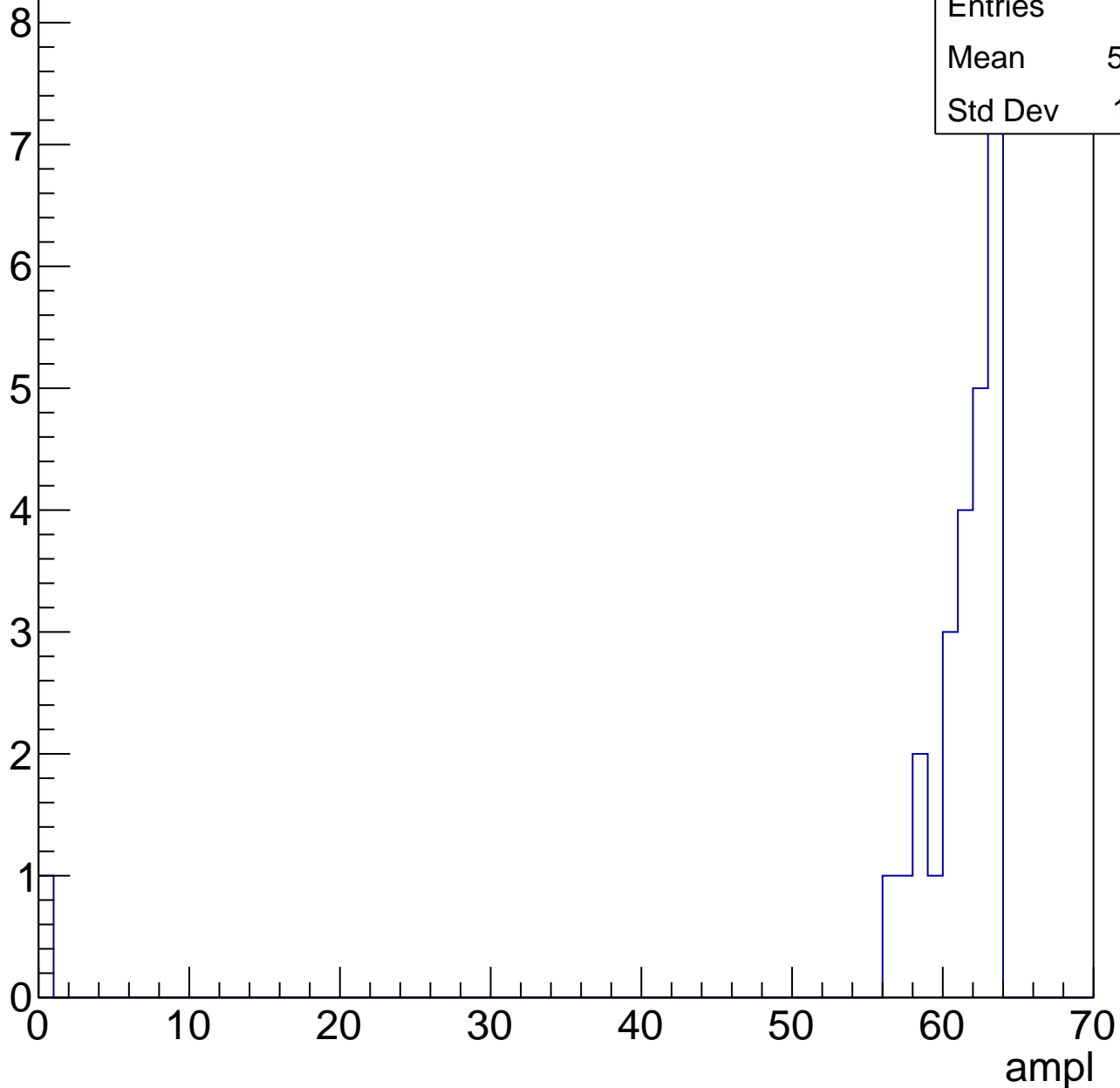


# B0L001S, U6-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	26
Mean	58.69
Std Dev	11.91



# B0L001S, U6-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	62
Std Dev	0



# B0L001S, U6-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U6-ch4, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	78
Mean	31.79
Std Dev	3.495

**Gaus mean : 33.0031**

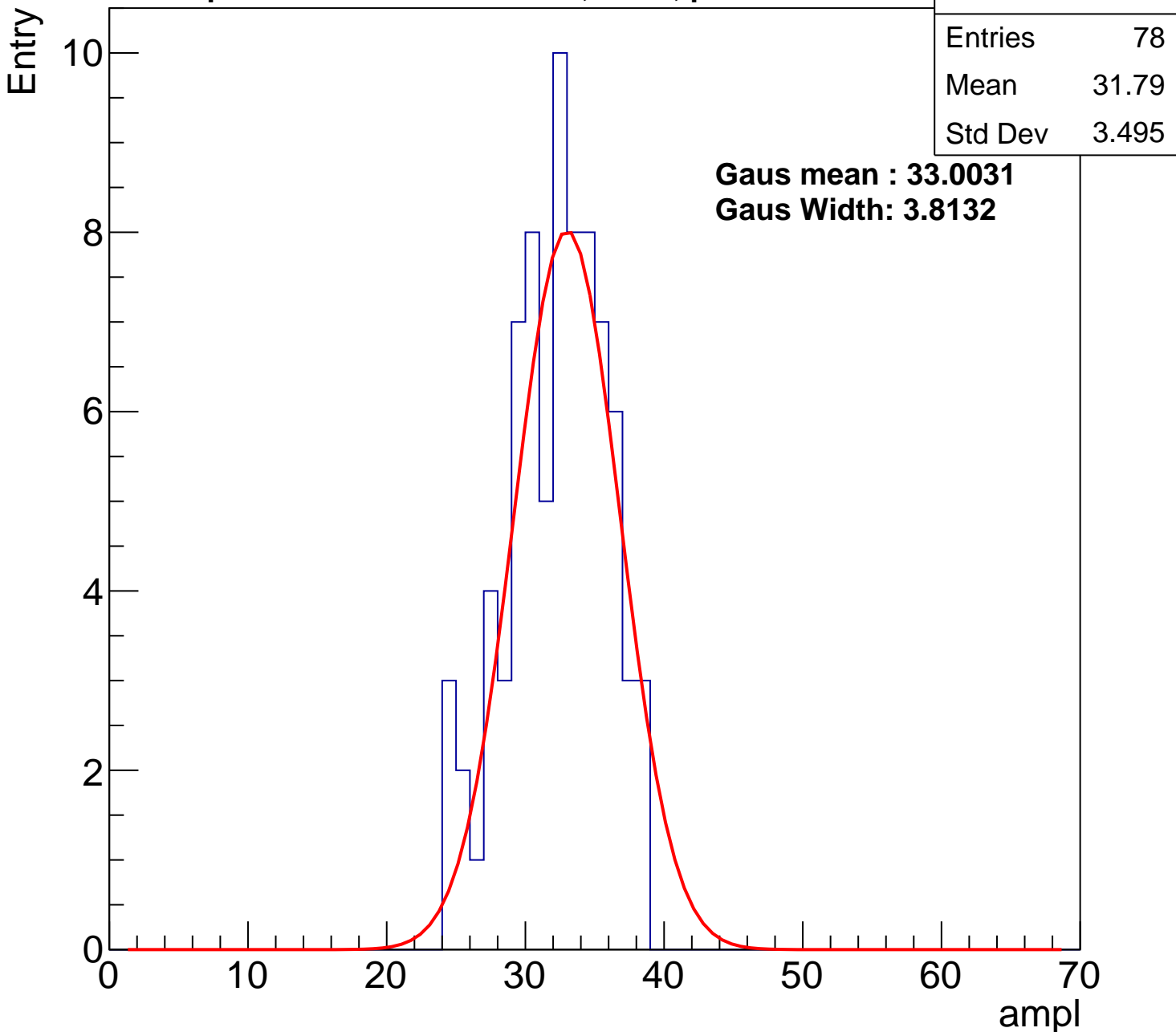
**Gaus Width: 3.8132**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U6-ch4, adc1

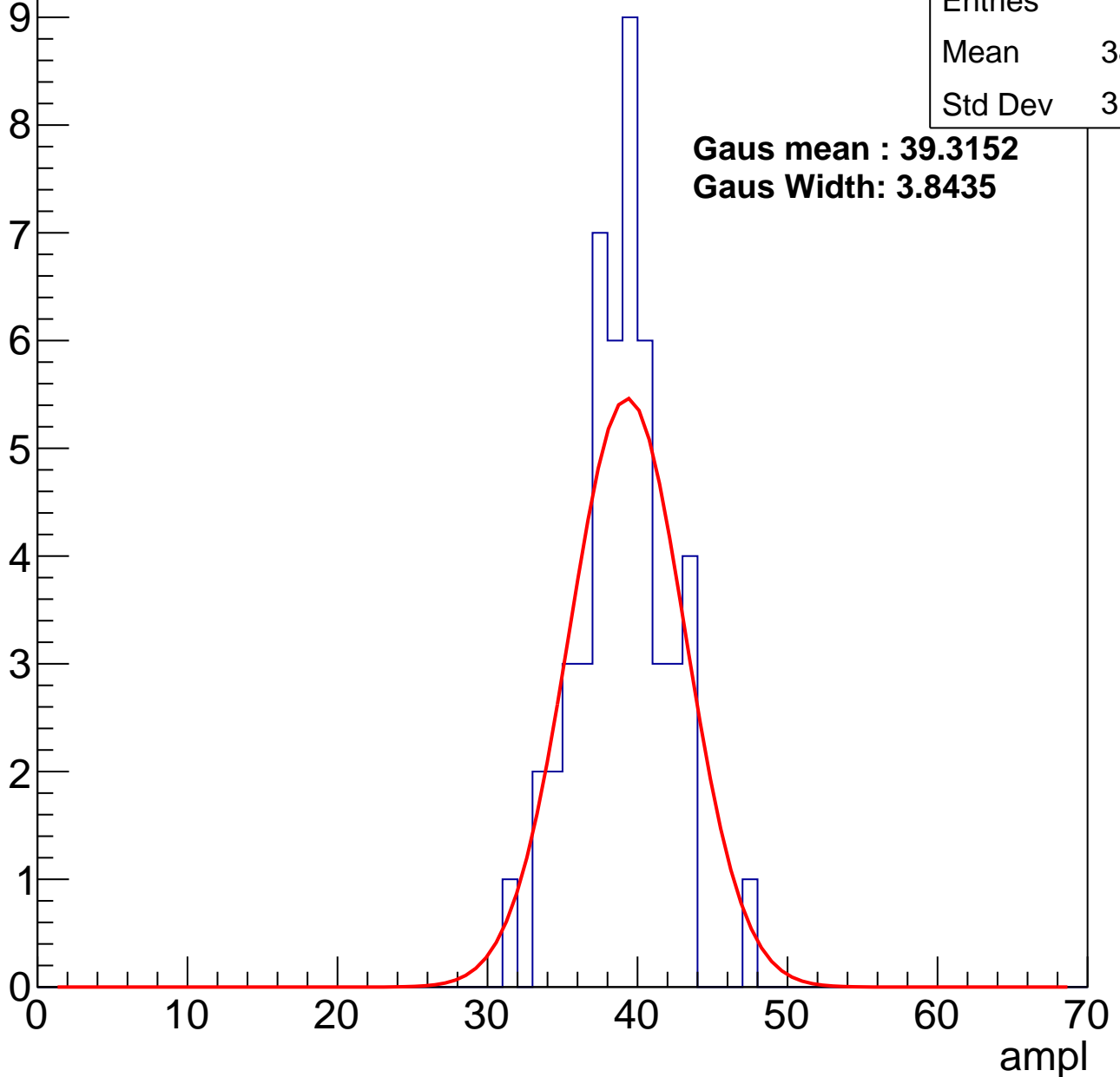
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	38.48
Std Dev	3.015

**Gaus mean : 39.3152**

**Gaus Width: 3.8435**



# B0L001S, U6-ch4, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	66
Mean	44.06
Std Dev	2.865

**Gaus mean : 44.9719**

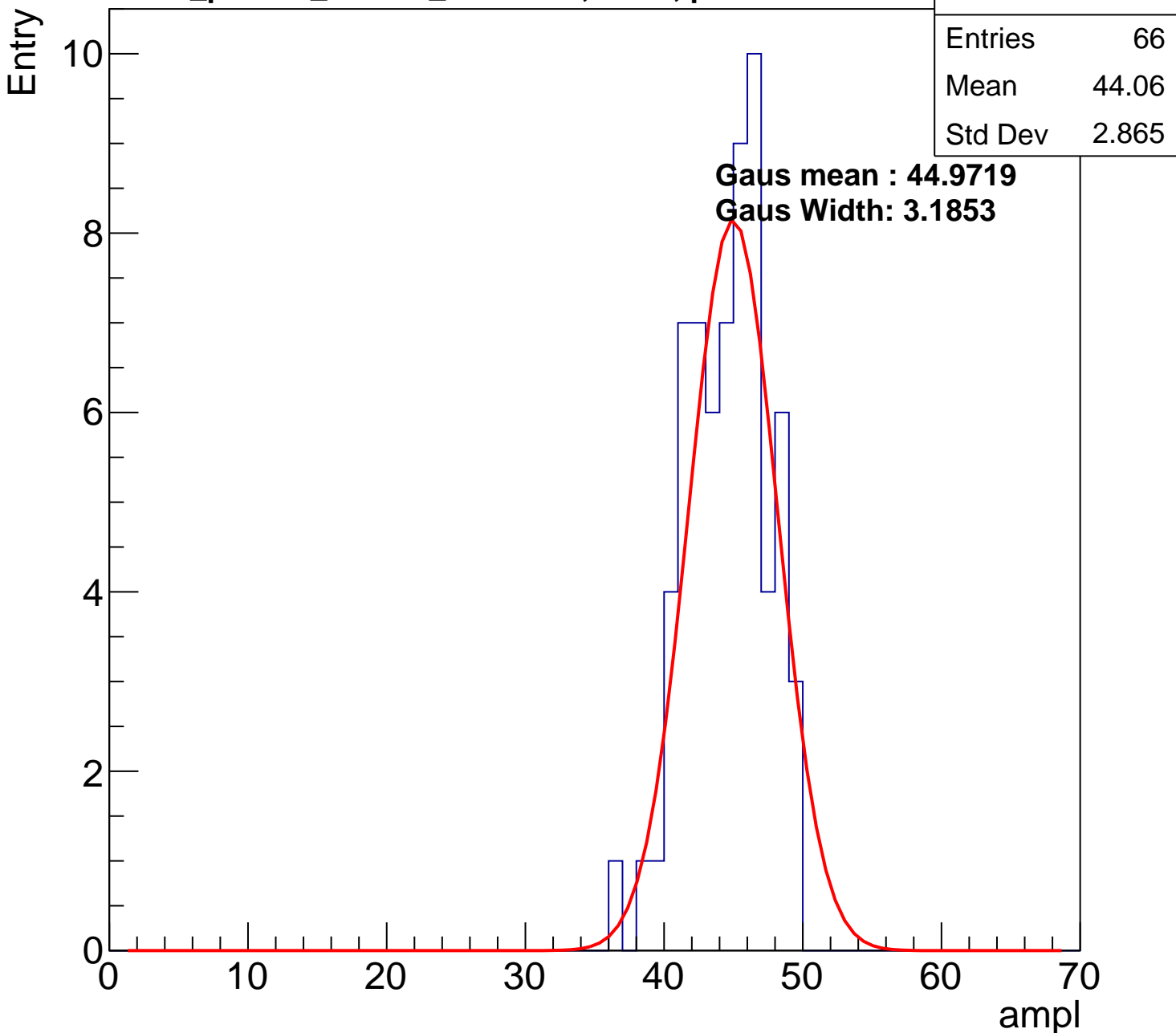
**Gaus Width: 3.1853**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

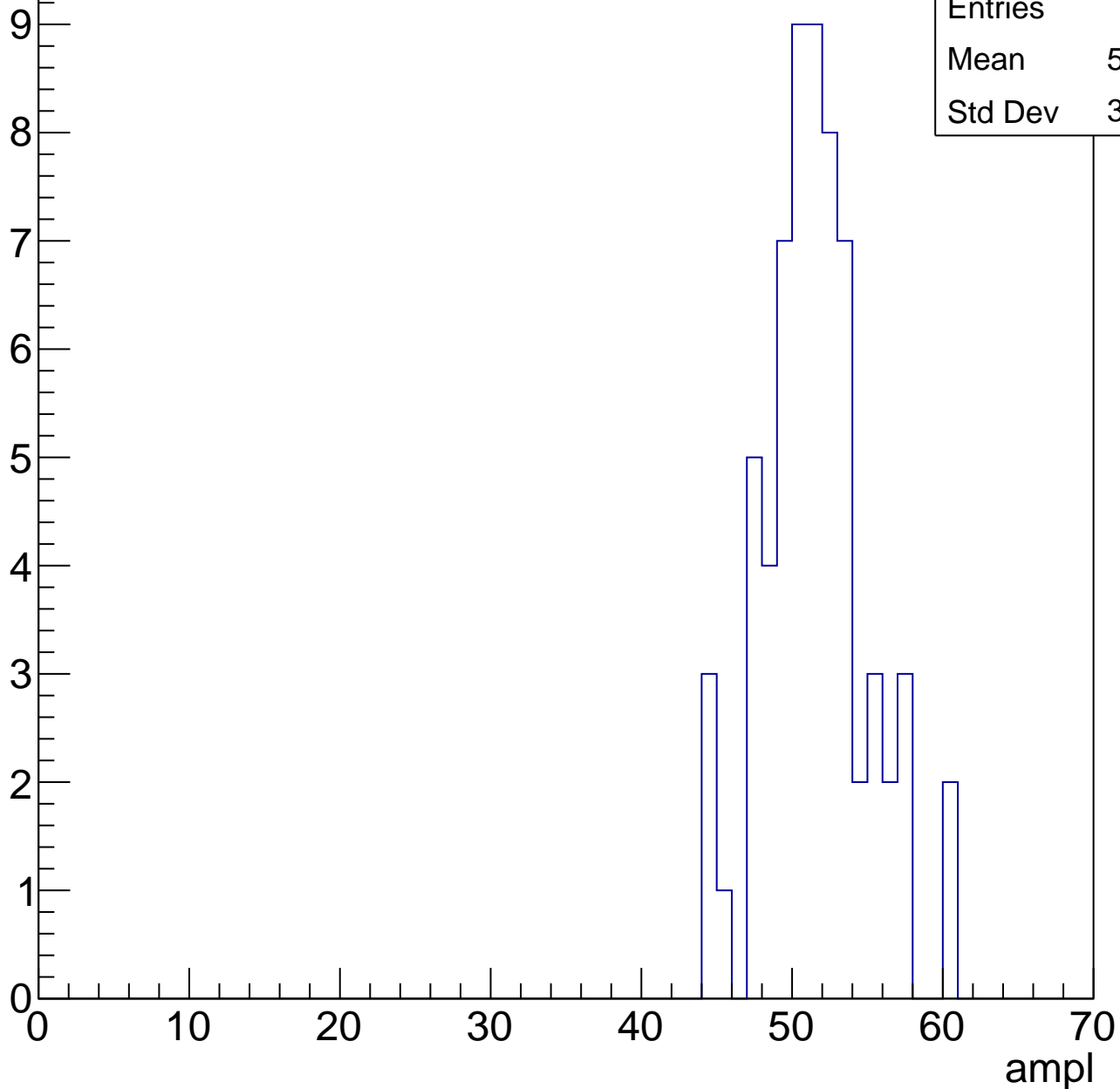


# B0L001S, U6-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	51.06
Std Dev	3.414



# B0L001S, U6-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

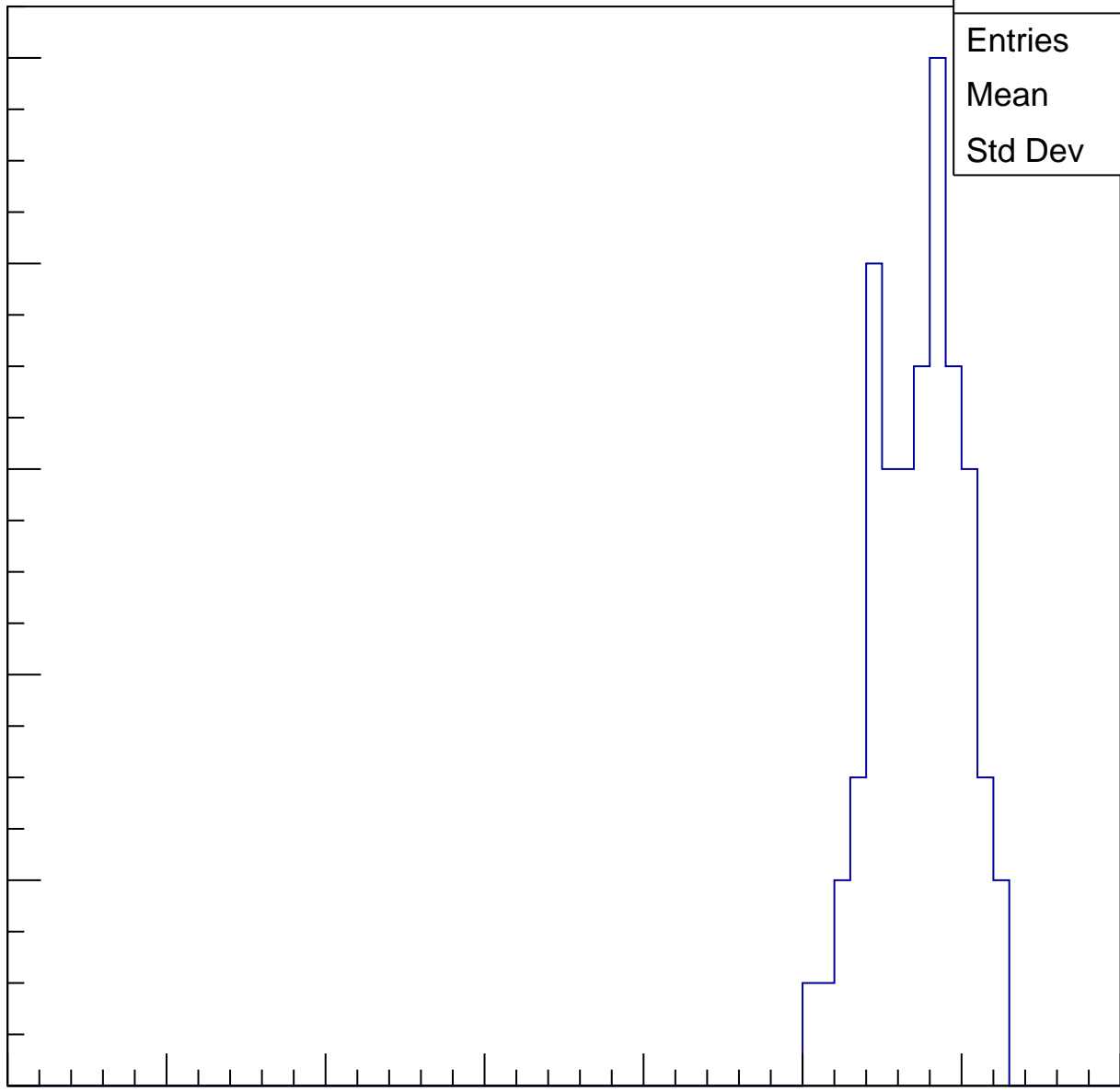
Entries	62
Mean	56.79
Std Dev	2.76

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

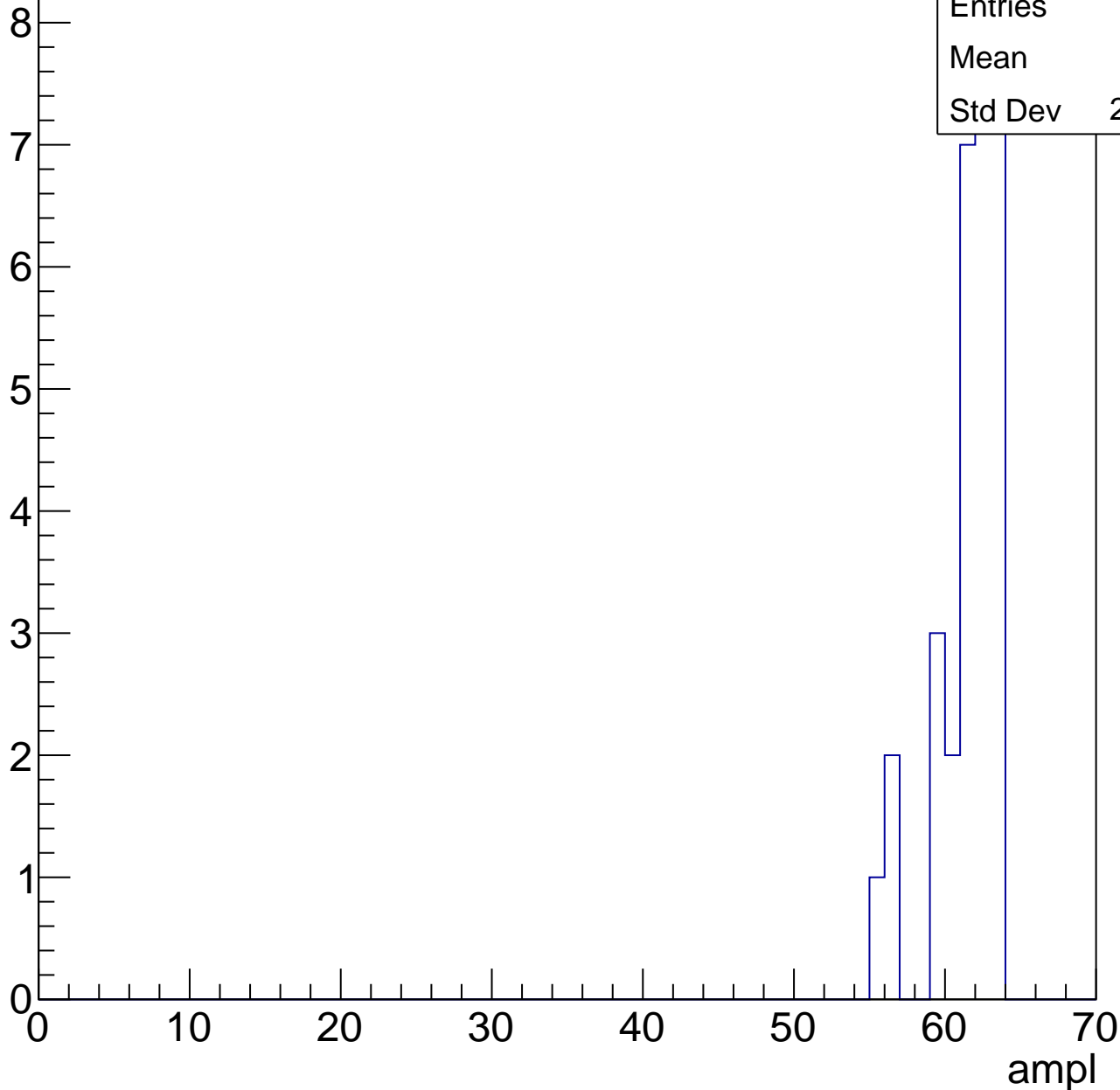


# B0L001S, U6-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

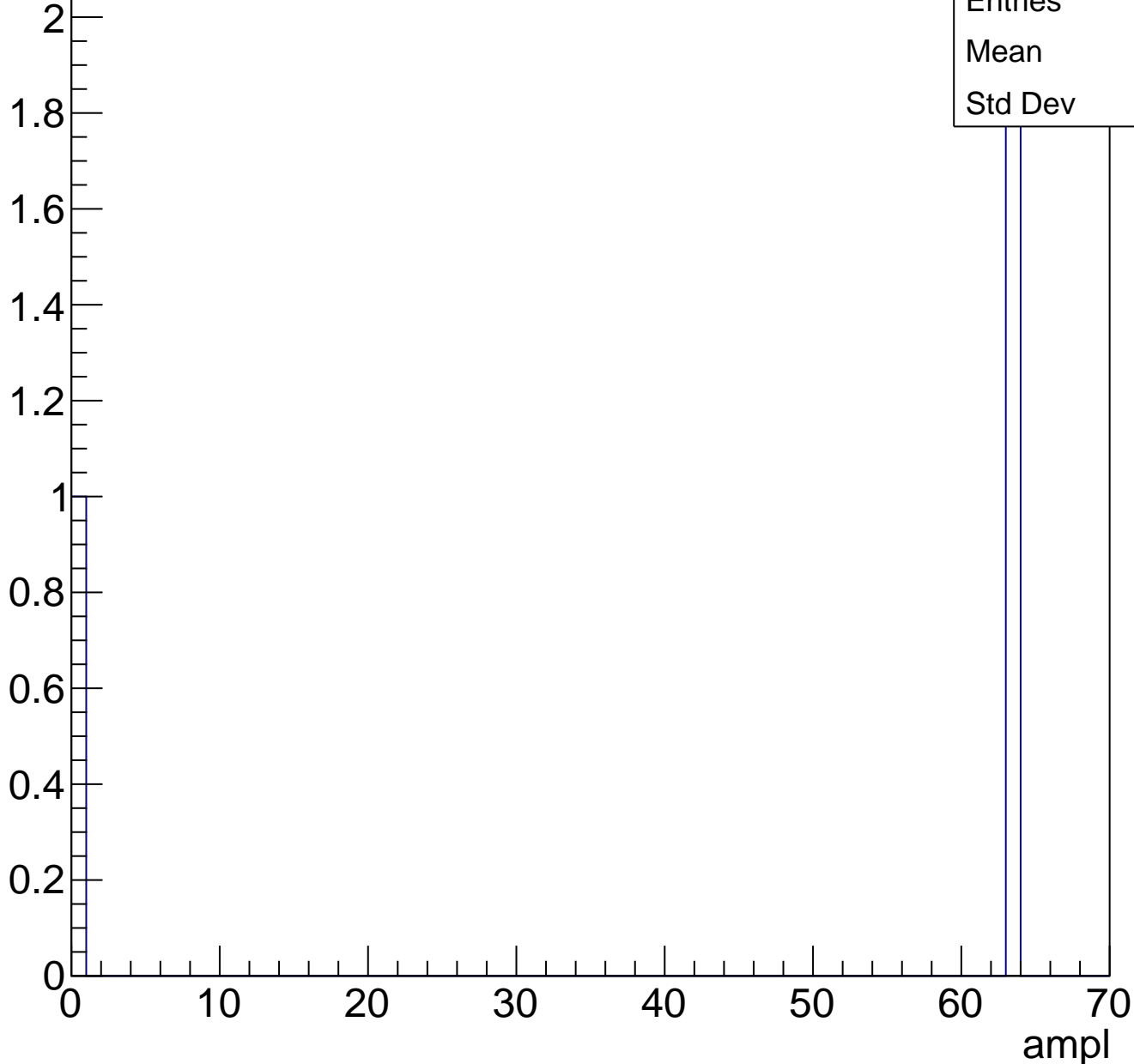
Entries	31
Mean	61
Std Dev	2.125



# B0L001S, U6-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

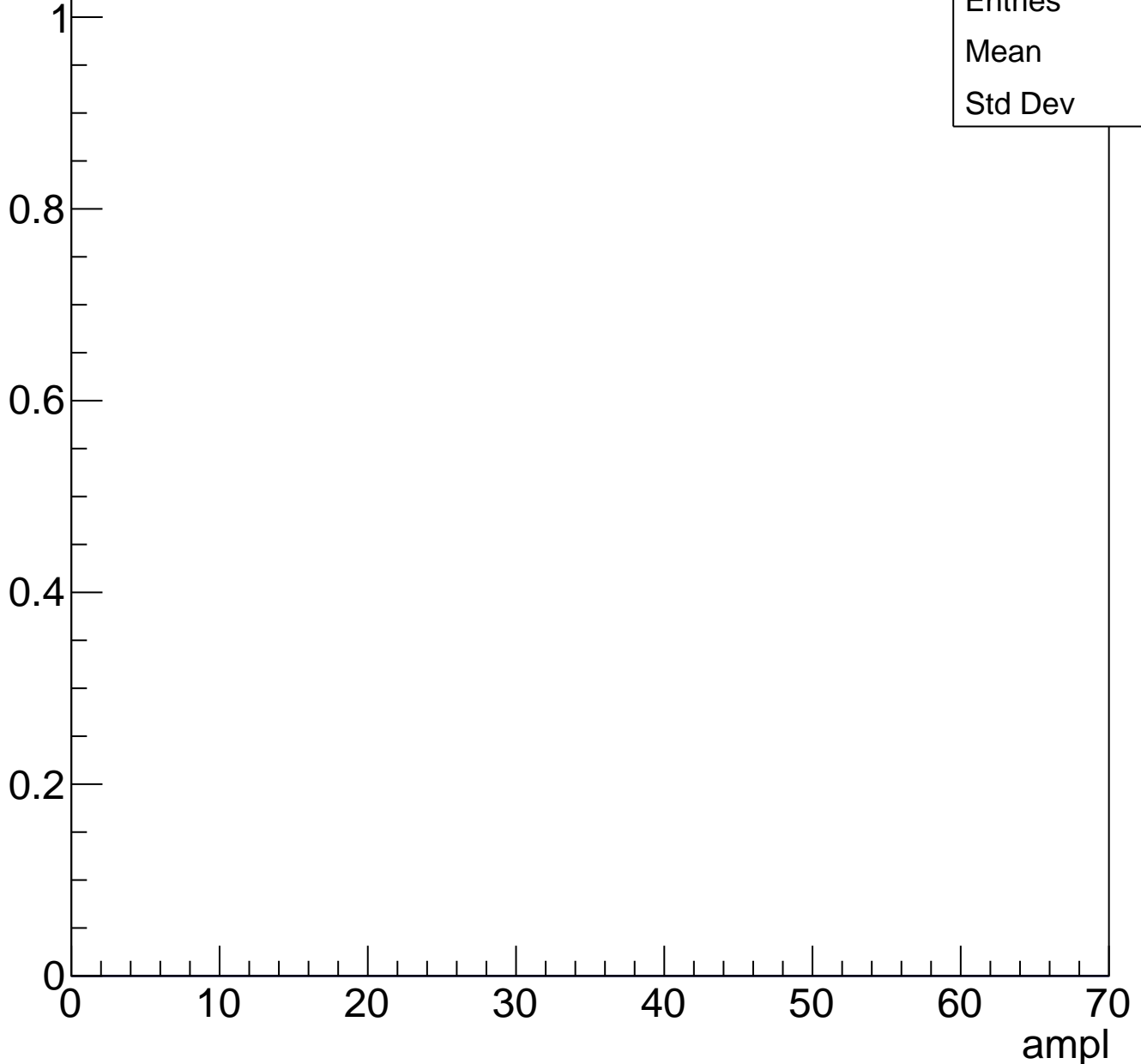




# B0L001S, U6-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U6-ch5, adc0

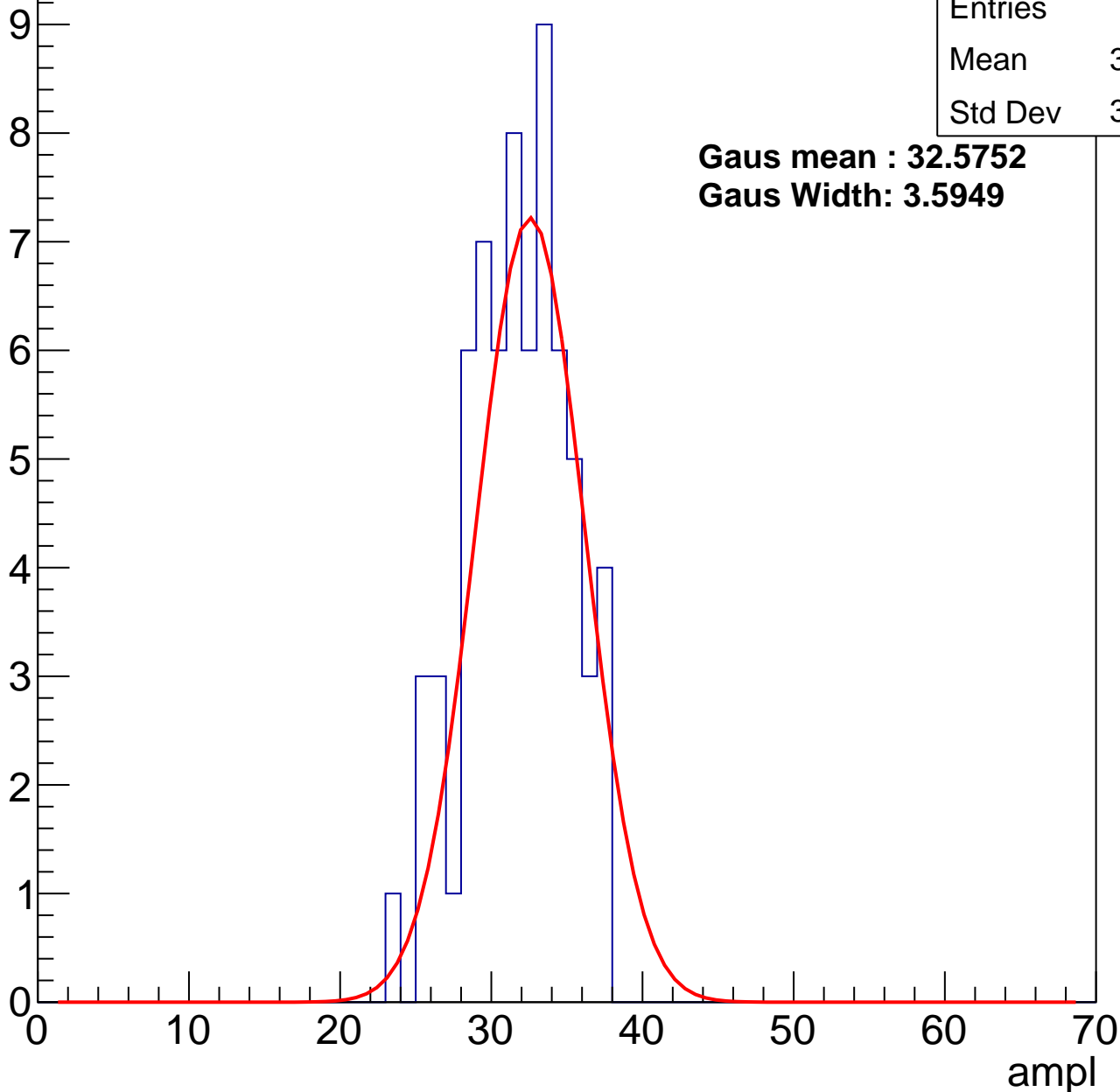
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	31.26
Std Dev	3.302

**Gaus mean : 32.5752**

**Gaus Width: 3.5949**



# B0L001S, U6-ch5, adc1

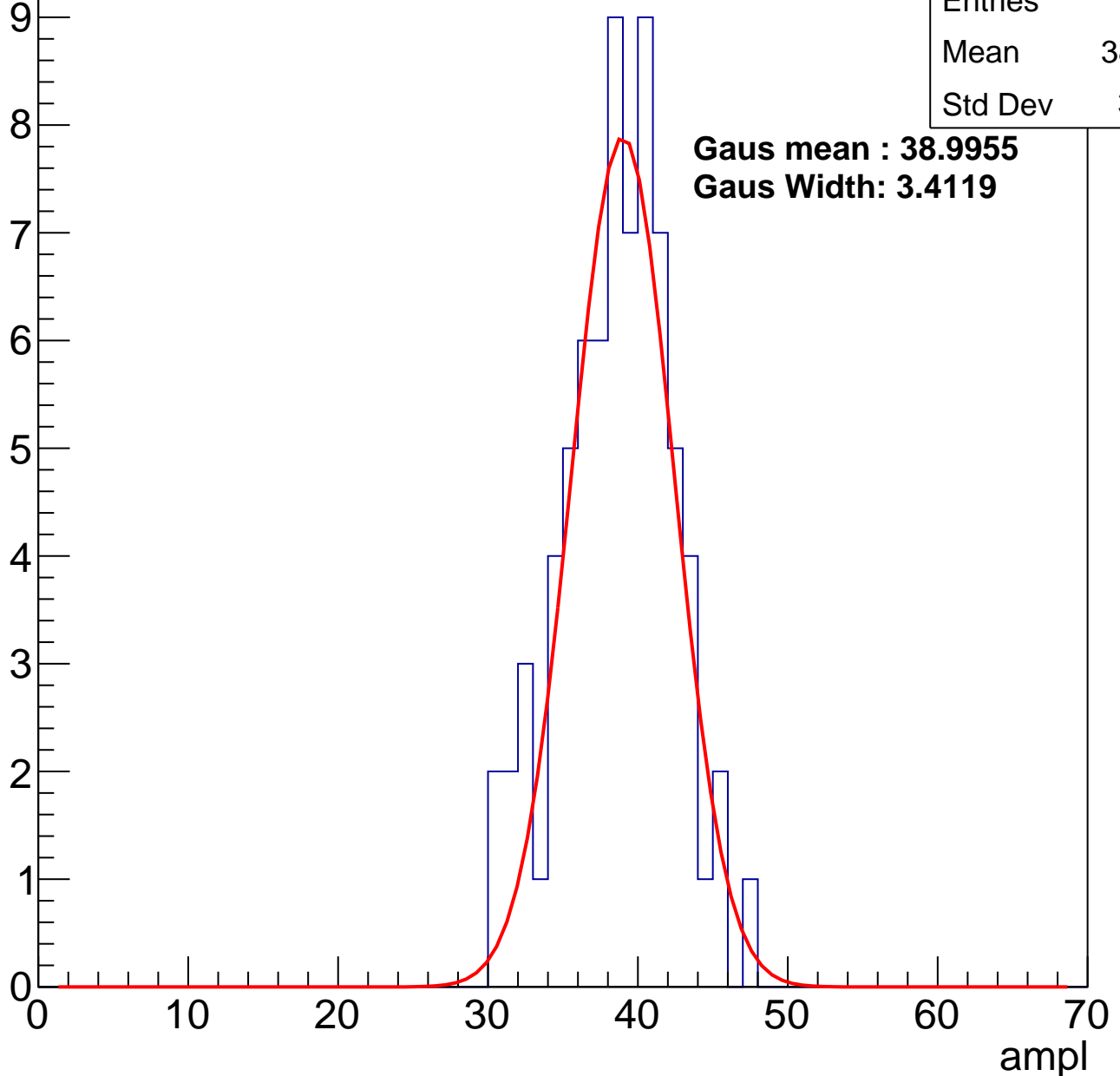
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	38.18
Std Dev	3.67

**Gaus mean : 38.9955**

**Gaus Width: 3.4119**



# B0L001S, U6-ch5, adc2

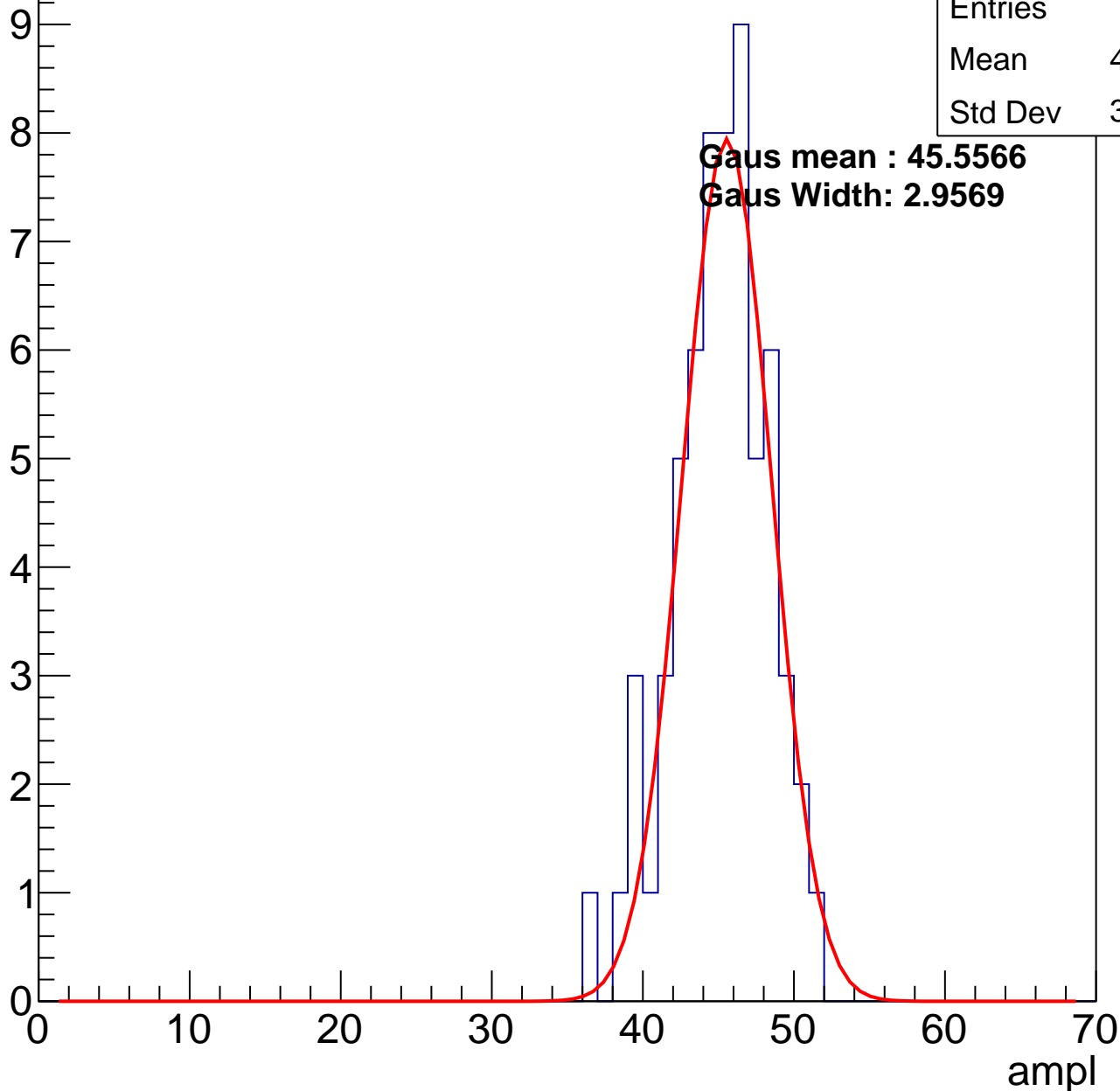
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	44.66
Std Dev	3.105

Gaus mean : 45.5566

Gaus Width: 2.9569



# B0L001S, U6-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

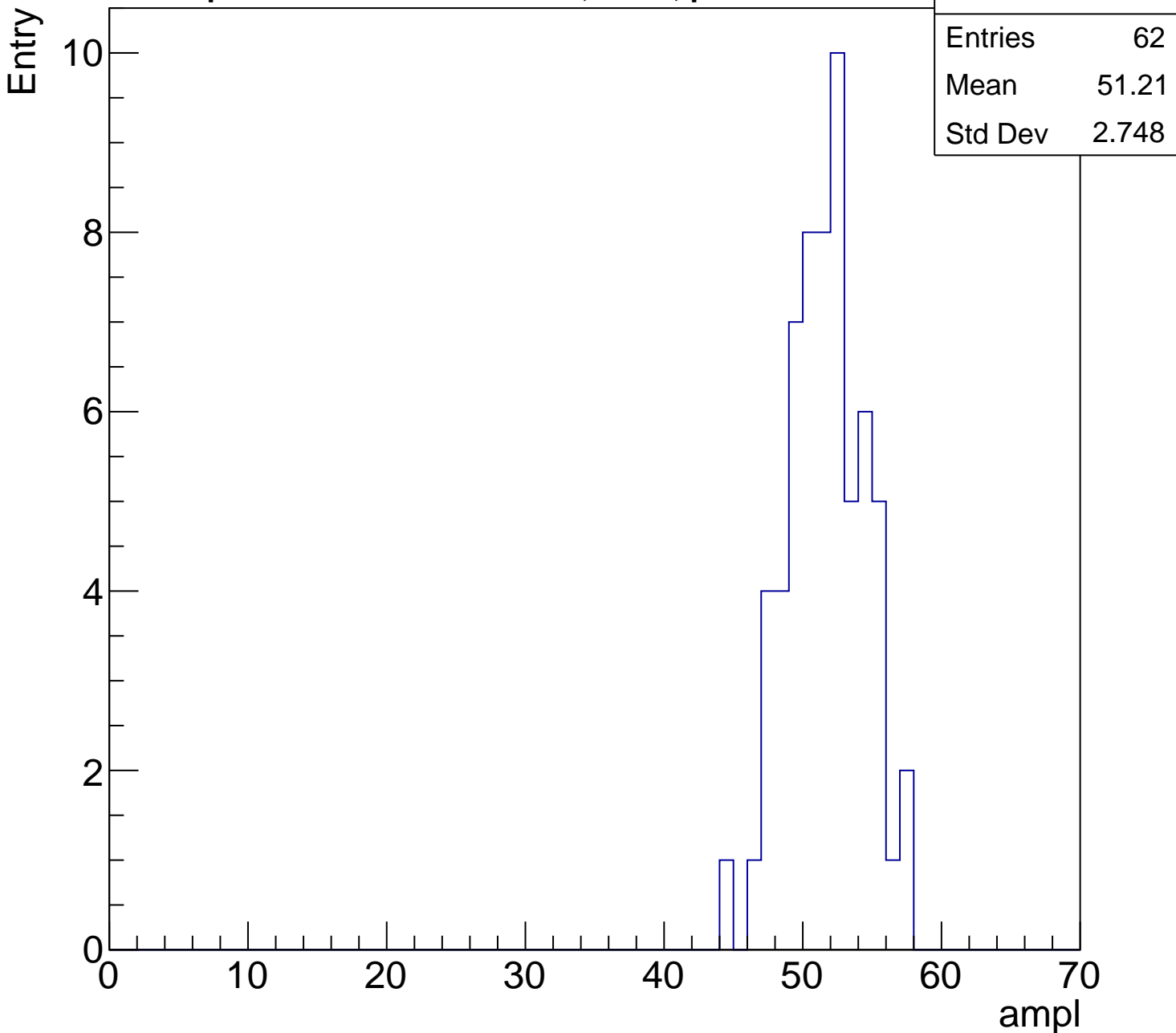
Entries	62
Mean	51.21
Std Dev	2.748

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

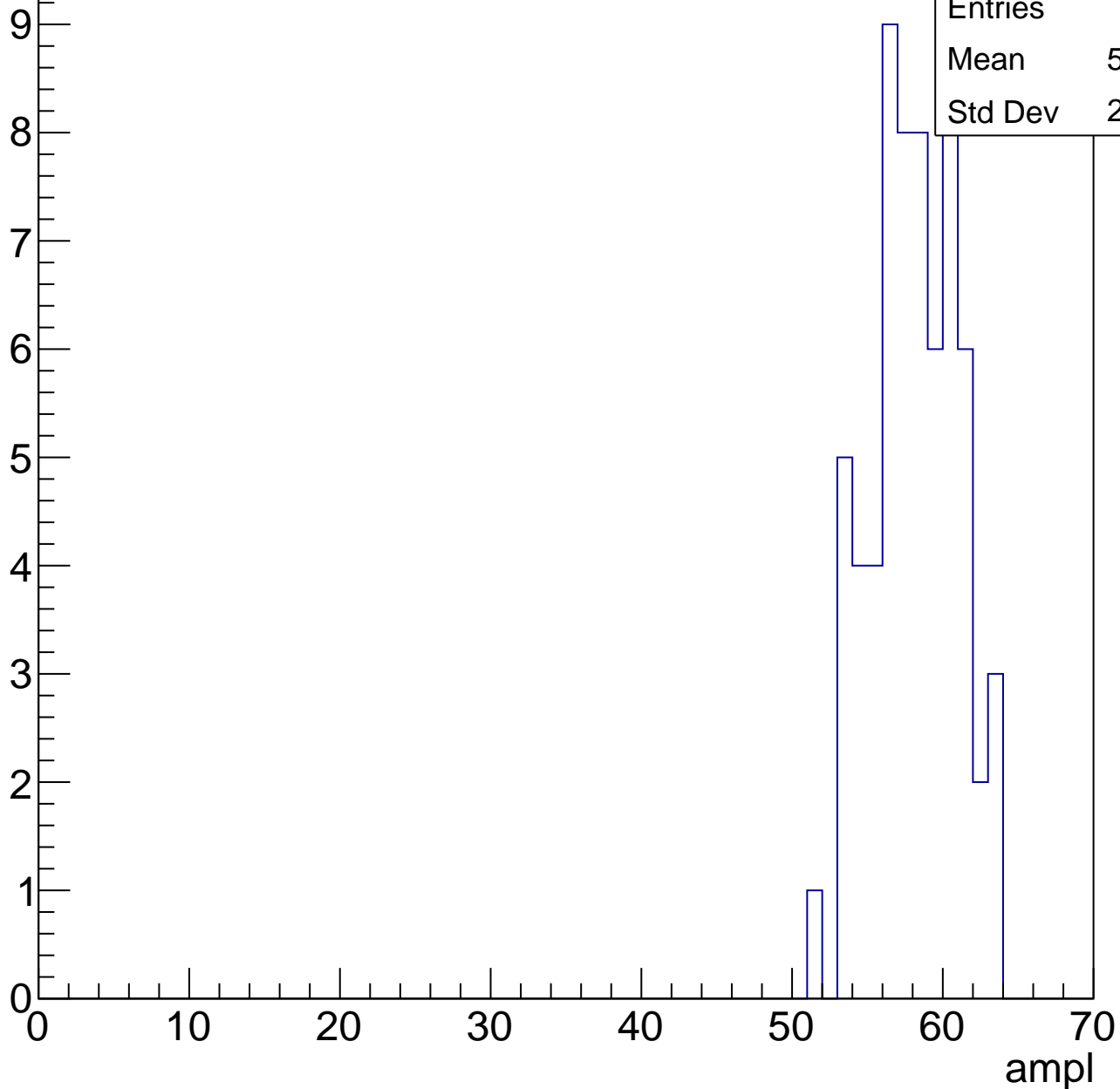
ampl



# B0L001S, U6-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

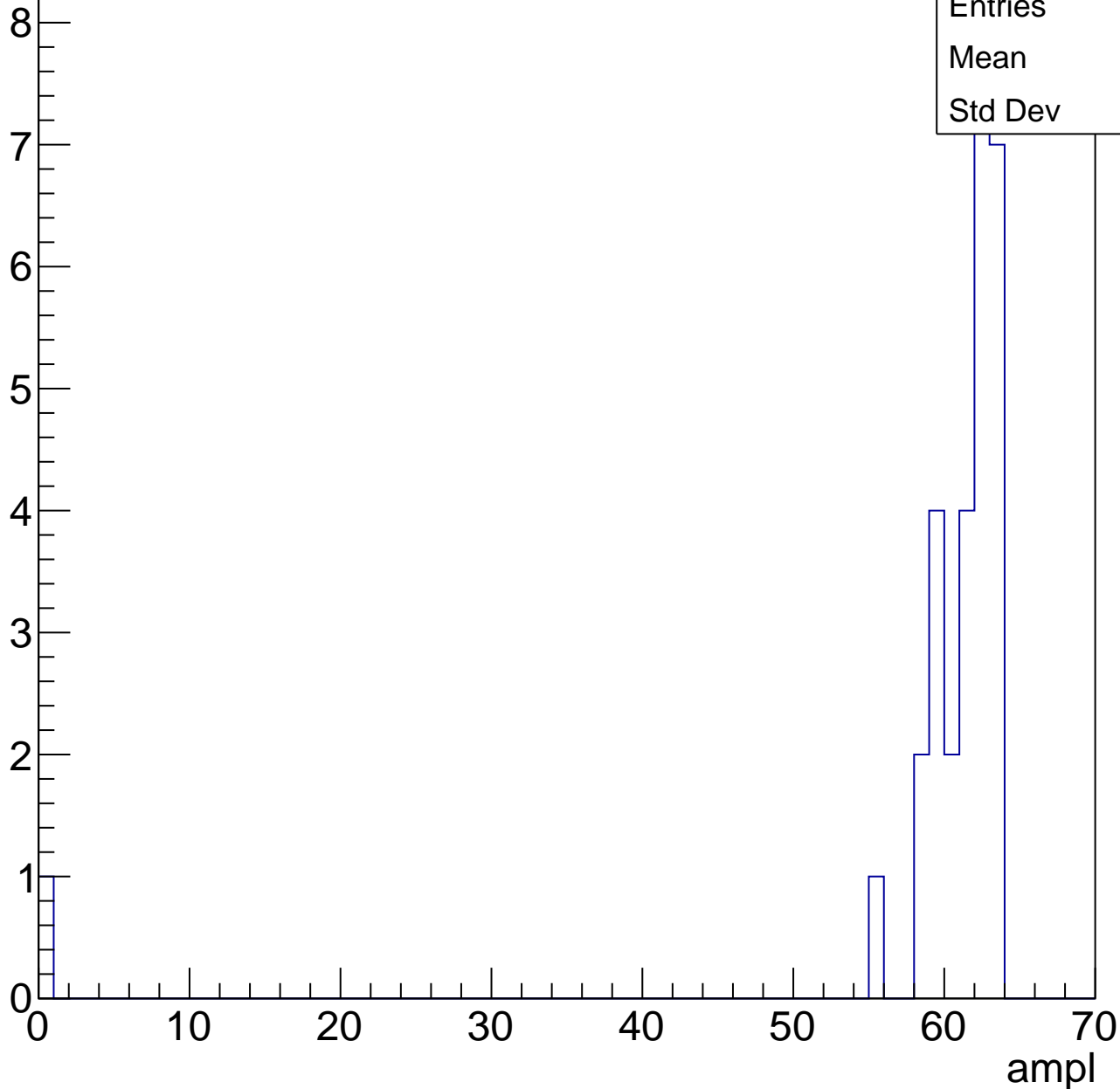


# B0L001S, U6-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	29
Mean	58.9
Std Dev	11.3



# B0L001S, U6-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U6-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch6, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	71
Mean	30.34
Std Dev	3.233

**Gaus mean : 31.2402**

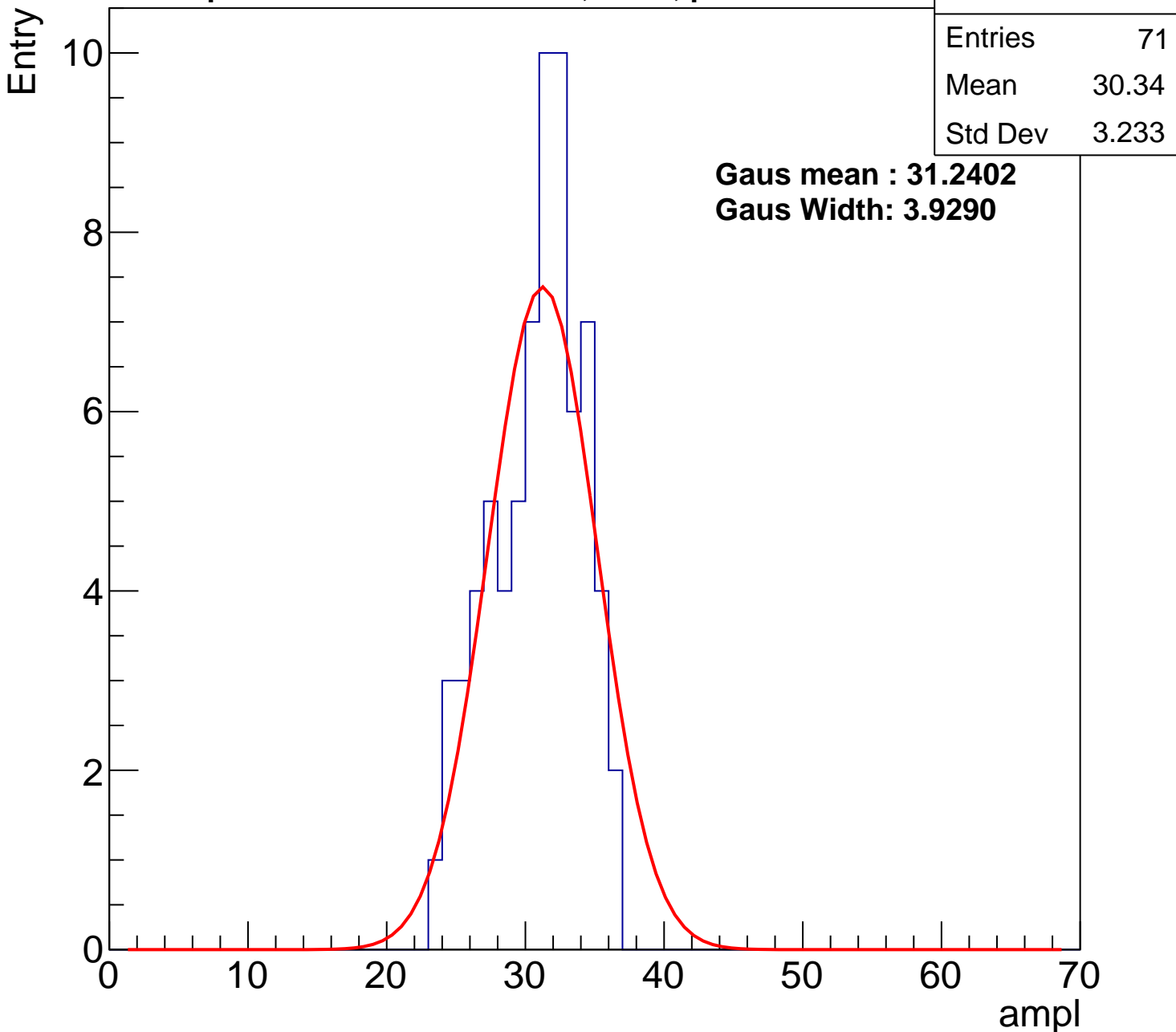
**Gaus Width: 3.9290**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



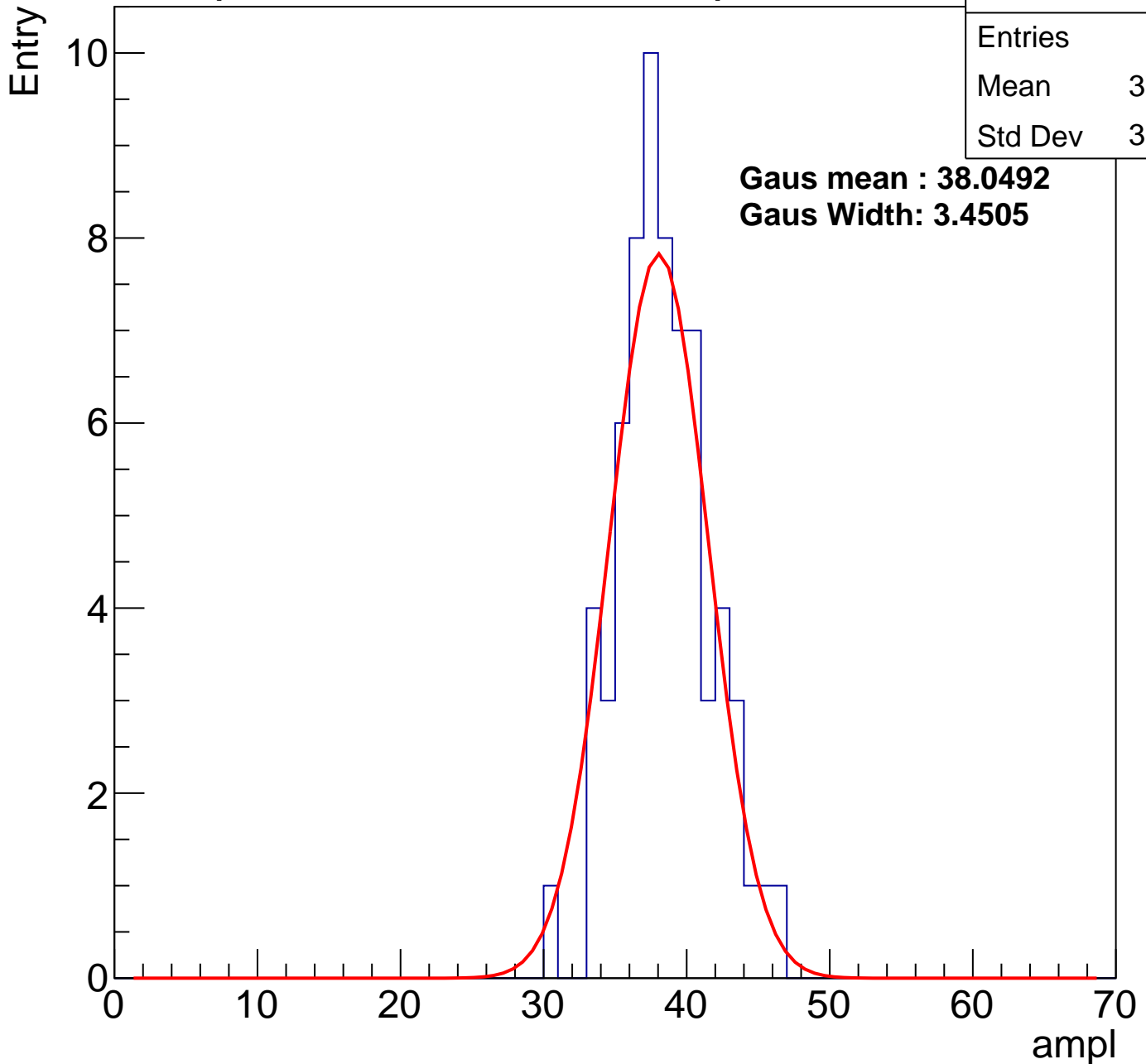
# B0L001S, U6-ch6, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	67
Mean	37.97
Std Dev	3.134

**Gaus mean : 38.0492**

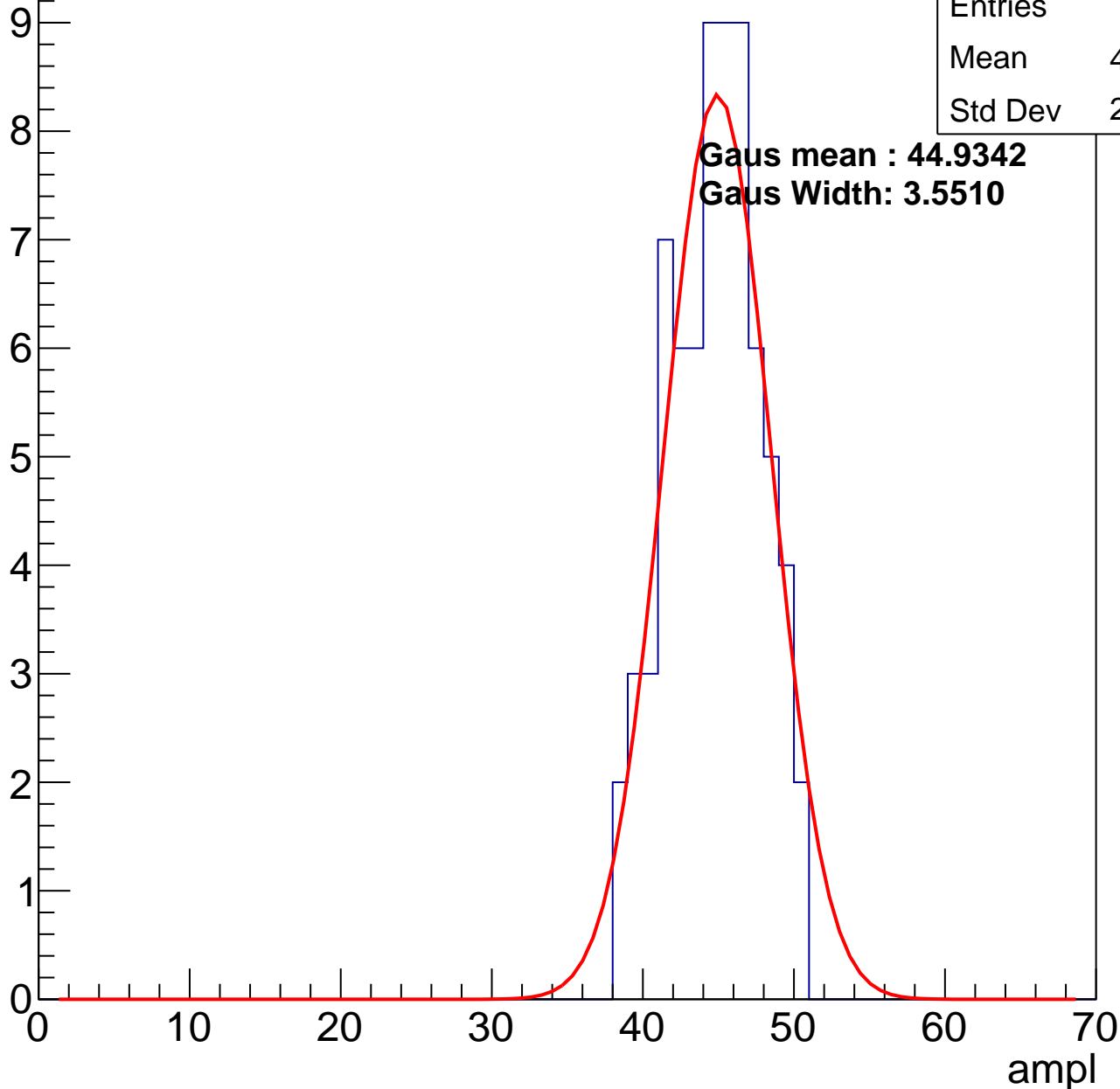
**Gaus Width: 3.4505**



# B0L001S, U6-ch6, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

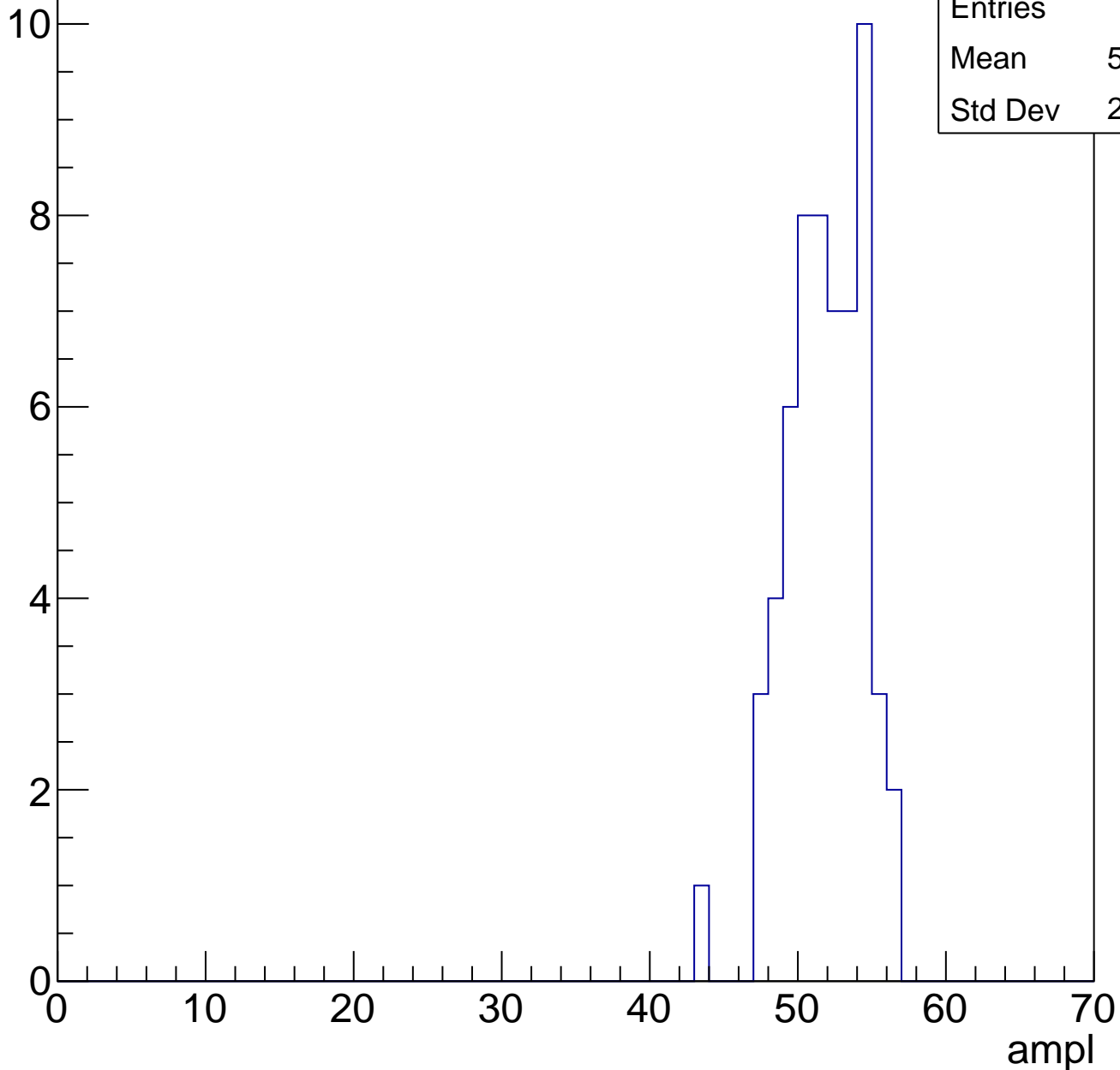


# B0L001S, U6-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	59
Mean	51.36
Std Dev	2.589

Entry



# B0L001S, U6-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	64
Mean	57.03
Std Dev	3.302

Entry

10

8

6

4

2

0

0

10

20

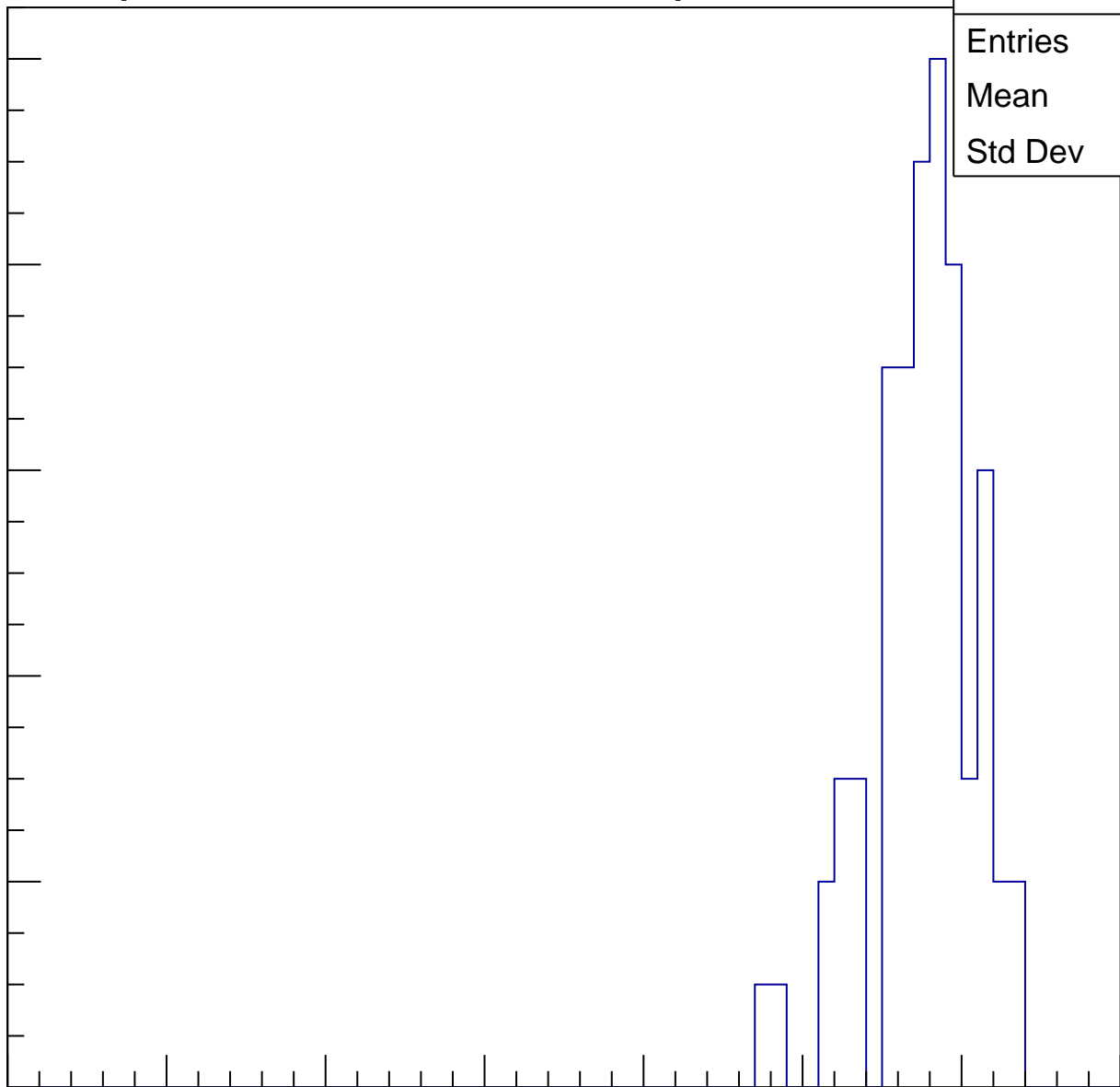
30

40

50

60

ampl



# B0L001S, U6-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	32
Mean	59.22
Std Dev	10.78

ampl

0

10

20

30

40

50

60

70

# B0L001S, U6-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U6-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch7, adc0

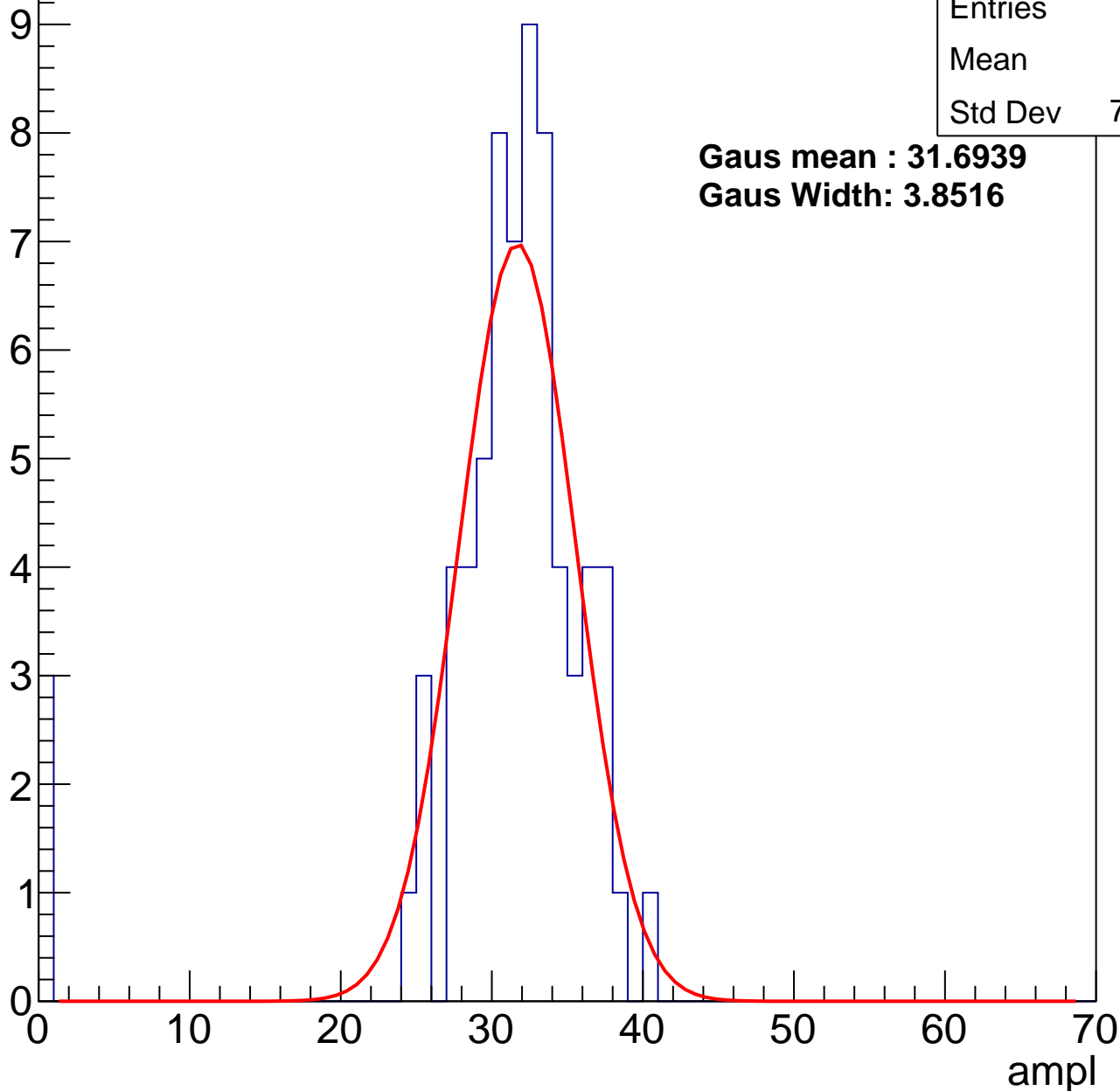
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	30.2
Std Dev	7.246

**Gaus mean : 31.6939**

**Gaus Width: 3.8516**



# B0L001S, U6-ch7, adc1

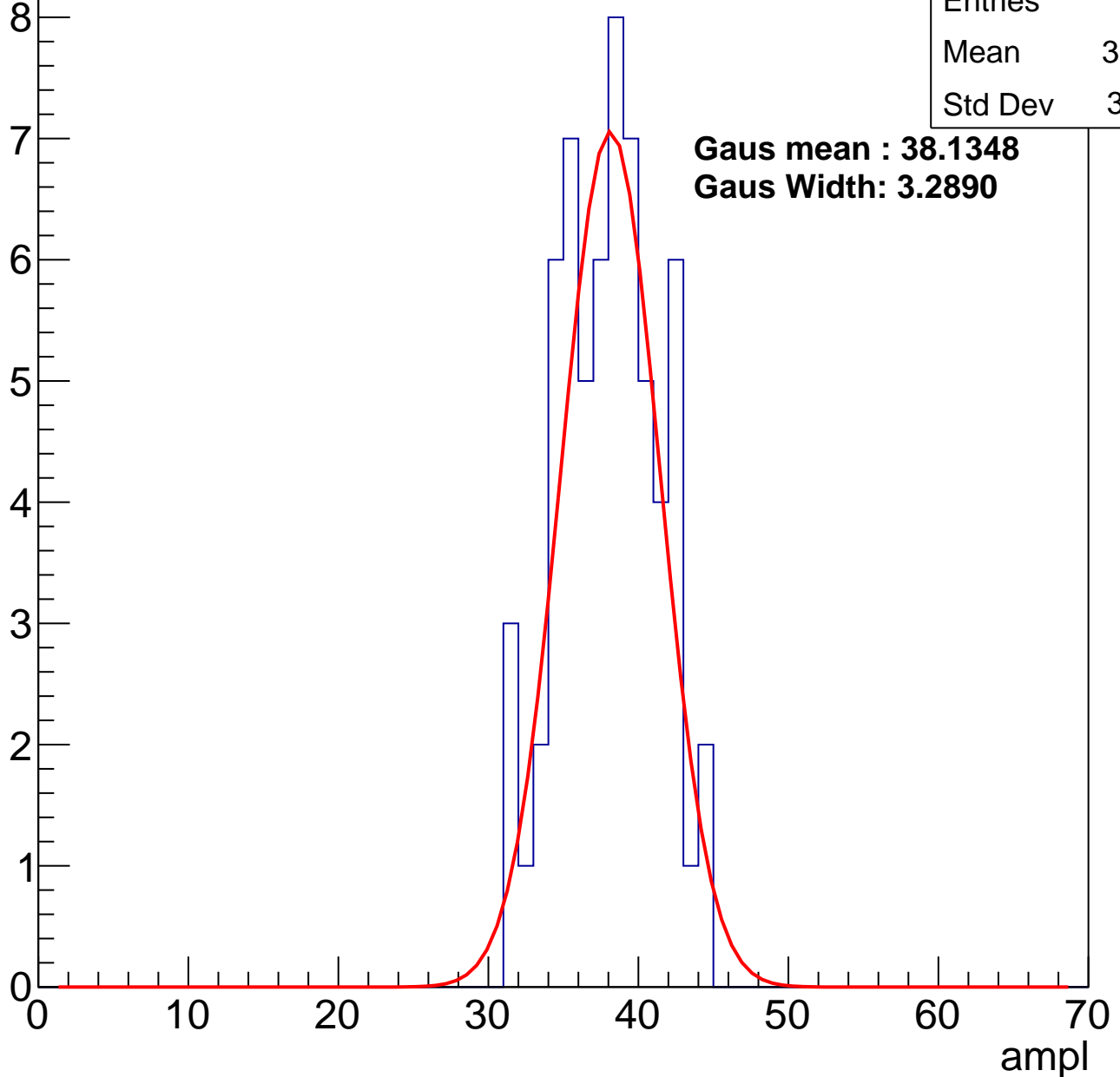
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	37.56
Std Dev	3.241

**Gaus mean : 38.1348**

**Gaus Width: 3.2890**



# B0L001S, U6-ch7, adc2

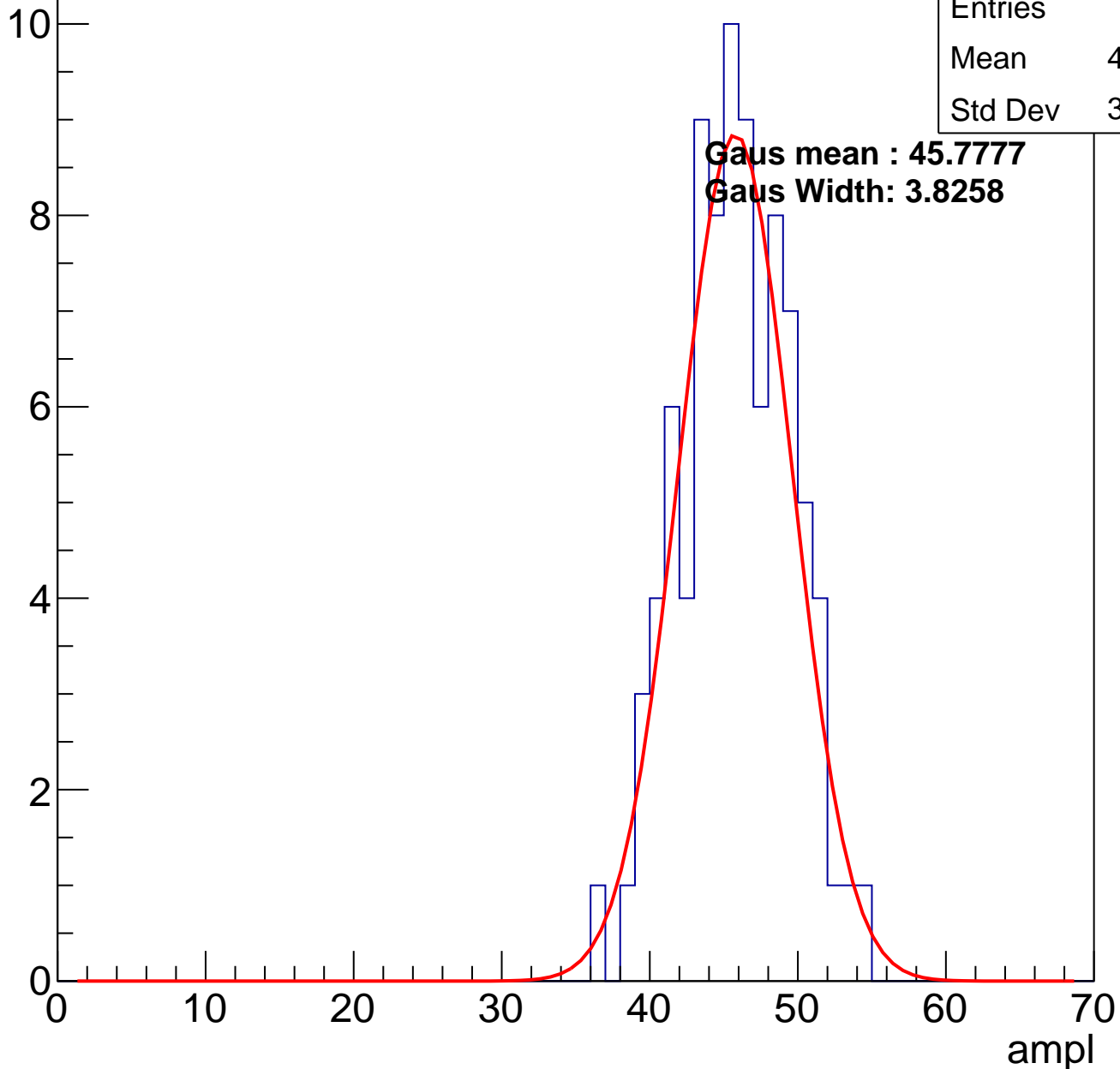
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	88
Mean	45.34
Std Dev	3.668

**Gaus mean : 45.7777**

**Gaus Width: 3.8258**

Entry

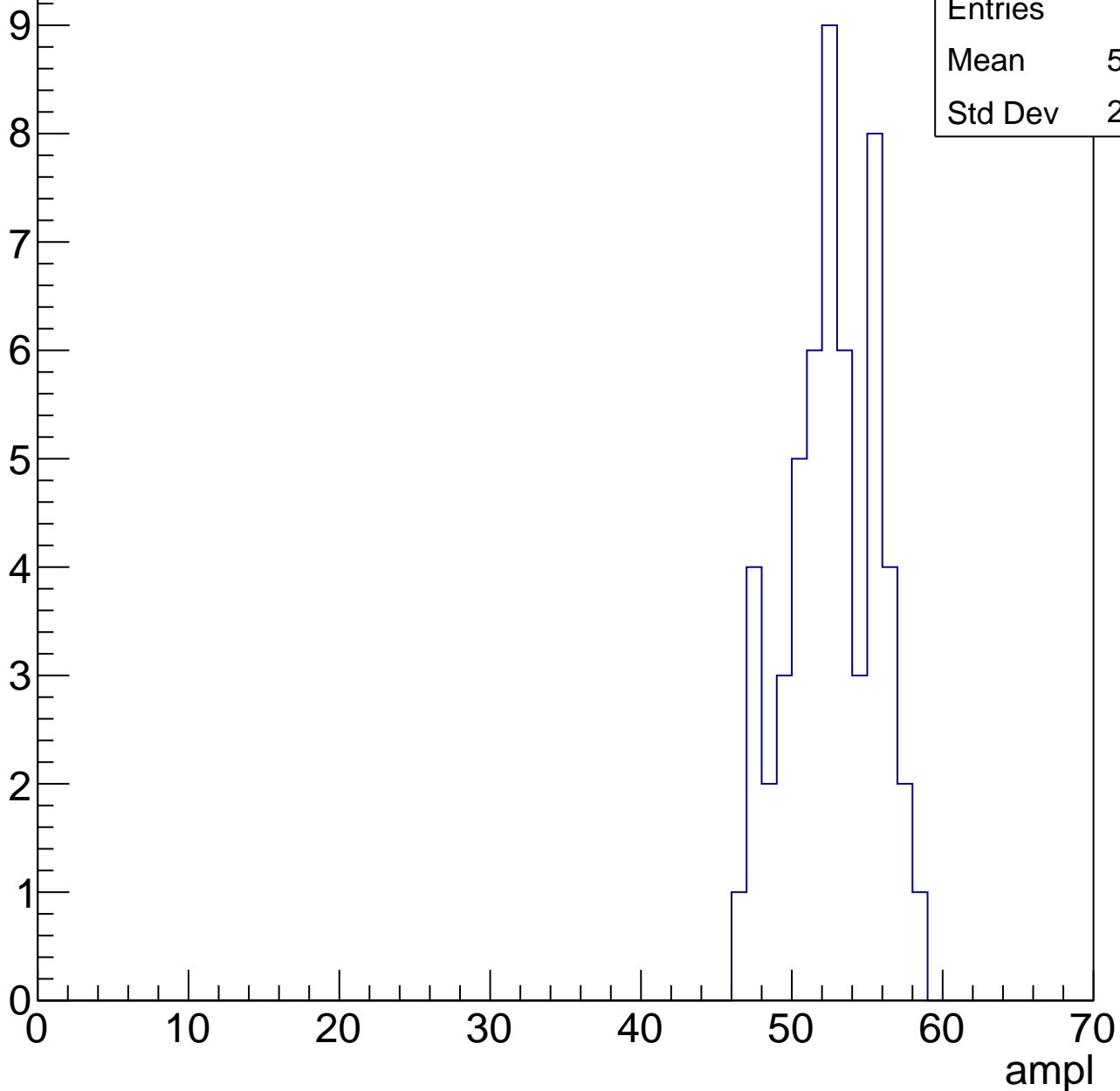


# B0L001S, U6-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	52.17
Std Dev	2.917

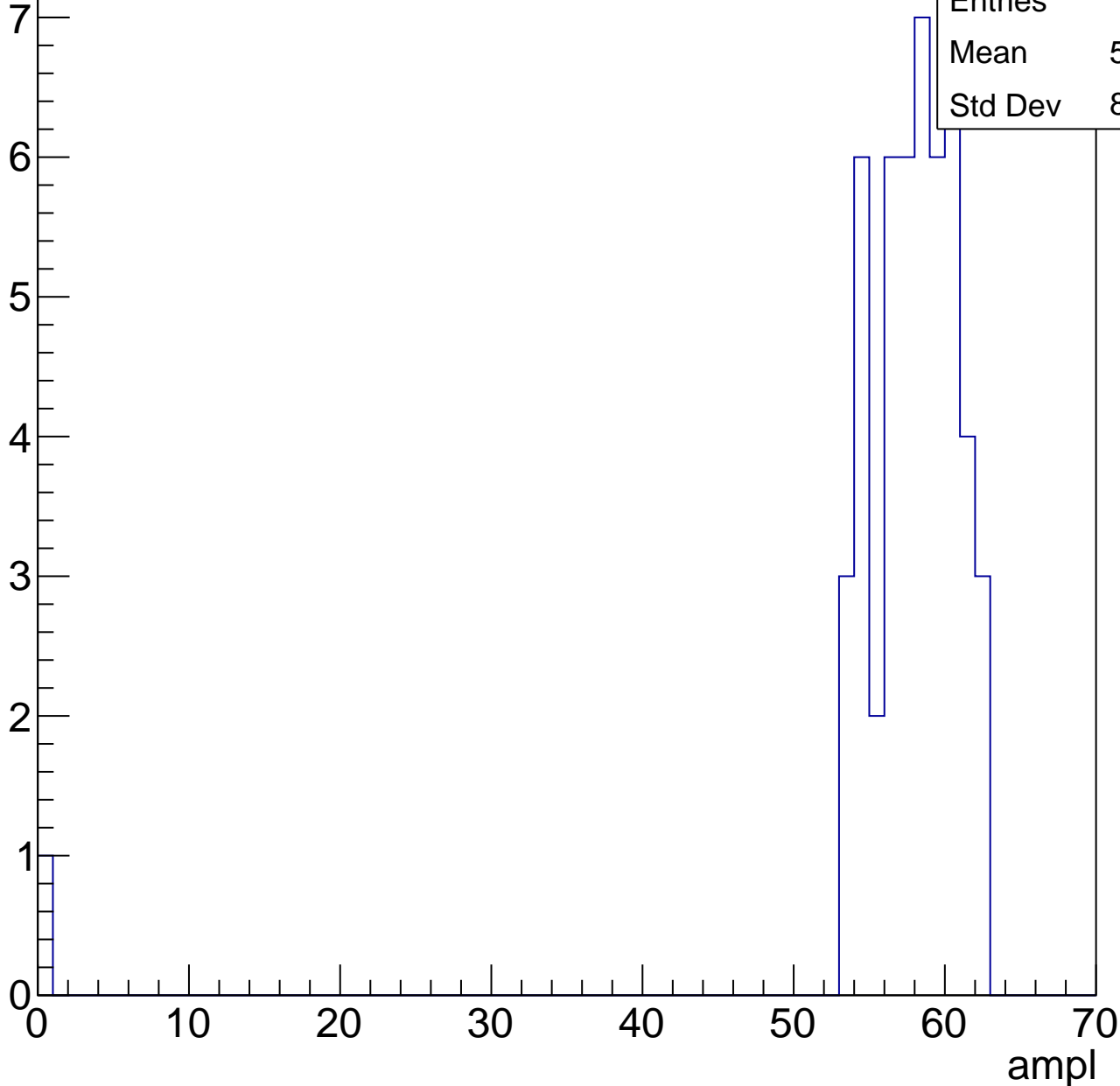


# B0L001S, U6-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	56.49
Std Dev	8.384



# B0L001S, U6-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	34
Mean	61.06
Std Dev	1.846

Entry

10

8

6

4

2

0

0

10

20

30

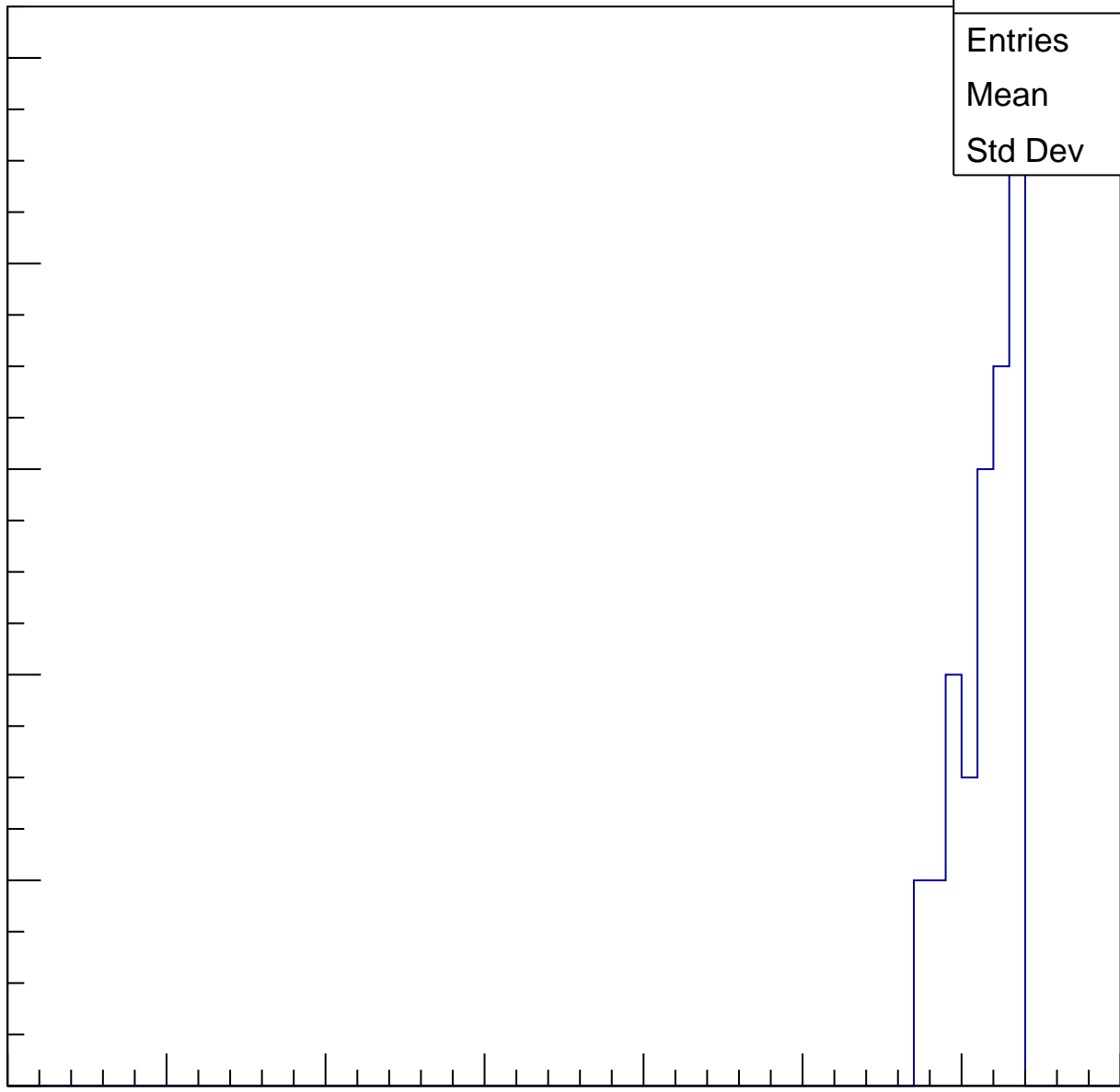
40

50

60

70

ampl



# B0L001S, U6-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U6-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U6-ch8, adc0

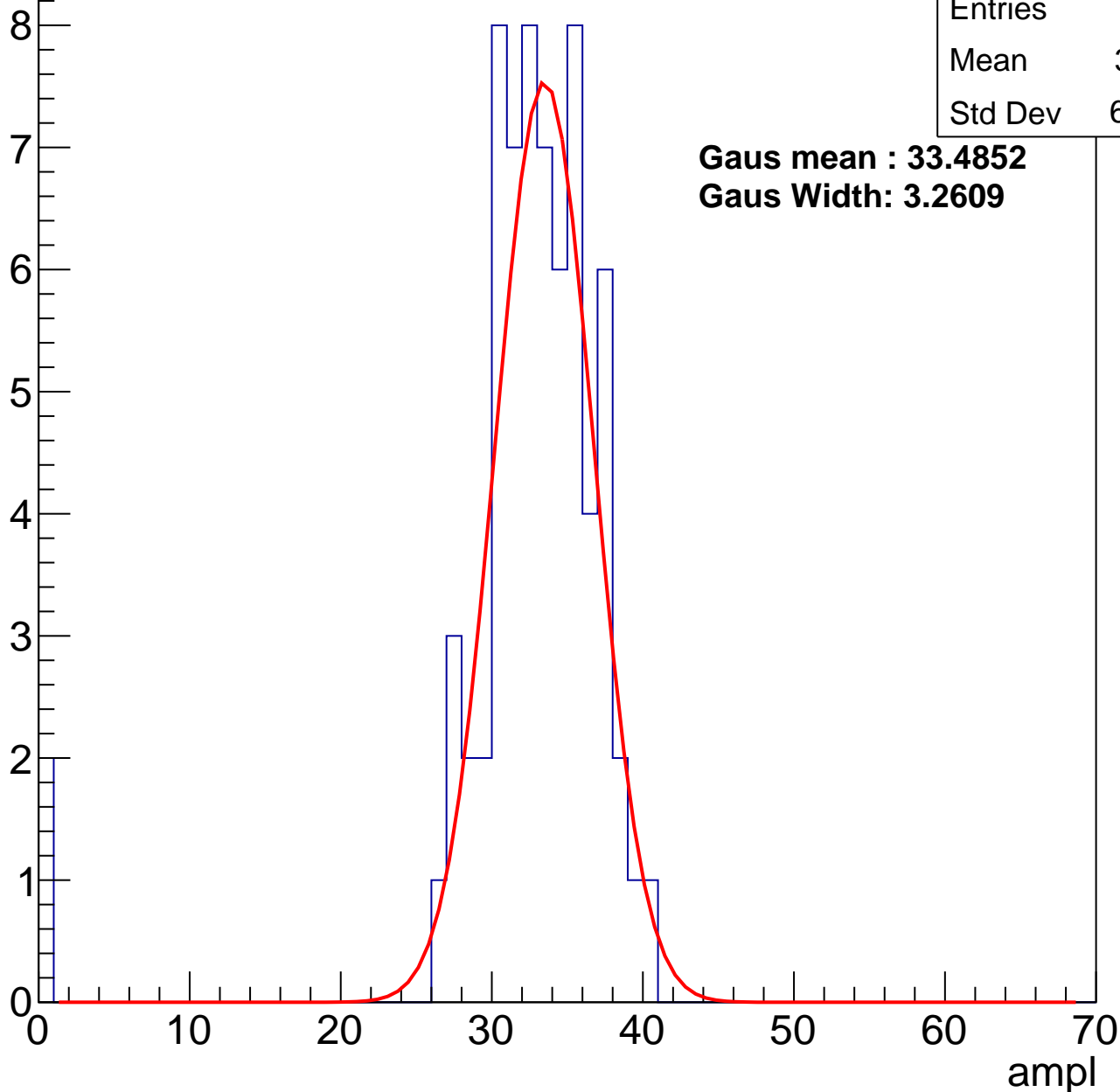
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	31.91
Std Dev	6.359

**Gaus mean : 33.4852**

**Gaus Width: 3.2609**



# B0L001S, U6-ch8, adc1

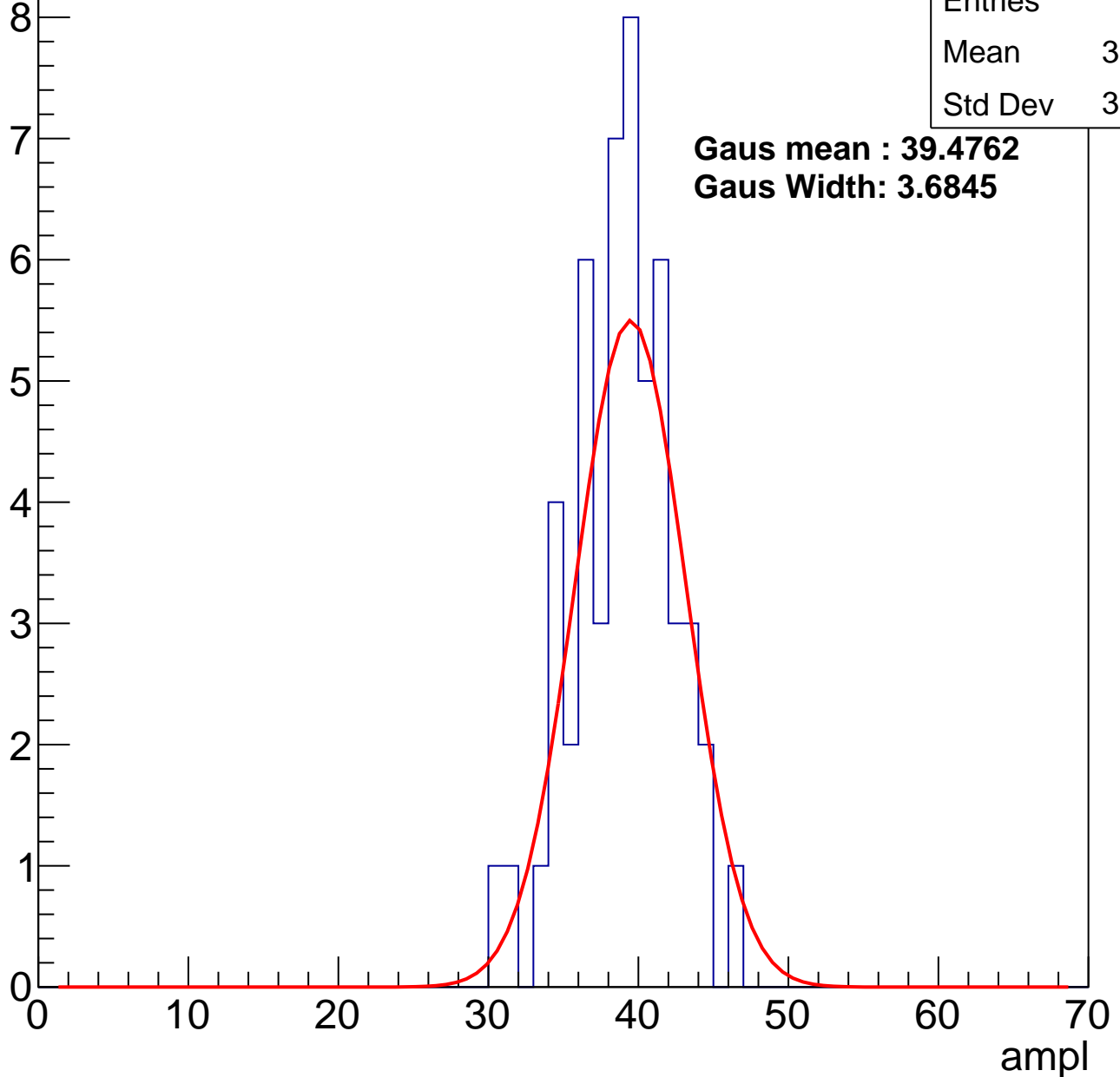
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	38.49
Std Dev	3.294

**Gaus mean : 39.4762**

**Gaus Width: 3.6845**



# B0L001S, U6-ch8, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	73
Mean	44.81
Std Dev	3.143

**Gaus mean : 45.3984**

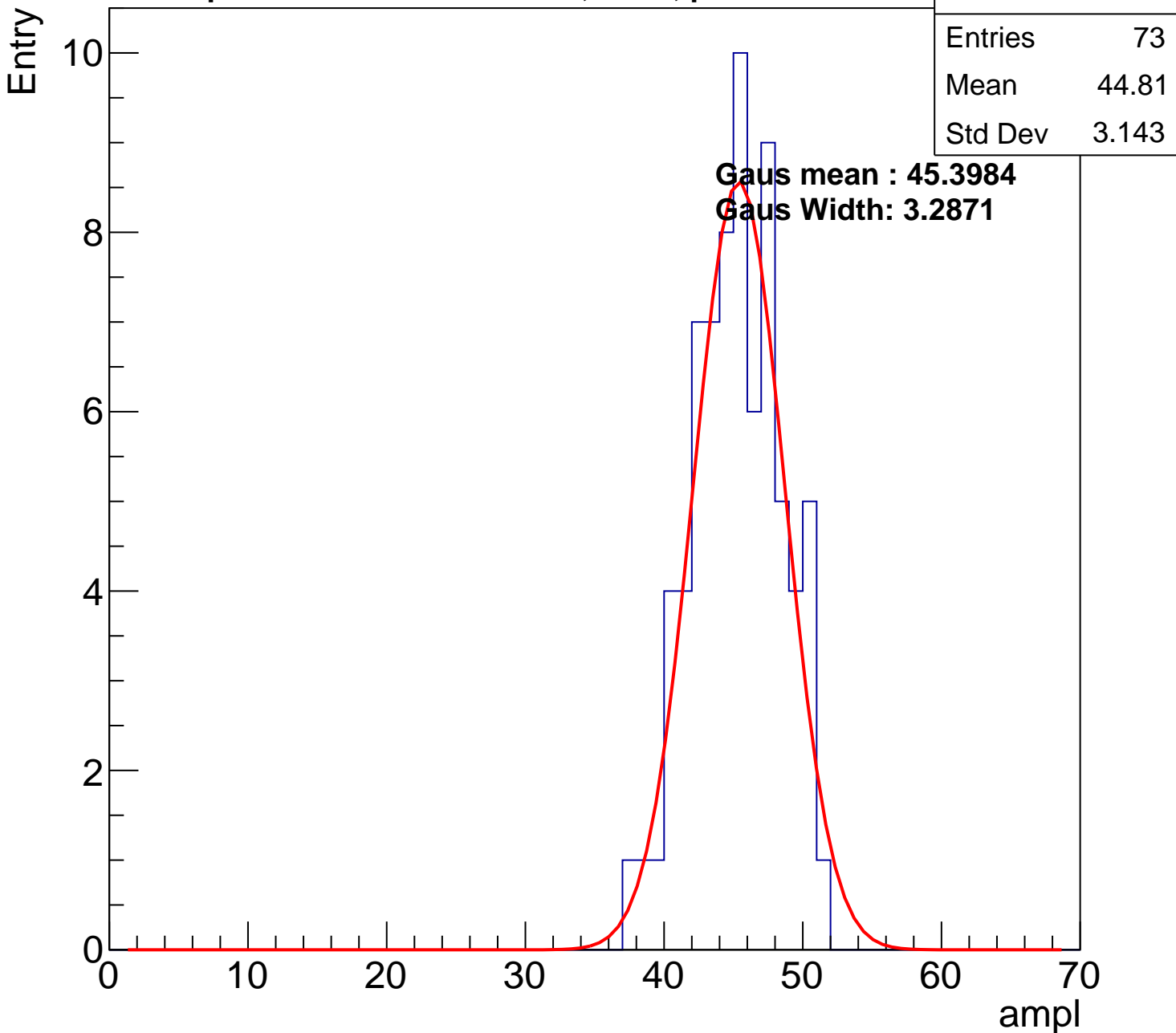
**Gaus Width: 3.2871**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

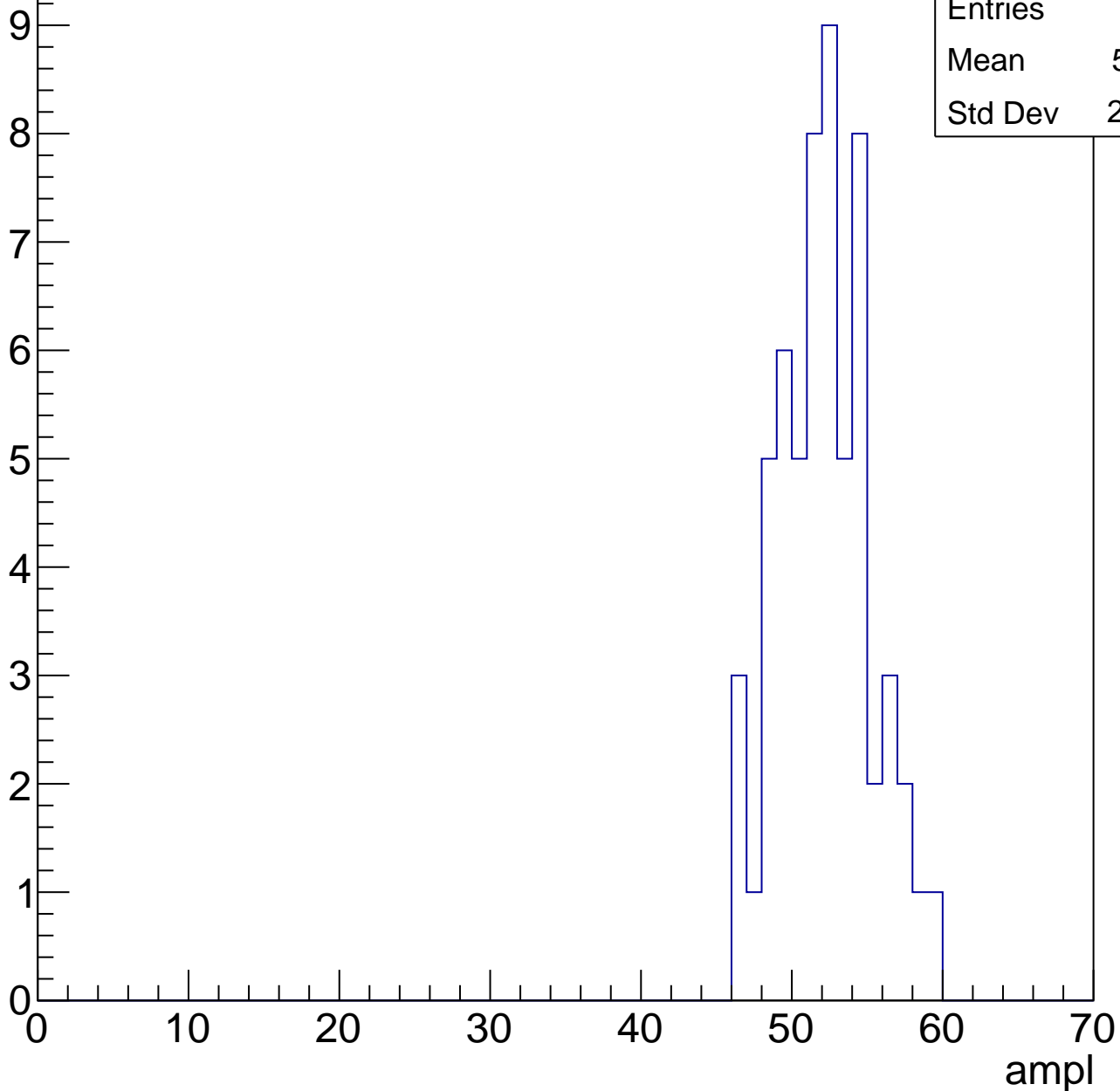


# B0L001S, U6-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	51.71
Std Dev	2.992



# B0L001S, U6-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	46
Mean	56.48
Std Dev	2.517

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

7

8

# B0L001S, U6-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	44
Mean	59.45
Std Dev	9.228

Entry

10

8

6

4

2

0

0

10

20

30

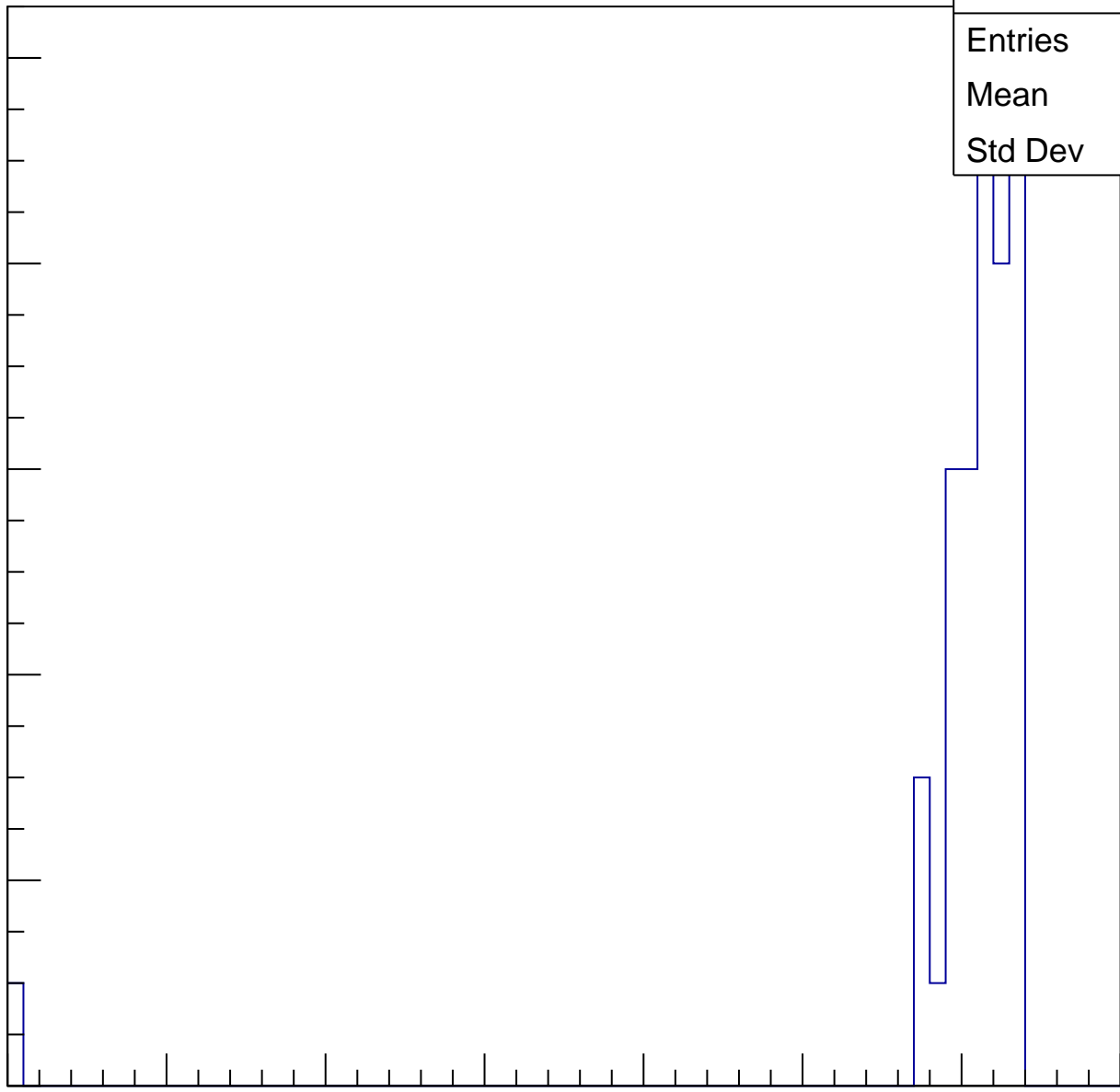
40

50

60

70

ampl



# B0L001S, U6-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U6-ch9, adc0

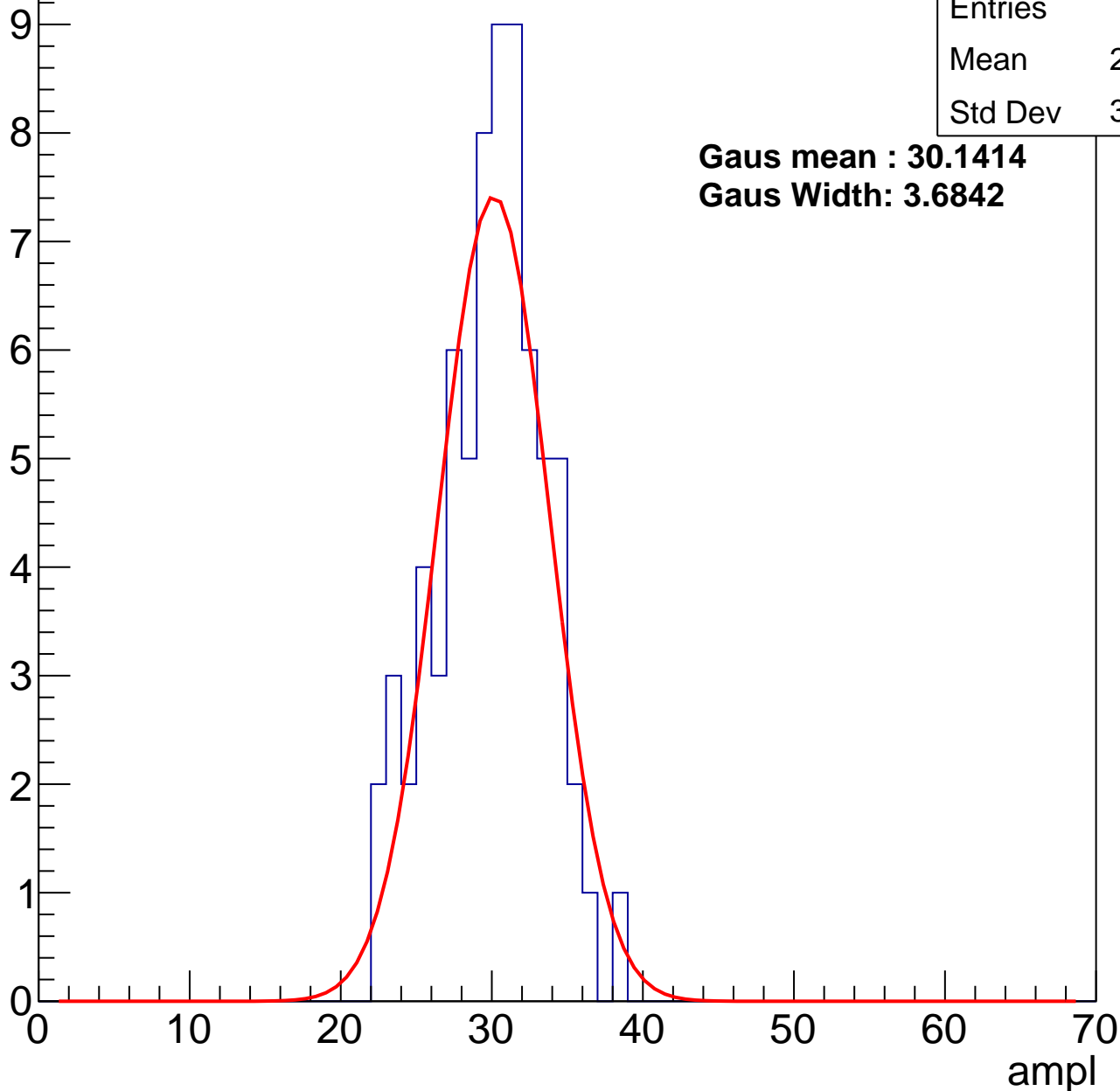
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	29.48
Std Dev	3.492

**Gaus mean : 30.1414**

**Gaus Width: 3.6842**



# B0L001S, U6-ch9, adc1

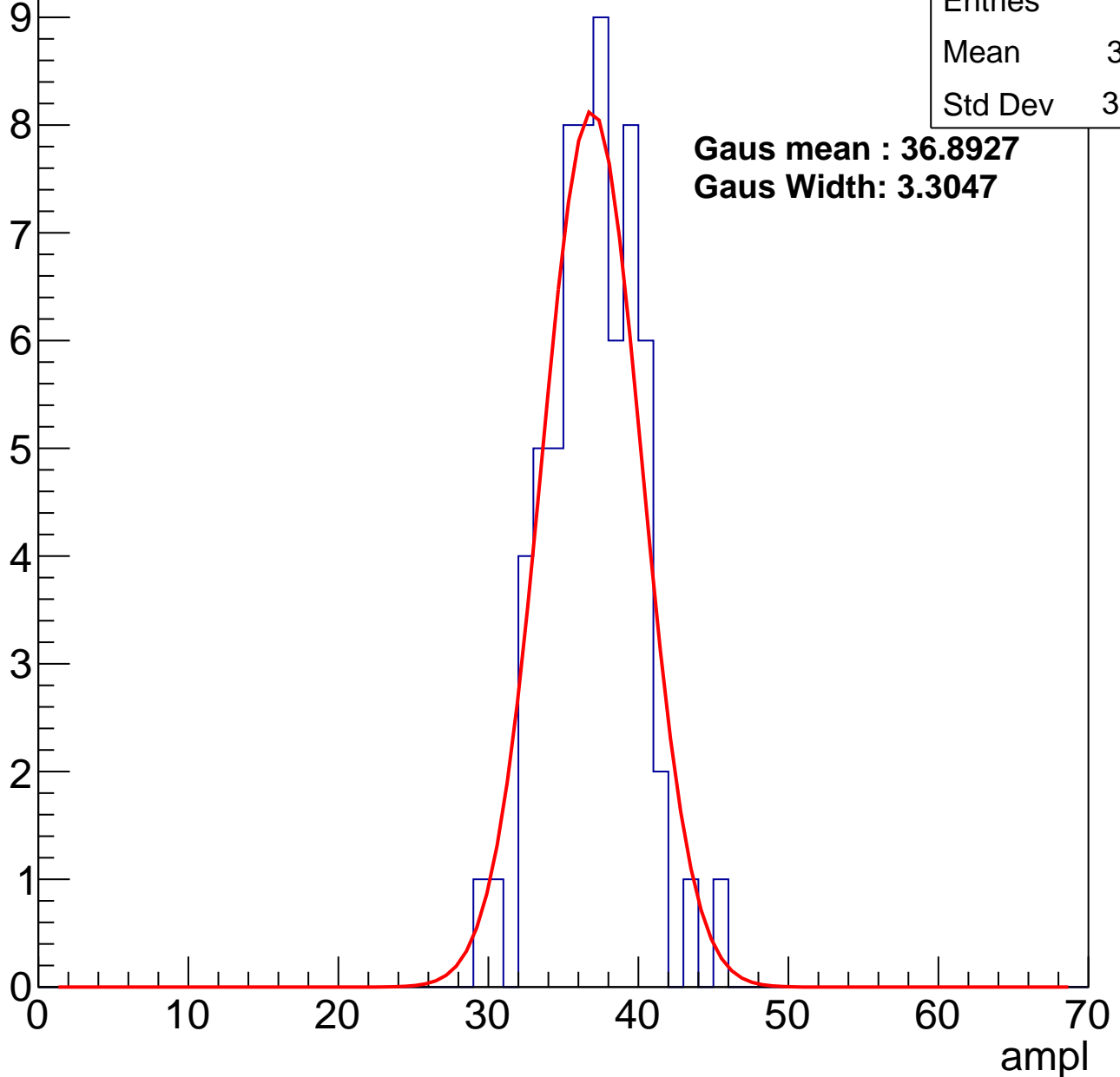
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	36.51
Std Dev	3.003

**Gaus mean : 36.8927**

**Gaus Width: 3.3047**



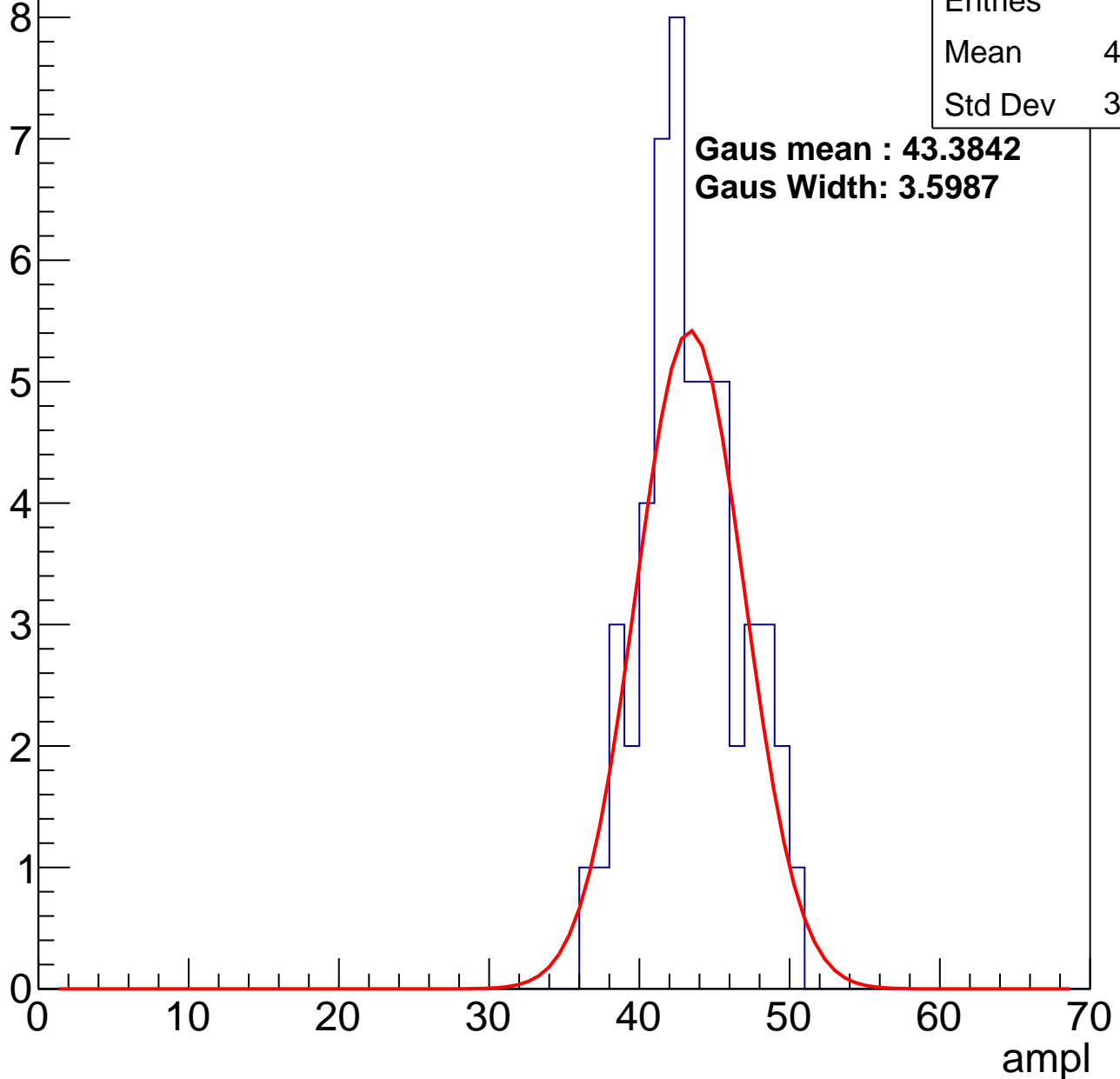
# B0L001S, U6-ch9, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	42.94
Std Dev	3.255

**Gaus mean : 43.3842**  
**Gaus Width: 3.5987**

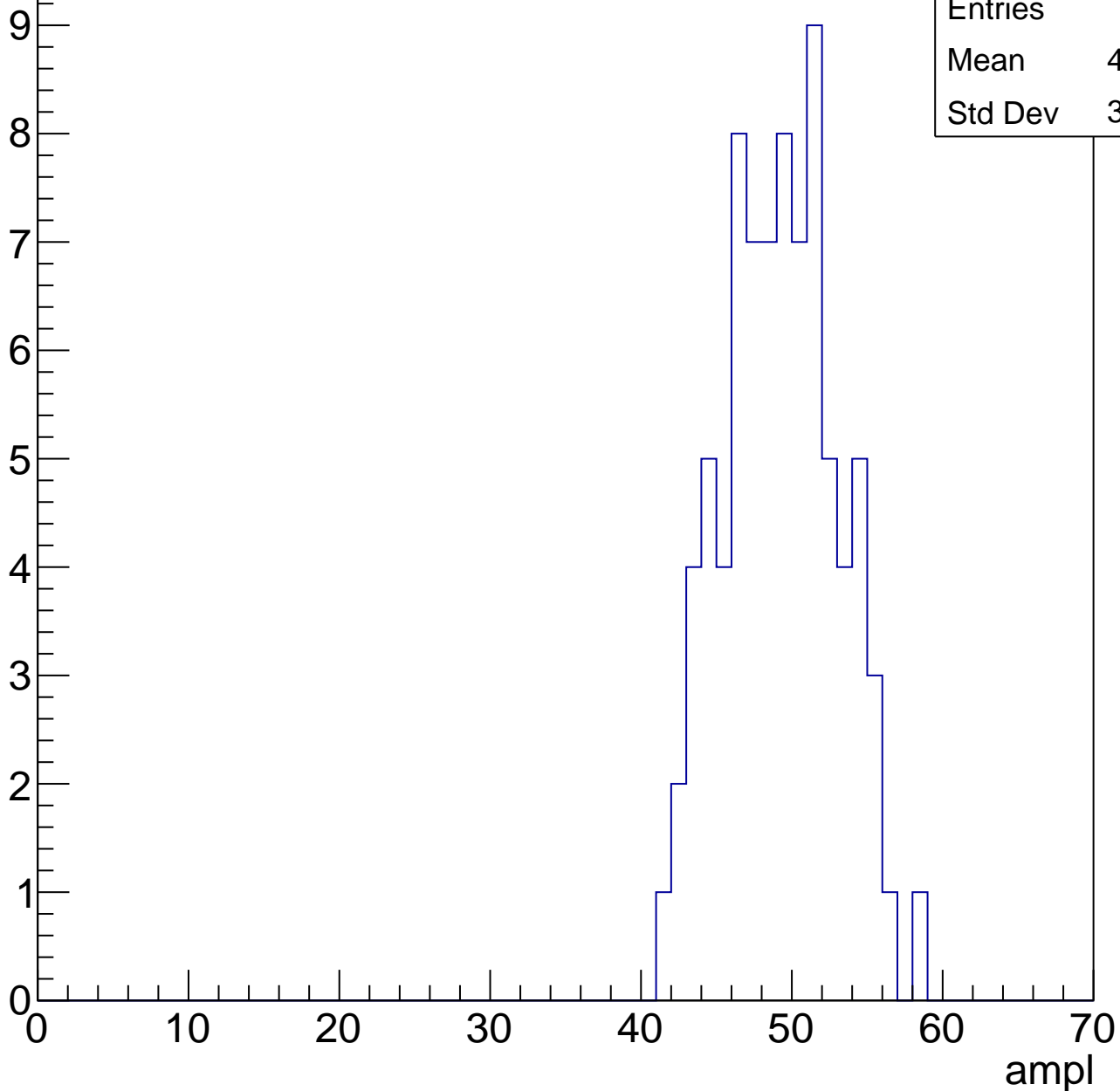


# B0L001S, U6-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	48.79
Std Dev	3.708



# B0L001S, U6-ch9, adc4

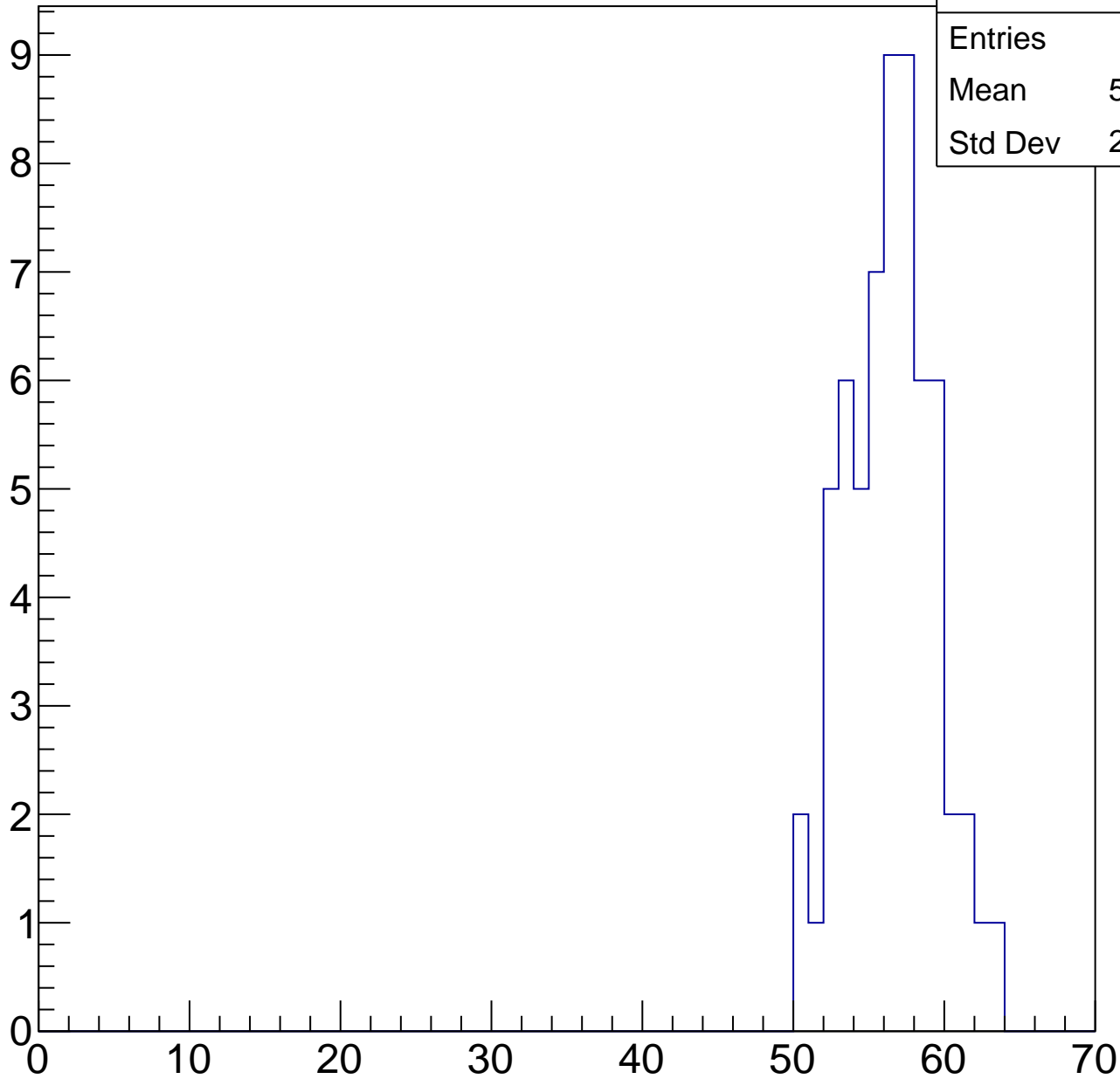
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	62
Mean	55.97
Std Dev	2.874

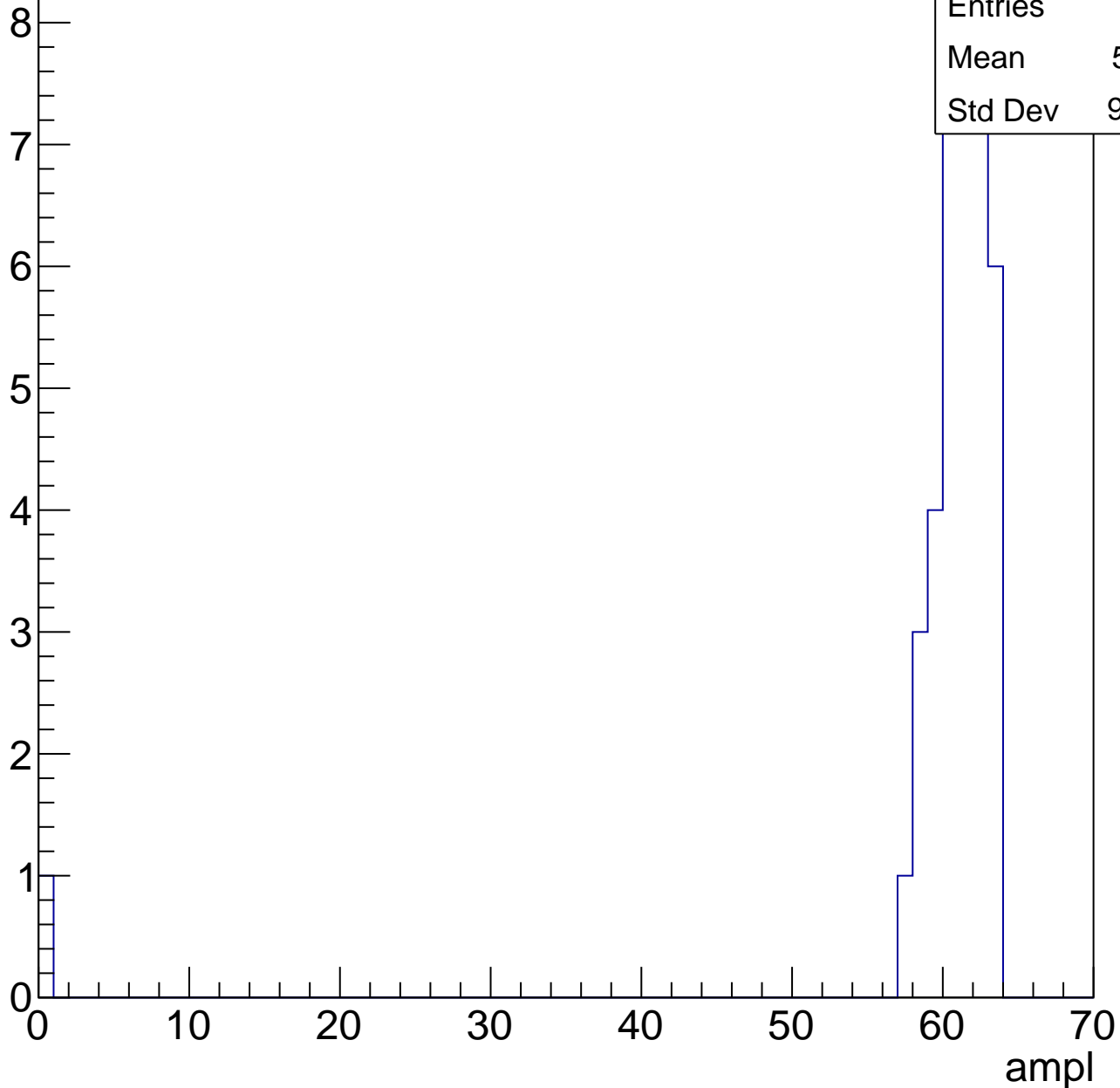
ampl



# B0L001S, U6-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U6-ch10, adc0

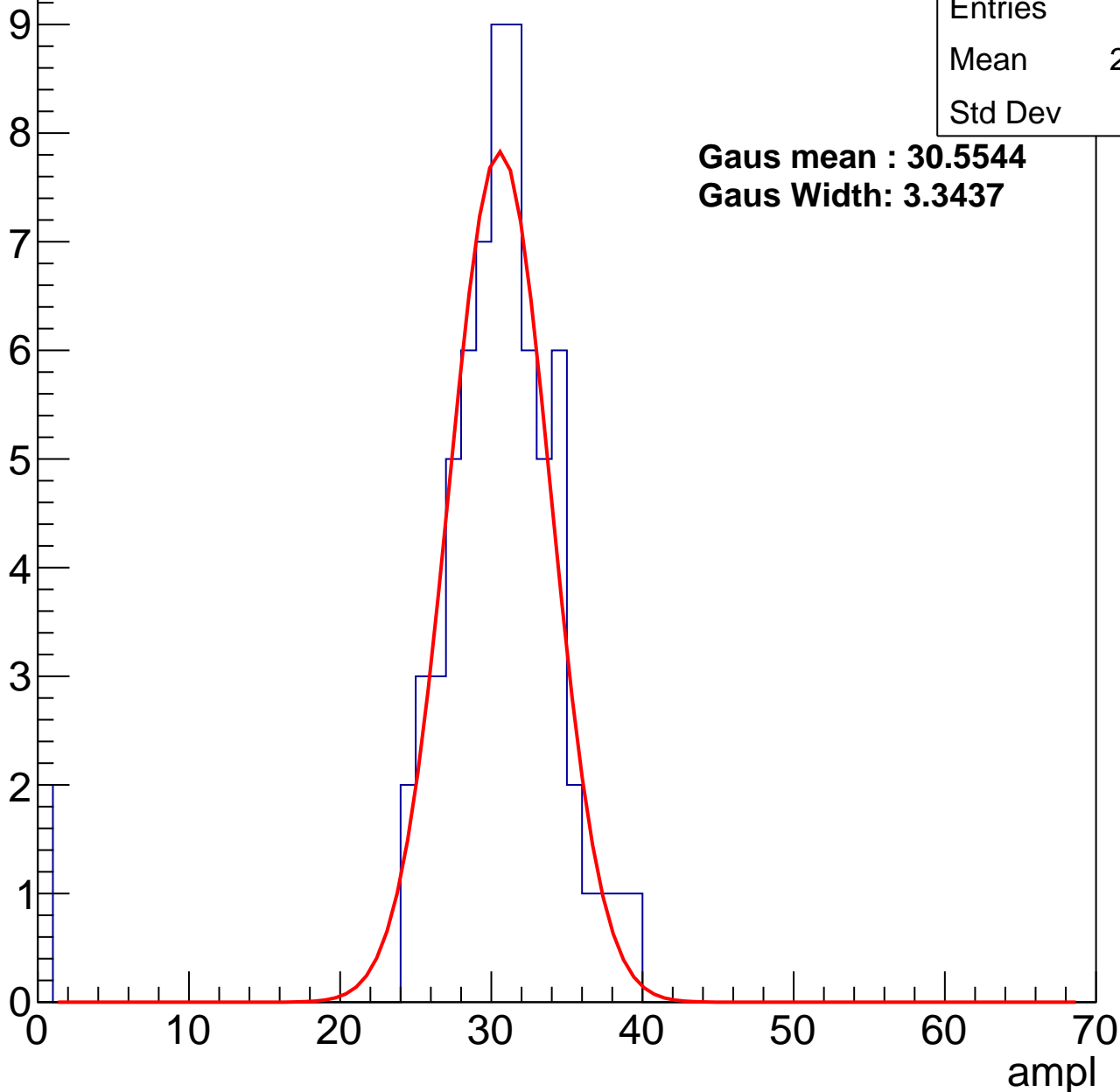
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	29.52
Std Dev	6.03

**Gaus mean : 30.5544**

**Gaus Width: 3.3437**



# B0L001S, U6-ch10, adc1

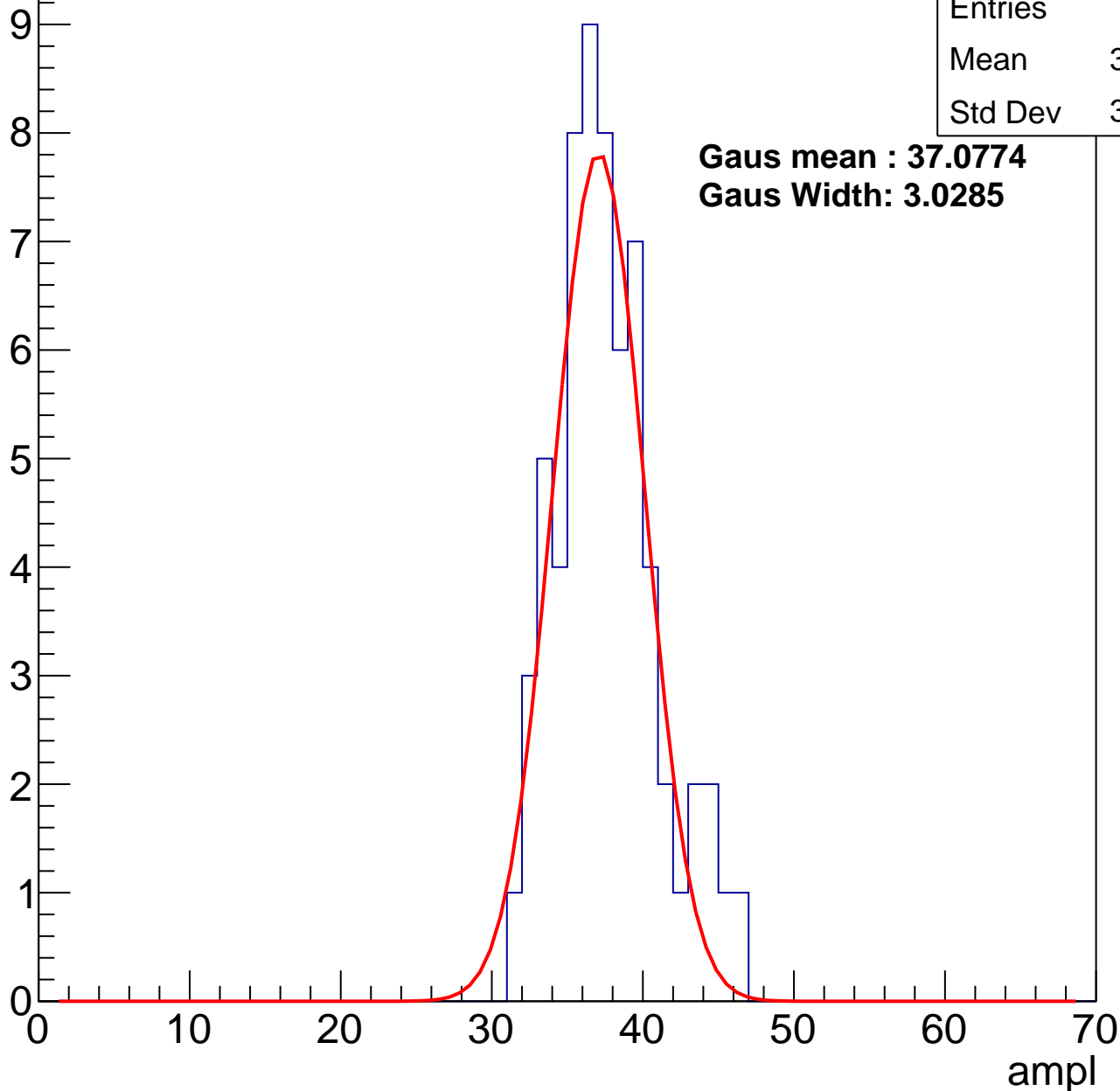
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	37.16
Std Dev	3.327

**Gaus mean : 37.0774**

**Gaus Width: 3.0285**



# B0L001S, U6-ch10, adc2

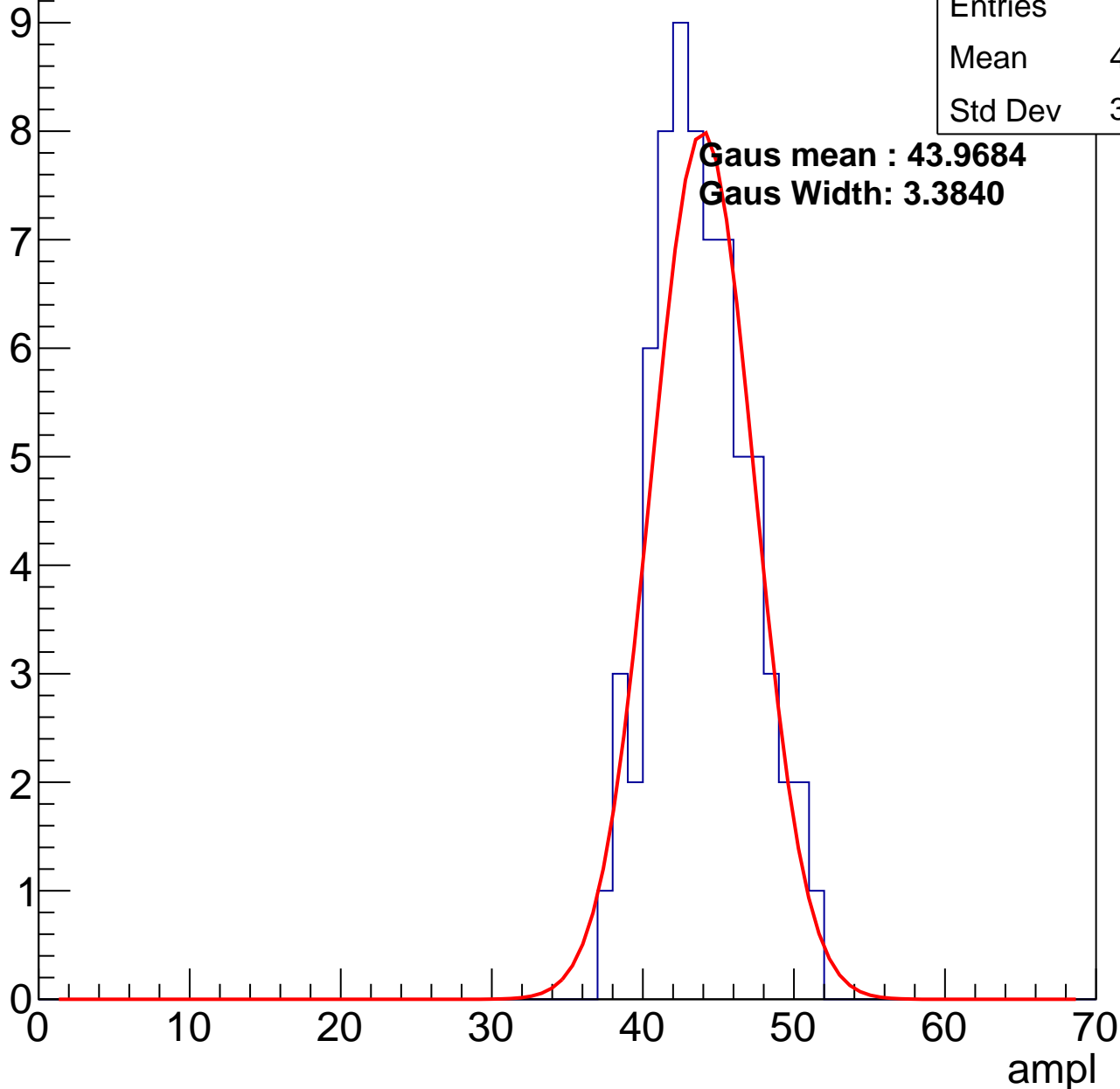
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	43.48
Std Dev	3.165

**Gaus mean : 43.9684**

**Gaus Width: 3.3840**

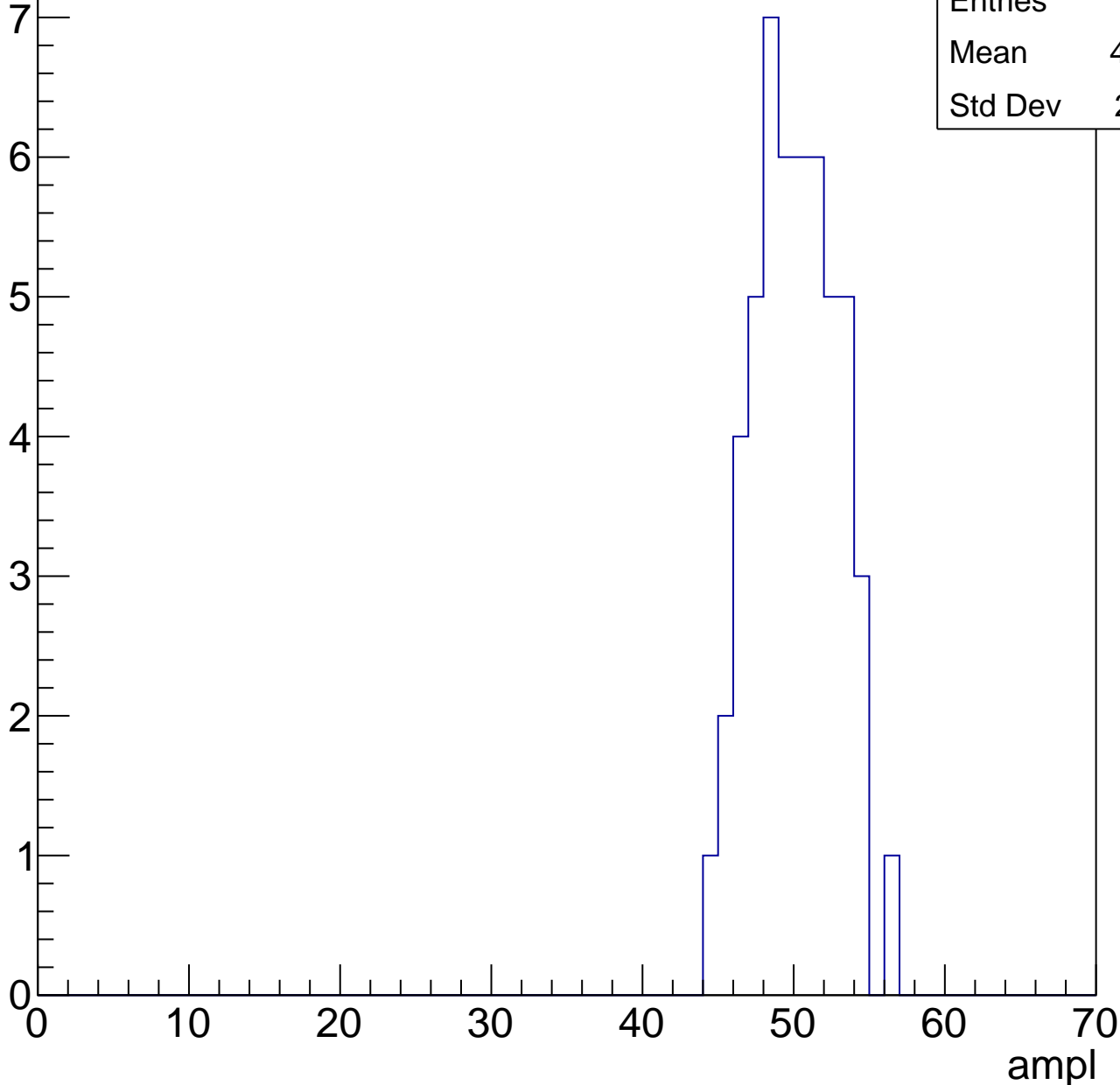


# B0L001S, U6-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	49.65
Std Dev	2.721

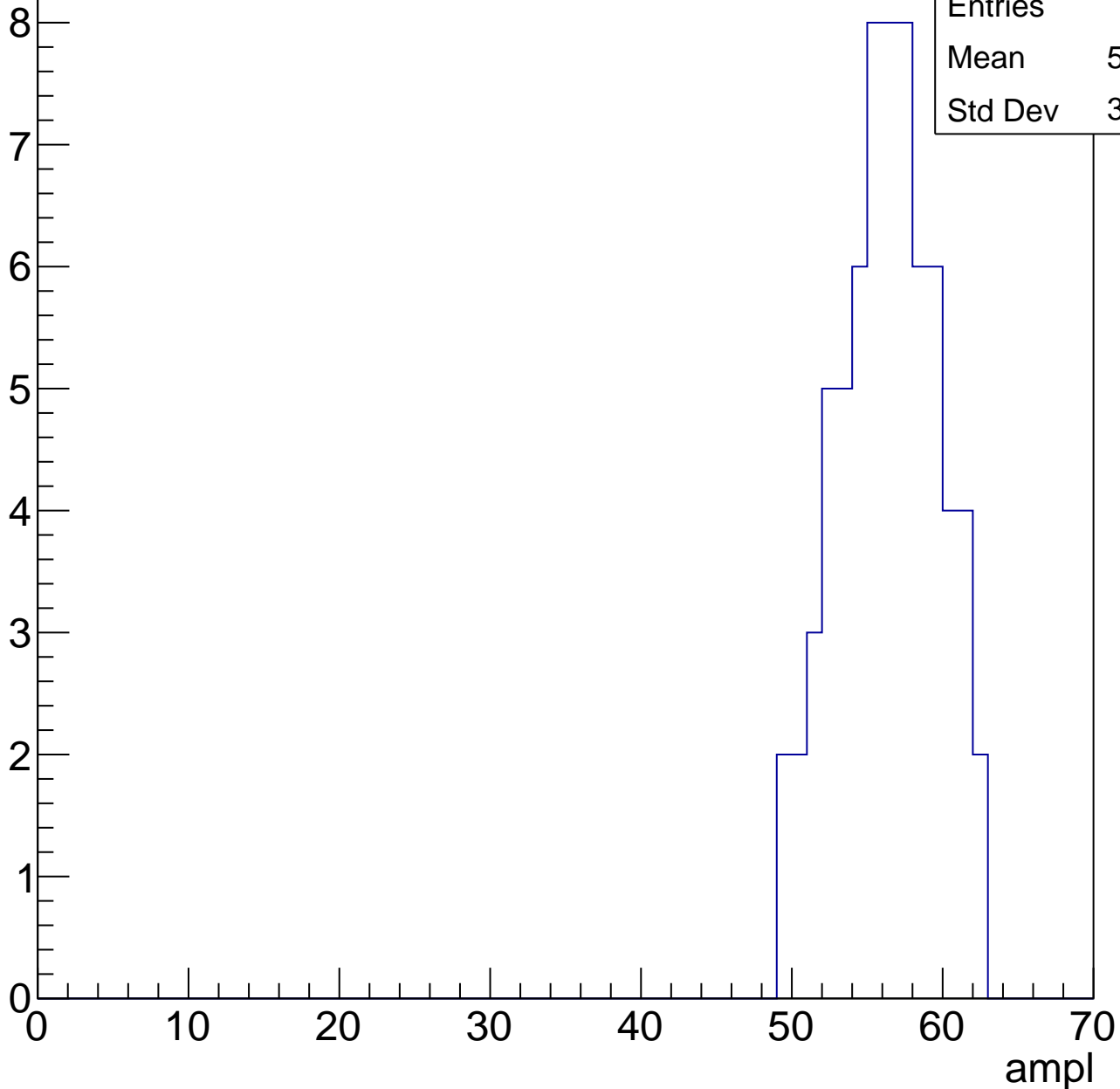


# B0L001S, U6-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	55.86
Std Dev	3.236

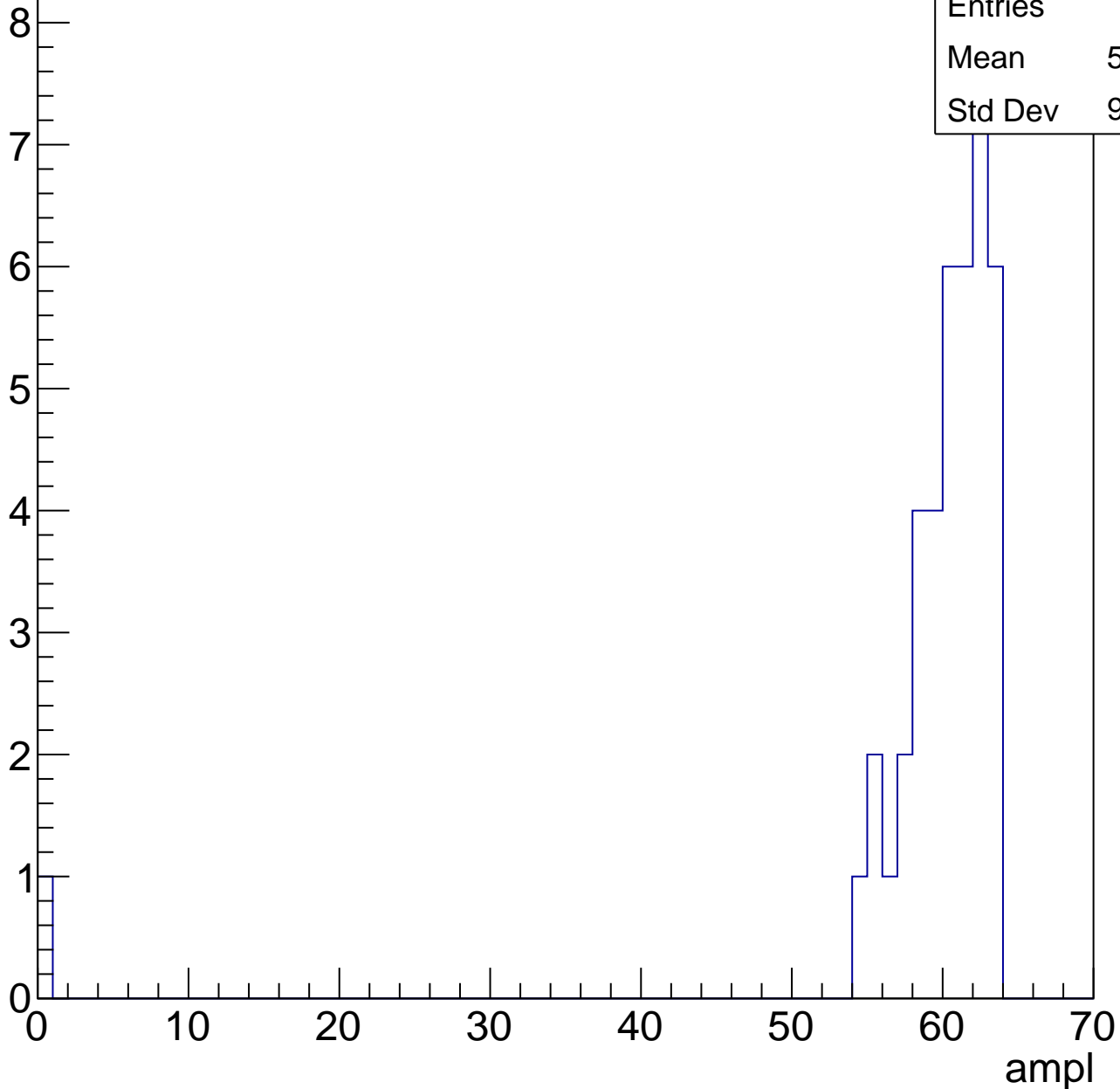


# B0L001S, U6-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	41
Mean	58.59
Std Dev	9.564



# B0L001S, U6-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U6-ch11, adc0

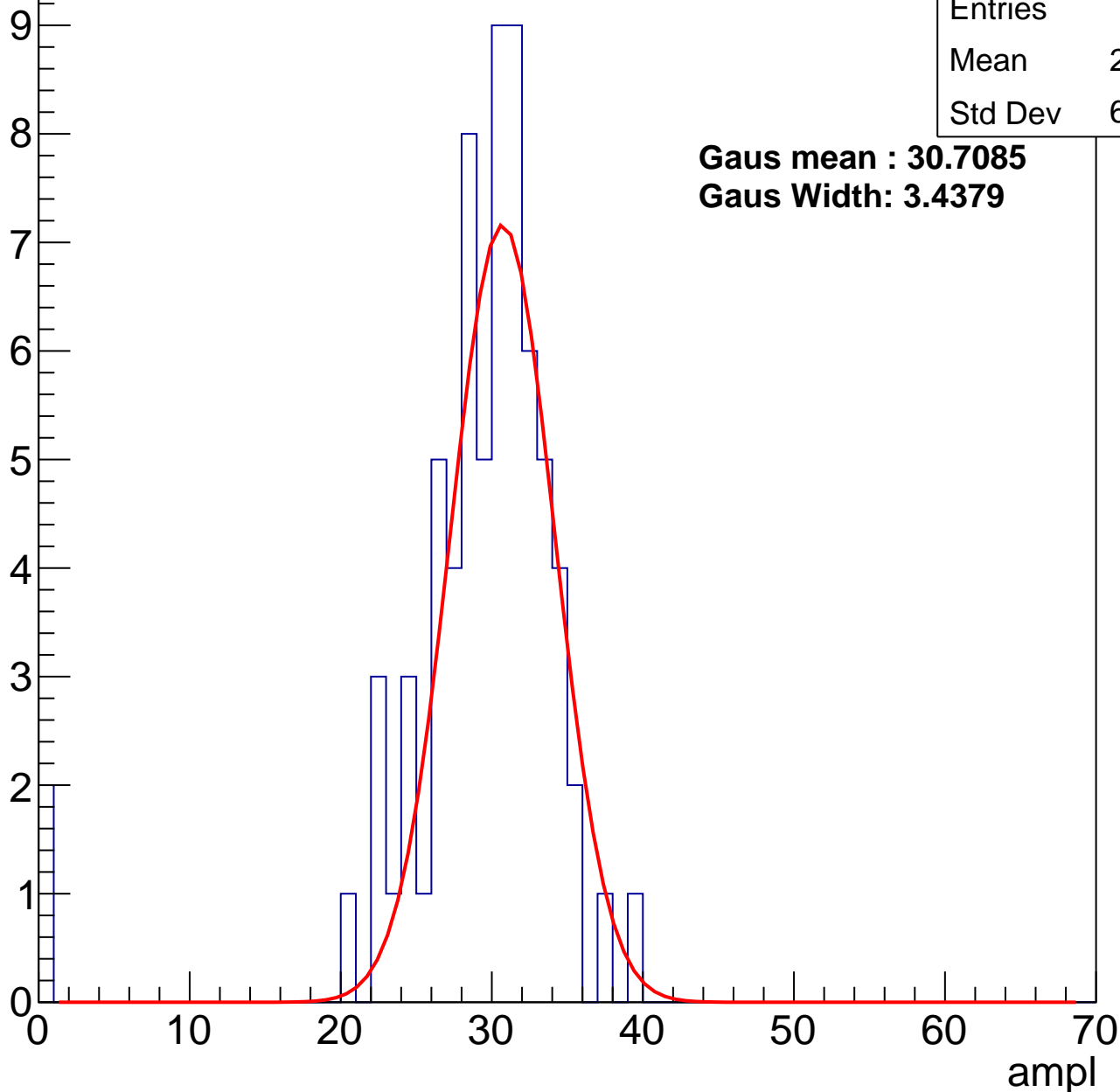
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	28.59
Std Dev	6.105

**Gaus mean : 30.7085**

**Gaus Width: 3.4379**



# B0L001S, U6-ch11, adc1

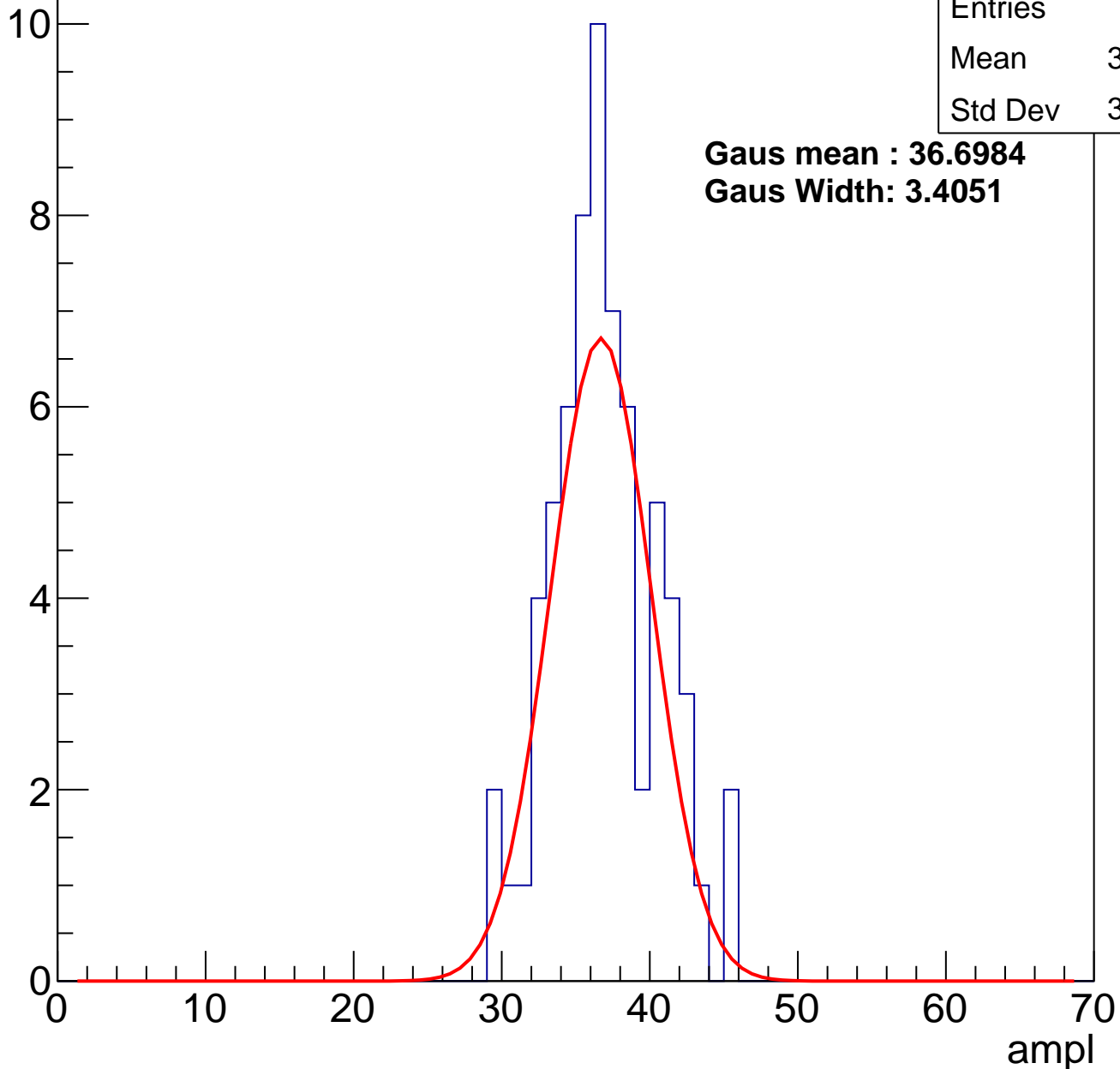
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	67
Mean	36.48
Std Dev	3.525

**Gaus mean : 36.6984**

**Gaus Width: 3.4051**

Entry



# B0L001S, U6-ch11, adc2

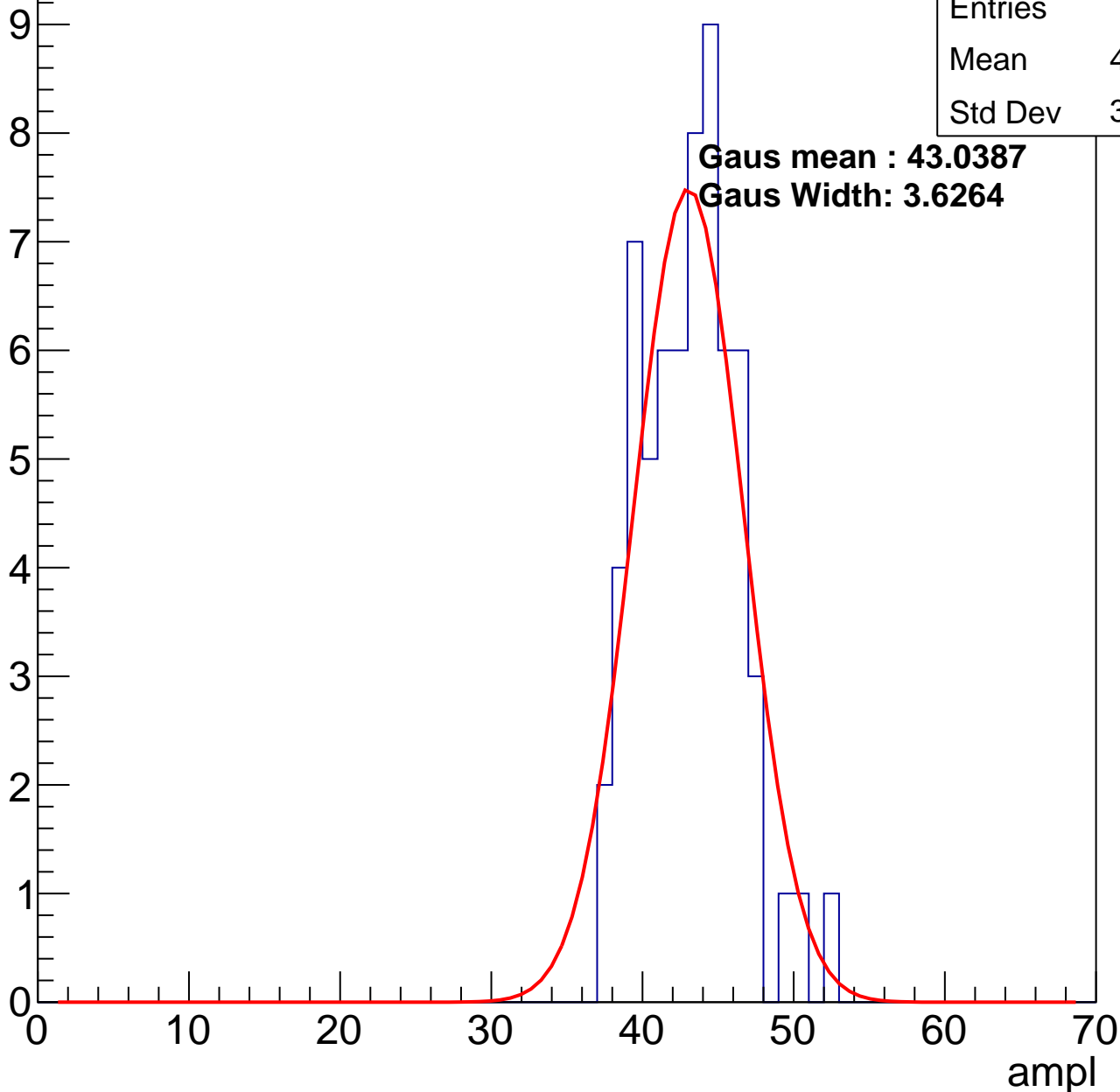
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	42.69
Std Dev	3.172

**Gaus mean : 43.0387**

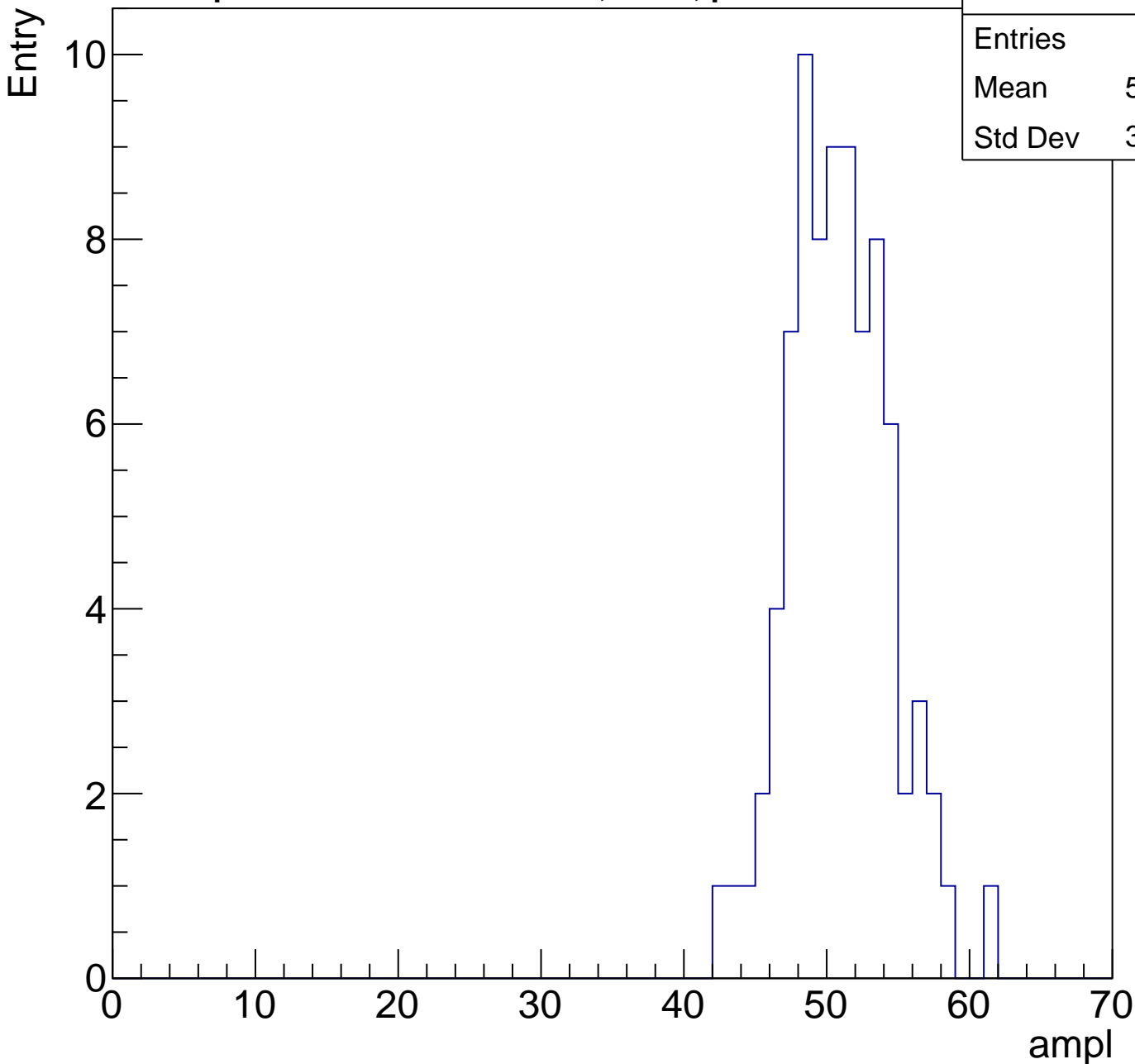
**Gaus Width: 3.6264**



# B0L001S, U6-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	82
Mean	50.44
Std Dev	3.499

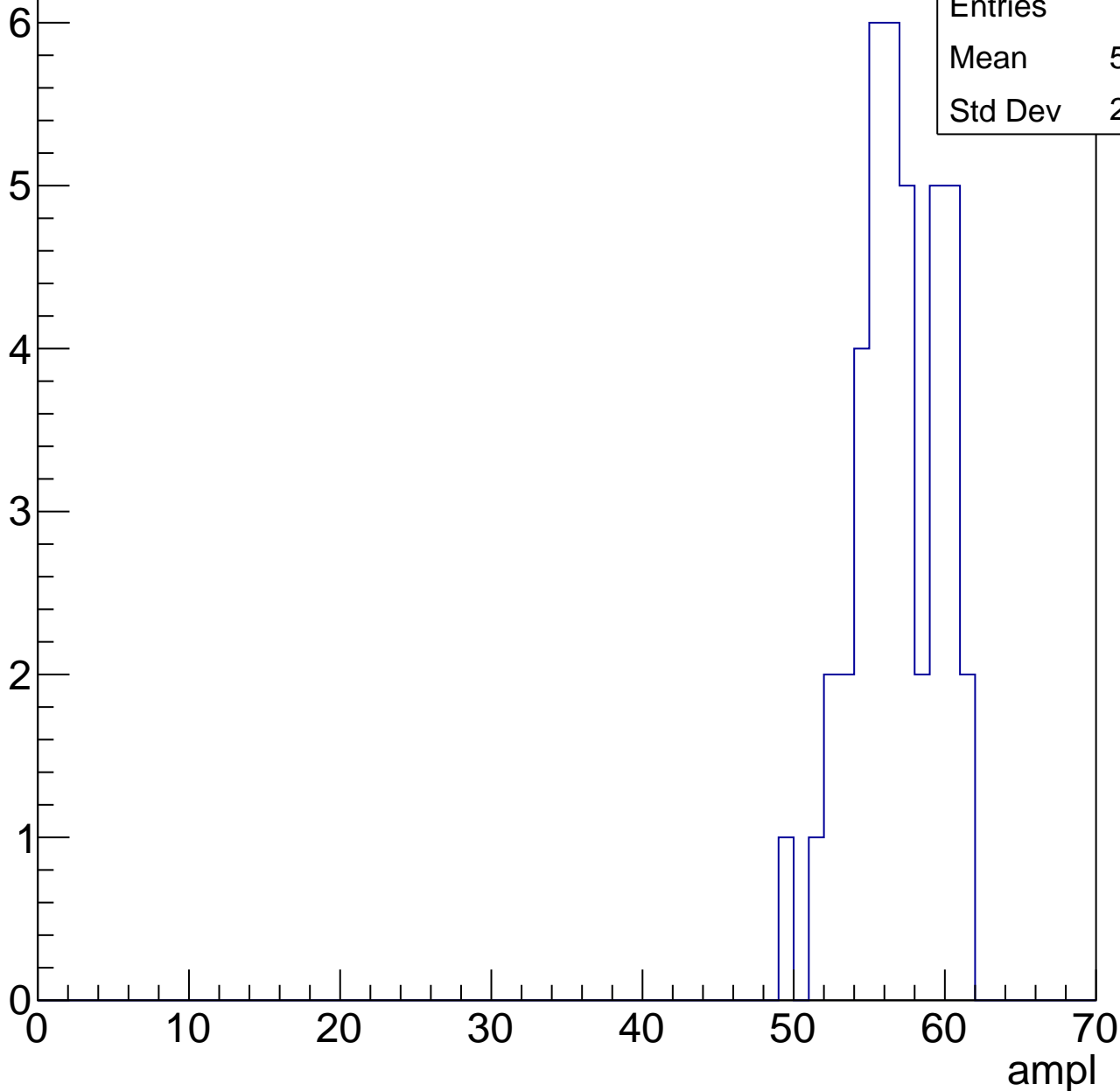


# B0L001S, U6-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	41
Mean	56.34
Std Dev	2.834

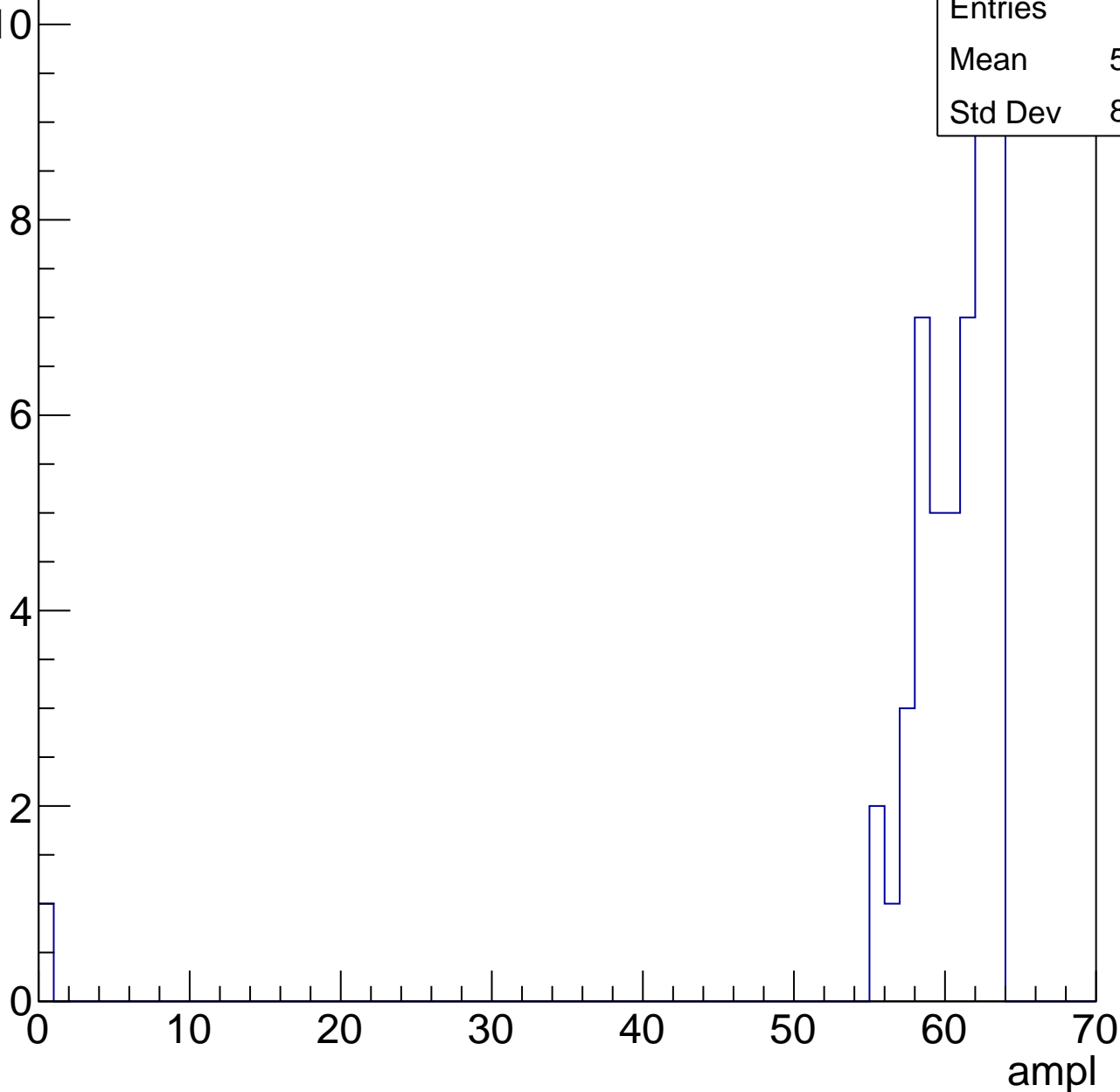


# B0L001S, U6-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	59.06
Std Dev	8.735



# B0L001S, U6-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U6-ch12, adc0

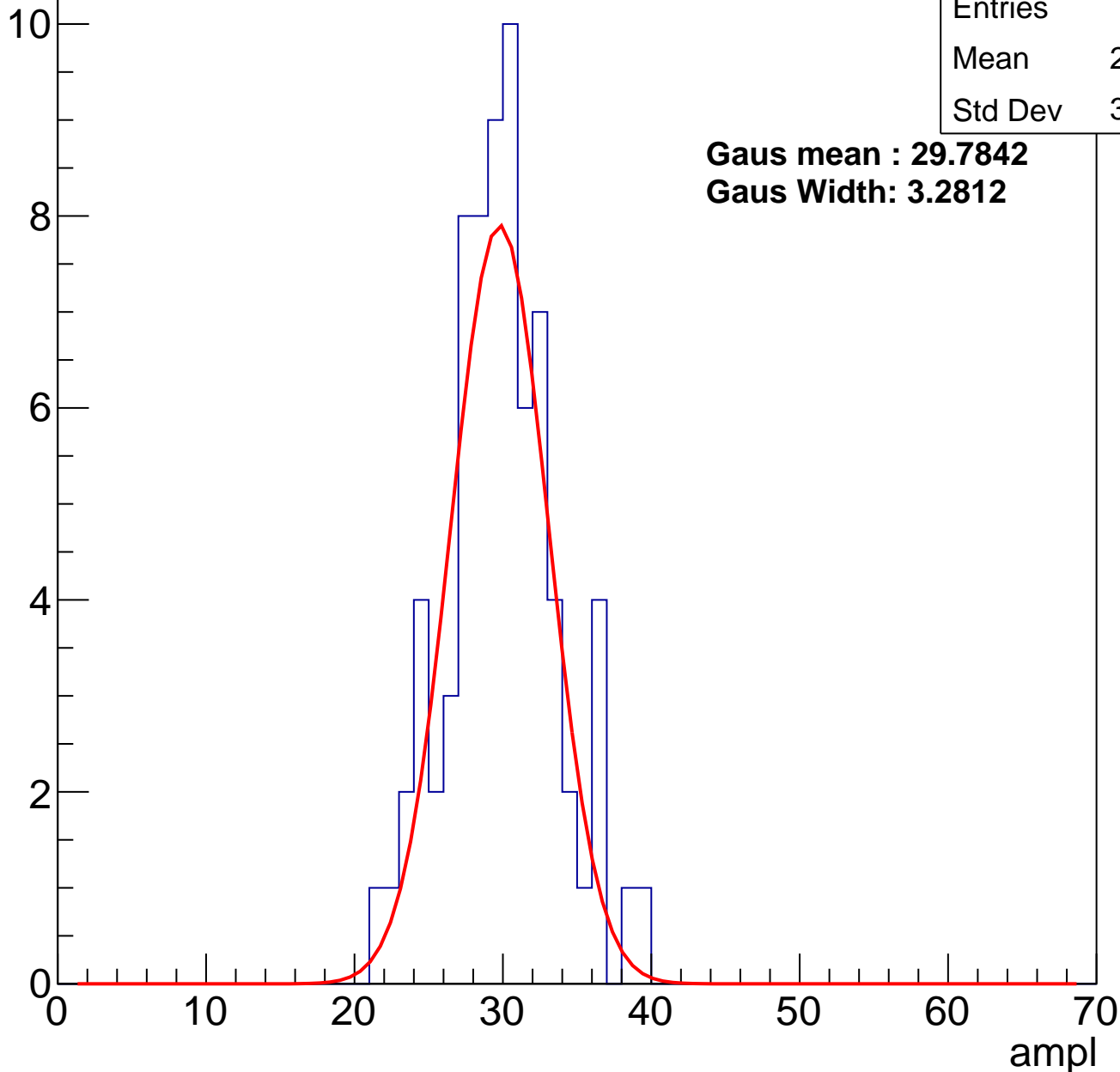
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	74
Mean	29.46
Std Dev	3.662

**Gaus mean : 29.7842**

**Gaus Width: 3.2812**

Entry



# B0L001S, U6-ch12, adc1

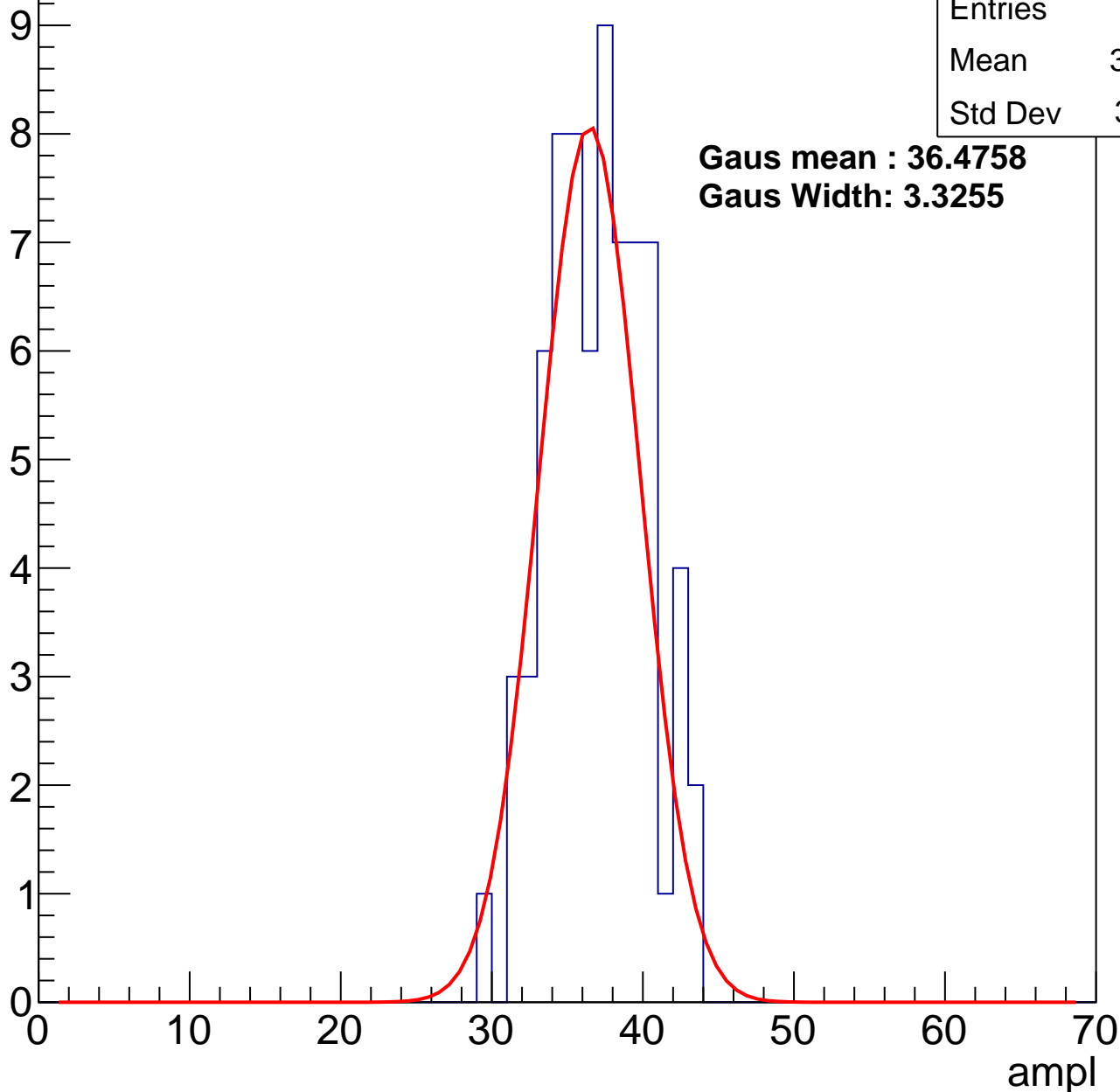
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	36.54
Std Dev	3.171

**Gaus mean : 36.4758**

**Gaus Width: 3.3255**



# B0L001S, U6-ch12, adc2

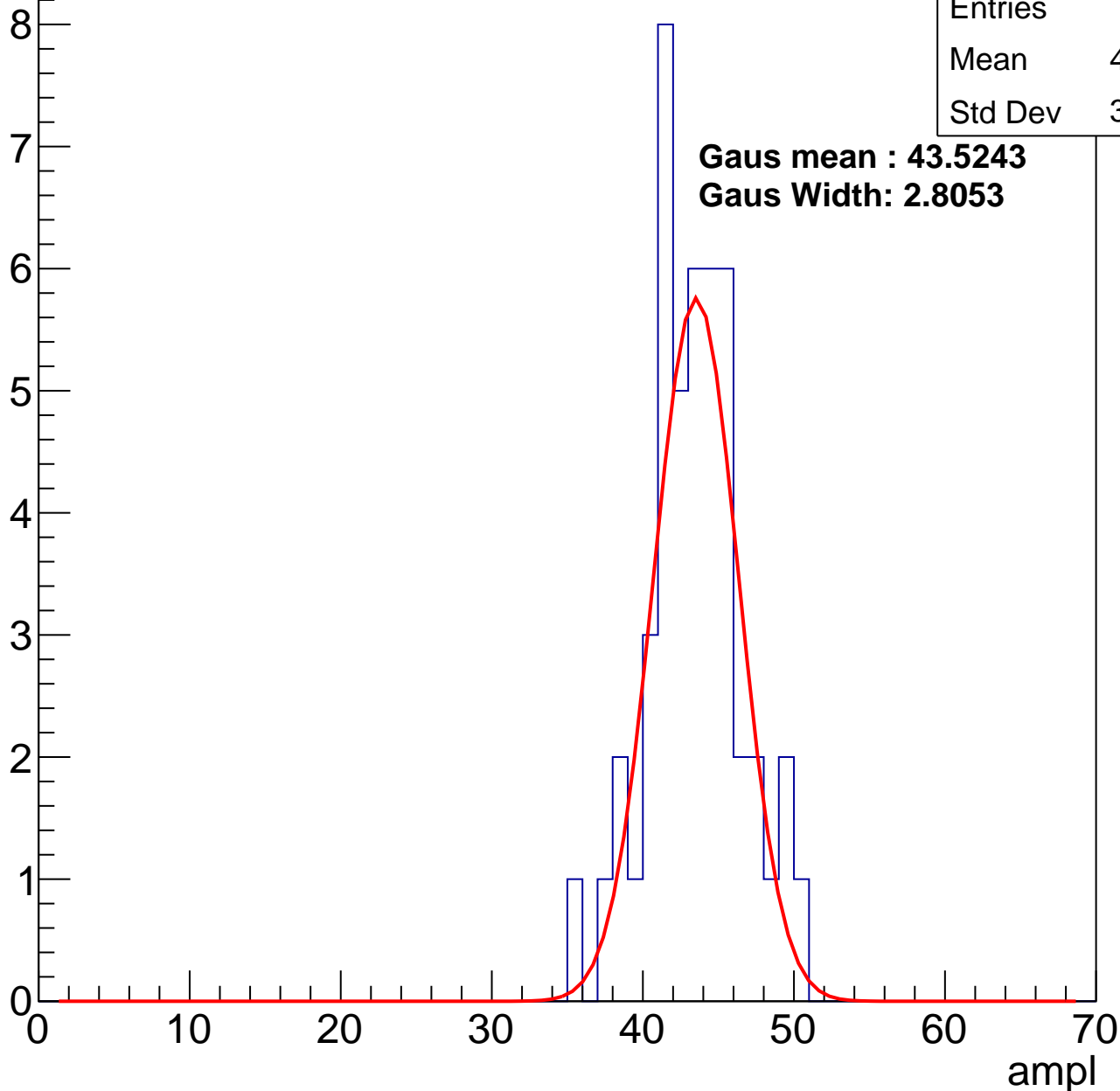
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	42.96
Std Dev	3.115

**Gaus mean : 43.5243**

**Gaus Width: 2.8053**



# B0L001S, U6-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

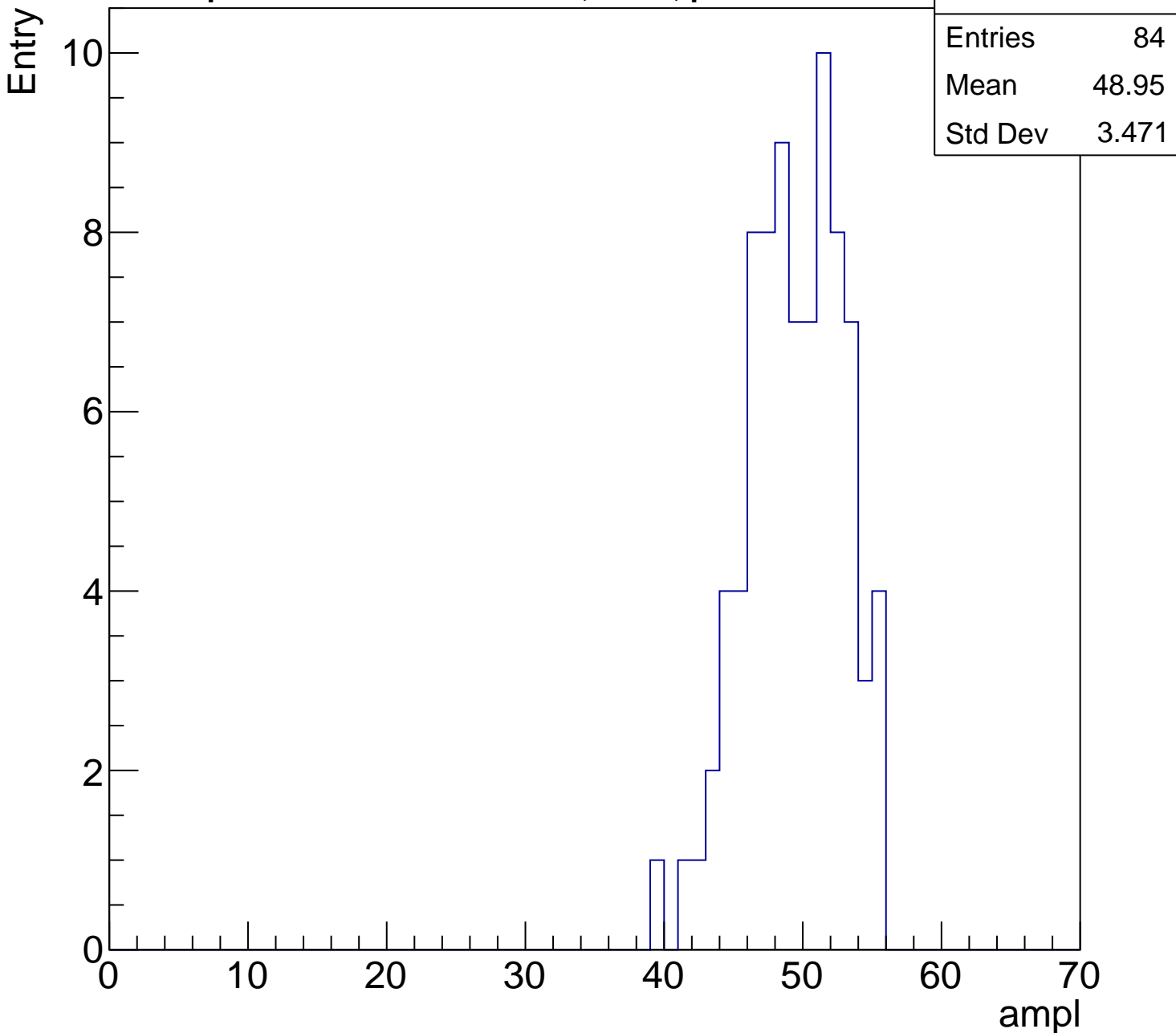
Entries	84
Mean	48.95
Std Dev	3.471

Entry

10  
8  
6  
4  
2  
0

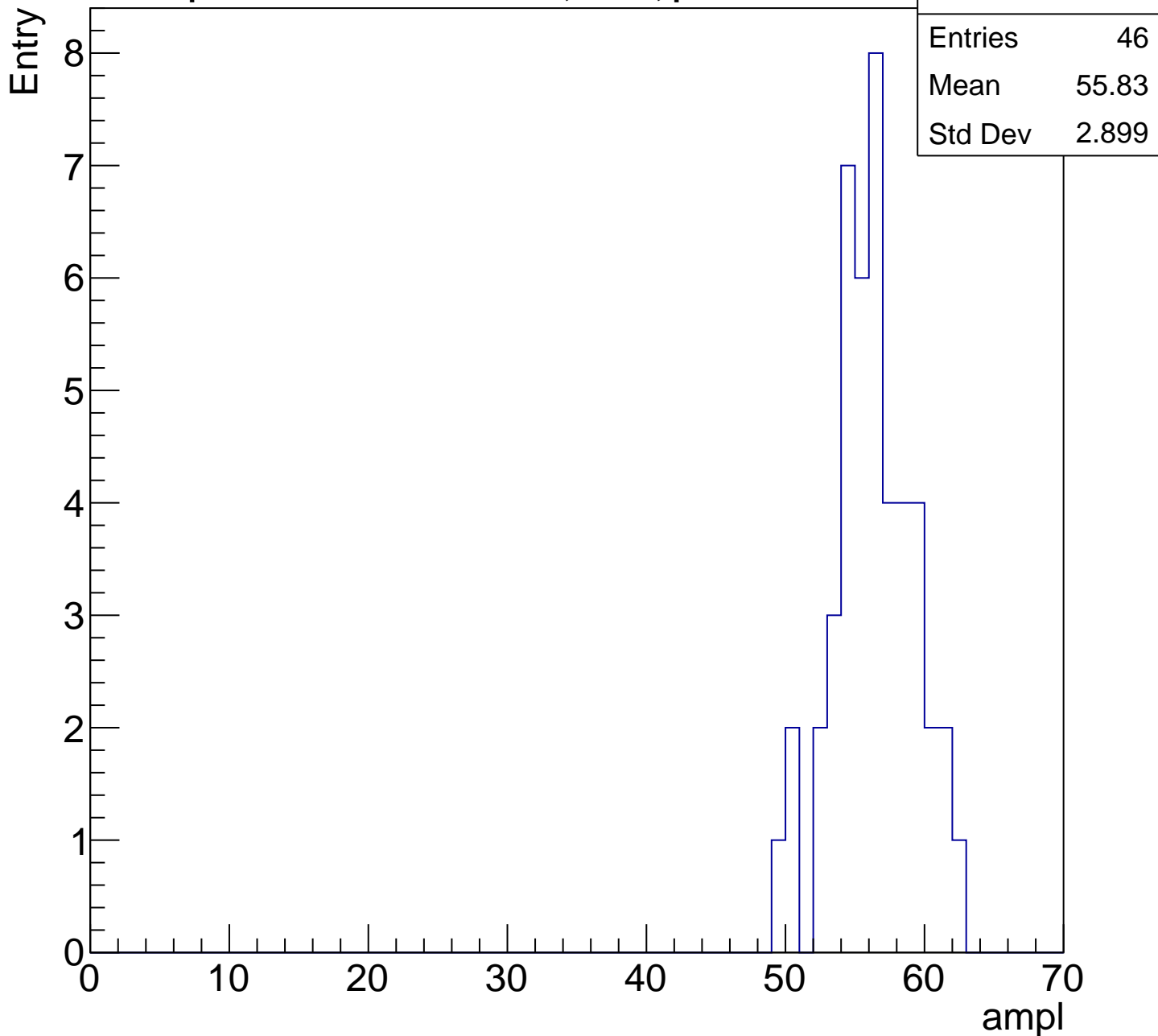
0 10 20 30 40 50 60 70

ampl



# B0L001S, U6-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

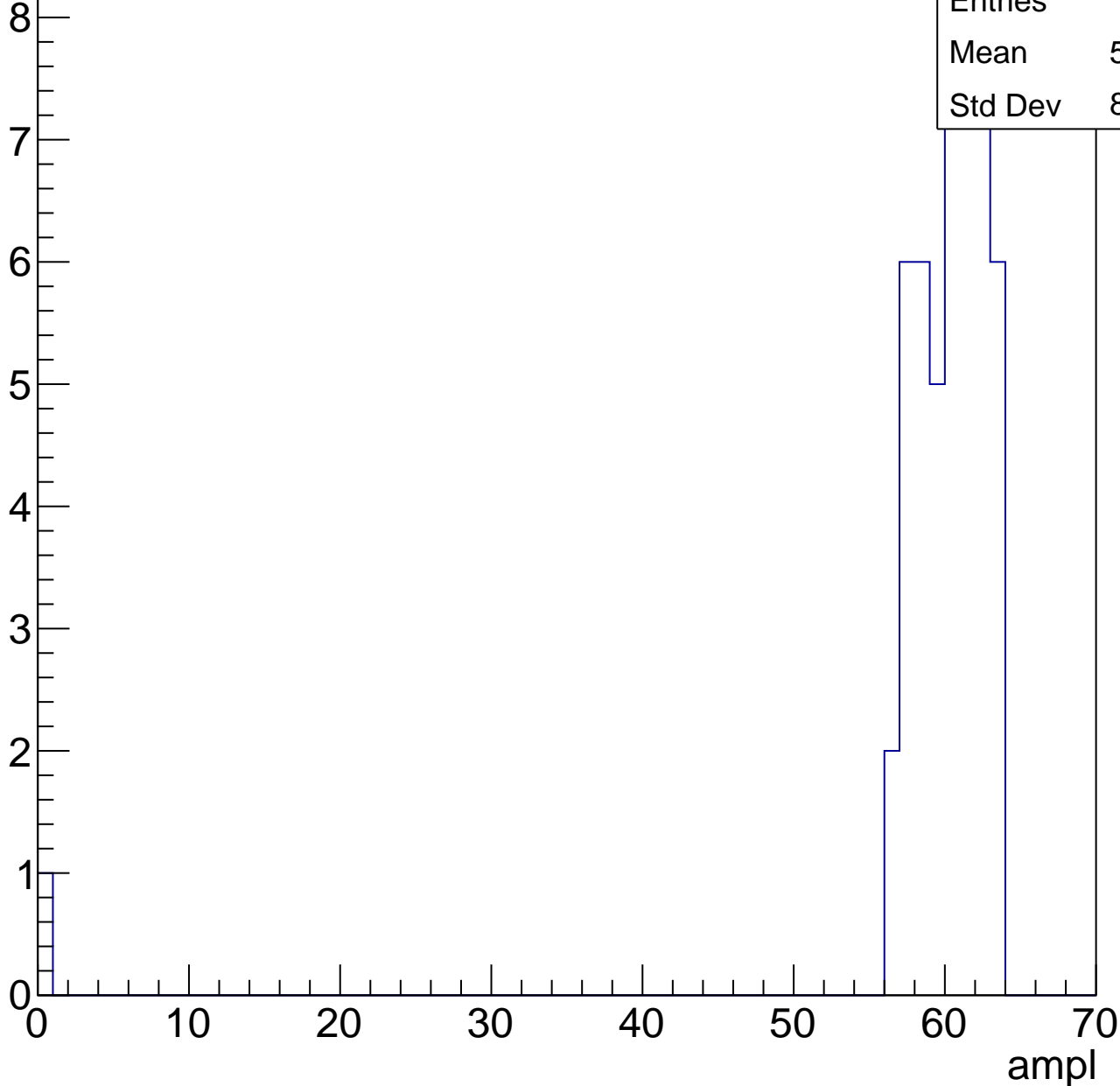


# B0L001S, U6-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

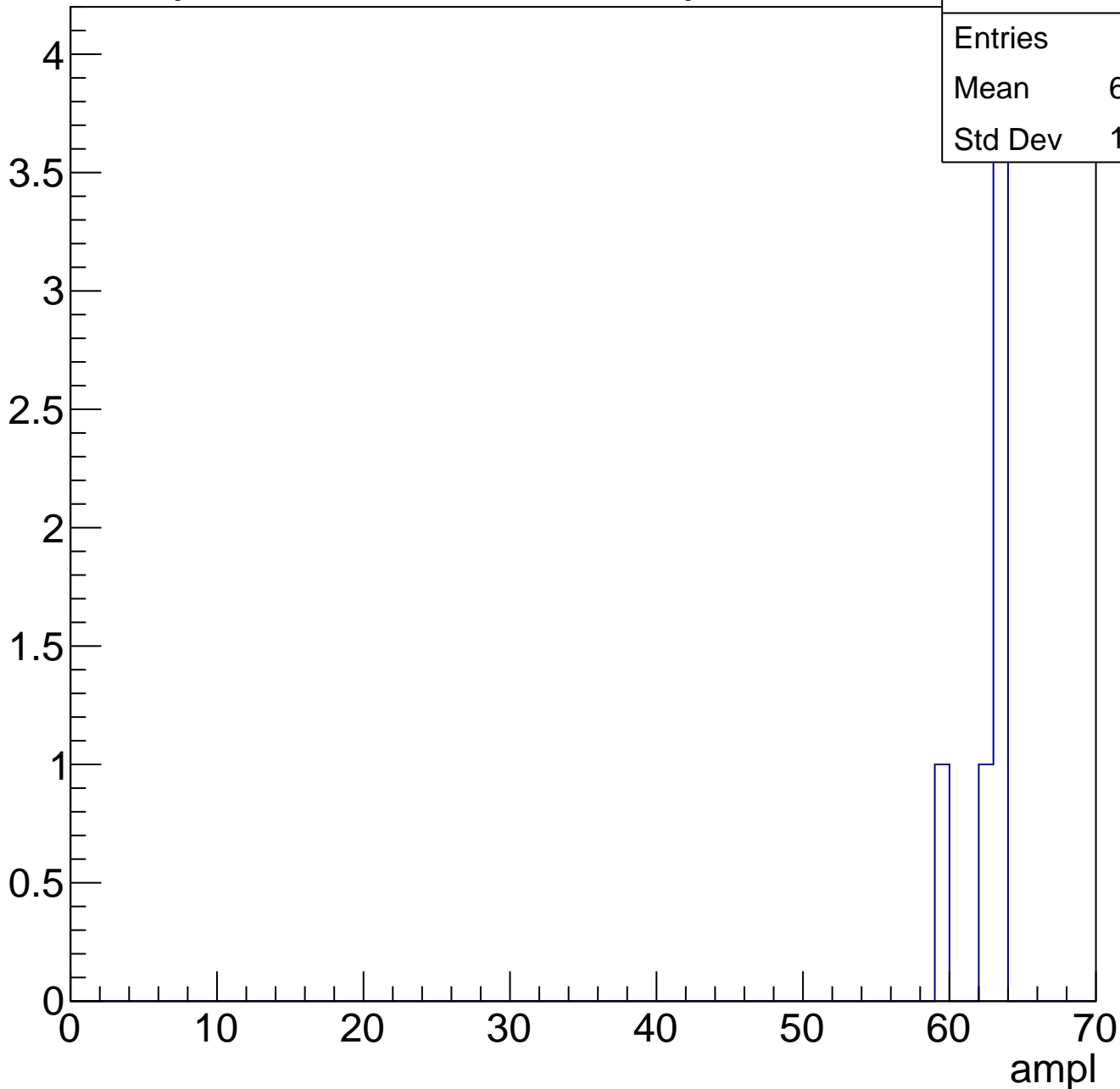
Entries	50
Mean	58.78
Std Dev	8.642



# B0L001S, U6-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U6-ch13, adc0

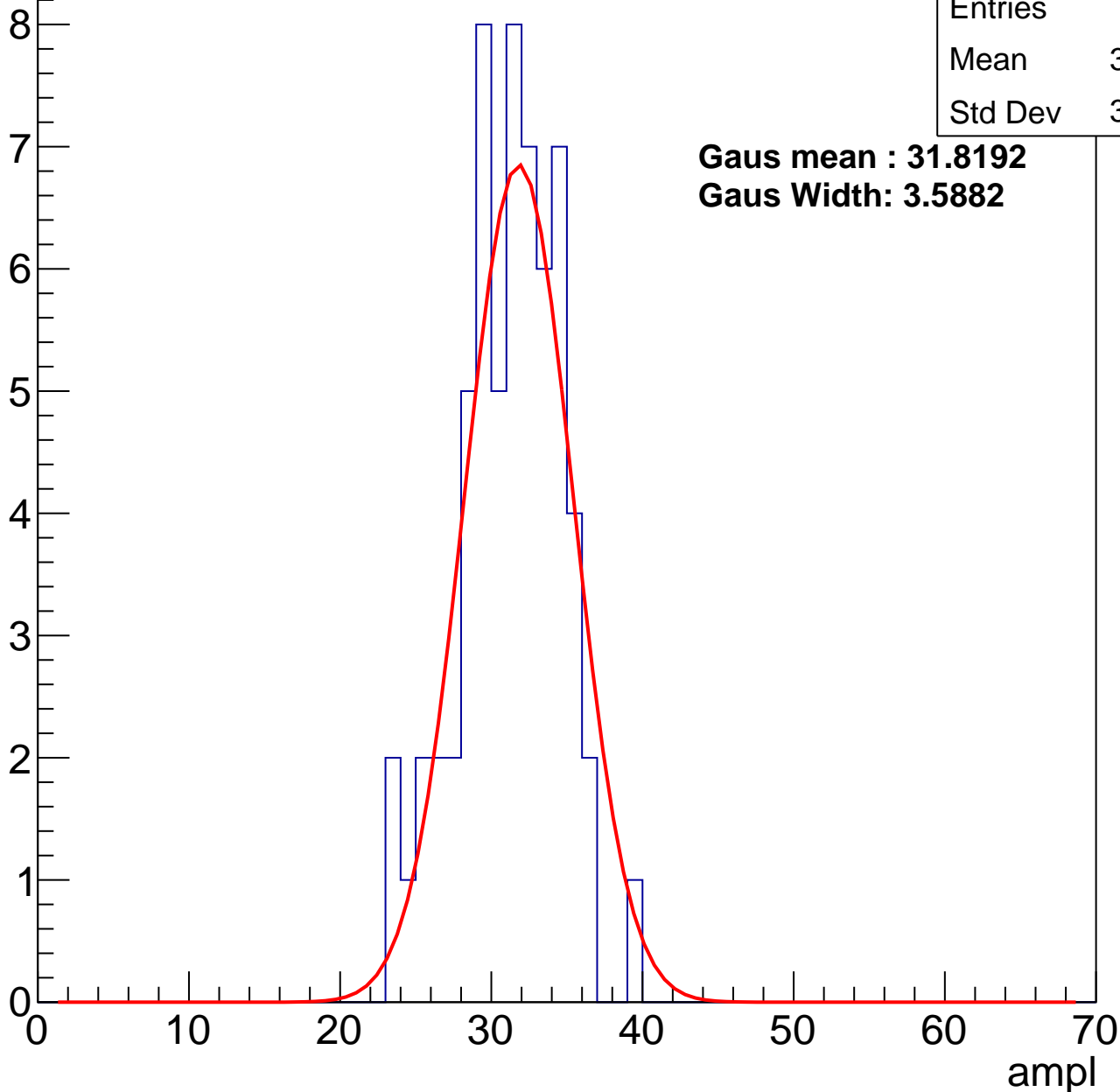
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	30.76
Std Dev	3.315

**Gaus mean : 31.8192**

**Gaus Width: 3.5882**



# B0L001S, U6-ch13, adc1

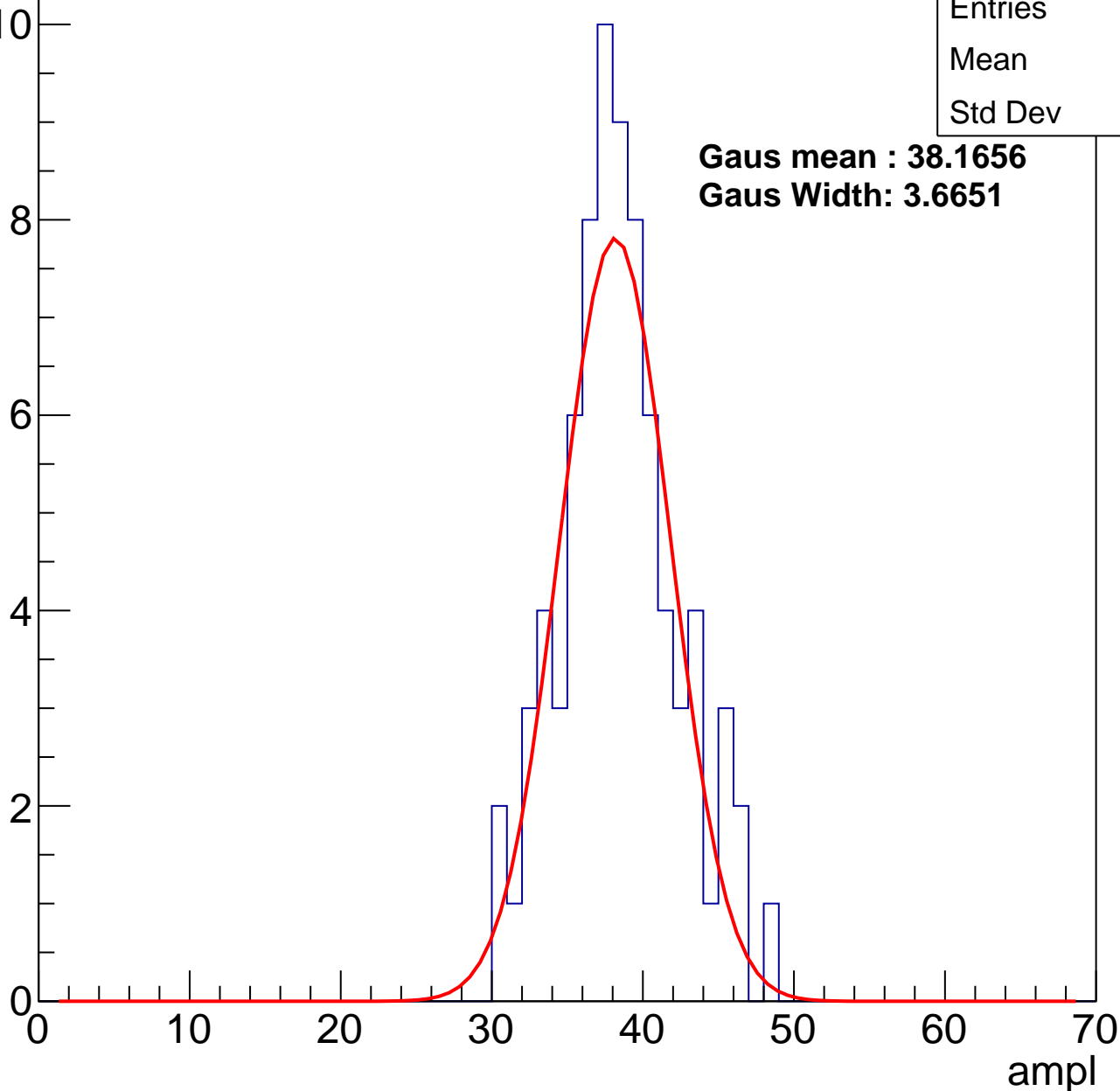
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	38
Std Dev	3.85

**Gaus mean : 38.1656**

**Gaus Width: 3.6651**



# B0L001S, U6-ch13, adc2

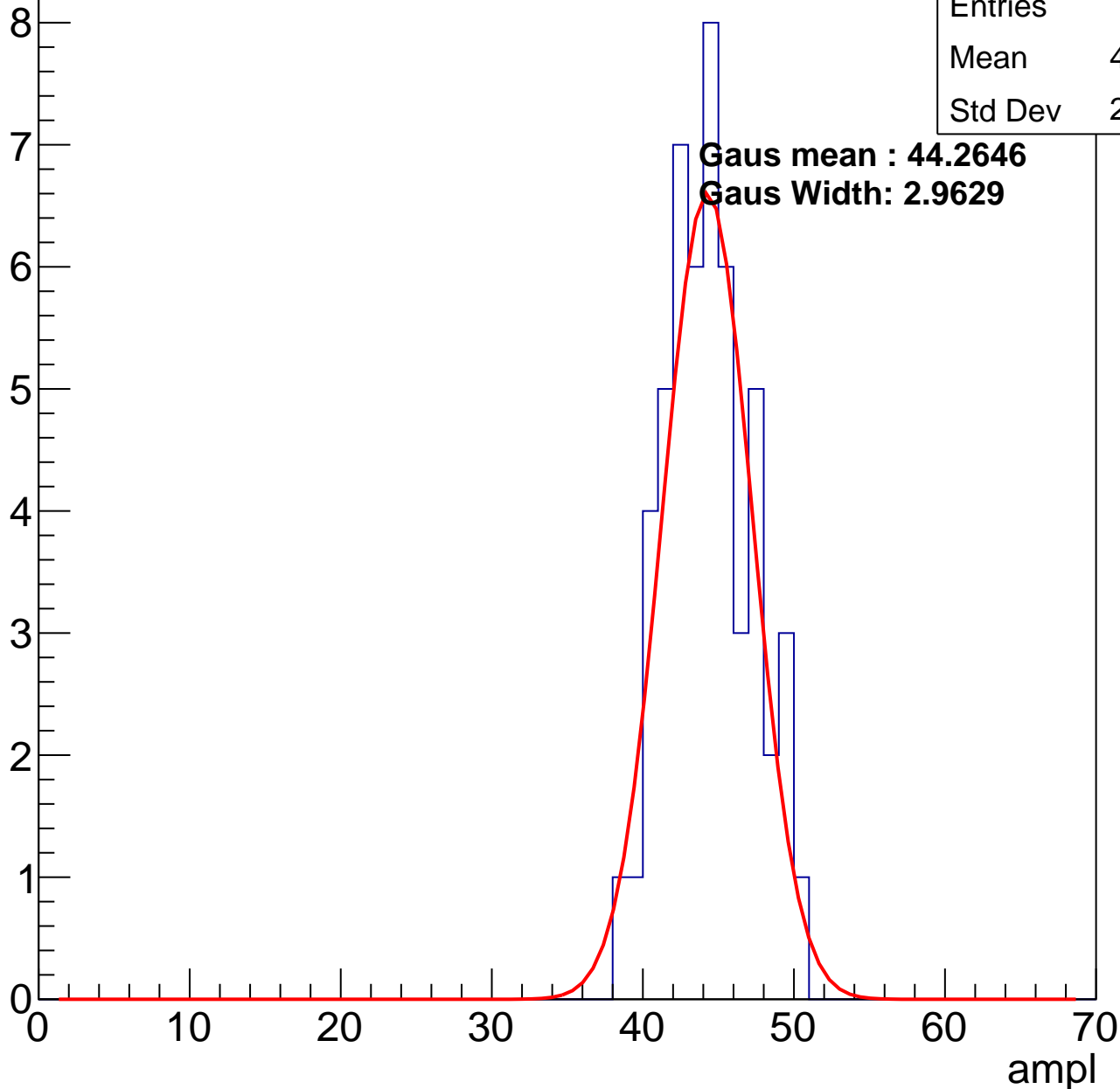
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	43.88
Std Dev	2.806

**Gaus mean : 44.2646**

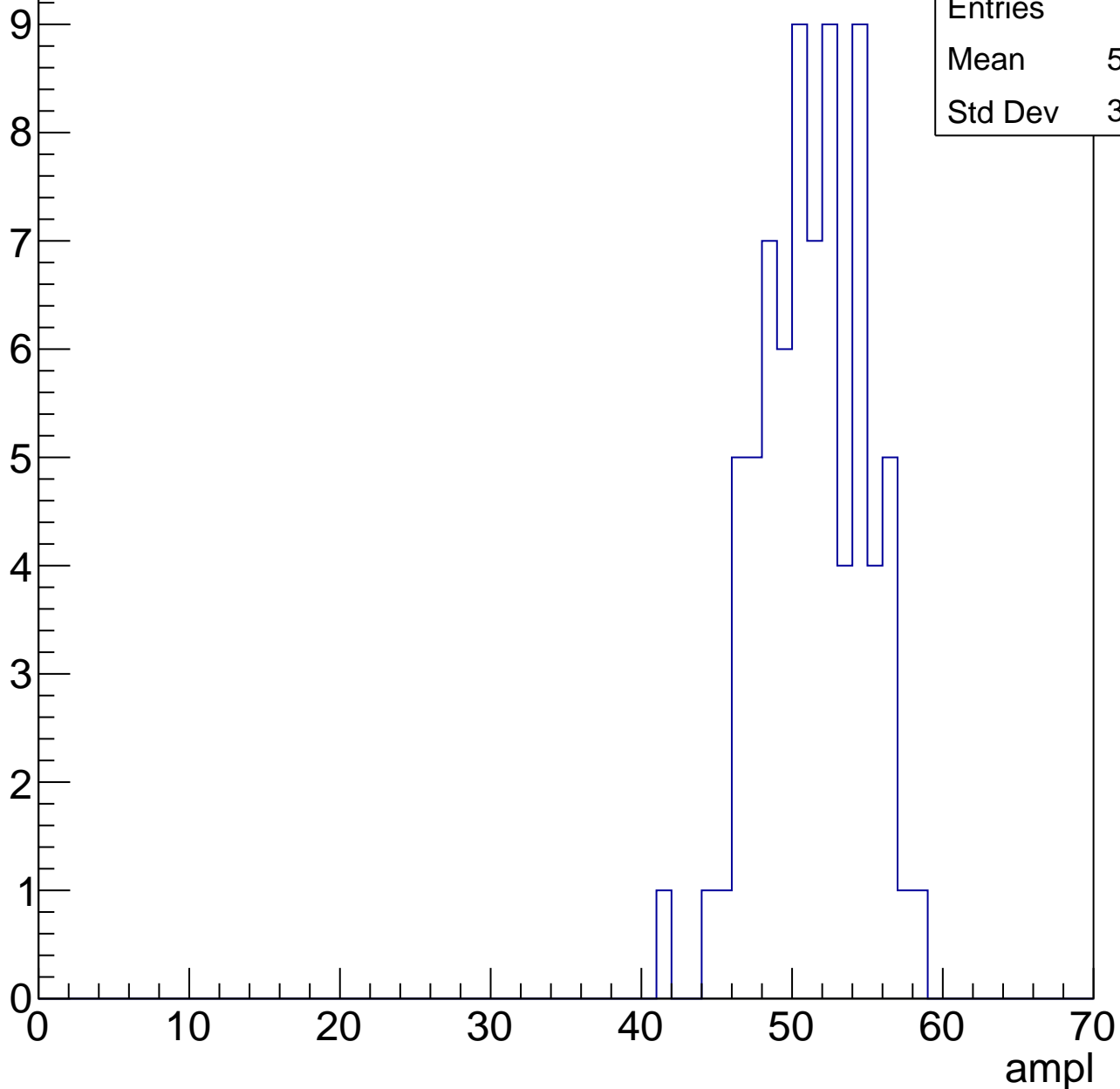
**Gaus Width: 2.9629**



# B0L001S, U6-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

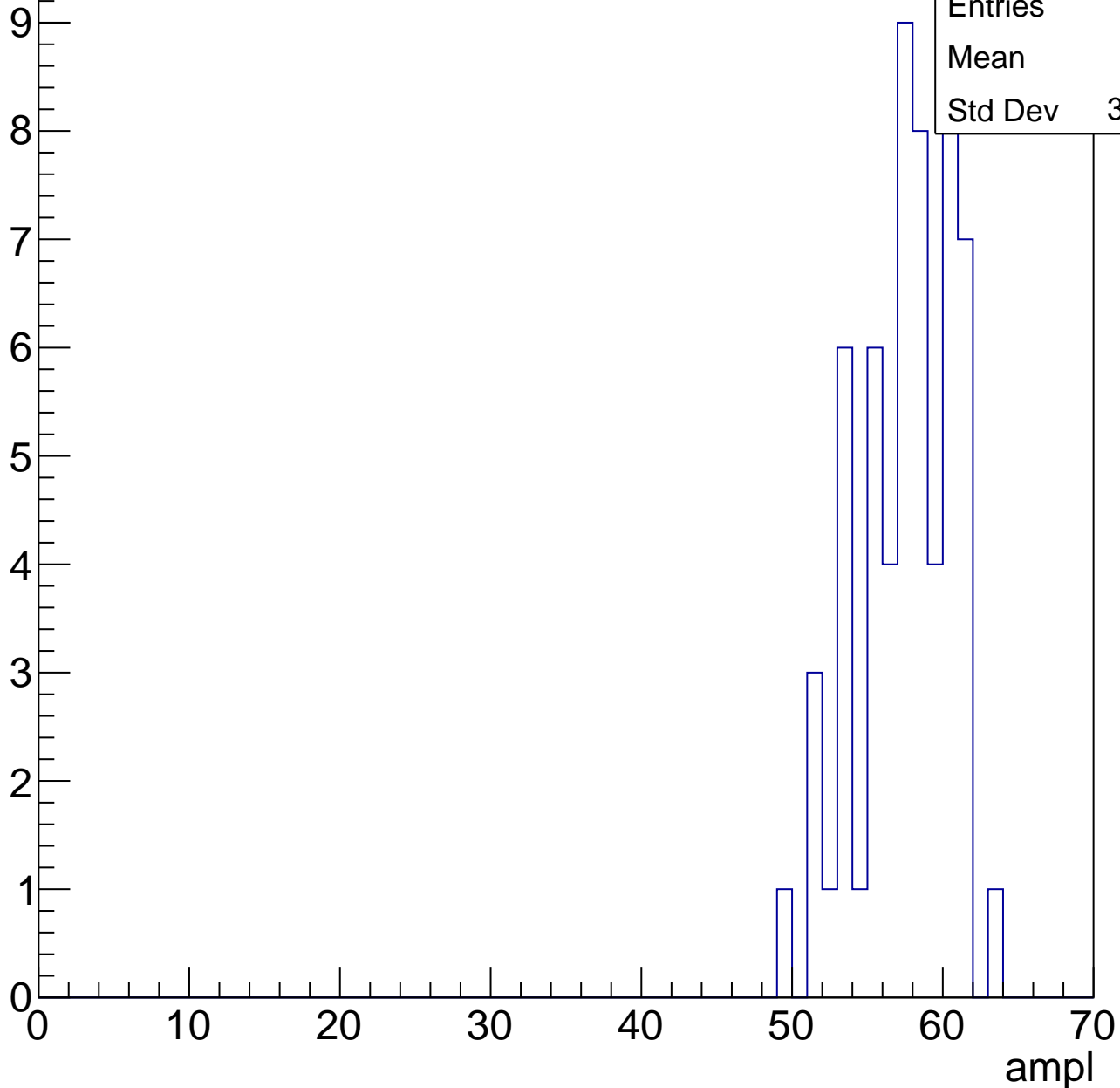


Entries	75
Mean	50.84
Std Dev	3.394

# B0L001S, U6-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

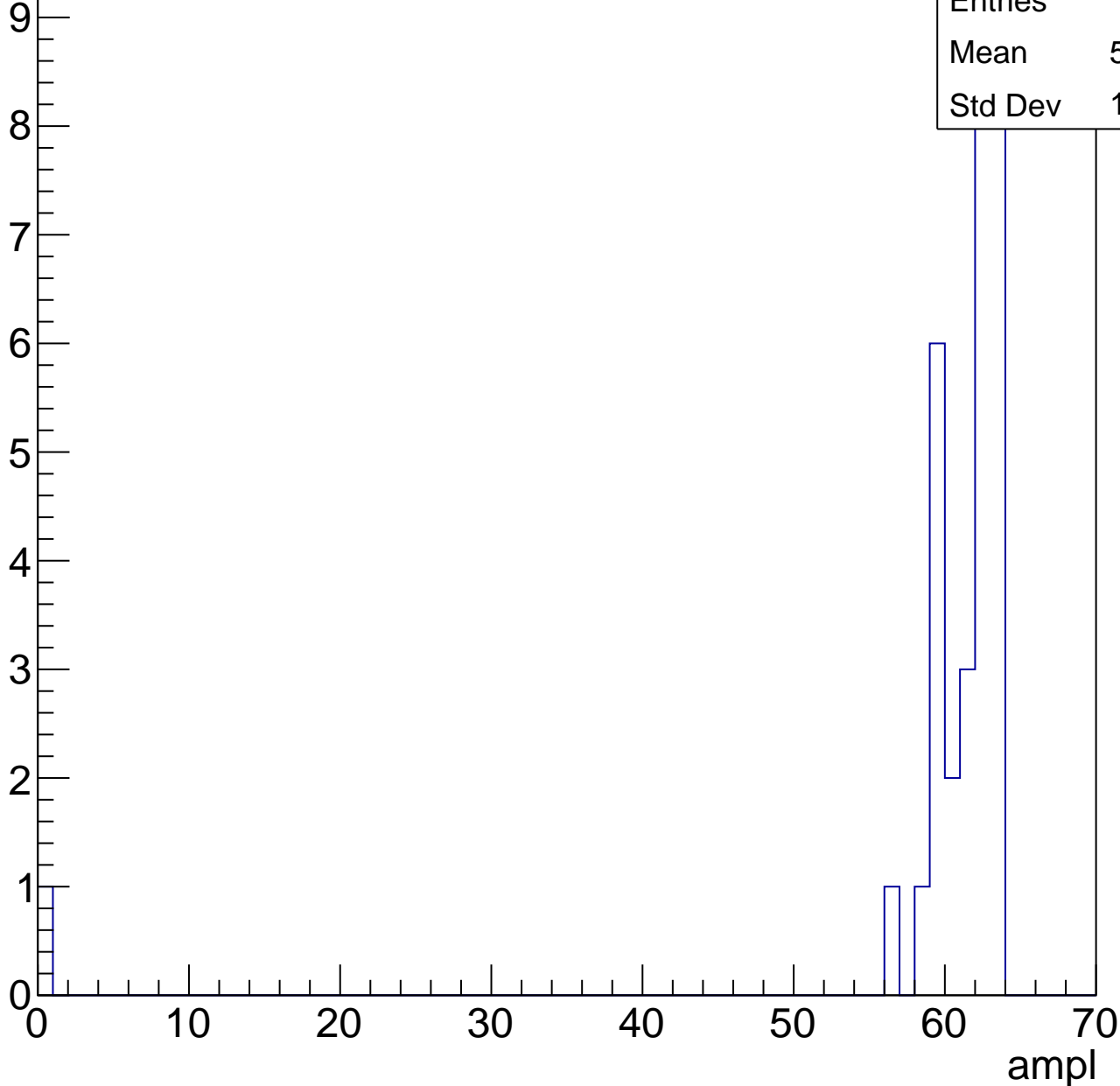


# B0L001S, U6-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	31
Mean	59.16
Std Dev	10.95



# B0L001S, U6-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	62
Std Dev	0

ampl



# B0L001S, U6-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U6-ch14, adc0

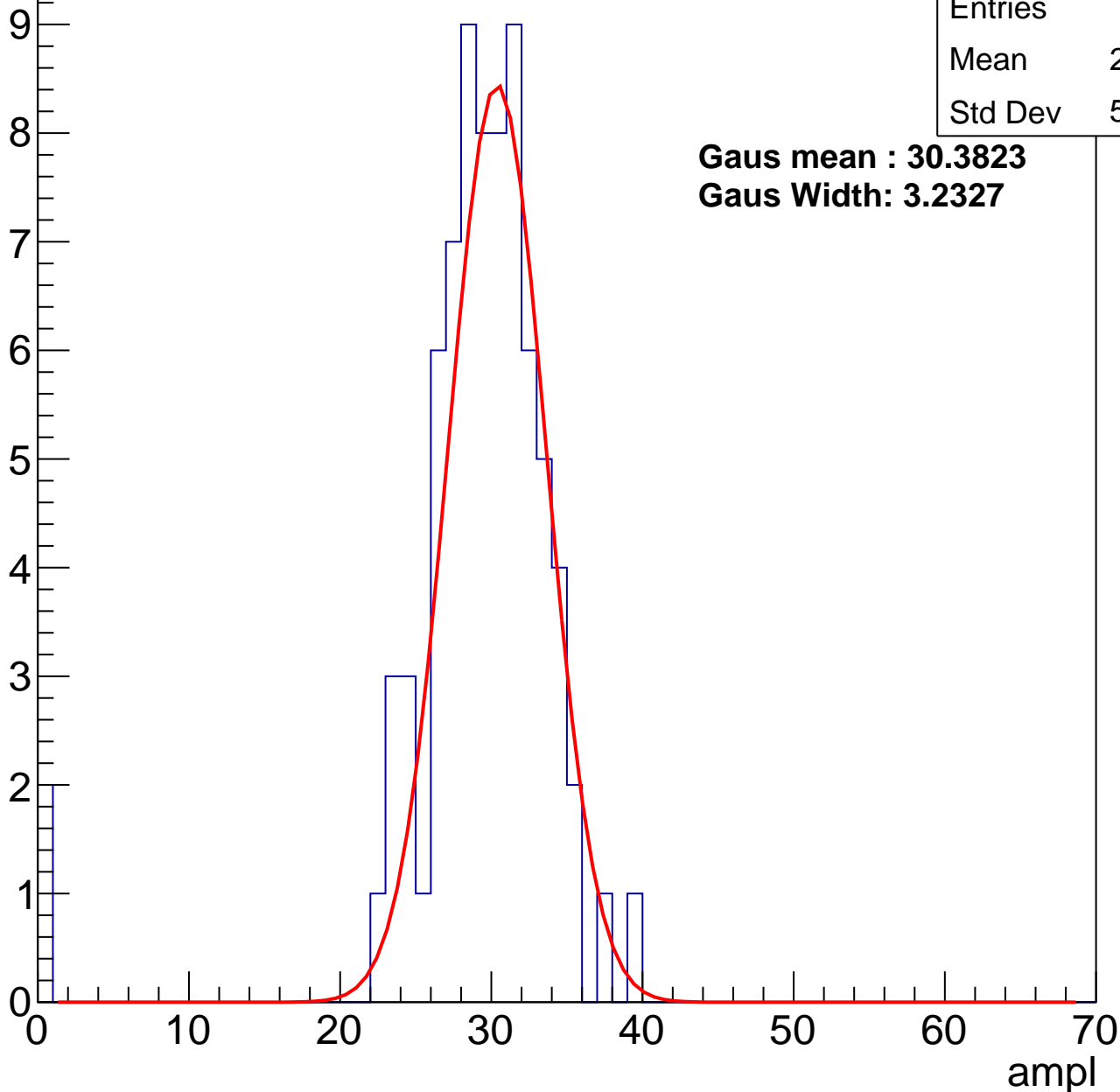
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	28.62
Std Dev	5.763

**Gaus mean : 30.3823**

**Gaus Width: 3.2327**



# B0L001S, U6-ch14, adc1

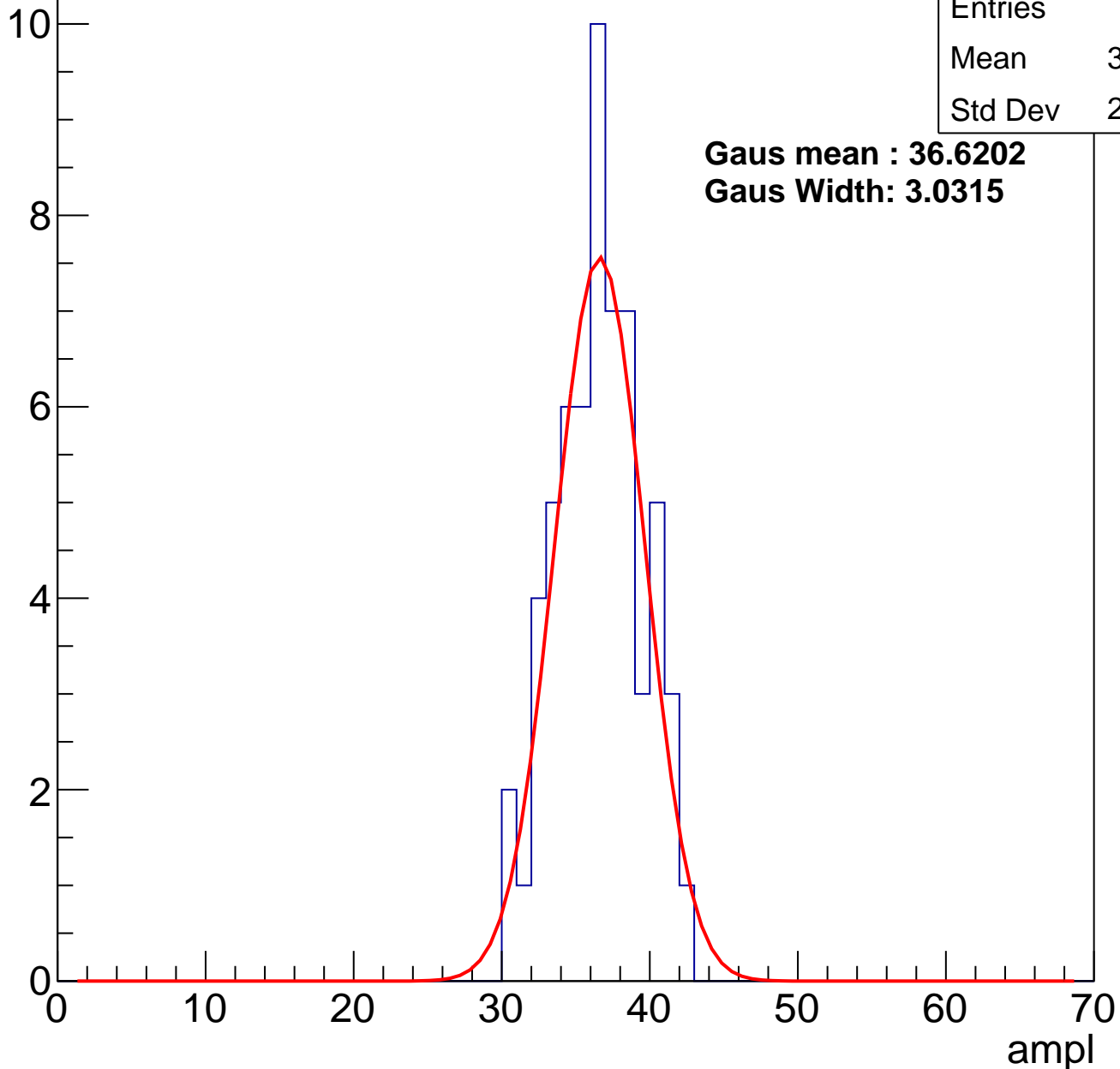
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	60
Mean	36.08
Std Dev	2.854

**Gaus mean : 36.6202**

**Gaus Width: 3.0315**

Entry



# B0L001S, U6-ch14, adc2

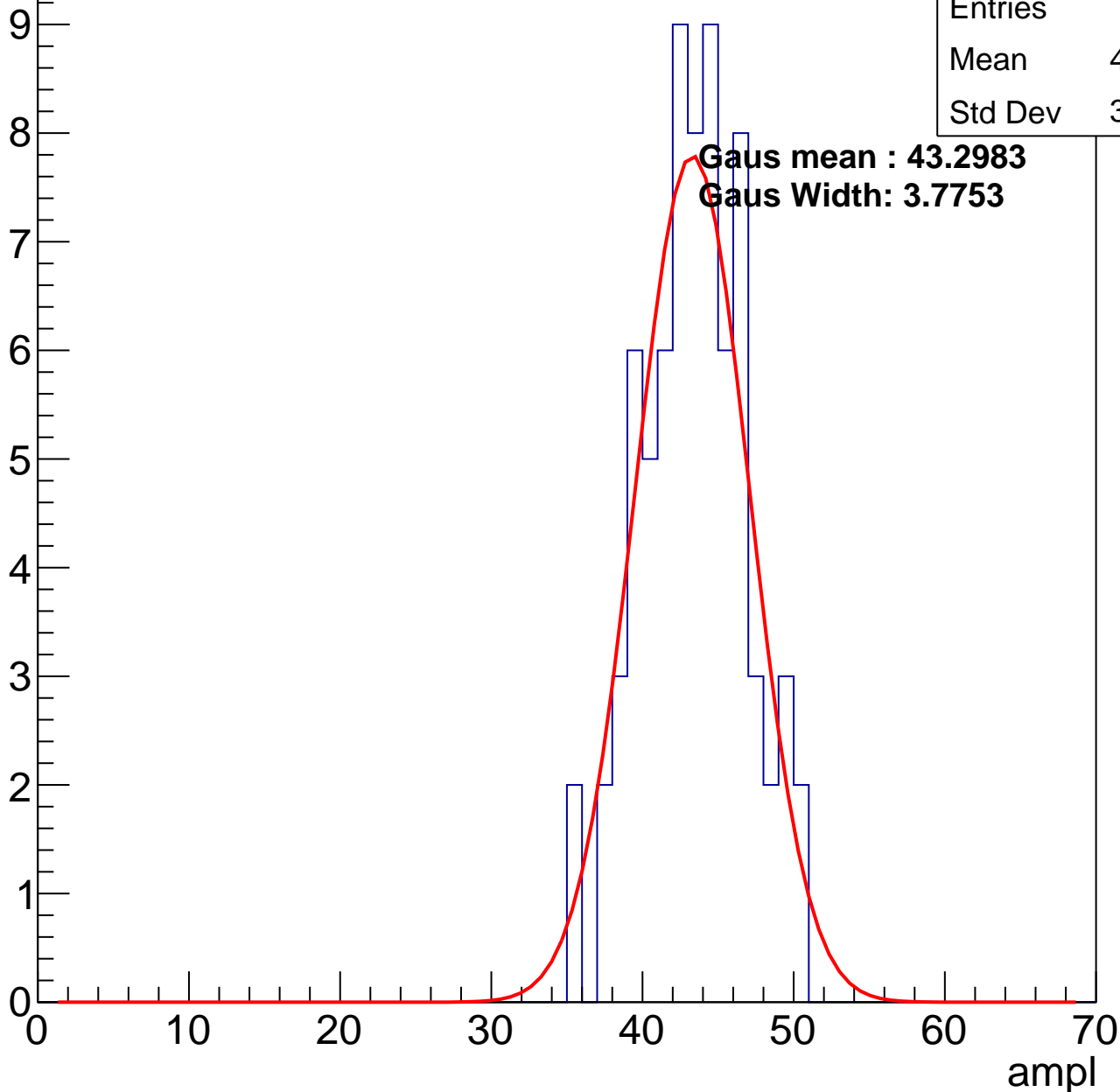
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	42.95
Std Dev	3.405

**Gaus mean : 43.2983**

**Gaus Width: 3.7753**



# B0L001S, U6-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	64
Mean	49.61
Std Dev	3.296

Entry

10

8

6

4

2

0

0

10

20

30

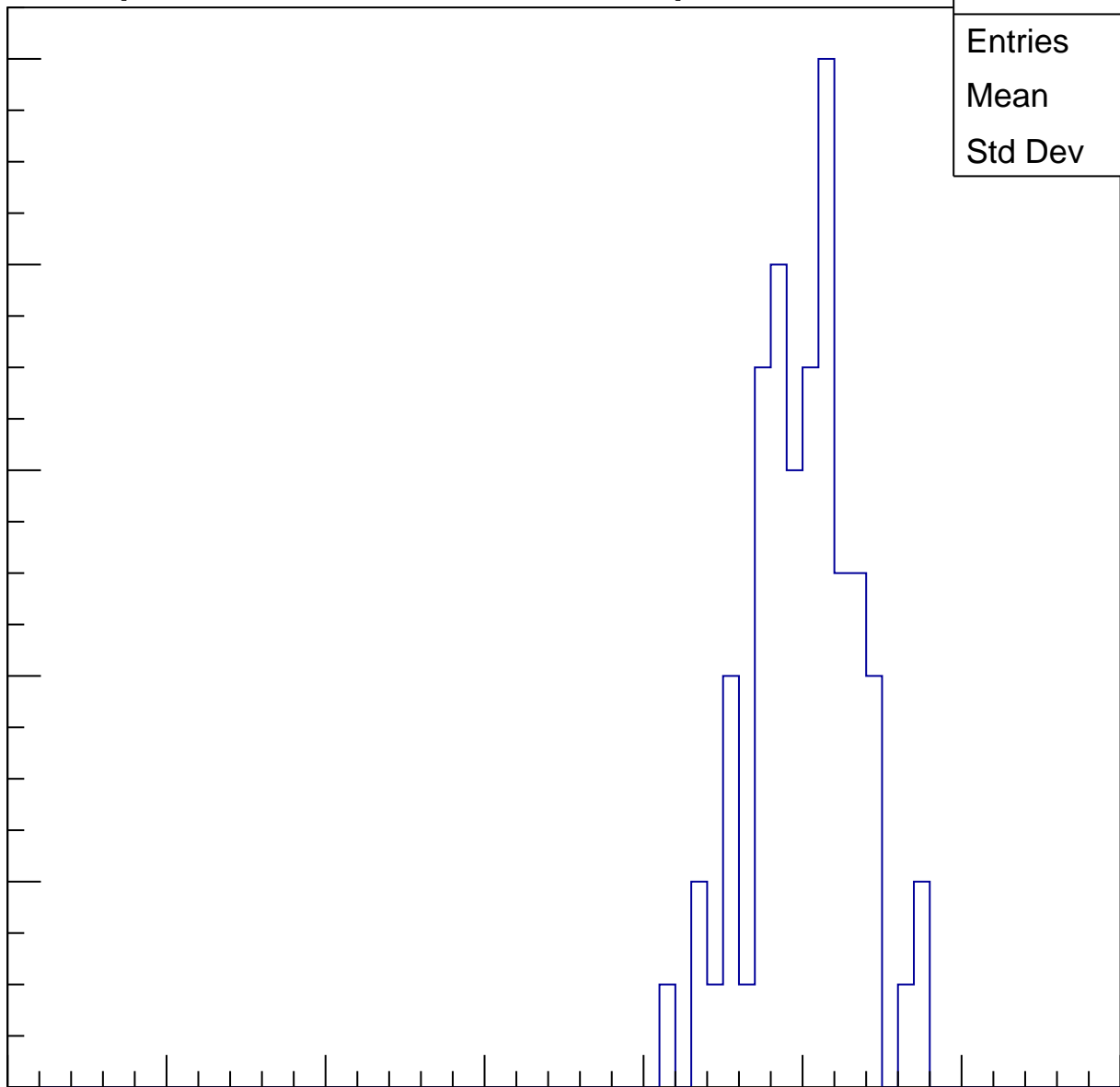
40

50

60

70

ampl

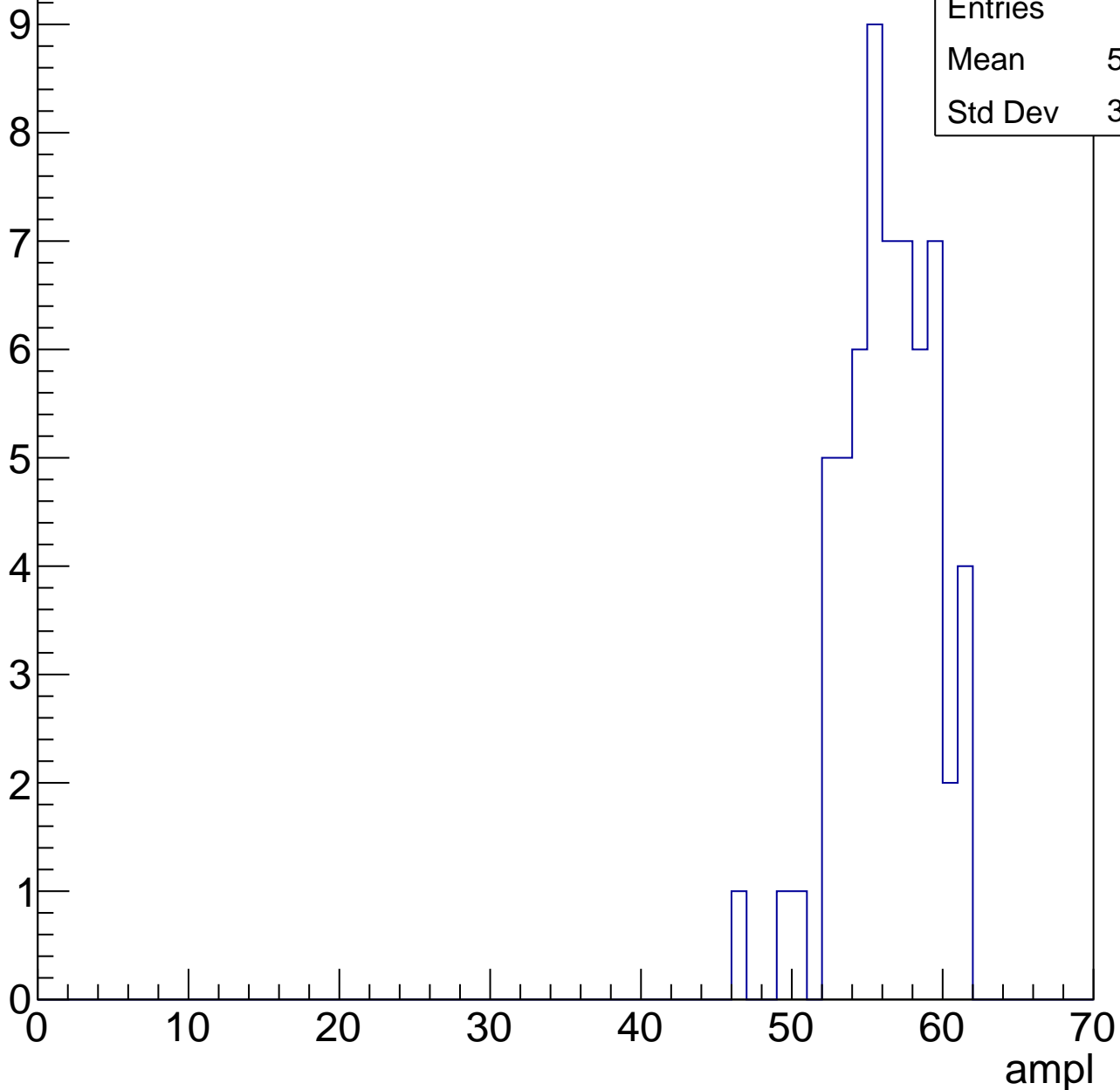


# B0L001S, U6-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	55.82
Std Dev	3.049



# B0L001S, U6-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

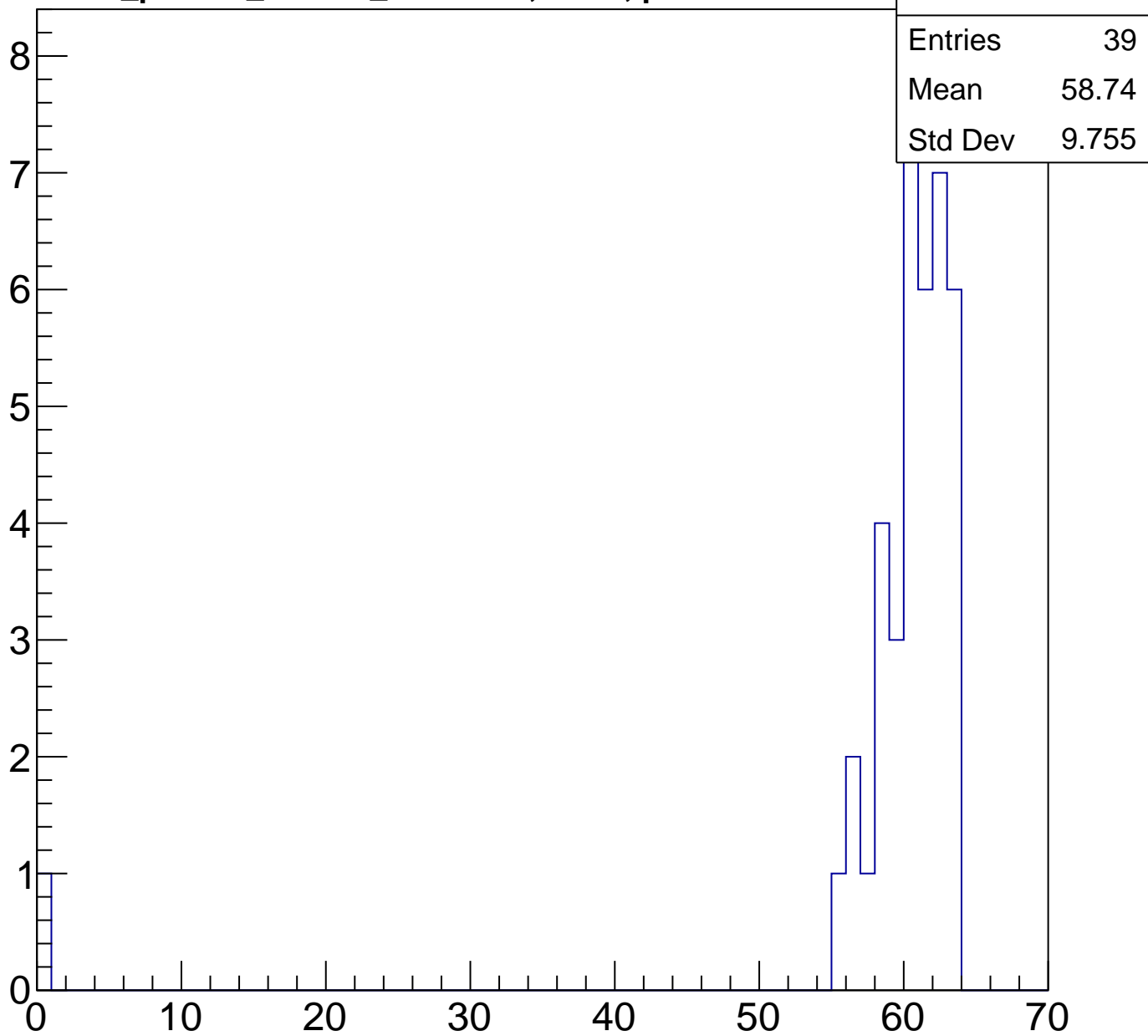
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	39
Mean	58.74
Std Dev	9.755

ampl

0 10 20 30 40 50 60 70



# B0L001S, U6-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	7
Mean	62.57
Std Dev	0.4949



# B0L001S, U6-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U6-ch15, adc0

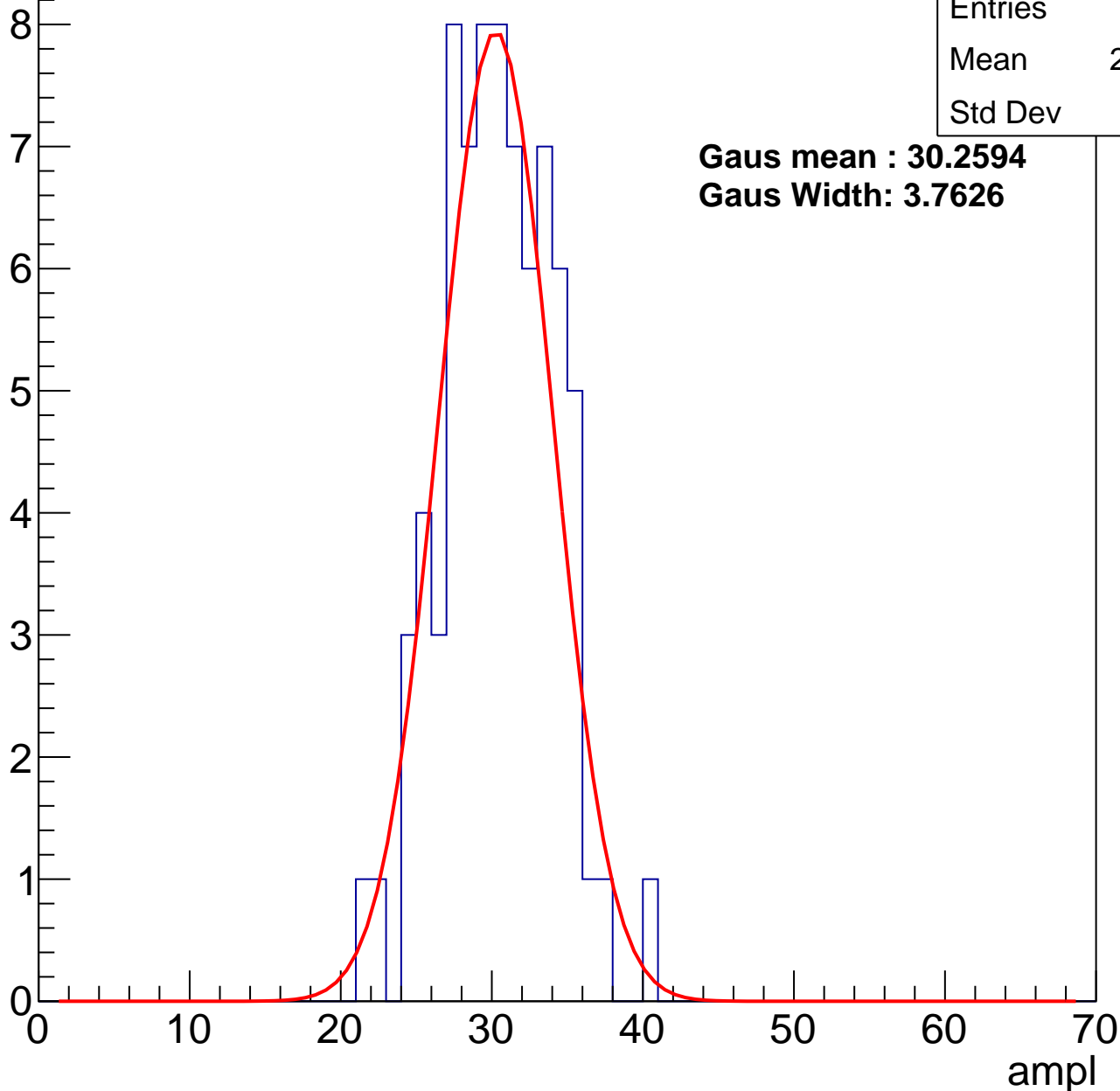
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	29.99
Std Dev	3.62

**Gaus mean : 30.2594**

**Gaus Width: 3.7626**



# B0L001S, U6-ch15, adc1

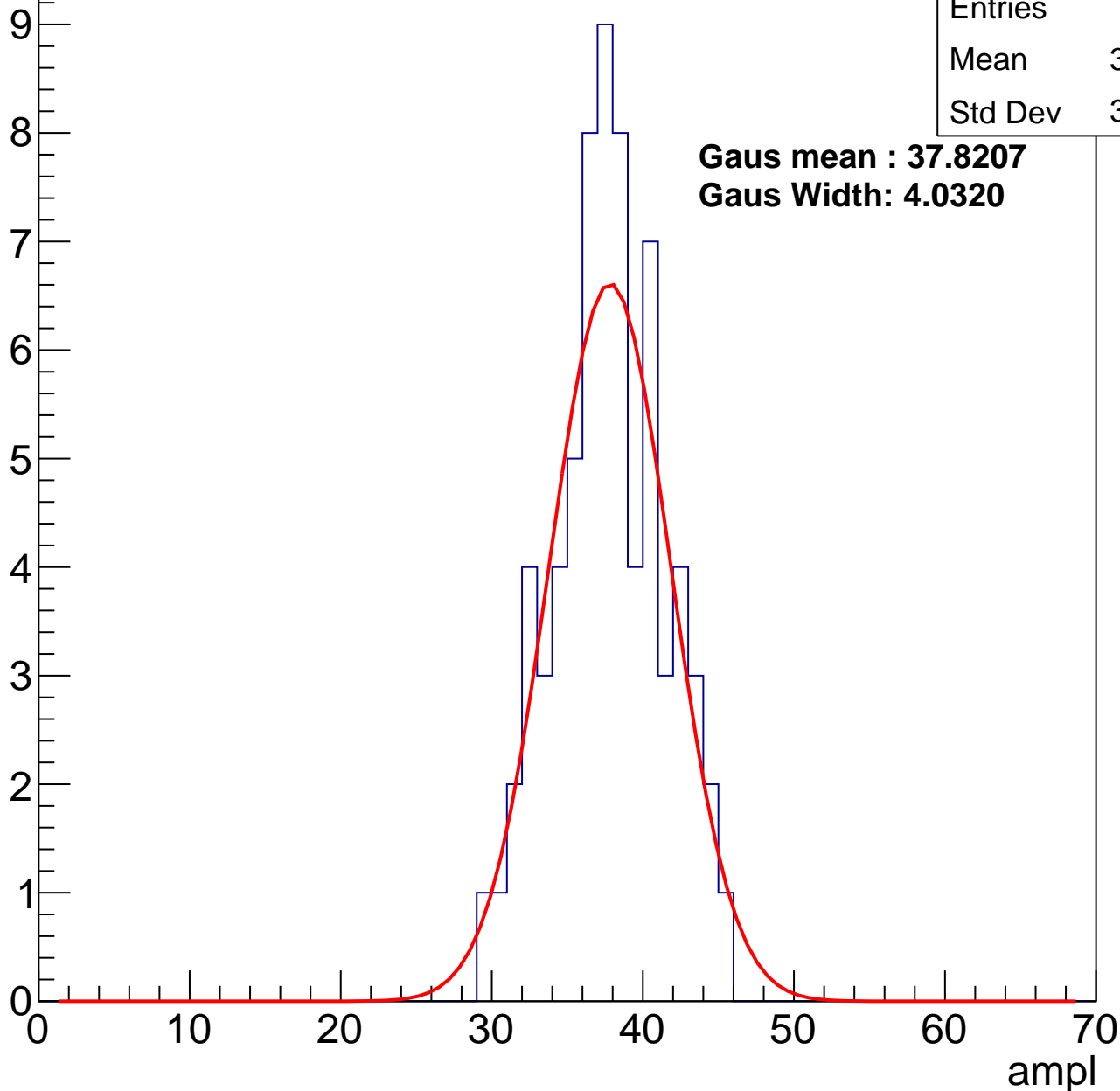
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	37.29
Std Dev	3.604

**Gaus mean : 37.8207**

**Gaus Width: 4.0320**



# B0L001S, U6-ch15, adc2

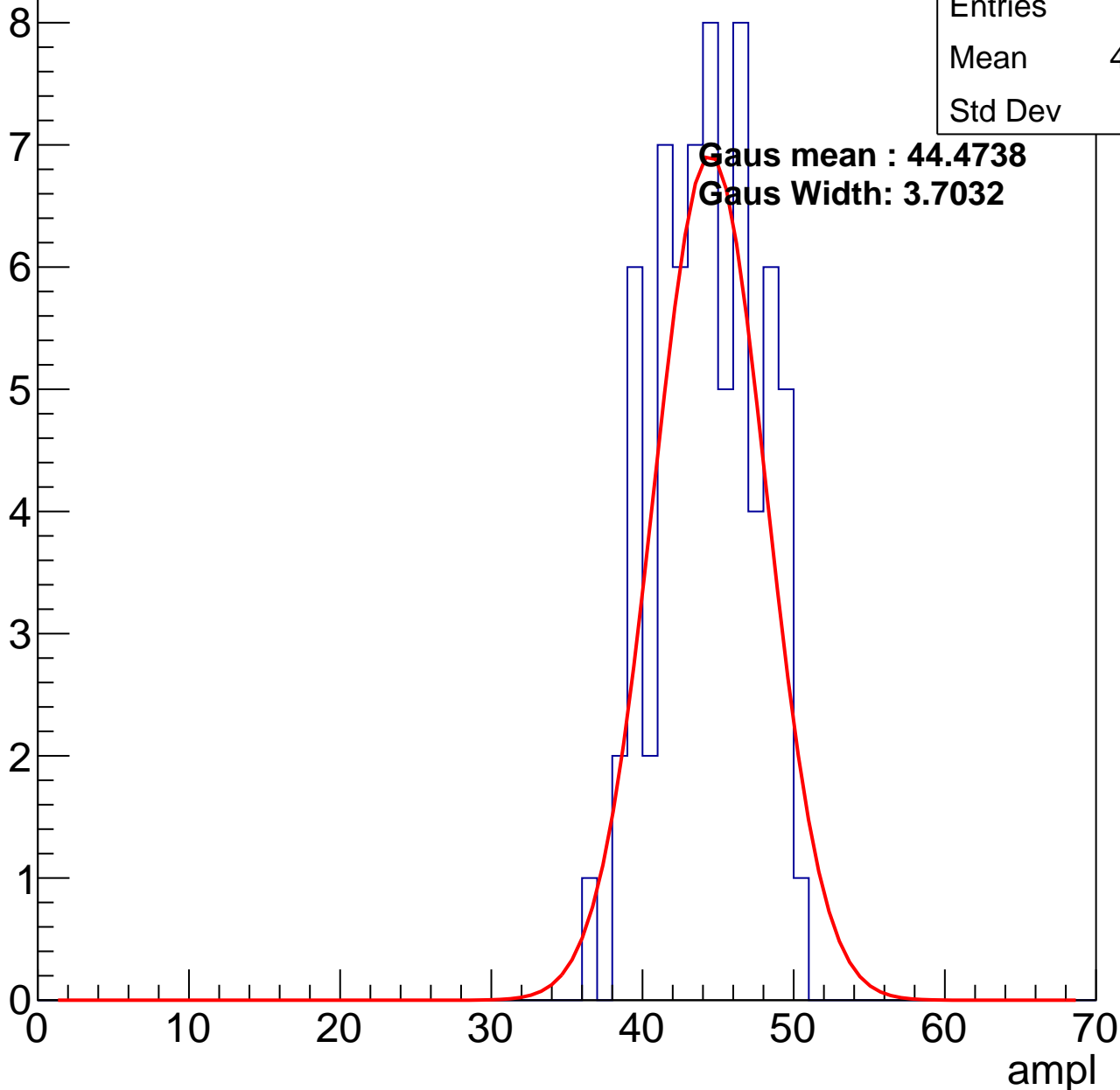
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	43.85
Std Dev	3.3

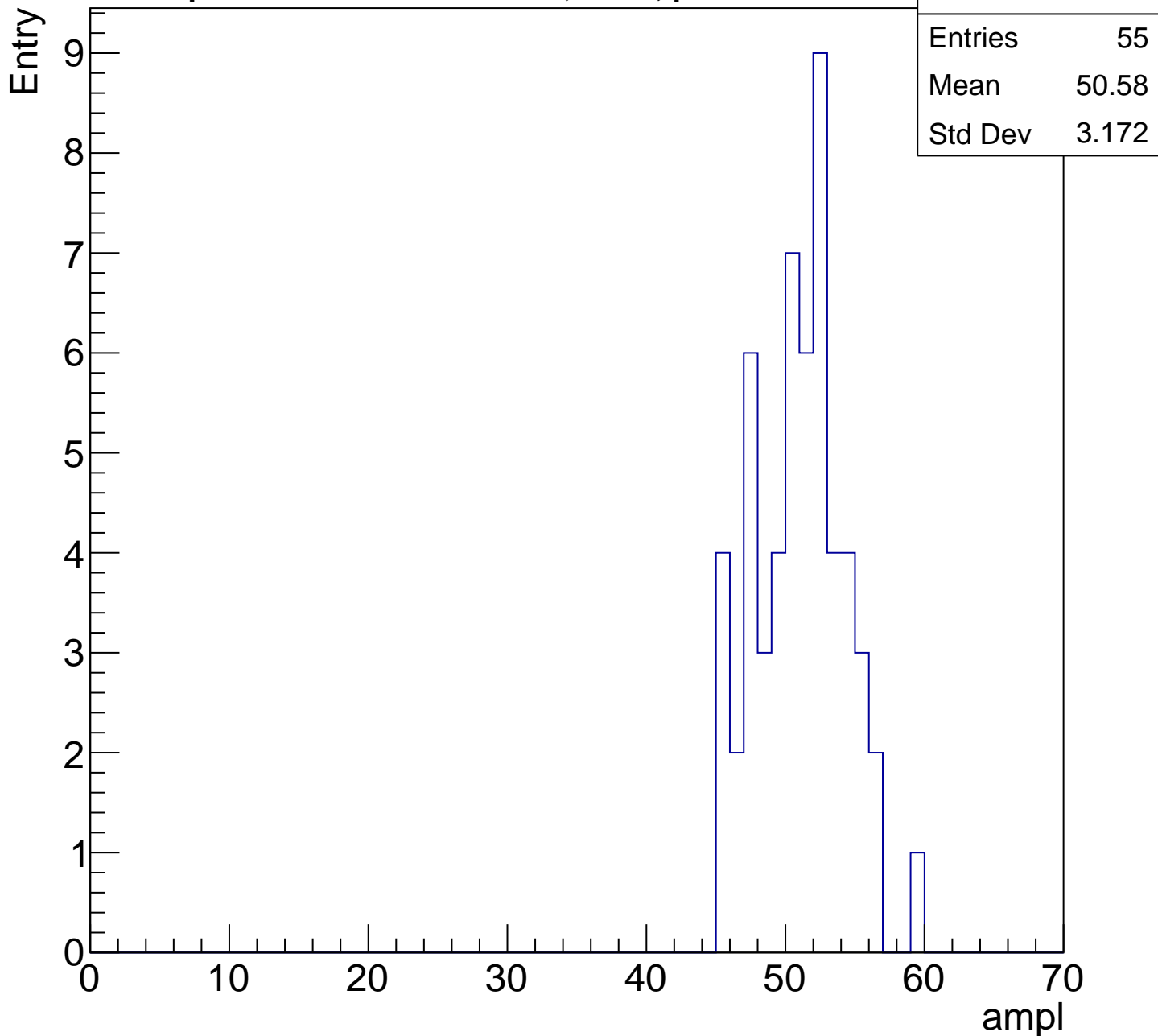
**Gaus mean : 44.4738**

**Gaus Width: 3.7032**



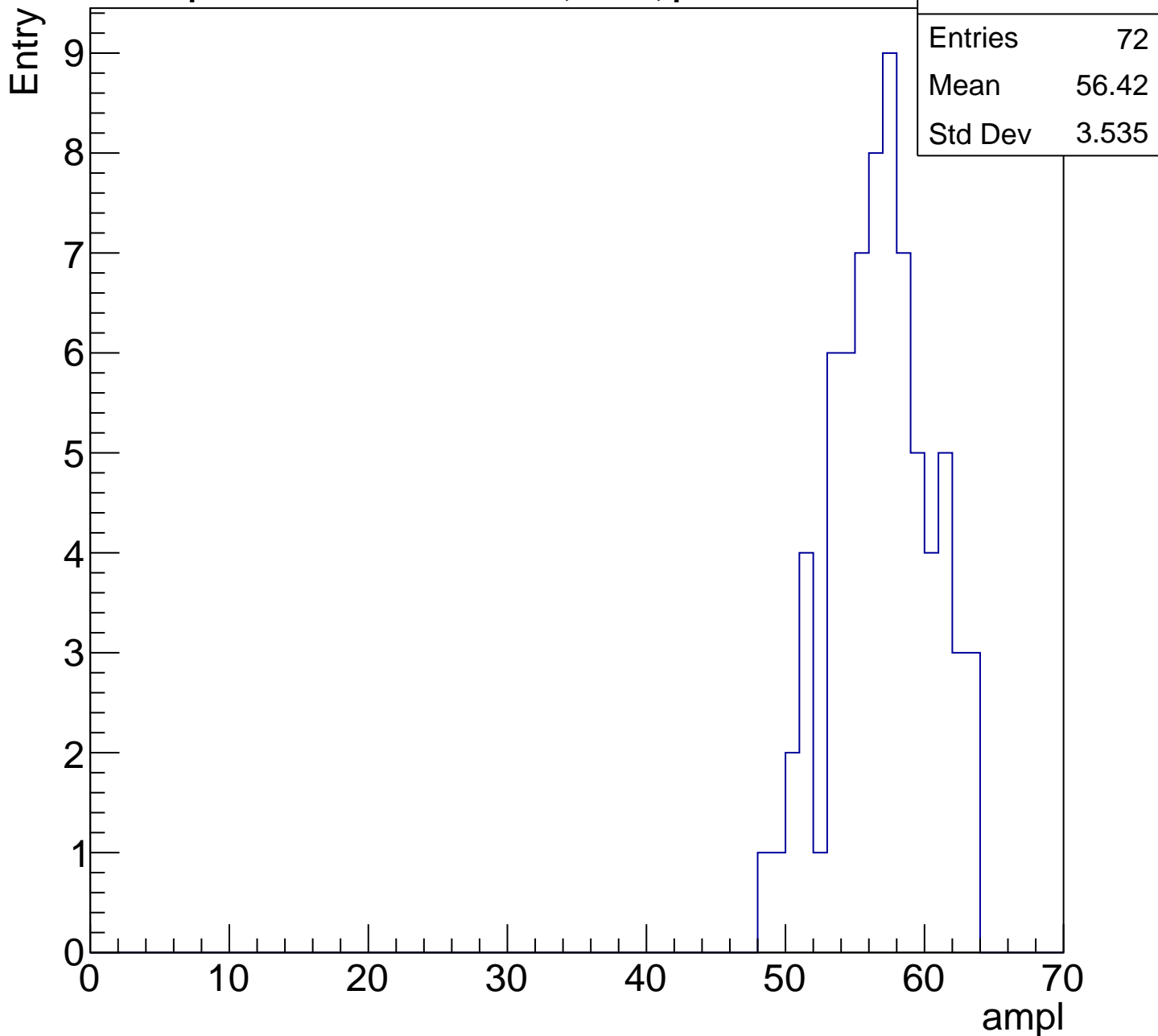
# B0L001S, U6-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U6-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

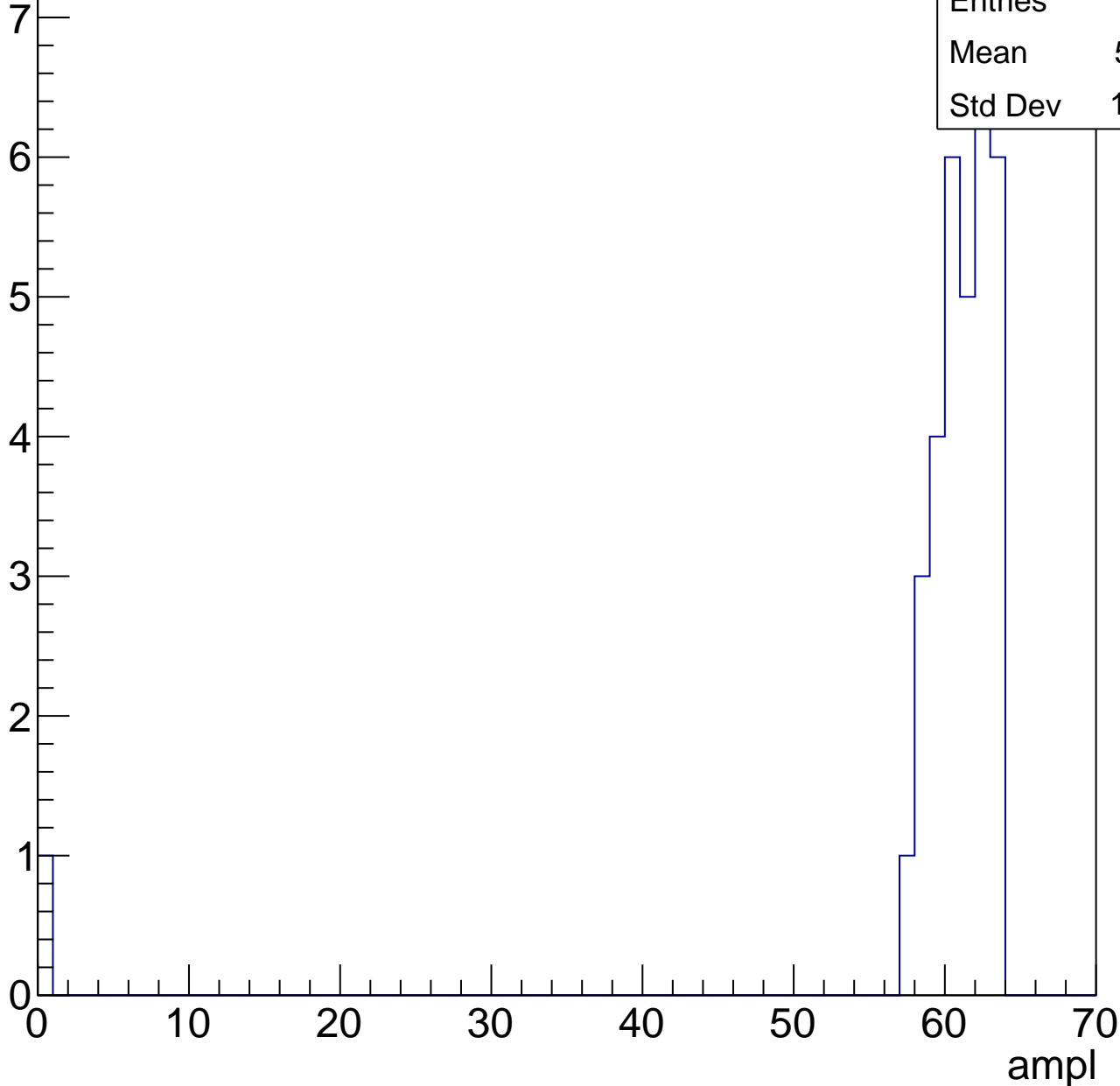


# B0L001S, U6-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	33
Mean	58.91
Std Dev	10.55



# B0L001S, U6-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U6-ch16, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	79
Mean	30.28
Std Dev	3.352

**Gaus mean : 30.9408**

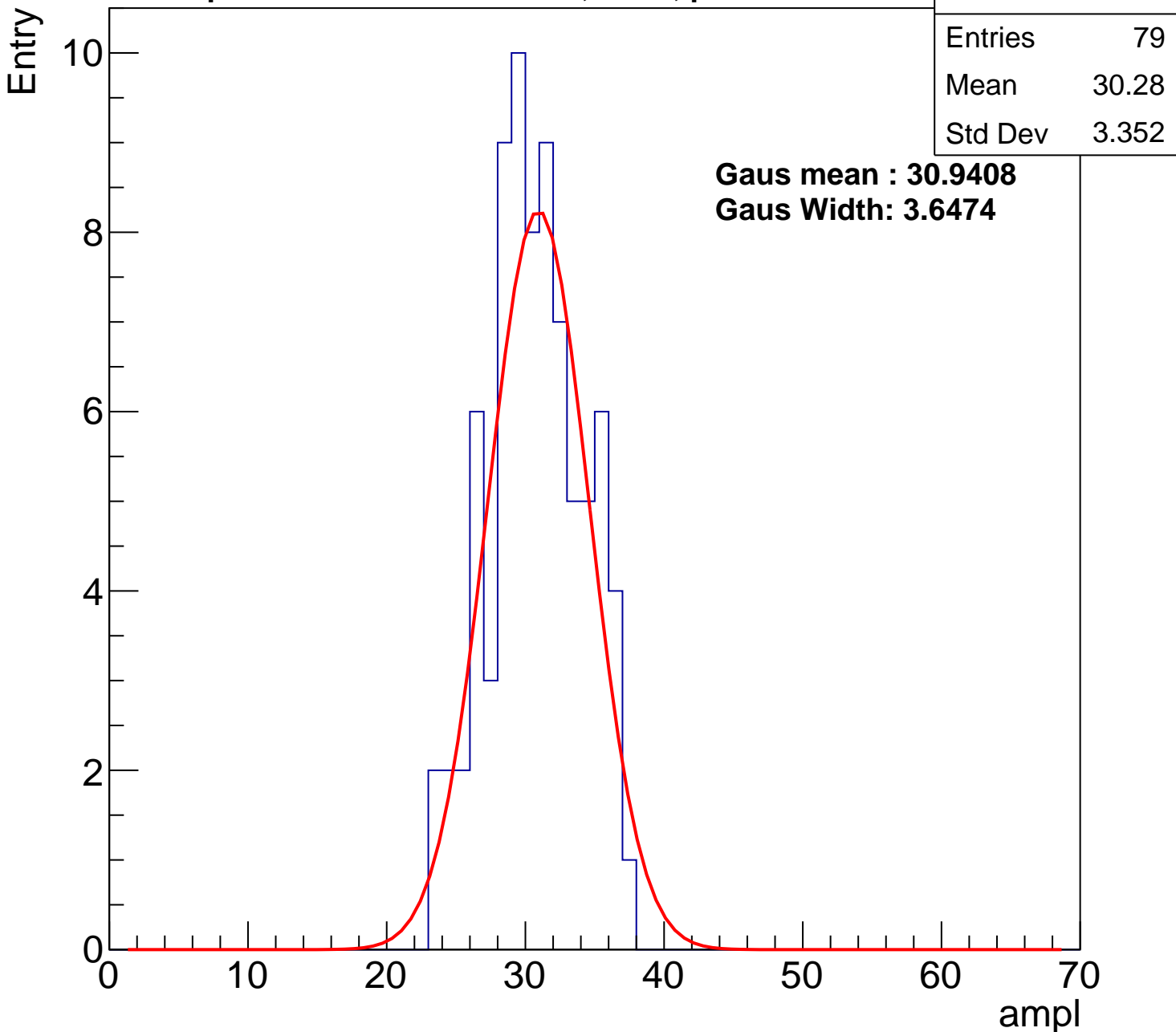
**Gaus Width: 3.6474**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U6-ch16, adc1

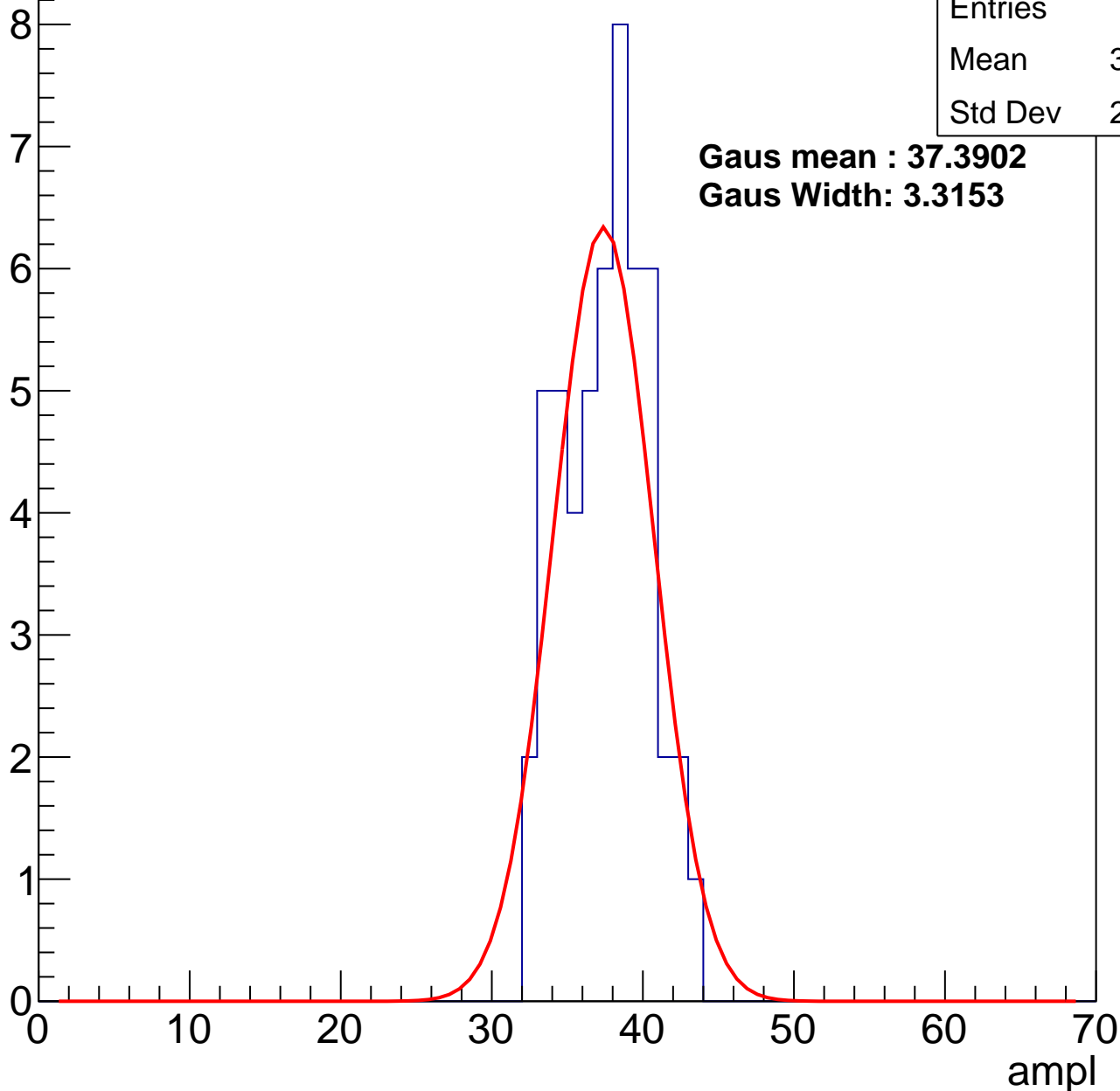
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	37.08
Std Dev	2.772

**Gaus mean : 37.3902**

**Gaus Width: 3.3153**



# B0L001S, U6-ch16, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	84
Mean	43.73
Std Dev	3.701

**Gaus mean : 44.3255**

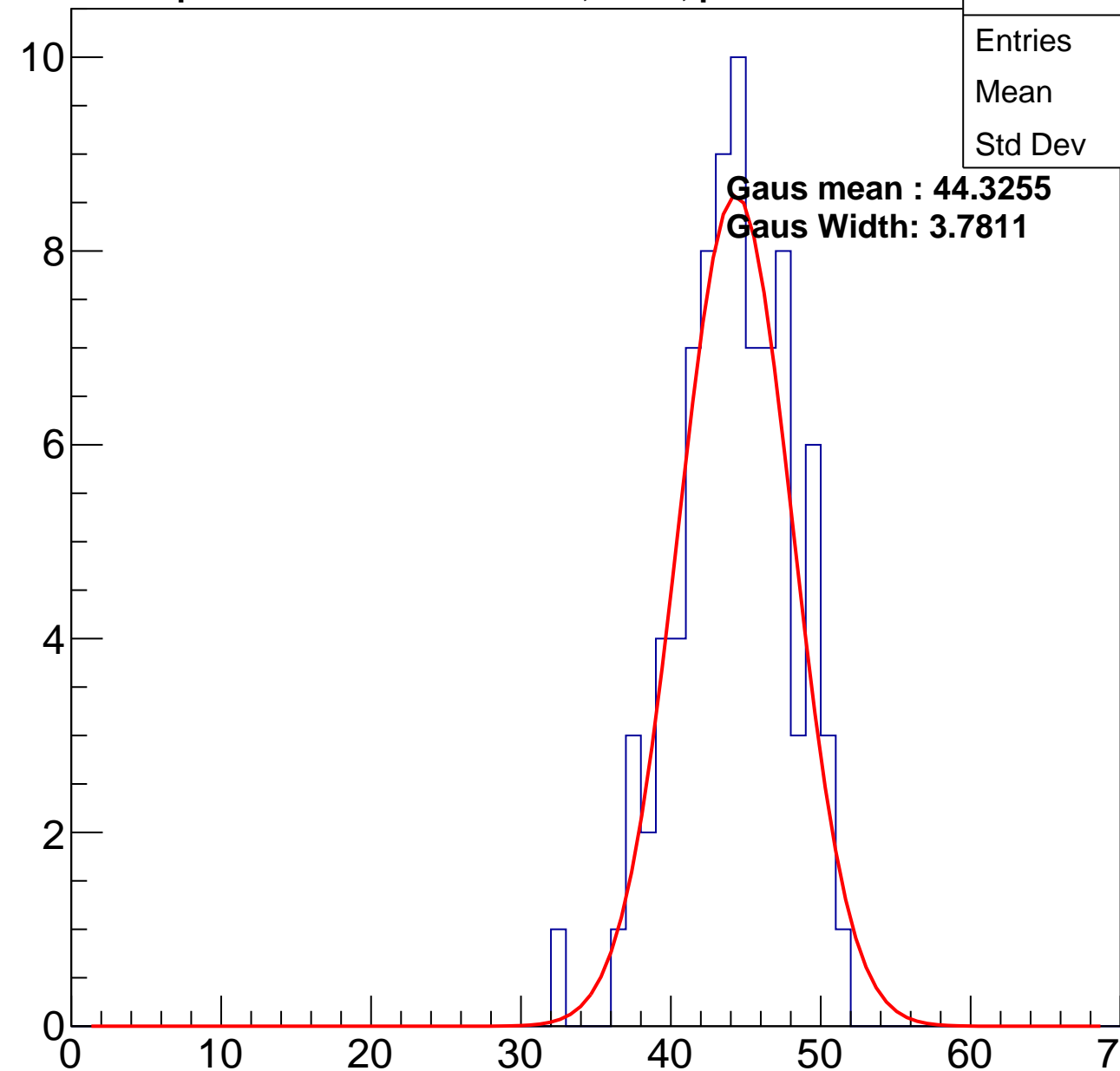
**Gaus Width: 3.7811**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

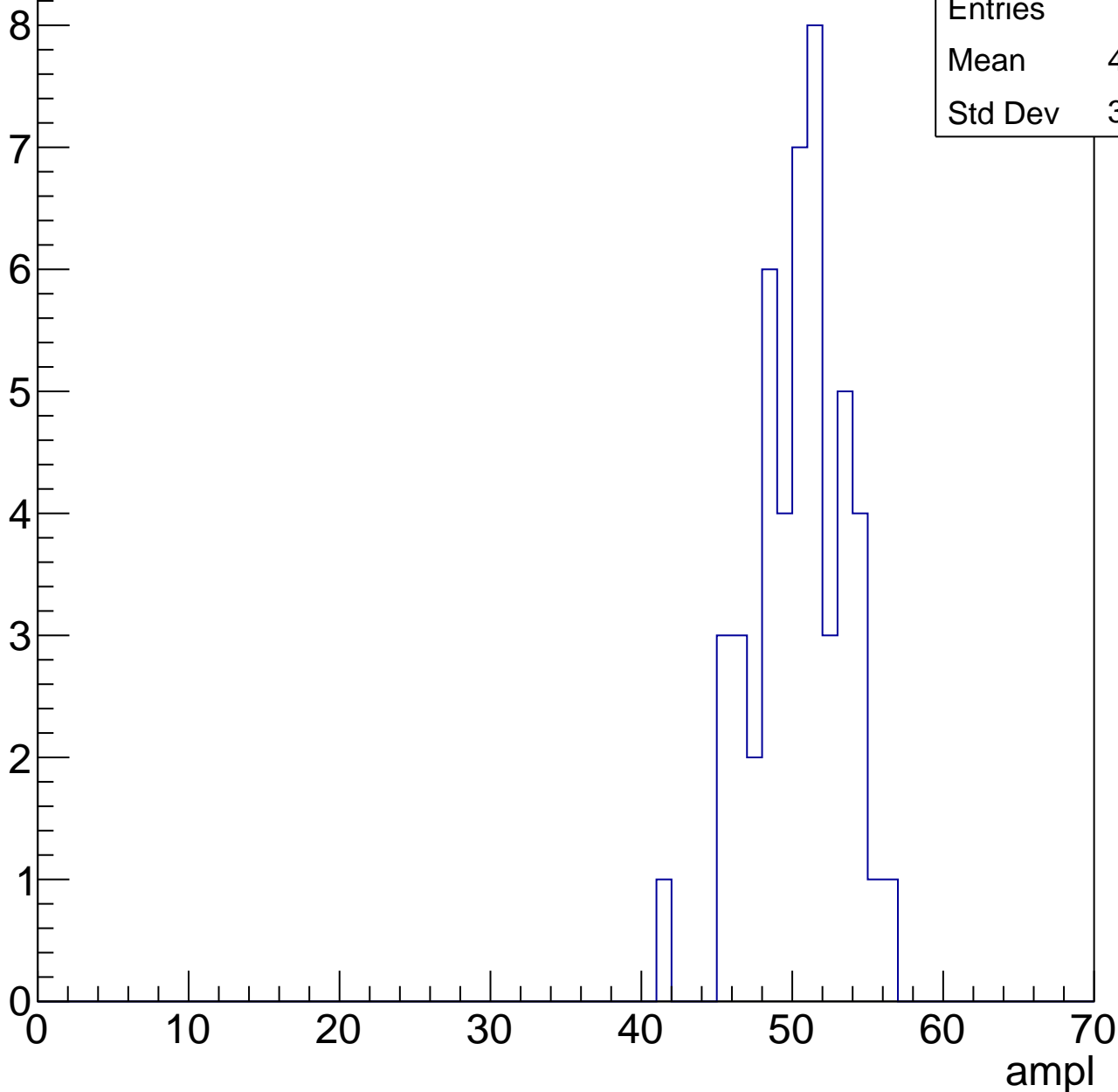


# B0L001S, U6-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	49.96
Std Dev	3.027

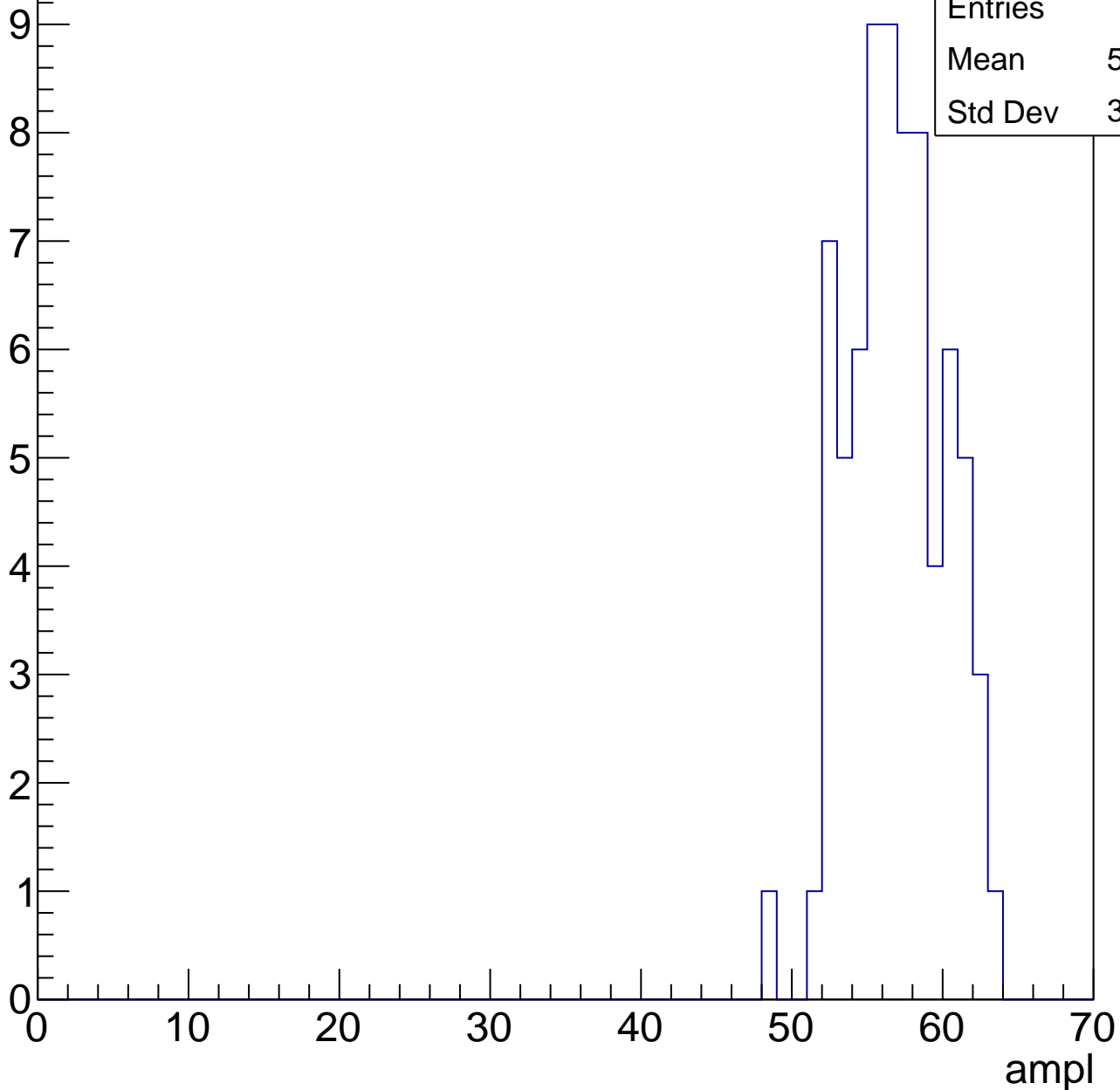


# B0L001S, U6-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	56.45
Std Dev	3.136

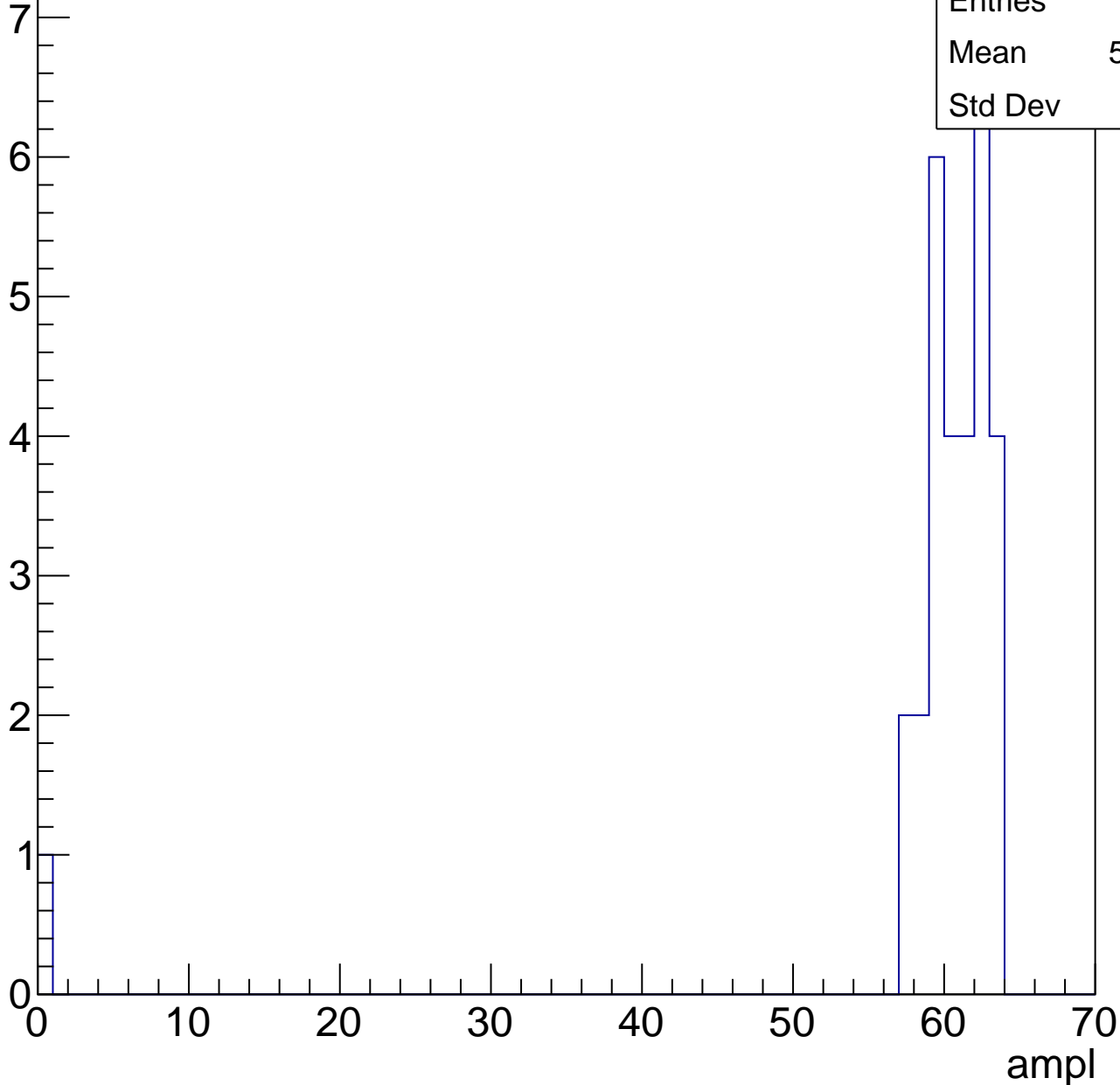


# B0L001S, U6-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	30
Mean	58.47
Std Dev	11

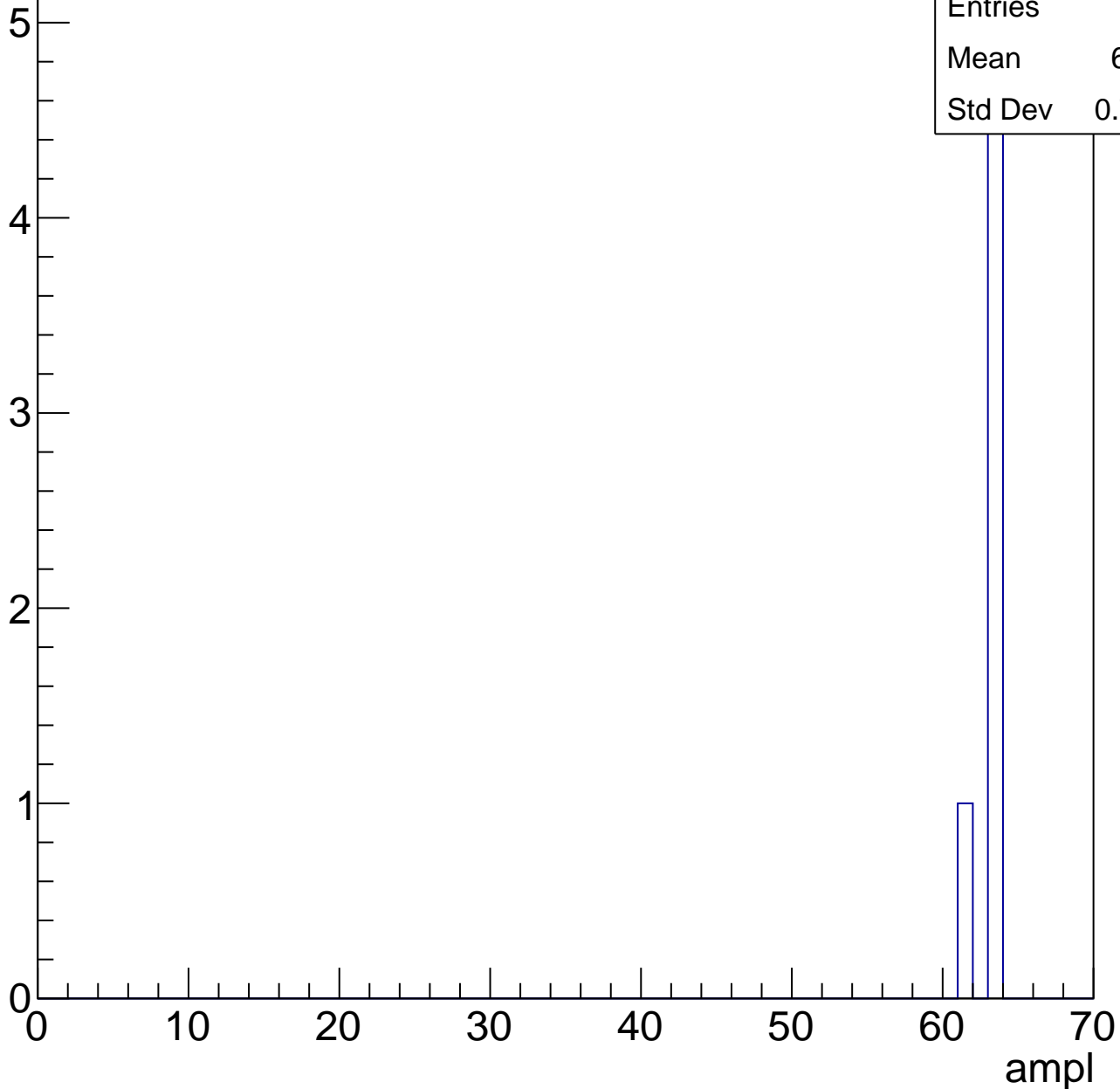


# B0L001S, U6-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	6
Mean	62.67
Std Dev	0.7454





# B0L001S, U6-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U6-ch17, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	74
Mean	31.53
Std Dev	4.78

**Gaus mean : 32.4049**

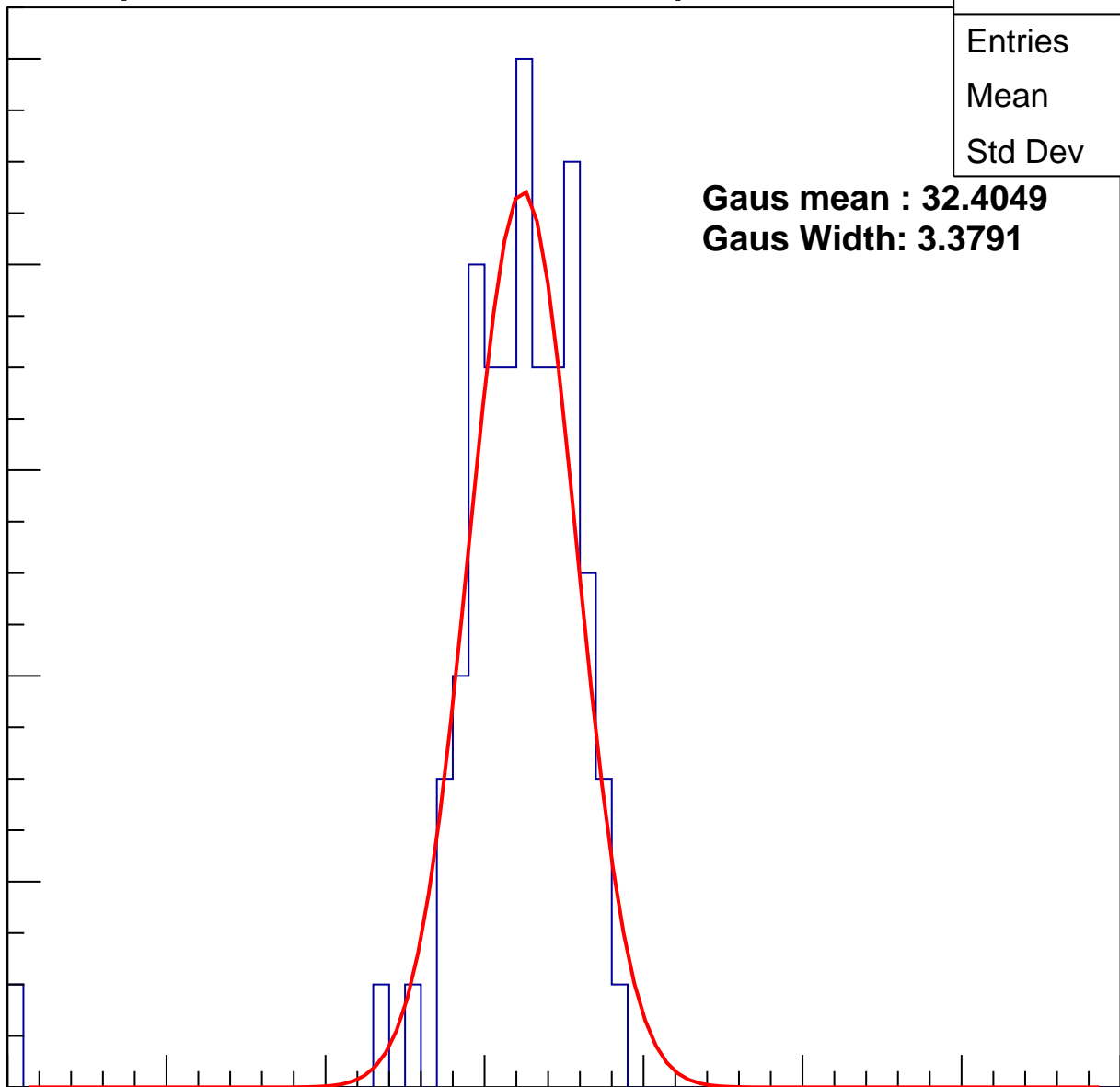
**Gaus Width: 3.3791**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U6-ch17, adc1

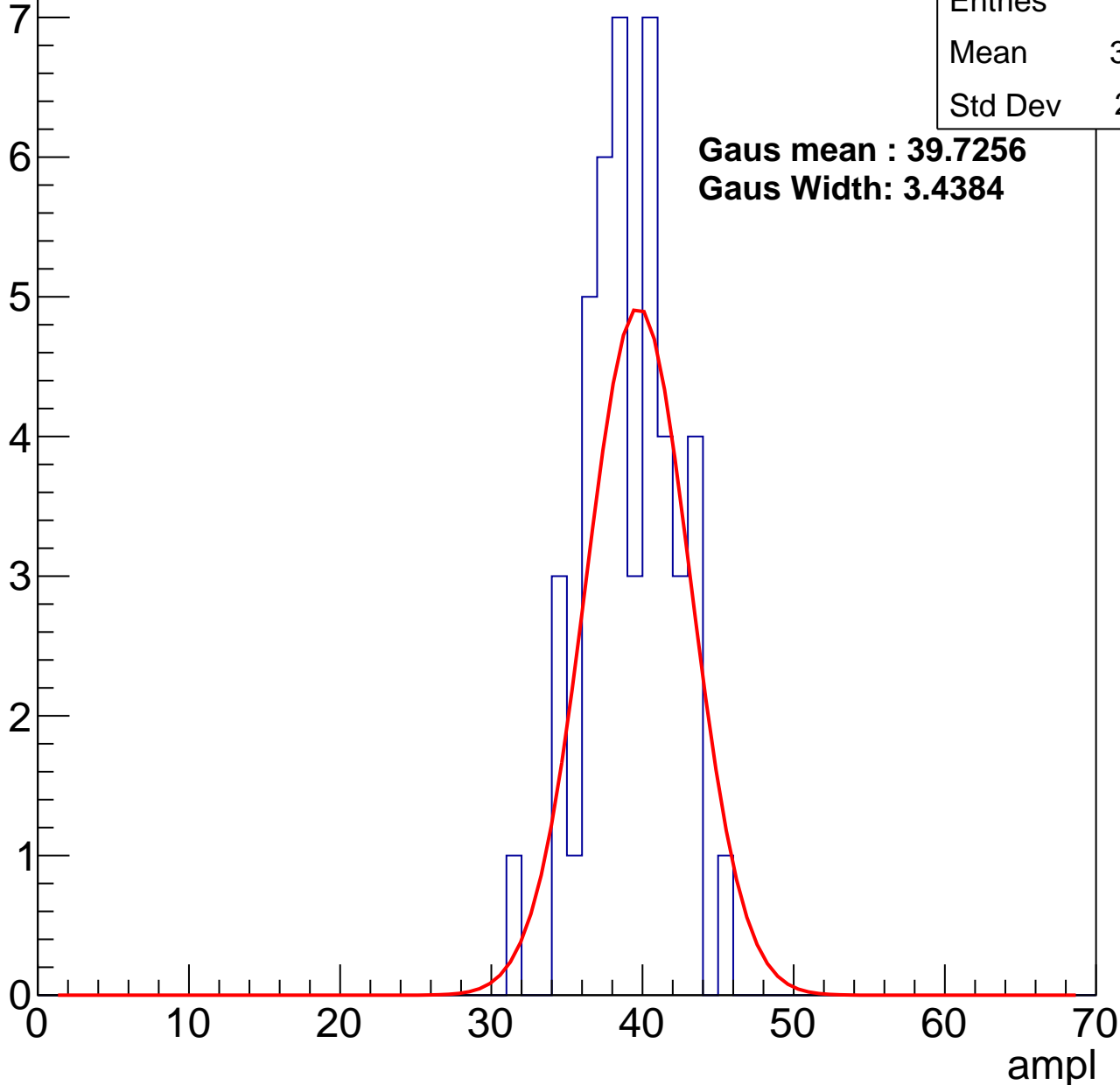
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	45
Mean	38.67
Std Dev	2.891

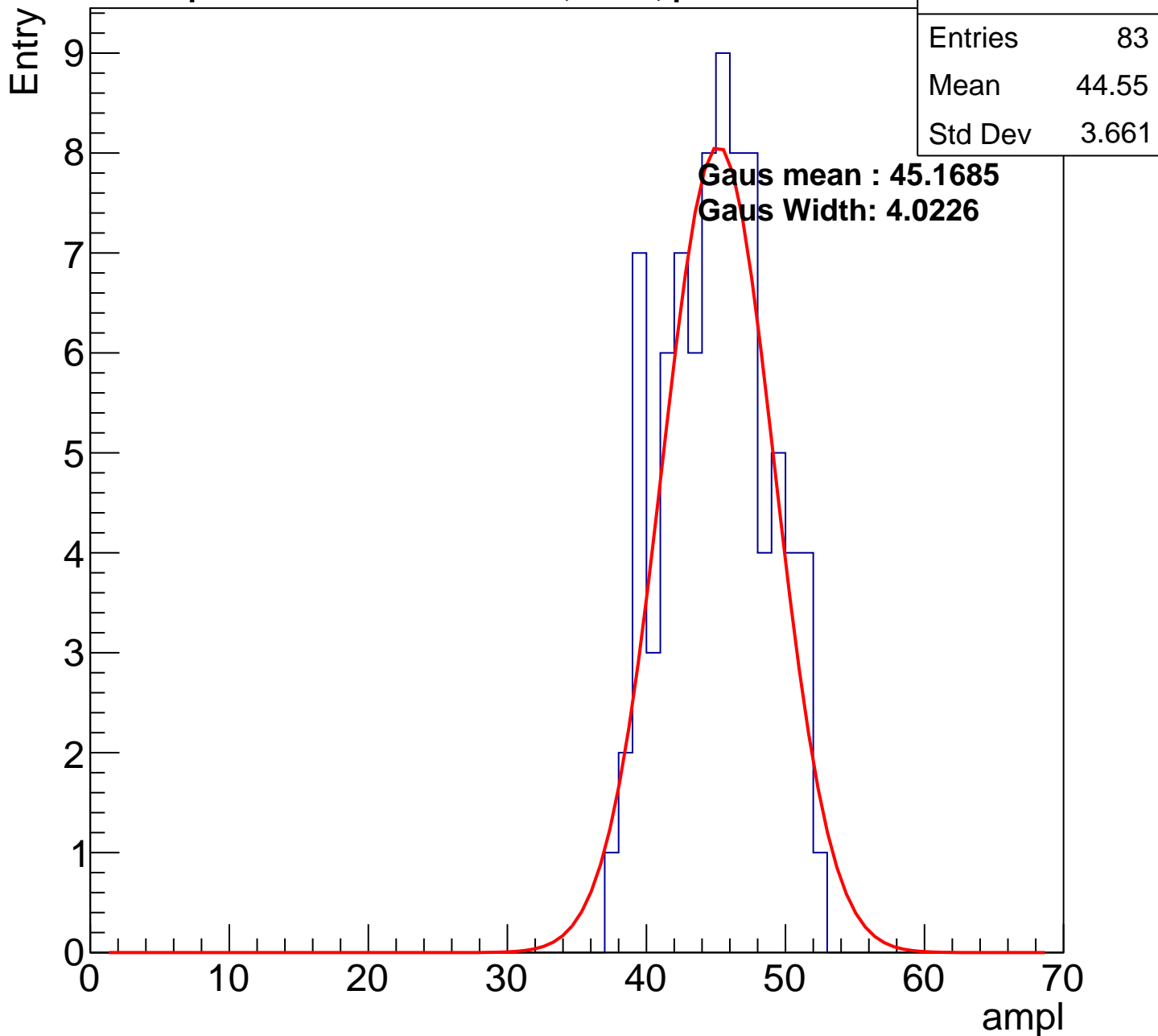
**Gaus mean : 39.7256**

**Gaus Width: 3.4384**



# B0L001S, U6-ch17, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

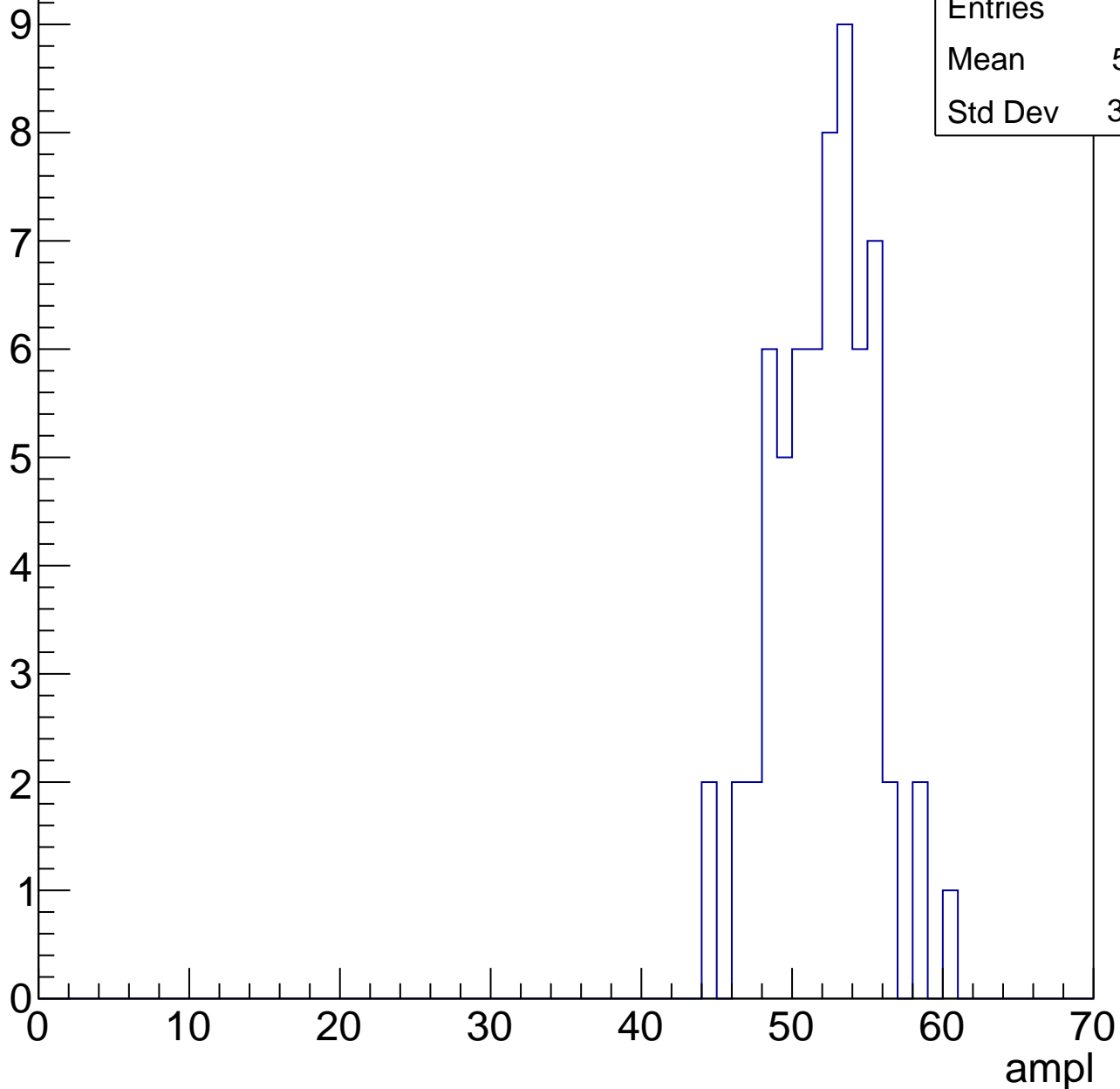


# B0L001S, U6-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	51.61
Std Dev	3.248



# B0L001S, U6-ch17, adc4

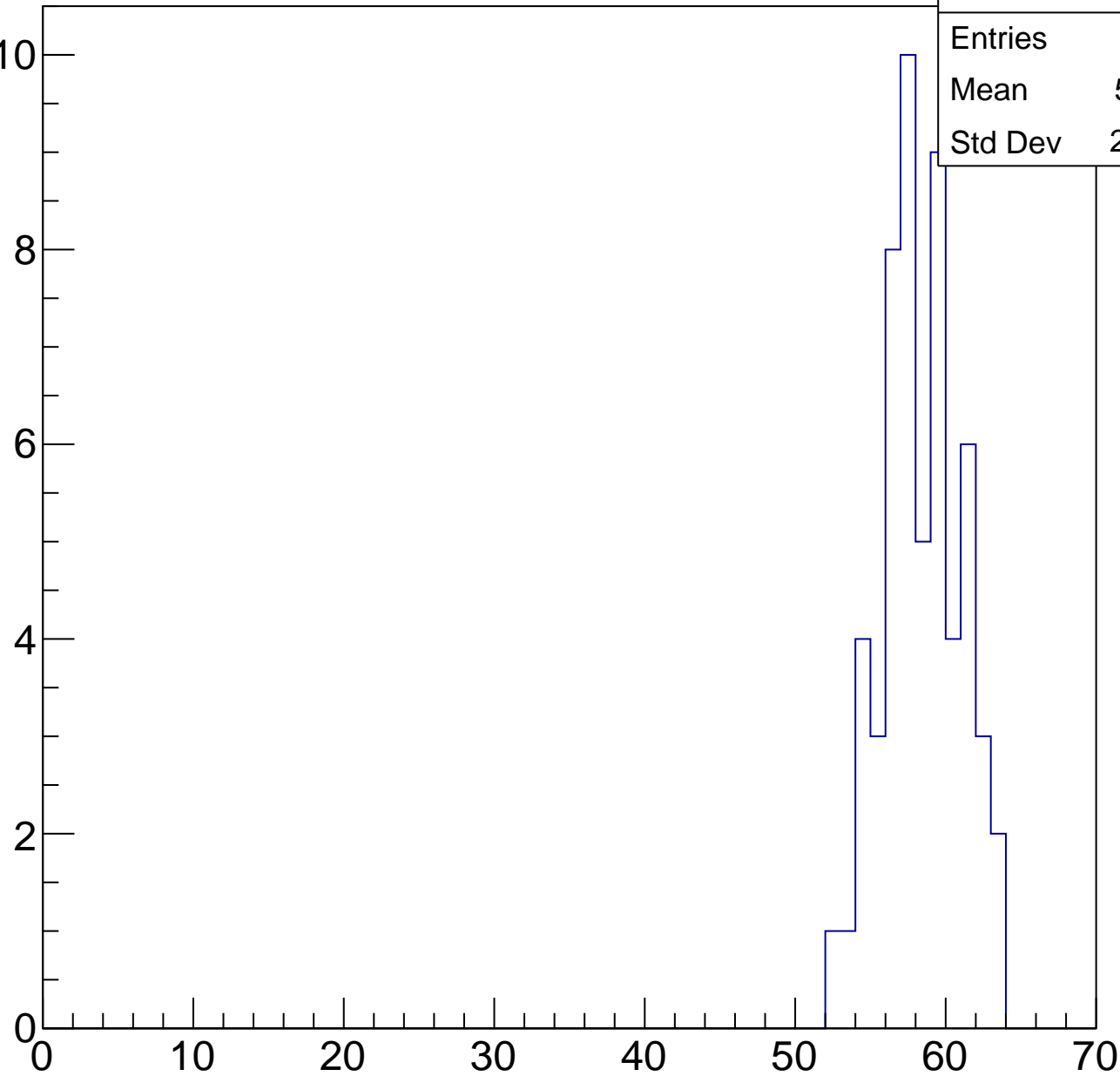
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

10  
8  
6  
4  
2  
0

Entries	56
Mean	57.91
Std Dev	2.572

ampl

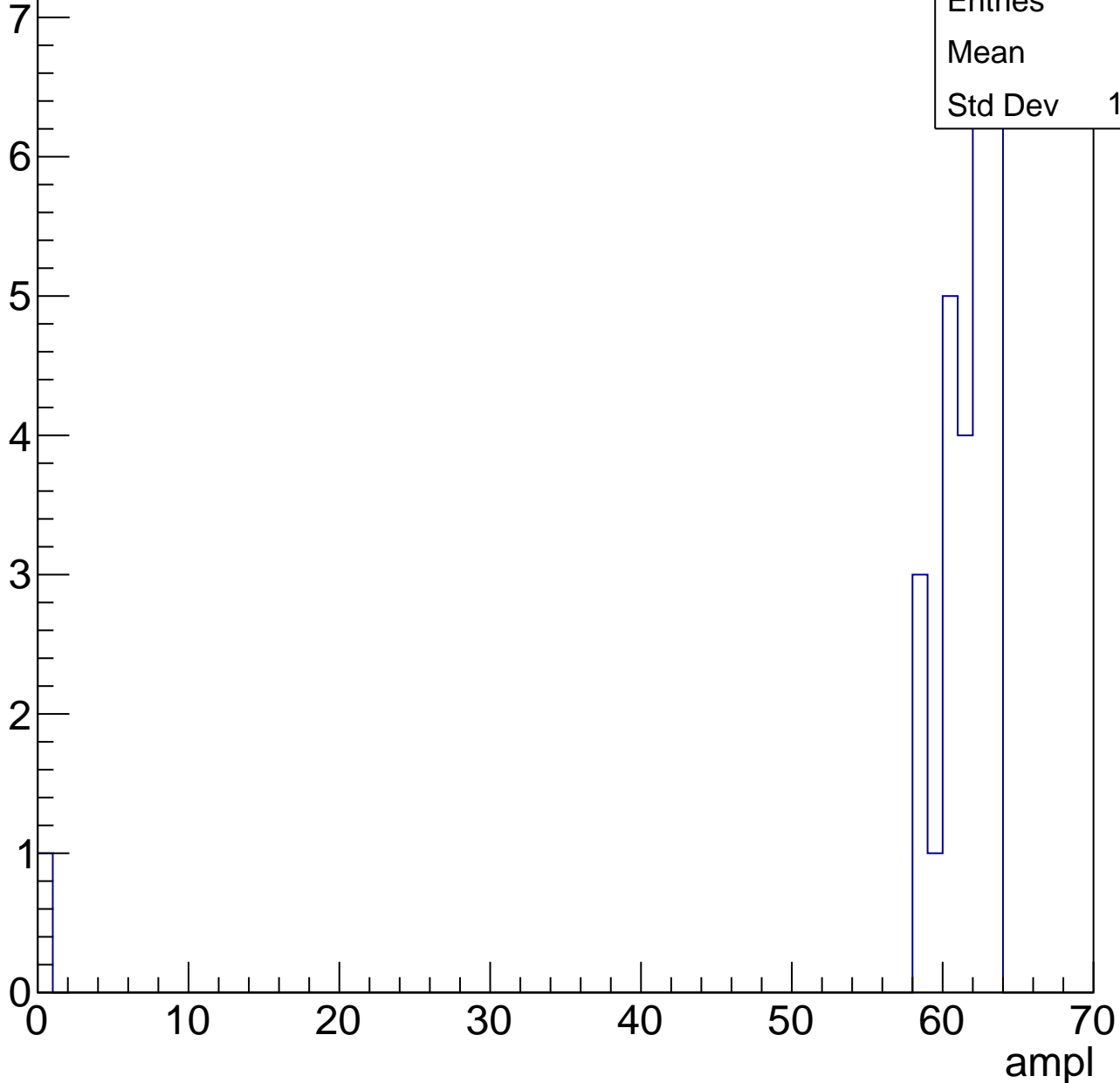


# B0L001S, U6-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	28
Mean	59
Std Dev	11.46



# B0L001S, U6-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U6-ch18, adc0

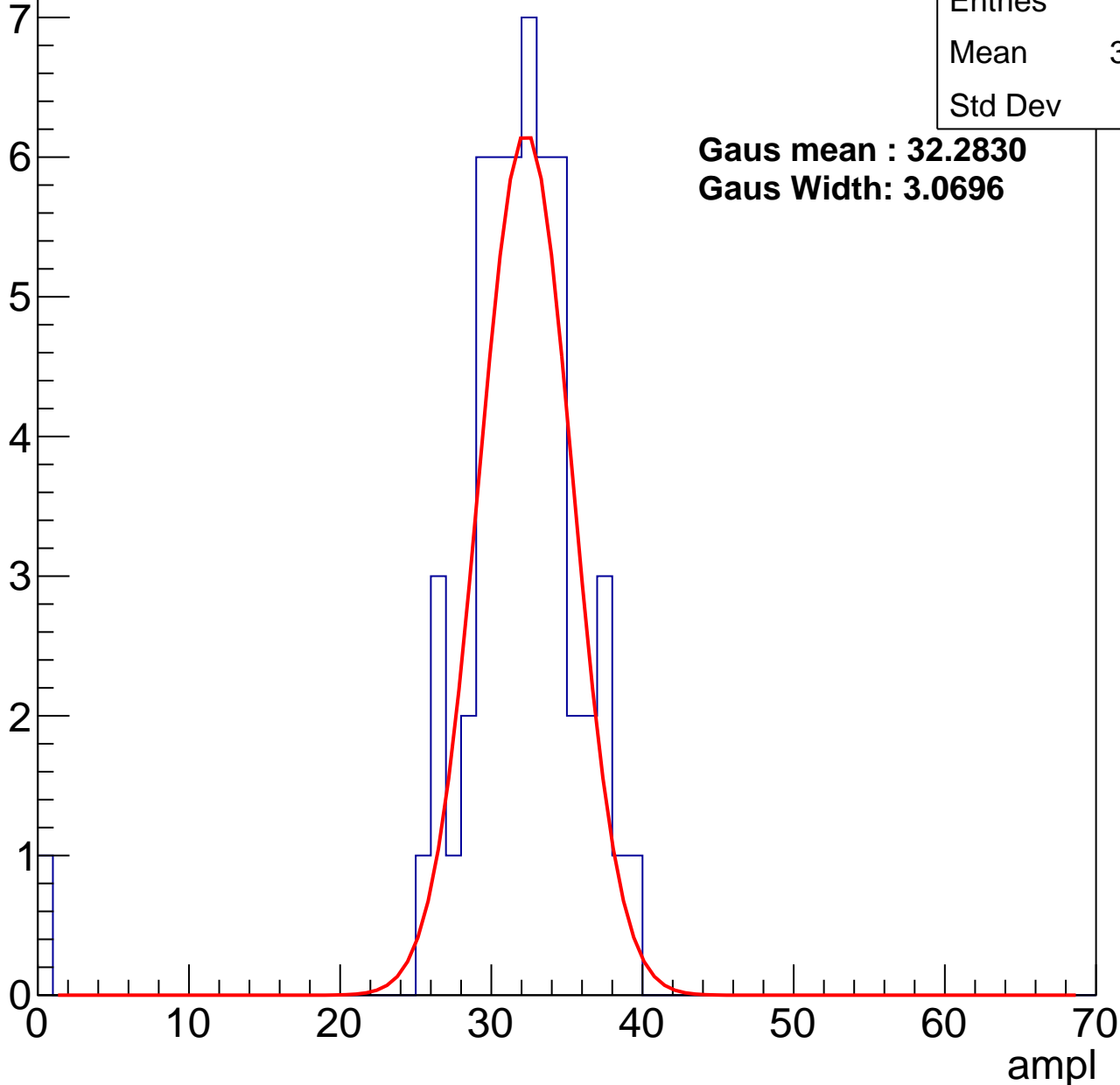
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	31.15
Std Dev	5.31

**Gaus mean : 32.2830**

**Gaus Width: 3.0696**



# B0L001S, U6-ch18, adc1

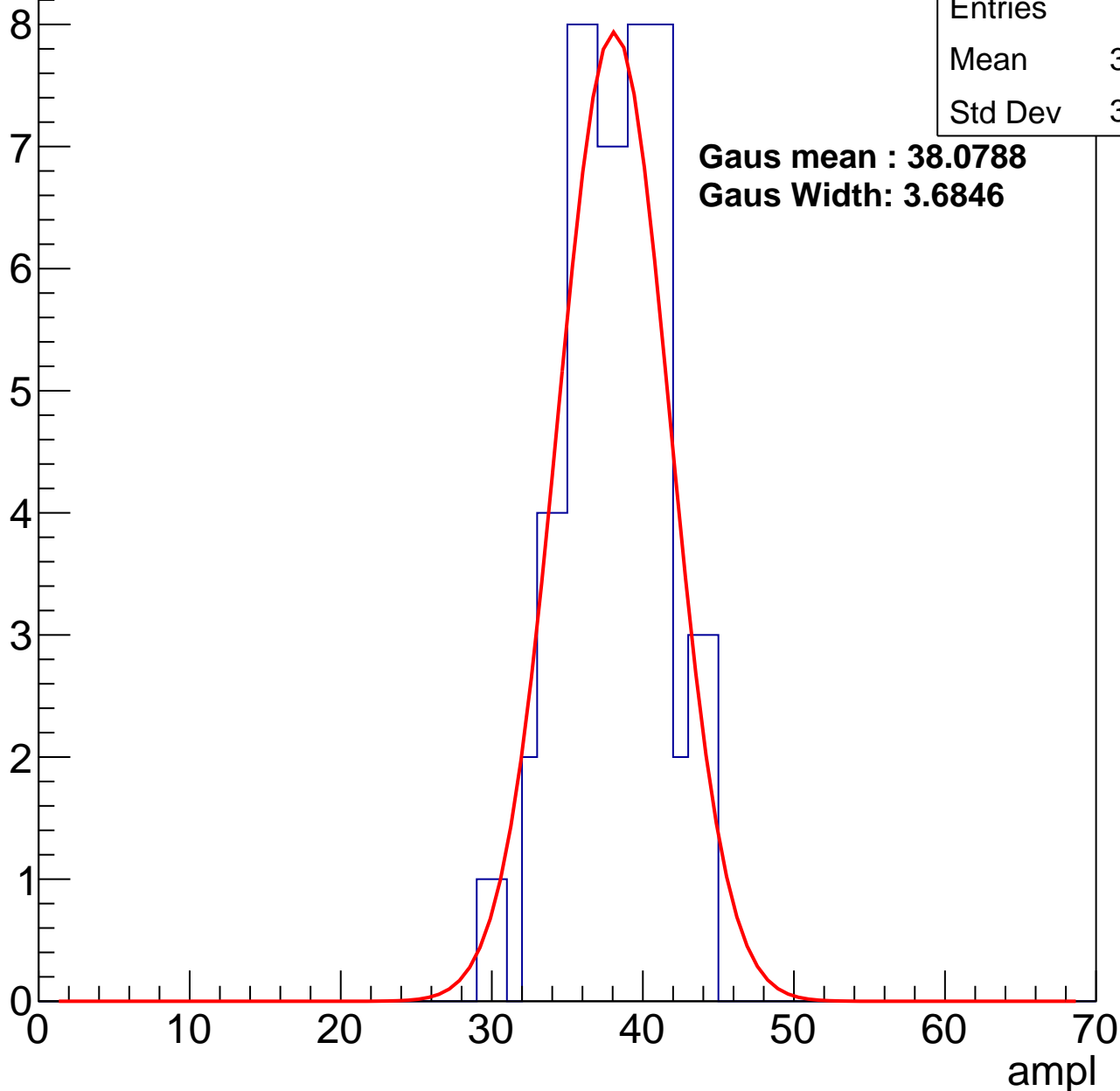
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	37.69
Std Dev	3.312

**Gaus mean : 38.0788**

**Gaus Width: 3.6846**



# B0L001S, U6-ch18, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	66
Mean	44.89
Std Dev	2.965

**Gaus mean : 45.3547**

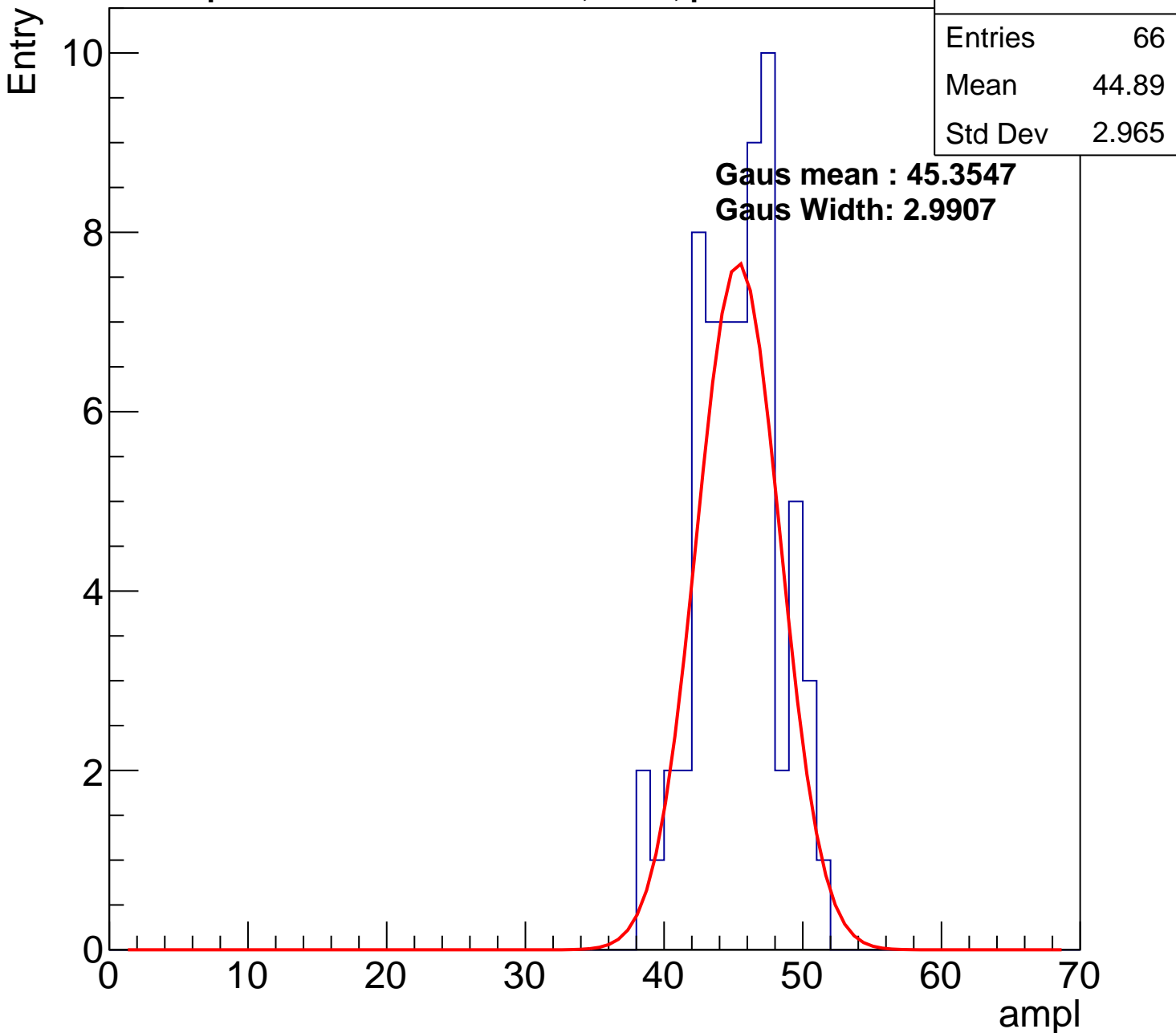
**Gaus Width: 2.9907**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

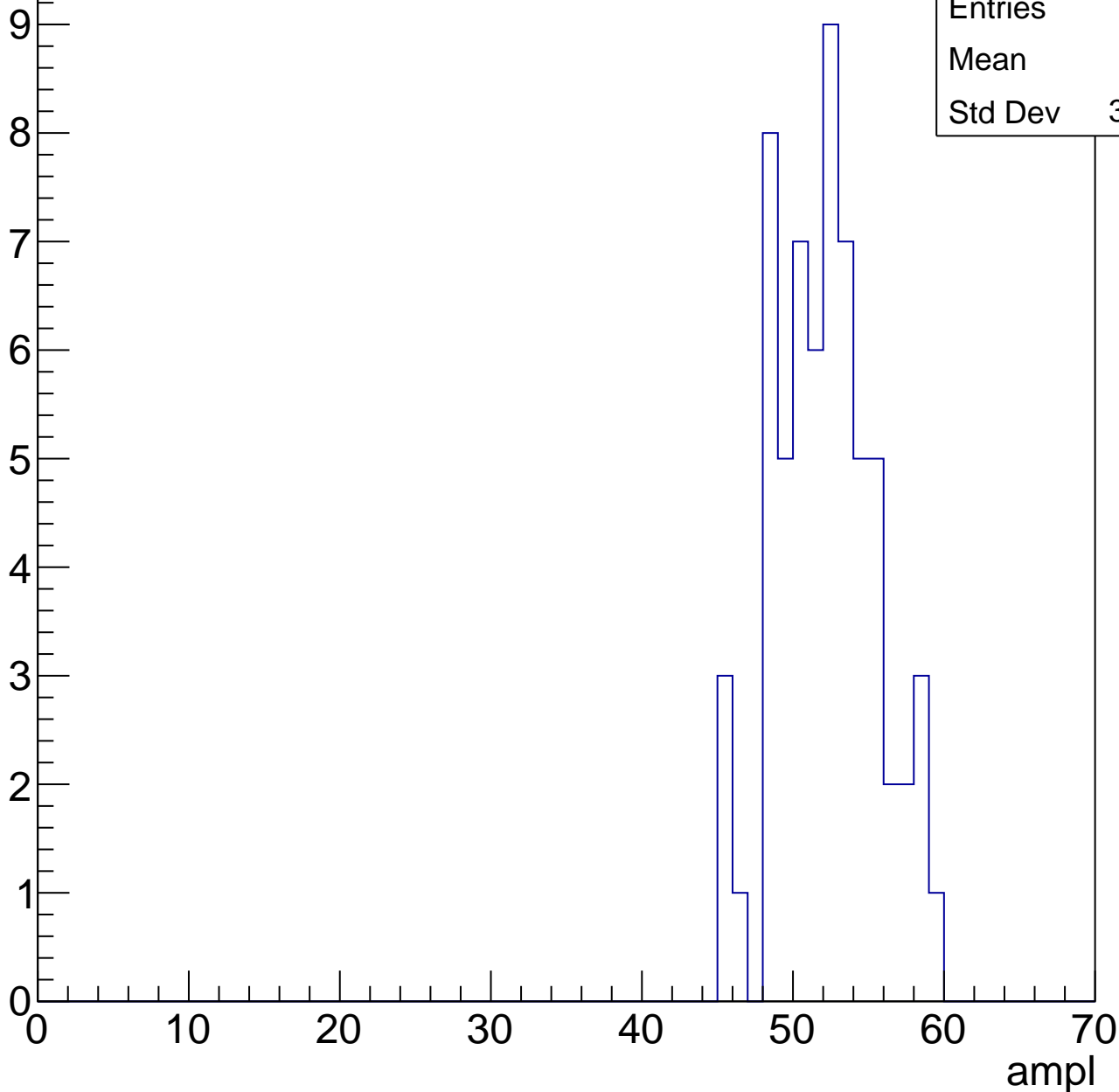


# B0L001S, U6-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	51.7
Std Dev	3.296

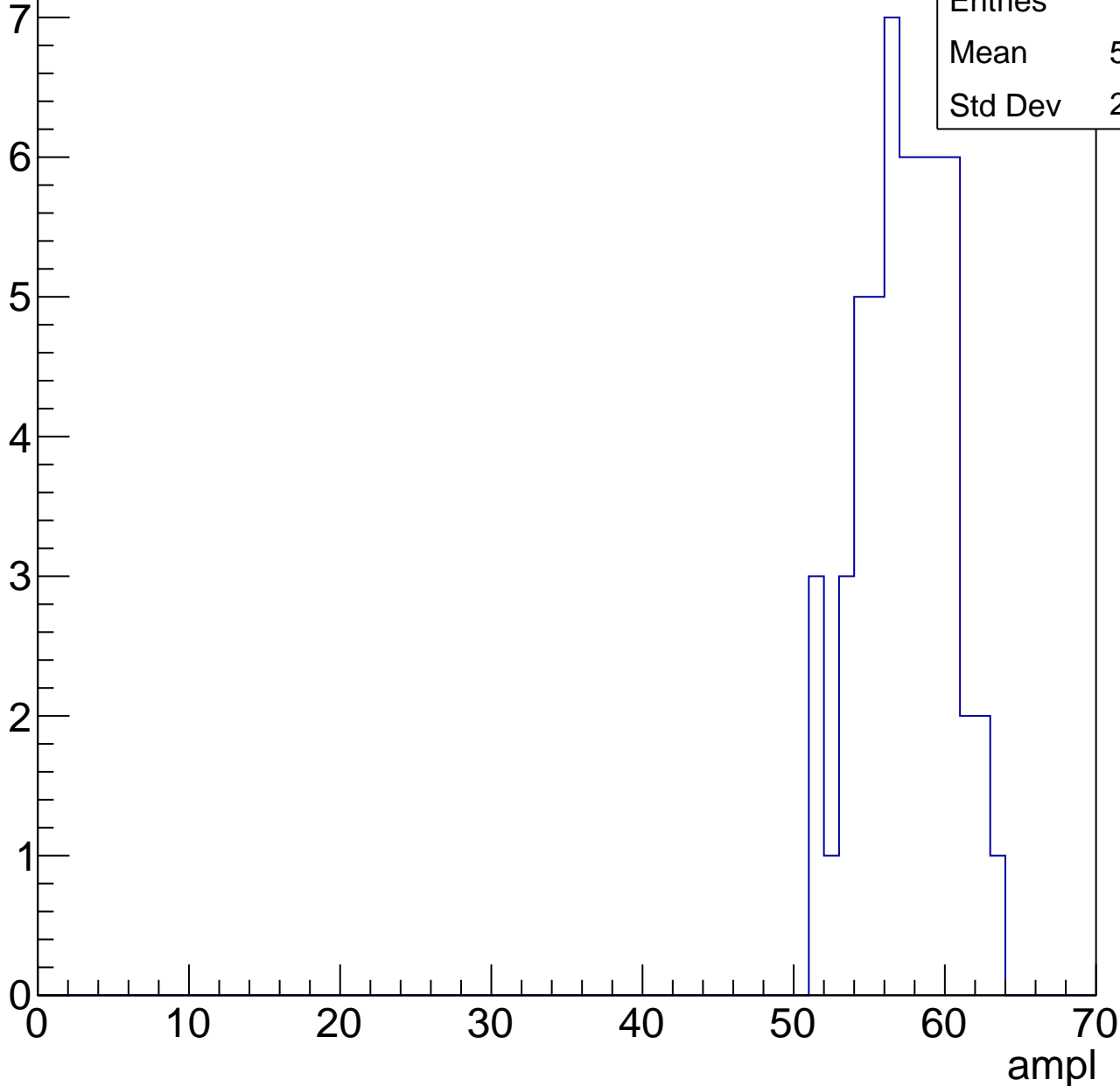


# B0L001S, U6-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	56.87
Std Dev	2.927



# B0L001S, U6-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

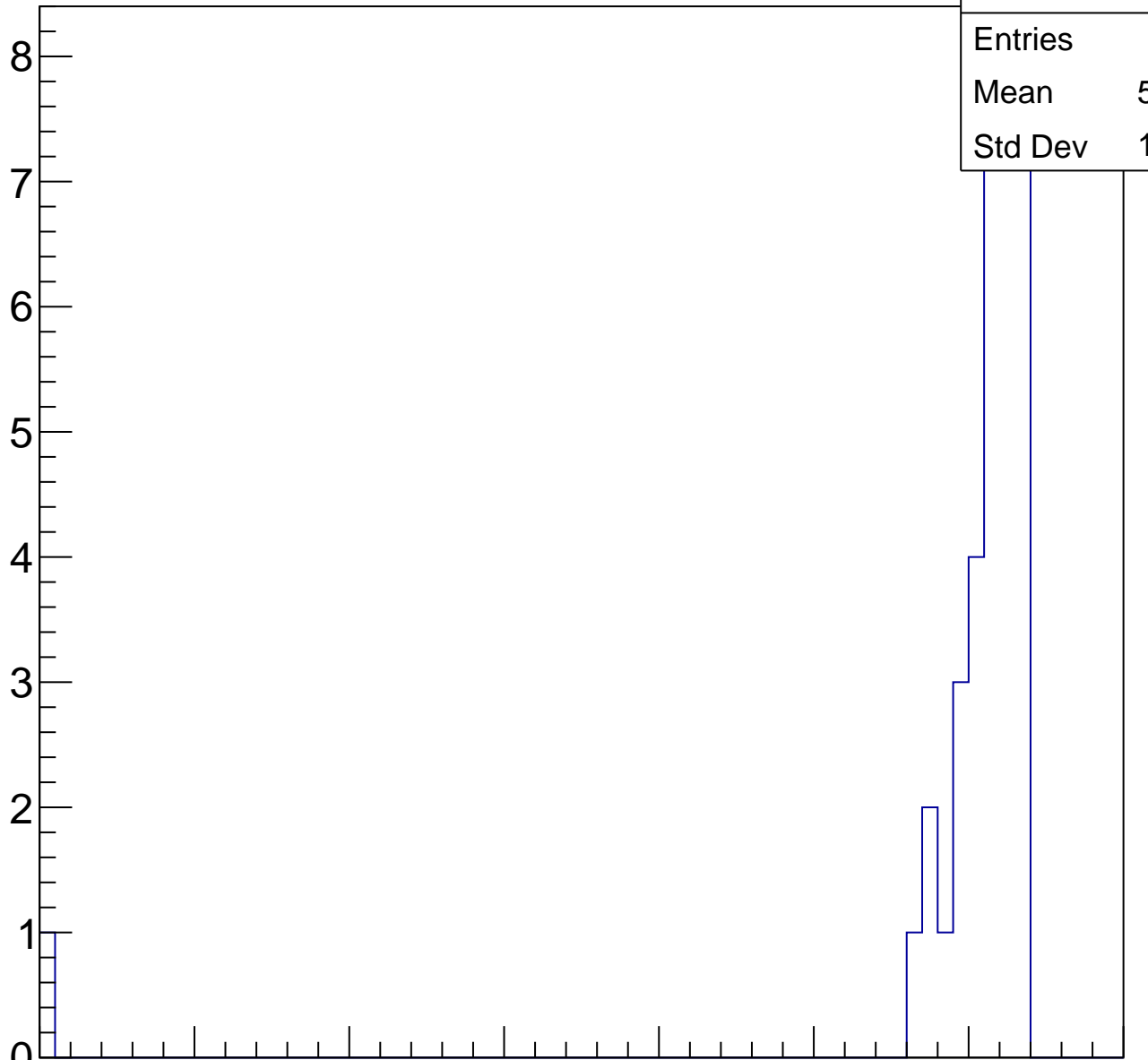
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	36
Mean	59.25
Std Dev	10.18

ampl

0 10 20 30 40 50 60 70



# B0L001S, U6-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U6-ch19, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	86
Mean	29.42
Std Dev	6.699

**Gaus mean : 30.8259**

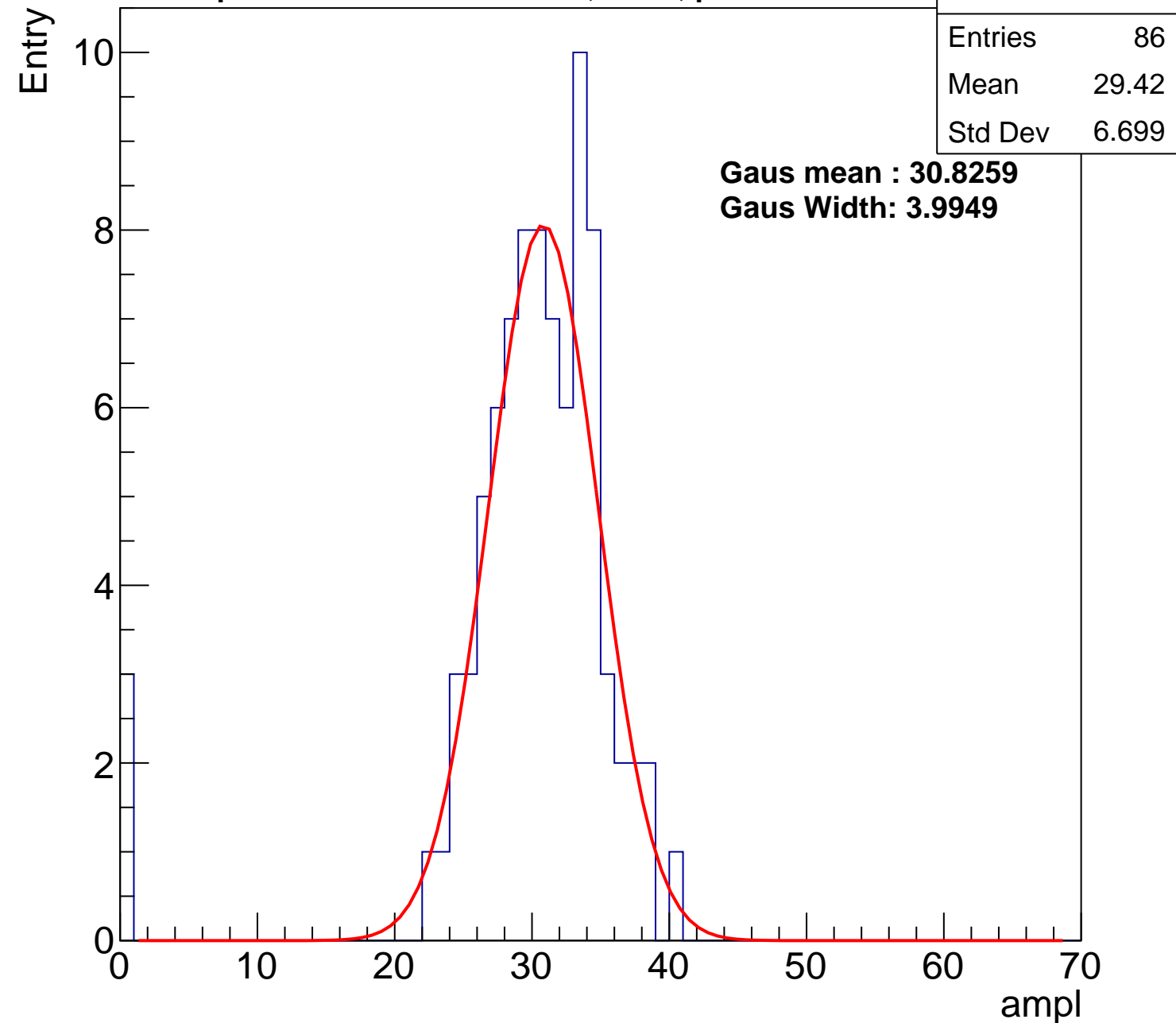
**Gaus Width: 3.9949**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U6-ch19, adc1

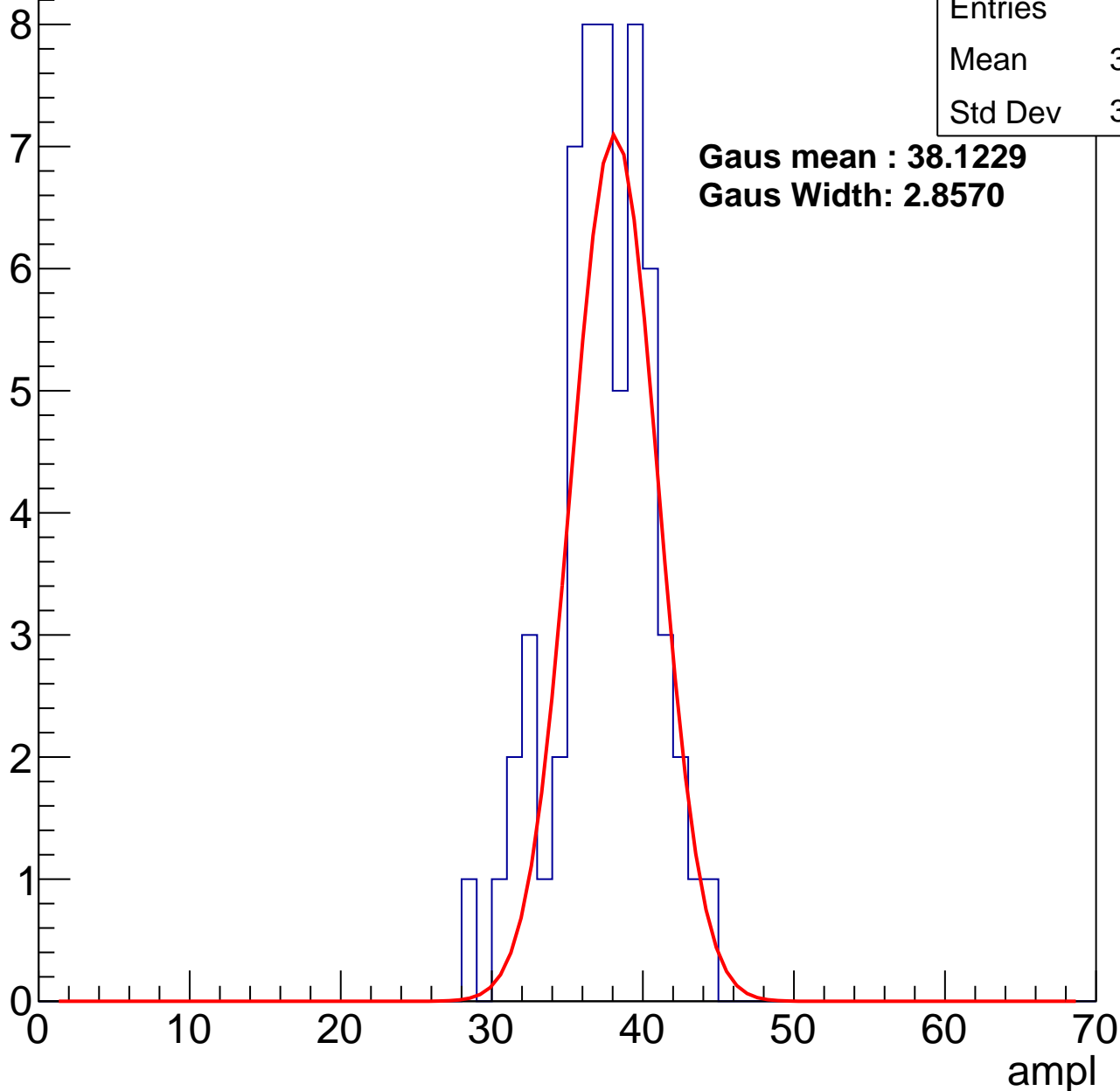
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	36.98
Std Dev	3.244

**Gaus mean : 38.1229**

**Gaus Width: 2.8570**



# B0L001S, U6-ch19, adc2

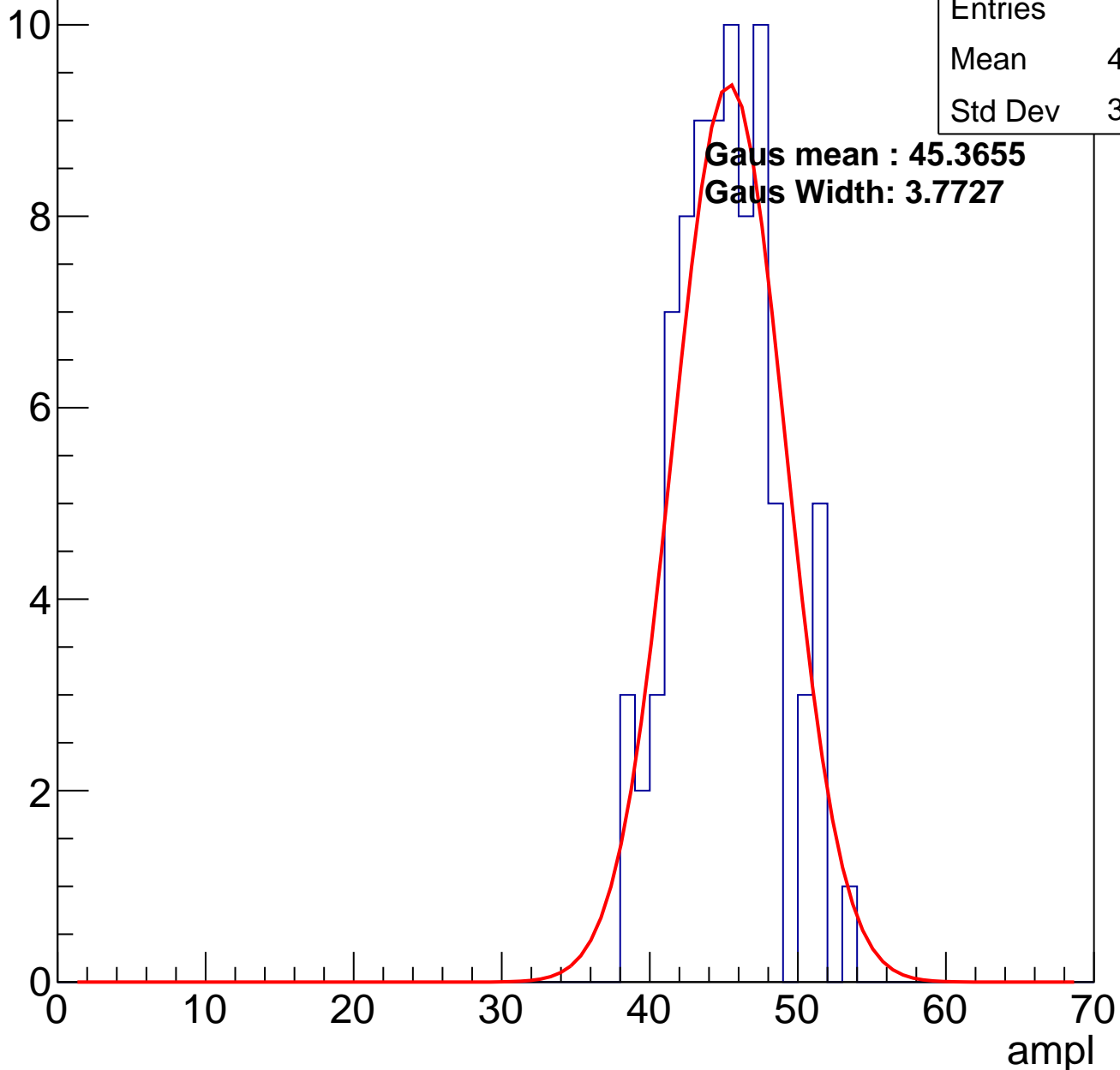
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	83
Mean	44.63
Std Dev	3.336

**Gaus mean : 45.3655**

**Gaus Width: 3.7727**

Entry

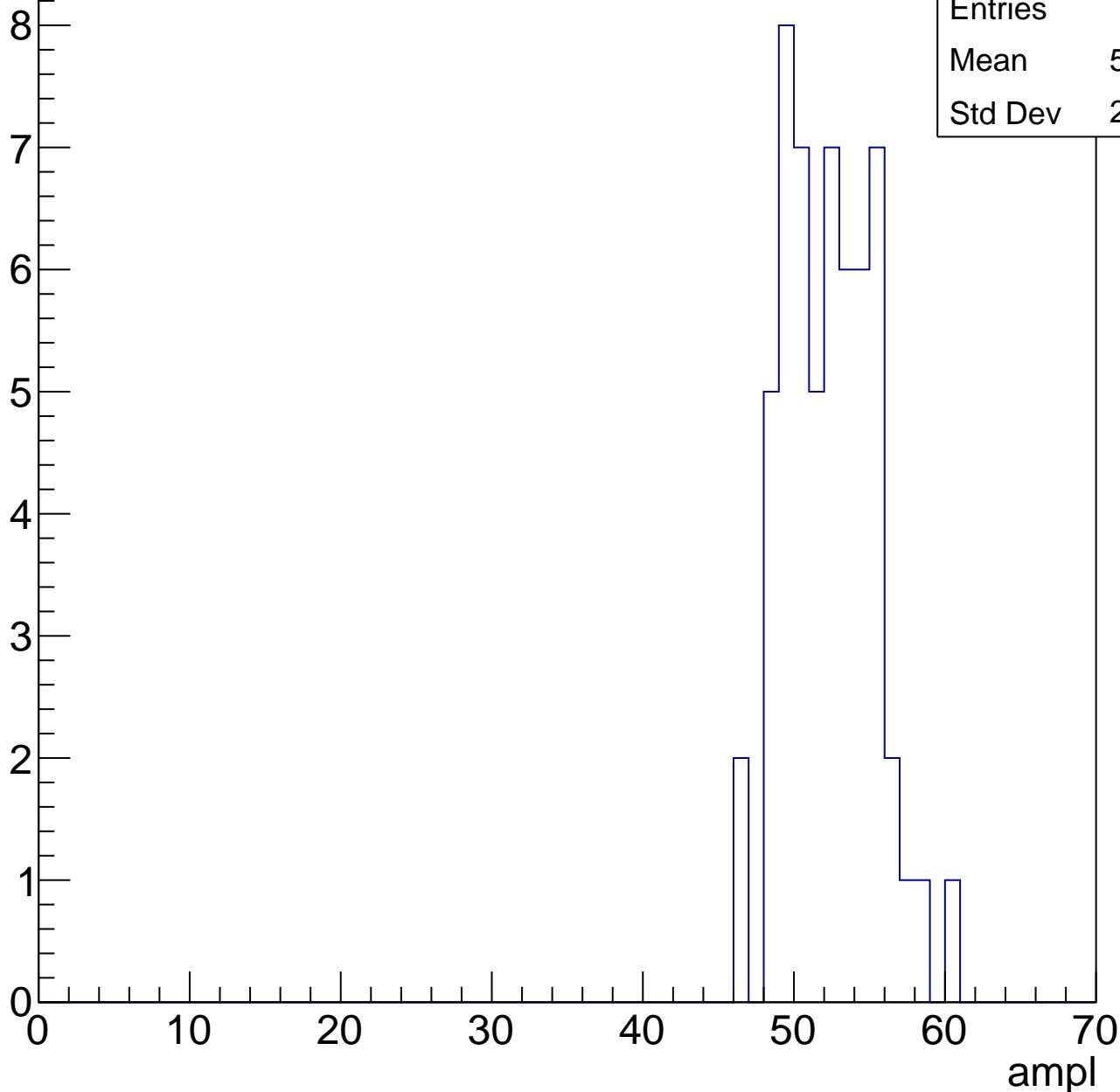


# B0L001S, U6-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	51.84
Std Dev	2.953

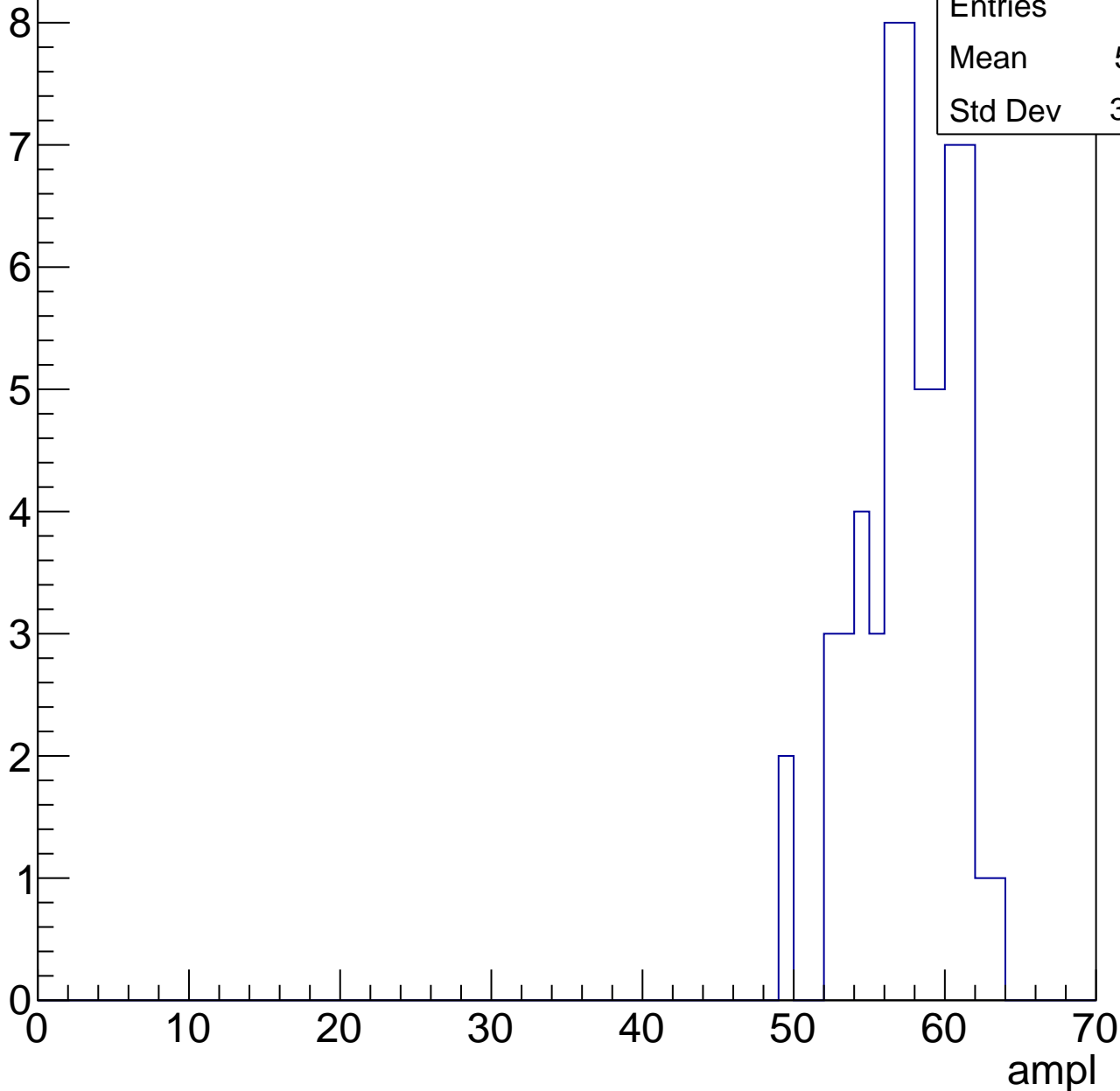


# B0L001S, U6-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	57.11
Std Dev	3.155

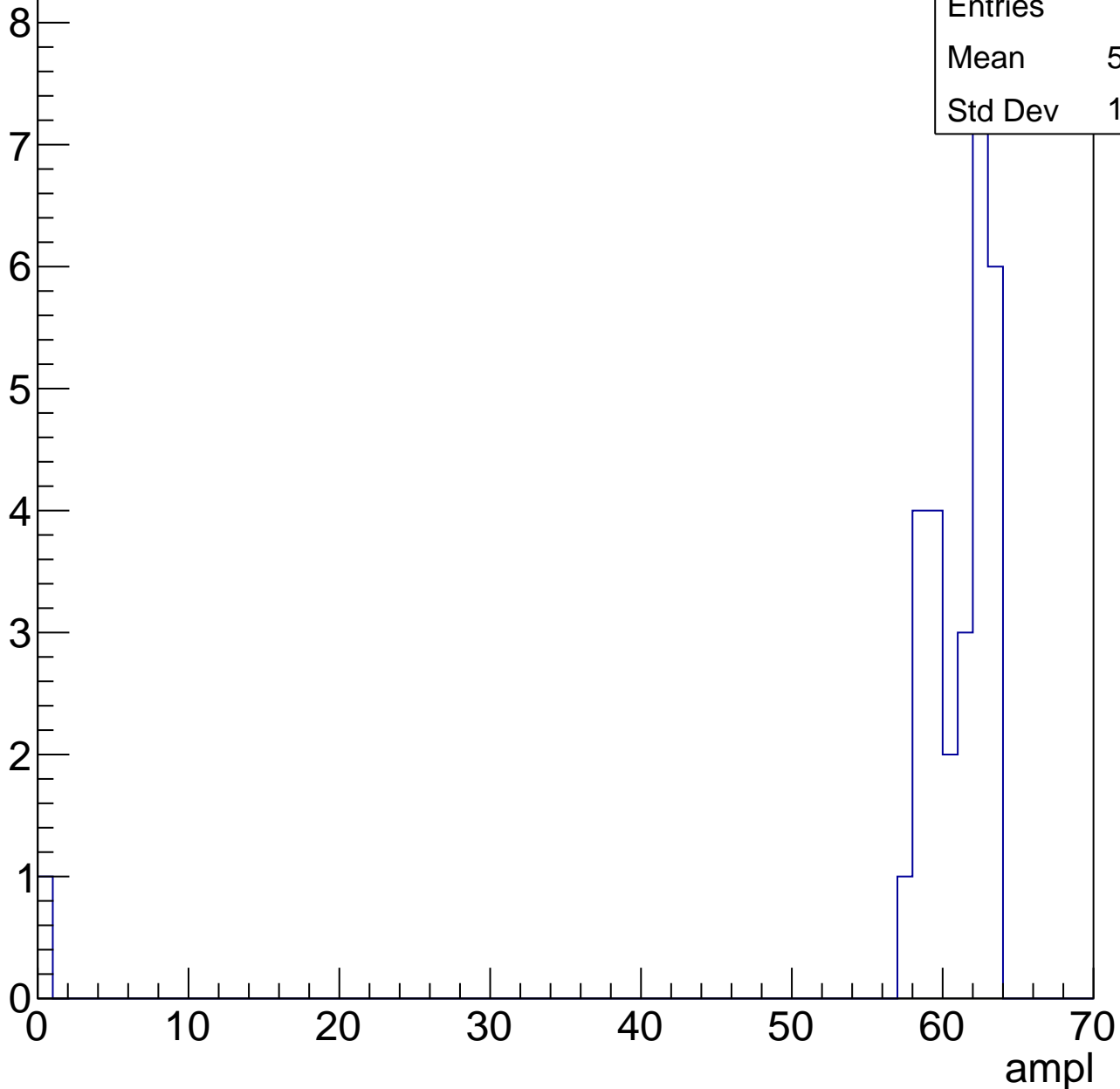


# B0L001S, U6-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	29
Mean	58.69
Std Dev	11.25



# B0L001S, U6-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

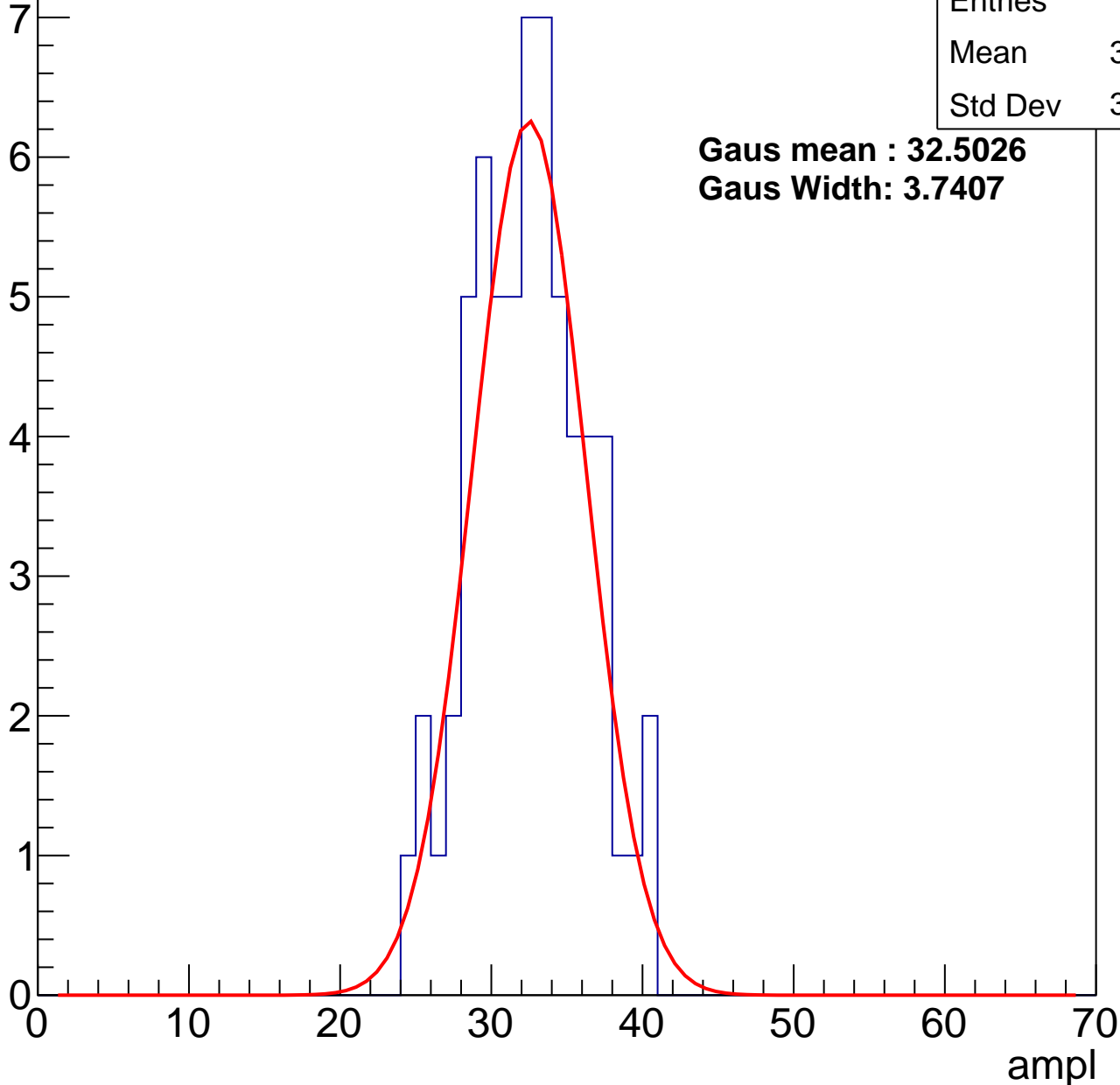
# B0L001S, U6-ch20, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	32.05
Std Dev	3.696

**Gaus mean : 32.5026**  
**Gaus Width: 3.7407**



# B0L001S, U6-ch20, adc1

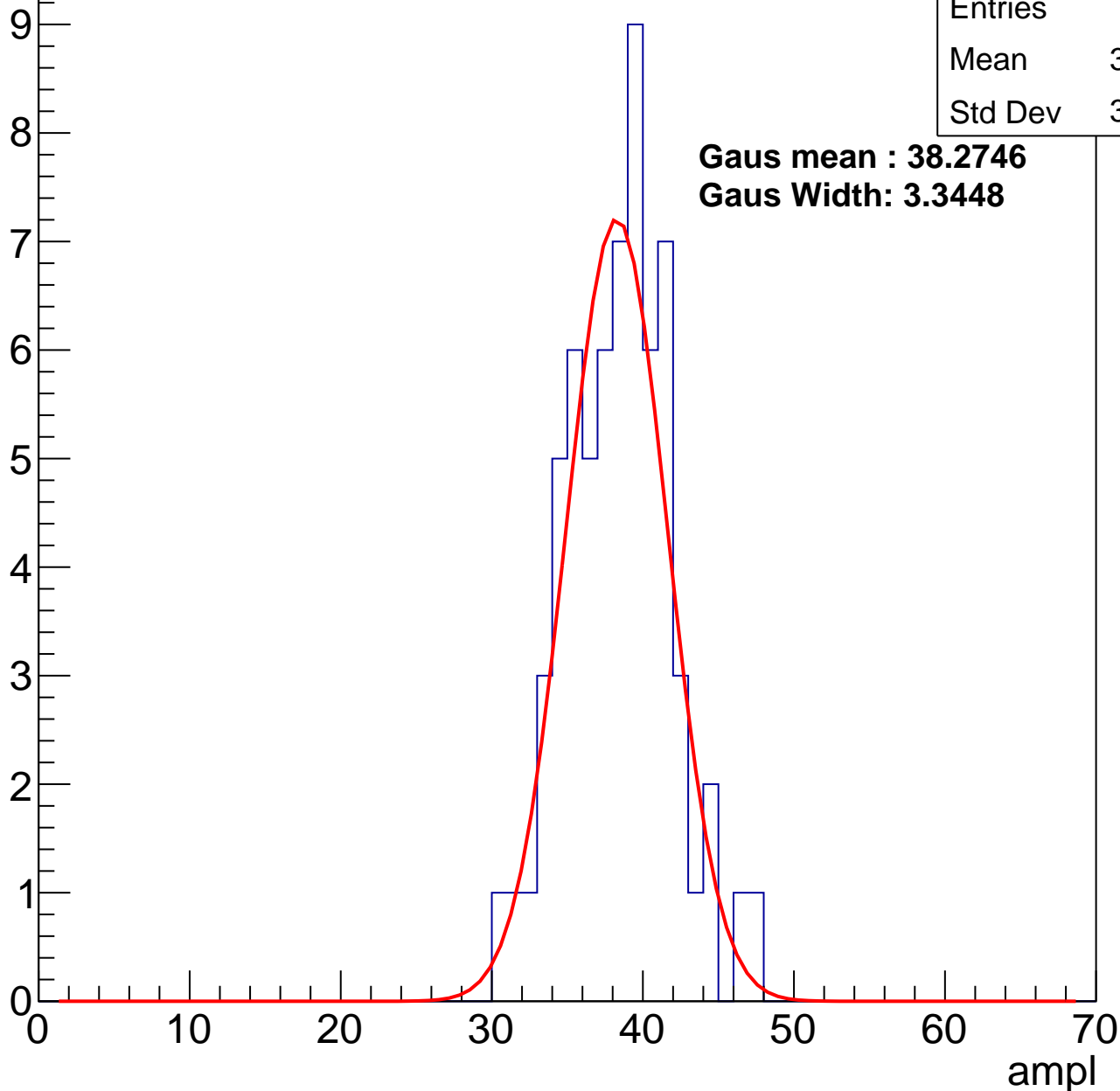
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	37.97
Std Dev	3.442

**Gaus mean : 38.2746**

**Gaus Width: 3.3448**



# B0L001S, U6-ch20, adc2

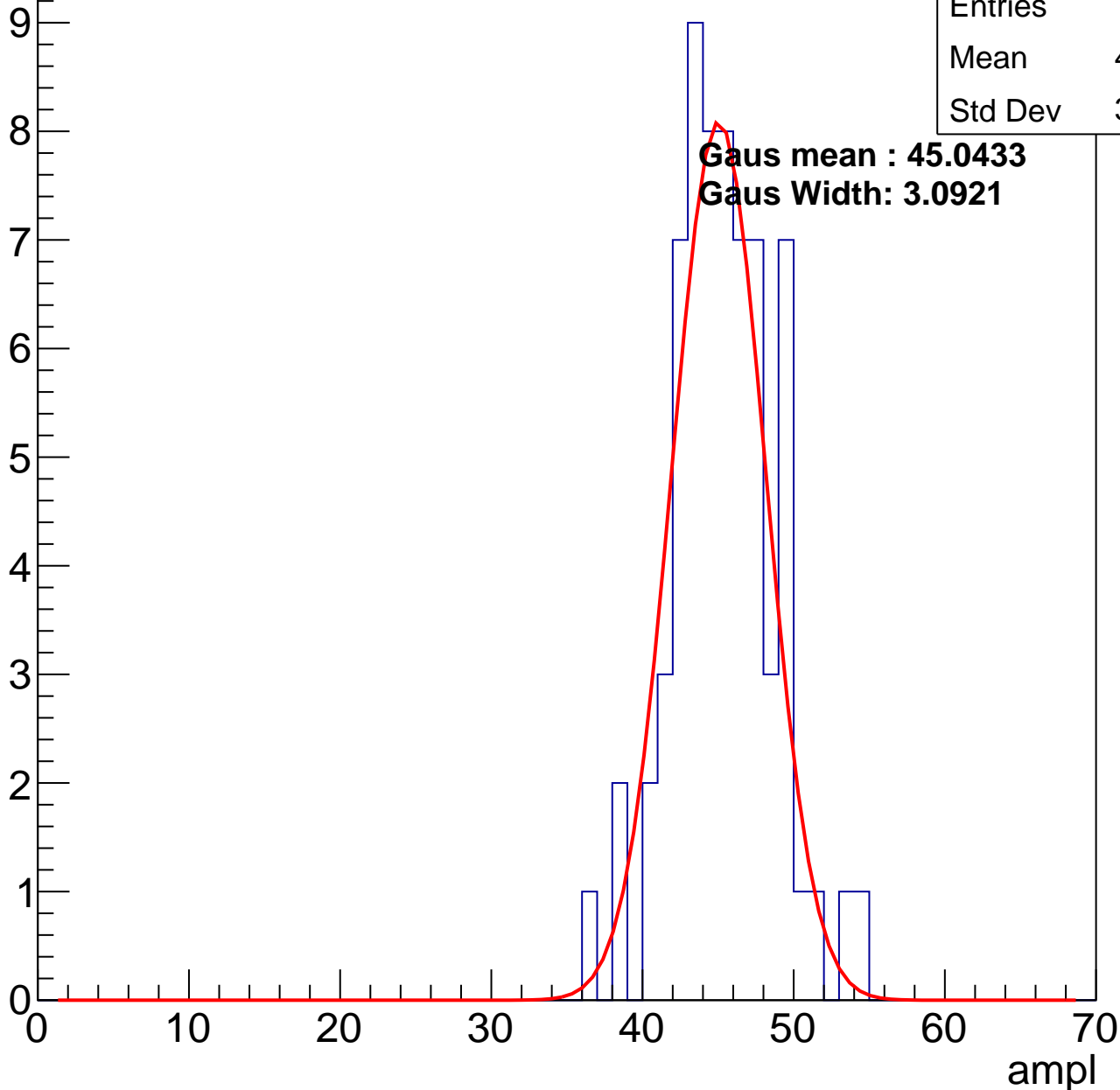
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	44.91
Std Dev	3.351

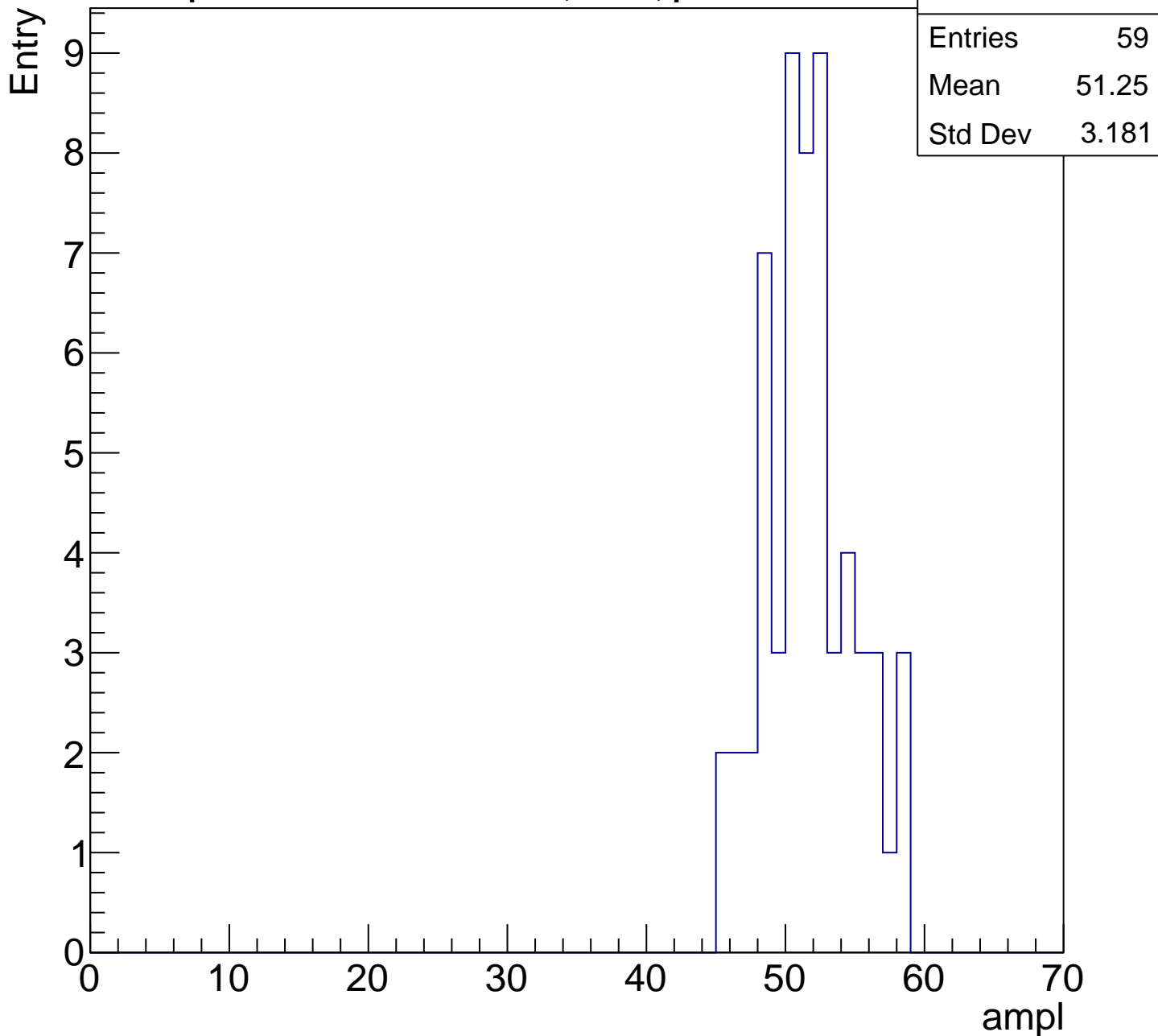
**Gaus mean : 45.0433**

**Gaus Width: 3.0921**



# B0L001S, U6-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

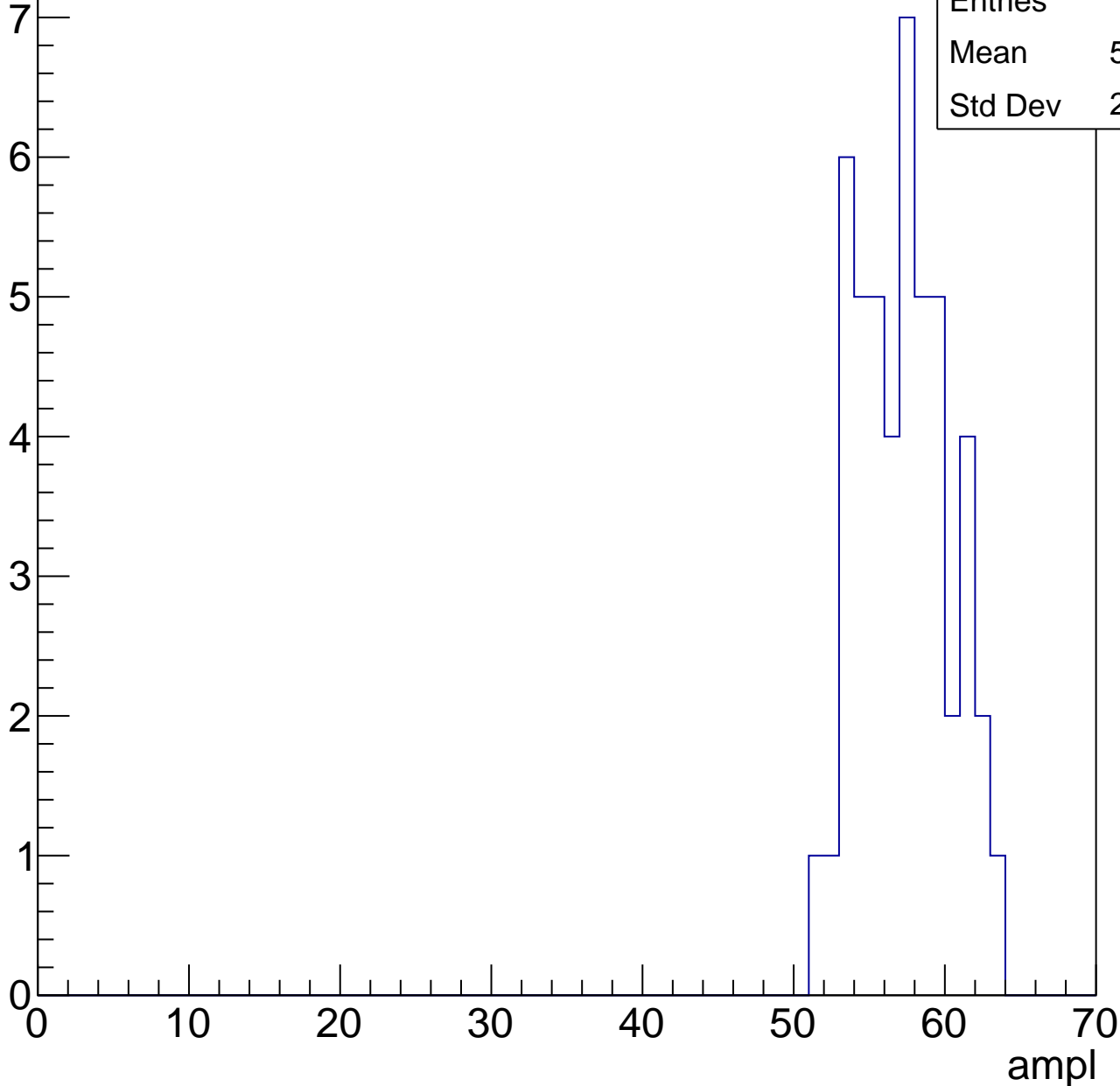


# B0L001S, U6-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	56.77
Std Dev	2.946



# B0L001S, U6-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

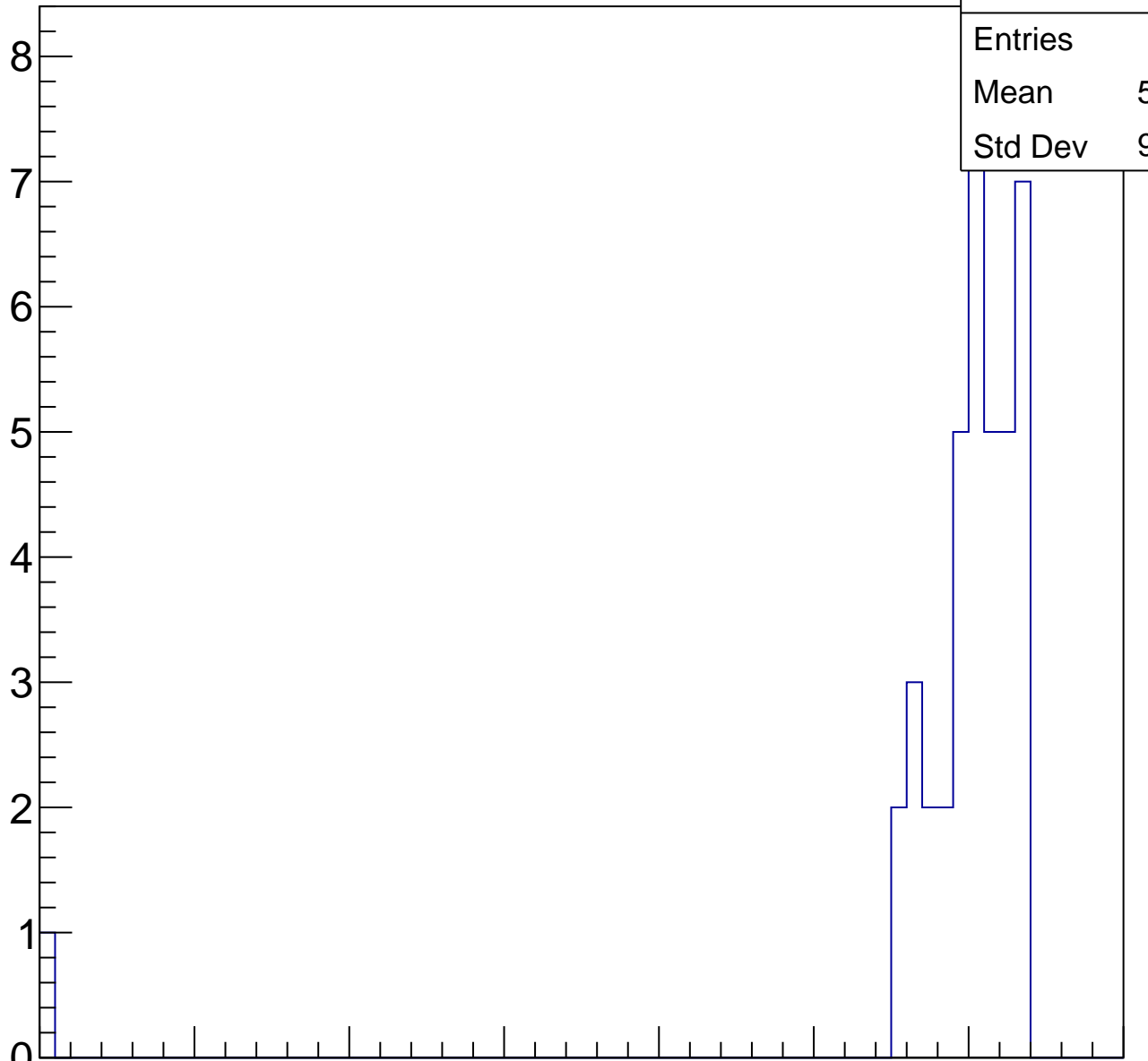
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	40
Mean	58.48
Std Dev	9.649

ampl

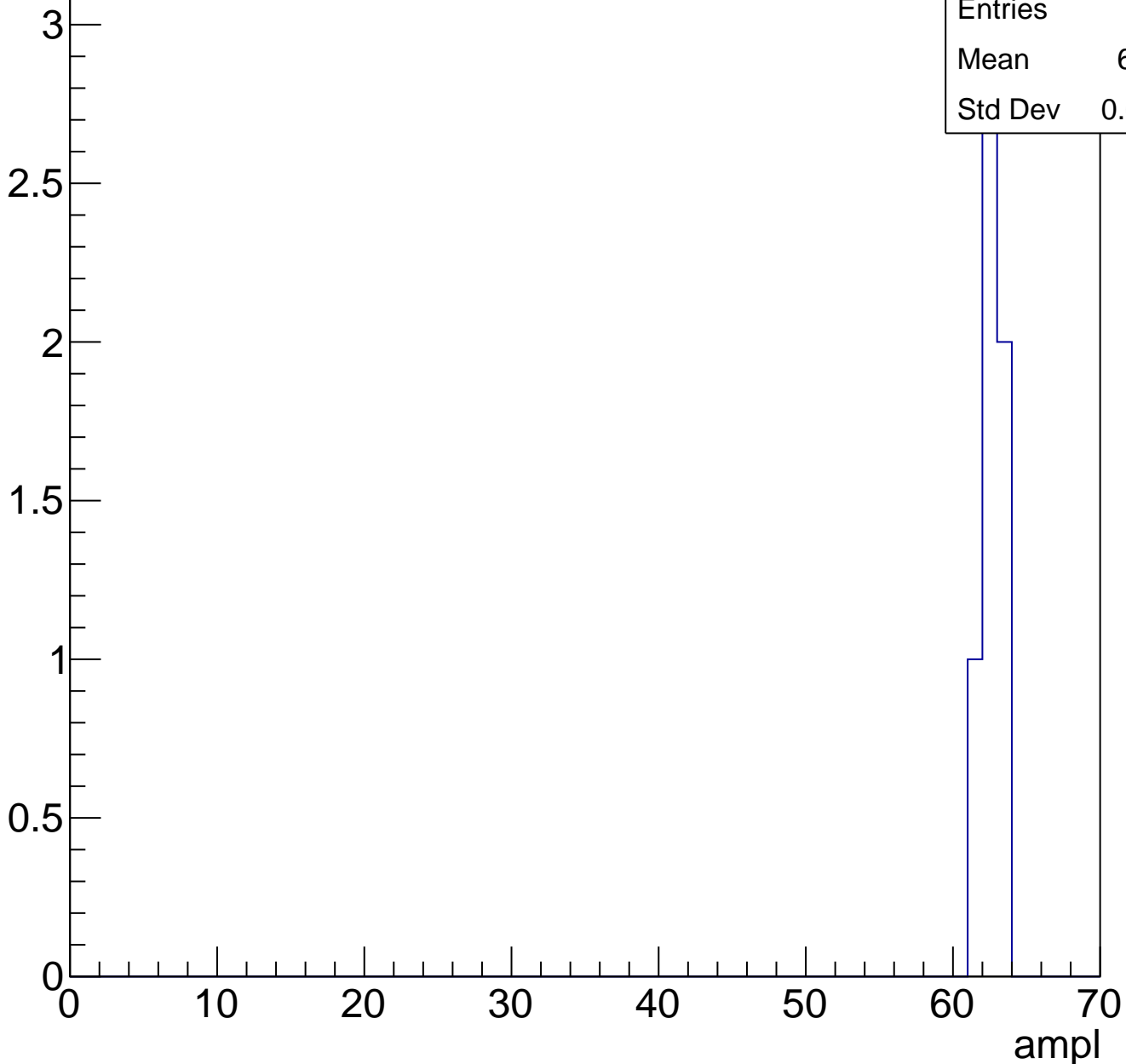
0 10 20 30 40 50 60 70



# B0L001S, U6-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

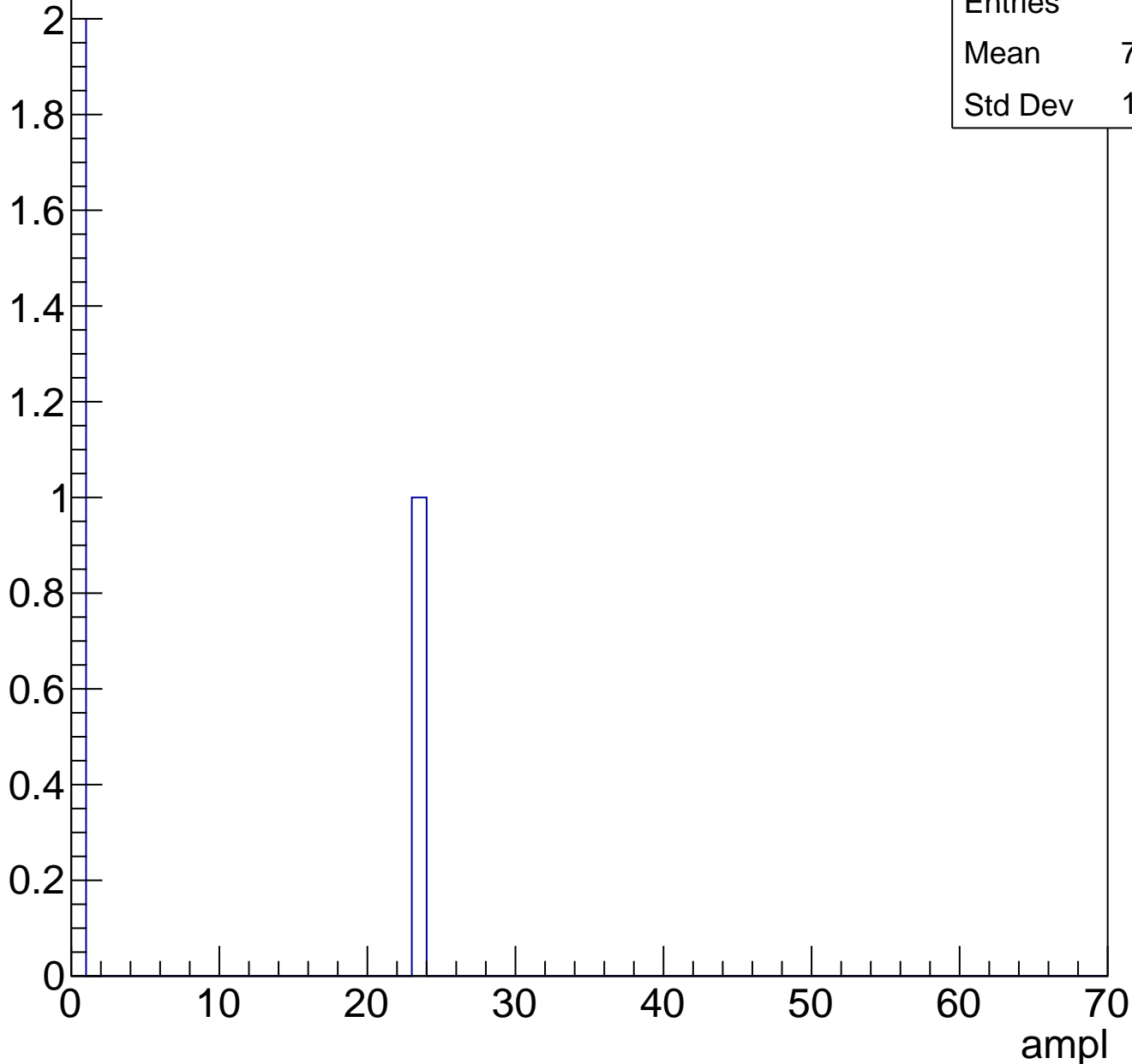




# B0L001S, U6-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	7.667
Std Dev	10.84

# B0L001S, U6-ch21, adc0

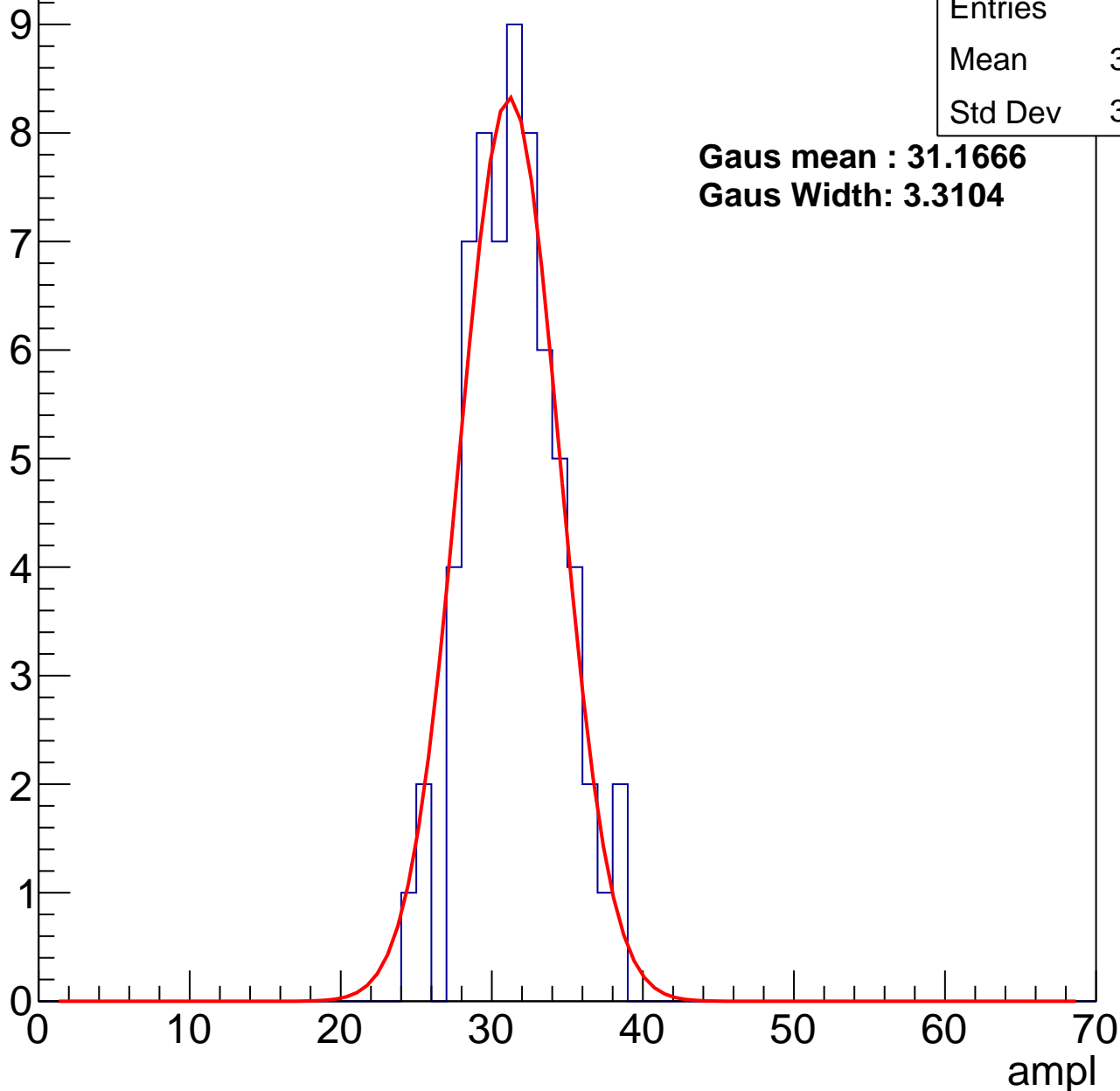
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	31.03
Std Dev	3.045

**Gaus mean : 31.1666**

**Gaus Width: 3.3104**



# B0L001S, U6-ch21, adc1

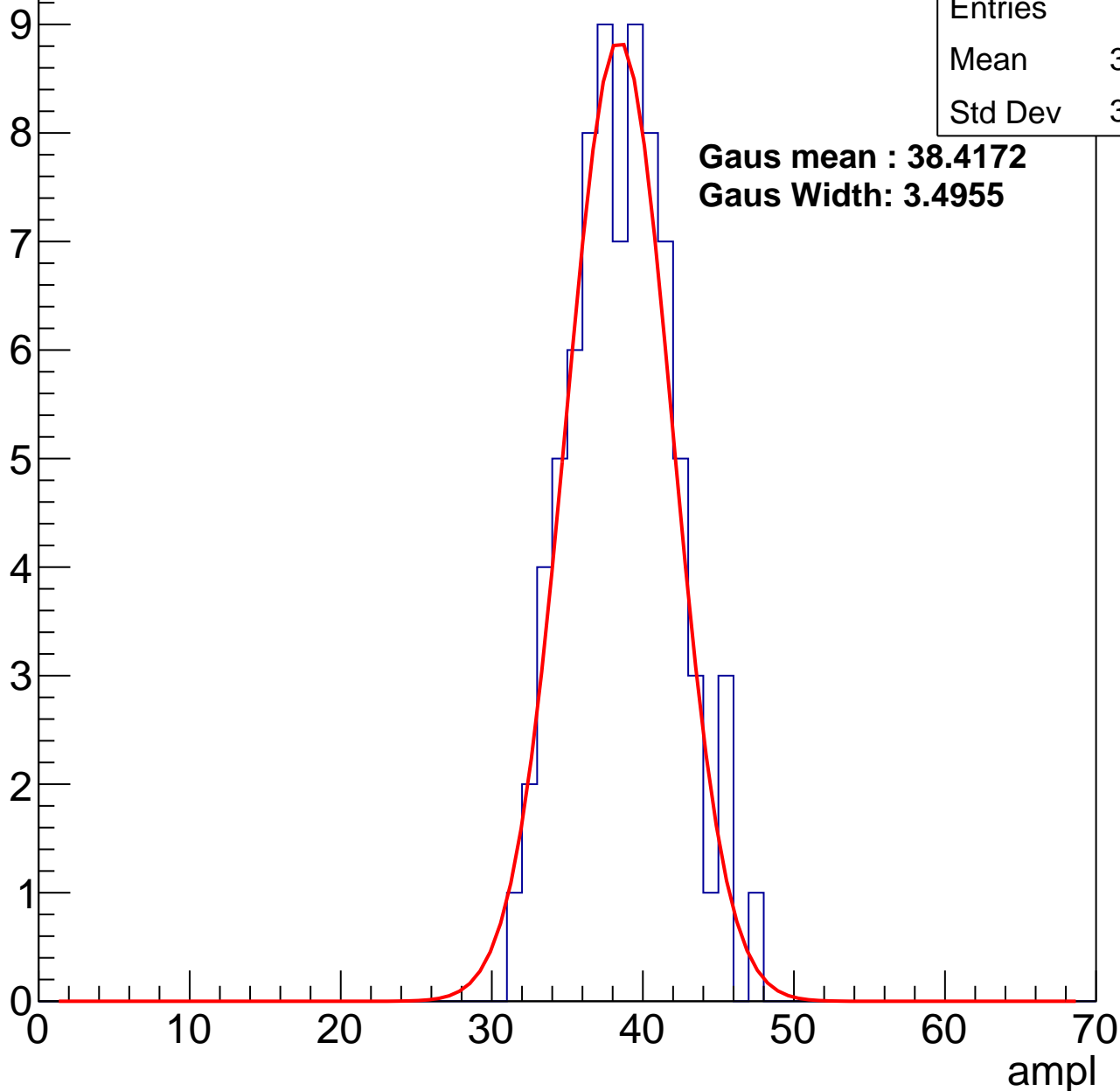
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	38.19
Std Dev	3.405

**Gaus mean : 38.4172**

**Gaus Width: 3.4955**



# B0L001S, U6-ch21, adc2

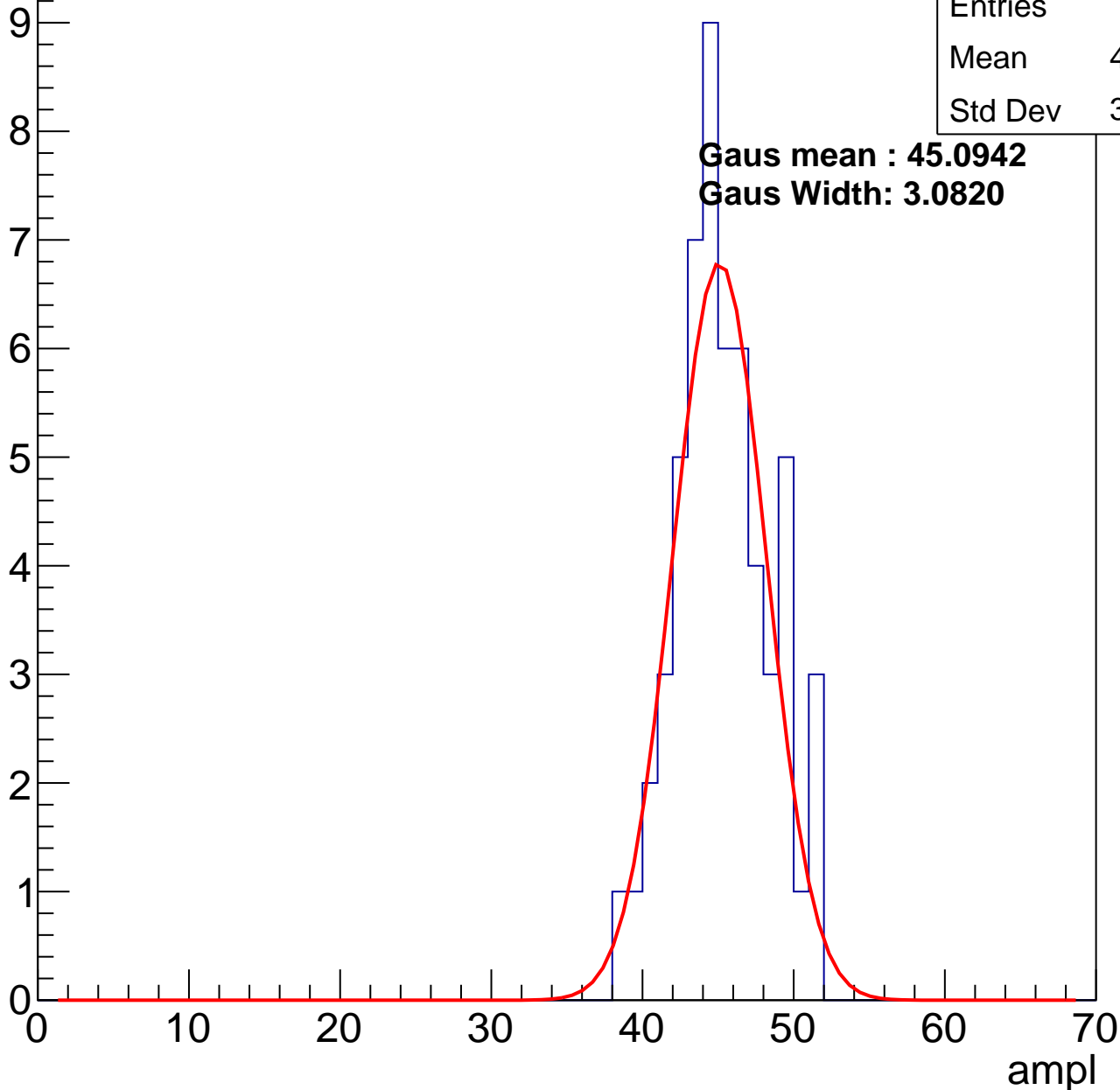
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	44.88
Std Dev	3.065

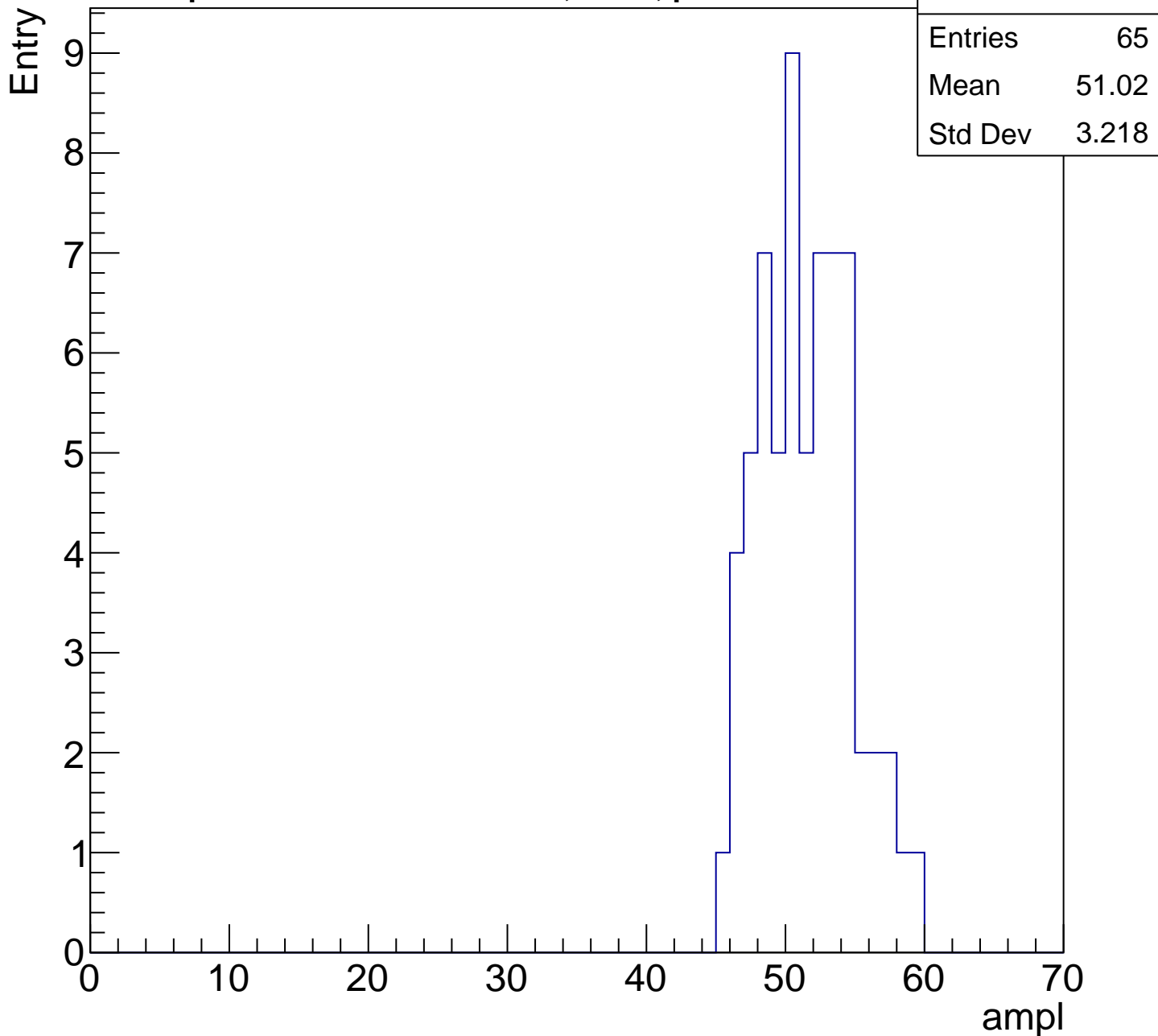
**Gaus mean : 45.0942**

**Gaus Width: 3.0820**



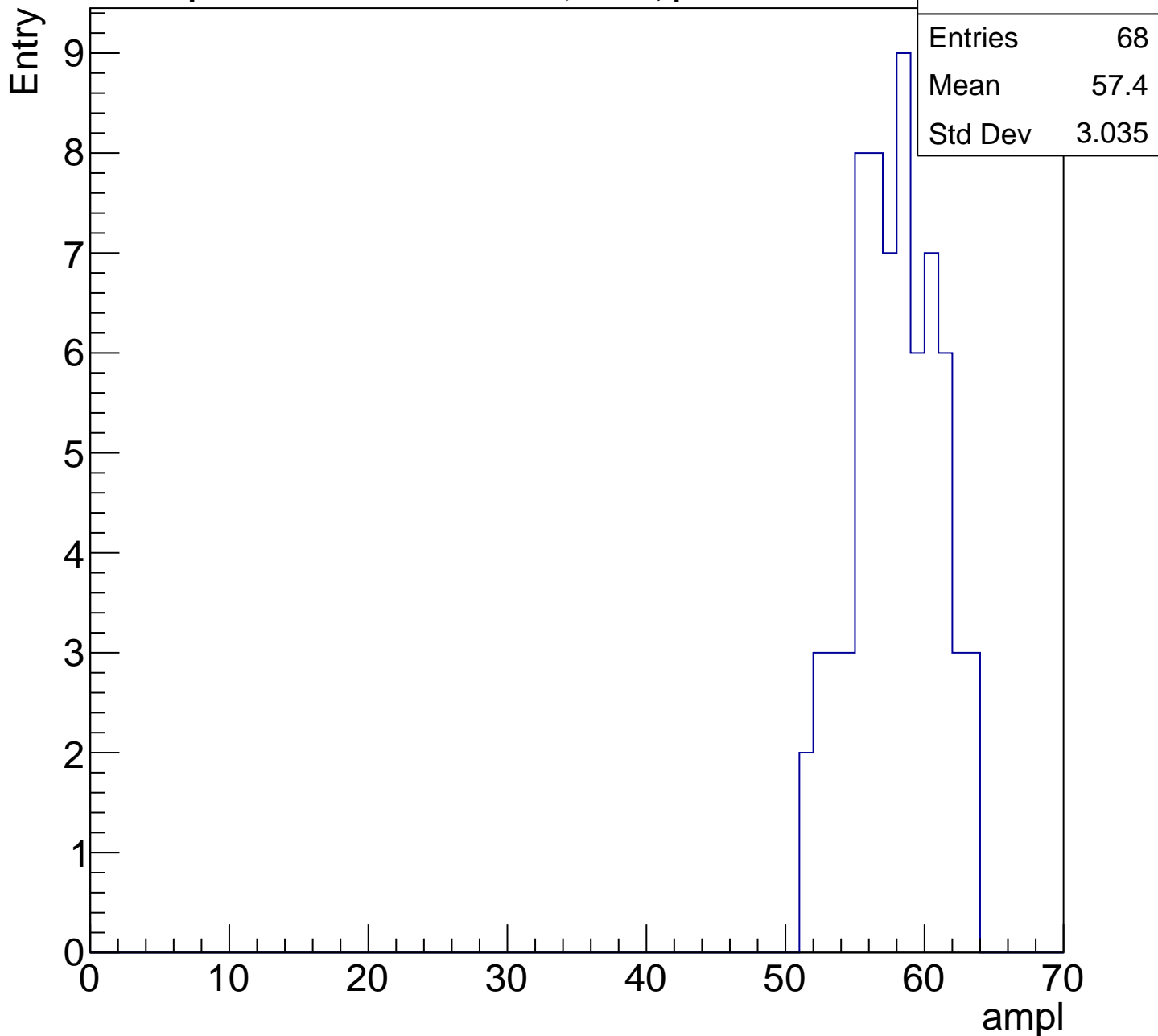
# B0L001S, U6-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U6-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

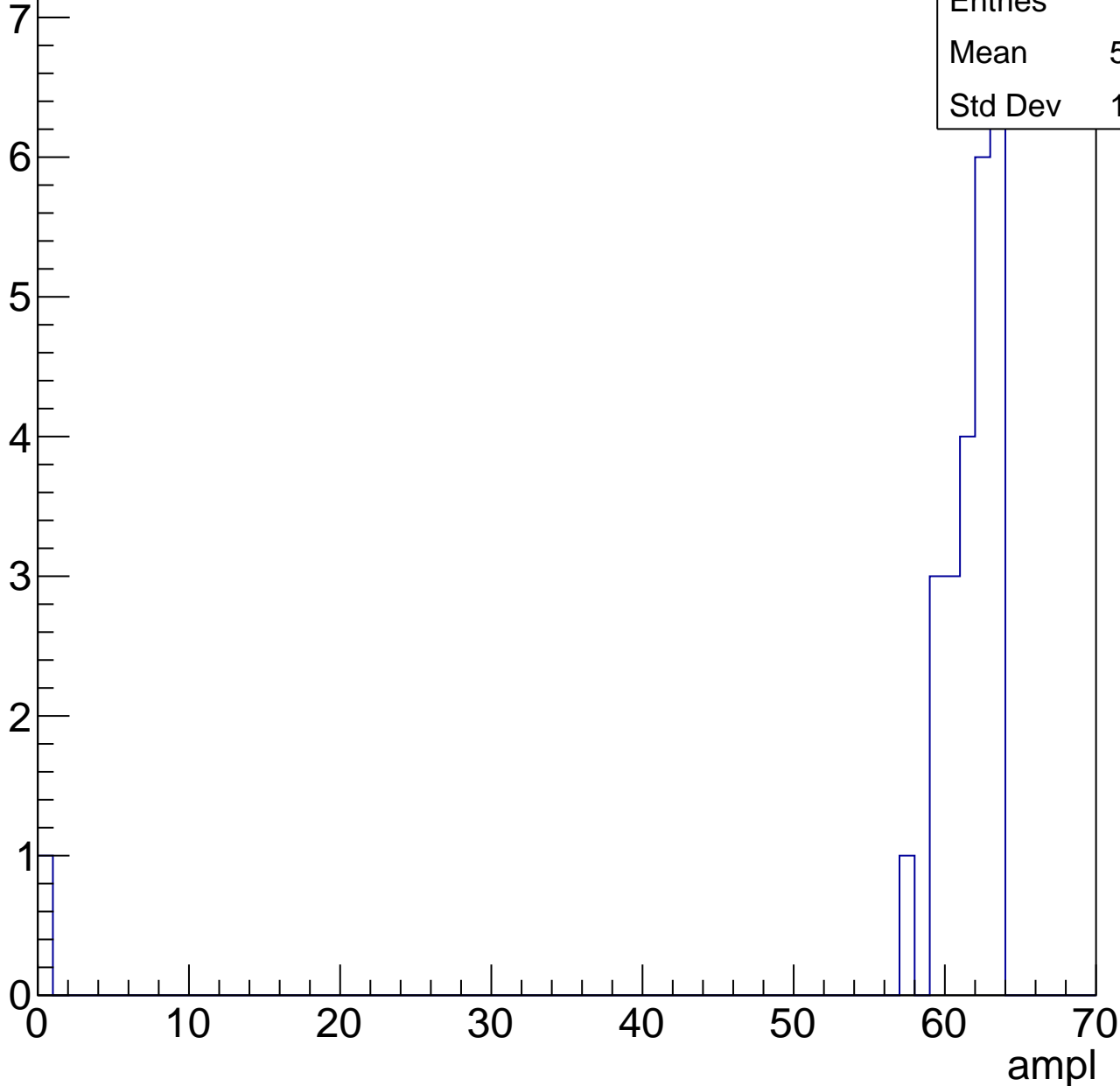


# B0L001S, U6-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

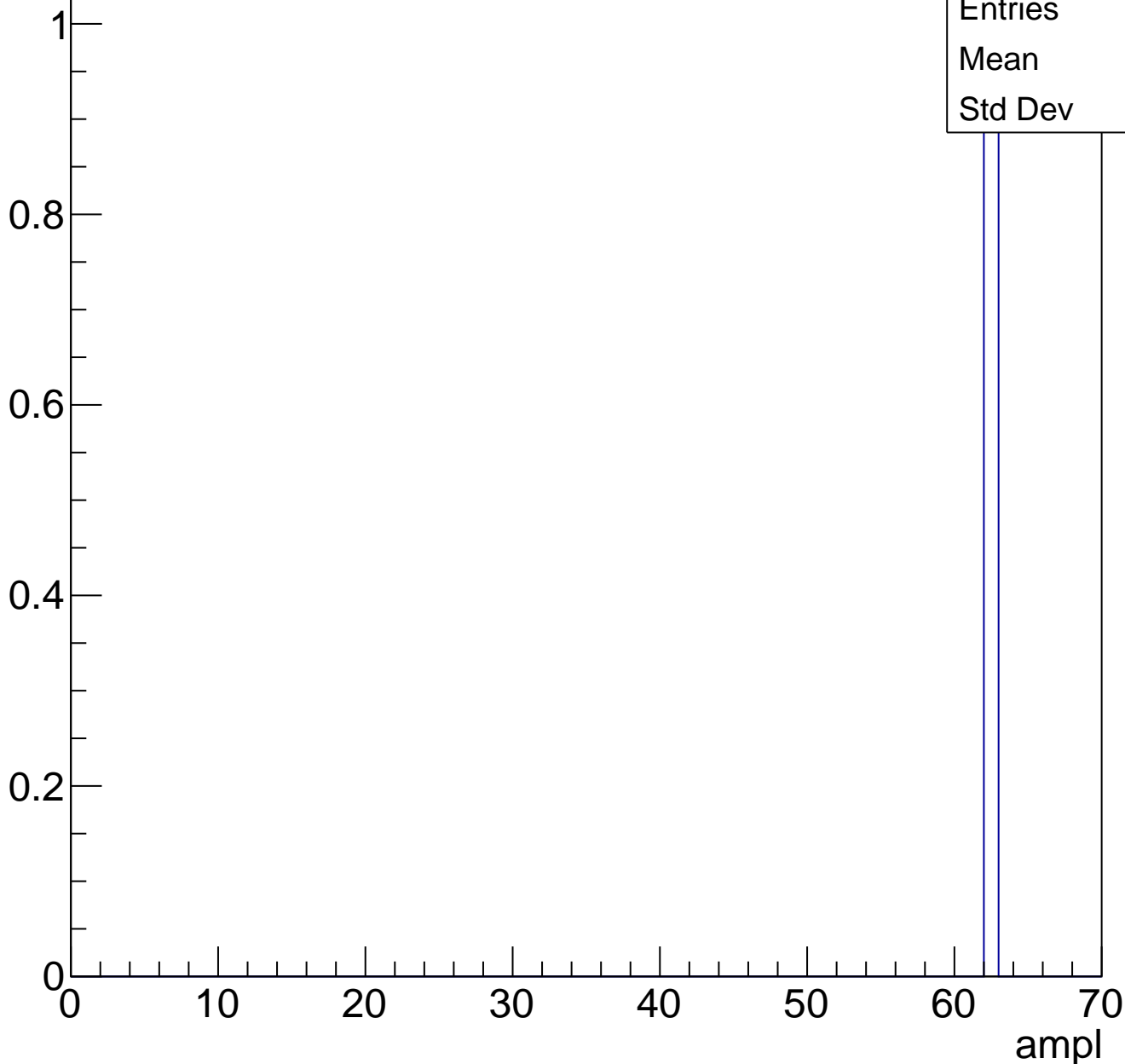
Entries	25
Mean	58.84
Std Dev	12.12



# B0L001S, U6-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U6-ch22, adc0

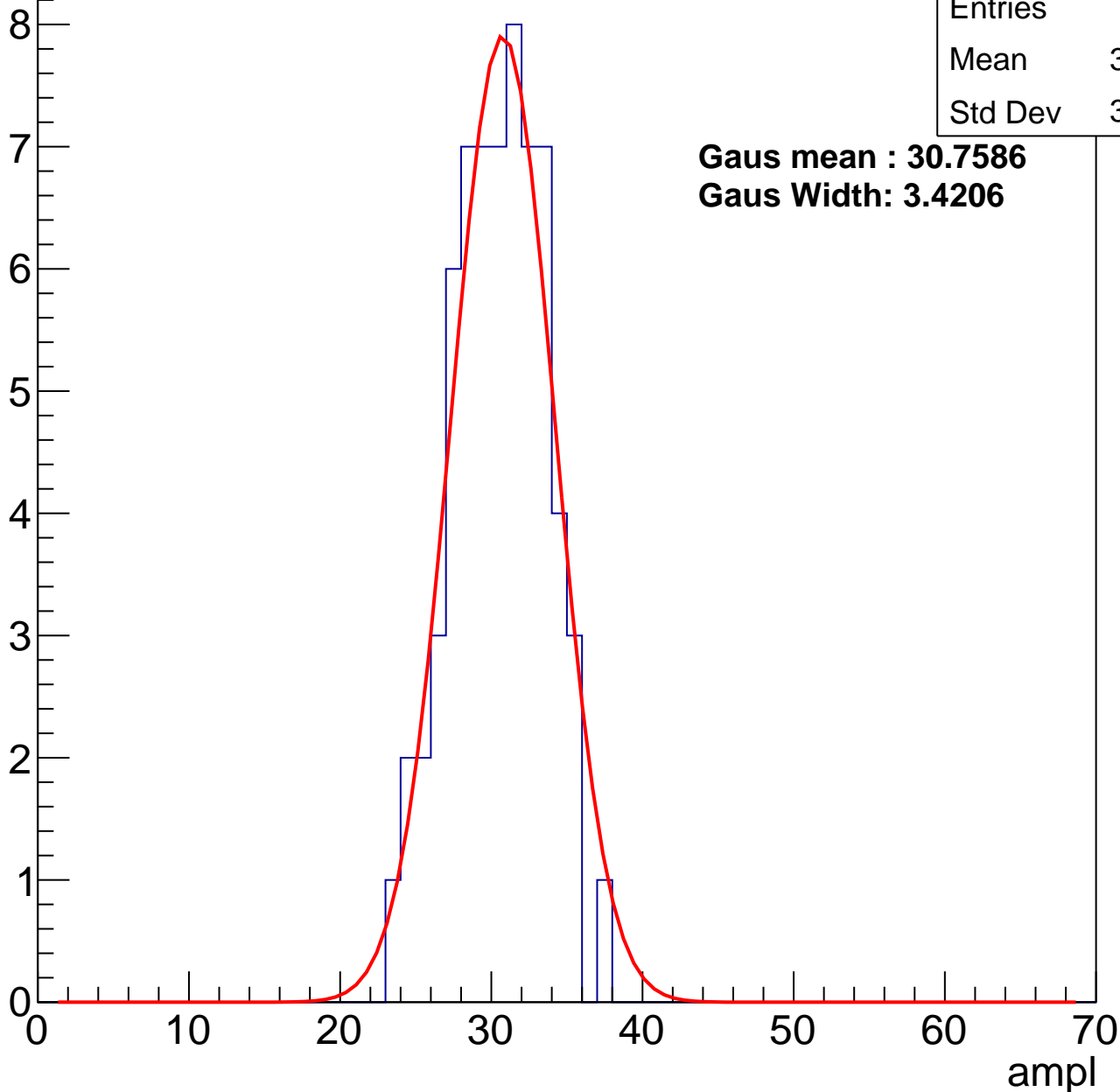
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	30.02
Std Dev	3.025

**Gaus mean : 30.7586**

**Gaus Width: 3.4206**



# B0L001S, U6-ch22, adc1

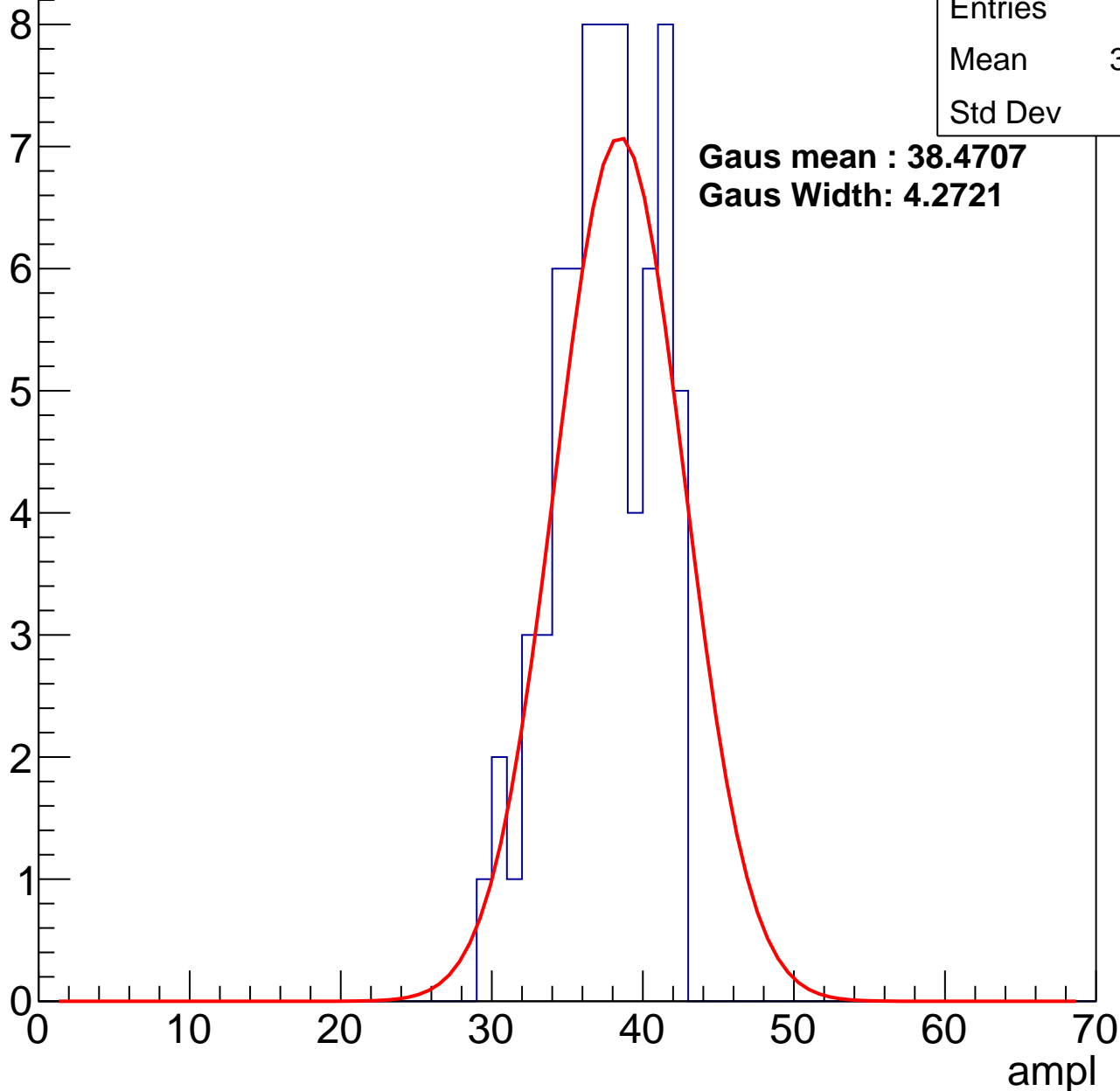
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	36.97
Std Dev	3.27

**Gaus mean : 38.4707**

**Gaus Width: 4.2721**



# B0L001S, U6-ch22, adc2

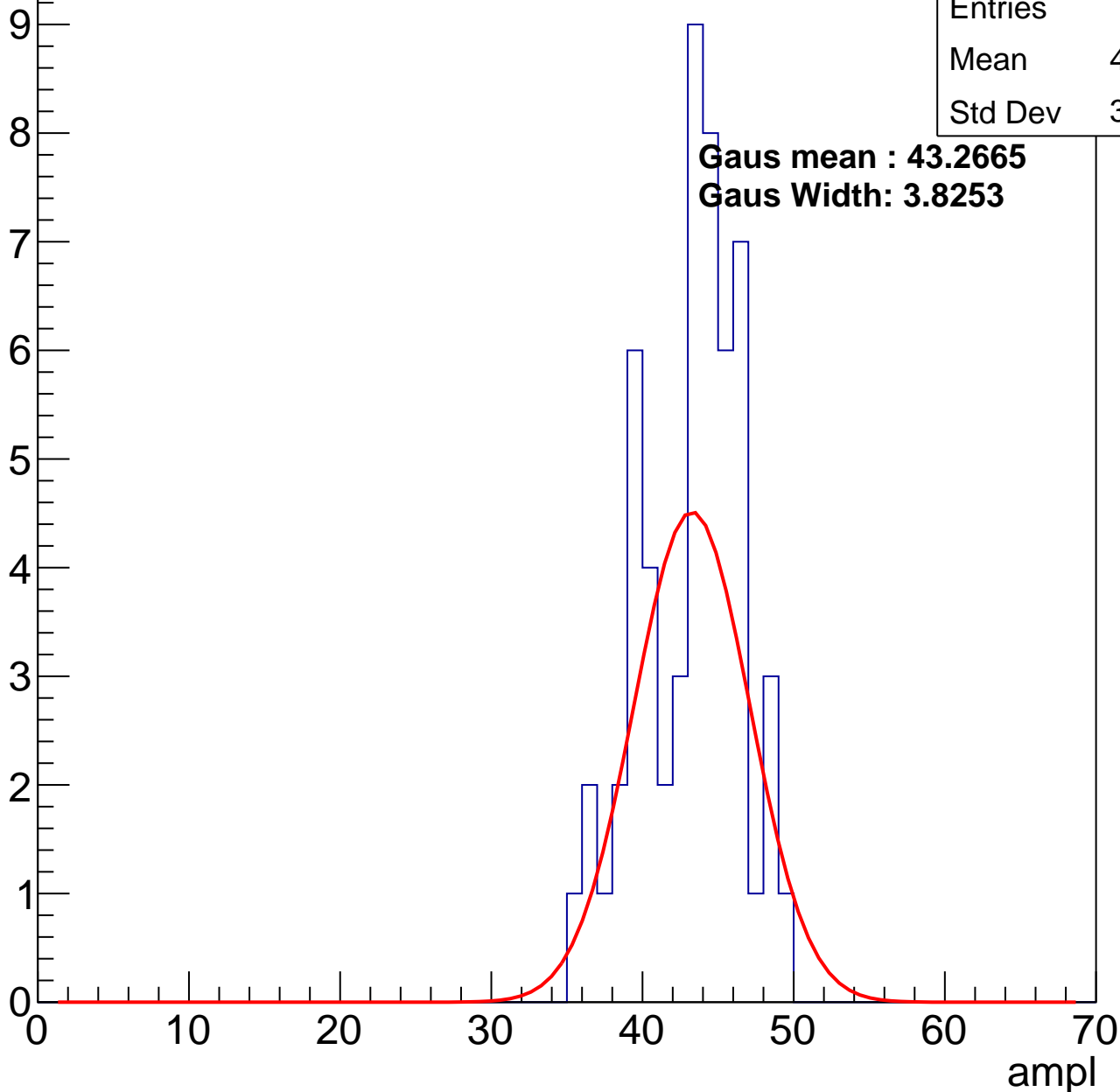
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	42.73
Std Dev	3.298

**Gaus mean : 43.2665**

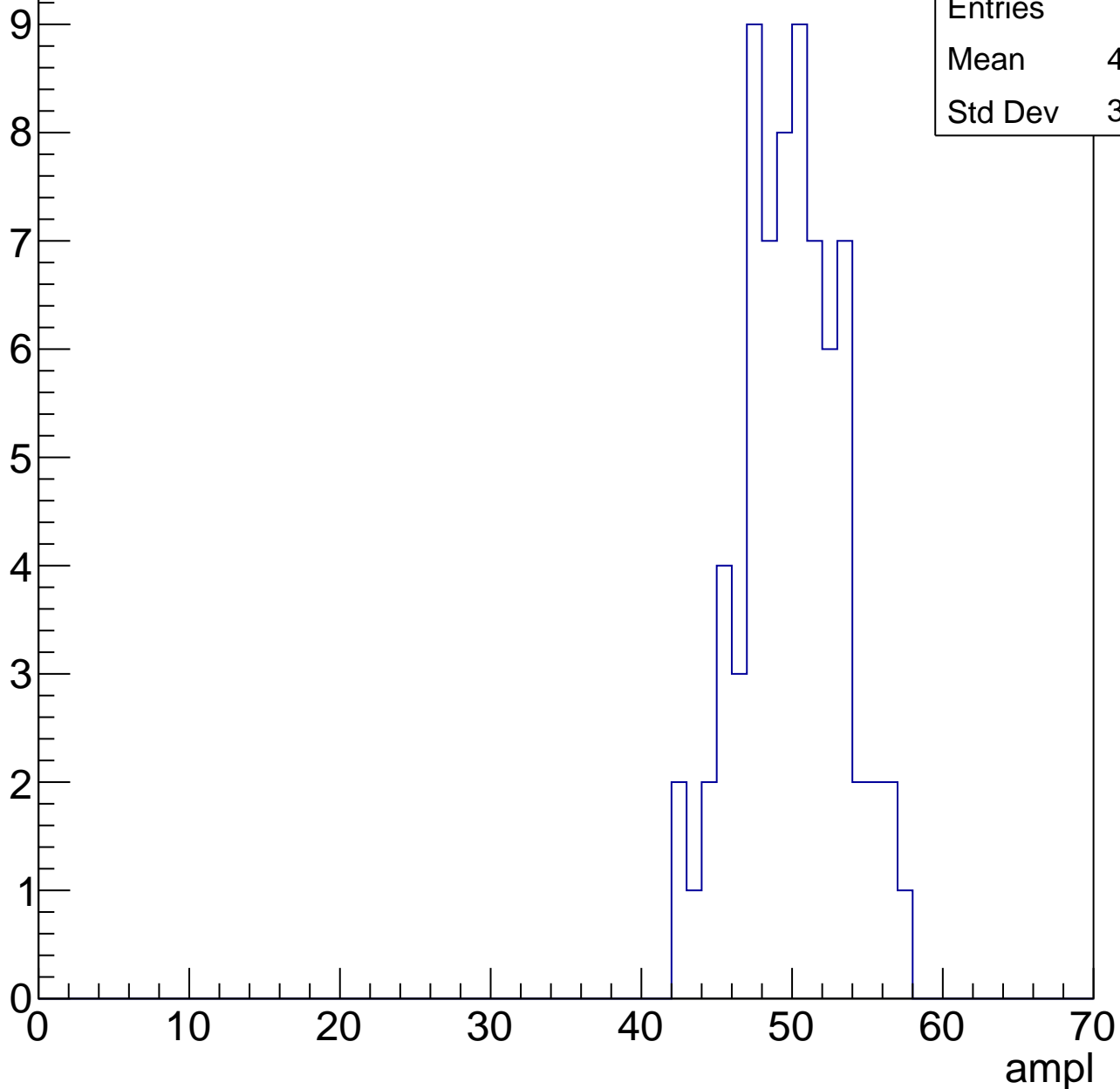
**Gaus Width: 3.8253**



# B0L001S, U6-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



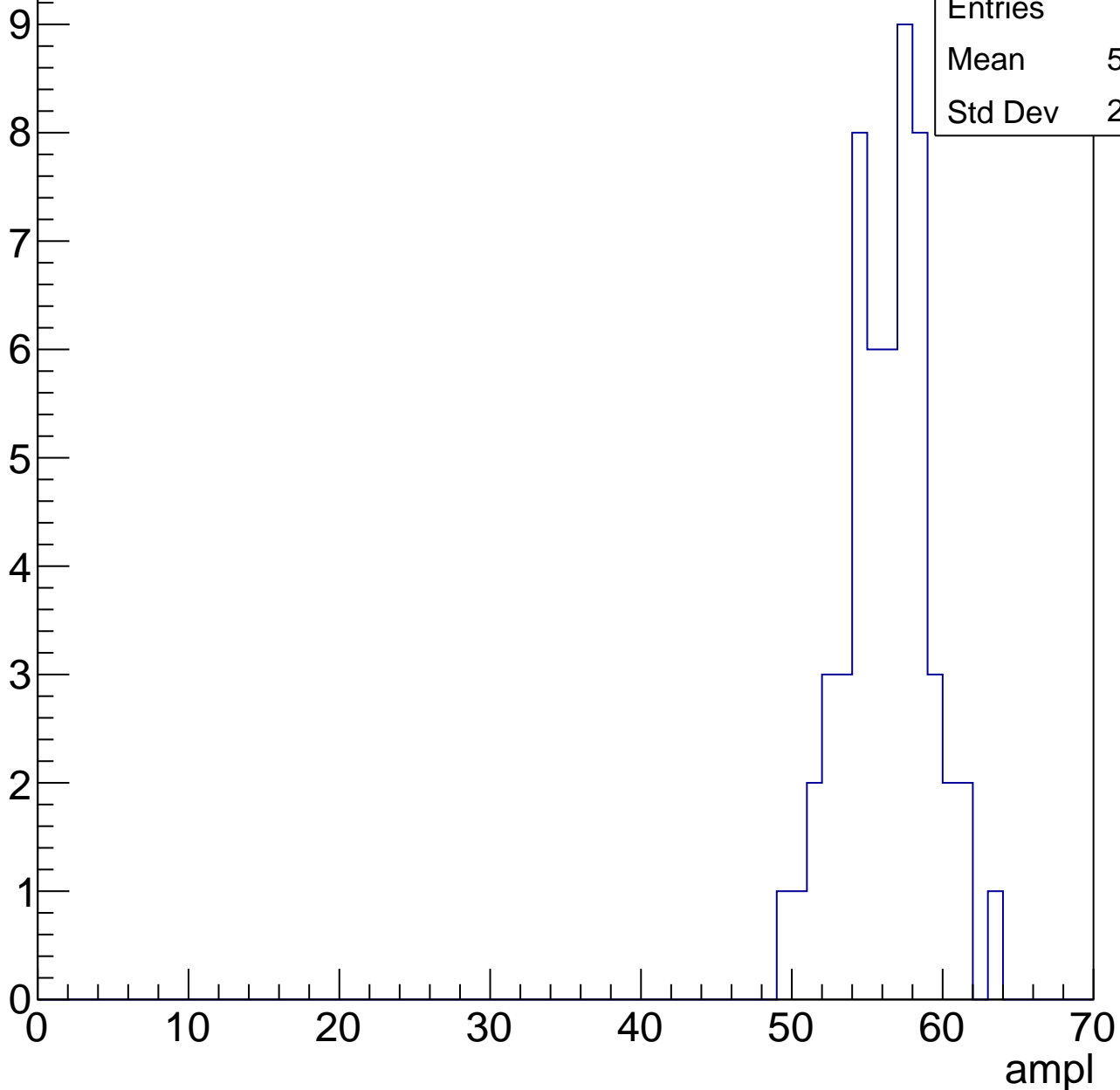
Entries	72
Mean	49.46
Std Dev	3.312

# B0L001S, U6-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	55.87
Std Dev	2.848

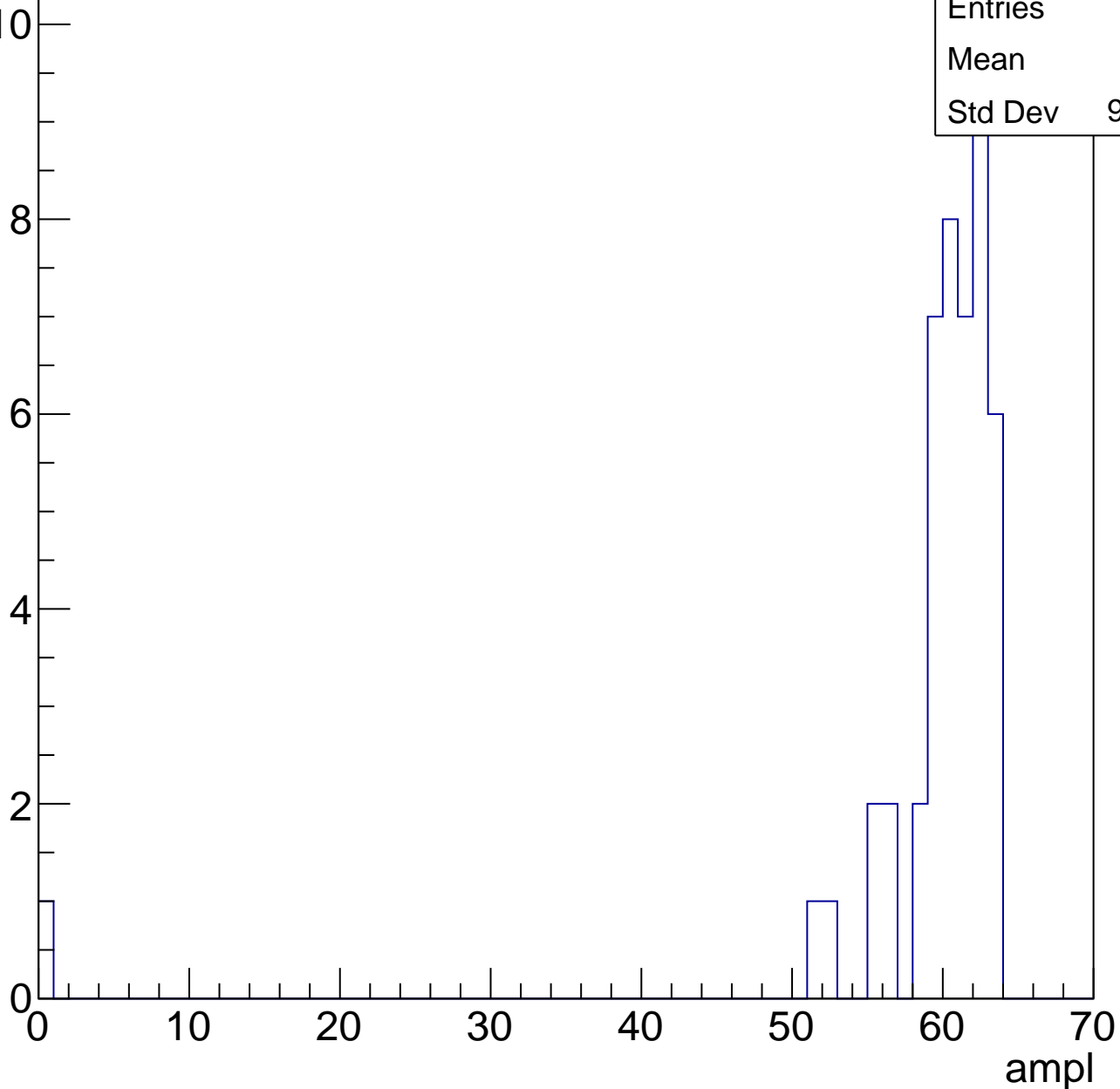


# B0L001S, U6-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	58.7
Std Dev	9.067



# B0L001S, U6-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch23, adc0

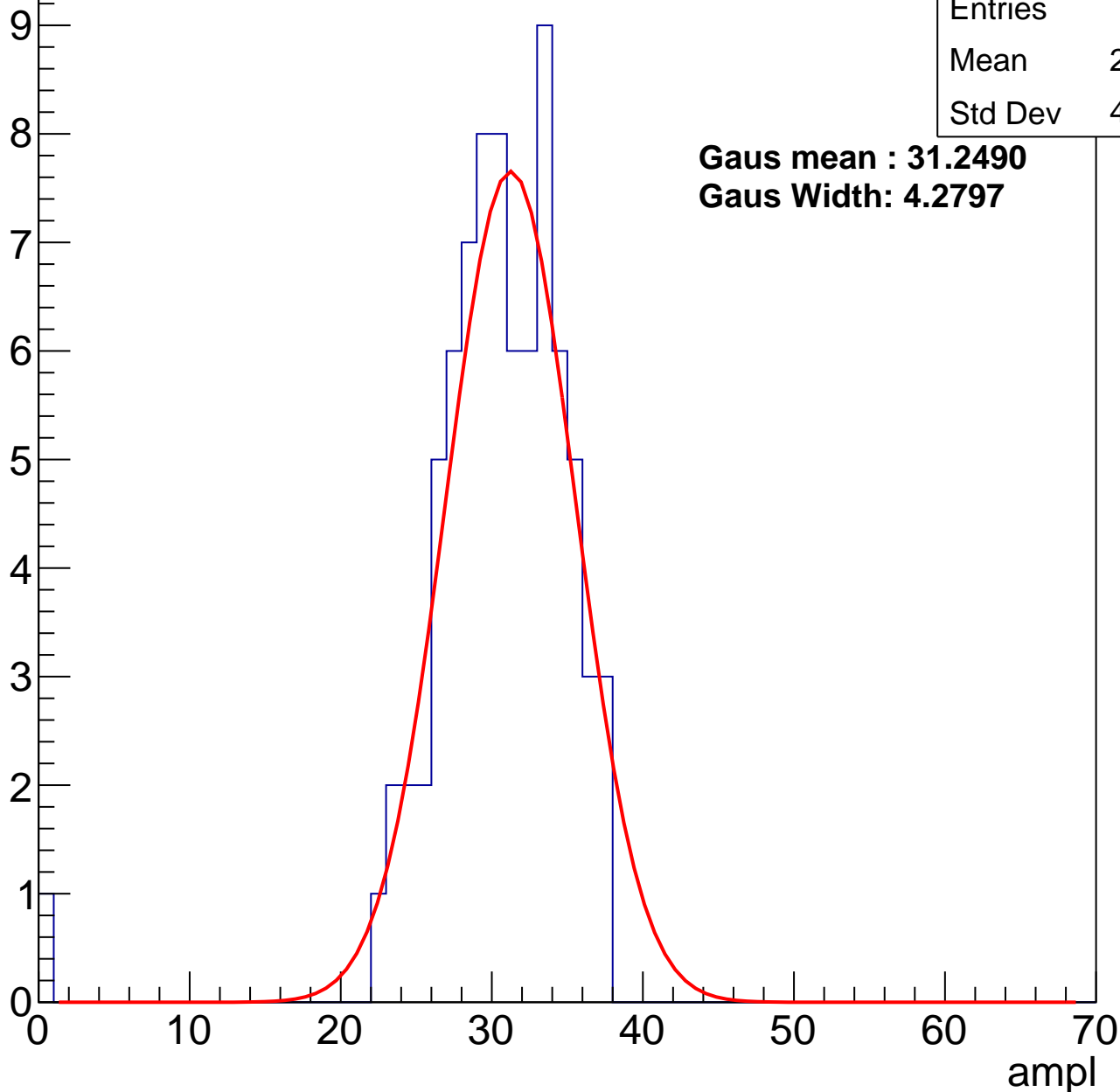
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	80
Mean	29.99
Std Dev	4.926

**Gaus mean : 31.2490**

**Gaus Width: 4.2797**



# B0L001S, U6-ch23, adc1

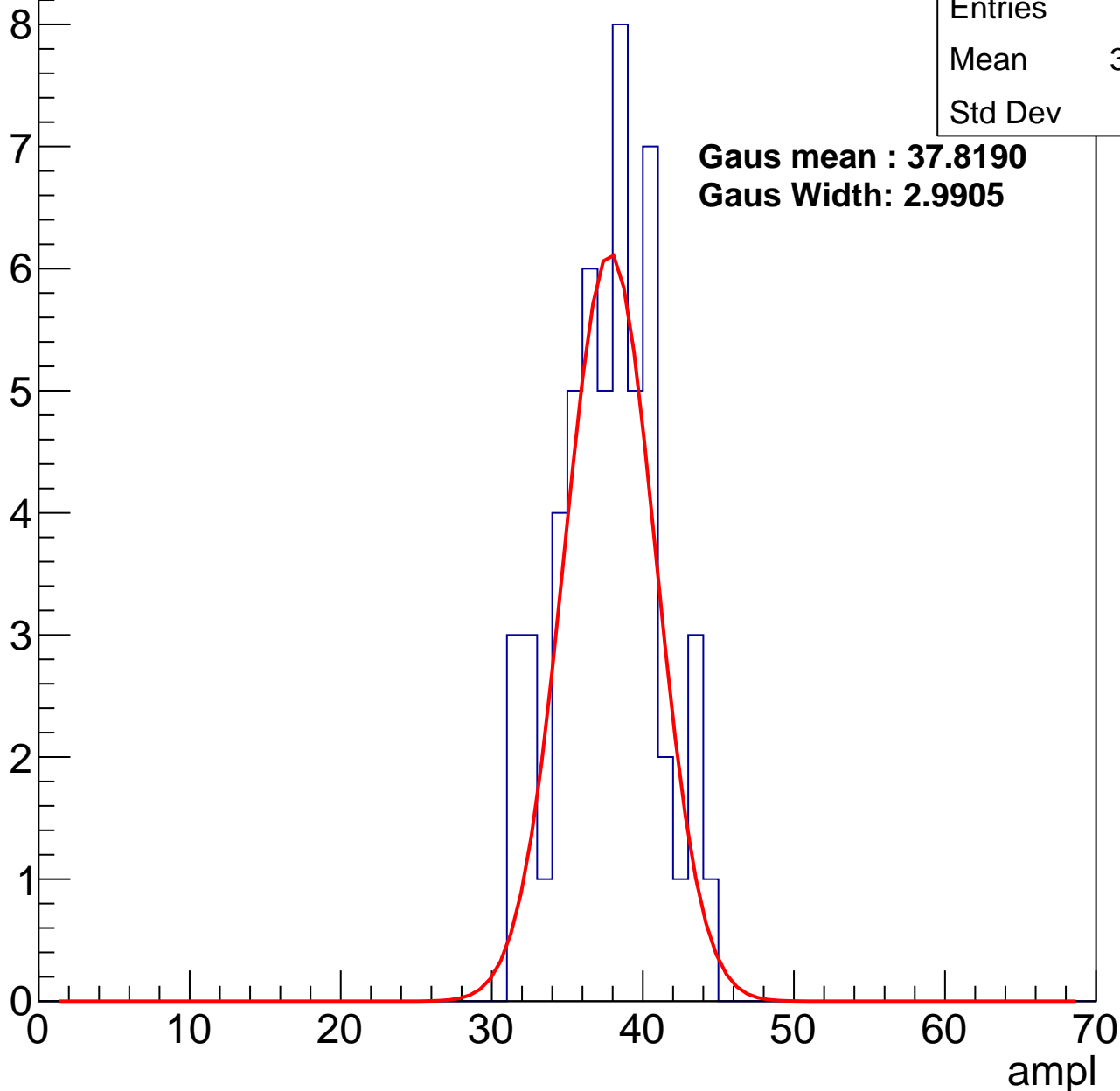
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	37.22
Std Dev	3.23

**Gaus mean : 37.8190**

**Gaus Width: 2.9905**



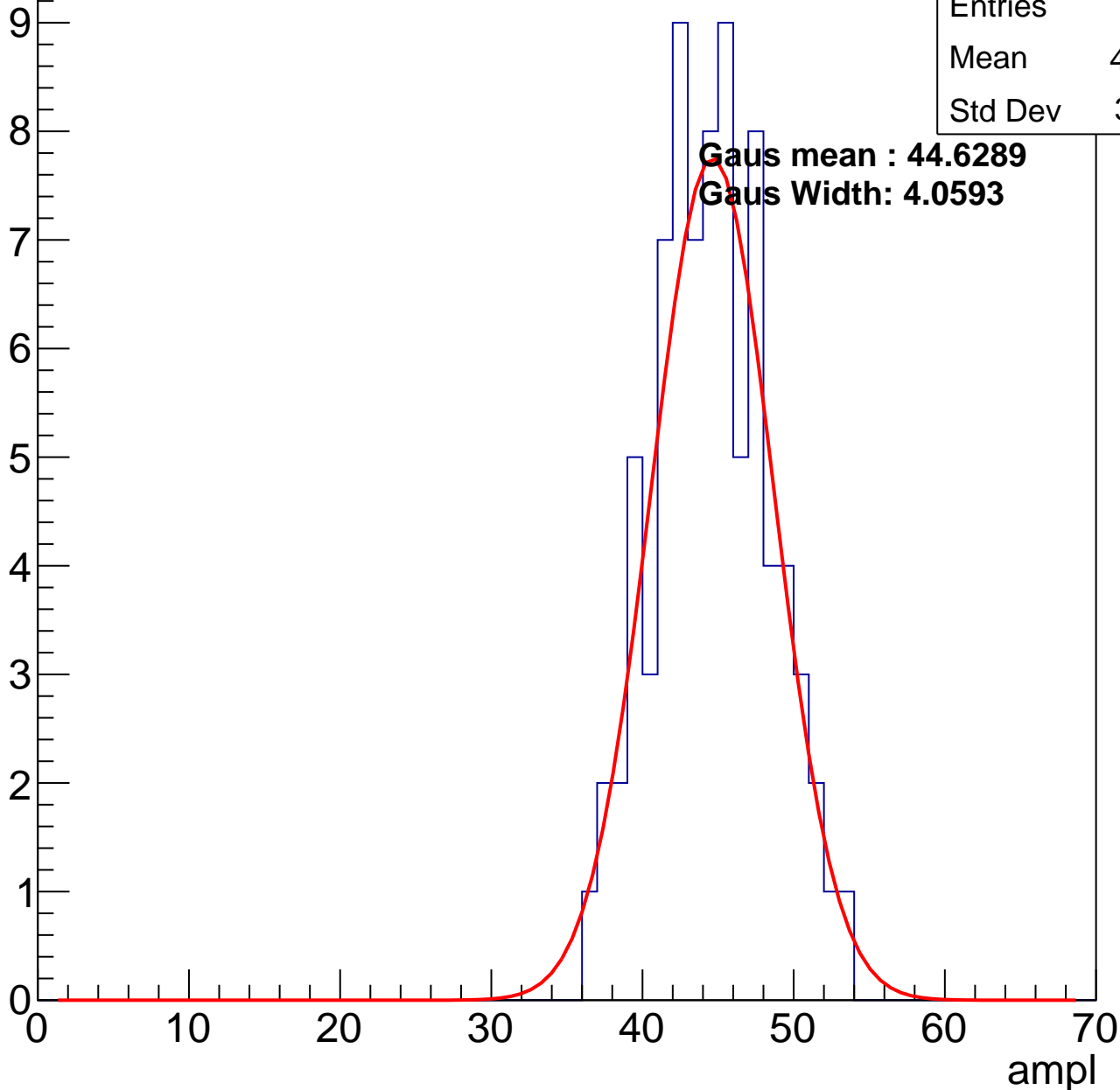
# B0L001S, U6-ch23, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	44.14
Std Dev	3.731

**Gaus mean : 44.6289**  
**Gaus Width: 4.0593**

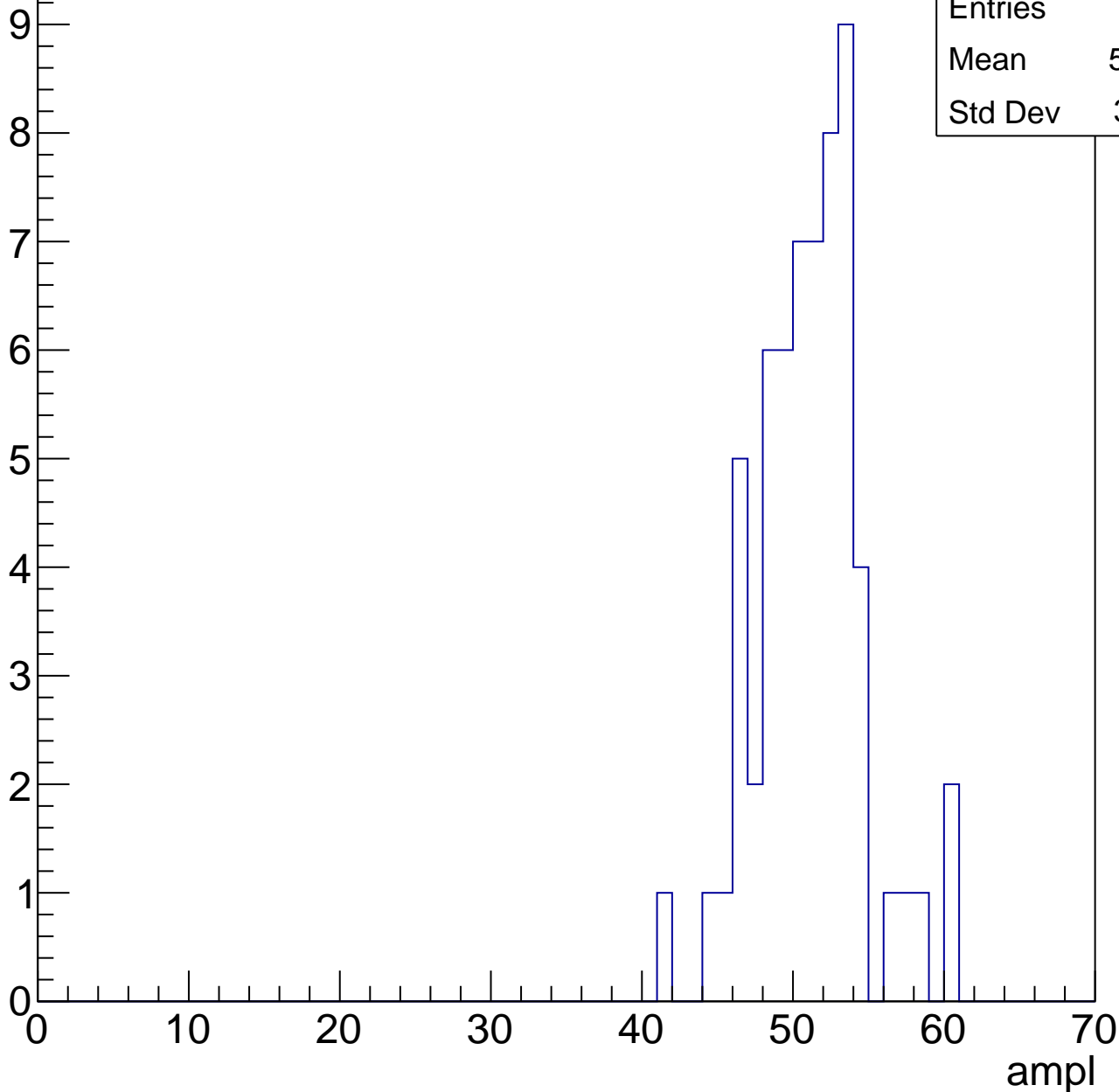


# B0L001S, U6-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	50.69
Std Dev	3.531



# B0L001S, U6-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	58
Mean	57.22
Std Dev	2.607

Entry

10  
8  
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4  
2  
0

0 10 20 30 40 50 60 70

ampl

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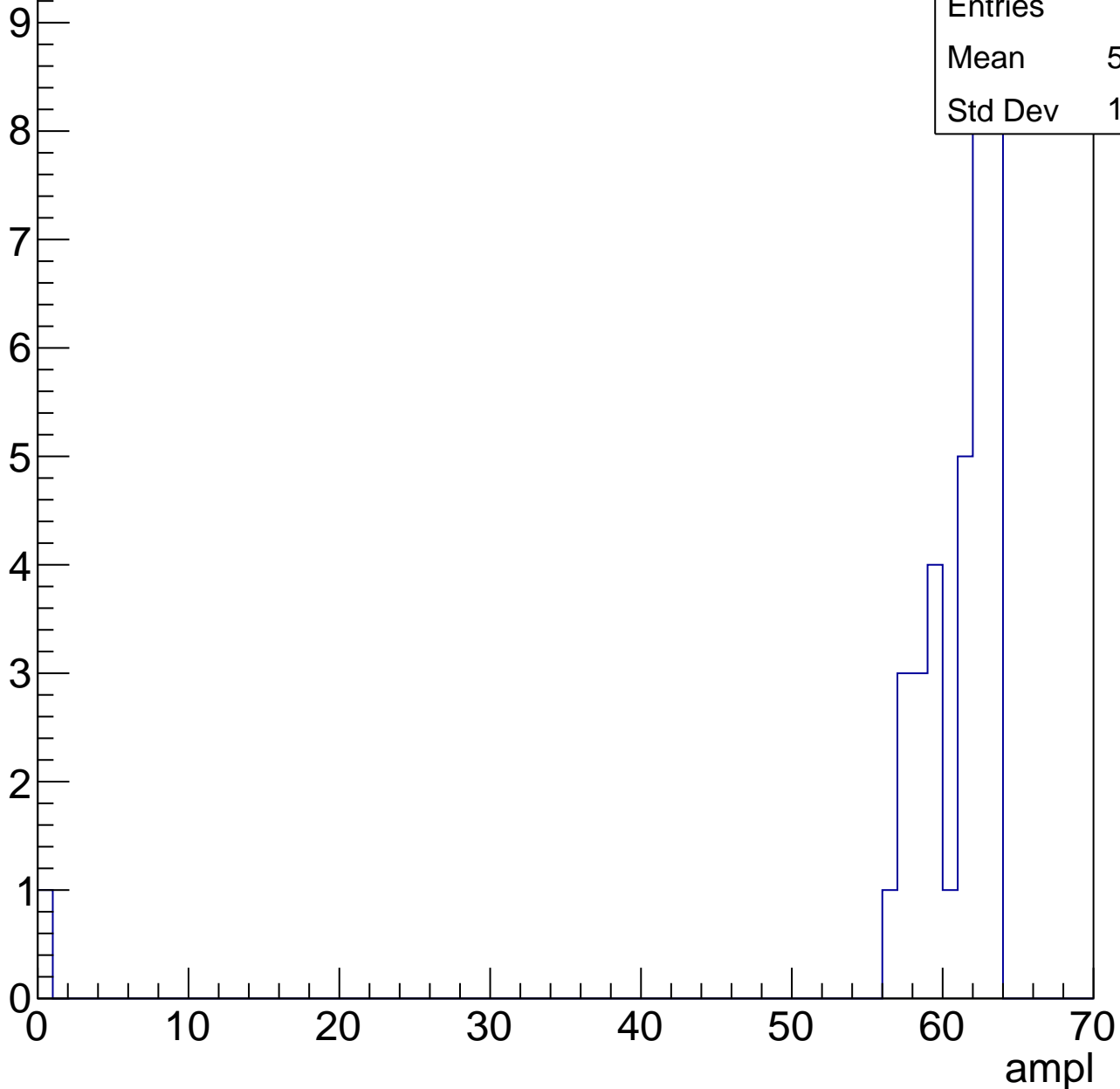
319

# B0L001S, U6-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

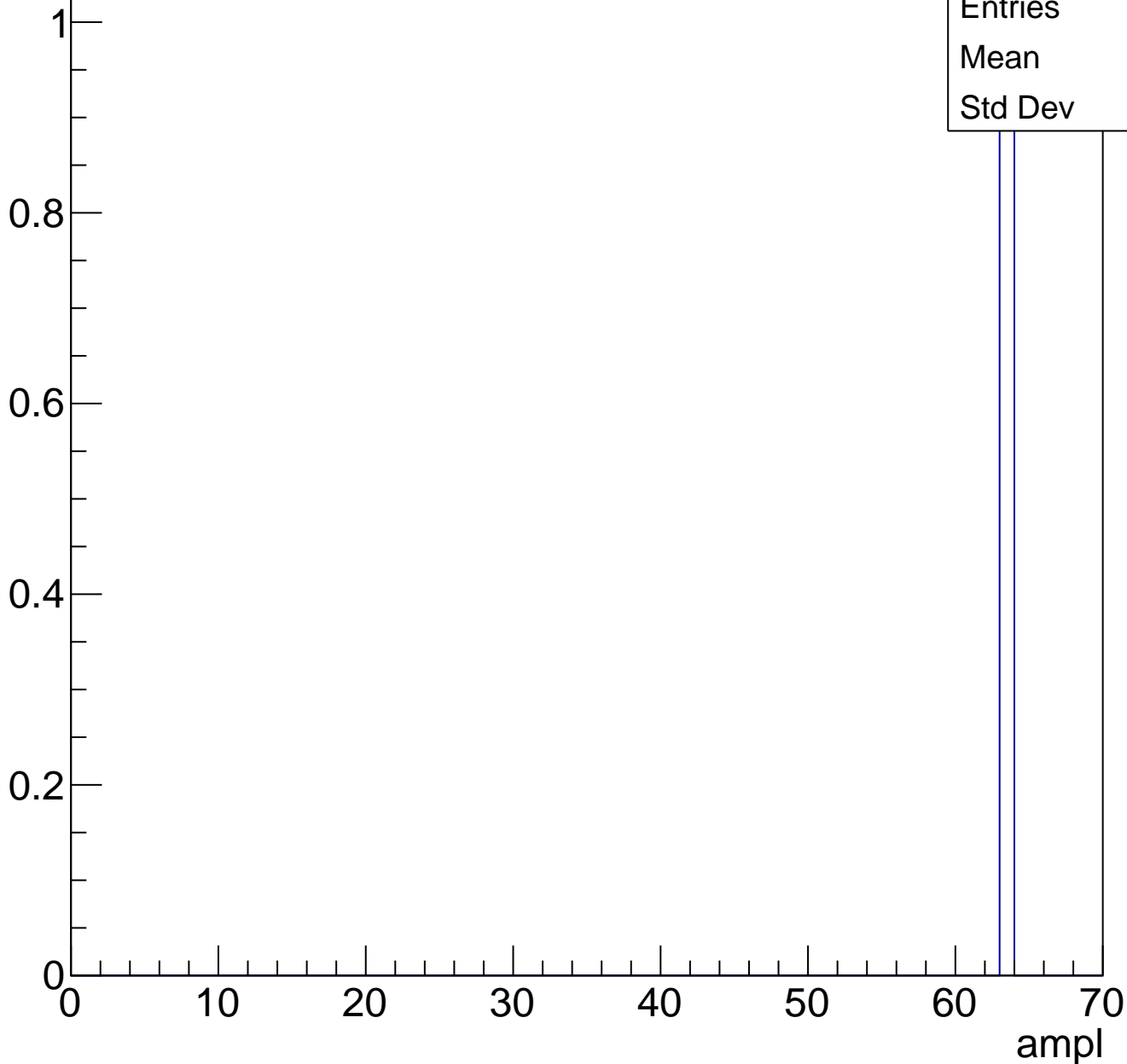
Entries	35
Mean	58.97
Std Dev	10.33



# B0L001S, U6-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U6-ch24, adc0

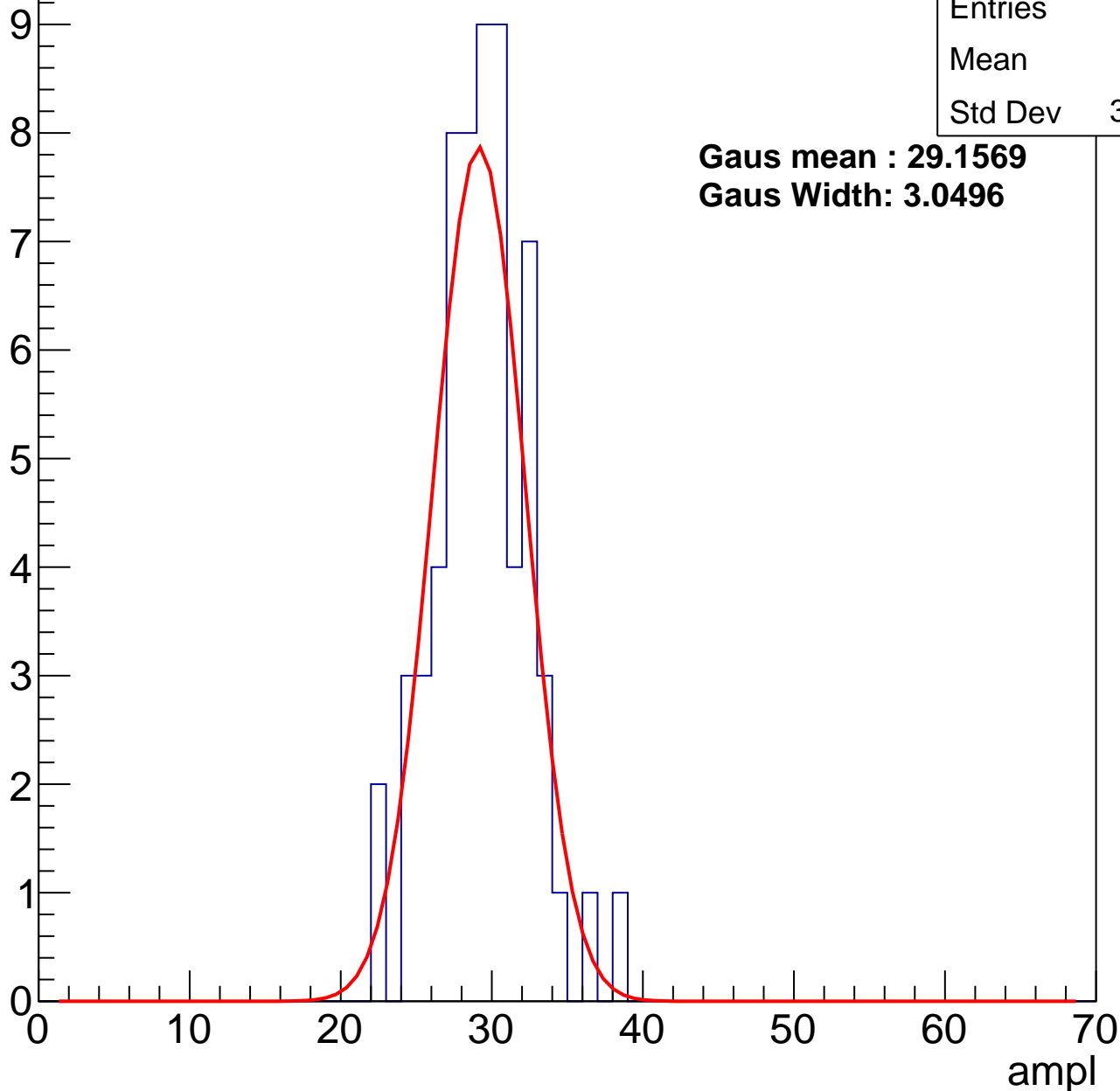
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	28.9
Std Dev	3.054

**Gaus mean : 29.1569**

**Gaus Width: 3.0496**



# B0L001S, U6-ch24, adc1

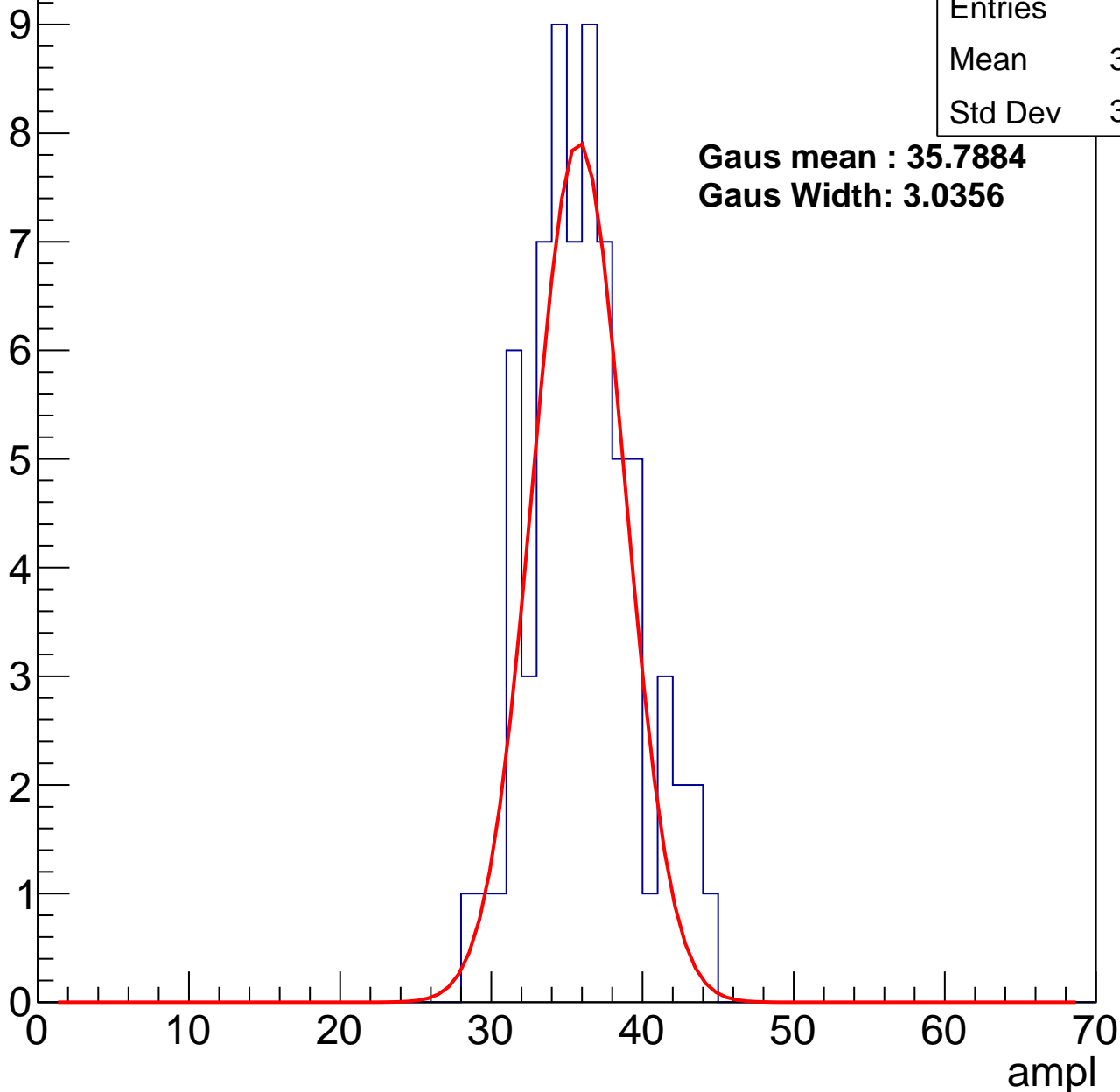
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	35.66
Std Dev	3.468

**Gaus mean : 35.7884**

**Gaus Width: 3.0356**



# B0L001S, U6-ch24, adc2

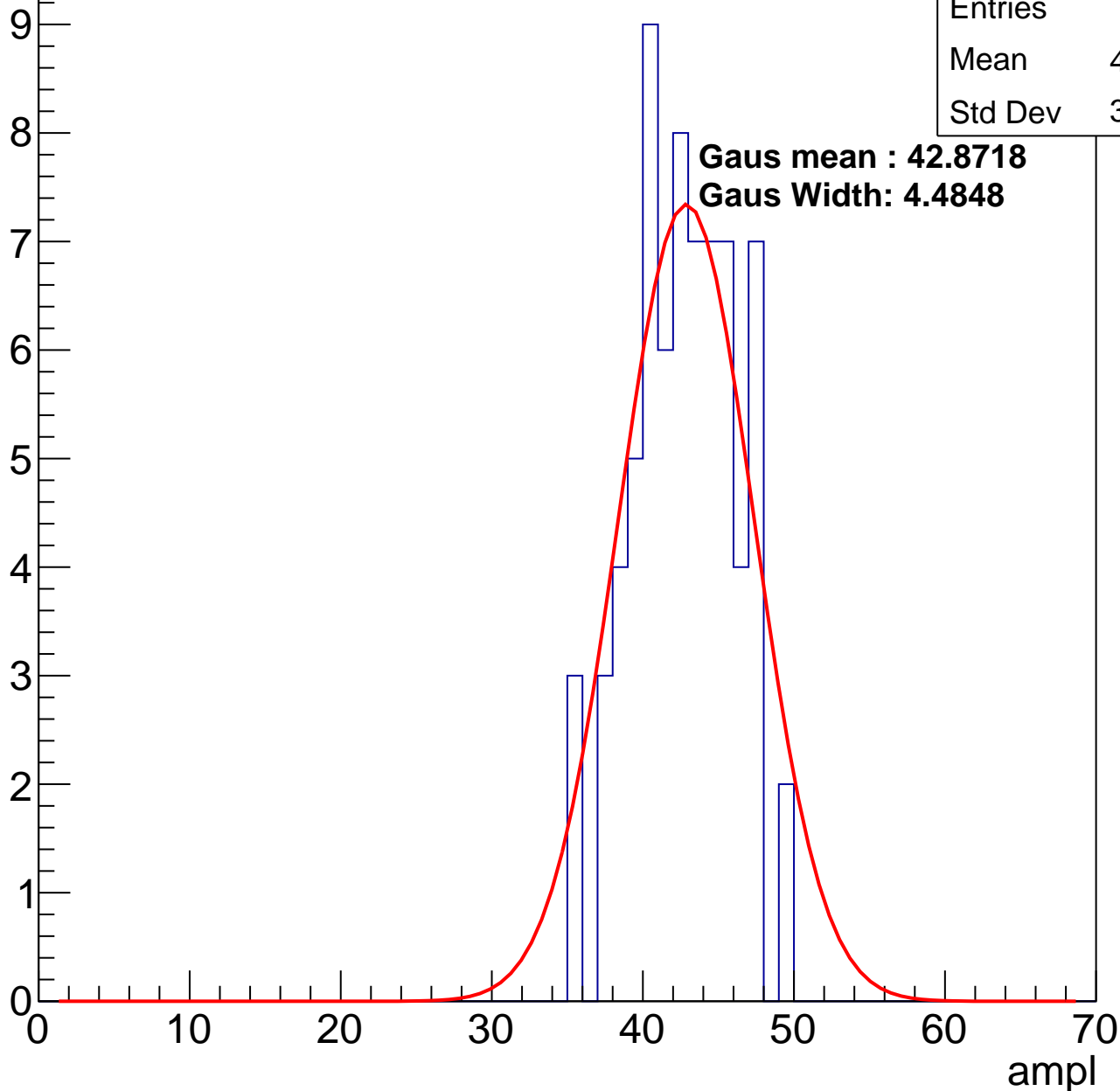
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	42.22
Std Dev	3.343

**Gaus mean : 42.8718**

**Gaus Width: 4.4848**

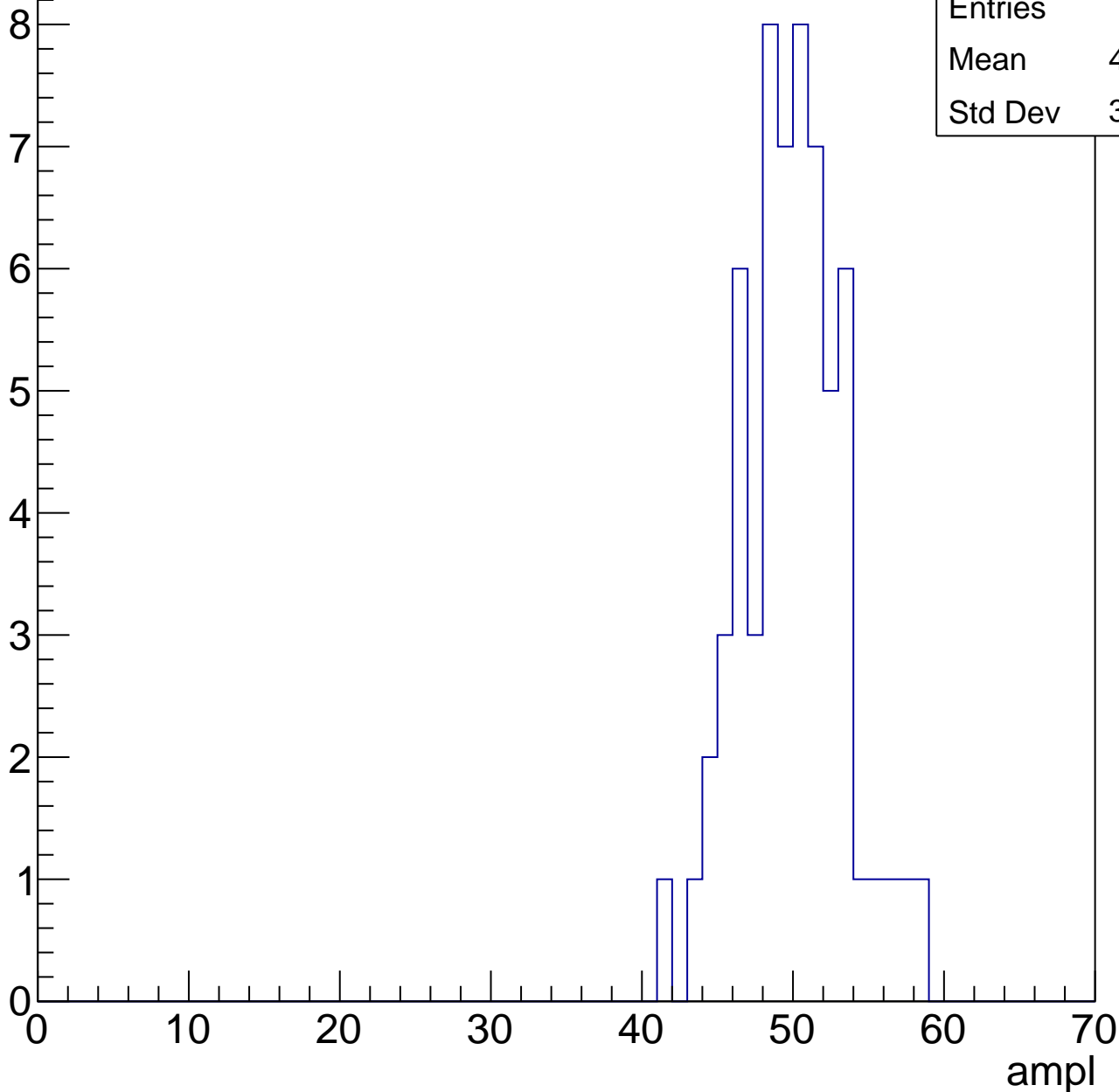


# B0L001S, U6-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	49.45
Std Dev	3.339

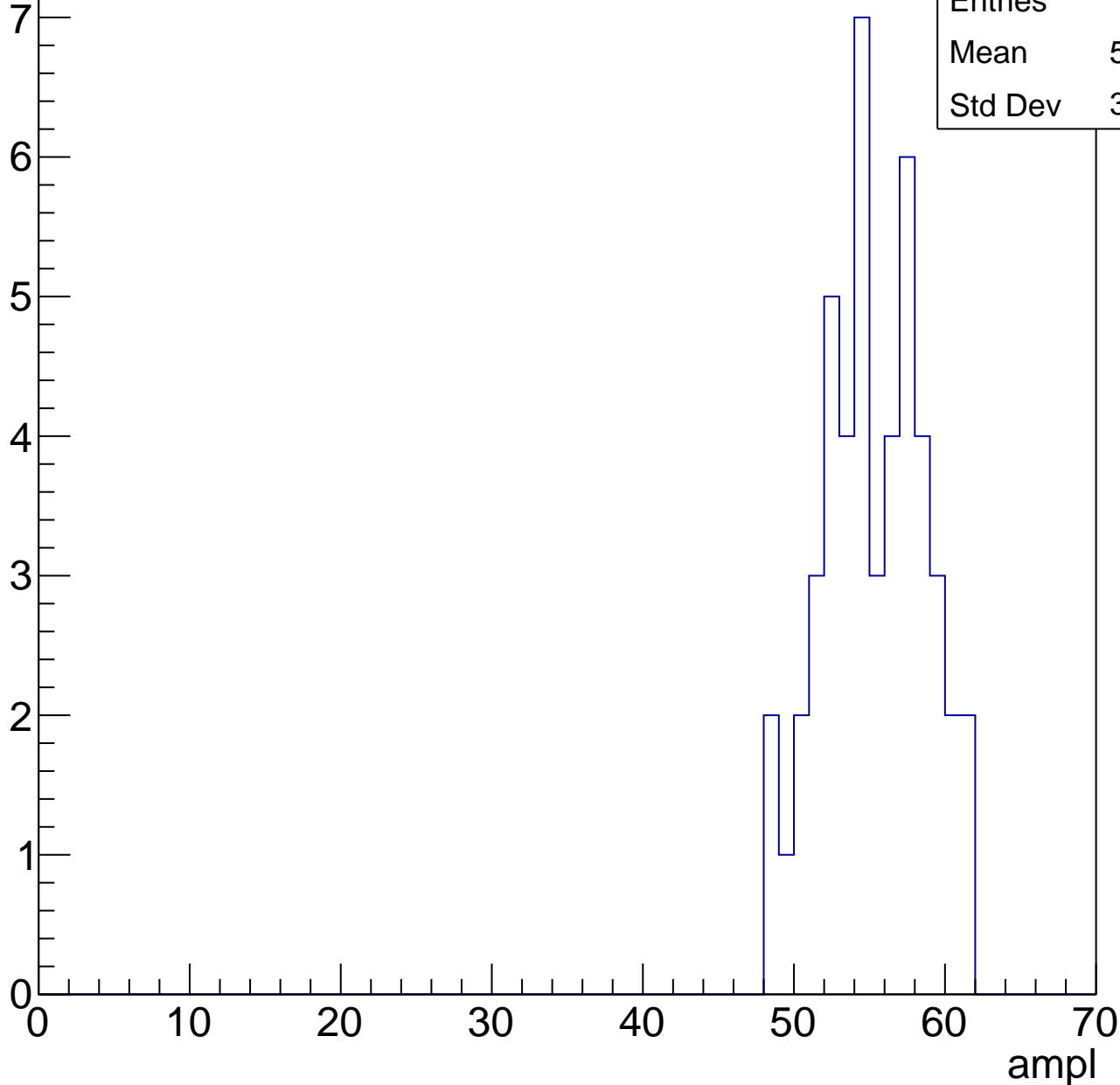


# B0L001S, U6-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	54.79
Std Dev	3.329

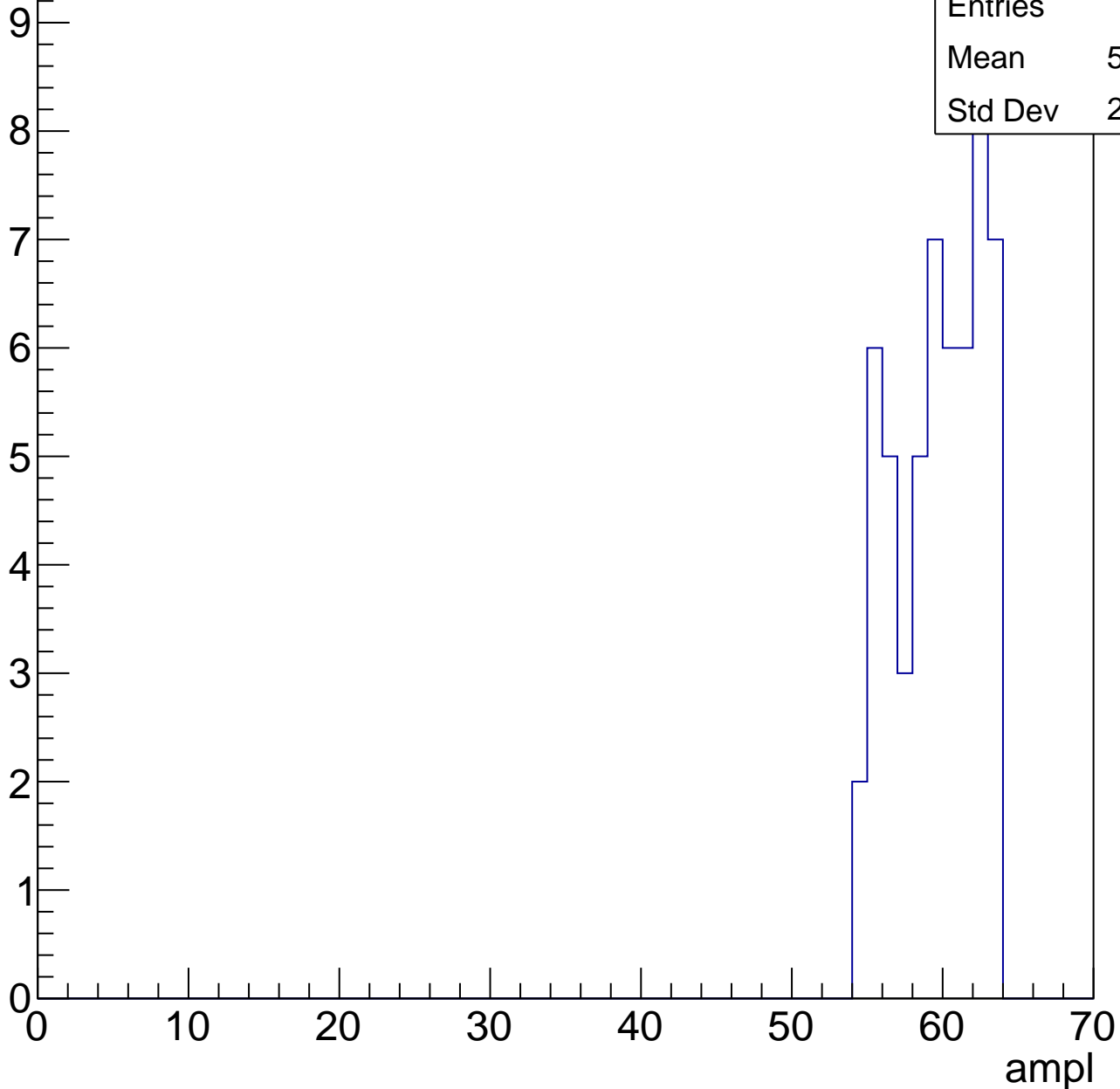


# B0L001S, U6-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

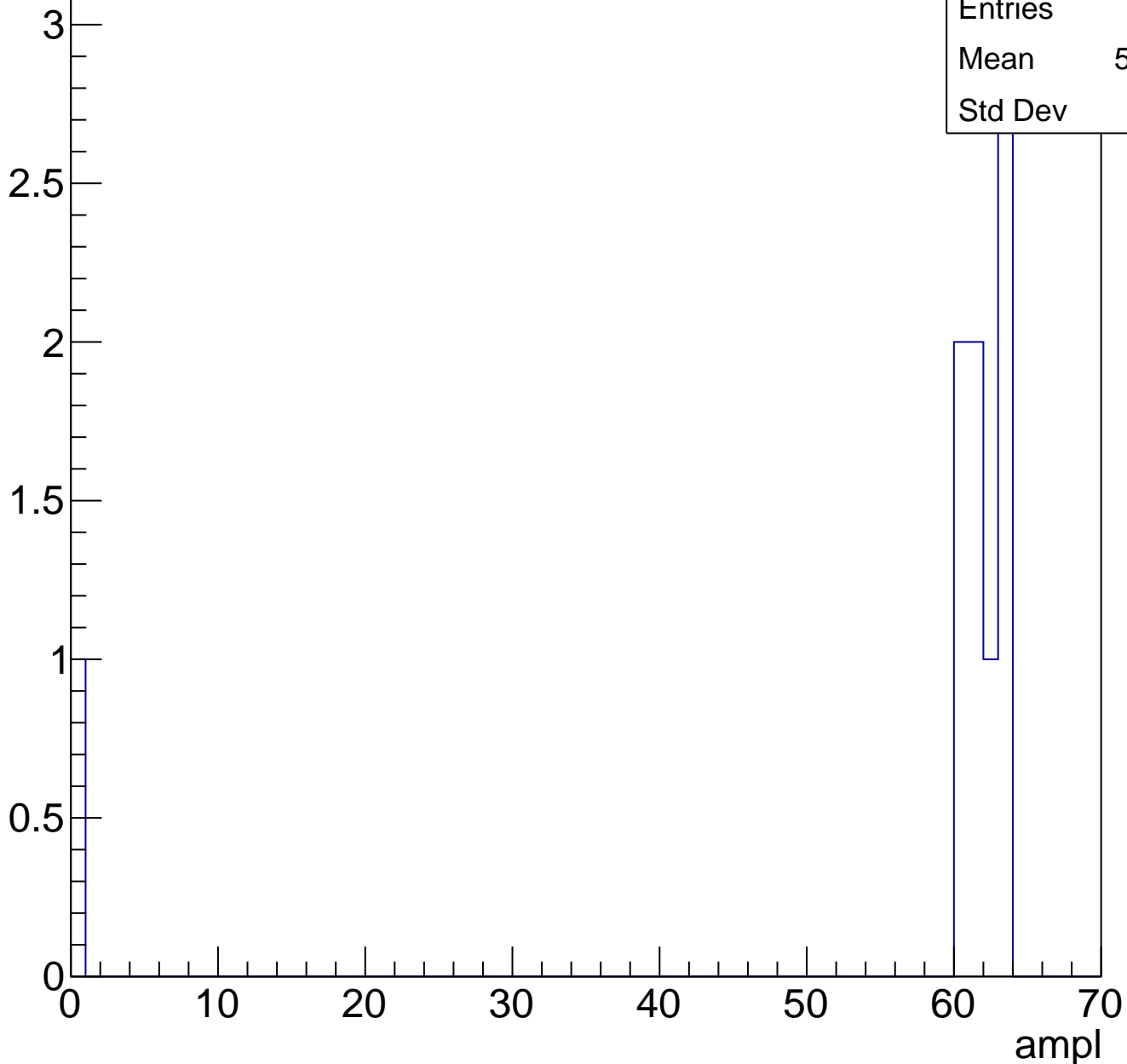
Entries	56
Mean	59.23
Std Dev	2.765



# B0L001S, U6-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	9
Mean	54.78
Std Dev	19.4



# B0L001S, U6-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U6-ch25, adc0

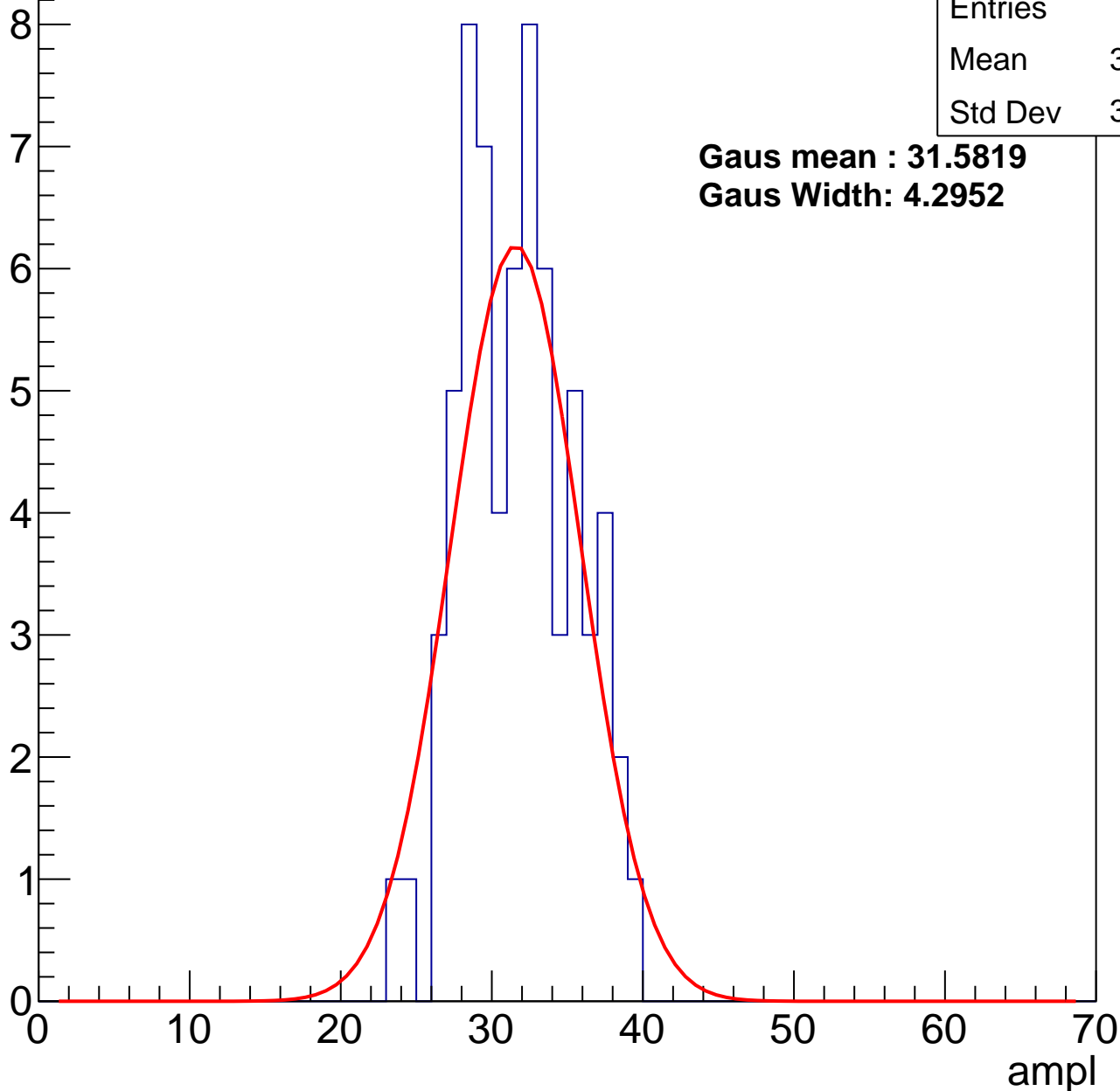
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	31.27
Std Dev	3.639

**Gaus mean : 31.5819**

**Gaus Width: 4.2952**



# B0L001S, U6-ch25, adc1

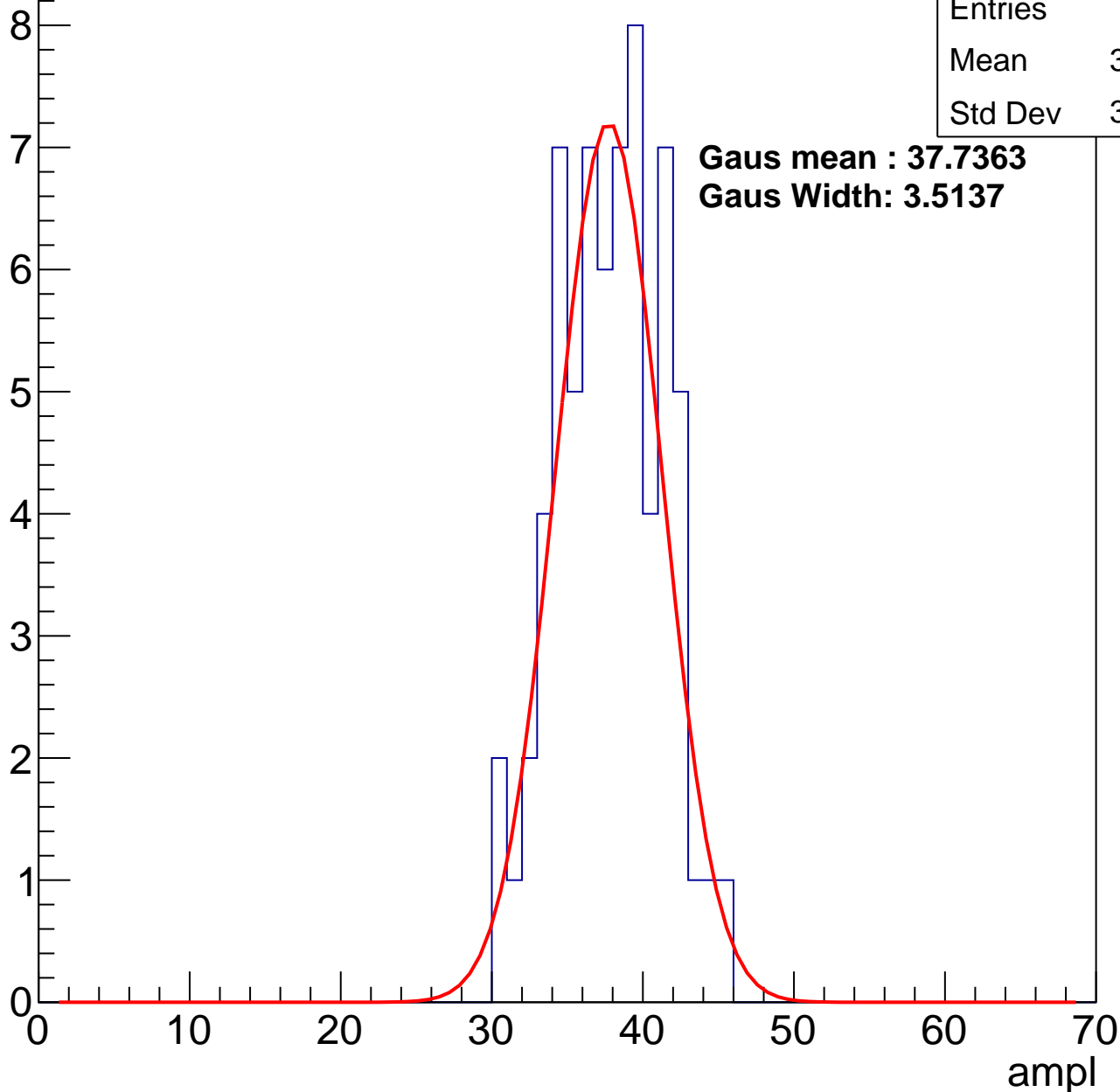
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	37.37
Std Dev	3.408

**Gaus mean : 37.7363**

**Gaus Width: 3.5137**



# B0L001S, U6-ch25, adc2

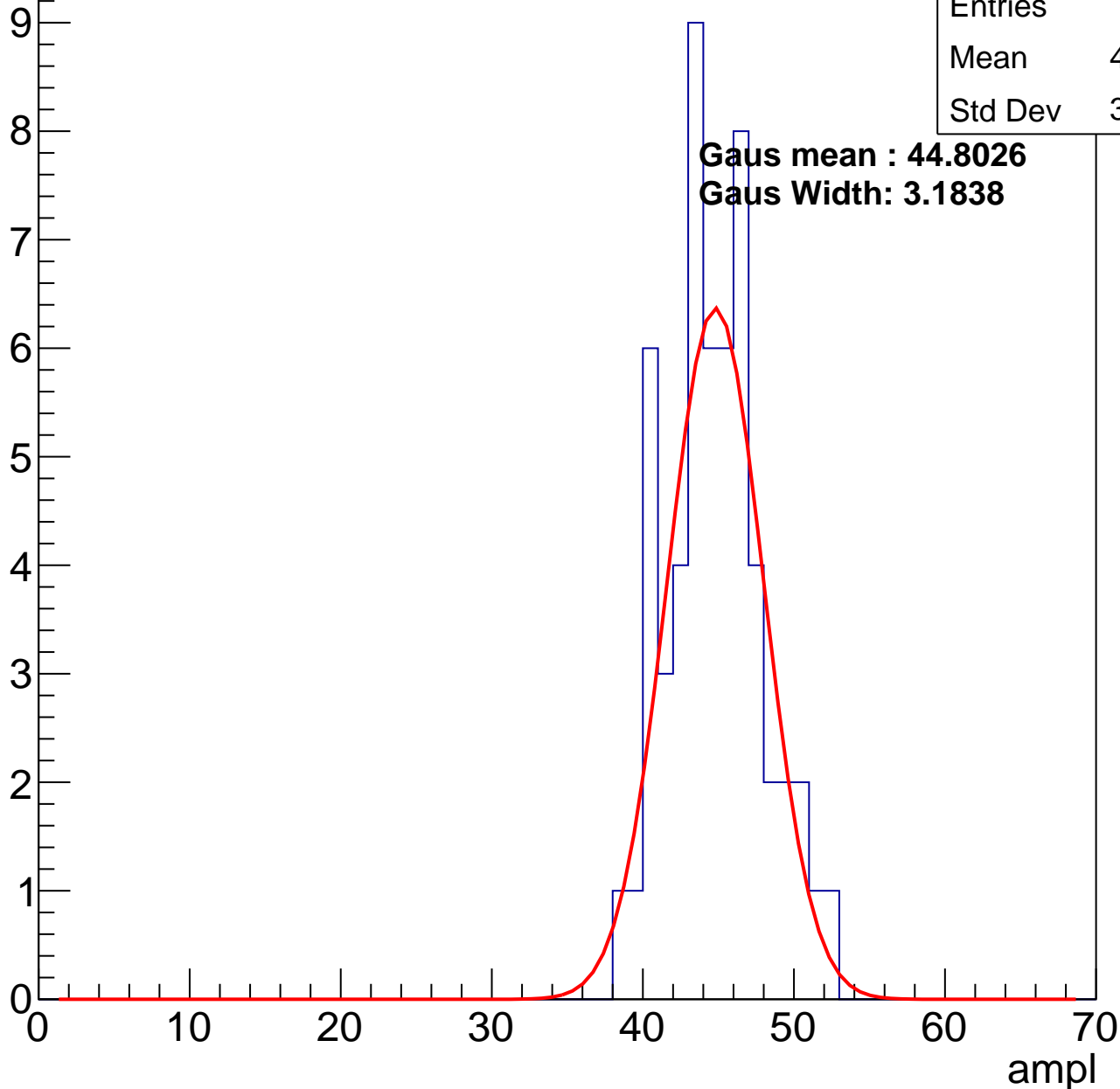
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	44.32
Std Dev	3.117

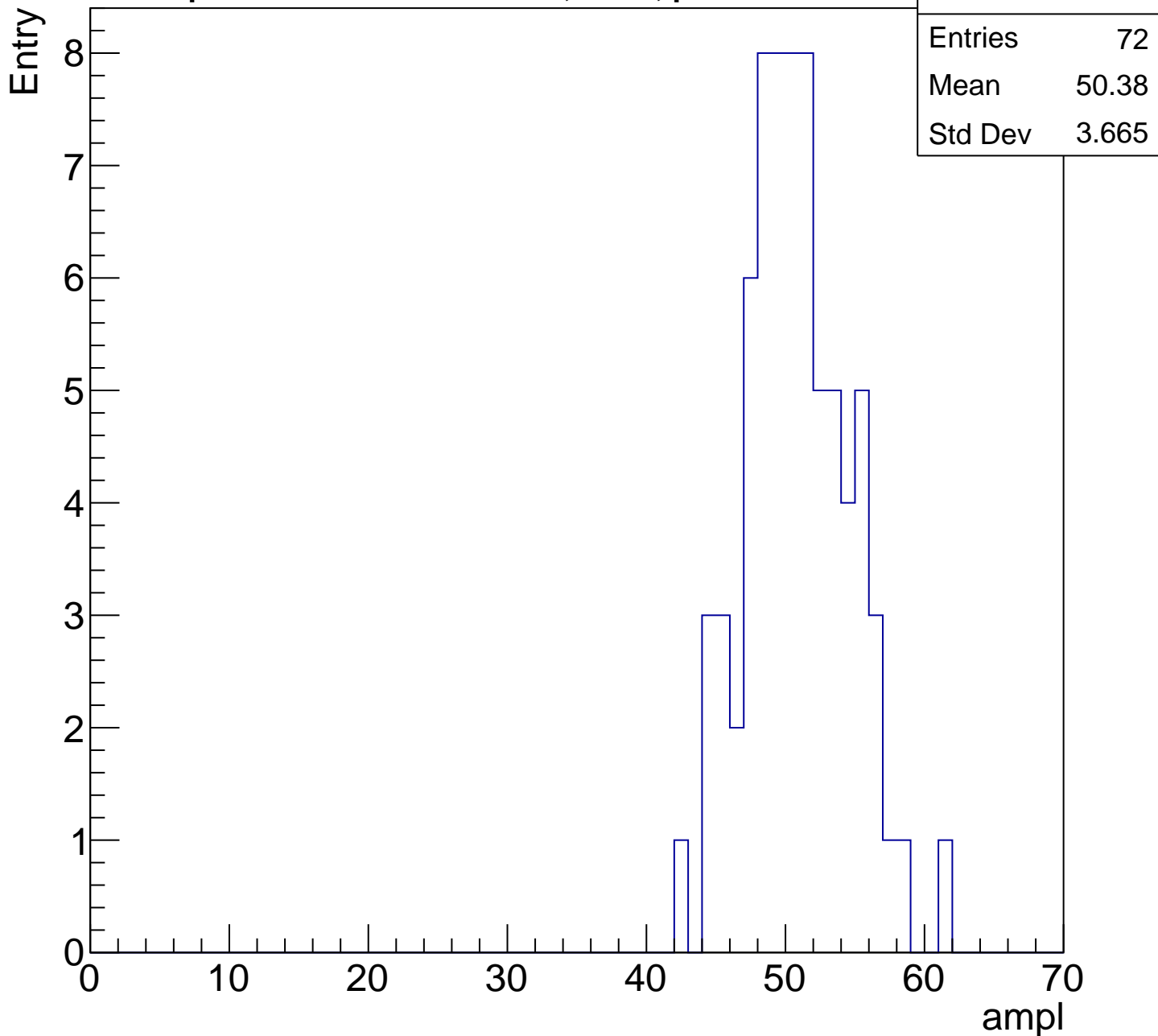
**Gaus mean : 44.8026**

**Gaus Width: 3.1838**



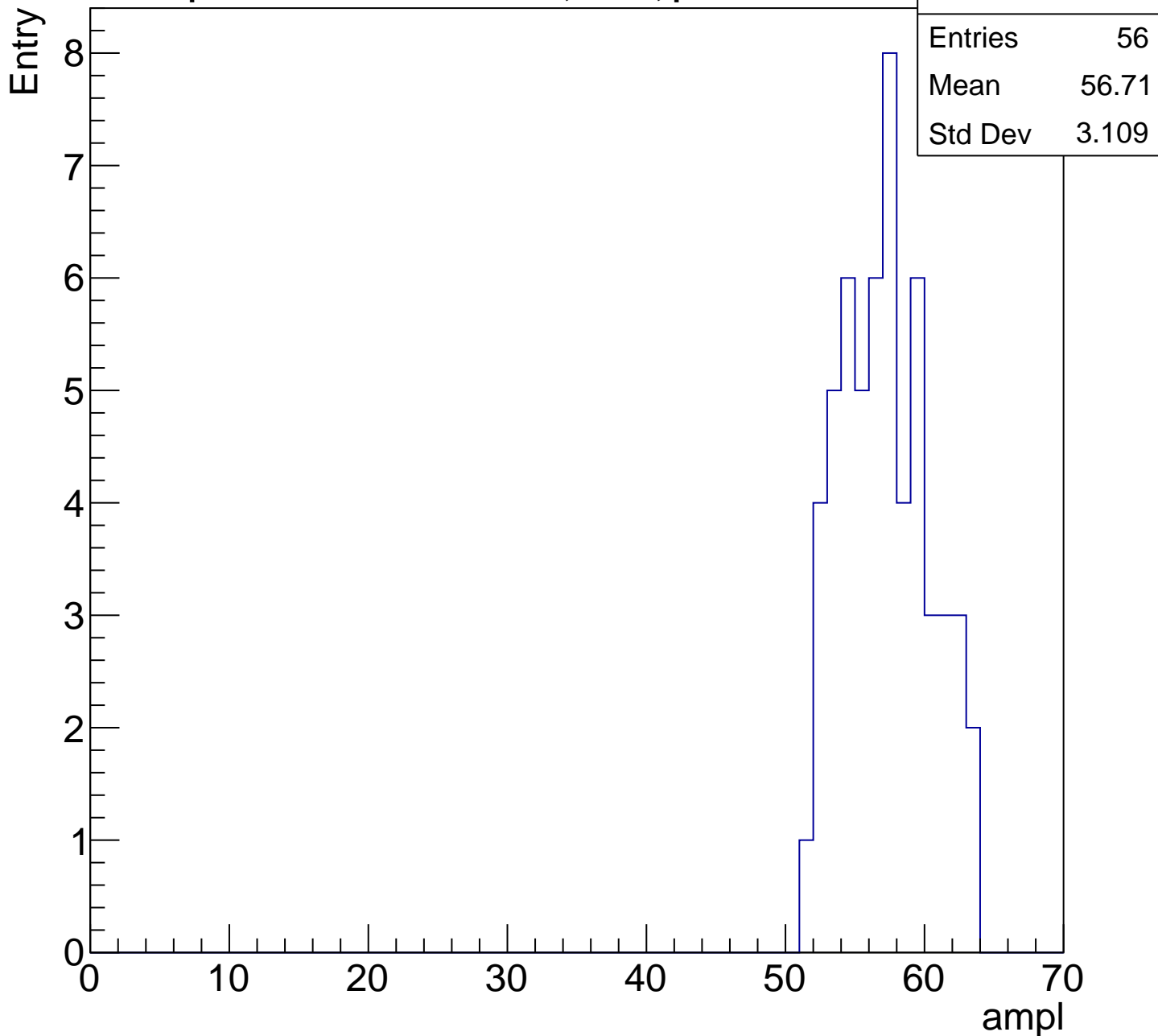
# B0L001S, U6-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U6-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

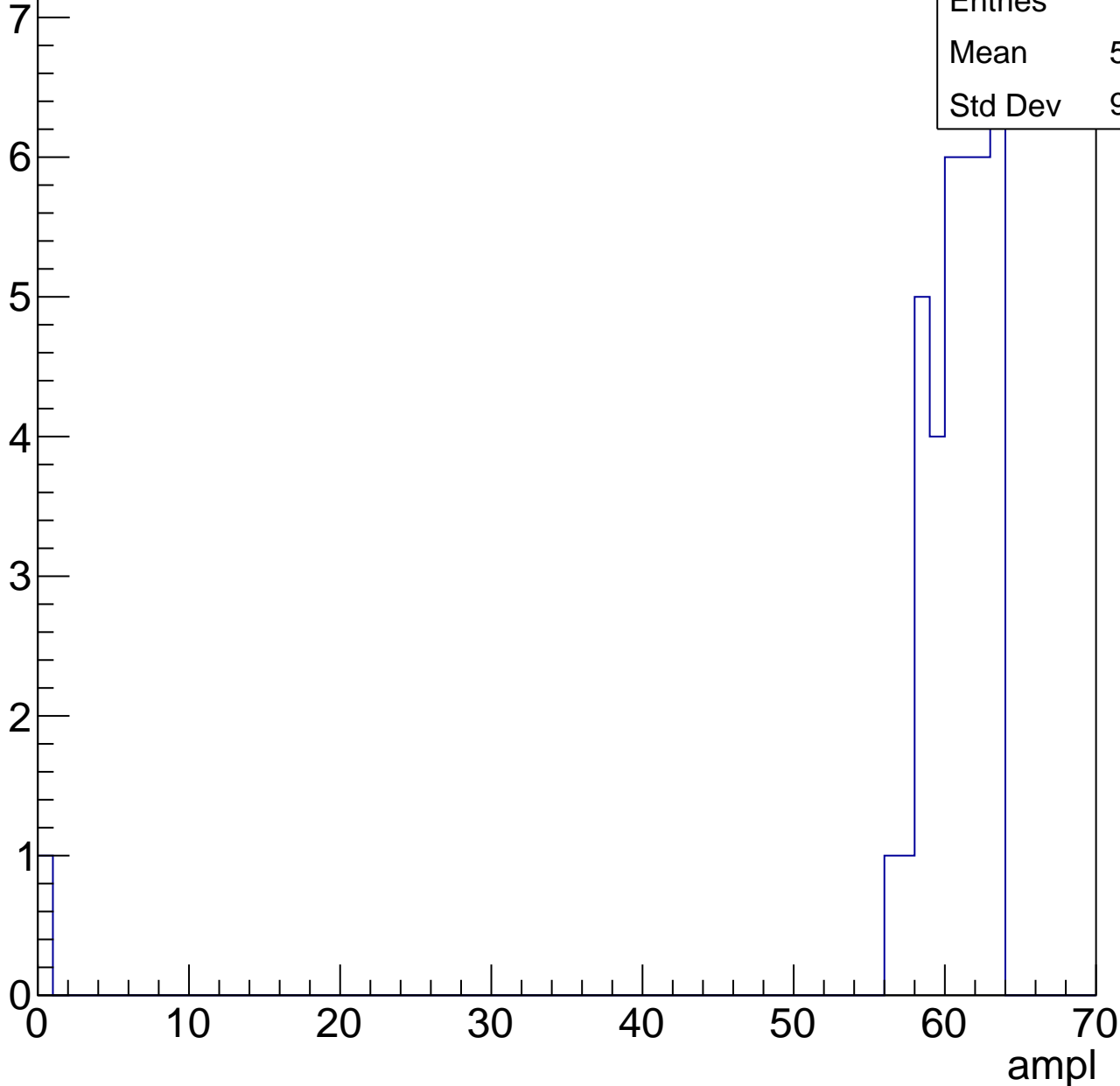


# B0L001S, U6-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

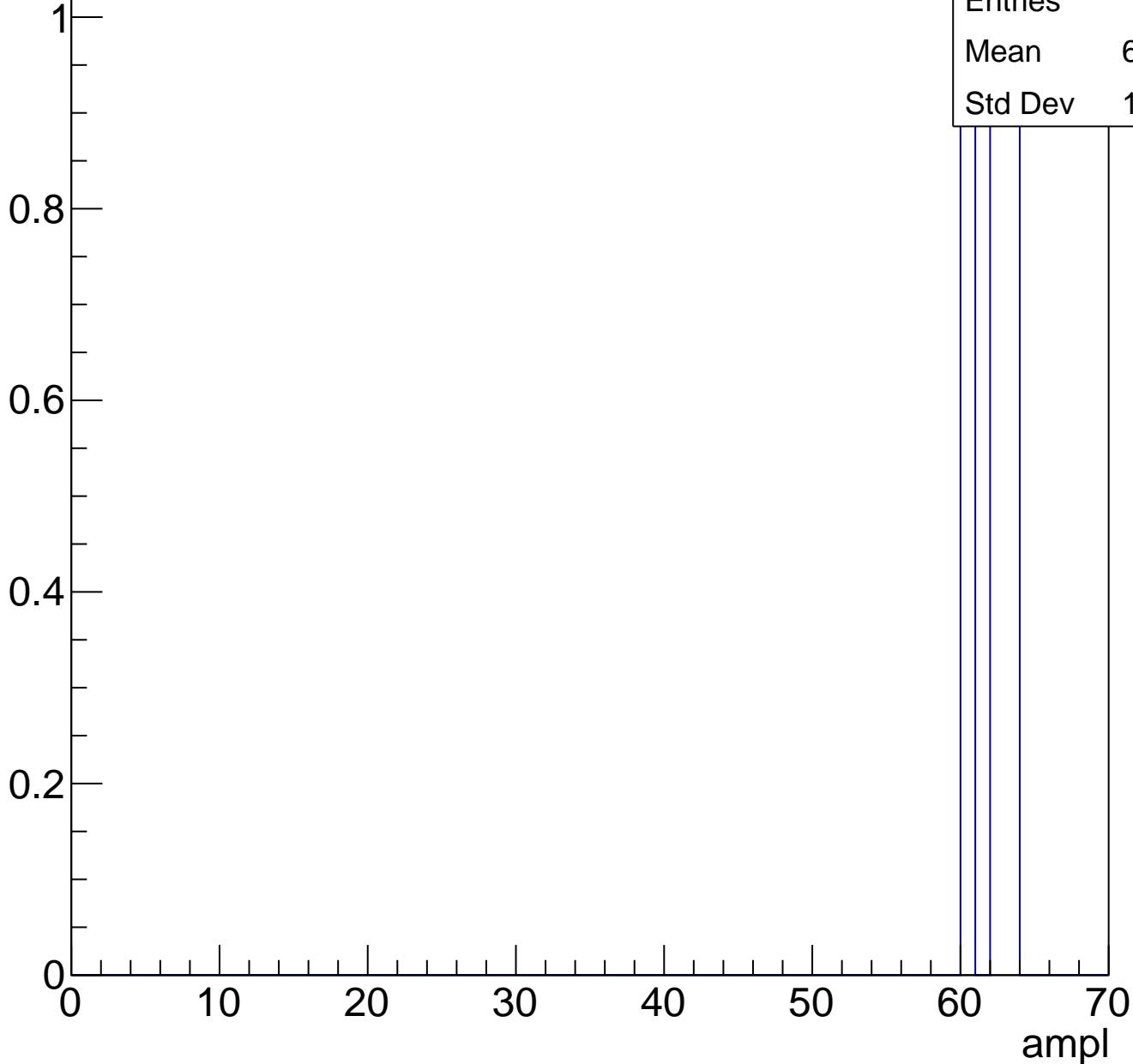
Entries	37
Mean	58.86
Std Dev	9.992



# B0L001S, U6-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U6-ch26, adc0

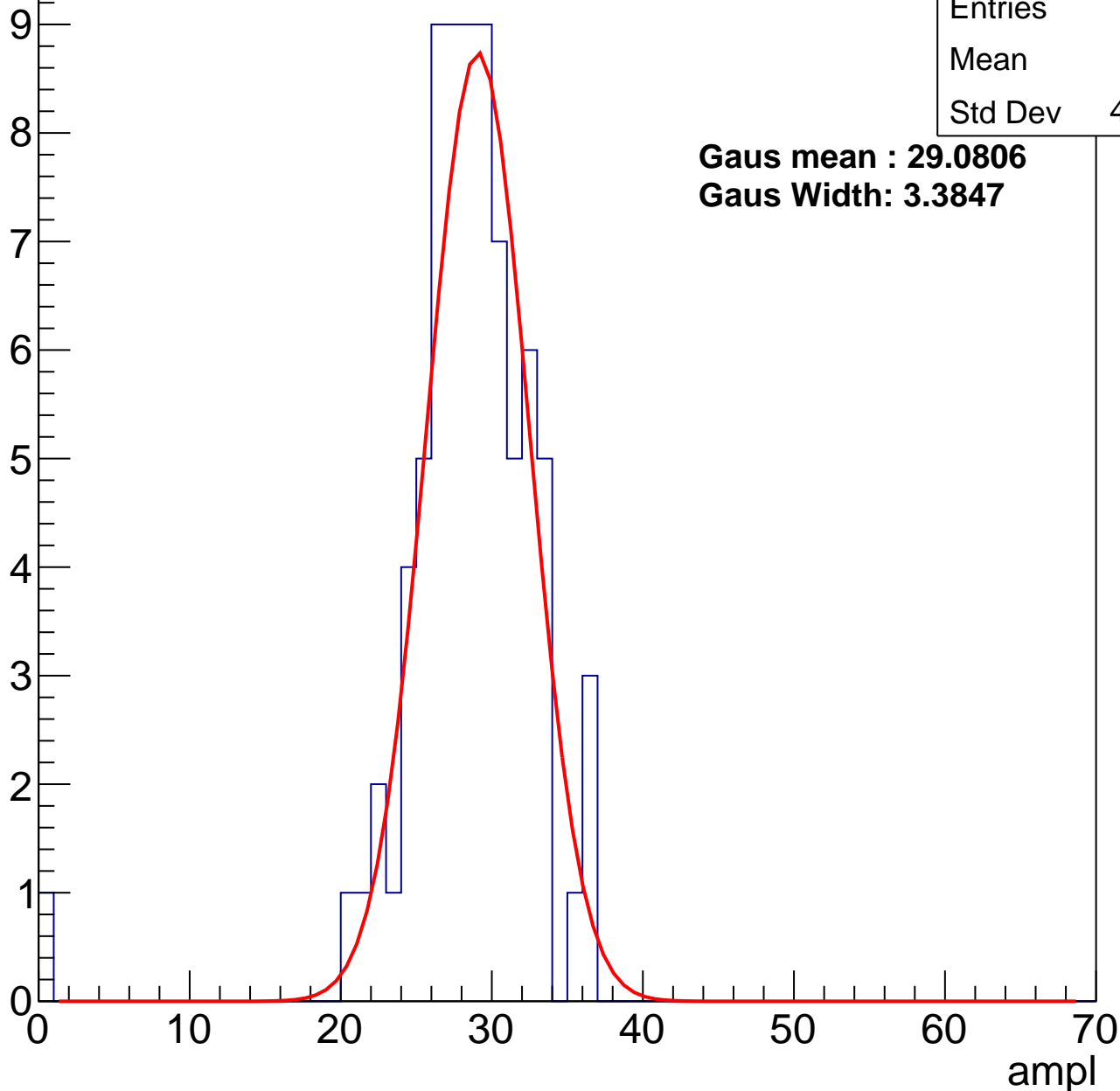
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	28
Std Dev	4.658

**Gaus mean : 29.0806**

**Gaus Width: 3.3847**



# B0L001S, U6-ch26, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	72
Mean	35.74
Std Dev	3.162

**Gaus mean : 35.9885**

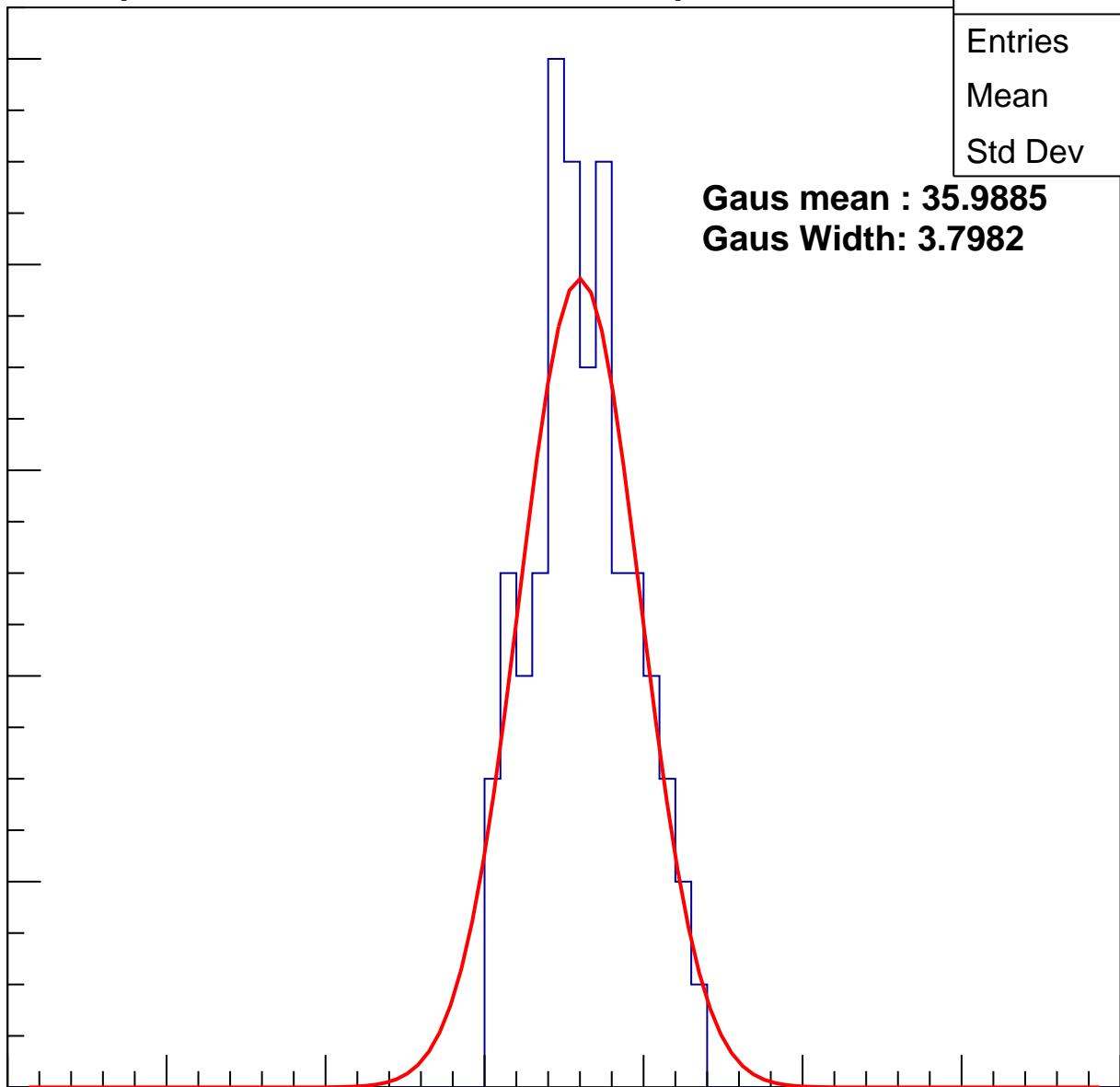
**Gaus Width: 3.7982**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U6-ch26, adc2

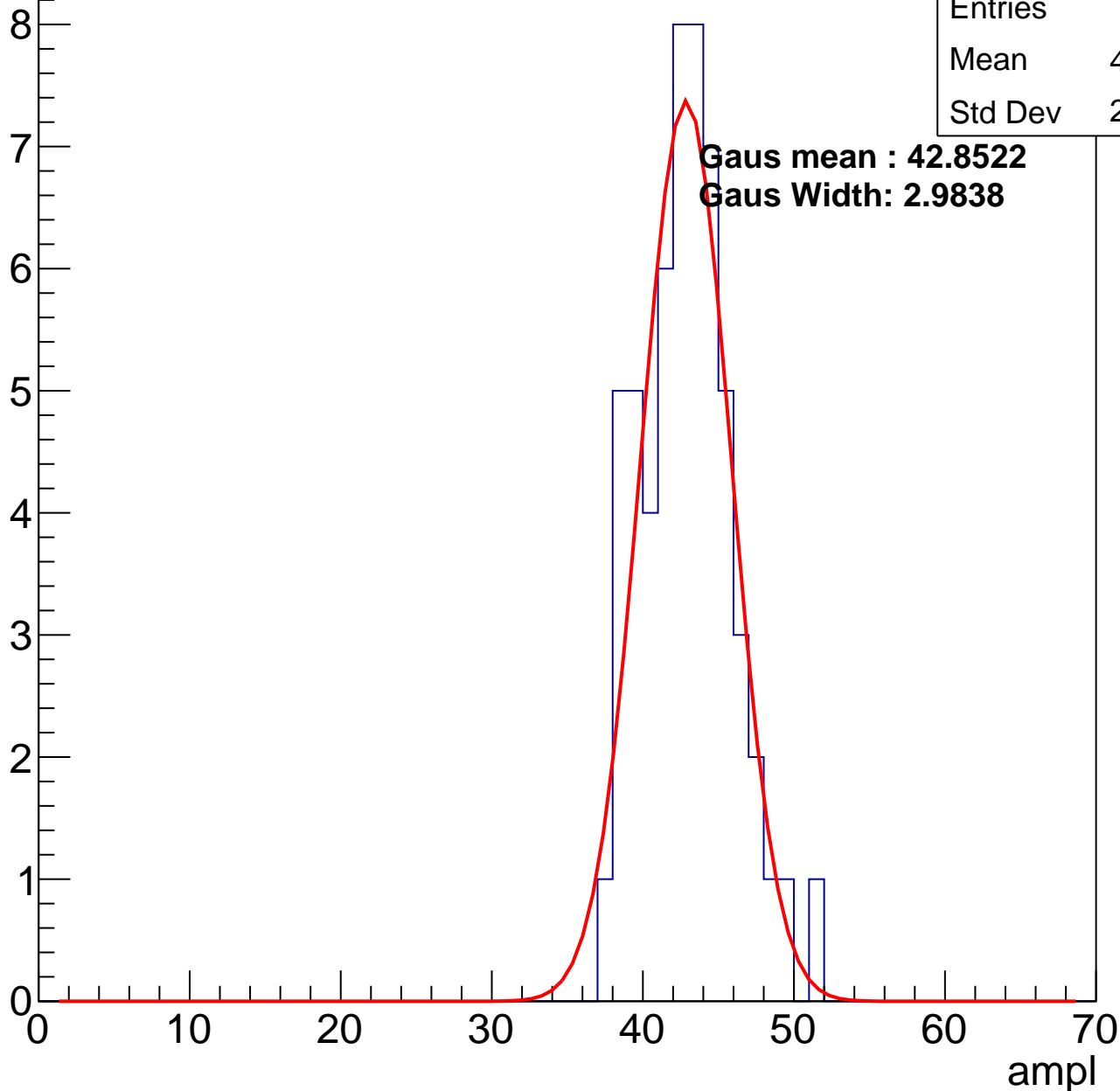
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	42.47
Std Dev	2.974

**Gaus mean : 42.8522**

**Gaus Width: 2.9838**



# B0L001S, U6-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

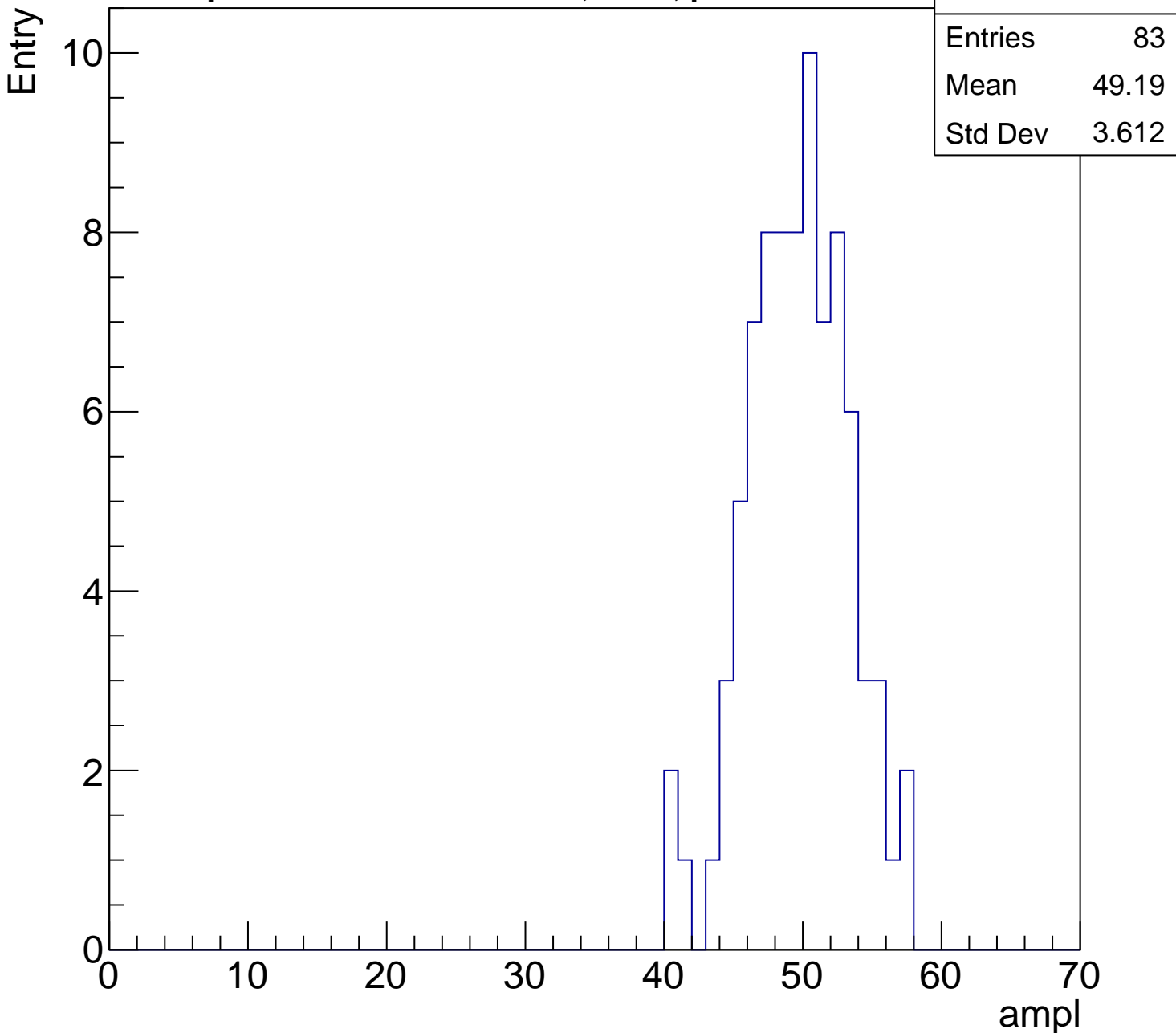
Entries	83
Mean	49.19
Std Dev	3.612

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

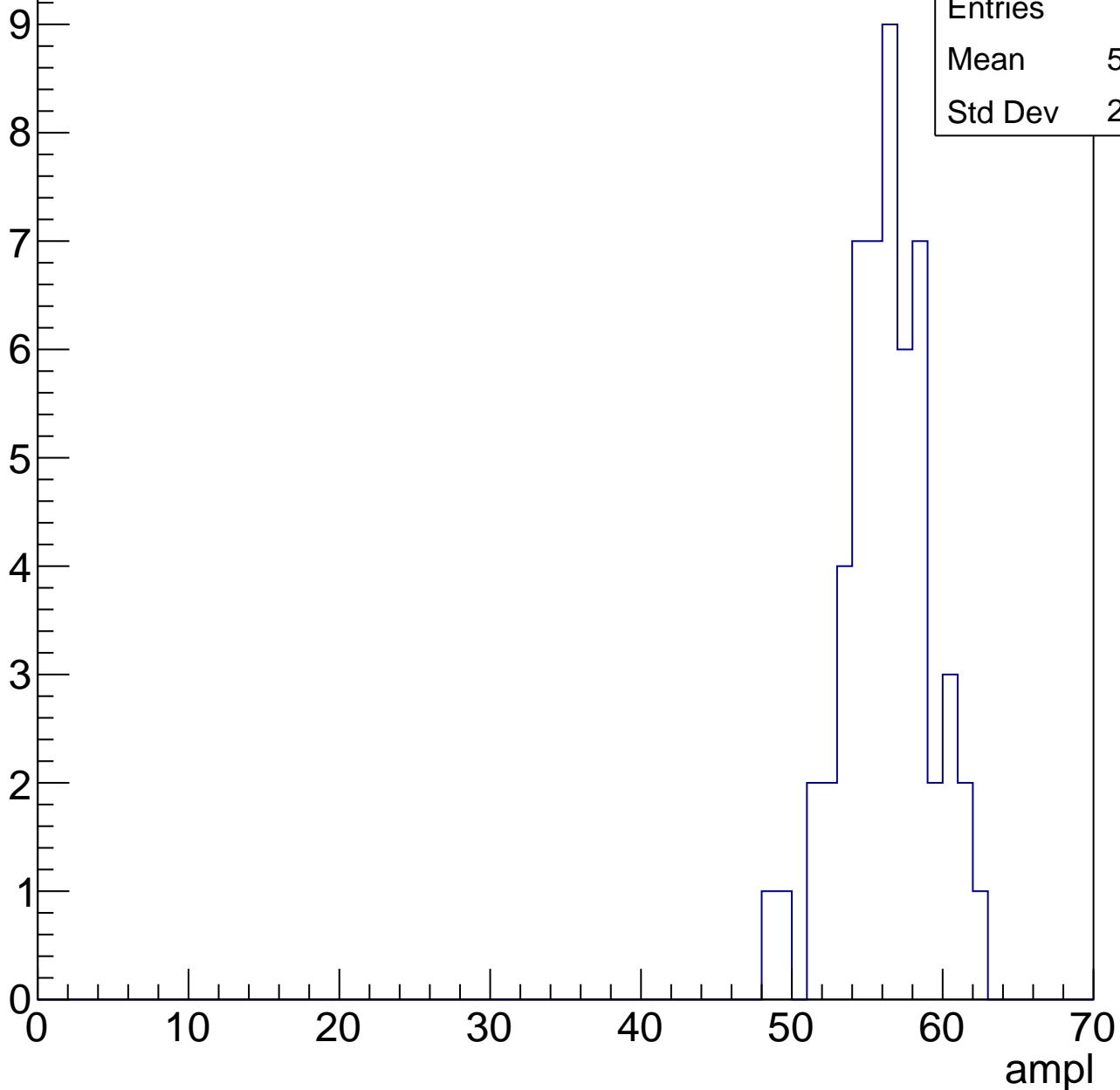


# B0L001S, U6-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

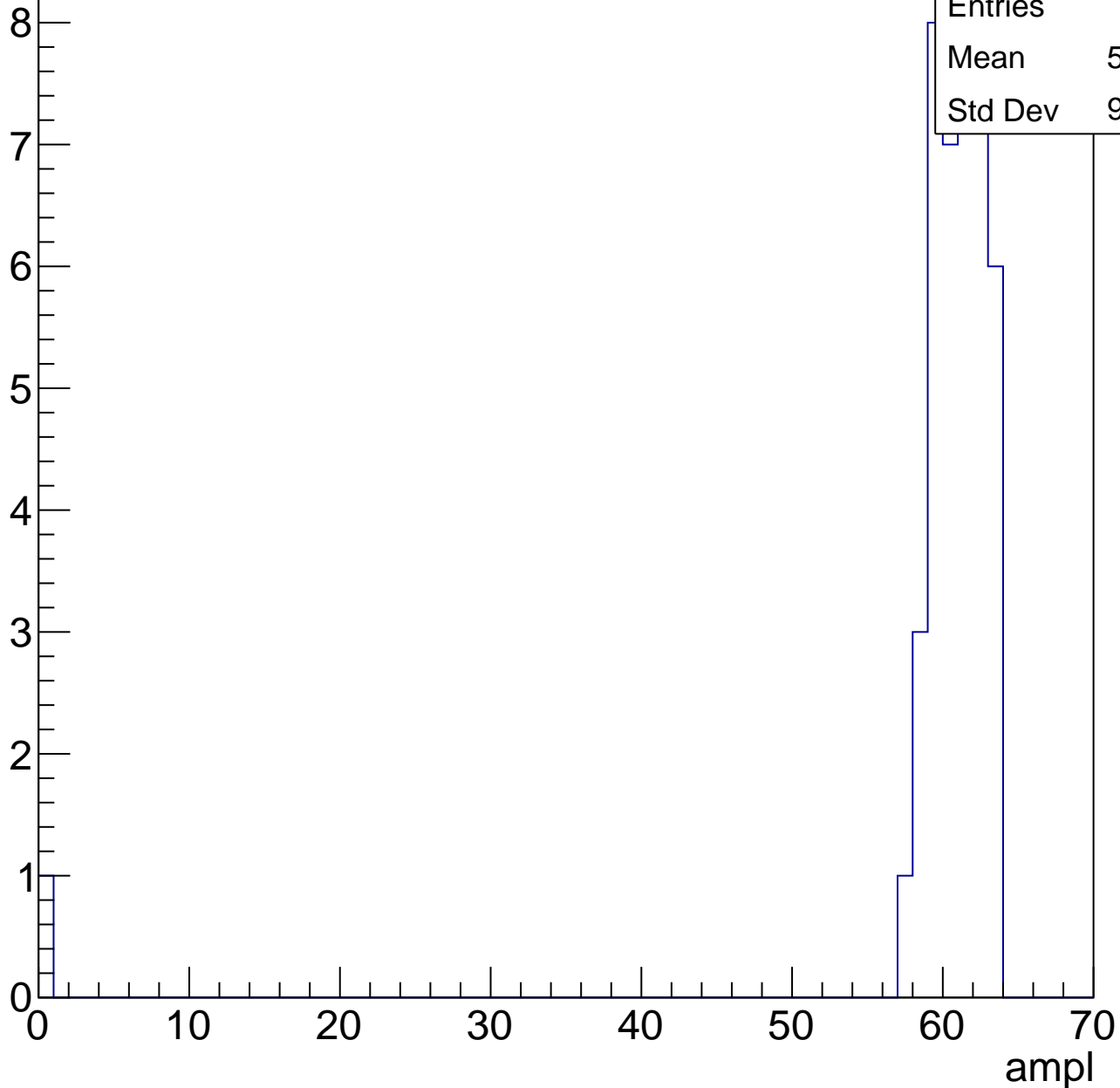
Entries	54
Mean	55.78
Std Dev	2.885



# B0L001S, U6-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

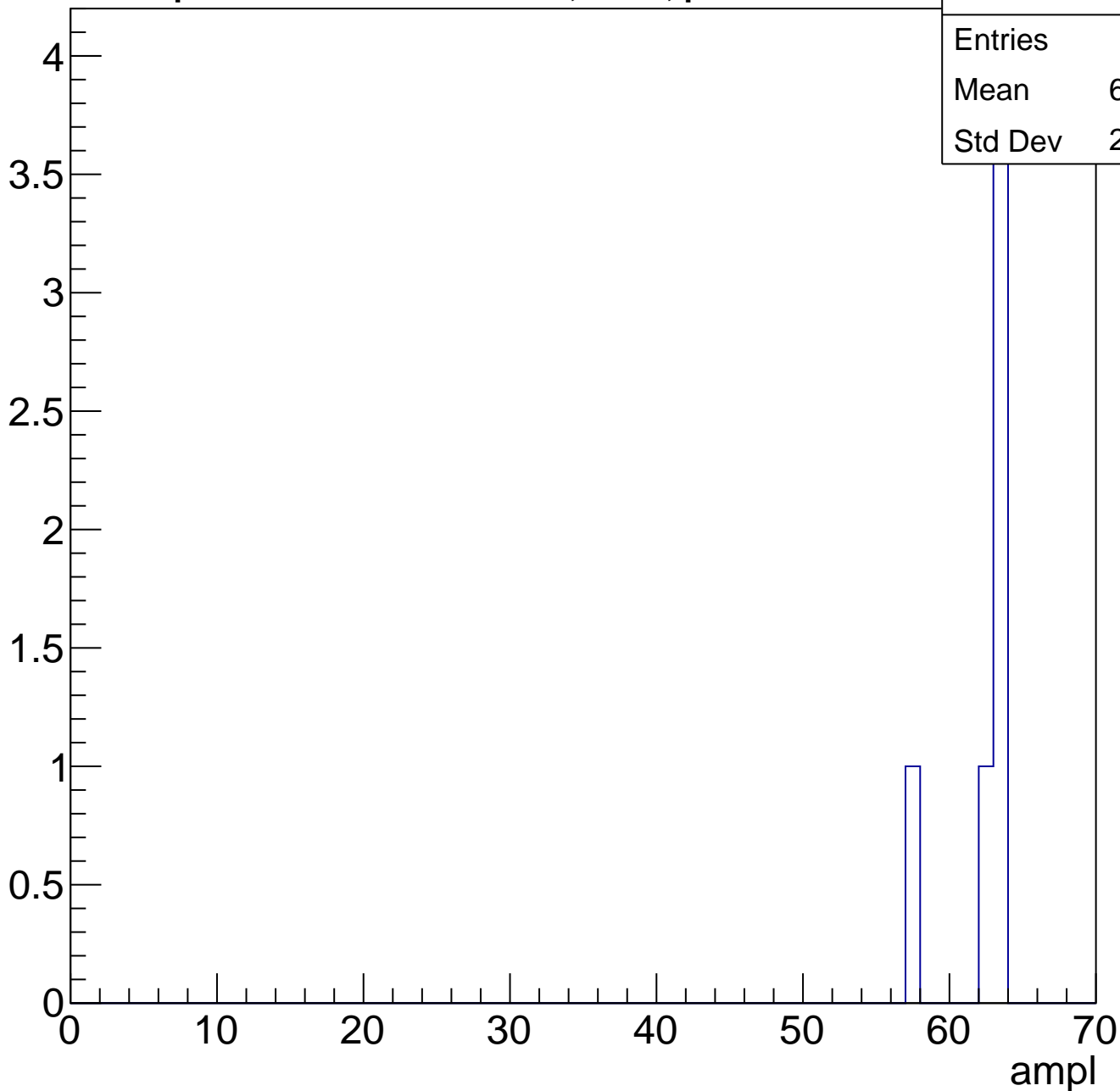
Entry



# B0L001S, U6-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch27, adc0

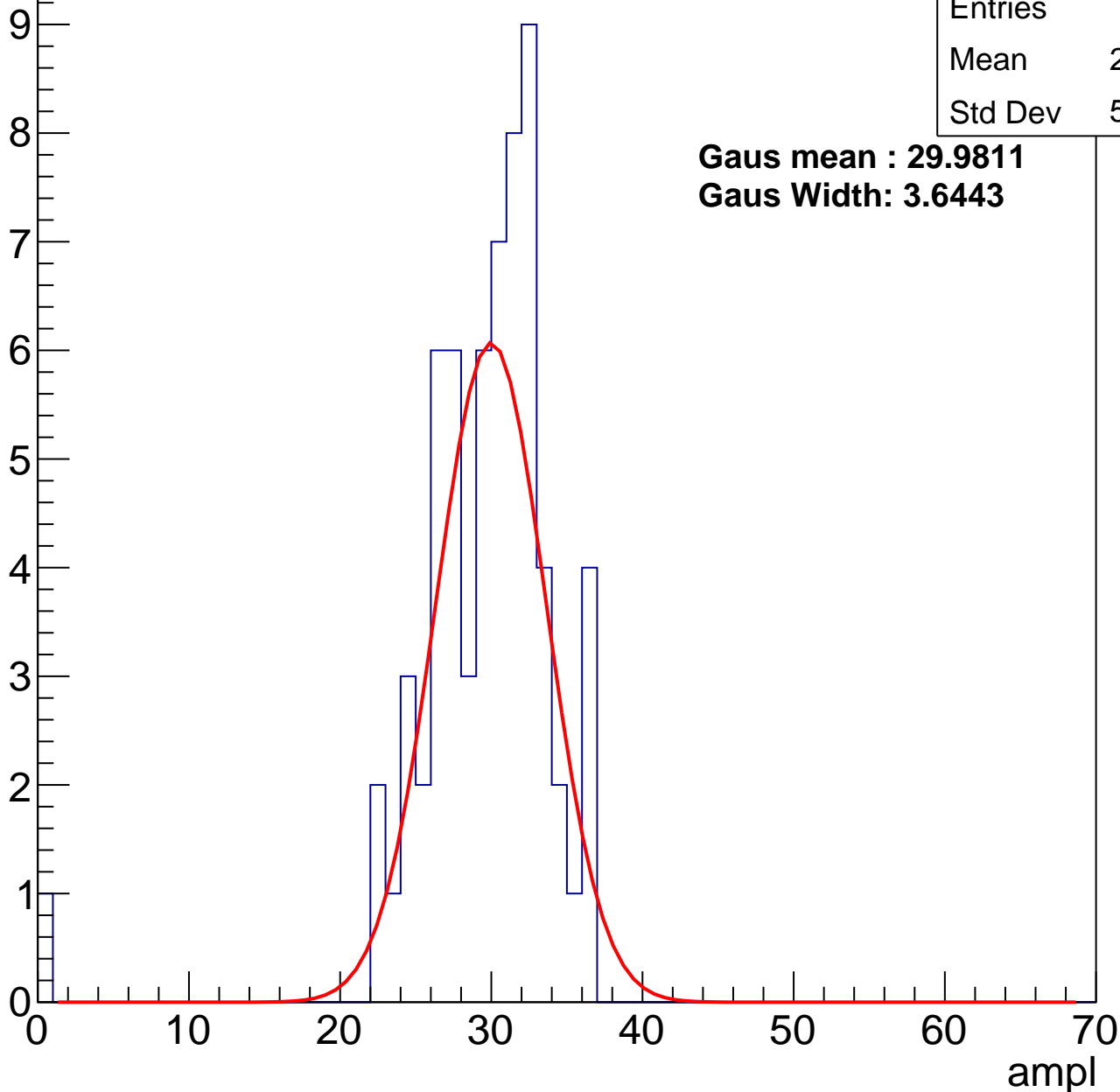
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	29.08
Std Dev	5.006

**Gaus mean : 29.9811**

**Gaus Width: 3.6443**



# B0L001S, U6-ch27, adc1

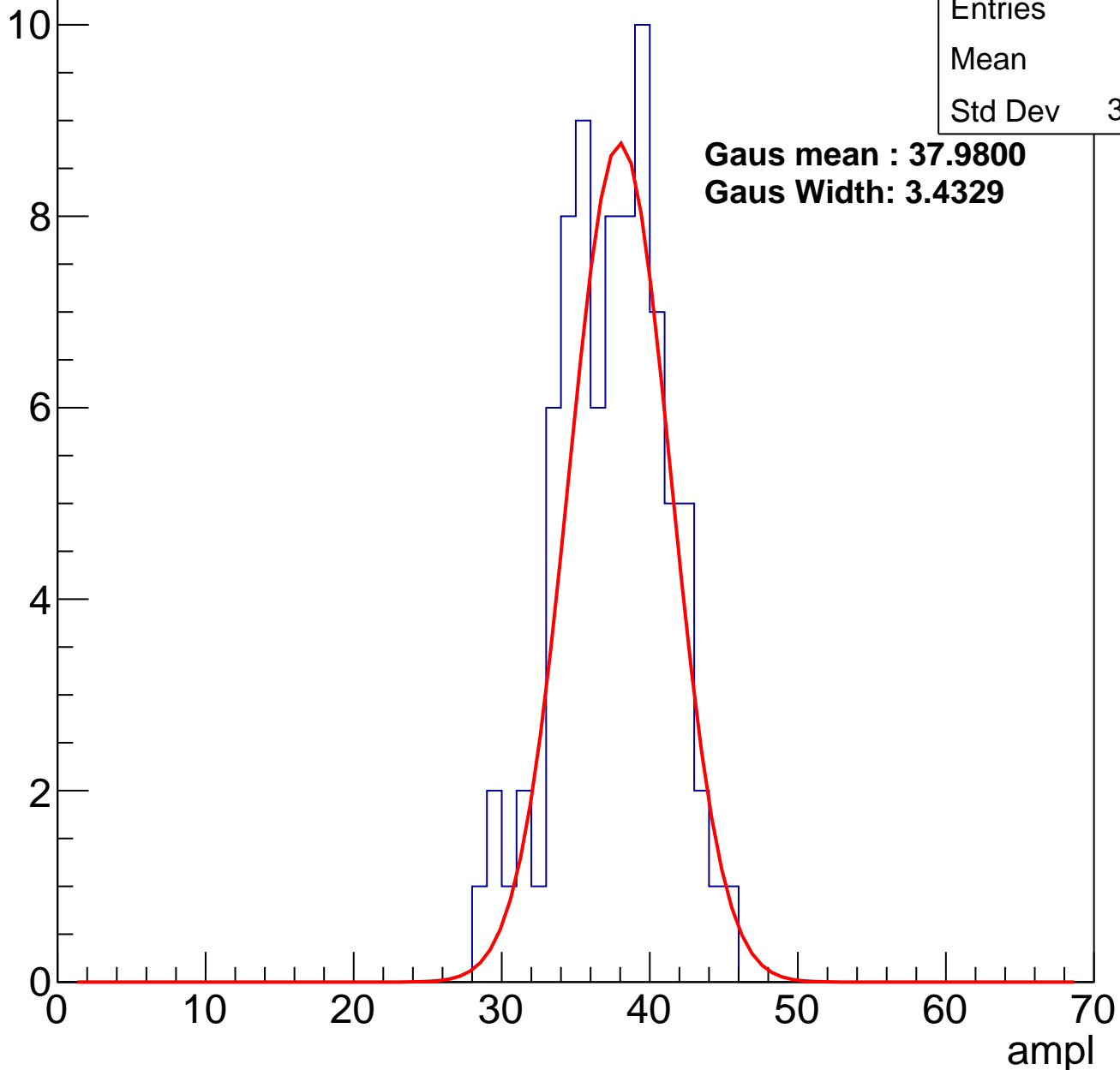
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	83
Mean	37
Std Dev	3.584

**Gaus mean : 37.9800**

**Gaus Width: 3.4329**

Entry



# B0L001S, U6-ch27, adc2

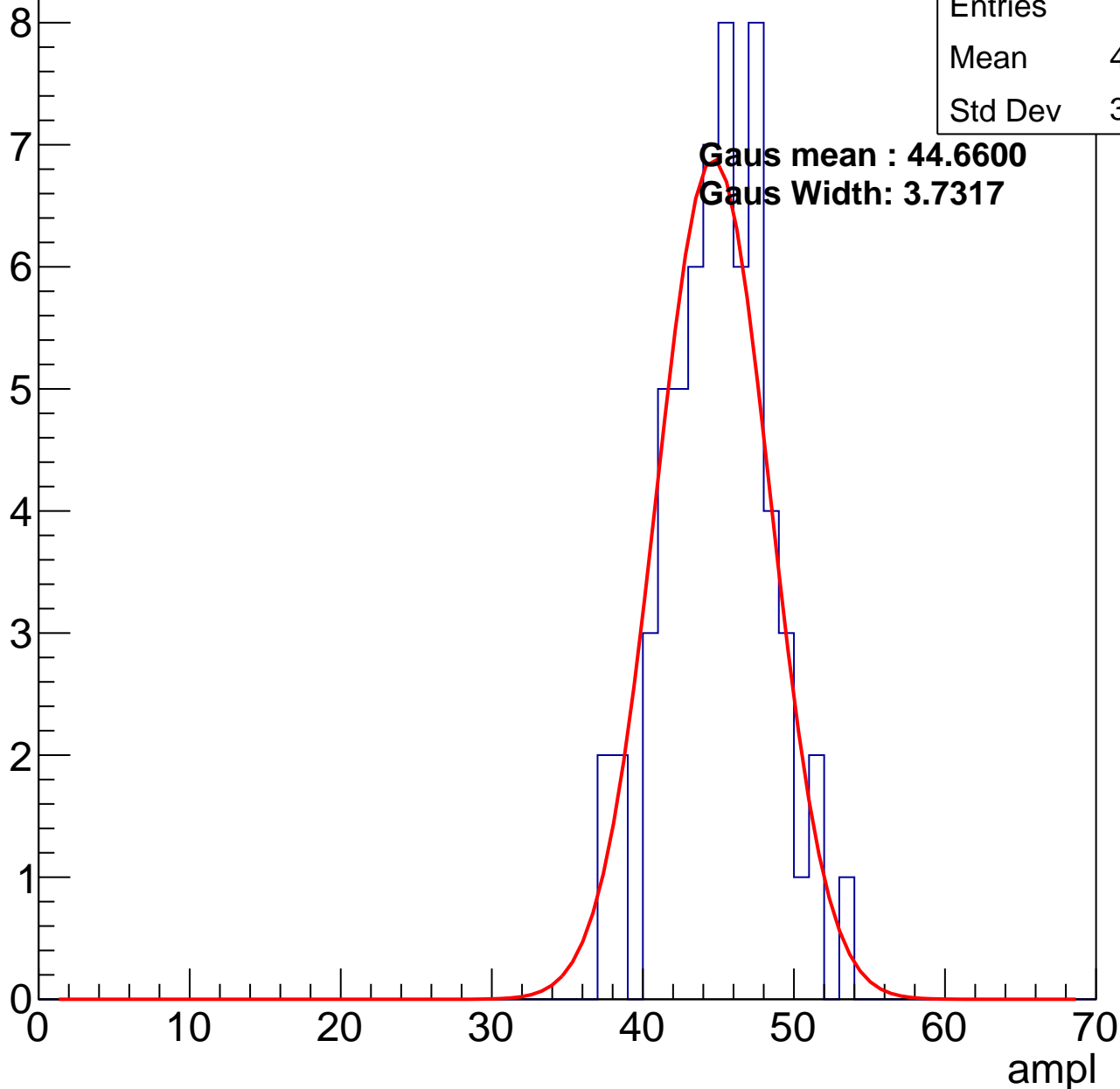
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	44.56
Std Dev	3.398

**Gaus mean : 44.6600**

**Gaus Width: 3.7317**

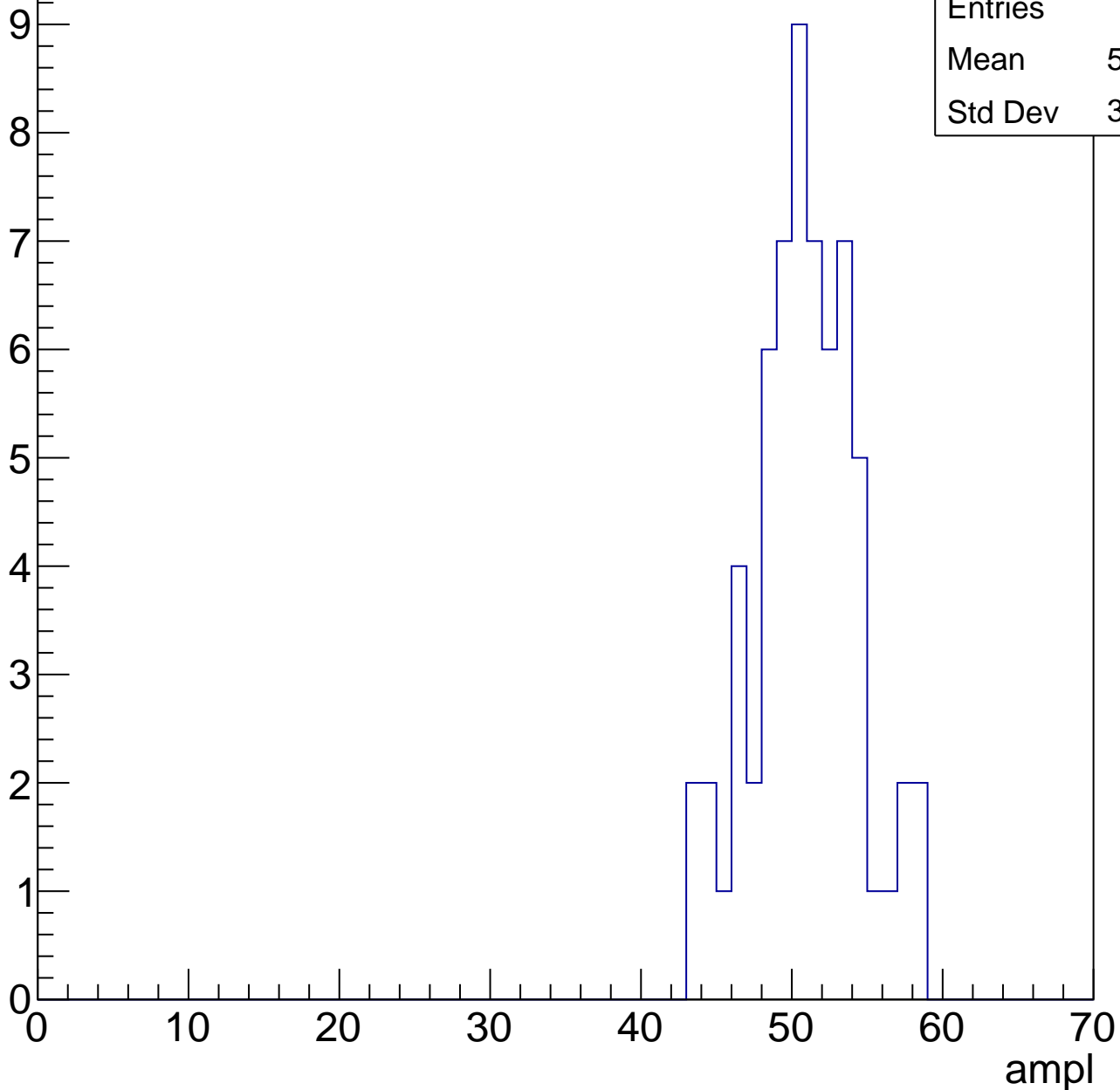


# B0L001S, U6-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

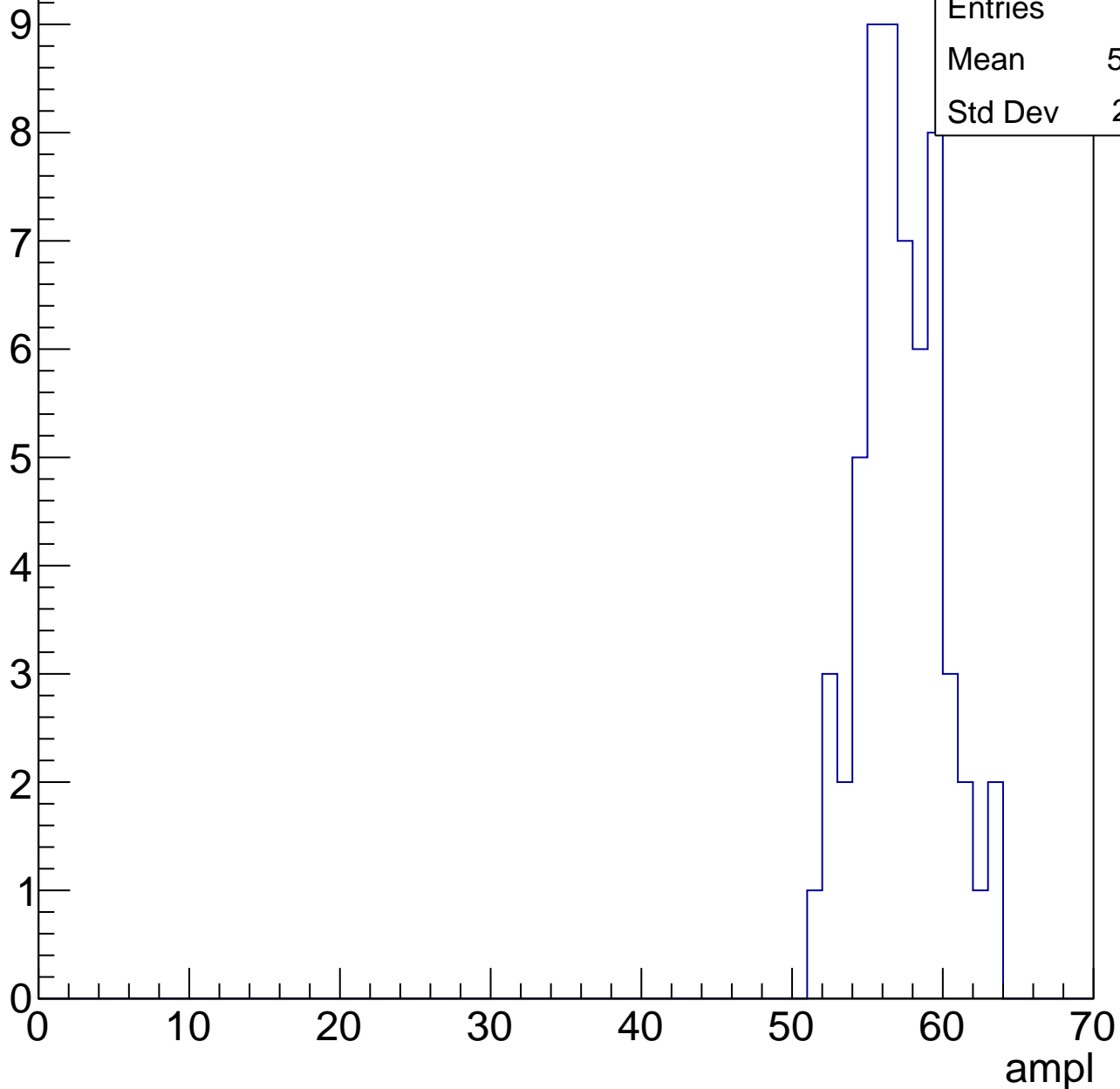
Entries	64
Mean	50.45
Std Dev	3.437



# B0L001S, U6-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



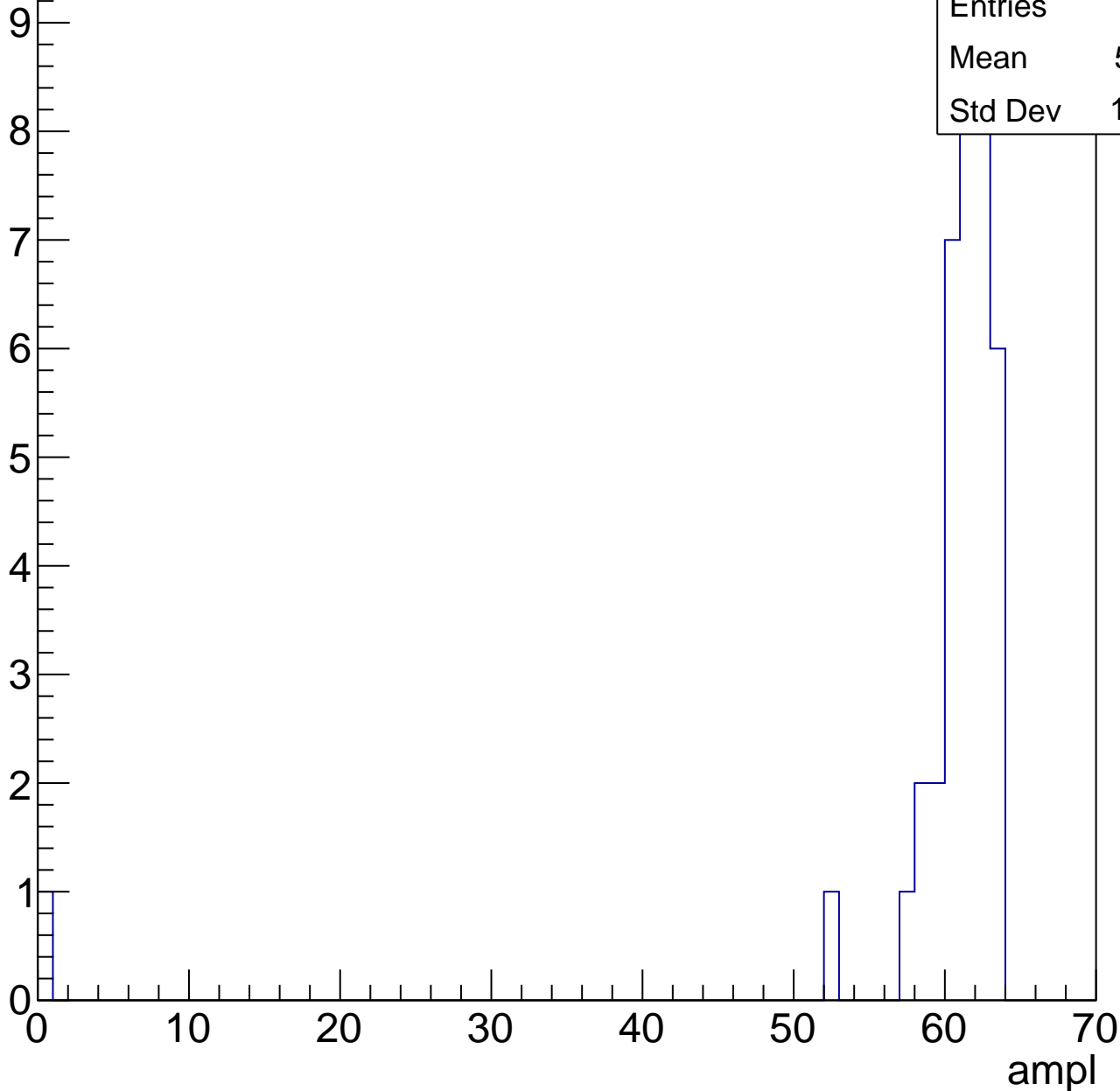
Entries	58
Mean	56.74
Std Dev	2.701

# B0L001S, U6-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	37
Mean	59.11
Std Dev	10.07



# B0L001S, U6-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	7
Std Dev	9.899

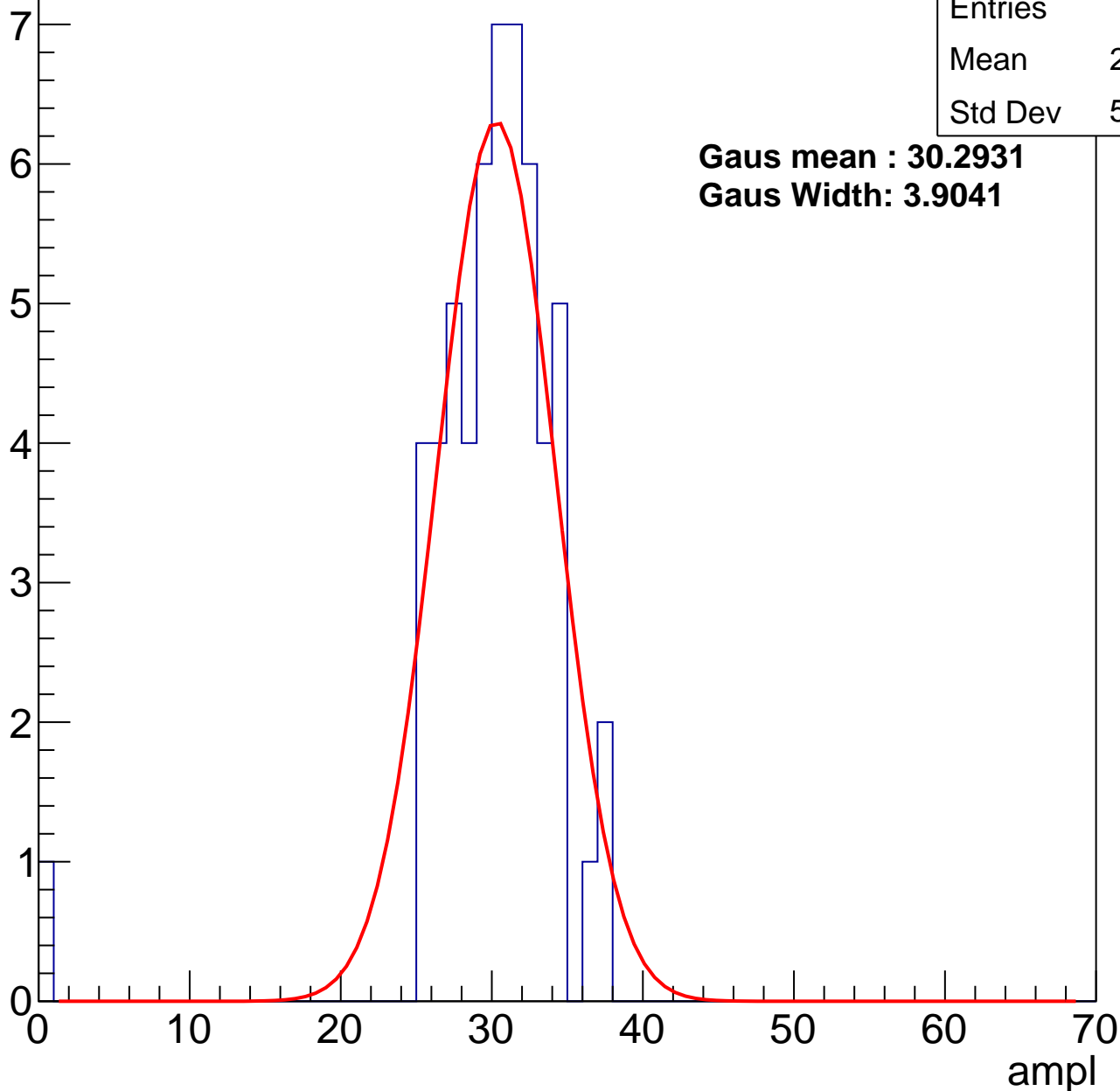
# B0L001S, U6-ch28, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	29.57
Std Dev	5.003

**Gaus mean : 30.2931**  
**Gaus Width: 3.9041**



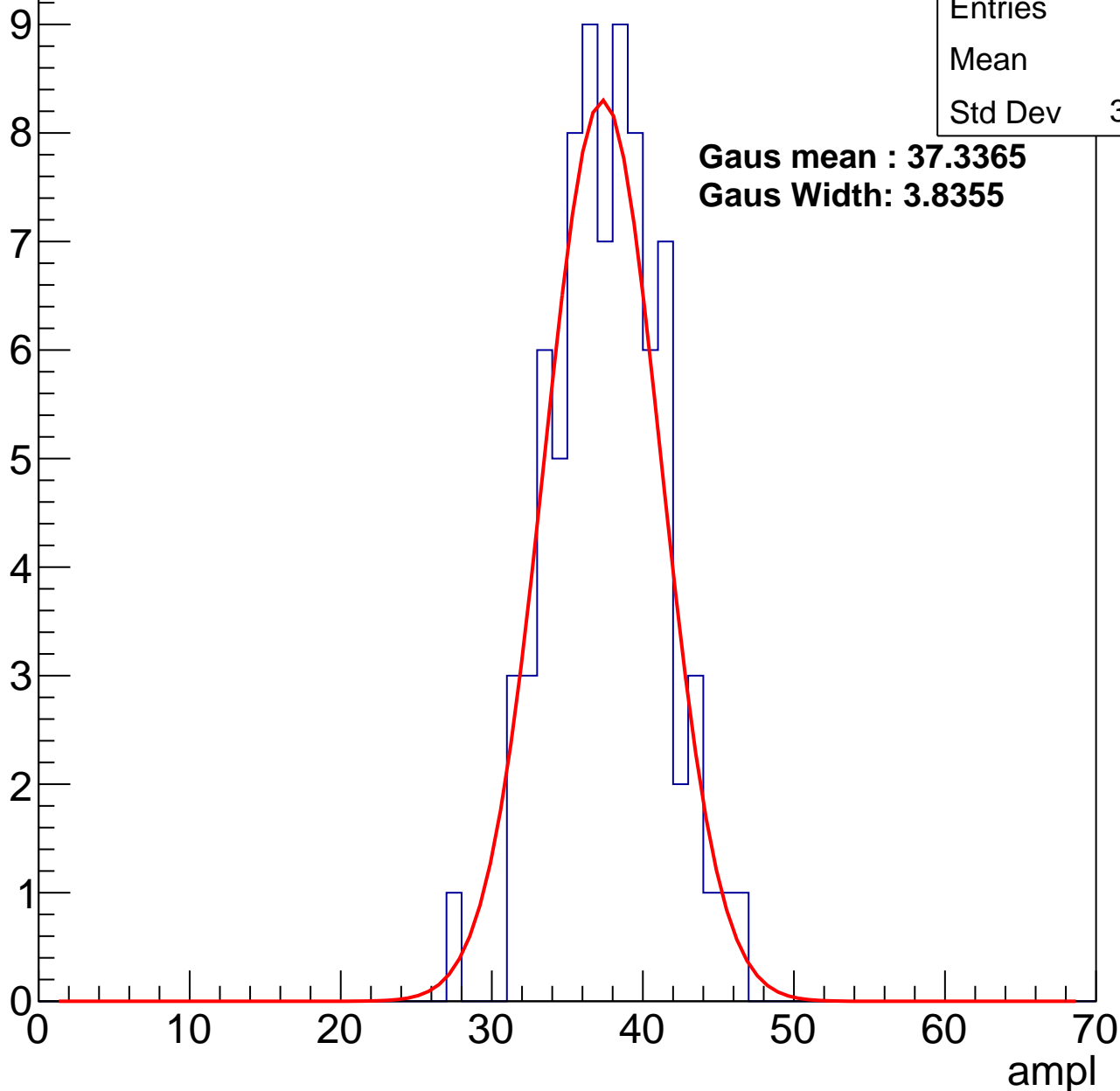
# B0L001S, U6-ch28, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	80
Mean	37.2
Std Dev	3.572

**Gaus mean : 37.3365**  
**Gaus Width: 3.8355**



# B0L001S, U6-ch28, adc2

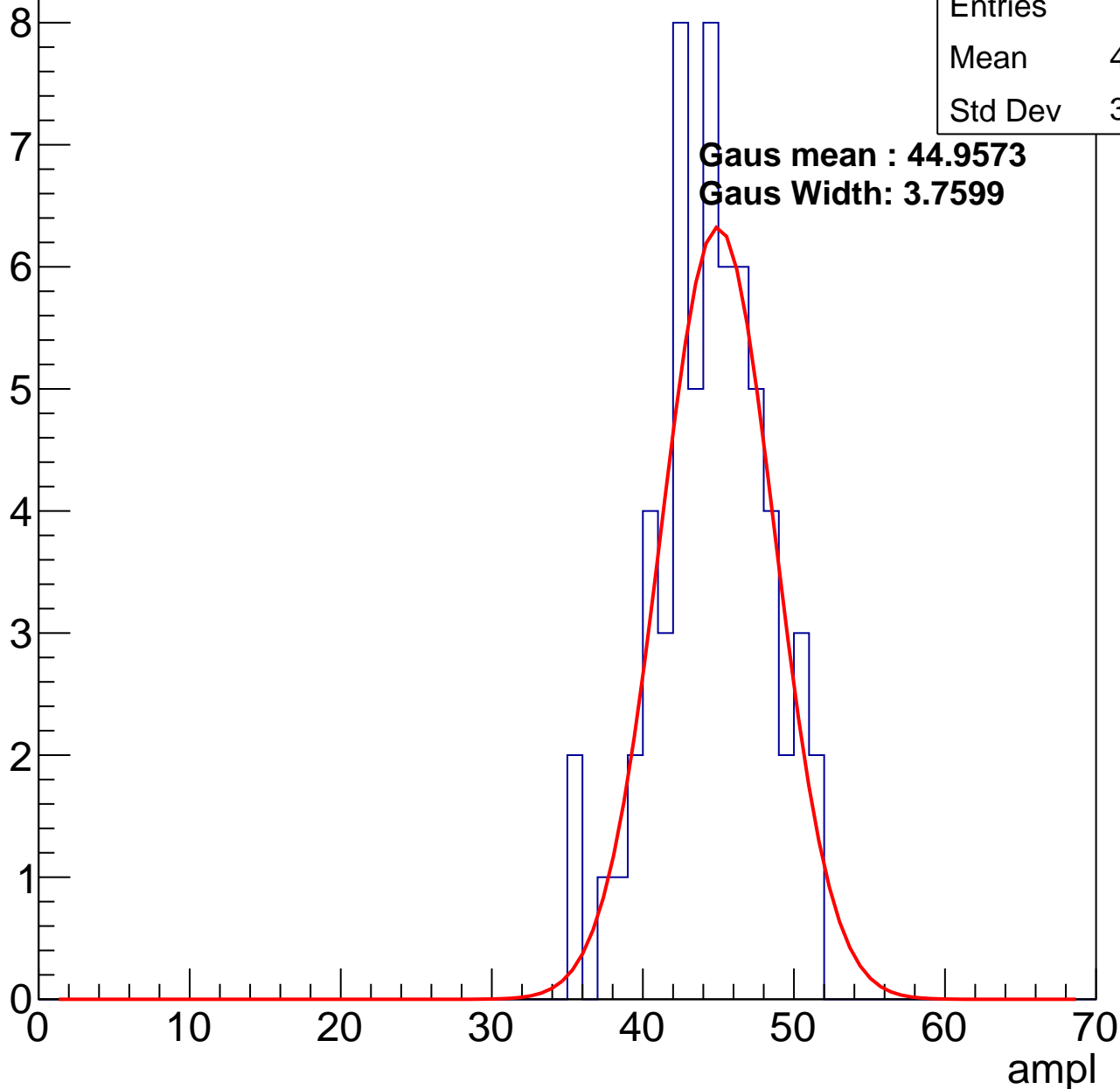
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	44.06
Std Dev	3.636

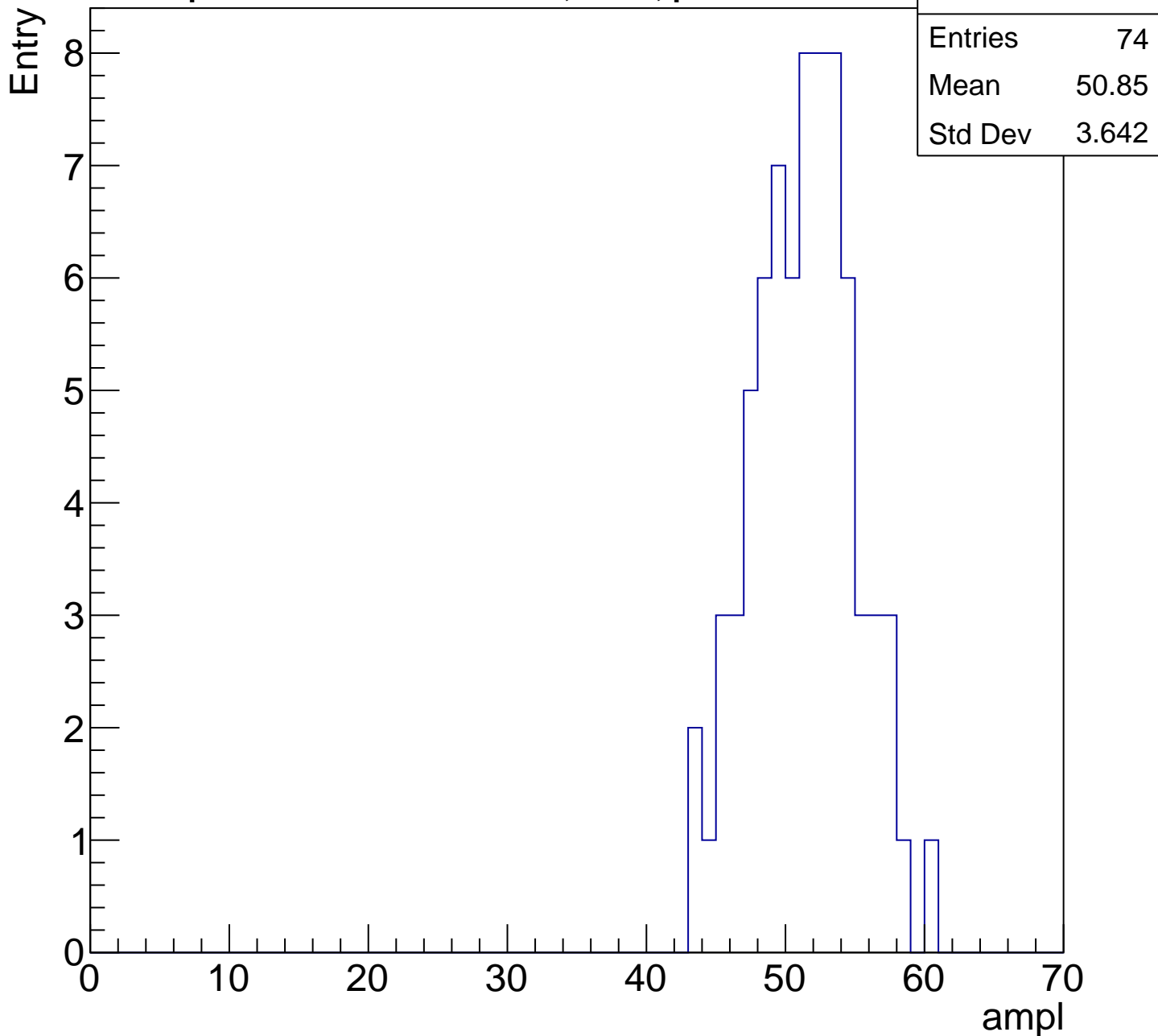
**Gaus mean : 44.9573**

**Gaus Width: 3.7599**



# B0L001S, U6-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

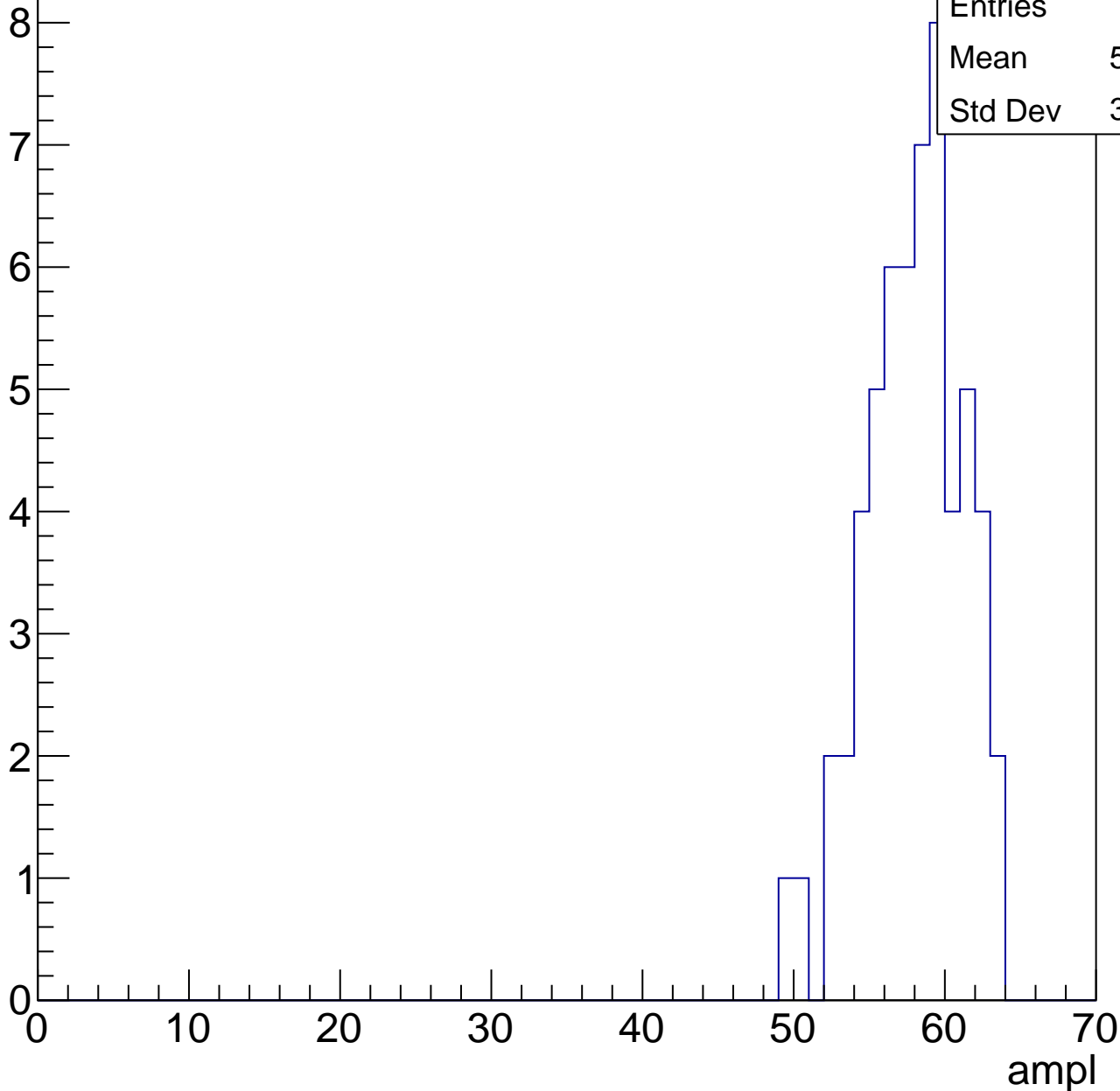


# B0L001S, U6-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	57.46
Std Dev	3.168

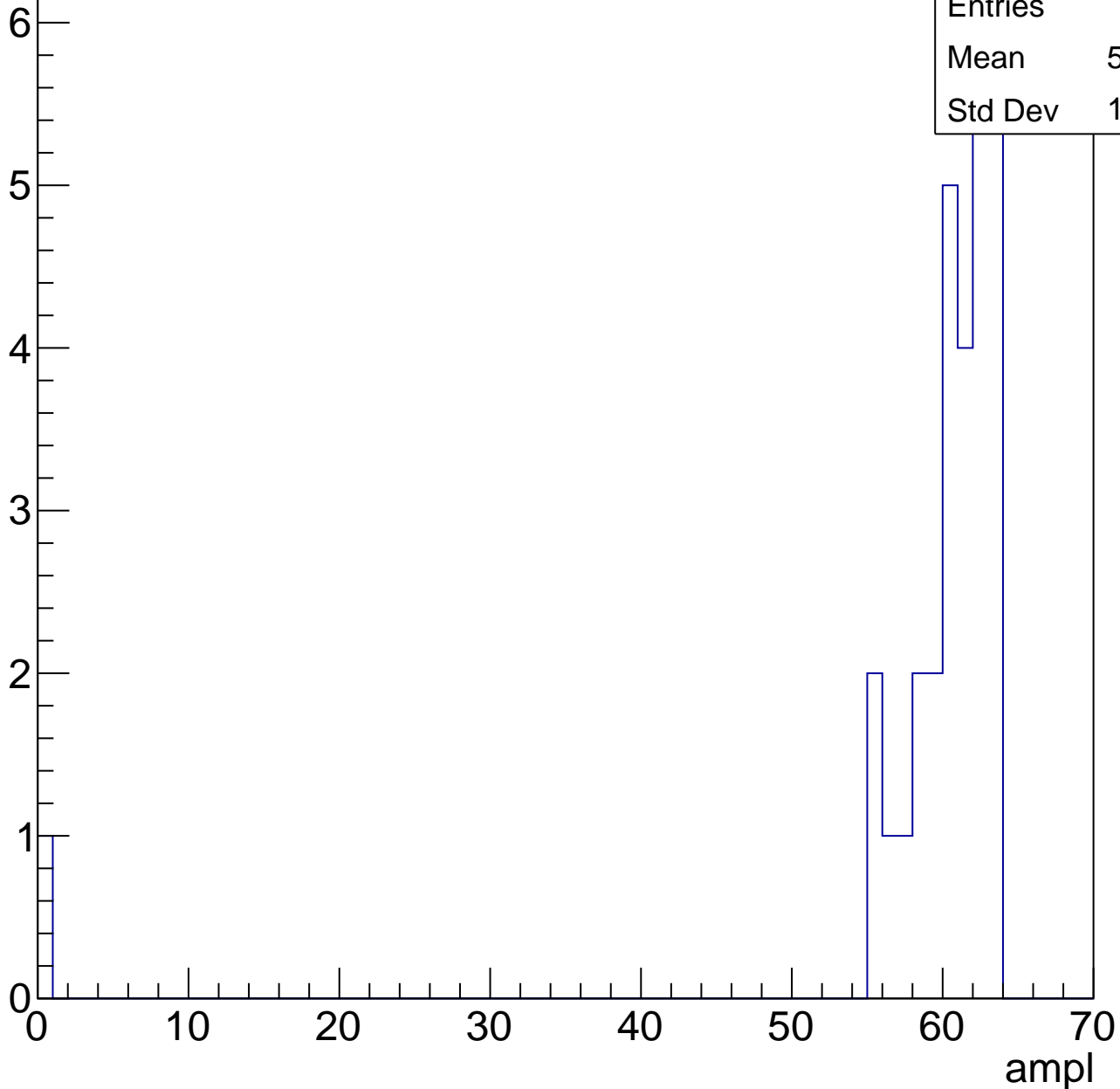


# B0L001S, U6-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	30
Mean	58.37
Std Dev	11.09



# B0L001S, U6-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch29, adc0

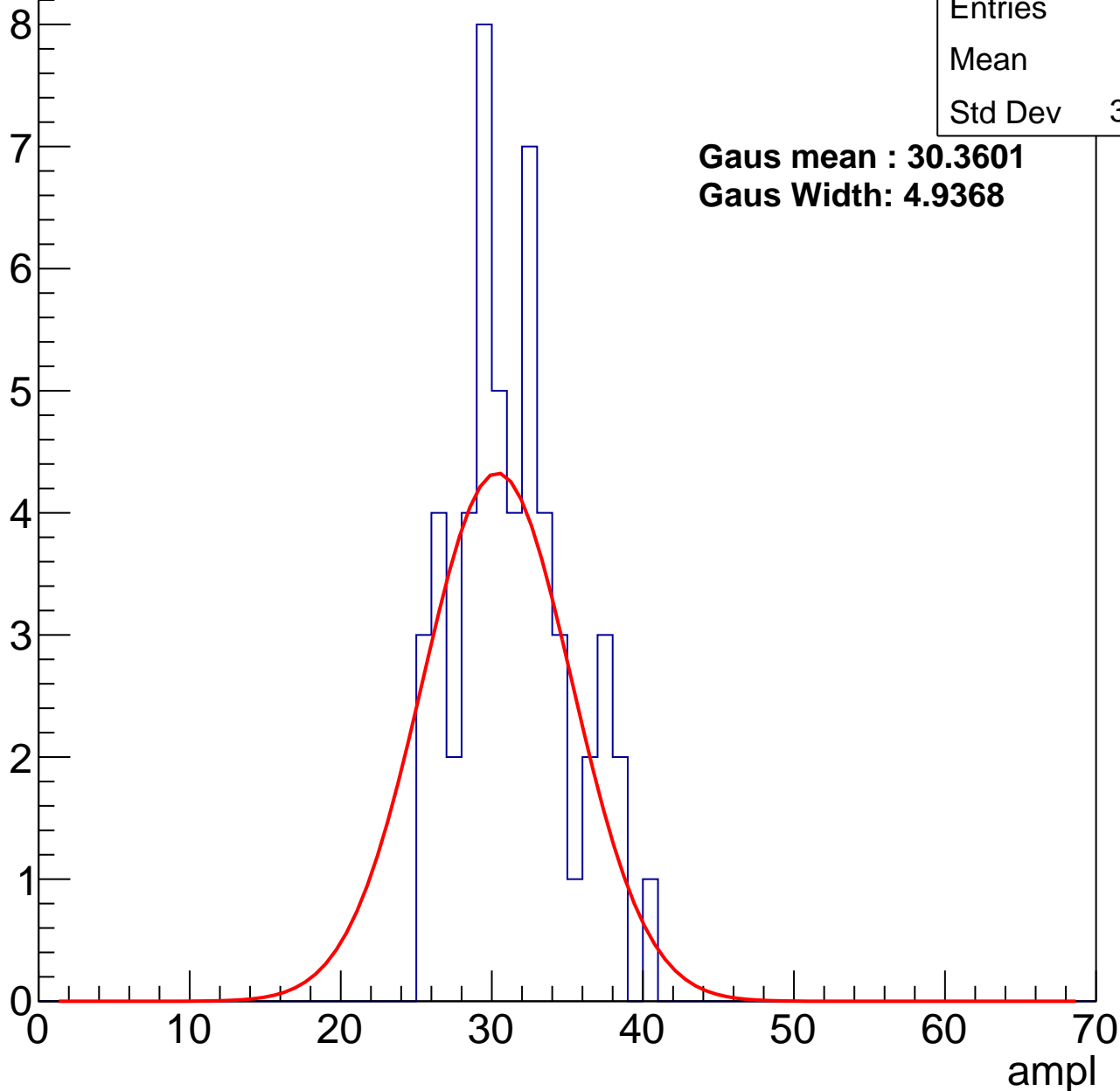
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	31
Std Dev	3.676

**Gaus mean : 30.3601**

**Gaus Width: 4.9368**



# B0L001S, U6-ch29, adc1

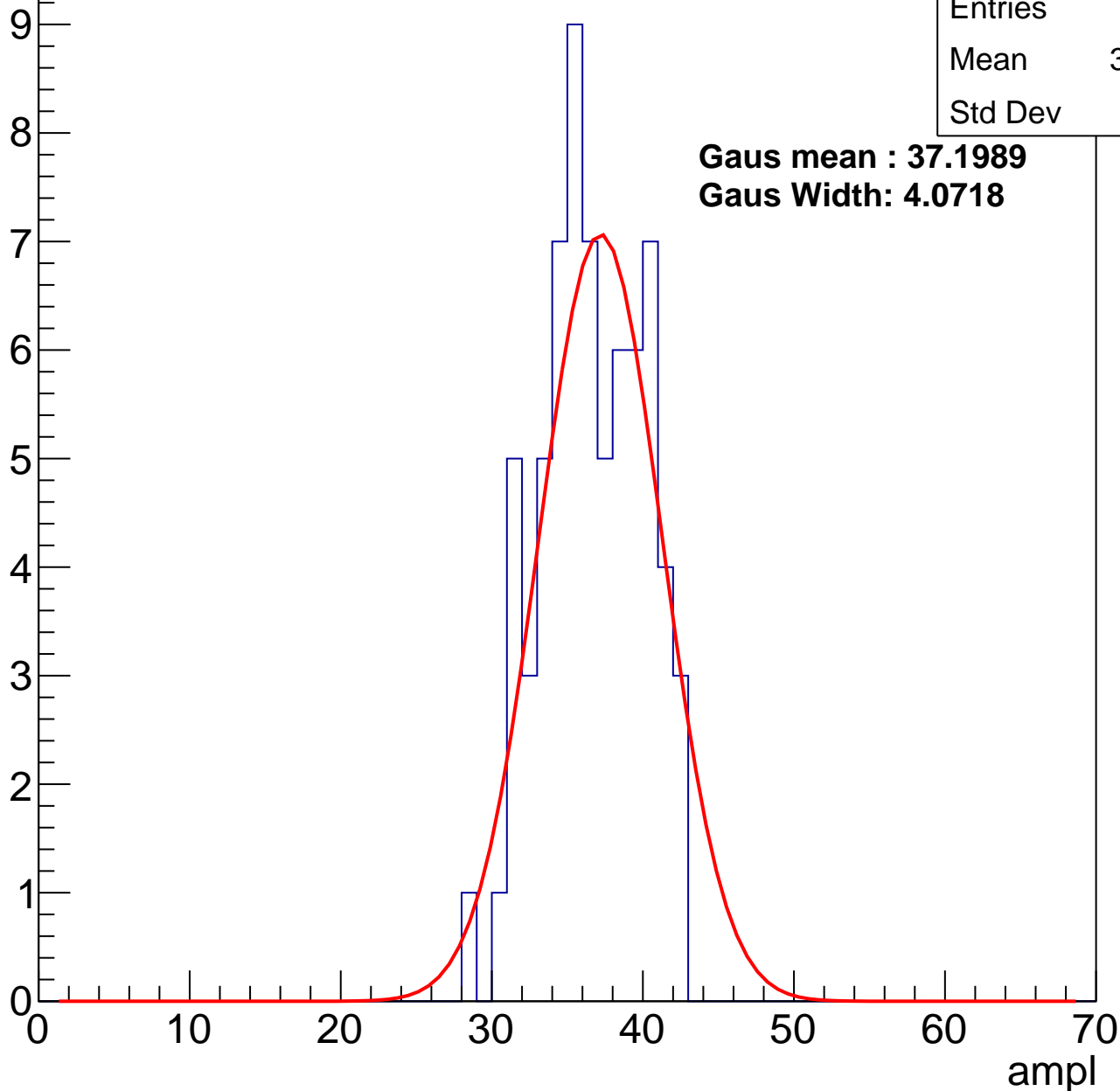
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	36.17
Std Dev	3.31

**Gaus mean : 37.1989**

**Gaus Width: 4.0718**



# B0L001S, U6-ch29, adc2

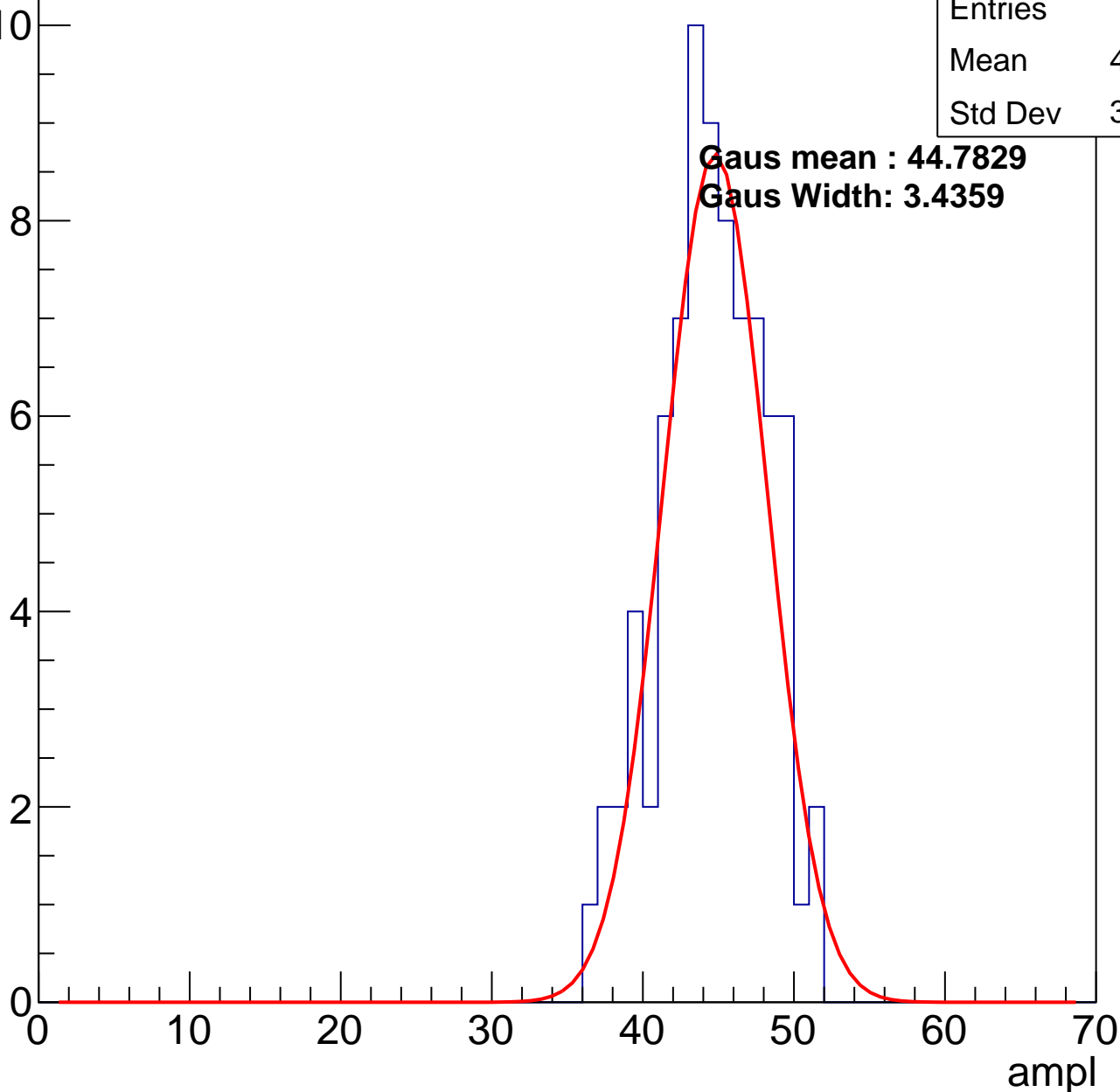
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	80
Mean	44.16
Std Dev	3.418

**Gaus mean : 44.7829**

**Gaus Width: 3.4359**

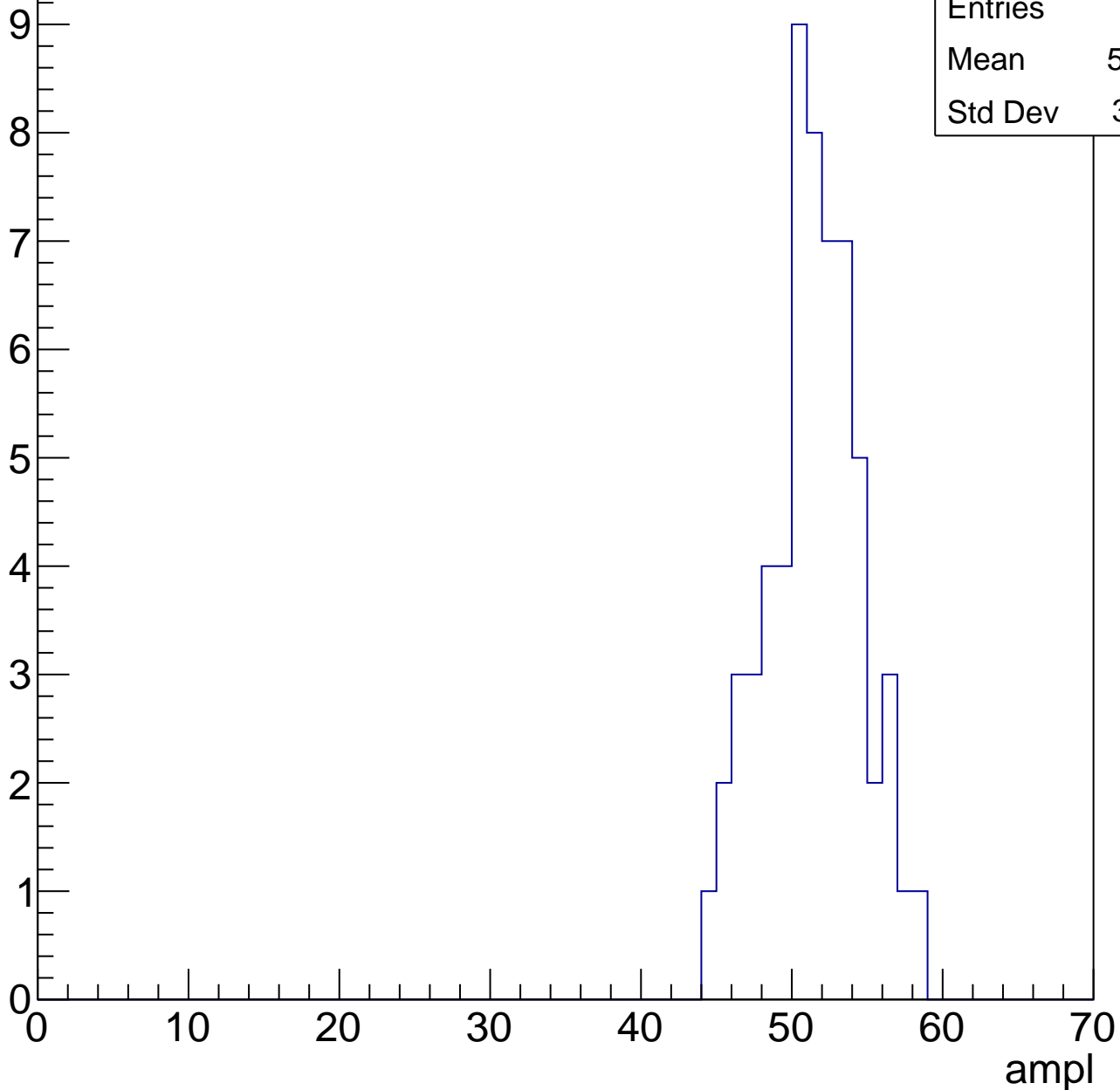


# B0L001S, U6-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	50.95
Std Dev	3.101

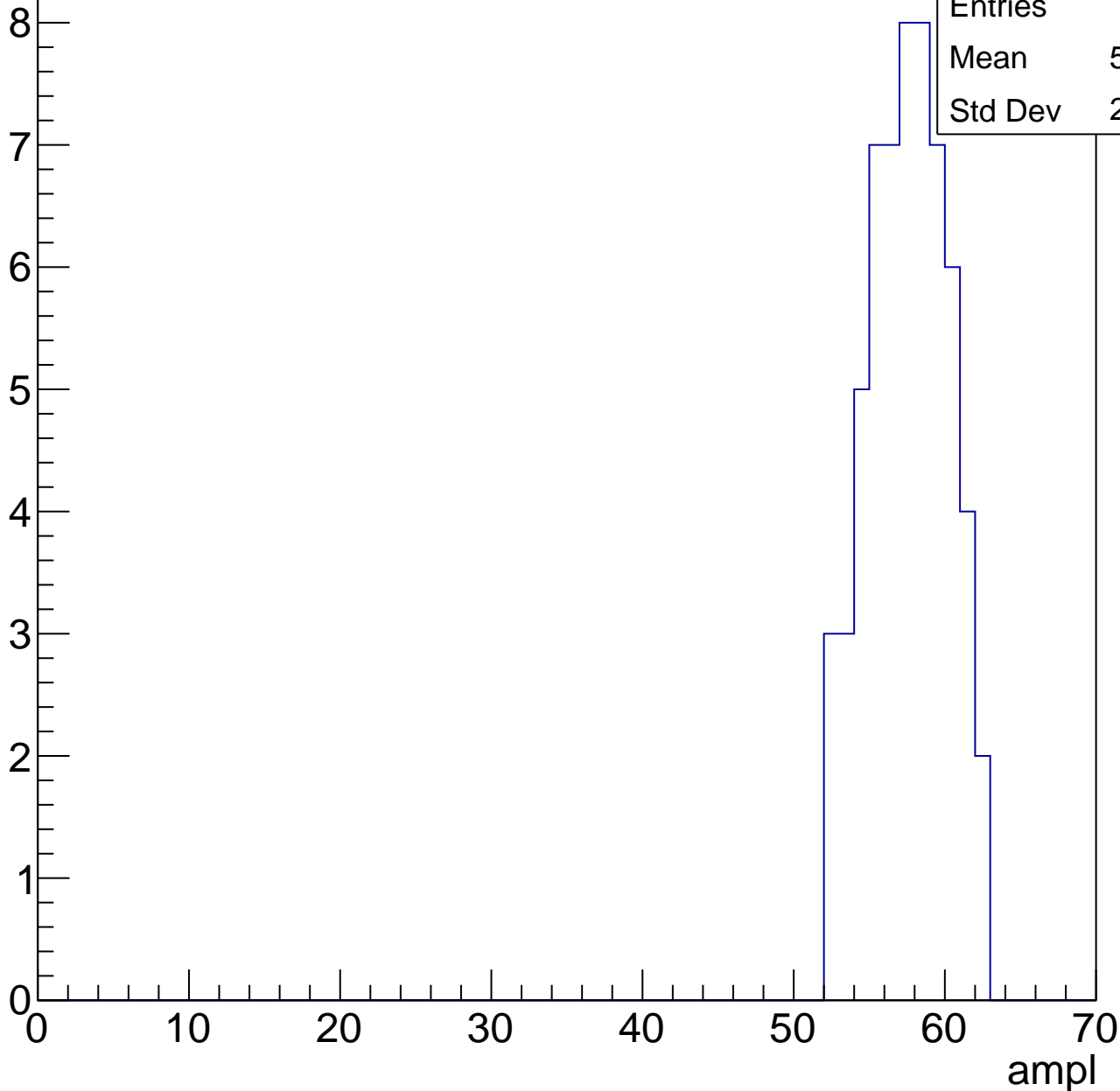


# B0L001S, U6-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	57.05
Std Dev	2.604



# B0L001S, U6-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

Entries	35
Mean	59.4
Std Dev	10.36

0

2

4

6

8

10

# B0L001S, U6-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U6-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch30, adc0

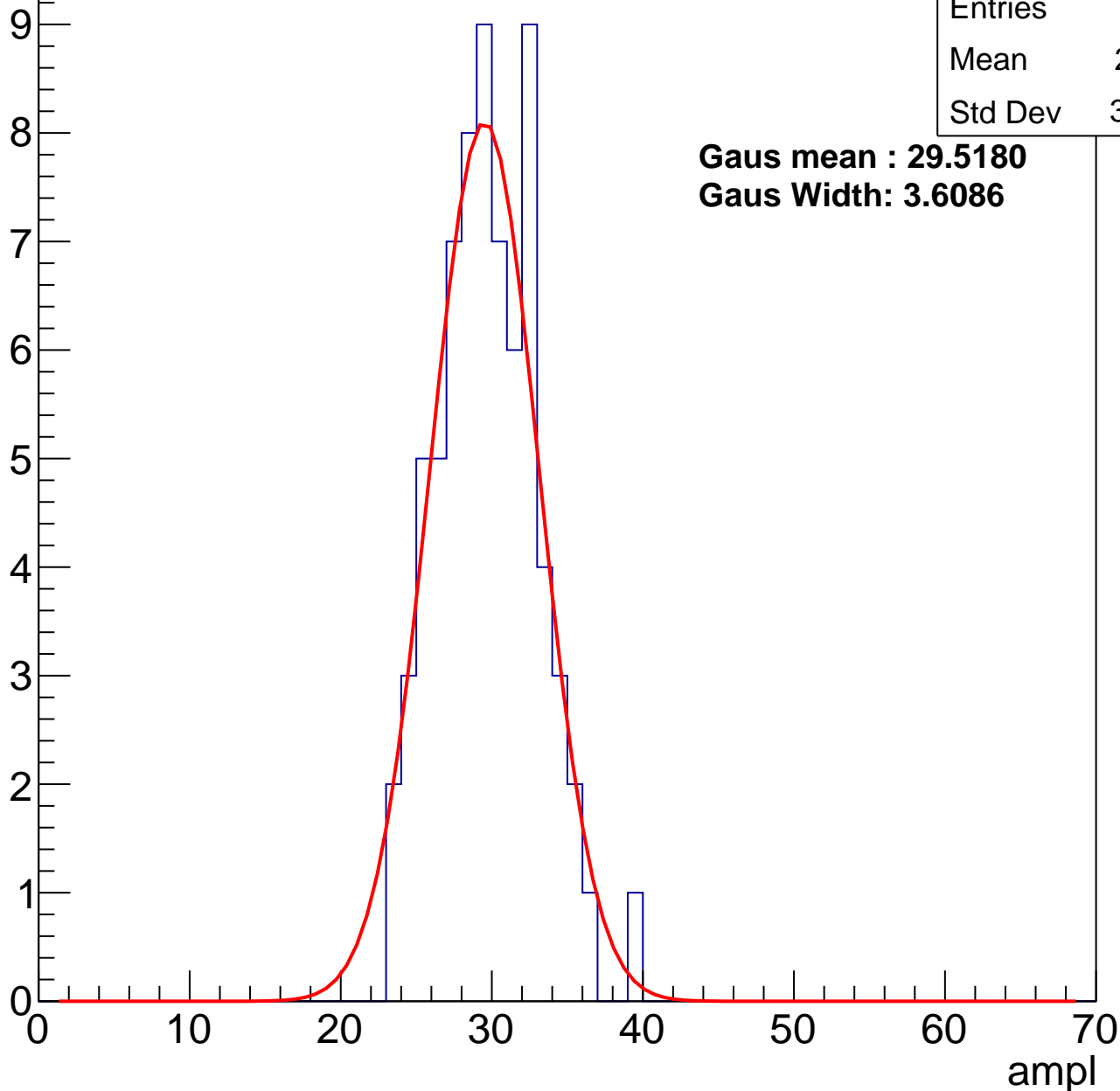
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	29.31
Std Dev	3.277

**Gaus mean : 29.5180**

**Gaus Width: 3.6086**



# B0L001S, U6-ch30, adc1

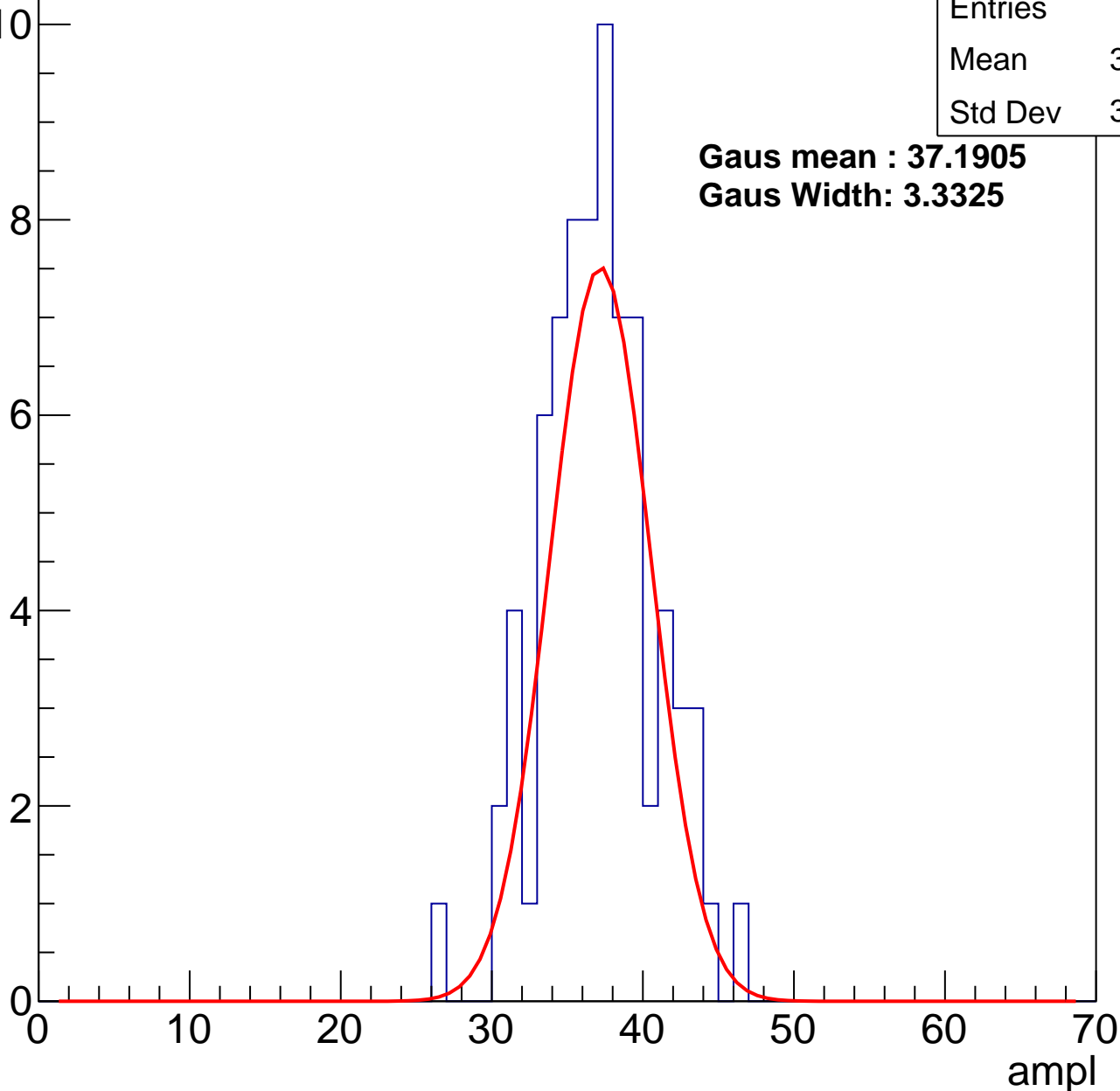
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	36.59
Std Dev	3.659

**Gaus mean : 37.1905**

**Gaus Width: 3.3325**



# B0L001S, U6-ch30, adc2

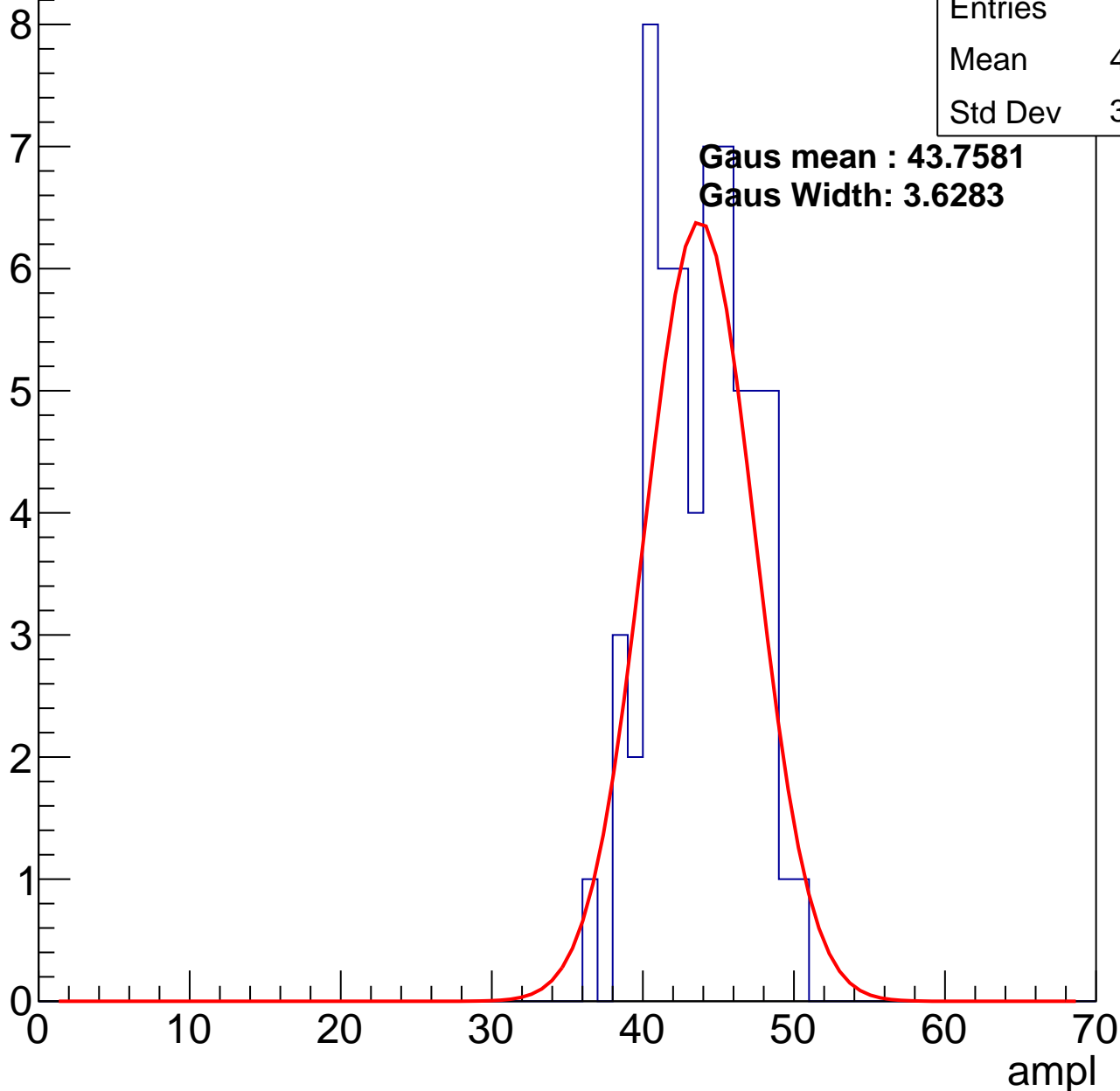
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	43.36
Std Dev	3.188

**Gaus mean : 43.7581**

**Gaus Width: 3.6283**

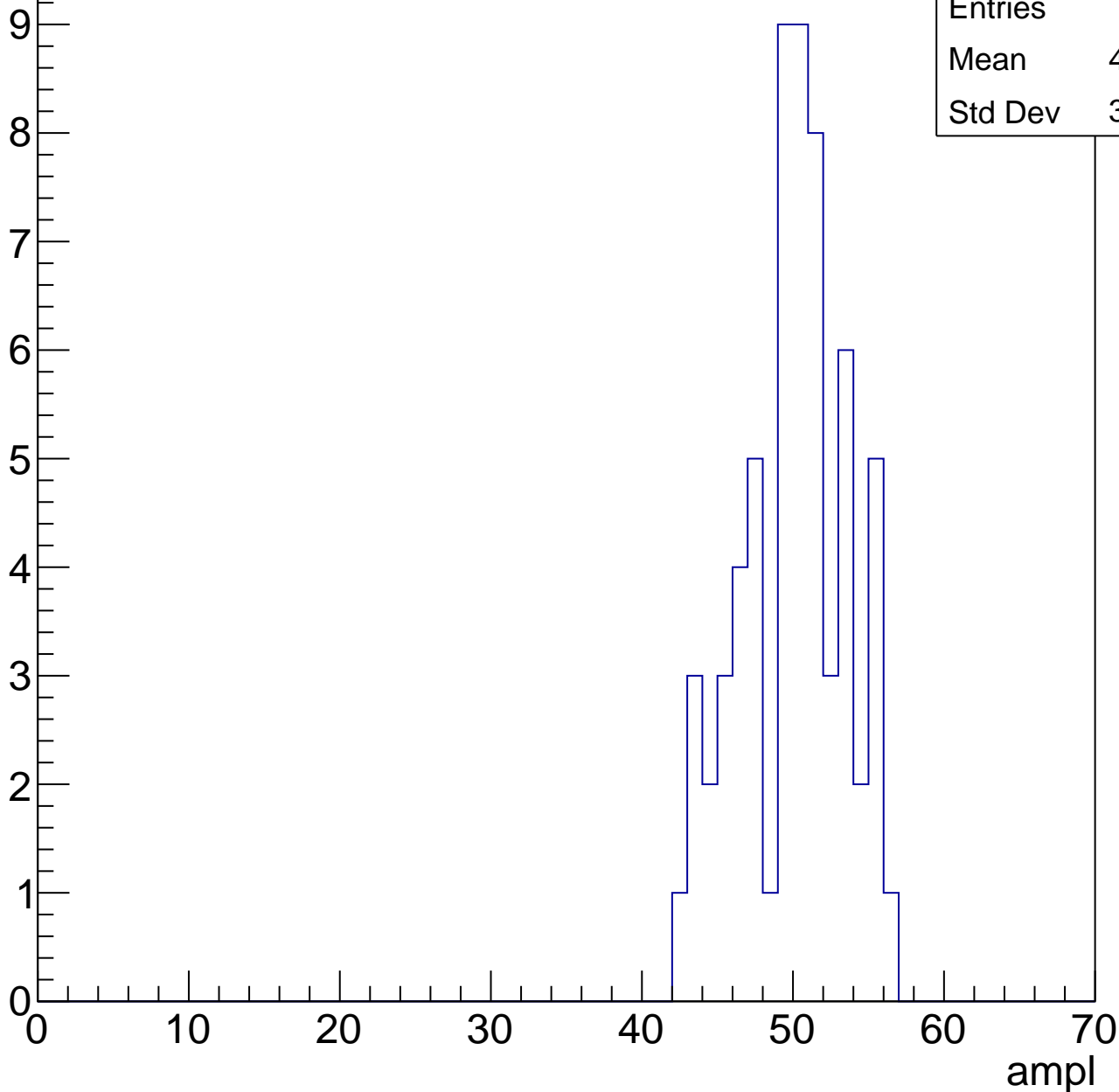


# B0L001S, U6-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	49.56
Std Dev	3.444

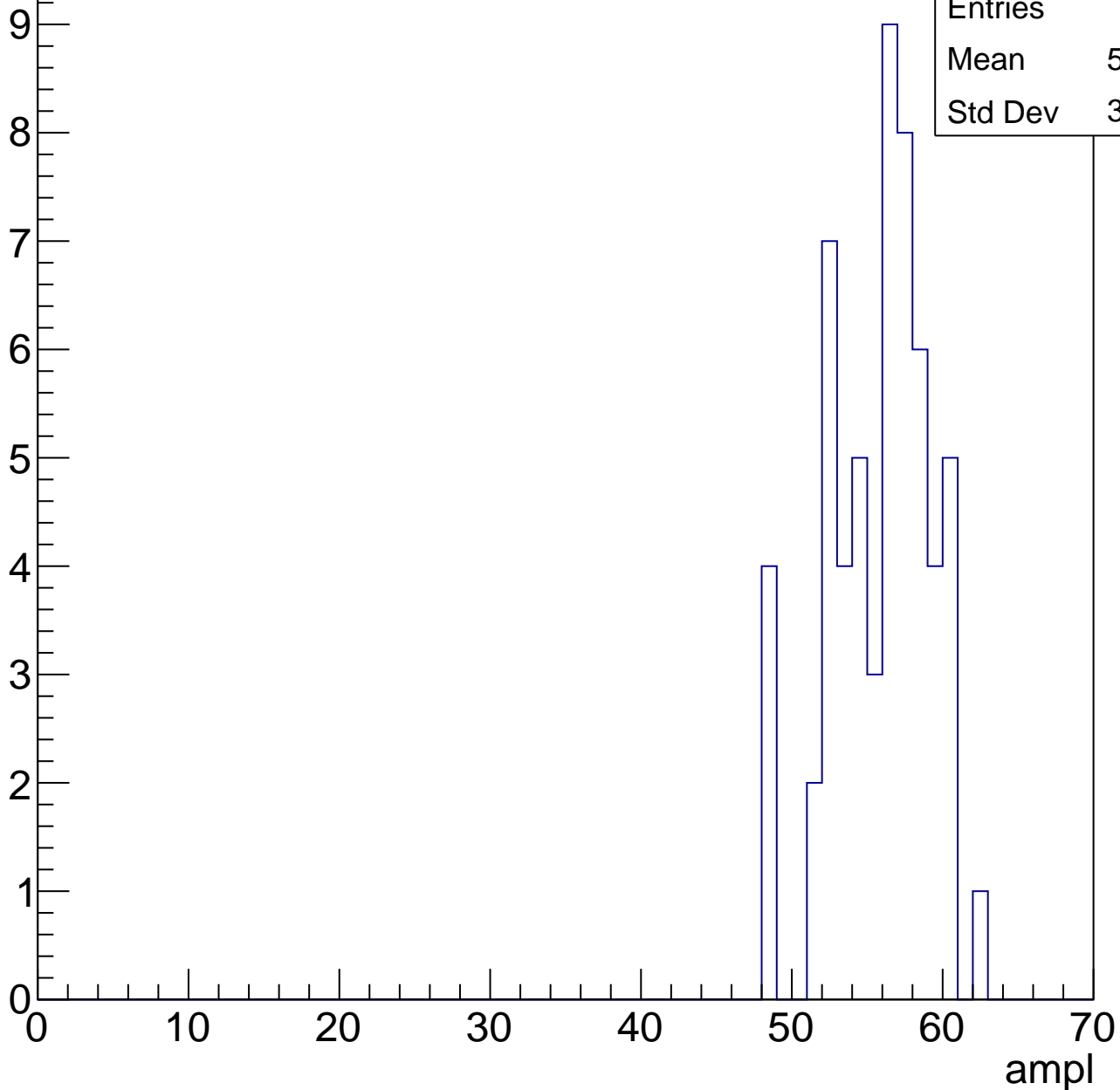


# B0L001S, U6-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	55.36
Std Dev	3.315

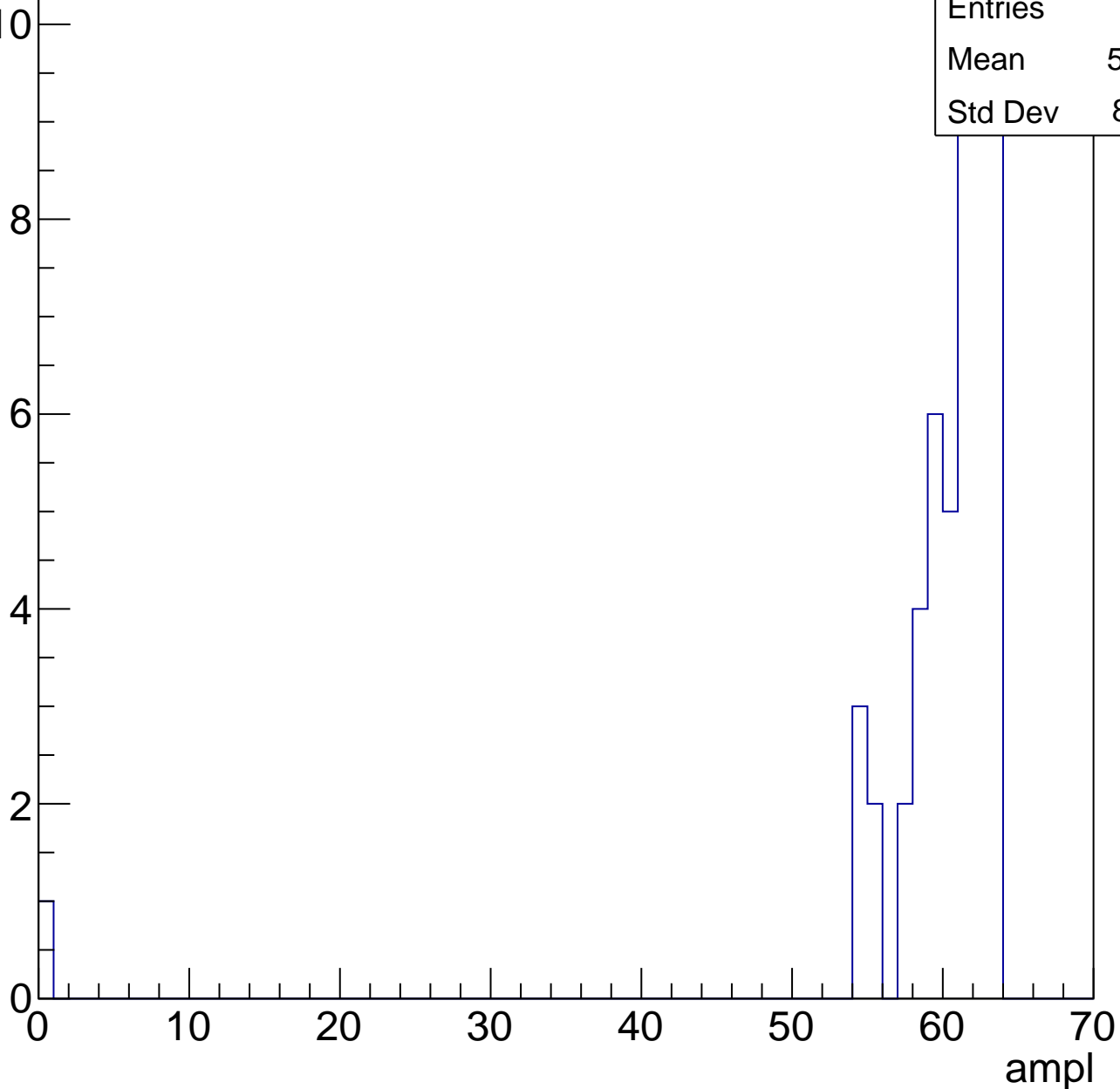


# B0L001S, U6-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	58.96
Std Dev	8.711



# B0L001S, U6-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch31, adc0

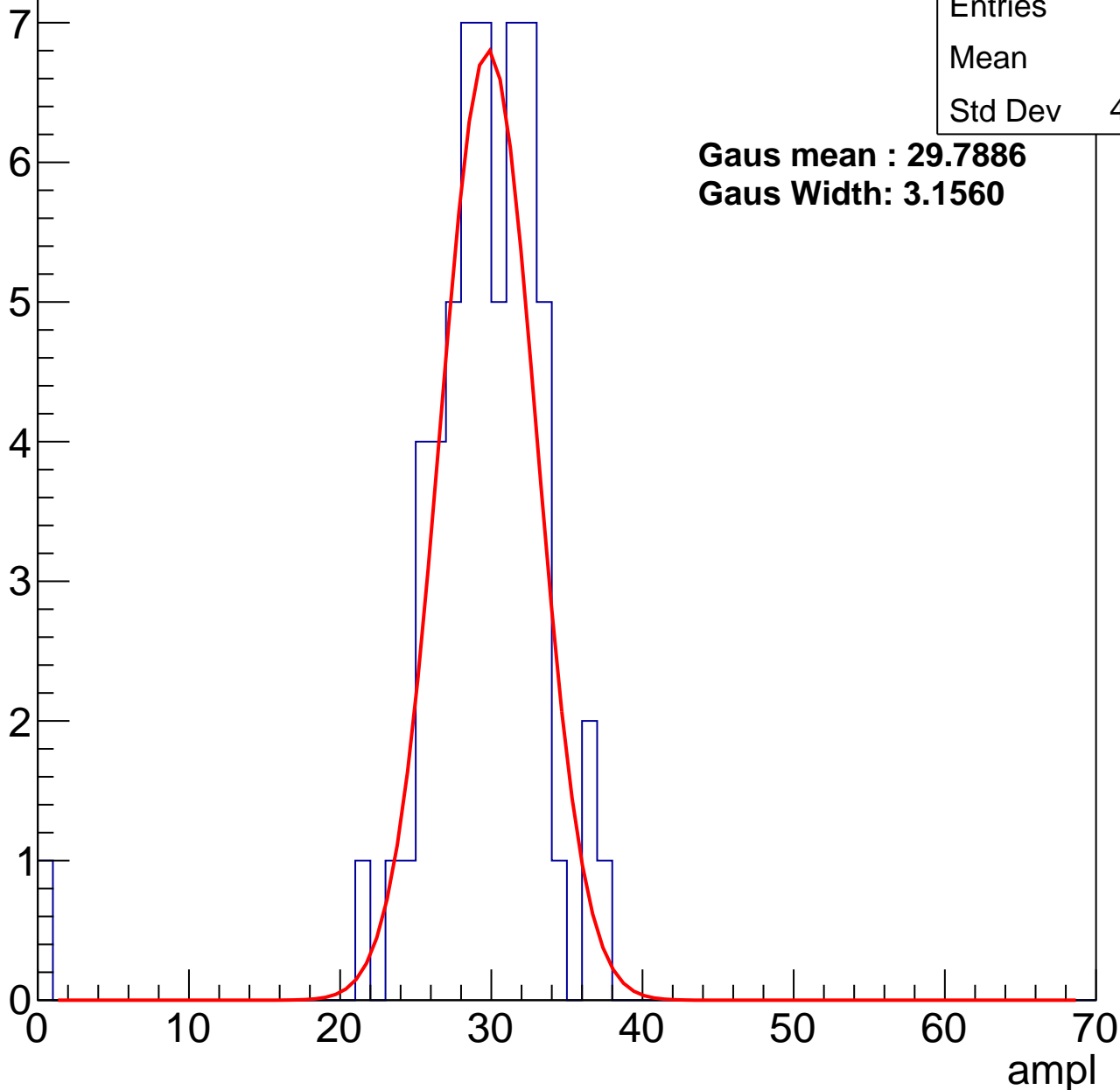
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	28.9
Std Dev	4.967

**Gaus mean : 29.7886**

**Gaus Width: 3.1560**



# B0L001S, U6-ch31, adc1

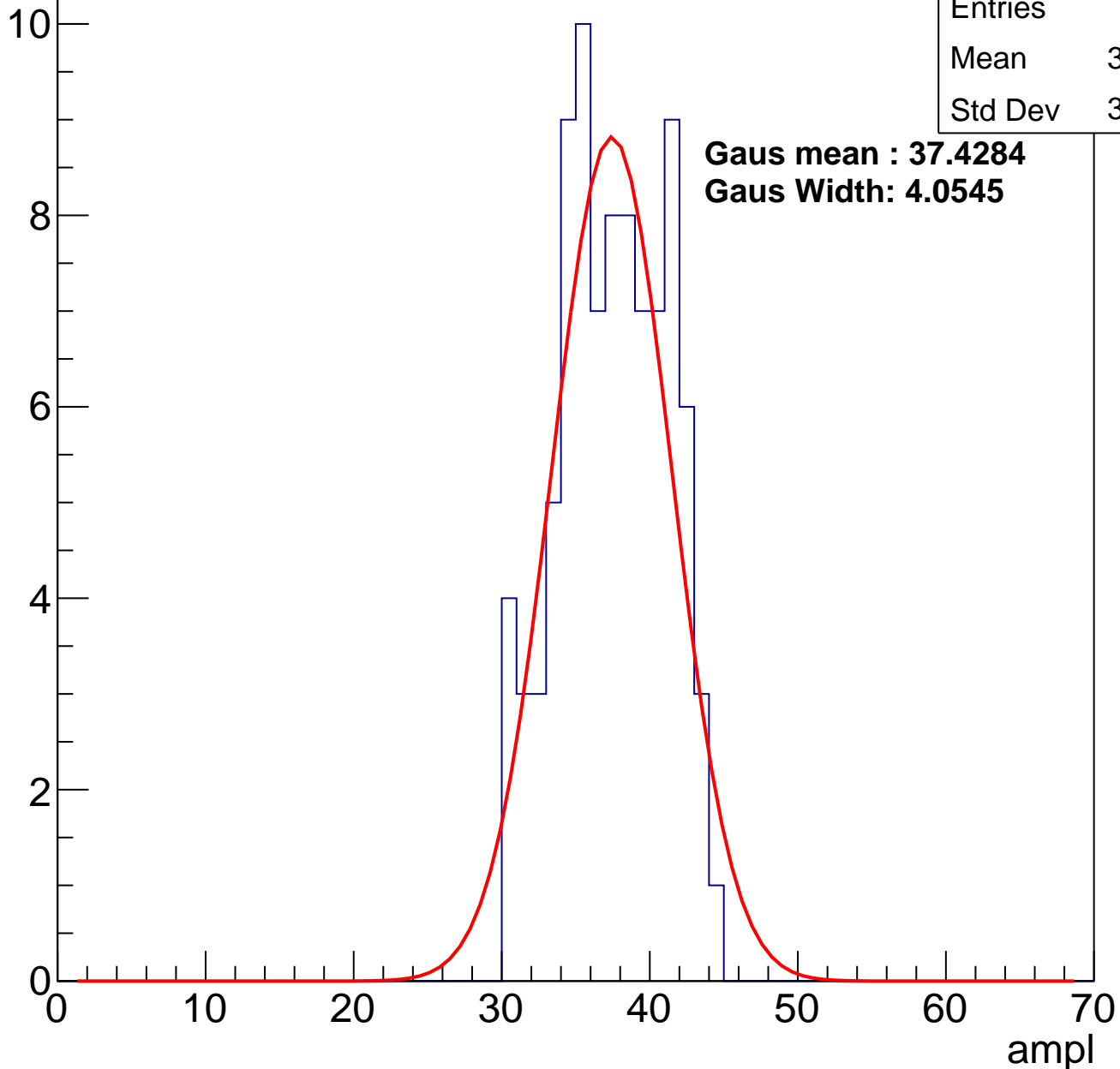
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	90
Mean	36.99
Std Dev	3.554

**Gaus mean : 37.4284**

**Gaus Width: 4.0545**

Entry

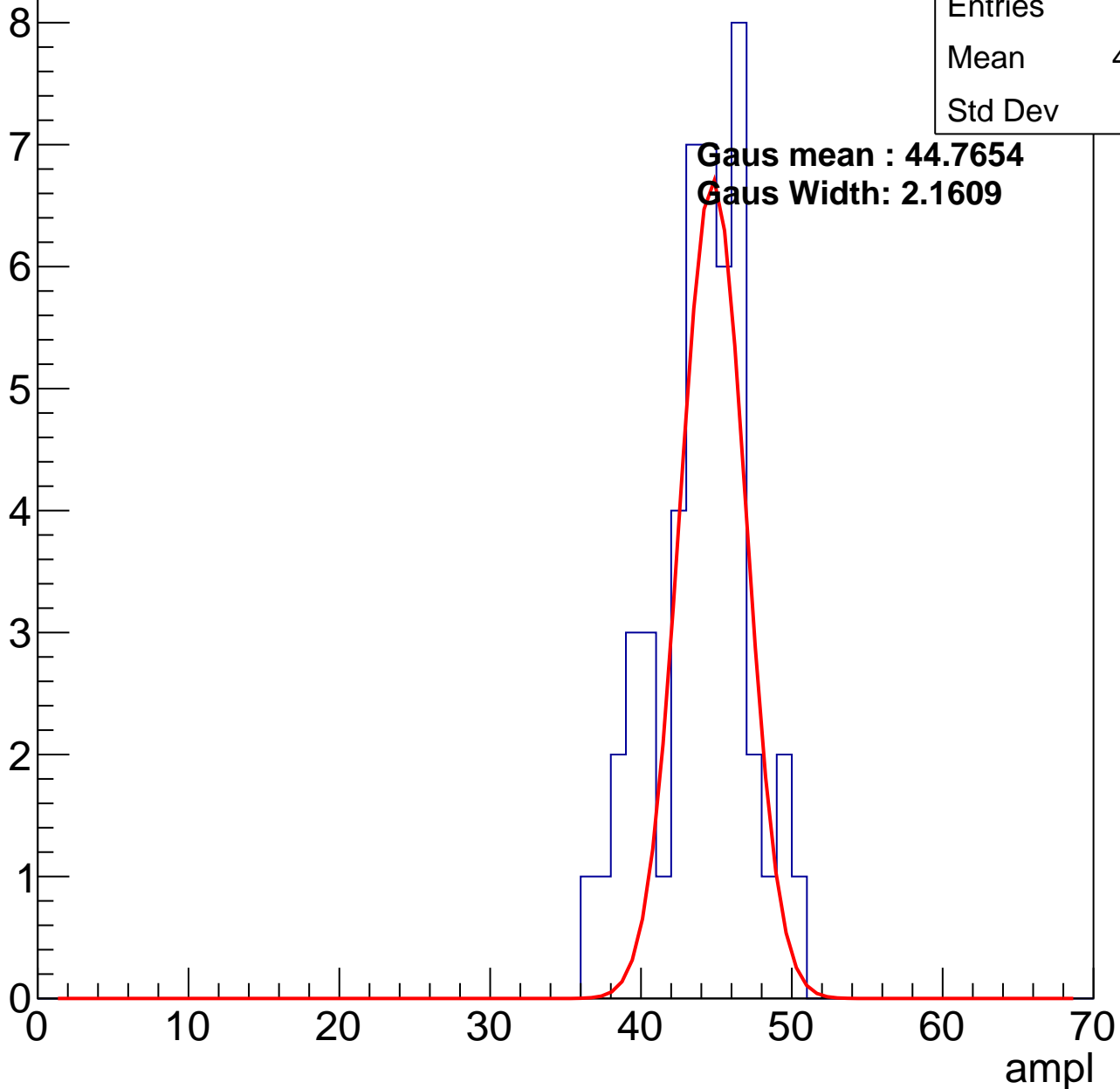


# B0L001S, U6-ch31, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	43.51
Std Dev	3.15



# B0L001S, U6-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

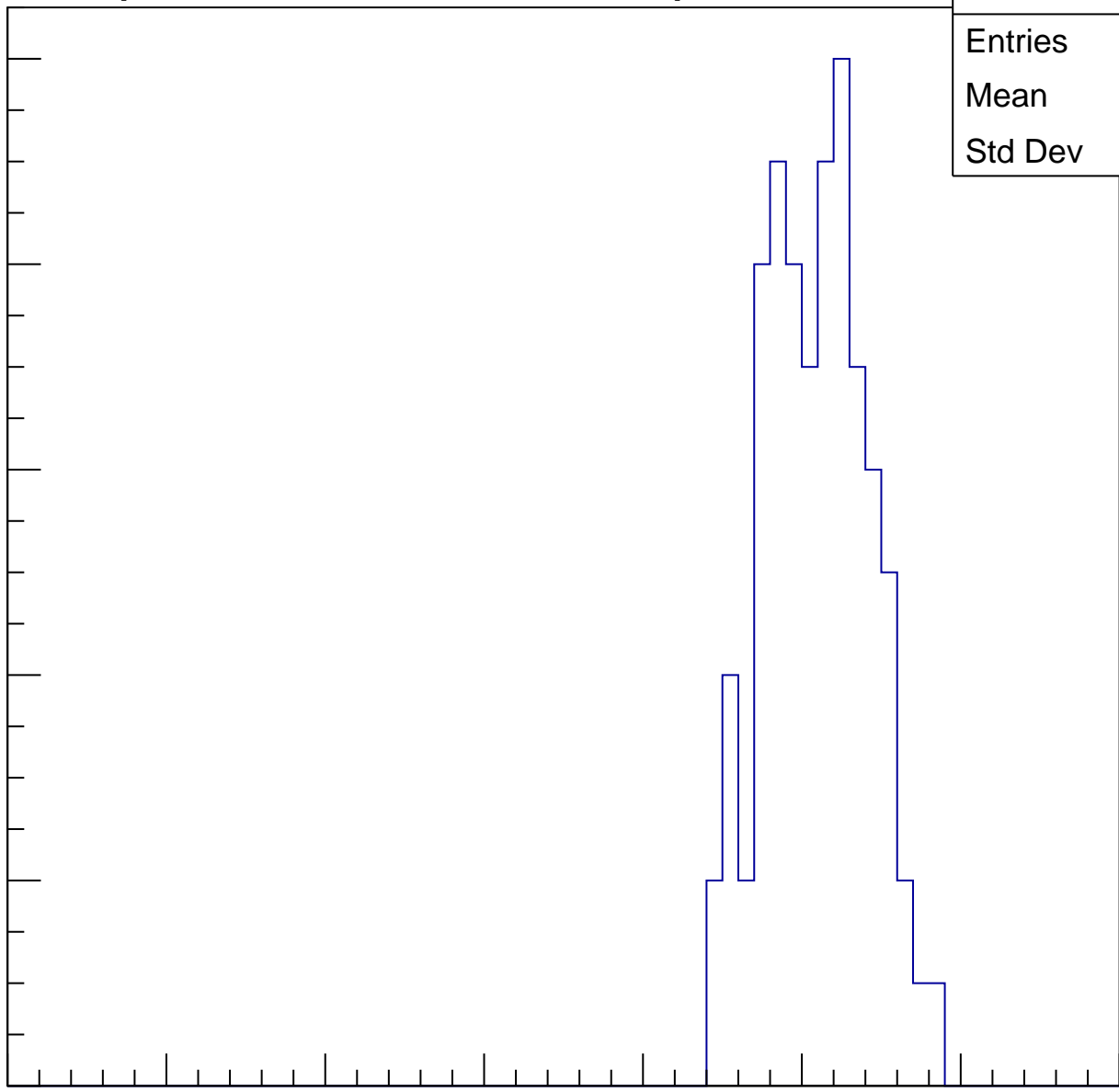
Entries	81
Mean	50.44
Std Dev	3.186

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

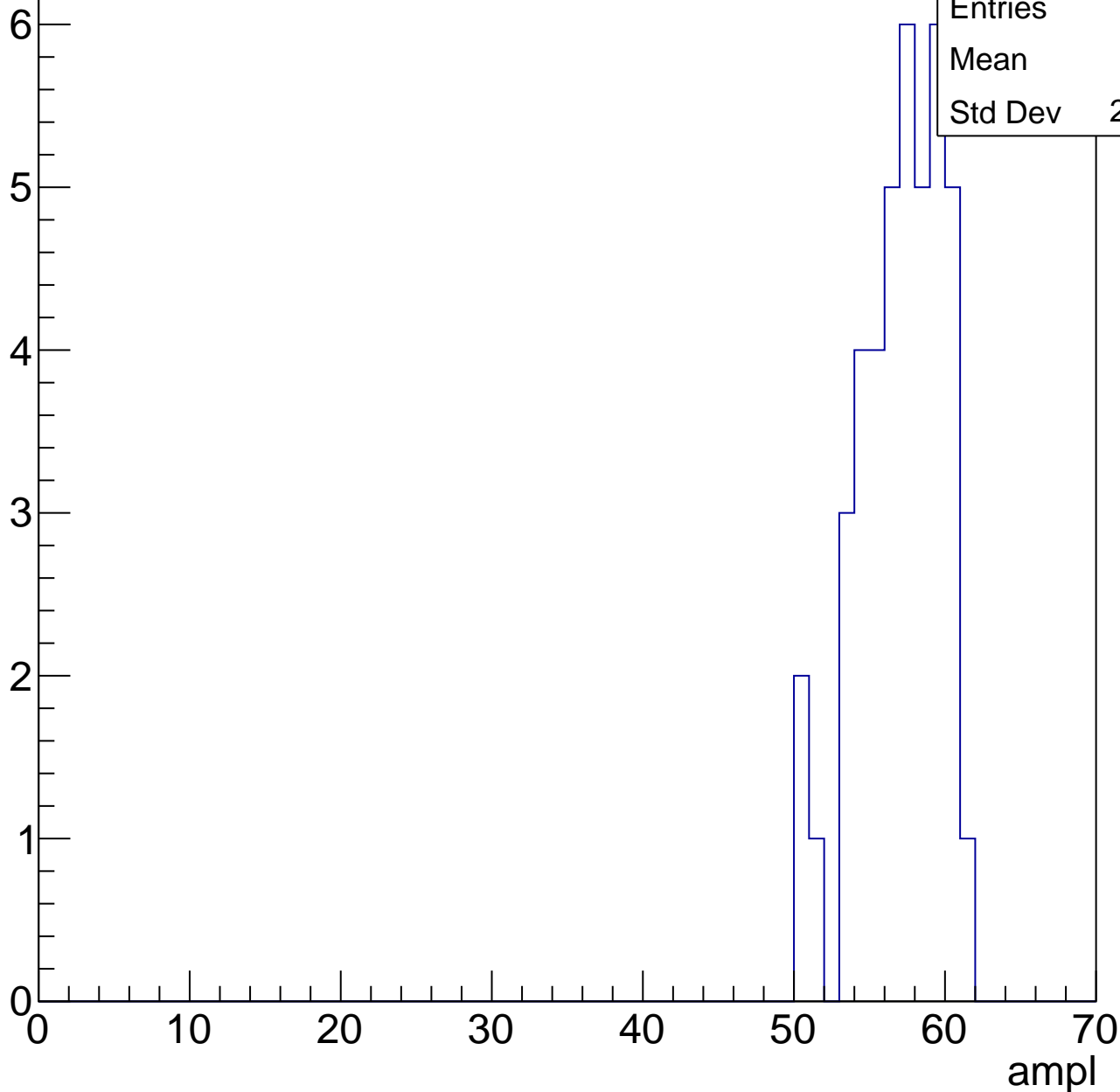


# B0L001S, U6-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	42
Mean	56.5
Std Dev	2.754

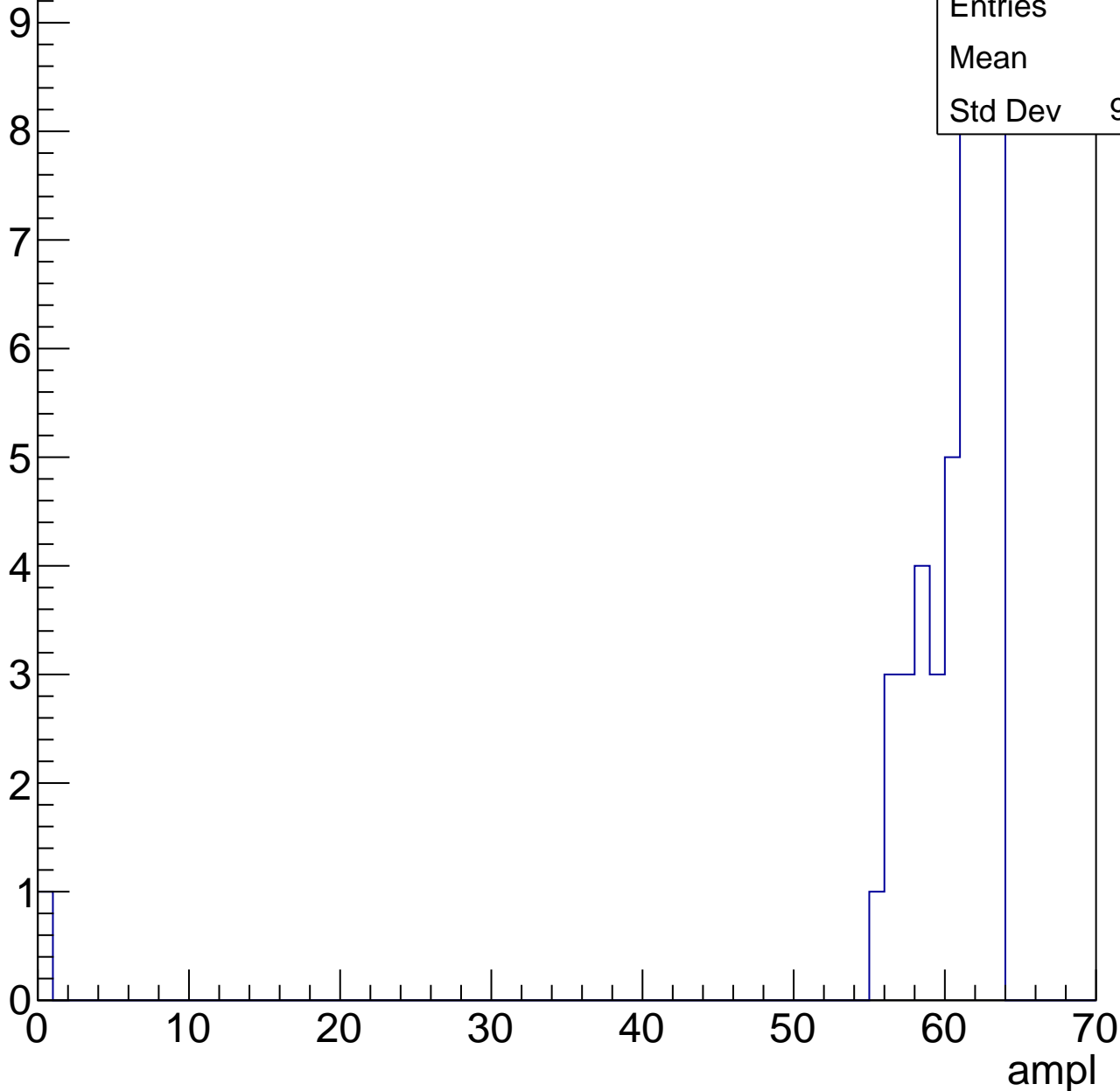


# B0L001S, U6-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	59
Std Dev	9.077



# B0L001S, U6-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U6-ch32, adc0

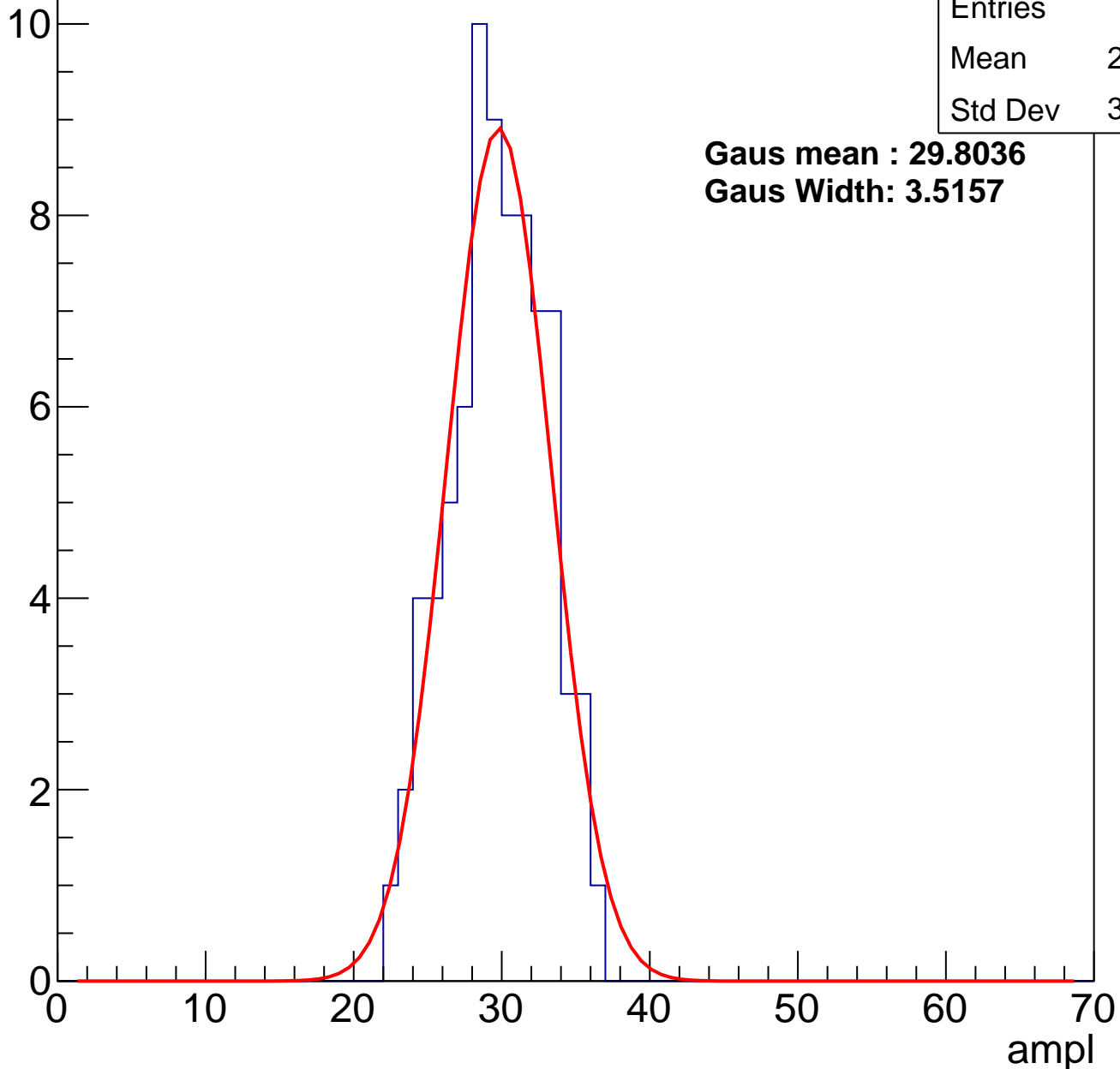
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	78
Mean	29.27
Std Dev	3.213

**Gaus mean : 29.8036**

**Gaus Width: 3.5157**

Entry



# B0L001S, U6-ch32, adc1

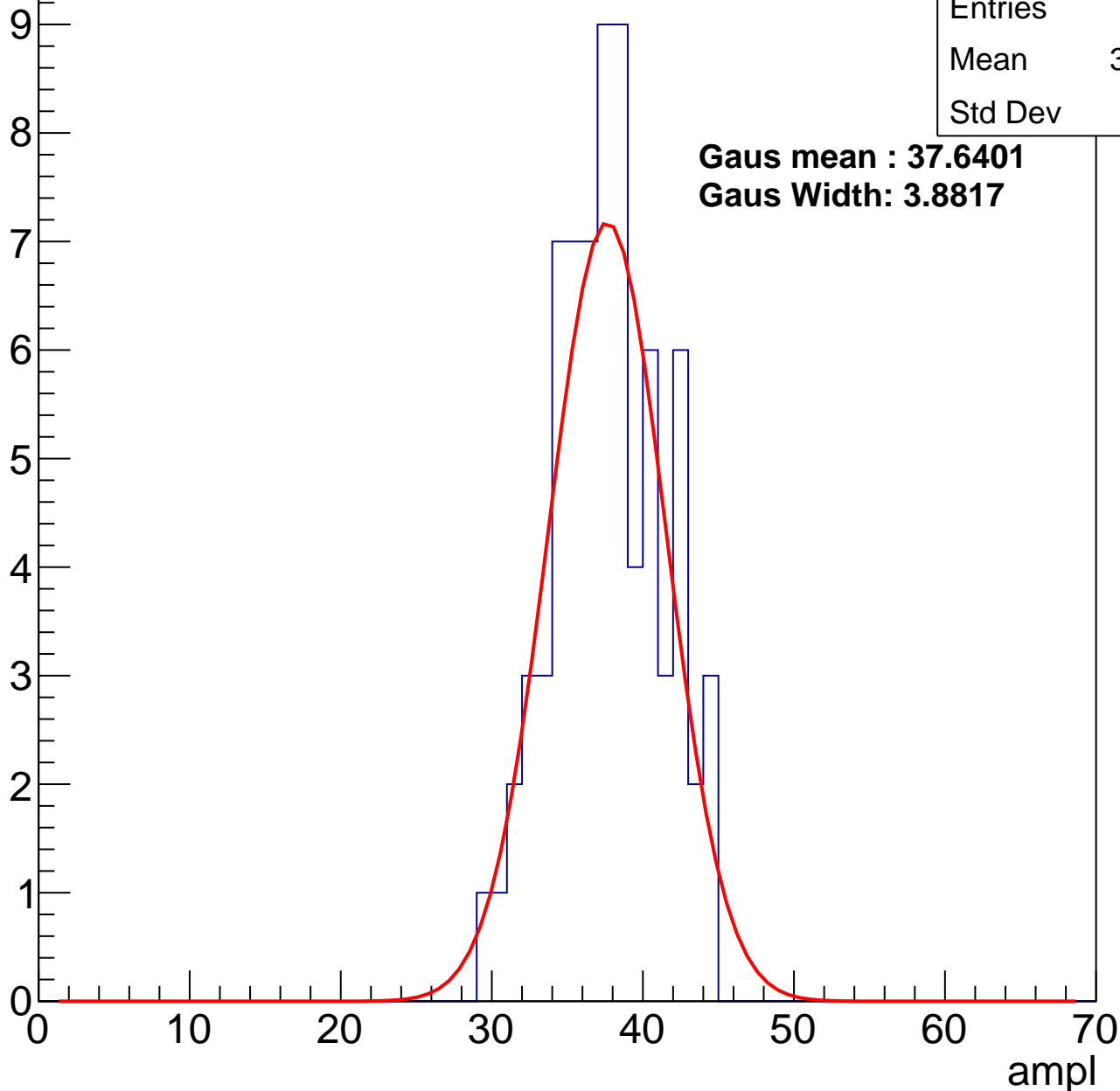
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	37.19
Std Dev	3.51

**Gaus mean : 37.6401**

**Gaus Width: 3.8817**



# B0L001S, U6-ch32, adc2

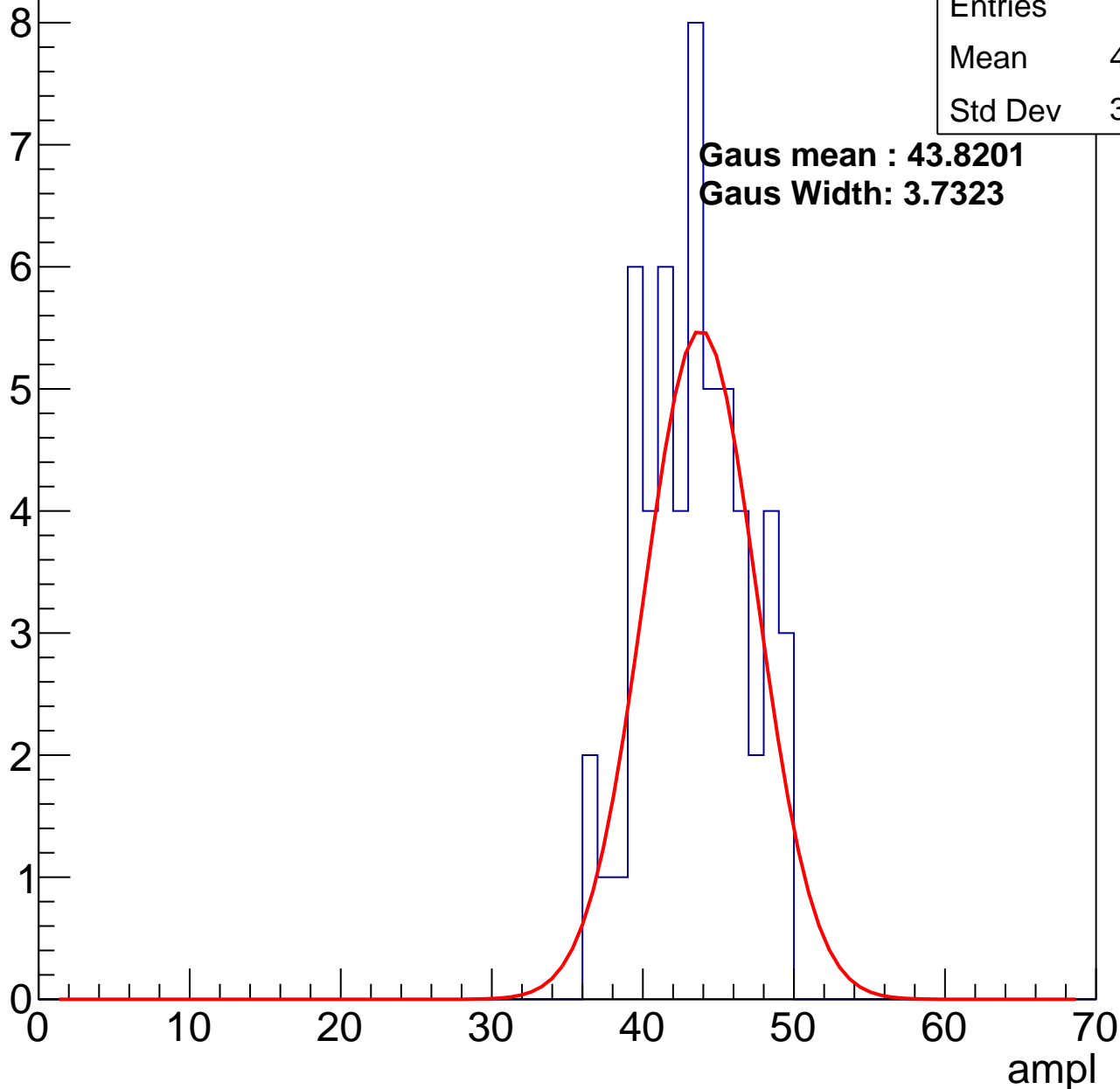
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	42.93
Std Dev	3.357

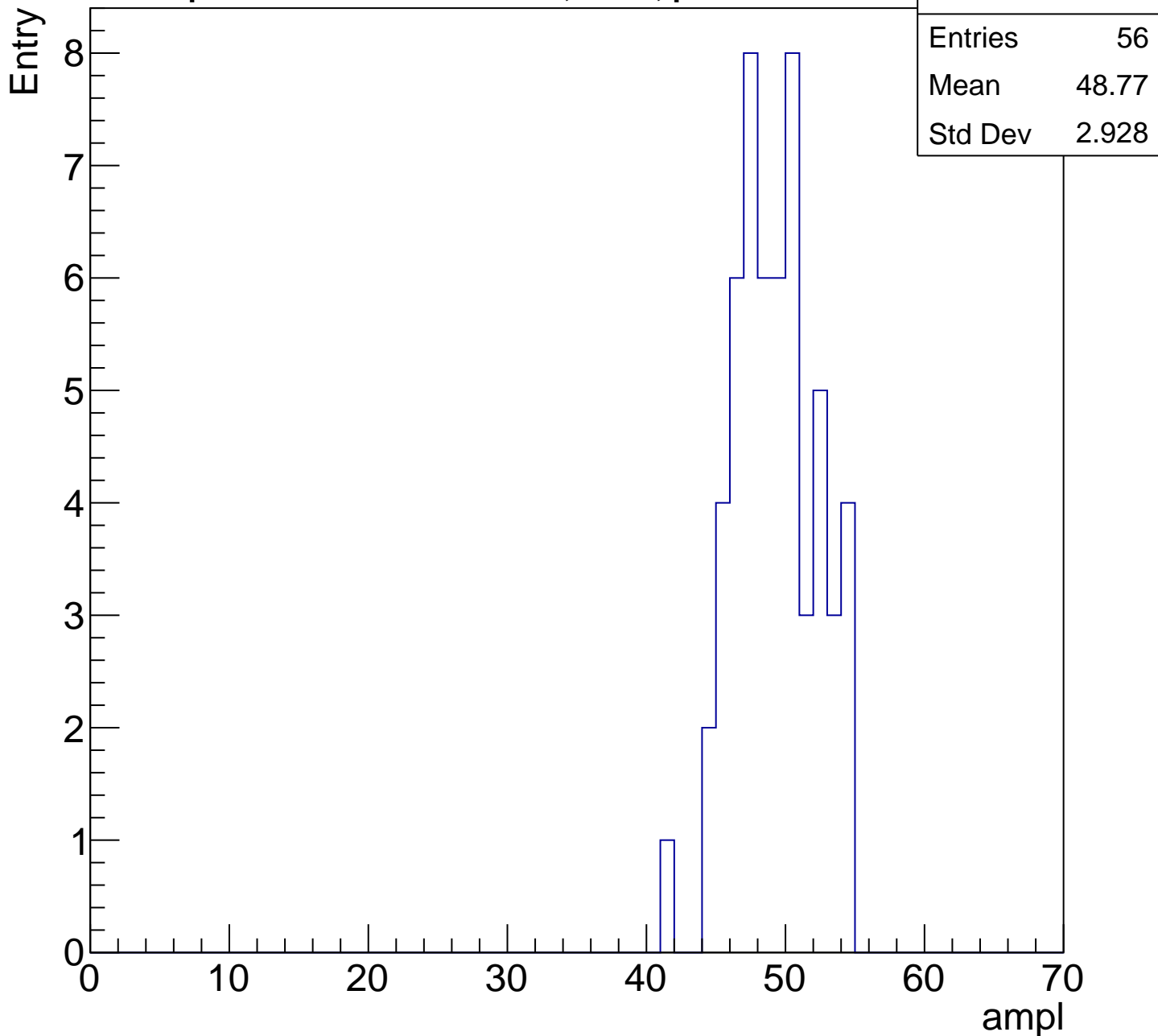
**Gaus mean : 43.8201**

**Gaus Width: 3.7323**



# B0L001S, U6-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

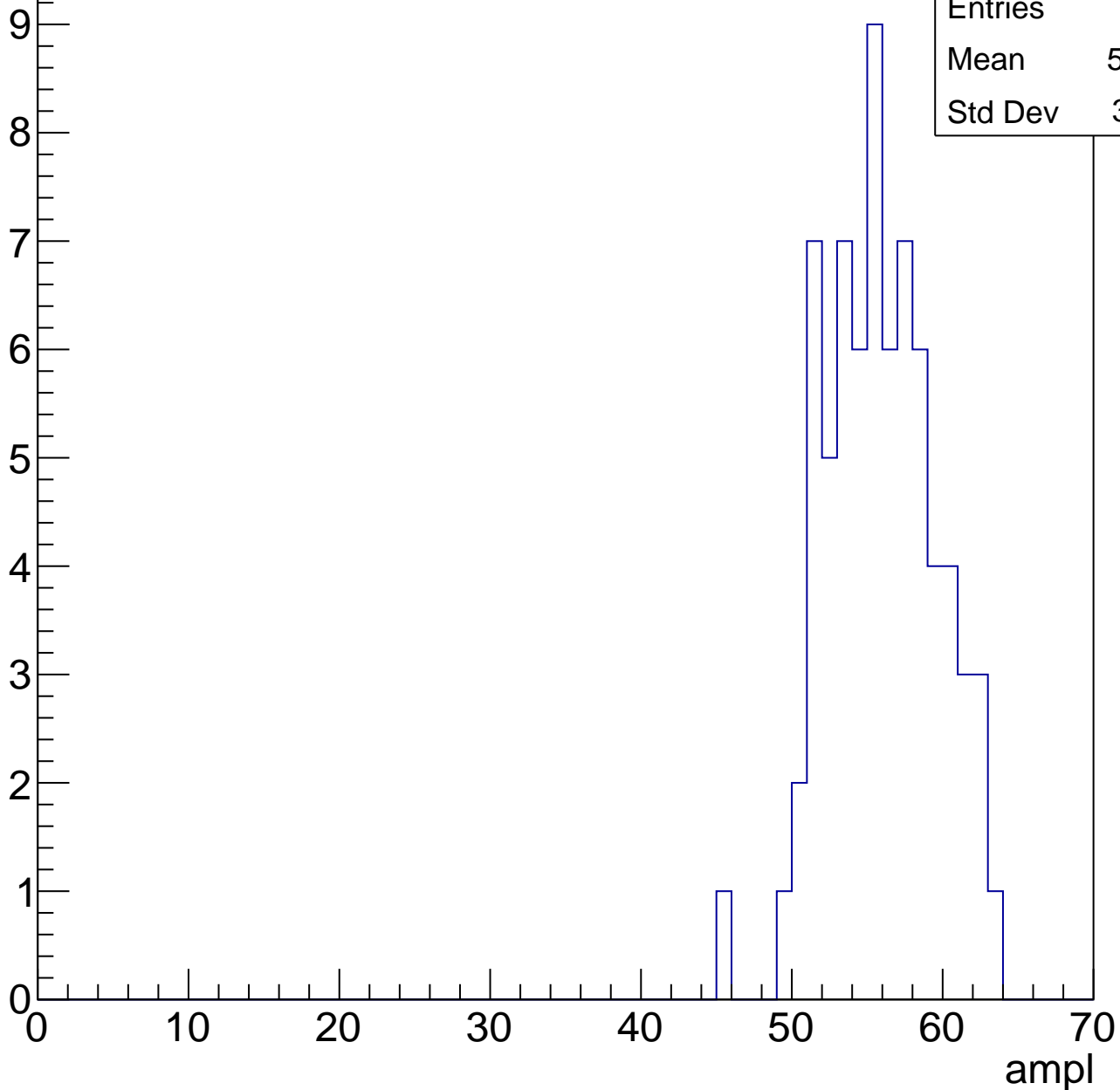


# B0L001S, U6-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	55.44
Std Dev	3.601

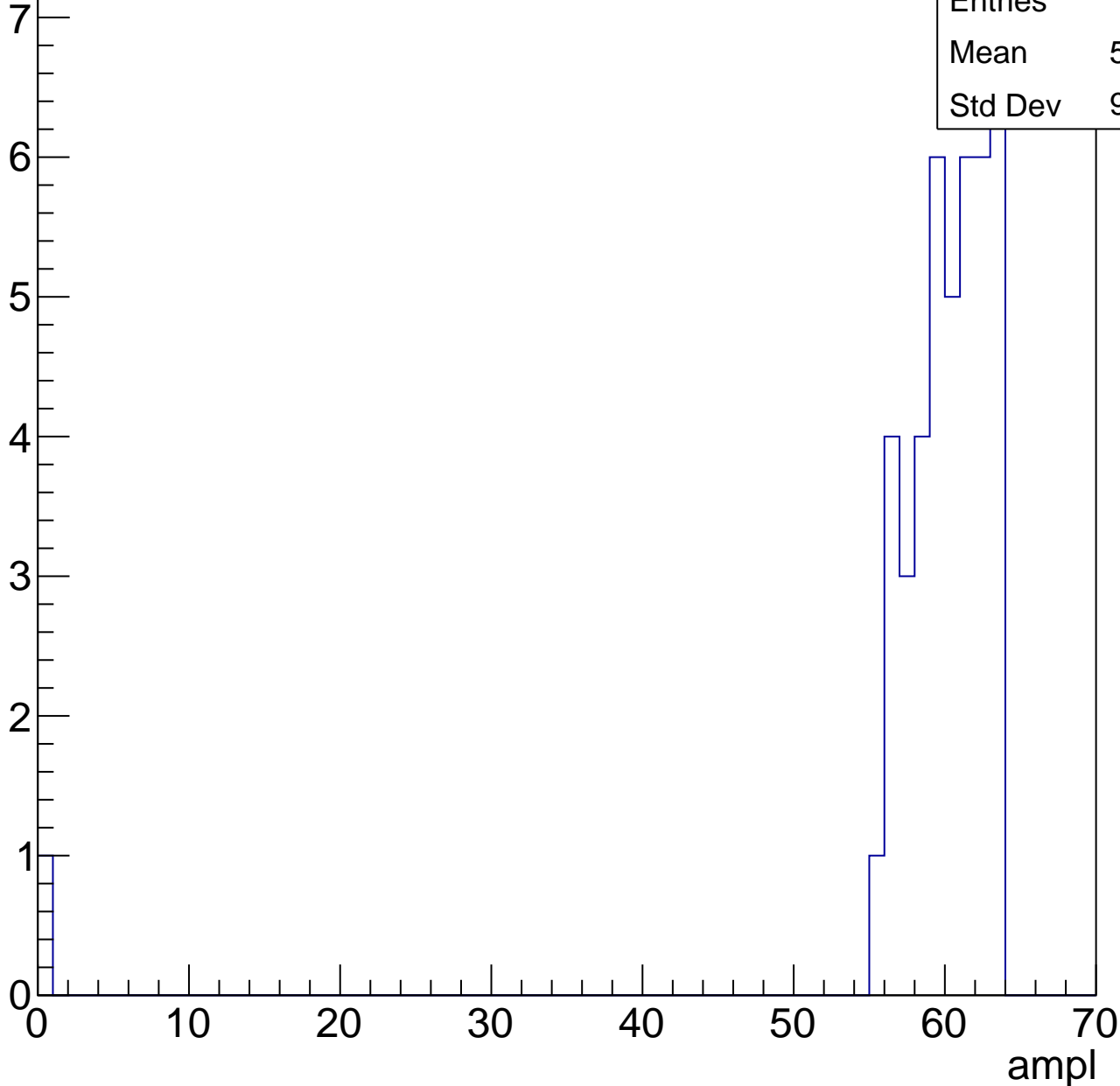


# B0L001S, U6-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	43
Mean	58.49
Std Dev	9.317



# B0L001S, U6-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	5
Mean	61.8
Std Dev	1.166



# B0L001S, U6-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U6-ch33, adc0

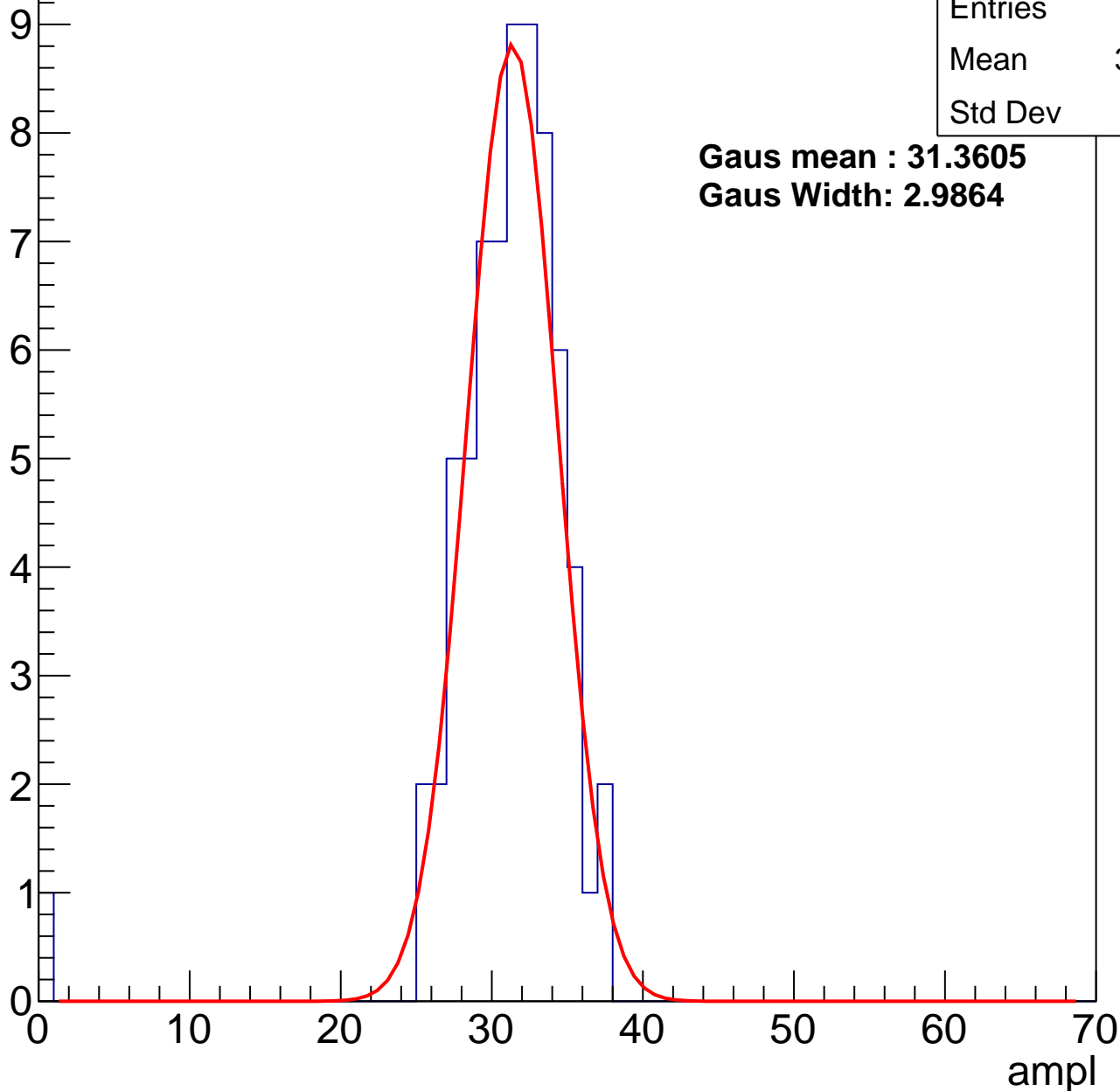
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	30.51
Std Dev	4.67

**Gaus mean : 31.3605**

**Gaus Width: 2.9864**



# B0L001S, U6-ch33, adc1

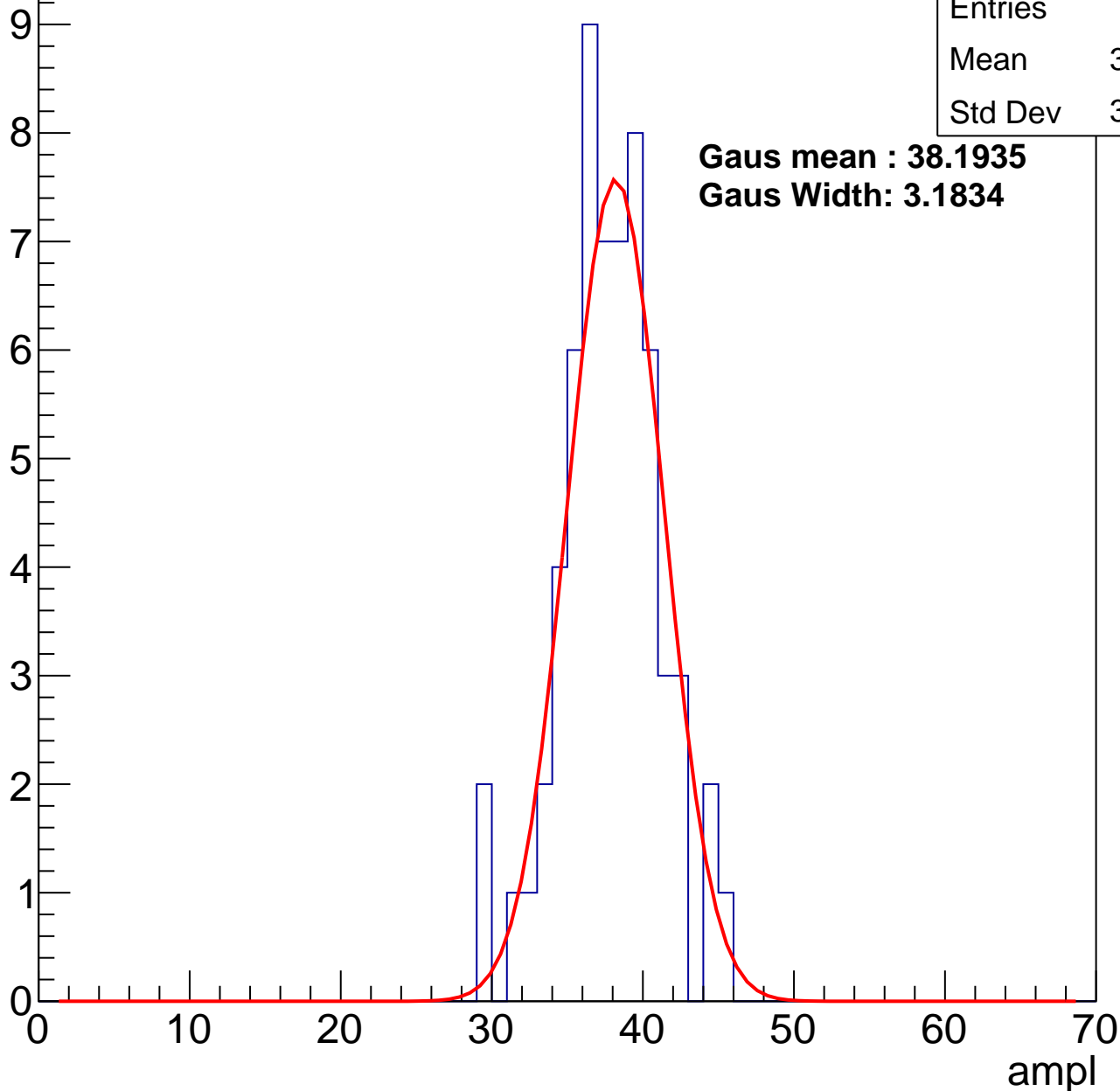
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	37.35
Std Dev	3.263

**Gaus mean : 38.1935**

**Gaus Width: 3.1834**



# B0L001S, U6-ch33, adc2

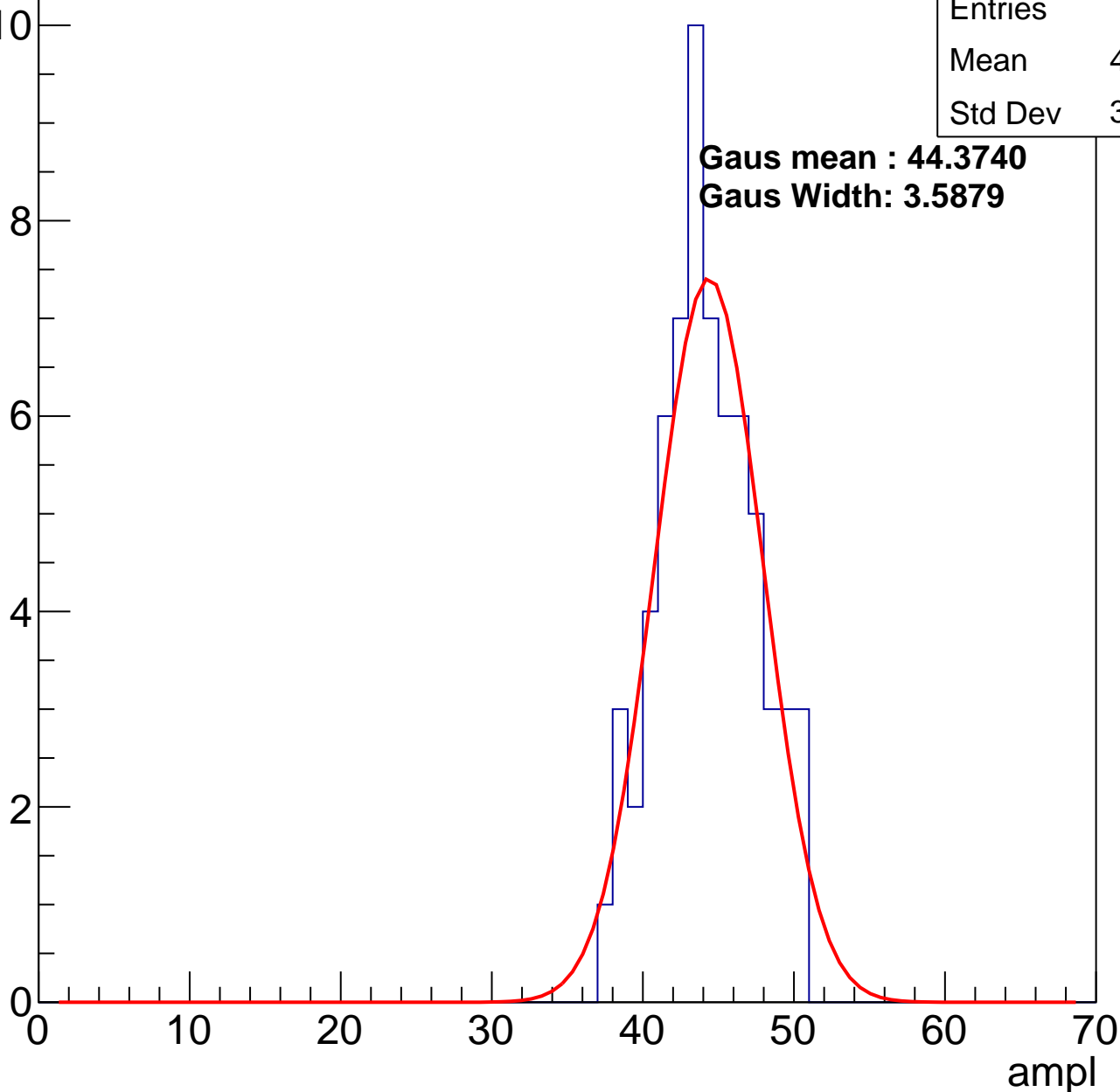
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	43.77
Std Dev	3.176

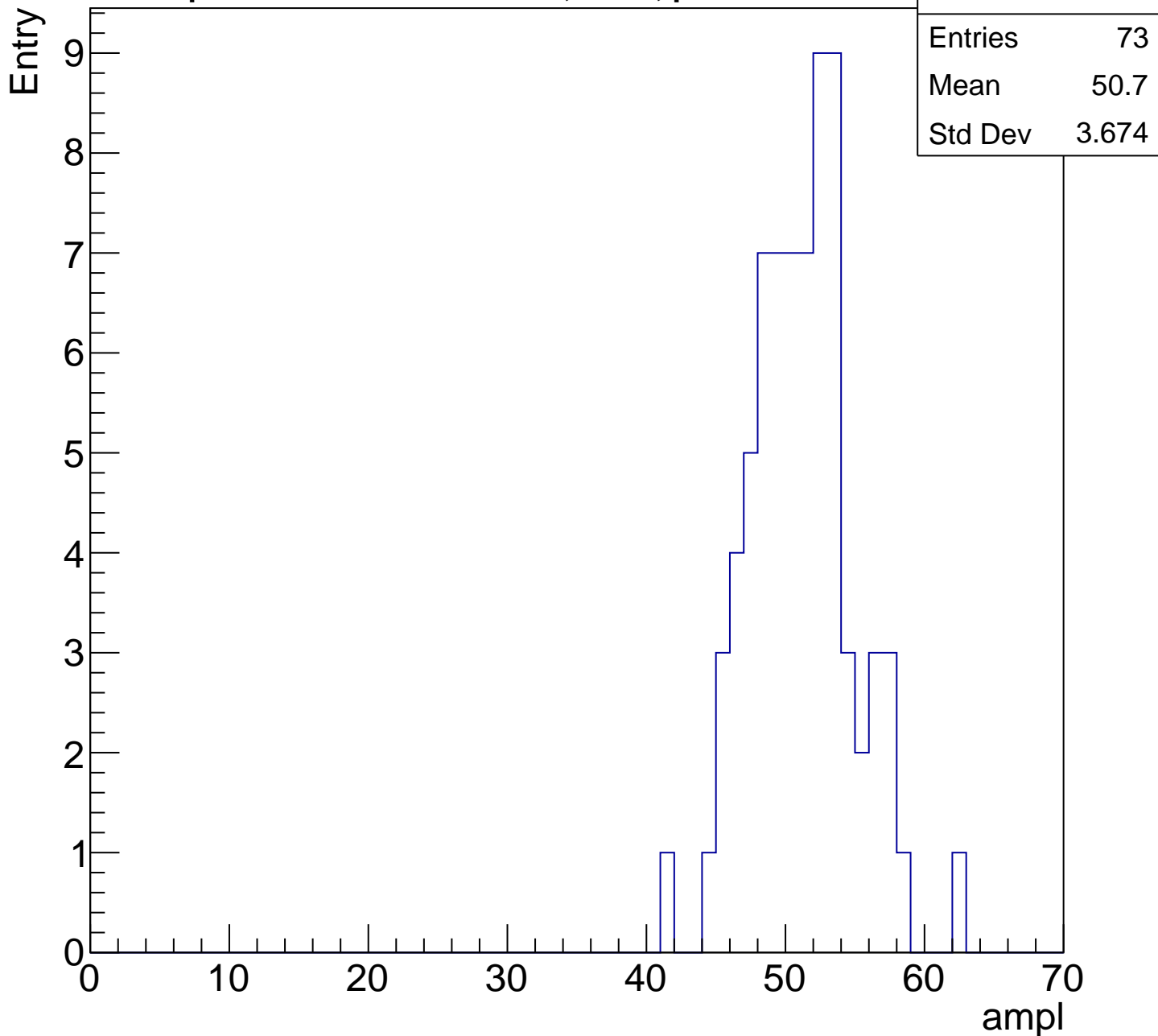
**Gaus mean : 44.3740**

**Gaus Width: 3.5879**



# B0L001S, U6-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

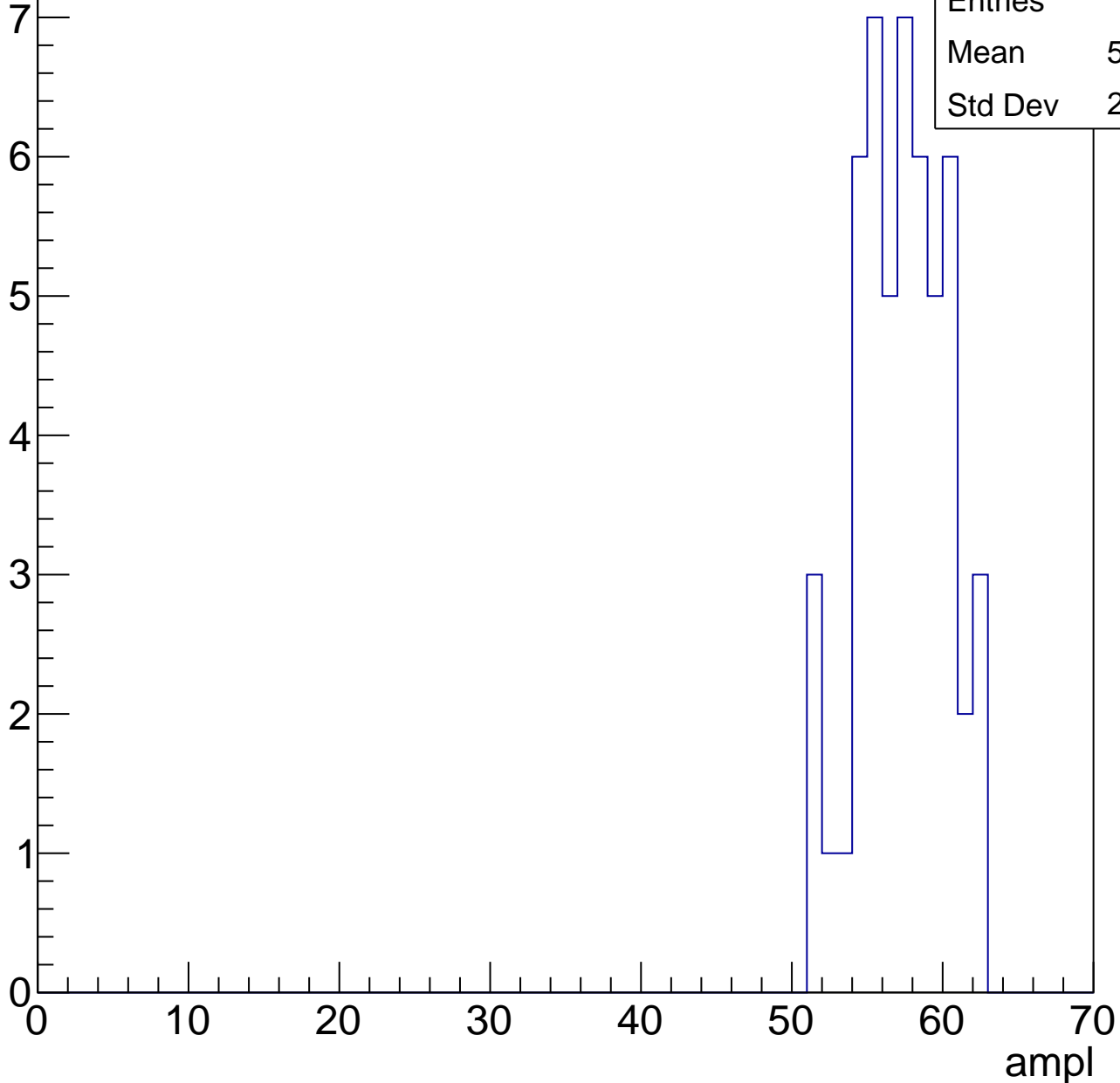


# B0L001S, U6-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	56.87
Std Dev	2.849

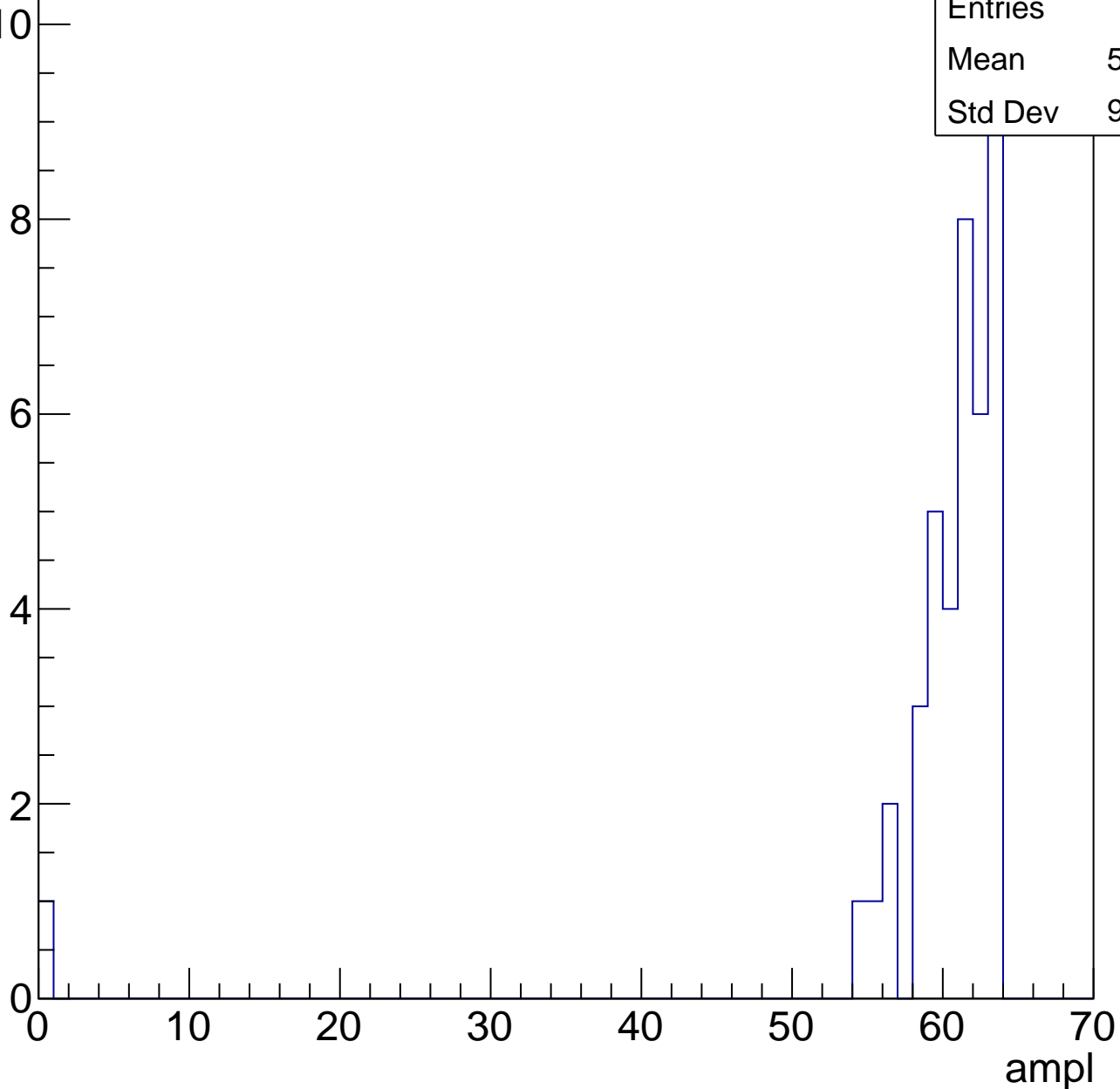


# B0L001S, U6-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	41
Mean	59.02
Std Dev	9.618



# B0L001S, U6-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U6-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U6-ch34, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	78
Mean	29.37
Std Dev	3.163

**Gaus mean : 29.8017**

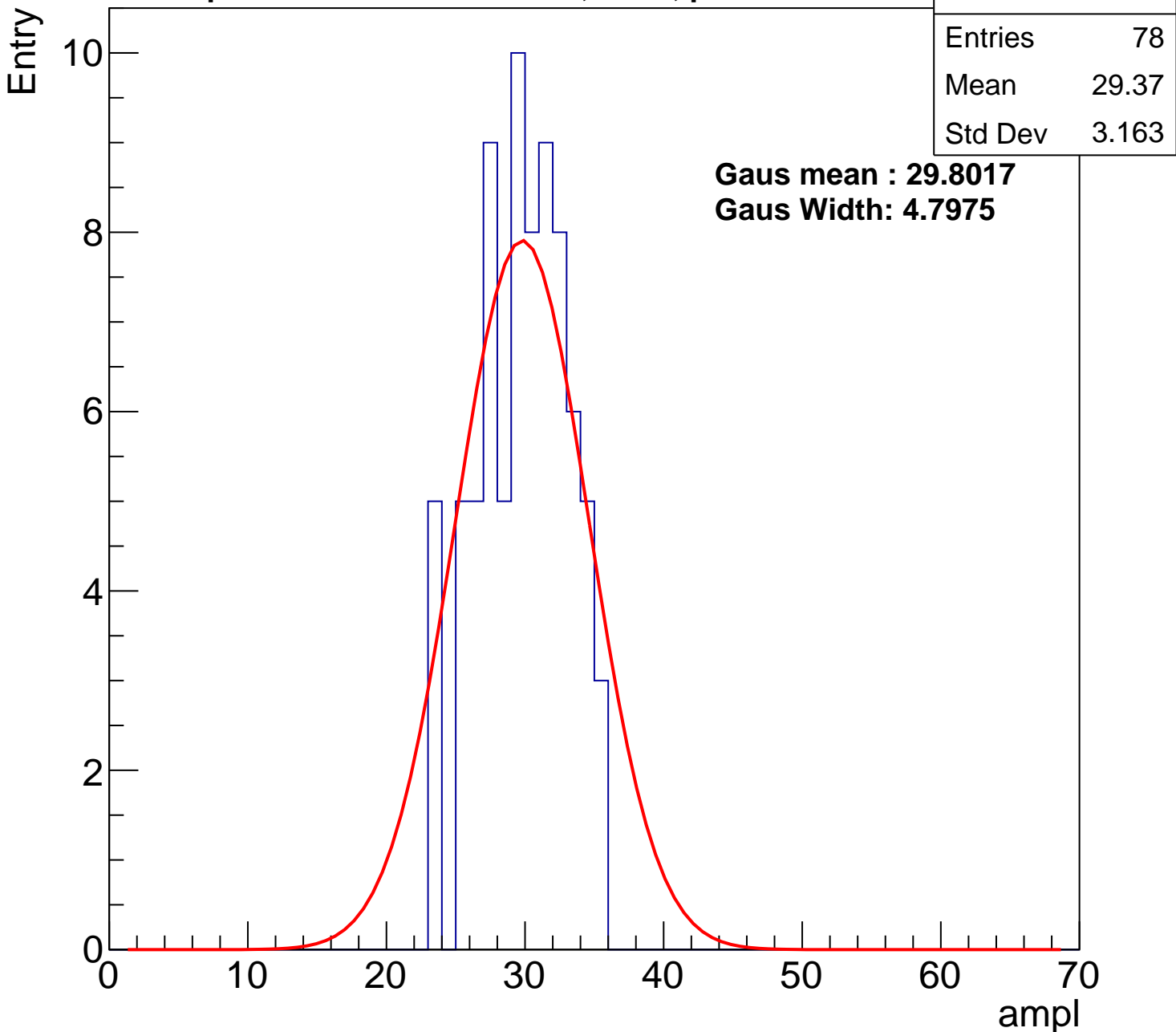
**Gaus Width: 4.7975**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U6-ch34, adc1

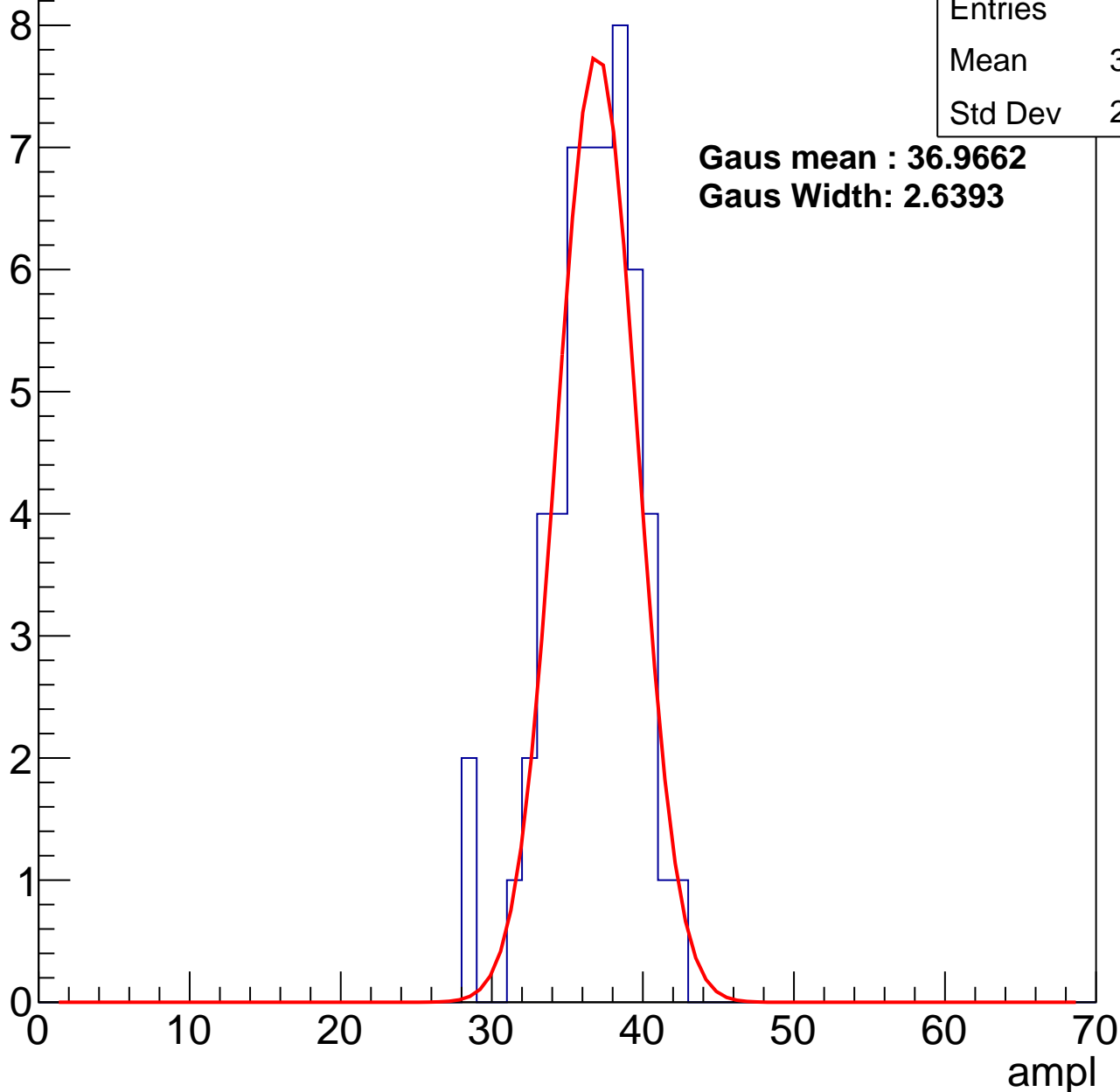
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	36.22
Std Dev	2.917

**Gaus mean : 36.9662**

**Gaus Width: 2.6393**



# B0L001S, U6-ch34, adc2

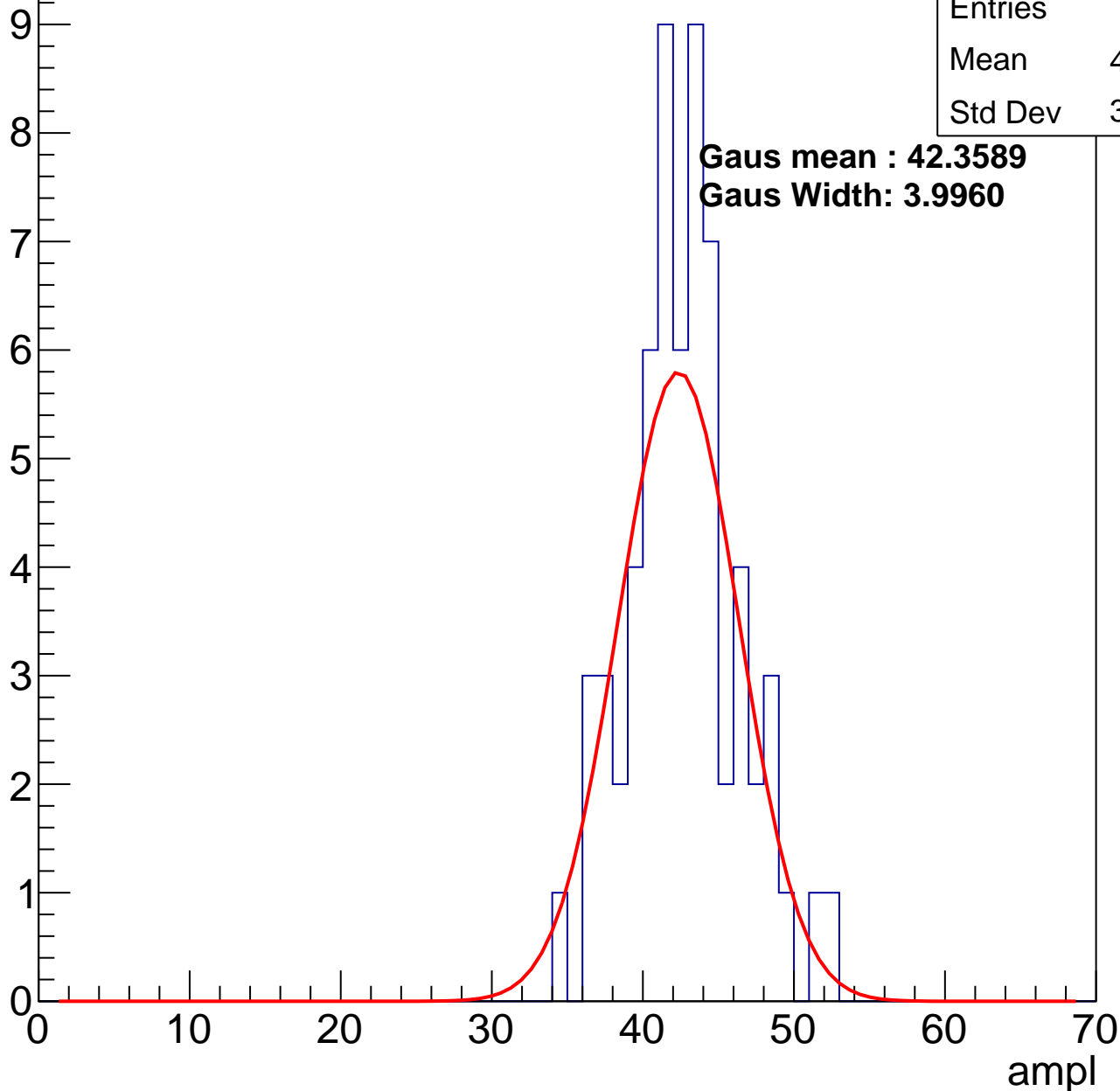
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	42.27
Std Dev	3.645

**Gaus mean : 42.3589**

**Gaus Width: 3.9960**

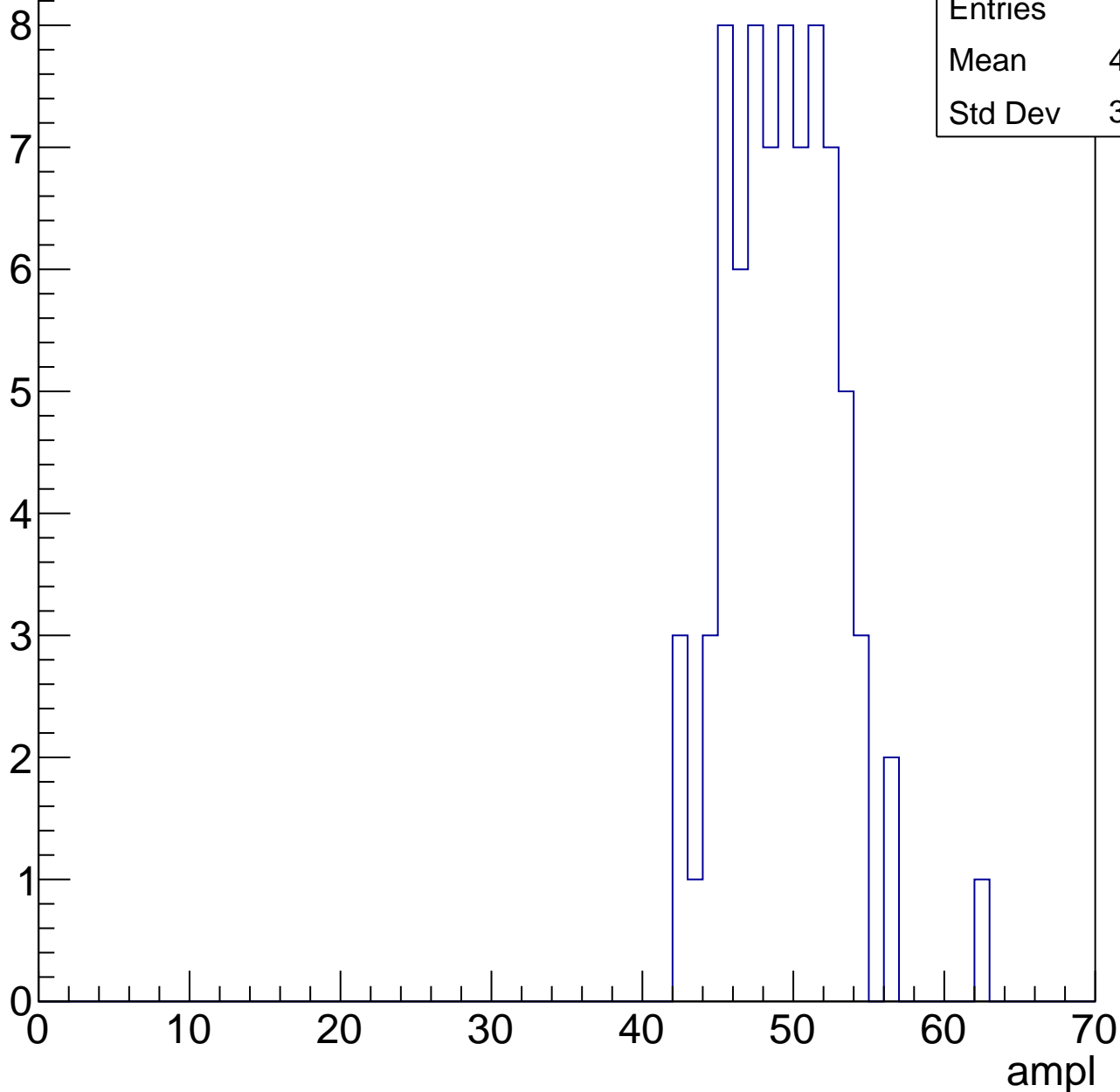


# B0L001S, U6-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

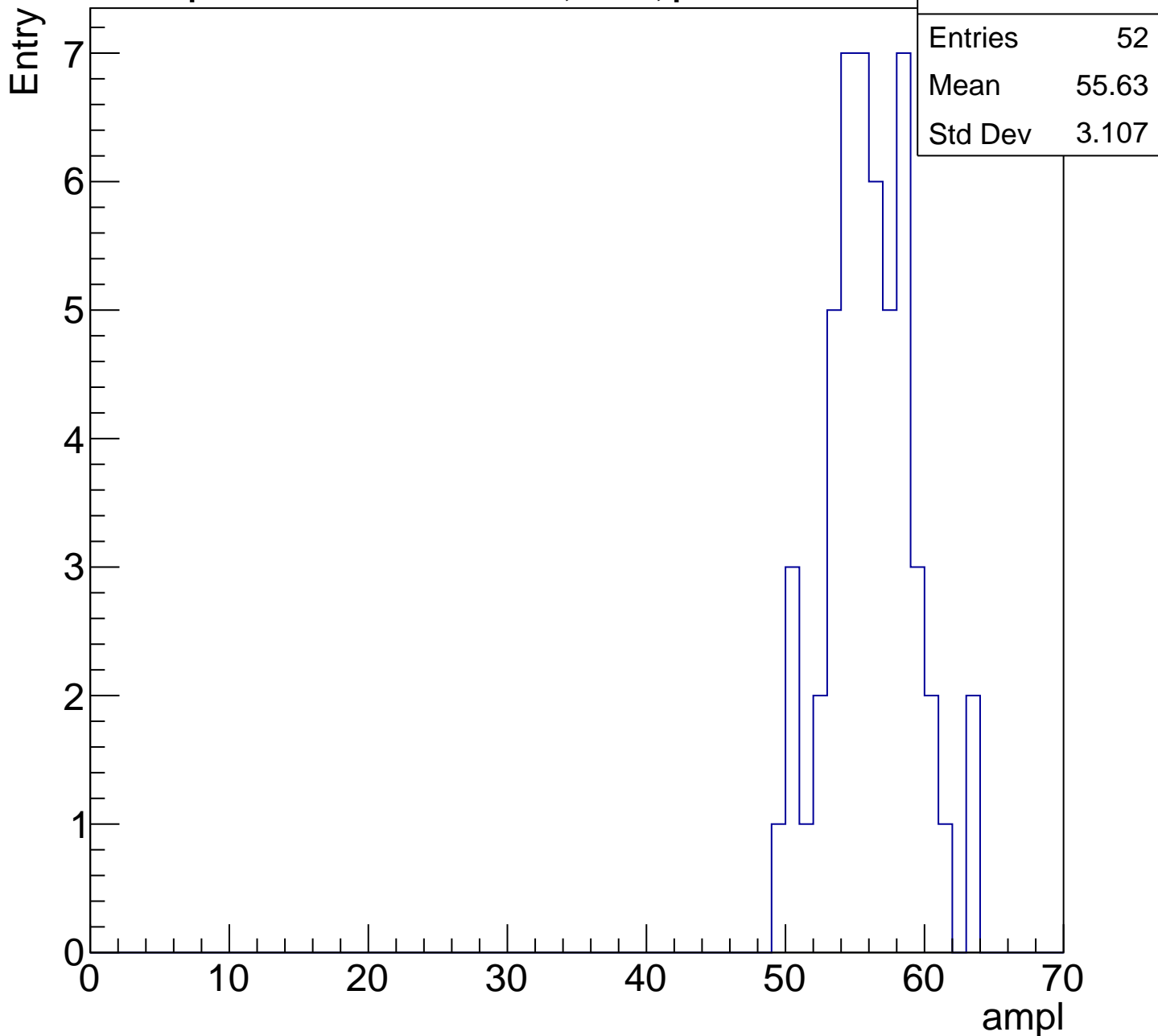
Entry

Entries	77
Mean	48.88
Std Dev	3.607



# B0L001S, U6-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

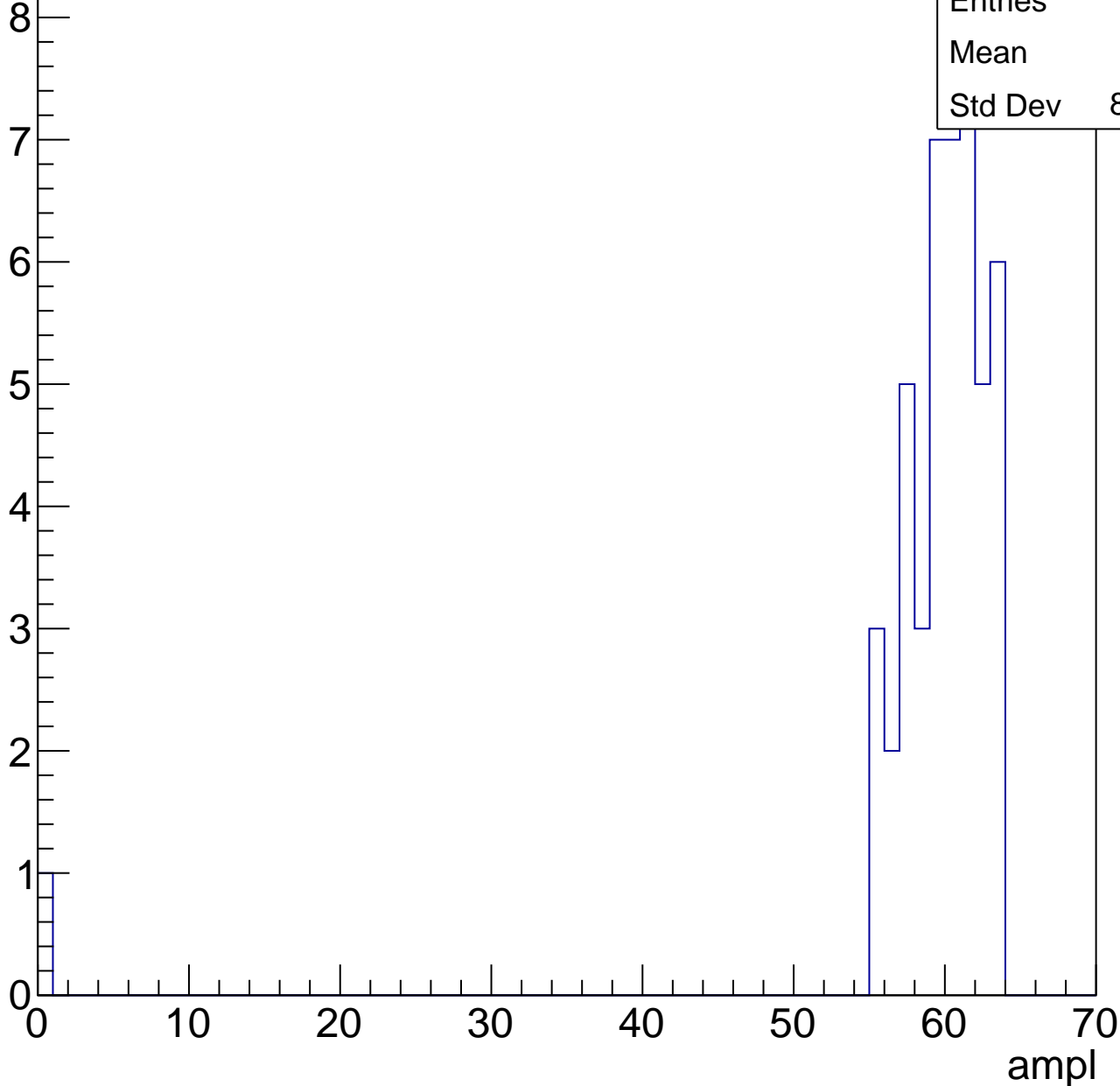


# B0L001S, U6-ch34, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

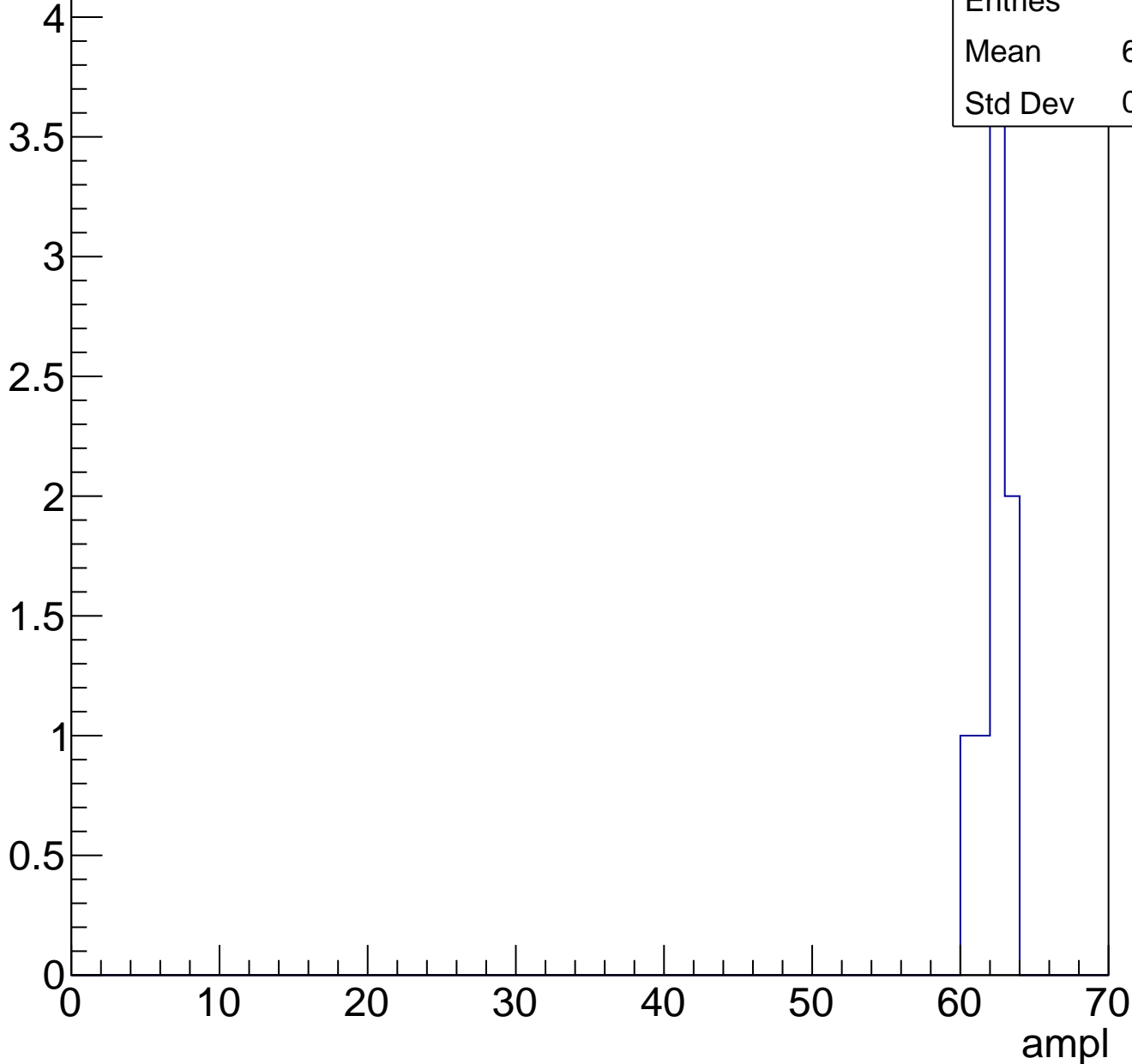
Entries	47
Mean	58.4
Std Dev	8.912



# B0L001S, U6-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch35, adc0

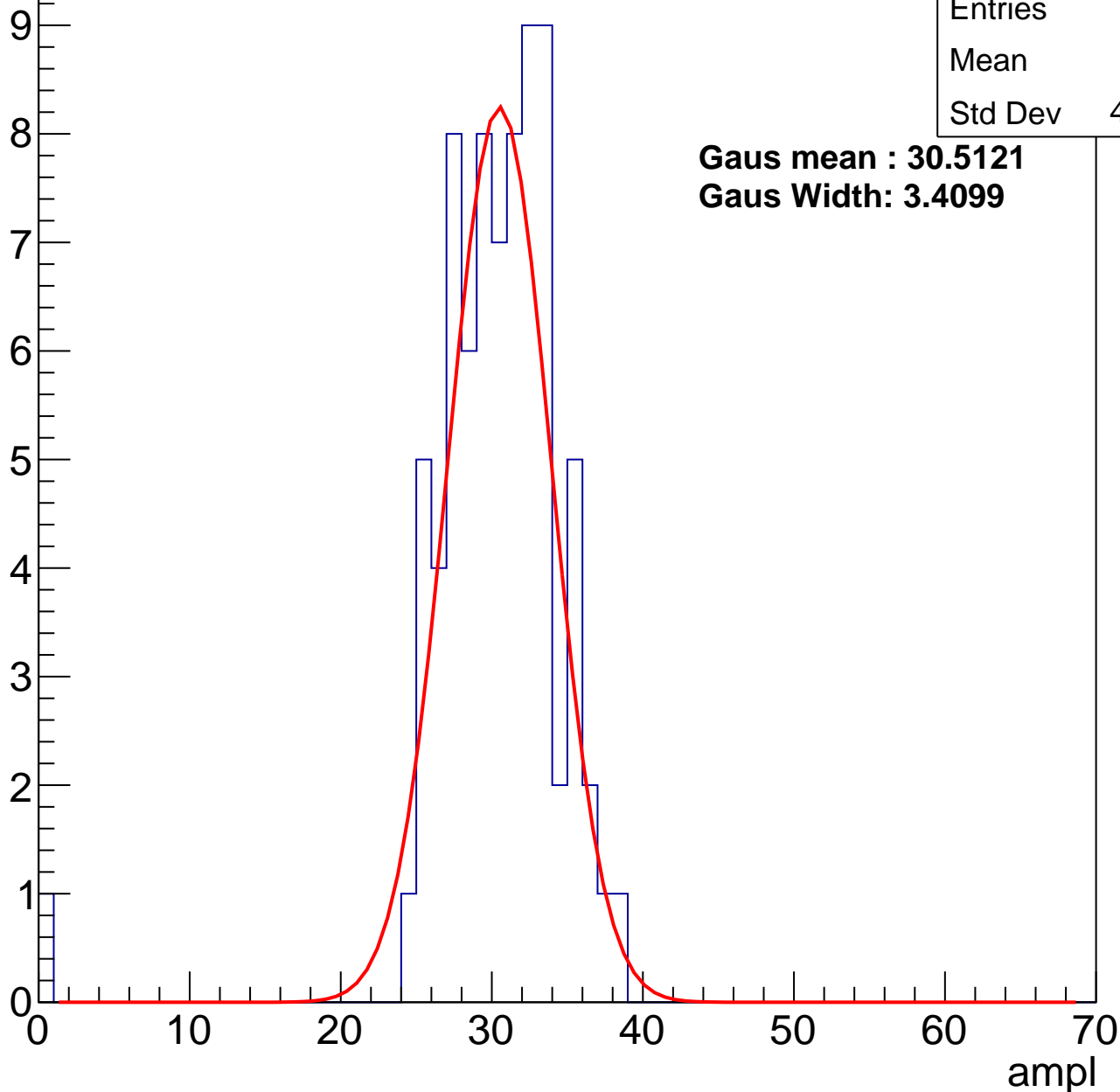
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	29.9
Std Dev	4.692

**Gaus mean : 30.5121**

**Gaus Width: 3.4099**



# B0L001S, U6-ch35, adc1

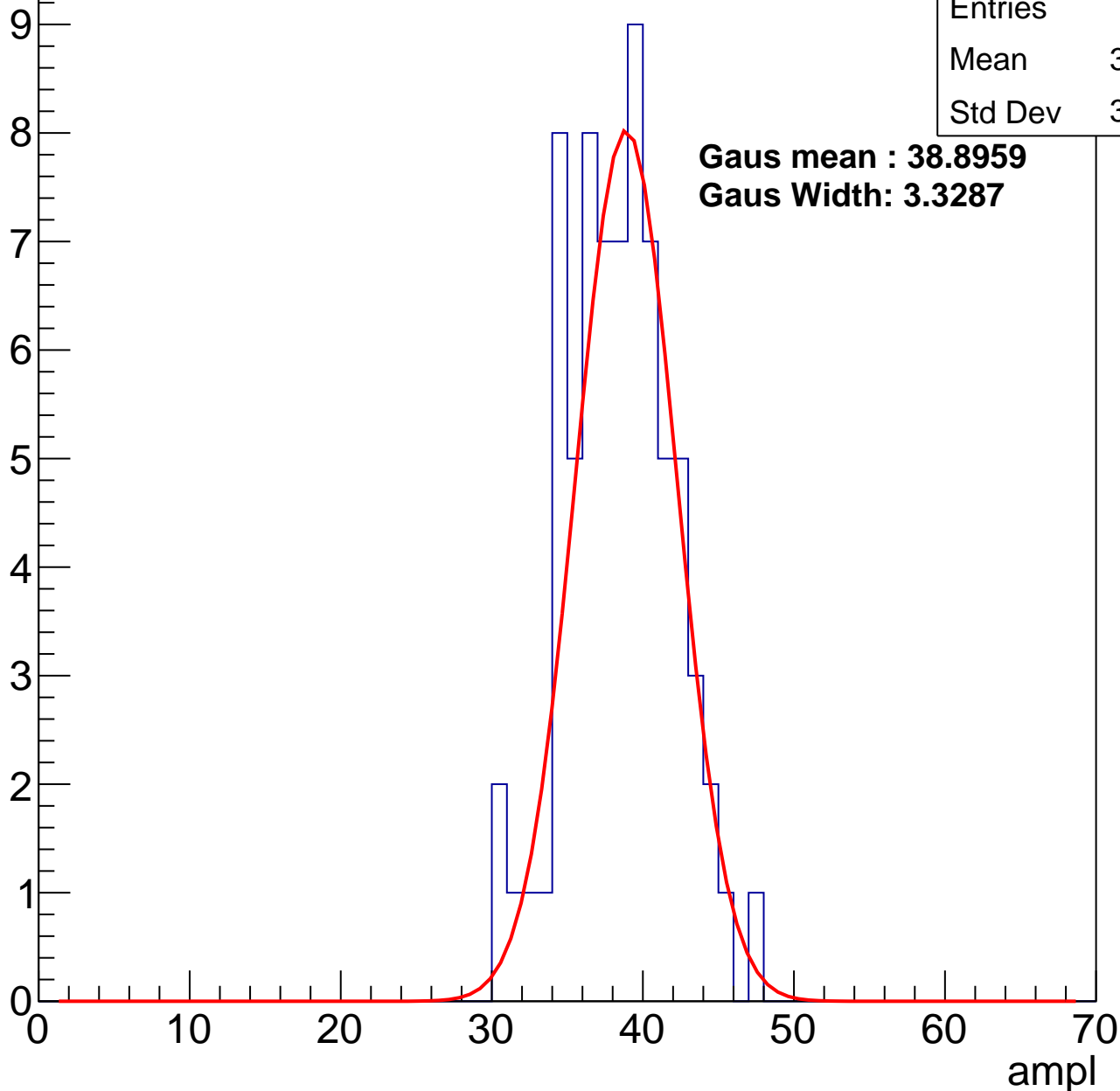
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	37.96
Std Dev	3.489

**Gaus mean : 38.8959**

**Gaus Width: 3.3287**



# B0L001S, U6-ch35, adc2

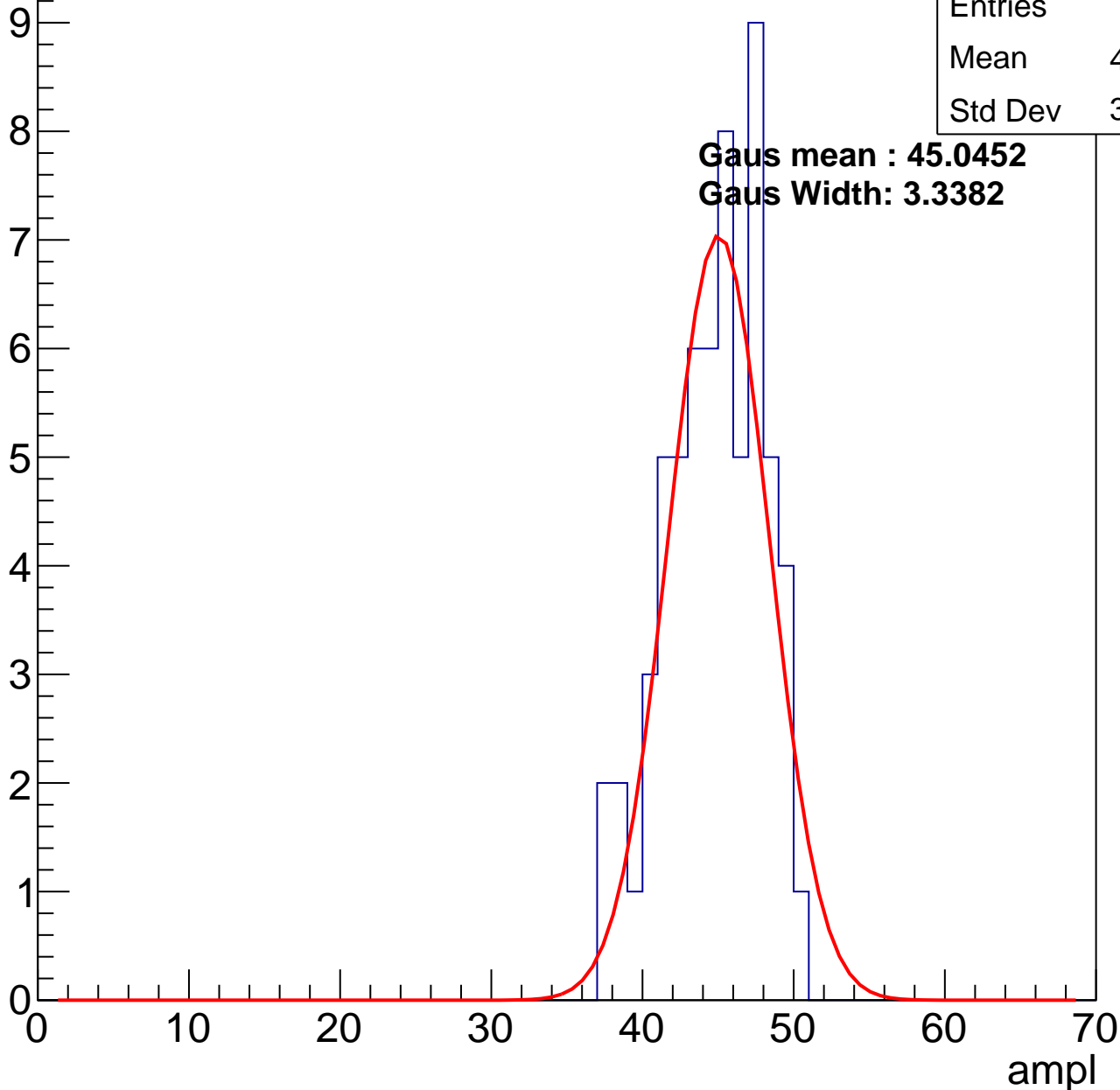
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	44.27
Std Dev	3.199

**Gaus mean : 45.0452**

**Gaus Width: 3.3382**

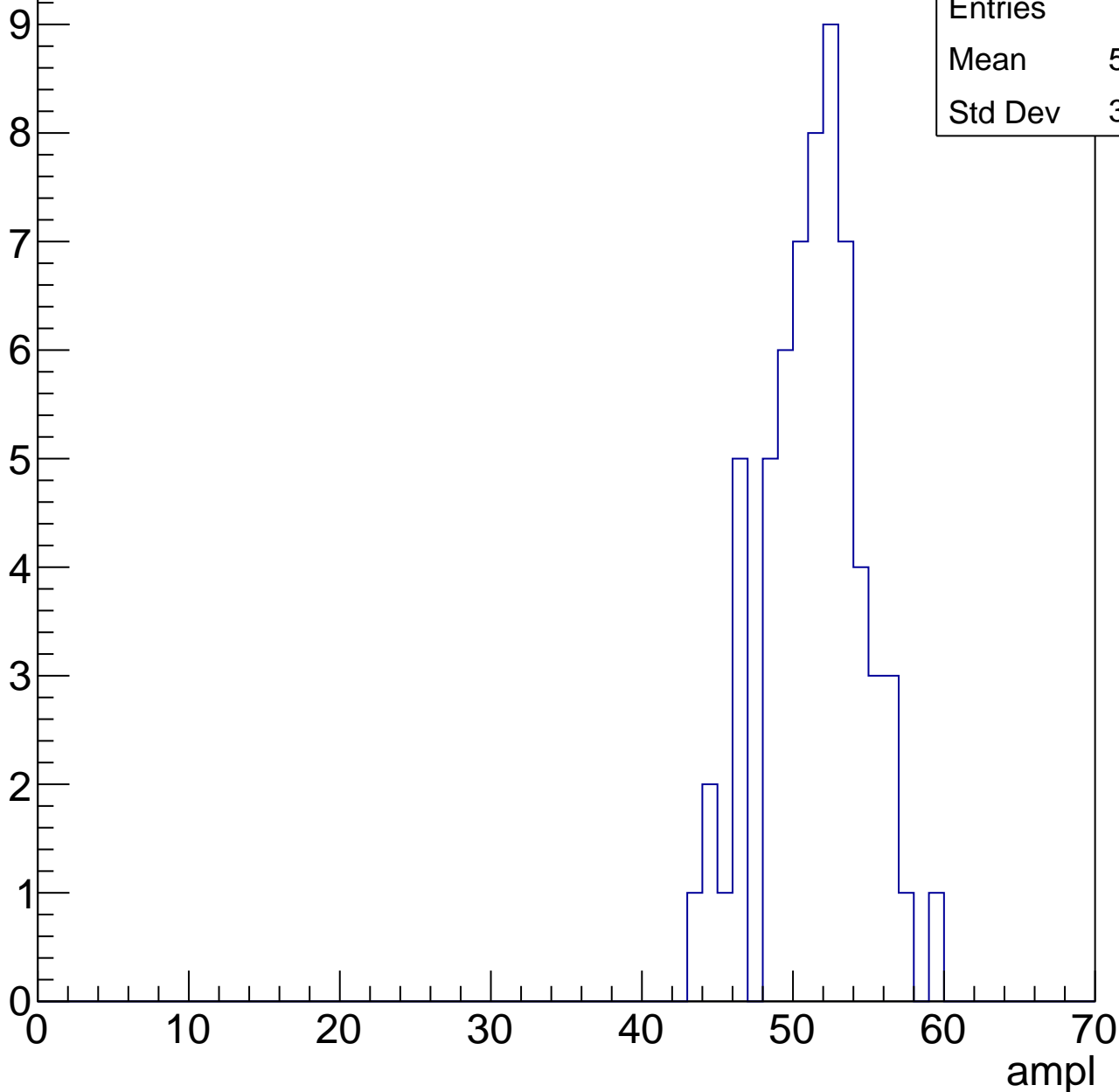


# B0L001S, U6-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

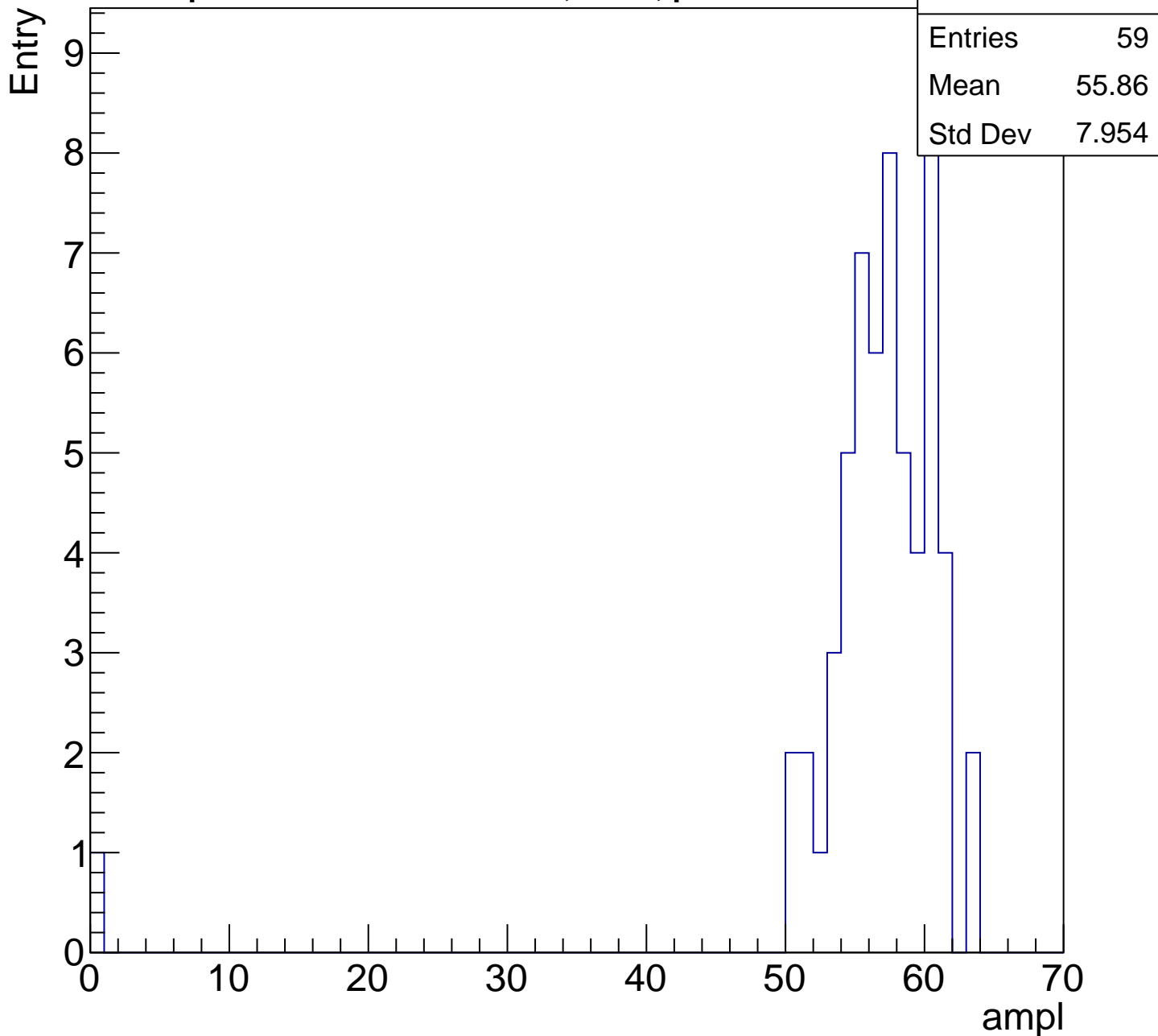
Entry

Entries	63
Mean	50.83
Std Dev	3.317



# B0L001S, U6-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

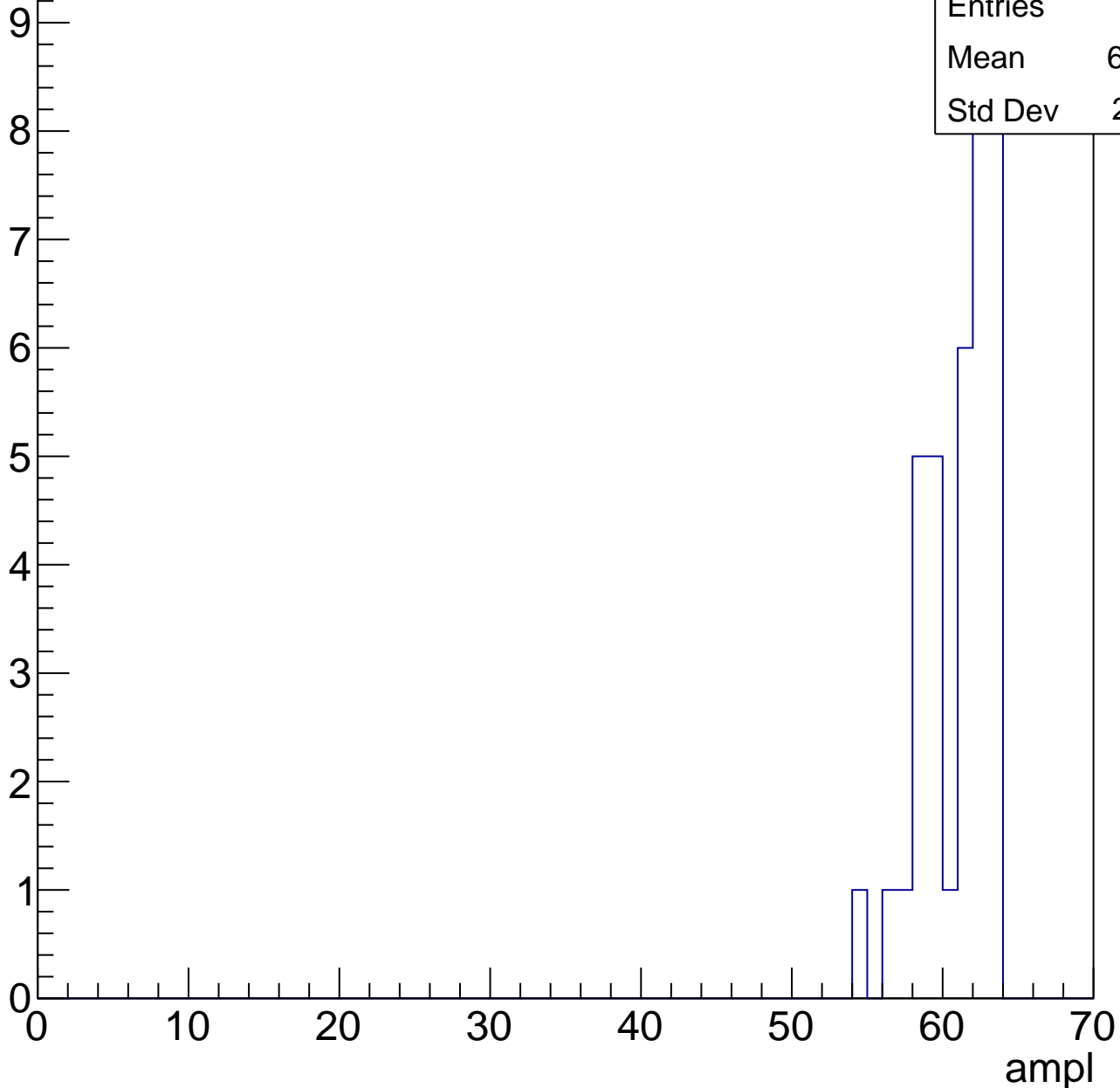


# B0L001S, U6-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	37
Mean	60.54
Std Dev	2.261



# B0L001S, U6-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U6-ch36, adc0

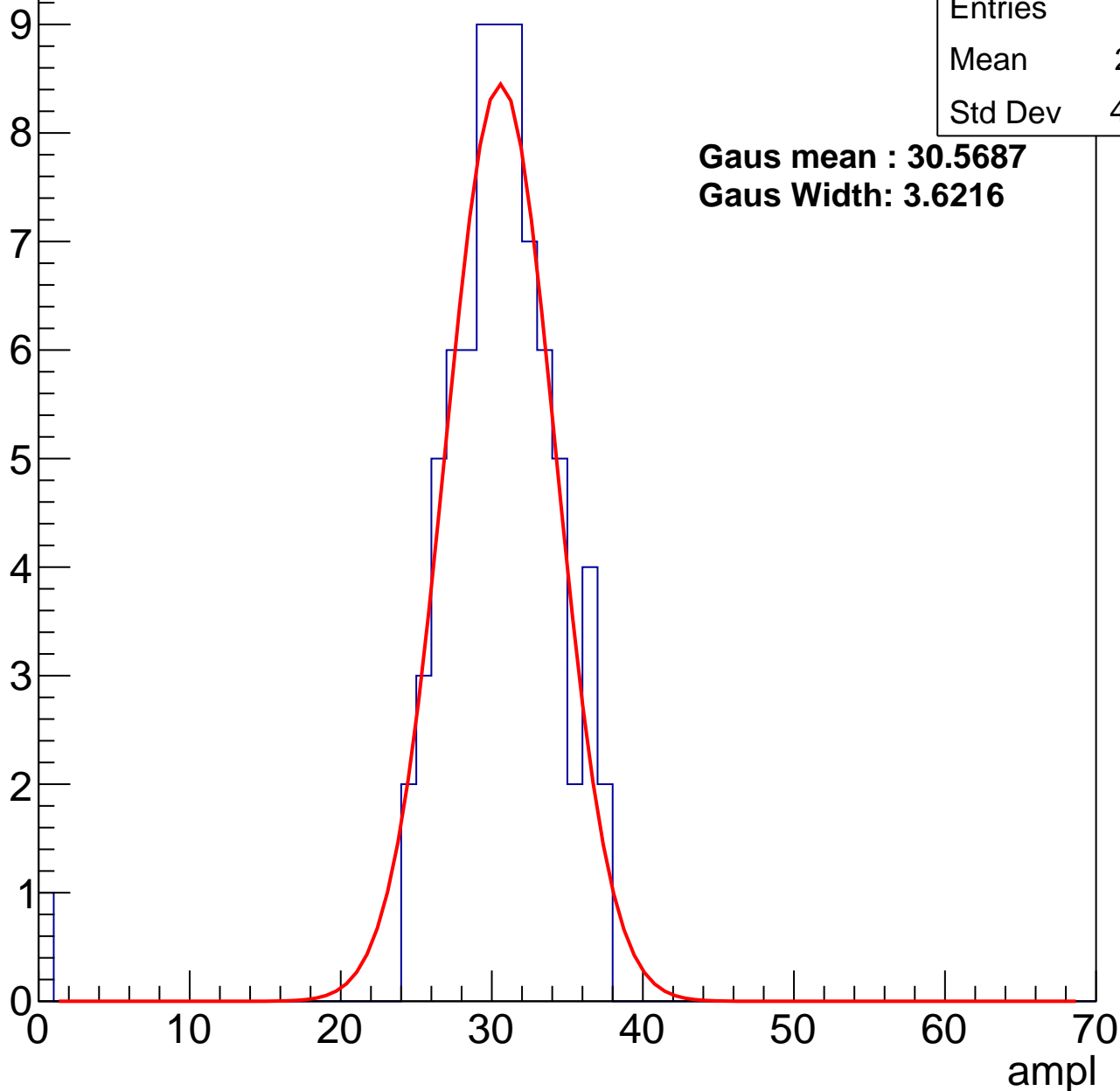
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	29.91
Std Dev	4.697

**Gaus mean : 30.5687**

**Gaus Width: 3.6216**



# B0L001S, U6-ch36, adc1

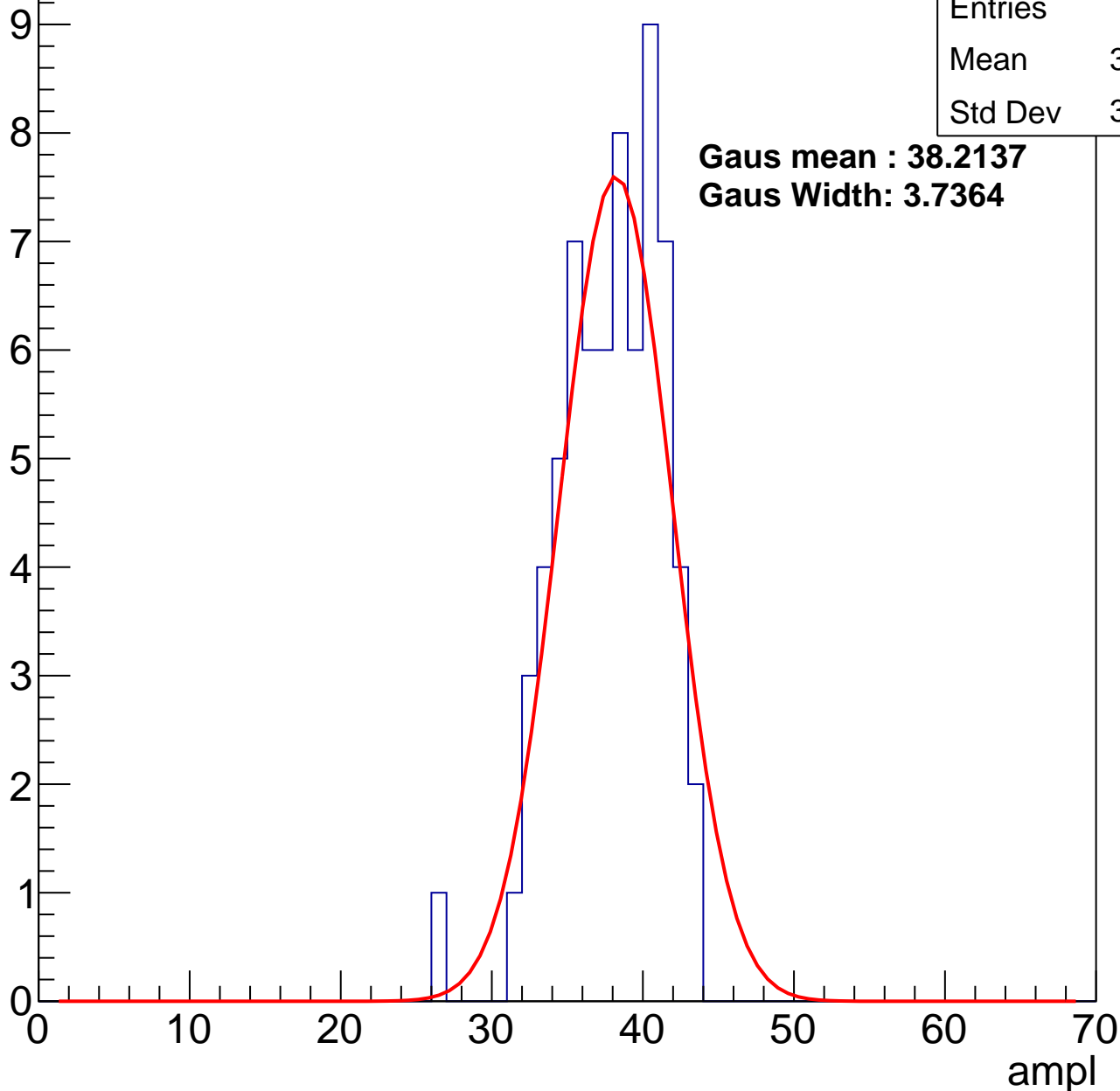
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	37.35
Std Dev	3.327

**Gaus mean : 38.2137**

**Gaus Width: 3.7364**



# B0L001S, U6-ch36, adc2

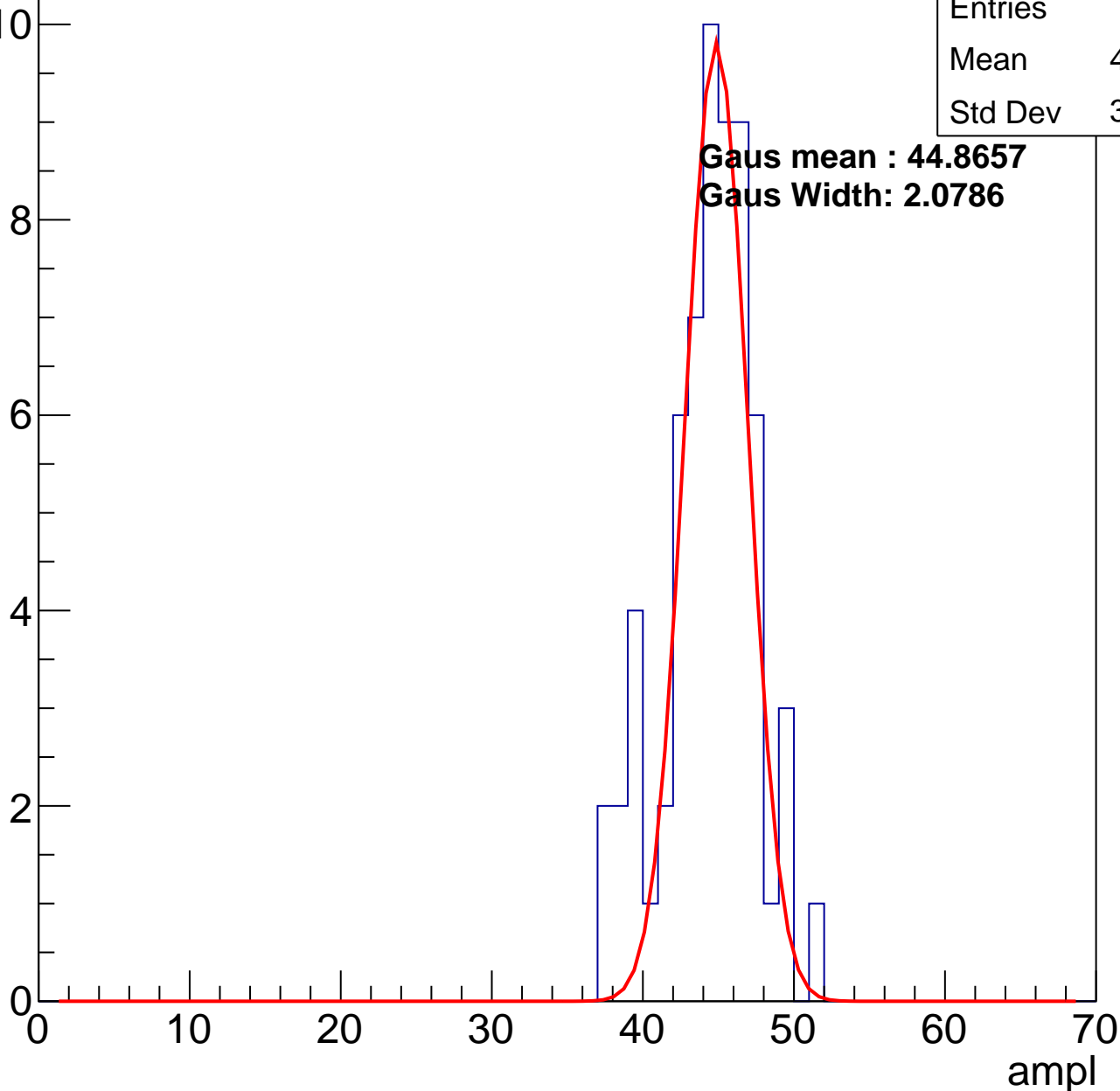
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	43.94
Std Dev	3.018

**Gaus mean : 44.8657**

**Gaus Width: 2.0786**

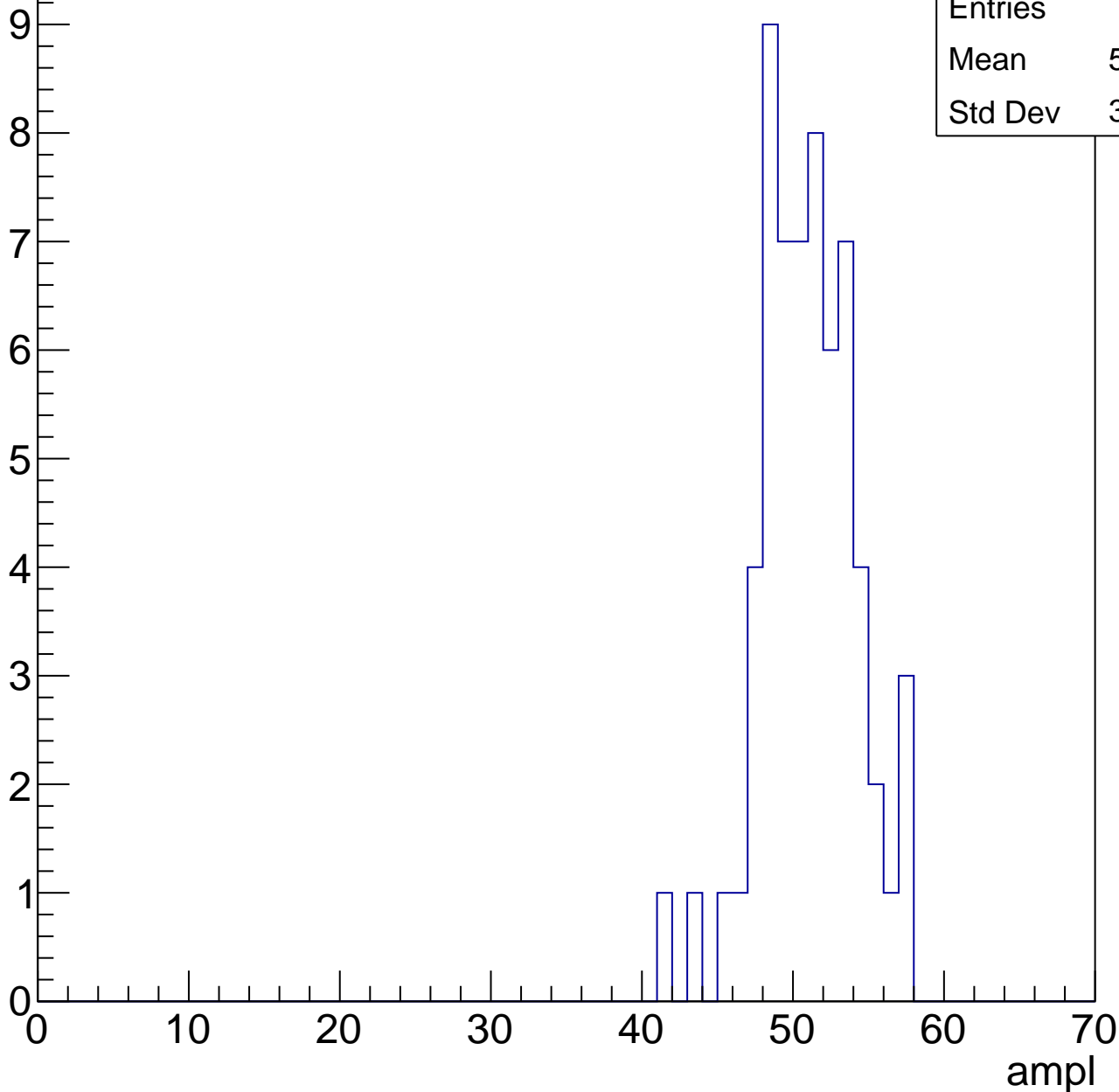


# B0L001S, U6-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

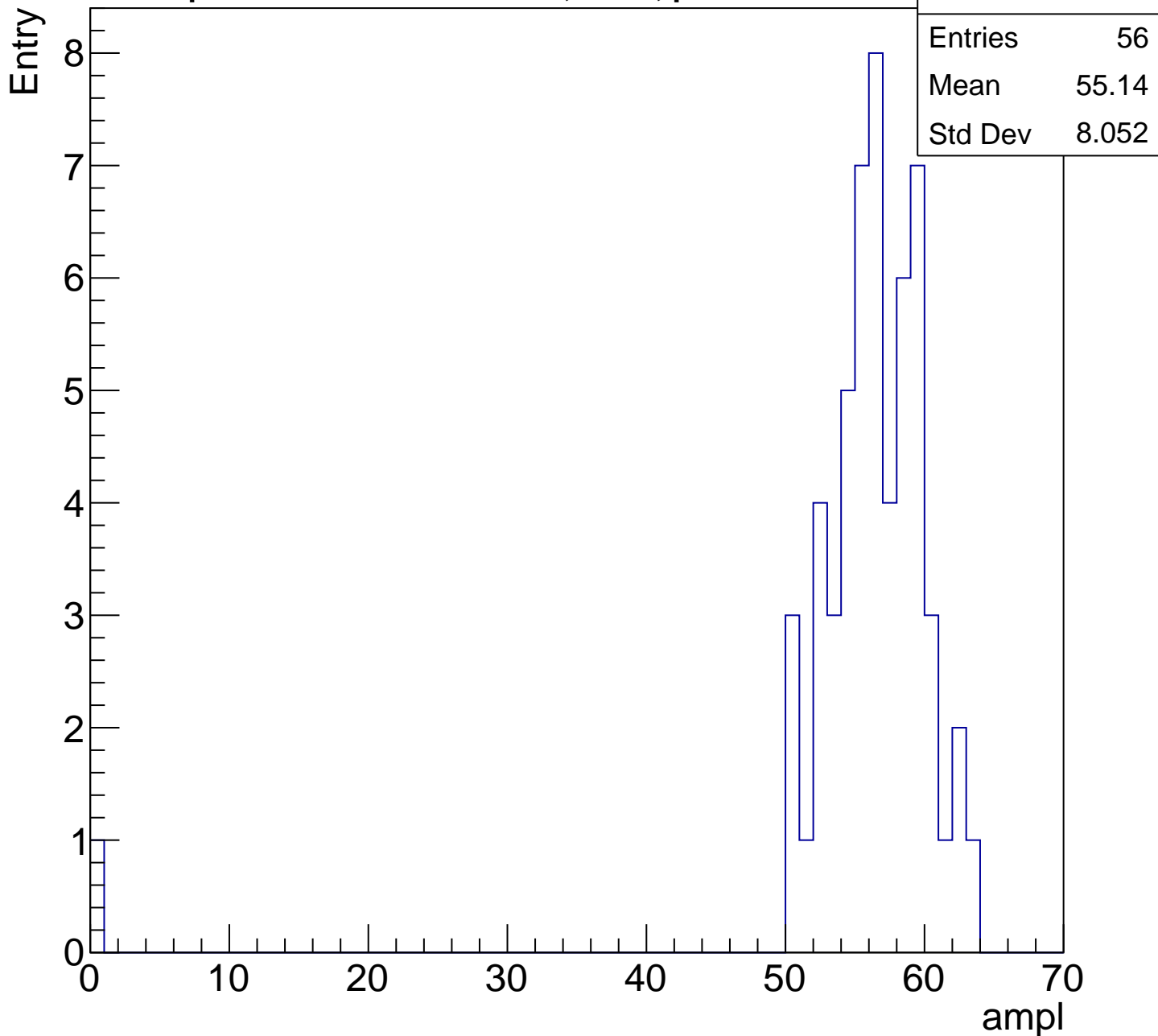
Entry

Entries	62
Mean	50.52
Std Dev	3.176



# B0L001S, U6-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

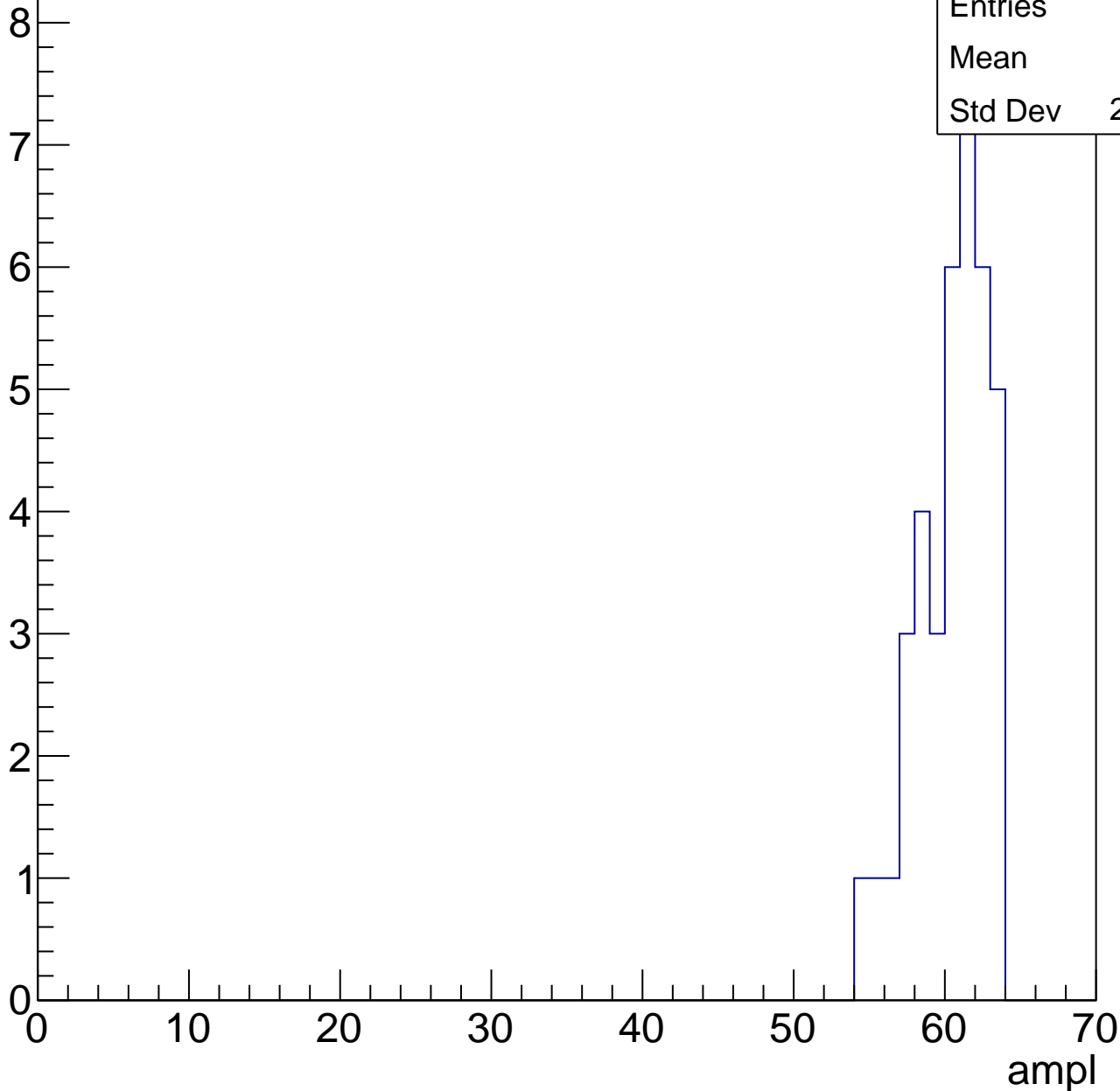


# B0L001S, U6-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

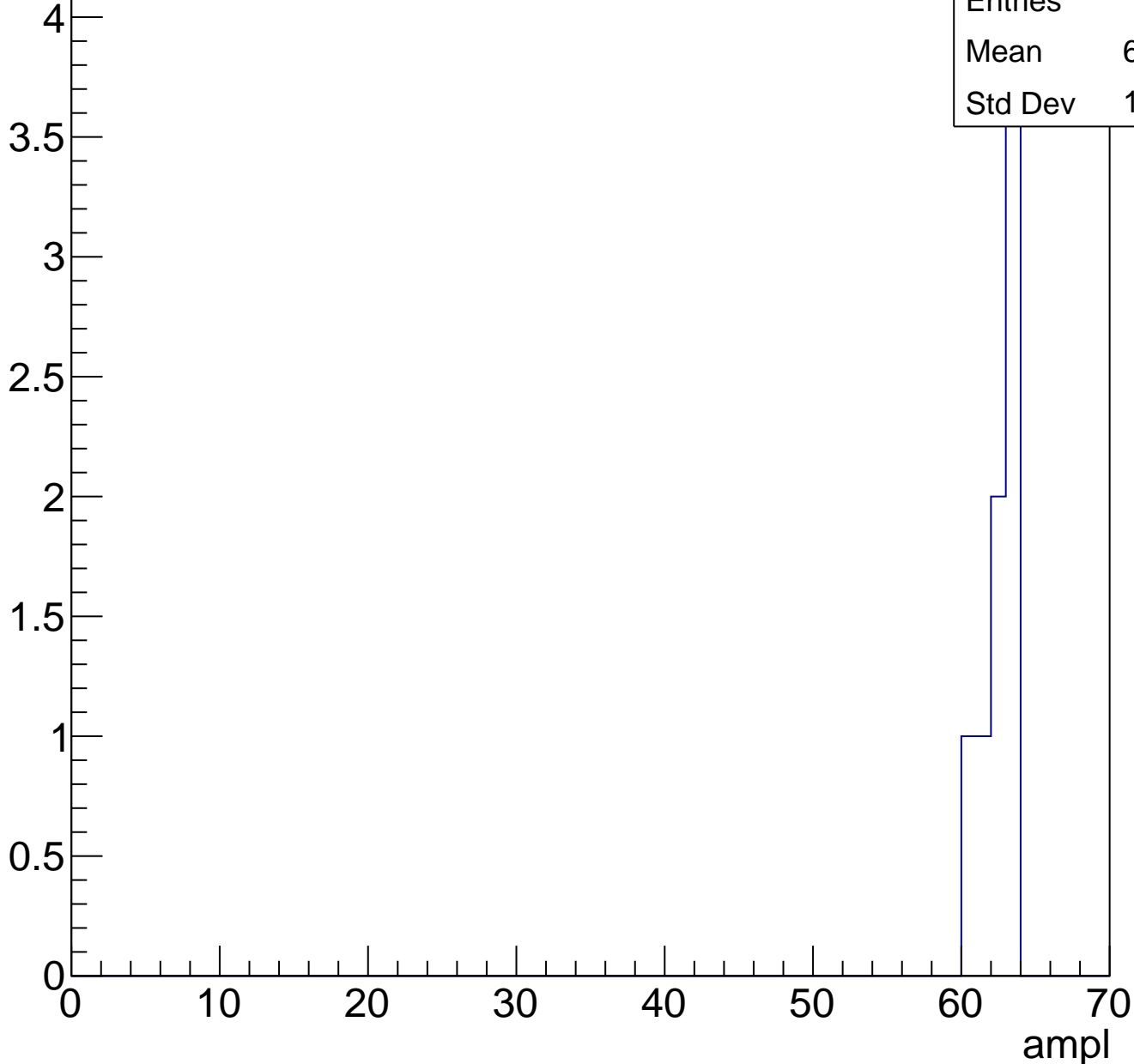
Entries	38
Mean	60
Std Dev	2.294



# B0L001S, U6-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	11
Std Dev	11

# B0L001S, U6-ch37, adc0

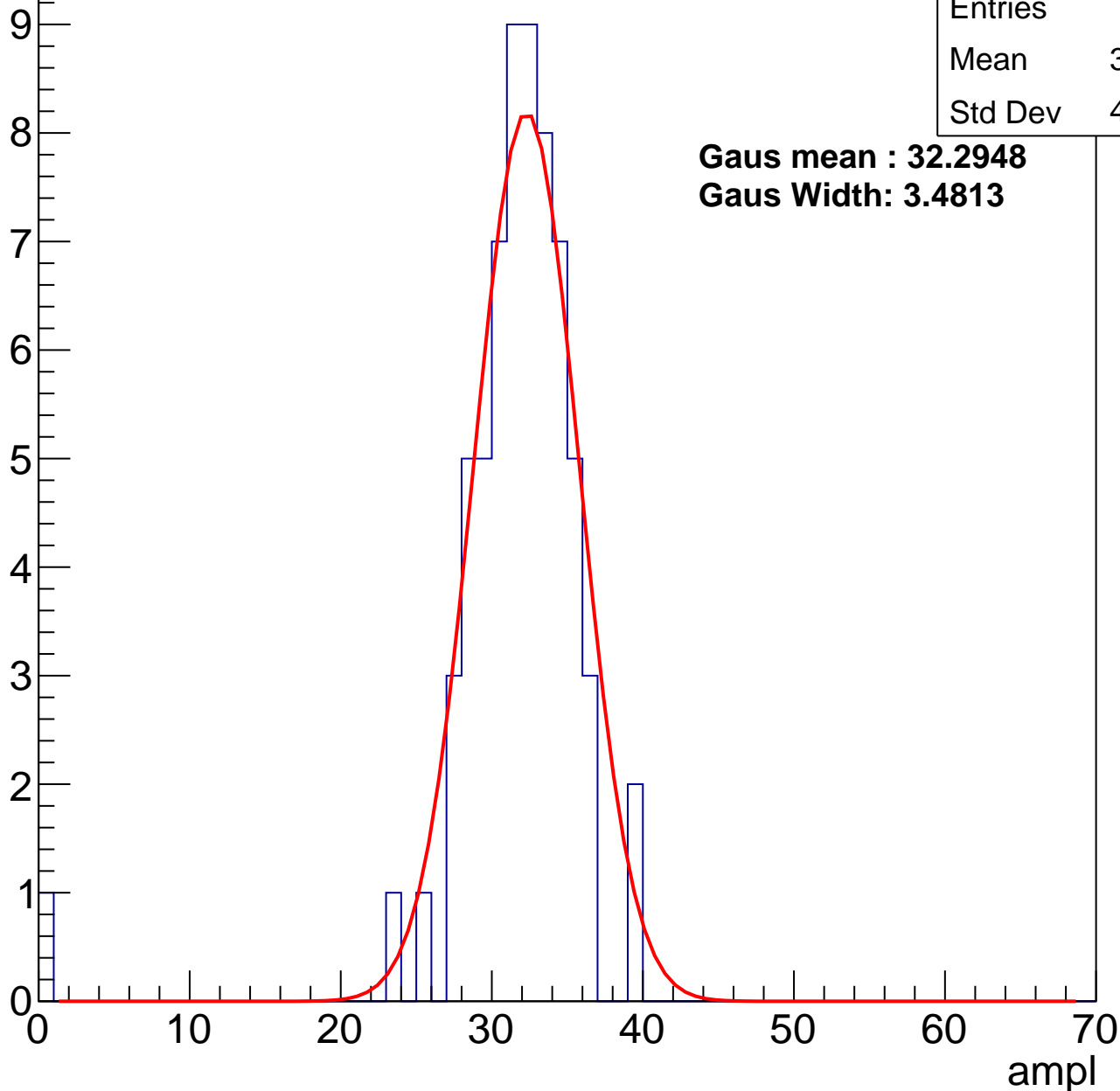
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	31.12
Std Dev	4.873

**Gaus mean : 32.2948**

**Gaus Width: 3.4813**



# B0L001S, U6-ch37, adc1

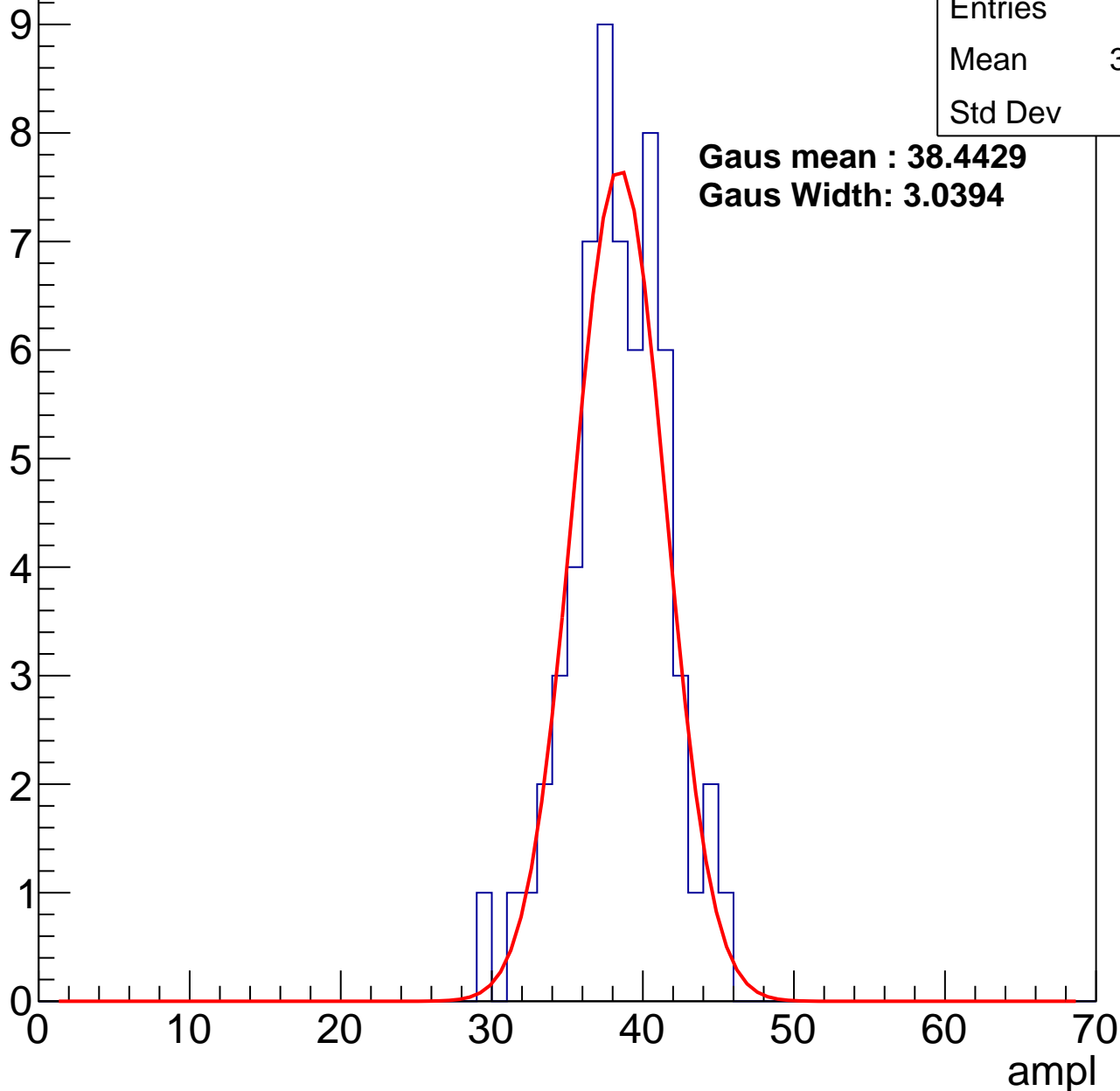
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	37.95
Std Dev	3.17

**Gaus mean : 38.4429**

**Gaus Width: 3.0394**



# B0L001S, U6-ch37, adc2

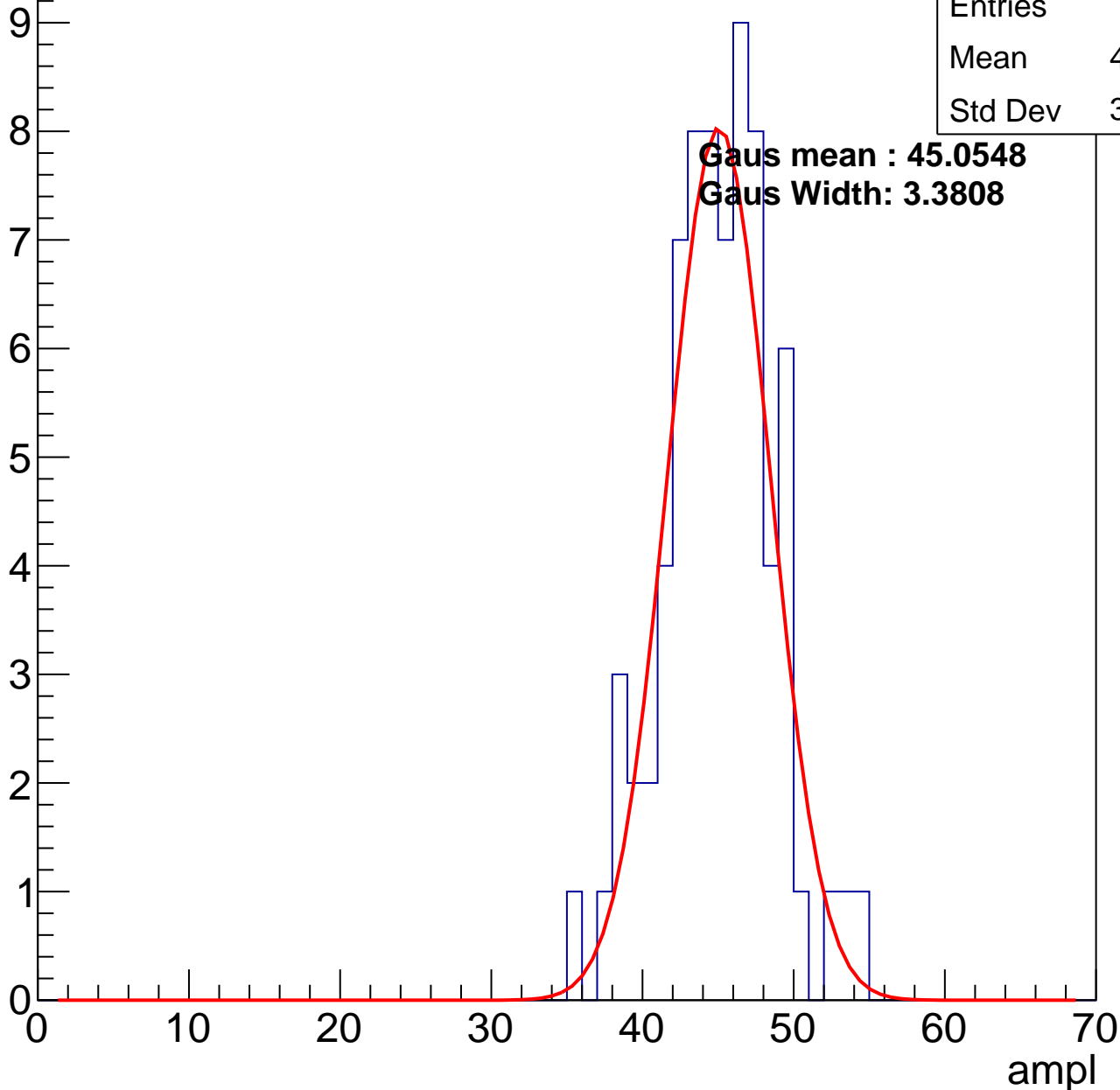
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	44.57
Std Dev	3.636

**Gaus mean : 45.0548**

**Gaus Width: 3.3808**

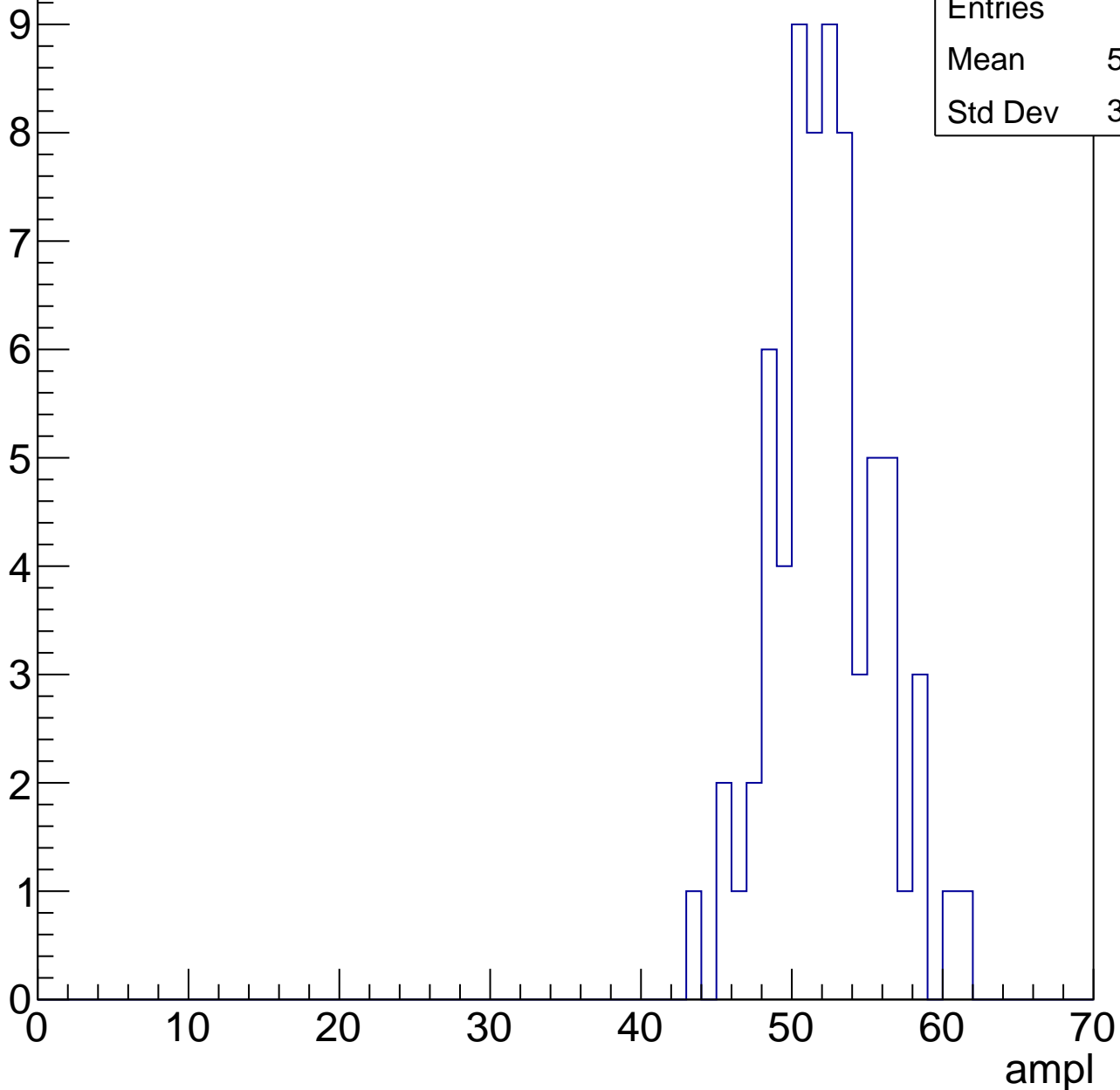


# B0L001S, U6-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

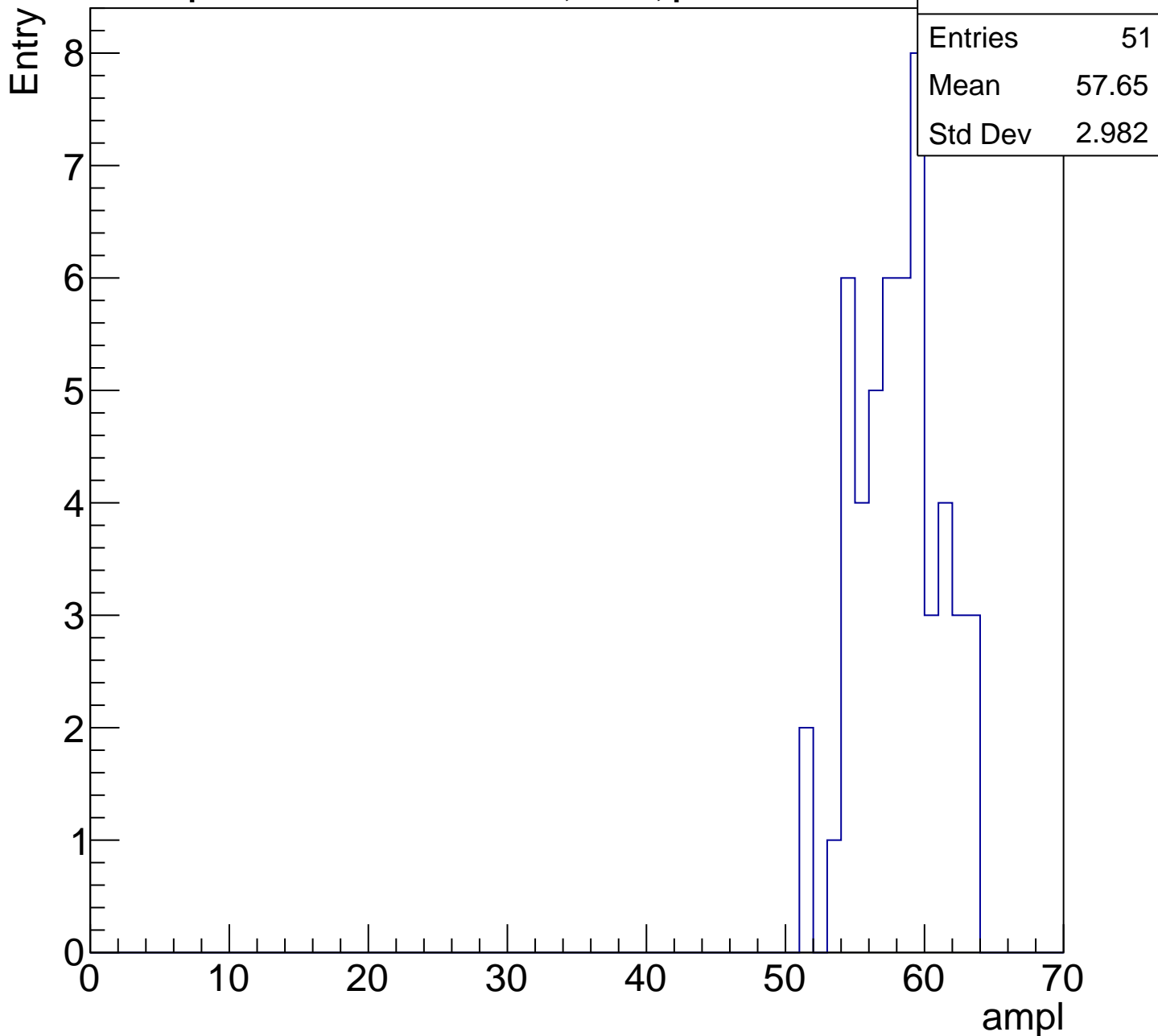
Entry

Entries	69
Mean	51.83
Std Dev	3.534



# B0L001S, U6-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

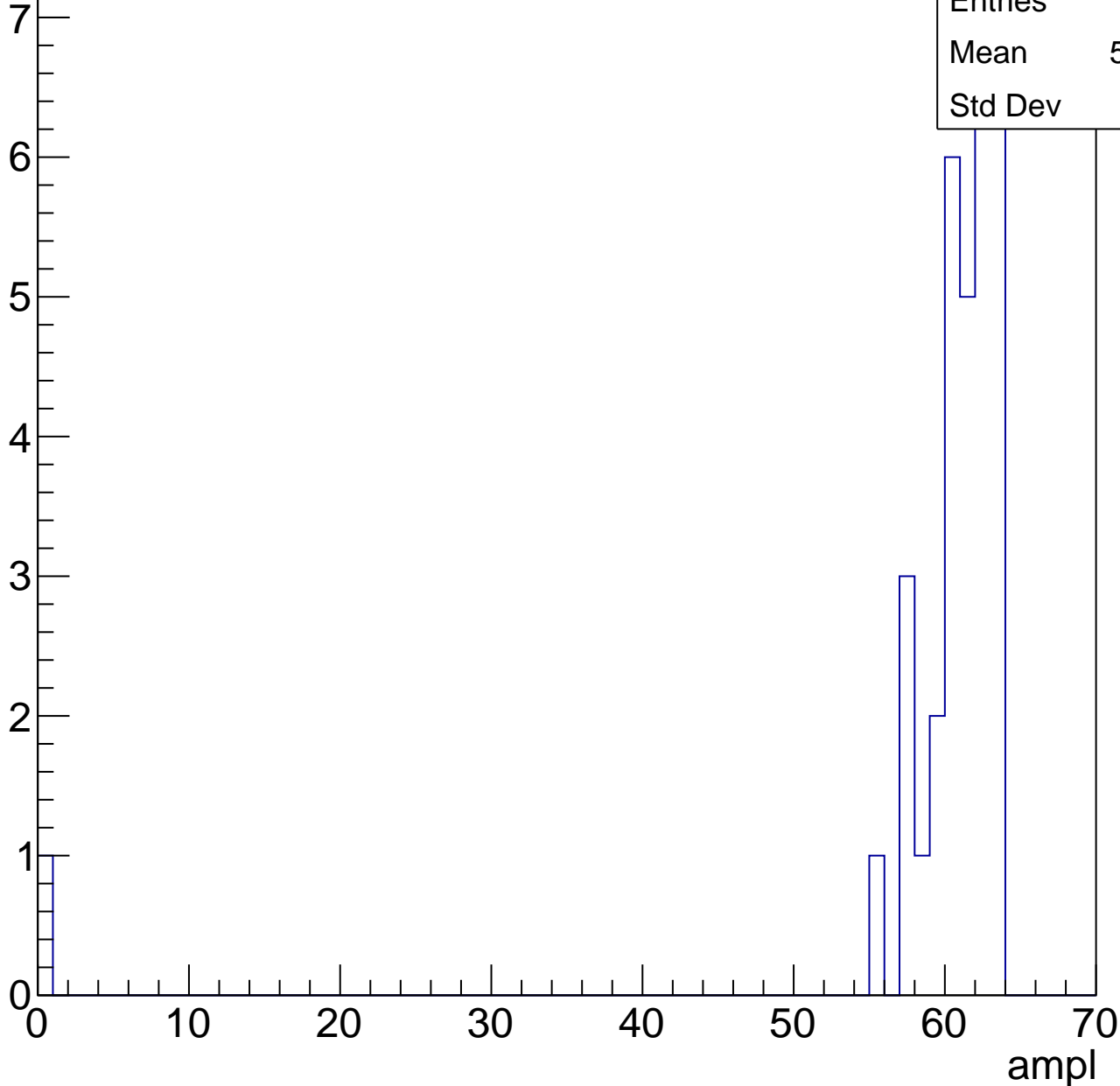


# B0L001S, U6-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	33
Mean	58.85
Std Dev	10.6



# B0L001S, U6-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U6-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch38, adc0

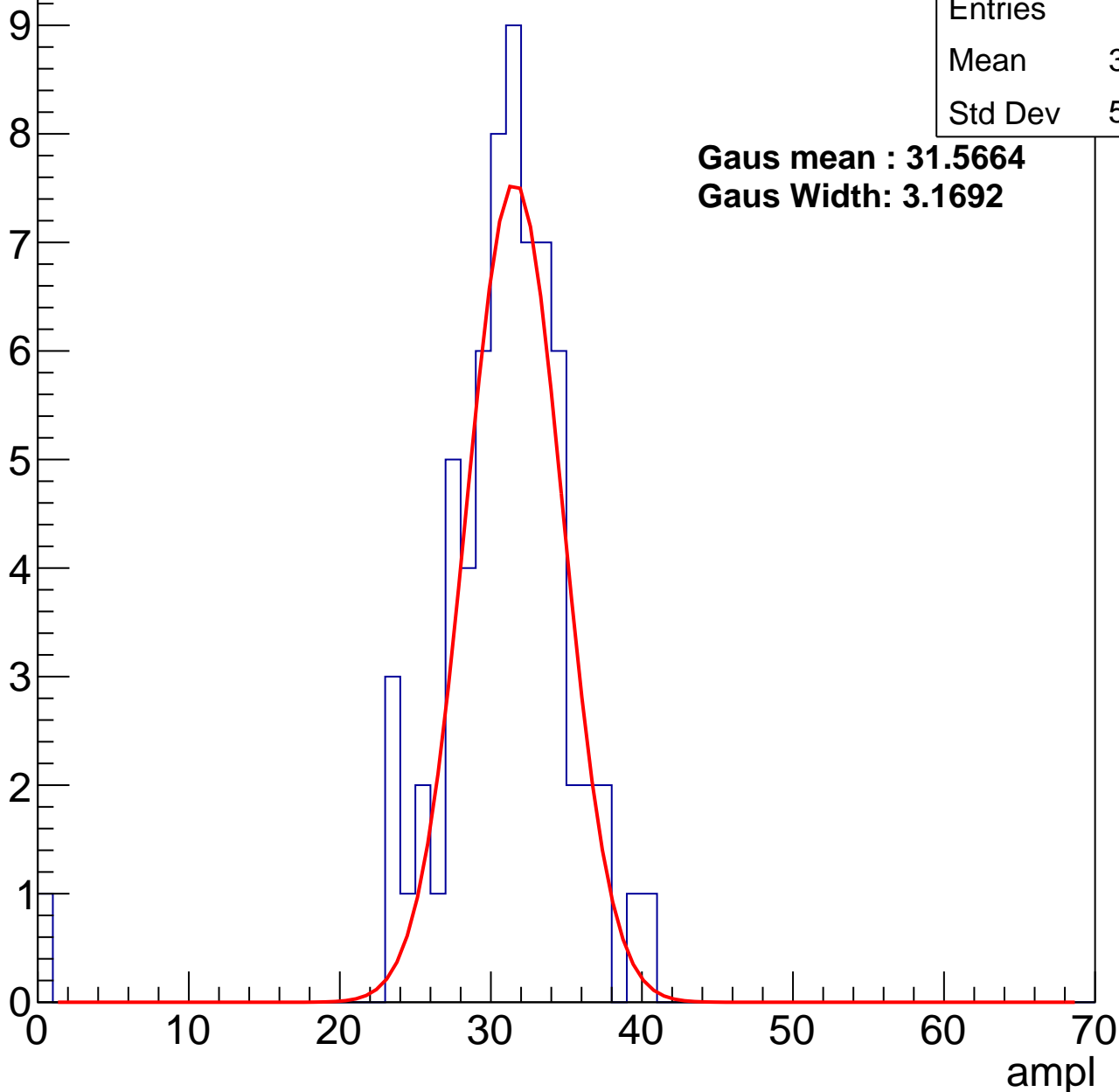
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	30.34
Std Dev	5.152

**Gaus mean : 31.5664**

**Gaus Width: 3.1692**



# B0L001S, U6-ch38, adc1

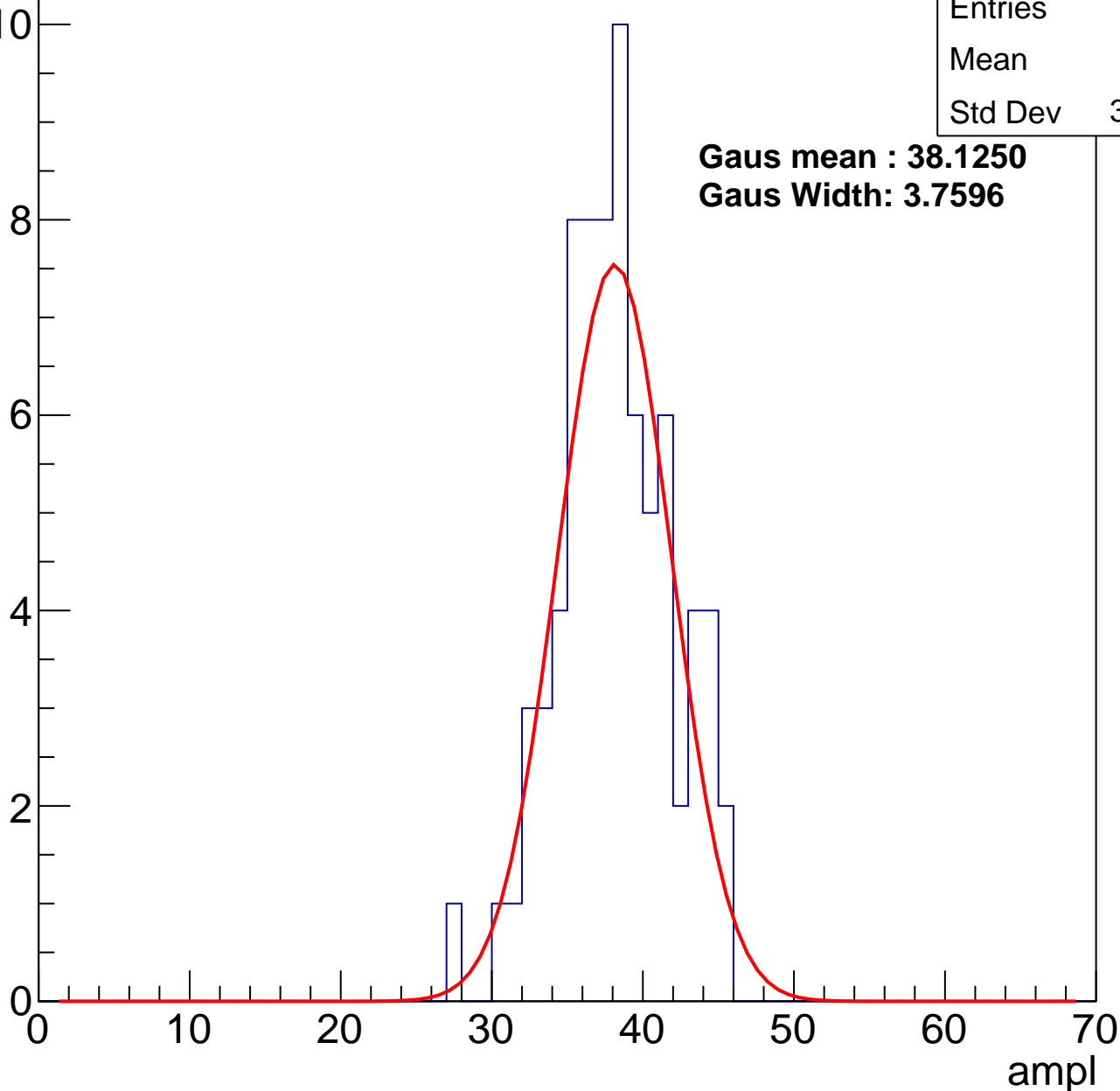
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	37.7
Std Dev	3.699

**Gaus mean : 38.1250**

**Gaus Width: 3.7596**



# B0L001S, U6-ch38, adc2

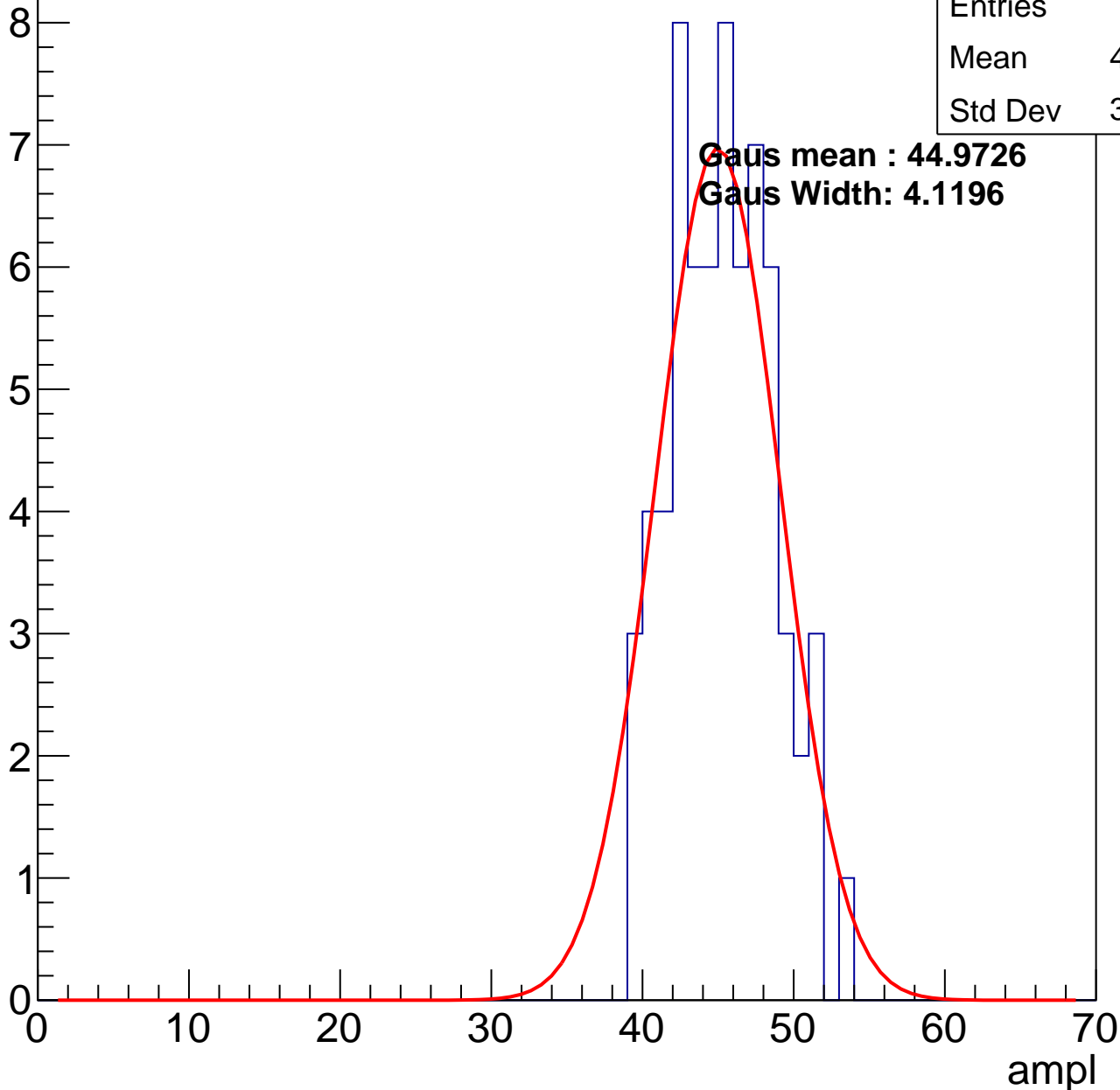
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	44.85
Std Dev	3.302

Gaus mean : 44.9726

Gaus Width: 4.1196

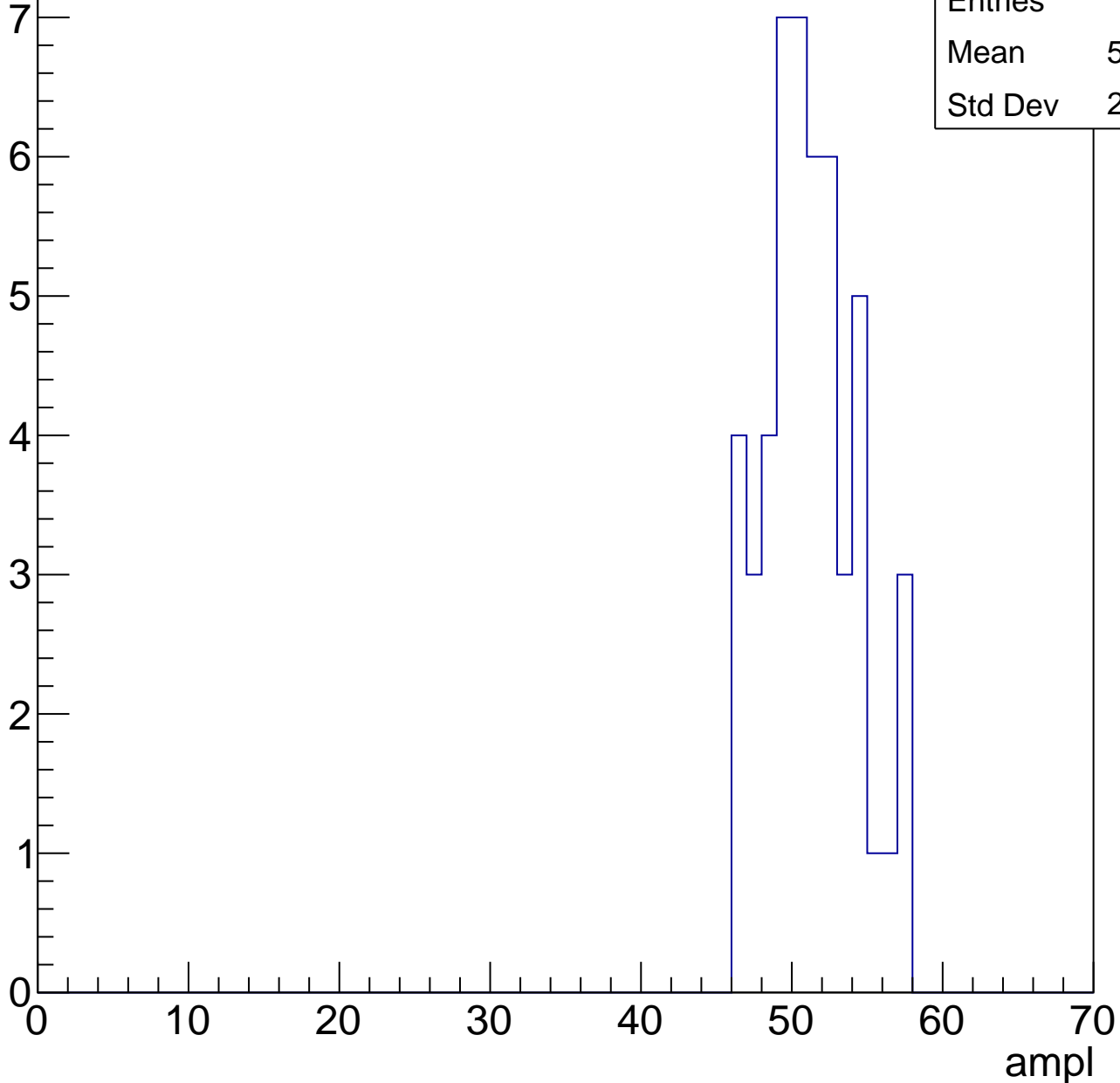


# B0L001S, U6-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

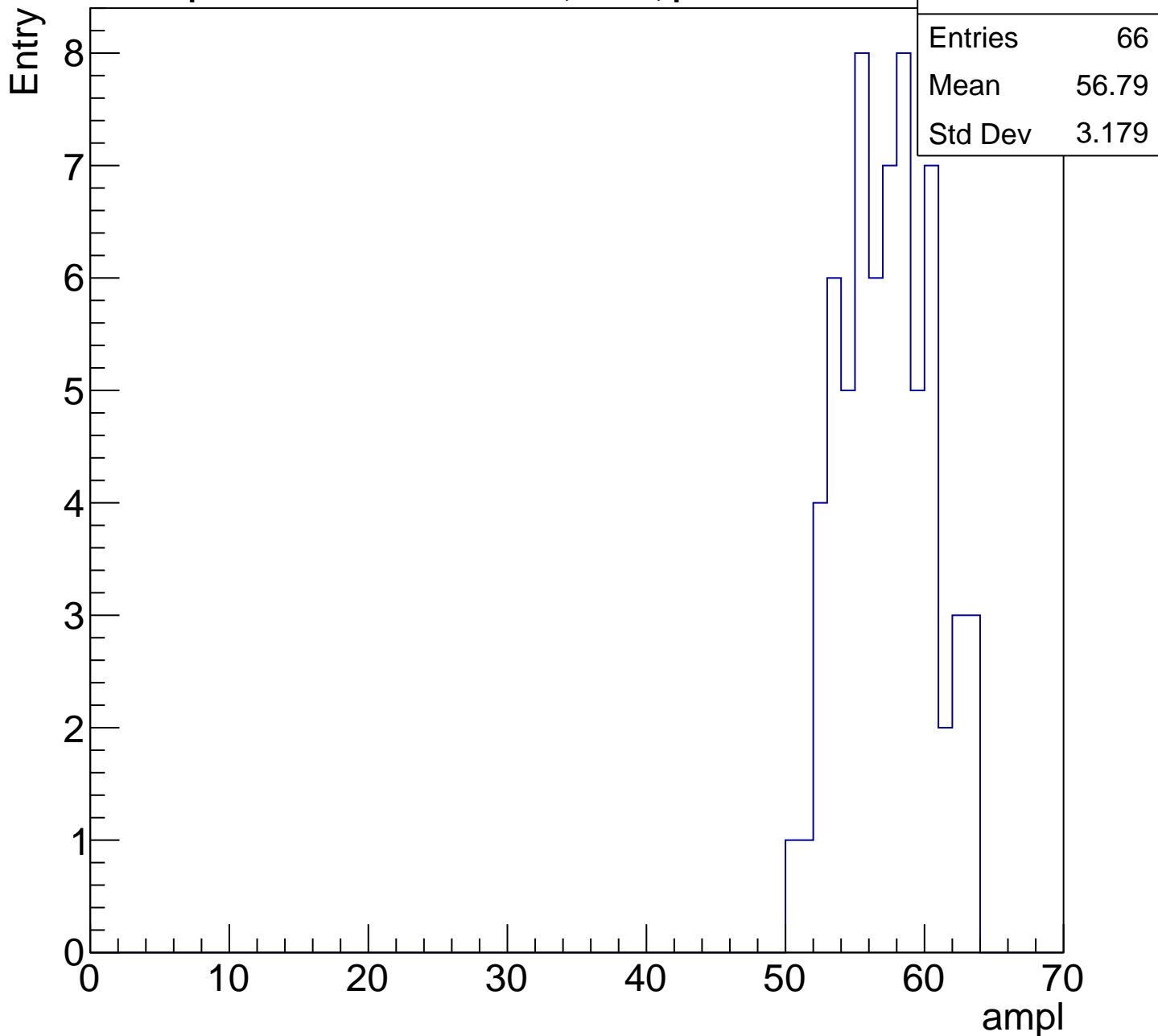
Entry

Entries	50
Mean	50.78
Std Dev	2.928



# B0L001S, U6-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

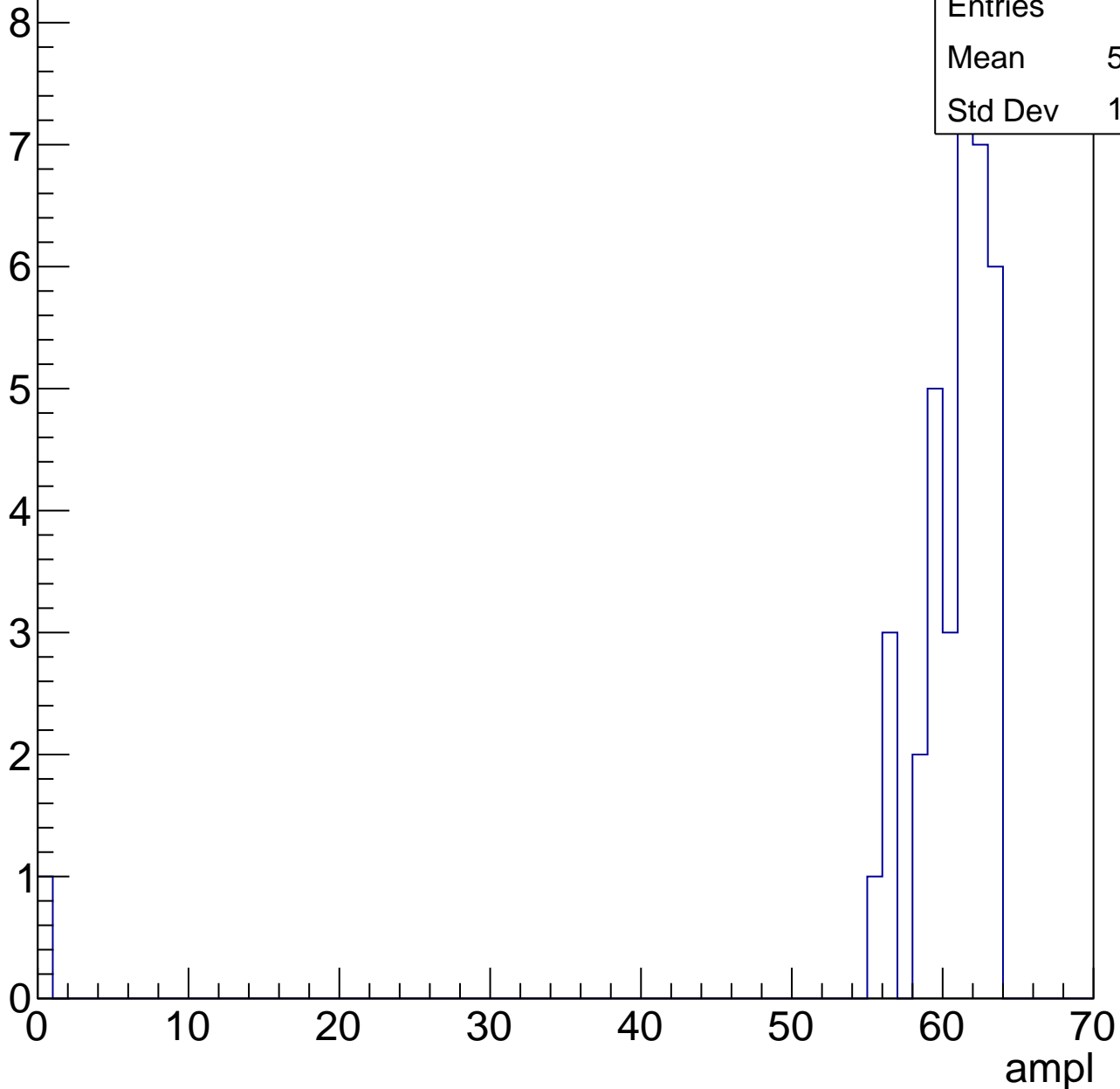


# B0L001S, U6-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	36
Mean	58.72
Std Dev	10.16



# B0L001S, U6-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U6-ch39, adc0

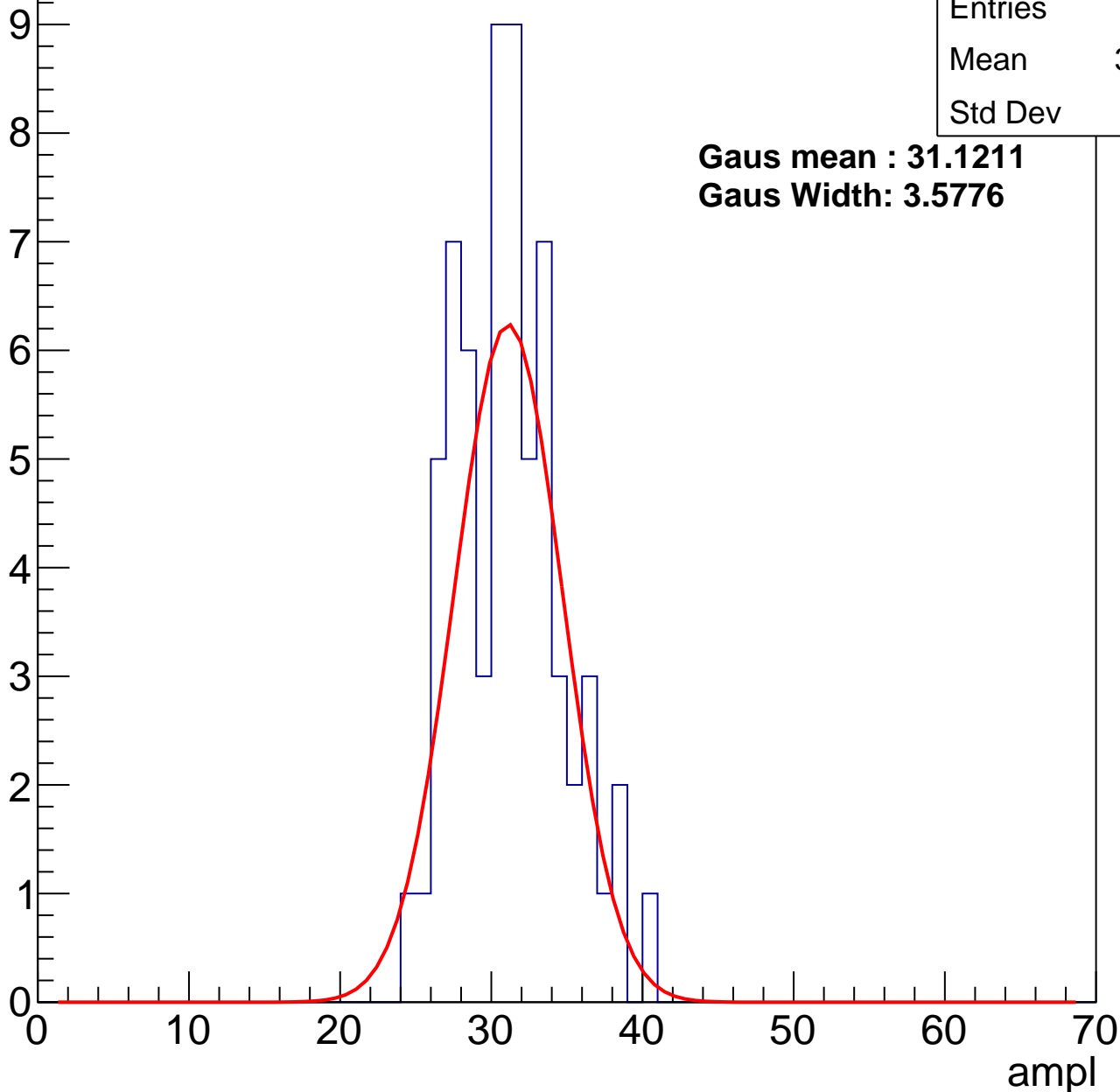
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	30.71
Std Dev	3.45

**Gaus mean : 31.1211**

**Gaus Width: 3.5776**



# B0L001S, U6-ch39, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	79
Mean	37.71
Std Dev	3.487

**Gaus mean : 38.1289**

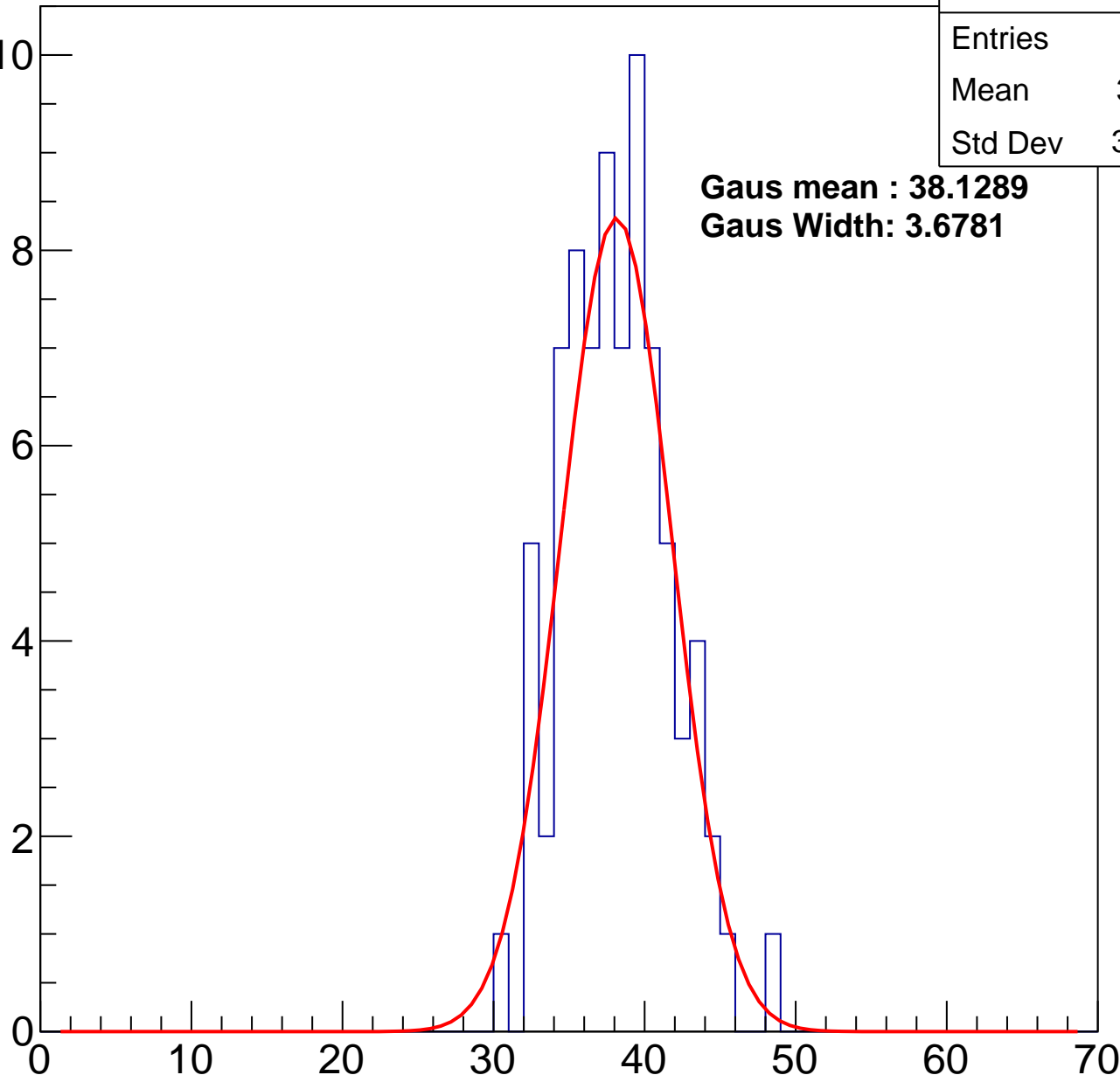
**Gaus Width: 3.6781**

Entry

10  
8  
6  
4  
2  
0

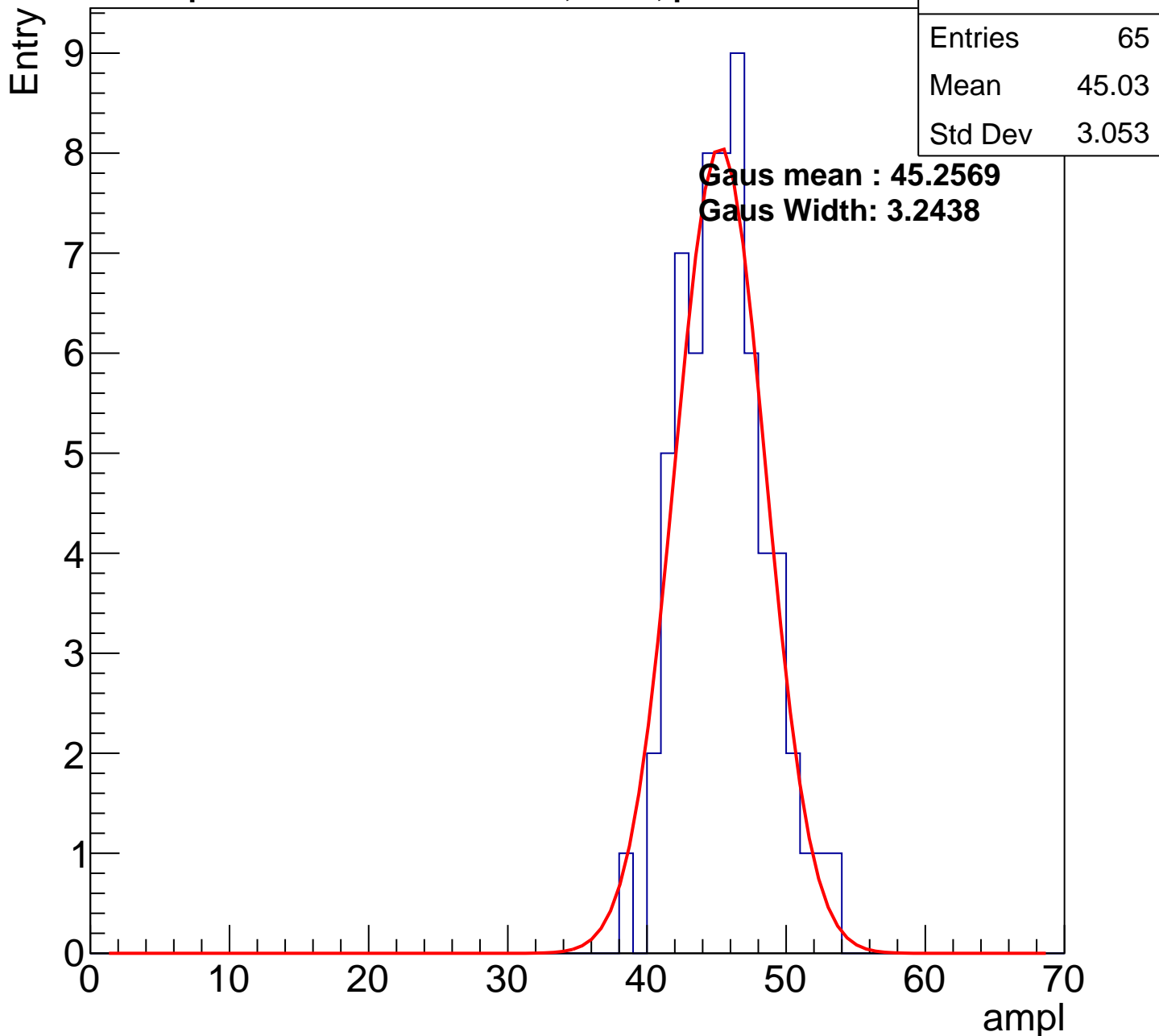
0 10 20 30 40 50 60 70

ampl



# B0L001S, U6-ch39, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

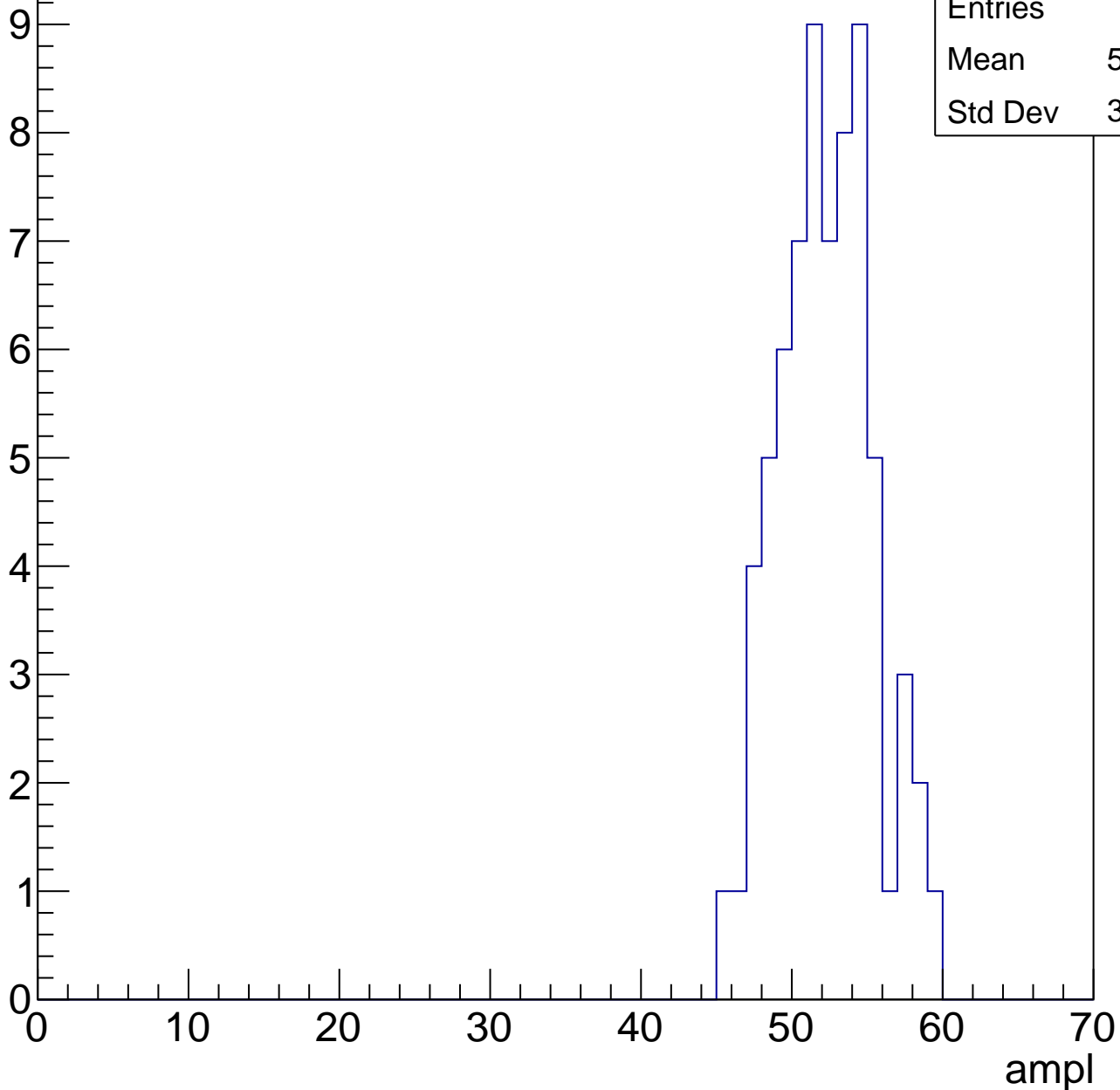


# B0L001S, U6-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

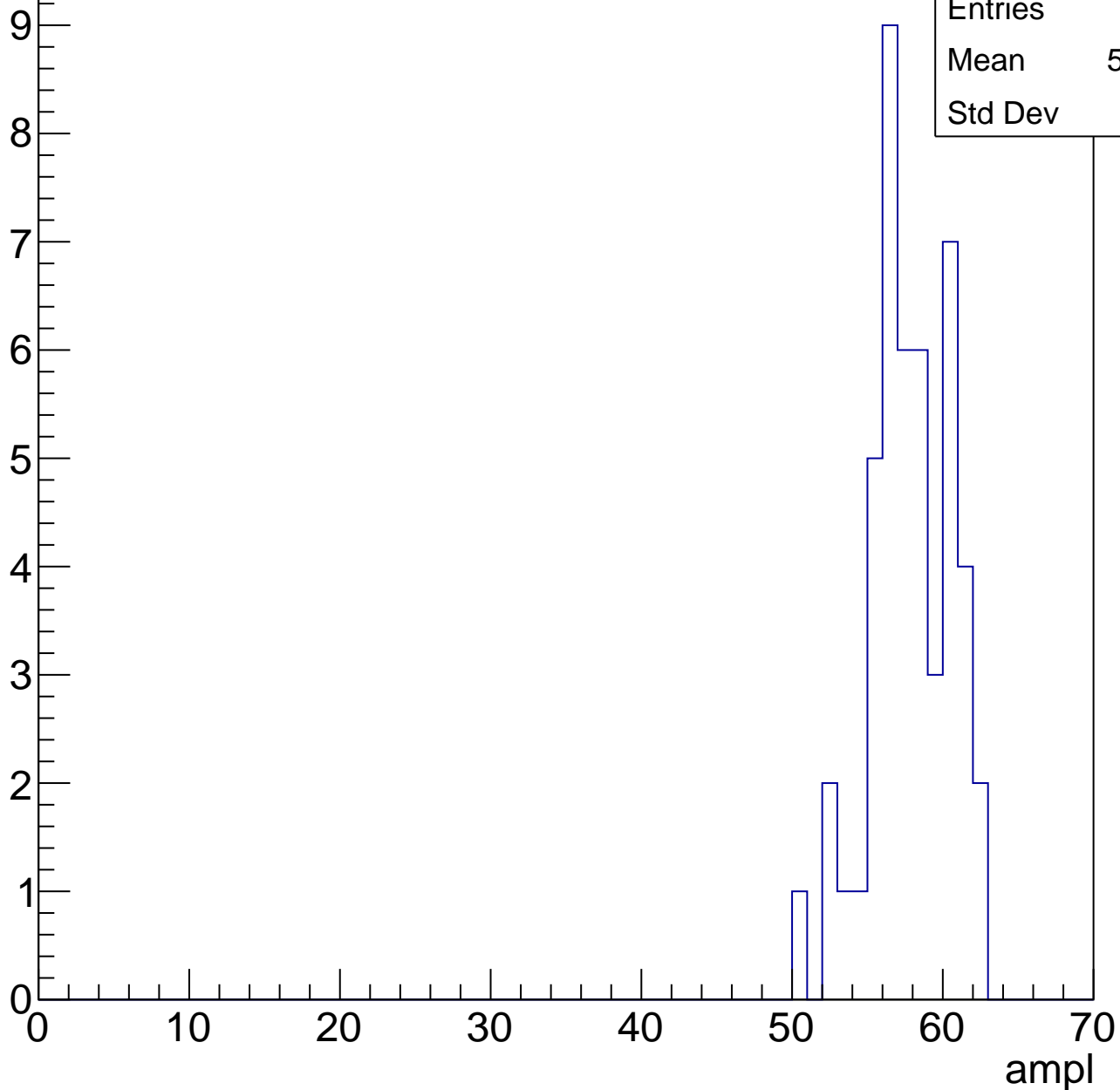
Entries	69
Mean	51.78
Std Dev	3.078



# B0L001S, U6-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



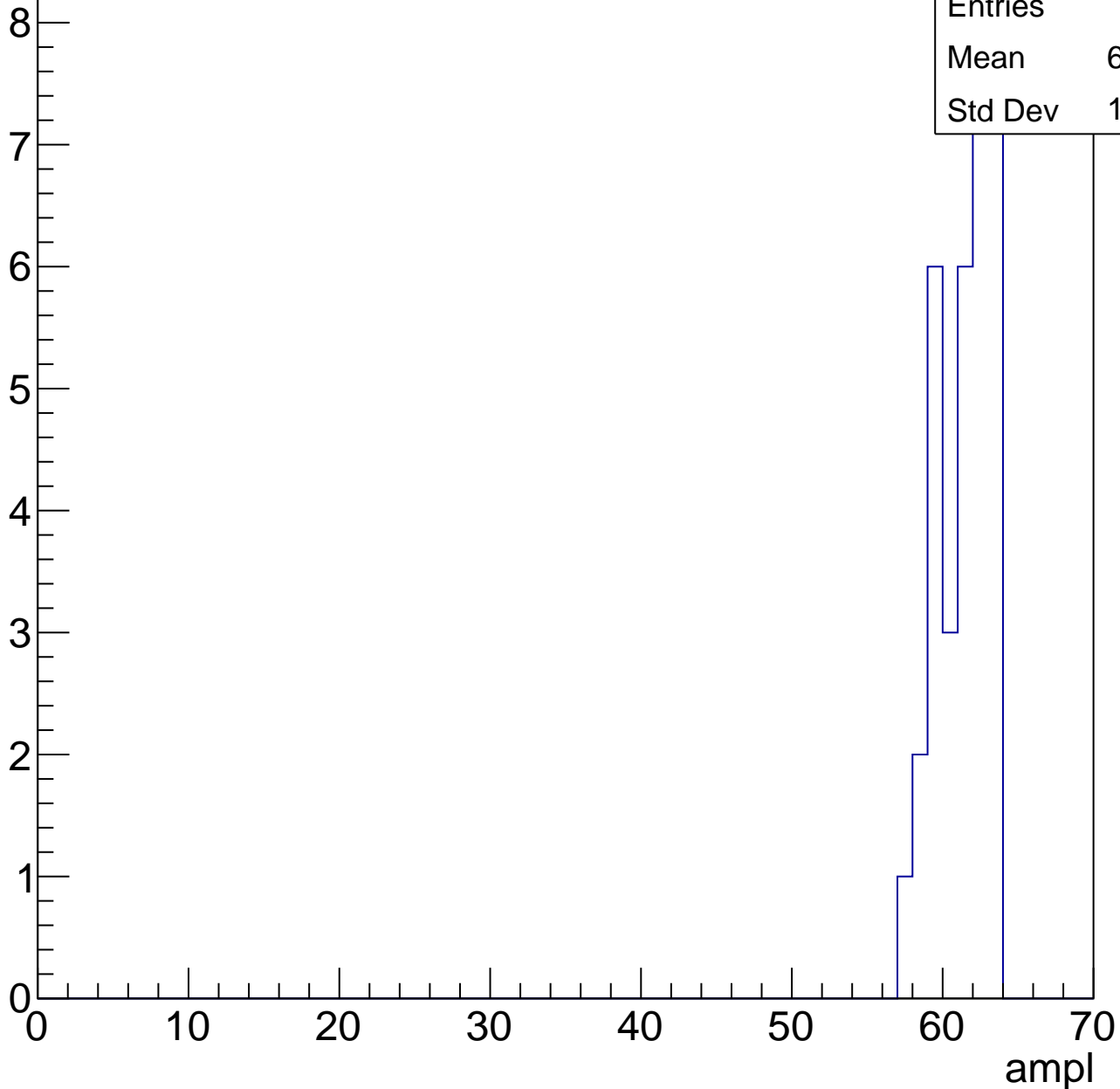
Entries	47
Mean	57.34
Std Dev	2.7

# B0L001S, U6-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	34
Mean	60.97
Std Dev	1.723



# B0L001S, U6-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U6-ch40, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	74
Mean	29.69
Std Dev	4.658

**Gaus mean : 30.3470**

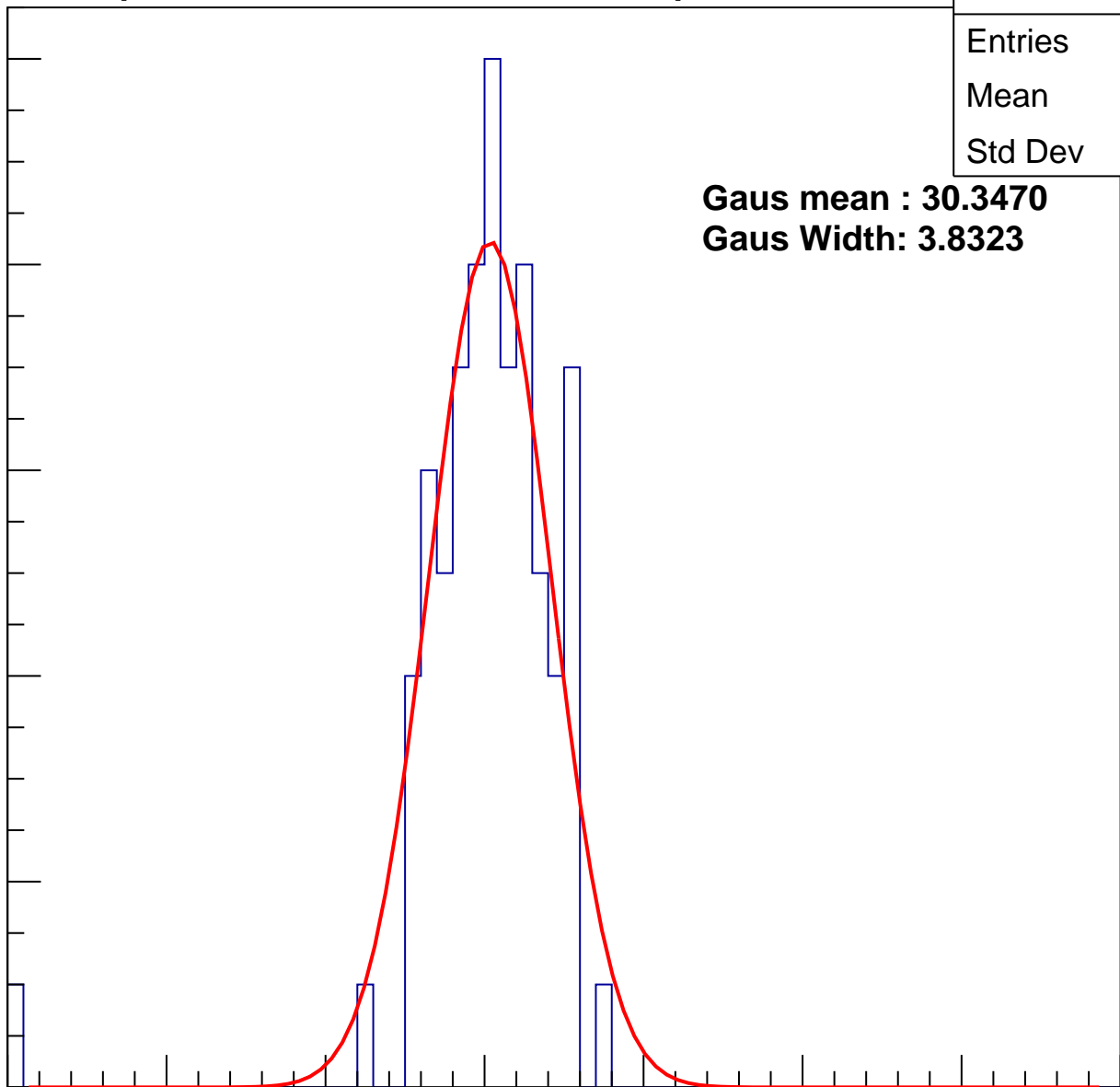
**Gaus Width: 3.8323**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U6-ch40, adc1

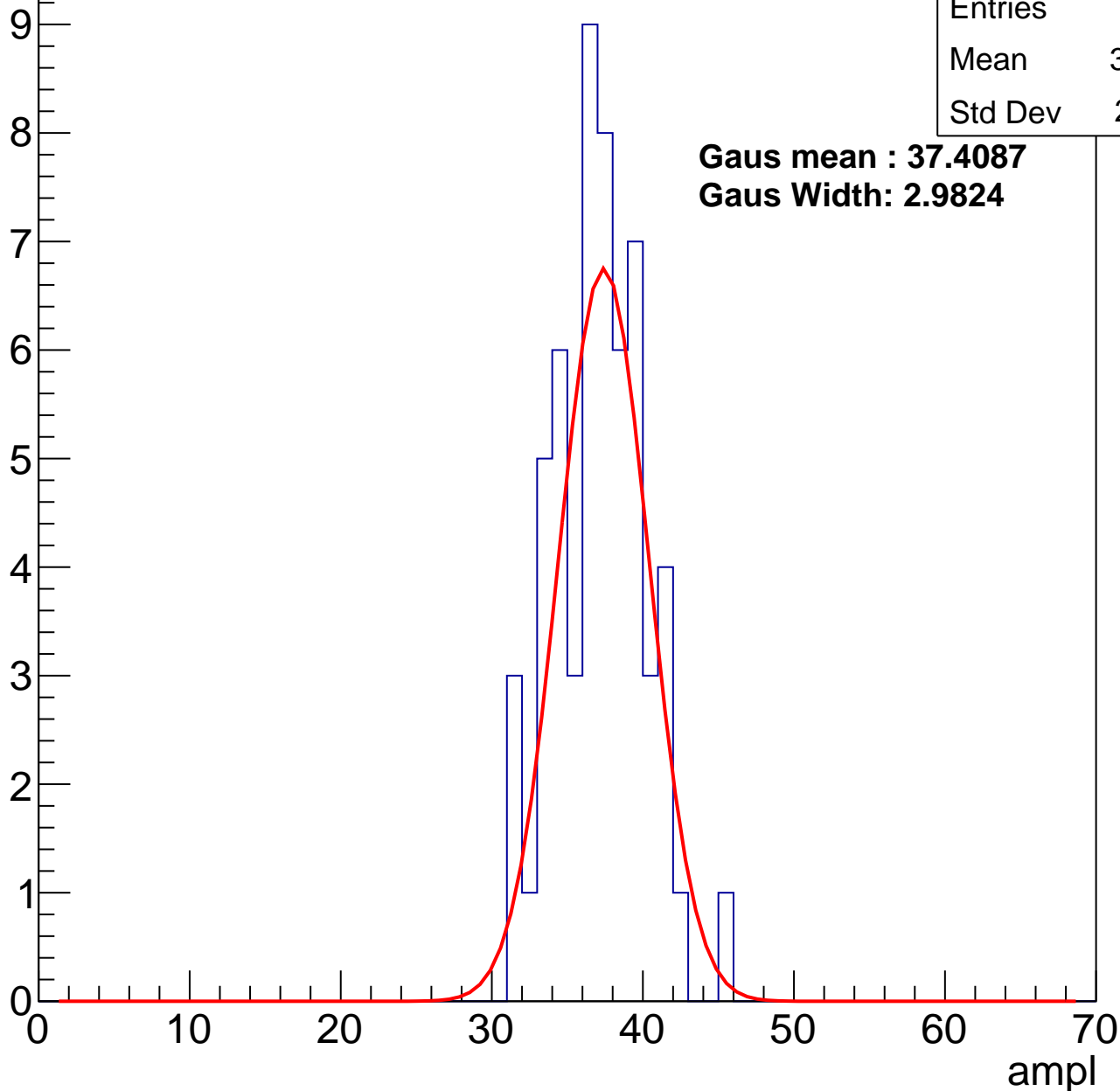
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	36.68
Std Dev	2.951

**Gaus mean : 37.4087**

**Gaus Width: 2.9824**



# B0L001S, U6-ch40, adc2

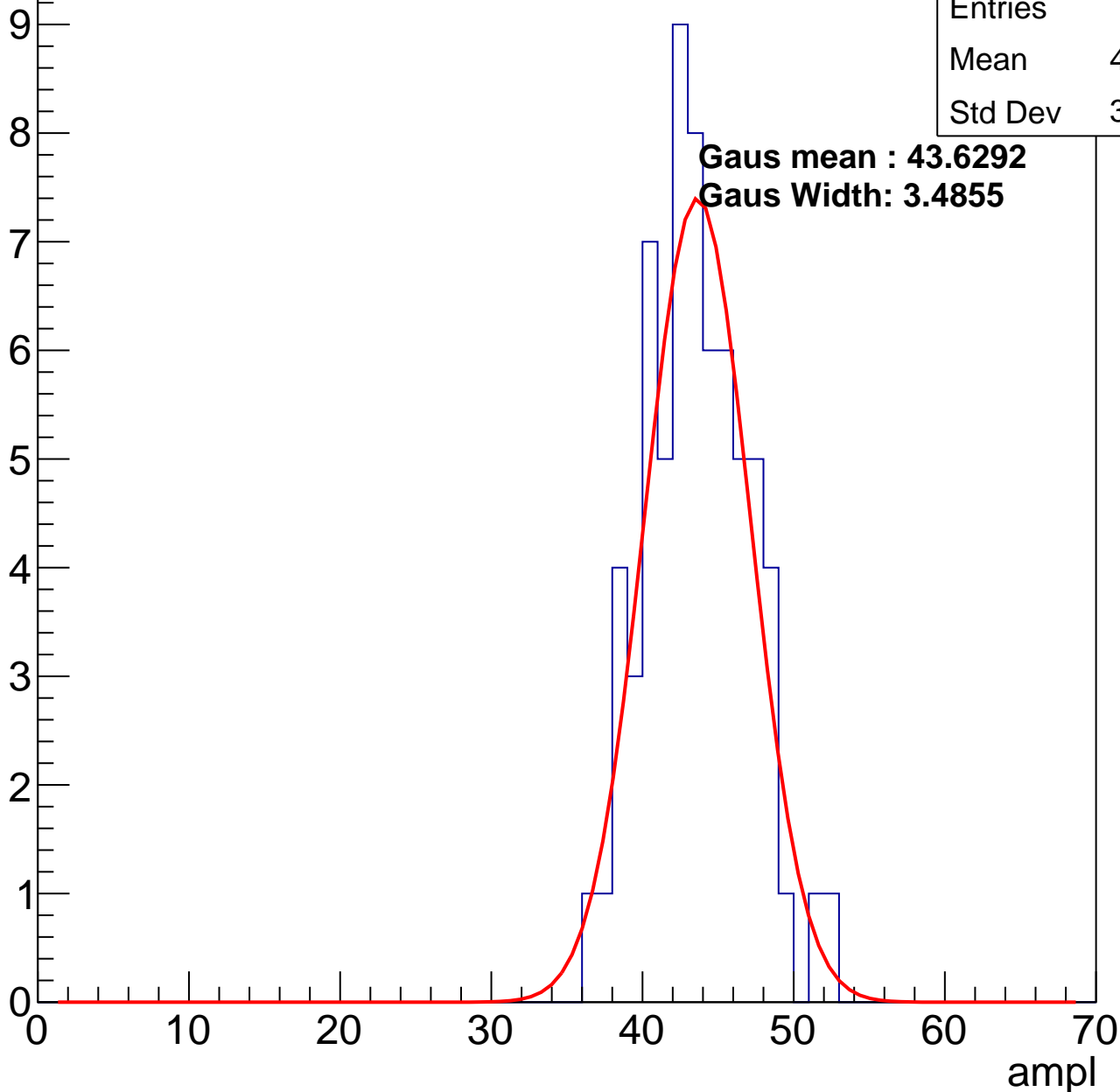
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	43.16
Std Dev	3.366

**Gaus mean : 43.6292**

**Gaus Width: 3.4855**

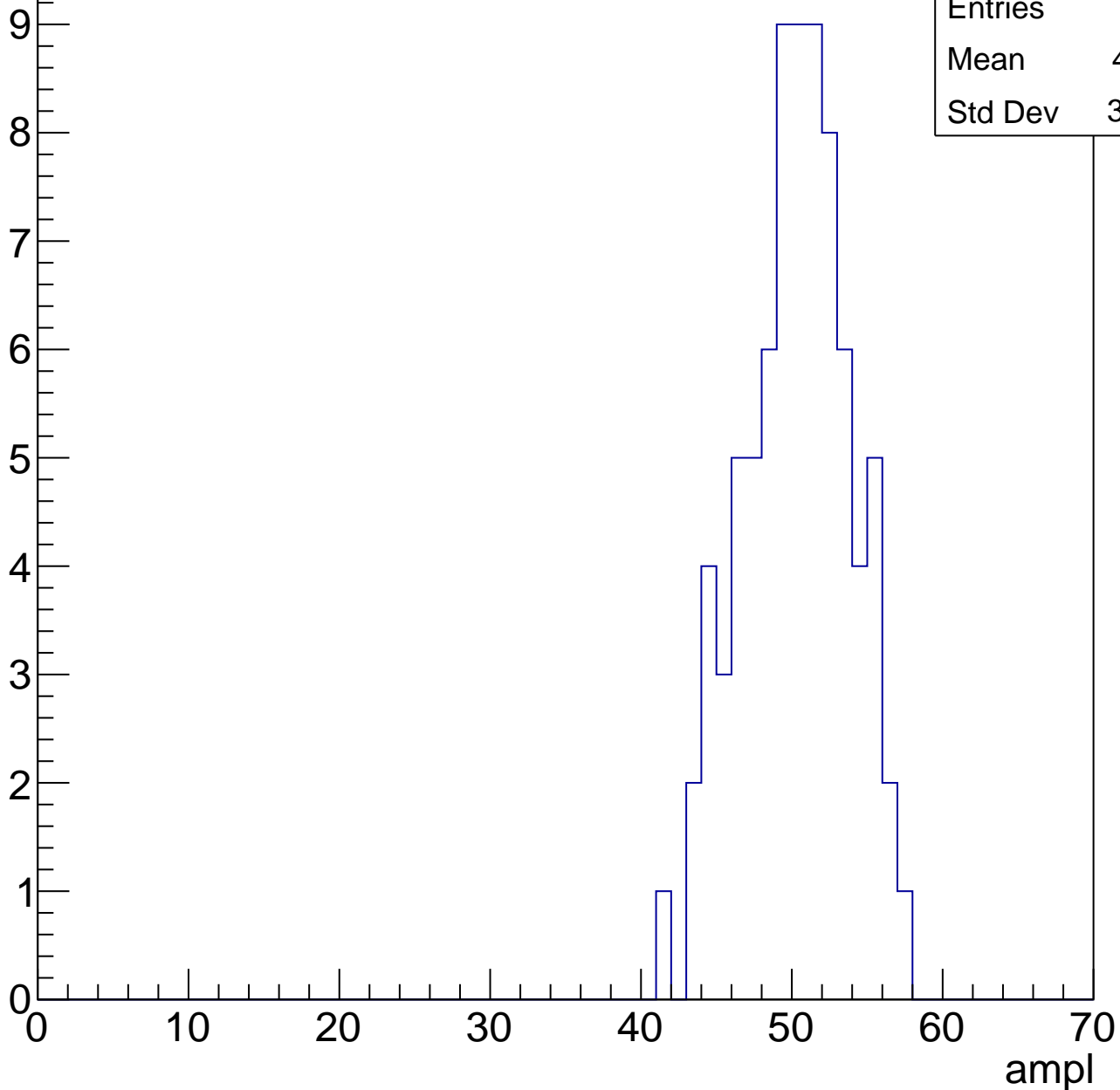


# B0L001S, U6-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	49.81
Std Dev	3.483

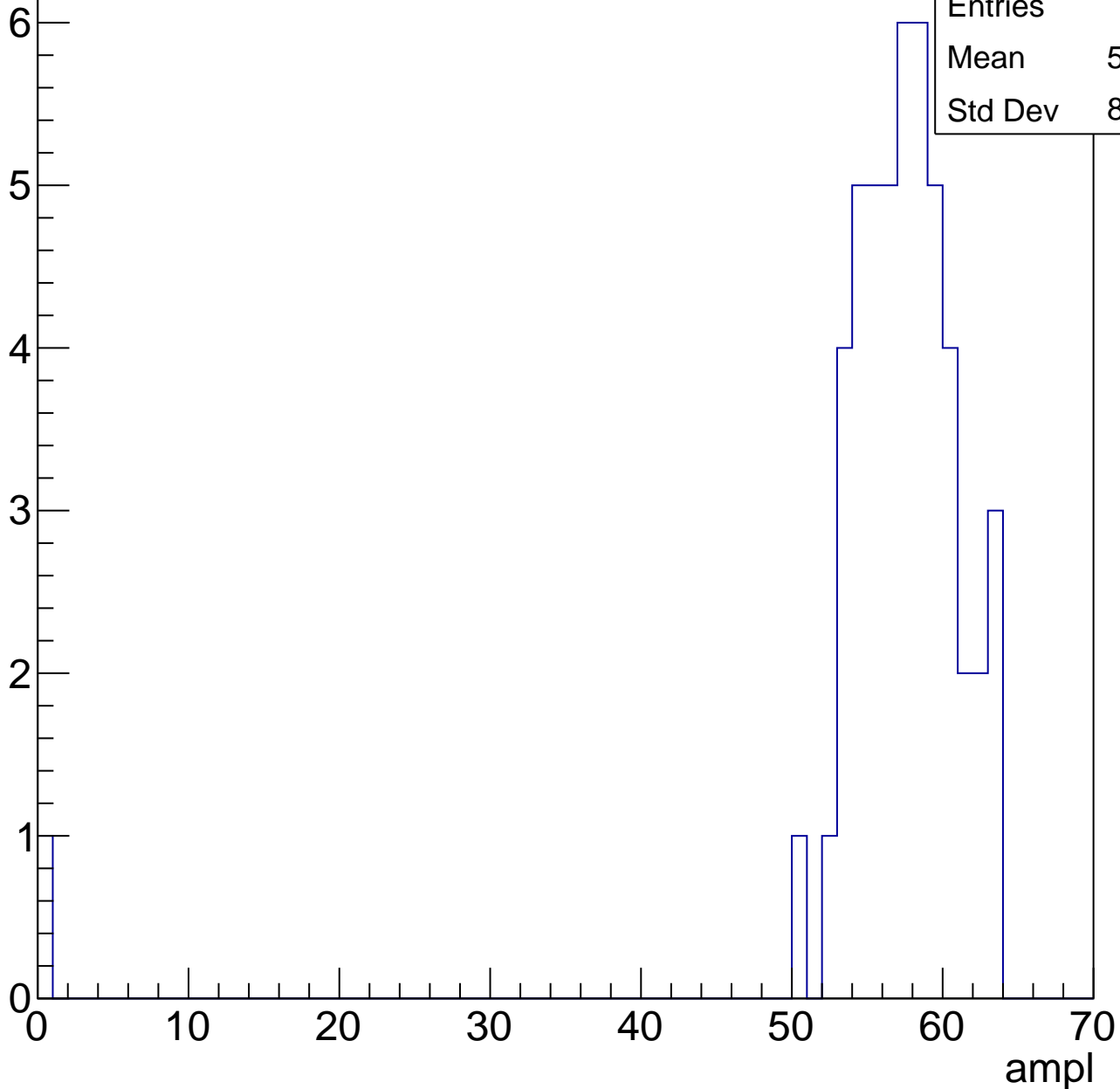


# B0L001S, U6-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	55.98
Std Dev	8.552

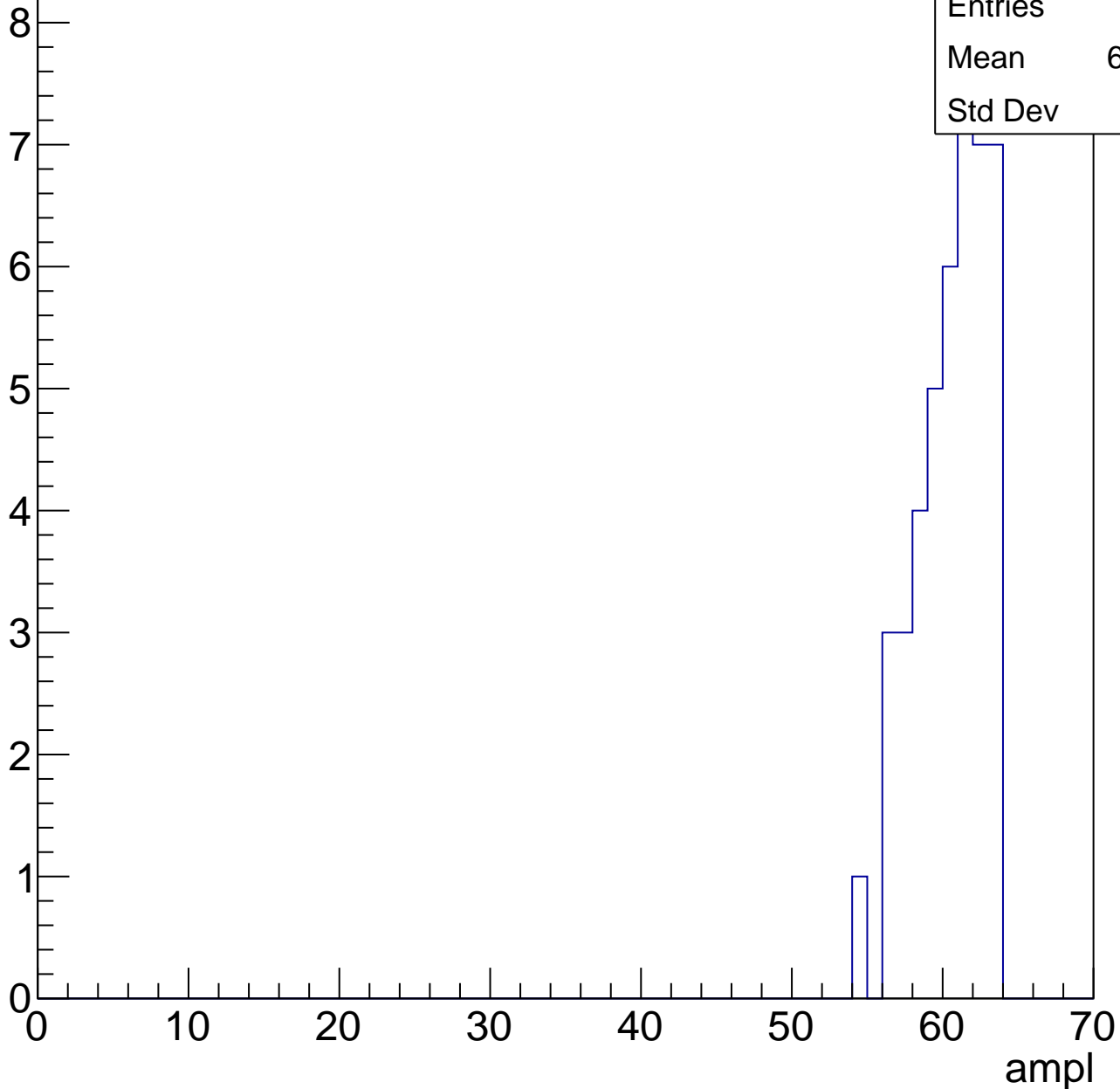


# B0L001S, U6-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	44
Mean	60.07
Std Dev	2.29



# B0L001S, U6-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	62
Std Dev	0

ampl



# B0L001S, U6-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U6-ch41, adc0

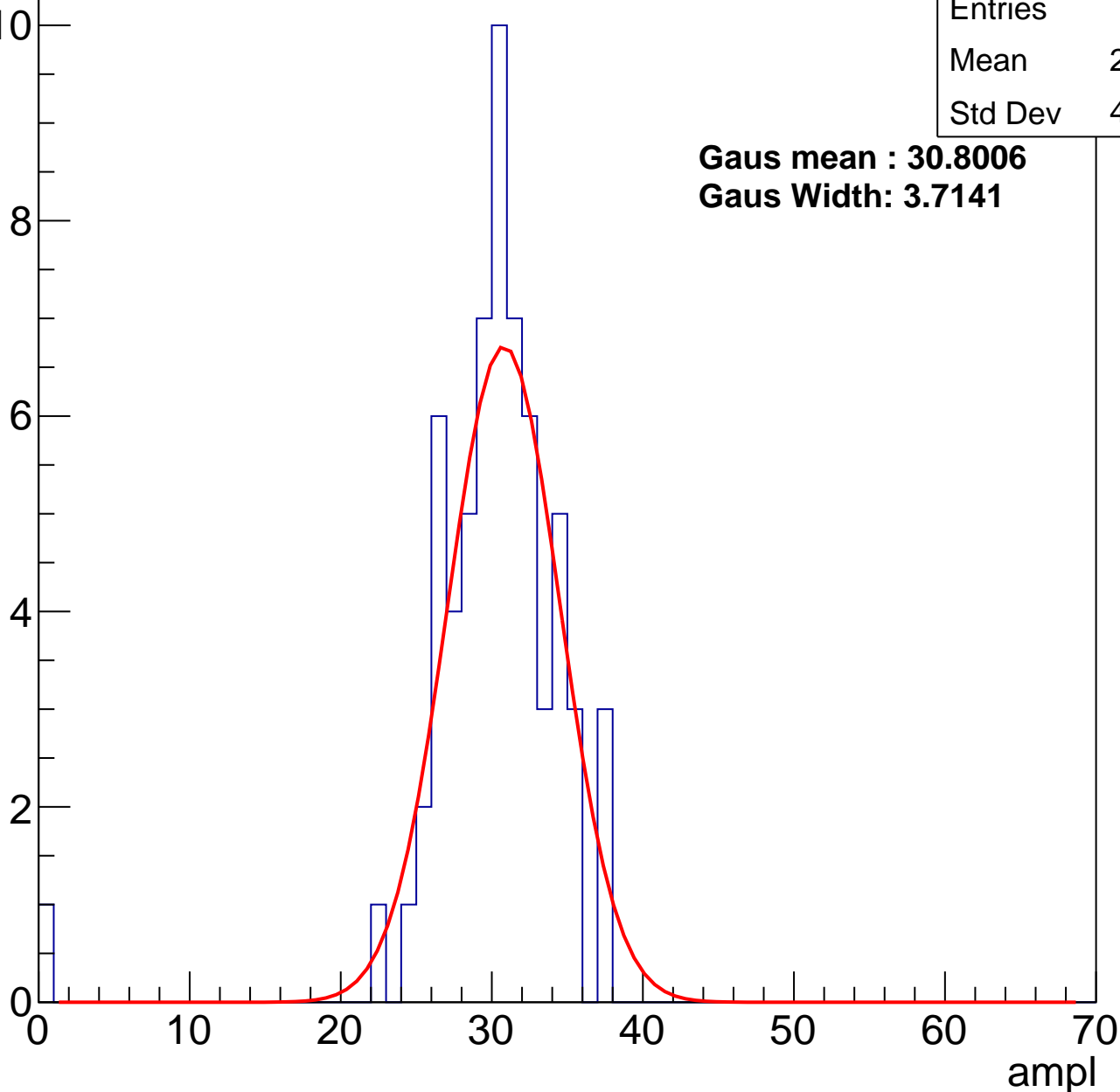
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	29.64
Std Dev	4.938

**Gaus mean : 30.8006**

**Gaus Width: 3.7141**



# B0L001S, U6-ch41, adc1

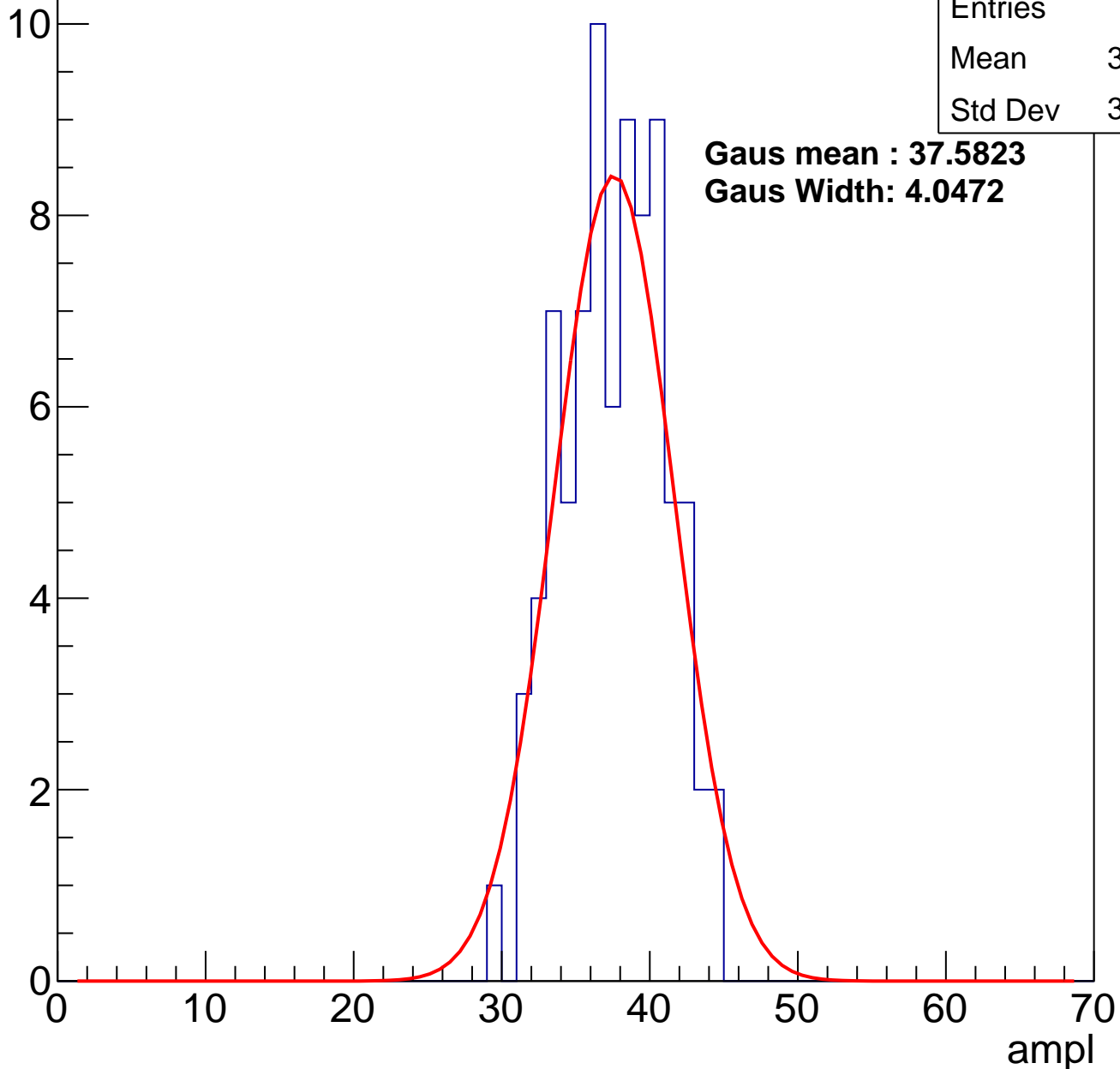
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	83
Mean	37.12
Std Dev	3.406

**Gaus mean : 37.5823**

**Gaus Width: 4.0472**

Entry



# B0L001S, U6-ch41, adc2

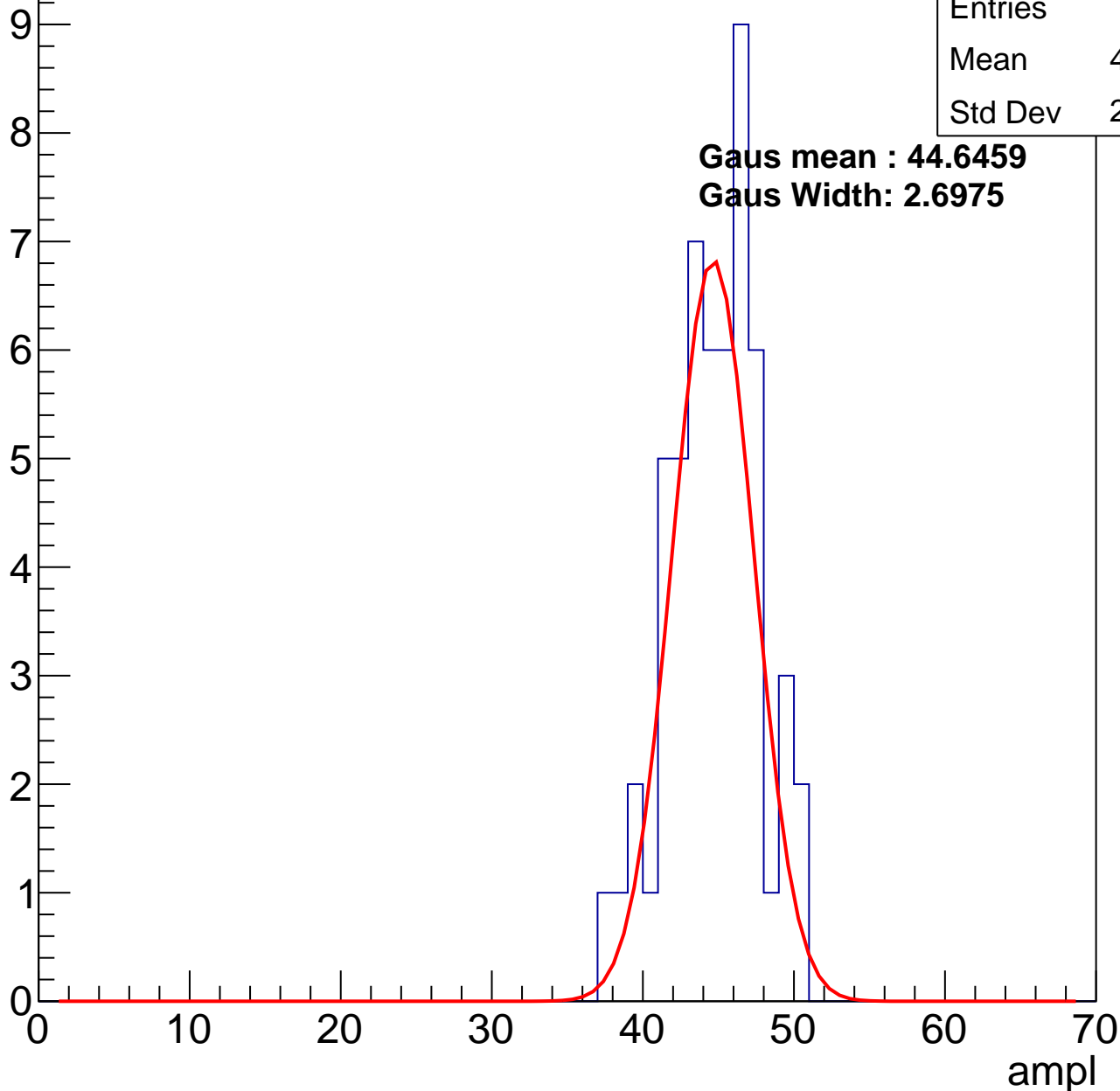
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	44.25
Std Dev	2.949

**Gaus mean : 44.6459**

**Gaus Width: 2.6975**

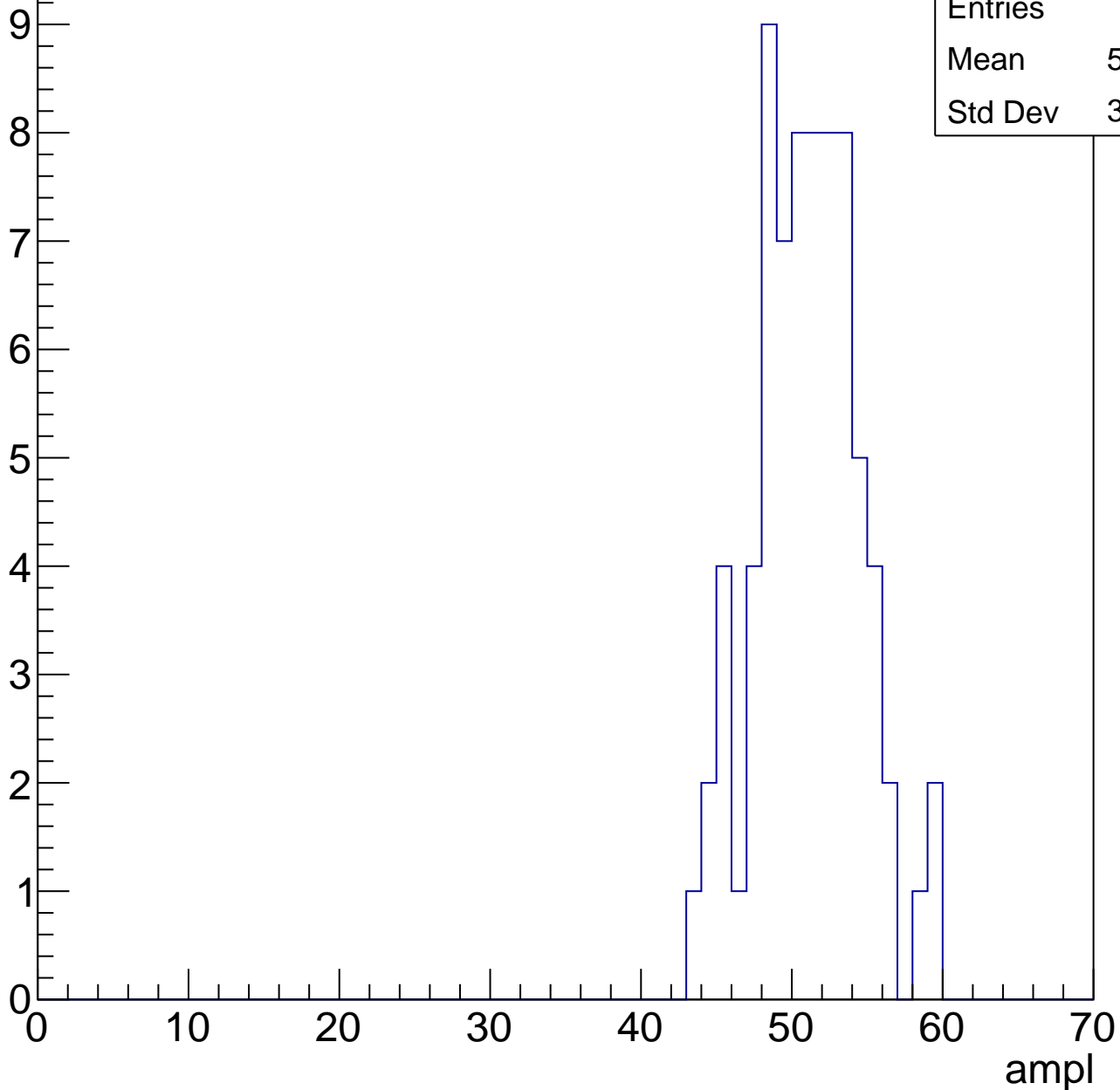


# B0L001S, U6-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

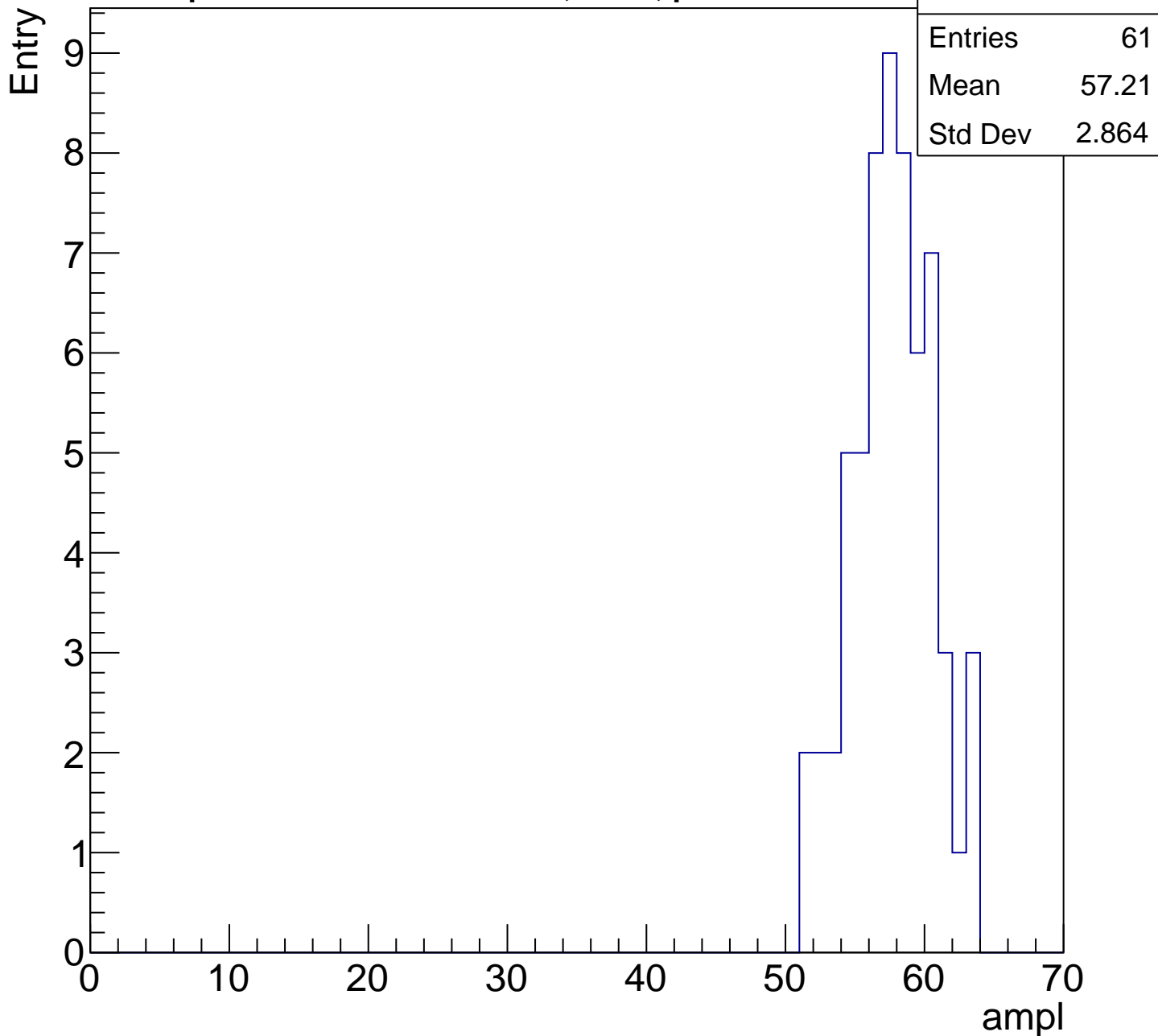
Entry

Entries	74
Mean	50.62
Std Dev	3.443



# B0L001S, U6-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

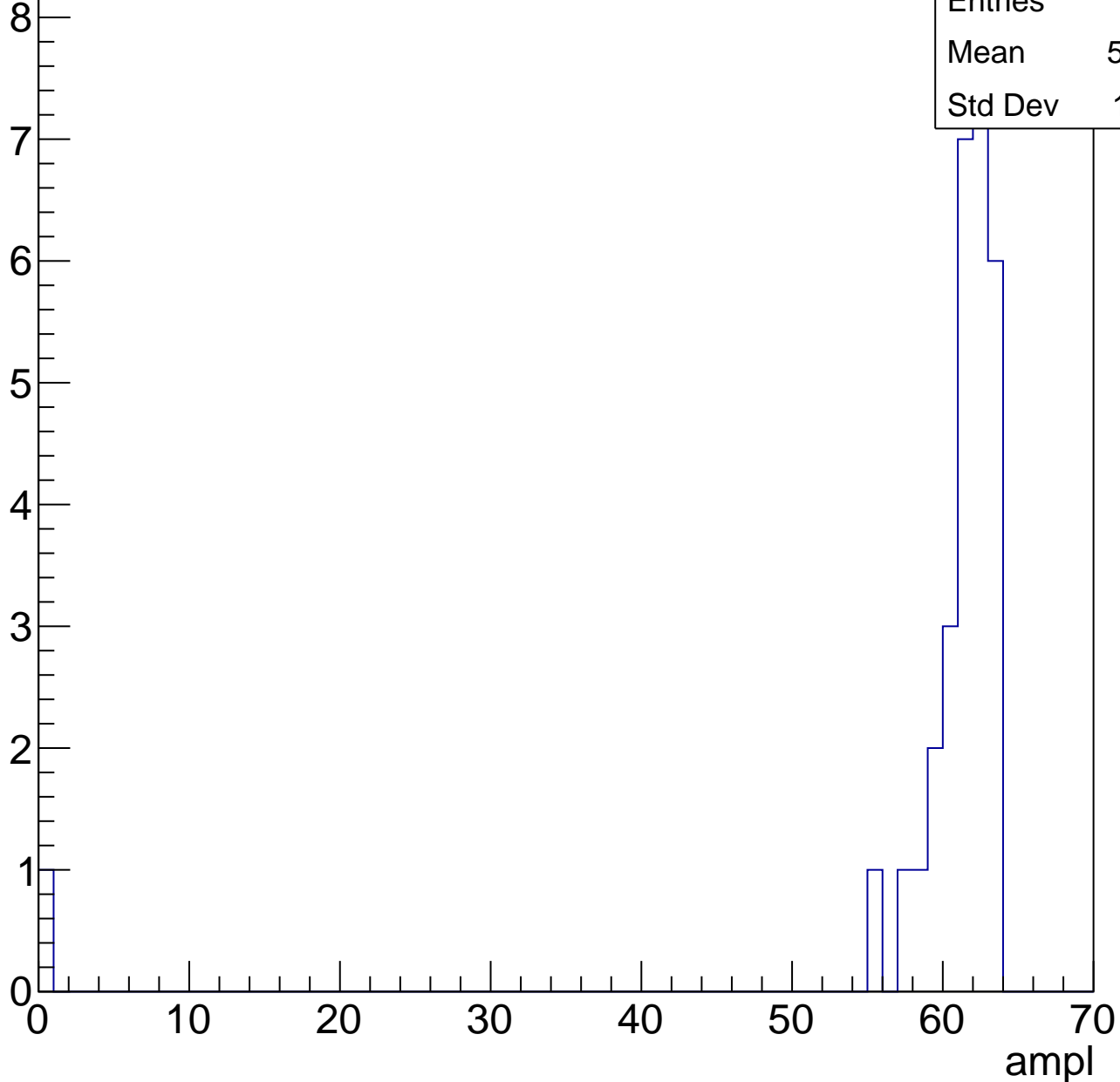


# B0L001S, U6-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	30
Mean	58.97
Std Dev	11.11



# B0L001S, U6-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch42, adc0

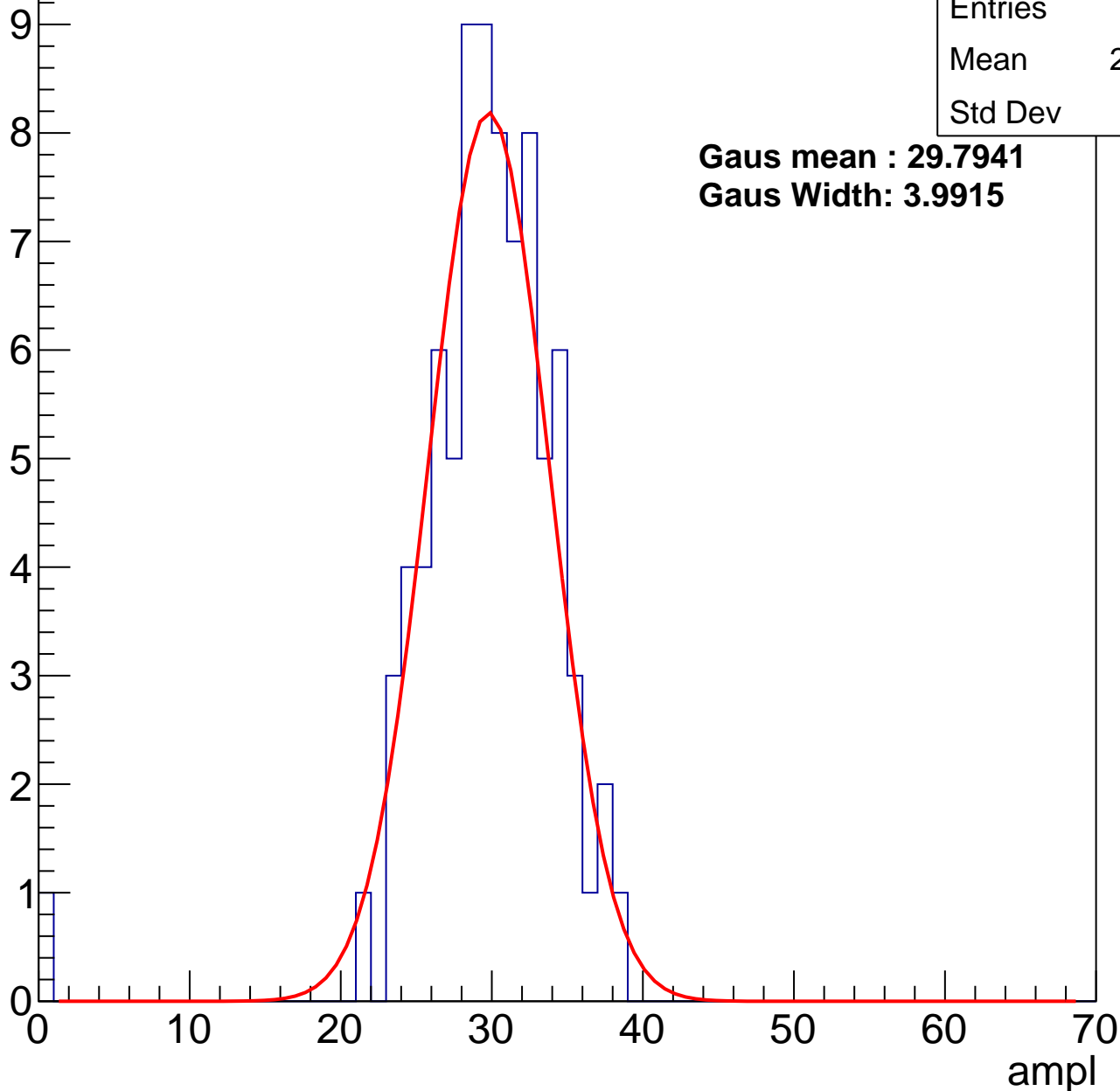
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	83
Mean	29.22
Std Dev	4.86

**Gaus mean : 29.7941**

**Gaus Width: 3.9915**



# B0L001S, U6-ch42, adc1

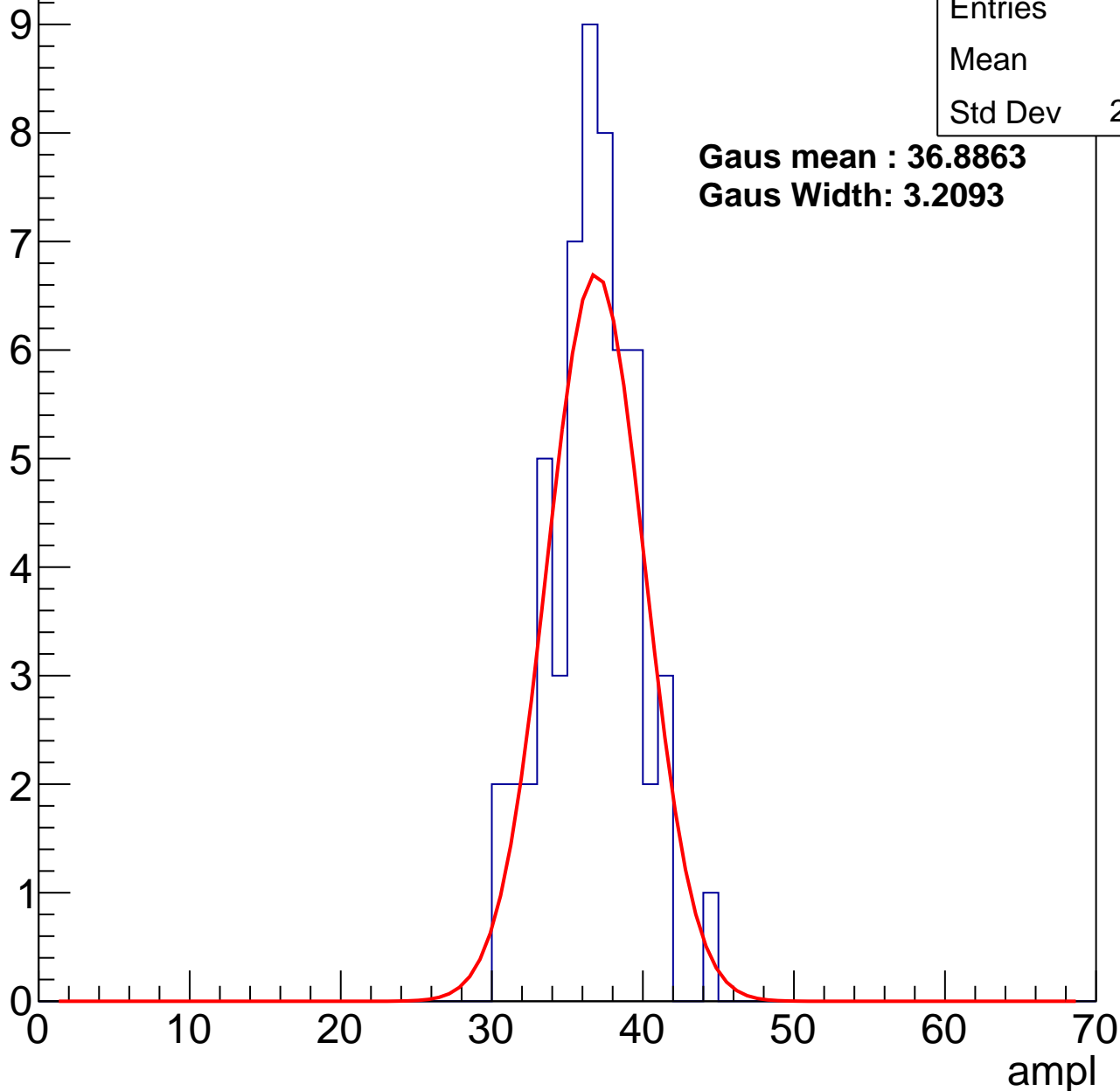
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	36.2
Std Dev	2.906

**Gaus mean : 36.8863**

**Gaus Width: 3.2093**



# B0L001S, U6-ch42, adc2

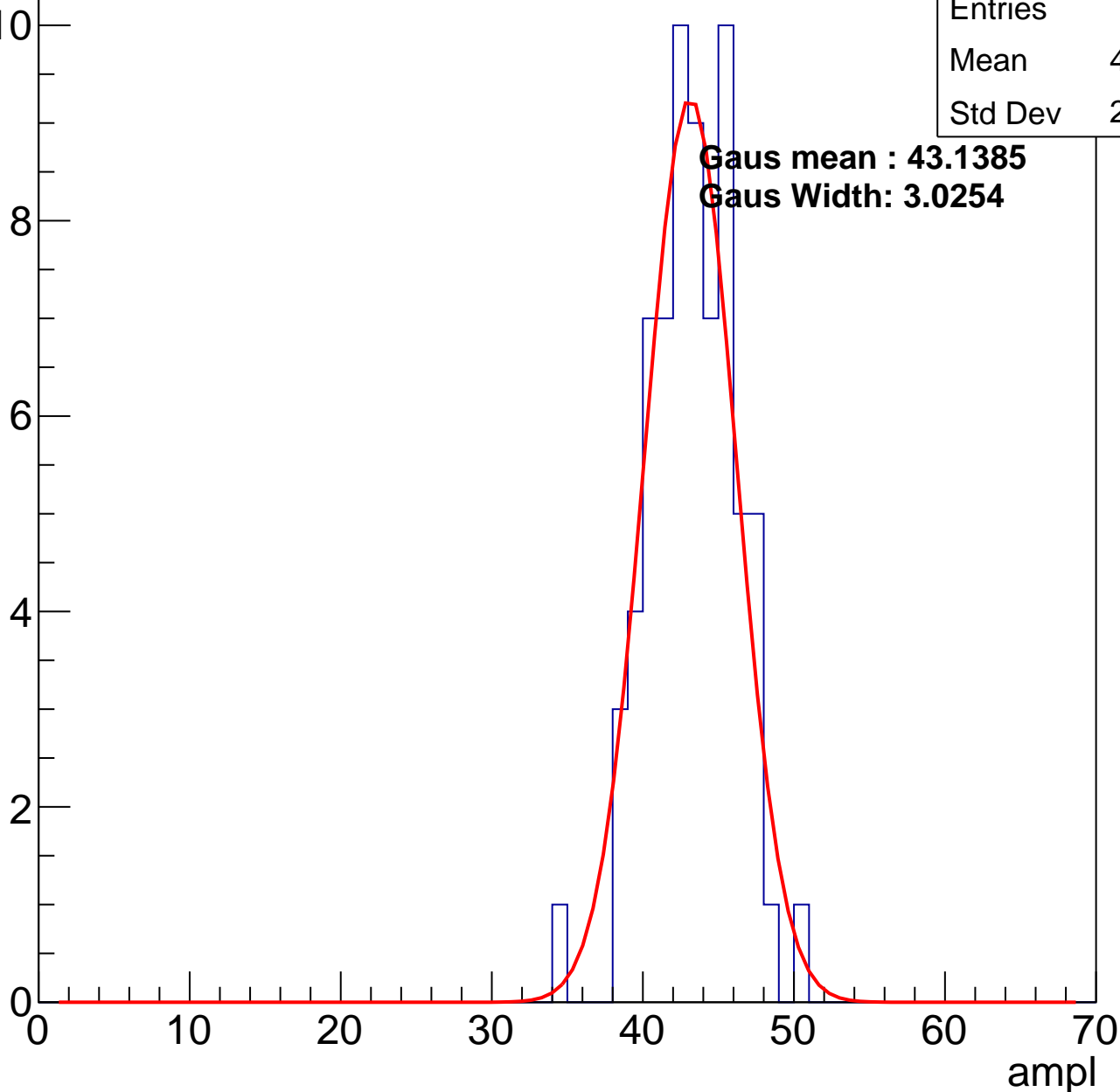
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	42.84
Std Dev	2.842

**Gaus mean : 43.1385**

**Gaus Width: 3.0254**



# B0L001S, U6-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

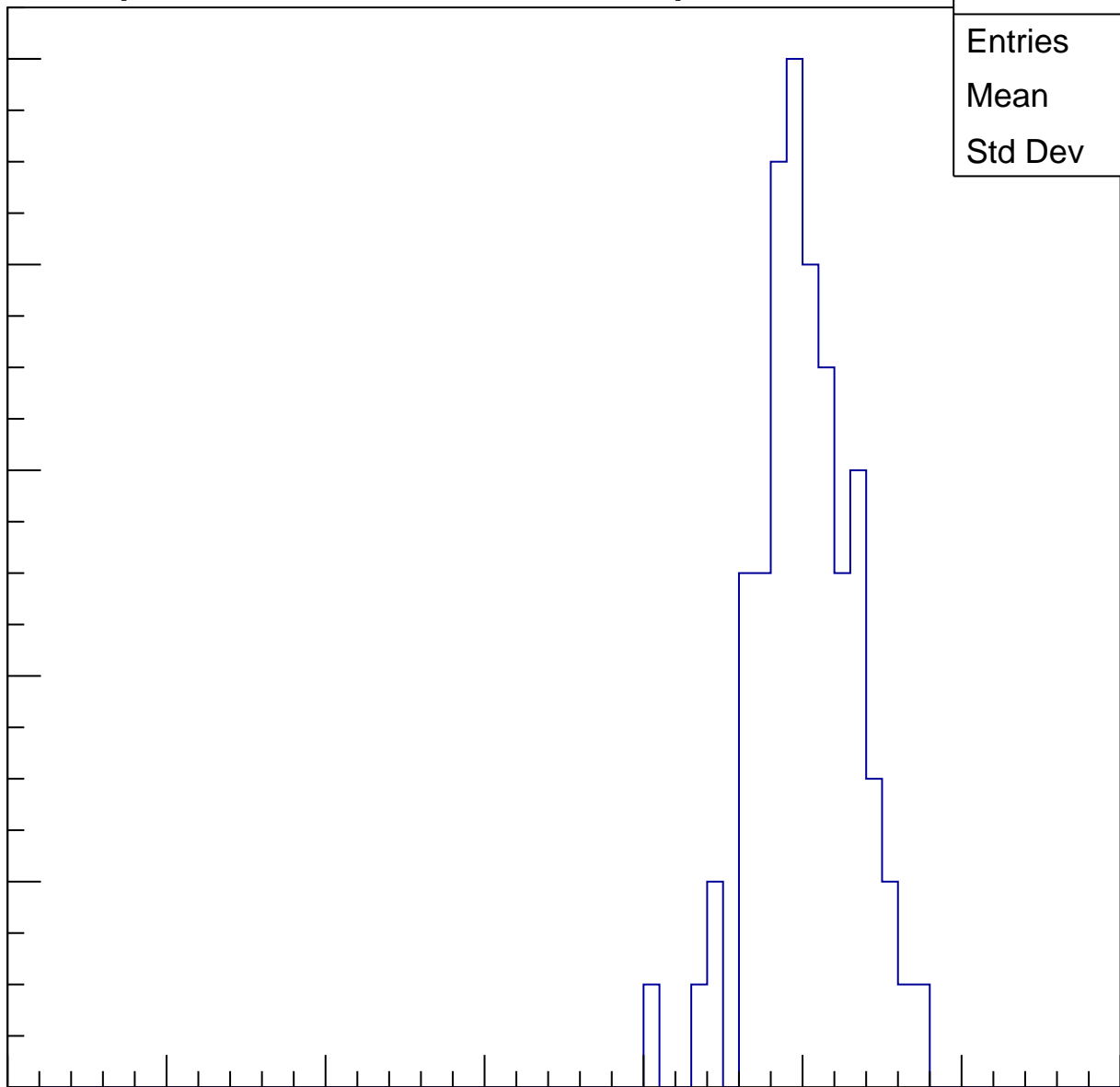
Entries	66
Mean	49.67
Std Dev	3.135

Entry

10  
8  
6  
4  
2  
0

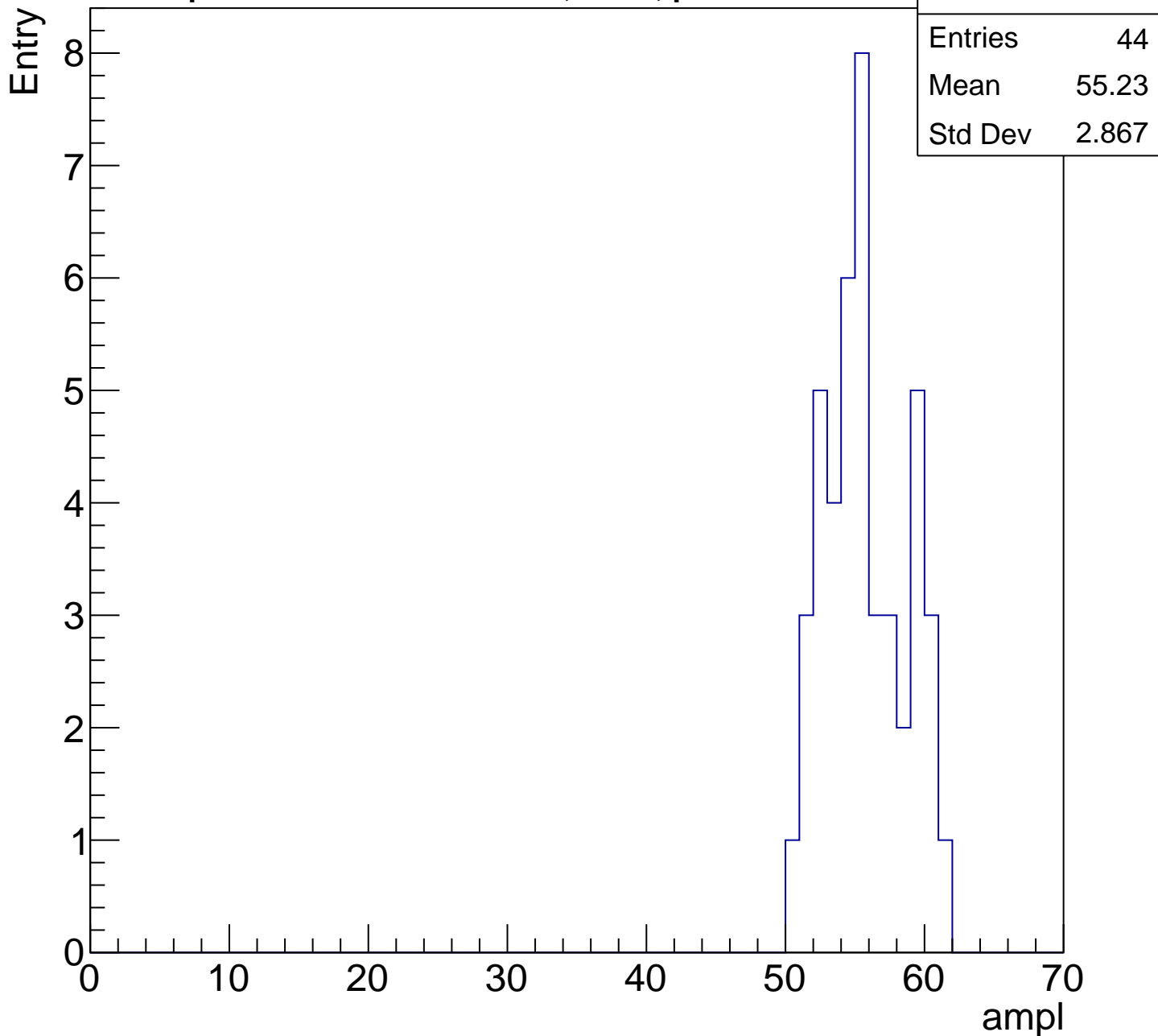
0 10 20 30 40 50 60 70

ampl



# B0L001S, U6-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

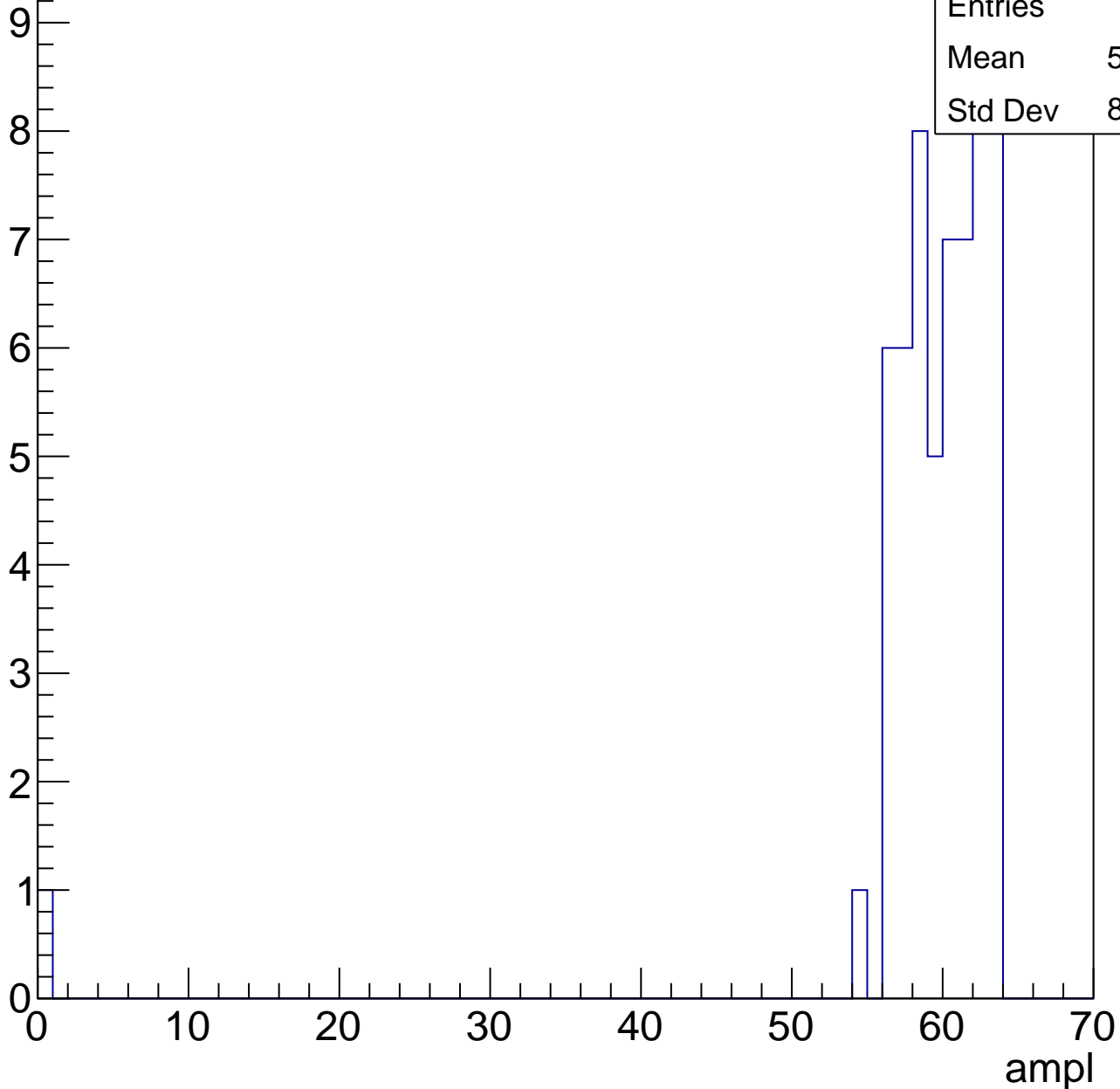


# B0L001S, U6-ch42, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	58.62
Std Dev	8.124



# B0L001S, U6-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

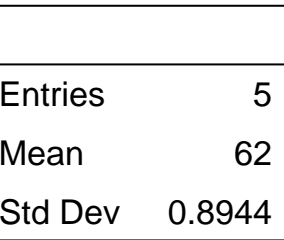
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	62
Std Dev	0.8944

0 10 20 30 40 50 60 70

ampl





# B0L001S, U6-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



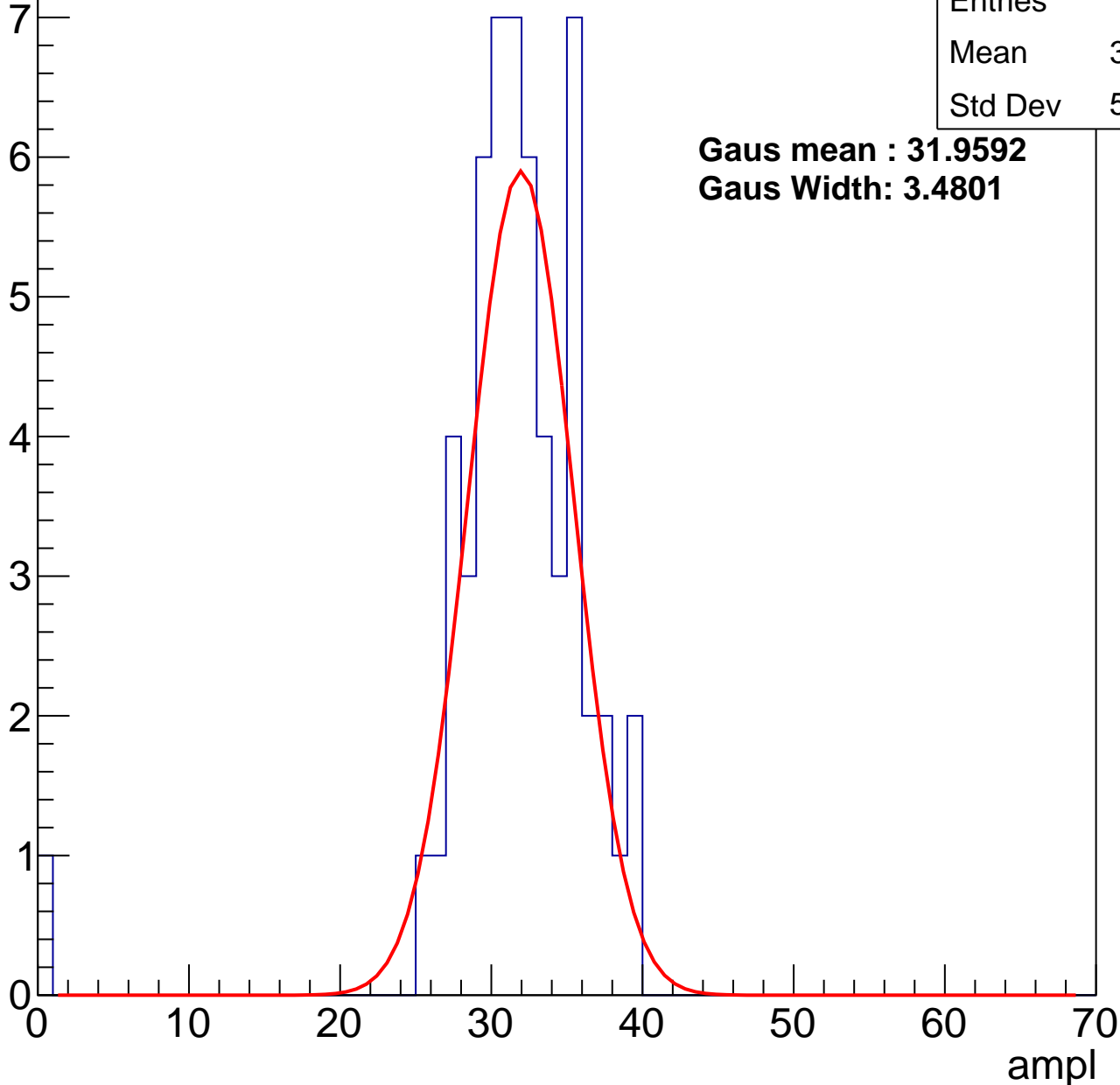
# B0L001S, U6-ch43, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	31.18
Std Dev	5.302

**Gaus mean : 31.9592**  
**Gaus Width: 3.4801**



# B0L001S, U6-ch43, adc1

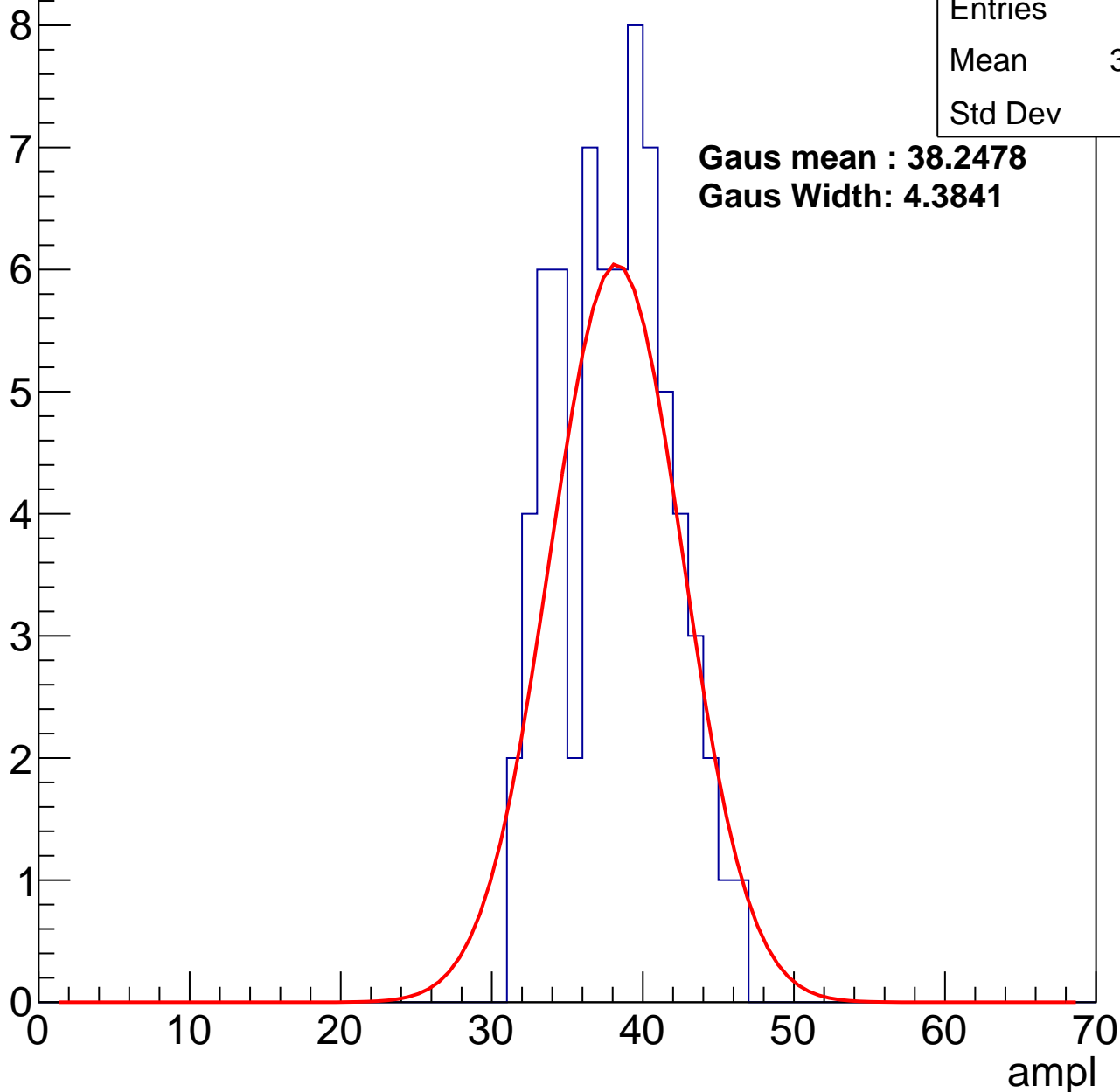
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	37.67
Std Dev	3.66

**Gaus mean : 38.2478**

**Gaus Width: 4.3841**



# B0L001S, U6-ch43, adc2

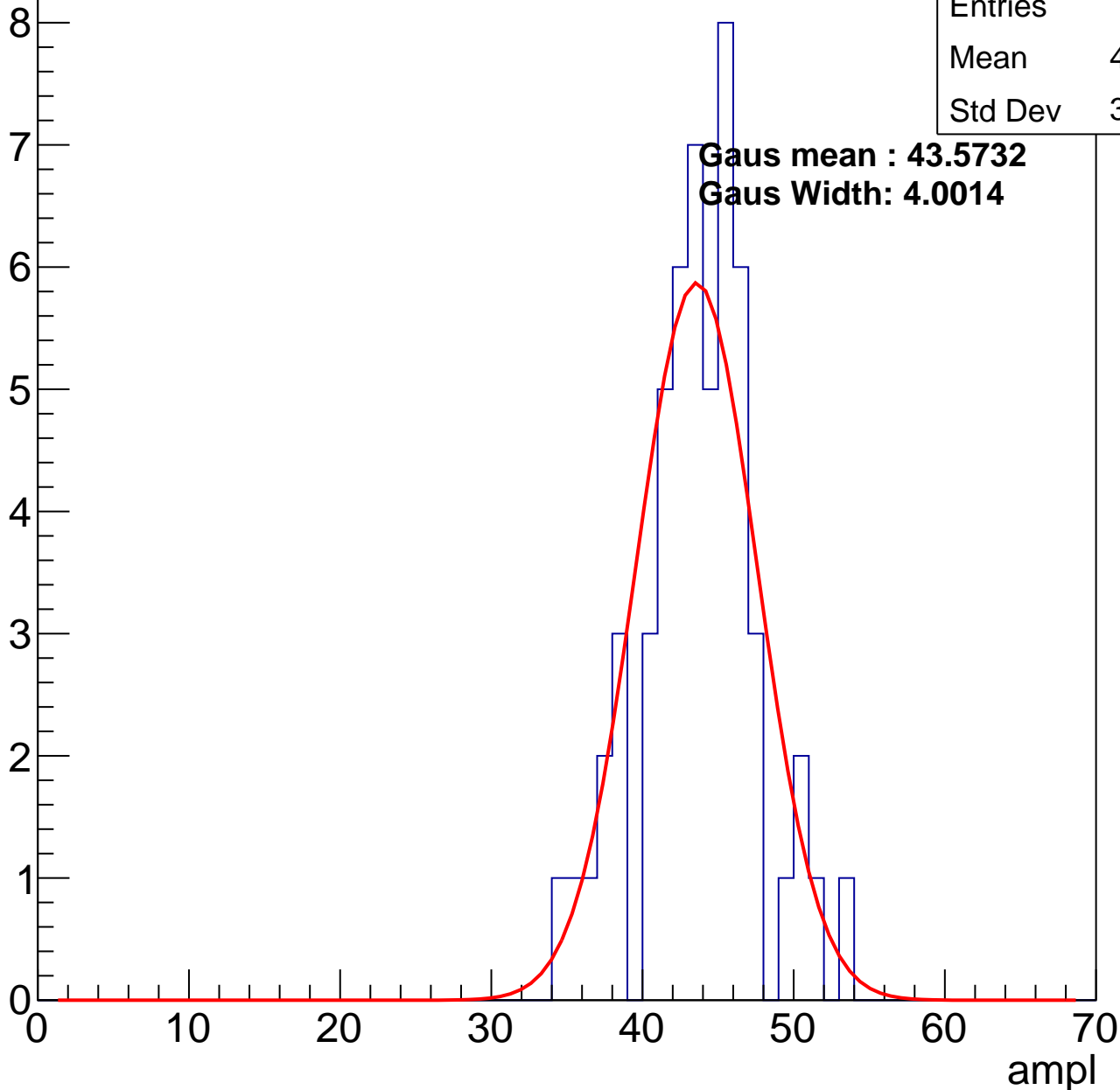
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	43.23
Std Dev	3.845

**Gaus mean : 43.5732**

**Gaus Width: 4.0014**



# B0L001S, U6-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

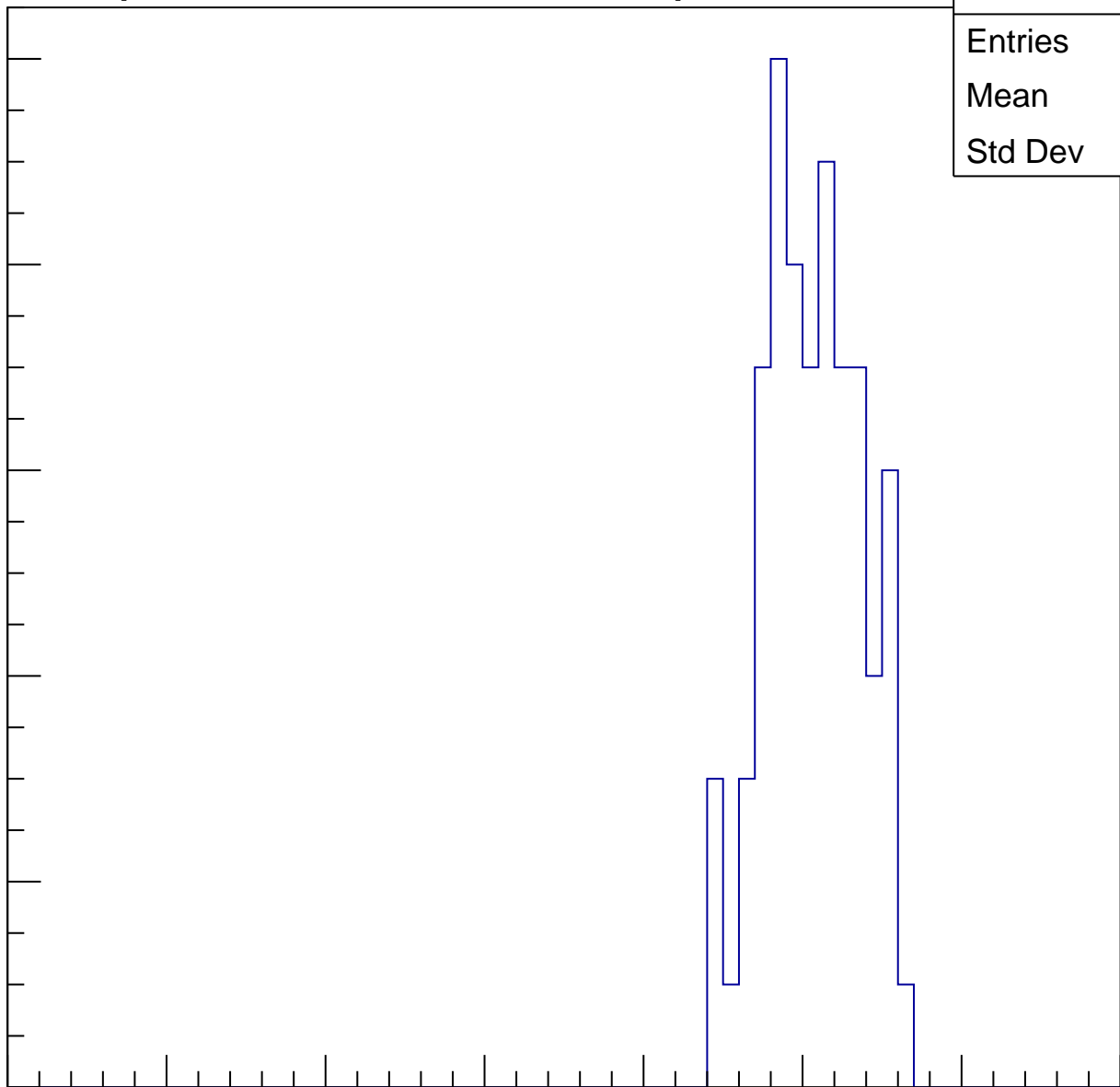
Entries	73
Mean	50.16
Std Dev	2.961

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

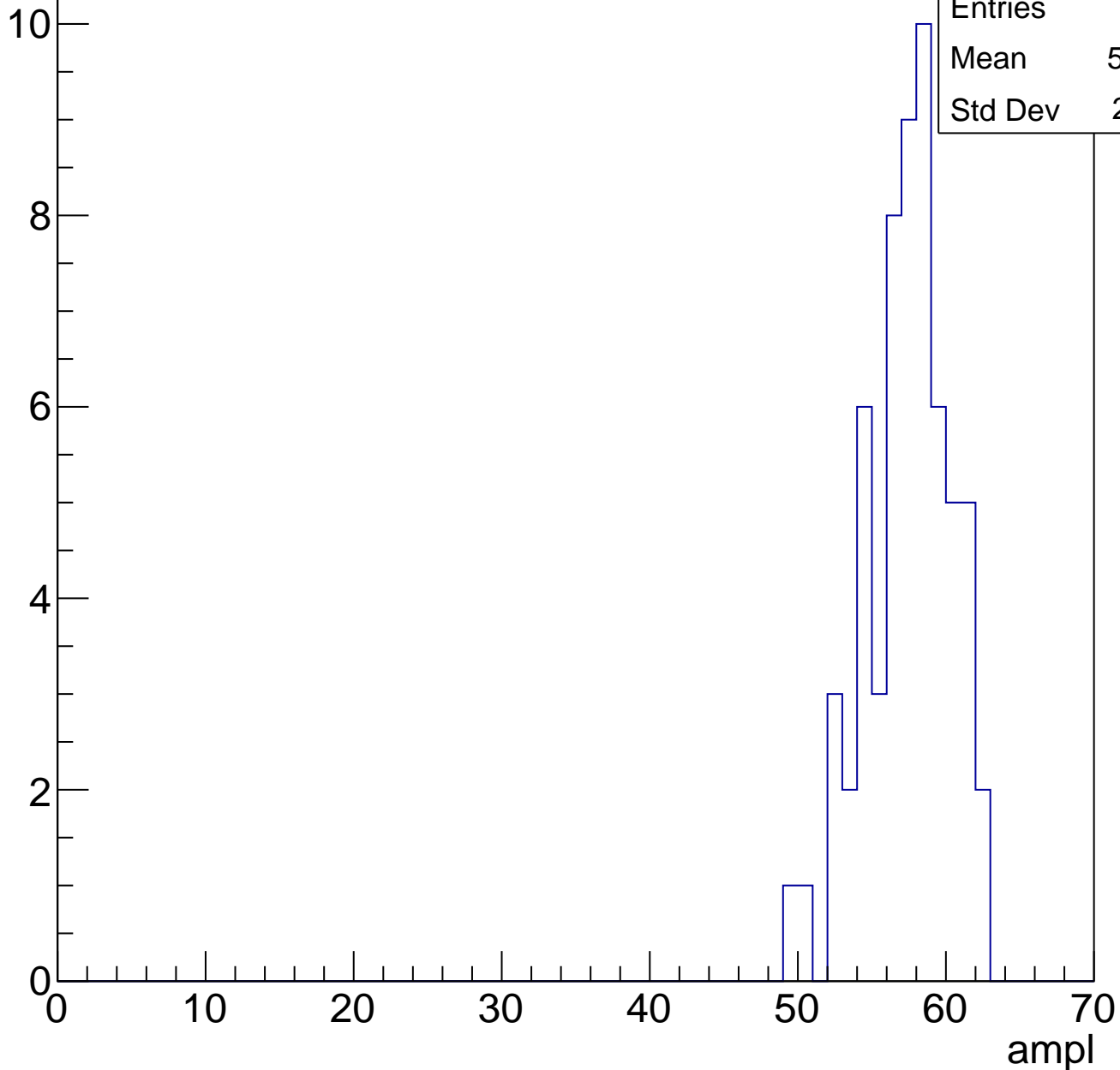


# B0L001S, U6-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	61
Mean	56.95
Std Dev	2.871

Entry

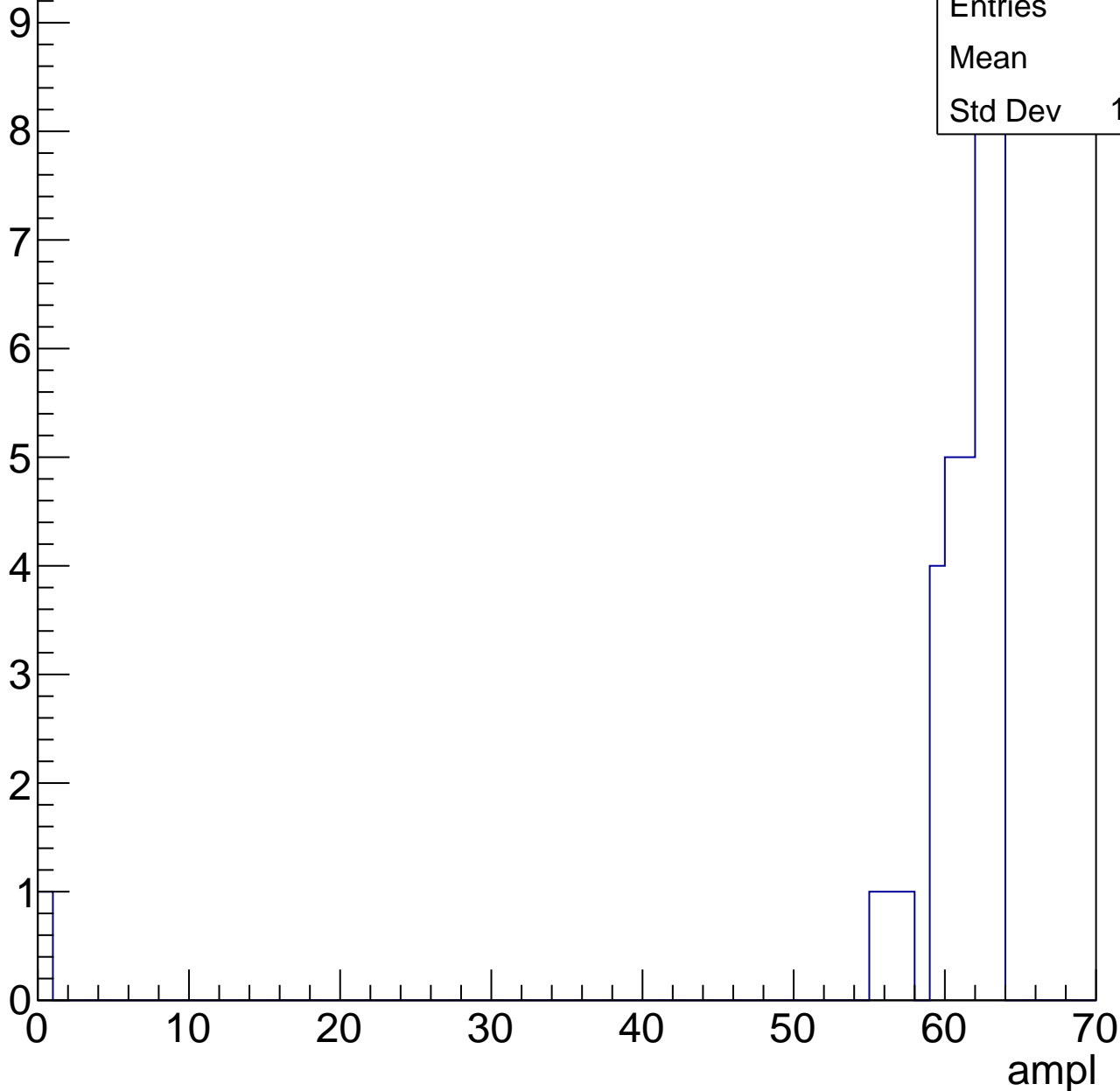


# B0L001S, U6-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	35
Mean	59.2
Std Dev	10.35



# B0L001S, U6-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U6-ch44, adc0

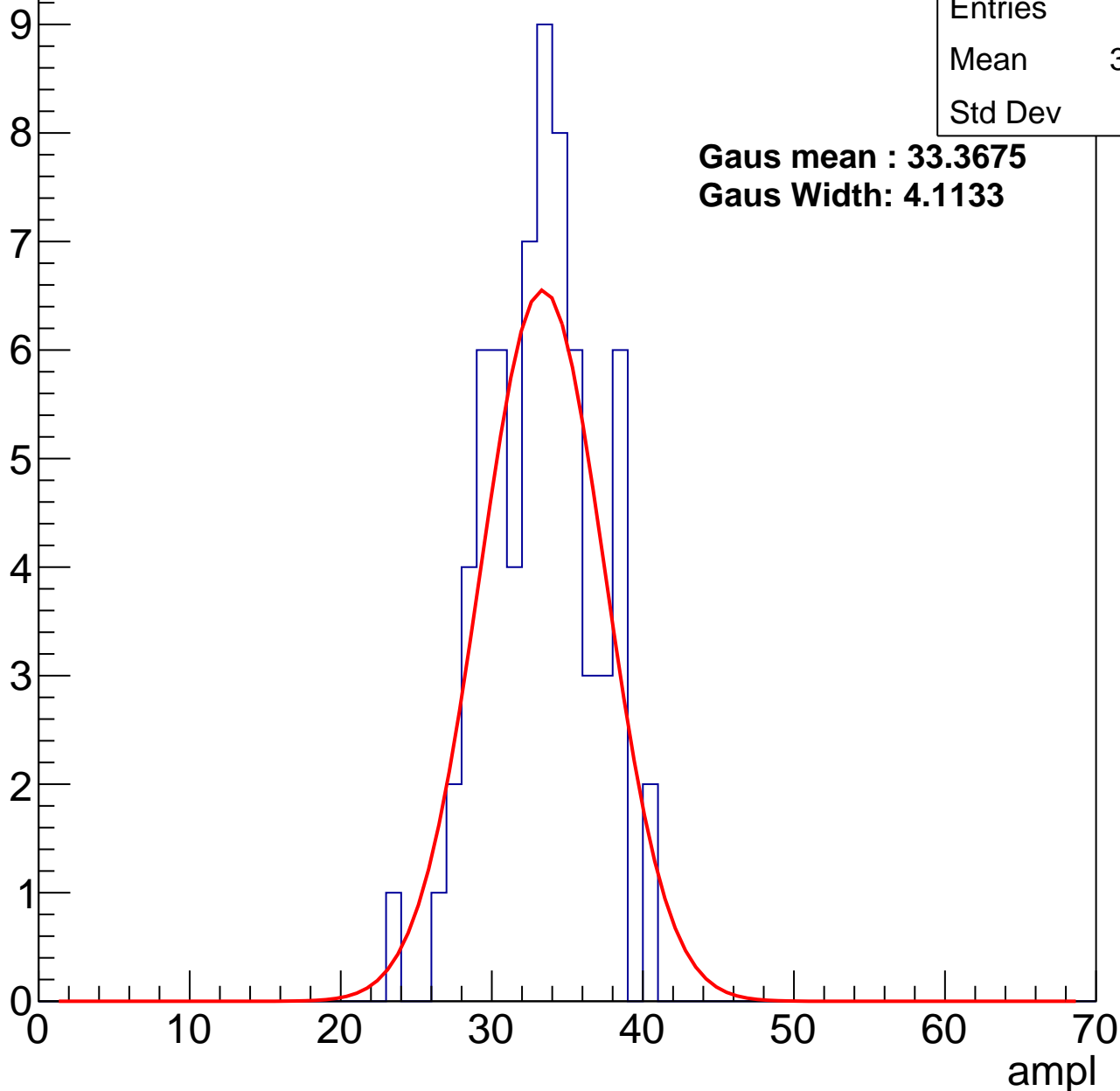
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	32.69
Std Dev	3.52

**Gaus mean : 33.3675**

**Gaus Width: 4.1133**



# B0L001S, U6-ch44, adc1

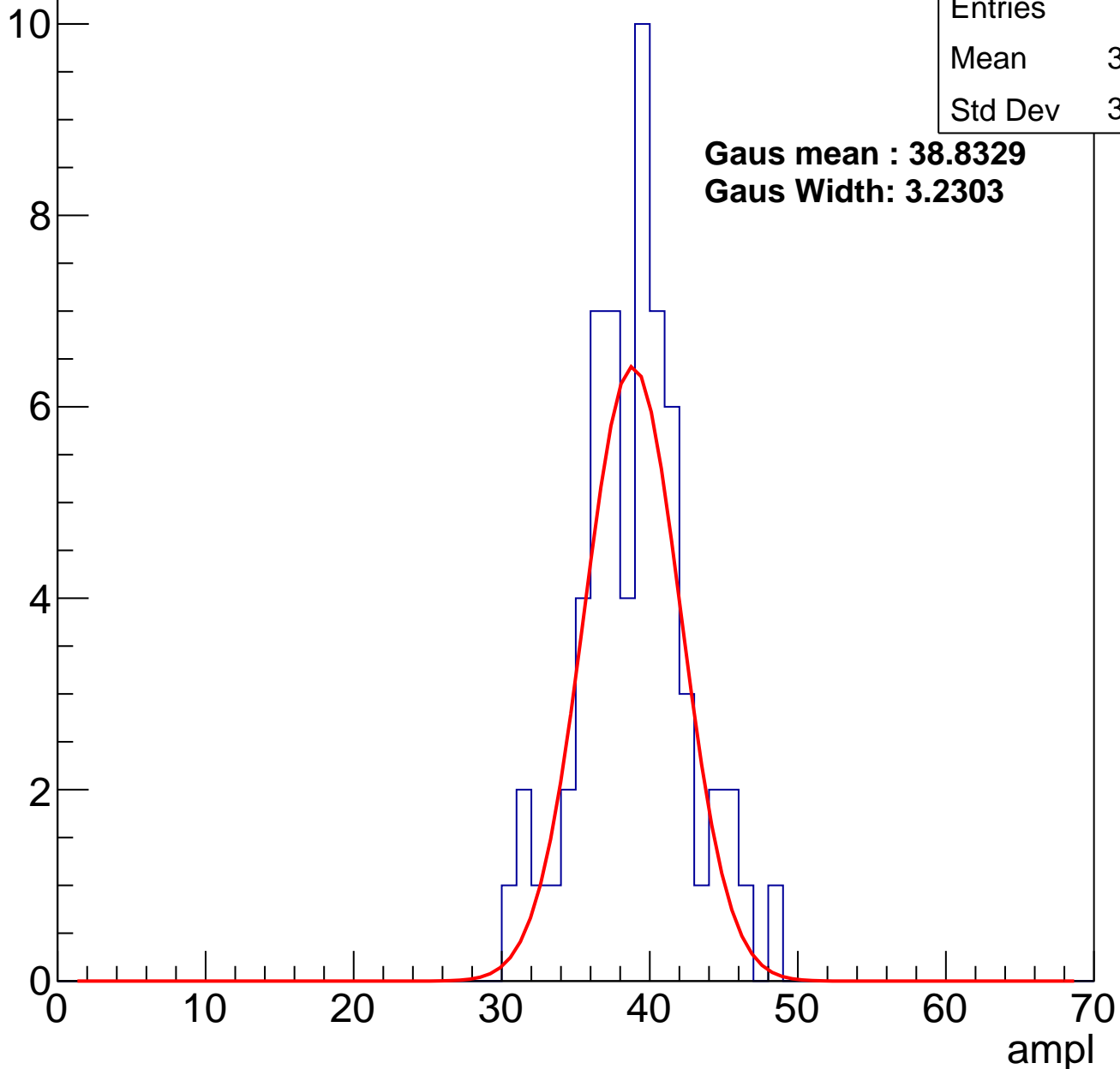
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	62
Mean	38.47
Std Dev	3.618

**Gaus mean : 38.8329**

**Gaus Width: 3.2303**

Entry



# B0L001S, U6-ch44, adc2

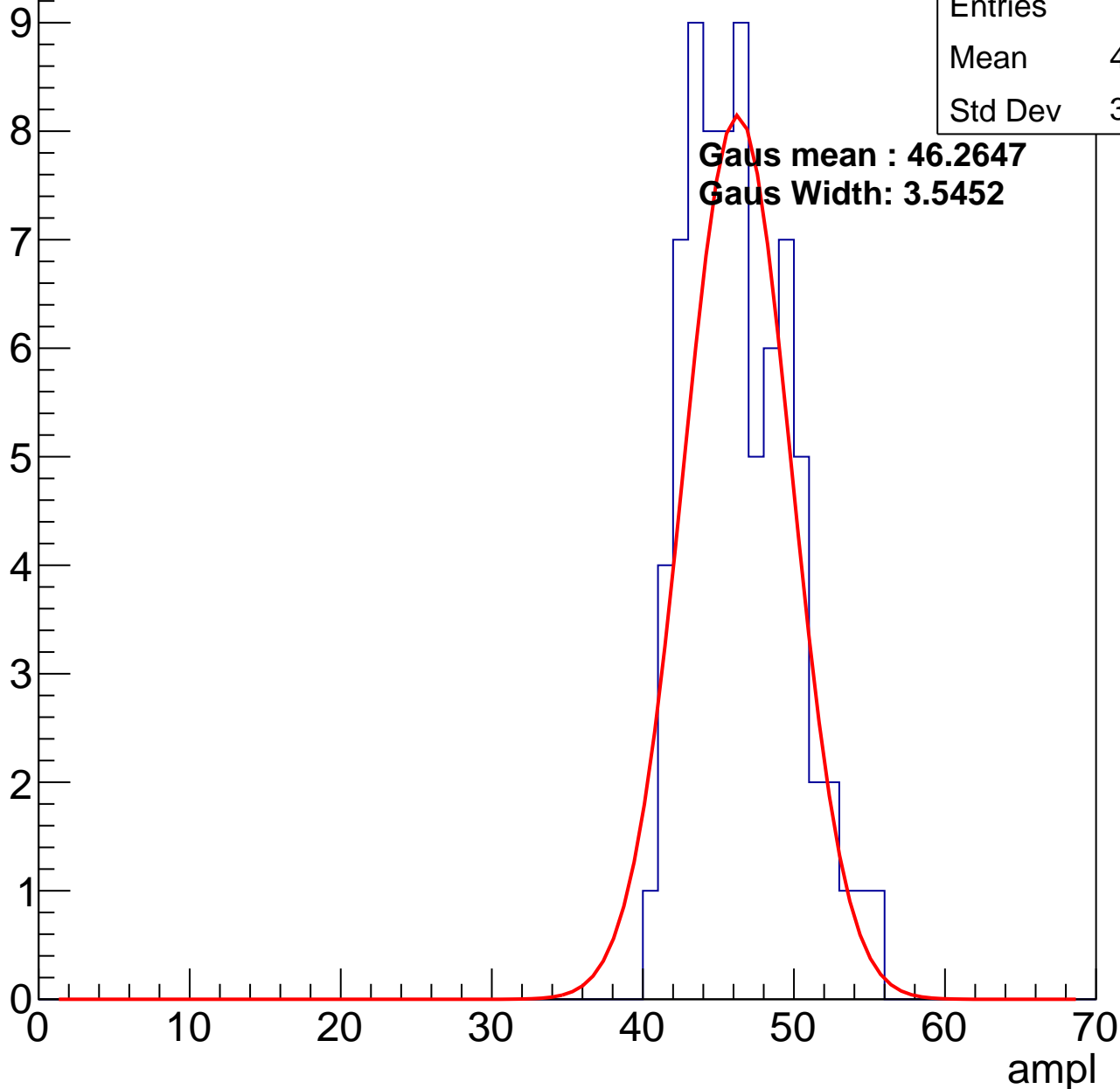
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	45.99
Std Dev	3.358

**Gaus mean : 46.2647**

**Gaus Width: 3.5452**

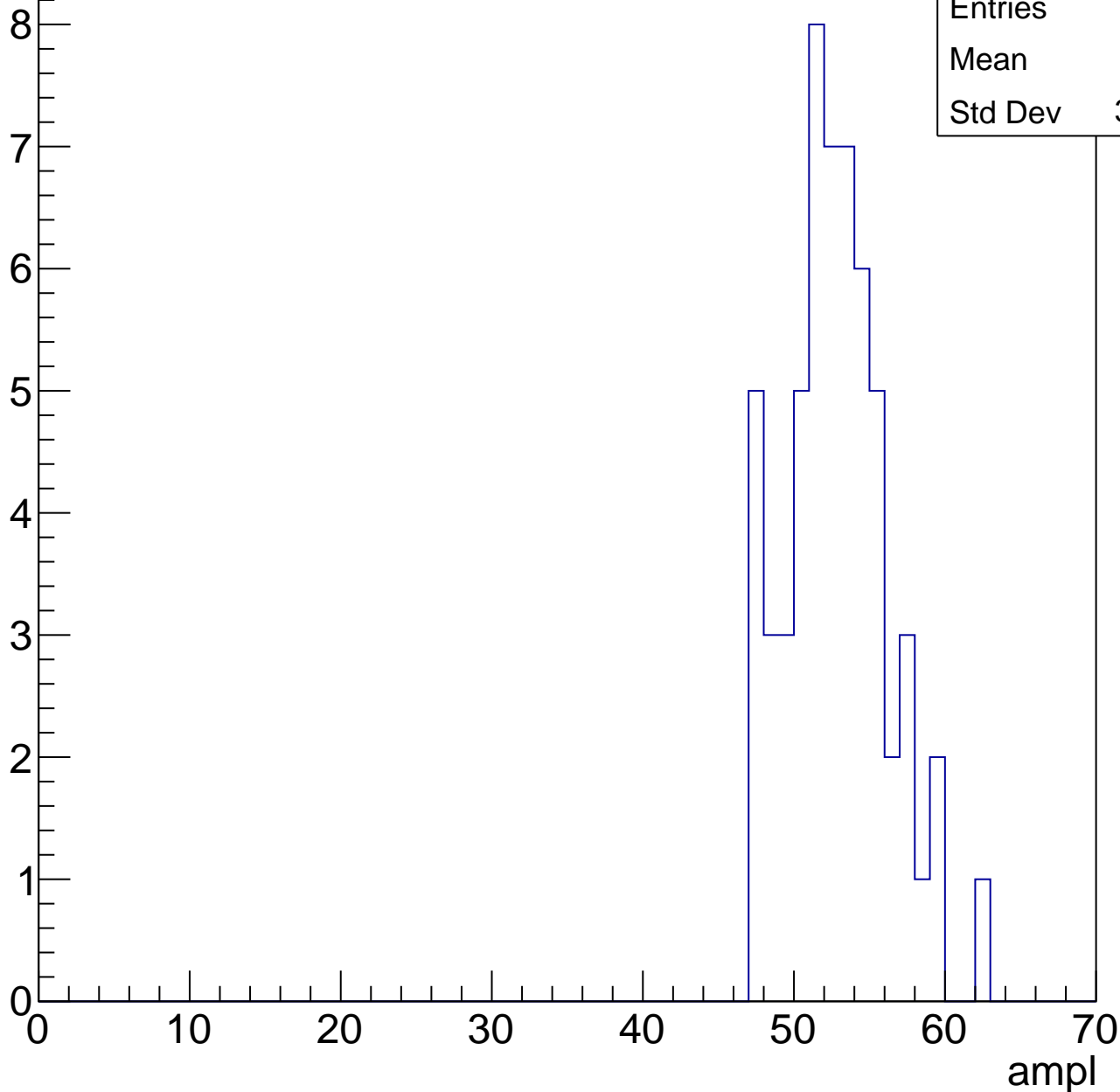


# B0L001S, U6-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	52.4
Std Dev	3.311

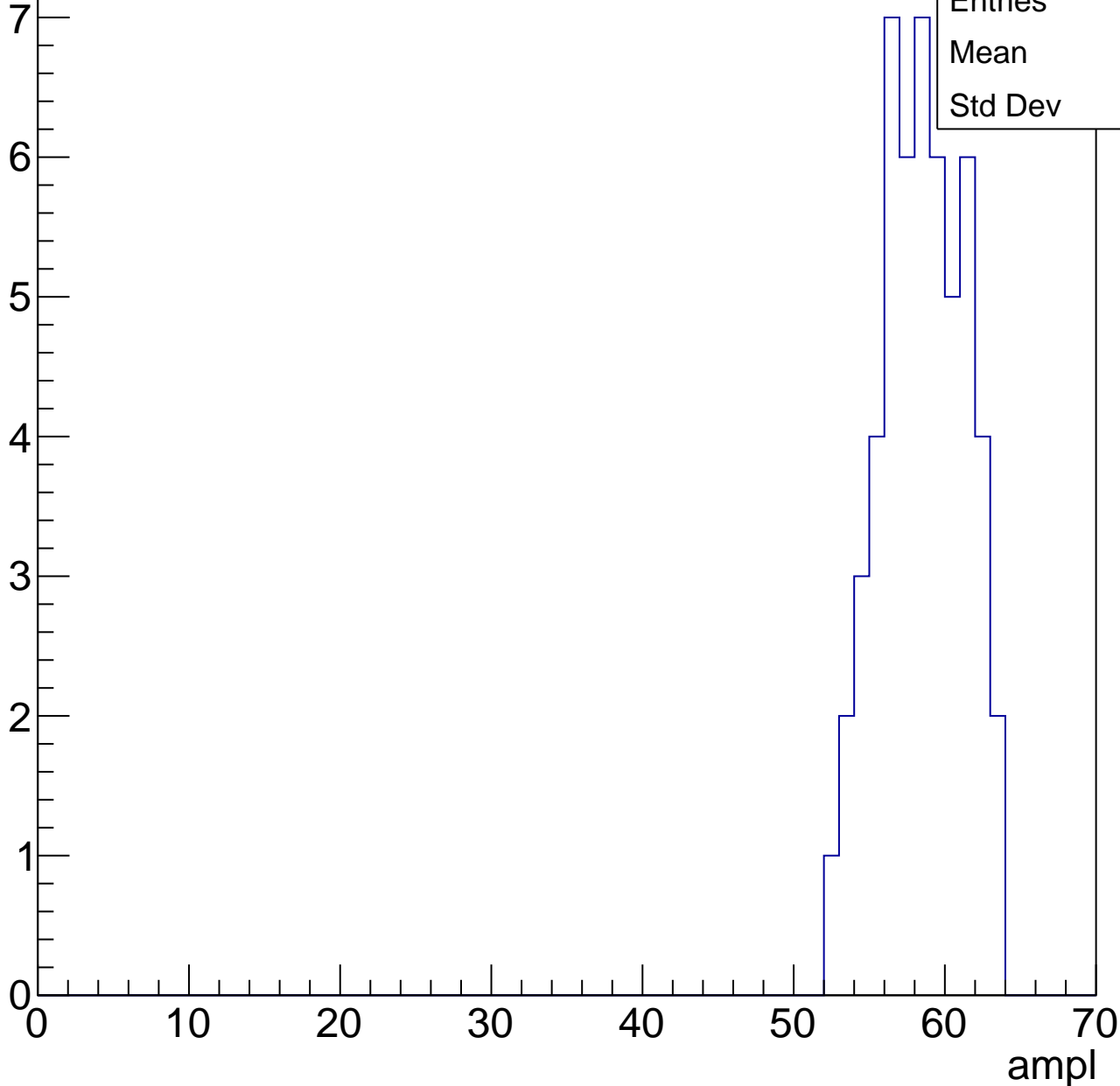


# B0L001S, U6-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	58
Std Dev	2.74

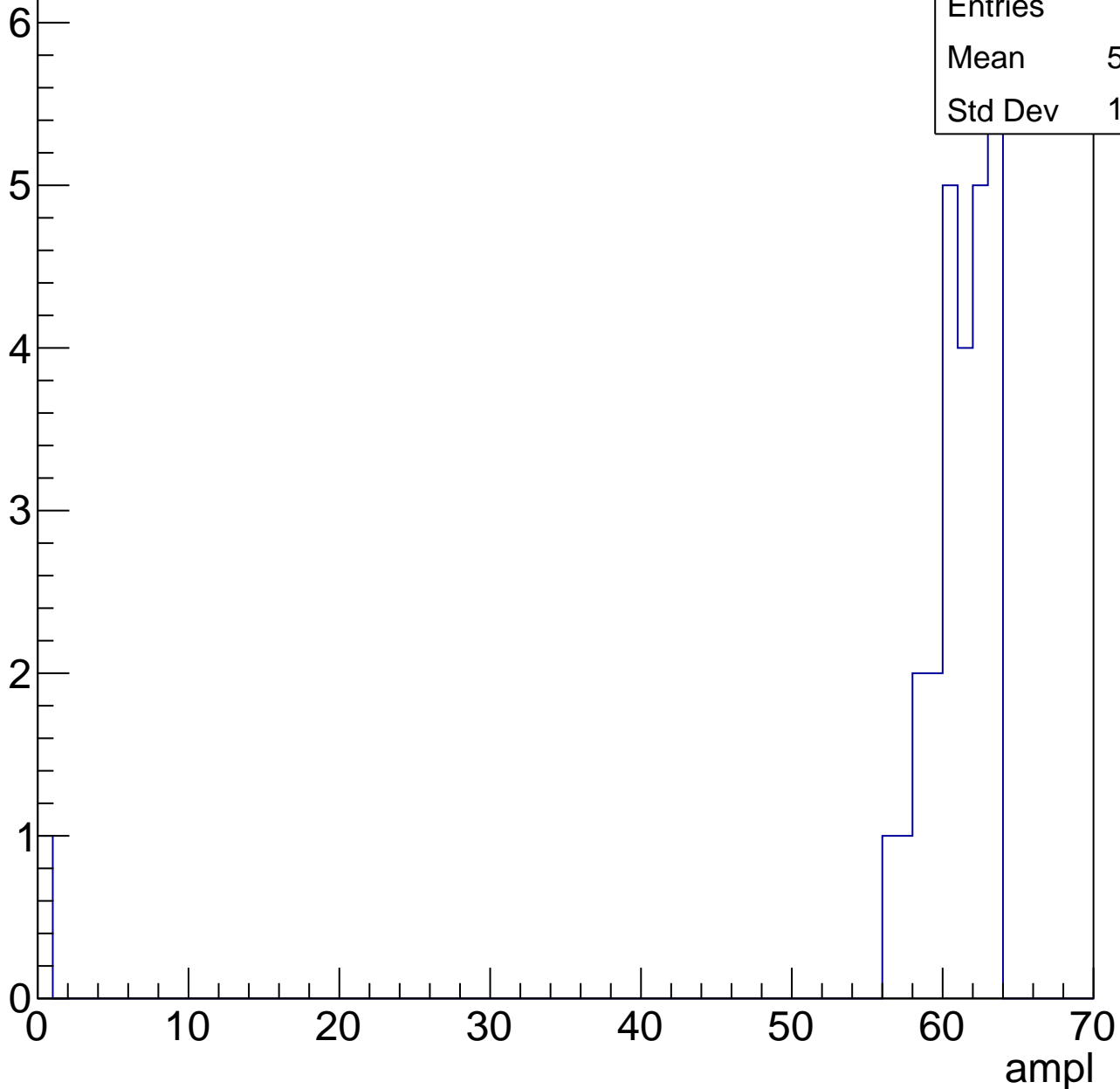


# B0L001S, U6-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	27
Mean	58.48
Std Dev	11.63



# B0L001S, U6-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

ampl



# B0L001S, U6-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch45, adc0

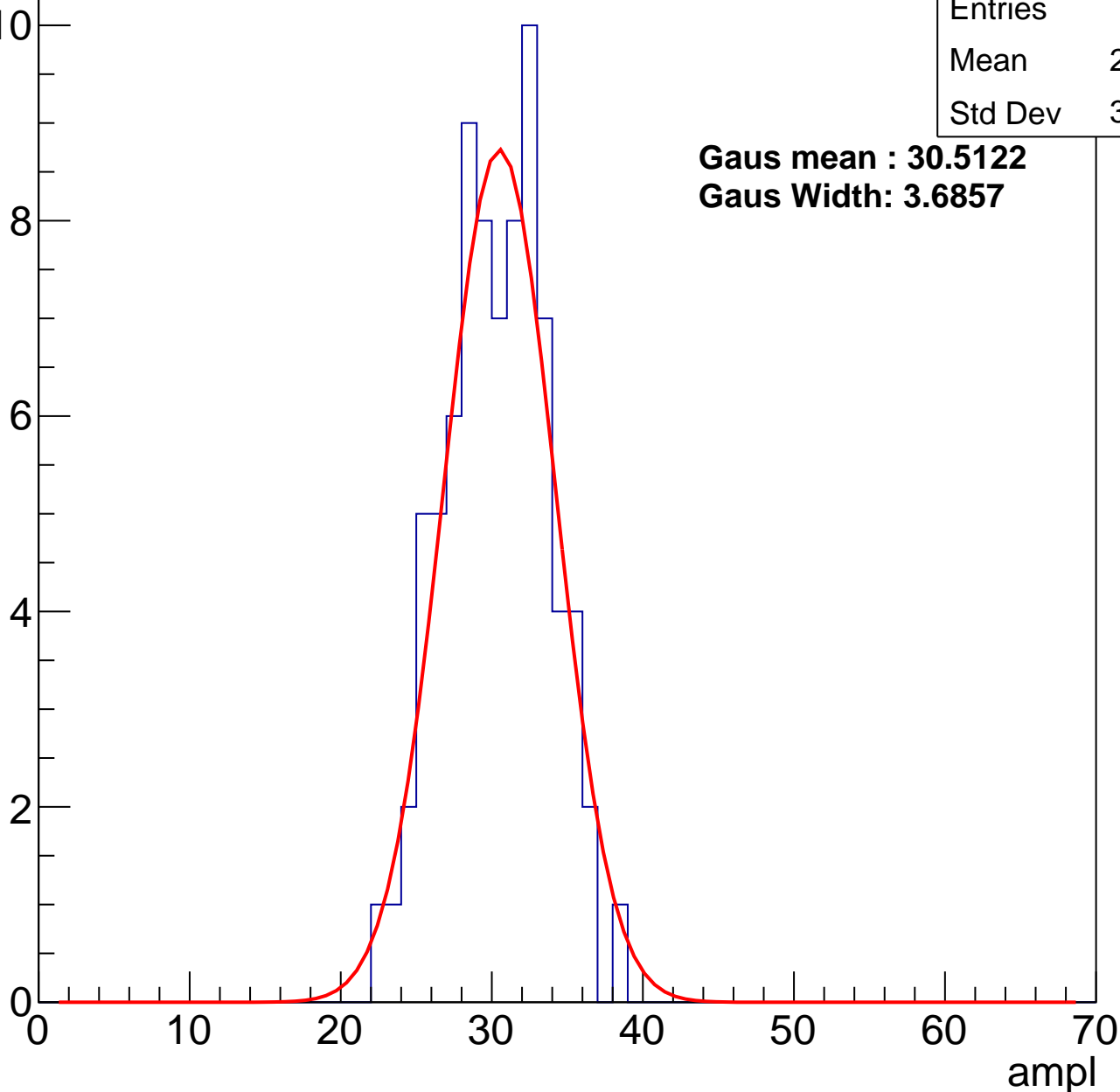
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	80
Mean	29.86
Std Dev	3.349

**Gaus mean : 30.5122**

**Gaus Width: 3.6857**



# B0L001S, U6-ch45, adc1

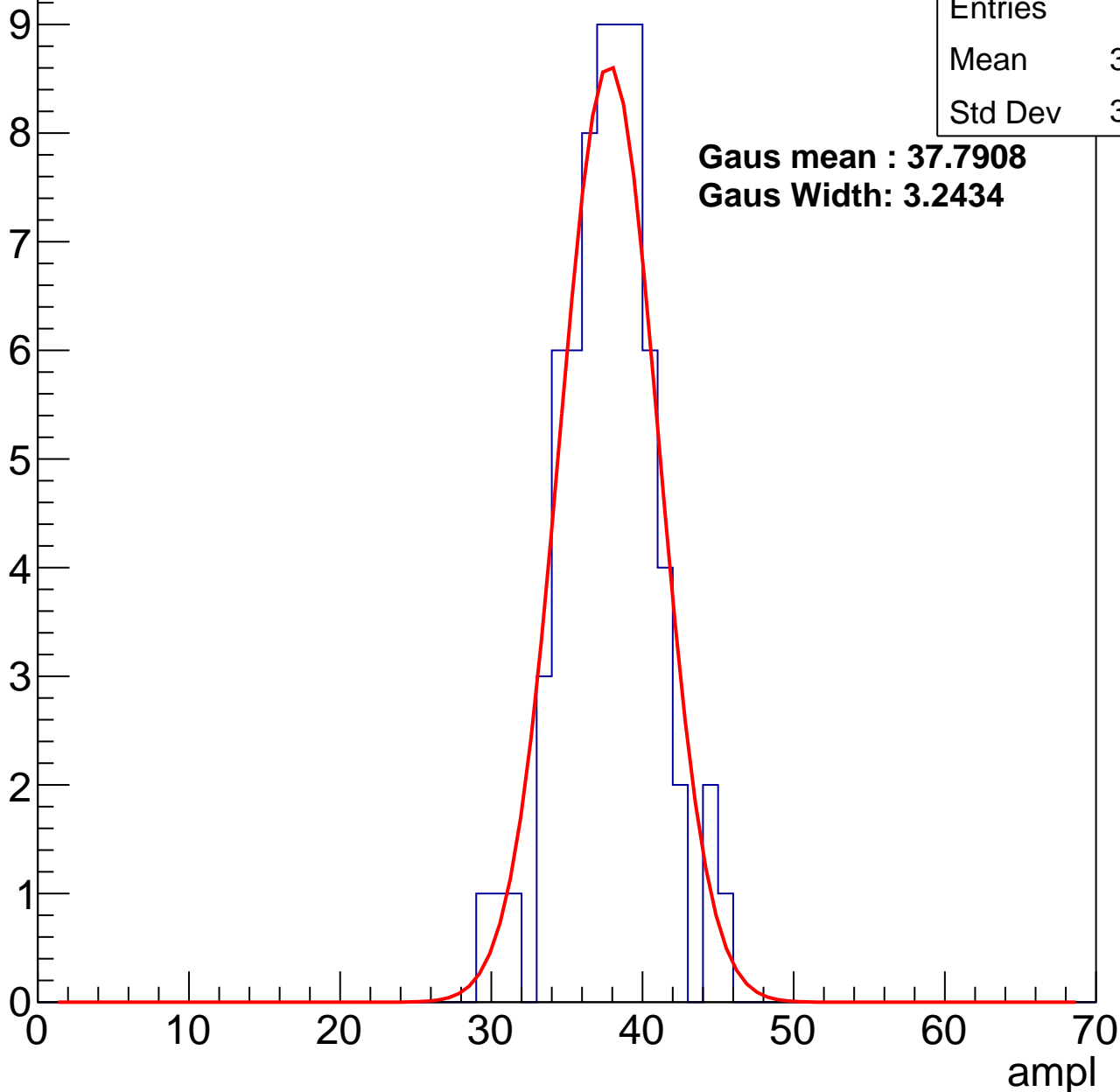
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	37.32
Std Dev	3.094

**Gaus mean : 37.7908**

**Gaus Width: 3.2434**



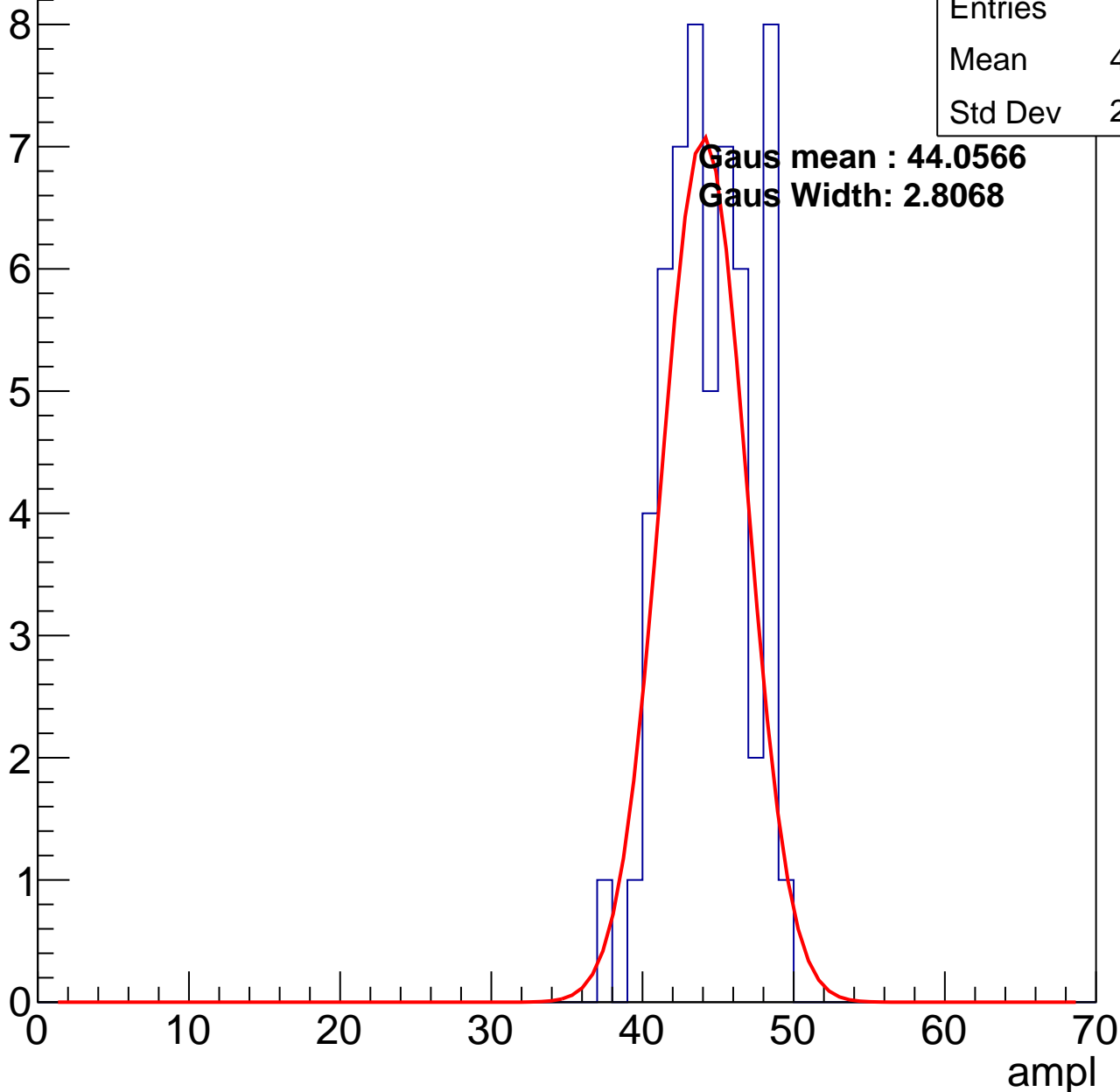
# B0L001S, U6-ch45, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	43.89
Std Dev	2.769

**Gaus mean : 44.0566**  
**Gaus Width: 2.8068**

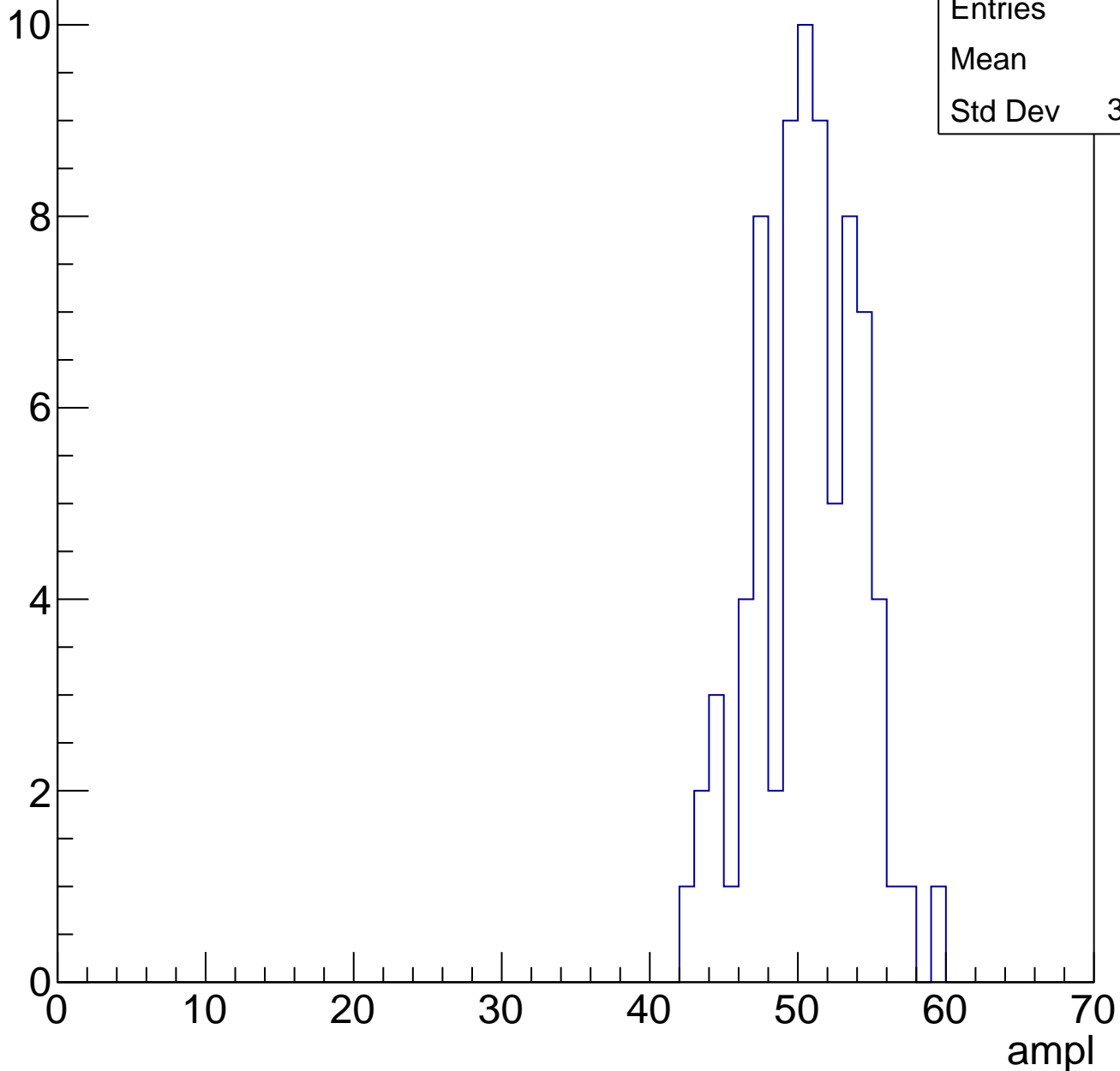


# B0L001S, U6-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

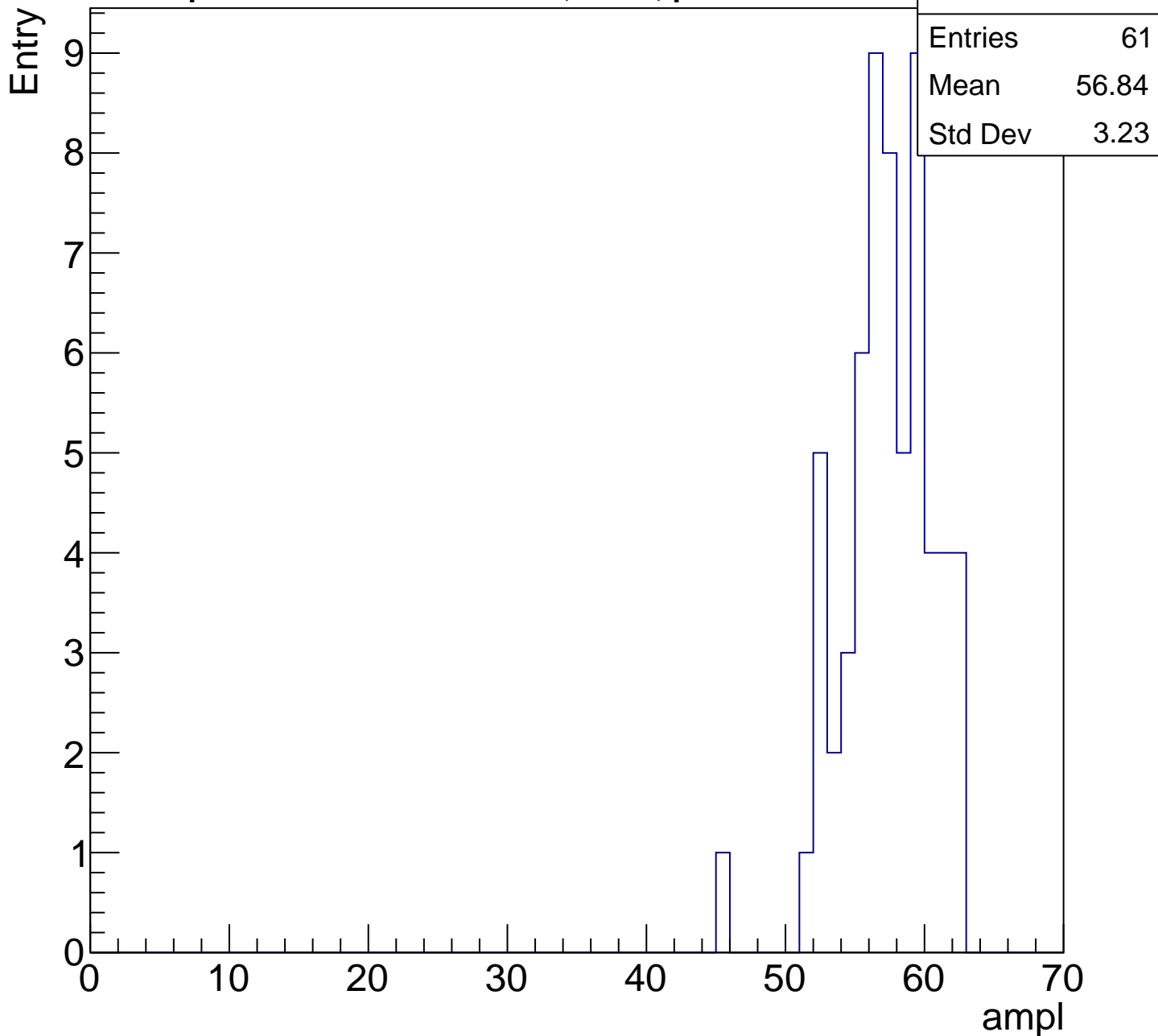
Entries	76
Mean	50.2
Std Dev	3.487

Entry



# B0L001S, U6-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

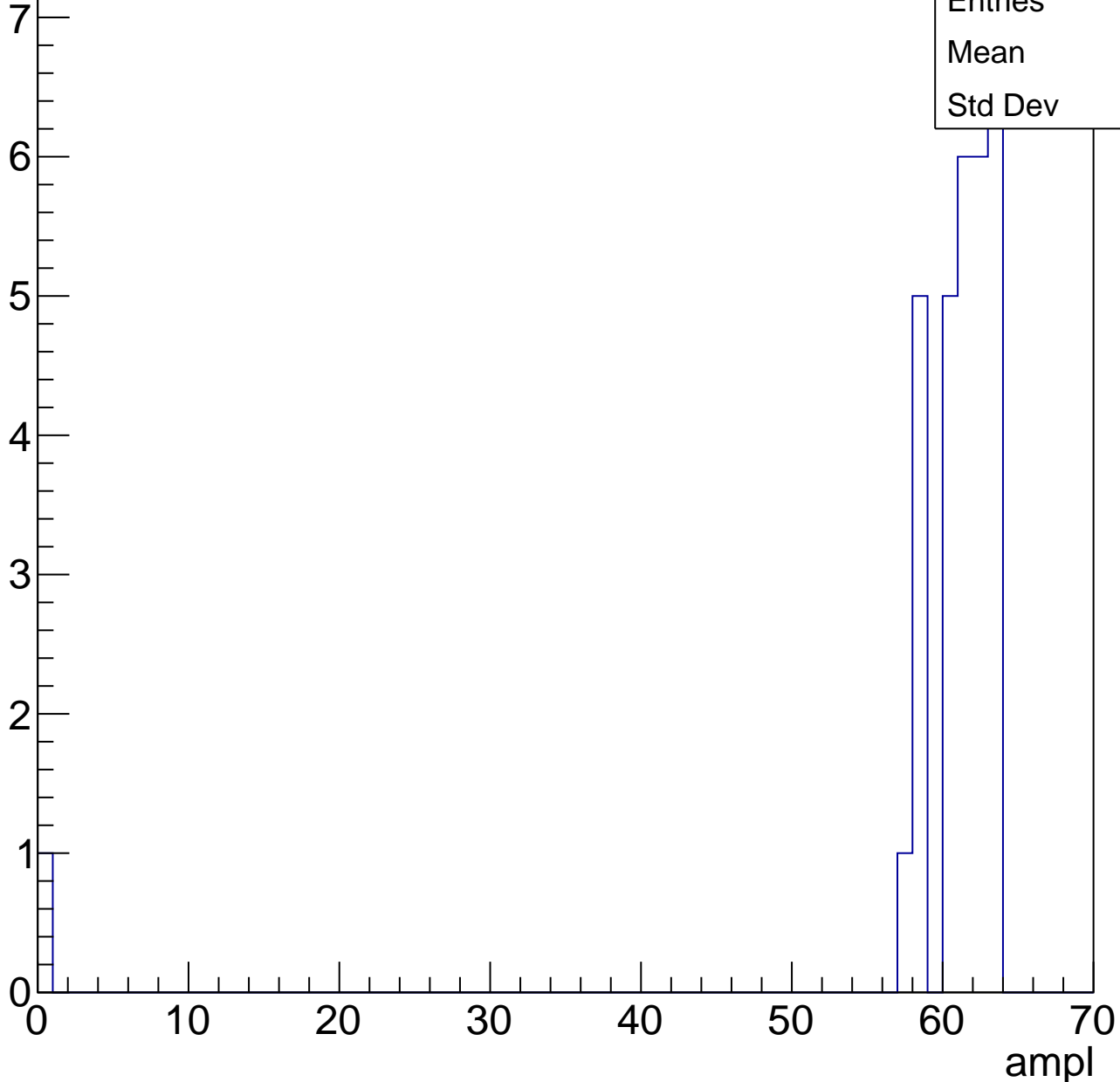


# B0L001S, U6-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

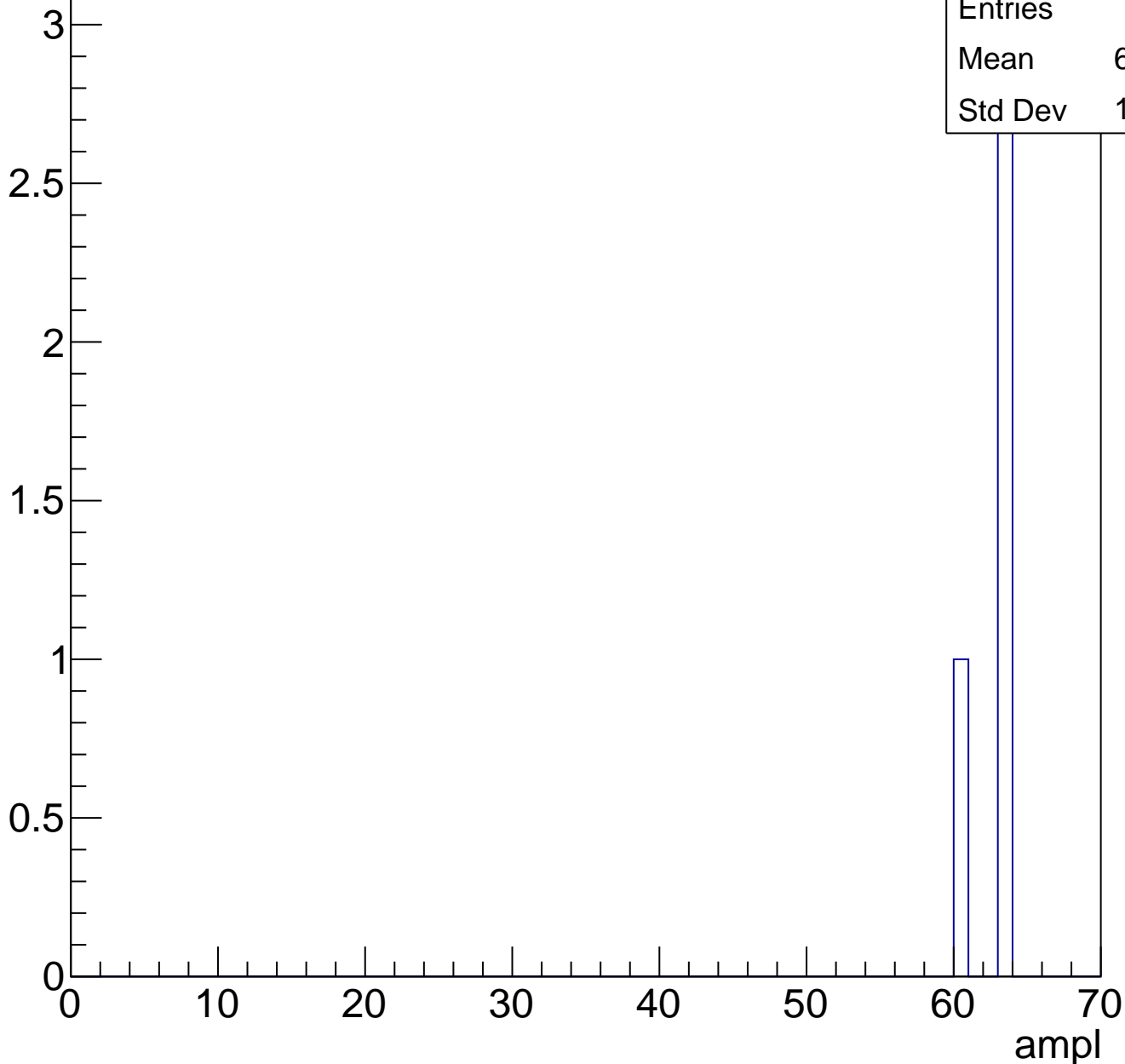
Entries	31
Mean	58.9
Std Dev	10.9



# B0L001S, U6-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch46, adc0

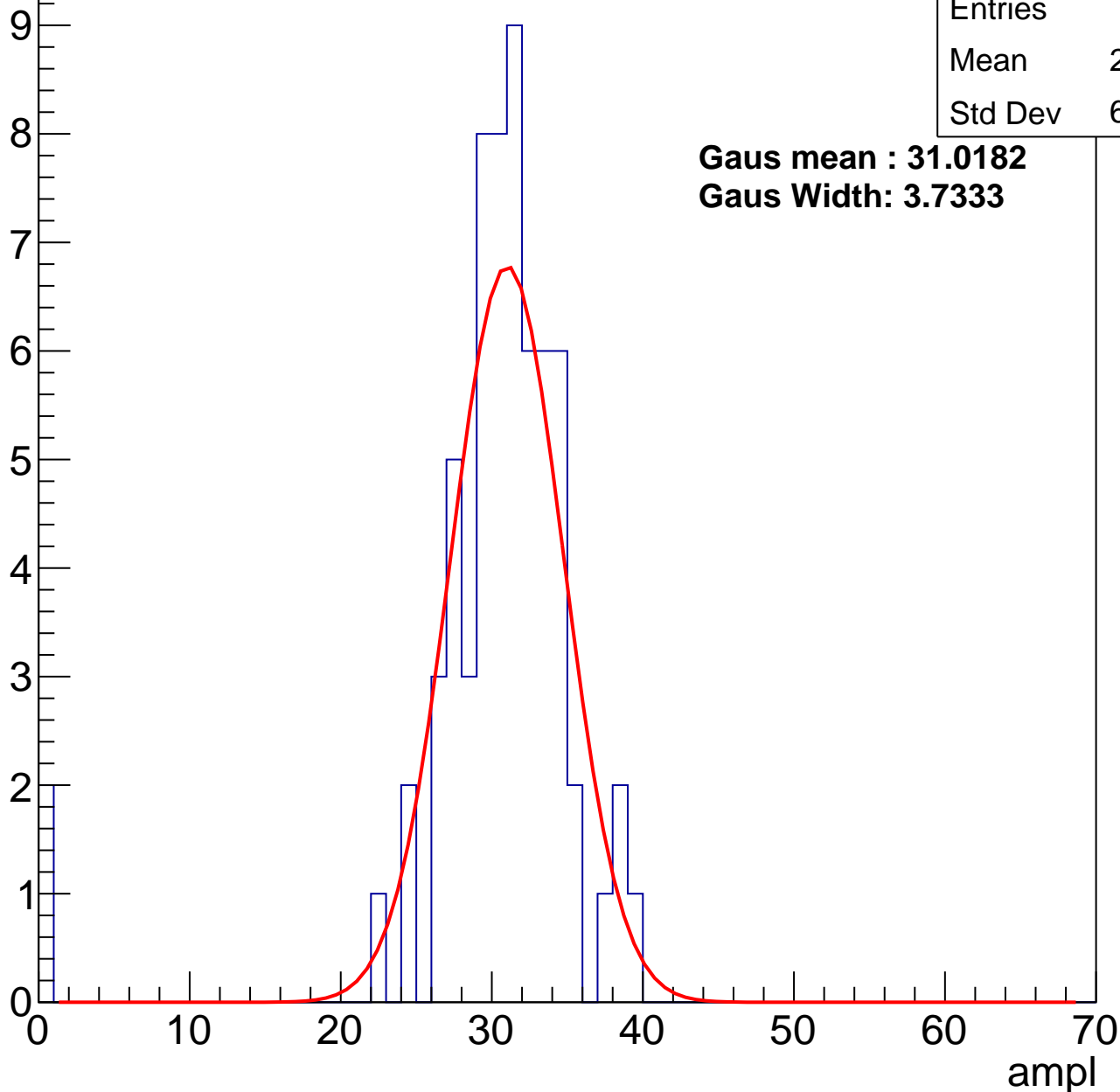
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	29.75
Std Dev	6.246

**Gaus mean : 31.0182**

**Gaus Width: 3.7333**



# B0L001S, U6-ch46, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	37.71
Std Dev	3.348

**Gaus mean : 38.3702**

**Gaus Width: 3.8174**

10

8

6

4

2

0

0

10

20

30

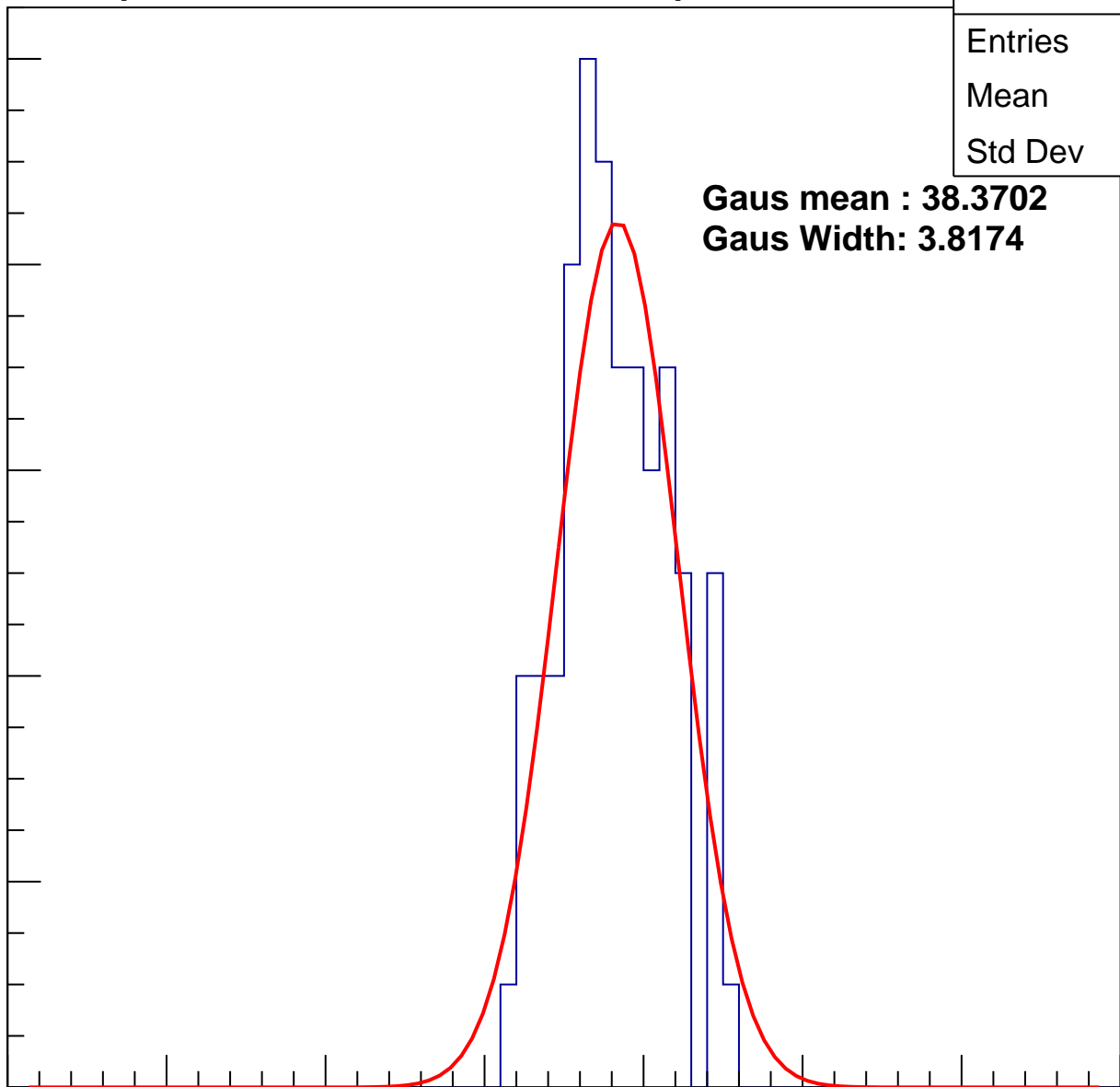
40

50

60

70

ampl



# B0L001S, U6-ch46, adc2

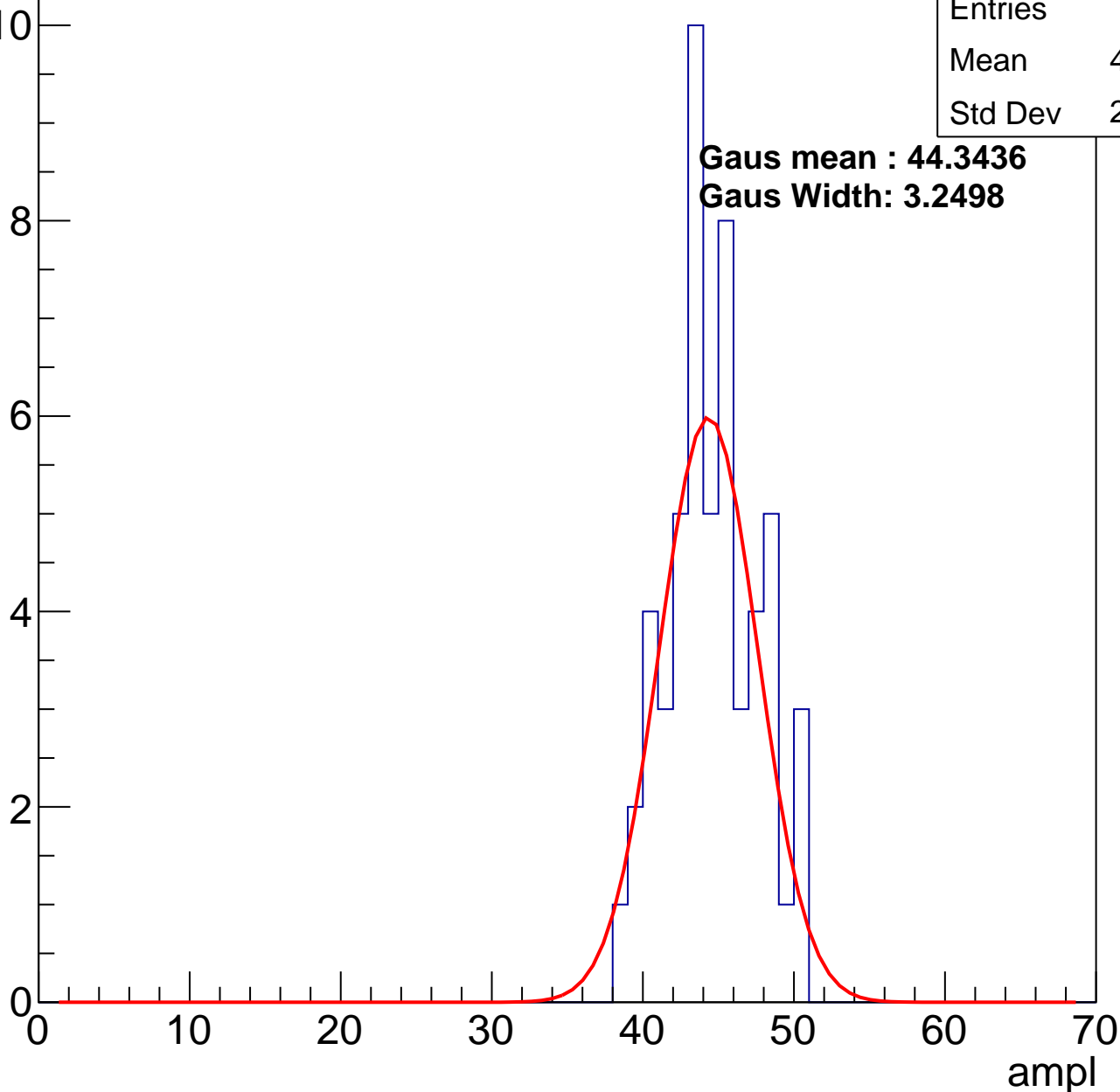
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	44.15
Std Dev	2.965

**Gaus mean : 44.3436**

**Gaus Width: 3.2498**

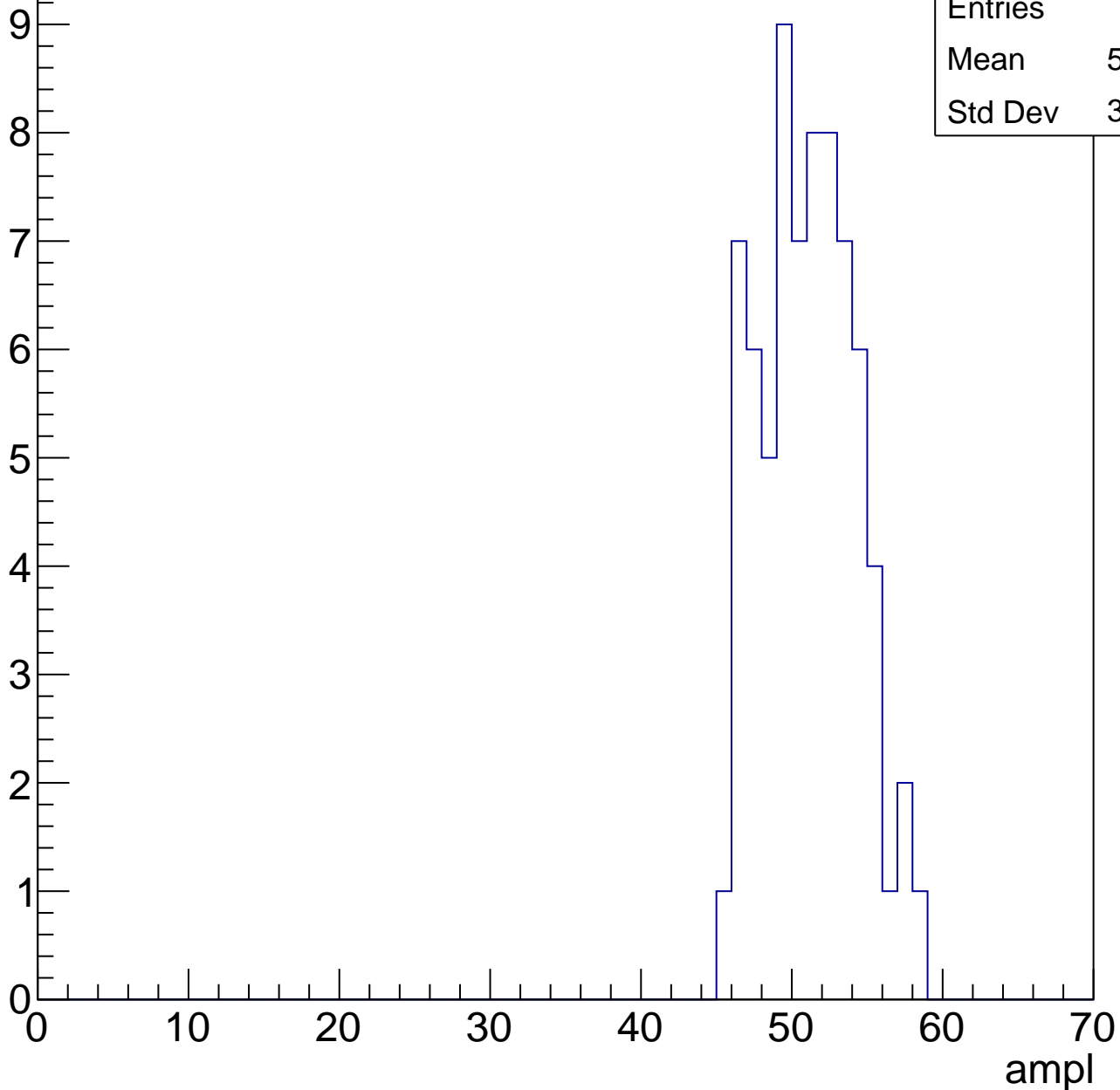


# B0L001S, U6-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	50.65
Std Dev	3.087

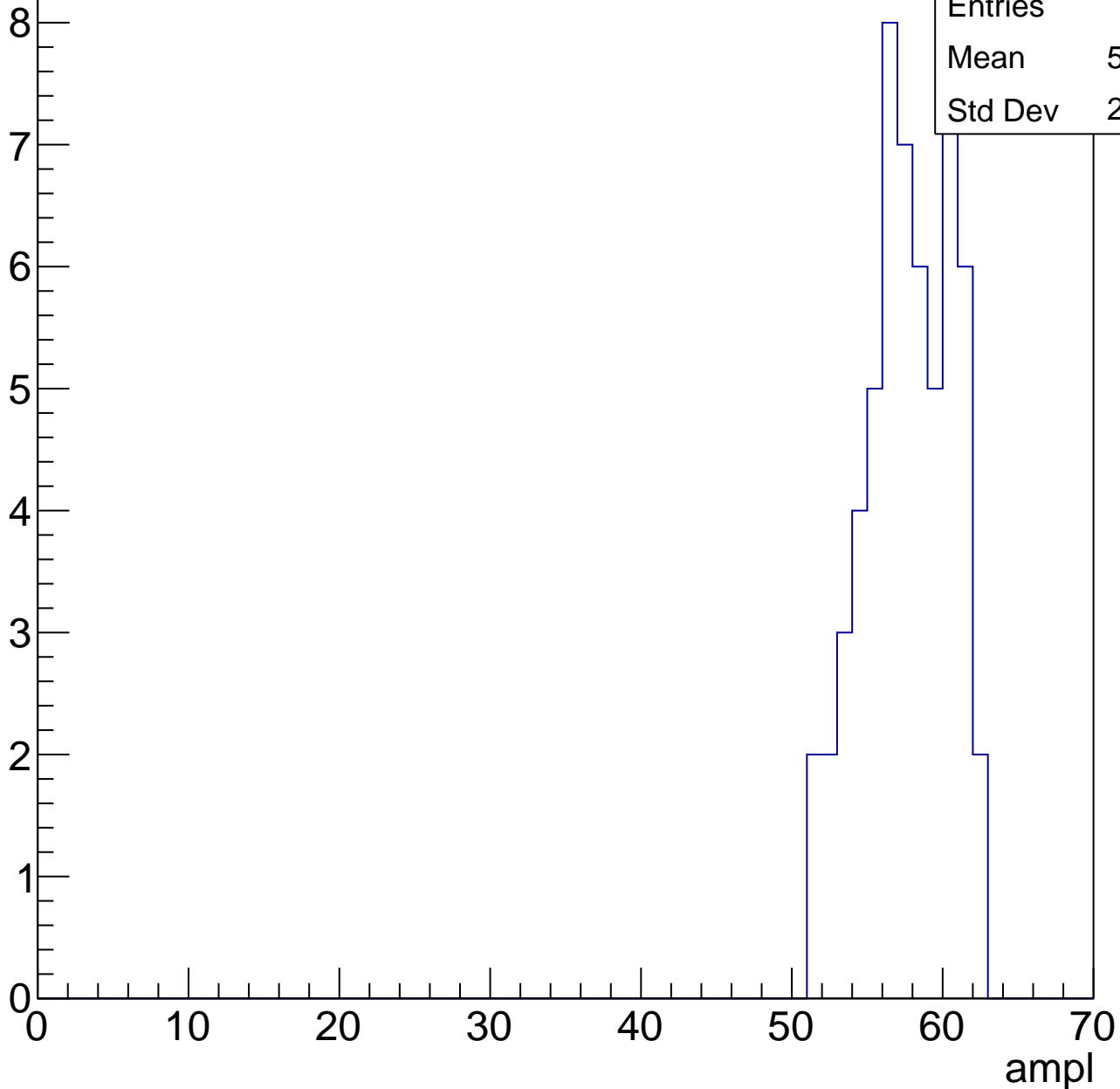


# B0L001S, U6-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

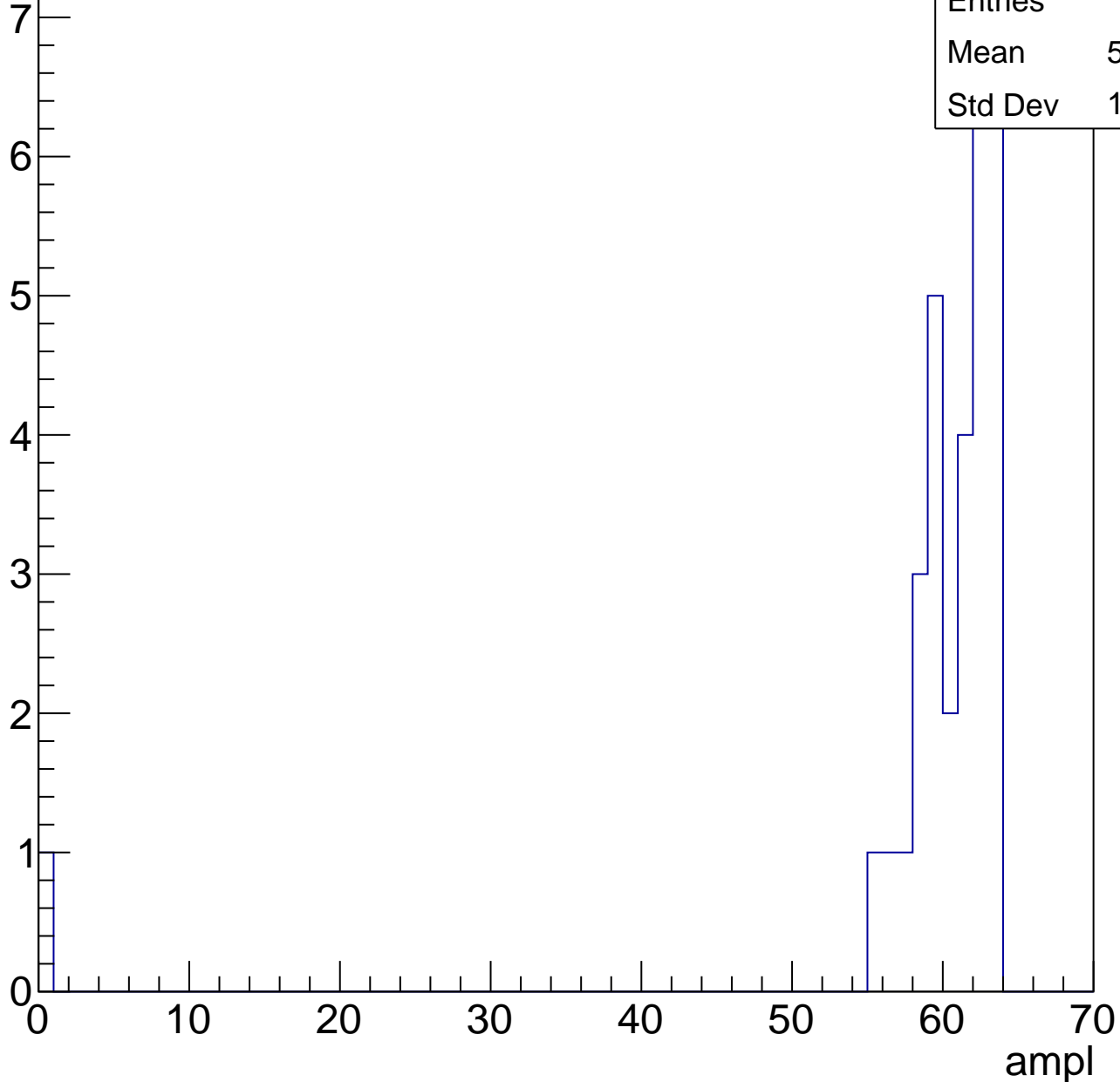
Entries	58
Mean	57.17
Std Dev	2.866



# B0L001S, U6-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

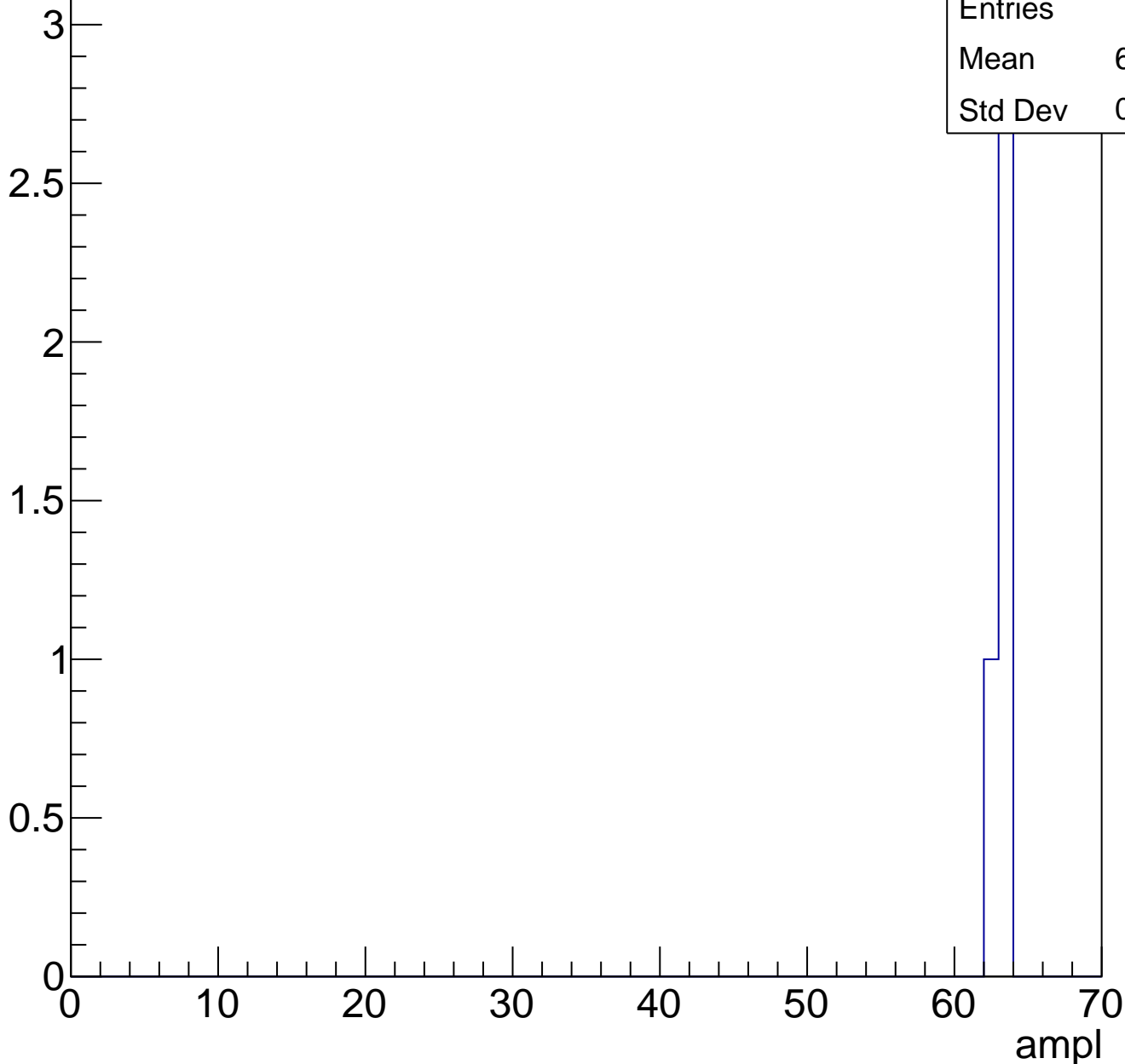
Entry



# B0L001S, U6-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U6-ch47, adc0

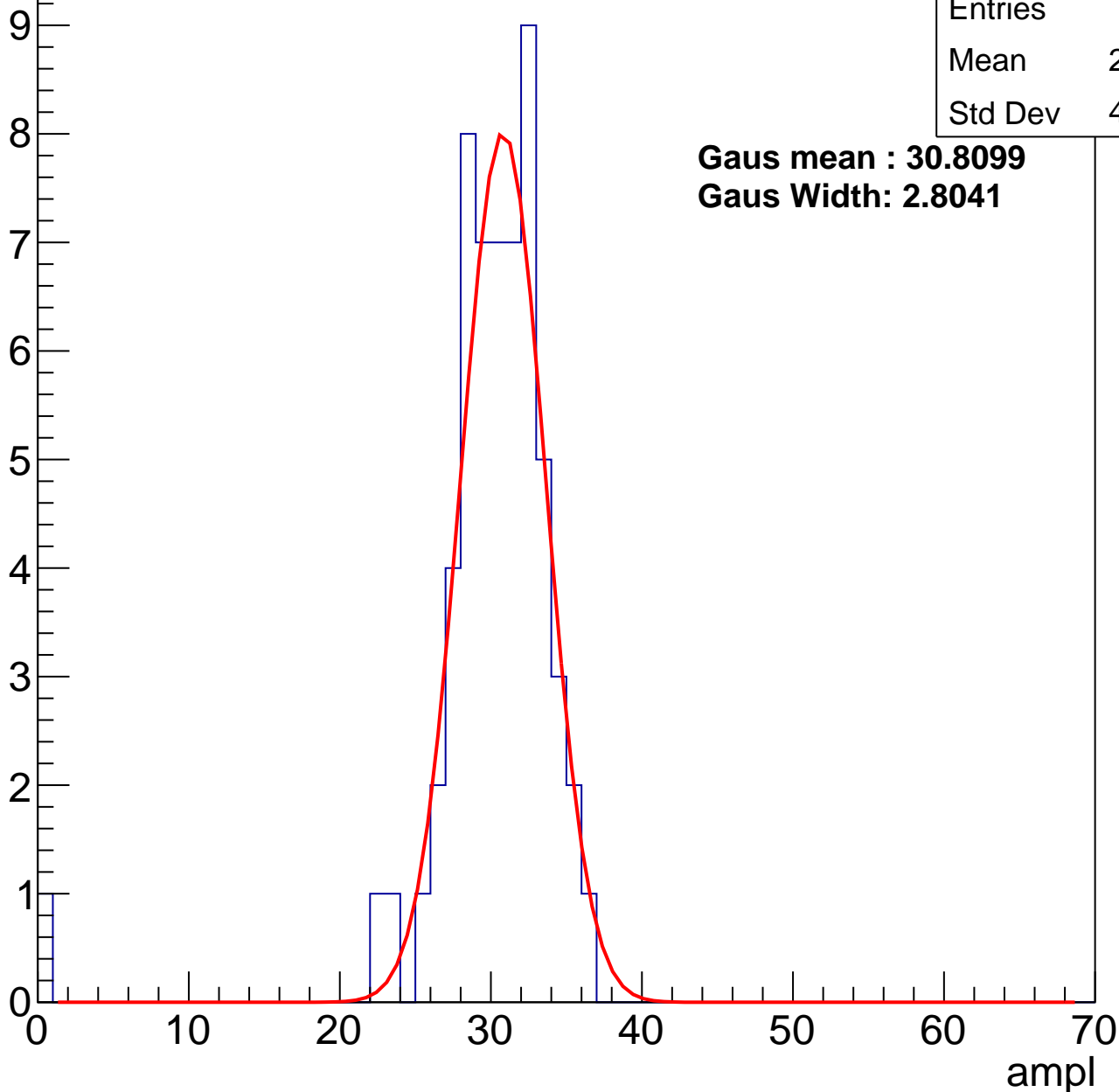
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	29.58
Std Dev	4.795

**Gaus mean : 30.8099**

**Gaus Width: 2.8041**



# B0L001S, U6-ch47, adc1

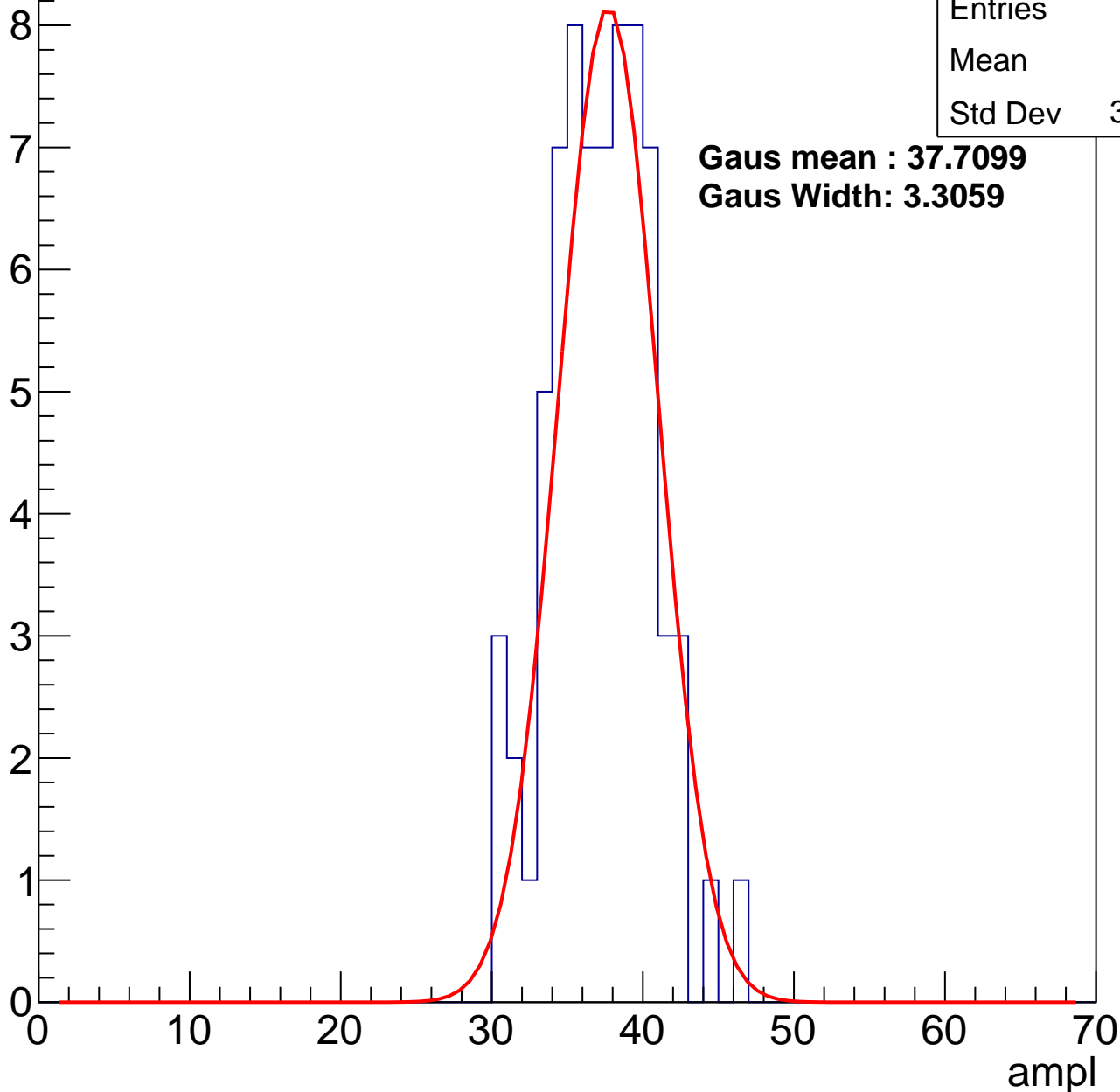
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	36.8
Std Dev	3.313

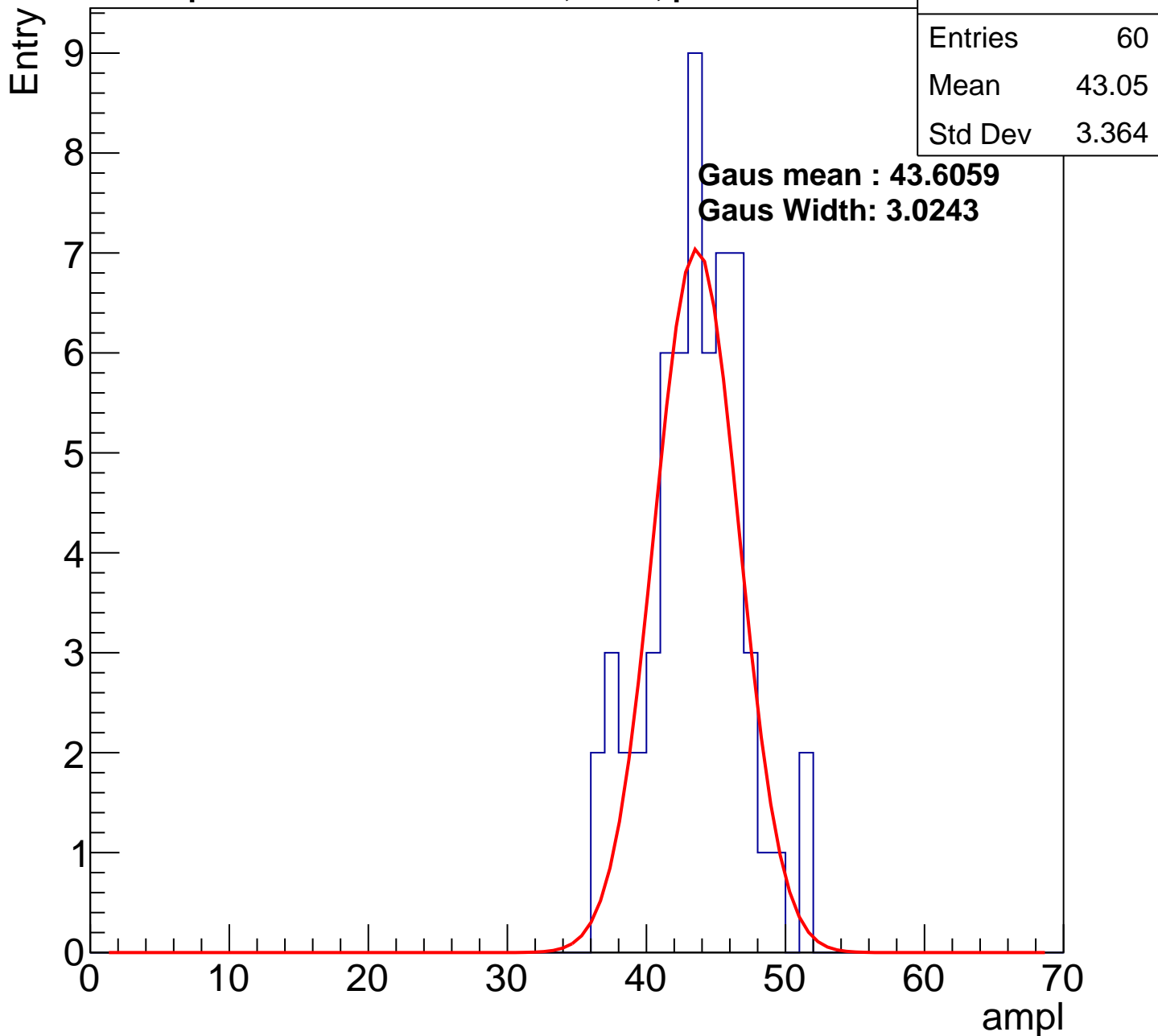
**Gaus mean : 37.7099**

**Gaus Width: 3.3059**



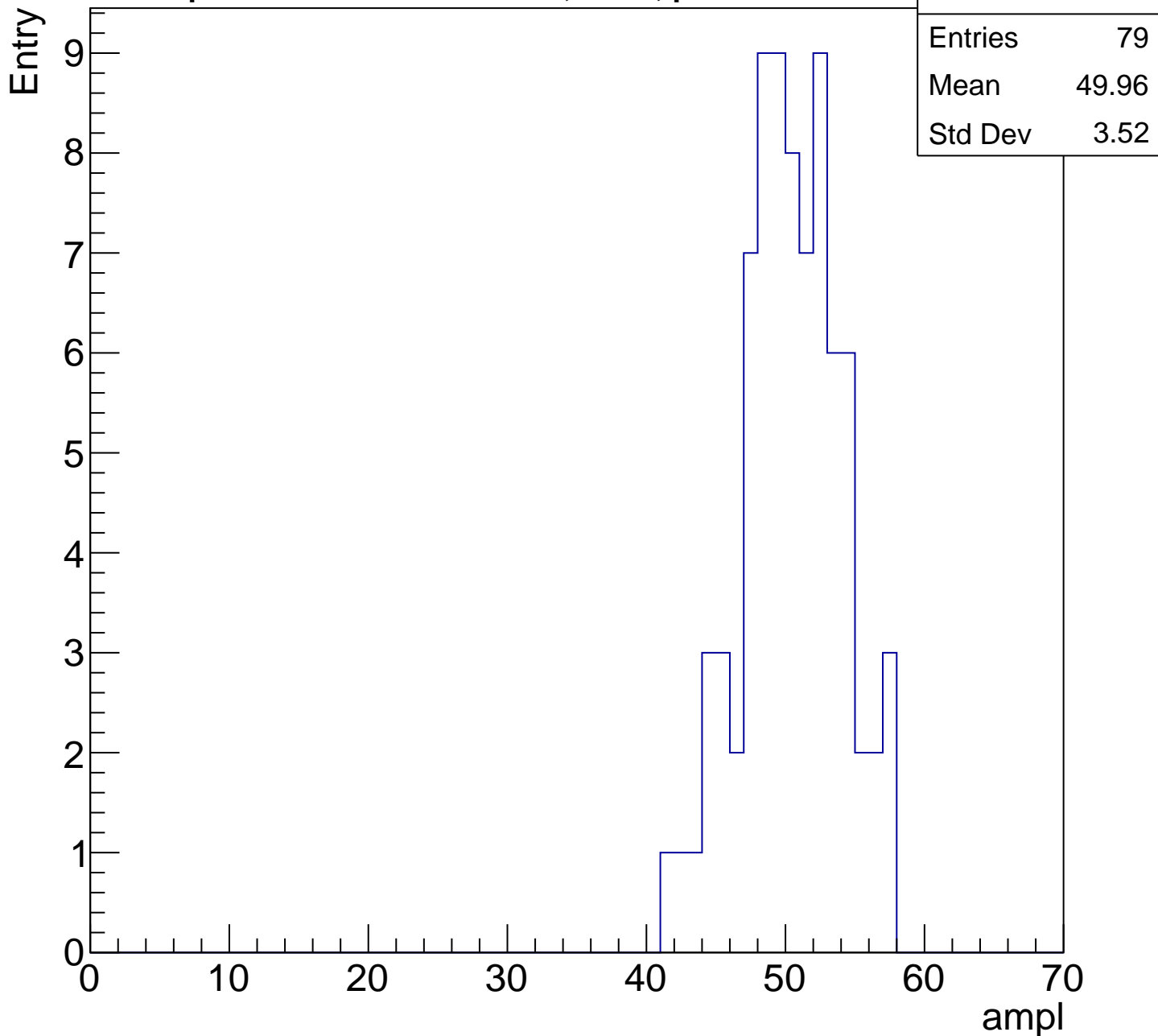
# B0L001S, U6-ch47, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1



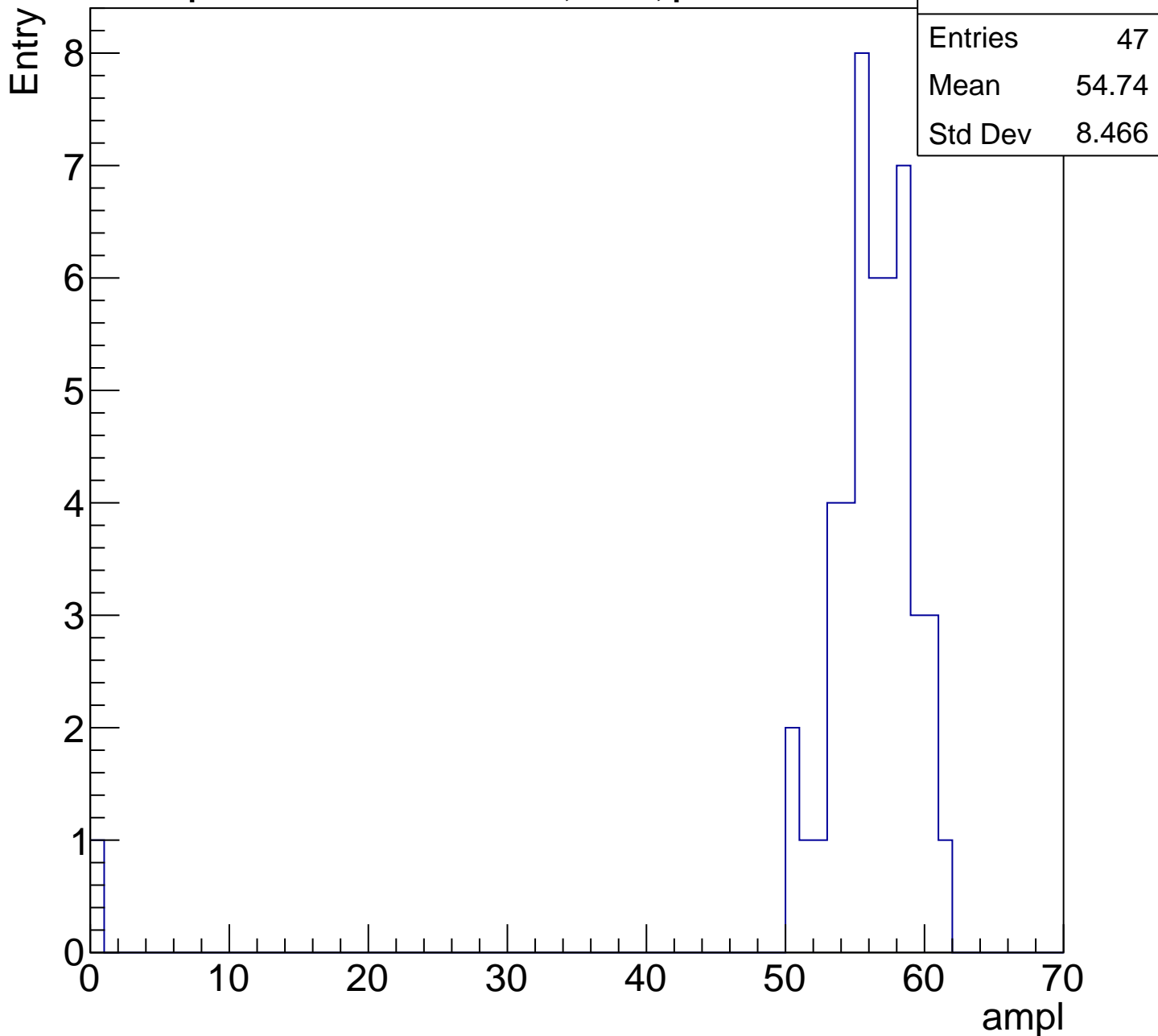
# B0L001S, U6-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U6-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

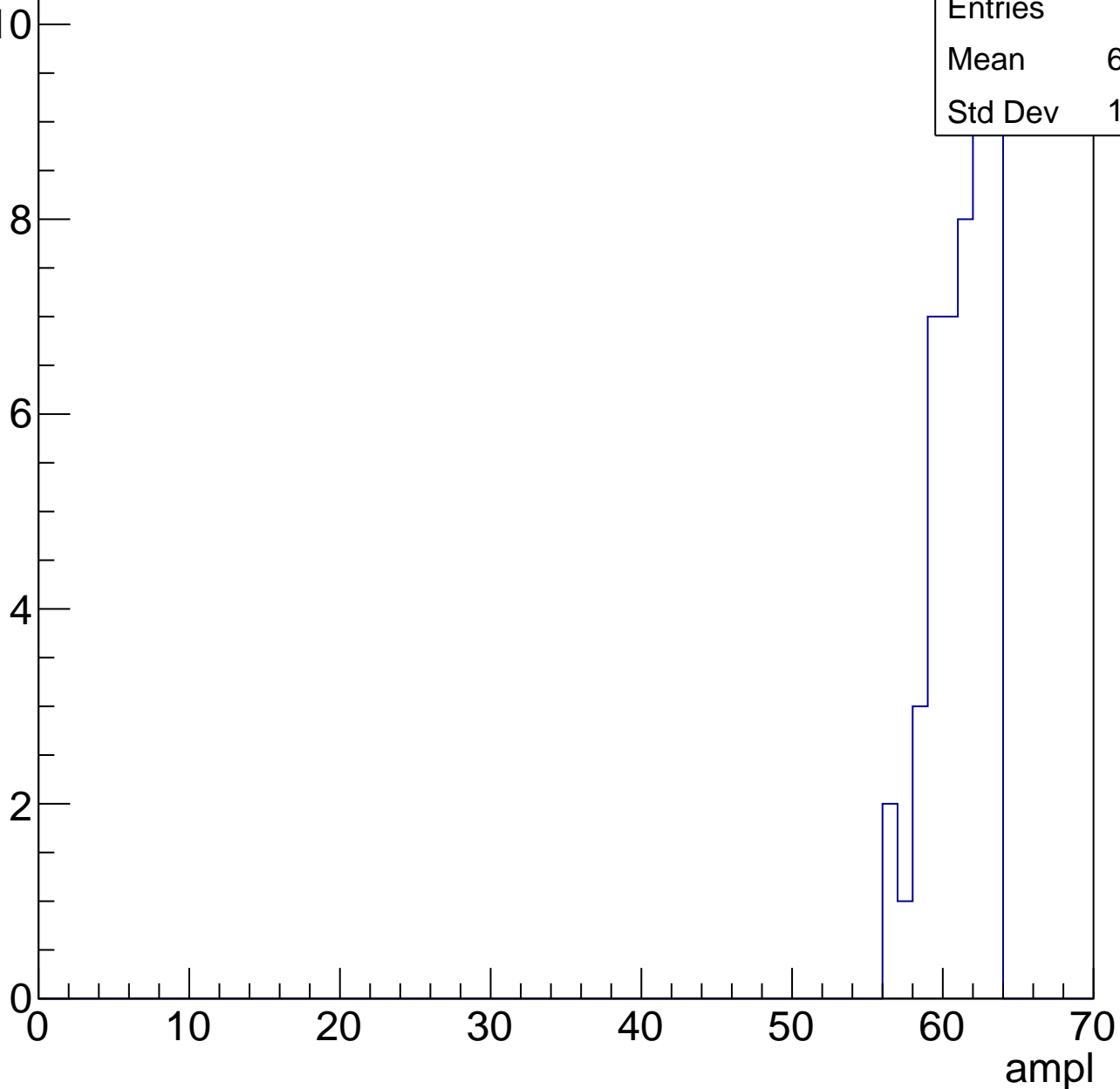


# B0L001S, U6-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

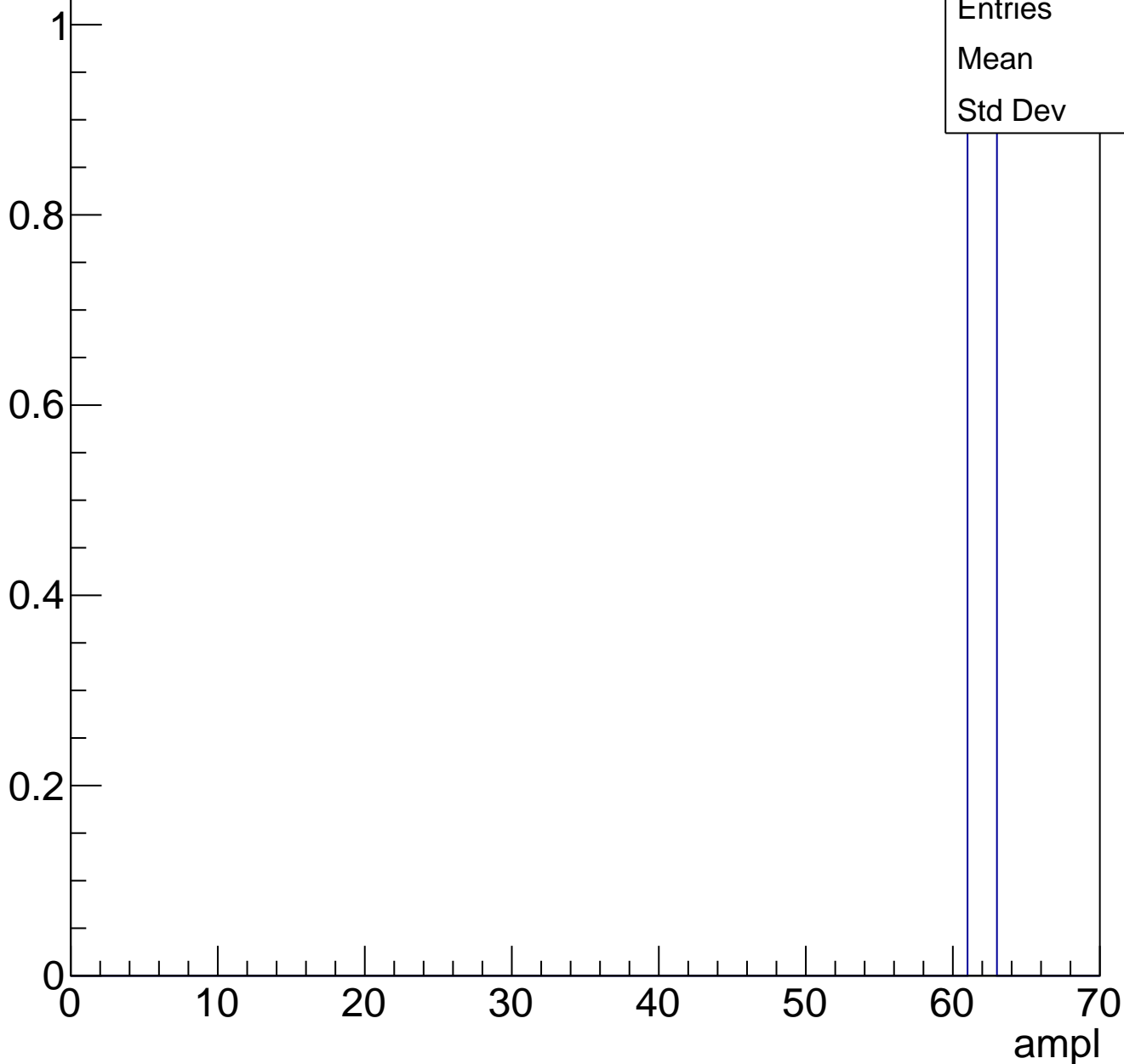
Entries	47
Mean	60.68
Std Dev	1.914



# B0L001S, U6-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U6-ch48, adc0

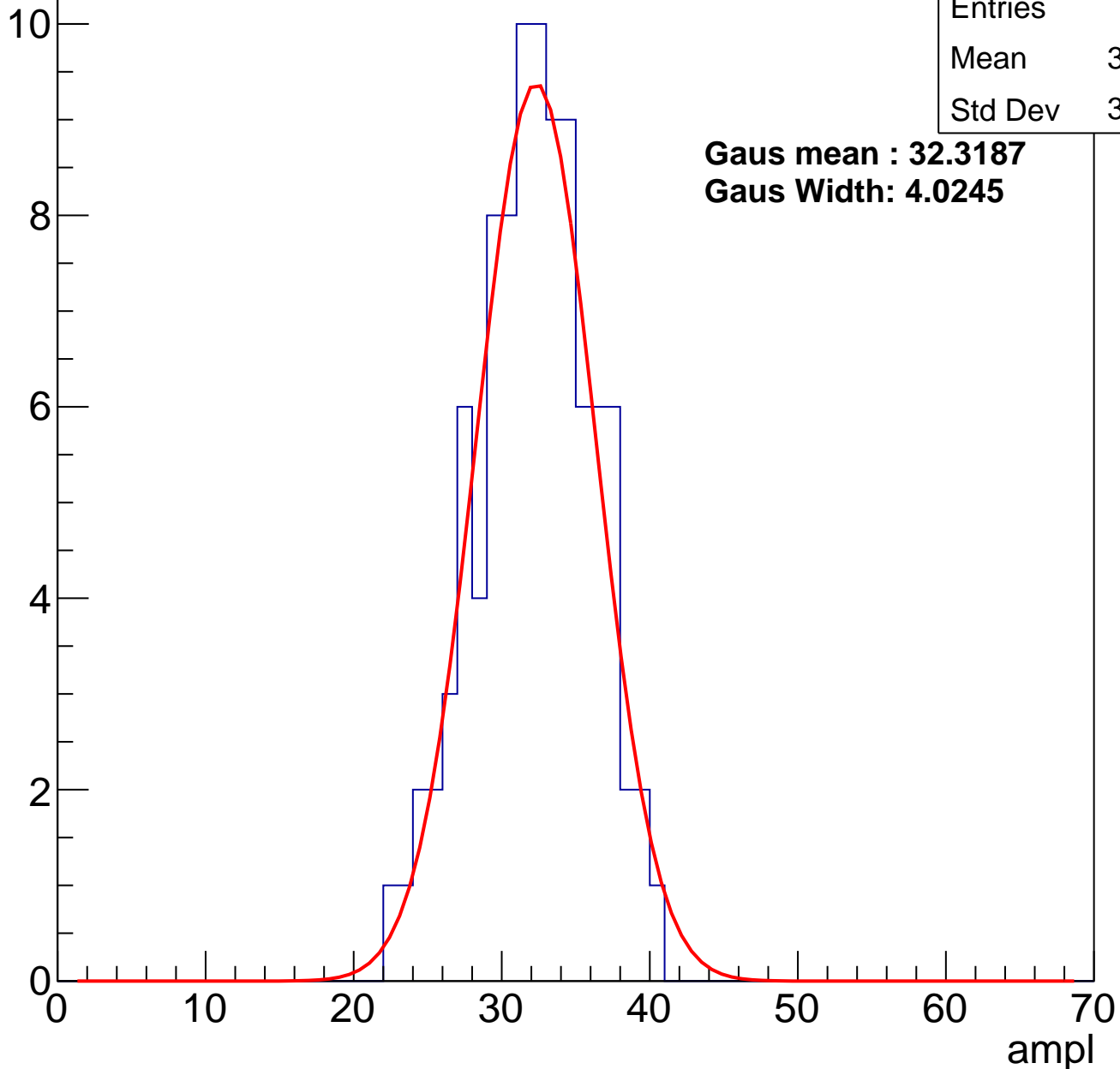
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	96
Mean	31.69
Std Dev	3.836

**Gaus mean : 32.3187**

**Gaus Width: 4.0245**

Entry



# B0L001S, U6-ch48, adc1

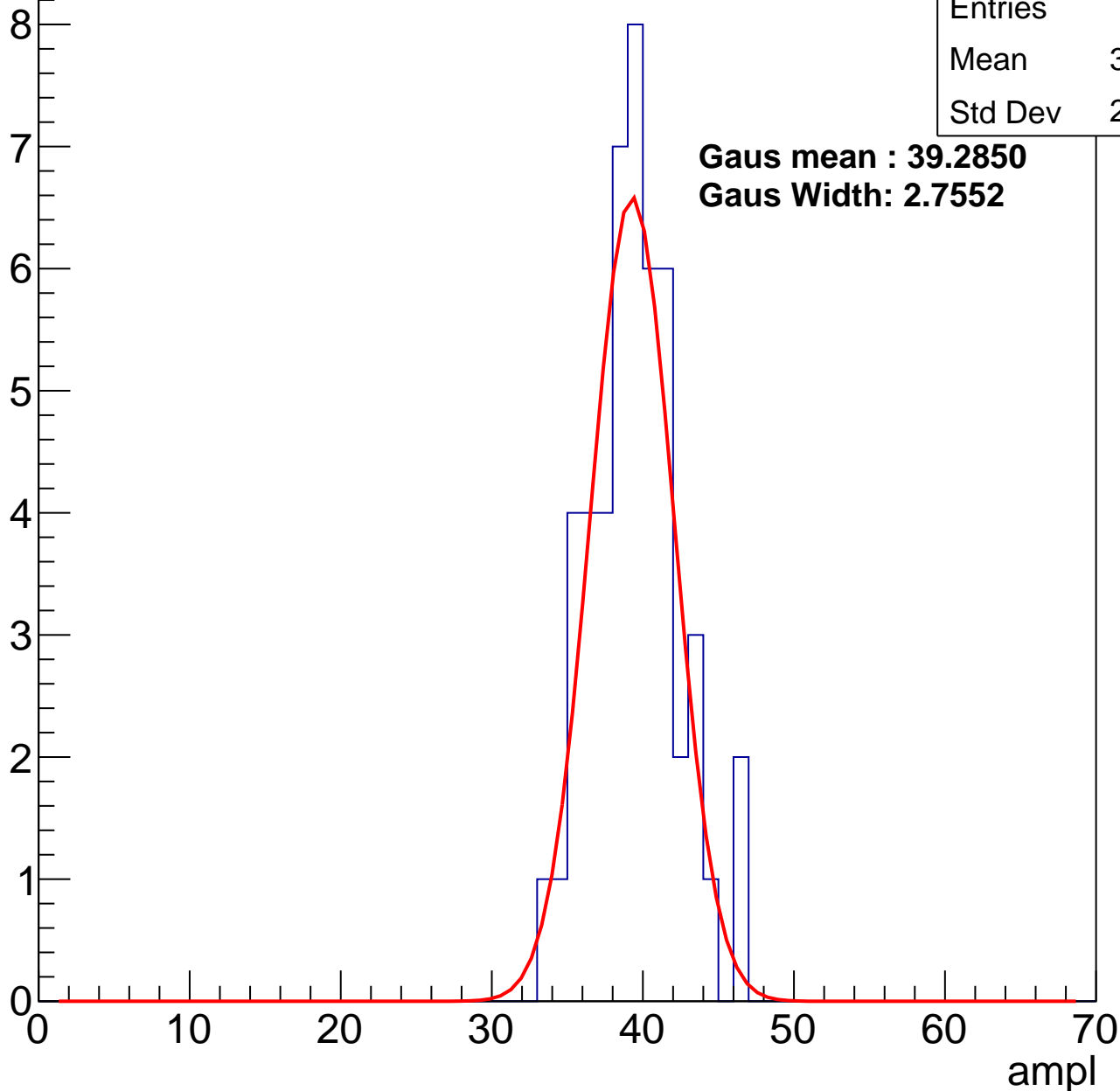
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	39.02
Std Dev	2.868

**Gaus mean : 39.2850**

**Gaus Width: 2.7552**



# B0L001S, U6-ch48, adc2

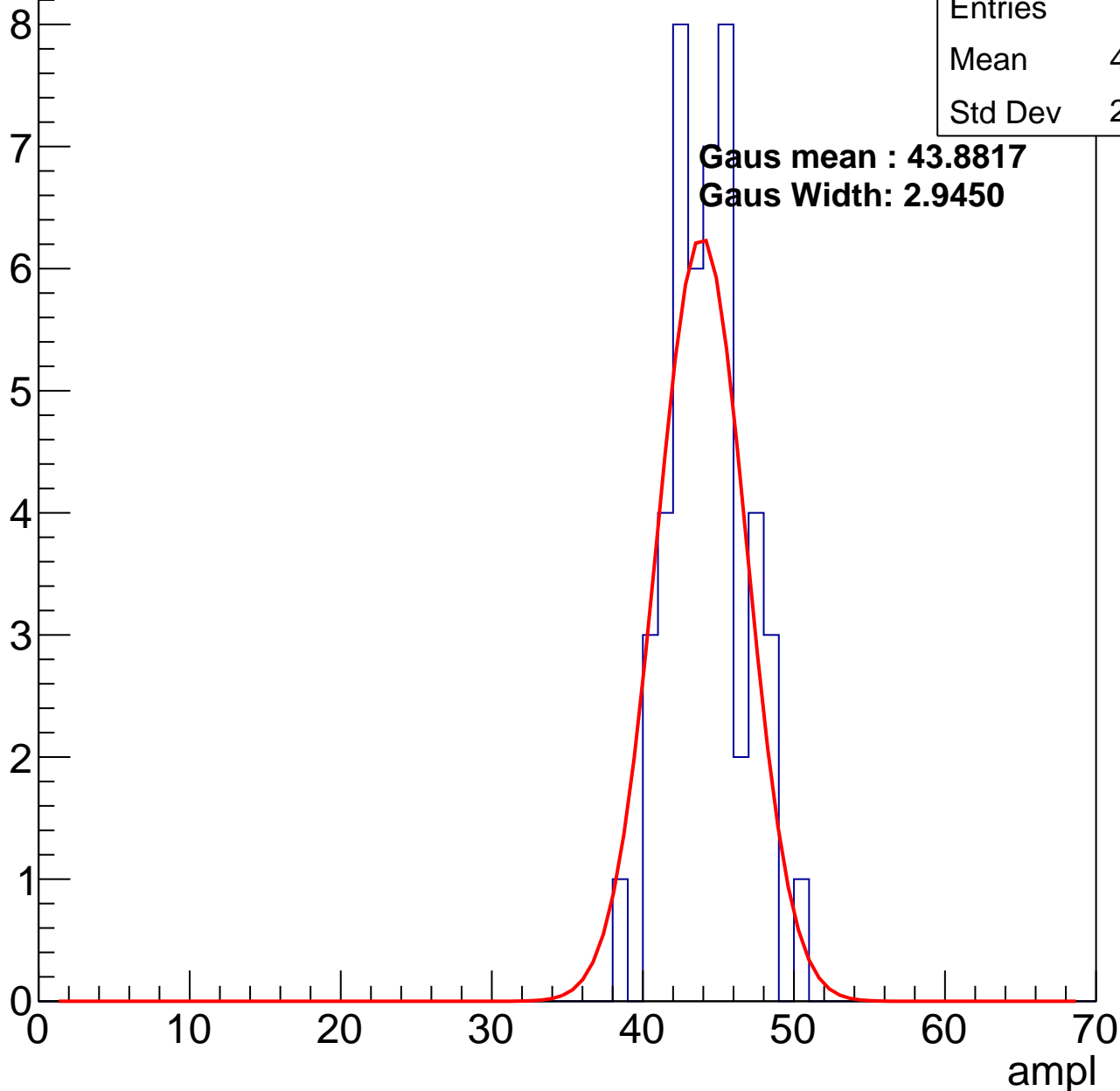
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	43.79
Std Dev	2.492

**Gaus mean : 43.8817**

**Gaus Width: 2.9450**

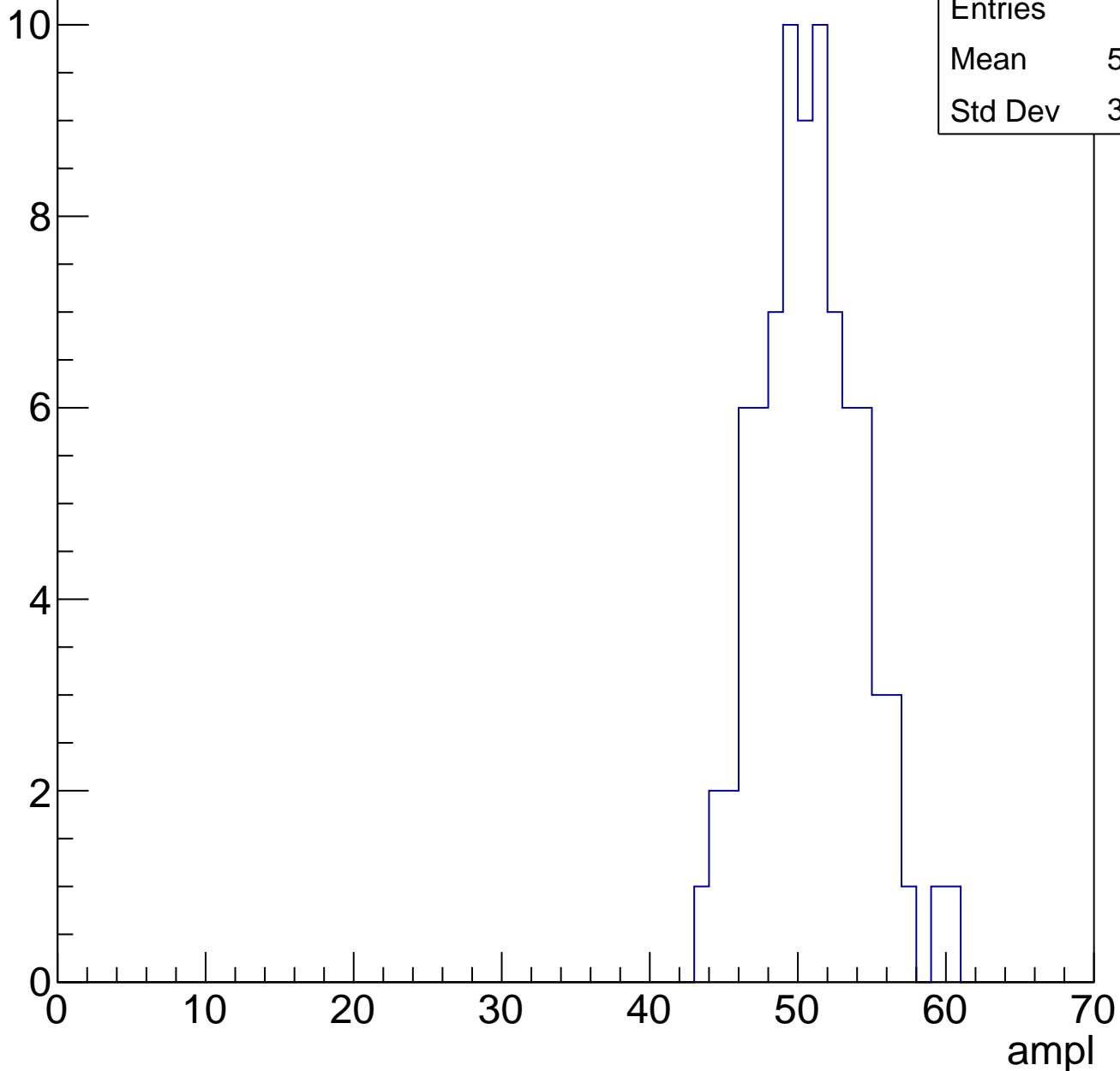


# B0L001S, U6-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	81
Mean	50.37
Std Dev	3.423

Entry

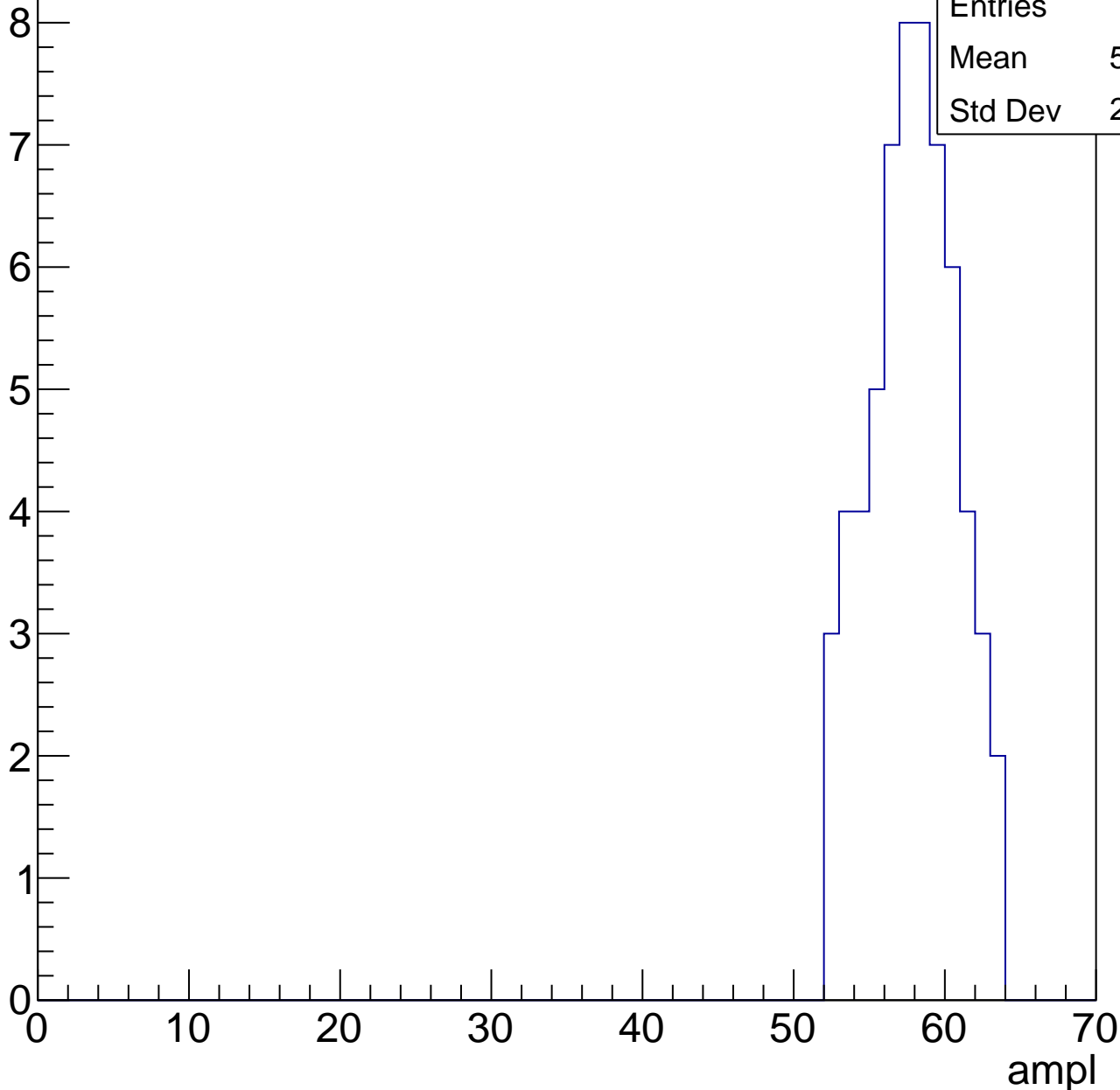


# B0L001S, U6-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	57.38
Std Dev	2.847

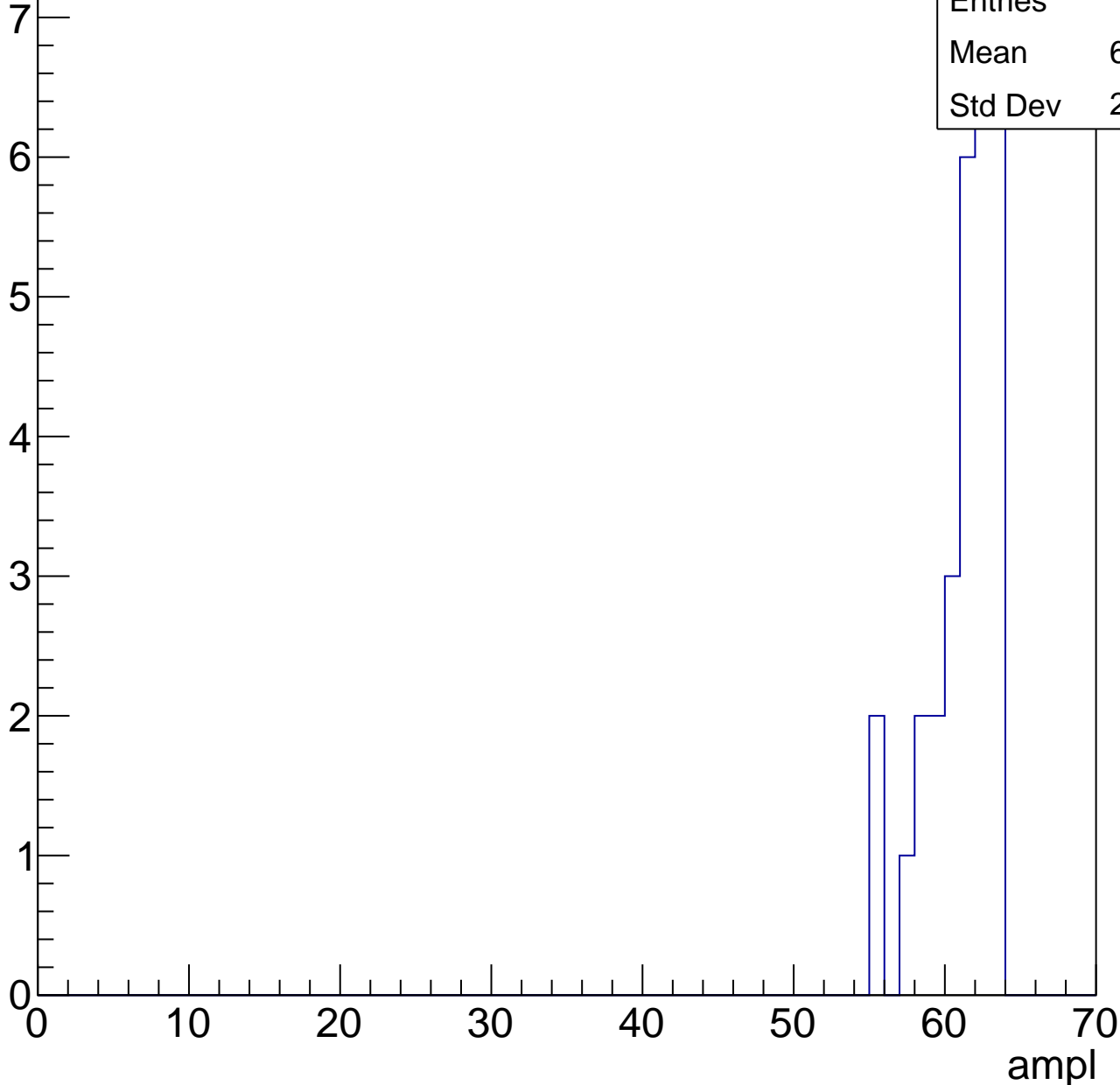


# B0L001S, U6-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

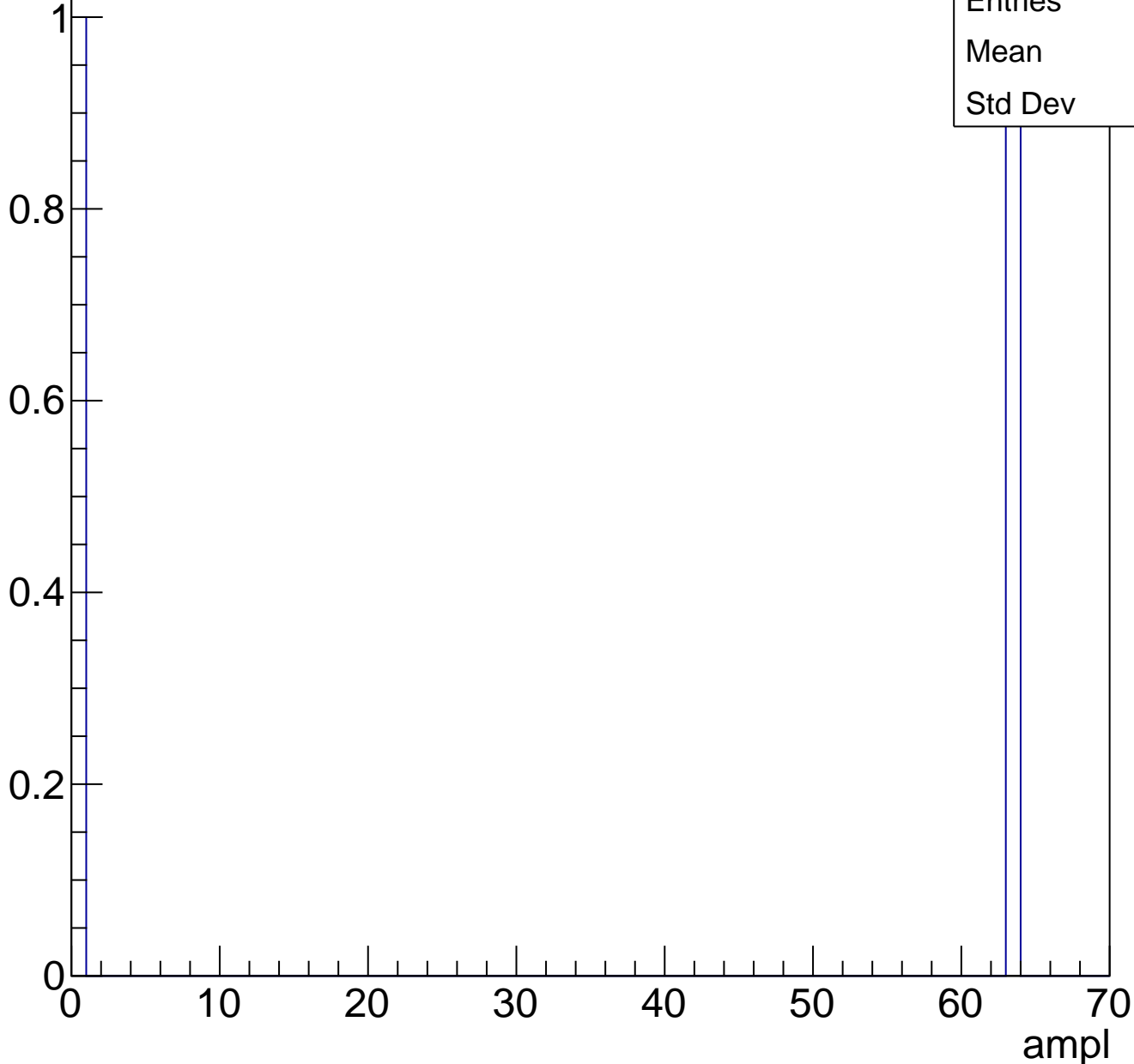
Entries	30
Mean	60.73
Std Dev	2.235



# B0L001S, U6-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

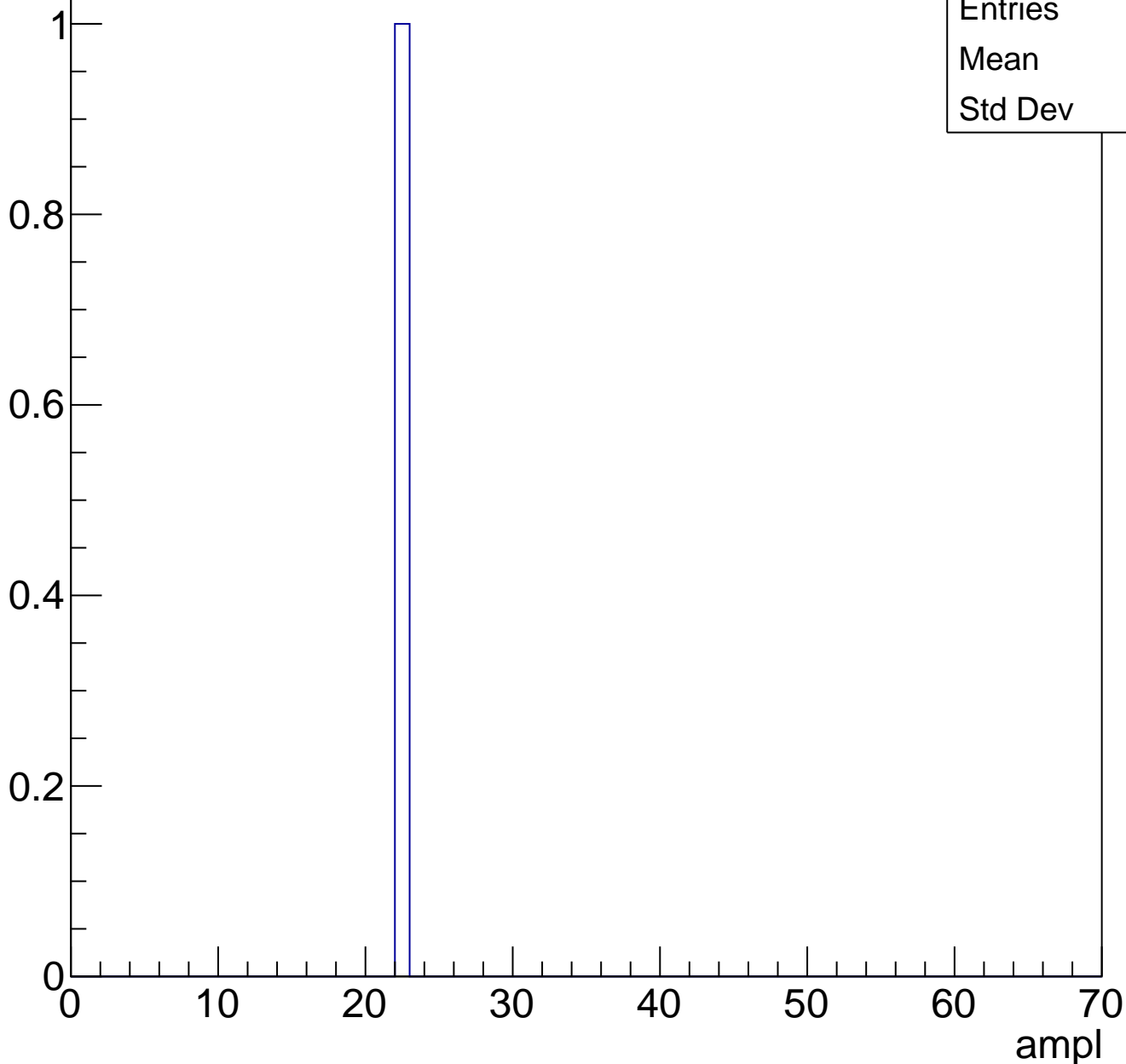




# B0L001S, U6-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch49, adc0

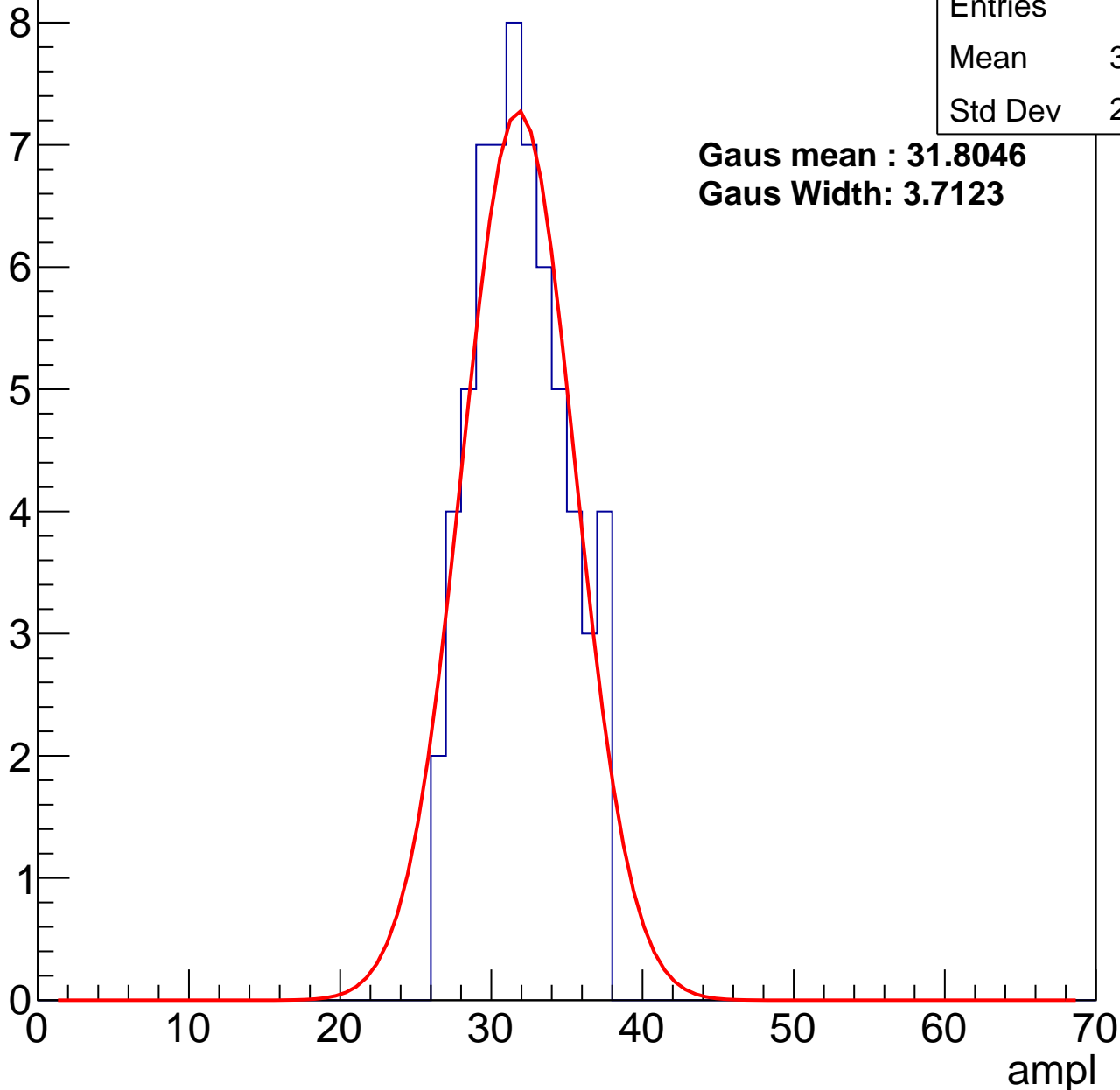
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	31.44
Std Dev	2.955

**Gaus mean : 31.8046**

**Gaus Width: 3.7123**



# B0L001S, U6-ch49, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	70
Mean	37.94
Std Dev	3.084

**Gaus mean : 38.6916**

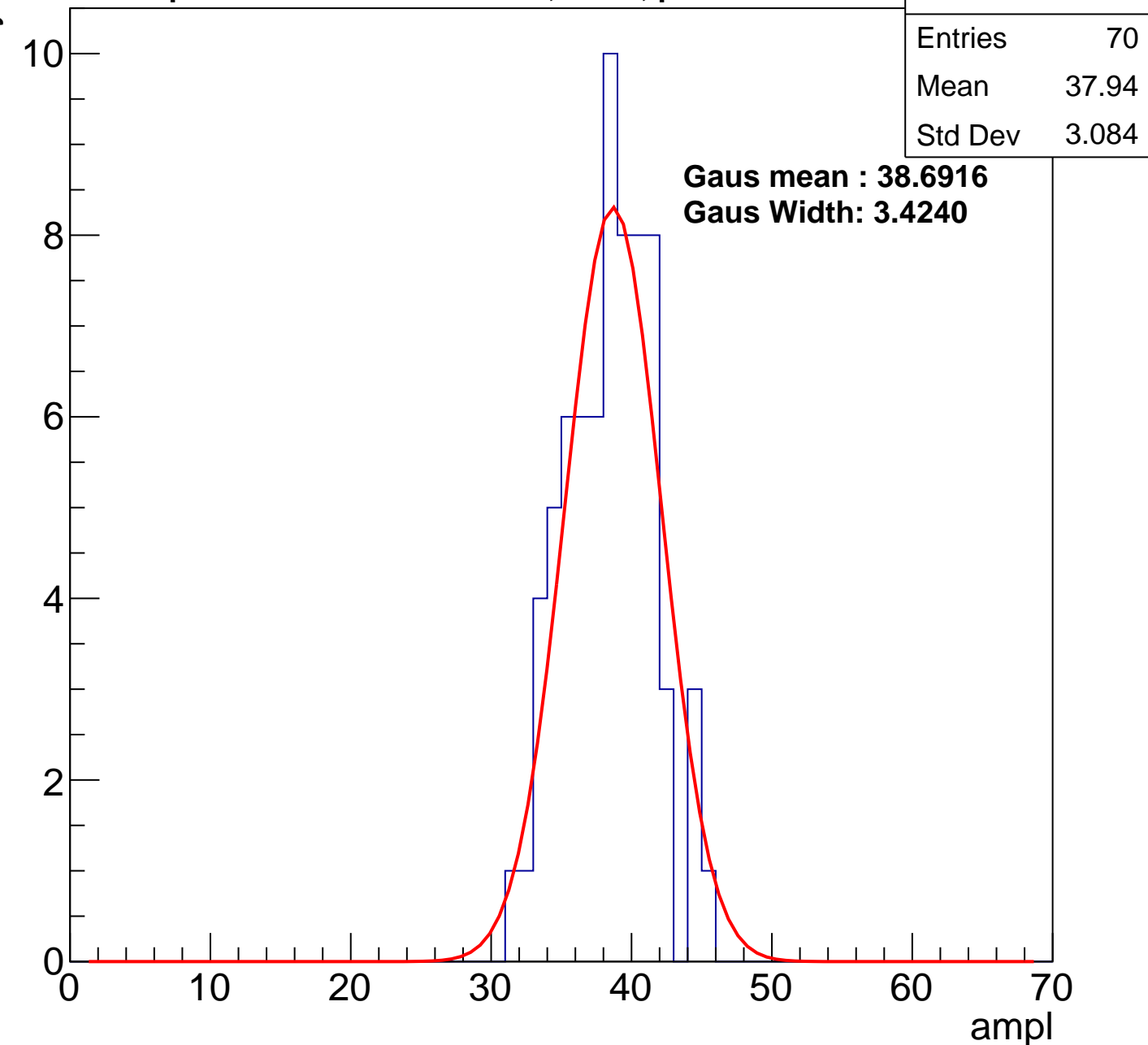
**Gaus Width: 3.4240**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U6-ch49, adc2

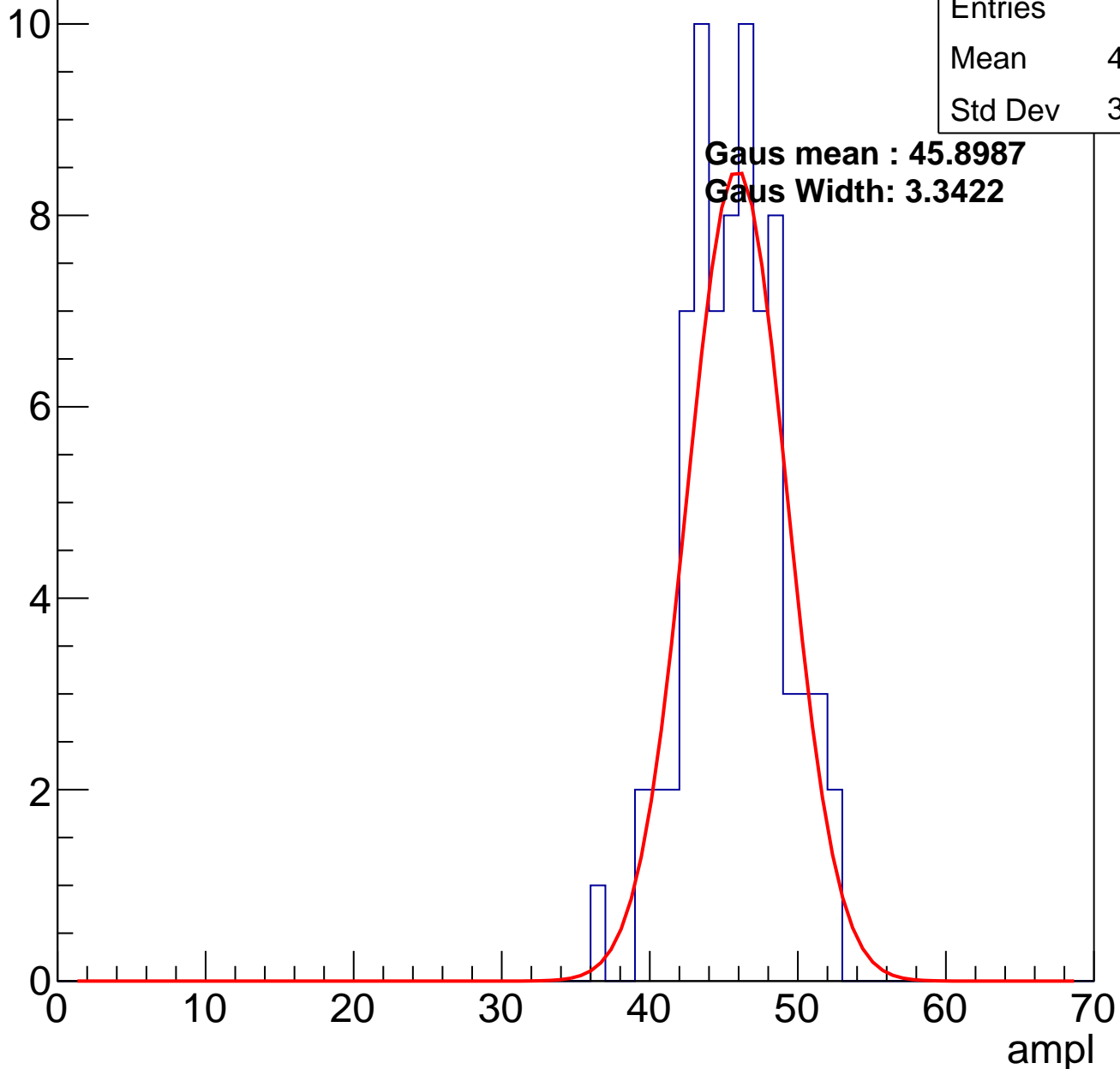
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	75
Mean	45.27
Std Dev	3.222

**Gaus mean : 45.8987**

**Gaus Width: 3.3422**

Entry

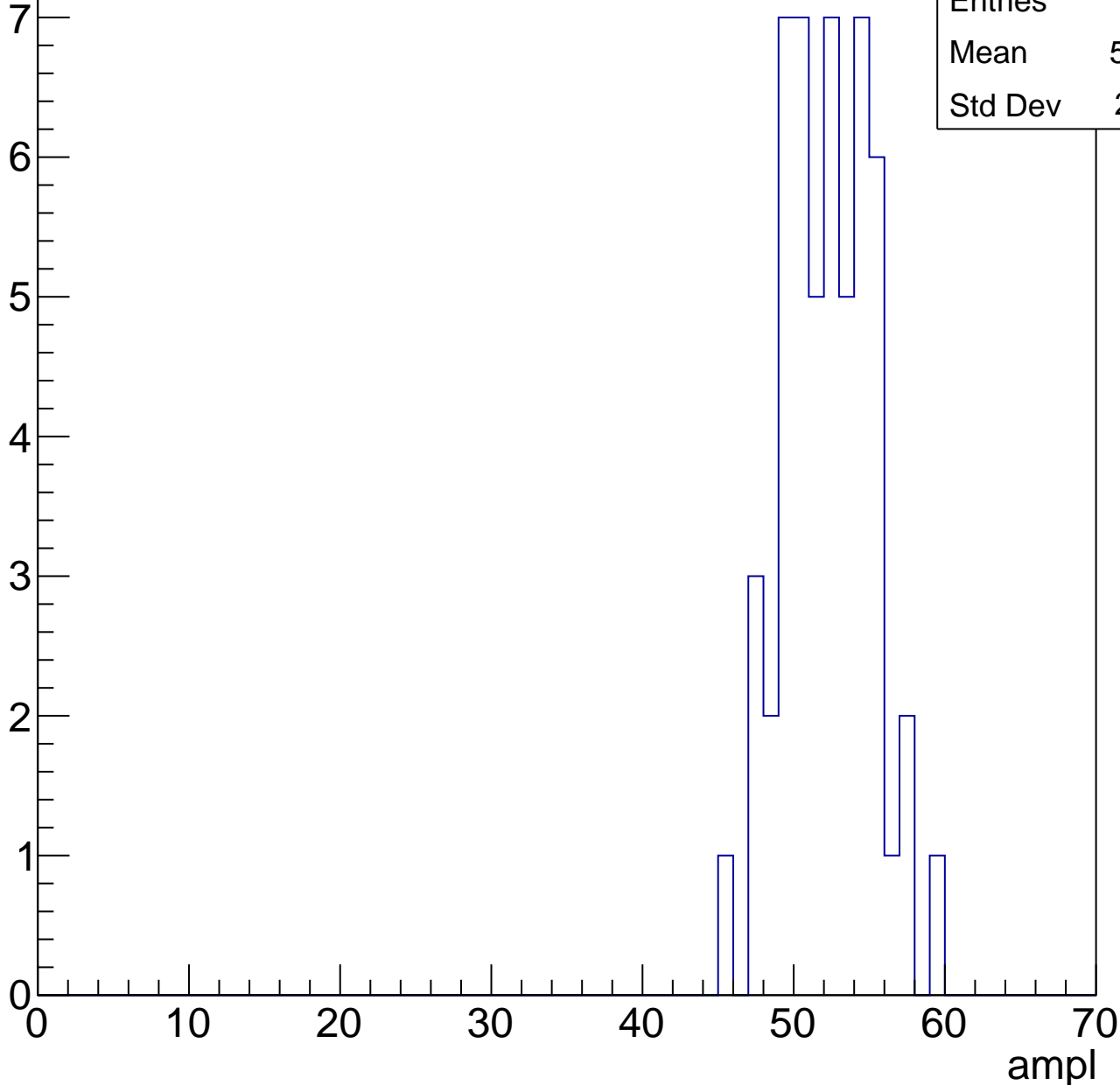


# B0L001S, U6-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	51.78
Std Dev	2.891

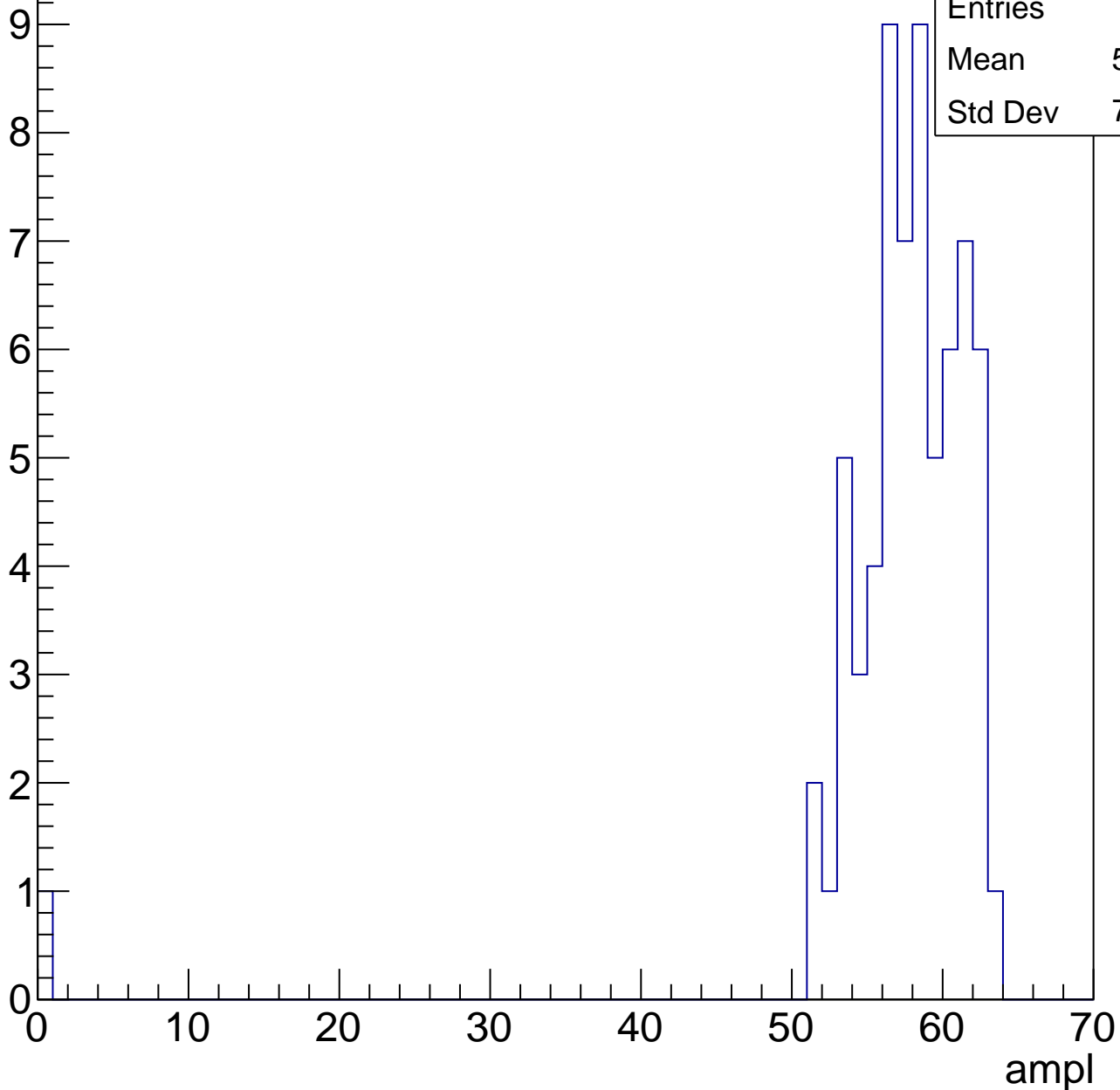


# B0L001S, U6-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	56.71
Std Dev	7.641

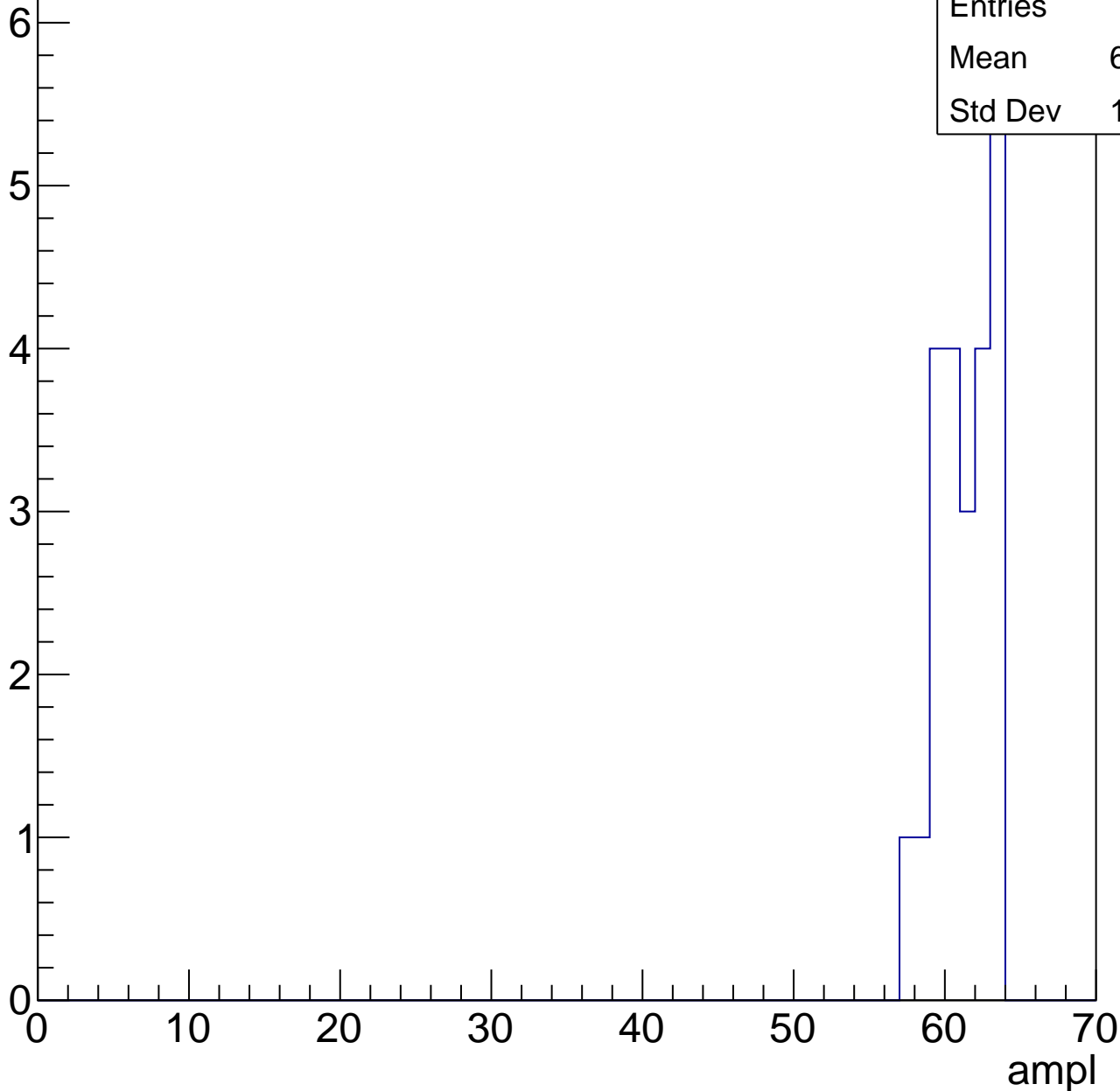


# B0L001S, U6-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	23
Mean	60.87
Std Dev	1.777



# B0L001S, U6-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



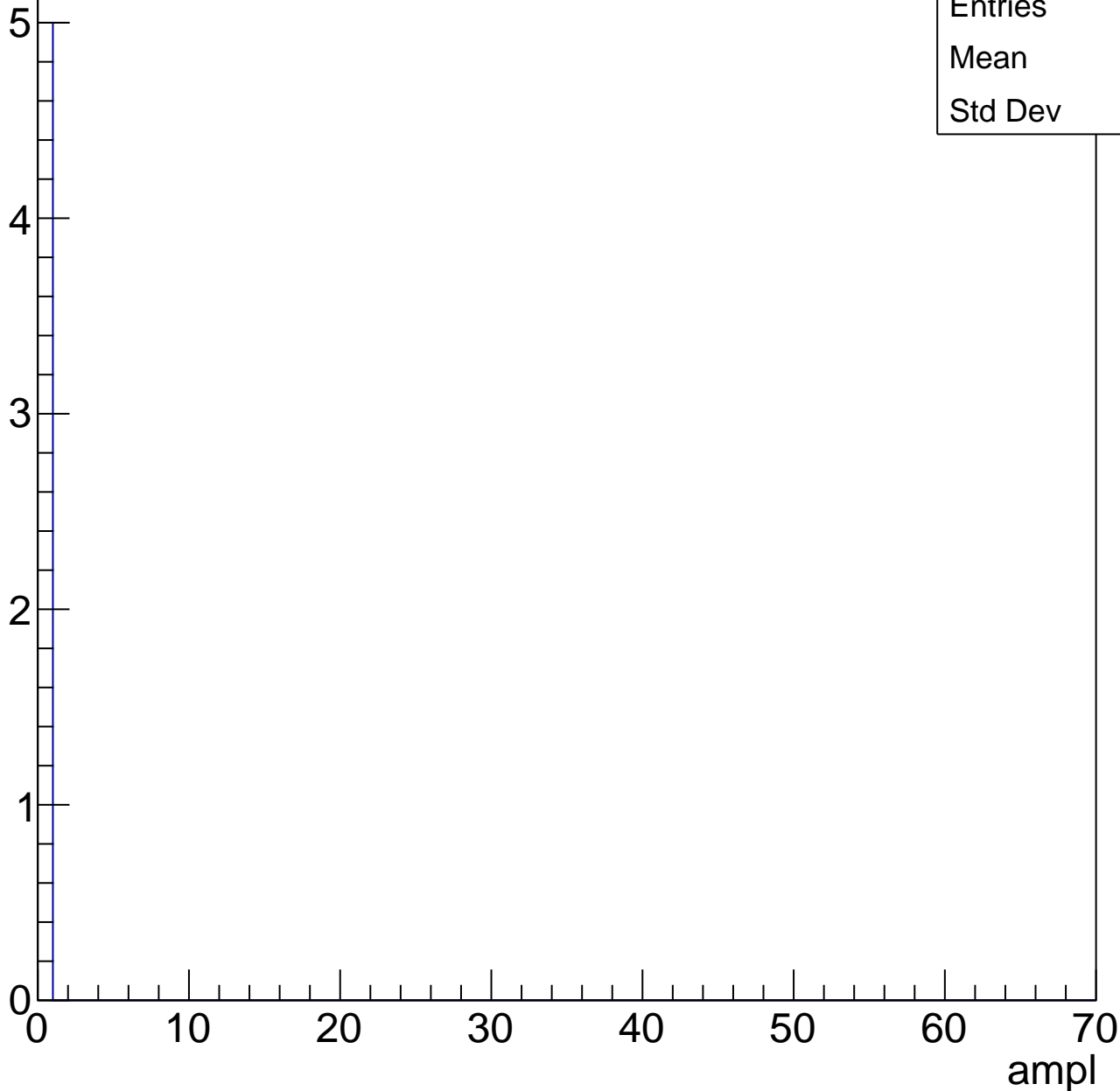


# B0L001S, U6-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	5
Mean	0
Std Dev	0



# B0L001S, U6-ch50, adc0

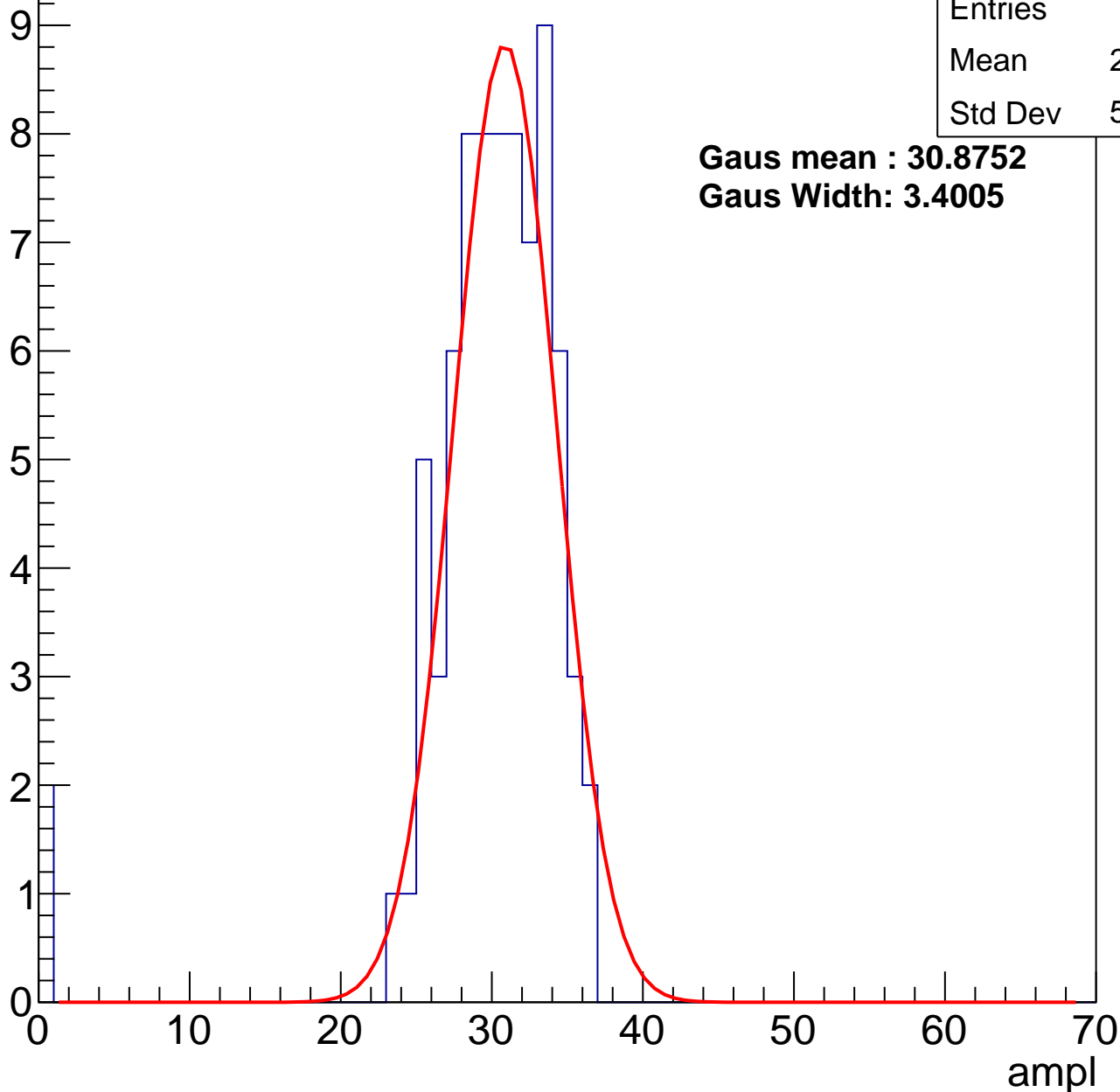
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	29.32
Std Dev	5.672

**Gaus mean : 30.8752**

**Gaus Width: 3.4005**



# B0L001S, U6-ch50, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	66
Mean	37.05
Std Dev	3.314

**Gaus mean : 38.0783**

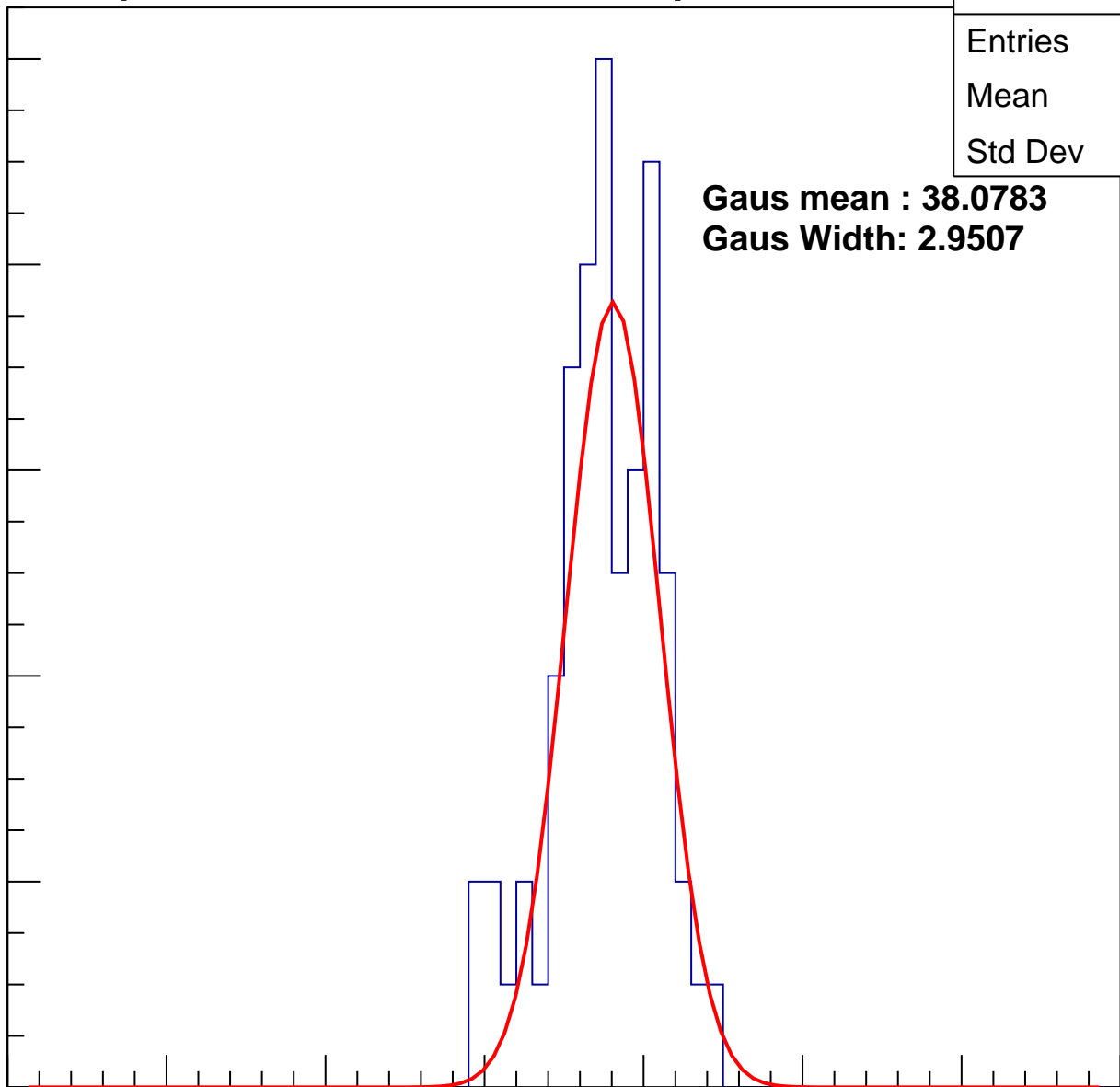
**Gaus Width: 2.9507**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U6-ch50, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	72
Mean	44.18
Std Dev	3.469

**Gaus mean : 45.0910**

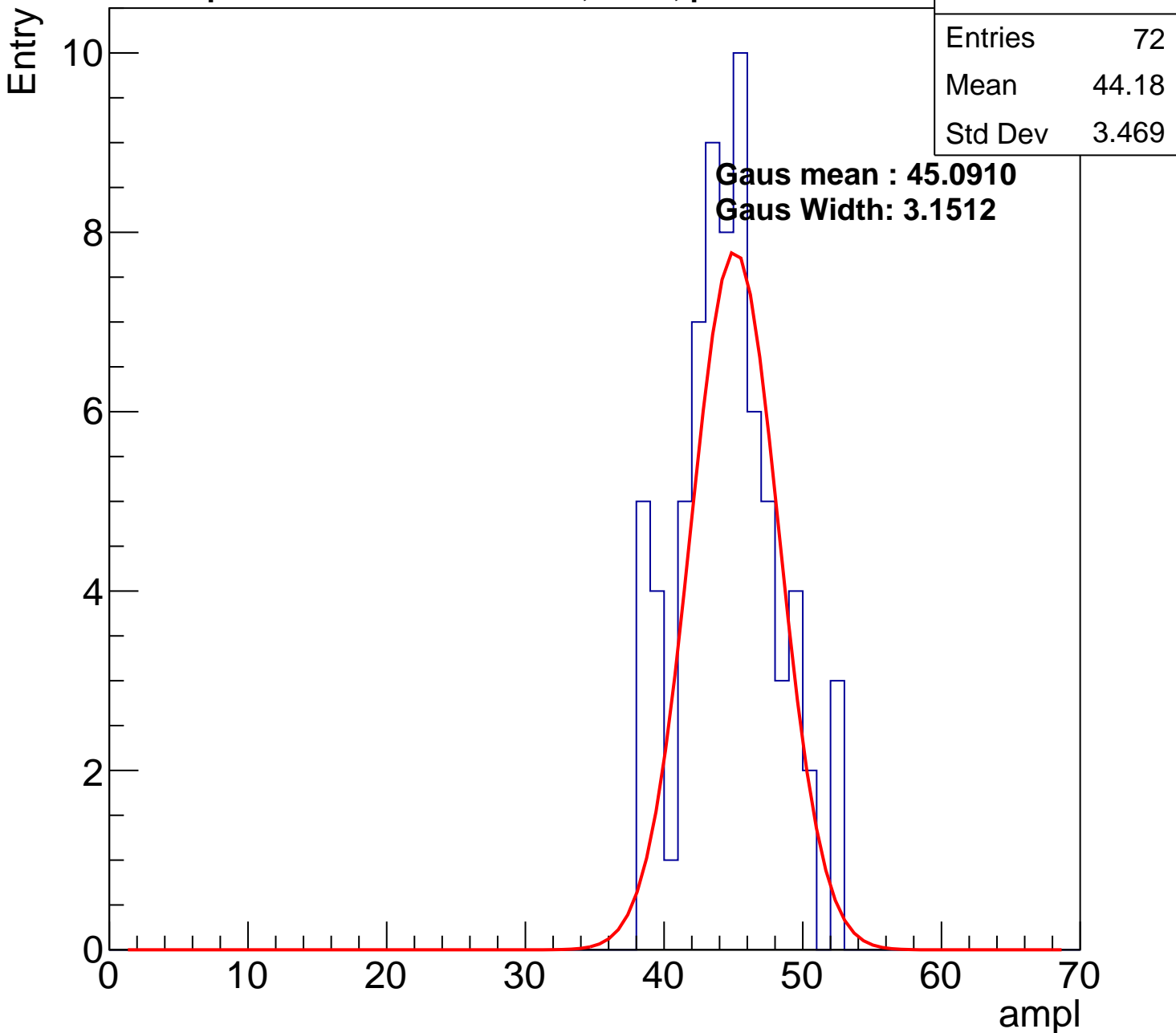
**Gaus Width: 3.1512**

Entry

10  
8  
6  
4  
2  
0

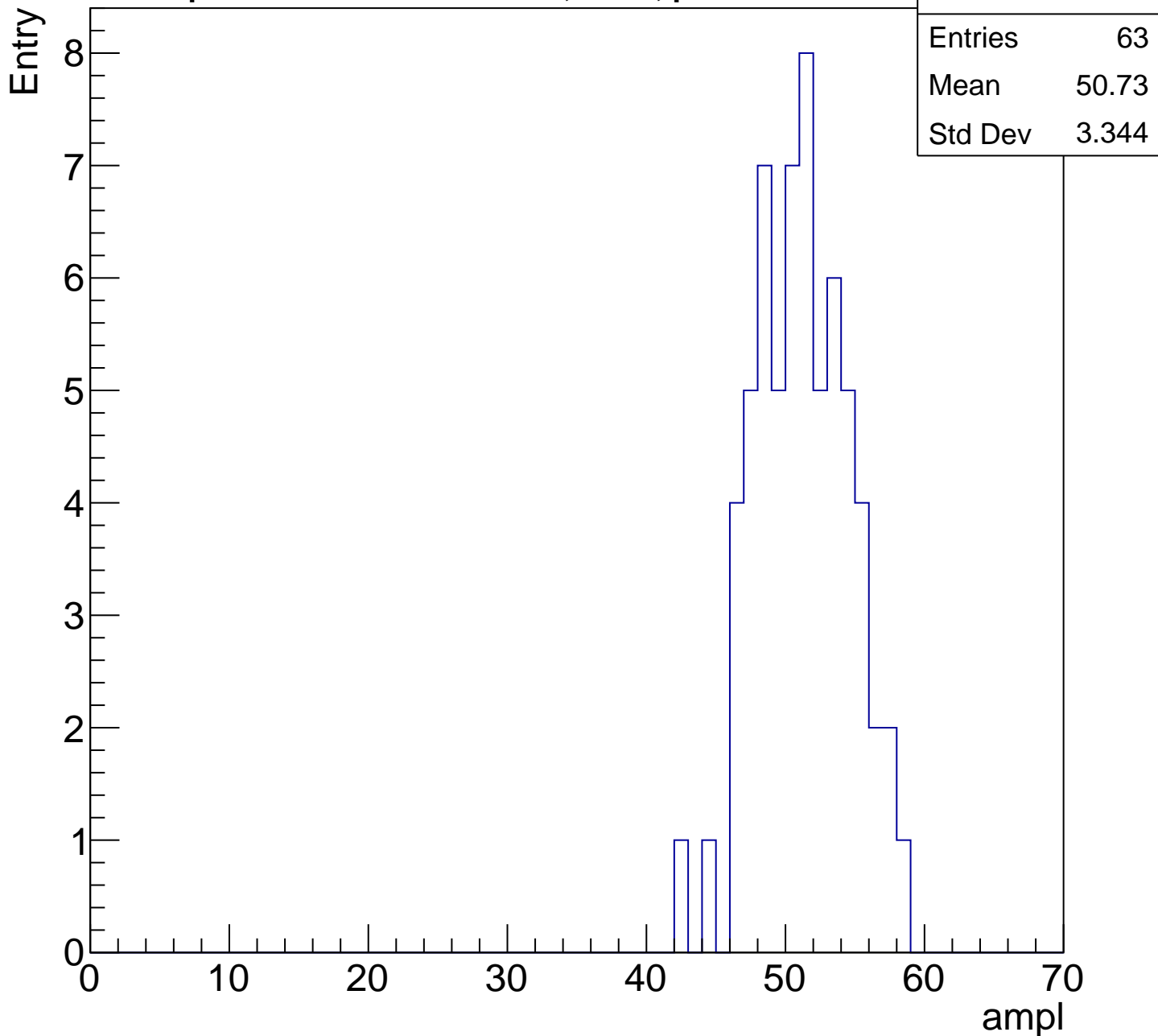
ampl

0 10 20 30 40 50 60 70



# B0L001S, U6-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

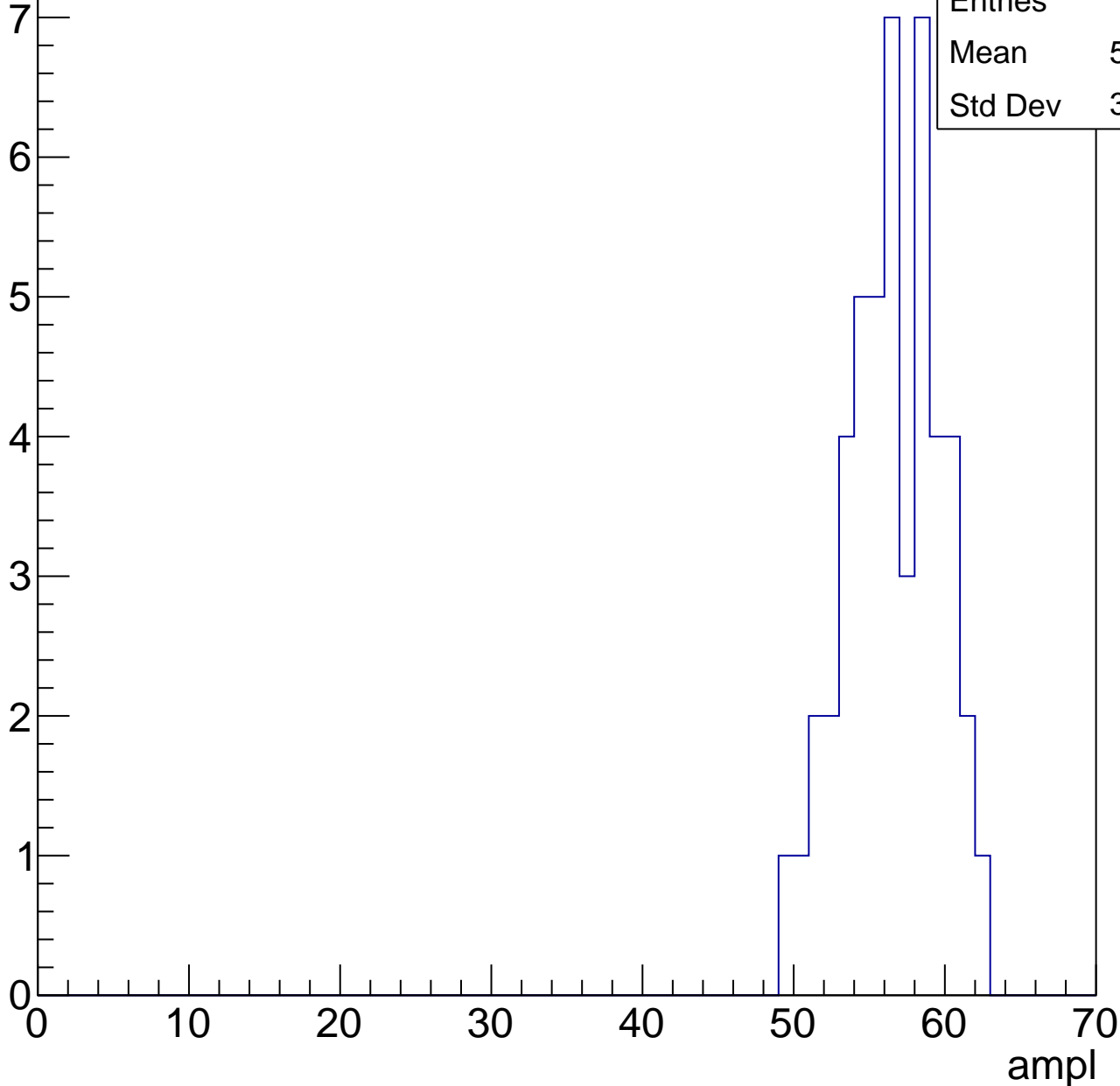


# B0L001S, U6-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	56.06
Std Dev	3.044

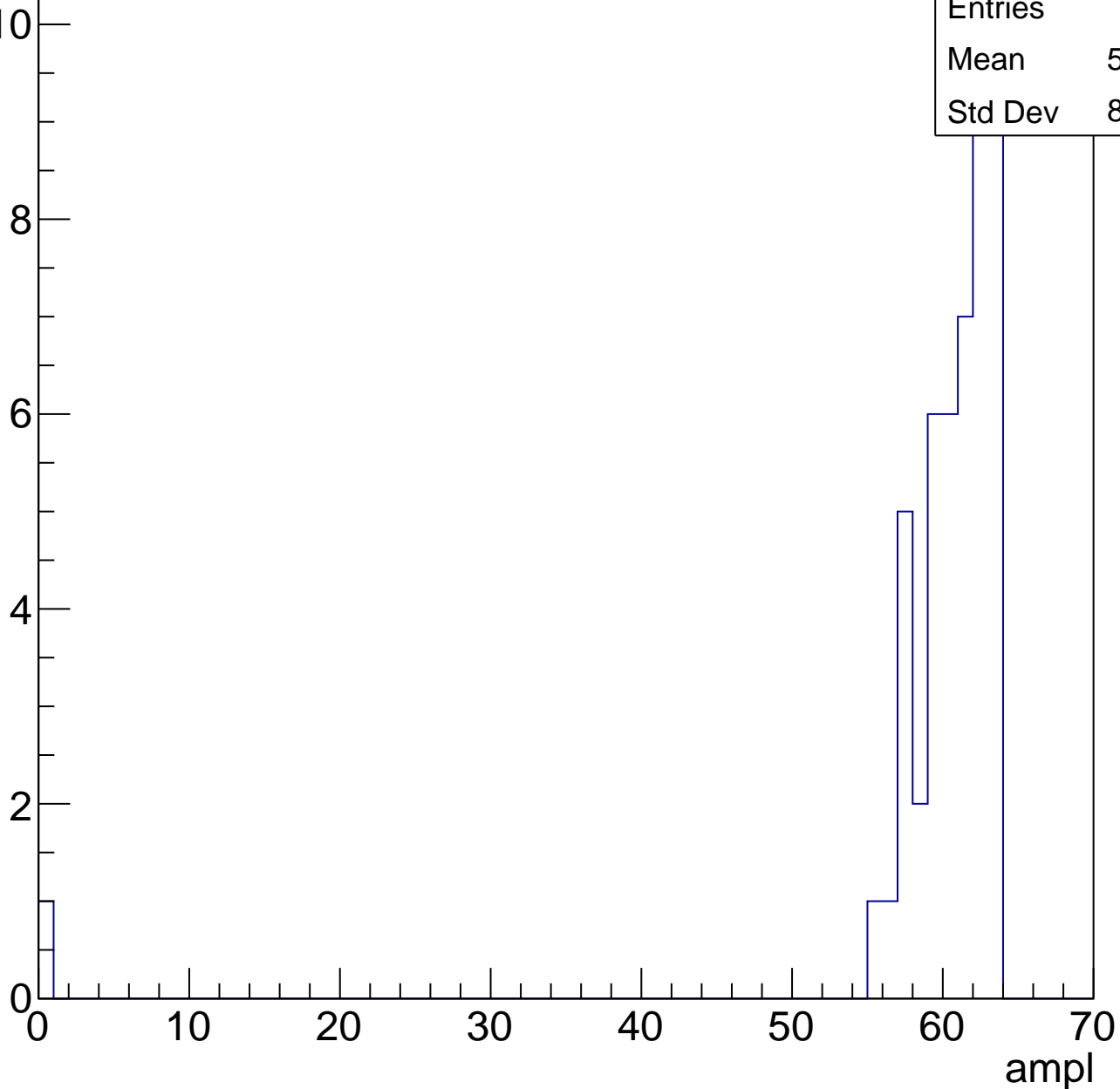


# B0L001S, U6-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

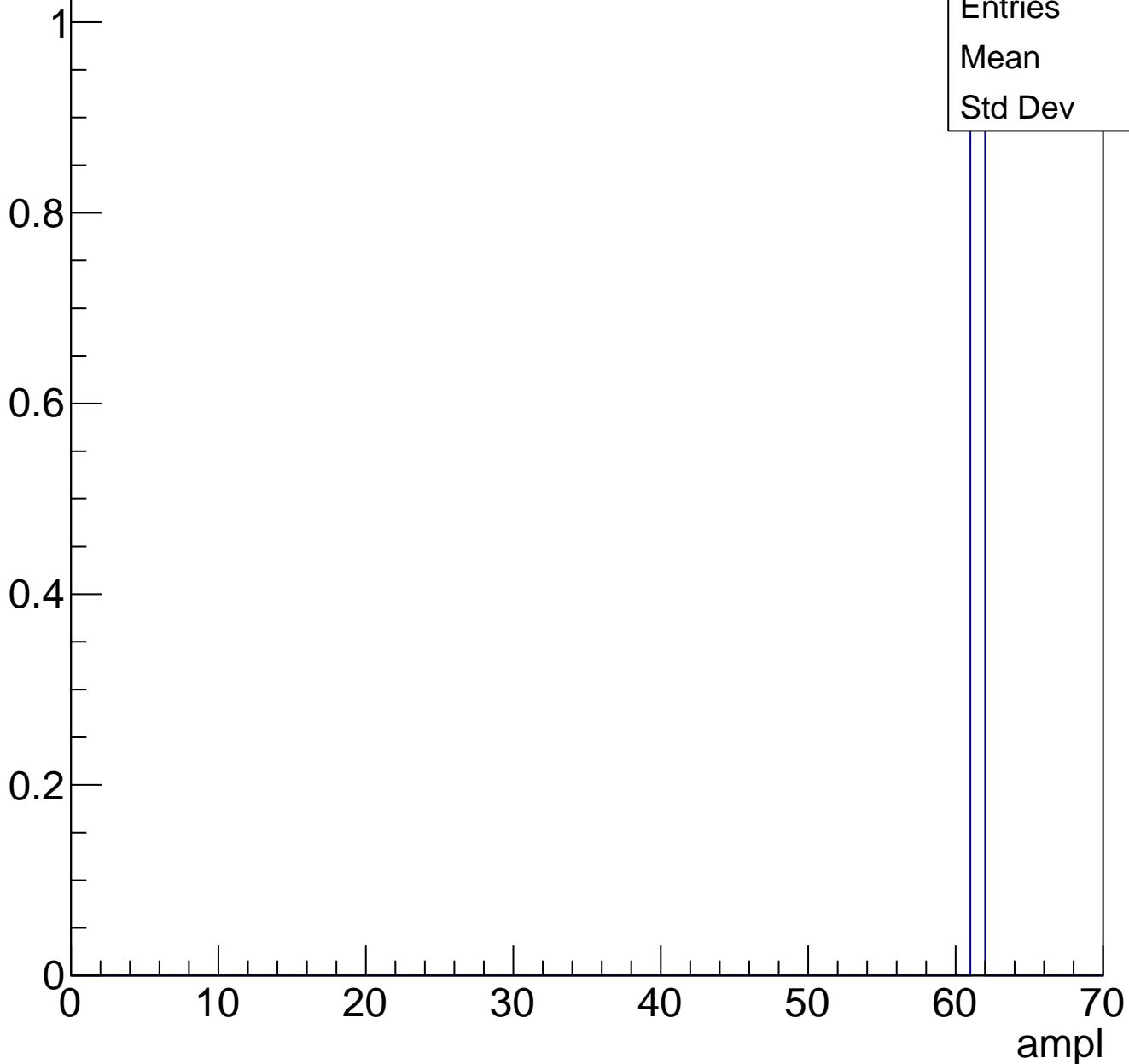
Entries	48
Mean	59.19
Std Dev	8.899



# B0L001S, U6-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U6-ch51, adc0

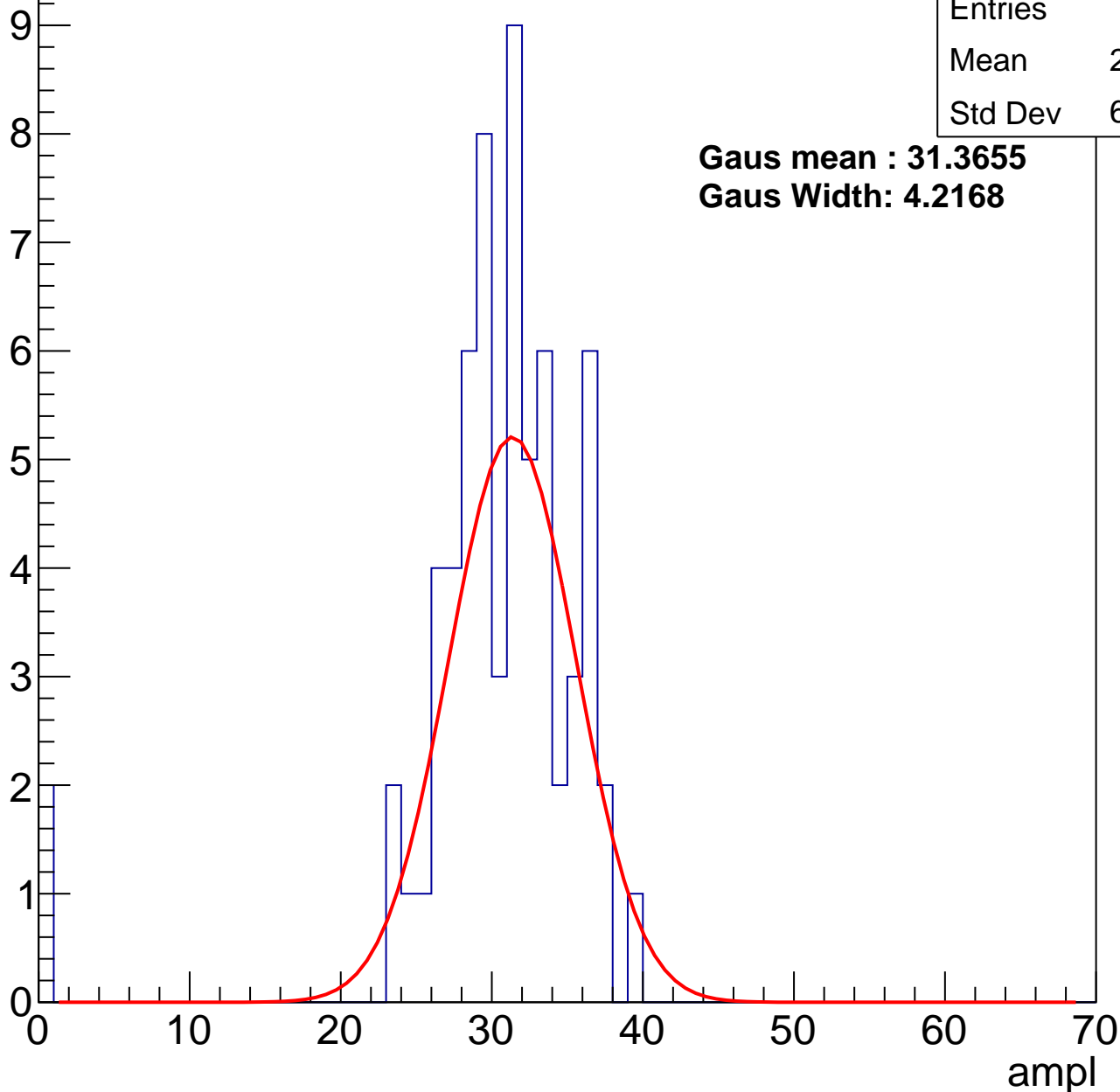
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	29.78
Std Dev	6.413

**Gaus mean : 31.3655**

**Gaus Width: 4.2168**



# B0L001S, U6-ch51, adc1

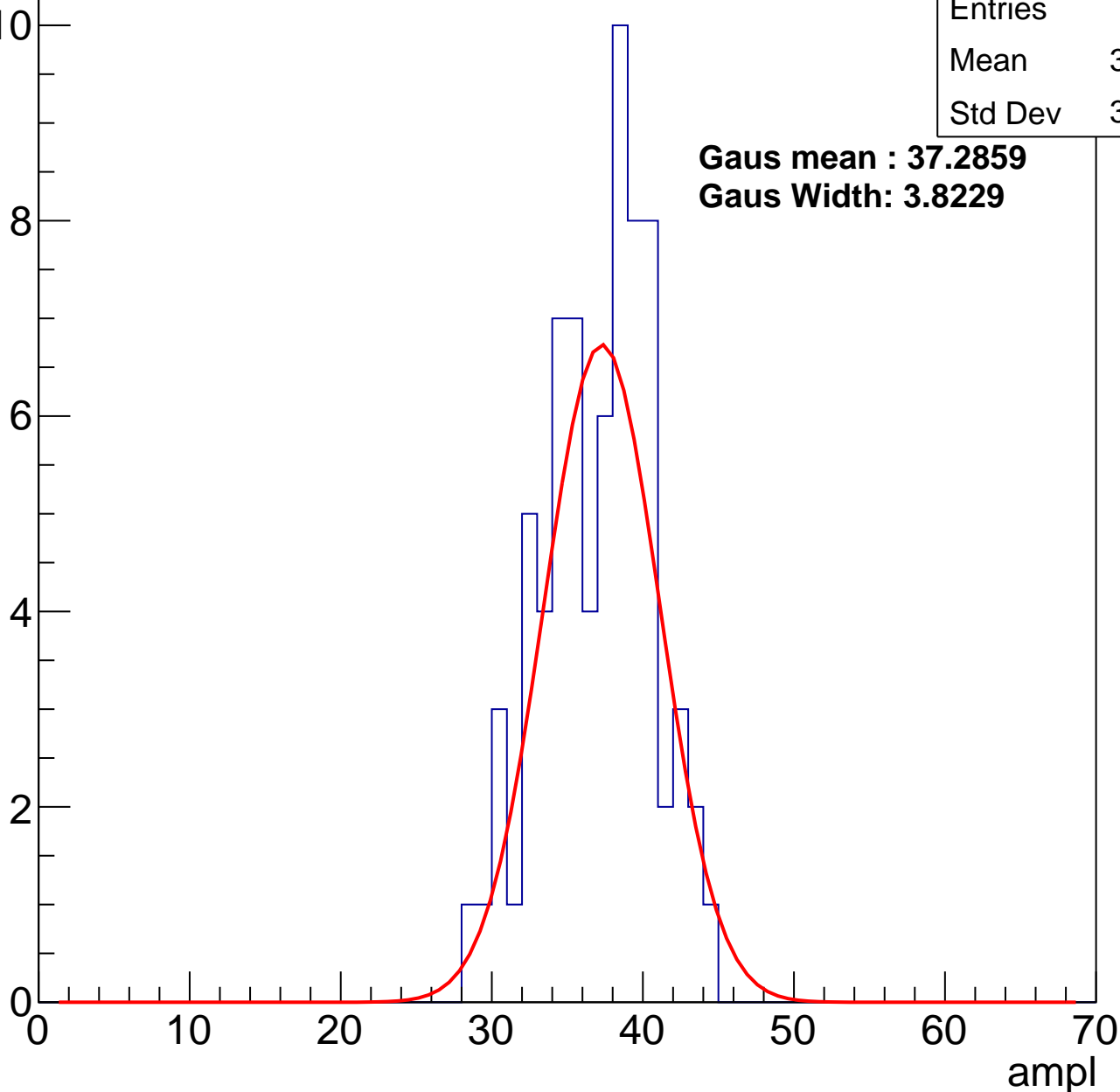
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	36.56
Std Dev	3.588

**Gaus mean : 37.2859**

**Gaus Width: 3.8229**



# B0L001S, U6-ch51, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	44.58
Std Dev	3.166

**Gaus mean : 45.0639**

**Gaus Width: 3.0467**

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

0

2

4

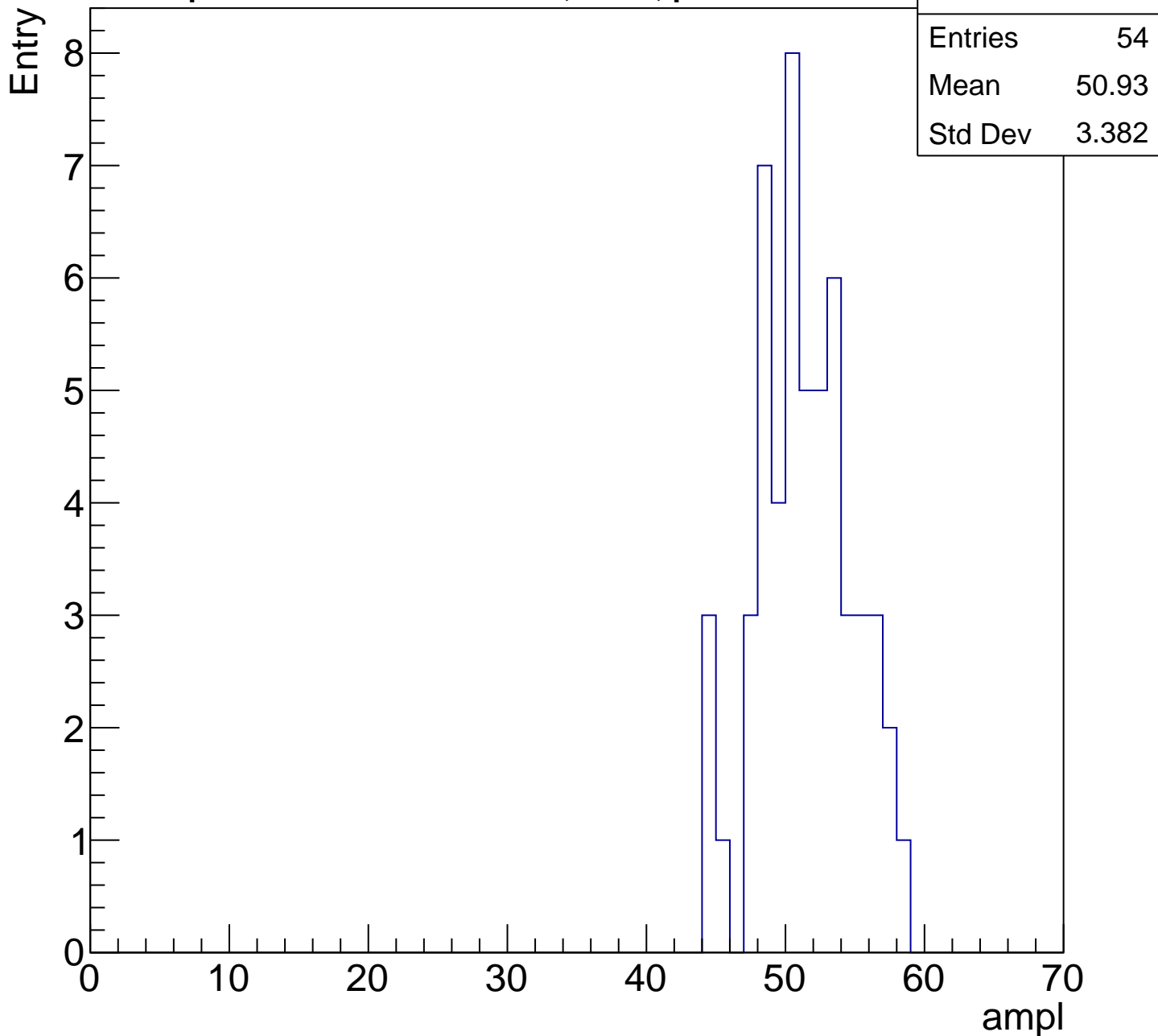
6

8

10

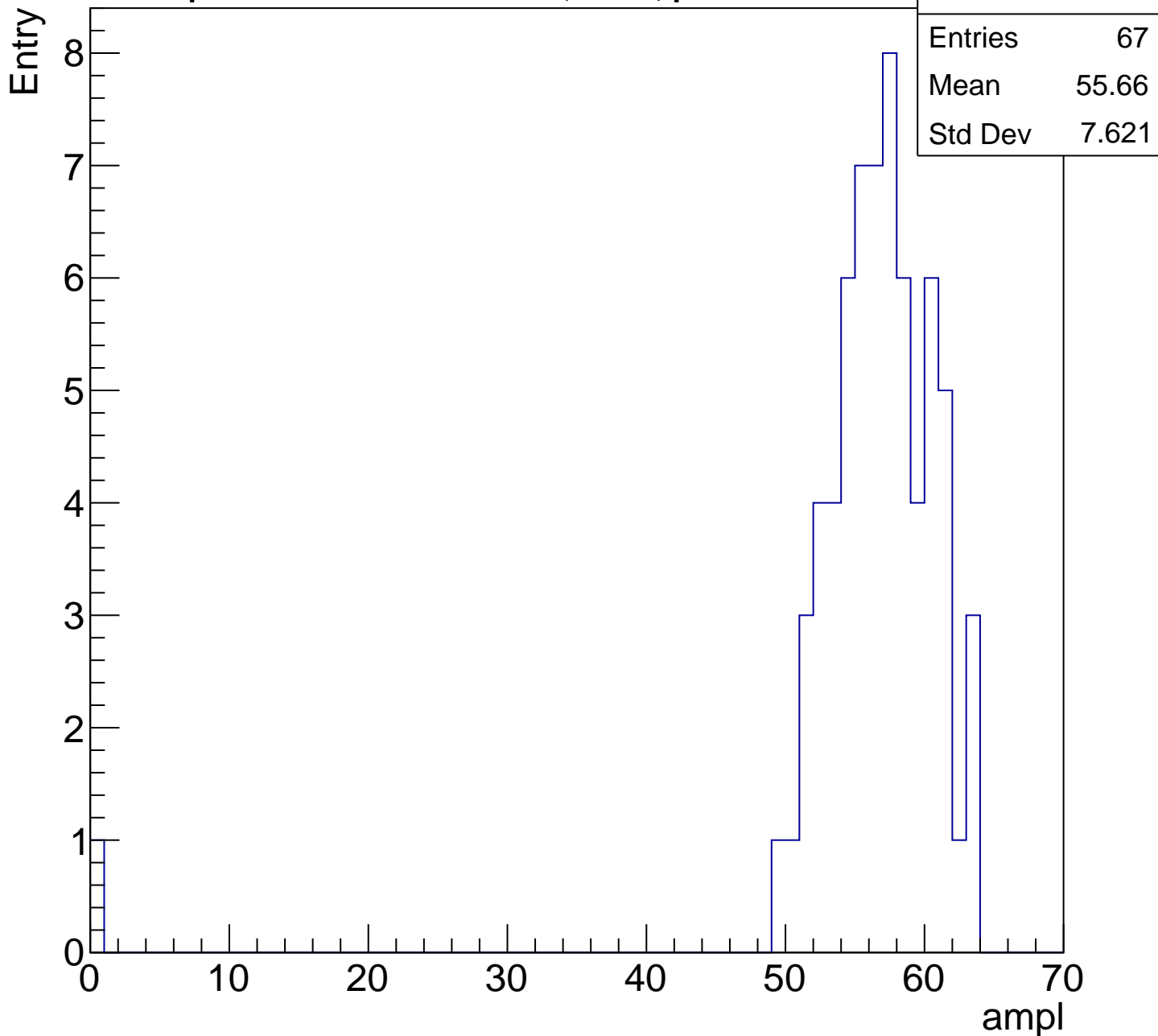
# B0L001S, U6-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U6-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

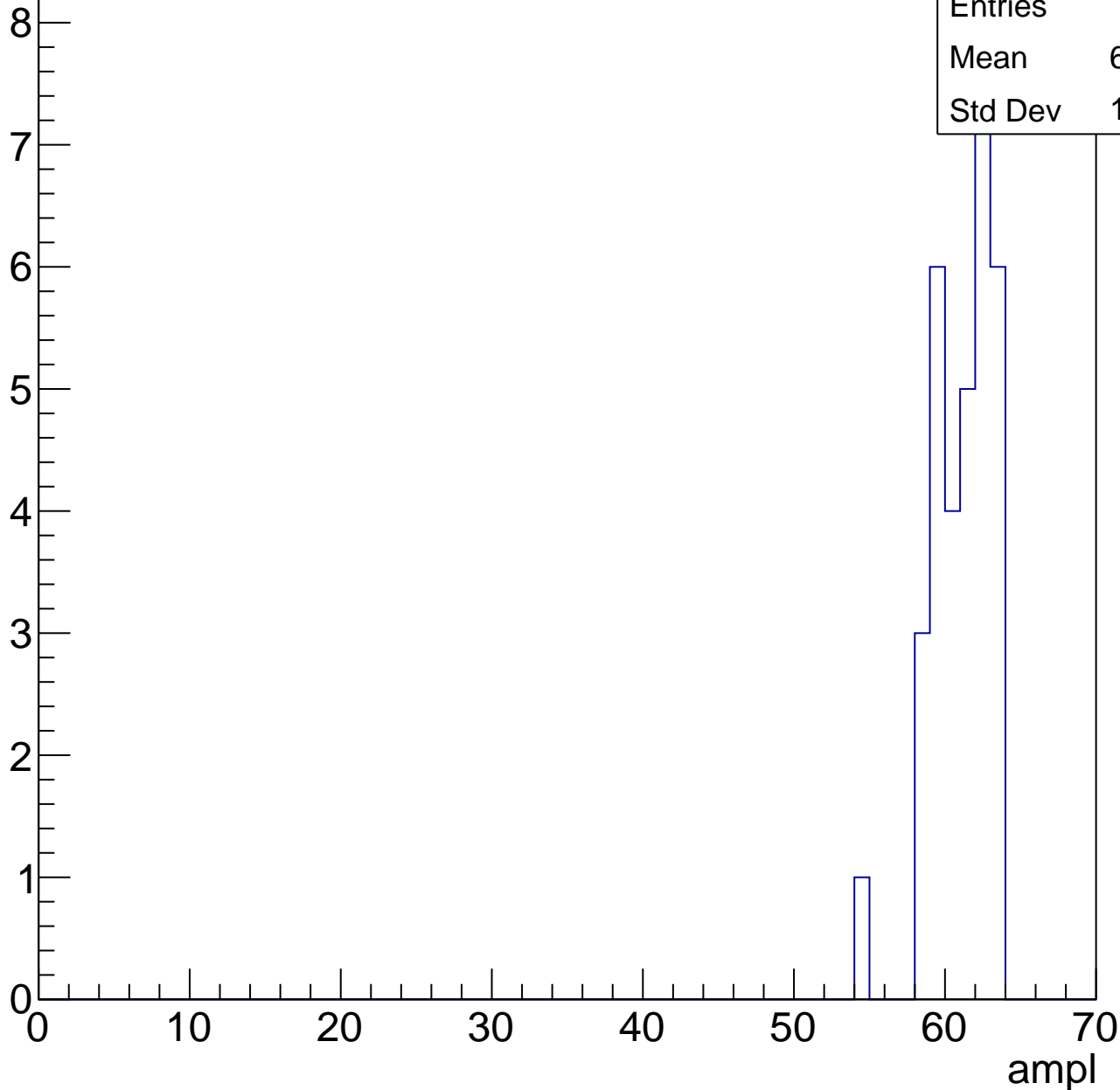


# B0L001S, U6-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	33
Mean	60.64
Std Dev	1.997



# B0L001S, U6-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U6-ch52, adc0

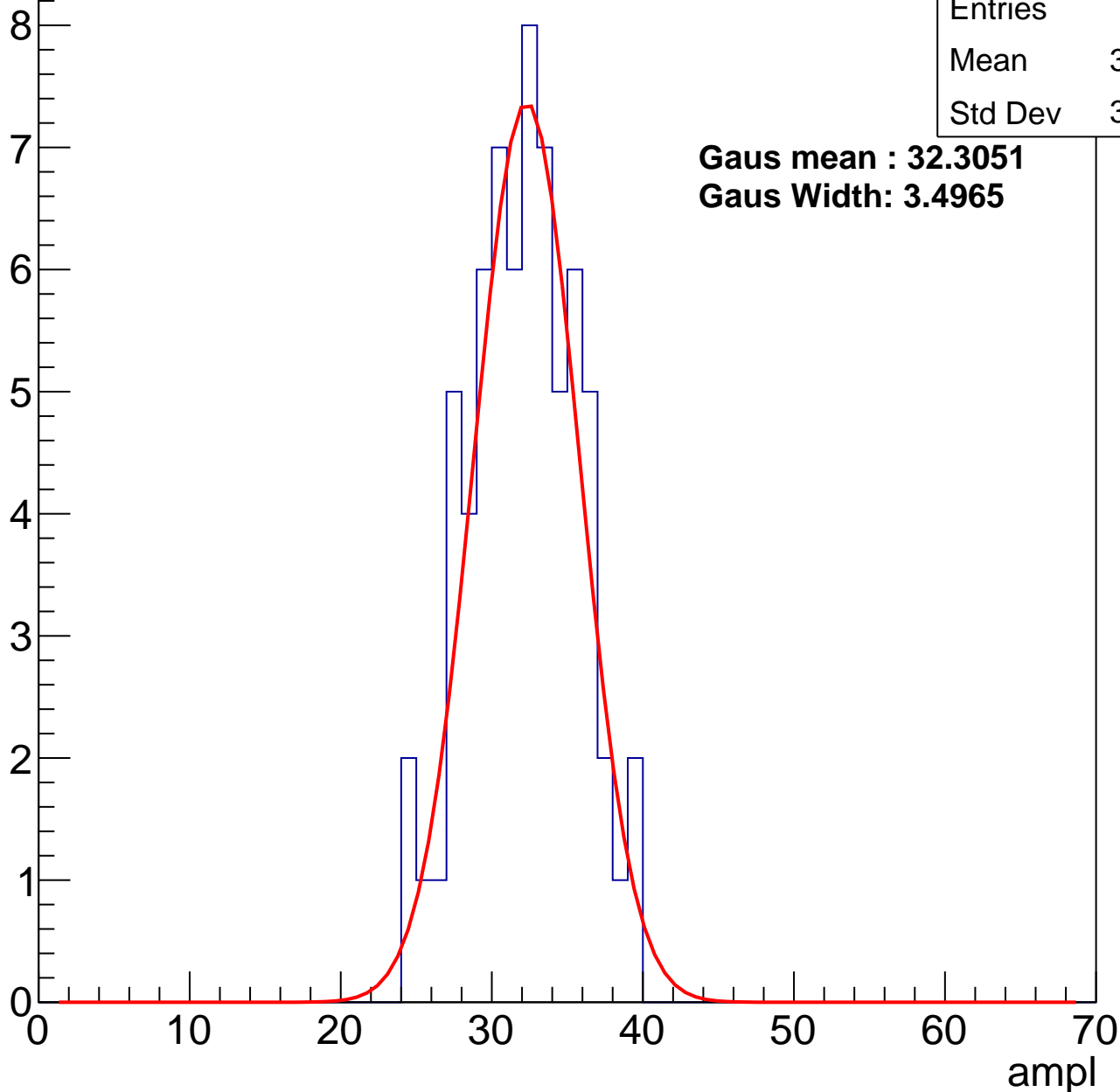
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	31.66
Std Dev	3.488

**Gaus mean : 32.3051**

**Gaus Width: 3.4965**



# B0L001S, U6-ch52, adc1

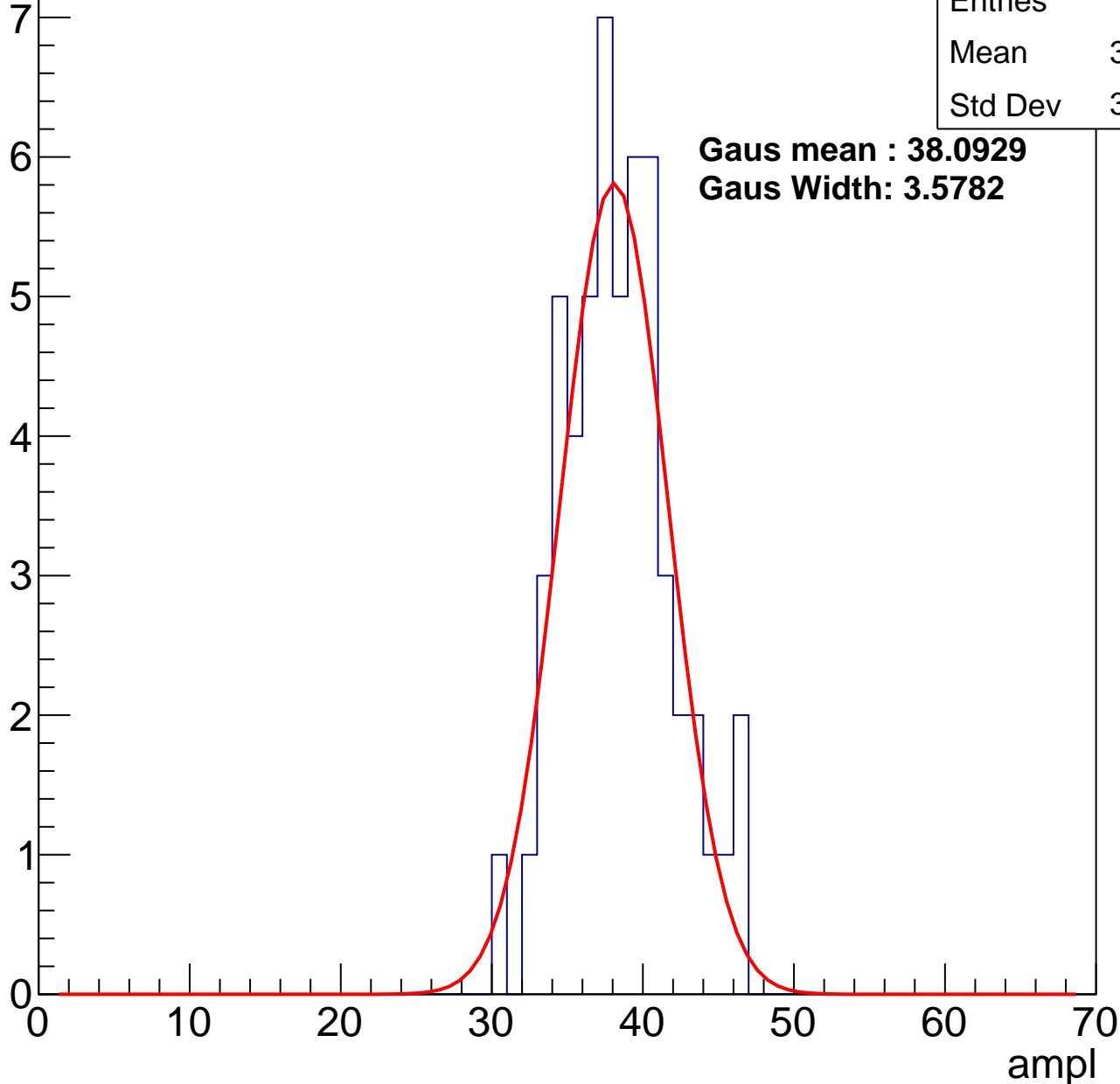
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	37.93
Std Dev	3.522

**Gaus mean : 38.0929**

**Gaus Width: 3.5782**



# B0L001S, U6-ch52, adc2

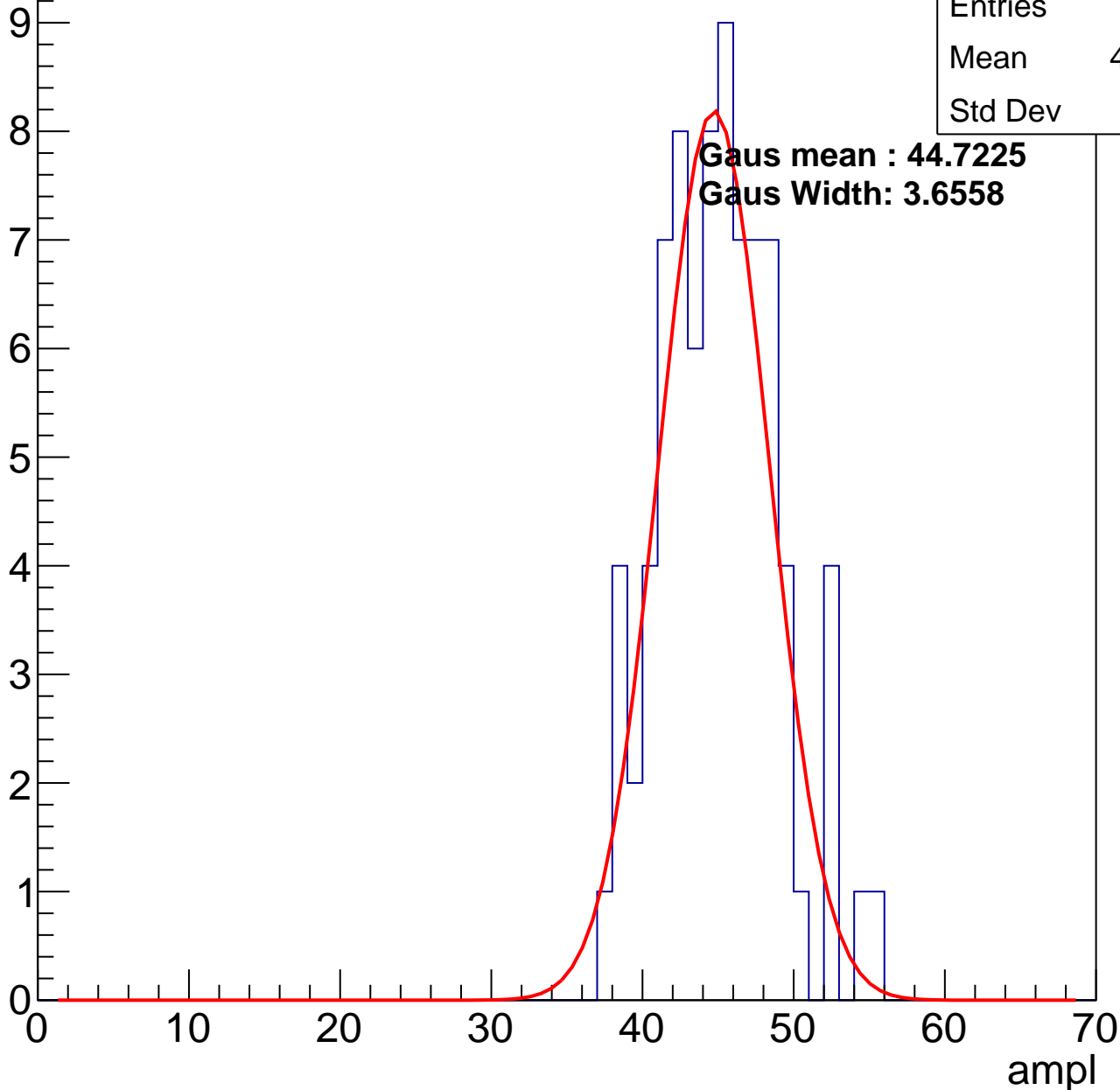
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	44.63
Std Dev	3.85

**Gaus mean : 44.7225**

**Gaus Width: 3.6558**

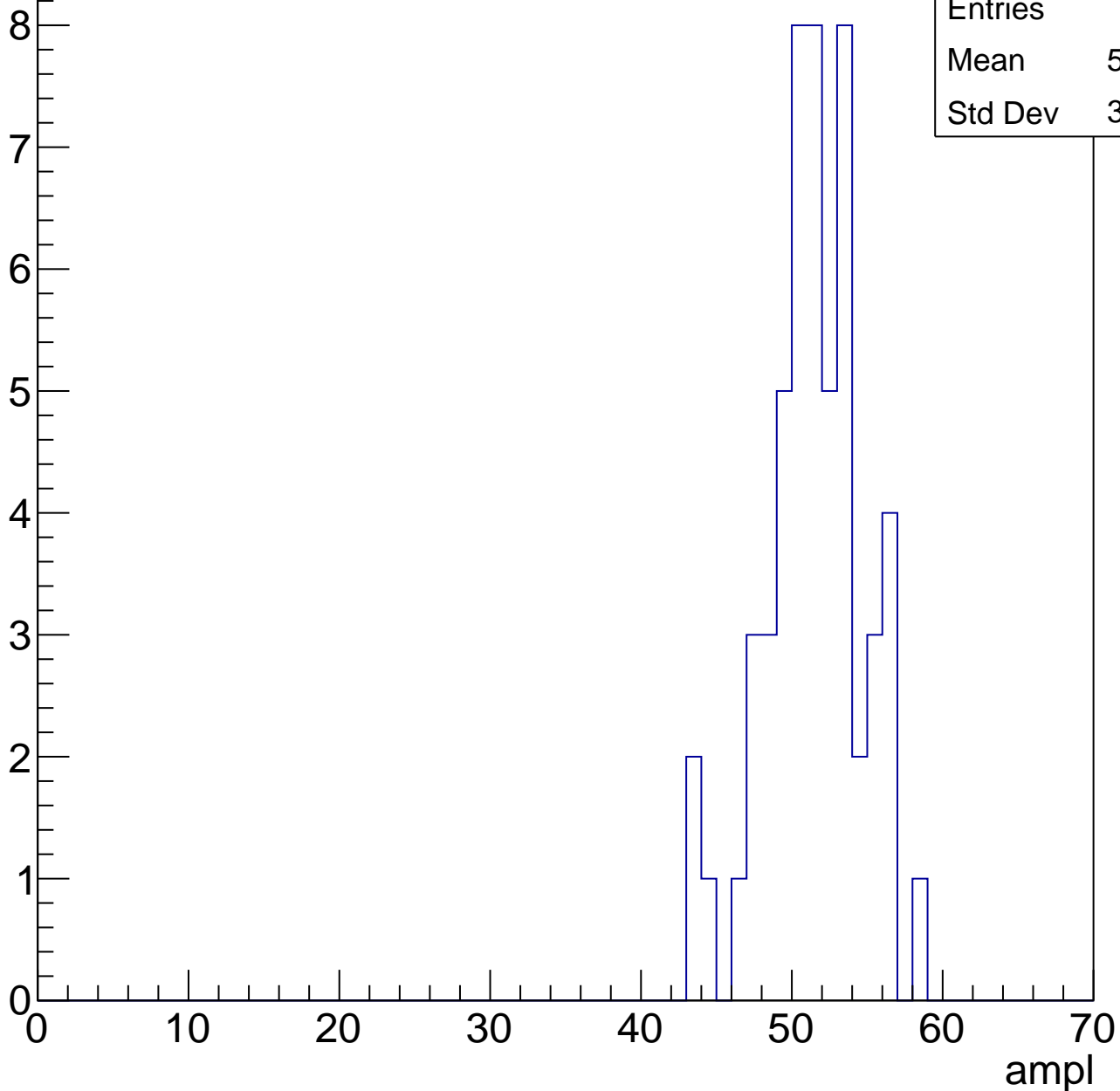


# B0L001S, U6-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	50.98
Std Dev	3.212



# B0L001S, U6-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	75
Mean	57.65
Std Dev	3.272

Entry

10

8

6

4

2

0

0

10

20

30

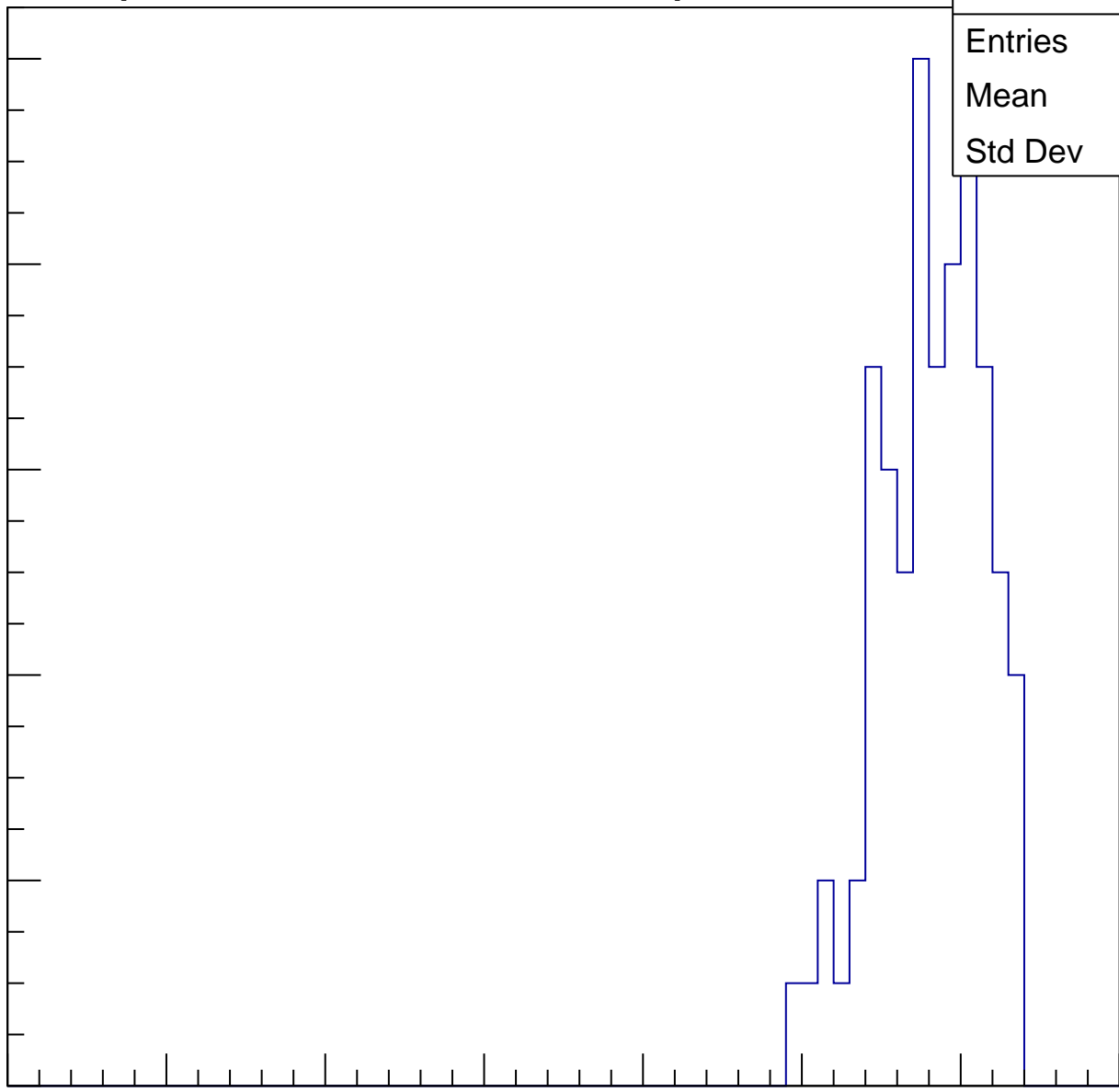
40

50

60

70

ampl

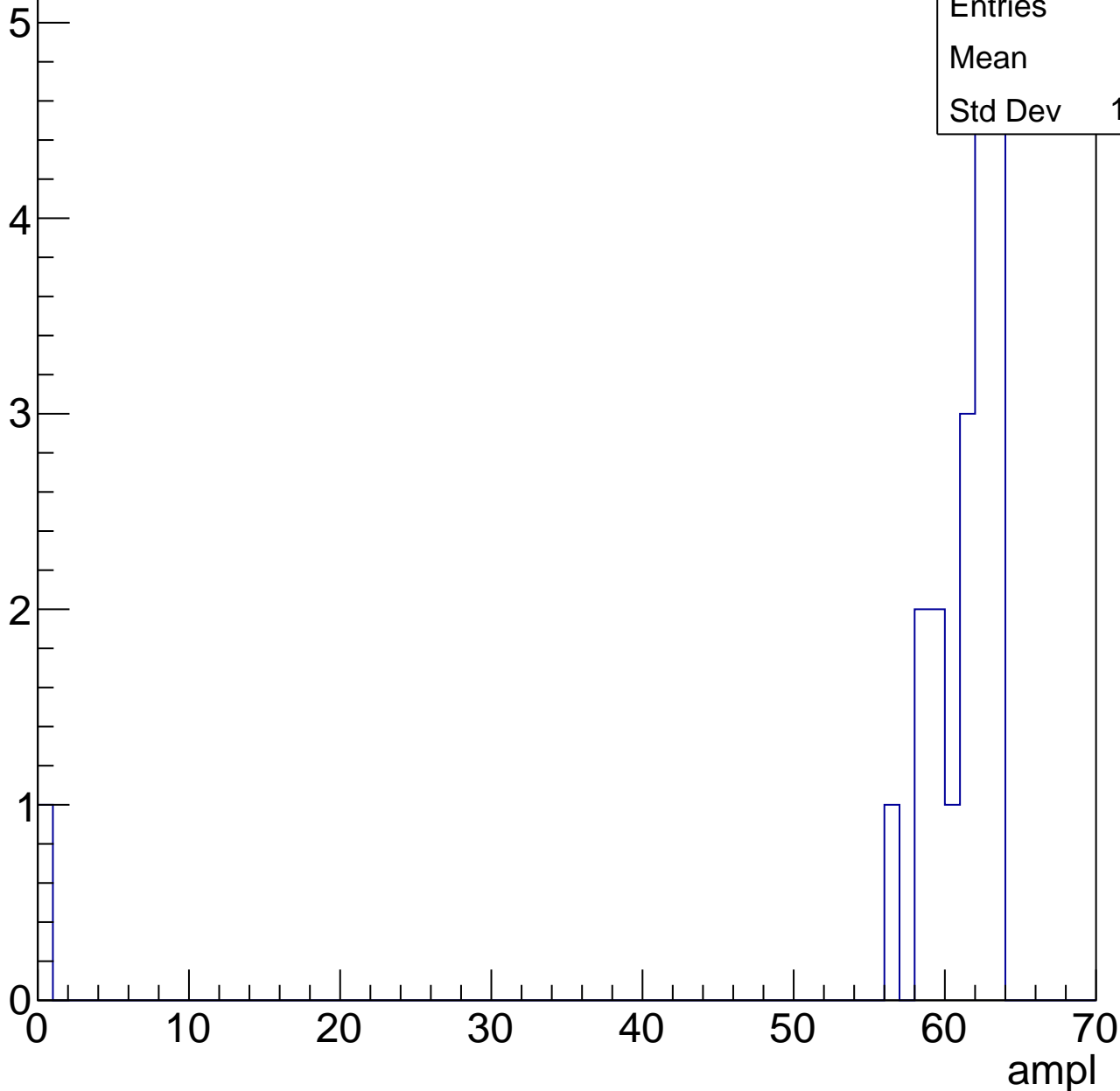


# B0L001S, U6-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	20
Mean	57.9
Std Dev	13.43



# B0L001S, U6-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	63
Std Dev	0

ampl



# B0L001S, U6-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch53, adc0

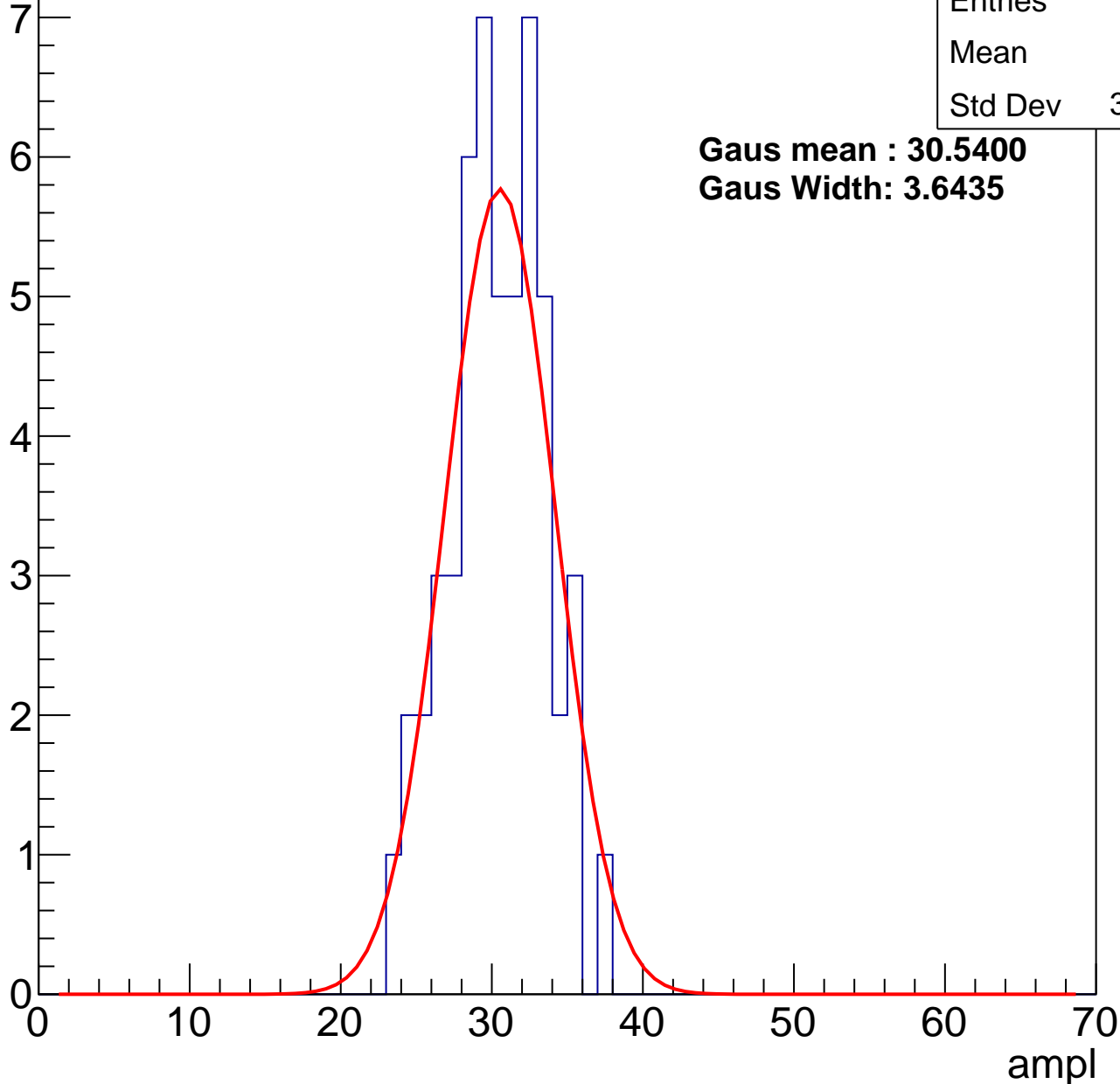
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	29.9
Std Dev	3.133

**Gaus mean : 30.5400**

**Gaus Width: 3.6435**



# B0L001S, U6-ch53, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	36.41
Std Dev	3.517

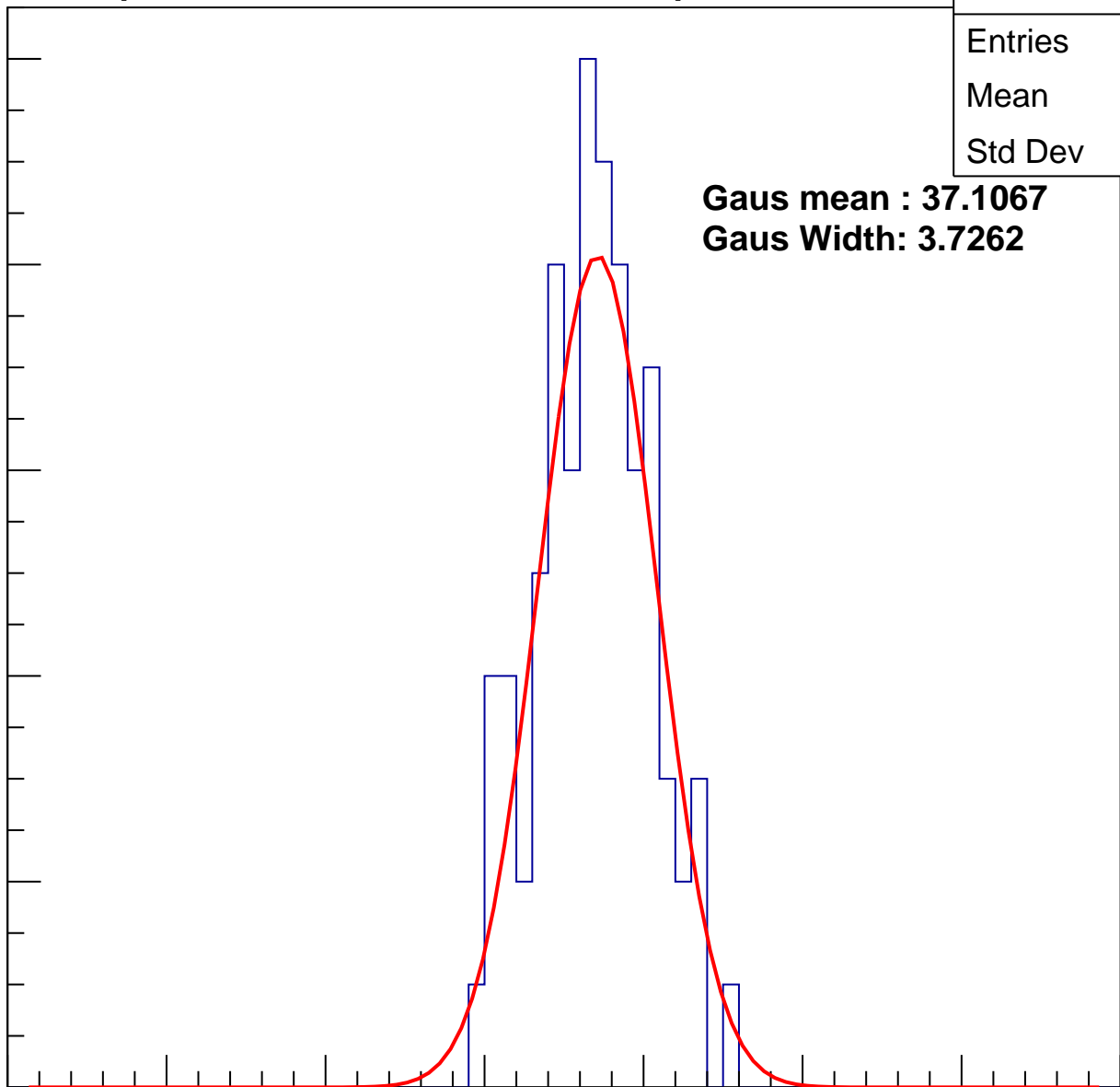
**Gaus mean : 37.1067**

**Gaus Width: 3.7262**

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U6-ch53, adc2

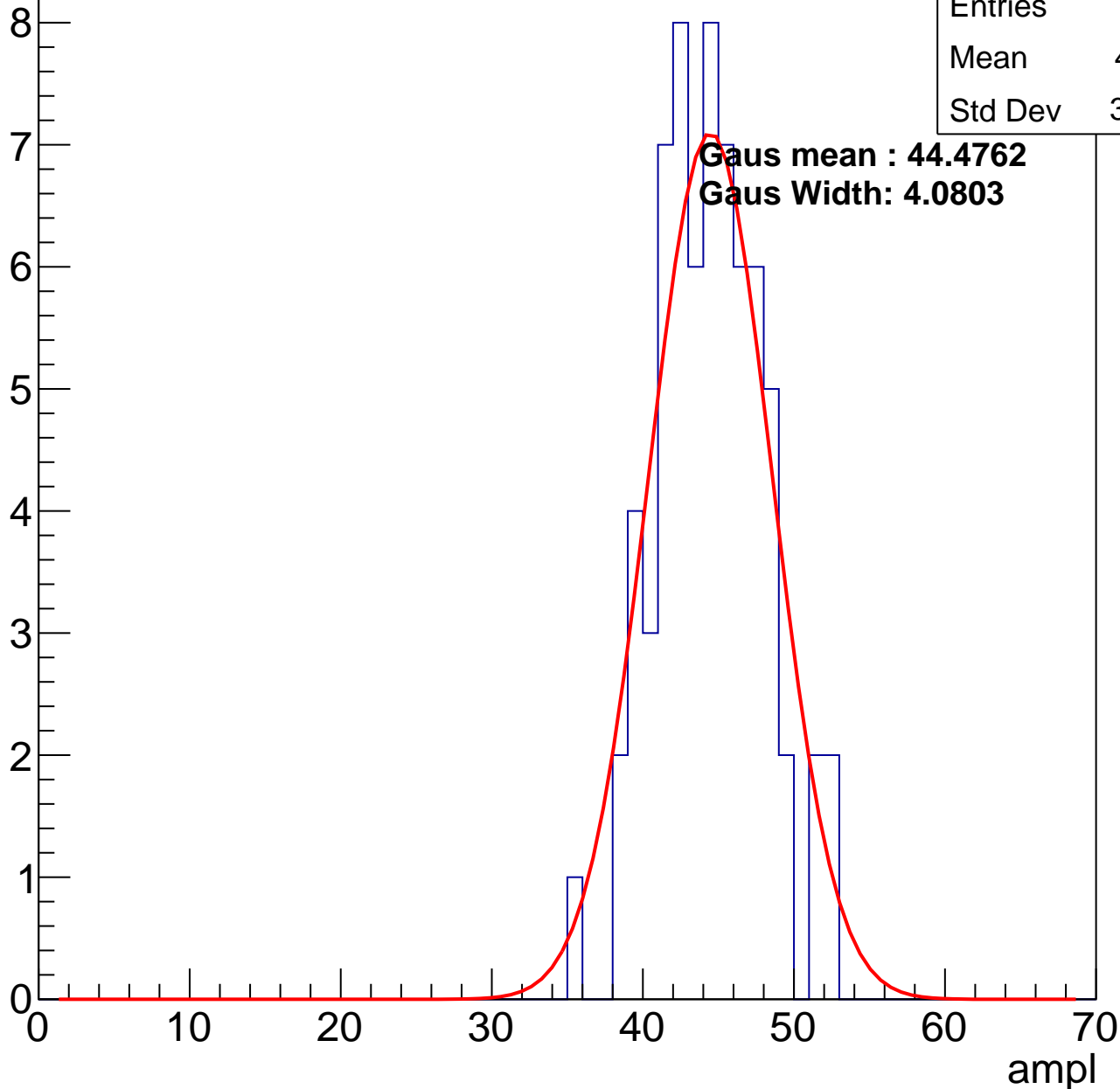
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	44.01
Std Dev	3.495

**Gaus mean : 44.4762**

**Gaus Width: 4.0803**



# B0L001S, U6-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

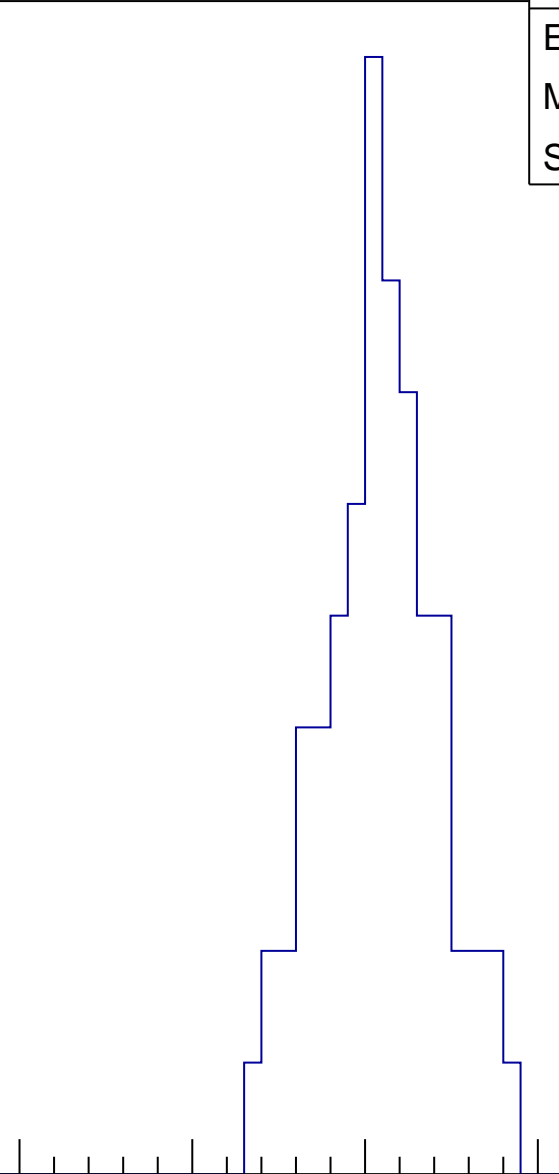
Entries	66
Mean	50.42
Std Dev	3.326

Entry

10  
8  
6  
4  
2  
0

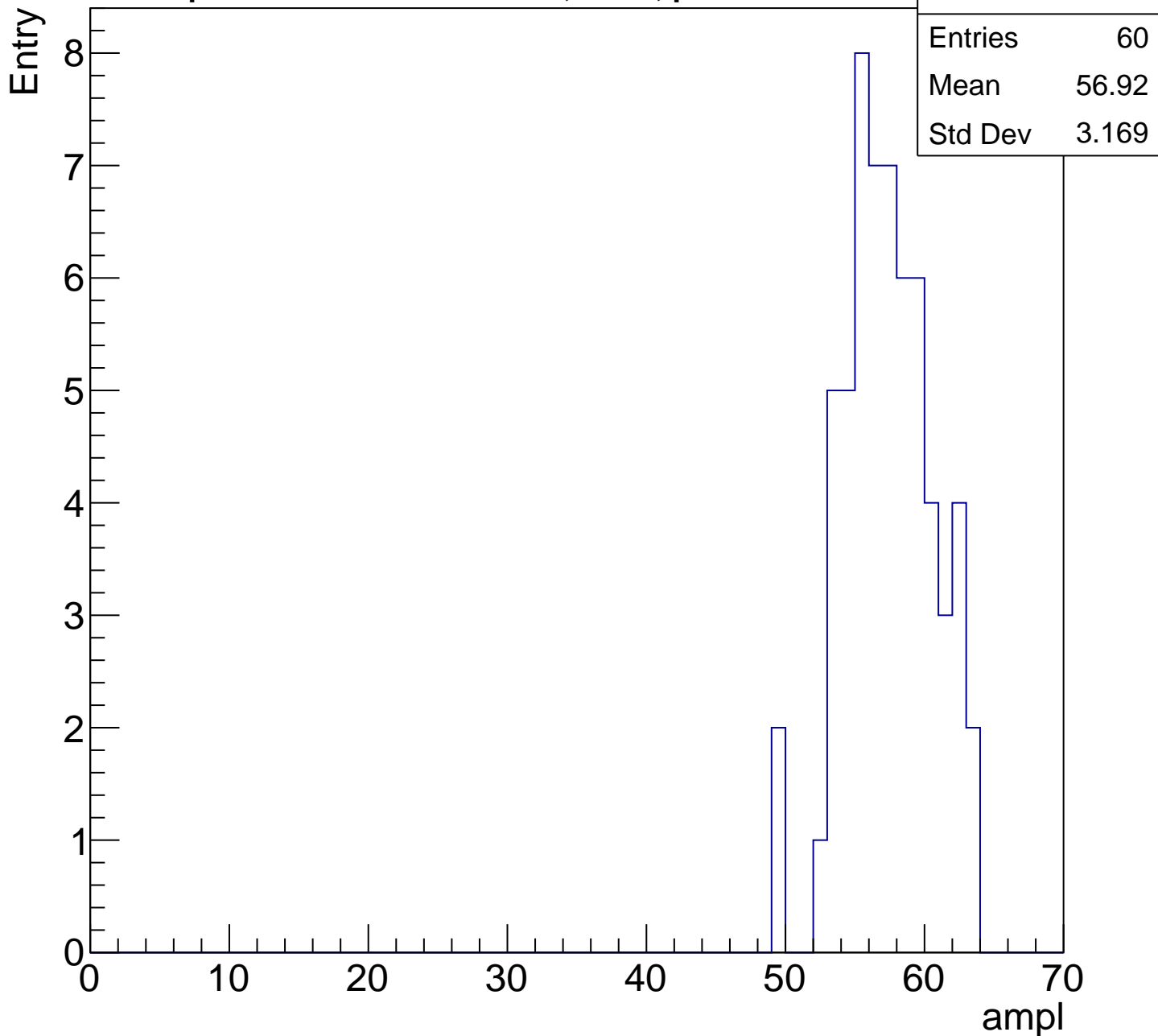
0 10 20 30 40 50 60 70

ampl



# B0L001S, U6-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U6-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

7

6

5

4

3

2

1

0

Entries

34

Mean

60.59

Std Dev

1.833

ampl

0

10

20

30

40

50

60

70

# B0L001S, U6-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch54, adc0

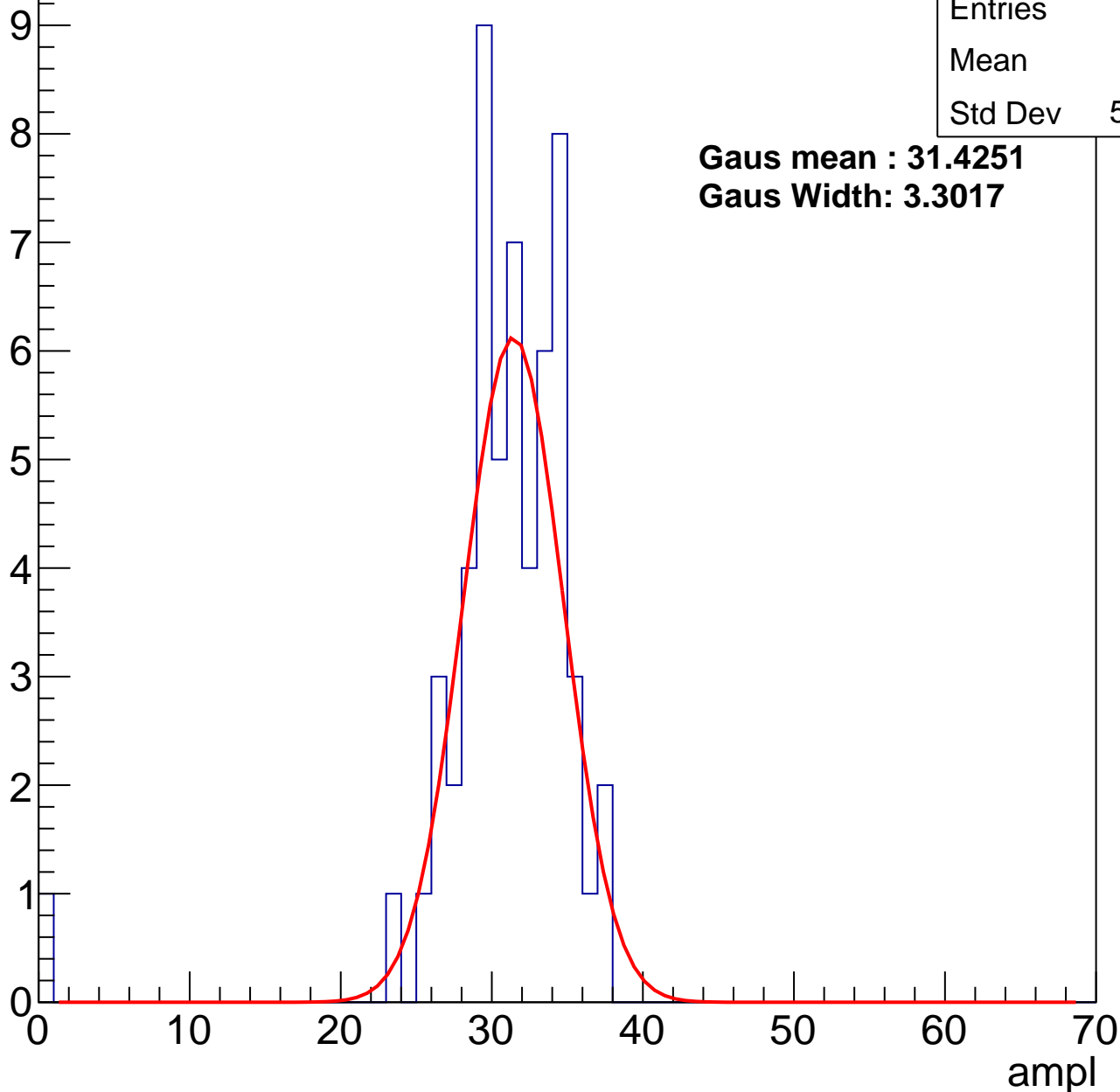
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	30.4
Std Dev	5.078

**Gaus mean : 31.4251**

**Gaus Width: 3.3017**



# B0L001S, U6-ch54, adc1

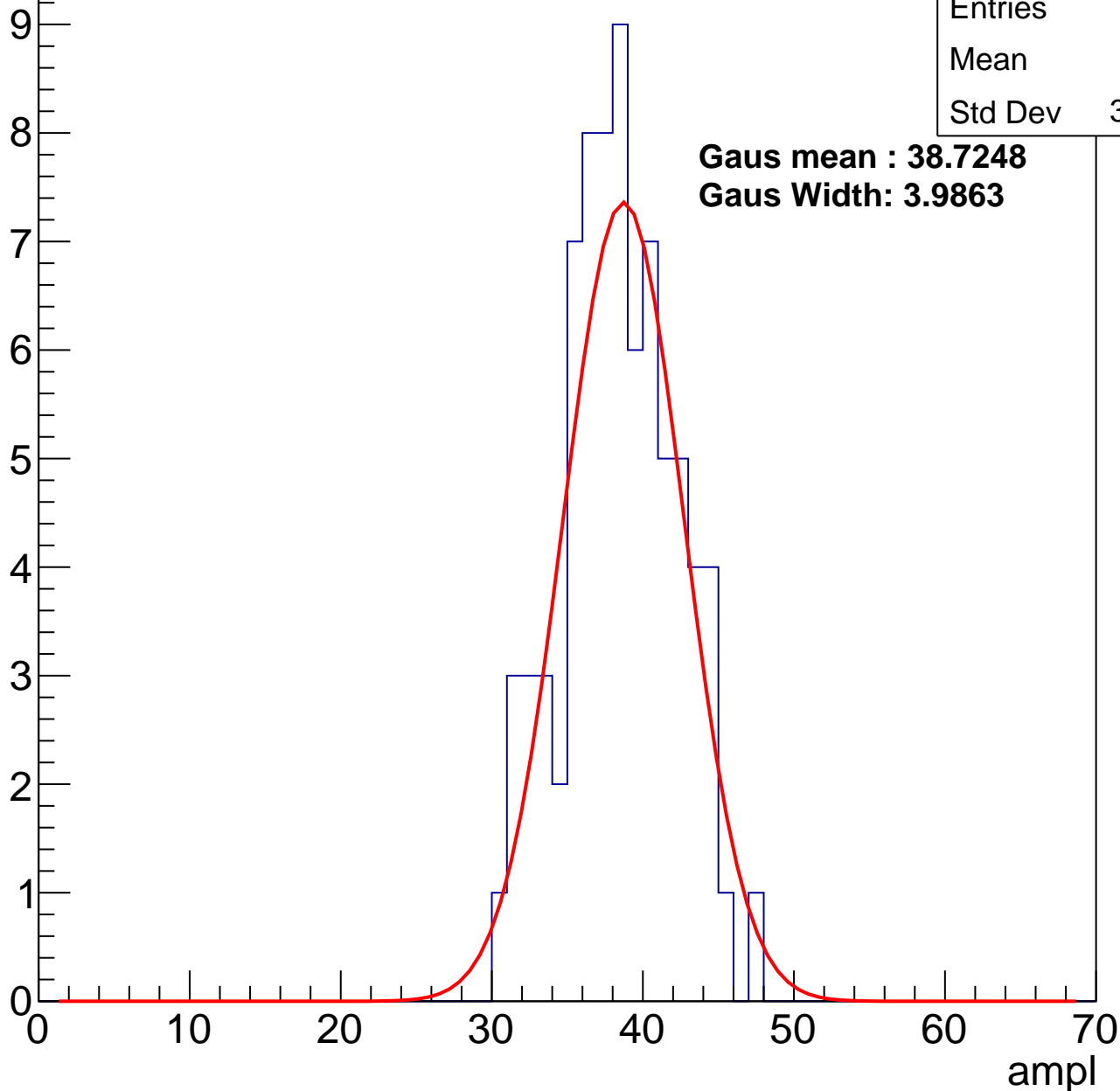
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	38
Std Dev	3.714

**Gaus mean : 38.7248**

**Gaus Width: 3.9863**



# B0L001S, U6-ch54, adc2

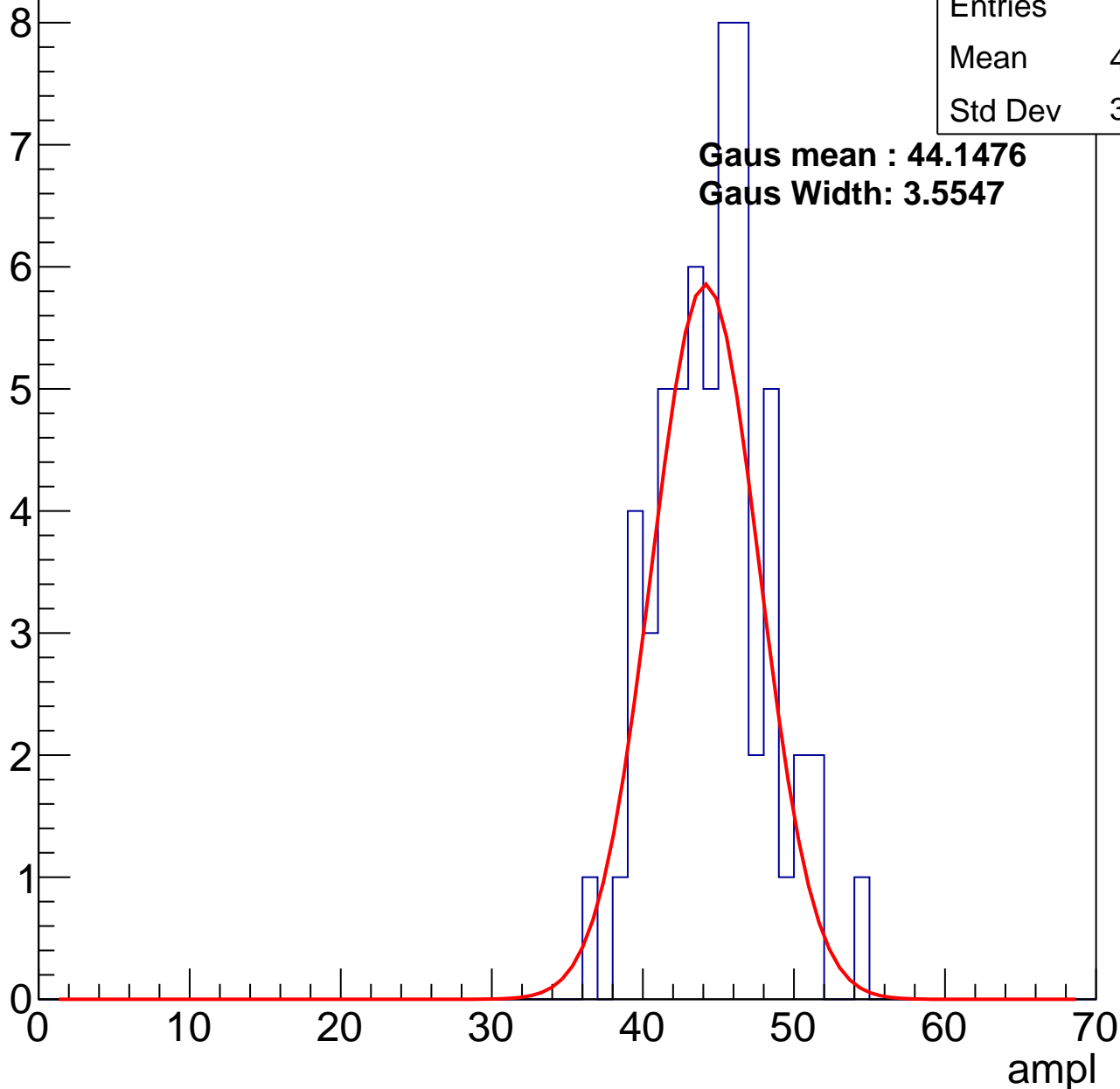
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	44.24
Std Dev	3.562

**Gaus mean : 44.1476**

**Gaus Width: 3.5547**

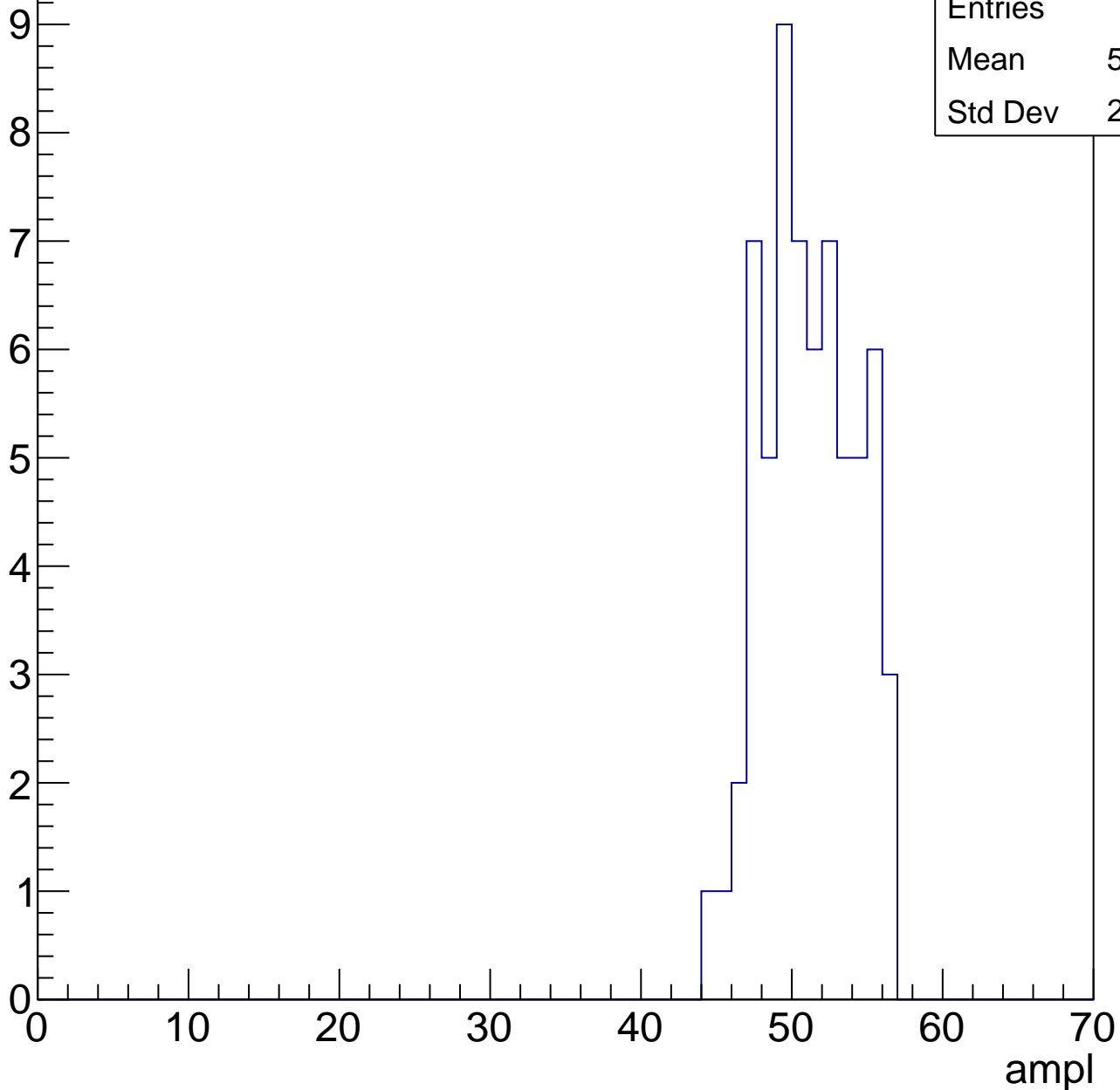


# B0L001S, U6-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	50.69
Std Dev	2.989

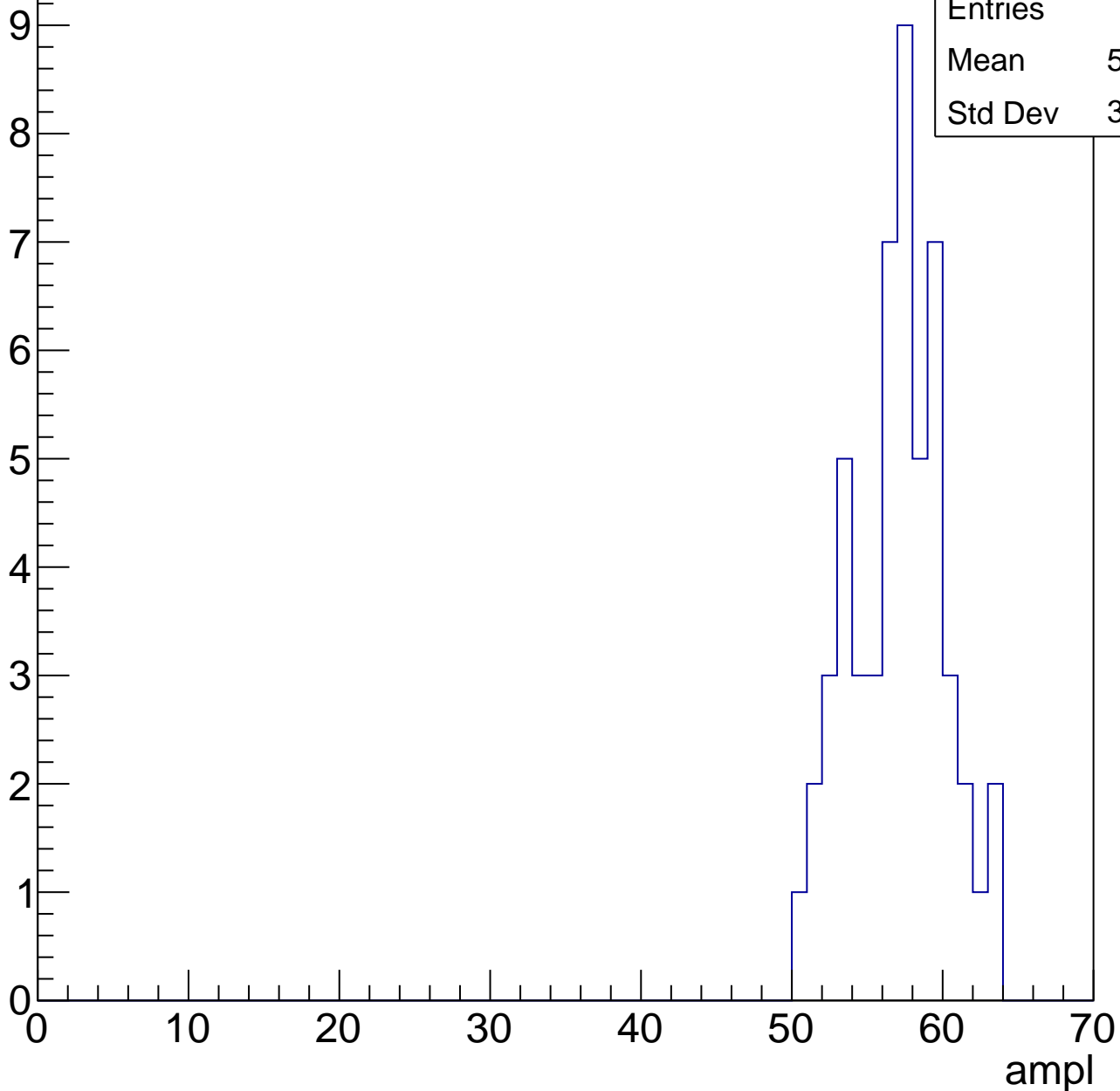


# B0L001S, U6-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	56.57
Std Dev	3.075



# B0L001S, U6-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	39
Mean	60.33
Std Dev	2.14

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

7

8

# B0L001S, U6-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U6-ch55, adc0

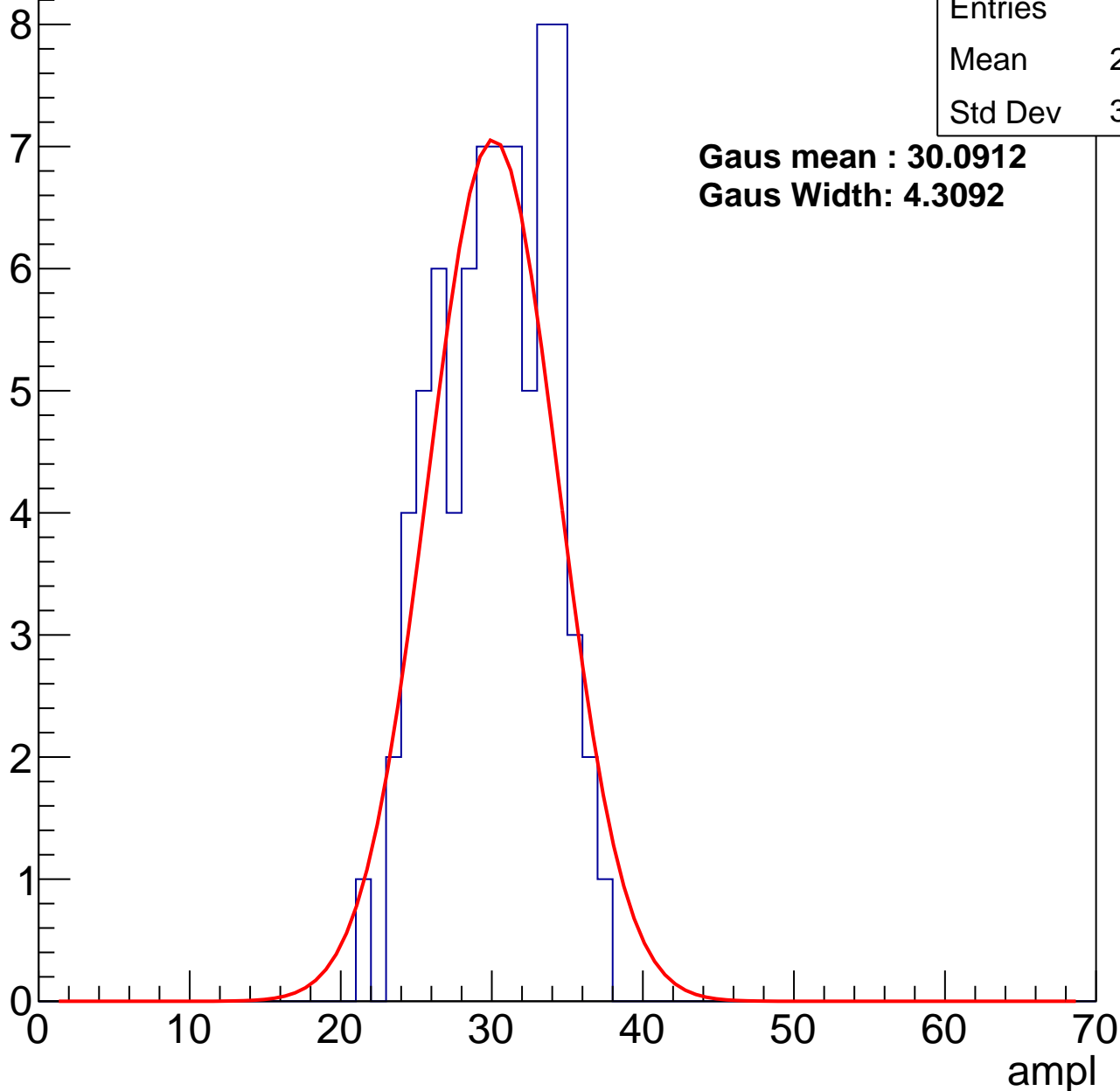
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	29.74
Std Dev	3.679

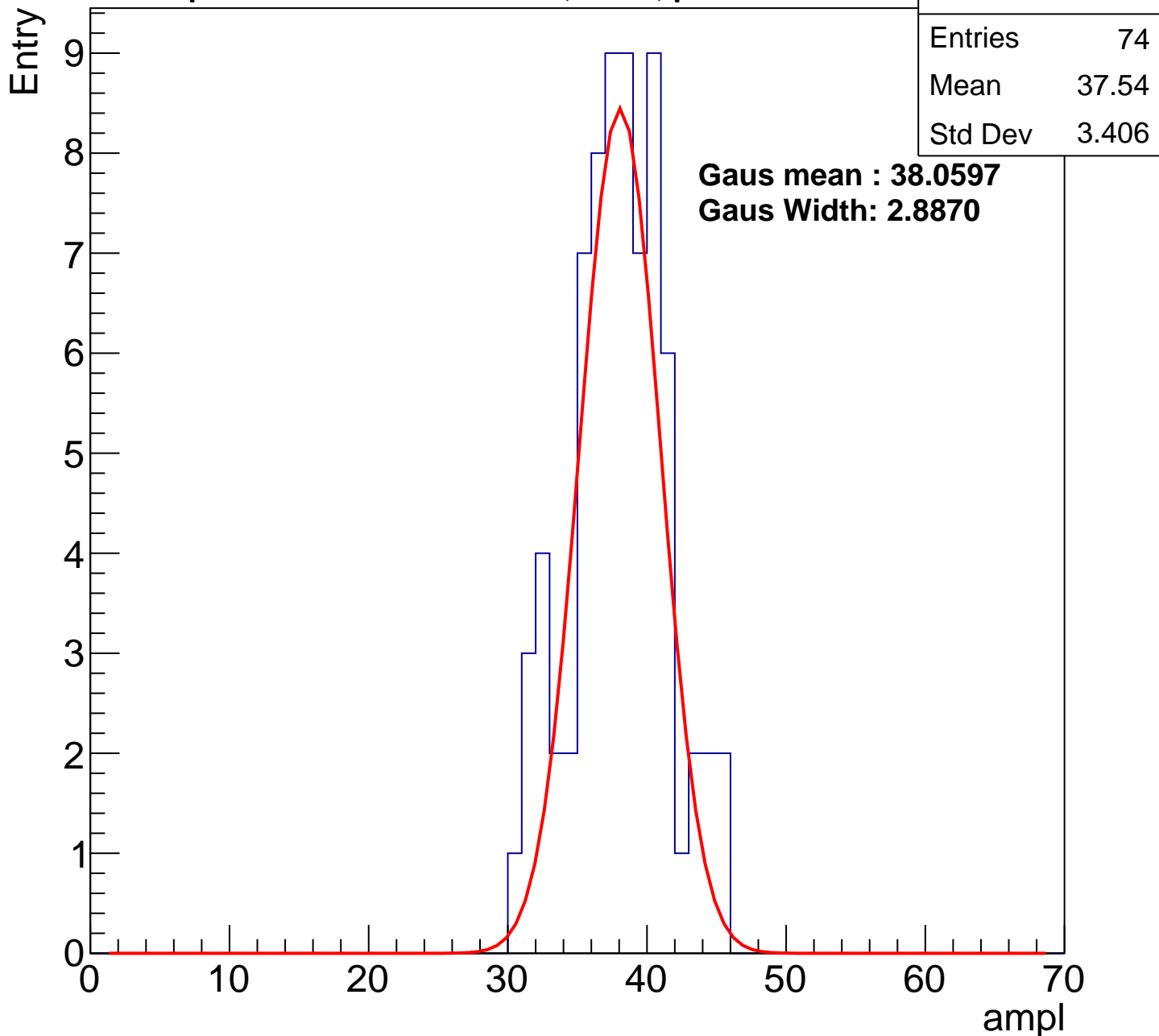
**Gaus mean : 30.0912**

**Gaus Width: 4.3092**



# B0L001S, U6-ch55, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U6-ch55, adc2

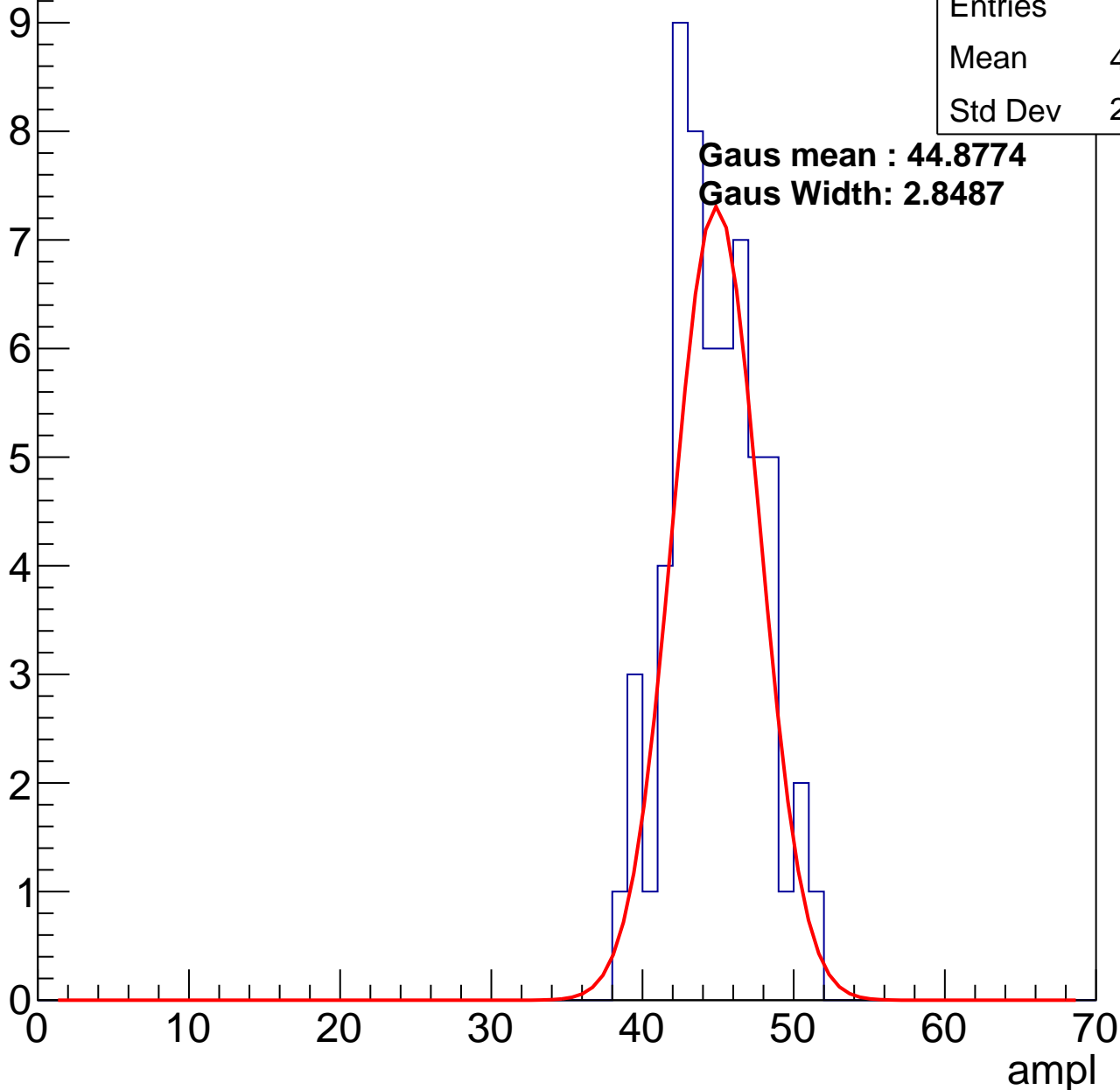
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	44.27
Std Dev	2.933

**Gaus mean : 44.8774**

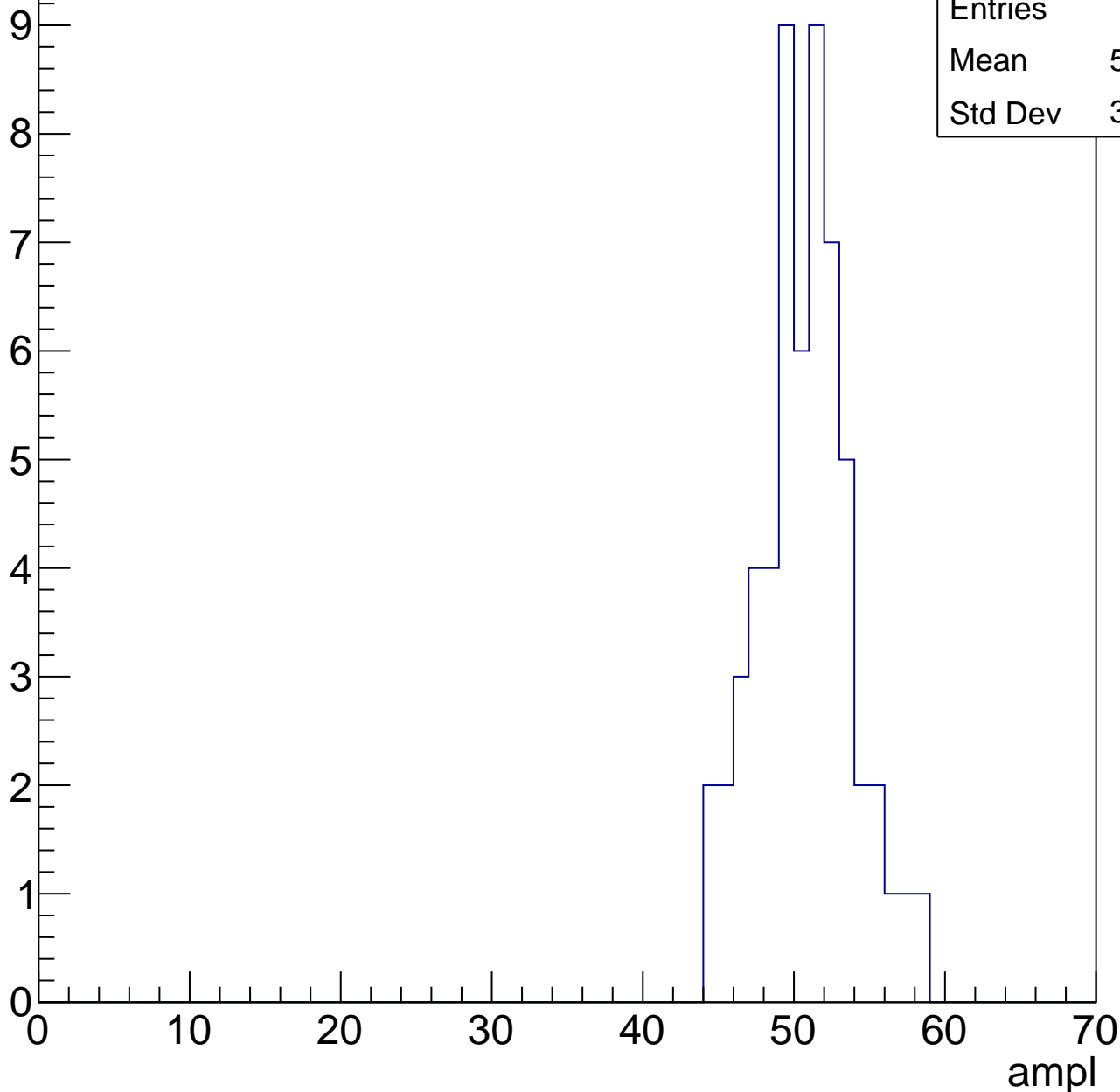
**Gaus Width: 2.8487**



# B0L001S, U6-ch55, adc3

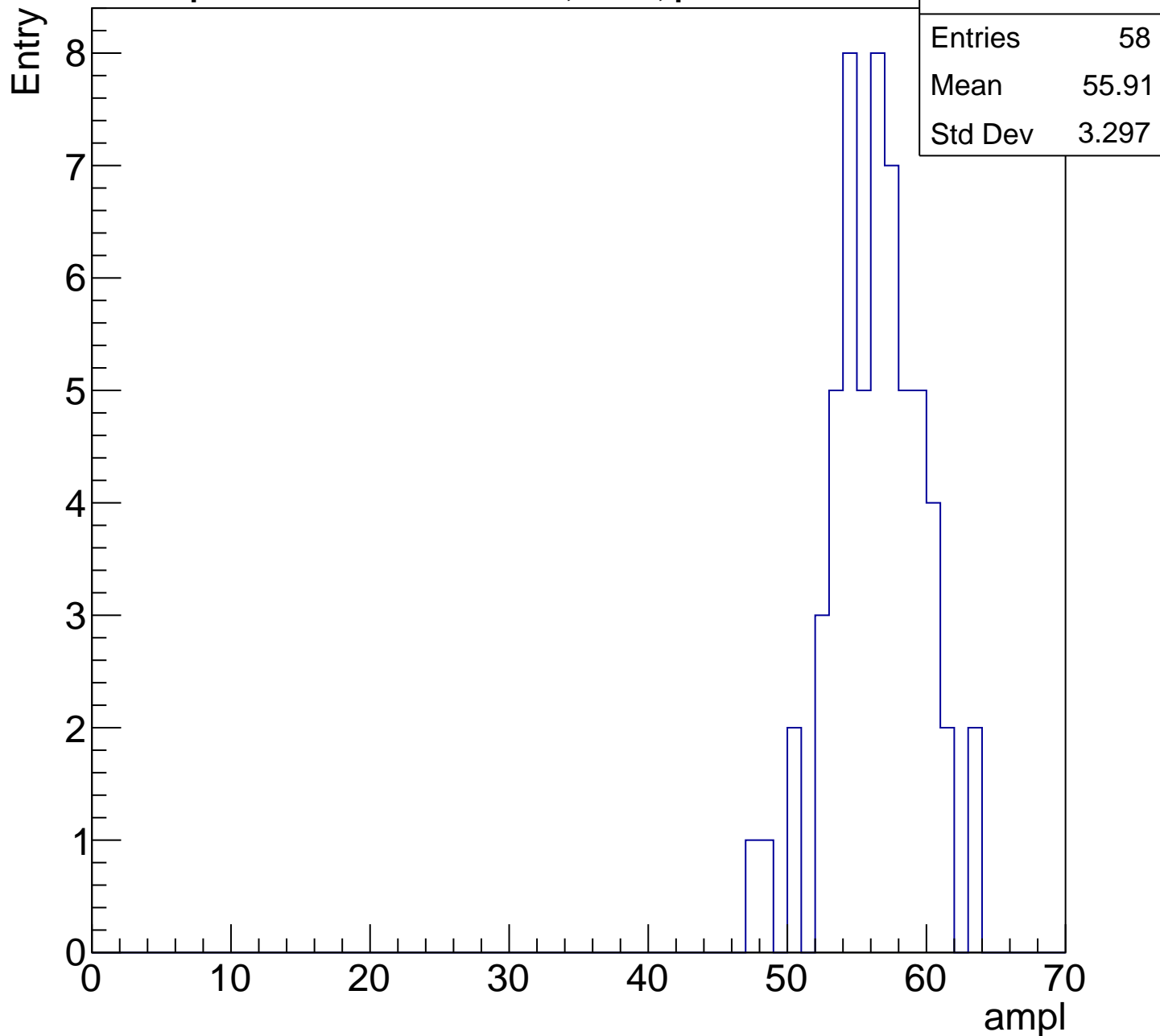
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

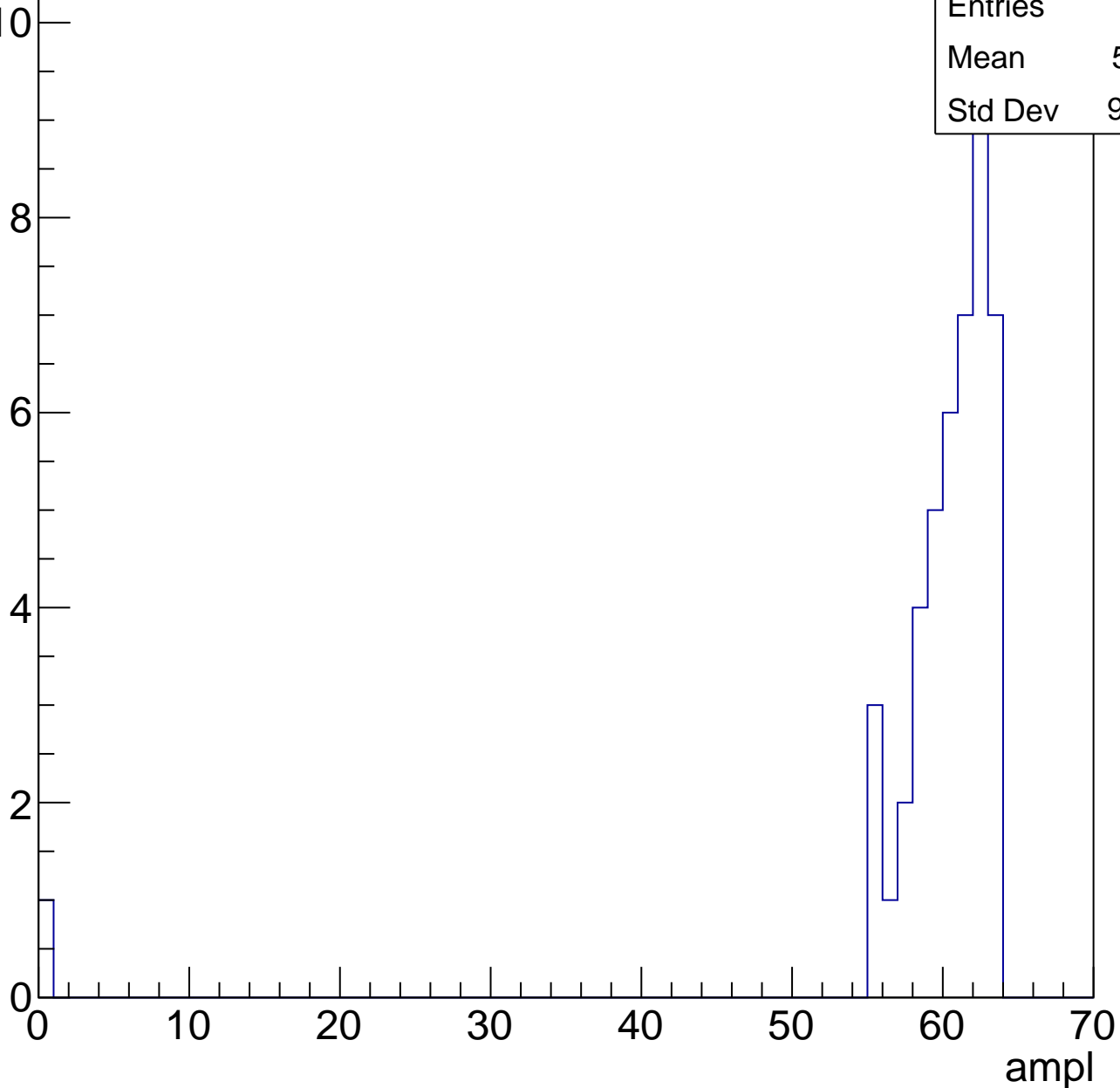


# B0L001S, U6-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	58.91
Std Dev	9.072



# B0L001S, U6-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch56, adc0

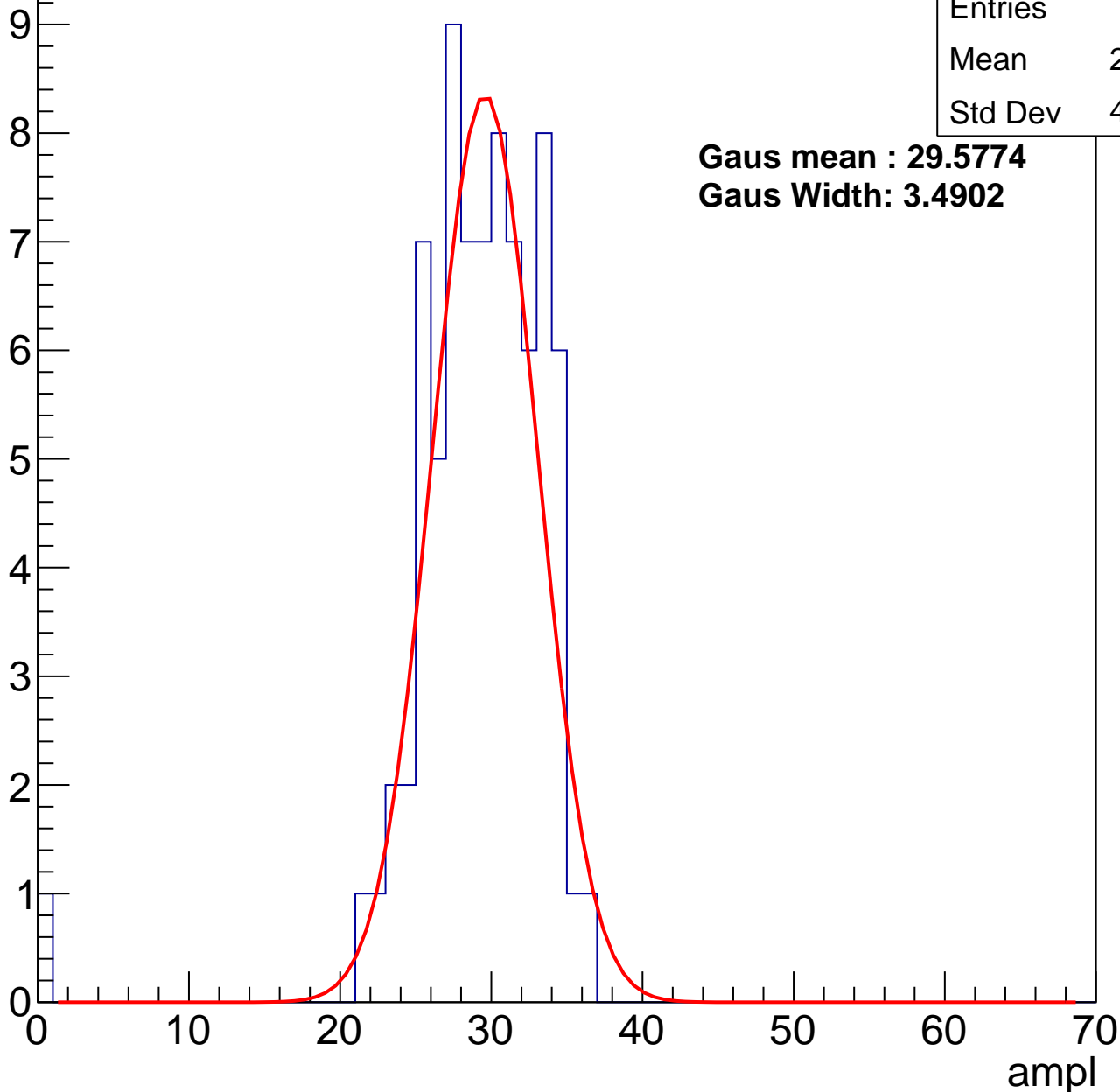
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	28.76
Std Dev	4.672

**Gaus mean : 29.5774**

**Gaus Width: 3.4902**



# B0L001S, U6-ch56, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	62
Mean	35.79
Std Dev	3.214

**Gaus mean : 36.7372**

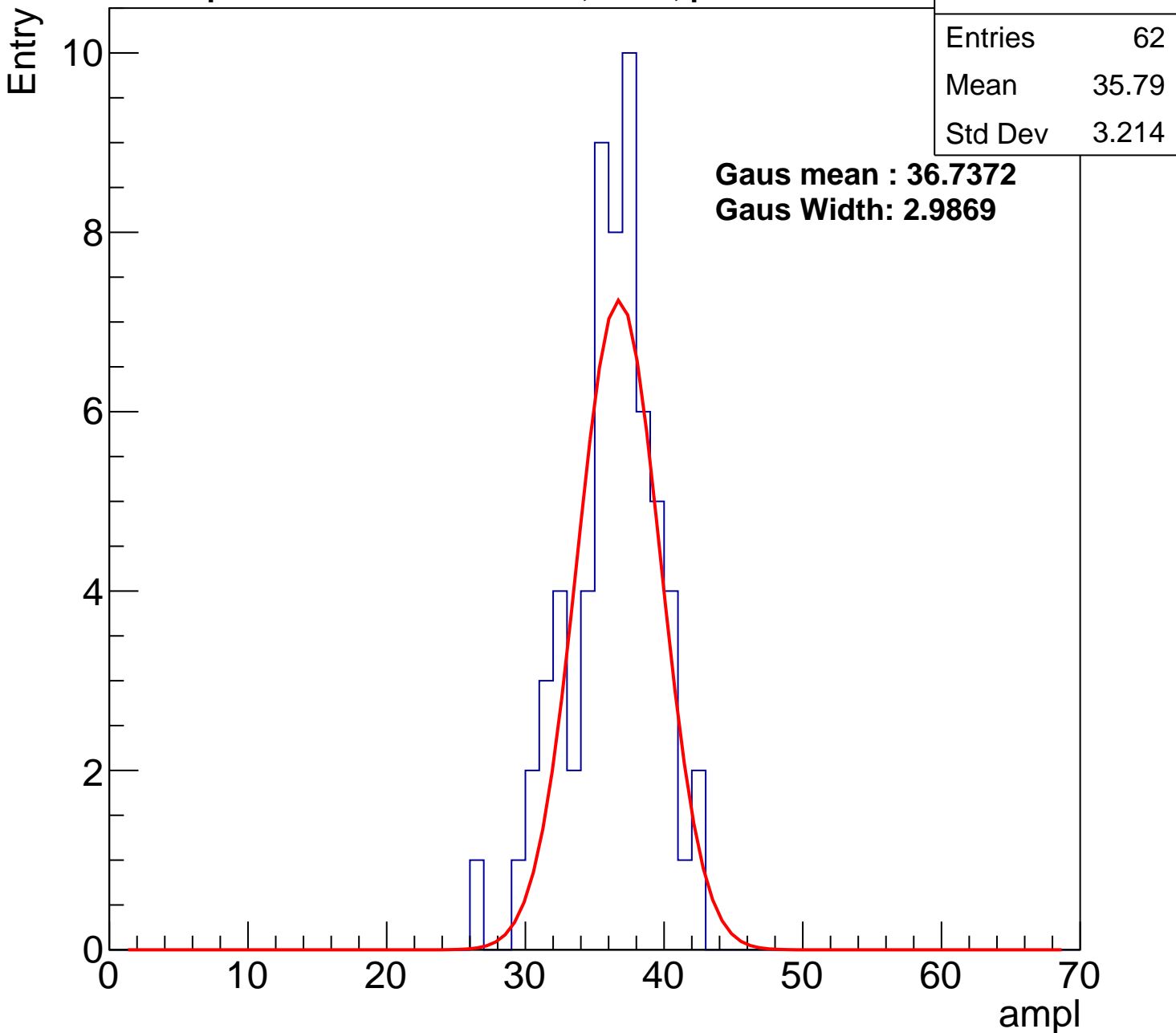
**Gaus Width: 2.9869**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U6-ch56, adc2

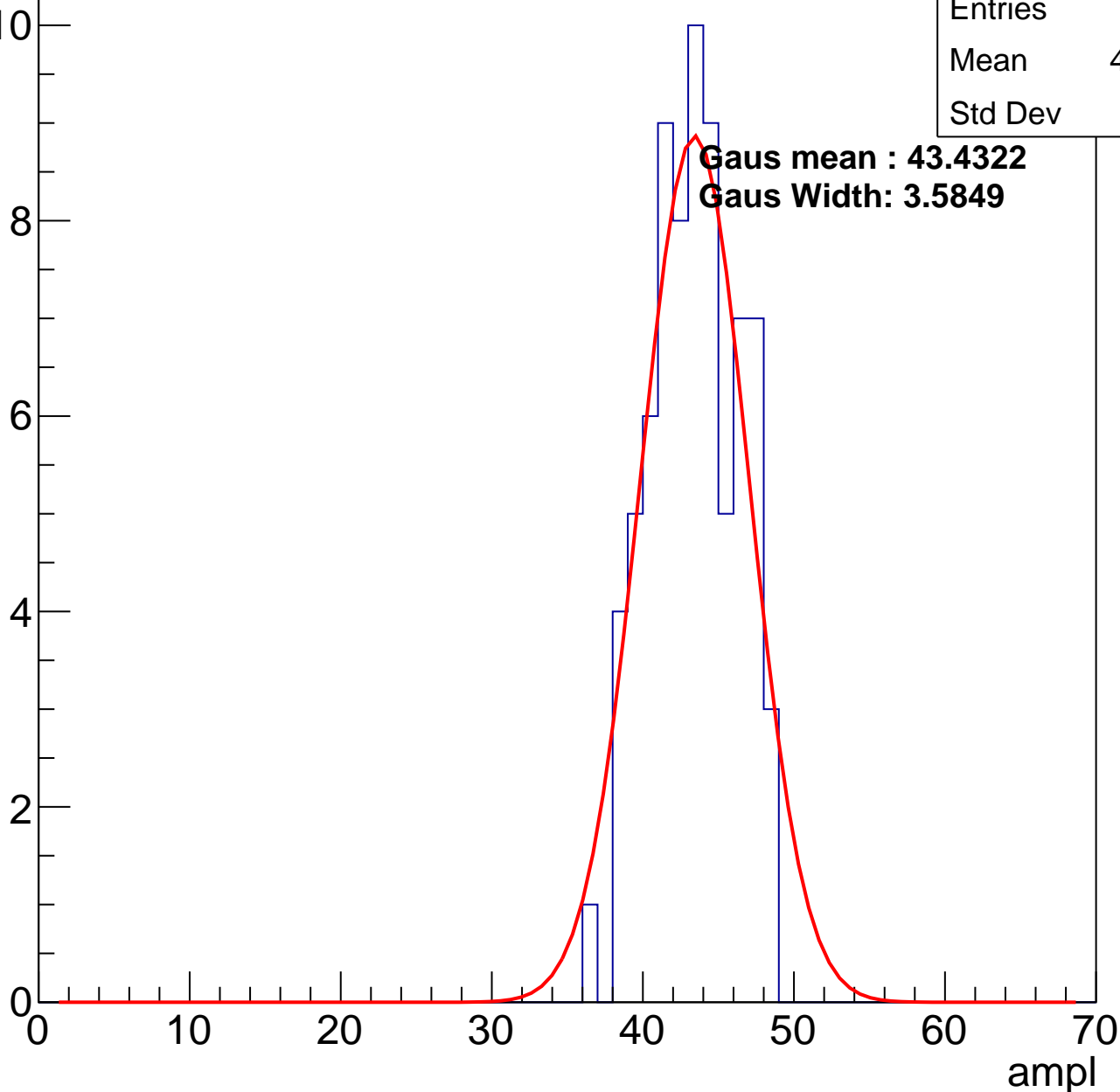
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	42.89
Std Dev	2.86

**Gaus mean : 43.4322**

**Gaus Width: 3.5849**



# B0L001S, U6-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

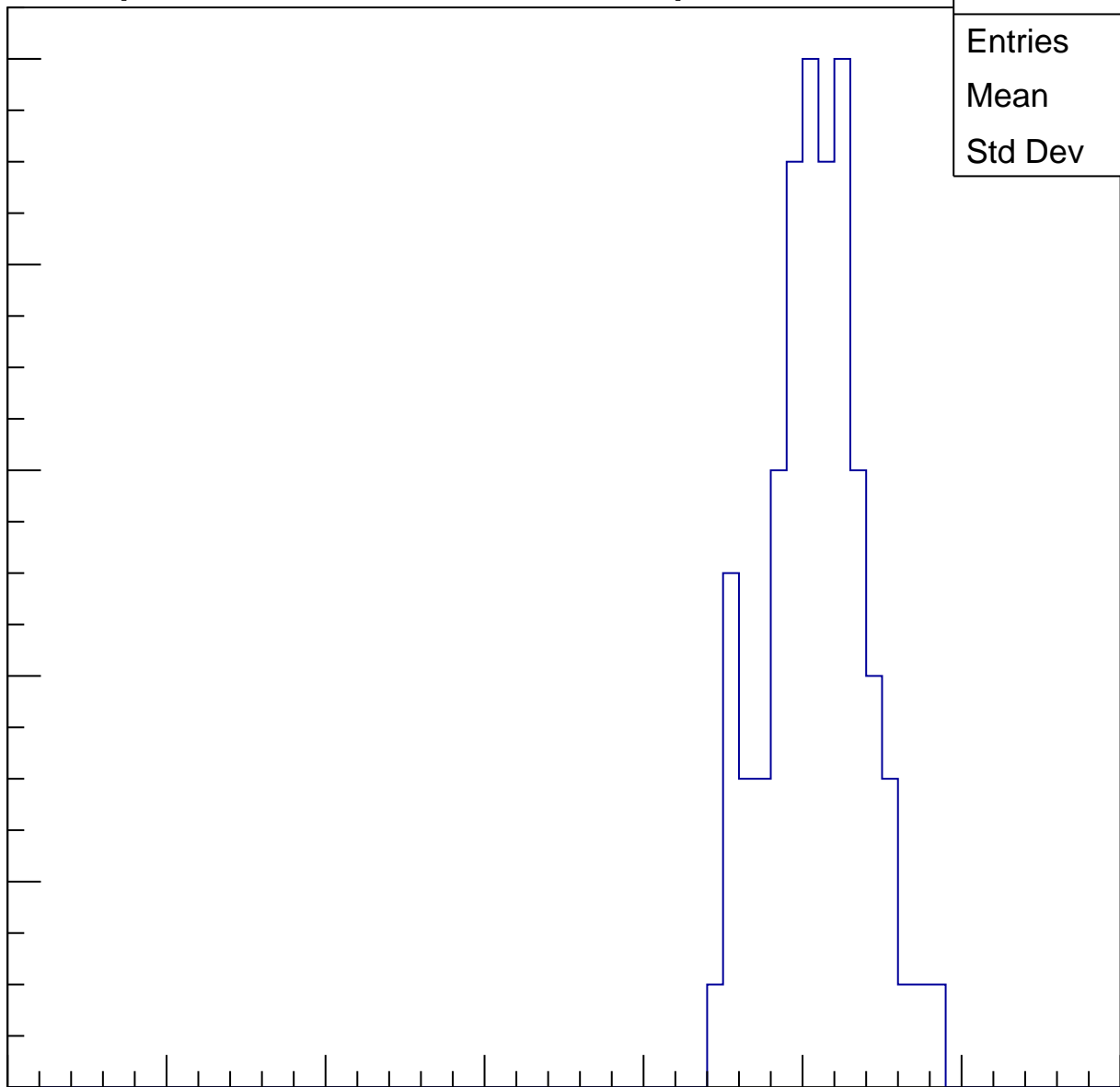
Entries	72
Mean	50.36
Std Dev	3.006

Entry

10  
8  
6  
4  
2  
0

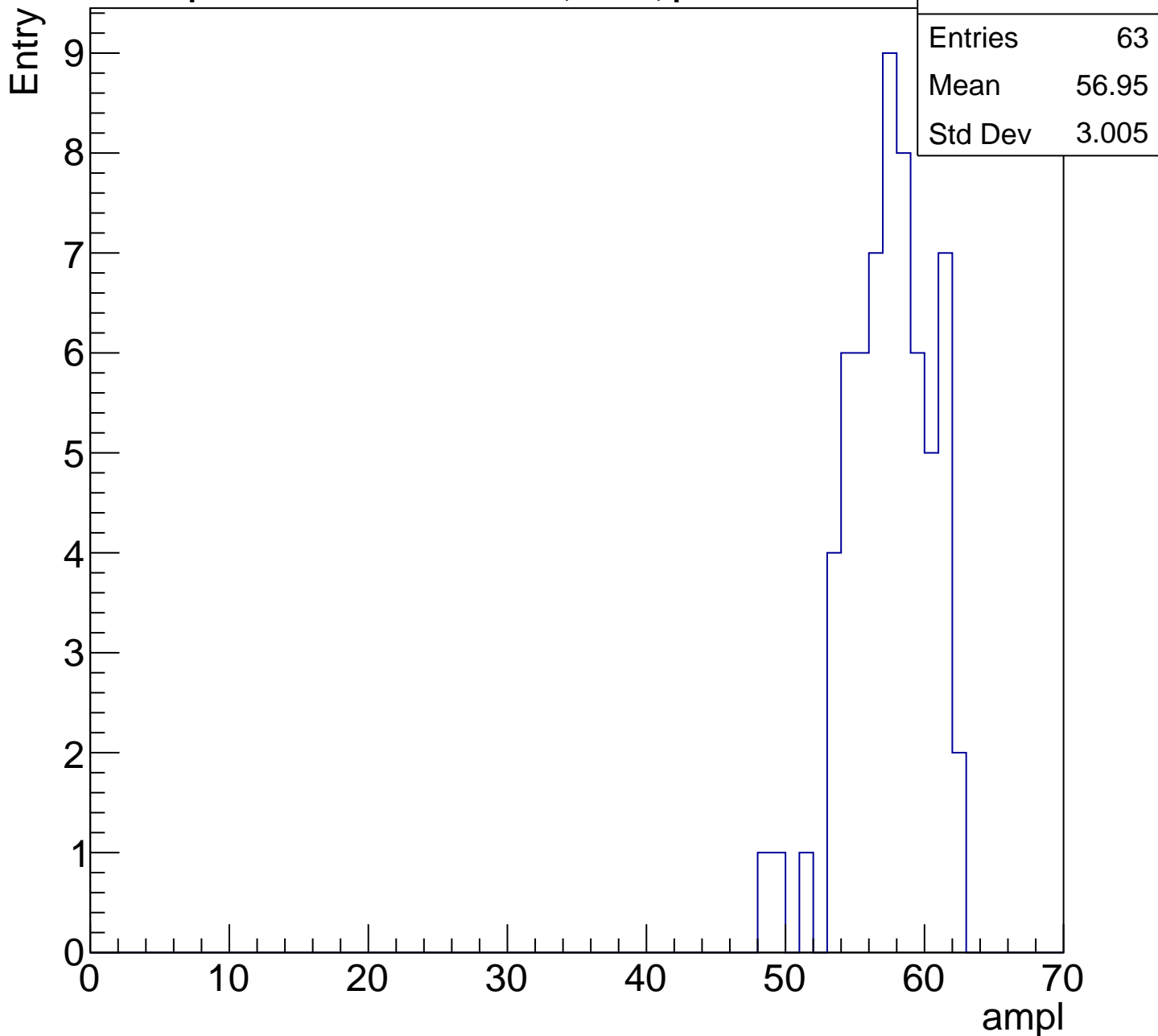
0 10 20 30 40 50 60 70

ampl



# B0L001S, U6-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

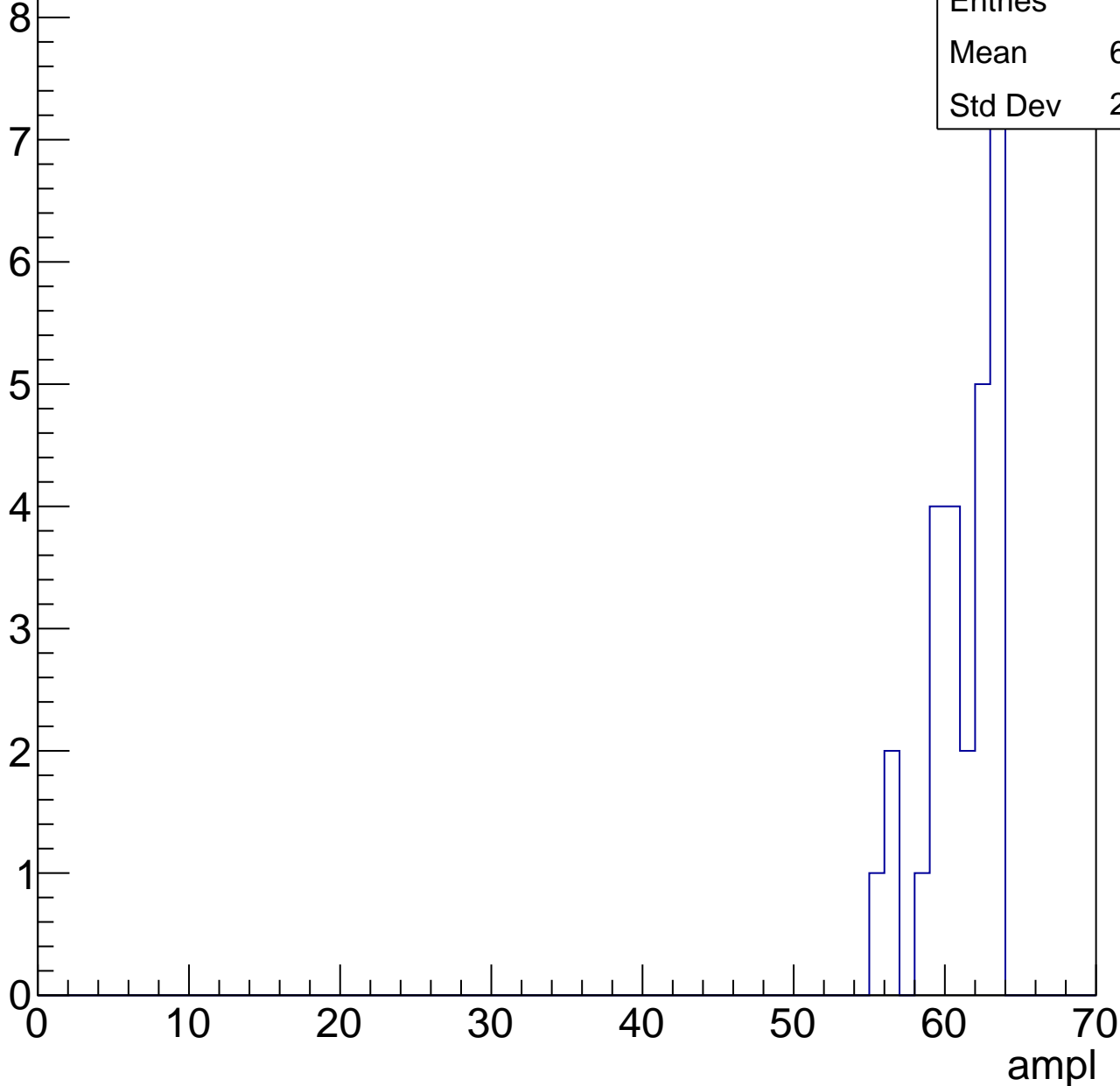


# B0L001S, U6-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

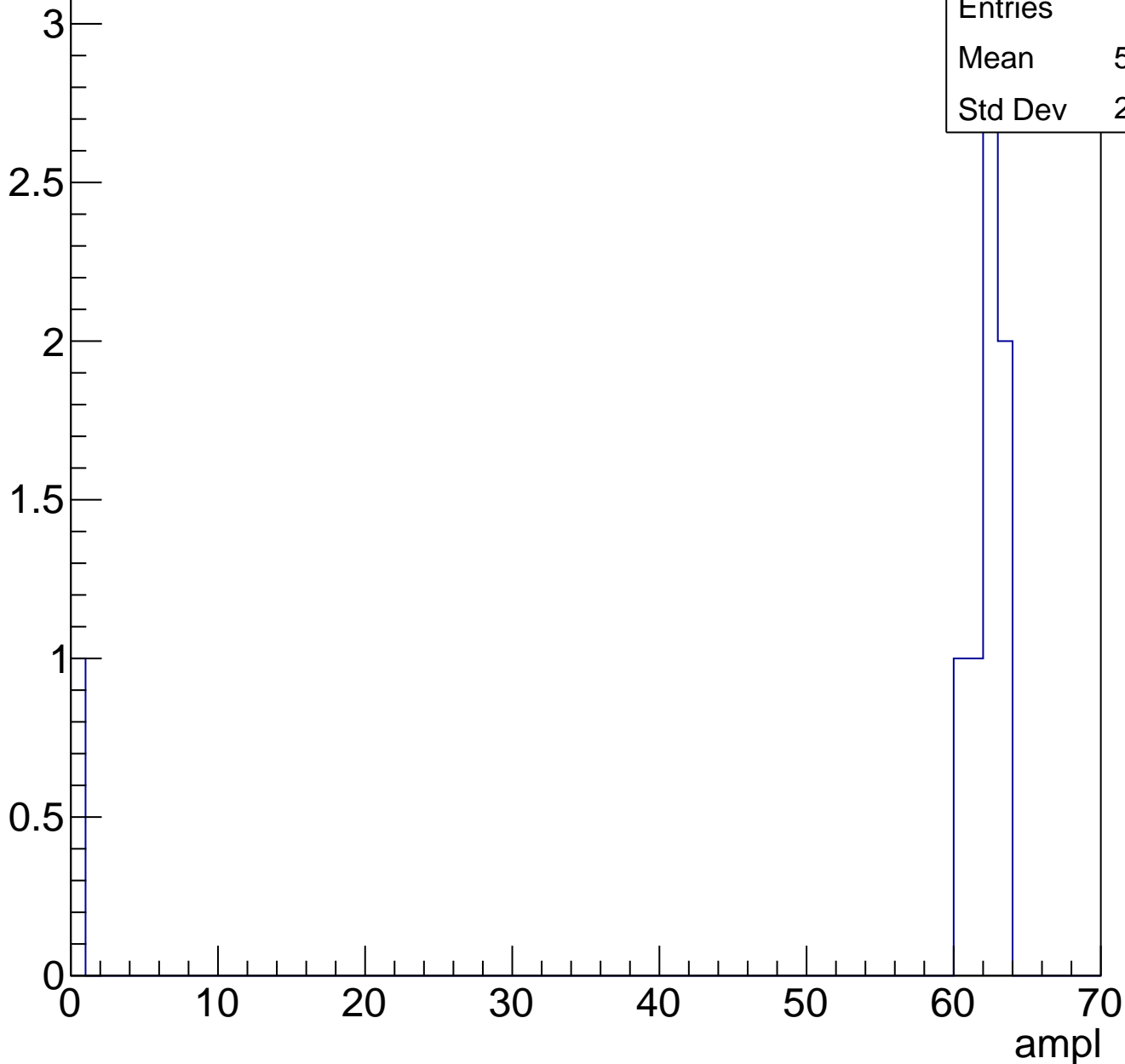
Entries	27
Mean	60.63
Std Dev	2.344



# B0L001S, U6-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch57, adc0

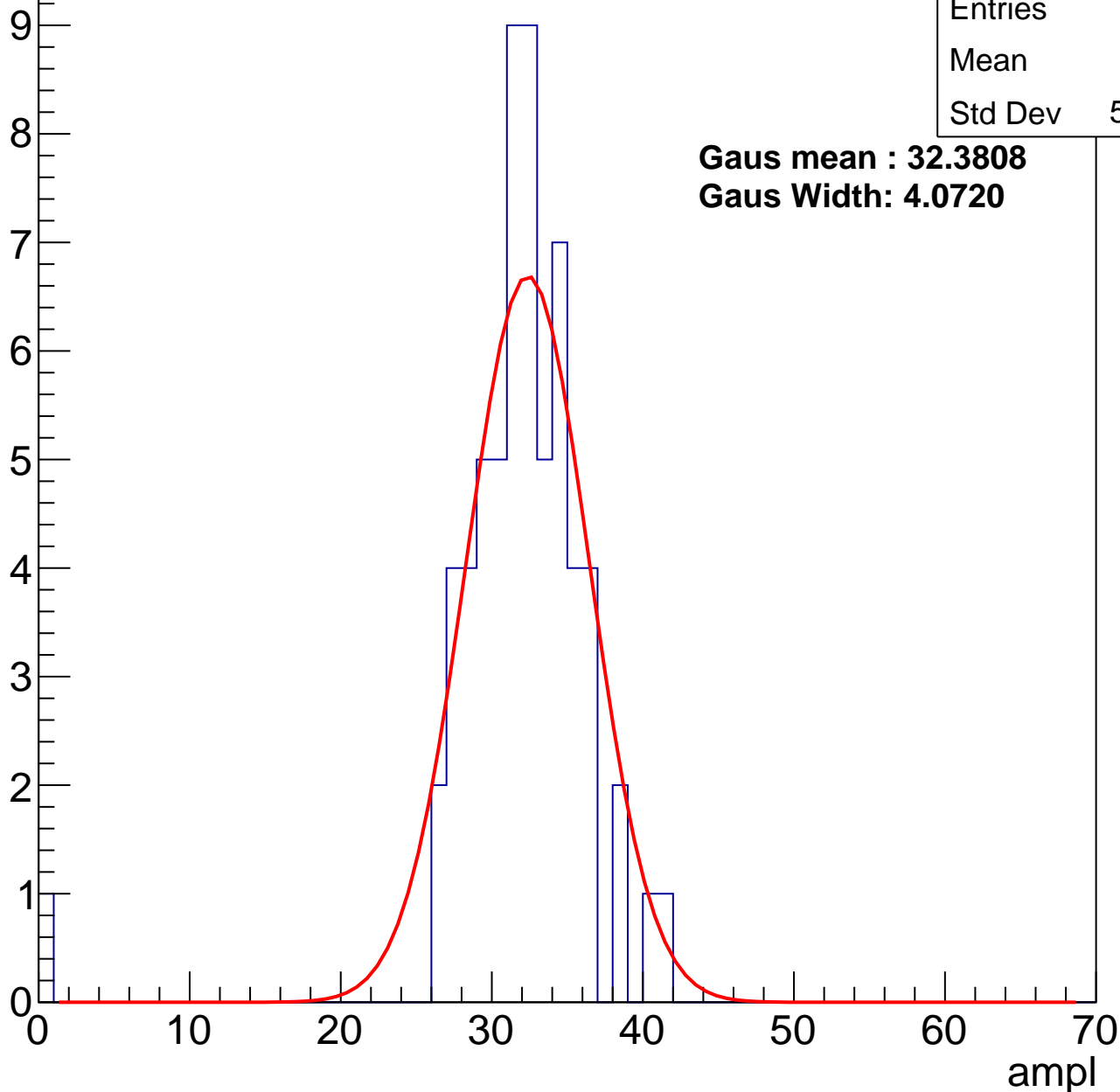
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	31.4
Std Dev	5.135

**Gaus mean : 32.3808**

**Gaus Width: 4.0720**



# B0L001S, U6-ch57, adc1

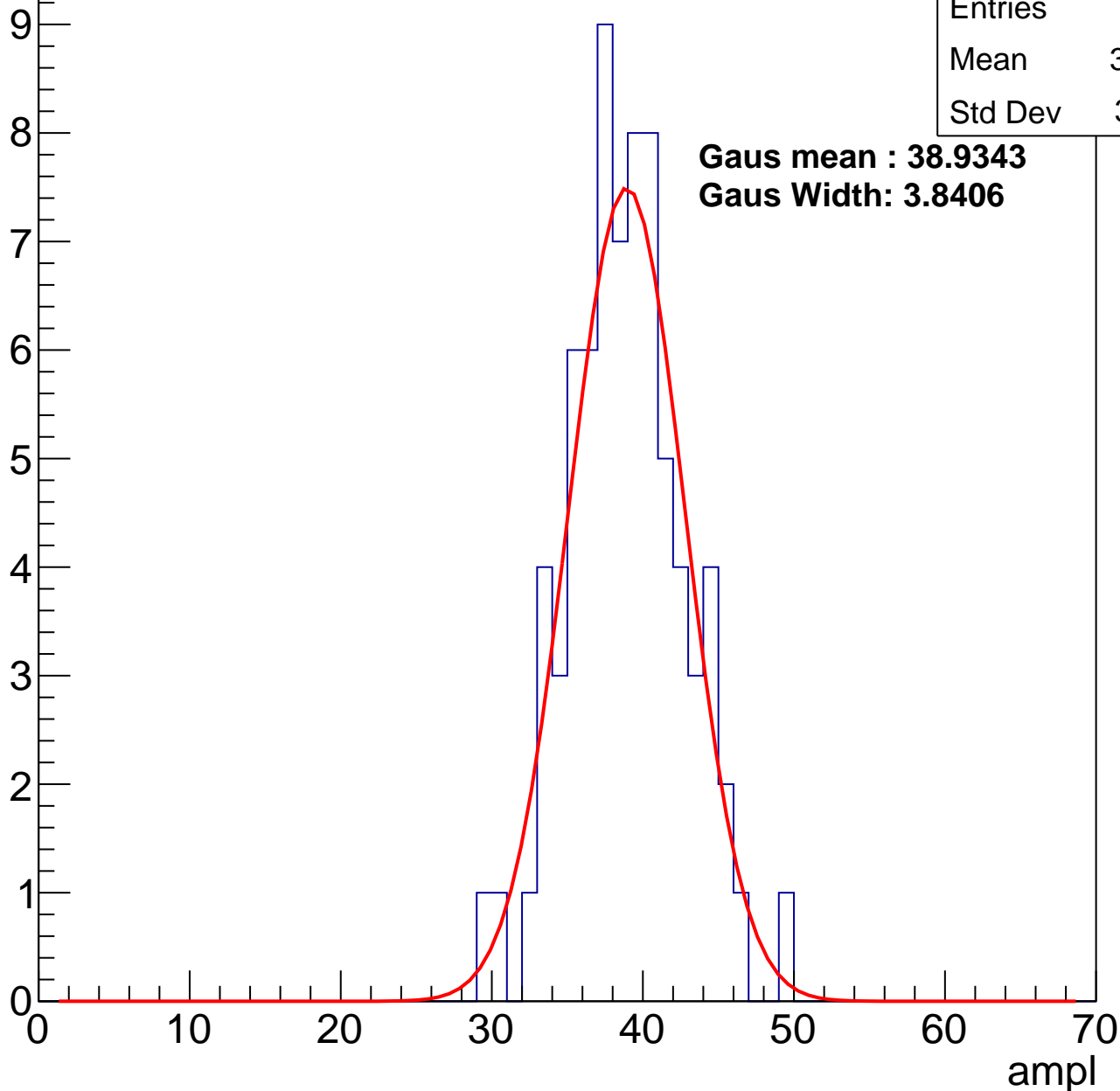
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	38.45
Std Dev	3.771

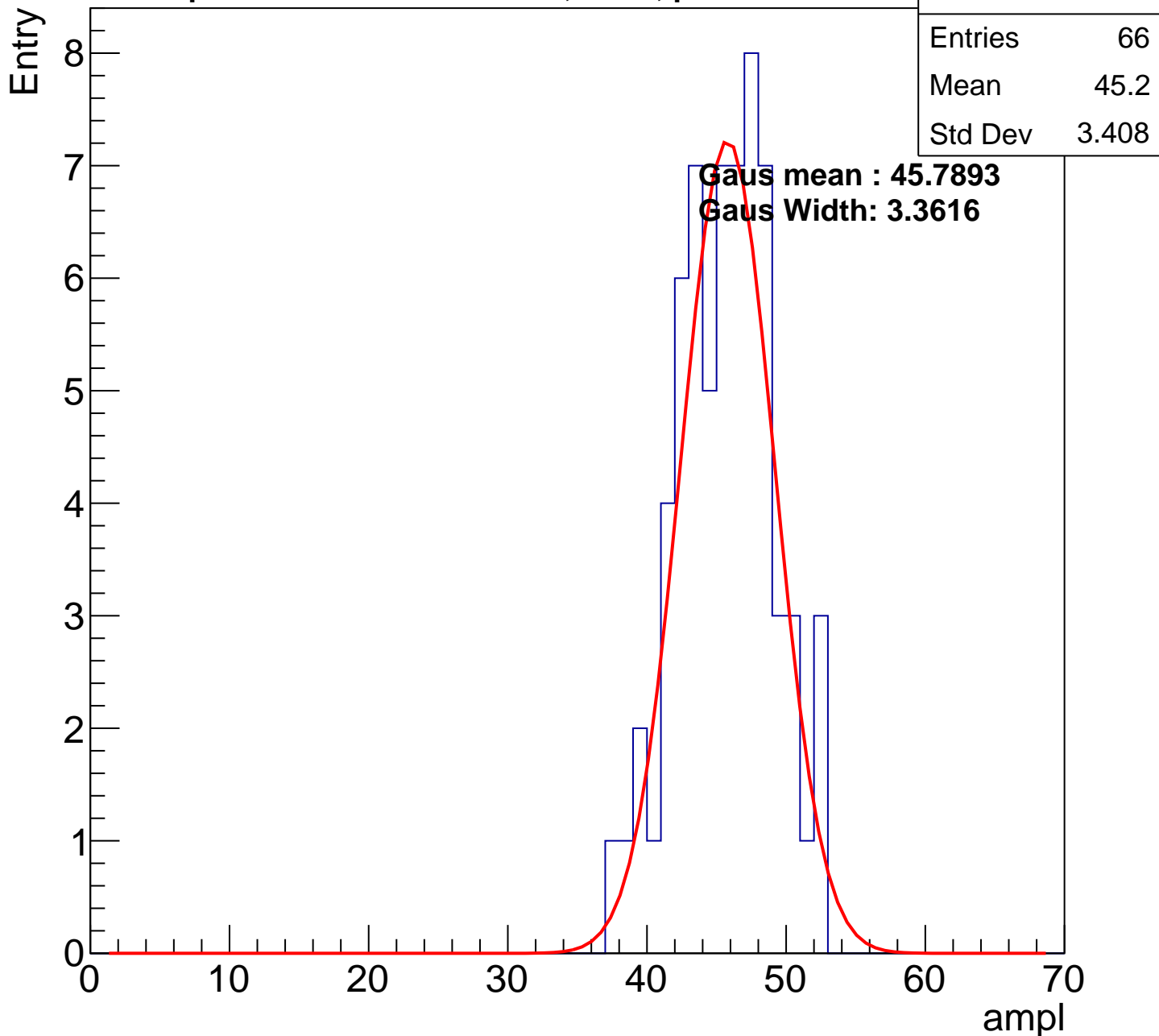
**Gaus mean : 38.9343**

**Gaus Width: 3.8406**



# B0L001S, U6-ch57, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

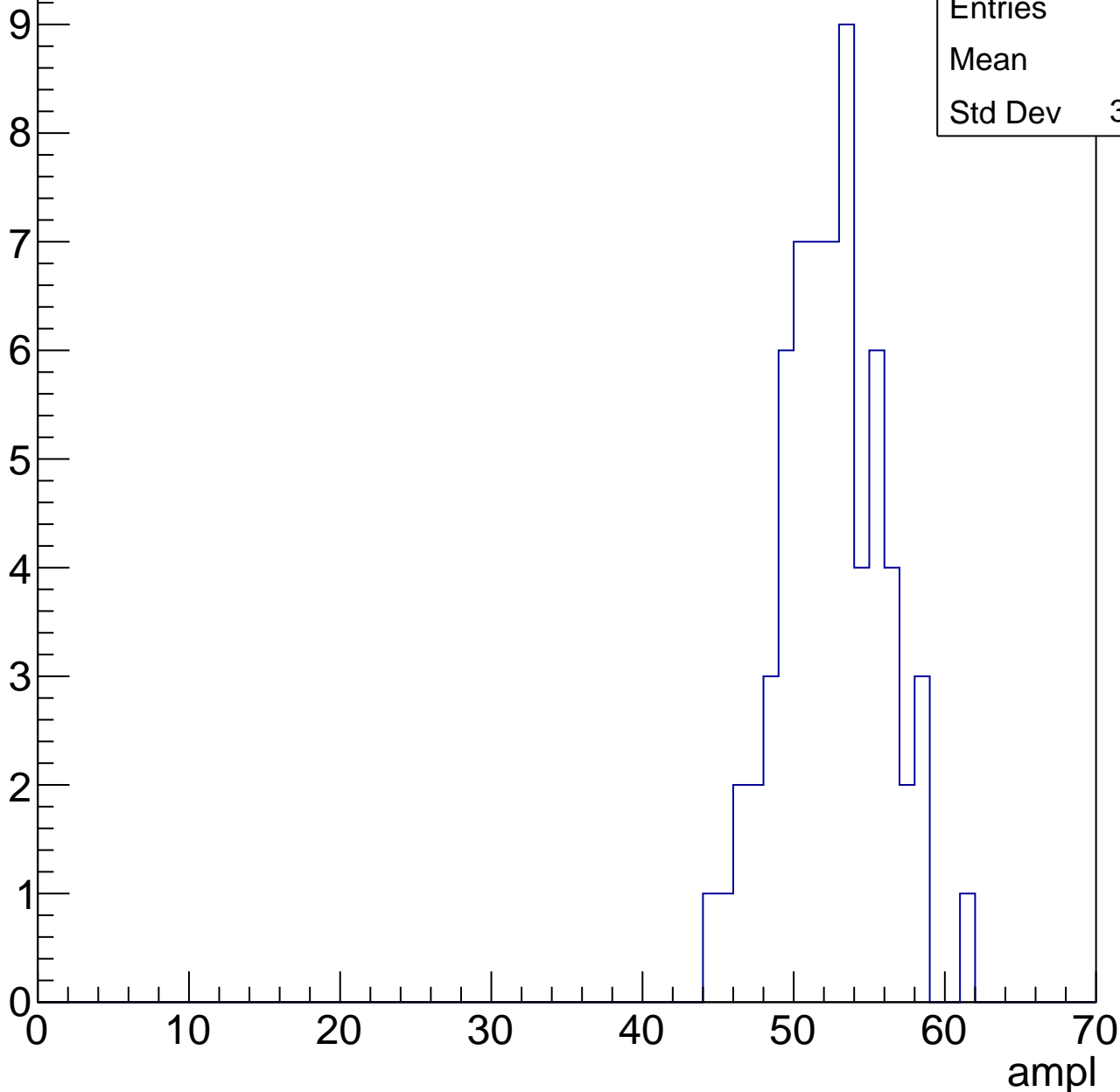


# B0L001S, U6-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	52
Std Dev	3.406

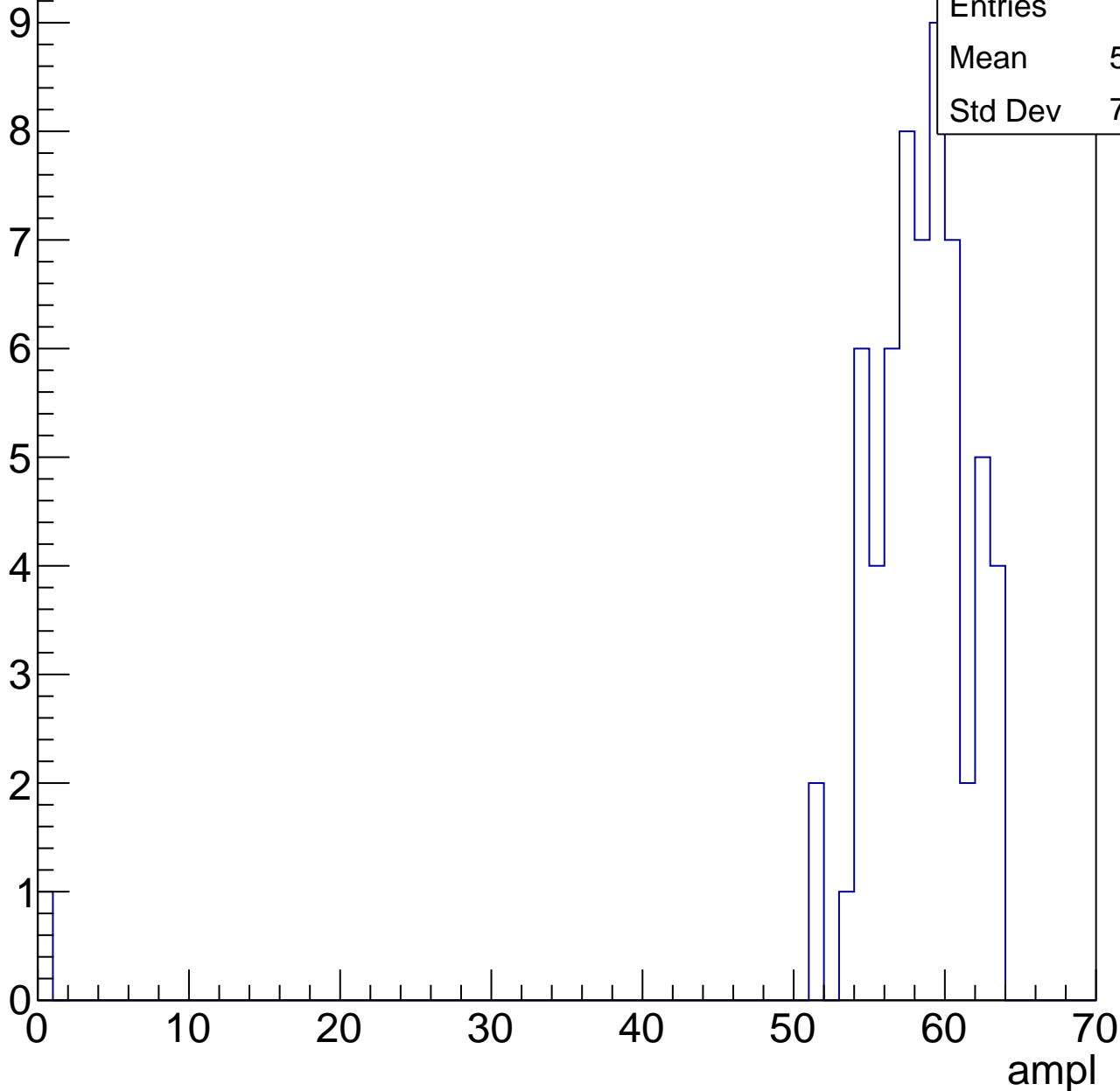


# B0L001S, U6-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	56.97
Std Dev	7.849

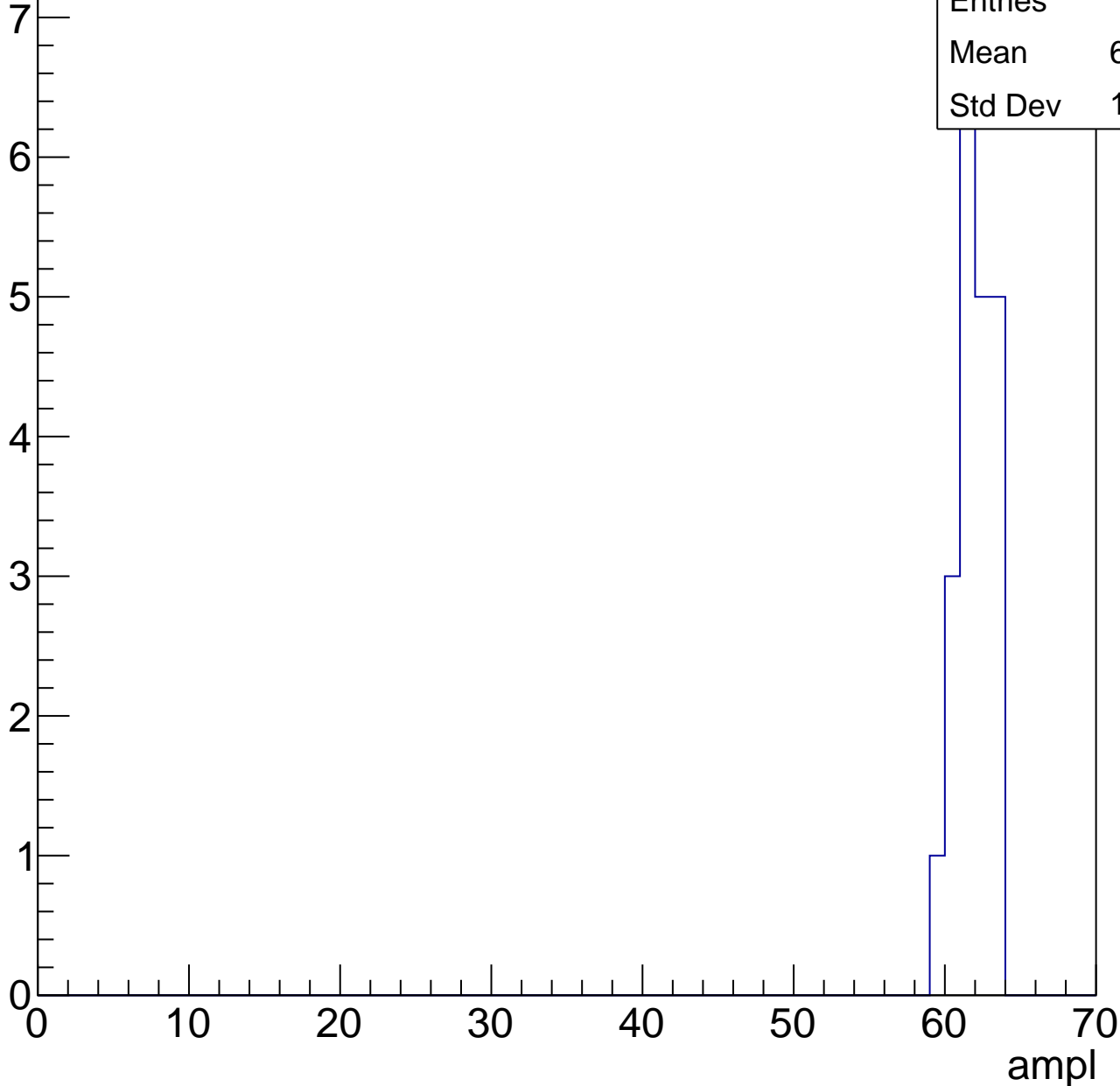


# B0L001S, U6-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	21
Mean	61.48
Std Dev	1.139



# B0L001S, U6-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

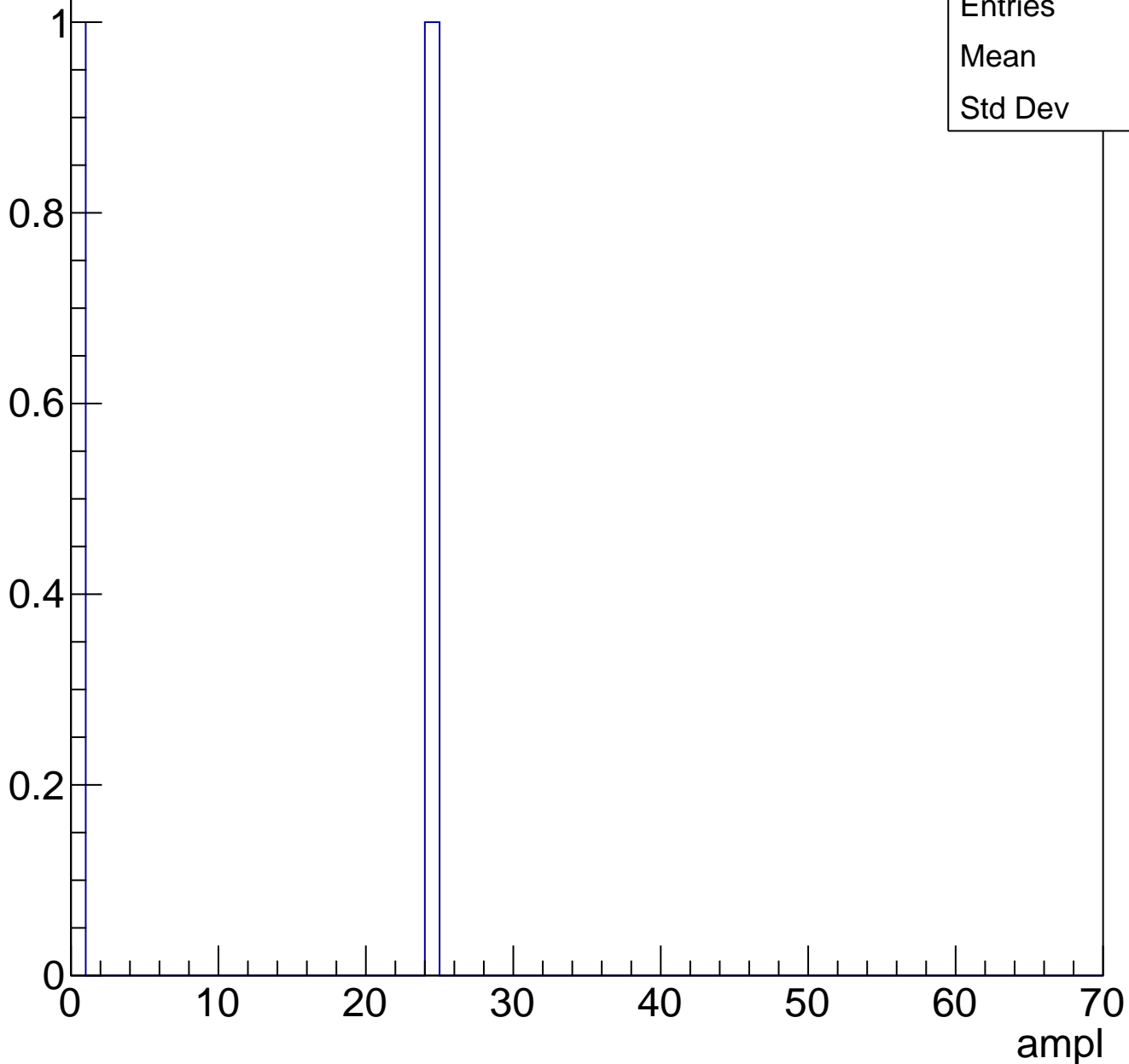




# B0L001S, U6-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch58, adc0

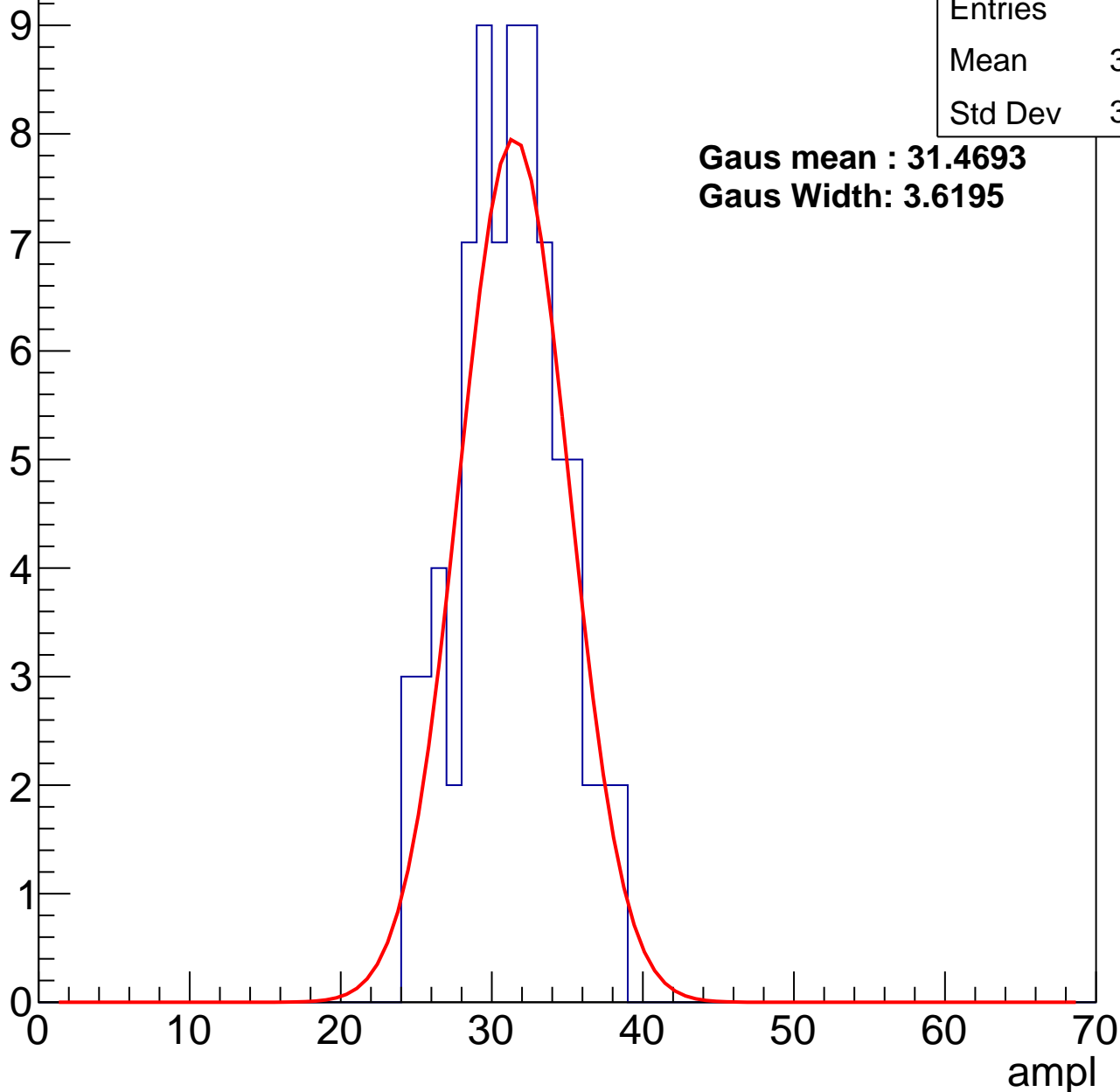
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	30.75
Std Dev	3.384

**Gaus mean : 31.4693**

**Gaus Width: 3.6195**



# B0L001S, U6-ch58, adc1

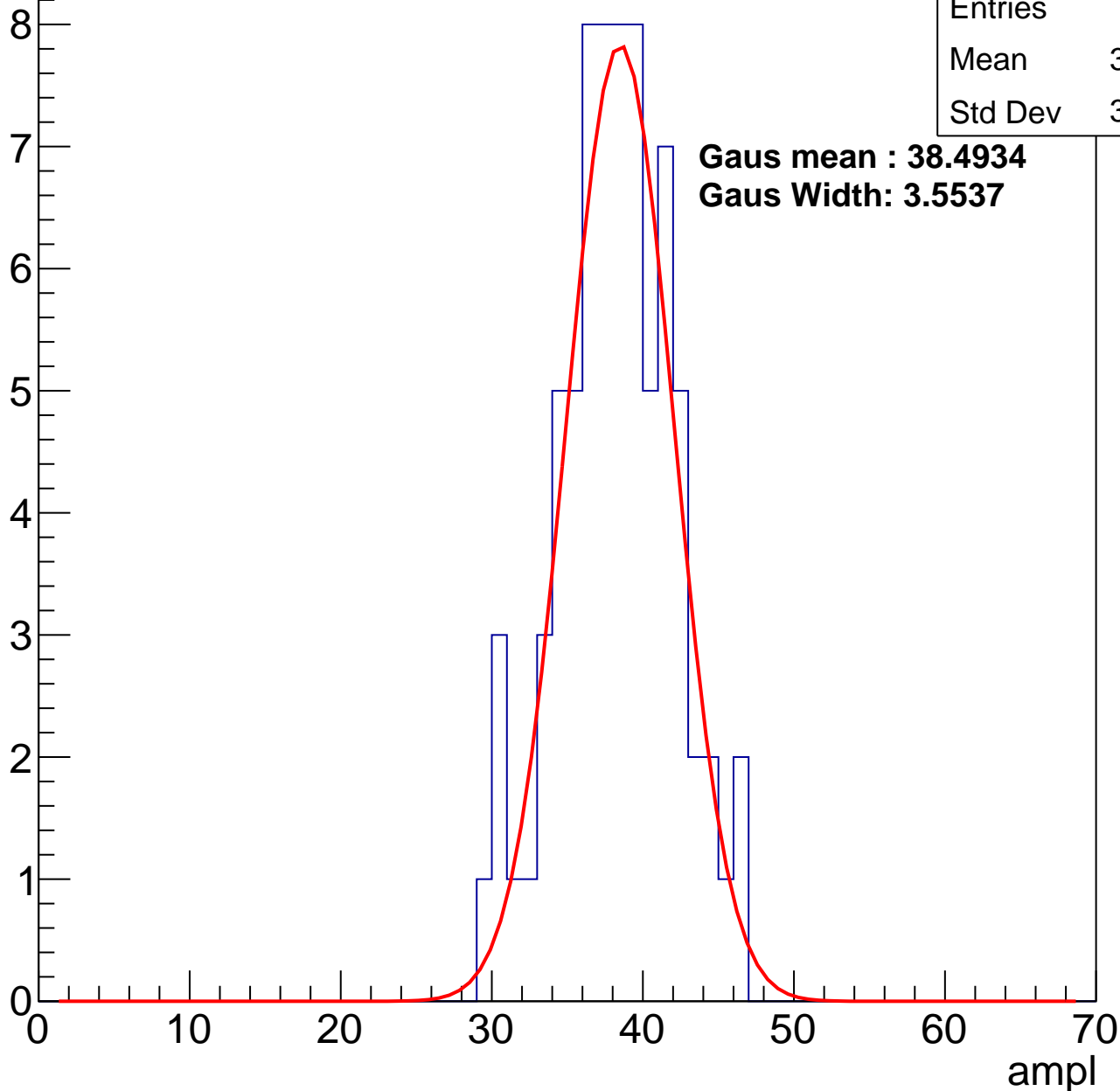
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	37.79
Std Dev	3.768

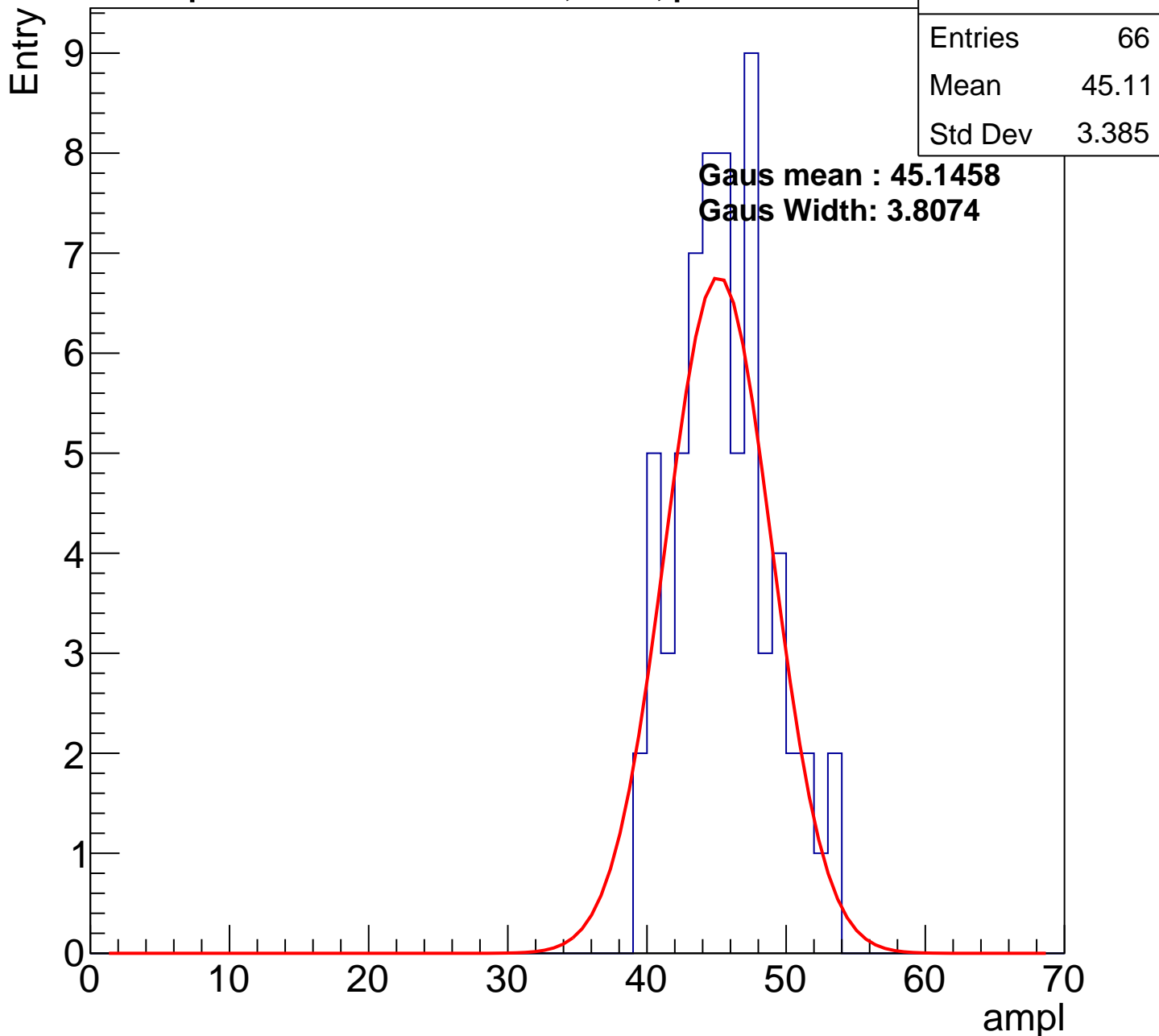
**Gaus mean : 38.4934**

**Gaus Width: 3.5537**



# B0L001S, U6-ch58, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

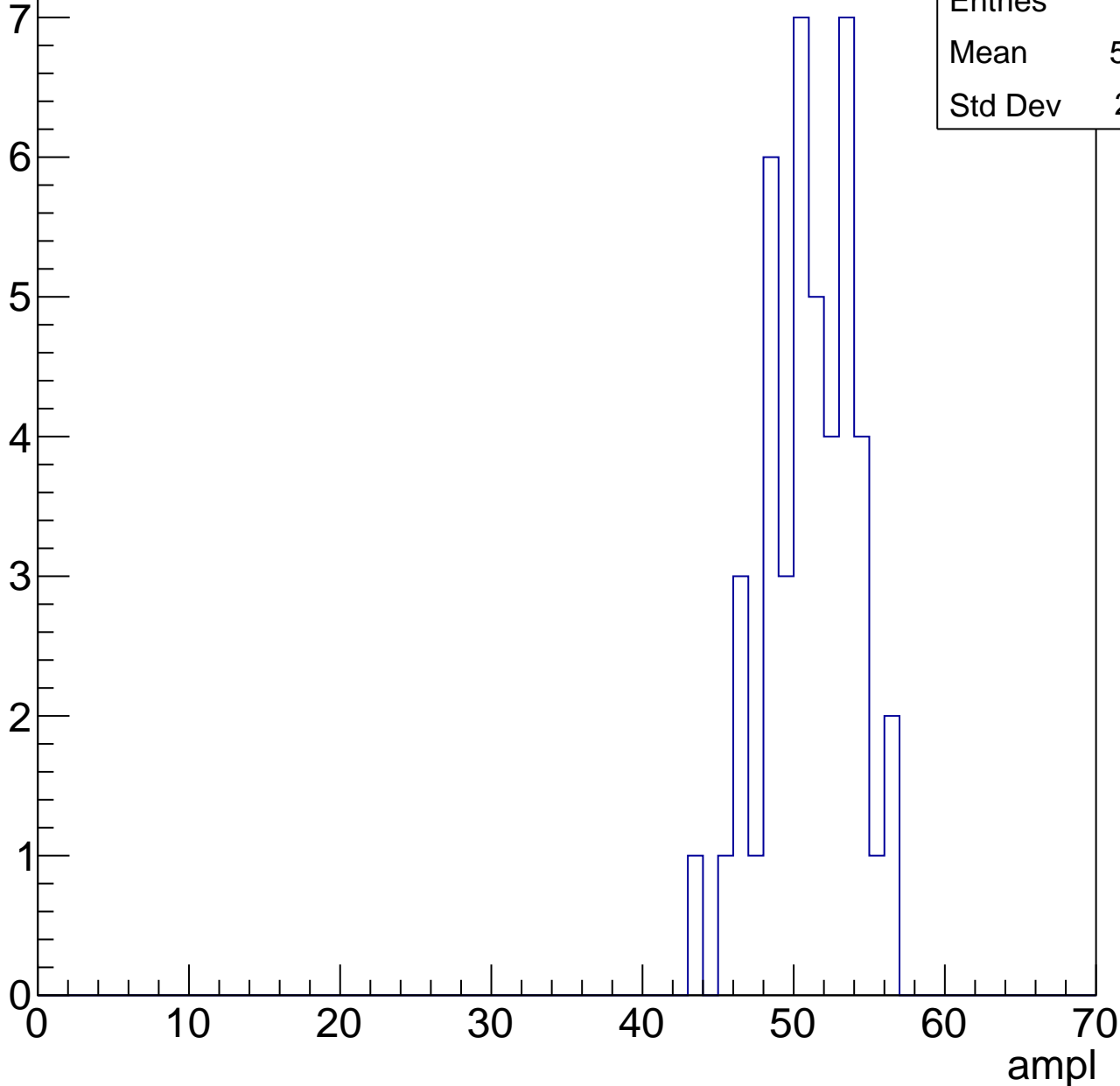


# B0L001S, U6-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

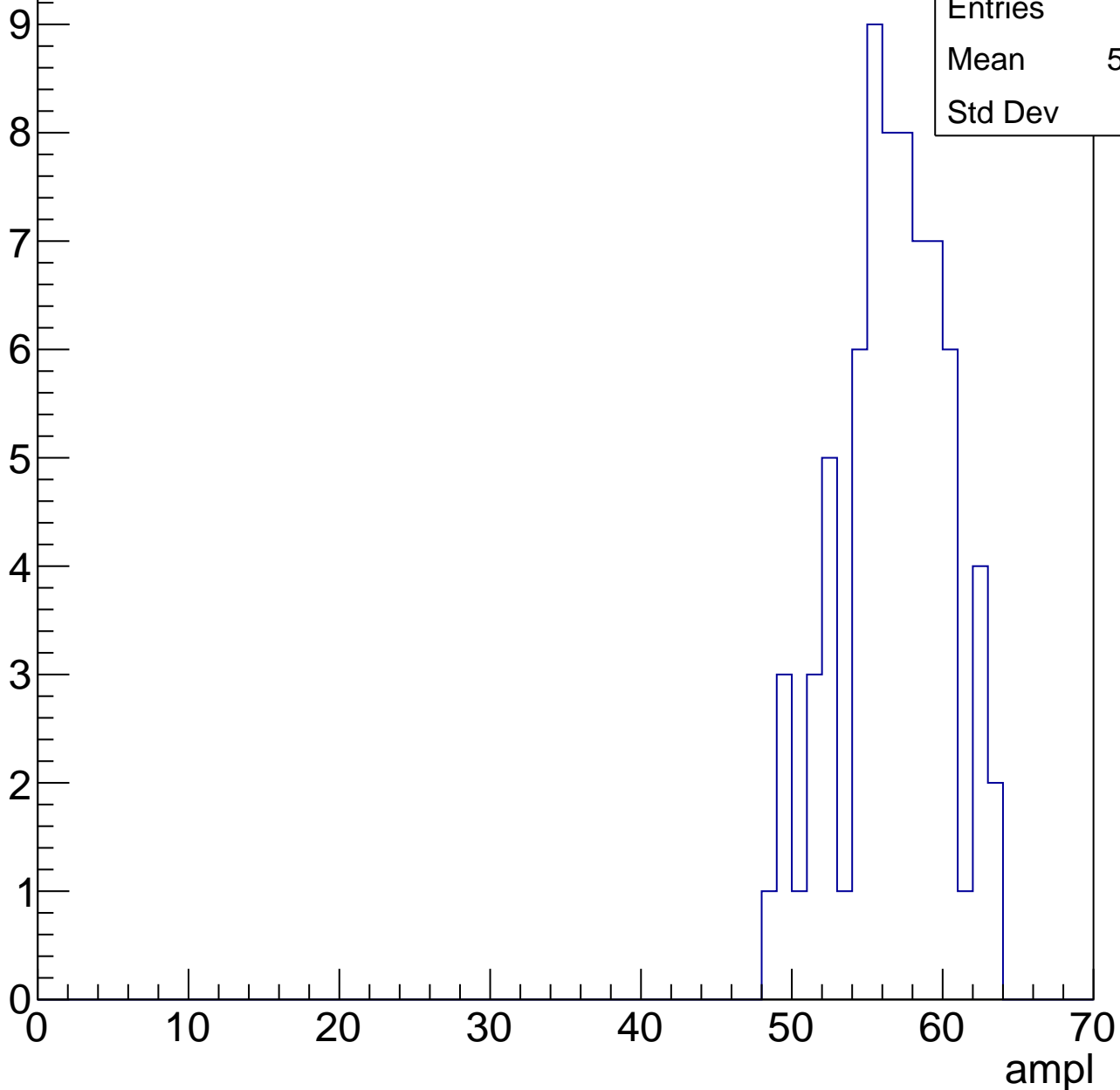
Entries	45
Mean	50.56
Std Dev	2.941



# B0L001S, U6-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



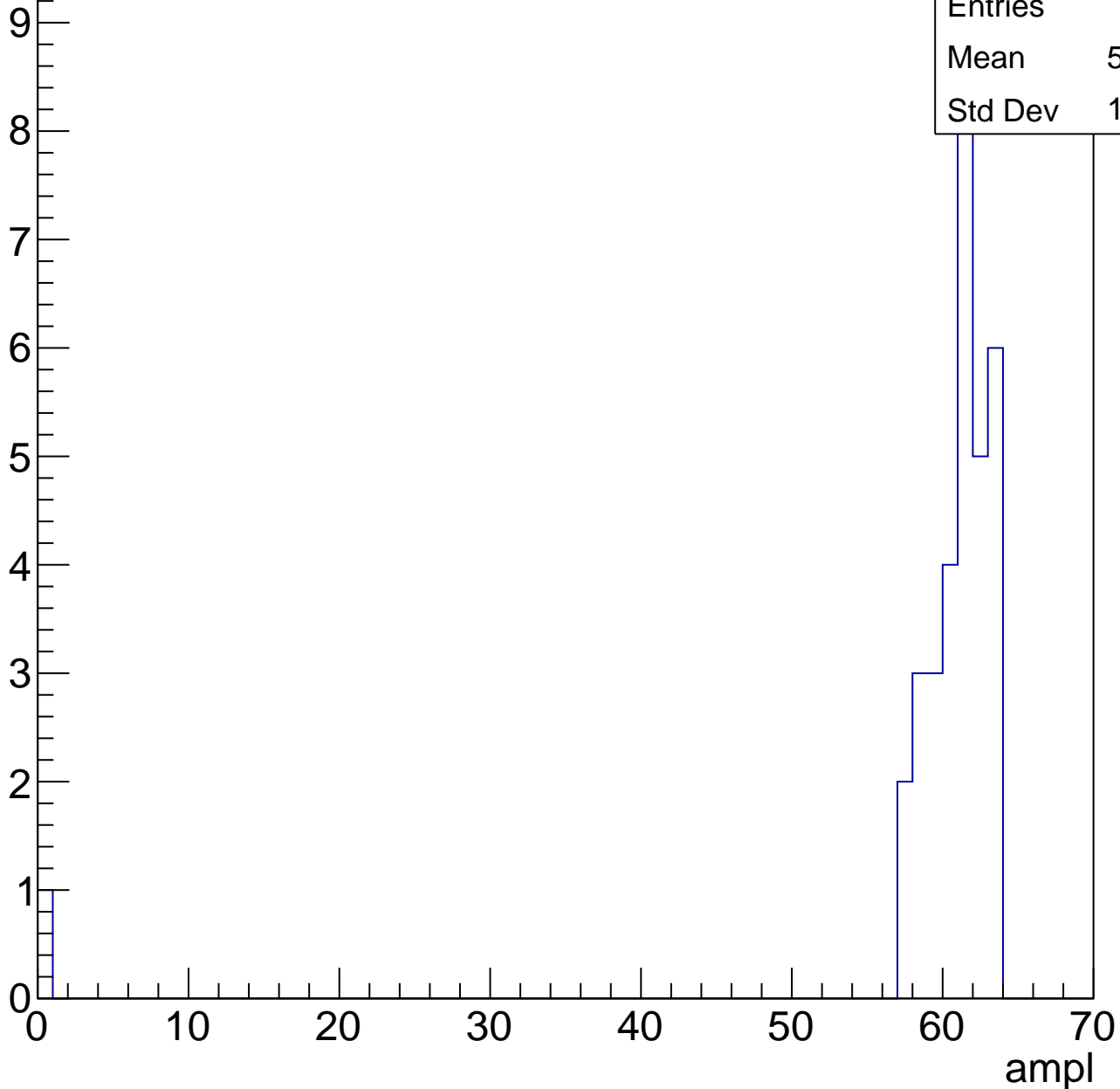
Entries	72
Mean	56.22
Std Dev	3.54

# B0L001S, U6-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	33
Mean	58.85
Std Dev	10.55



# B0L001S, U6-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B0L001S, U6-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L001S, U6-ch59, adc0

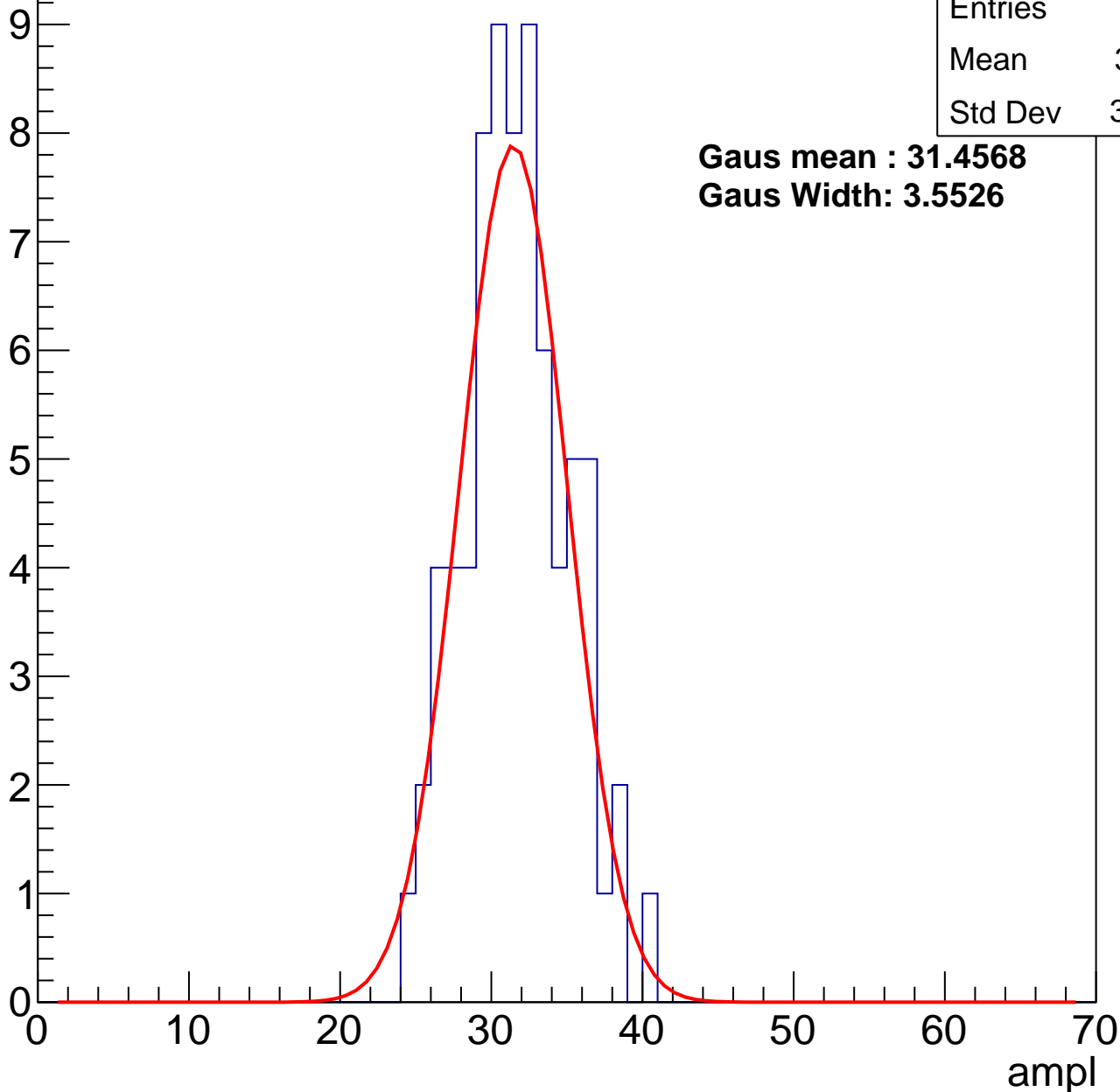
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	31.21
Std Dev	3.408

**Gaus mean : 31.4568**

**Gaus Width: 3.5526**



# B0L001S, U6-ch59, adc1

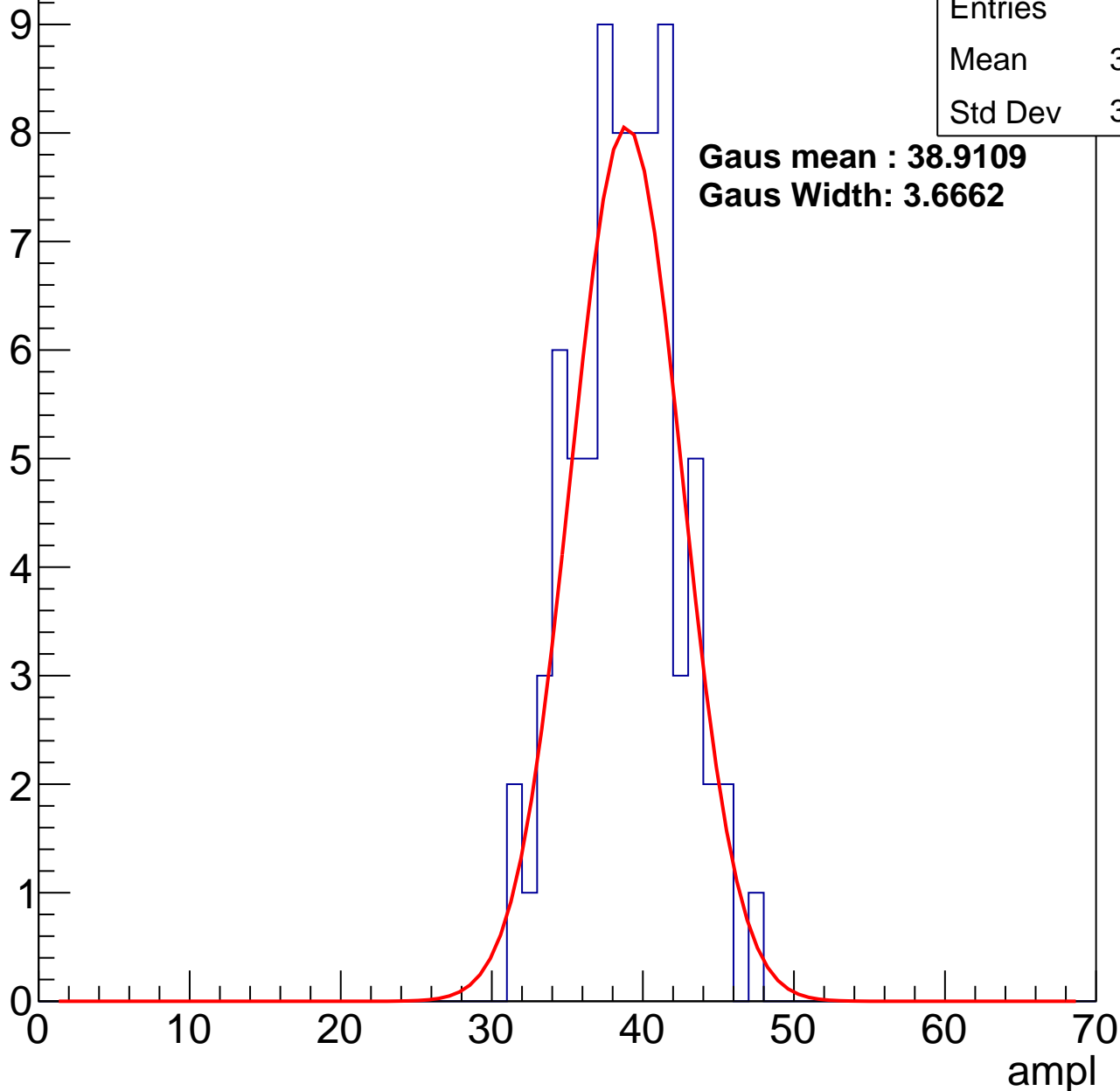
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	38.39
Std Dev	3.442

**Gaus mean : 38.9109**

**Gaus Width: 3.6662**



# B0L001S, U6-ch59, adc2

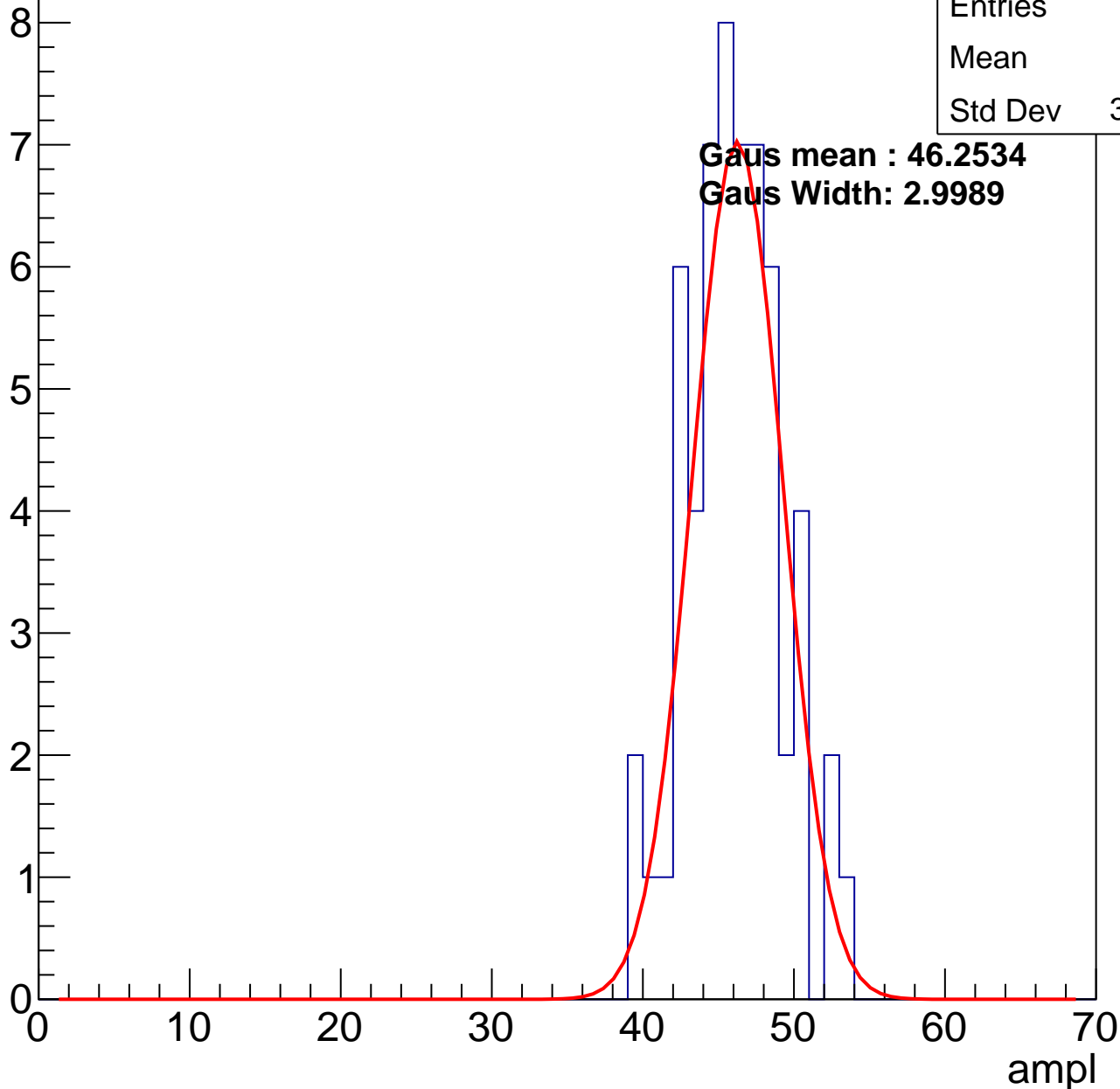
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	45.6
Std Dev	3.085

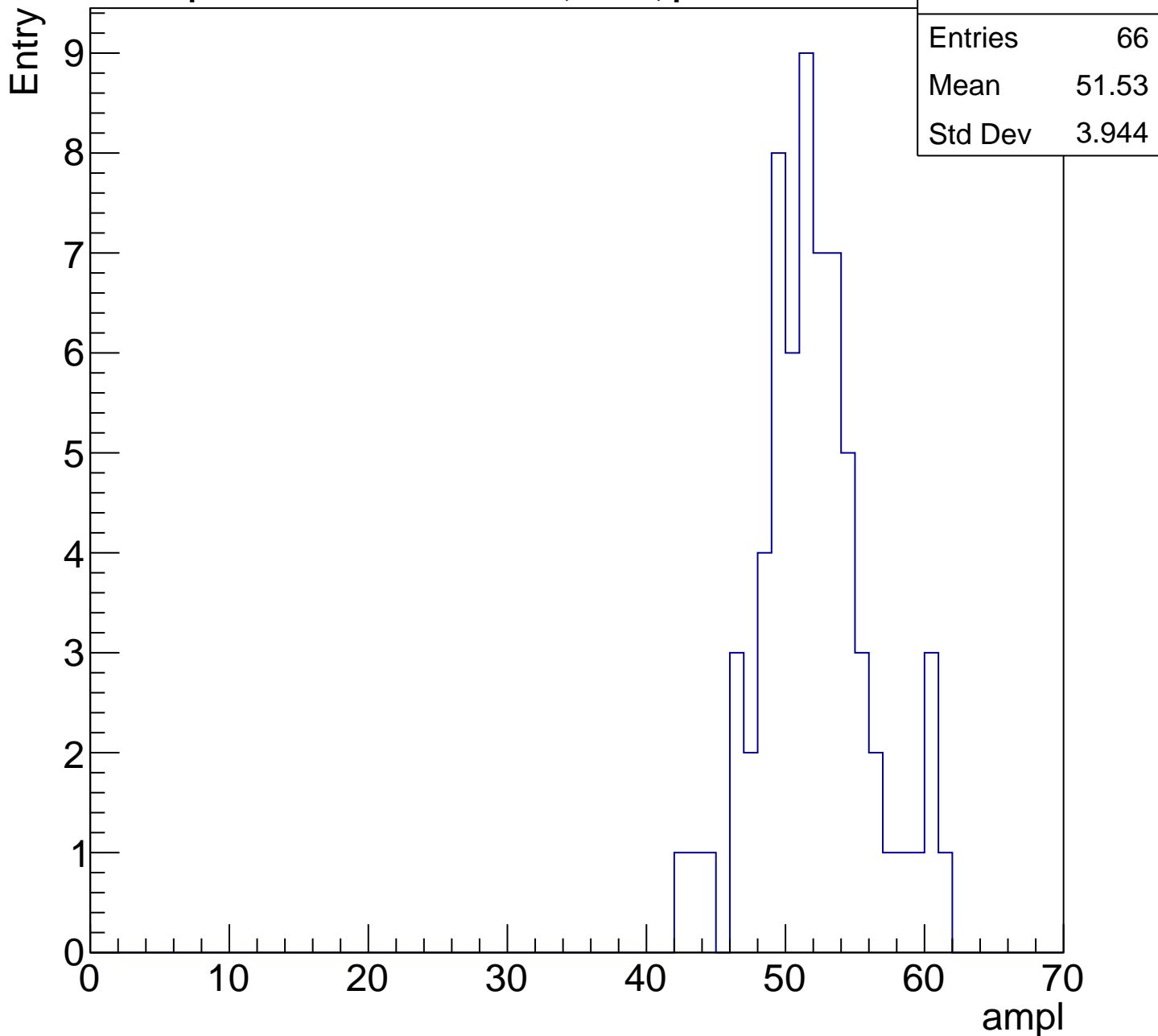
**Gaus mean : 46.2534**

**Gaus Width: 2.9989**



# B0L001S, U6-ch59, adc3

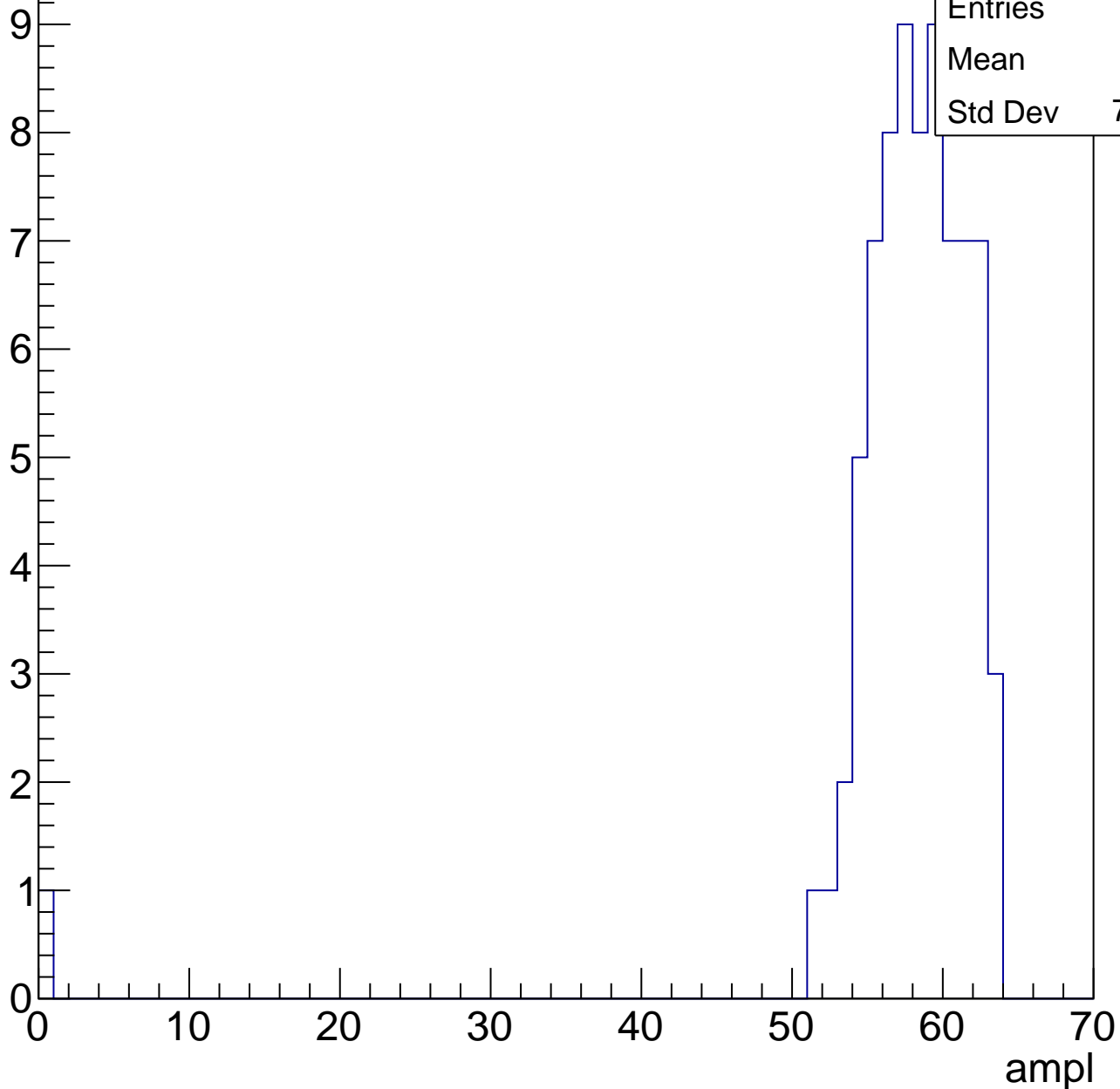
calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U6-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

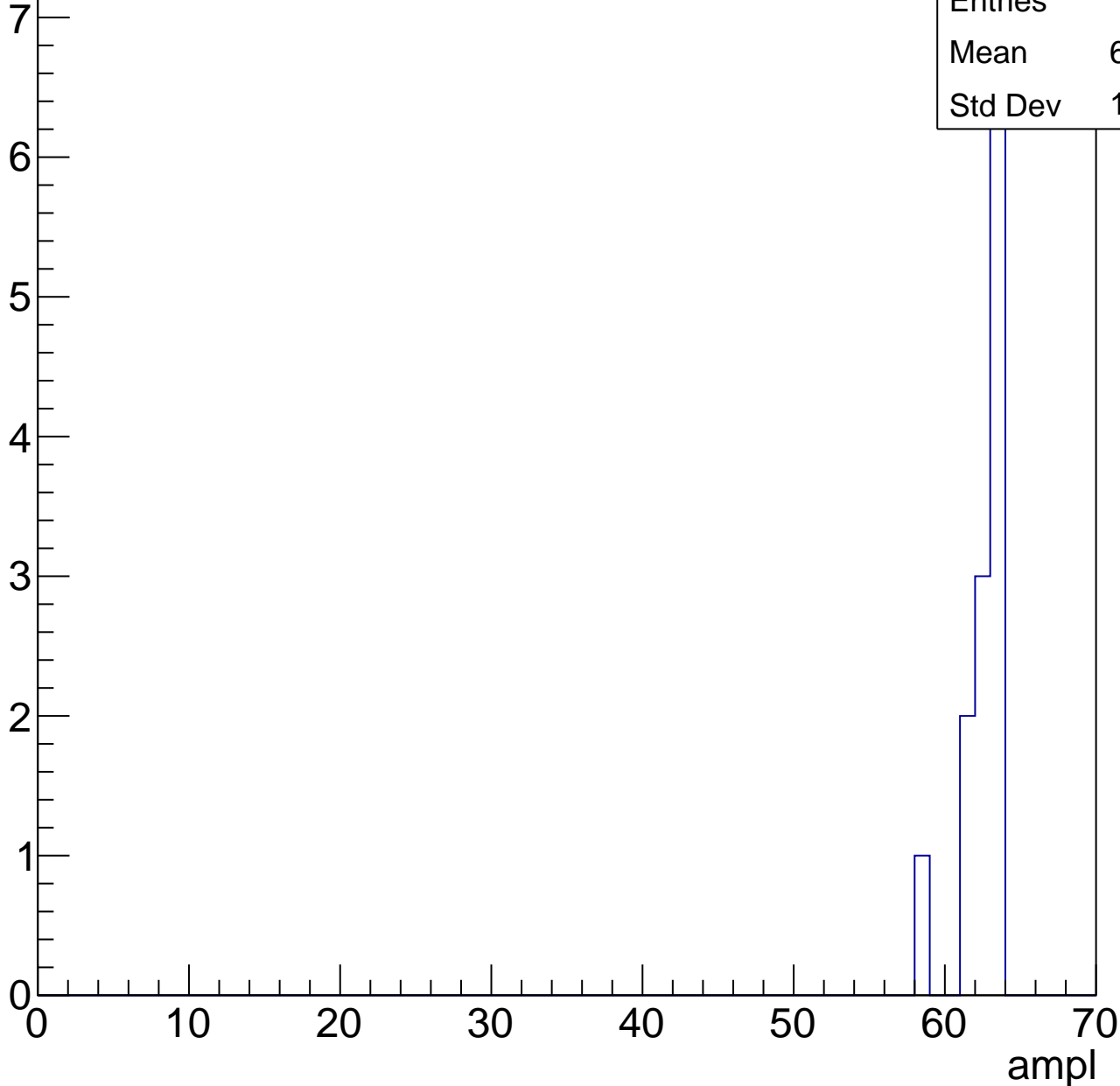


# B0L001S, U6-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	13
Mean	62.08
Std Dev	1.385



# B0L001S, U6-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U6-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U6-ch60, adc0

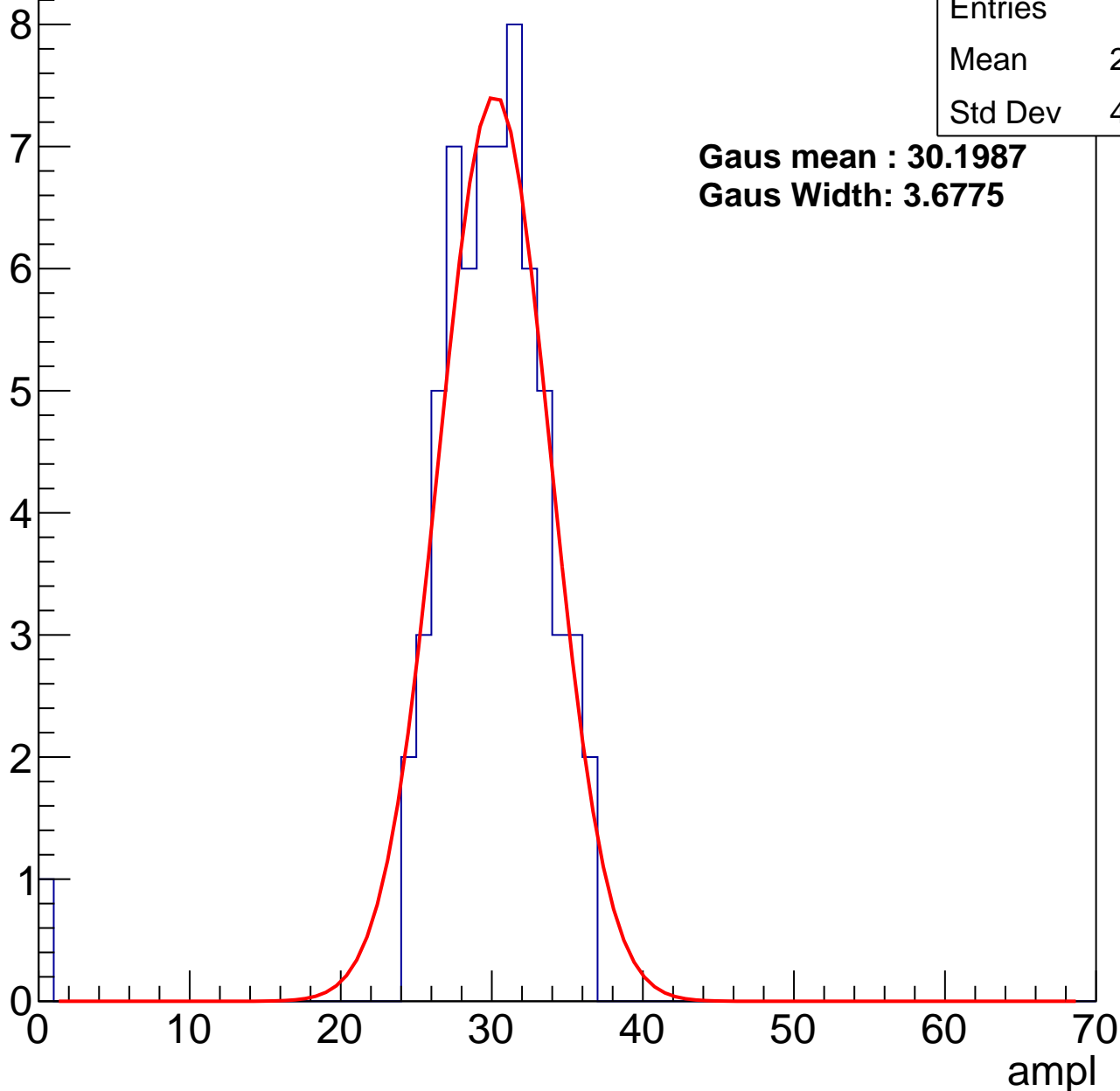
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	29.34
Std Dev	4.747

**Gaus mean : 30.1987**

**Gaus Width: 3.6775**



# B0L001S, U6-ch60, adc1

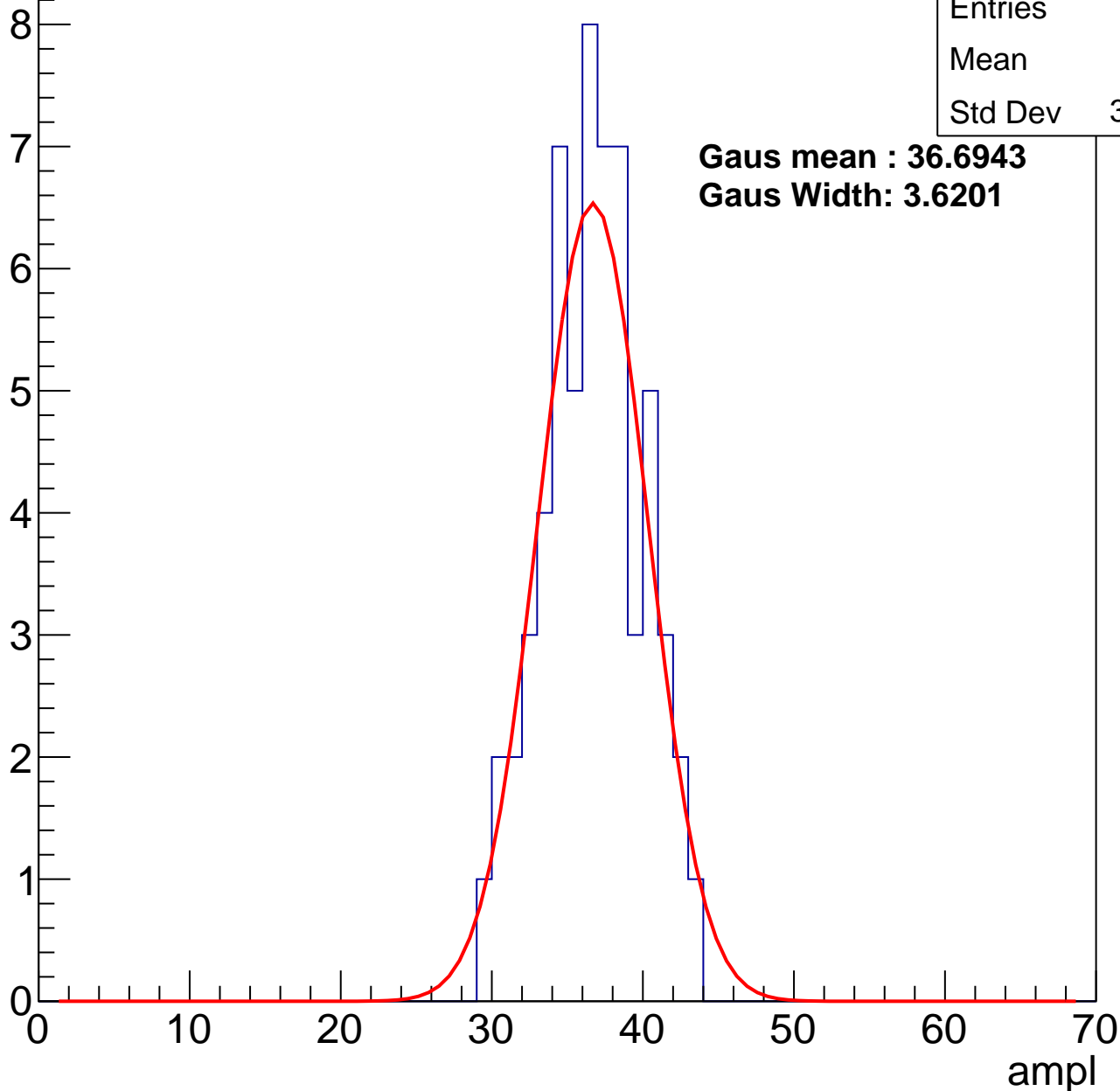
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	36.2
Std Dev	3.224

**Gaus mean : 36.6943**

**Gaus Width: 3.6201**



# B0L001S, U6-ch60, adc2

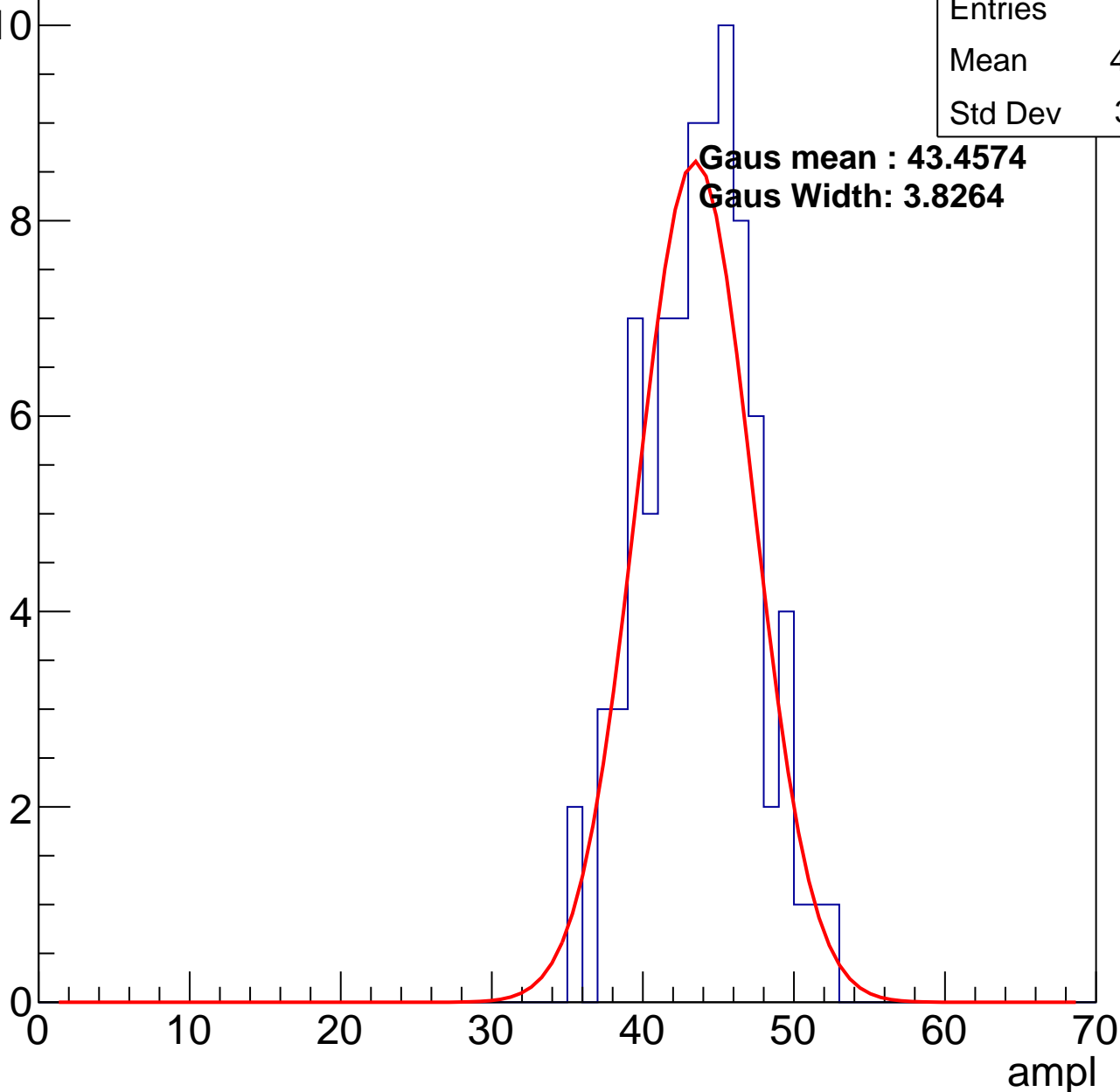
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	85
Mean	43.26
Std Dev	3.601

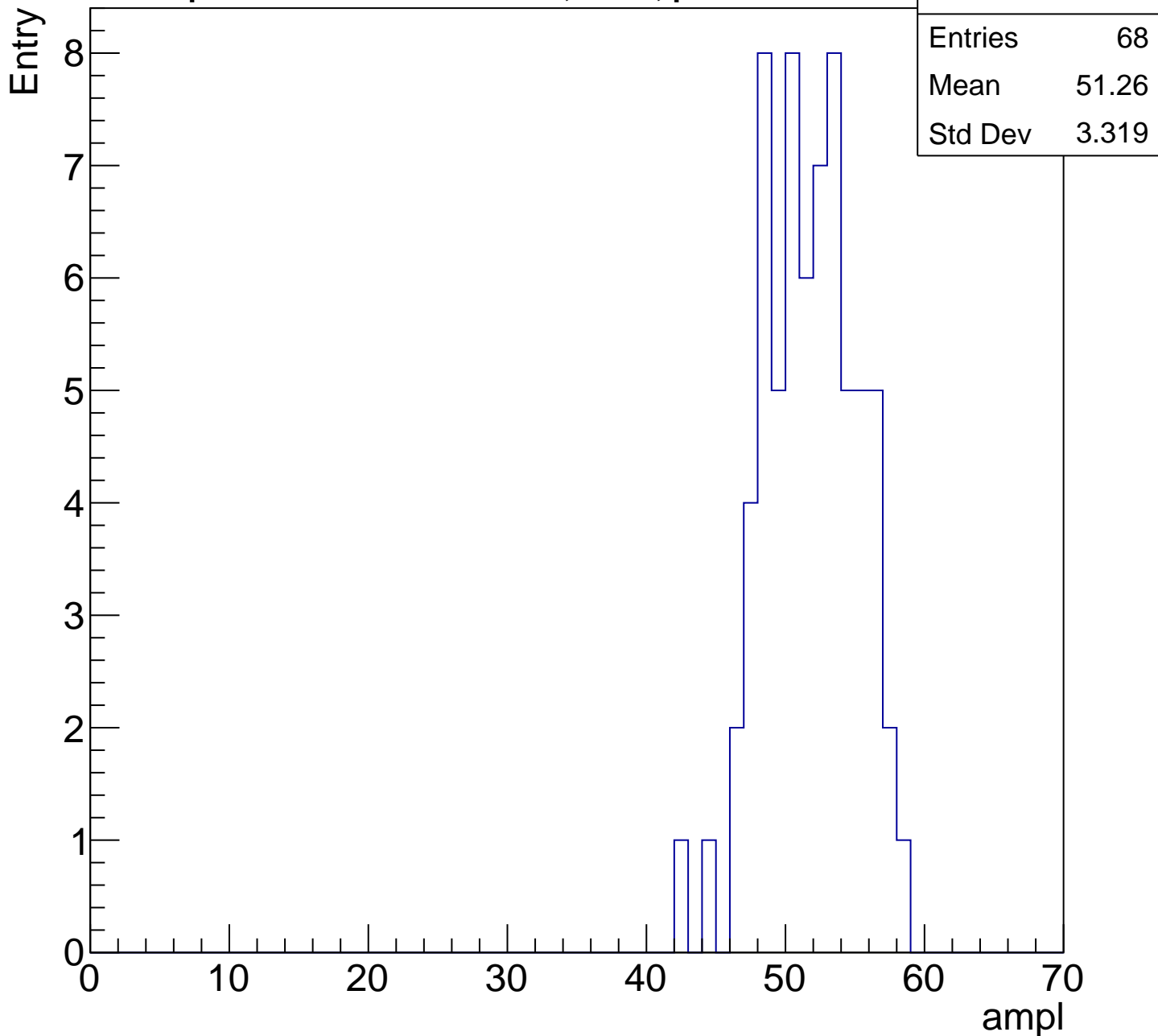
**Gaus mean : 43.4574**

**Gaus Width: 3.8264**



# B0L001S, U6-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

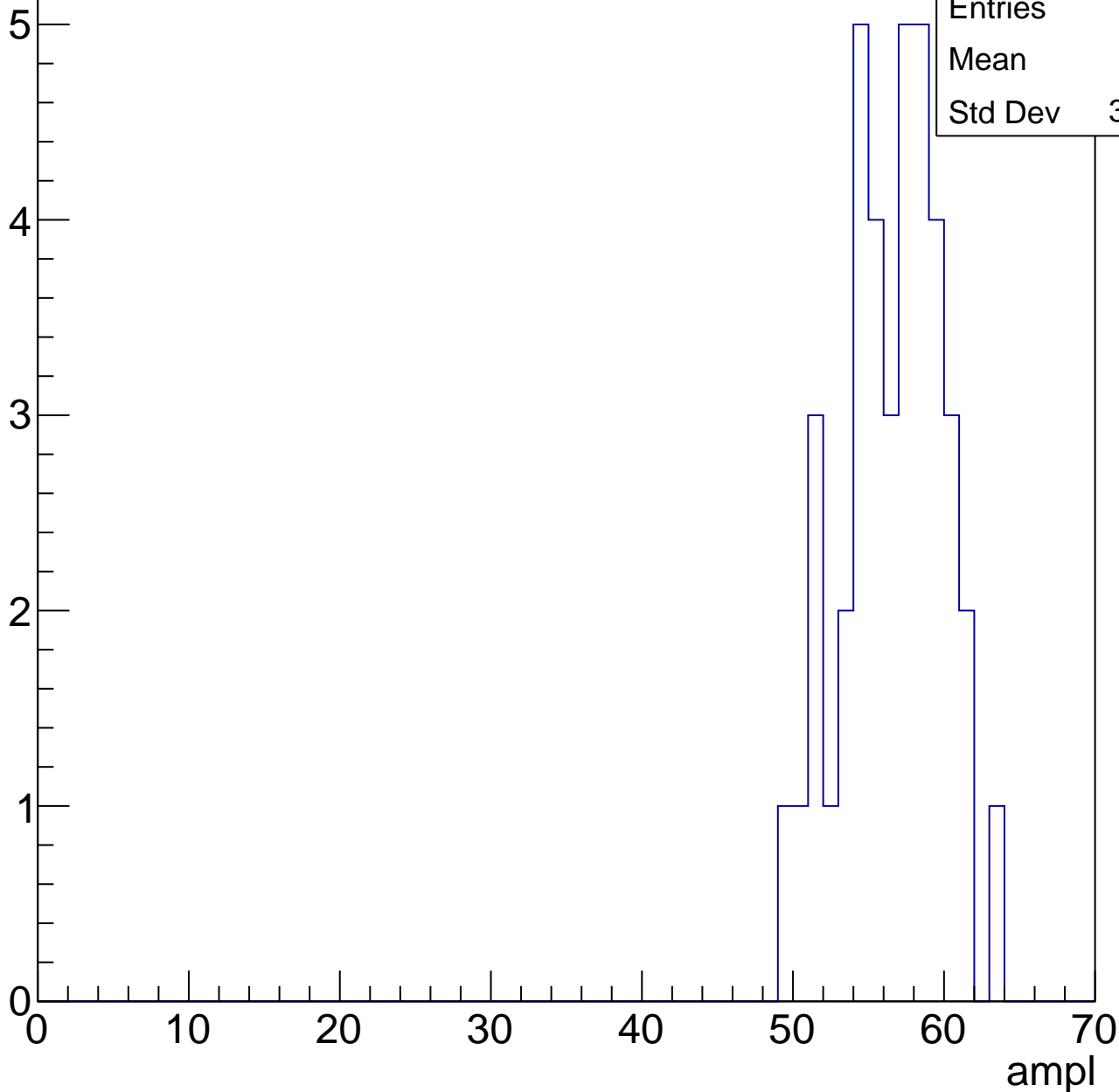


# B0L001S, U6-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	40
Mean	56.1
Std Dev	3.262

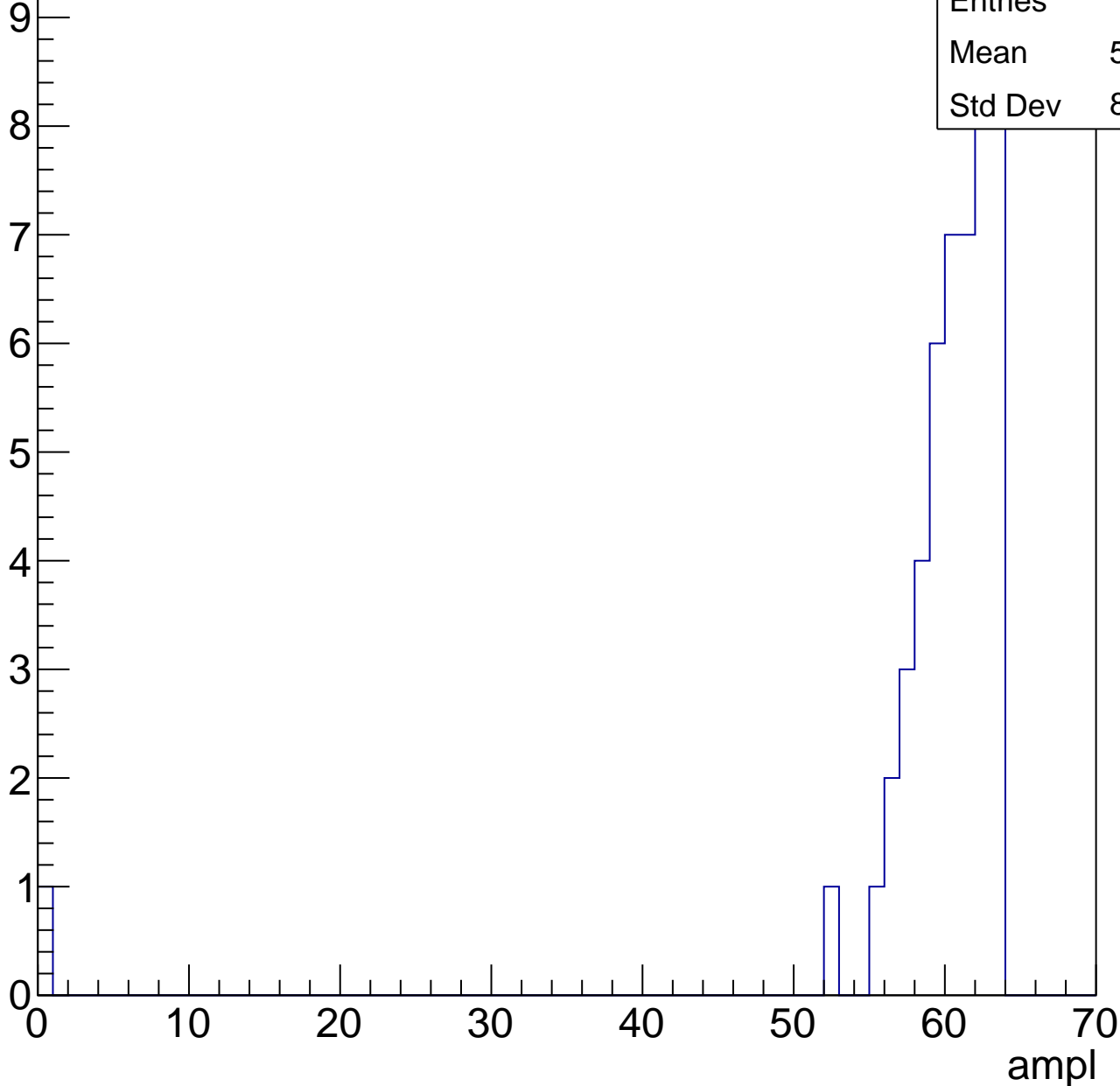


# B0L001S, U6-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	58.88
Std Dev	8.833



# B0L001S, U6-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U6-ch61, adc0

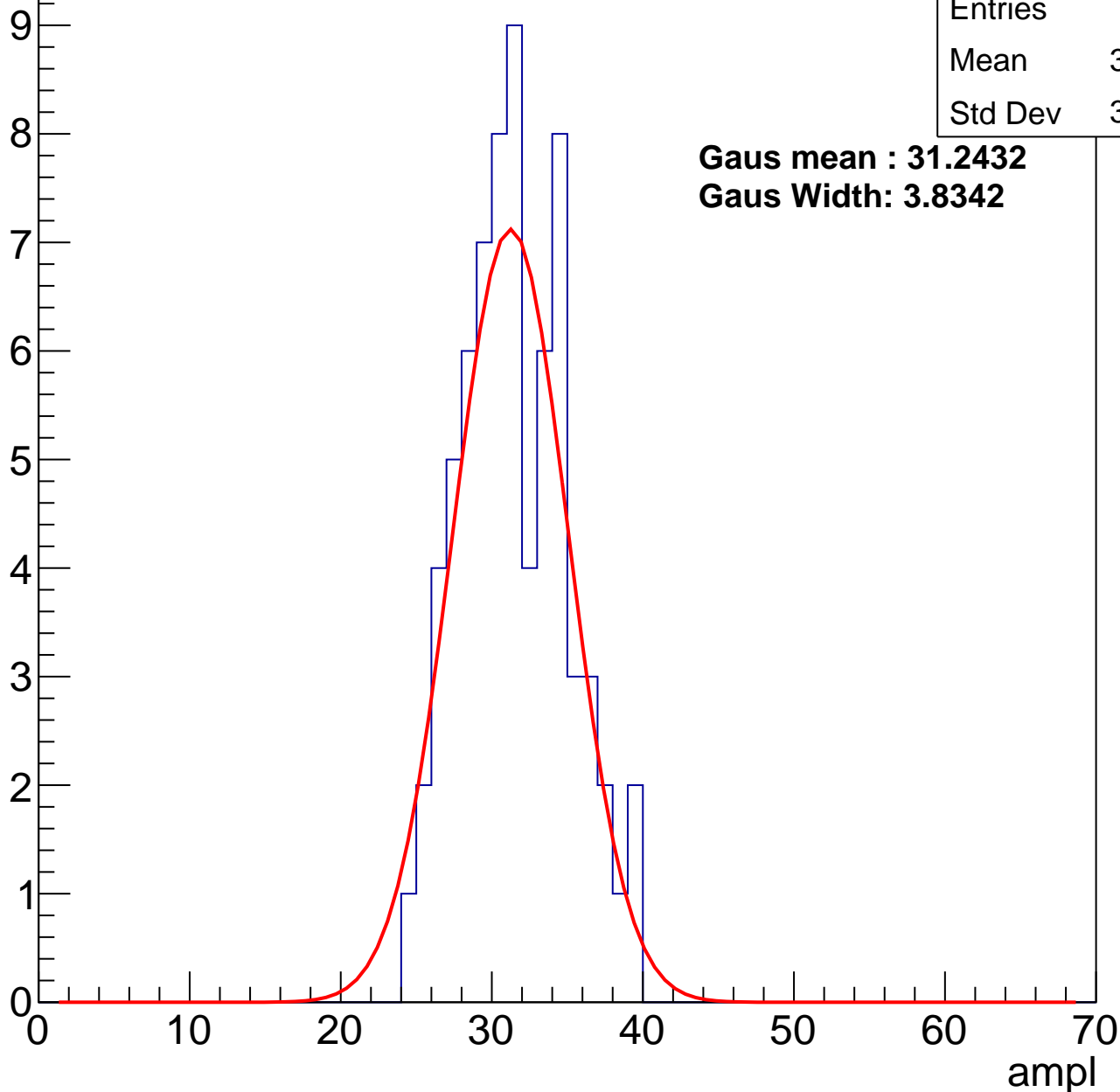
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	31.04
Std Dev	3.486

**Gaus mean : 31.2432**

**Gaus Width: 3.8342**



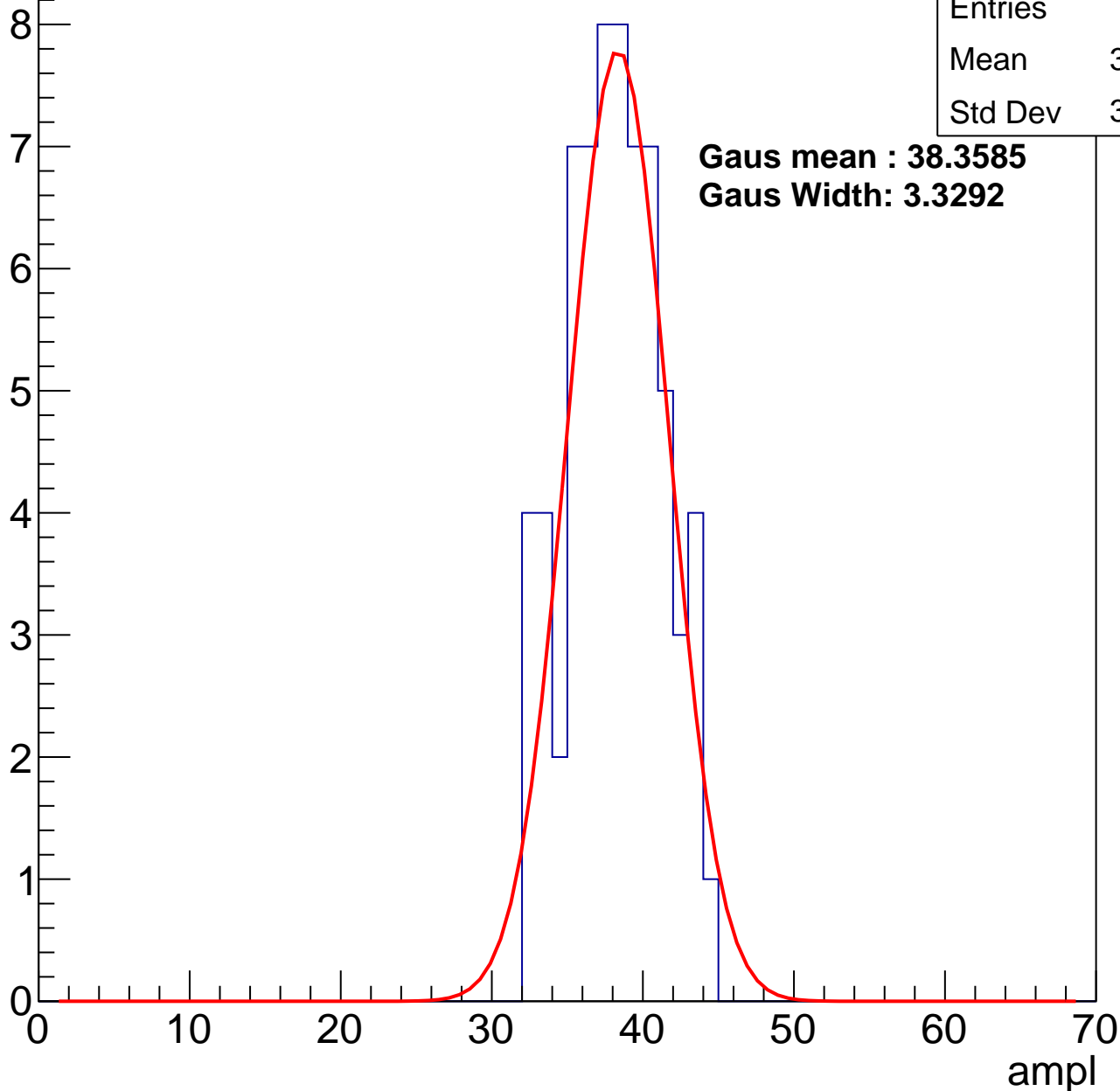
# B0L001S, U6-ch61, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	37.69
Std Dev	3.072

**Gaus mean : 38.3585**  
**Gaus Width: 3.3292**



# B0L001S, U6-ch61, adc2

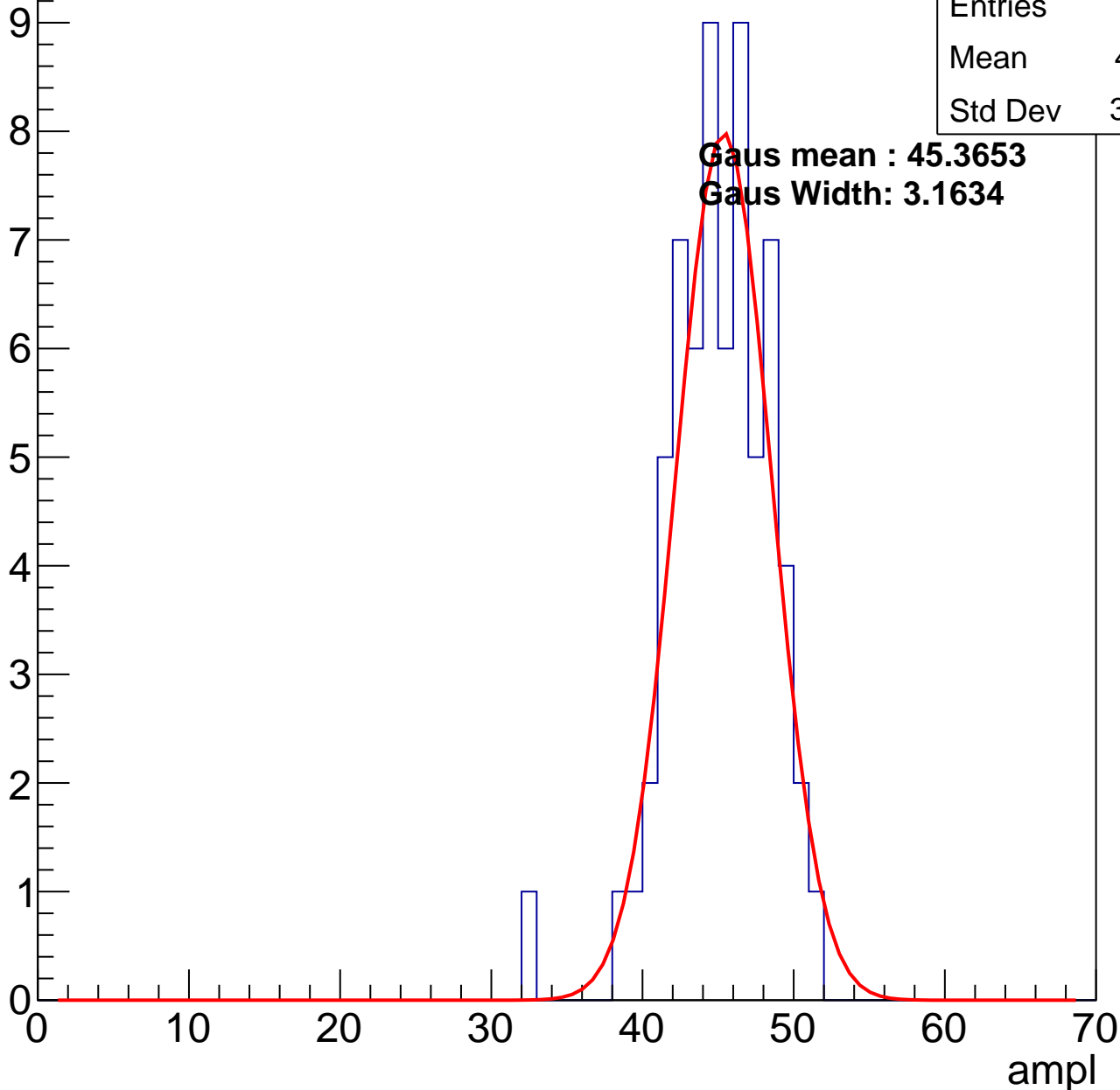
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	44.61
Std Dev	3.284

**Gaus mean : 45.3653**

**Gaus Width: 3.1634**



# B0L001S, U6-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

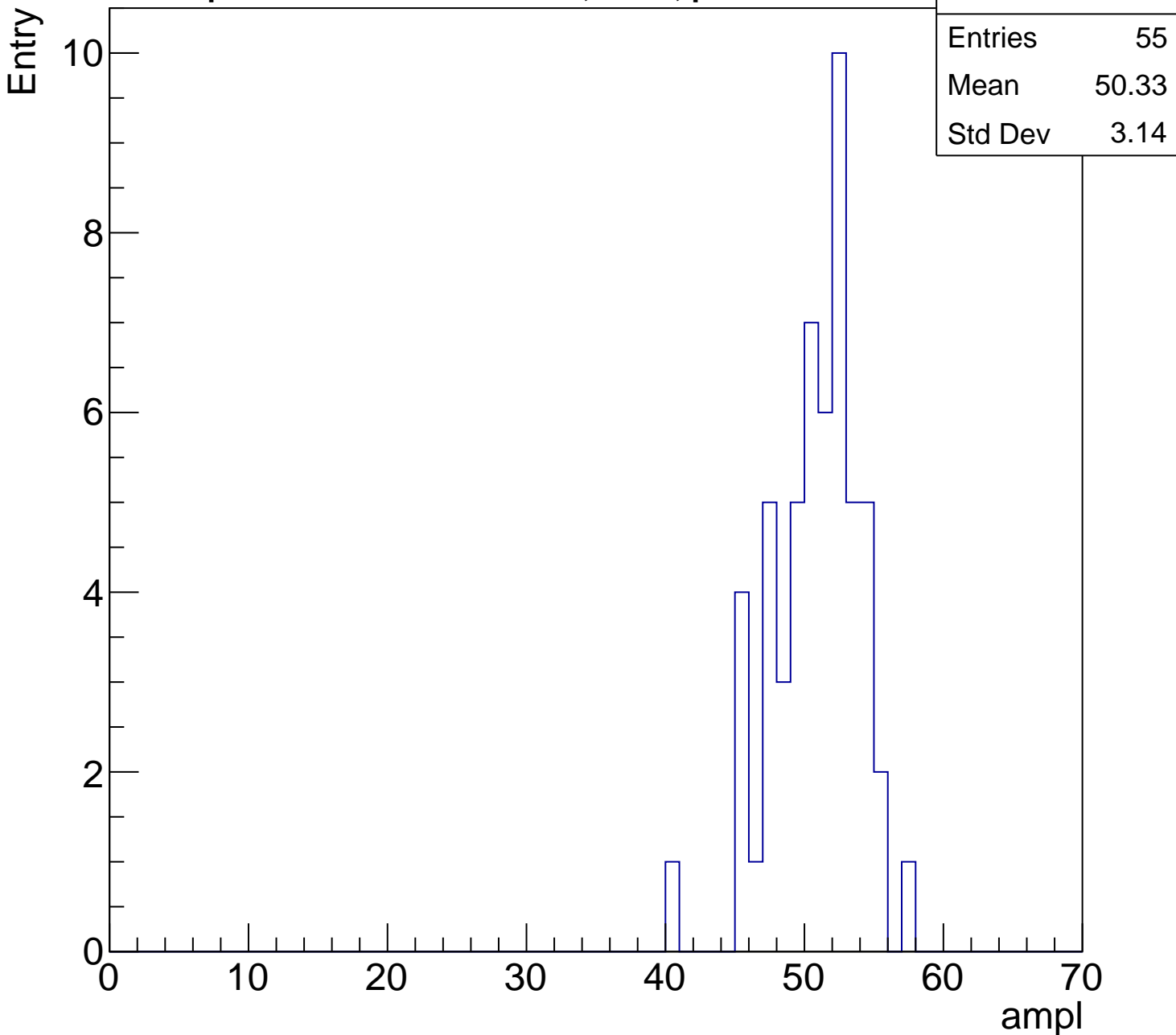
Entries	55
Mean	50.33
Std Dev	3.14

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U6-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

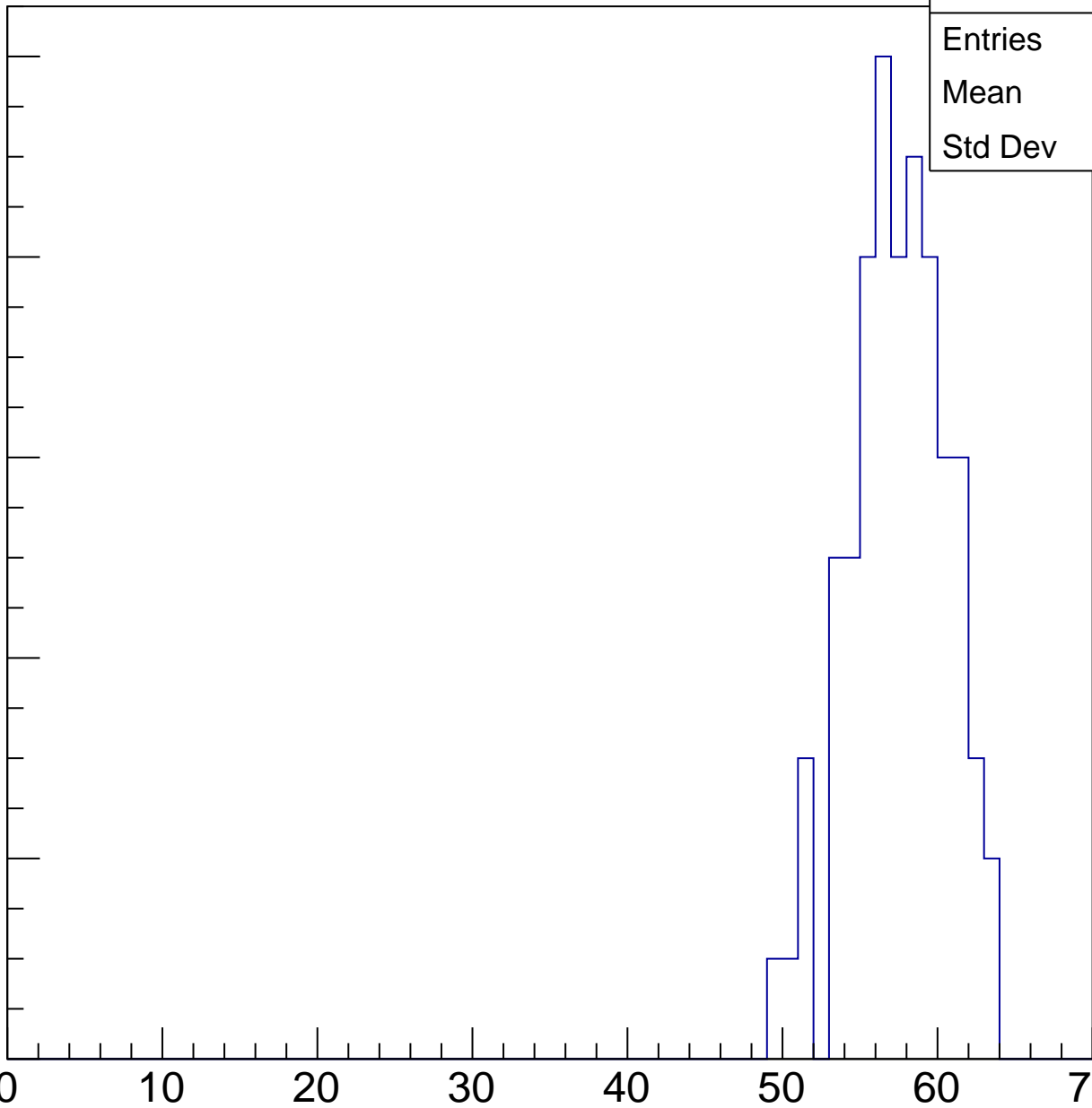
Entries	75
Mean	57
Std Dev	3.111

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

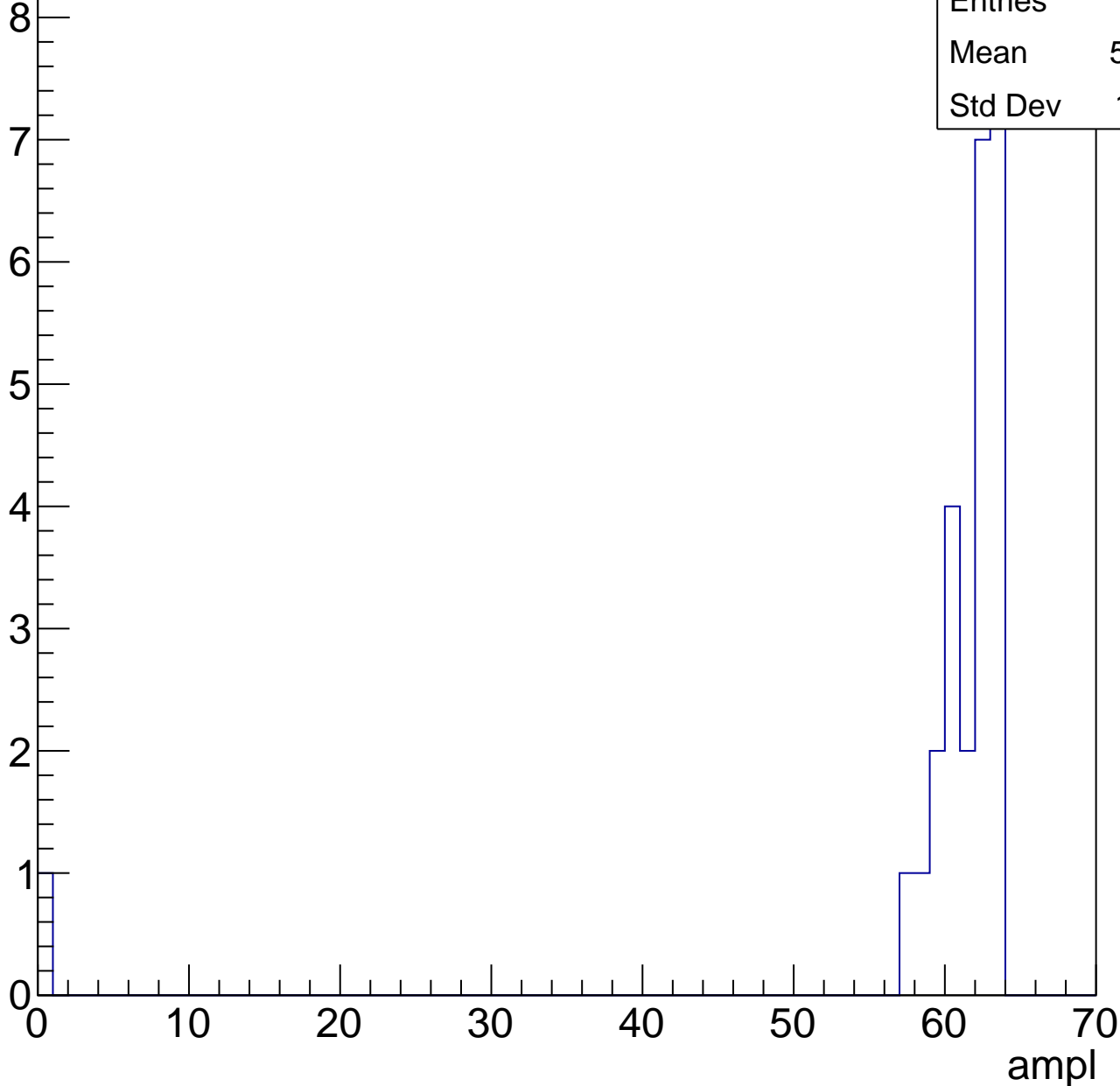


# B0L001S, U6-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

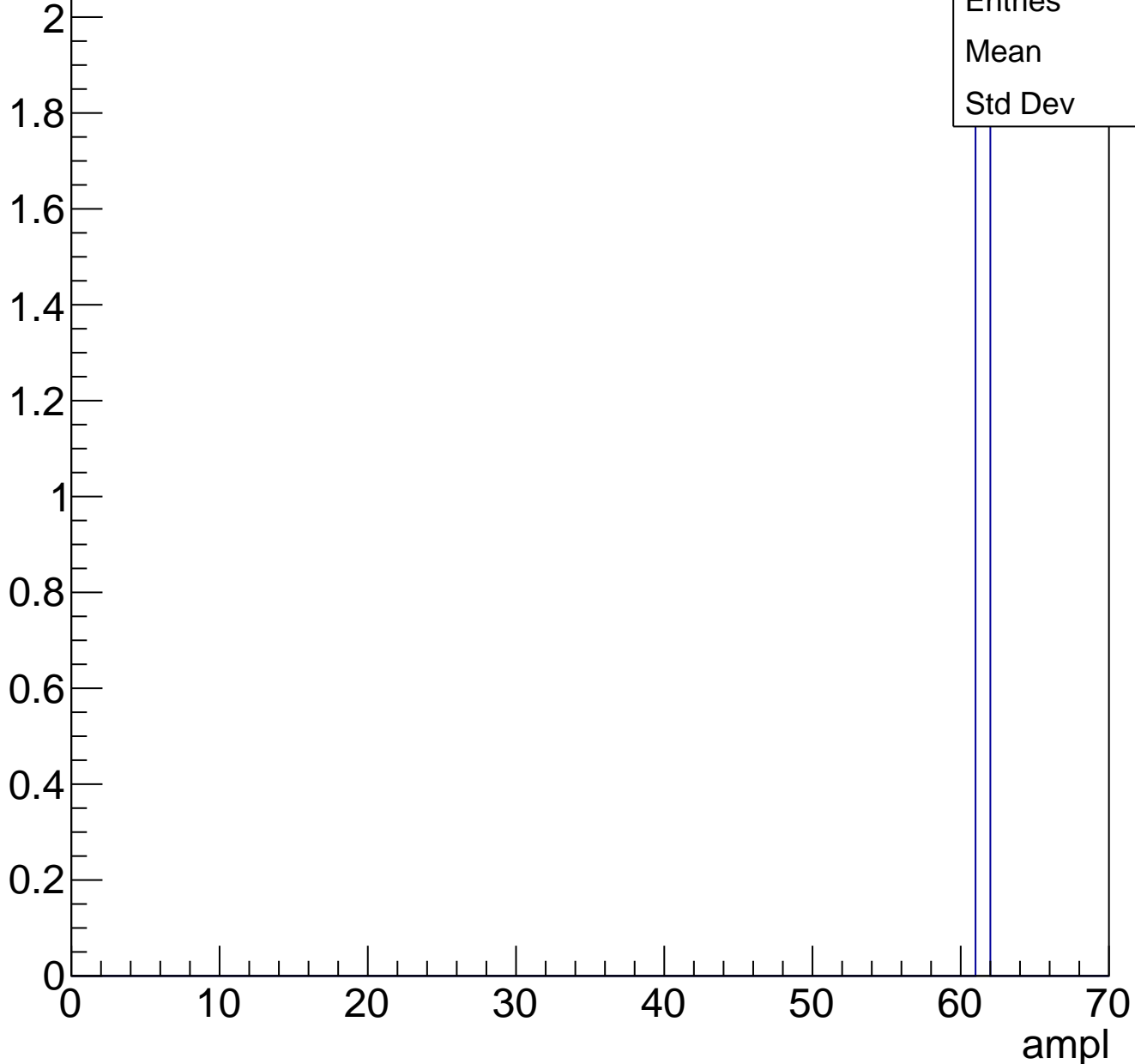
Entries	26
Mean	58.96
Std Dev	11.91



# B0L001S, U6-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch62, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	63
Mean	29.67
Std Dev	4.461

**Gaus mean : 29.2139**

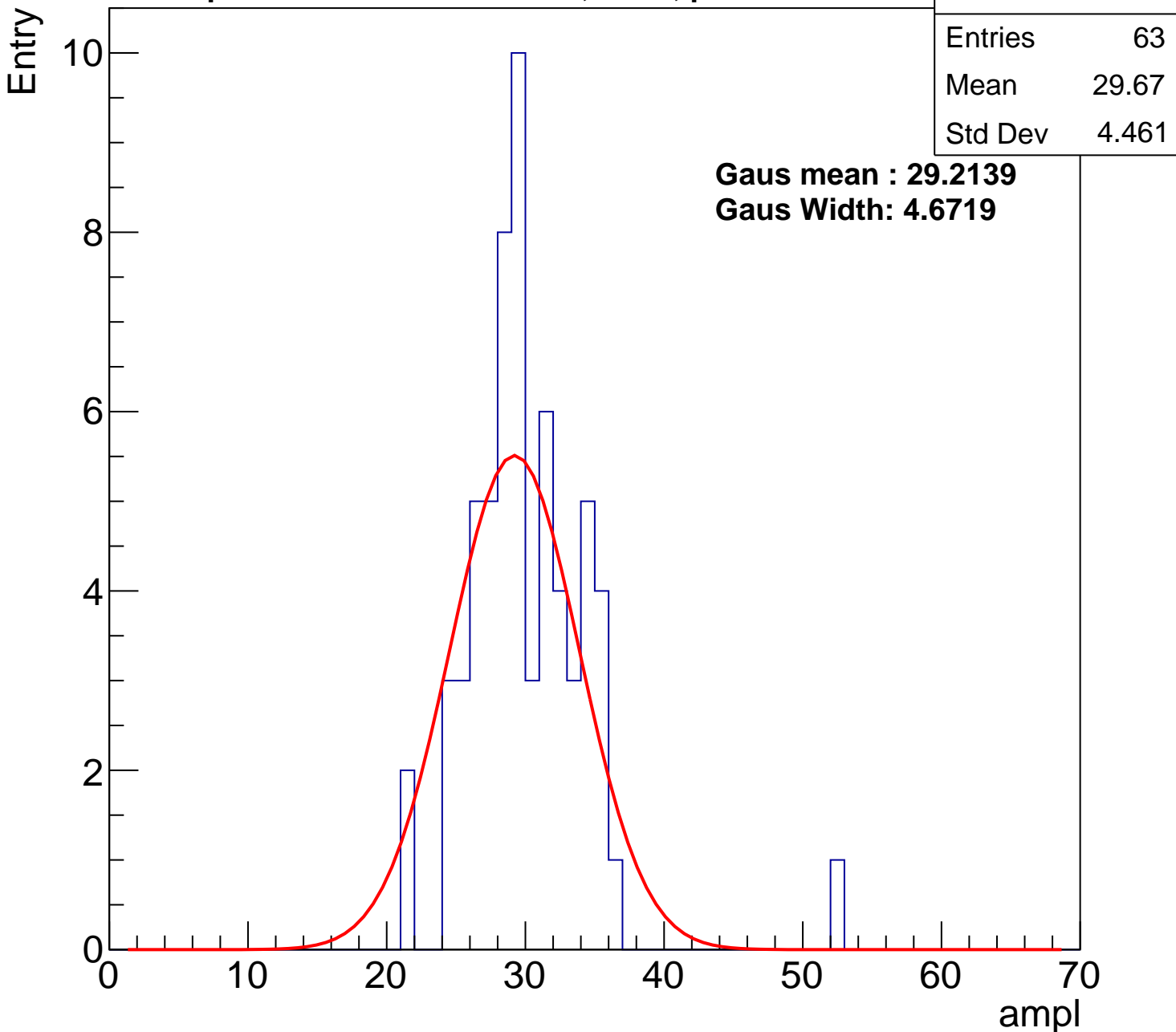
**Gaus Width: 4.6719**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U6-ch62, adc1

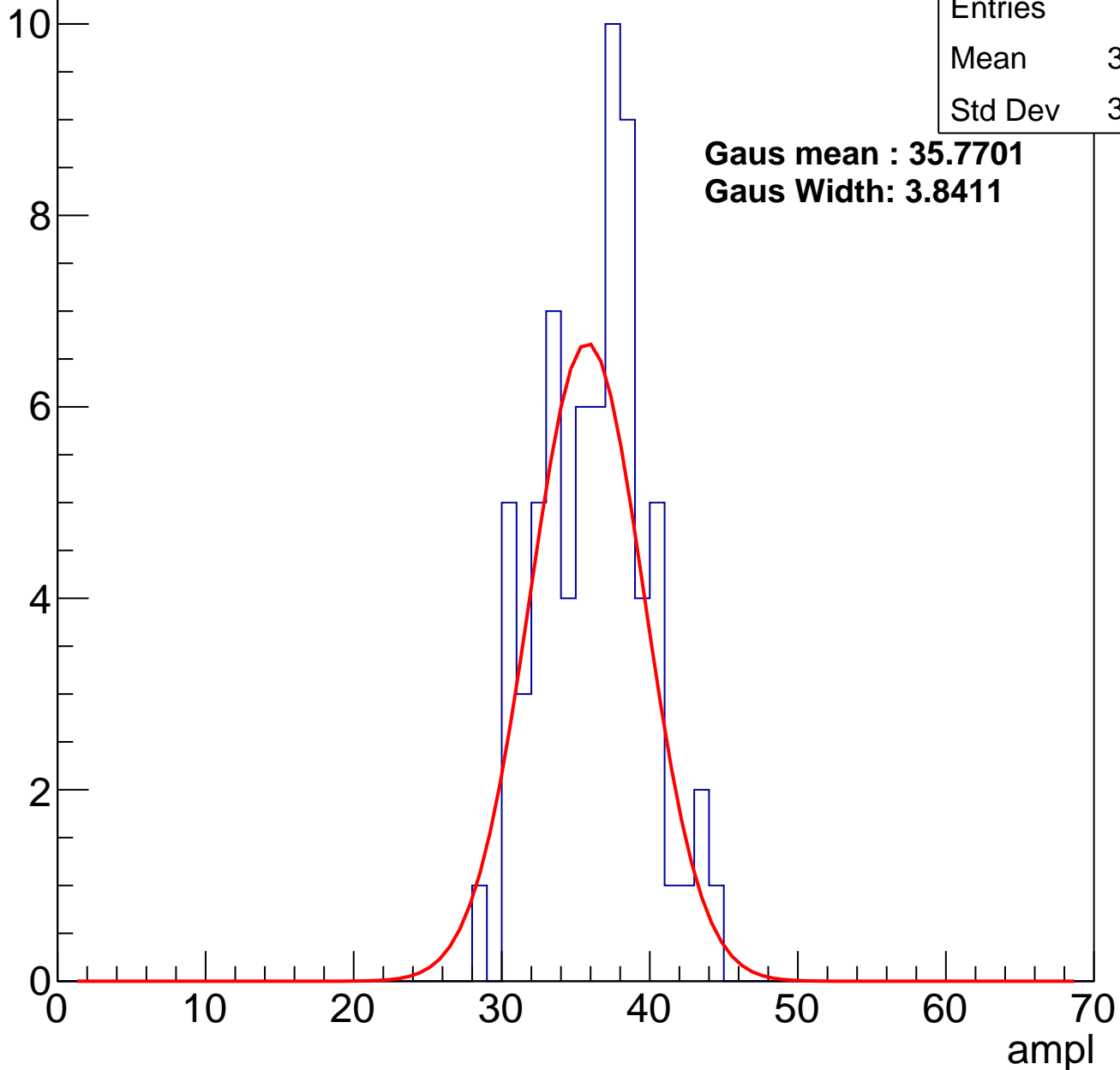
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	70
Mean	35.79
Std Dev	3.517

**Gaus mean : 35.7701**

**Gaus Width: 3.8411**

Entry



# B0L001S, U6-ch62, adc2

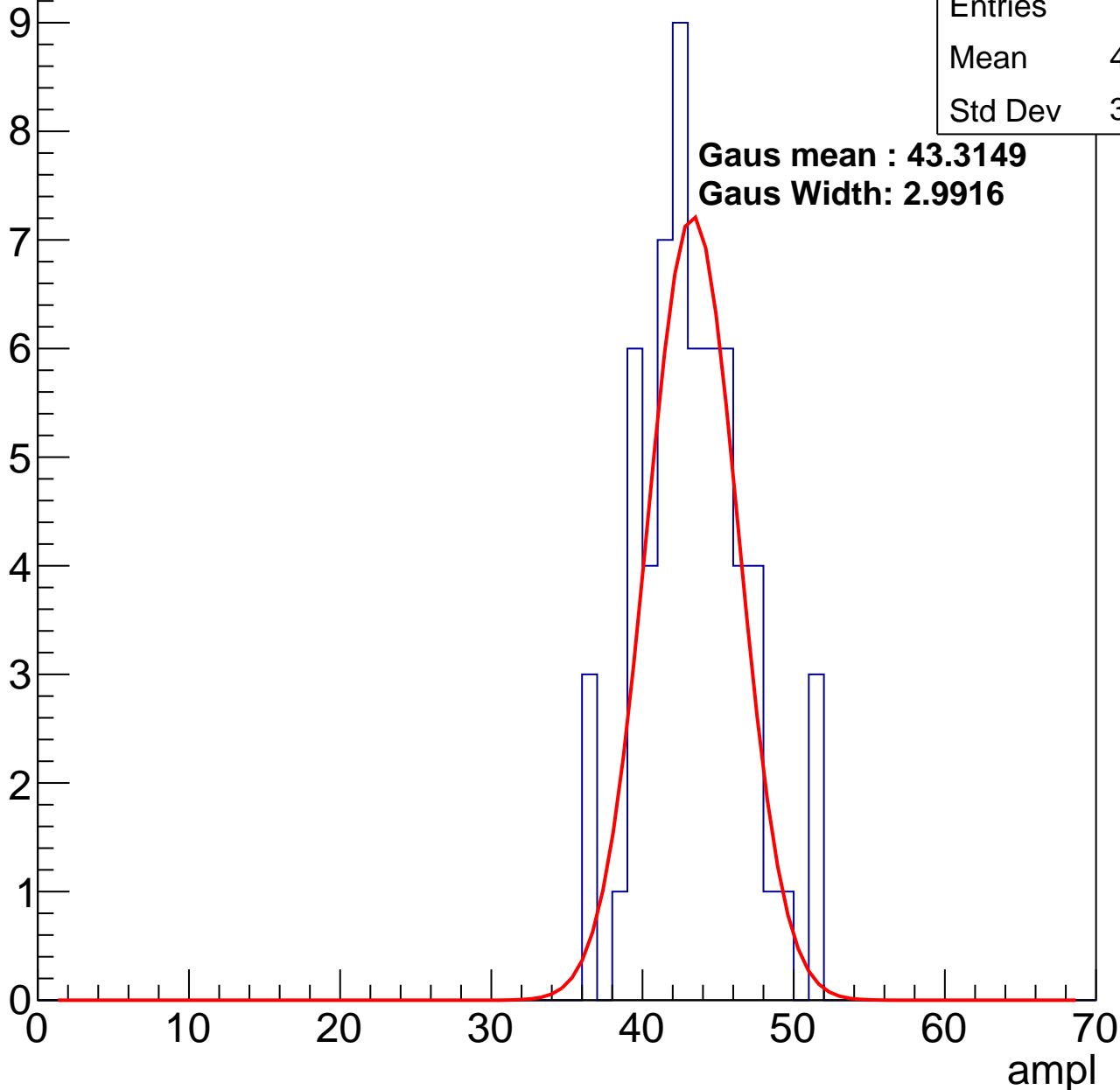
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	42.93
Std Dev	3.444

**Gaus mean : 43.3149**

**Gaus Width: 2.9916**

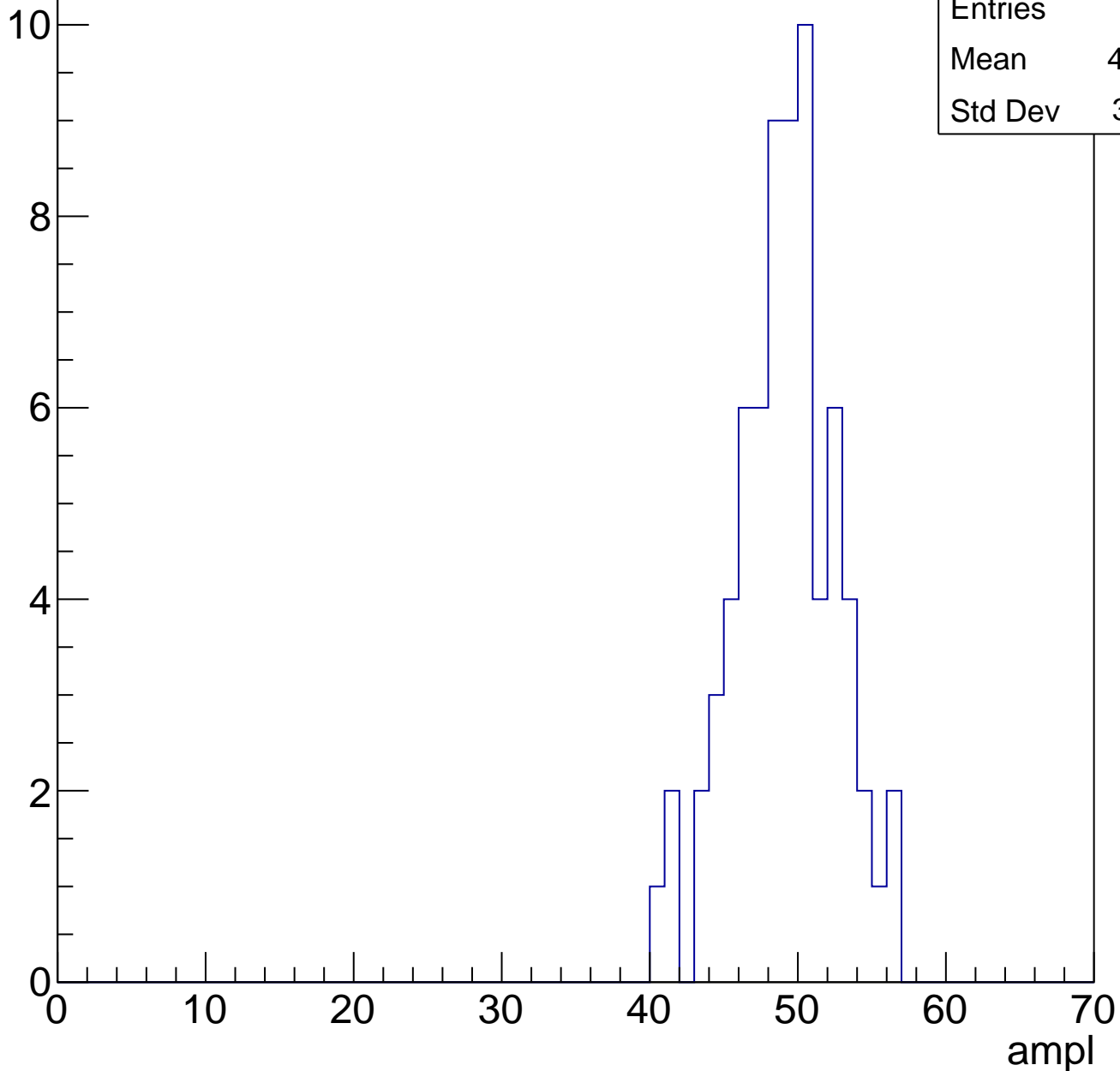


# B0L001S, U6-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	71
Mean	48.65
Std Dev	3.411

Entry

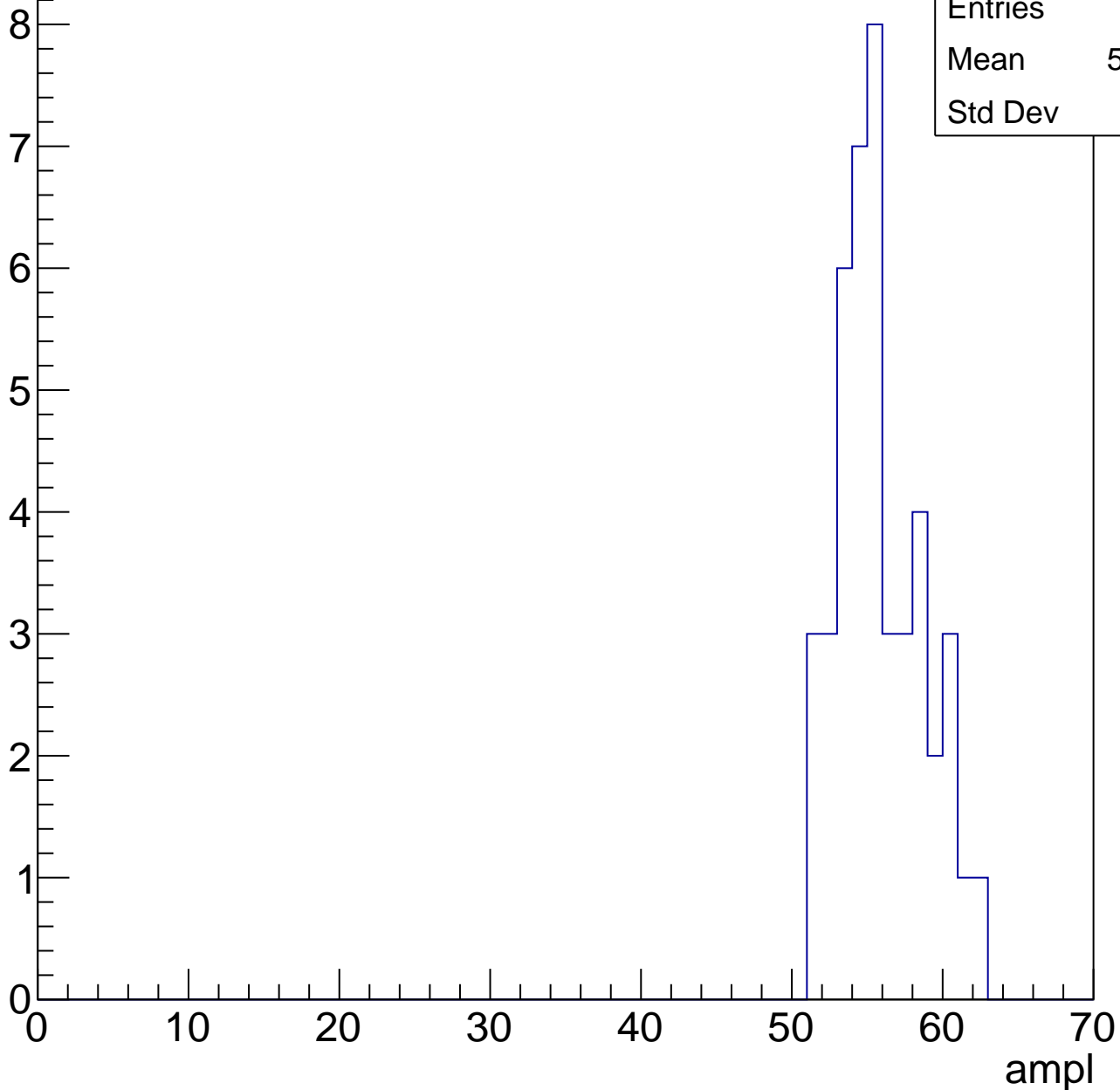


# B0L001S, U6-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

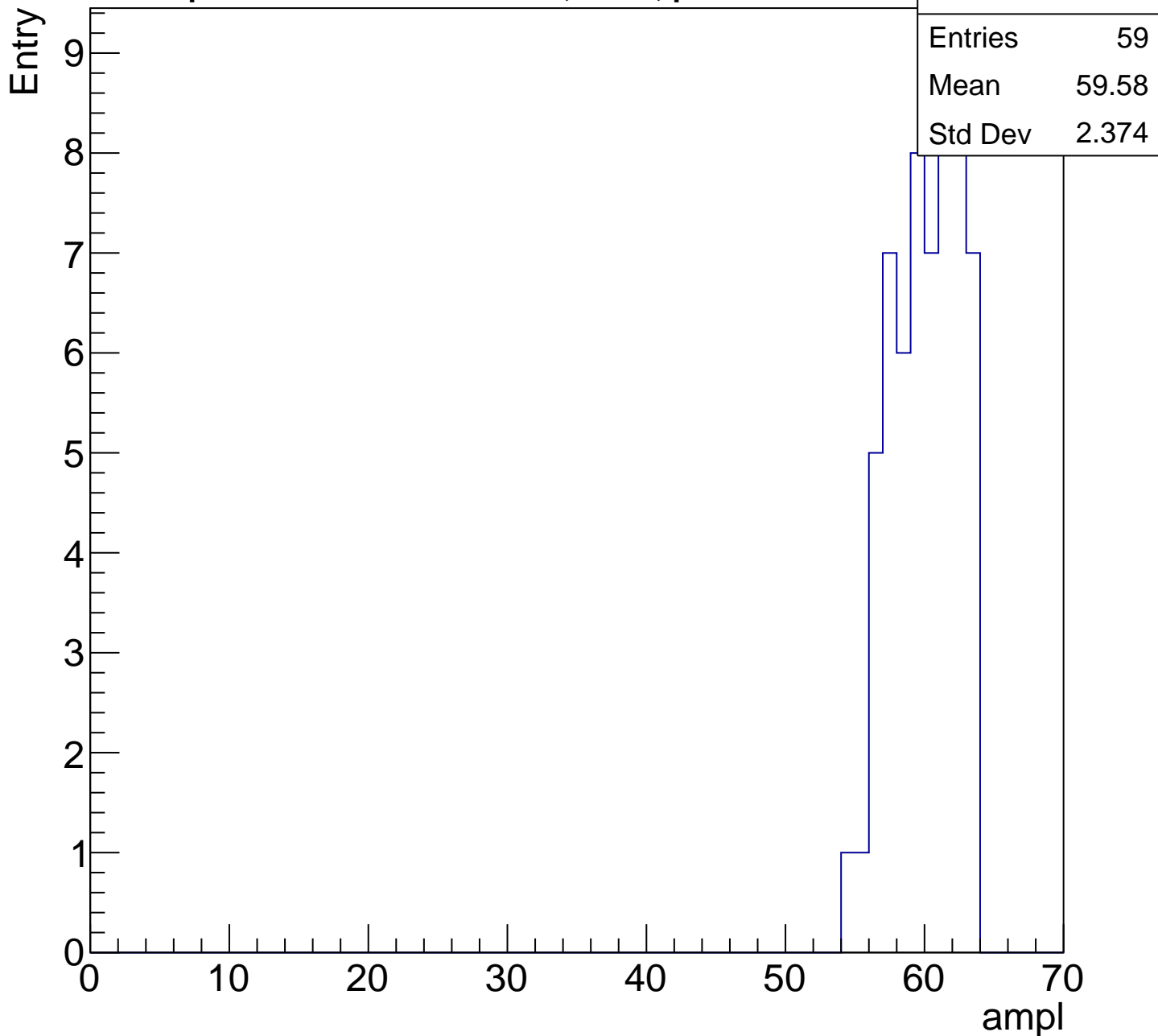
Entry

Entries	44
Mean	55.39
Std Dev	2.79



# B0L001S, U6-ch62, adc5

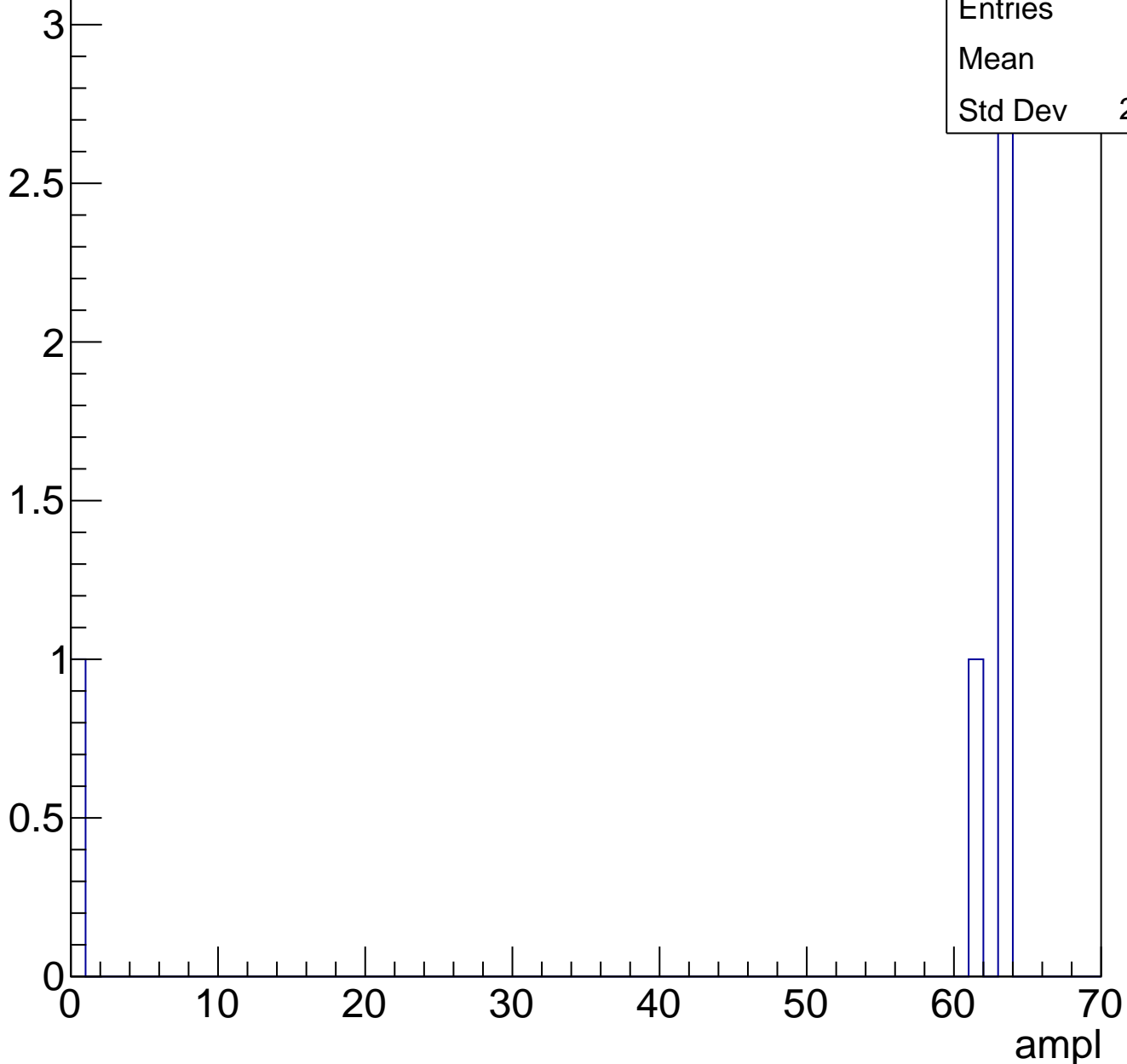
calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U6-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch63, adc0

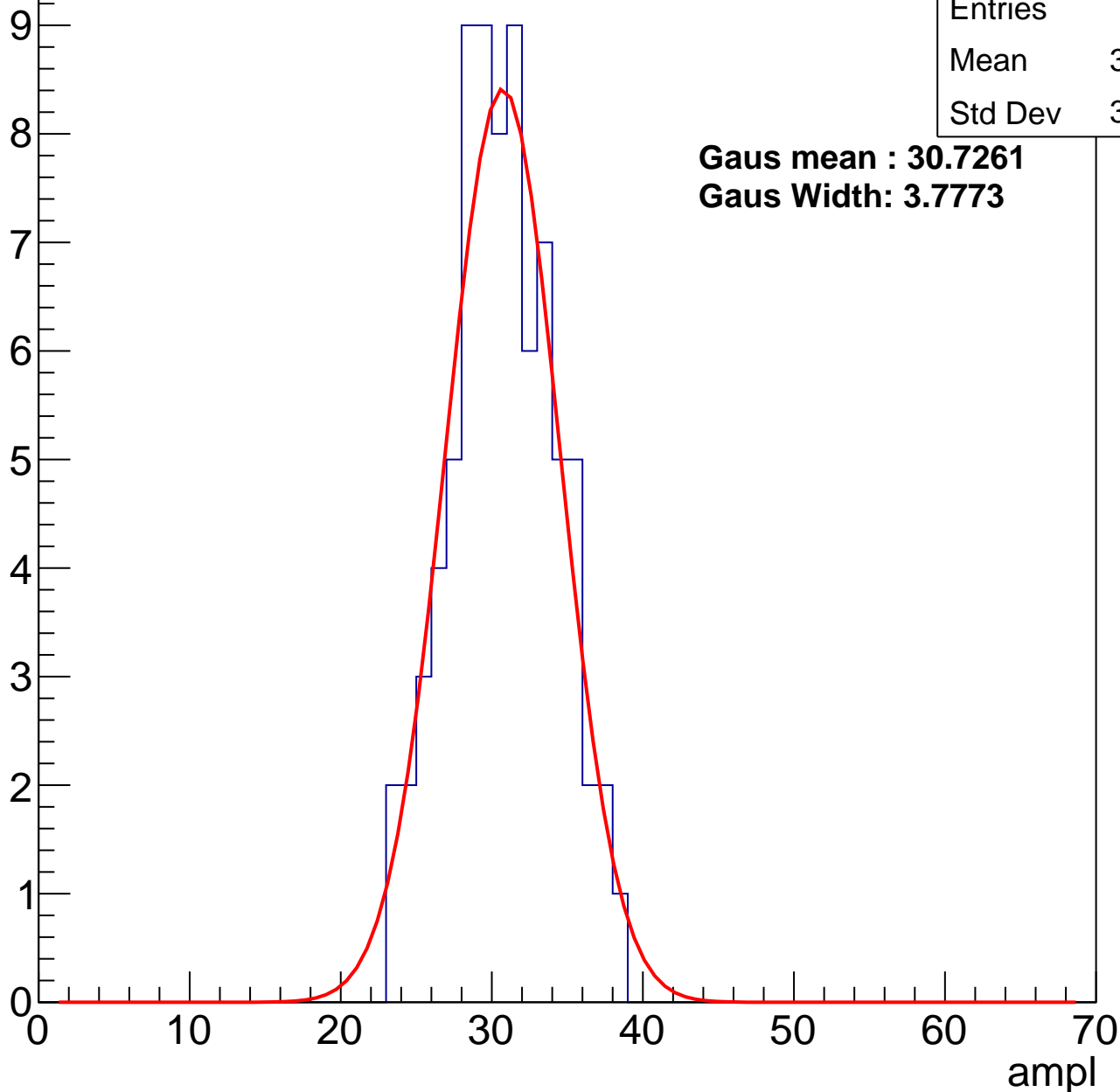
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	30.28
Std Dev	3.427

**Gaus mean : 30.7261**

**Gaus Width: 3.7773**



# B0L001S, U6-ch63, adc1

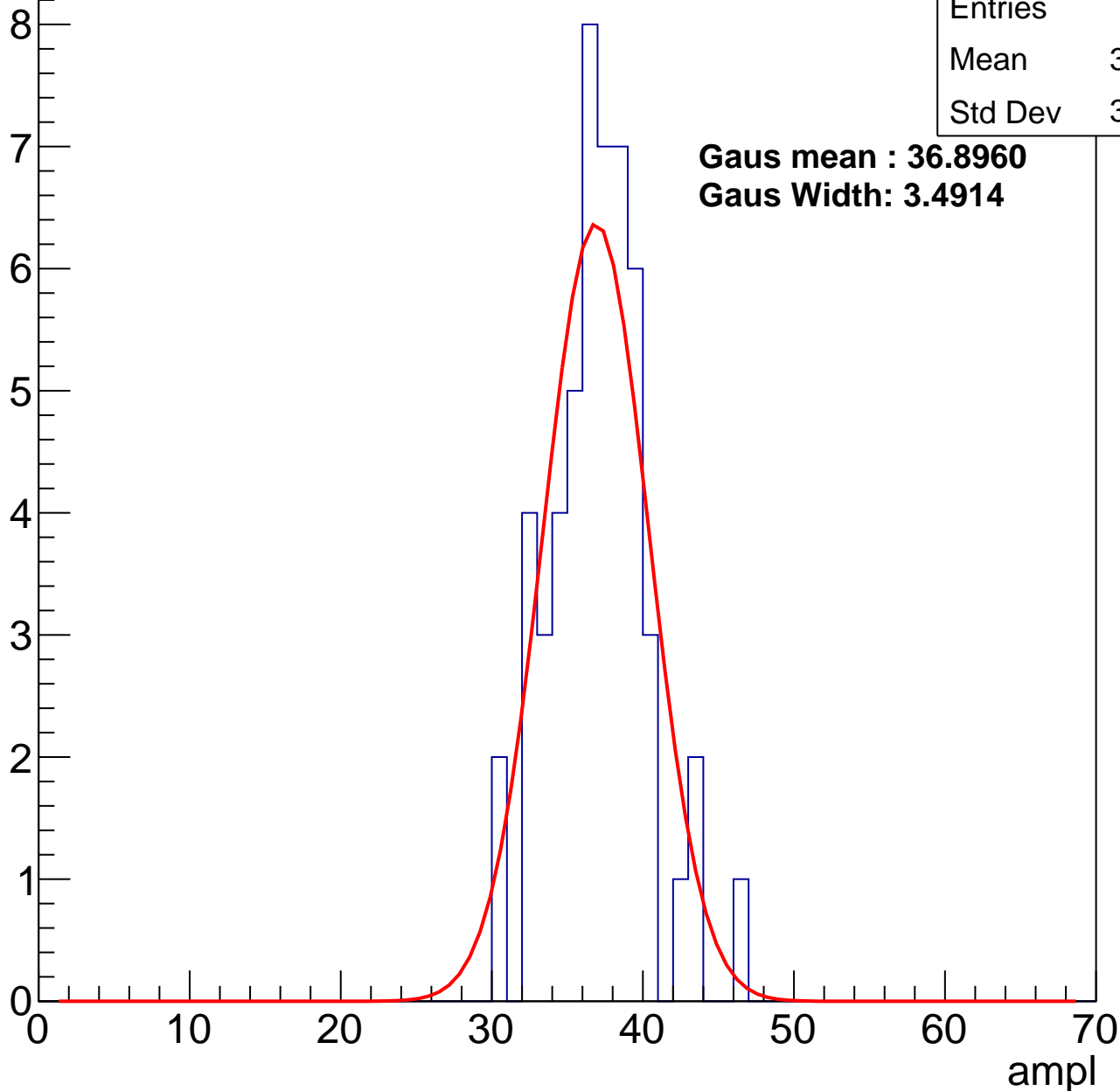
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	36.58
Std Dev	3.183

**Gaus mean : 36.8960**

**Gaus Width: 3.4914**



# B0L001S, U6-ch63, adc2

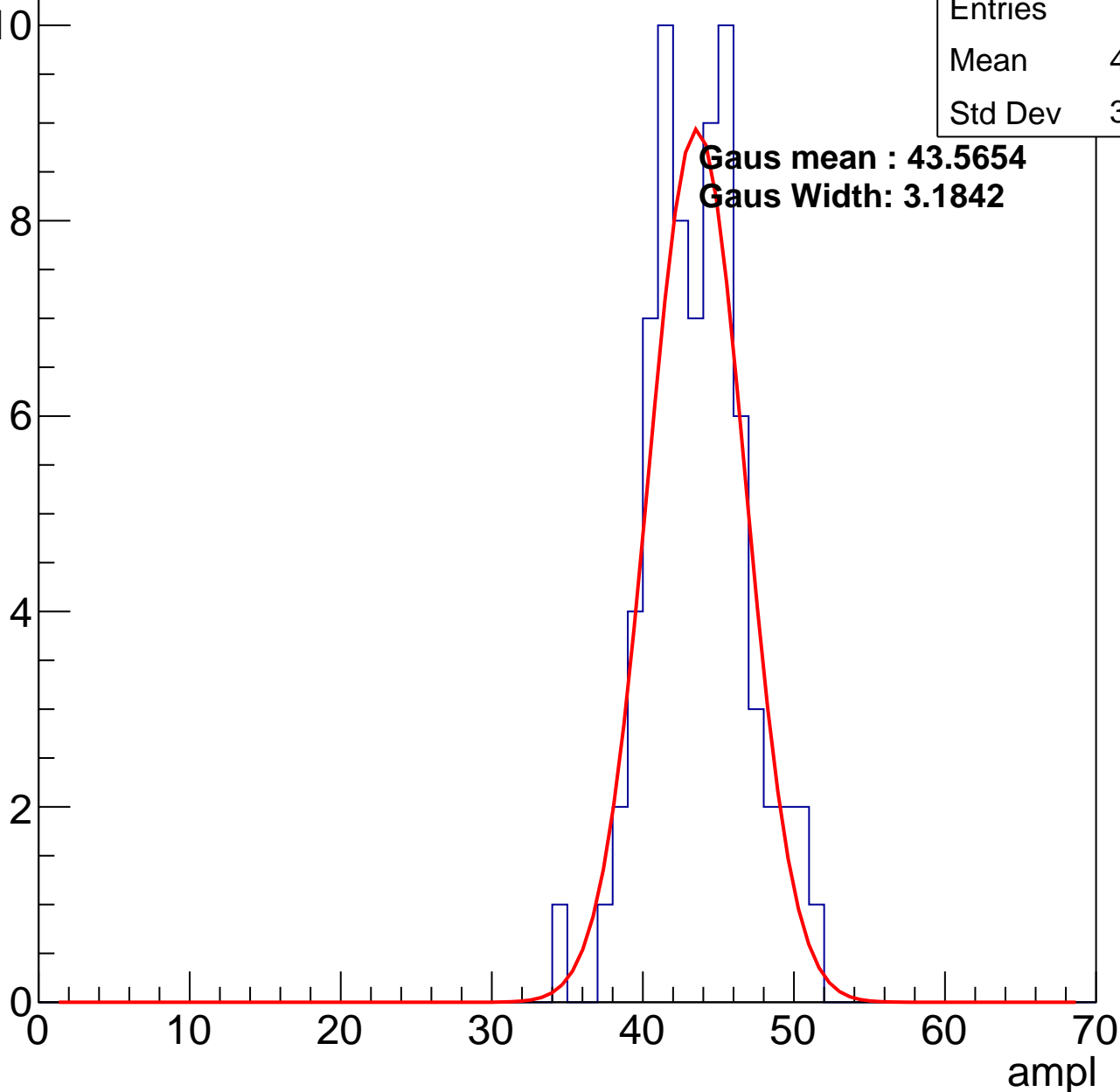
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	43.17
Std Dev	3.214

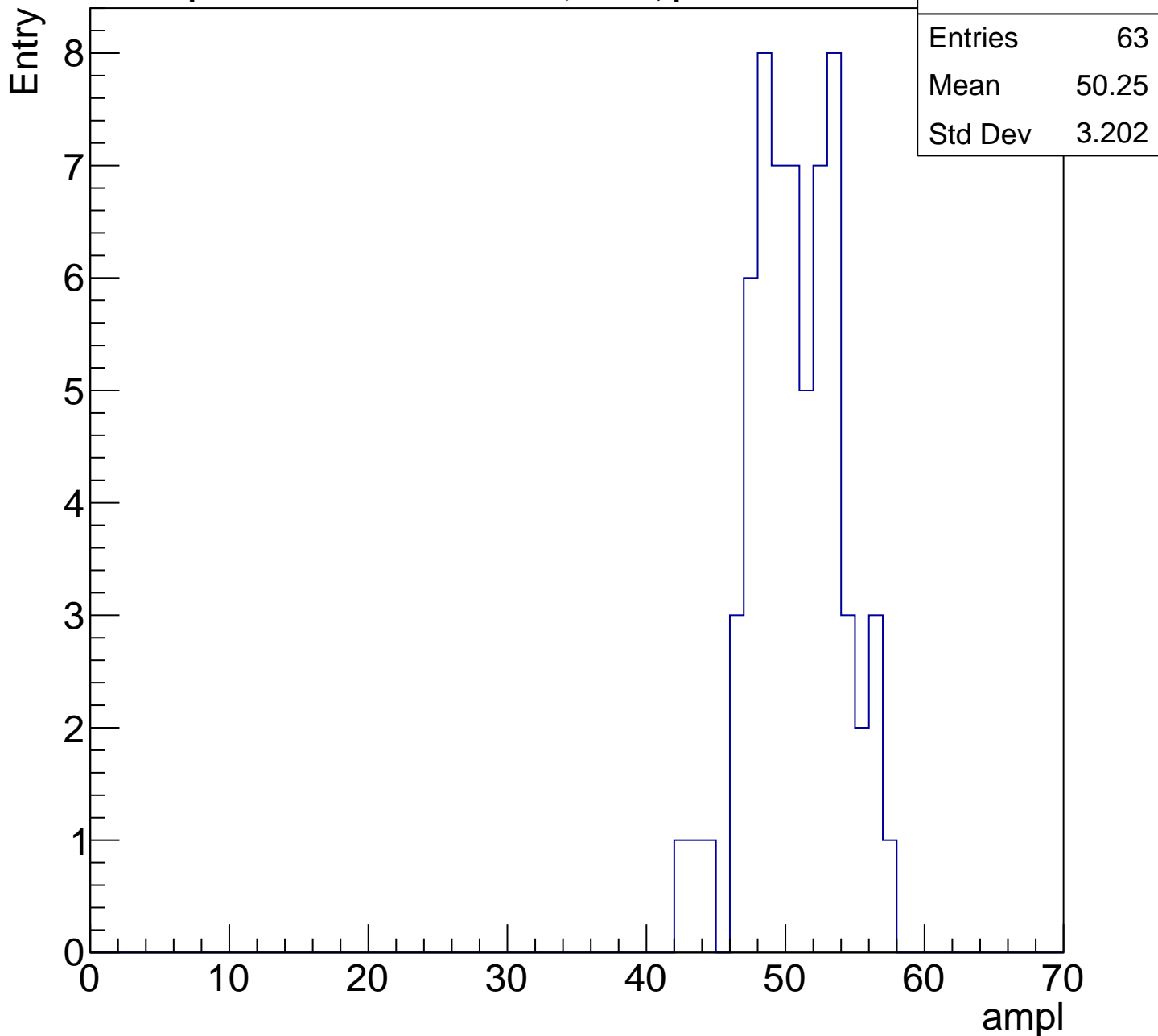
**Gaus mean : 43.5654**

**Gaus Width: 3.1842**



# B0L001S, U6-ch63, adc3

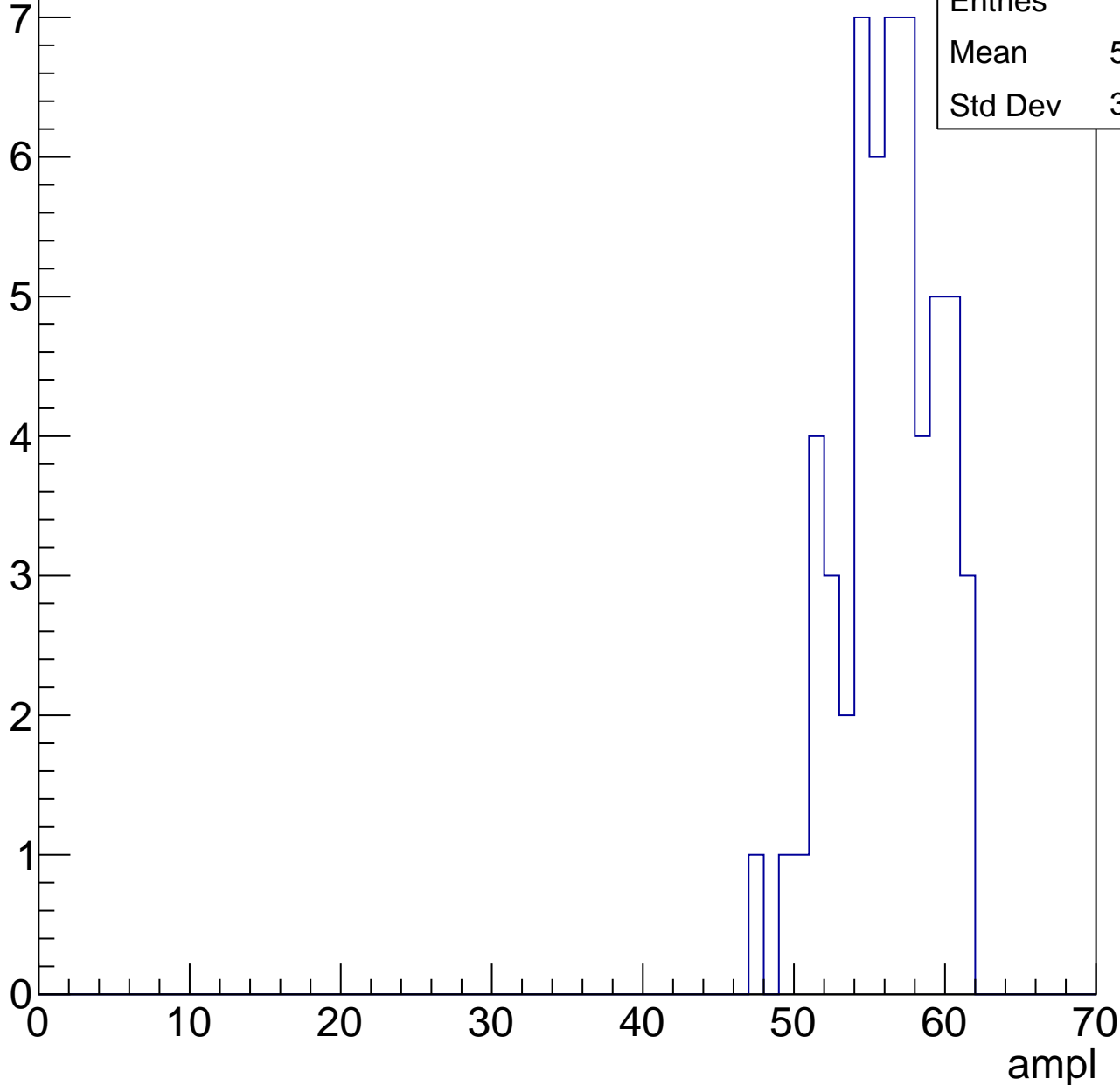
calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U6-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



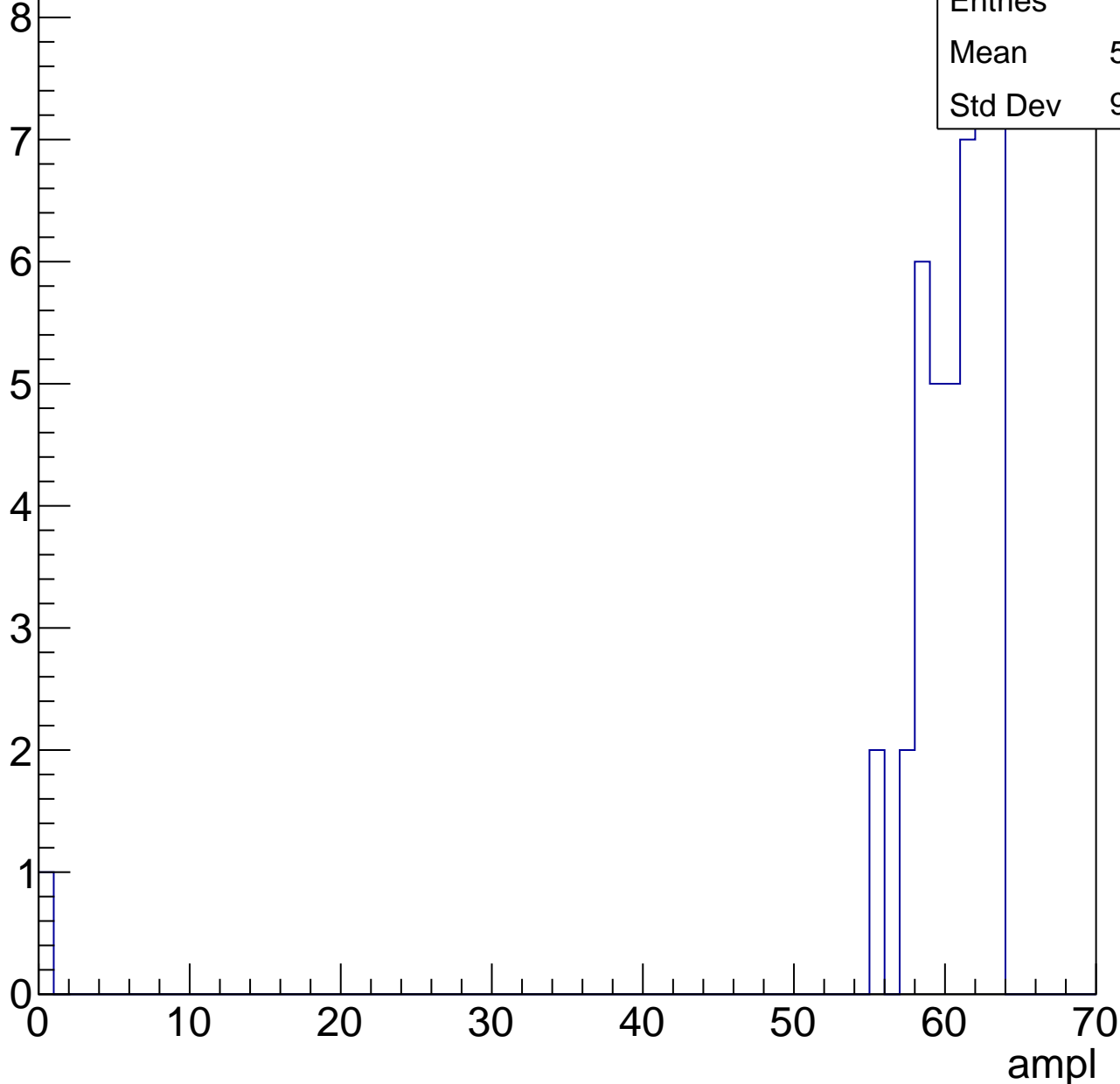
Entries	56
Mean	55.73
Std Dev	3.232

# B0L001S, U6-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	44
Mean	58.95
Std Dev	9.244



# B0L001S, U6-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch64, adc0

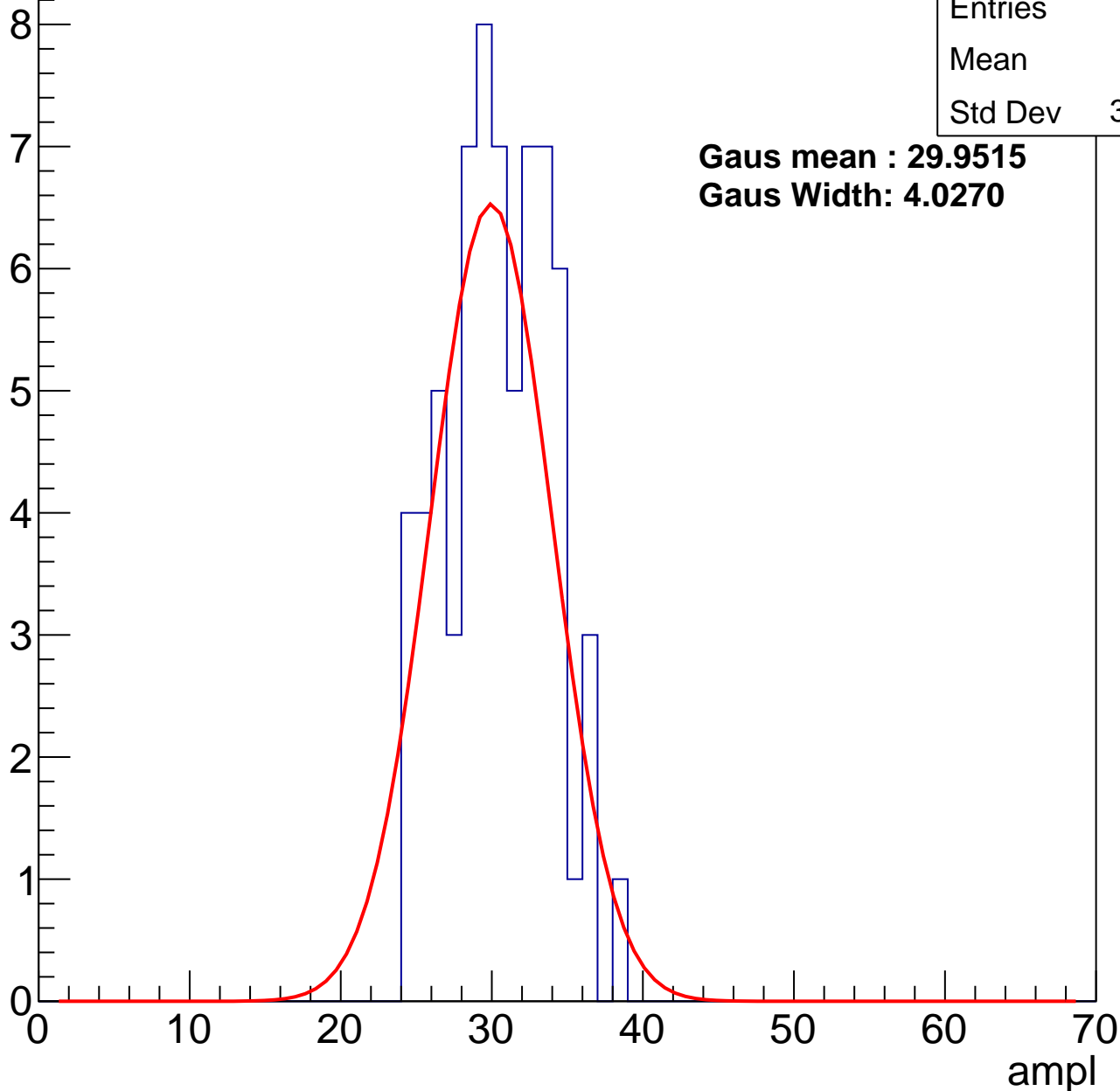
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	30
Std Dev	3.378

**Gaus mean : 29.9515**

**Gaus Width: 4.0270**



# B0L001S, U6-ch64, adc1

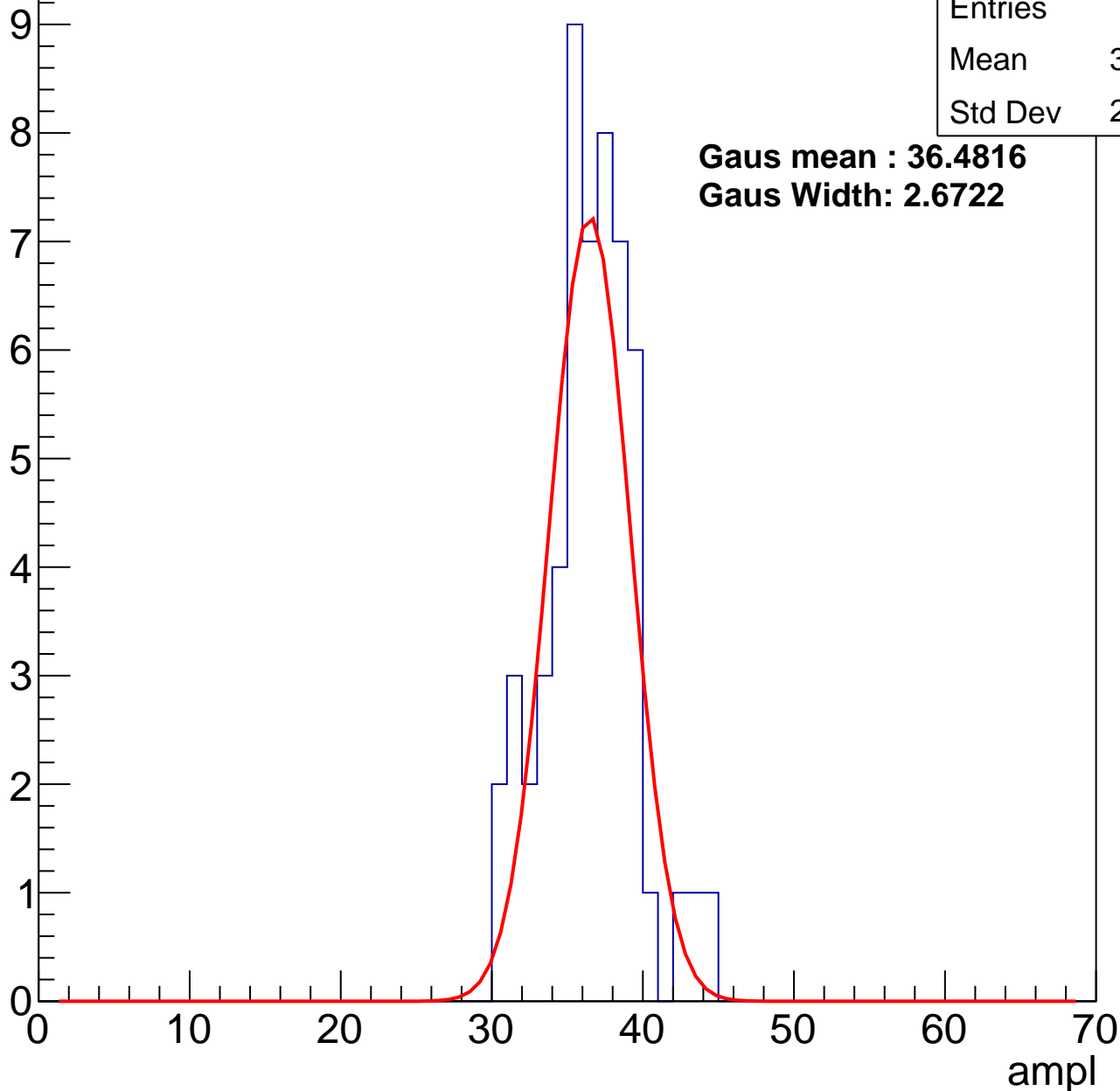
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	36.07
Std Dev	2.972

**Gaus mean : 36.4816**

**Gaus Width: 2.6722**



# B0L001S, U6-ch64, adc2

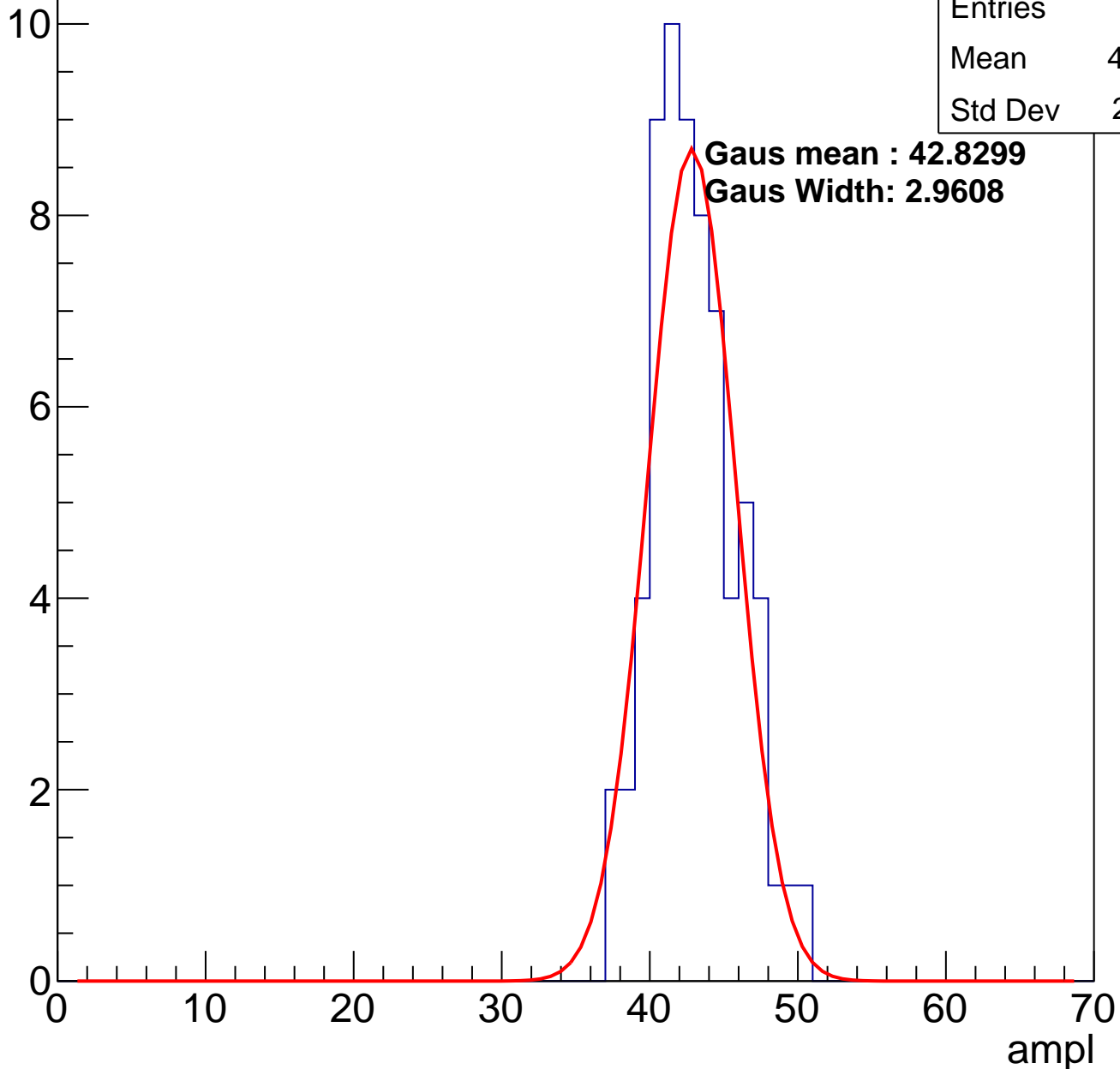
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	67
Mean	42.55
Std Dev	2.851

**Gaus mean : 42.8299**

**Gaus Width: 2.9608**

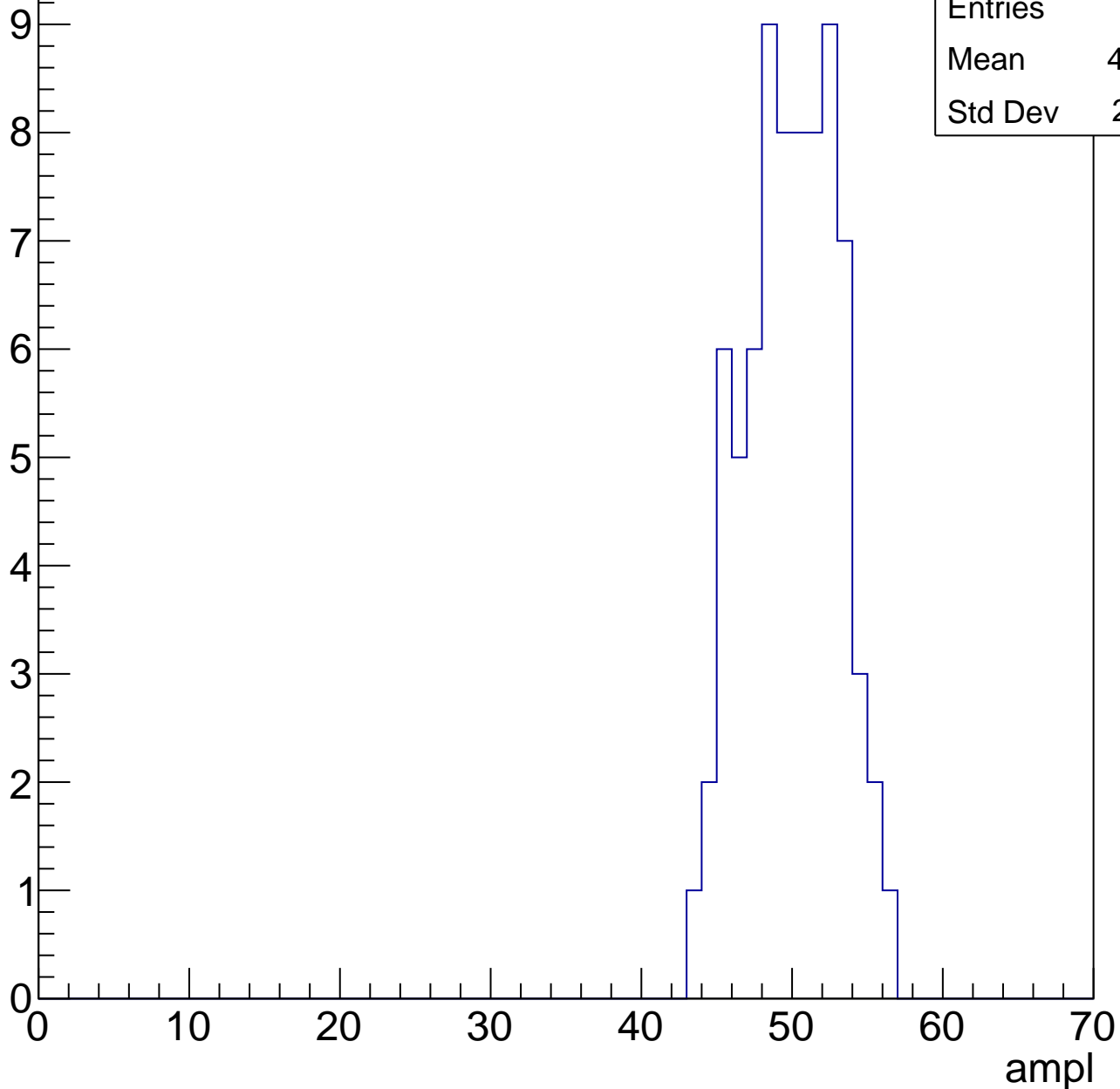
Entry



# B0L001S, U6-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



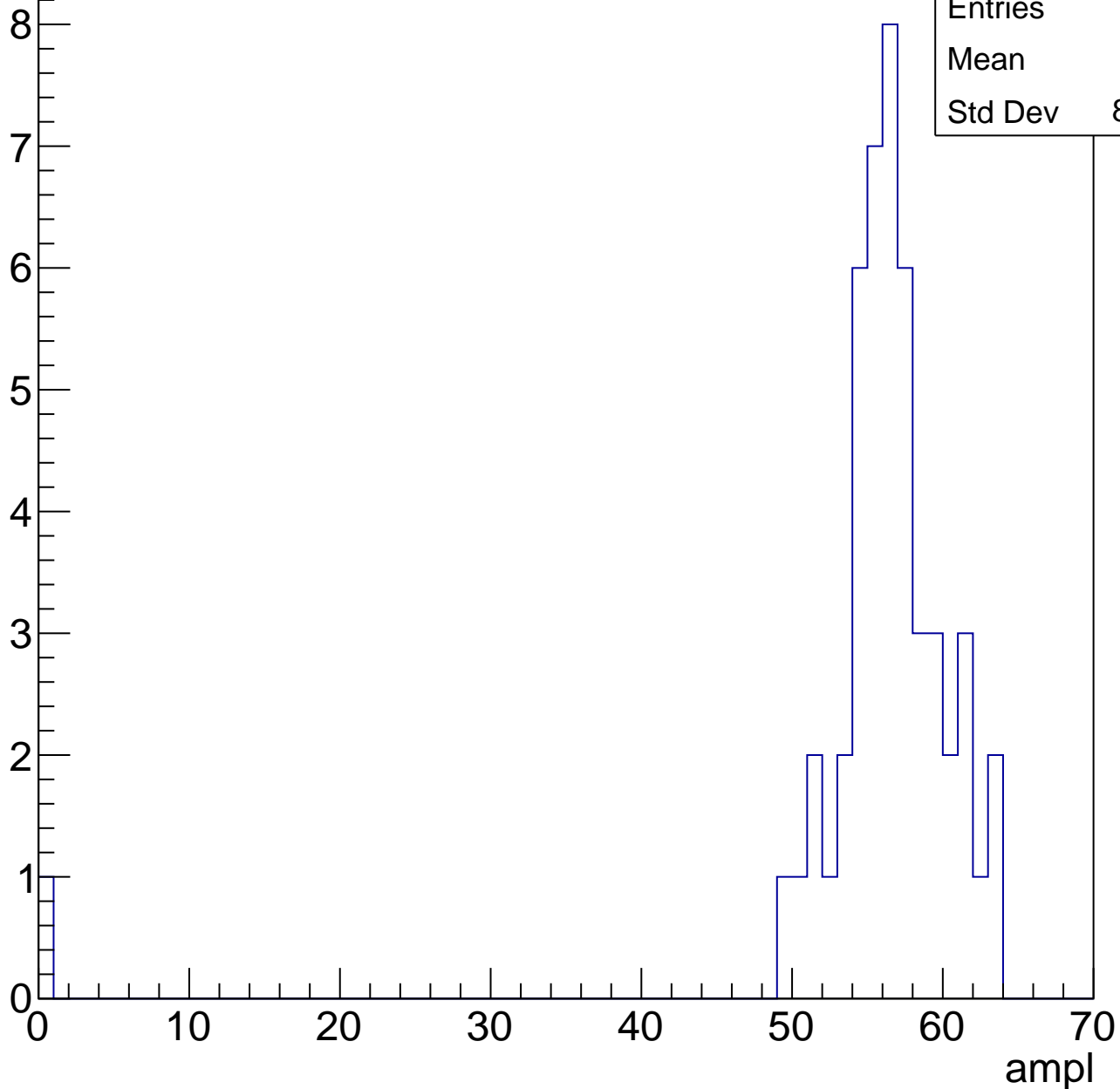
Entries	75
Mean	49.49
Std Dev	2.991

# B0L001S, U6-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	55.1
Std Dev	8.551



# B0L001S, U6-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	59.65
Std Dev	2.385

ampl

0

10

20

30

40

50

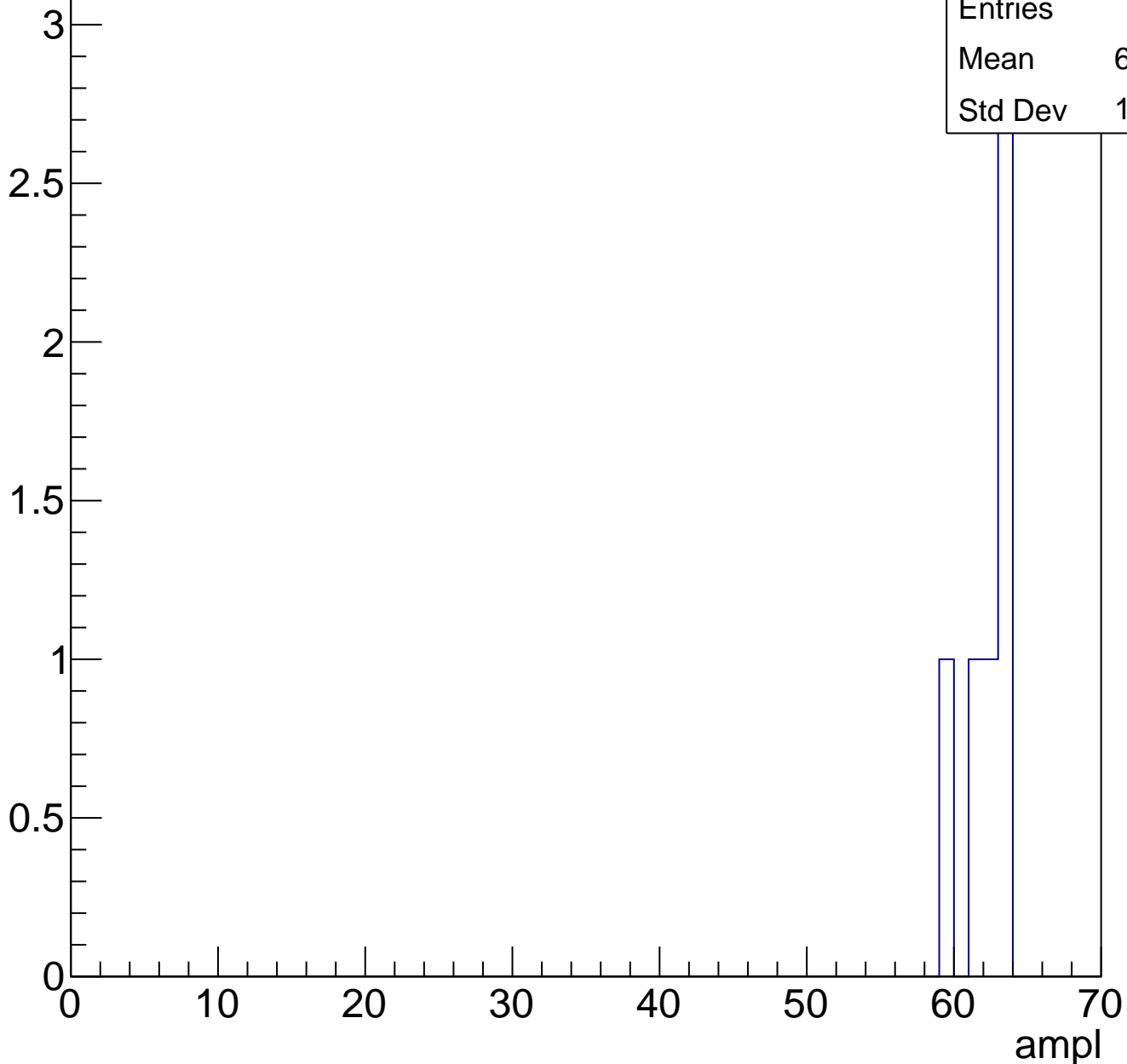
60

70

# B0L001S, U6-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

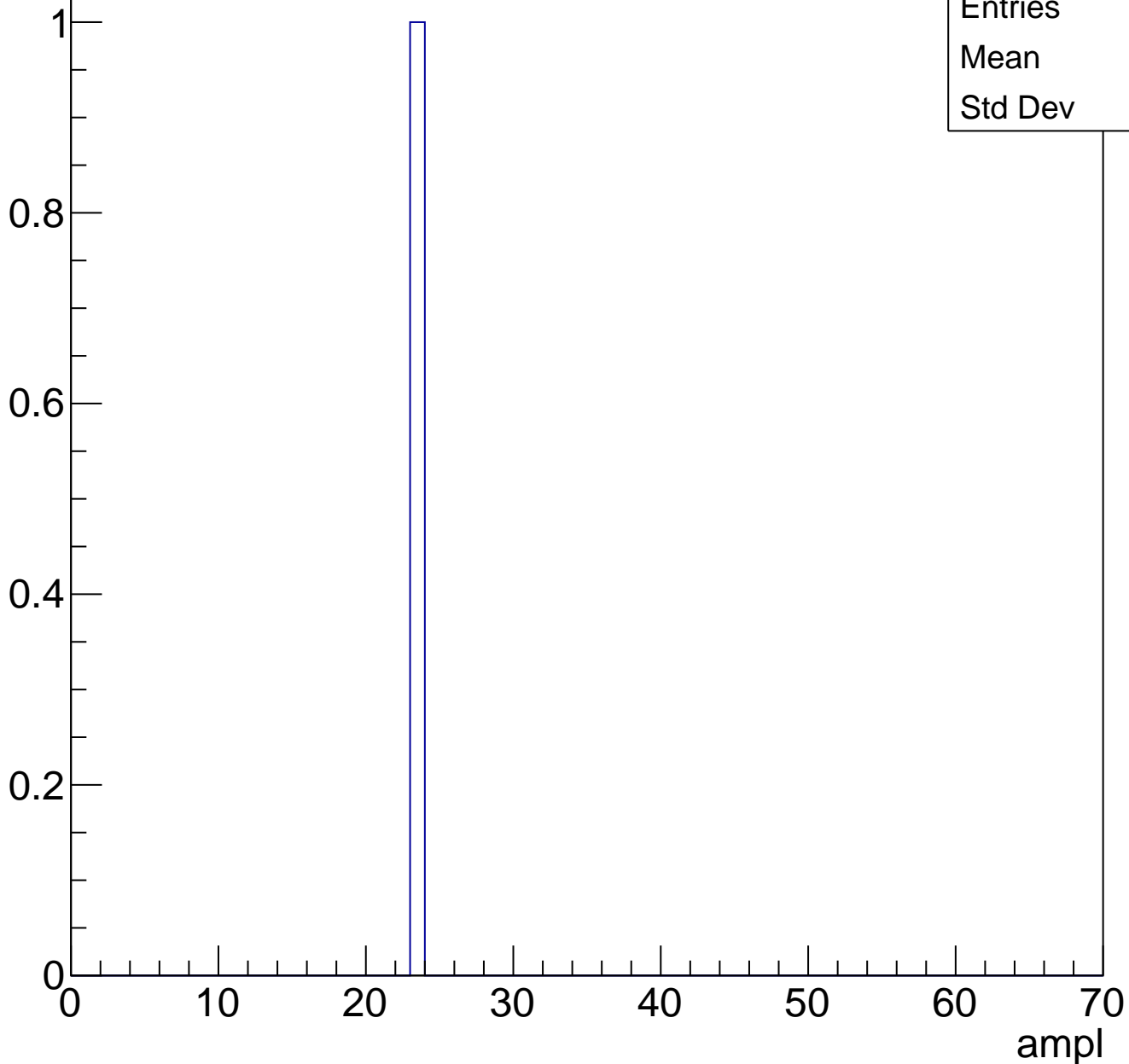




# B0L001S, U6-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch65, adc0

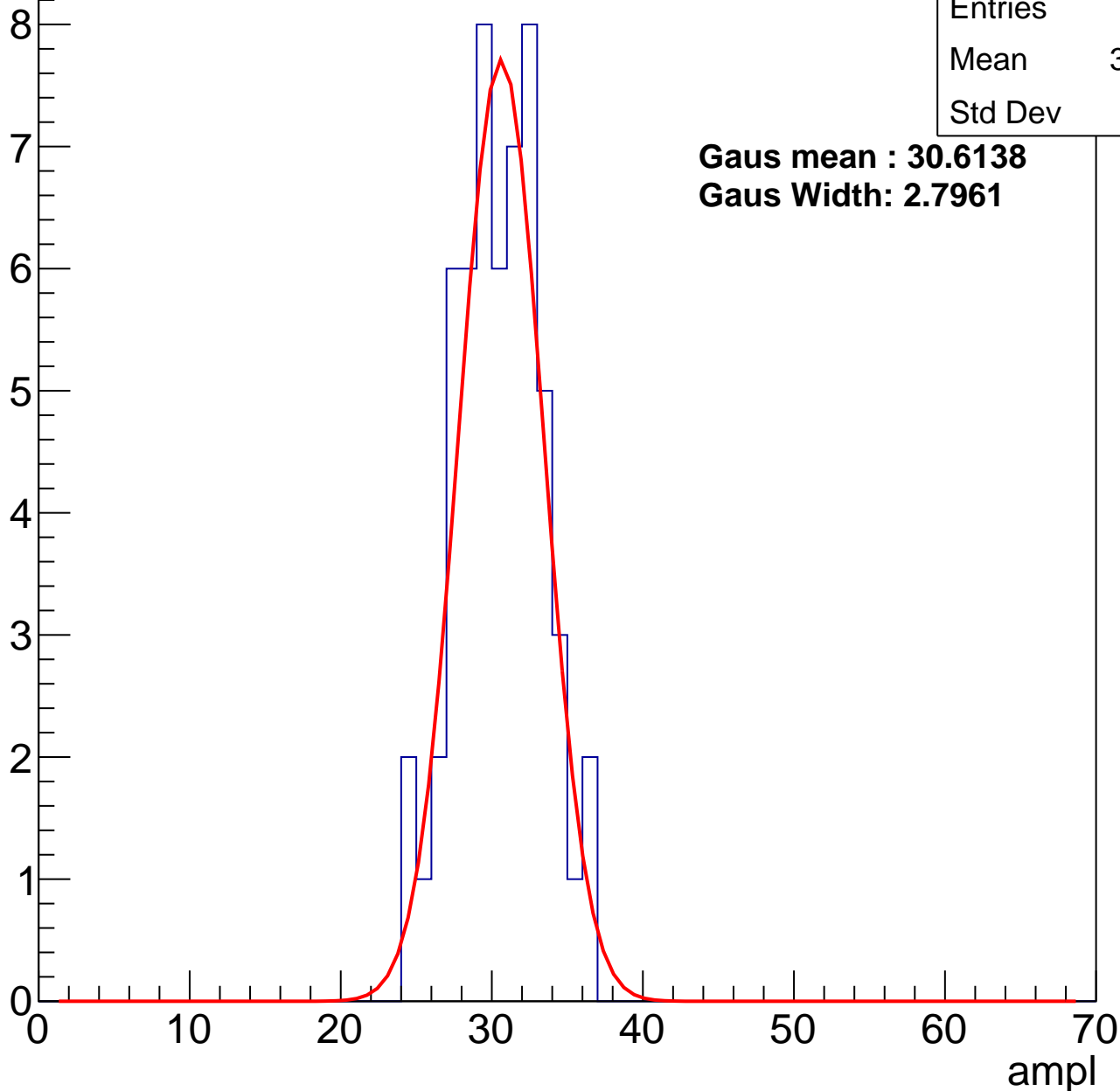
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	30.07
Std Dev	2.79

**Gaus mean : 30.6138**

**Gaus Width: 2.7961**



# B0L001S, U6-ch65, adc1

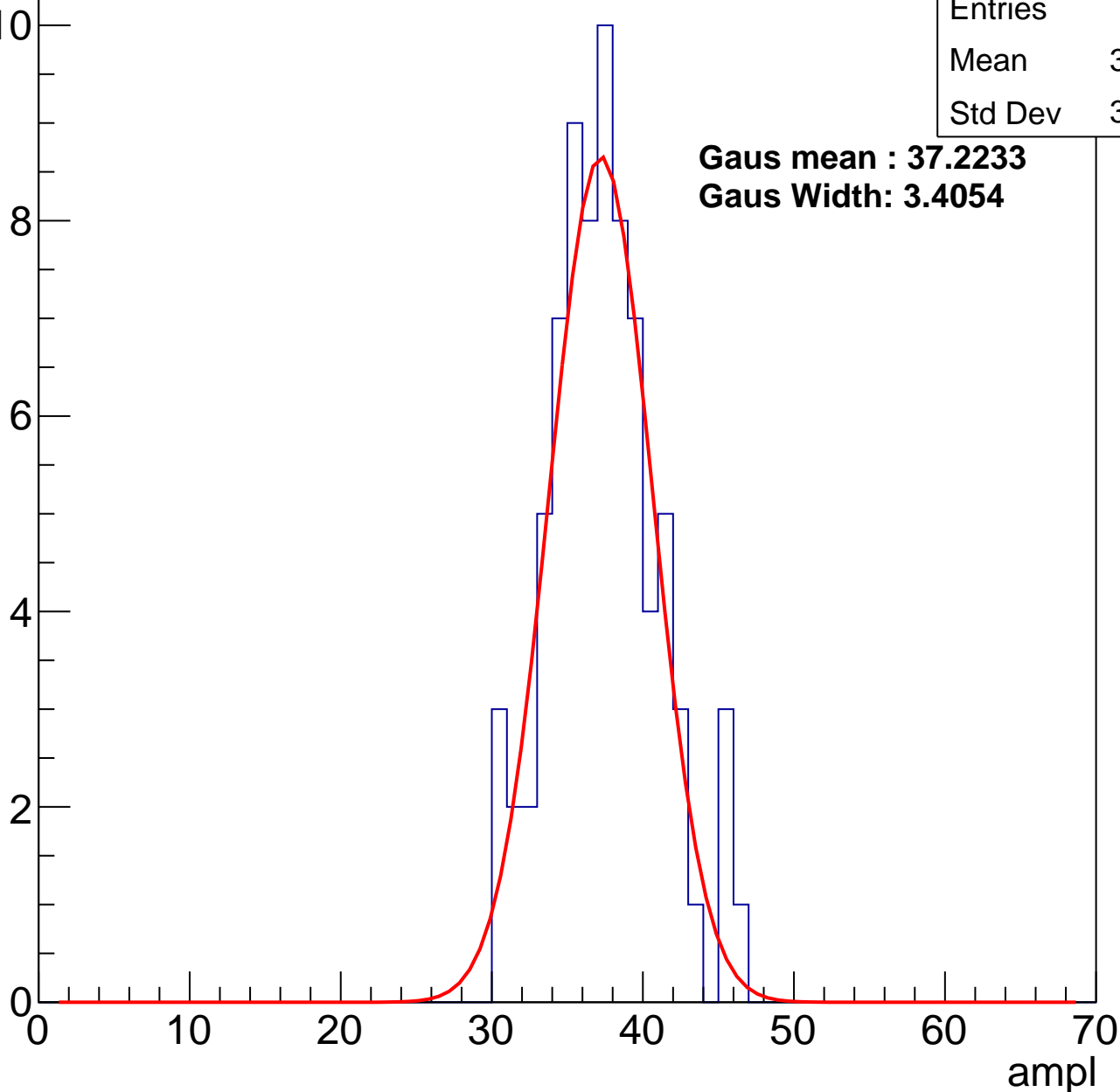
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	36.97
Std Dev	3.566

**Gaus mean : 37.2233**

**Gaus Width: 3.4054**



# B0L001S, U6-ch65, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	57
Mean	43.58
Std Dev	3.123

**Gaus mean : 43.5257**

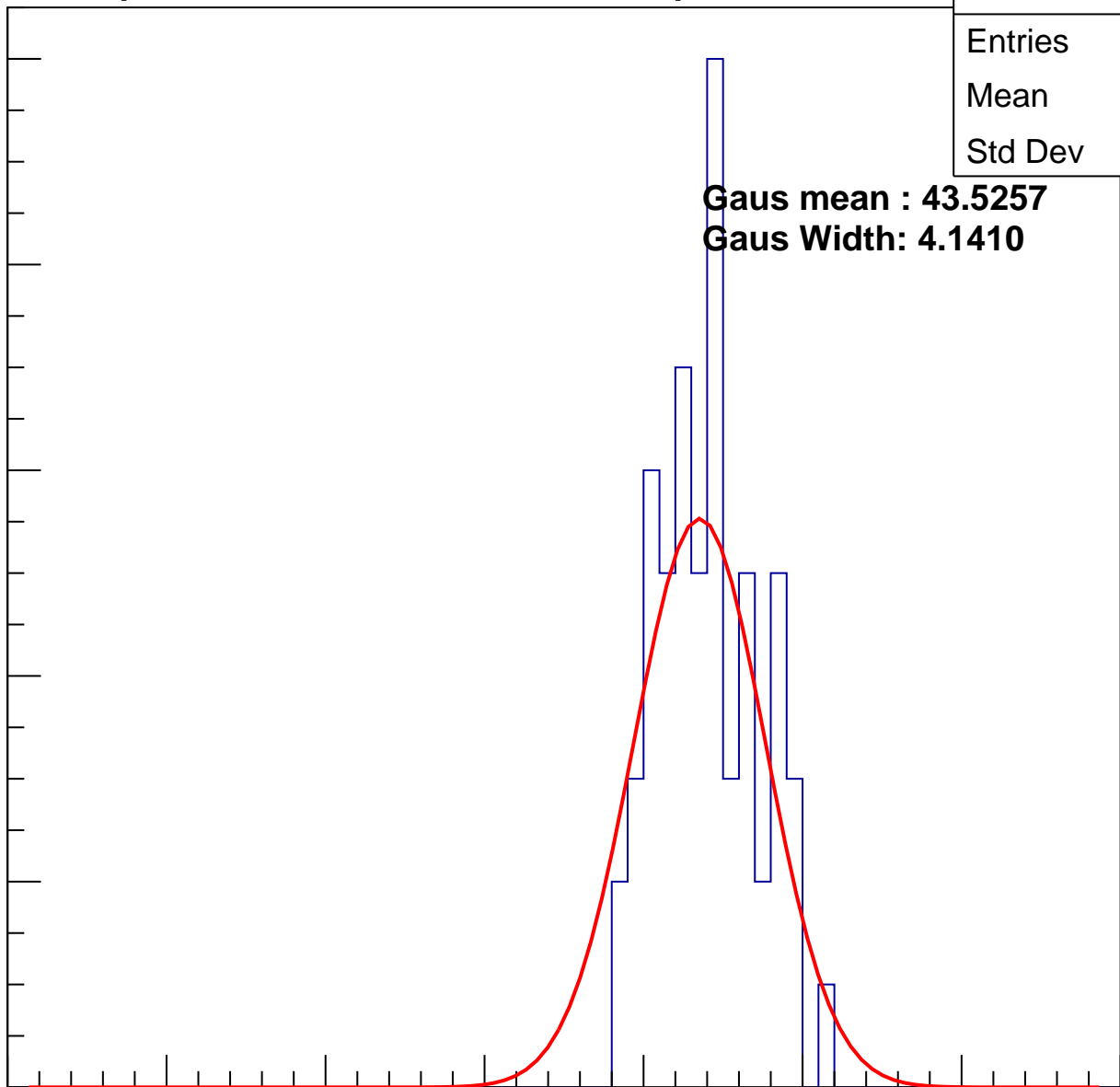
**Gaus Width: 4.1410**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U6-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

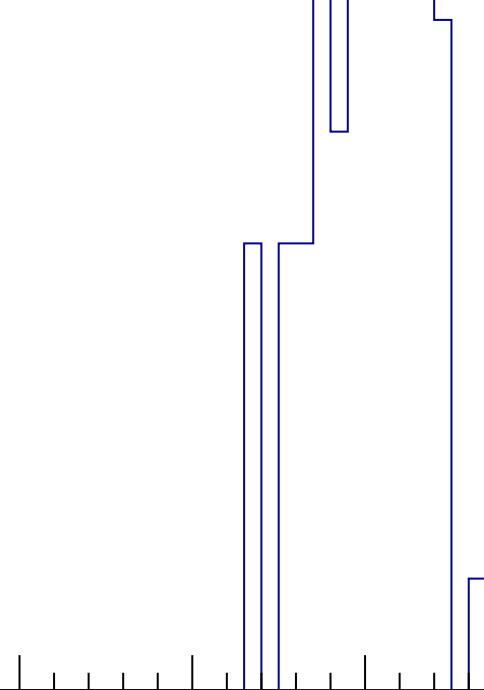
Entries	75
Mean	49.87
Std Dev	3.328

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

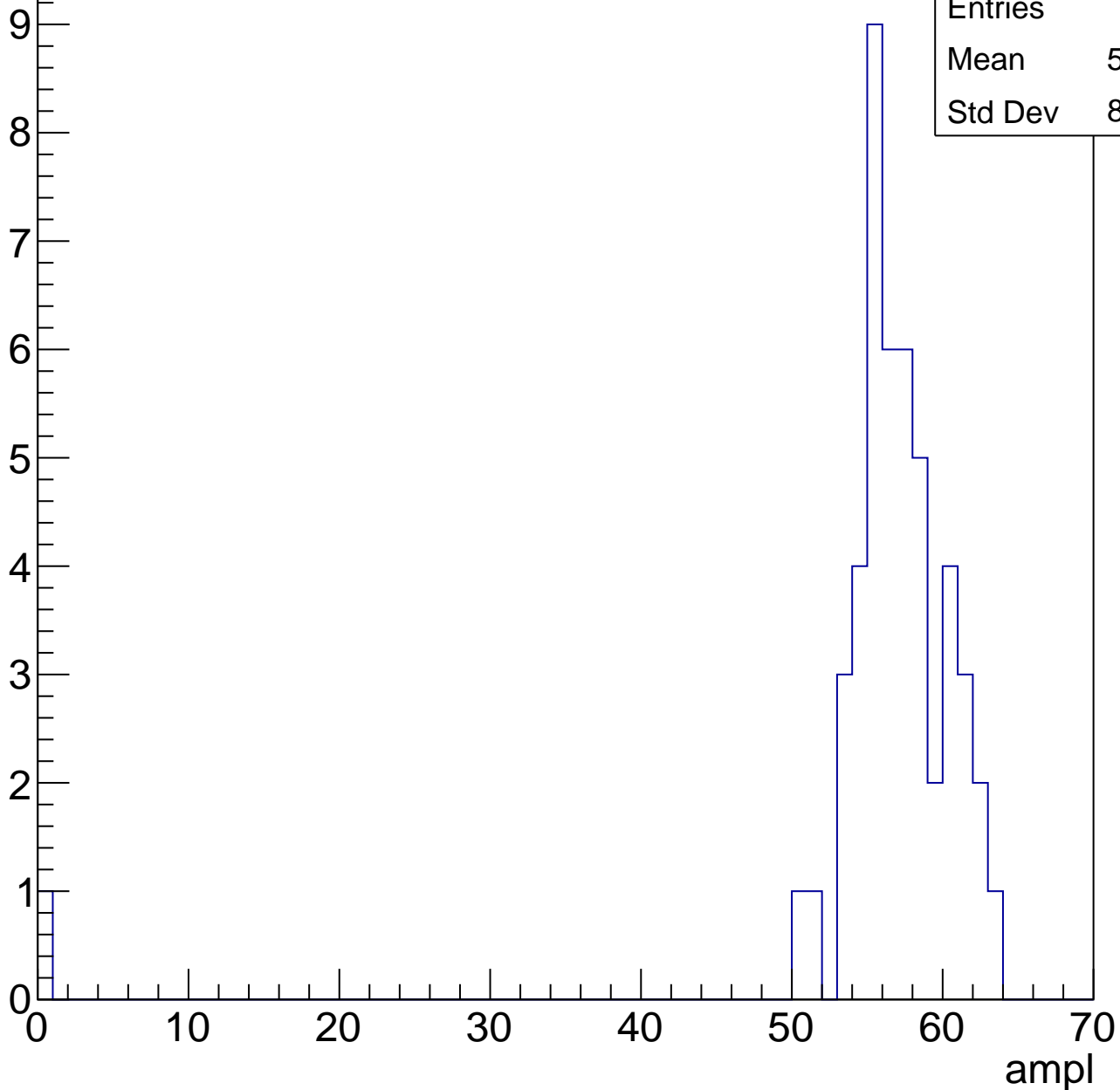


# B0L001S, U6-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	55.56
Std Dev	8.592

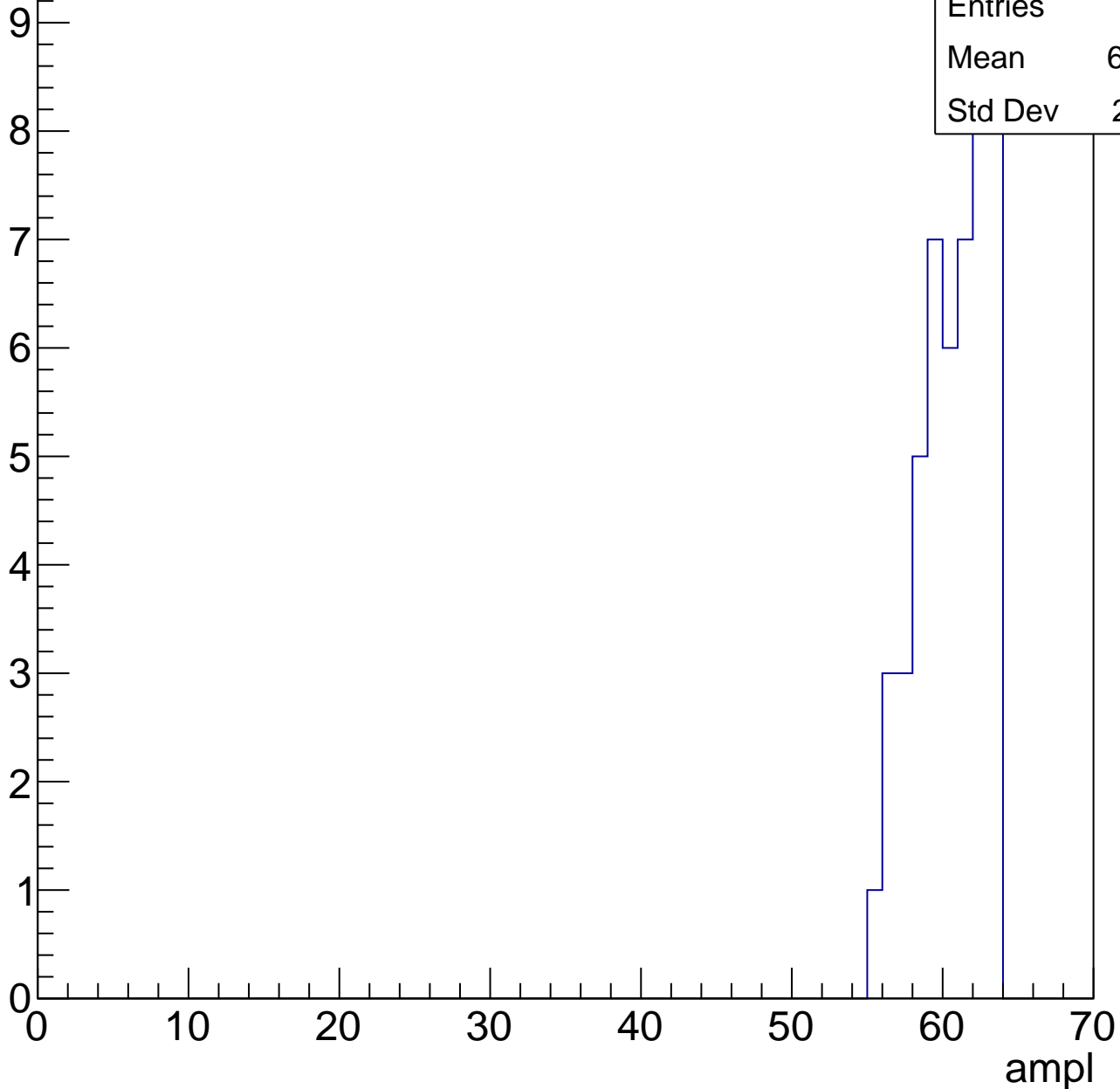


# B0L001S, U6-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	60.14
Std Dev	2.241



# B0L001S, U6-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U6-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U6-ch66, adc0

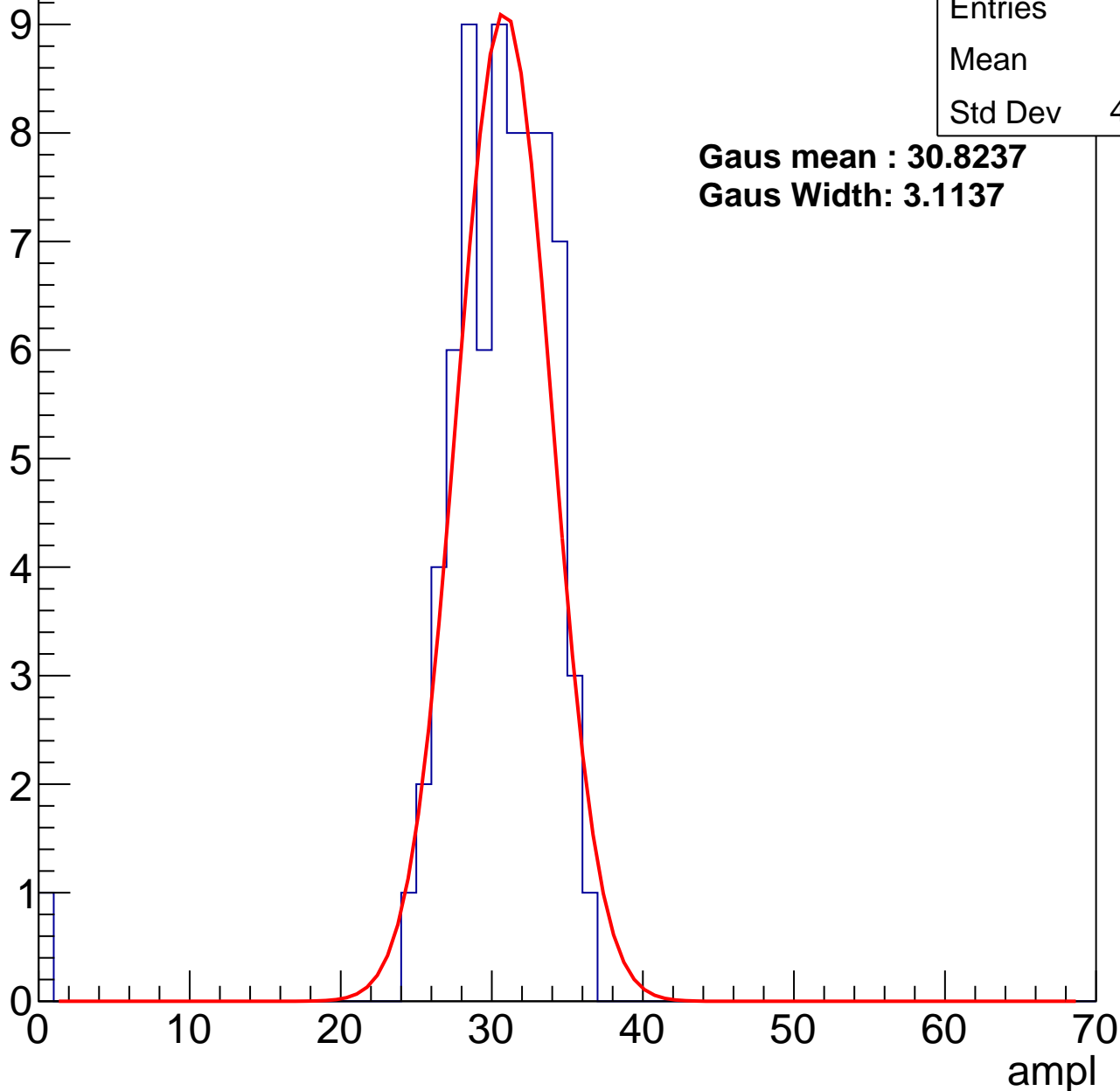
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	29.9
Std Dev	4.503

**Gaus mean : 30.8237**

**Gaus Width: 3.1137**



# B0L001S, U6-ch66, adc1

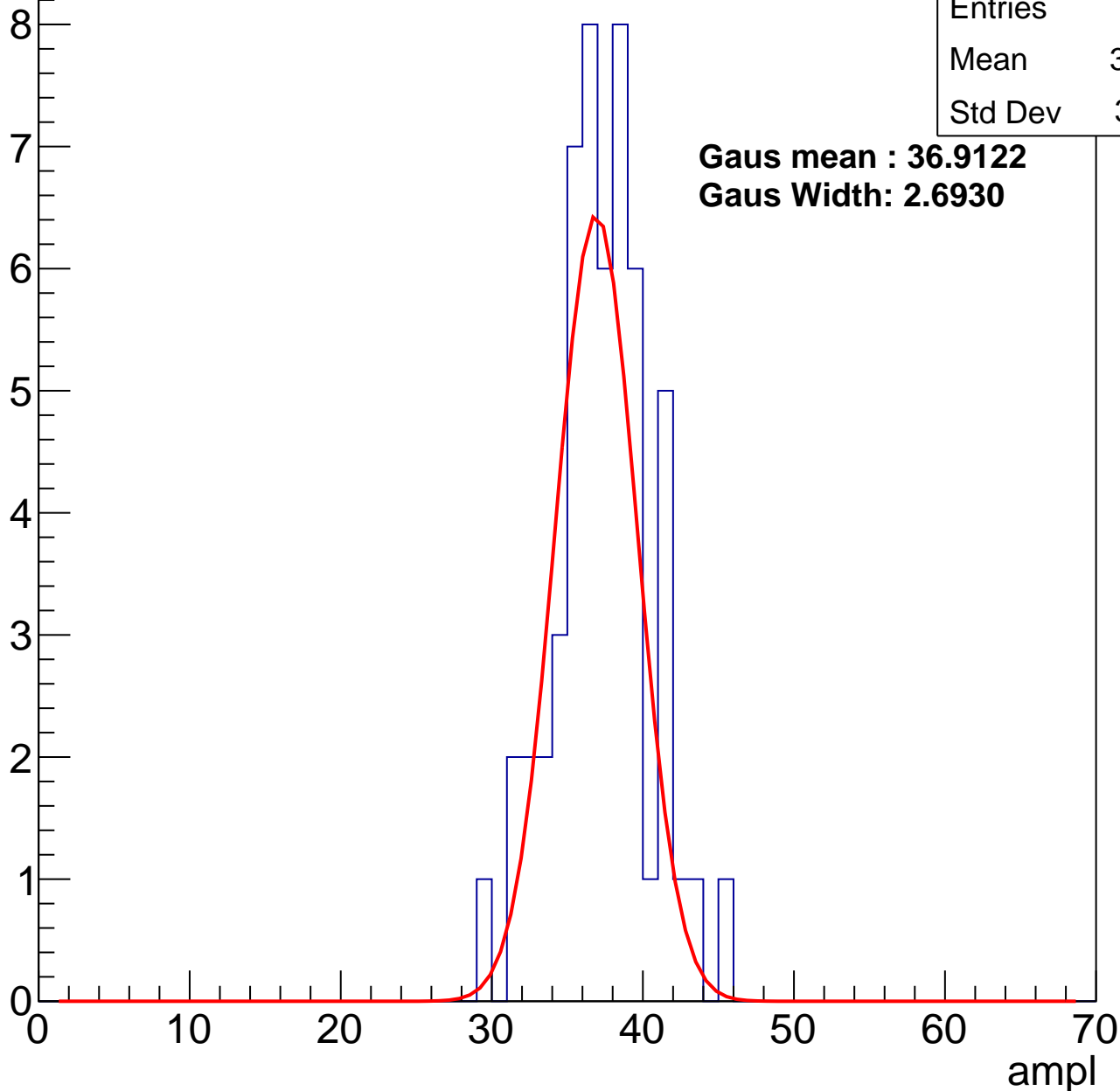
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	36.87
Std Dev	3.121

**Gaus mean : 36.9122**

**Gaus Width: 2.6930**



# B0L001S, U6-ch66, adc2

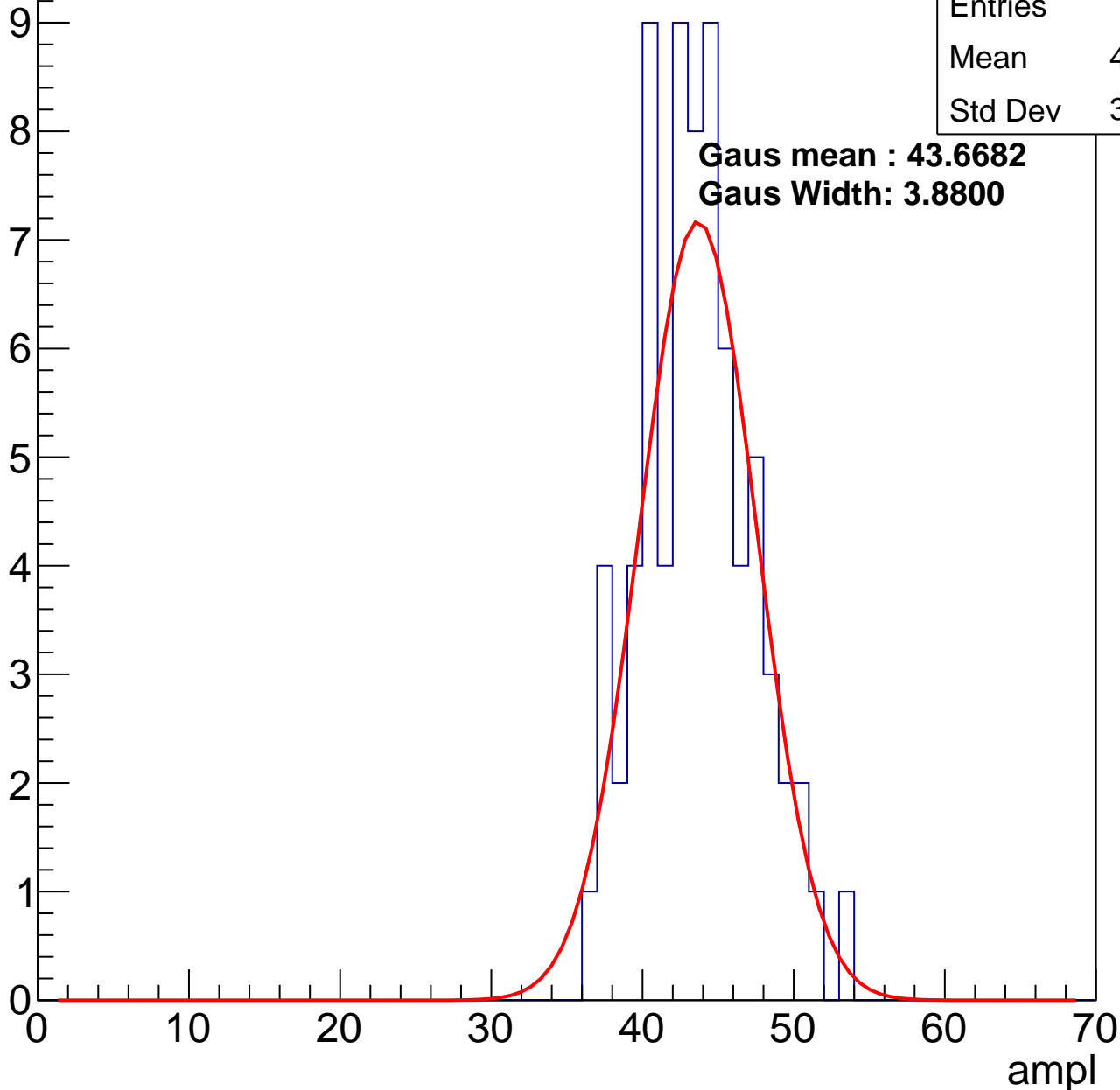
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	43.15
Std Dev	3.619

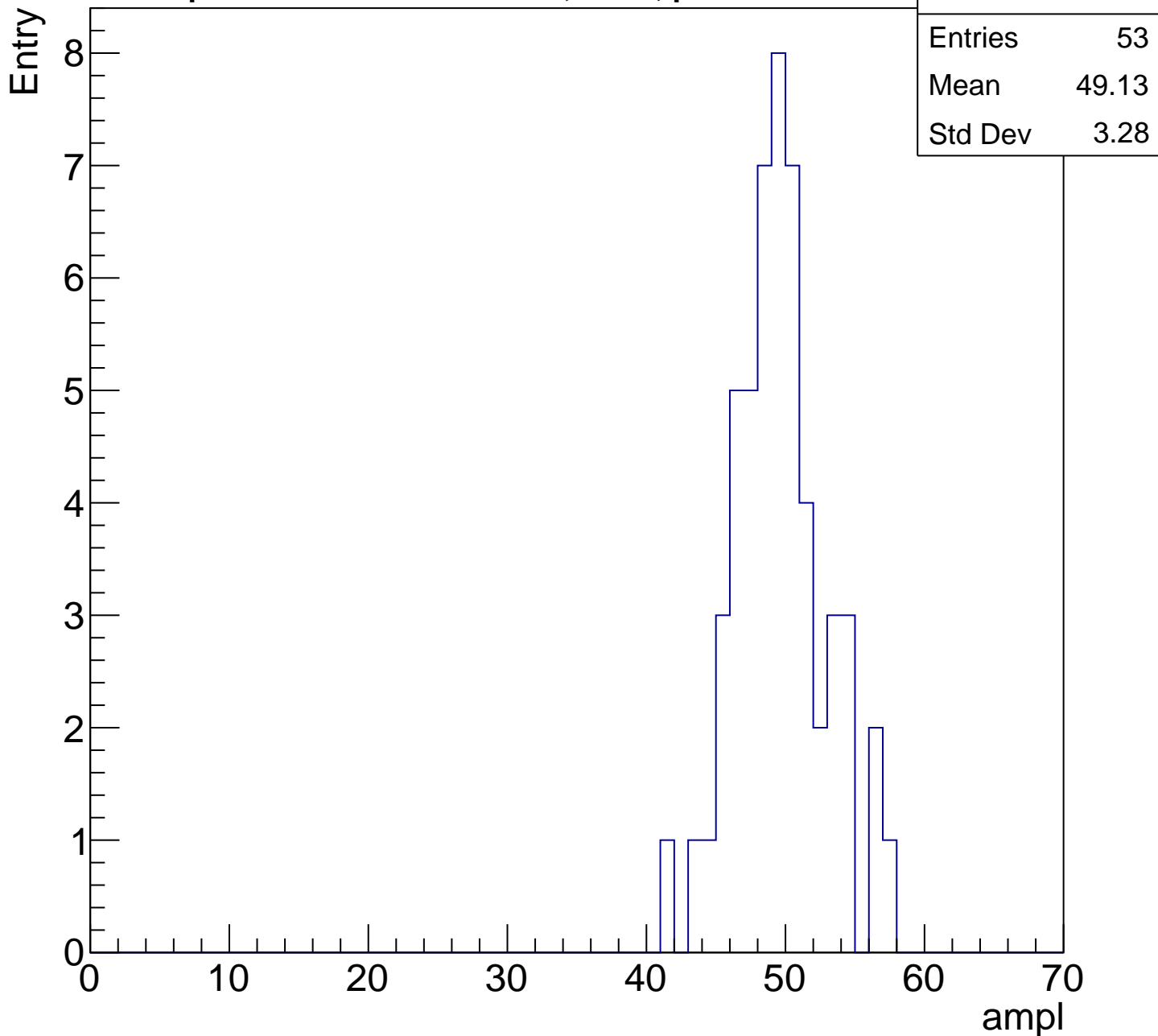
**Gaus mean : 43.6682**

**Gaus Width: 3.8800**



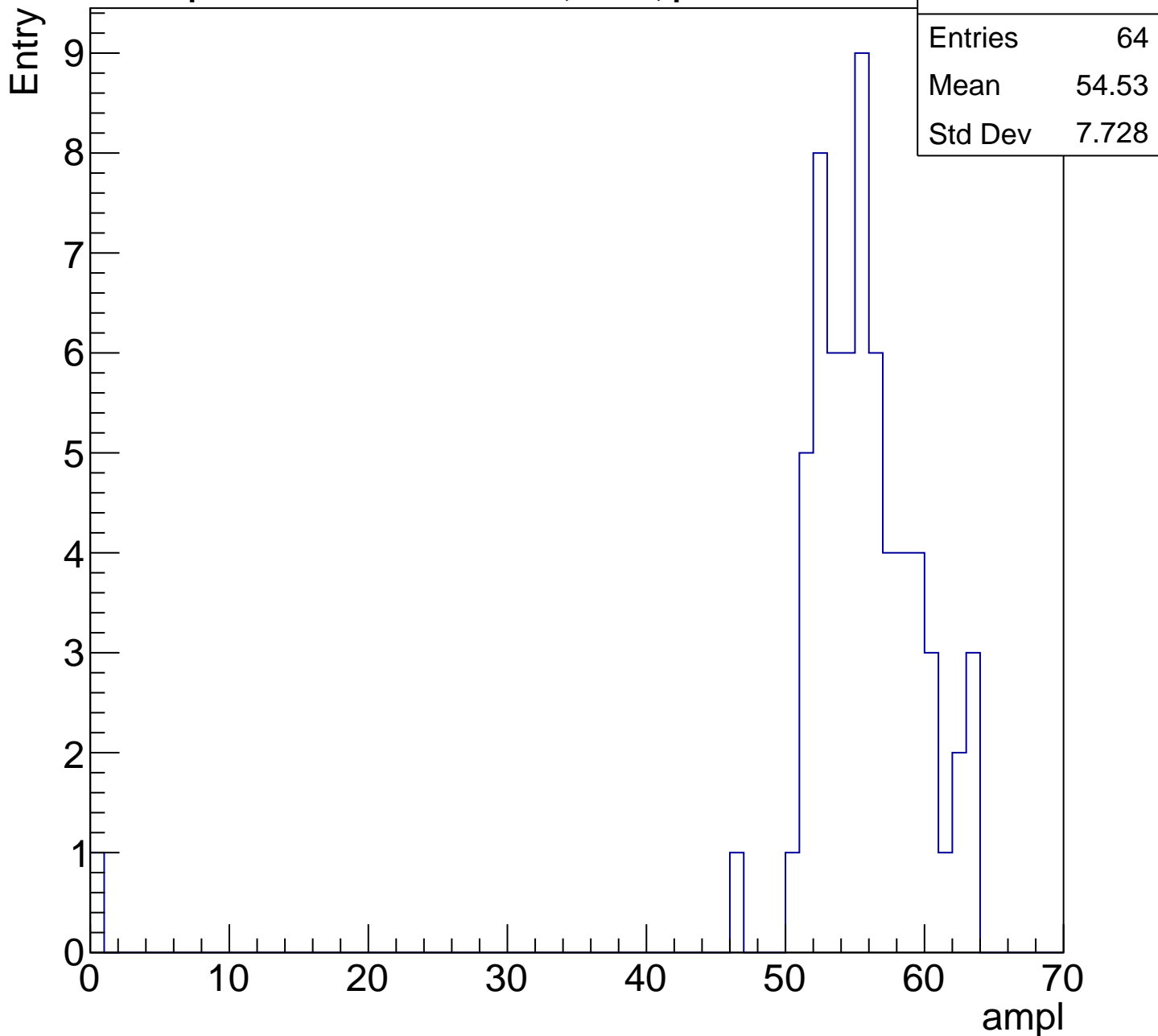
# B0L001S, U6-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U6-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U6-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

7

6

5

4

3

2

1

0

Entries

41

Mean

59.39

Std Dev

2.174

ampl

0

10

20

30

40

50

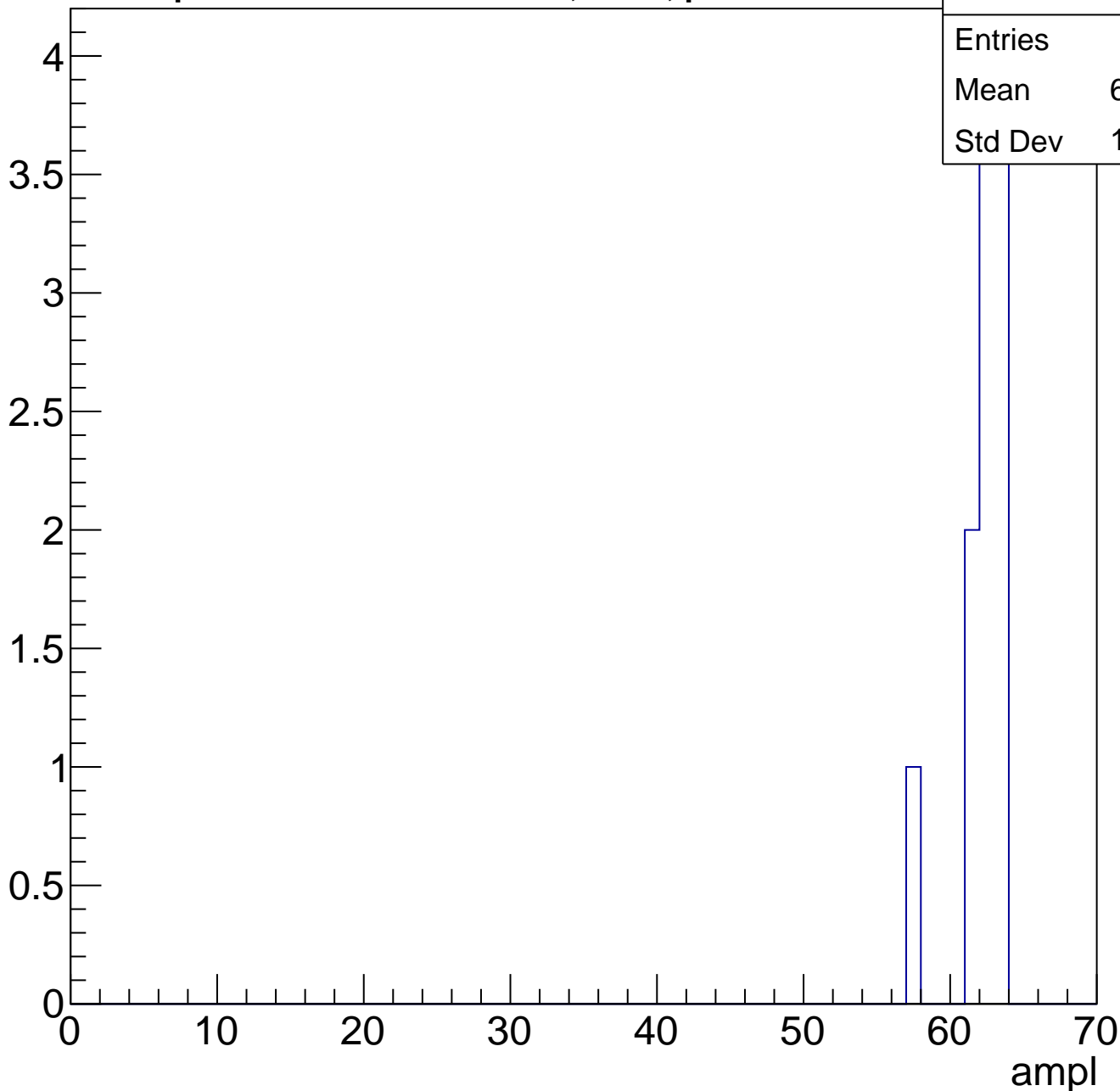
60

70

# B0L001S, U6-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	11.5
Std Dev	11.5

# B0L001S, U6-ch67, adc0

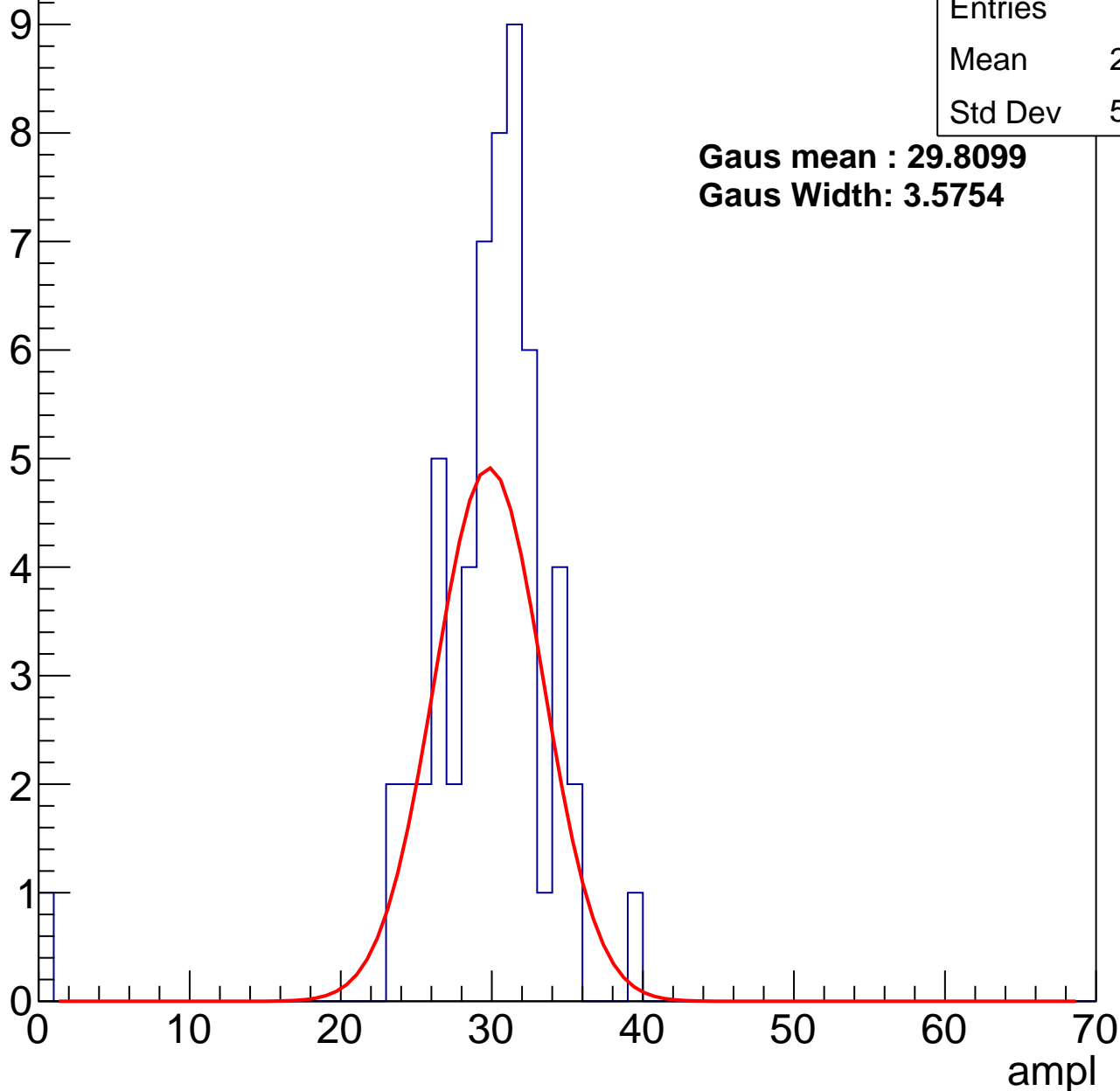
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	29.14
Std Dev	5.065

**Gaus mean : 29.8099**

**Gaus Width: 3.5754**



# B0L001S, U6-ch67, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	79
Mean	36.92
Std Dev	3.906

**Gaus mean : 37.2130**

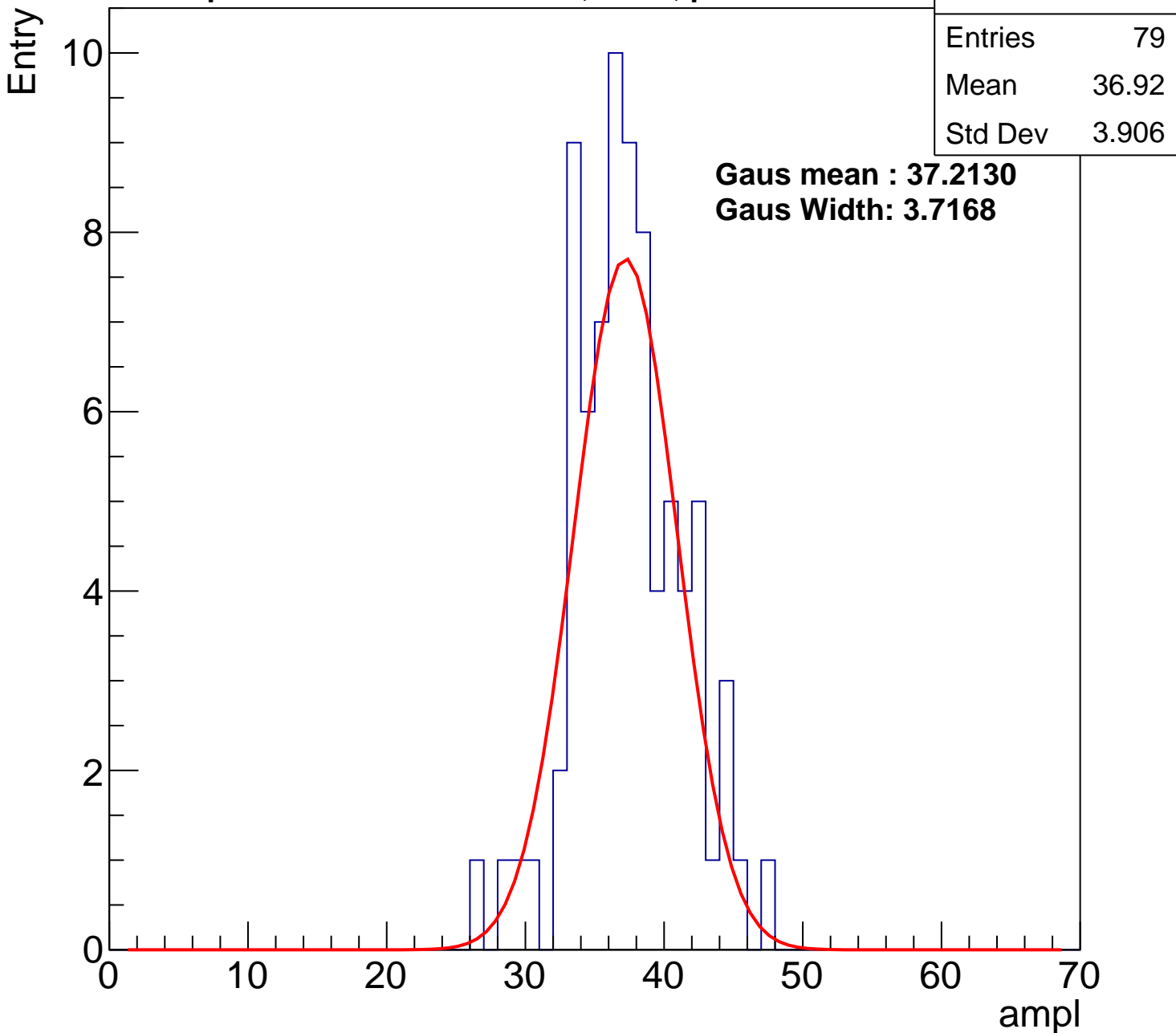
**Gaus Width: 3.7168**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



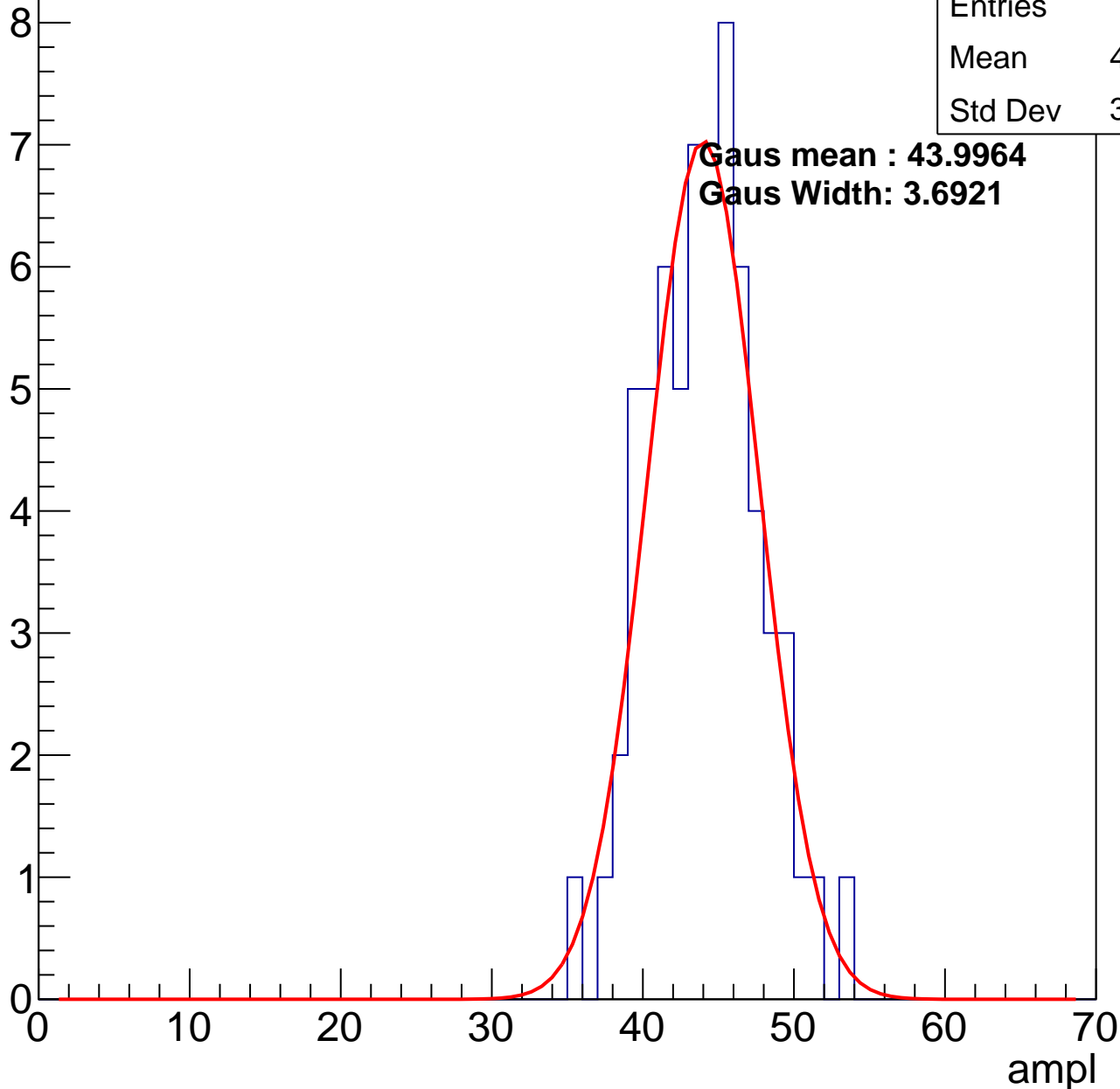
# B0L001S, U6-ch67, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

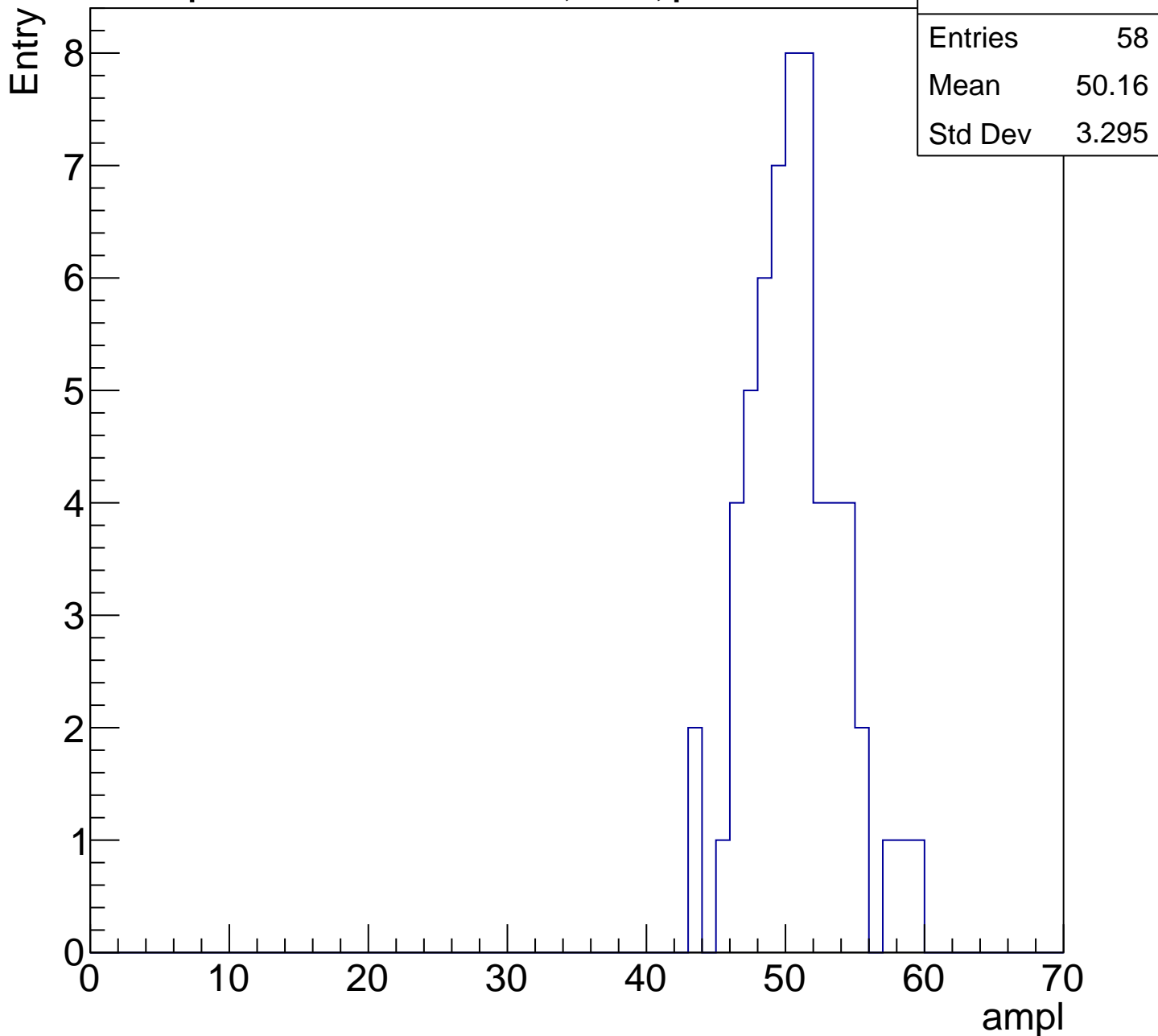
Entries	66
Mean	43.59
Std Dev	3.555

**Gaus mean : 43.9964**  
**Gaus Width: 3.6921**



# B0L001S, U6-ch67, adc3

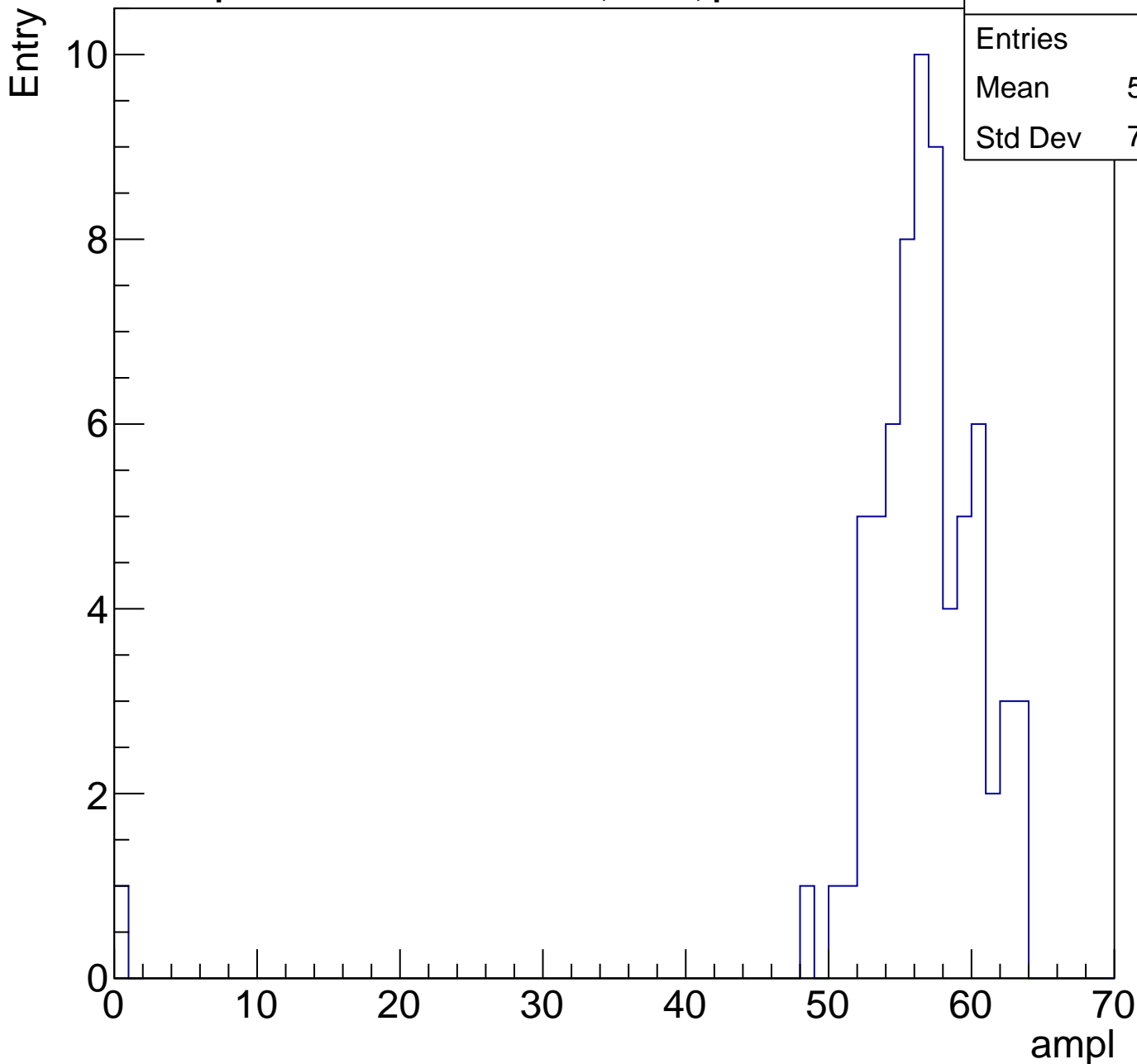
calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U6-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	70
Mean	55.64
Std Dev	7.445

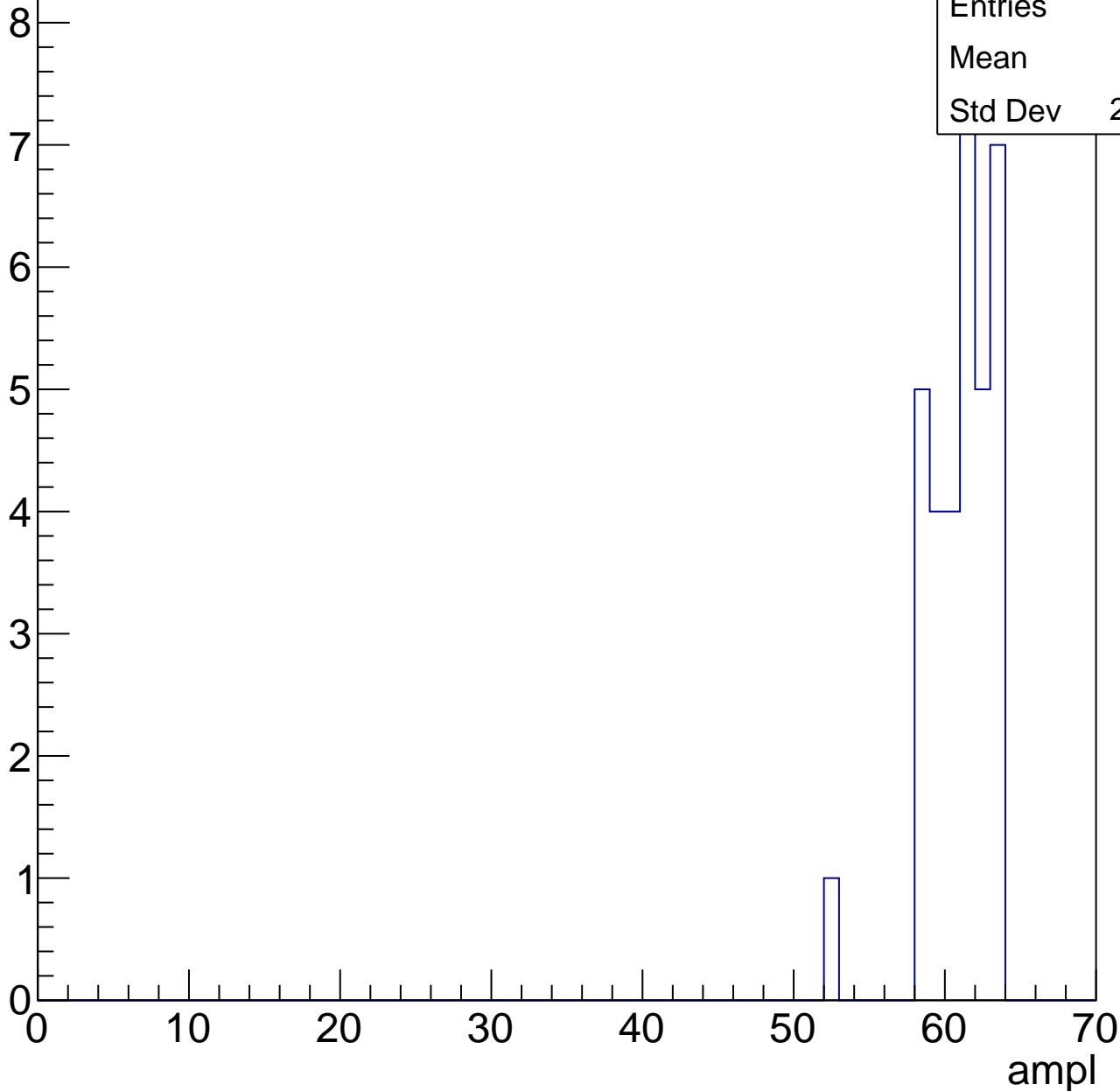


# B0L001S, U6-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	34
Mean	60.5
Std Dev	2.239



# B0L001S, U6-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U6-ch68, adc0

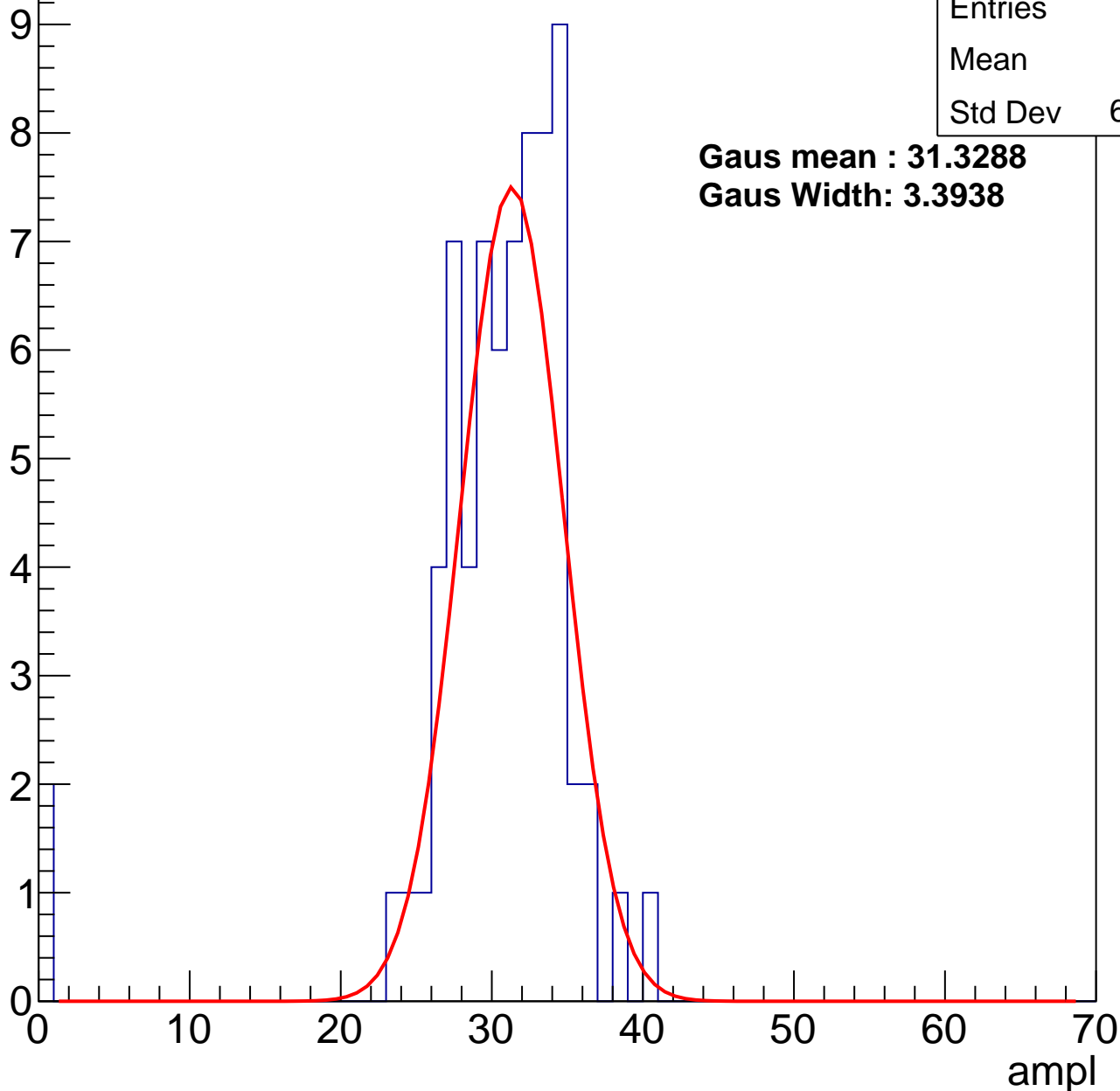
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	29.9
Std Dev	6.052

**Gaus mean : 31.3288**

**Gaus Width: 3.3938**



# B0L001S, U6-ch68, adc1

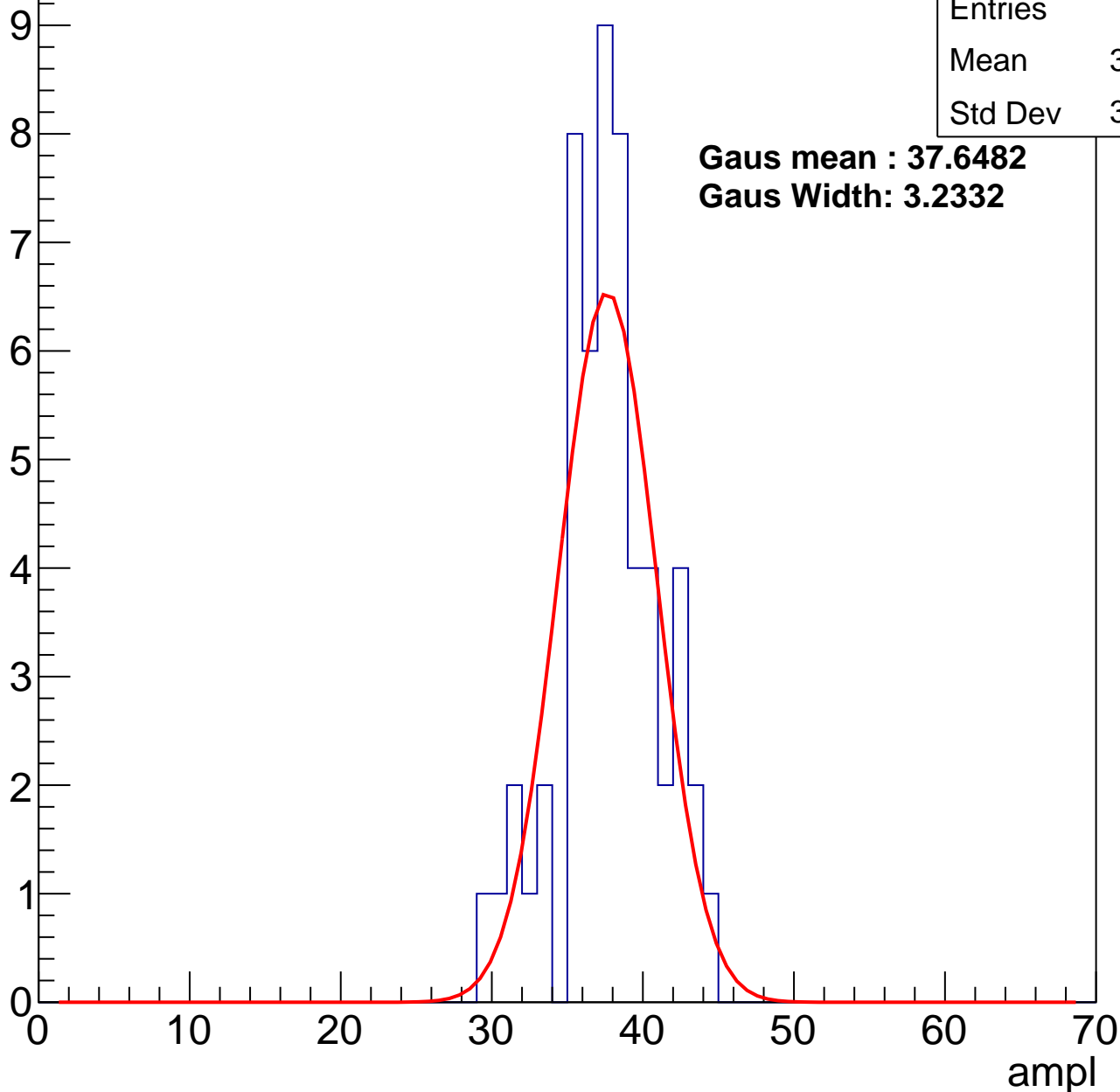
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	37.24
Std Dev	3.275

**Gaus mean : 37.6482**

**Gaus Width: 3.2332**



# B0L001S, U6-ch68, adc2

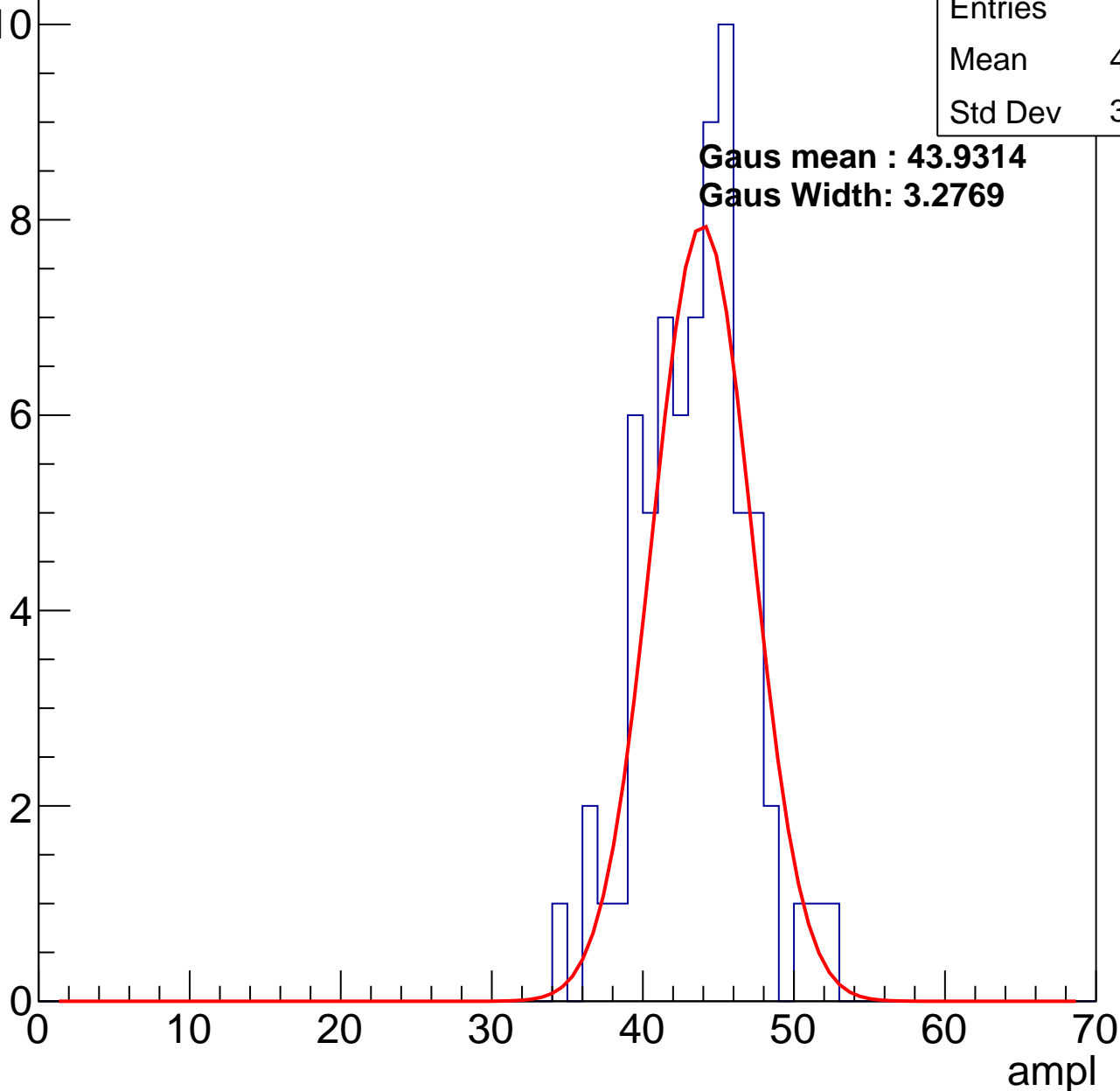
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	70
Mean	43.07
Std Dev	3.449

**Gaus mean : 43.9314**

**Gaus Width: 3.2769**

Entry

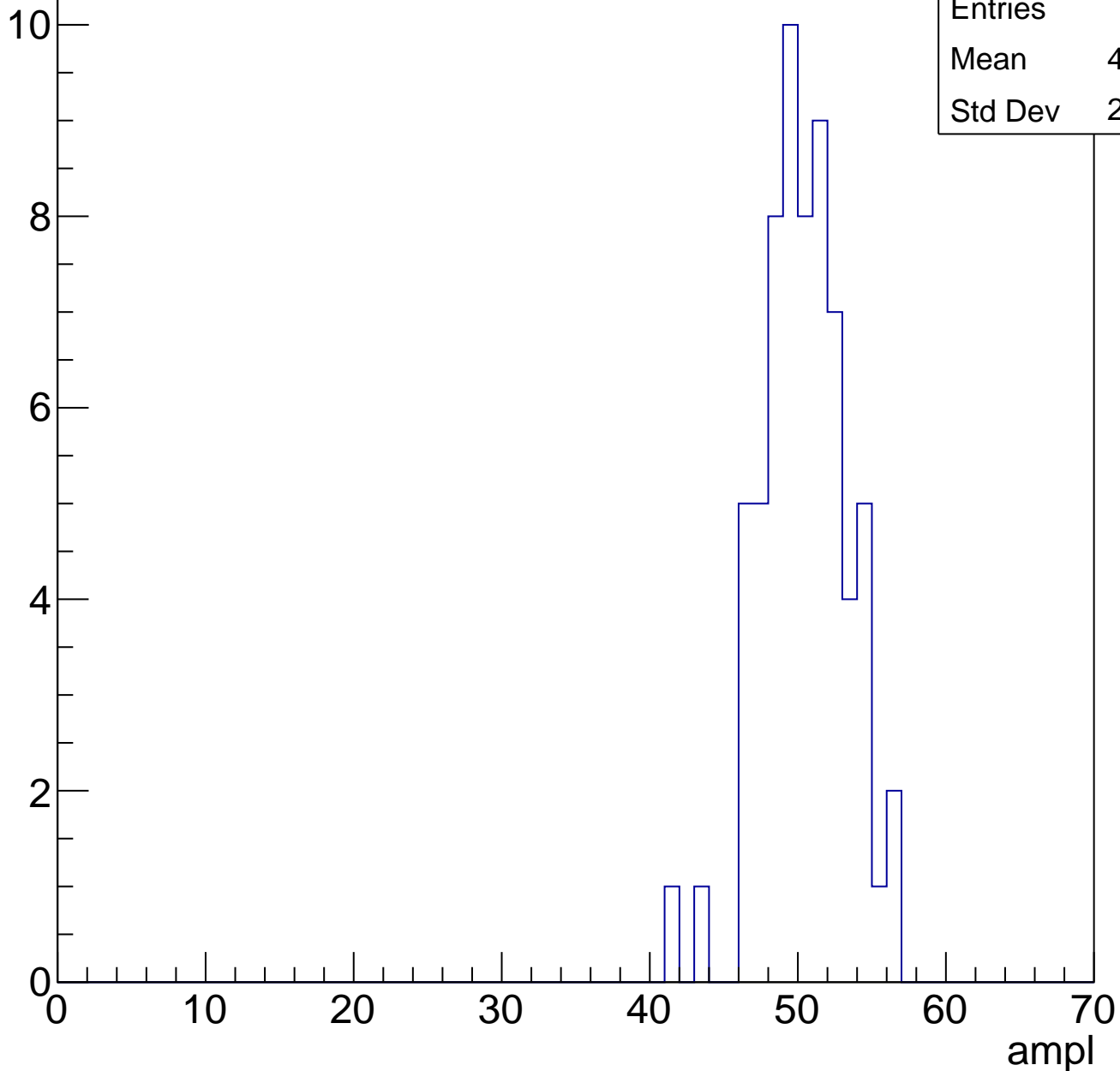


# B0L001S, U6-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	66
Mean	49.92
Std Dev	2.878

Entry

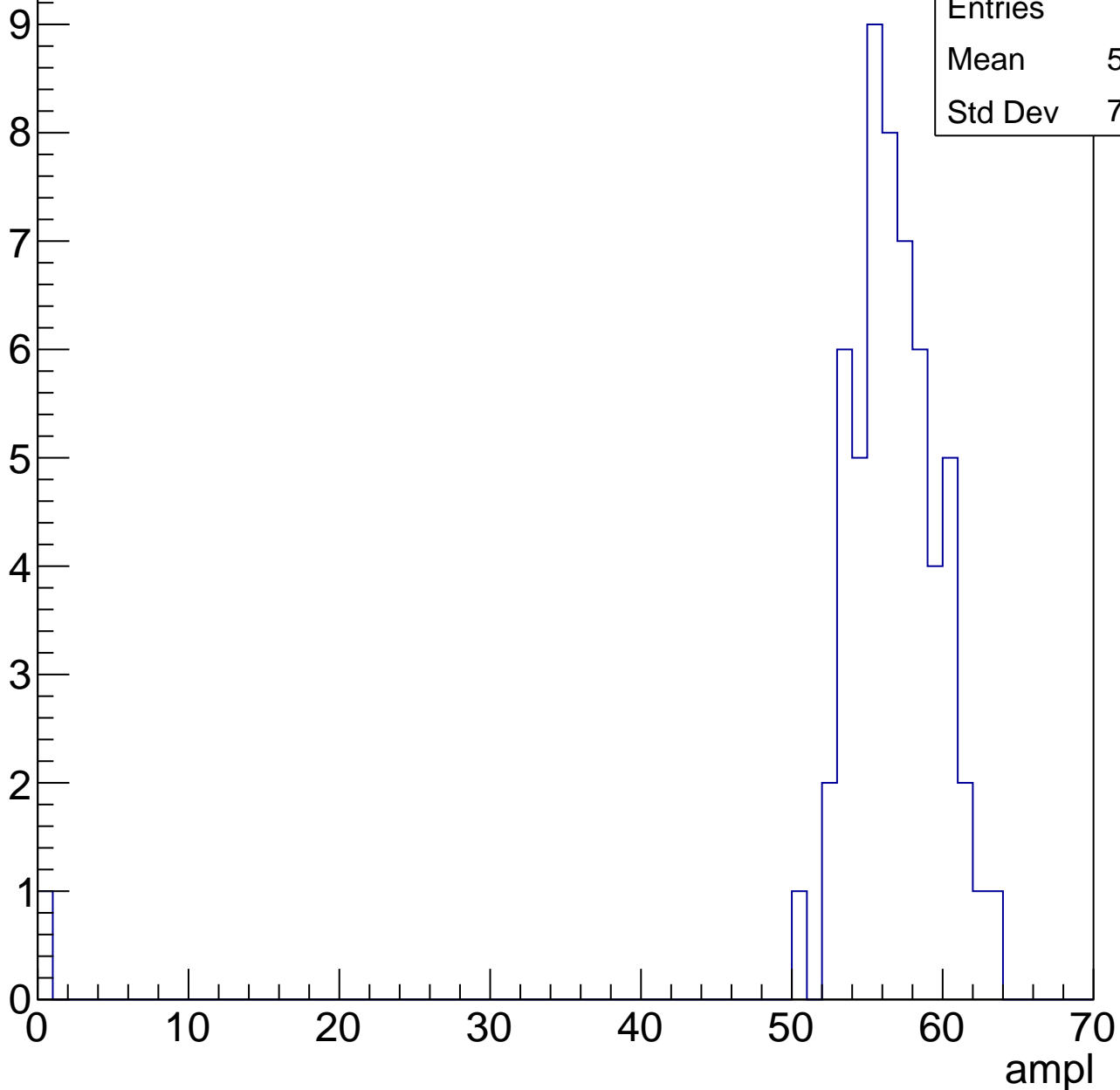


# B0L001S, U6-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	55.43
Std Dev	7.824

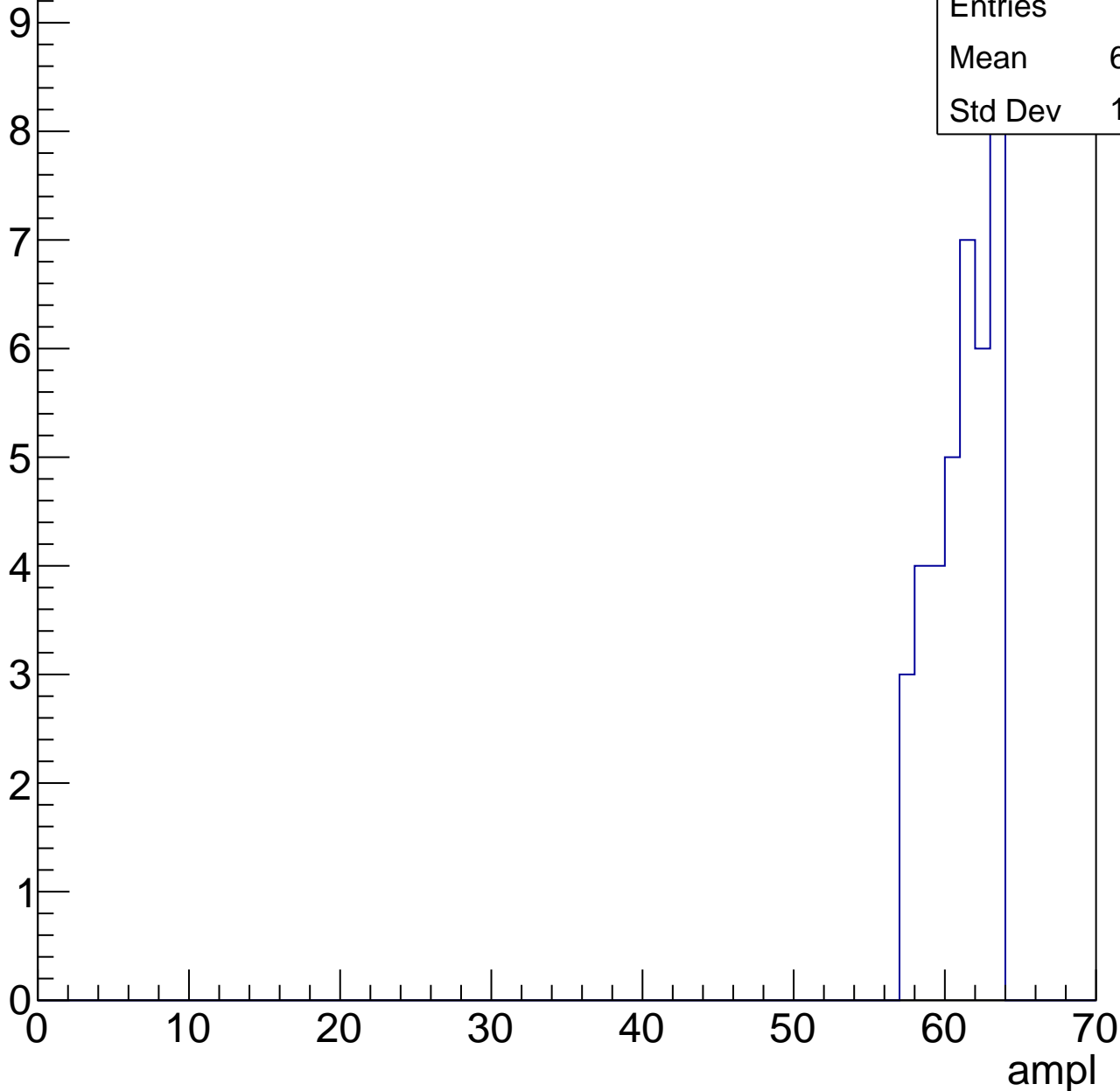


# B0L001S, U6-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

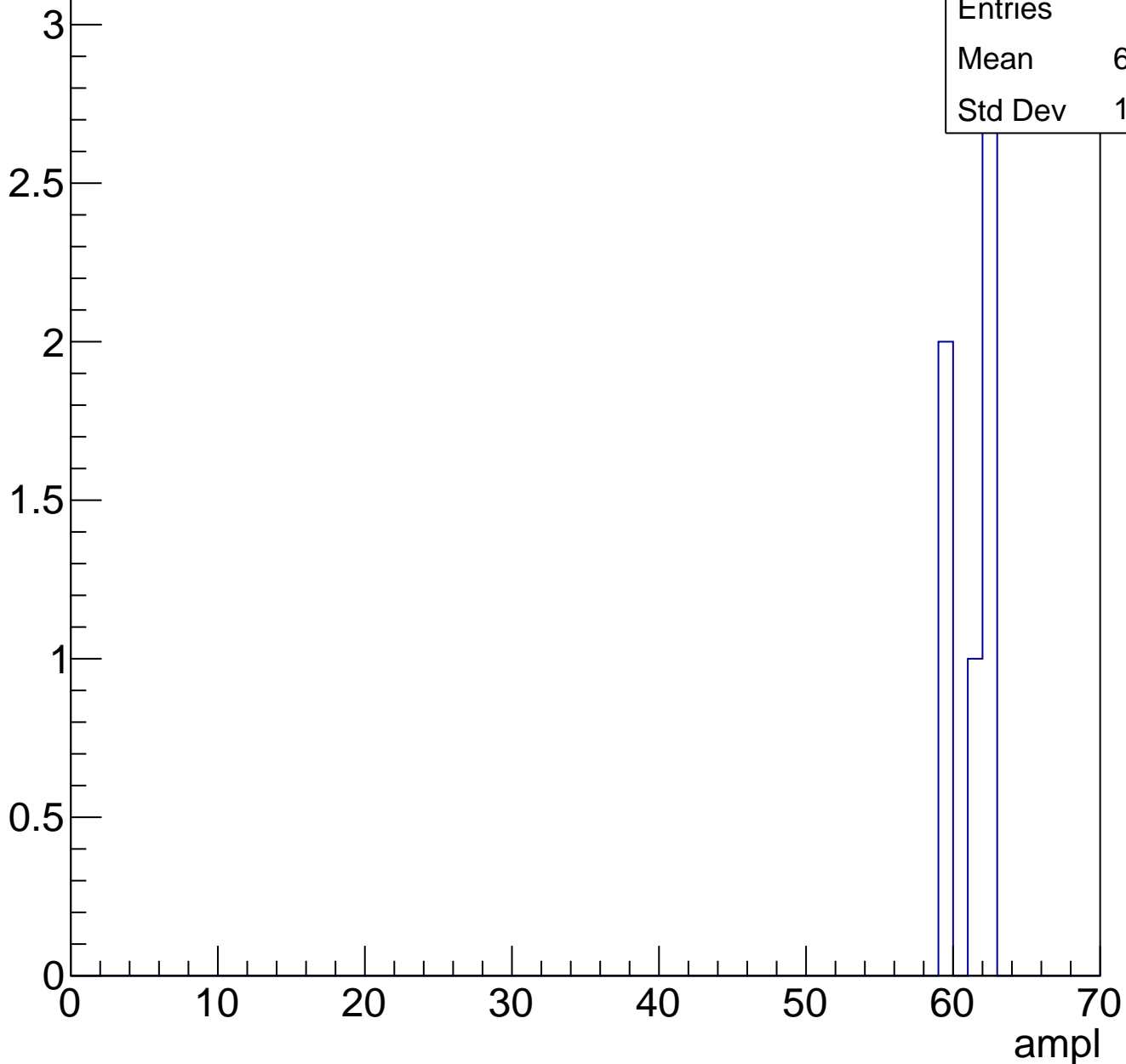
Entries	38
Mean	60.66
Std Dev	1.937



# B0L001S, U6-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U6-ch69, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	70
Mean	28.9
Std Dev	4.899

**Gaus mean : 29.9370**

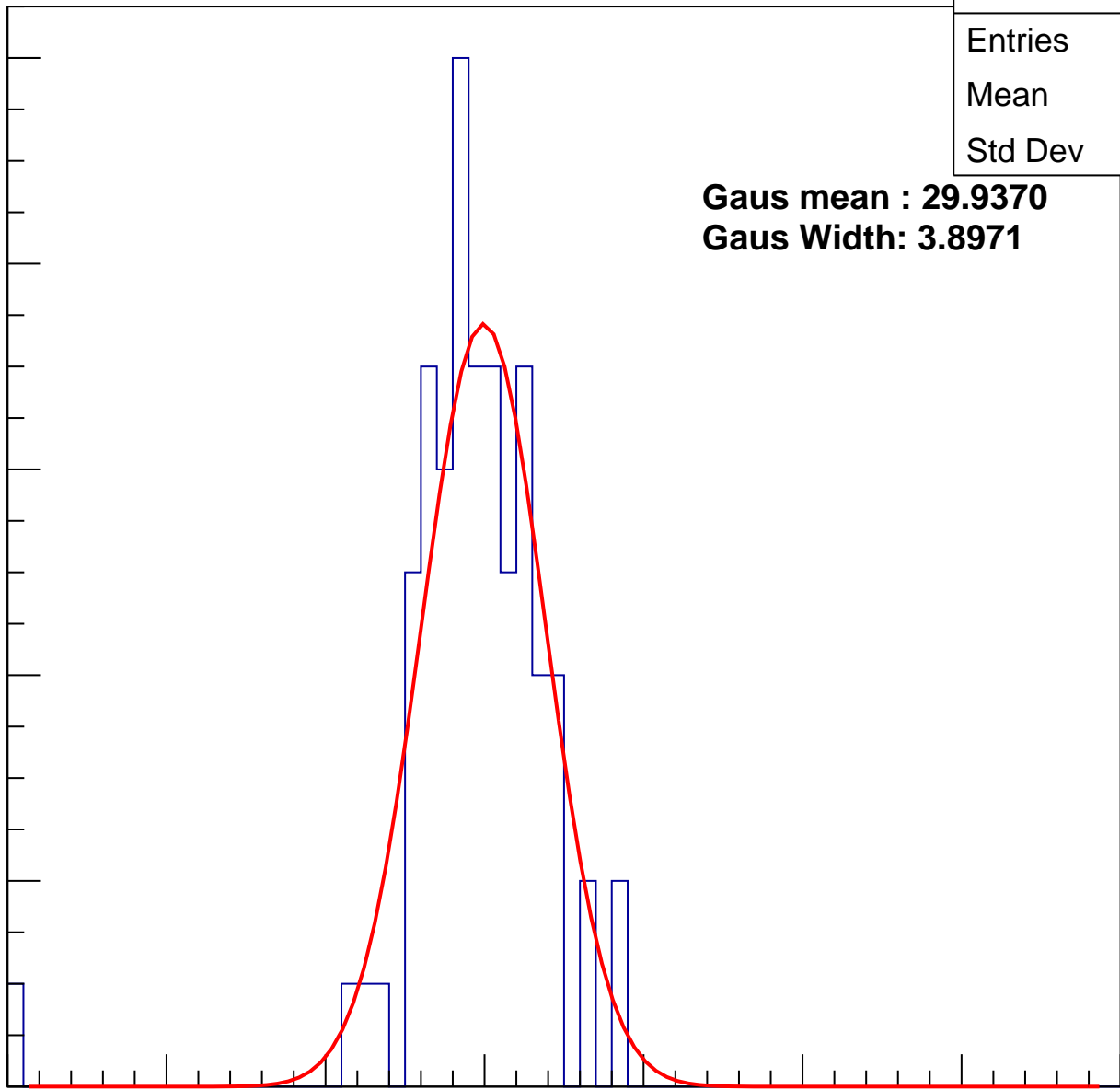
**Gaus Width: 3.8971**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U6-ch69, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	68
Mean	35.65
Std Dev	3.407

**Gaus mean : 36.3888**

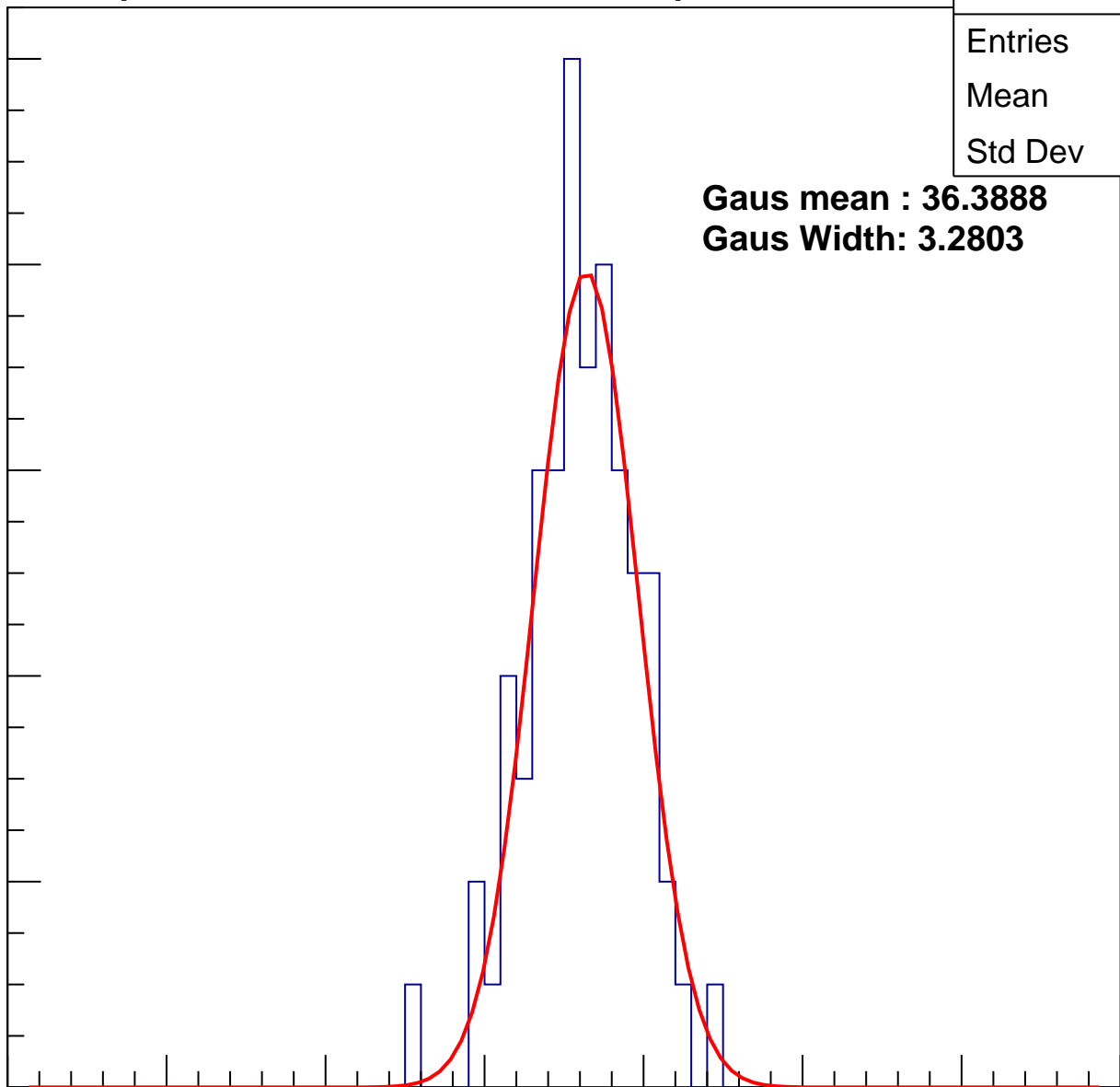
**Gaus Width: 3.2803**

Entry

10  
8  
6  
4  
2  
0

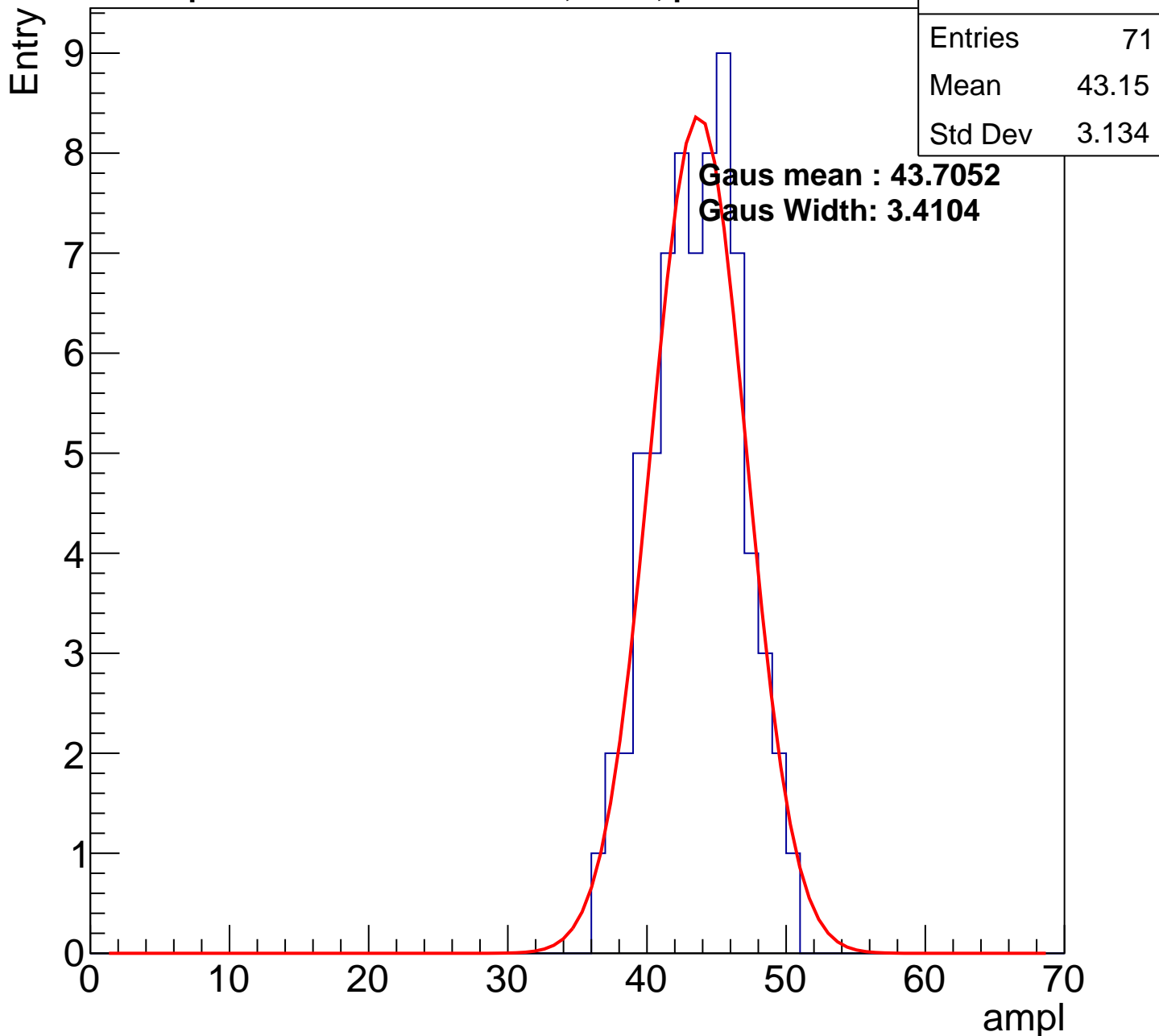
ampl

0 10 20 30 40 50 60 70



# B0L001S, U6-ch69, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

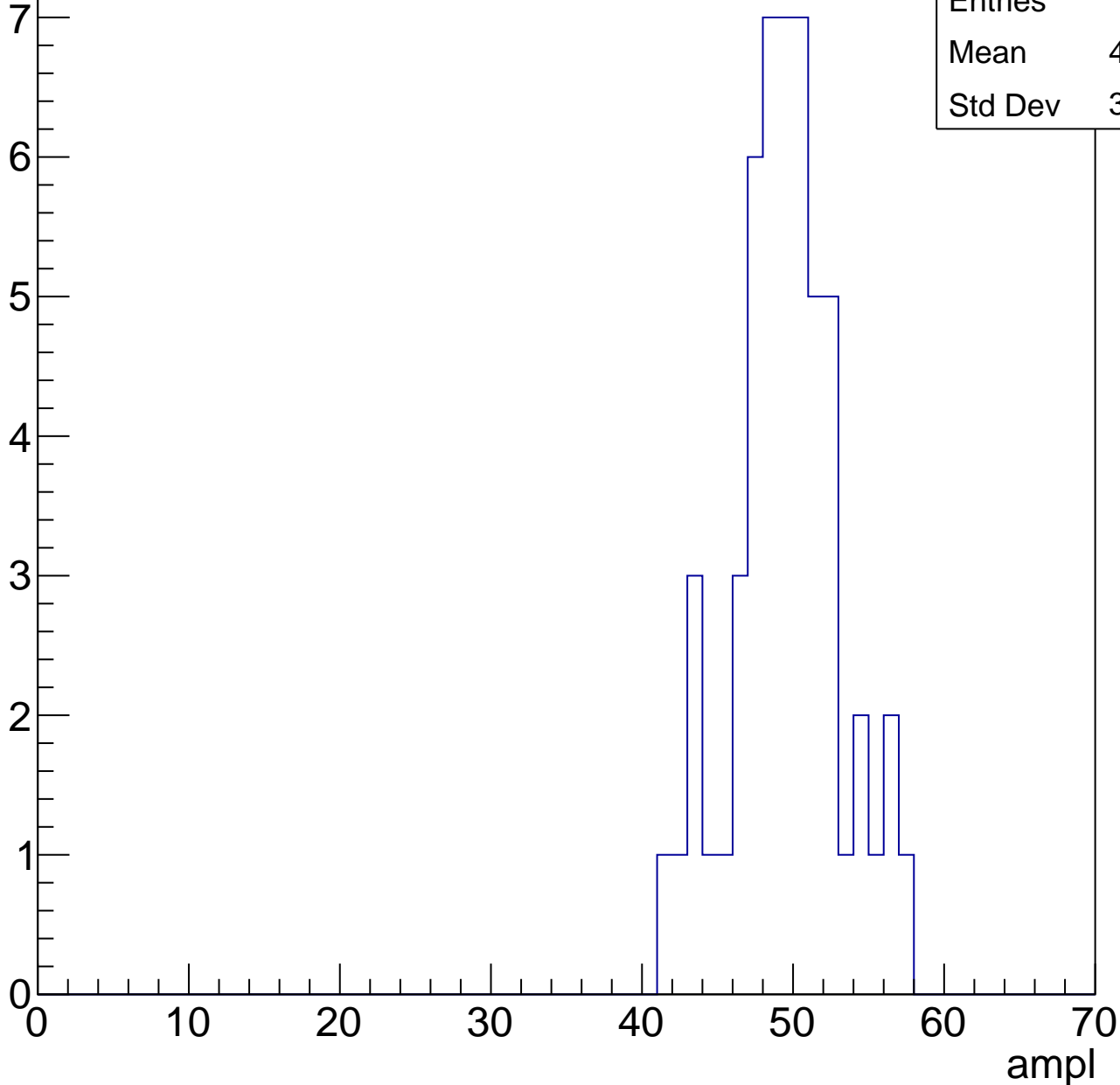


# B0L001S, U6-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	49.07
Std Dev	3.485

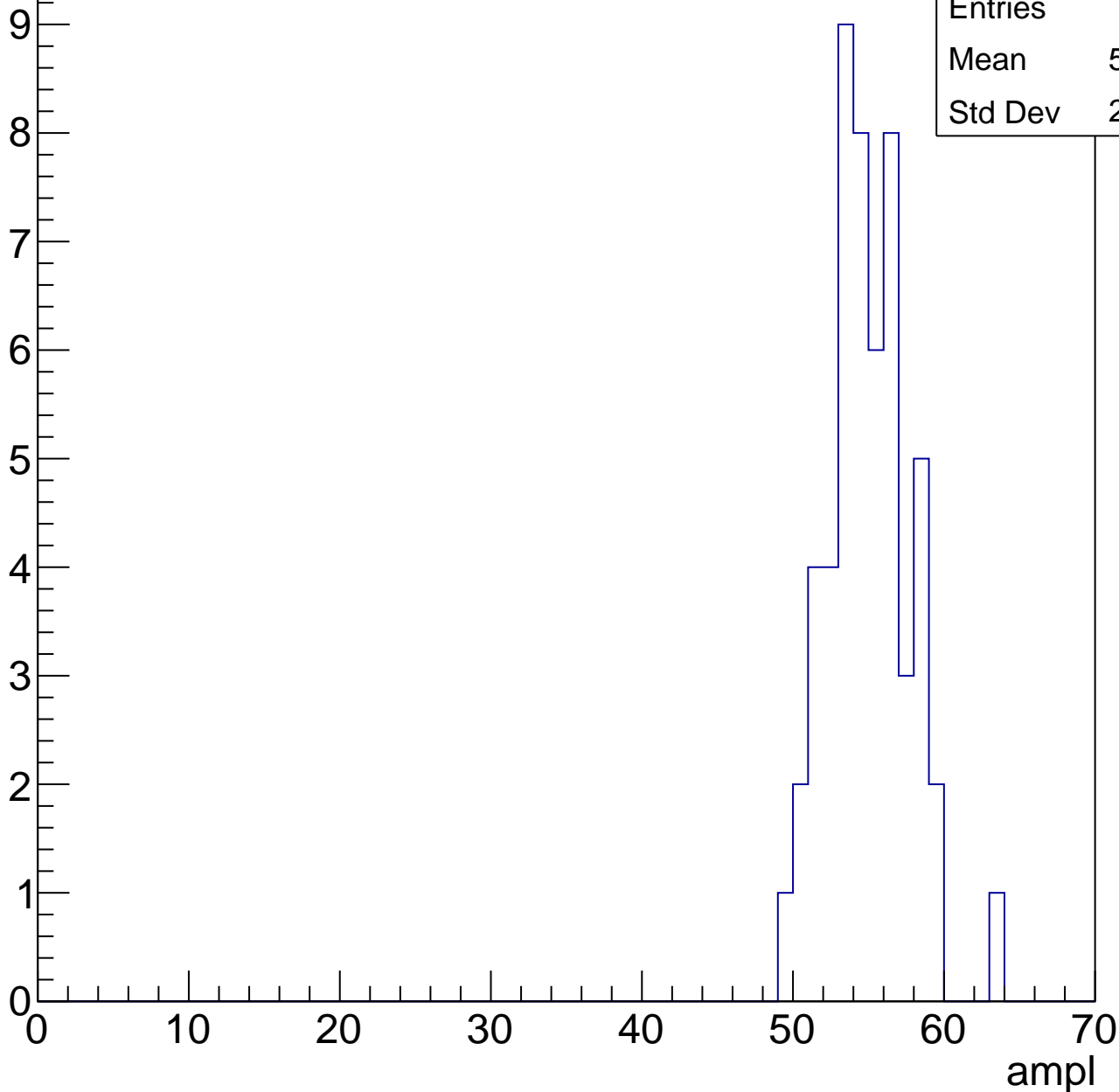


# B0L001S, U6-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	54.53
Std Dev	2.675

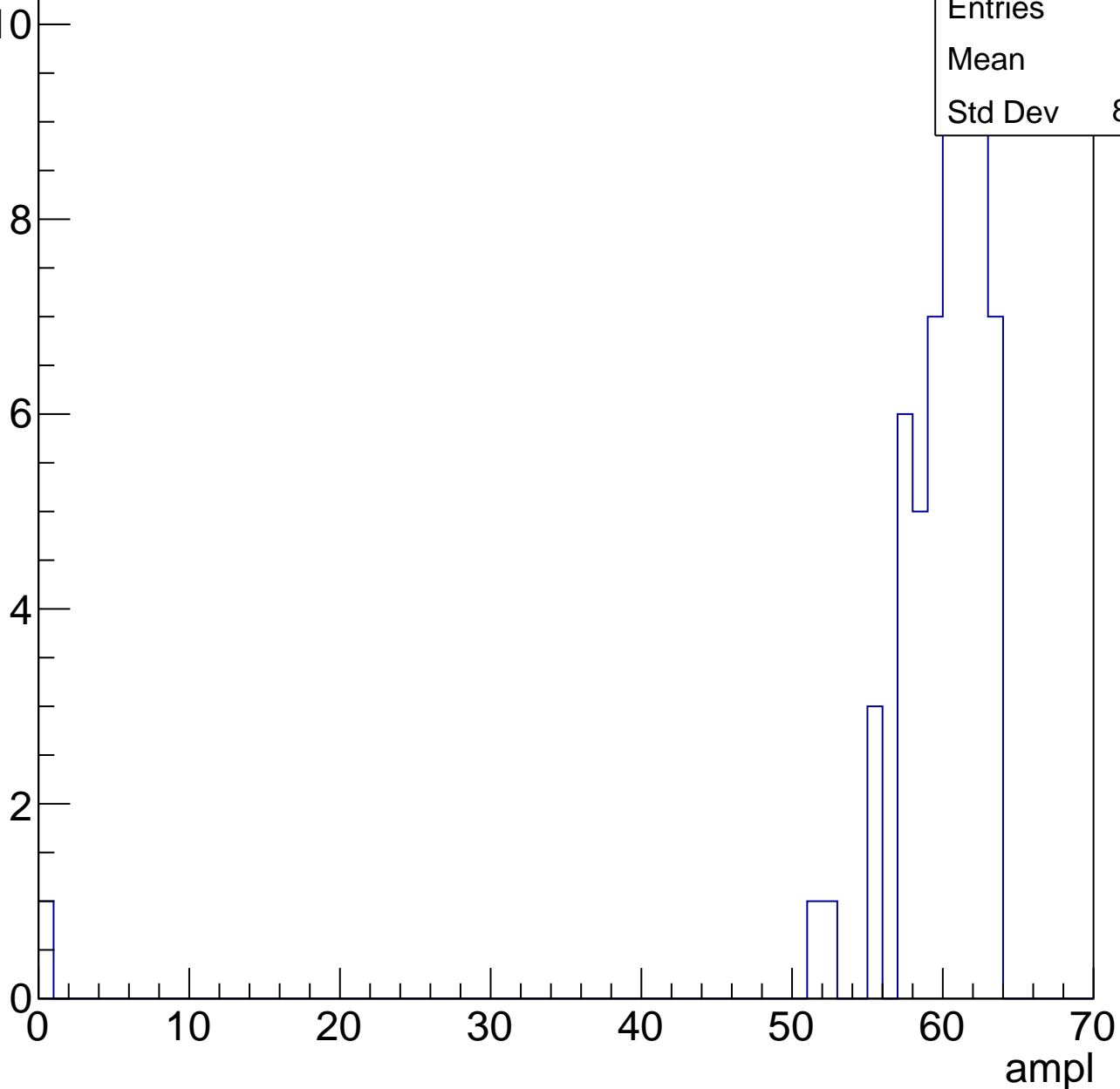


# B0L001S, U6-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	58.7
Std Dev	8.071



# B0L001S, U6-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch70, adc0

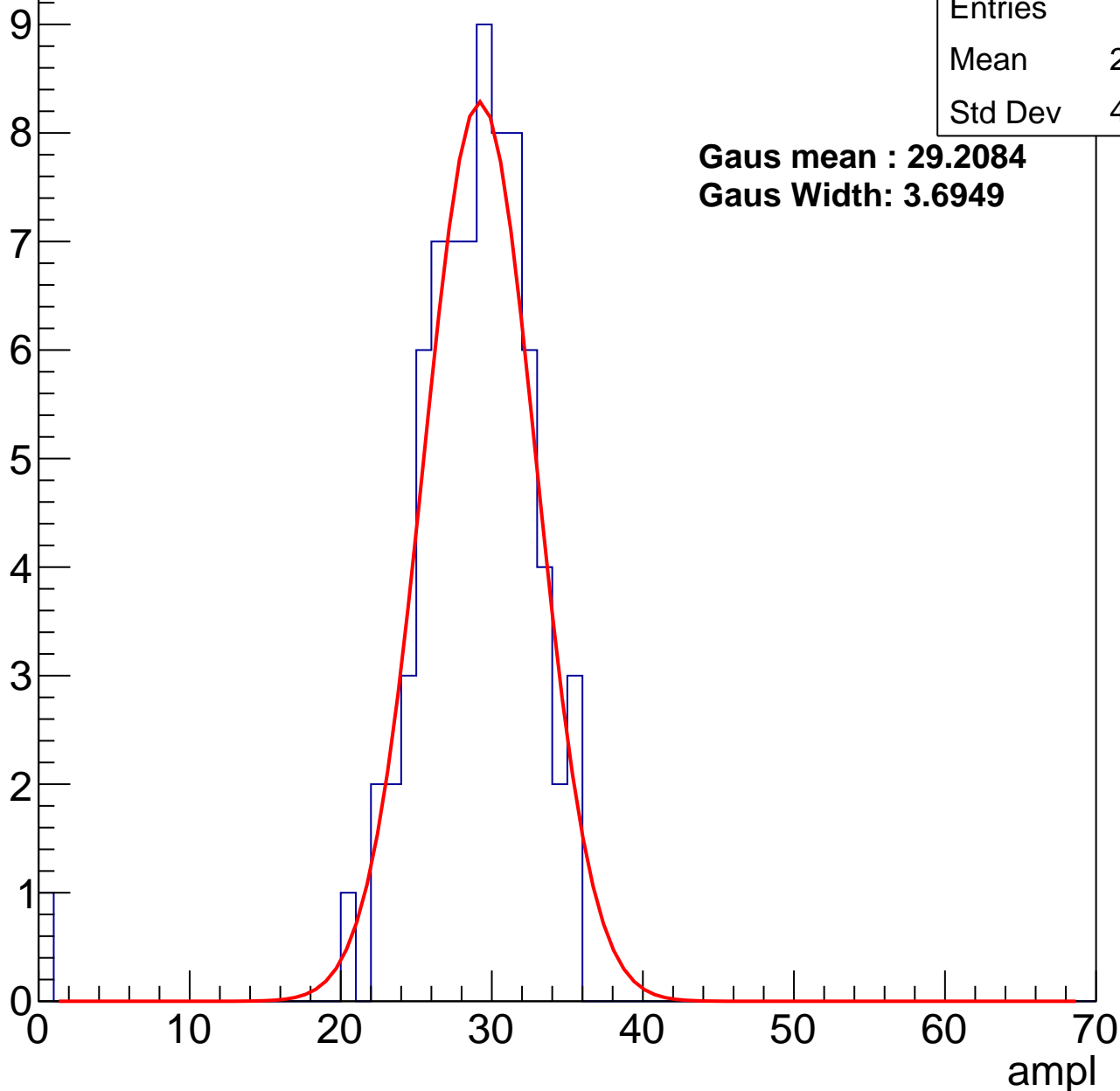
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	28.22
Std Dev	4.633

**Gaus mean : 29.2084**

**Gaus Width: 3.6949**



# B0L001S, U6-ch70, adc1

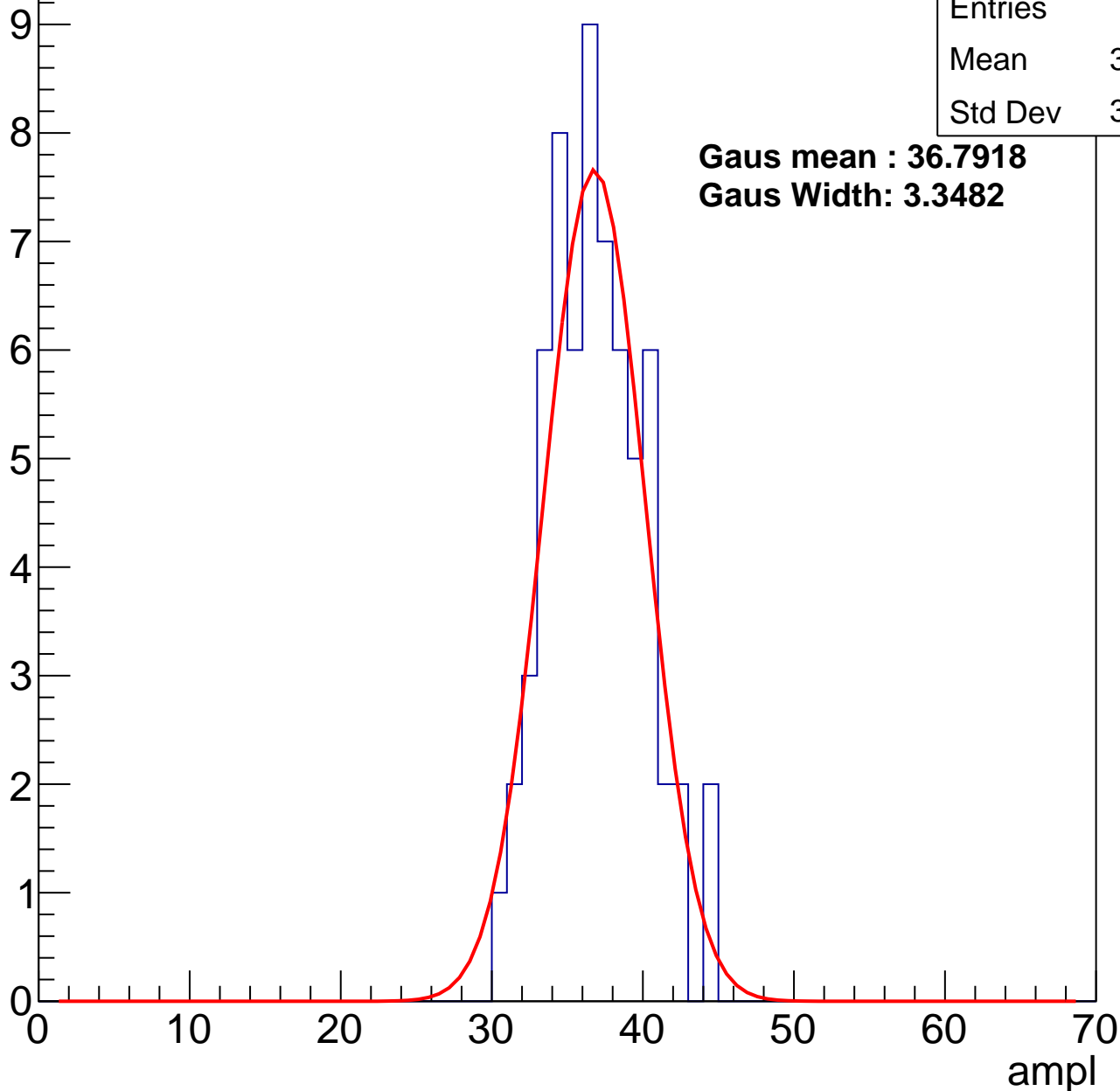
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	36.43
Std Dev	3.128

**Gaus mean : 36.7918**

**Gaus Width: 3.3482**



# B0L001S, U6-ch70, adc2

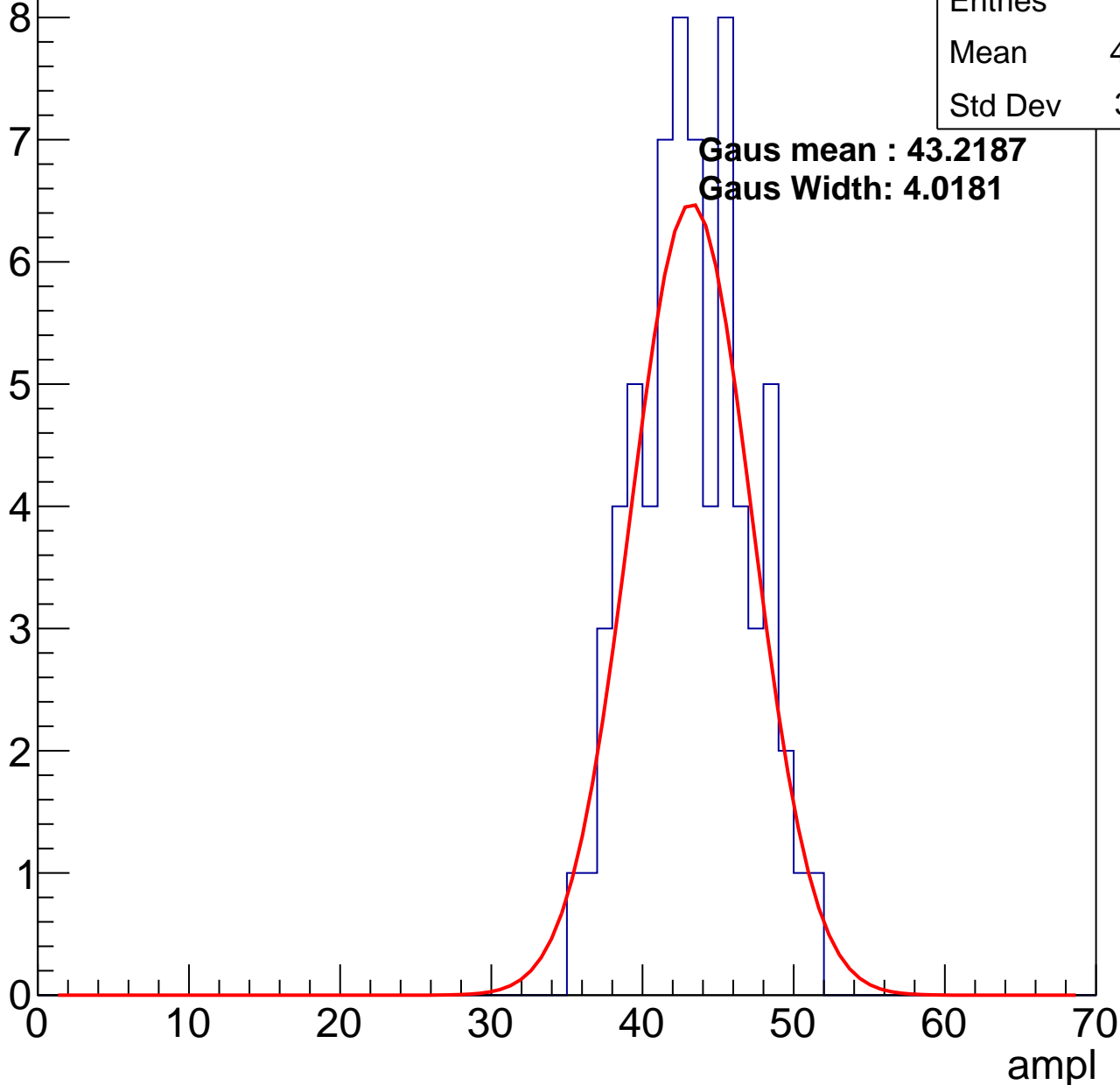
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	42.84
Std Dev	3.641

**Gaus mean : 43.2187**

**Gaus Width: 4.0181**

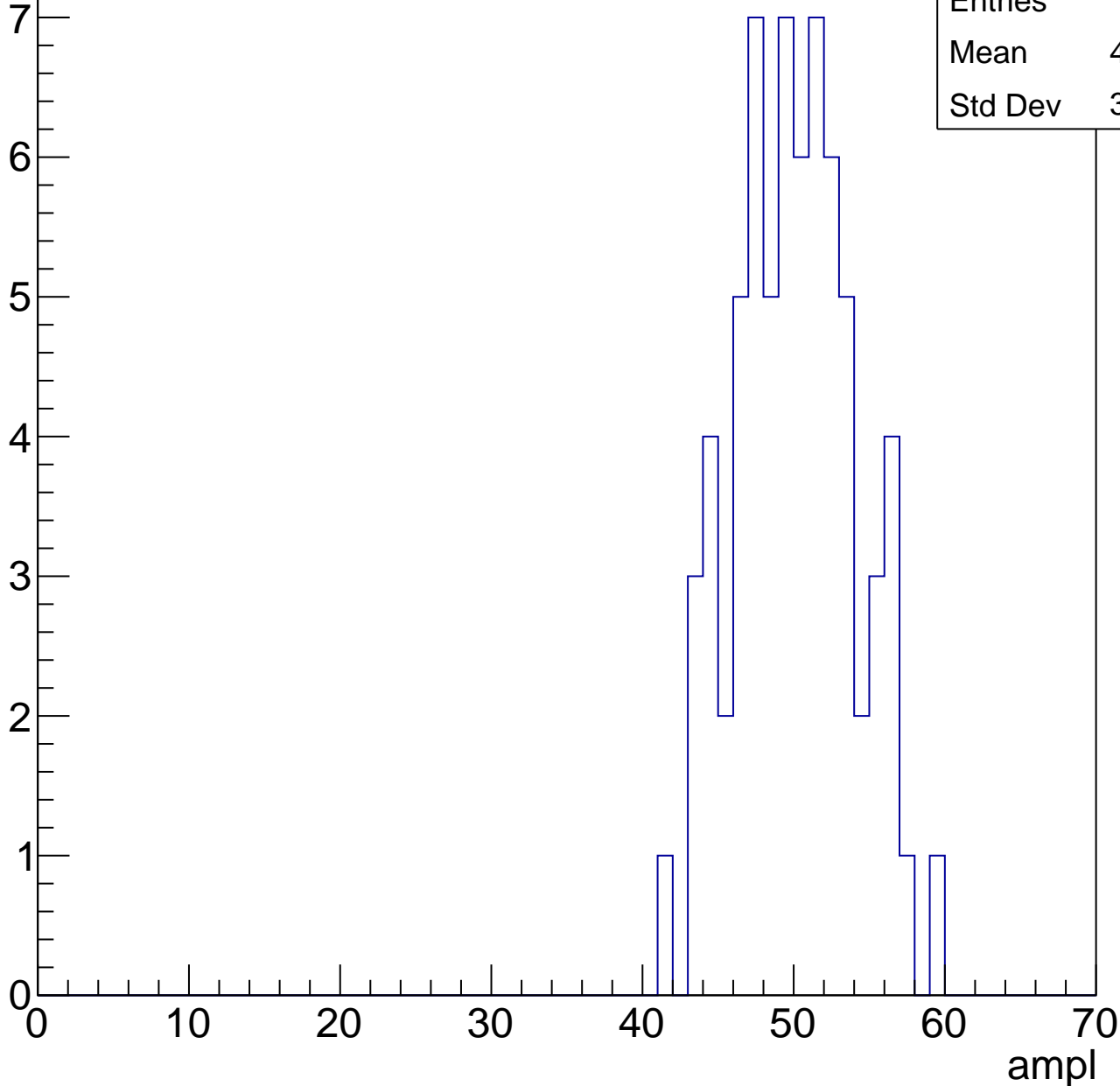


# B0L001S, U6-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

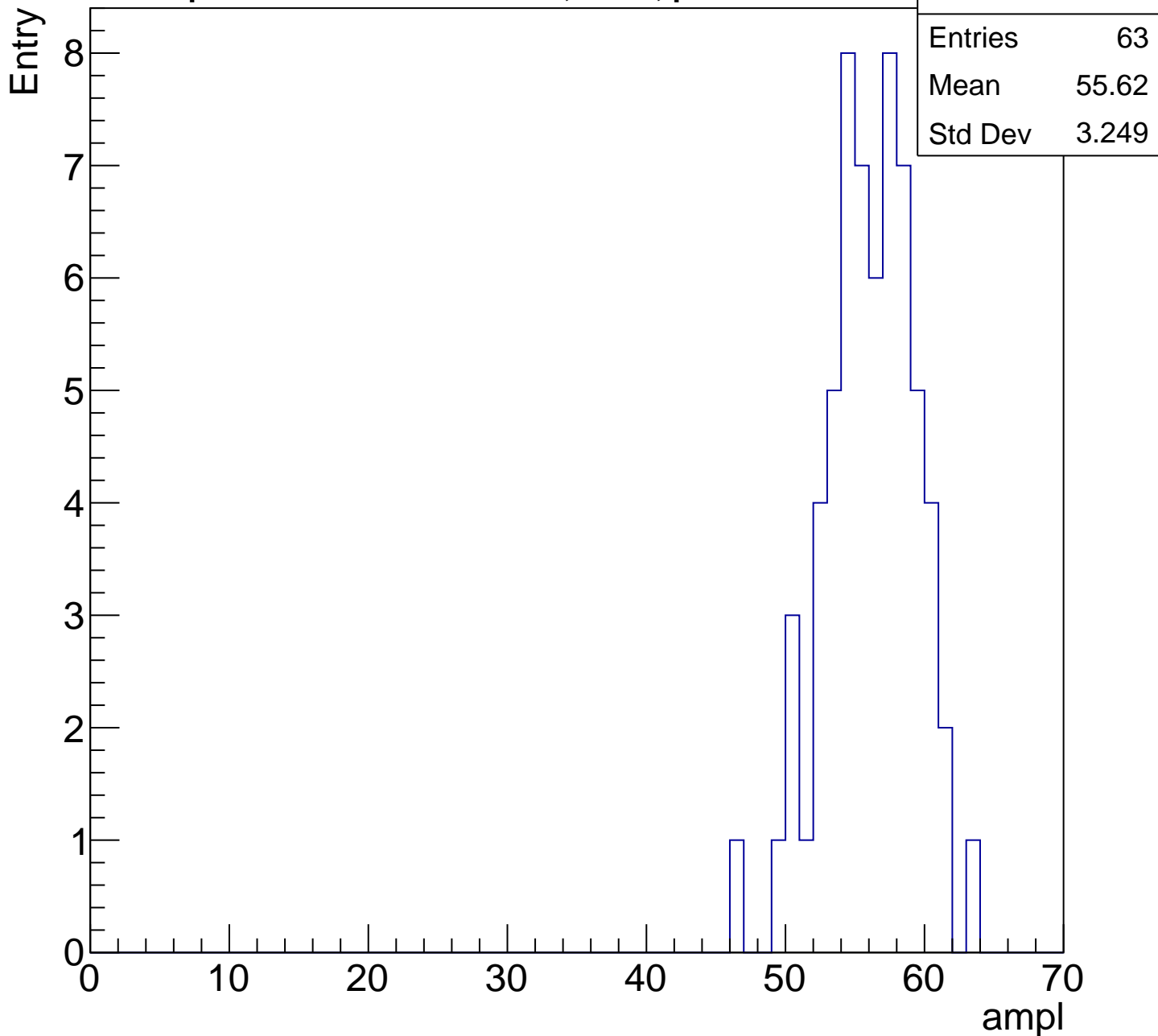
Entry

Entries	69
Mean	49.64
Std Dev	3.882



# B0L001S, U6-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

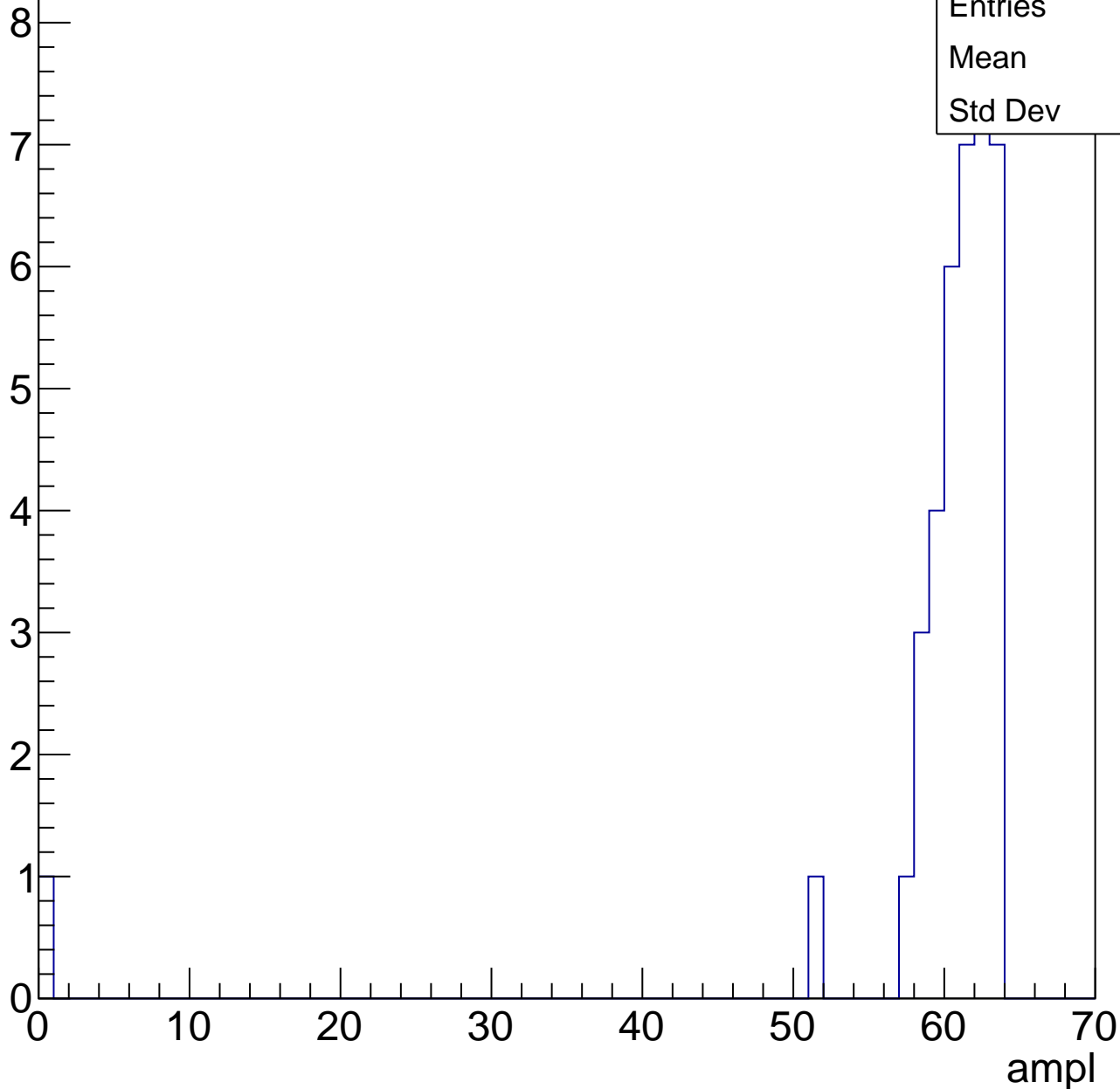


# B0L001S, U6-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	38
Mean	59
Std Dev	9.96



# B0L001S, U6-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	62.2
Std Dev	0.7483

ampl

0 10 20 30 40 50 60 70



# B0L001S, U6-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch71, adc0

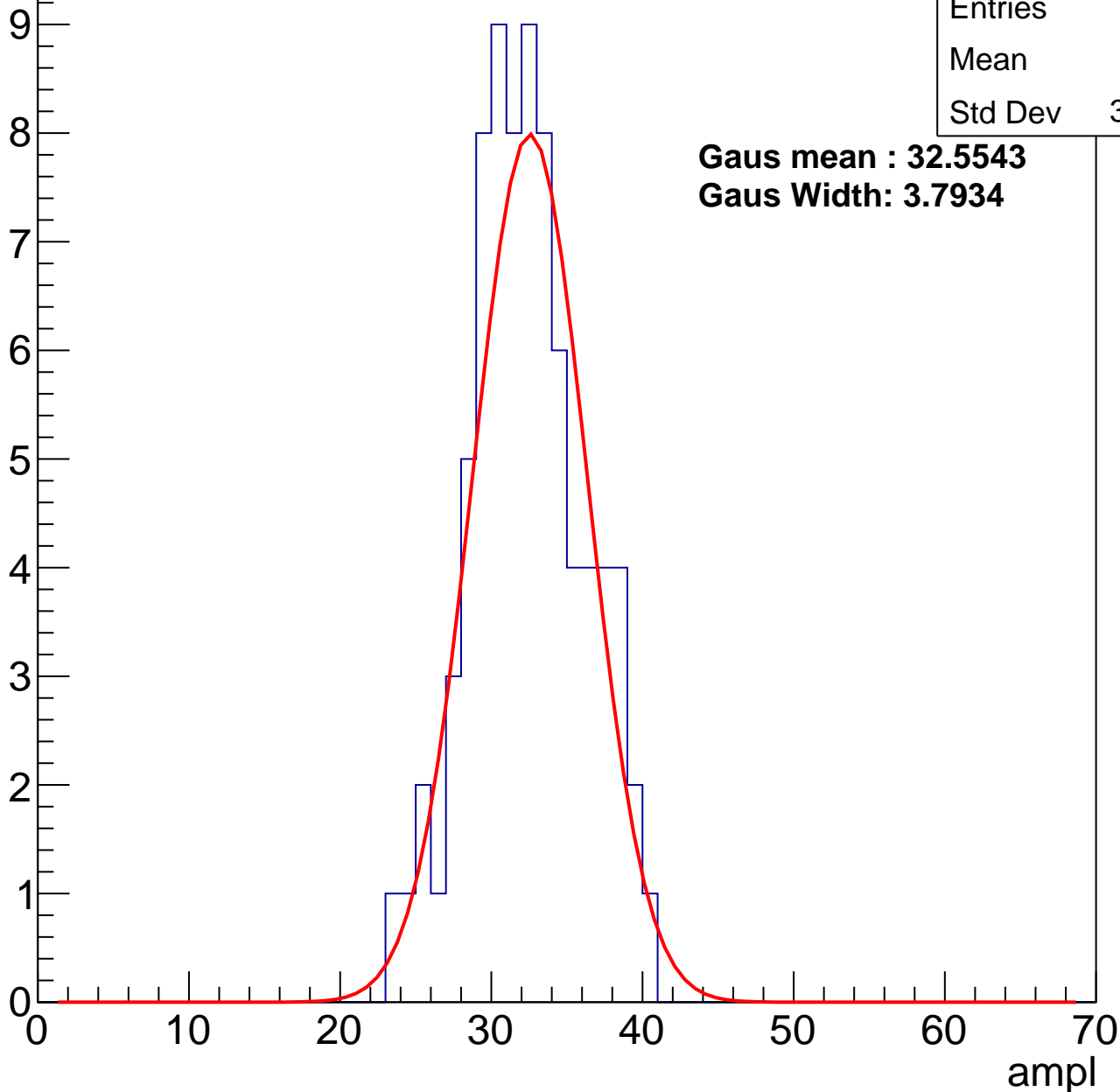
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	80
Mean	31.9
Std Dev	3.686

**Gaus mean : 32.5543**

**Gaus Width: 3.7934**



# B0L001S, U6-ch71, adc1

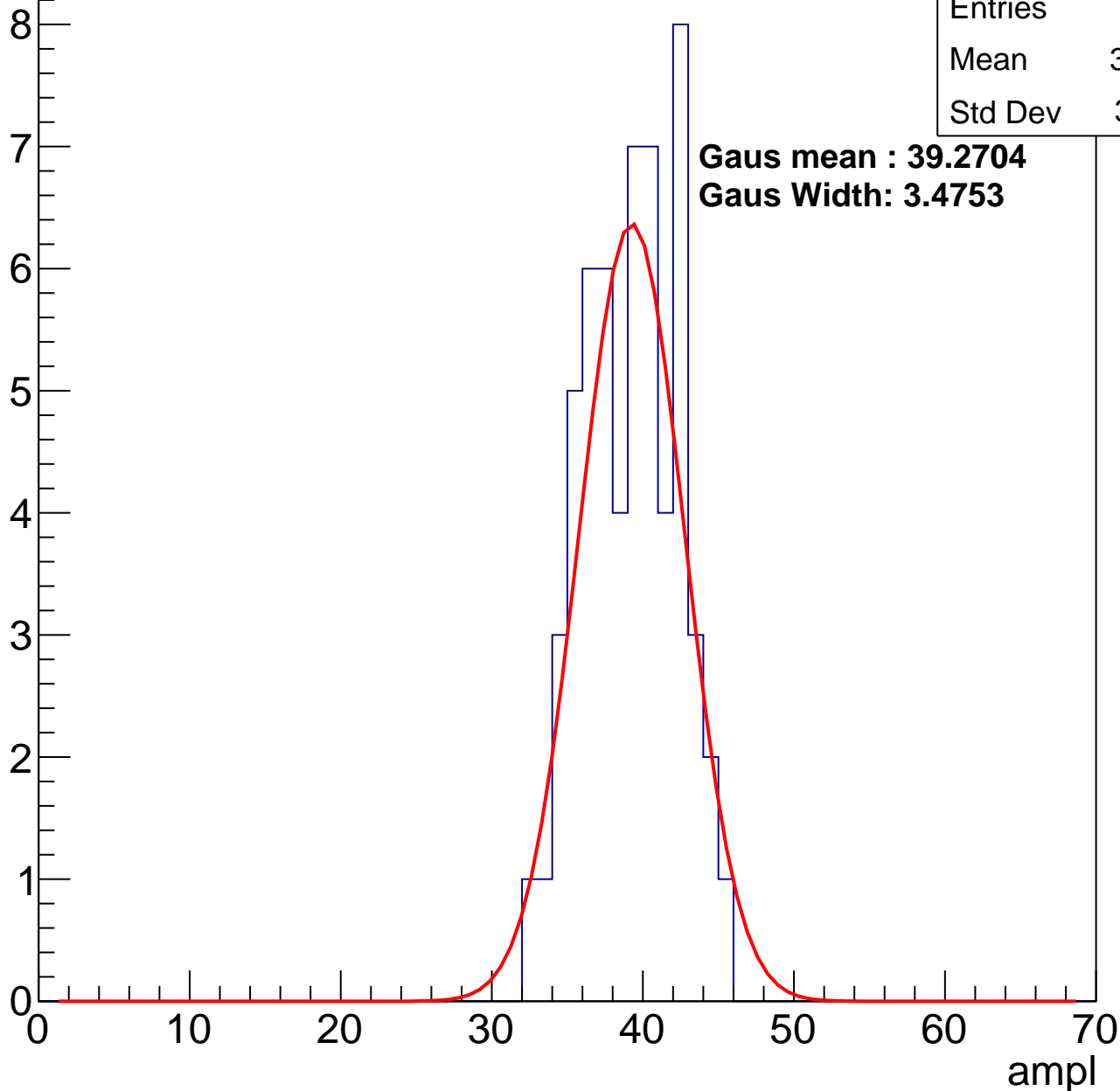
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	38.74
Std Dev	3.071

**Gaus mean : 39.2704**

**Gaus Width: 3.4753**



# B0L001S, U6-ch71, adc2

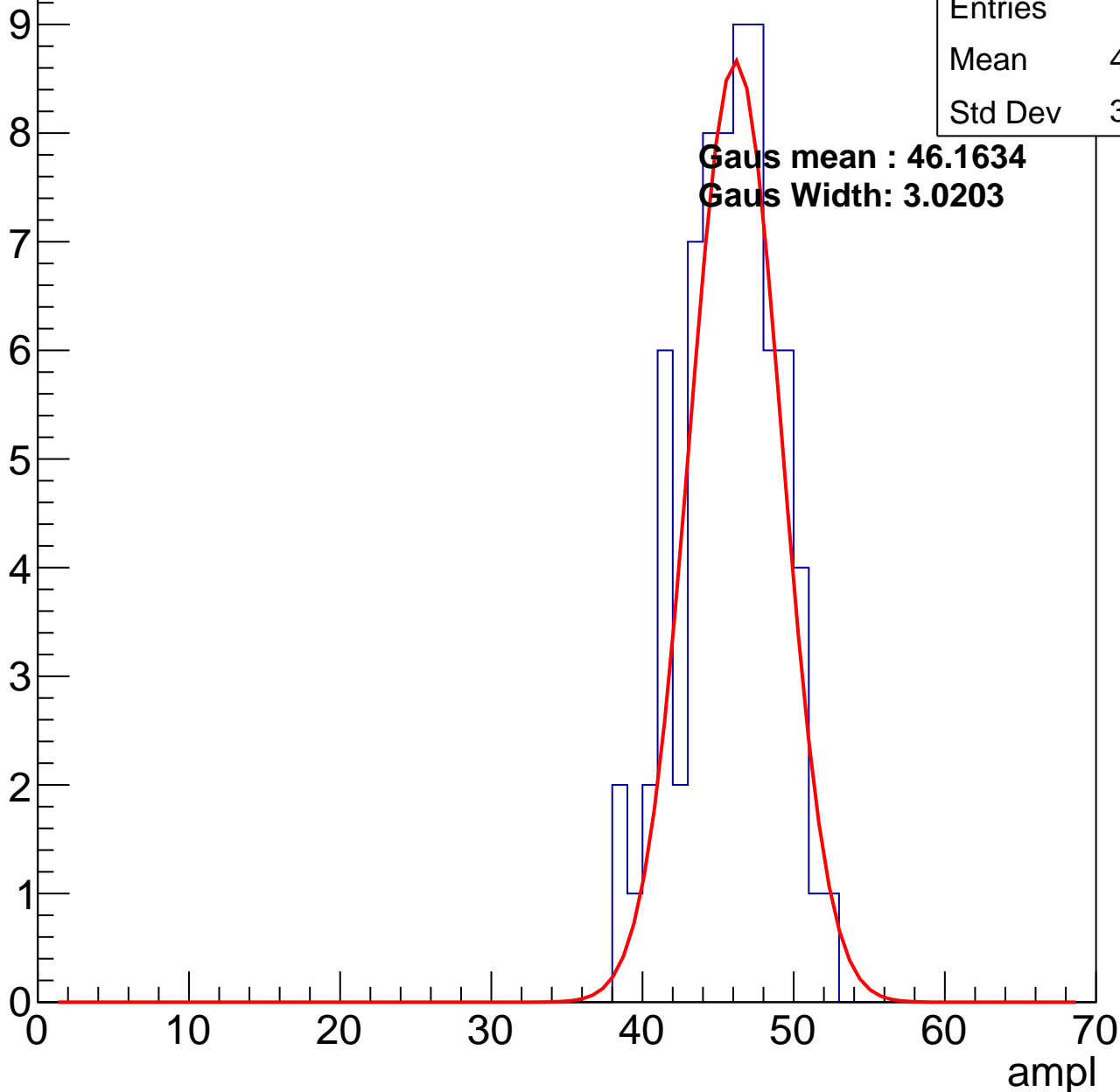
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	45.28
Std Dev	3.137

**Gaus mean : 46.1634**

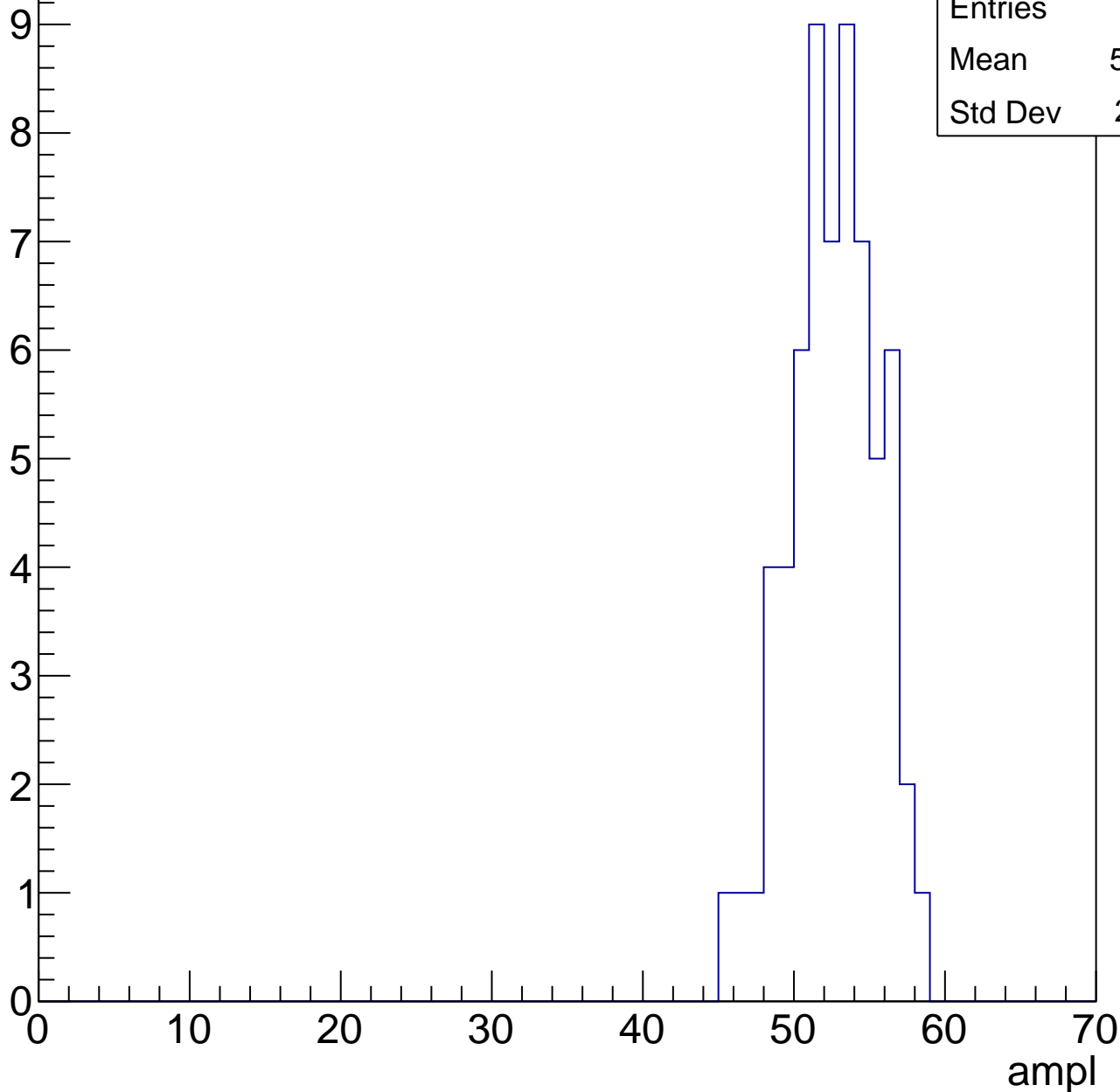
**Gaus Width: 3.0203**



# B0L001S, U6-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

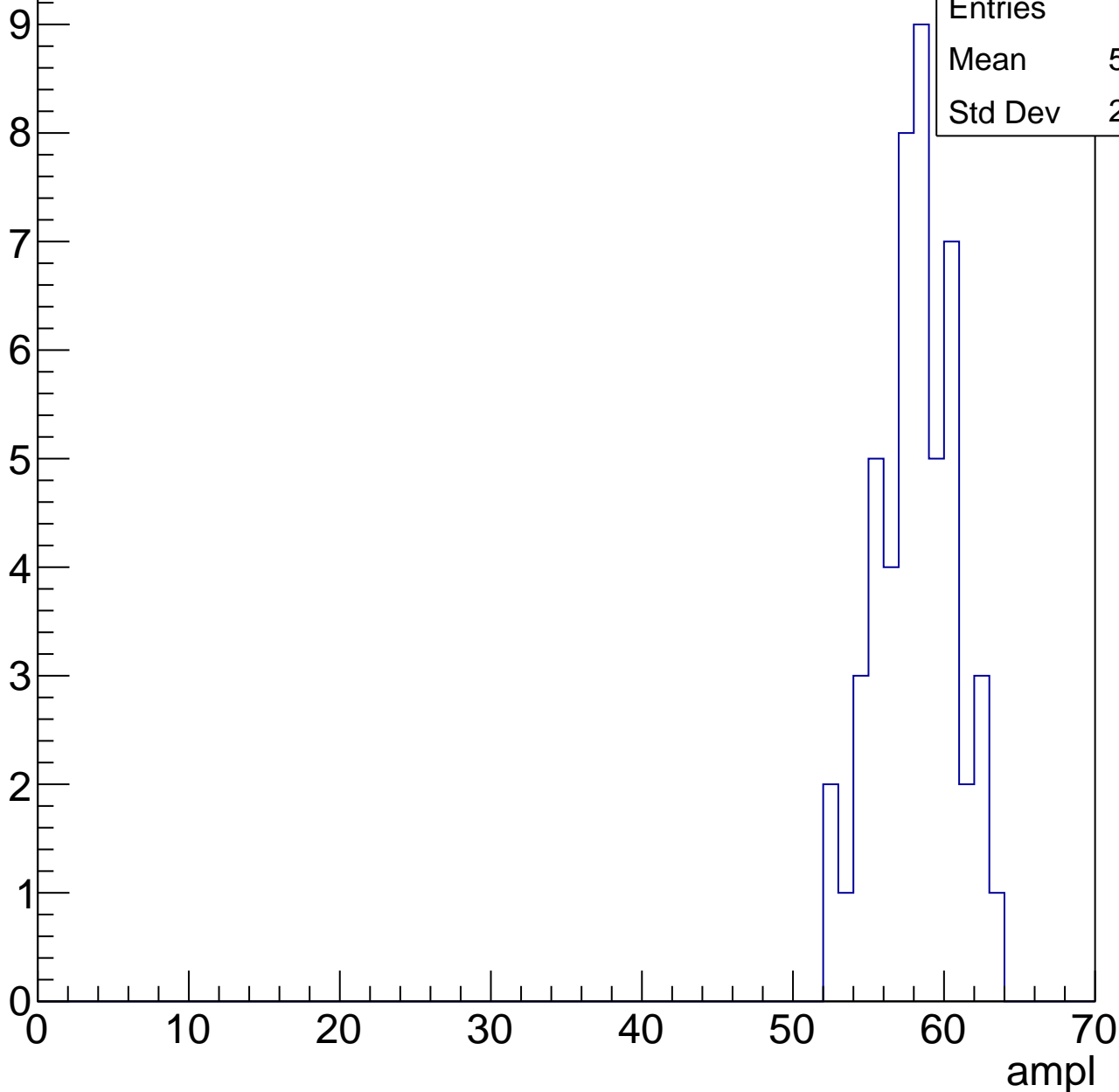


# B0L001S, U6-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

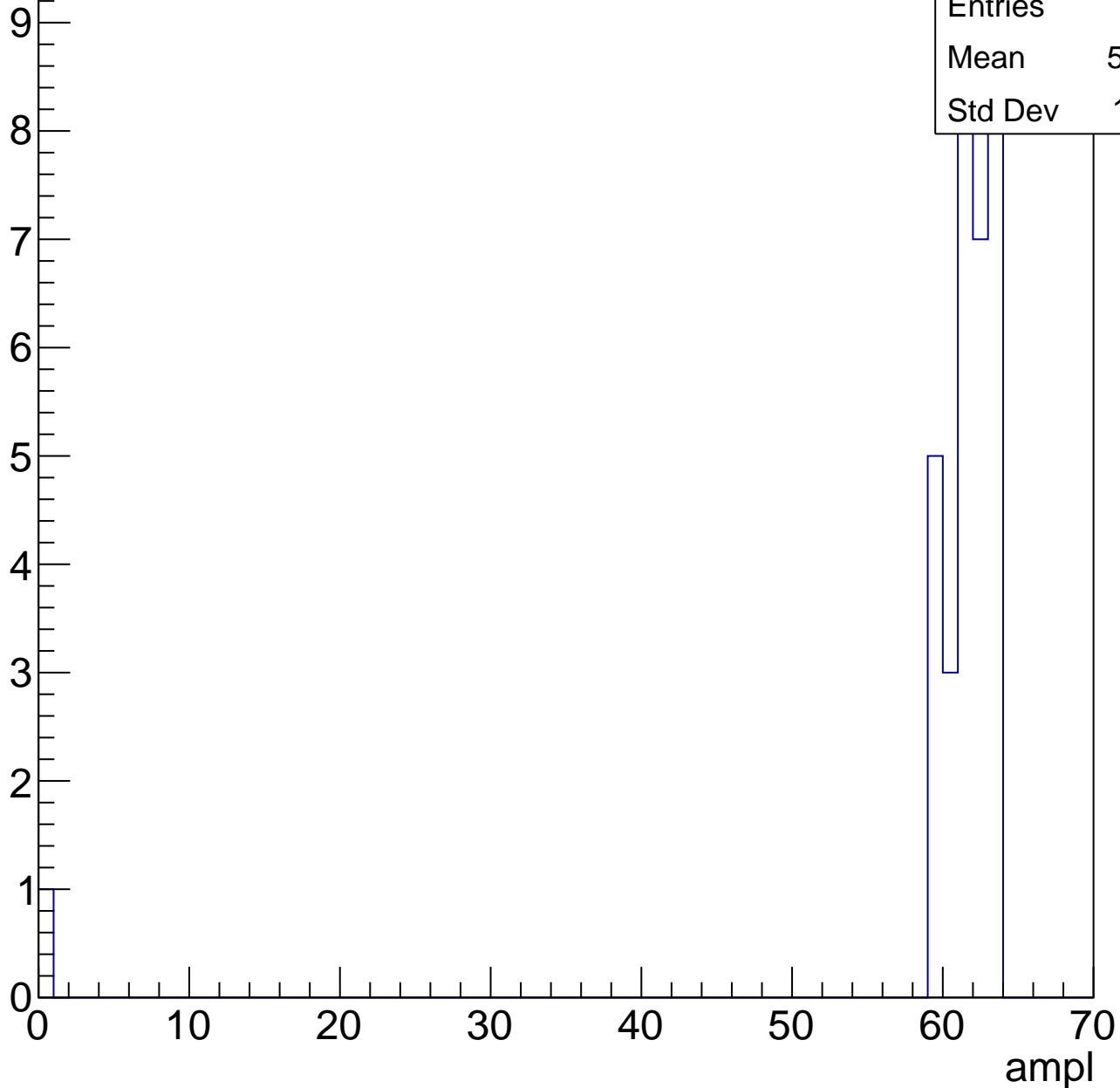
Entries	50
Mean	57.64
Std Dev	2.575



# B0L001S, U6-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U6-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U6-ch72, adc0

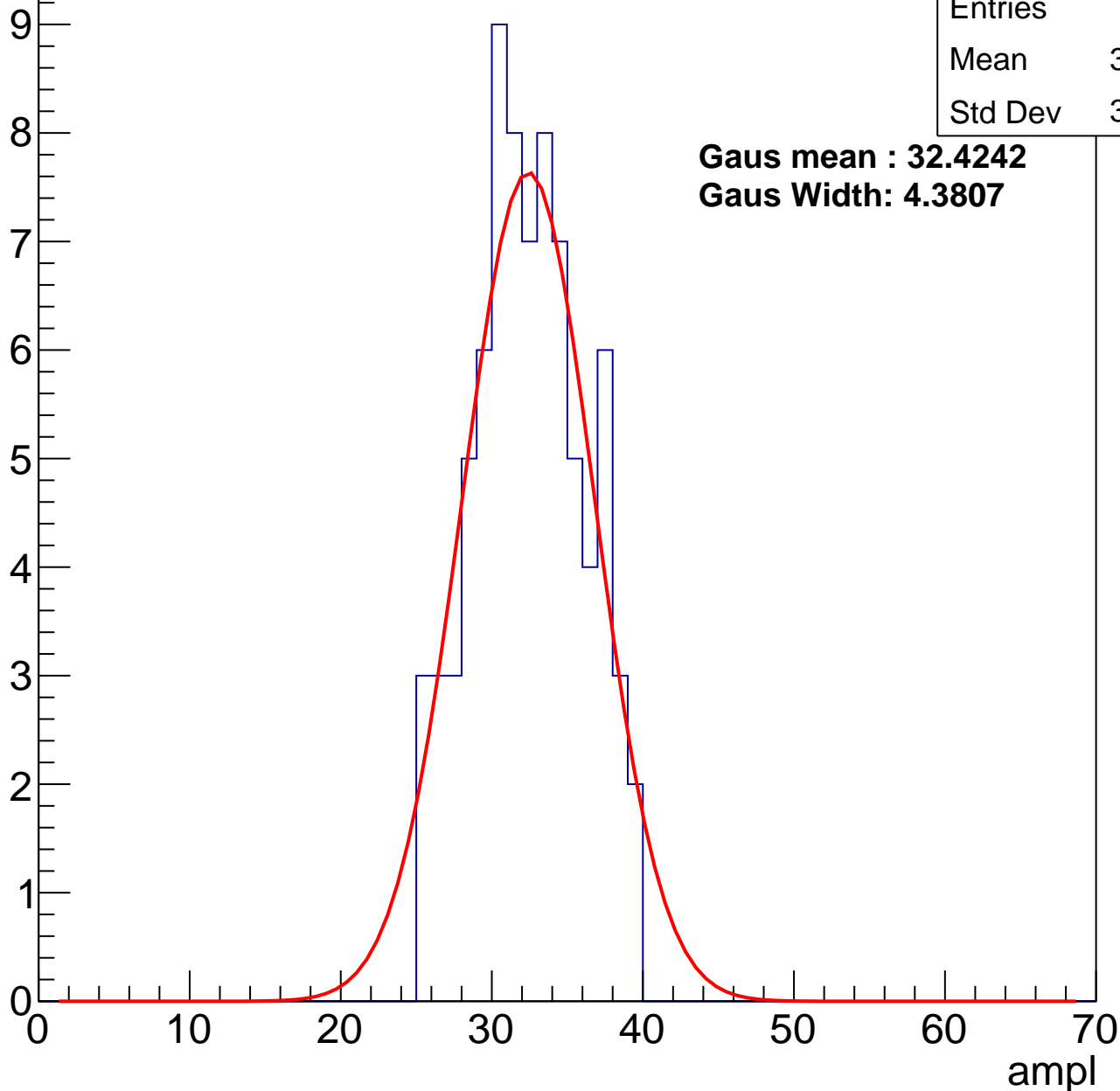
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	31.96
Std Dev	3.574

**Gaus mean : 32.4242**

**Gaus Width: 4.3807**



# B0L001S, U6-ch72, adc1

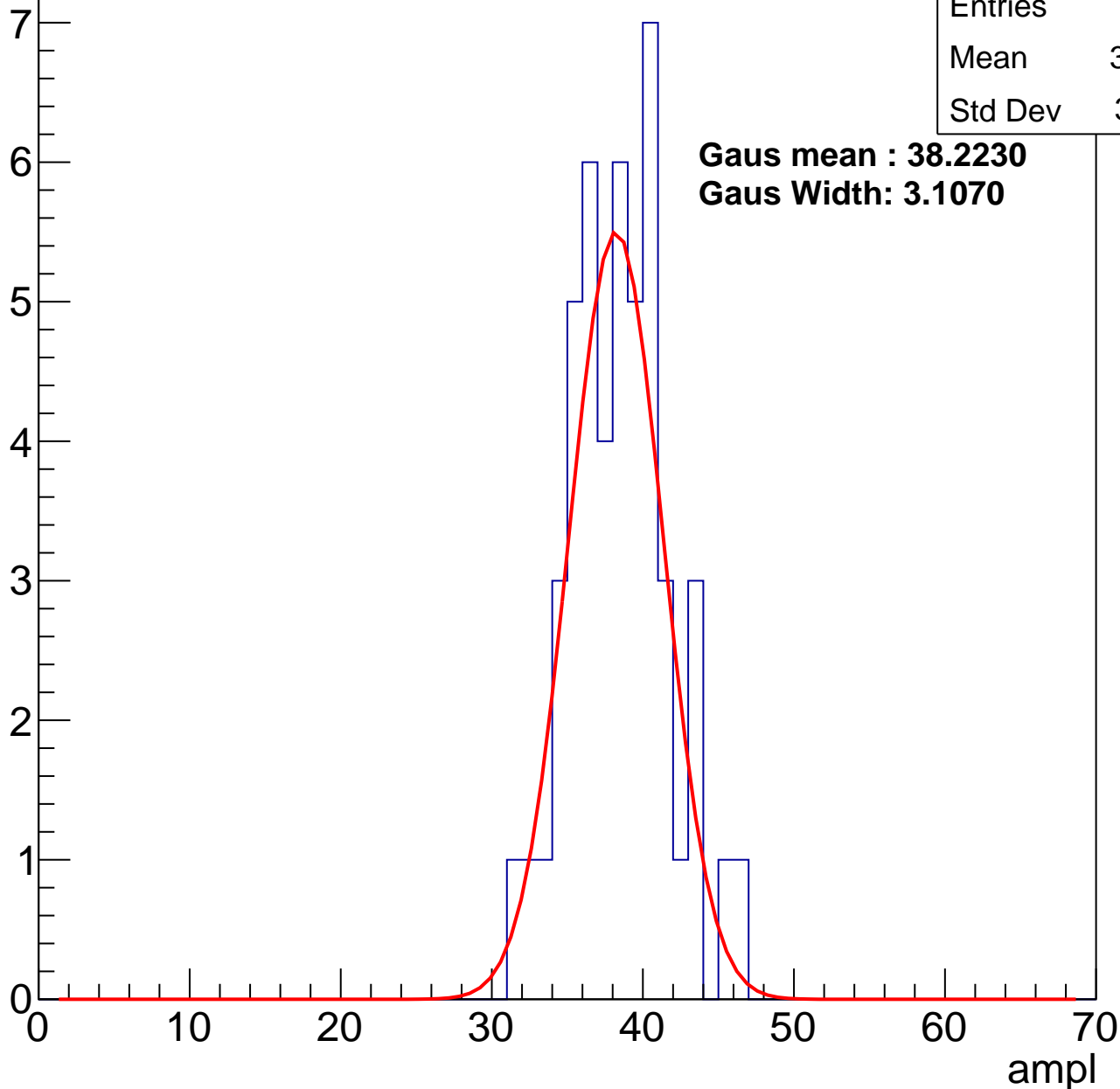
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	38.02
Std Dev	3.211

**Gaus mean : 38.2230**

**Gaus Width: 3.1070**



# B0L001S, U6-ch72, adc2

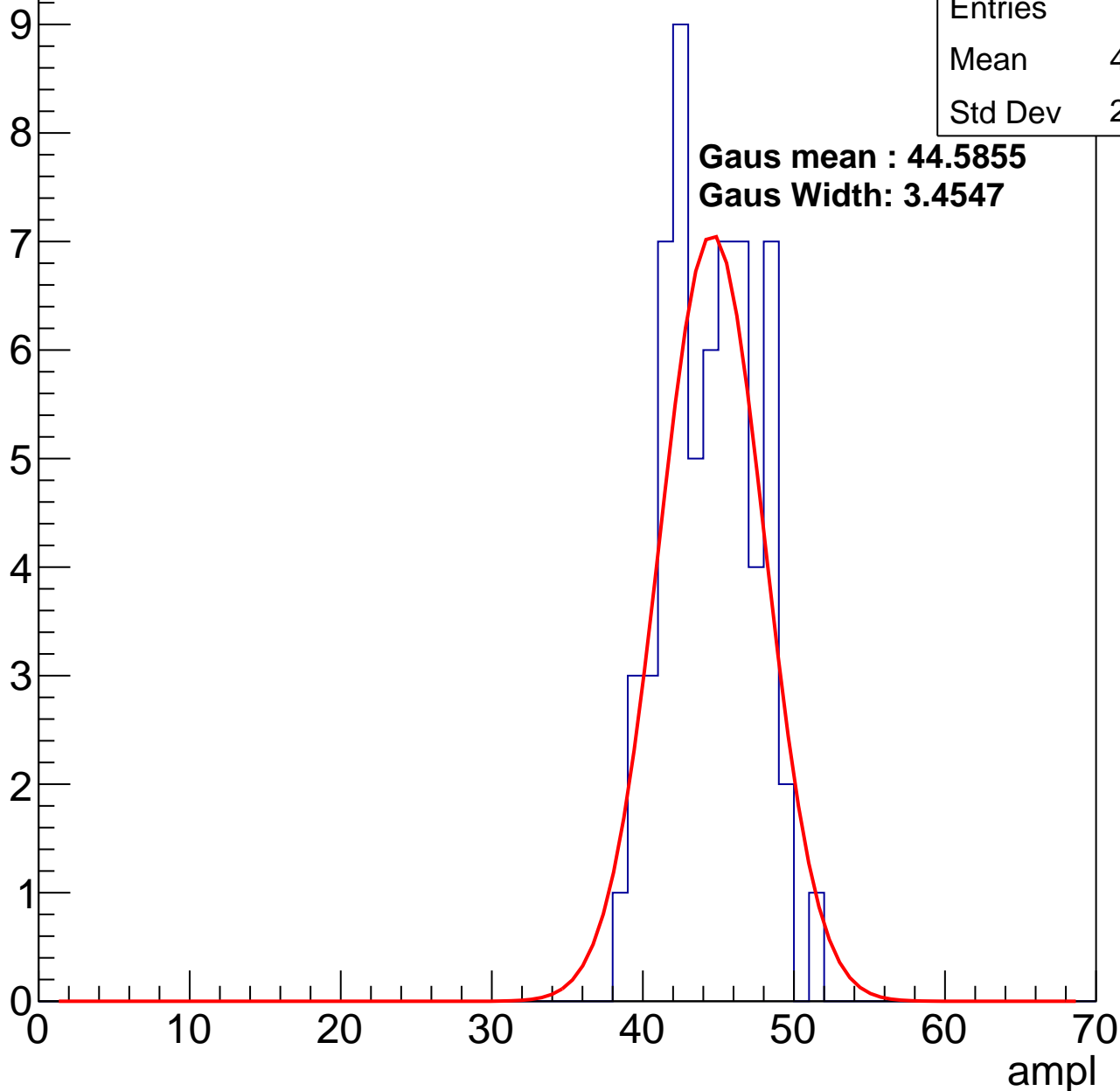
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	44.02
Std Dev	2.965

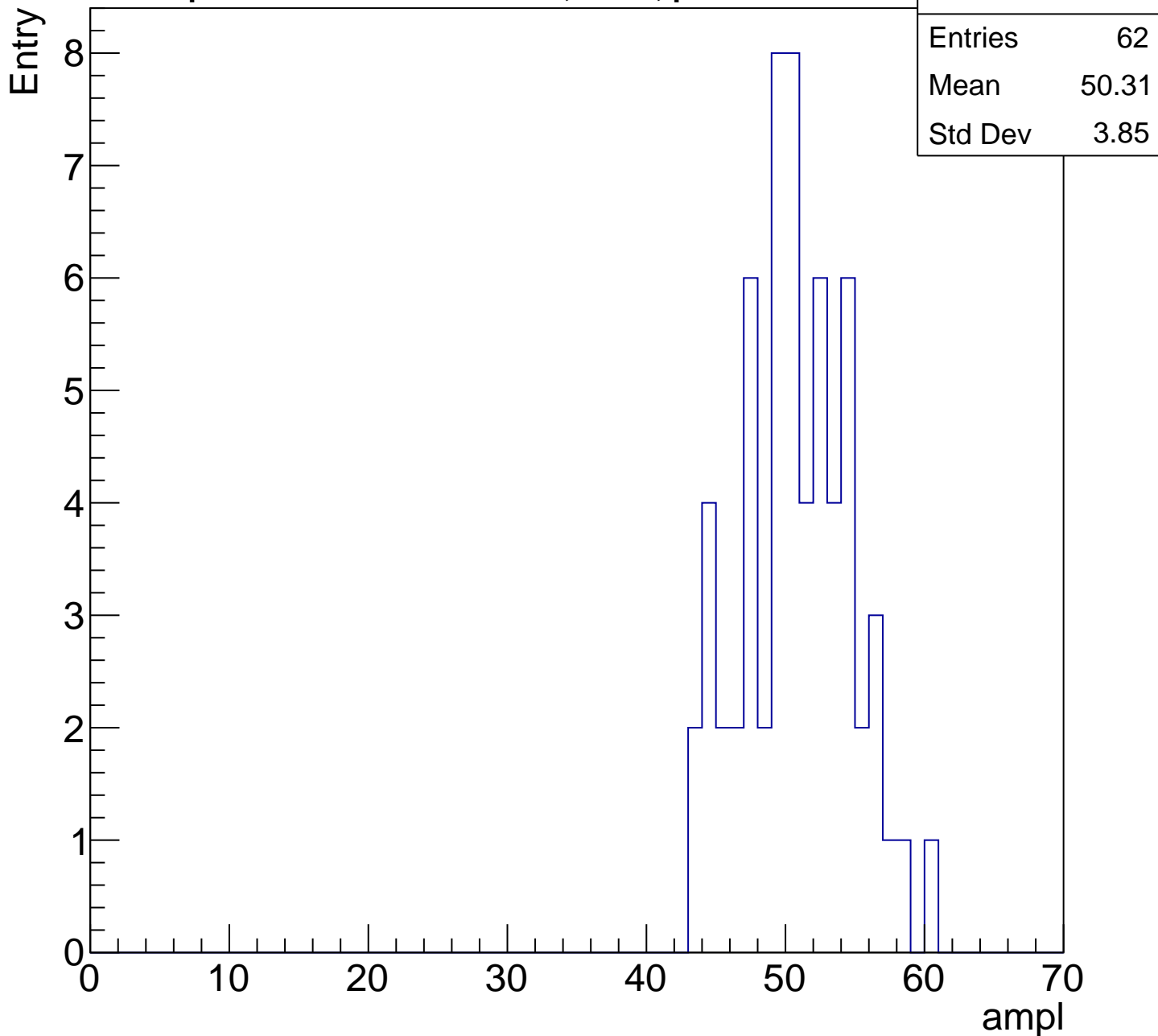
**Gaus mean : 44.5855**

**Gaus Width: 3.4547**



# B0L001S, U6-ch72, adc3

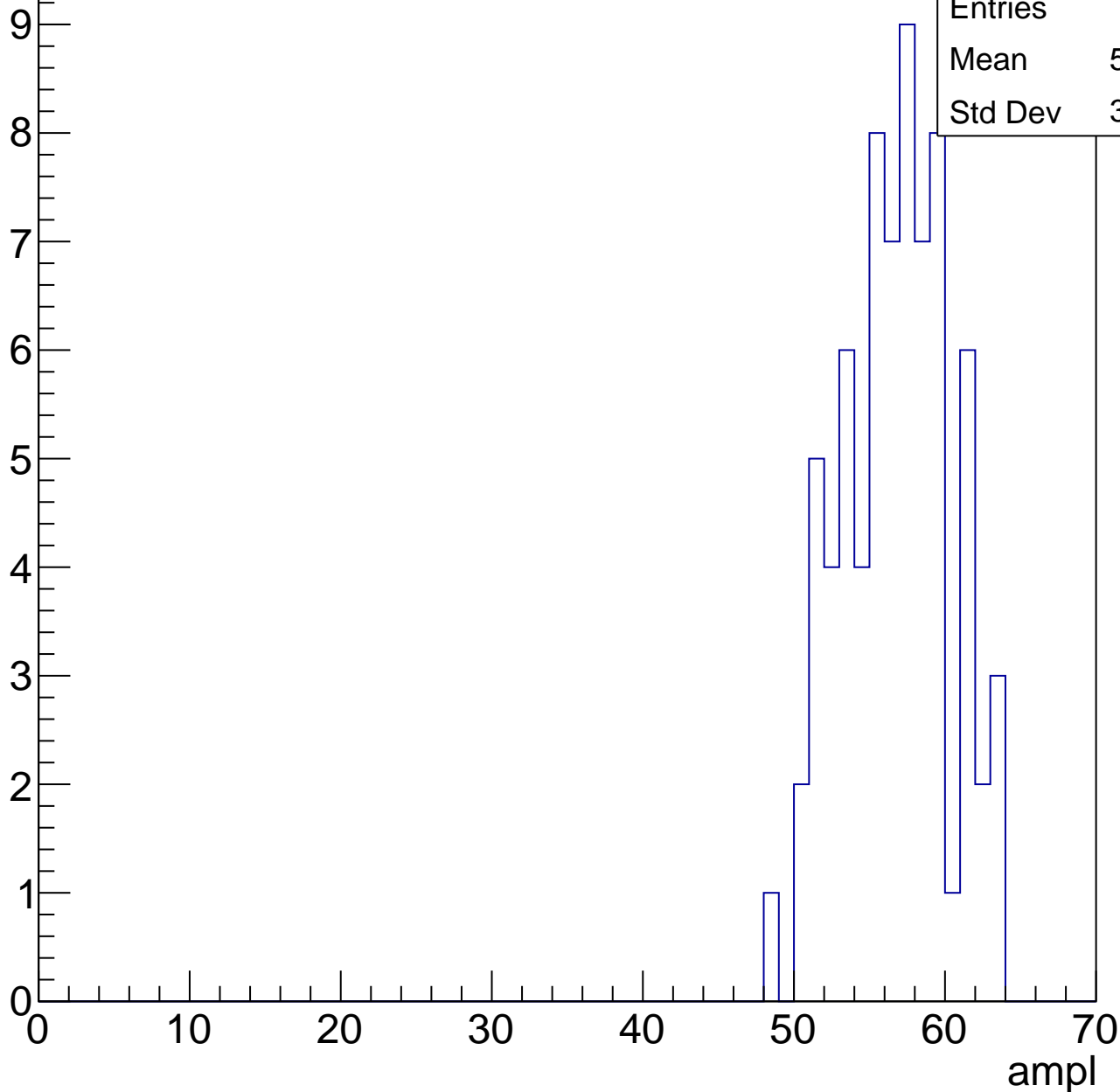
calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U6-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	31
Mean	59.1
Std Dev	10.89

ampl

0

10

20

30

40

50

60

70

# B0L001S, U6-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch73, adc0

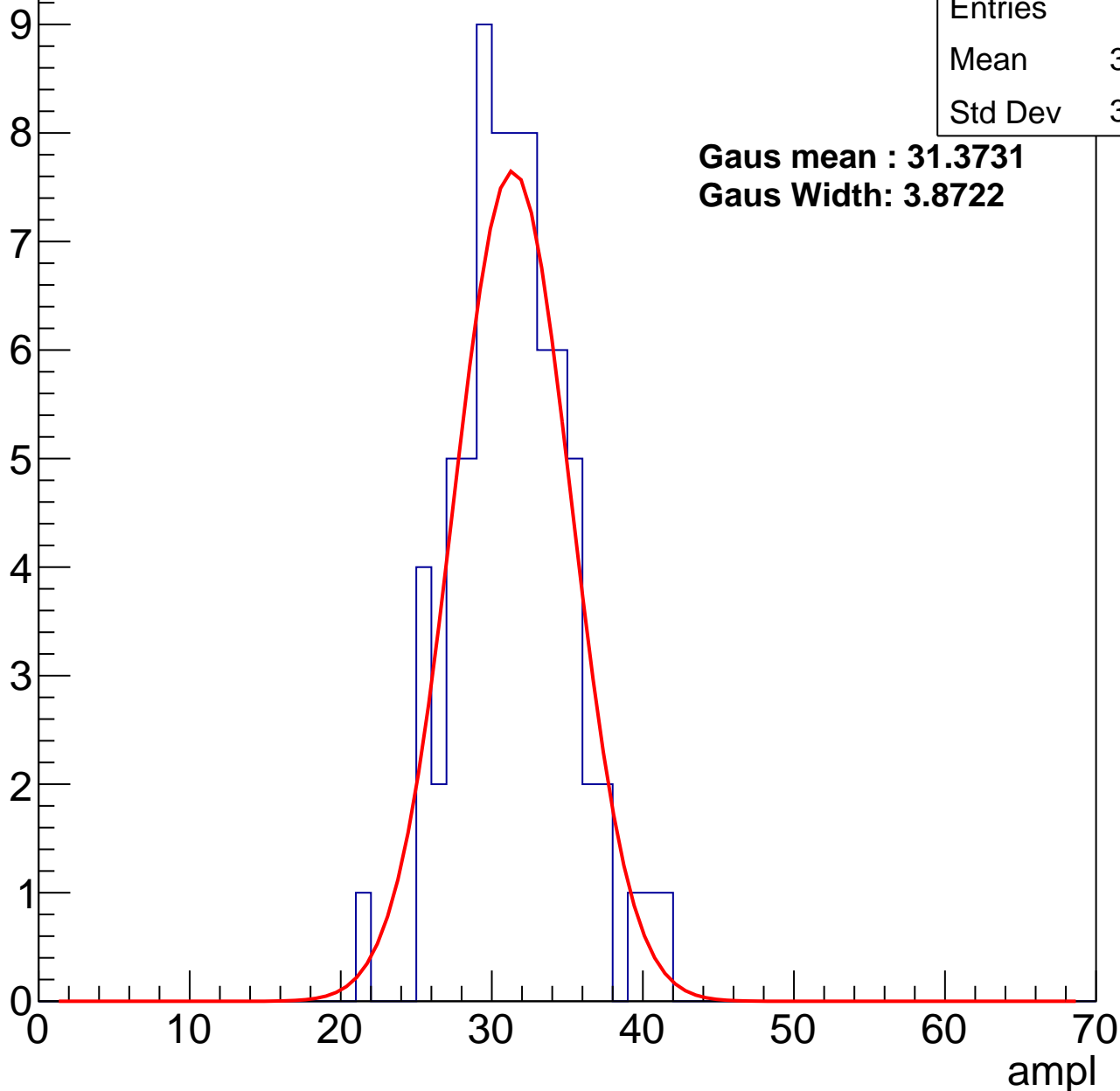
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	31.03
Std Dev	3.669

**Gaus mean : 31.3731**

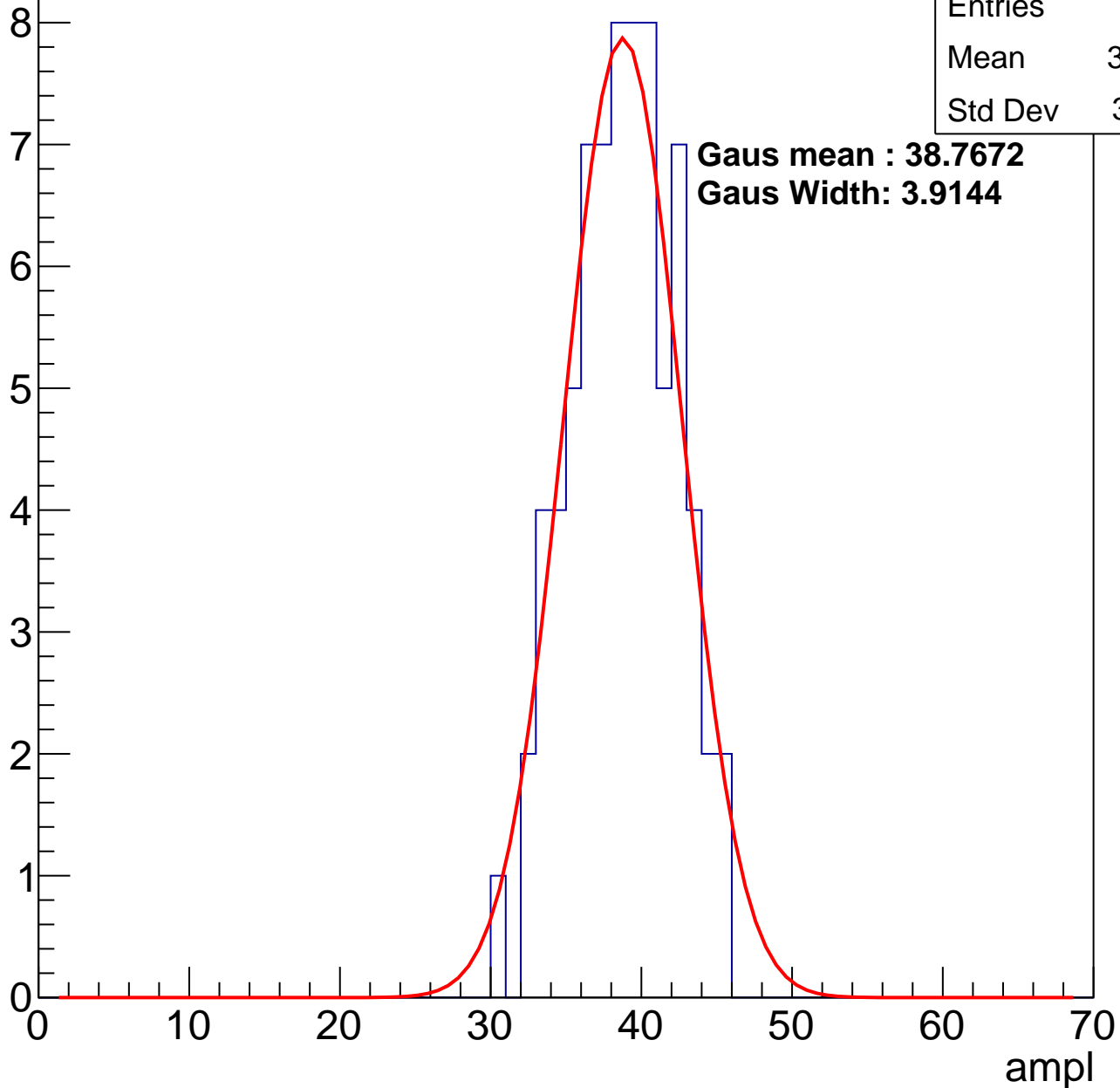
**Gaus Width: 3.8722**



# B0L001S, U6-ch73, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch73, adc2

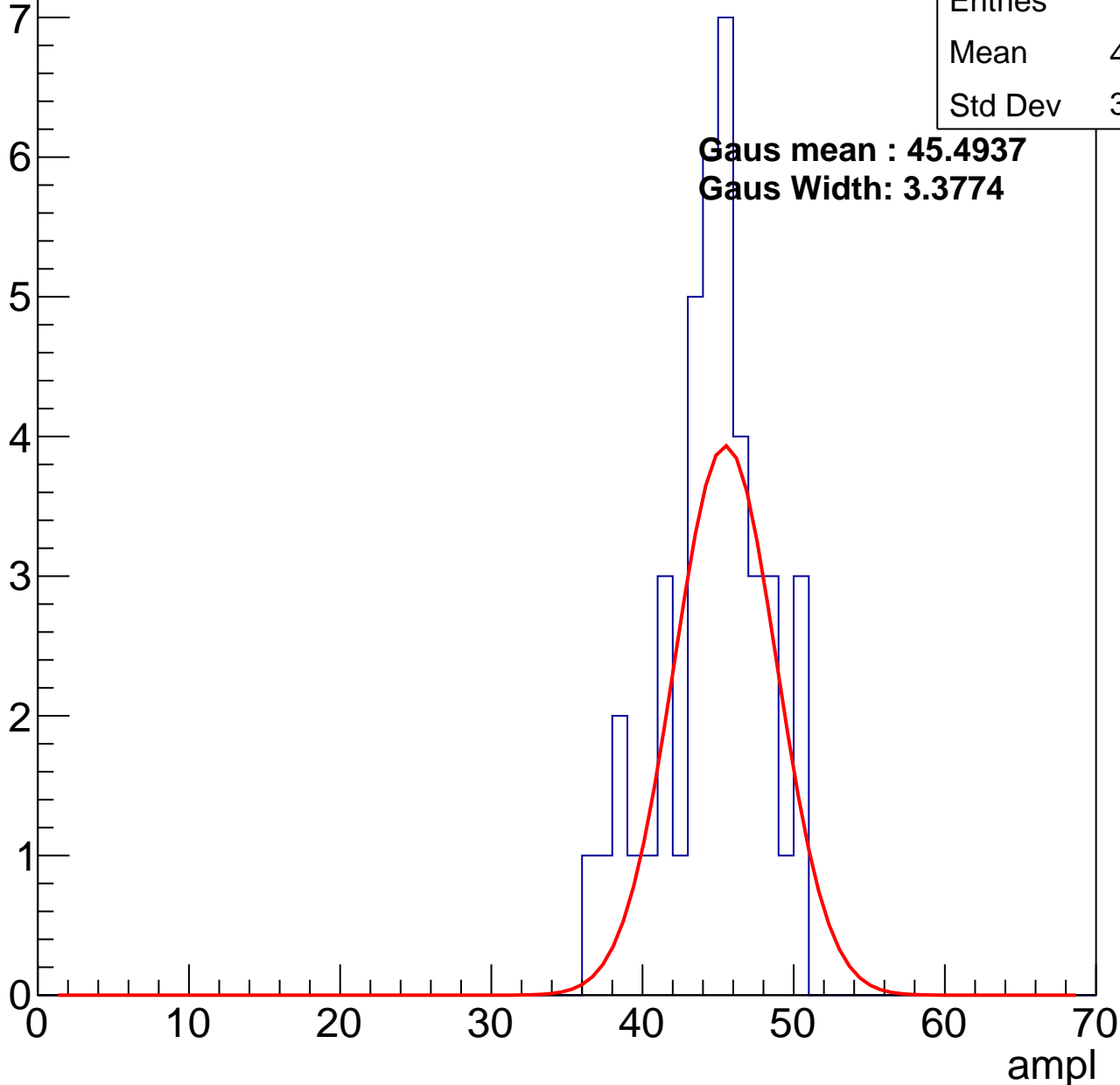
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	42
Mean	44.17
Std Dev	3.422

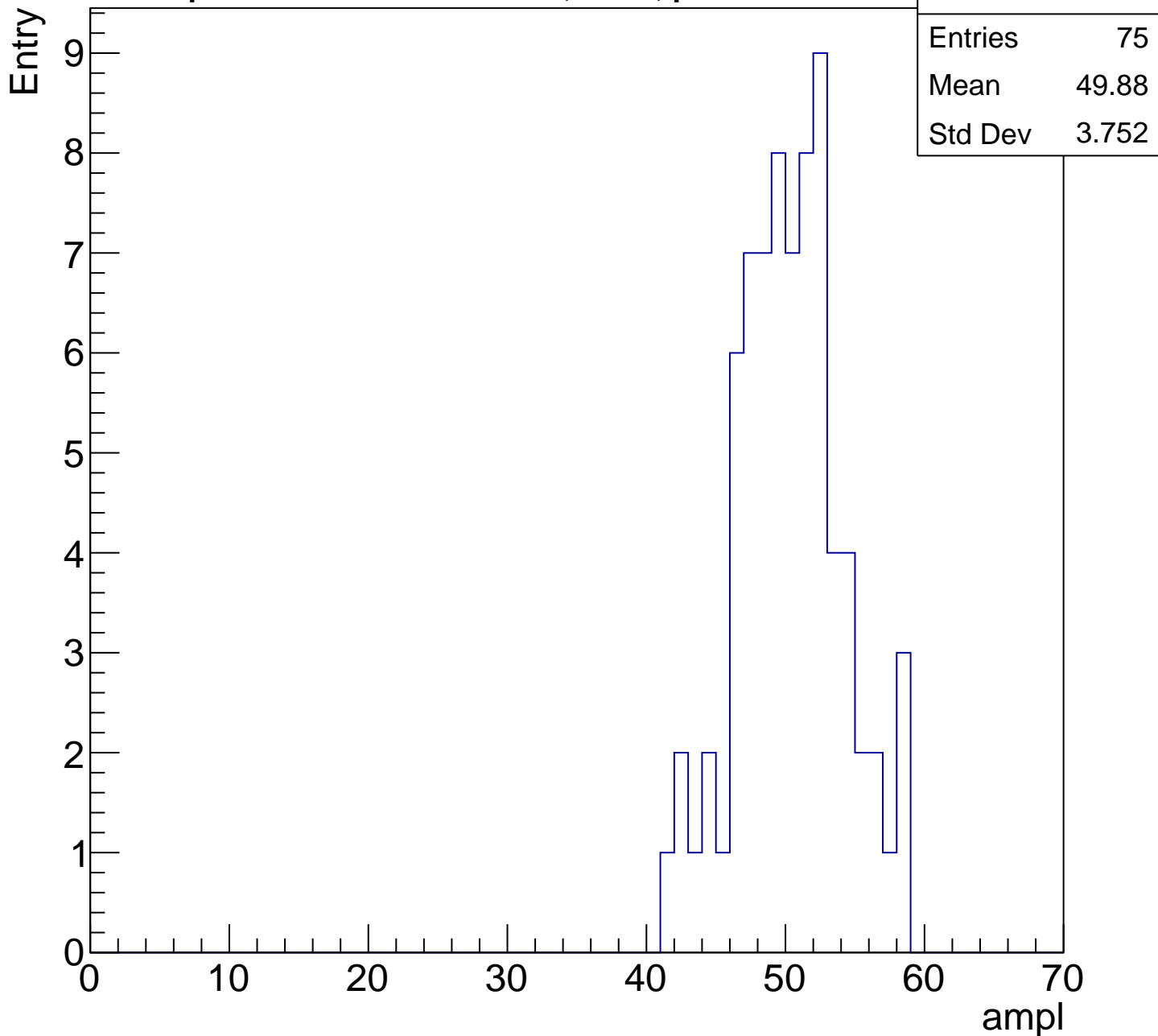
**Gaus mean : 45.4937**

**Gaus Width: 3.3774**



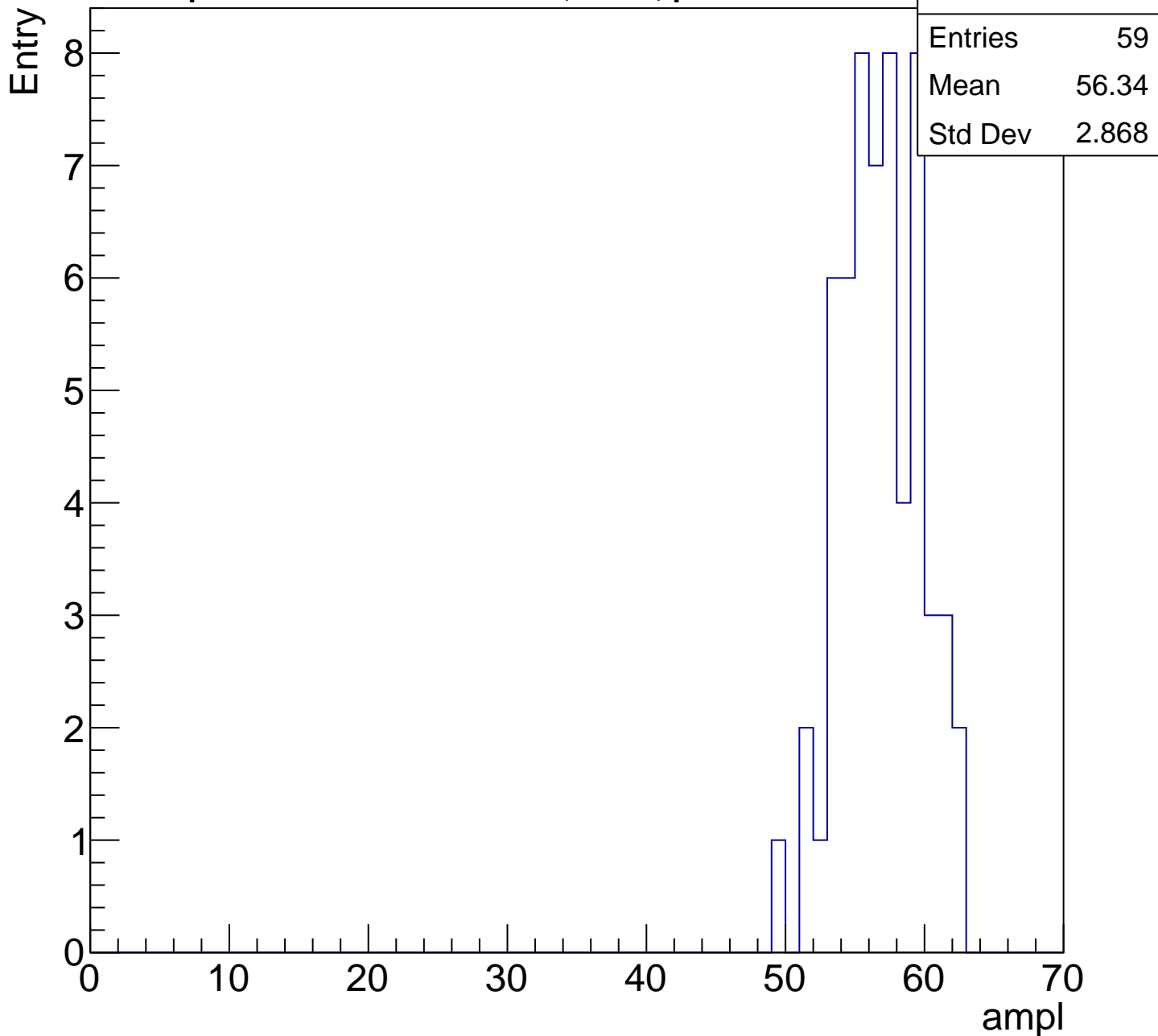
# B0L001S, U6-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U6-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

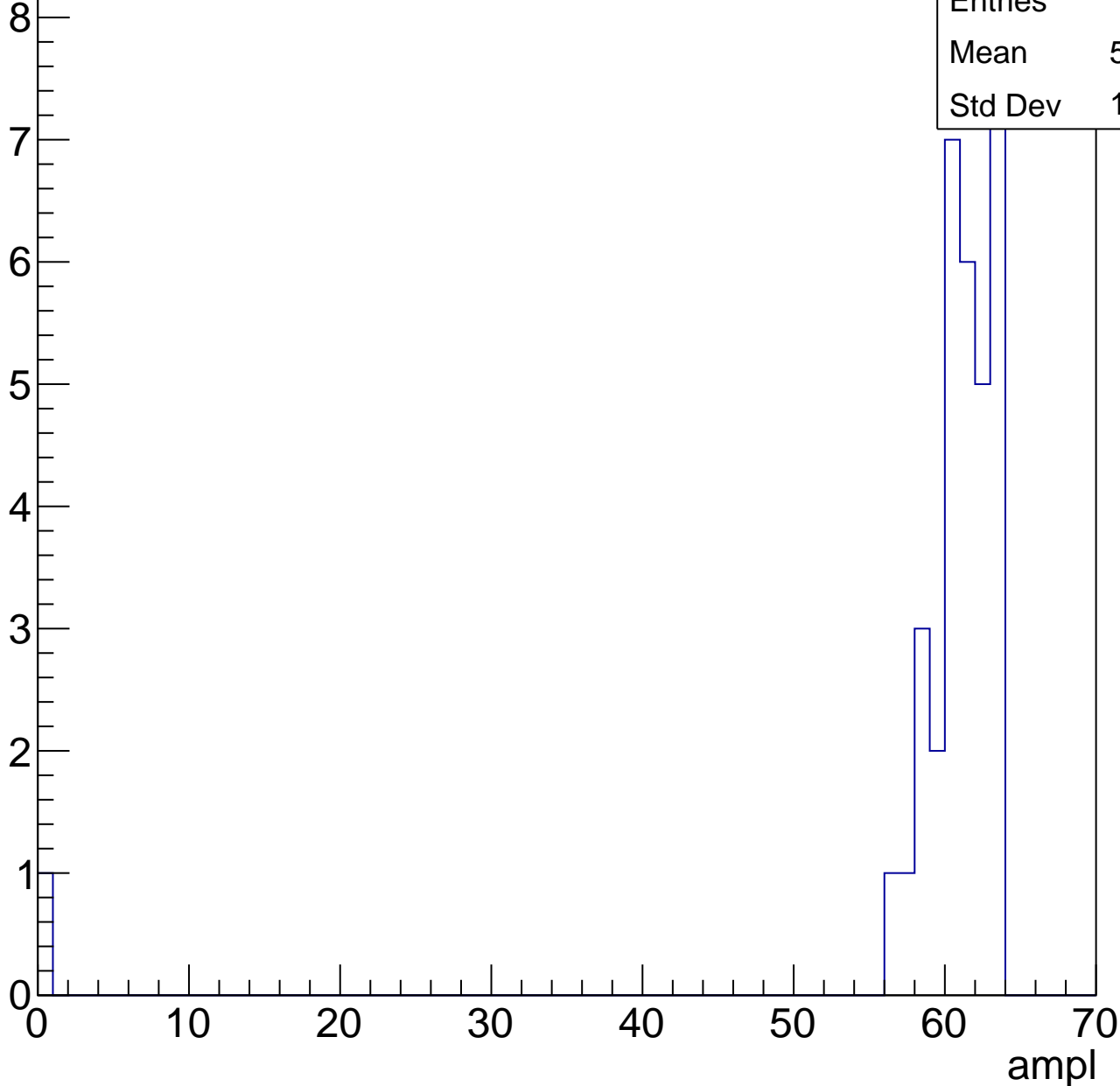


# B0L001S, U6-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	34
Mean	58.97
Std Dev	10.43



# B0L001S, U6-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch74, adc0

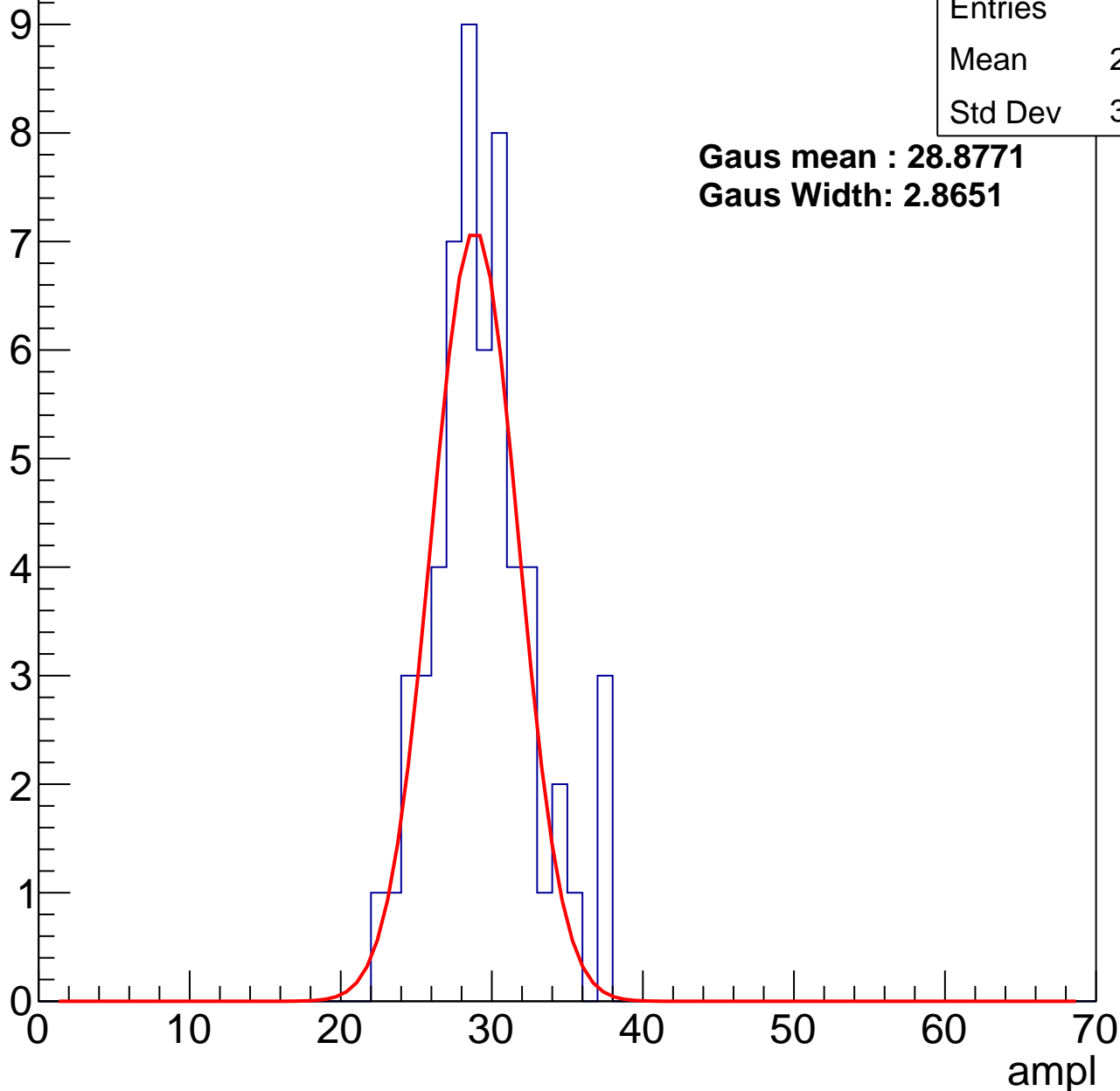
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	28.95
Std Dev	3.337

**Gaus mean : 28.8771**

**Gaus Width: 2.8651**



# B0L001S, U6-ch74, adc1

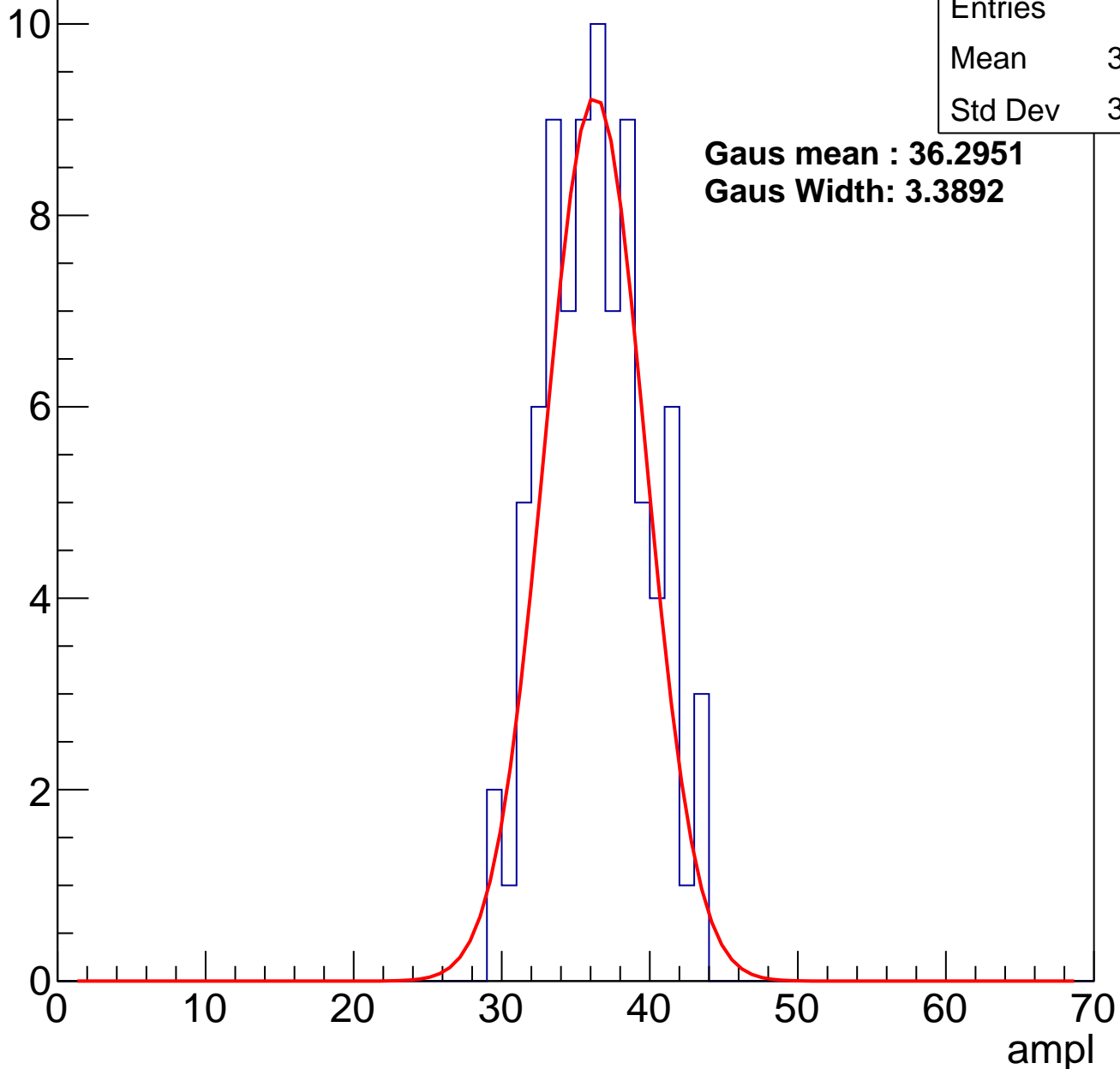
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	84
Mean	35.93
Std Dev	3.376

**Gaus mean : 36.2951**

**Gaus Width: 3.3892**

Entry



# B0L001S, U6-ch74, adc2

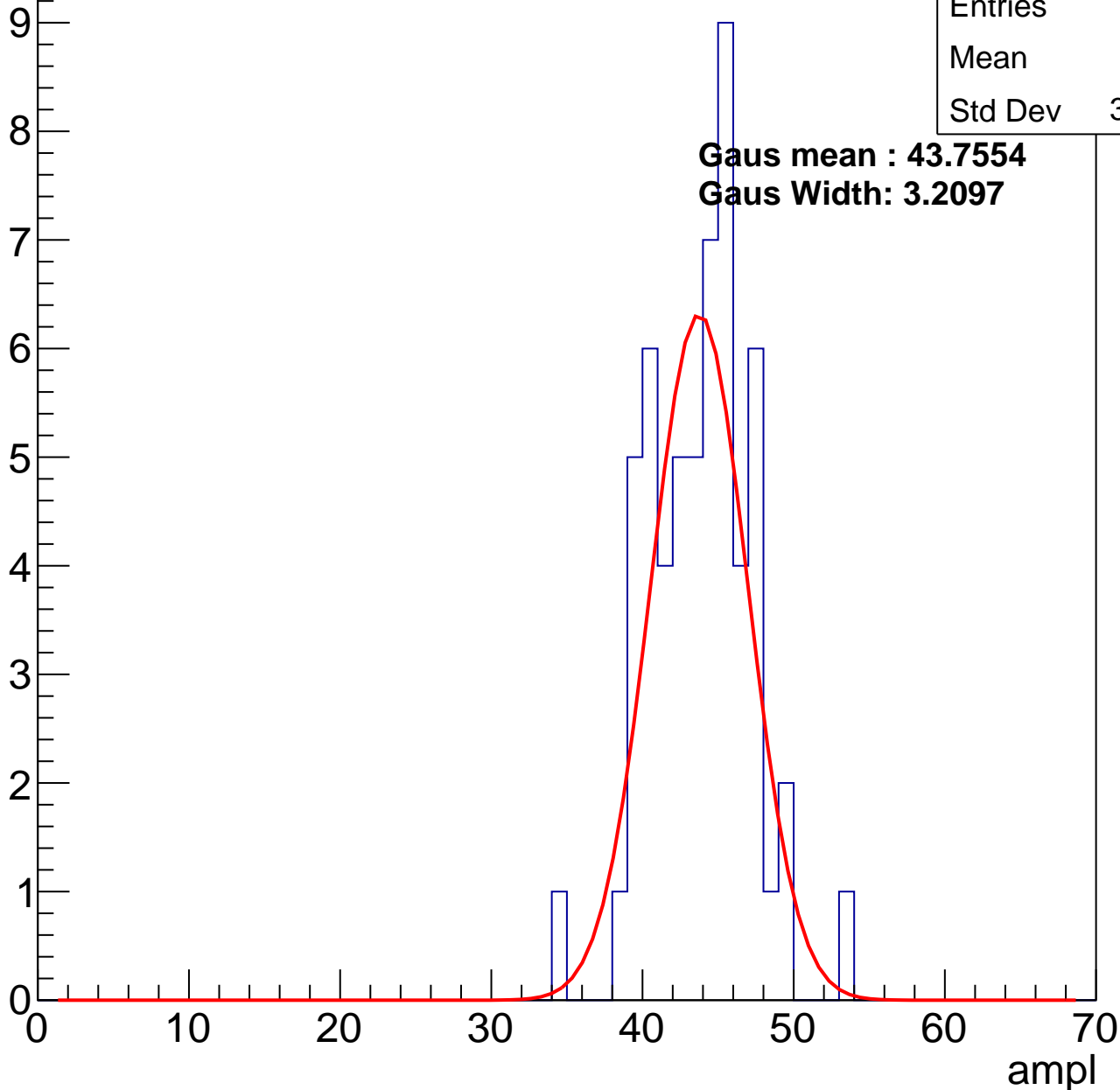
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	43.4
Std Dev	3.308

**Gaus mean : 43.7554**

**Gaus Width: 3.2097**

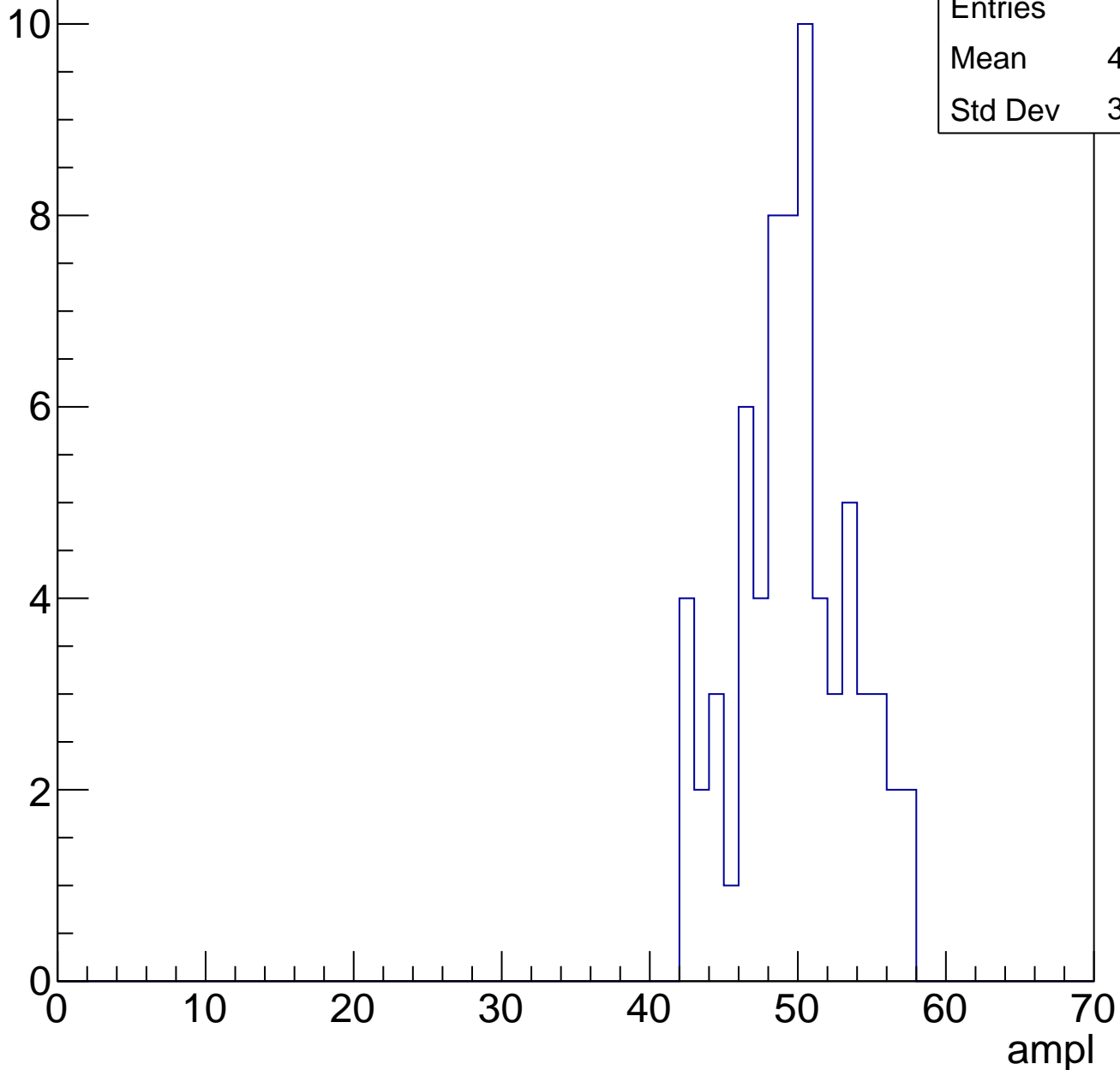


# B0L001S, U6-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	68
Mean	49.25
Std Dev	3.786

Entry

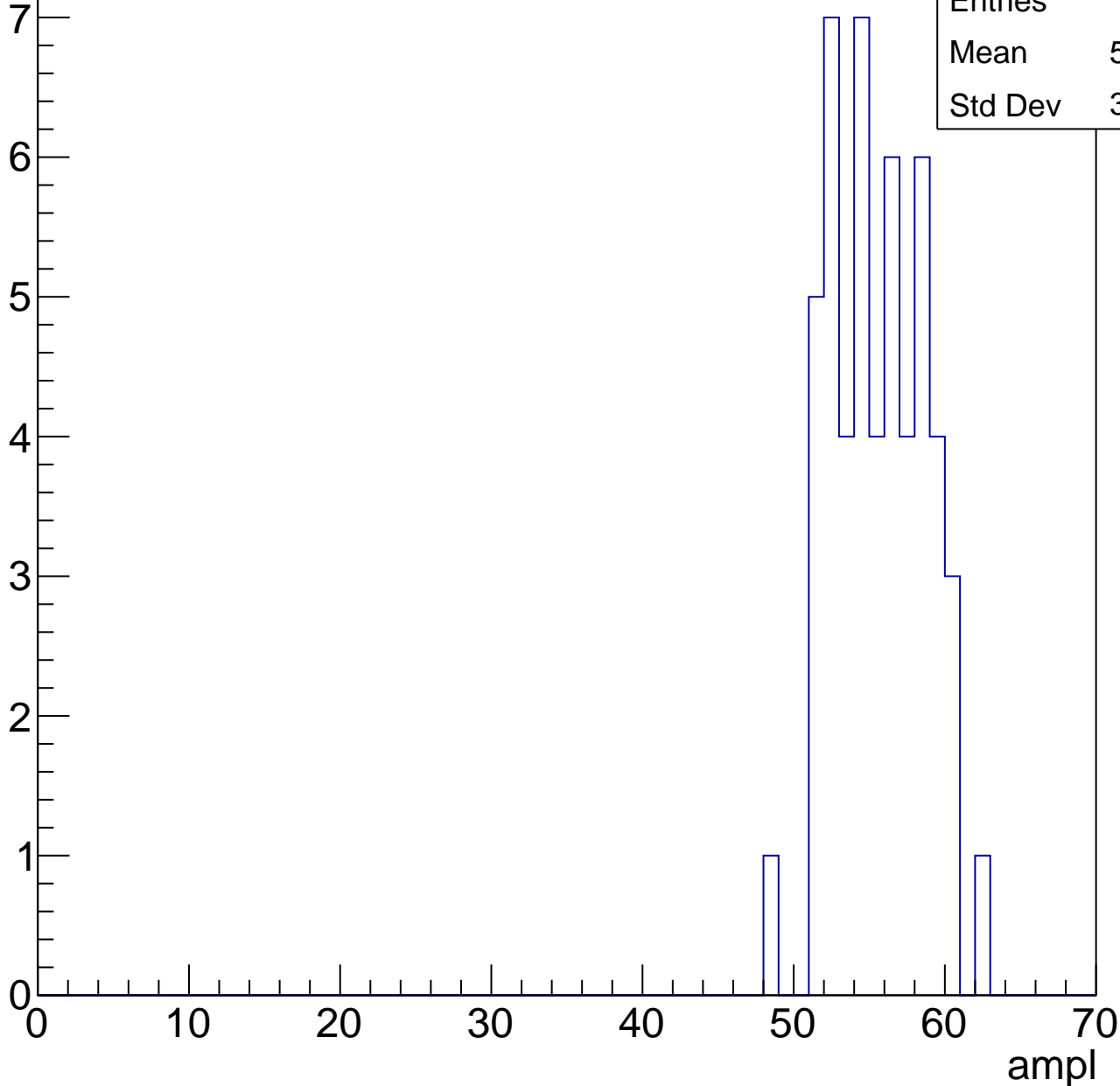


# B0L001S, U6-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	55.13
Std Dev	3.032

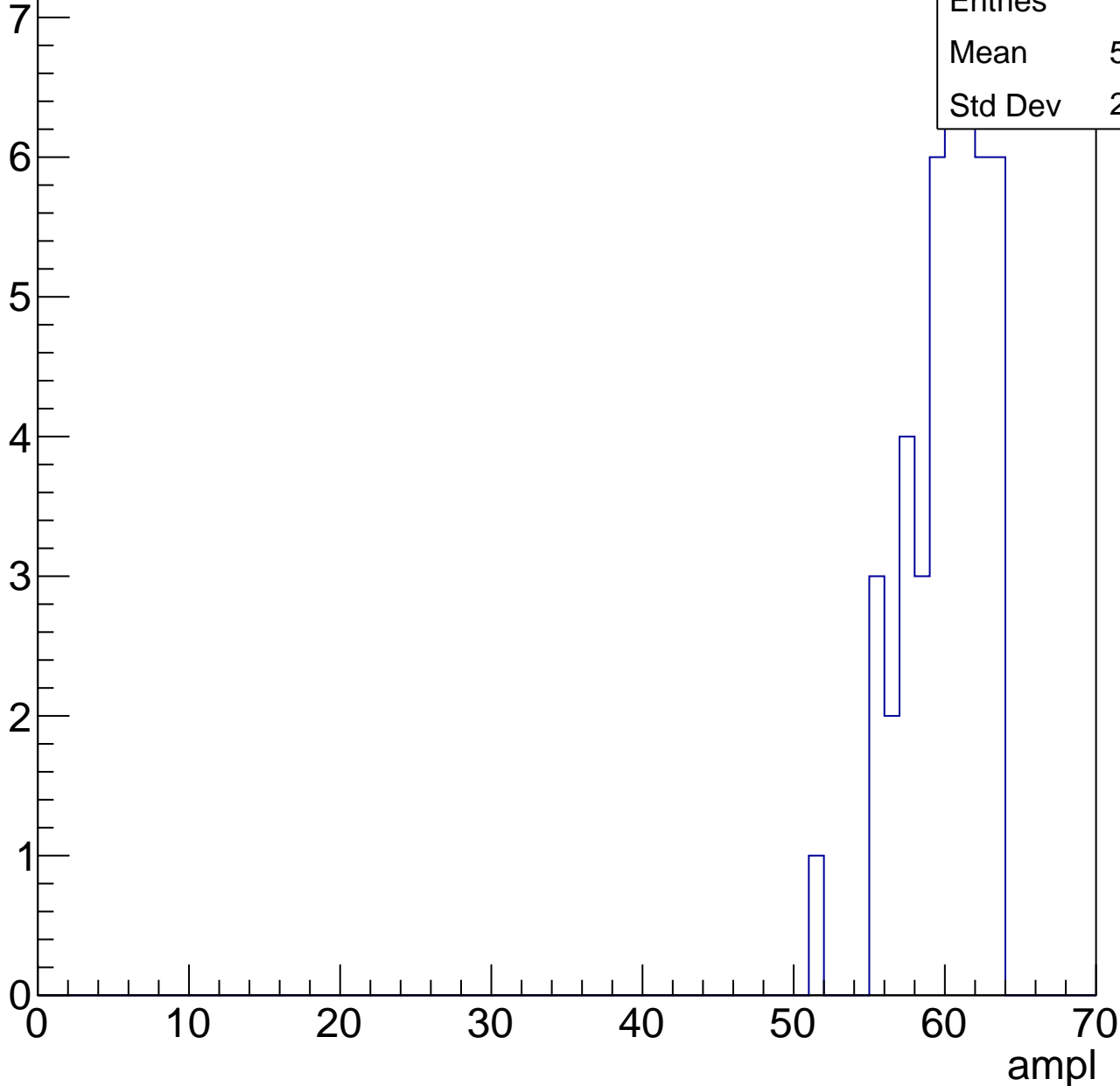


# B0L001S, U6-ch74, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

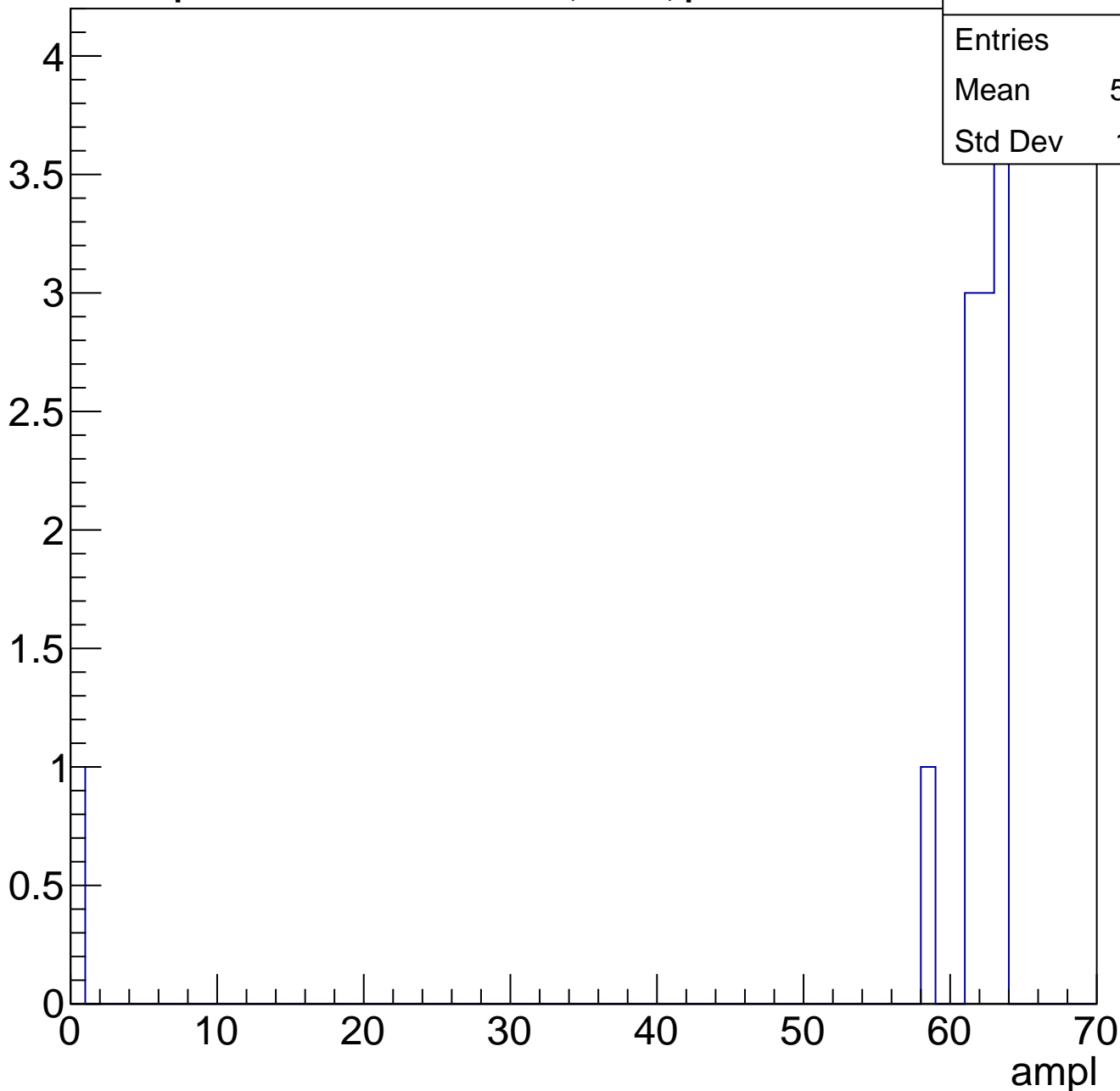
Entries	45
Mean	59.58
Std Dev	2.662



# B0L001S, U6-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch75, adc0

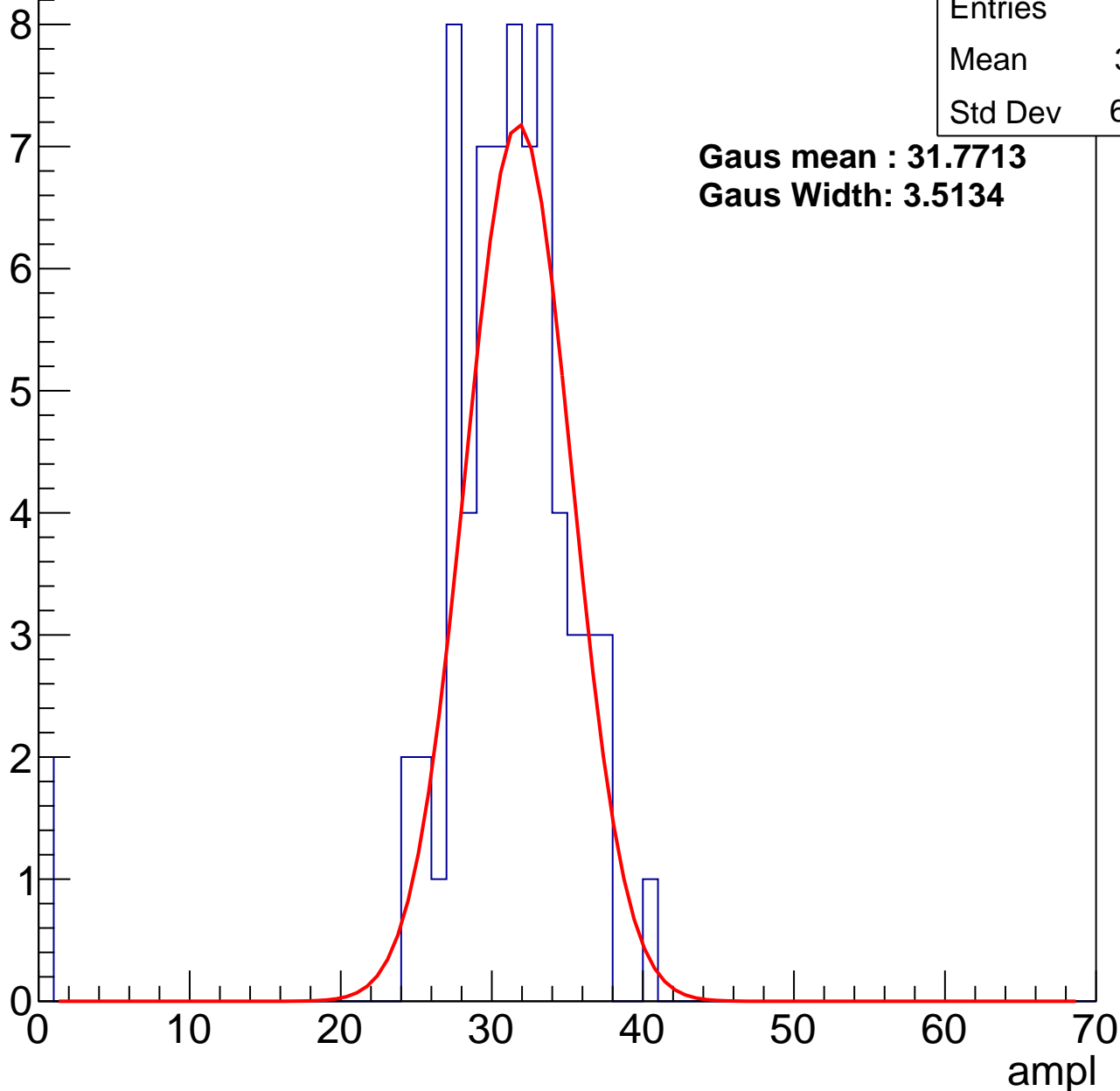
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	30.01
Std Dev	6.135

**Gaus mean : 31.7713**

**Gaus Width: 3.5134**



# B0L001S, U6-ch75, adc1

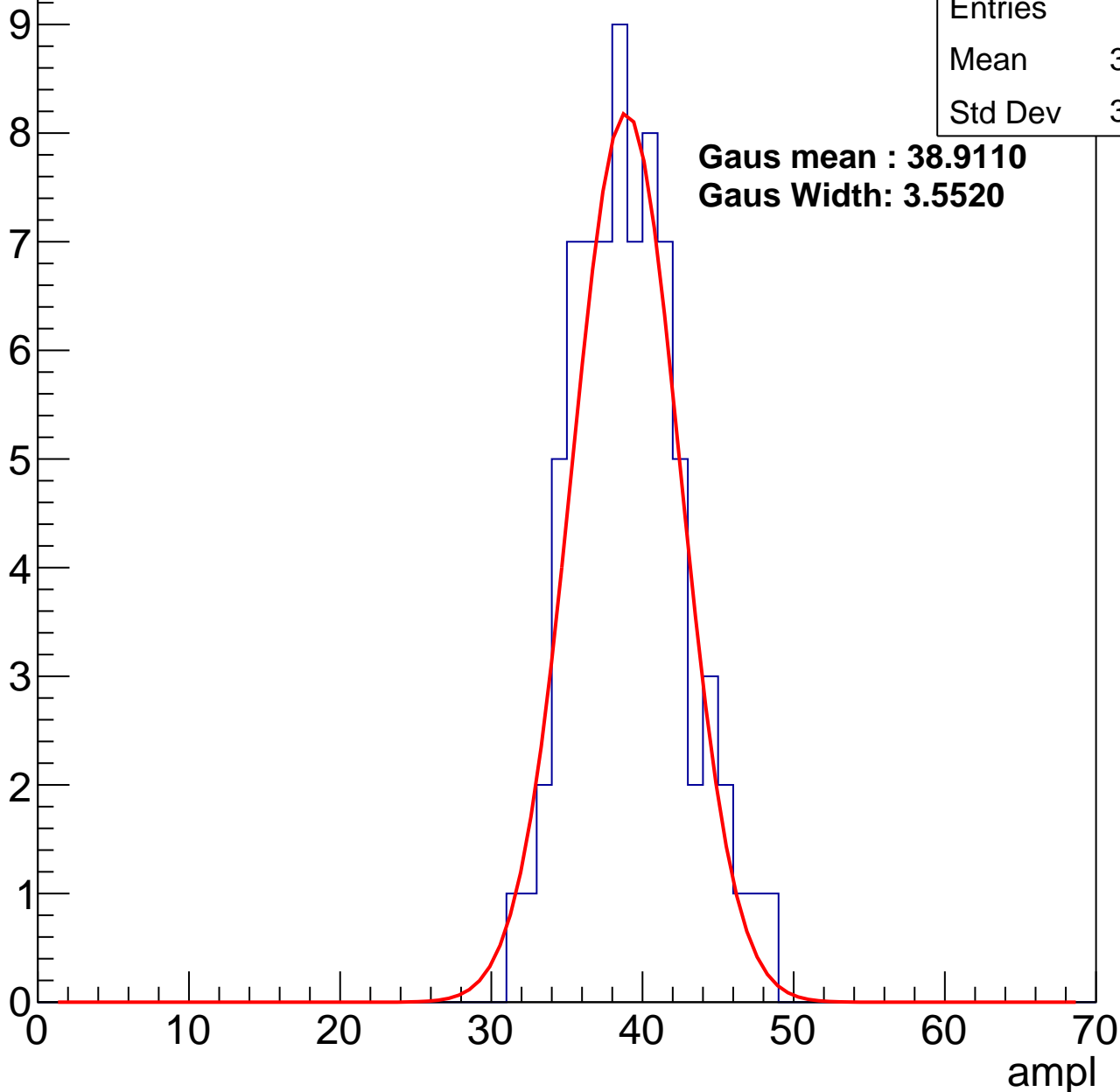
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	38.63
Std Dev	3.565

**Gaus mean : 38.9110**

**Gaus Width: 3.5520**



# B0L001S, U6-ch75, adc2

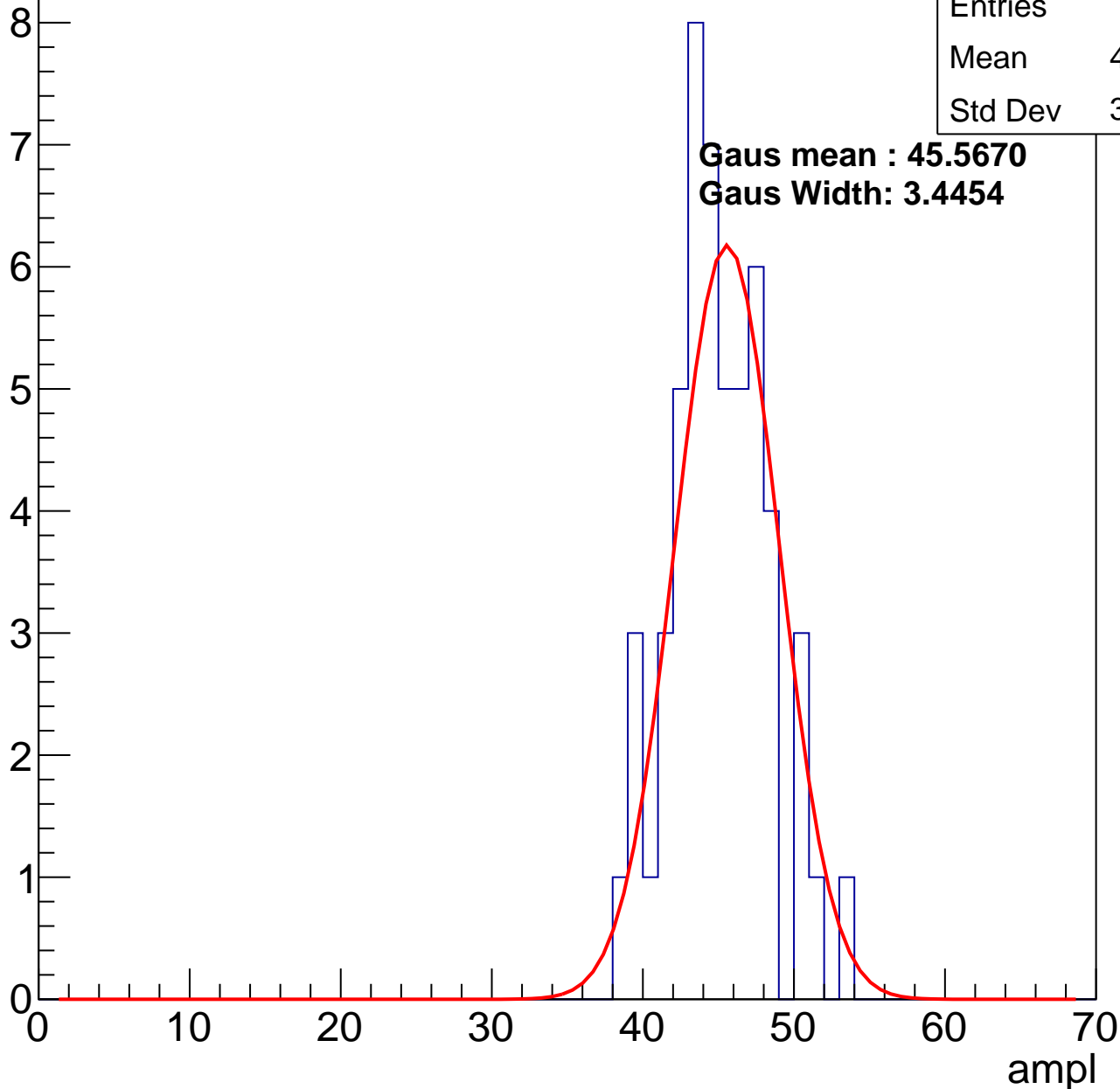
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	44.58
Std Dev	3.206

**Gaus mean : 45.5670**

**Gaus Width: 3.4454**

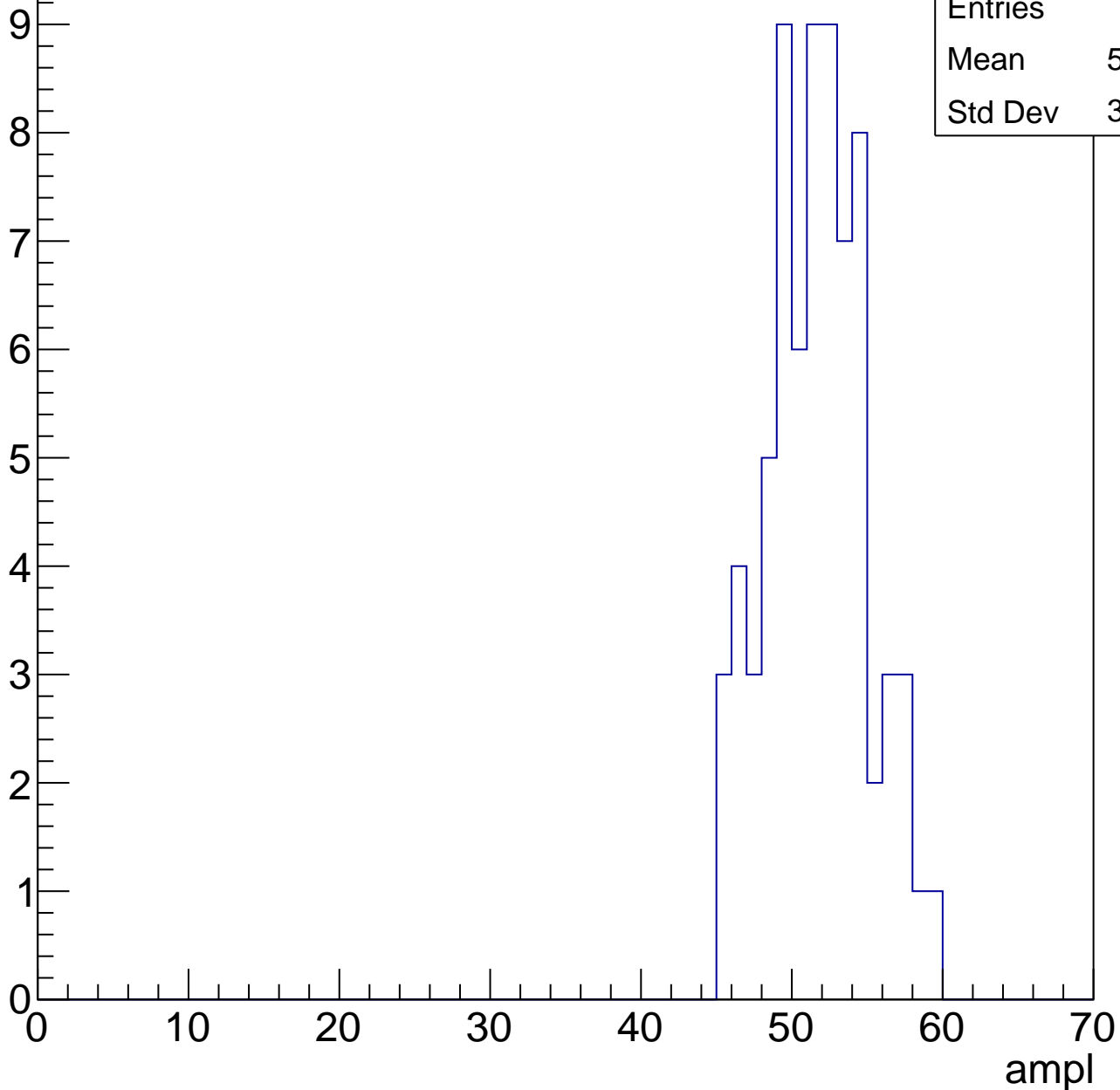


# B0L001S, U6-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	51.19
Std Dev	3.263

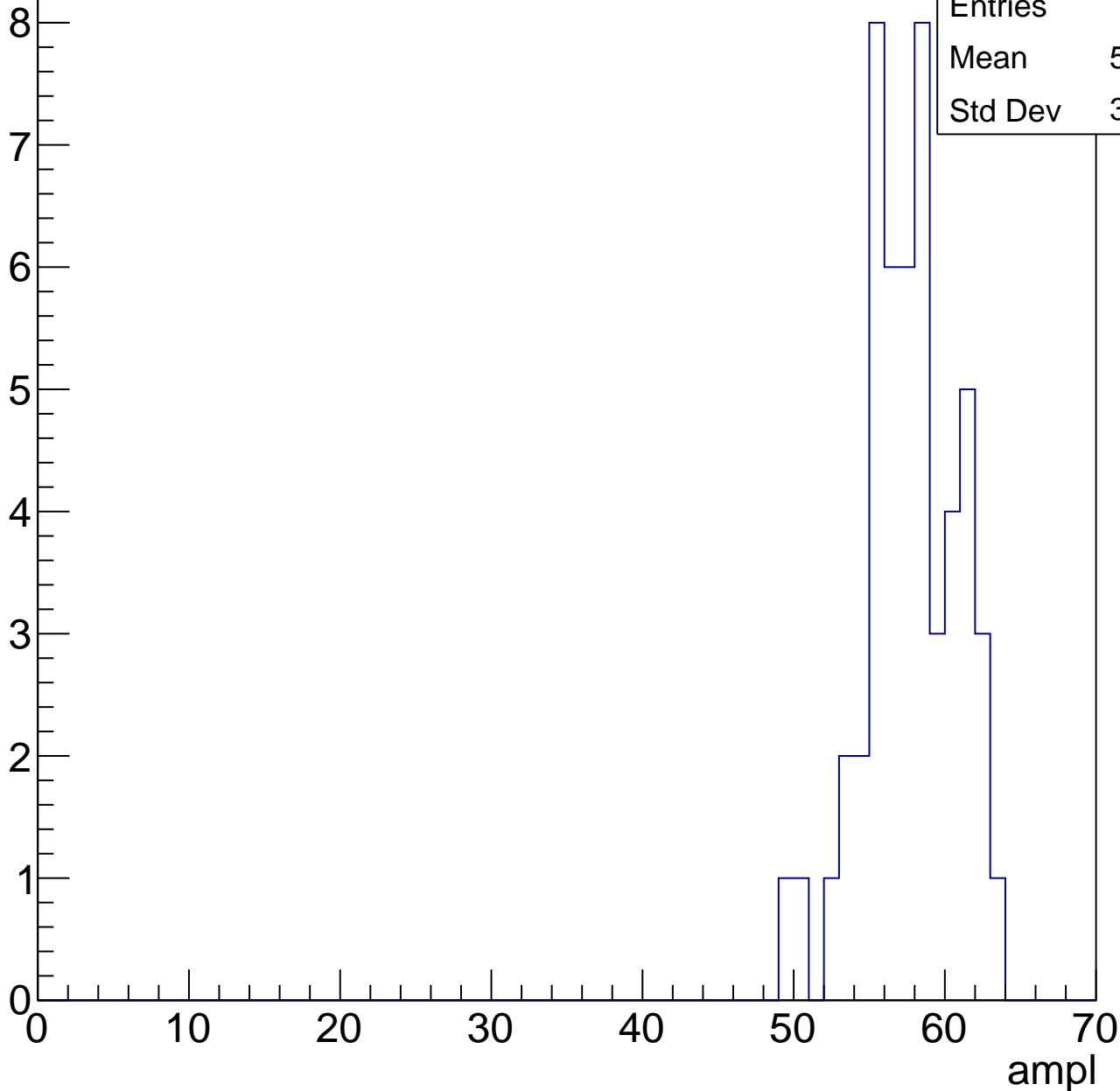


# B0L001S, U6-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	57.22
Std Dev	3.038

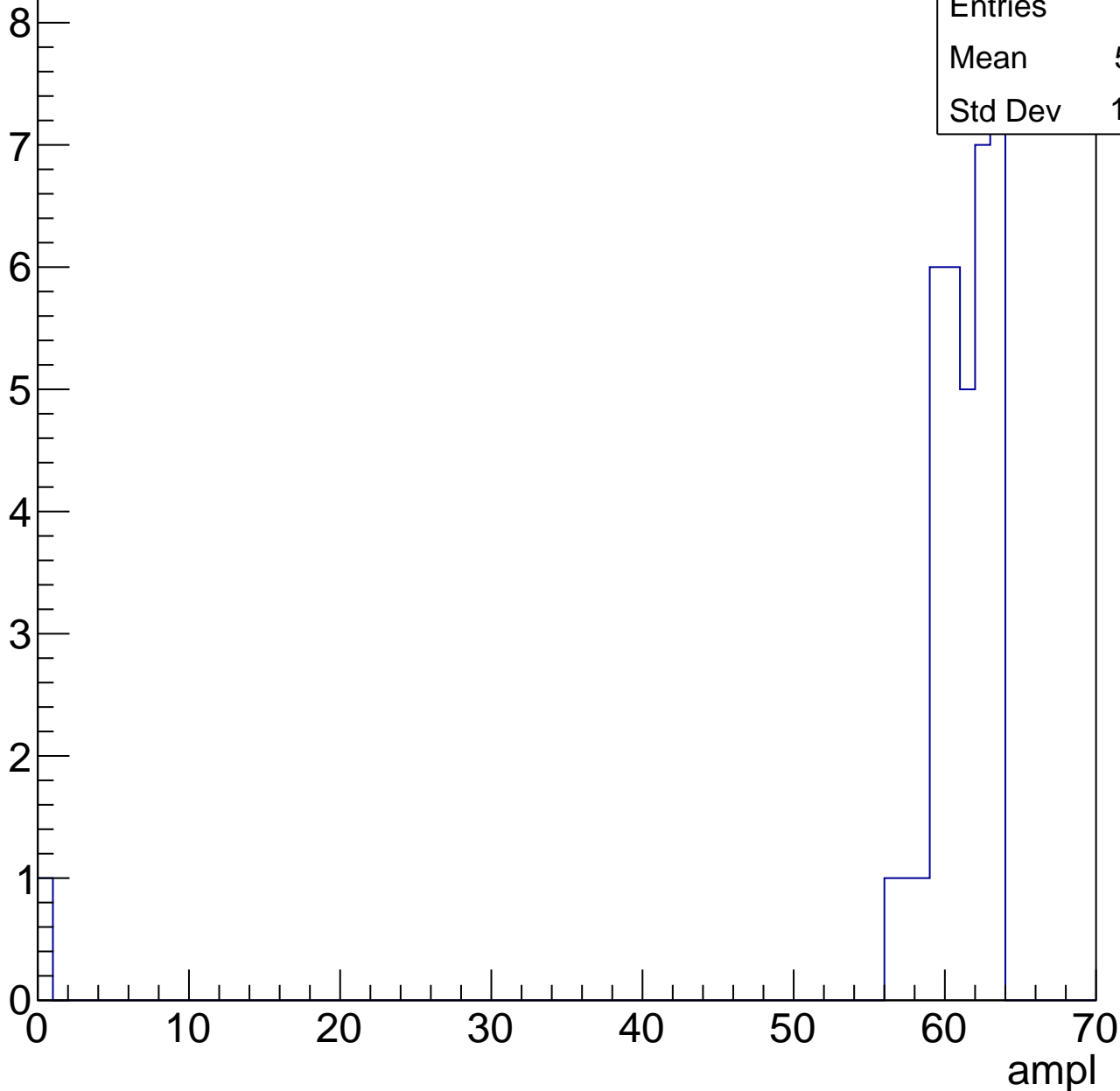


# B0L001S, U6-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	36
Mean	59.11
Std Dev	10.15



# B0L001S, U6-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U6-ch76, adc0

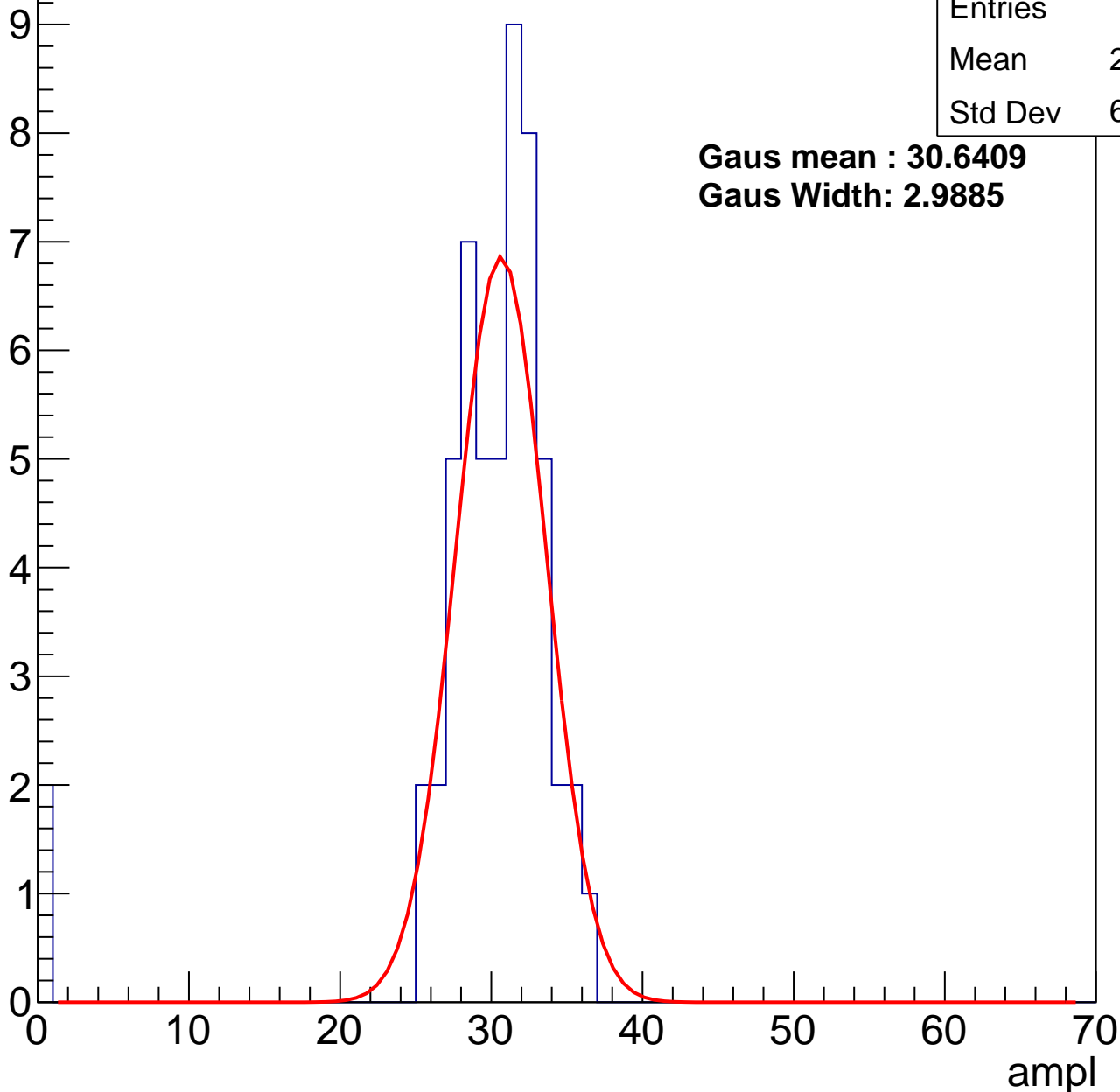
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	29.13
Std Dev	6.212

**Gaus mean : 30.6409**

**Gaus Width: 2.9885**



# B0L001S, U6-ch76, adc1

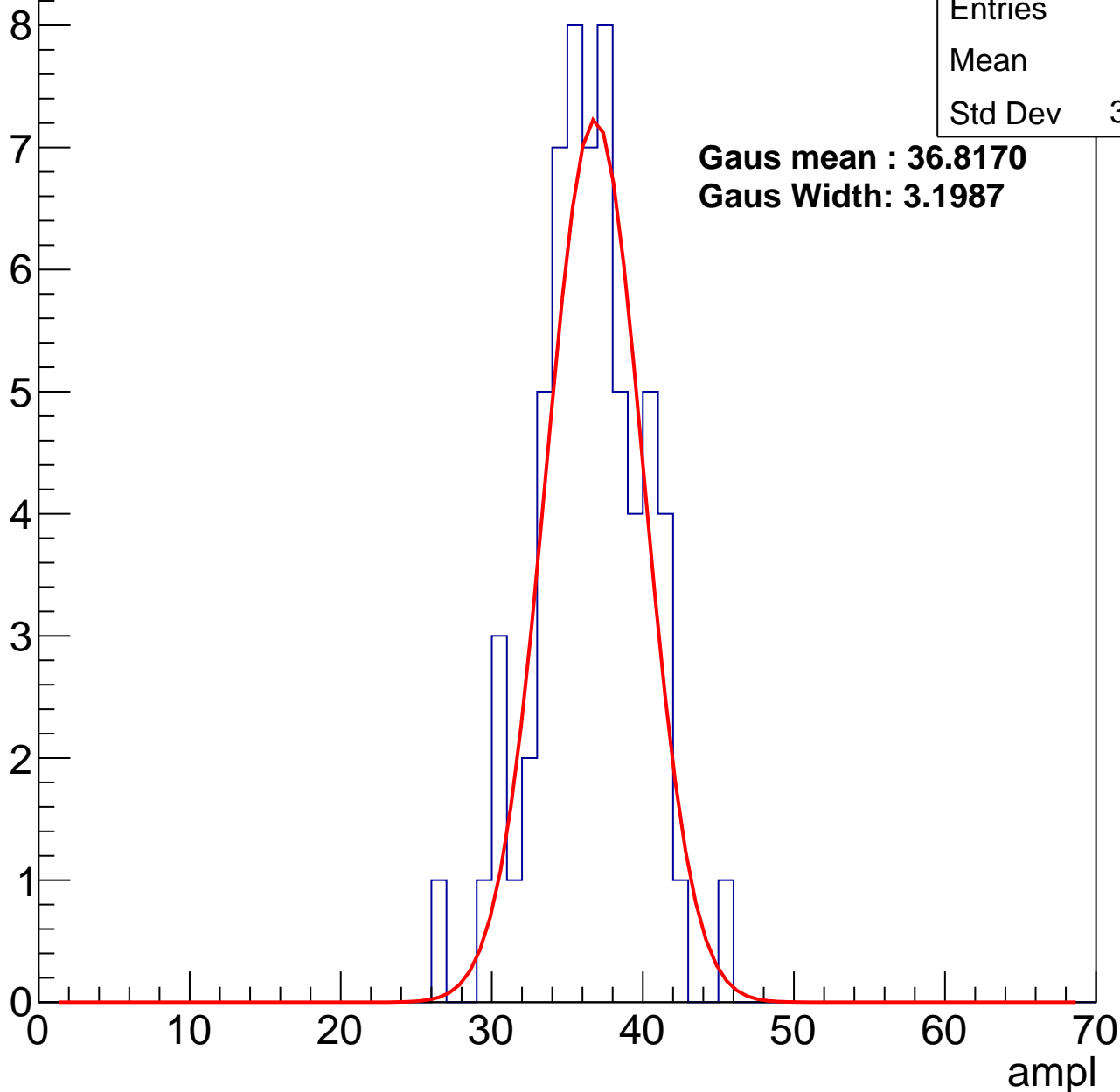
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	36
Std Dev	3.464

**Gaus mean : 36.8170**

**Gaus Width: 3.1987**



# B0L001S, U6-ch76, adc2

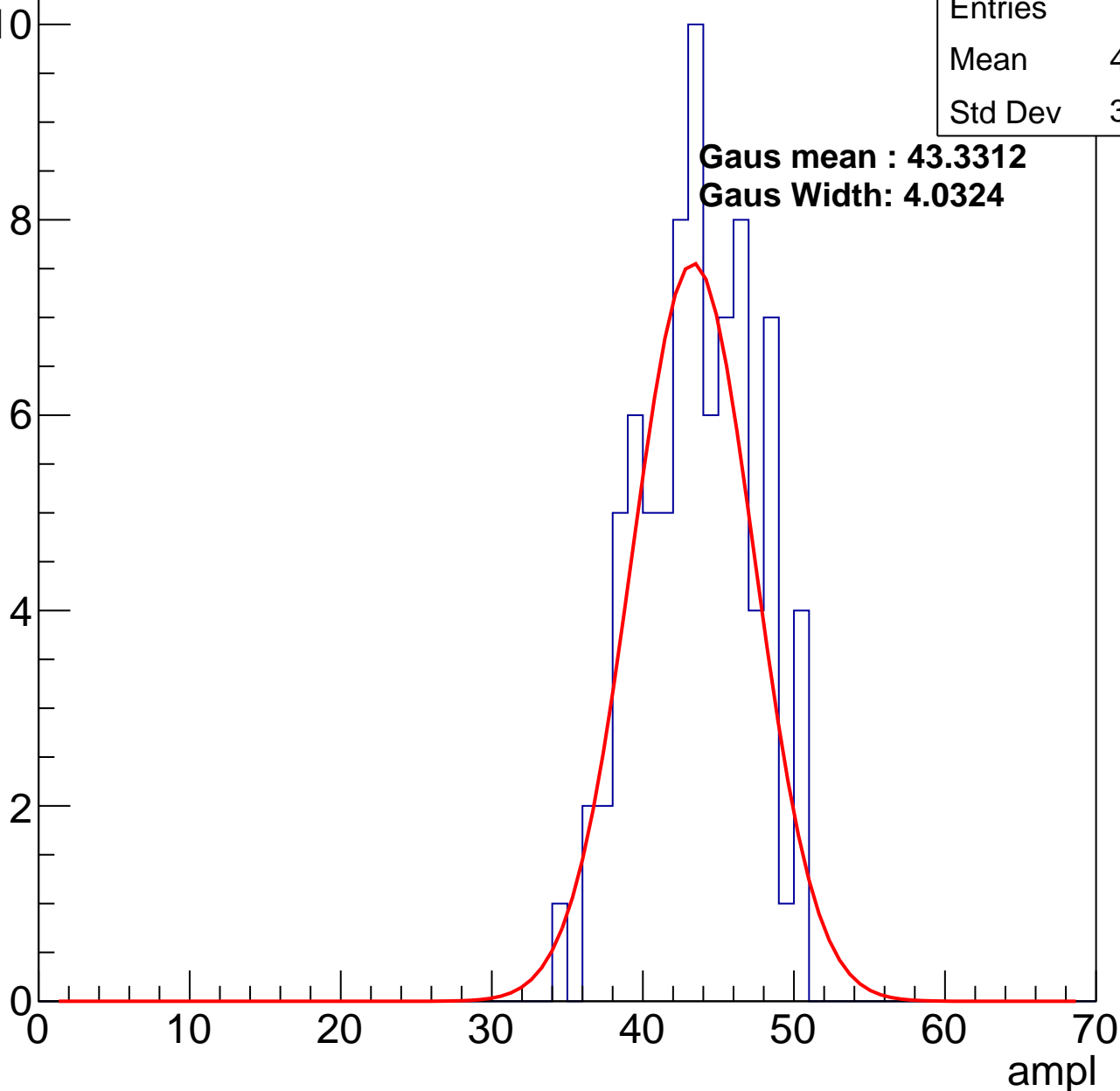
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	43.15
Std Dev	3.719

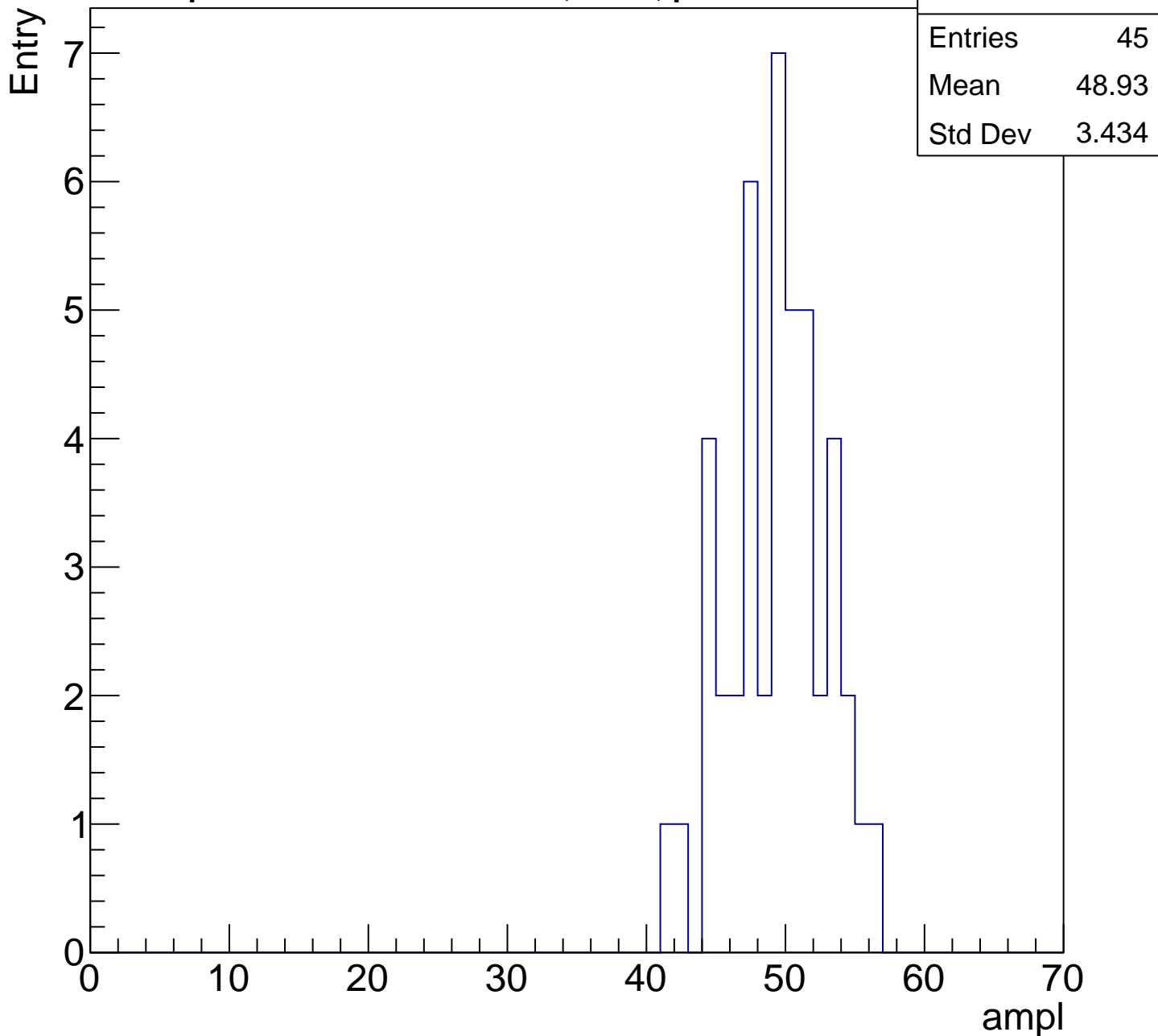
**Gaus mean : 43.3312**

**Gaus Width: 4.0324**



# B0L001S, U6-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

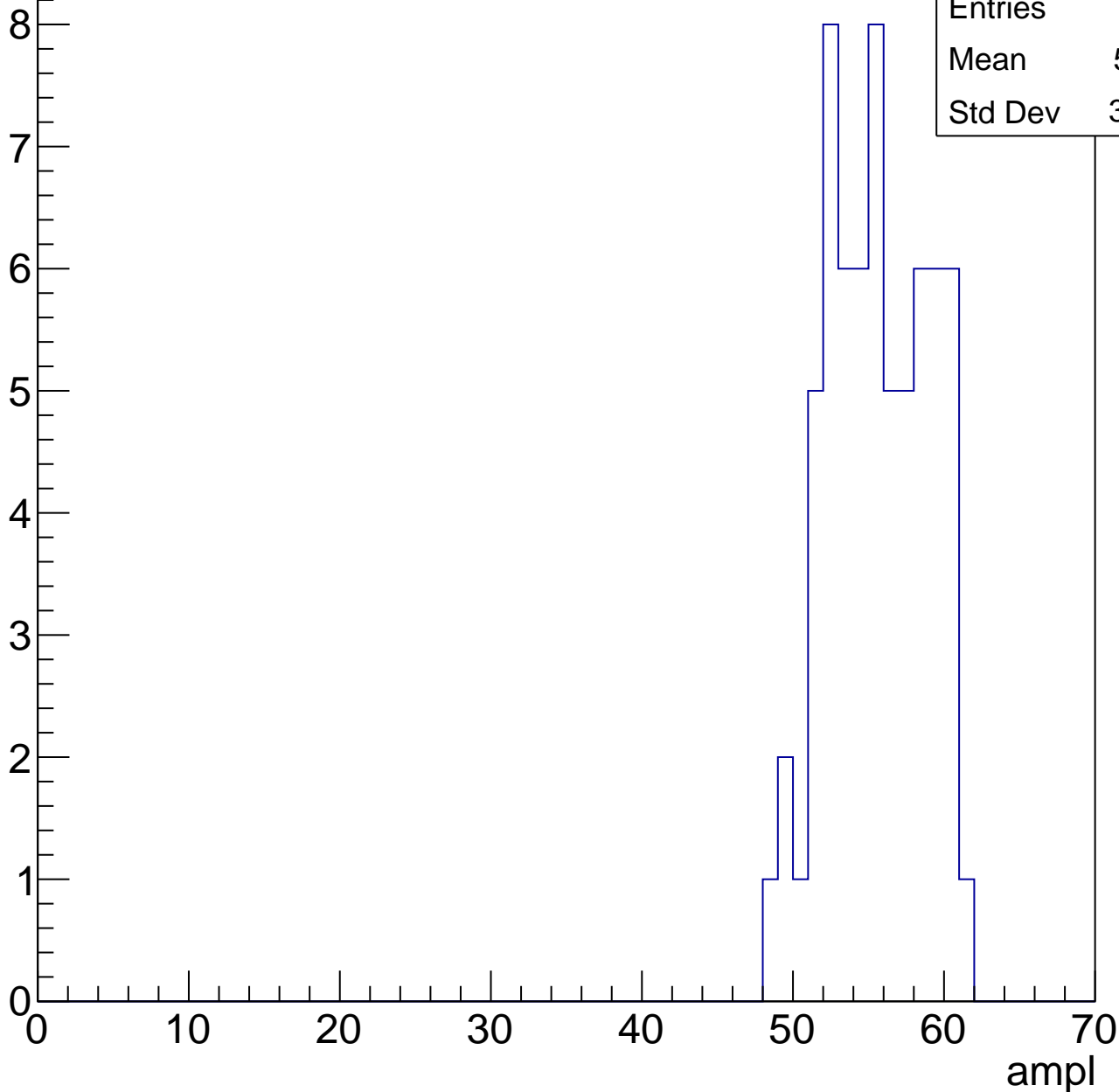


# B0L001S, U6-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	55.11
Std Dev	3.229

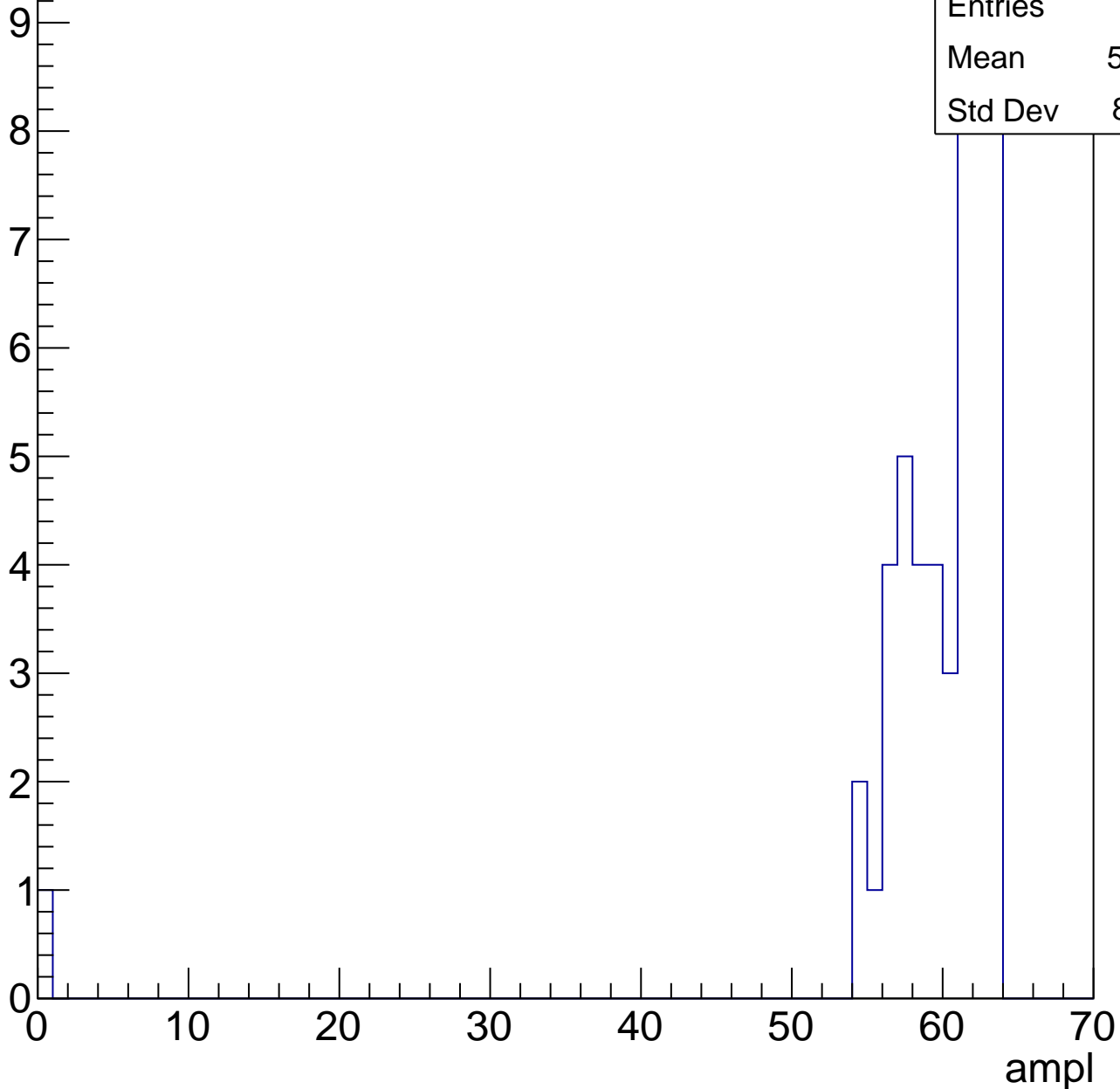


# B0L001S, U6-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

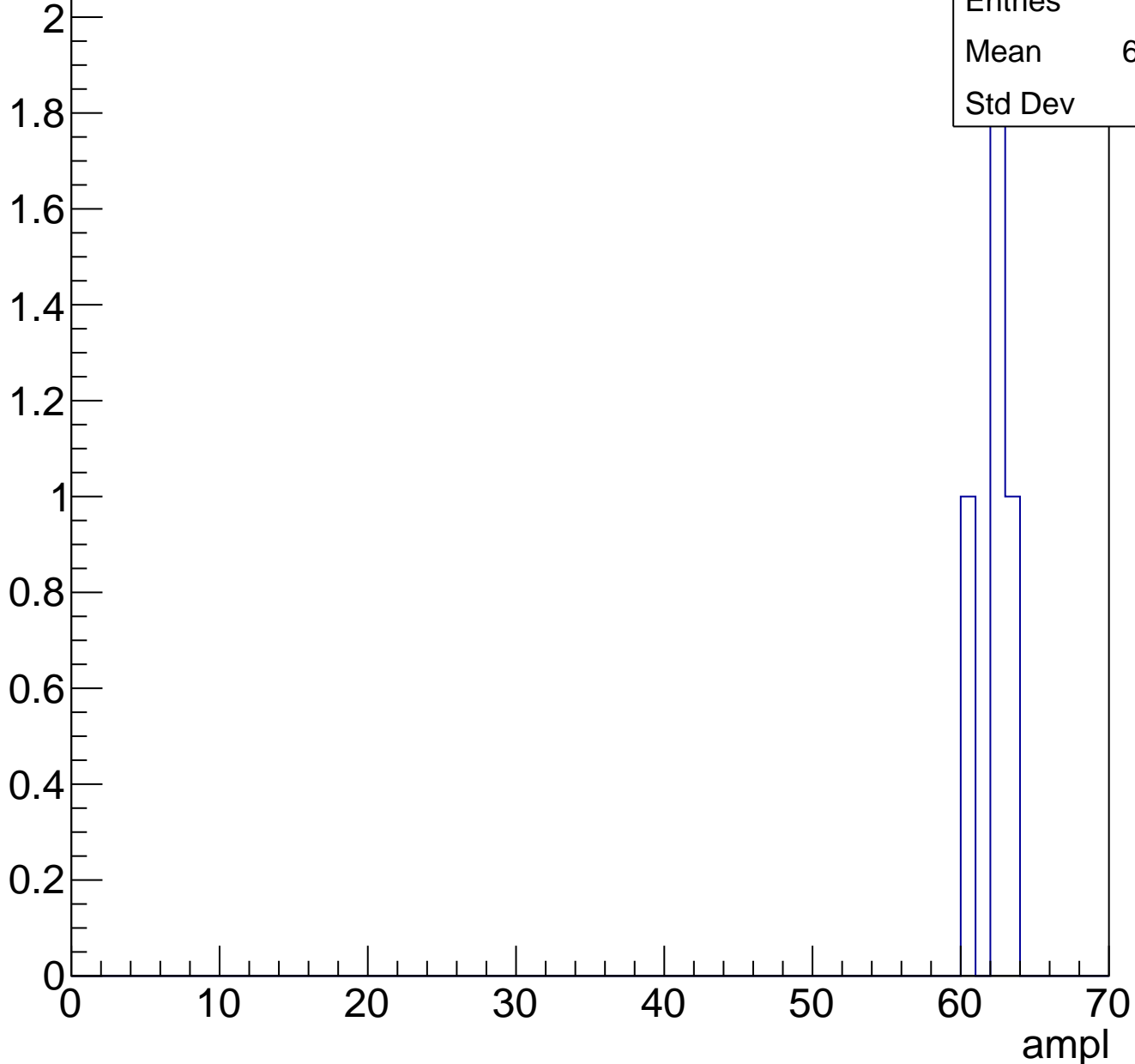
Entries	50
Mean	58.64
Std Dev	8.781



# B0L001S, U6-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch77, adc0

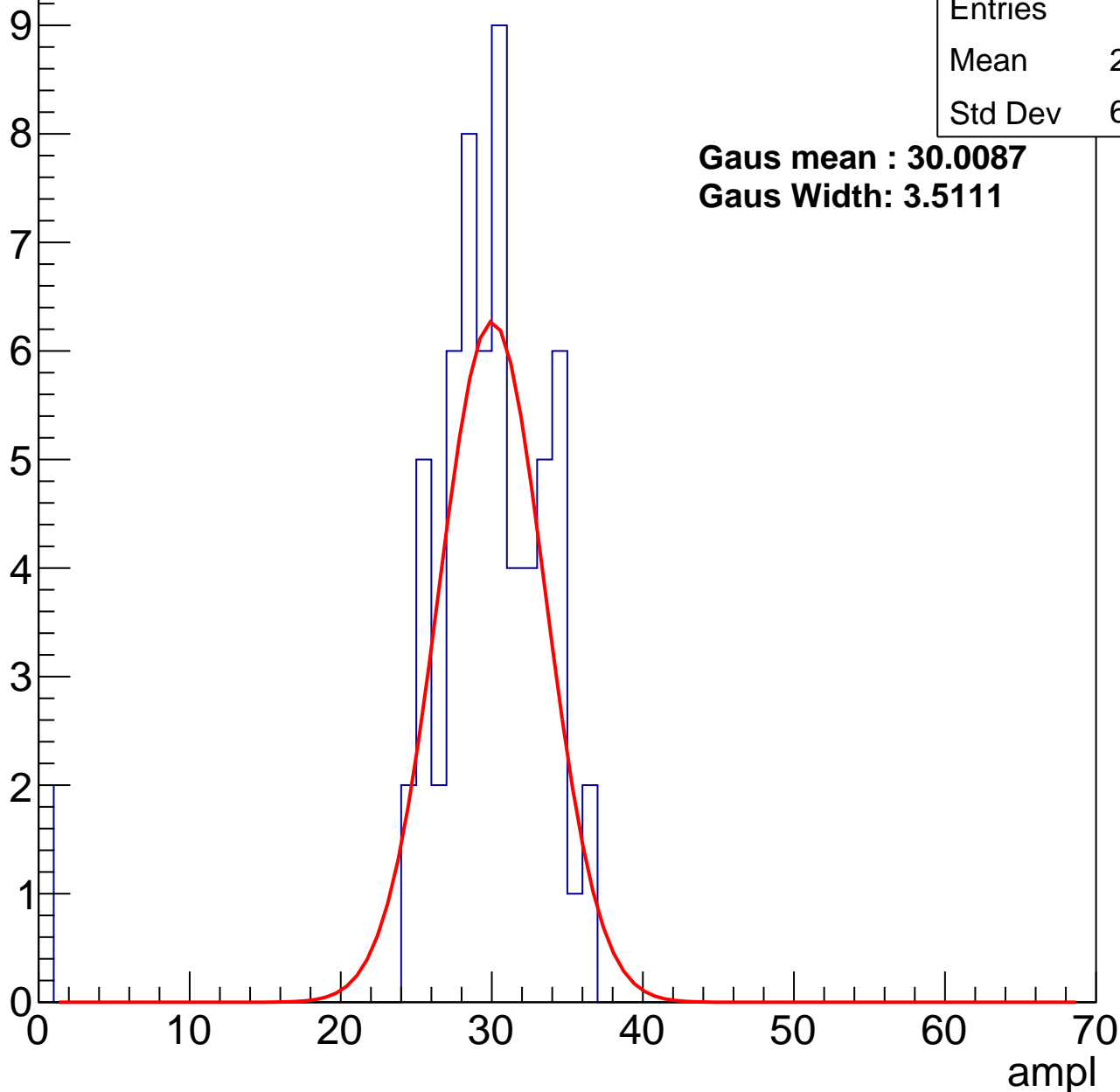
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	28.76
Std Dev	6.069

**Gaus mean : 30.0087**

**Gaus Width: 3.5111**



# B0L001S, U6-ch77, adc1

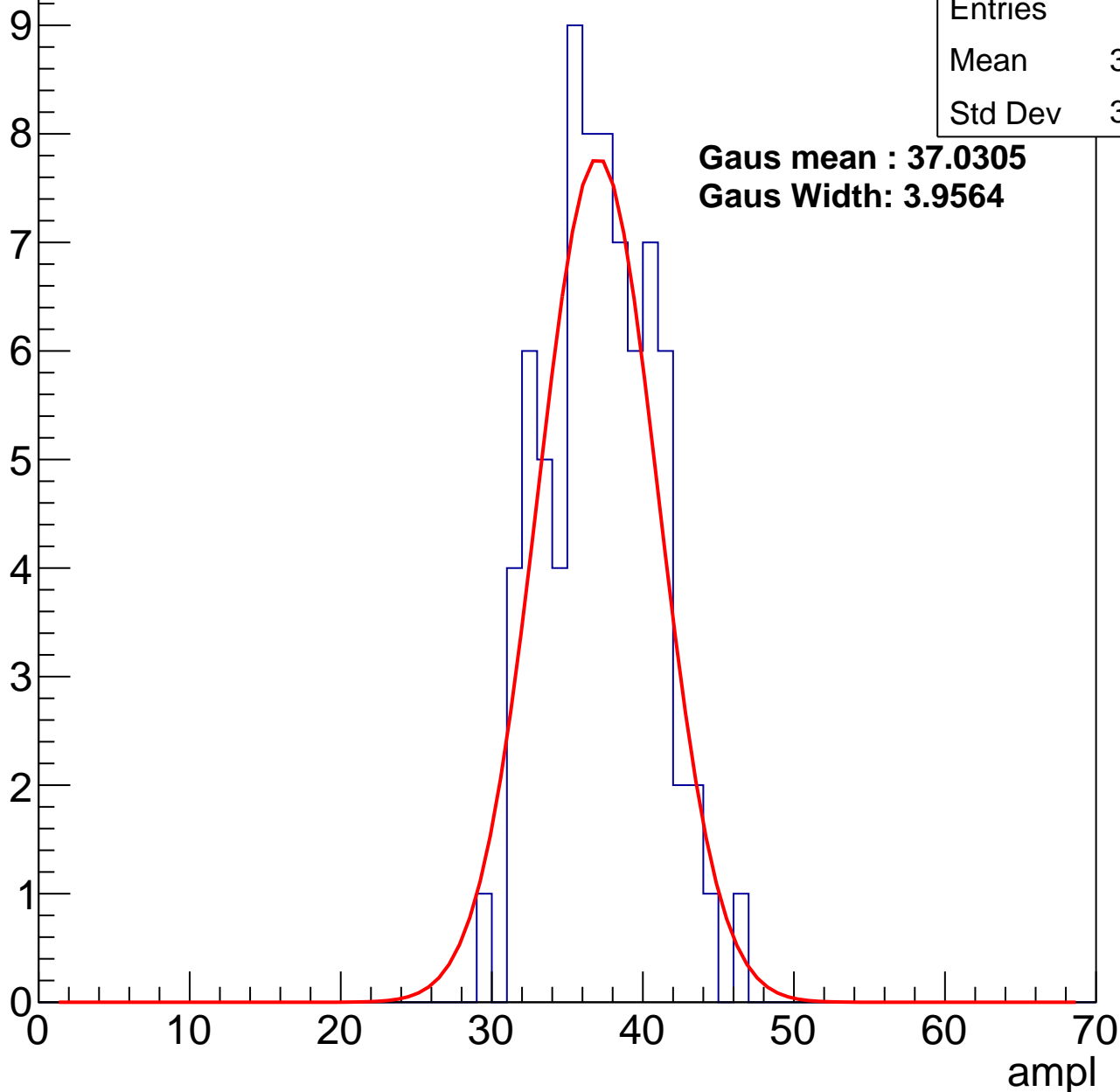
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	36.77
Std Dev	3.523

**Gaus mean : 37.0305**

**Gaus Width: 3.9564**



# B0L001S, U6-ch77, adc2

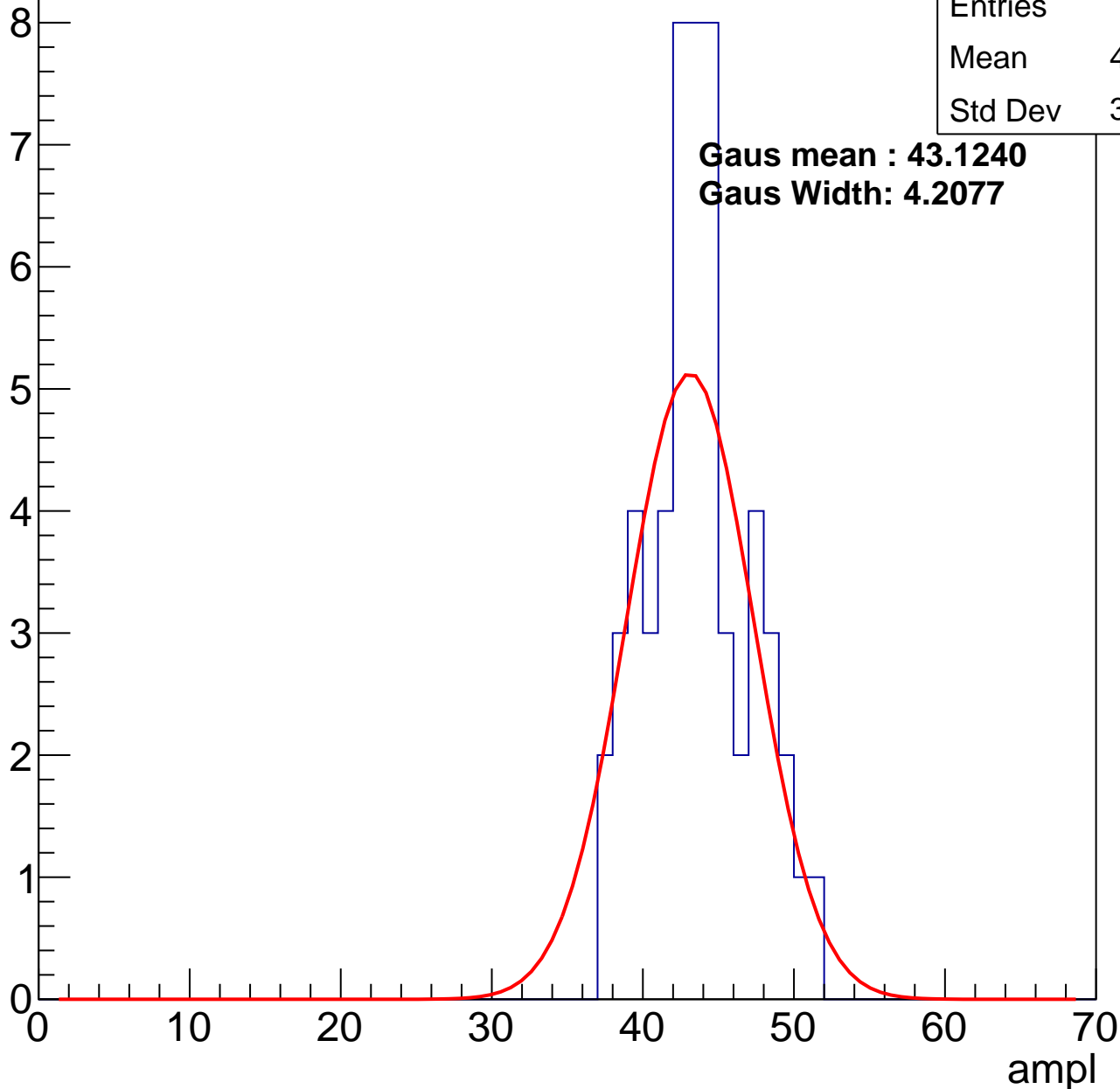
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	43.18
Std Dev	3.333

**Gaus mean : 43.1240**

**Gaus Width: 4.2077**

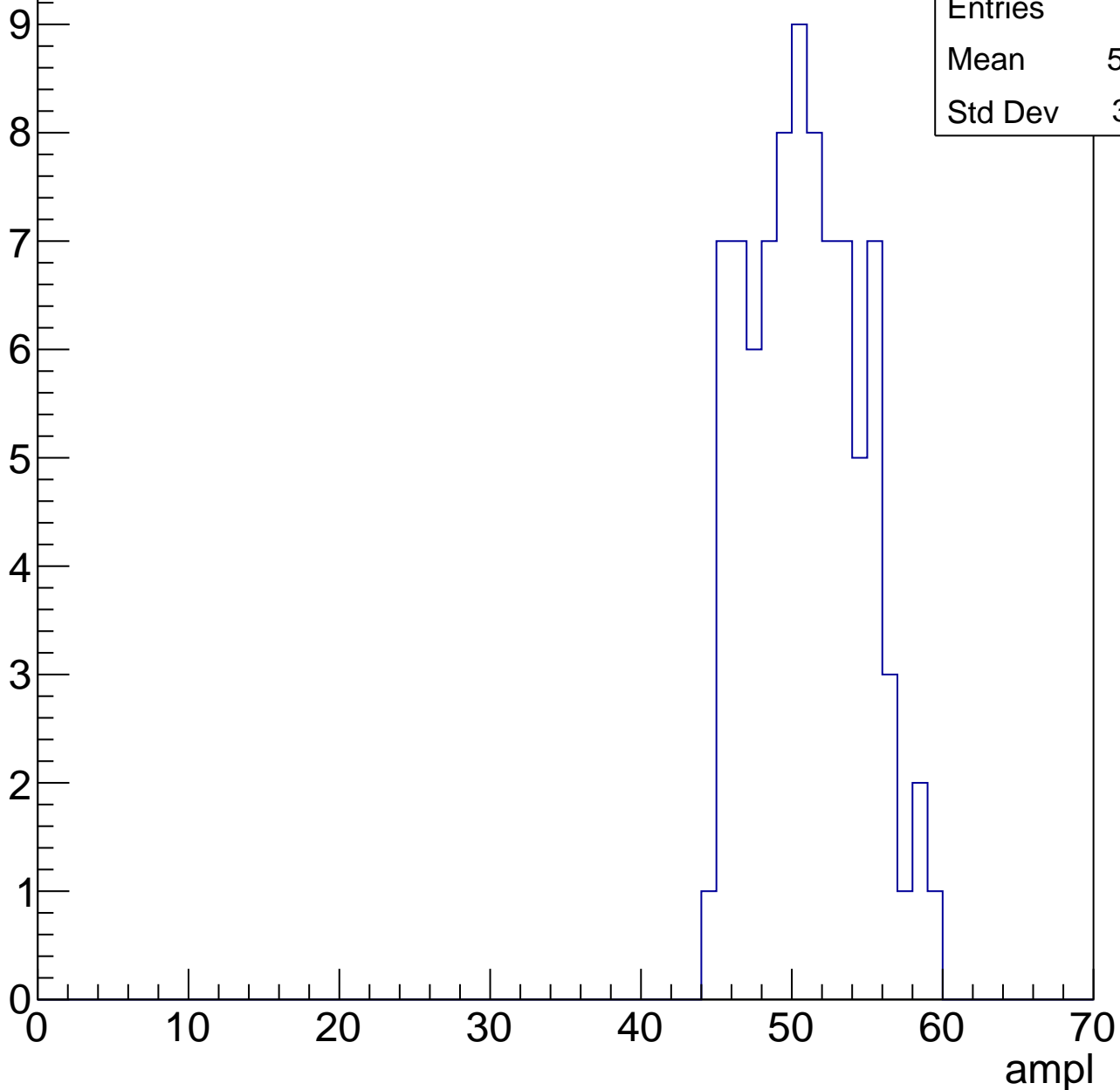


# B0L001S, U6-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	86
Mean	50.45
Std Dev	3.601



# B0L001S, U6-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

7

6

5

4

3

2

1

0

0

10

20

30

40

50

60

70

ampl

Entries

56

Mean

57.41

Std Dev

3.005

0

1

2

3

4

5

6

7

6

5

4

3

2

1

0

0

10

20

30

40

50

60

70

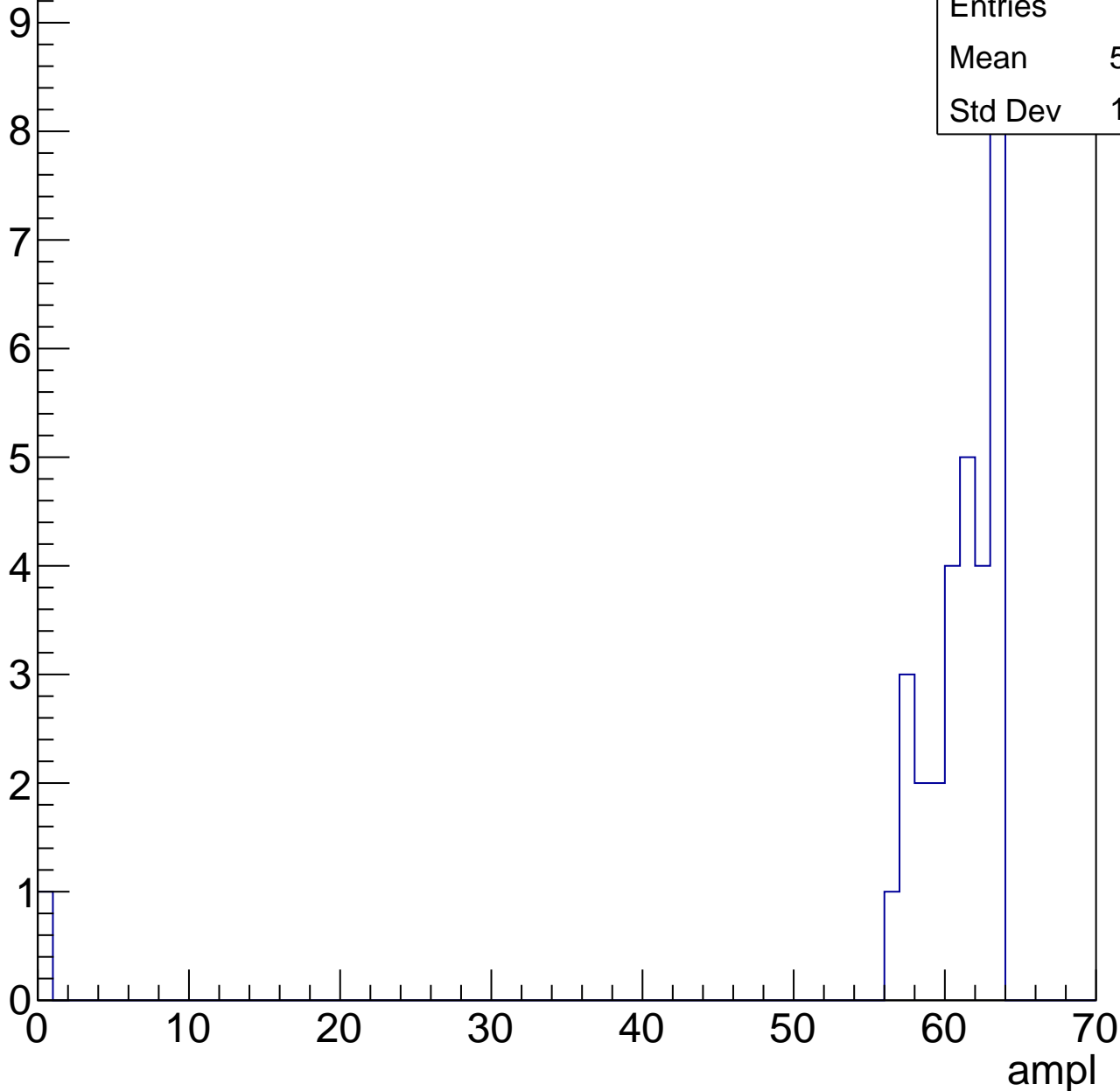
ampl

# B0L001S, U6-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	31
Mean	58.74
Std Dev	10.93



# B0L001S, U6-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch78, adc0

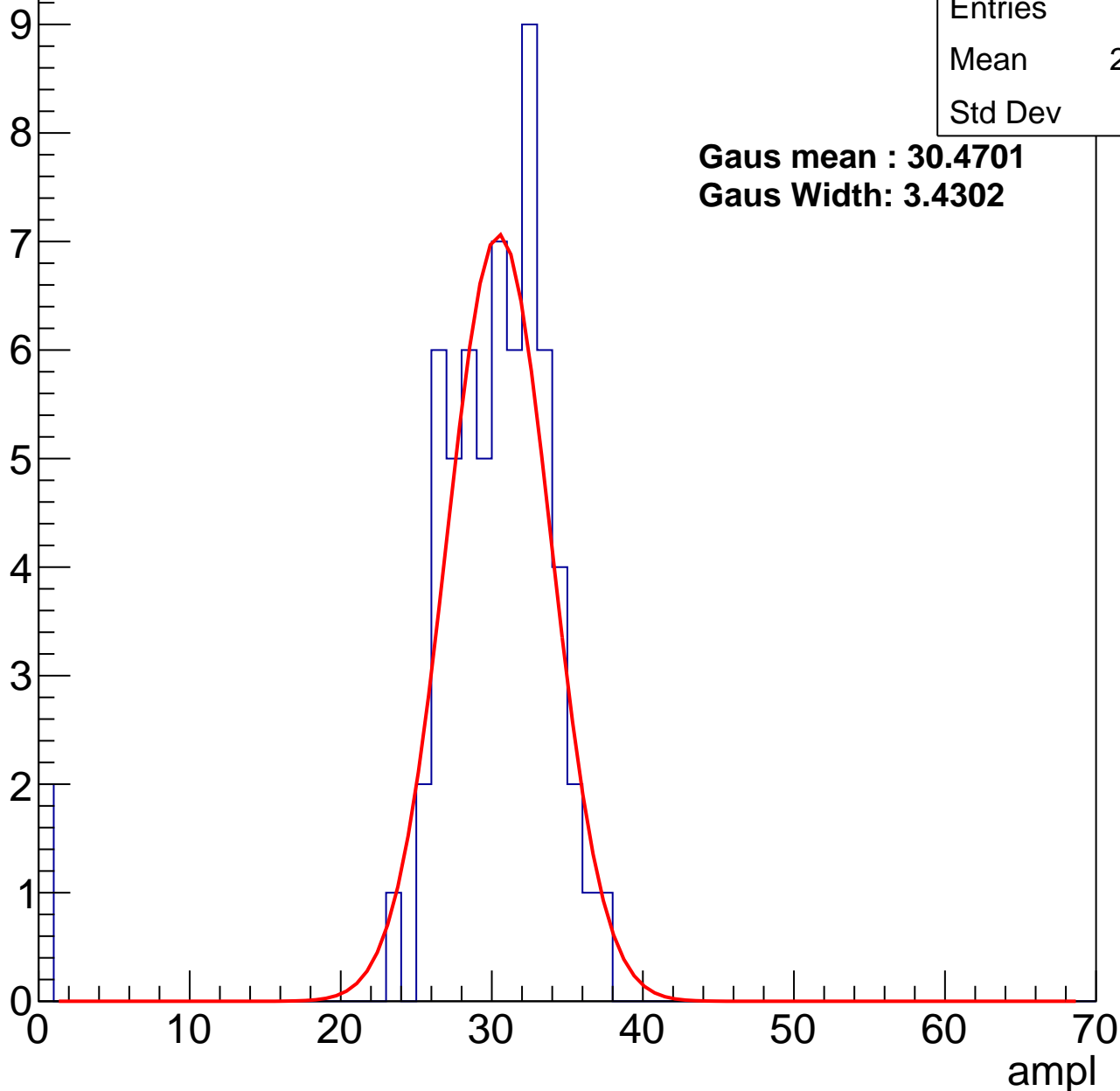
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	29.17
Std Dev	6.07

**Gaus mean : 30.4701**

**Gaus Width: 3.4302**



# B0L001S, U6-ch78, adc1

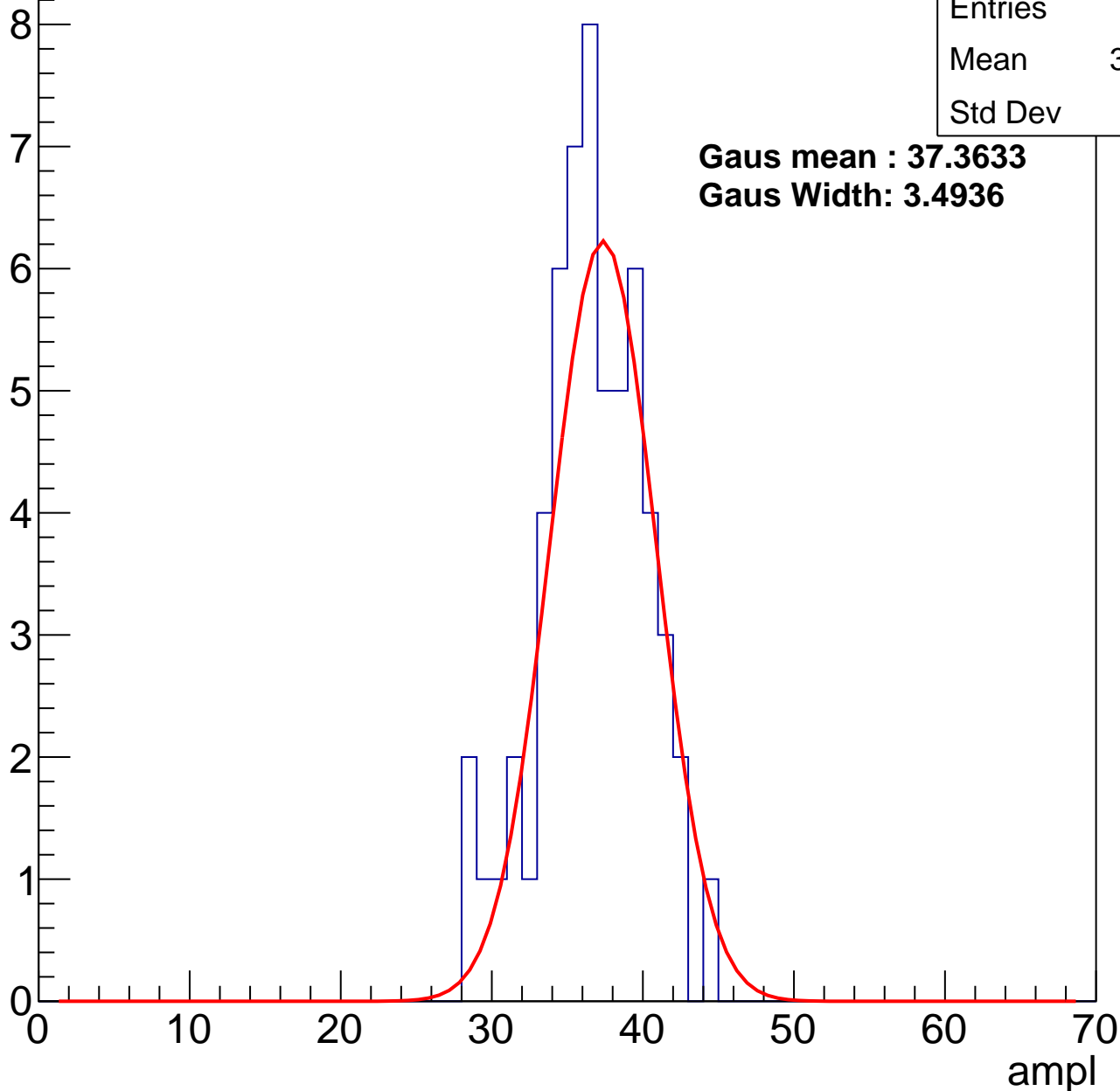
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	36.17
Std Dev	3.47

**Gaus mean : 37.3633**

**Gaus Width: 3.4936**



# B0L001S, U6-ch78, adc2

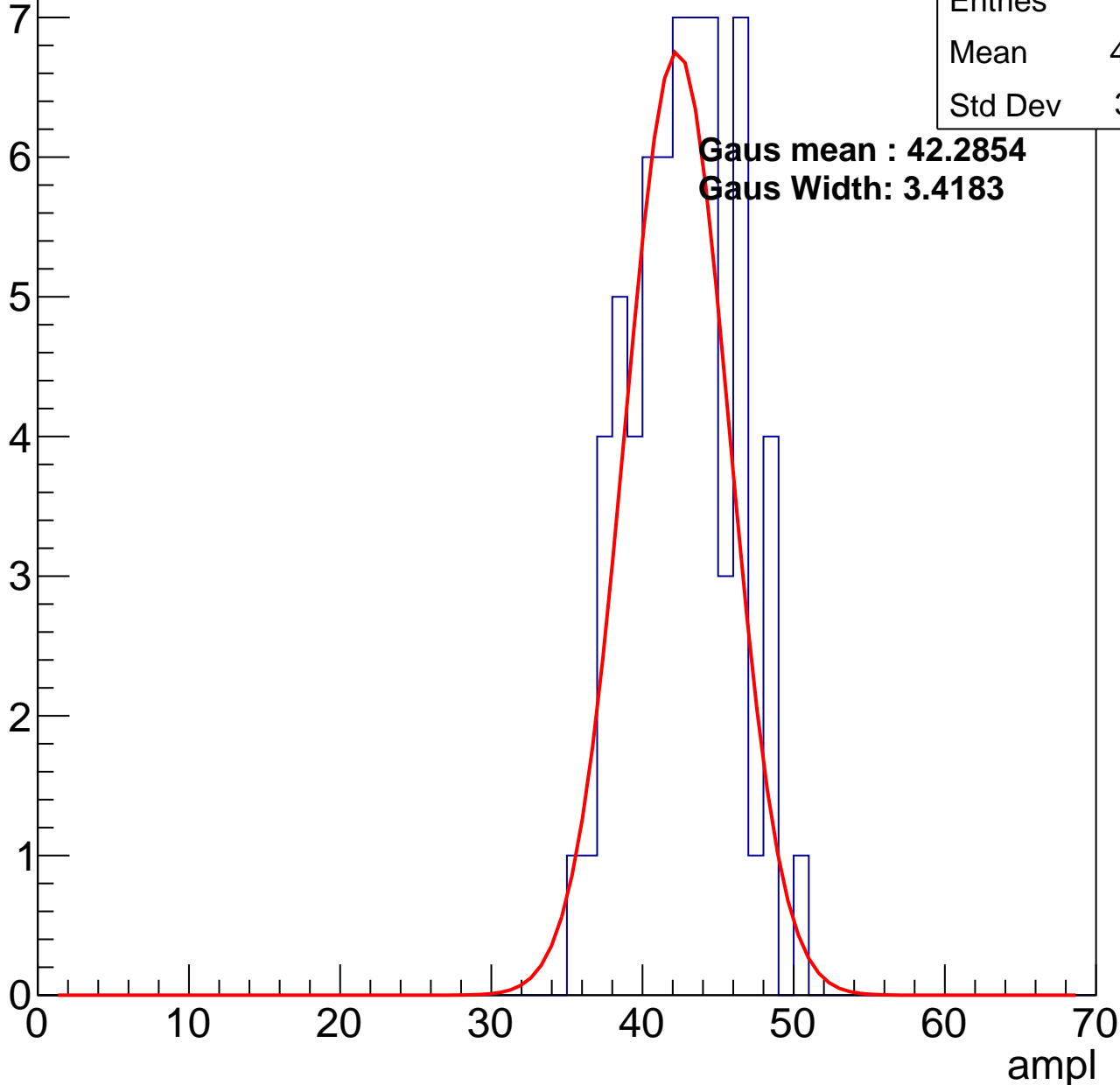
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	42.19
Std Dev	3.391

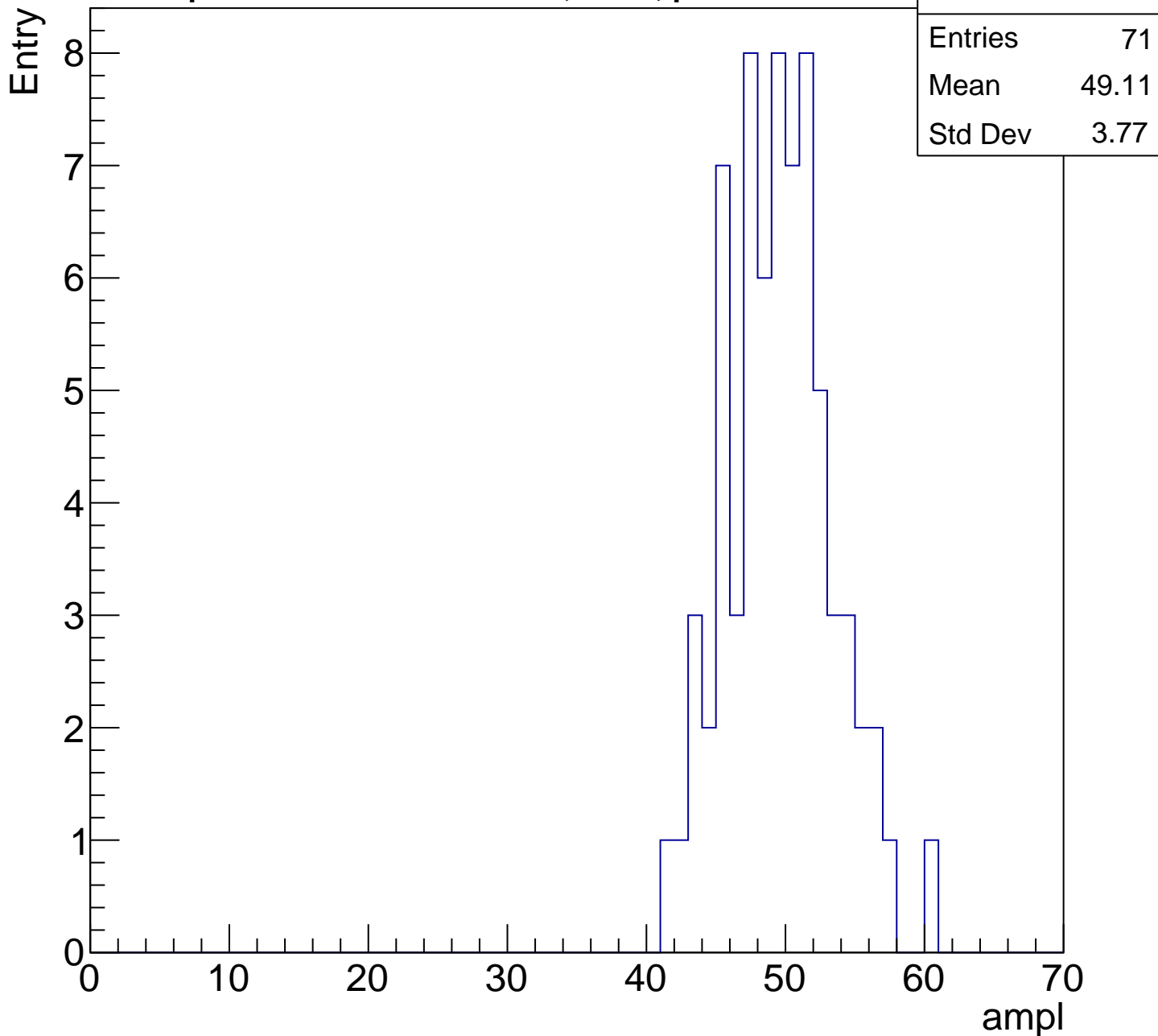
**Gaus mean : 42.2854**

**Gaus Width: 3.4183**



# B0L001S, U6-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

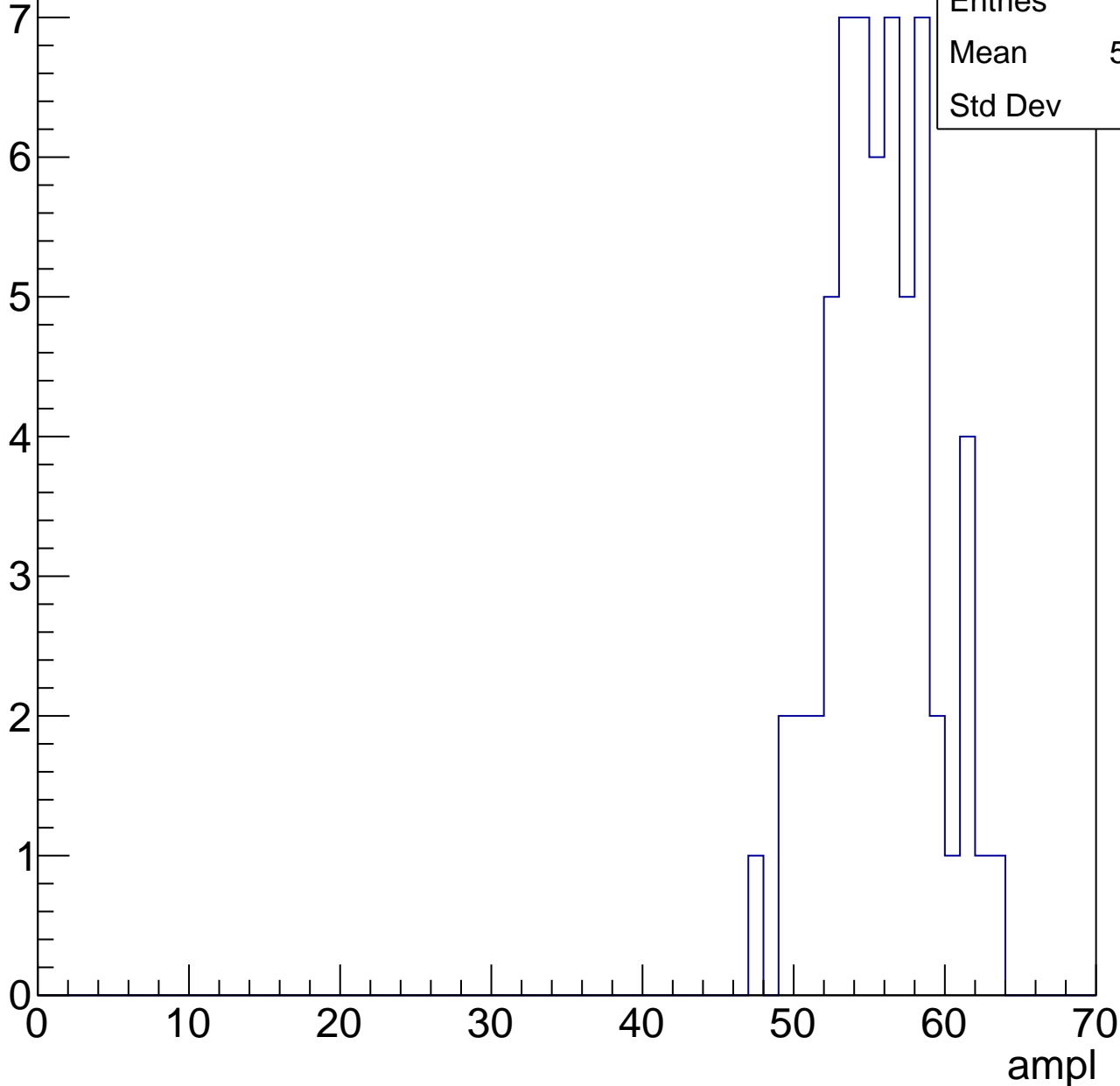


# B0L001S, U6-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	55.27
Std Dev	3.41

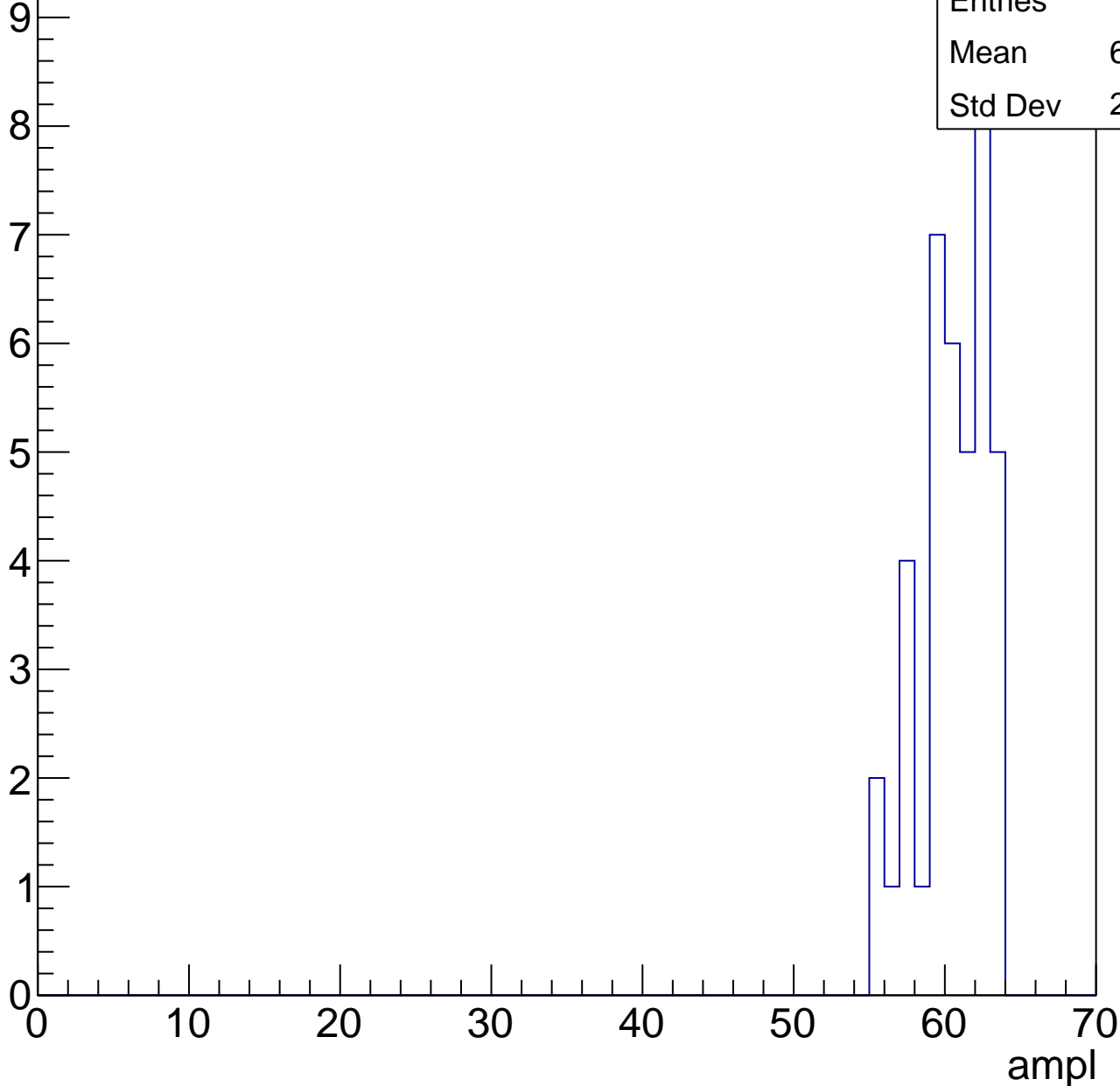


# B0L001S, U6-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

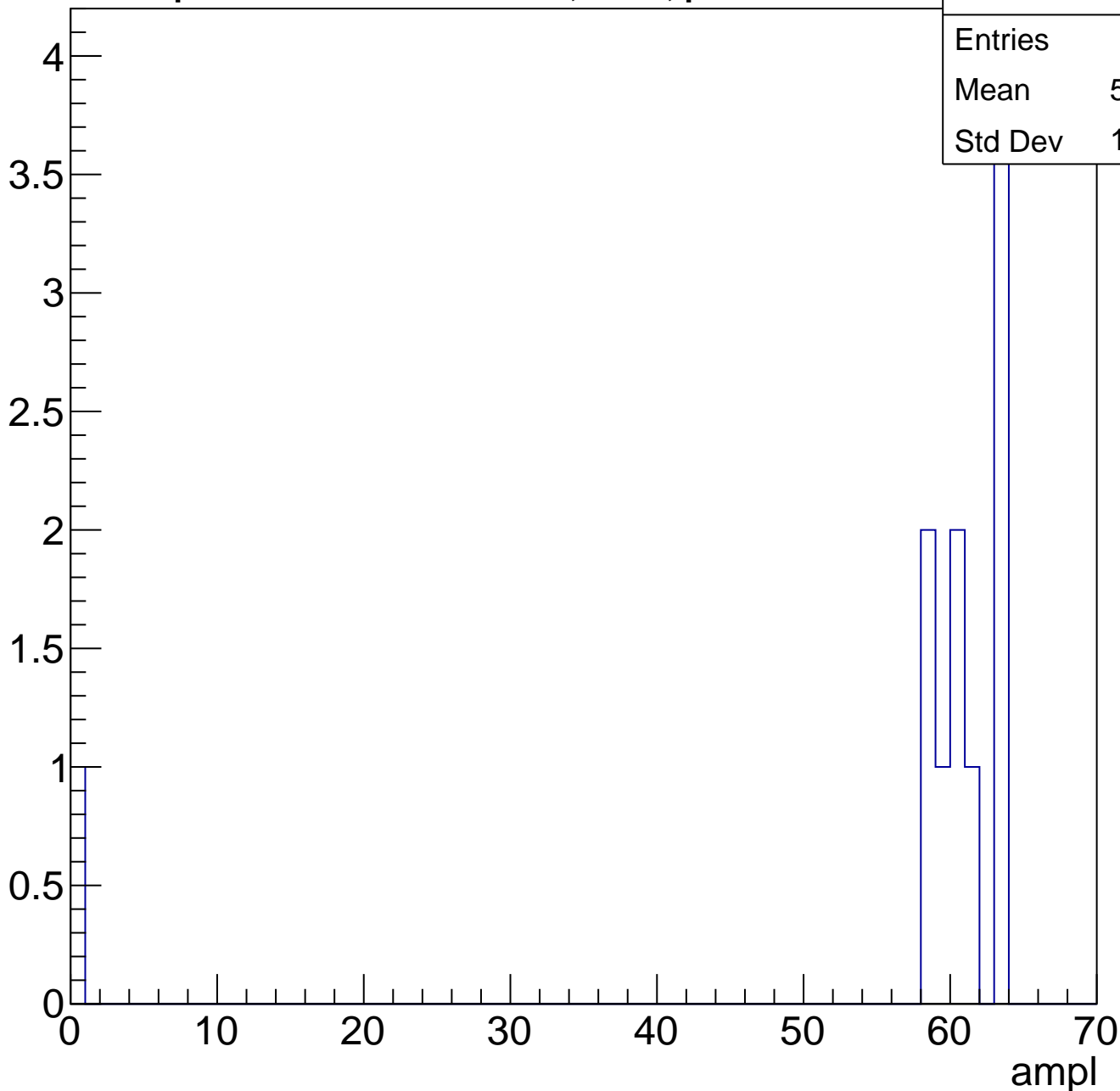
Entries	40
Mean	60.08
Std Dev	2.229



# B0L001S, U6-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch79, adc0

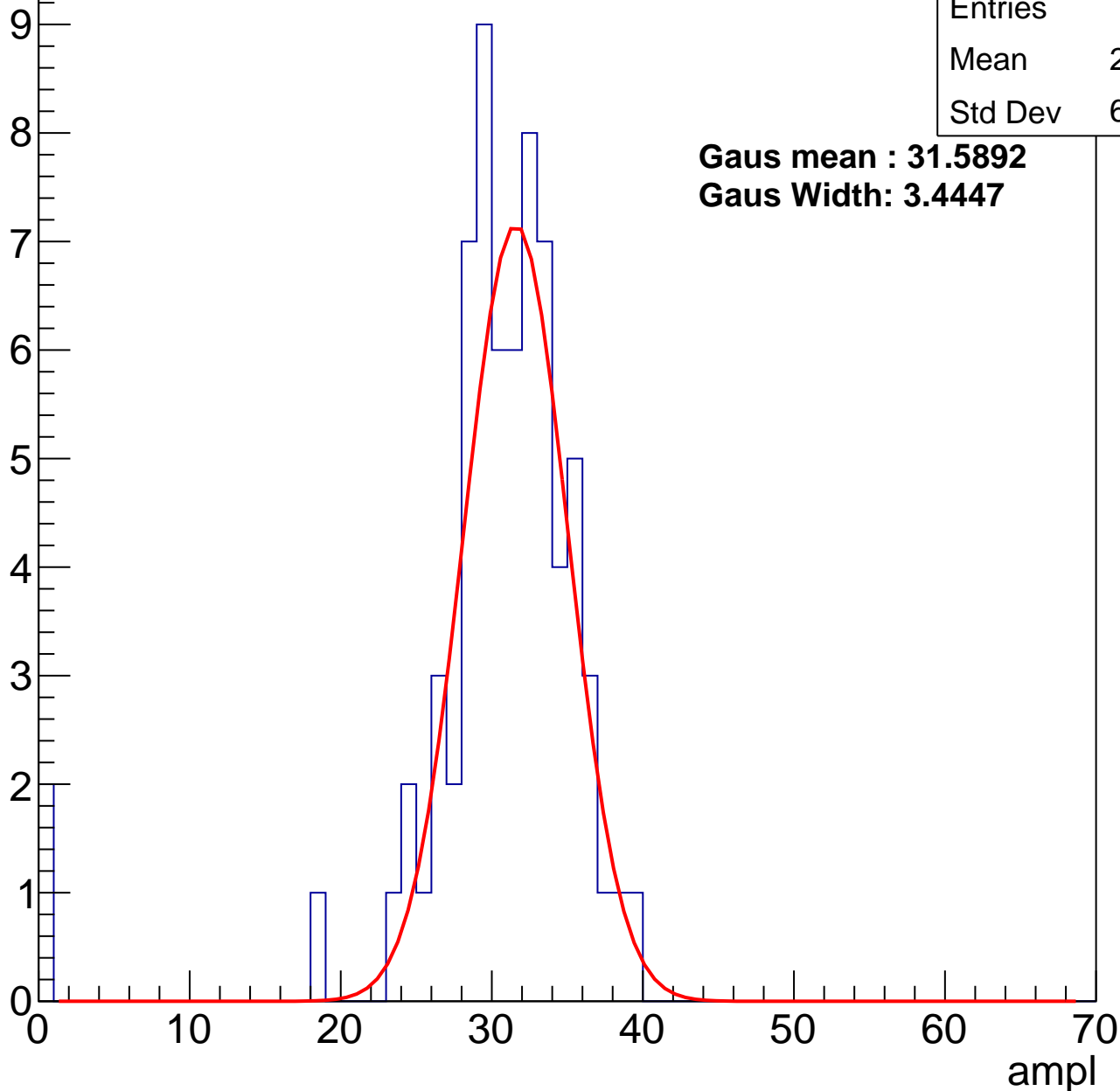
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	29.84
Std Dev	6.306

**Gaus mean : 31.5892**

**Gaus Width: 3.4447**



# B0L001S, U6-ch79, adc1

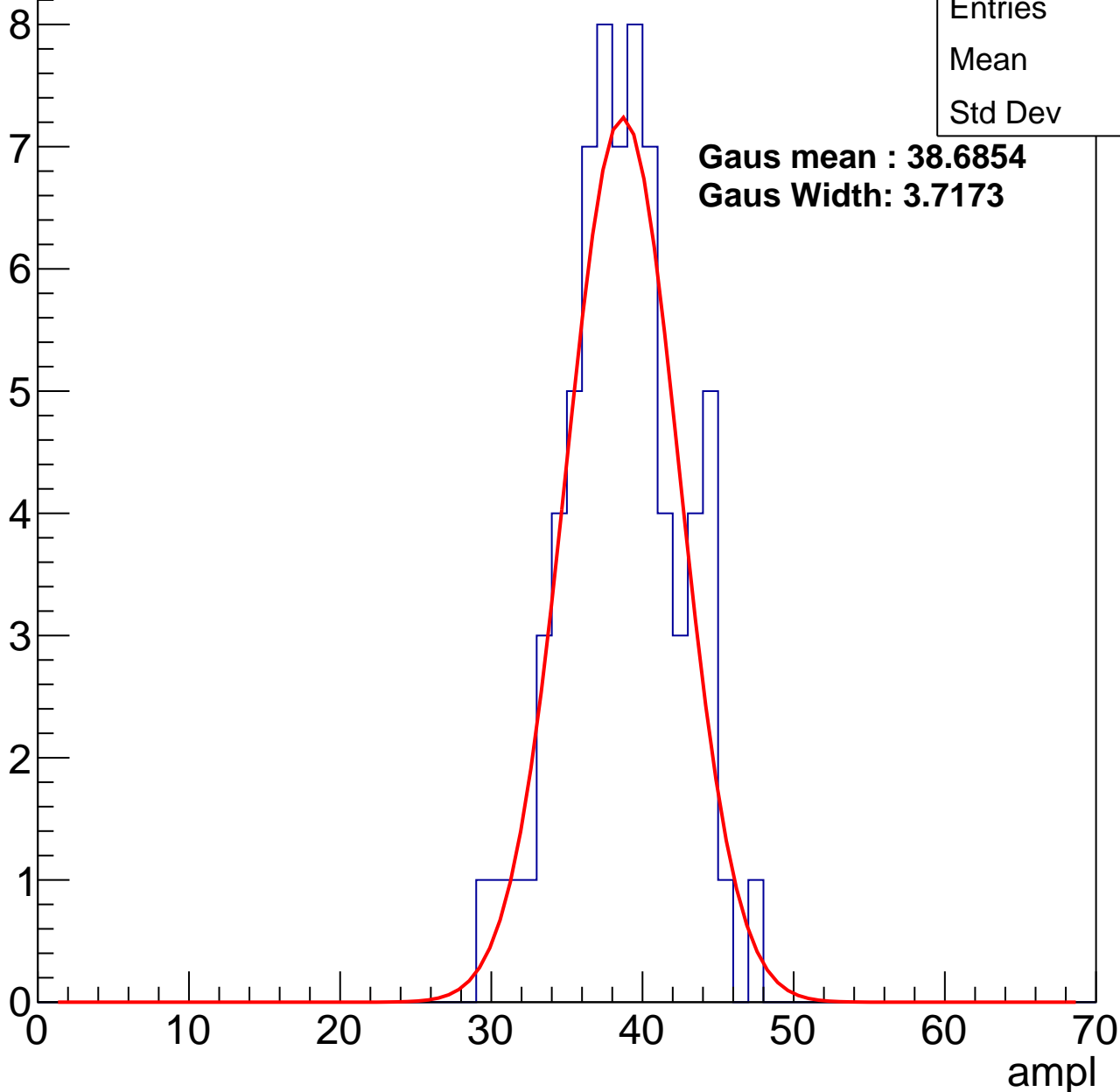
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	38.2
Std Dev	3.71

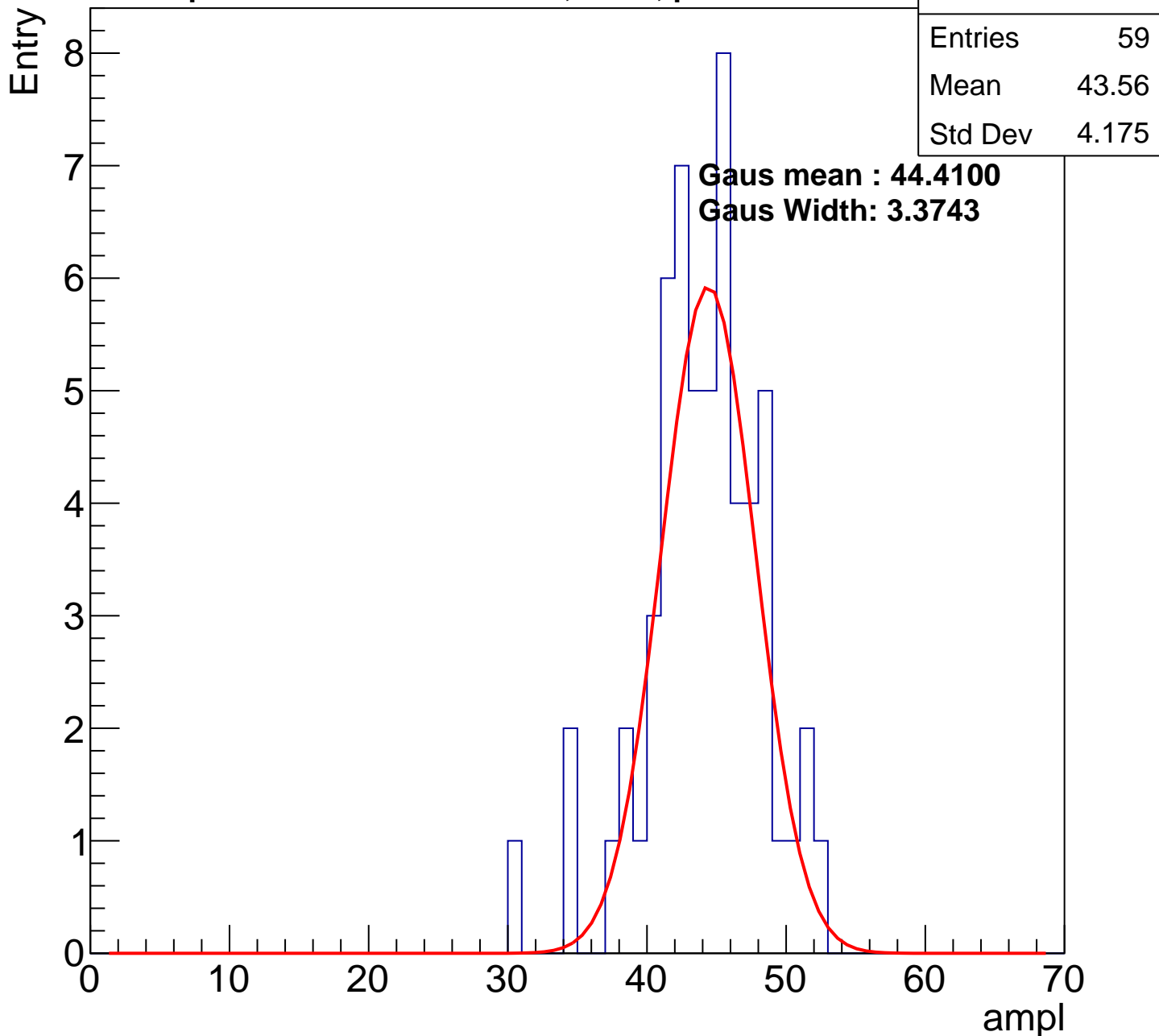
**Gaus mean : 38.6854**

**Gaus Width: 3.7173**



# B0L001S, U6-ch79, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

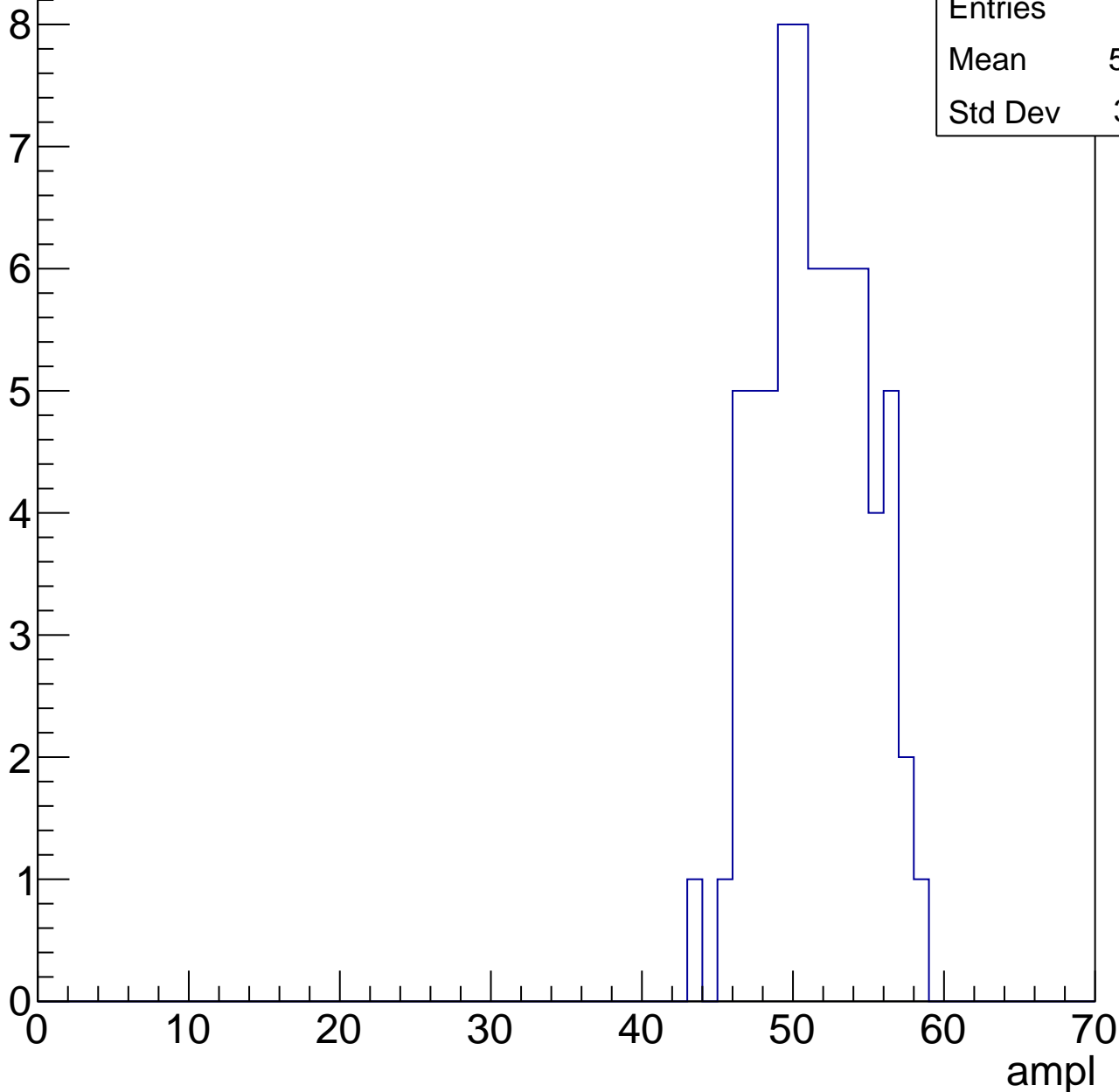


# B0L001S, U6-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	50.97
Std Dev	3.371

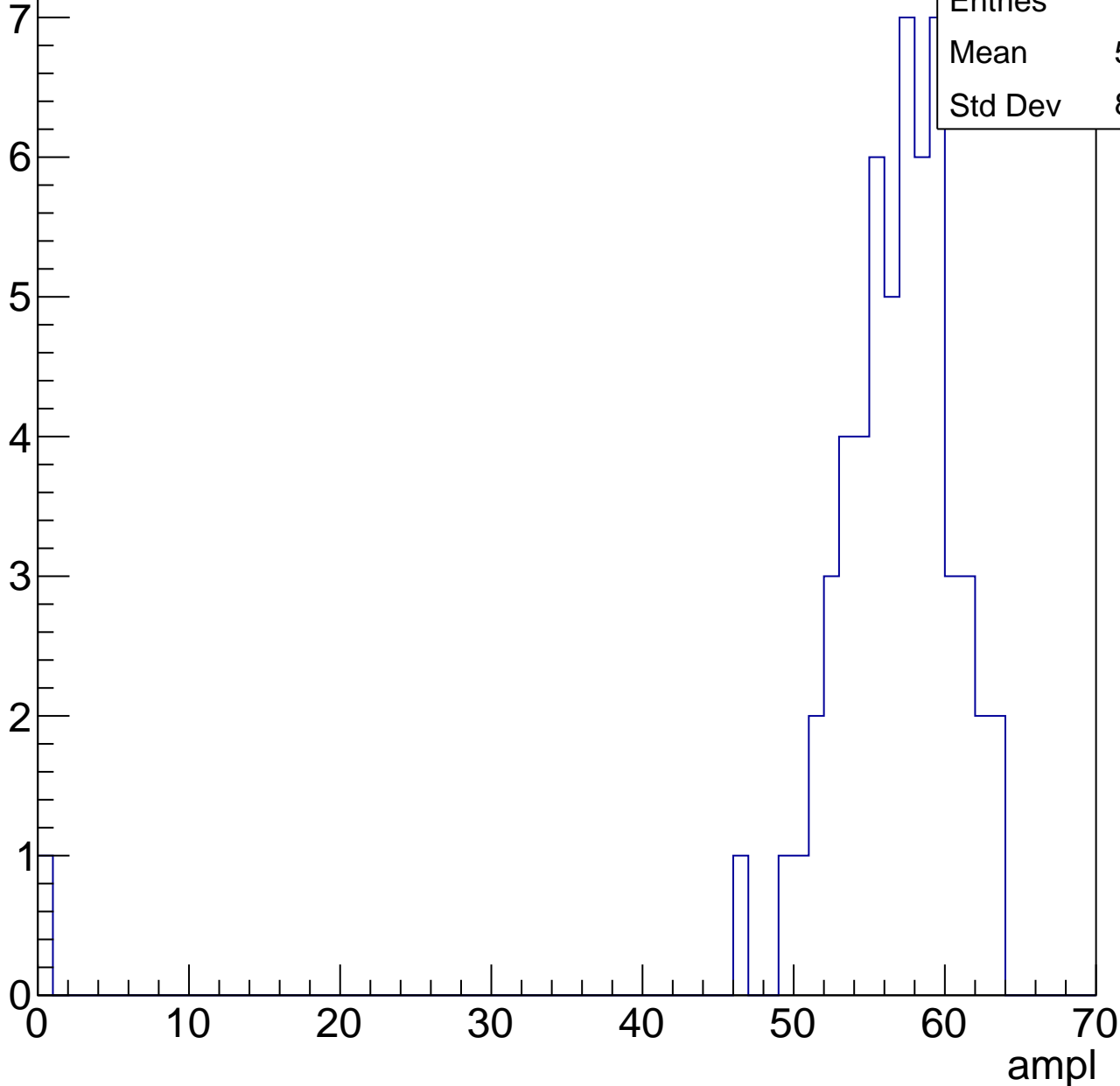


# B0L001S, U6-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

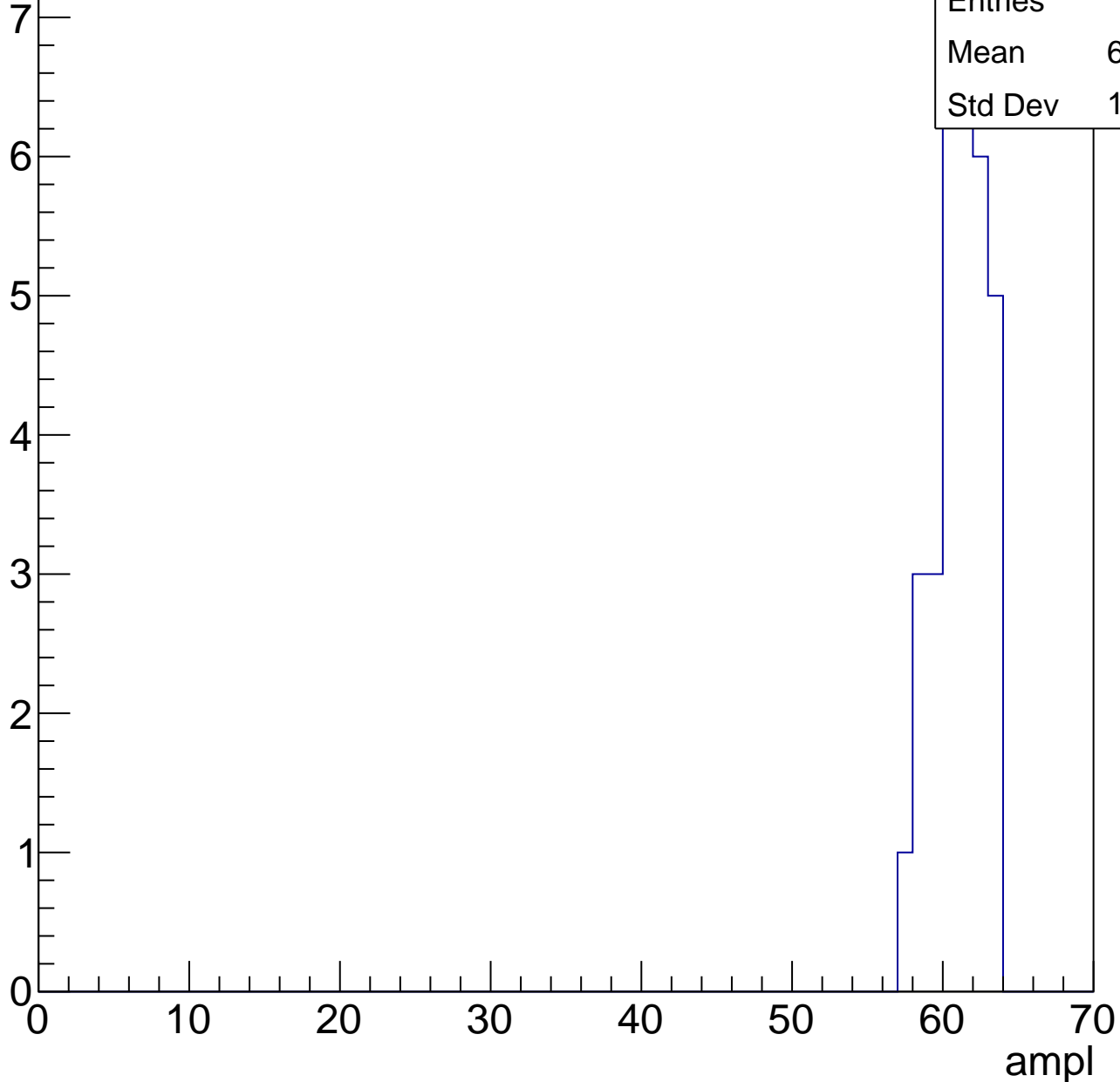
Entries	58
Mean	55.41
Std Dev	8.141



# B0L001S, U6-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U6-ch80, adc0

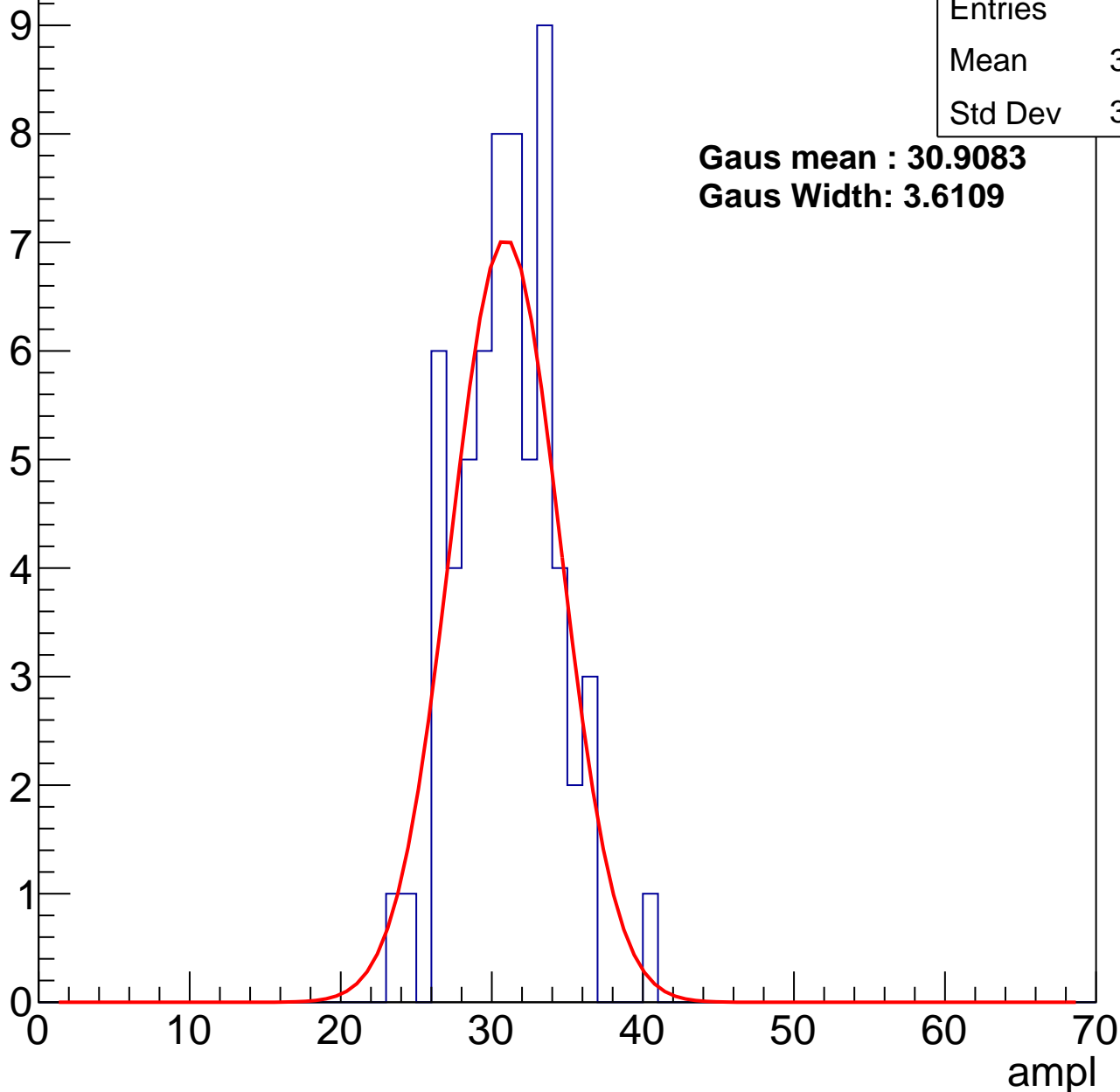
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	30.54
Std Dev	3.226

**Gaus mean : 30.9083**

**Gaus Width: 3.6109**



# B0L001S, U6-ch80, adc1

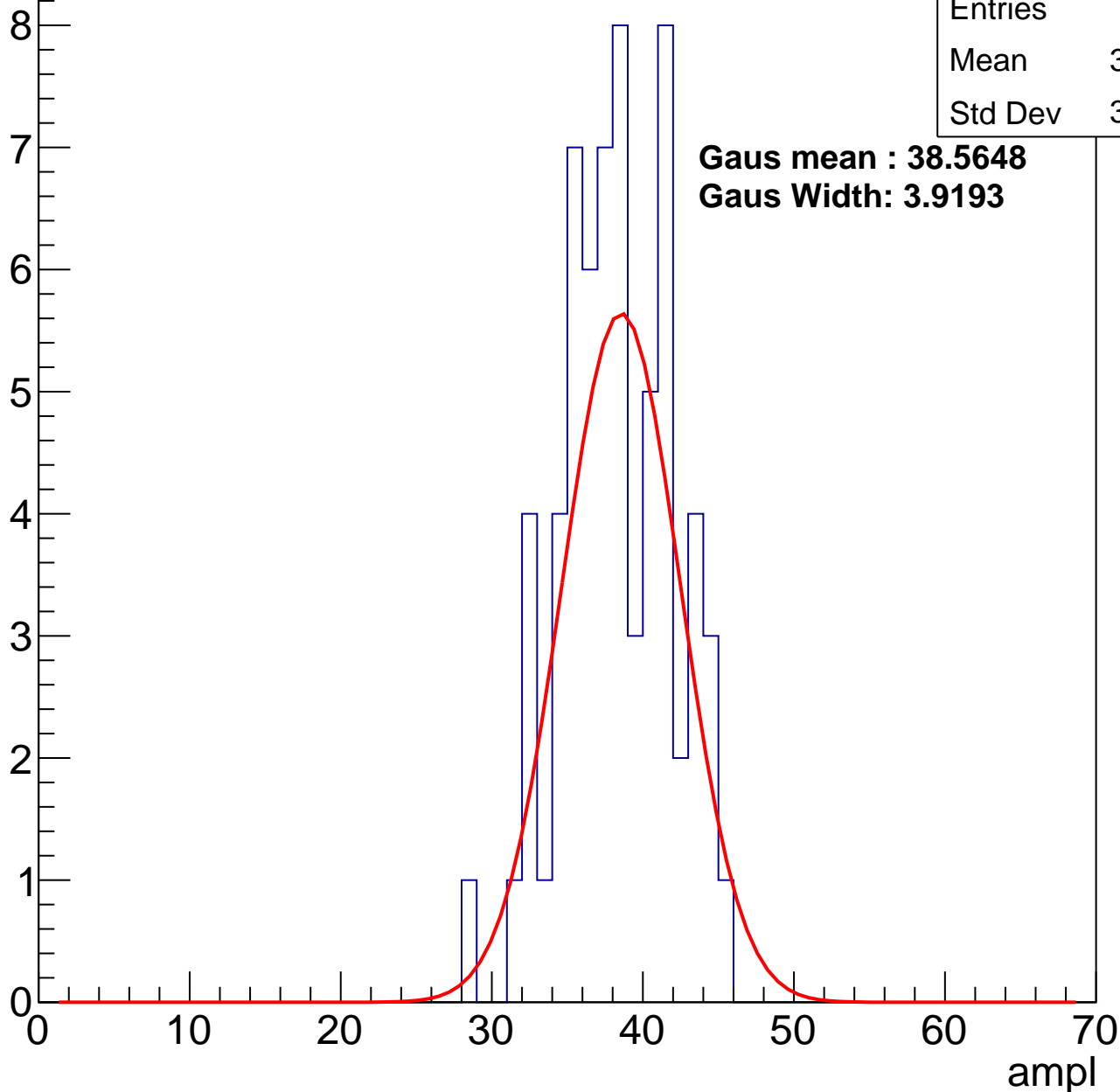
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	37.82
Std Dev	3.633

**Gaus mean : 38.5648**

**Gaus Width: 3.9193**



# B0L001S, U6-ch80, adc2

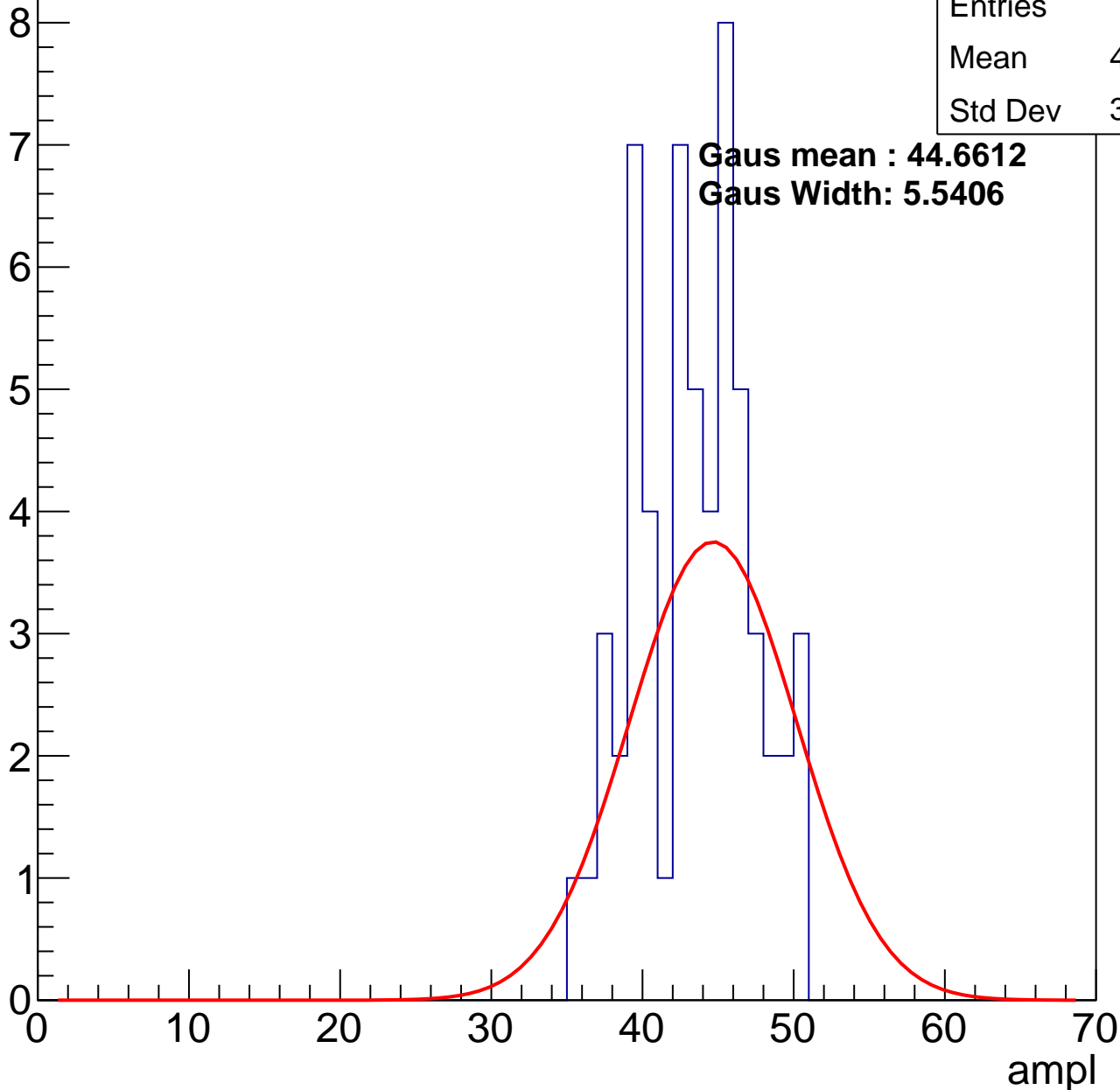
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	42.97
Std Dev	3.778

**Gaus mean : 44.6612**

**Gaus Width: 5.5406**

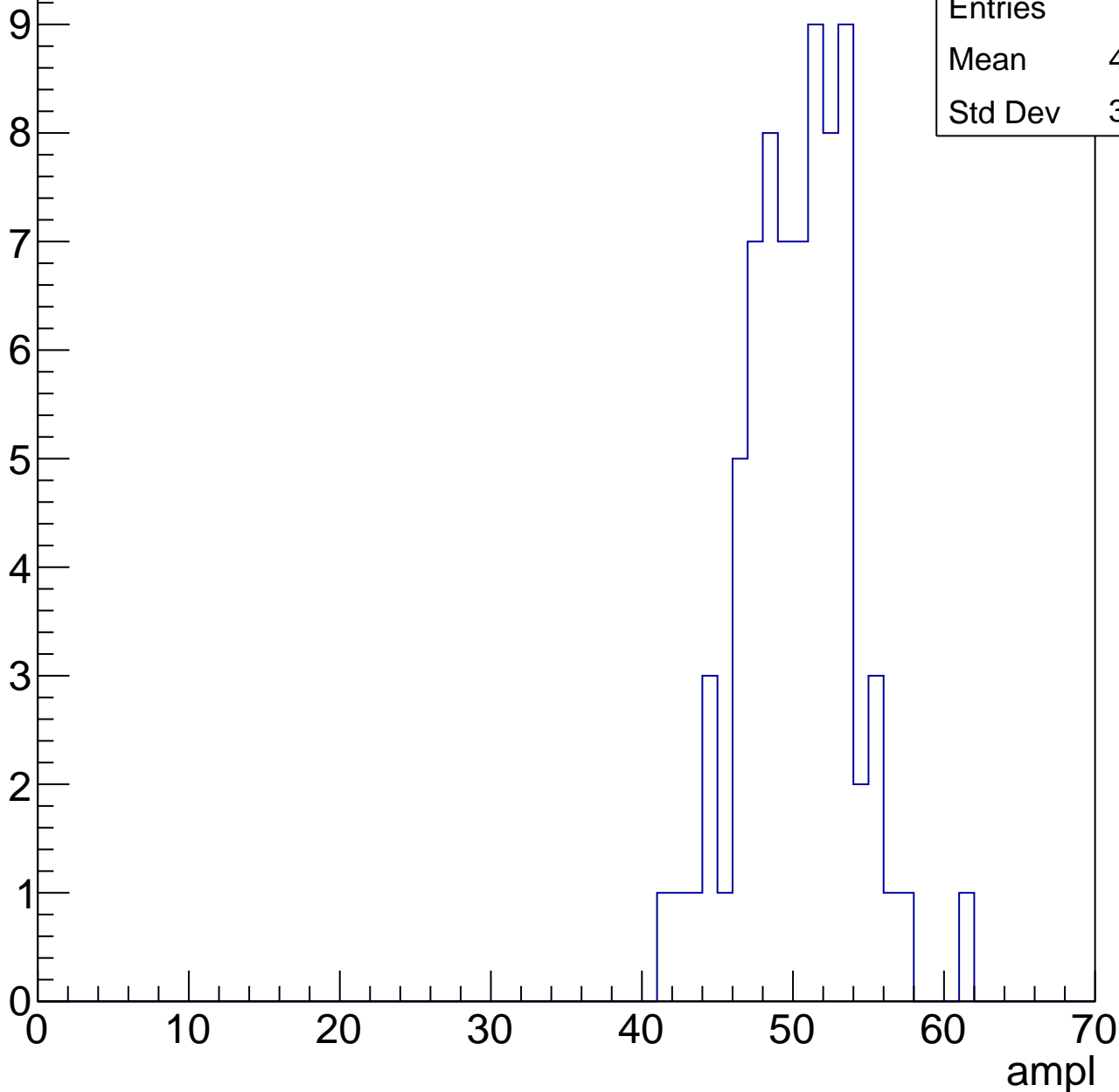


# B0L001S, U6-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	49.84
Std Dev	3.544

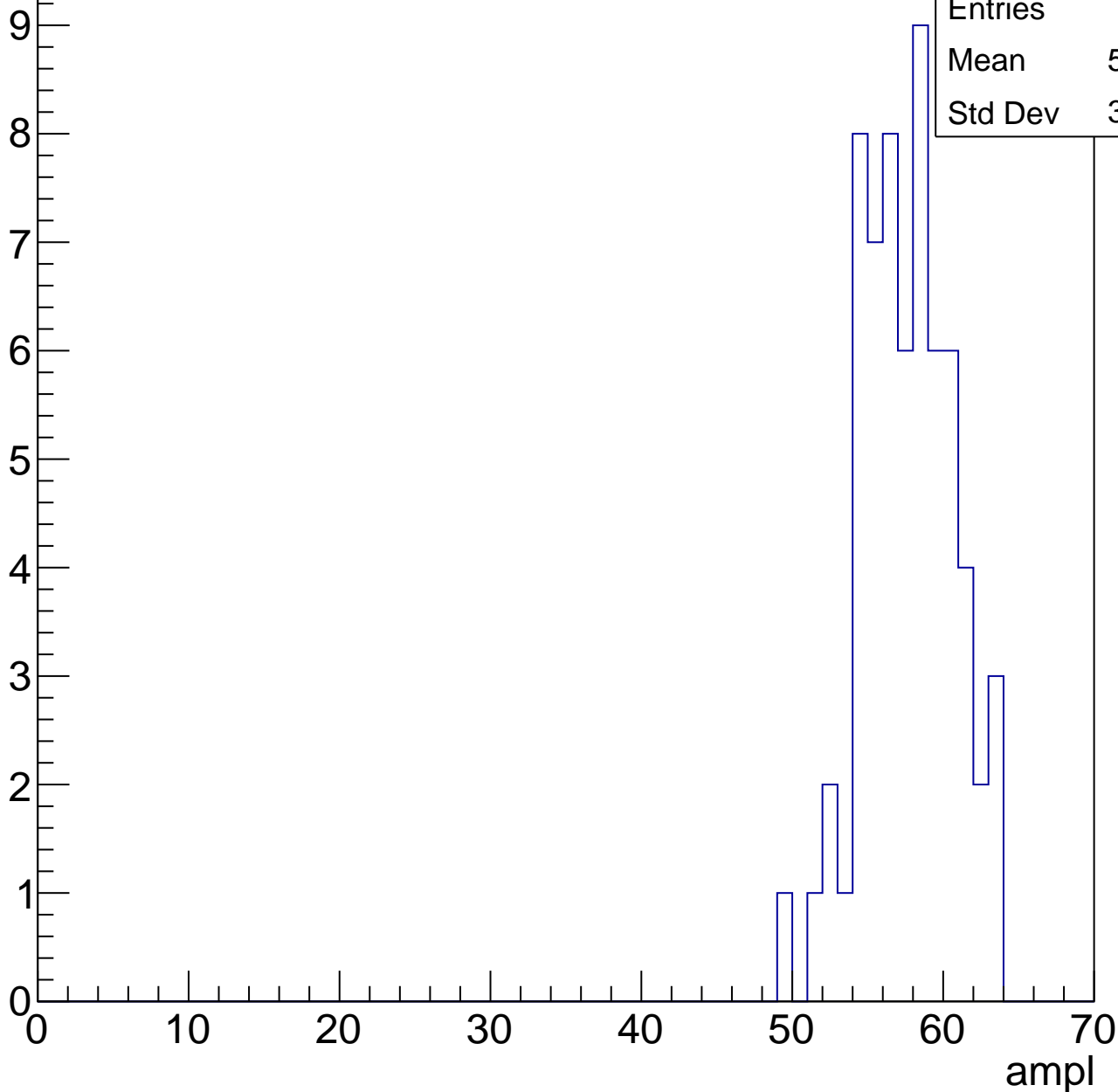


# B0L001S, U6-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	57.14
Std Dev	3.015

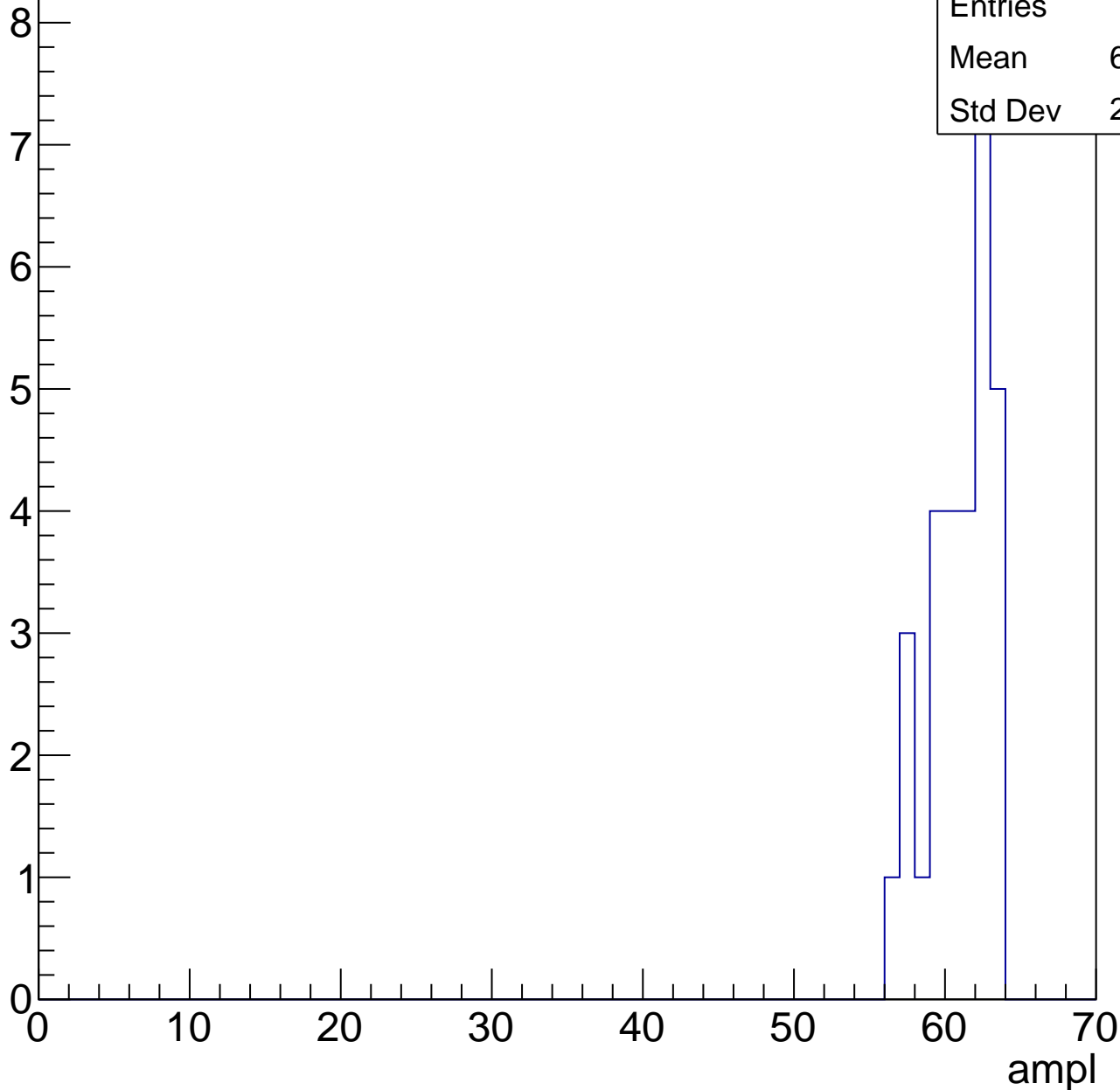


# B0L001S, U6-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	30
Mean	60.53
Std Dev	2.029



# B0L001S, U6-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

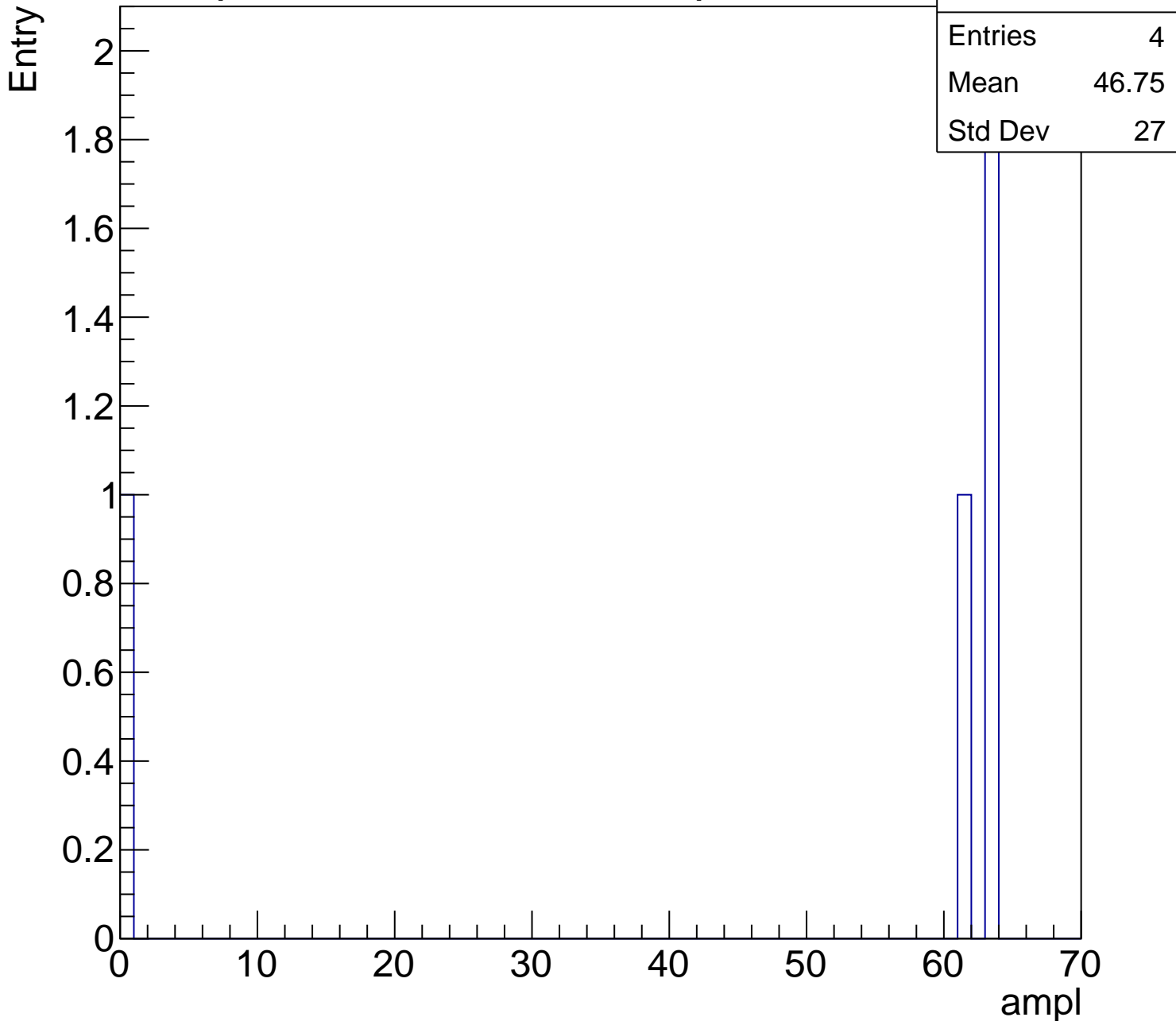
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	46.75
Std Dev	27

0 10 20 30 40 50 60 70

ampl





# B0L001S, U6-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch81, adc0

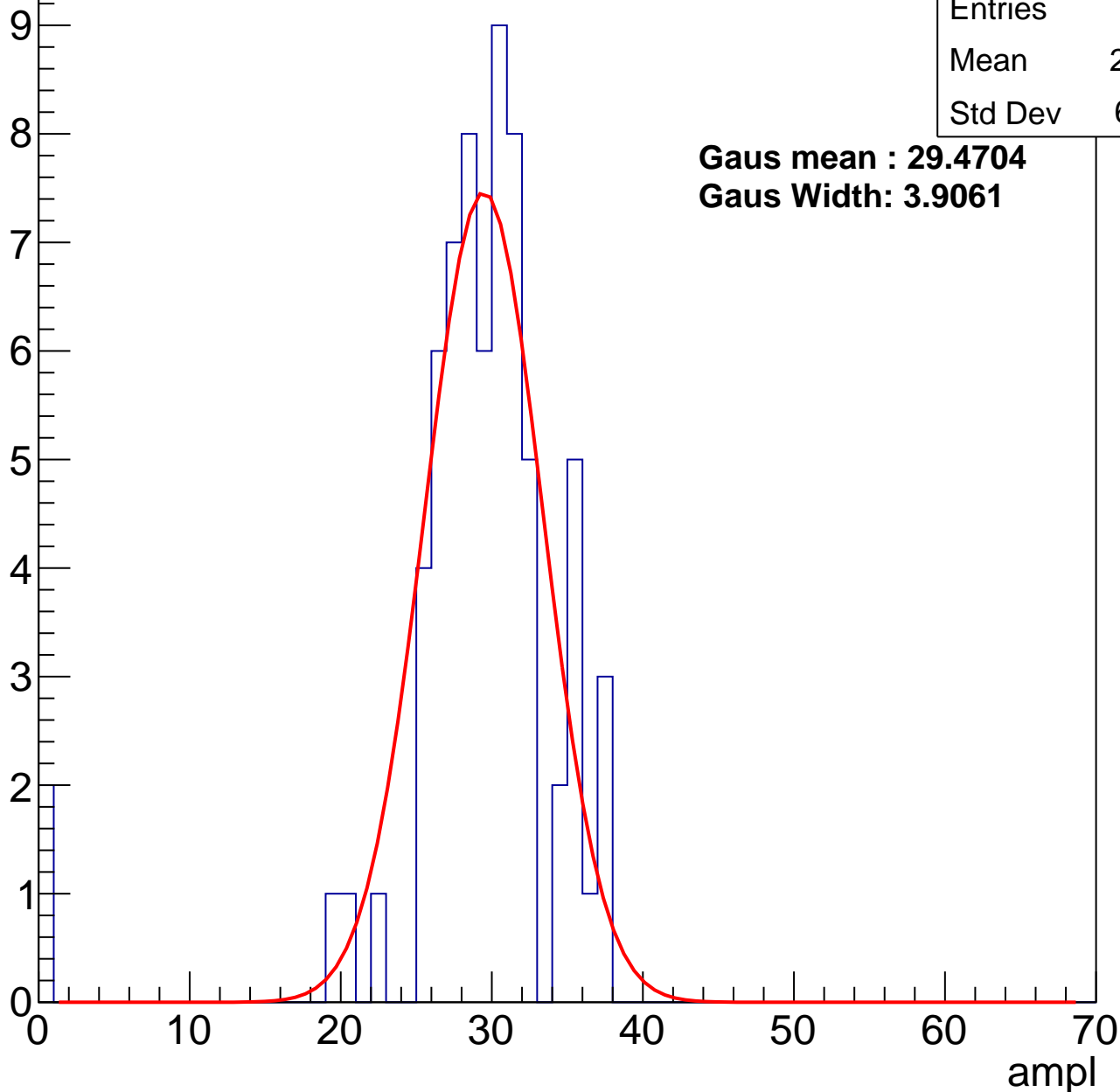
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	28.58
Std Dev	6.151

**Gaus mean : 29.4704**

**Gaus Width: 3.9061**



# B0L001S, U6-ch81, adc1

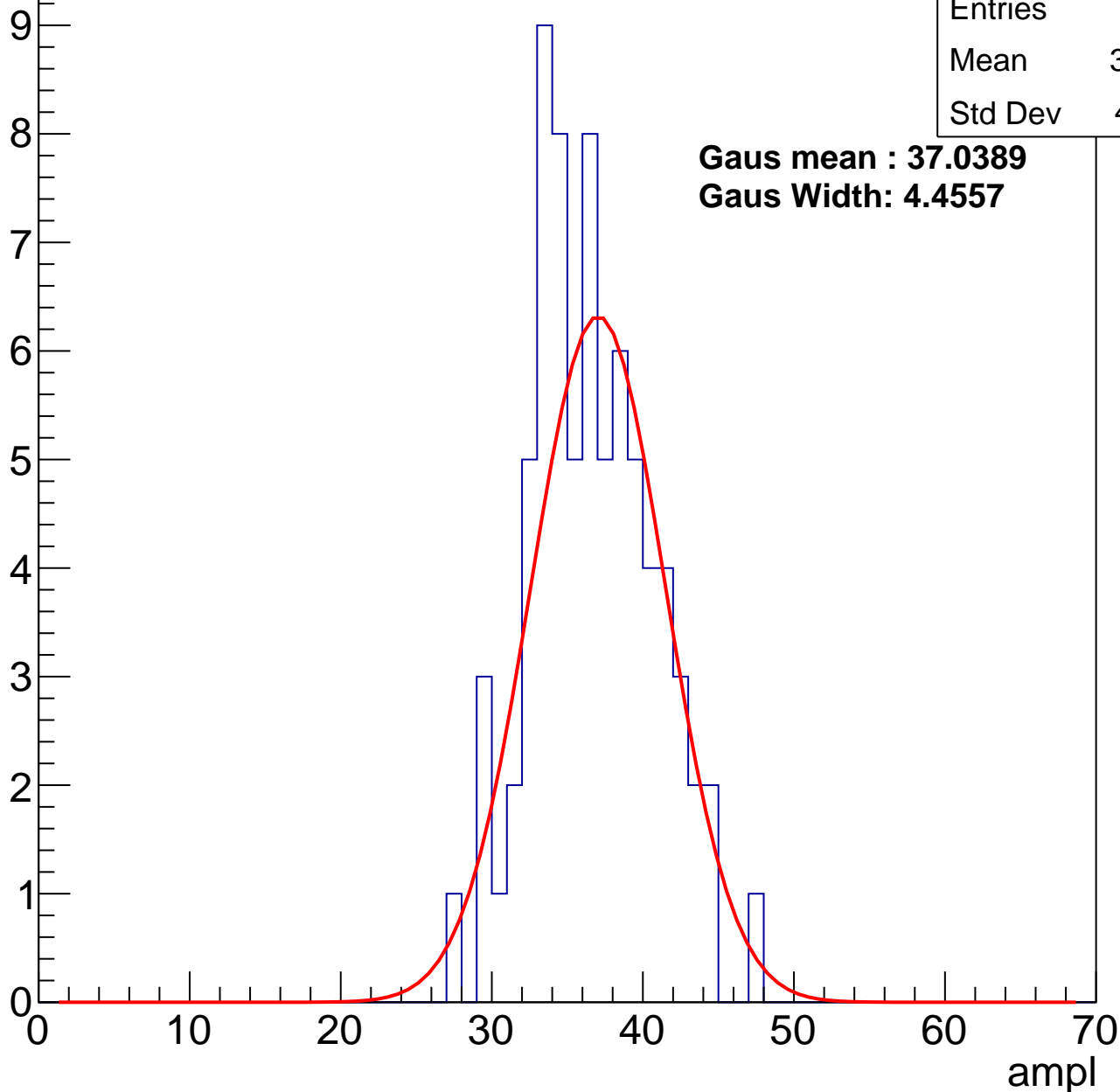
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	36.18
Std Dev	4.031

**Gaus mean : 37.0389**

**Gaus Width: 4.4557**



# B0L001S, U6-ch81, adc2

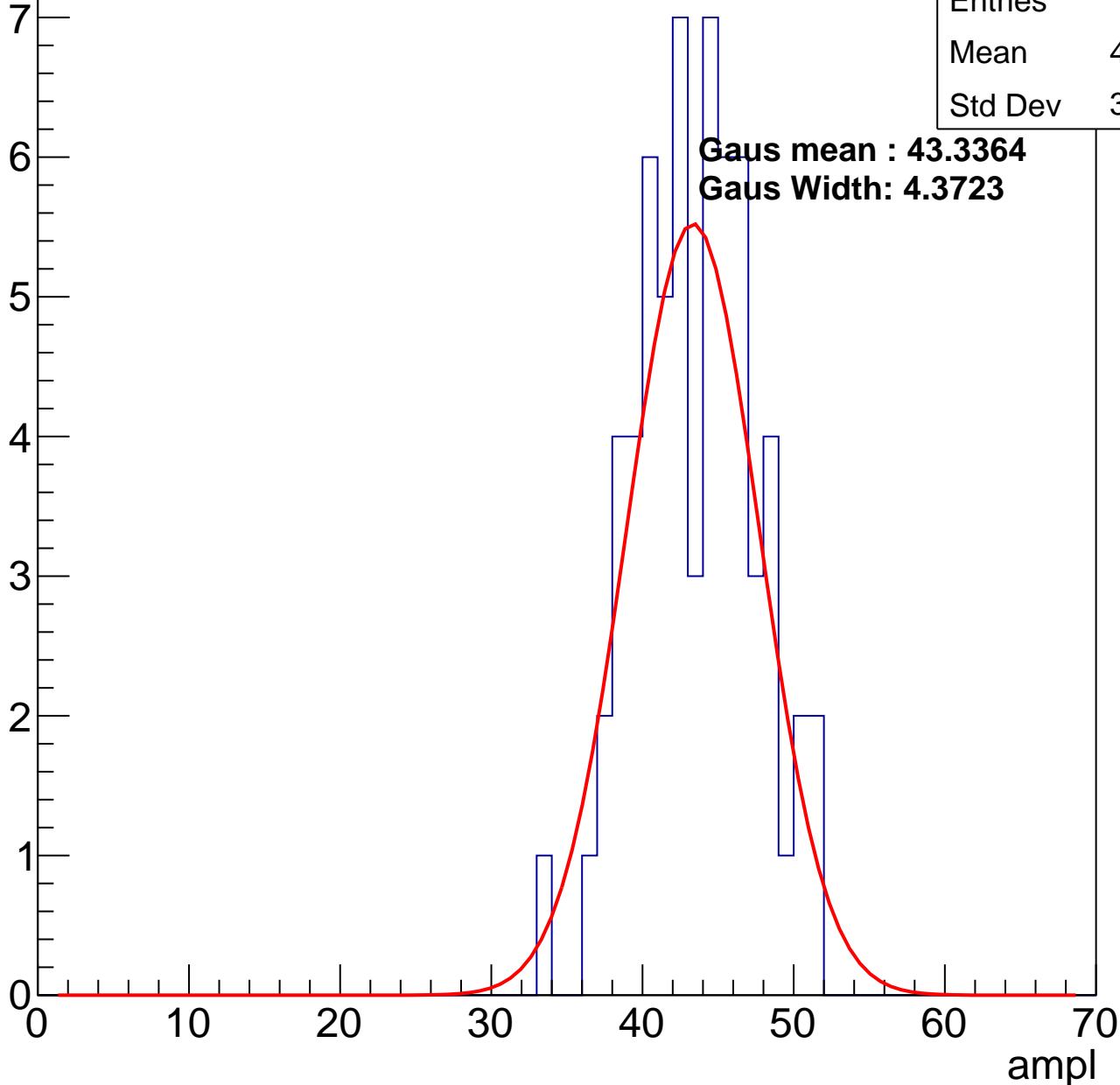
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	43.08
Std Dev	3.874

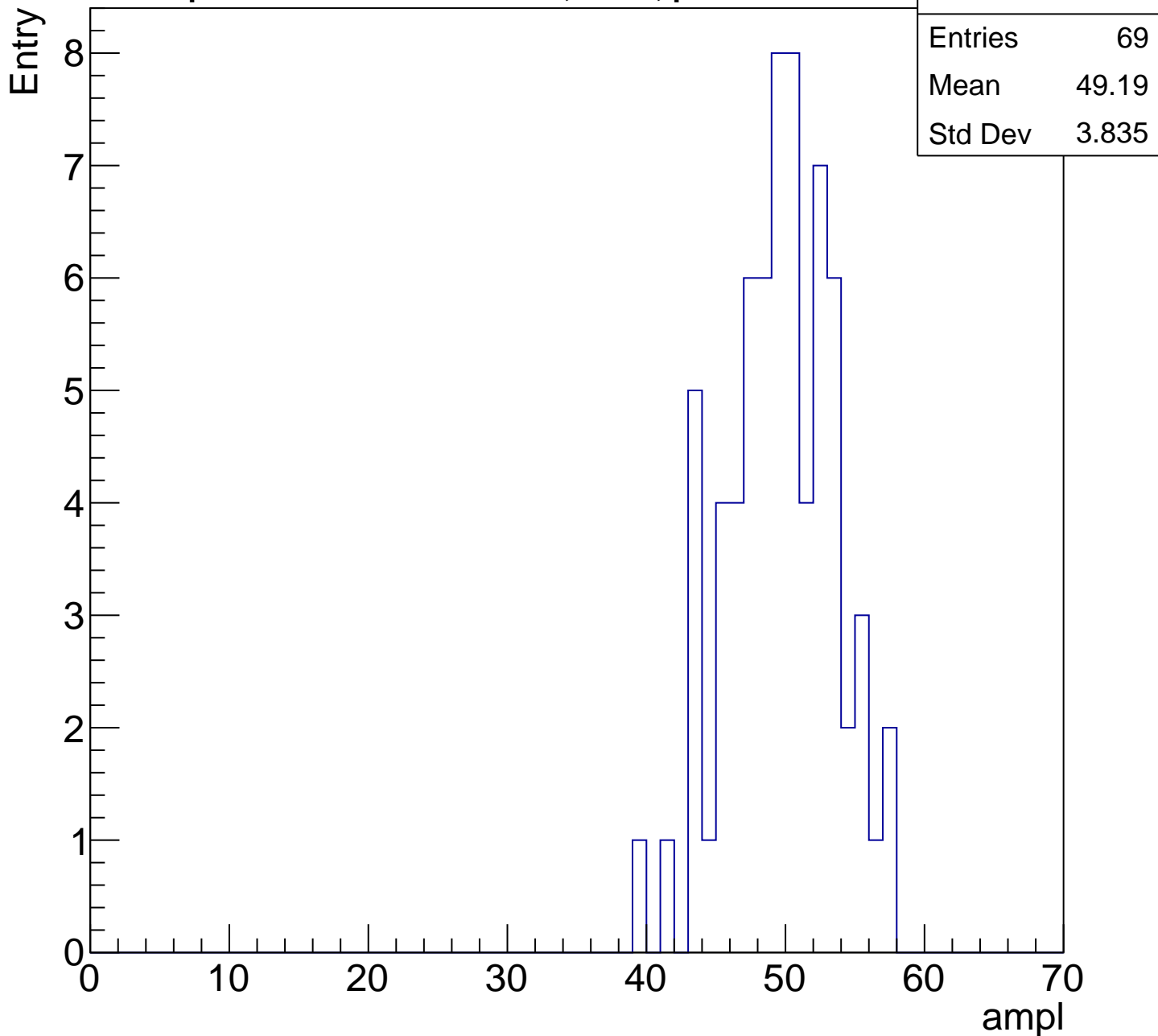
**Gaus mean : 43.3364**

**Gaus Width: 4.3723**



# B0L001S, U6-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

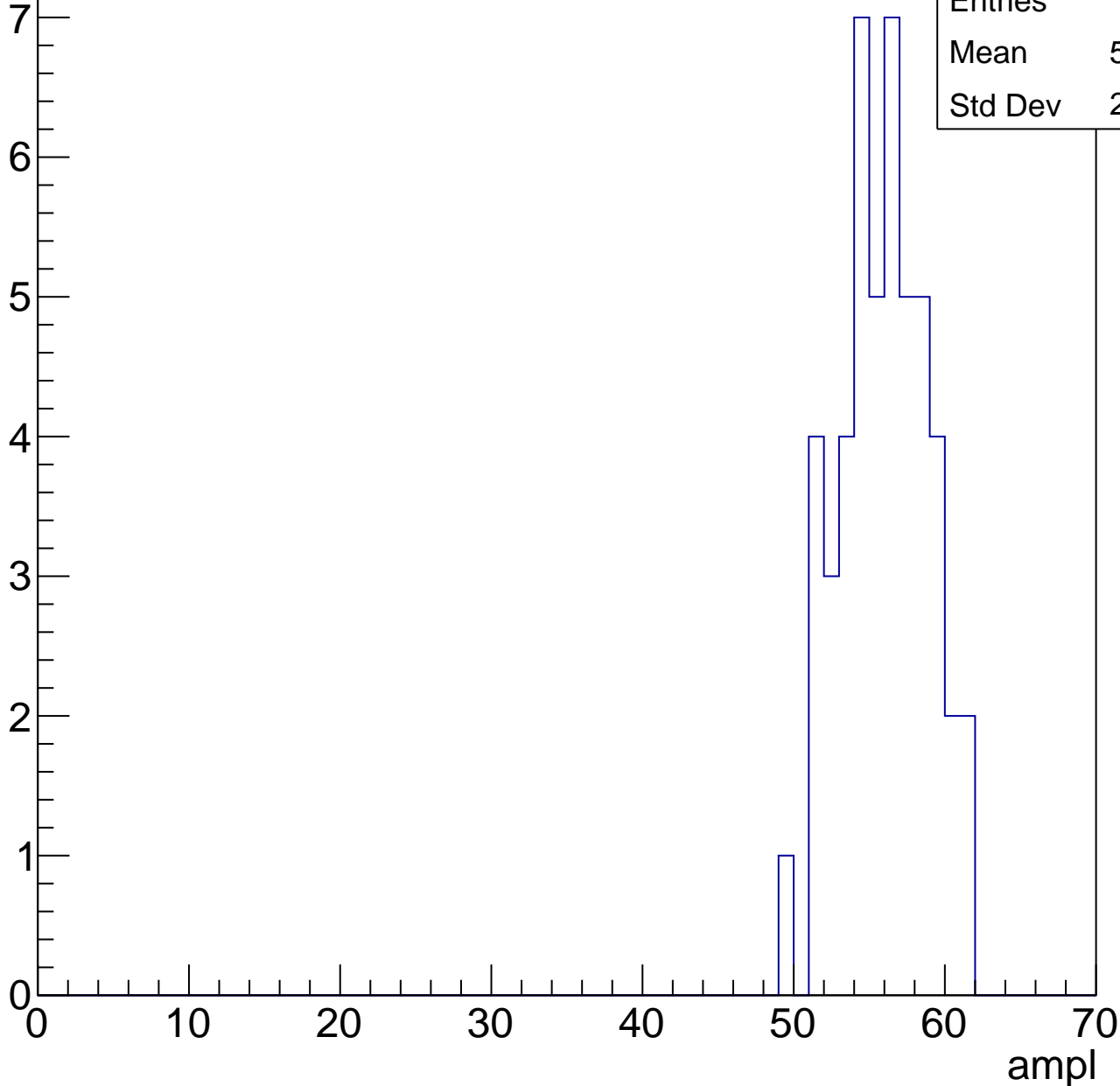


# B0L001S, U6-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	55.49
Std Dev	2.844

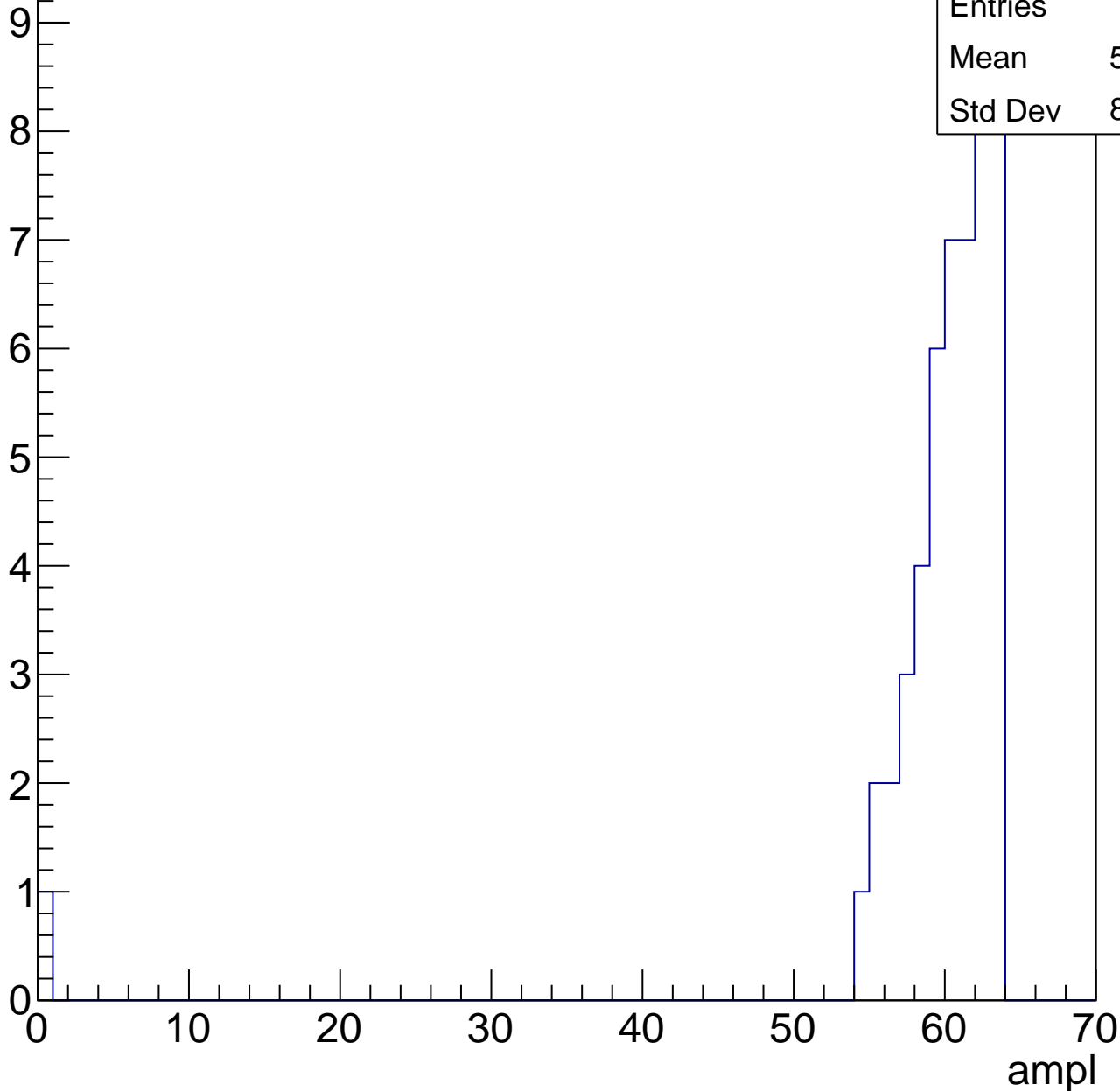


# B0L001S, U6-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

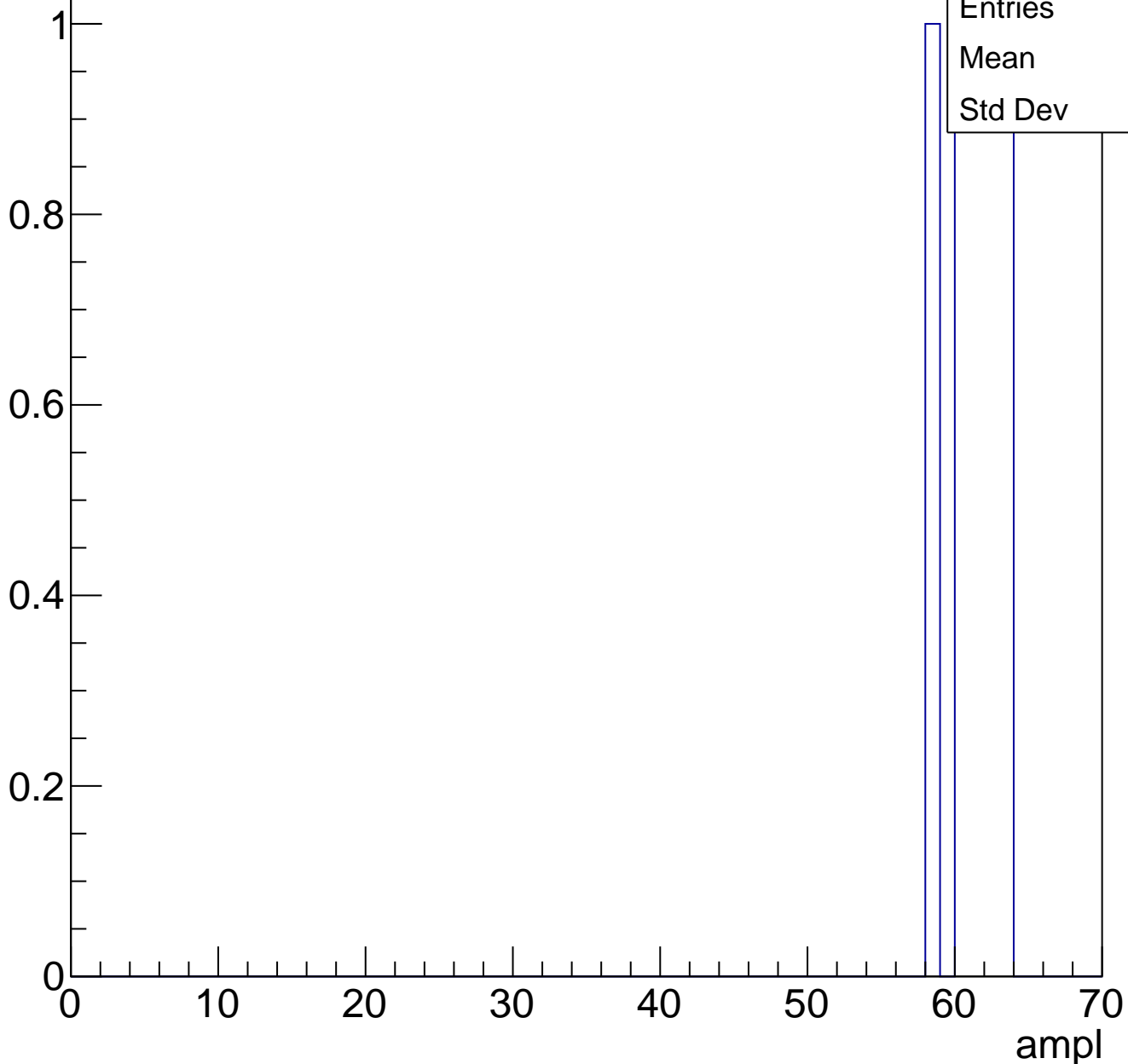
Entries	51
Mean	58.92
Std Dev	8.668



# B0L001S, U6-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U6-ch82, adc0

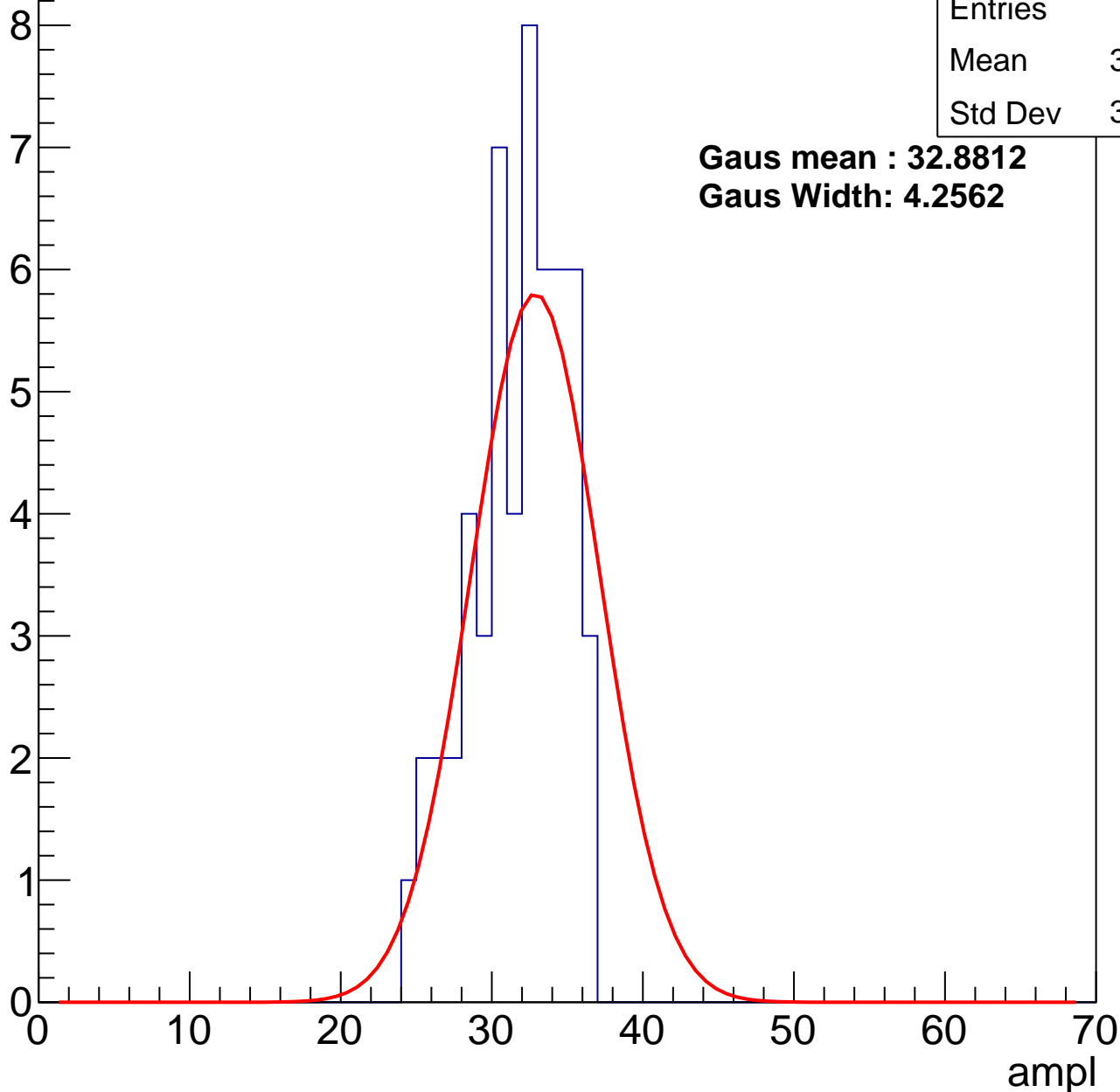
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	31.28
Std Dev	3.076

**Gaus mean : 32.8812**

**Gaus Width: 4.2562**



# B0L001S, U6-ch82, adc1

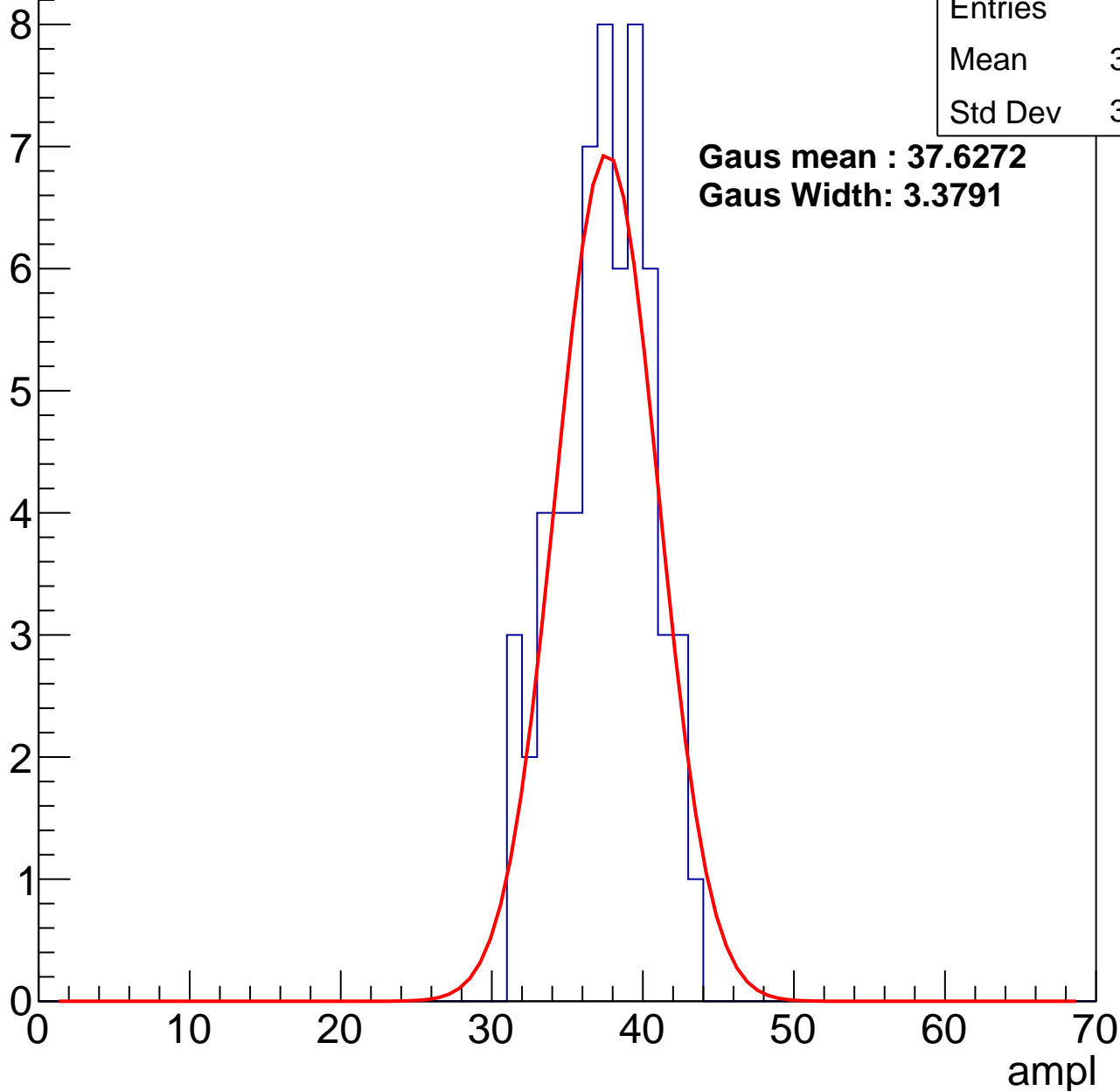
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	37.03
Std Dev	3.003

**Gaus mean : 37.6272**

**Gaus Width: 3.3791**



# B0L001S, U6-ch82, adc2

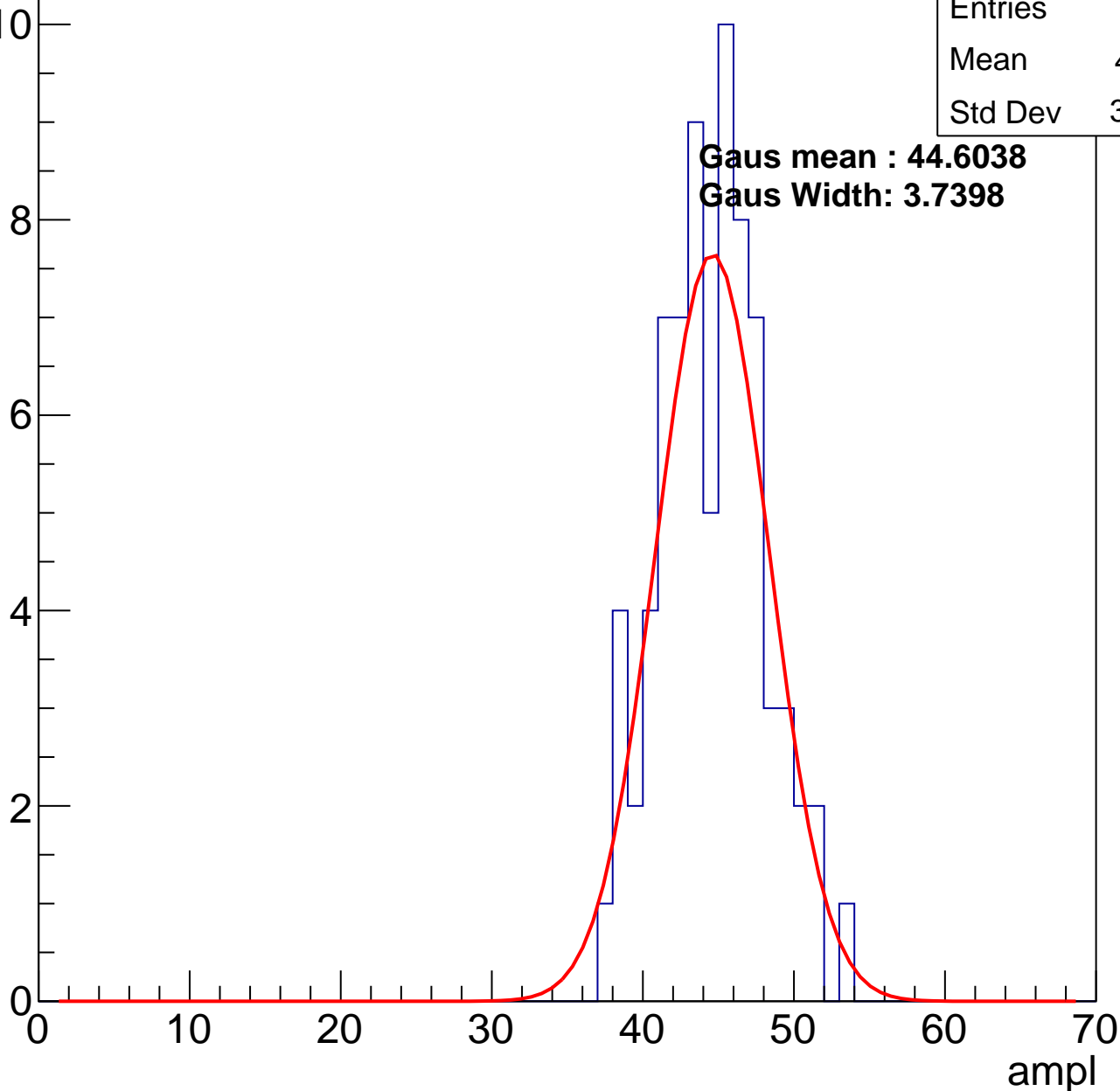
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	44.11
Std Dev	3.435

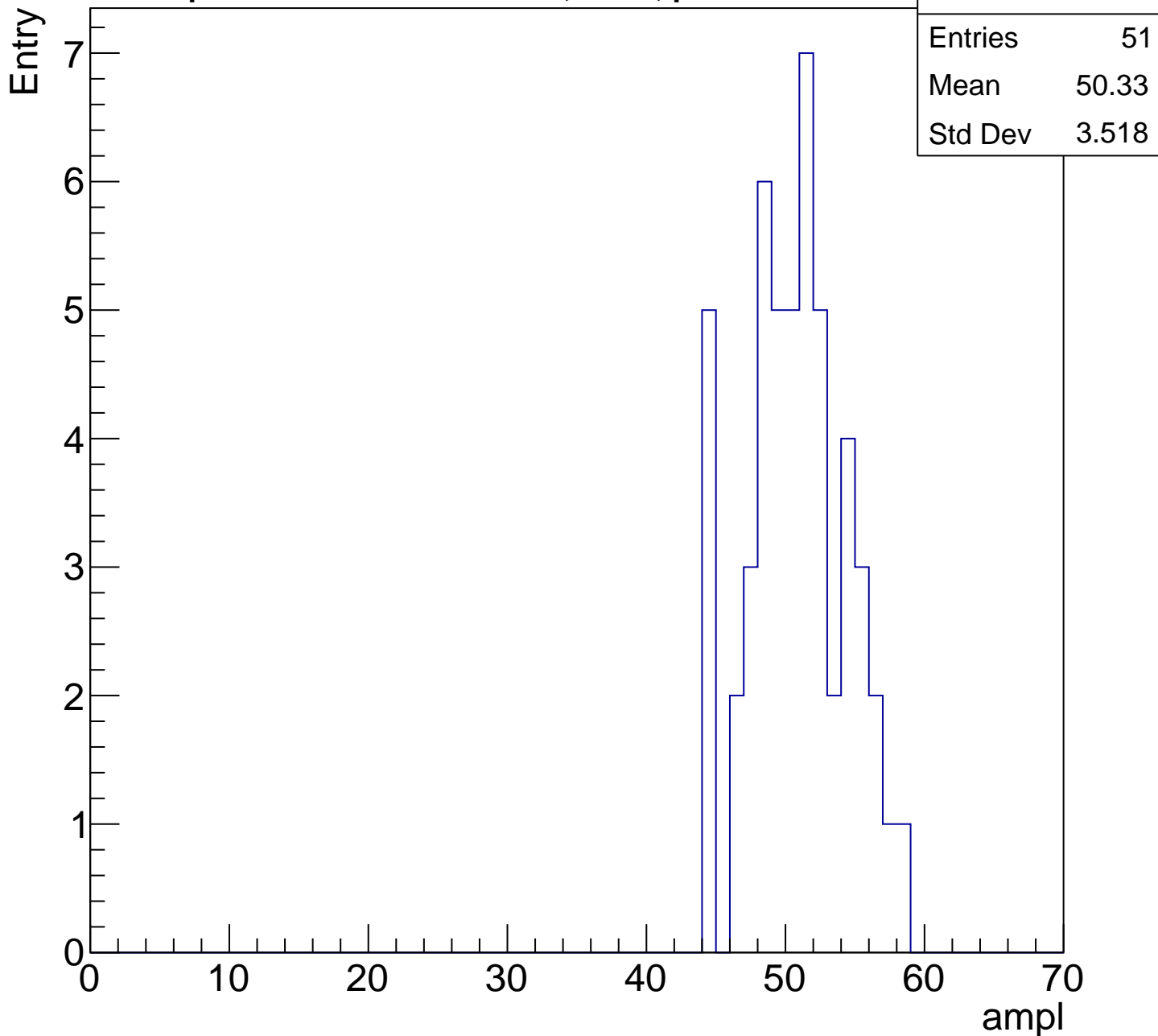
**Gaus mean : 44.6038**

**Gaus Width: 3.7398**



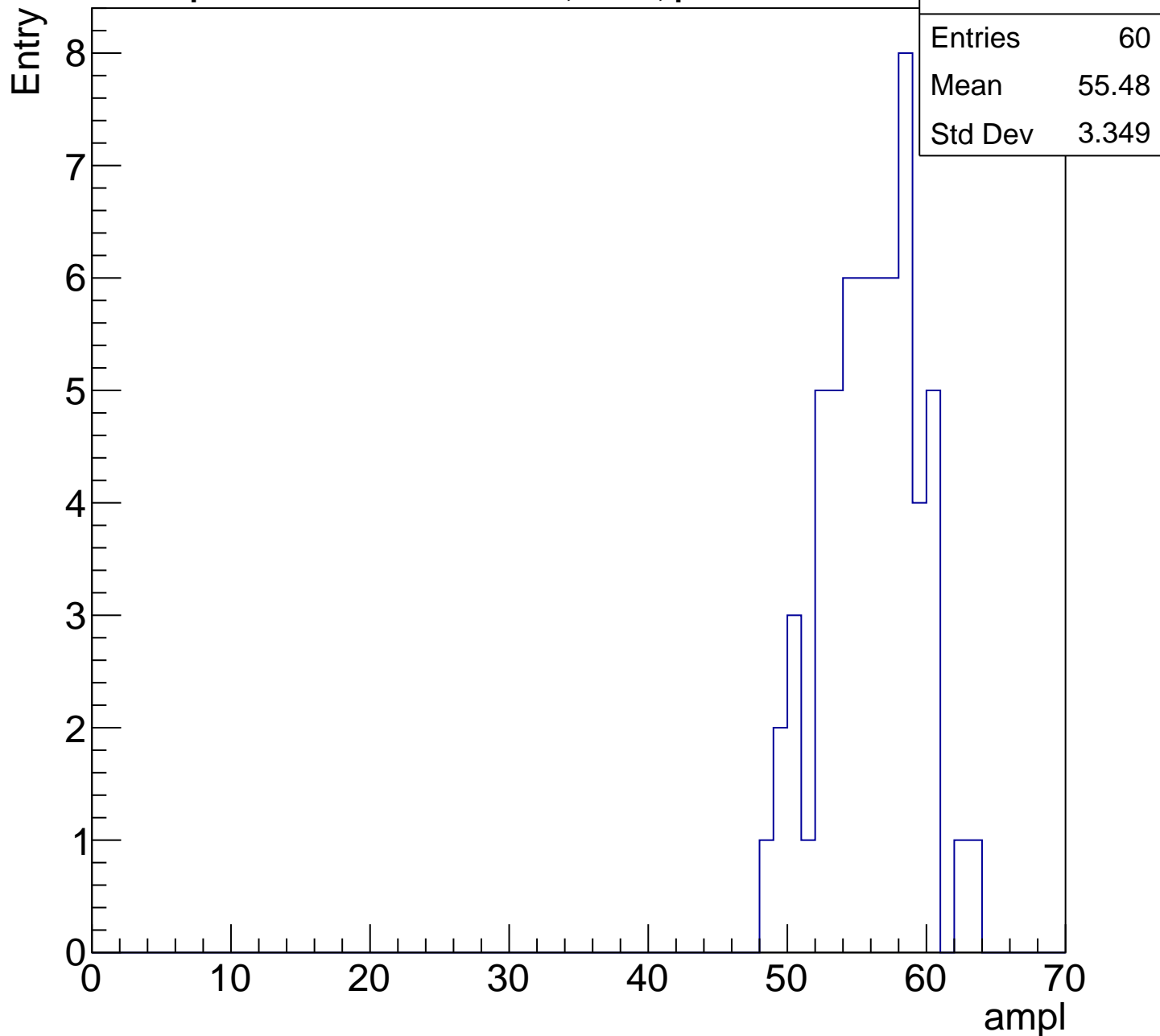
# B0L001S, U6-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U6-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

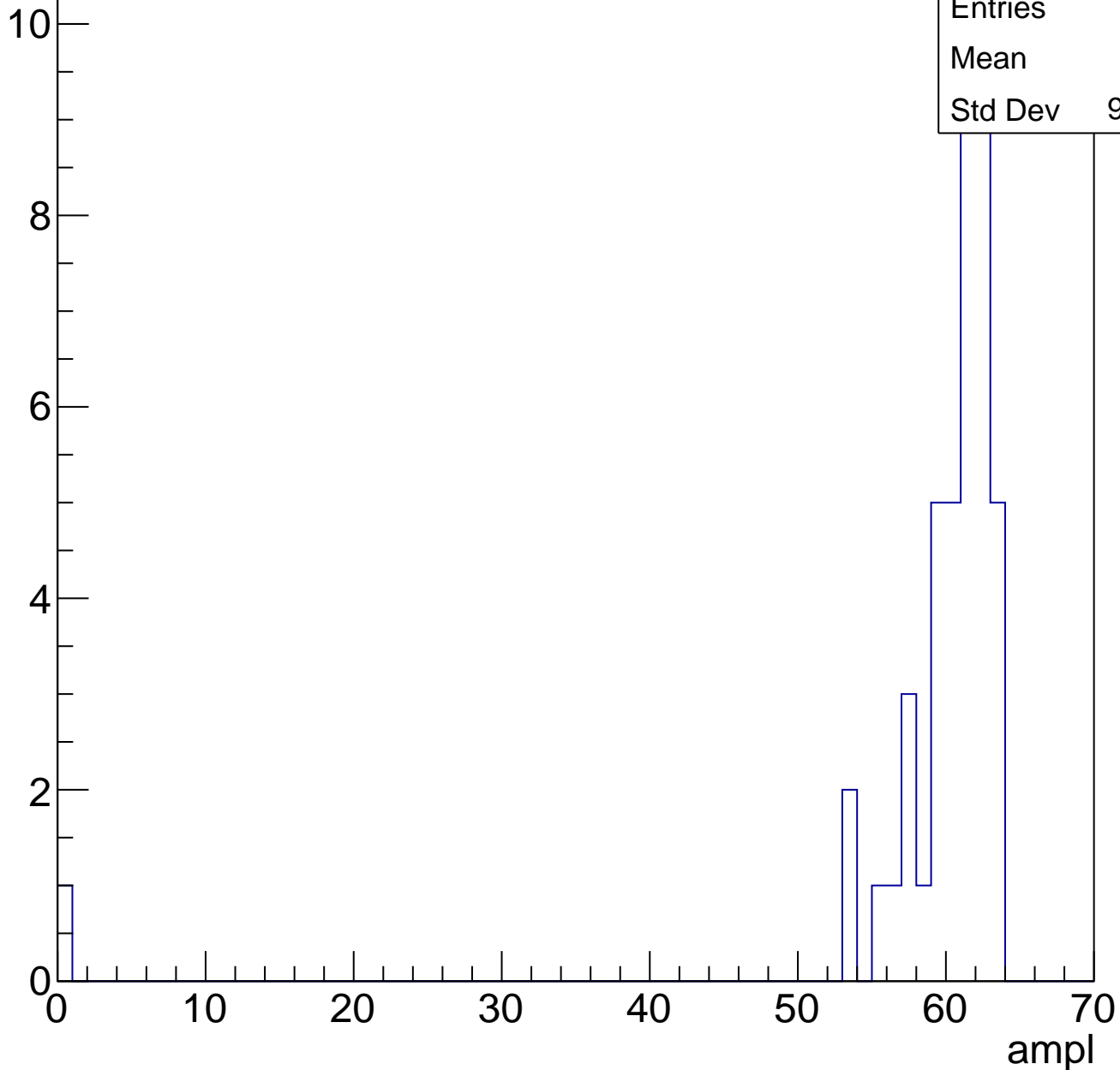


# B0L001S, U6-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	43
Mean	58.7
Std Dev	9.392

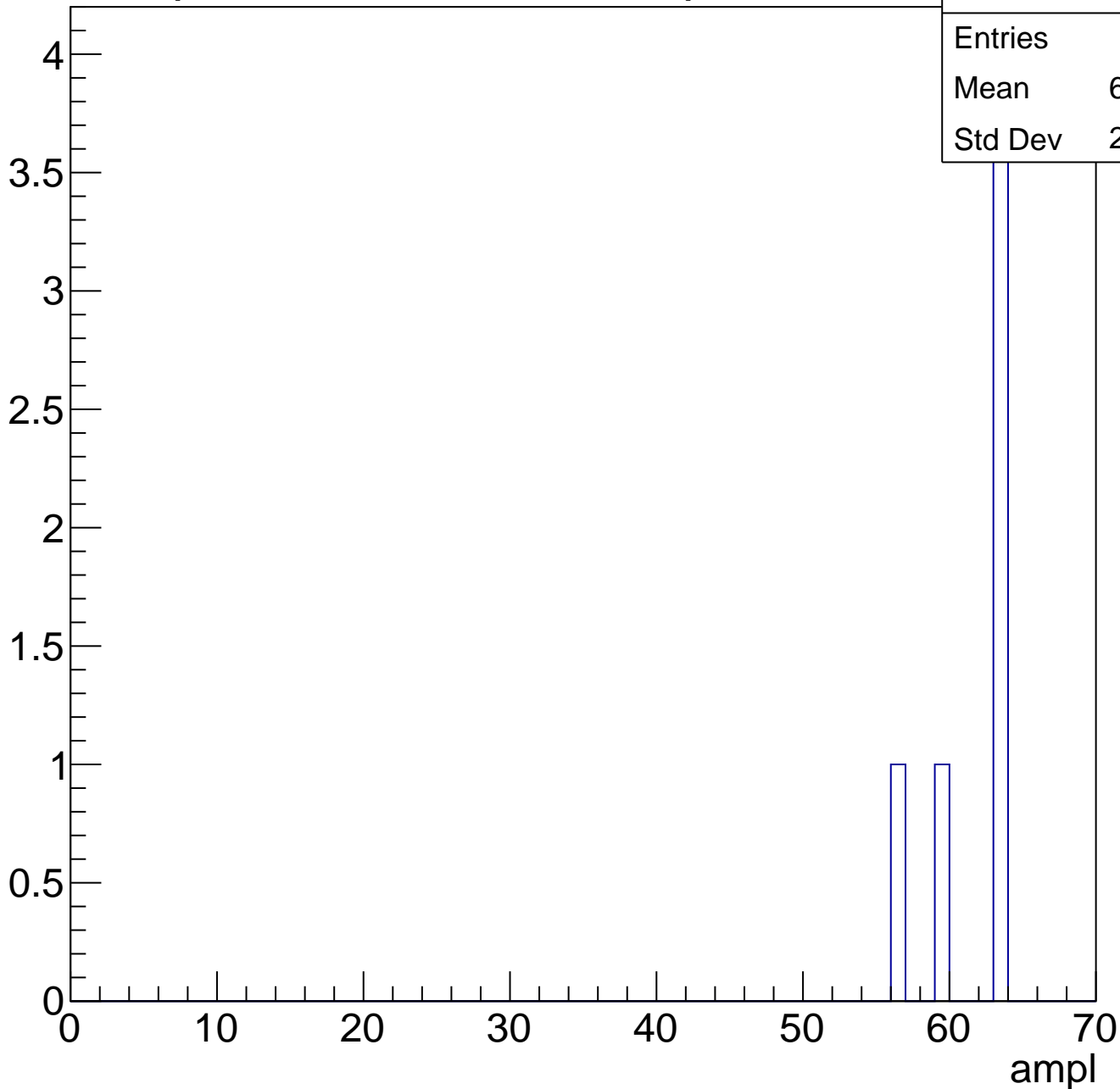
Entry



# B0L001S, U6-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch83, adc0

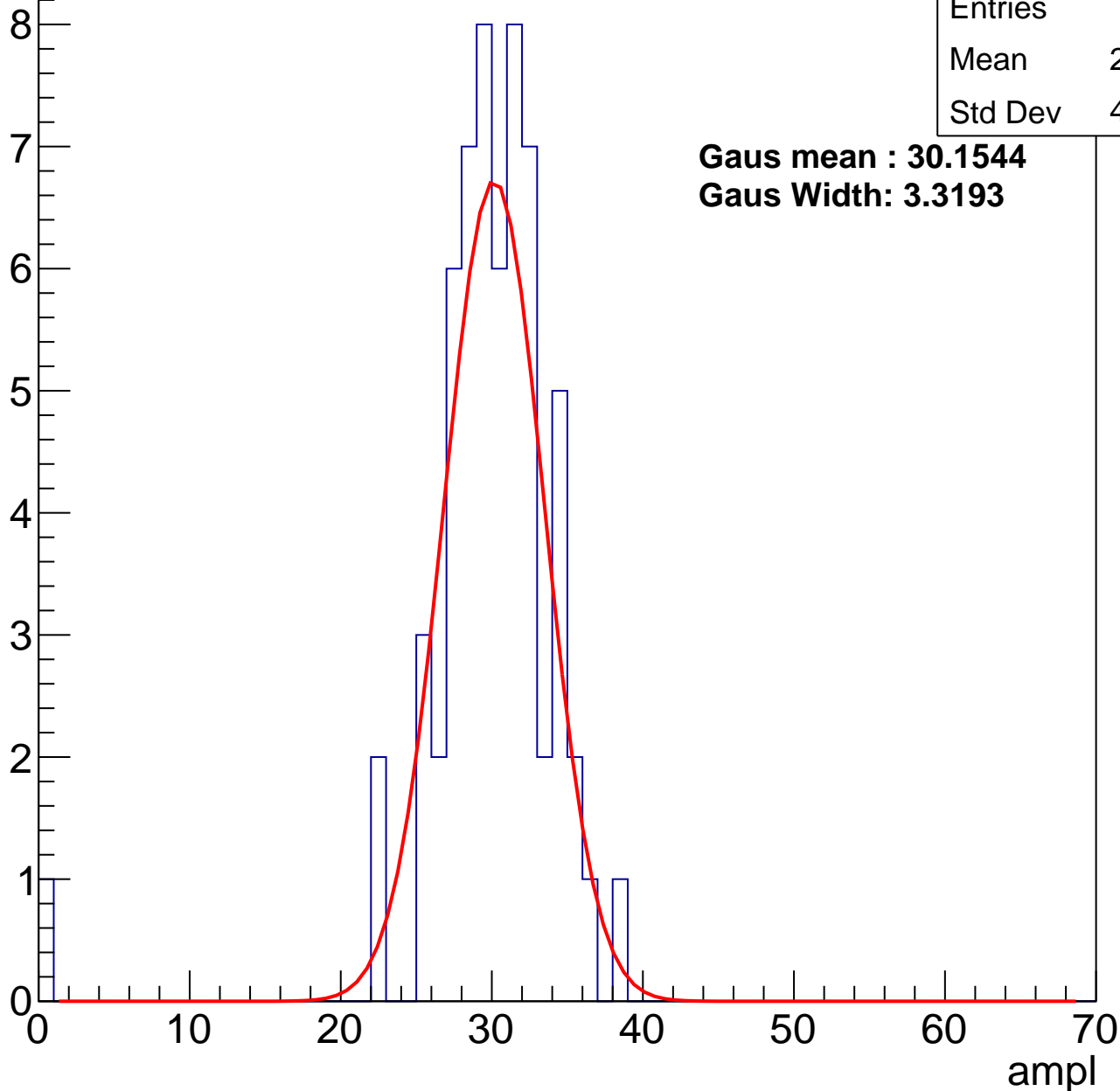
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	29.39
Std Dev	4.937

**Gaus mean : 30.1544**

**Gaus Width: 3.3193**



# B0L001S, U6-ch83, adc1

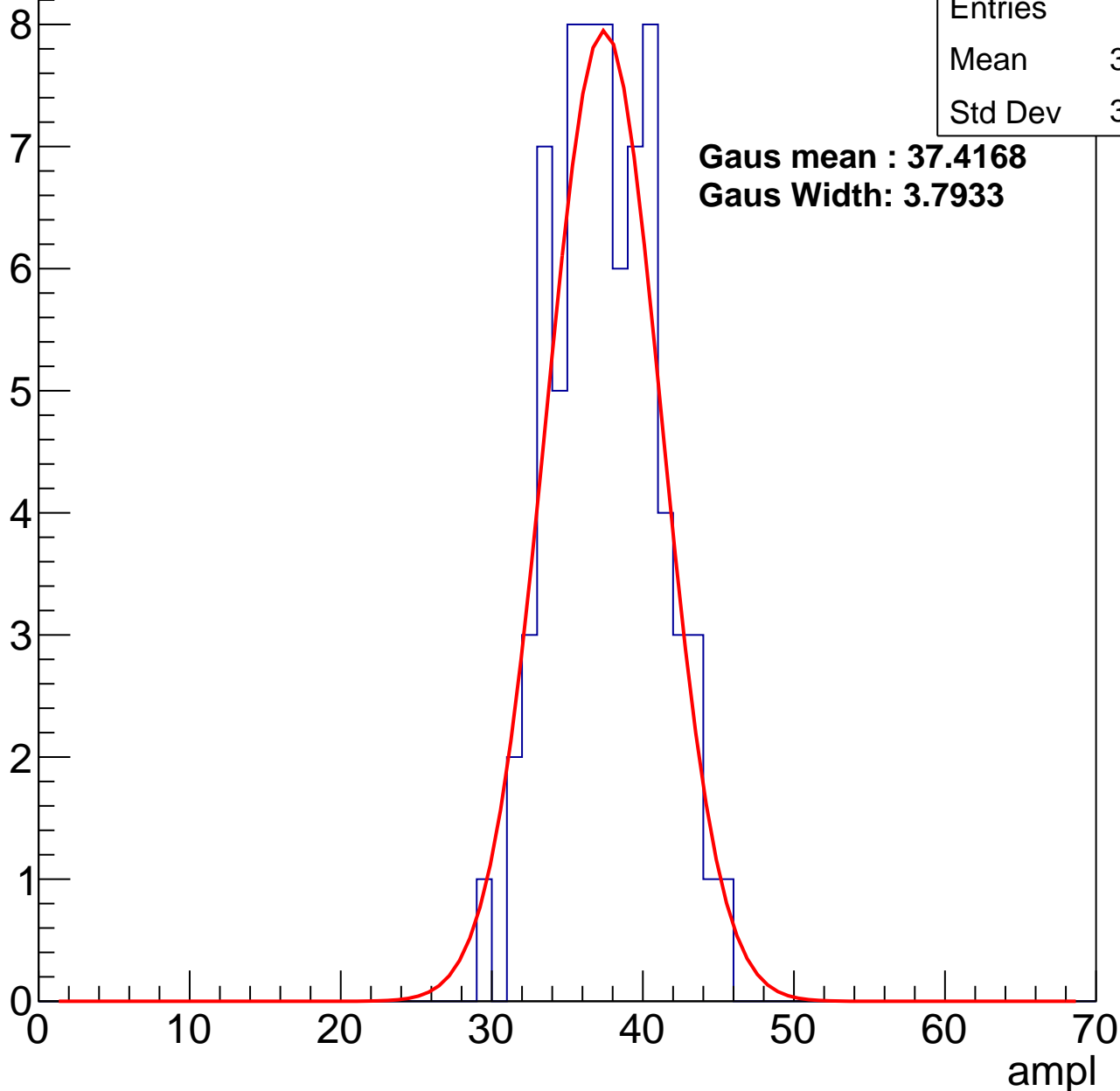
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	37.08
Std Dev	3.413

**Gaus mean : 37.4168**

**Gaus Width: 3.7933**



# B0L001S, U6-ch83, adc2

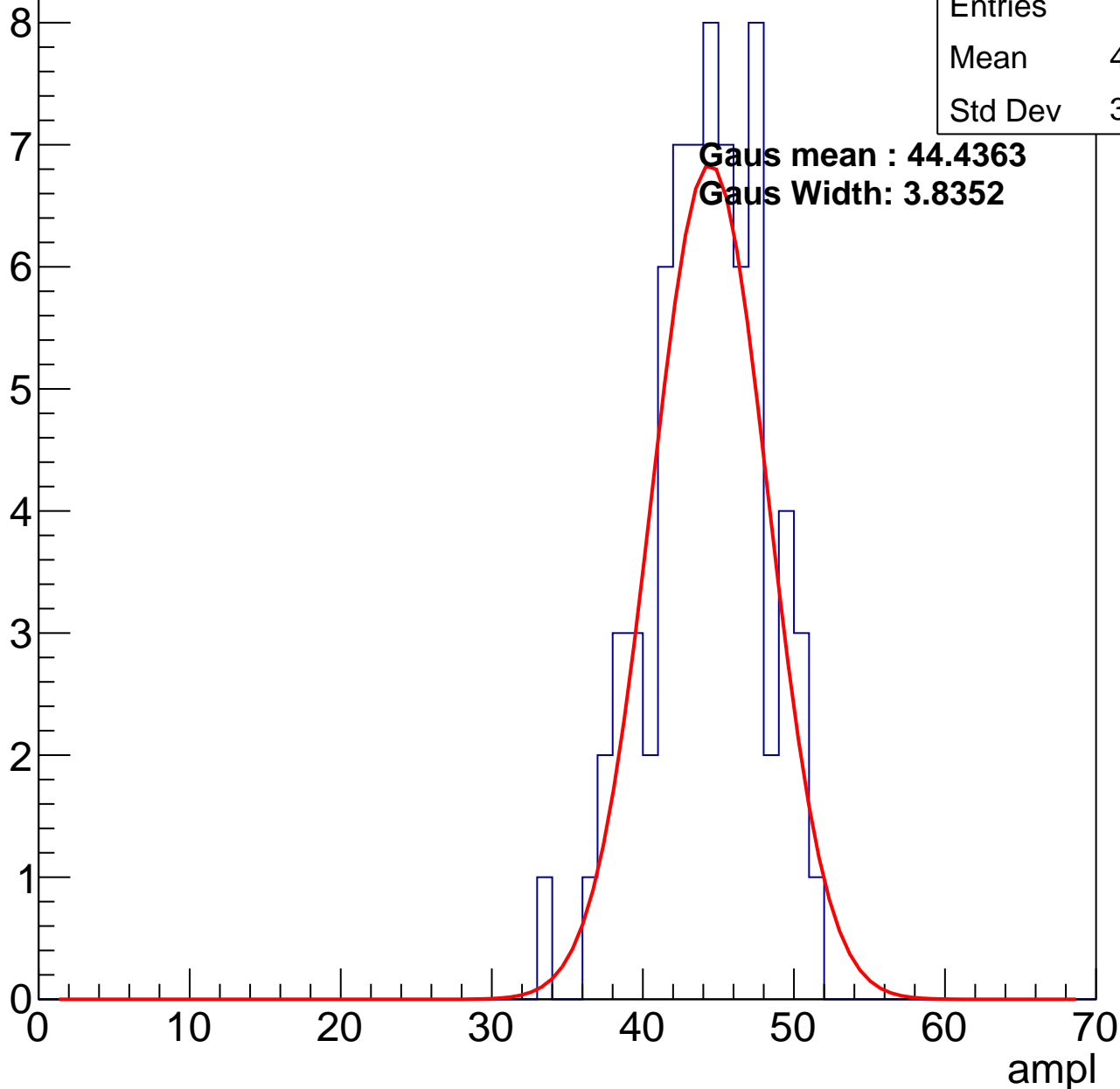
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	43.76
Std Dev	3.706

**Gaus mean : 44.4363**

**Gaus Width: 3.8352**

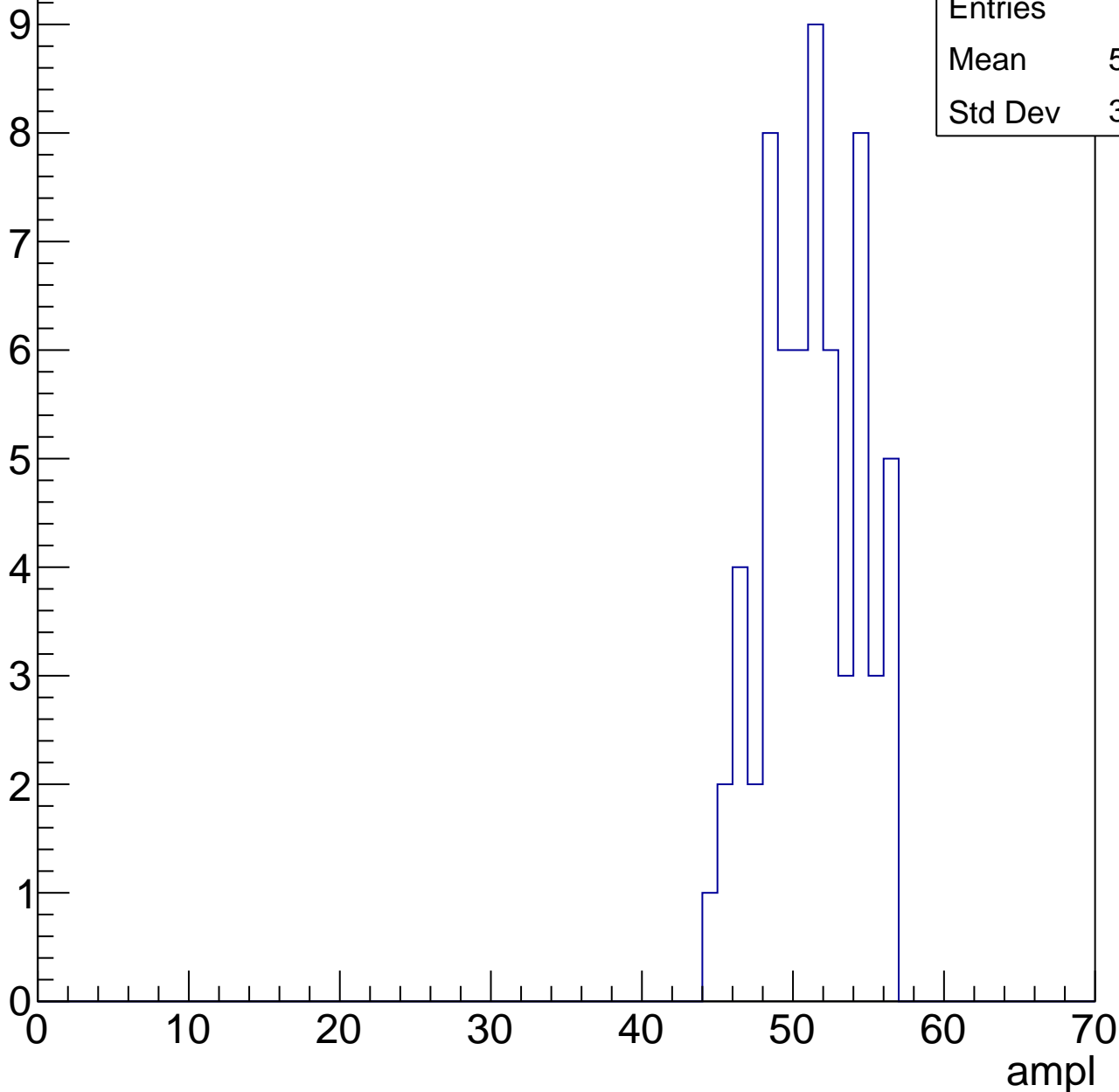


# B0L001S, U6-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	50.75
Std Dev	3.122

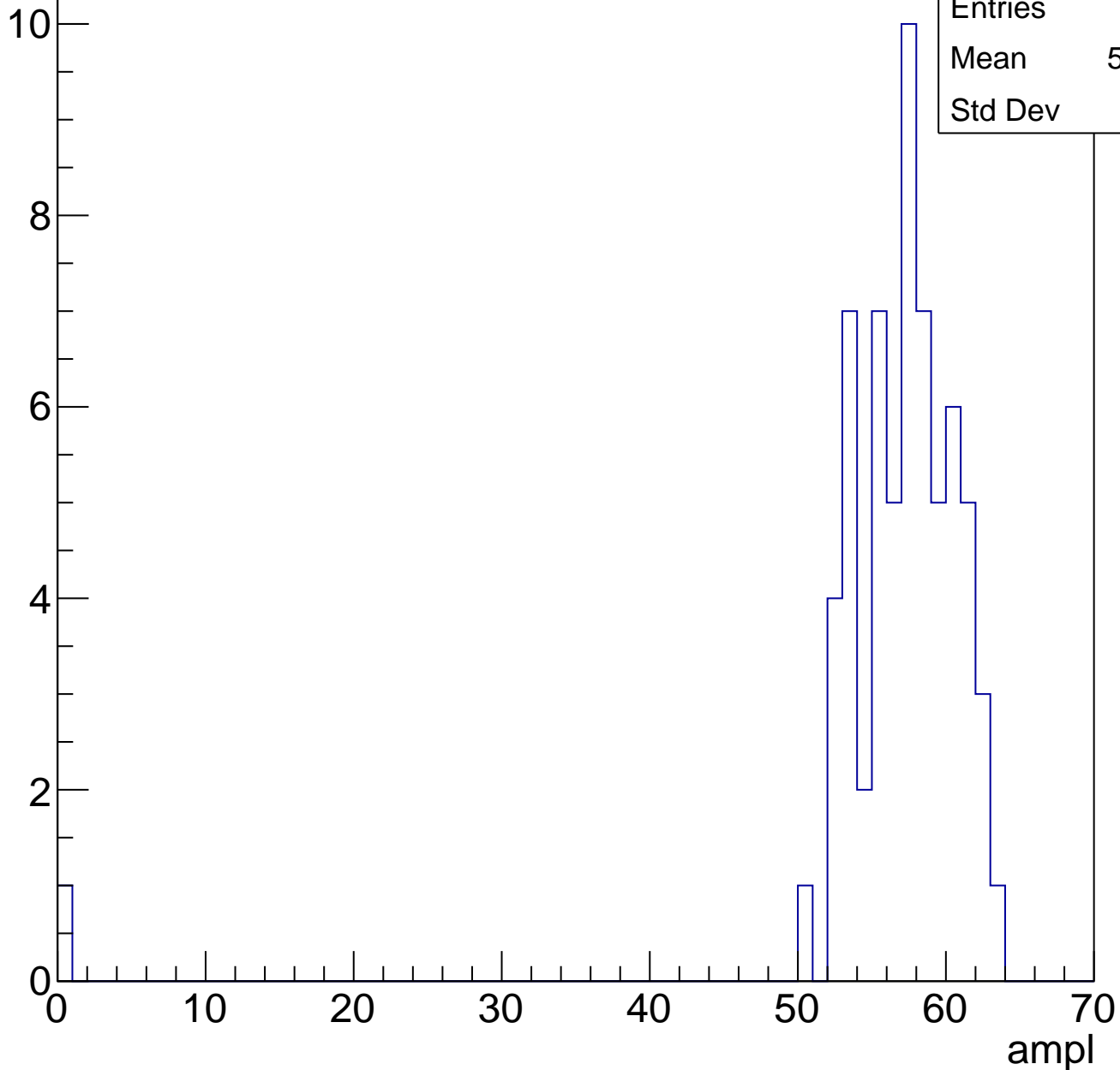


# B0L001S, U6-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	64
Mean	56.05
Std Dev	7.68

Entry



# B0L001S, U6-ch83, adc5

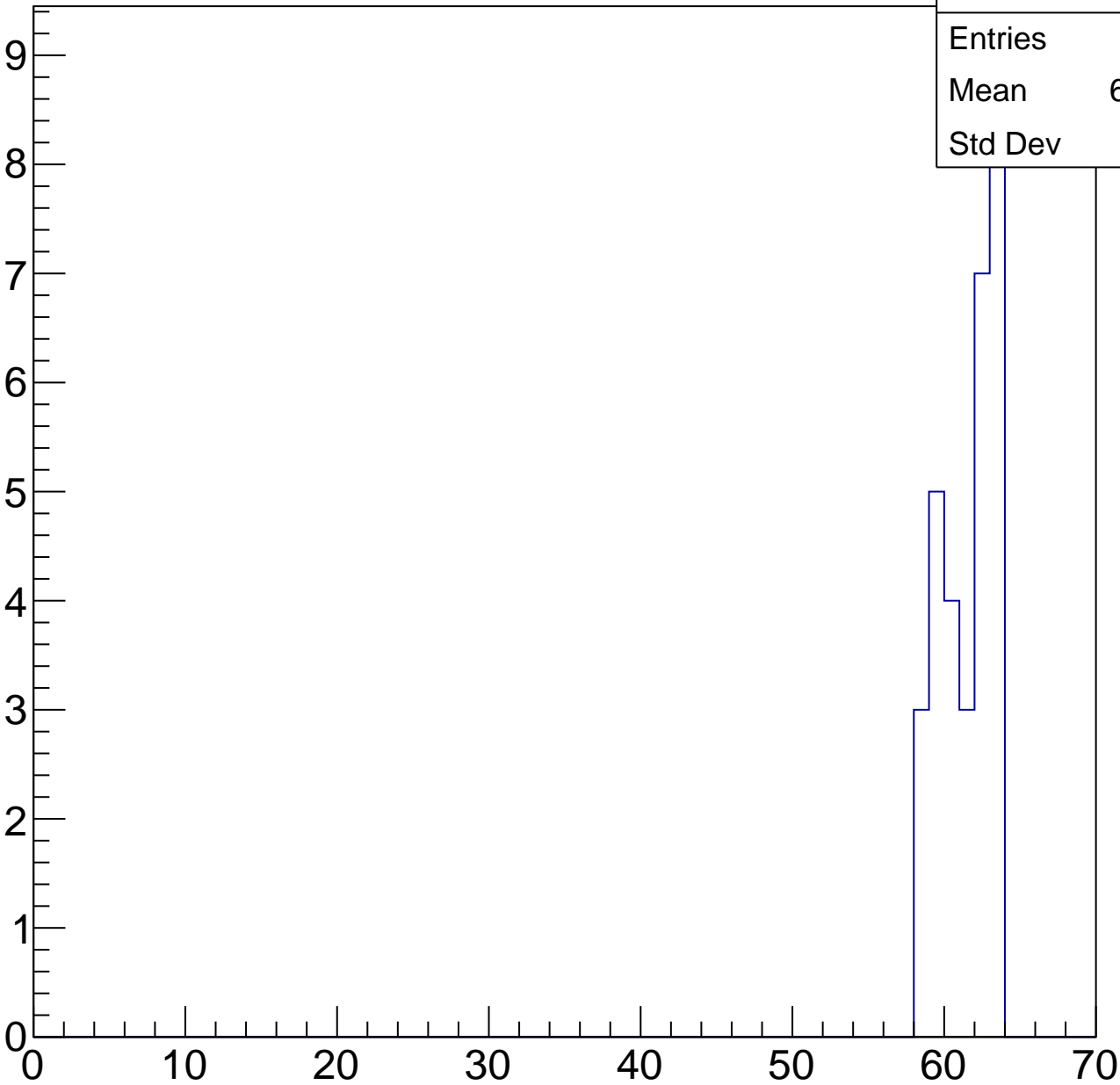
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	31
Mean	61.06
Std Dev	1.74

ampl



# B0L001S, U6-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	61
Std Dev	0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U6-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U6-ch84, adc0

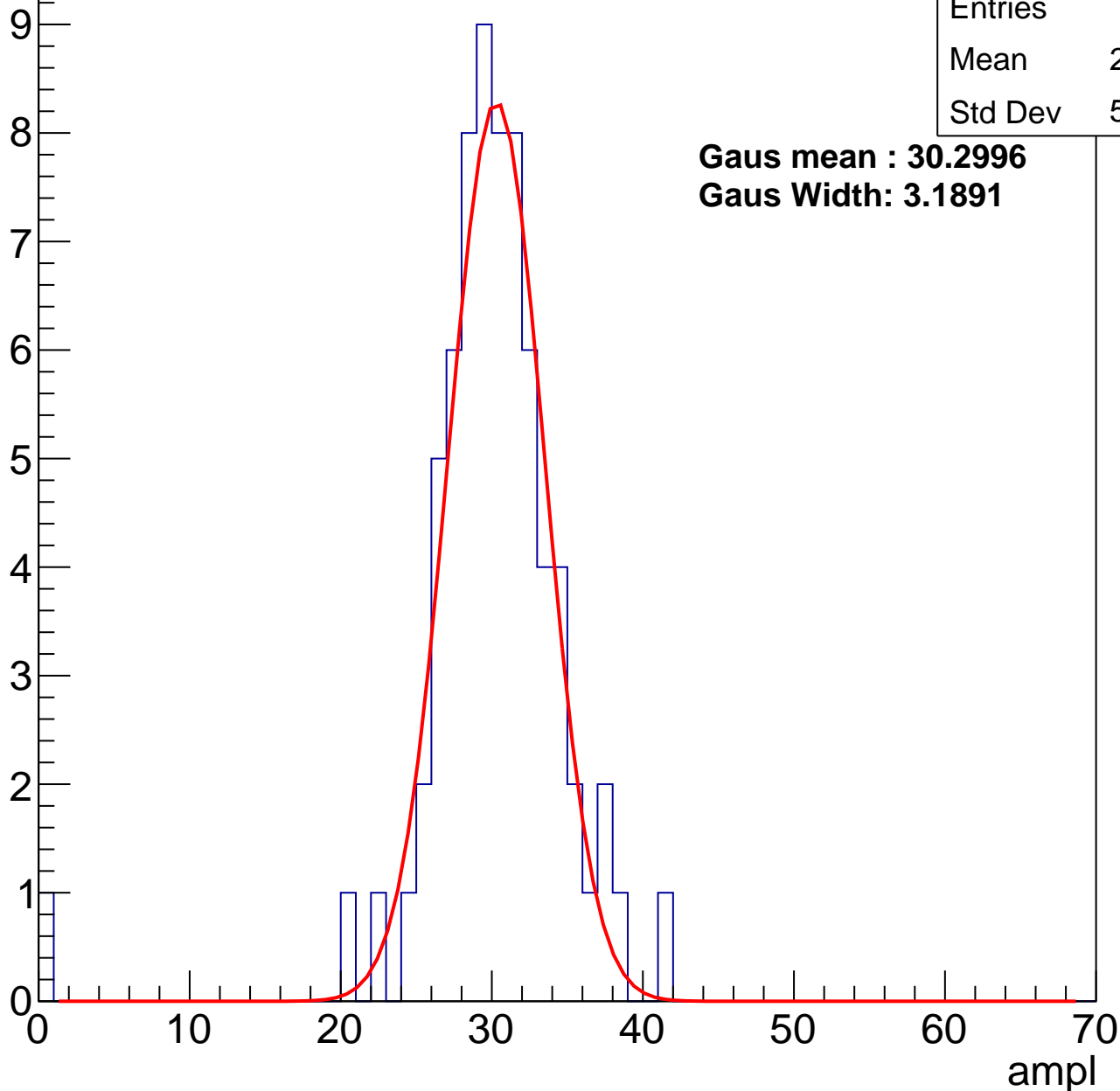
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	29.58
Std Dev	5.054

**Gaus mean : 30.2996**

**Gaus Width: 3.1891**



# B0L001S, U6-ch84, adc1

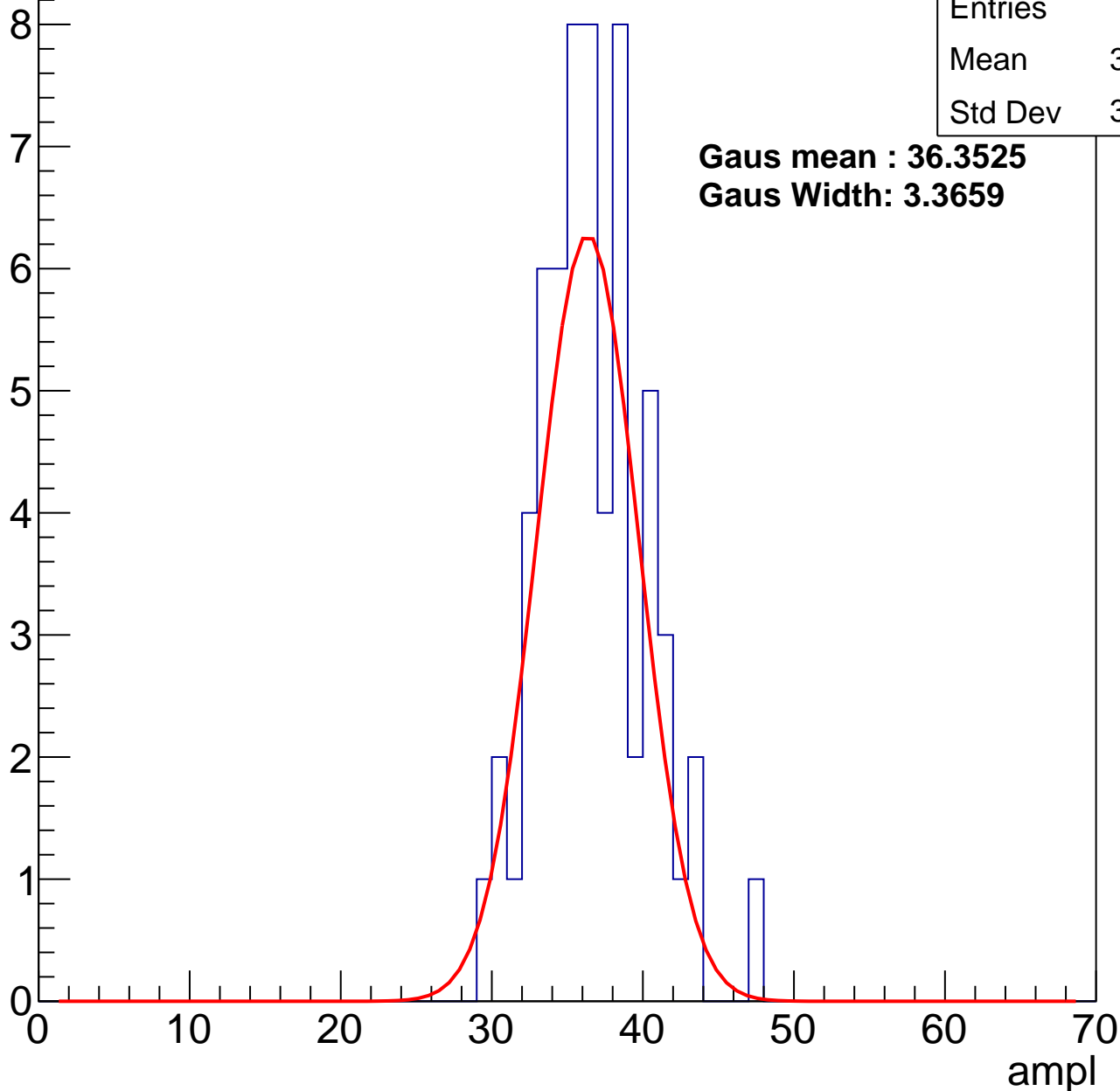
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	36.23
Std Dev	3.494

**Gaus mean : 36.3525**

**Gaus Width: 3.3659**



# B0L001S, U6-ch84, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	42.88
Std Dev	3.598

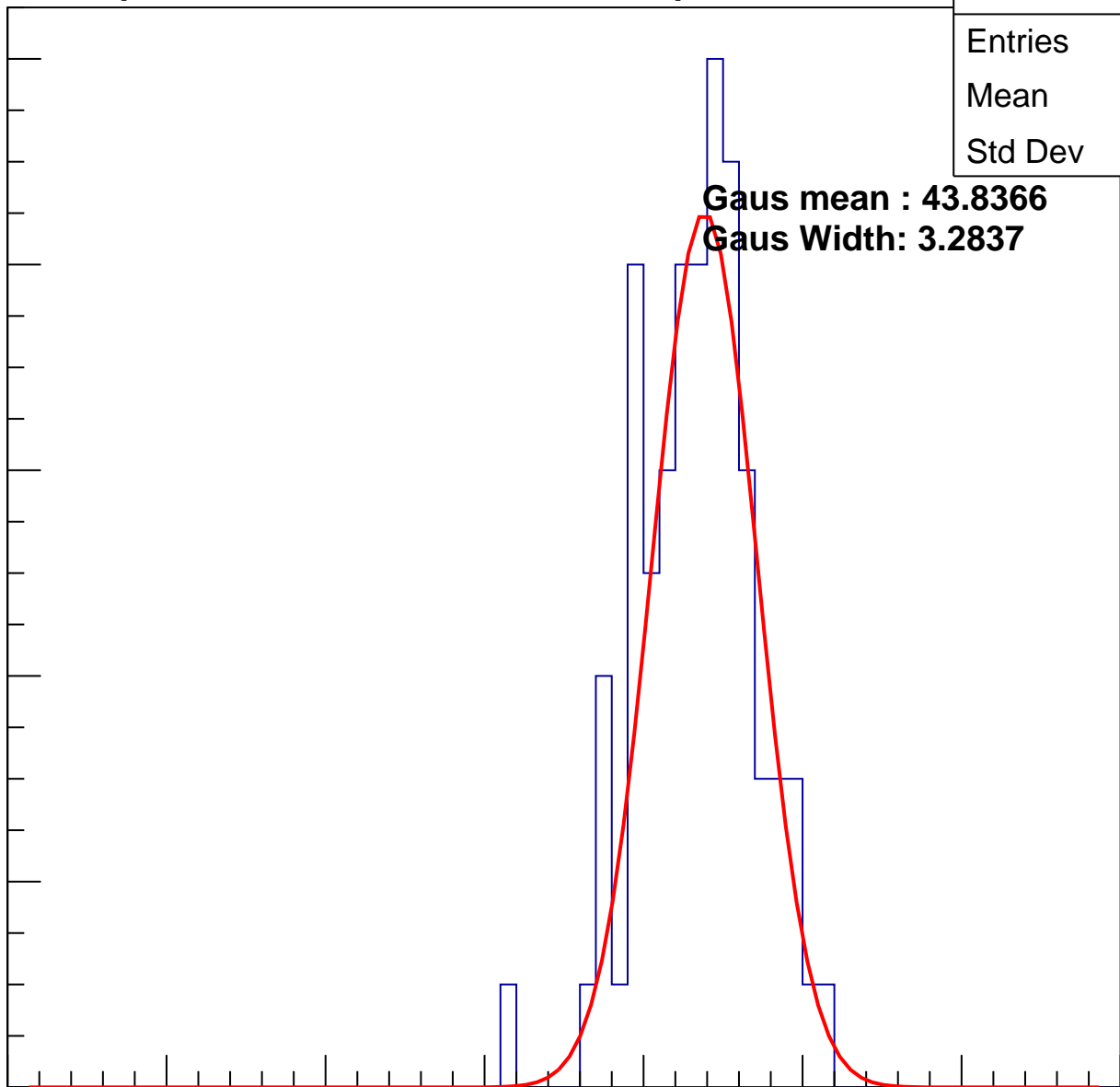
**Gaus mean : 43.8366**

**Gaus Width: 3.2837**

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

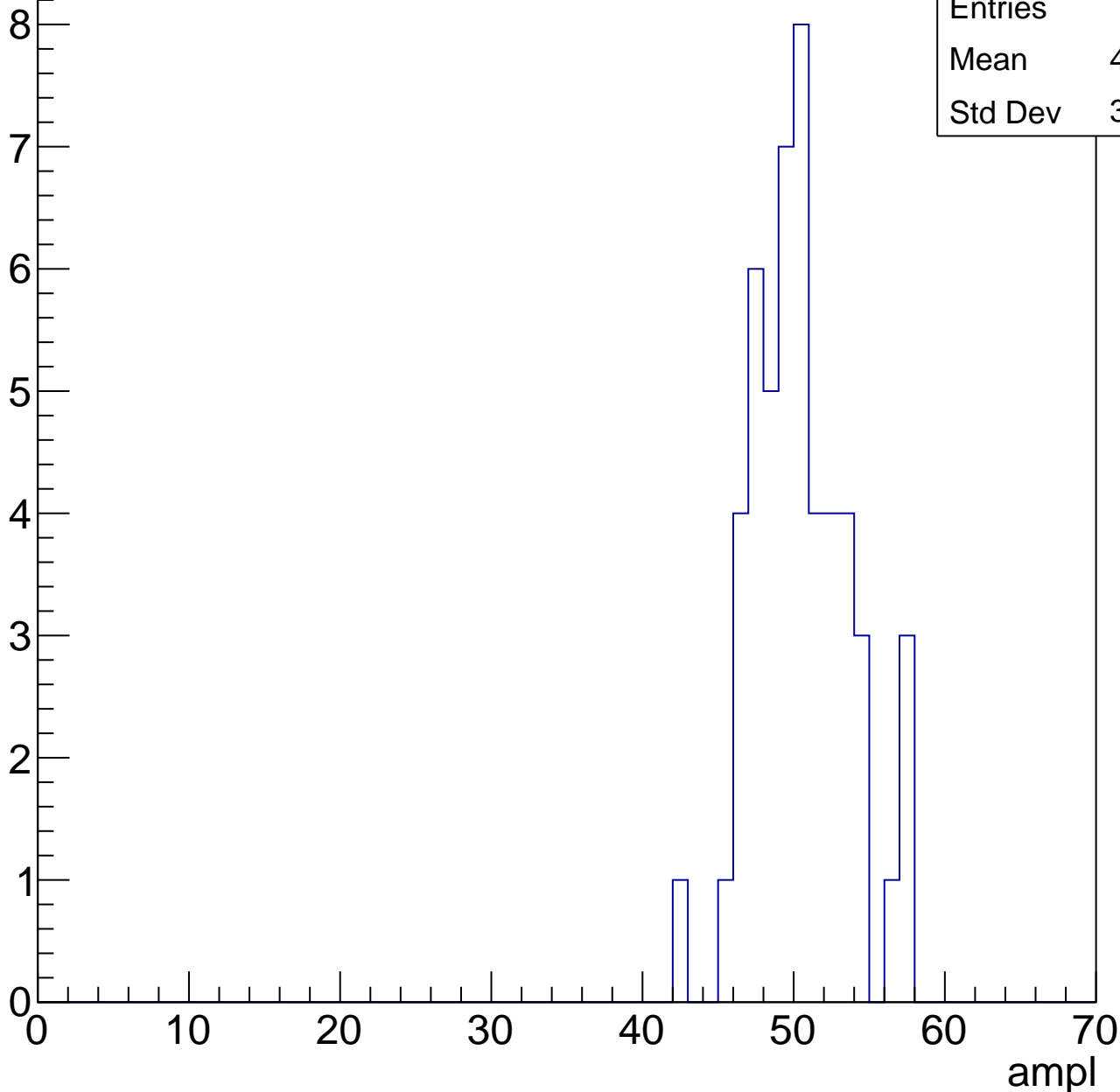


# B0L001S, U6-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	49.98
Std Dev	3.196

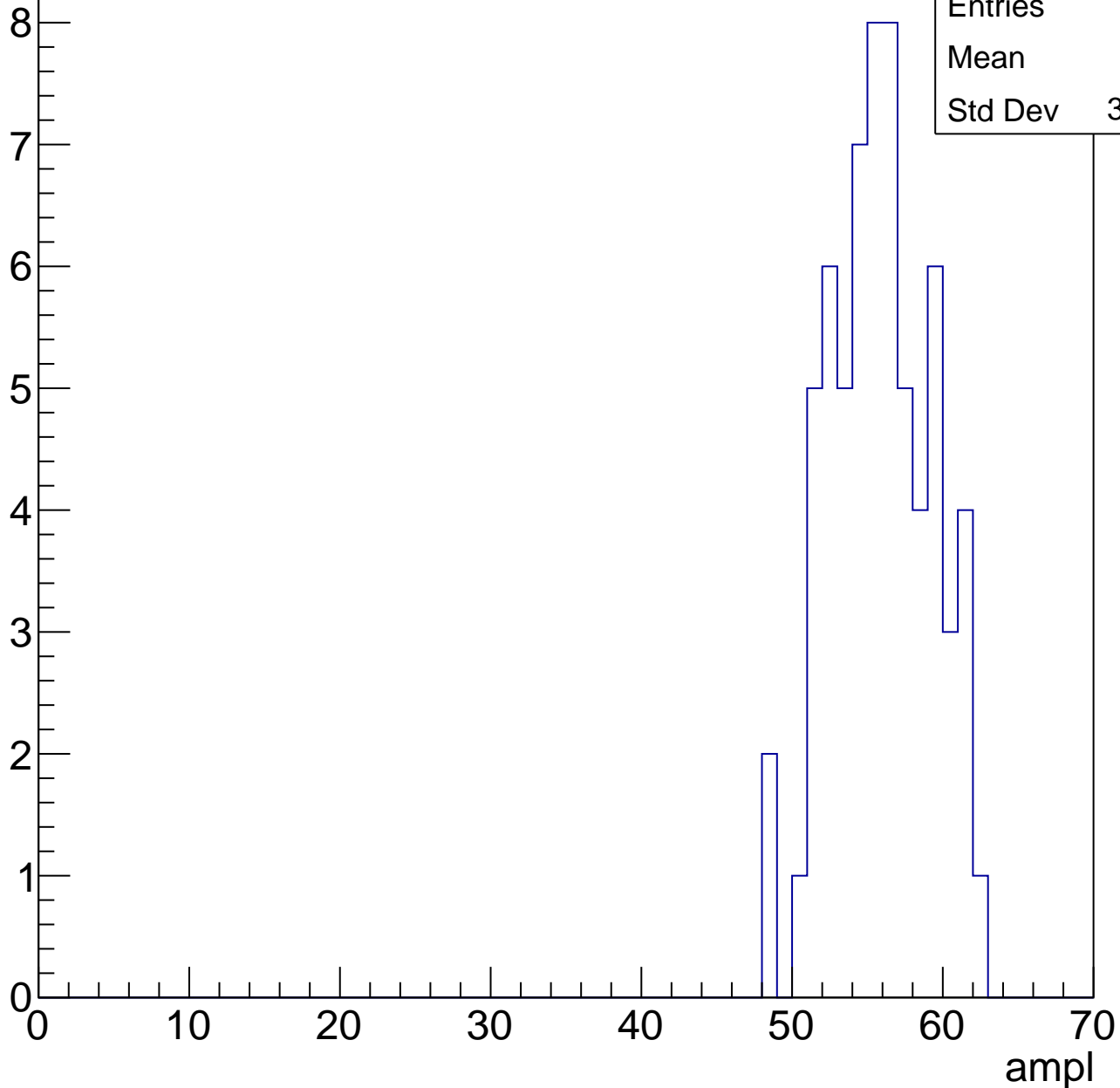


# B0L001S, U6-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	55.4
Std Dev	3.285

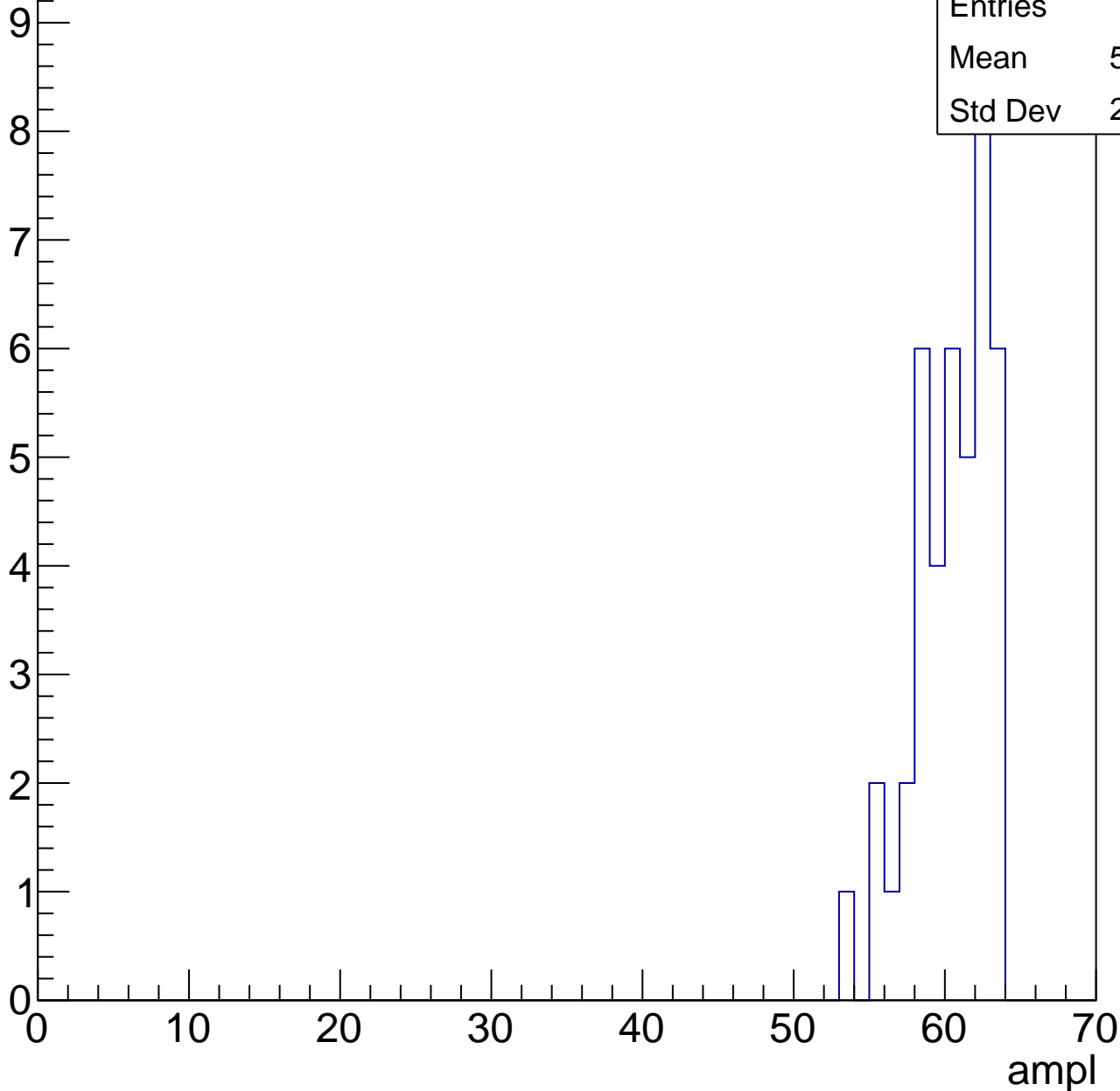


# B0L001S, U6-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

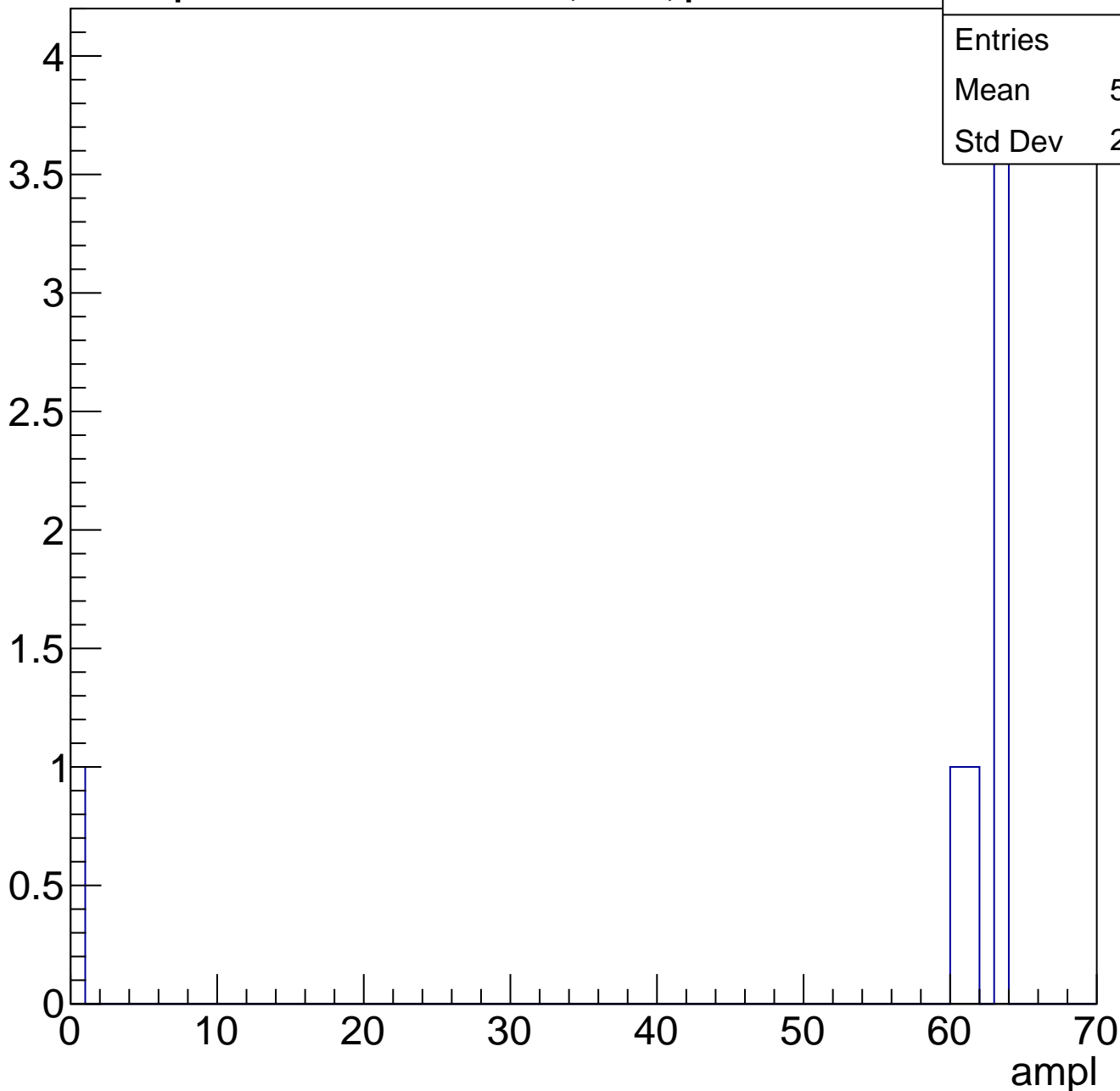
Entries	42
Mean	59.95
Std Dev	2.468



# B0L001S, U6-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U6-ch85, adc0

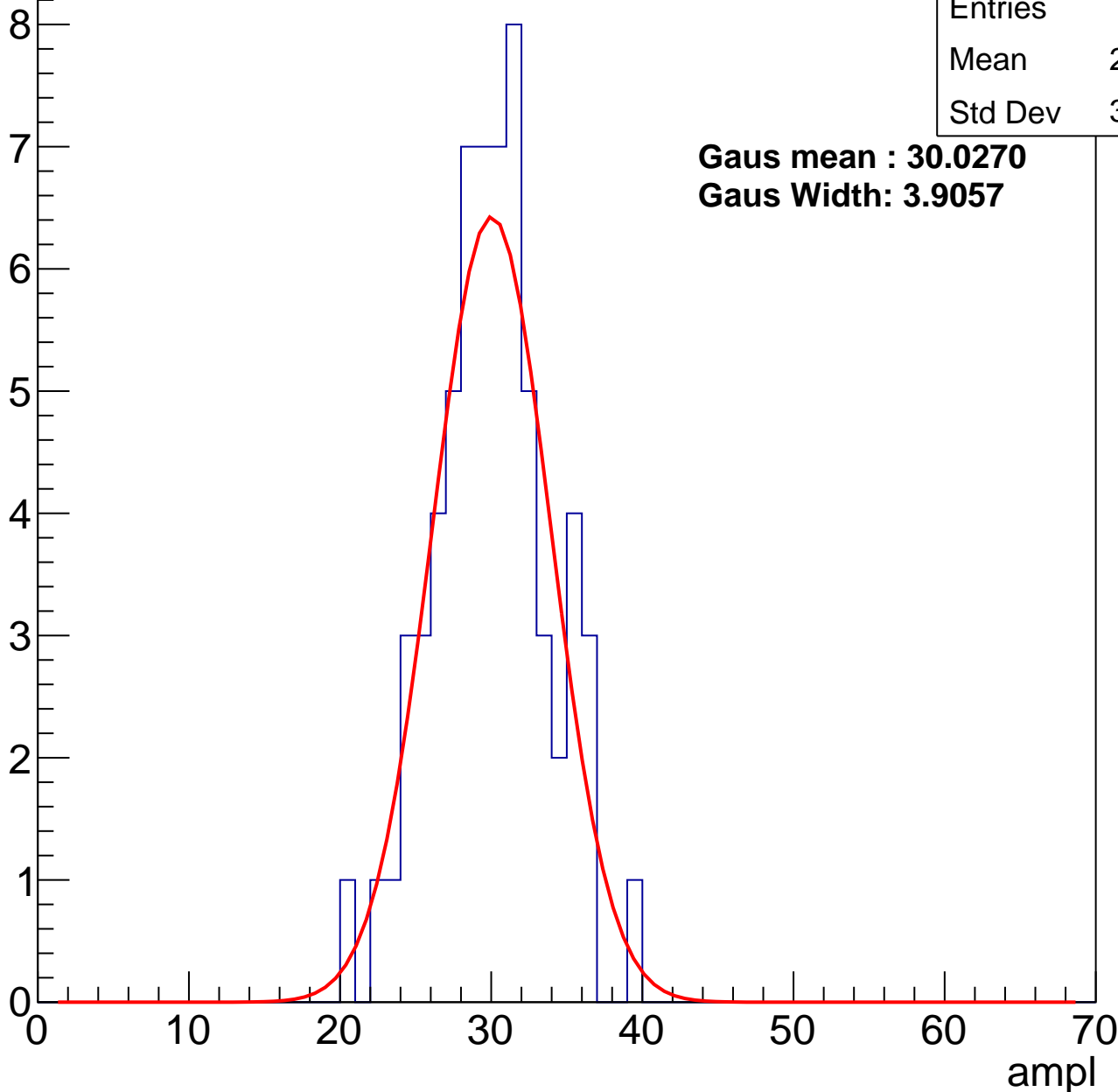
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	29.57
Std Dev	3.729

**Gaus mean : 30.0270**

**Gaus Width: 3.9057**



# B0L001S, U6-ch85, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	75
Mean	36.25
Std Dev	3.703

**Gaus mean : 36.5972**

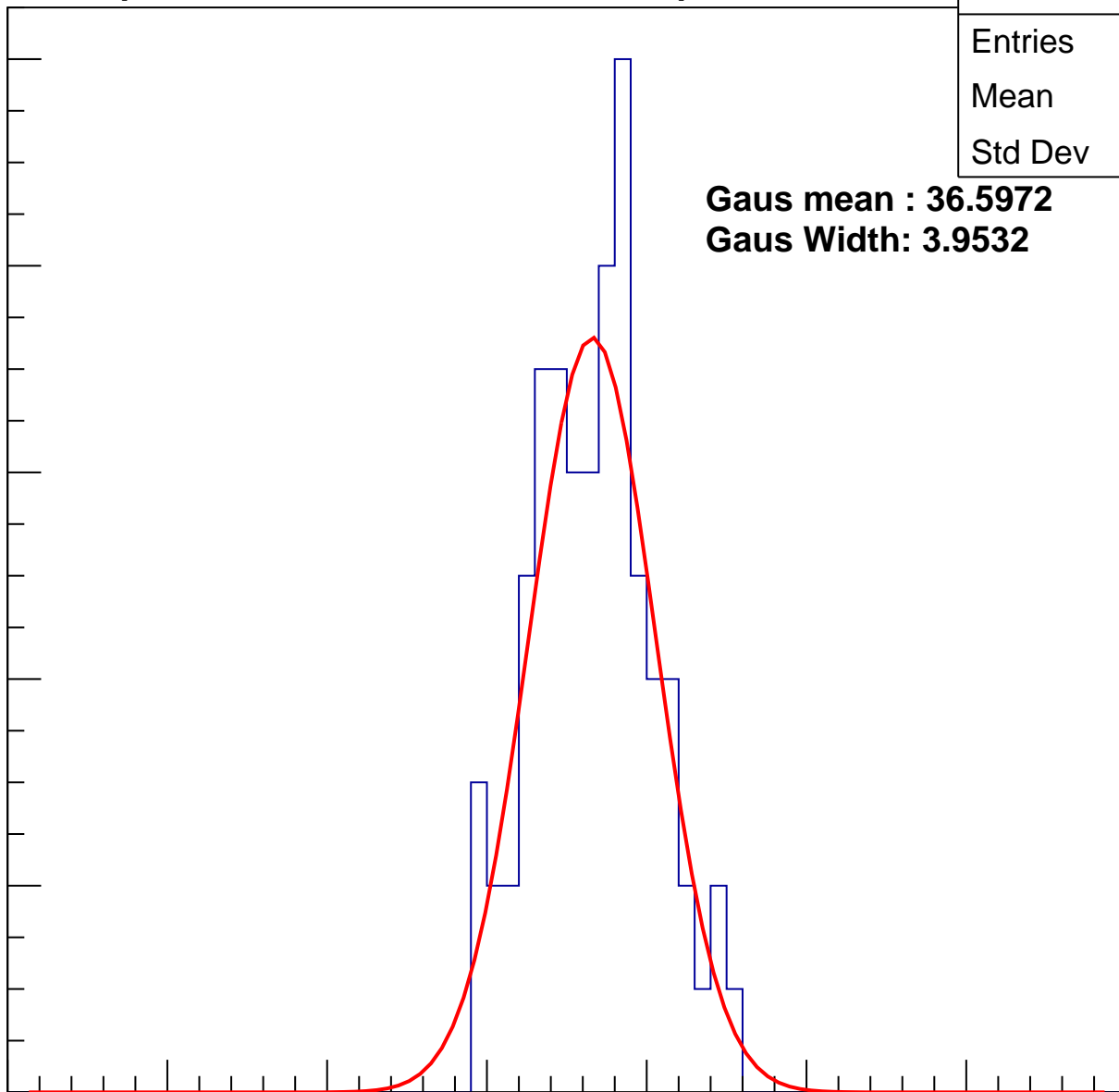
**Gaus Width: 3.9532**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U6-ch85, adc2

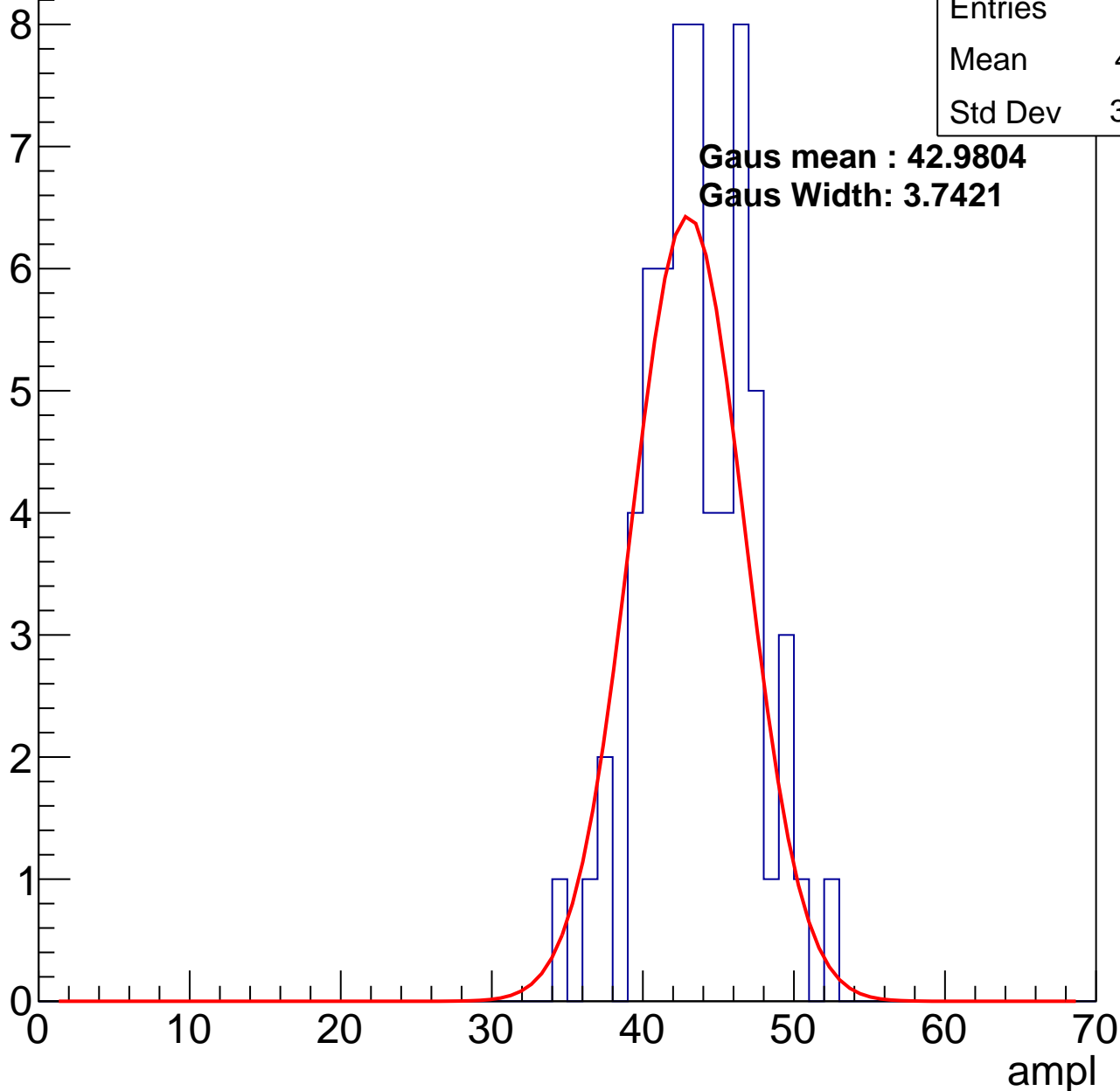
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	43.21
Std Dev	3.528

**Gaus mean : 42.9804**

**Gaus Width: 3.7421**

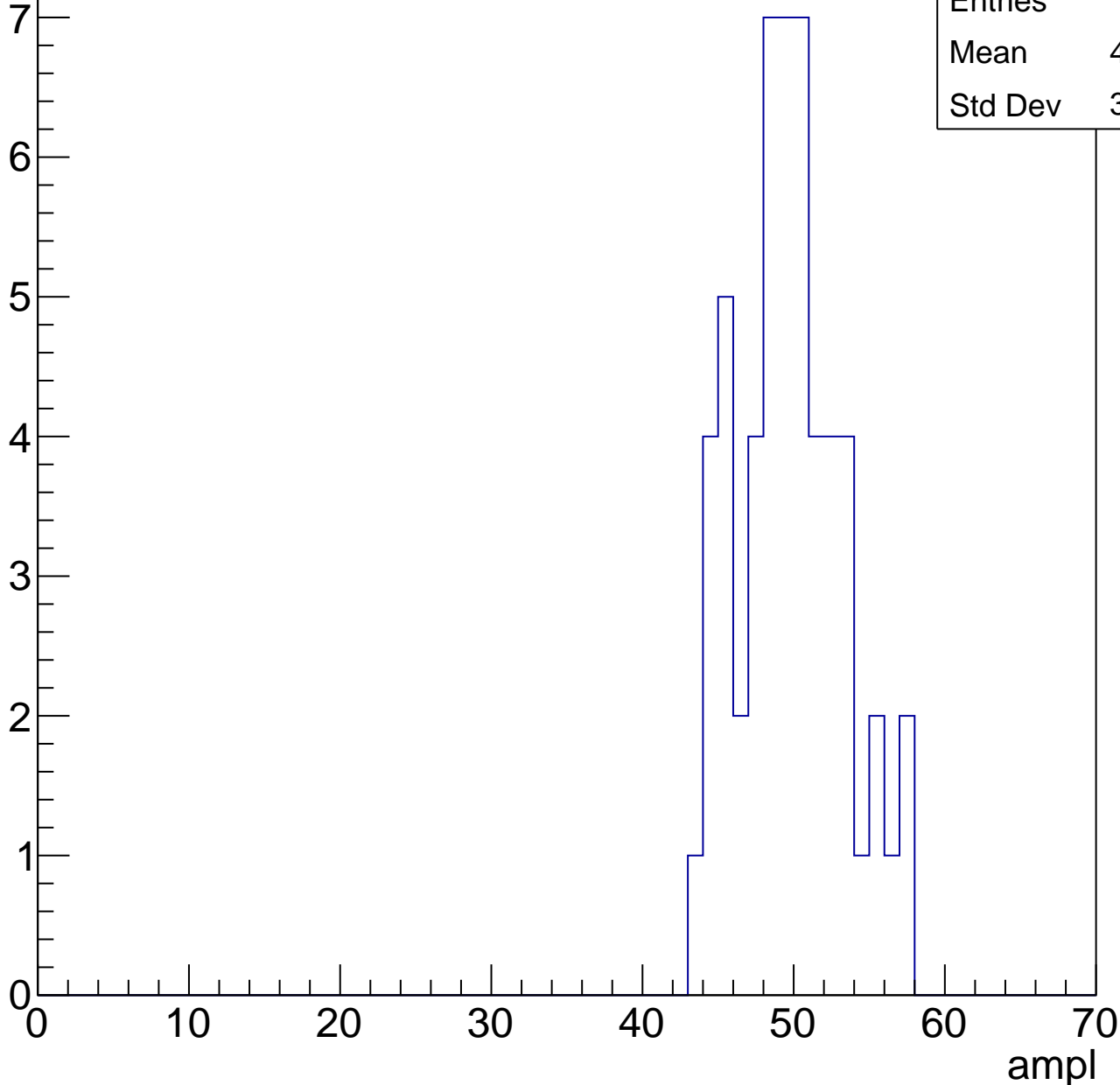


# B0L001S, U6-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	49.29
Std Dev	3.436

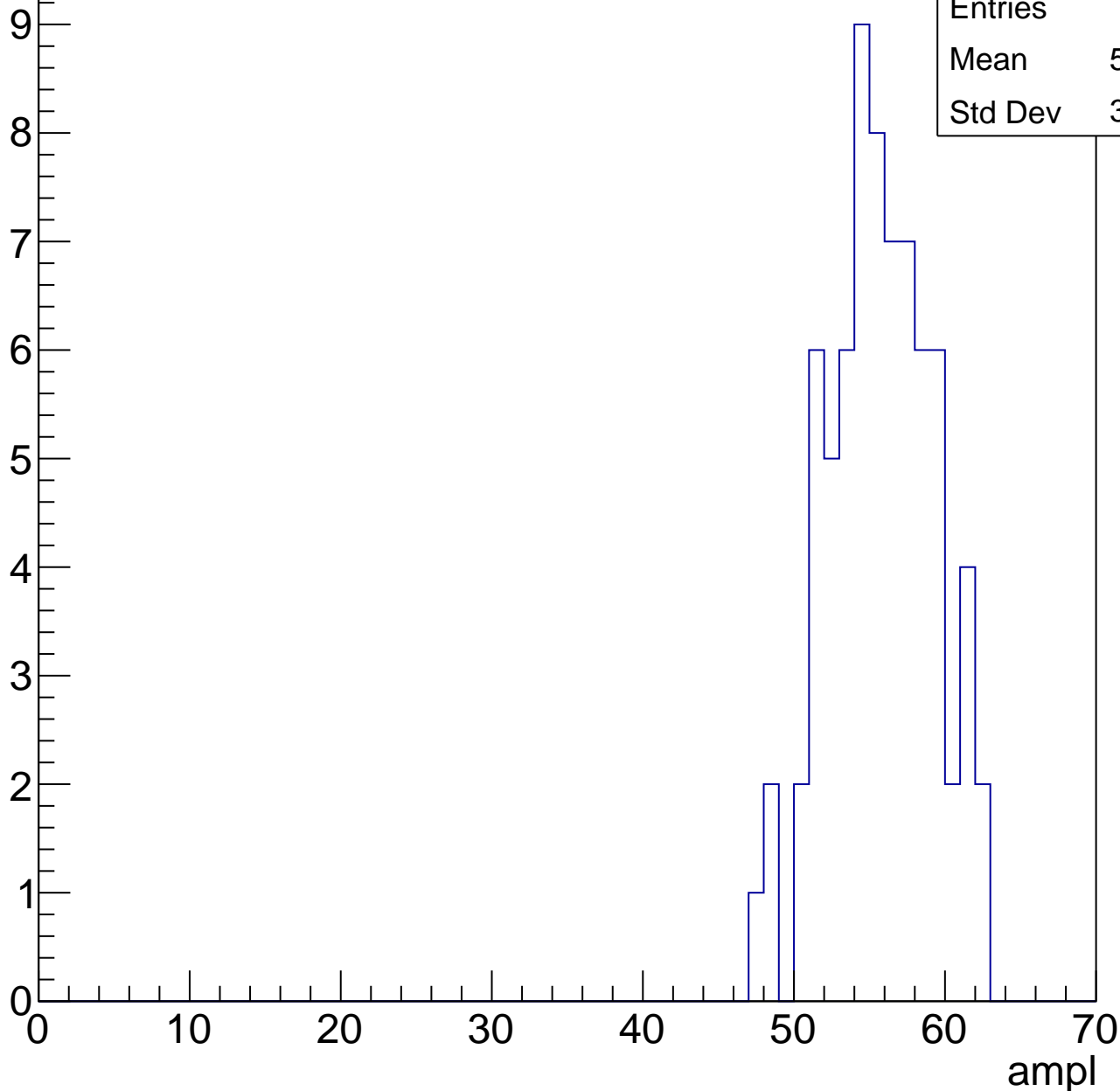


# B0L001S, U6-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

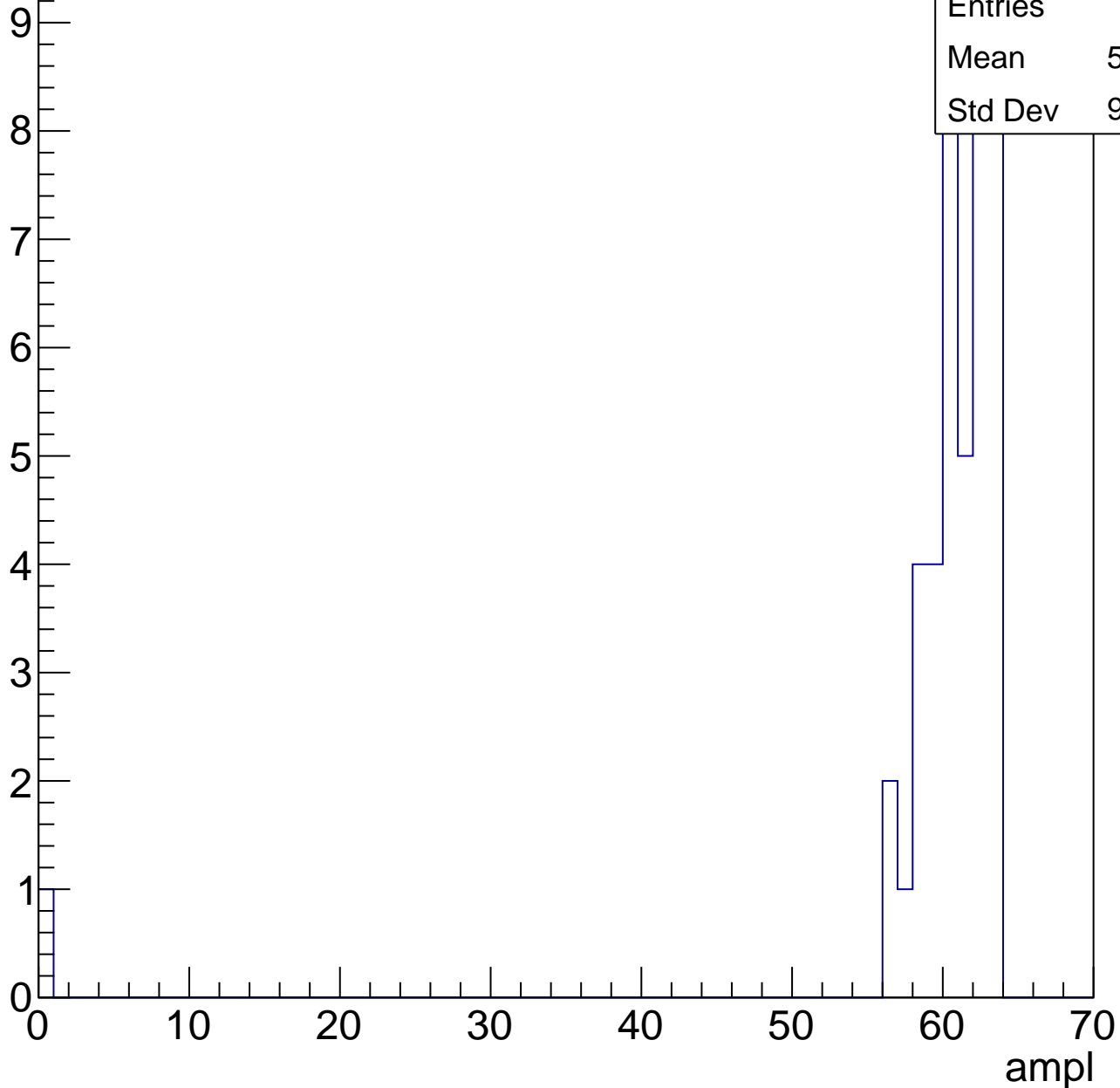
Entries	73
Mean	55.26
Std Dev	3.428



# B0L001S, U6-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

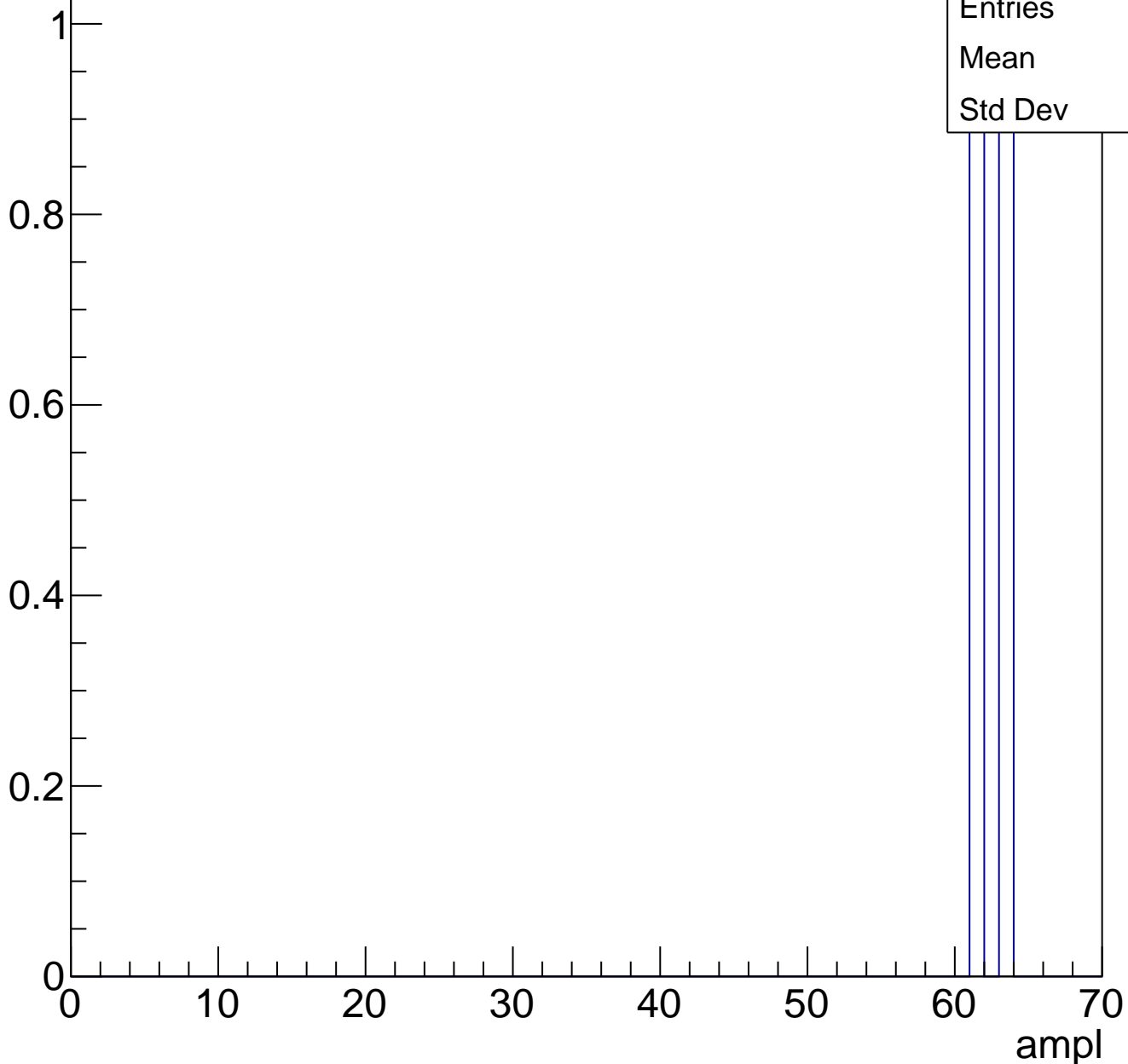
Entry



# B0L001S, U6-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U6-ch86, adc0

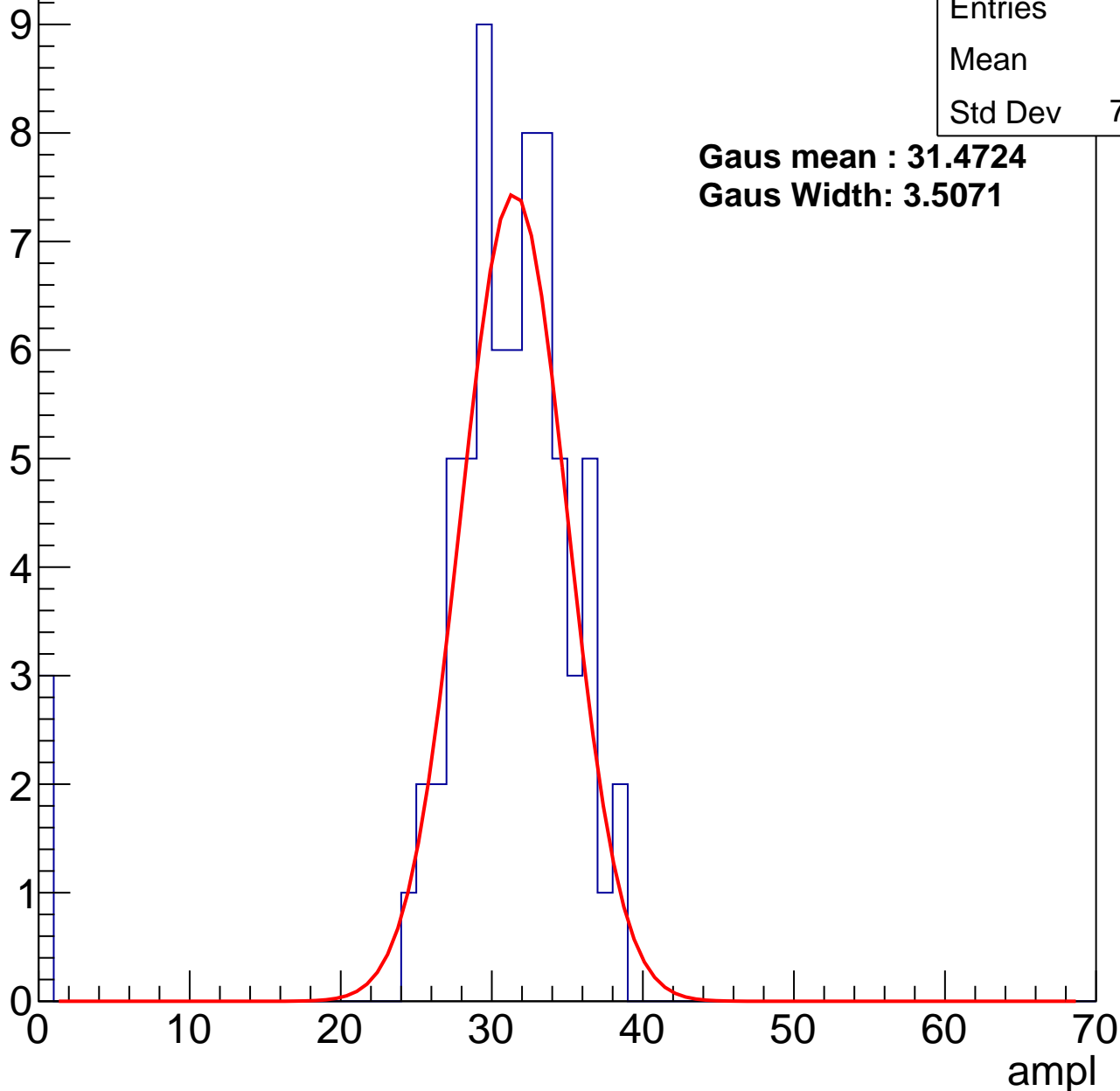
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	29.8
Std Dev	7.032

**Gaus mean : 31.4724**

**Gaus Width: 3.5071**



# B0L001S, U6-ch86, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	64
Mean	37.44
Std Dev	3.288

**Gaus mean : 37.8918**

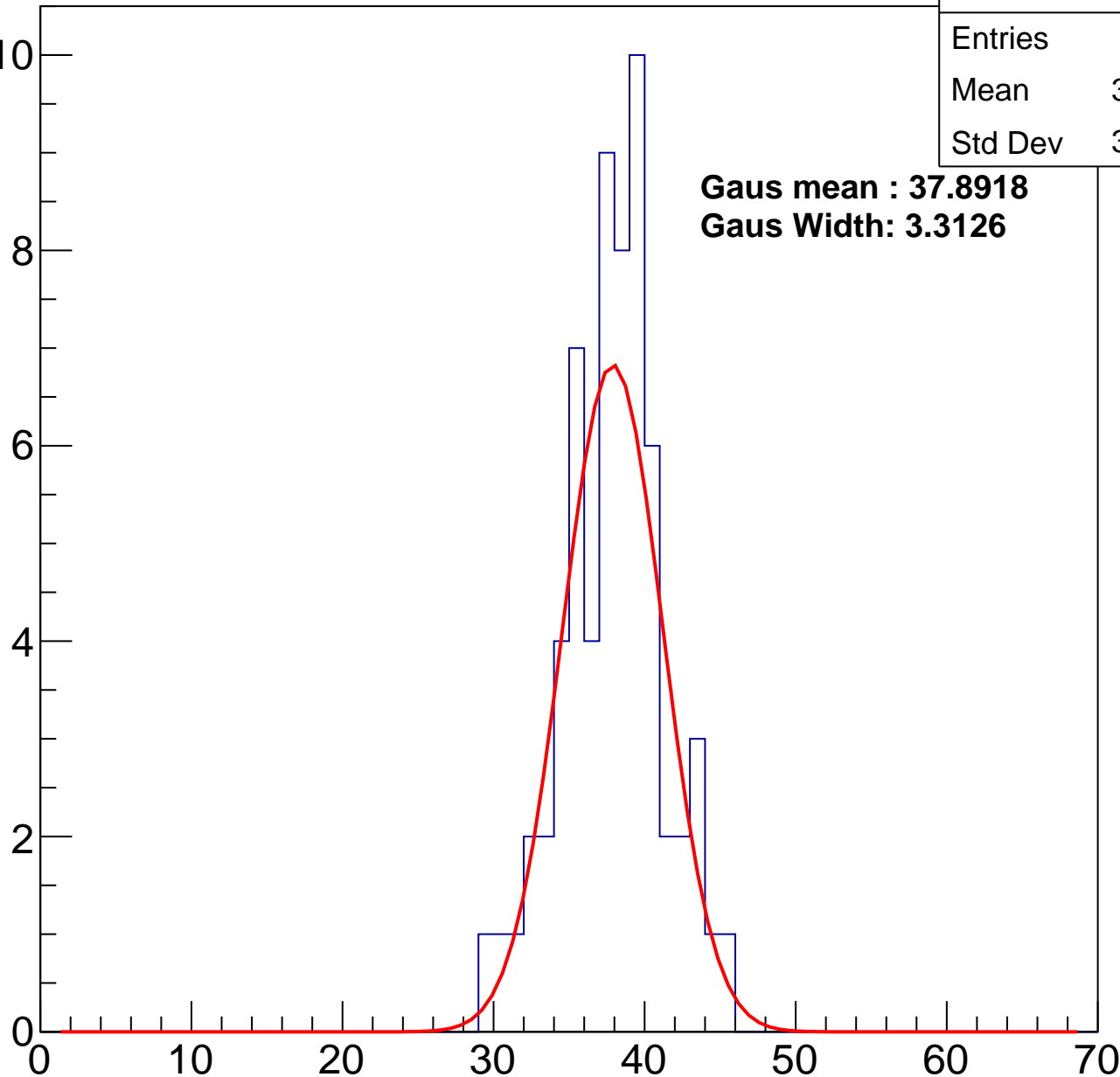
**Gaus Width: 3.3126**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U6-ch86, adc2

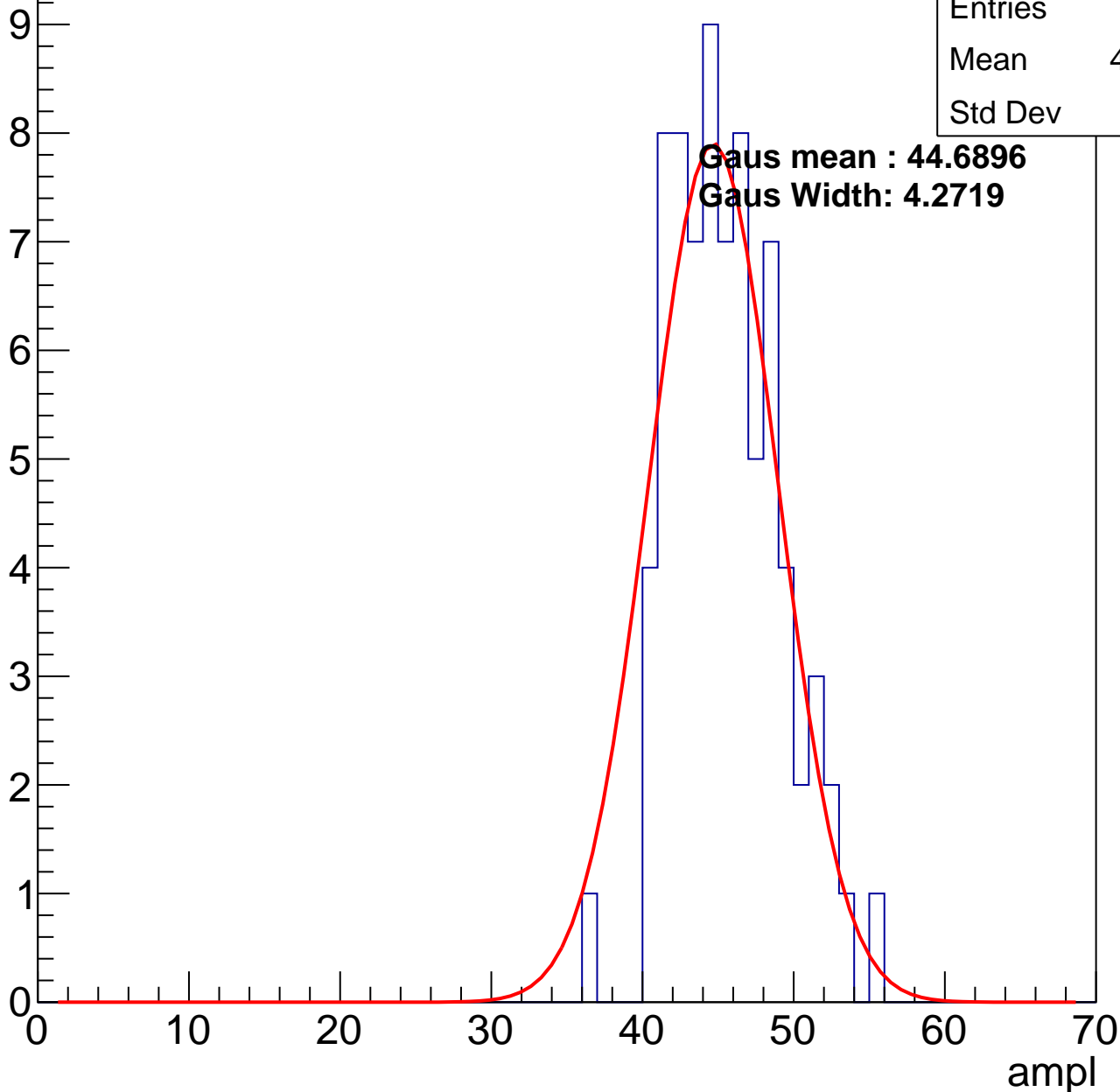
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	45.09
Std Dev	3.59

**Gaus mean : 44.6896**

**Gaus Width: 4.2719**

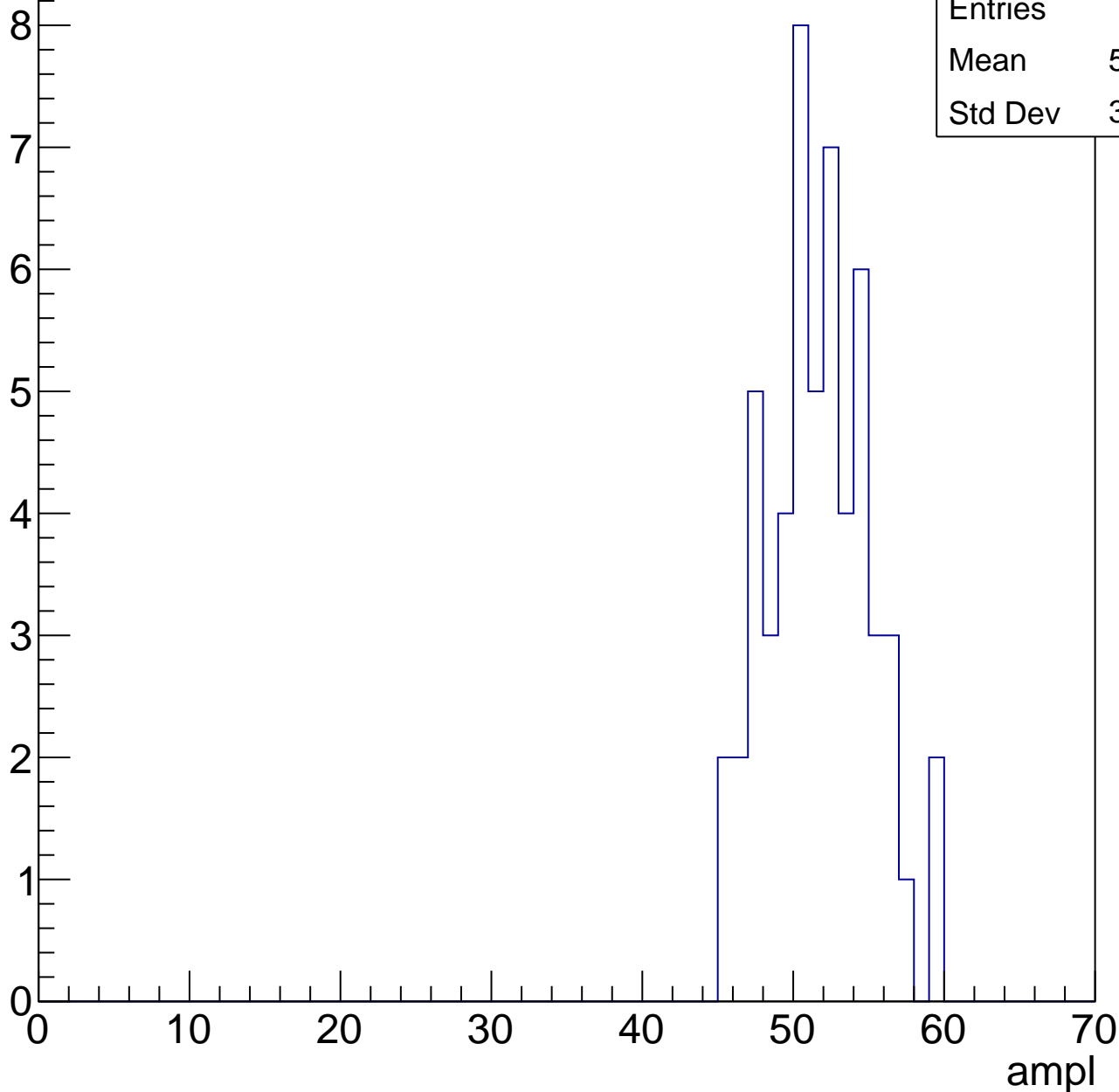


# B0L001S, U6-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	51.27
Std Dev	3.338

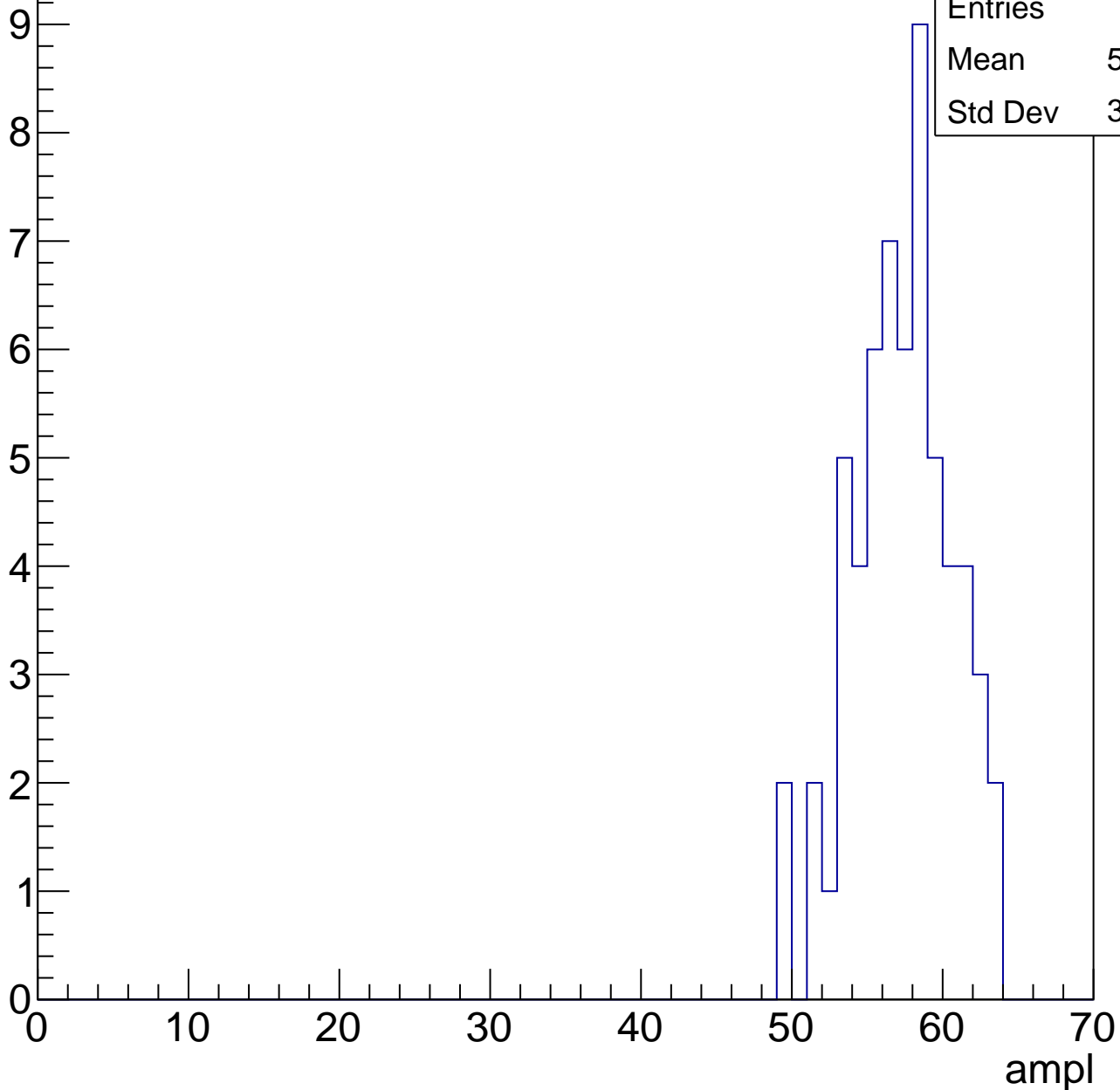


# B0L001S, U6-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	56.83
Std Dev	3.282

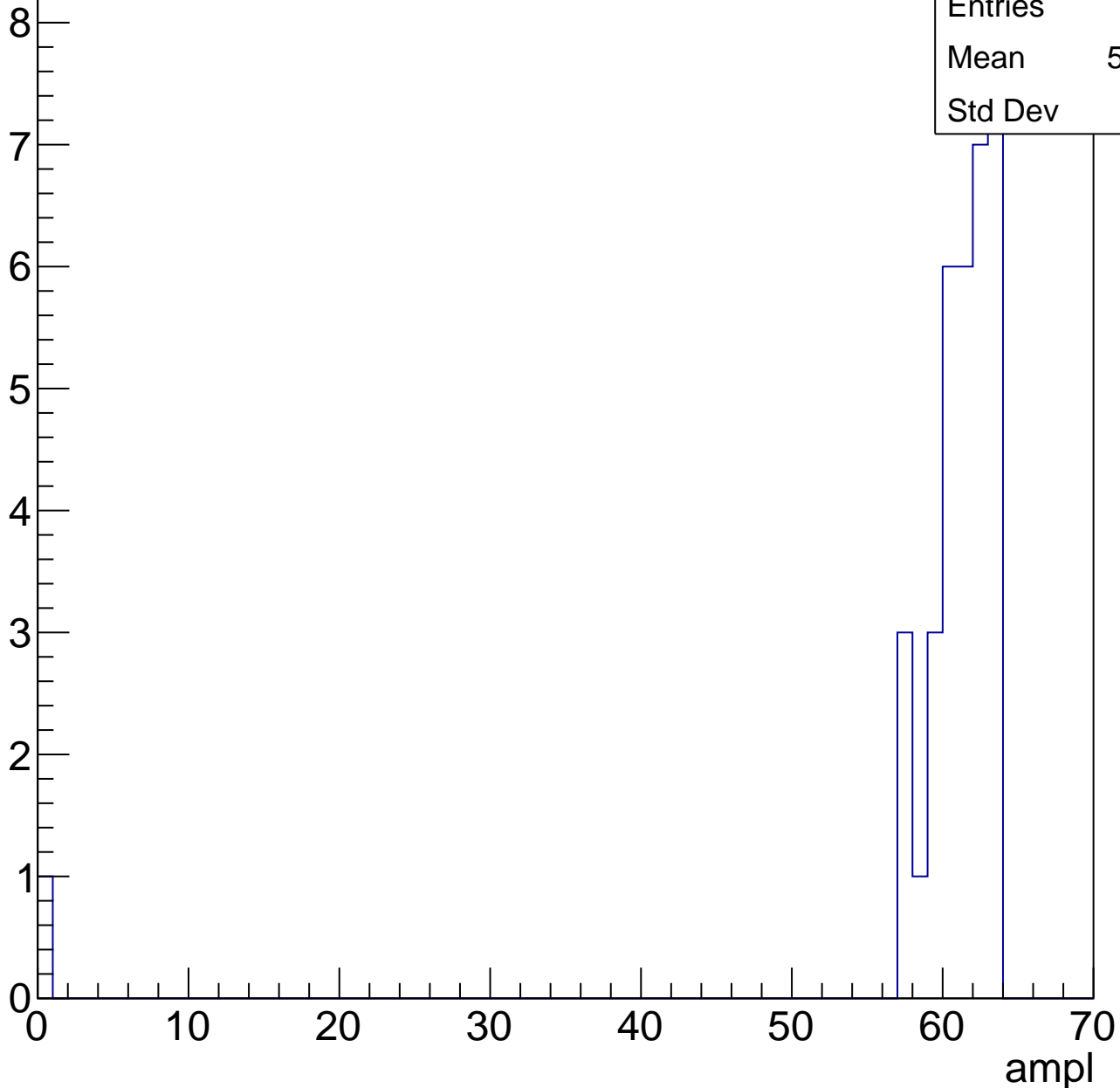


# B0L001S, U6-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	35
Mean	59.14
Std Dev	10.3



# B0L001S, U6-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U6-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U6-ch87, adc0

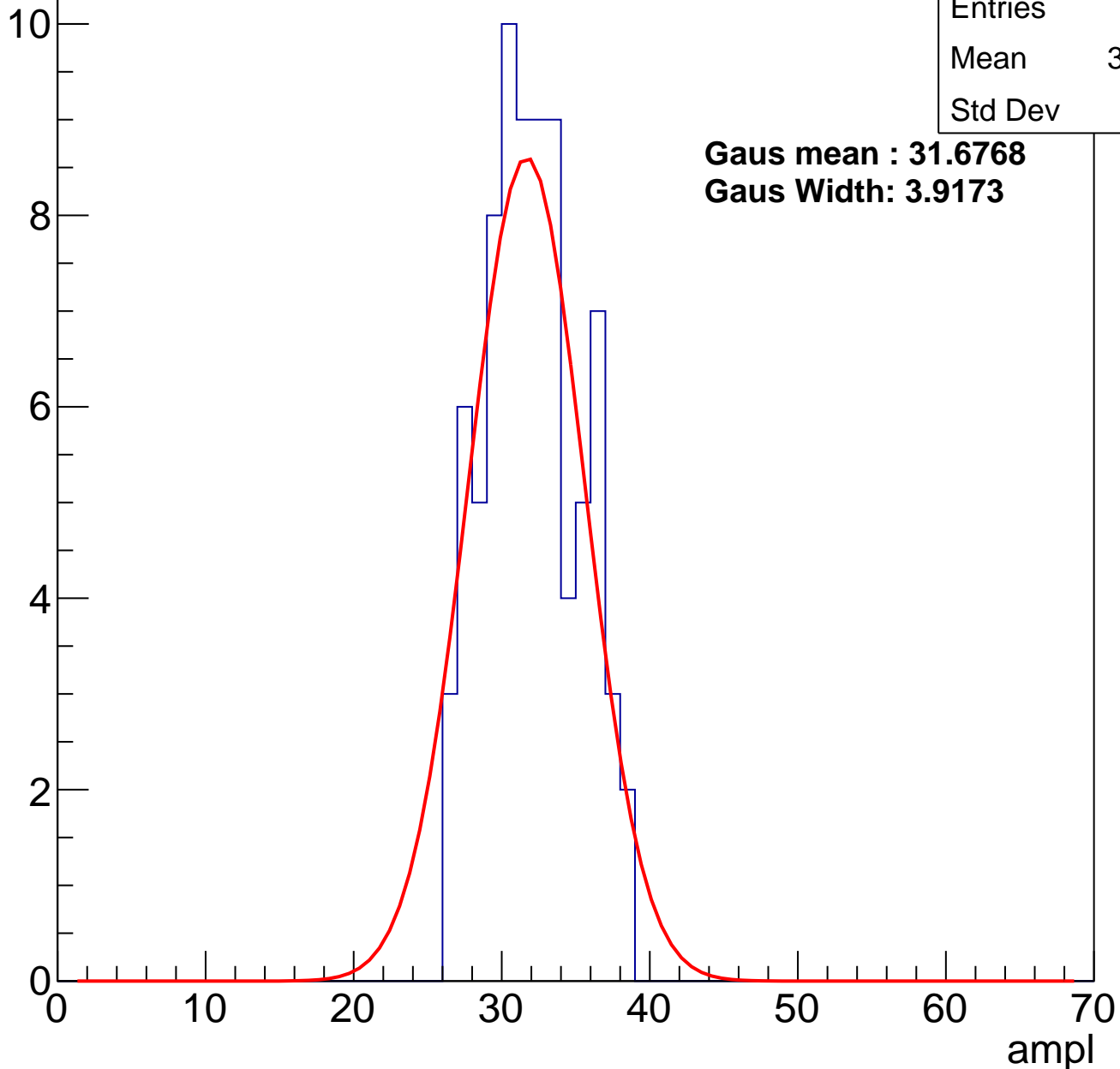
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	80
Mean	31.57
Std Dev	3.11

**Gaus mean : 31.6768**

**Gaus Width: 3.9173**

Entry



# B0L001S, U6-ch87, adc1

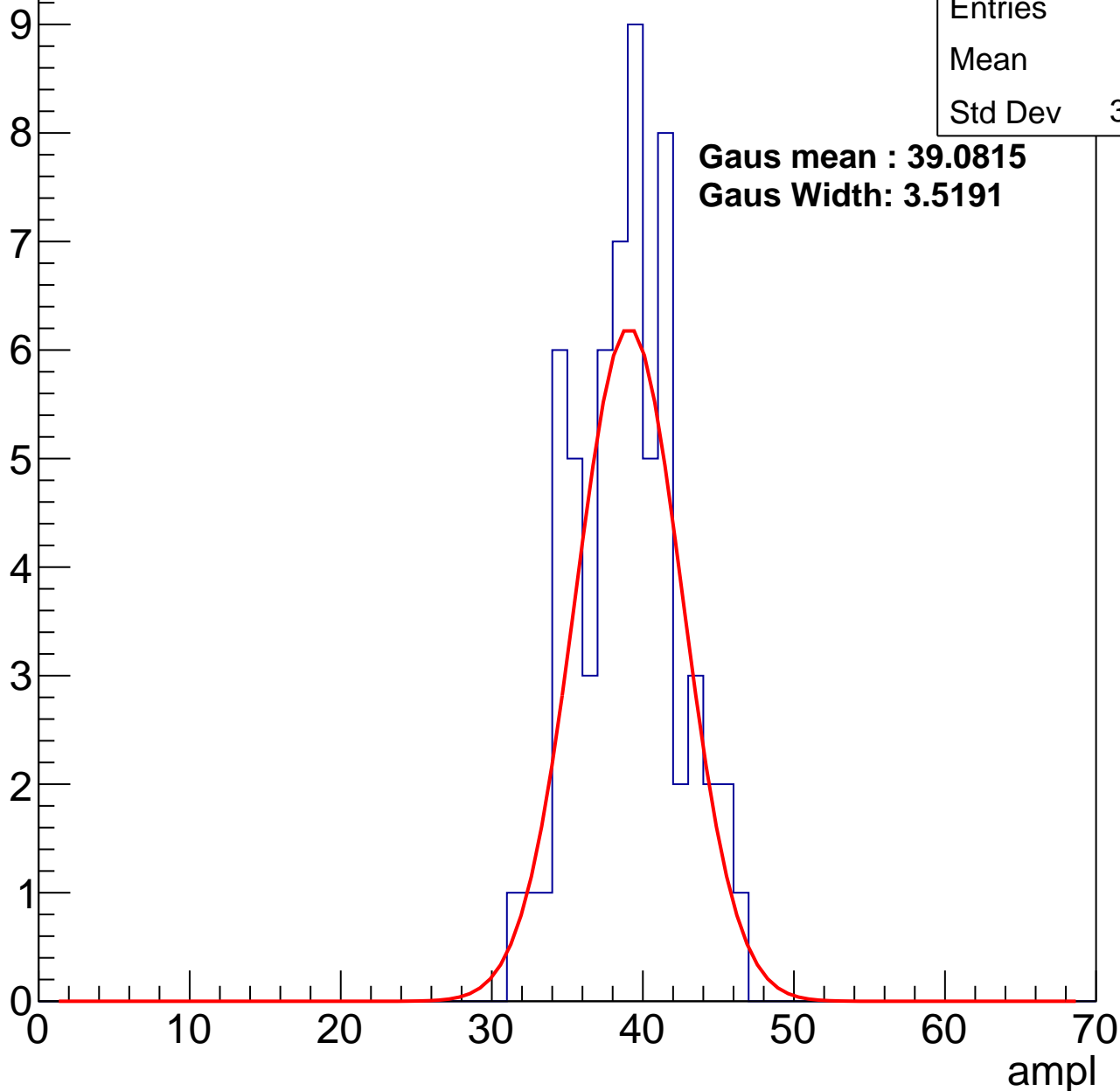
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	38.5
Std Dev	3.349

**Gaus mean : 39.0815**

**Gaus Width: 3.5191**



# B0L001S, U6-ch87, adc2

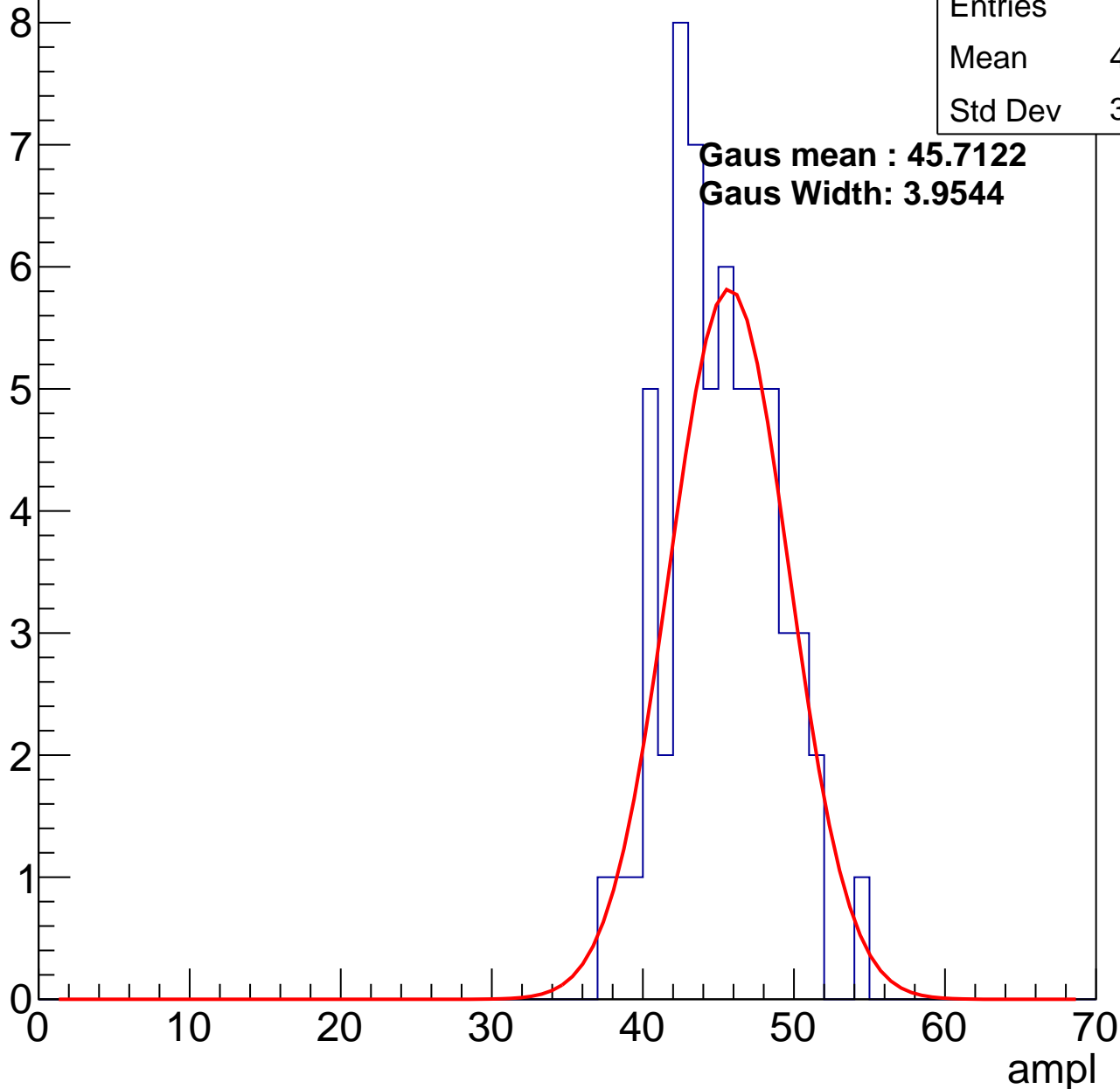
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	44.68
Std Dev	3.538

**Gaus mean : 45.7122**

**Gaus Width: 3.9544**

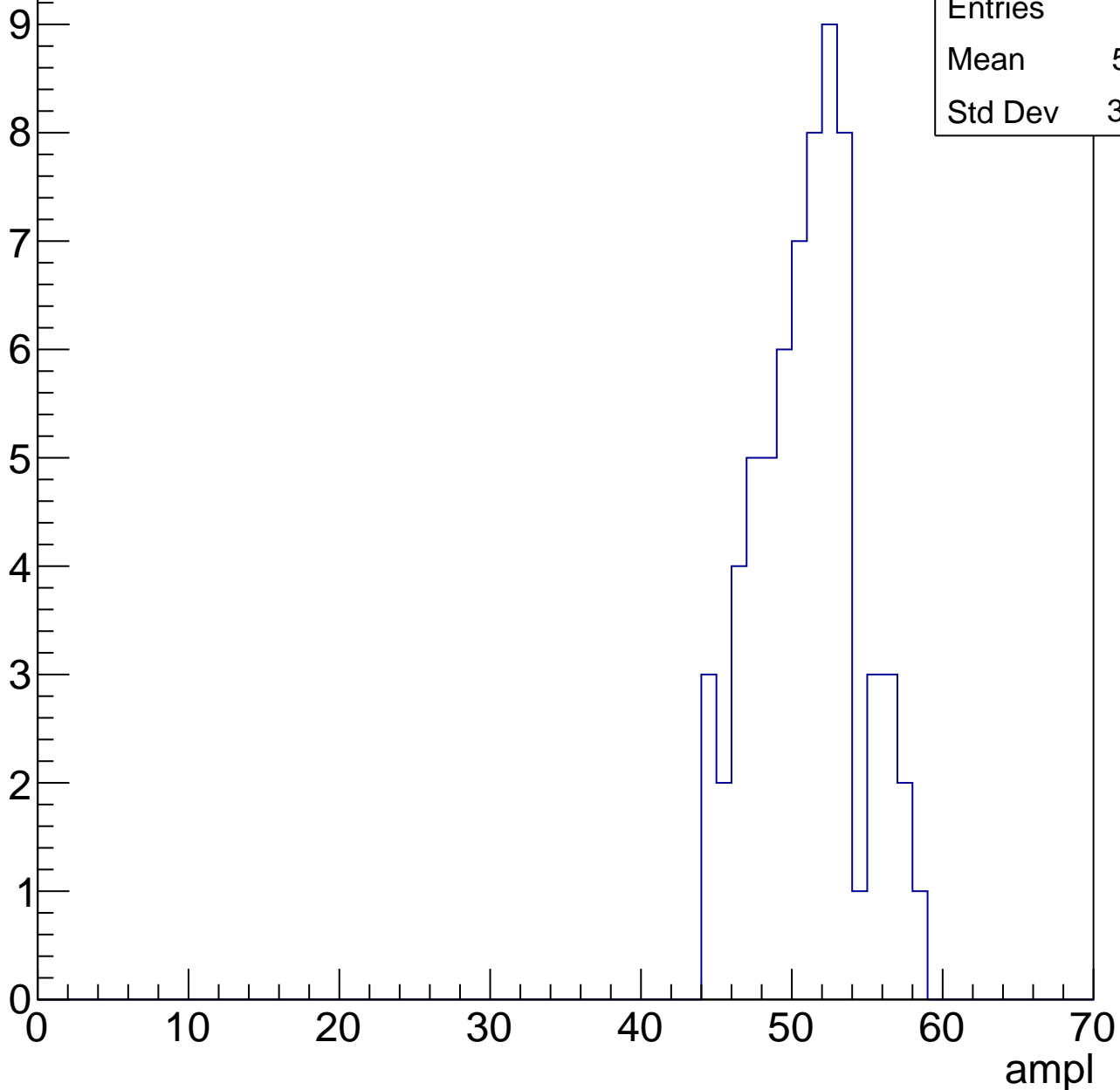


# B0L001S, U6-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

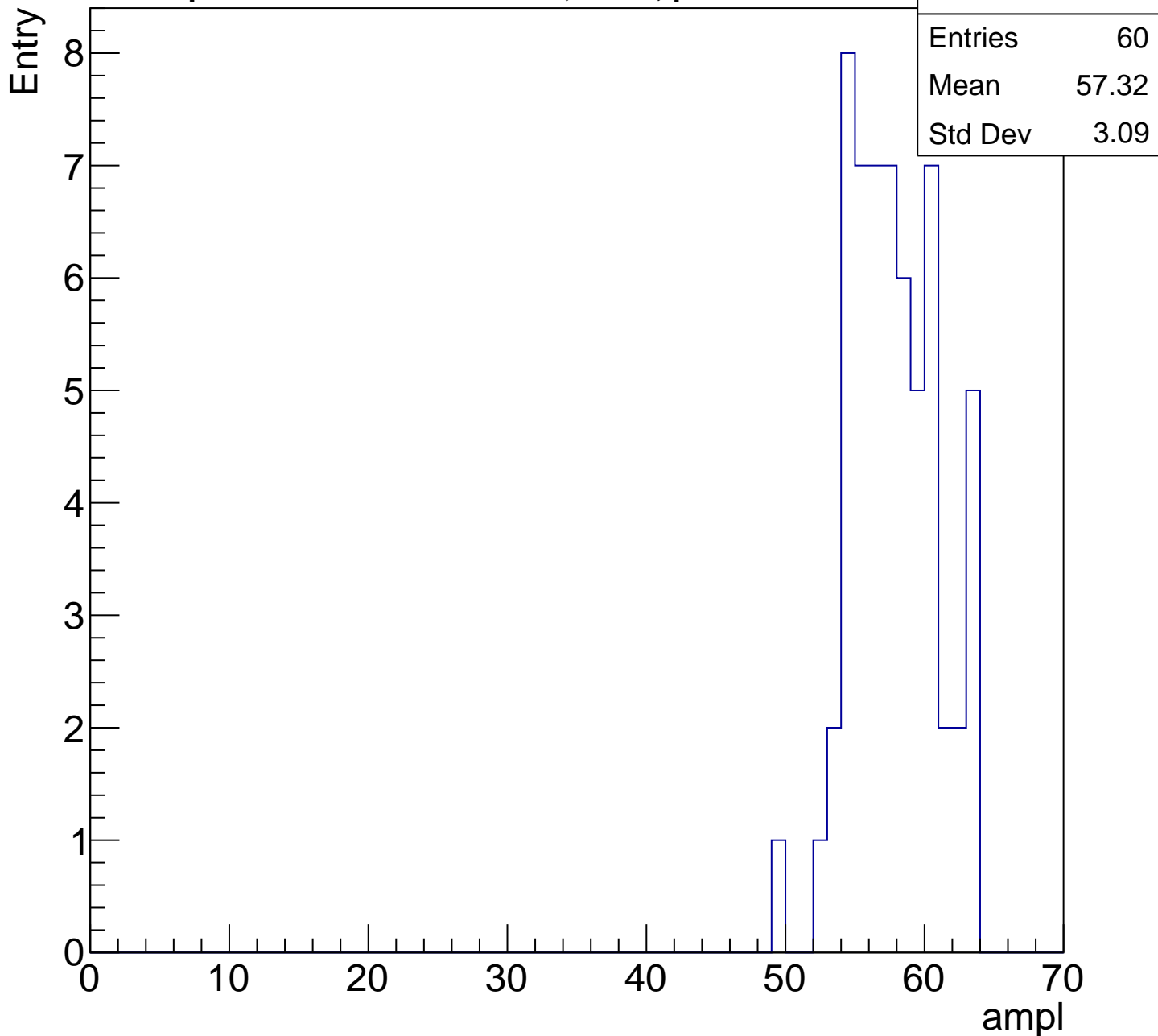
Entry

Entries	67
Mean	50.51
Std Dev	3.352



# B0L001S, U6-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

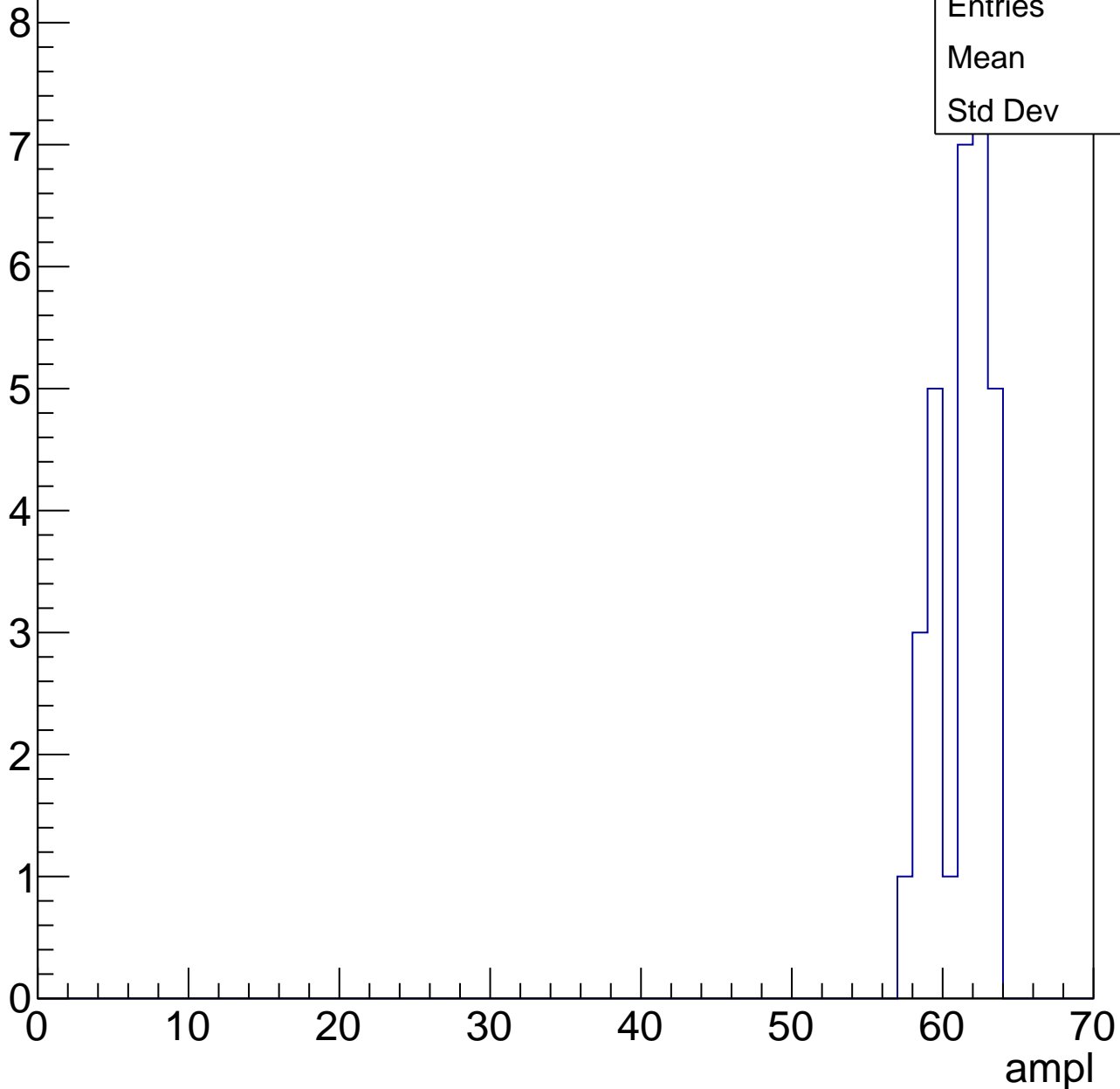


# B0L001S, U6-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

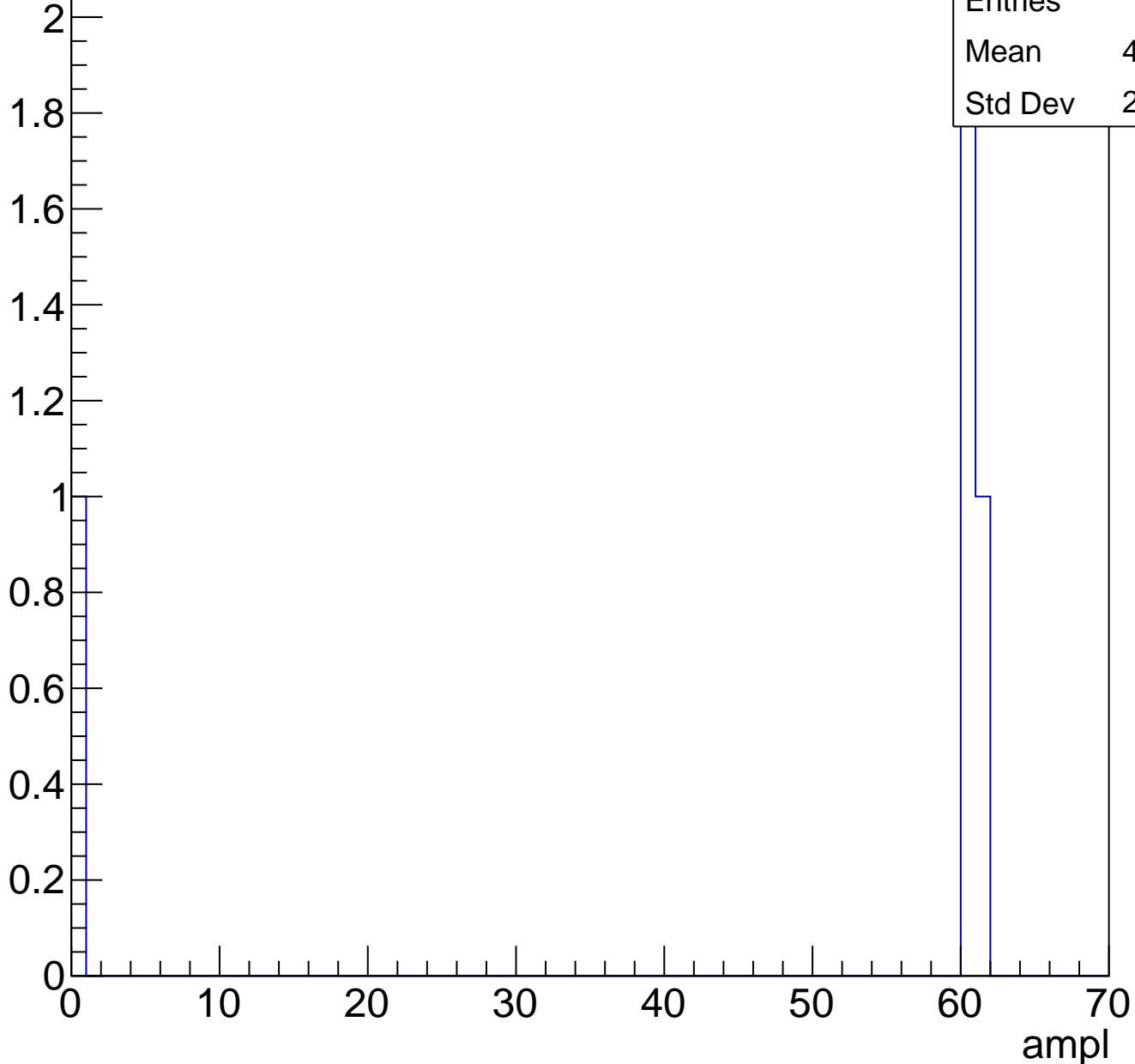
Entries	30
Mean	60.8
Std Dev	1.74



# B0L001S, U6-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	4
Mean	45.25
Std Dev	26.13



# B0L001S, U6-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch88, adc0

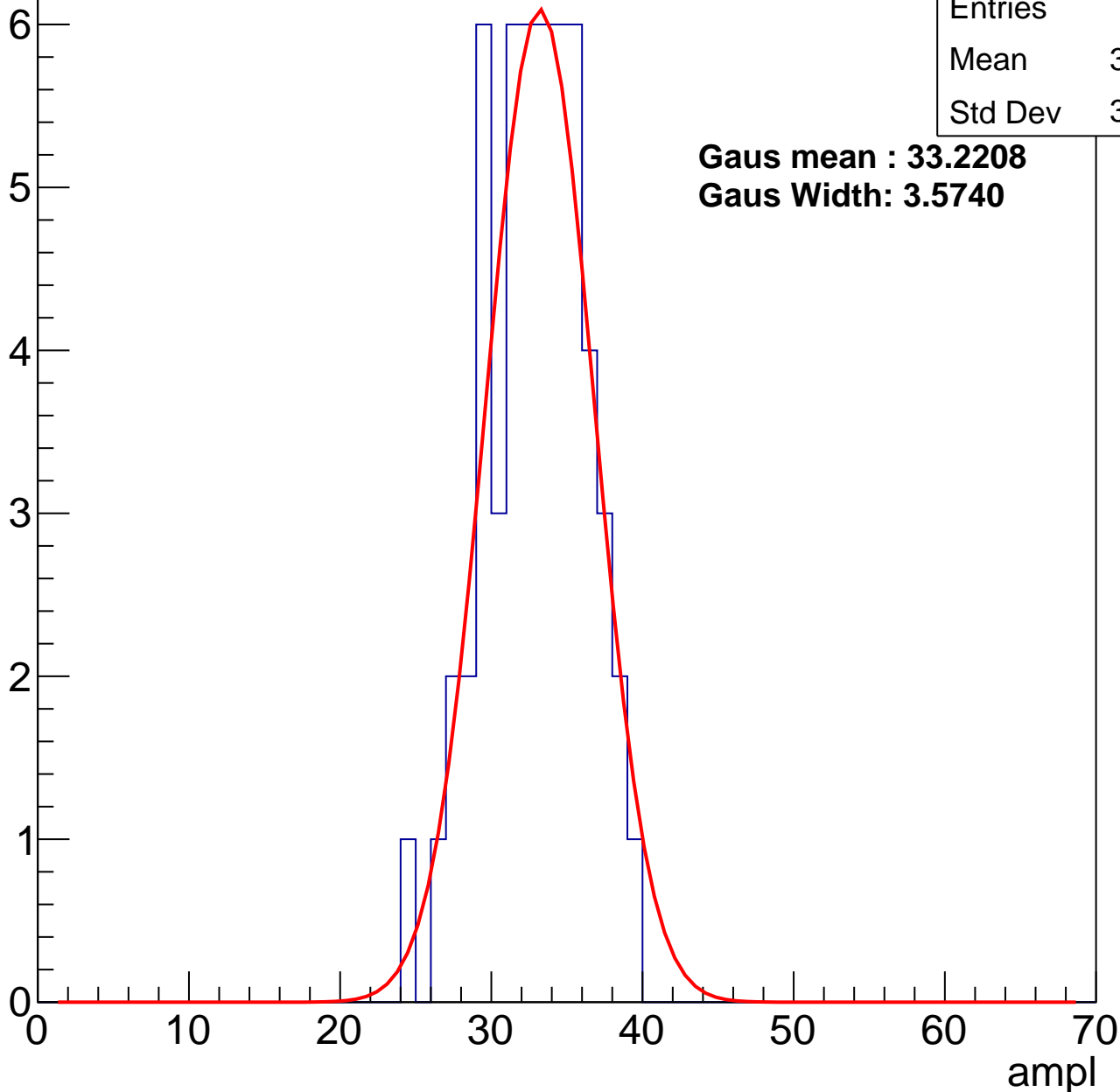
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	32.44
Std Dev	3.268

**Gaus mean : 33.2208**

**Gaus Width: 3.5740**



# B0L001S, U6-ch88, adc1

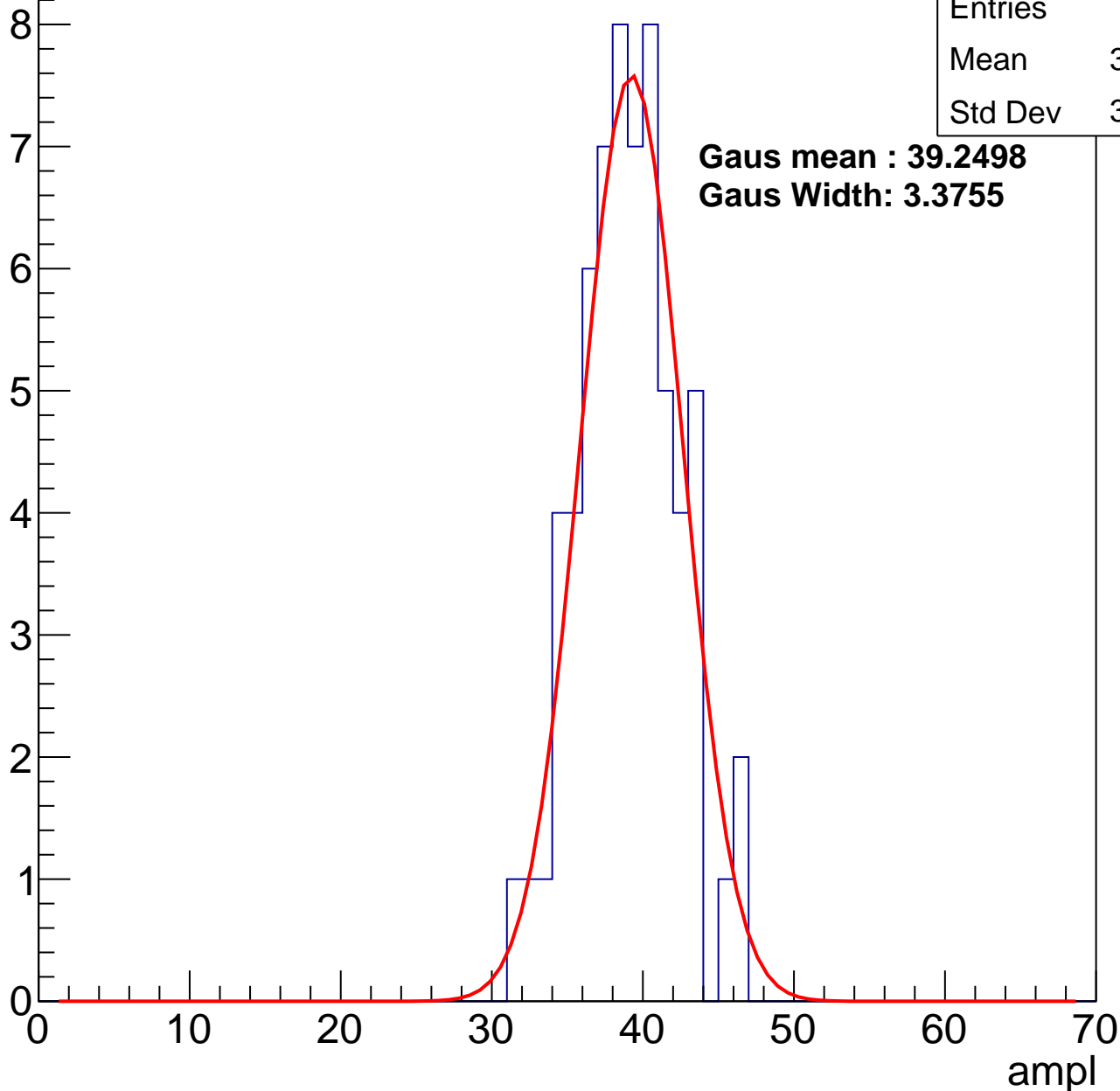
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	38.58
Std Dev	3.235

**Gaus mean : 39.2498**

**Gaus Width: 3.3755**



# B0L001S, U6-ch88, adc2

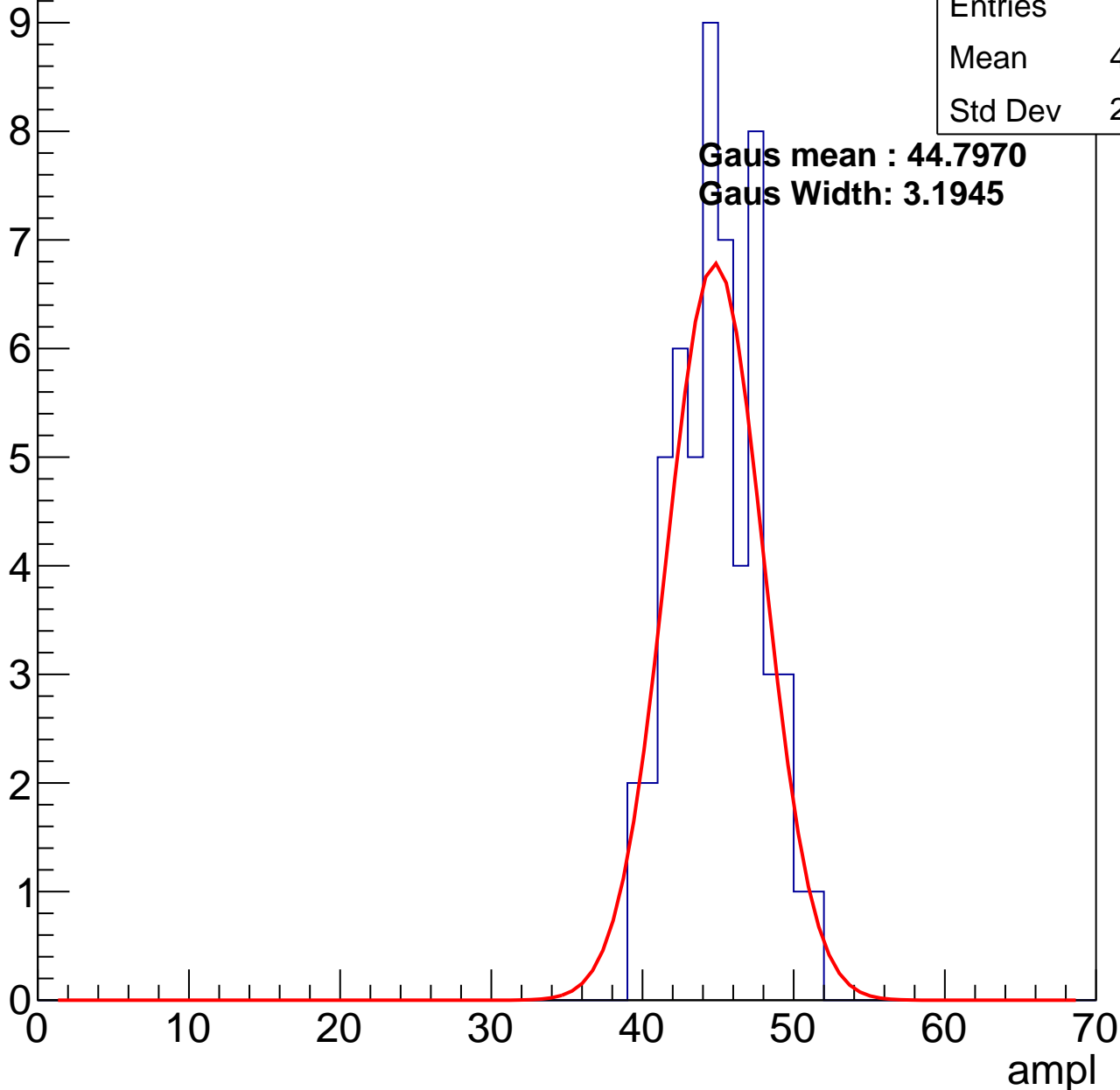
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	44.52
Std Dev	2.816

**Gaus mean : 44.7970**

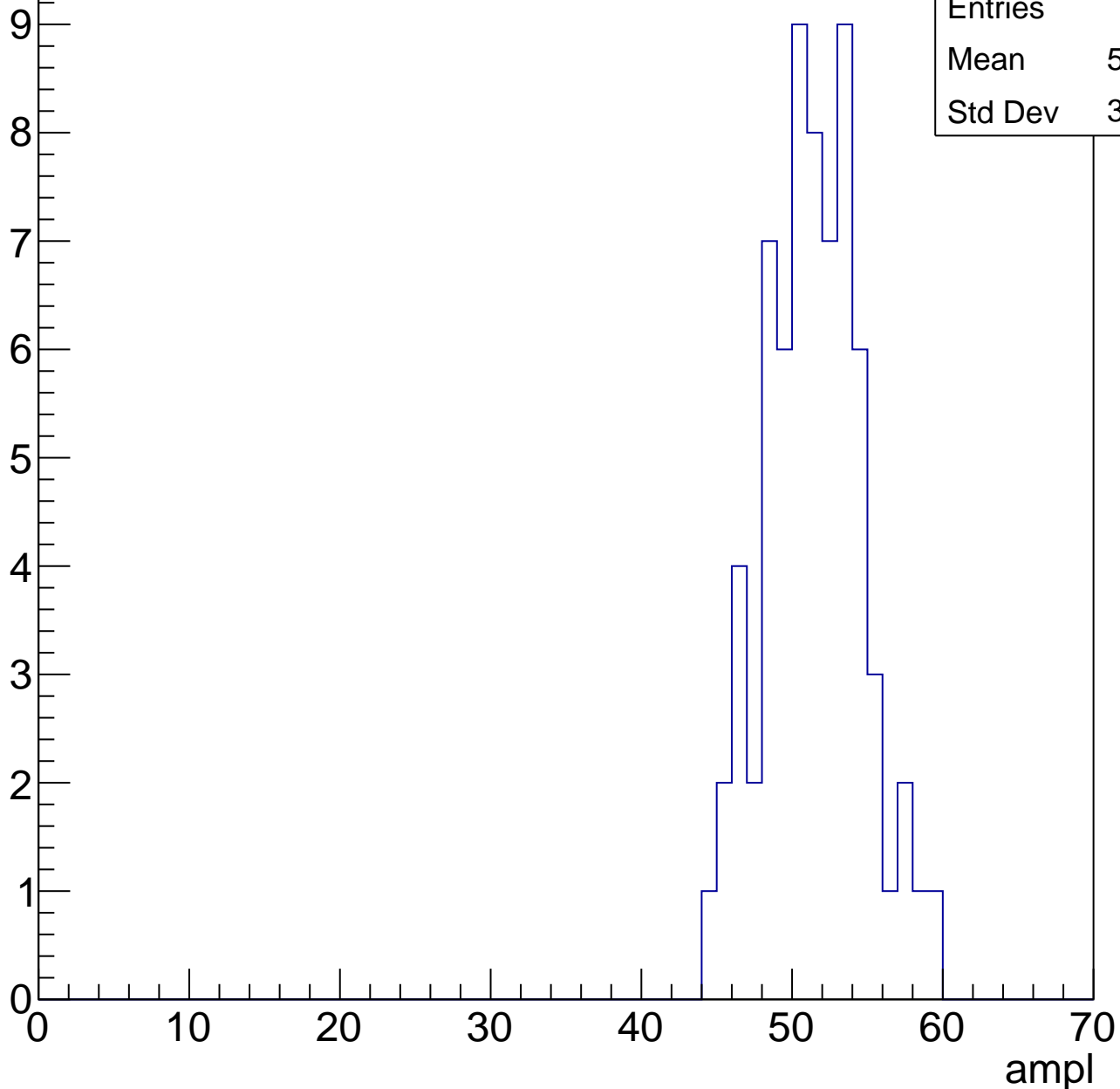
**Gaus Width: 3.1945**



# B0L001S, U6-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

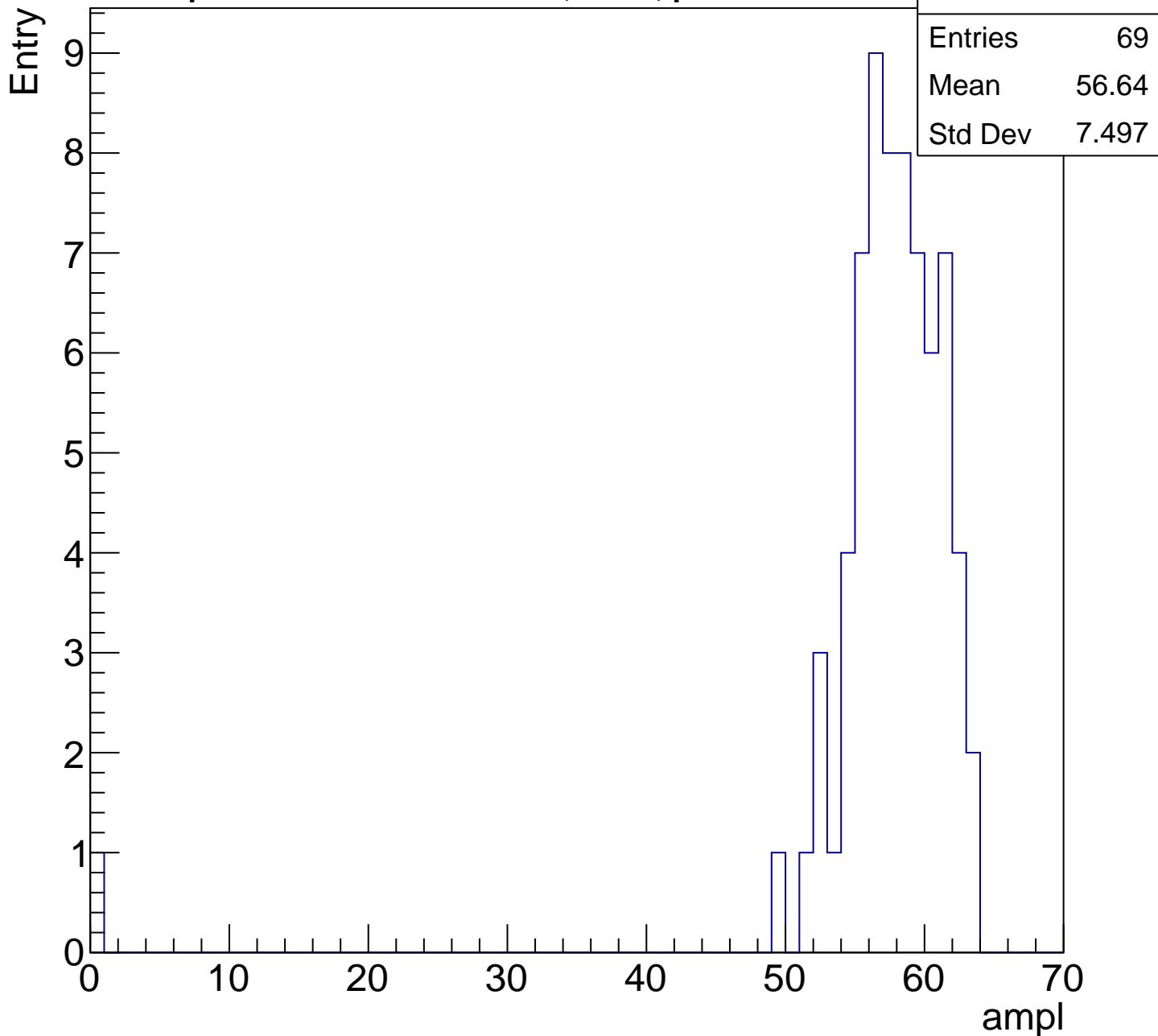
Entry



Entries	69
Mean	50.97
Std Dev	3.194

# B0L001S, U6-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

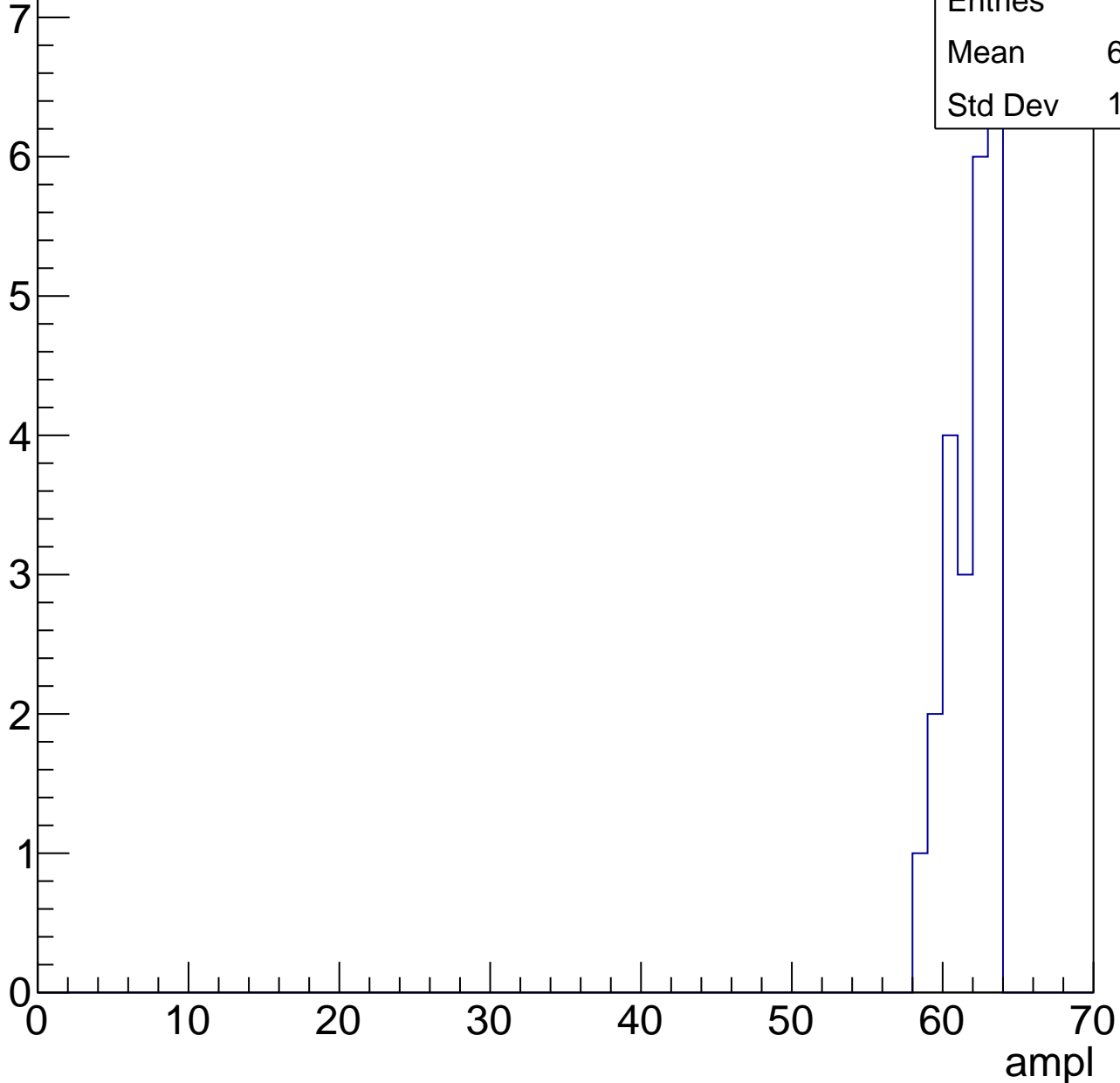


# B0L001S, U6-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

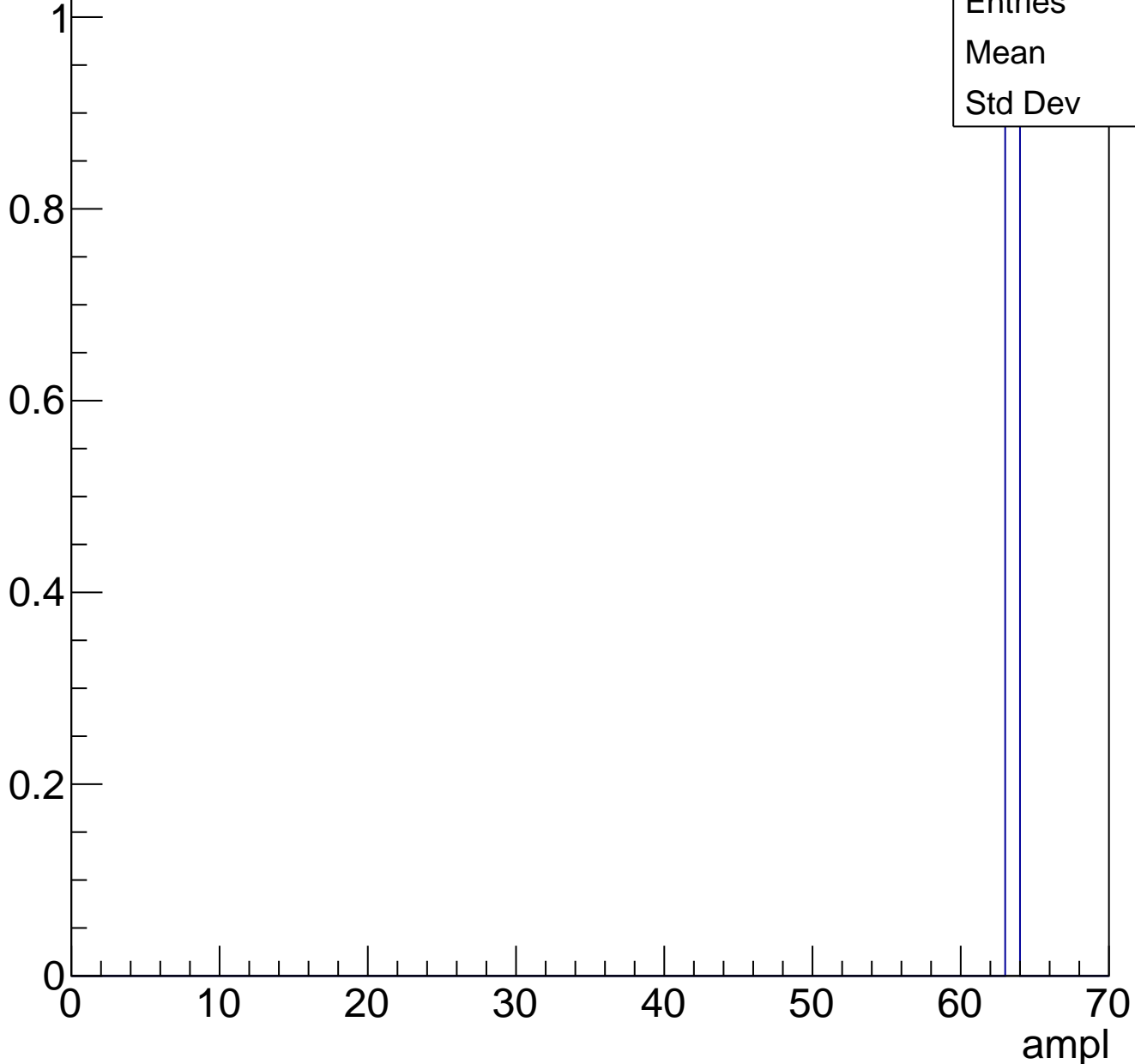
Entries	23
Mean	61.39
Std Dev	1.496



# B0L001S, U6-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U6-ch89, adc0

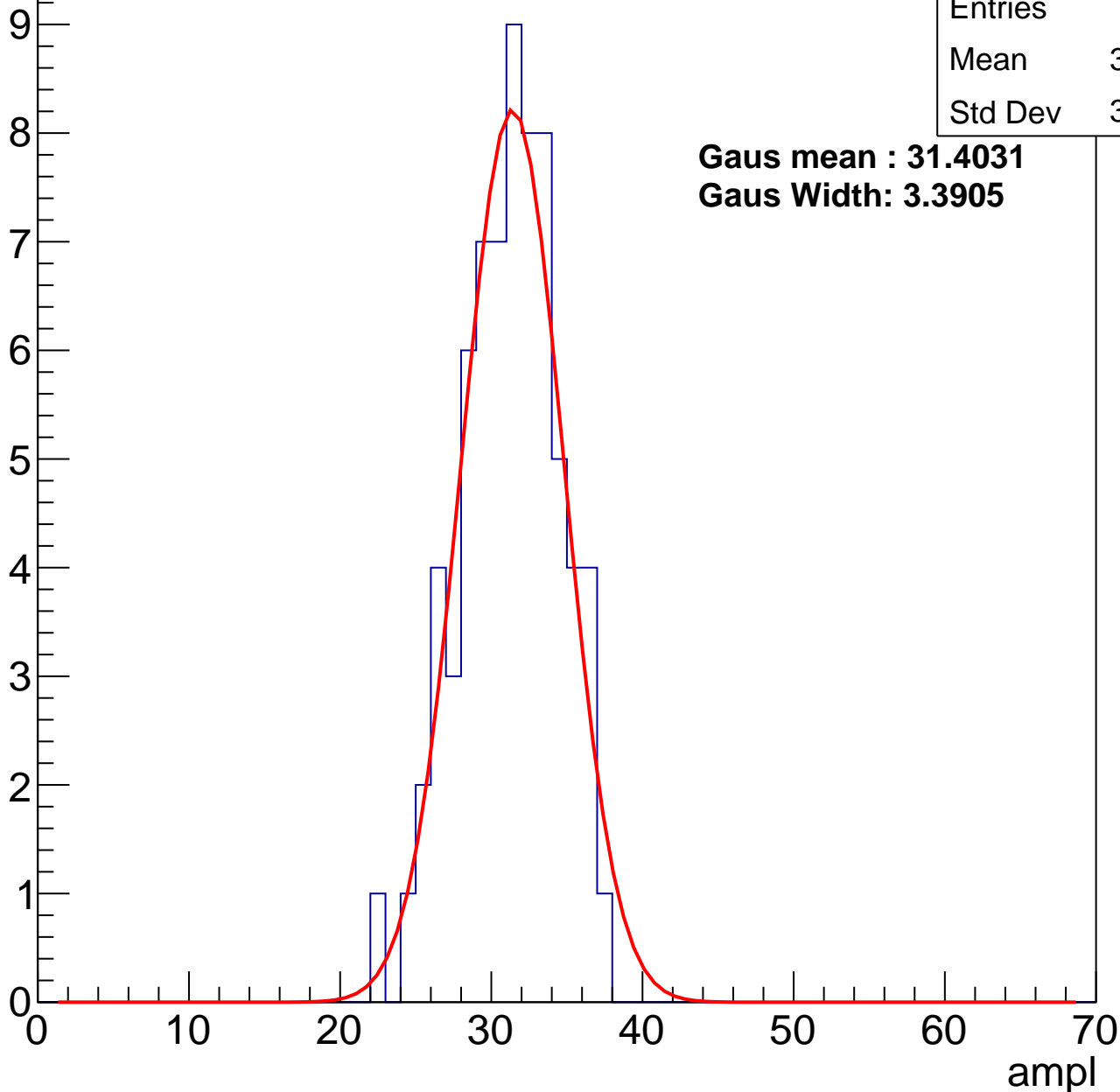
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	30.74
Std Dev	3.206

**Gaus mean : 31.4031**

**Gaus Width: 3.3905**



# B0L001S, U6-ch89, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	63
Mean	37.86
Std Dev	3.299

**Gaus mean : 38.2498**

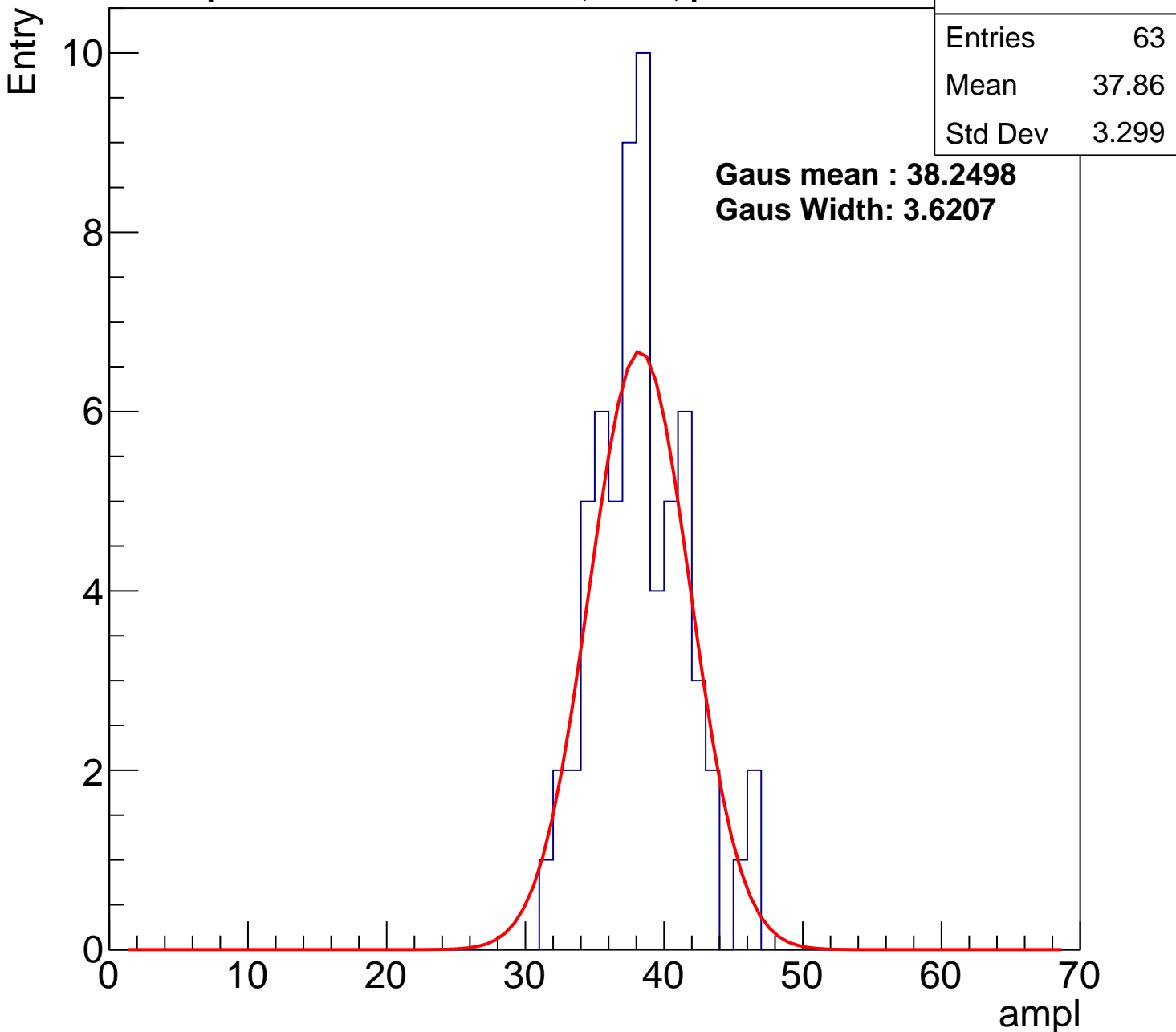
**Gaus Width: 3.6207**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U6-ch89, adc2

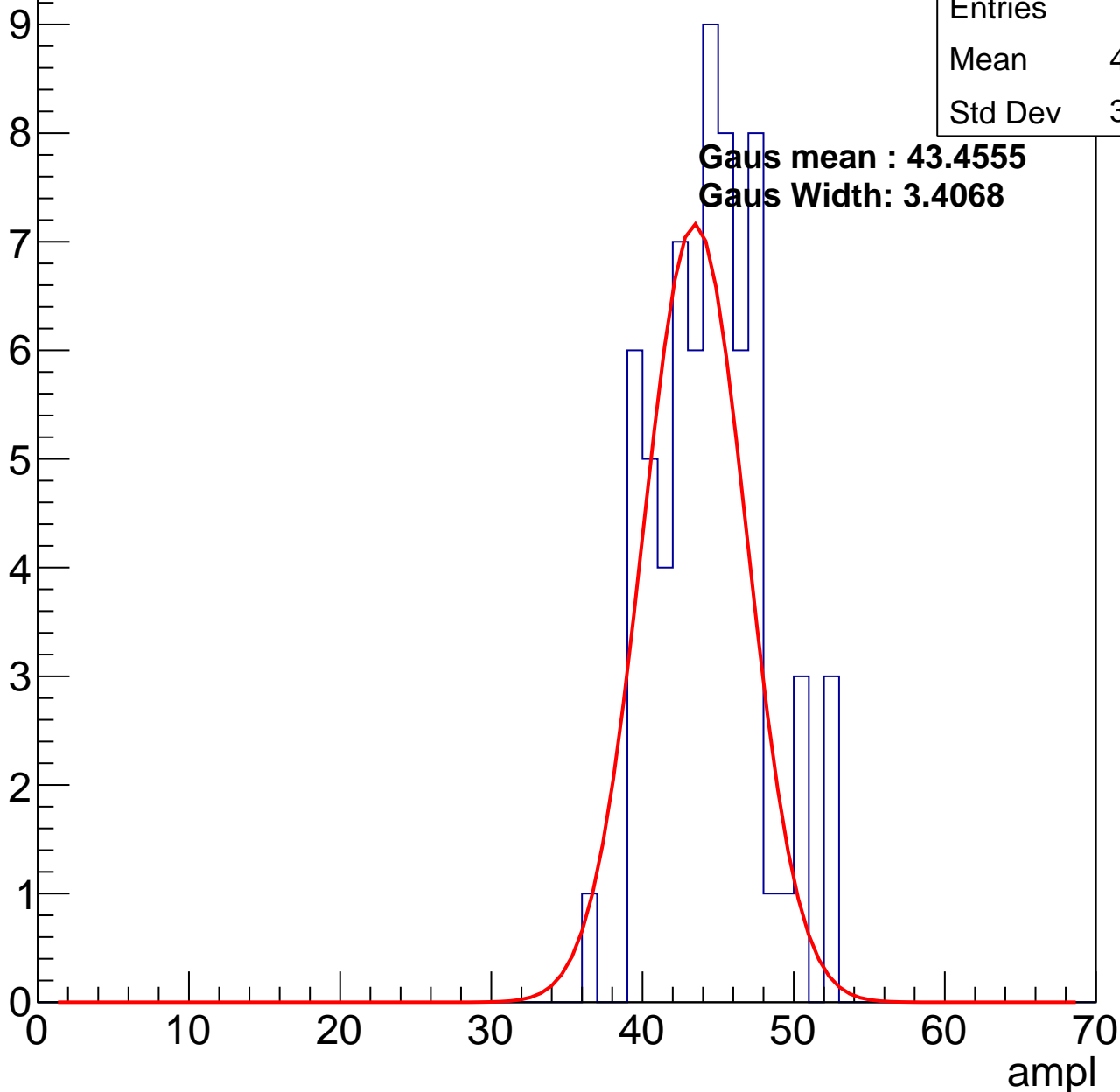
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	44.07
Std Dev	3.448

**Gaus mean : 43.4555**

**Gaus Width: 3.4068**

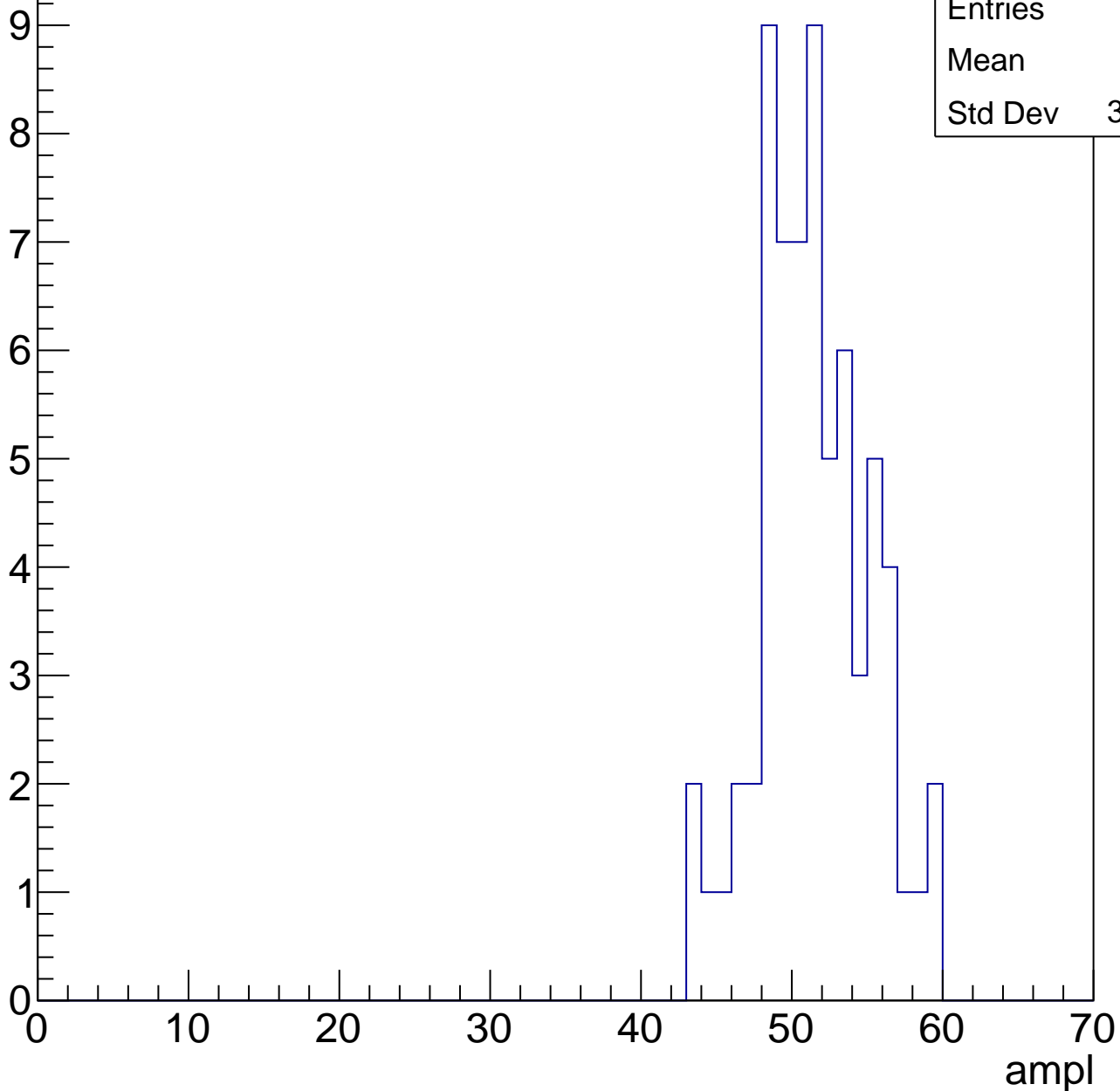


# B0L001S, U6-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	51
Std Dev	3.583

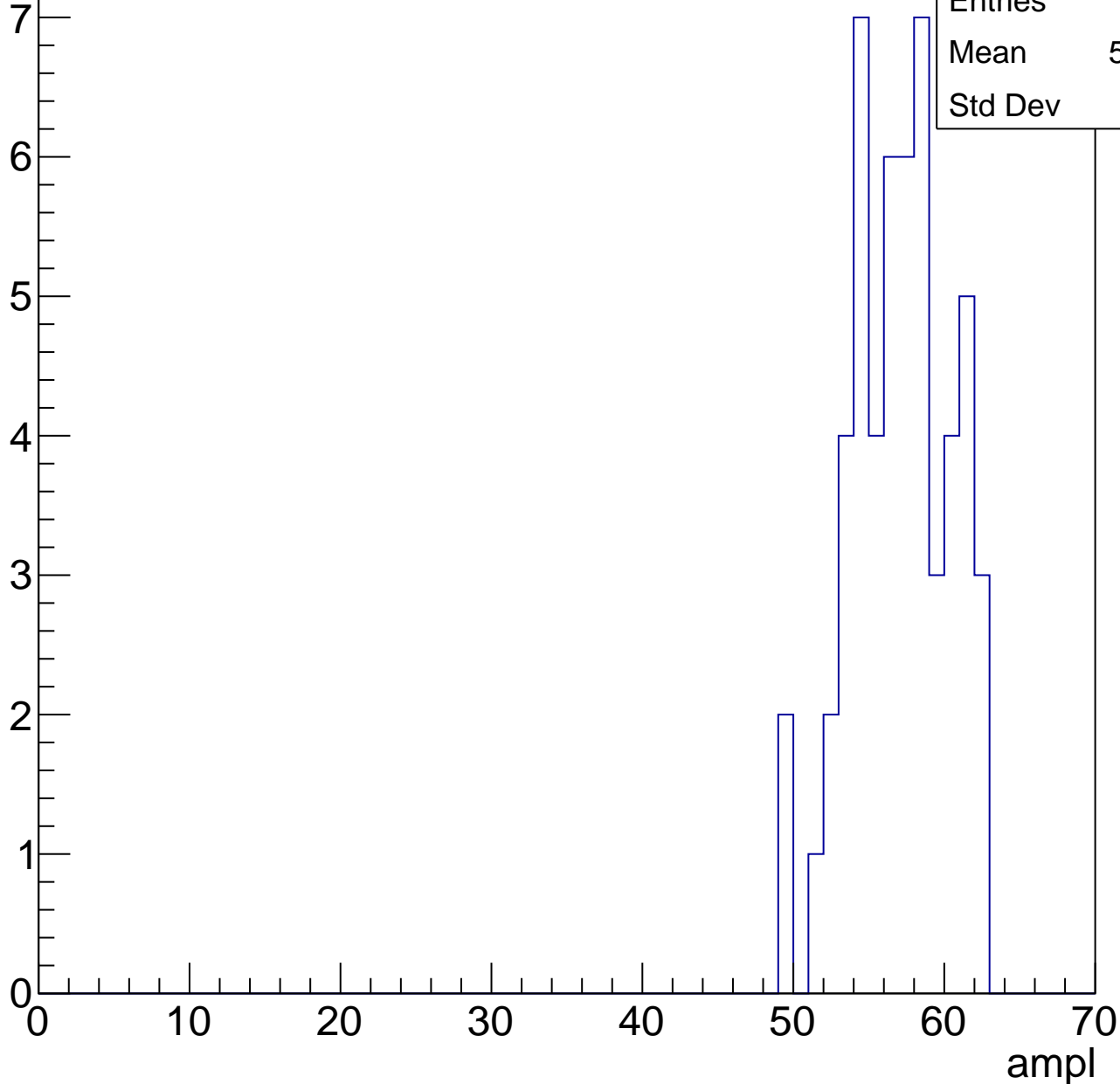


# B0L001S, U6-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	56.57
Std Dev	3.23

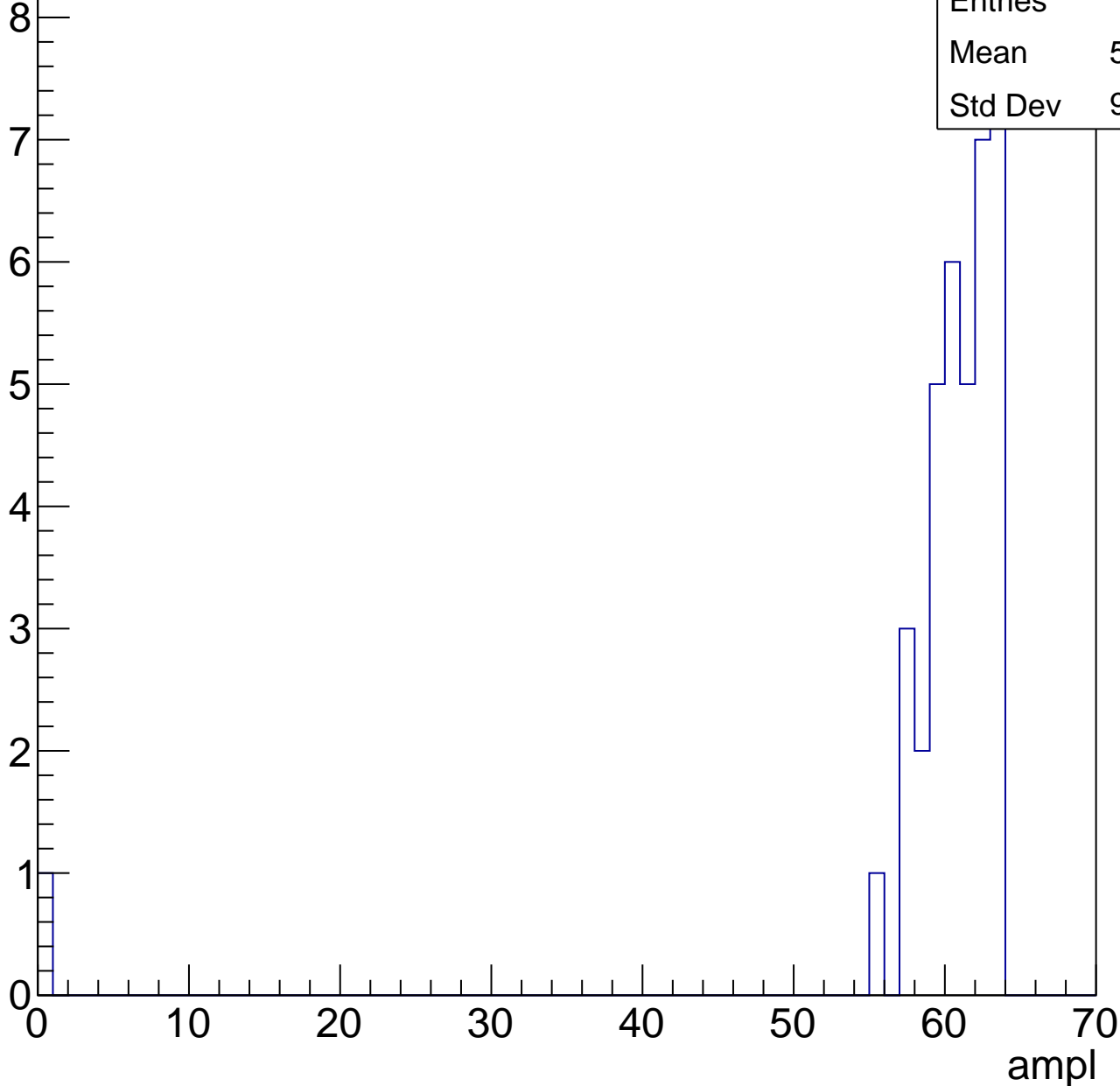


# B0L001S, U6-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	38
Mean	58.95
Std Dev	9.905



# B0L001S, U6-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch90, adc0

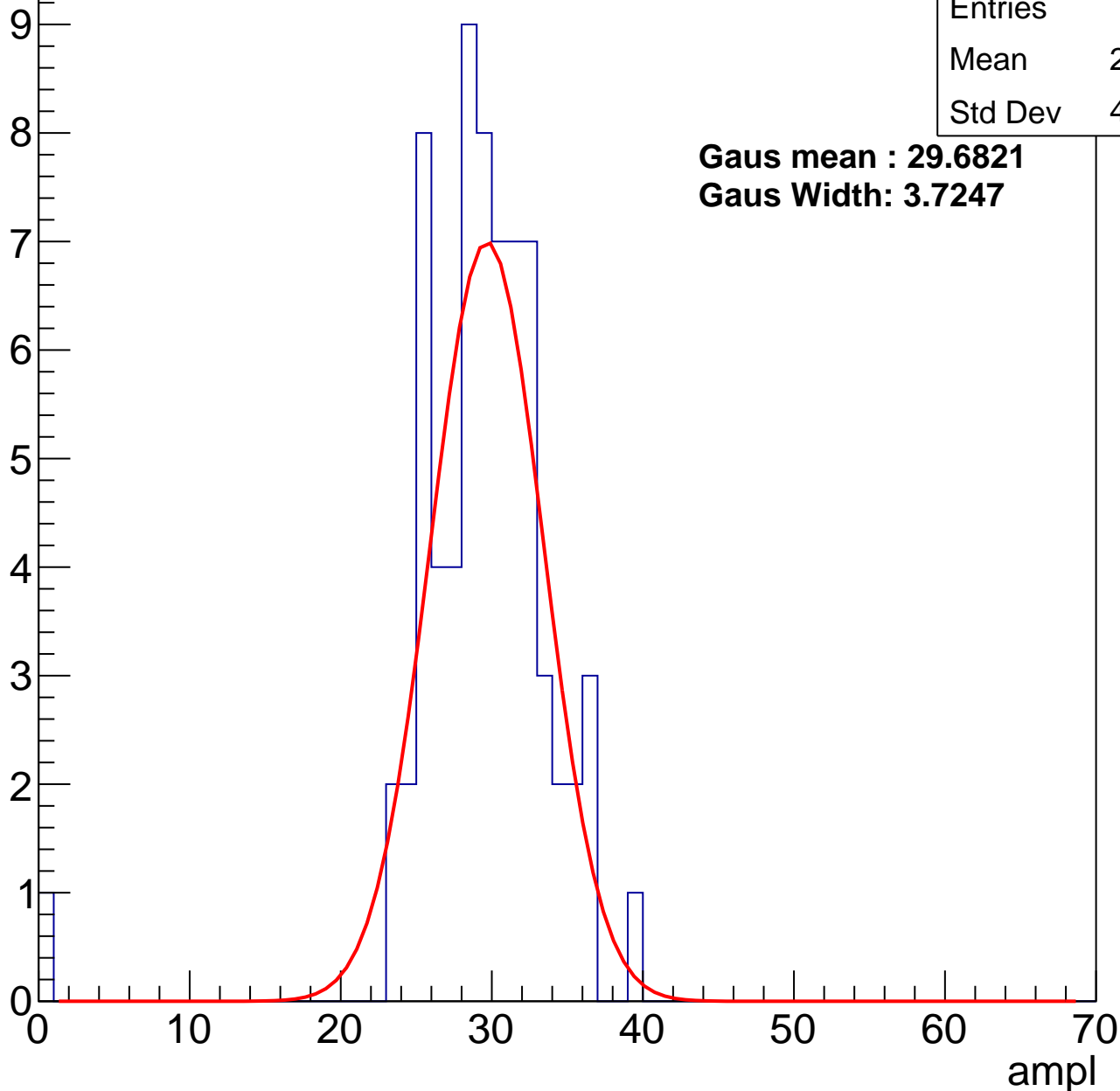
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	28.93
Std Dev	4.879

**Gaus mean : 29.6821**

**Gaus Width: 3.7247**



# B0L001S, U6-ch90, adc1

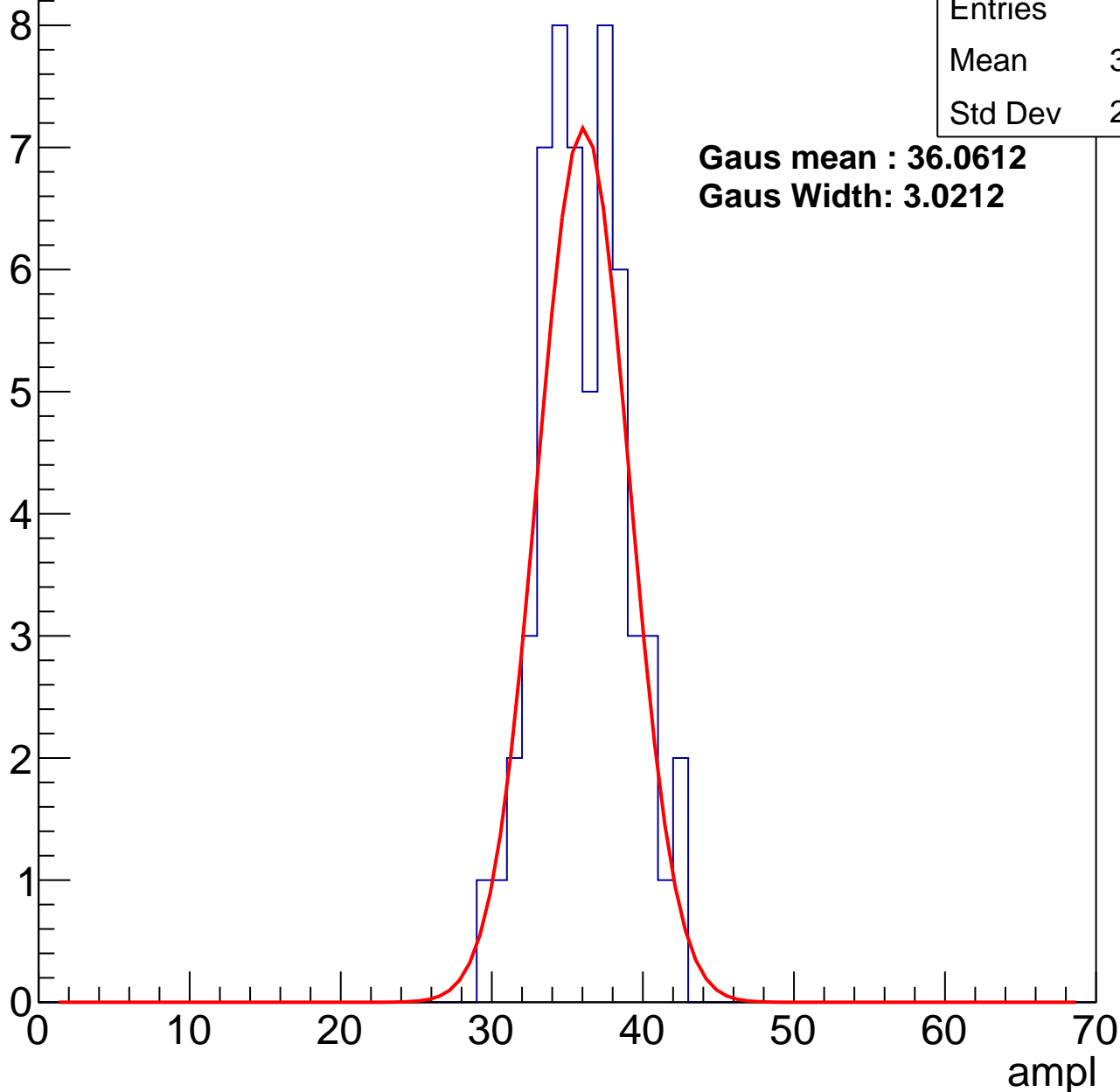
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	35.63
Std Dev	2.906

**Gaus mean : 36.0612**

**Gaus Width: 3.0212**



# B0L001S, U6-ch90, adc2

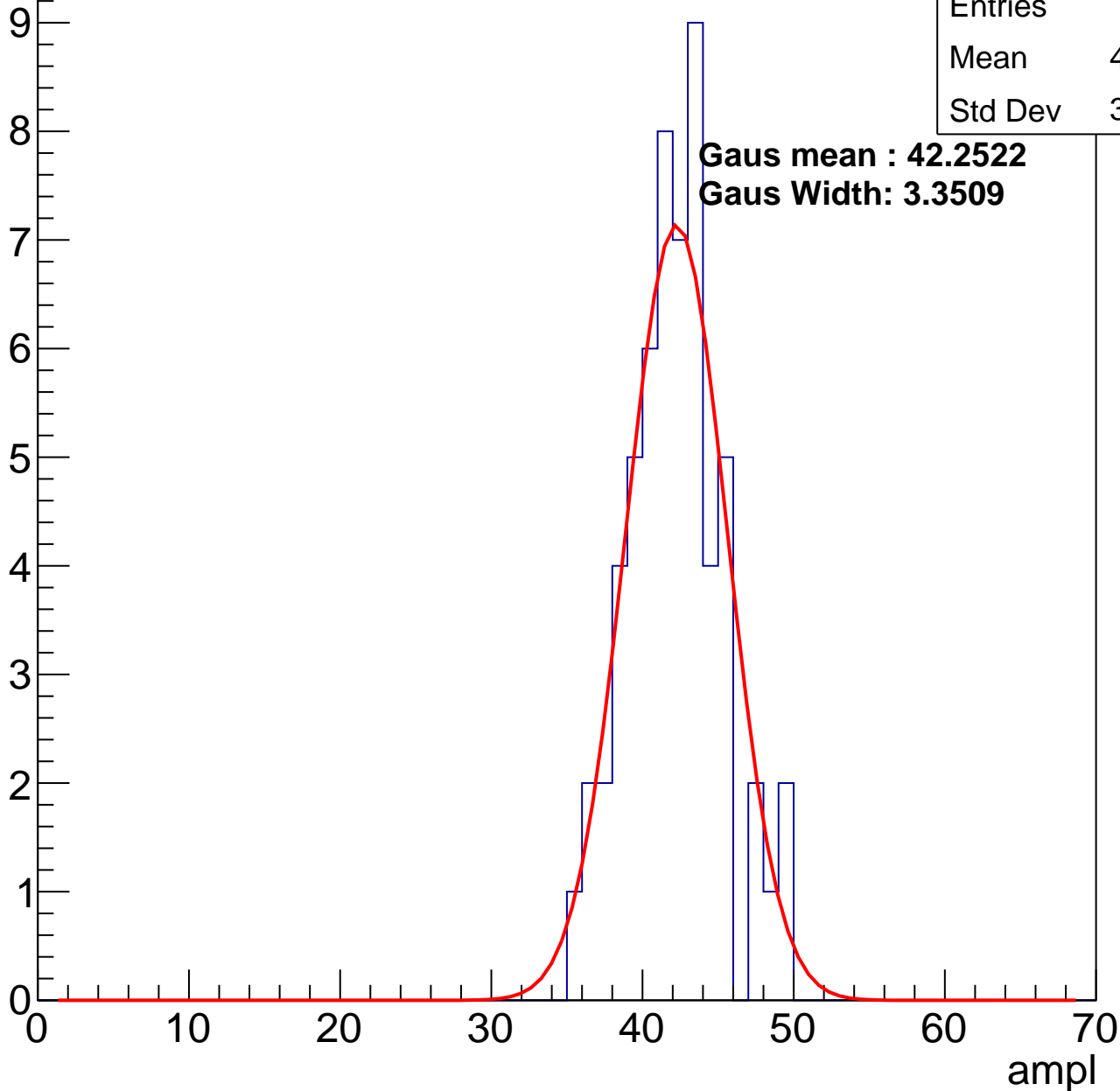
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	41.69
Std Dev	3.108

**Gaus mean : 42.2522**

**Gaus Width: 3.3509**



# B0L001S, U6-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

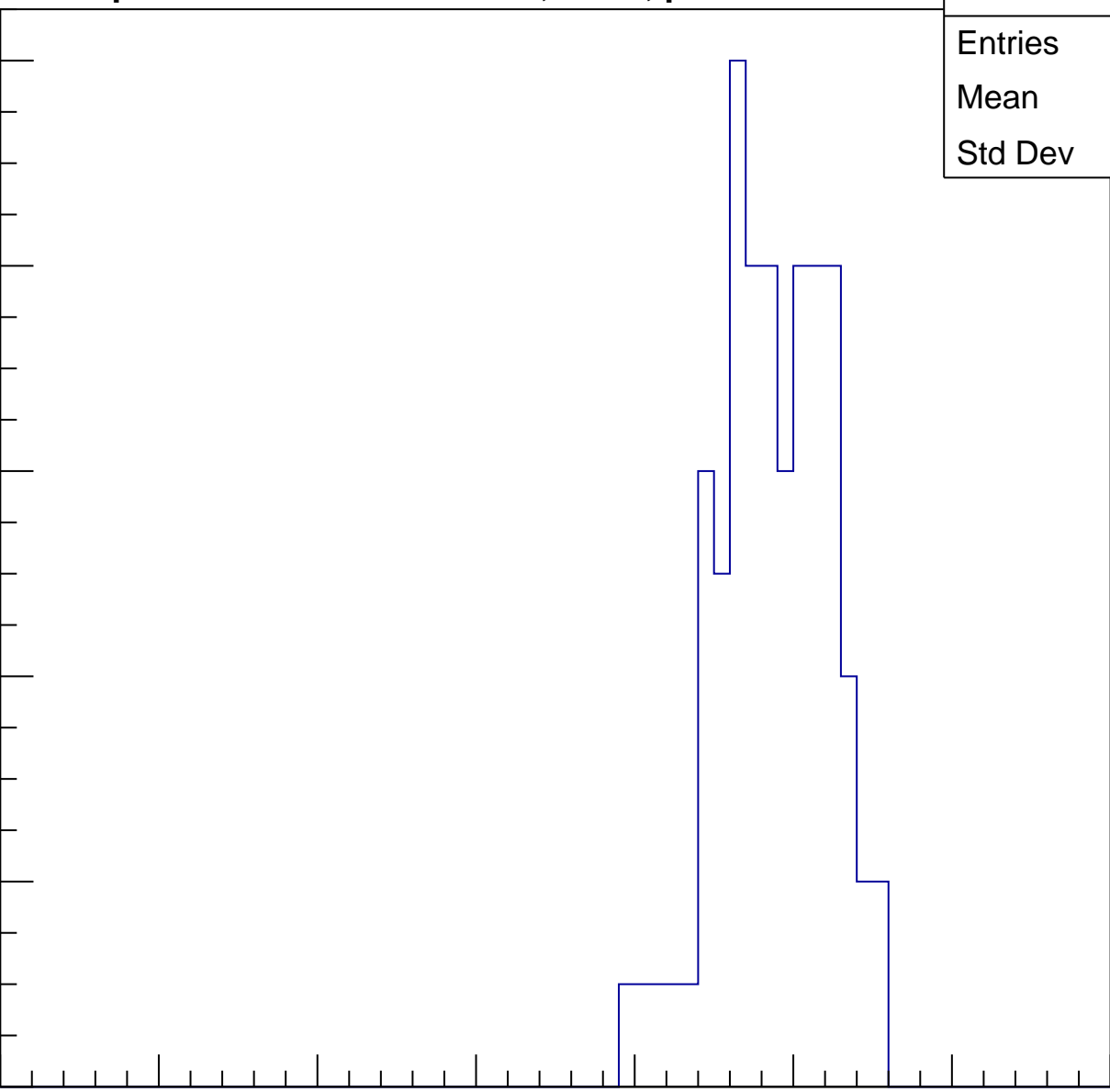
Entries	80
Mean	48.27
Std Dev	3.439

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

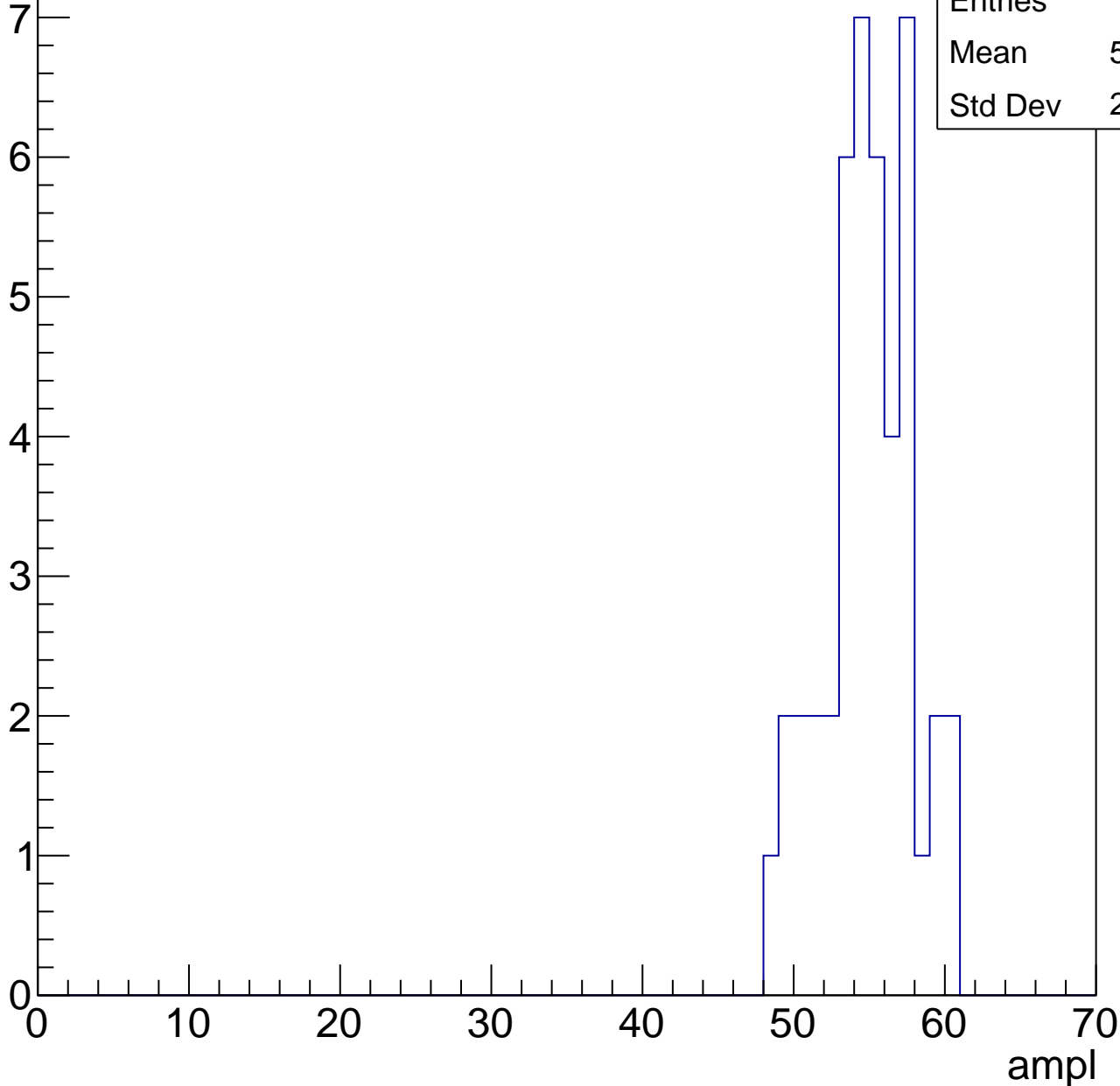


# B0L001S, U6-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	44
Mean	54.48
Std Dev	2.872



# B0L001S, U6-ch90, adc5

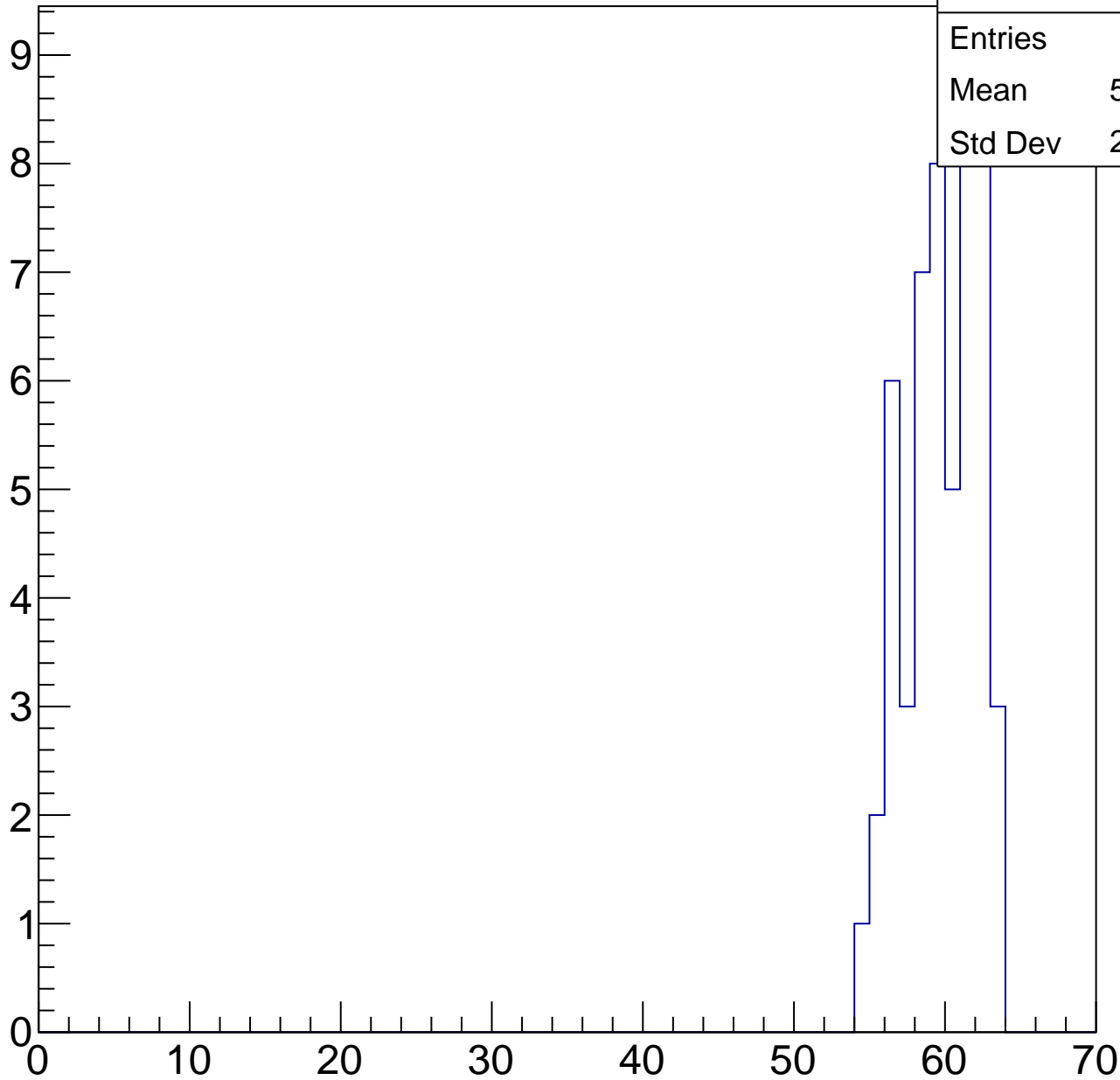
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	53
Mean	59.34
Std Dev	2.355

ampl

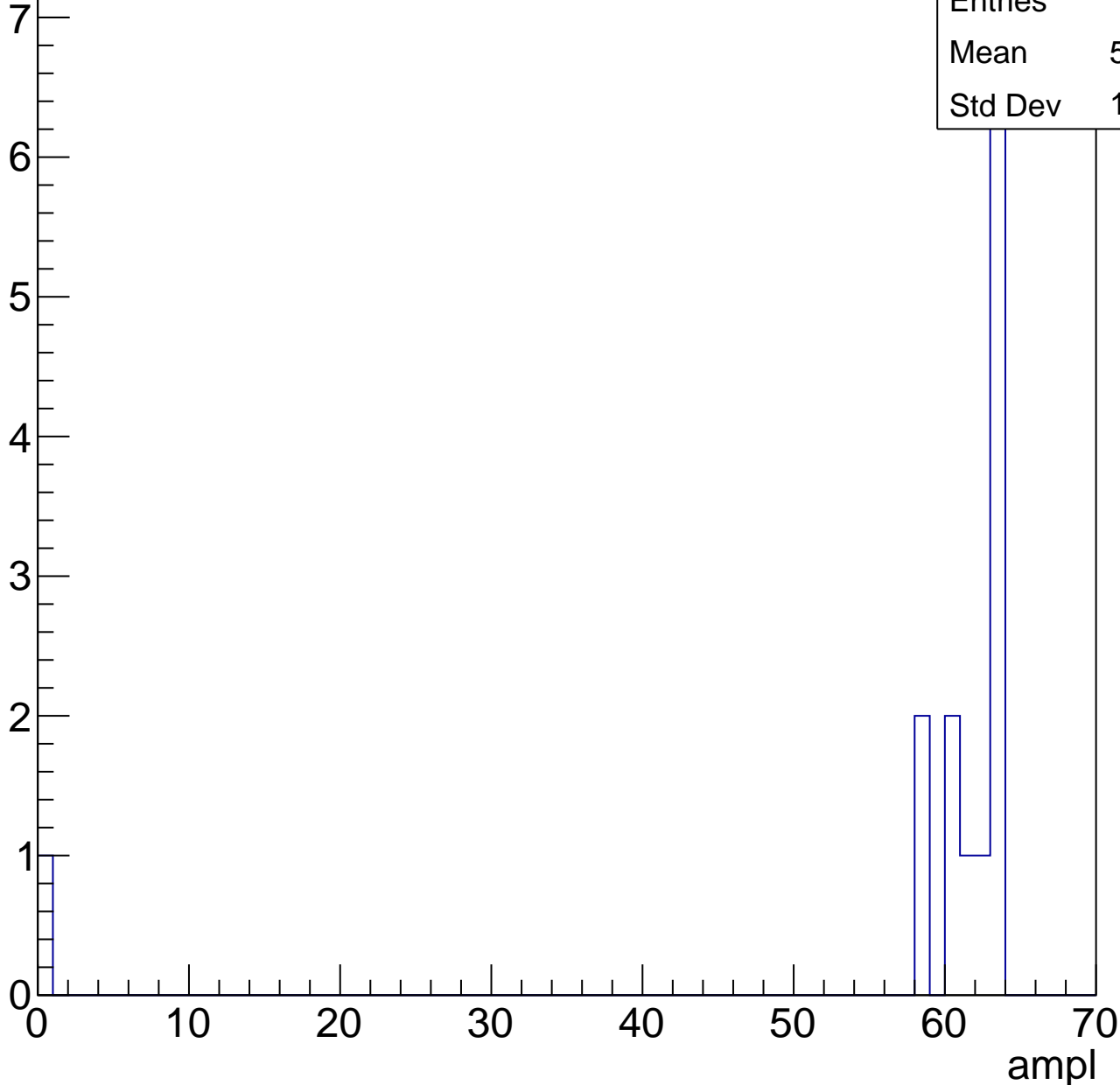


# B0L001S, U6-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	14
Mean	57.14
Std Dev	15.95

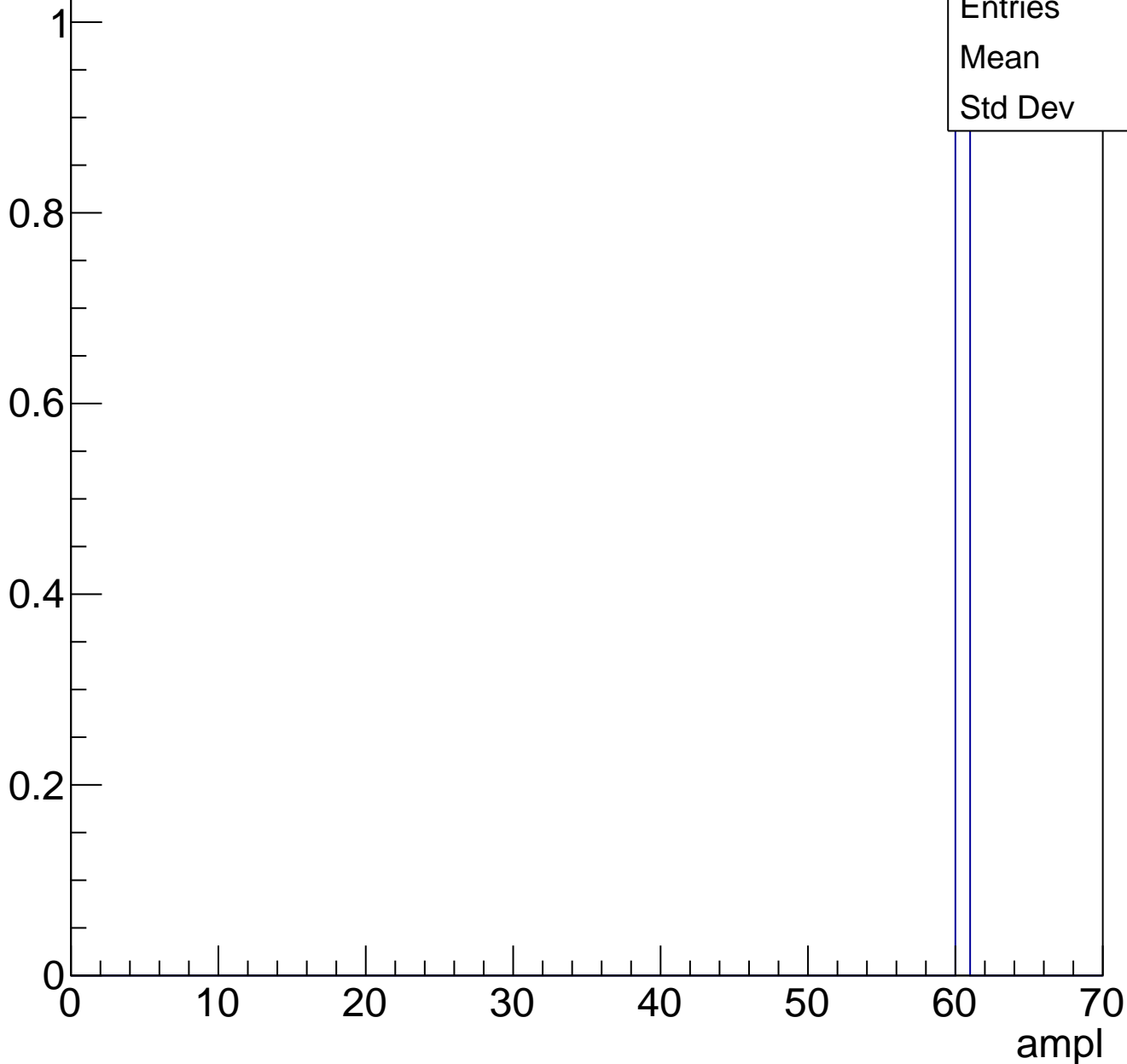




# B0L001S, U6-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch91, adc0

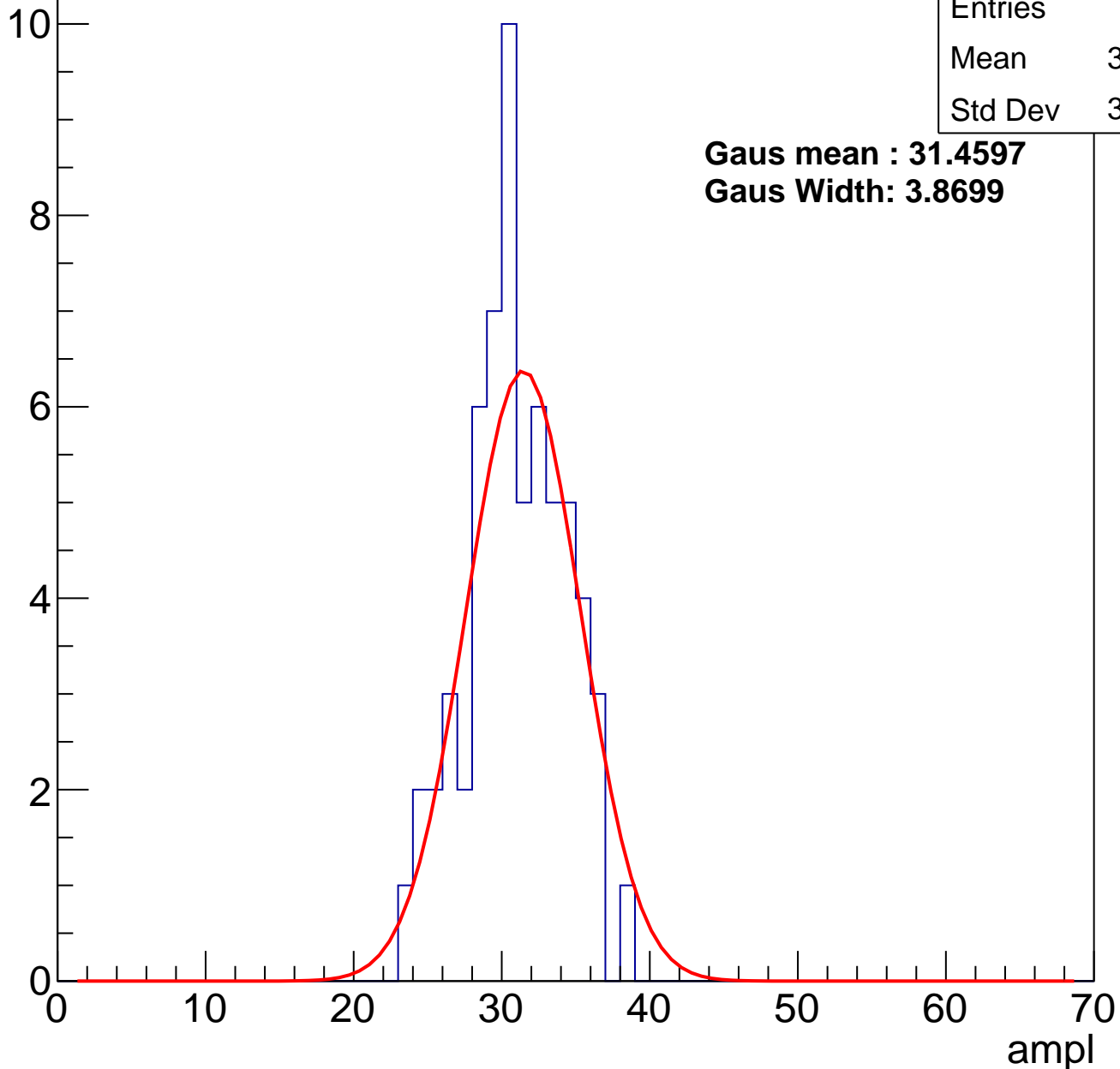
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	62
Mean	30.52
Std Dev	3.306

**Gaus mean : 31.4597**

**Gaus Width: 3.8699**

Entry



# B0L001S, U6-ch91, adc1

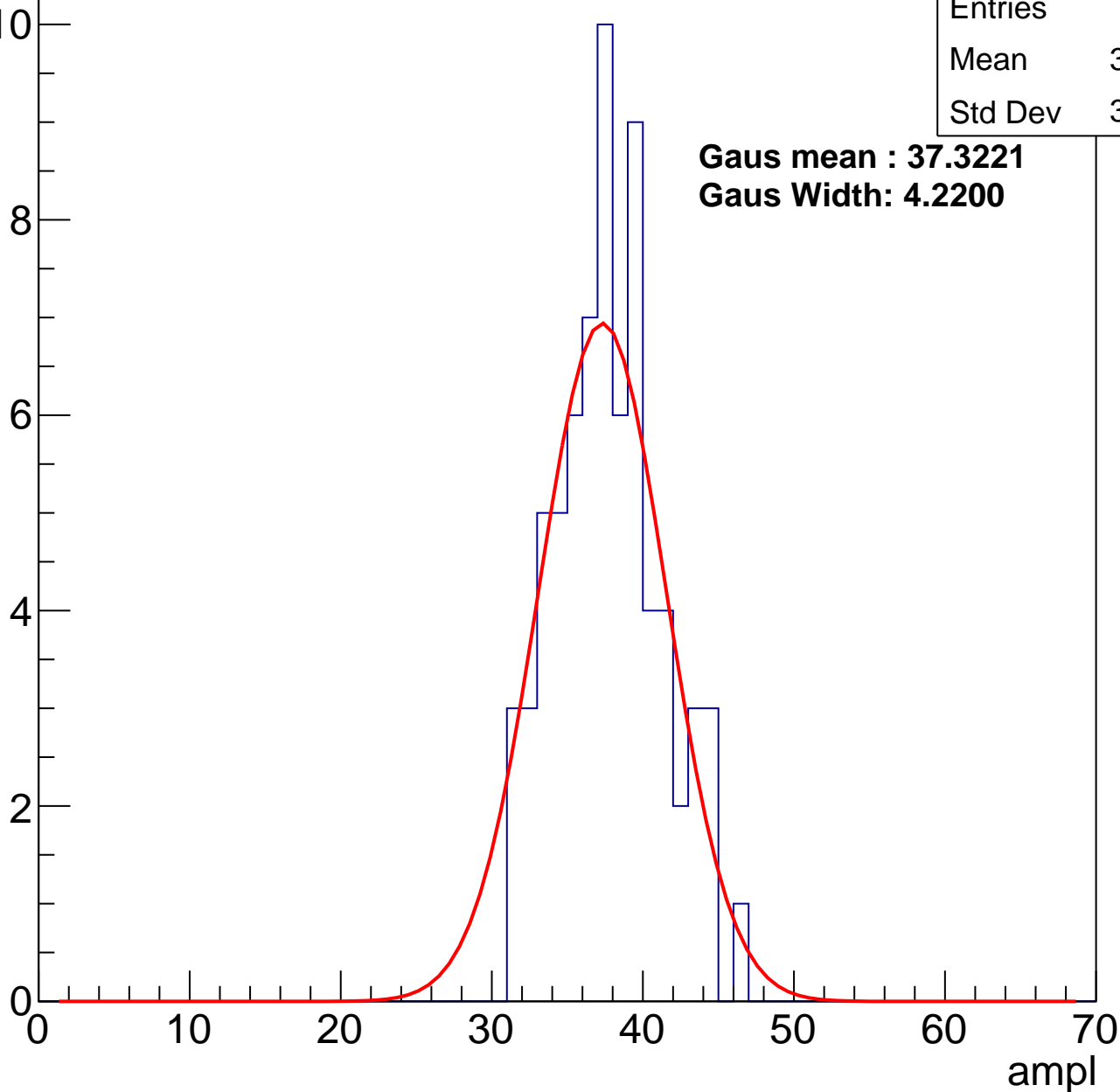
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	37.32
Std Dev	3.479

**Gaus mean : 37.3221**

**Gaus Width: 4.2200**



# B0L001S, U6-ch91, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	77
Mean	44.49
Std Dev	3.337

**Gaus mean : 45.1769**

**Gaus Width: 3.5416**

Entry

10

8

6

4

2

0

0

10

20

30

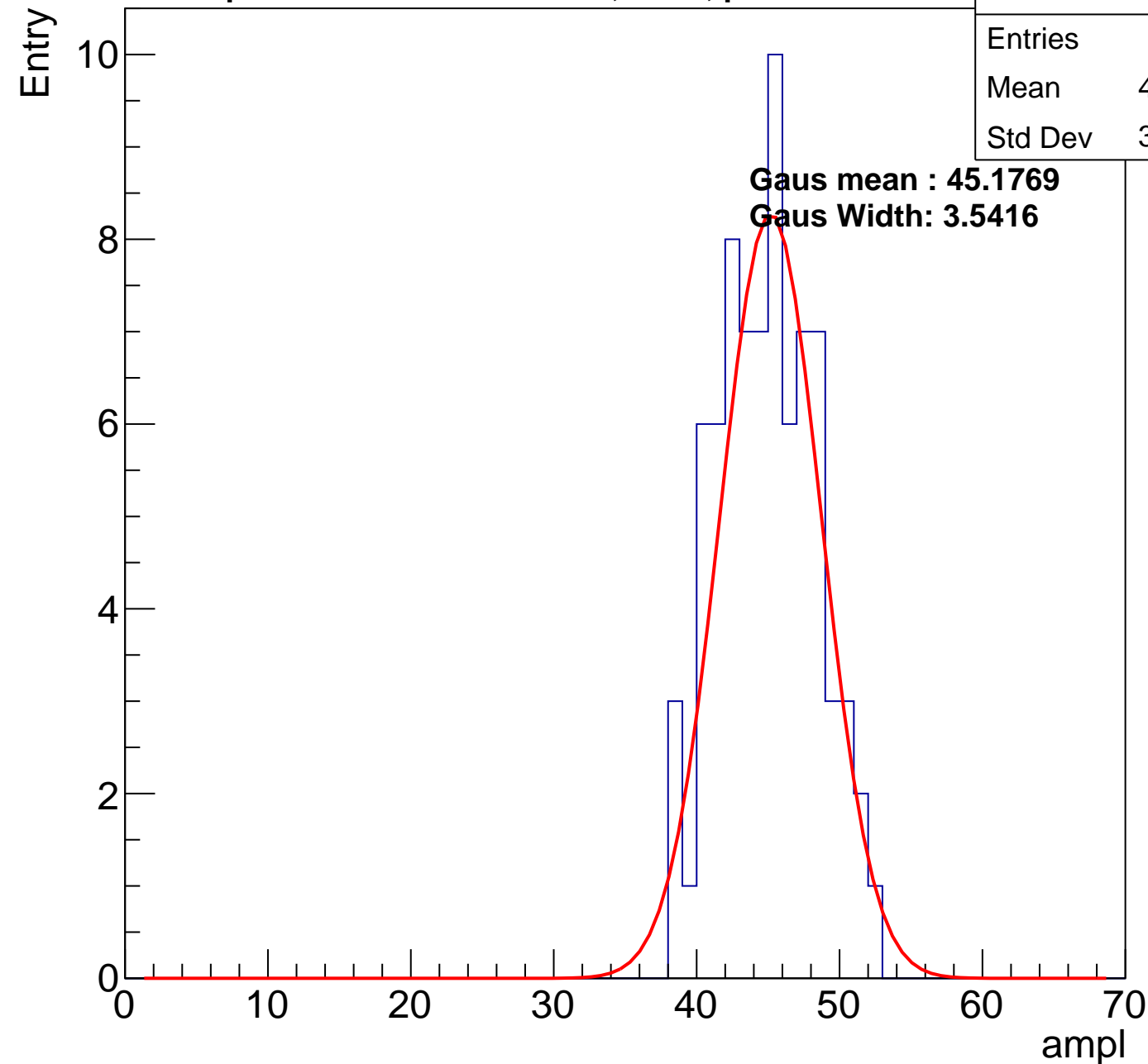
40

50

60

70

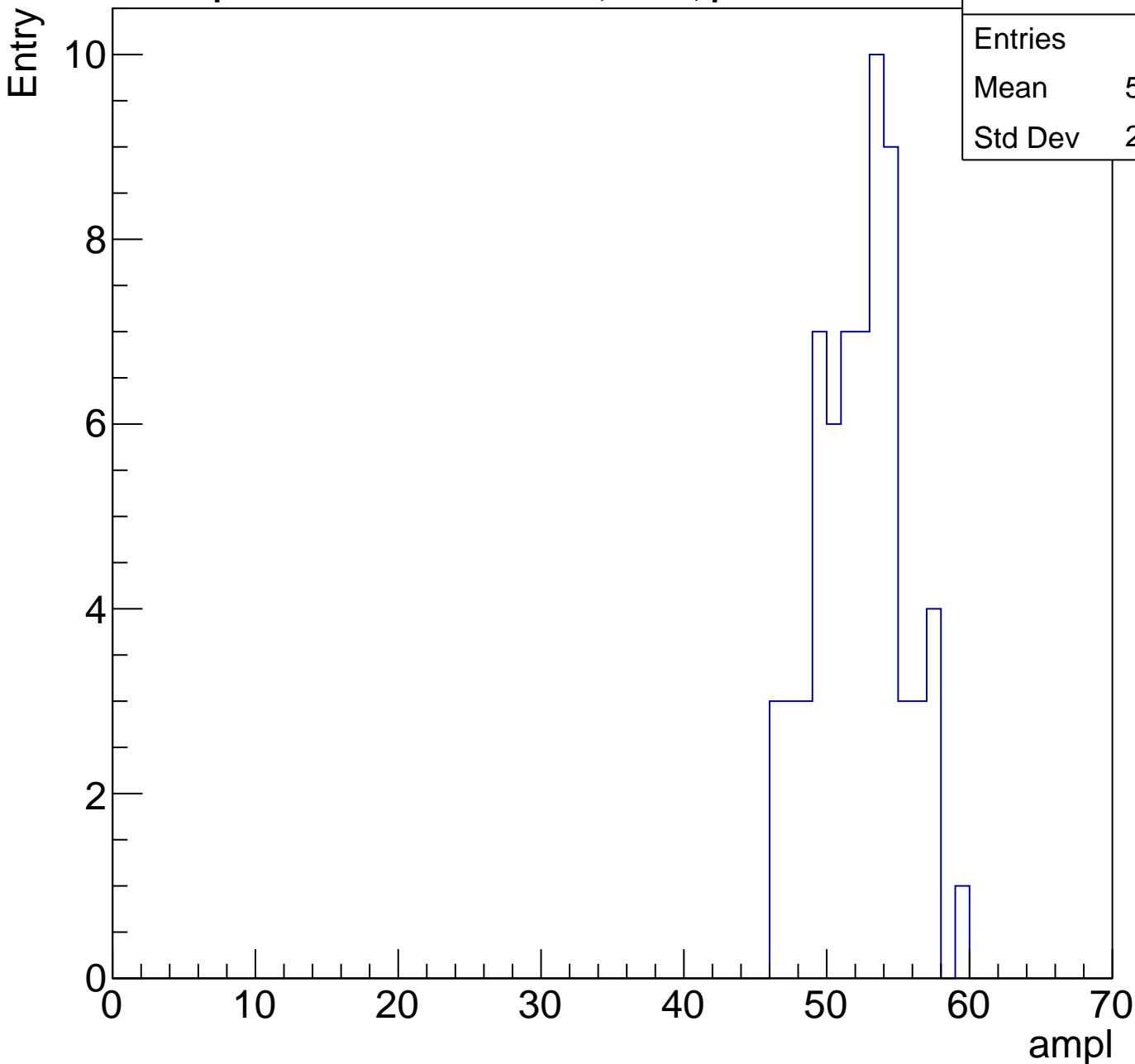
ampl



# B0L001S, U6-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	66
Mean	51.86
Std Dev	2.999

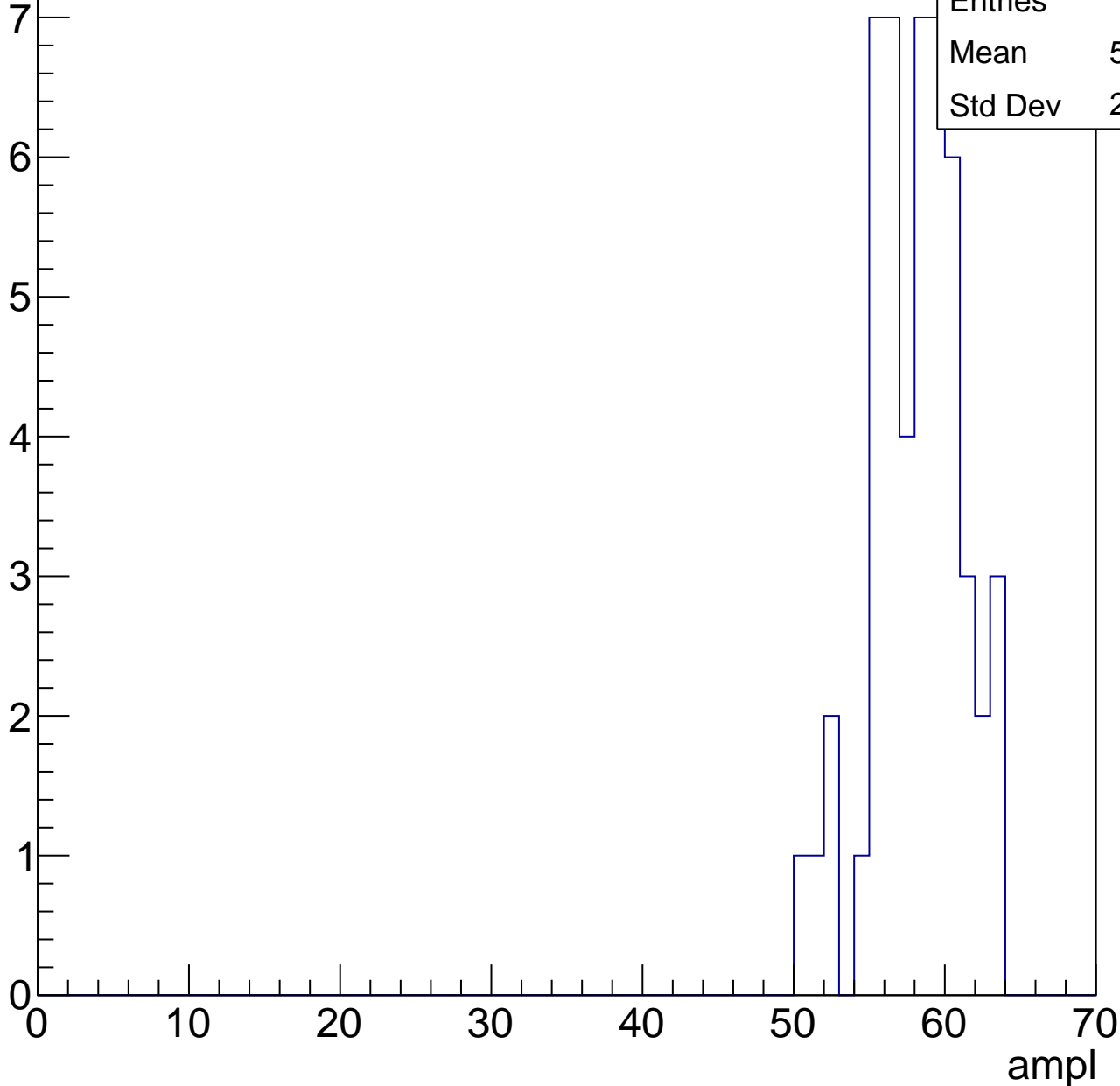


# B0L001S, U6-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	57.63
Std Dev	2.983

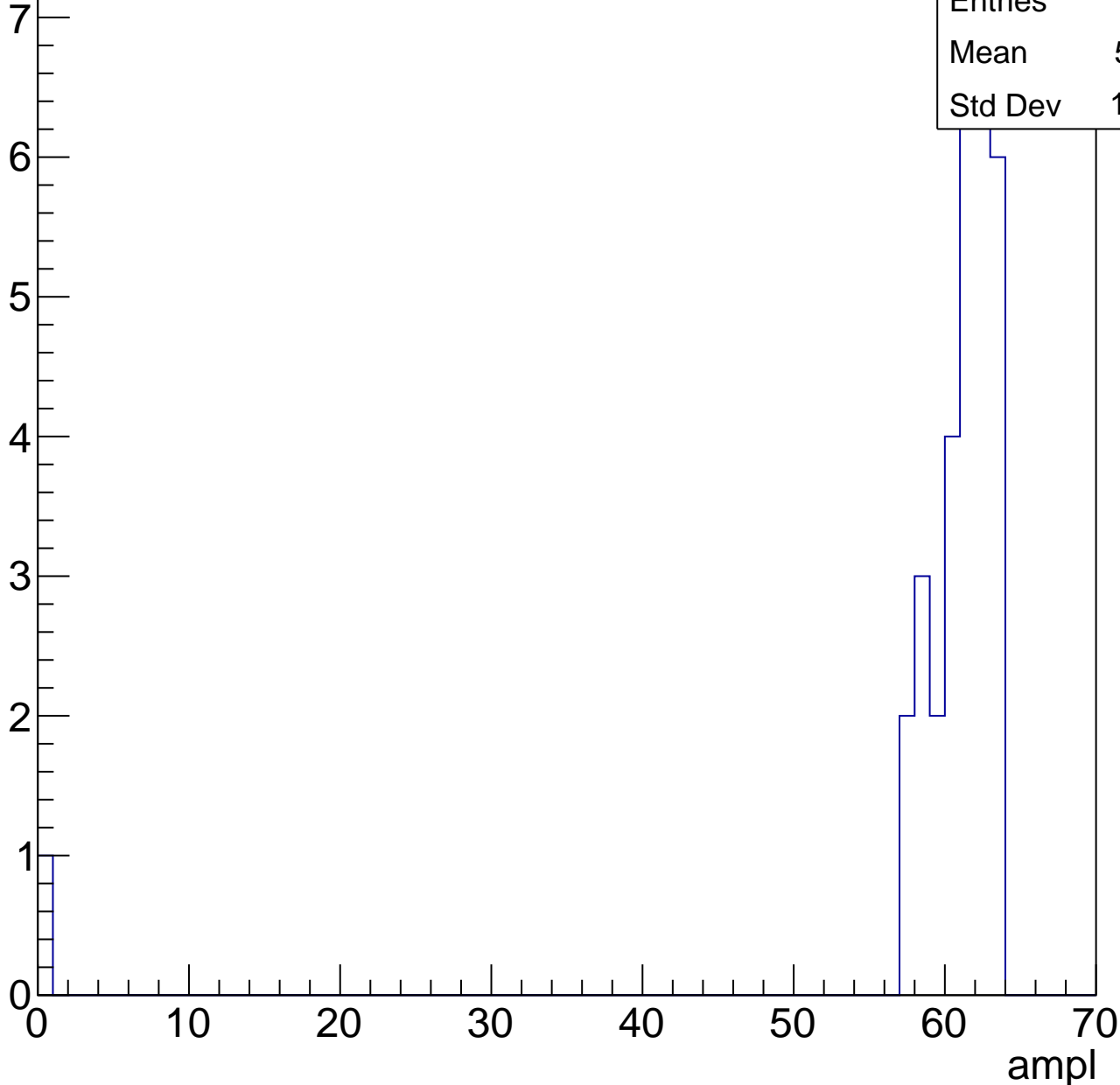


# B0L001S, U6-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	32
Mean	58.91
Std Dev	10.73



# B0L001S, U6-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch92, adc0

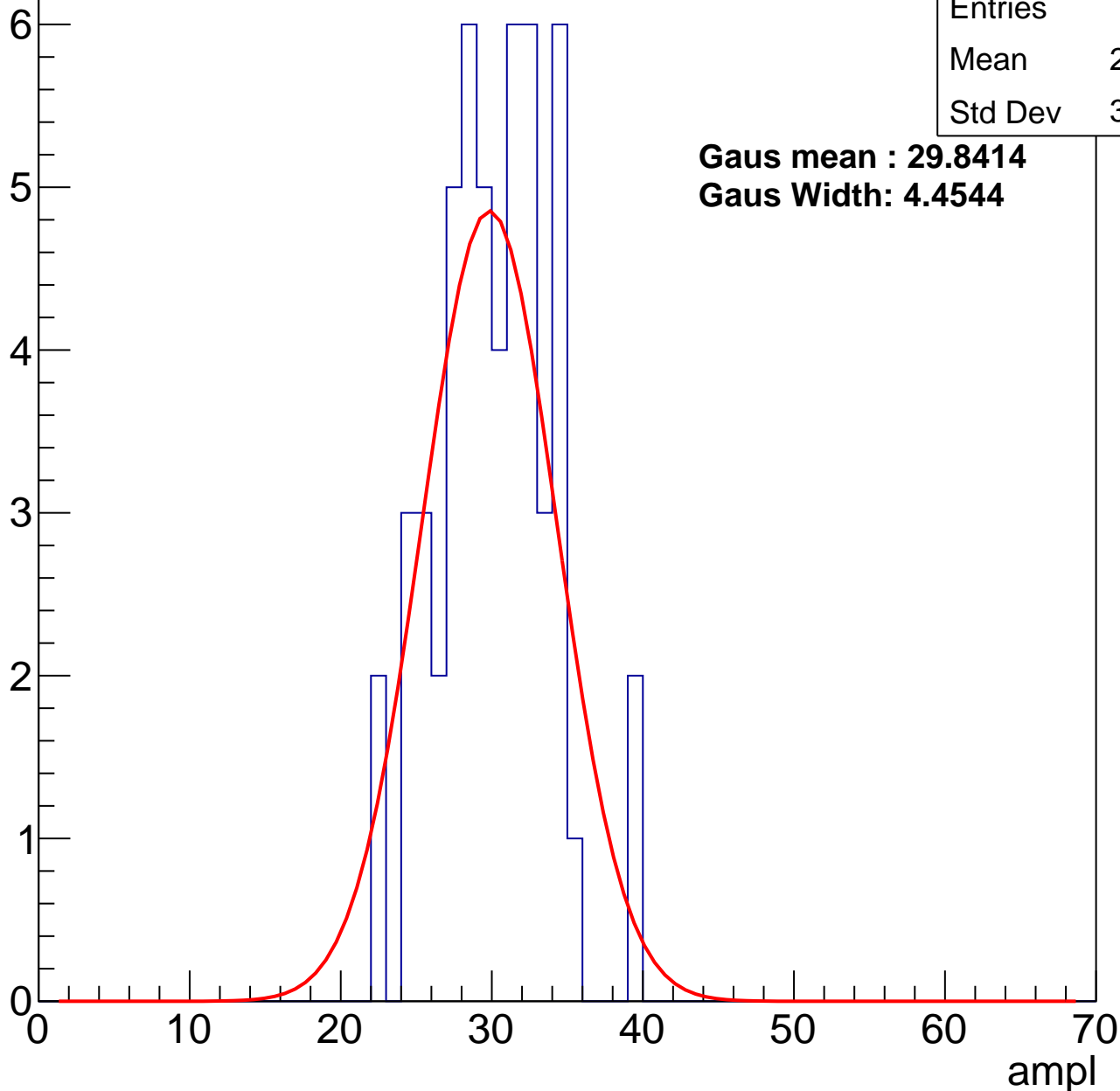
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	29.72
Std Dev	3.734

**Gaus mean : 29.8414**

**Gaus Width: 4.4544**



# B0L001S, U6-ch92, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	84
Mean	36.04
Std Dev	3.743

**Gaus mean : 36.5179**

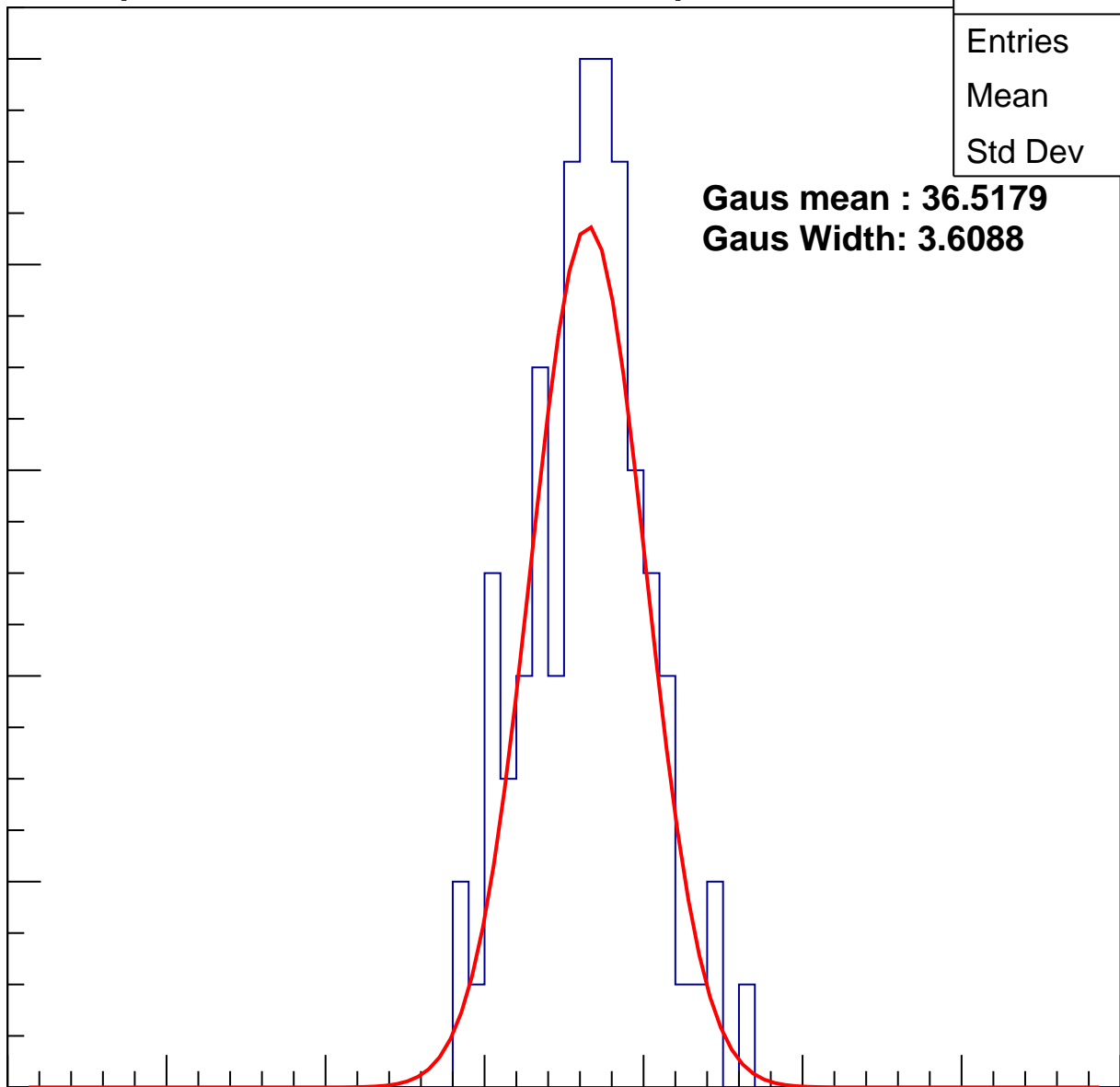
**Gaus Width: 3.6088**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U6-ch92, adc2

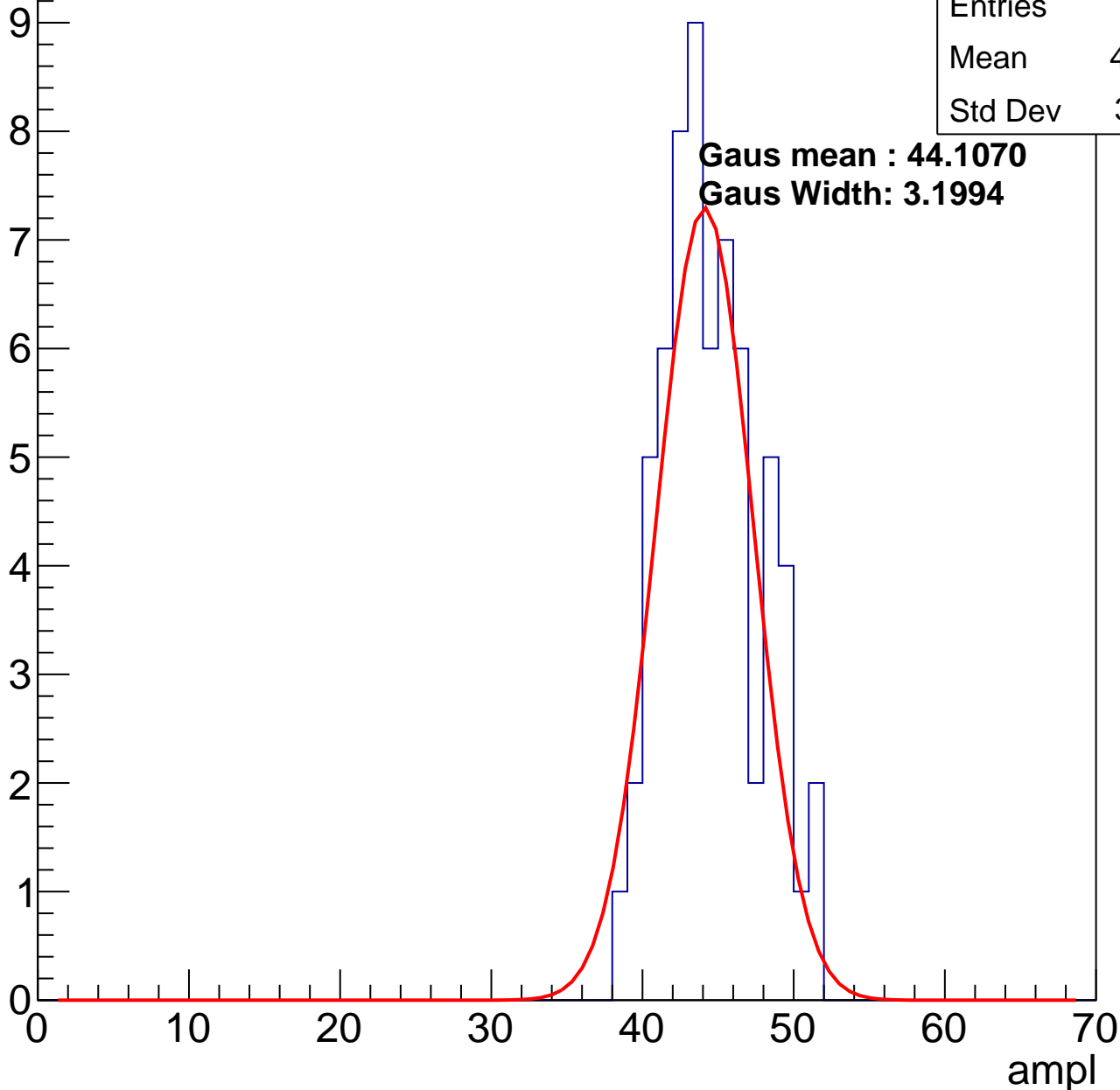
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	44.09
Std Dev	3.121

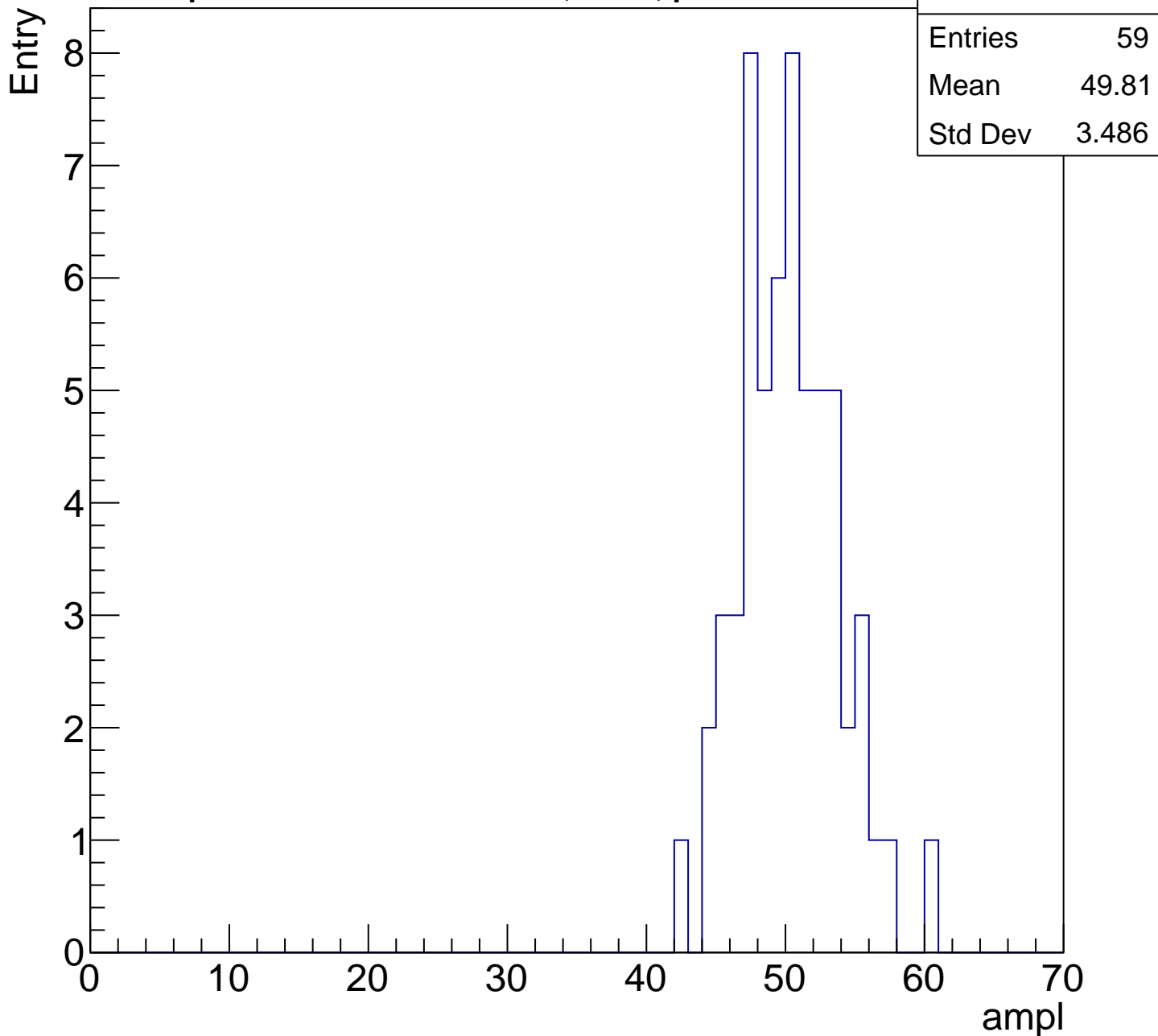
**Gaus mean : 44.1070**

**Gaus Width: 3.1994**



# B0L001S, U6-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

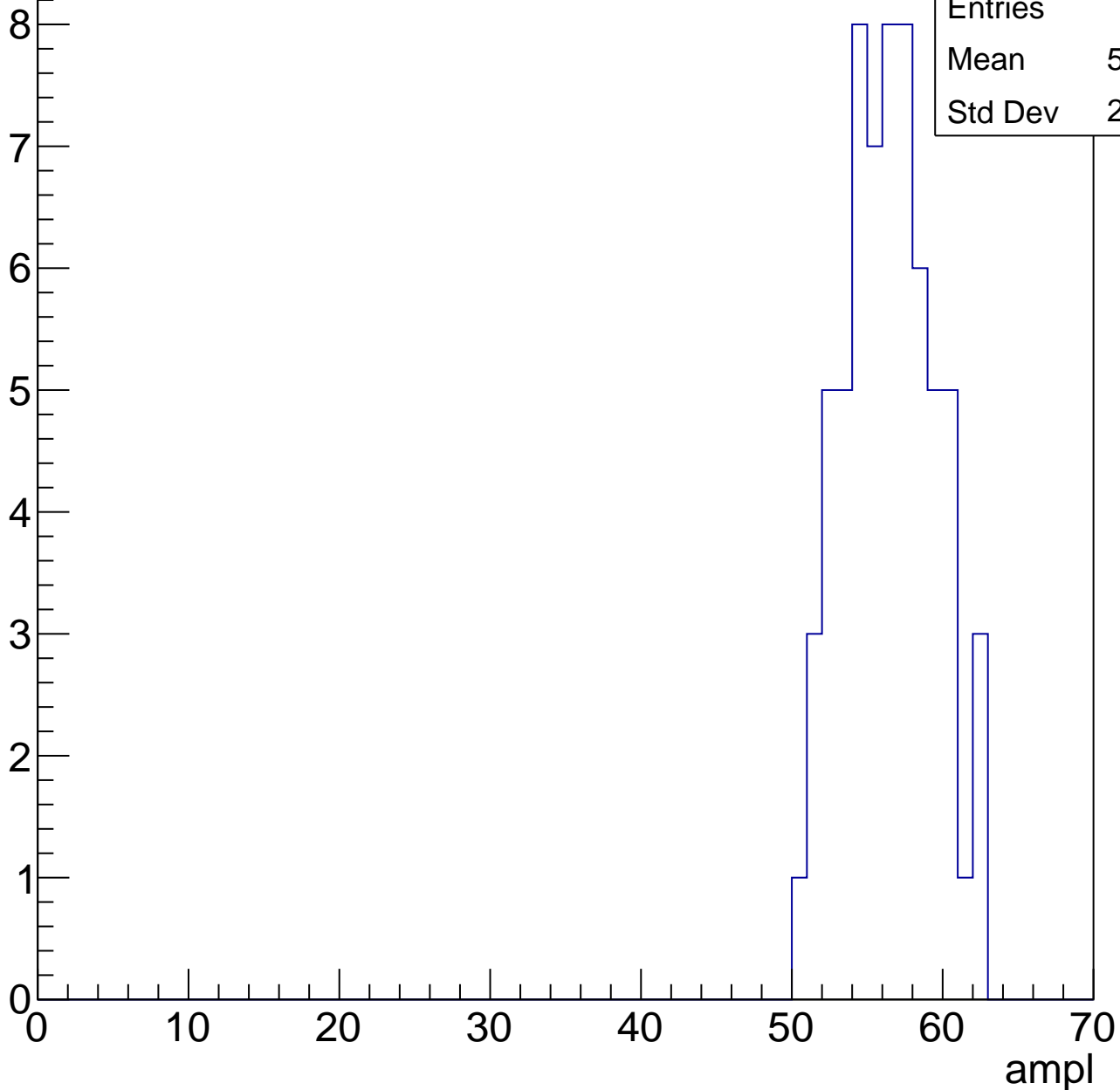


# B0L001S, U6-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	55.98
Std Dev	2.948

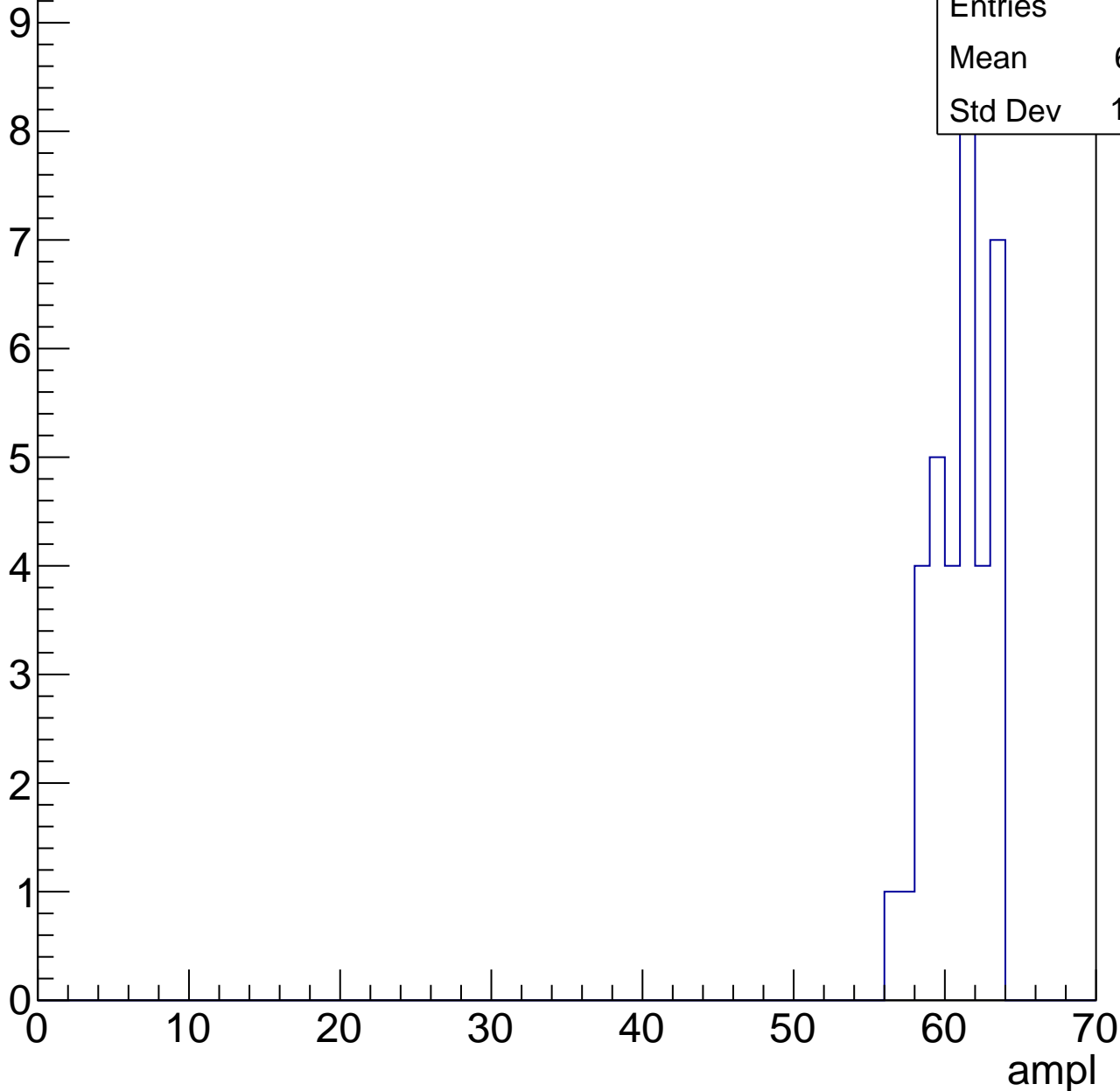


# B0L001S, U6-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

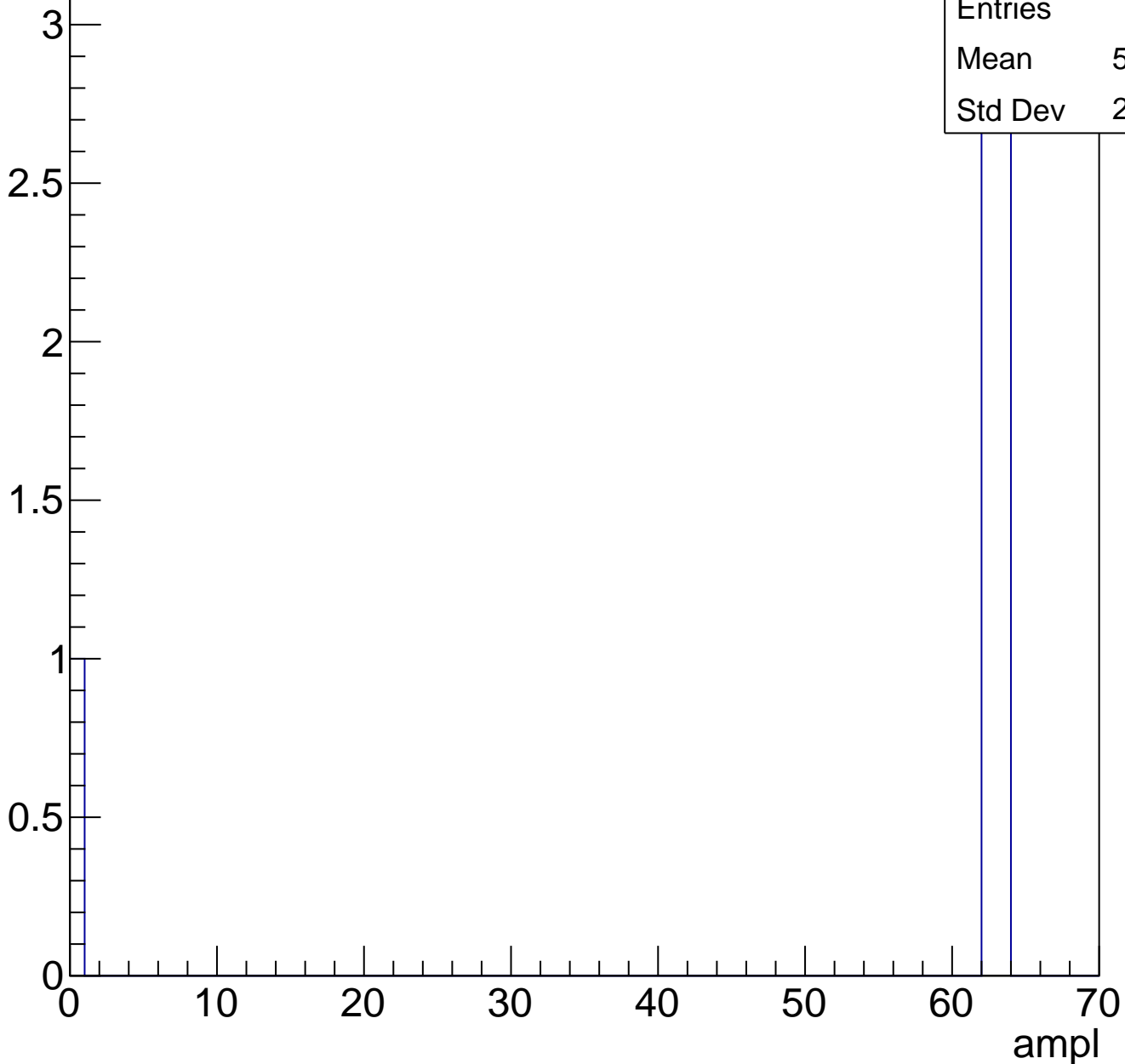
Entries	35
Mean	60.51
Std Dev	1.888



# B0L001S, U6-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U6-ch93, adc0

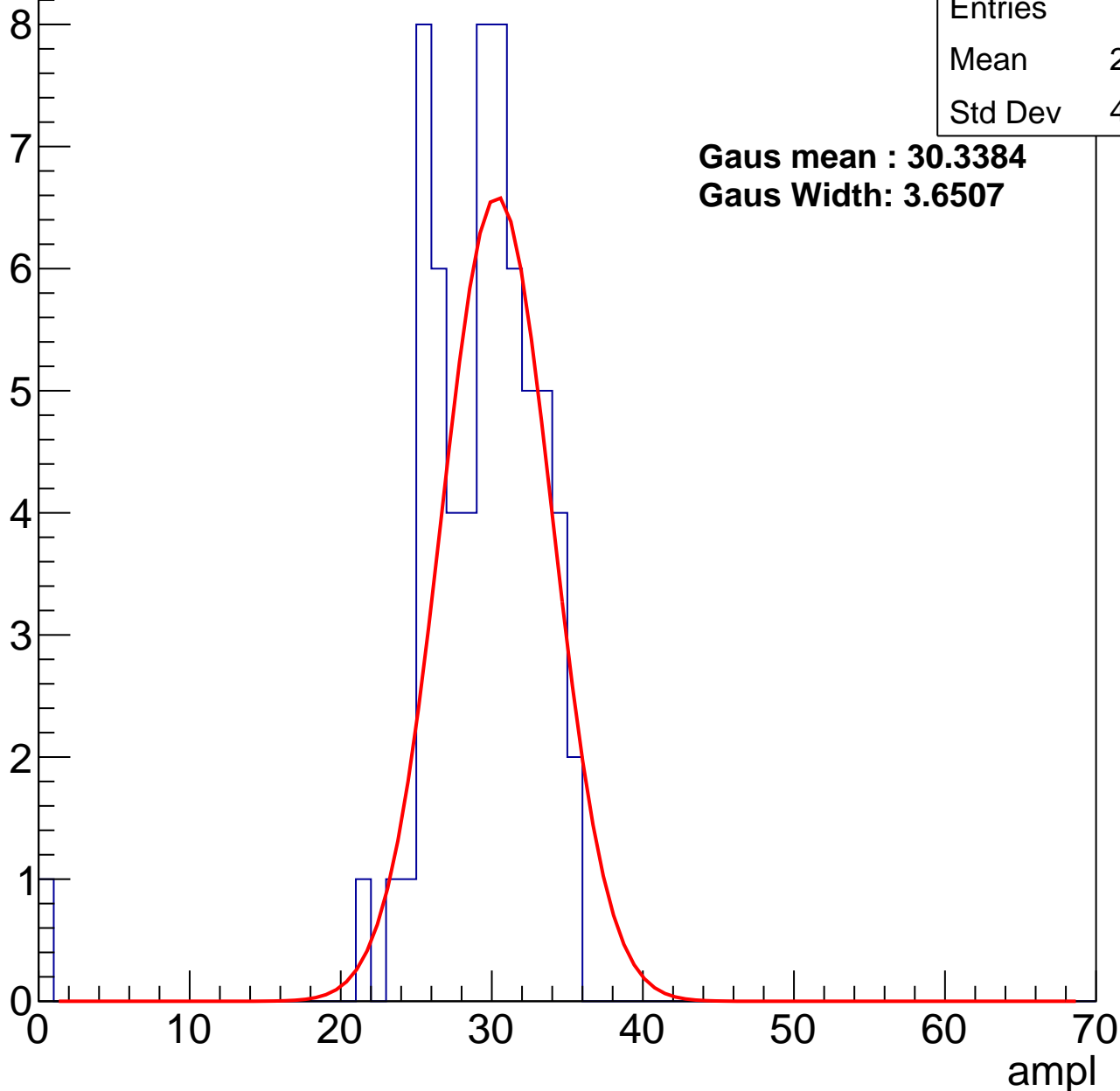
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	28.64
Std Dev	4.823

**Gaus mean : 30.3384**

**Gaus Width: 3.6507**



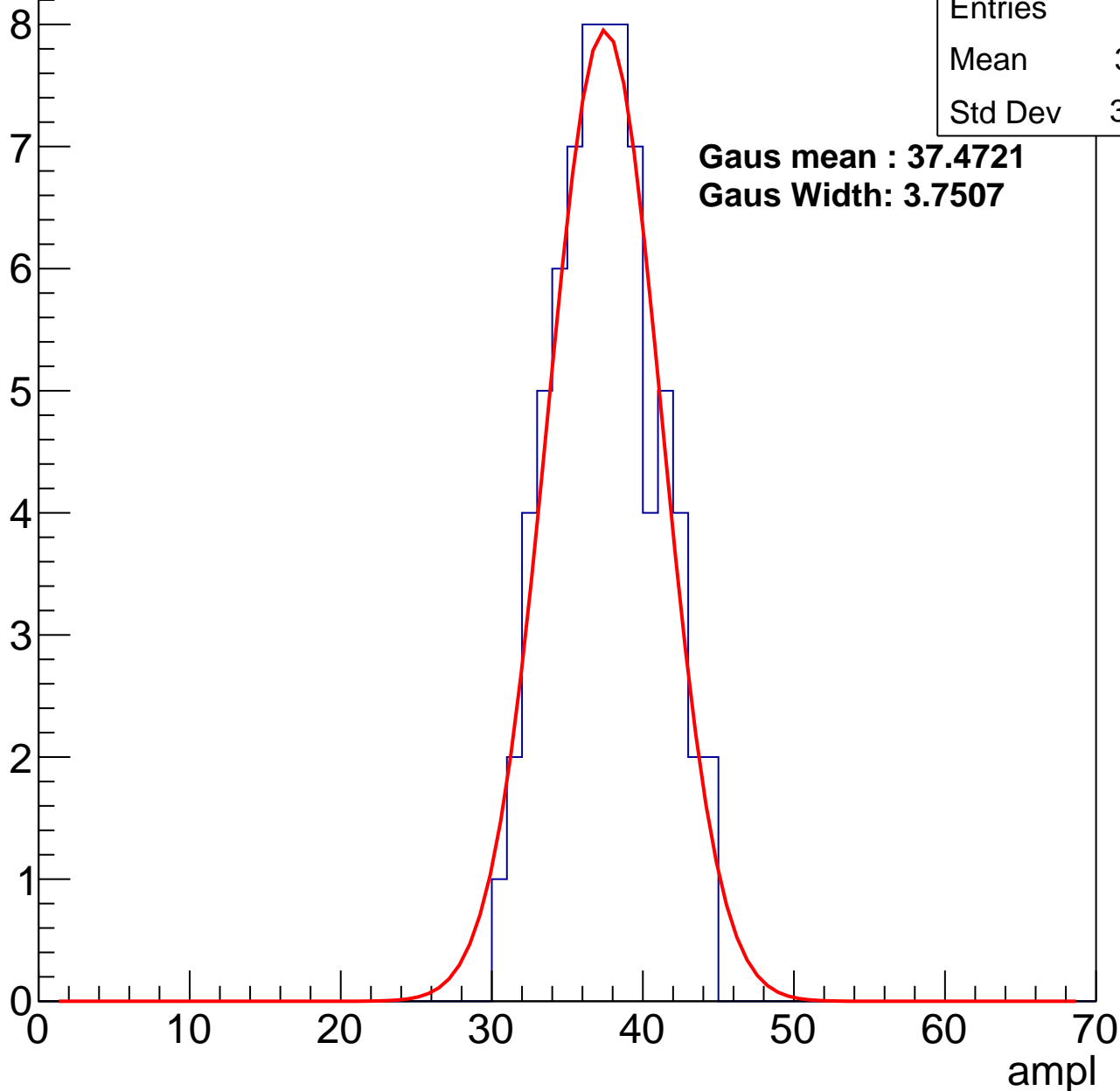
# B0L001S, U6-ch93, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	37.01
Std Dev	3.337

**Gaus mean : 37.4721**  
**Gaus Width: 3.7507**



# B0L001S, U6-ch93, adc2

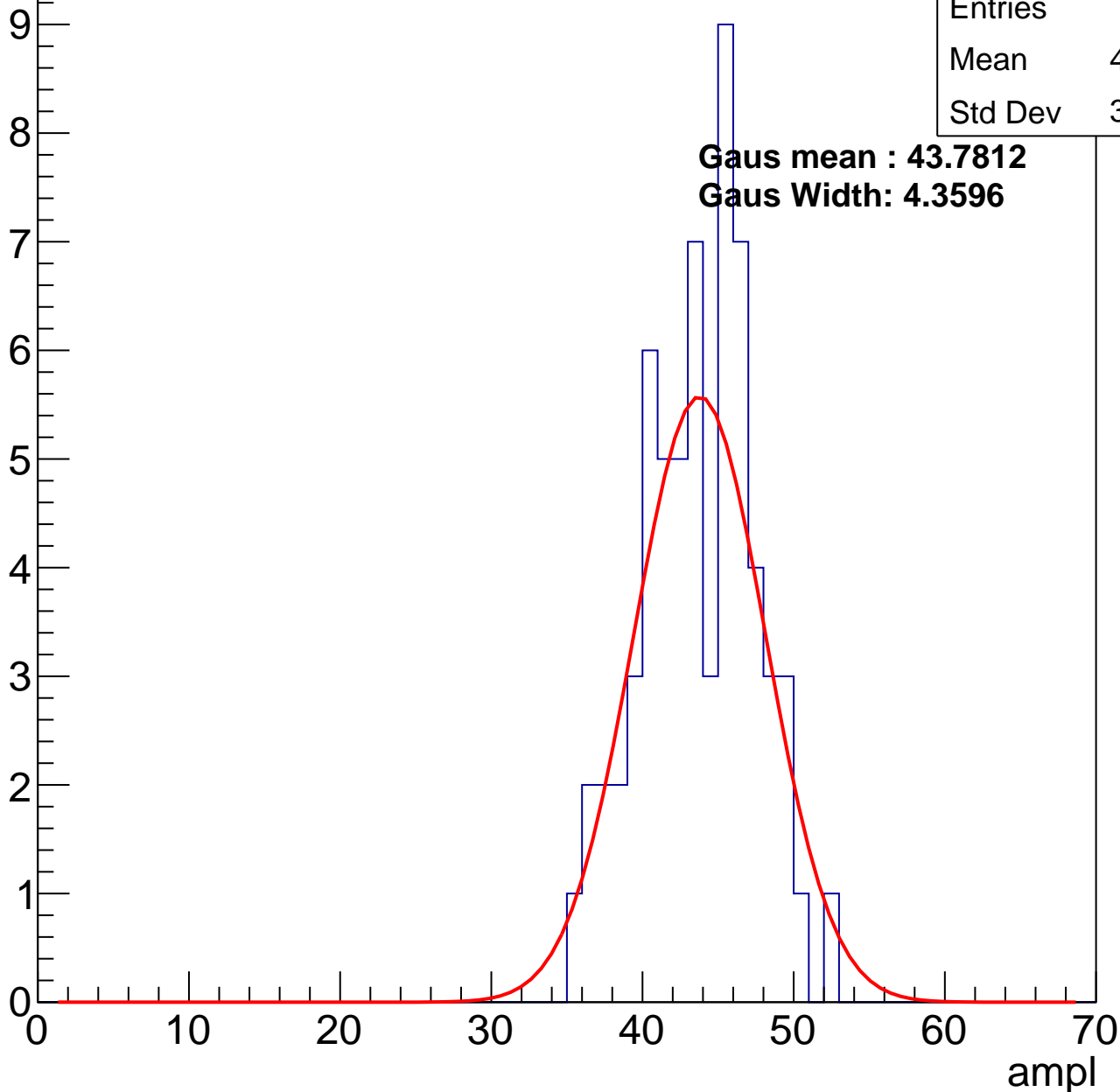
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	43.28
Std Dev	3.718

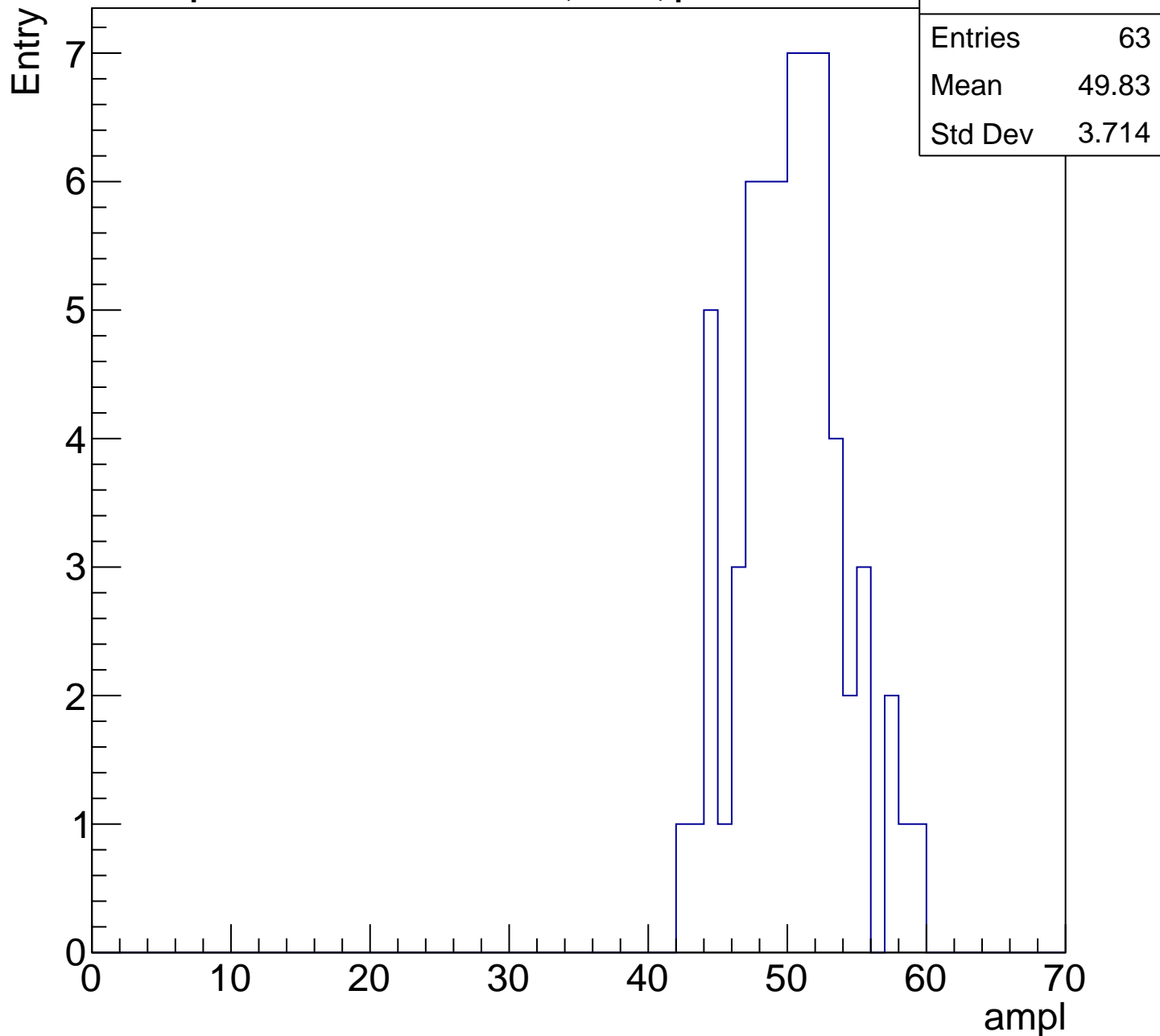
**Gaus mean : 43.7812**

**Gaus Width: 4.3596**



# B0L001S, U6-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

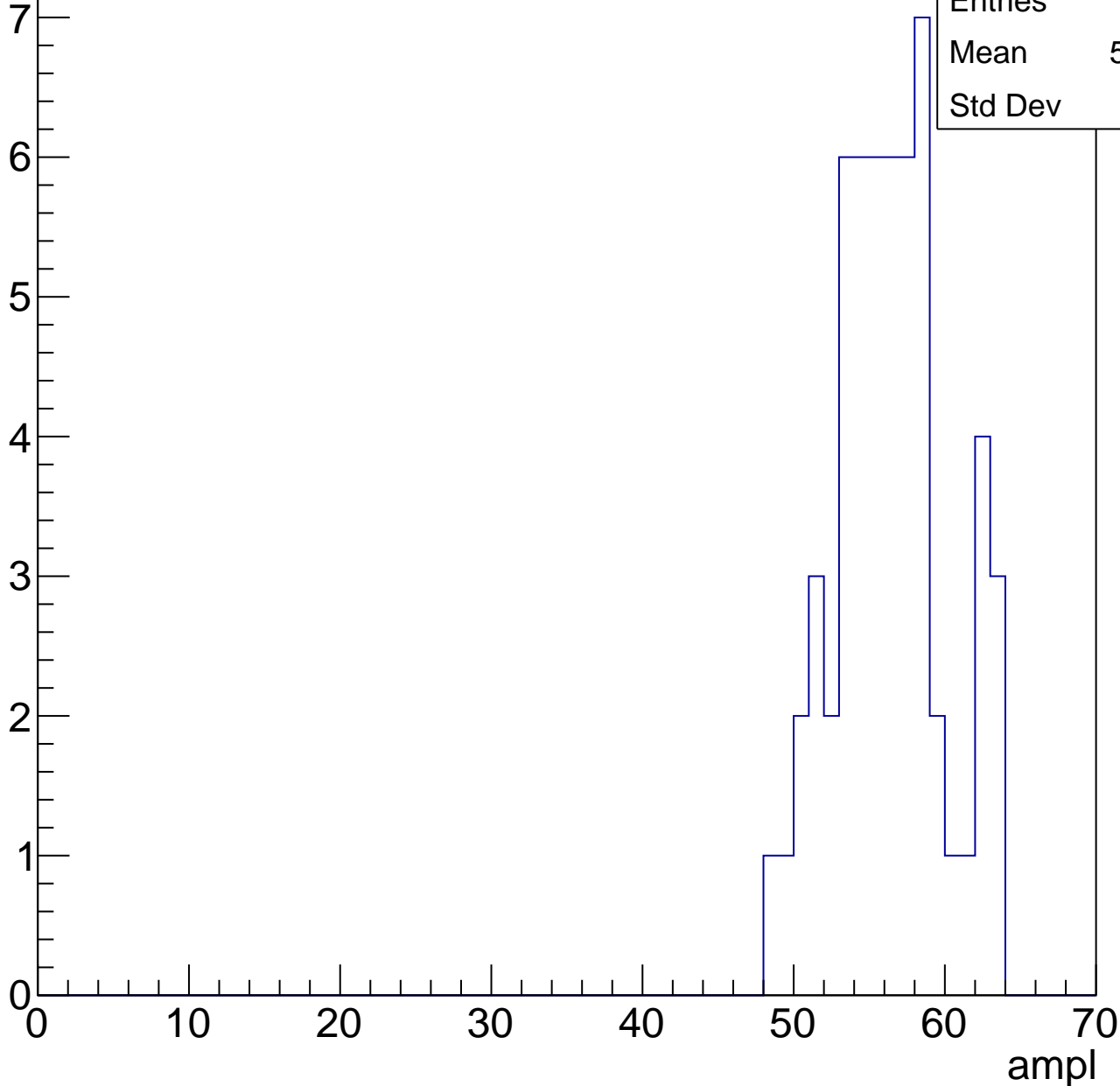


# B0L001S, U6-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	55.89
Std Dev	3.65

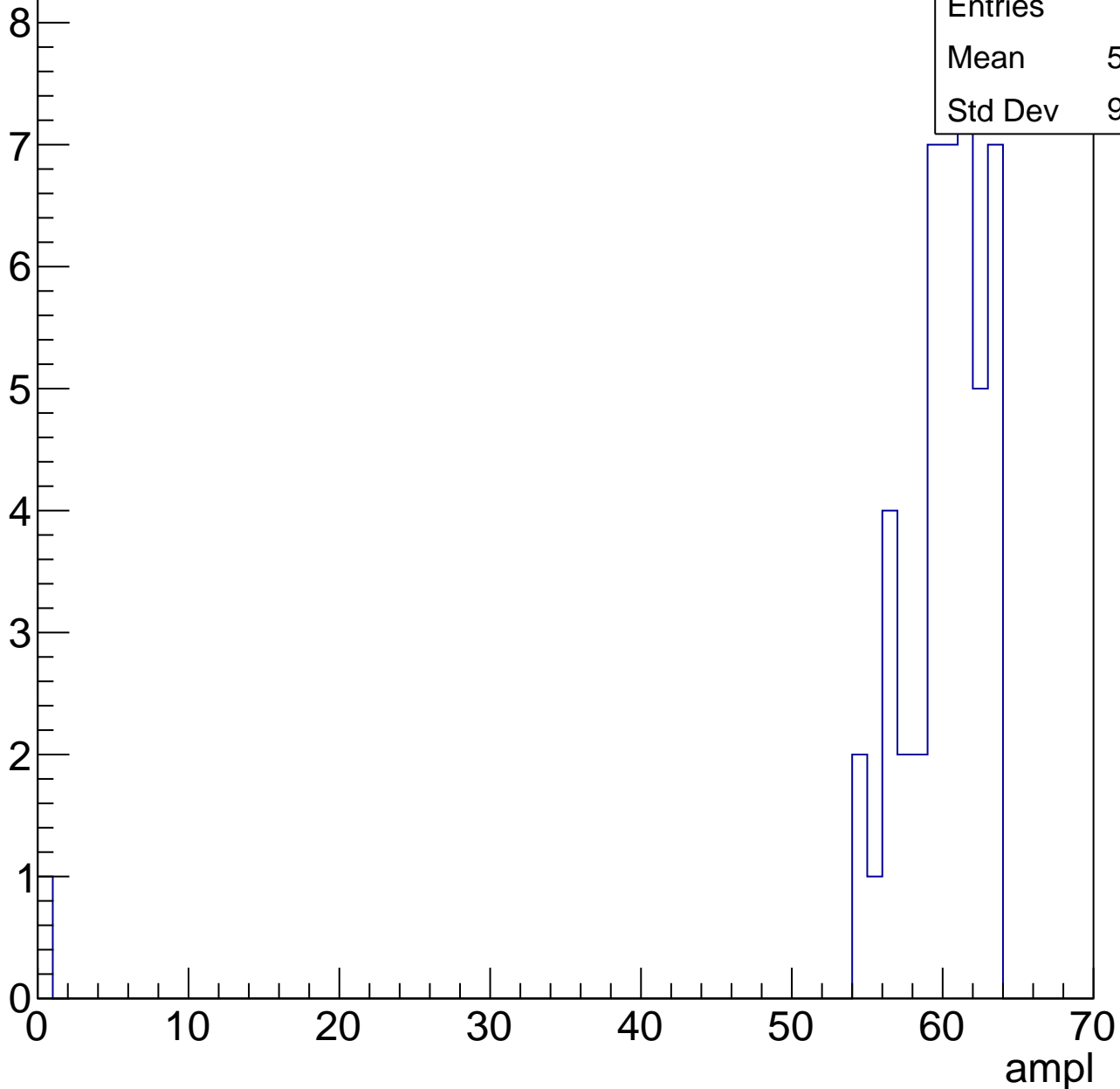


# B0L001S, U6-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	58.46
Std Dev	9.059



# B0L001S, U6-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	60.75
Std Dev	0.8292

ampl

0 10 20 30 40 50 60 70



# B0L001S, U6-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	20
Std Dev	0

ampl

# B0L001S, U6-ch94, adc0

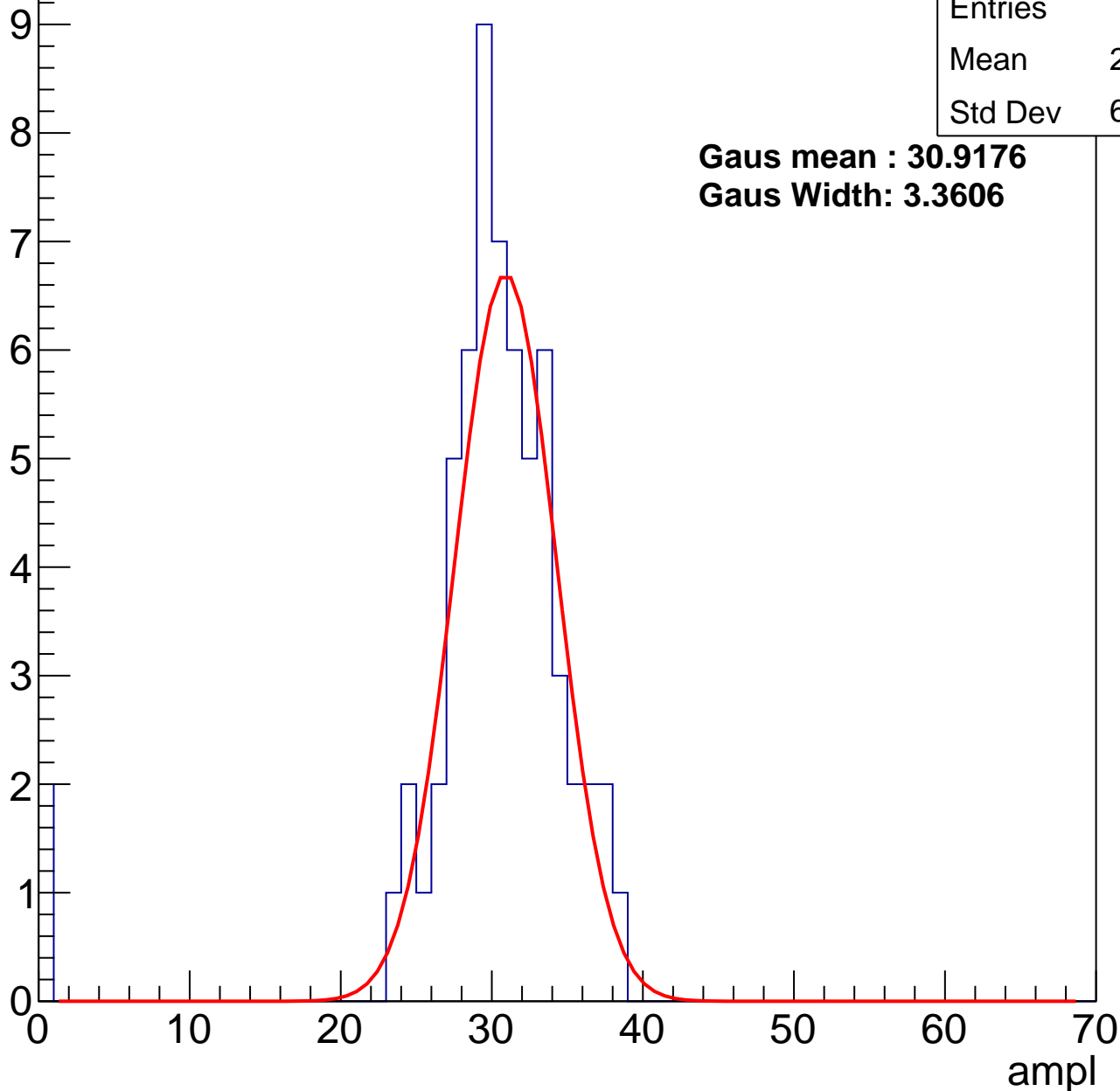
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	29.39
Std Dev	6.279

**Gaus mean : 30.9176**

**Gaus Width: 3.3606**



# B0L001S, U6-ch94, adc1

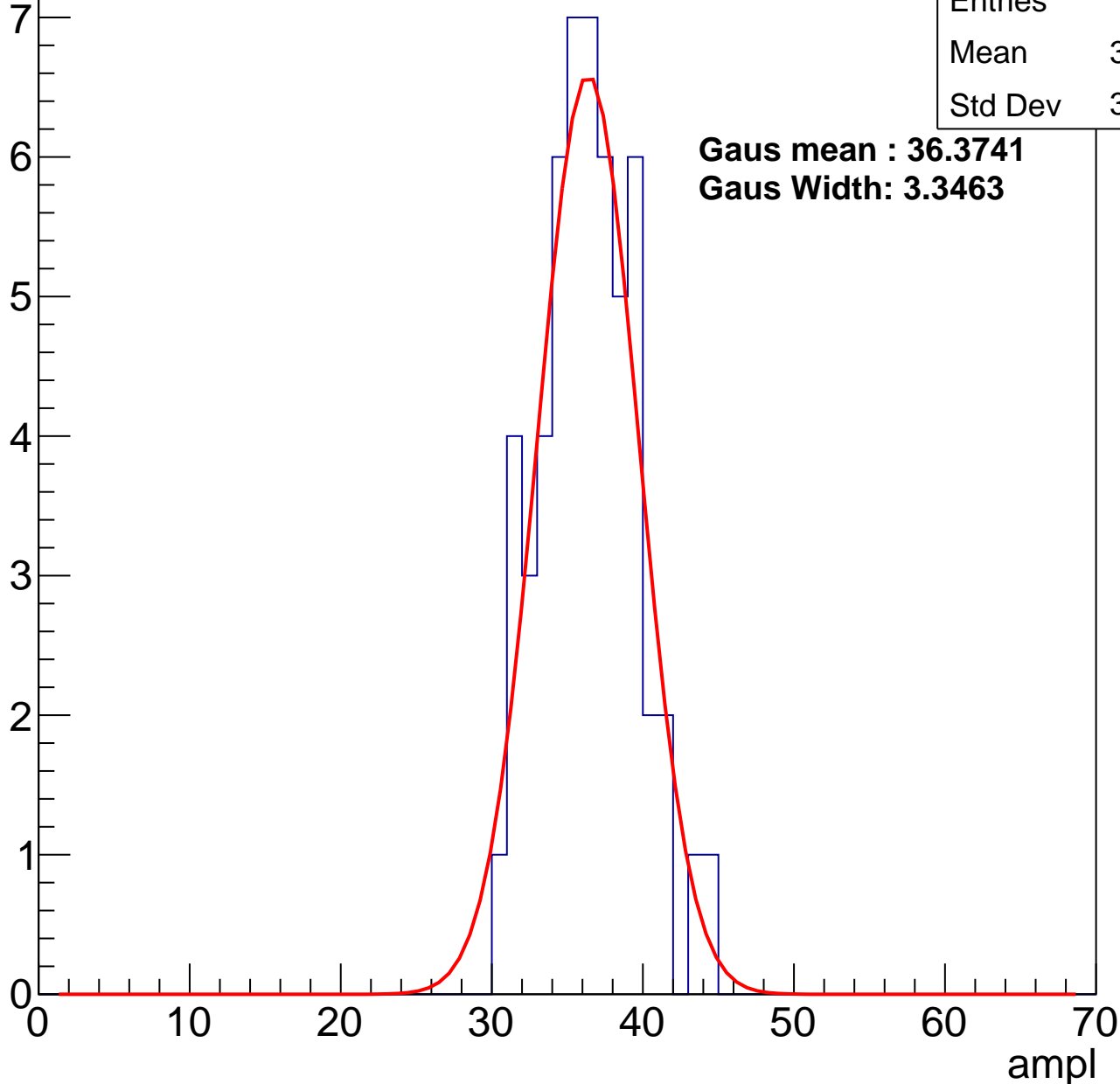
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	35.96
Std Dev	3.092

**Gaus mean : 36.3741**

**Gaus Width: 3.3463**



# B0L001S, U6-ch94, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	75
Mean	42.39
Std Dev	3.629

**Gaus mean : 42.9368**

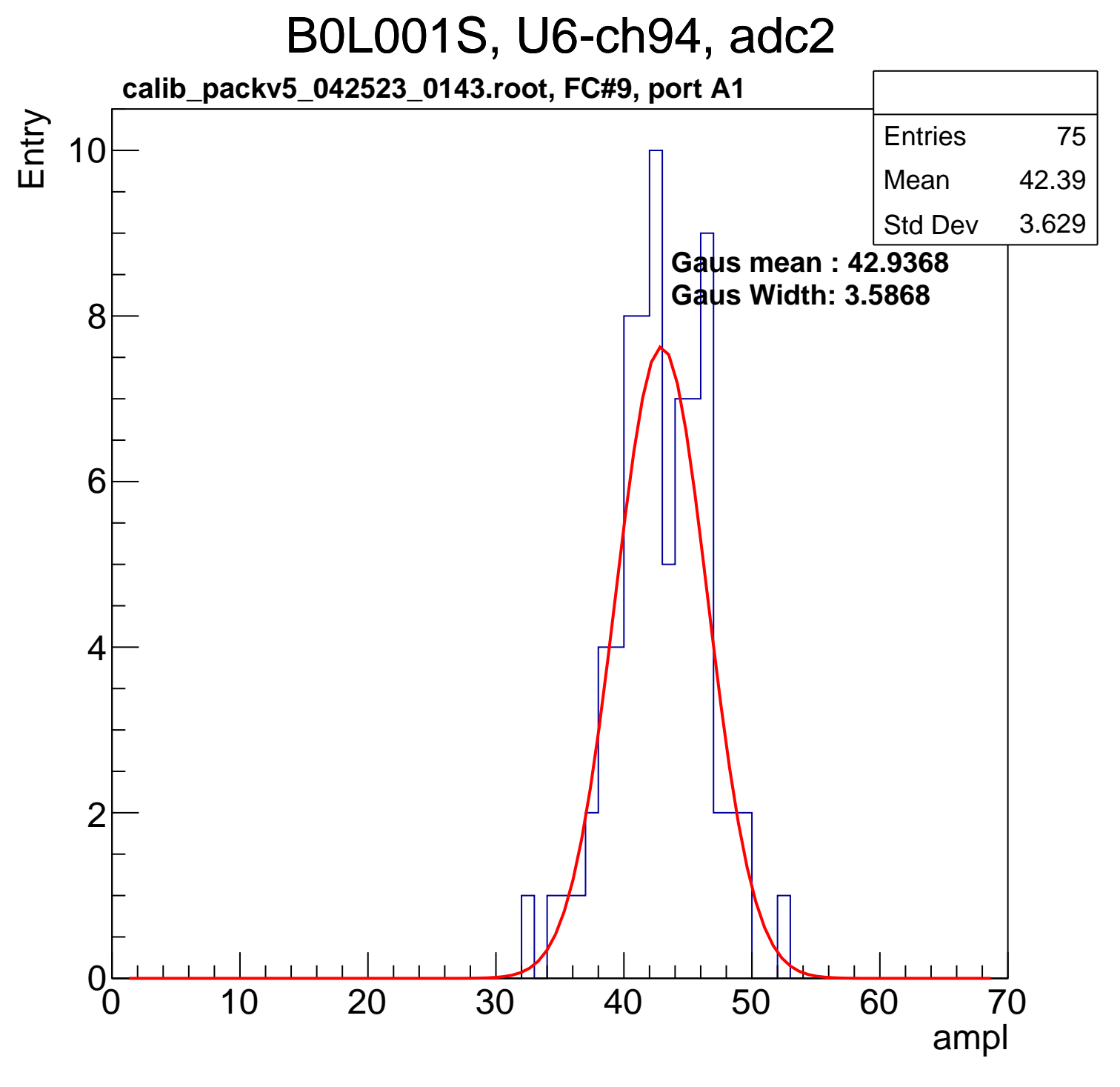
**Gaus Width: 3.5868**

Entry

10  
8  
6  
4  
2  
0

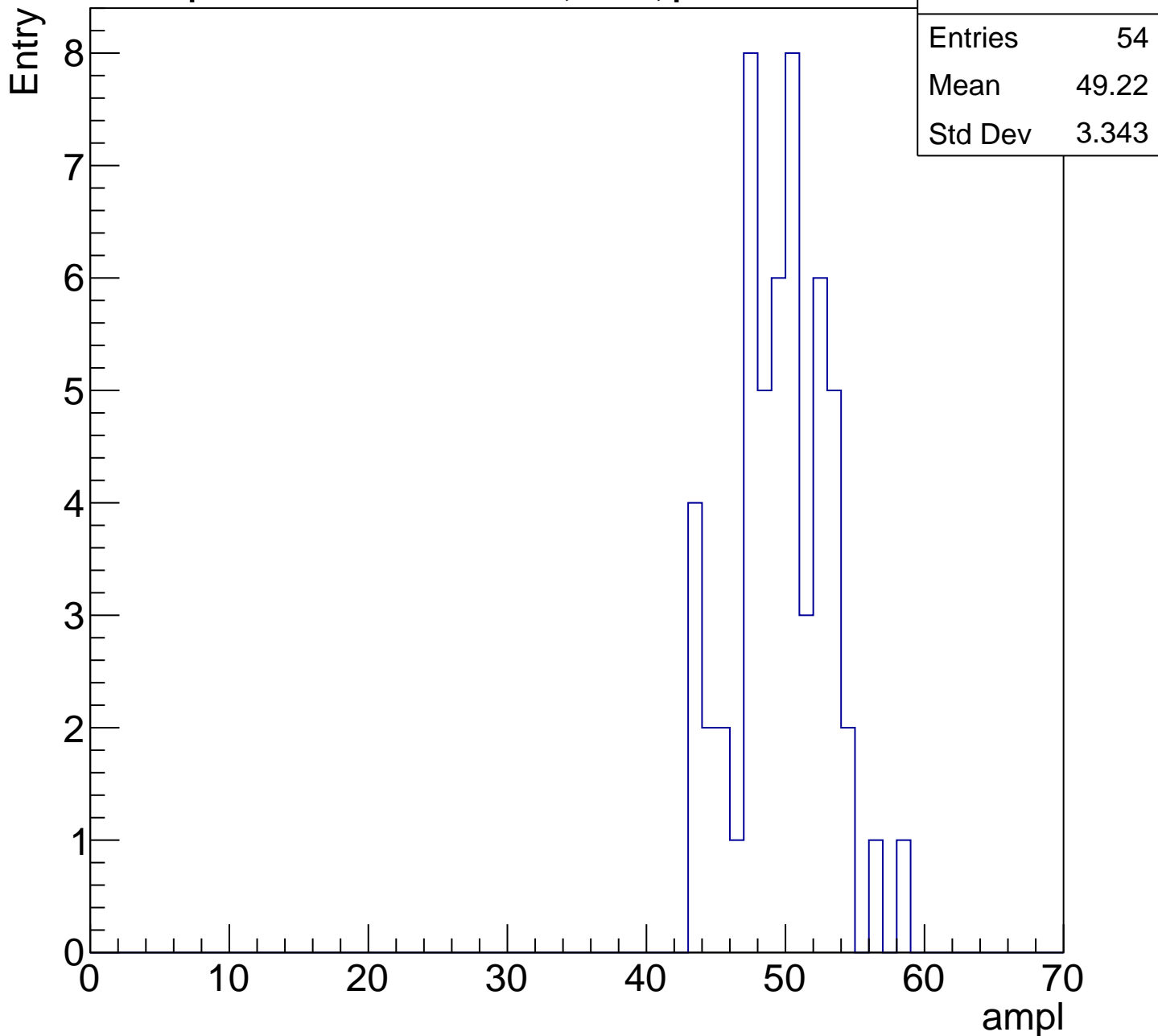
ampl

0 10 20 30 40 50 60 70



# B0L001S, U6-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

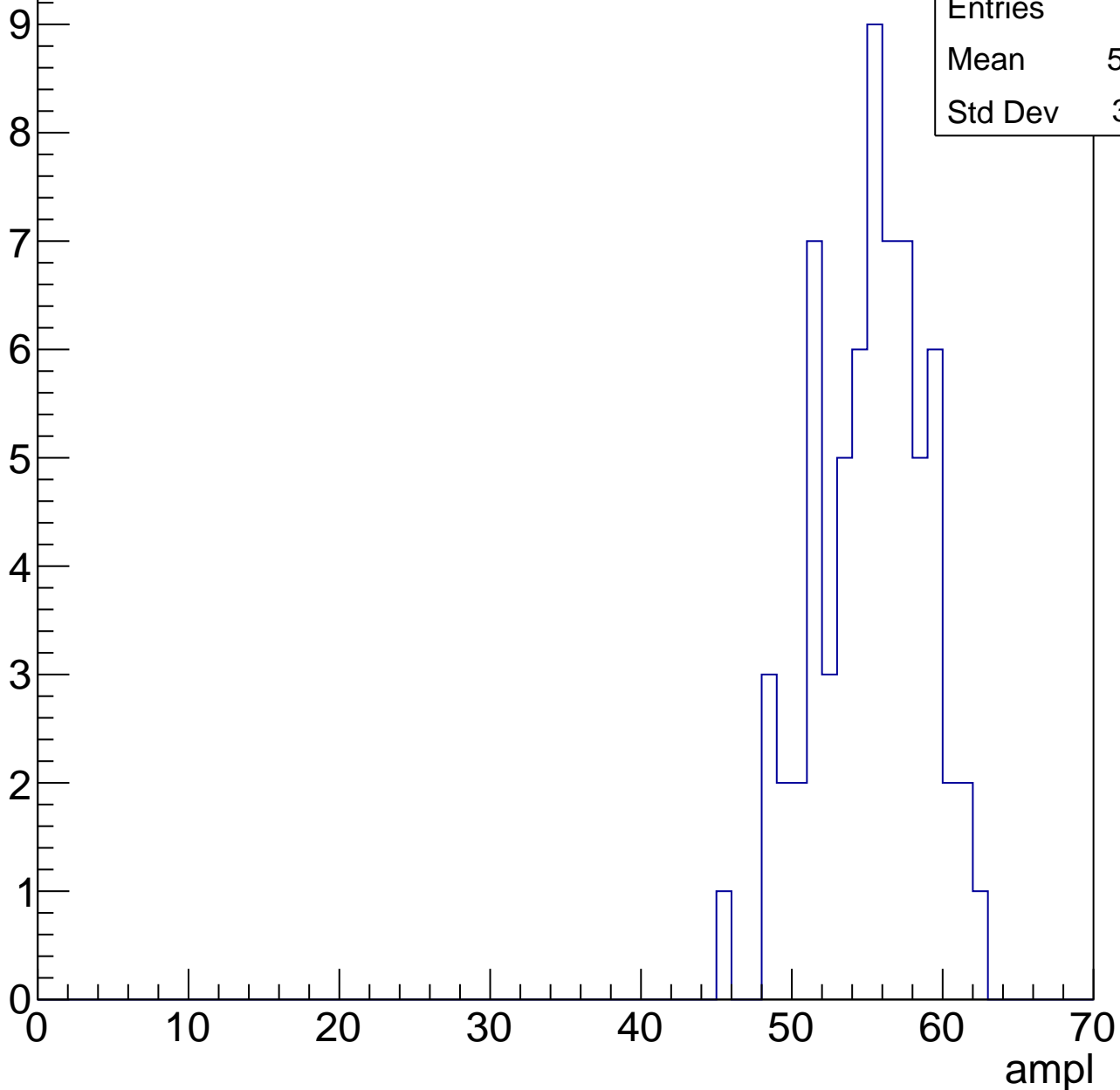


# B0L001S, U6-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

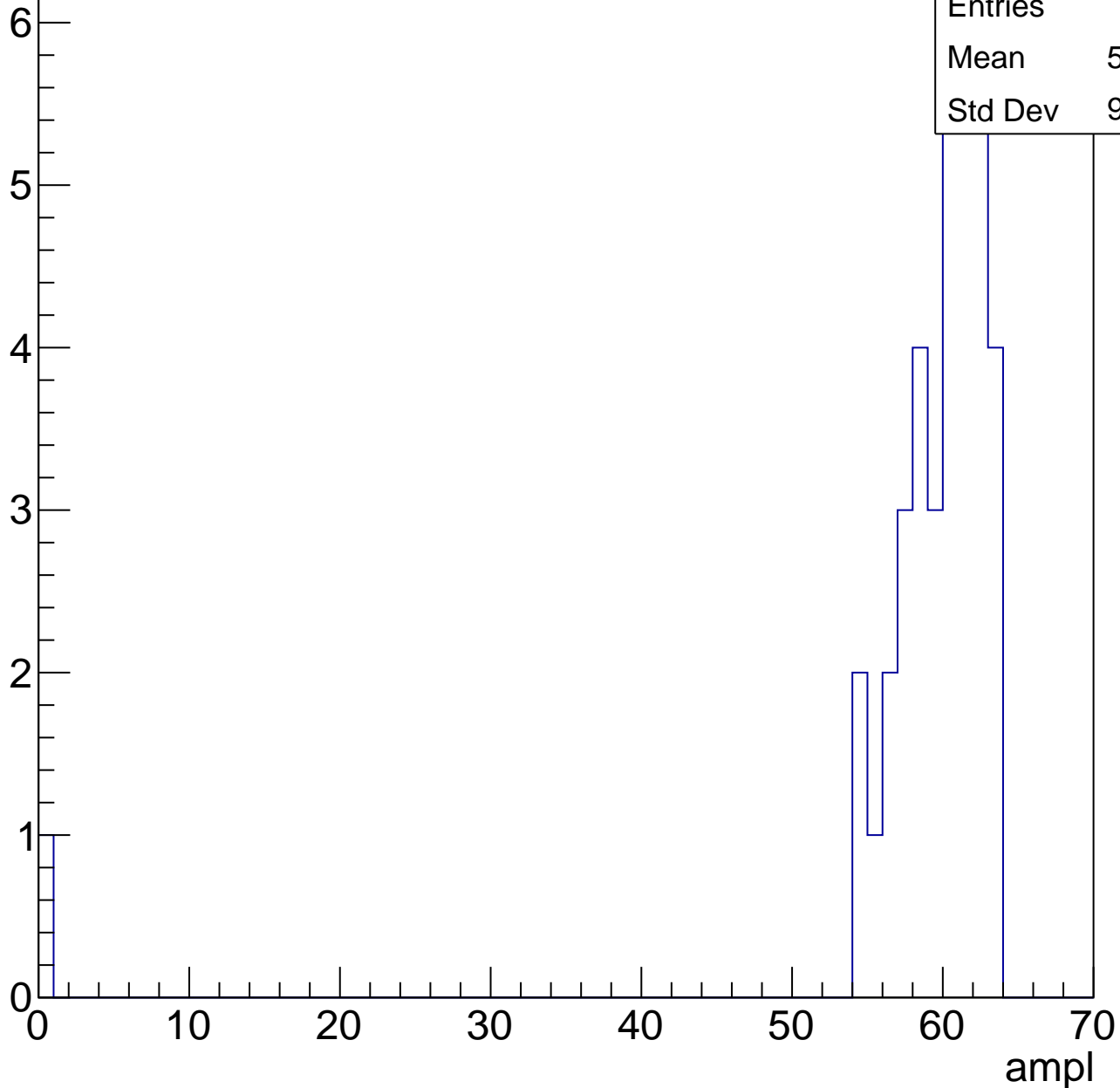
Entries	68
Mean	54.75
Std Dev	3.591



# B0L001S, U6-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

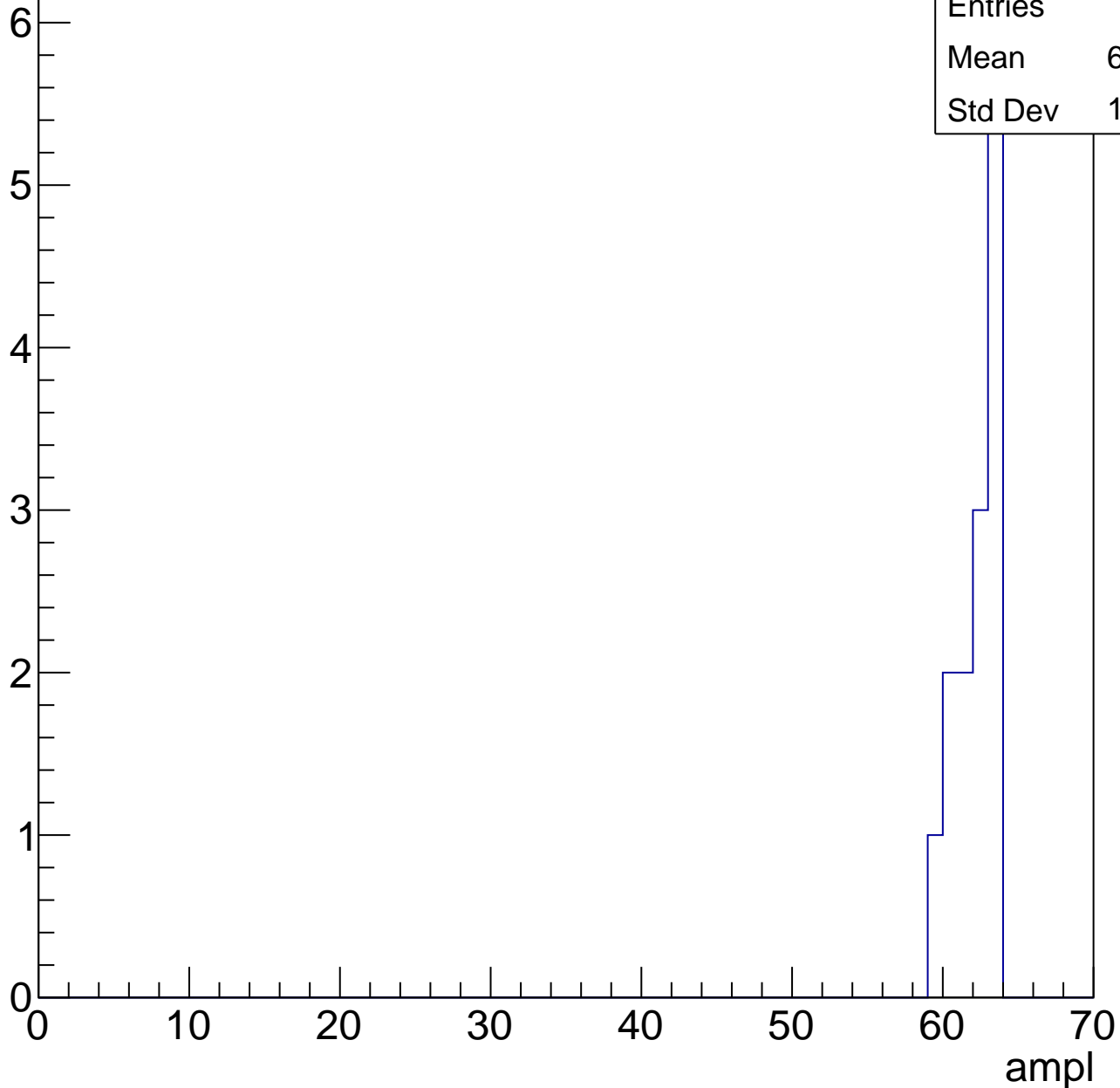
Entry



# B0L001S, U6-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	7.333
Std Dev	10.37

# B0L001S, U6-ch95, adc0

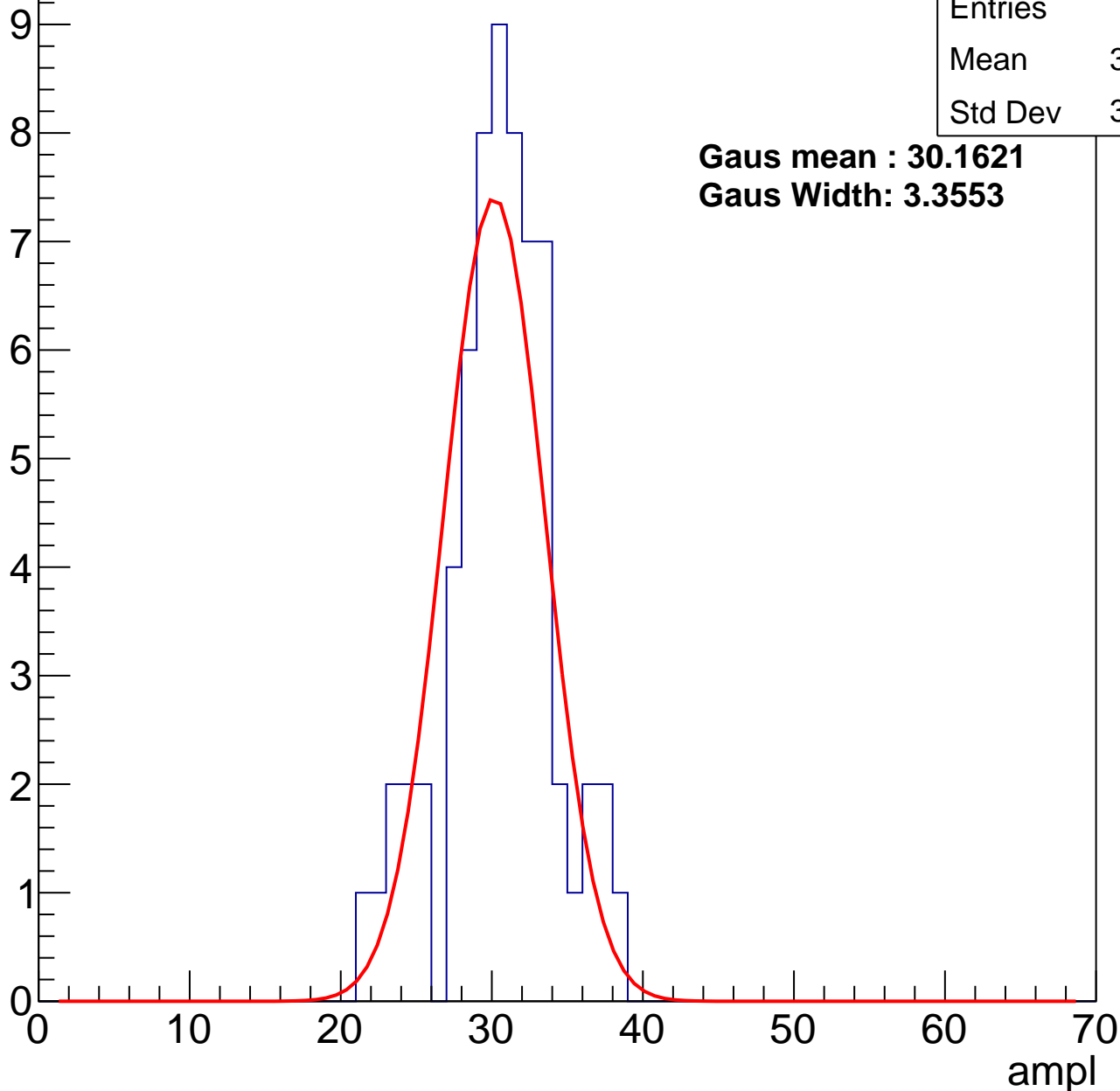
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	30.08
Std Dev	3.557

**Gaus mean : 30.1621**

**Gaus Width: 3.3553**



# B0L001S, U6-ch95, adc1

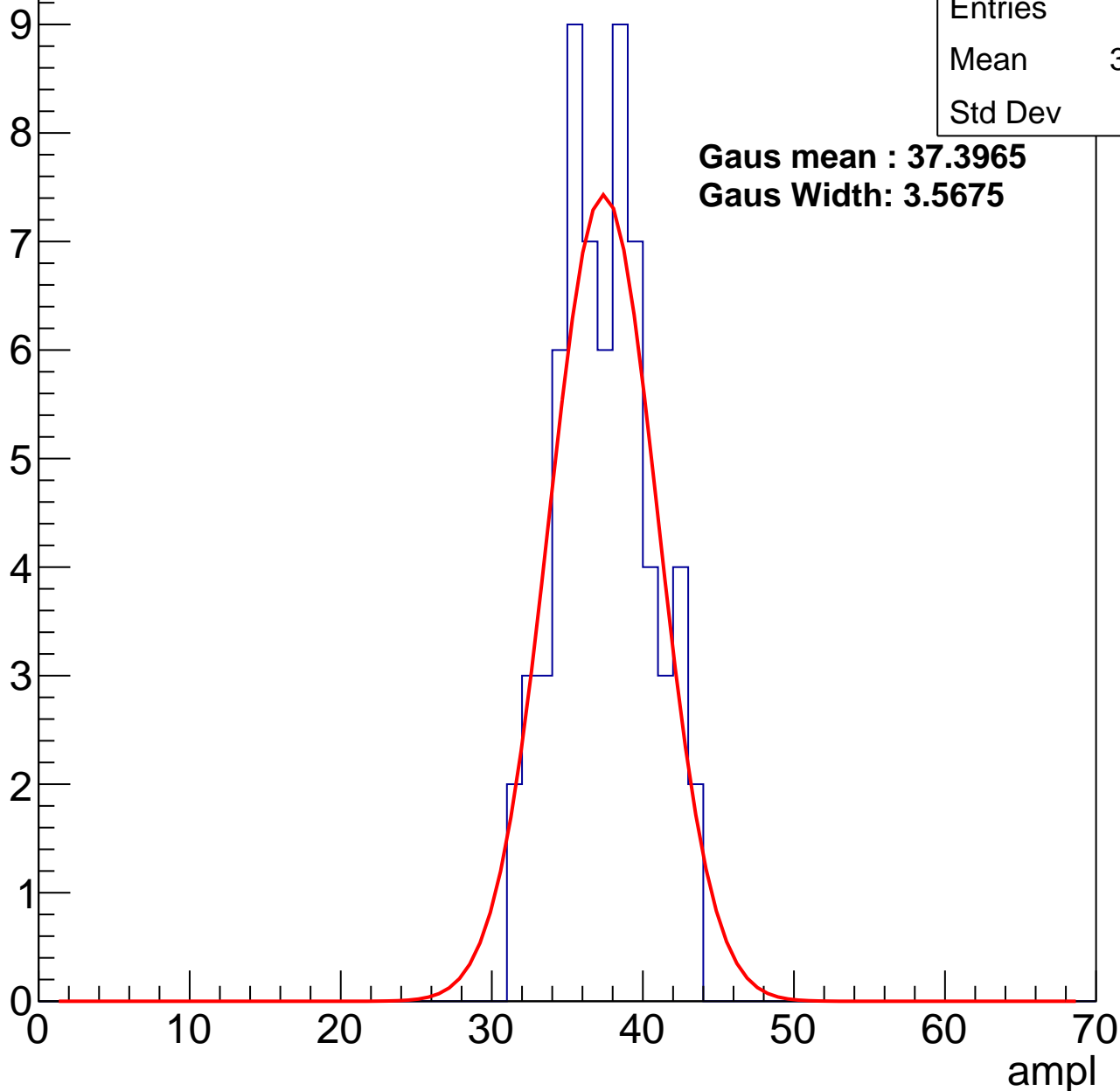
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	36.95
Std Dev	3

**Gaus mean : 37.3965**

**Gaus Width: 3.5675**



# B0L001S, U6-ch95, adc2

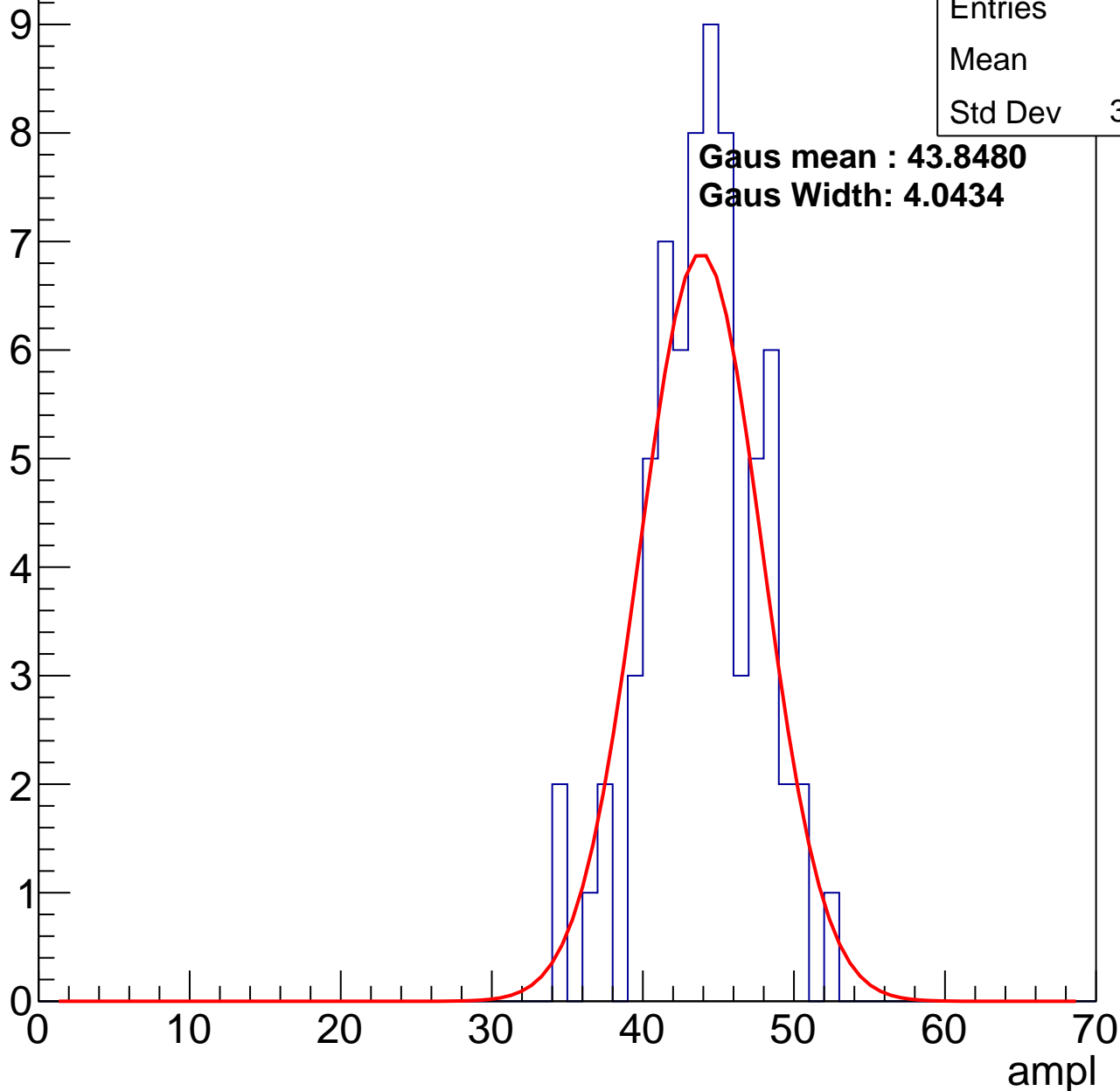
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	43.5
Std Dev	3.667

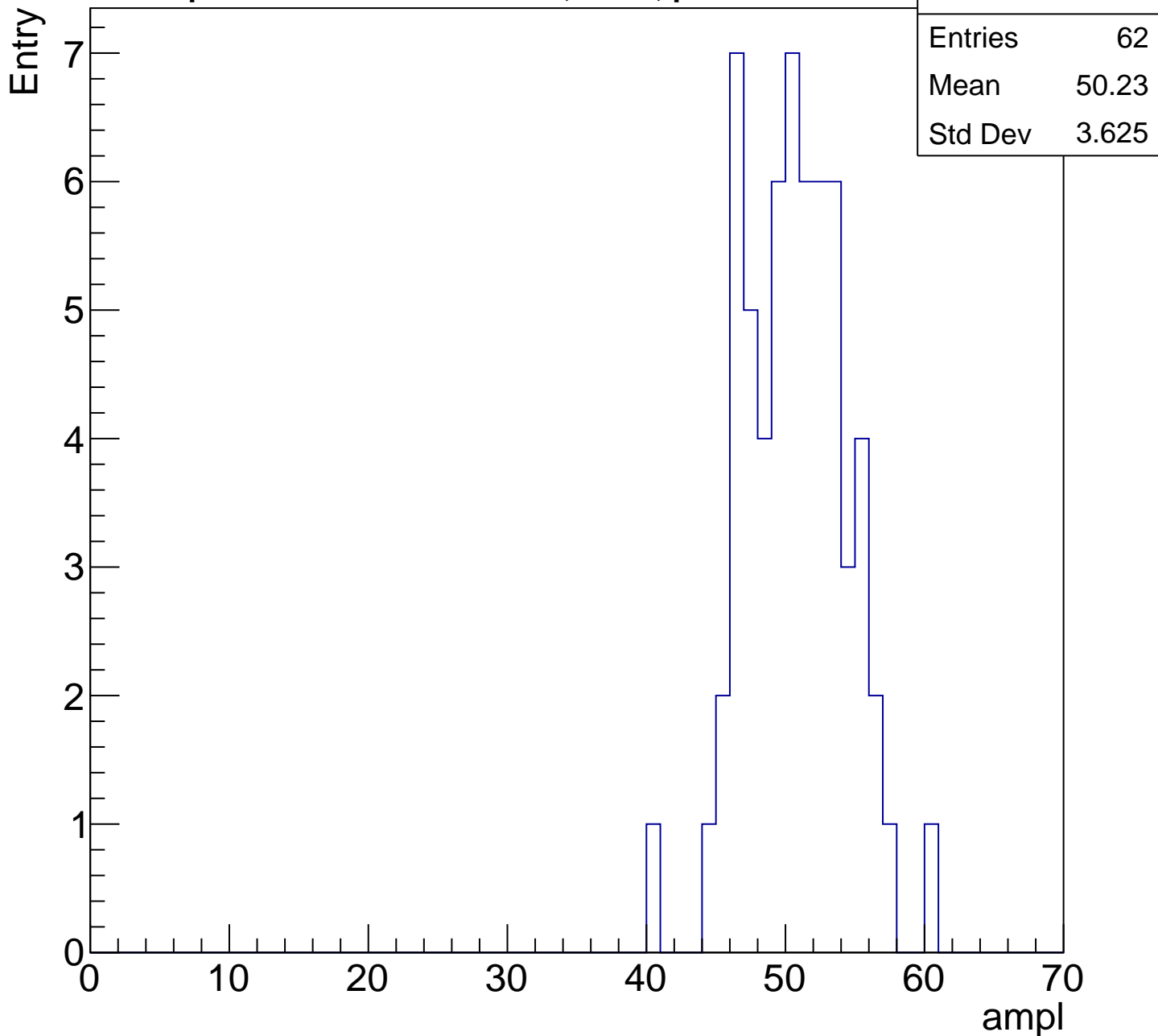
**Gaus mean : 43.8480**

**Gaus Width: 4.0434**



# B0L001S, U6-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

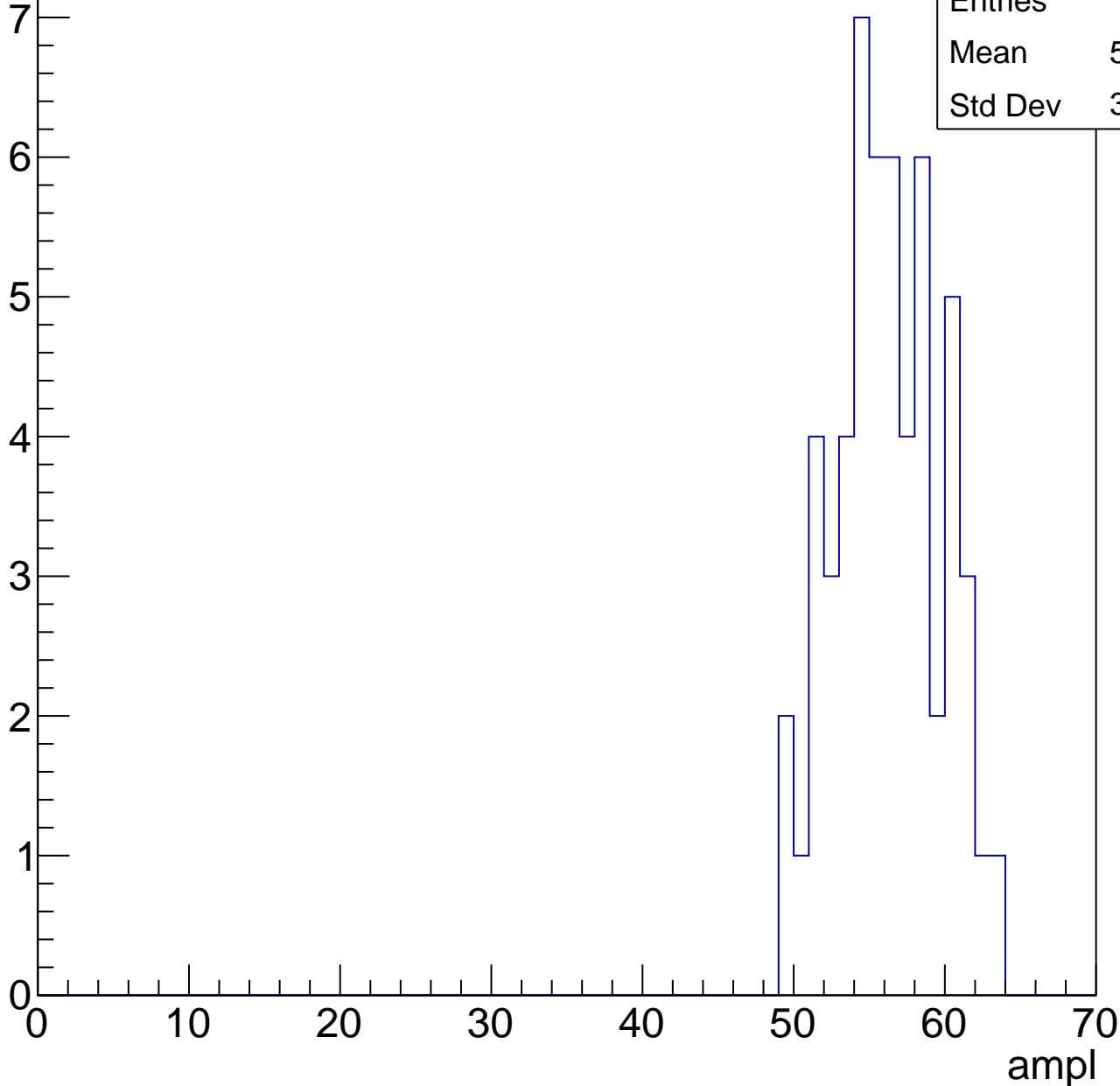


# B0L001S, U6-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	55.75
Std Dev	3.396



# B0L001S, U6-ch95, adc5

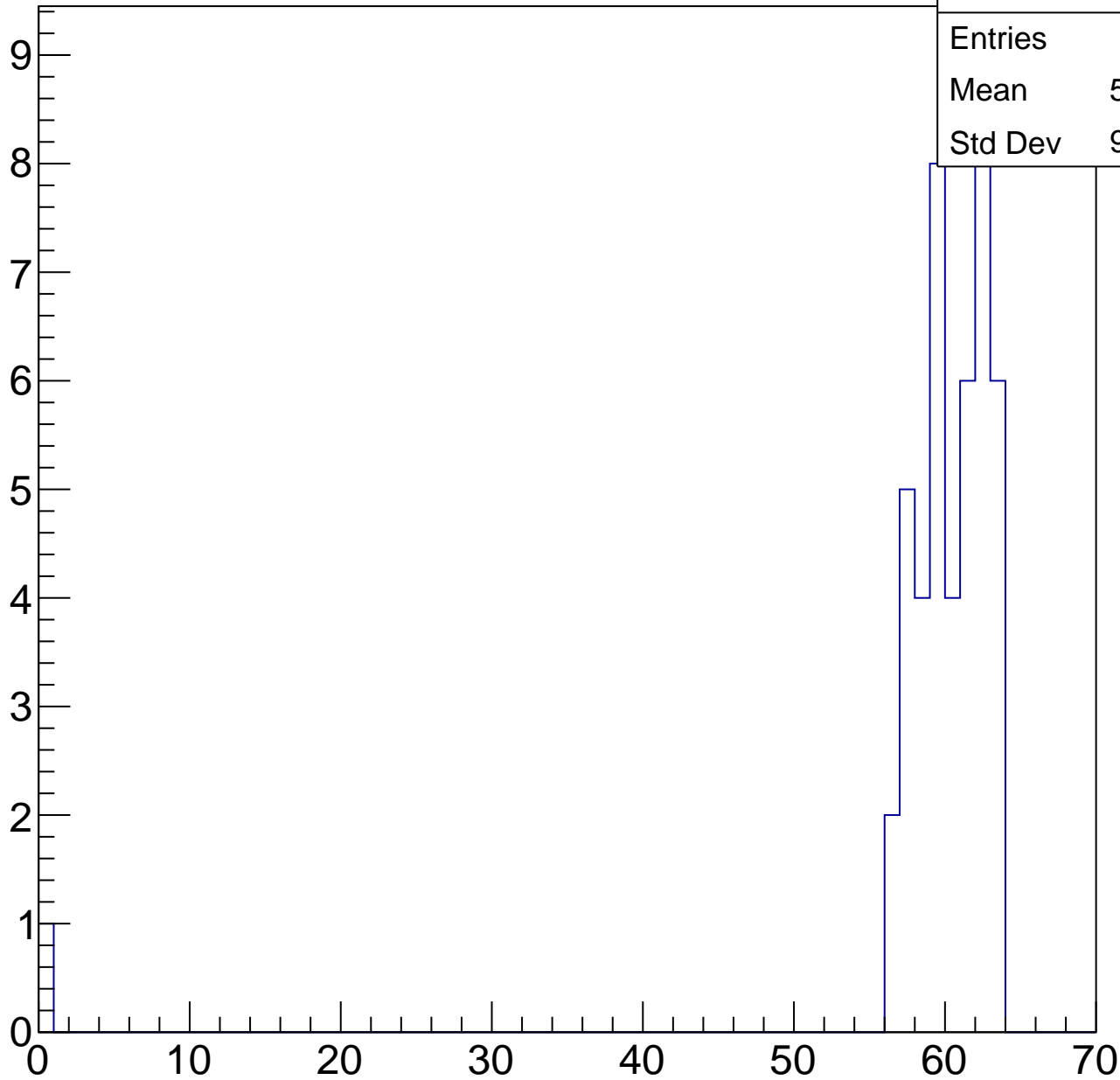
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	45
Mean	58.73
Std Dev	9.098

ampl



# B0L001S, U6-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U6-ch96, adc0

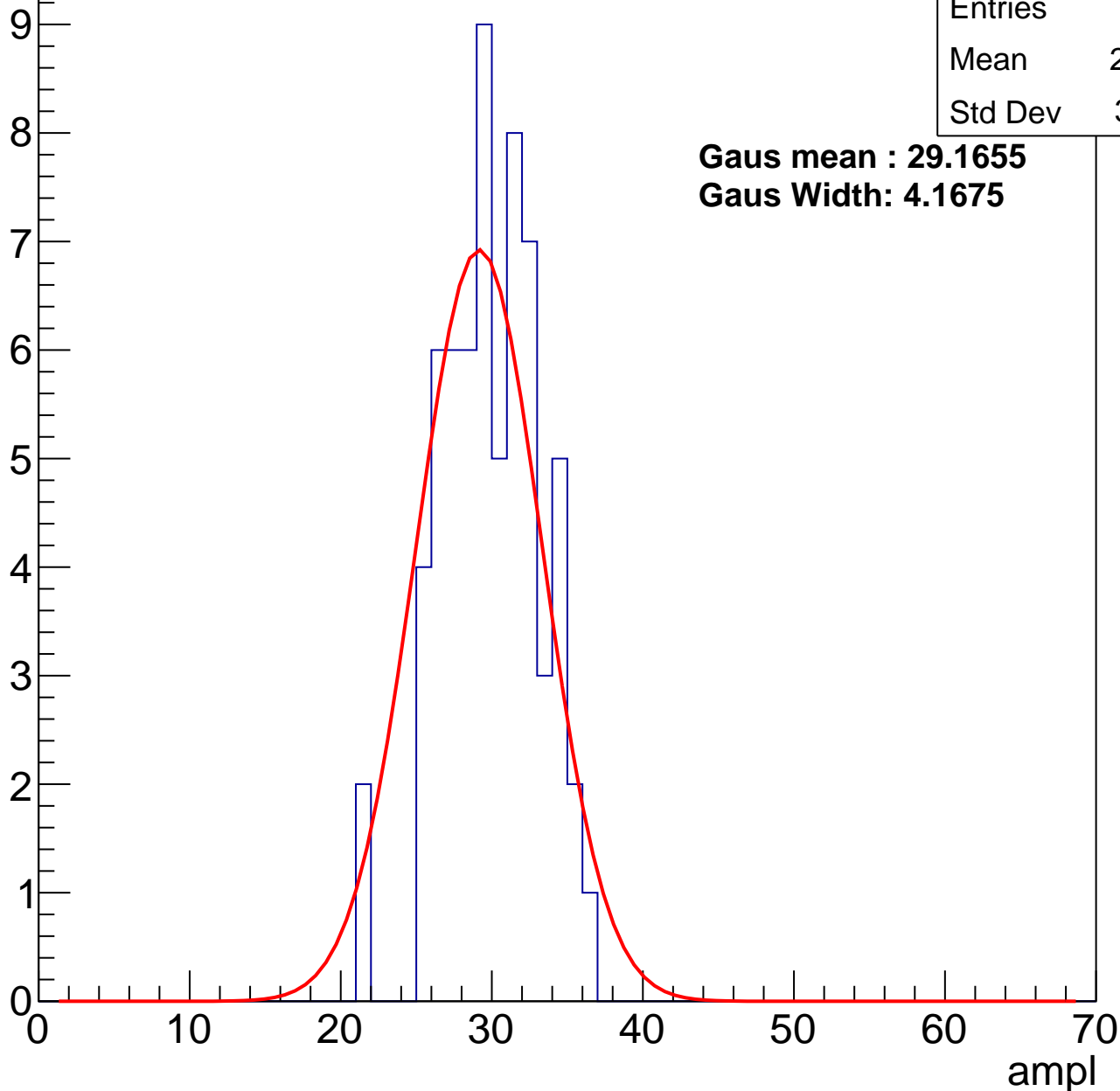
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	29.47
Std Dev	3.201

**Gaus mean : 29.1655**

**Gaus Width: 4.1675**



# B0L001S, U6-ch96, adc1

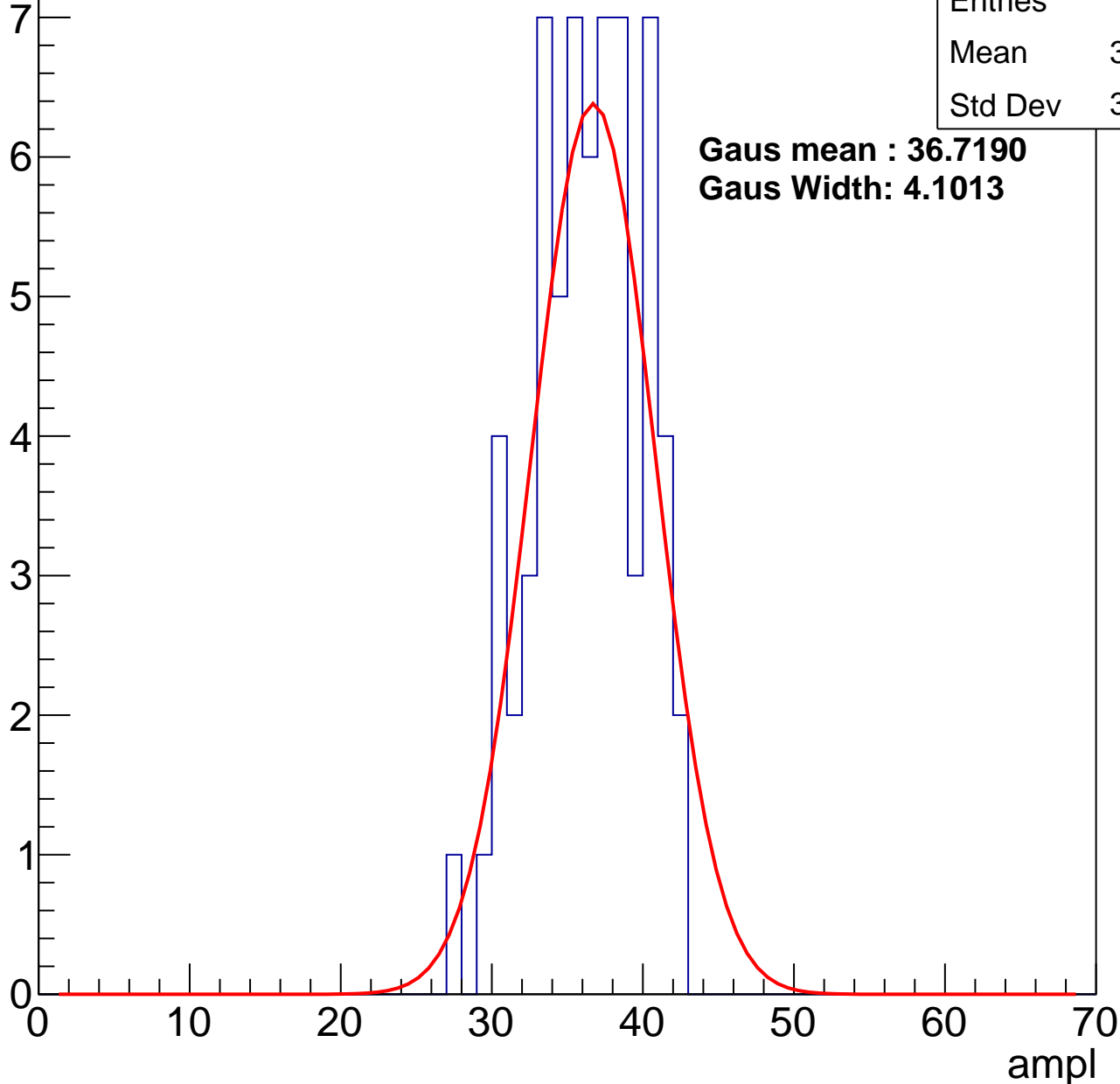
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	35.85
Std Dev	3.496

**Gaus mean : 36.7190**

**Gaus Width: 4.1013**



# B0L001S, U6-ch96, adc2

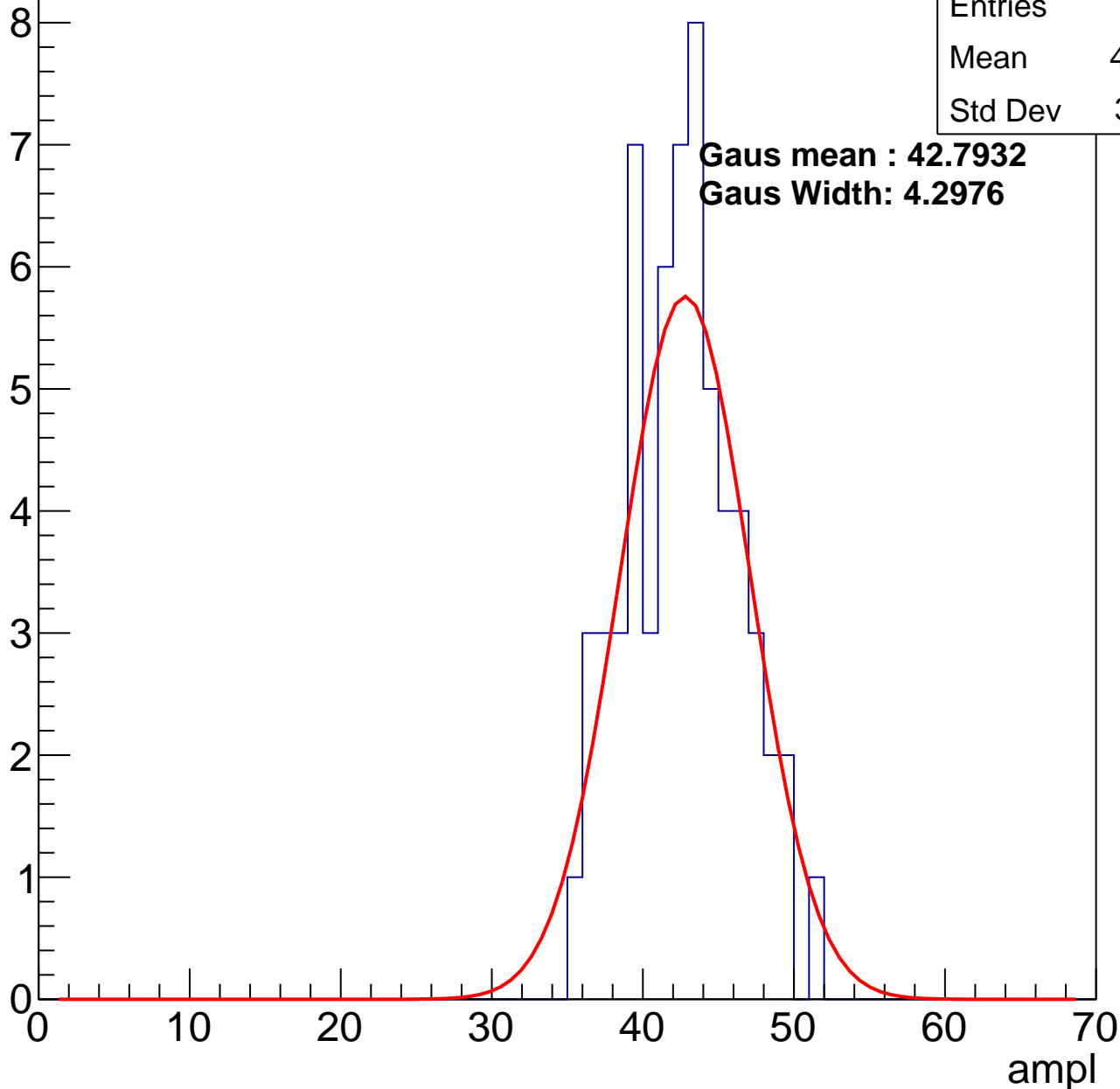
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	42.18
Std Dev	3.621

**Gaus mean : 42.7932**

**Gaus Width: 4.2976**

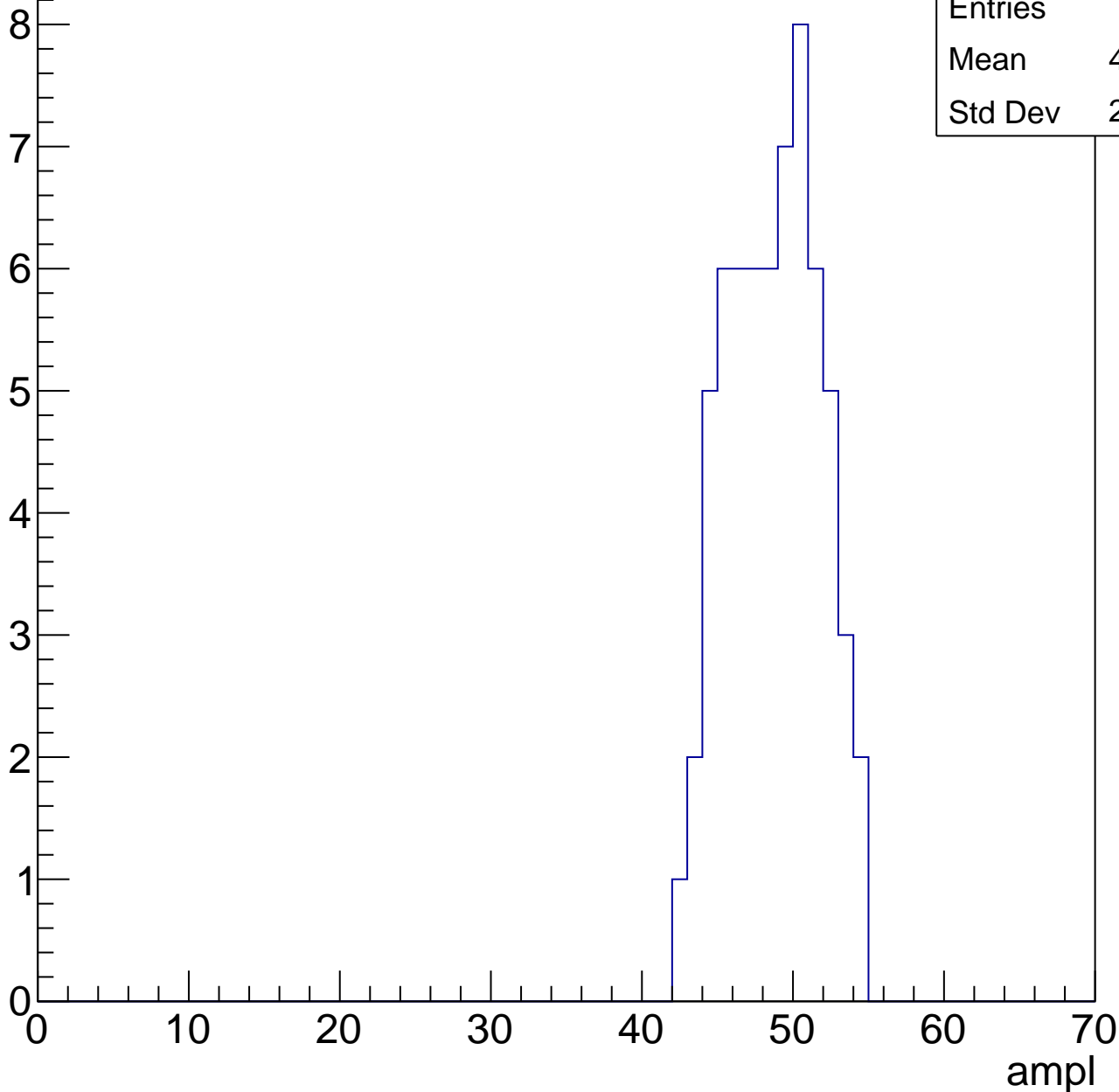


# B0L001S, U6-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	48.25
Std Dev	2.997

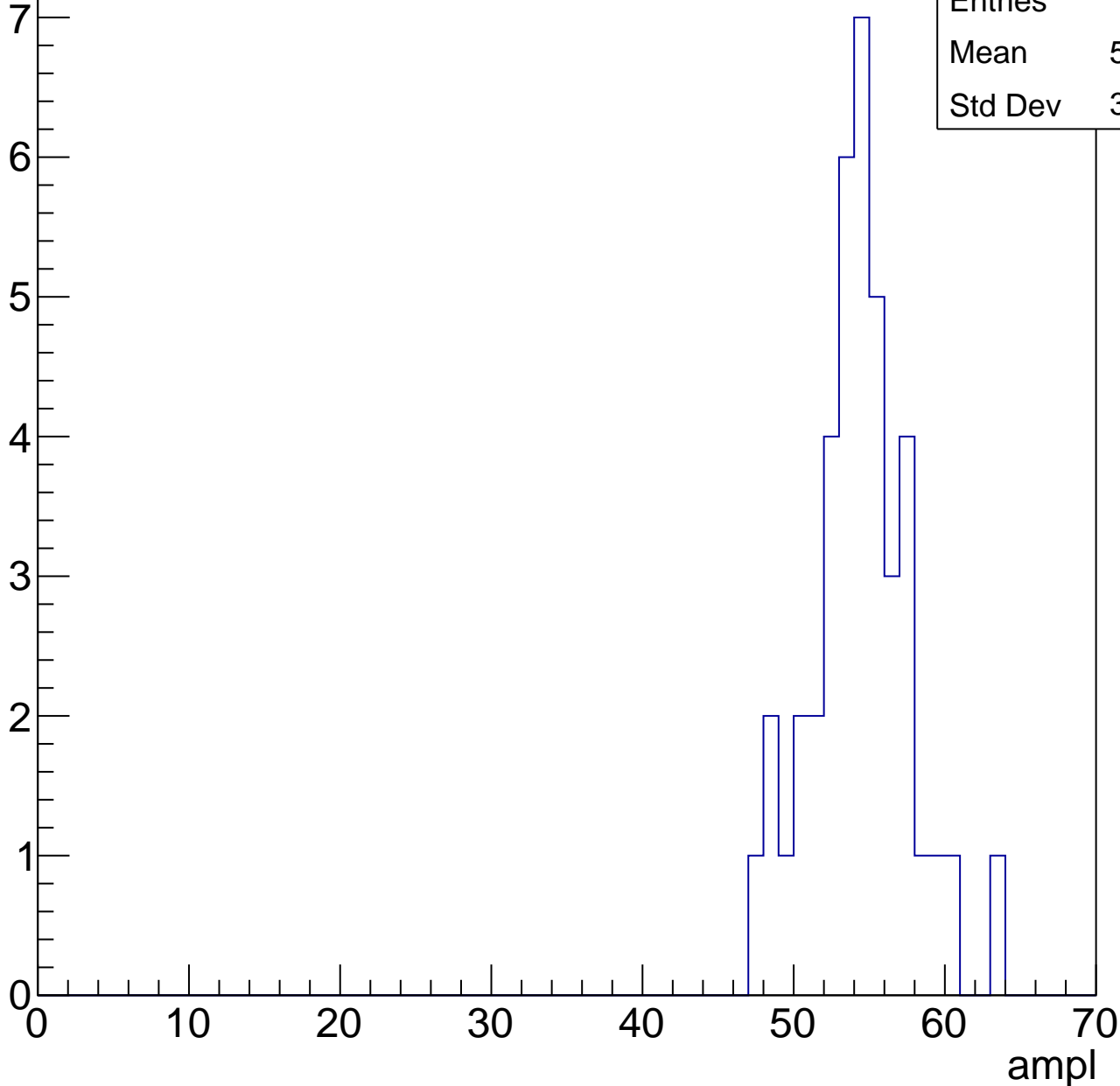


# B0L001S, U6-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	41
Mean	53.88
Std Dev	3.232



# B0L001S, U6-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

10

8

6

4

2

0

0

10

20

30

40

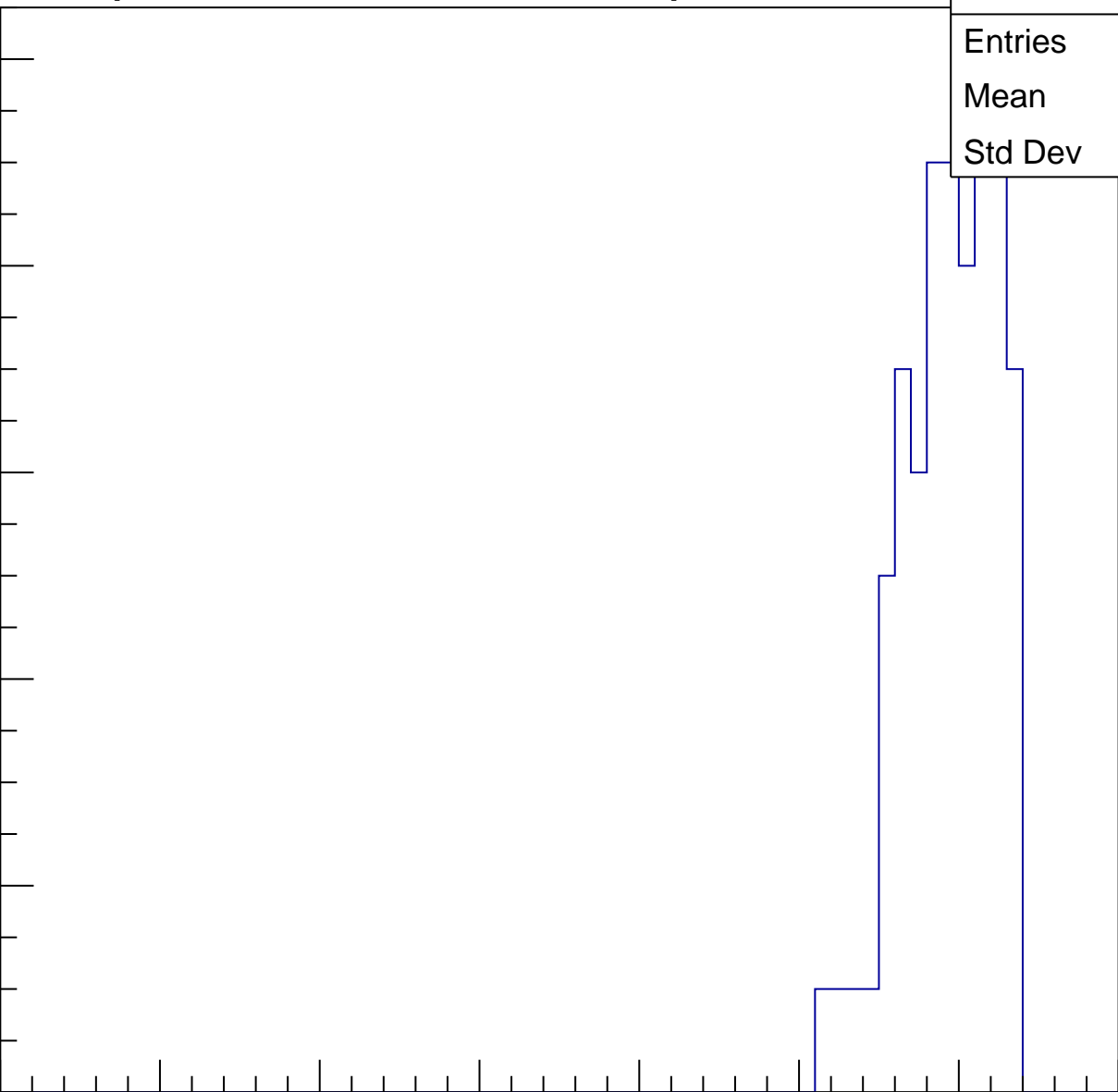
50

60

70

ampl

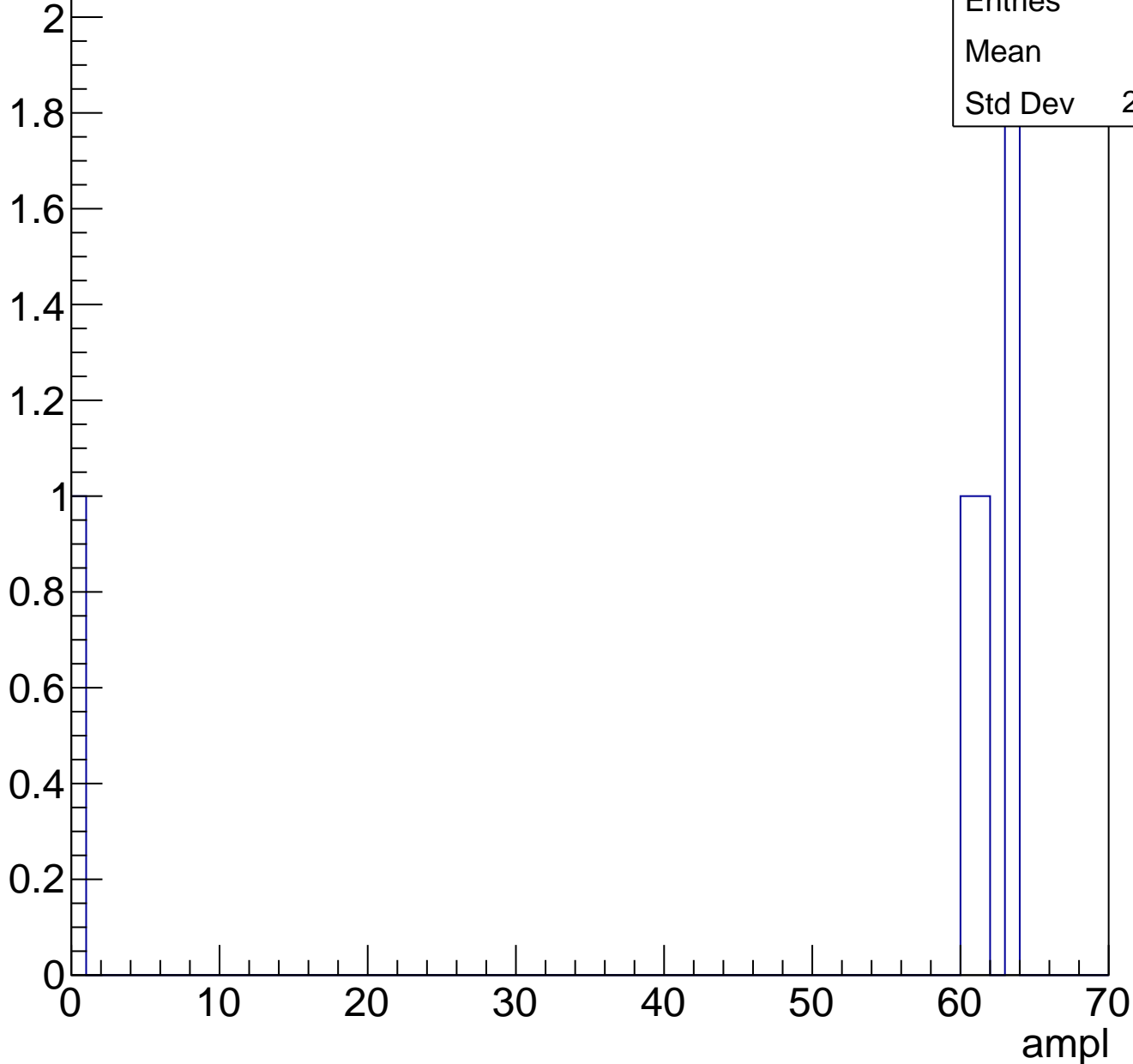
Entries	74
Mean	58.95
Std Dev	2.837



# B0L001S, U6-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch97, adc0

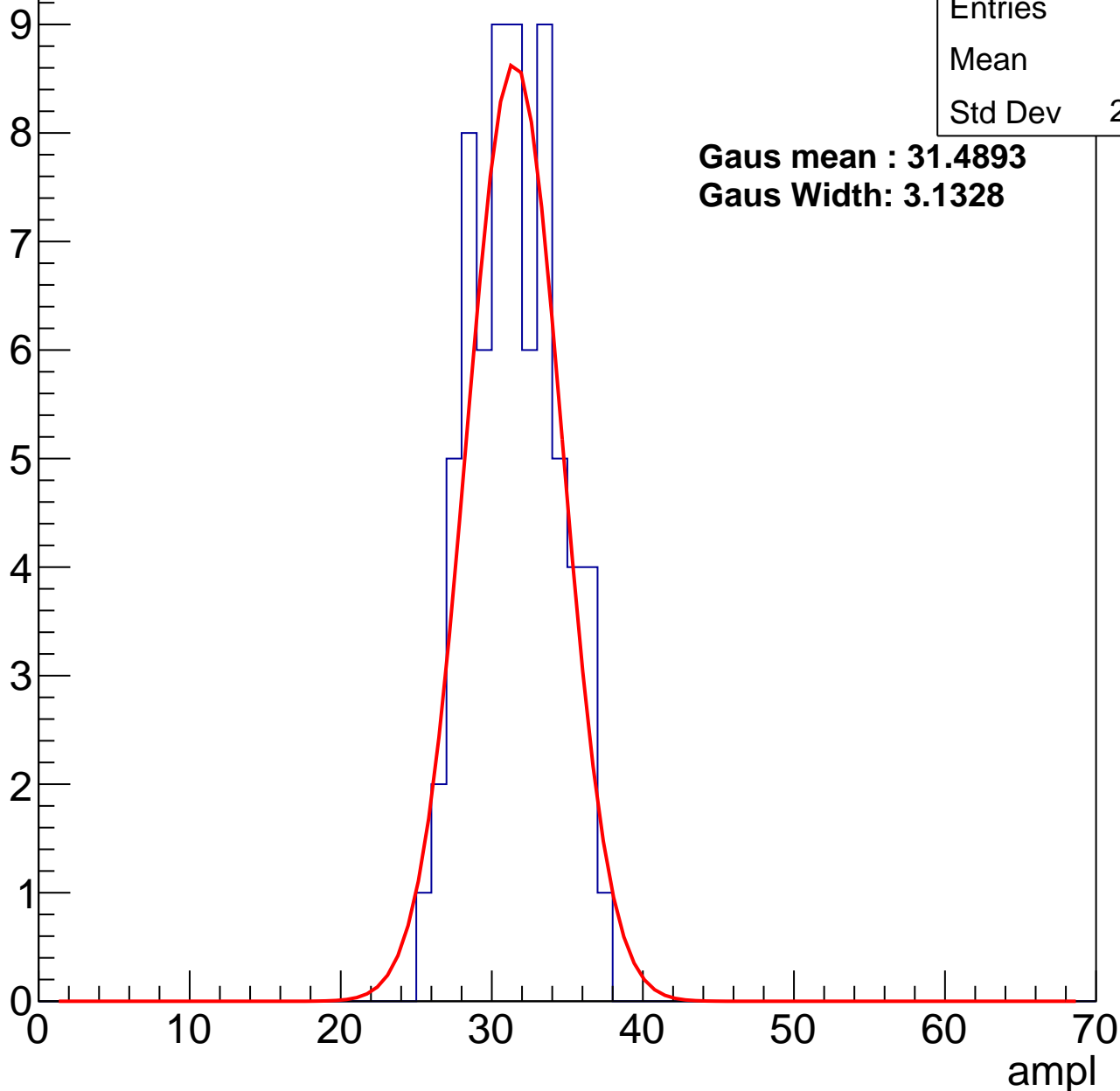
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	31
Std Dev	2.844

**Gaus mean : 31.4893**

**Gaus Width: 3.1328**



# B0L001S, U6-ch97, adc1

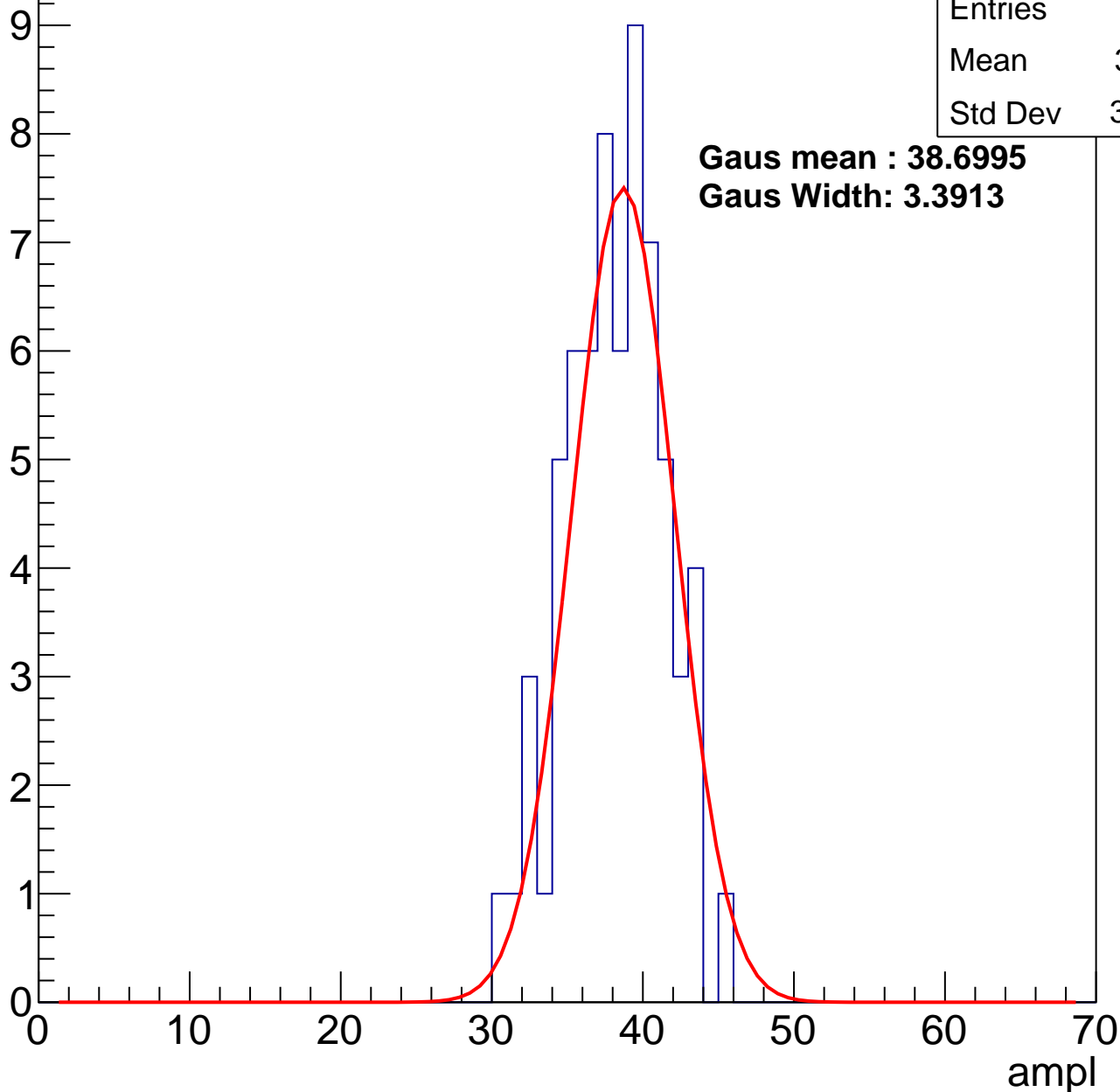
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	37.71
Std Dev	3.223

**Gaus mean : 38.6995**

**Gaus Width: 3.3913**



# B0L001S, U6-ch97, adc2

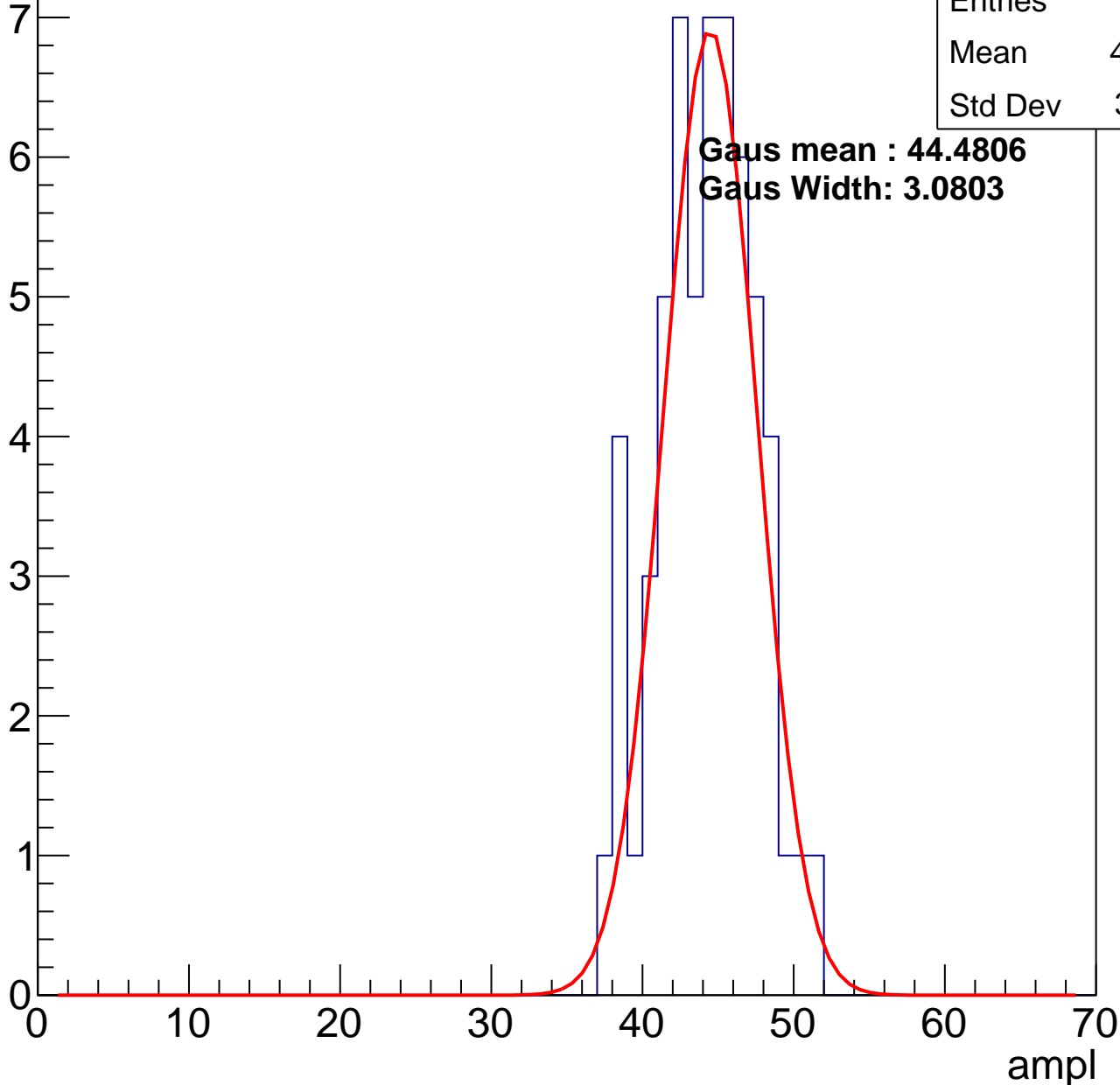
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	43.76
Std Dev	3.191

**Gaus mean : 44.4806**

**Gaus Width: 3.0803**

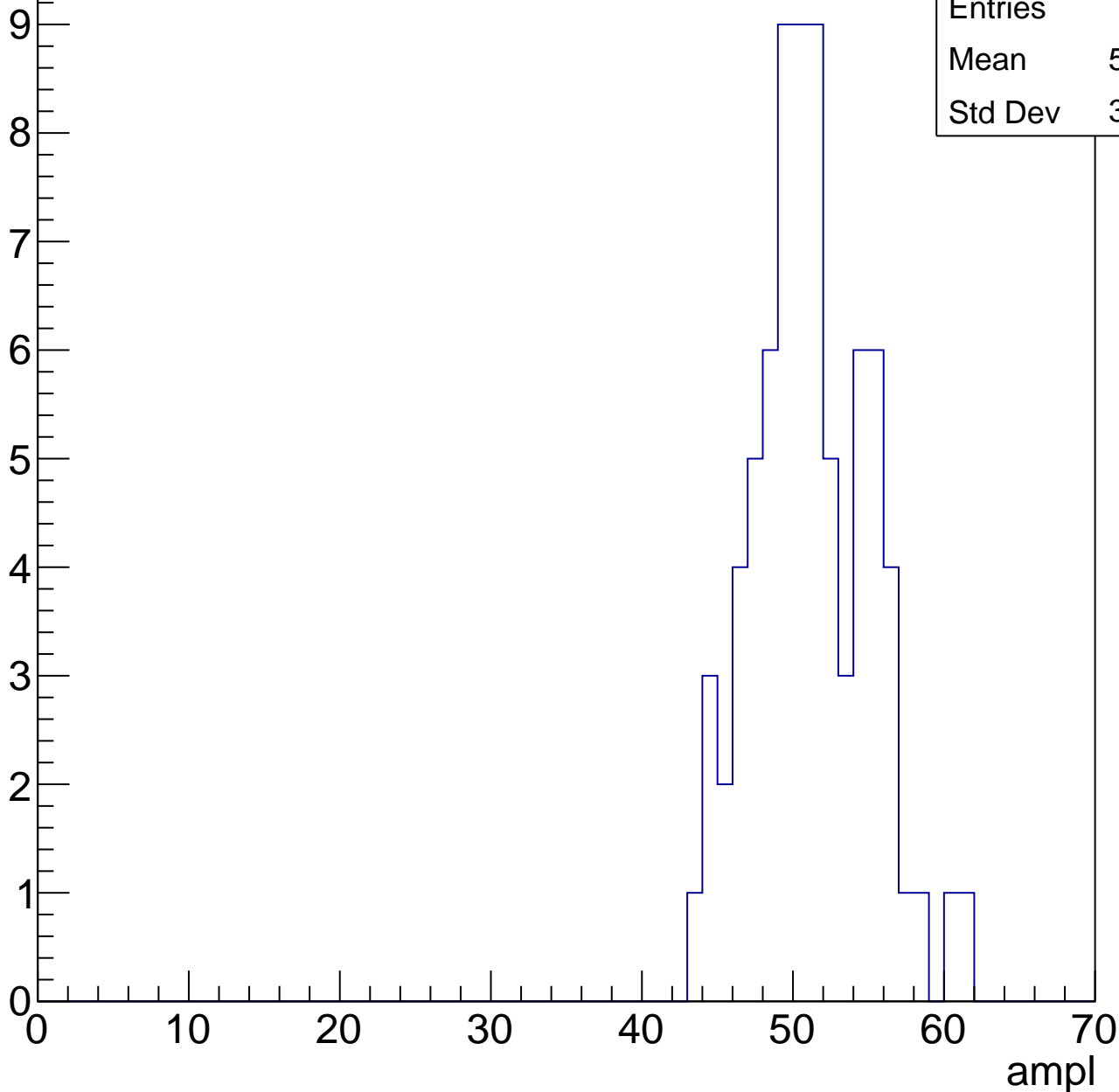


# B0L001S, U6-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

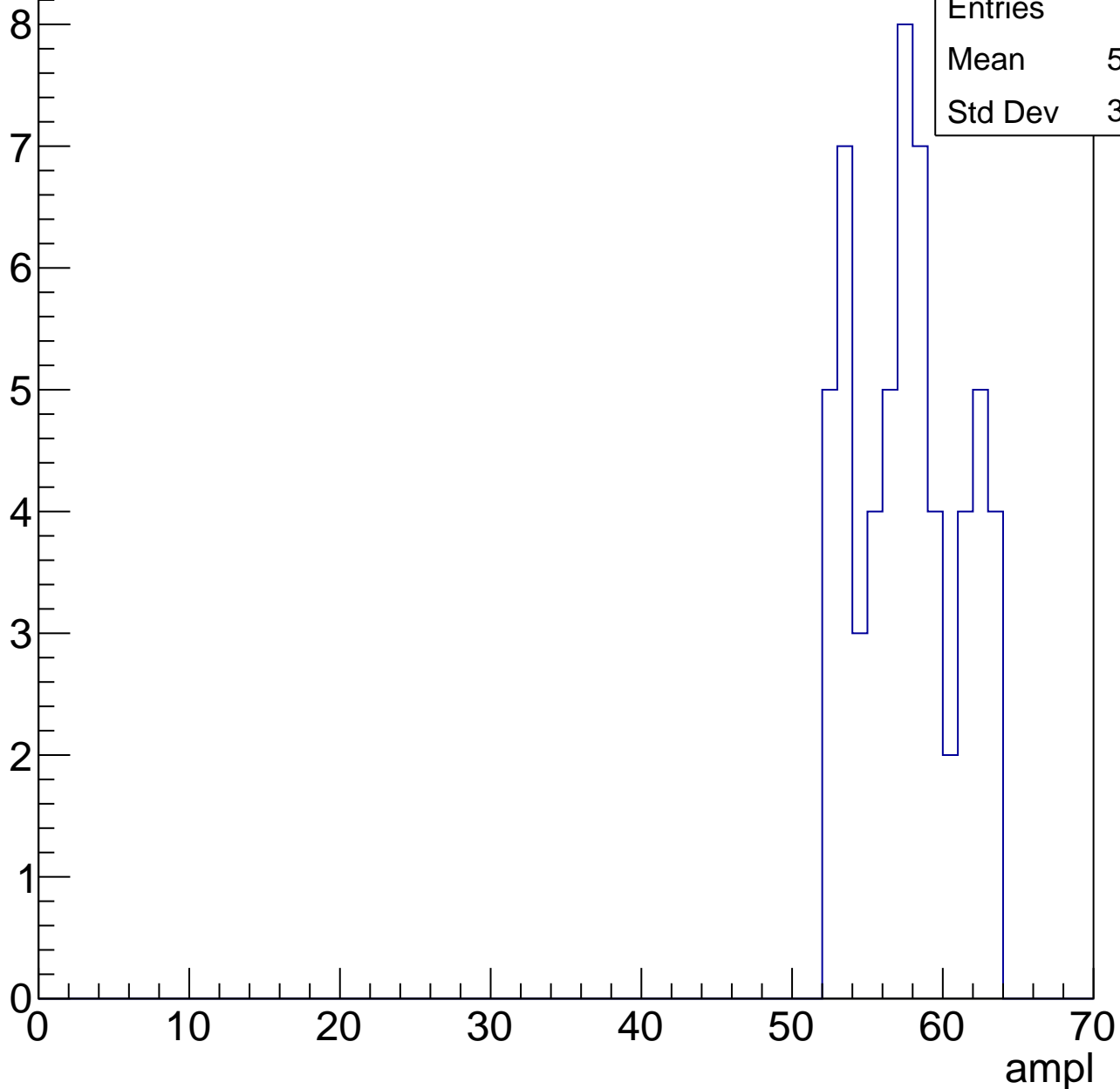
Entries	76
Mean	50.72
Std Dev	3.786



# B0L001S, U6-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



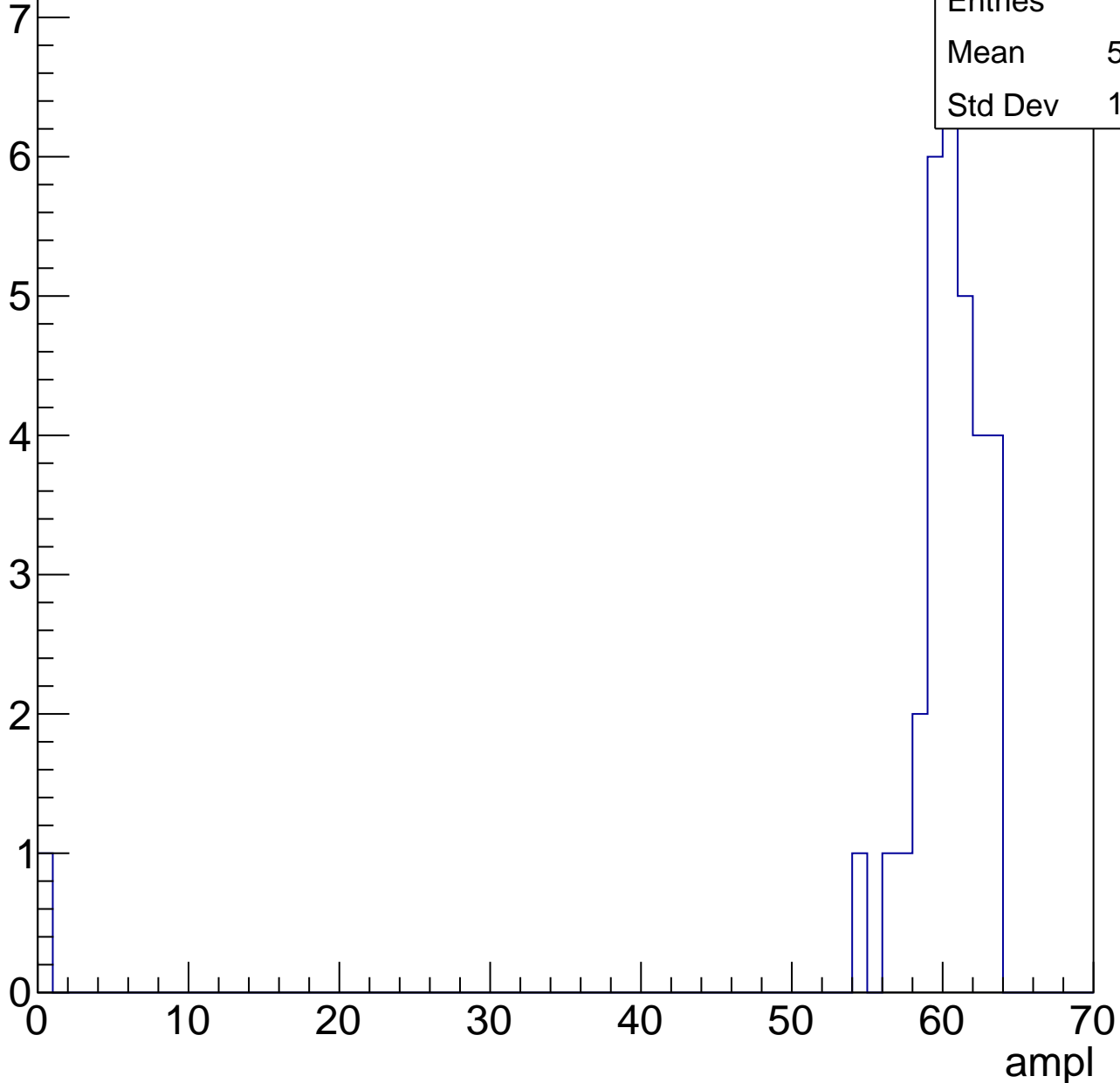
Entries	58
Mean	57.19
Std Dev	3.365

# B0L001S, U6-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	32
Mean	58.19
Std Dev	10.65



# B0L001S, U6-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

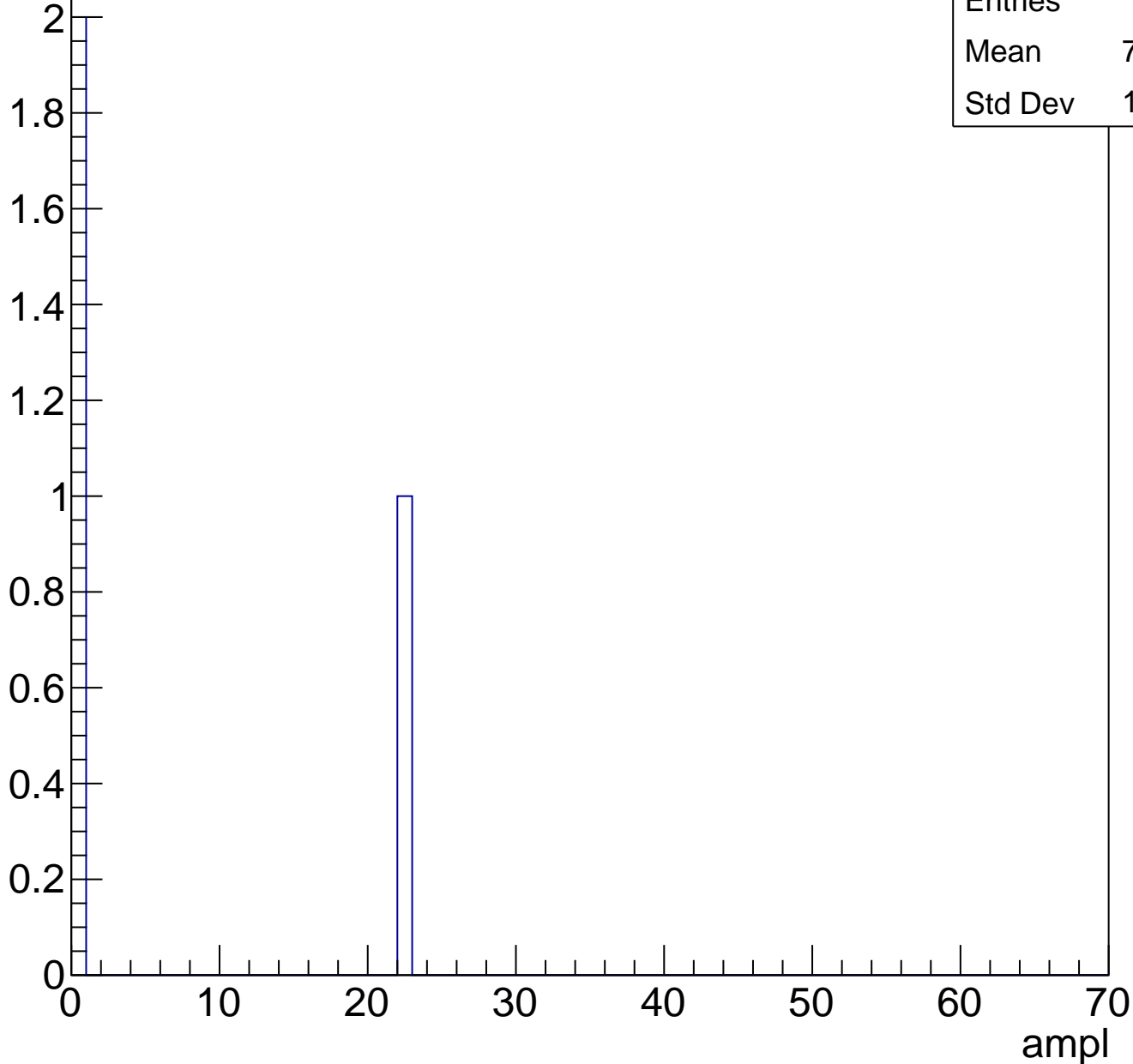
0 10 20 30 40 50 60 70



# B0L001S, U6-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch98, adc0

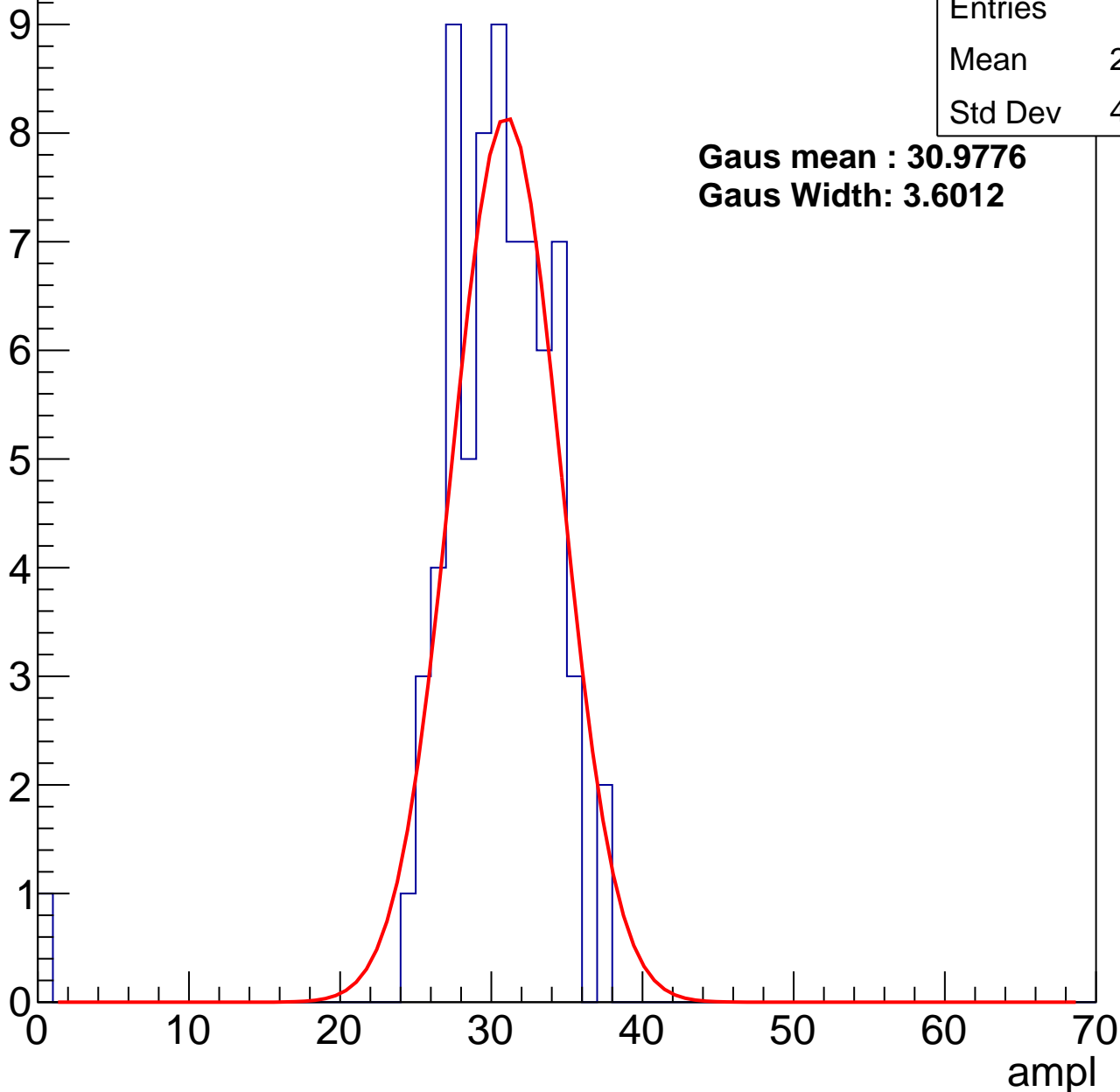
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	29.78
Std Dev	4.646

**Gaus mean : 30.9776**

**Gaus Width: 3.6012**



# B0L001S, U6-ch98, adc1

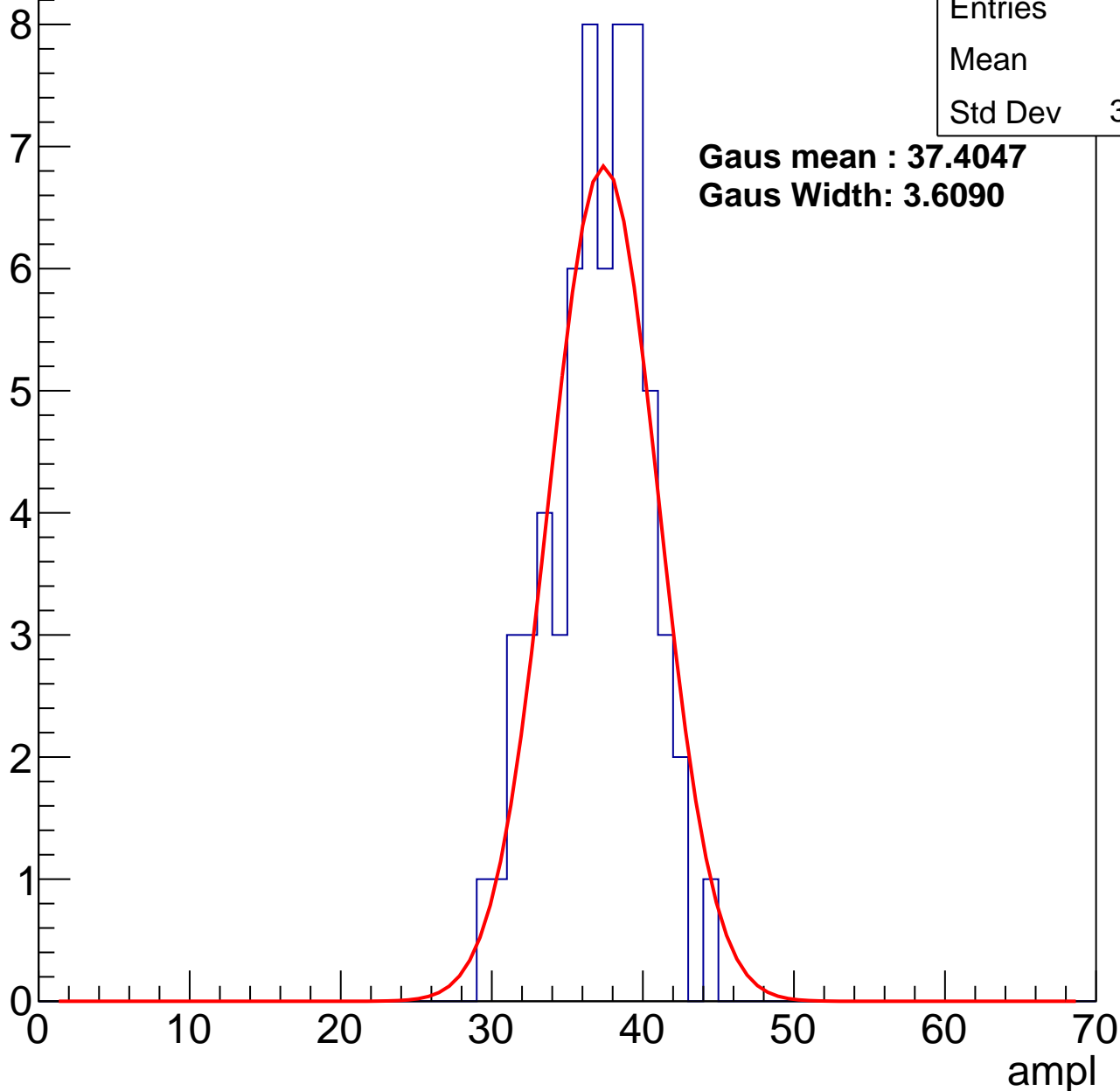
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	36.6
Std Dev	3.215

**Gaus mean : 37.4047**

**Gaus Width: 3.6090**



# B0L001S, U6-ch98, adc2

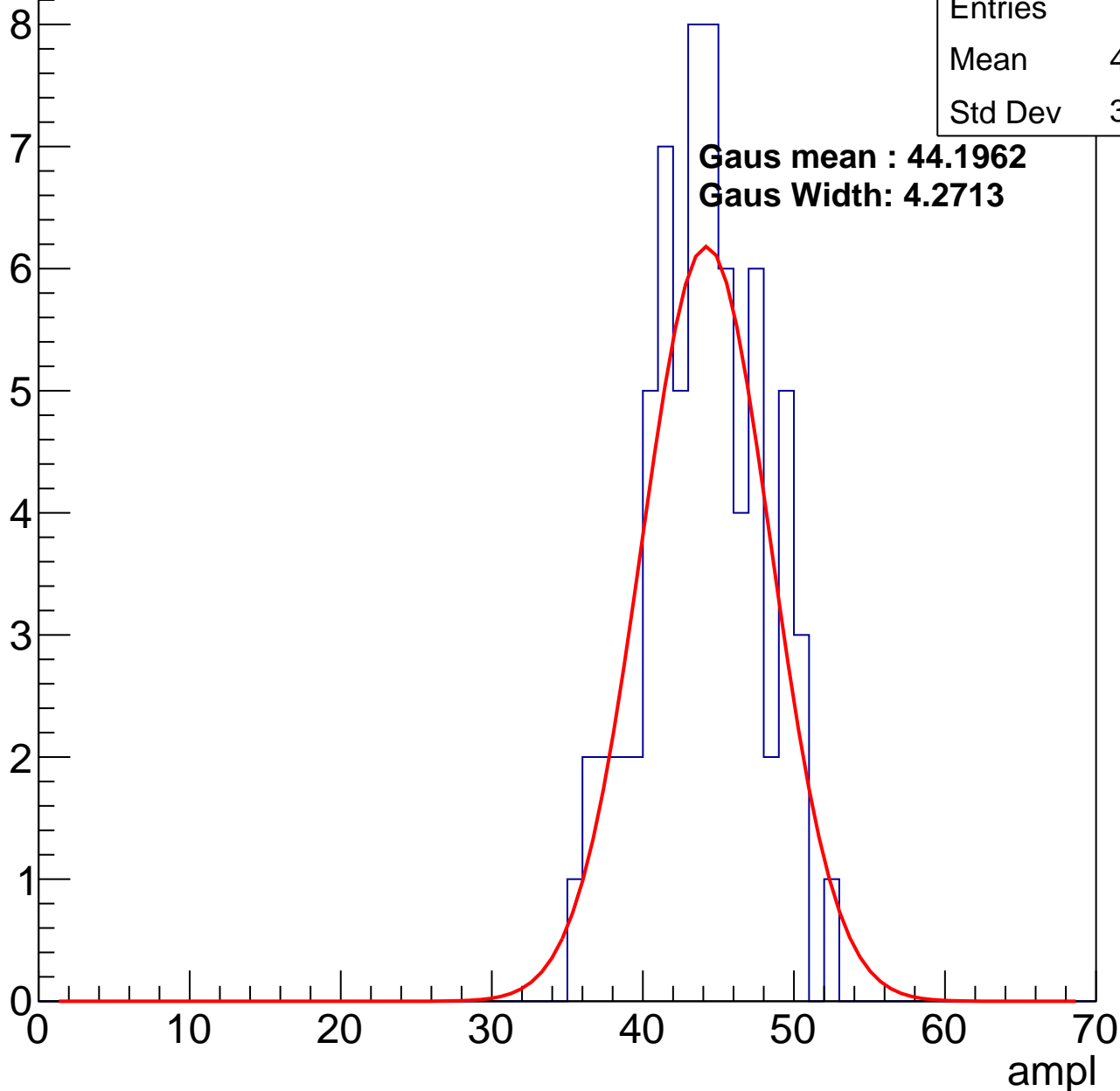
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	43.58
Std Dev	3.793

**Gaus mean : 44.1962**

**Gaus Width: 4.2713**

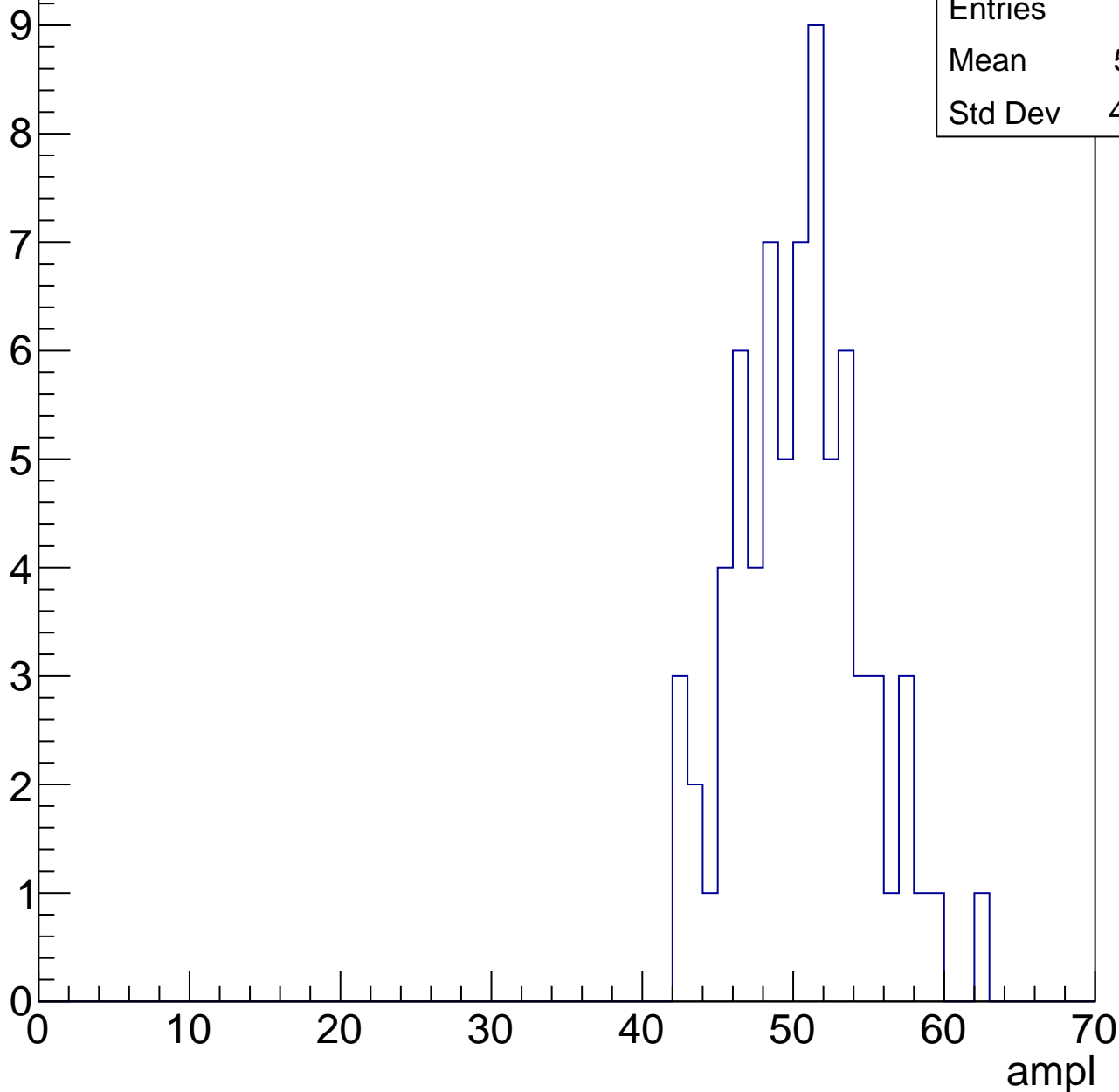


# B0L001S, U6-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	50.01
Std Dev	4.198

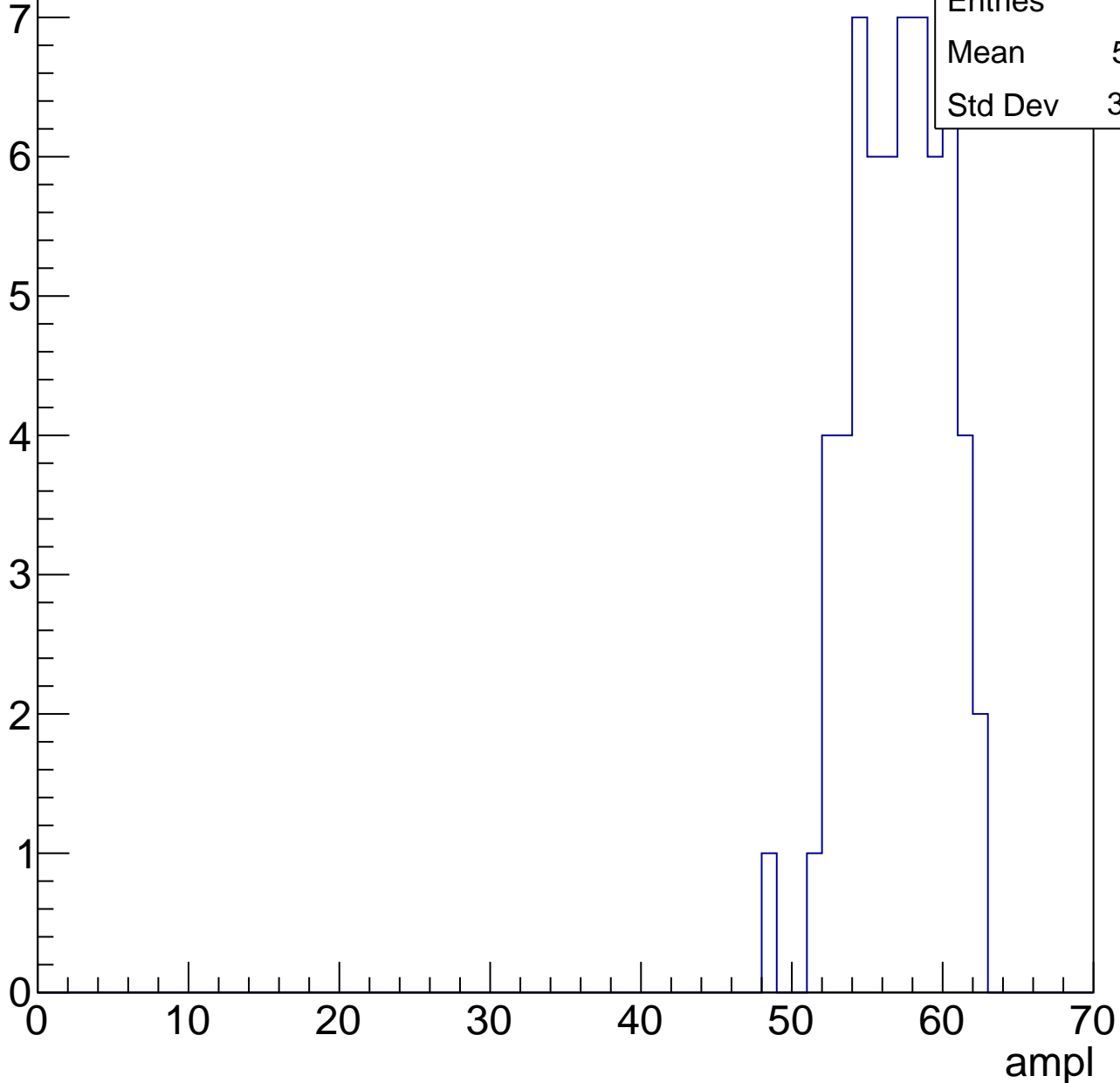


# B0L001S, U6-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	56.61
Std Dev	3.039

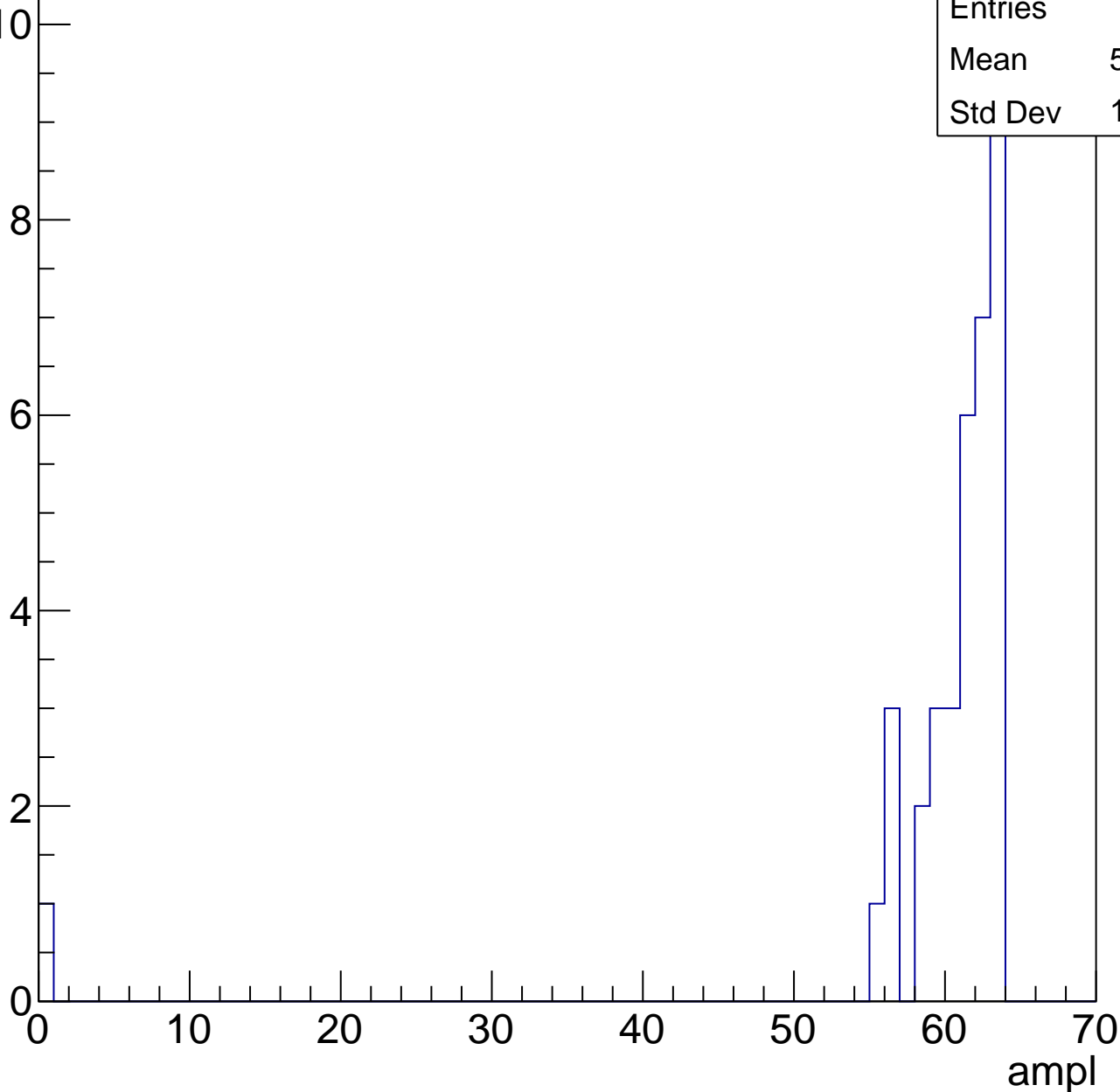


# B0L001S, U6-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	36
Mean	59.06
Std Dev	10.24



# B0L001S, U6-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



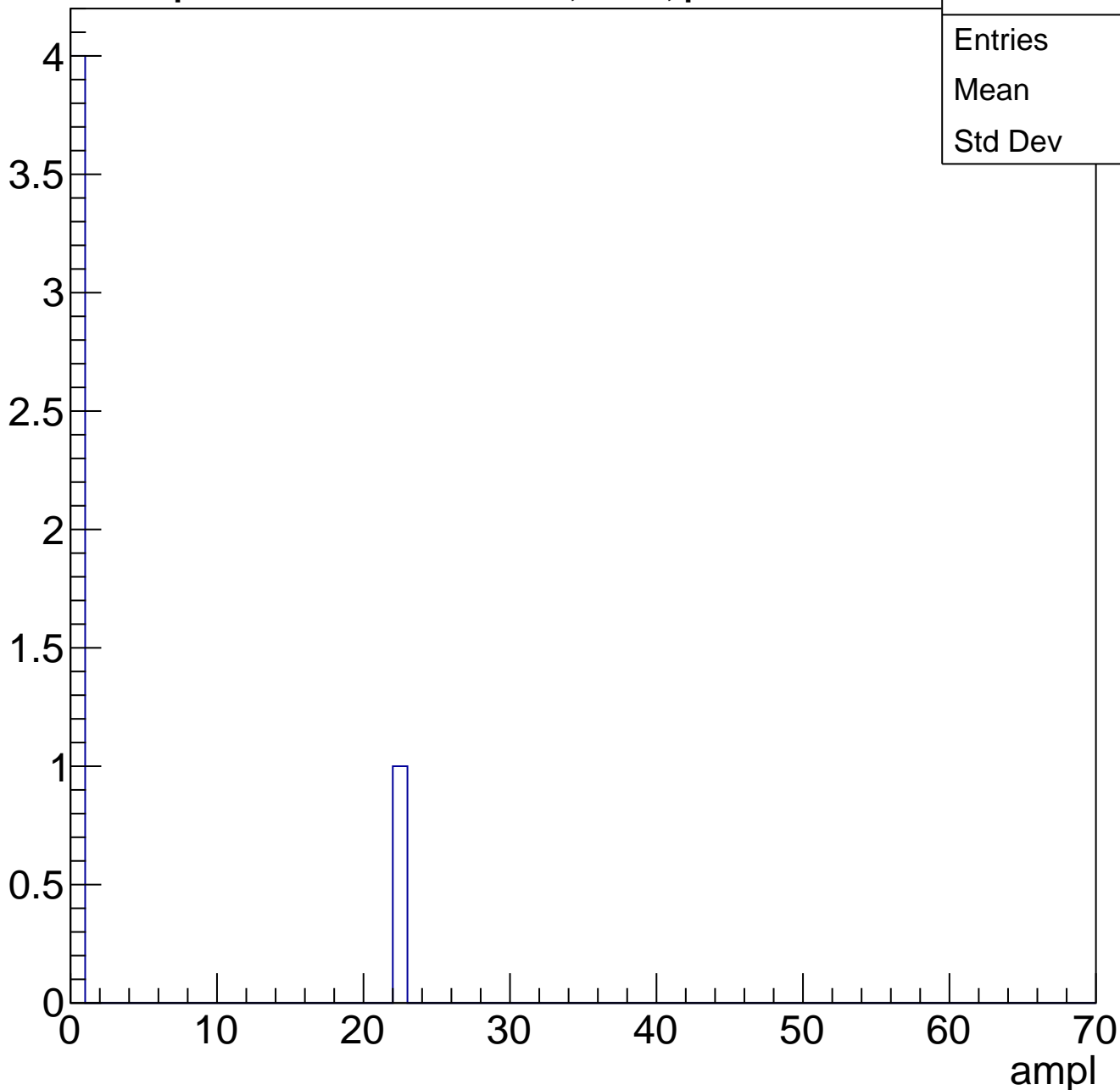
Entries	0
Mean	0
Std Dev	0



# B0L001S, U6-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	5
Mean	4.4
Std Dev	8.8

# B0L001S, U6-ch99, adc0

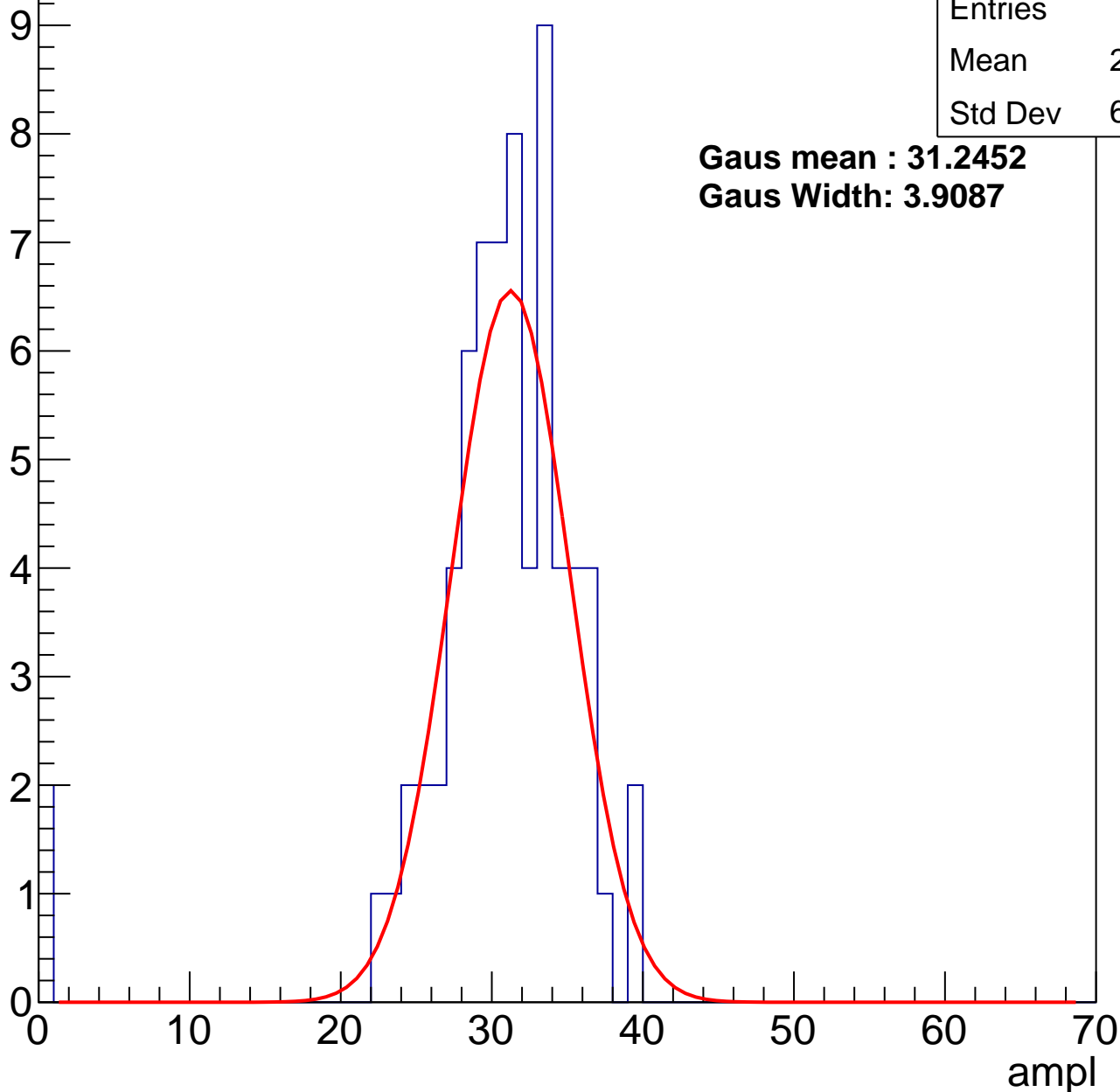
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	29.89
Std Dev	6.276

**Gaus mean : 31.2452**

**Gaus Width: 3.9087**



# B0L001S, U6-ch99, adc1

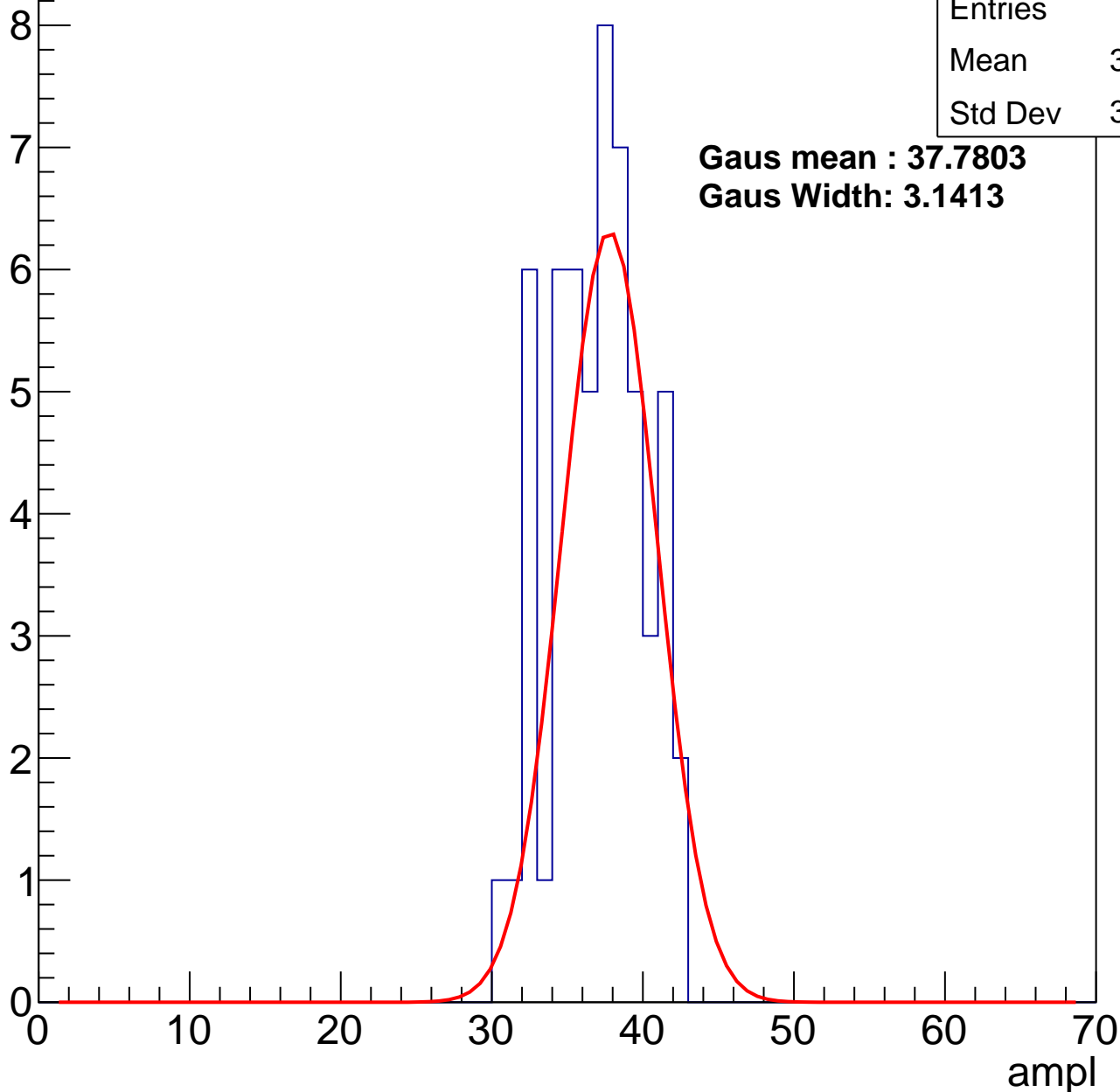
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	36.54
Std Dev	3.006

**Gaus mean : 37.7803**

**Gaus Width: 3.1413**



# B0L001S, U6-ch99, adc2

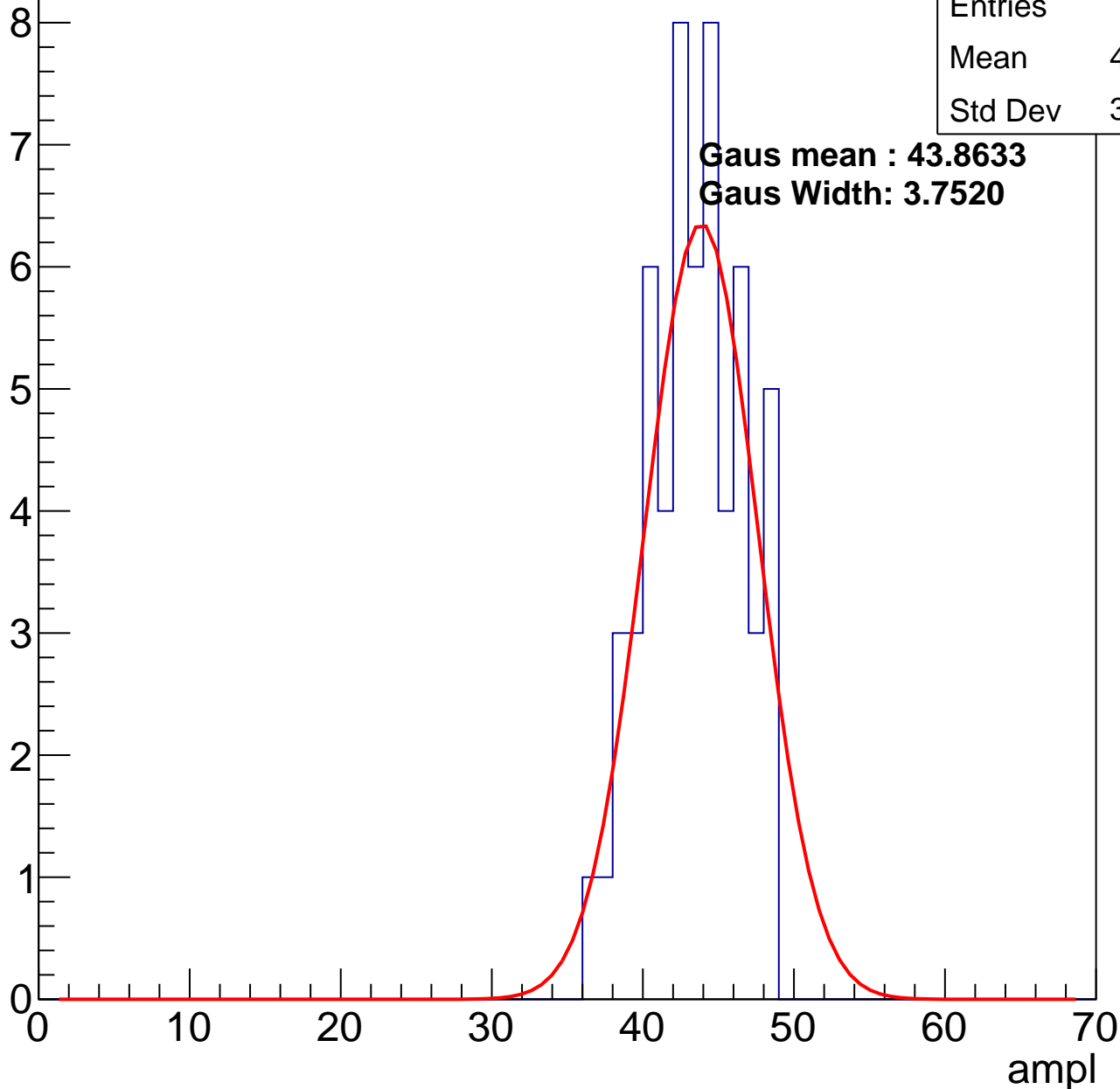
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	42.95
Std Dev	3.042

**Gaus mean : 43.8633**

**Gaus Width: 3.7520**

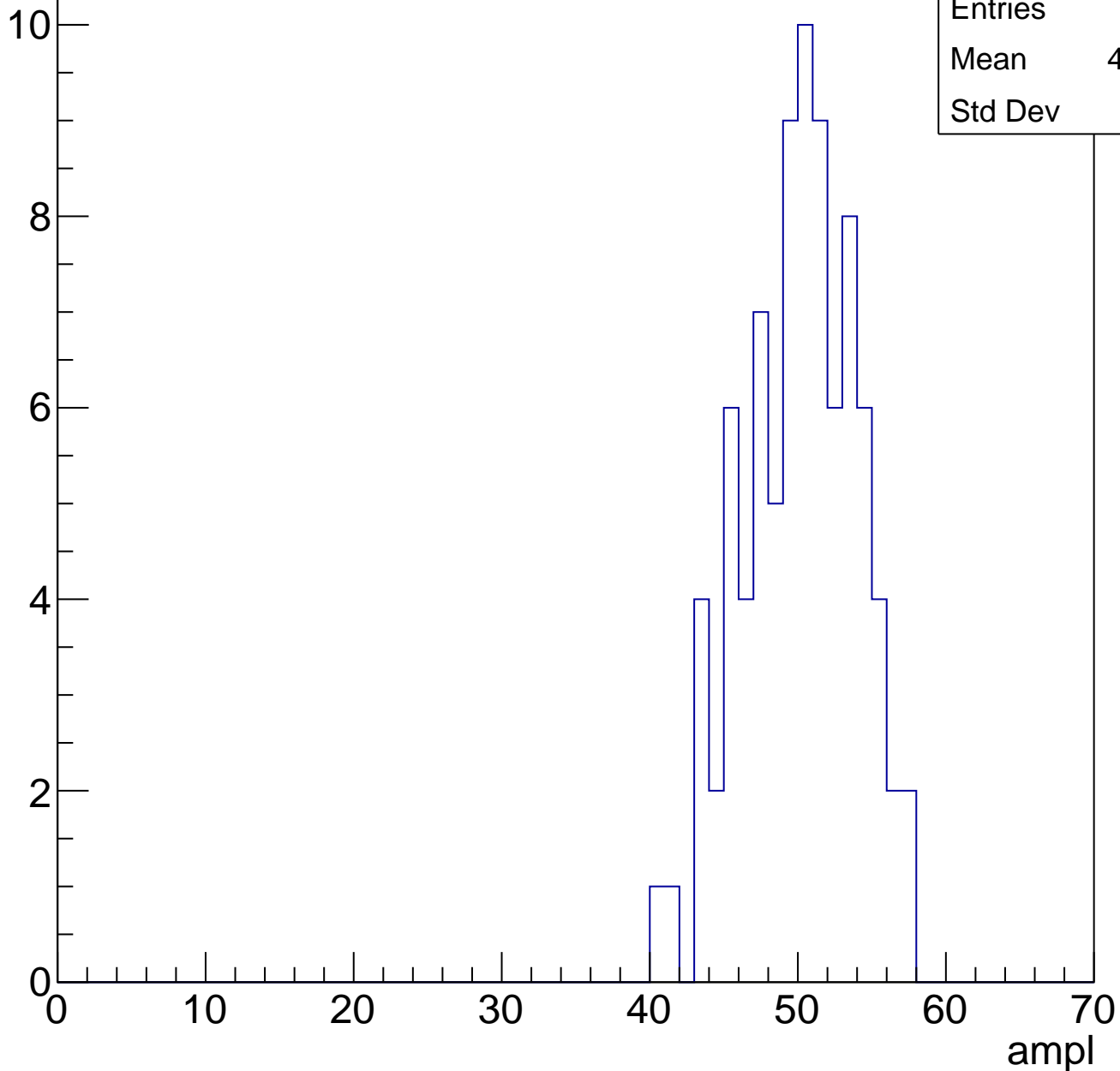


# B0L001S, U6-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	86
Mean	49.65
Std Dev	3.76

Entry

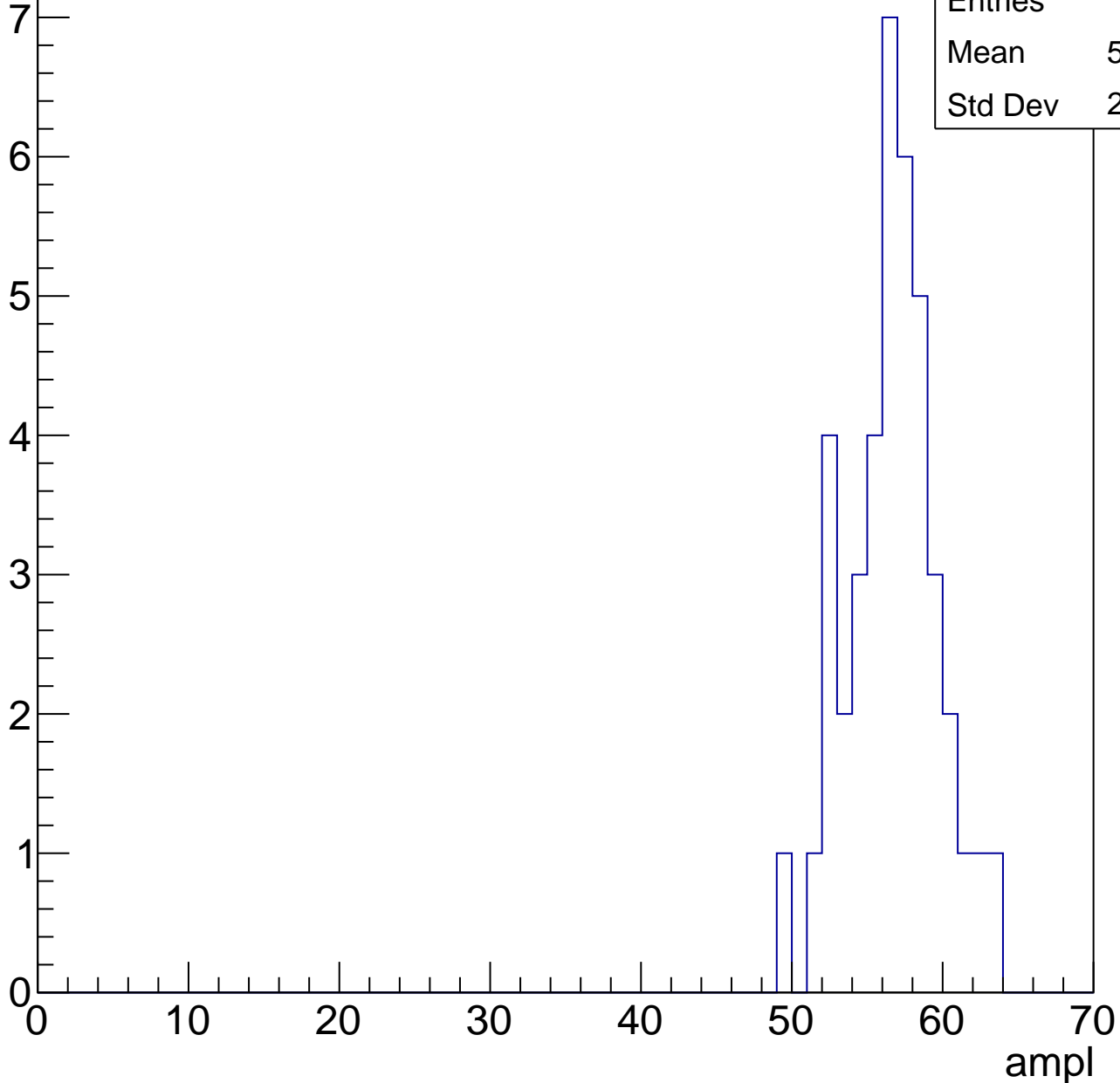


# B0L001S, U6-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

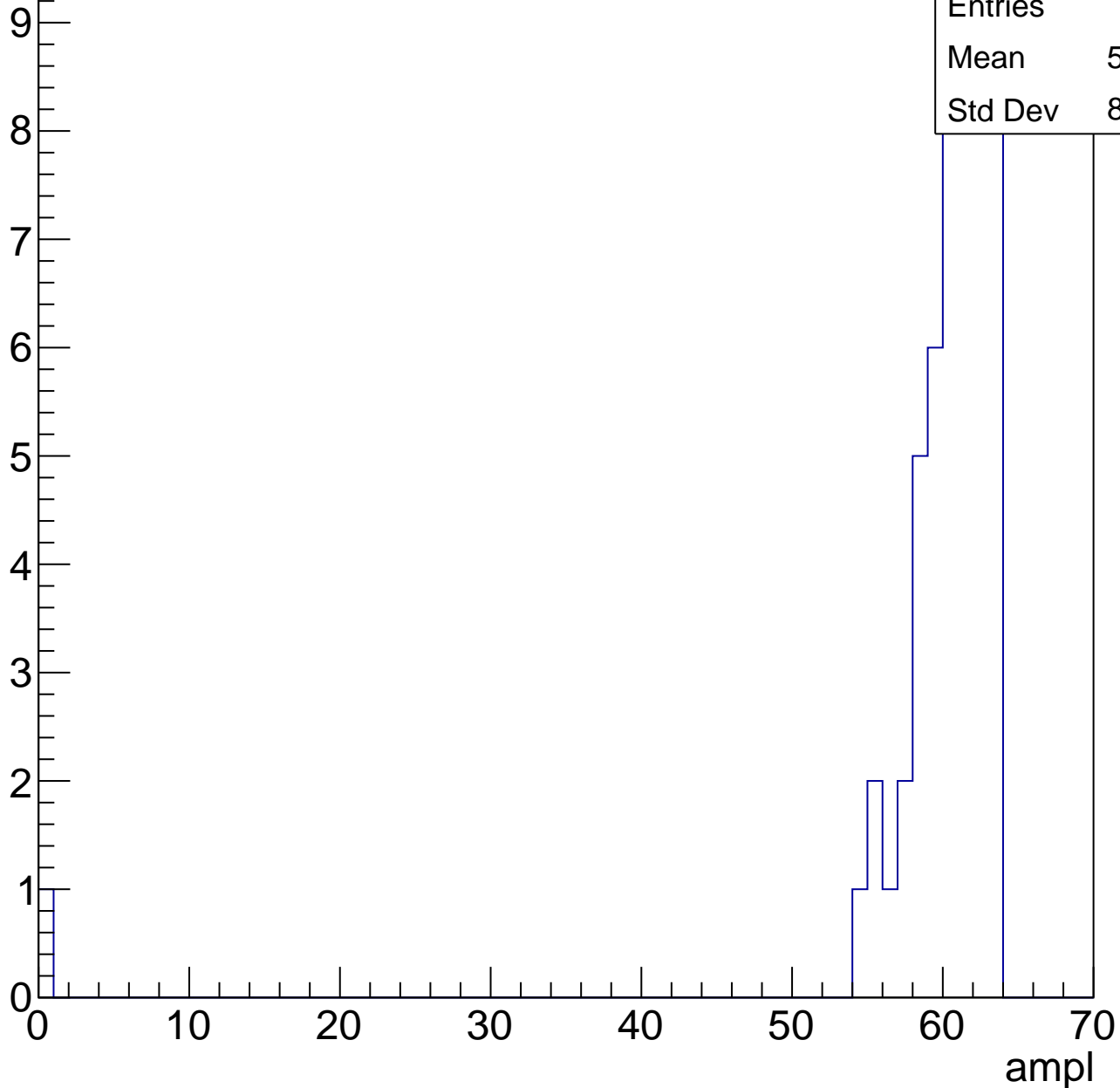
Entries	41
Mean	56.17
Std Dev	2.987



# B0L001S, U6-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

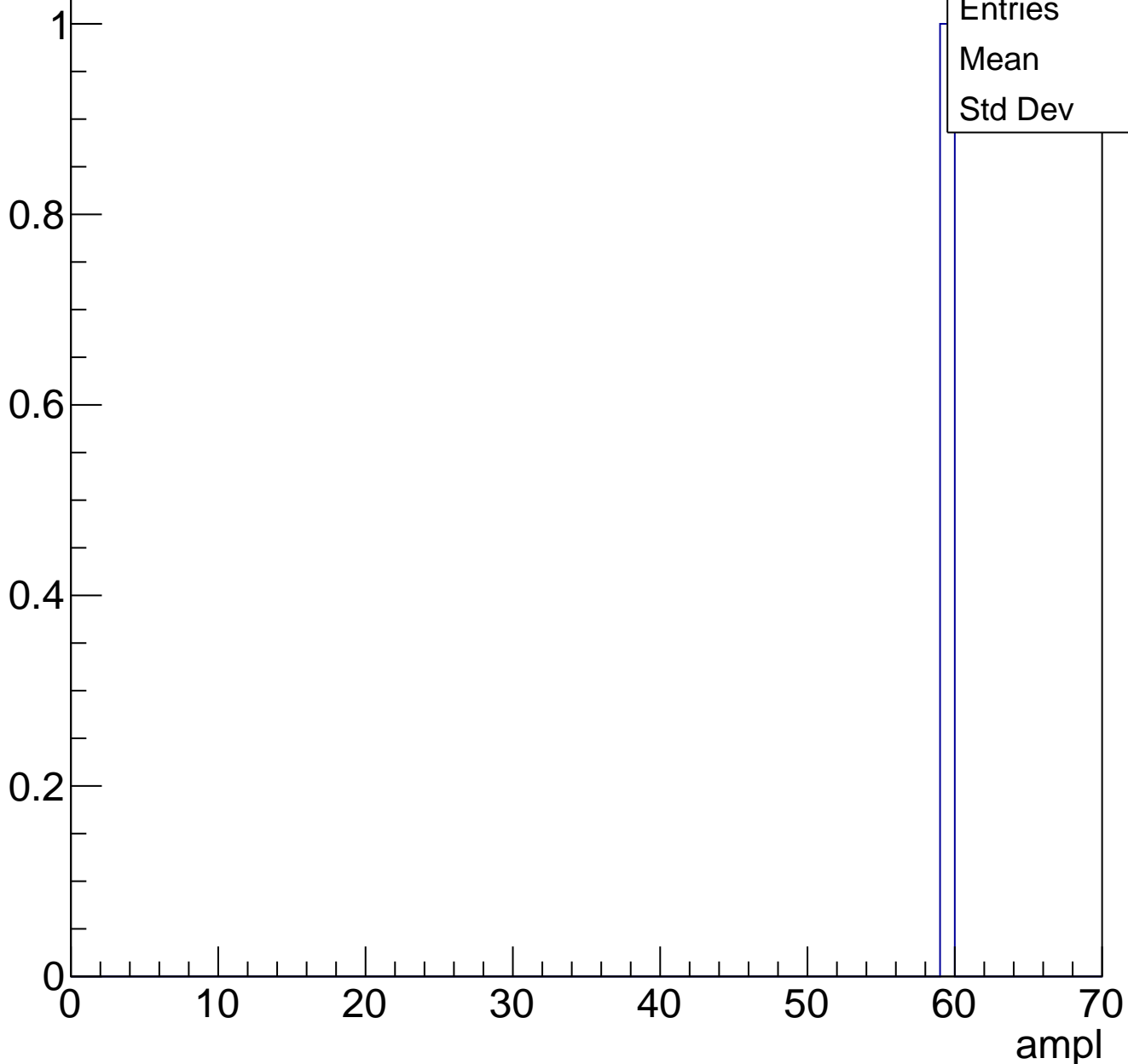
Entry



# B0L001S, U6-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	59
Std Dev	0



# B0L001S, U6-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch100, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	70
Mean	29.93
Std Dev	3.309

**Gaus mean : 30.1255**

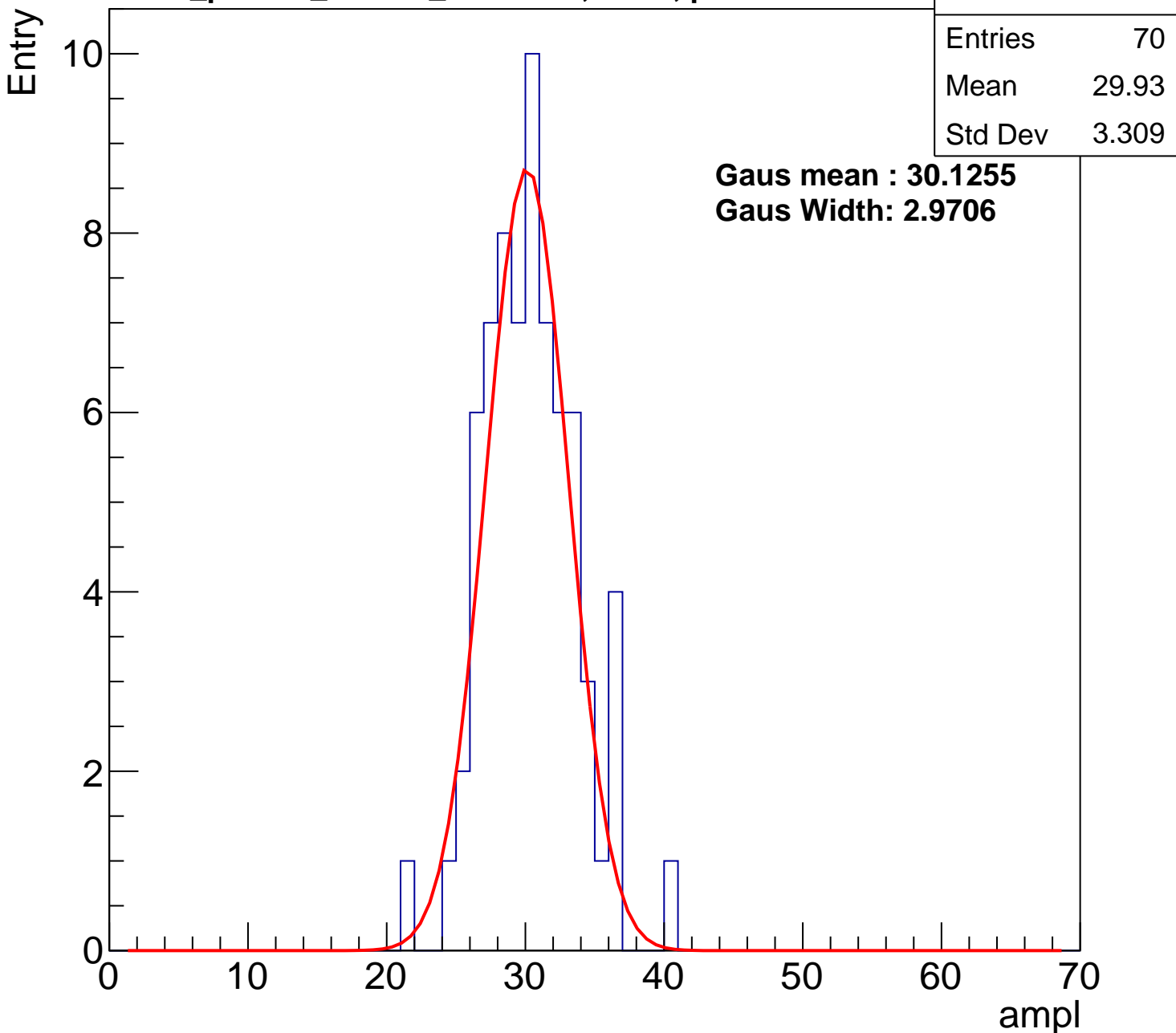
**Gaus Width: 2.9706**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U6-ch100, adc1

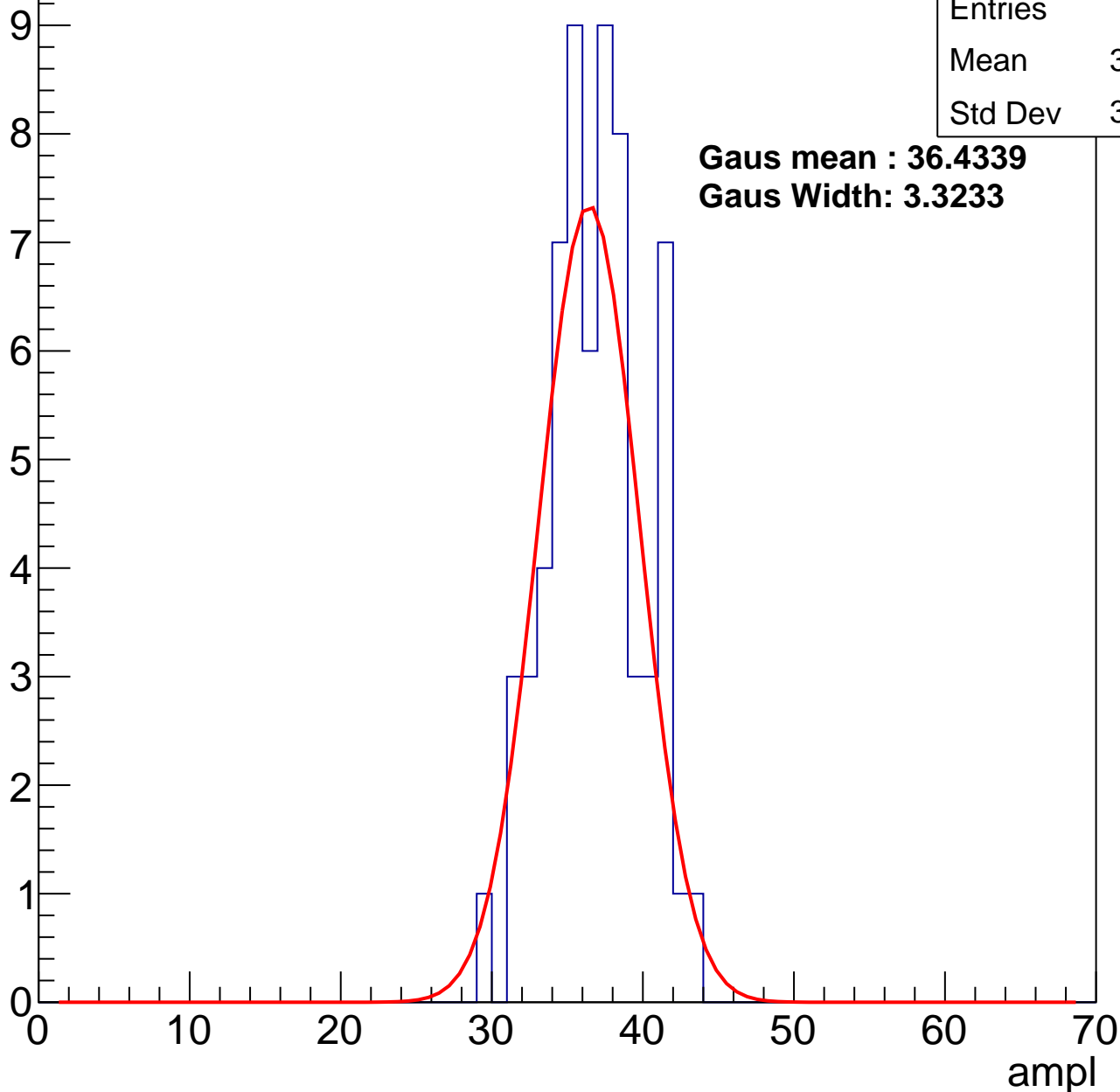
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	36.38
Std Dev	3.067

**Gaus mean : 36.4339**

**Gaus Width: 3.3233**



# B0L001S, U6-ch100, adc2

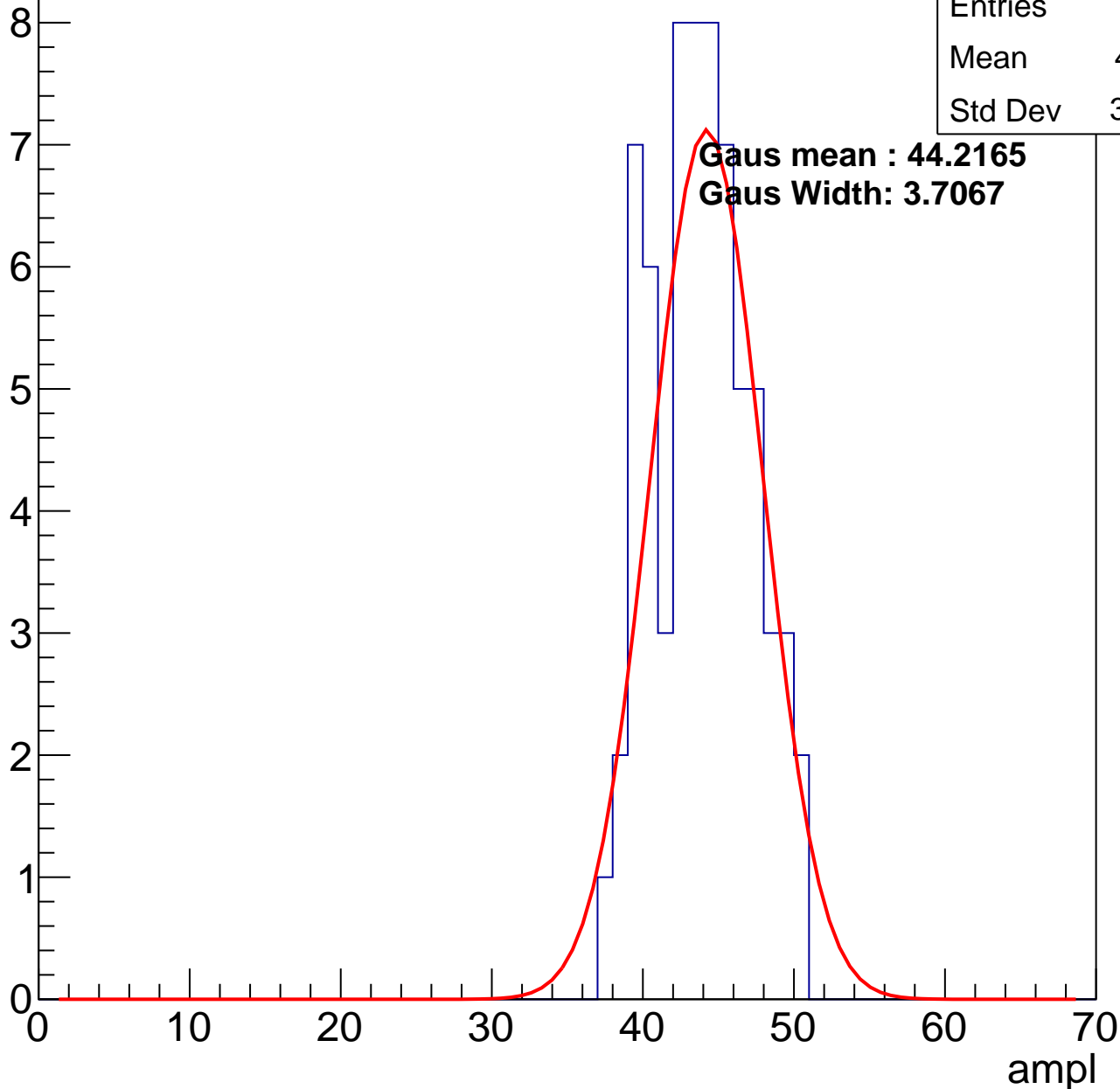
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	43.41
Std Dev	3.214

**Gaus mean : 44.2165**

**Gaus Width: 3.7067**

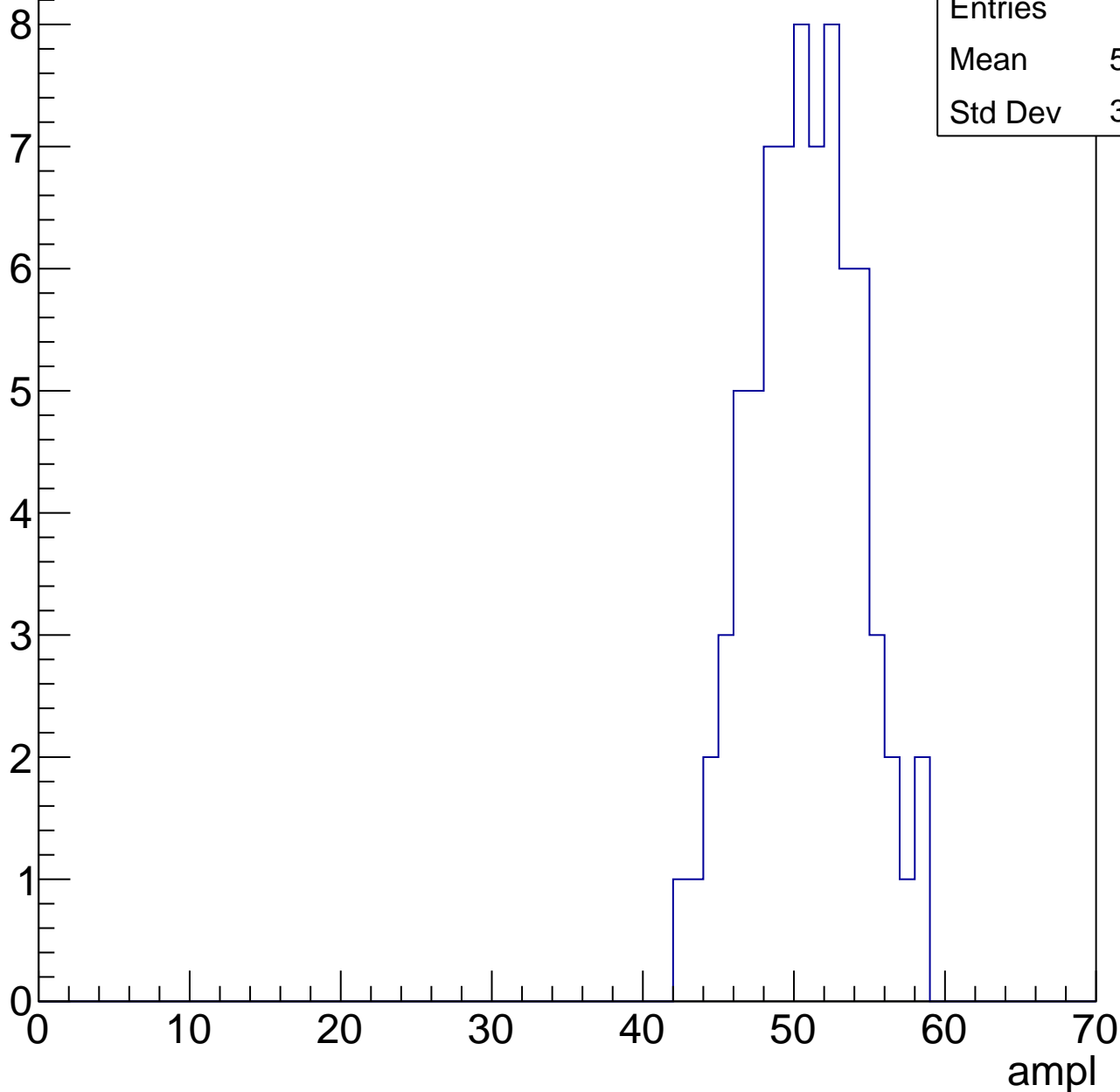


# B0L001S, U6-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

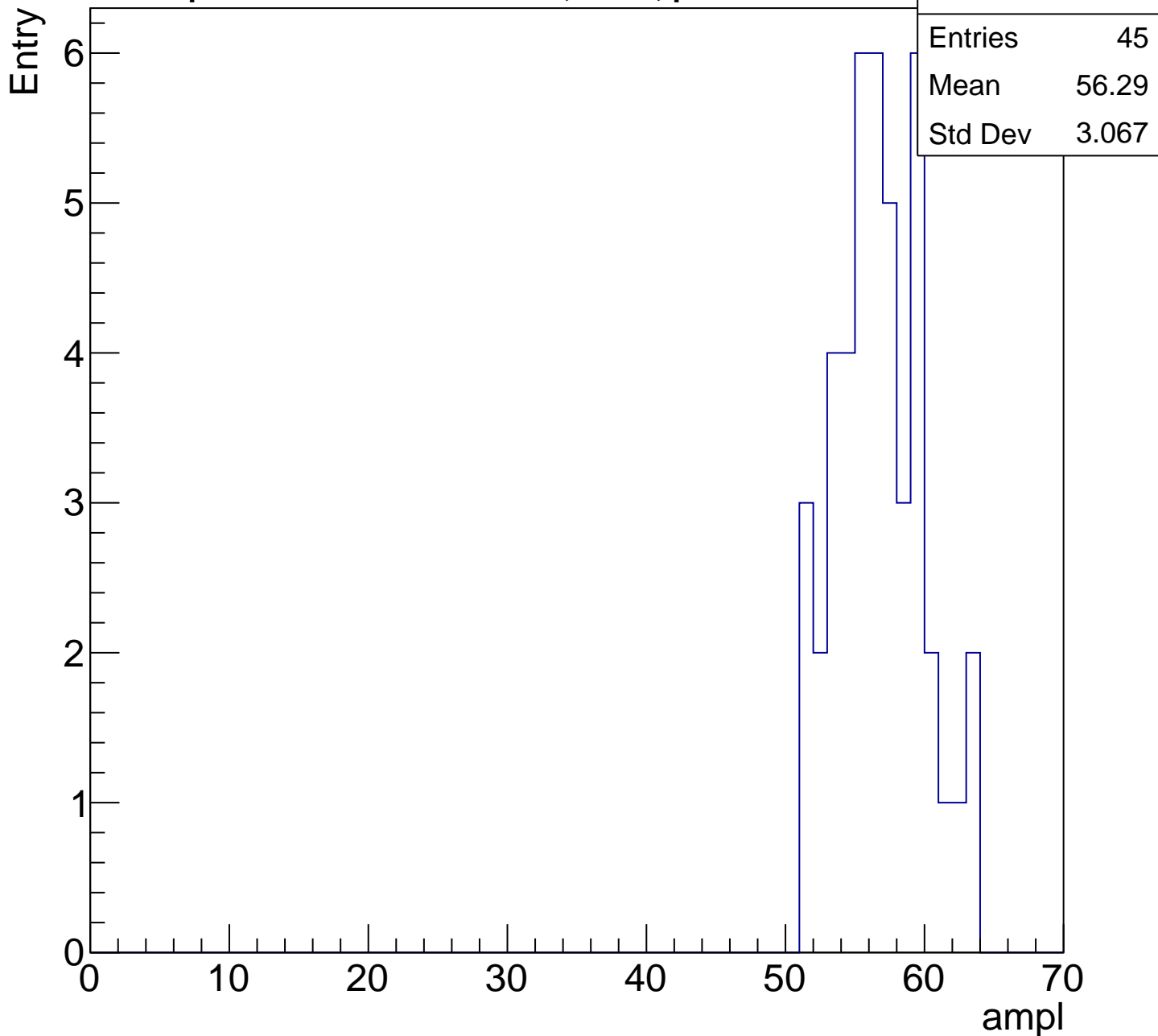
Entry

Entries	74
Mean	50.23
Std Dev	3.543



# B0L001S, U6-ch100, adc4

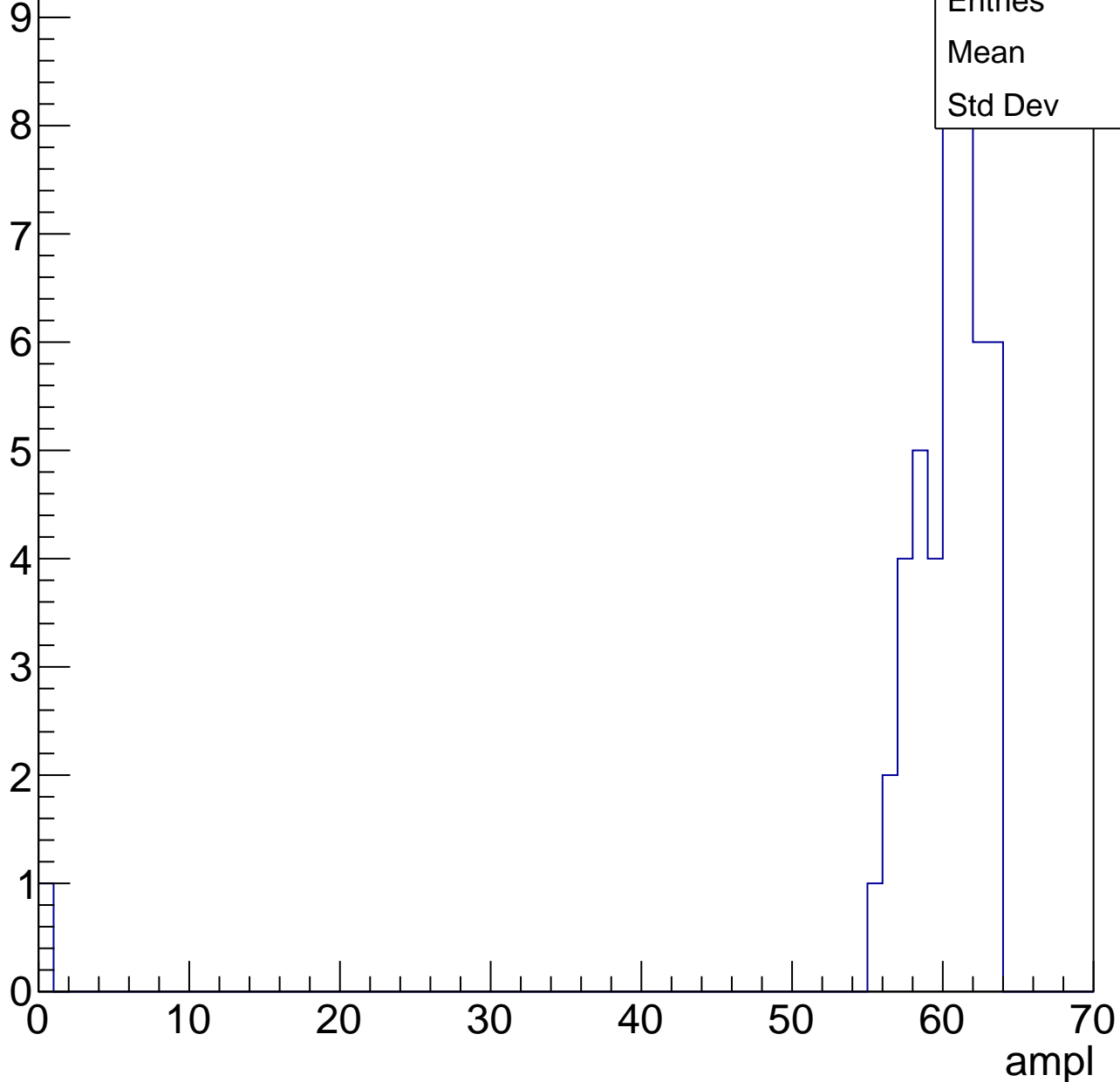
calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U6-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

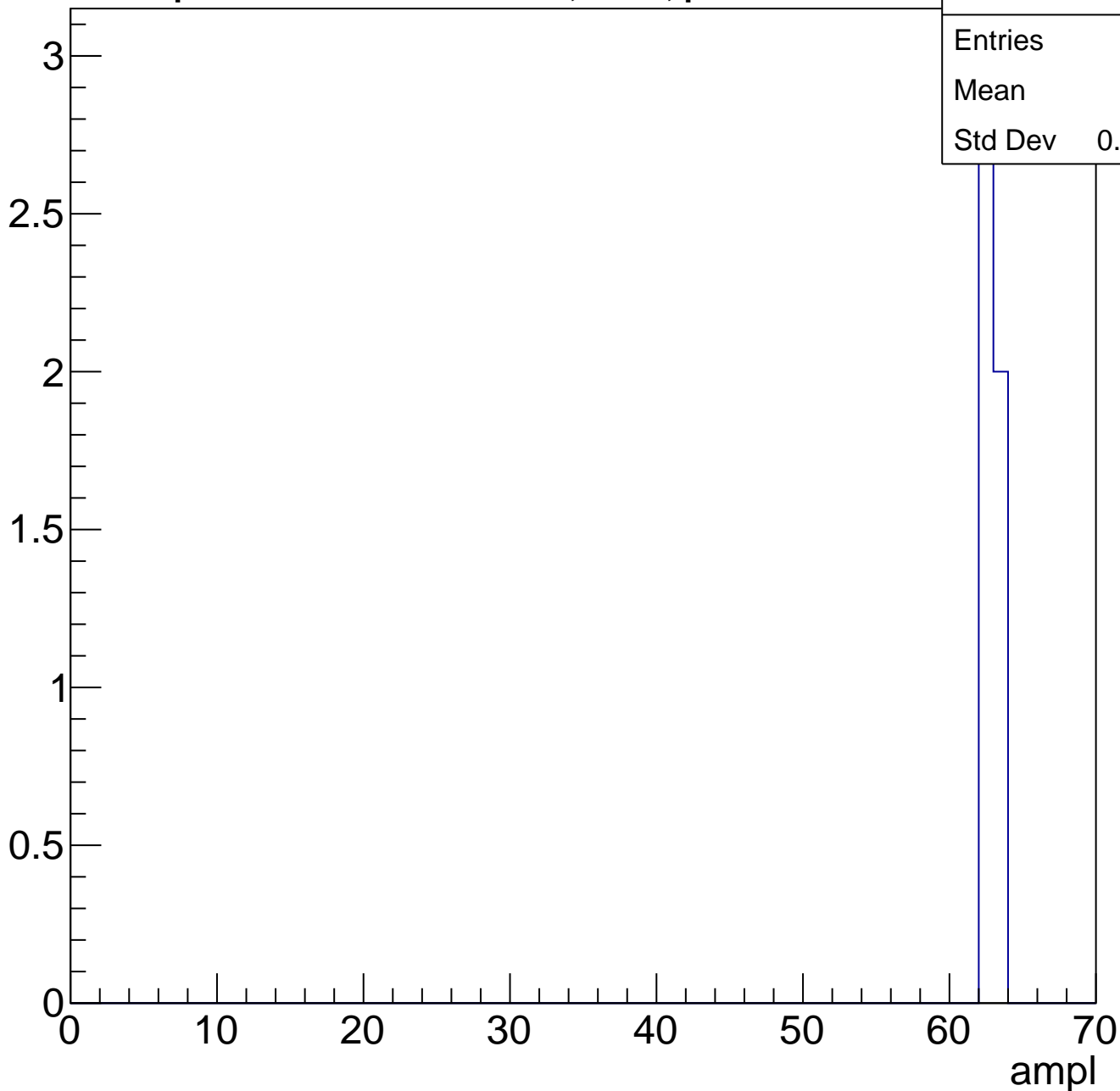
Entry



# B0L001S, U6-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U6-ch101, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	89
Mean	29.93
Std Dev	5.599

**Gaus mean : 31.0886**

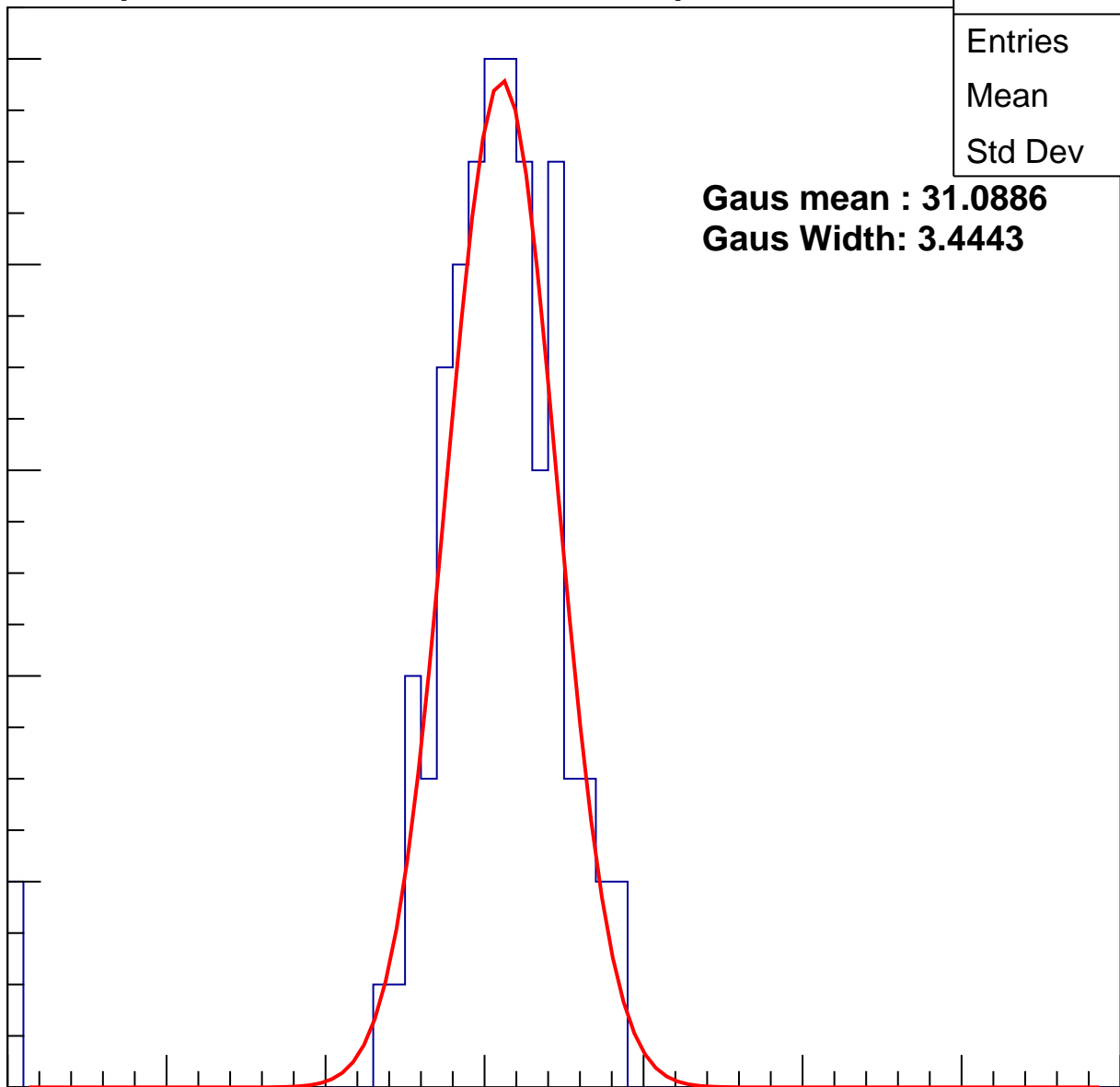
**Gaus Width: 3.4443**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U6-ch101, adc1

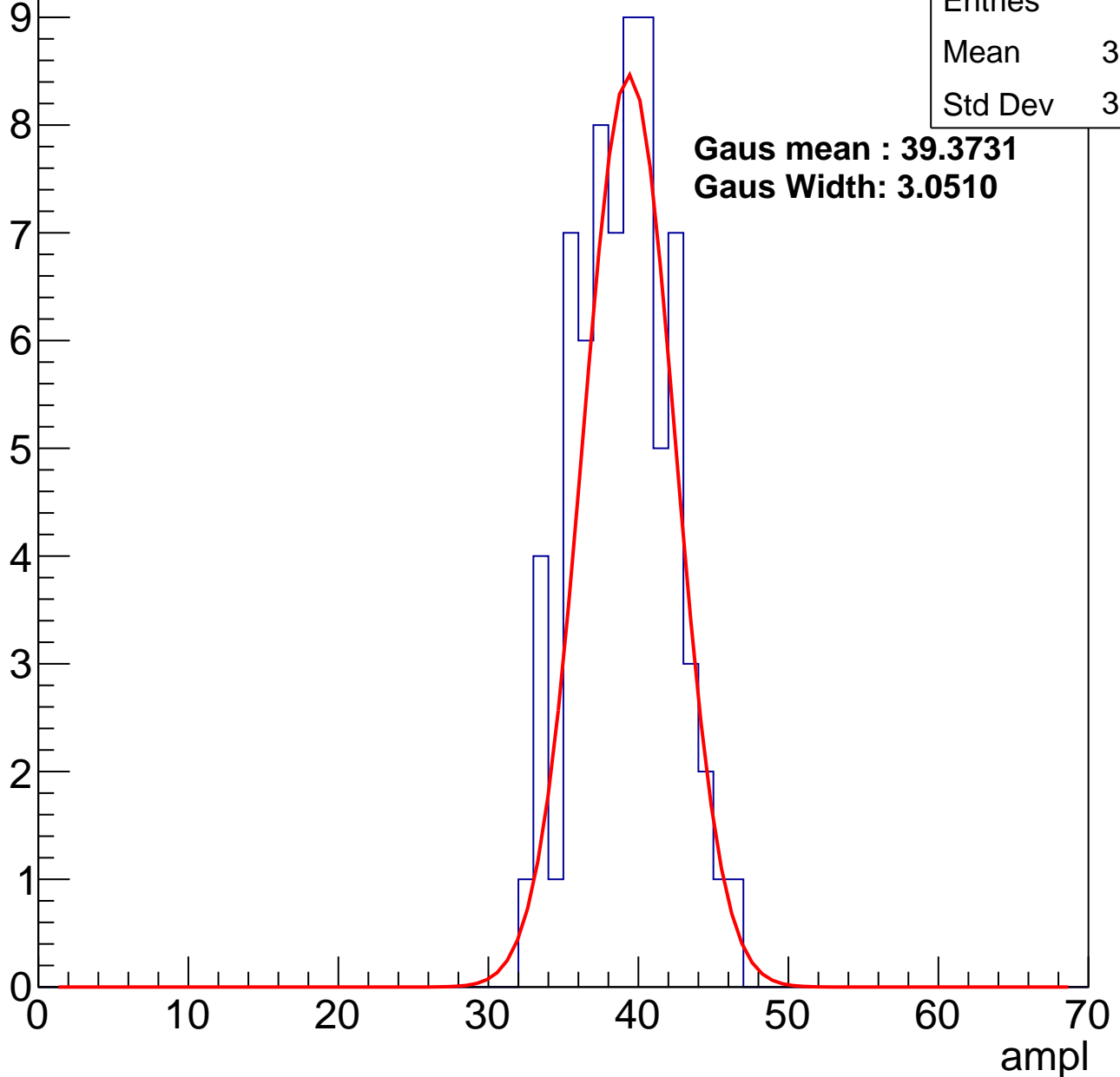
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	38.58
Std Dev	3.107

**Gaus mean : 39.3731**

**Gaus Width: 3.0510**

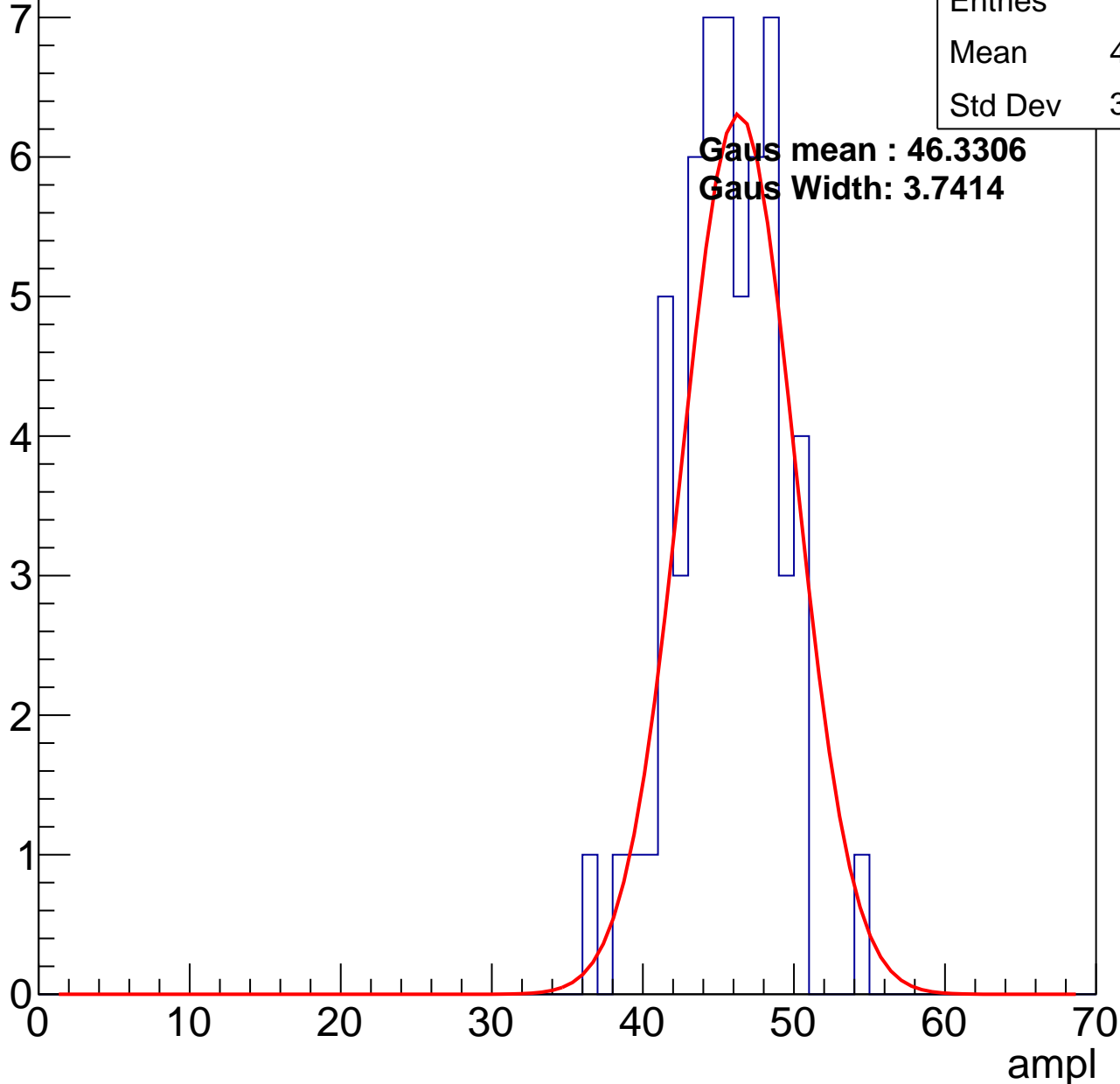


# B0L001S, U6-ch101, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	45.07
Std Dev	3.347

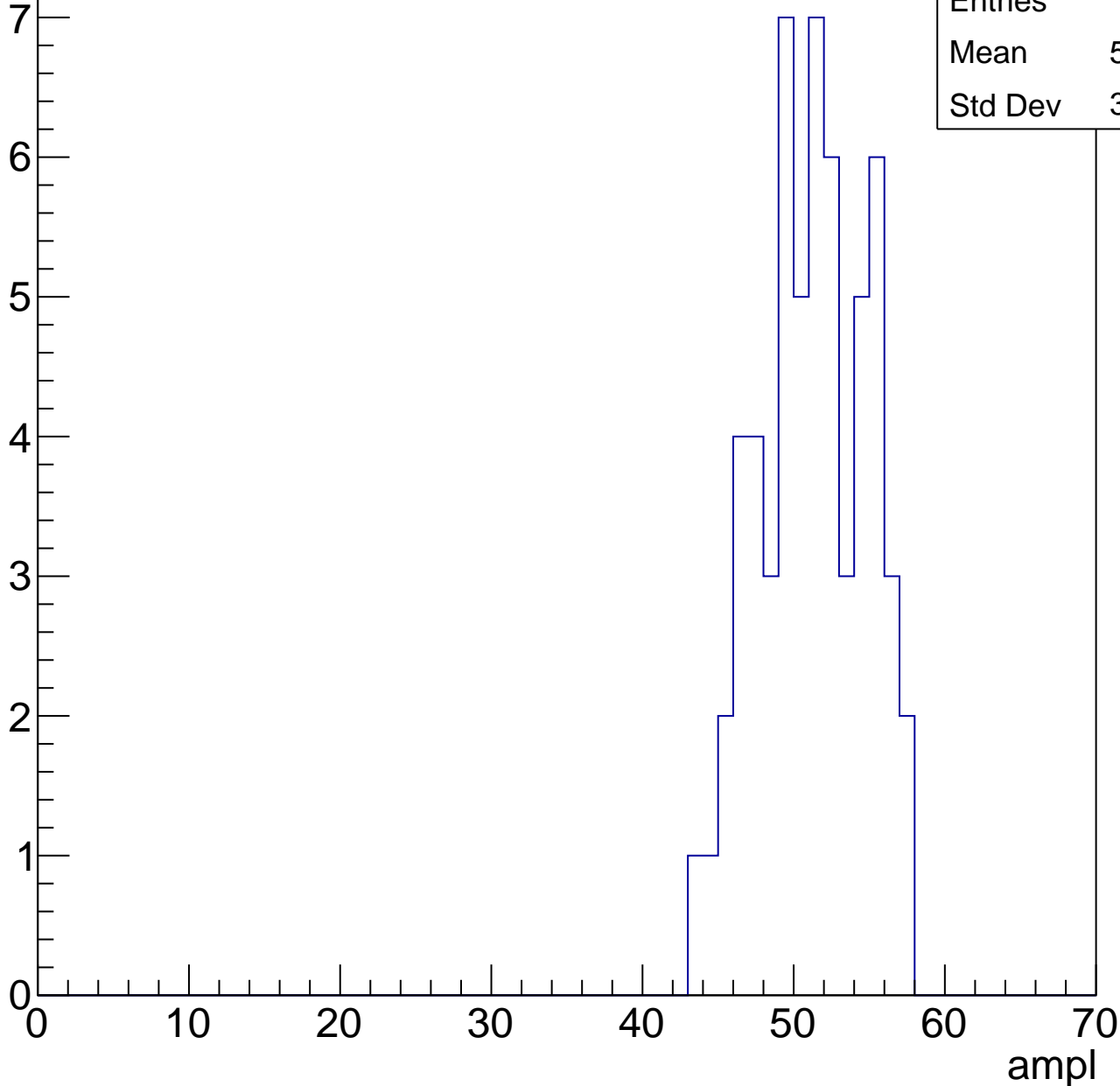


# B0L001S, U6-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	50.78
Std Dev	3.474

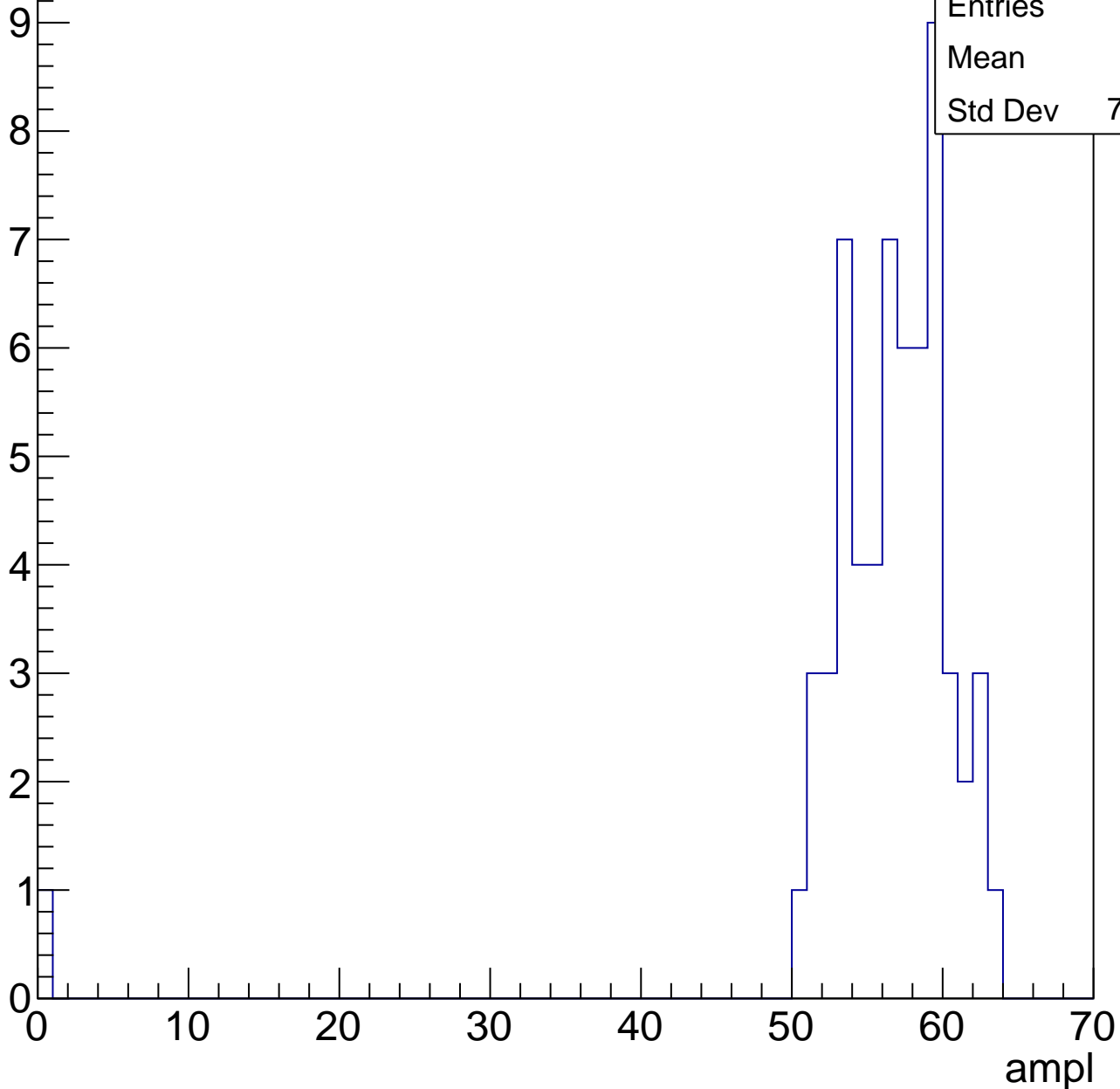


# B0L001S, U6-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	55.5
Std Dev	7.884

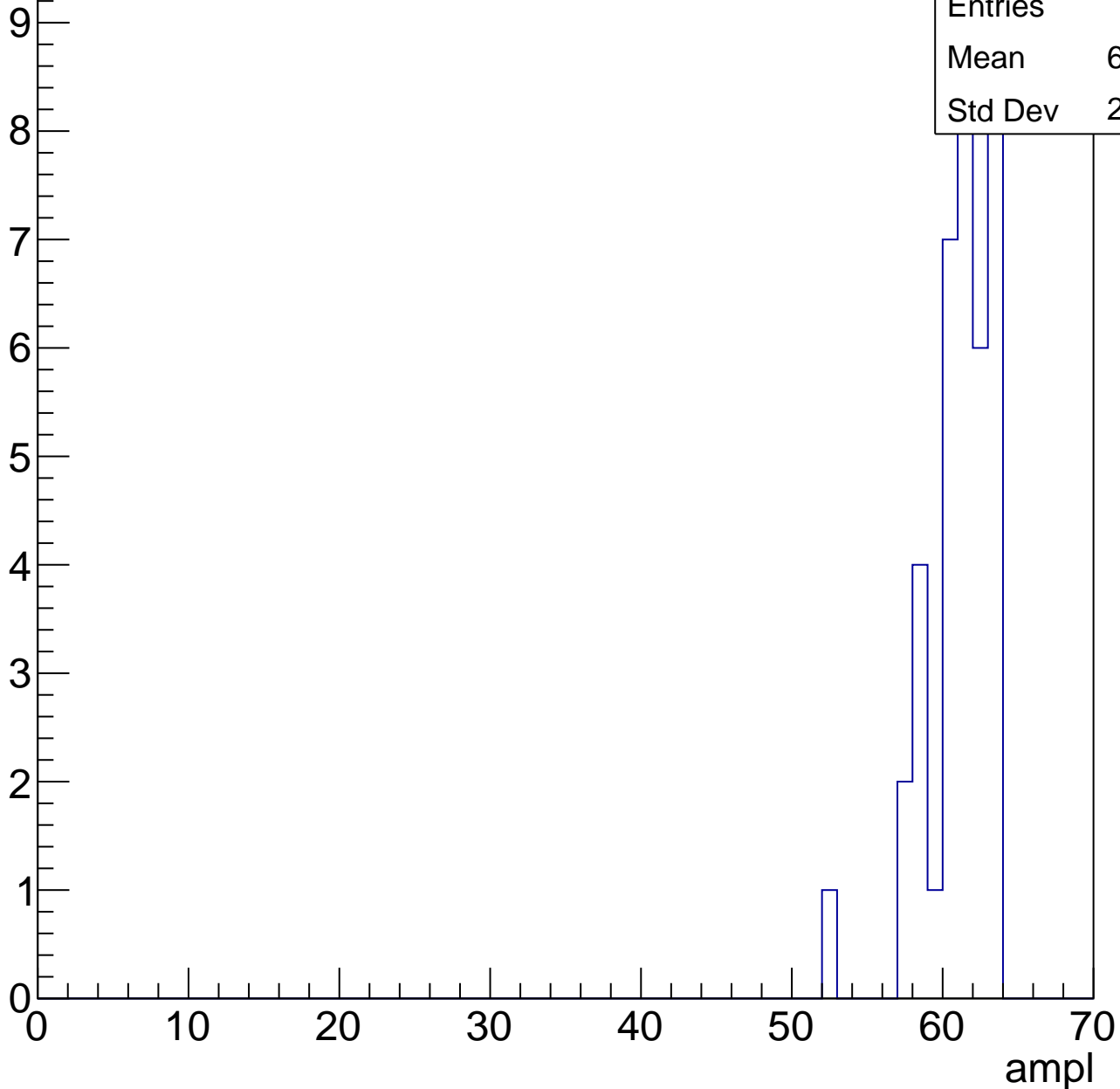


# B0L001S, U6-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	38
Mean	60.63
Std Dev	2.276



# B0L001S, U6-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	22
Std Dev	0

# B0L001S, U6-ch102, adc0

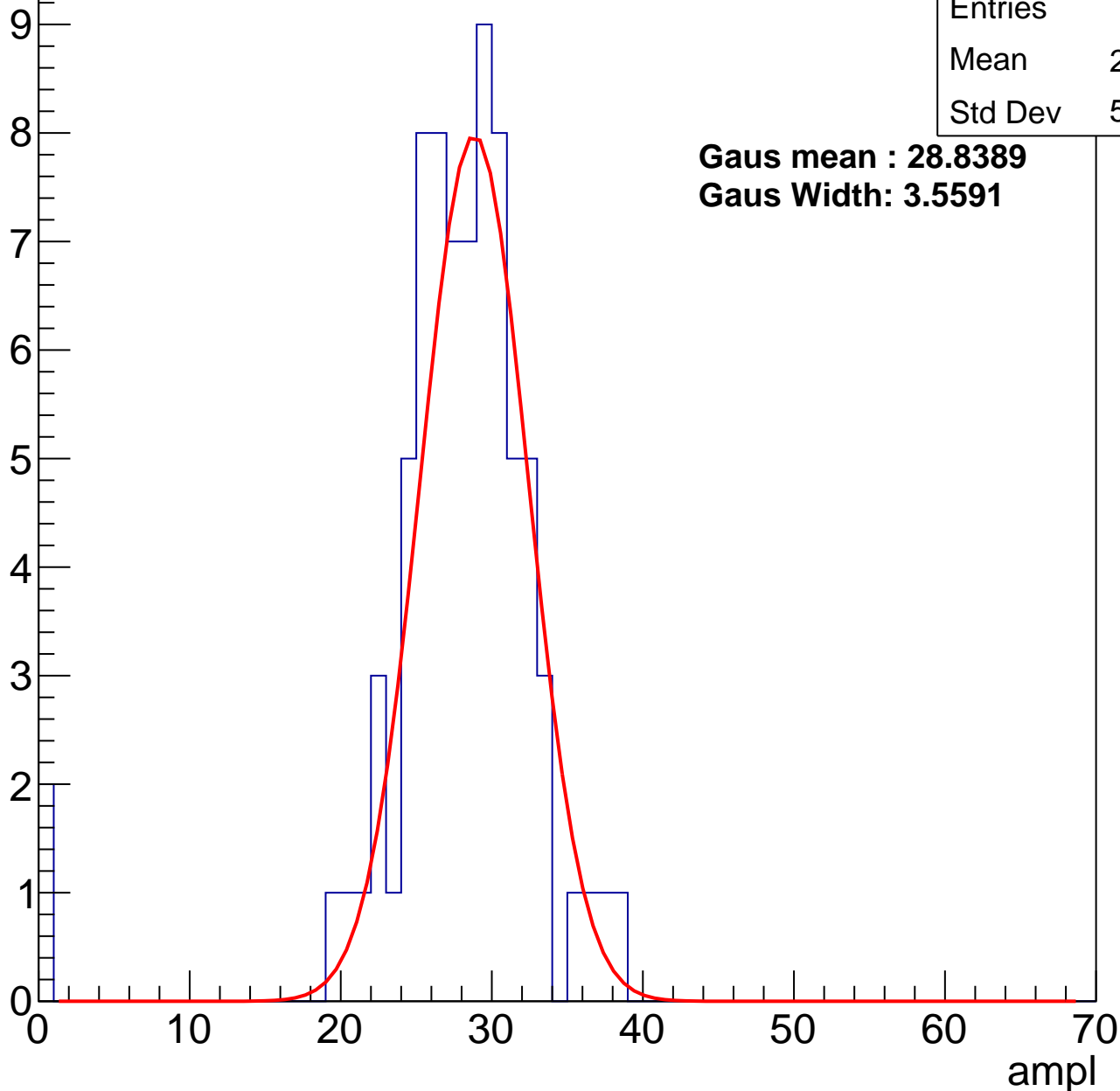
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	27.22
Std Dev	5.744

**Gaus mean : 28.8389**

**Gaus Width: 3.5591**



# B0L001S, U6-ch102, adc1

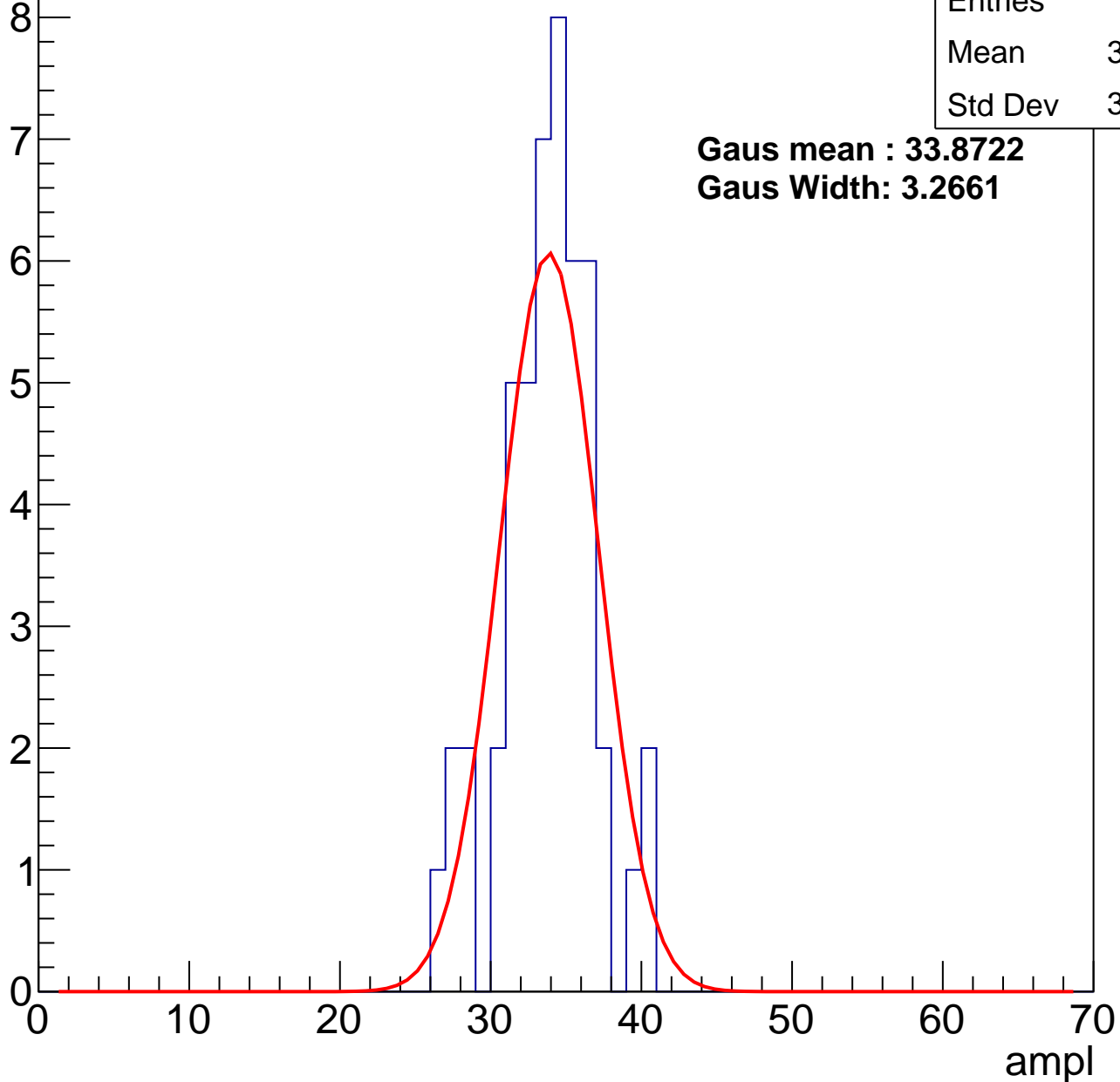
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	33.33
Std Dev	3.067

**Gaus mean : 33.8722**

**Gaus Width: 3.2661**



# B0L001S, U6-ch102, adc2

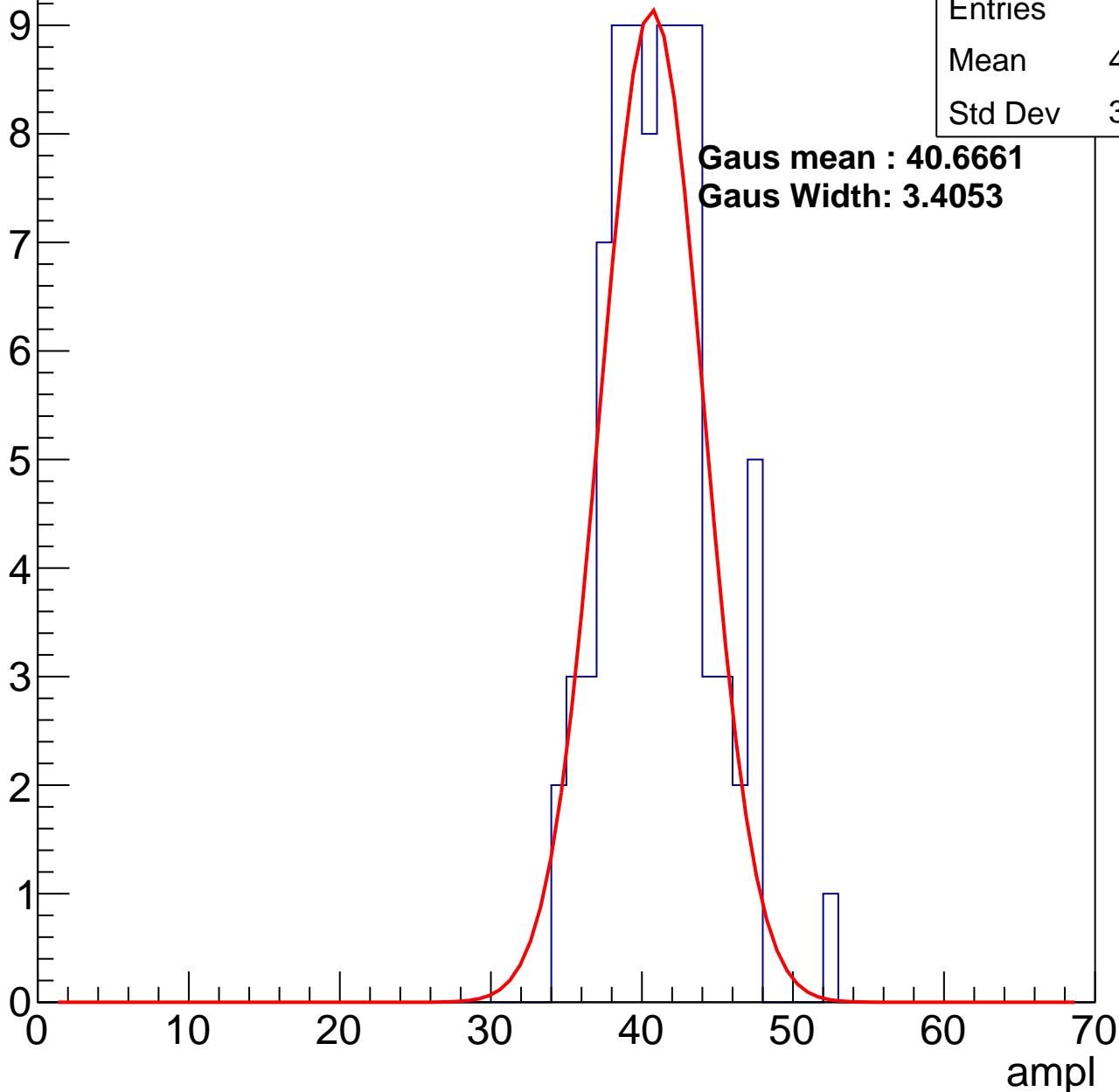
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	82
Mean	40.65
Std Dev	3.455

**Gaus mean : 40.6661**

**Gaus Width: 3.4053**

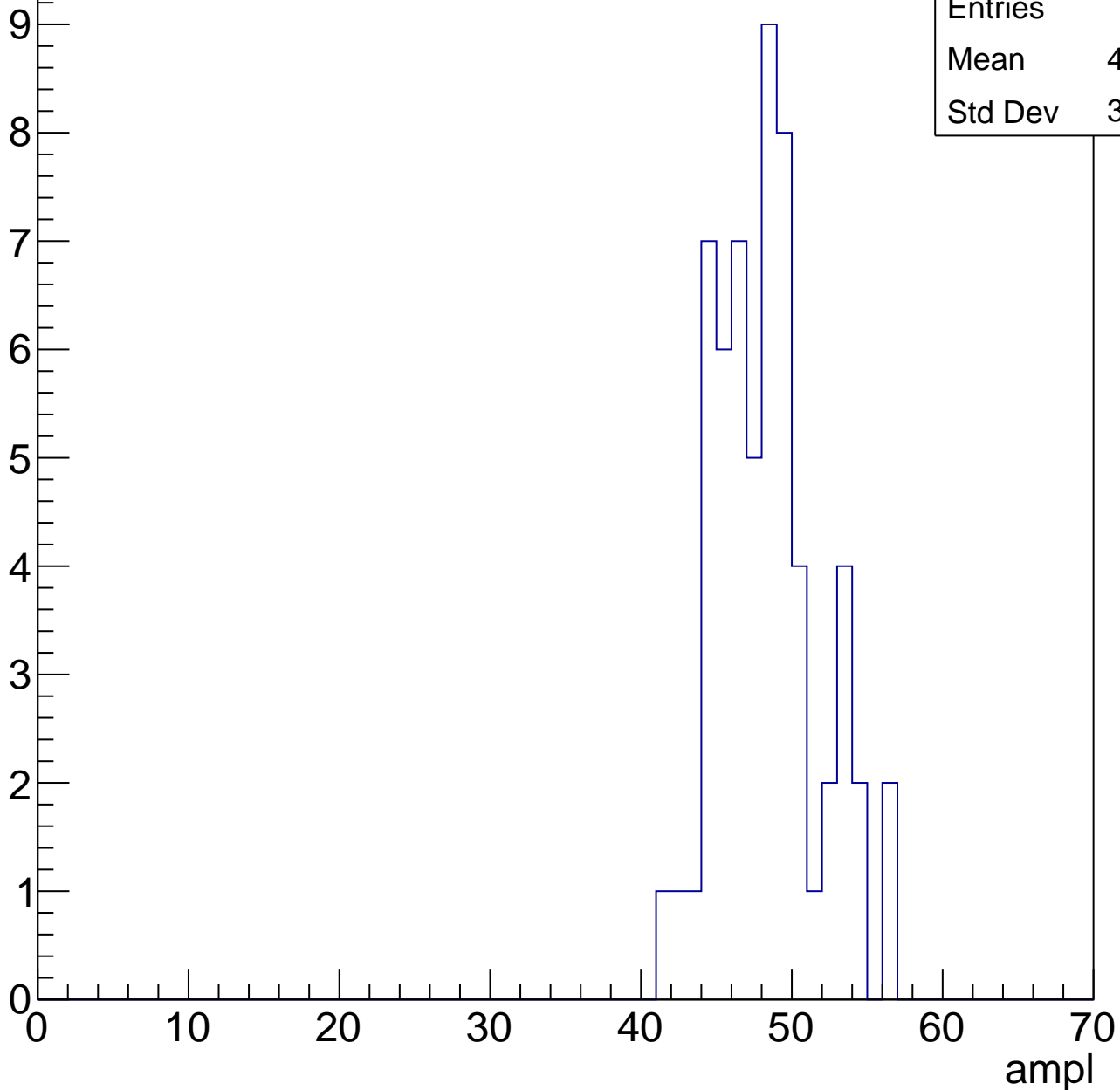


# B0L001S, U6-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	47.87
Std Dev	3.349

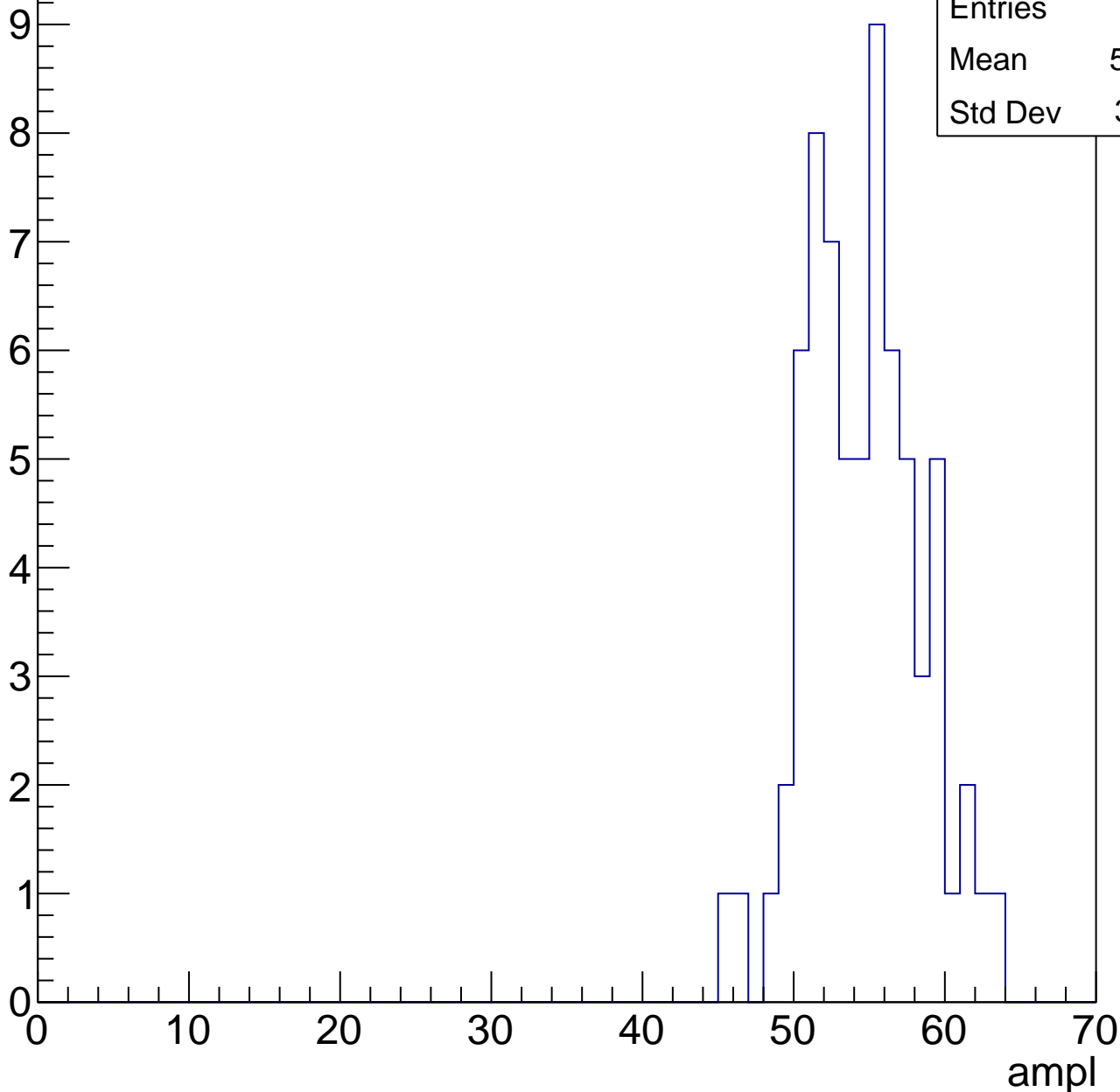


# B0L001S, U6-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	54.14
Std Dev	3.731

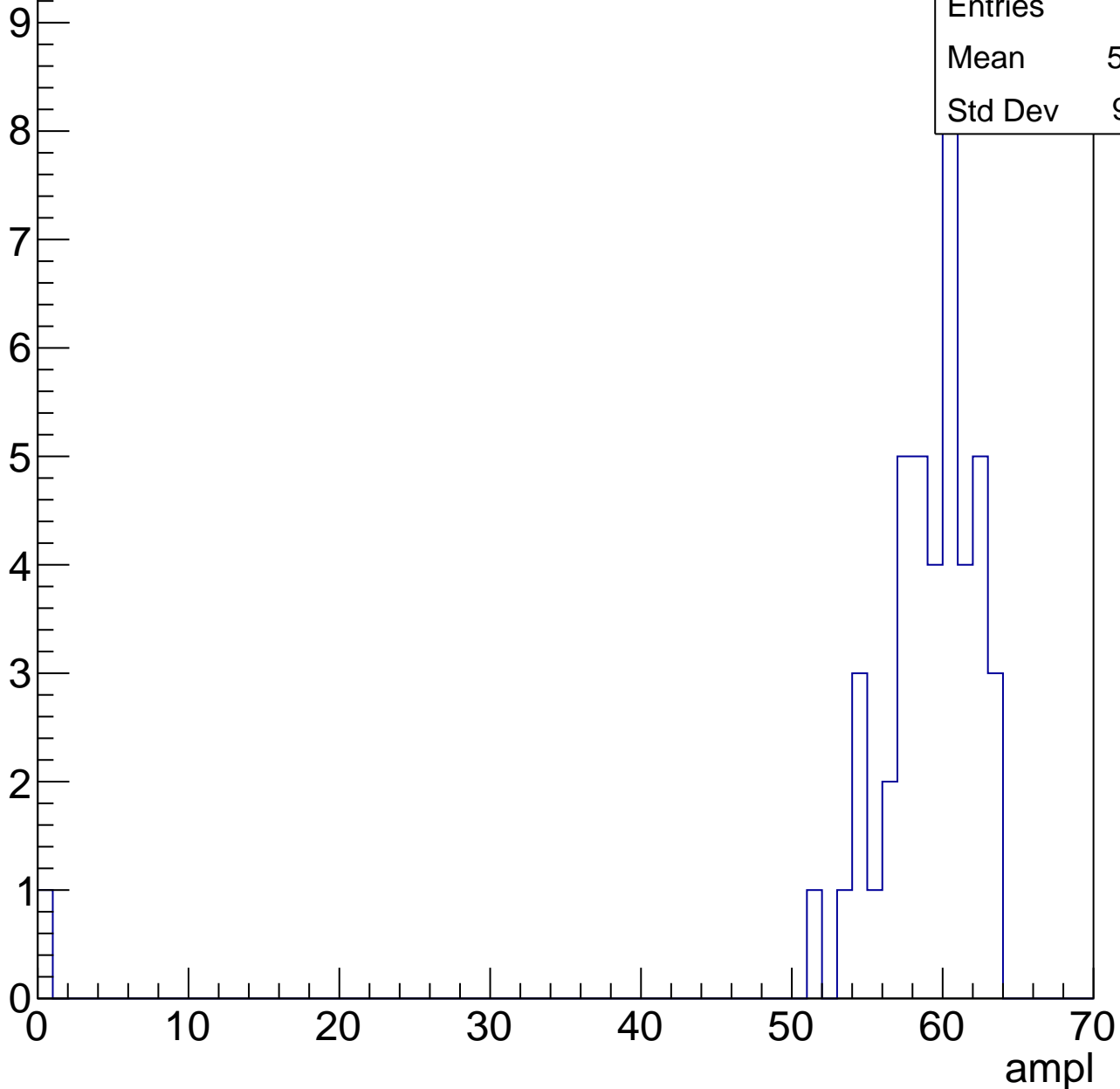


# B0L001S, U6-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	44
Mean	57.43
Std Dev	9.201

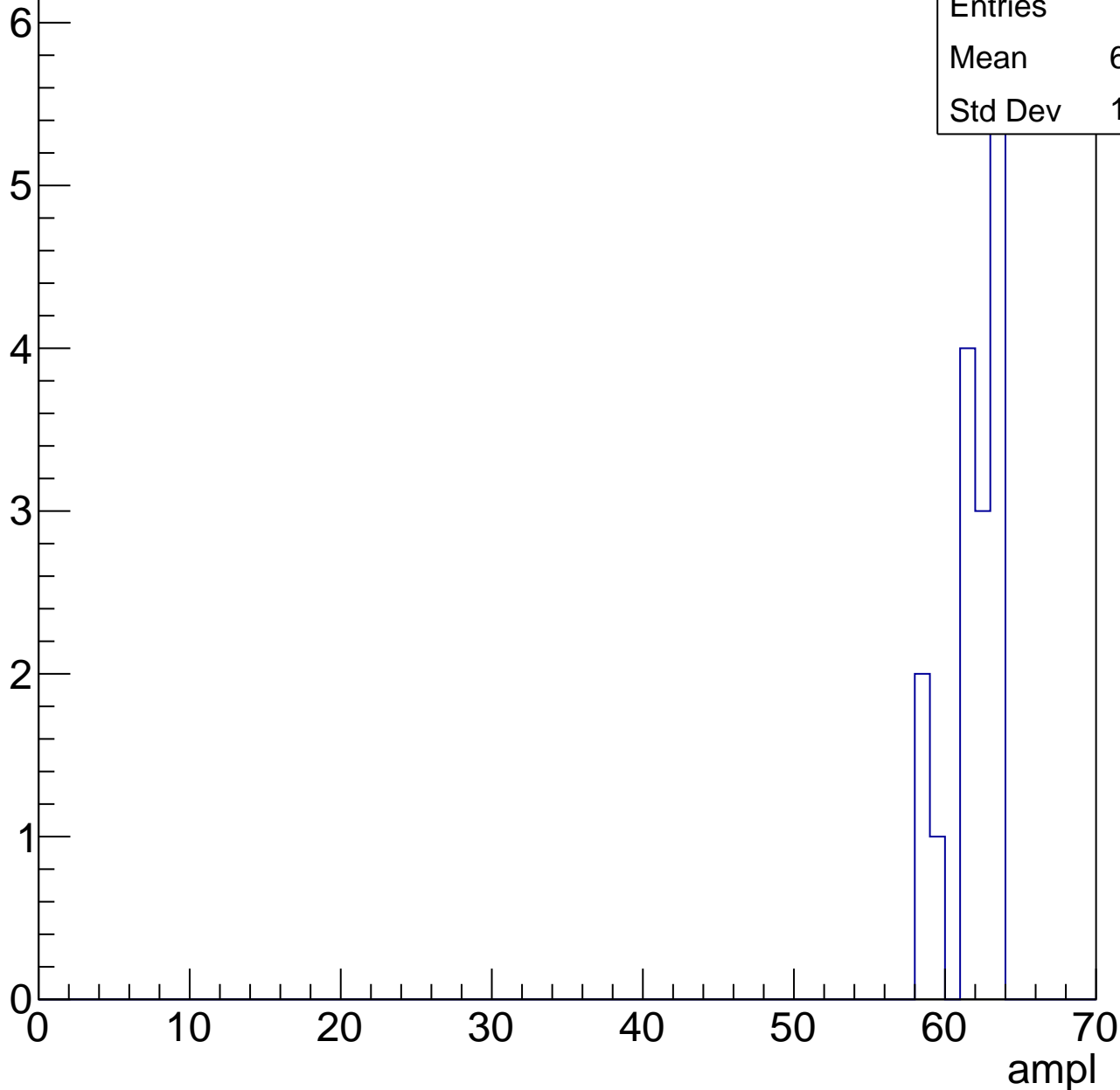


# B0L001S, U6-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	16
Mean	61.44
Std Dev	1.694





# B0L001S, U6-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch103, adc0

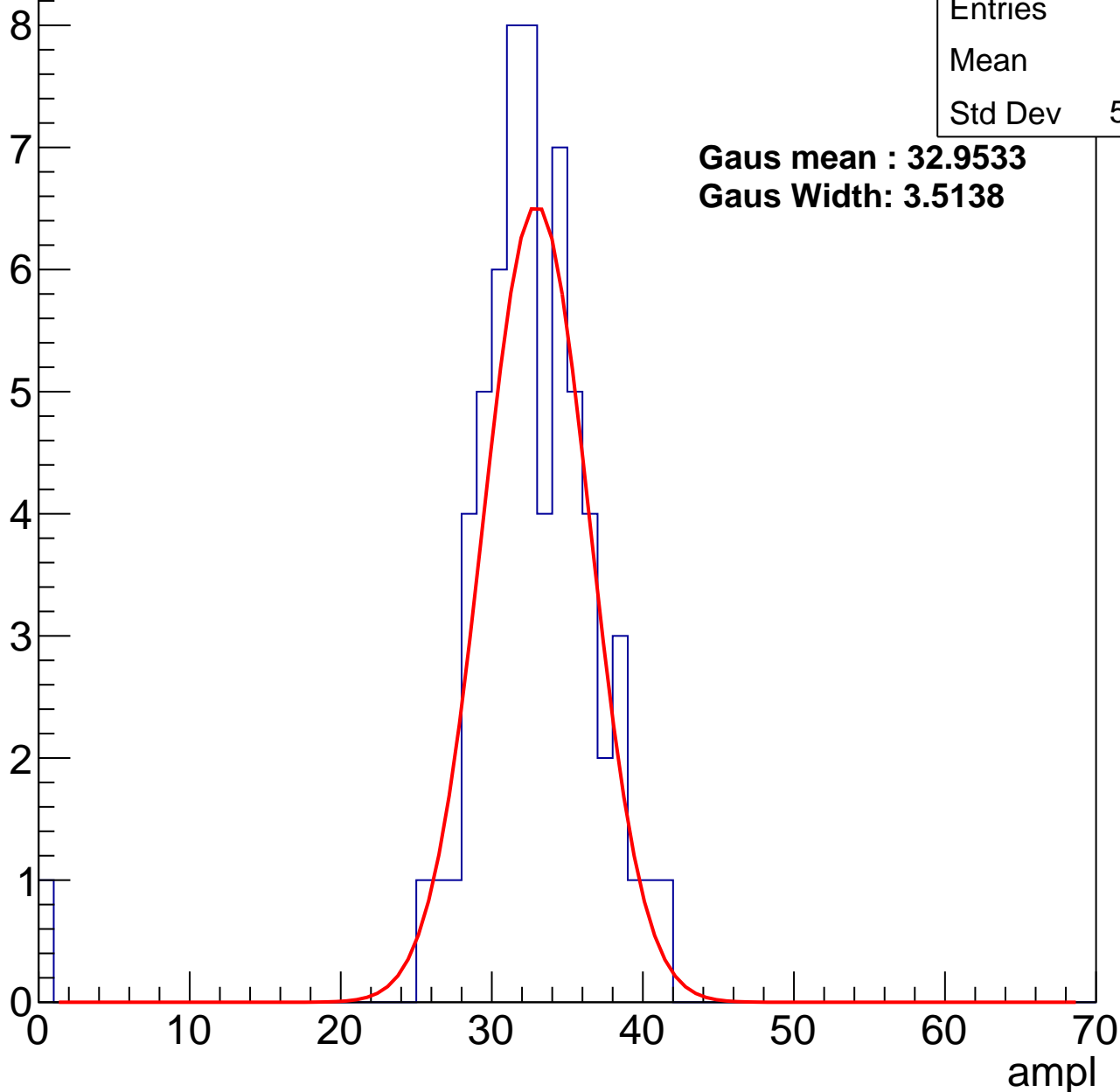
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	32
Std Dev	5.297

**Gaus mean : 32.9533**

**Gaus Width: 3.5138**



# B0L001S, U6-ch103, adc1

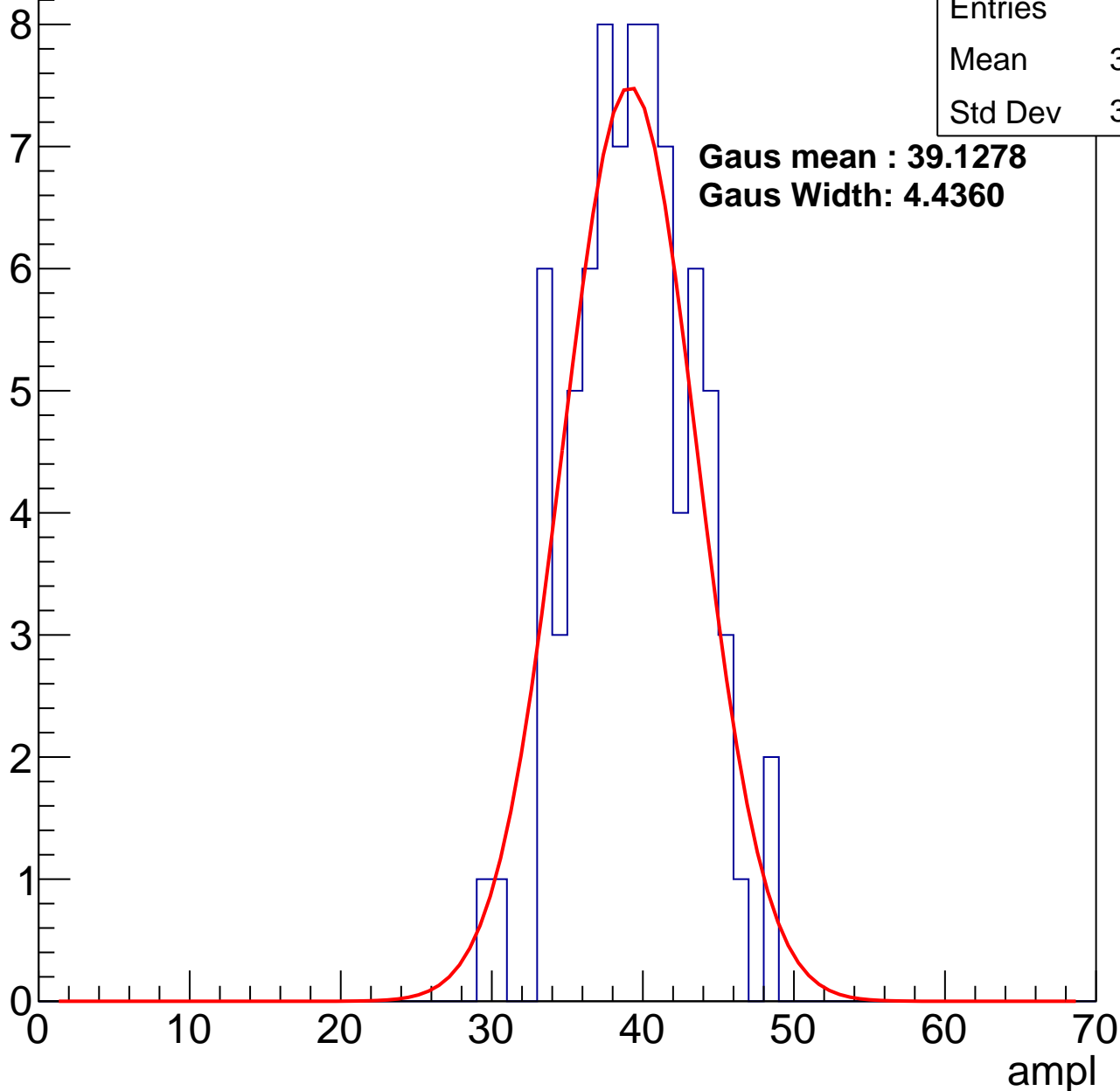
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	38.94
Std Dev	3.939

**Gaus mean : 39.1278**

**Gaus Width: 4.4360**

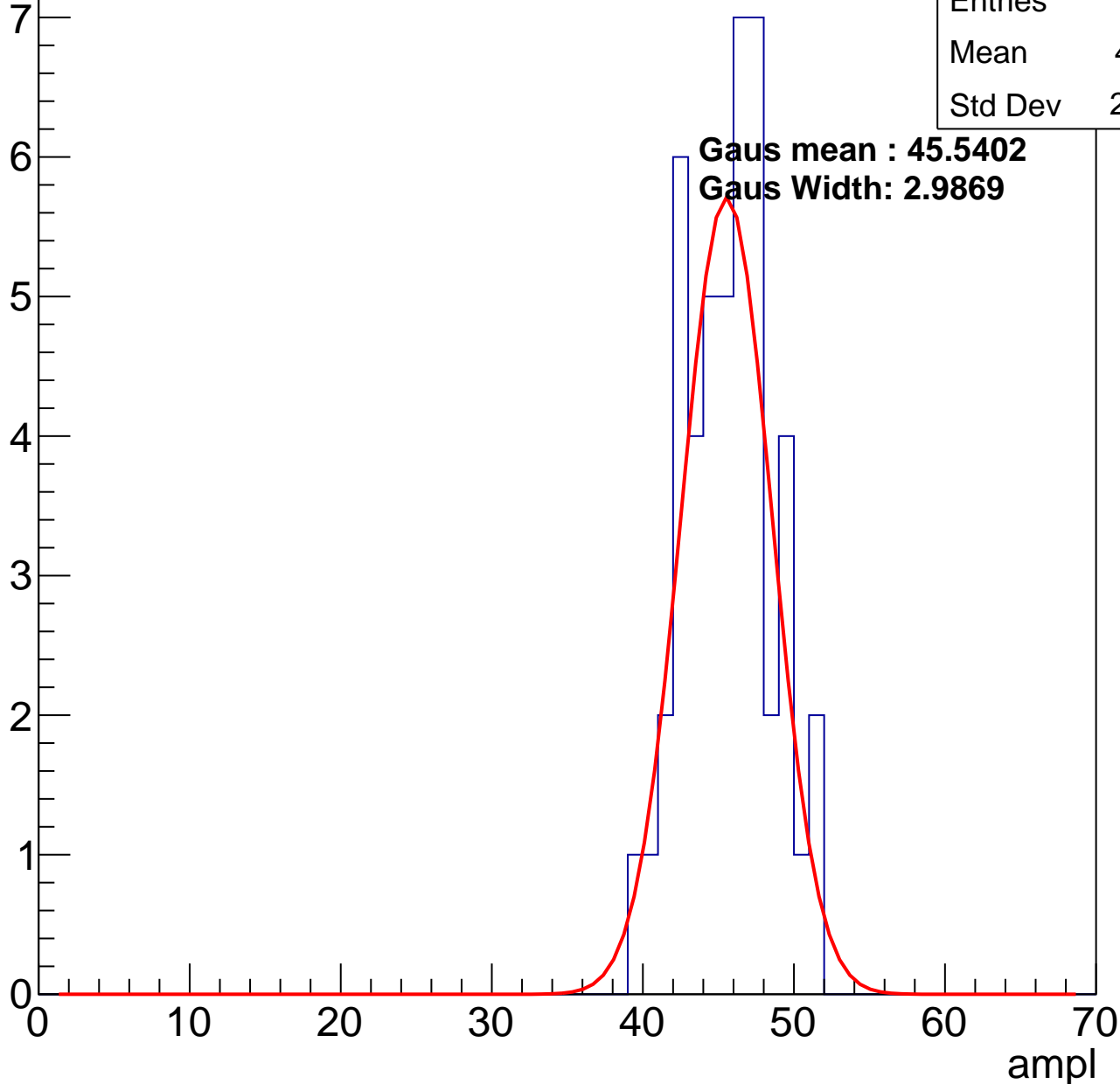


# B0L001S, U6-ch103, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	45.21
Std Dev	2.843



# B0L001S, U6-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

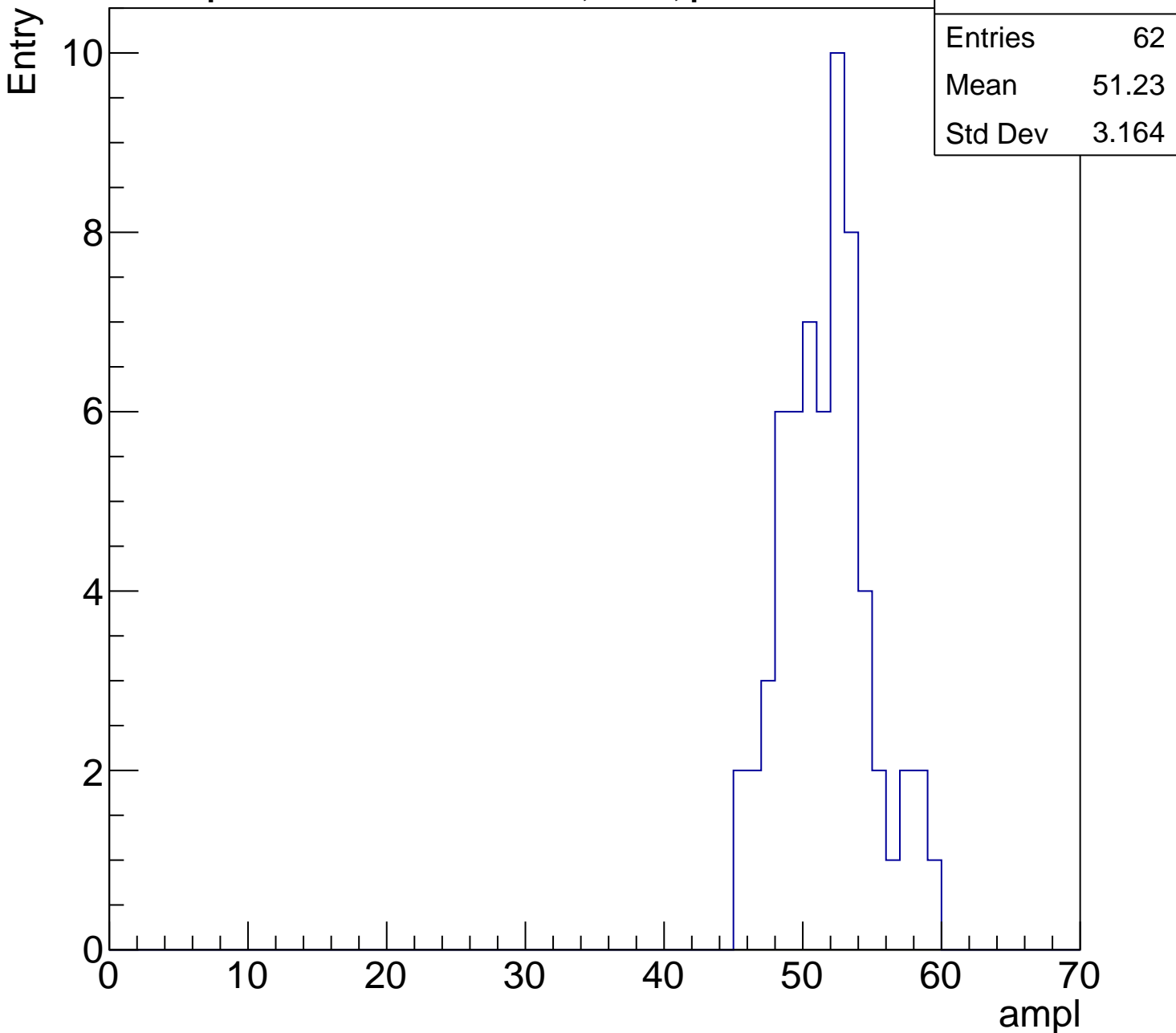
Entries	62
Mean	51.23
Std Dev	3.164

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

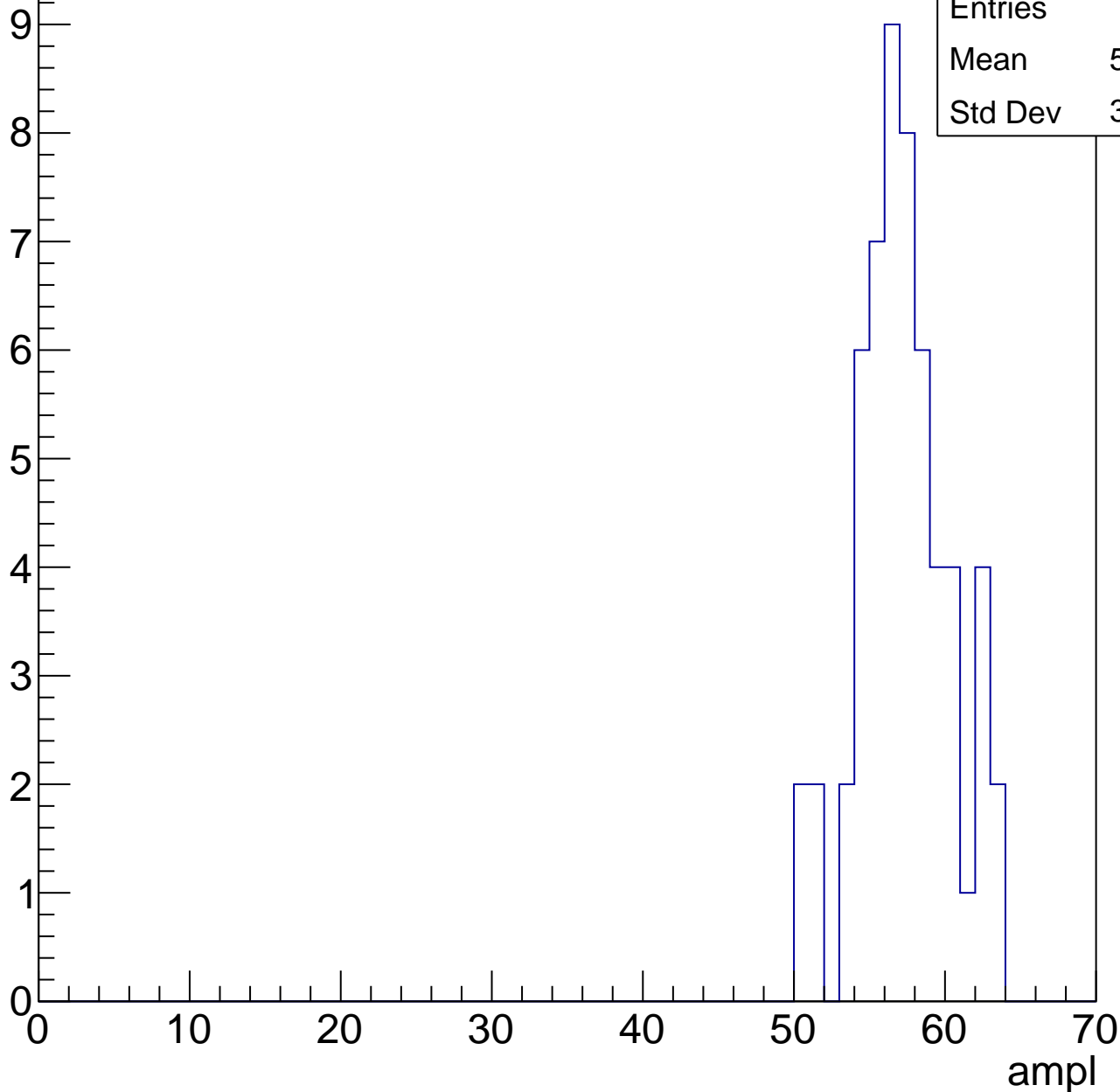


# B0L001S, U6-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

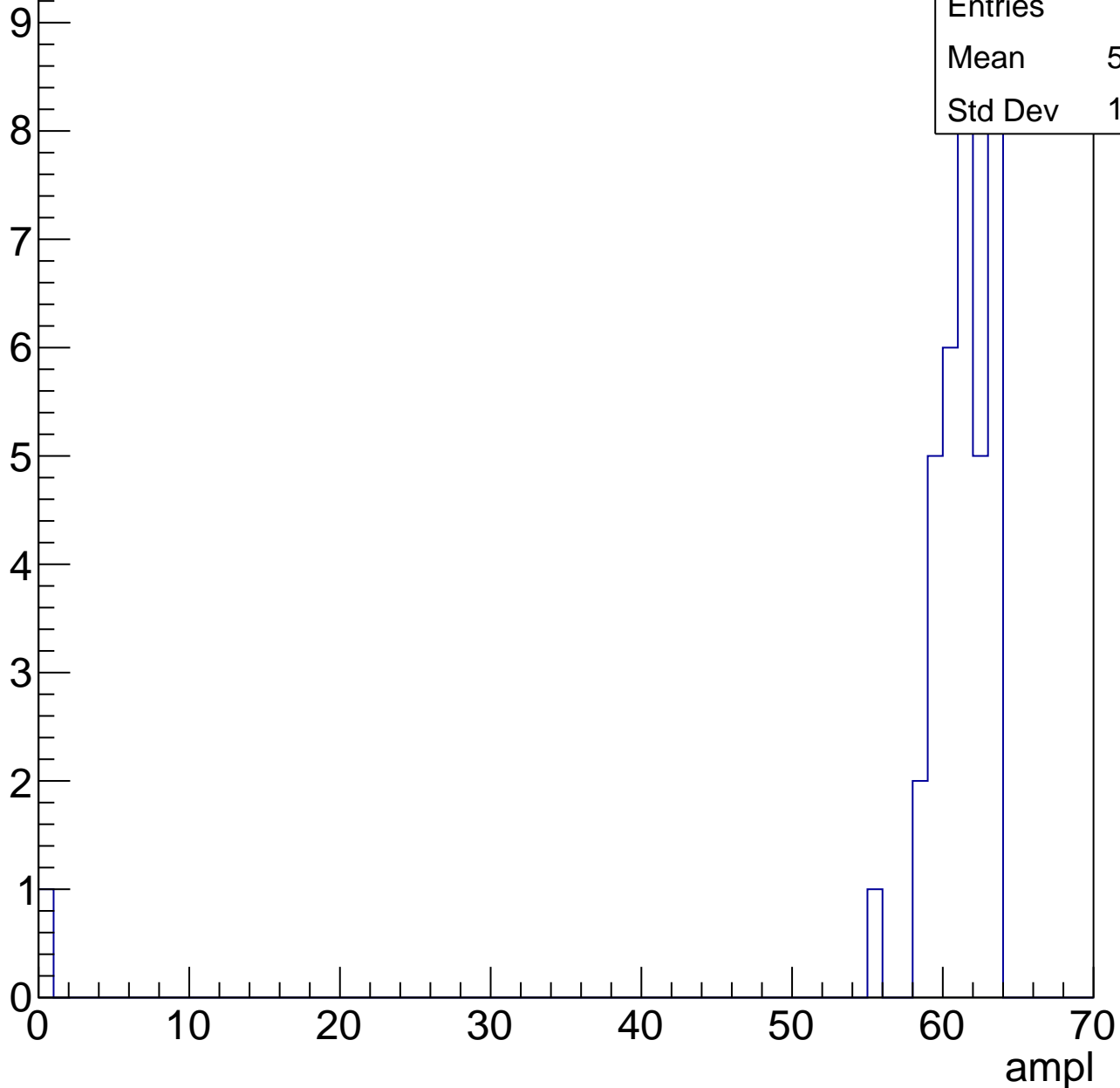
Entries	57
Mean	56.77
Std Dev	3.067



# B0L001S, U6-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U6-ch104, adc0

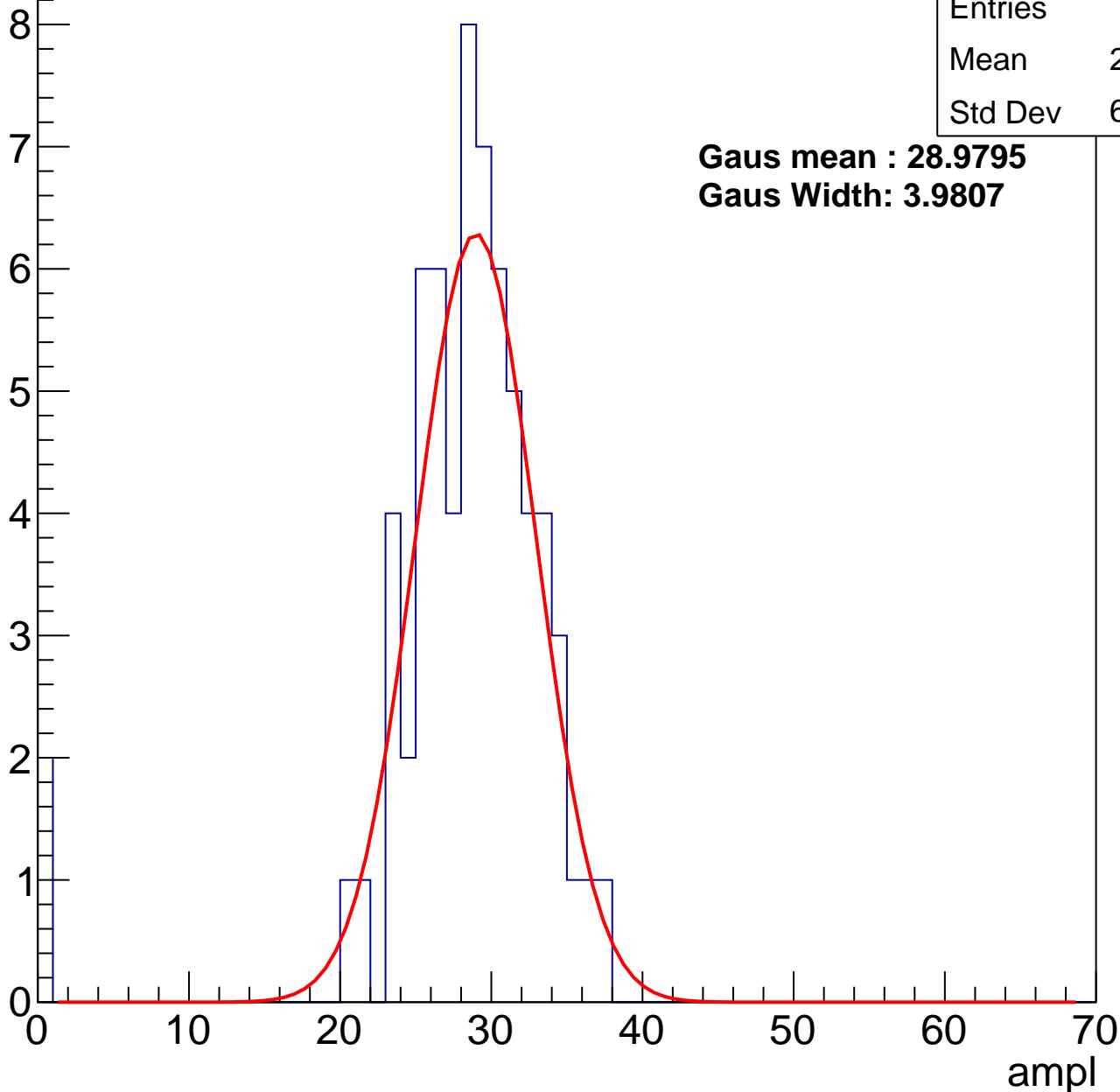
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	27.68
Std Dev	6.068

**Gaus mean : 28.9795**

**Gaus Width: 3.9807**



# B0L001S, U6-ch104, adc1

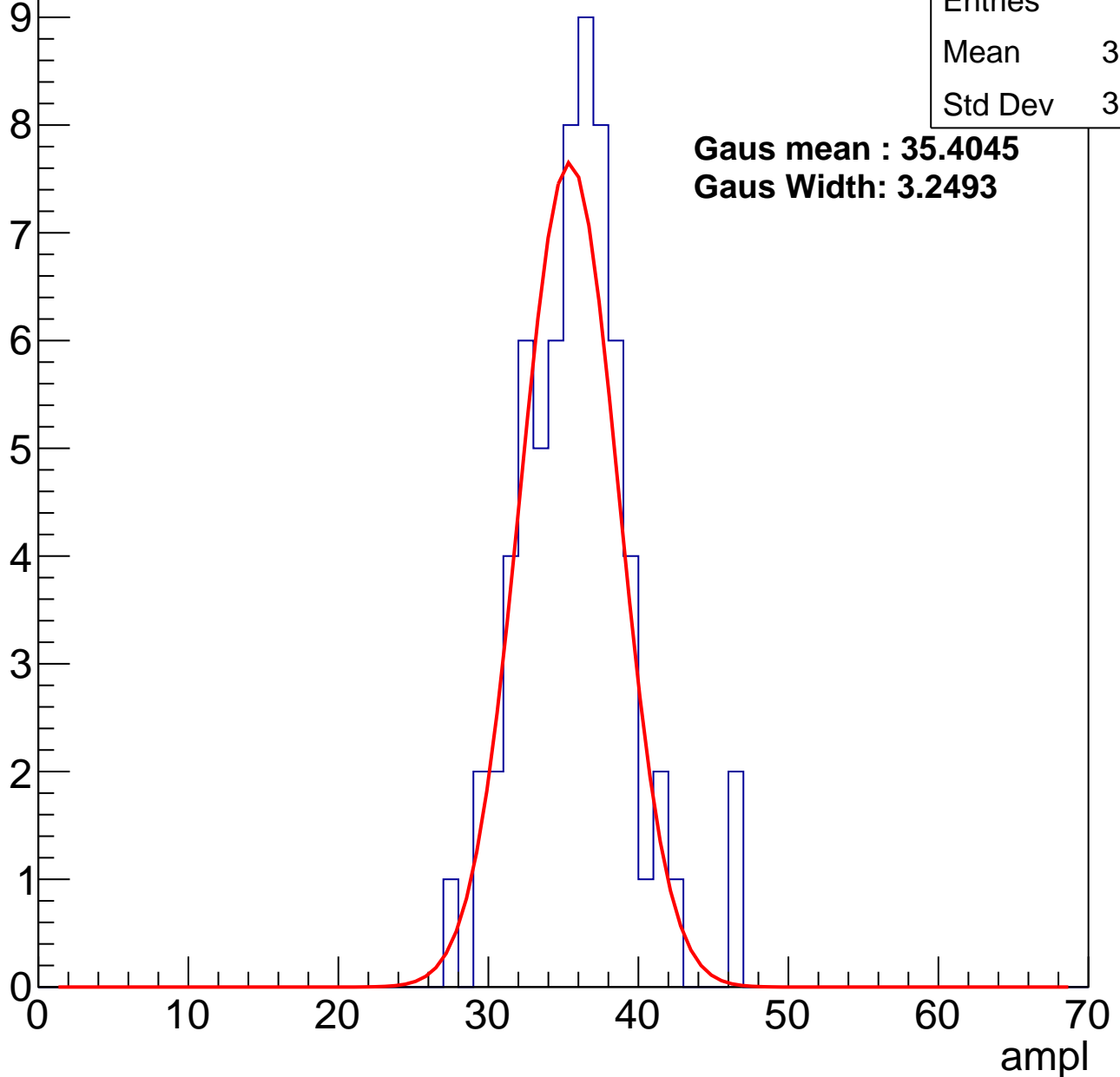
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	35.37
Std Dev	3.599

**Gaus mean : 35.4045**

**Gaus Width: 3.2493**



# B0L001S, U6-ch104, adc2

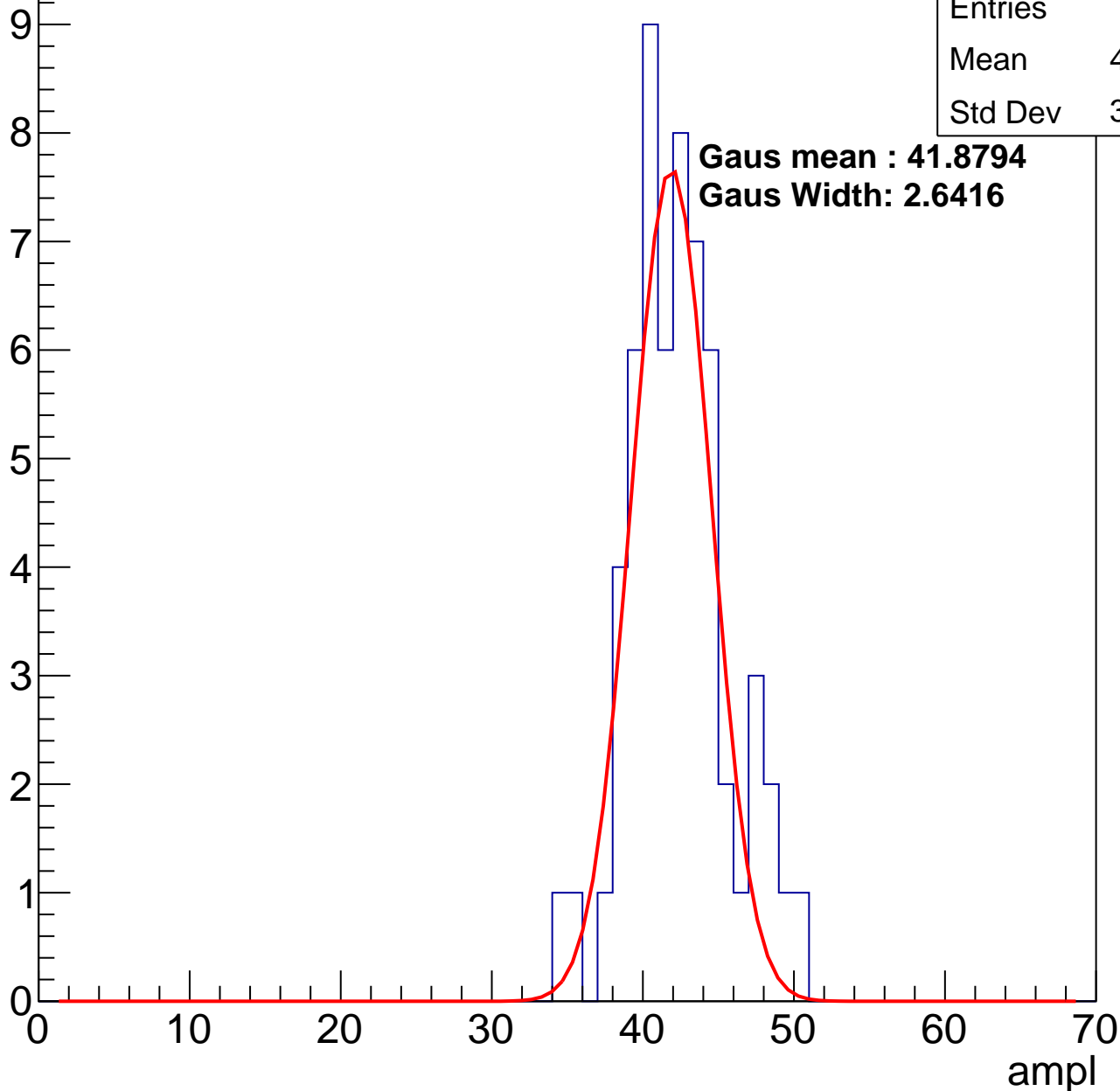
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	41.88
Std Dev	3.247

**Gaus mean : 41.8794**

**Gaus Width: 2.6416**

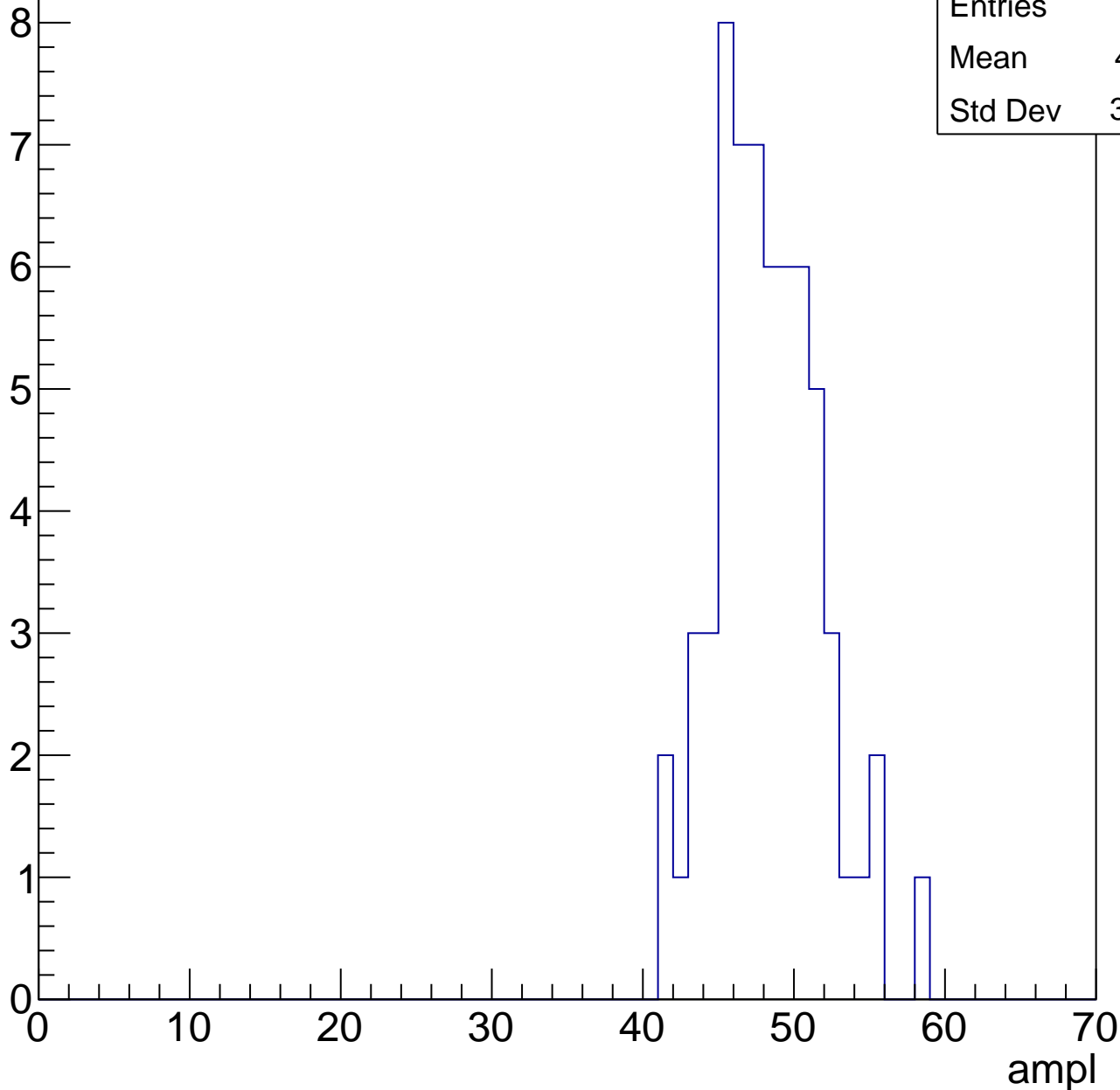


# B0L001S, U6-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

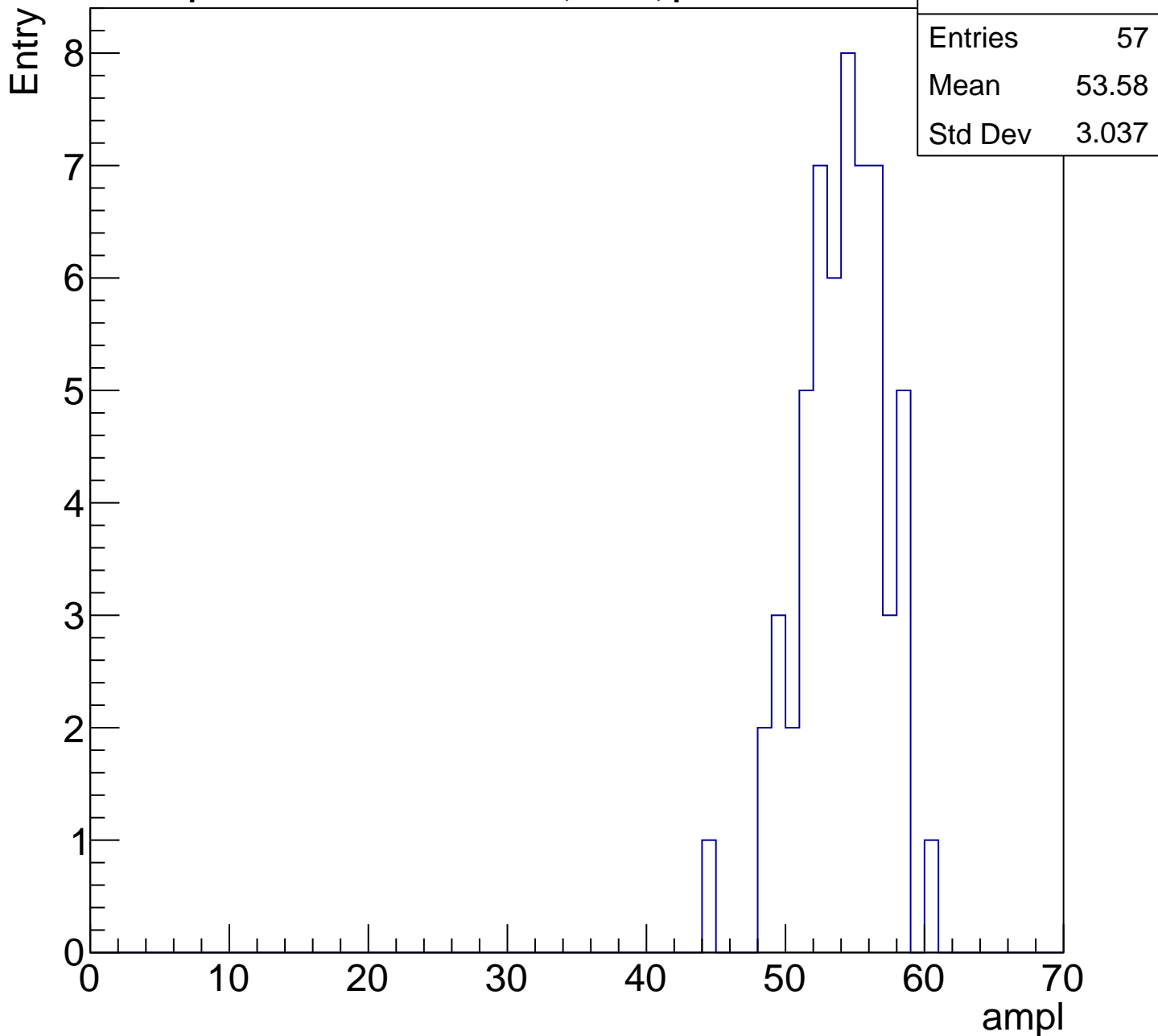
Entry

Entries	62
Mean	47.81
Std Dev	3.463



# B0L001S, U6-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

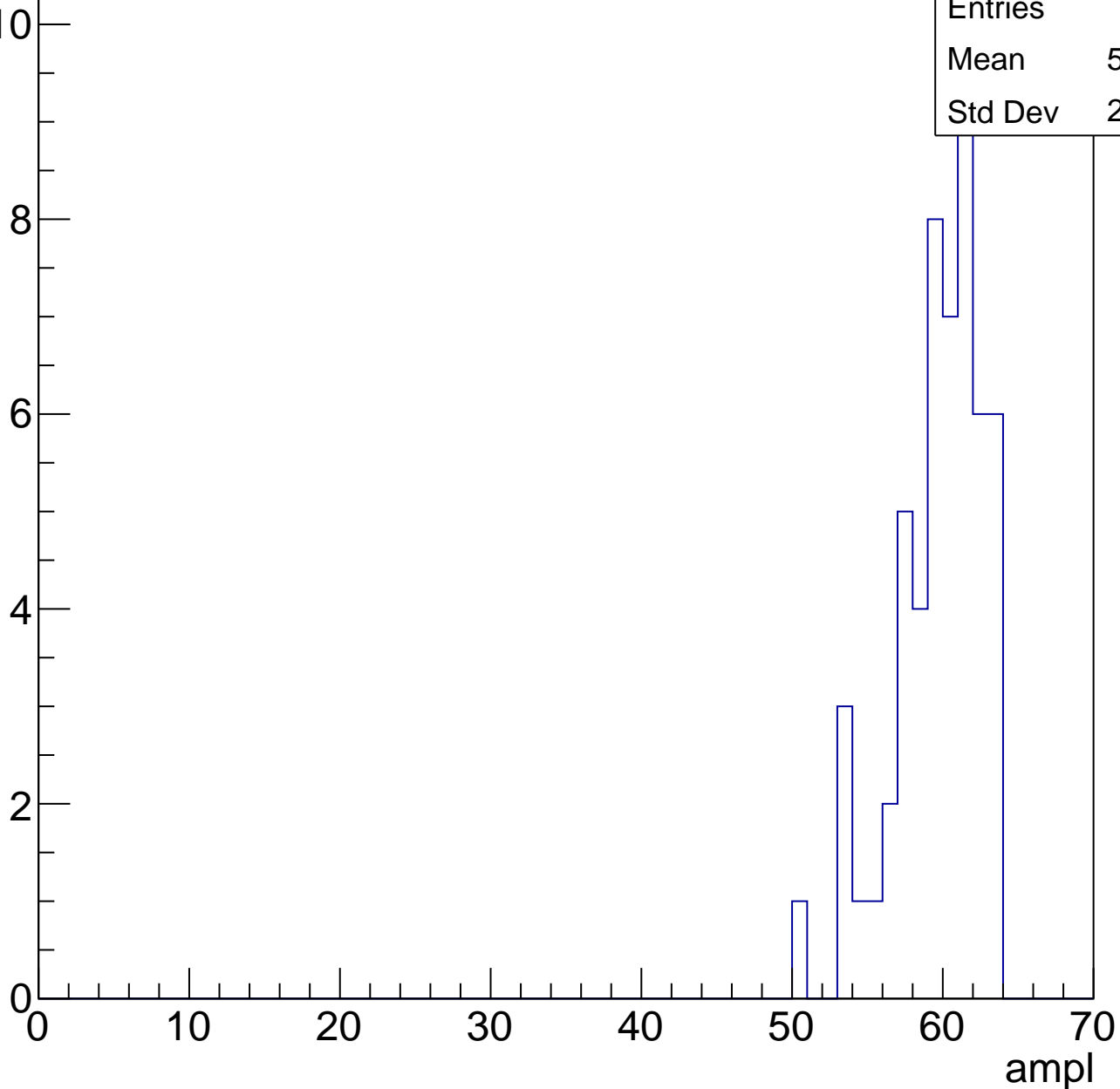


# B0L001S, U6-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

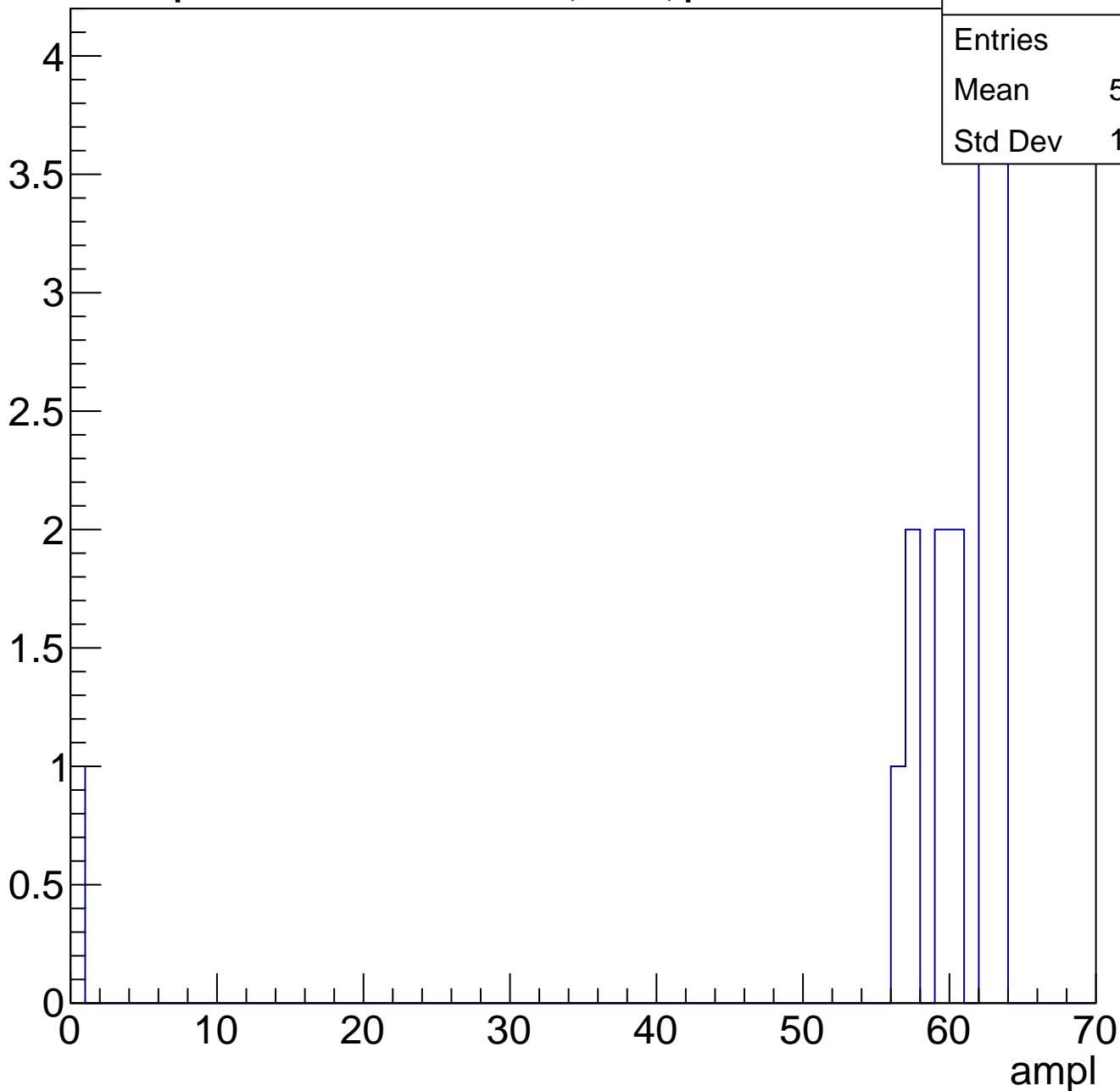
Entries	54
Mean	59.24
Std Dev	2.937



# B0L001S, U6-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U6-ch105, adc0

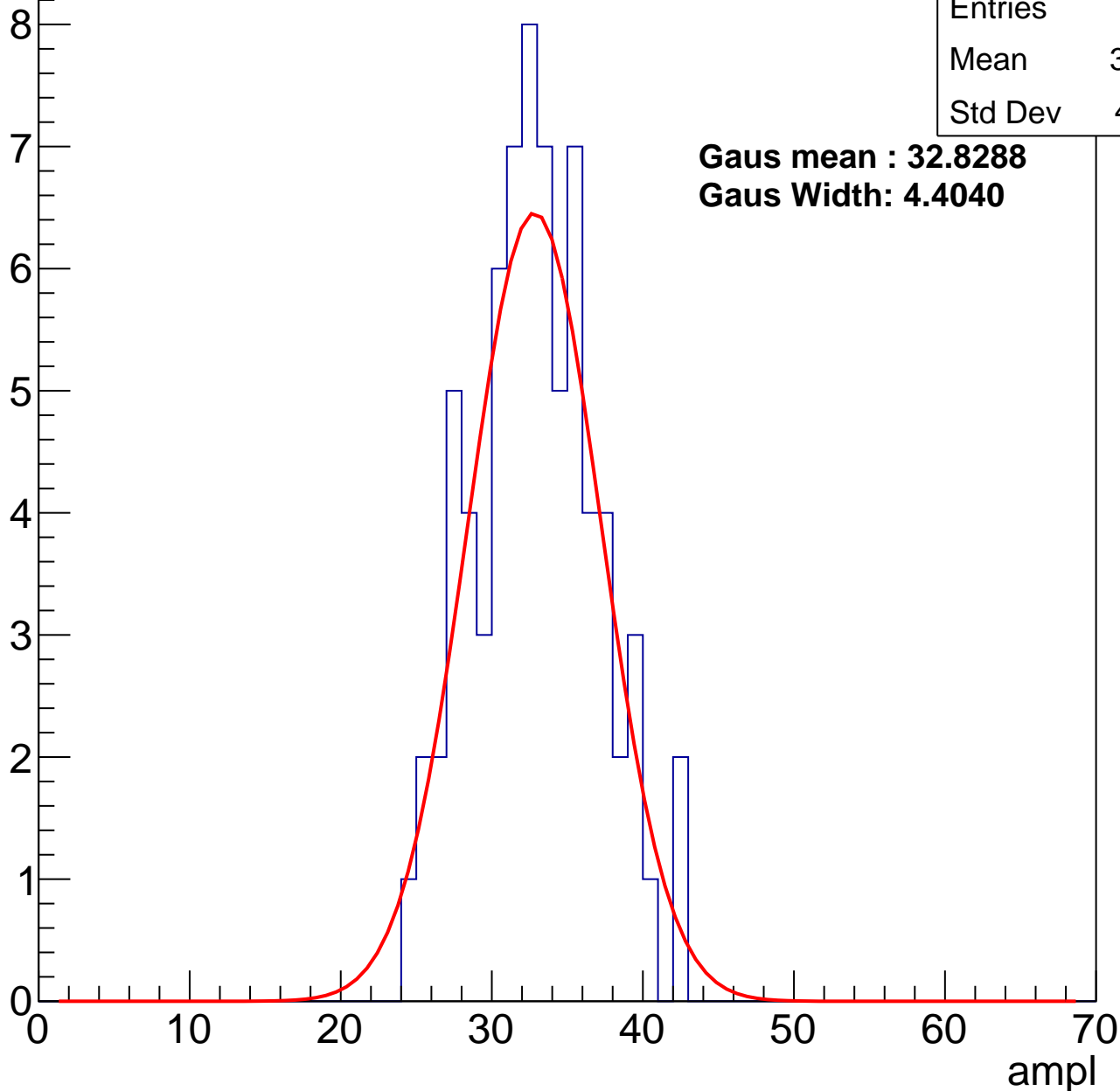
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	32.44
Std Dev	4.061

**Gaus mean : 32.8288**

**Gaus Width: 4.4040**



# B0L001S, U6-ch105, adc1

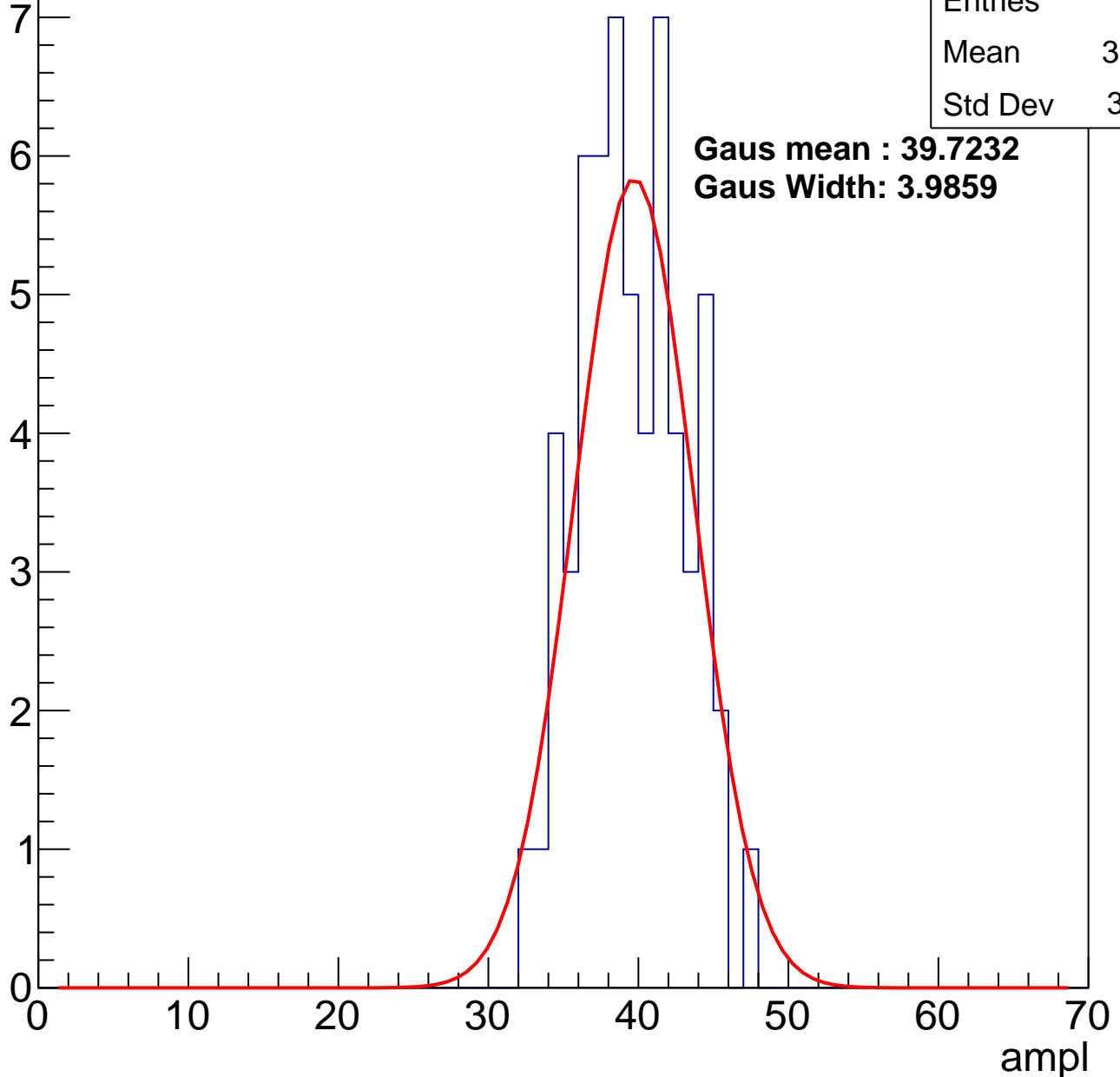
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	39.08
Std Dev	3.431

**Gaus mean : 39.7232**

**Gaus Width: 3.9859**



# B0L001S, U6-ch105, adc2

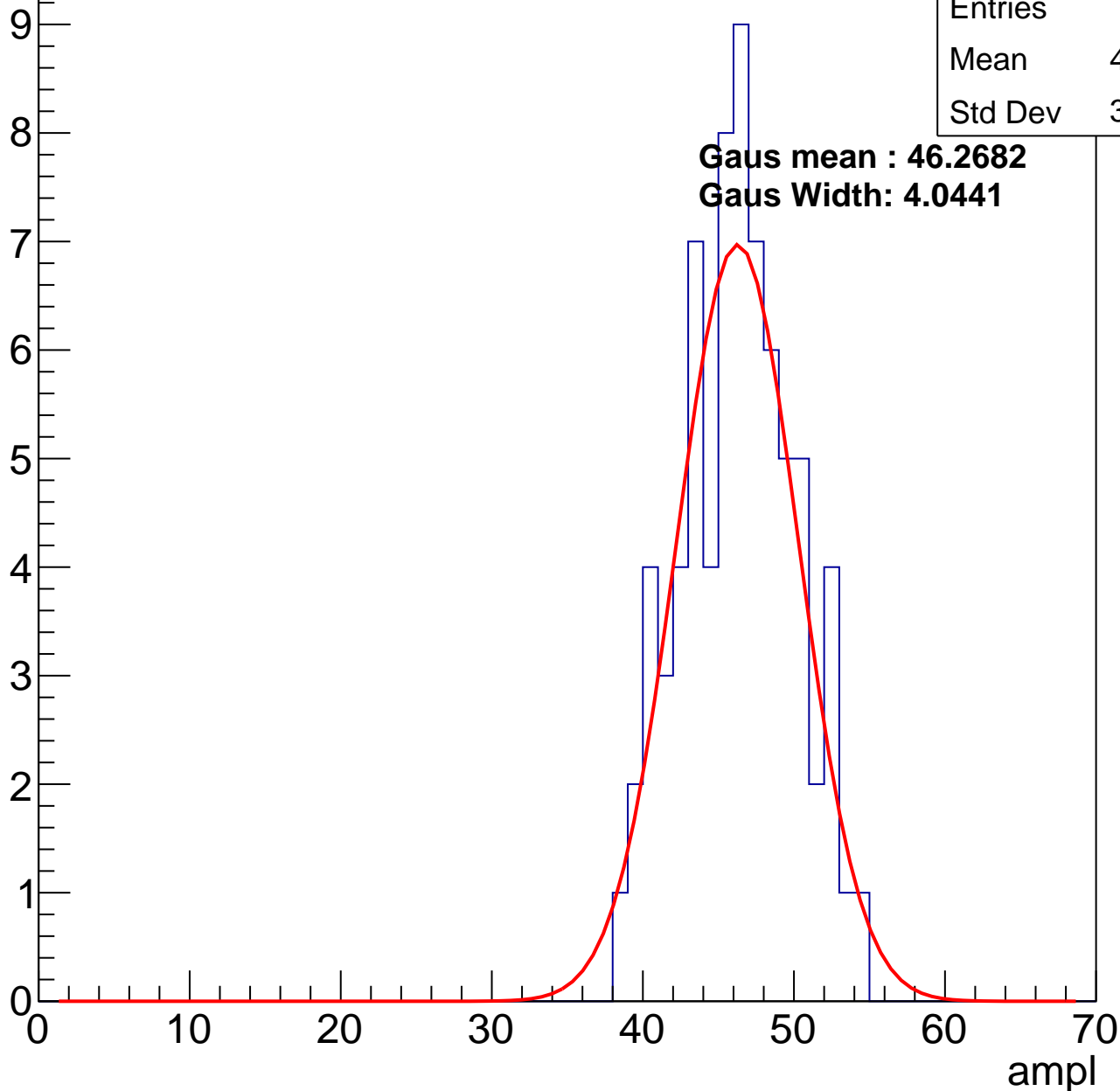
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	45.85
Std Dev	3.689

**Gaus mean : 46.2682**

**Gaus Width: 4.0441**

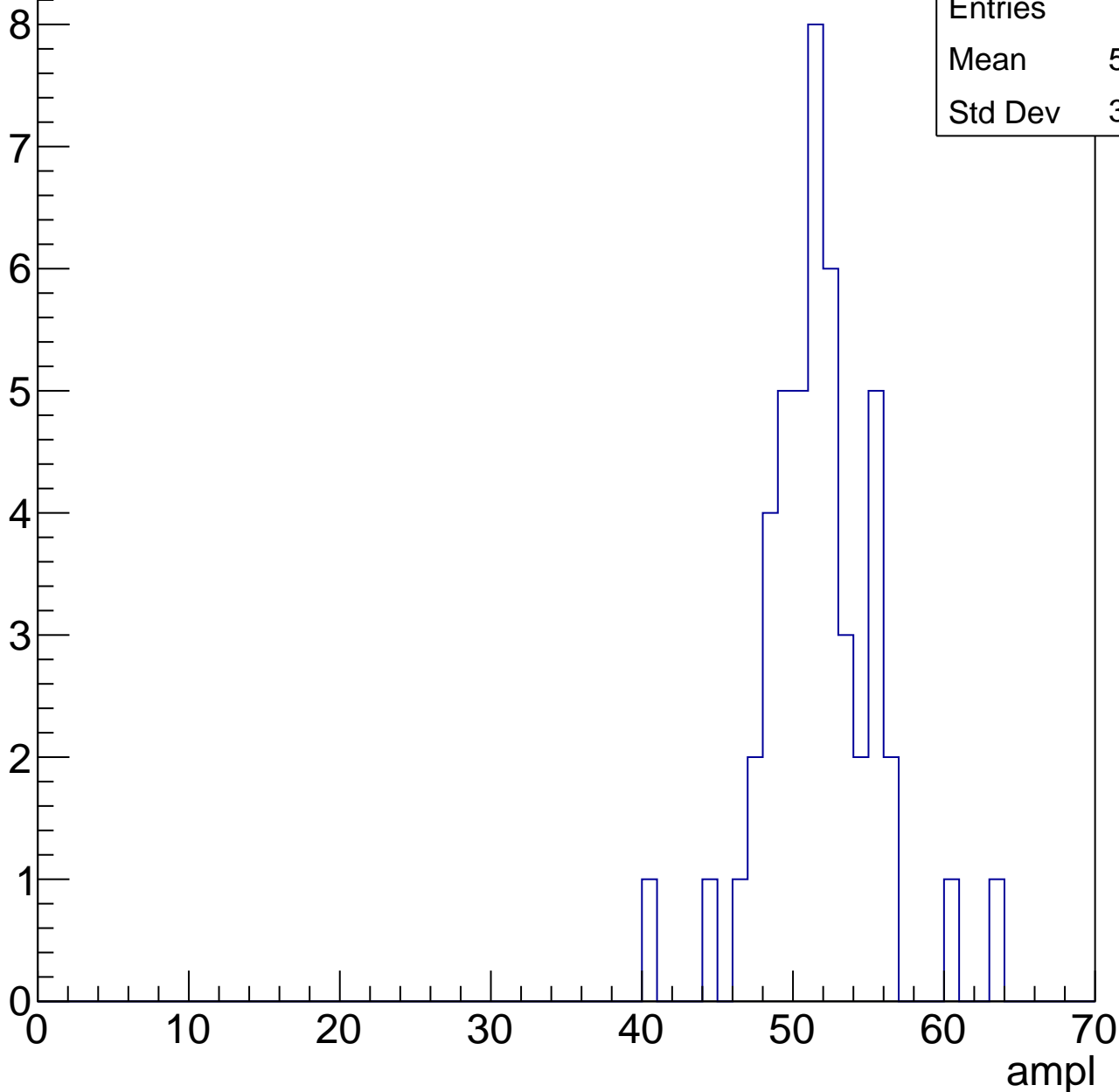


# B0L001S, U6-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

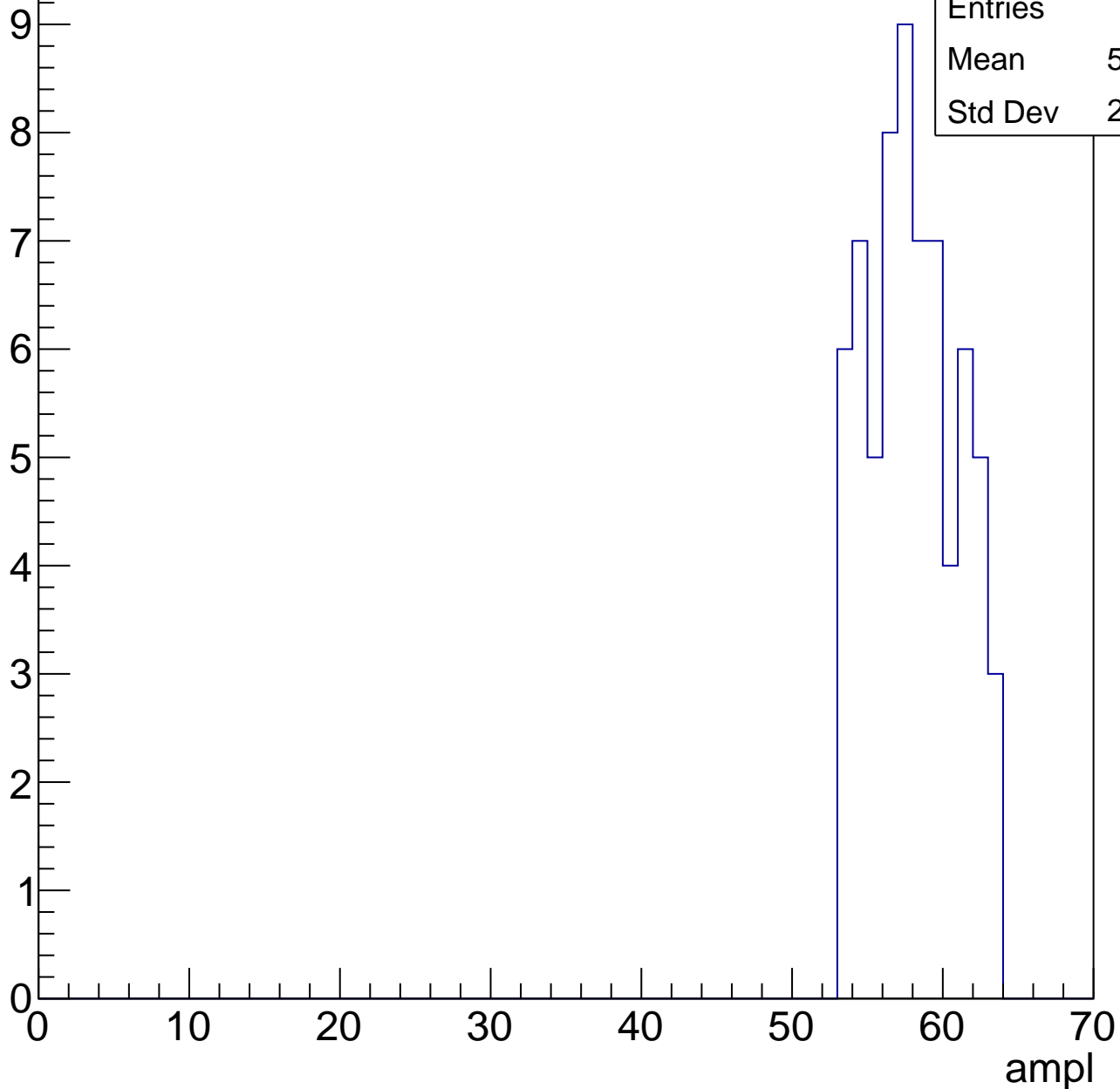
Entries	47
Mean	51.23
Std Dev	3.794



# B0L001S, U6-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

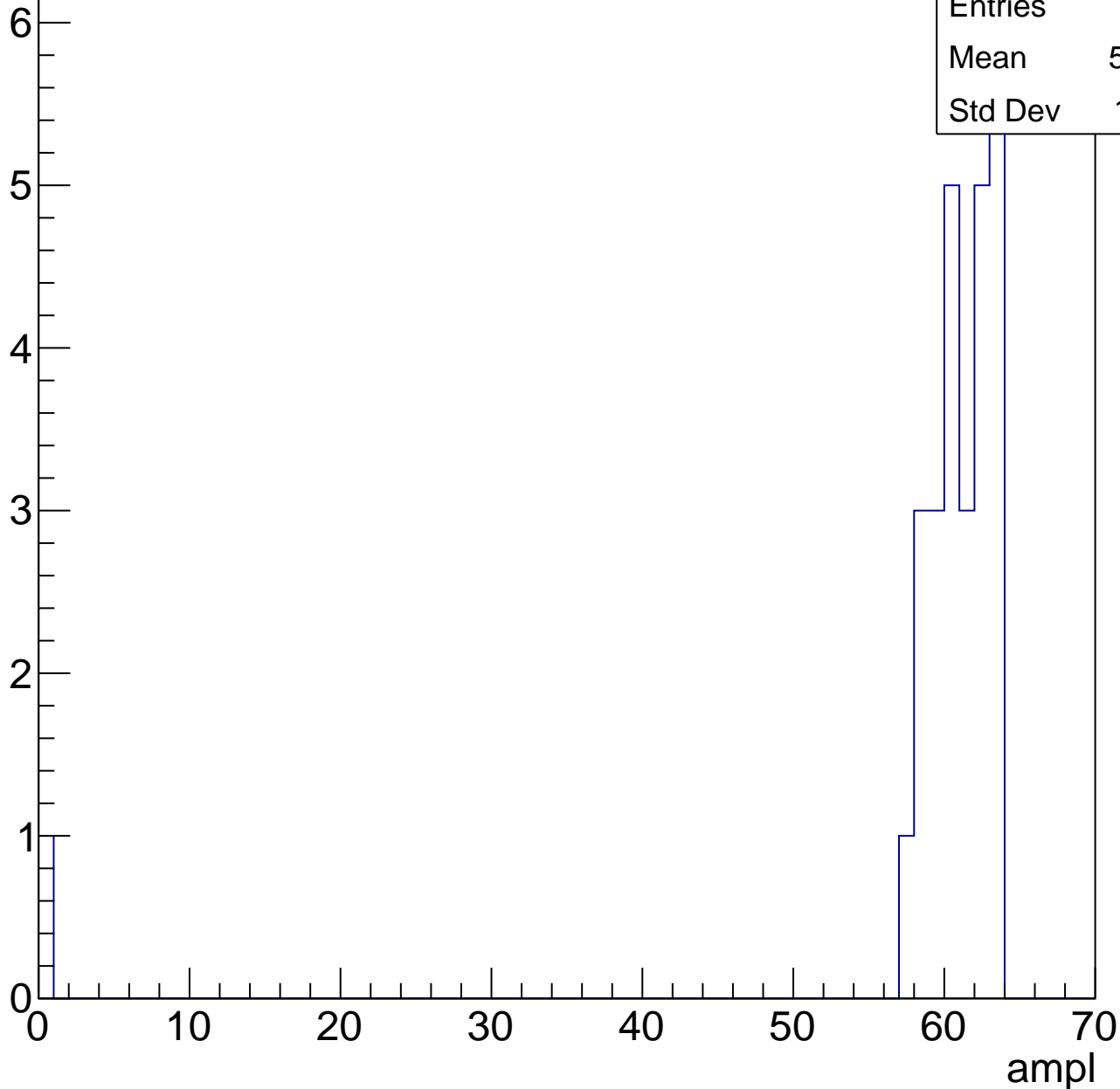


# B0L001S, U6-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	27
Mean	58.48
Std Dev	11.61



# B0L001S, U6-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch106, adc0

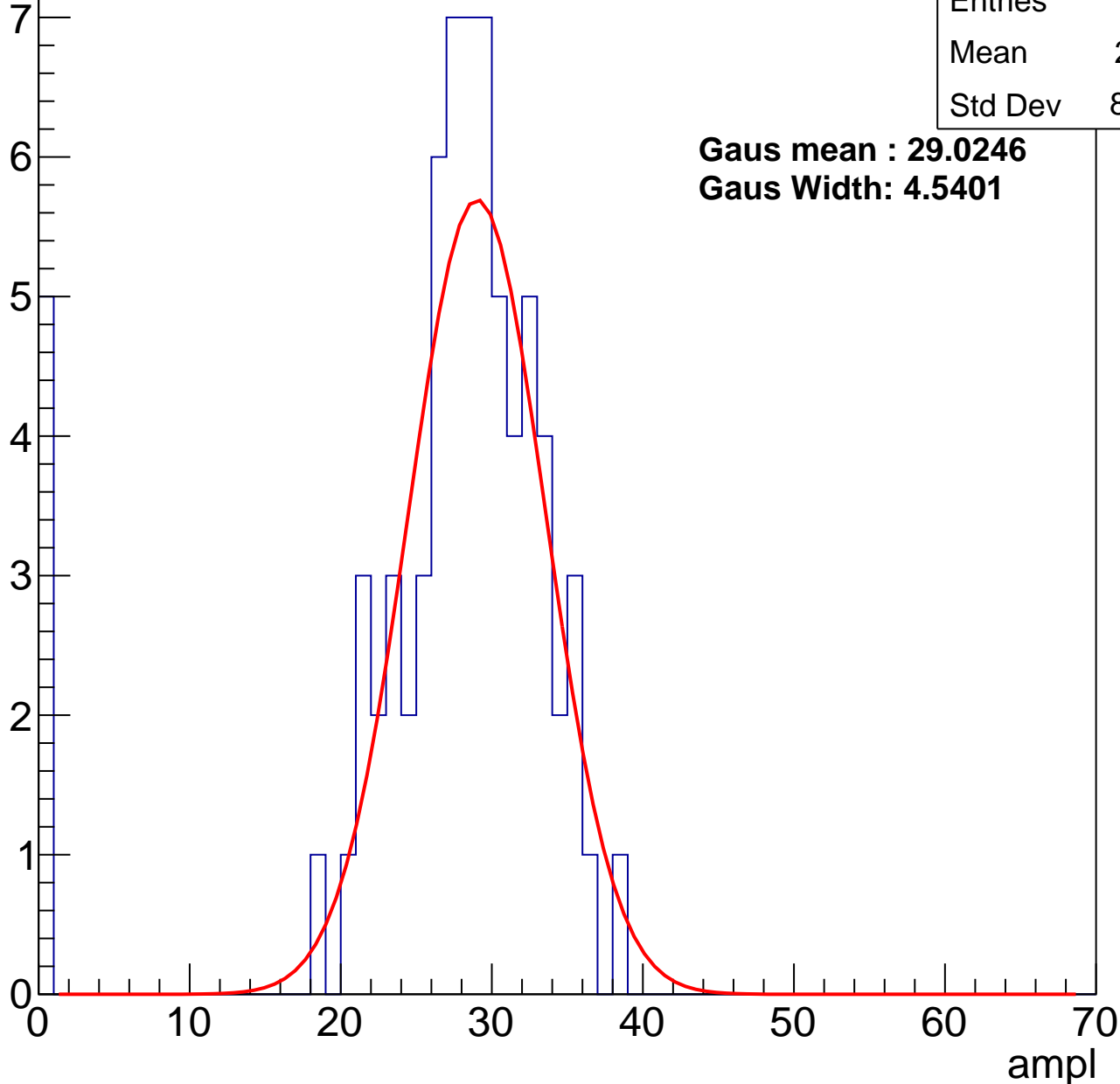
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	26.31
Std Dev	8.239

**Gaus mean : 29.0246**

**Gaus Width: 4.5401**



# B0L001S, U6-ch106, adc1

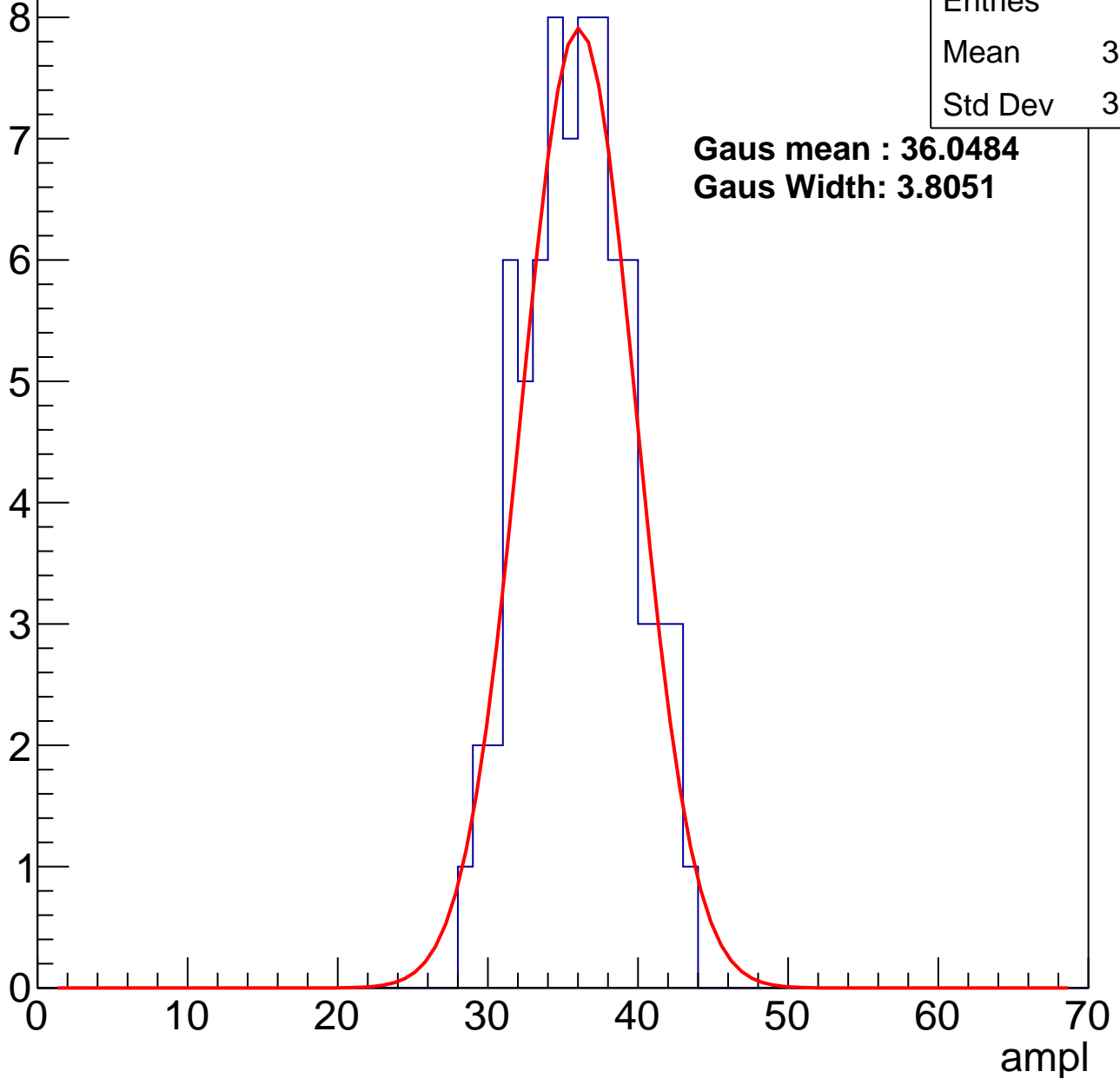
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	35.53
Std Dev	3.477

**Gaus mean : 36.0484**

**Gaus Width: 3.8051**



# B0L001S, U6-ch106, adc2

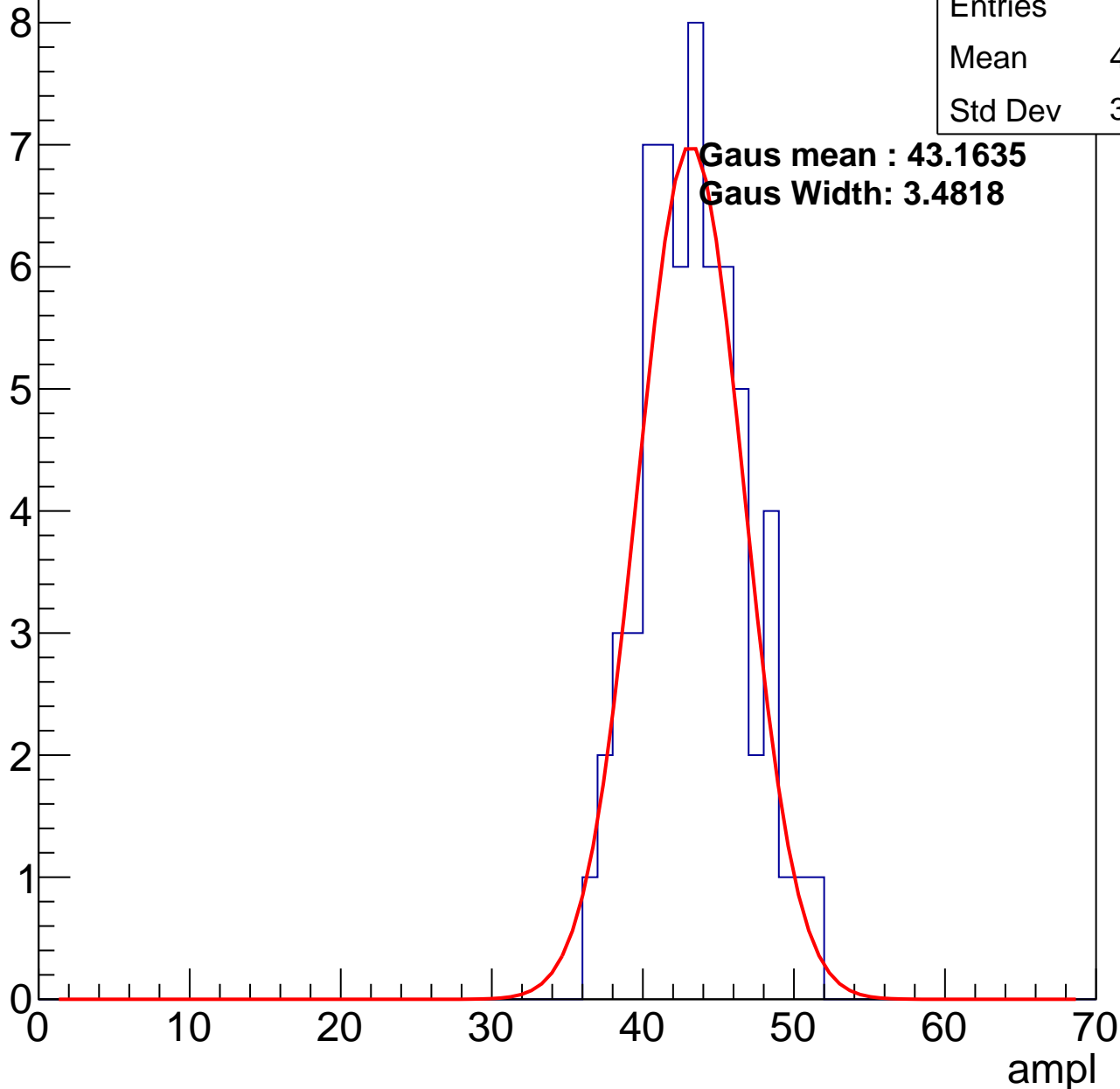
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	42.92
Std Dev	3.325

**Gaus mean : 43.1635**

**Gaus Width: 3.4818**

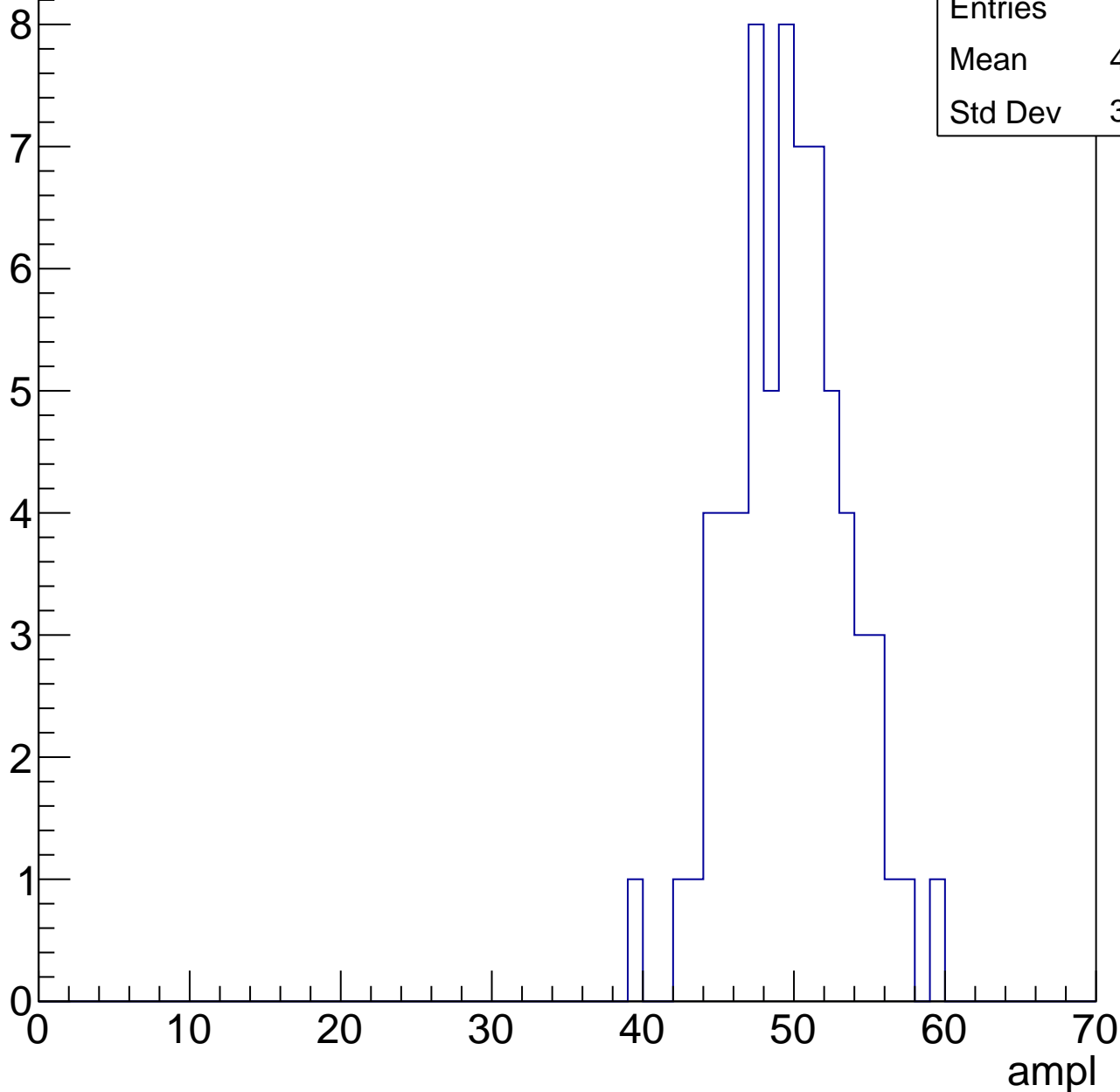


# B0L001S, U6-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	49.26
Std Dev	3.752

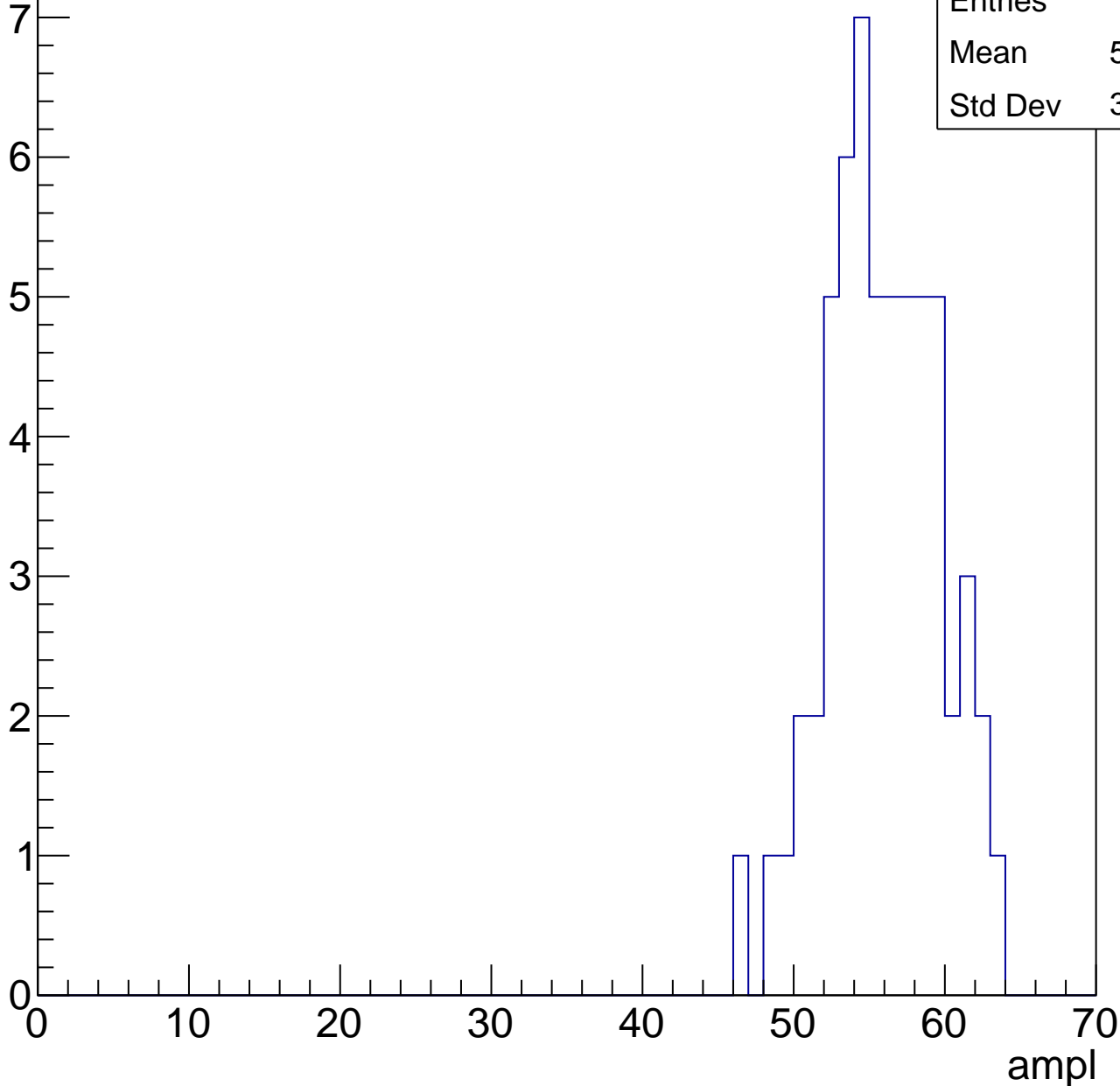


# B0L001S, U6-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

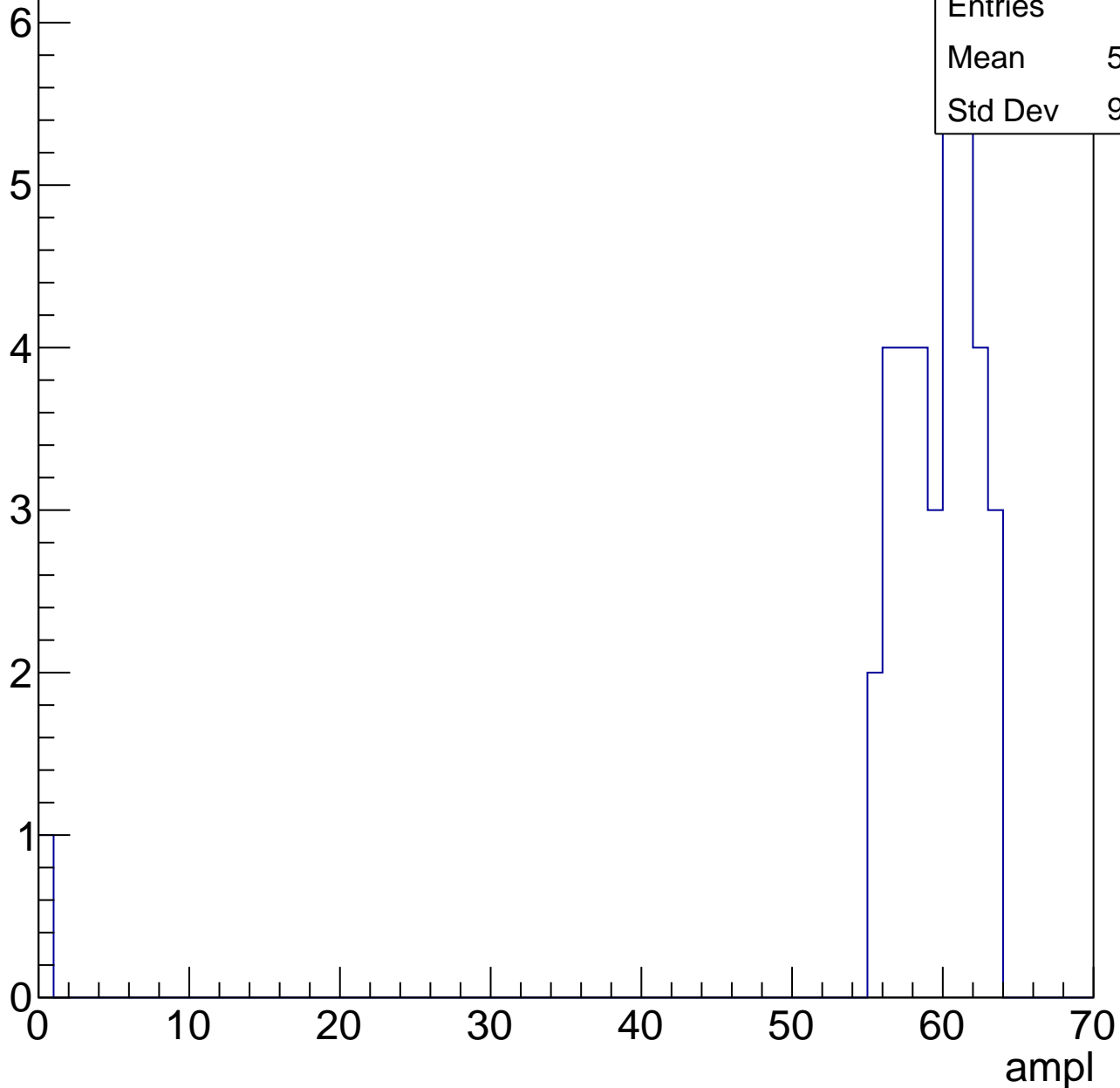
Entries	58
Mean	55.45
Std Dev	3.673



# B0L001S, U6-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

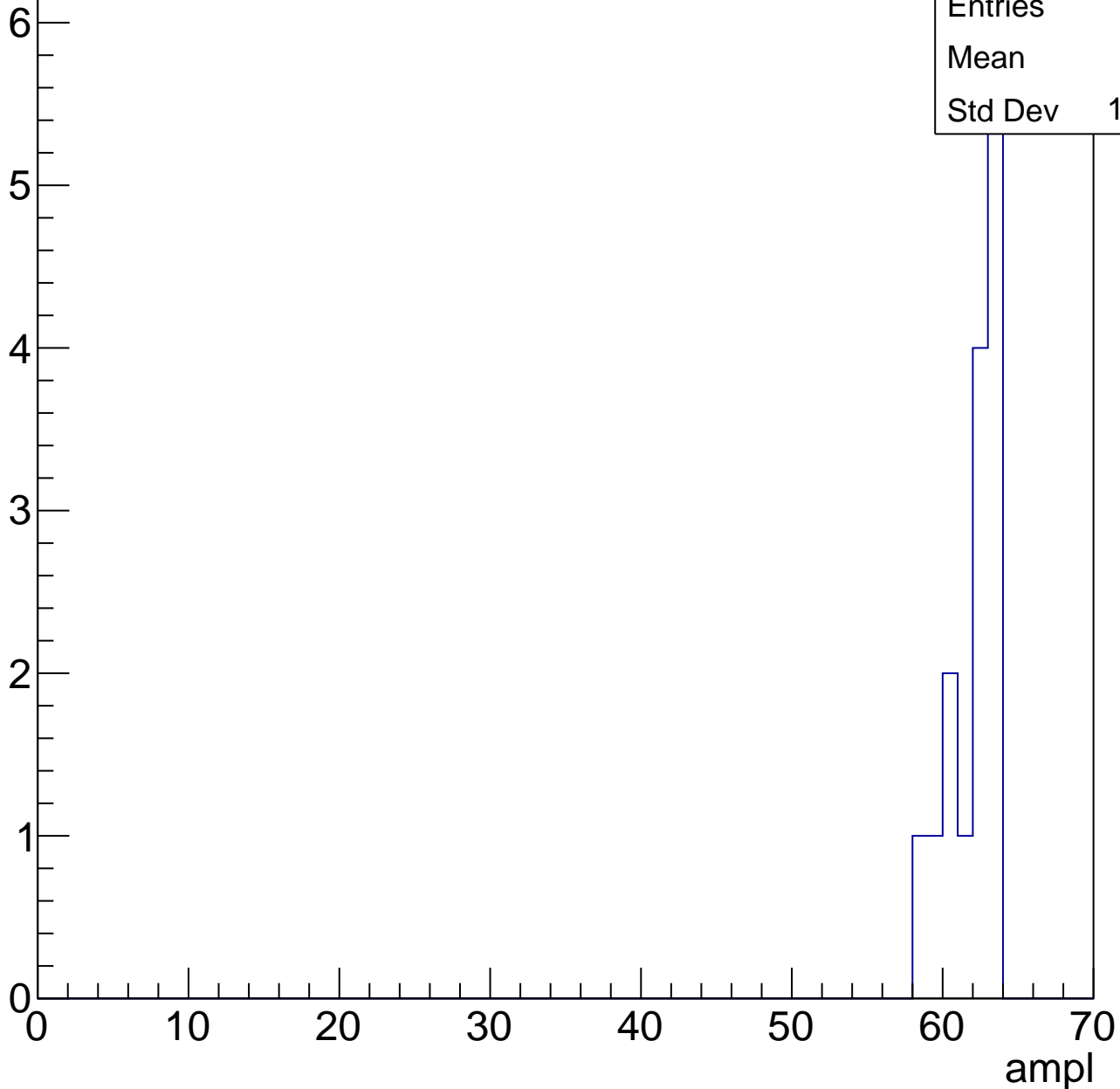


# B0L001S, U6-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	15
Mean	61.6
Std Dev	1.583





# B0L001S, U6-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch107, adc0

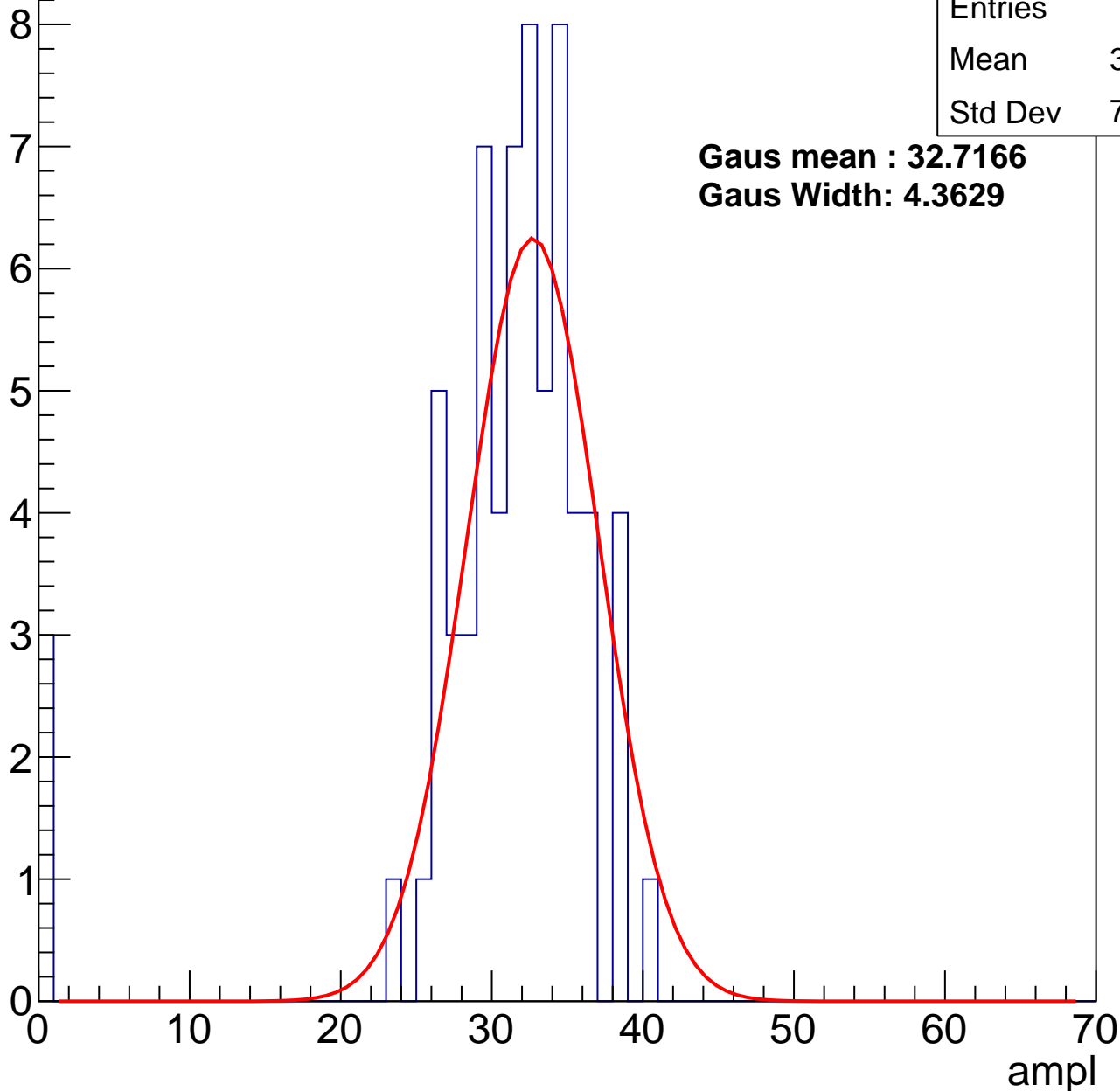
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	30.18
Std Dev	7.386

**Gaus mean : 32.7166**

**Gaus Width: 4.3629**



# B0L001S, U6-ch107, adc1

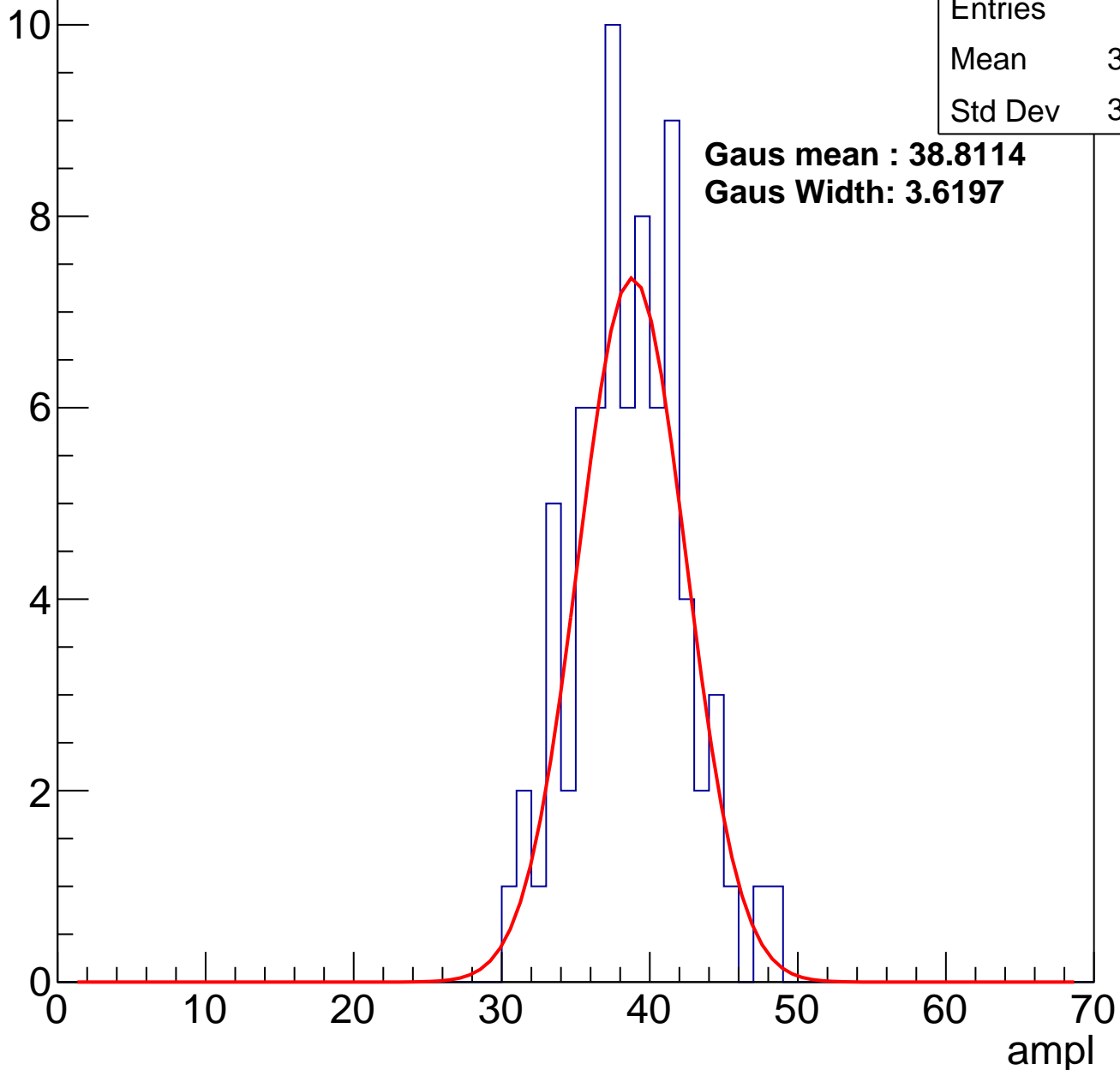
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	74
Mean	38.22
Std Dev	3.684

**Gaus mean : 38.8114**

**Gaus Width: 3.6197**

Entry



# B0L001S, U6-ch107, adc2

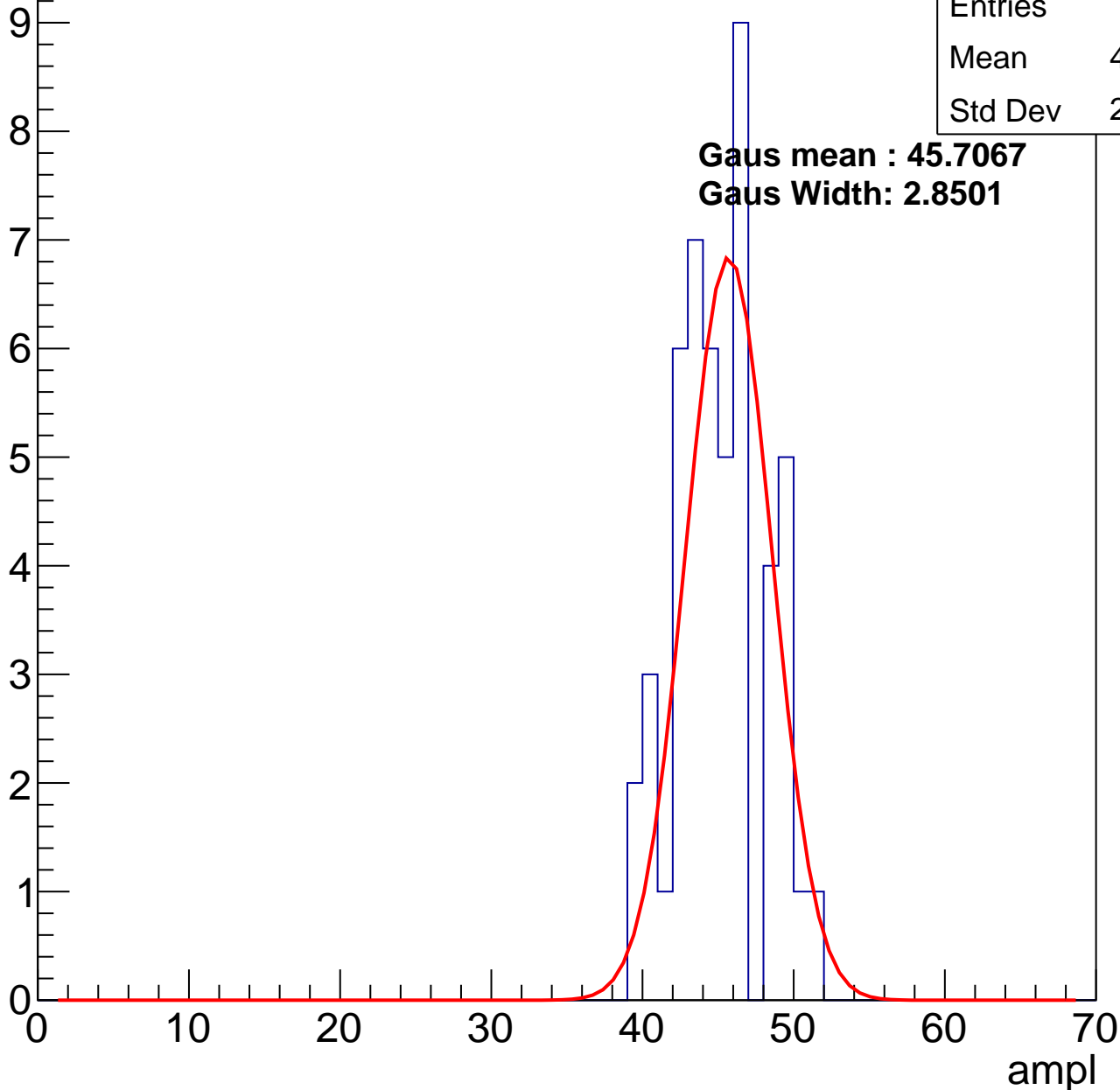
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	44.66
Std Dev	2.937

**Gaus mean : 45.7067**

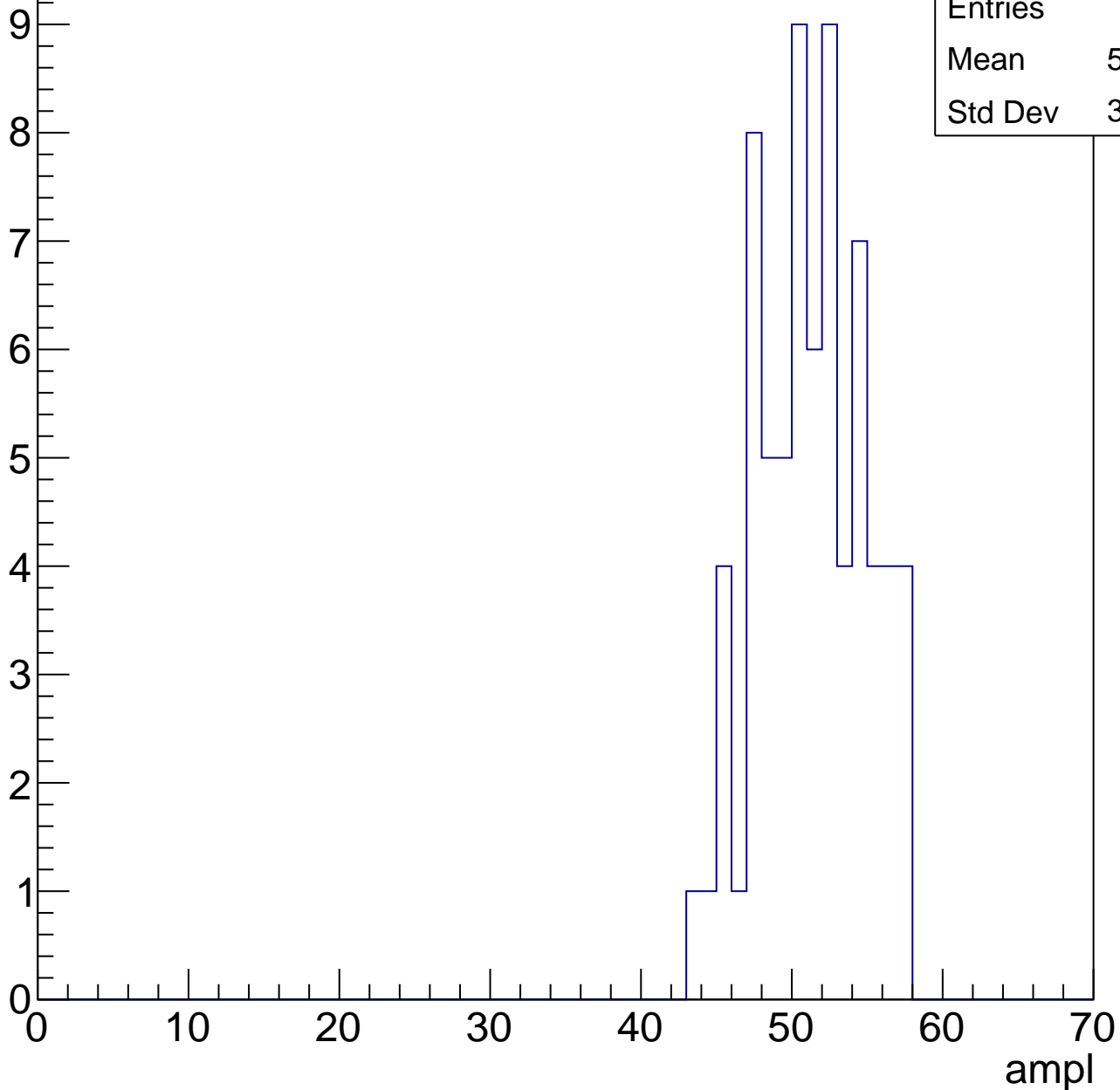
**Gaus Width: 2.8501**



# B0L001S, U6-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



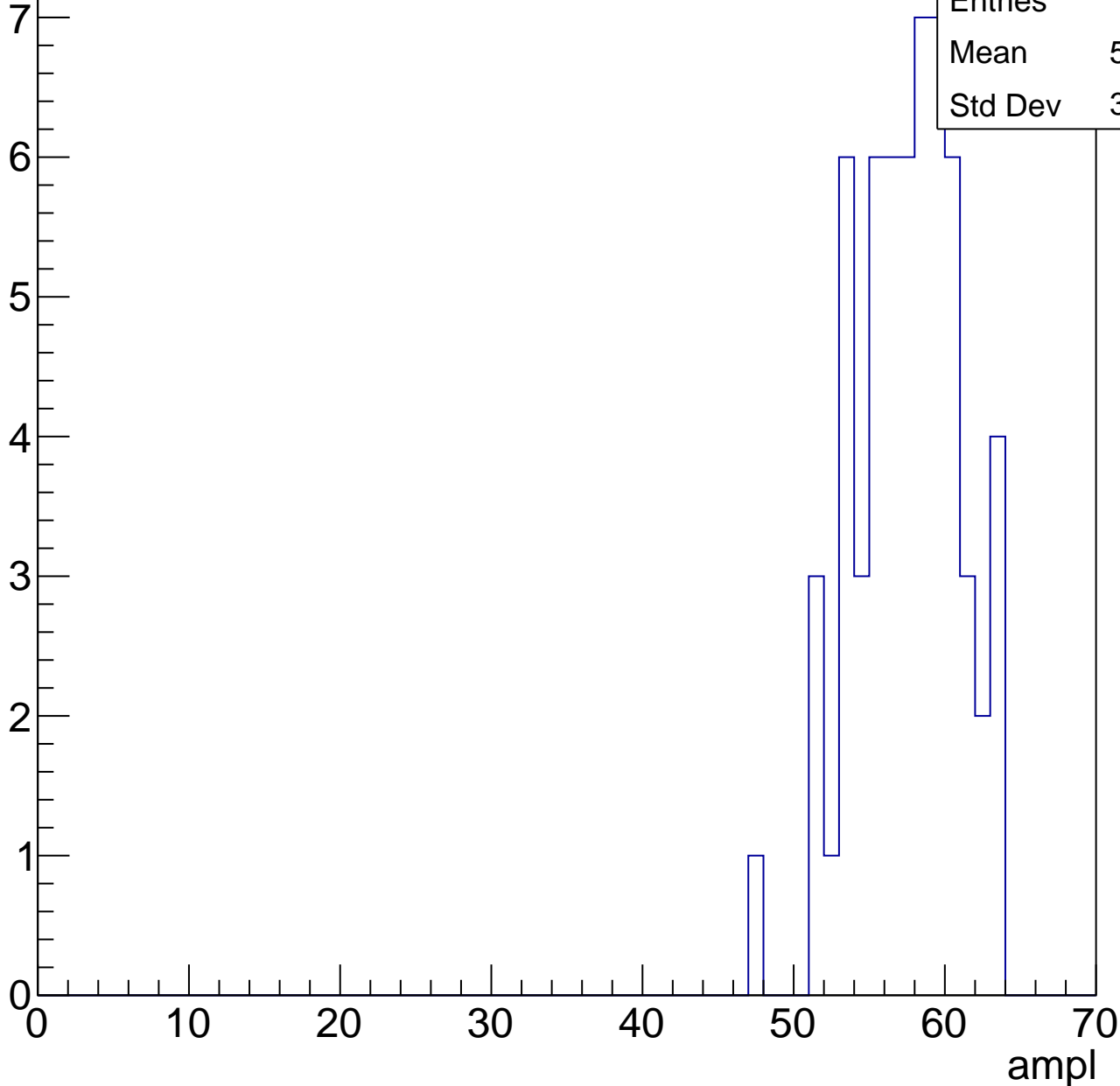
Entries	72
Mean	50.83
Std Dev	3.492

# B0L001S, U6-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	57.02
Std Dev	3.428



# B0L001S, U6-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

7

6

5

4

3

2

1

0

Entries

30

Mean

61

Std Dev

1.571

0

ampl

0

10

20

30

40

50

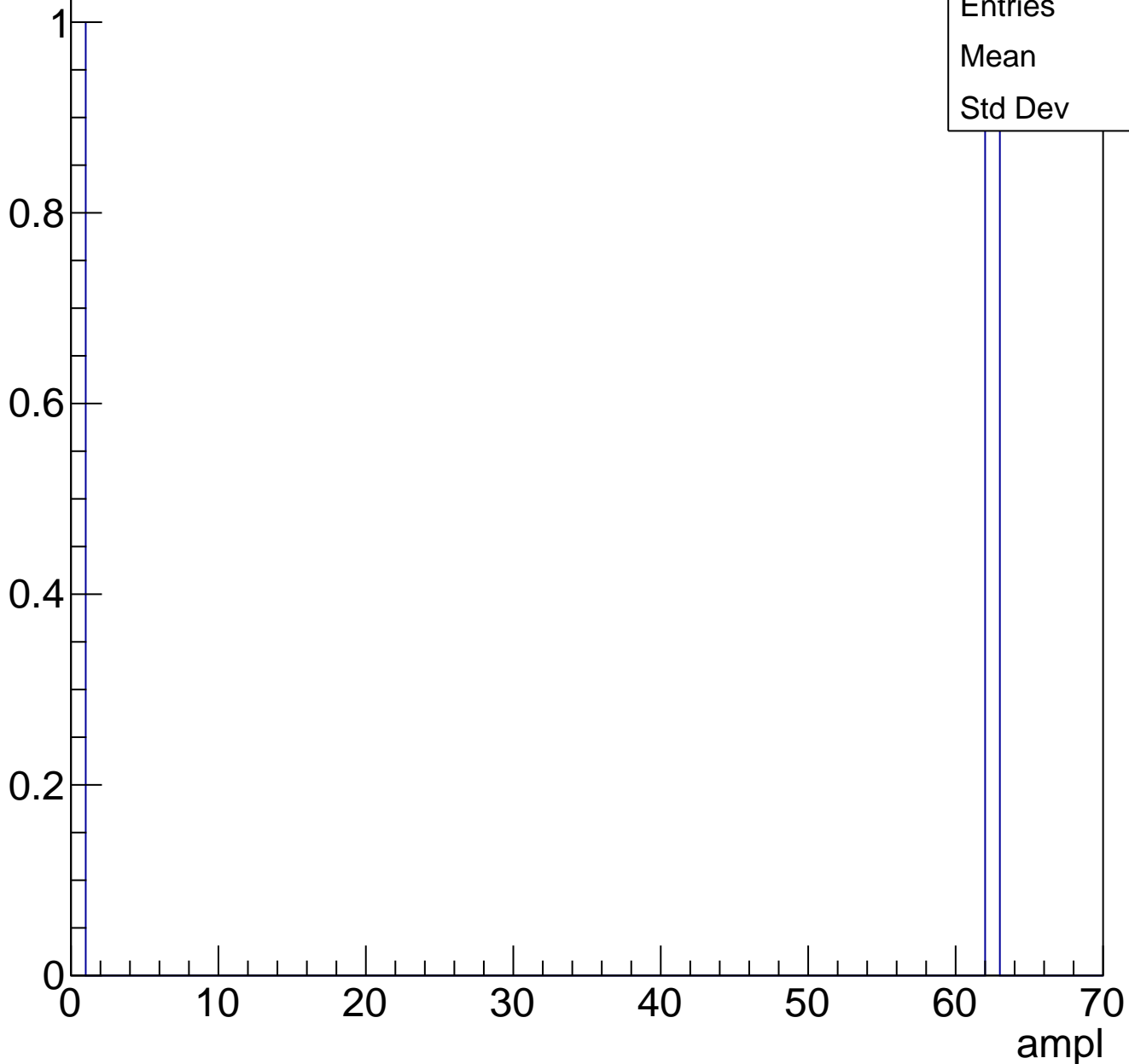
60

70

# B0L001S, U6-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L001S, U6-ch108, adc0

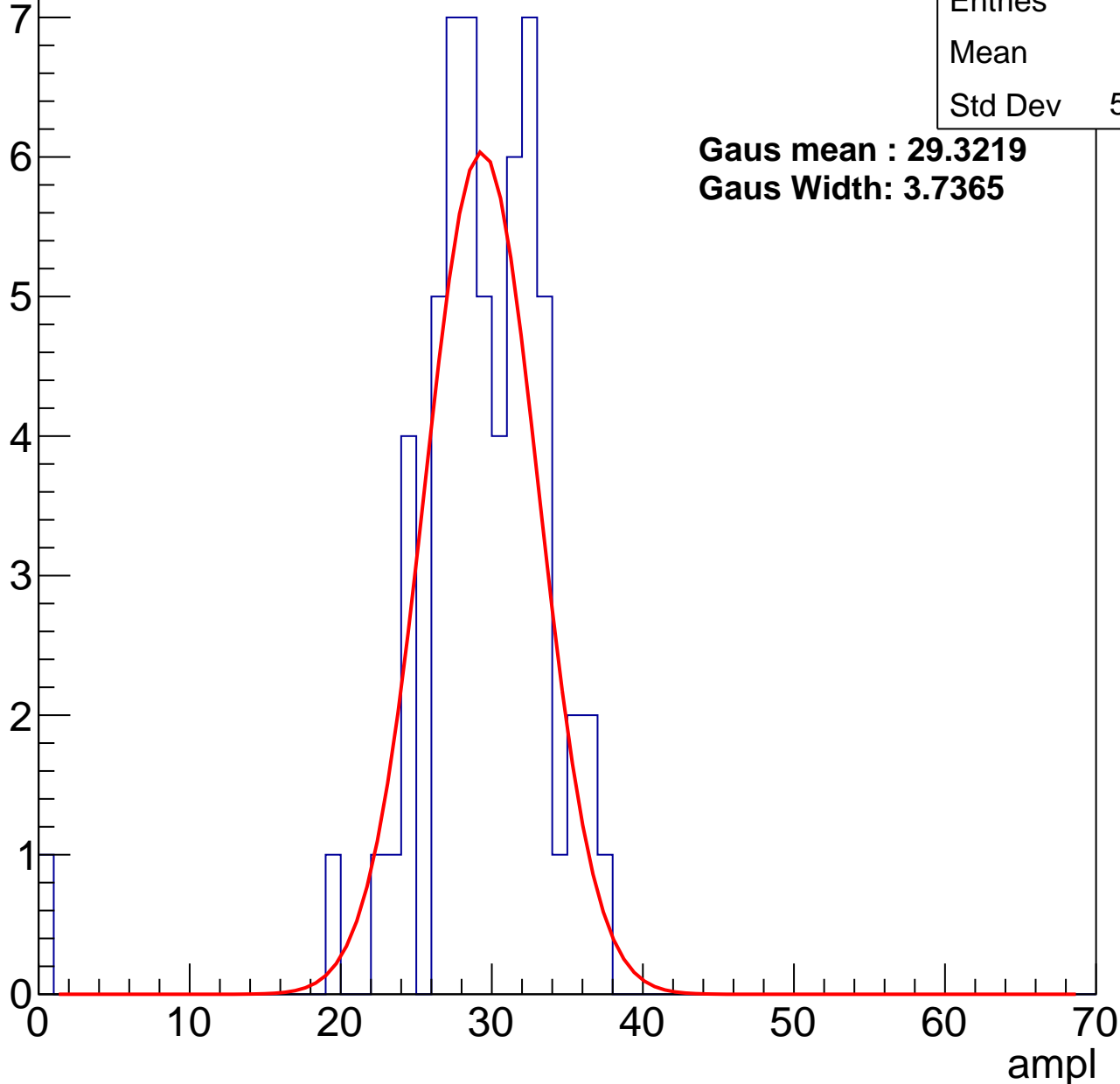
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	28.8
Std Dev	5.218

**Gaus mean : 29.3219**

**Gaus Width: 3.7365**



# B0L001S, U6-ch108, adc1

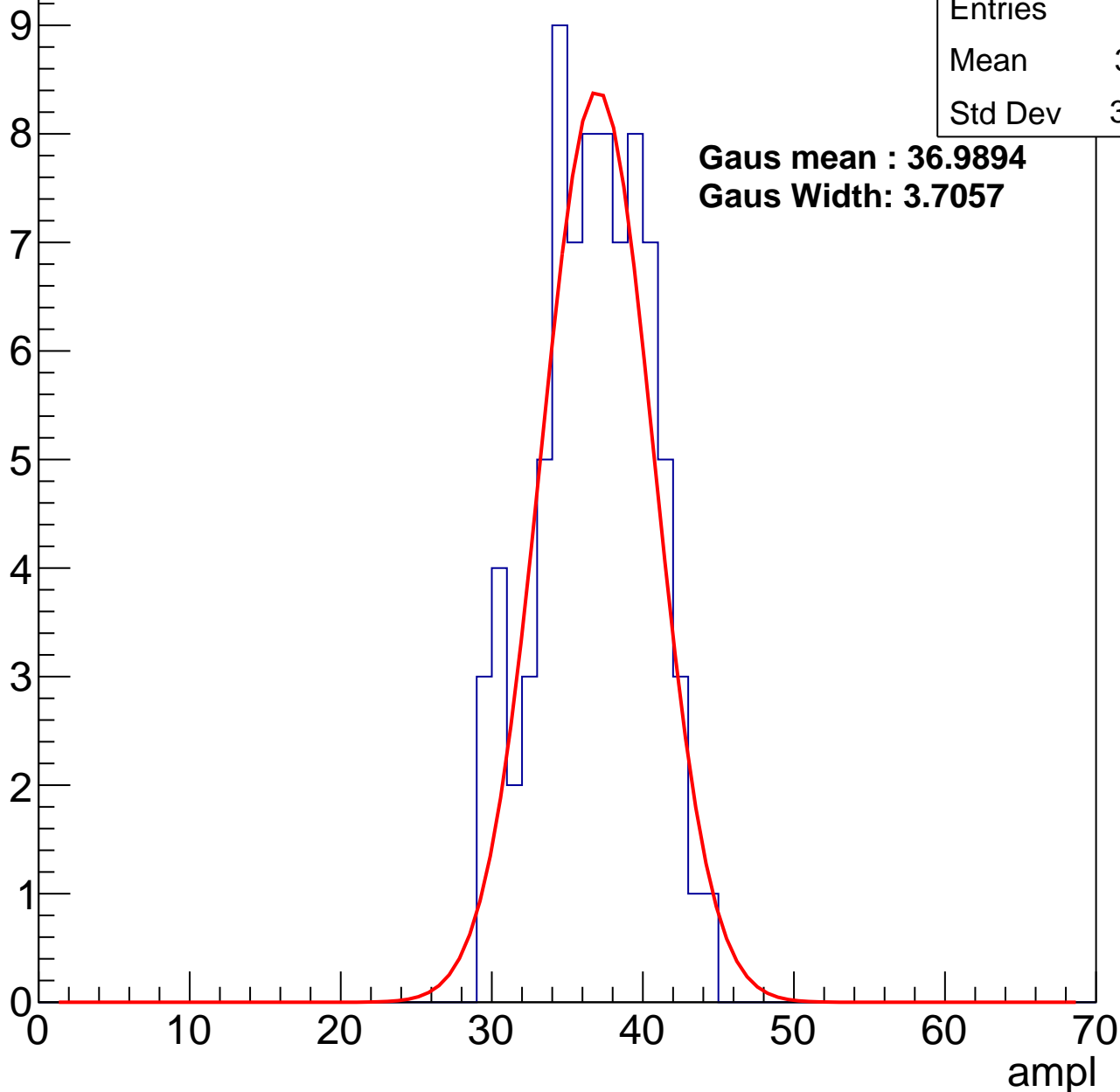
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	36.31
Std Dev	3.575

**Gaus mean : 36.9894**

**Gaus Width: 3.7057**



# B0L001S, U6-ch108, adc2

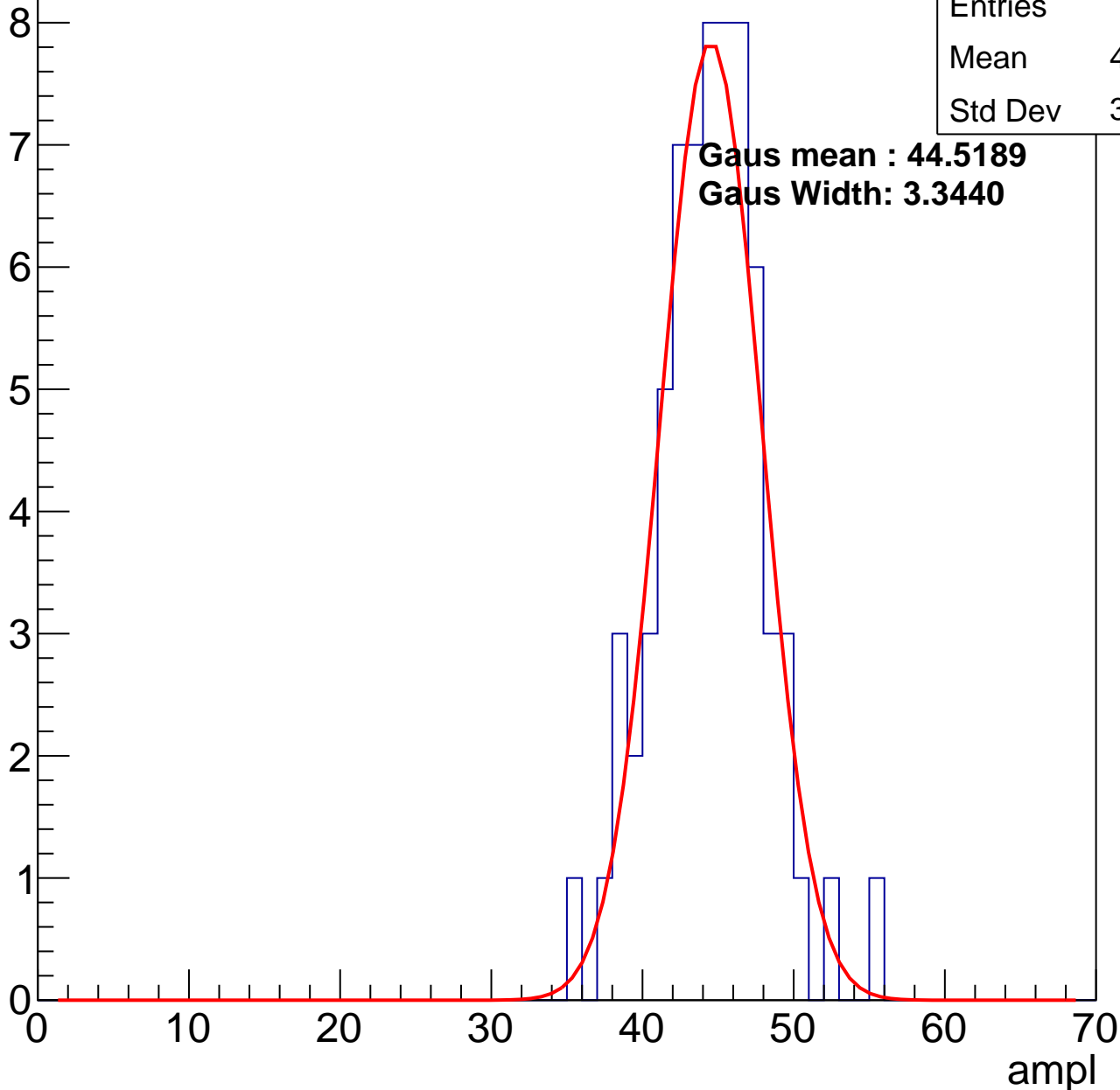
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	44.03
Std Dev	3.544

**Gaus mean : 44.5189**

**Gaus Width: 3.3440**

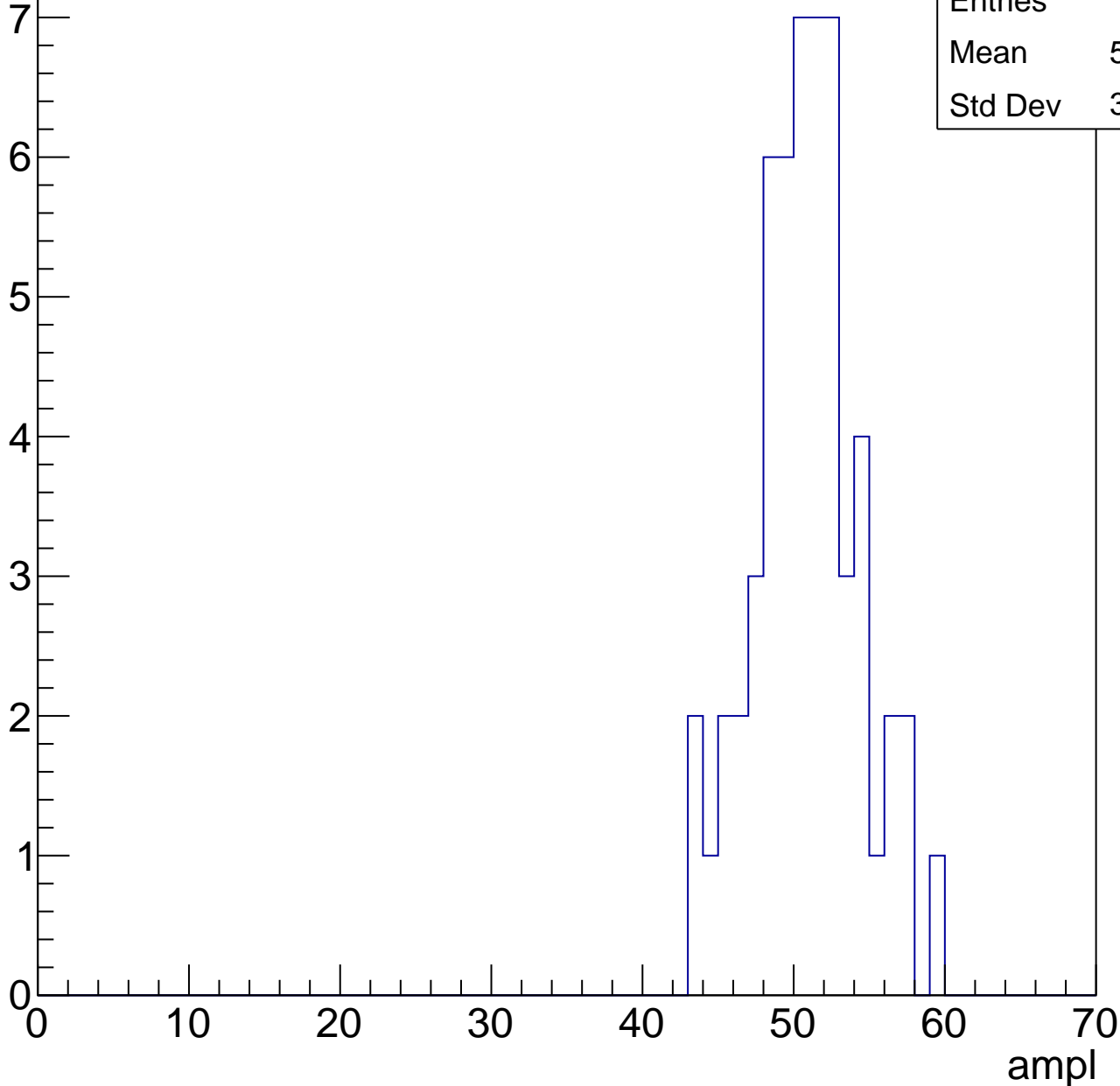


# B0L001S, U6-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

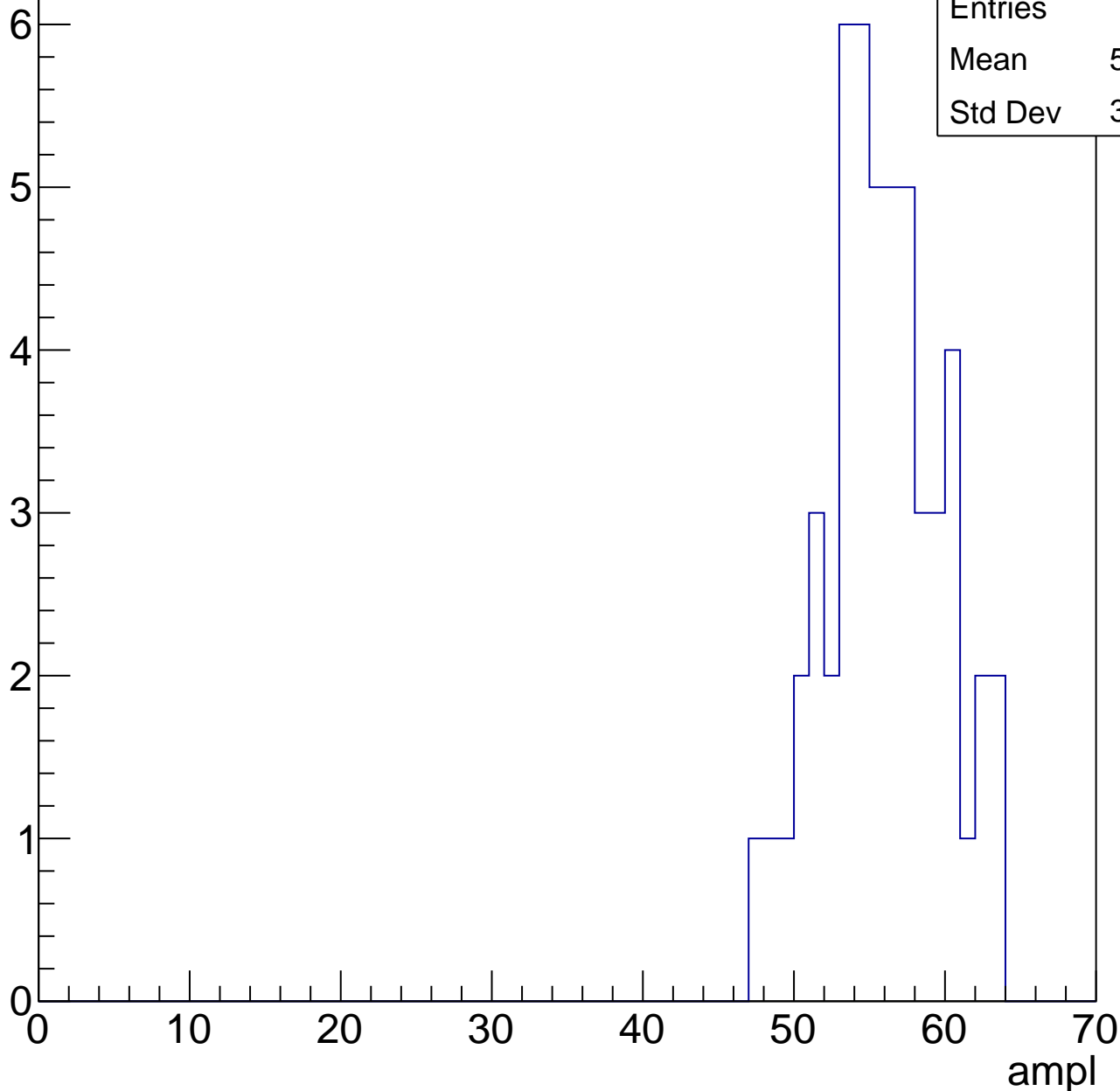
Entries	56
Mean	50.38
Std Dev	3.452



# B0L001S, U6-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	52
Mean	55.48
Std Dev	3.785

# B0L001S, U6-ch108, adc5

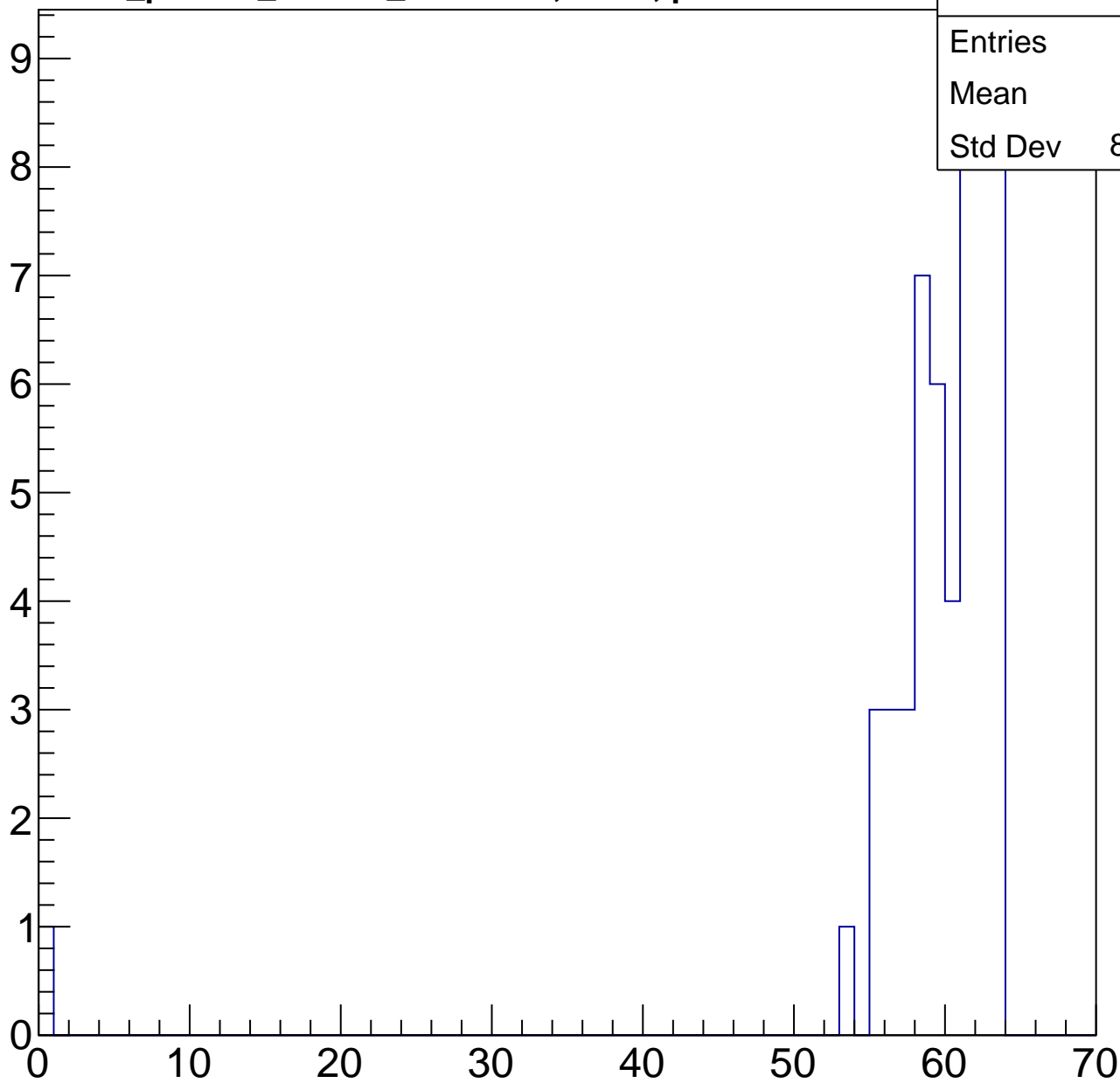
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	53
Mean	58.6
Std Dev	8.515

ampl



# B0L001S, U6-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	60
Std Dev	0

ampl



# B0L001S, U6-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U6-ch109, adc0

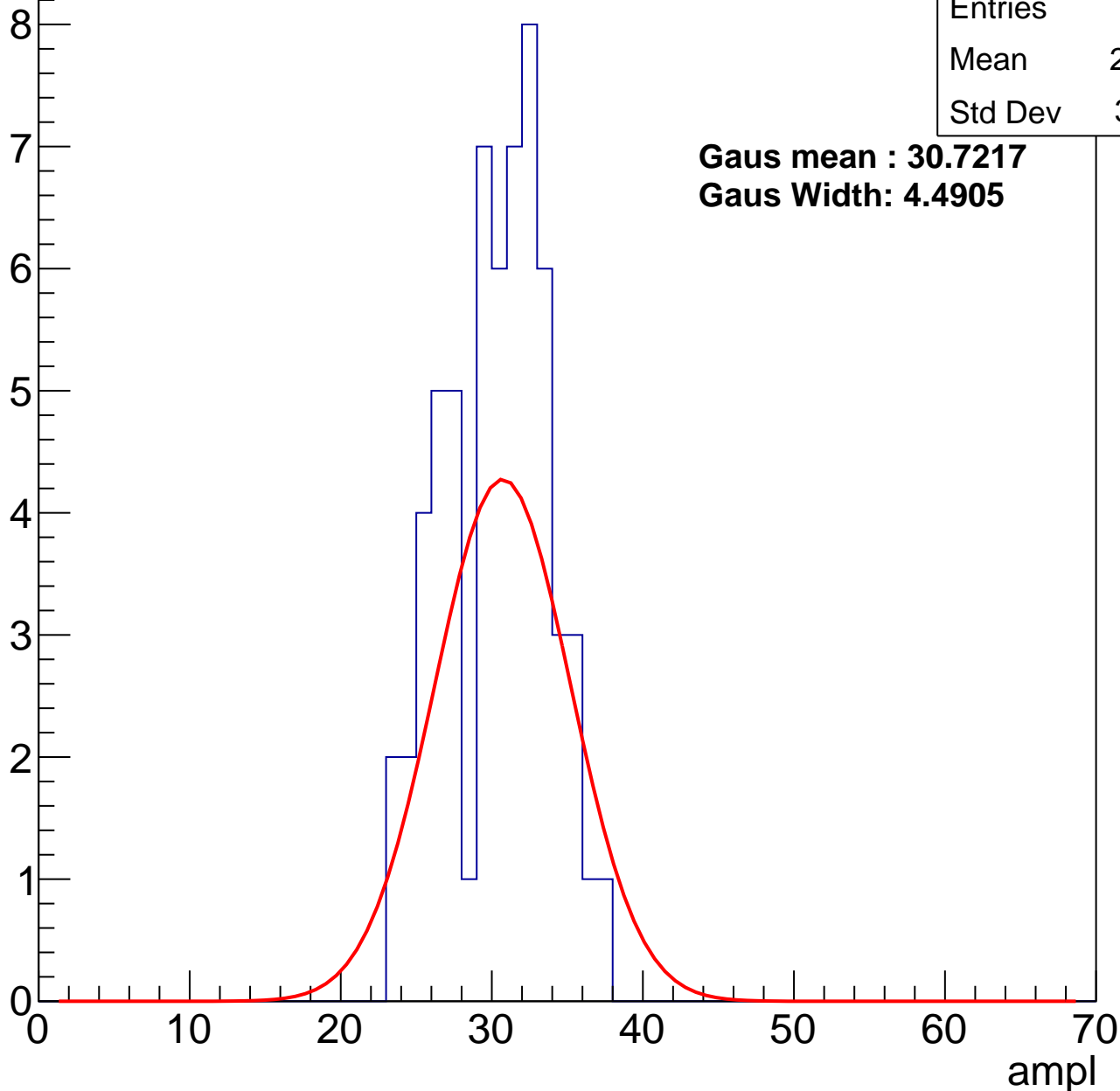
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	29.85
Std Dev	3.401

**Gaus mean : 30.7217**

**Gaus Width: 4.4905**



# B0L001S, U6-ch109, adc1

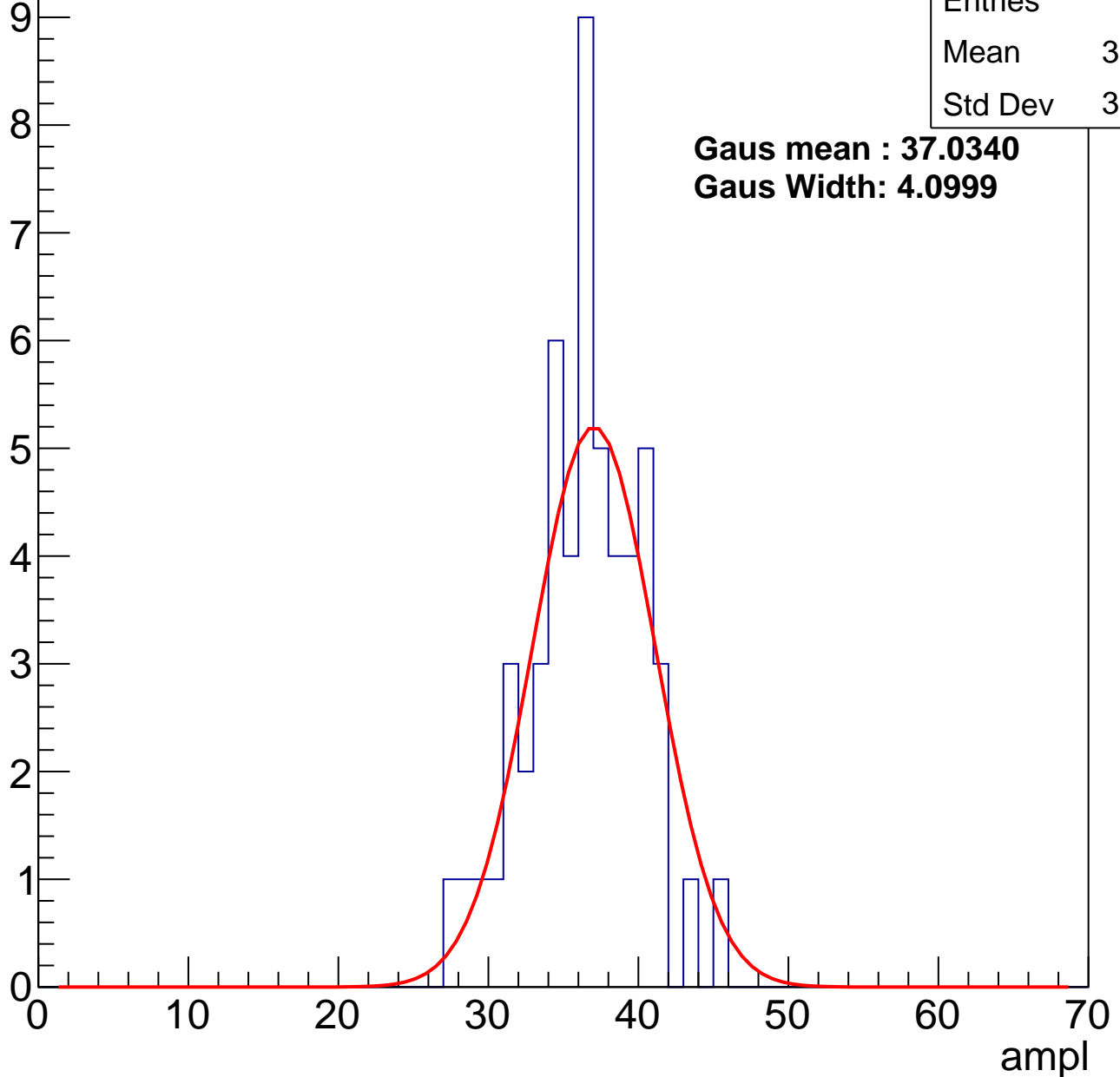
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	35.96
Std Dev	3.687

**Gaus mean : 37.0340**

**Gaus Width: 4.0999**



# B0L001S, U6-ch109, adc2

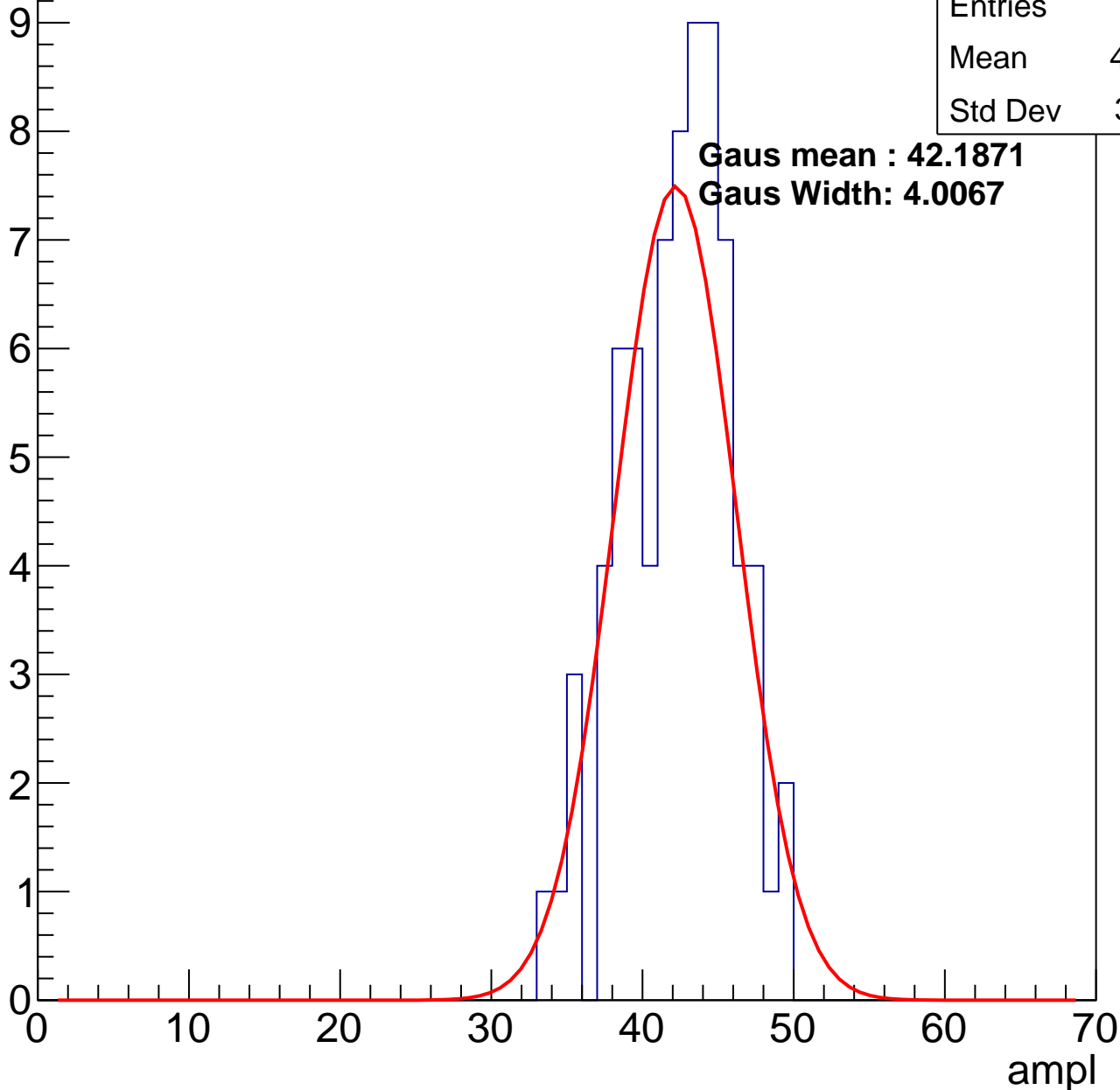
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	41.86
Std Dev	3.571

**Gaus mean : 42.1871**

**Gaus Width: 4.0067**

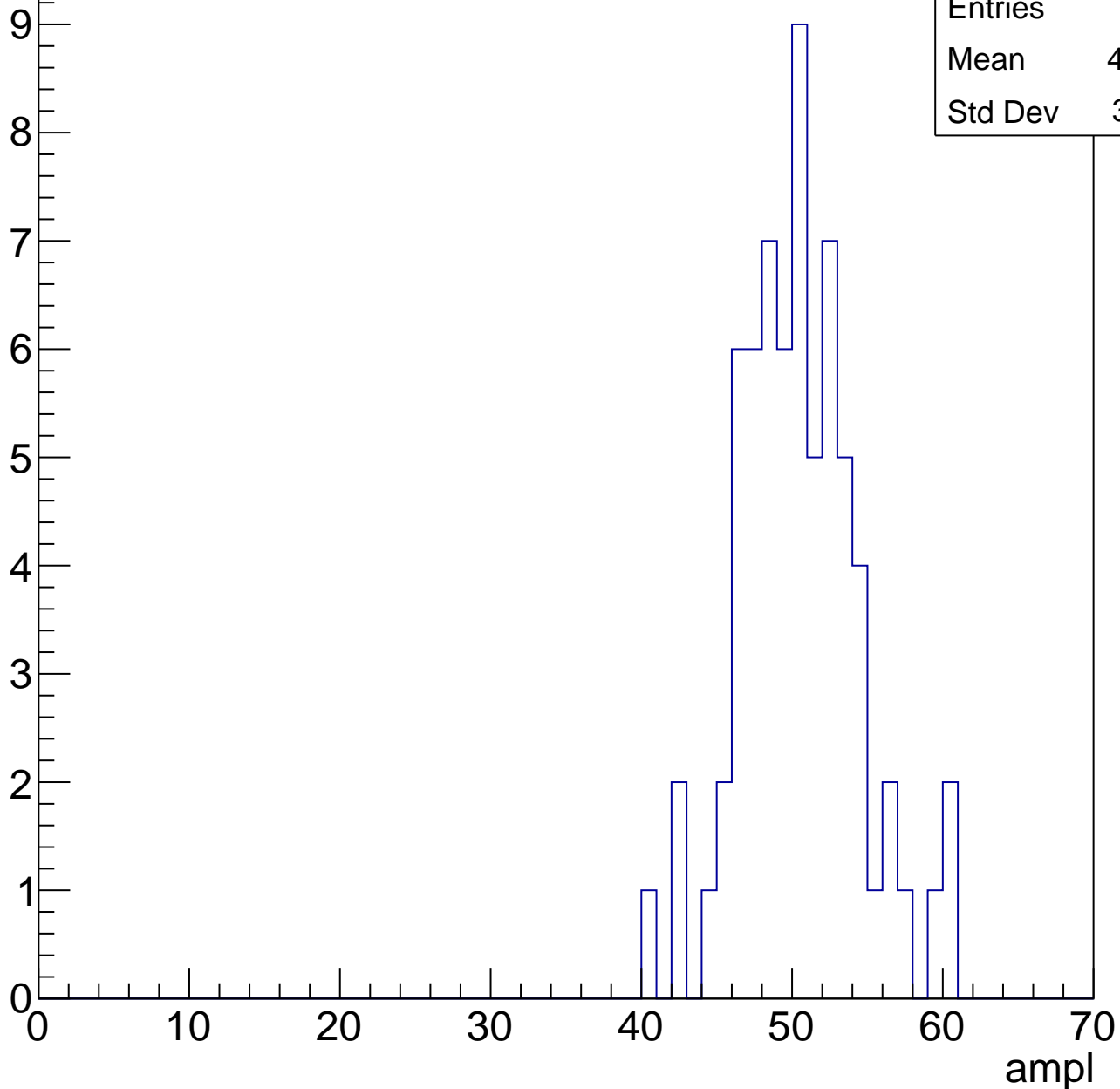


# B0L001S, U6-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	49.99
Std Dev	3.961

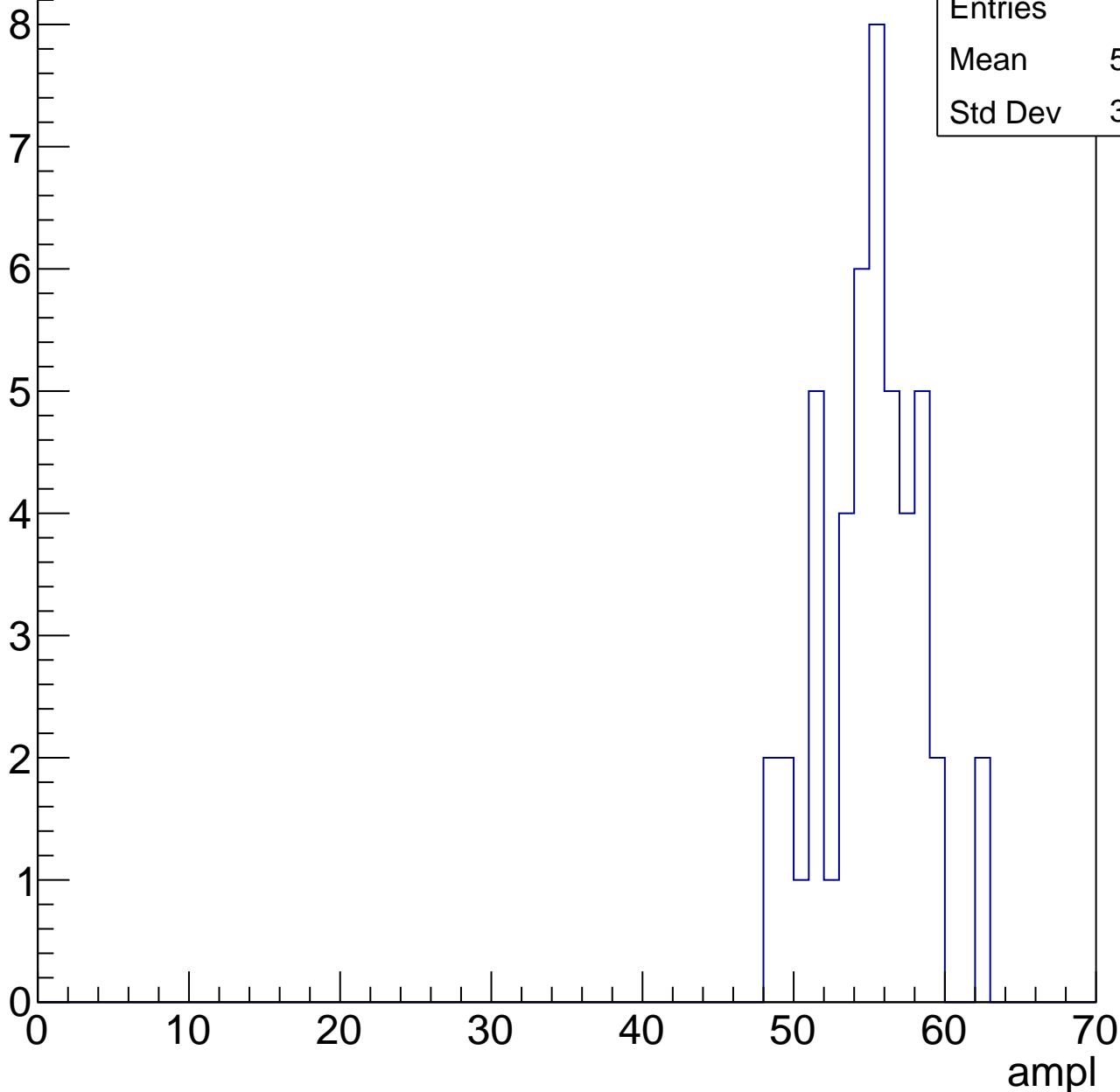


# B0L001S, U6-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	54.62
Std Dev	3.246

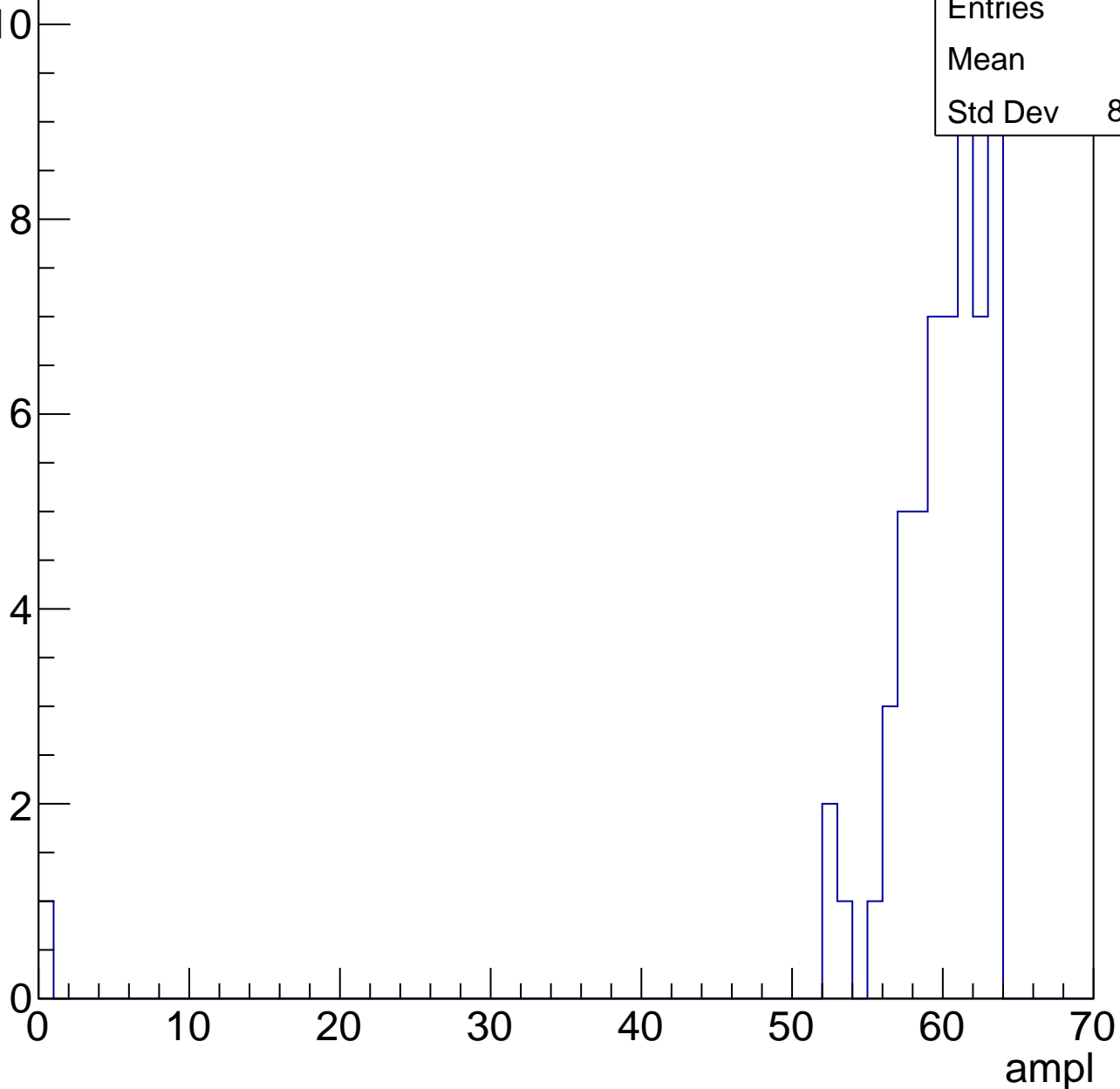


# B0L001S, U6-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

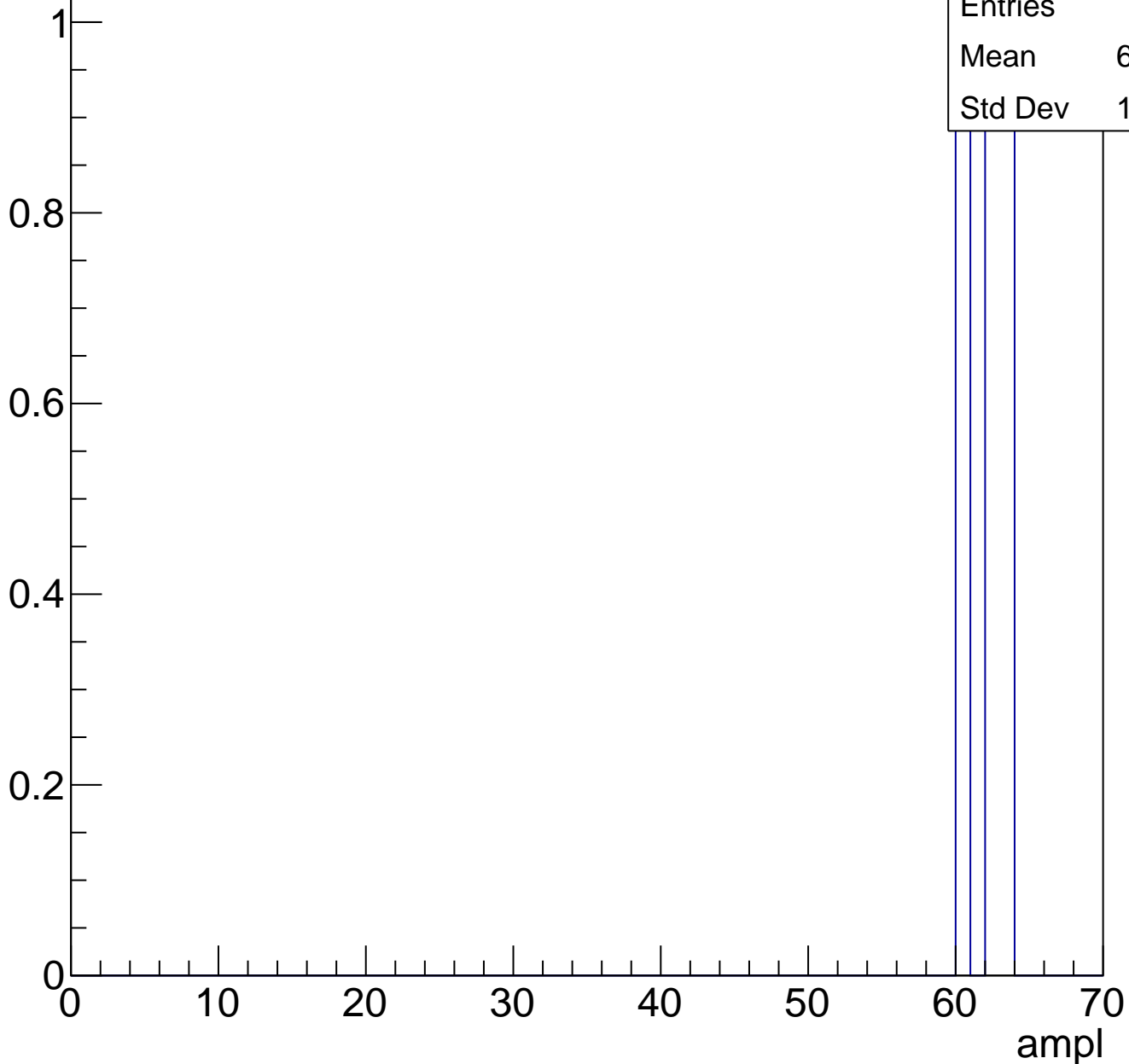
Entries	58
Mean	58.6
Std Dev	8.229



# B0L001S, U6-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U6-ch110, adc0

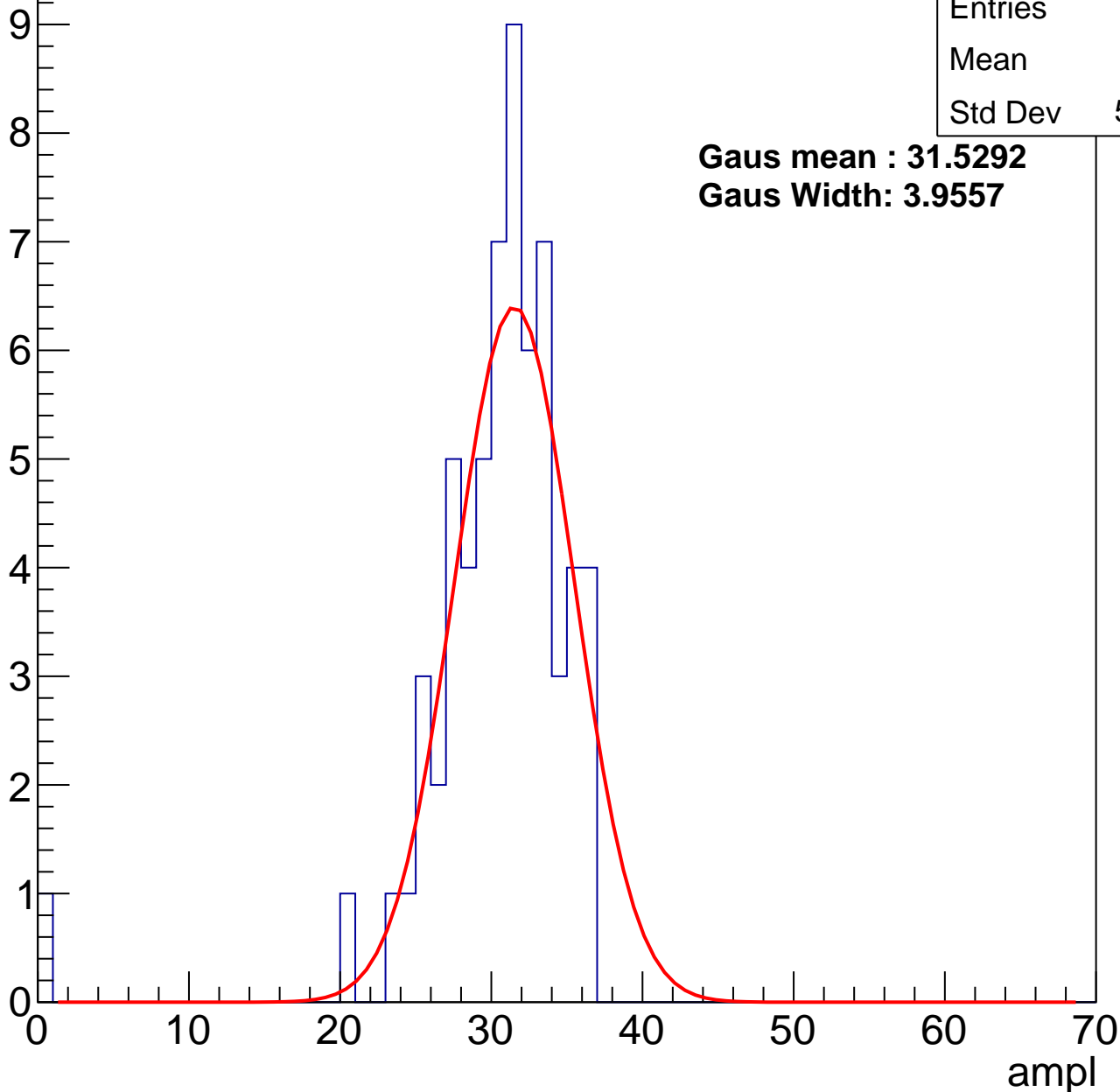
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	29.9
Std Dev	5.111

**Gaus mean : 31.5292**

**Gaus Width: 3.9557**



# B0L001S, U6-ch110, adc1

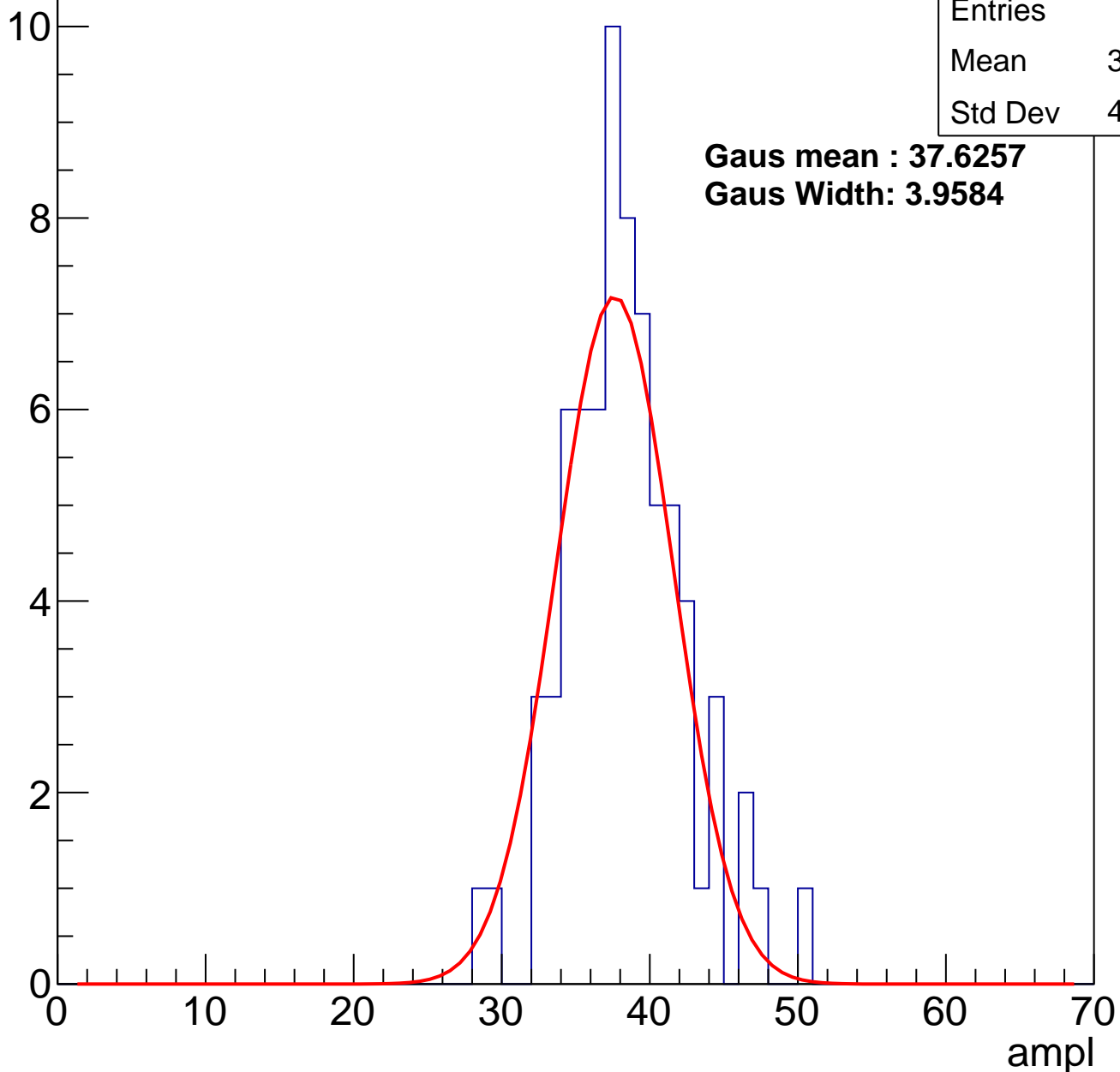
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	73
Mean	37.89
Std Dev	4.002

**Gaus mean : 37.6257**

**Gaus Width: 3.9584**

Entry



# B0L001S, U6-ch110, adc2

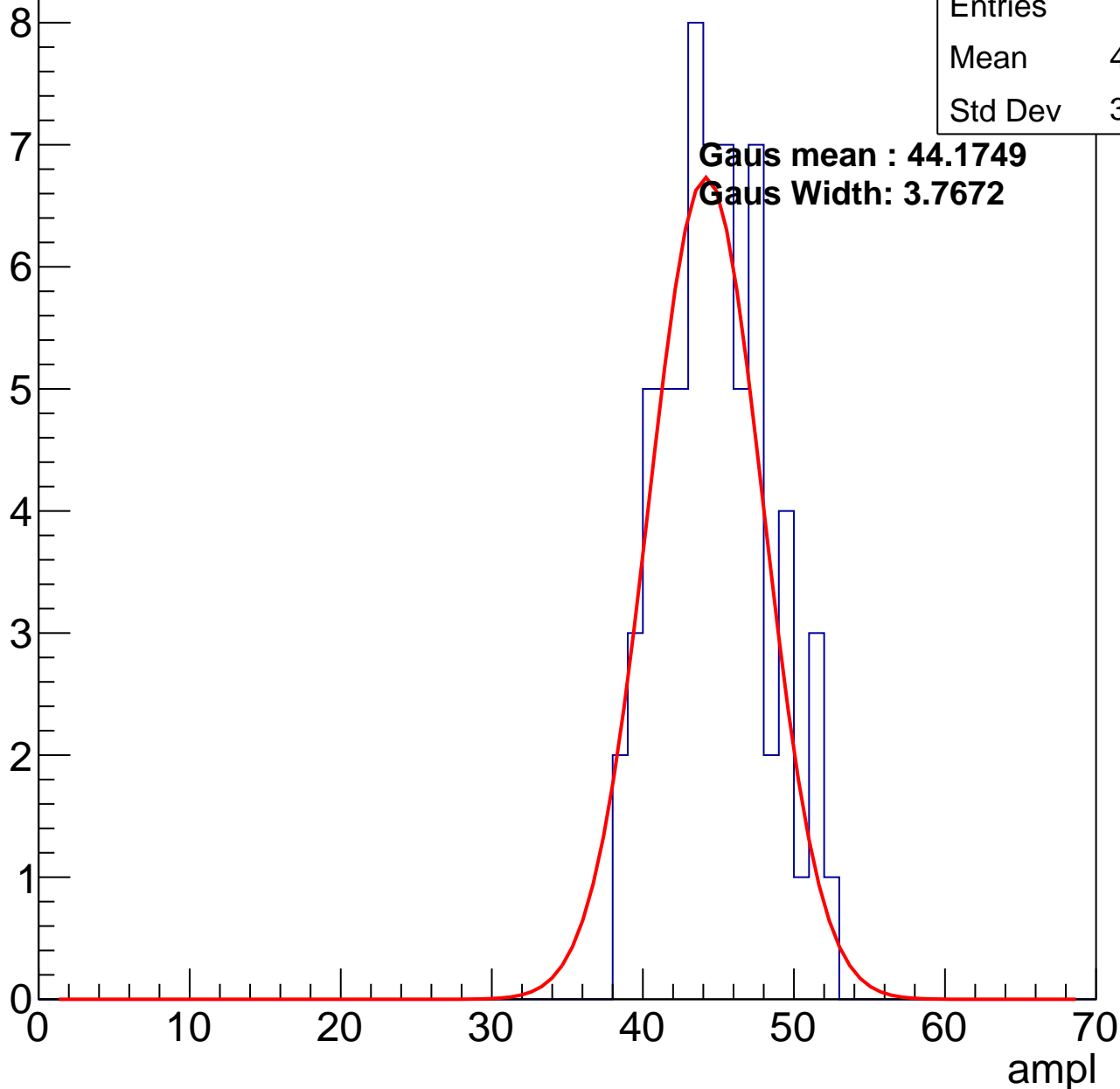
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	44.32
Std Dev	3.424

**Gaus mean : 44.1749**

**Gaus Width: 3.7672**

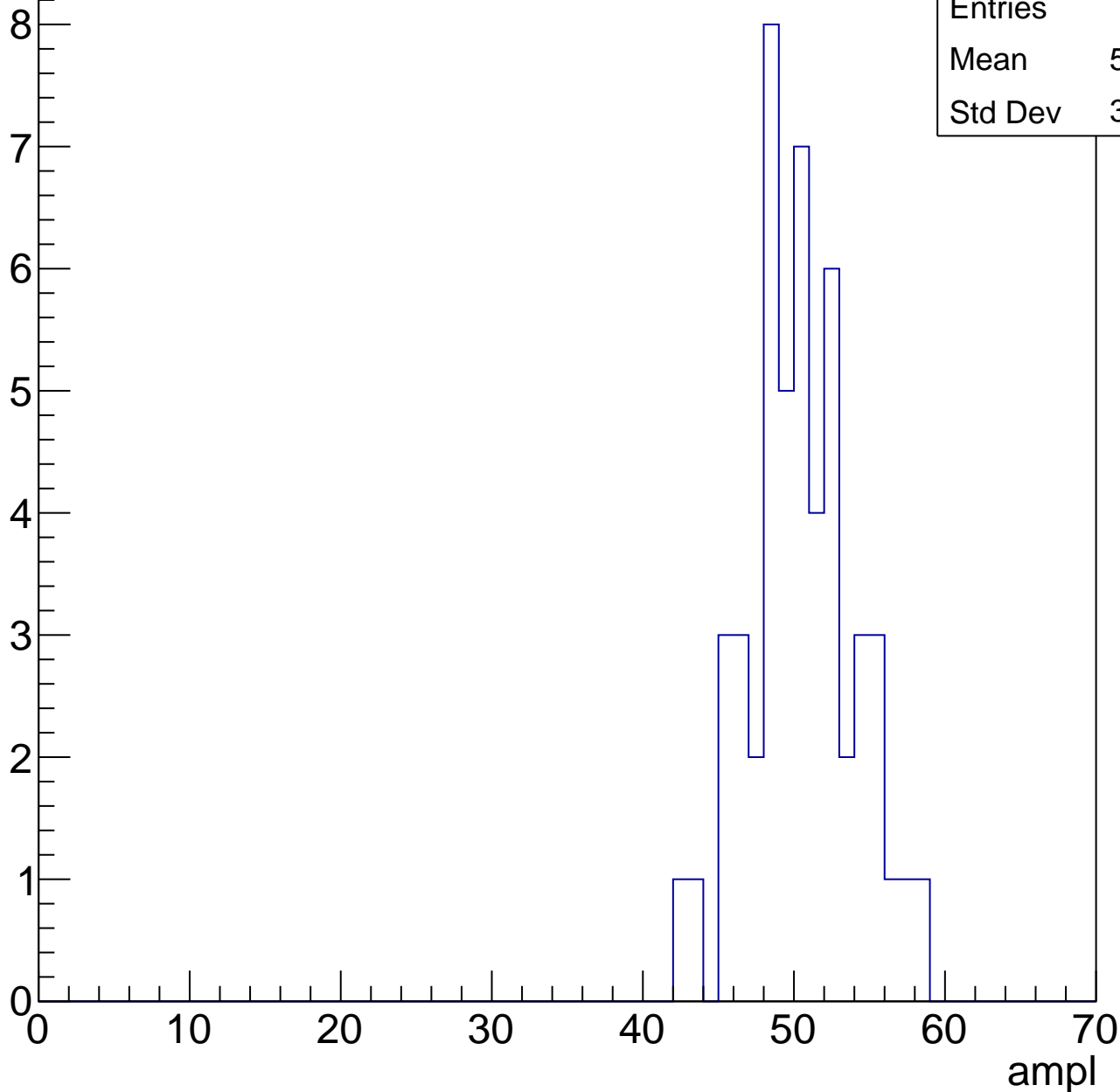


# B0L001S, U6-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	50.02
Std Dev	3.456

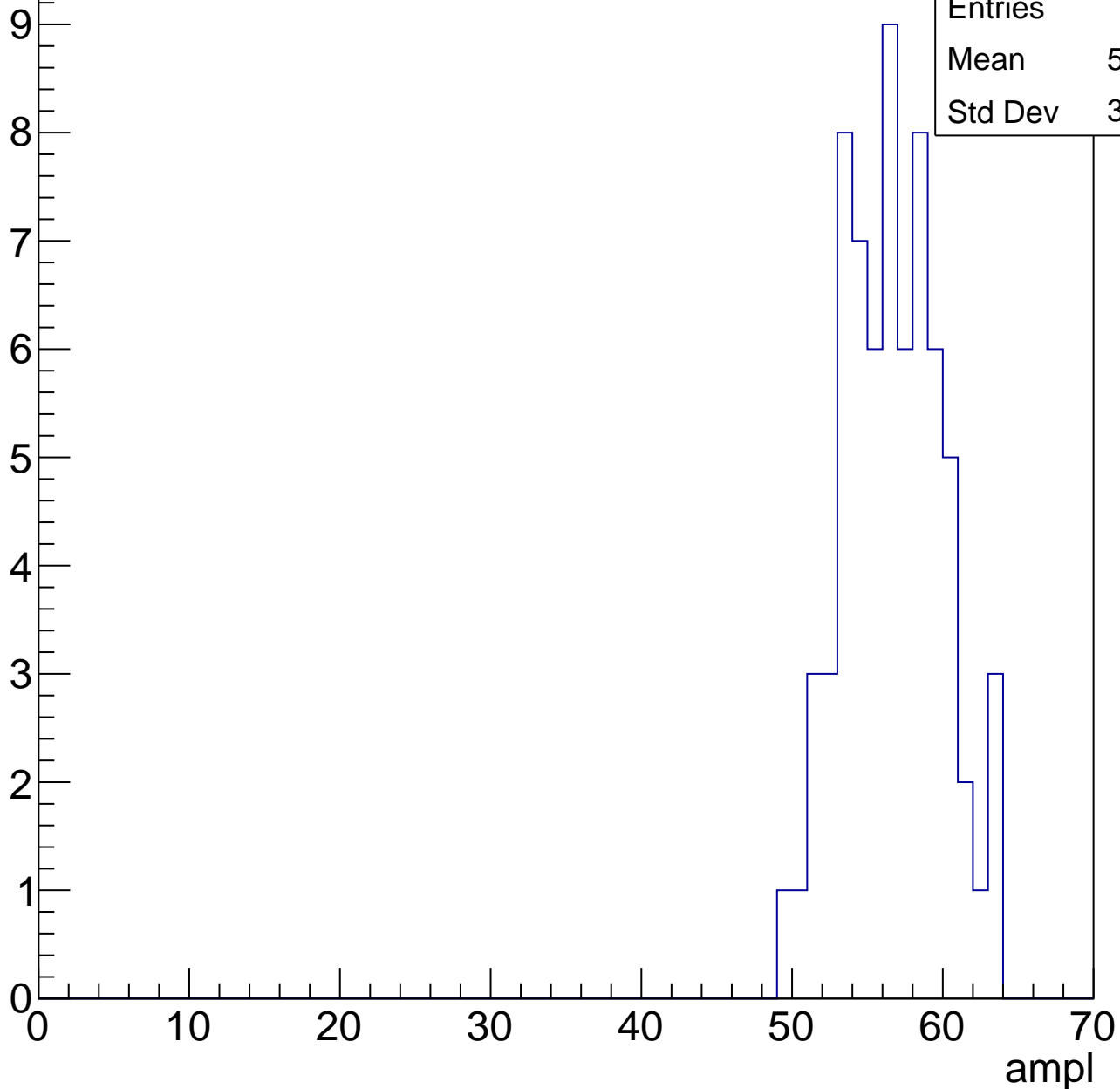


# B0L001S, U6-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	56.19
Std Dev	3.223

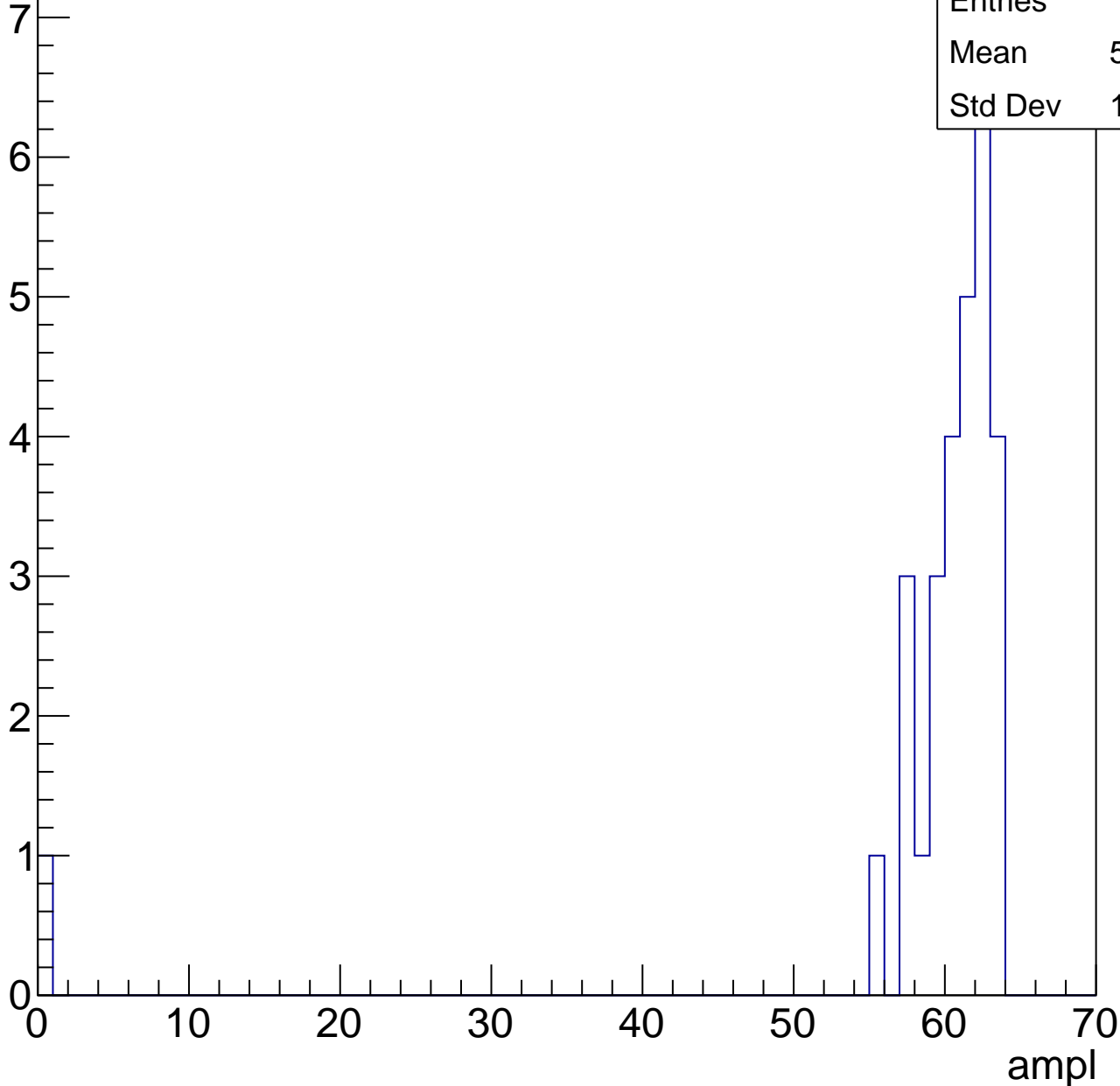


# B0L001S, U6-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

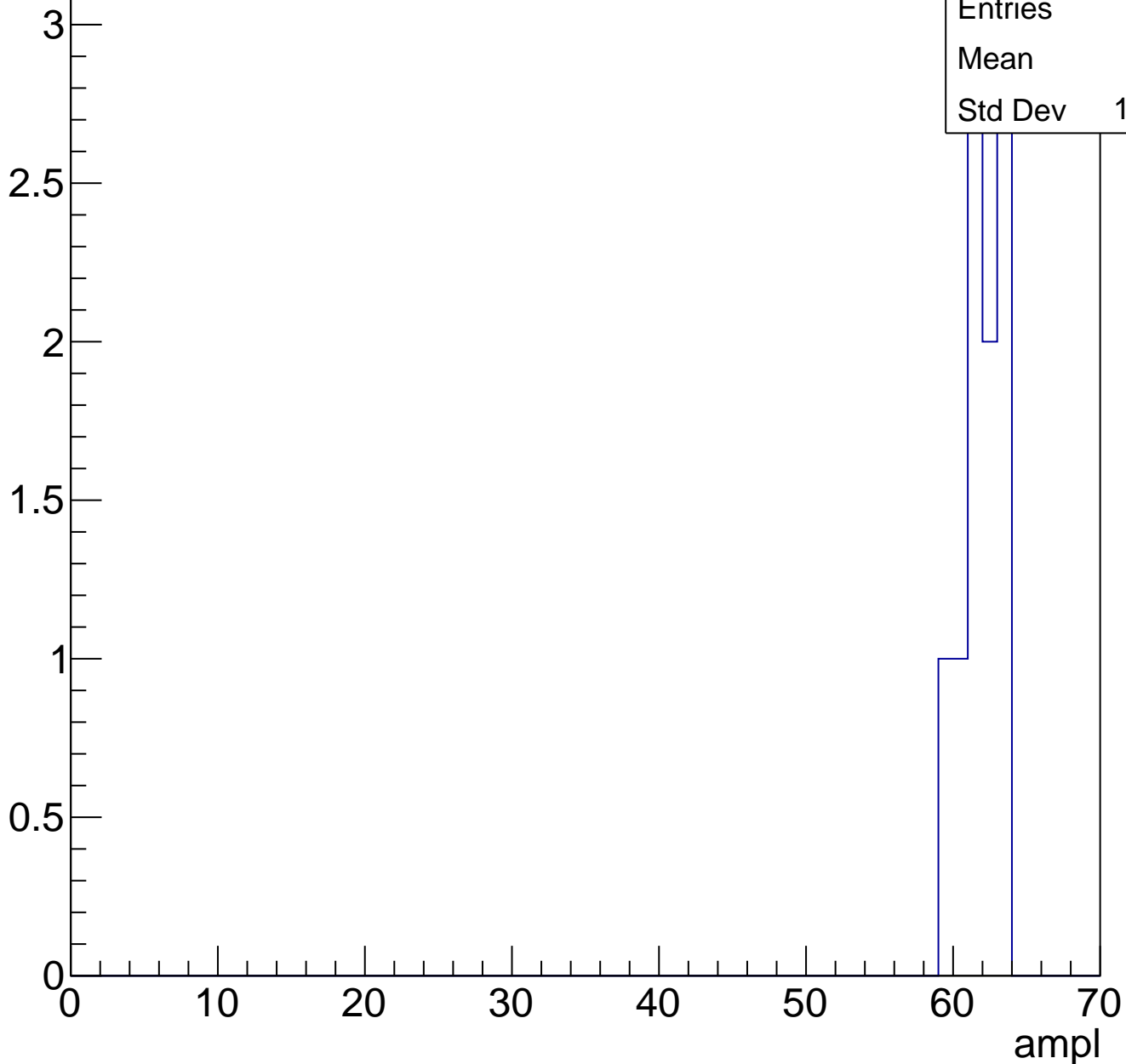
Entries	29
Mean	58.34
Std Dev	11.22



# B0L001S, U6-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch111, adc0

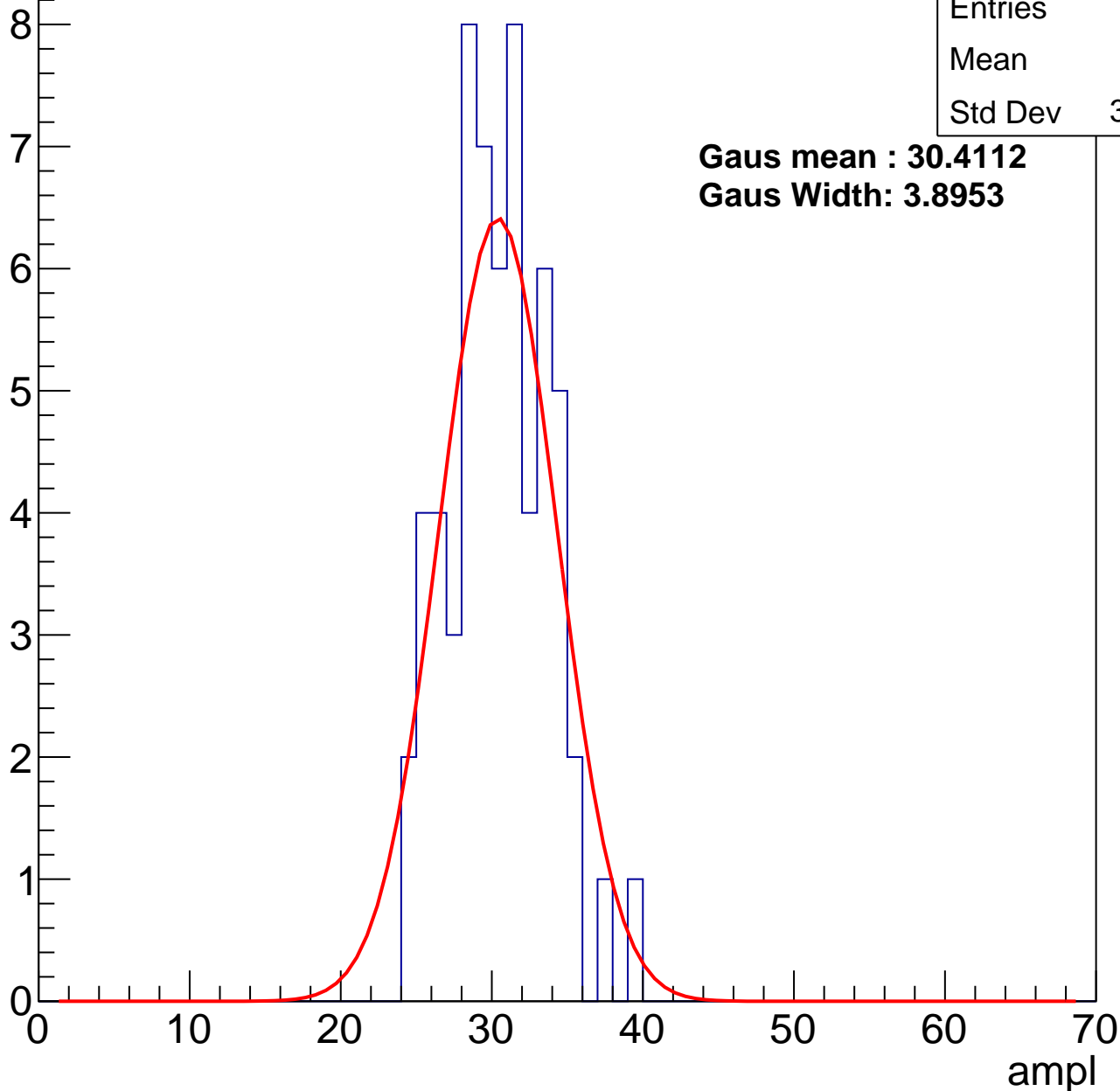
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	30
Std Dev	3.239

**Gaus mean : 30.4112**

**Gaus Width: 3.8953**



# B0L001S, U6-ch111, adc1

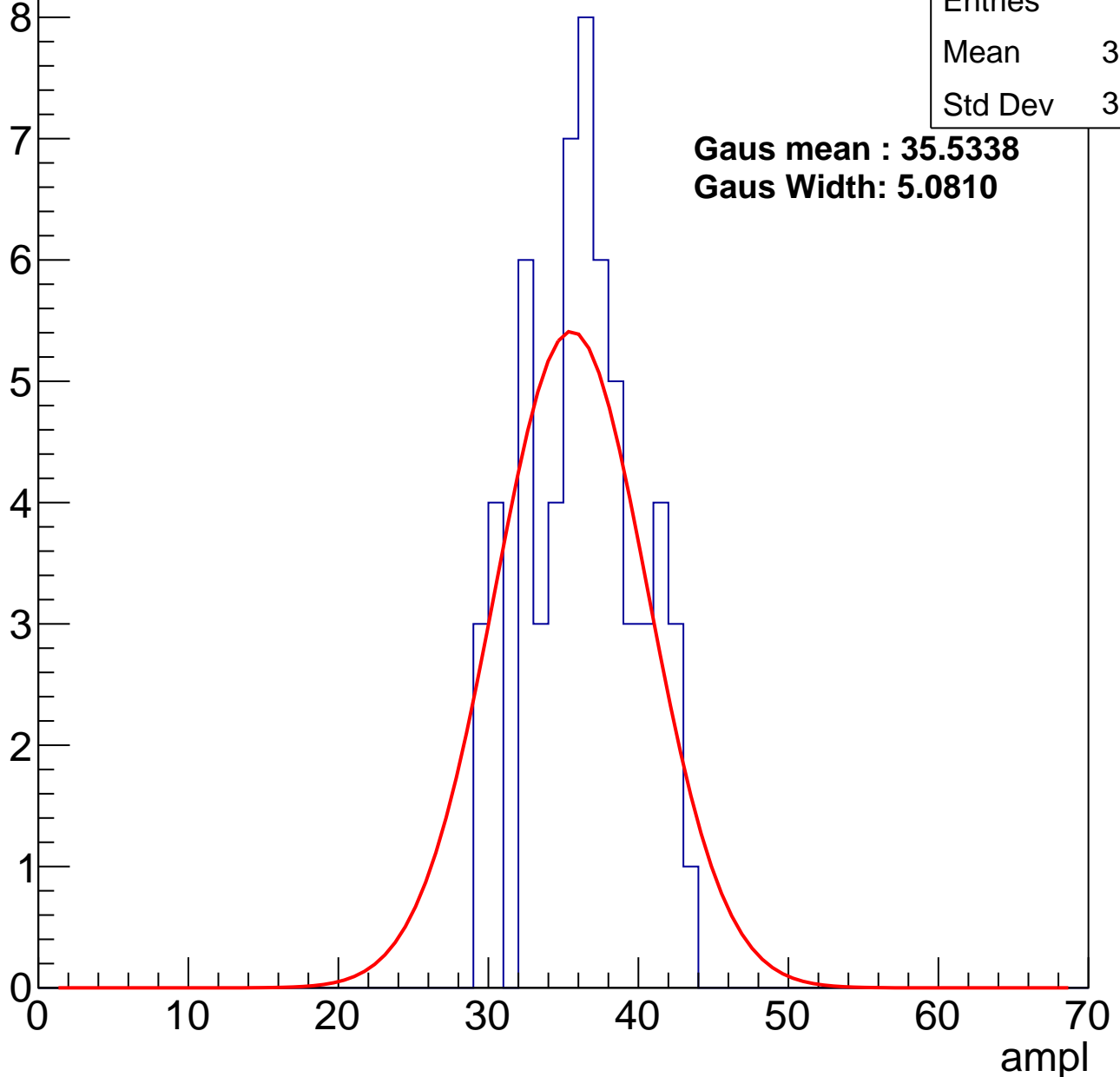
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	35.82
Std Dev	3.635

**Gaus mean : 35.5338**

**Gaus Width: 5.0810**

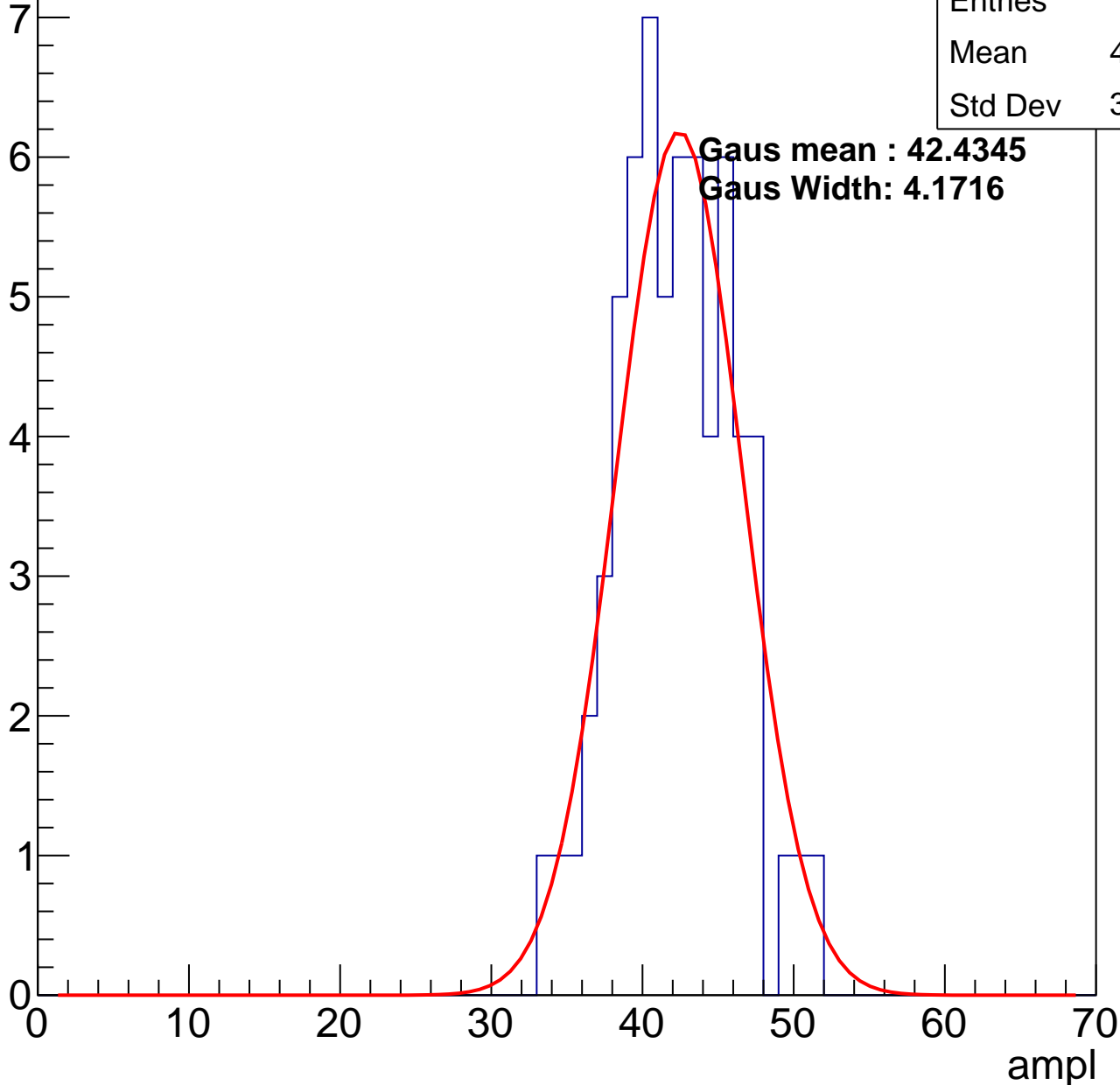


# B0L001S, U6-ch111, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	41.75
Std Dev	3.828



# B0L001S, U6-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

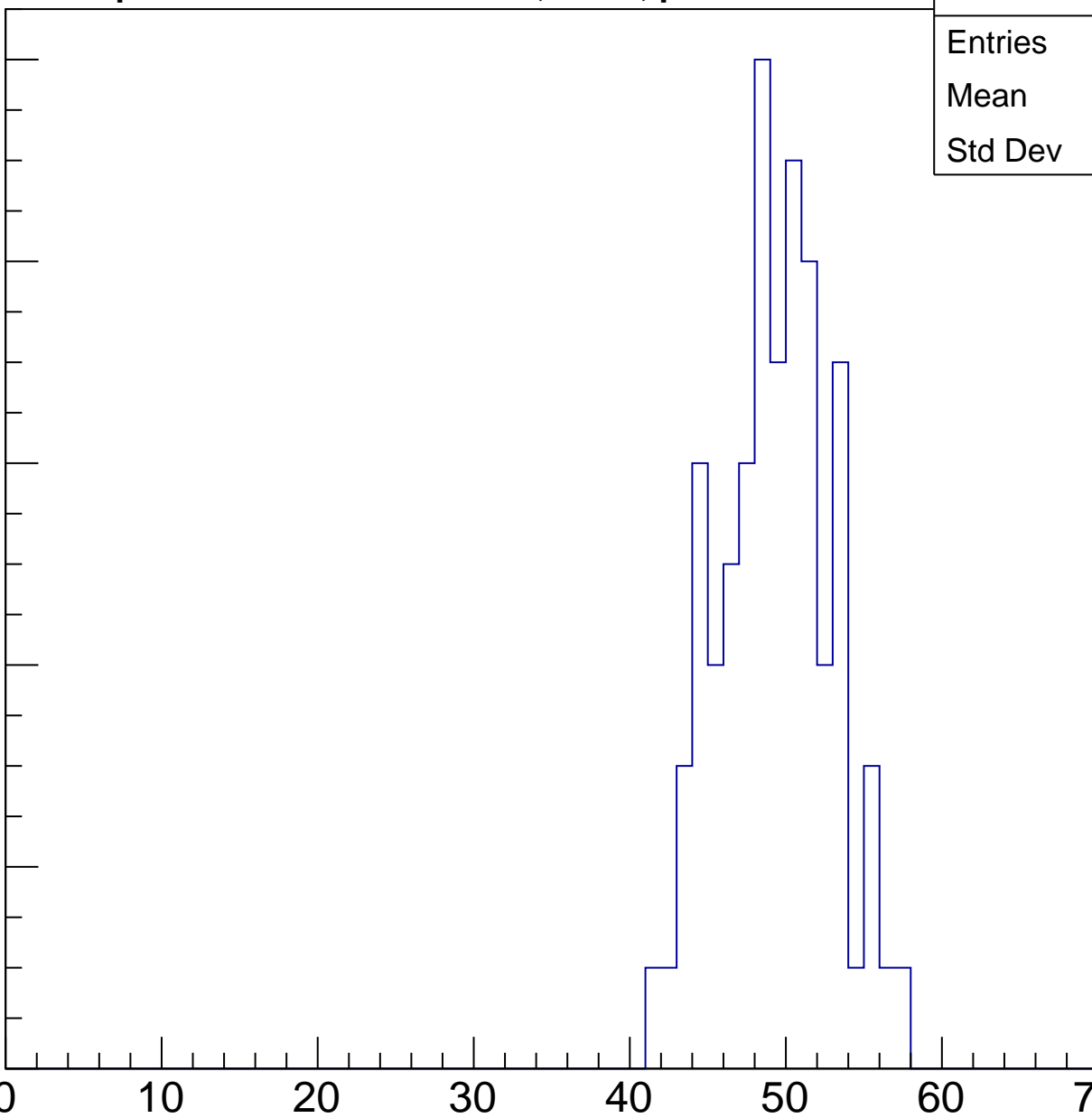
Entries	77
Mean	48.83
Std Dev	3.507

Entry

10  
8  
6  
4  
2  
0

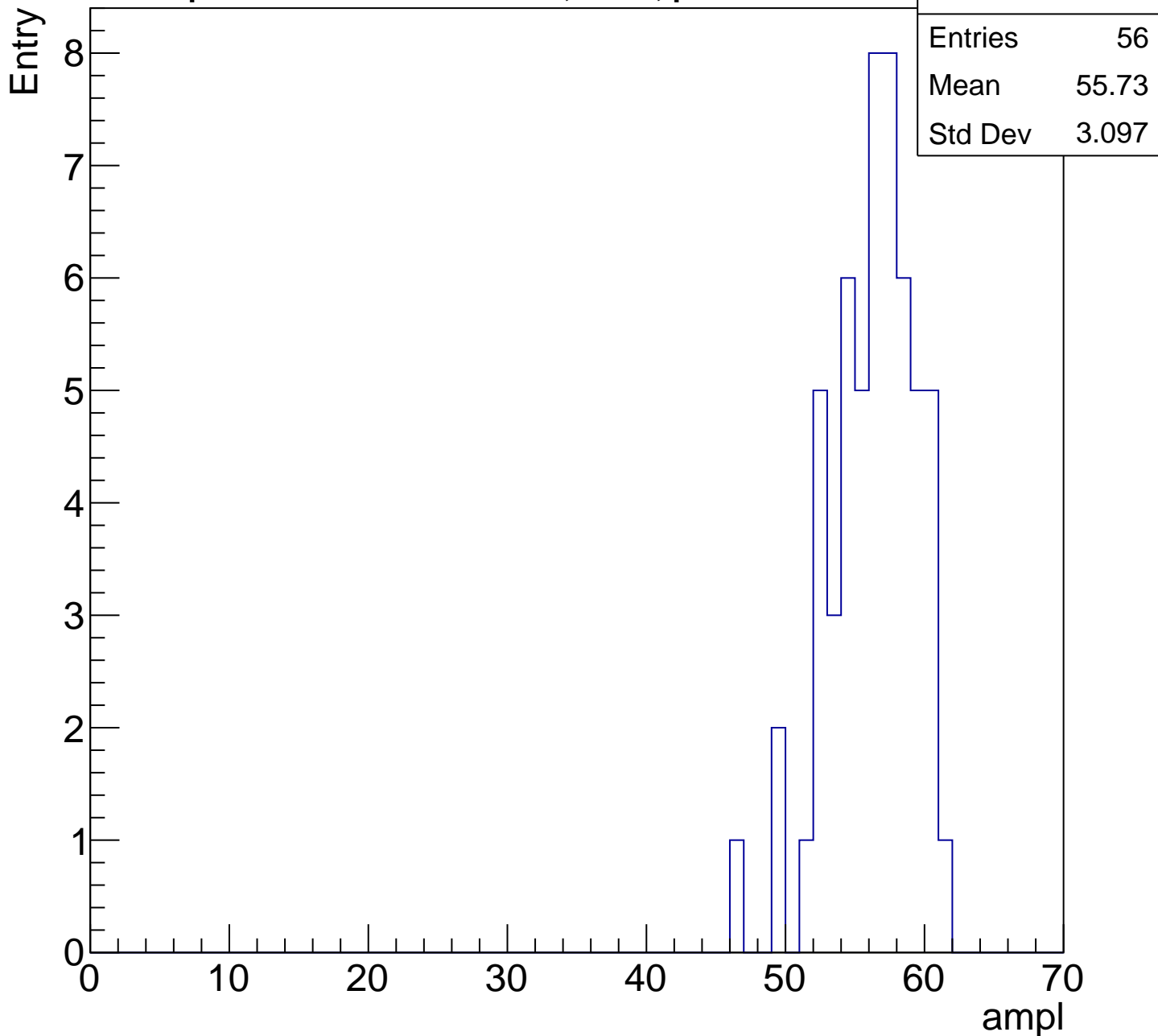
0 10 20 30 40 50 60 70

ampl



# B0L001S, U6-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

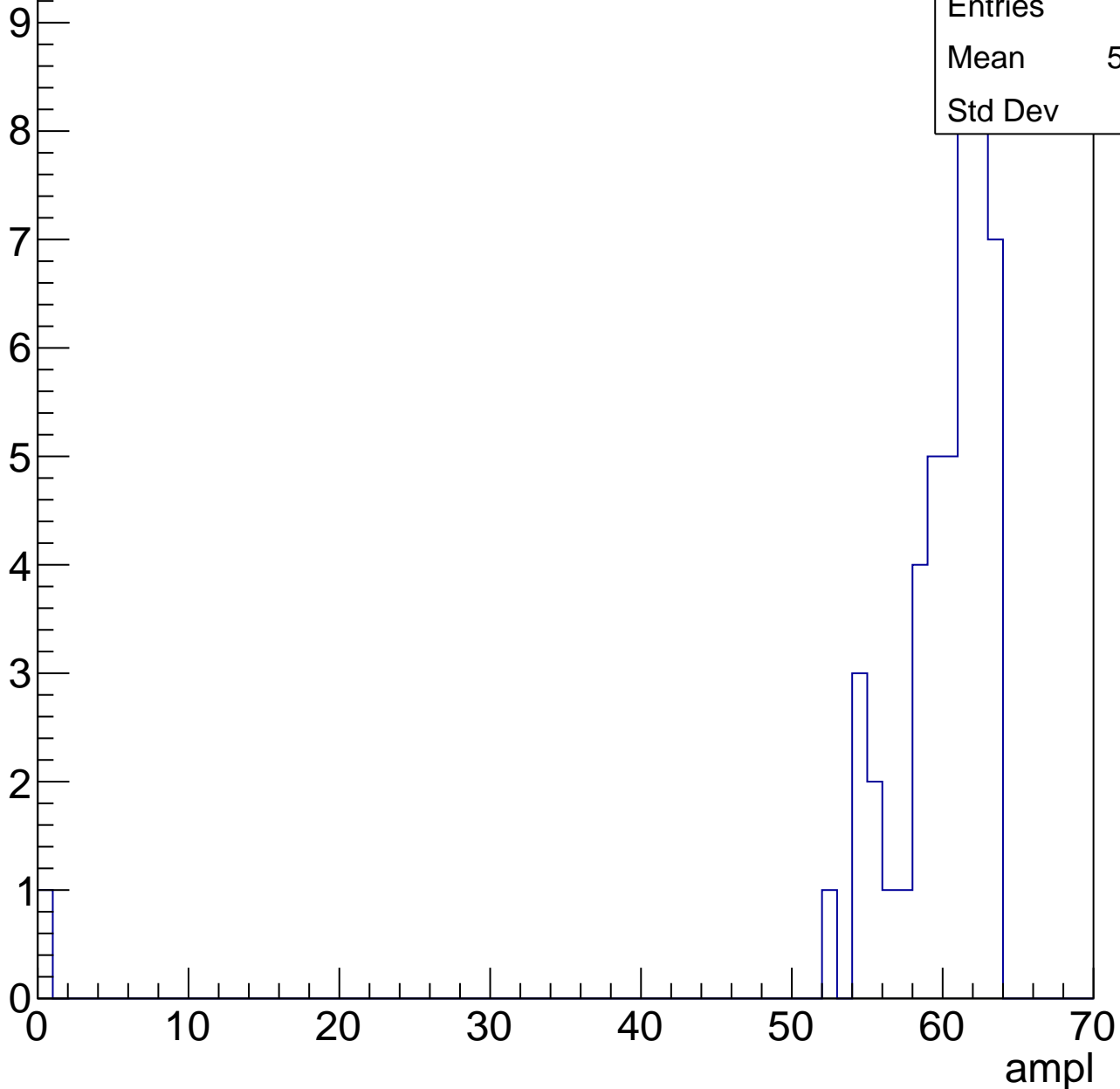


# B0L001S, U6-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	58.58
Std Dev	8.99



# B0L001S, U6-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L001S, U6-ch112, adc0

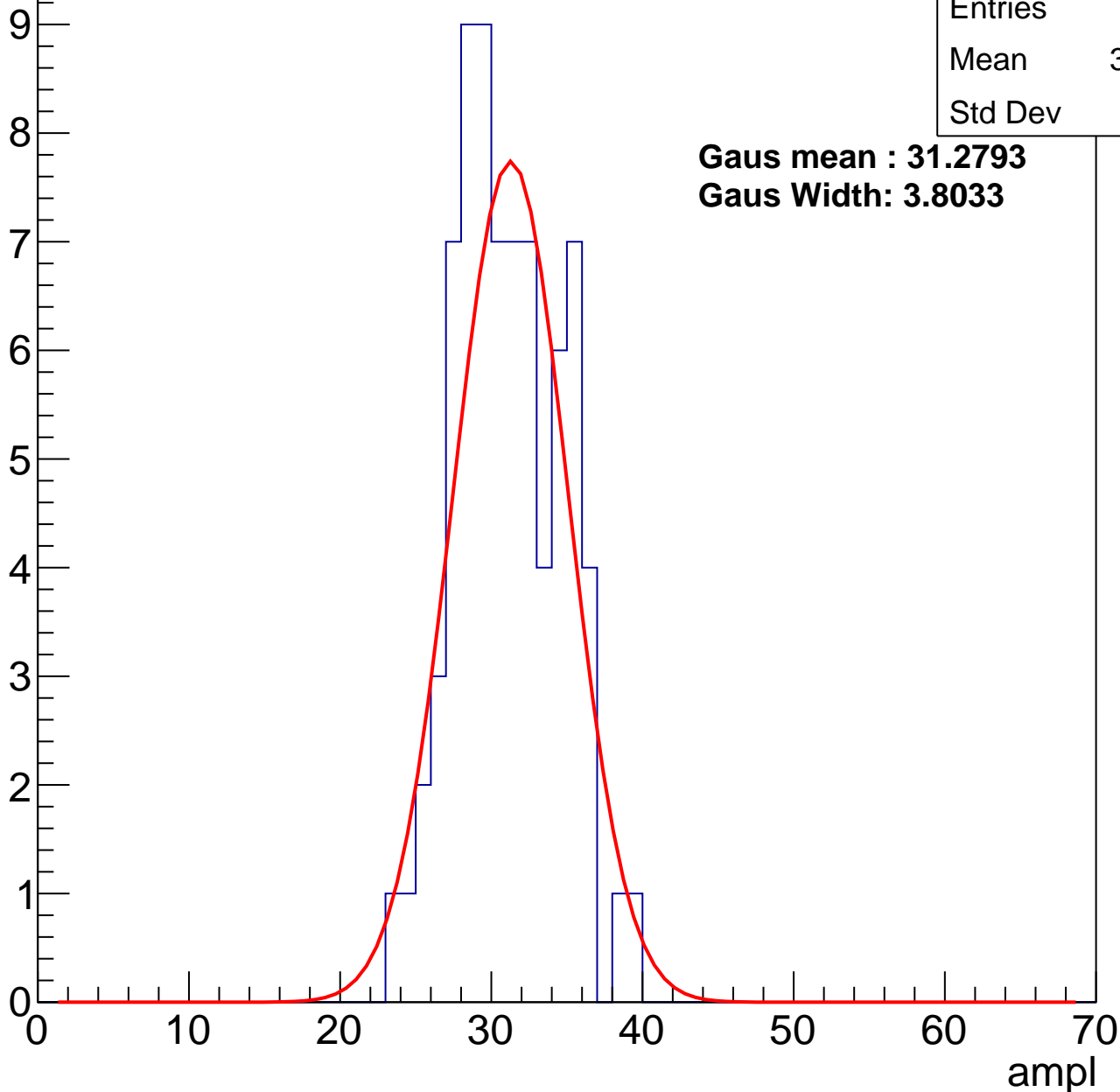
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	30.66
Std Dev	3.42

**Gaus mean : 31.2793**

**Gaus Width: 3.8033**



# B0L001S, U6-ch112, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	63
Mean	36.79
Std Dev	3.414

**Gaus mean : 37.9736**

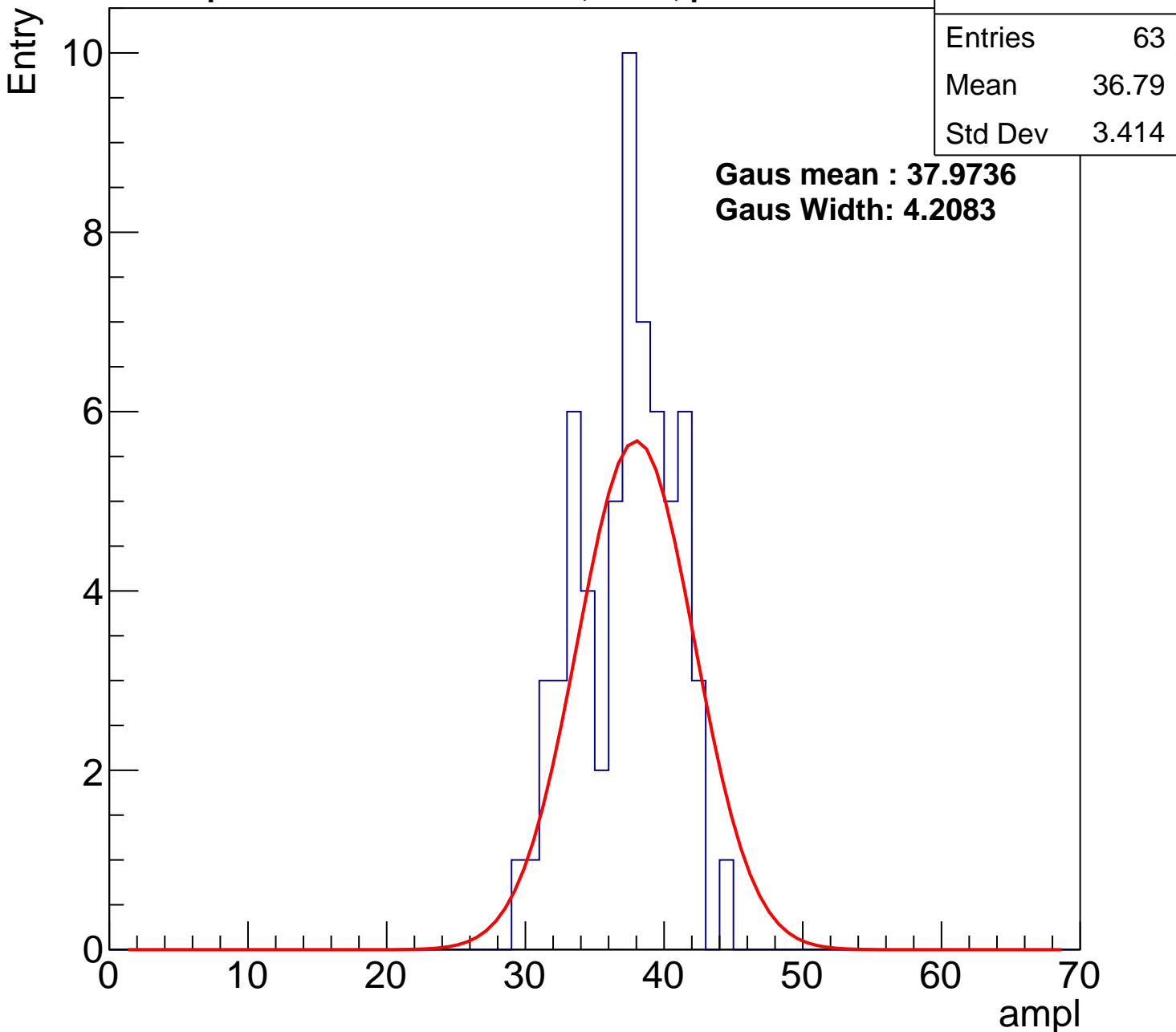
**Gaus Width: 4.2083**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U6-ch112, adc2

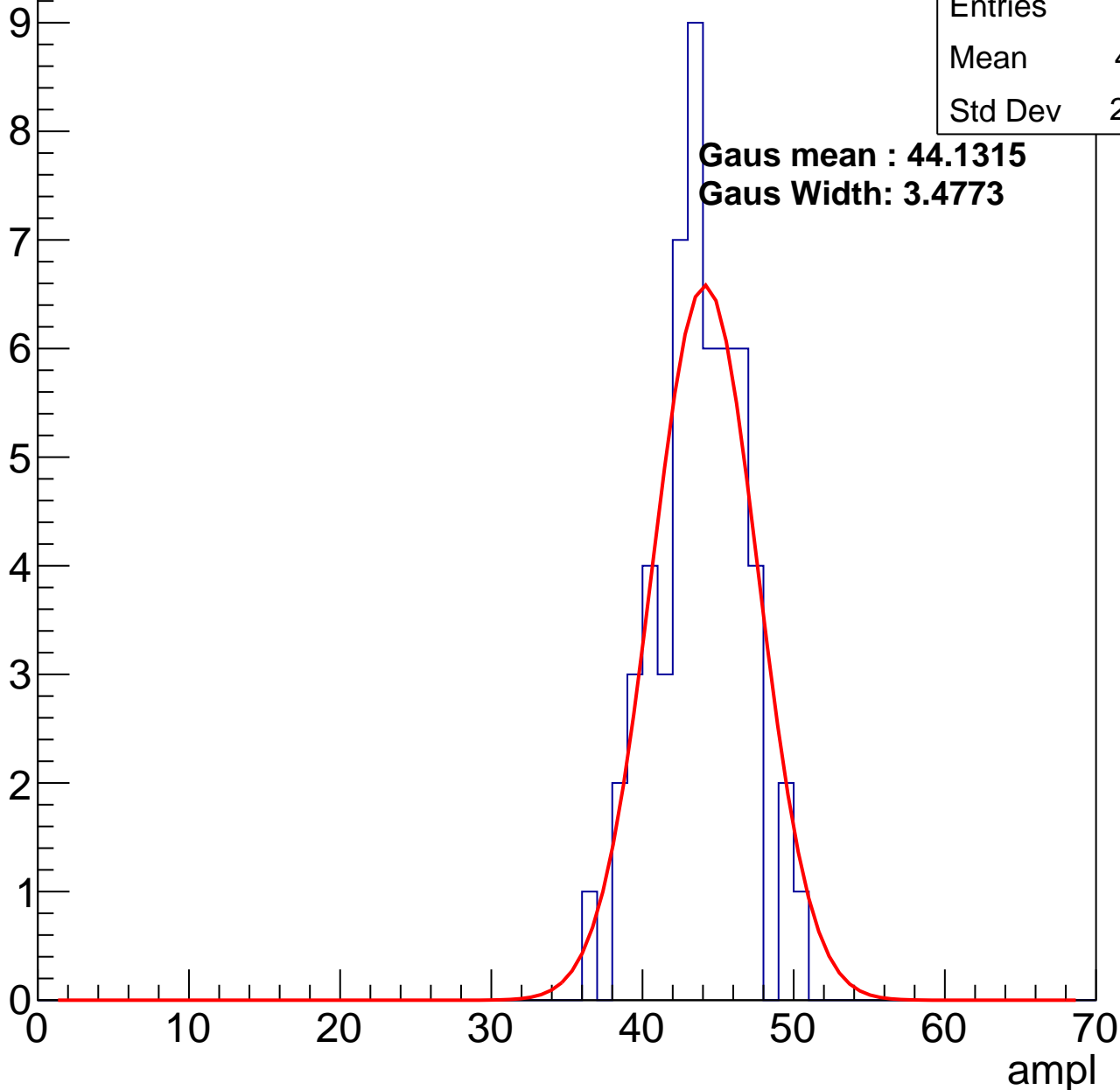
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	43.31
Std Dev	2.937

**Gaus mean : 44.1315**

**Gaus Width: 3.4773**

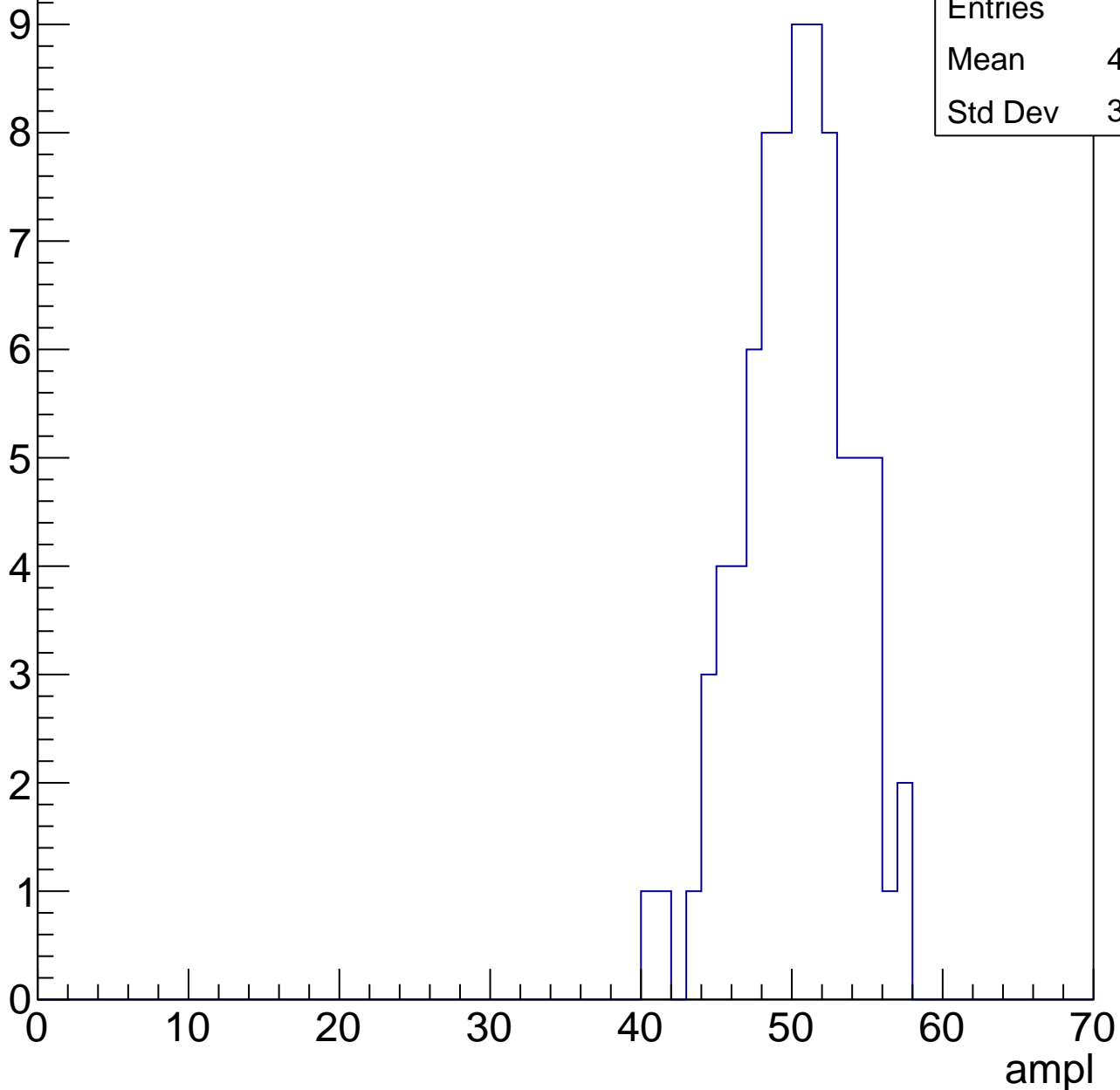


# B0L001S, U6-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	80
Mean	49.79
Std Dev	3.566

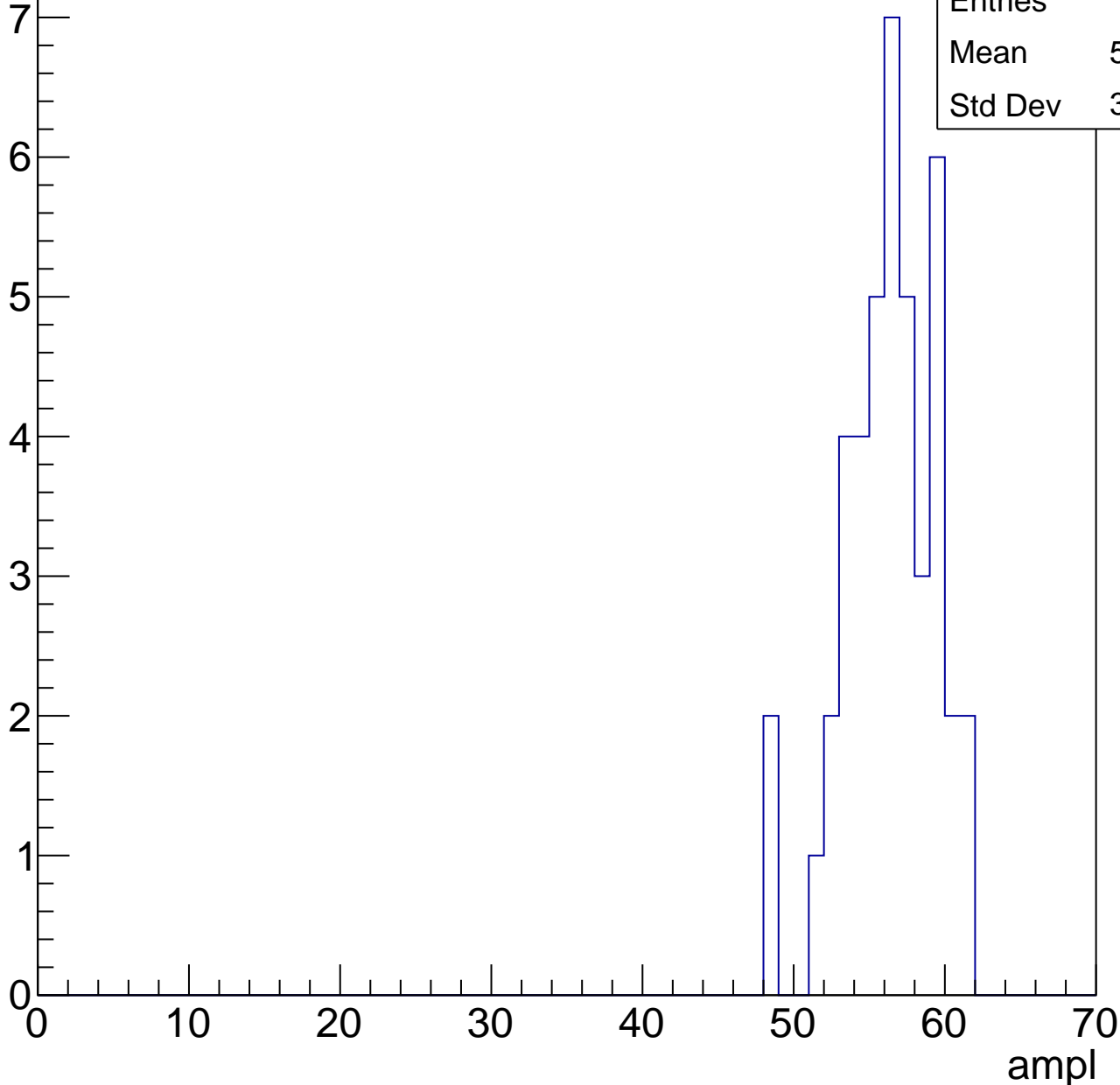


# B0L001S, U6-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	43
Mean	55.84
Std Dev	3.026

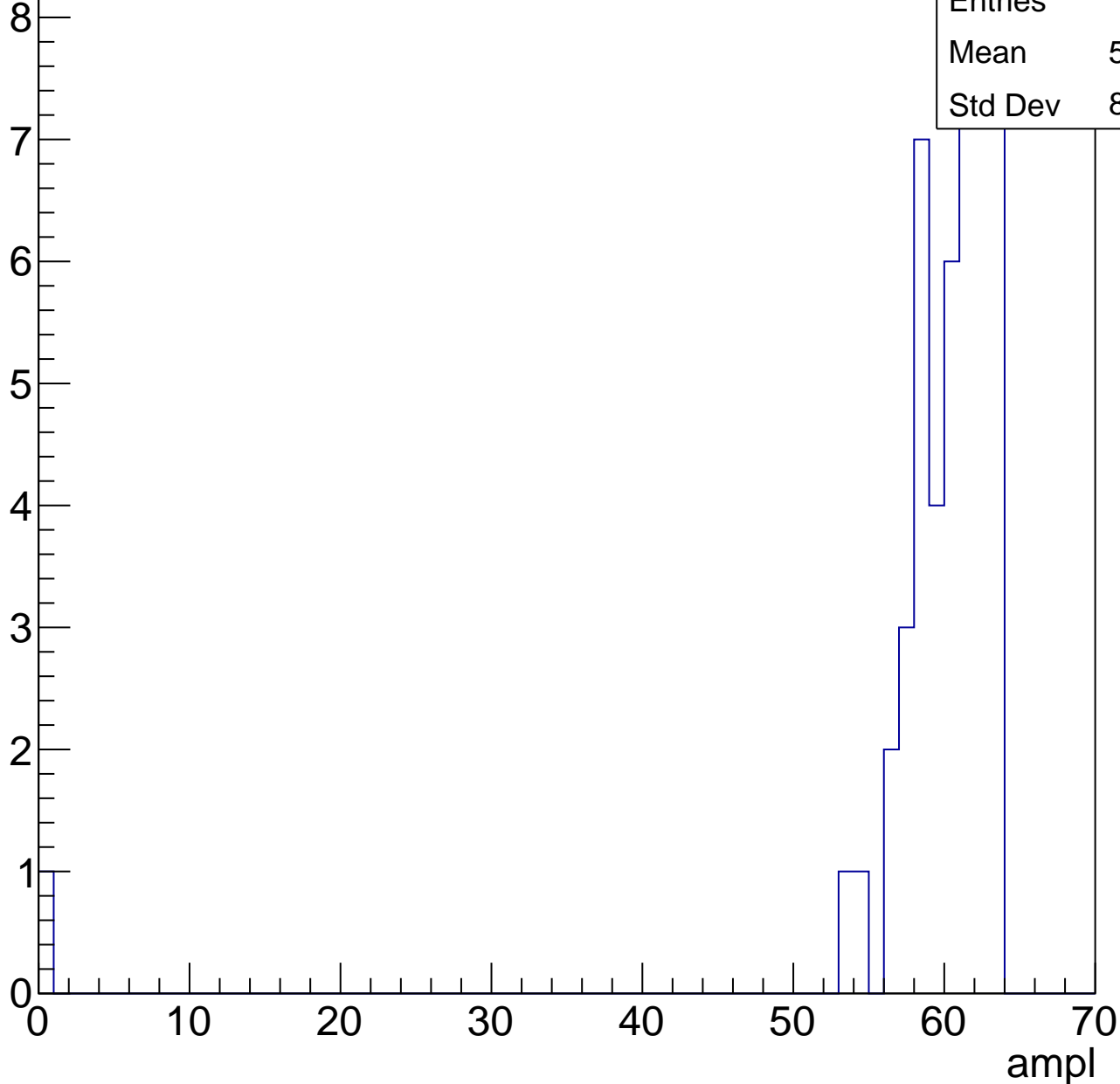


# B0L001S, U6-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	58.78
Std Dev	8.823



# B0L001S, U6-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.67
Std Dev	1.247

ampl

0 10 20 30 40 50 60 70



# B0L001S, U6-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U6-ch113, adc0

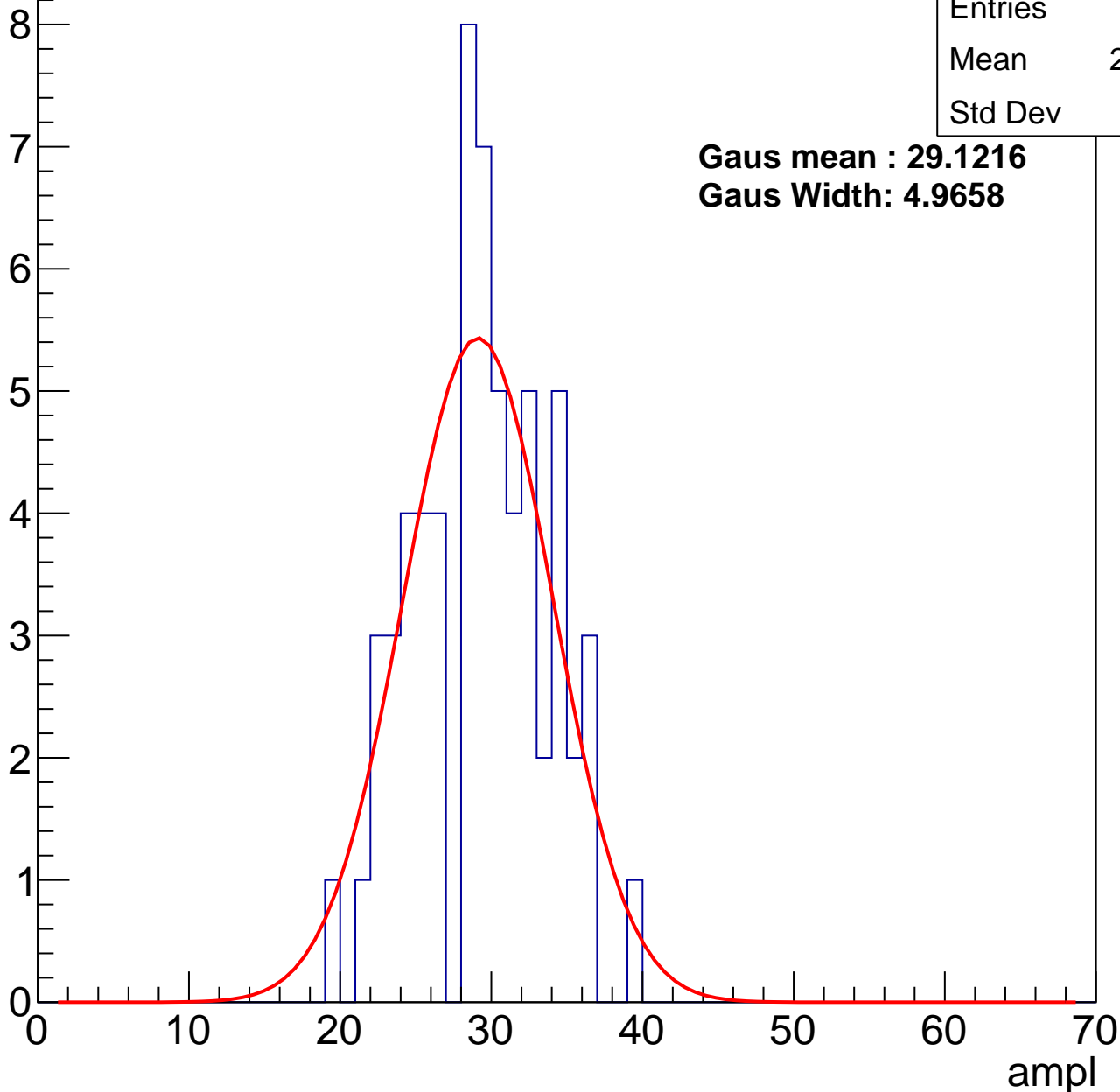
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	28.85
Std Dev	4.34

**Gaus mean : 29.1216**

**Gaus Width: 4.9658**



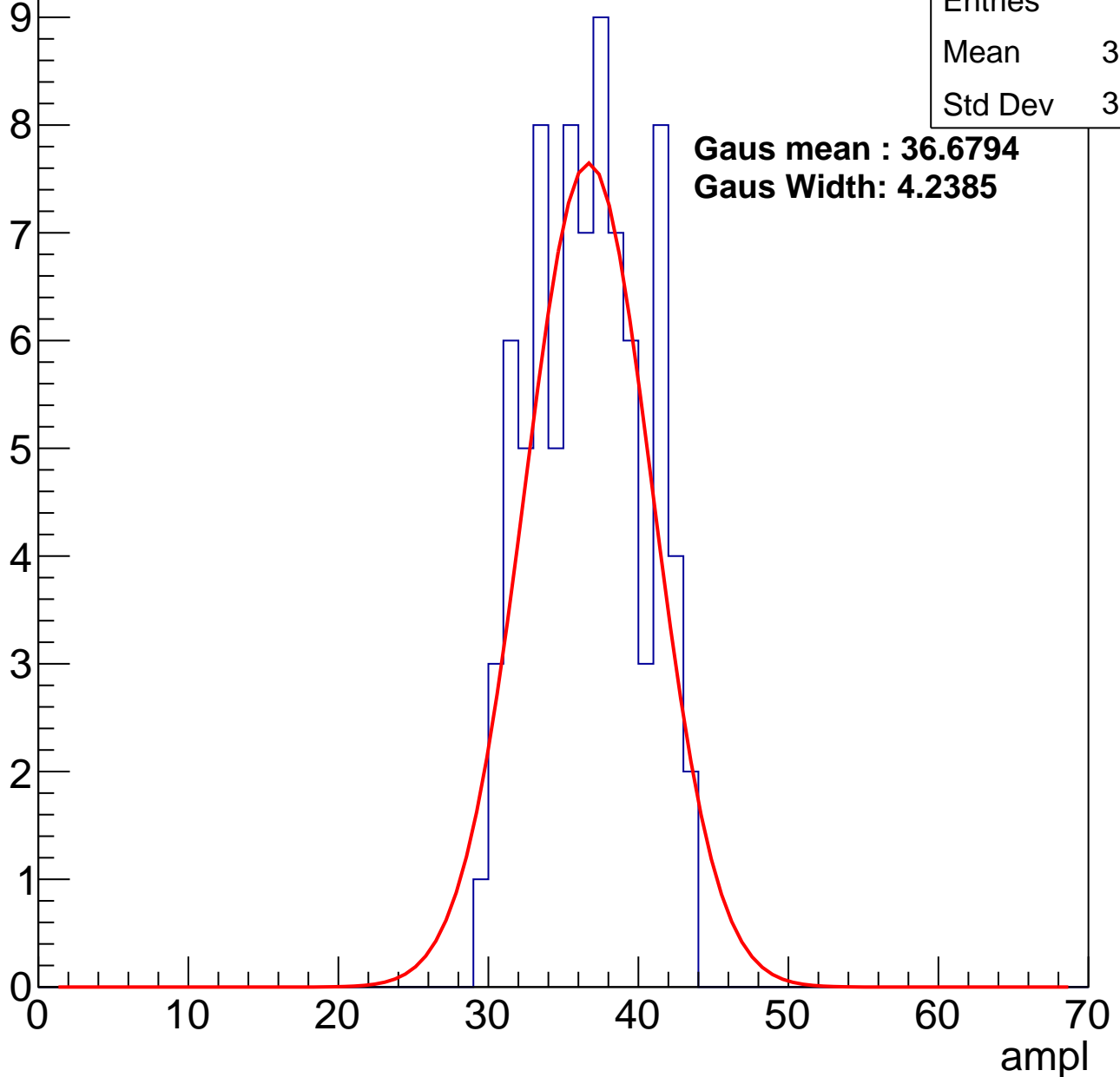
# B0L001S, U6-ch113, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	82
Mean	36.17
Std Dev	3.605

**Gaus mean : 36.6794**  
**Gaus Width: 4.2385**



# B0L001S, U6-ch113, adc2

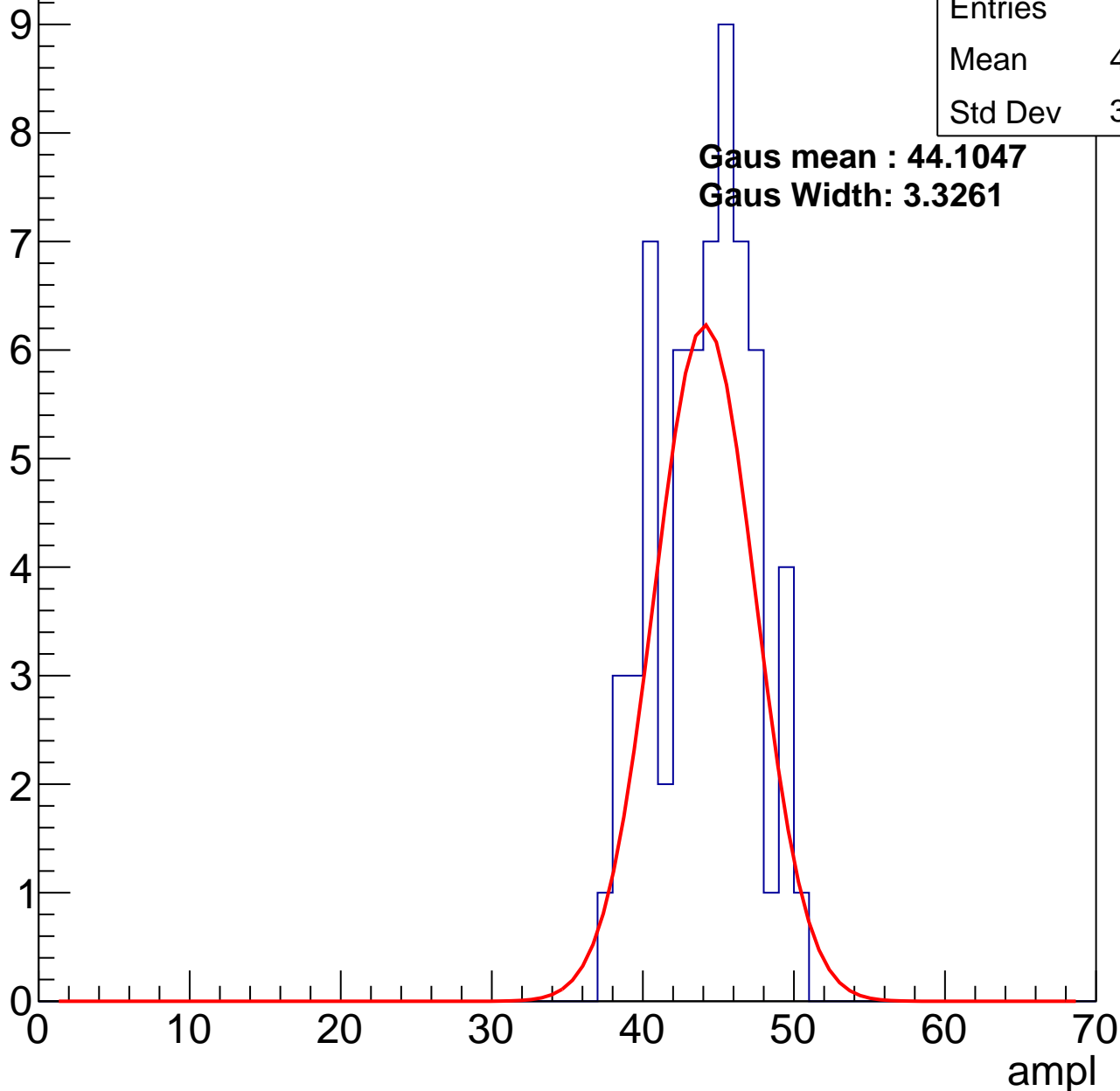
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	43.67
Std Dev	3.157

**Gaus mean : 44.1047**

**Gaus Width: 3.3261**



# B0L001S, U6-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

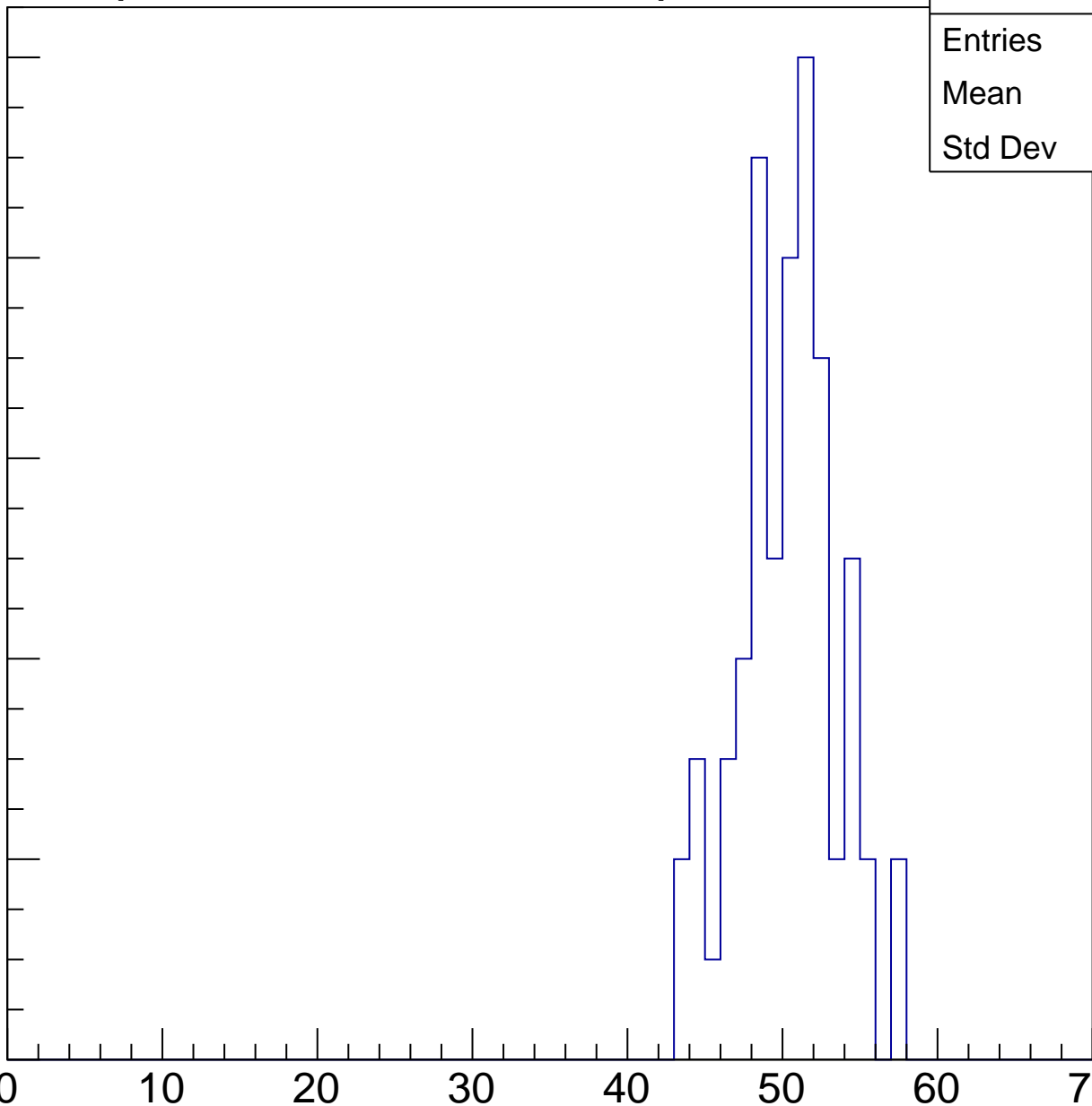
Entries	63
Mean	49.84
Std Dev	3.183

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

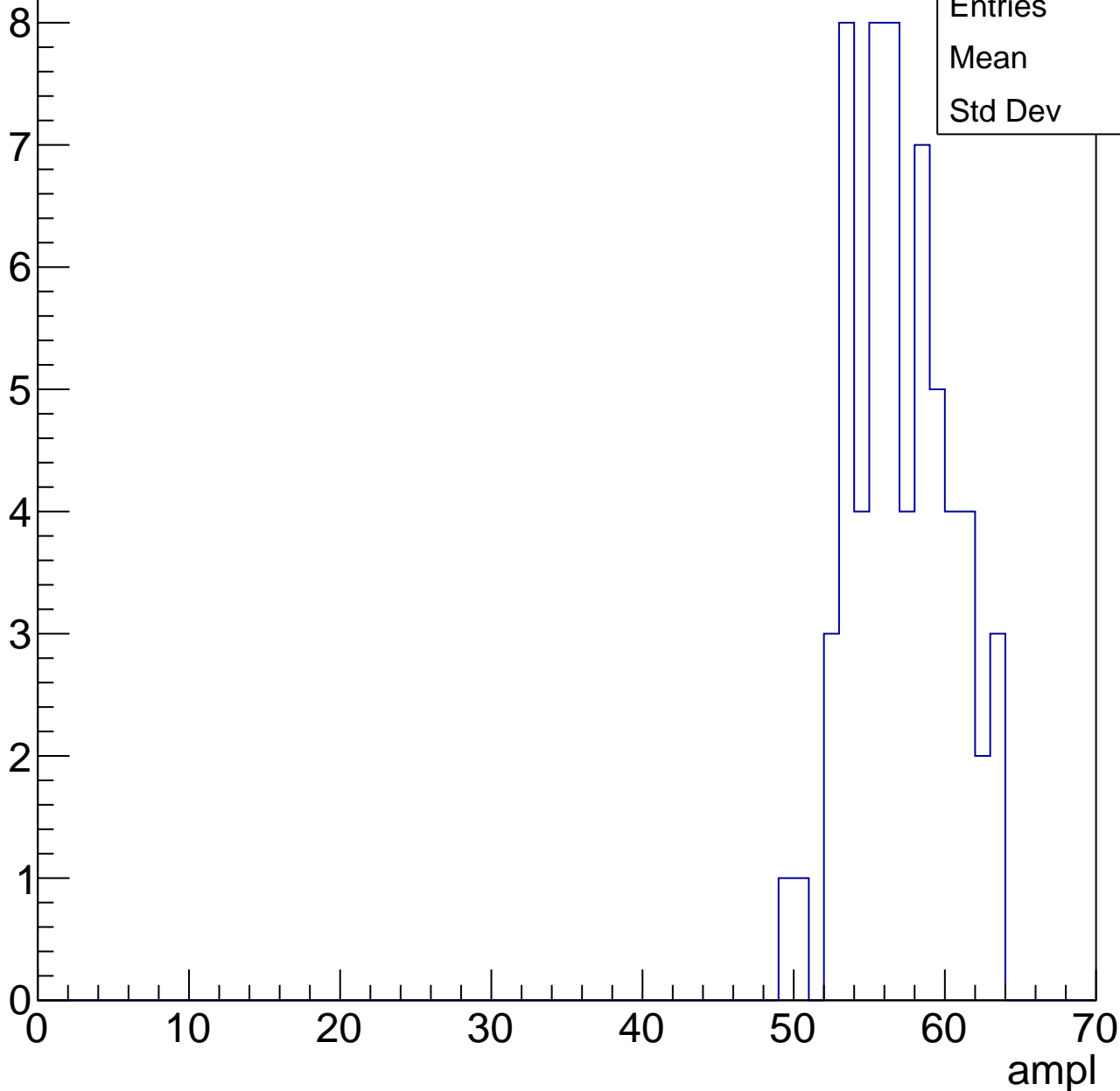


# B0L001S, U6-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	56.6
Std Dev	3.28

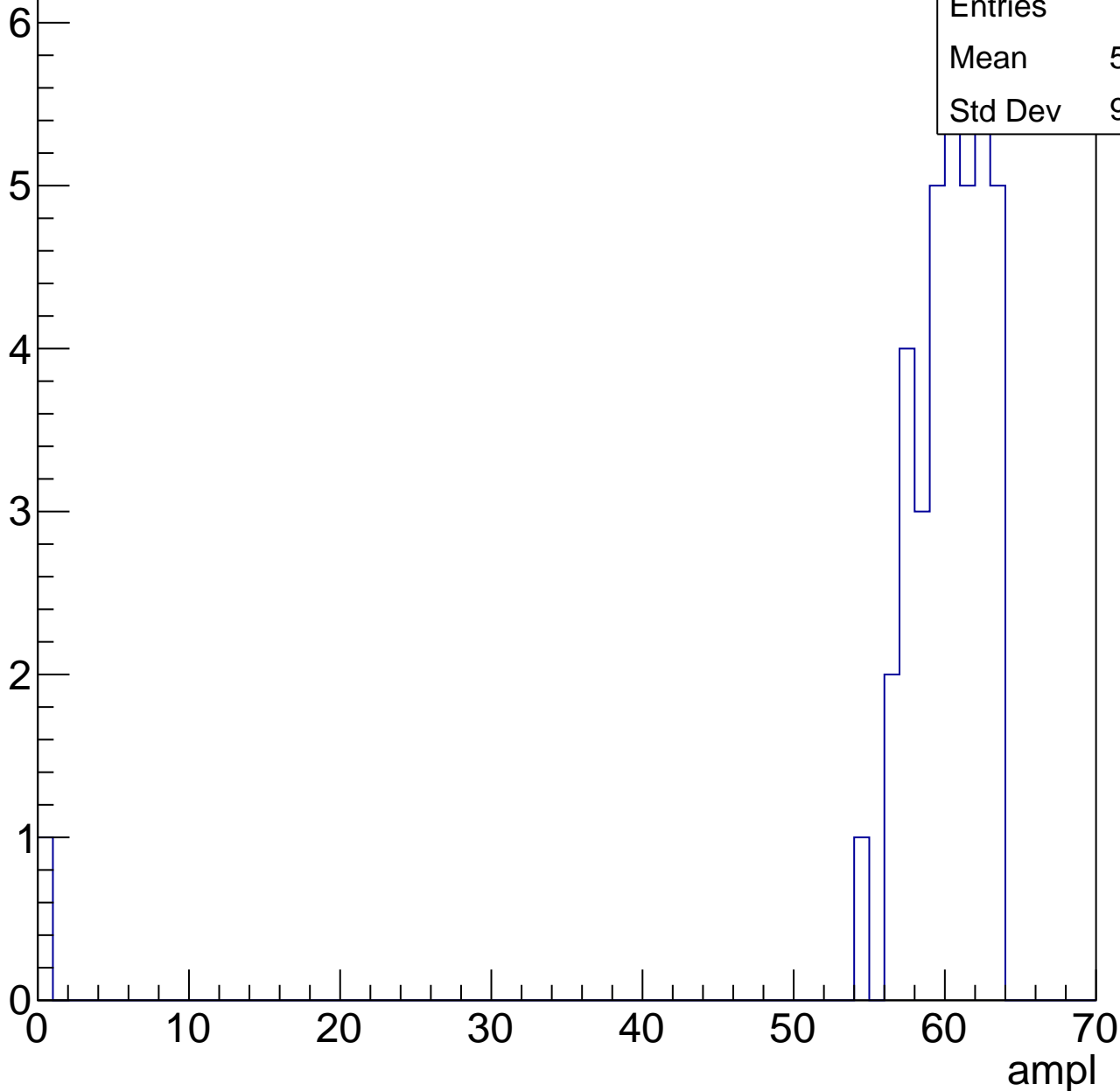


# B0L001S, U6-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	38
Mean	58.29
Std Dev	9.846



# B0L001S, U6-ch113, adc6

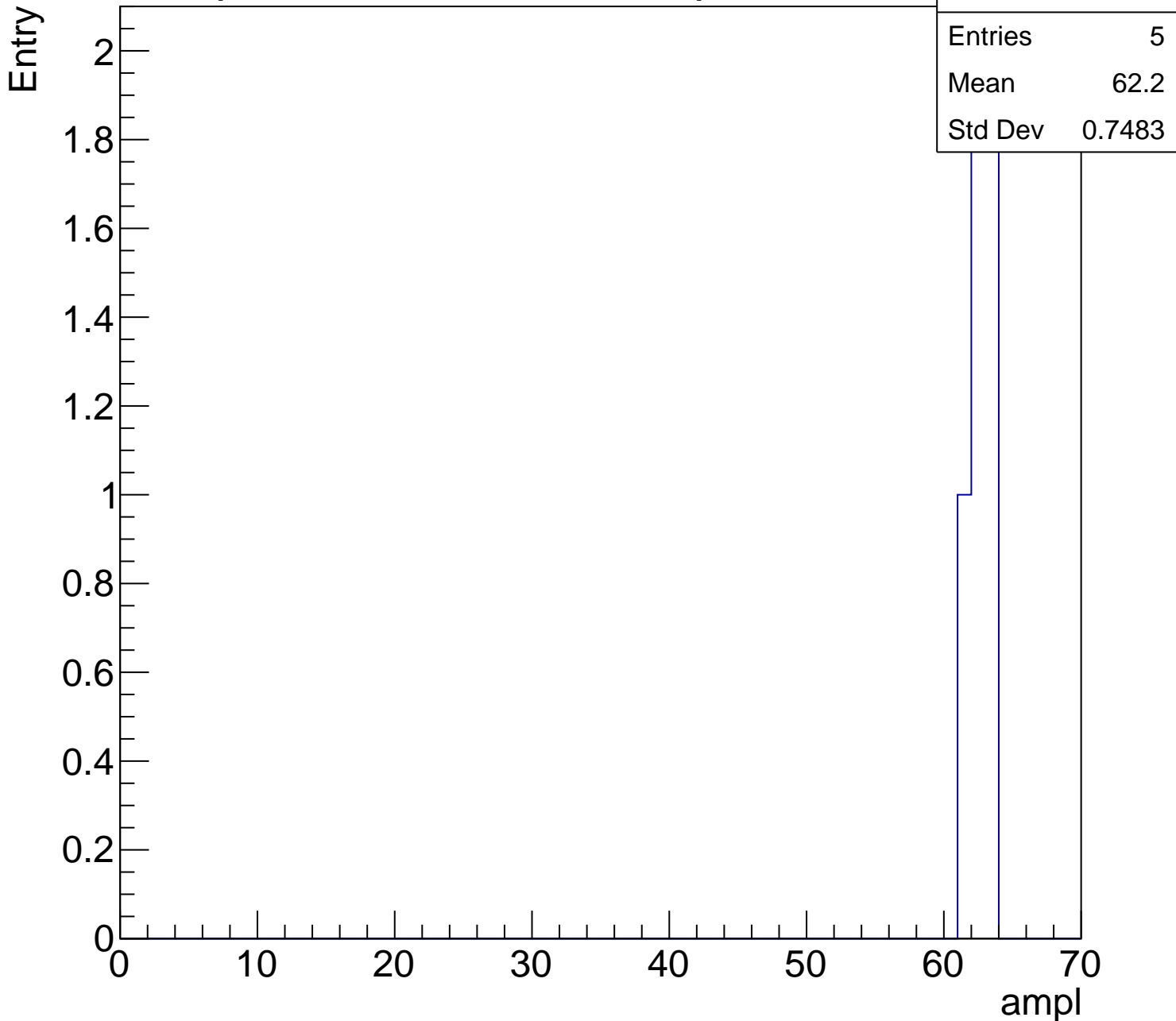
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	62.2
Std Dev	0.7483

ampl





# B0L001S, U6-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U6-ch114, adc0

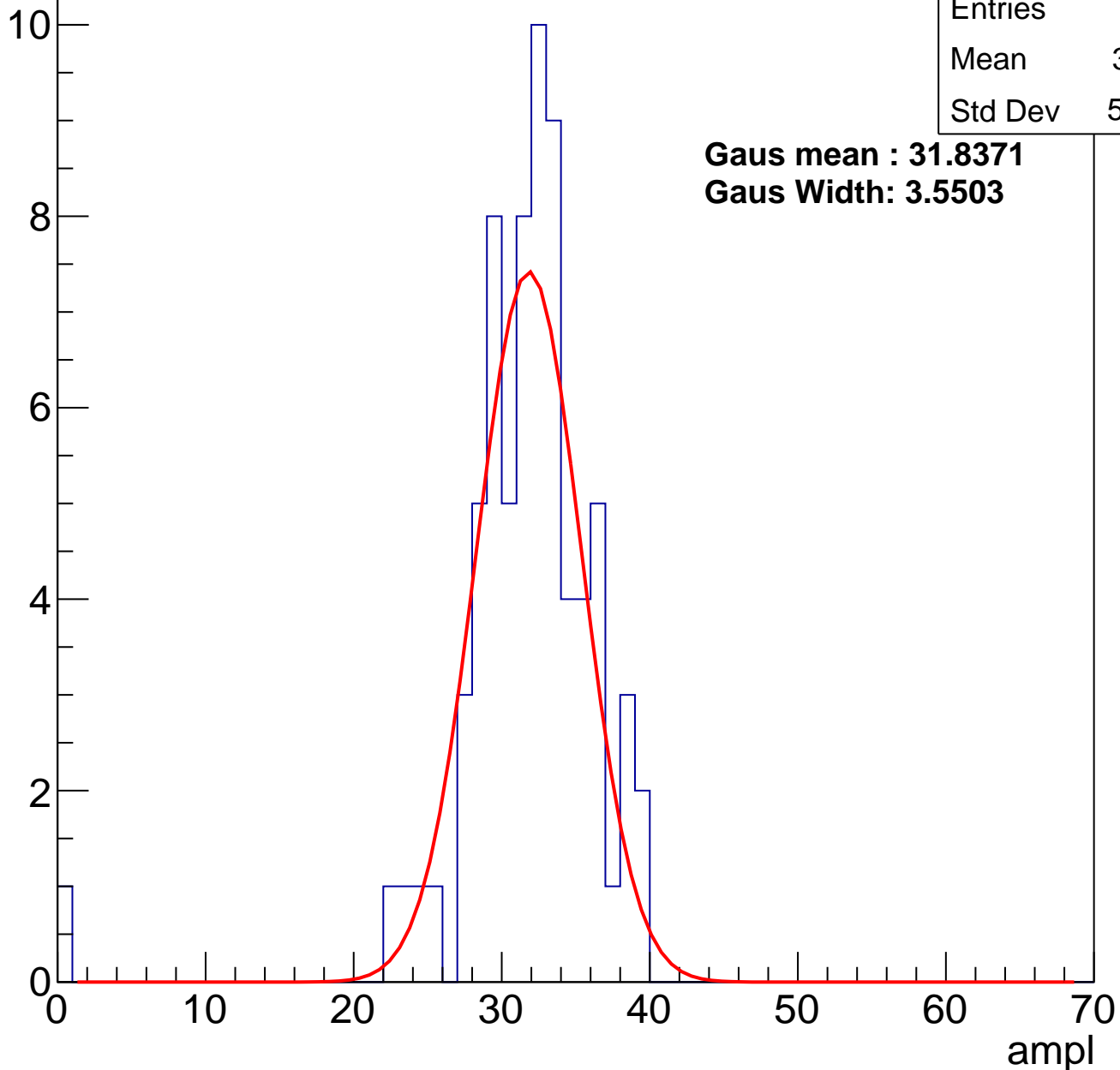
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	72
Mean	31.21
Std Dev	5.137

**Gaus mean : 31.8371**

**Gaus Width: 3.5503**

Entry



# B0L001S, U6-ch114, adc1

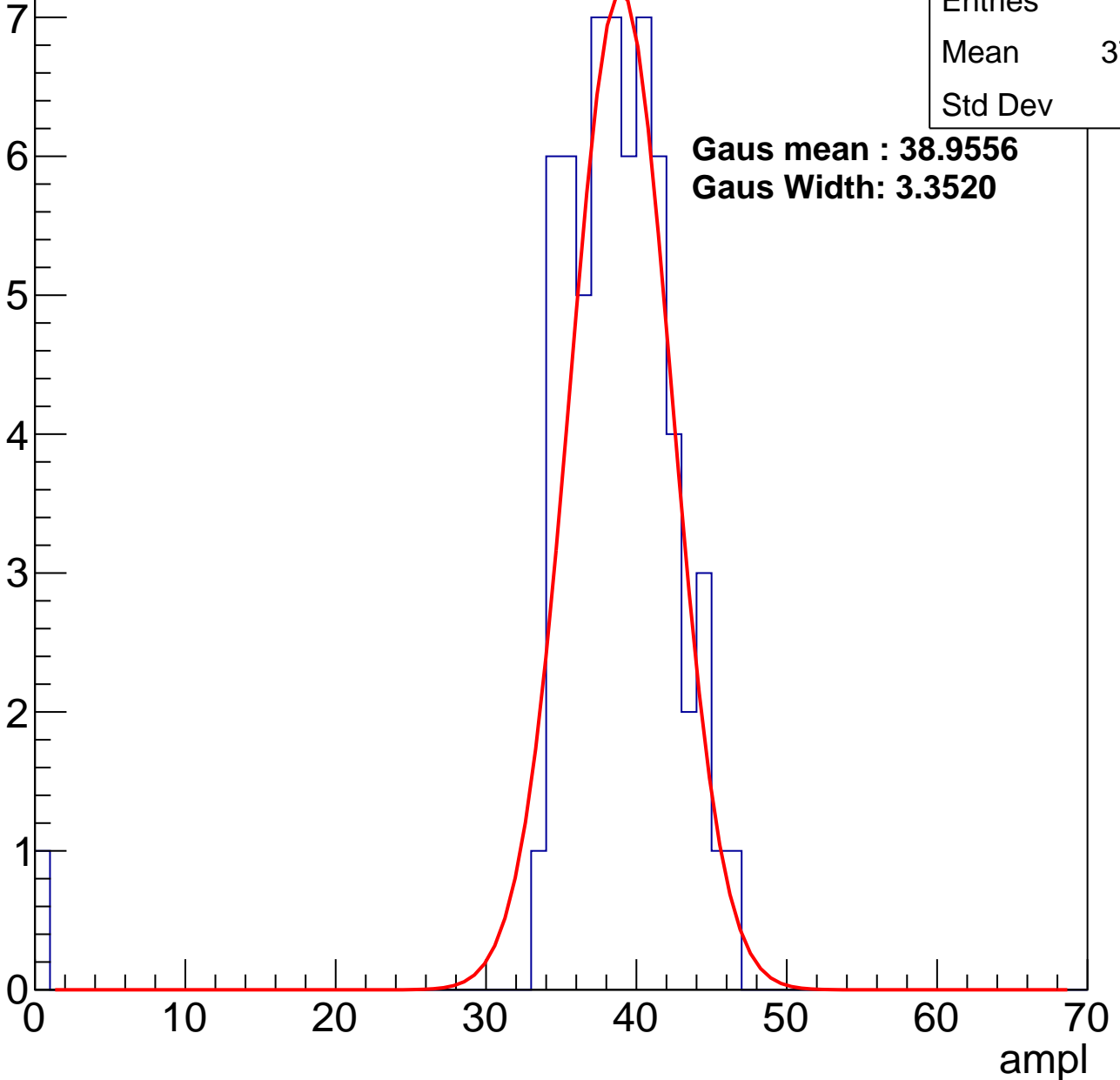
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	37.92
Std Dev	5.73

**Gaus mean : 38.9556**

**Gaus Width: 3.3520**



# B0L001S, U6-ch114, adc2

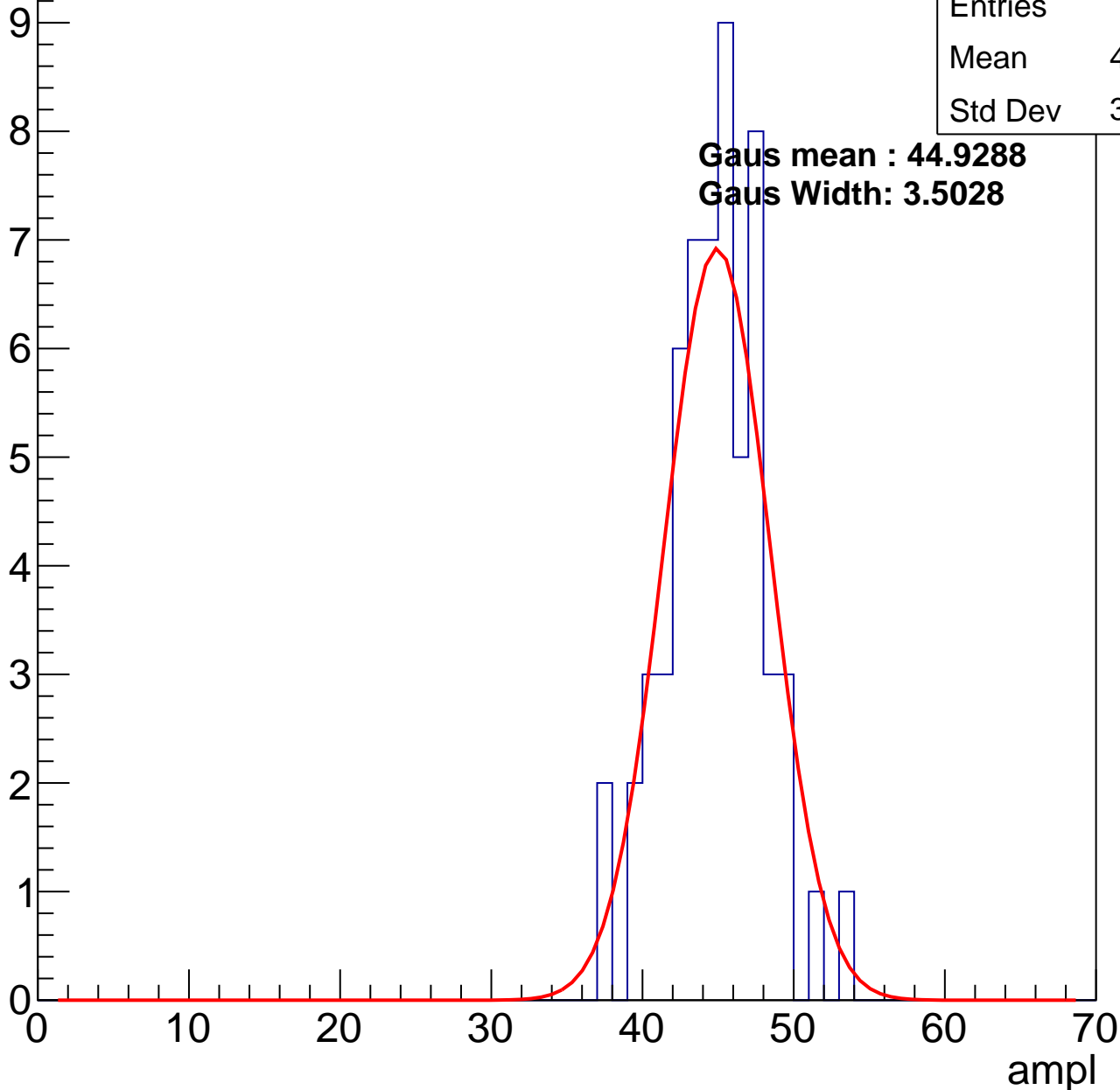
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	44.37
Std Dev	3.162

**Gaus mean : 44.9288**

**Gaus Width: 3.5028**

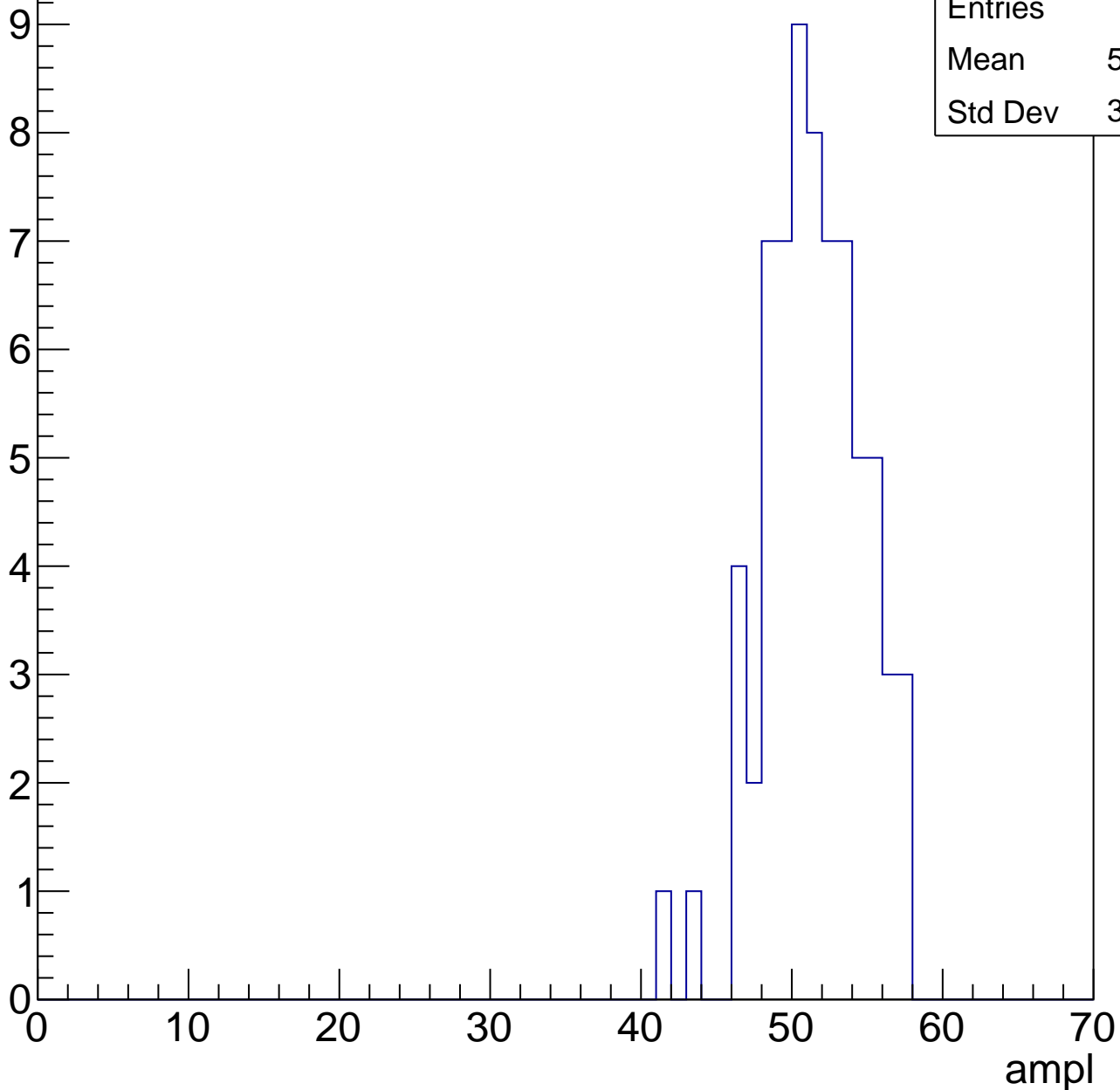


# B0L001S, U6-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

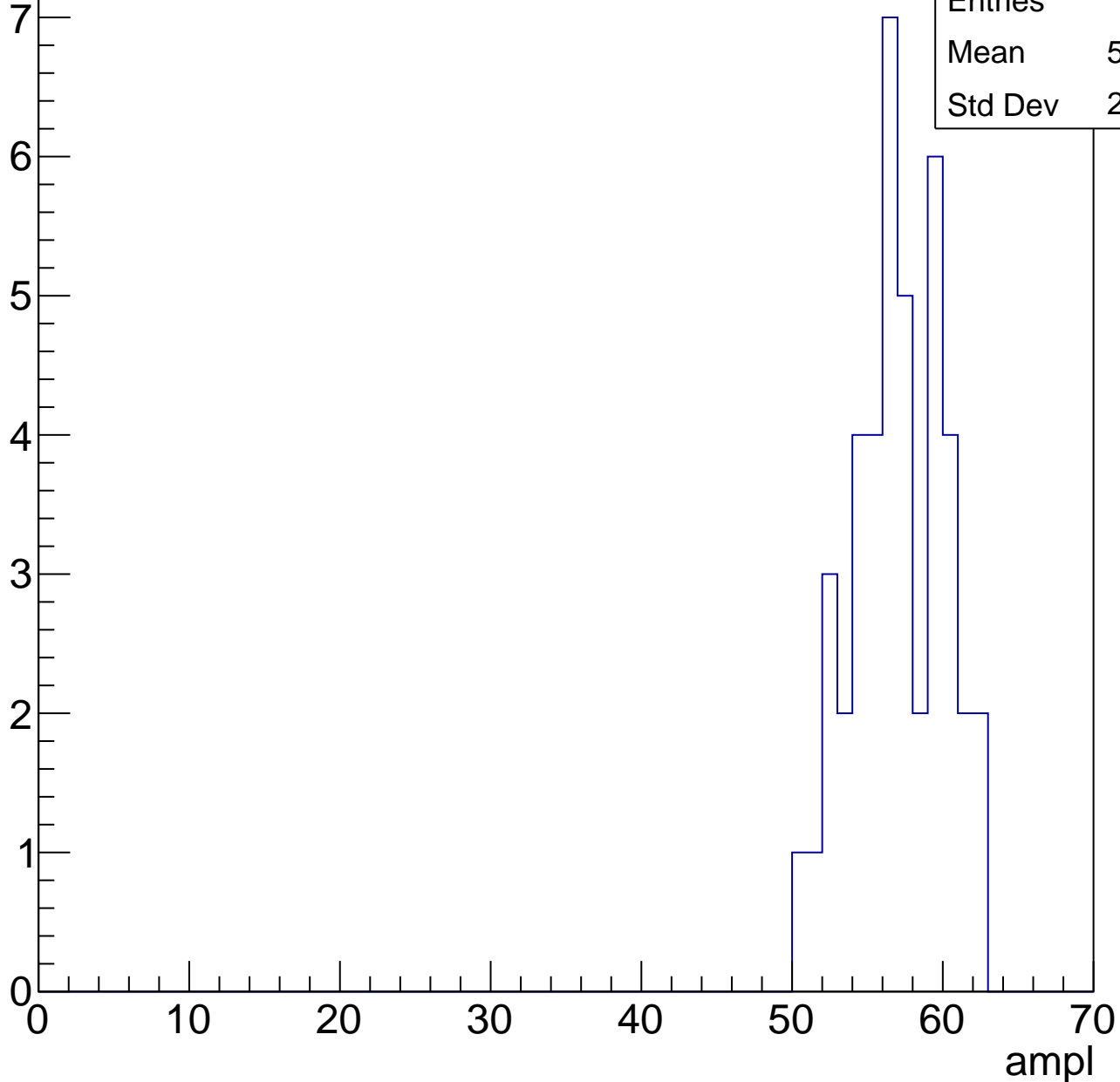
Entries	69
Mean	50.99
Std Dev	3.273



# B0L001S, U6-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

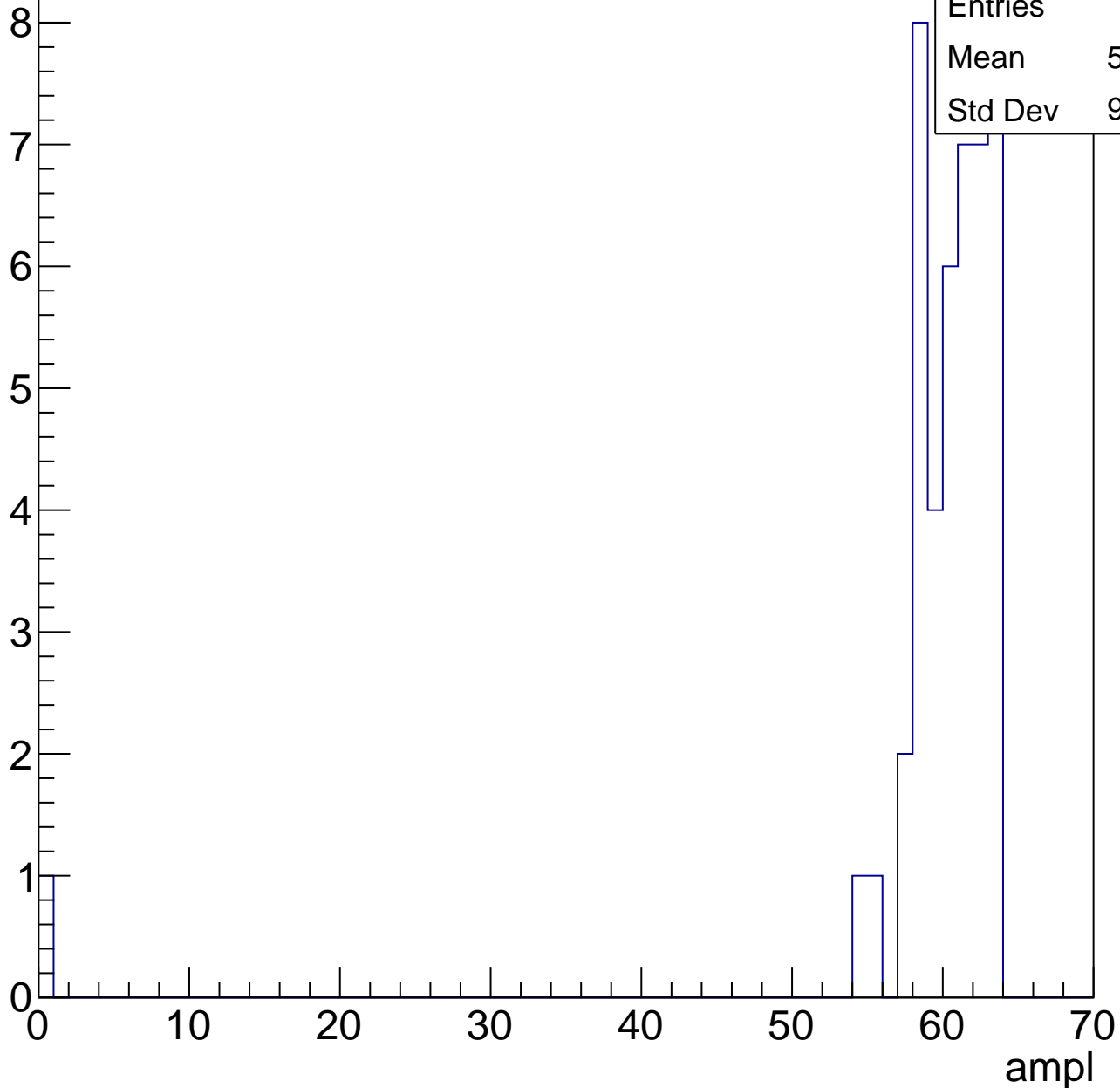
Entry



# B0L001S, U6-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U6-ch115, adc0

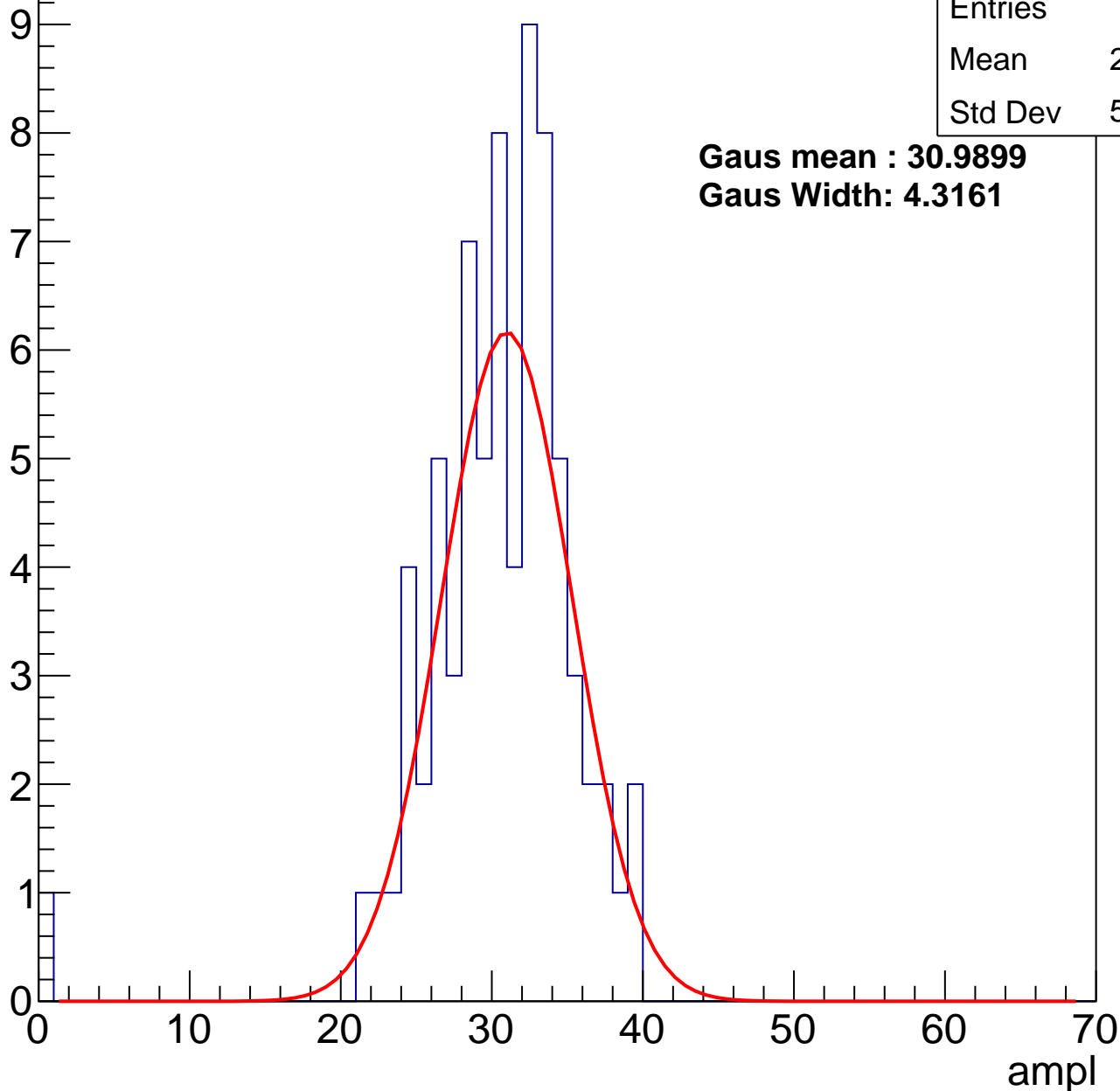
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	29.96
Std Dev	5.316

**Gaus mean : 30.9899**

**Gaus Width: 4.3161**



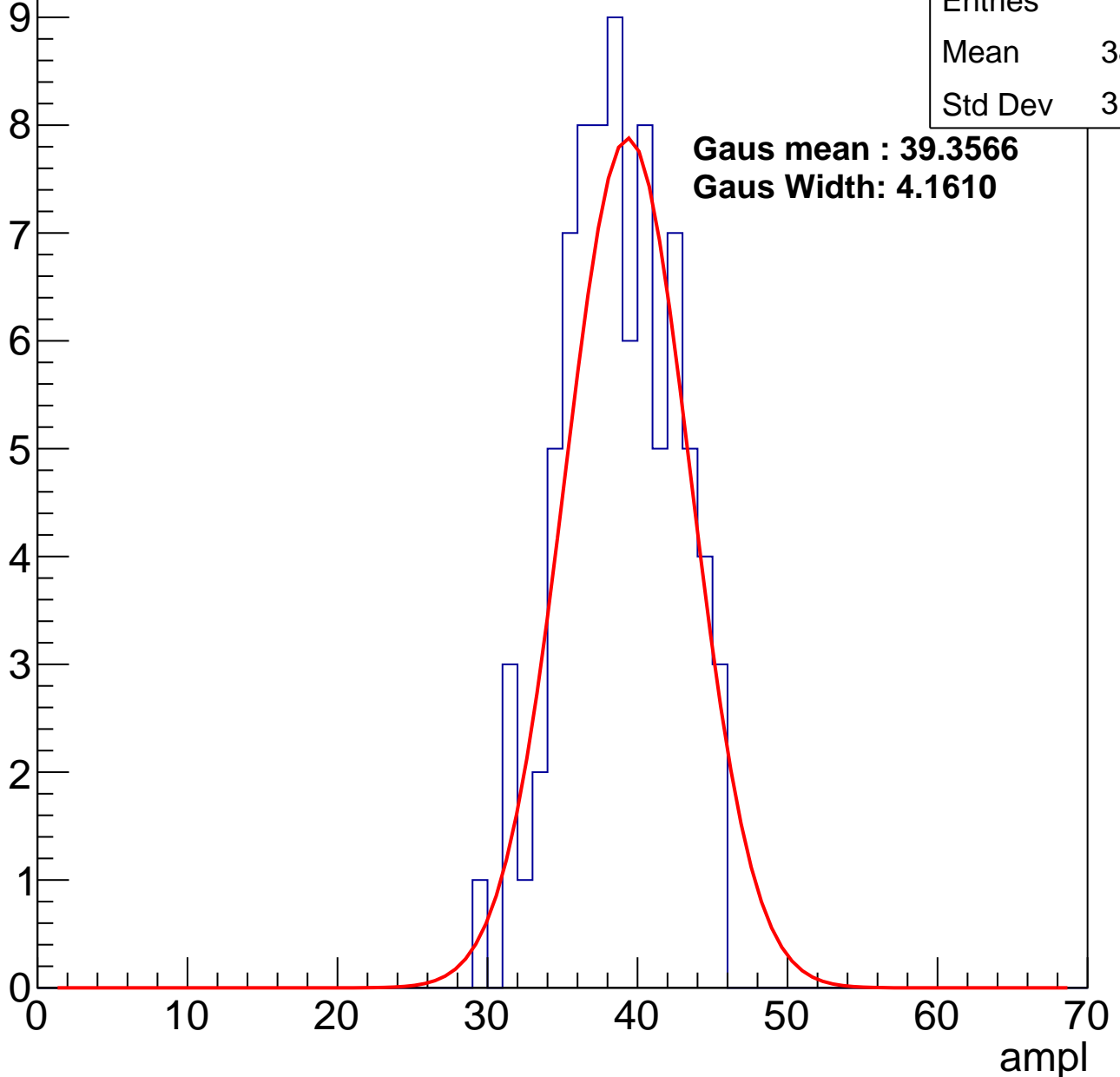
# B0L001S, U6-ch115, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	82
Mean	38.29
Std Dev	3.664

**Gaus mean : 39.3566**  
**Gaus Width: 4.1610**



# B0L001S, U6-ch115, adc2

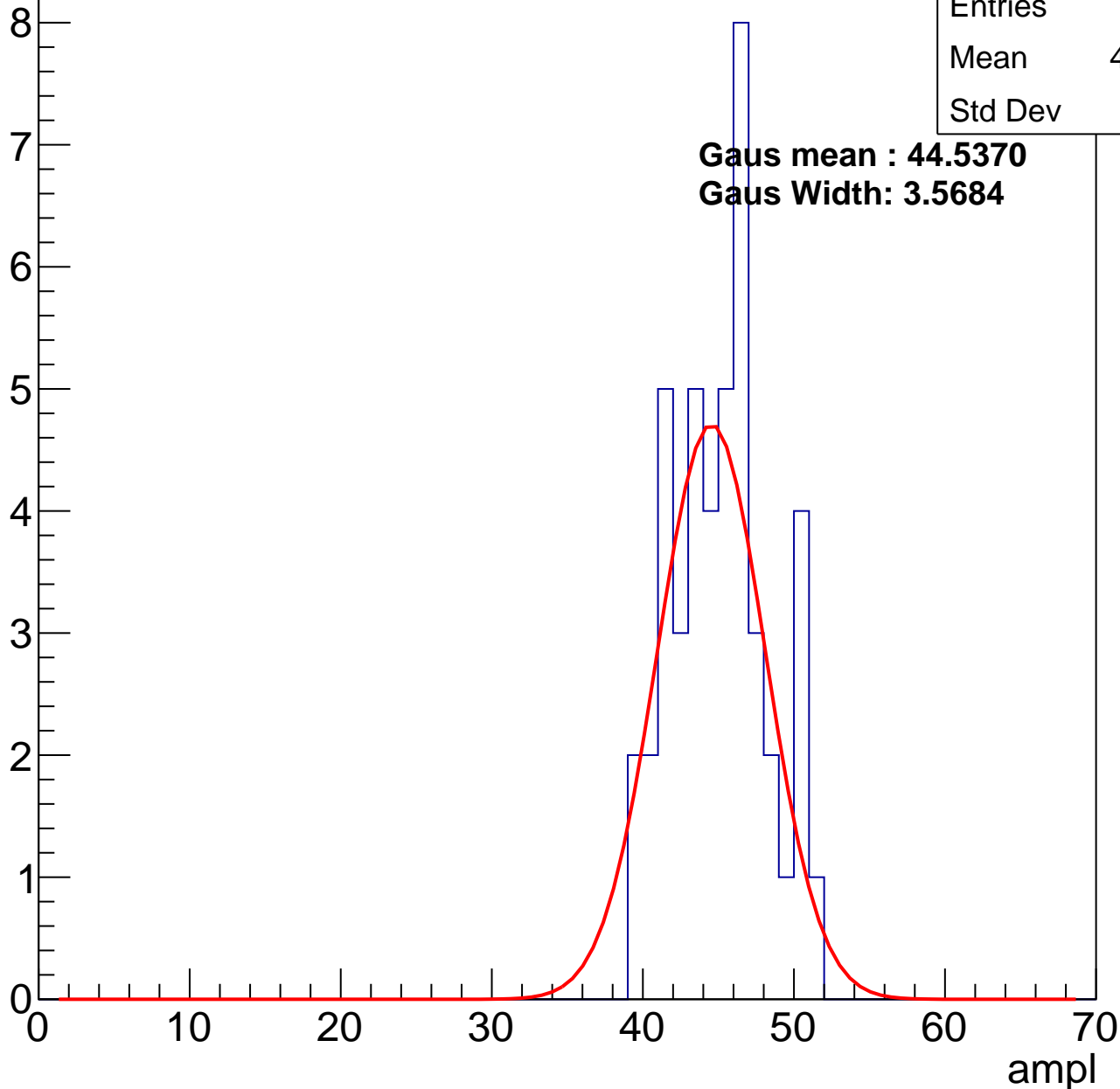
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	45
Mean	44.67
Std Dev	3.12

**Gaus mean : 44.5370**

**Gaus Width: 3.5684**

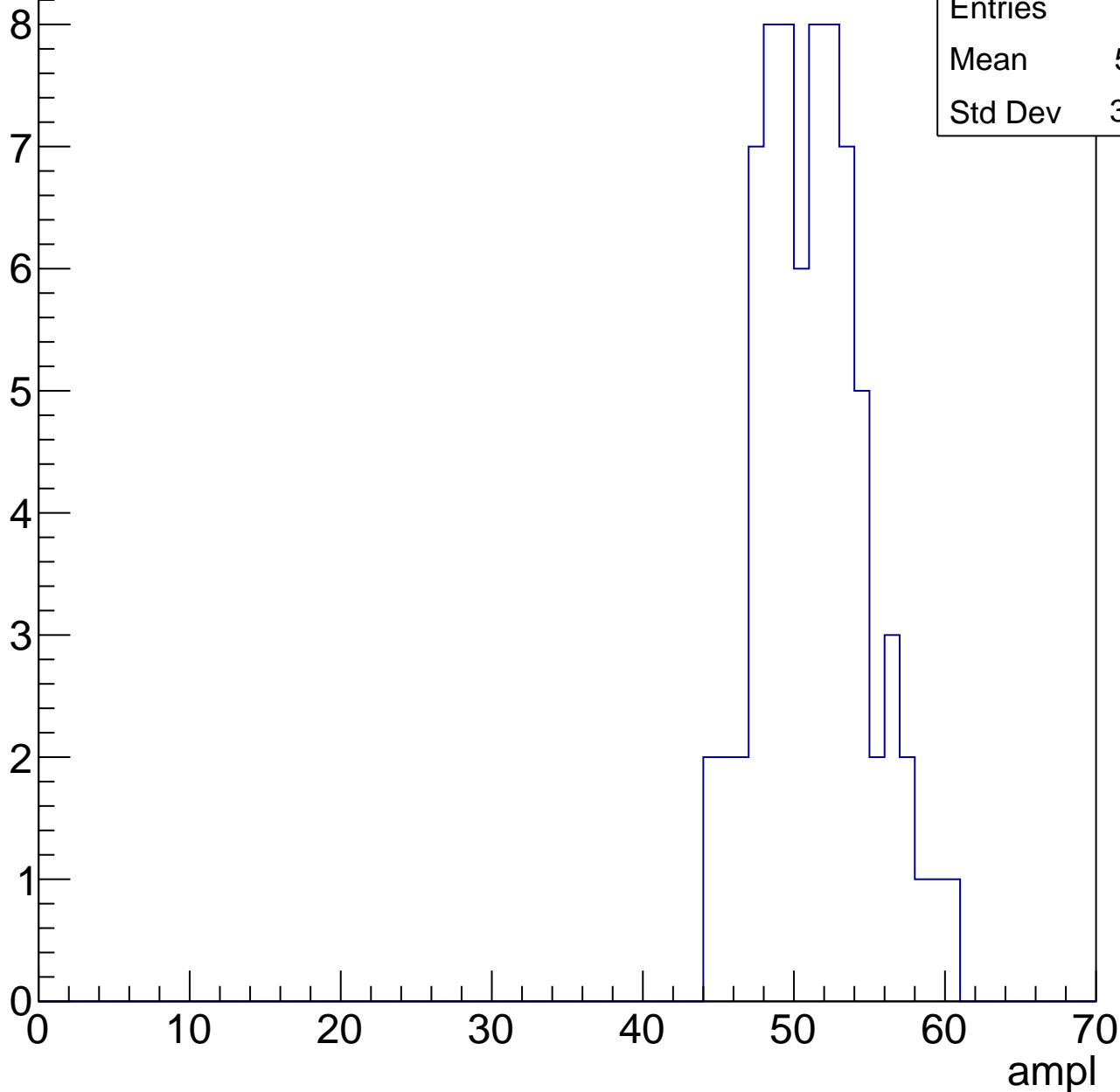


# B0L001S, U6-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	50.81
Std Dev	3.498

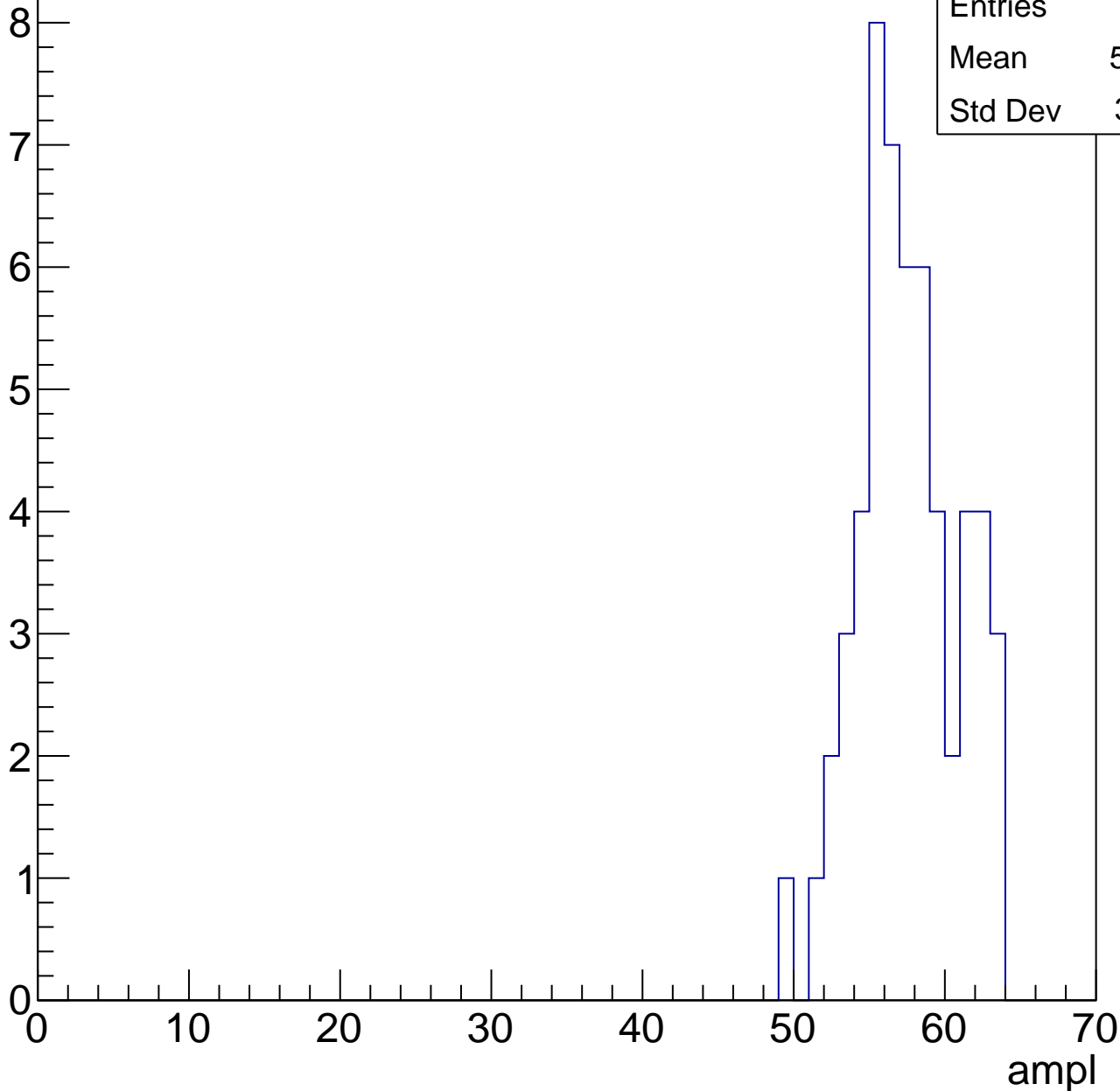


# B0L001S, U6-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	57.05
Std Dev	3.261





# B0L001S, U6-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch116, adc0

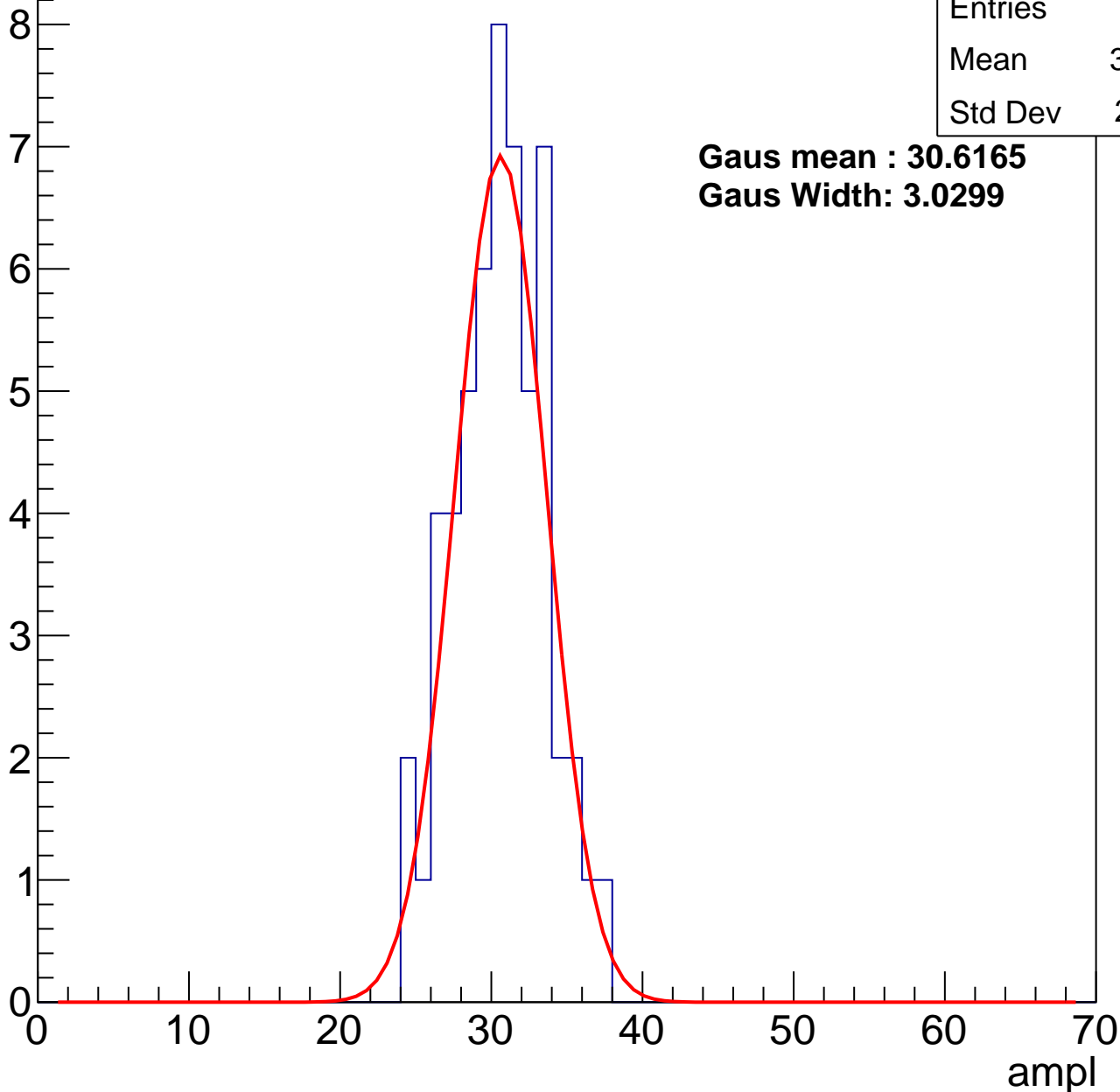
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	30.15
Std Dev	2.951

**Gaus mean : 30.6165**

**Gaus Width: 3.0299**



# B0L001S, U6-ch116, adc1

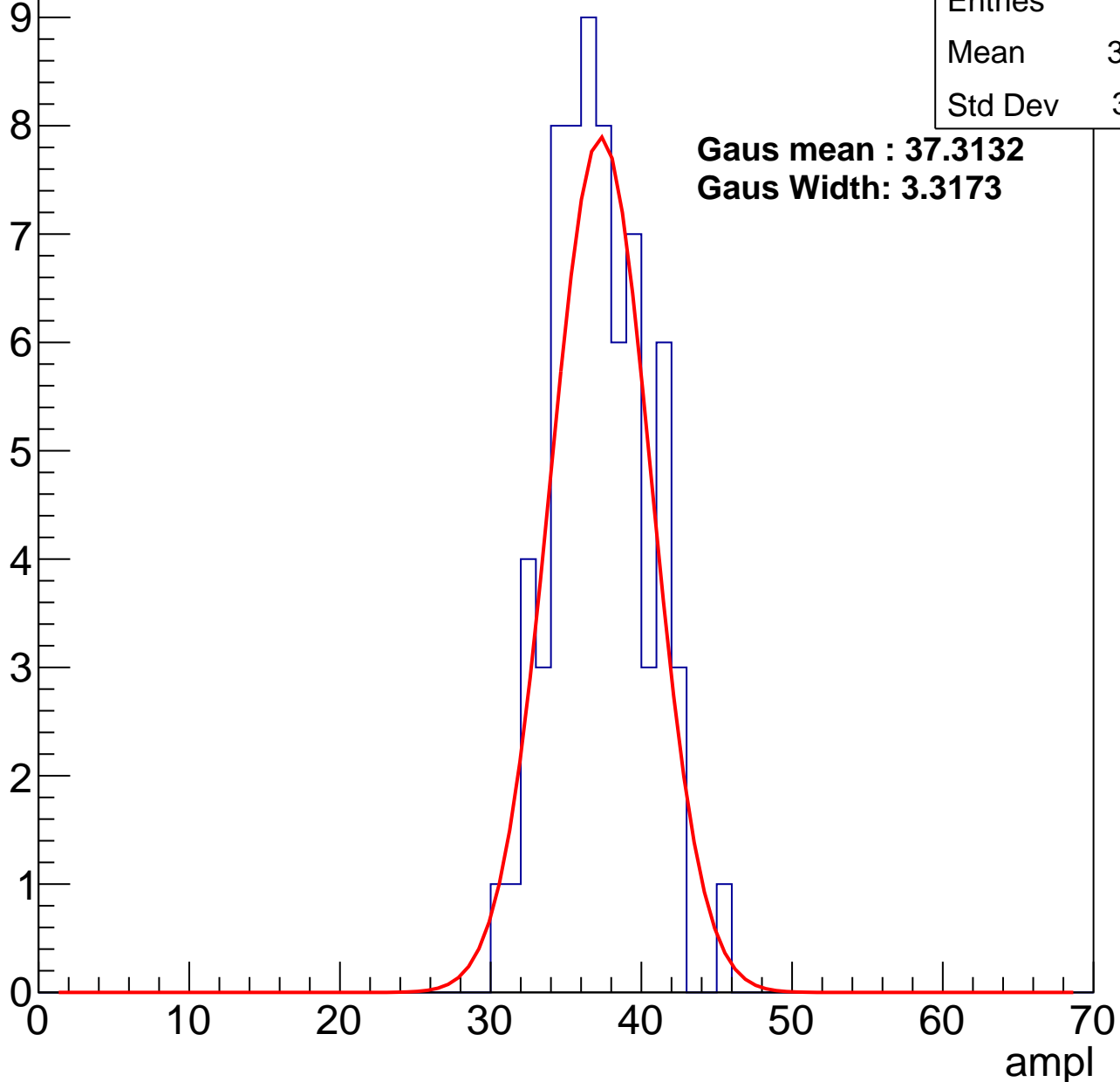
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	36.74
Std Dev	3.061

**Gaus mean : 37.3132**

**Gaus Width: 3.3173**



# B0L001S, U6-ch116, adc2

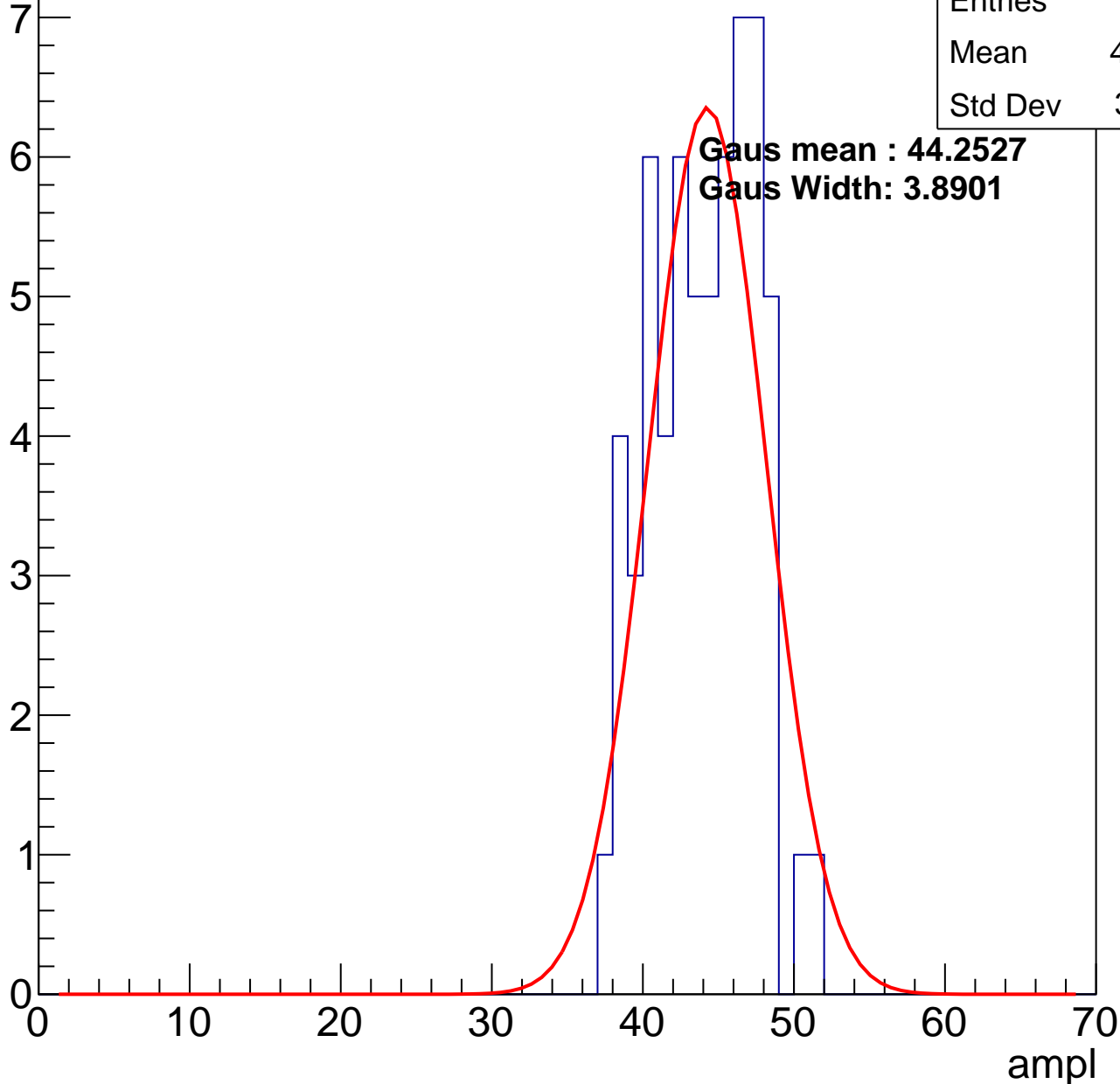
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	43.59
Std Dev	3.341

**Gaus mean : 44.2527**

**Gaus Width: 3.8901**

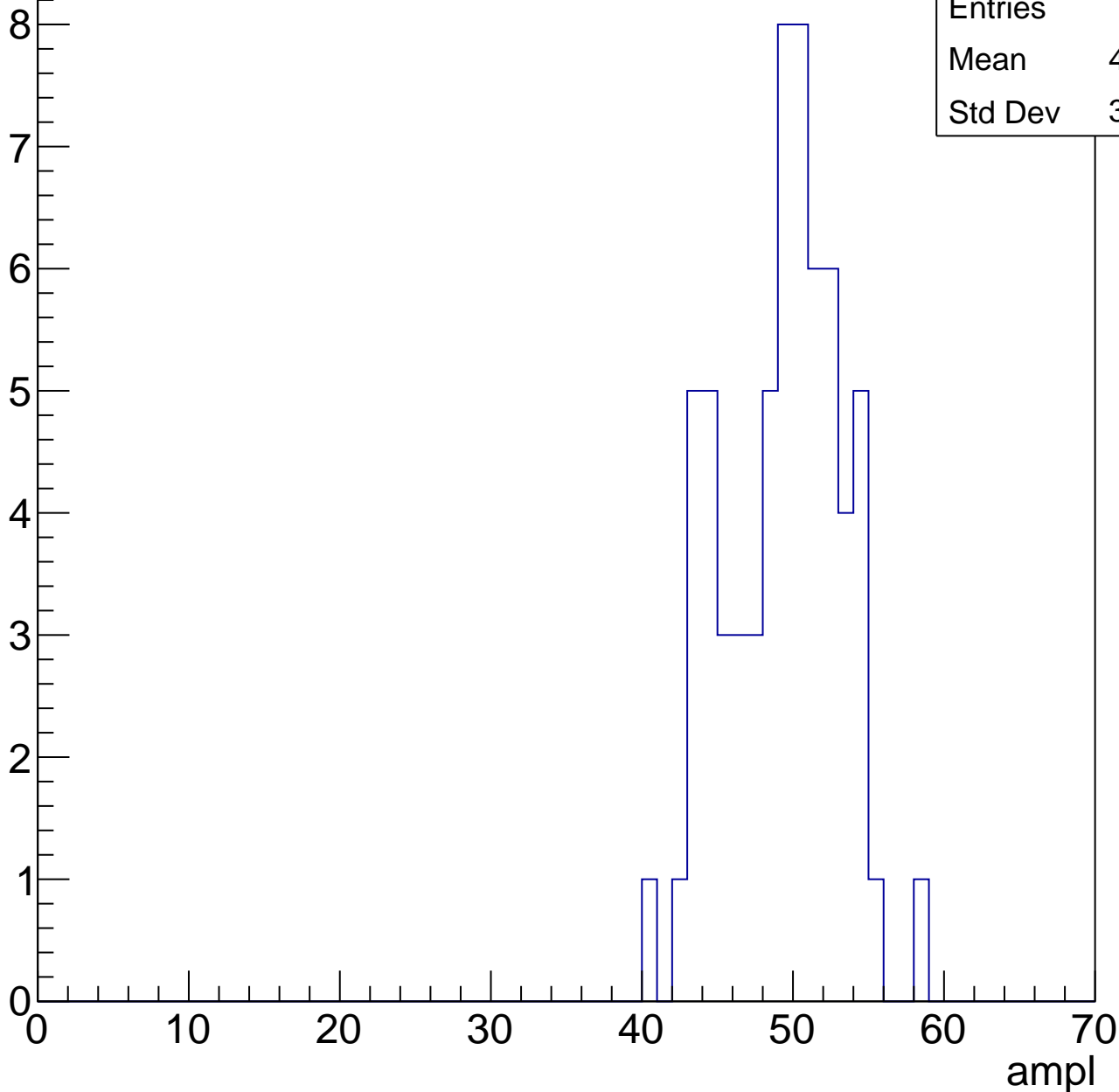


# B0L001S, U6-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	48.86
Std Dev	3.758

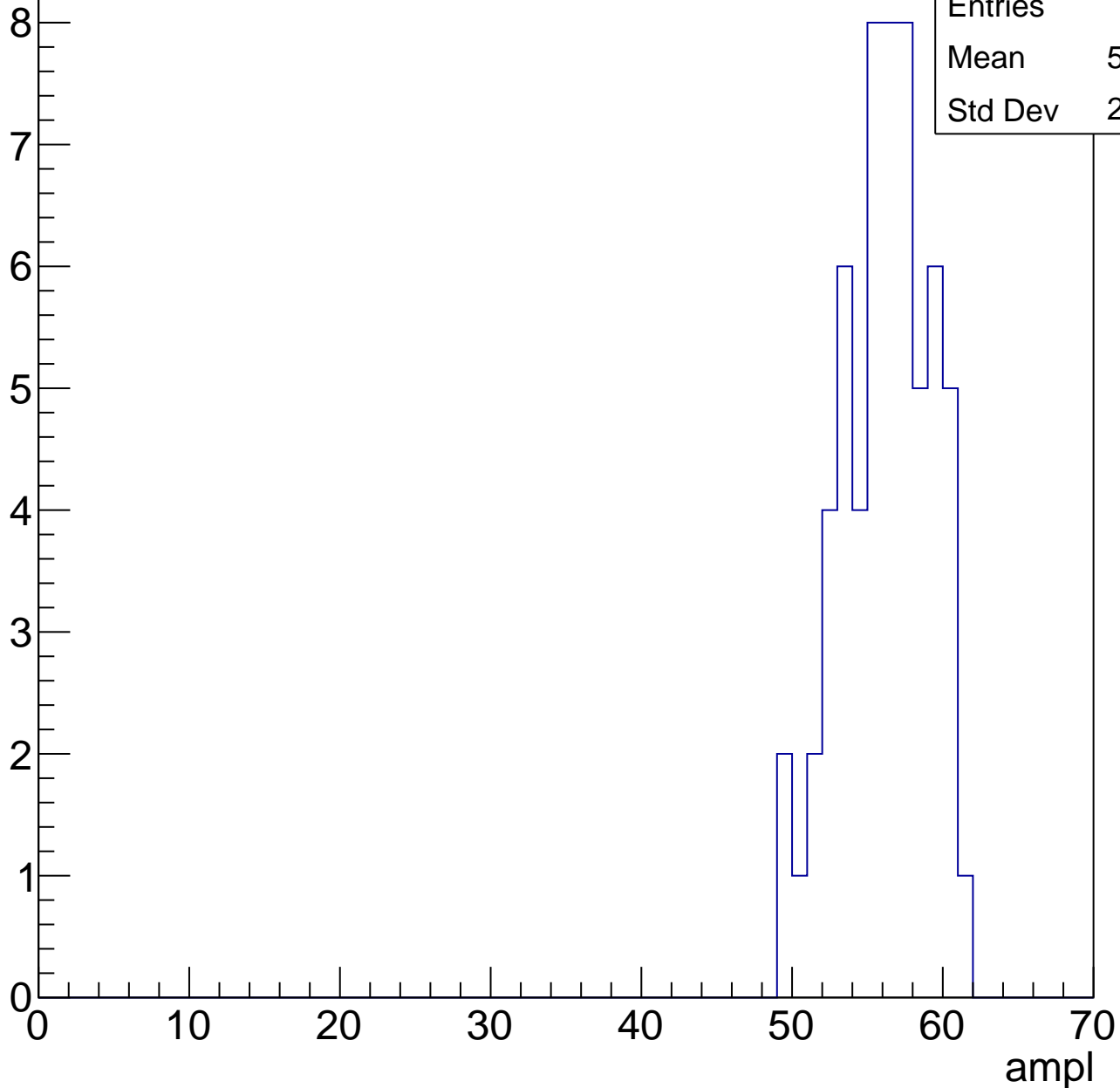


# B0L001S, U6-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	55.68
Std Dev	2.907

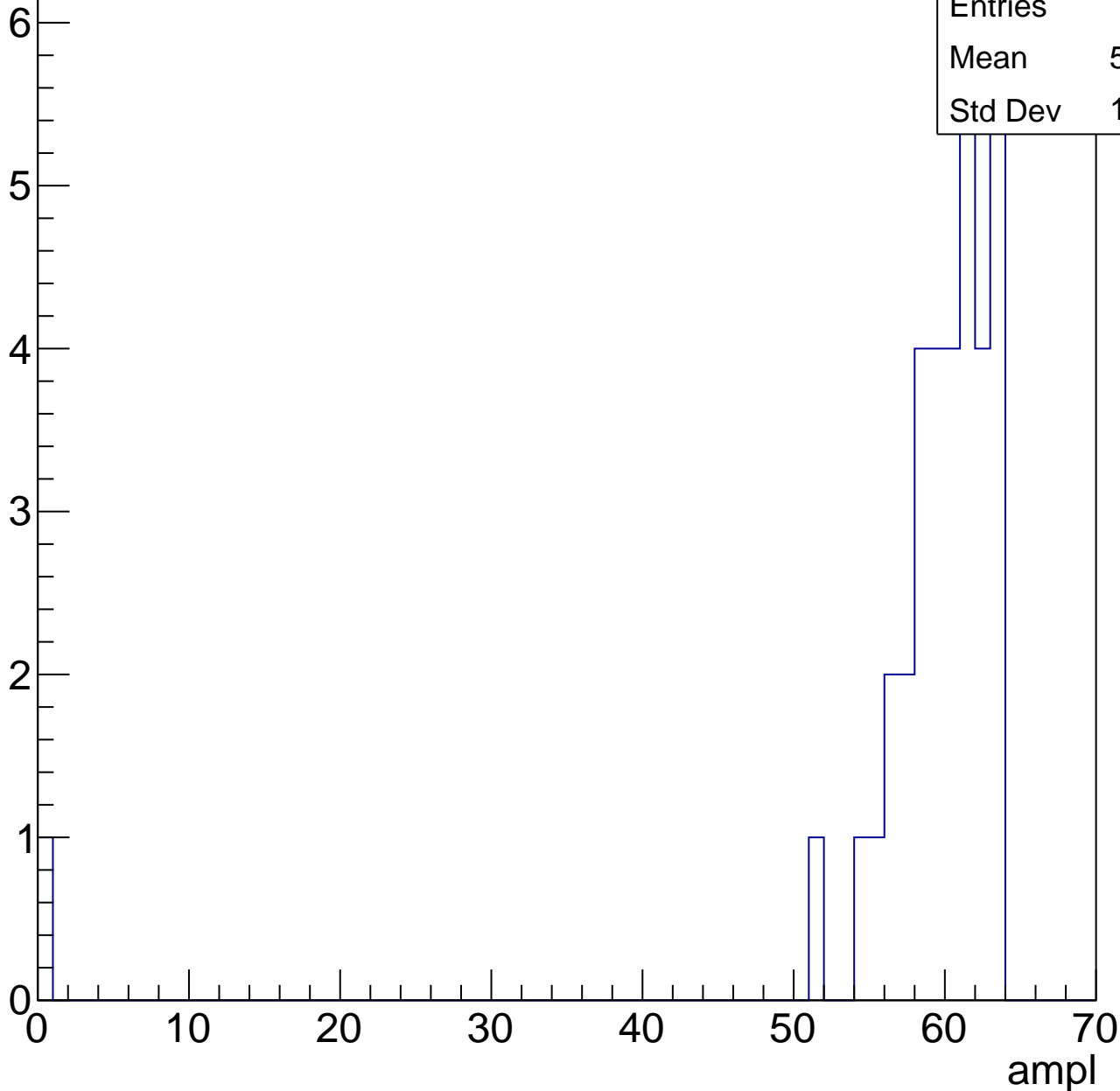


# B0L001S, U6-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	36
Mean	57.94
Std Dev	10.19

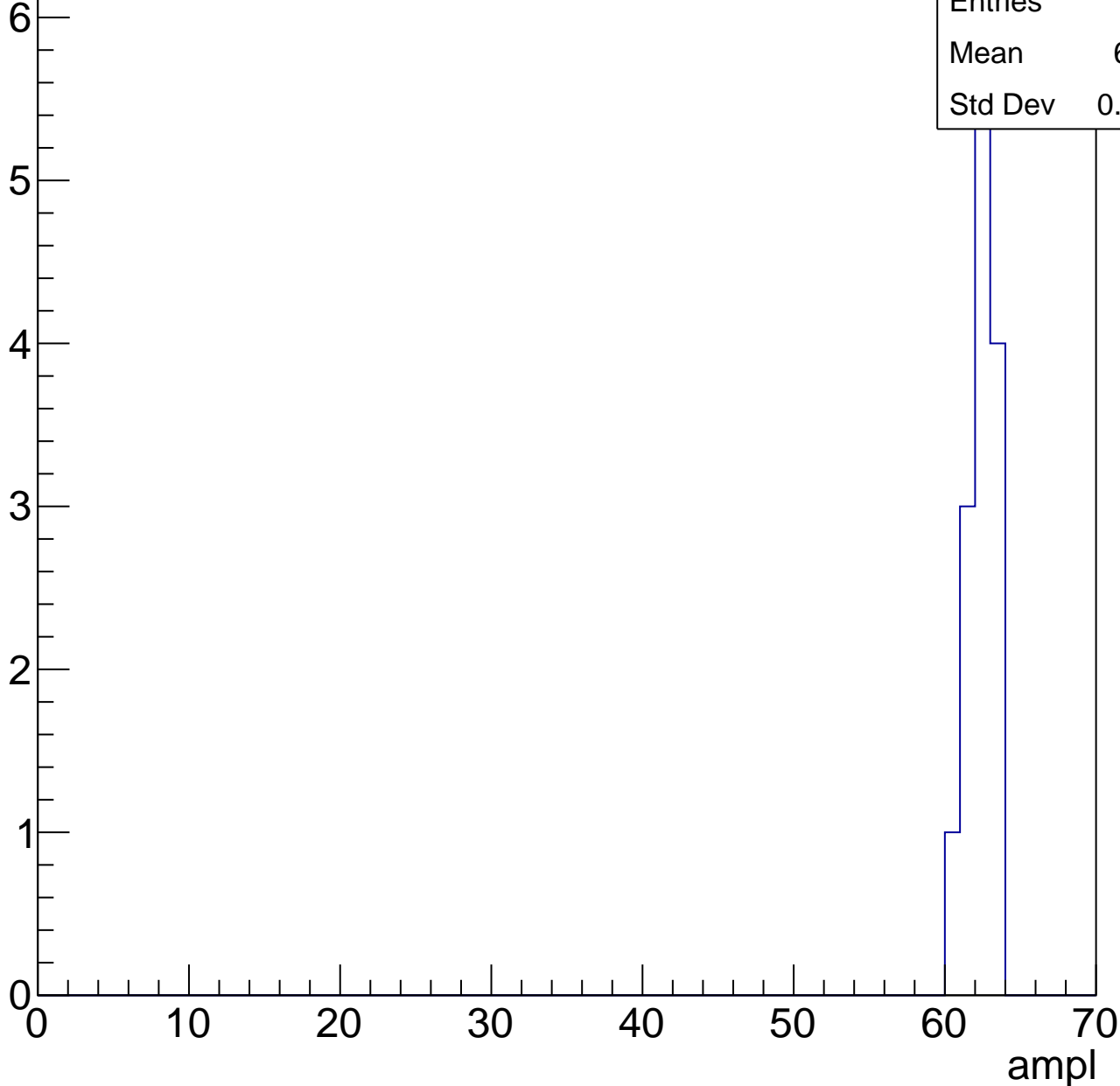


# B0L001S, U6-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	14
Mean	61.93
Std Dev	0.8835





# B0L001S, U6-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch117, adc0

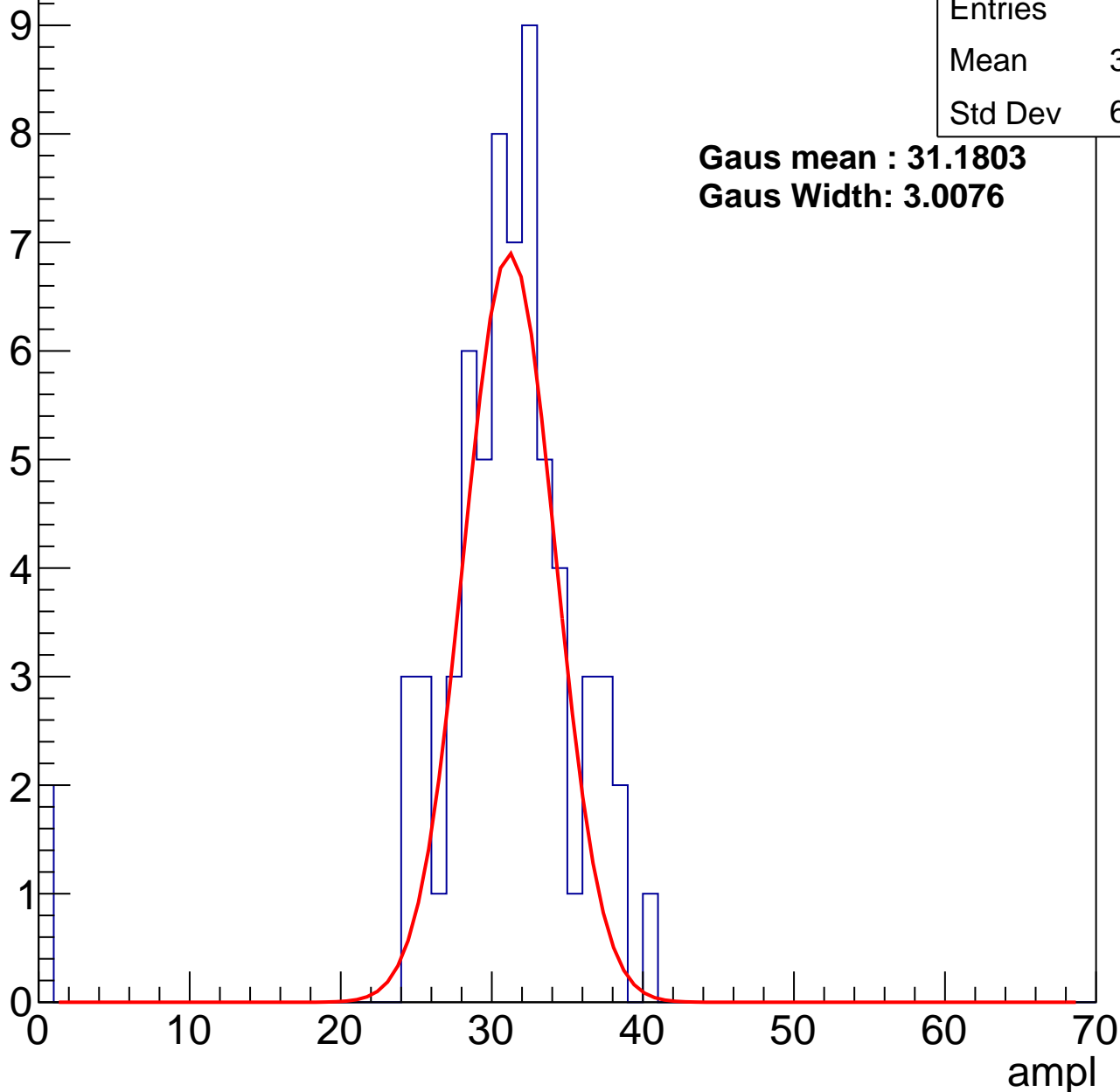
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	30.05
Std Dev	6.414

**Gaus mean : 31.1803**

**Gaus Width: 3.0076**



# B0L001S, U6-ch117, adc1

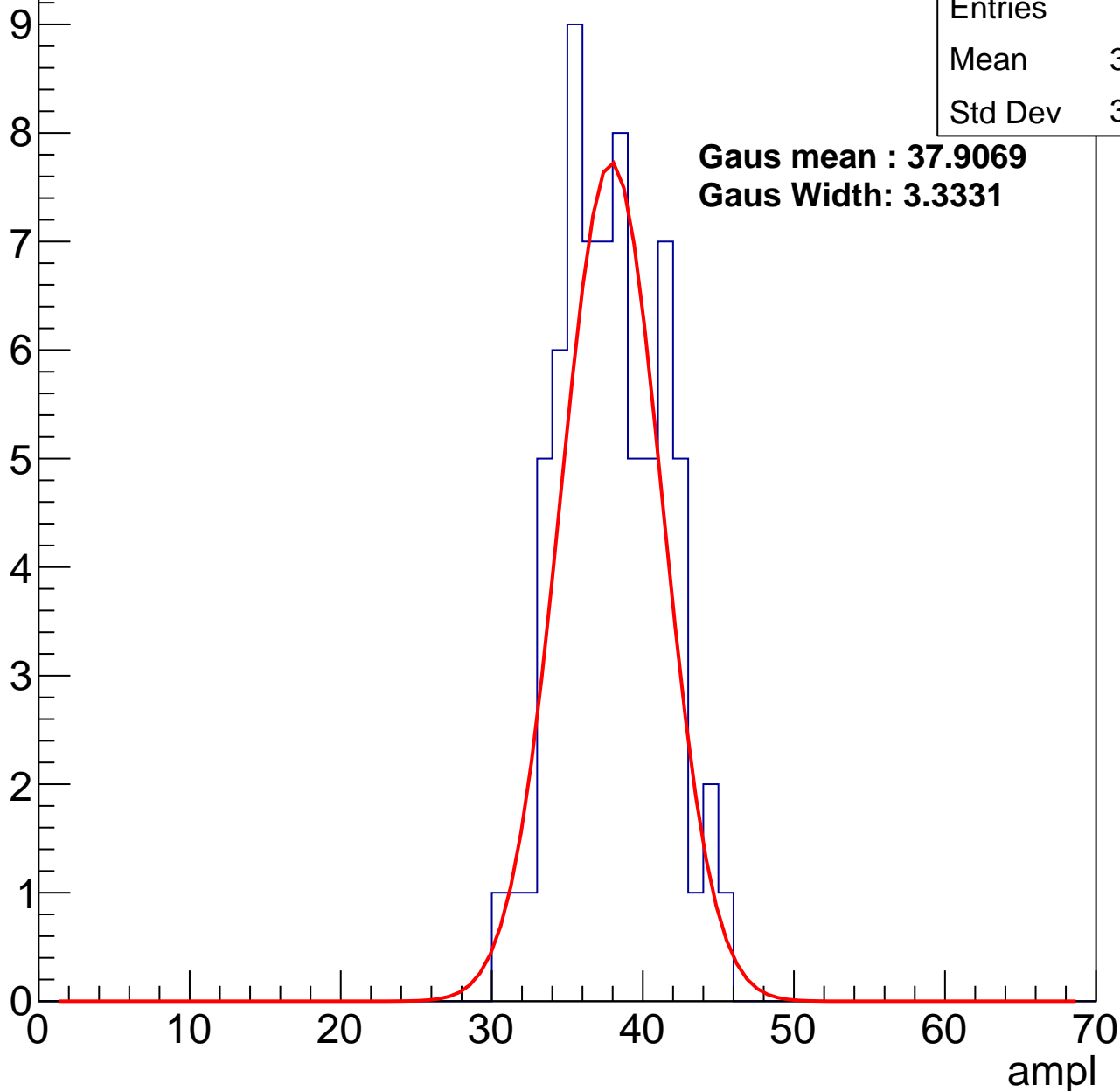
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	37.46
Std Dev	3.314

**Gaus mean : 37.9069**

**Gaus Width: 3.3331**



# B0L001S, U6-ch117, adc2

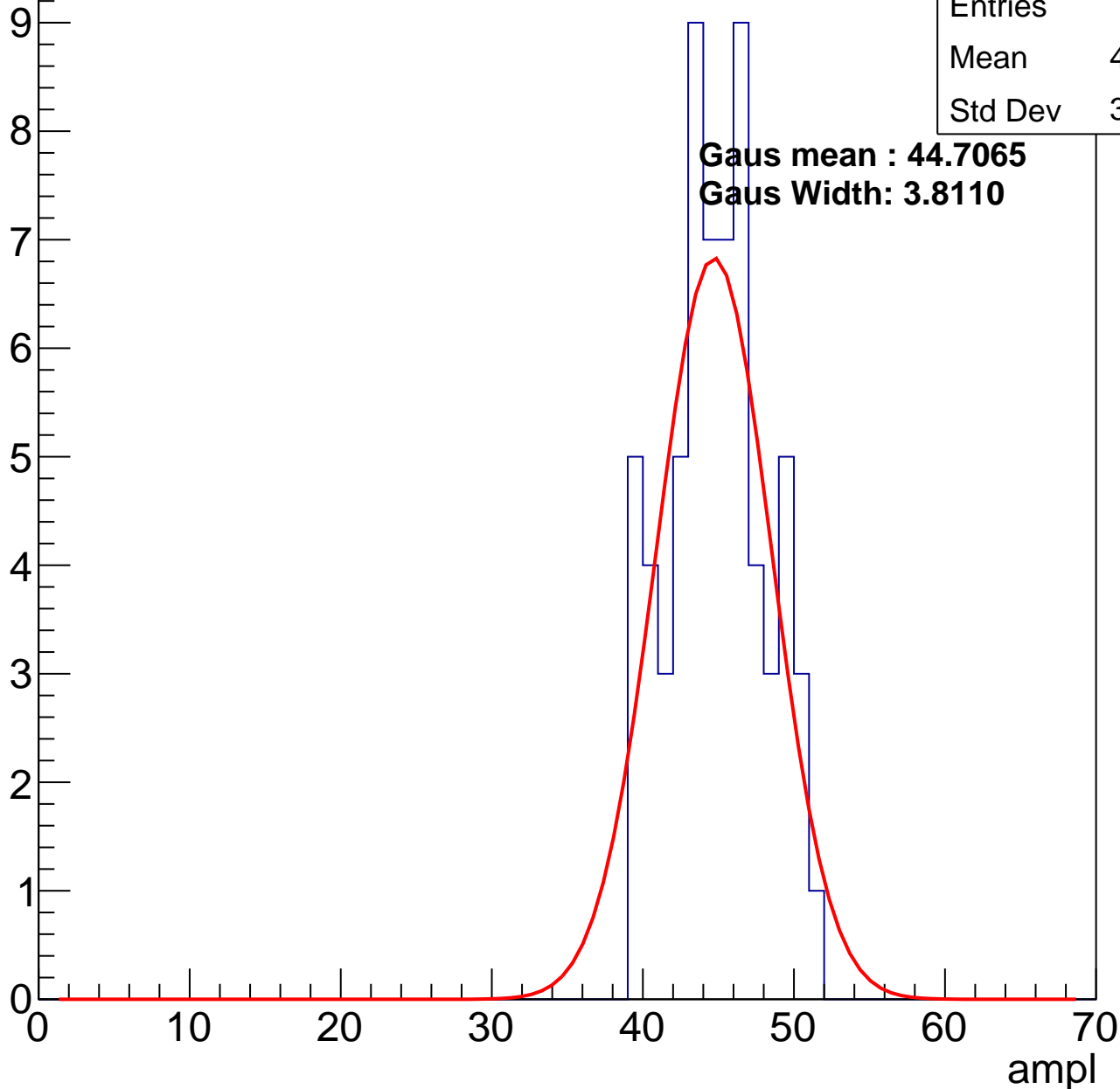
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	44.46
Std Dev	3.138

**Gaus mean : 44.7065**

**Gaus Width: 3.8110**

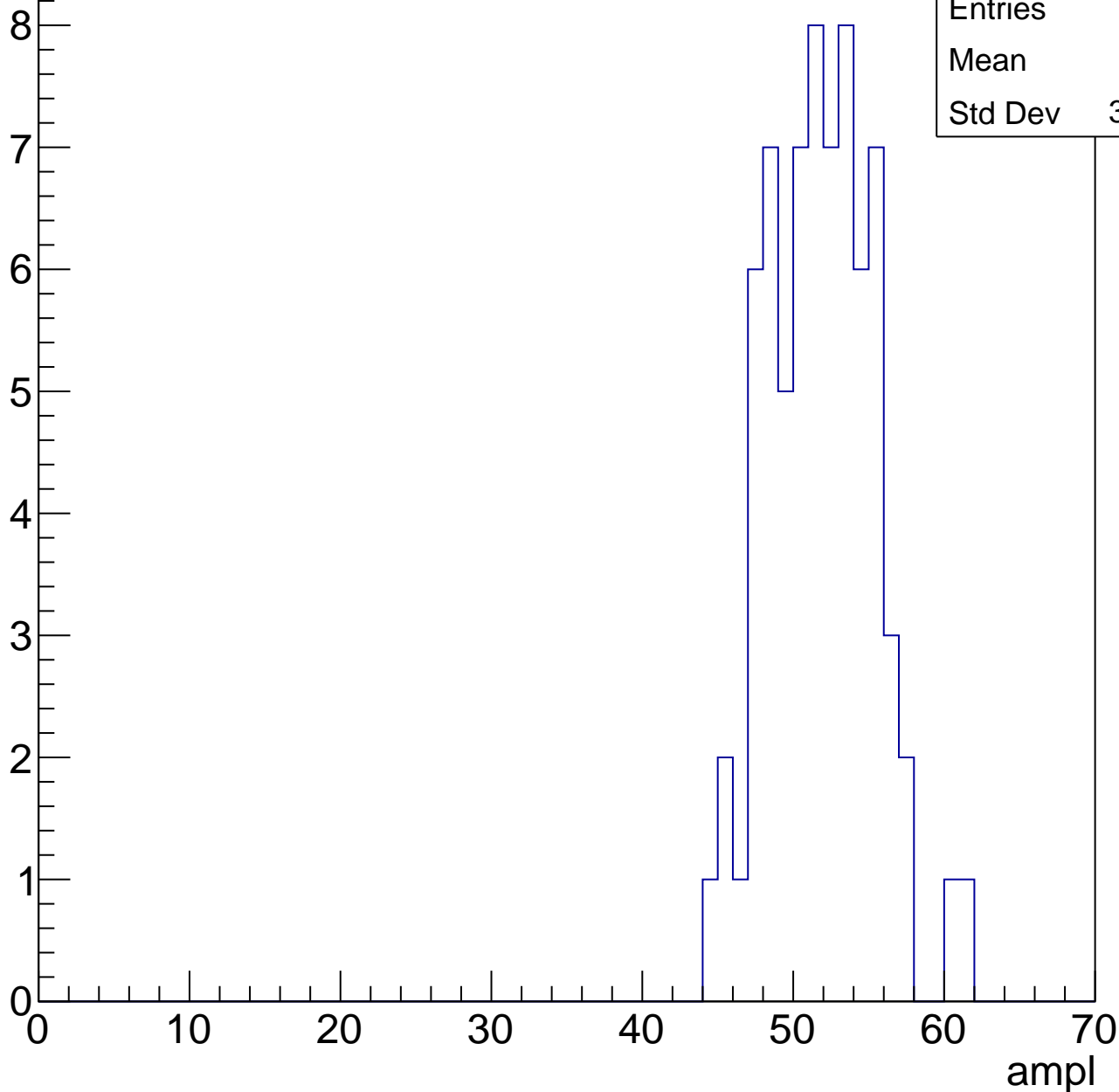


# B0L001S, U6-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

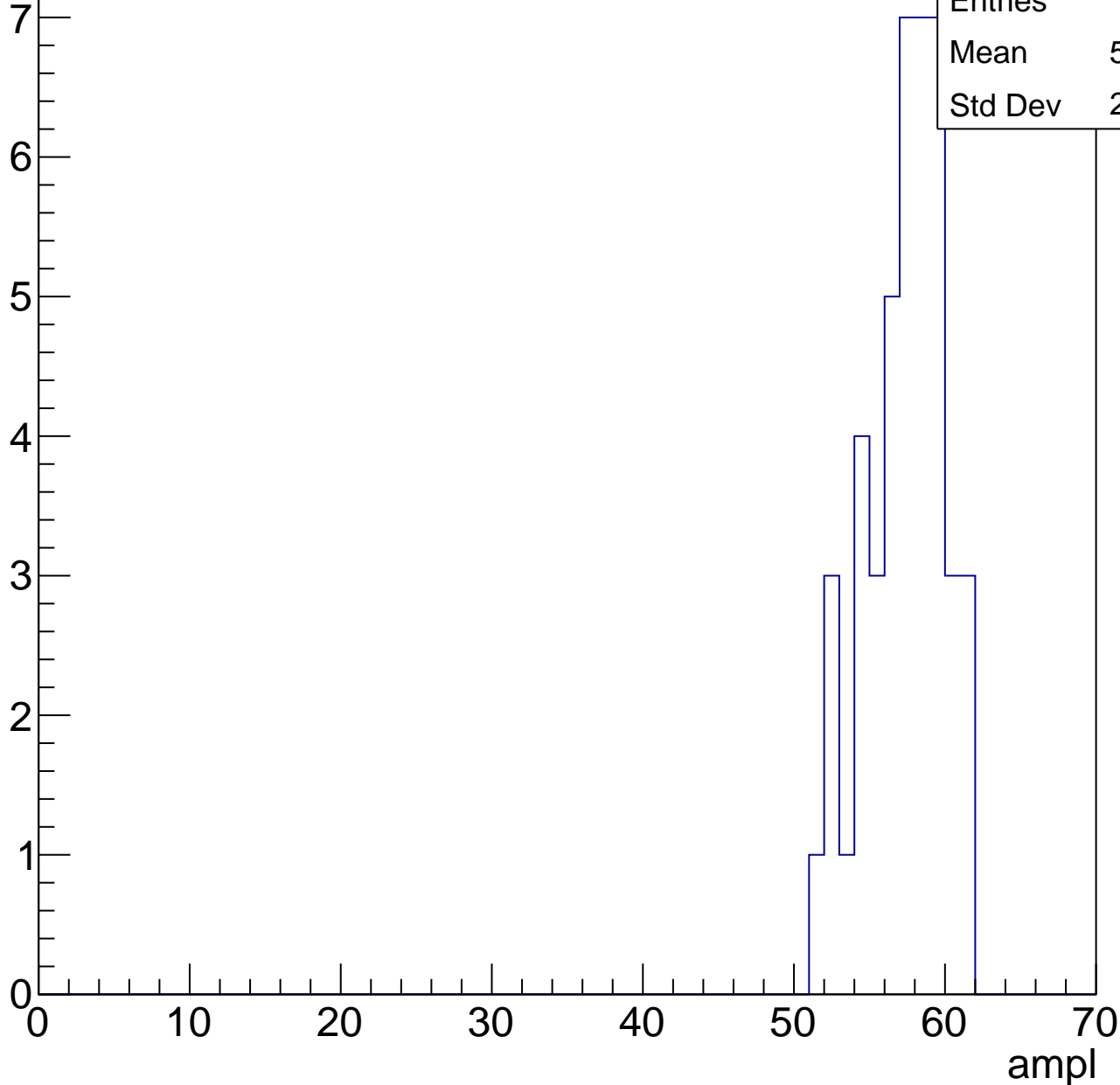
Entries	72
Mean	51.4
Std Dev	3.443



# B0L001S, U6-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



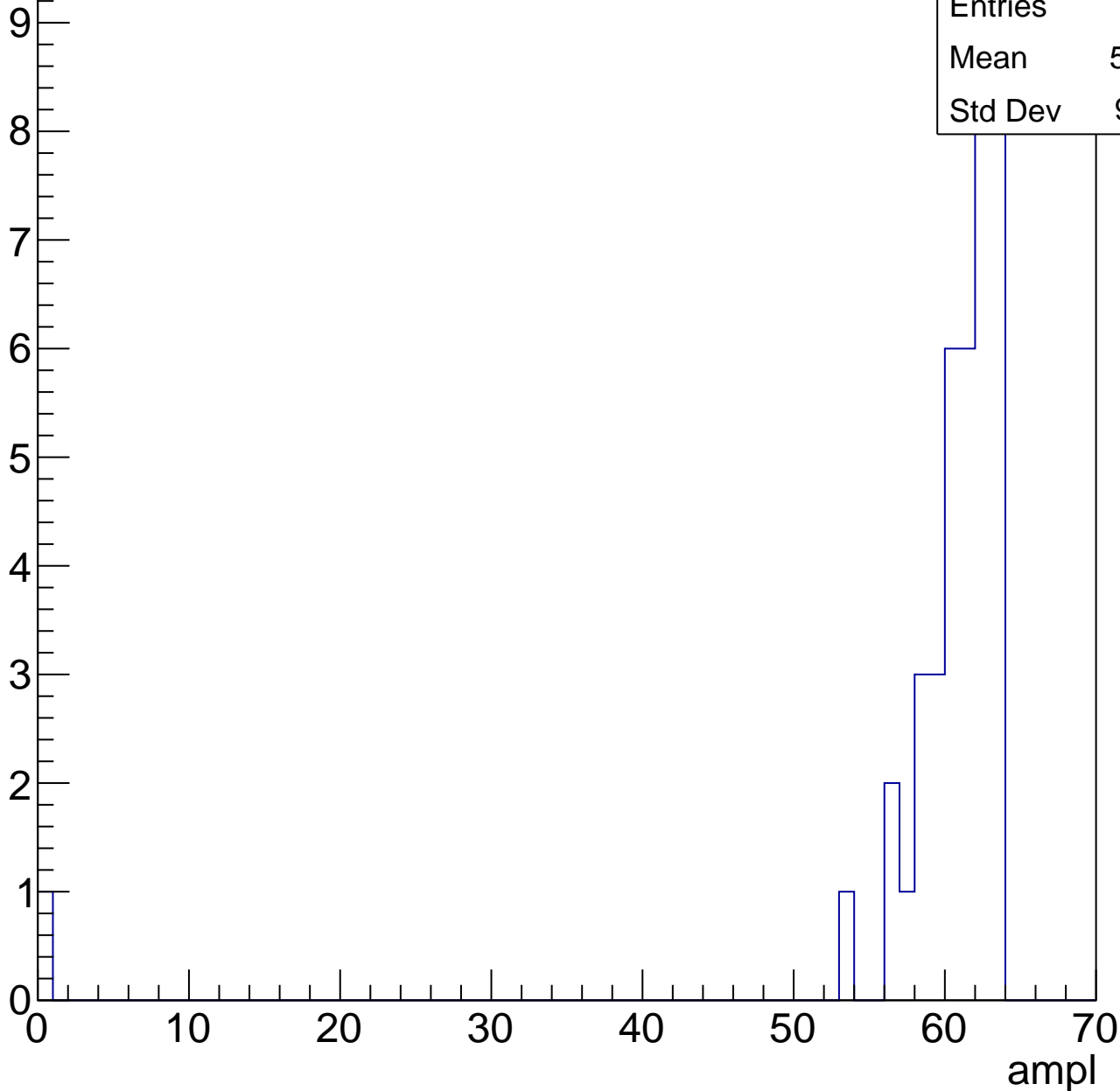
Entries	44
Mean	56.86
Std Dev	2.564

# B0L001S, U6-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	40
Mean	59.05
Std Dev	9.731



# B0L001S, U6-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B0L001S, U6-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch118, adc0

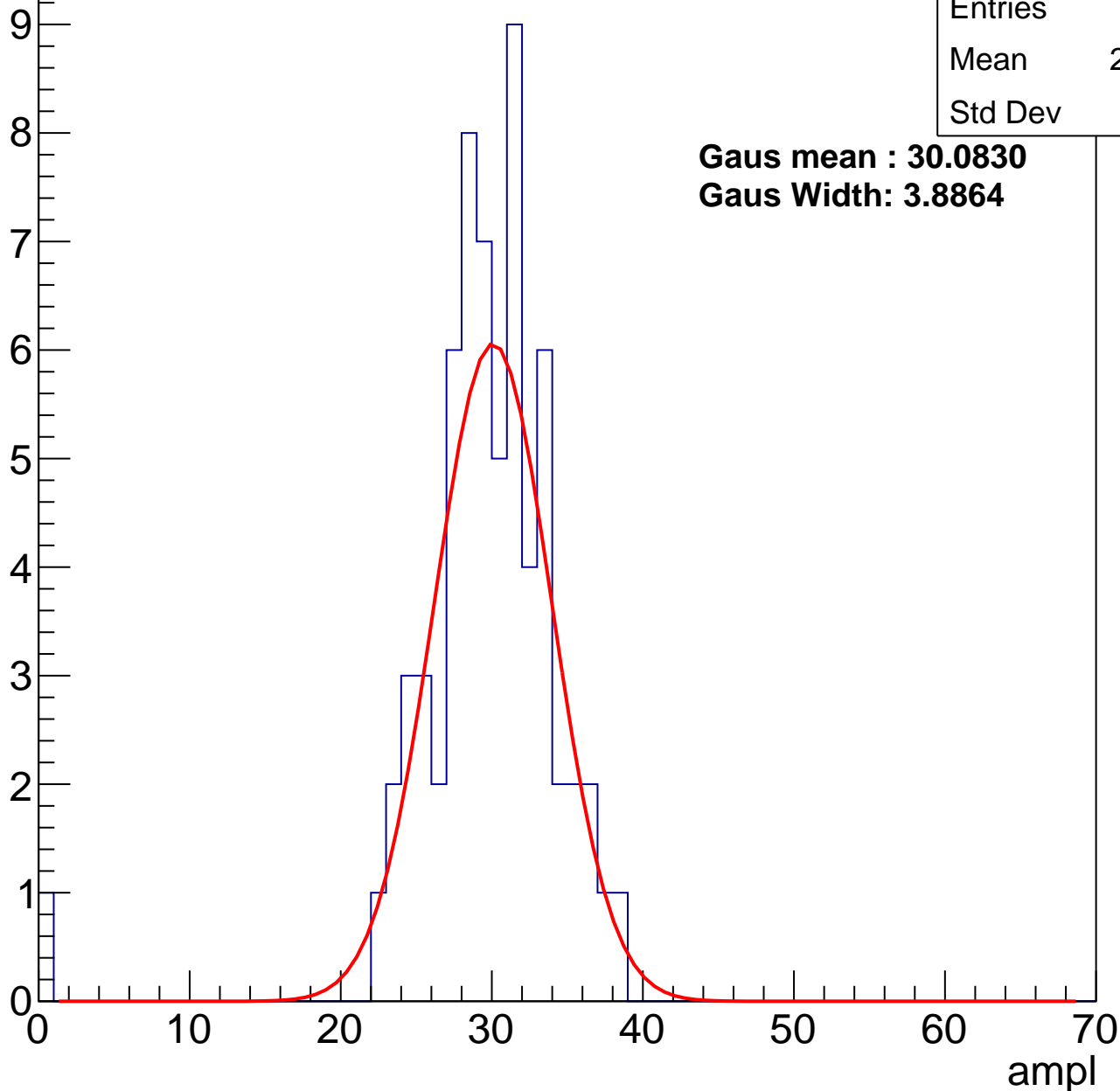
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	29.17
Std Dev	5.07

**Gaus mean : 30.0830**

**Gaus Width: 3.8864**



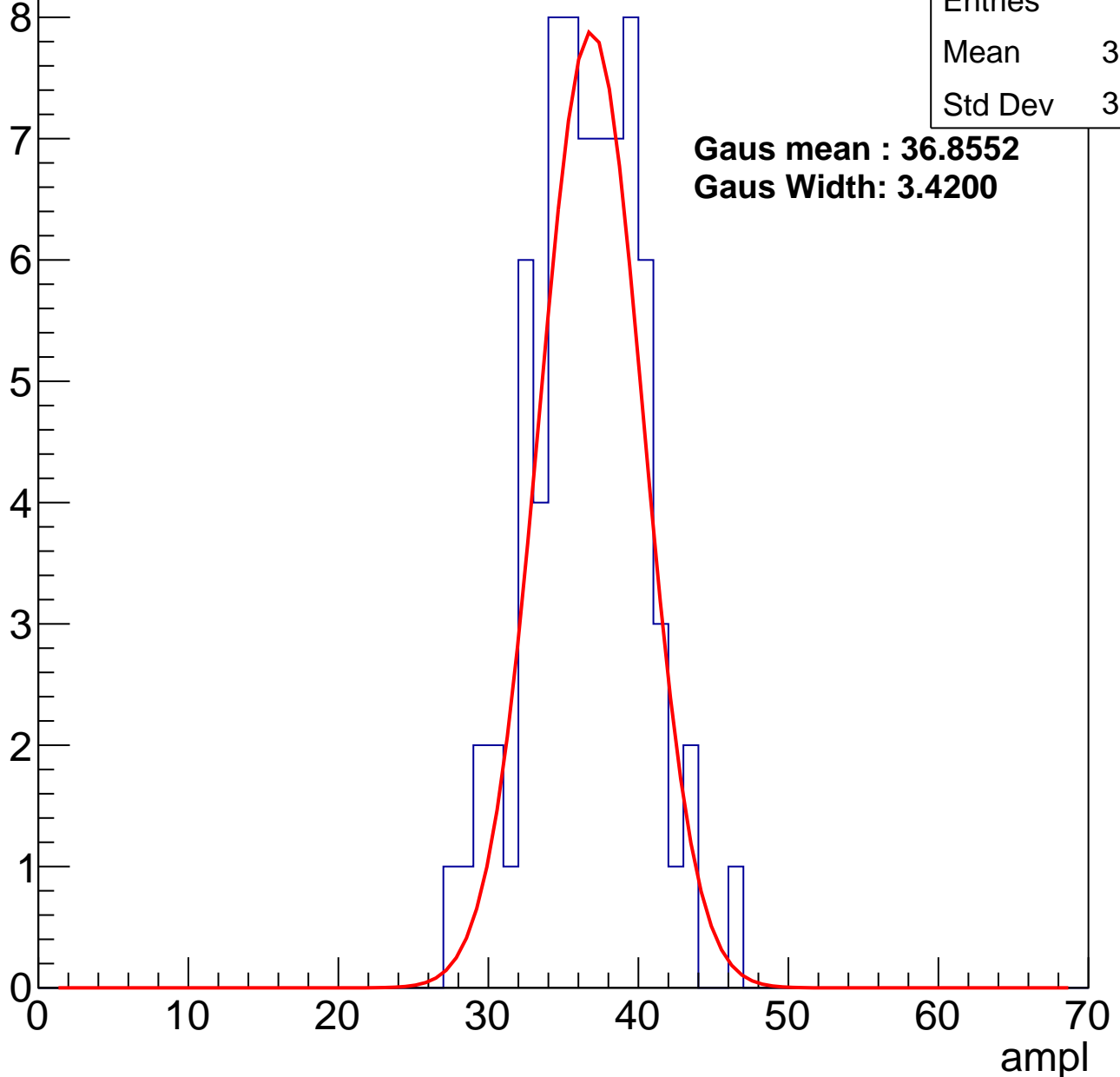
# B0L001S, U6-ch118, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	36.08
Std Dev	3.694

**Gaus mean : 36.8552**  
**Gaus Width: 3.4200**



# B0L001S, U6-ch118, adc2

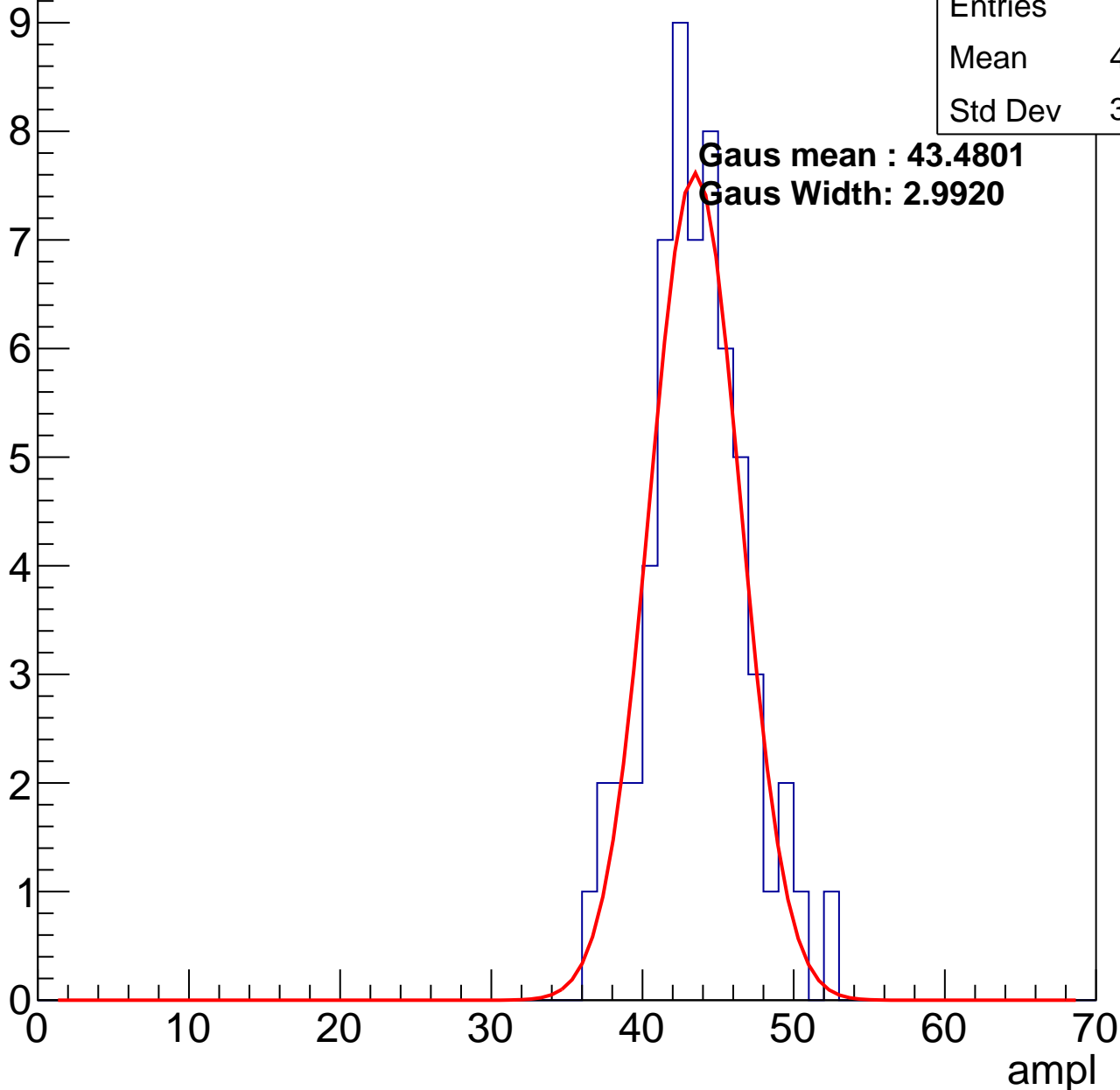
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	43.13
Std Dev	3.206

**Gaus mean : 43.4801**

**Gaus Width: 2.9920**

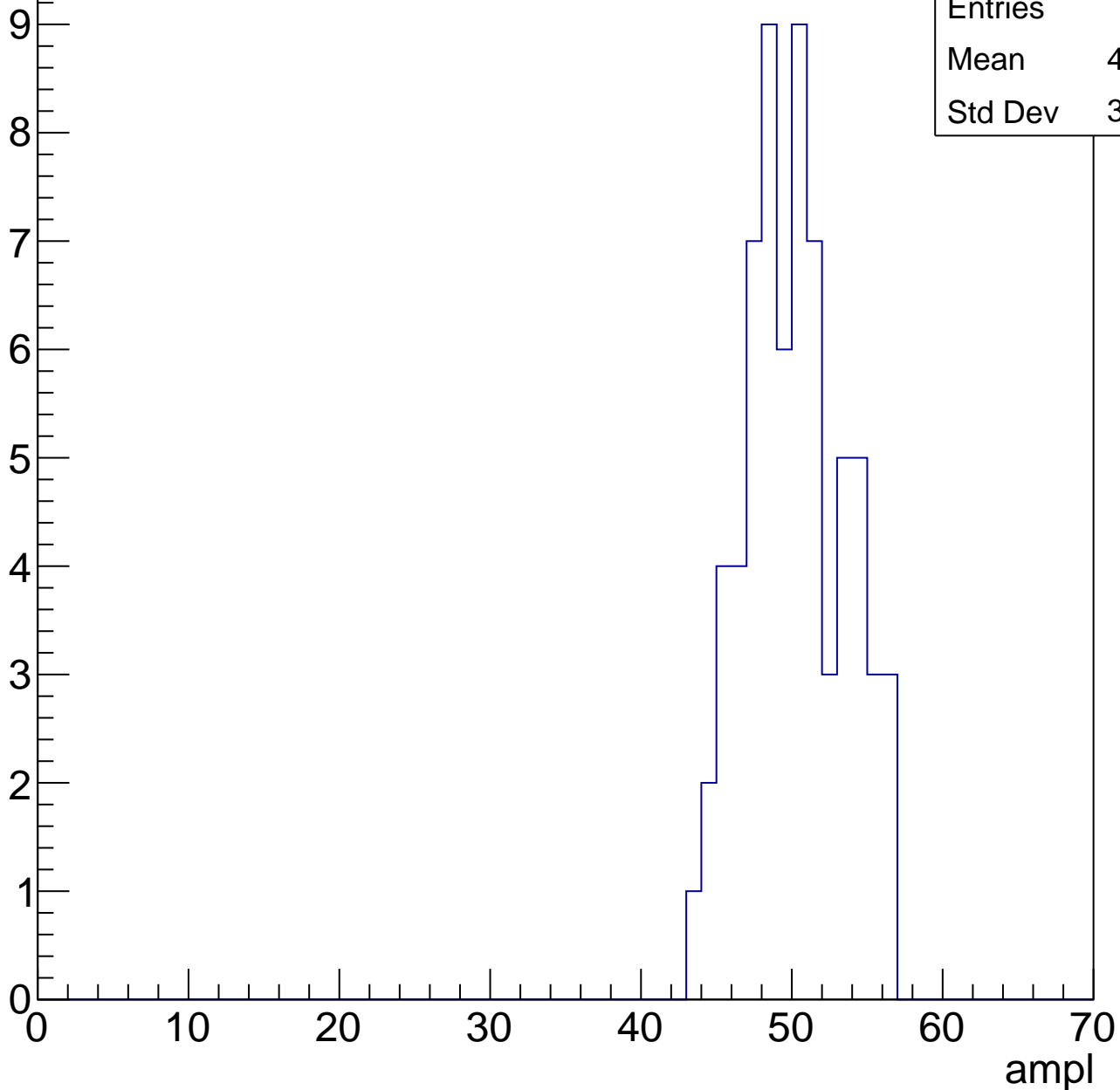


# B0L001S, U6-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	49.72
Std Dev	3.235

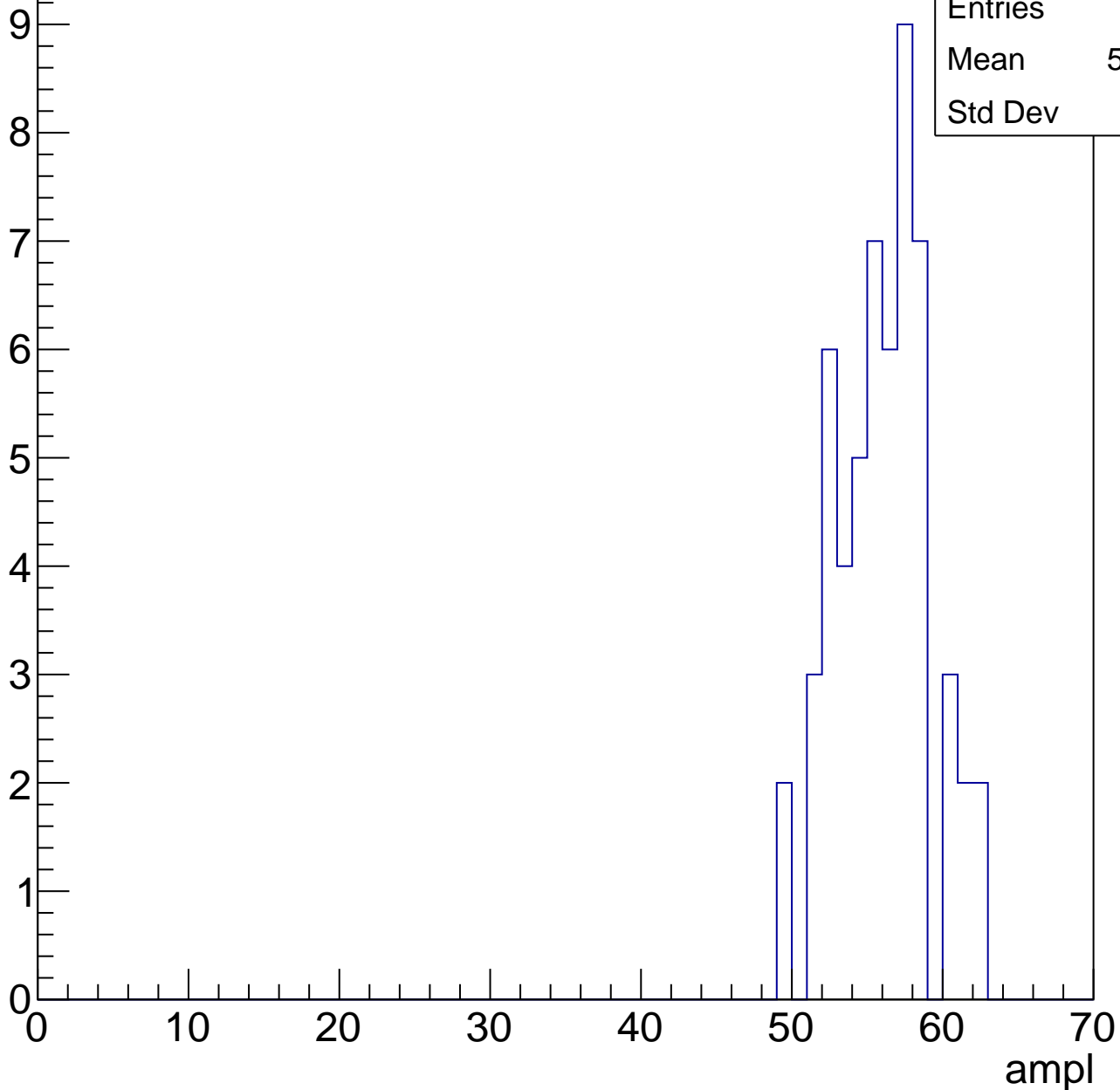


# B0L001S, U6-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	55.55
Std Dev	3.07



# B0L001S, U6-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

10

Entries 48

Mean 59.17

Std Dev 8.877

8

6

4

2

0

0

10

20

30

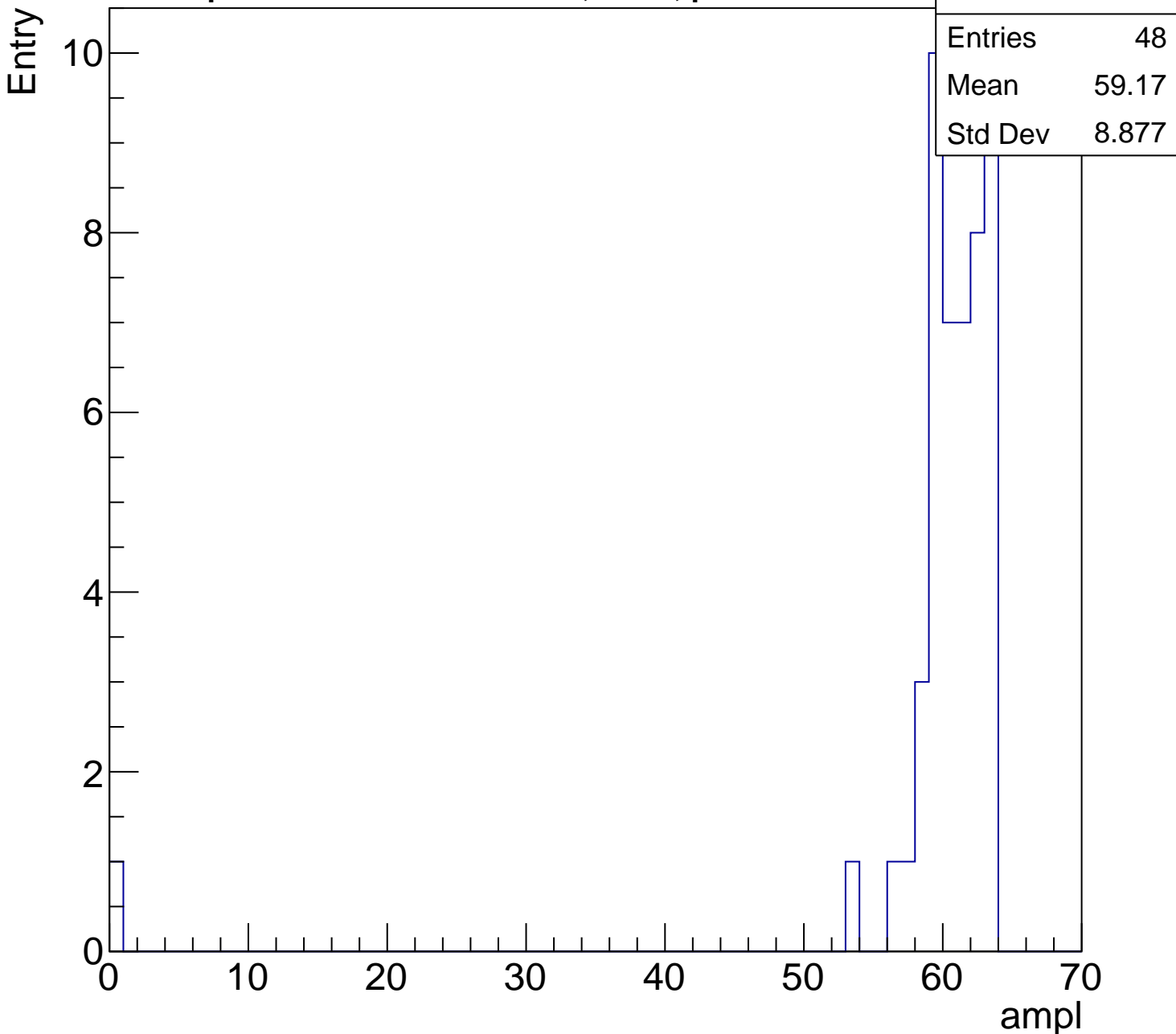
40

50

60

ampl

70



# B0L001S, U6-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch119, adc0

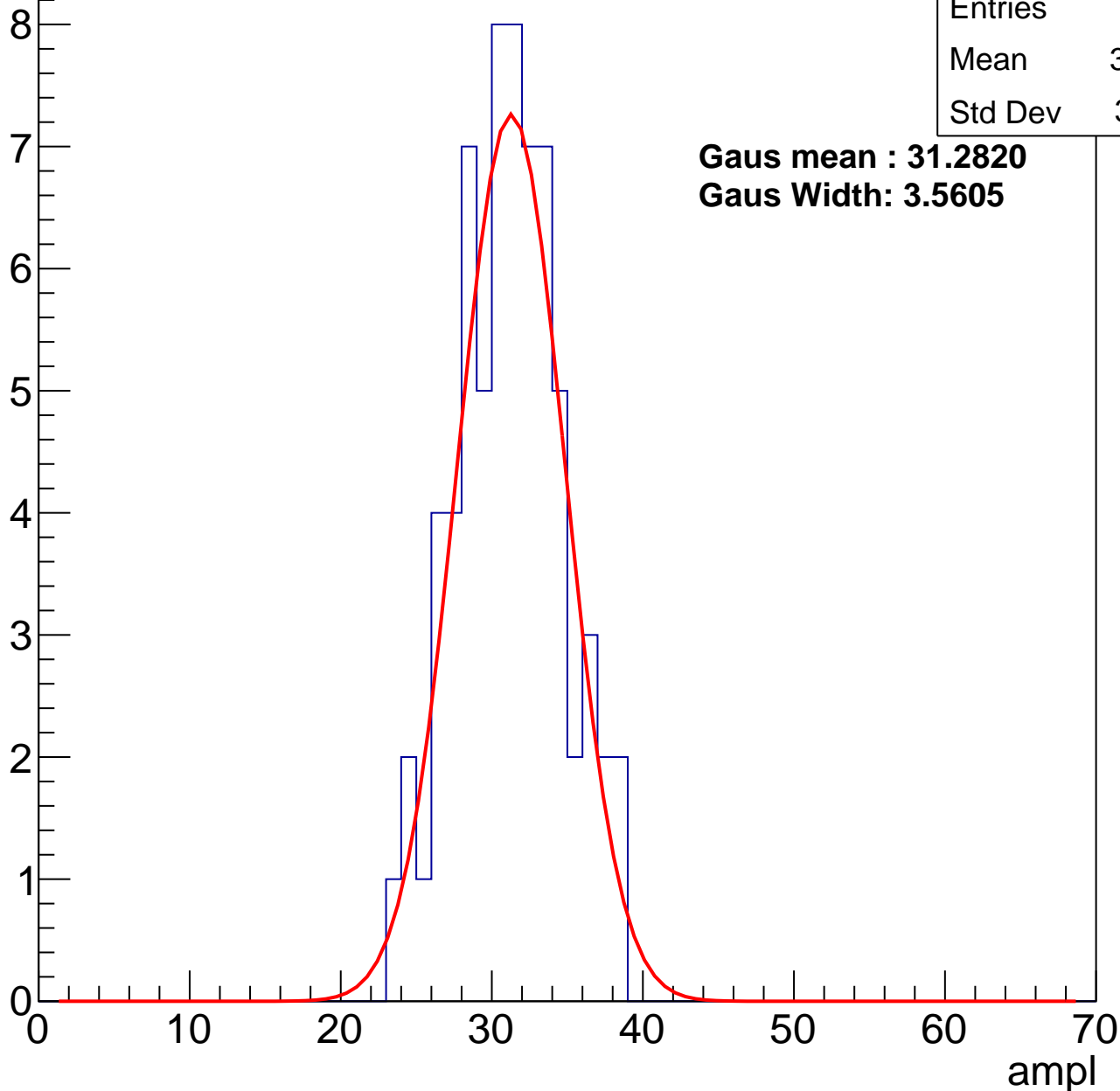
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	30.74
Std Dev	3.441

**Gaus mean : 31.2820**

**Gaus Width: 3.5605**



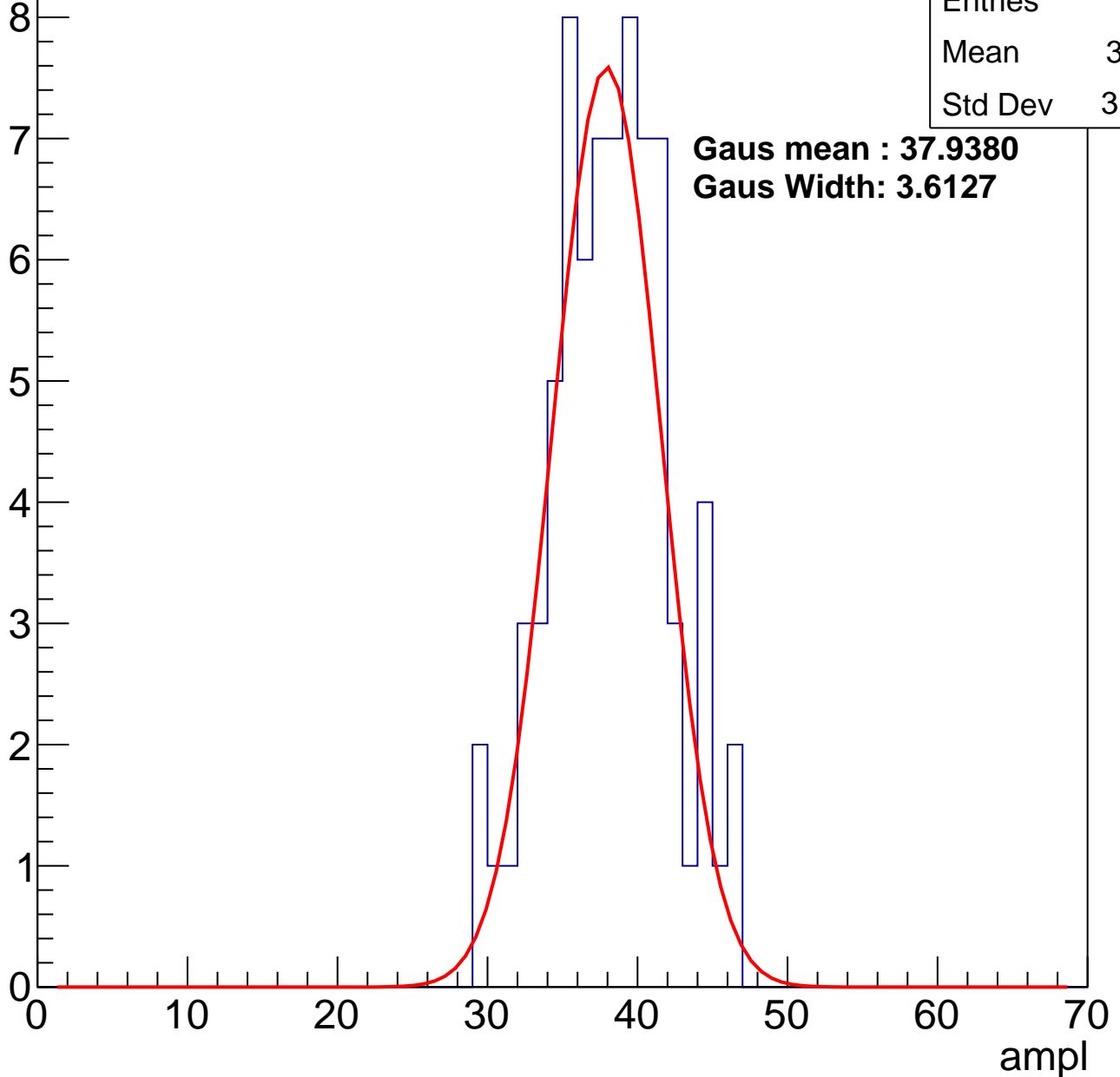
# B0L001S, U6-ch119, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	37.71
Std Dev	3.852

**Gaus mean : 37.9380**  
**Gaus Width: 3.6127**



# B0L001S, U6-ch119, adc2

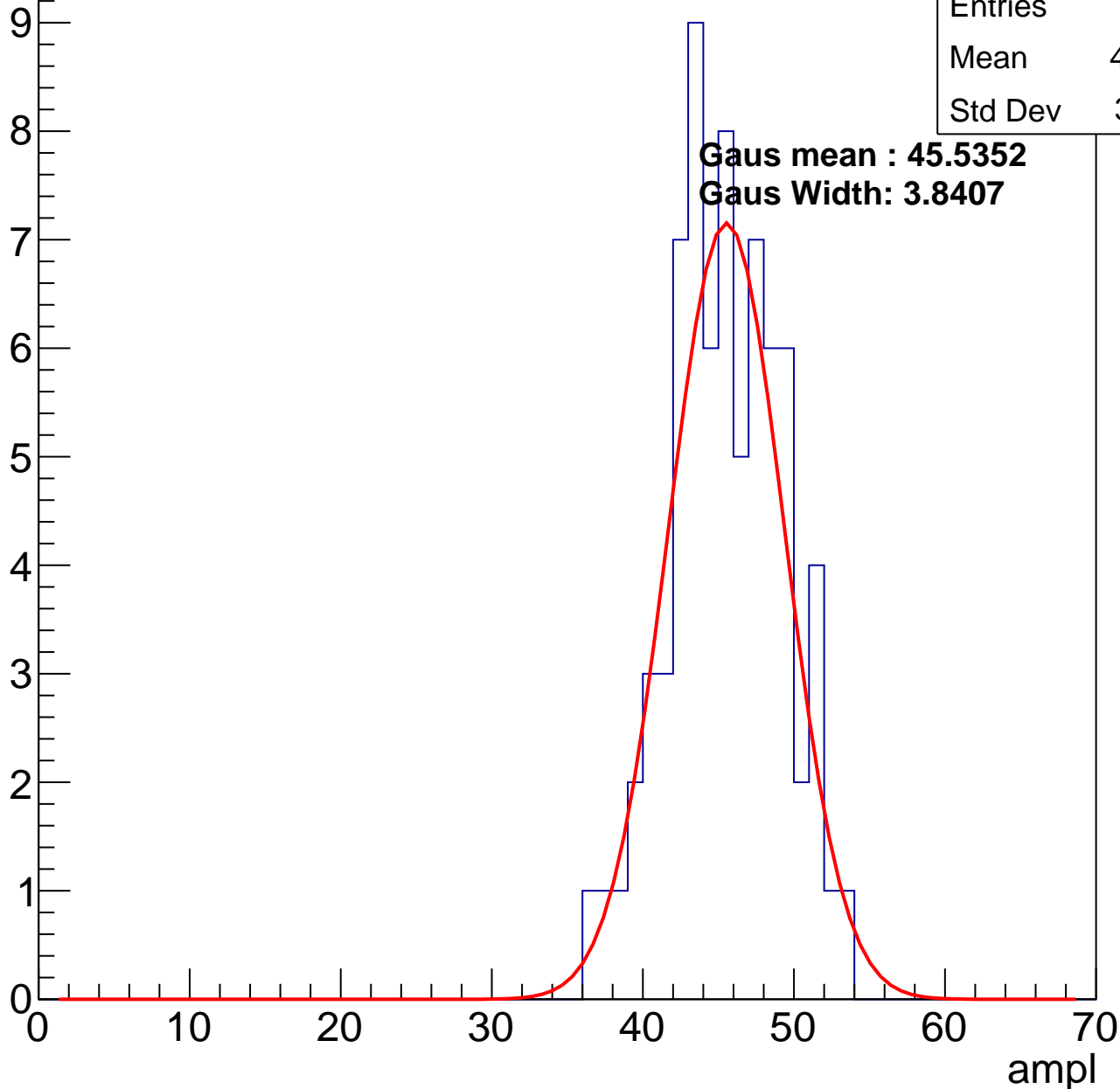
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	45.03
Std Dev	3.671

**Gaus mean : 45.5352**

**Gaus Width: 3.8407**

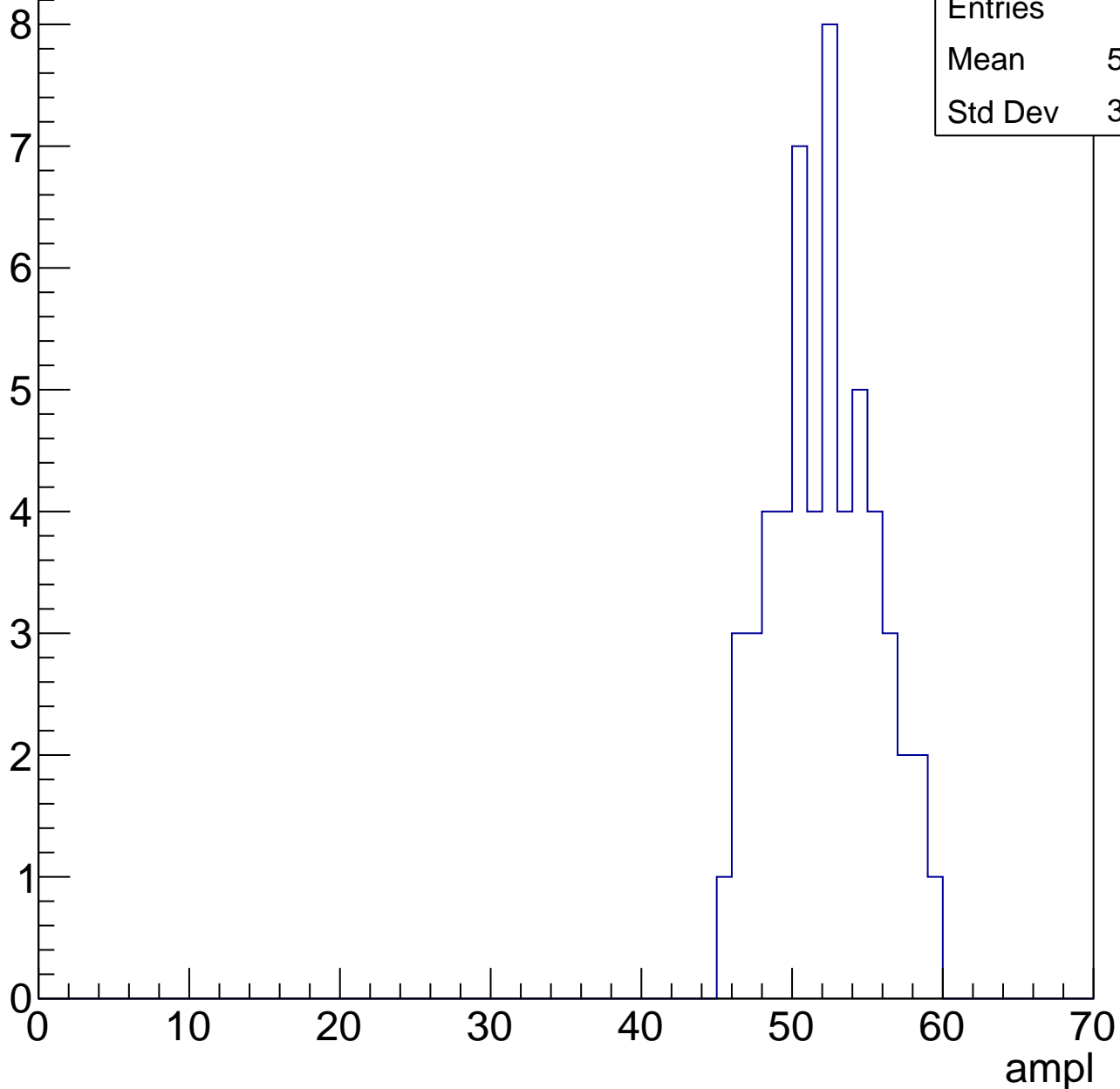


# B0L001S, U6-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	51.65
Std Dev	3.402

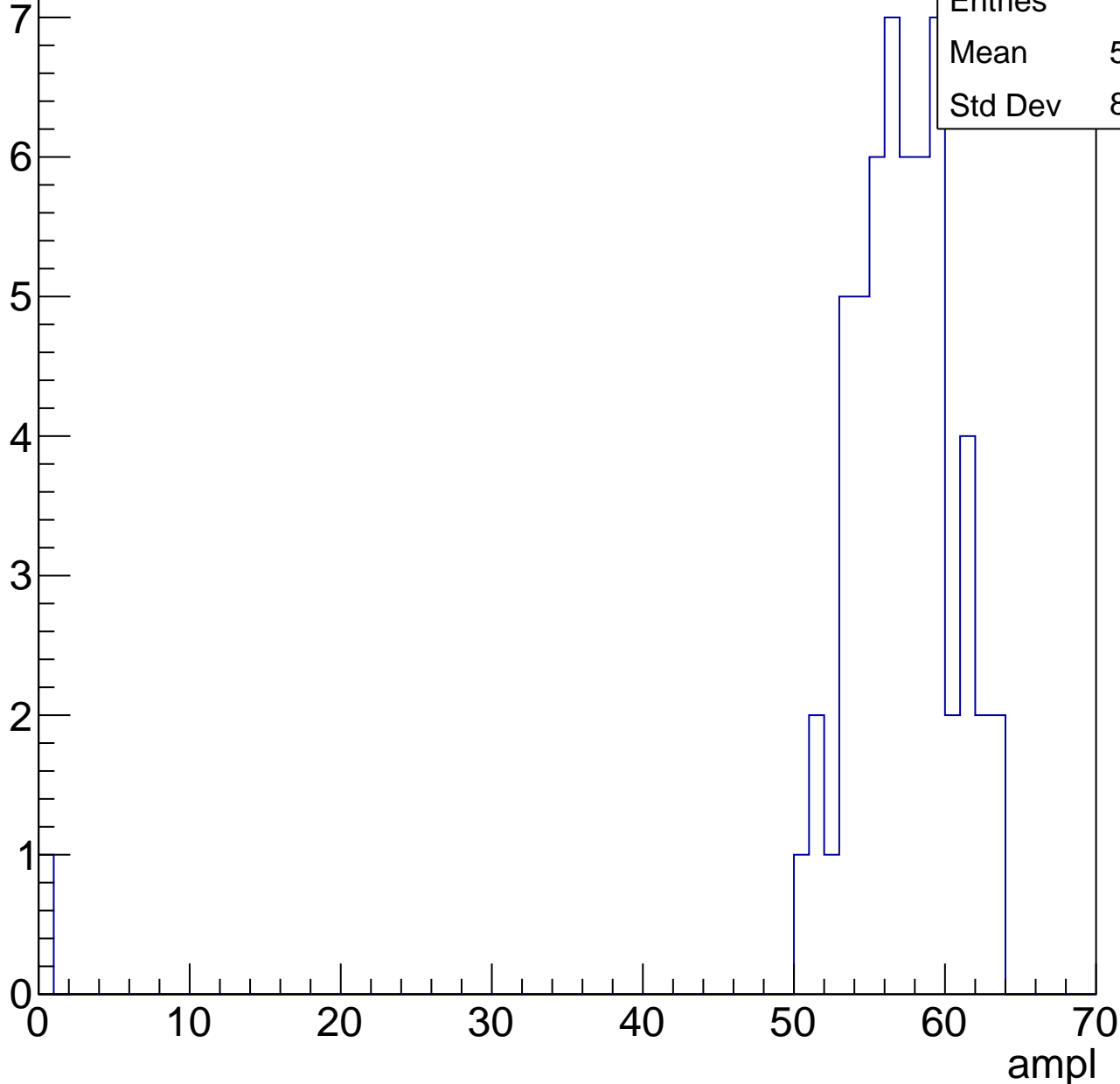


# B0L001S, U6-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	55.75
Std Dev	8.057



# B0L001S, U6-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

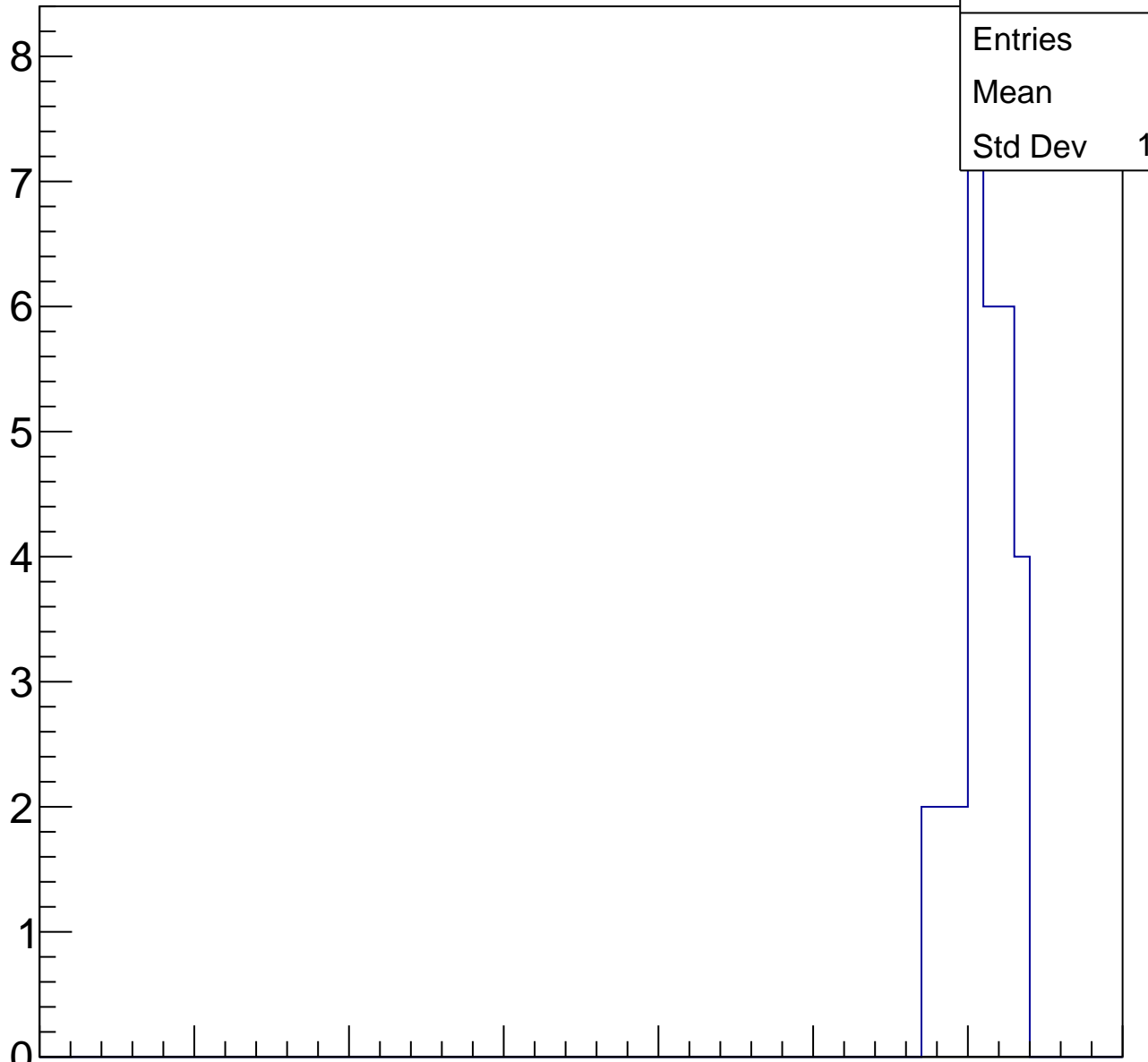
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	30
Mean	60.6
Std Dev	1.665

ampl

0 10 20 30 40 50 60 70



# B0L001S, U6-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U6-ch120, adc0

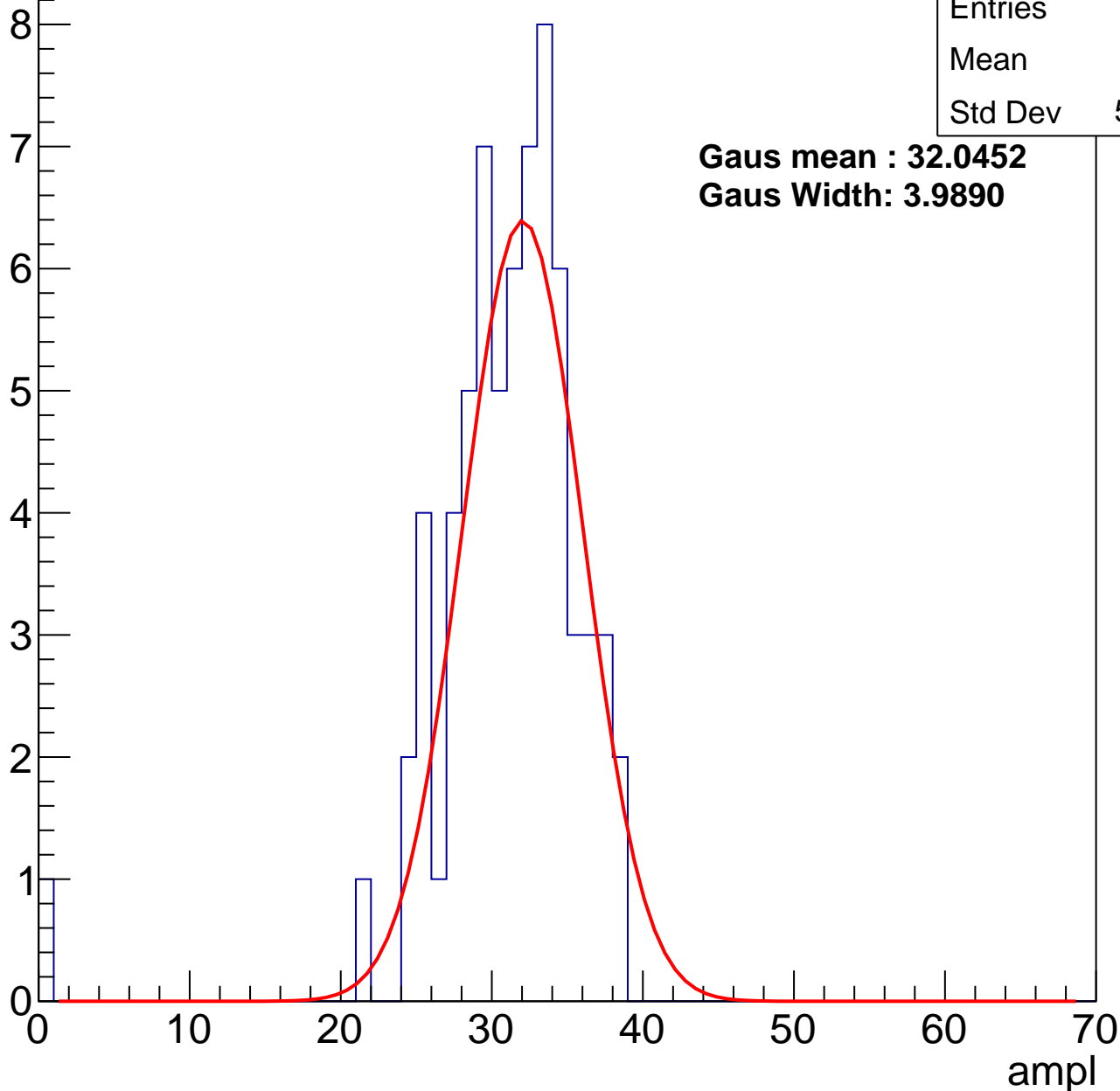
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	30.5
Std Dev	5.251

**Gaus mean : 32.0452**

**Gaus Width: 3.9890**



# B0L001S, U6-ch120, adc1

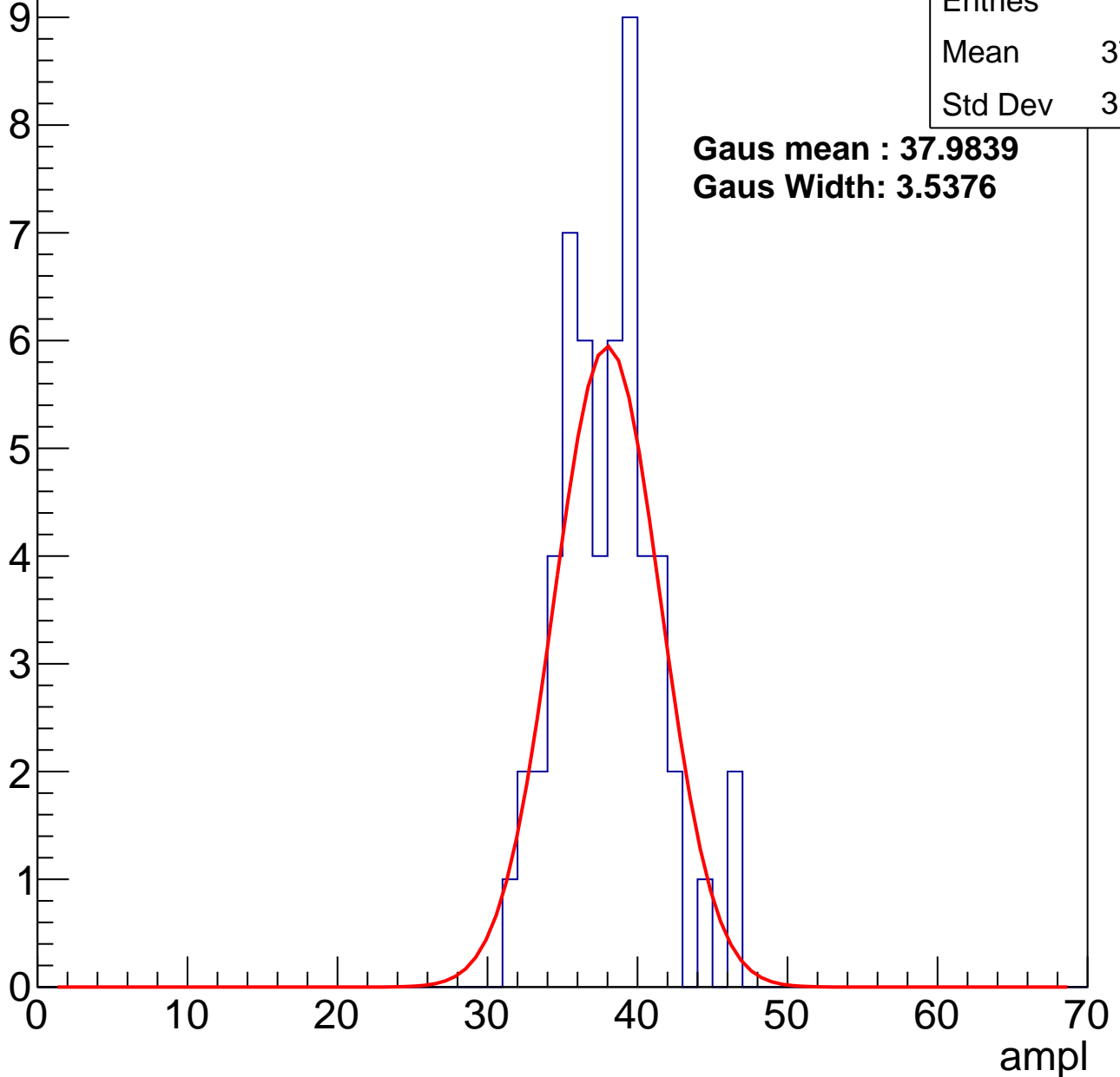
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	37.57
Std Dev	3.258

**Gaus mean : 37.9839**

**Gaus Width: 3.5376**



# B0L001S, U6-ch120, adc2

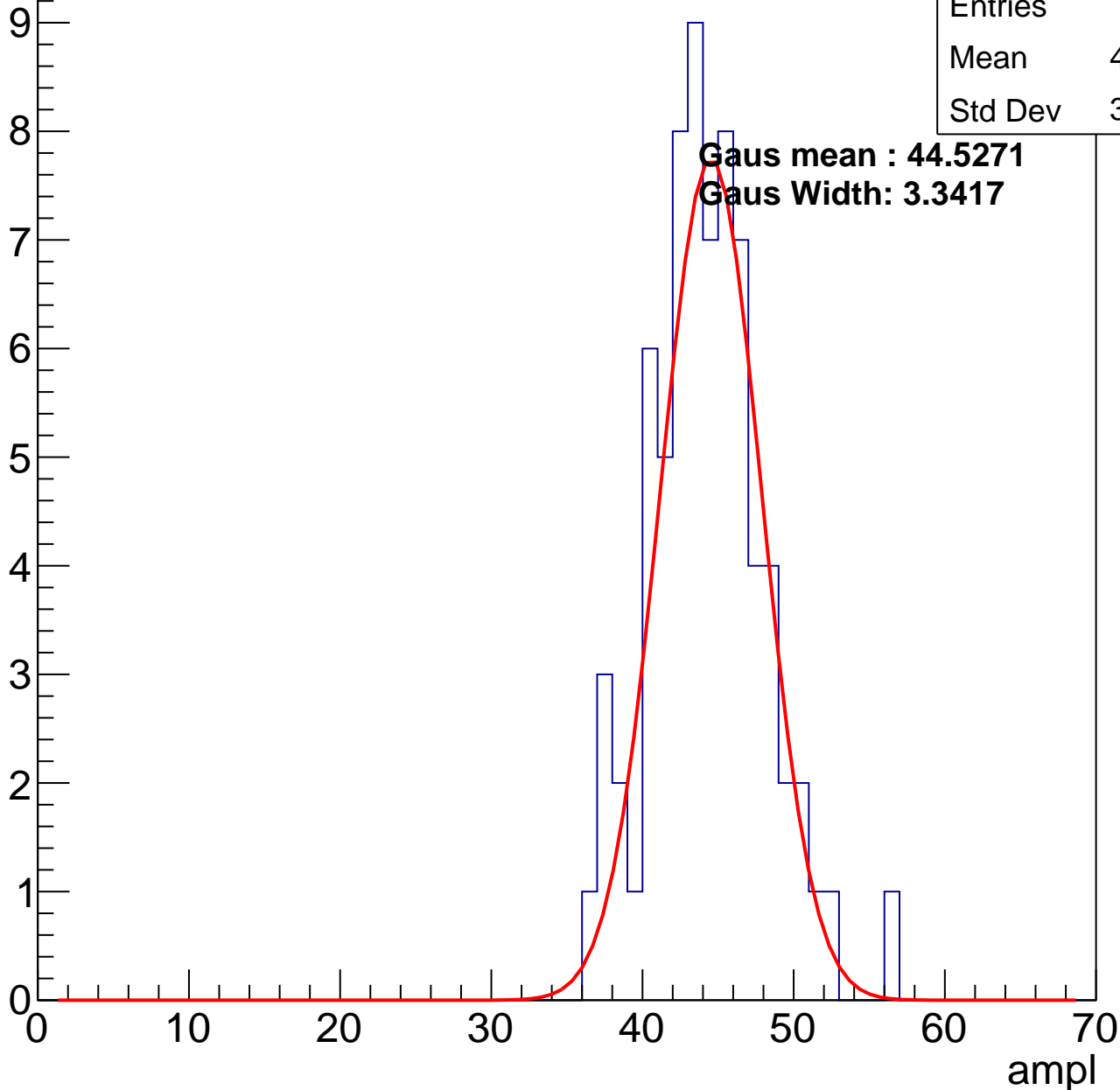
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	43.85
Std Dev	3.733

**Gaus mean : 44.5271**

**Gaus Width: 3.3417**

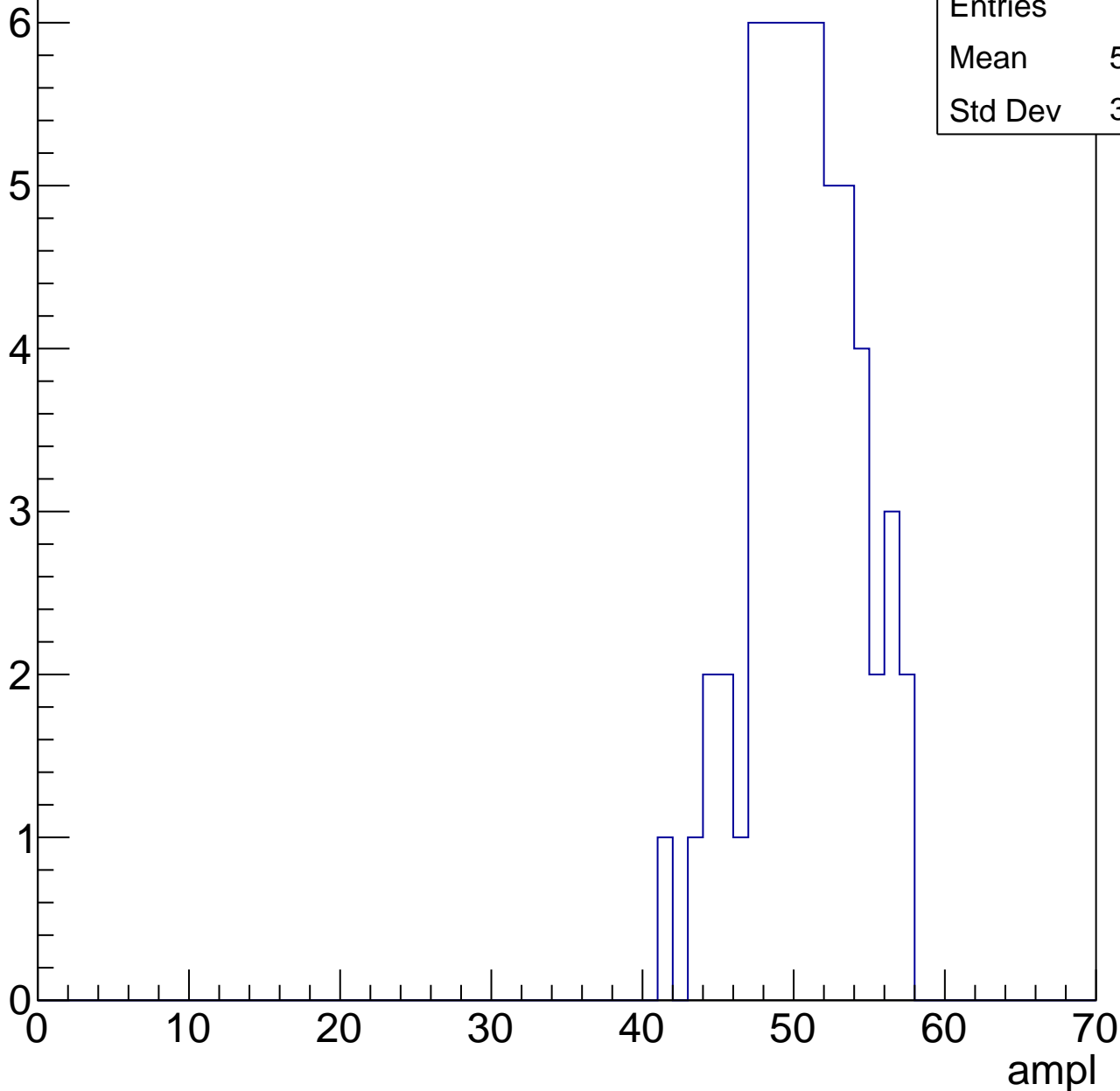


# B0L001S, U6-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	50.19
Std Dev	3.574

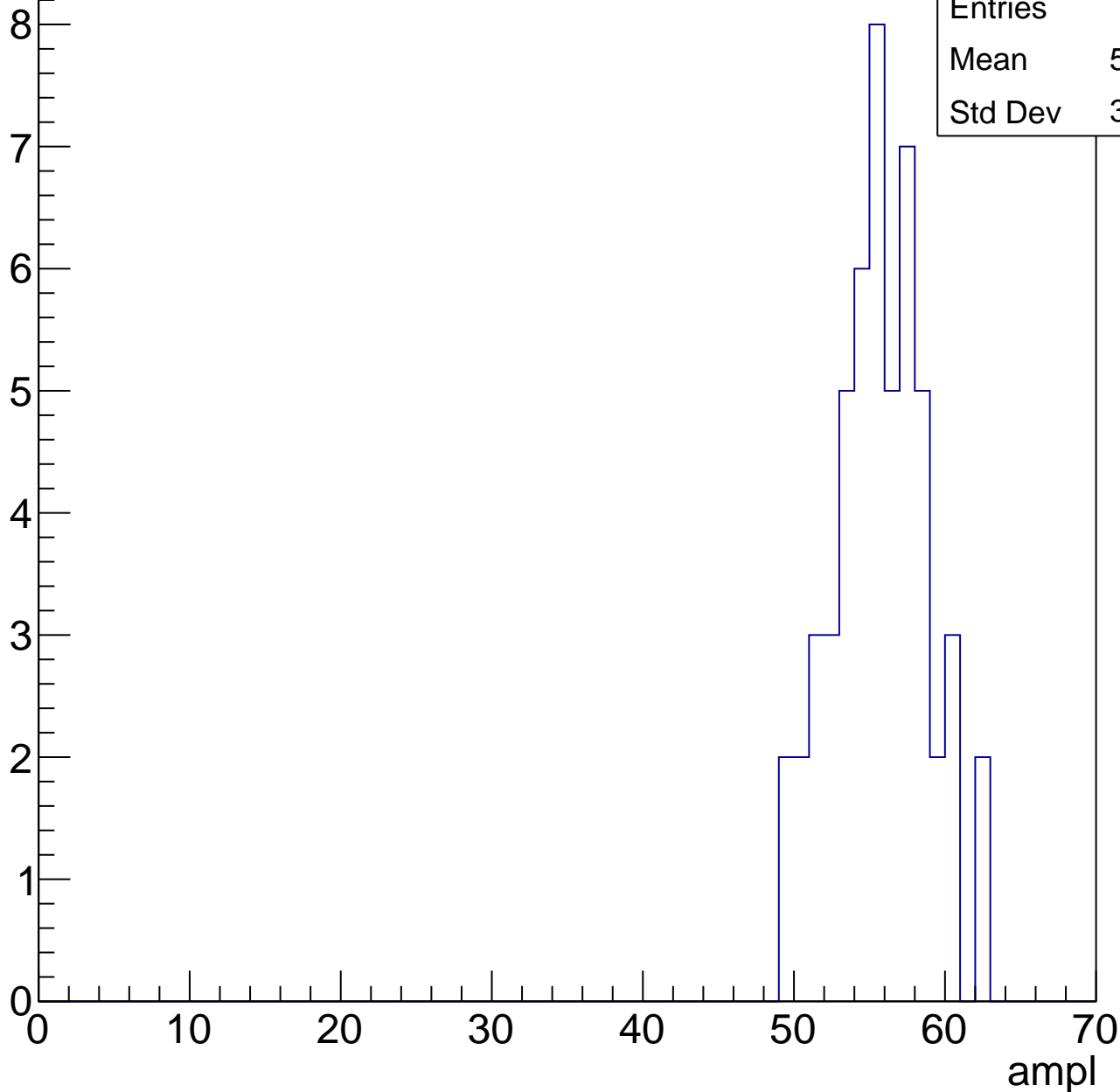


# B0L001S, U6-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	55.23
Std Dev	3.082



# B0L001S, U6-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	47
Mean	60.38
Std Dev	2.179

Entry

10

8

6

4

2

0

0

10

20

30

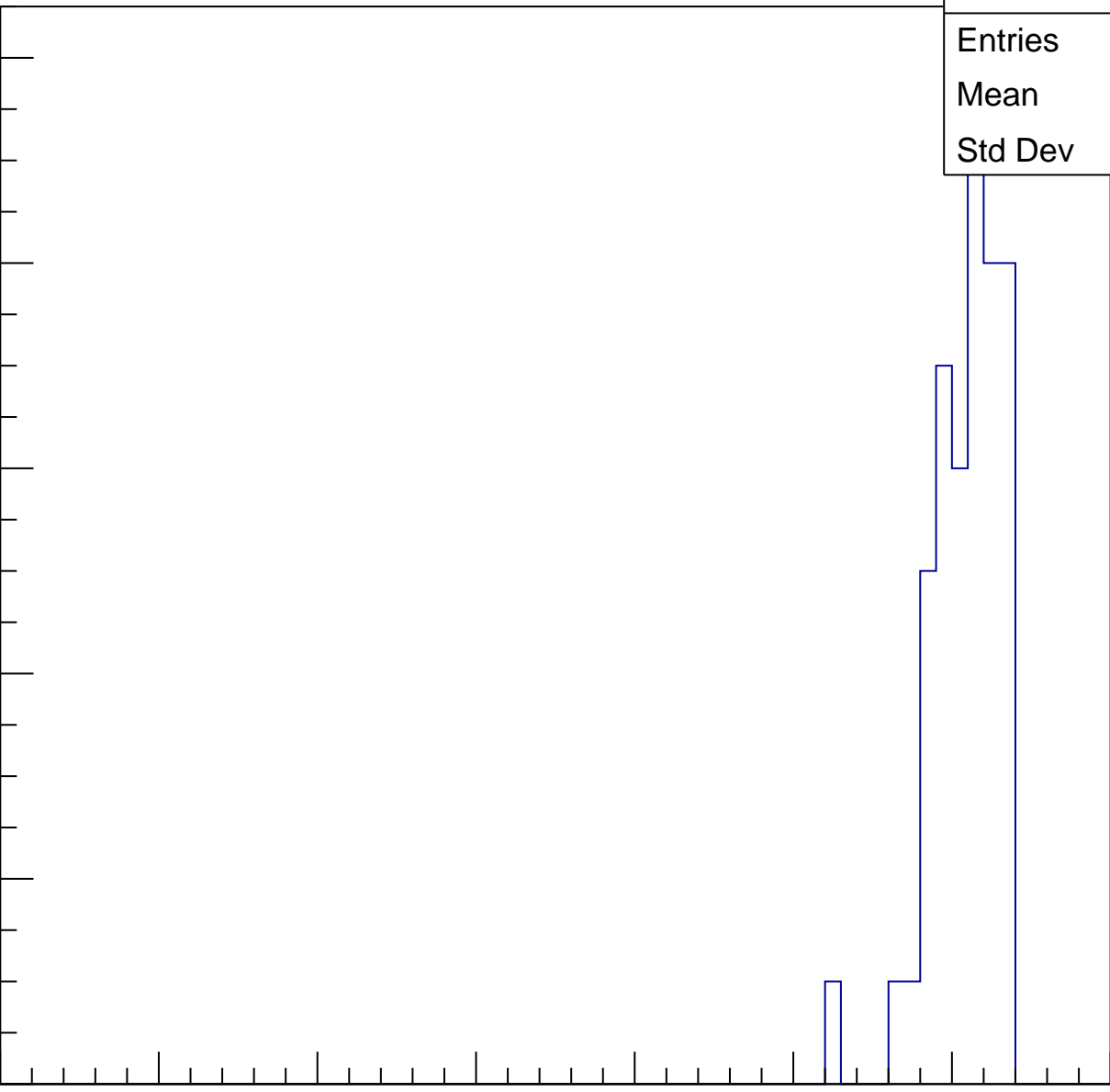
40

50

60

ampl

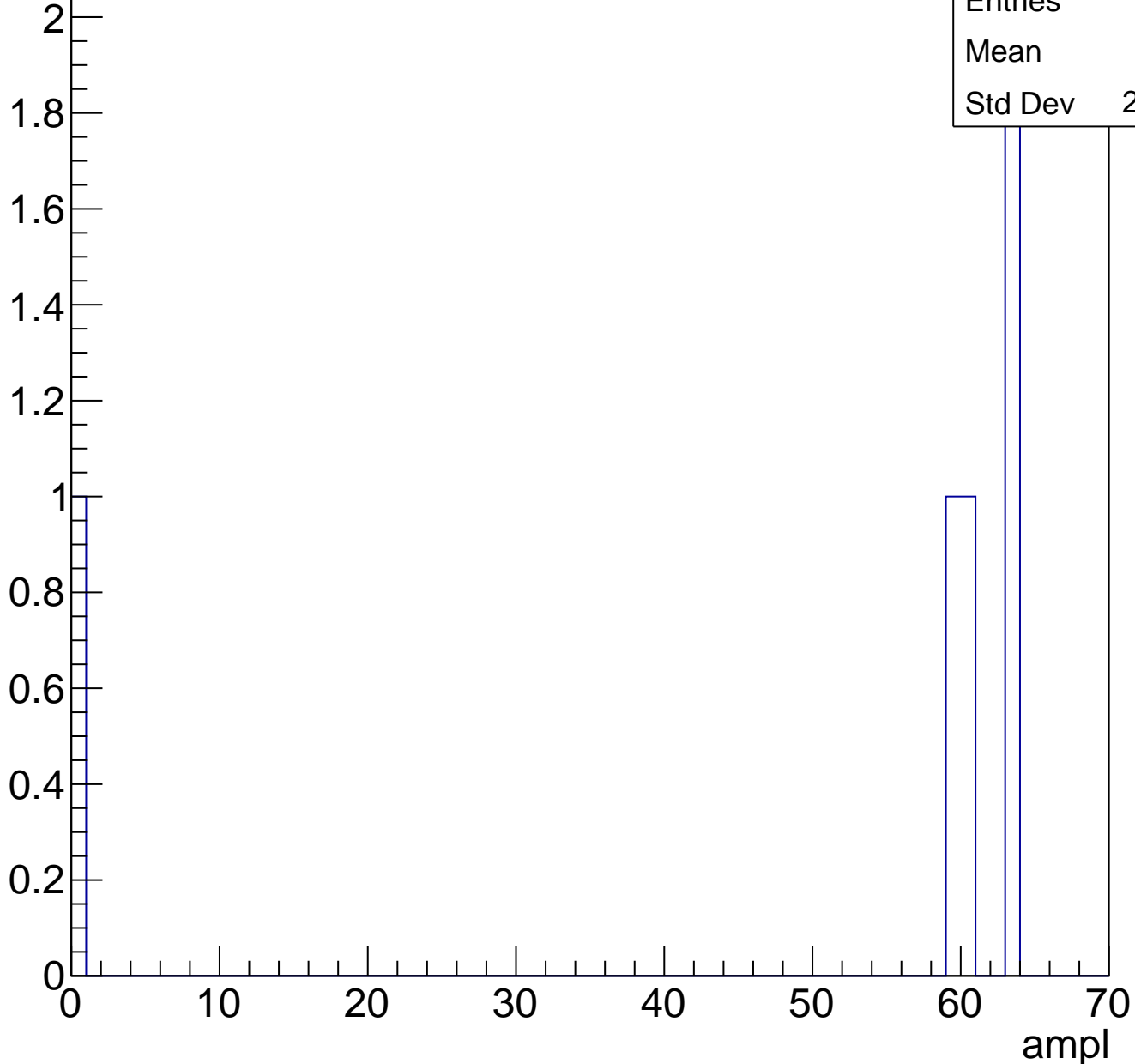
70



# B0L001S, U6-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U6-ch121, adc0

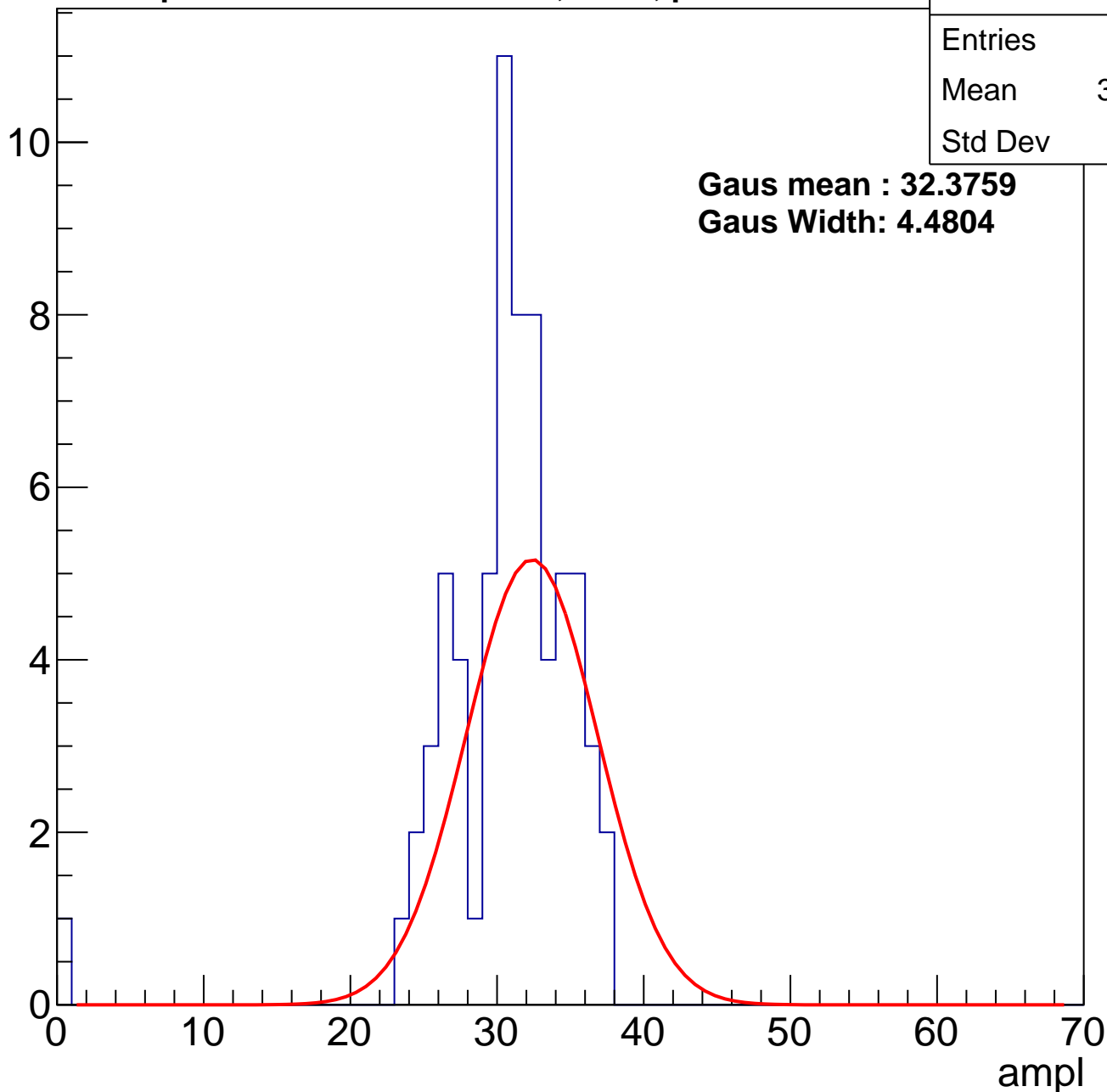
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	68
Mean	30.15
Std Dev	5.01

**Gaus mean : 32.3759**

**Gaus Width: 4.4804**

Entry

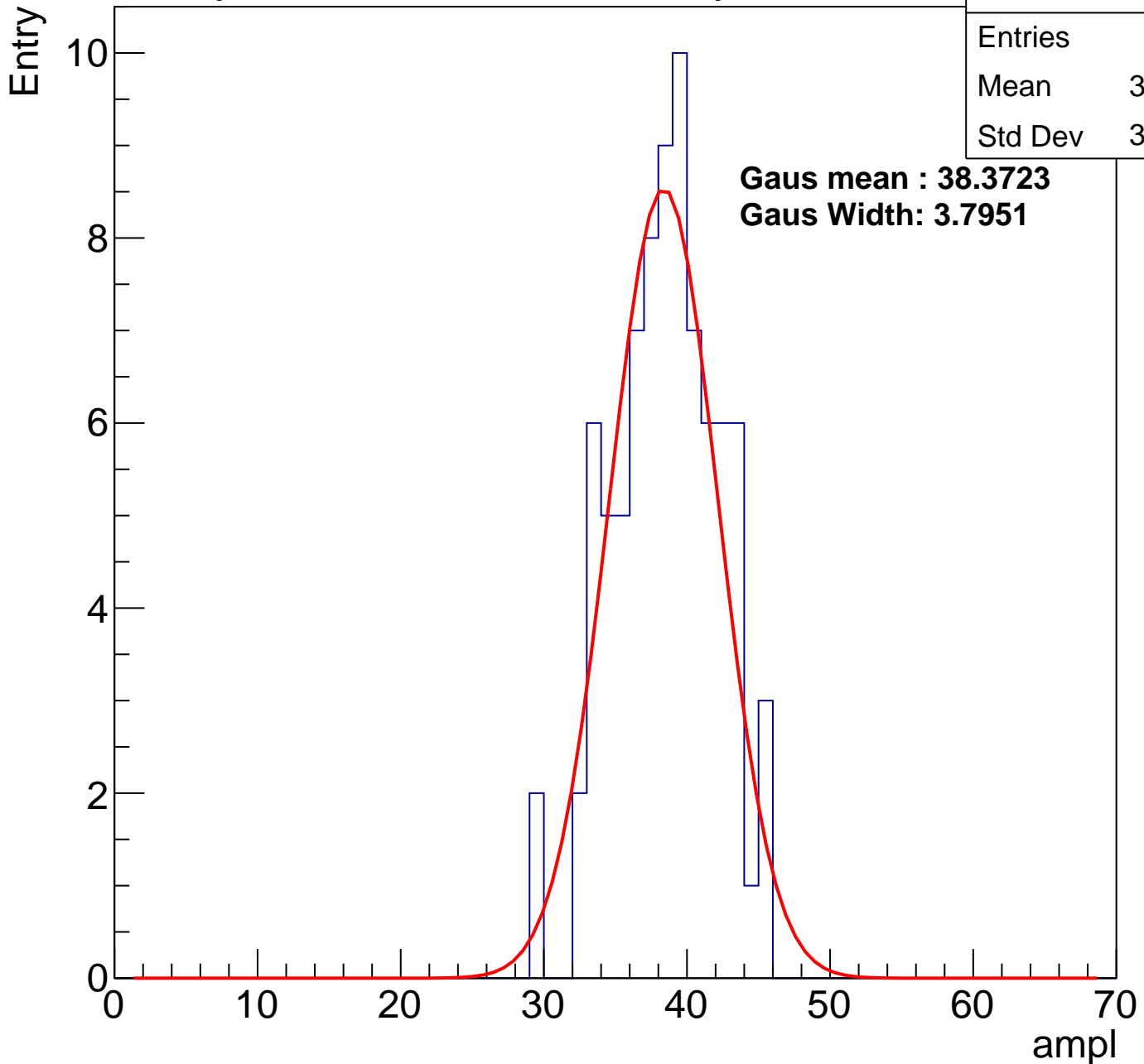


# B0L001S, U6-ch121, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	83
Mean	38.07
Std Dev	3.583

**Gaus mean : 38.3723**  
**Gaus Width: 3.7951**



# B0L001S, U6-ch121, adc2

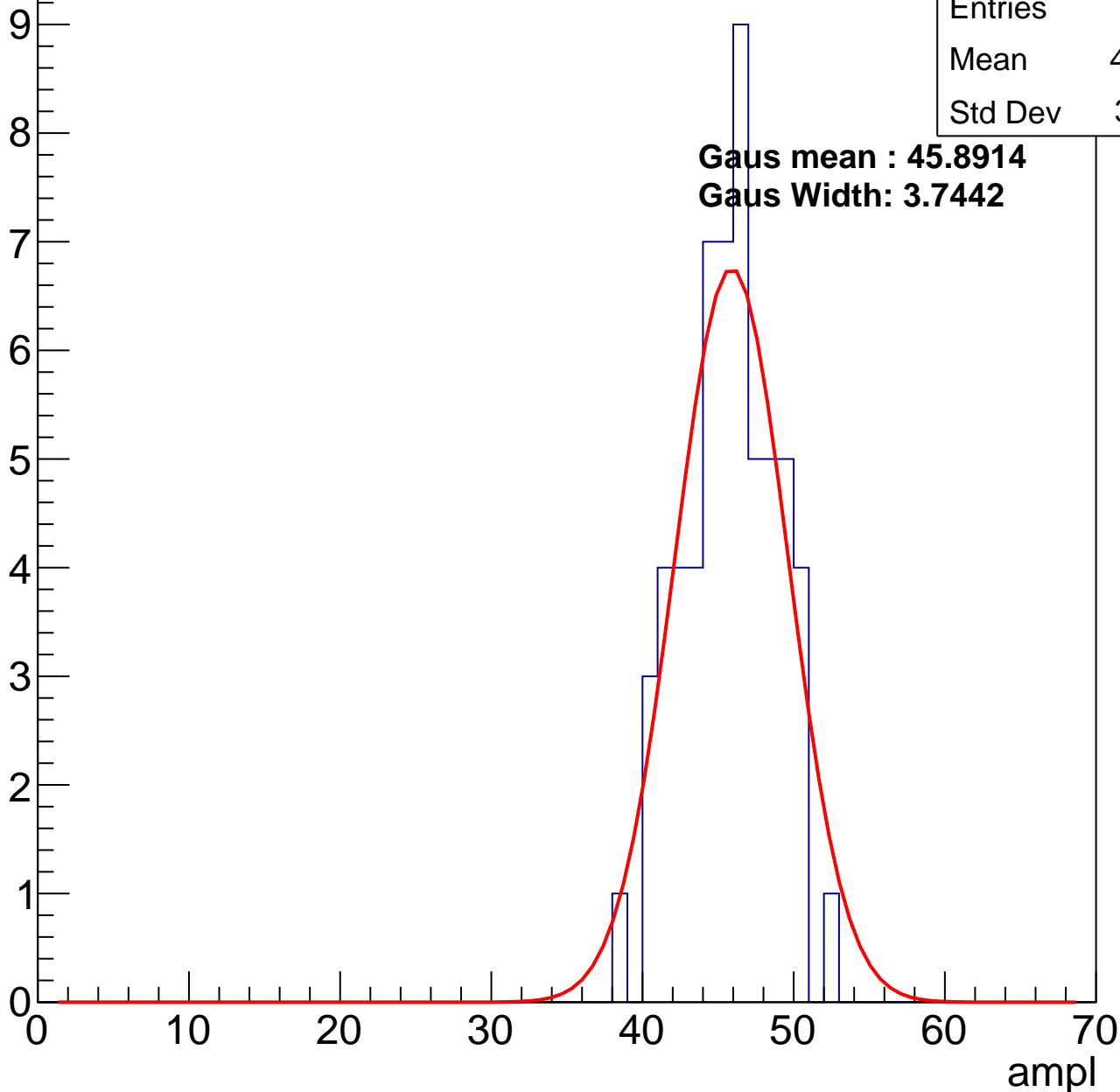
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	45.27
Std Dev	3.041

**Gaus mean : 45.8914**

**Gaus Width: 3.7442**

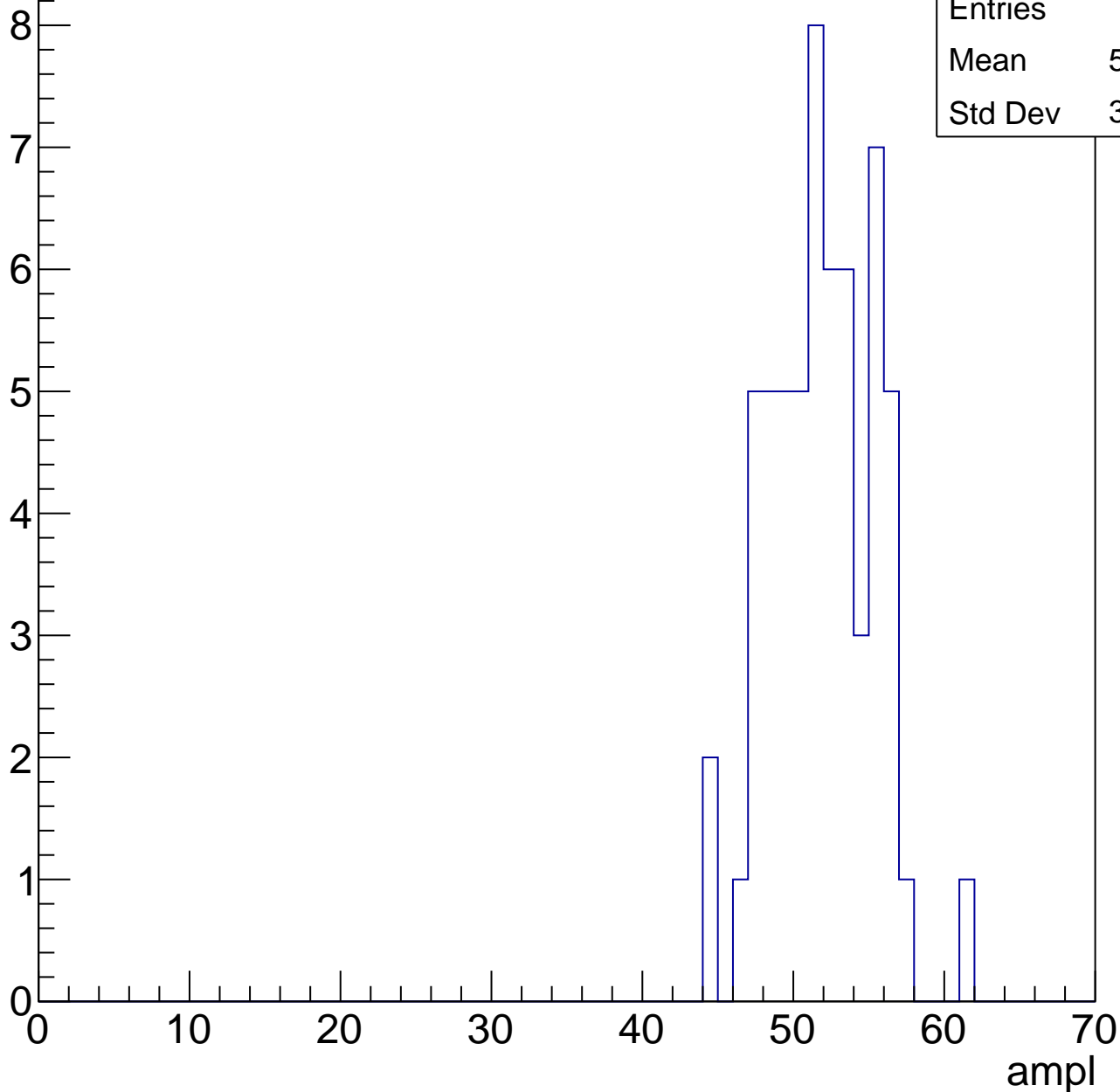


# B0L001S, U6-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	51.45
Std Dev	3.393

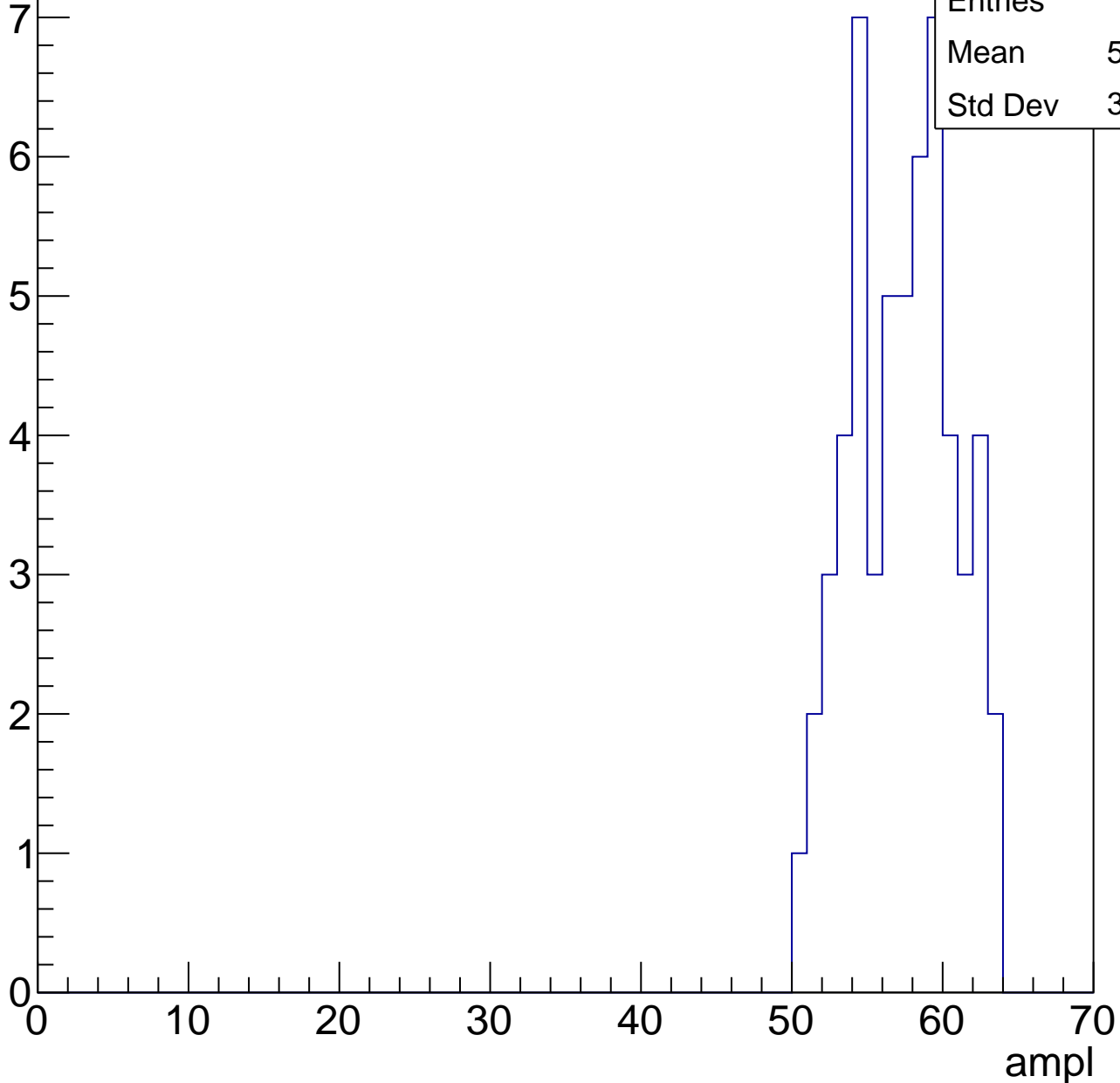


# B0L001S, U6-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	56.89
Std Dev	3.352

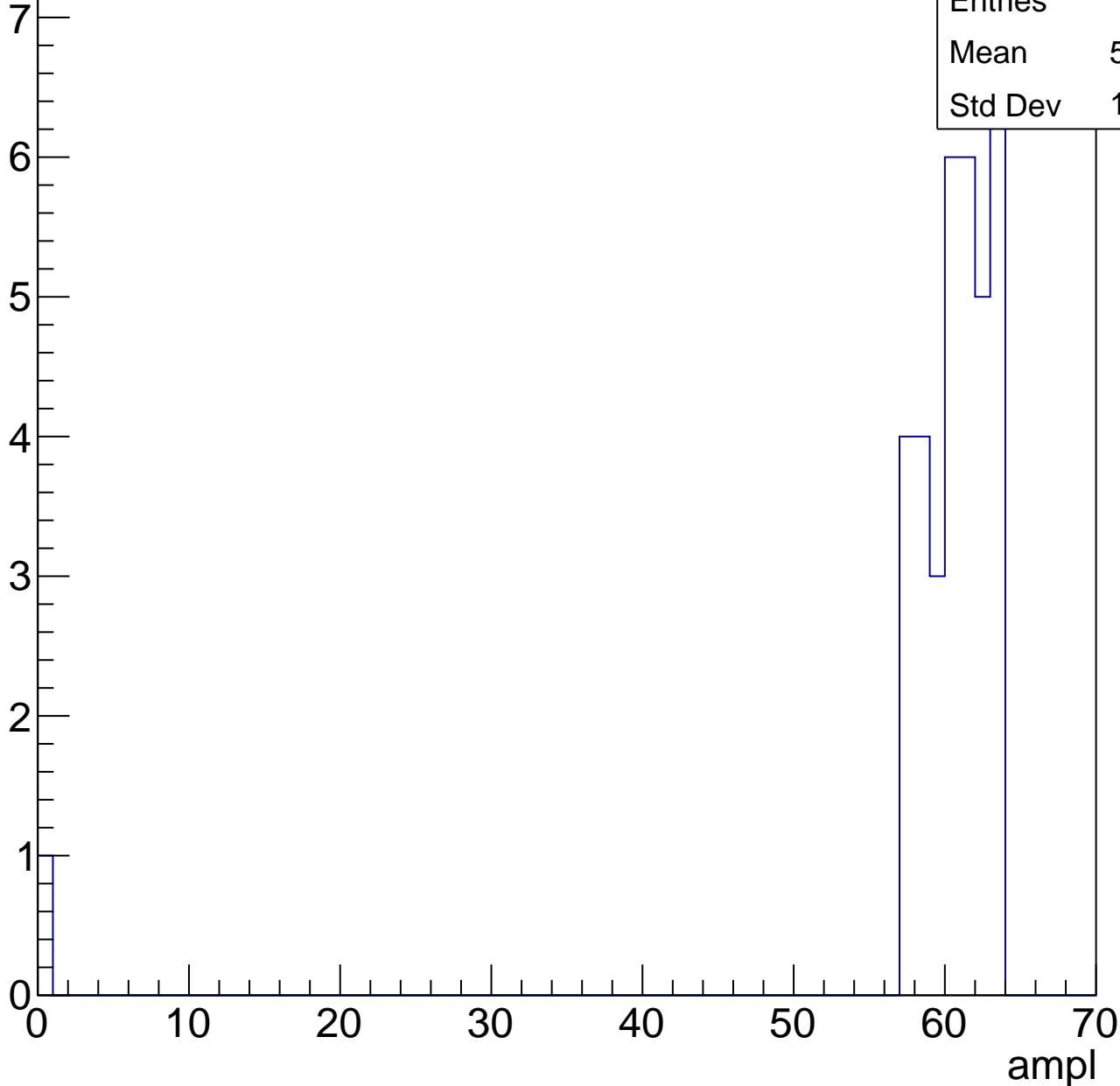


# B0L001S, U6-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	36
Mean	58.72
Std Dev	10.12



# B0L001S, U6-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U6-ch122, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	68
Mean	29.94
Std Dev	5.119

**Gaus mean : 31.0306**

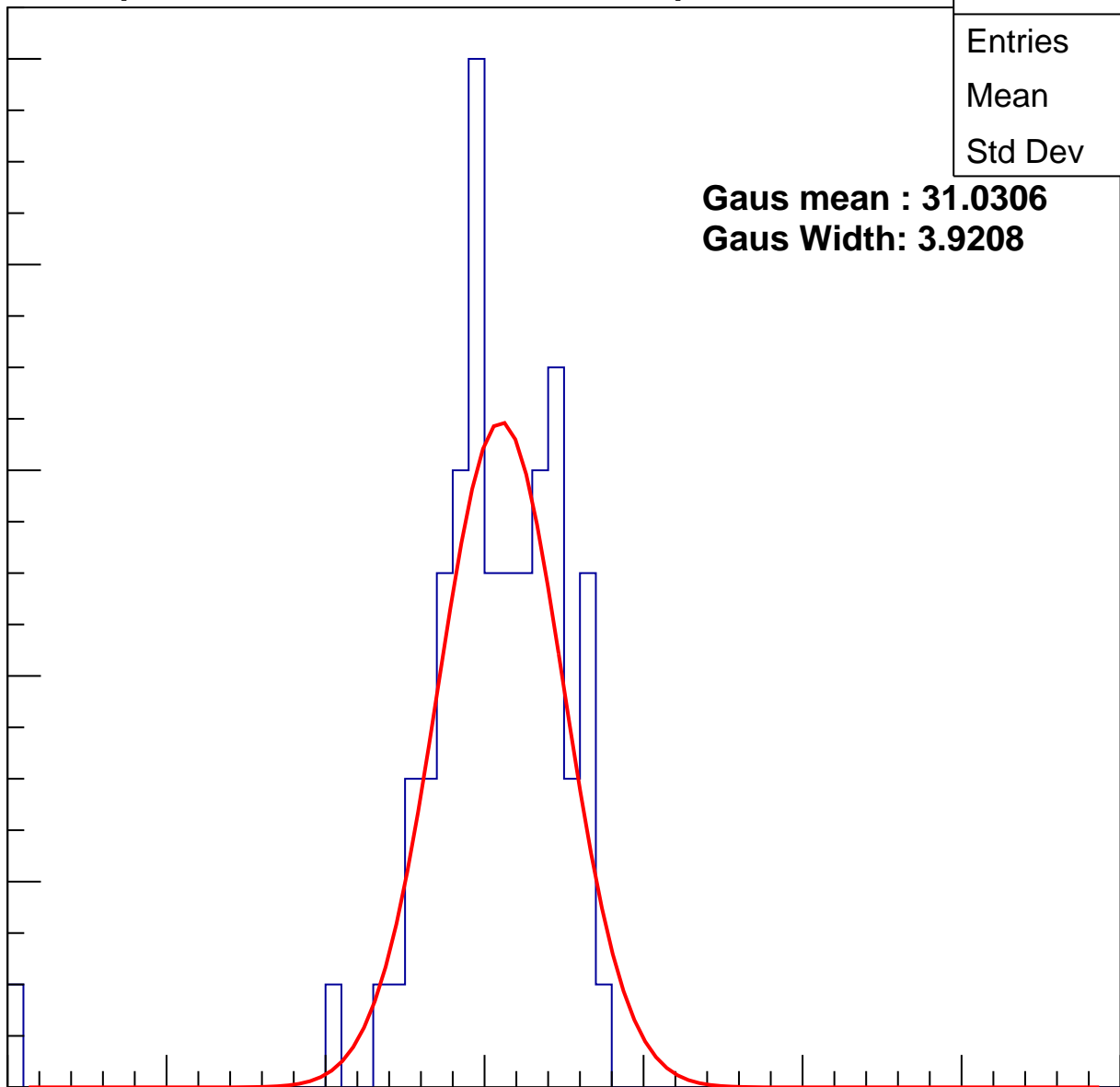
**Gaus Width: 3.9208**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U6-ch122, adc1

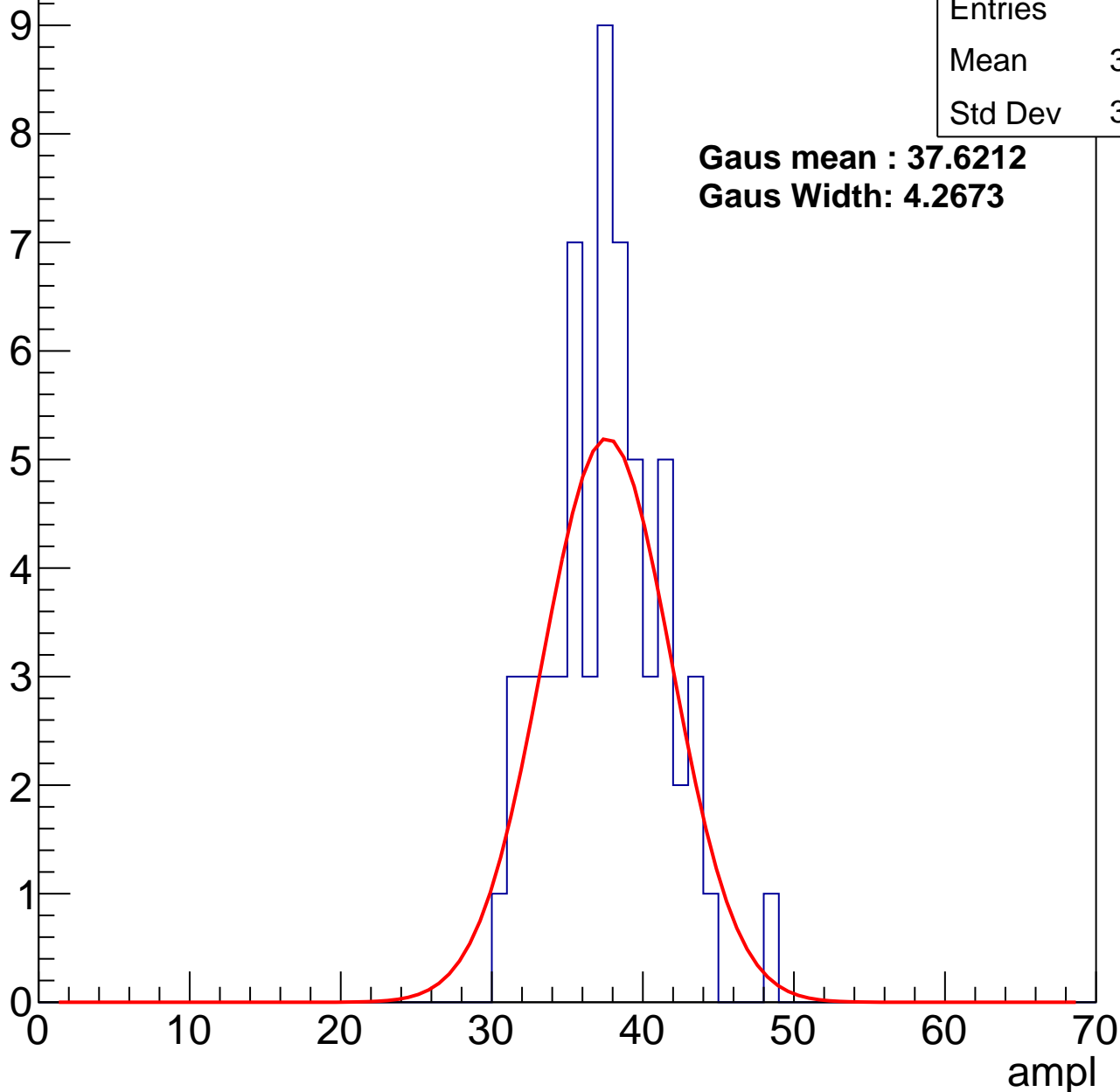
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	37.24
Std Dev	3.675

**Gaus mean : 37.6212**

**Gaus Width: 4.2673**



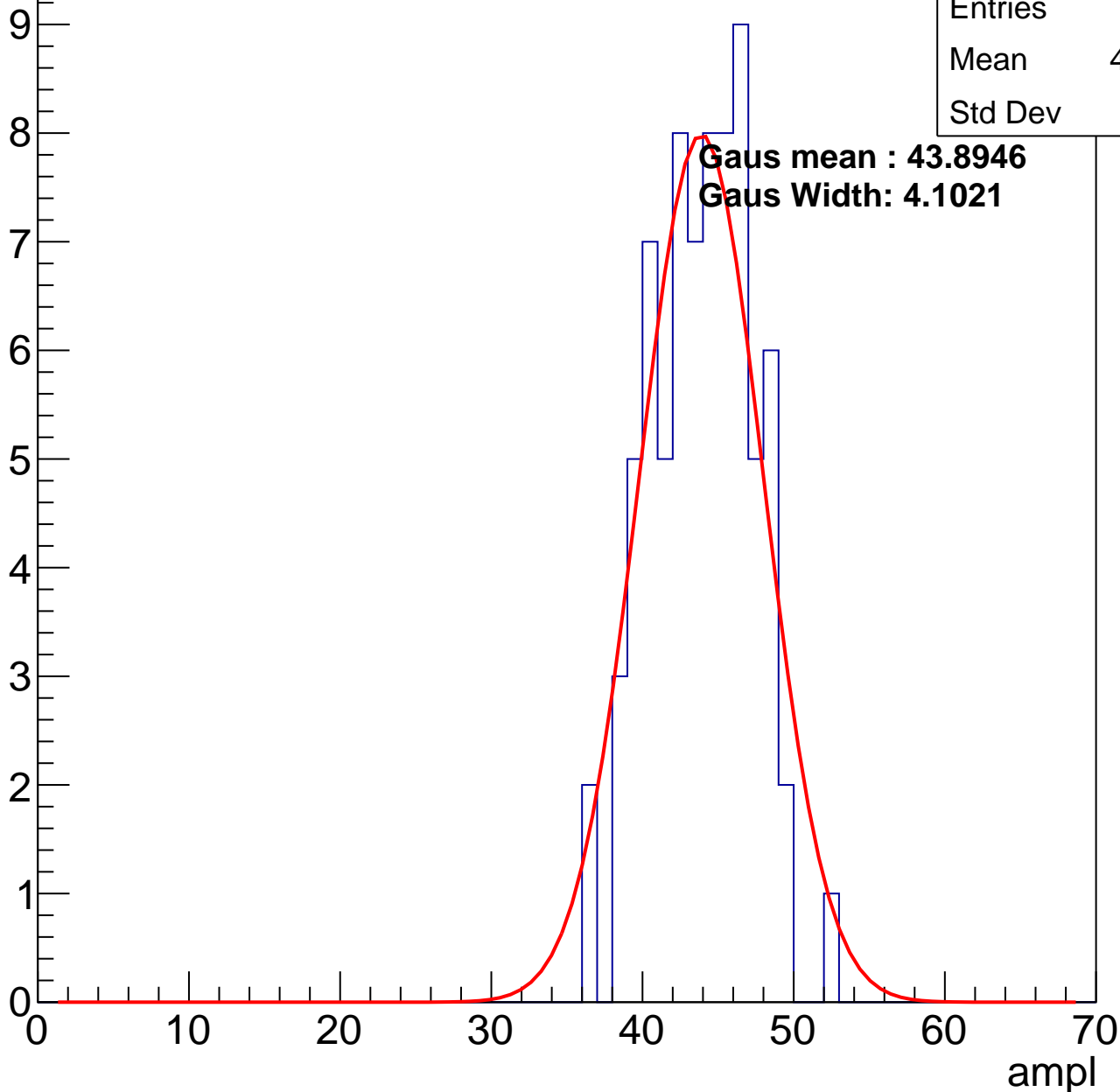
# B0L001S, U6-ch122, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	43.45
Std Dev	3.31

**Gaus mean : 43.8946**  
**Gaus Width: 4.1021**

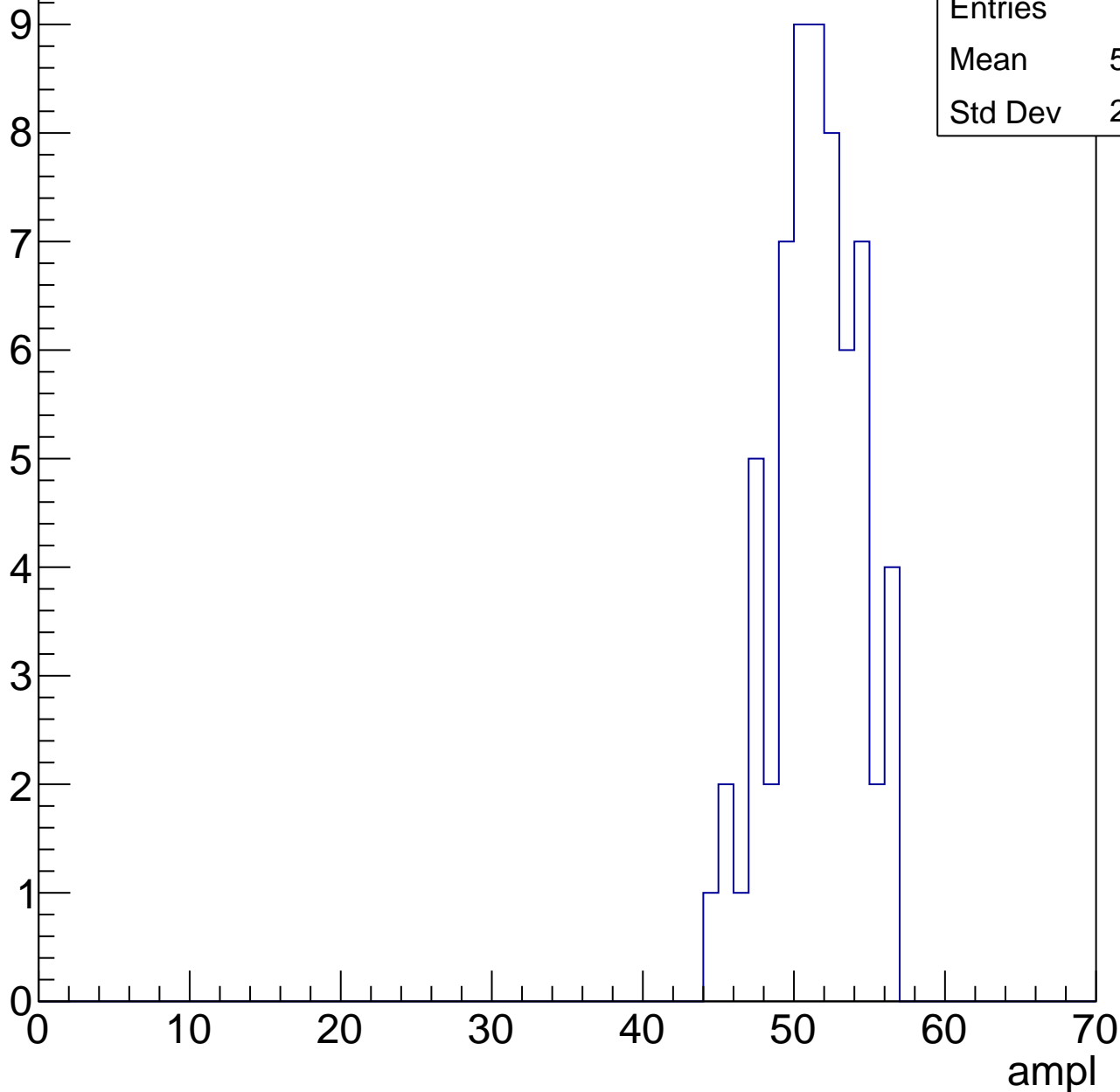


# B0L001S, U6-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

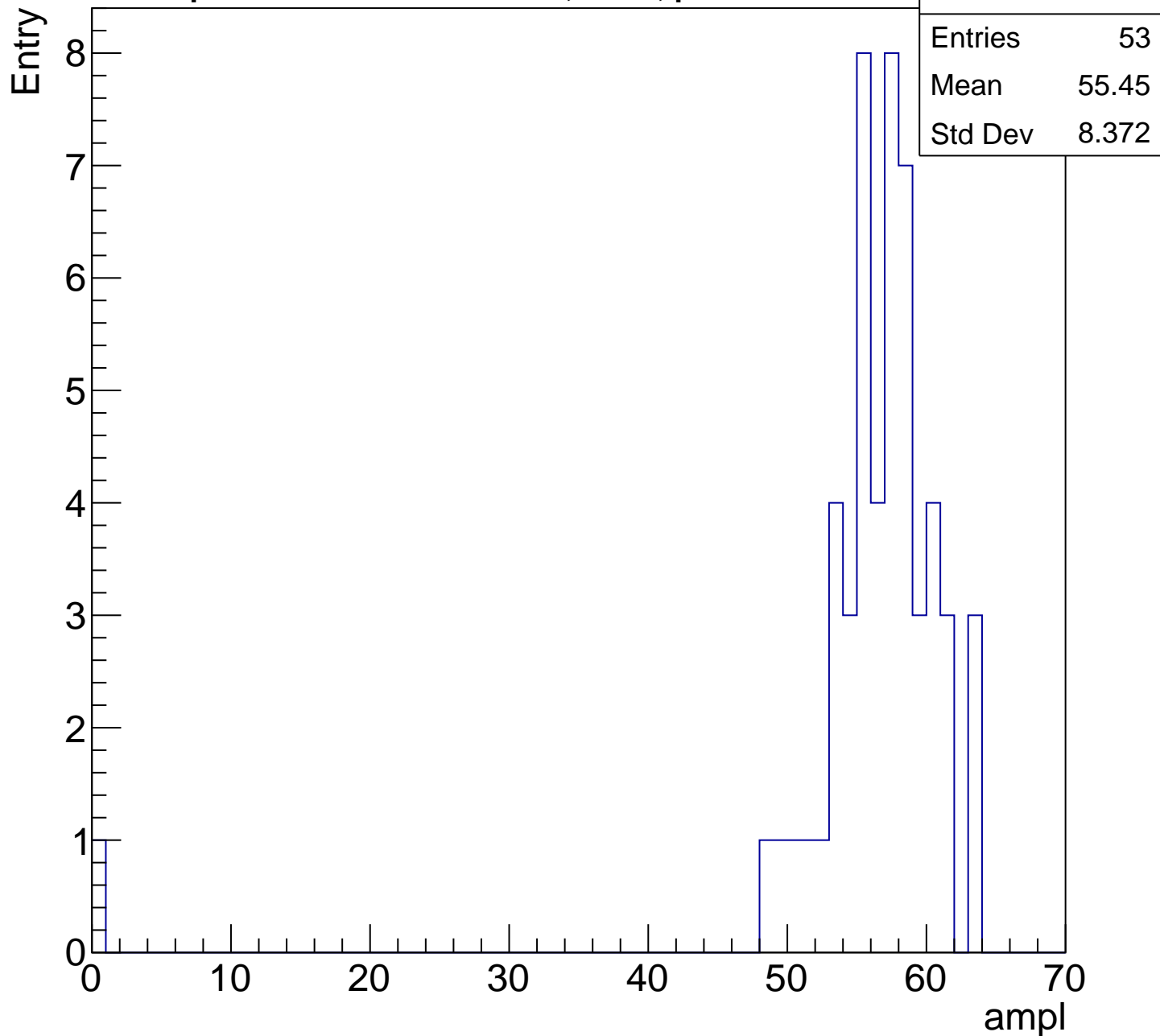
Entry

Entries	63
Mean	50.94
Std Dev	2.839



# B0L001S, U6-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

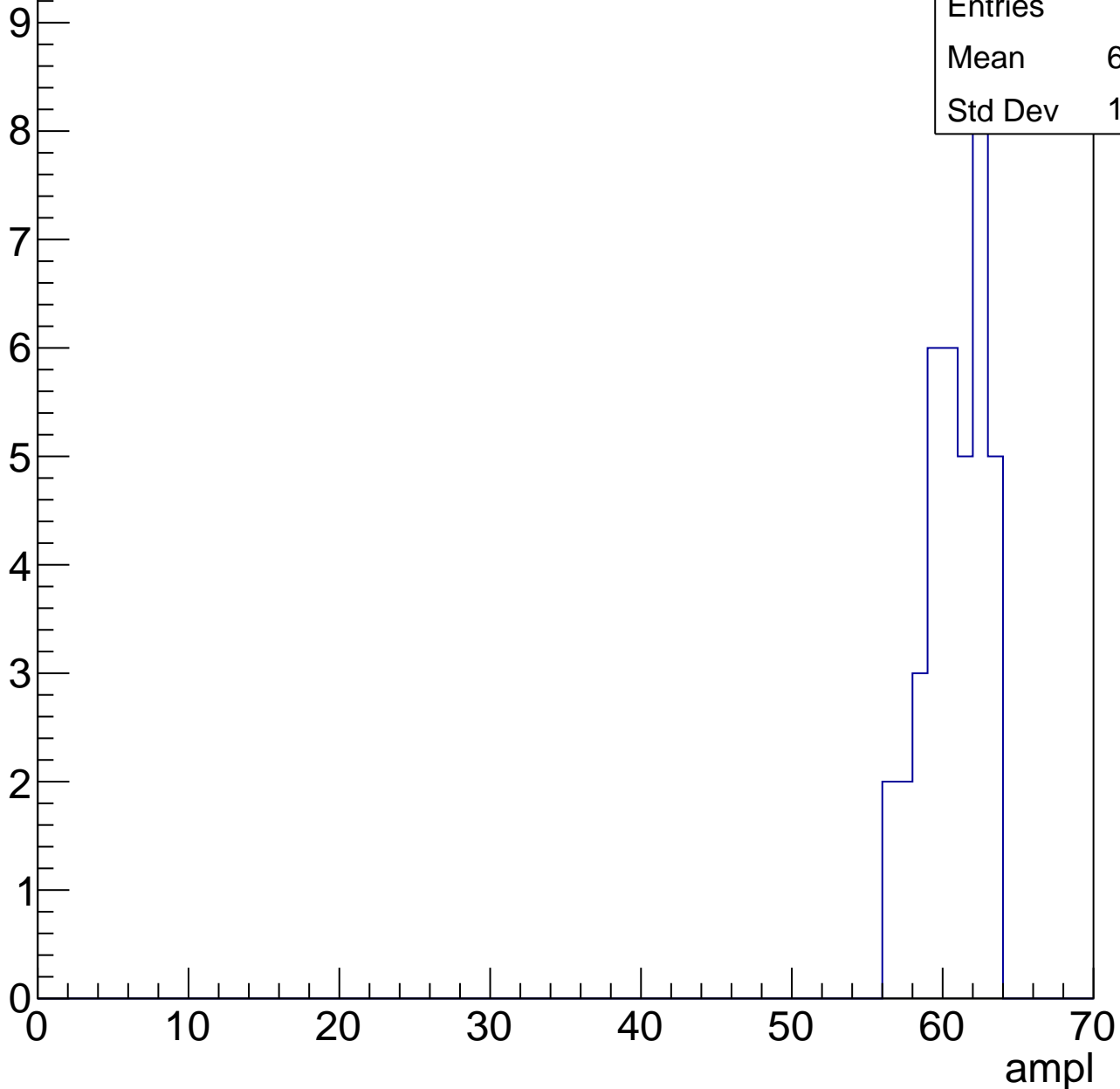


# B0L001S, U6-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

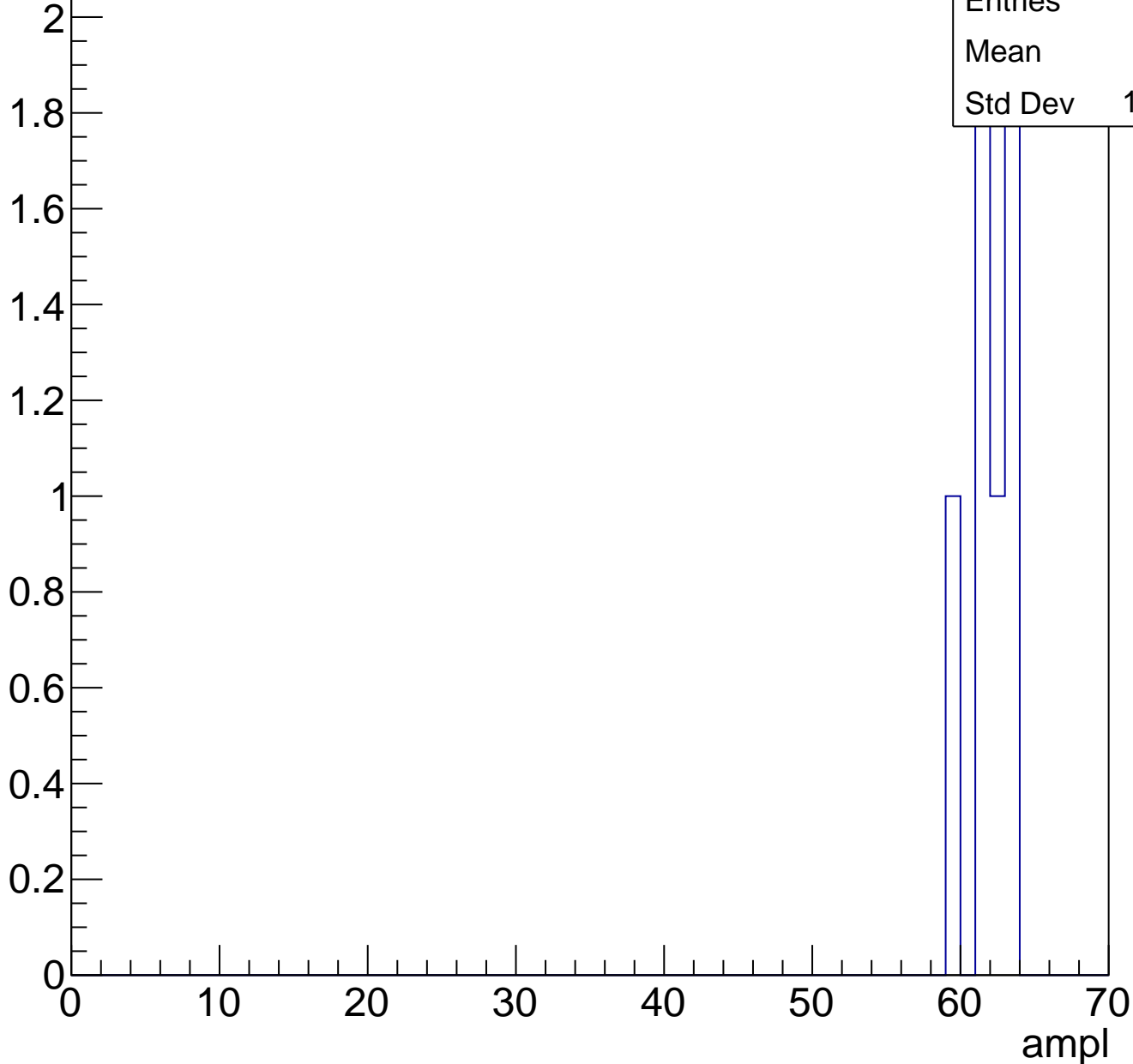
Entries	38
Mean	60.32
Std Dev	1.988



# B0L001S, U6-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch123, adc0

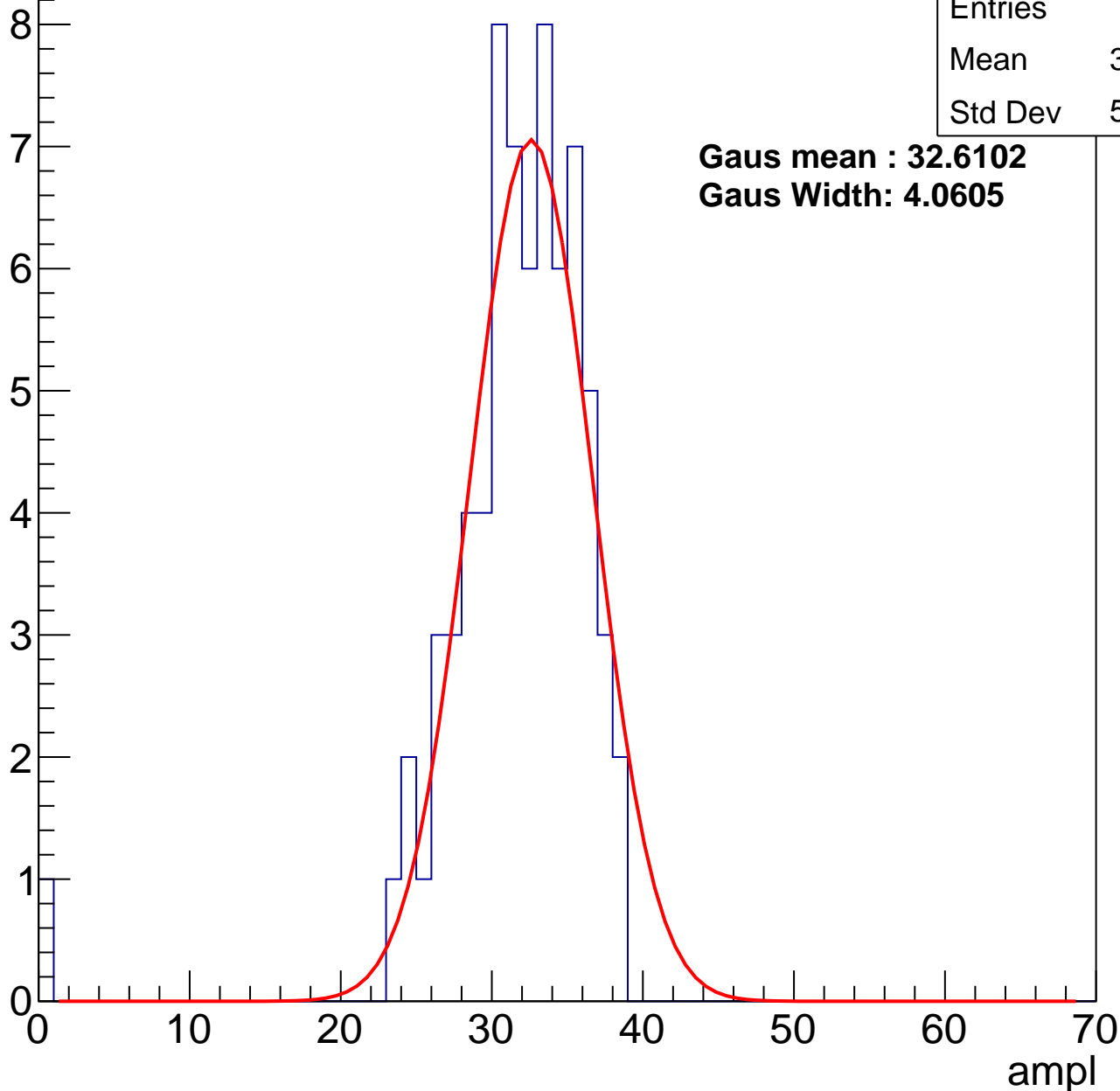
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	31.15
Std Dev	5.139

**Gaus mean : 32.6102**

**Gaus Width: 4.0605**



# B0L001S, U6-ch123, adc1

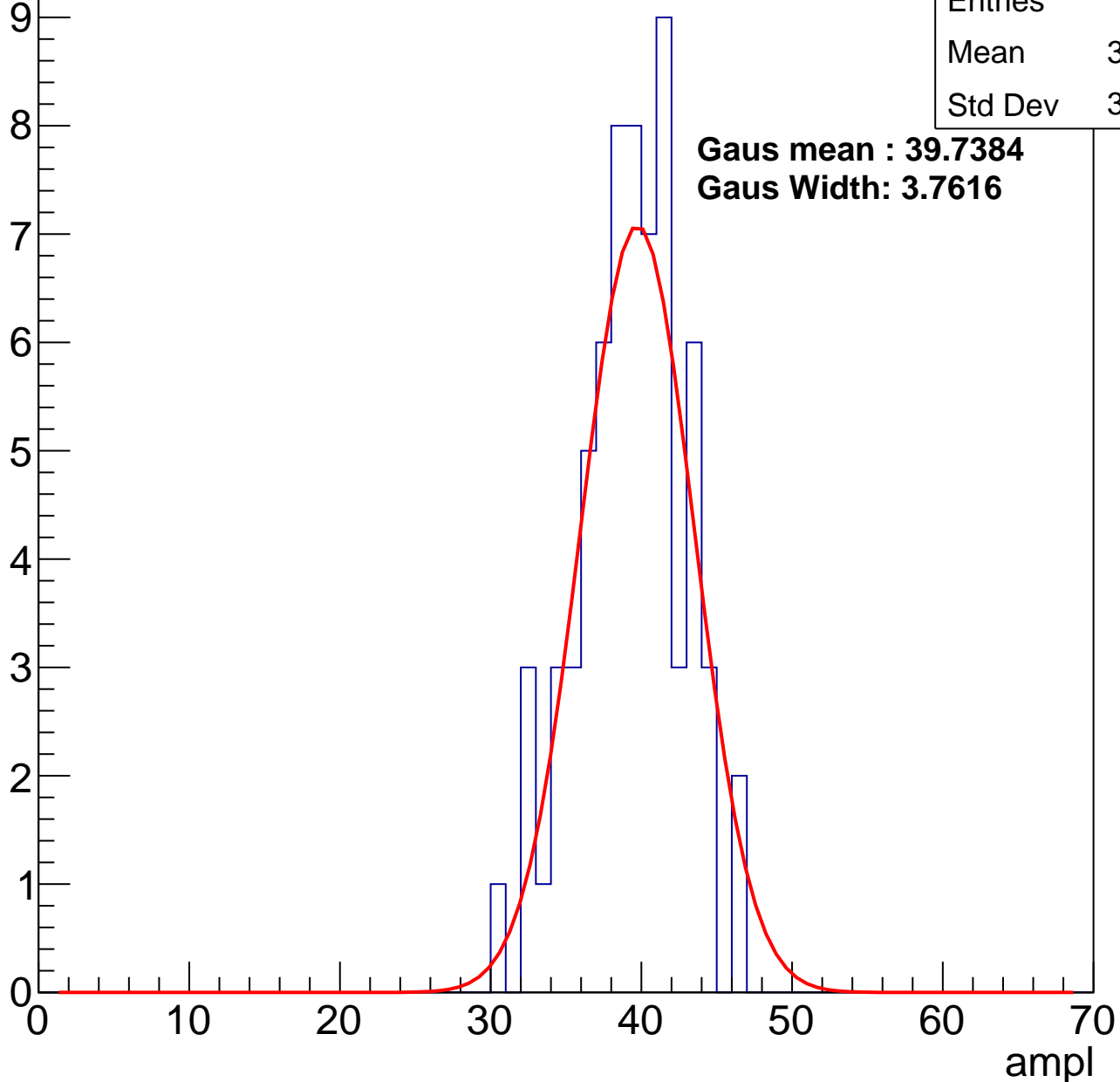
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	38.84
Std Dev	3.433

**Gaus mean : 39.7384**

**Gaus Width: 3.7616**



# B0L001S, U6-ch123, adc2

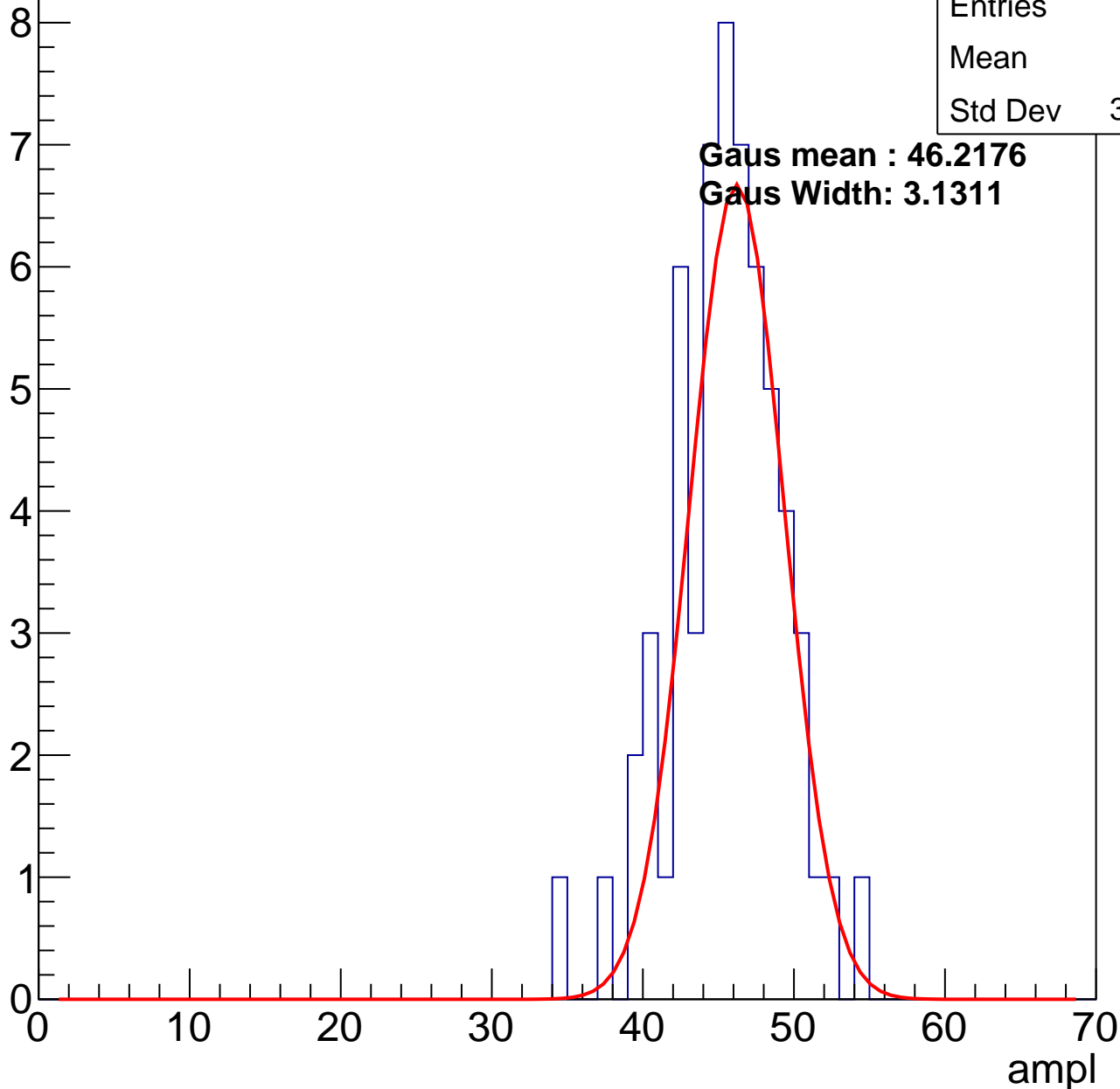
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	45.1
Std Dev	3.655

**Gaus mean : 46.2176**

**Gaus Width: 3.1311**

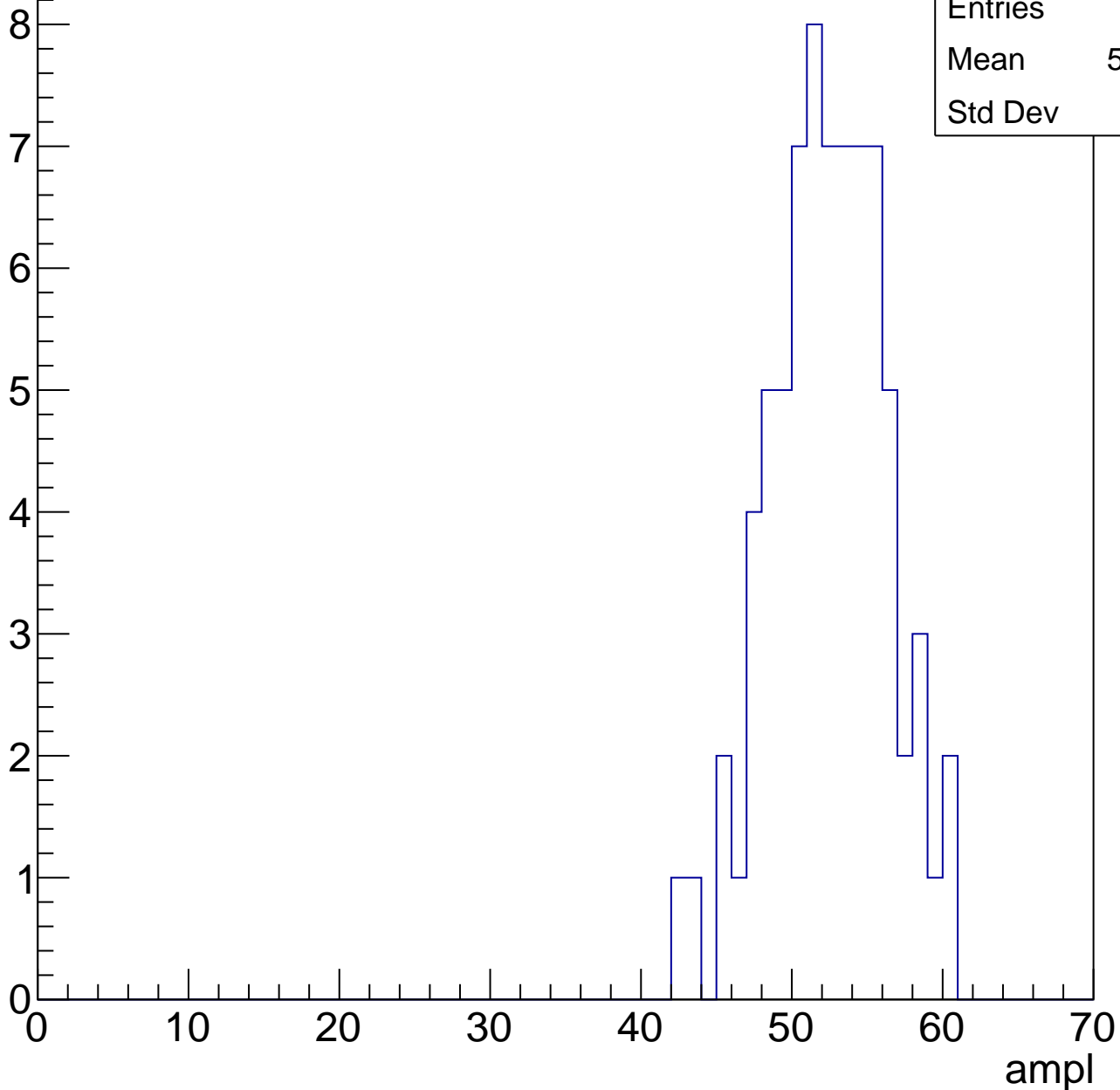


# B0L001S, U6-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

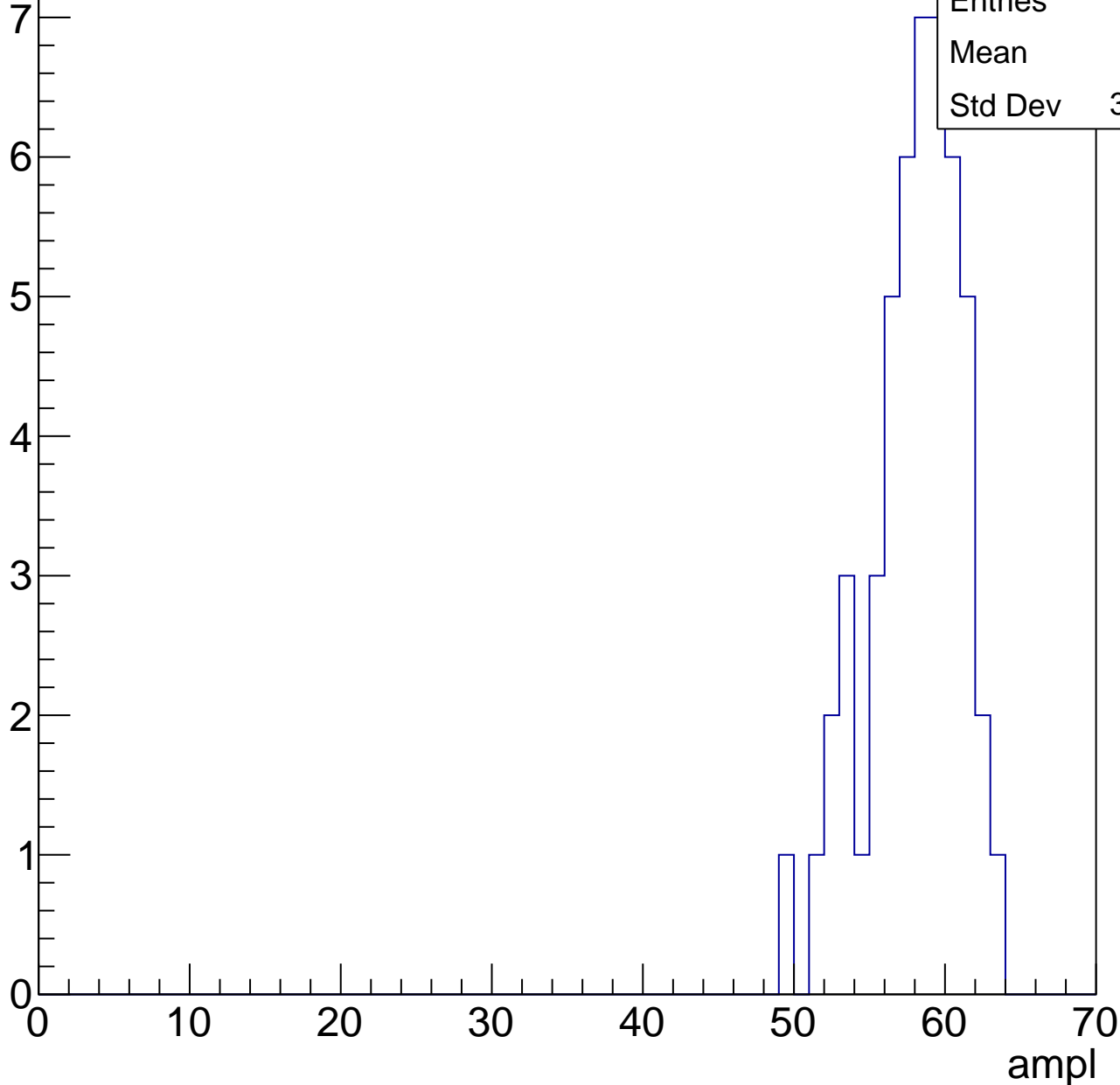
Entries	75
Mean	51.96
Std Dev	3.81



# B0L001S, U6-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



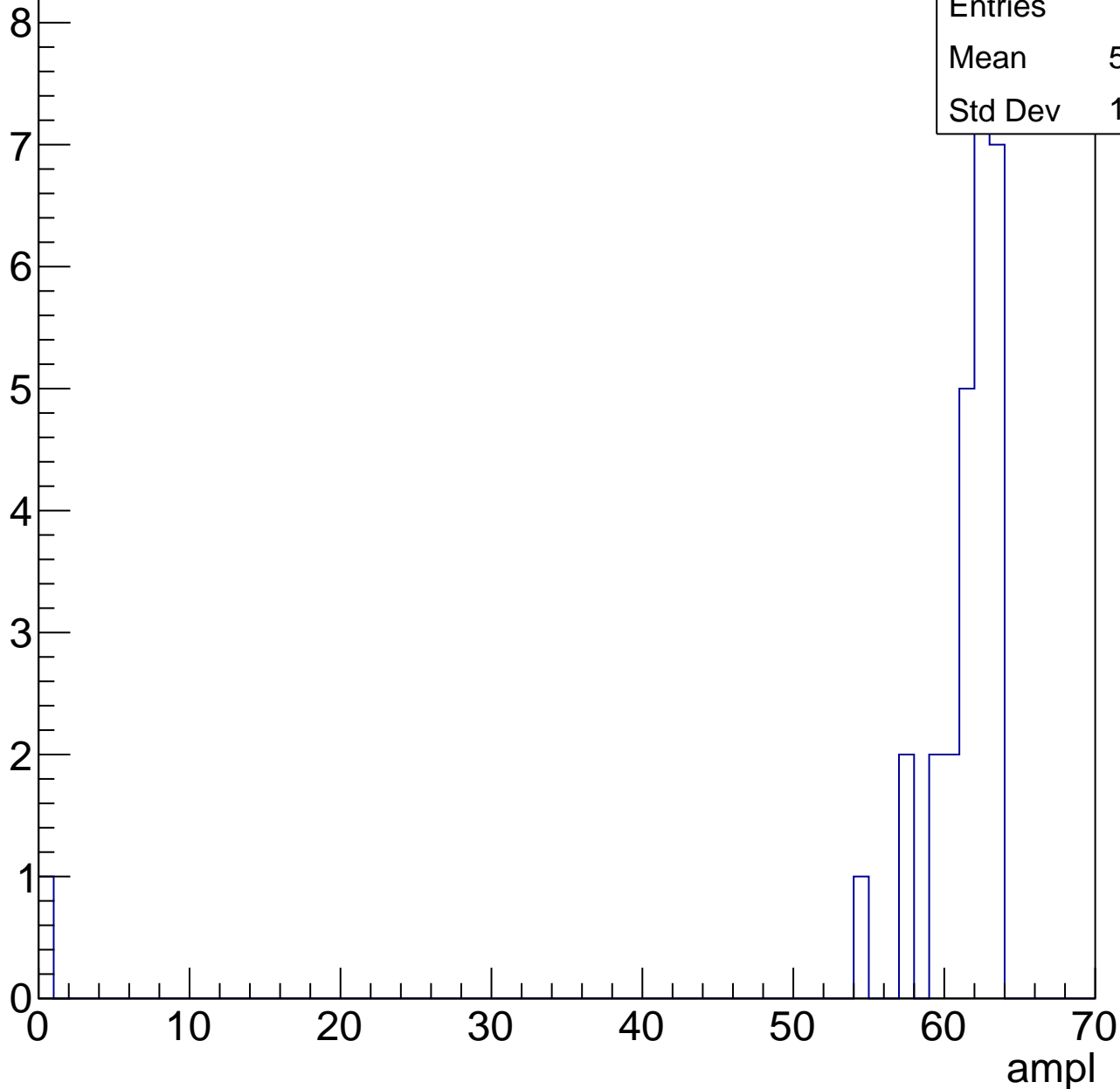
Entries	50
Mean	57.5
Std Dev	3.055

# B0L001S, U6-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	28
Mean	58.86
Std Dev	11.53



# B0L001S, U6-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

ampl



# B0L001S, U6-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch124, adc0

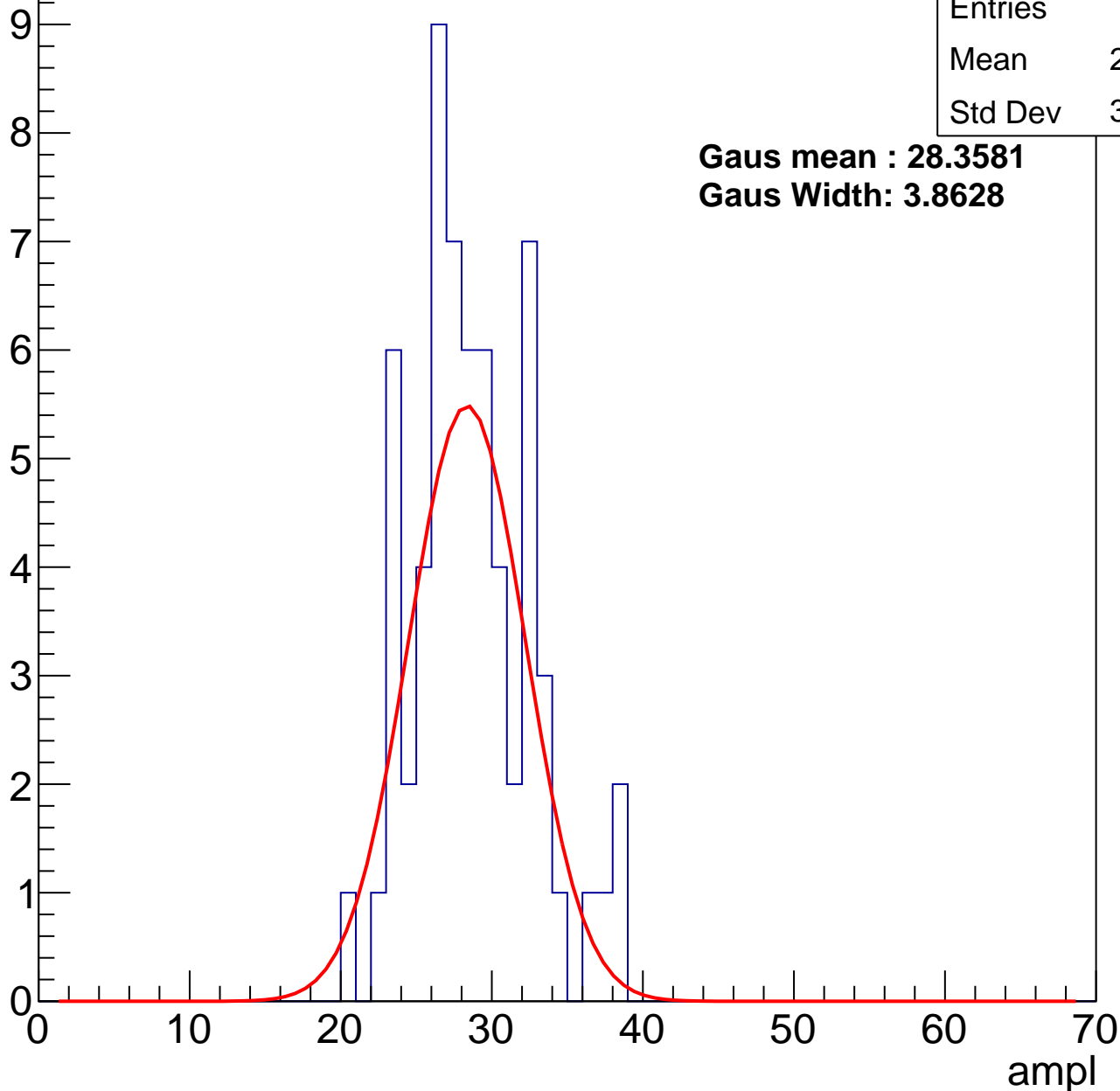
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	28.27
Std Dev	3.913

**Gaus mean : 28.3581**

**Gaus Width: 3.8628**



# B0L001S, U6-ch124, adc1

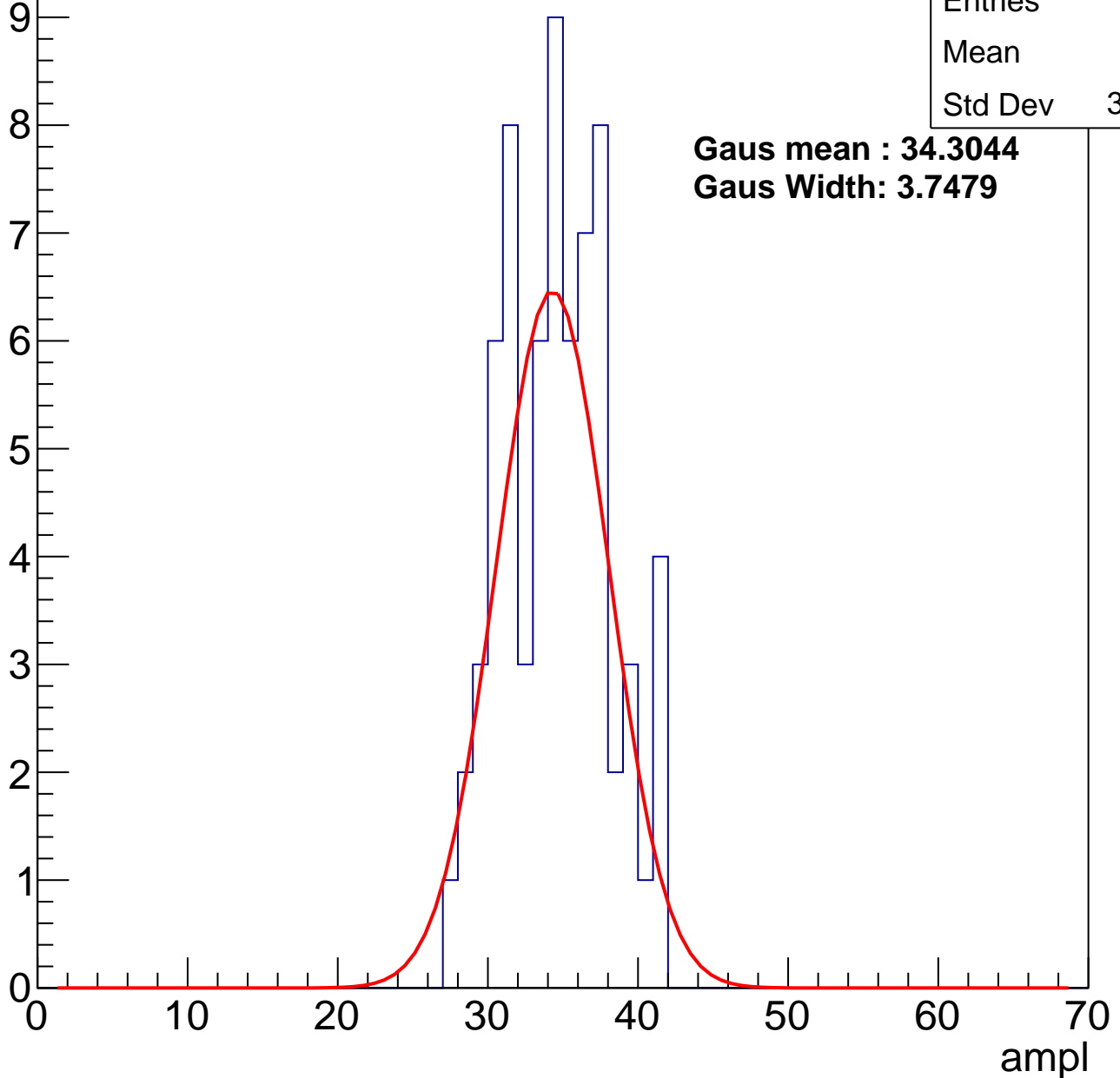
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	34.1
Std Dev	3.461

**Gaus mean : 34.3044**

**Gaus Width: 3.7479**



# B0L001S, U6-ch124, adc2

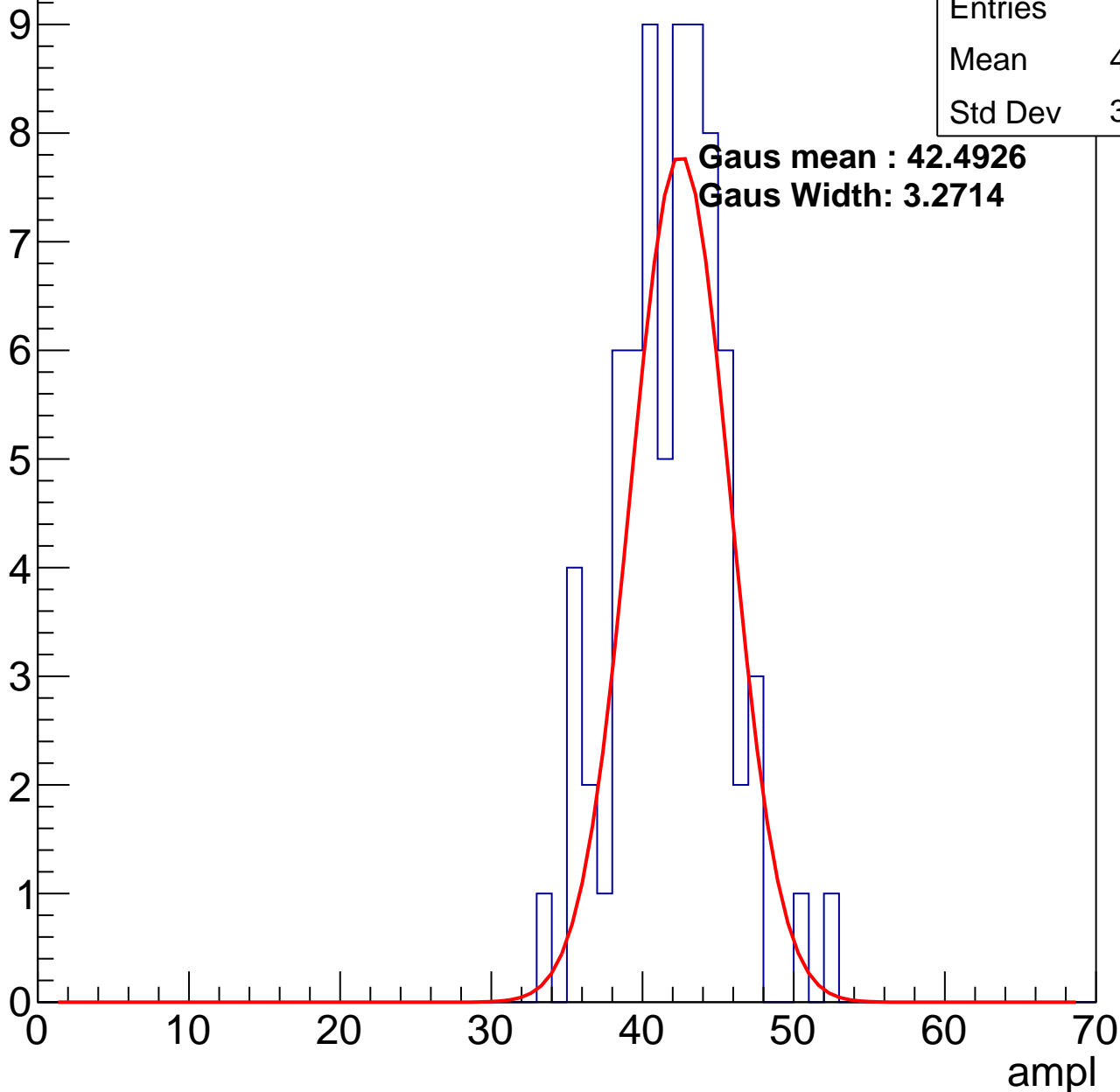
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	41.52
Std Dev	3.539

**Gaus mean : 42.4926**

**Gaus Width: 3.2714**

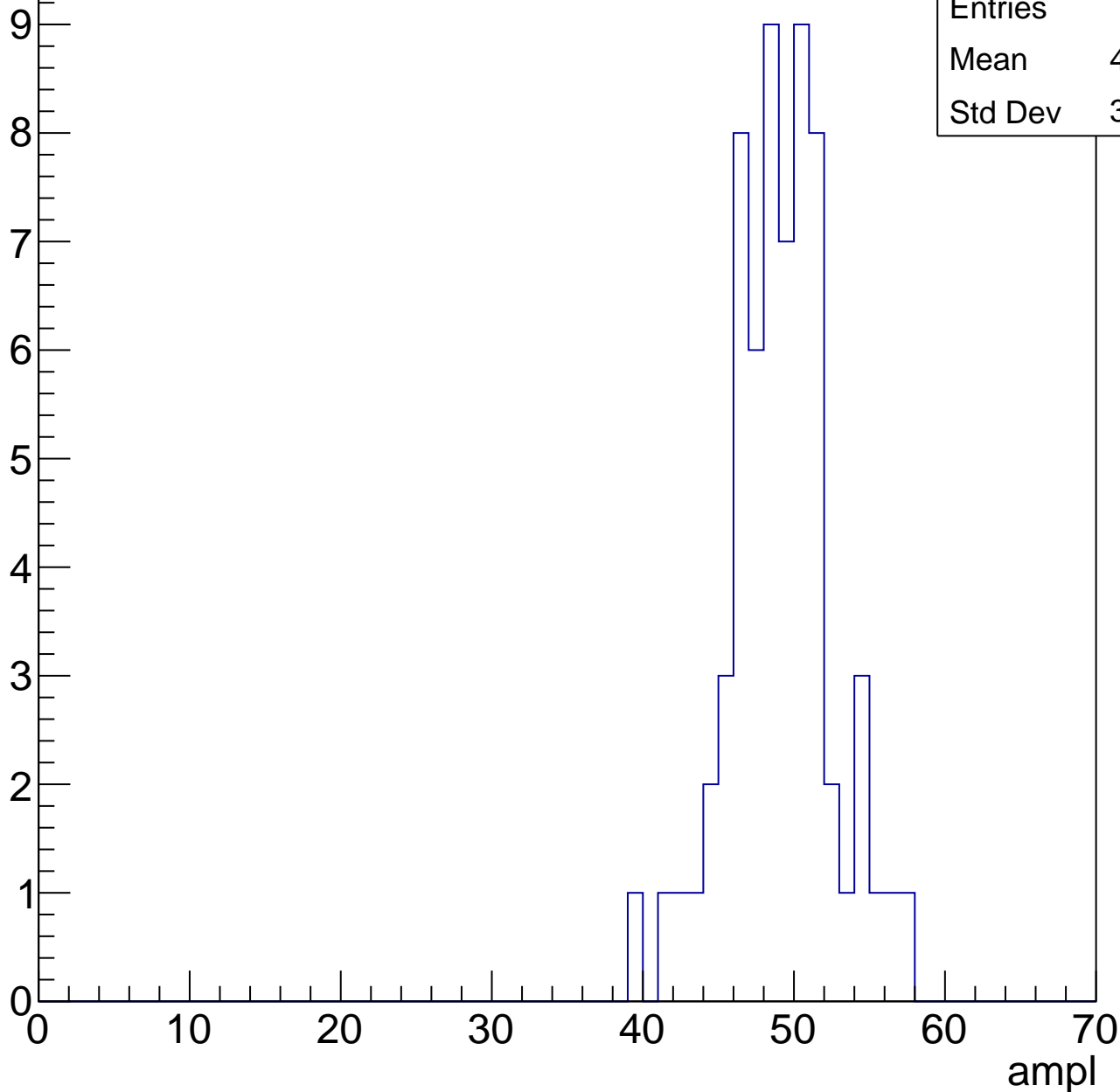


# B0L001S, U6-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	48.58
Std Dev	3.374

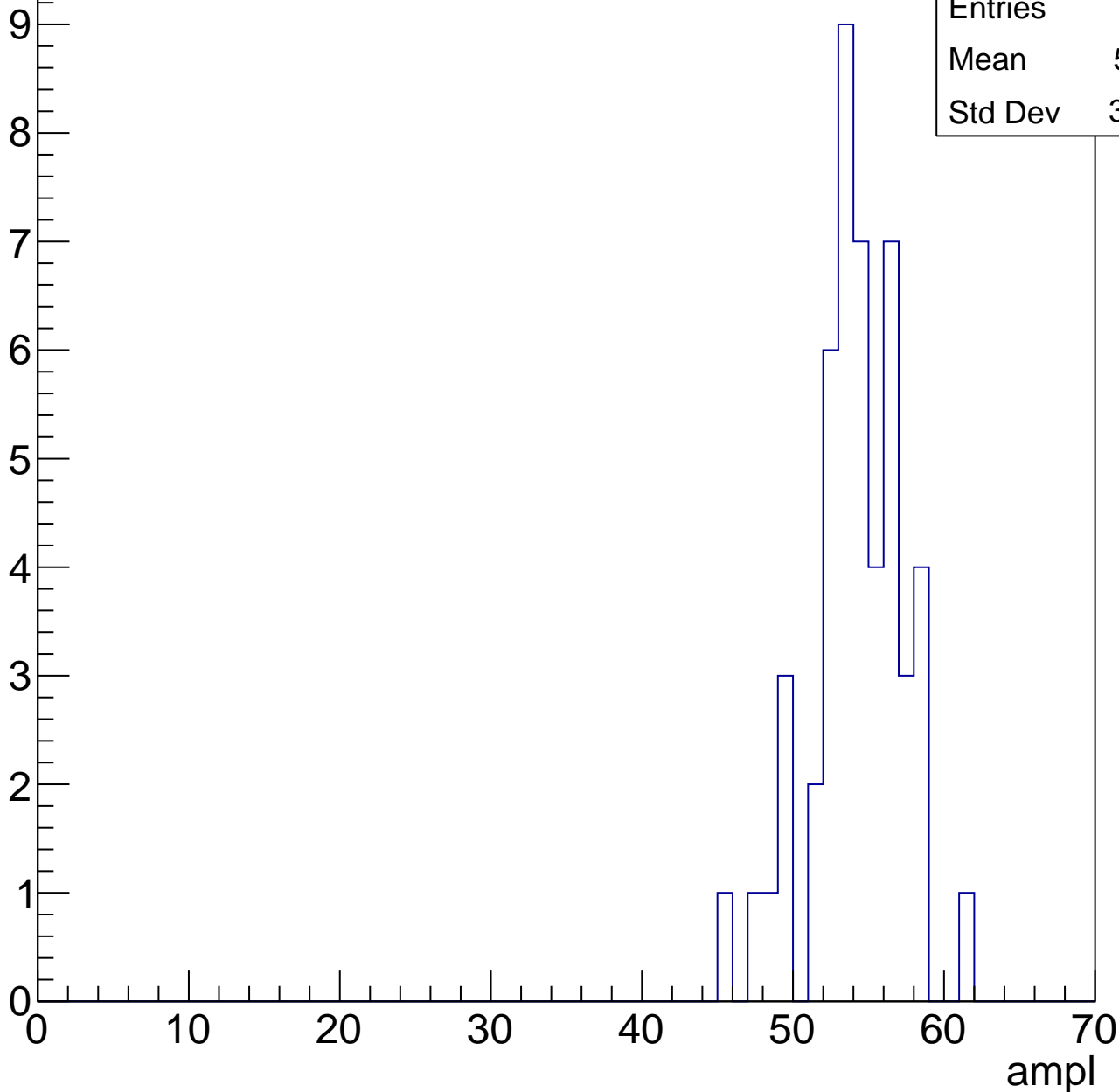


# B0L001S, U6-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	53.71
Std Dev	3.064

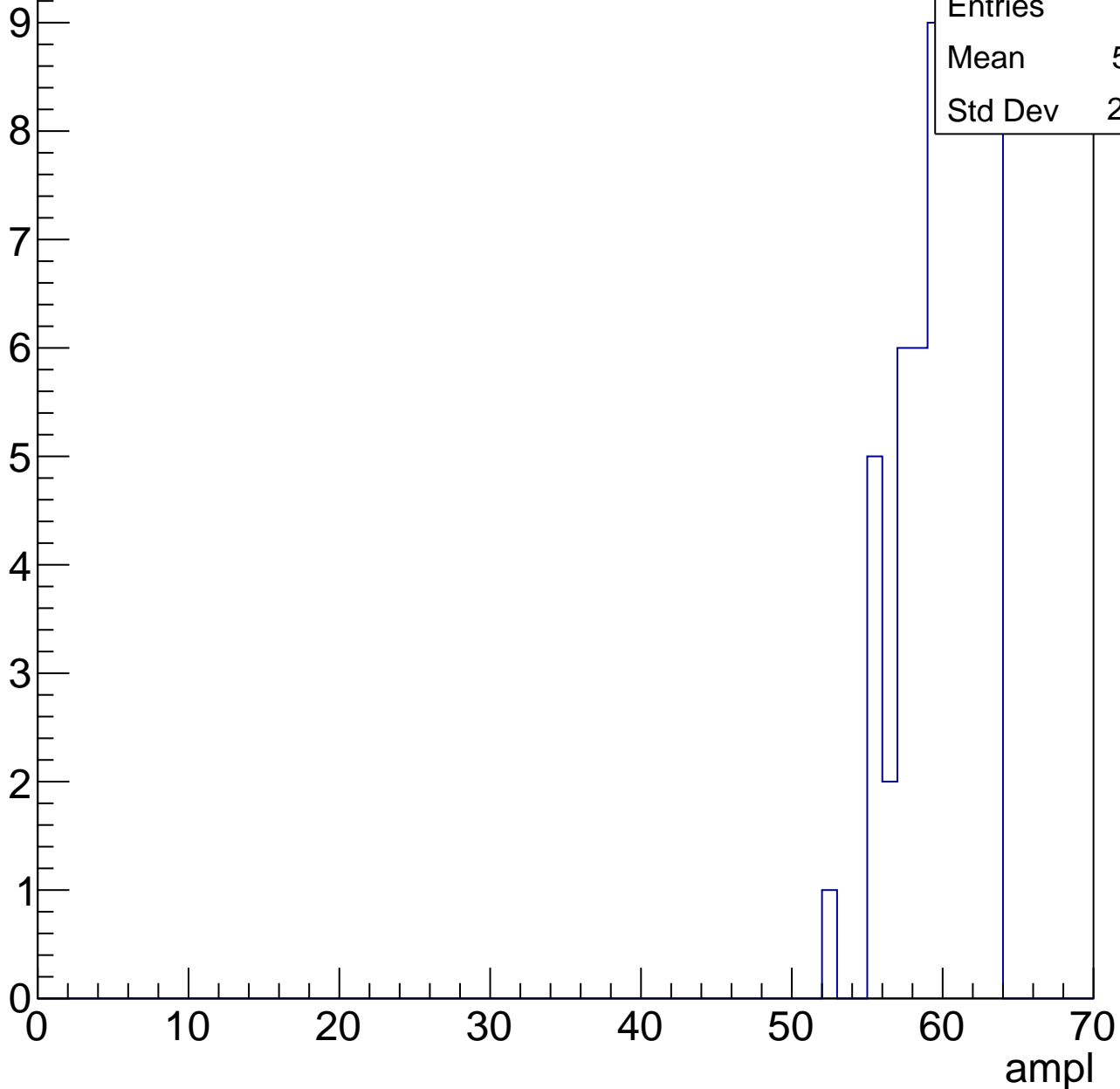


# B0L001S, U6-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	59.51
Std Dev	2.538



# B0L001S, U6-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

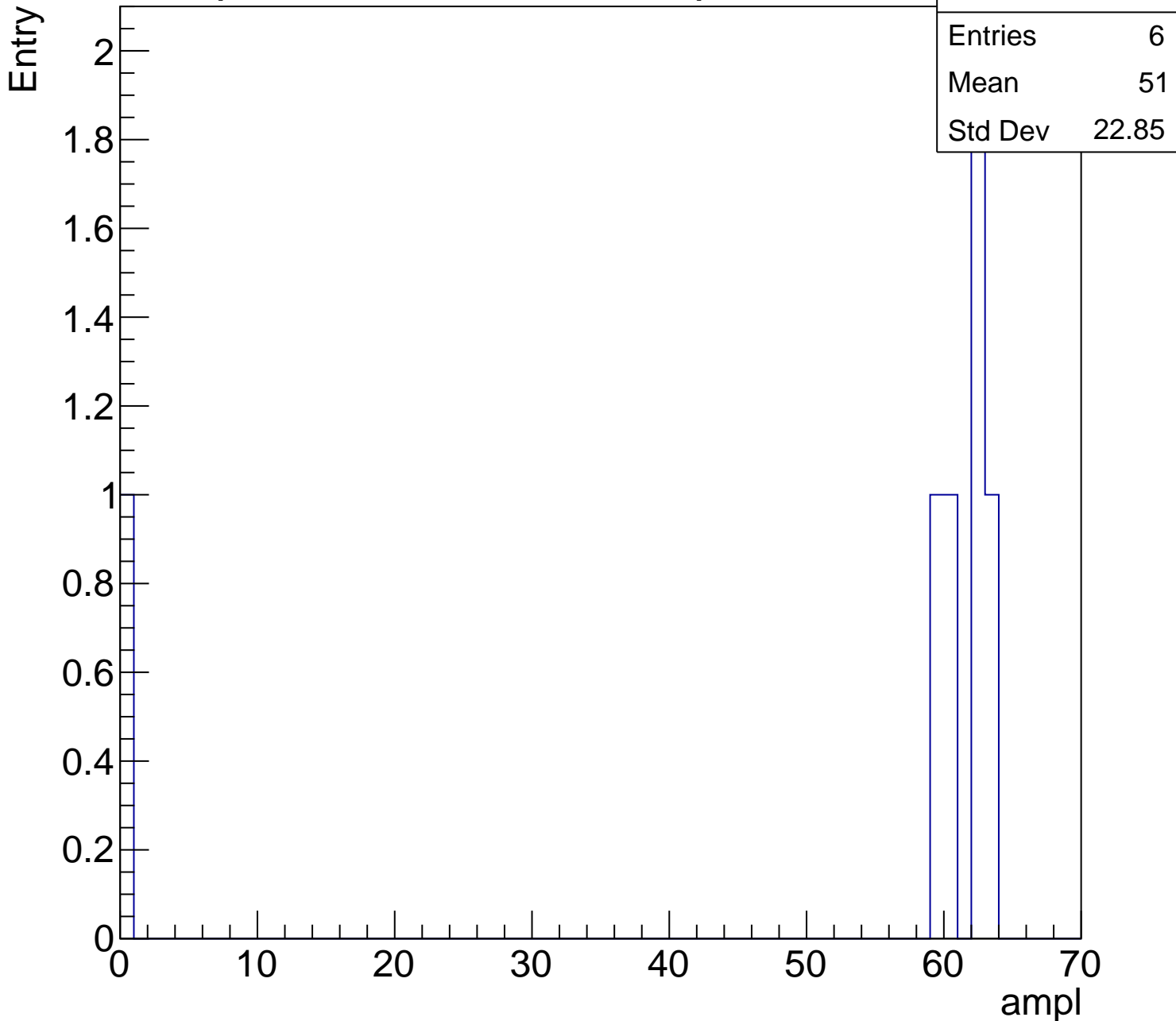
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	51
Std Dev	22.85

0 10 20 30 40 50 60 70

ampl





# B0L001S, U6-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch125, adc0

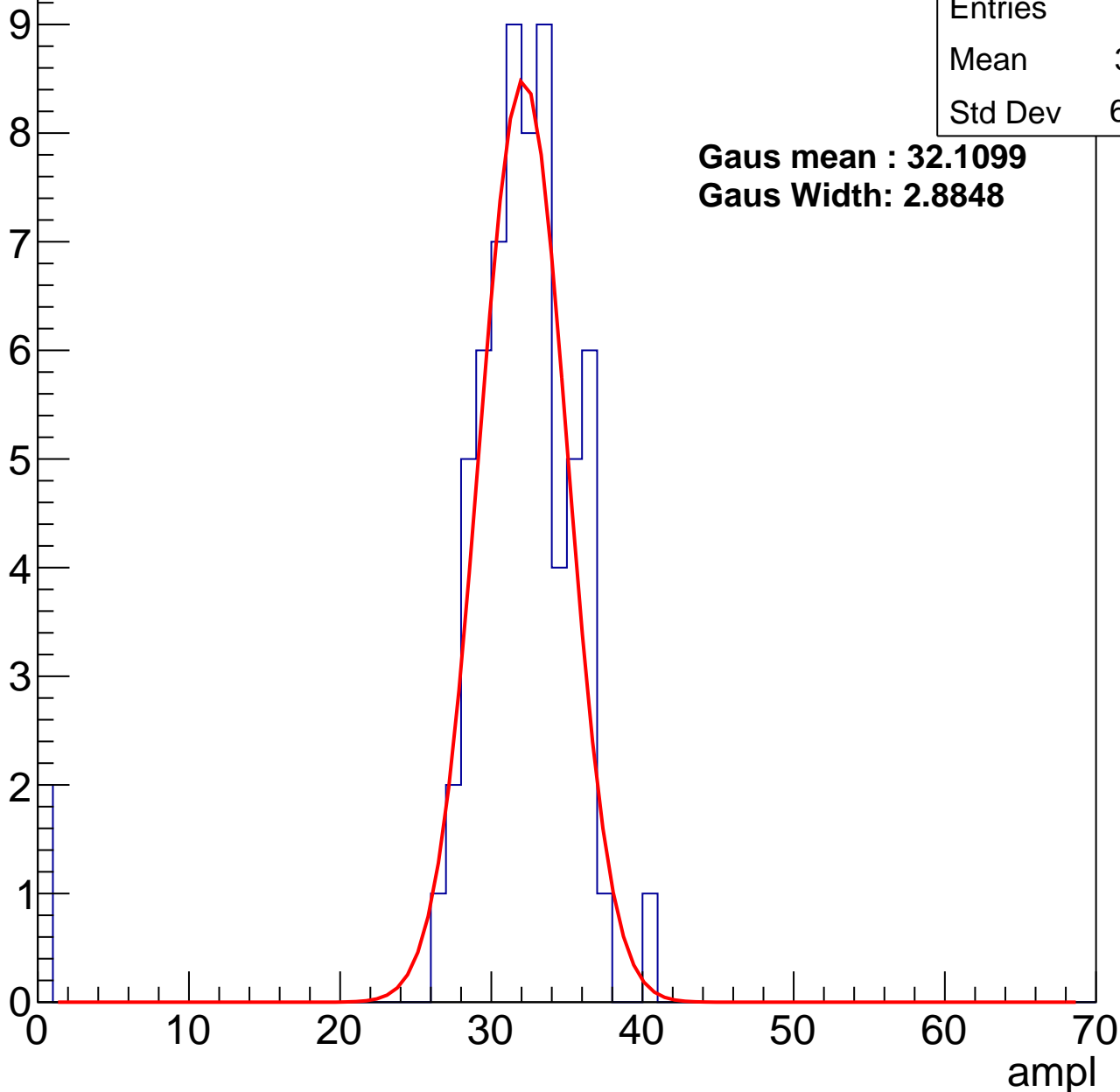
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	30.91
Std Dev	6.132

**Gaus mean : 32.1099**

**Gaus Width: 2.8848**



# B0L001S, U6-ch125, adc1

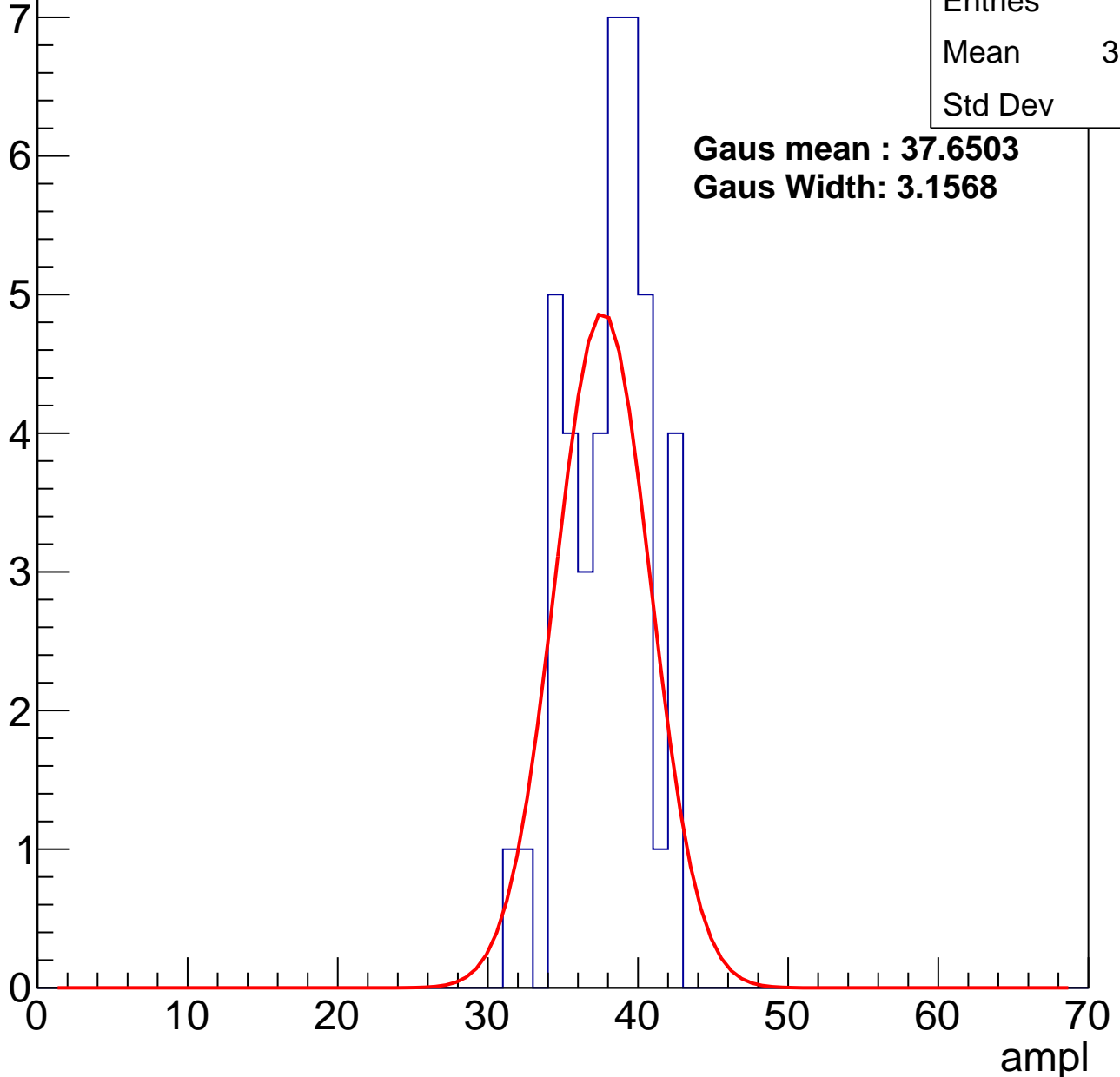
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	42
Mean	37.55
Std Dev	2.71

**Gaus mean : 37.6503**

**Gaus Width: 3.1568**



# B0L001S, U6-ch125, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	73
Mean	42.56
Std Dev	3.396

**Gaus mean : 43.3939**

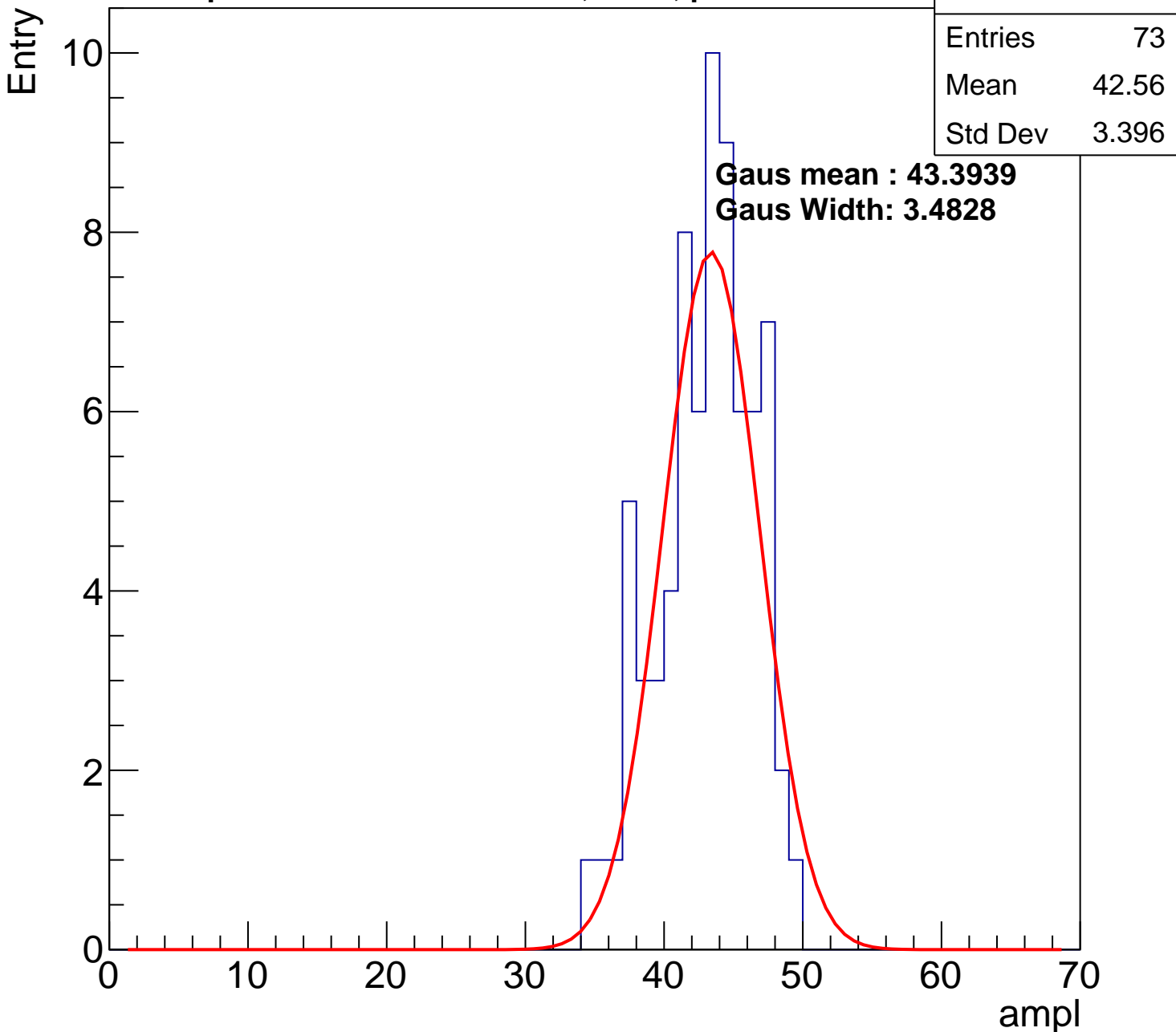
**Gaus Width: 3.4828**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

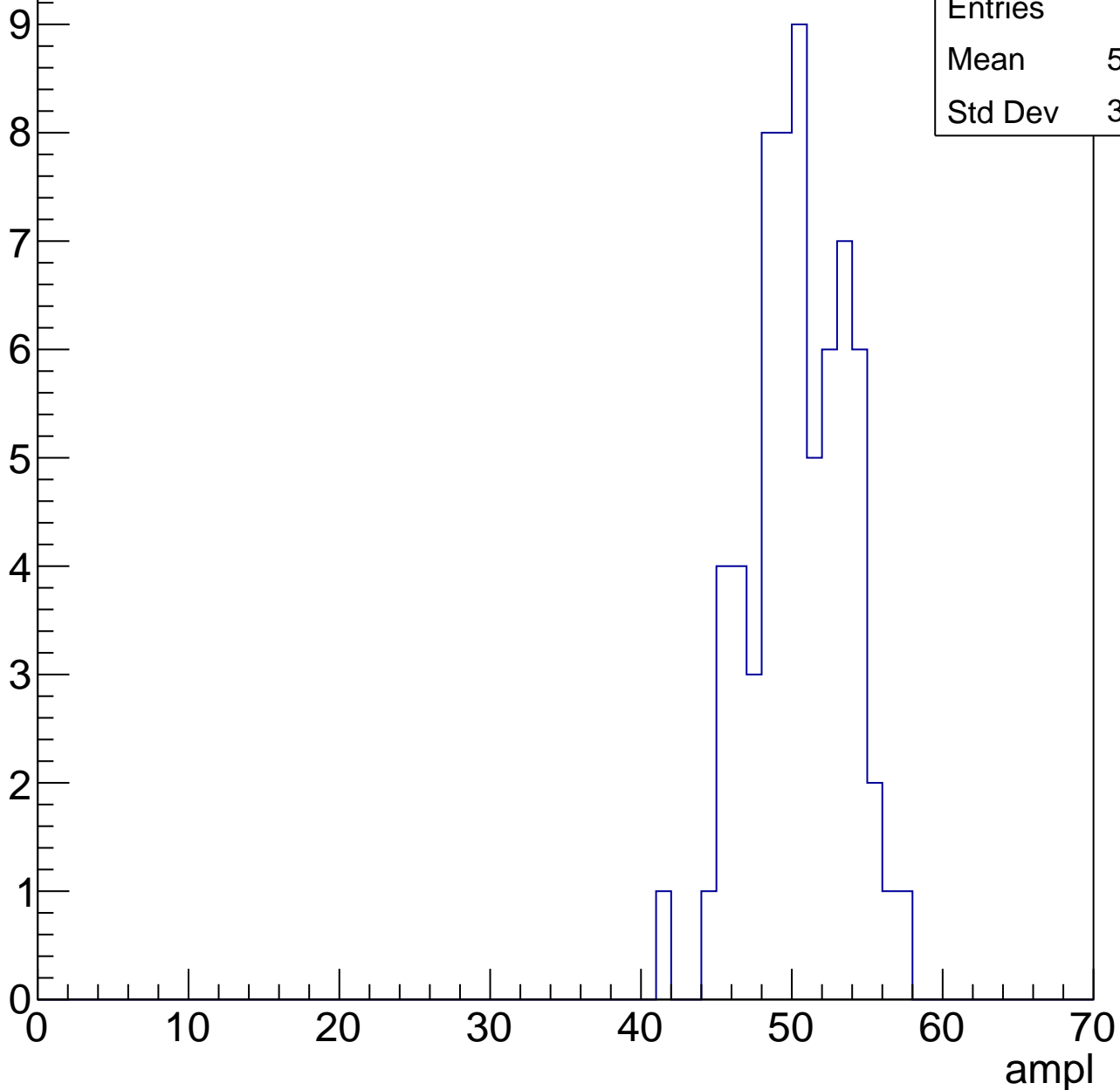


# B0L001S, U6-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	50.02
Std Dev	3.188

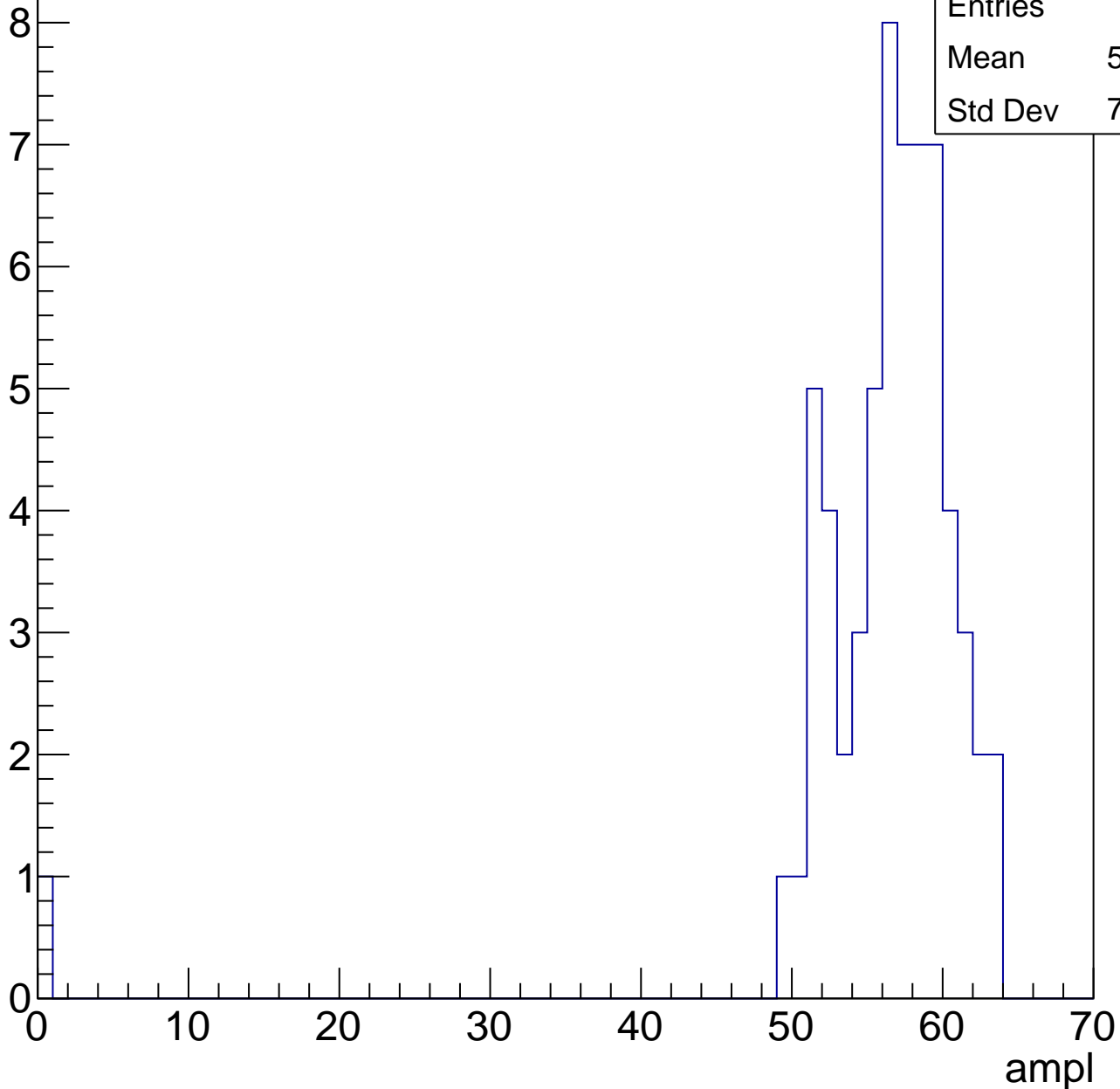


# B0L001S, U6-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	55.55
Std Dev	7.869

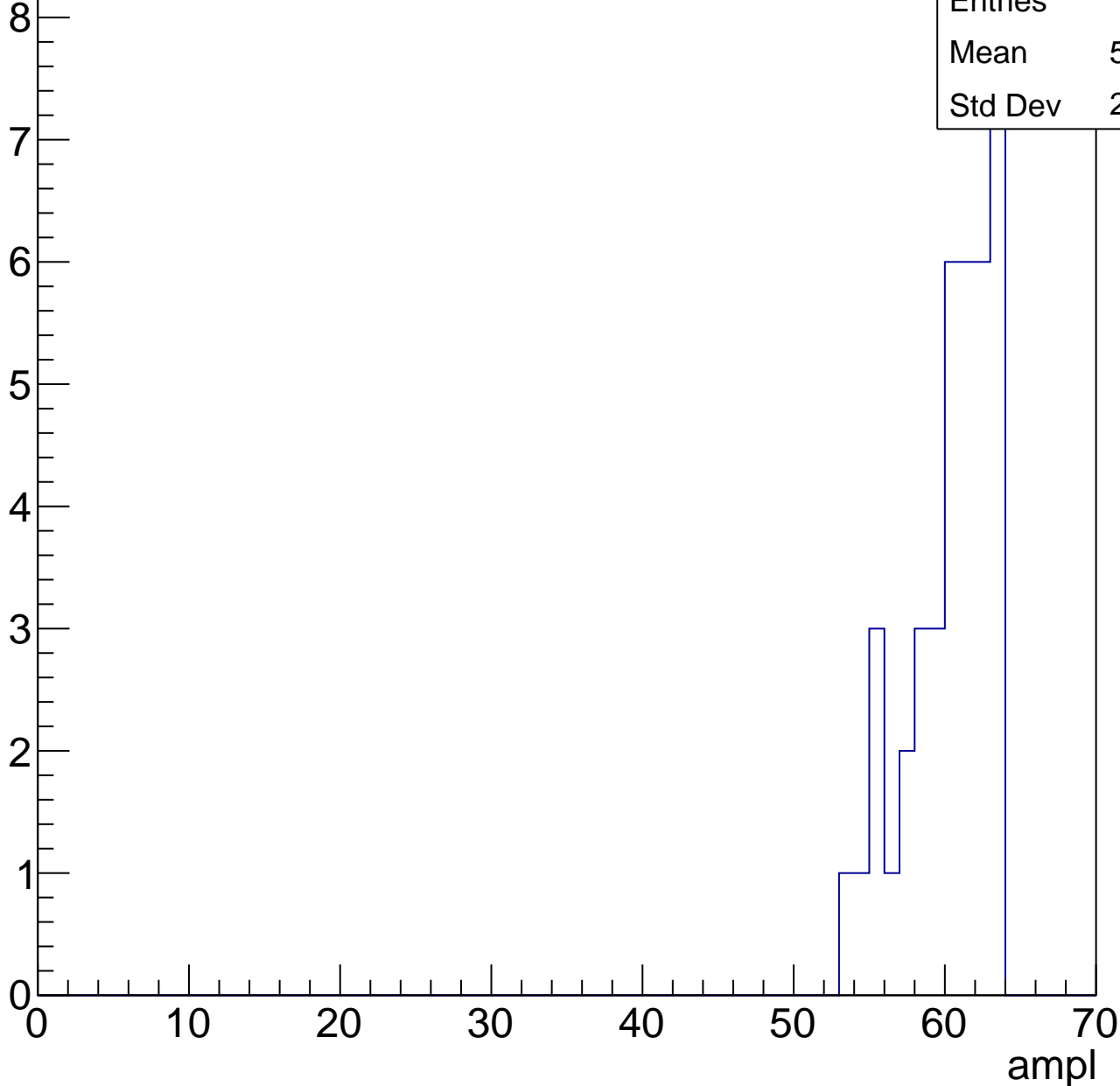


# B0L001S, U6-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	40
Mean	59.88
Std Dev	2.786



# B0L001S, U6-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	61.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B0L001S, U6-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U6-ch126, adc0

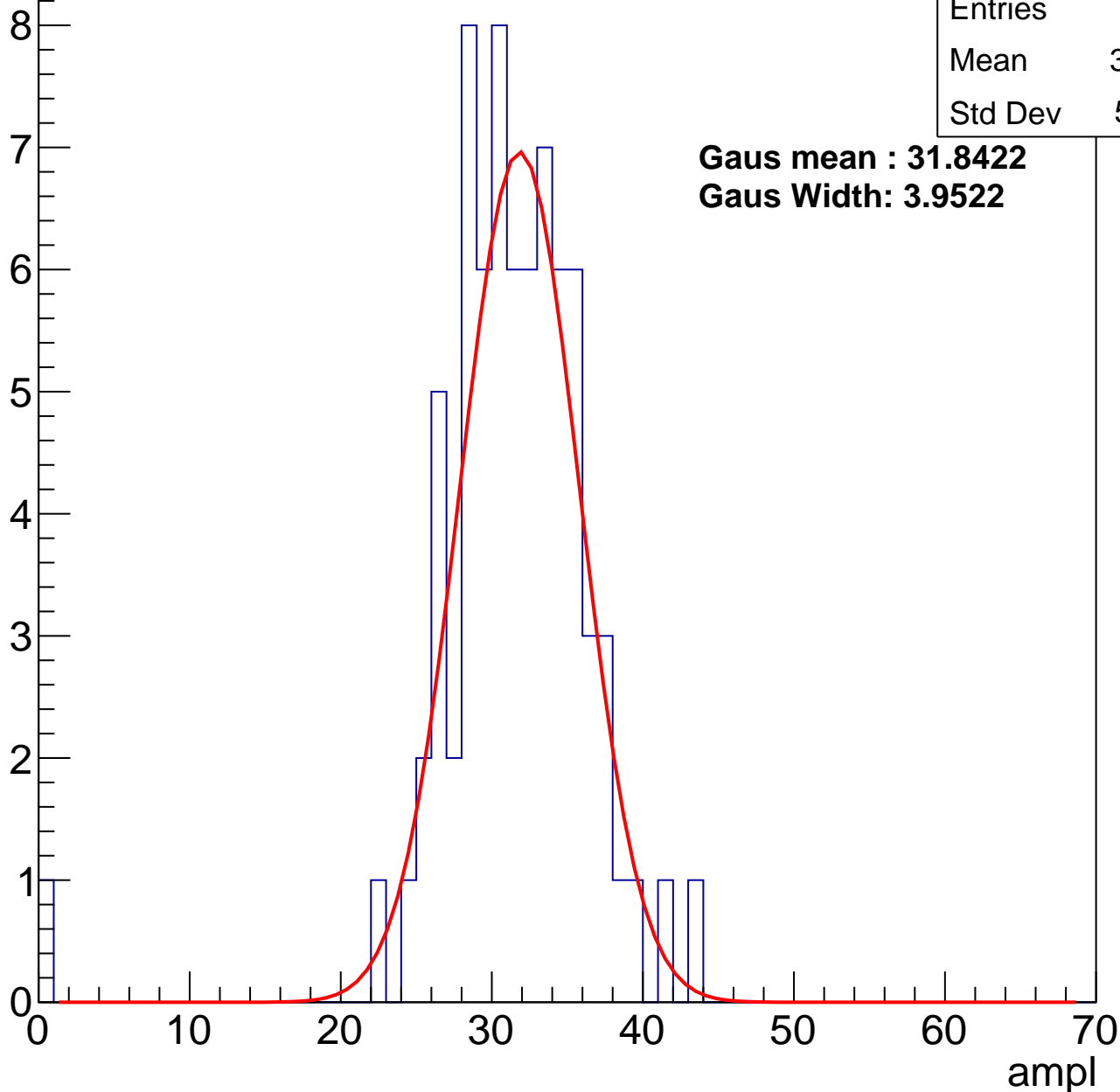
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	30.95
Std Dev	5.351

**Gaus mean : 31.8422**

**Gaus Width: 3.9522**



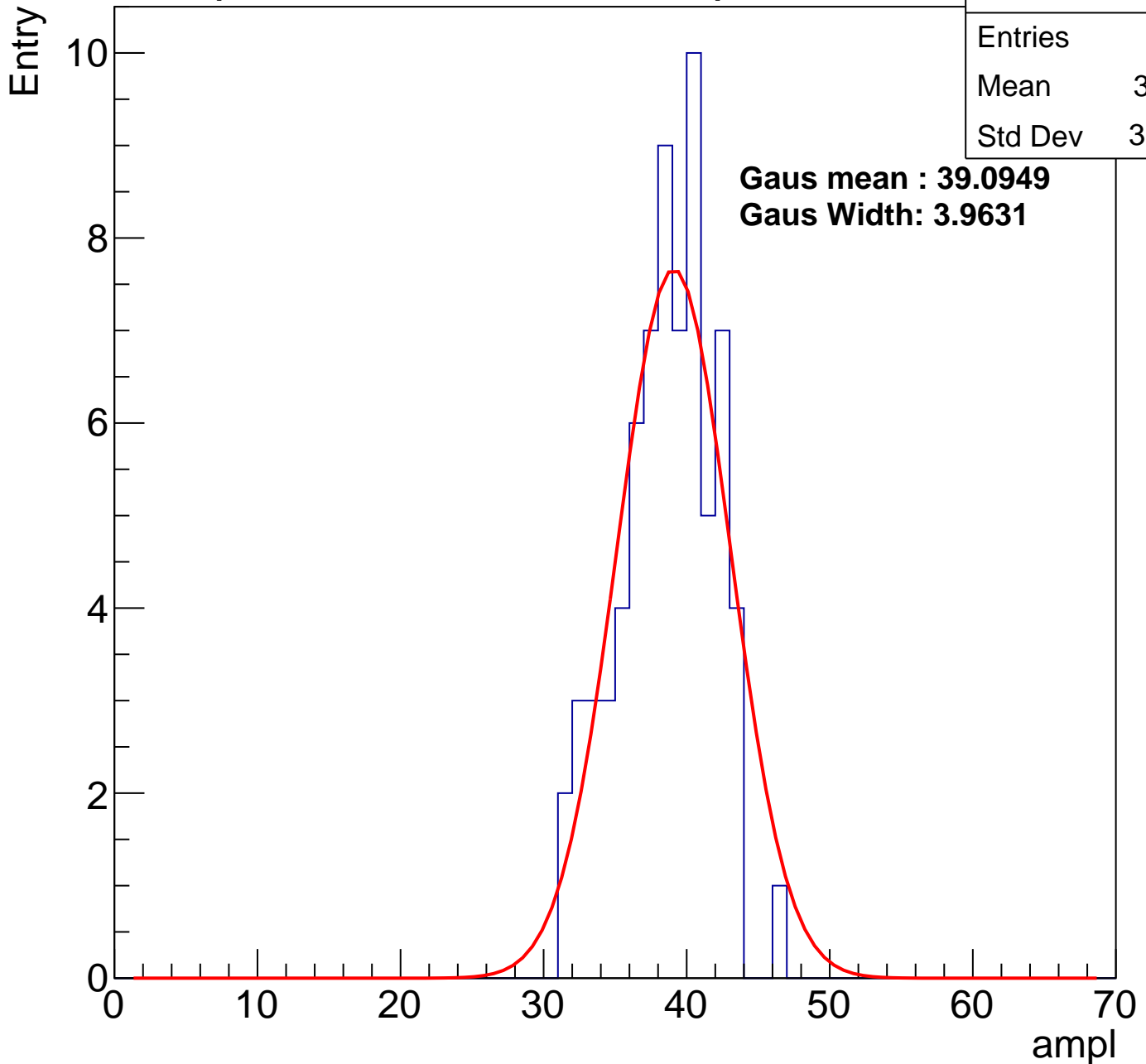
# B0L001S, U6-ch126, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	71
Mean	38.11
Std Dev	3.278

**Gaus mean : 39.0949**

**Gaus Width: 3.9631**



# B0L001S, U6-ch126, adc2

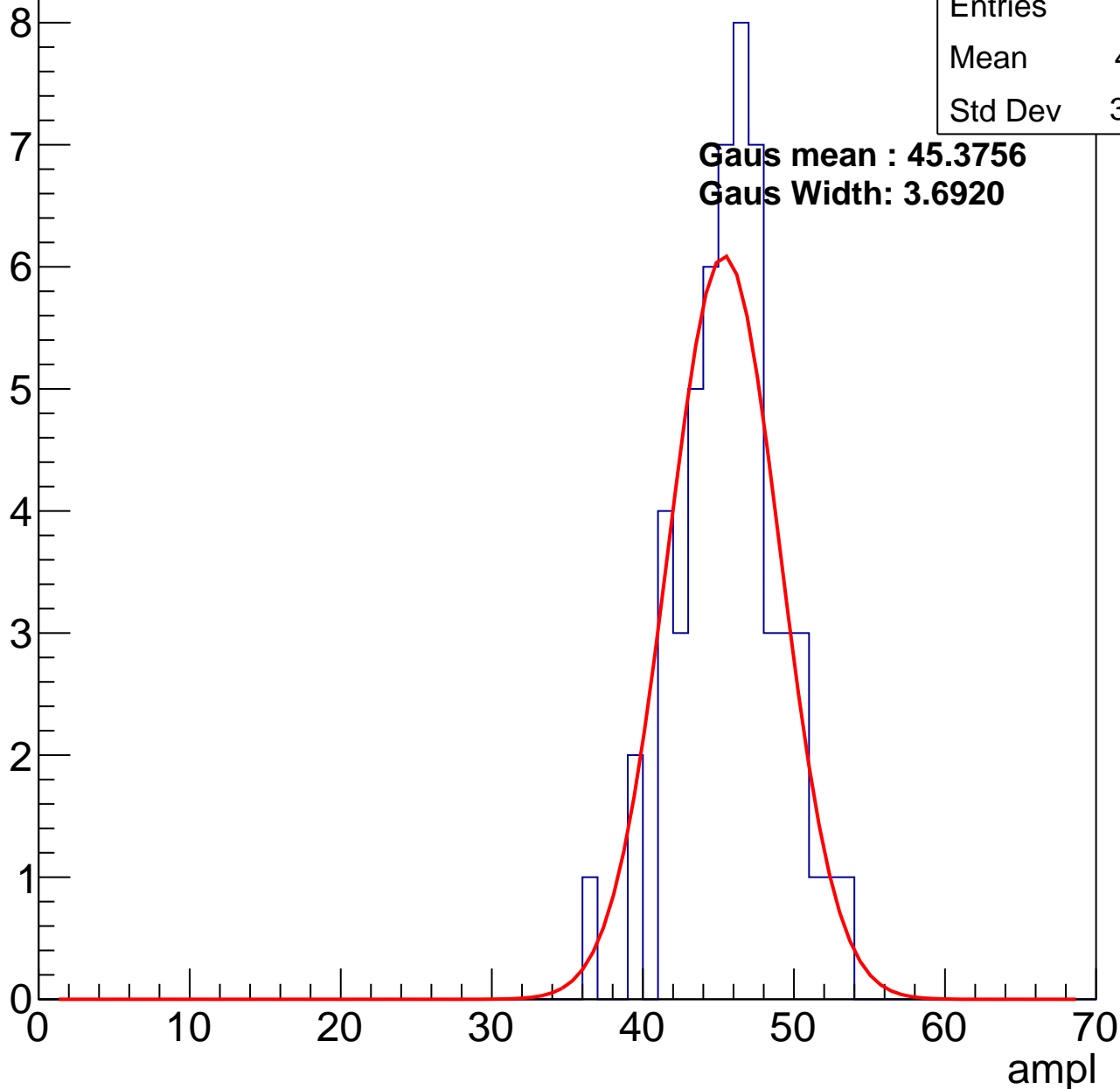
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	45.31
Std Dev	3.302

**Gaus mean : 45.3756**

**Gaus Width: 3.6920**

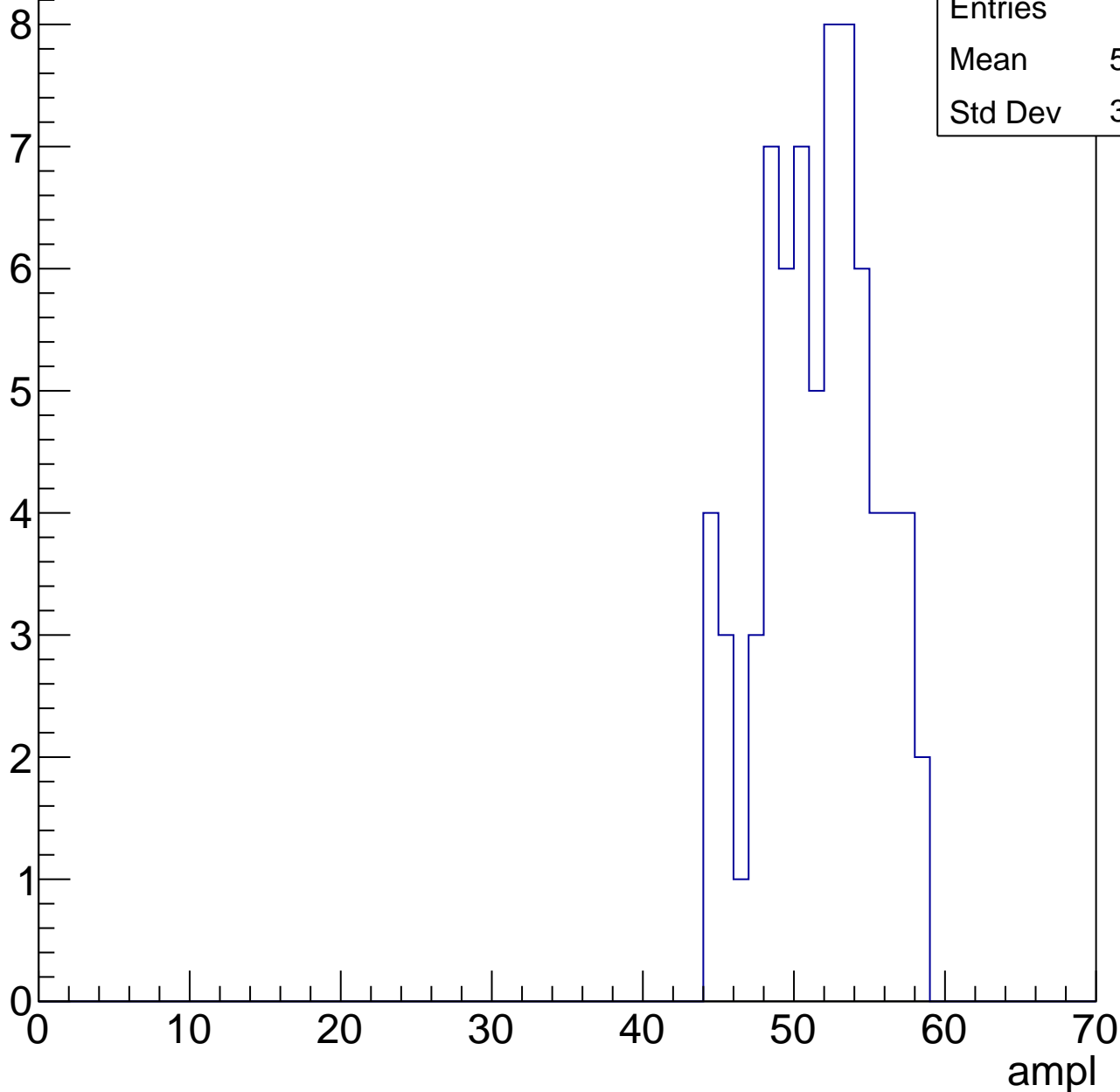


# B0L001S, U6-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	51.18
Std Dev	3.668

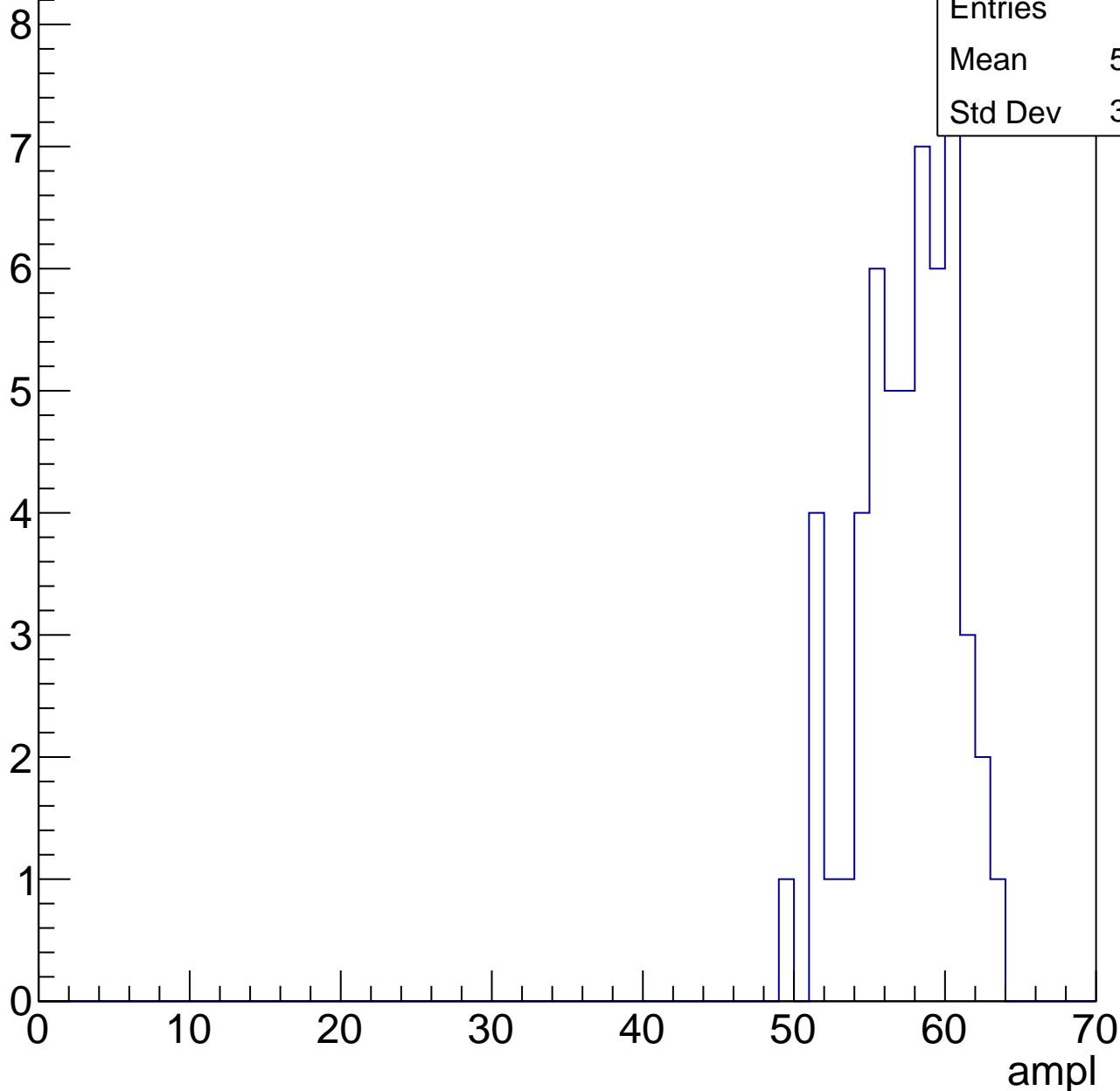


# B0L001S, U6-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	57.02
Std Dev	3.194



# B0L001S, U6-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	33
Mean	59.21
Std Dev	10.62

ampl

0 10 20 30 40 50 60 70

1

2

3

4

5

6

7

8

# B0L001S, U6-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	63
Std Dev	0



# B0L001S, U6-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U6-ch127, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	81
Mean	28.23
Std Dev	5.744

**Gaus mean : 29.8998**

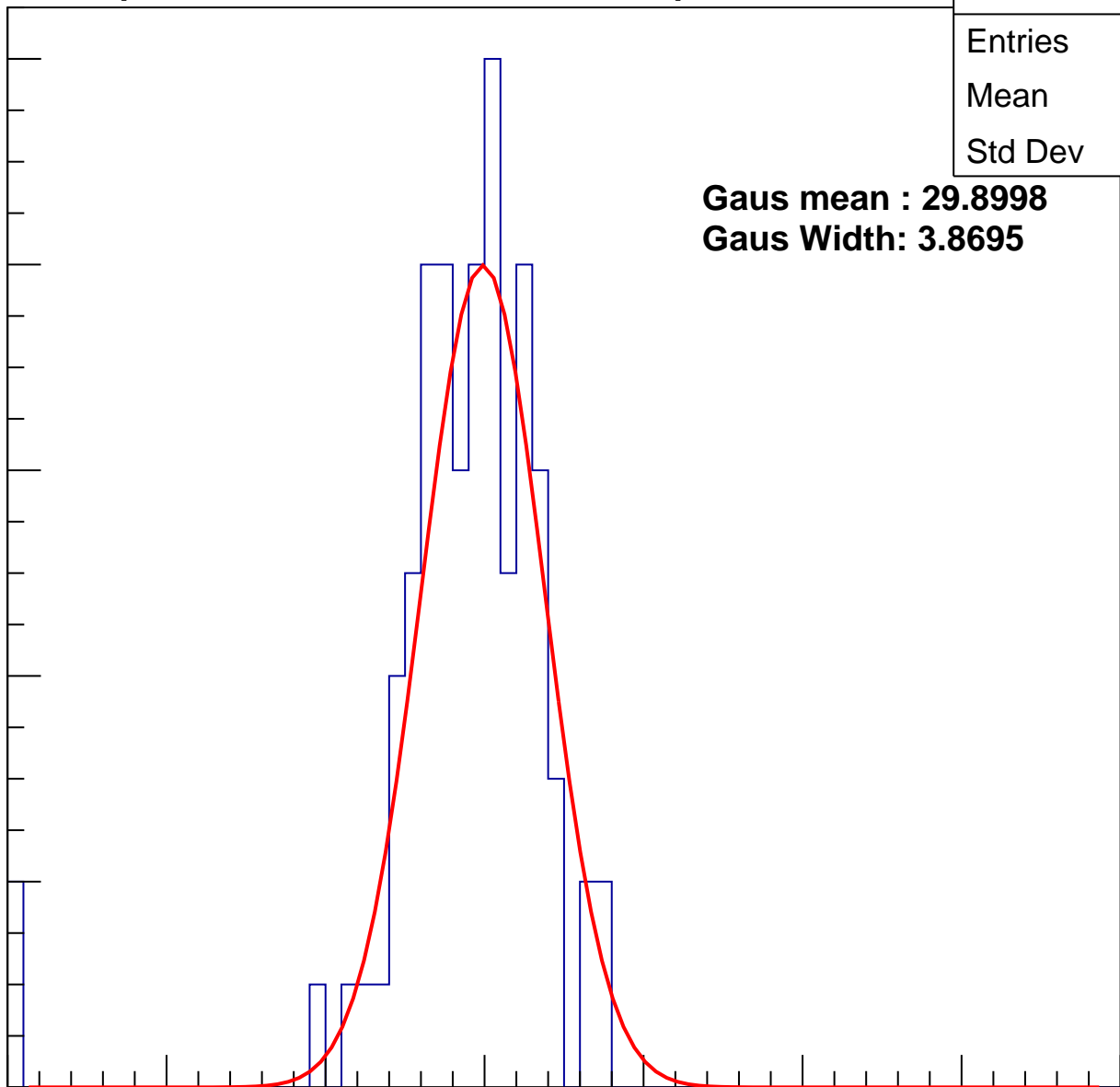
**Gaus Width: 3.8695**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U6-ch127, adc1

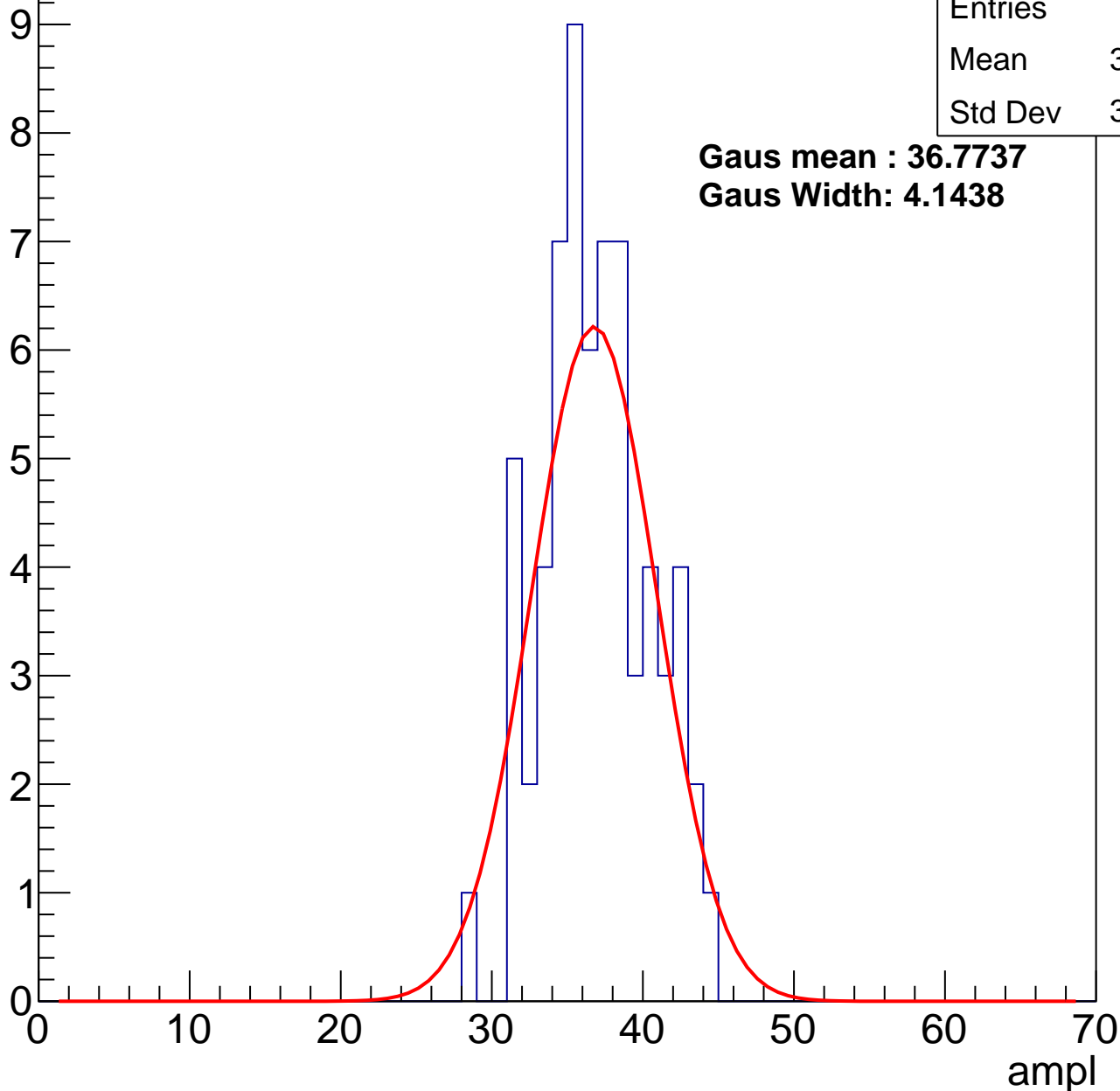
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	36.48
Std Dev	3.478

**Gaus mean : 36.7737**

**Gaus Width: 4.1438**



# B0L001S, U6-ch127, adc2

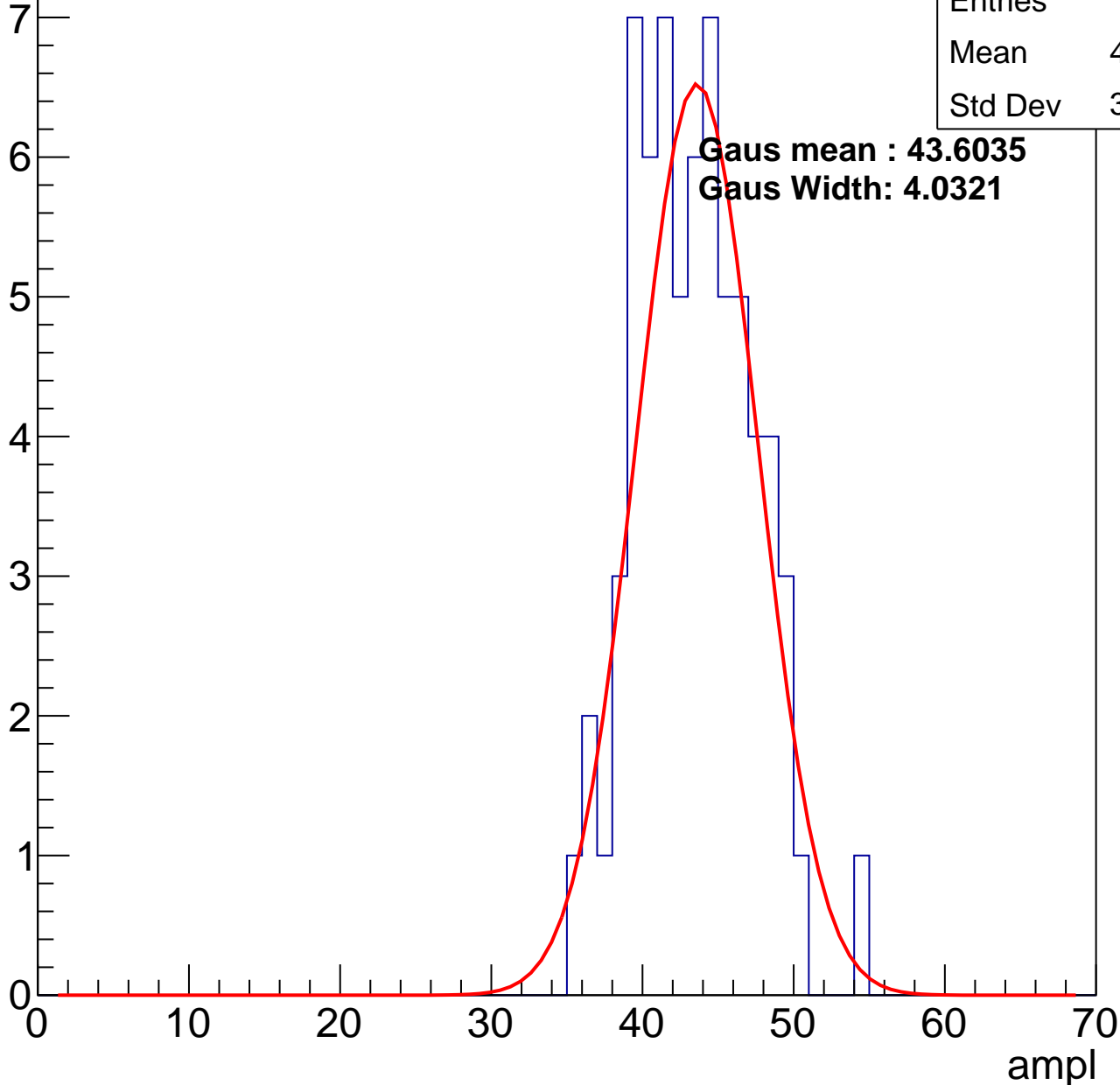
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	42.94
Std Dev	3.807

**Gaus mean : 43.6035**

**Gaus Width: 4.0321**

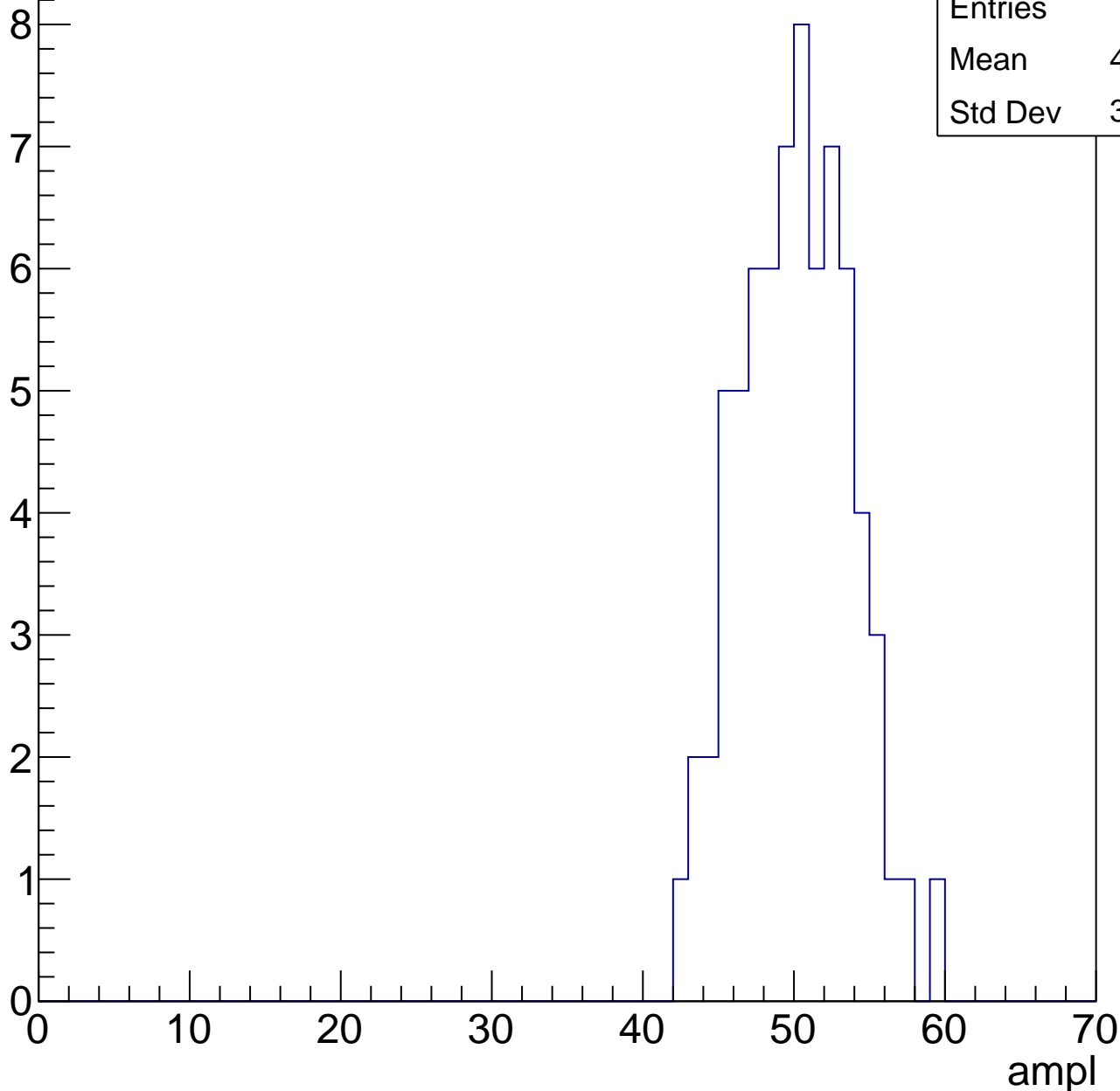


# B0L001S, U6-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	49.65
Std Dev	3.577

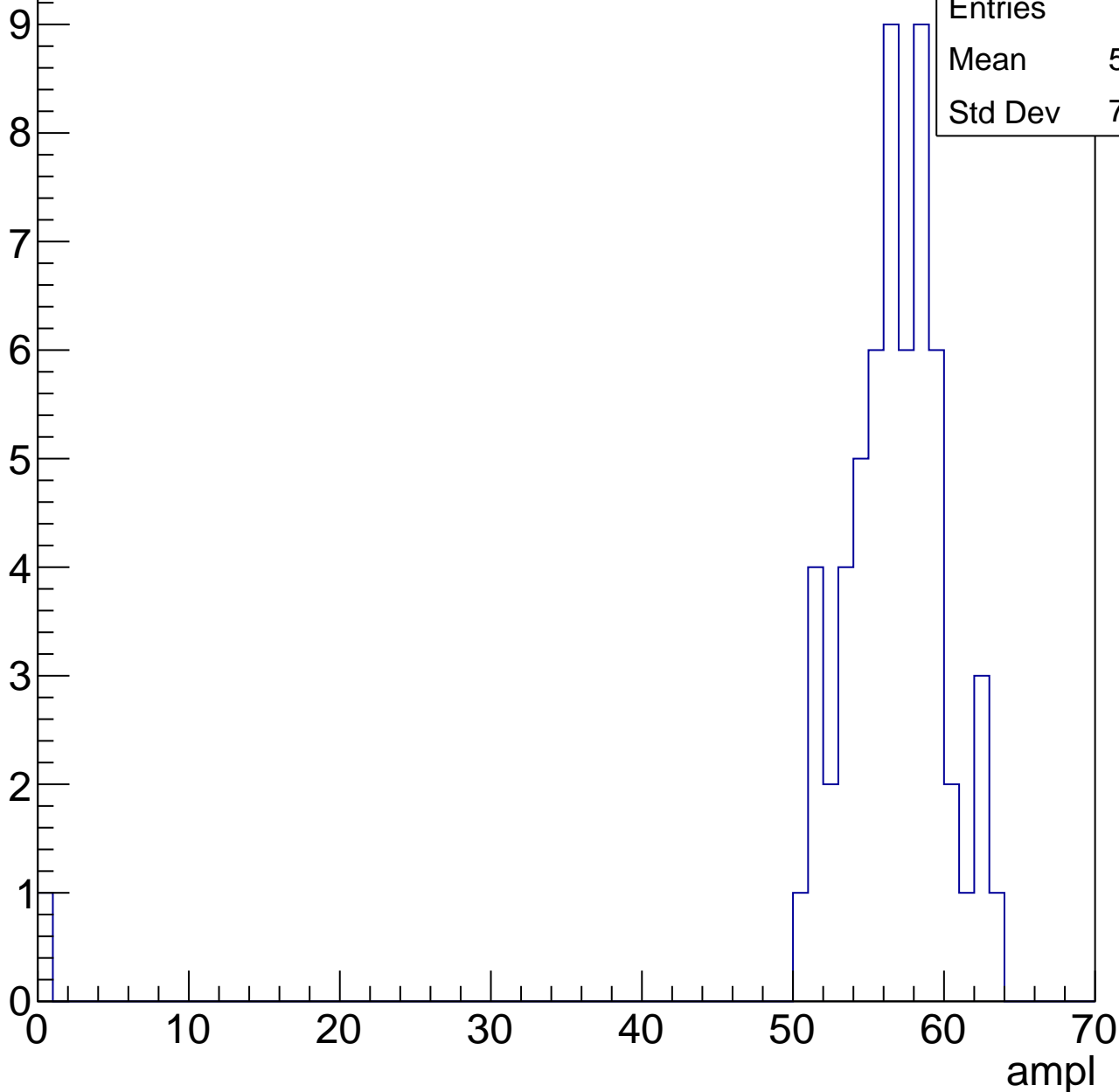


# B0L001S, U6-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	55.37
Std Dev	7.802

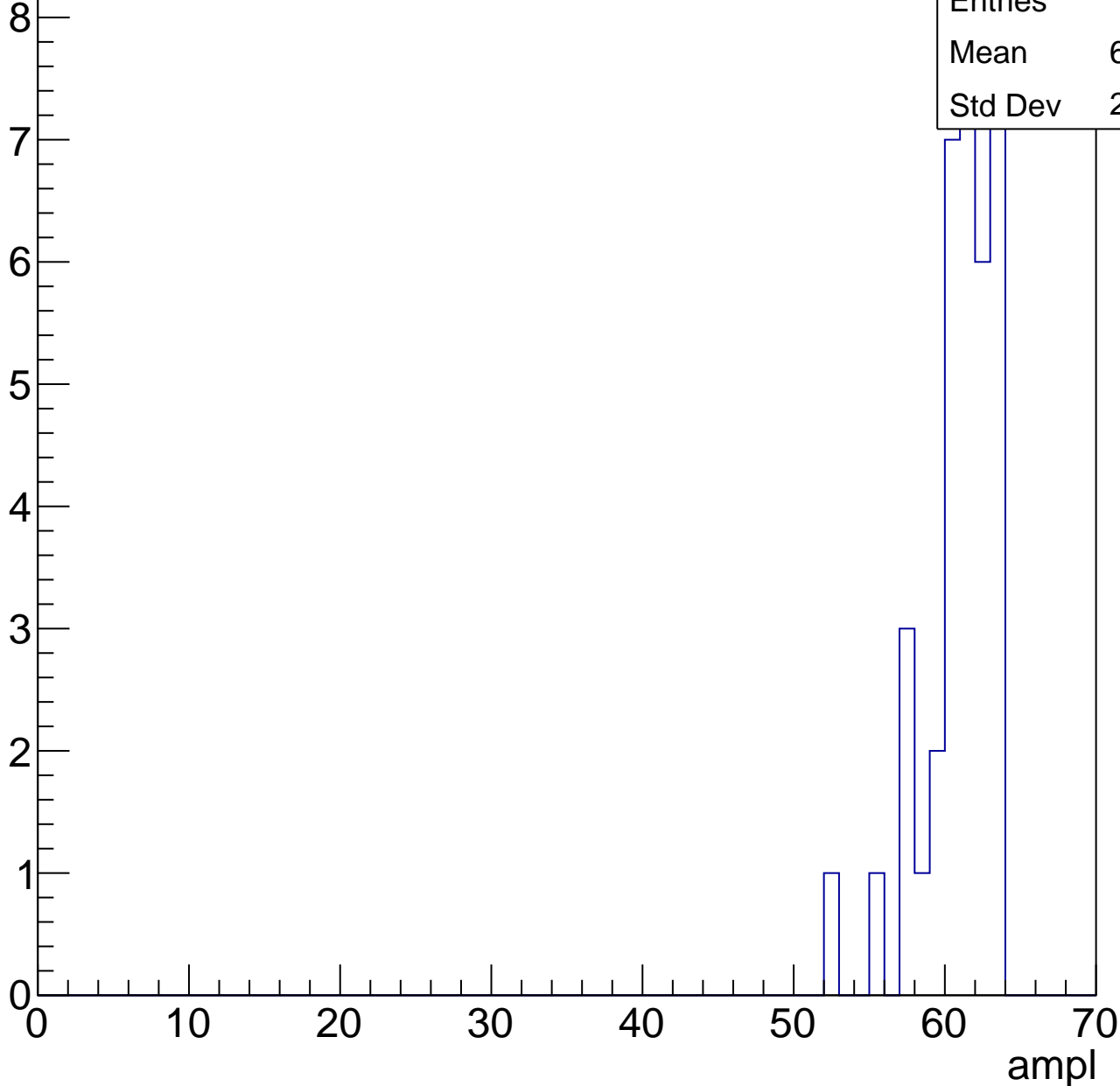


# B0L001S, U6-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

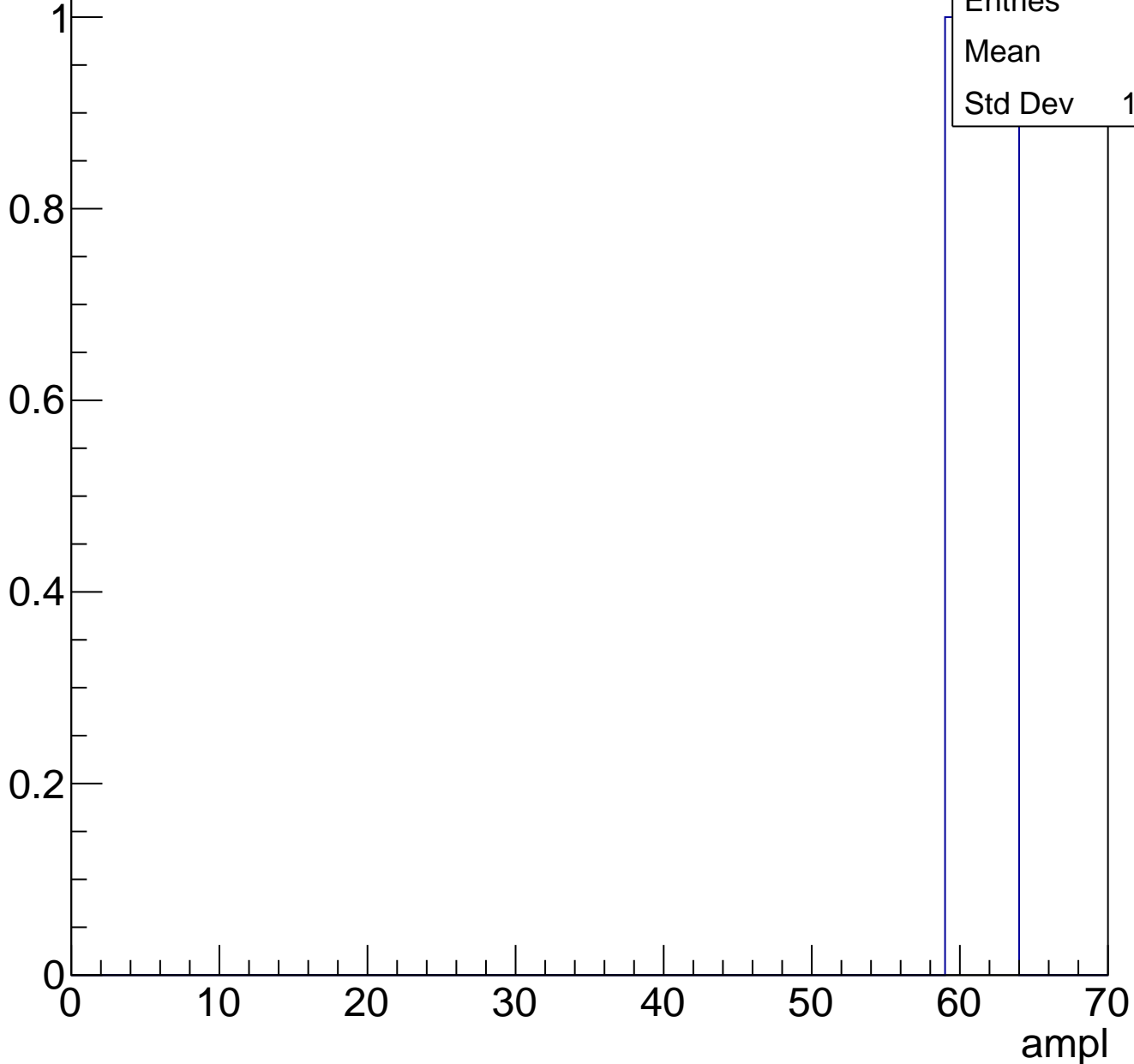
Entries	37
Mean	60.49
Std Dev	2.423



# B0L001S, U6-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U6-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U6-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0