



# B1L102S, U3-ch0, adc0

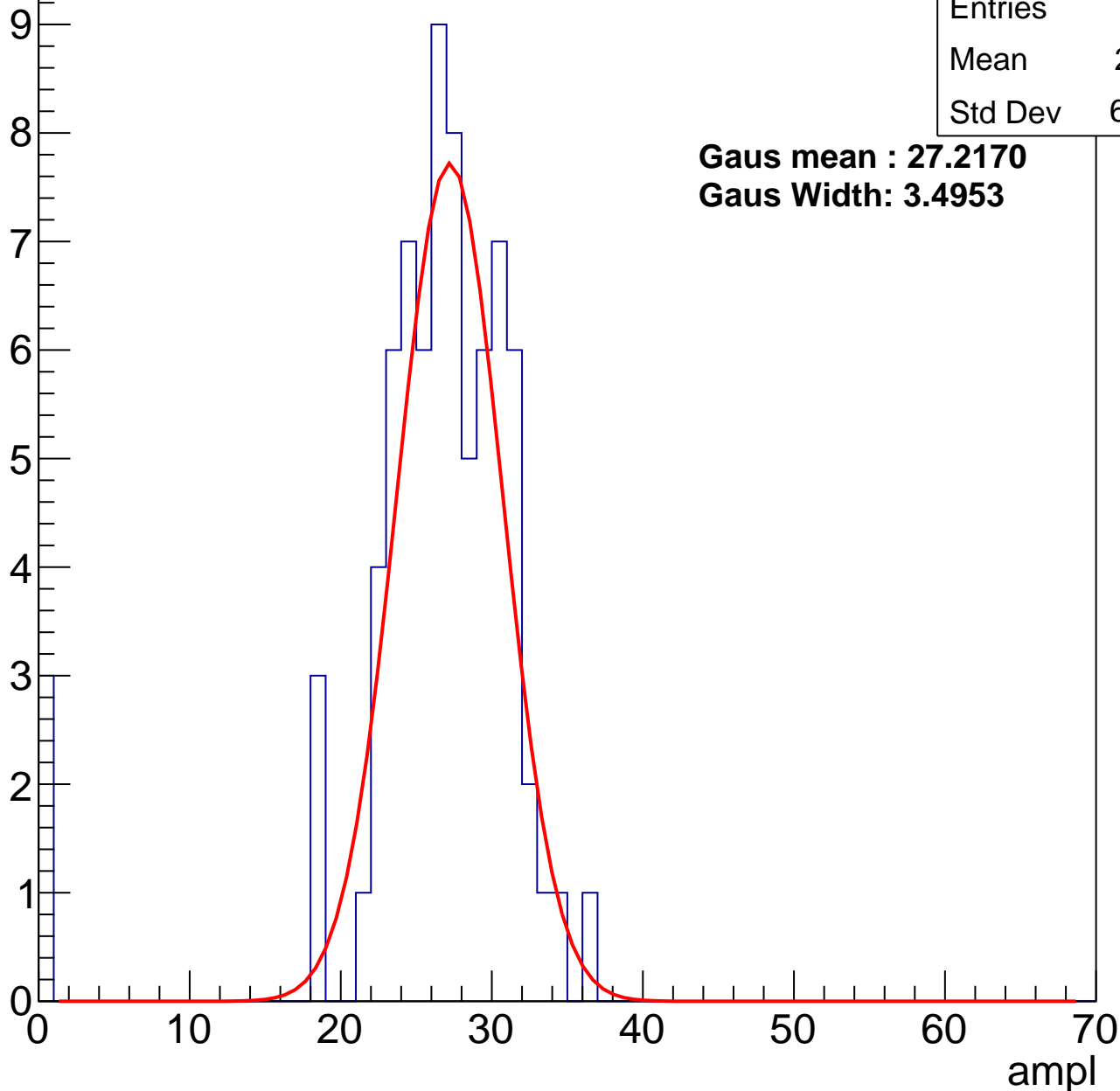
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	25.61
Std Dev	6.298

**Gaus mean : 27.2170**

**Gaus Width: 3.4953**



# B1L102S, U3-ch0, adc1

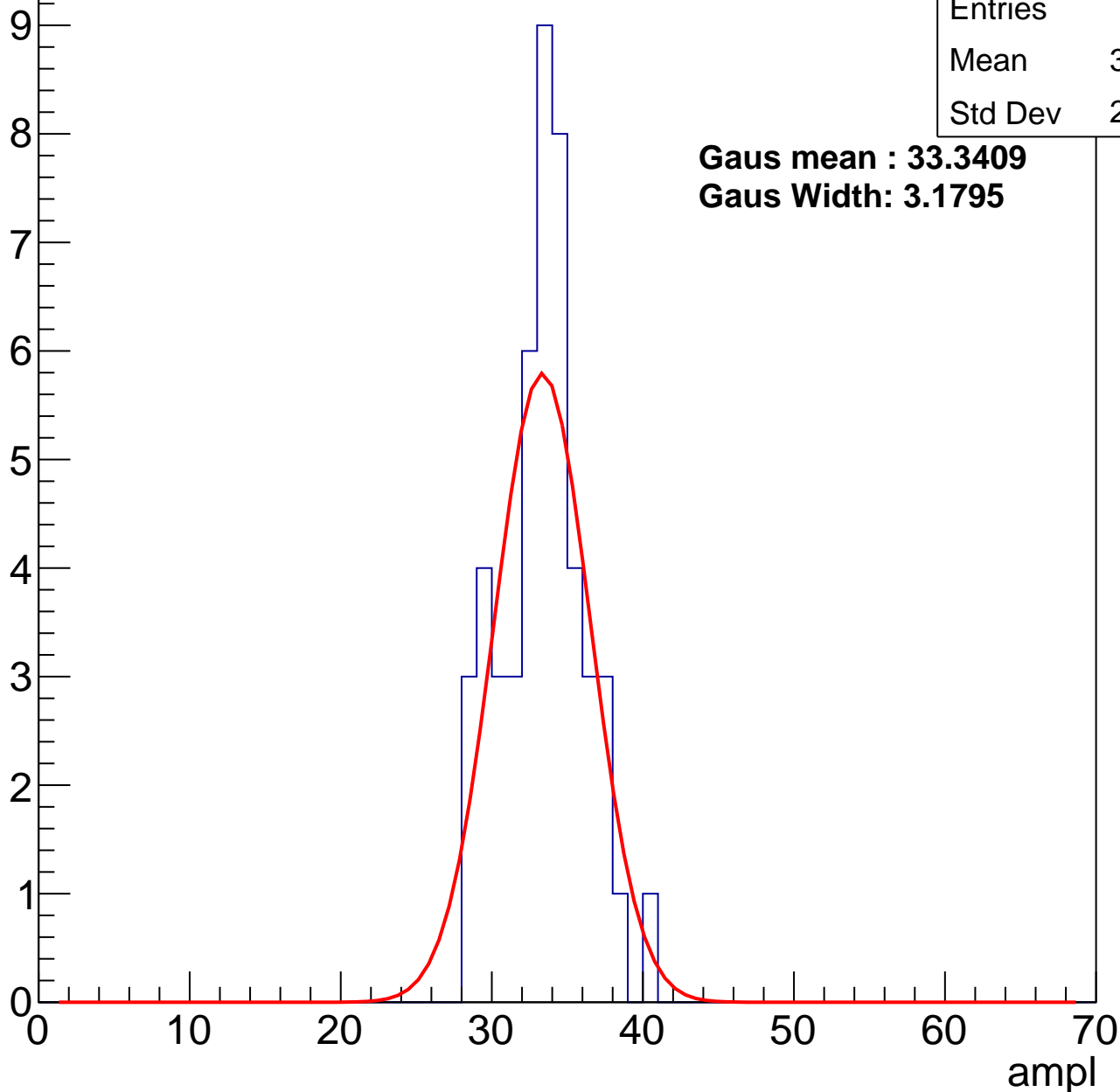
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	32.94
Std Dev	2.726

**Gaus mean : 33.3409**

**Gaus Width: 3.1795**



# B1L102S, U3-ch0, adc2

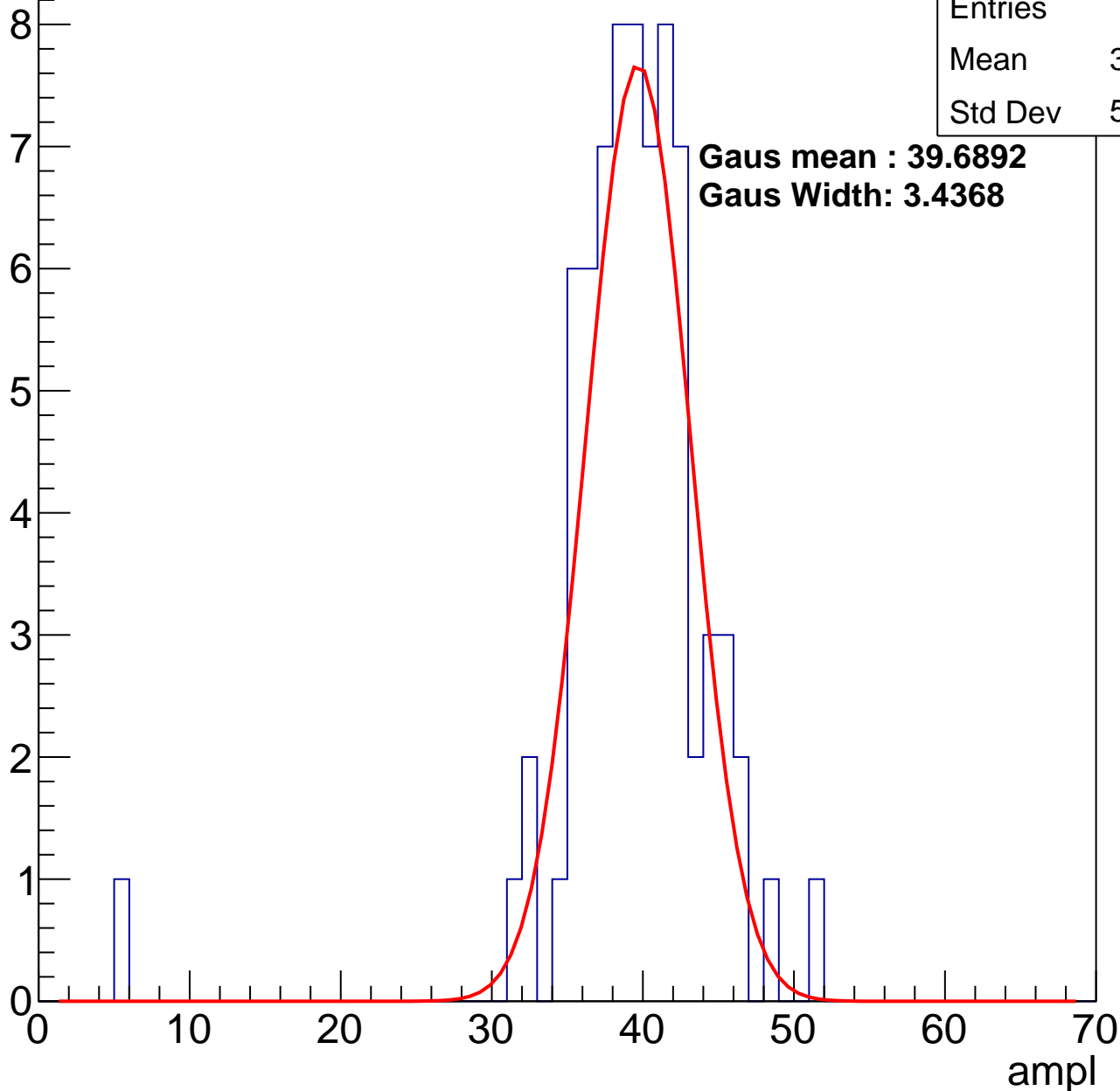
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	38.93
Std Dev	5.414

**Gaus mean : 39.6892**

**Gaus Width: 3.4368**

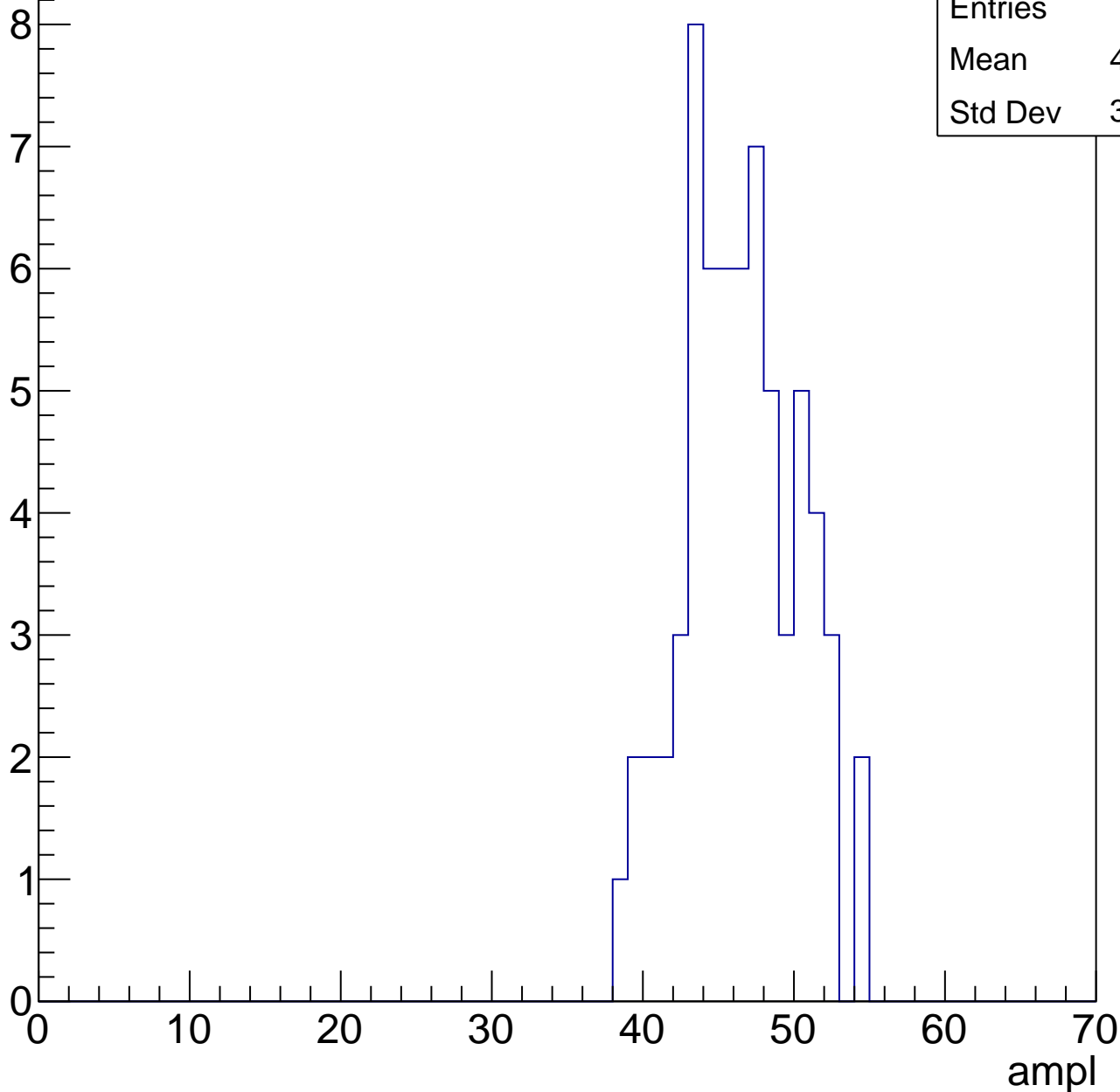


# B1L102S, U3-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	46.03
Std Dev	3.729



# B1L102S, U3-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	67
Mean	52.22
Std Dev	3.615

Entry

10

8

6

4

2

0

0

10

20

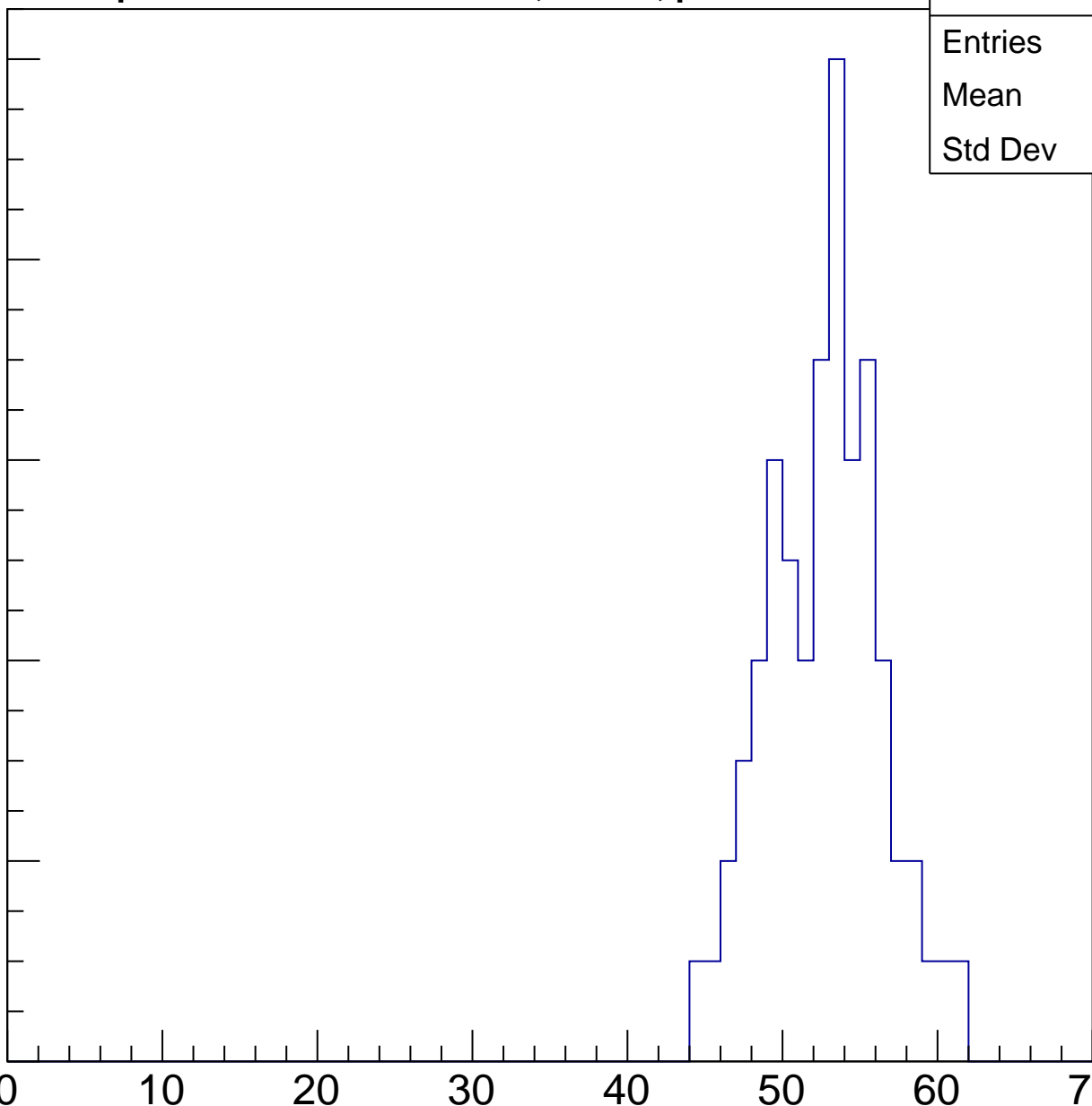
30

40

50

60

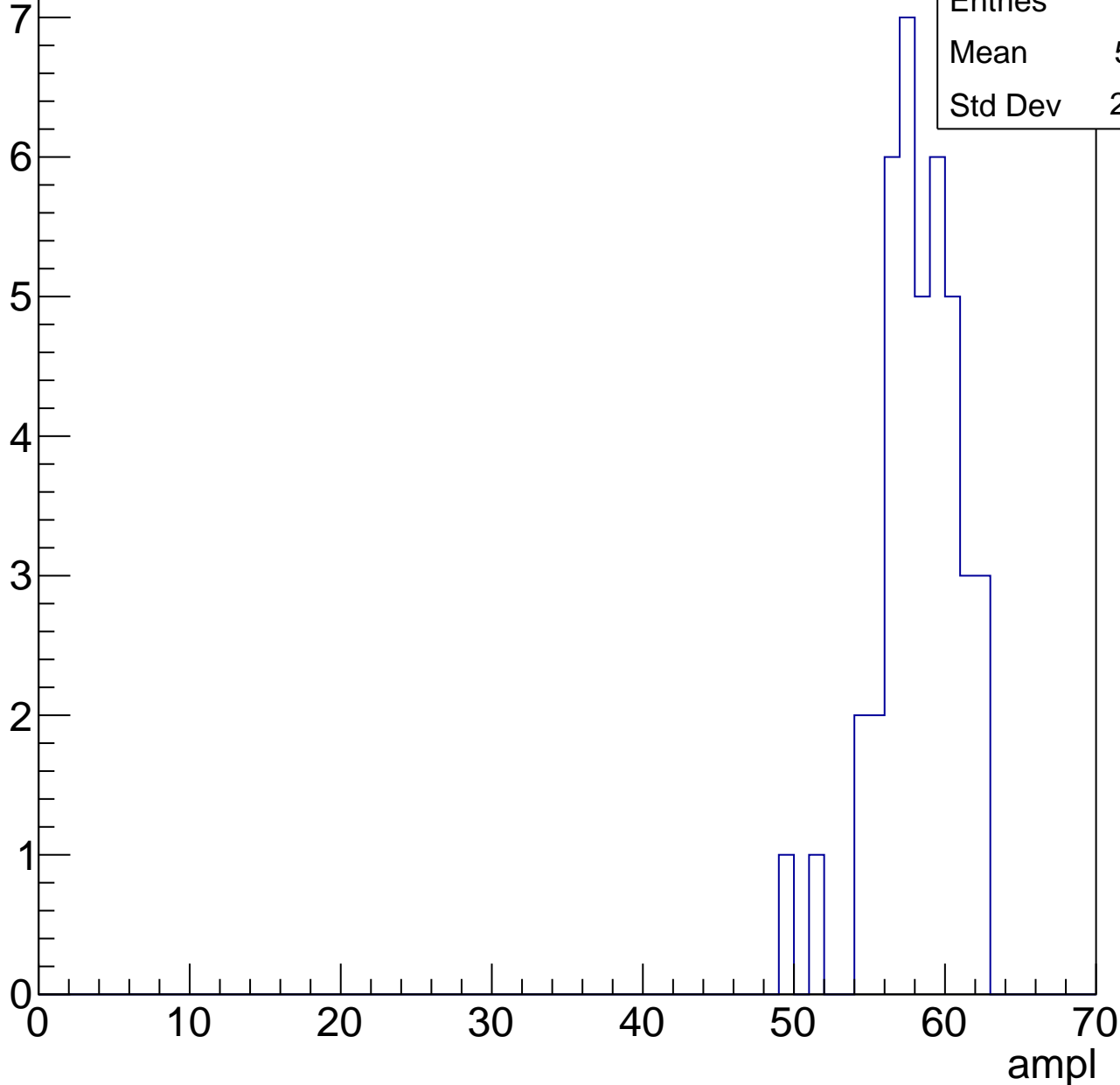
ampl



# B1L102S, U3-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

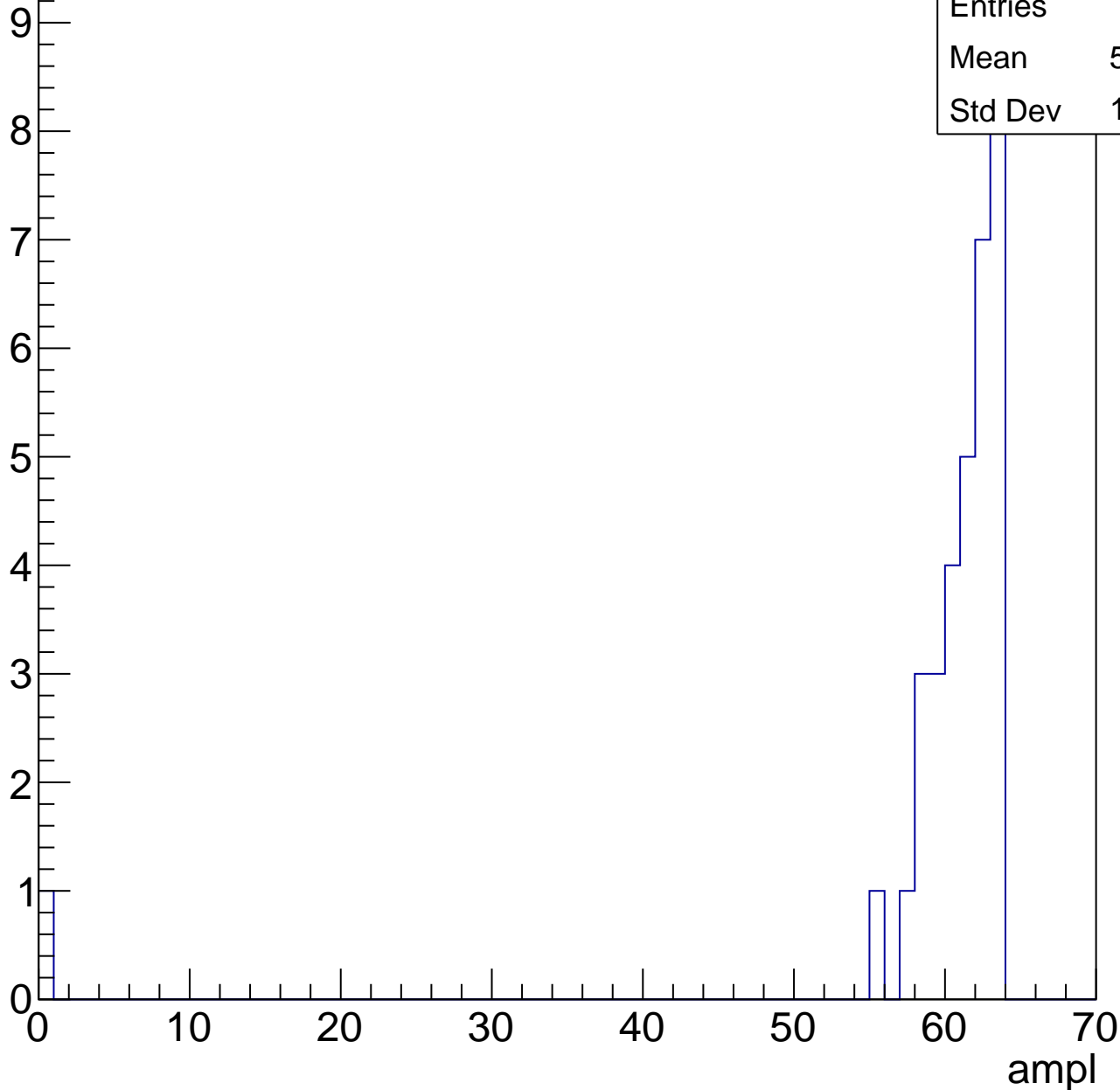


# B1L102S, U3-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	34
Mean	59.09
Std Dev	10.48

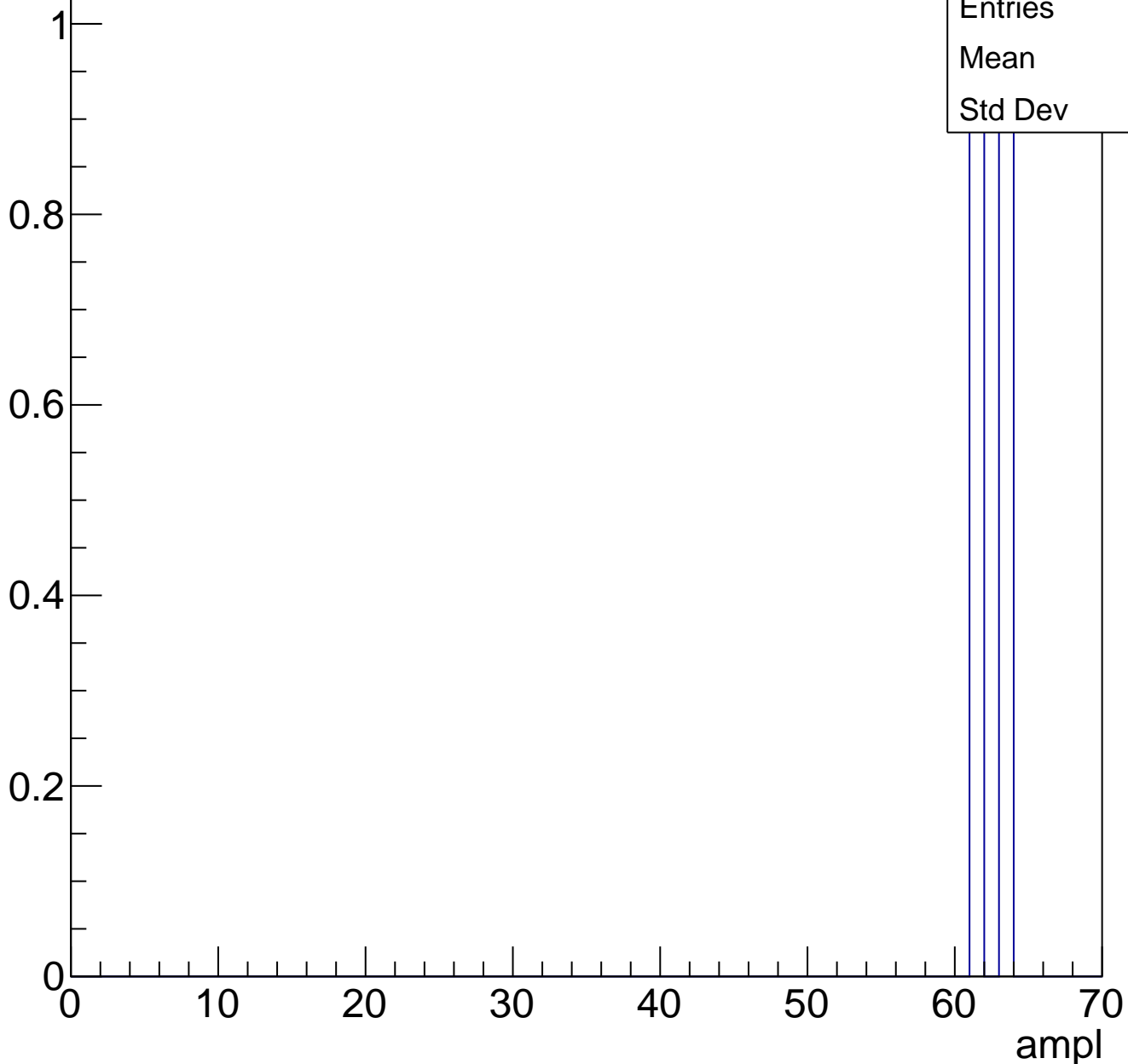




# B1L102S, U3-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch1, adc0

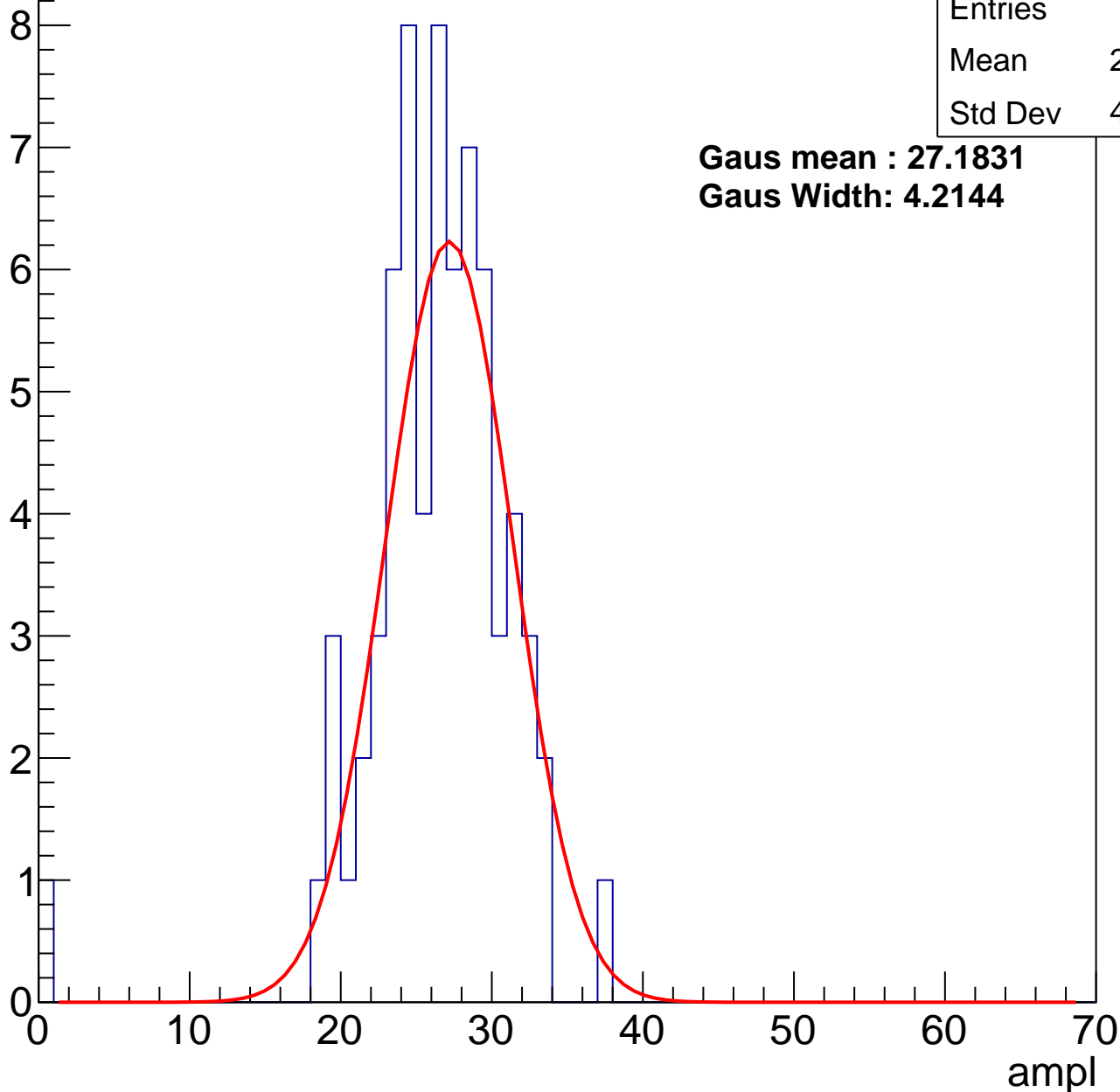
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	25.88
Std Dev	4.924

**Gaus mean : 27.1831**

**Gaus Width: 4.2144**



# B1L102S, U3-ch1, adc1

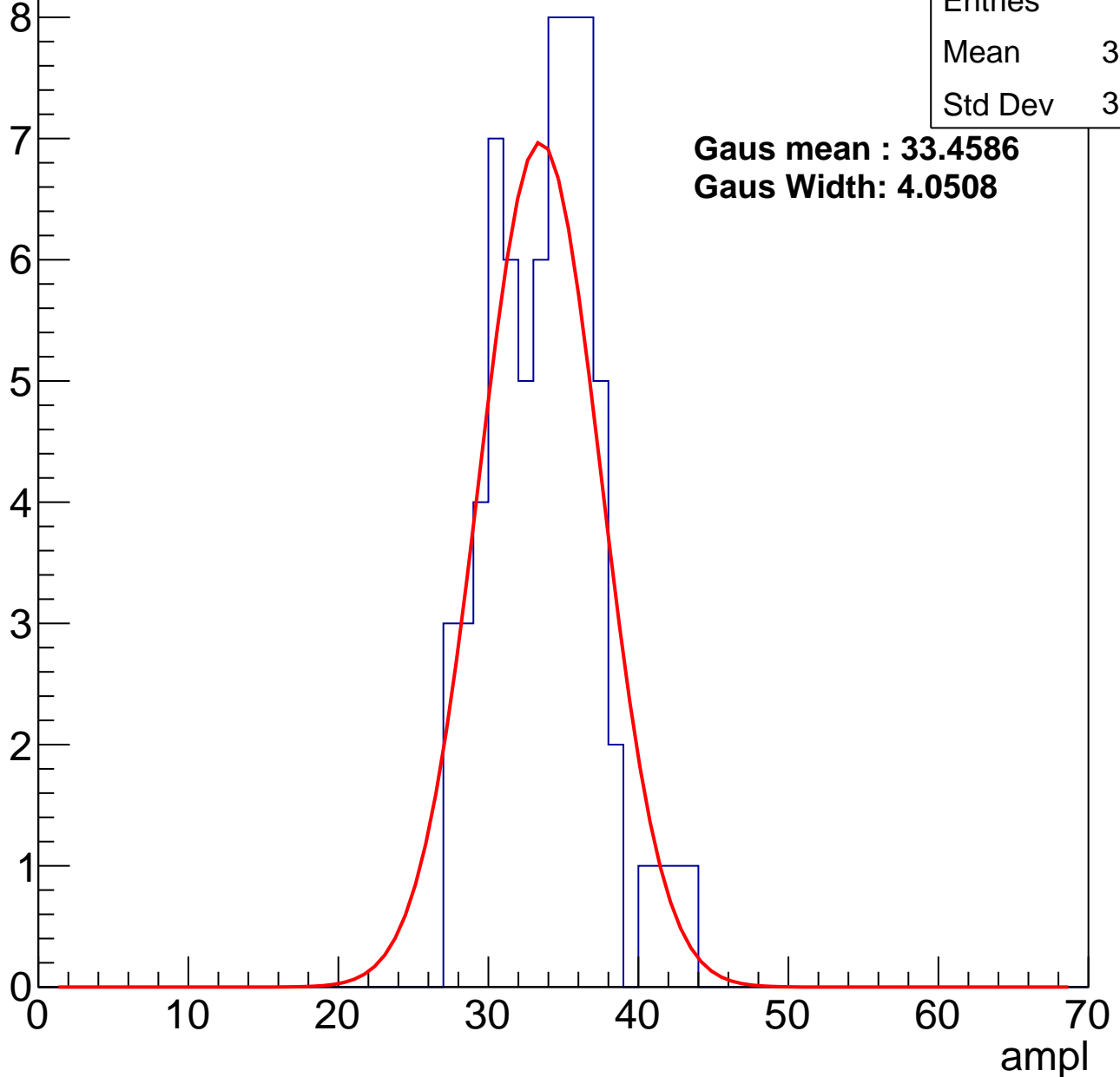
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	33.36
Std Dev	3.543

**Gaus mean : 33.4586**

**Gaus Width: 4.0508**



# B1L102S, U3-ch1, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	69
Mean	40.04
Std Dev	3.673

**Gaus mean : 41.0163**

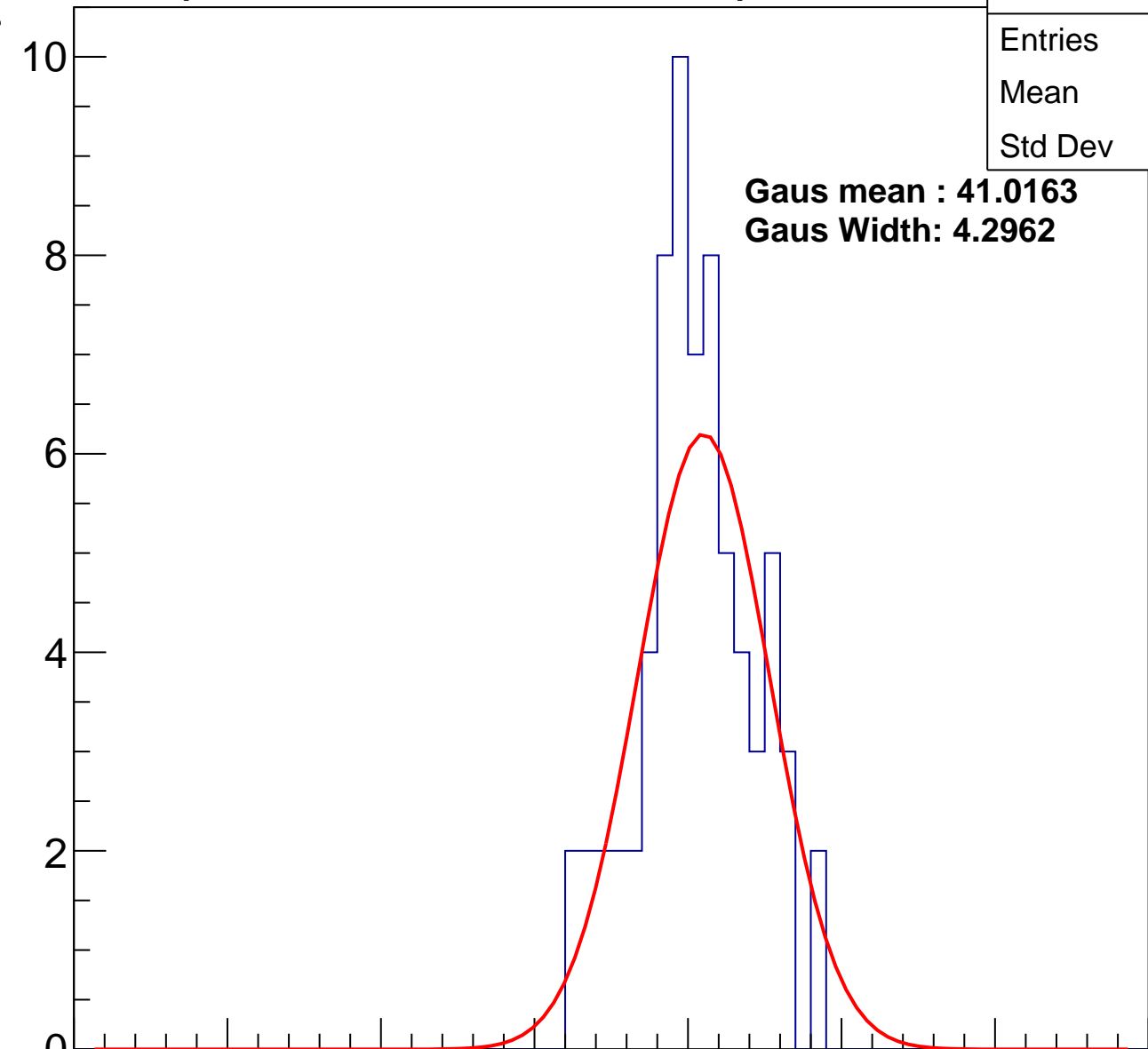
**Gaus Width: 4.2962**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

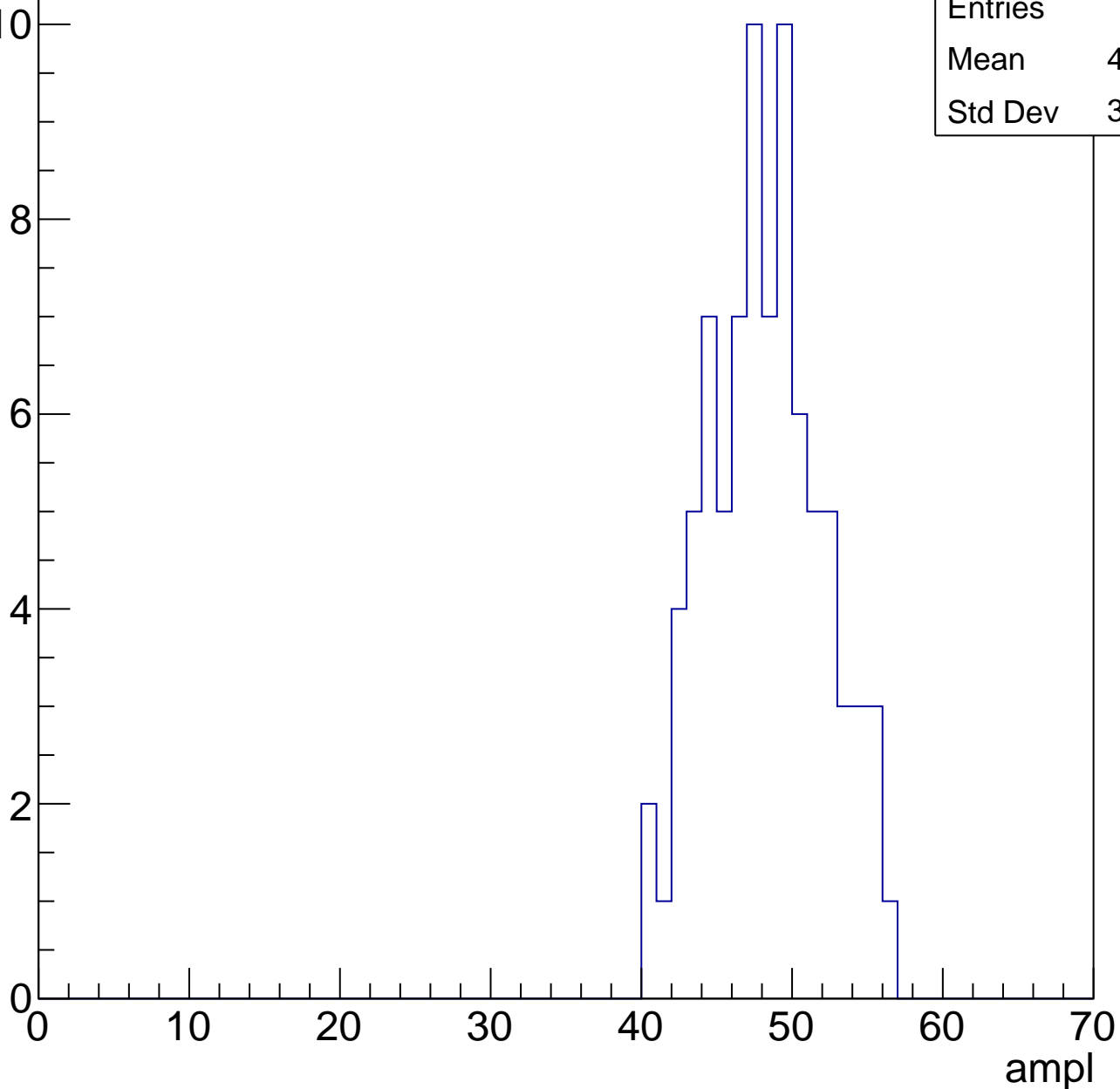


# B1L102S, U3-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	47.76
Std Dev	3.763

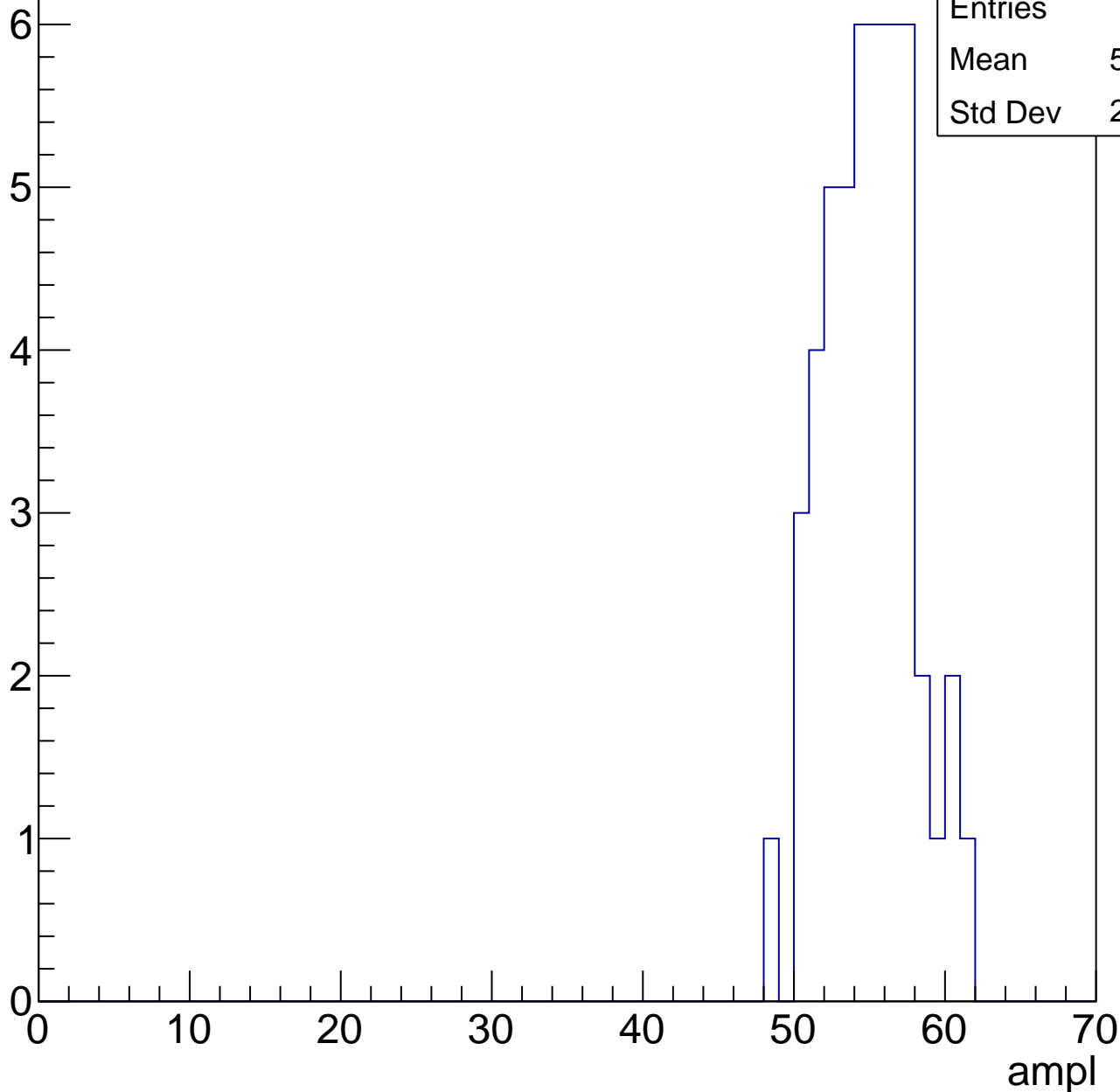


# B1L102S, U3-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

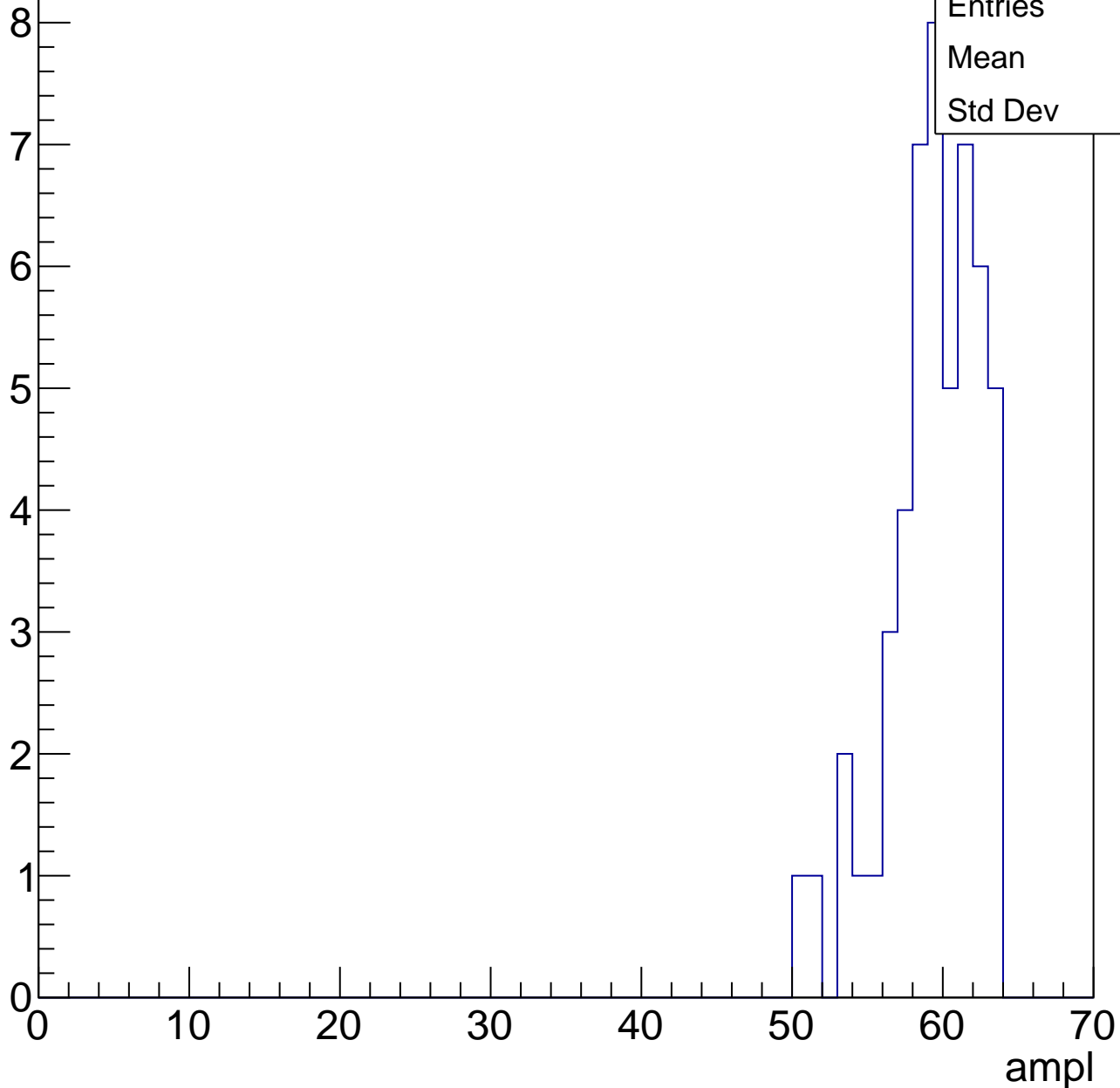
Entries	48
Mean	54.48
Std Dev	2.872



# B1L102S, U3-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

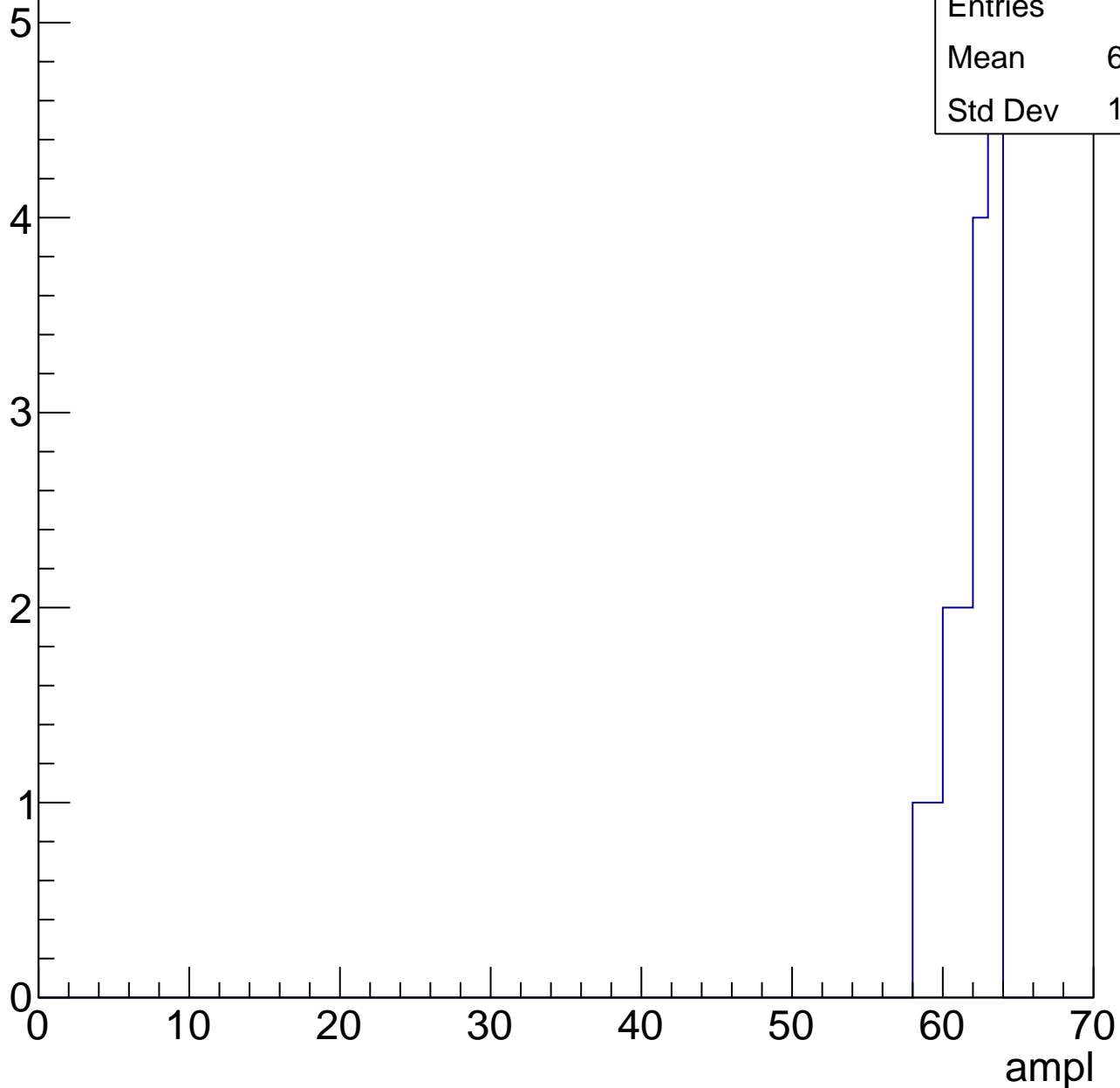


# B1L102S, U3-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	15
Mean	61.47
Std Dev	1.543

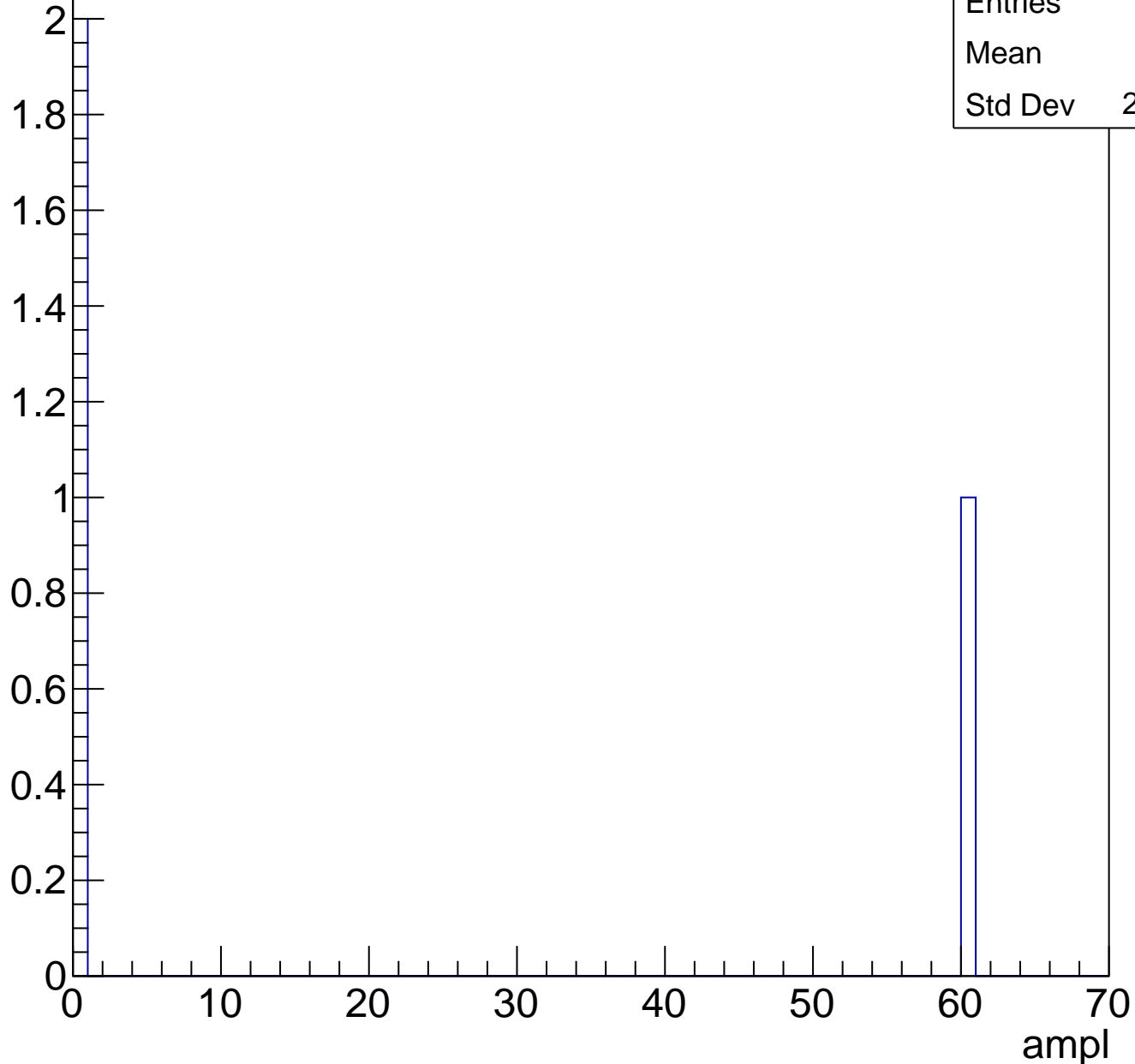




# B1L102S, U3-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	20
Std Dev	28.28

# B1L102S, U3-ch2, adc0

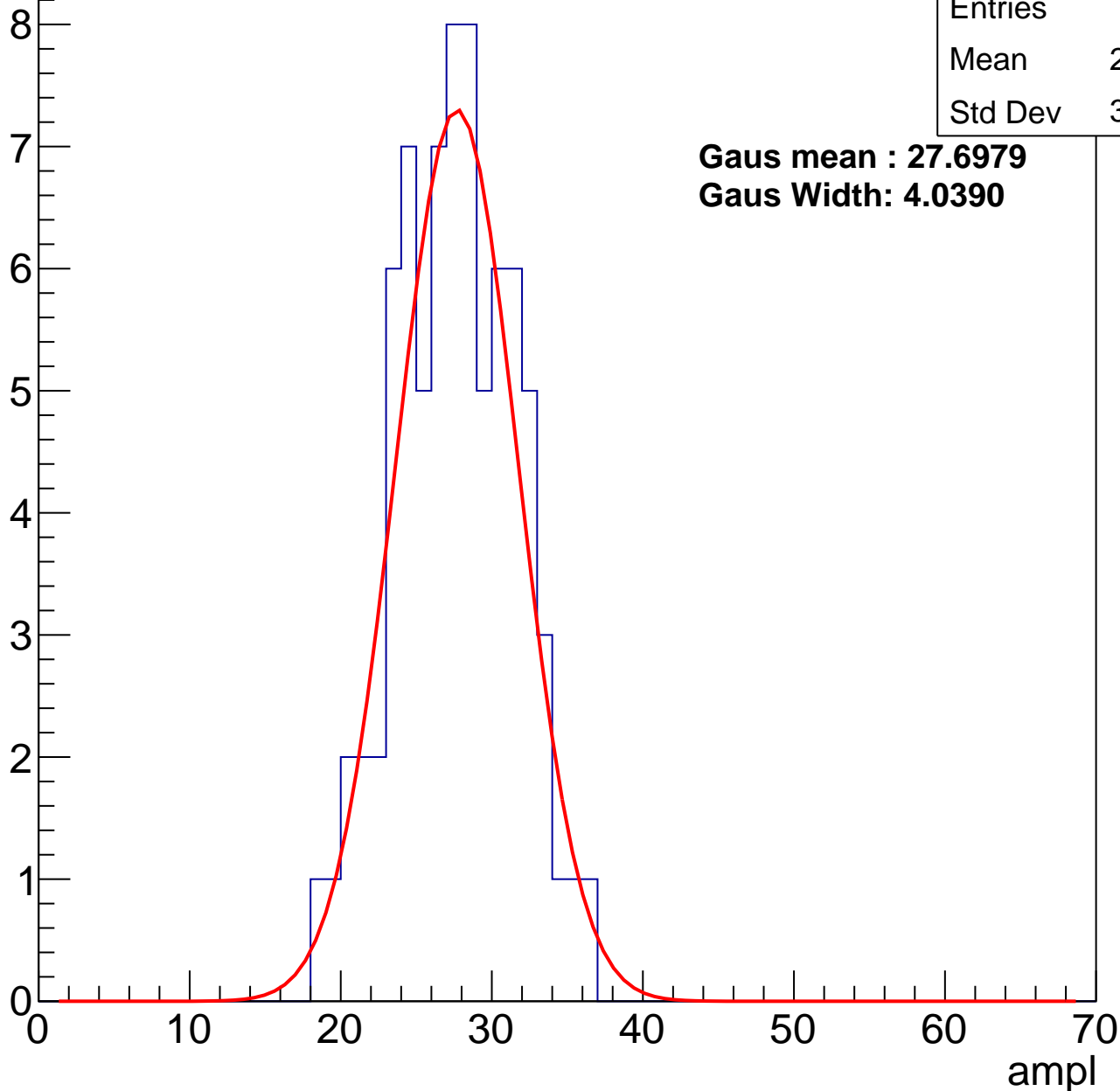
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	27.16
Std Dev	3.872

**Gaus mean : 27.6979**

**Gaus Width: 4.0390**



# B1L102S, U3-ch2, adc1

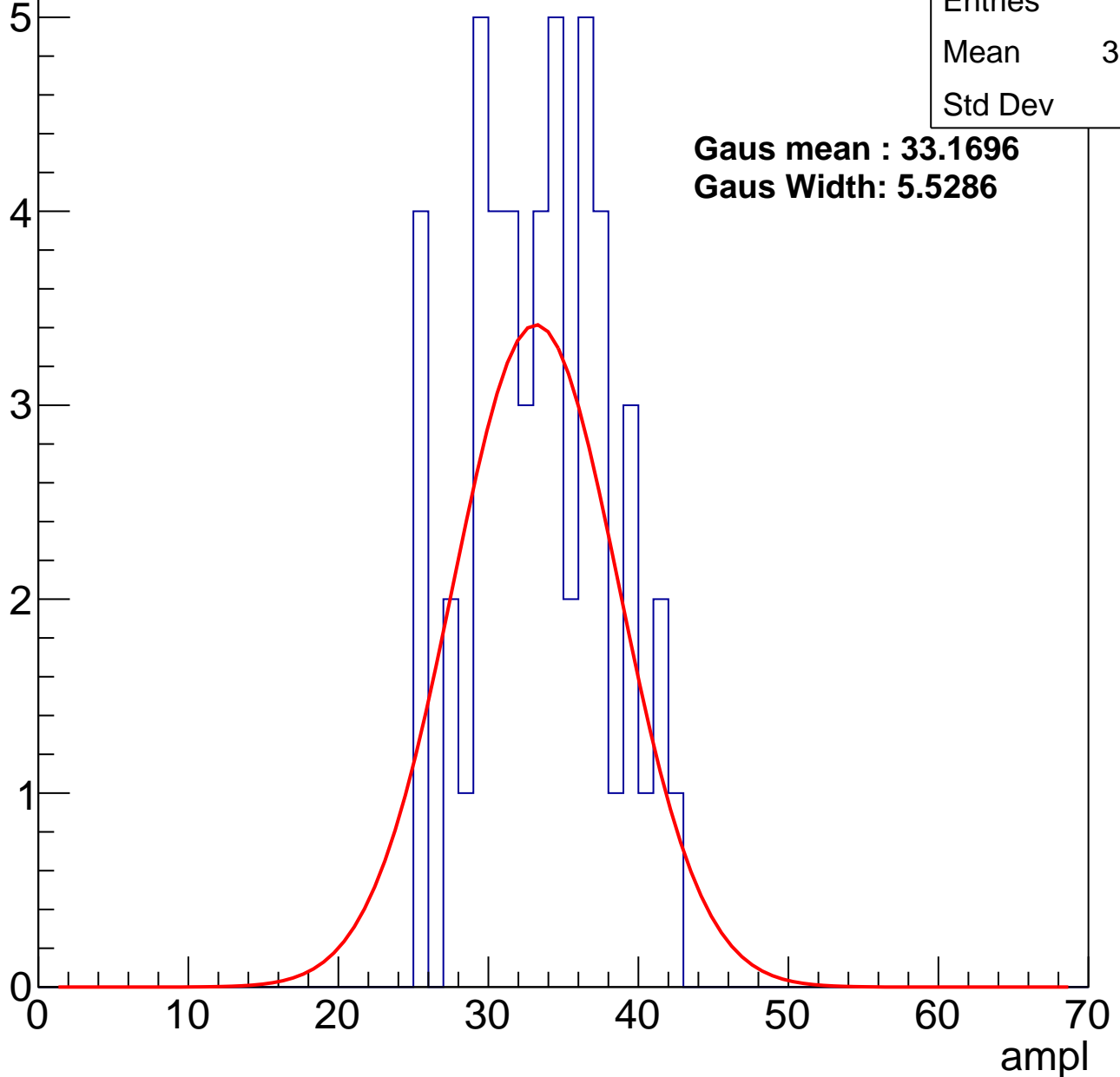
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	33.06
Std Dev	4.43

**Gaus mean : 33.1696**

**Gaus Width: 5.5286**



# B1L102S, U3-ch2, adc2

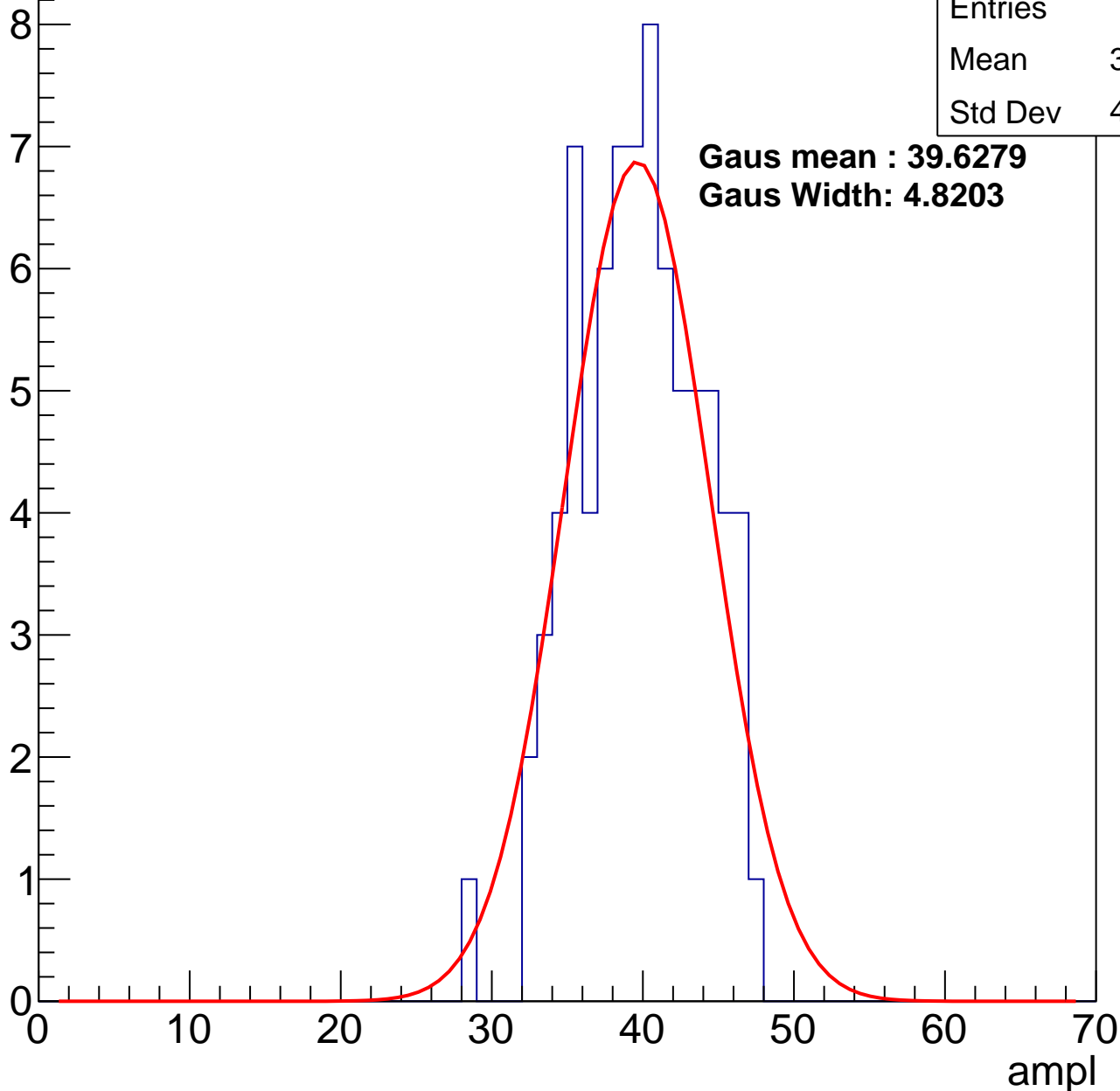
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	39.23
Std Dev	4.038

**Gaus mean : 39.6279**

**Gaus Width: 4.8203**

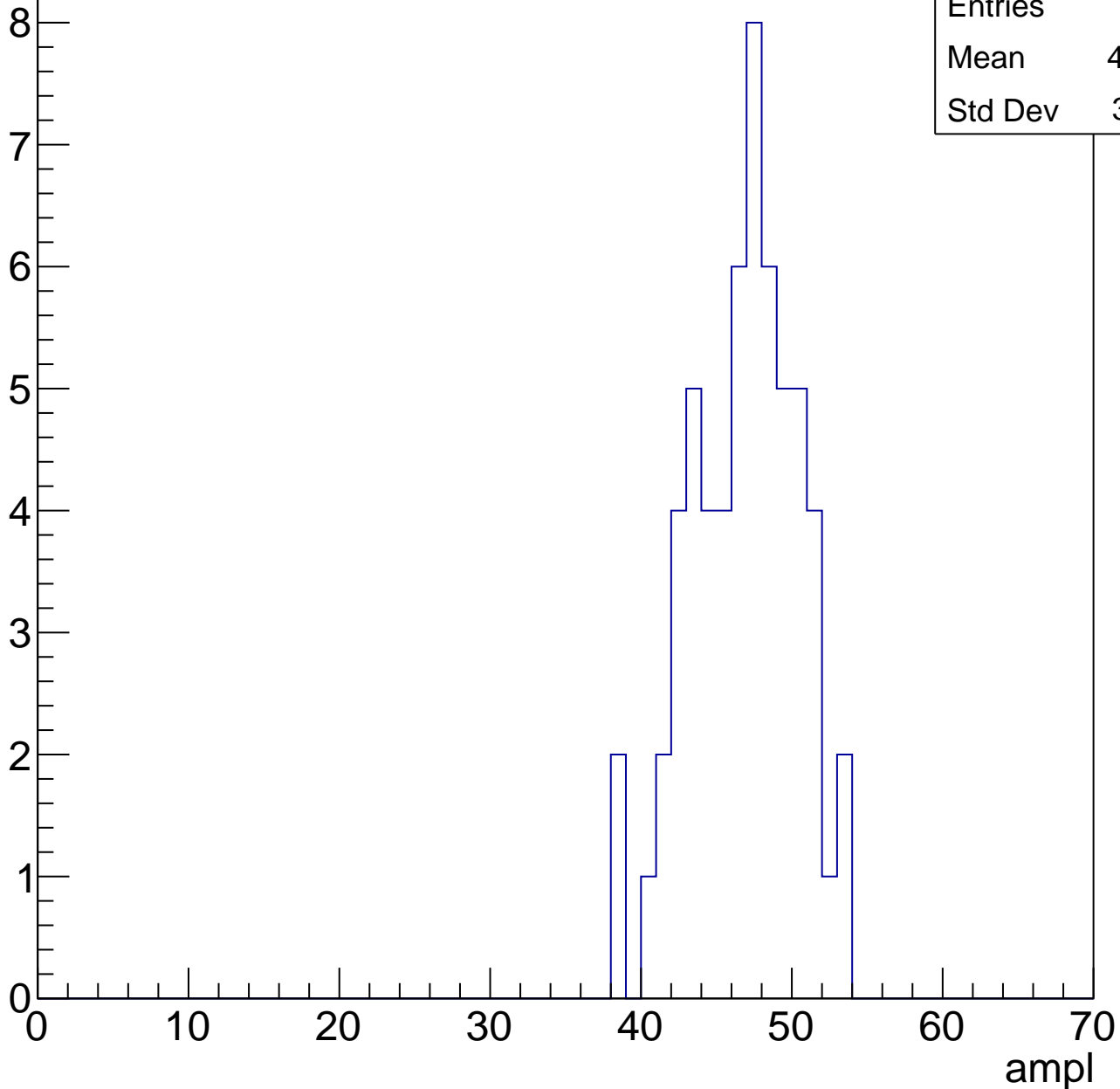


# B1L102S, U3-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	46.34
Std Dev	3.511

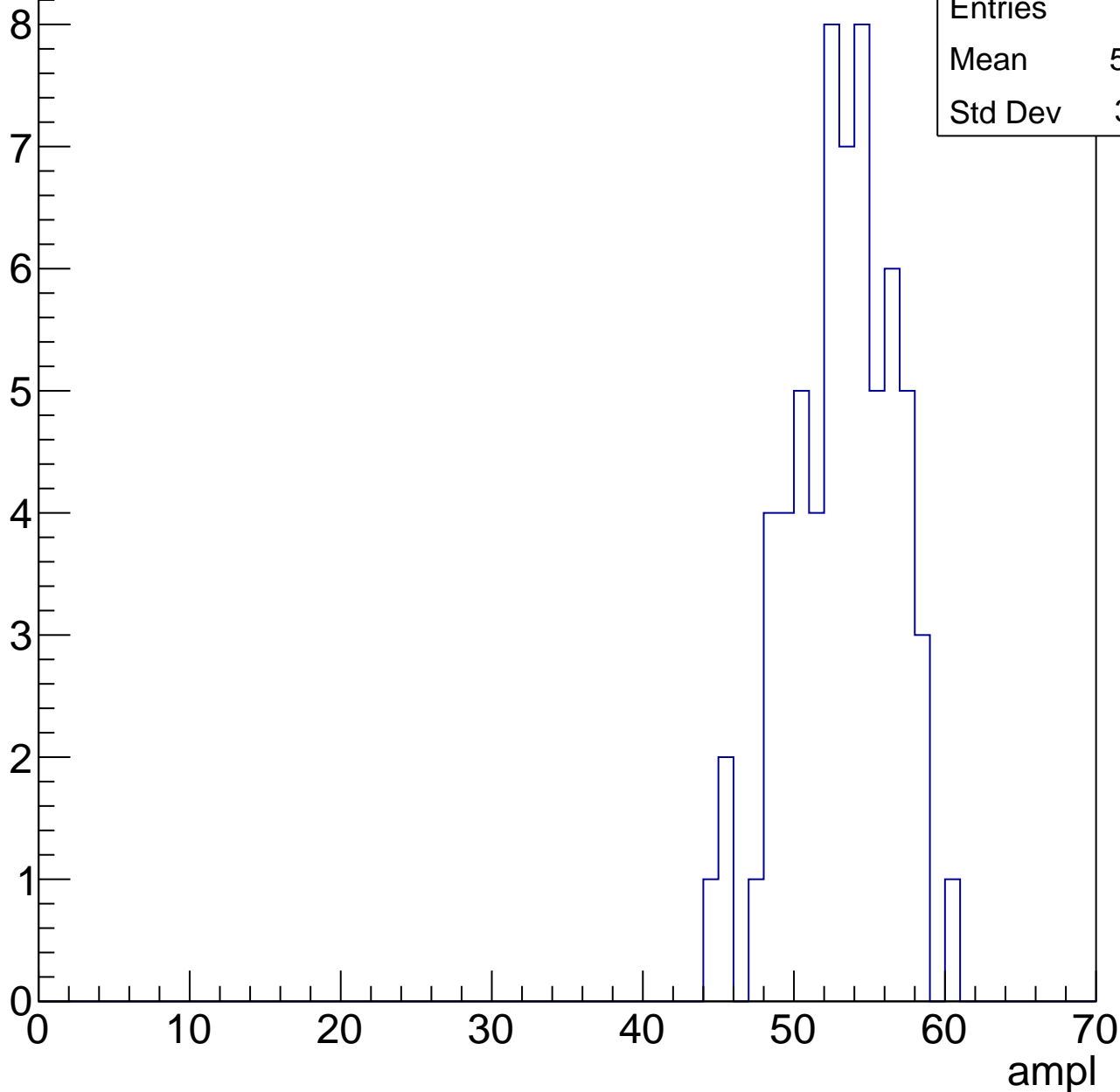


# B1L102S, U3-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	52.69
Std Dev	3.441

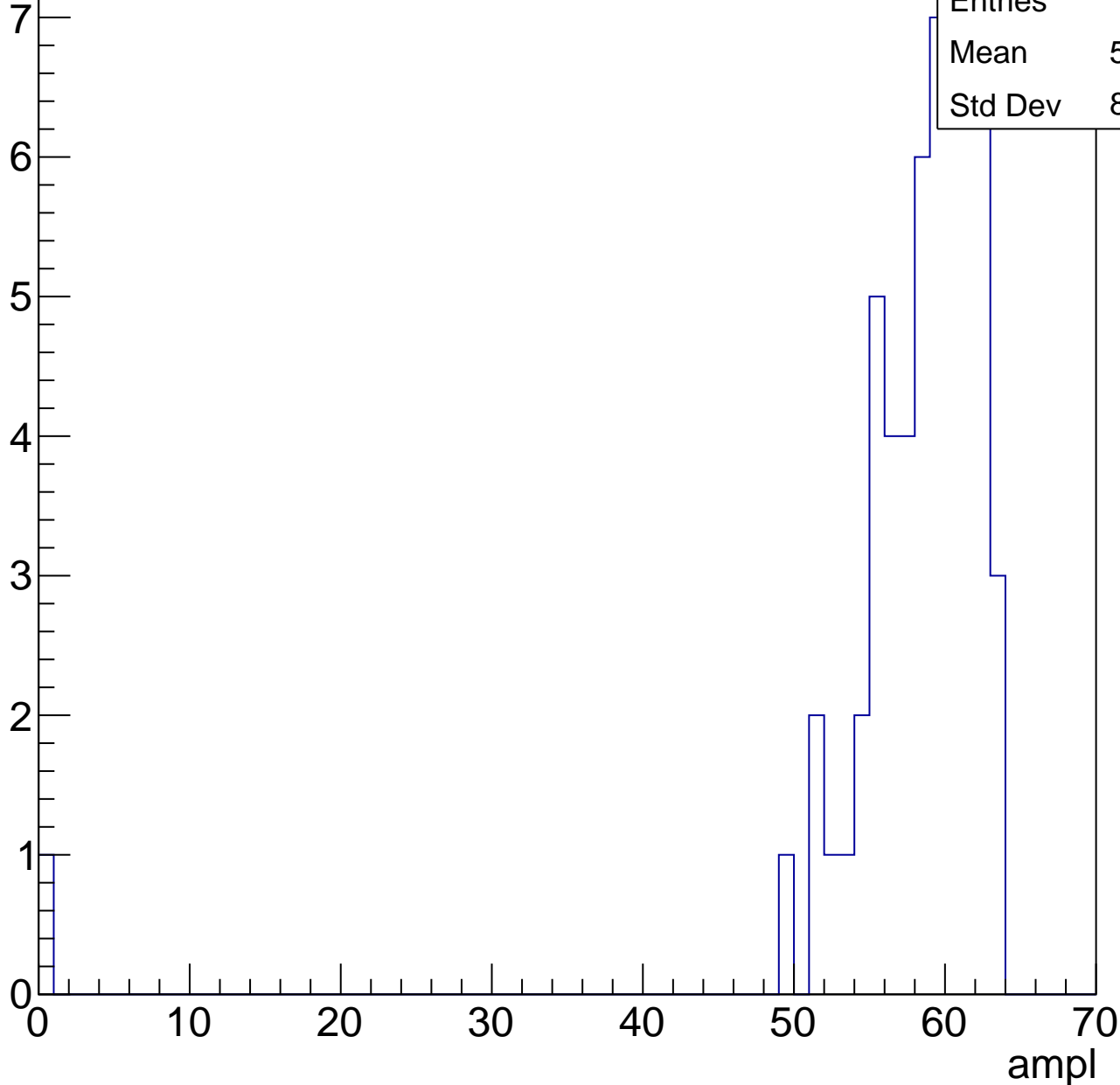


# B1L102S, U3-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	57.28
Std Dev	8.258

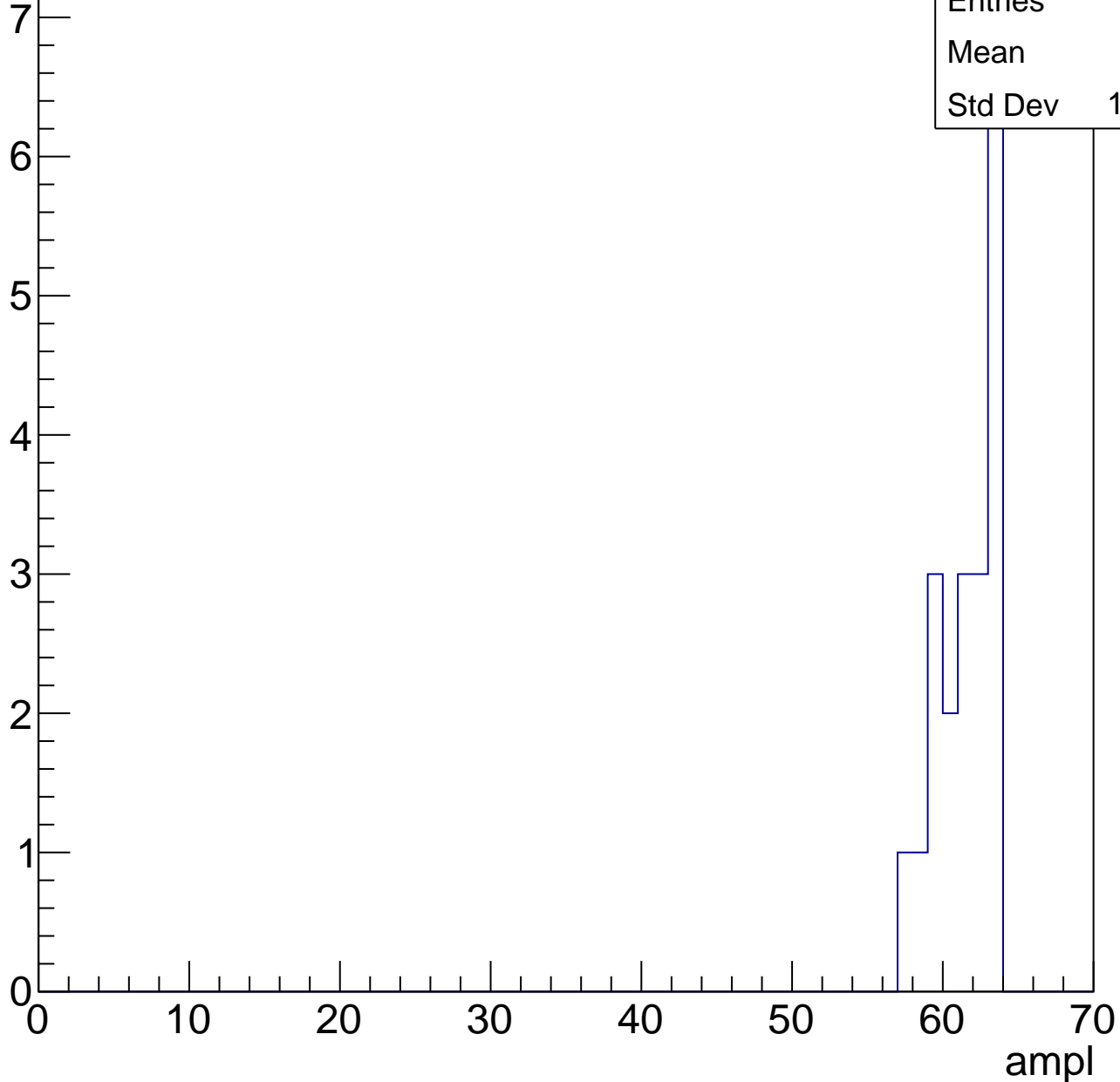


# B1L102S, U3-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	20
Mean	61.1
Std Dev	1.868





# B1L102S, U3-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U3-ch3, adc0

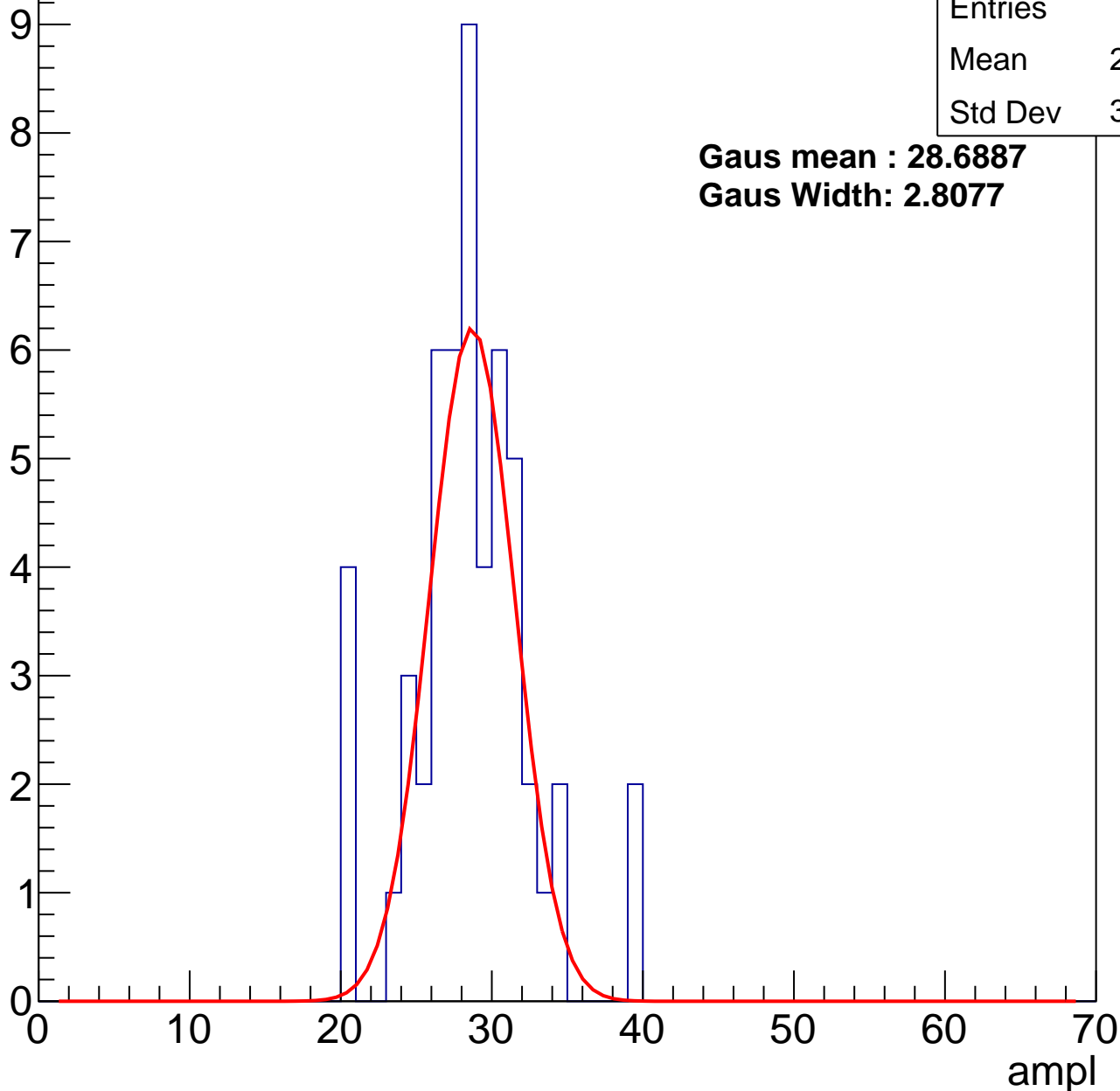
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	28.09
Std Dev	3.935

**Gaus mean : 28.6887**

**Gaus Width: 2.8077**



# B1L102S, U3-ch3, adc1

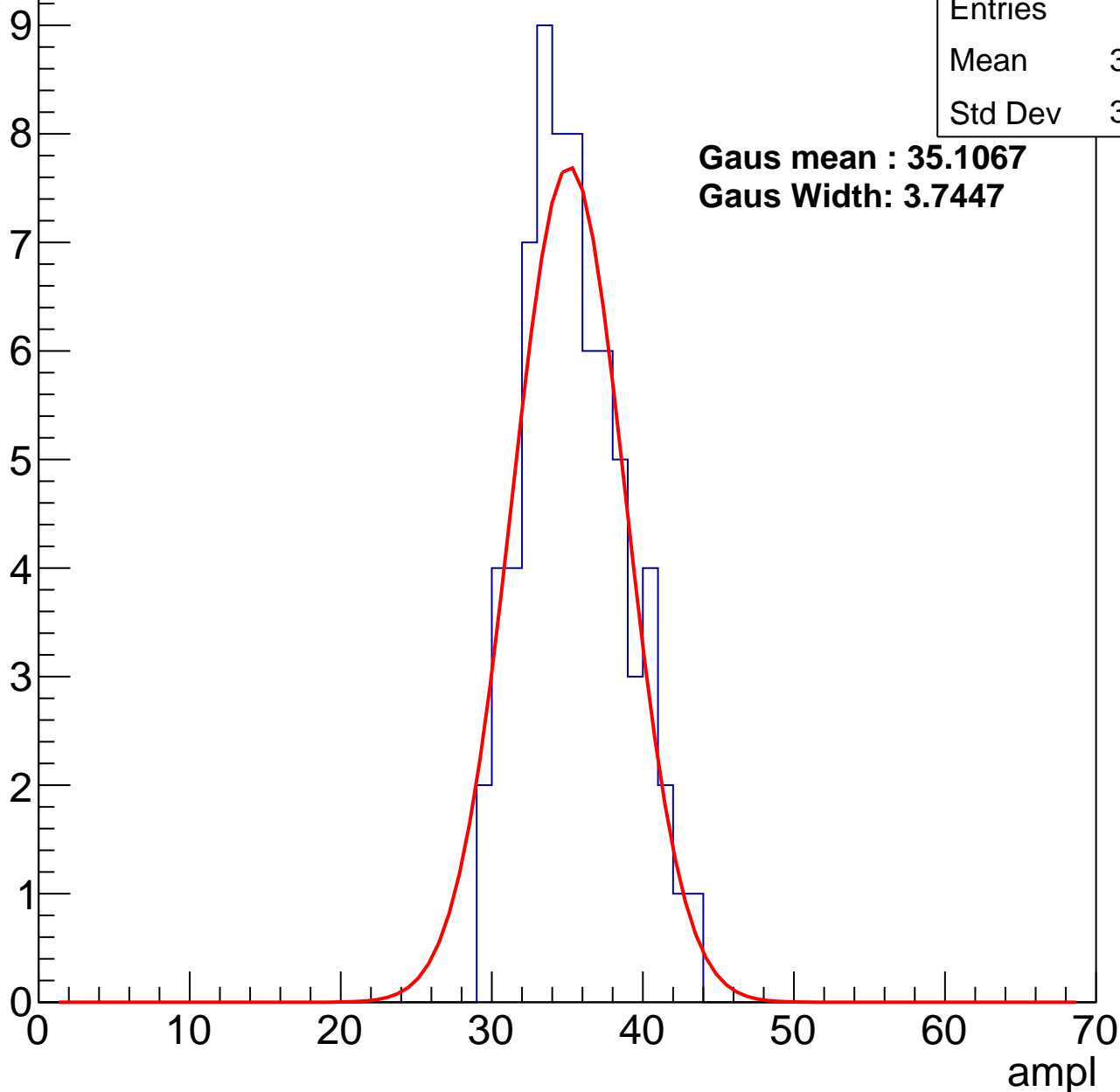
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	34.96
Std Dev	3.275

**Gaus mean : 35.1067**

**Gaus Width: 3.7447**



# B1L102S, U3-ch3, adc2

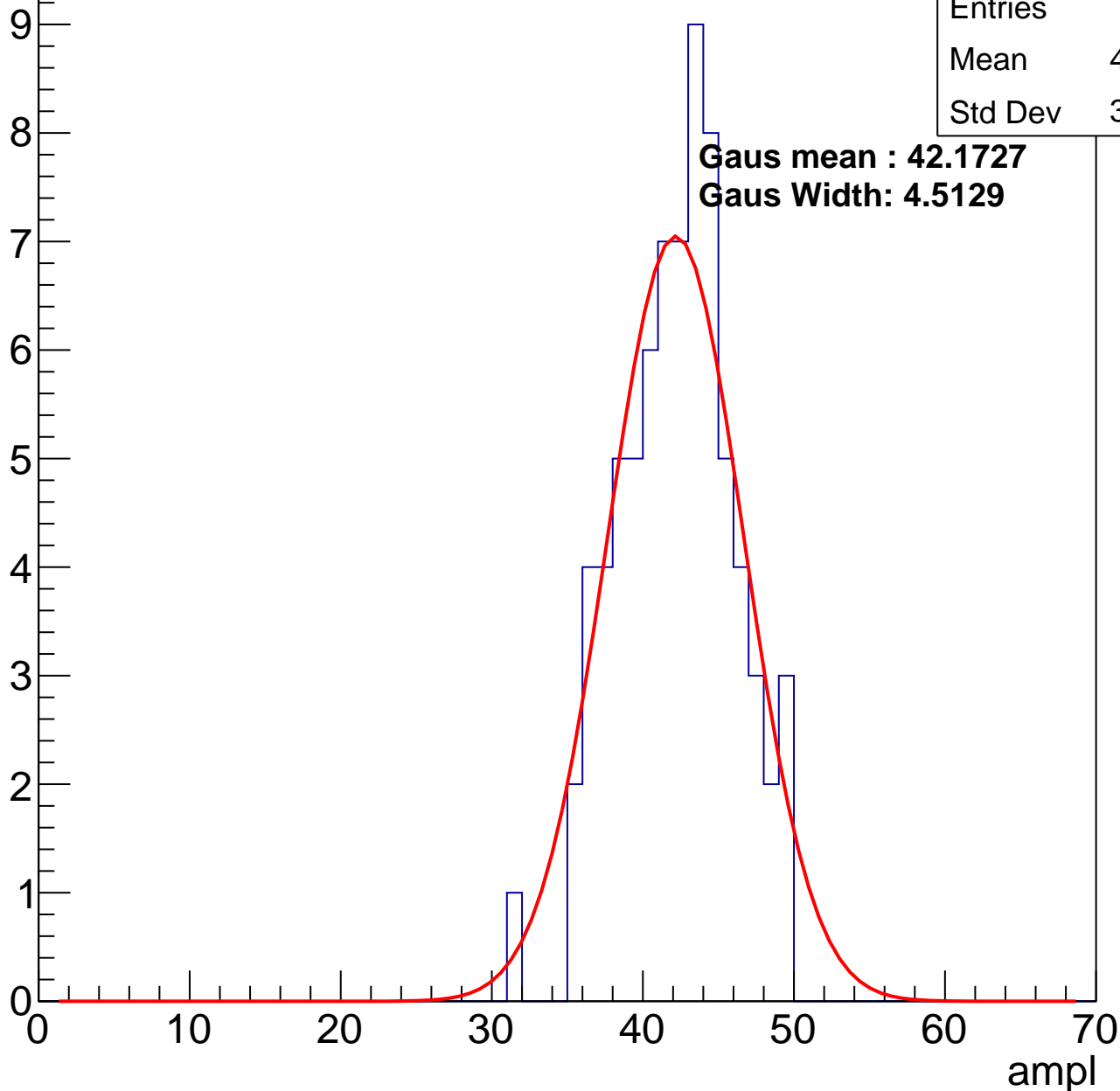
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	41.75
Std Dev	3.756

**Gaus mean : 42.1727**

**Gaus Width: 4.5129**

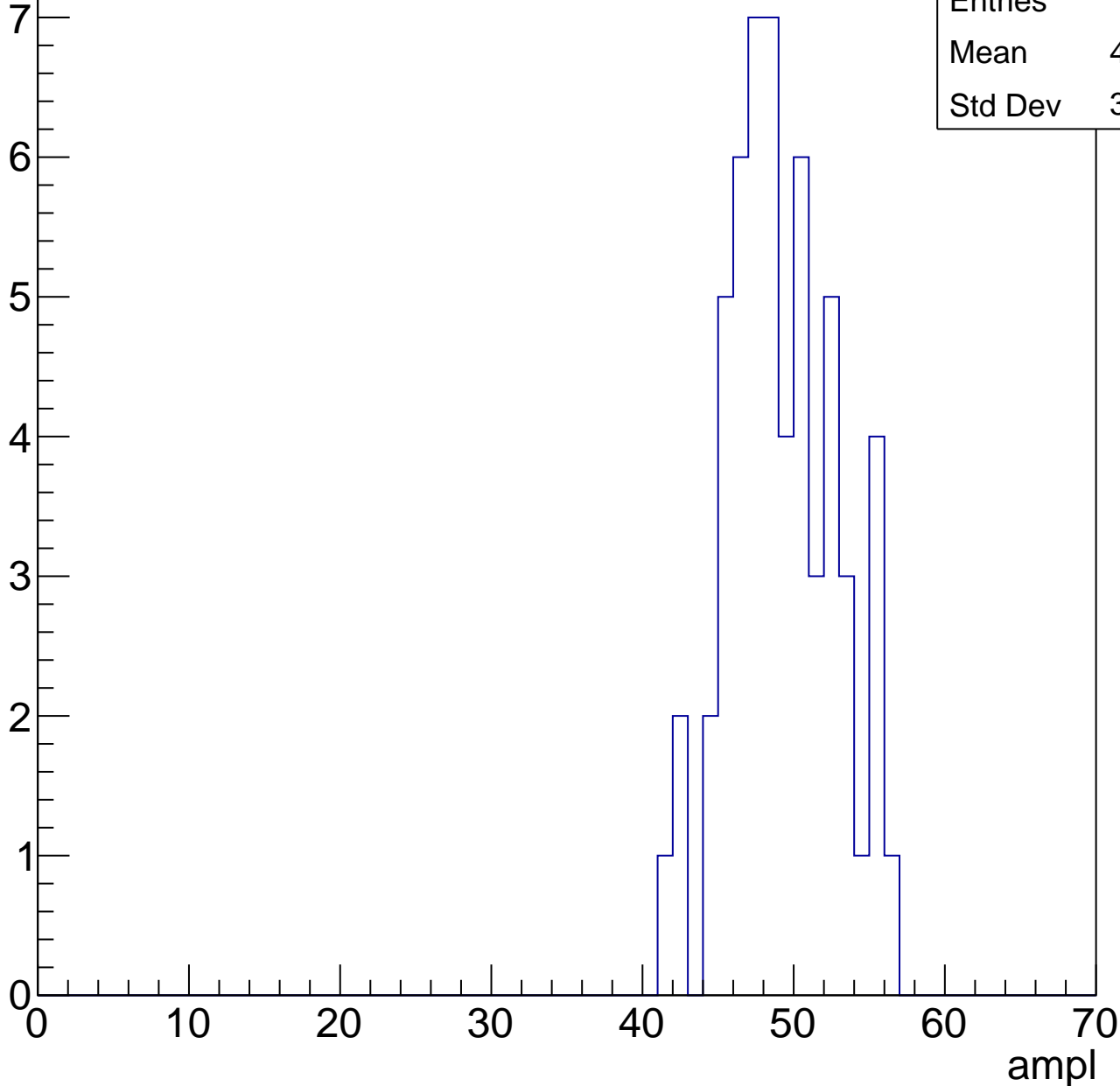


# B1L102S, U3-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

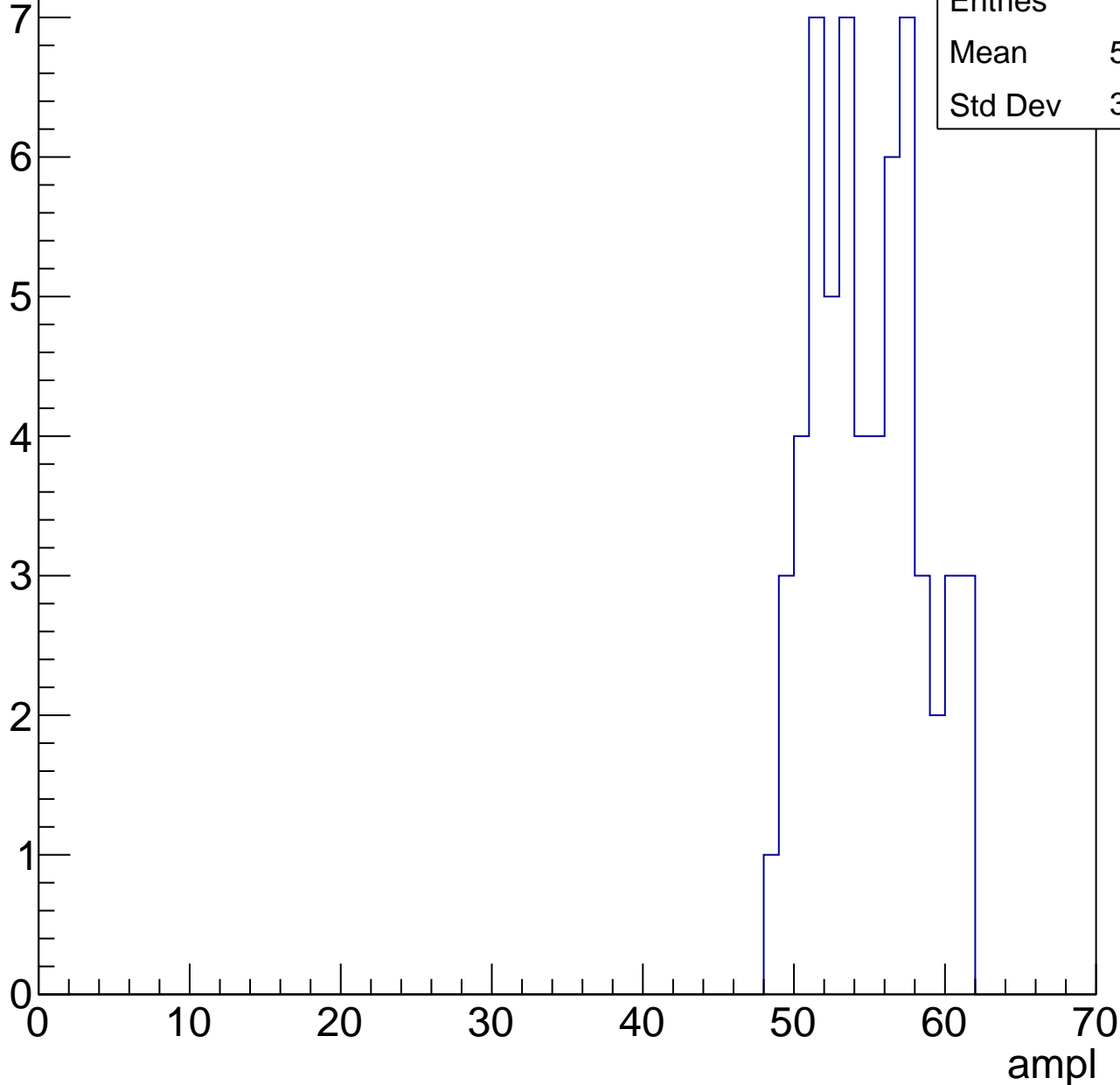
Entries	57
Mean	48.72
Std Dev	3.518



# B1L102S, U3-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



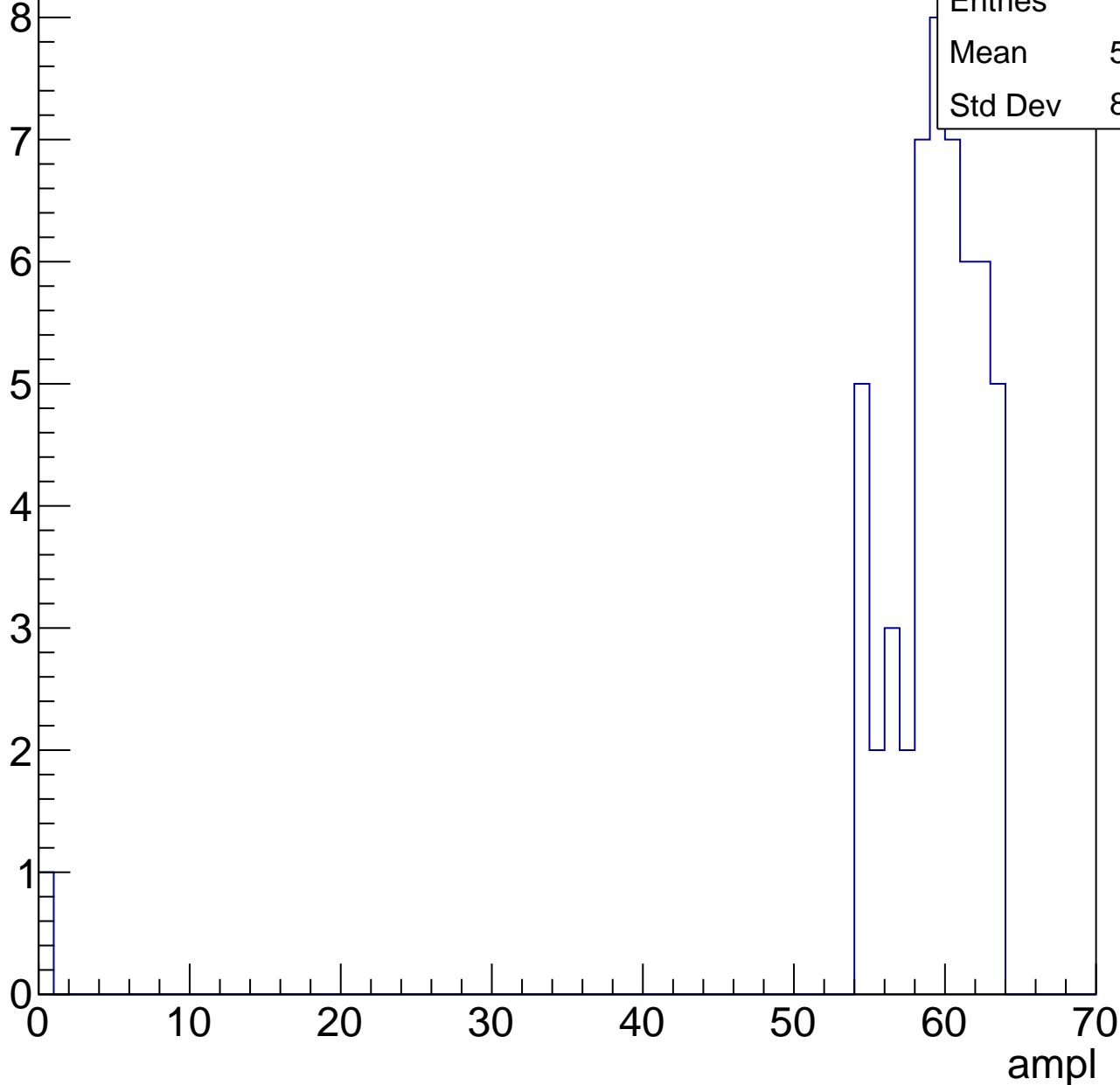
Entries	59
Mean	54.39
Std Dev	3.445

# B1L102S, U3-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	57.94
Std Dev	8.534

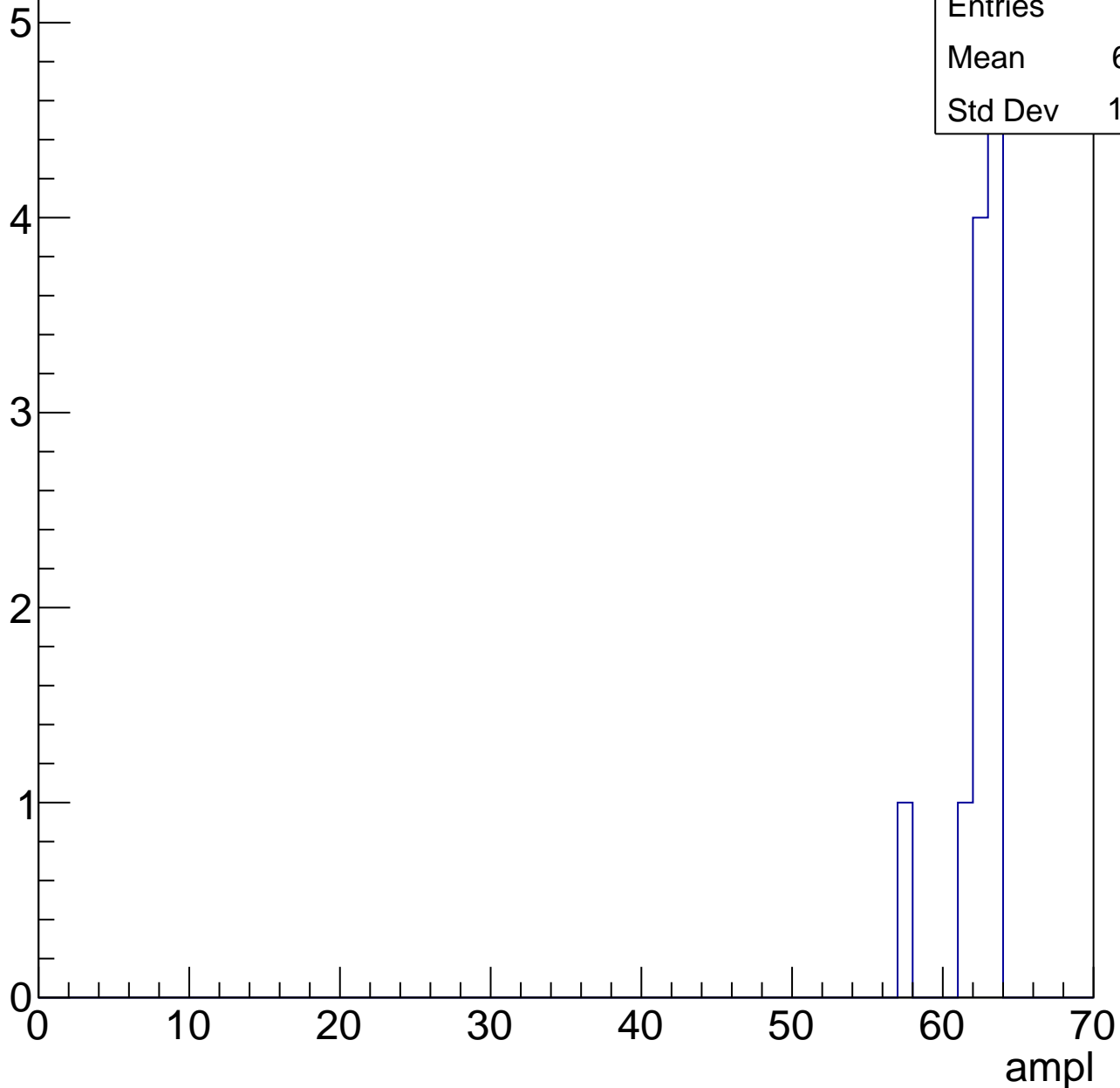


# B1L102S, U3-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	11
Mean	61.91
Std Dev	1.676





# B1L102S, U3-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U3-ch4, adc0

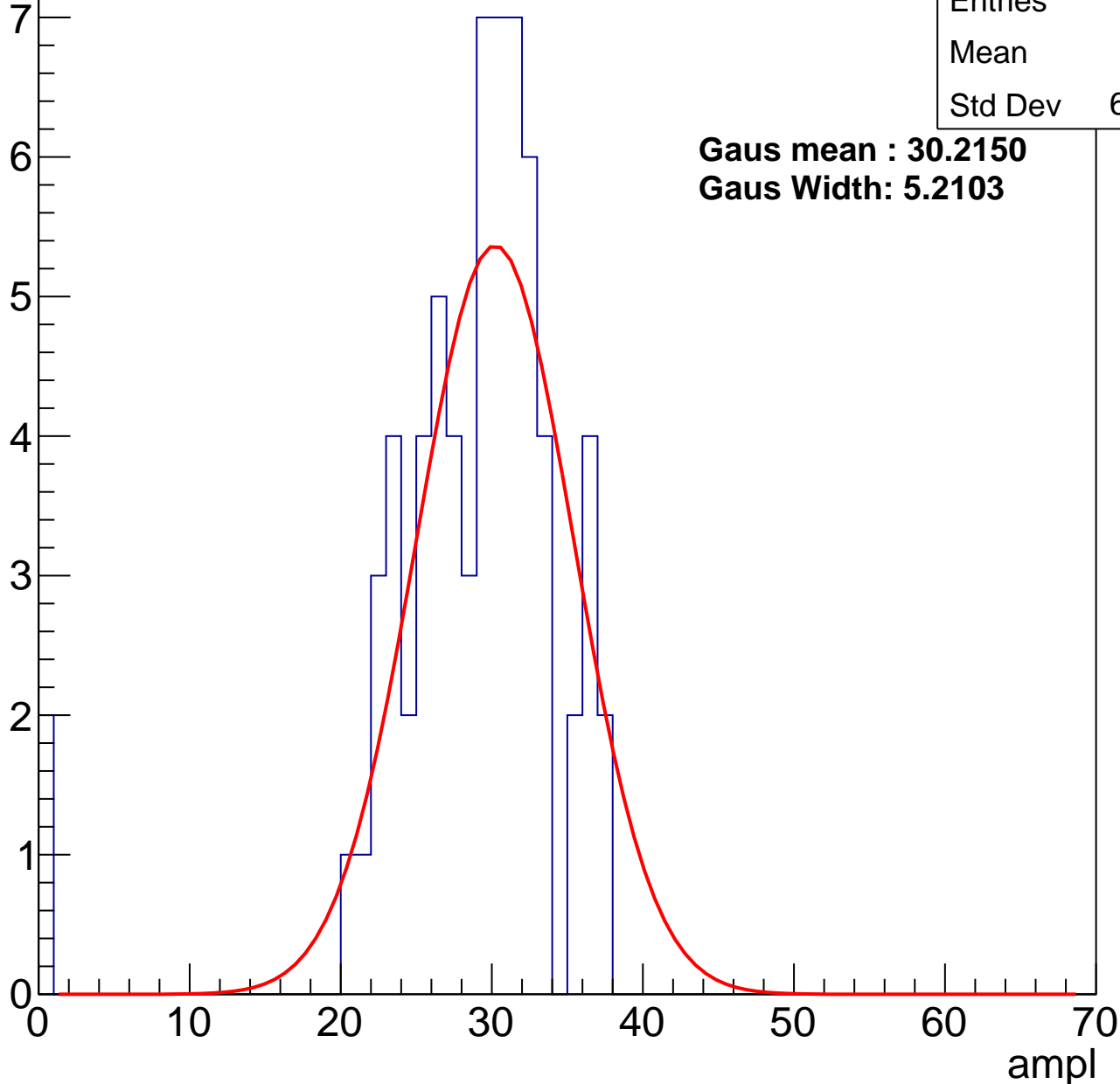
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	28.1
Std Dev	6.406

**Gaus mean : 30.2150**

**Gaus Width: 5.2103**



# B1L102S, U3-ch4, adc1

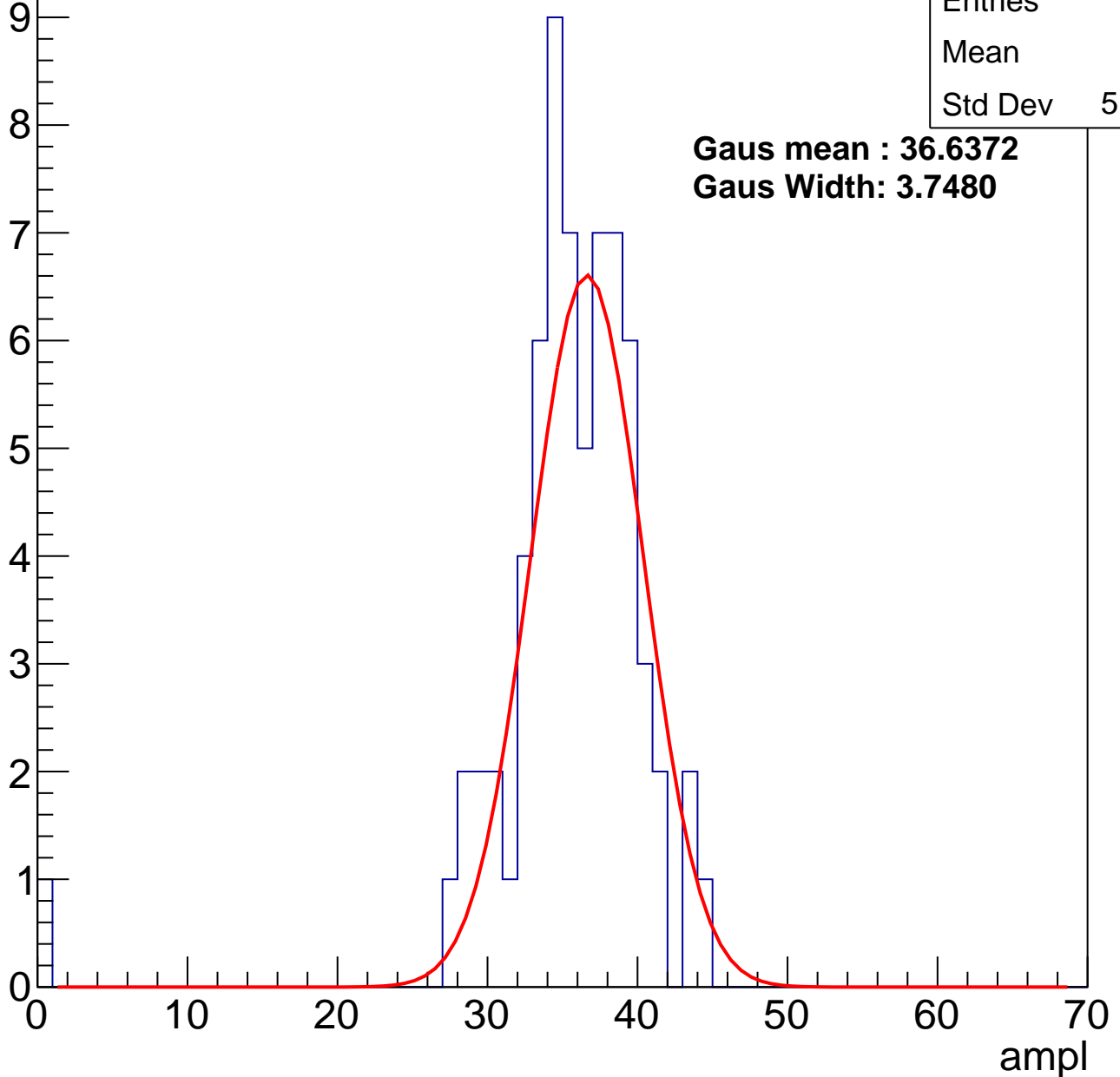
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	35
Std Dev	5.612

**Gaus mean : 36.6372**

**Gaus Width: 3.7480**



# B1L102S, U3-ch4, adc2

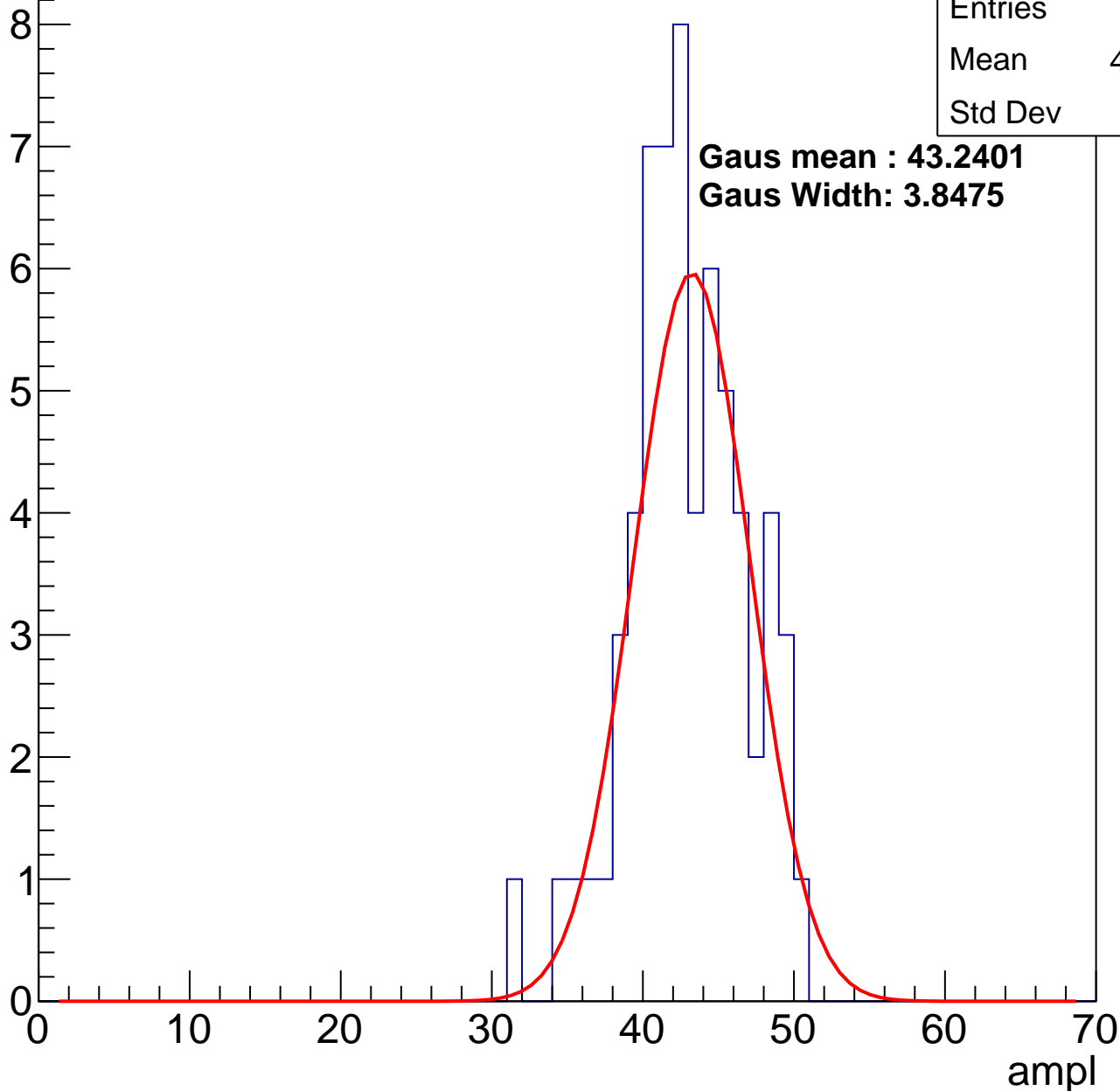
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	42.44
Std Dev	3.87

**Gaus mean : 43.2401**

**Gaus Width: 3.8475**

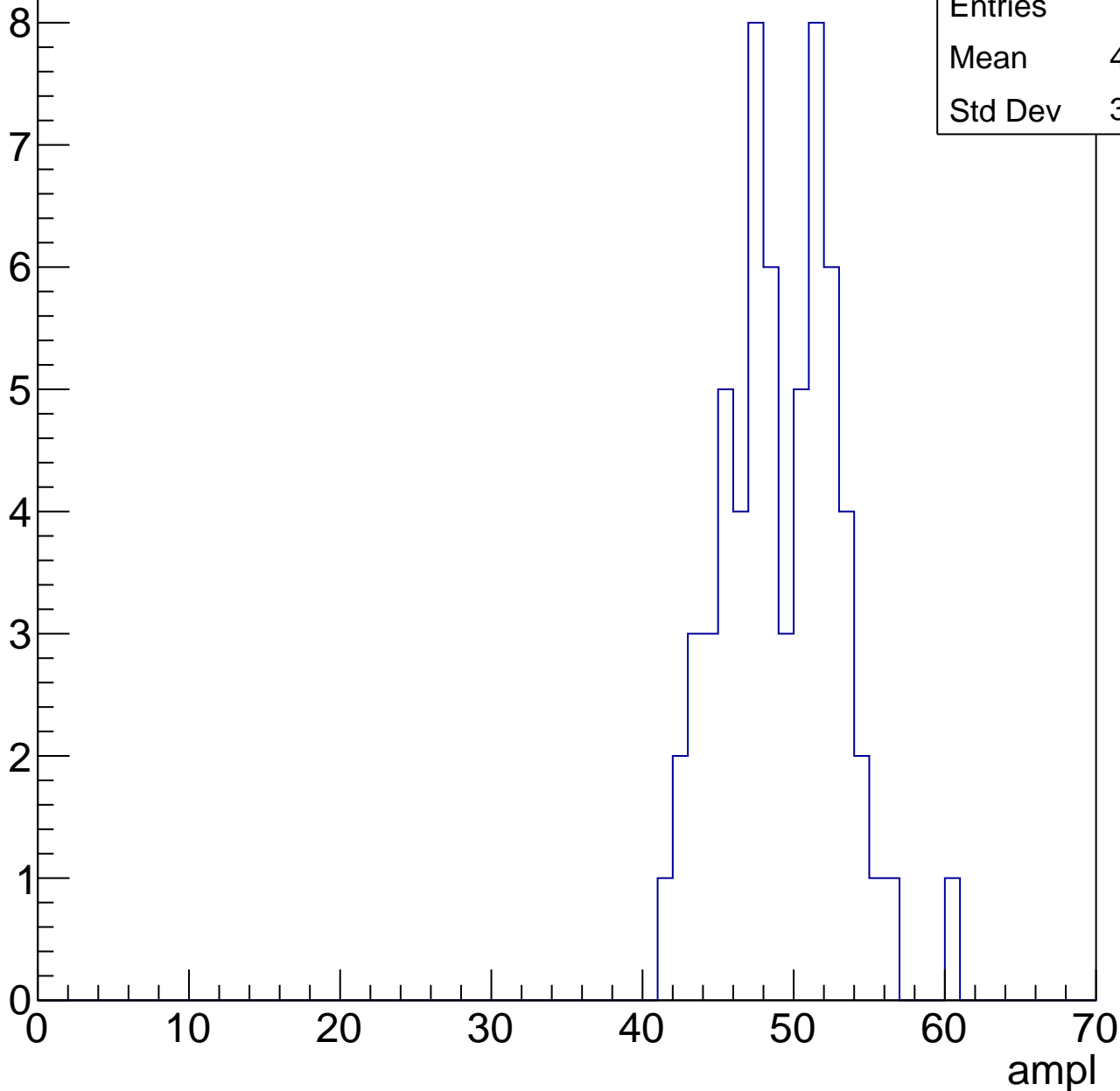


# B1L102S, U3-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	48.68
Std Dev	3.787

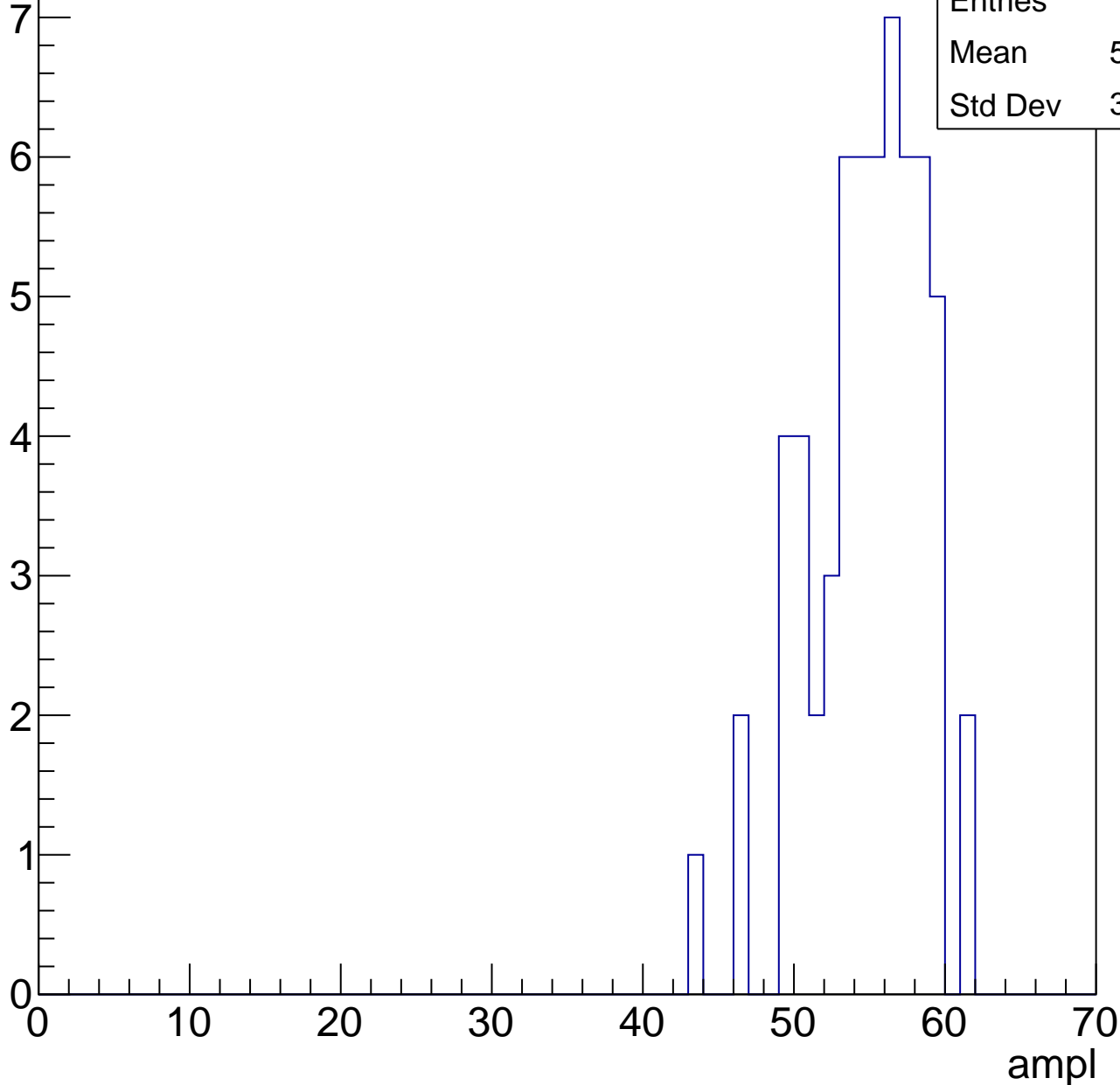


# B1L102S, U3-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	54.33
Std Dev	3.762

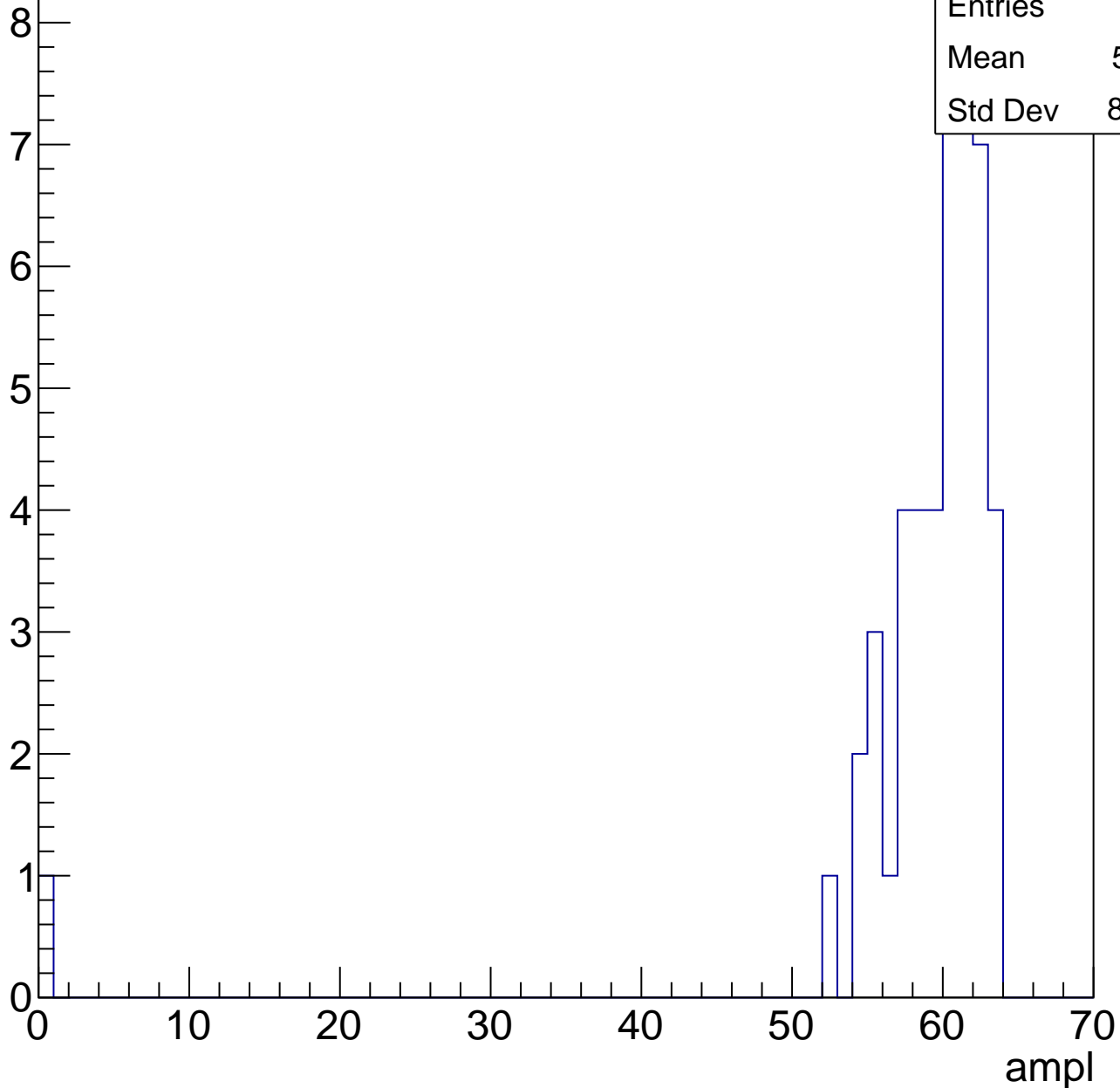


# B1L102S, U3-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	58.11
Std Dev	8.976

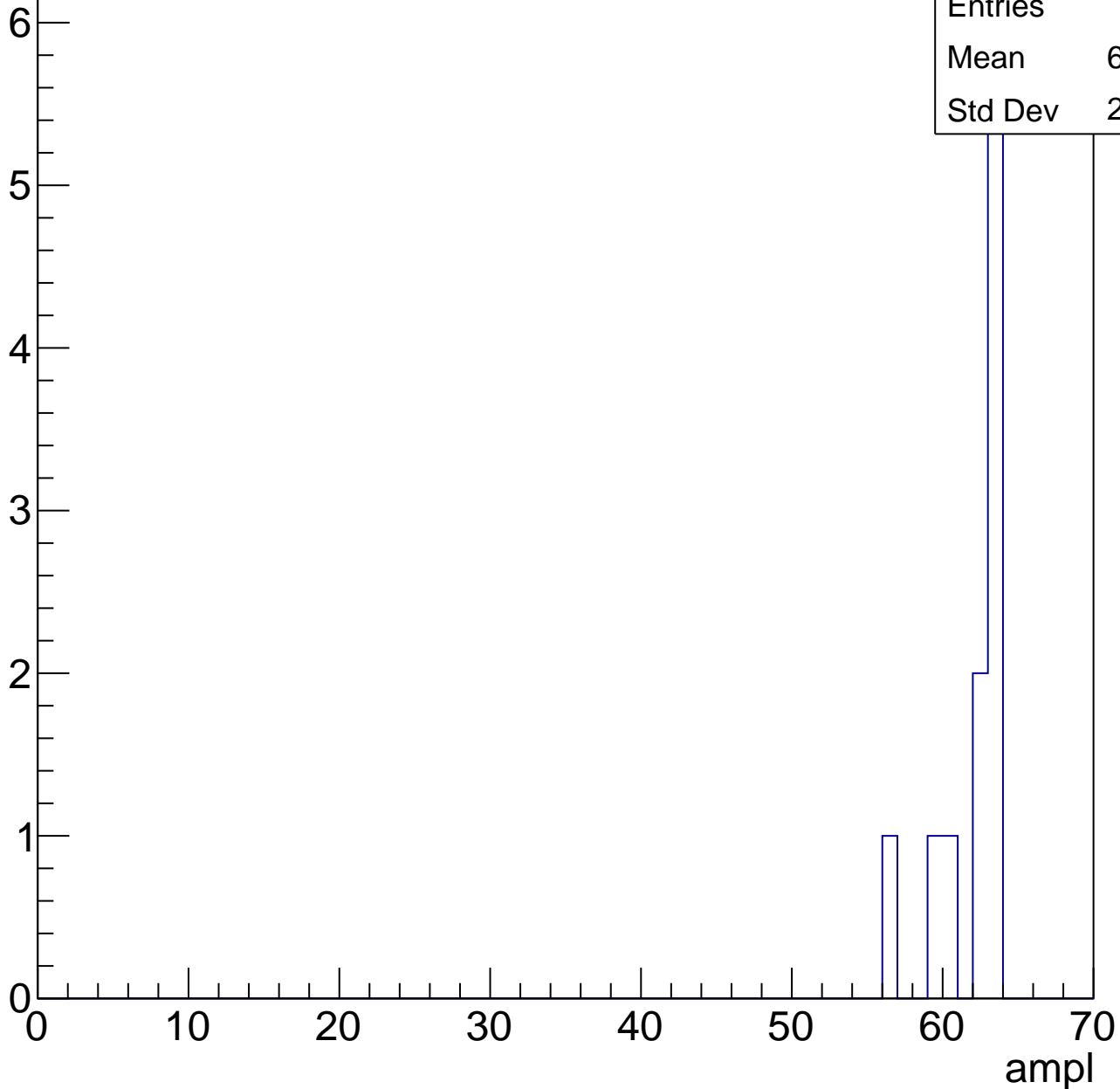


# B1L102S, U3-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	11
Mean	61.55
Std Dev	2.189





# B1L102S, U3-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch5, adc0

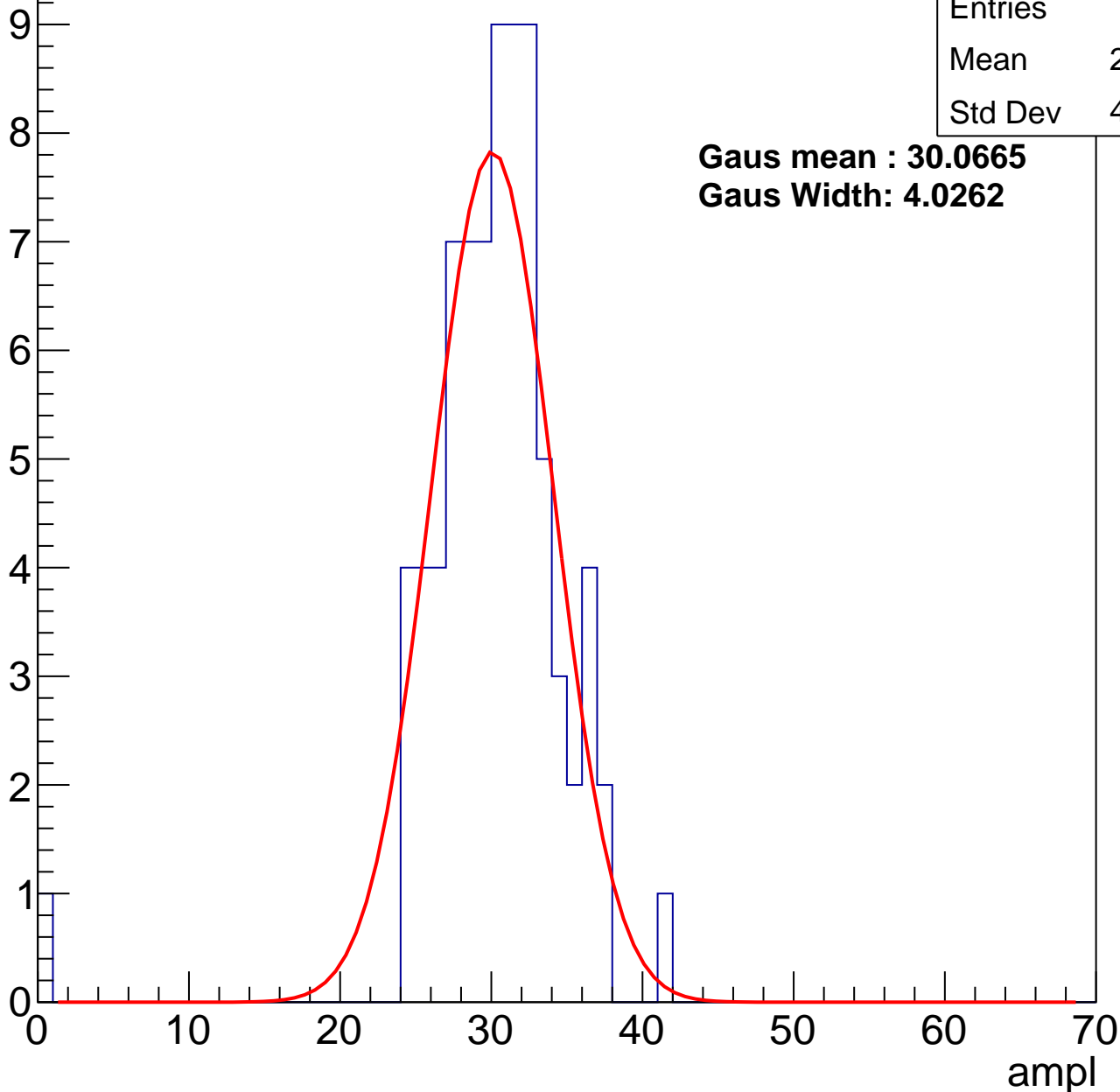
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	29.76
Std Dev	4.873

**Gaus mean : 30.0665**

**Gaus Width: 4.0262**



# B1L102S, U3-ch5, adc1

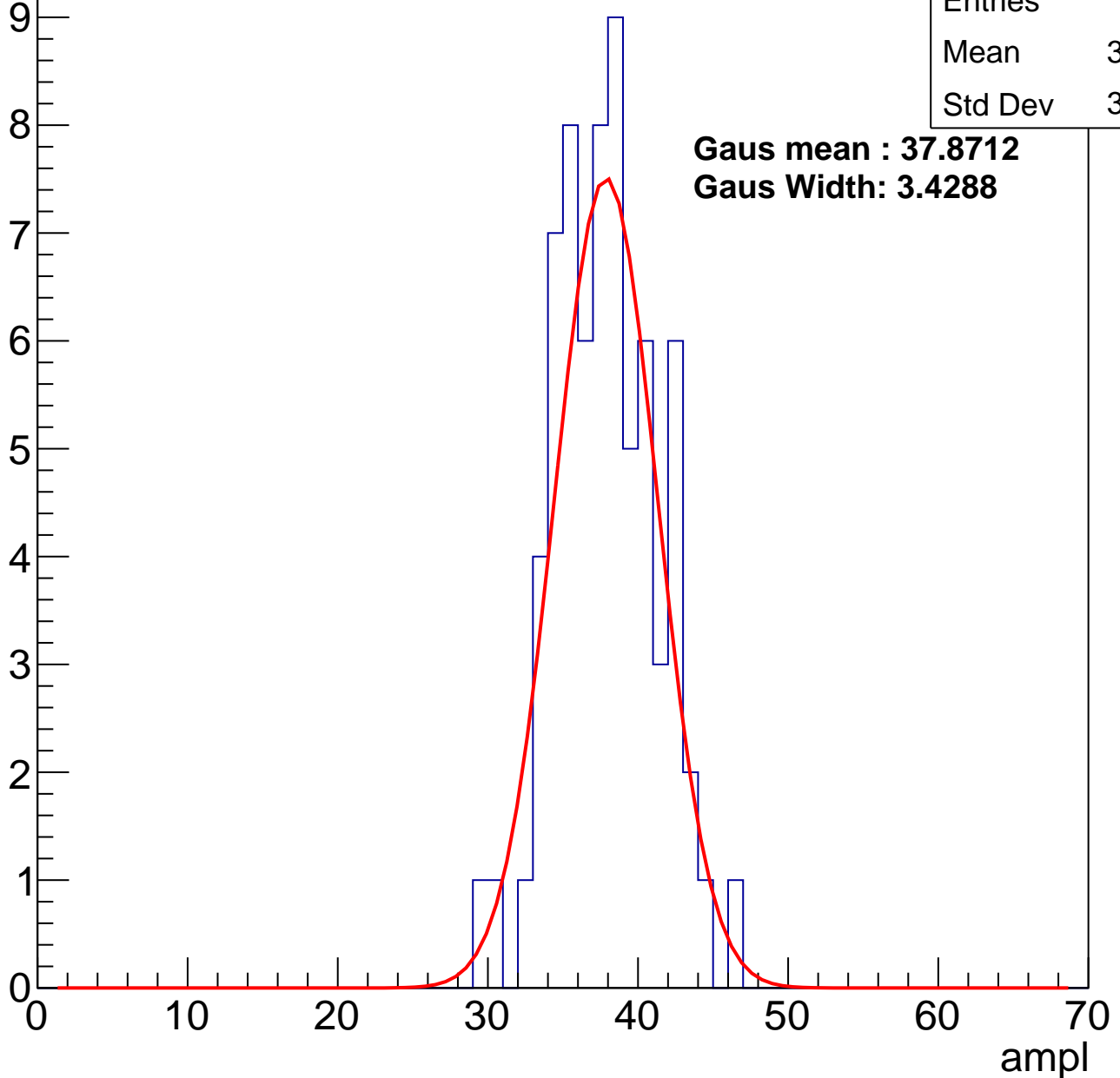
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	37.41
Std Dev	3.351

**Gaus mean : 37.8712**

**Gaus Width: 3.4288**



# B1L102S, U3-ch5, adc2

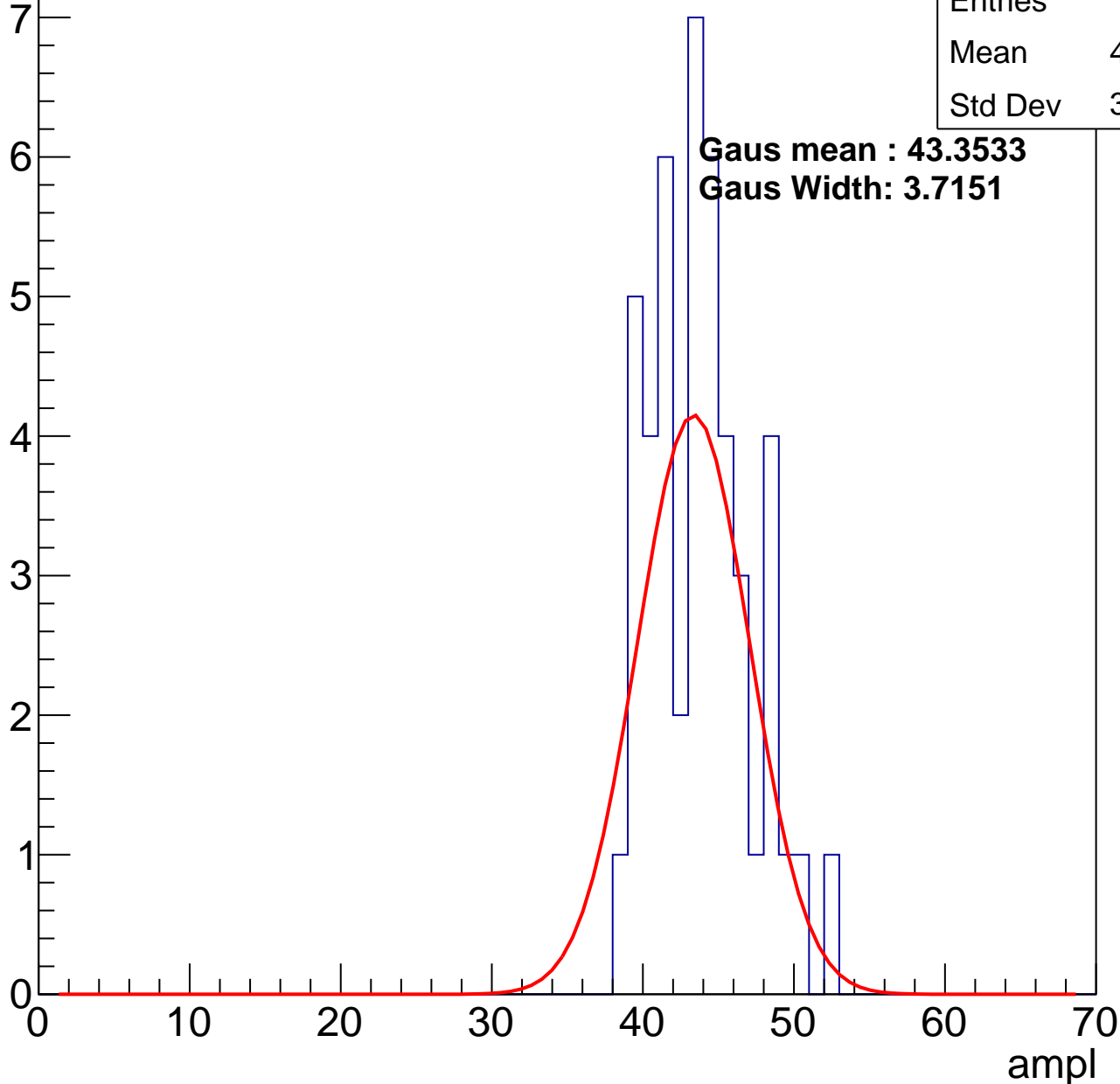
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	43.39
Std Dev	3.267

**Gaus mean : 43.3533**

**Gaus Width: 3.7151**

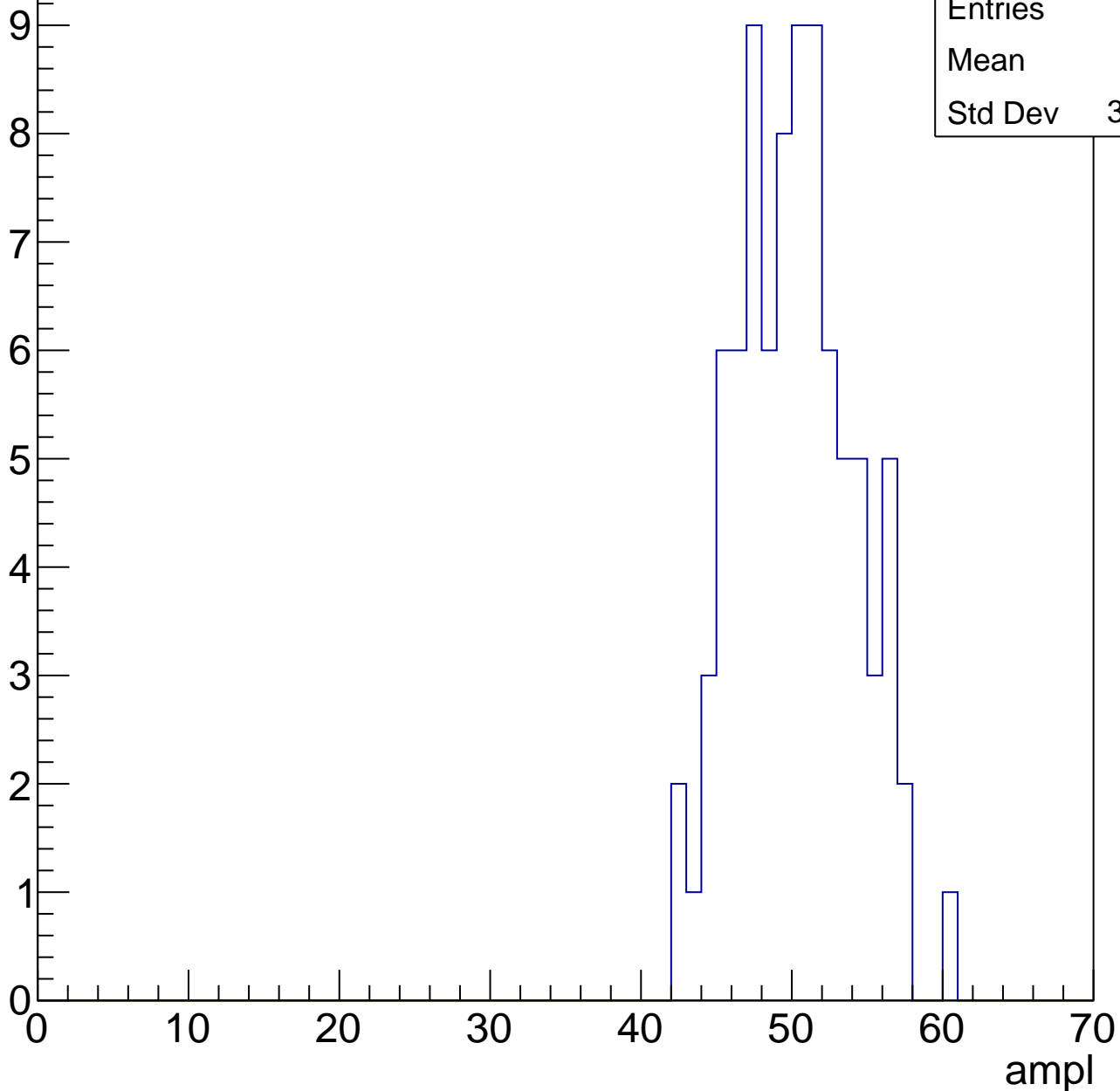


# B1L102S, U3-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	86
Mean	49.8
Std Dev	3.815

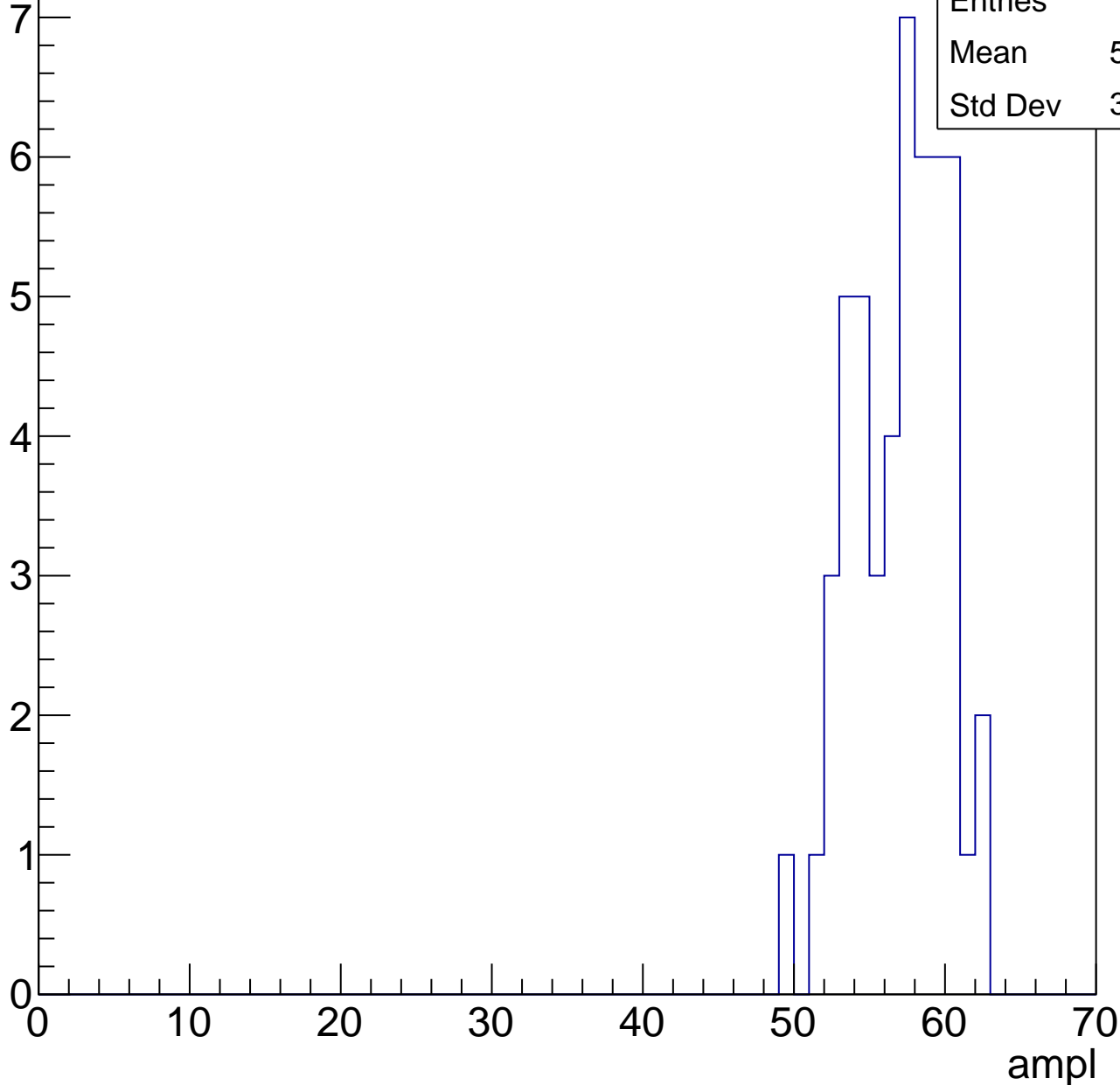


# B1L102S, U3-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	56.52
Std Dev	3.015

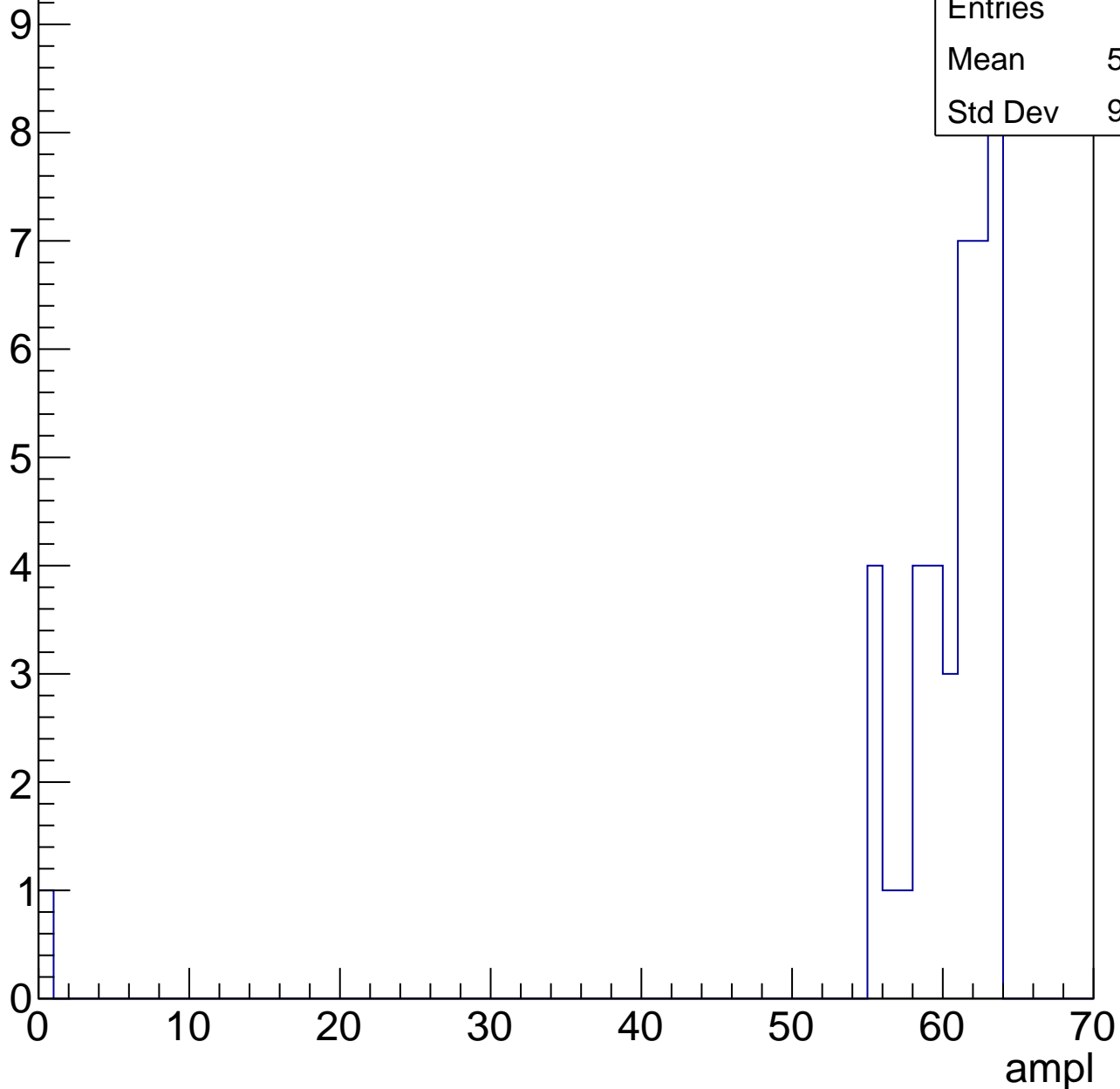


# B1L102S, U3-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	41
Mean	58.76
Std Dev	9.624



# B1L102S, U3-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

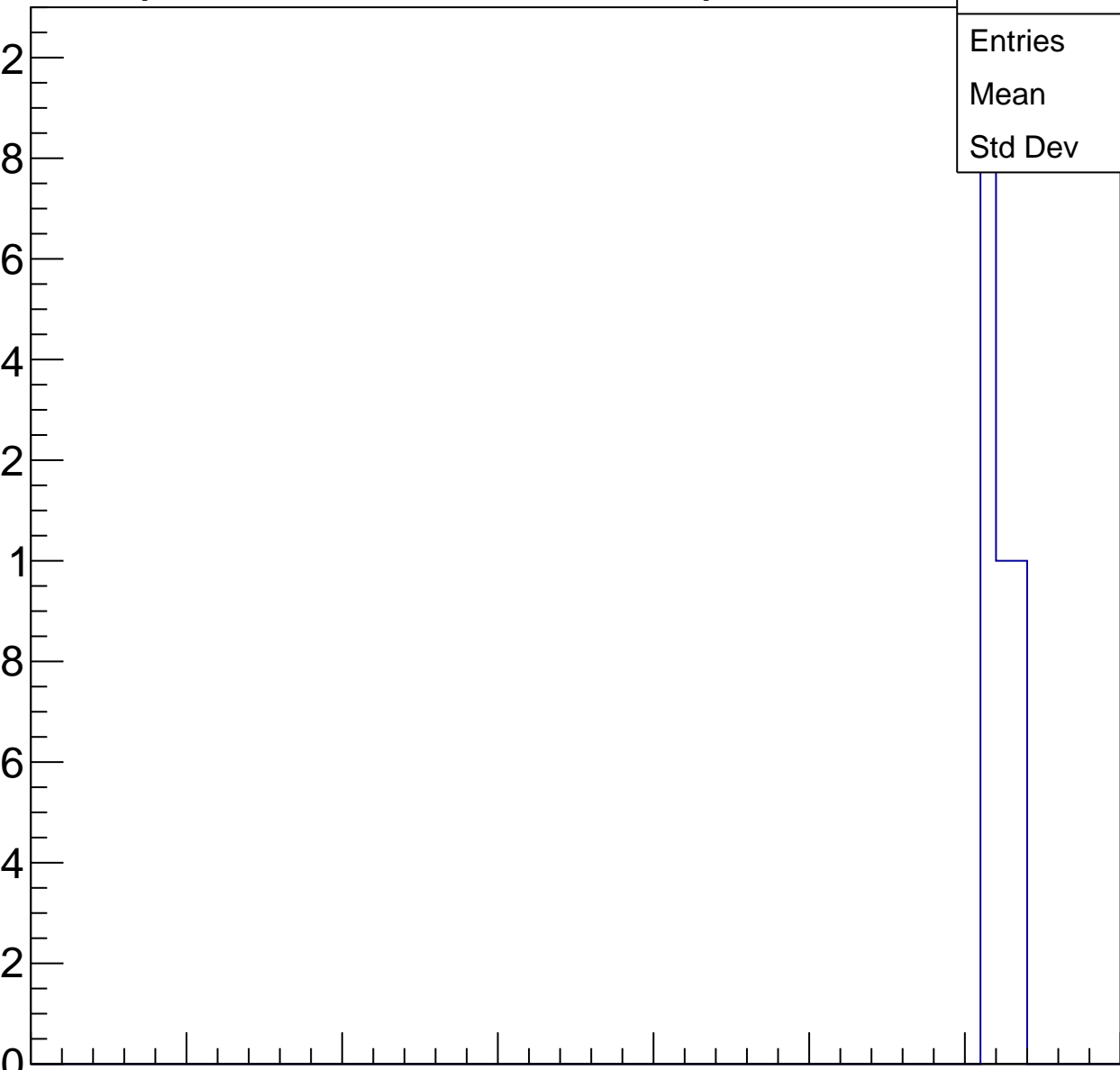
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	61.75
Std Dev	0.8292

0 10 20 30 40 50 60 70

ampl

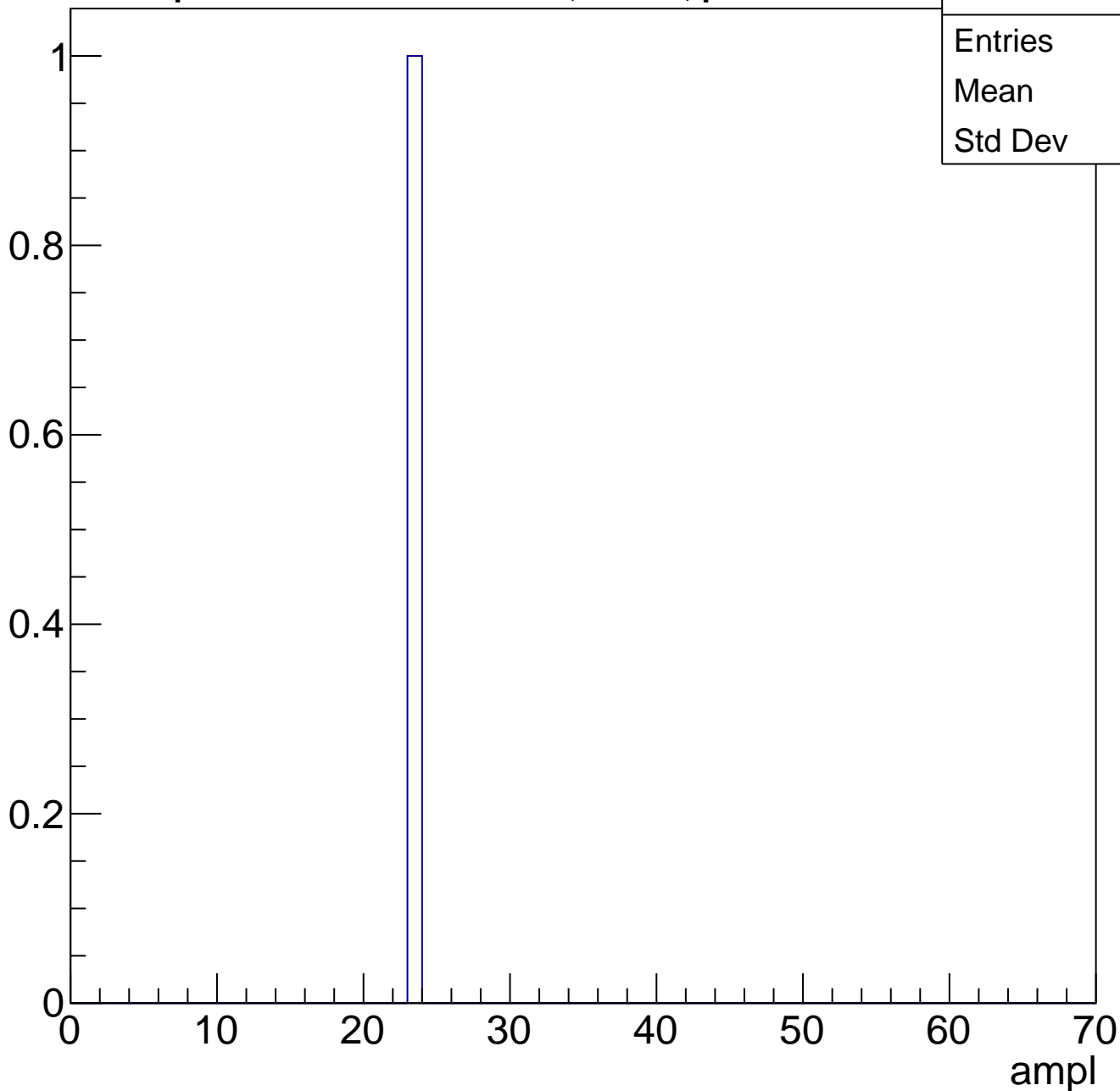




# B1L102S, U3-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	23
Std Dev	0

# B1L102S, U3-ch6, adc0

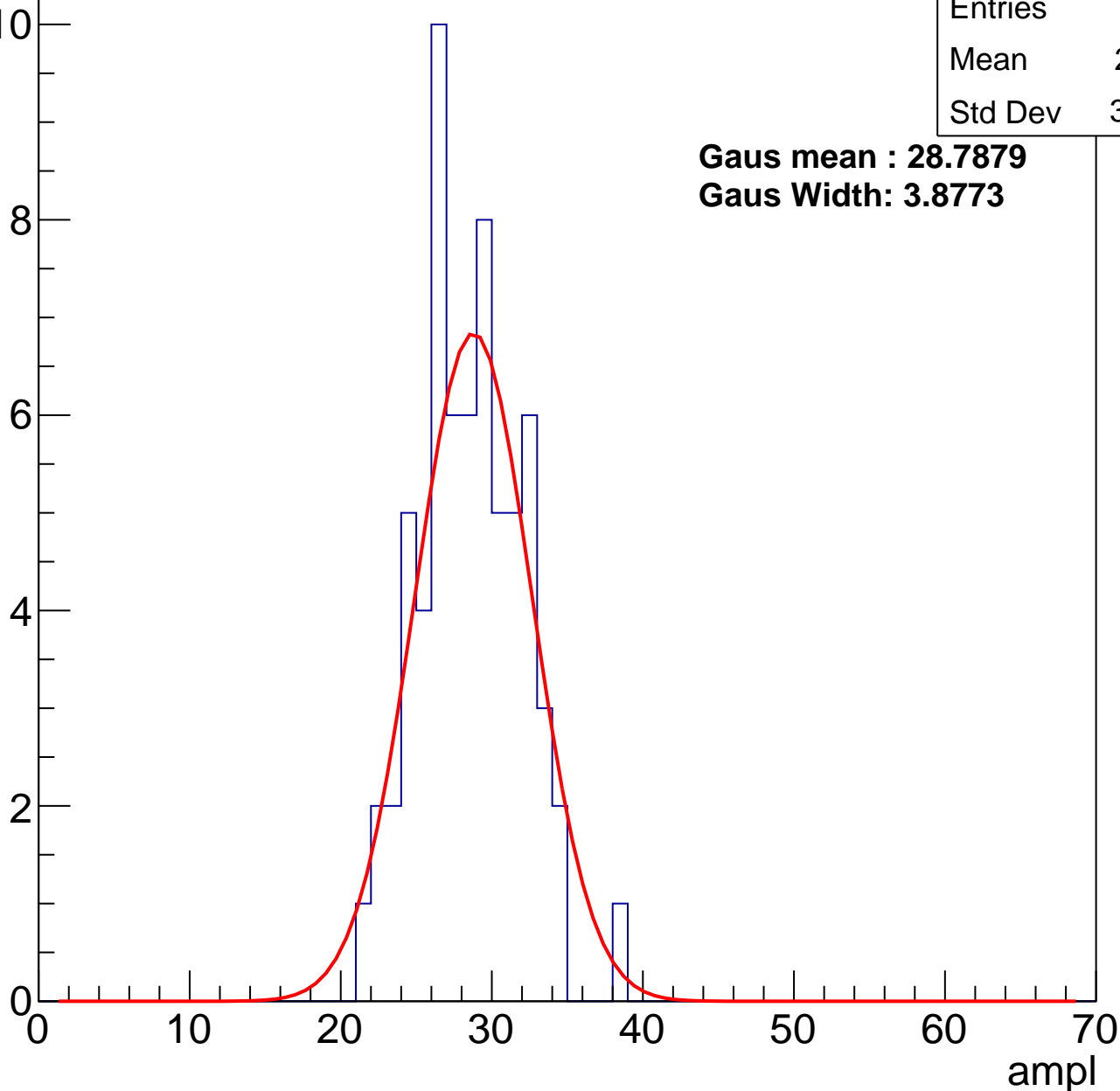
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	28.11
Std Dev	3.367

**Gaus mean : 28.7879**

**Gaus Width: 3.8773**



# B1L102S, U3-ch6, adc1

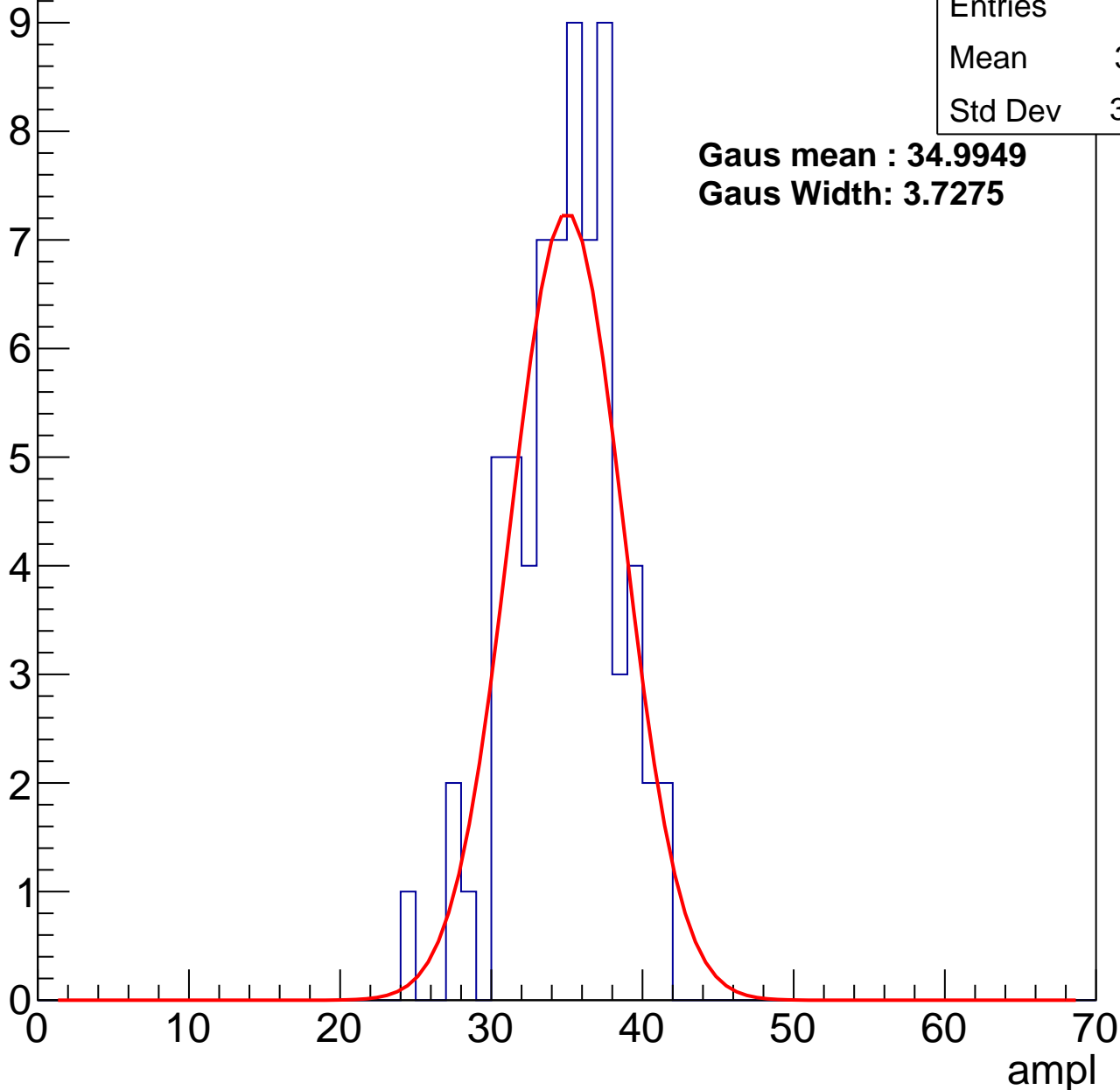
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	34.41
Std Dev	3.444

**Gaus mean : 34.9949**

**Gaus Width: 3.7275**



# B1L102S, U3-ch6, adc2

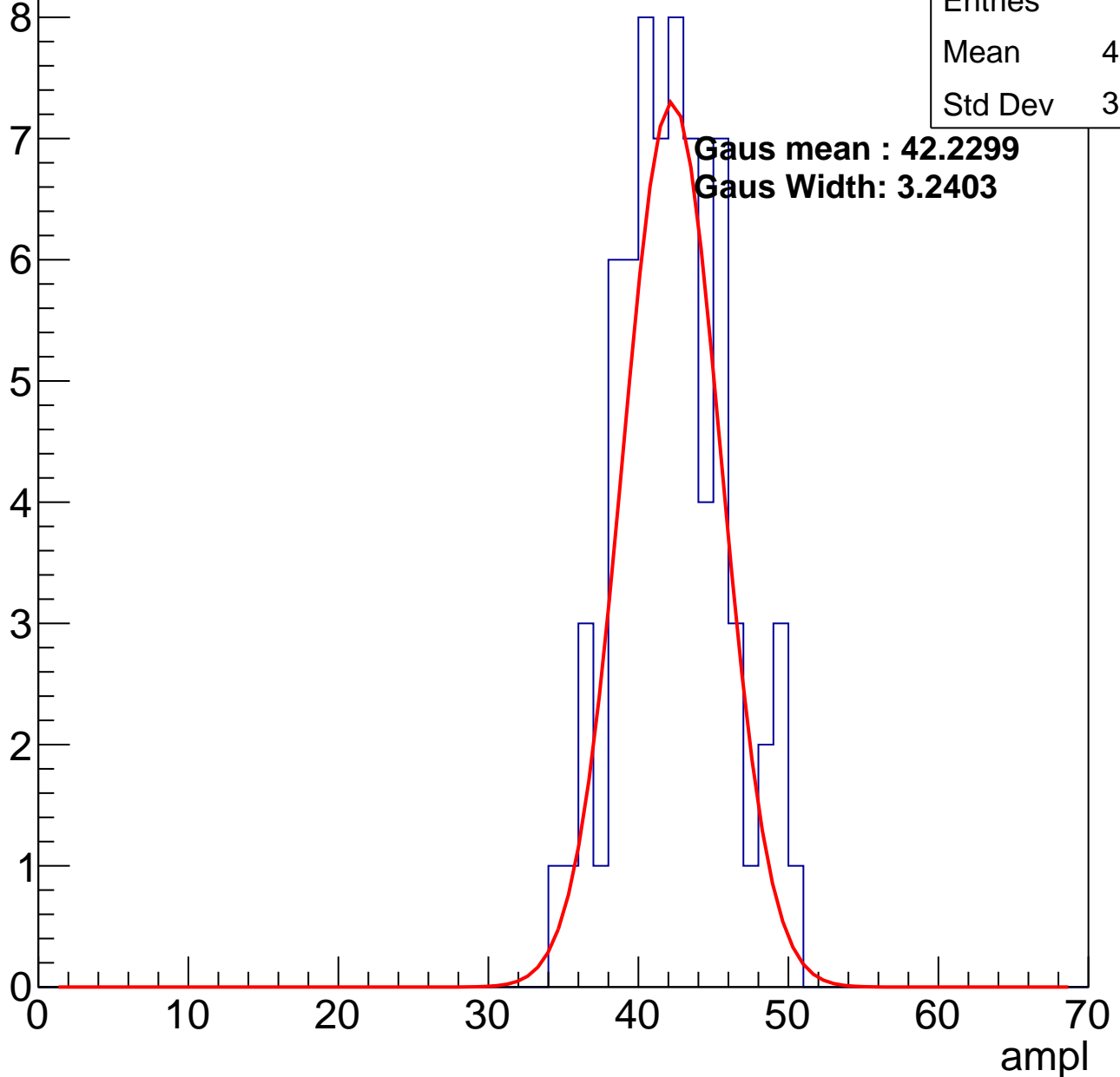
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	41.87
Std Dev	3.563

**Gaus mean : 42.2299**

**Gaus Width: 3.2403**

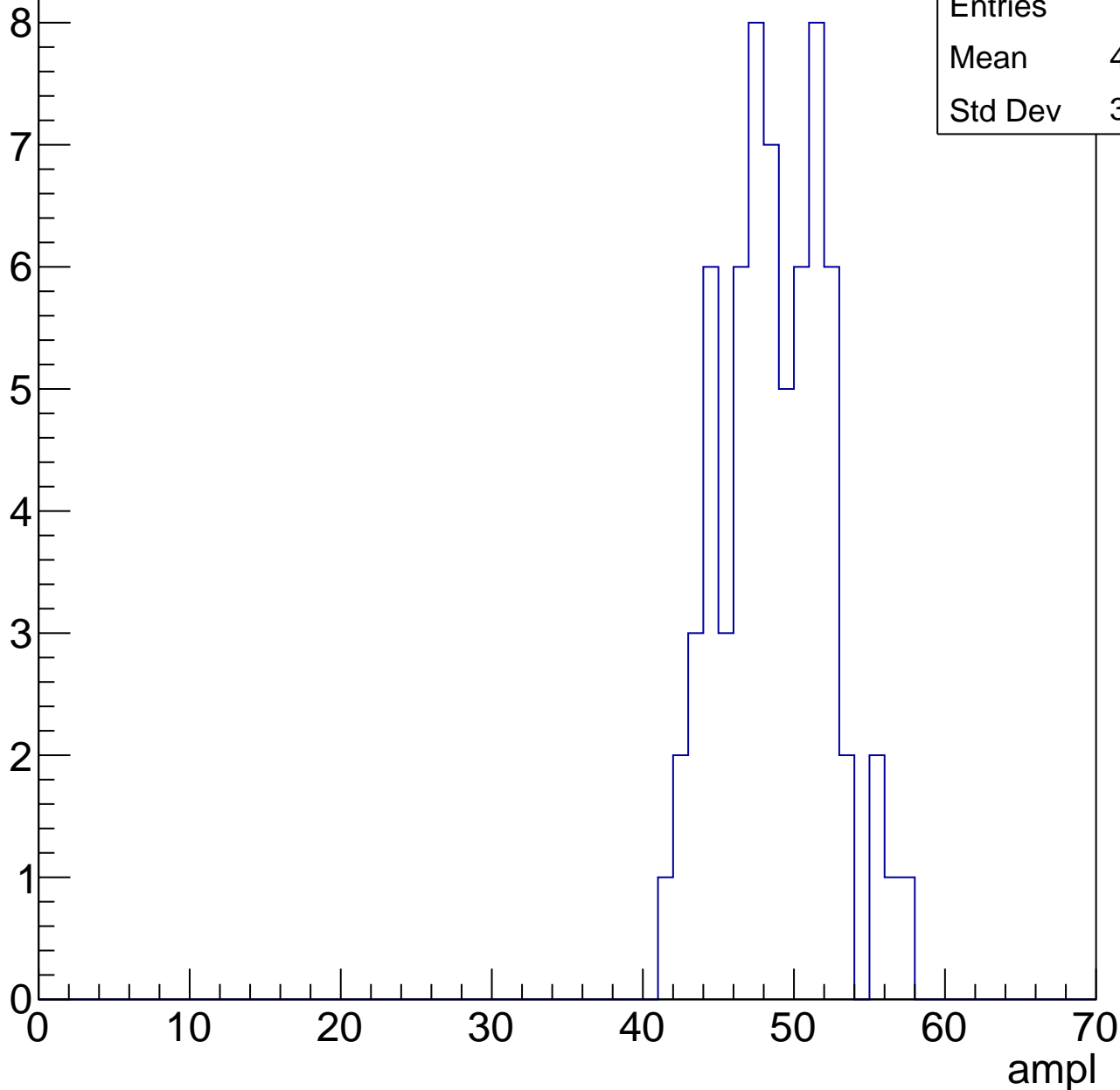


# B1L102S, U3-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	48.28
Std Dev	3.532

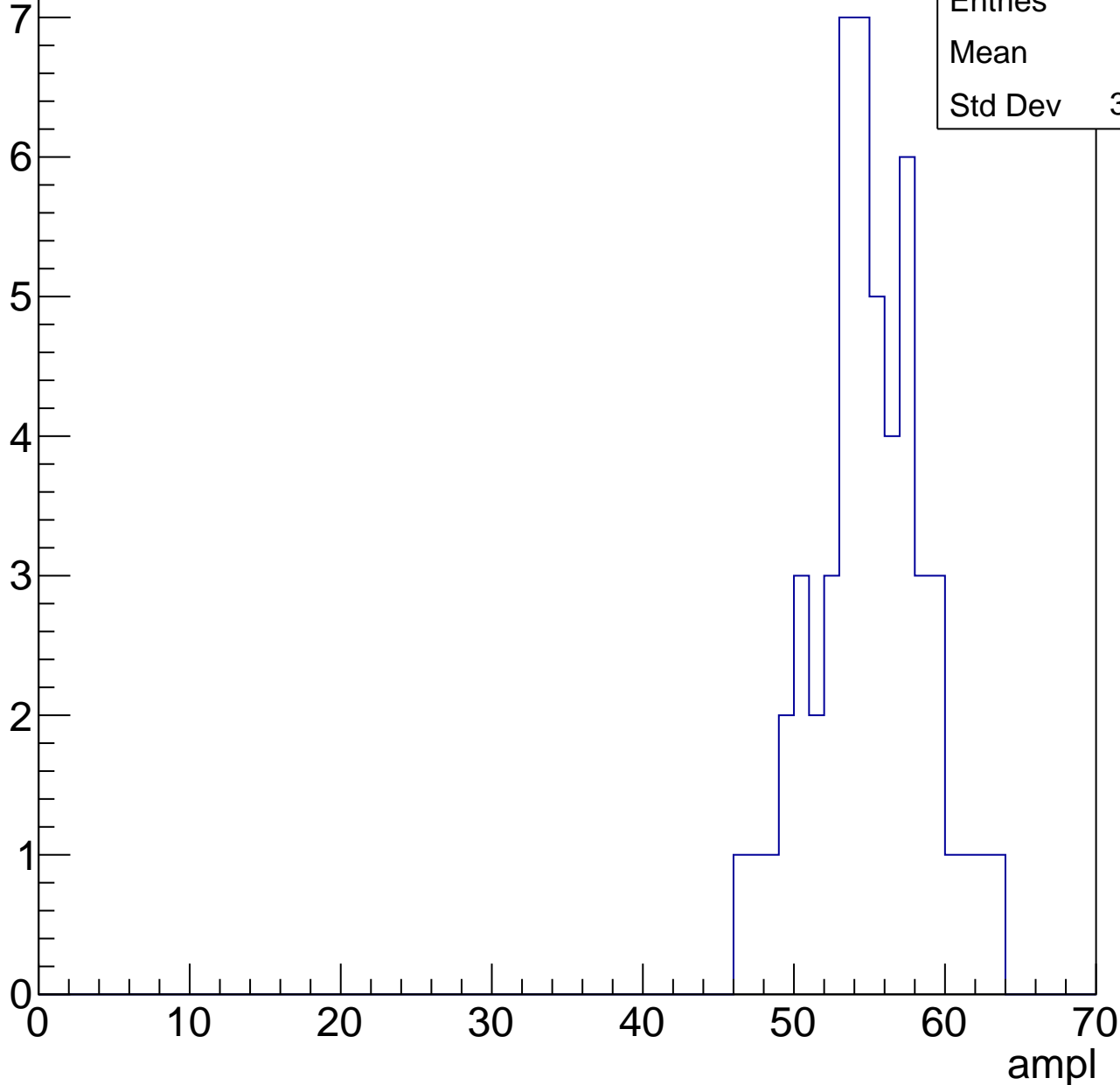


# B1L102S, U3-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

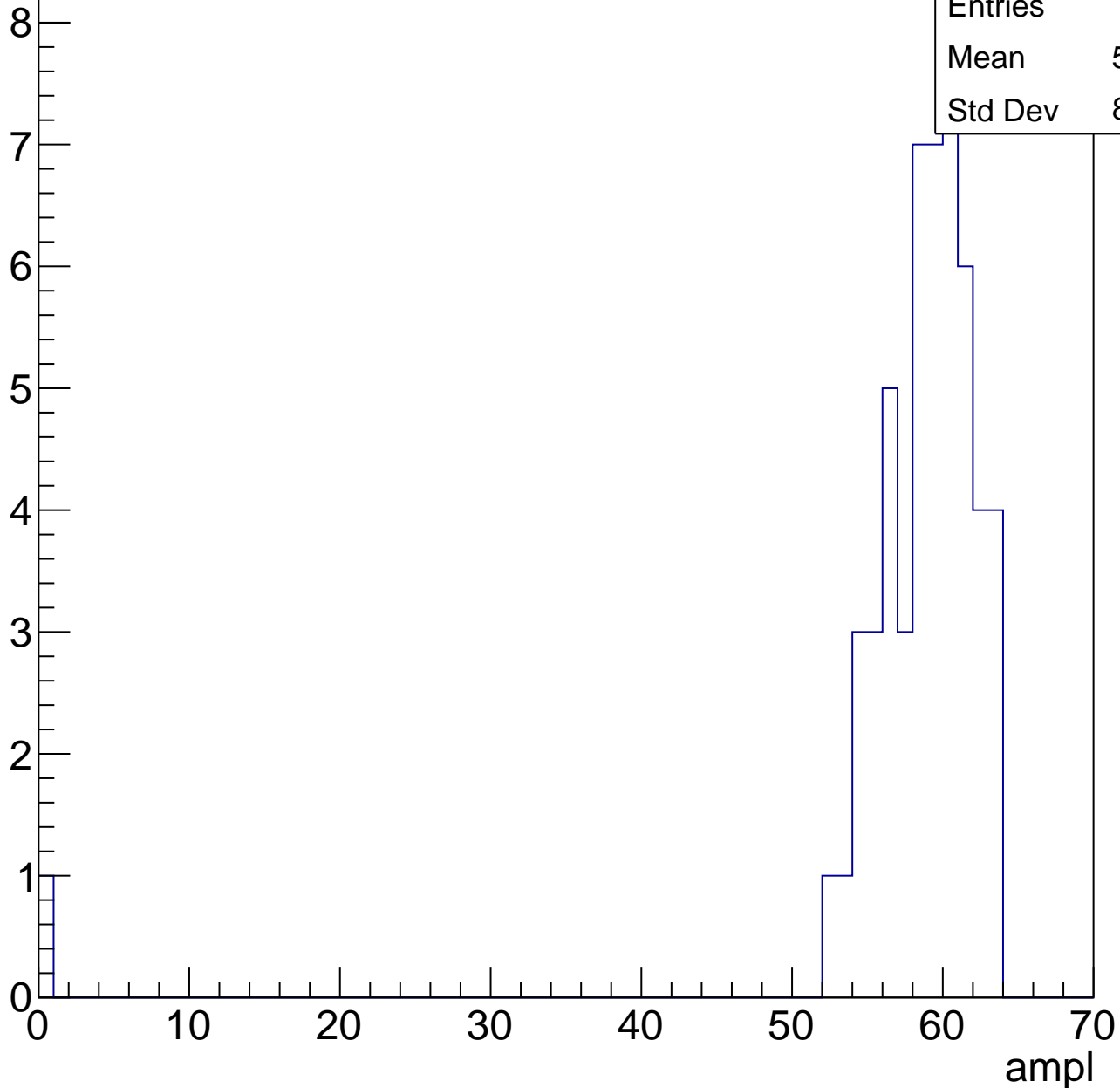
Entries	52
Mean	54.5
Std Dev	3.666



# B1L102S, U3-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

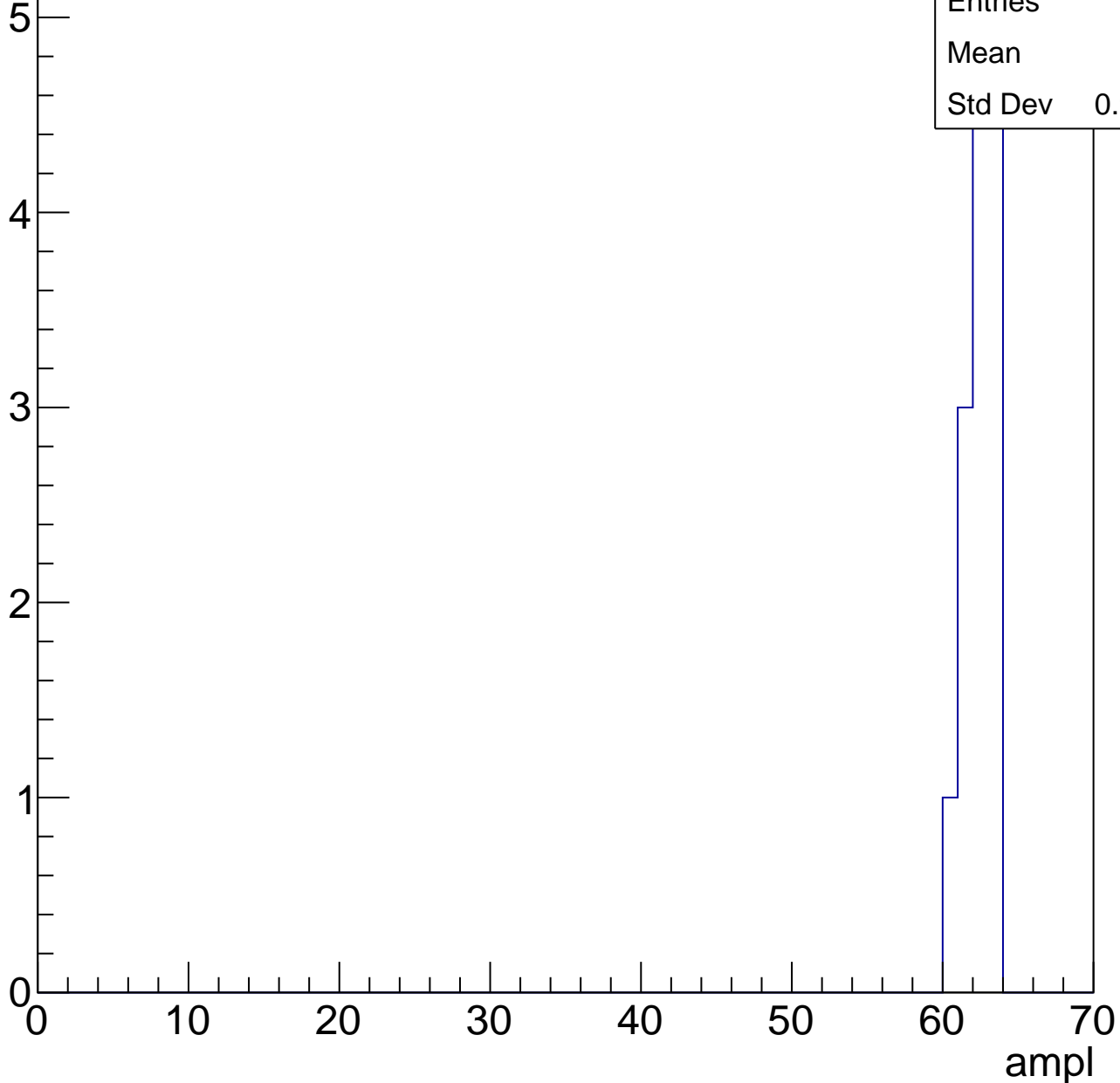


# B1L102S, U3-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	14
Mean	62
Std Dev	0.9258





# B1L102S, U3-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	20
Std Dev	0

ampl

# B1L102S, U3-ch7, adc0

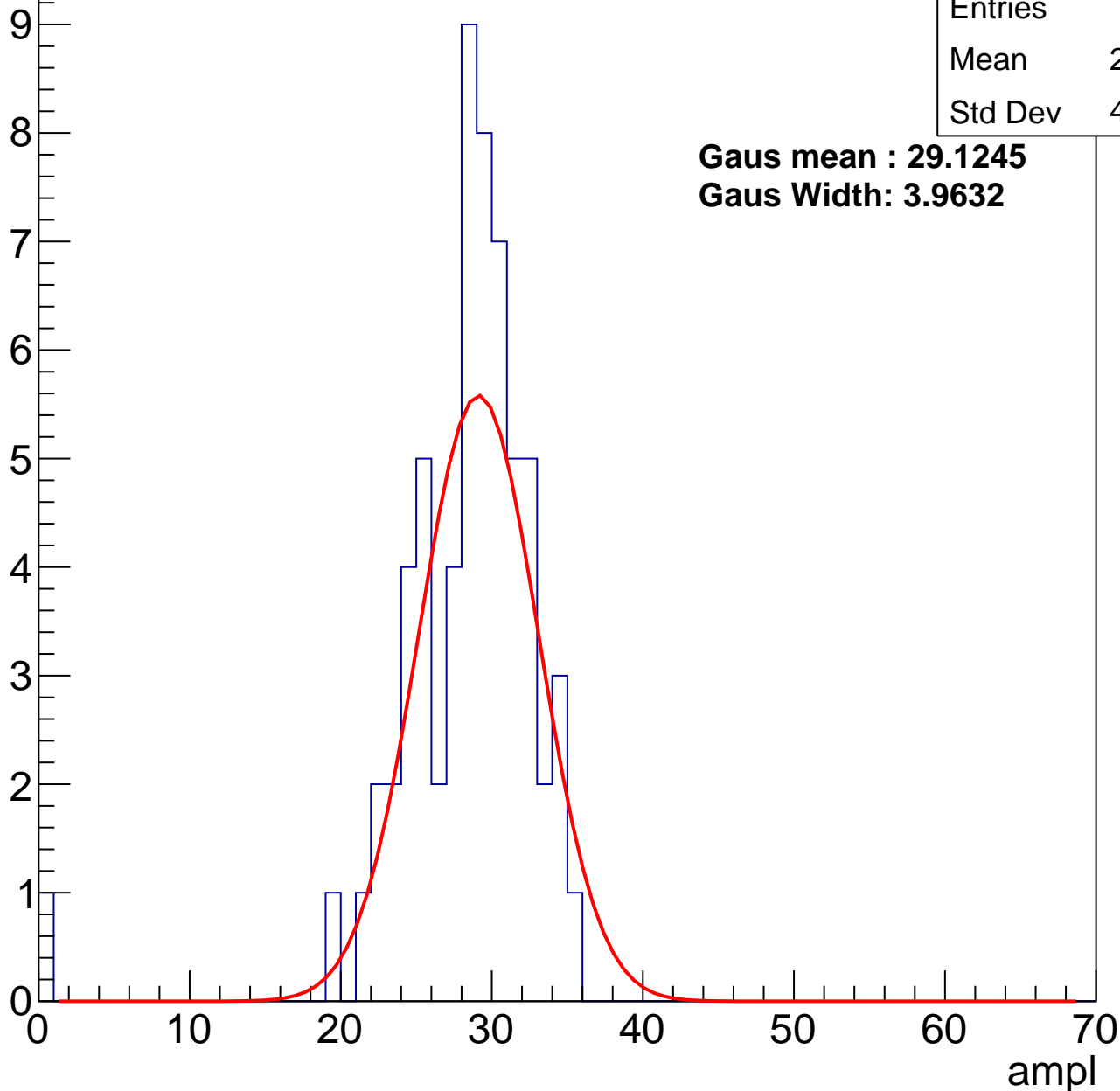
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	27.79
Std Dev	4.955

**Gaus mean : 29.1245**

**Gaus Width: 3.9632**



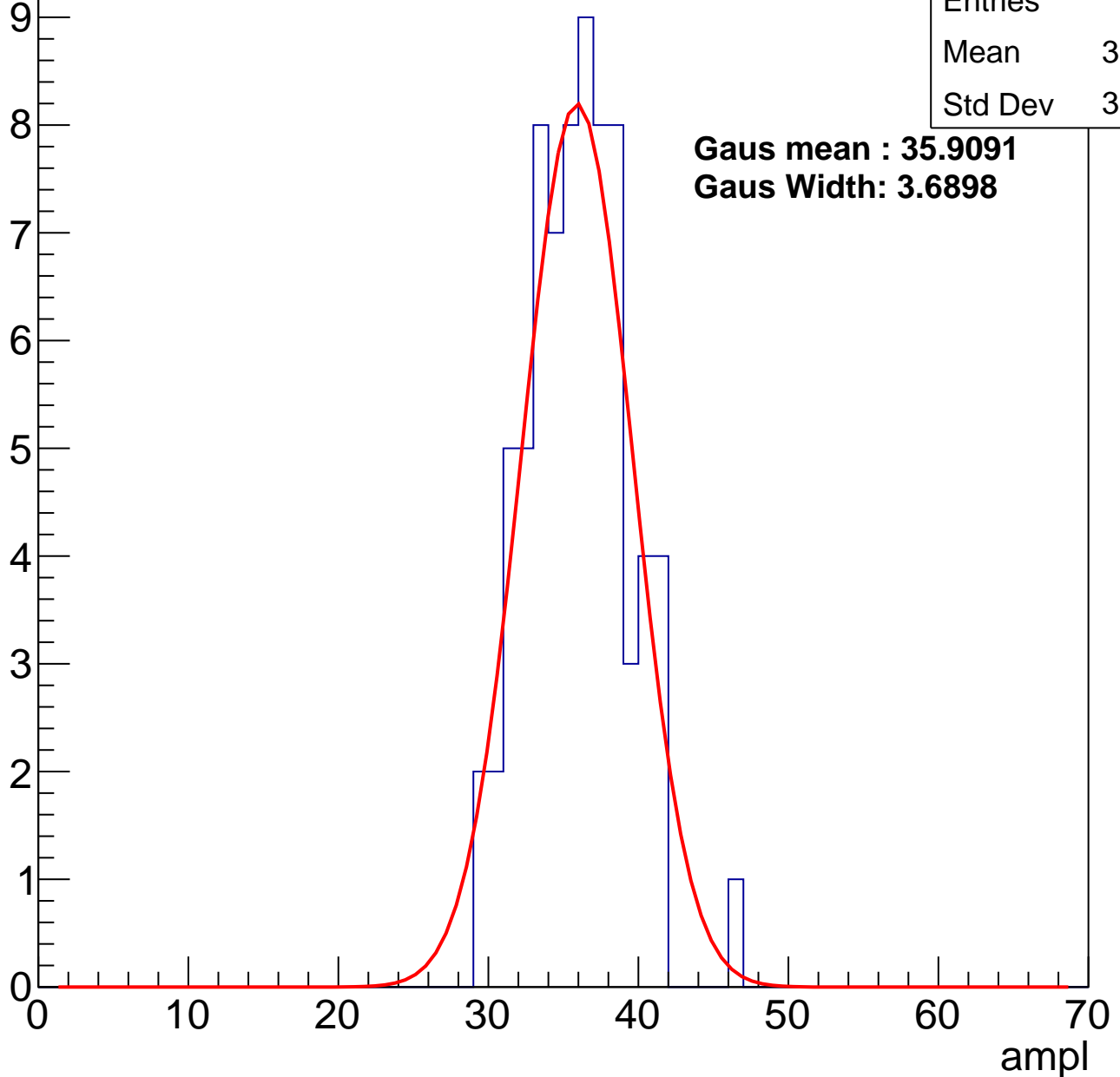
# B1L102S, U3-ch7, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	35.49
Std Dev	3.277

**Gaus mean : 35.9091**  
**Gaus Width: 3.6898**



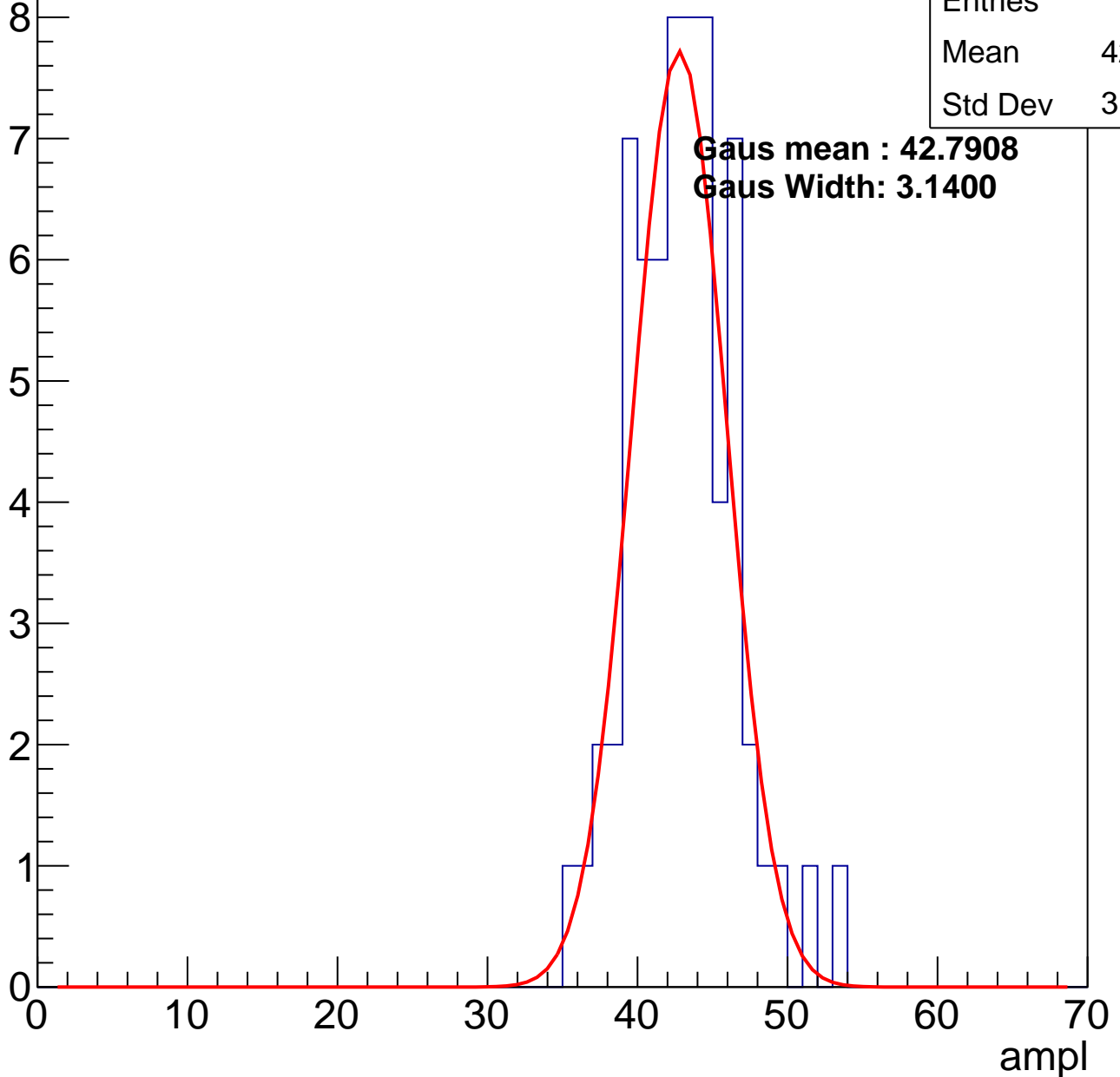
# B1L102S, U3-ch7, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	42.56
Std Dev	3.403

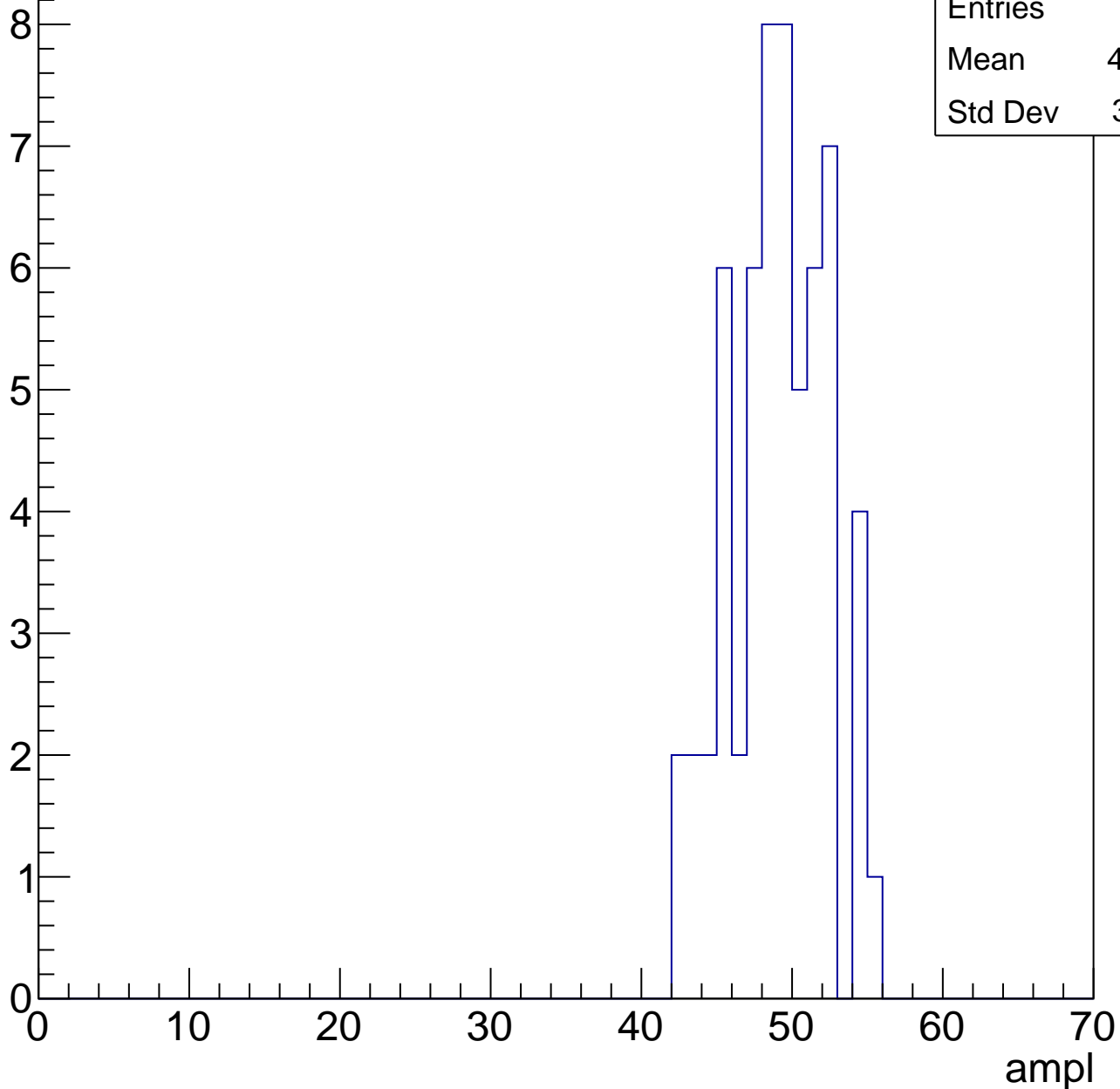
**Gaus mean : 42.7908**  
**Gaus Width: 3.1400**



# B1L102S, U3-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

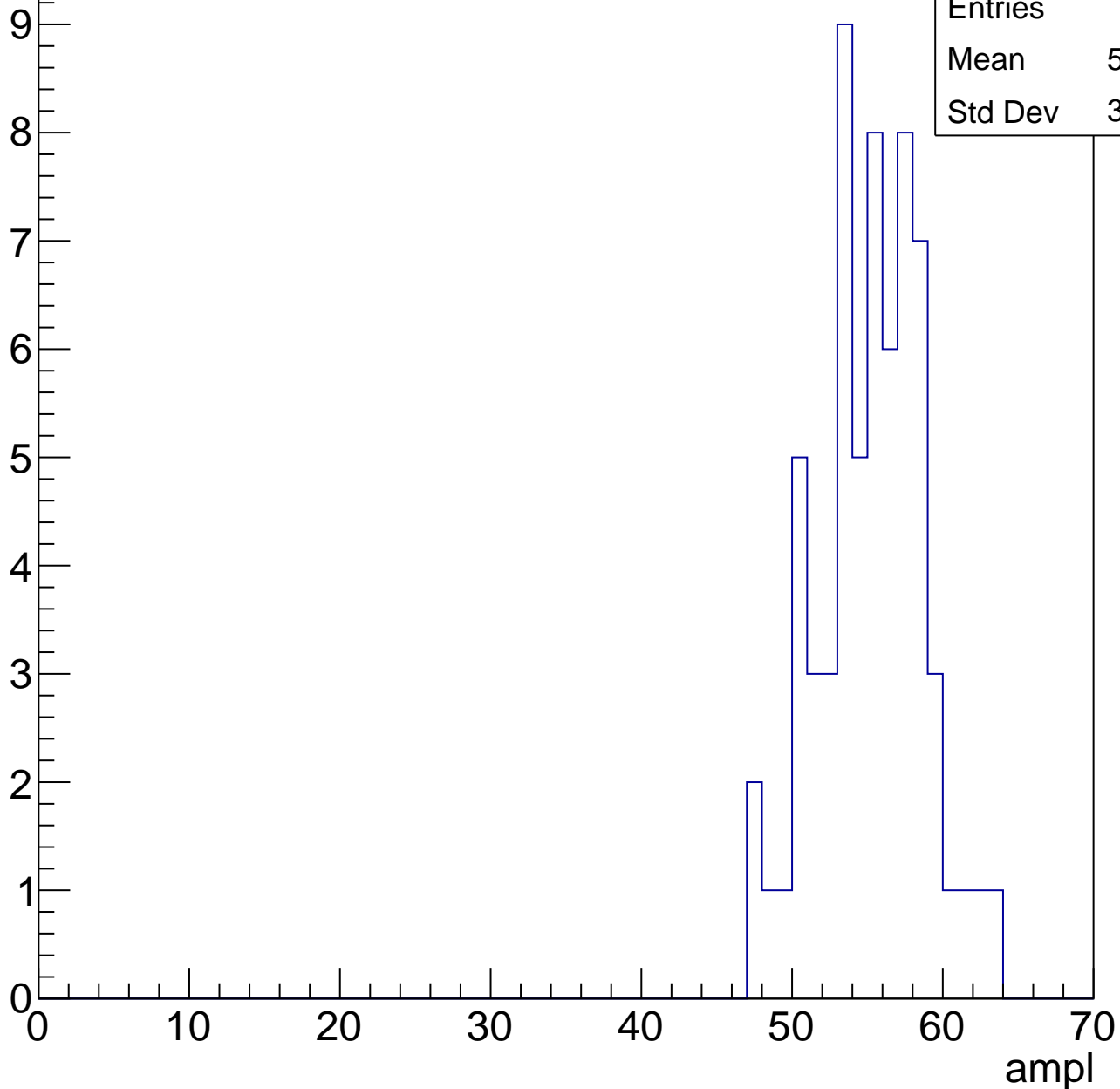


Entries	59
Mean	48.63
Std Dev	3.151

# B1L102S, U3-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch7, adc5

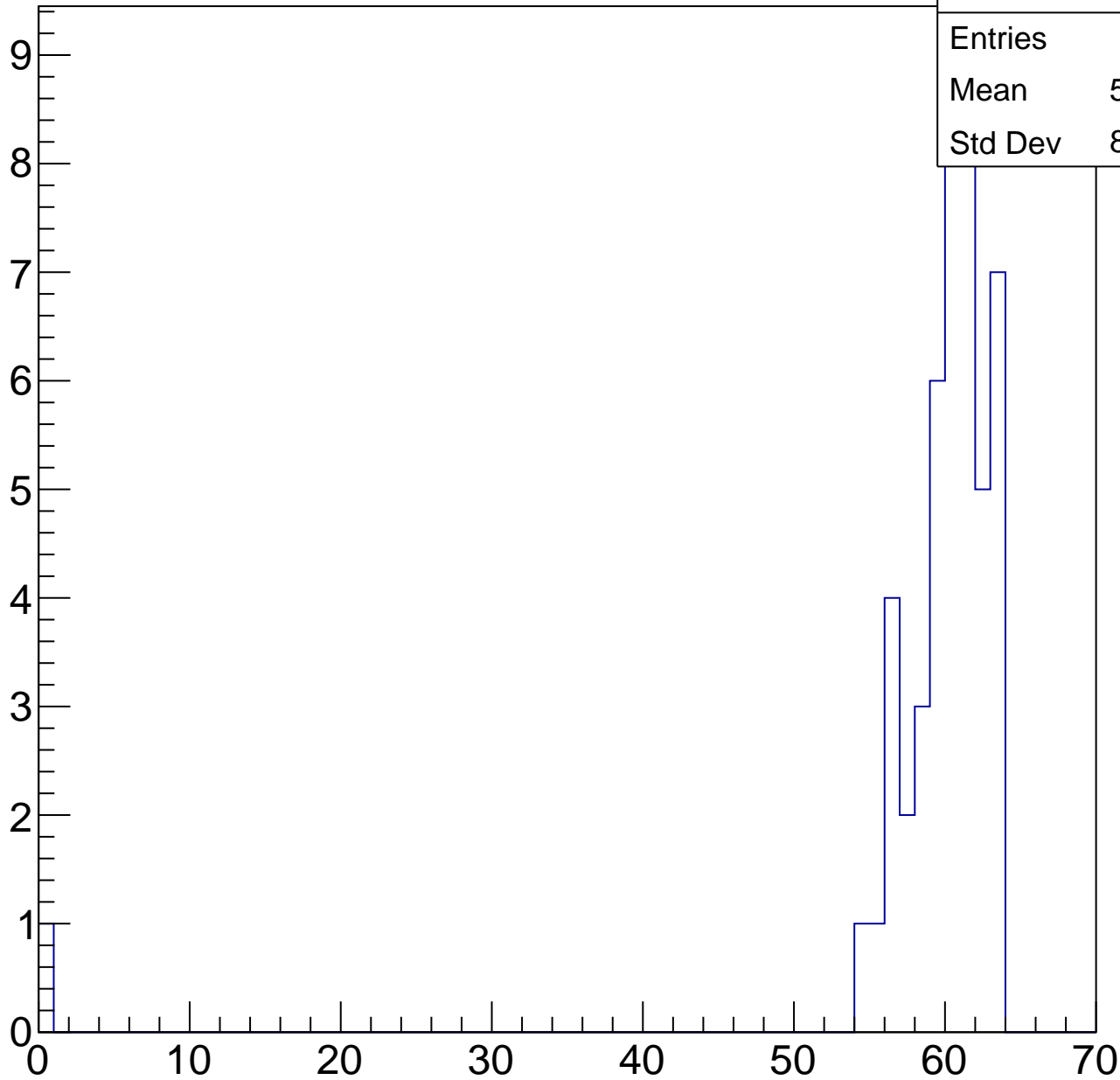
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	58.65
Std Dev	8.856

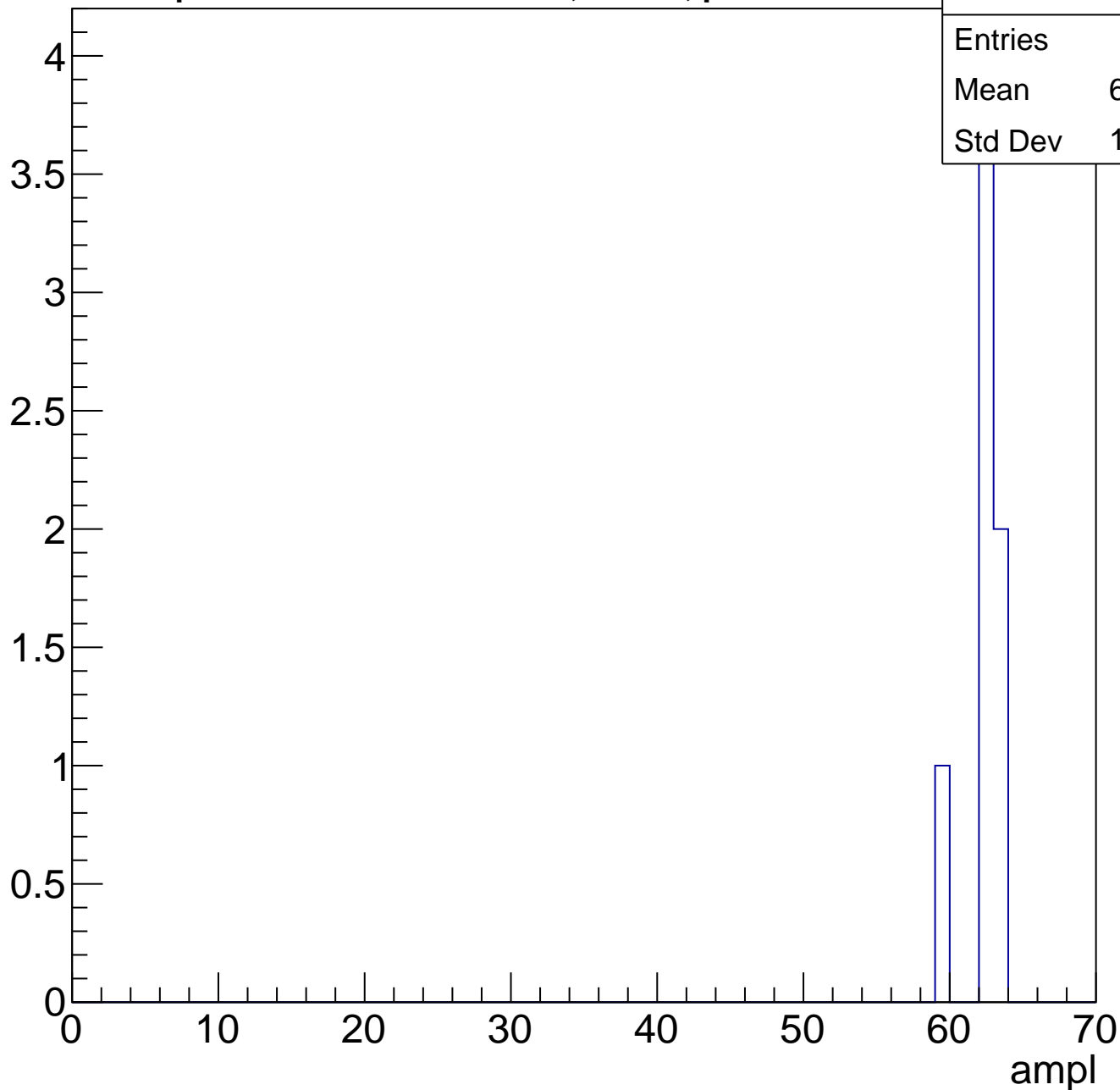
ampl



# B1L102S, U3-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U3-ch8, adc0

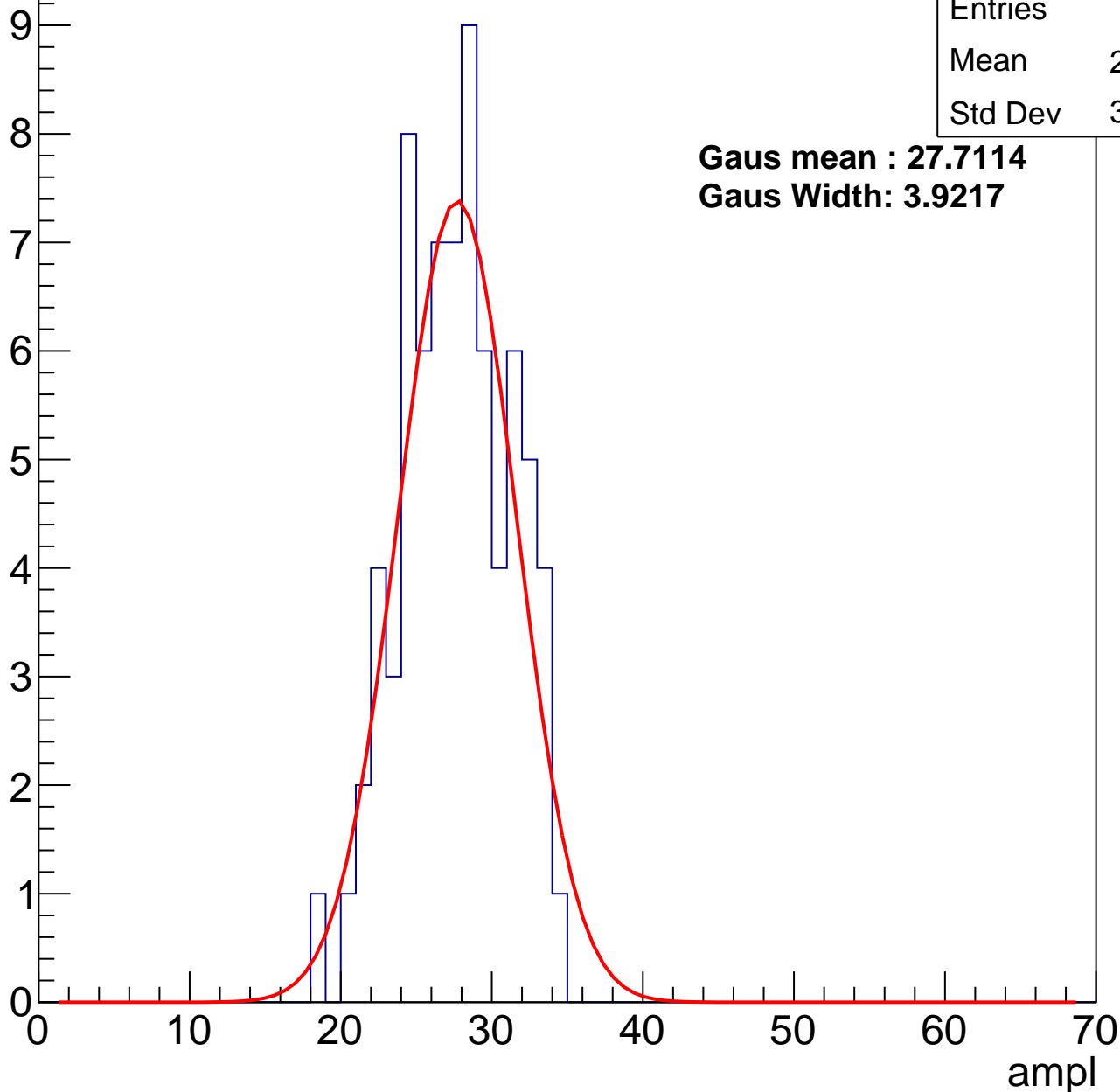
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	27.14
Std Dev	3.554

**Gaus mean : 27.7114**

**Gaus Width: 3.9217**



# B1L102S, U3-ch8, adc1

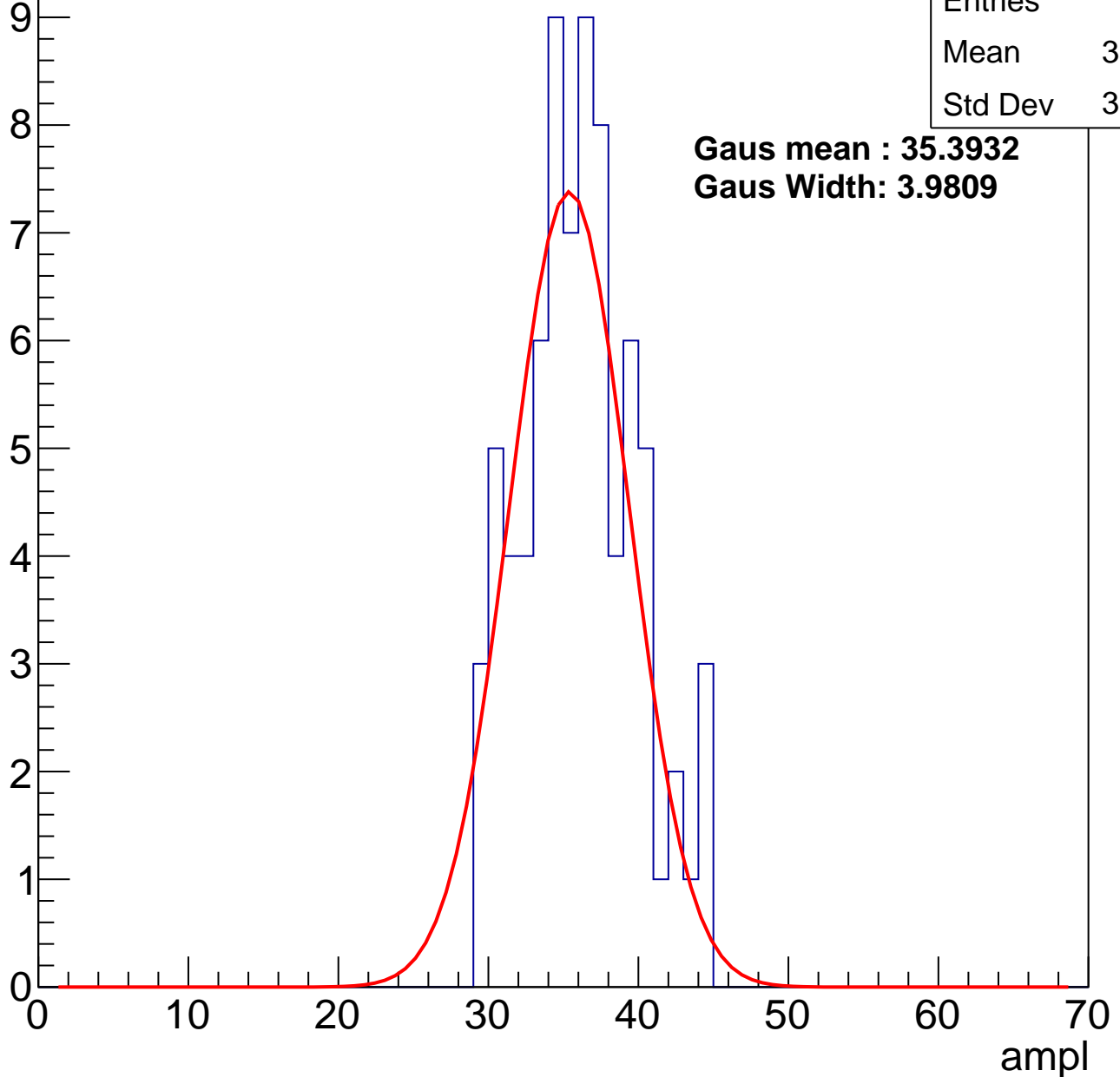
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	35.64
Std Dev	3.734

**Gaus mean : 35.3932**

**Gaus Width: 3.9809**



# B1L102S, U3-ch8, adc2

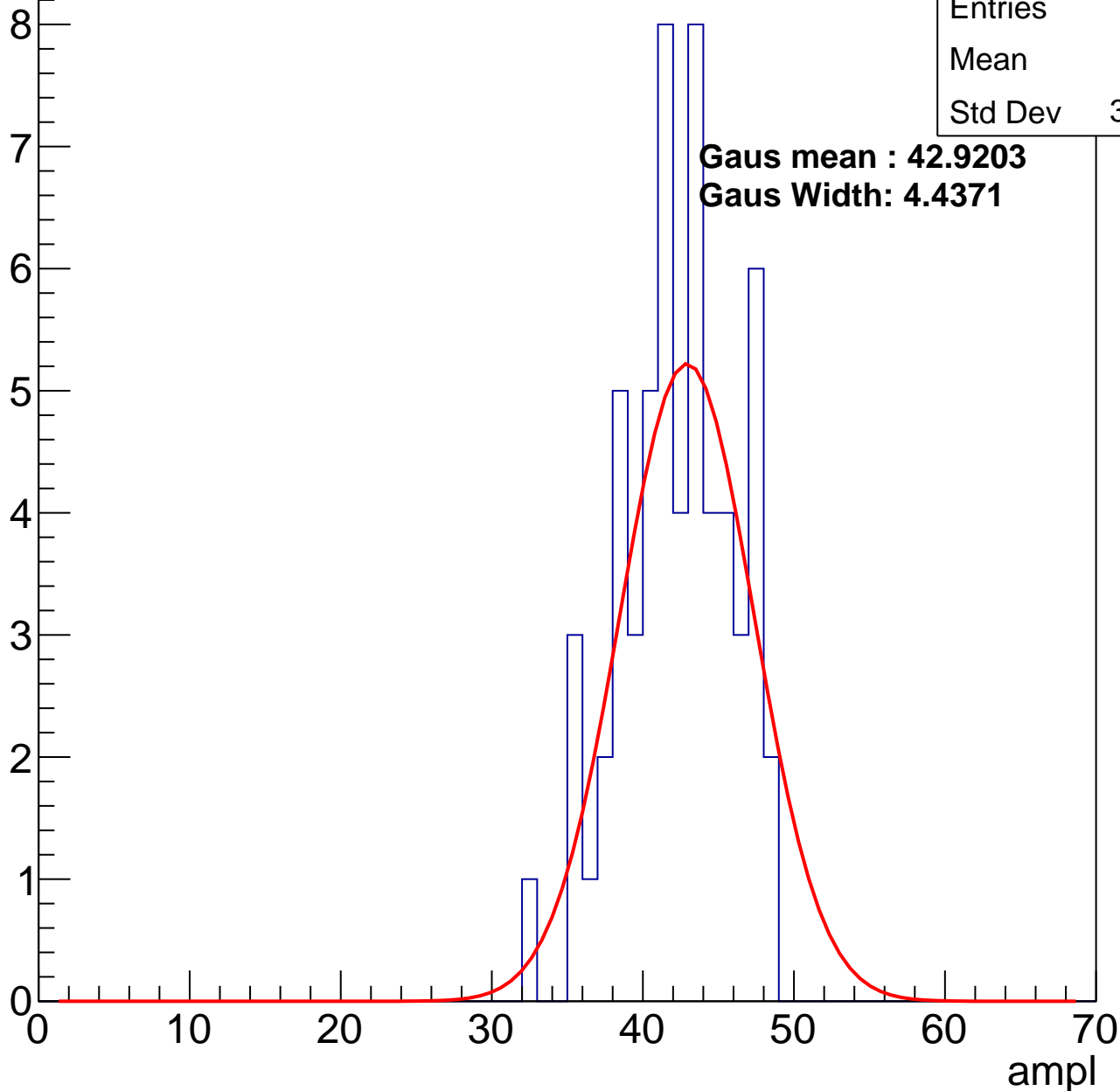
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	41.8
Std Dev	3.672

**Gaus mean : 42.9203**

**Gaus Width: 4.4371**

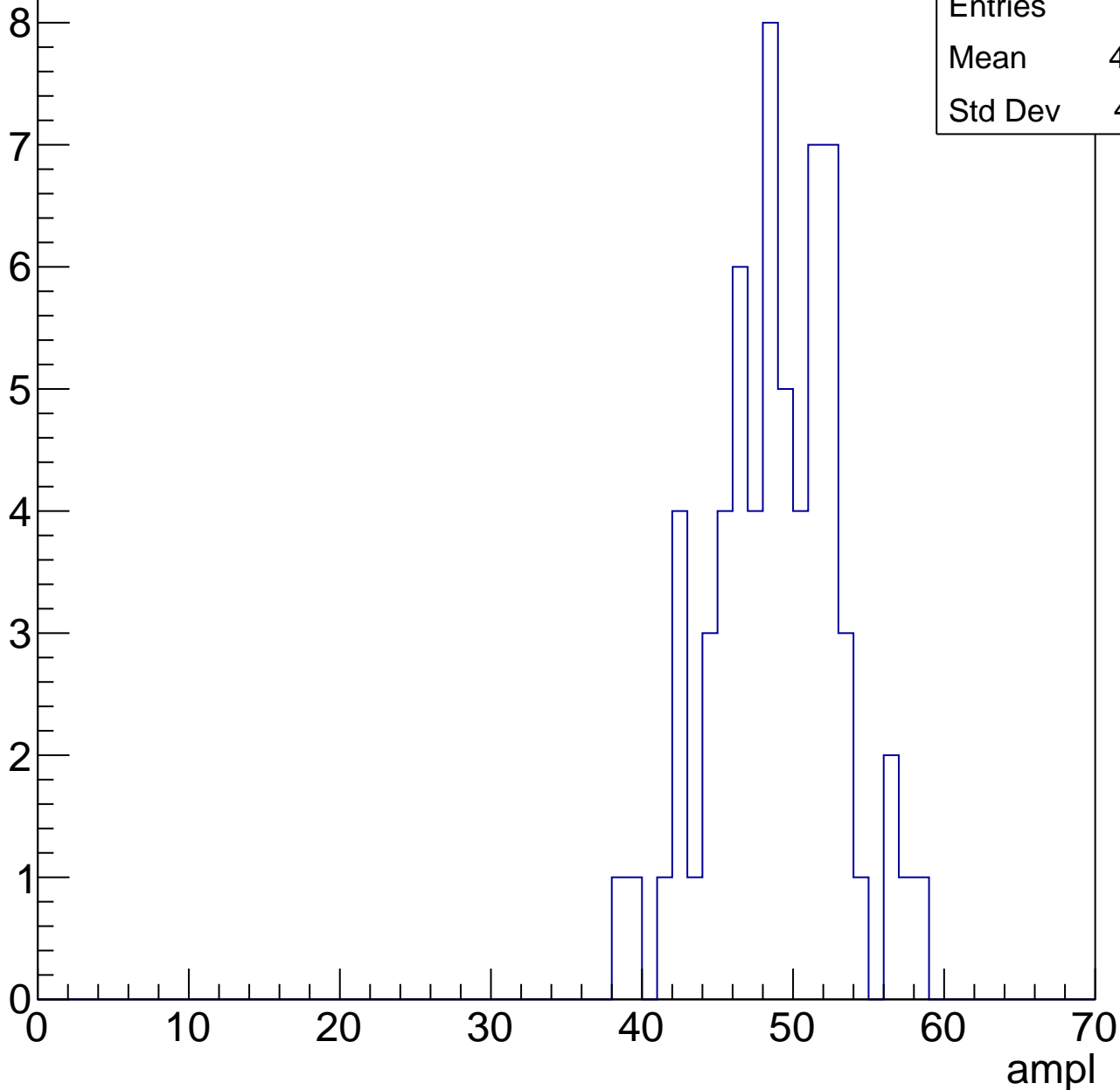


# B1L102S, U3-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	48.36
Std Dev	4.181

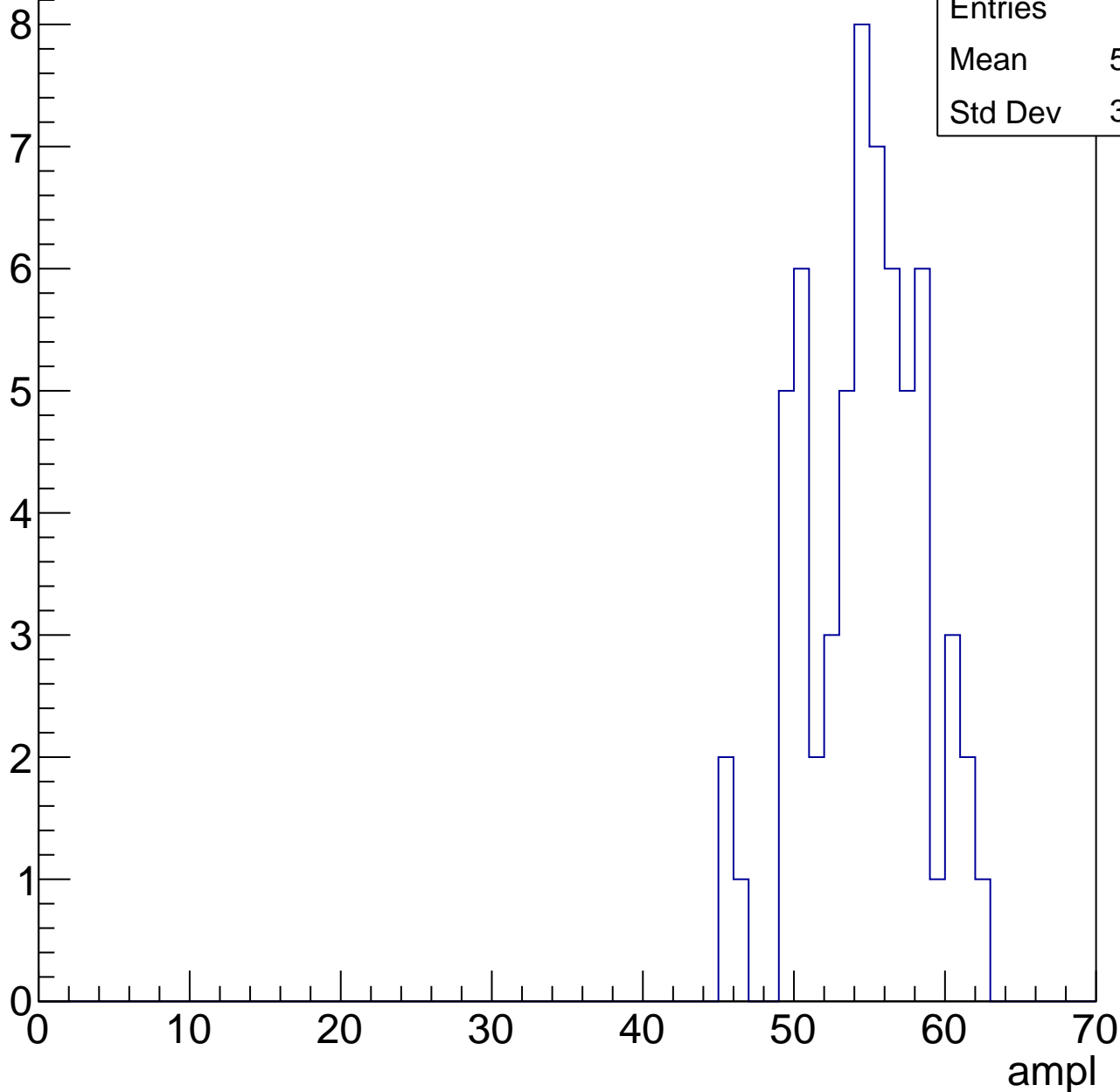


# B1L102S, U3-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	54.17
Std Dev	3.877

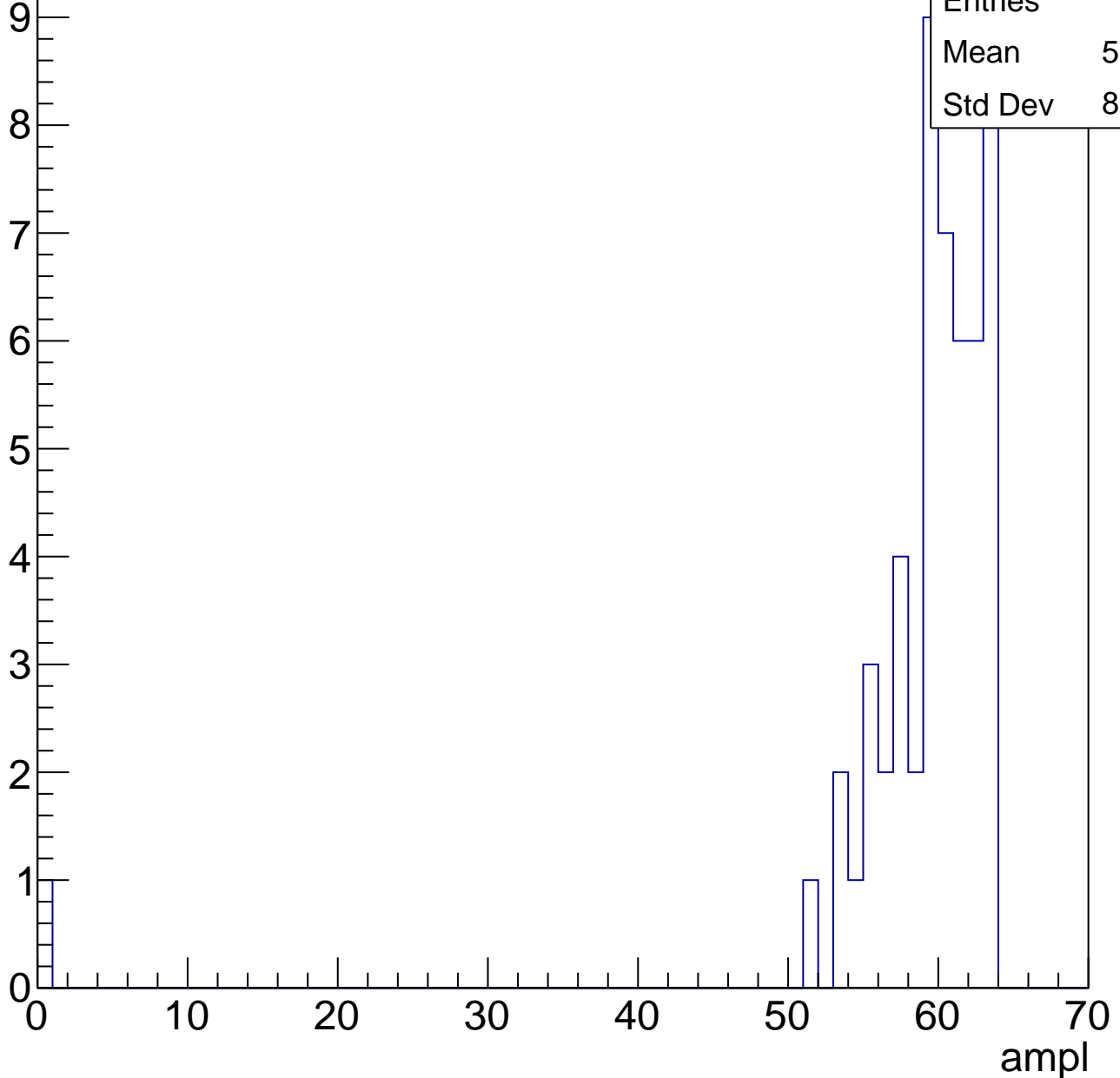


# B1L102S, U3-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

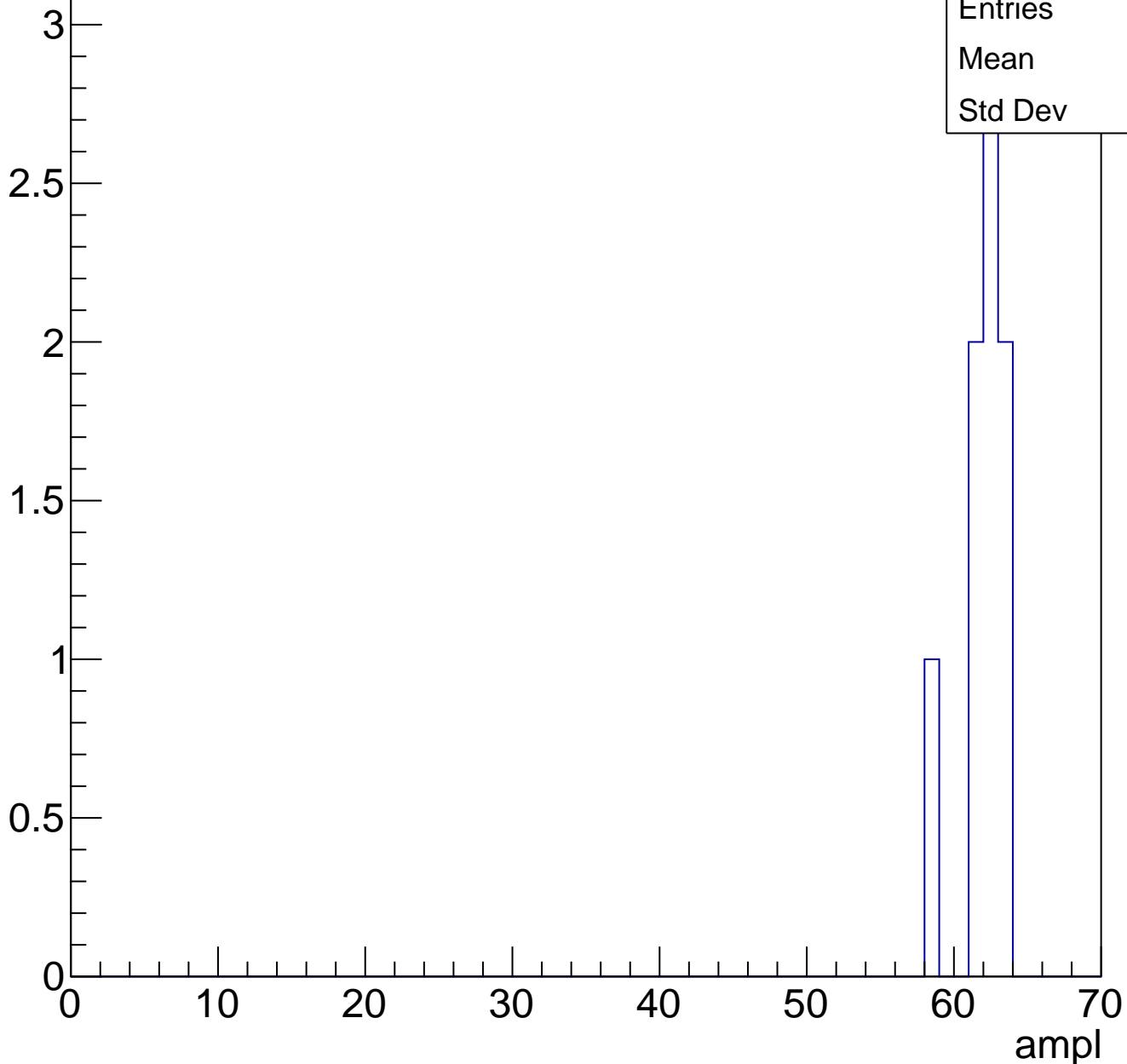
Entries	52
Mean	58.17
Std Dev	8.664



# B1L102S, U3-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

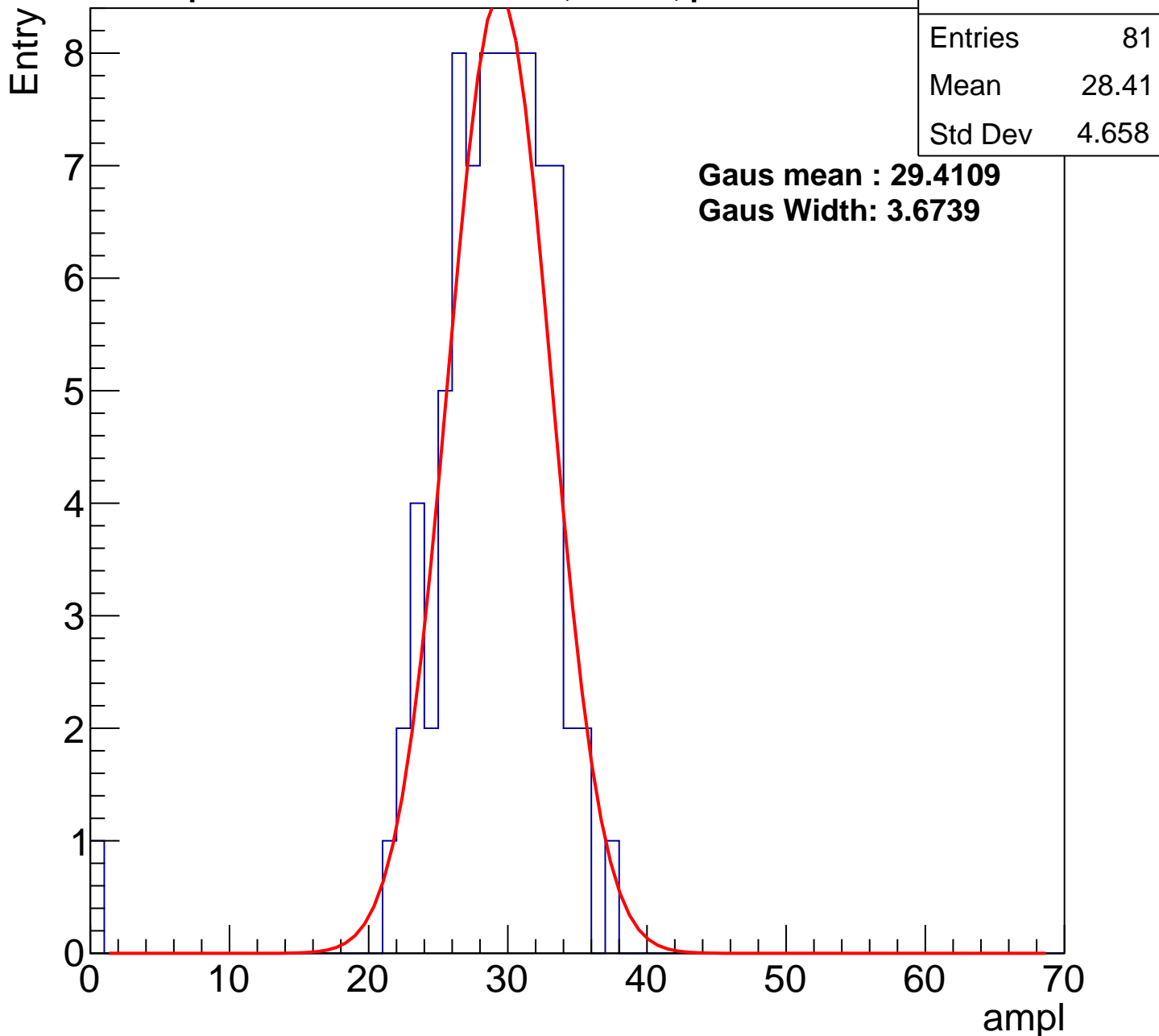
Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U3-ch9, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2



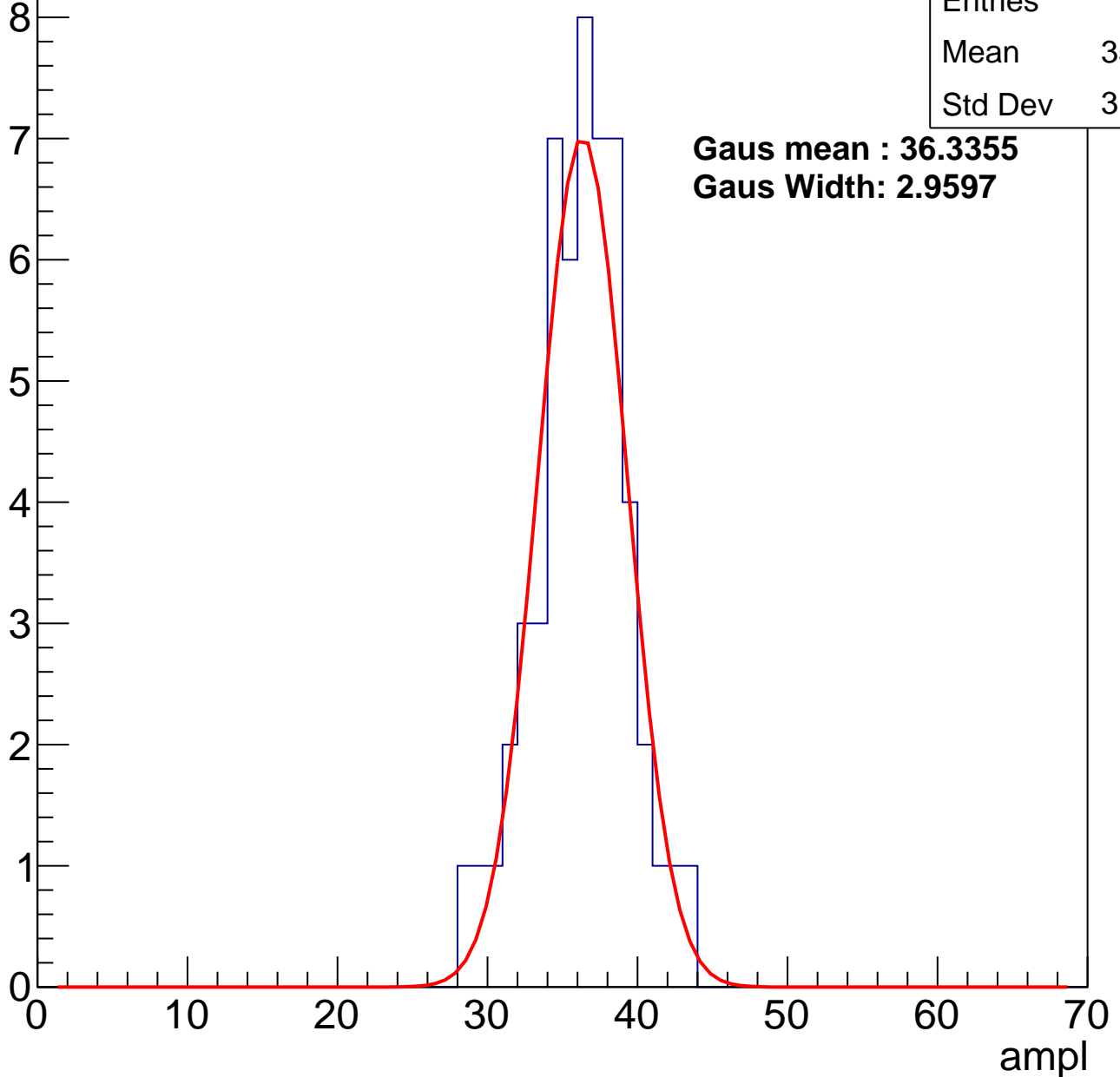
# B1L102S, U3-ch9, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	35.76
Std Dev	3.069

**Gaus mean : 36.3355**  
**Gaus Width: 2.9597**



# B1L102S, U3-ch9, adc2

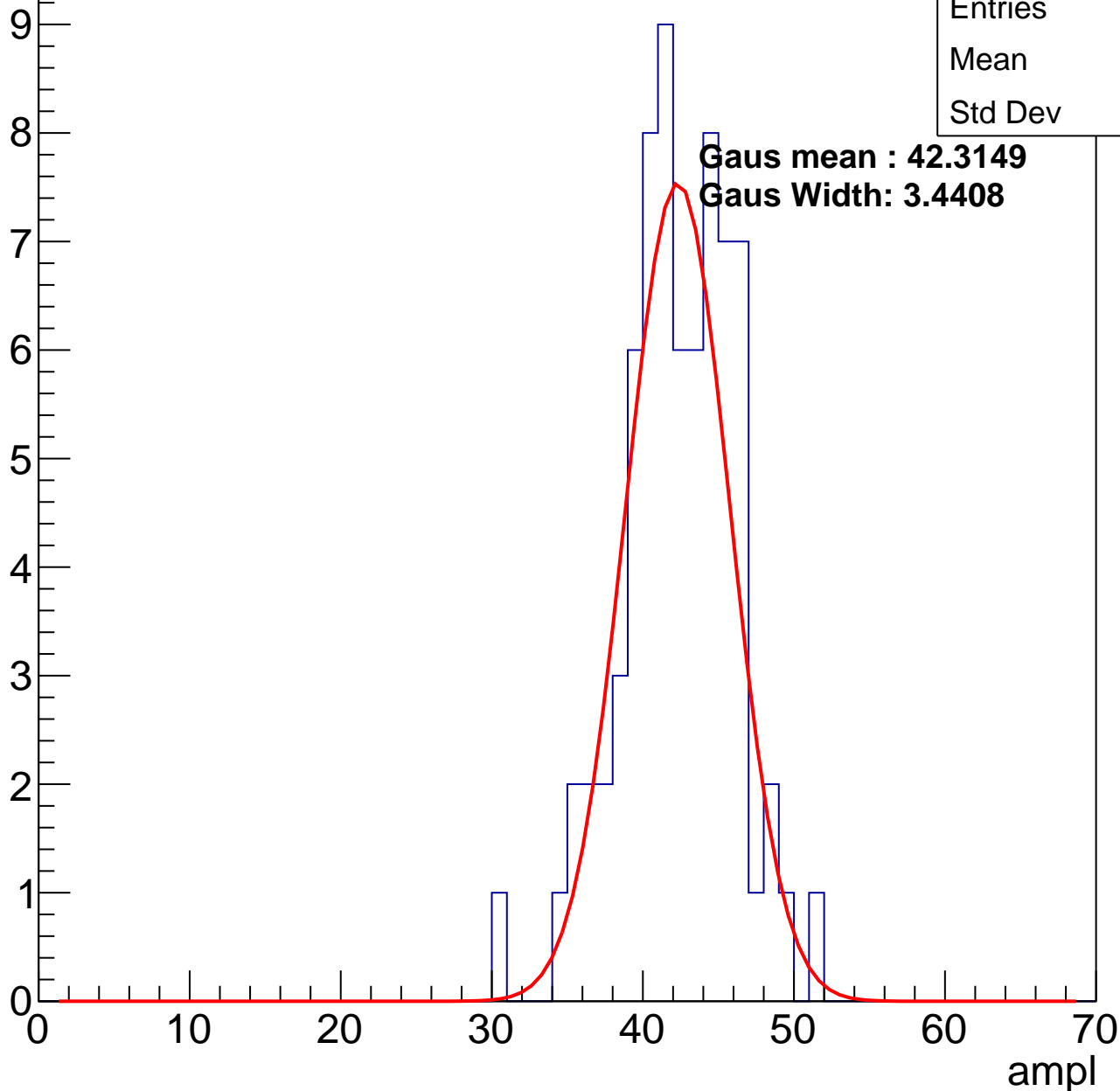
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	41.9
Std Dev	3.72

**Gaus mean : 42.3149**

**Gaus Width: 3.4408**

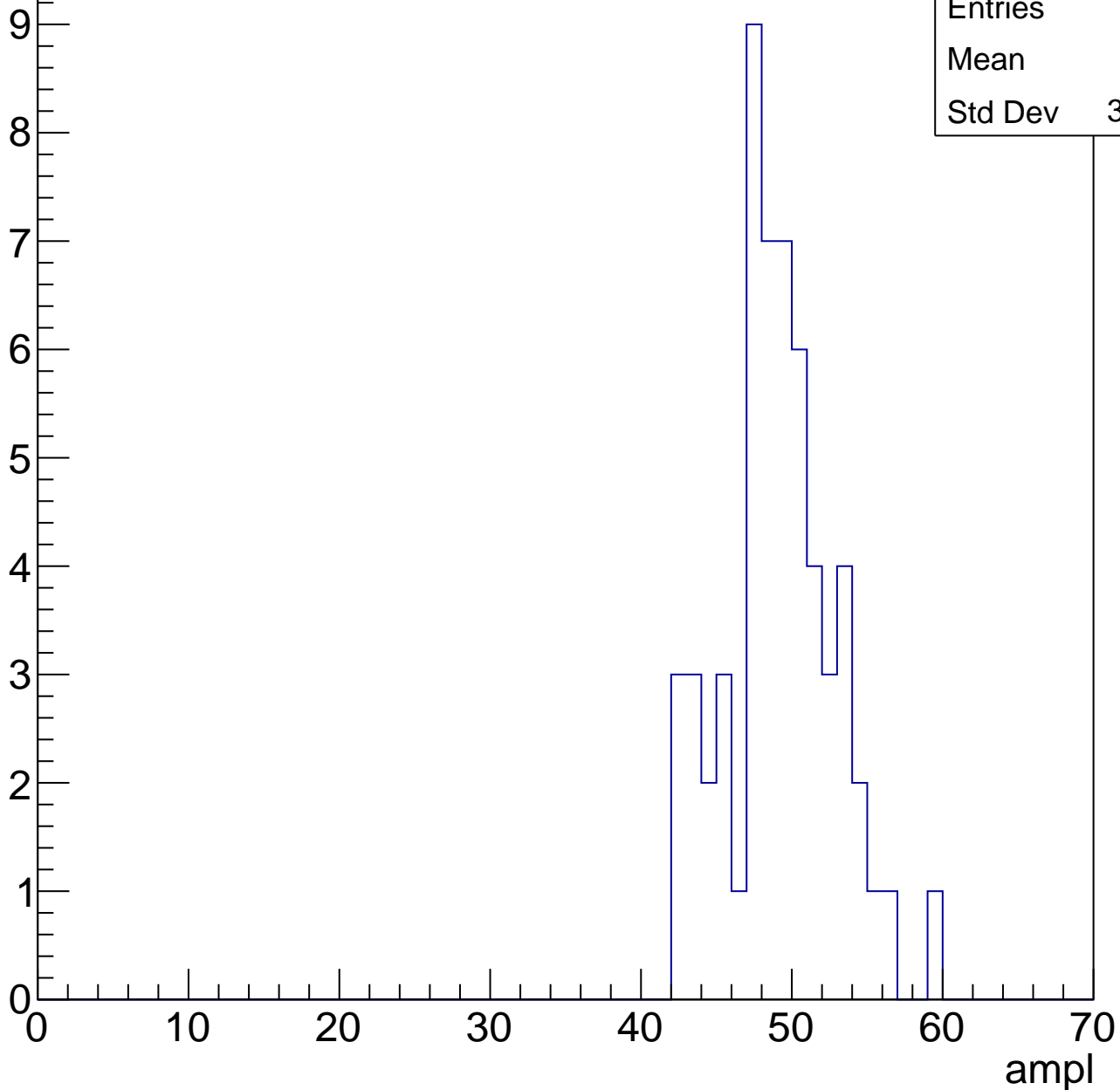


# B1L102S, U3-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	48.7
Std Dev	3.622

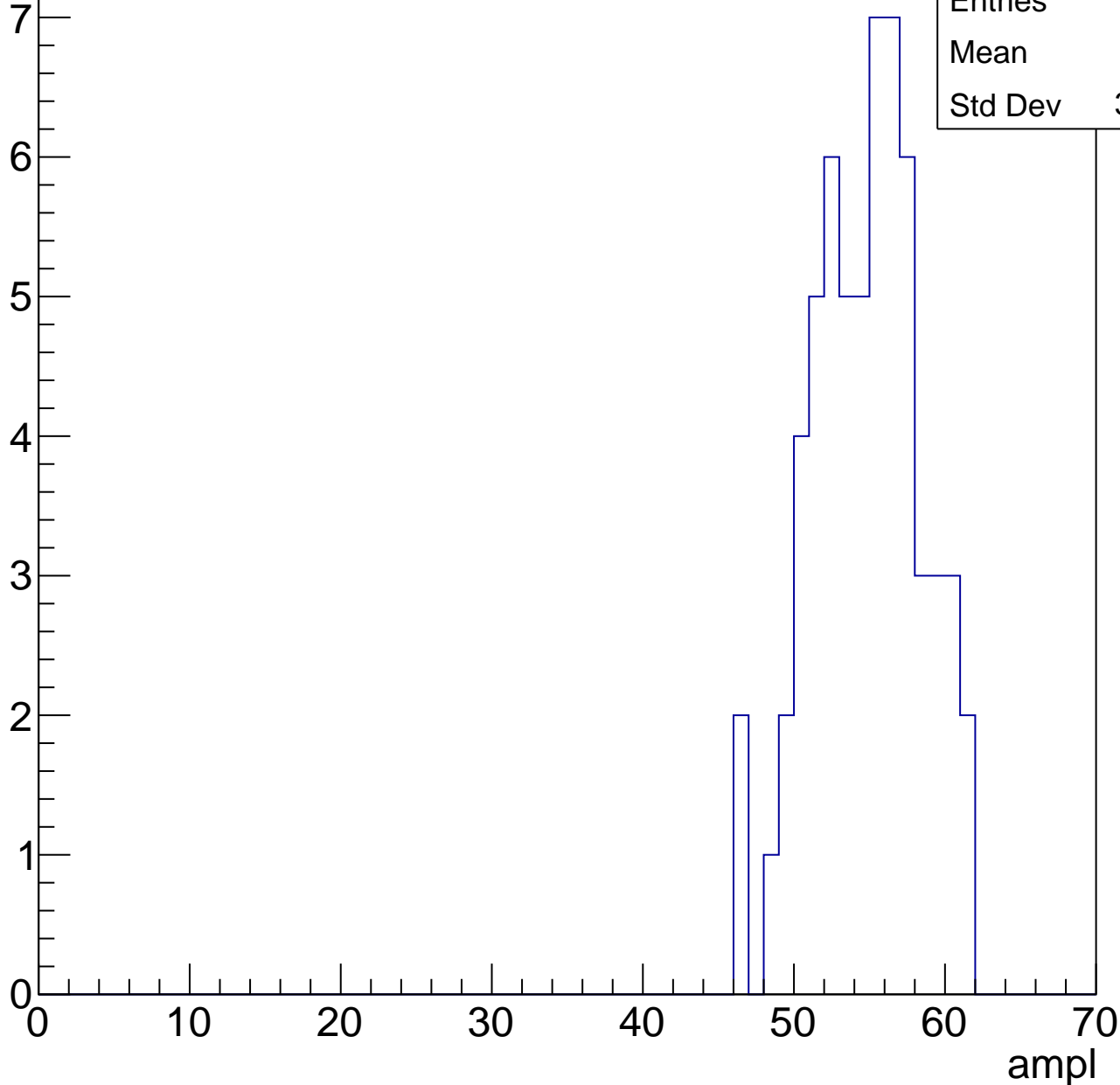


# B1L102S, U3-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	54.3
Std Dev	3.541

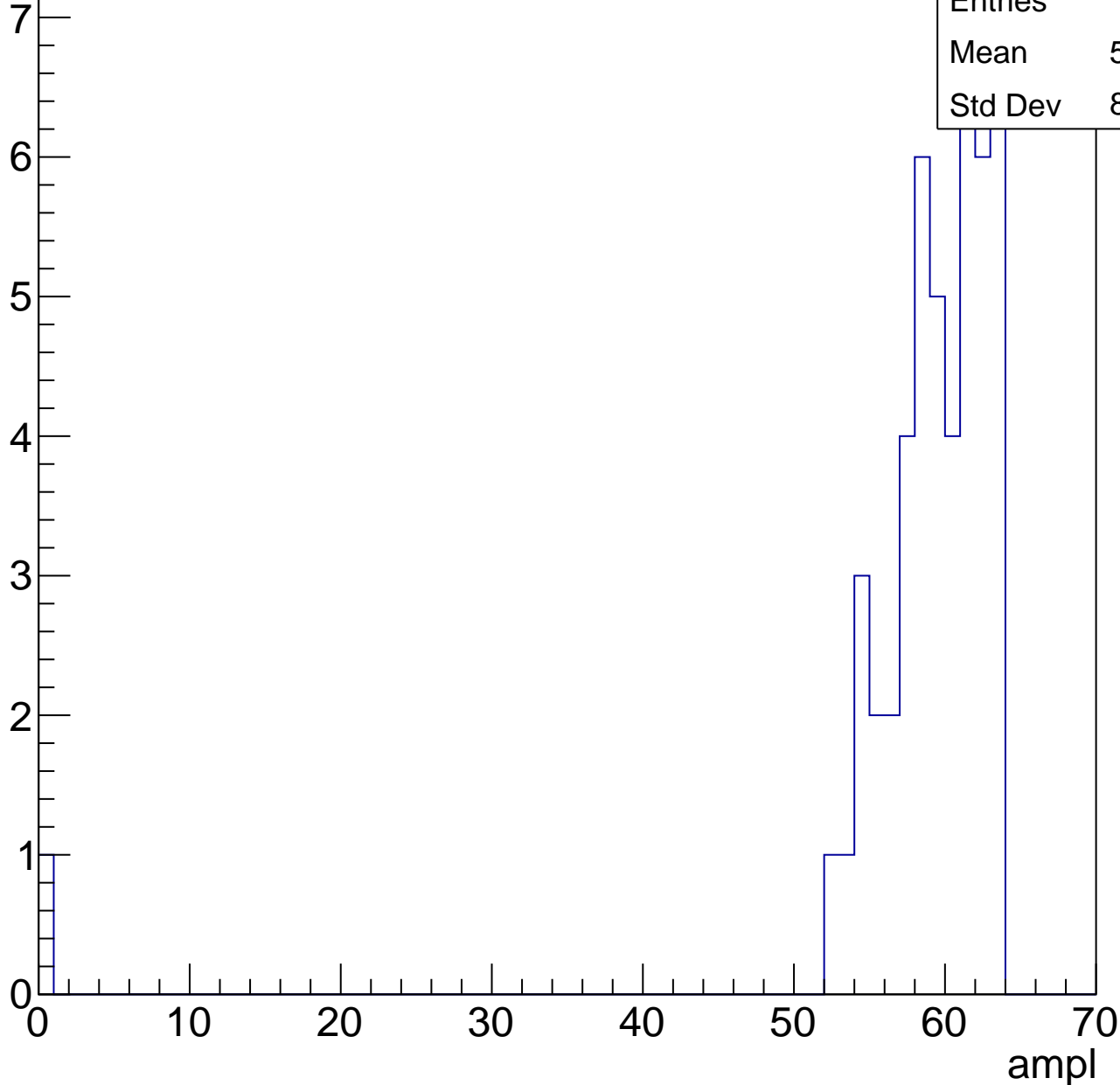


# B1L102S, U3-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

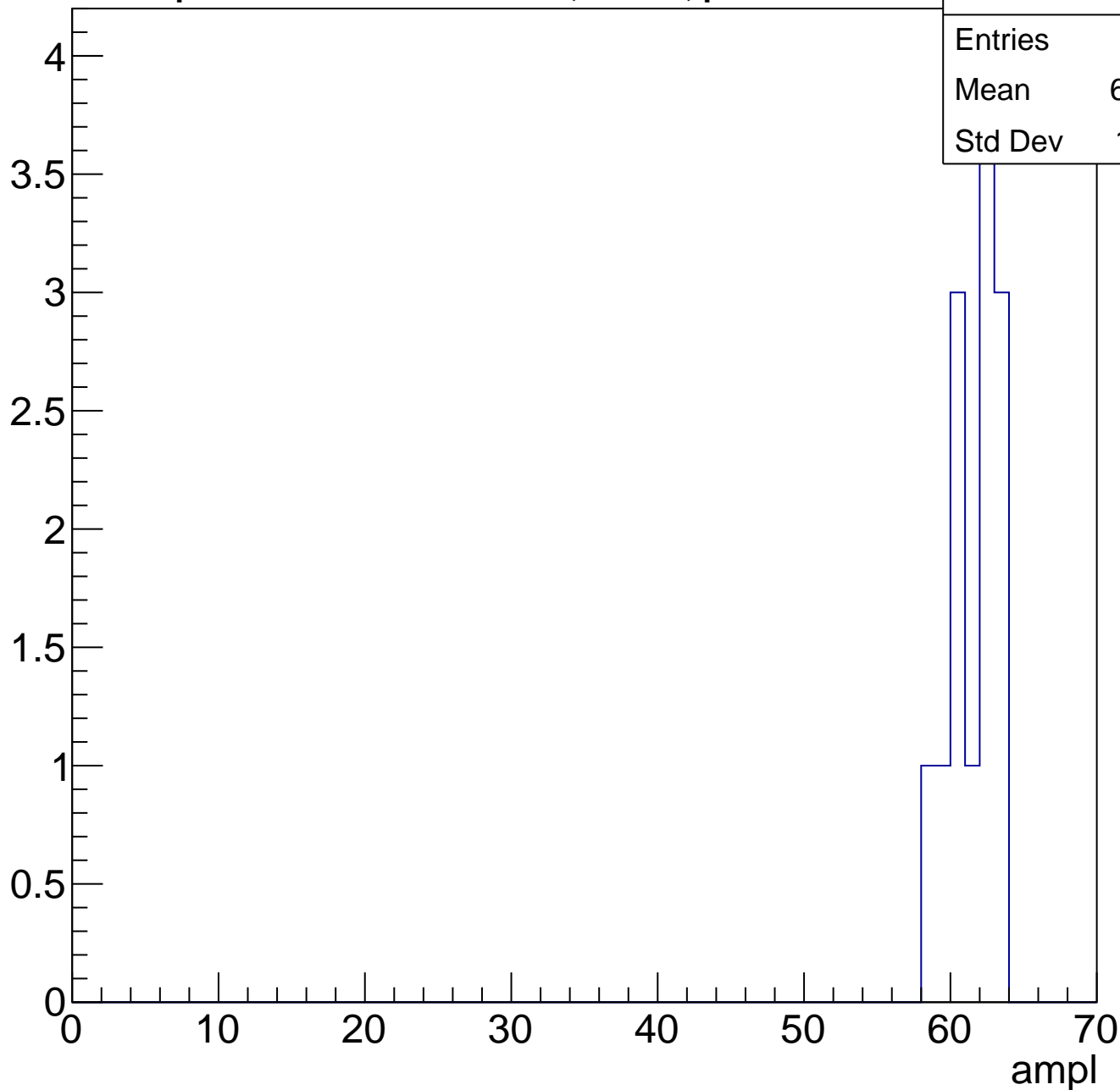
Entries	49
Mean	57.96
Std Dev	8.873



# B1L102S, U3-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

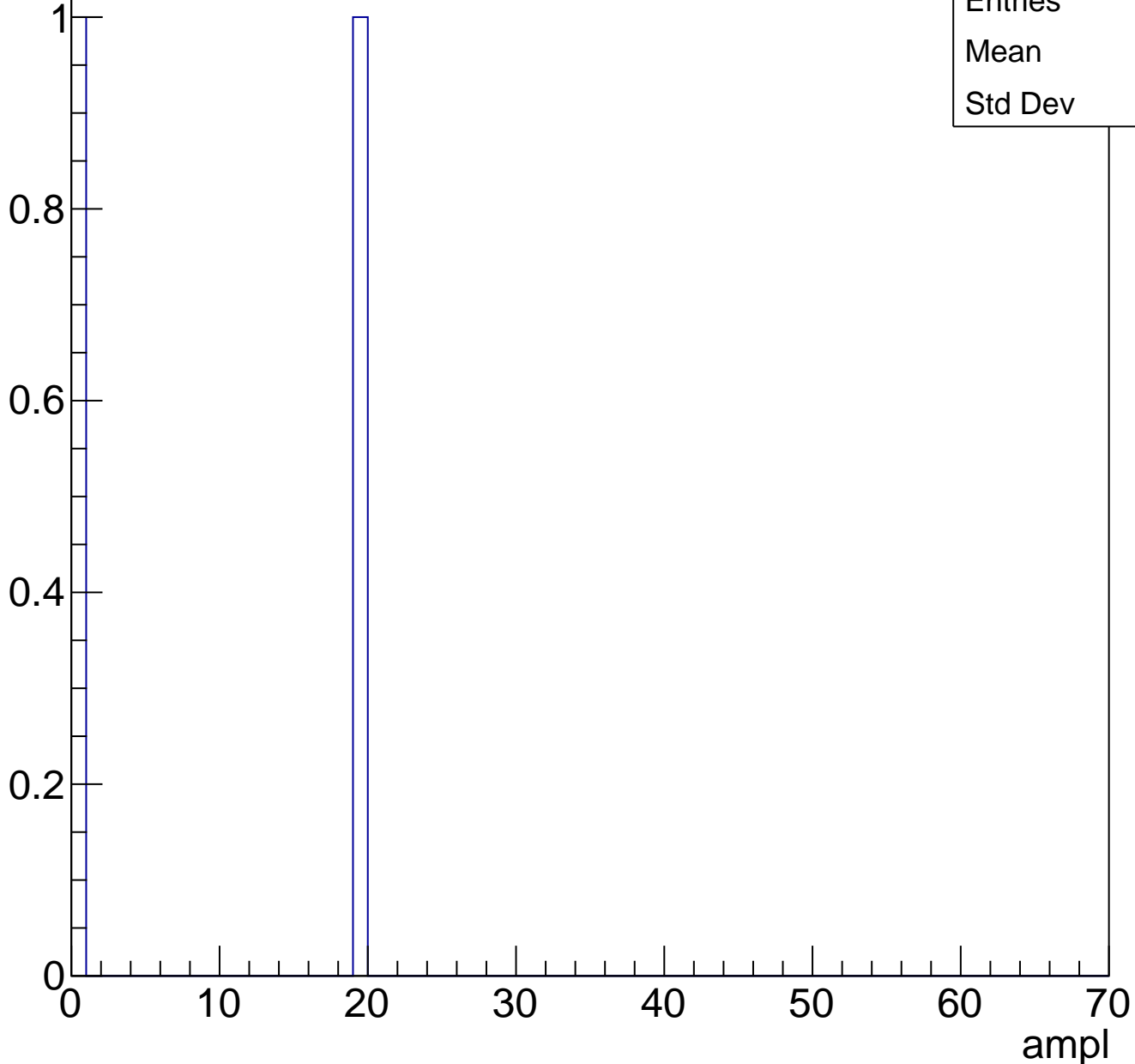




# B1L102S, U3-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	9.5
Std Dev	9.5

# B1L102S, U3-ch10, adc0

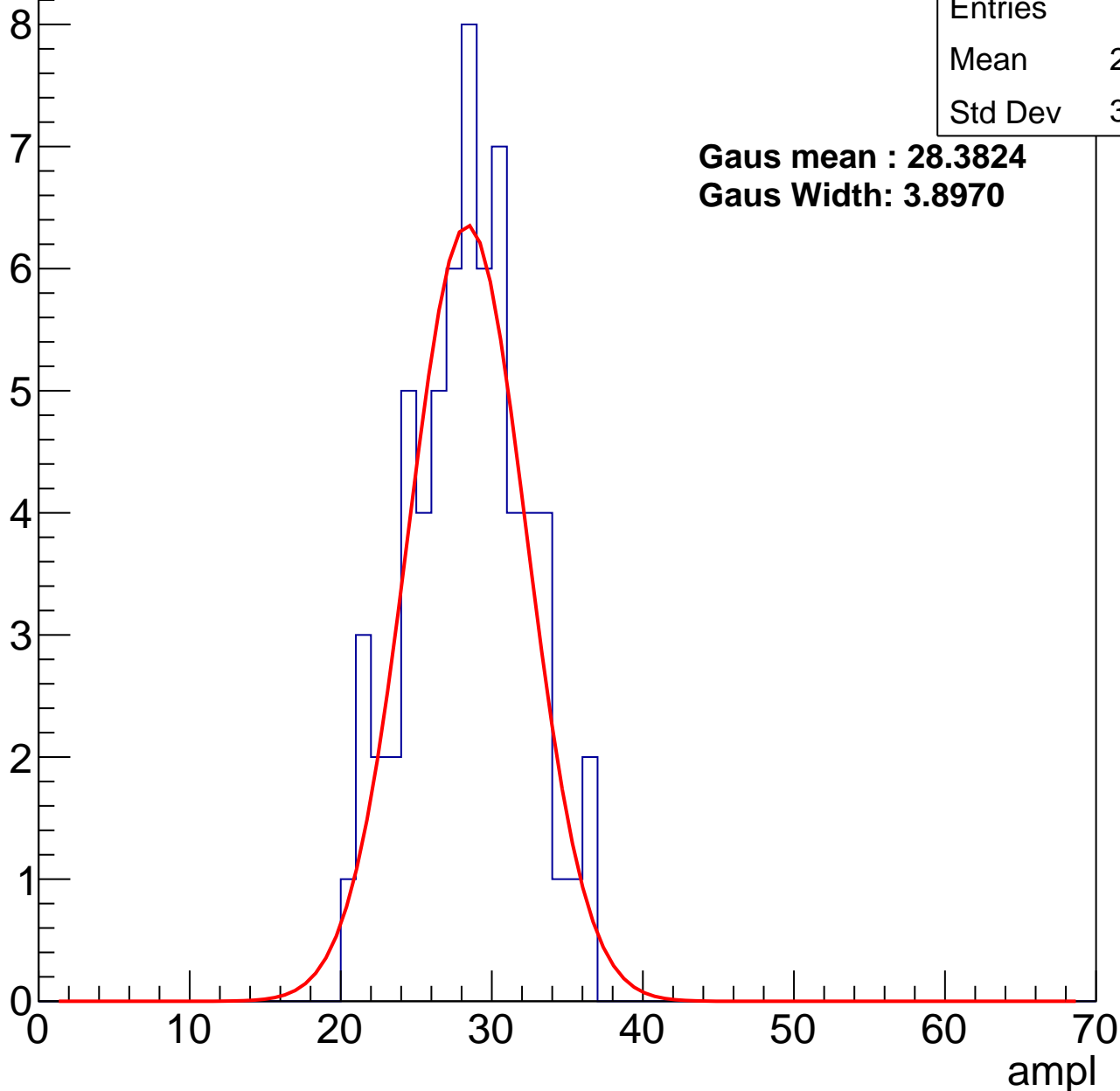
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	27.97
Std Dev	3.766

**Gaus mean : 28.3824**

**Gaus Width: 3.8970**



# B1L102S, U3-ch10, adc1

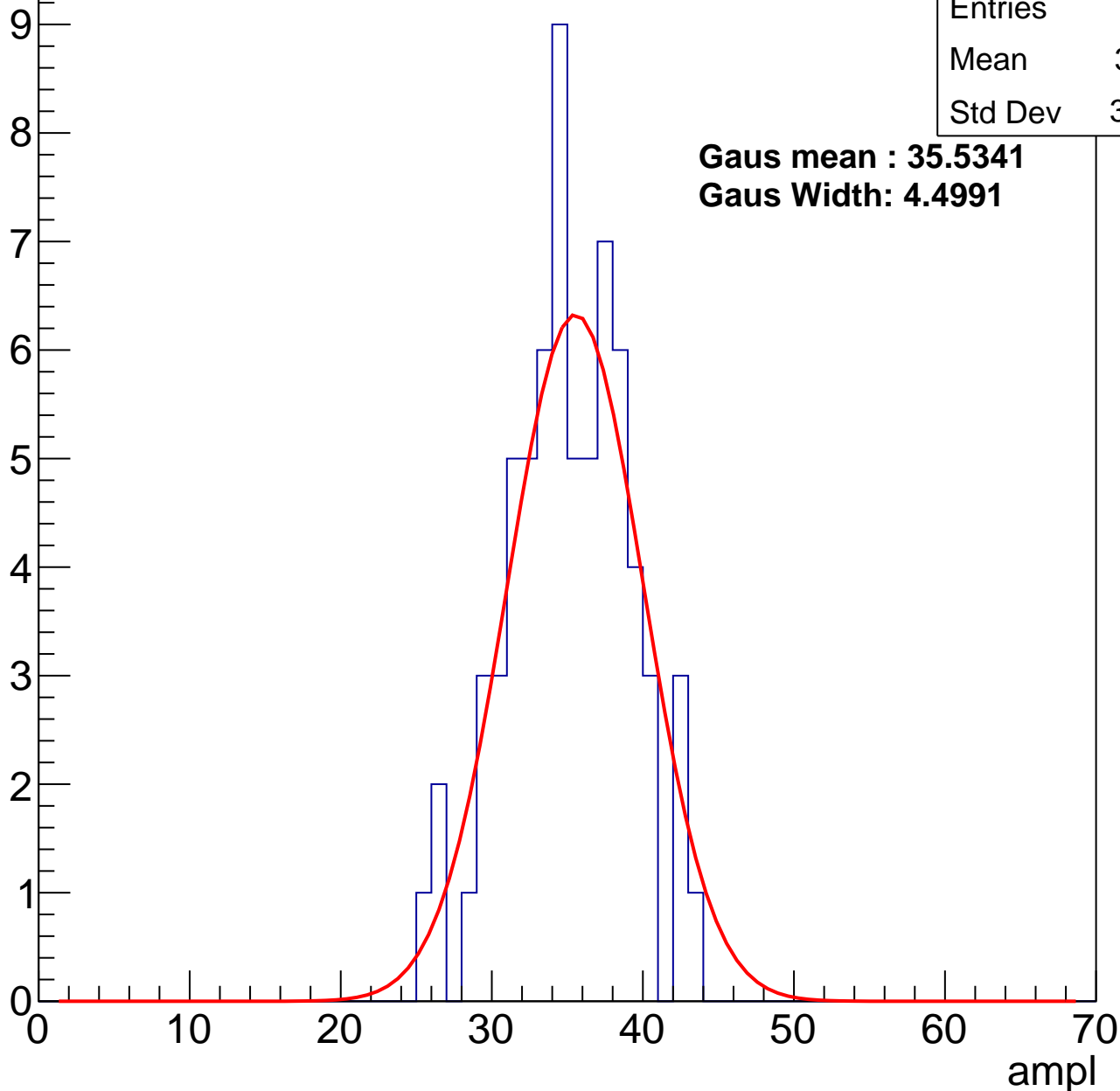
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	34.61
Std Dev	3.953

**Gaus mean : 35.5341**

**Gaus Width: 4.4991**



# B1L102S, U3-ch10, adc2

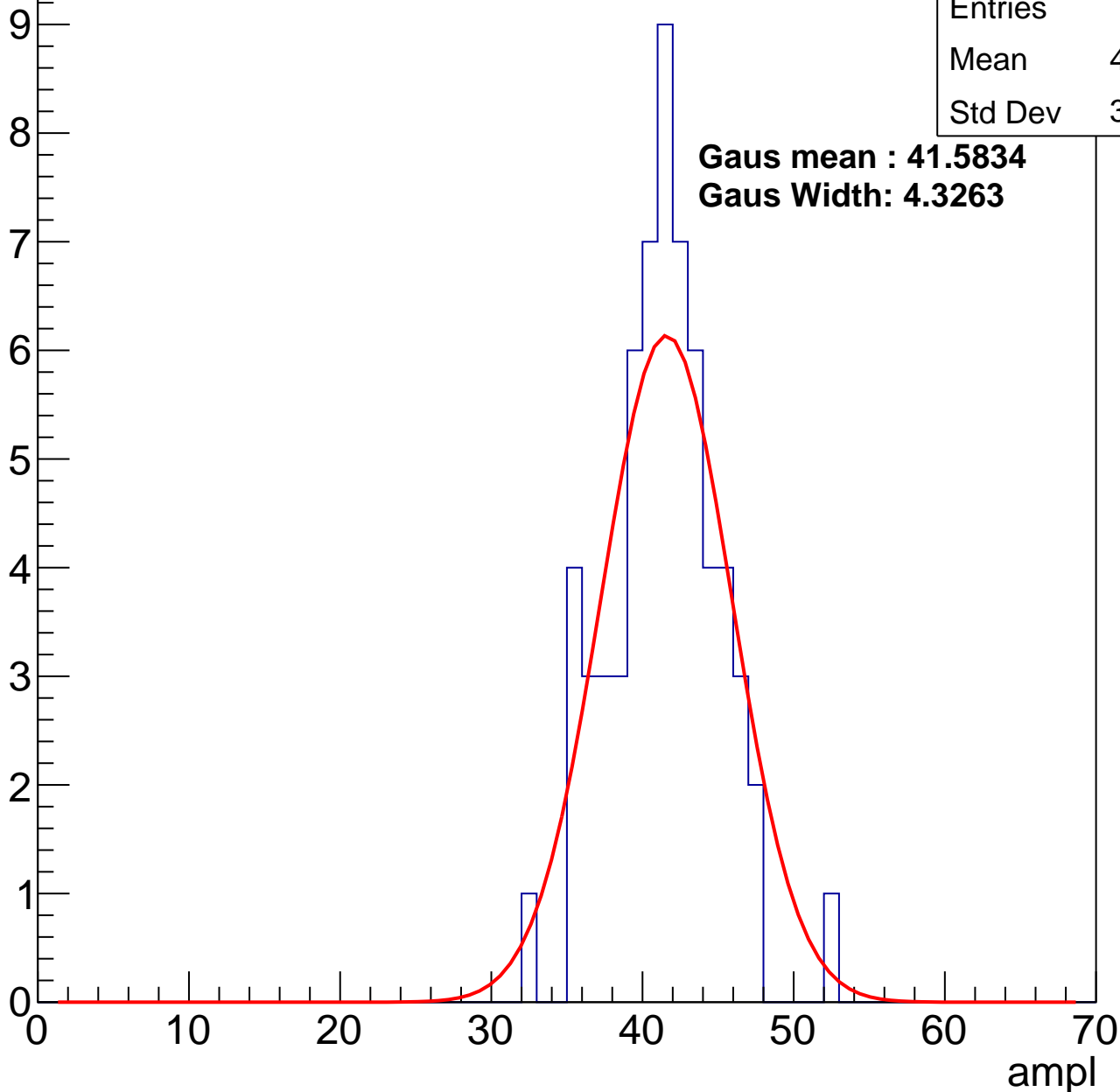
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	40.95
Std Dev	3.574

**Gaus mean : 41.5834**

**Gaus Width: 4.3263**

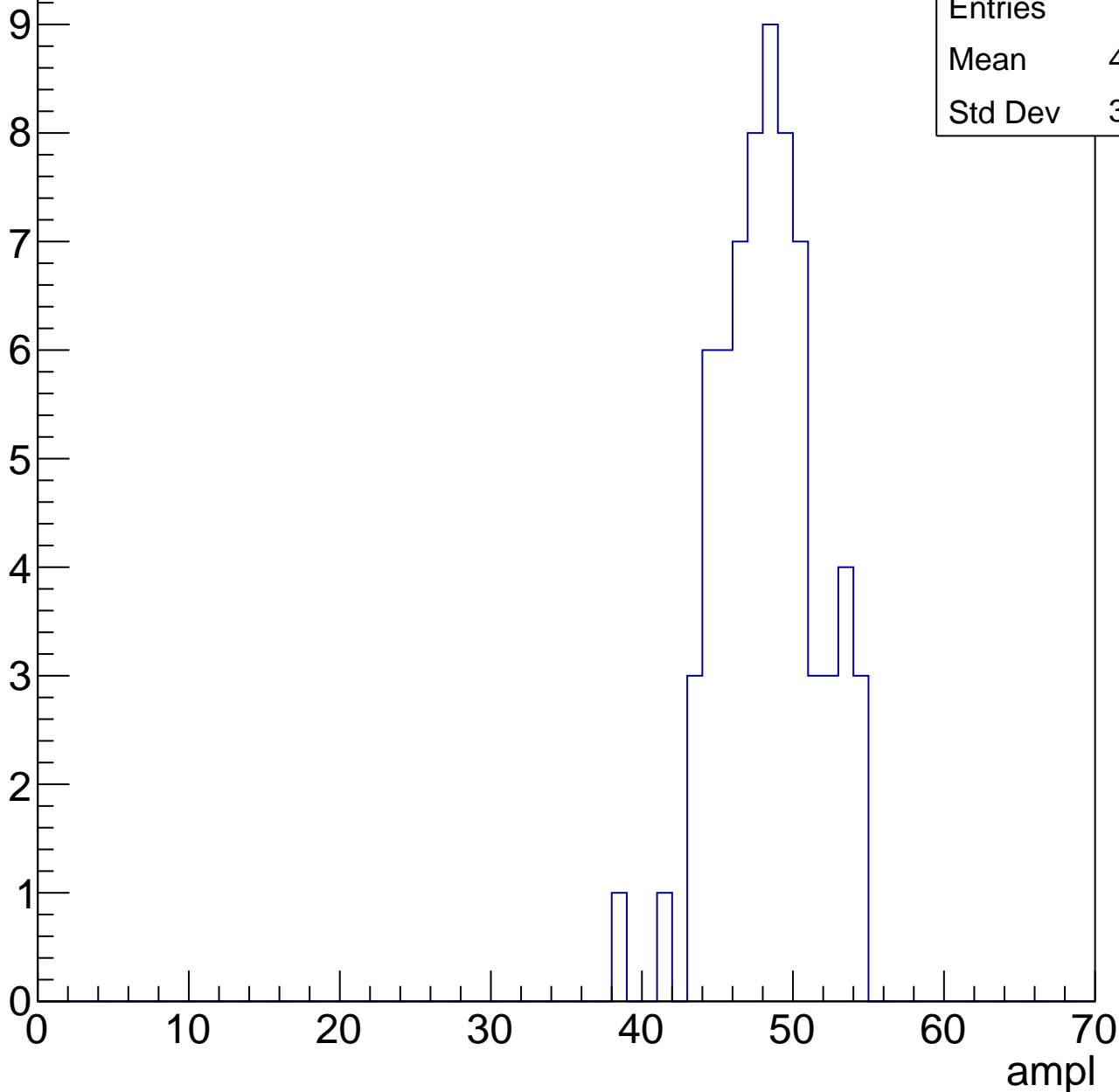


# B1L102S, U3-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	47.78
Std Dev	3.243

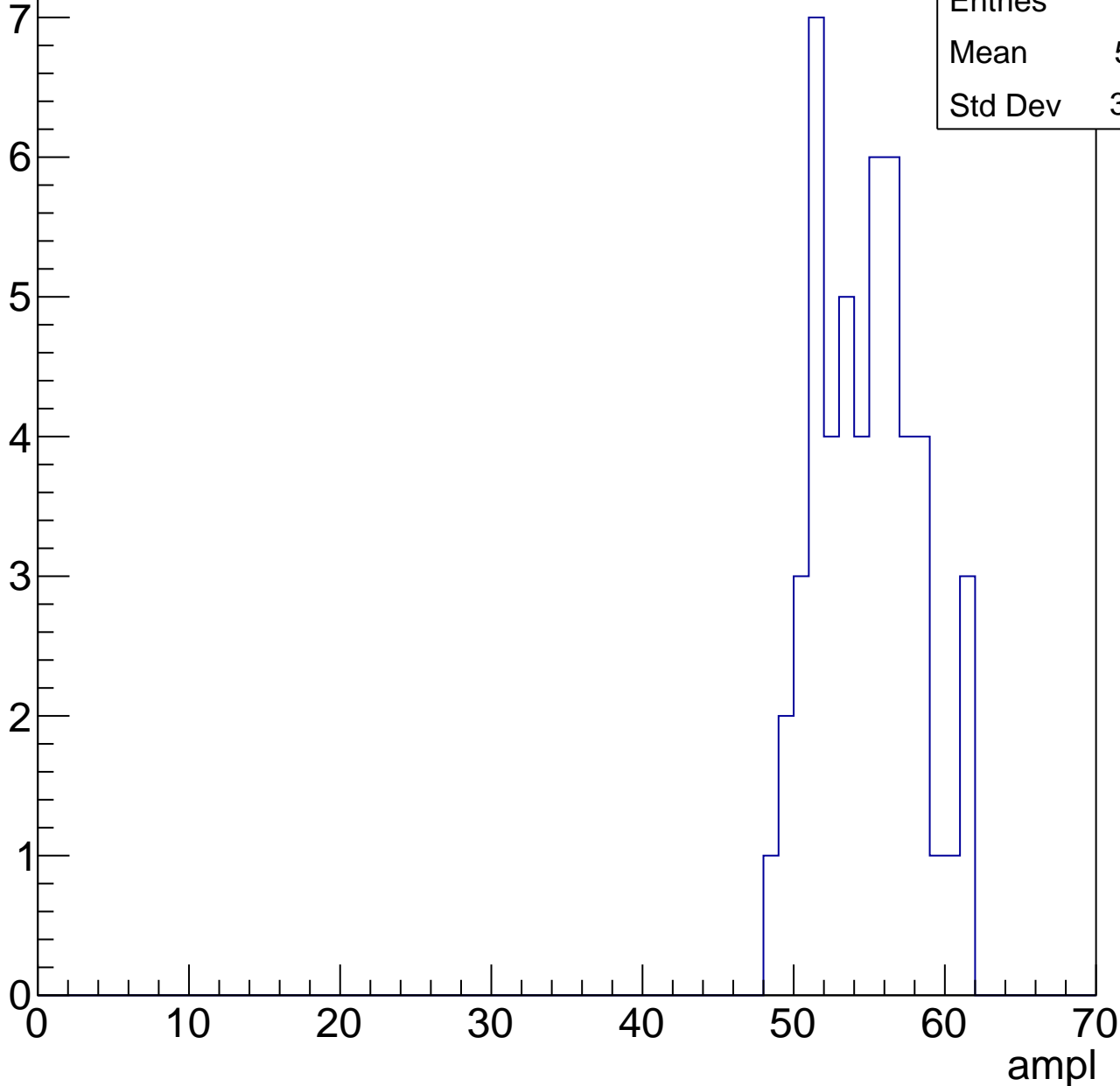


# B1L102S, U3-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	54.31
Std Dev	3.287

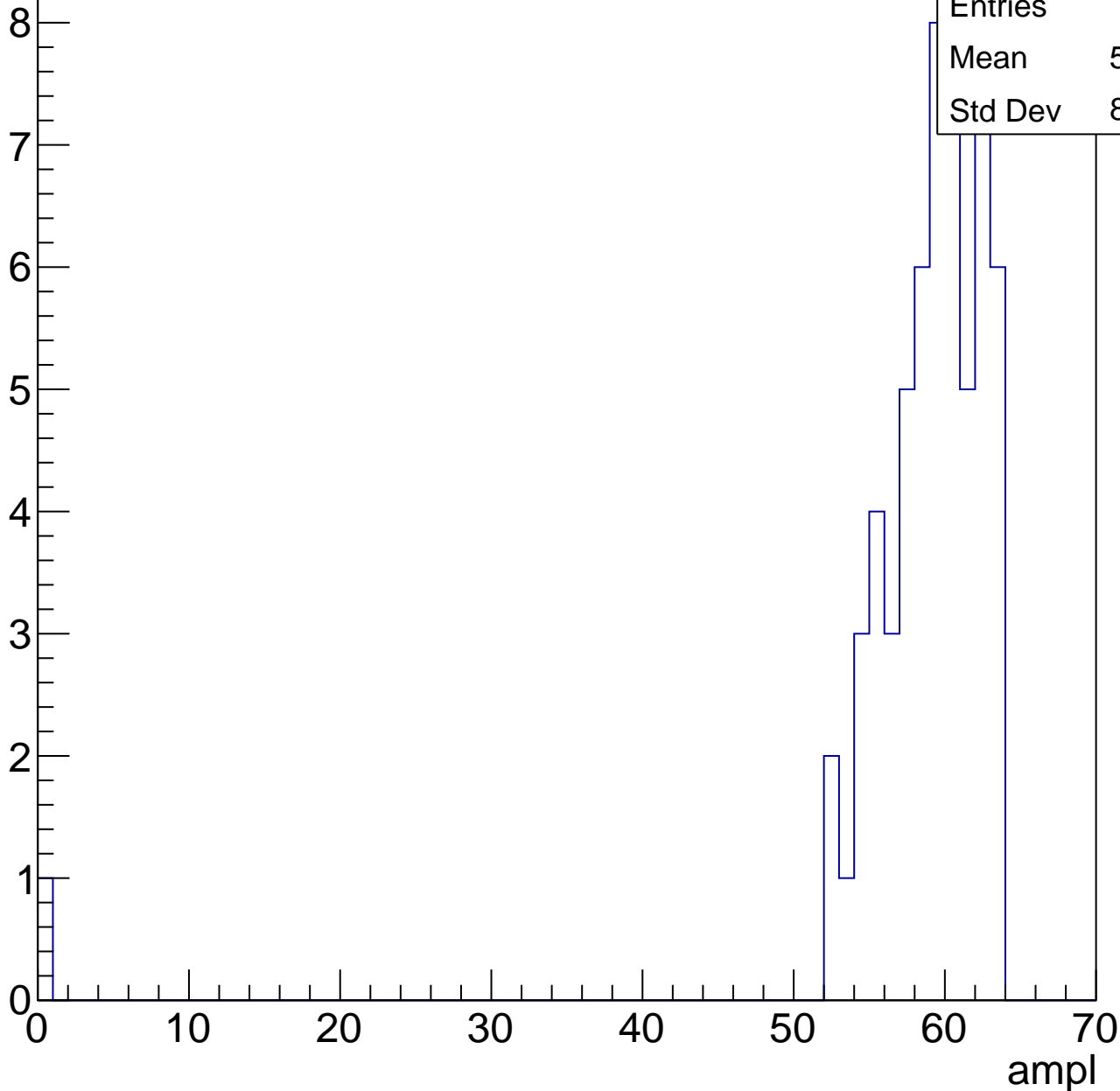


# B1L102S, U3-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

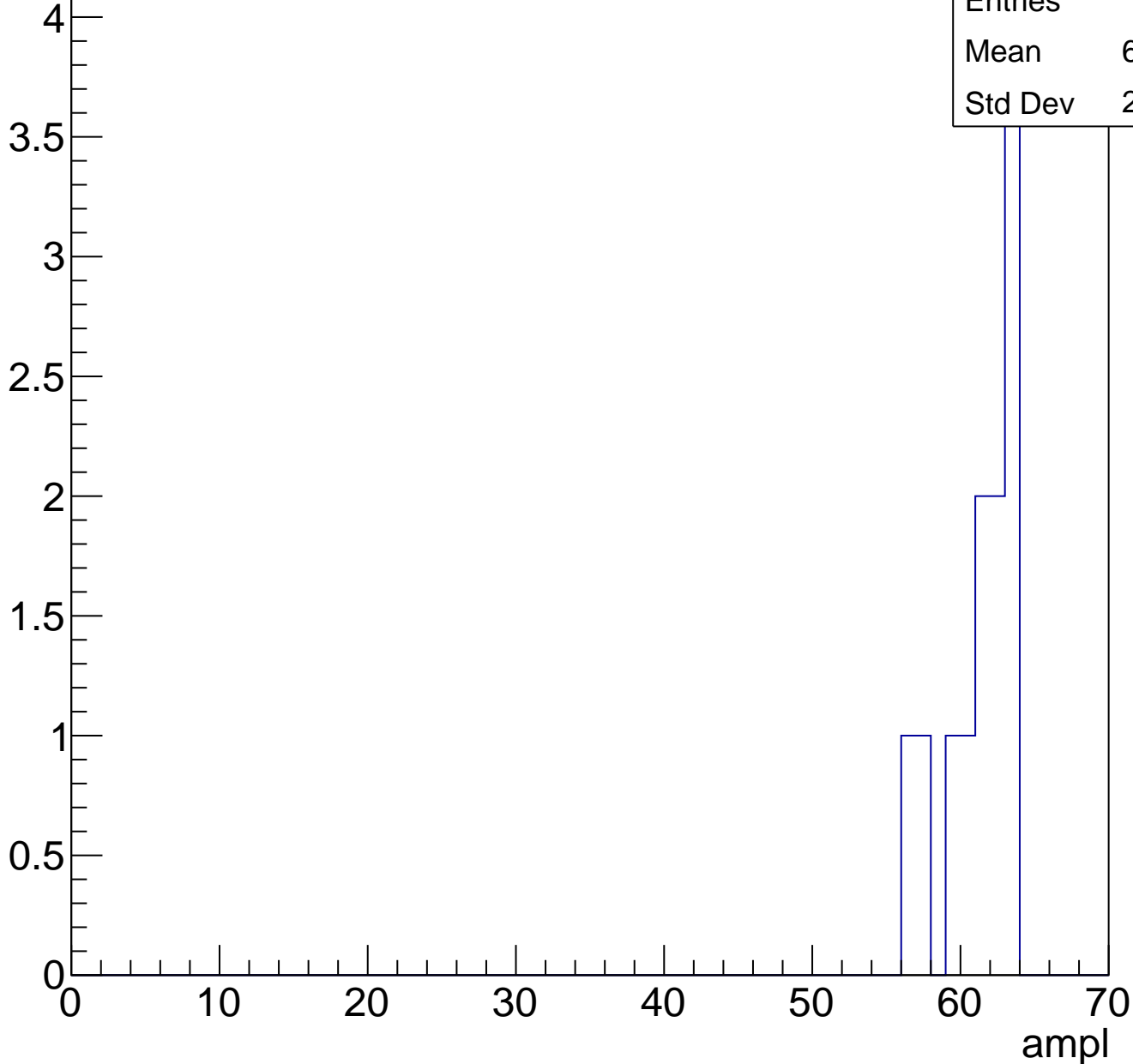
Entries	60
Mean	57.85
Std Dev	8.087



# B1L102S, U3-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U3-ch11, adc0

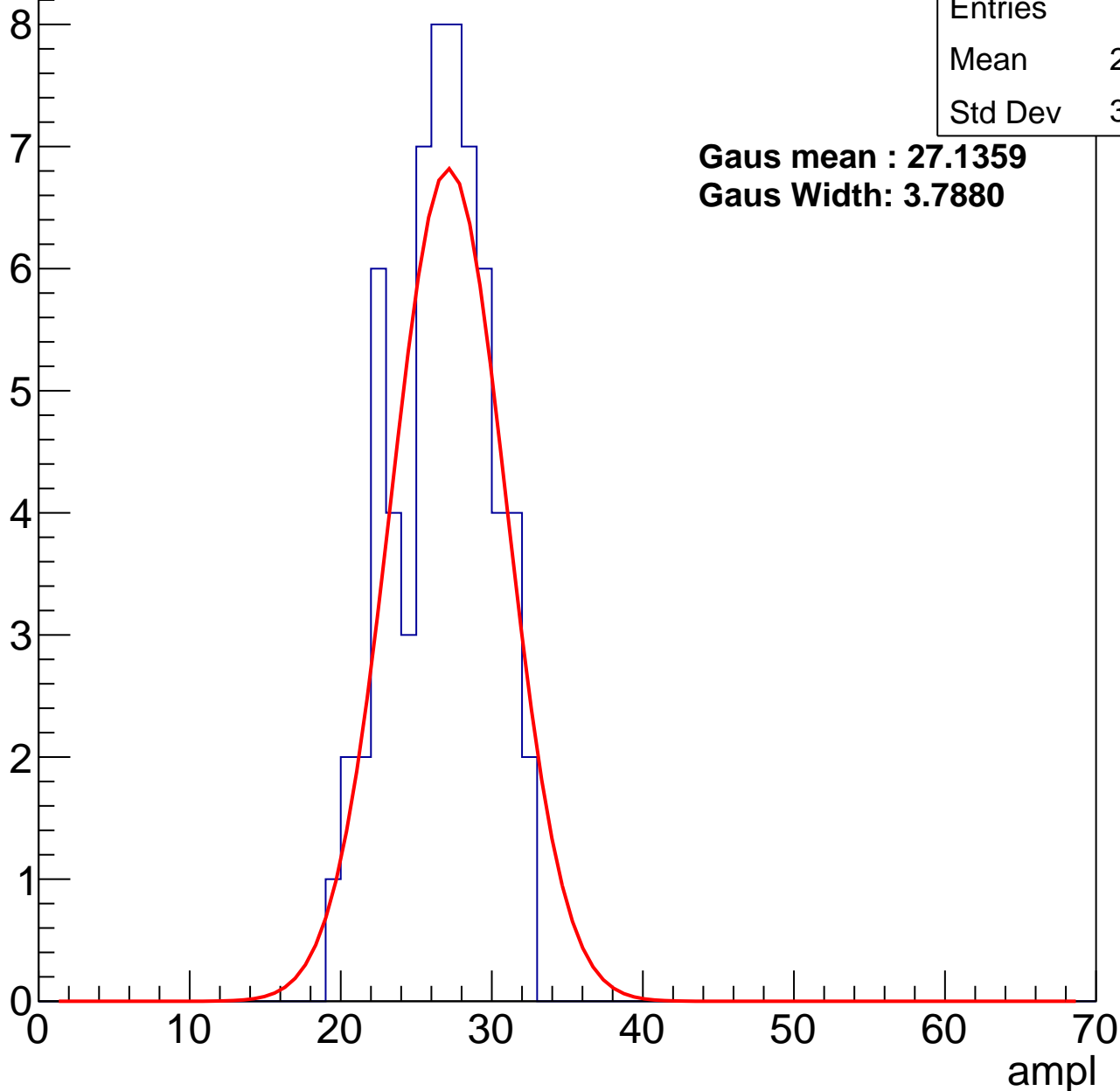
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	26.16
Std Dev	3.178

**Gaus mean : 27.1359**

**Gaus Width: 3.7880**



# B1L102S, U3-ch11, adc1

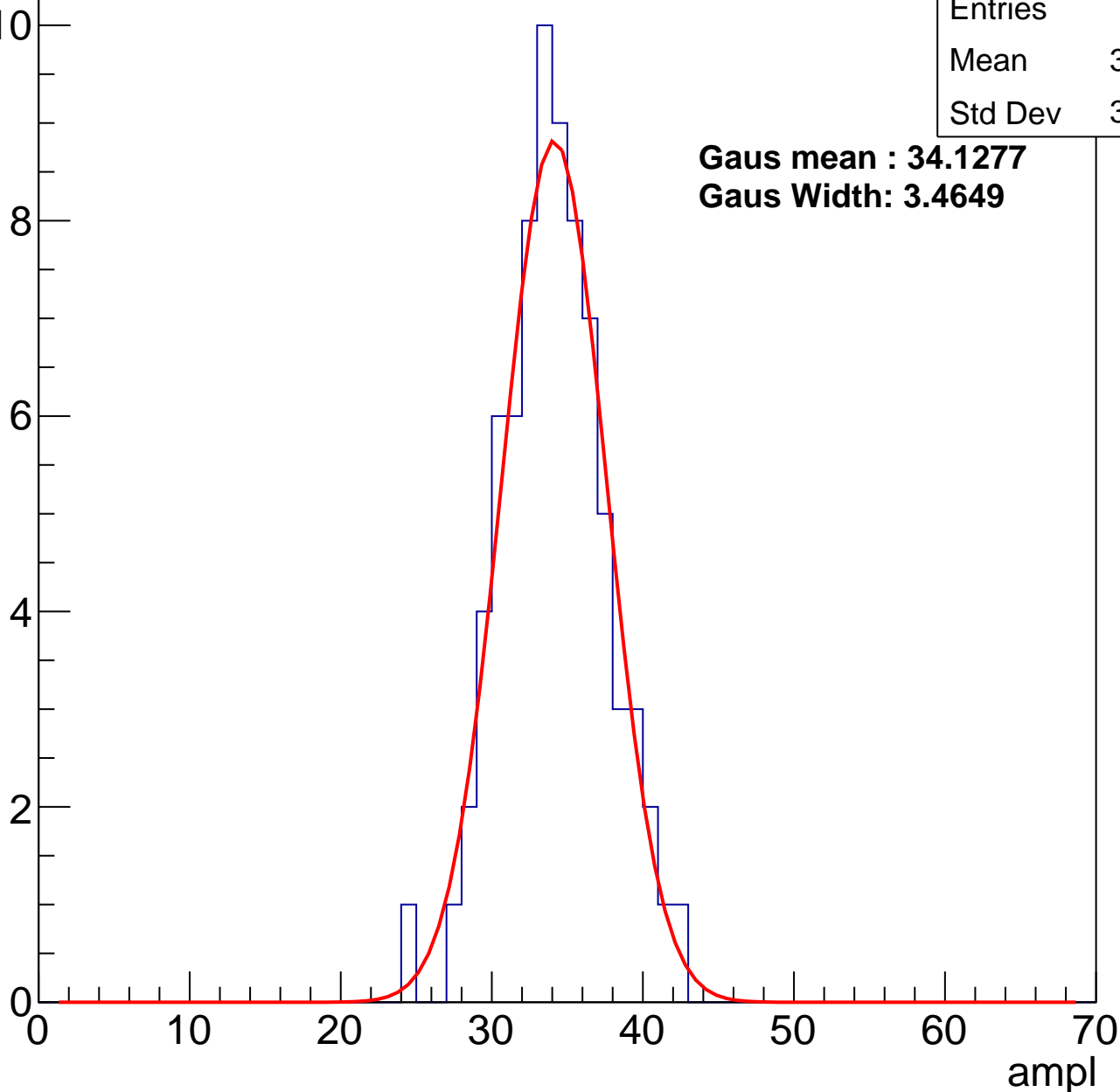
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	33.66
Std Dev	3.406

**Gaus mean : 34.1277**

**Gaus Width: 3.4649**



# B1L102S, U3-ch11, adc2

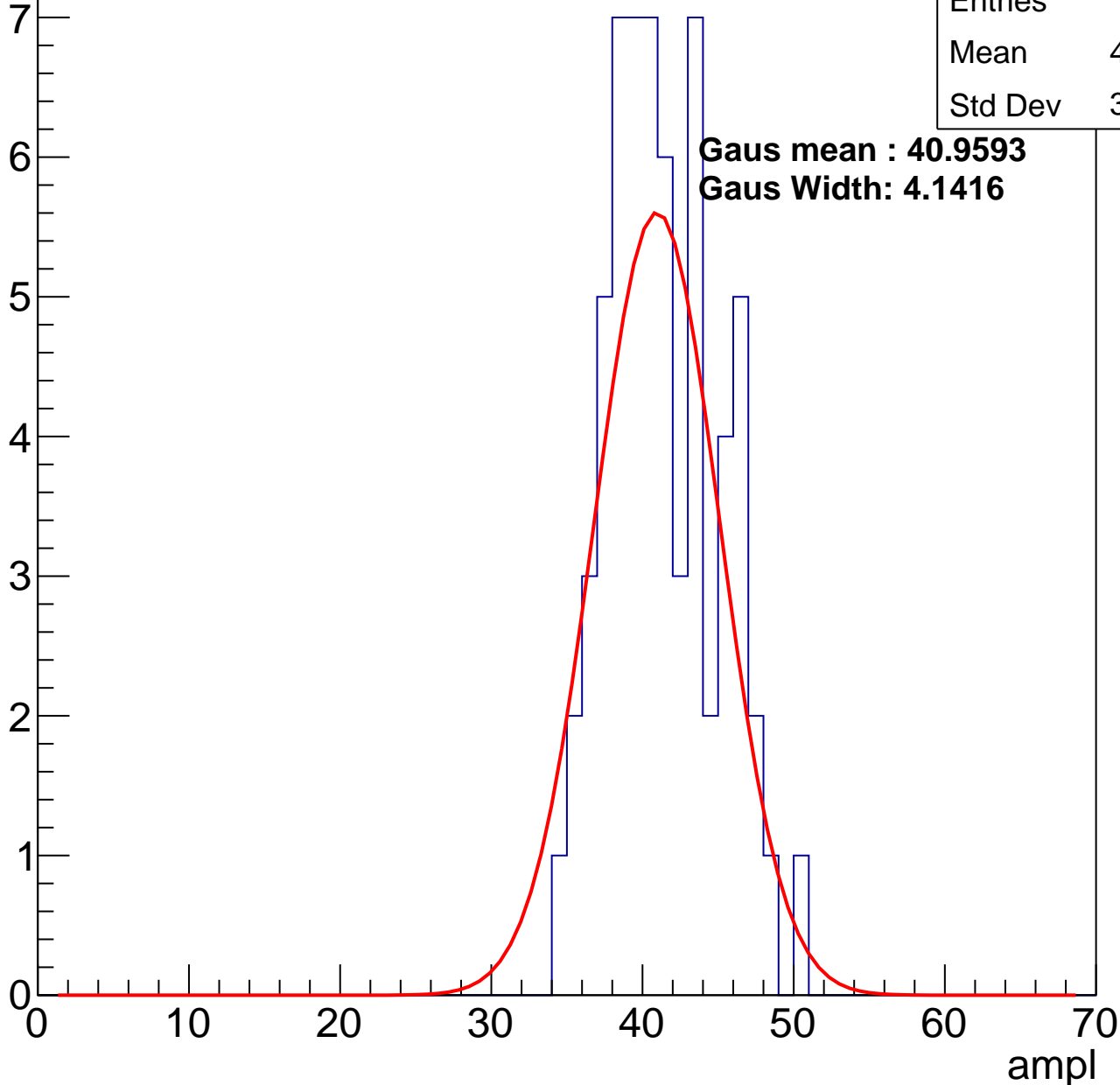
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	40.94
Std Dev	3.594

**Gaus mean : 40.9593**

**Gaus Width: 4.1416**

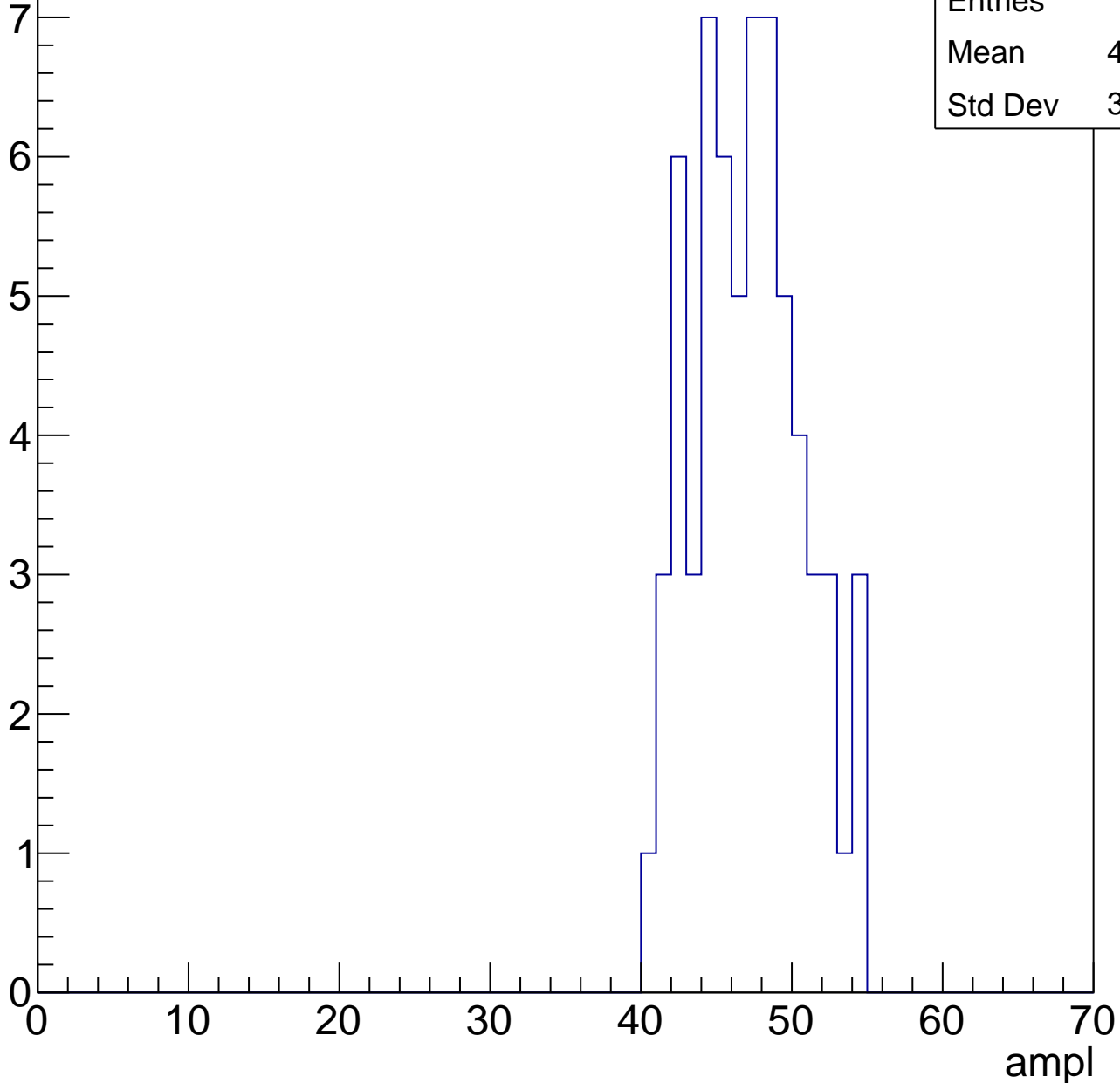


# B1L102S, U3-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	46.66
Std Dev	3.554

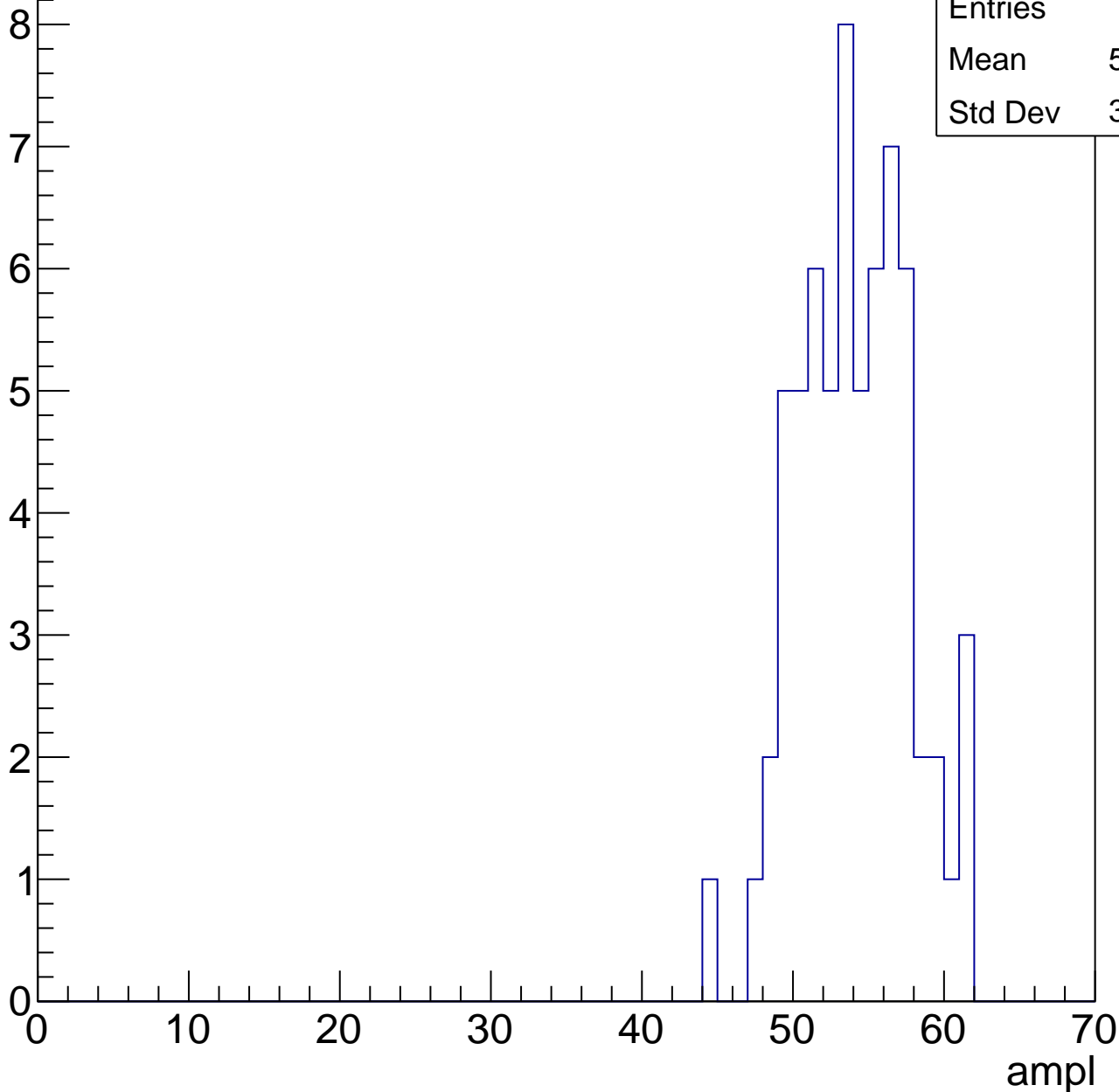


# B1L102S, U3-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	53.58
Std Dev	3.616

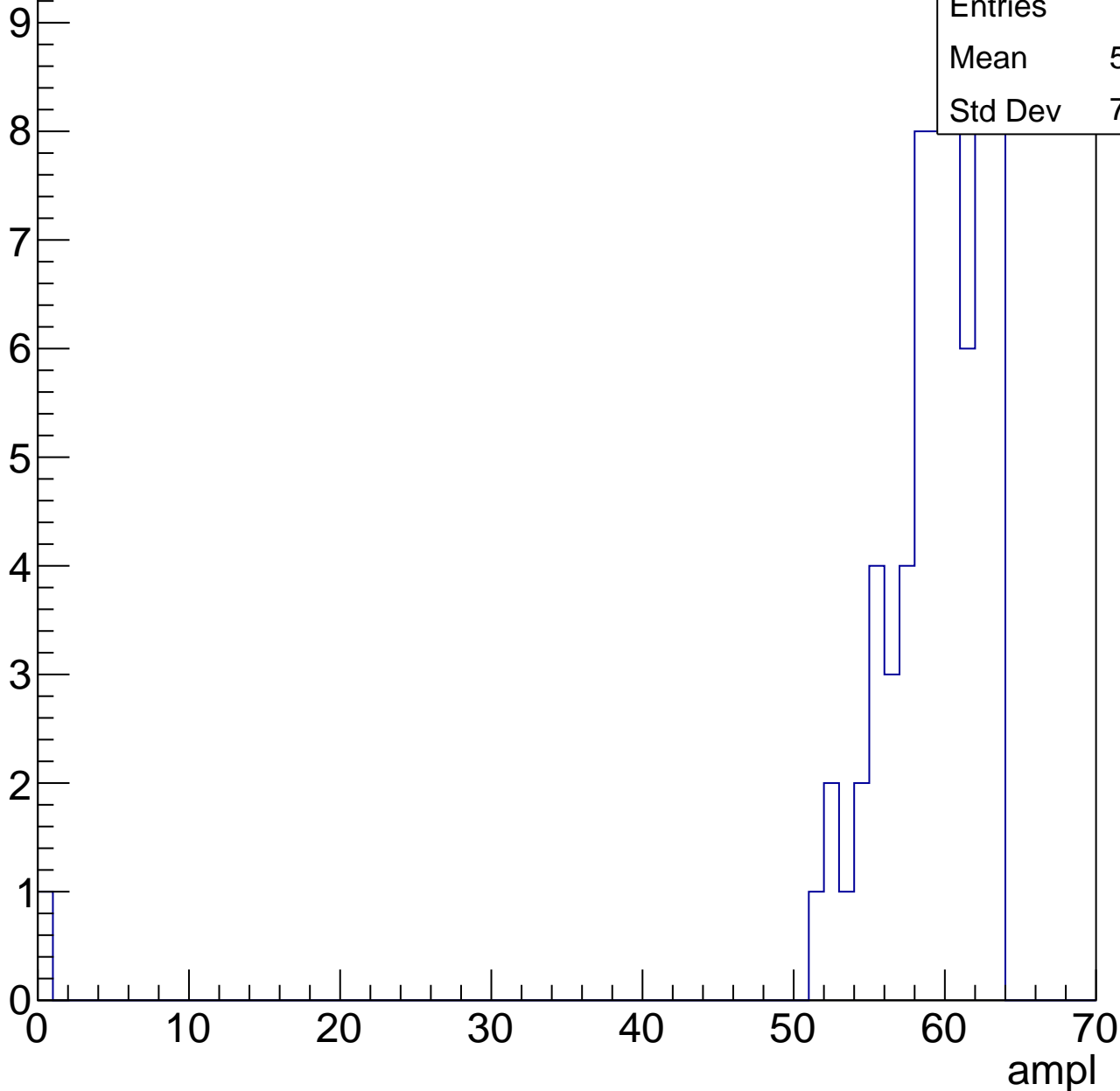


# B1L102S, U3-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

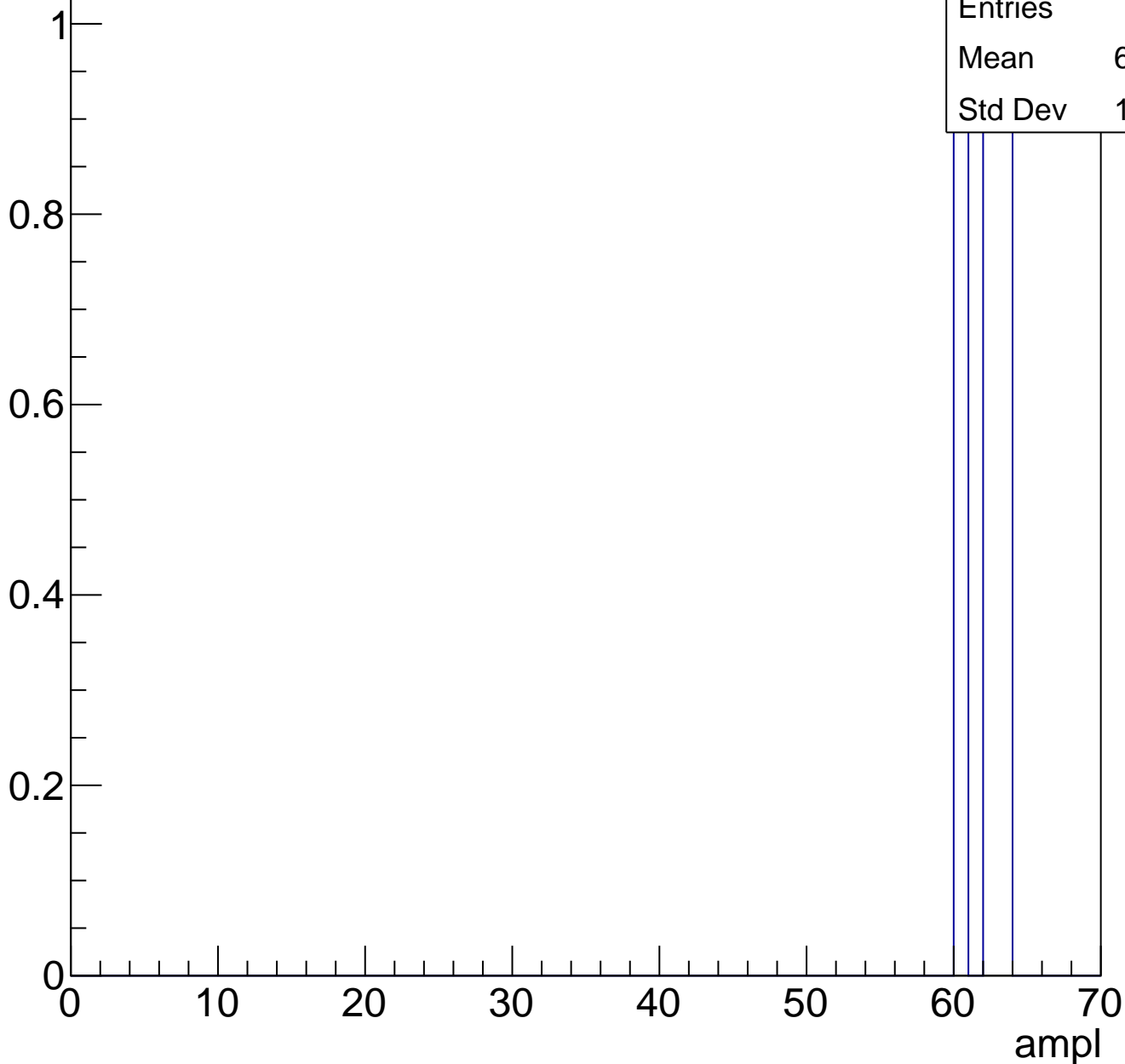
Entries	65
Mean	58.09
Std Dev	7.875



# B1L102S, U3-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch12, adc0

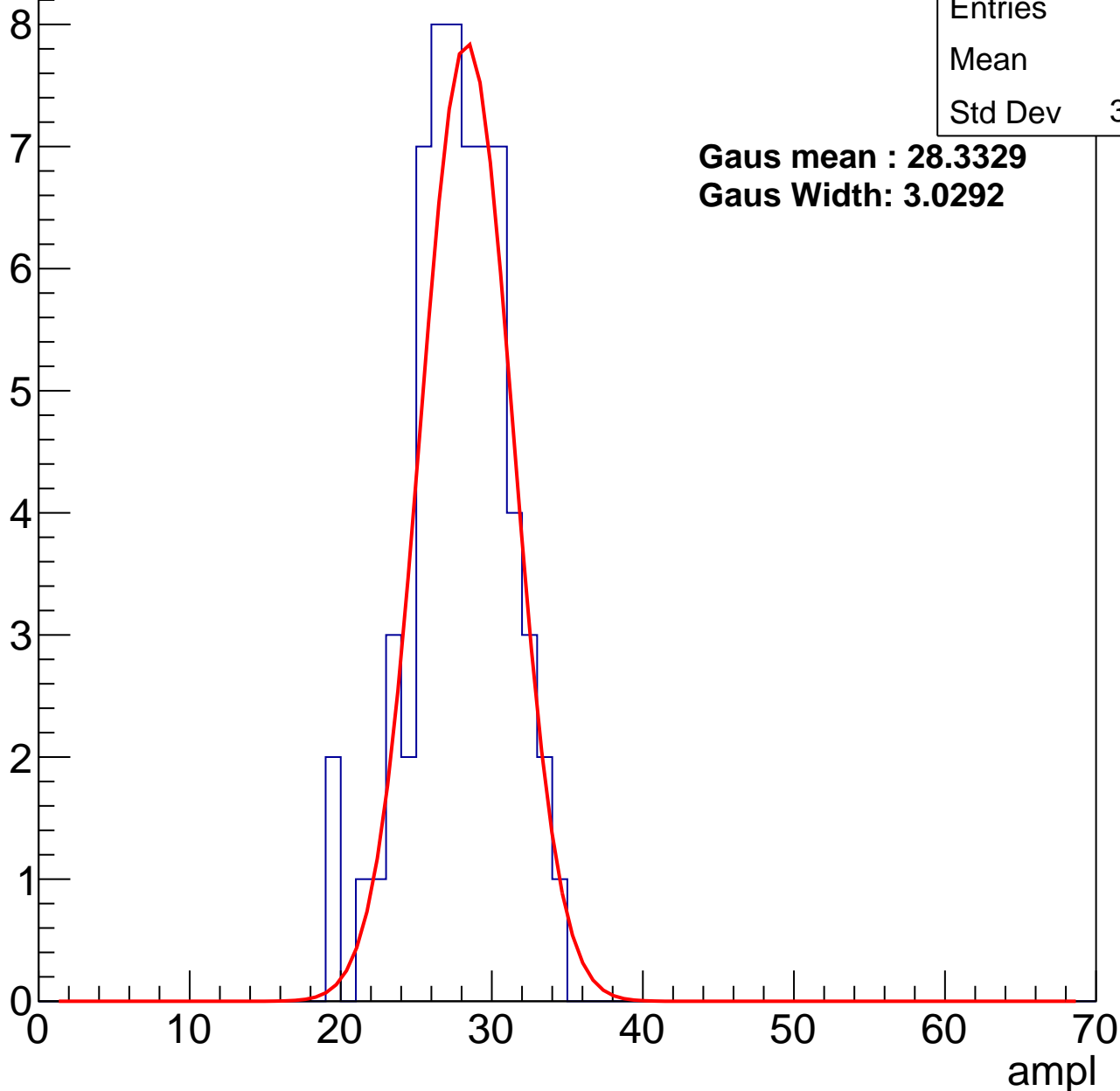
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	27.4
Std Dev	3.185

**Gaus mean : 28.3329**

**Gaus Width: 3.0292**



# B1L102S, U3-ch12, adc1

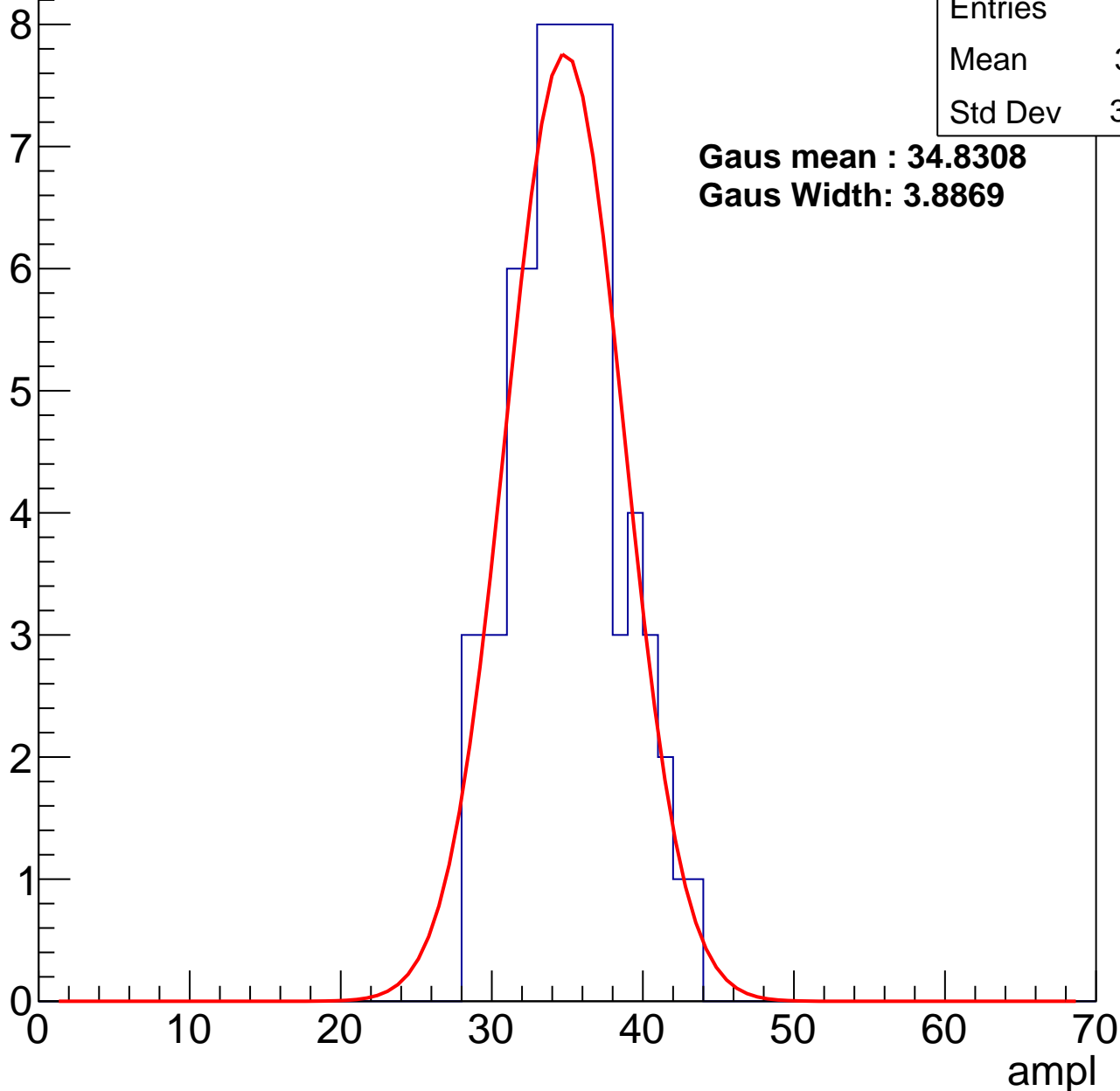
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	34.61
Std Dev	3.464

**Gaus mean : 34.8308**

**Gaus Width: 3.8869**

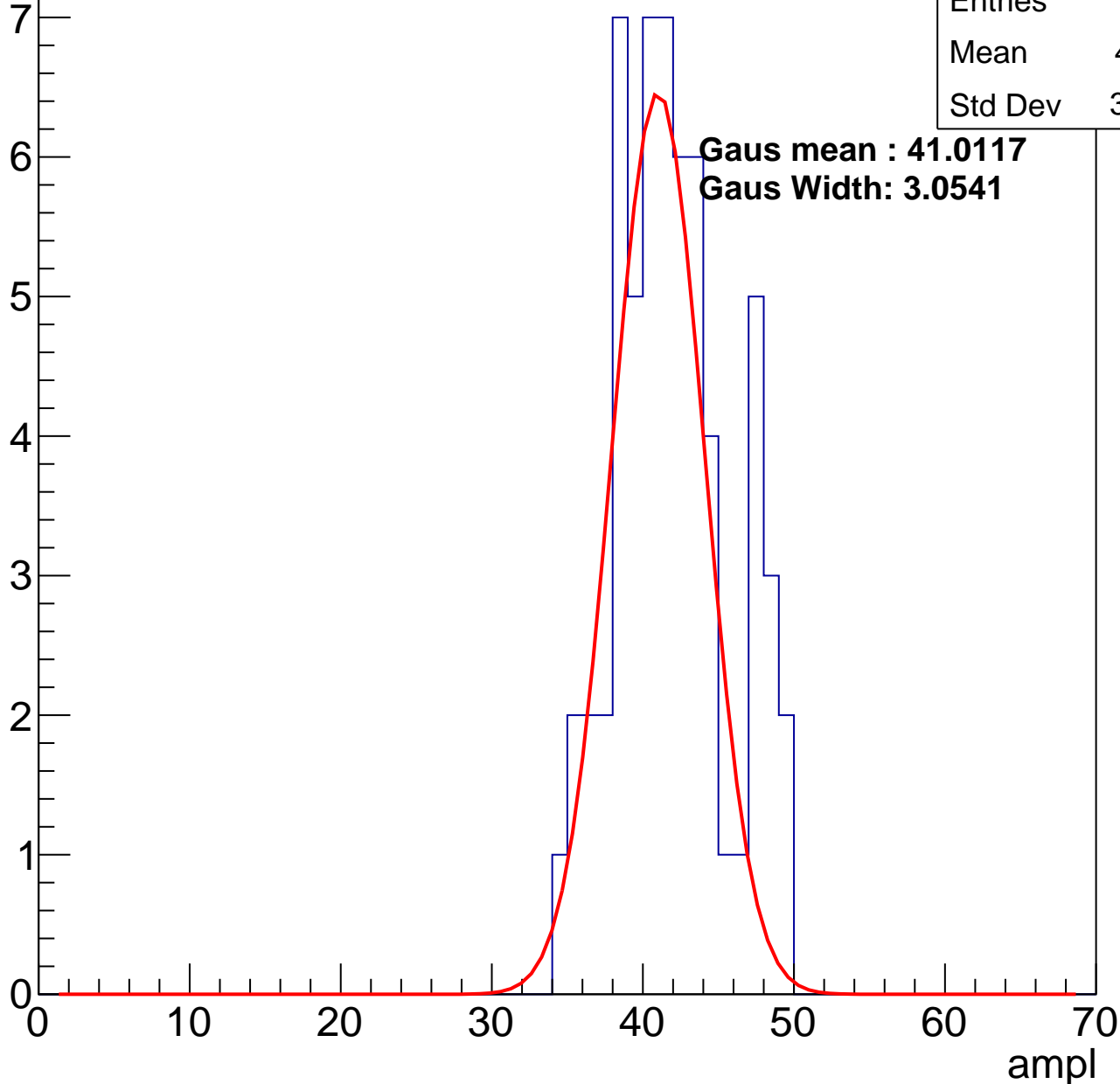


# B1L102S, U3-ch12, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

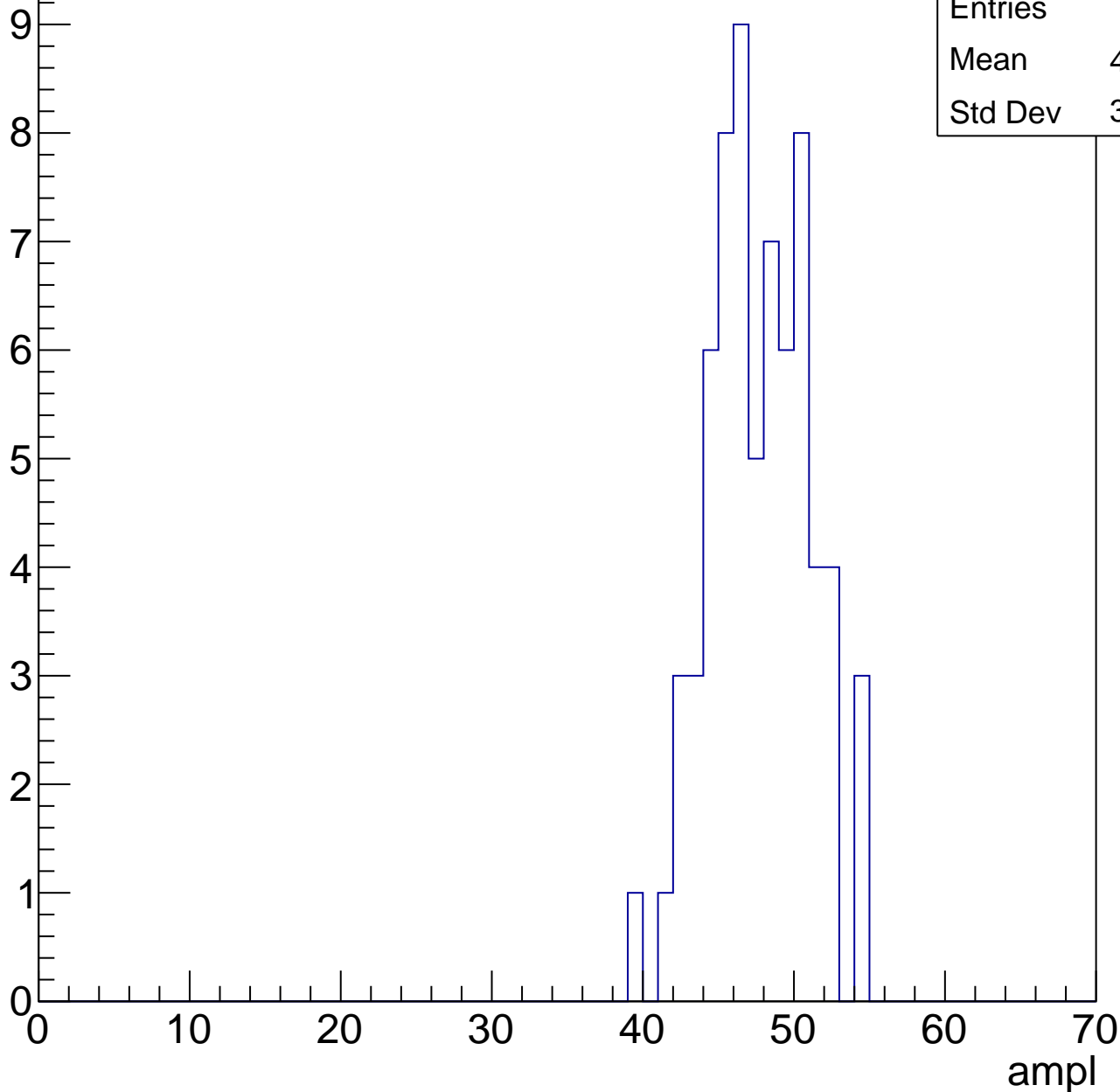
Entries	61
Mean	41.51
Std Dev	3.709



# B1L102S, U3-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



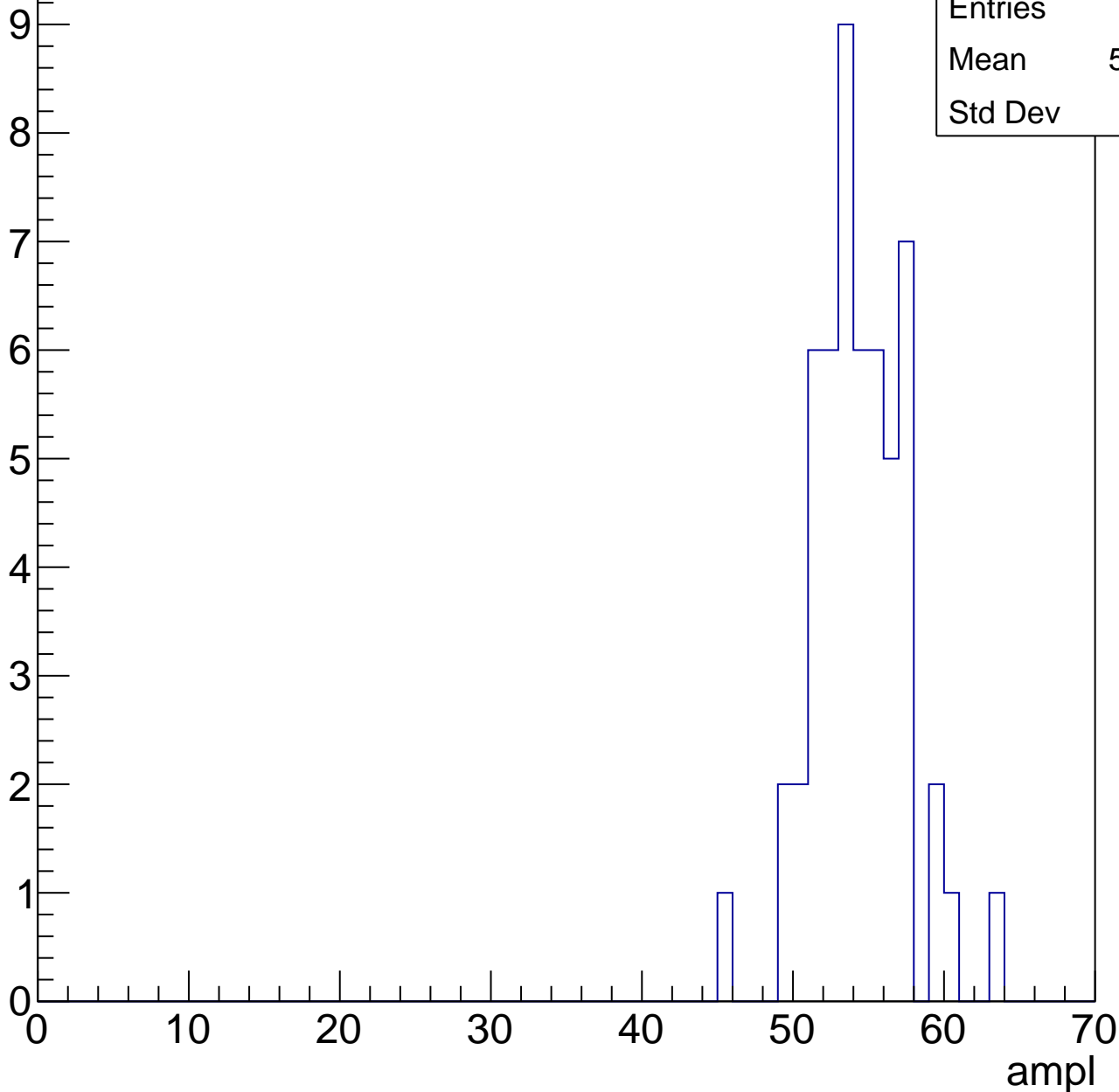
Entries	68
Mean	47.24
Std Dev	3.273

# B1L102S, U3-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	53.93
Std Dev	3.06



# B1L102S, U3-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	63
Mean	59.21
Std Dev	2.571

Entry

10

8

6

4

2

0

0

10

20

30

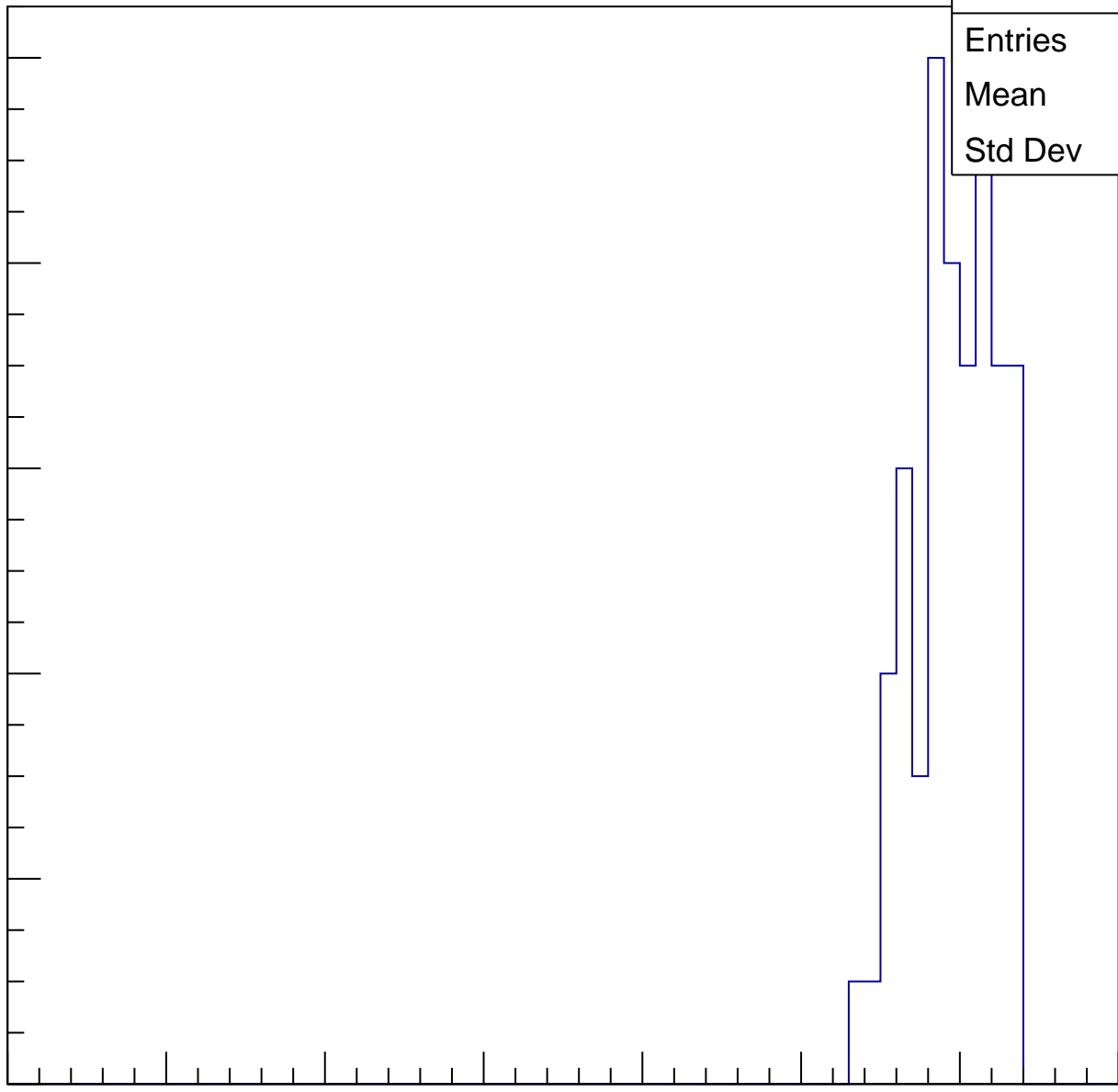
40

50

60

70

ampl



# B1L102S, U3-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	8
Mean	53.88
Std Dev	20.39

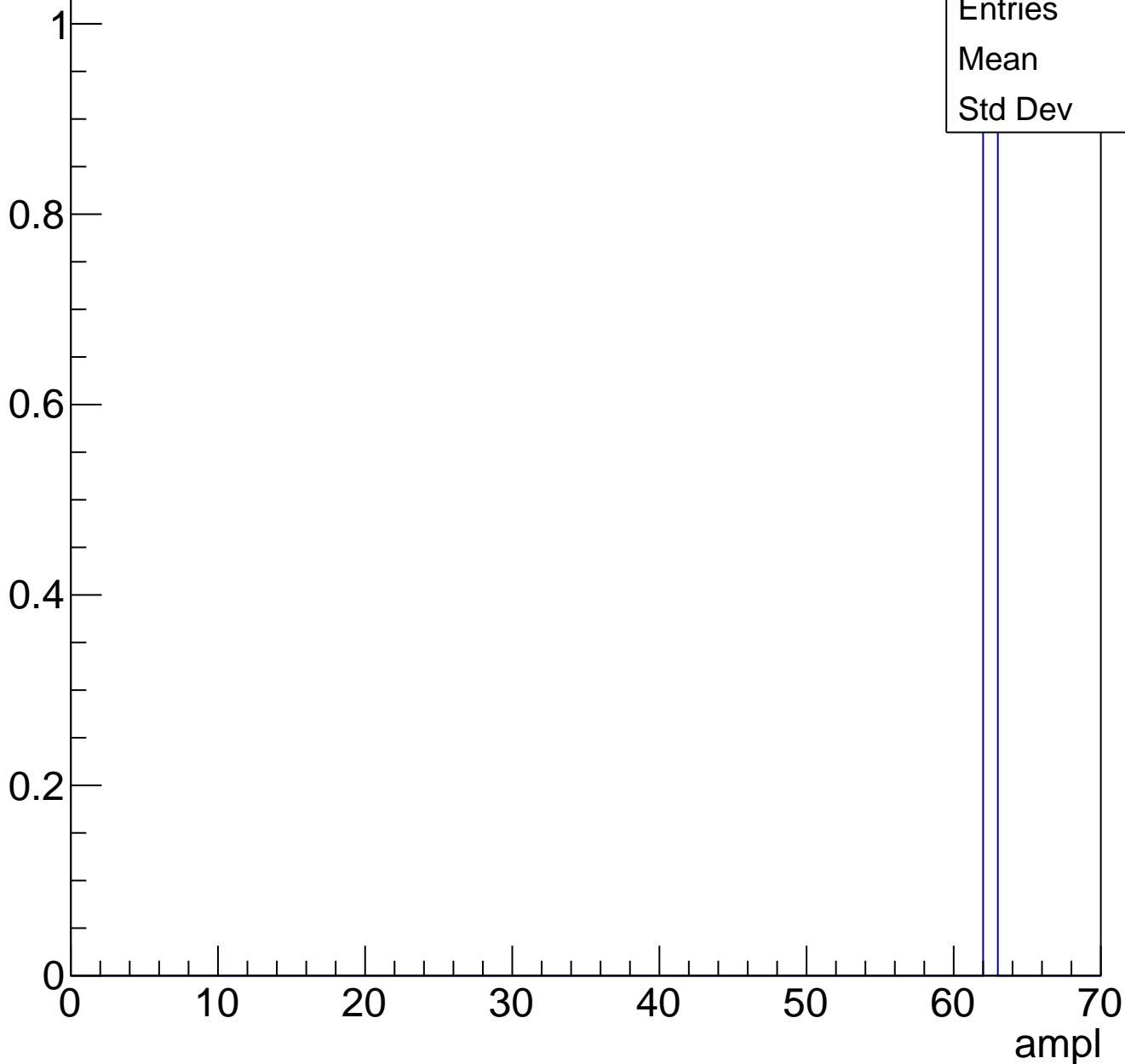
ampl



# B1L102S, U3-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch13, adc0

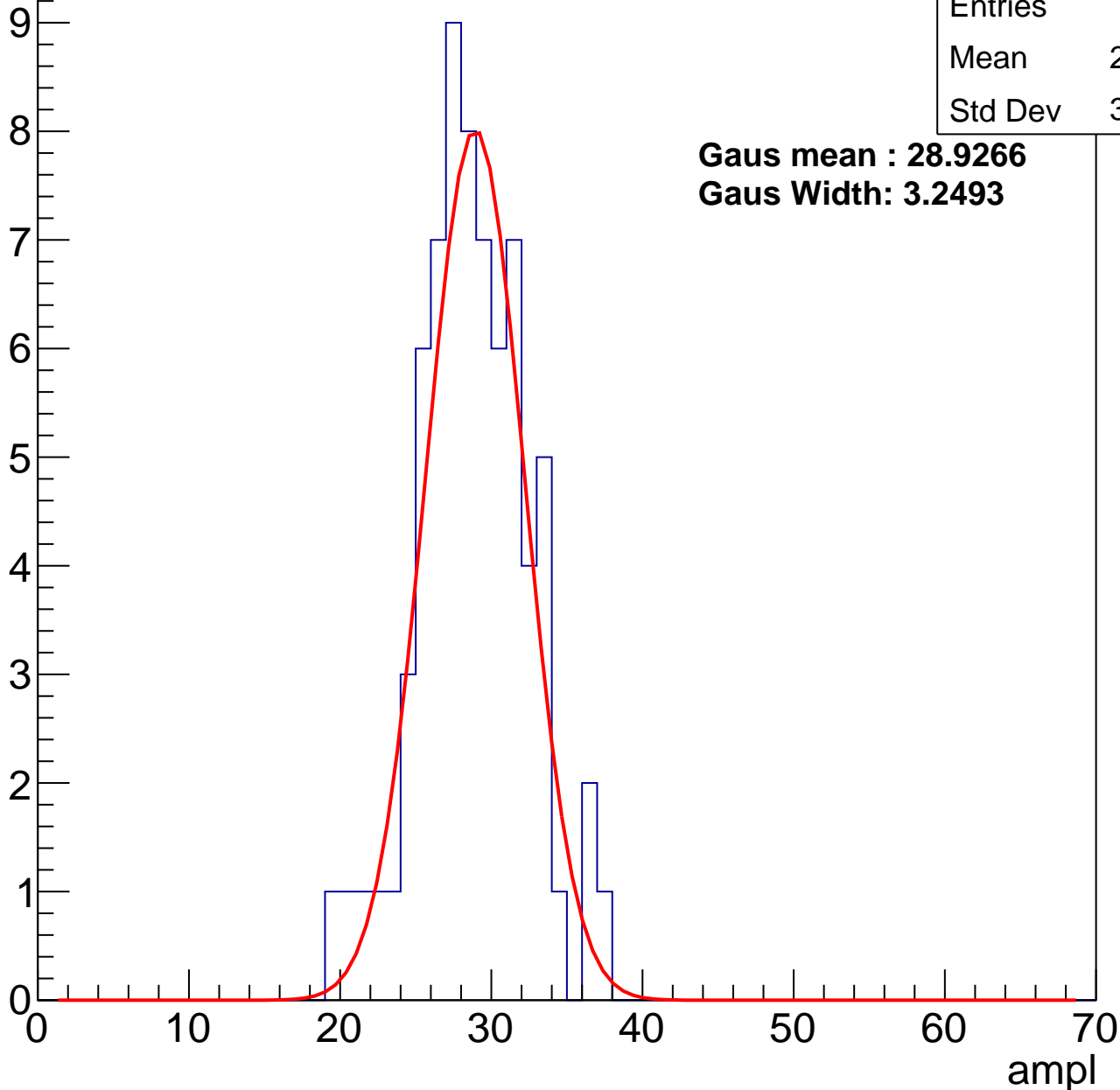
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	28.34
Std Dev	3.588

**Gaus mean : 28.9266**

**Gaus Width: 3.2493**



# B1L102S, U3-ch13, adc1

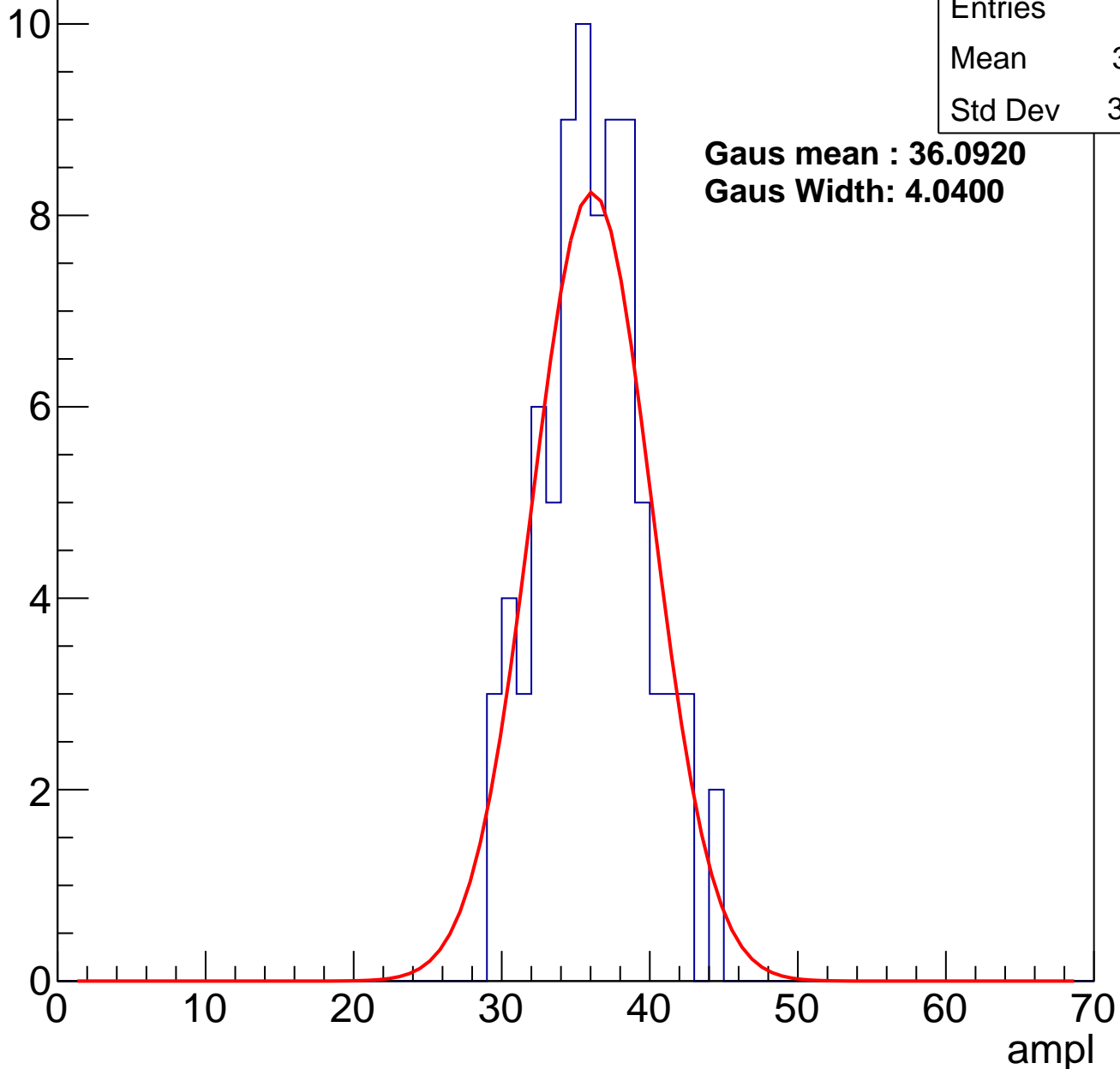
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	82
Mean	35.71
Std Dev	3.483

**Gaus mean : 36.0920**

**Gaus Width: 4.0400**

Entry



# B1L102S, U3-ch13, adc2

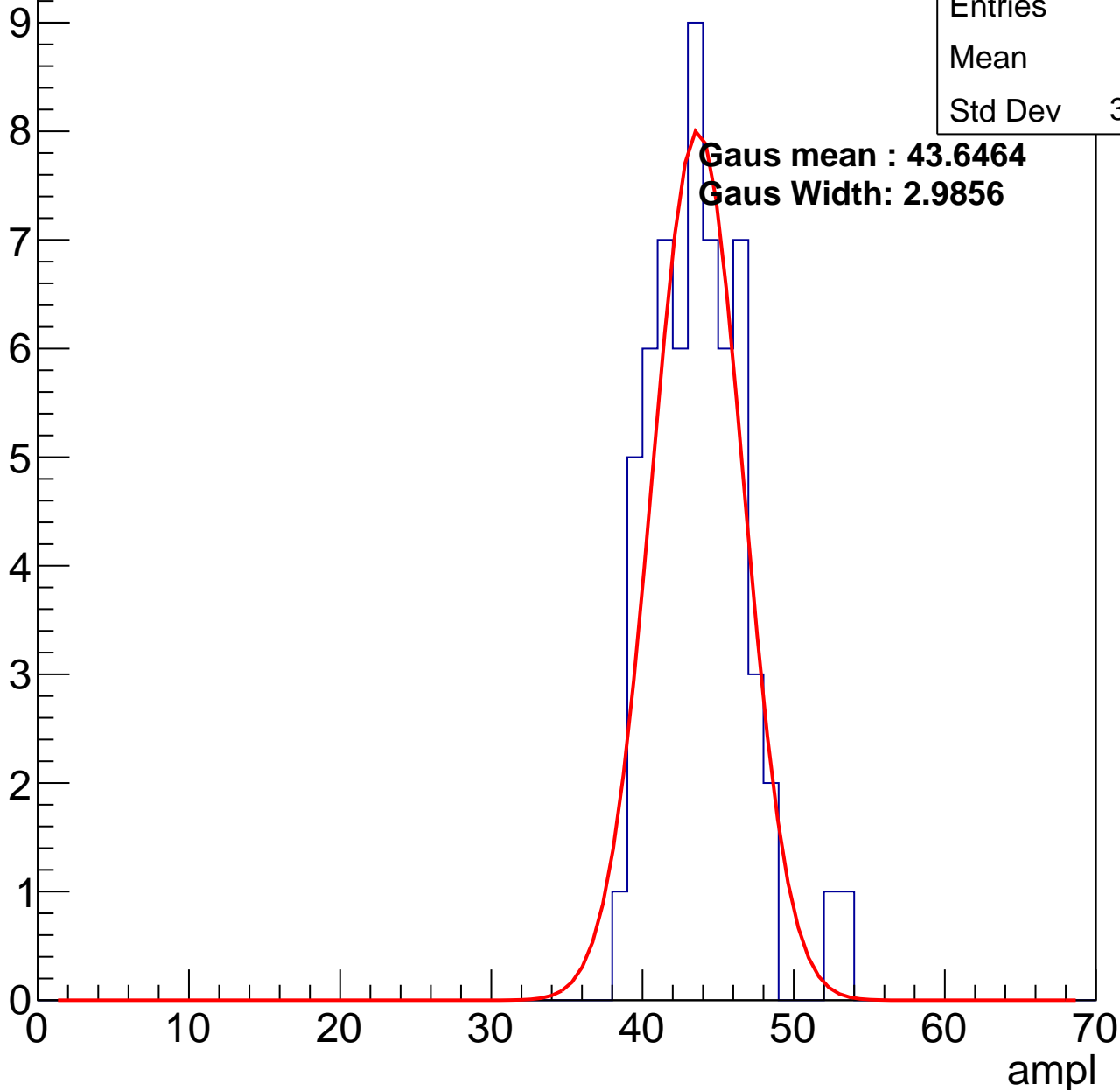
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	43.3
Std Dev	3.032

**Gaus mean : 43.6464**

**Gaus Width: 2.9856**

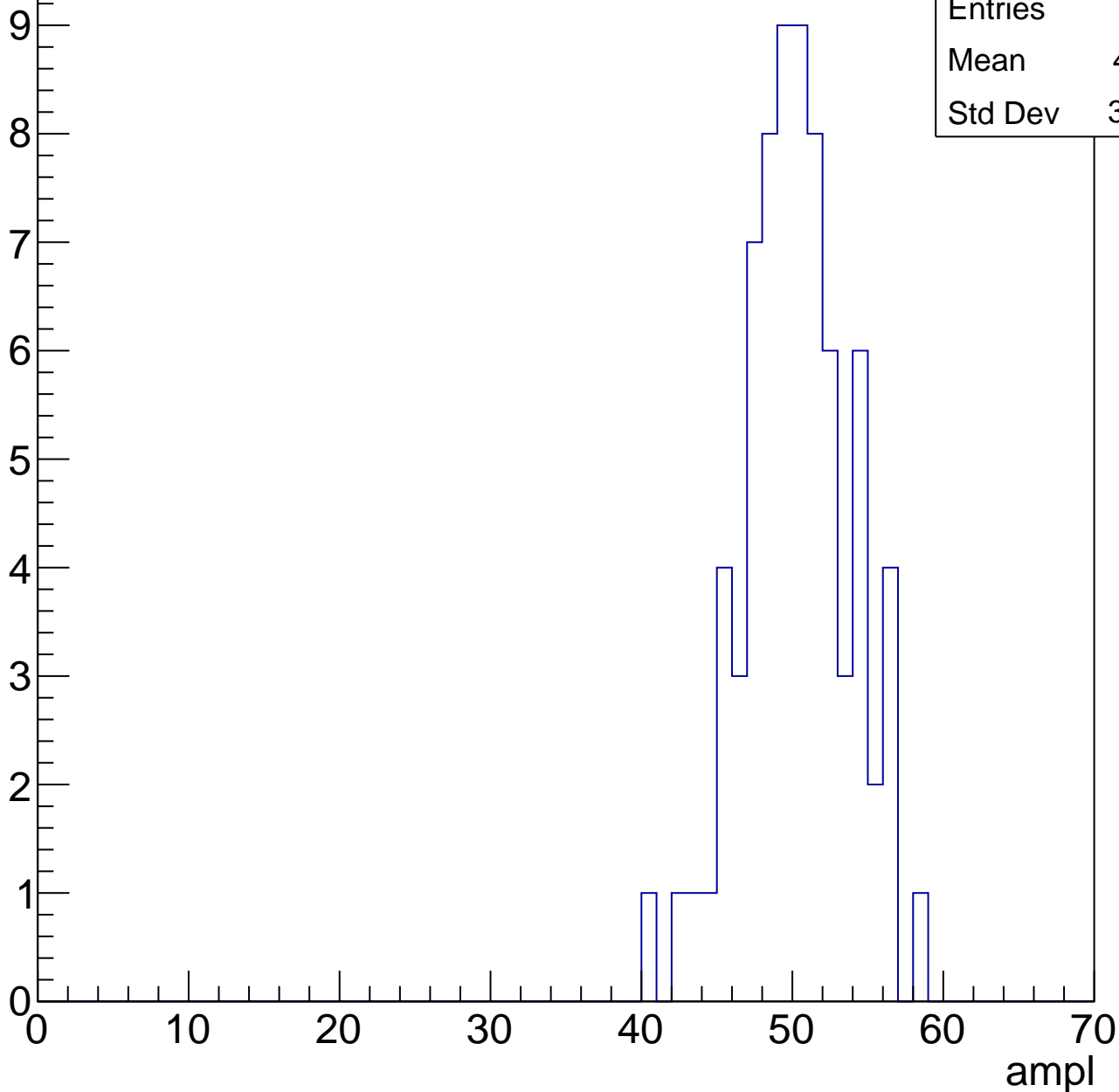


# B1L102S, U3-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	49.81
Std Dev	3.509



# B1L102S, U3-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

7

6

5

4

3

2

1

0

Entries 46

Mean 56.09

Std Dev 3.425

0

10

20

30

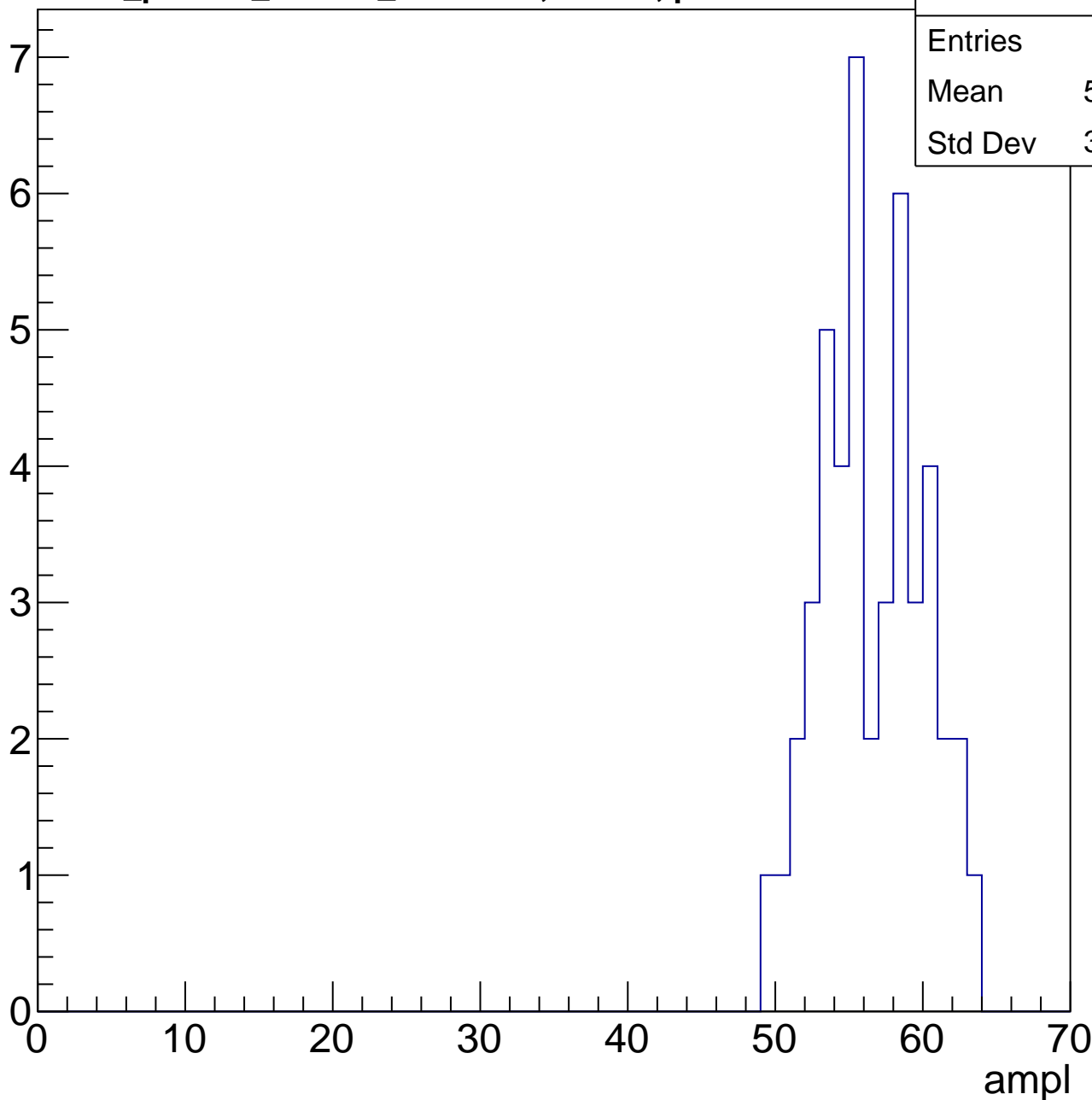
40

50

60

70

ampl

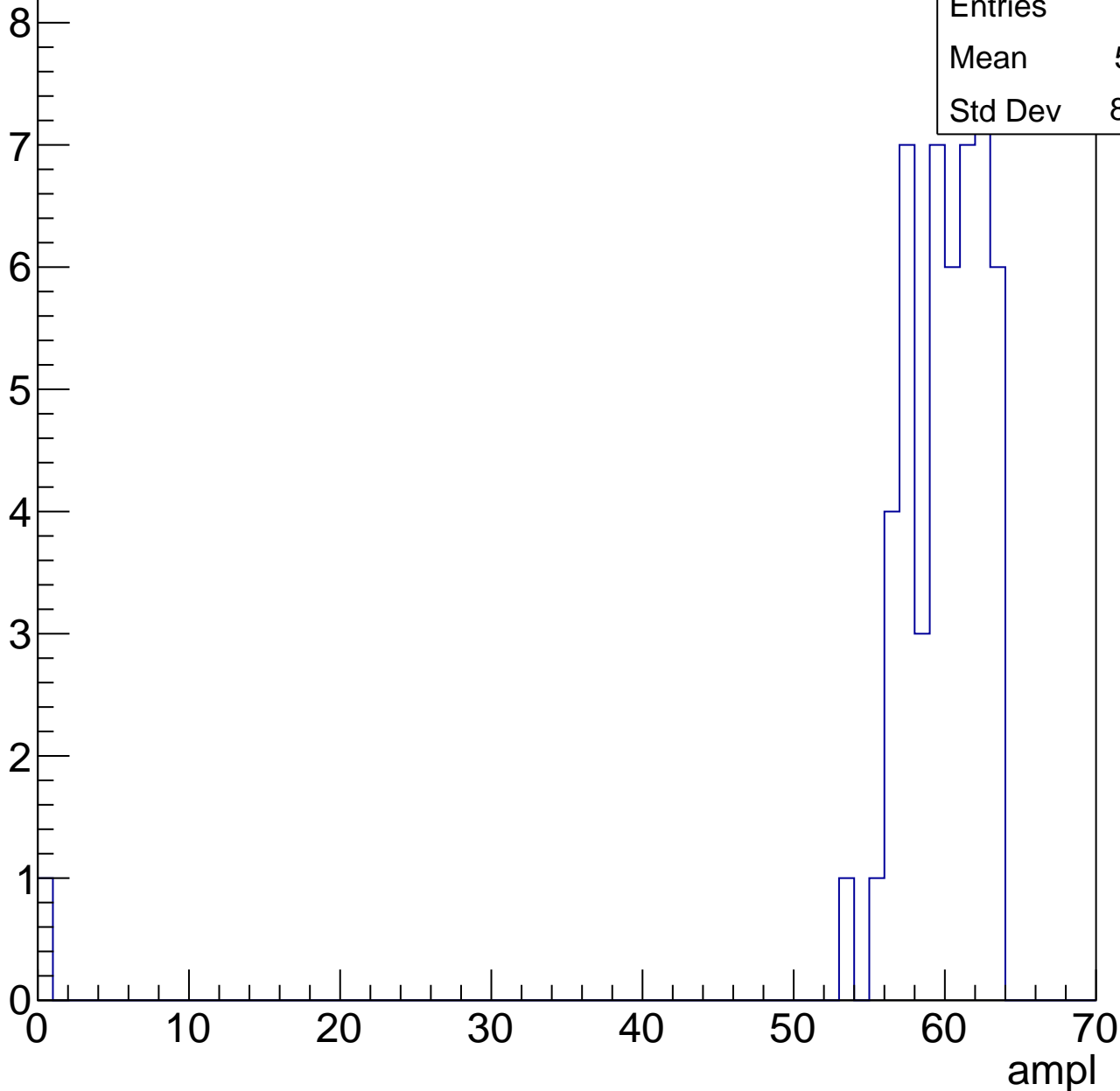


# B1L102S, U3-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	58.41
Std Dev	8.614



# B1L102S, U3-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch14, adc0

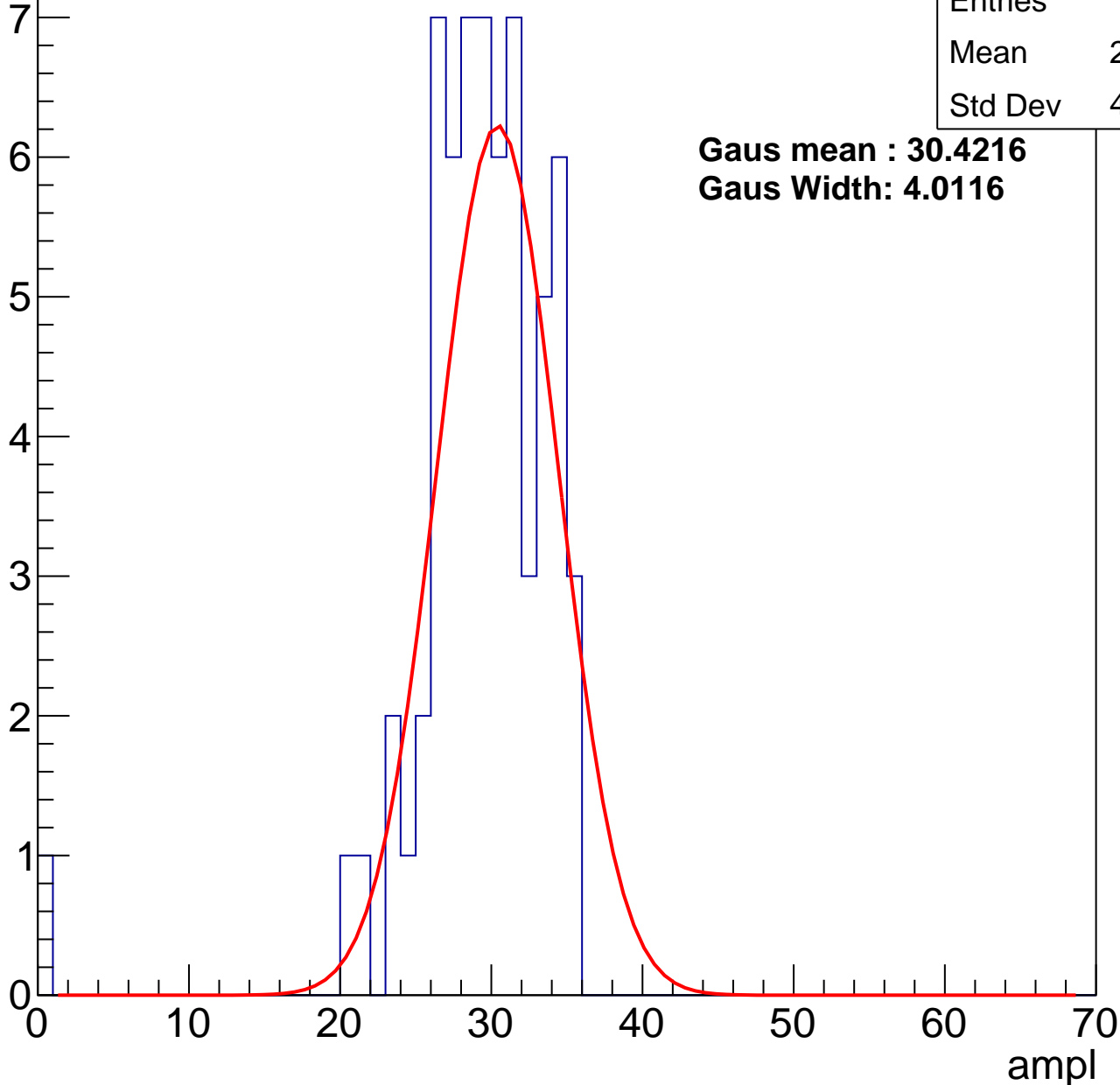
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	28.78
Std Dev	4.969

**Gaus mean : 30.4216**

**Gaus Width: 4.0116**



# B1L102S, U3-ch14, adc1

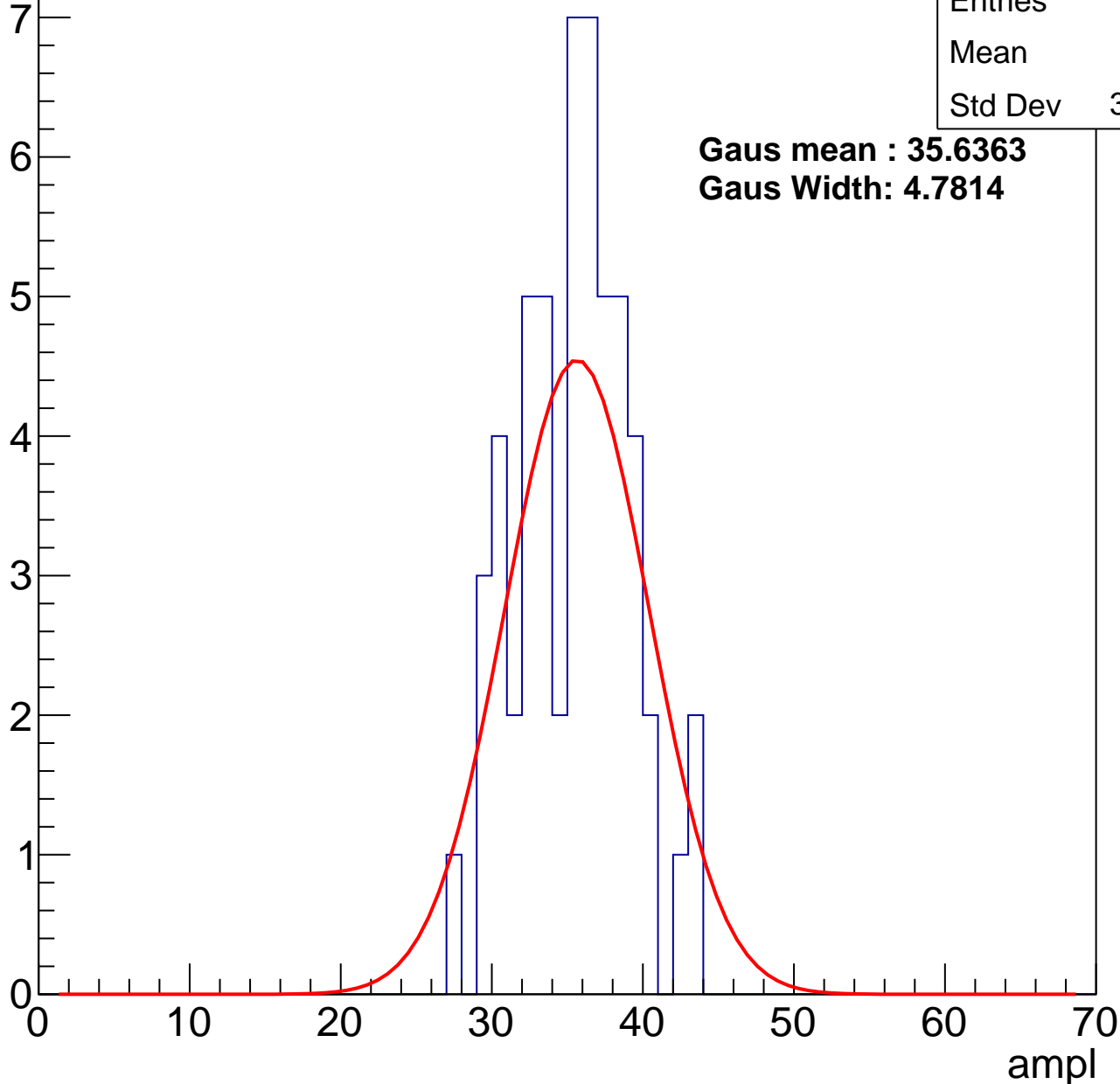
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	35
Std Dev	3.653

**Gaus mean : 35.6363**

**Gaus Width: 4.7814**



# B1L102S, U3-ch14, adc2

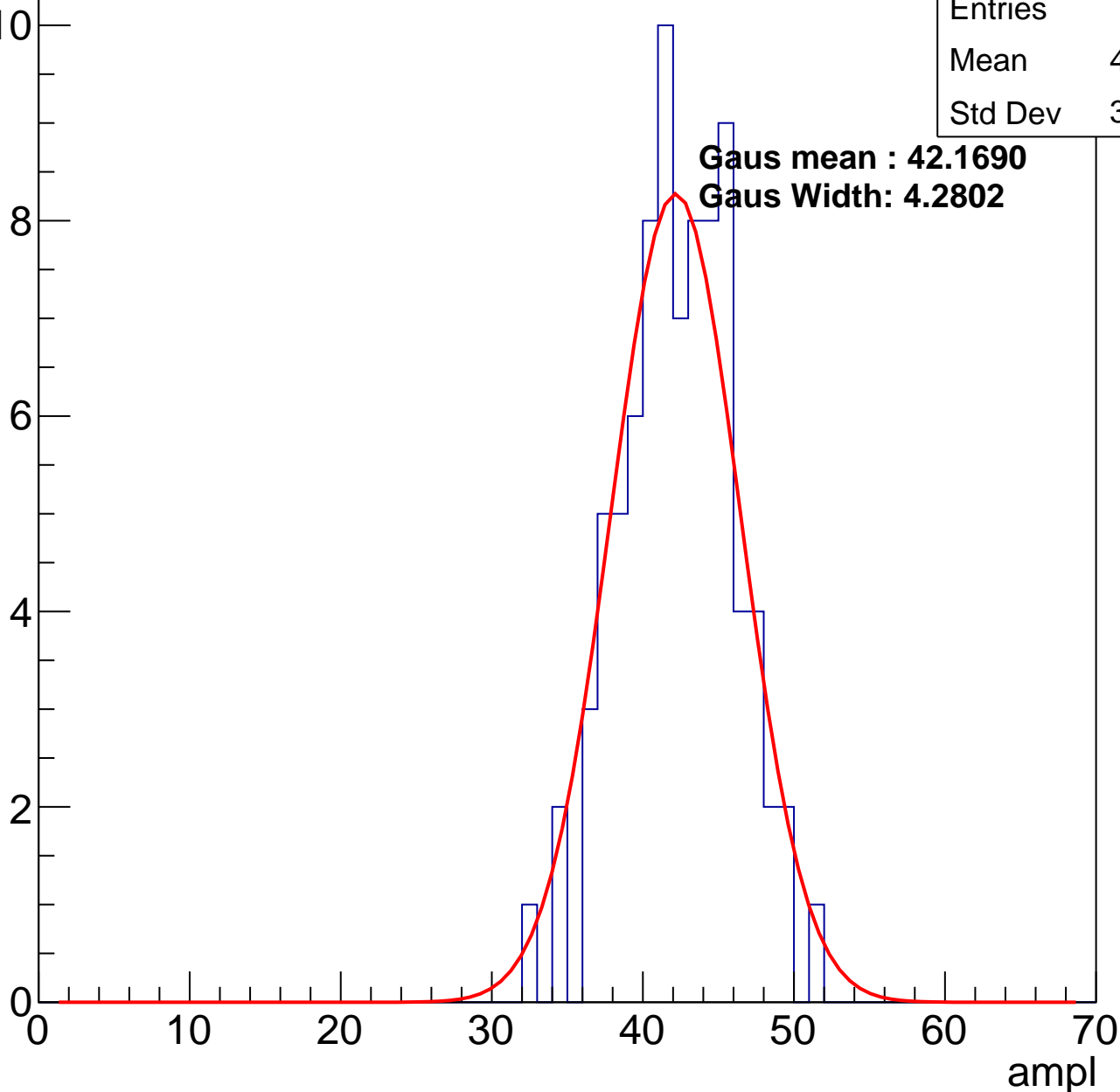
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	85
Mean	41.87
Std Dev	3.713

**Gaus mean : 42.1690**

**Gaus Width: 4.2802**

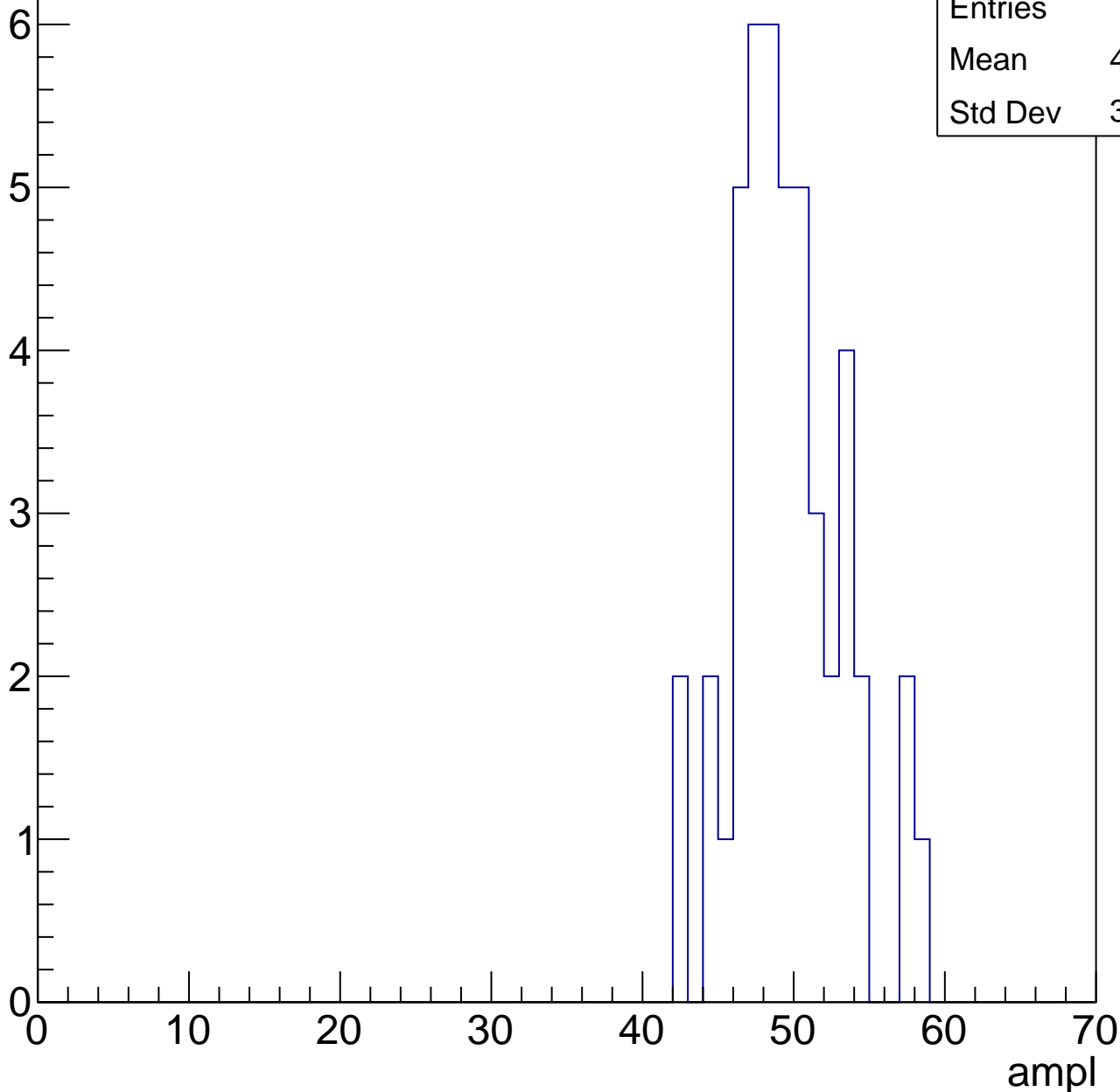


# B1L102S, U3-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	49.15
Std Dev	3.599

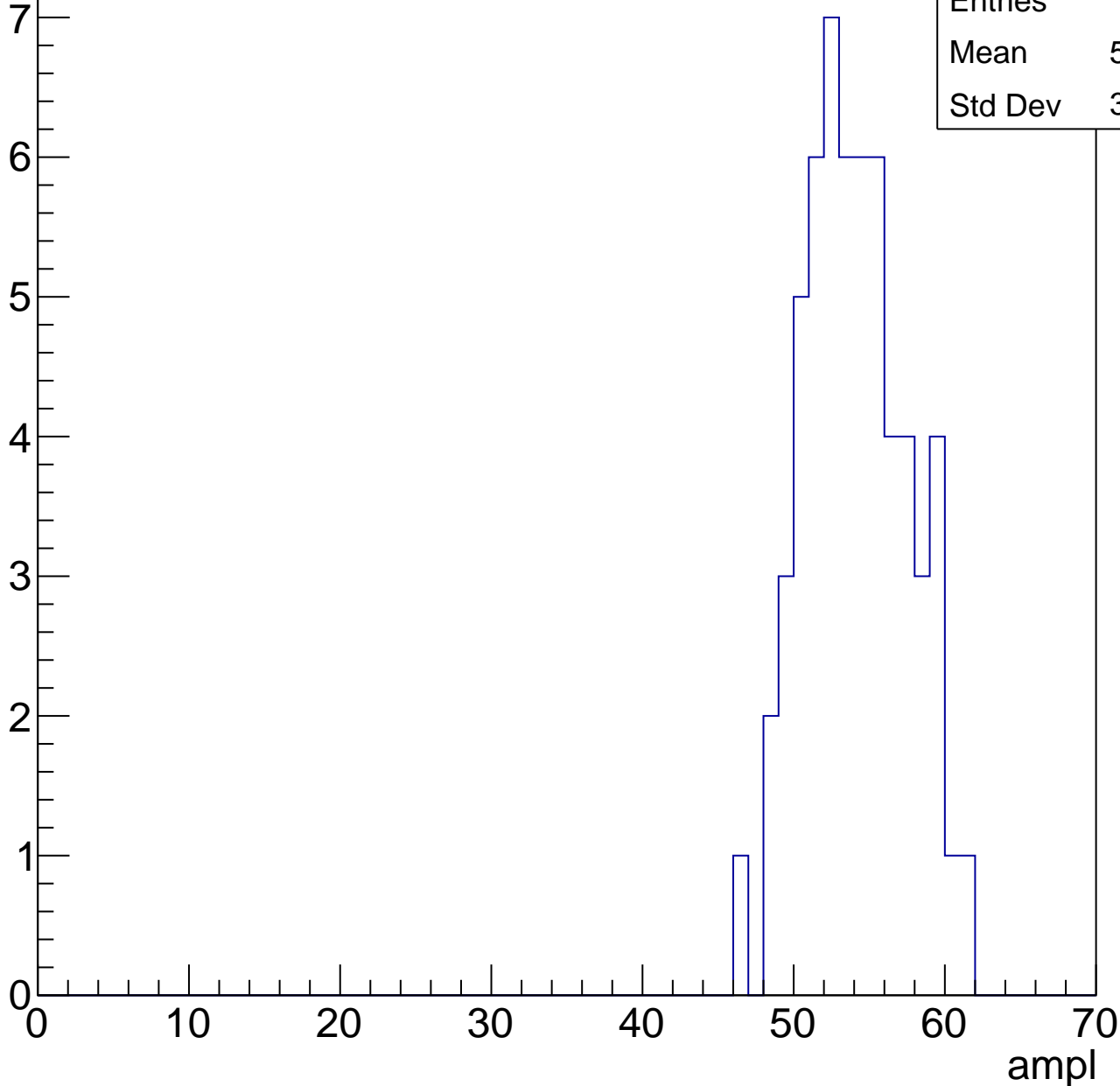


# B1L102S, U3-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	53.63
Std Dev	3.349

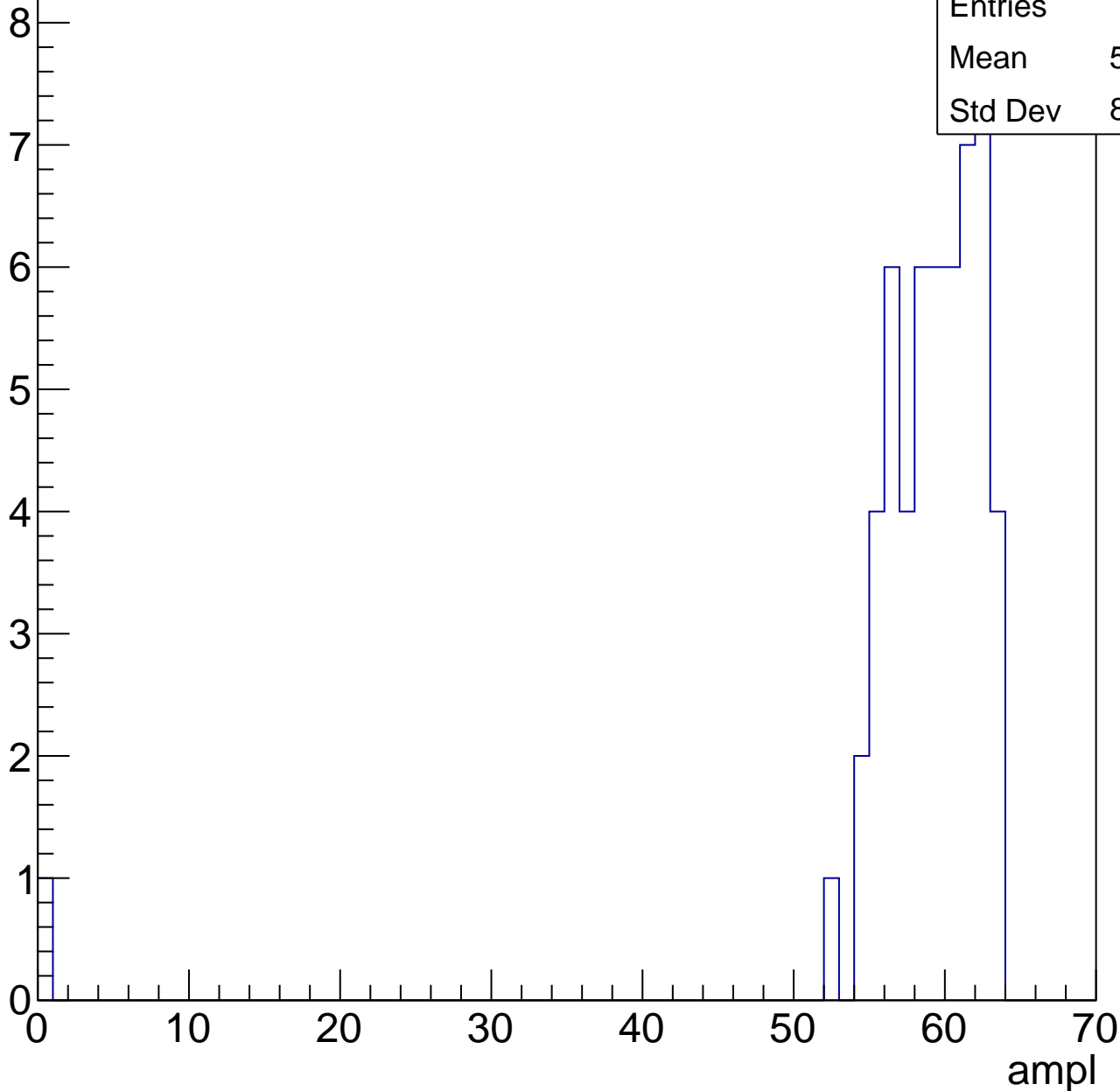


# B1L102S, U3-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

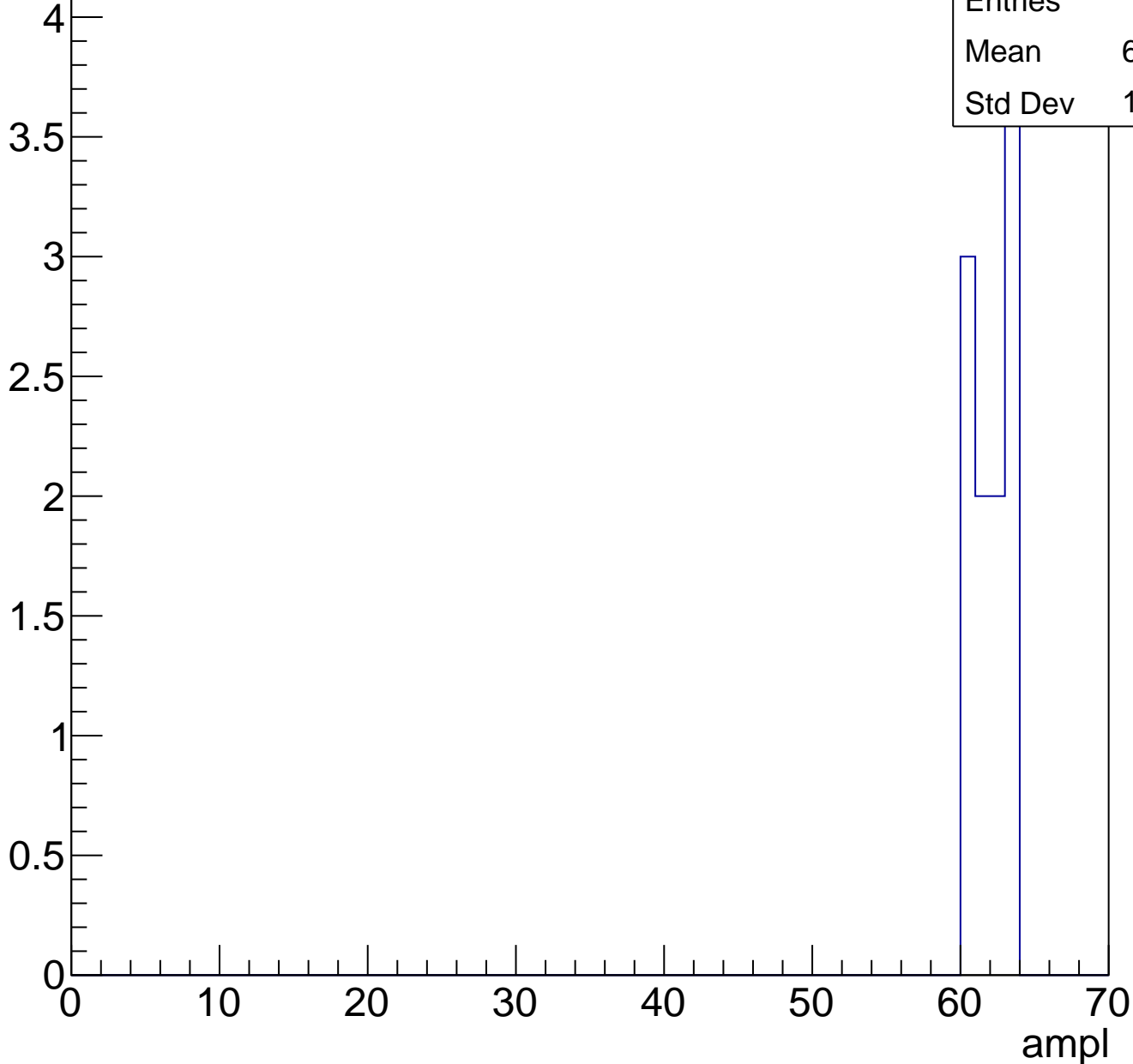
Entries	55
Mean	57.84
Std Dev	8.329



# B1L102S, U3-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch15, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	80
Mean	26.8
Std Dev	6.384

**Gaus mean : 28.1198**

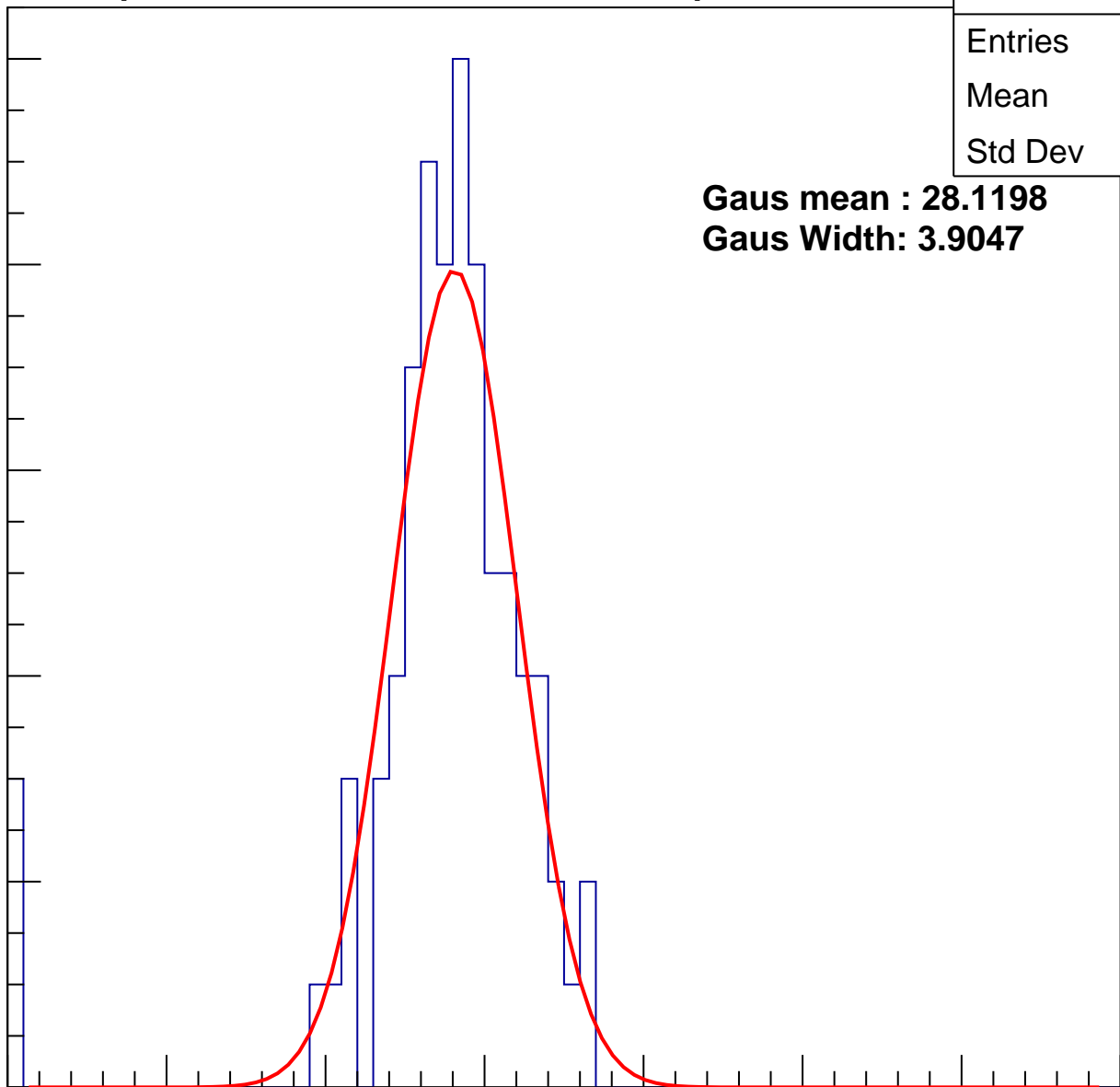
**Gaus Width: 3.9047**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U3-ch15, adc1

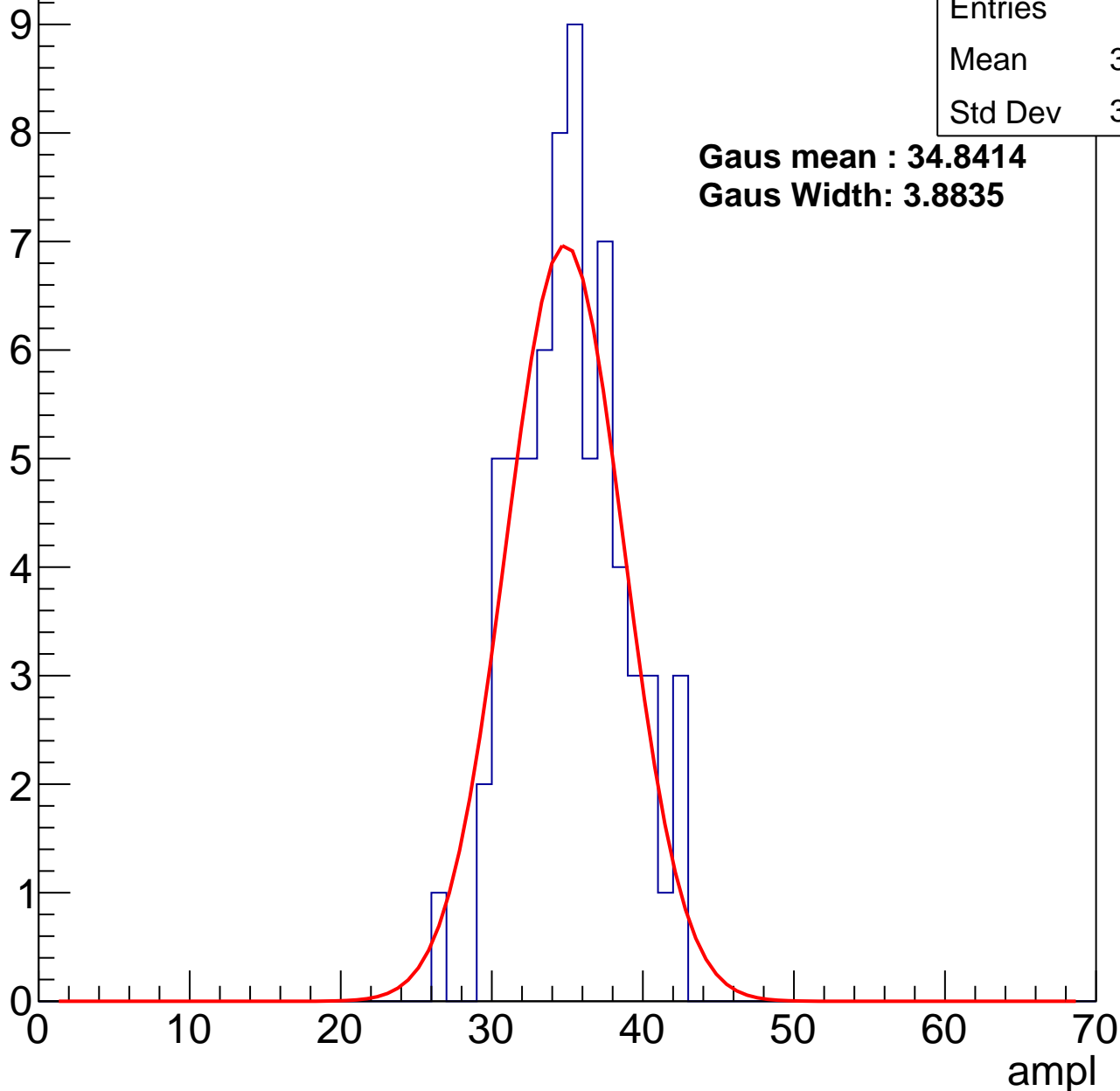
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	34.76
Std Dev	3.469

**Gaus mean : 34.8414**

**Gaus Width: 3.8835**



# B1L102S, U3-ch15, adc2

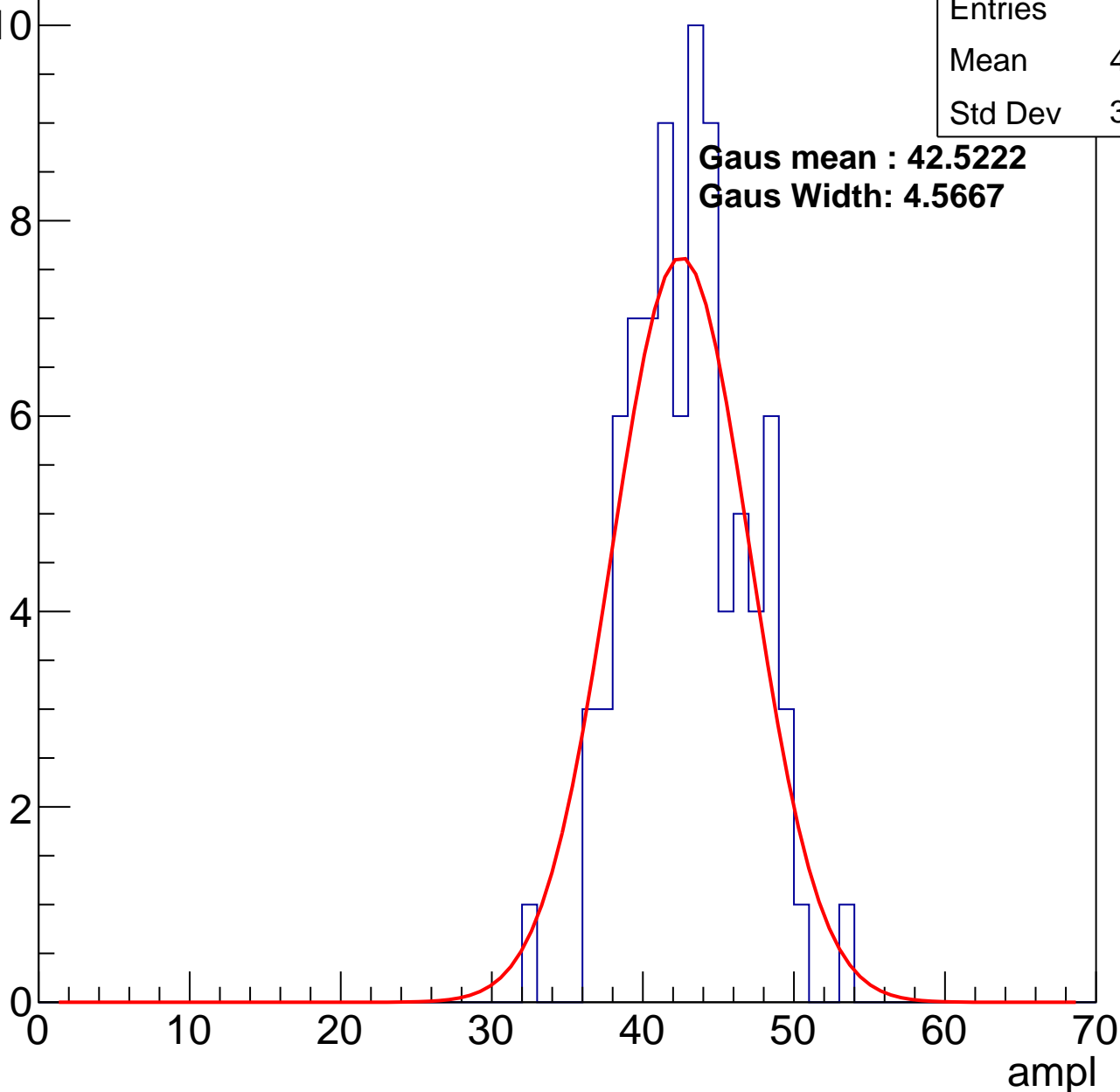
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	85
Mean	42.53
Std Dev	3.858

**Gaus mean : 42.5222**

**Gaus Width: 4.5667**

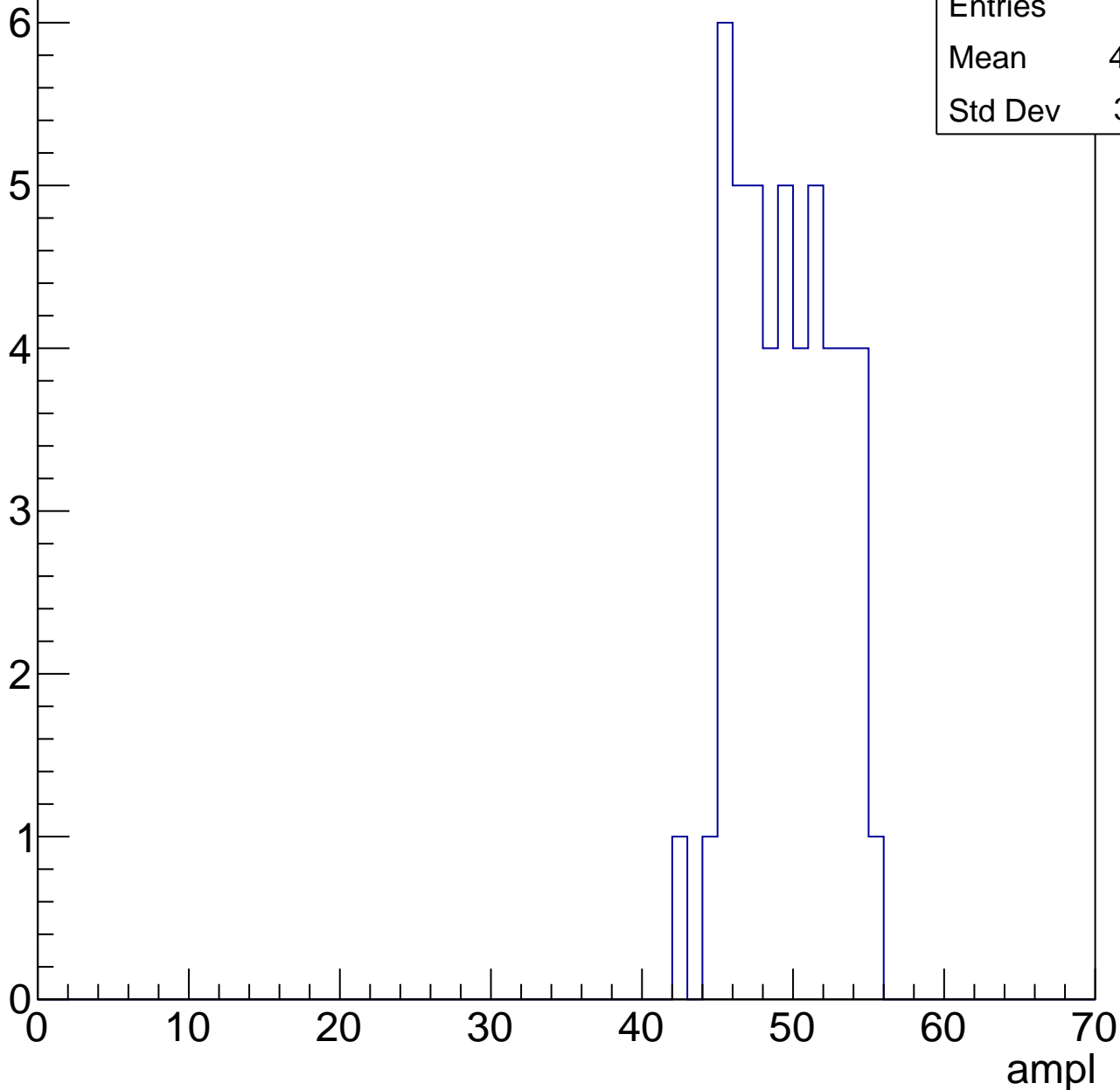


# B1L102S, U3-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	49.06
Std Dev	3.191

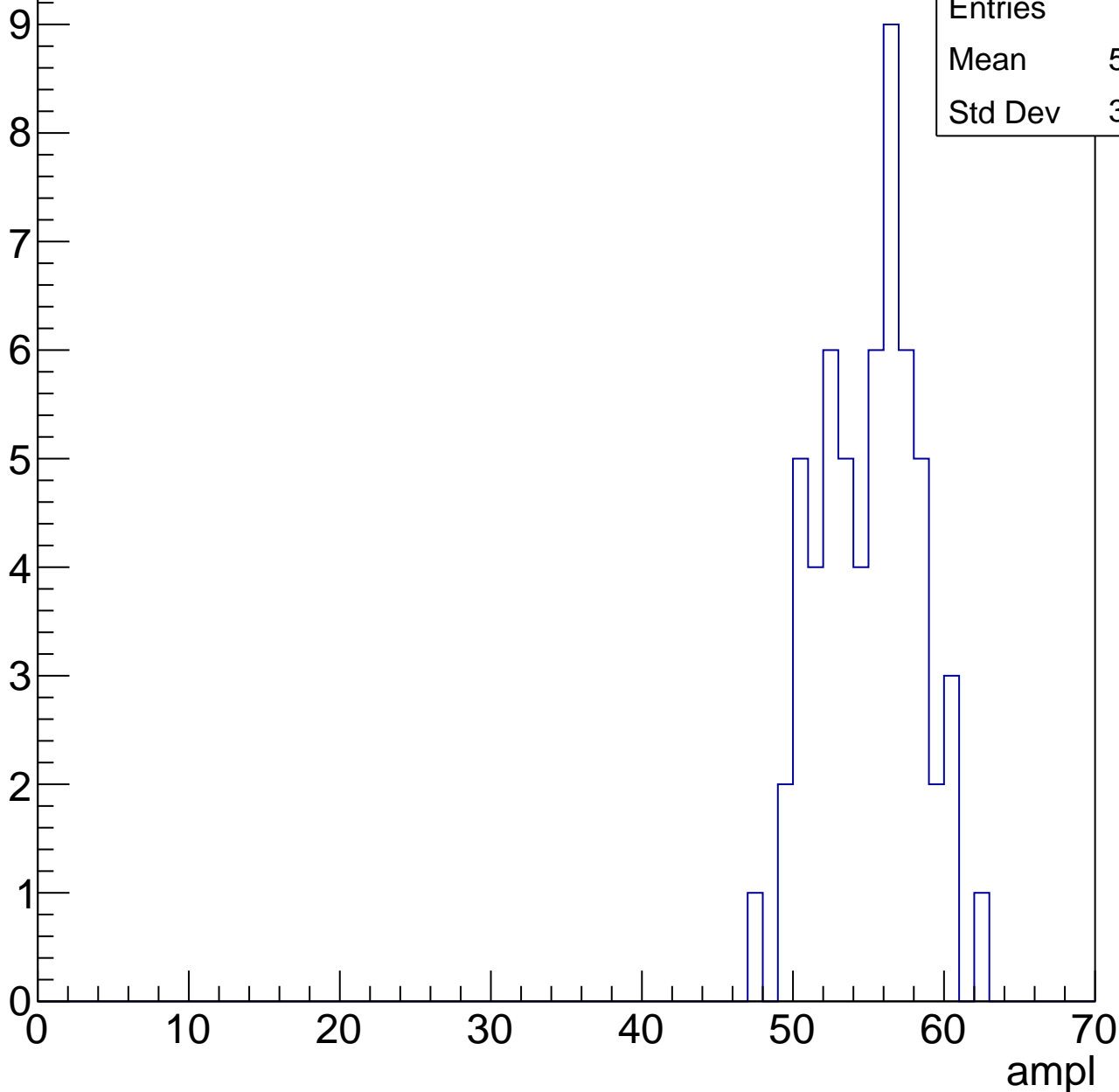


# B1L102S, U3-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	54.54
Std Dev	3.254

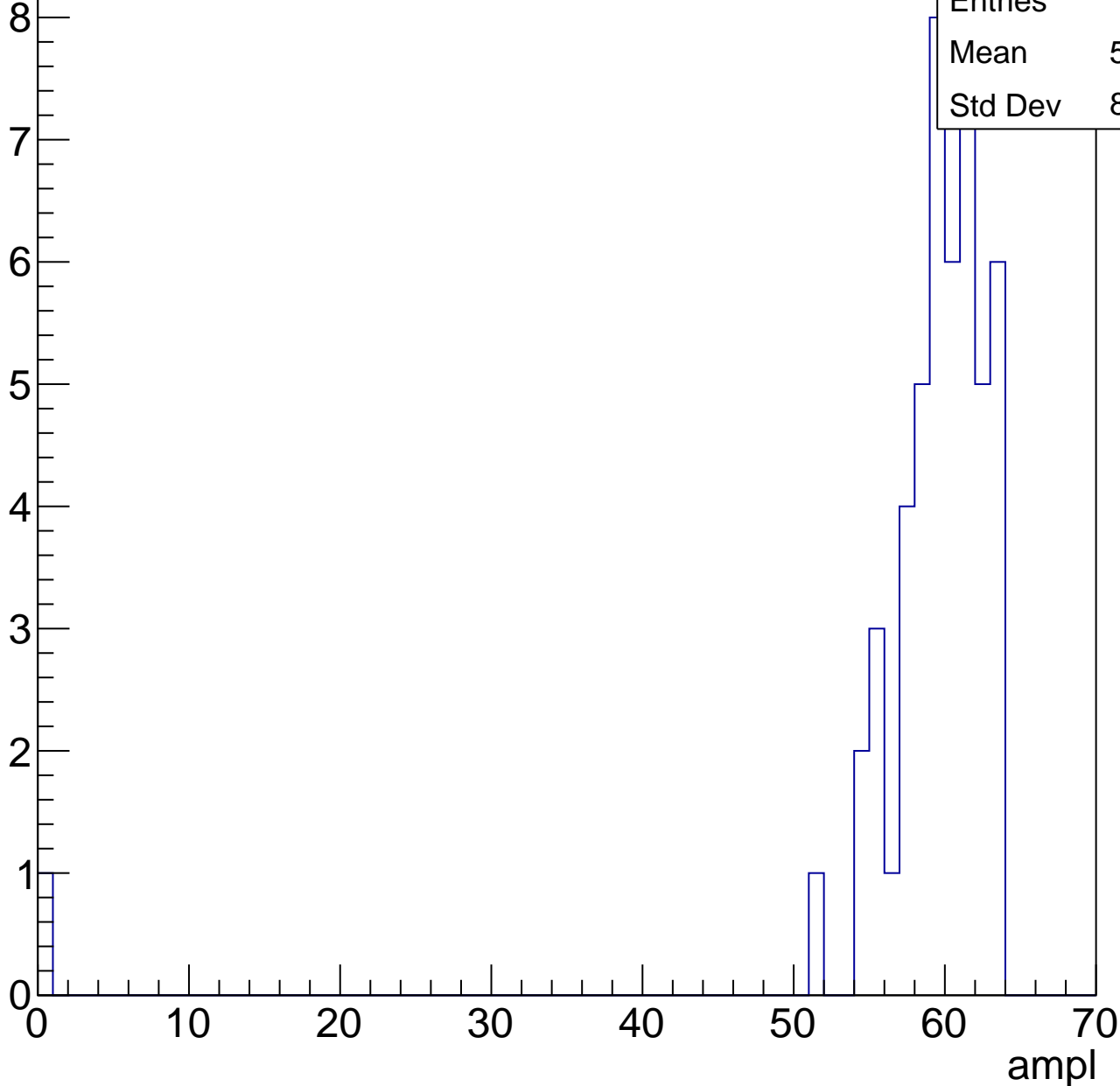


# B1L102S, U3-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

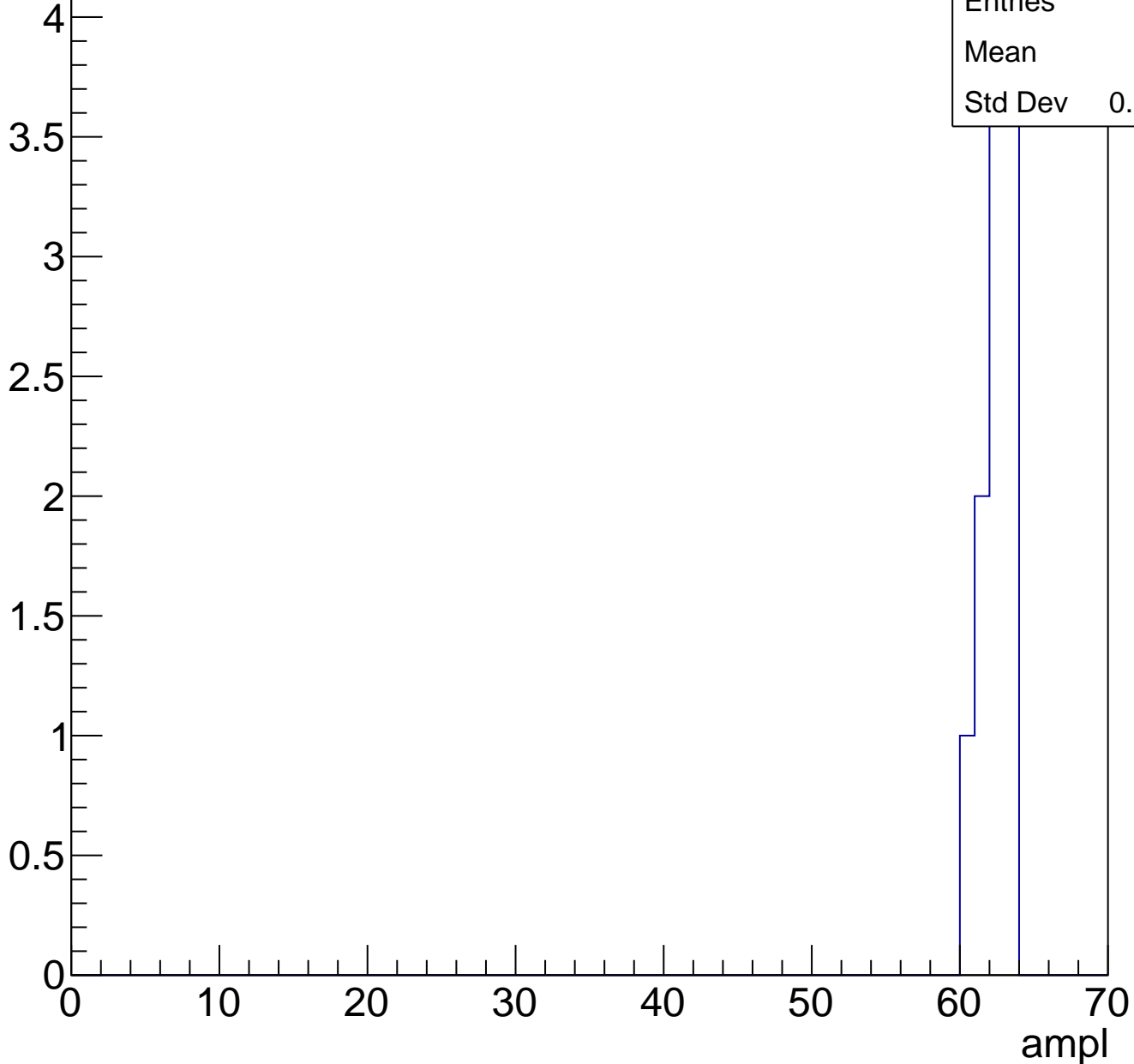
Entries	50
Mean	58.12
Std Dev	8.733



# B1L102S, U3-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	16
Std Dev	0

ampl

# B1L102S, U3-ch16, adc0

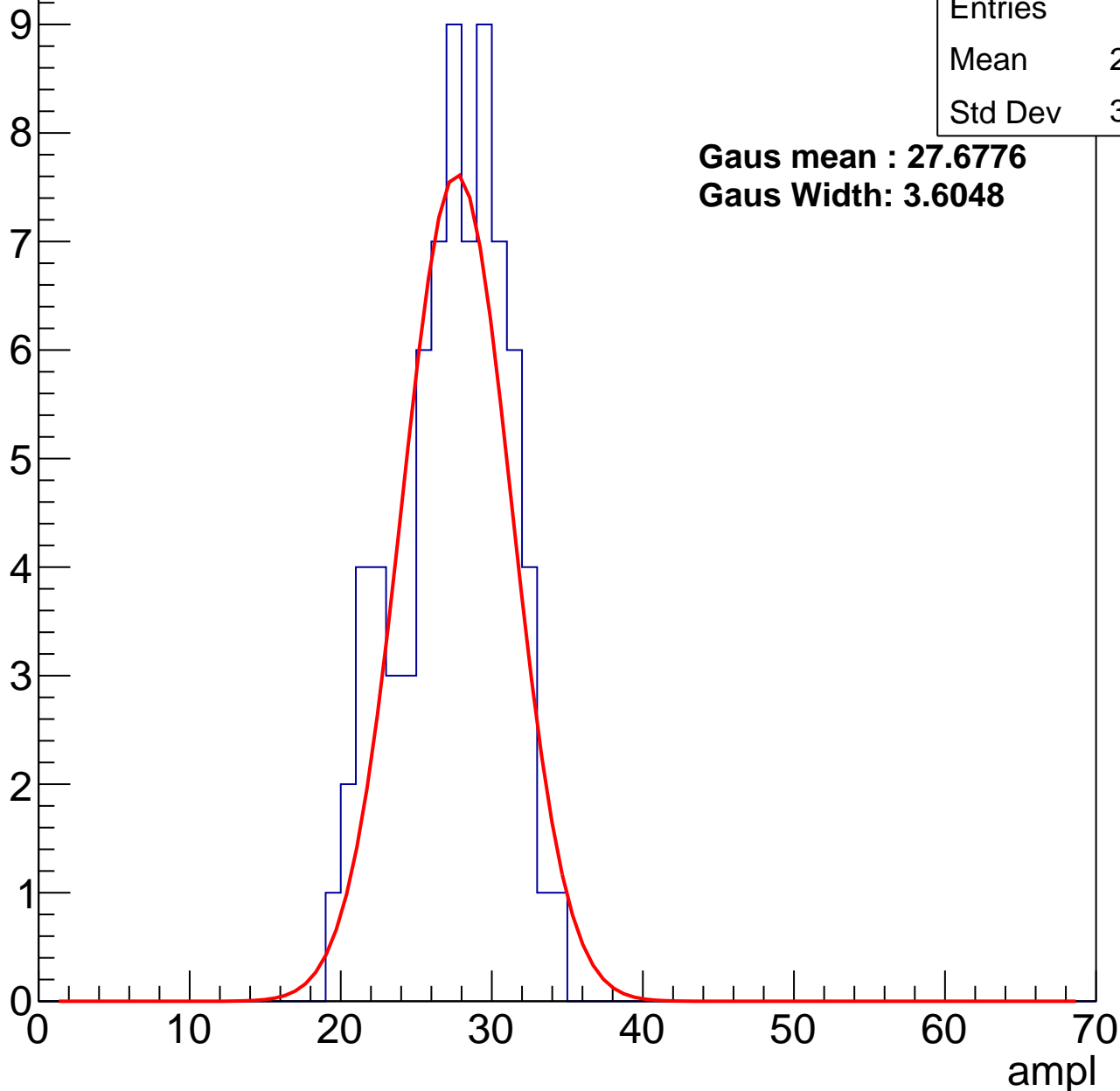
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	26.96
Std Dev	3.485

**Gaus mean : 27.6776**

**Gaus Width: 3.6048**



# B1L102S, U3-ch16, adc1

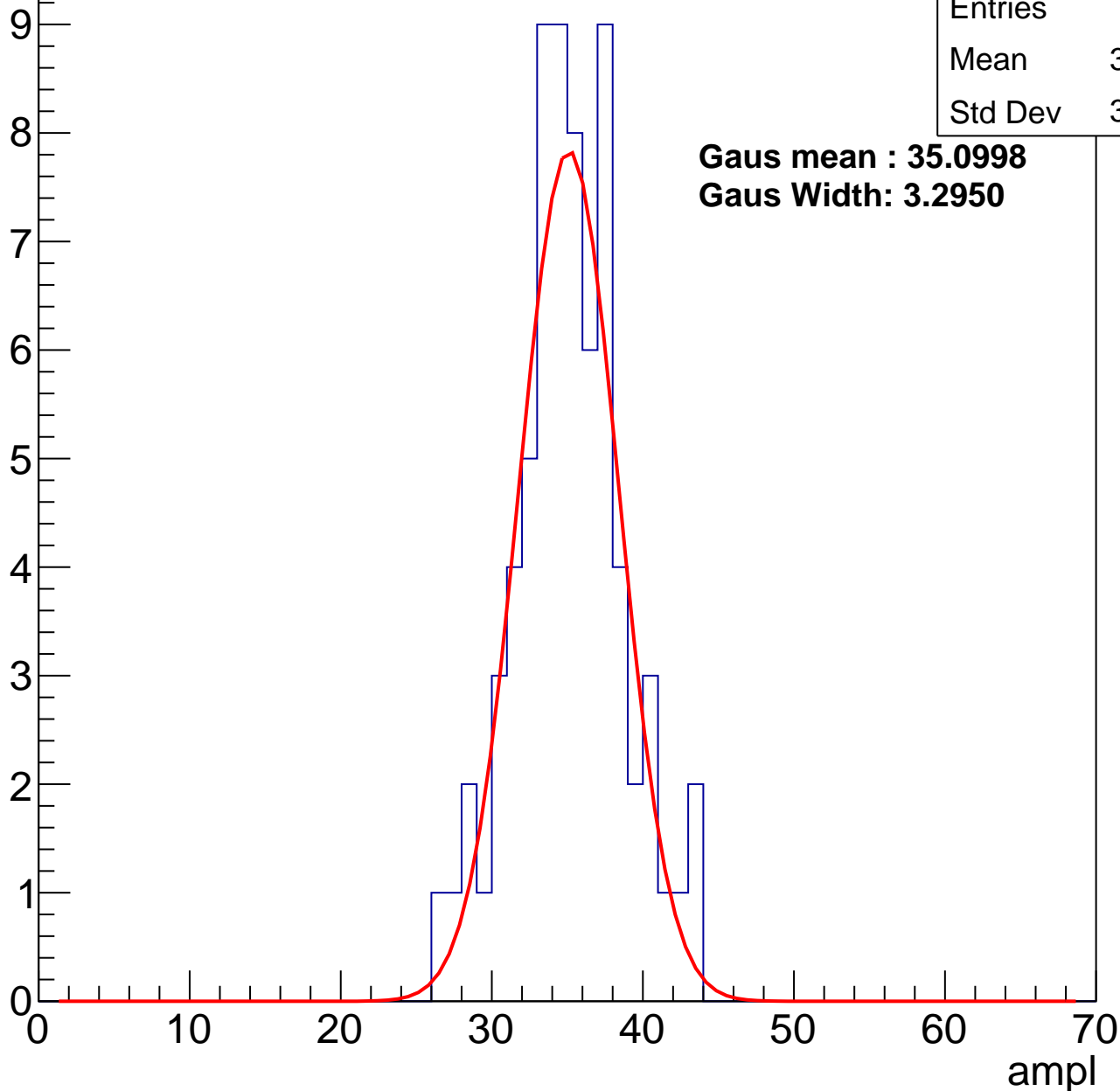
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	34.69
Std Dev	3.559

**Gaus mean : 35.0998**

**Gaus Width: 3.2950**



# B1L102S, U3-ch16, adc2

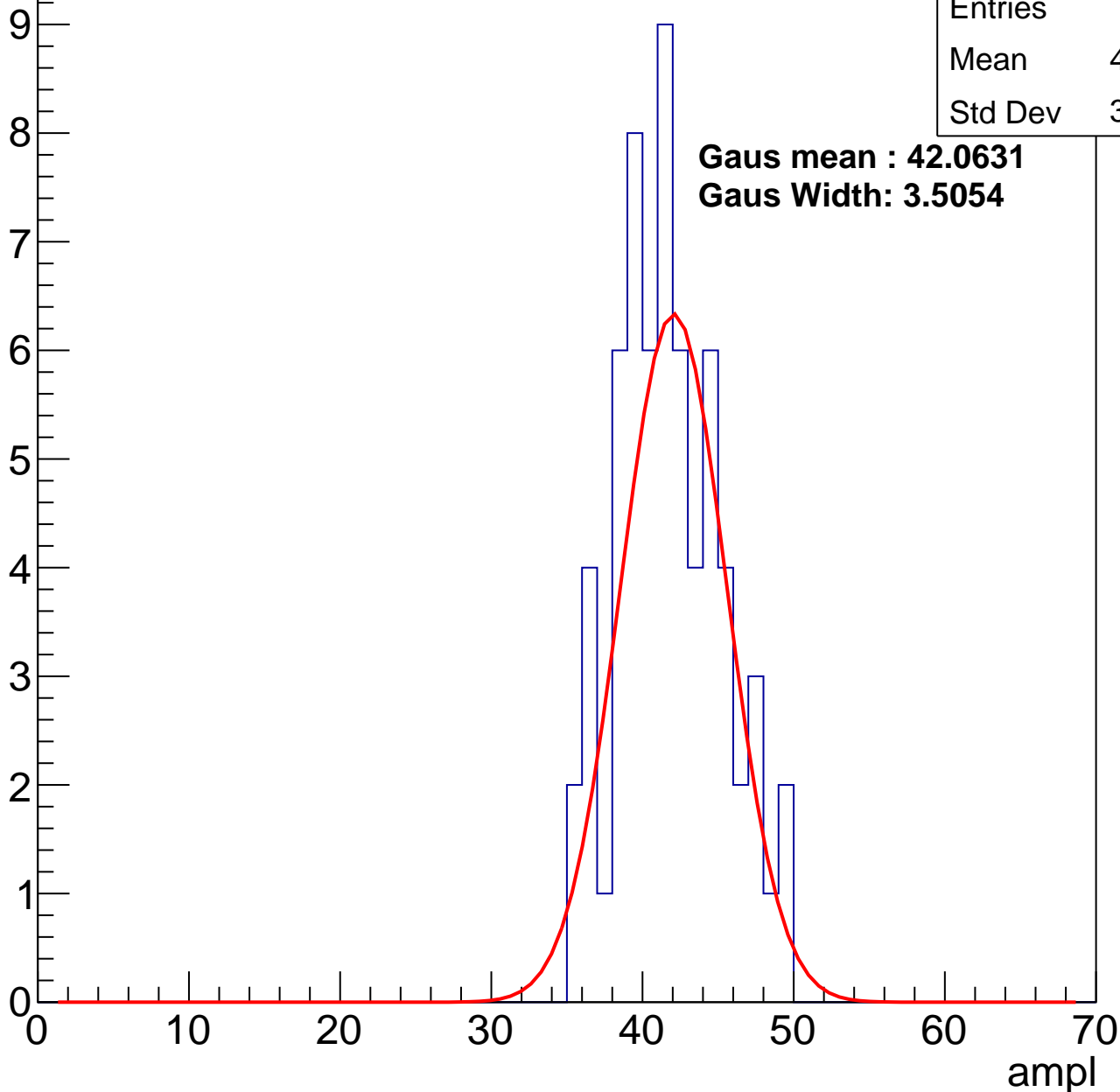
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	41.36
Std Dev	3.416

**Gaus mean : 42.0631**

**Gaus Width: 3.5054**

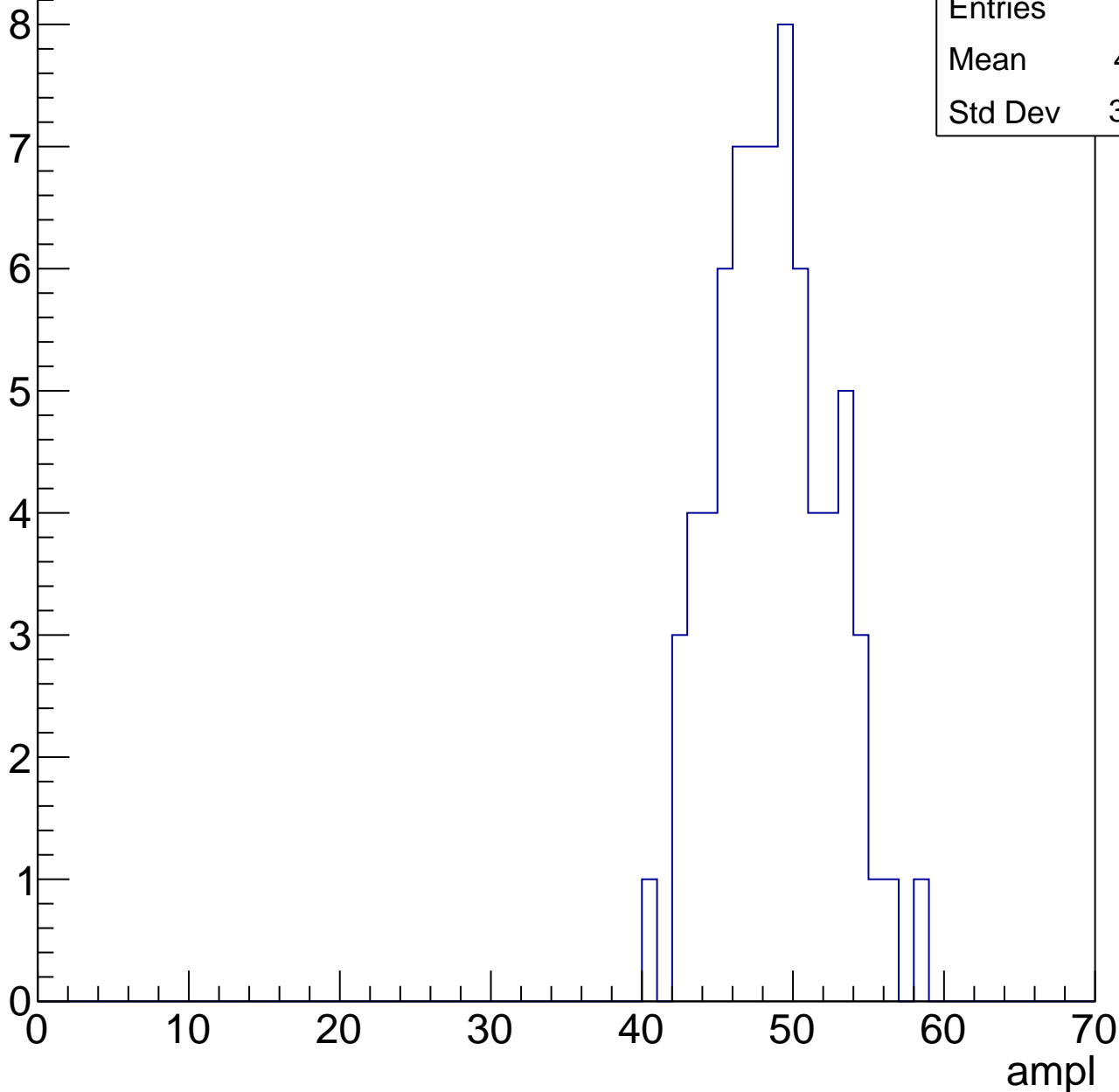


# B1L102S, U3-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	48.21
Std Dev	3.727

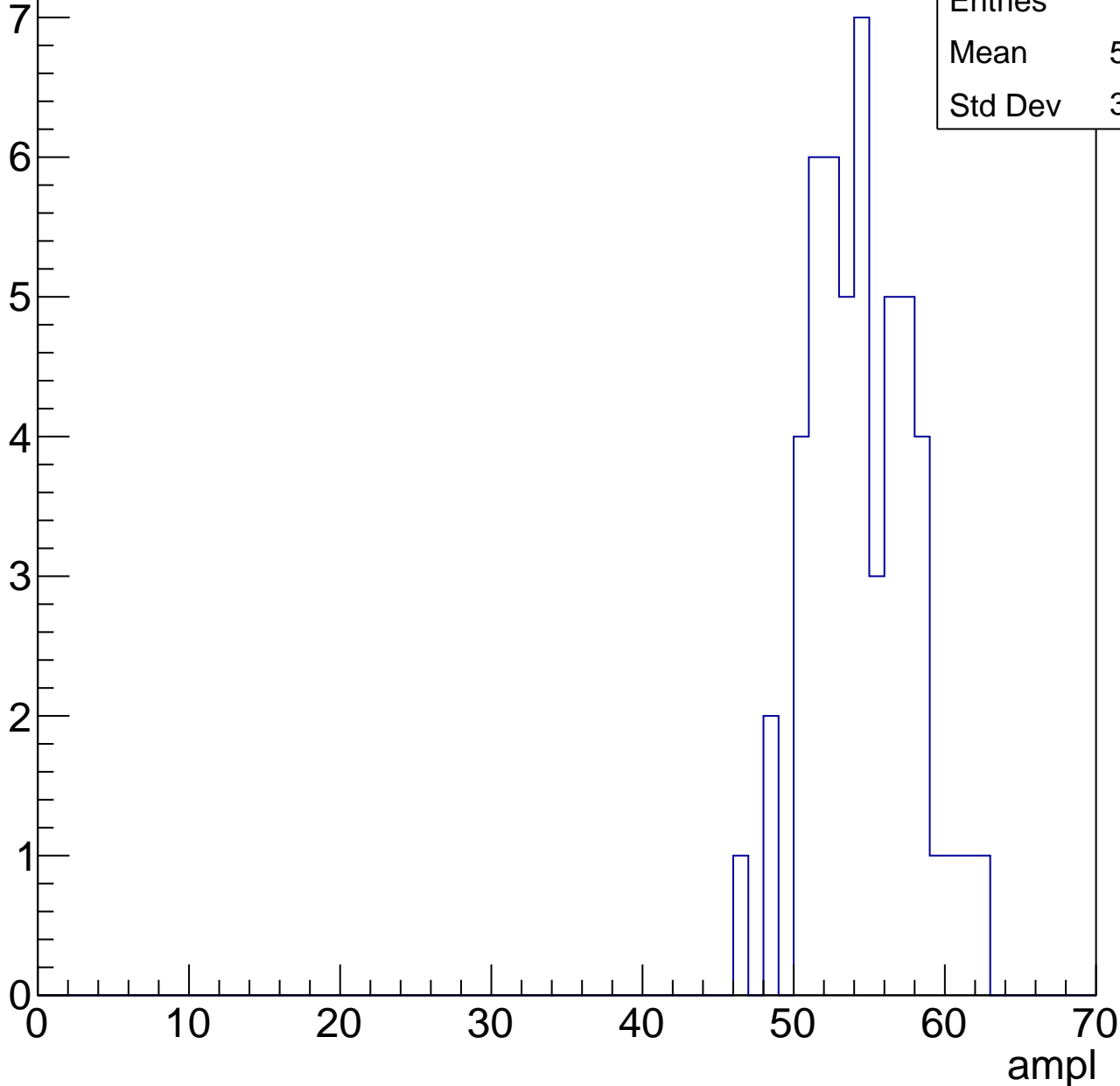


# B1L102S, U3-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	53.98
Std Dev	3.365



# B1L102S, U3-ch16, adc5

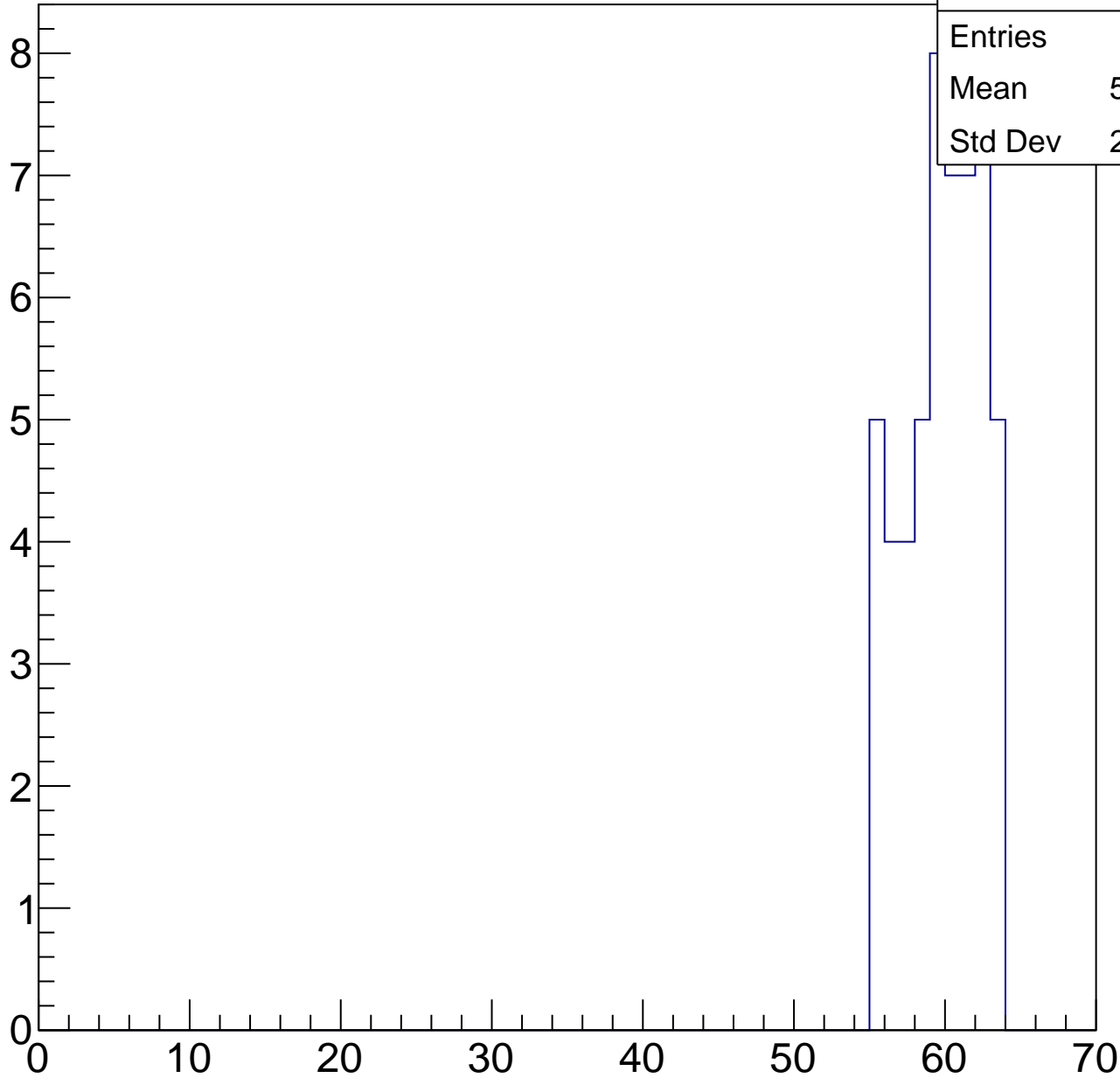
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	53
Mean	59.38
Std Dev	2.444

ampl

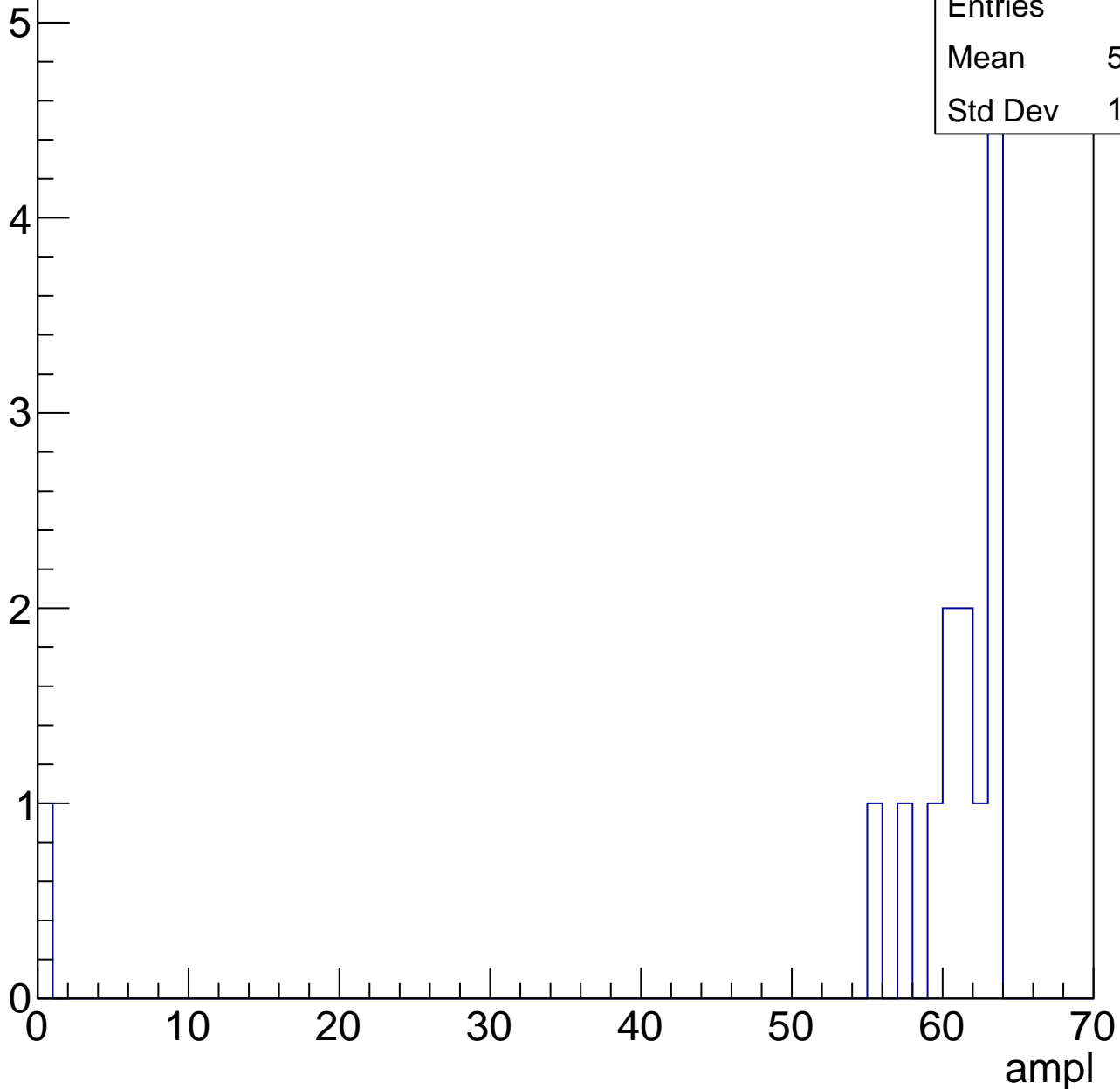


# B1L102S, U3-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	14
Mean	56.43
Std Dev	15.83





# B1L102S, U3-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L102S, U3-ch17, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	79
Mean	29.13
Std Dev	3.963

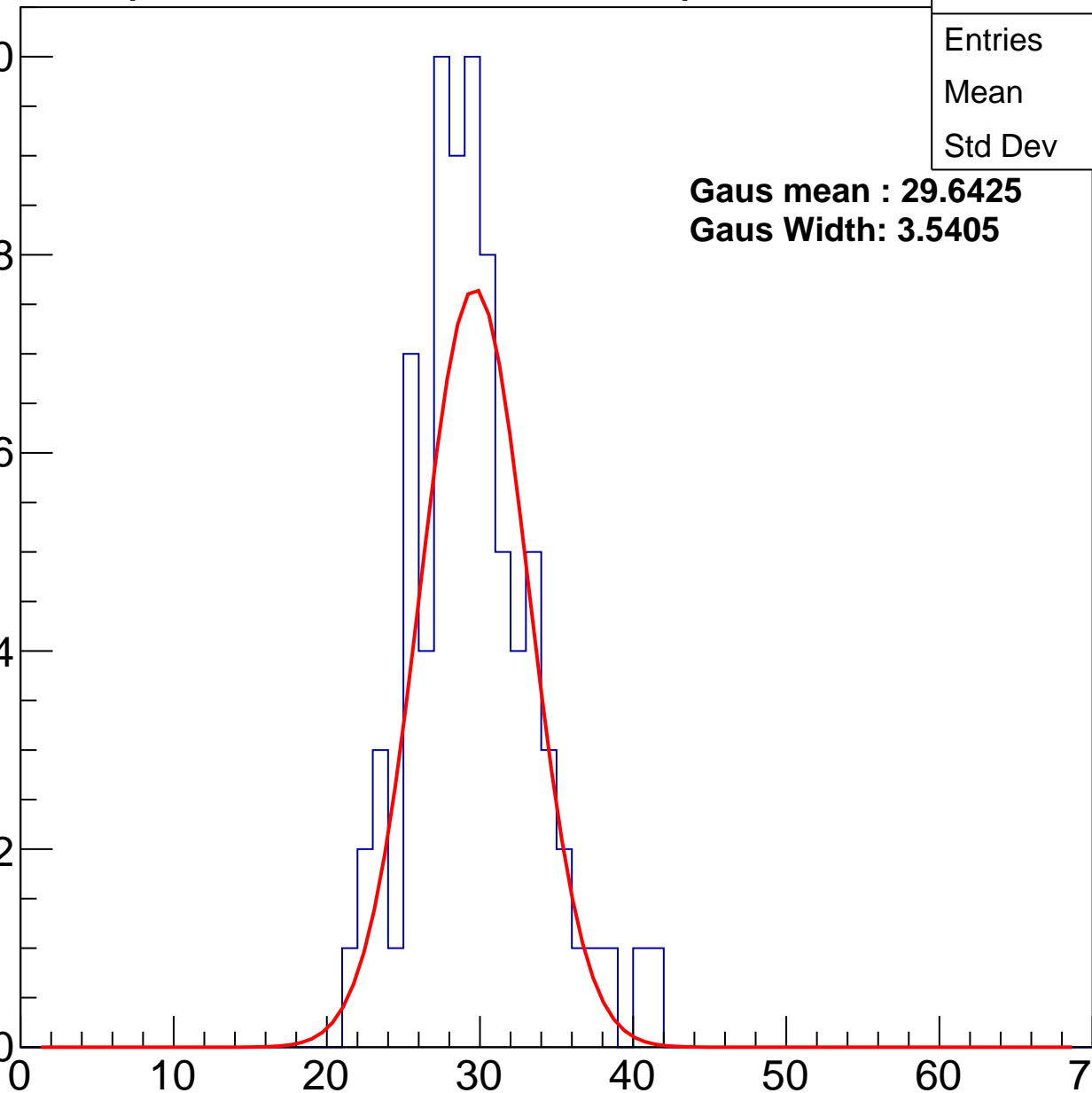
**Gaus mean : 29.6425**

**Gaus Width: 3.5405**

Entry

10  
8  
6  
4  
2  
0

ampl



# B1L102S, U3-ch17, adc1

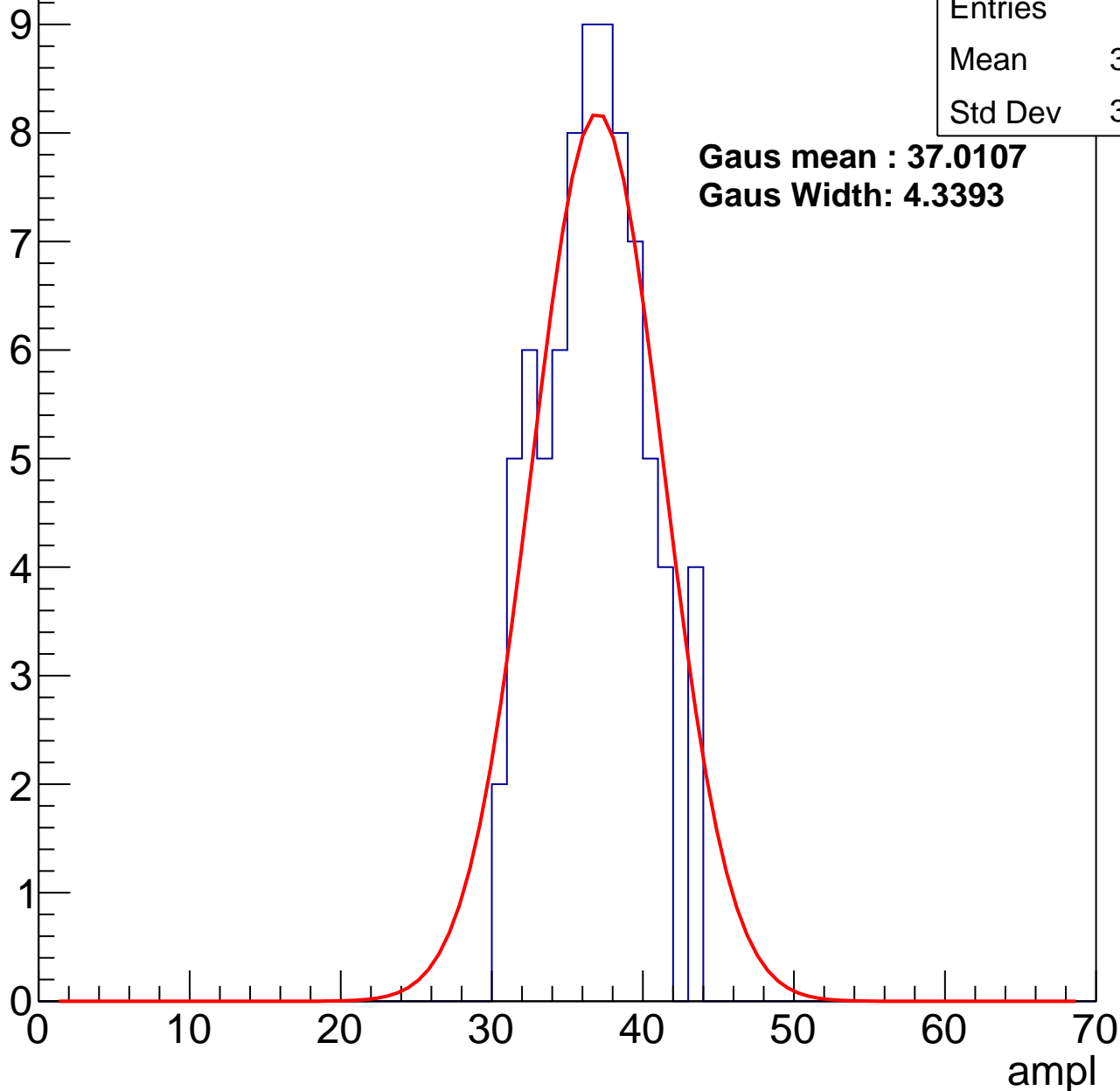
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	36.23
Std Dev	3.293

**Gaus mean : 37.0107**

**Gaus Width: 4.3393**



# B1L102S, U3-ch17, adc2

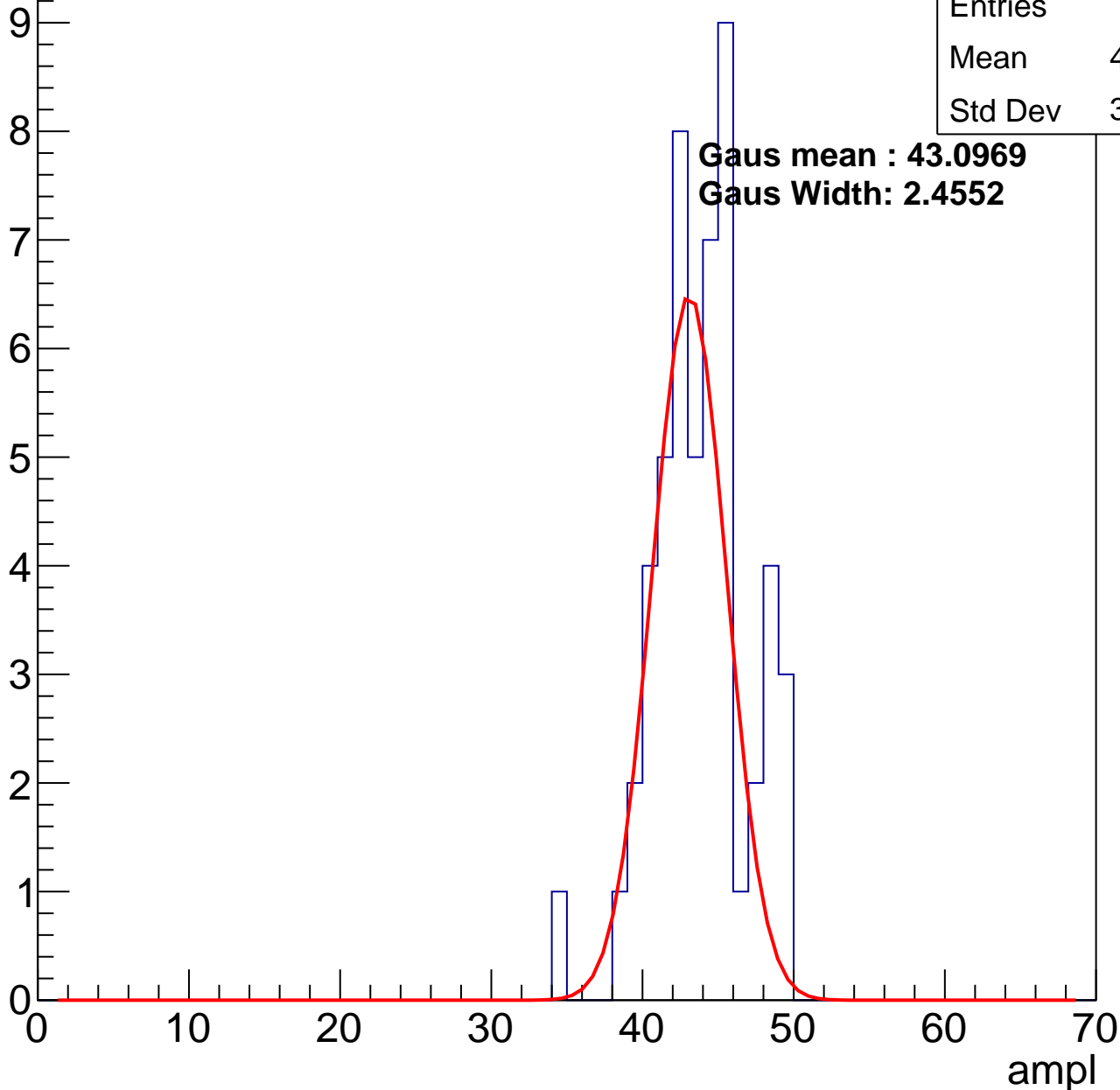
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	43.42
Std Dev	3.053

**Gaus mean : 43.0969**

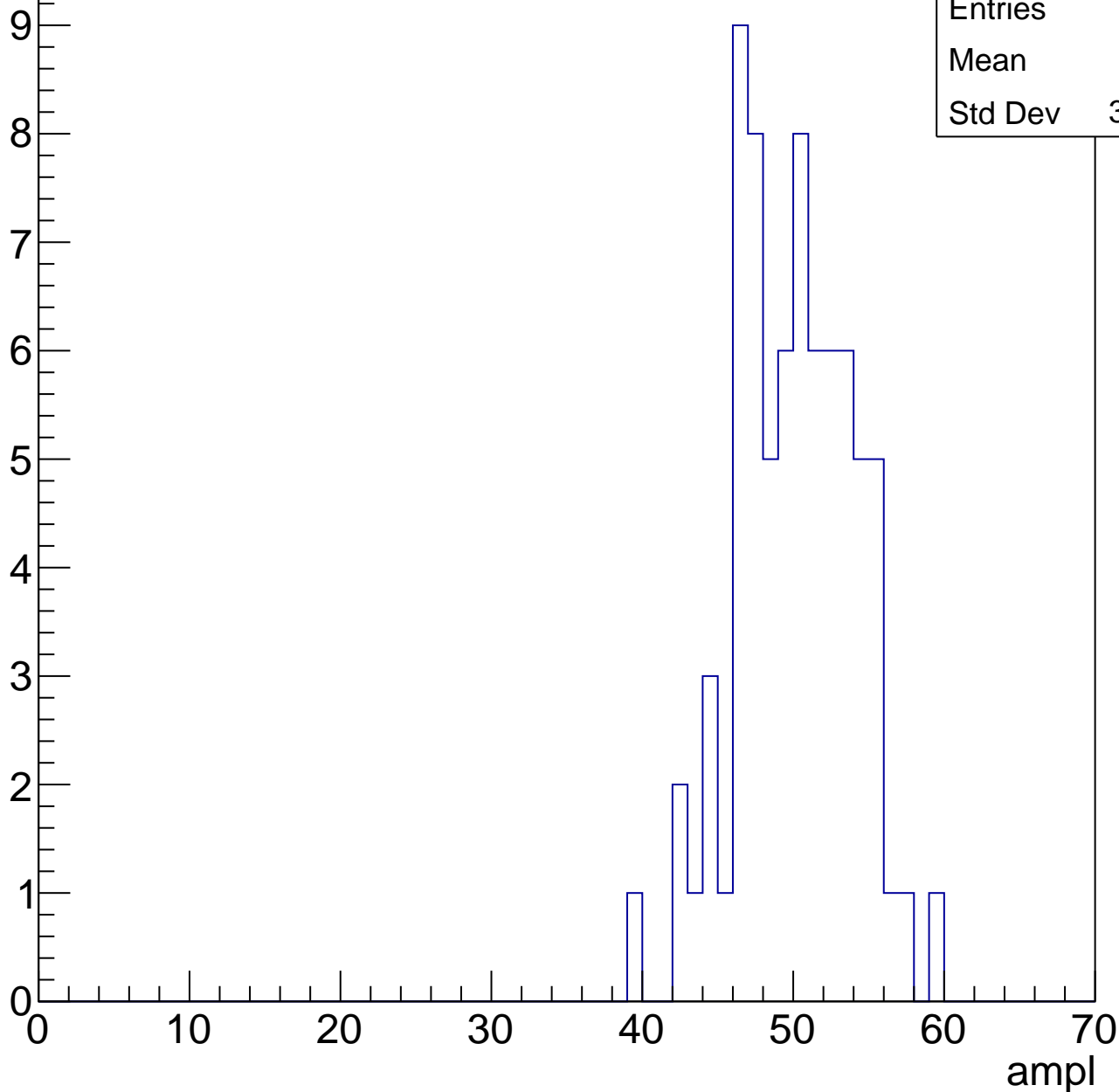
**Gaus Width: 2.4552**



# B1L102S, U3-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



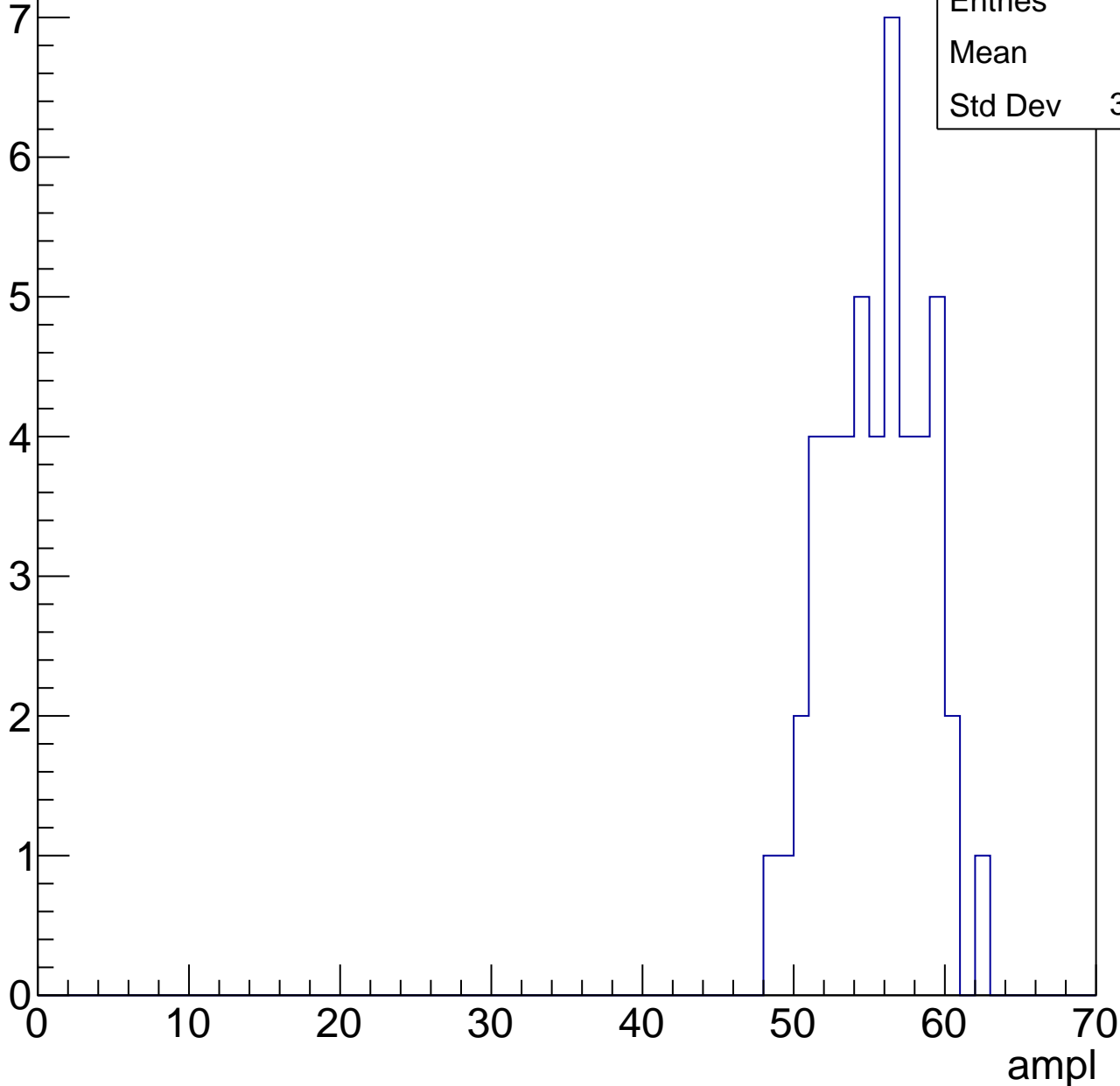
Entries	75
Mean	49.6
Std Dev	3.857

# B1L102S, U3-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	55
Std Dev	3.208



# B1L102S, U3-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

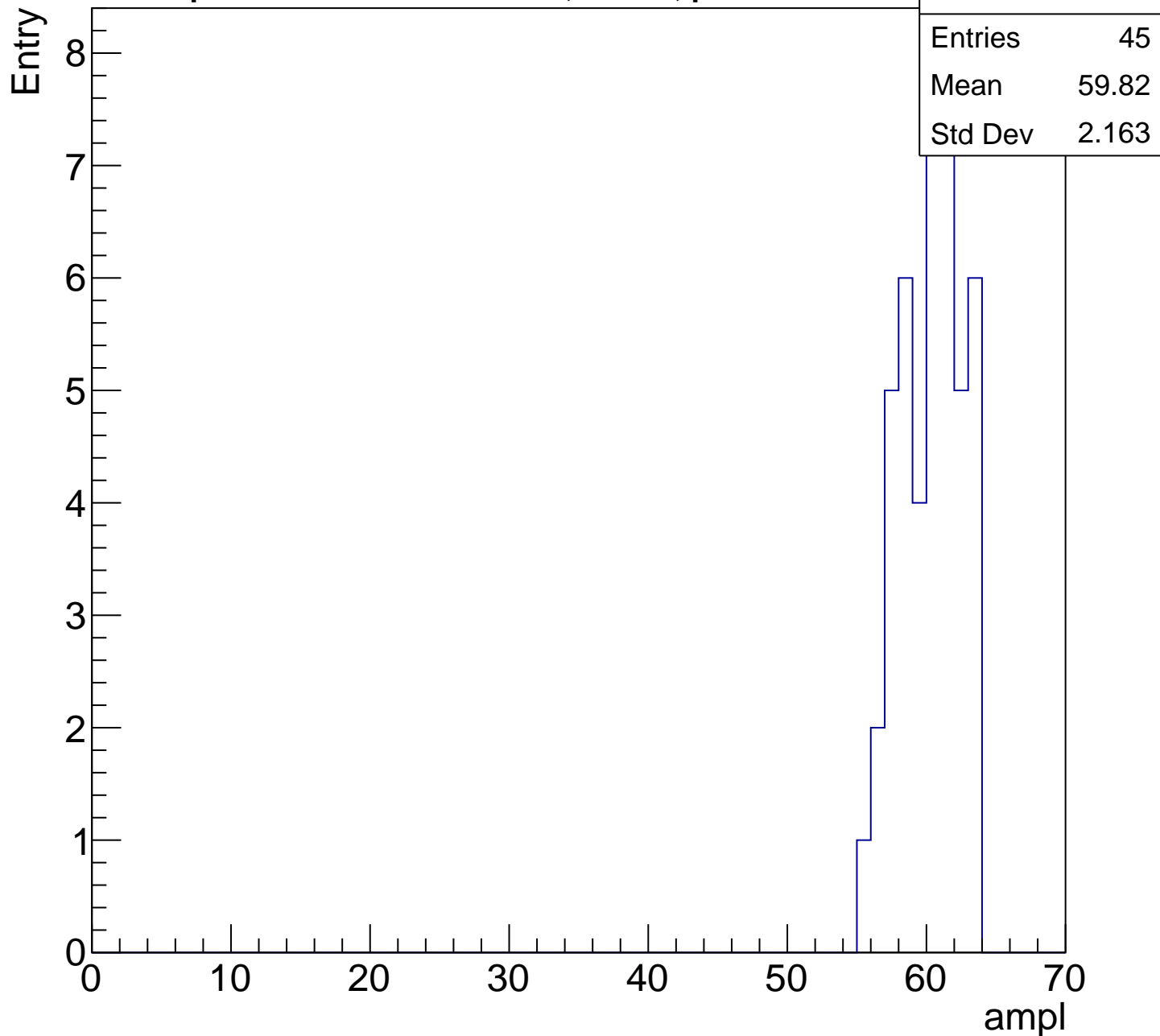
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	45
Mean	59.82
Std Dev	2.163

ampl

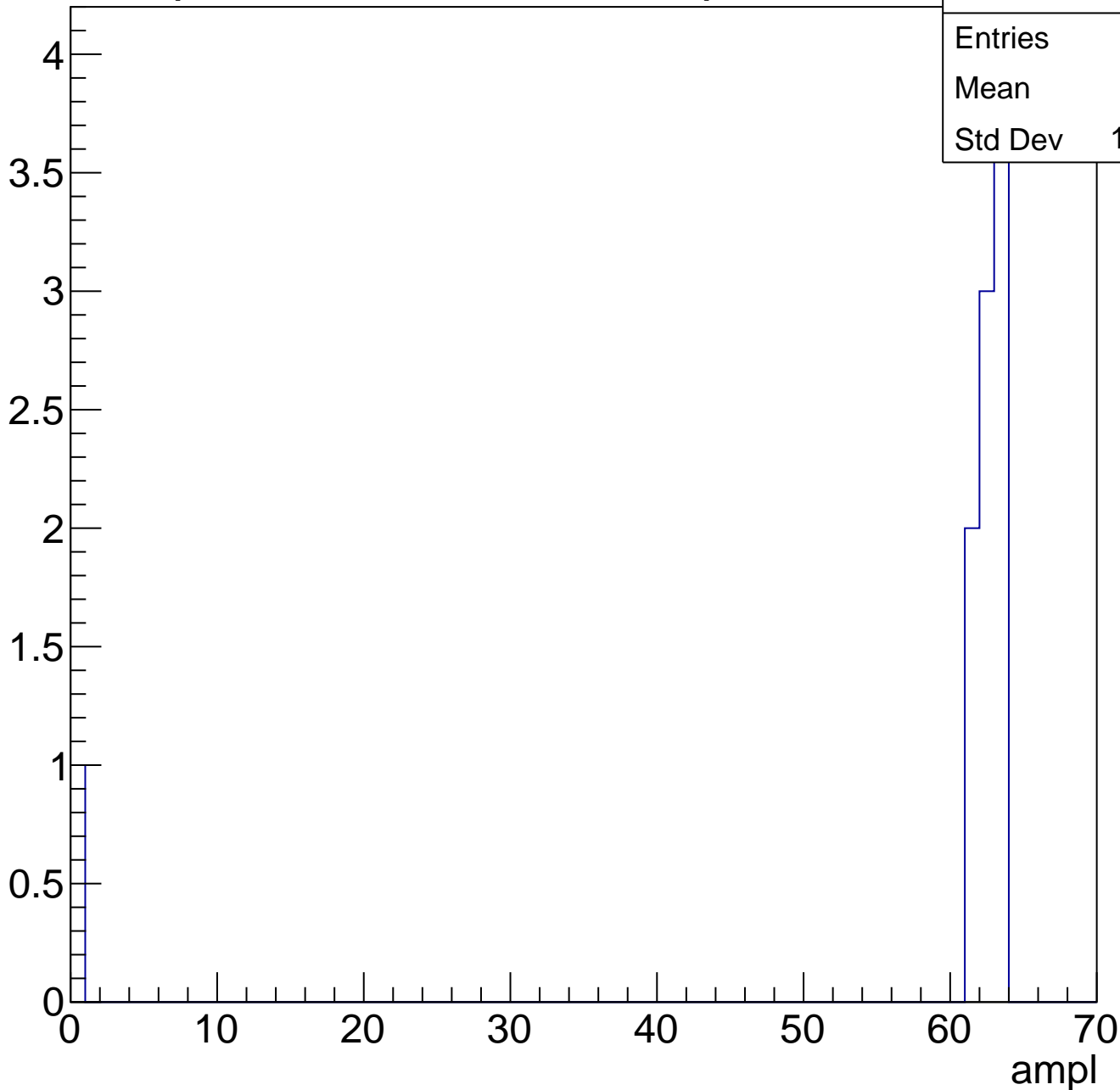
0 10 20 30 40 50 60 70



# B1L102S, U3-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch18, adc0

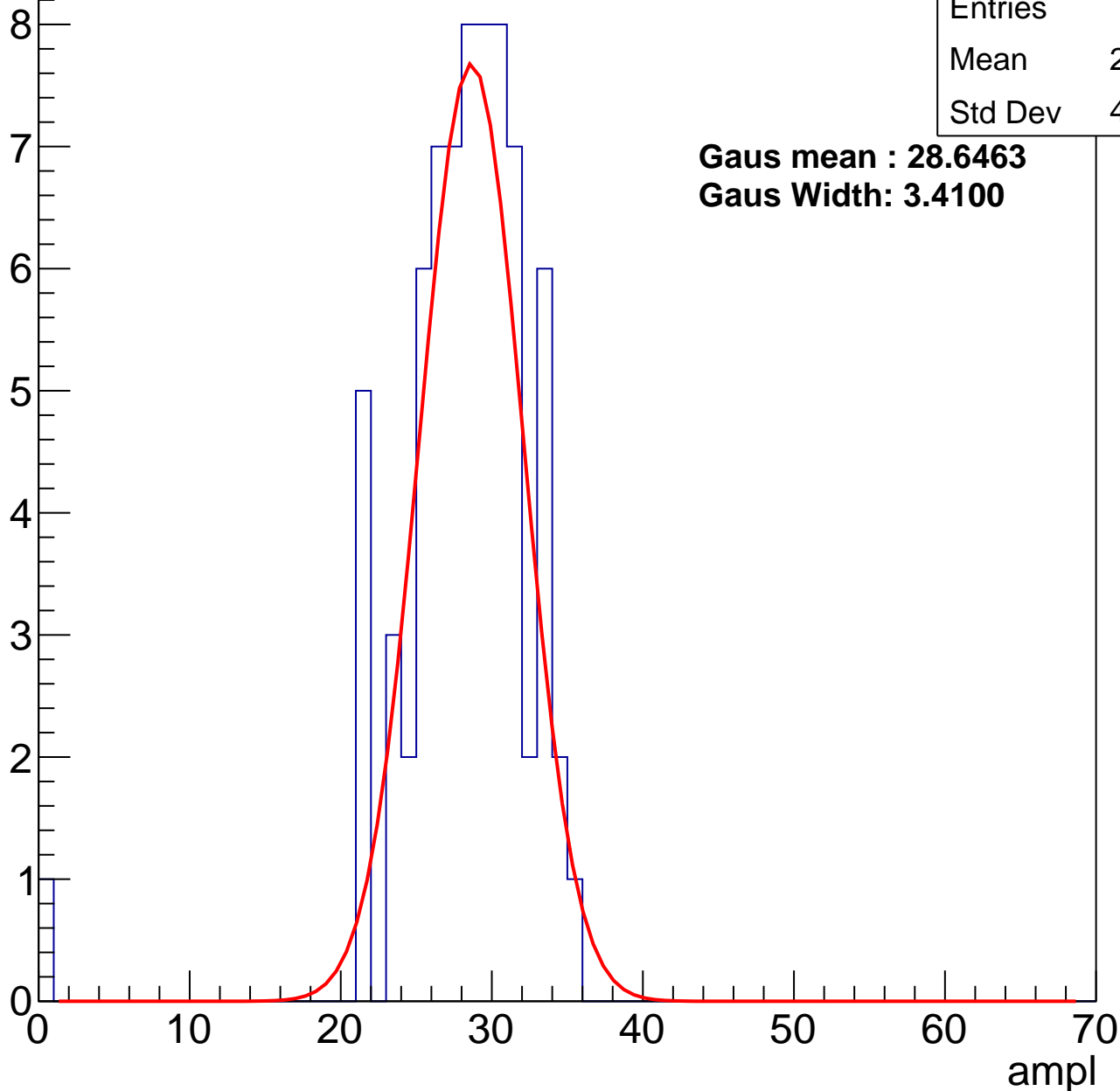
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	27.68
Std Dev	4.716

**Gaus mean : 28.6463**

**Gaus Width: 3.4100**



# B1L102S, U3-ch18, adc1

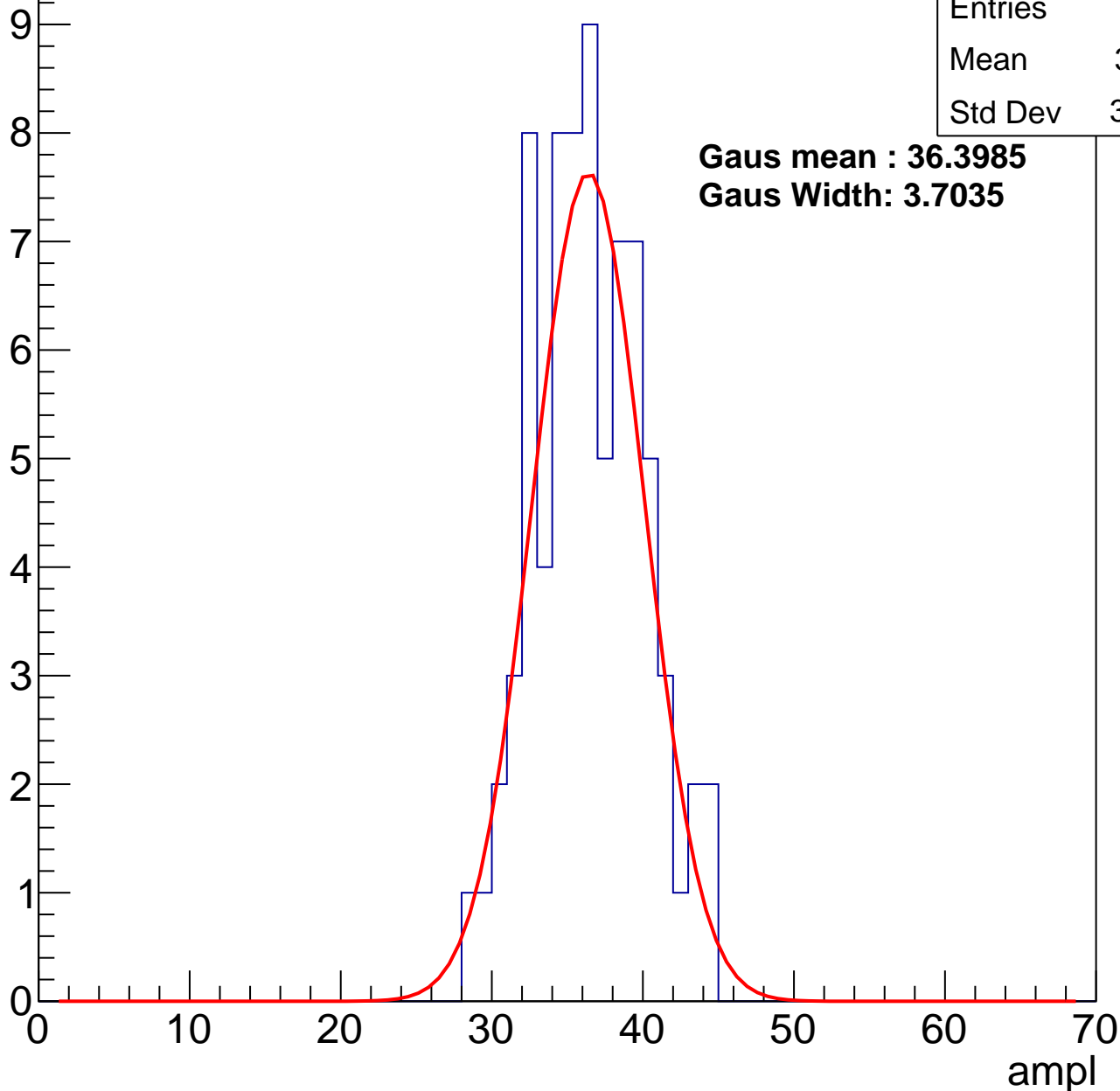
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	36.01
Std Dev	3.585

**Gaus mean : 36.3985**

**Gaus Width: 3.7035**



# B1L102S, U3-ch18, adc2

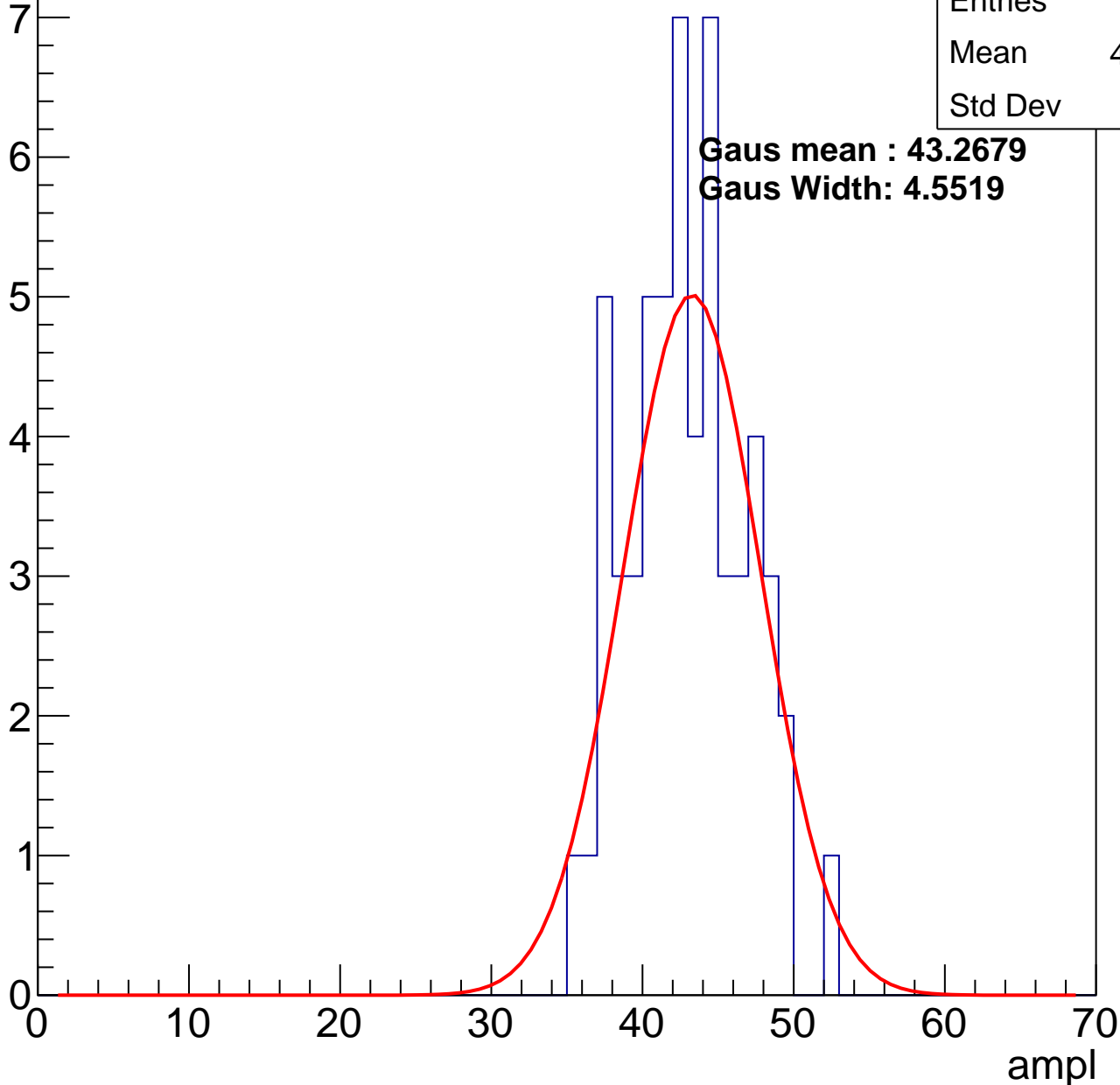
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	42.47
Std Dev	3.77

**Gaus mean : 43.2679**

**Gaus Width: 4.5519**



# B1L102S, U3-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

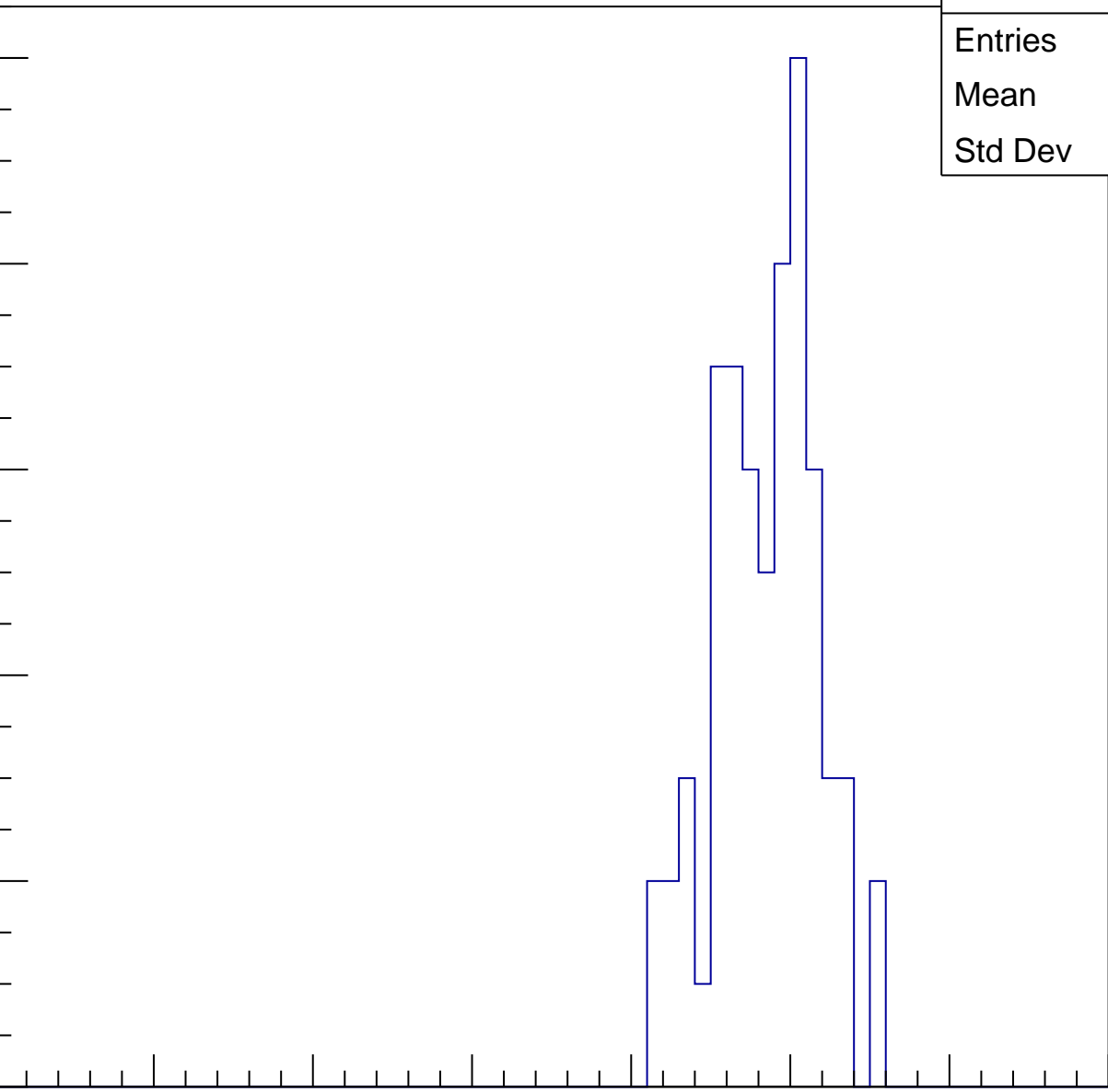
Entries	65
Mean	48.02
Std Dev	3.237

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

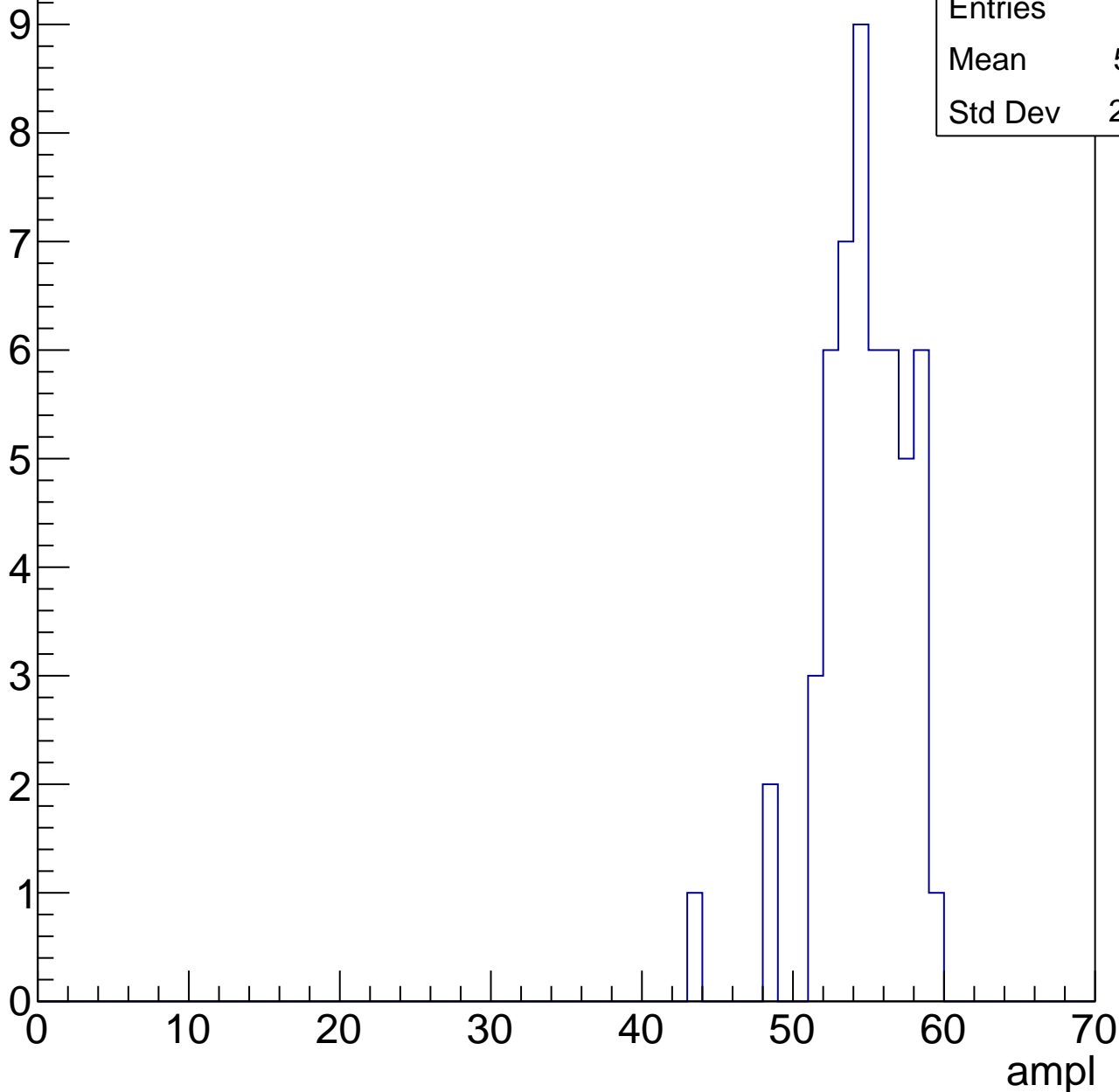


# B1L102S, U3-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	54.21
Std Dev	2.924

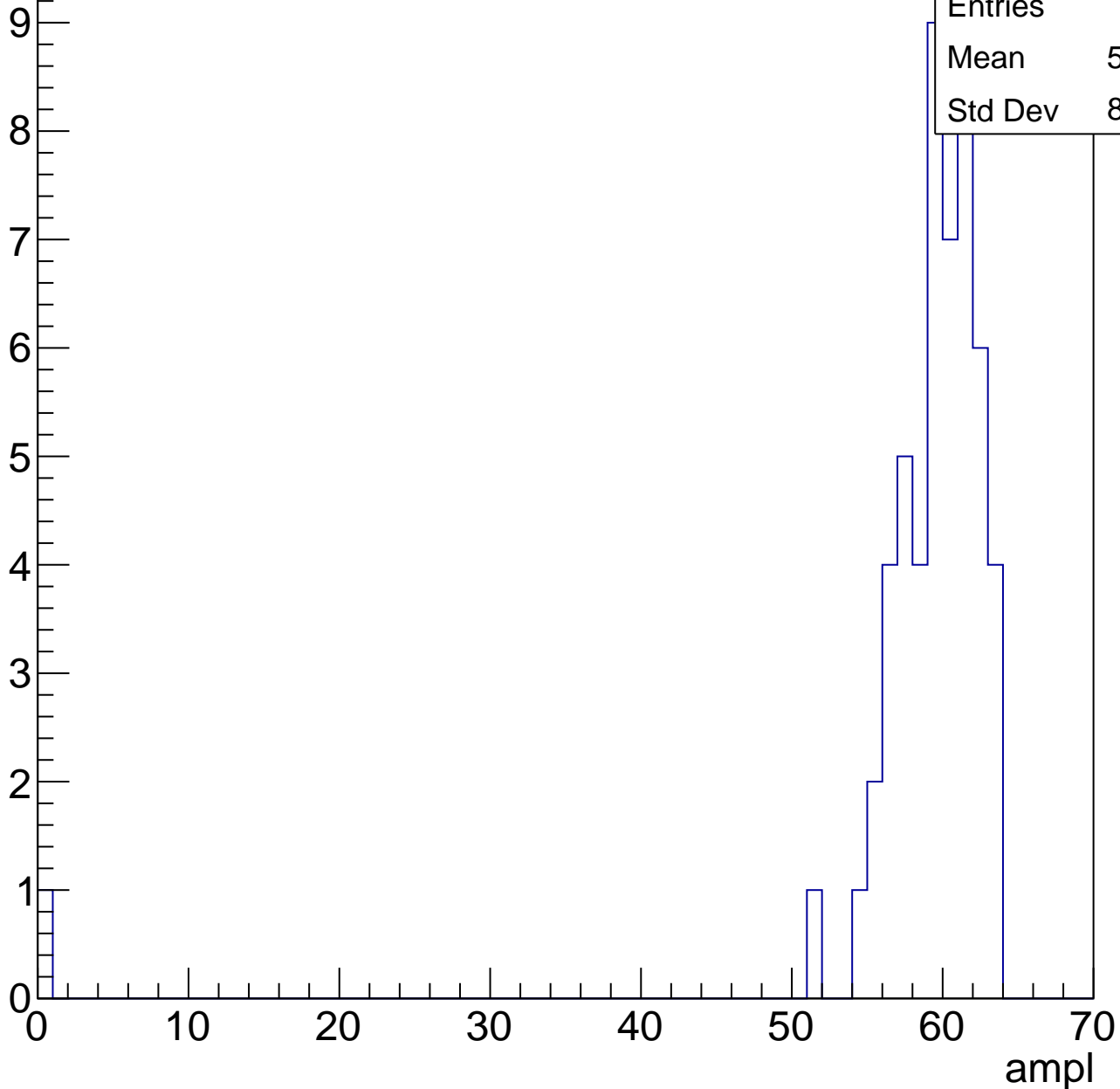


# B1L102S, U3-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	58.06
Std Dev	8.518

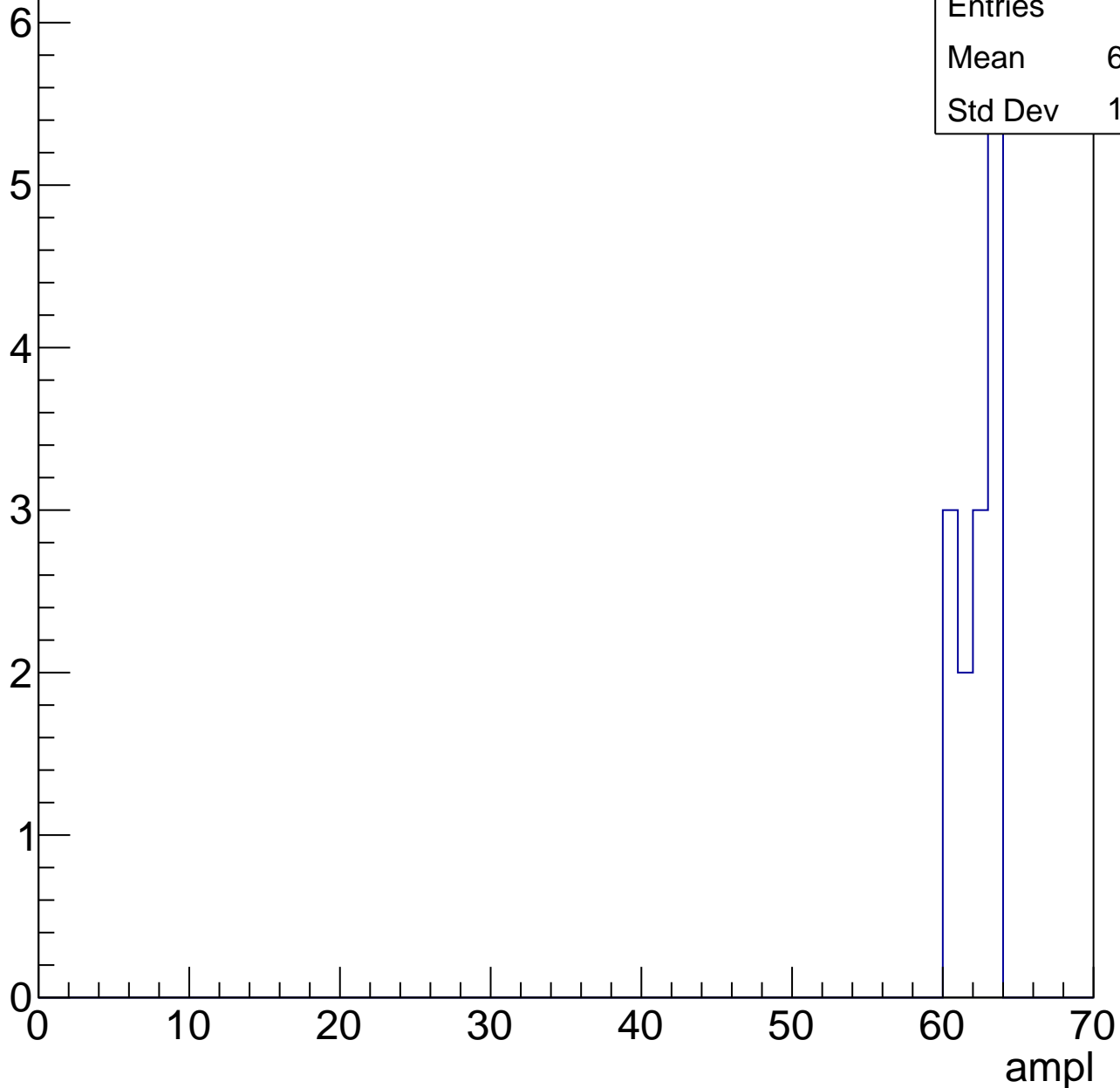


# B1L102S, U3-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	14
Mean	61.86
Std Dev	1.187





# B1L102S, U3-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch19, adc0

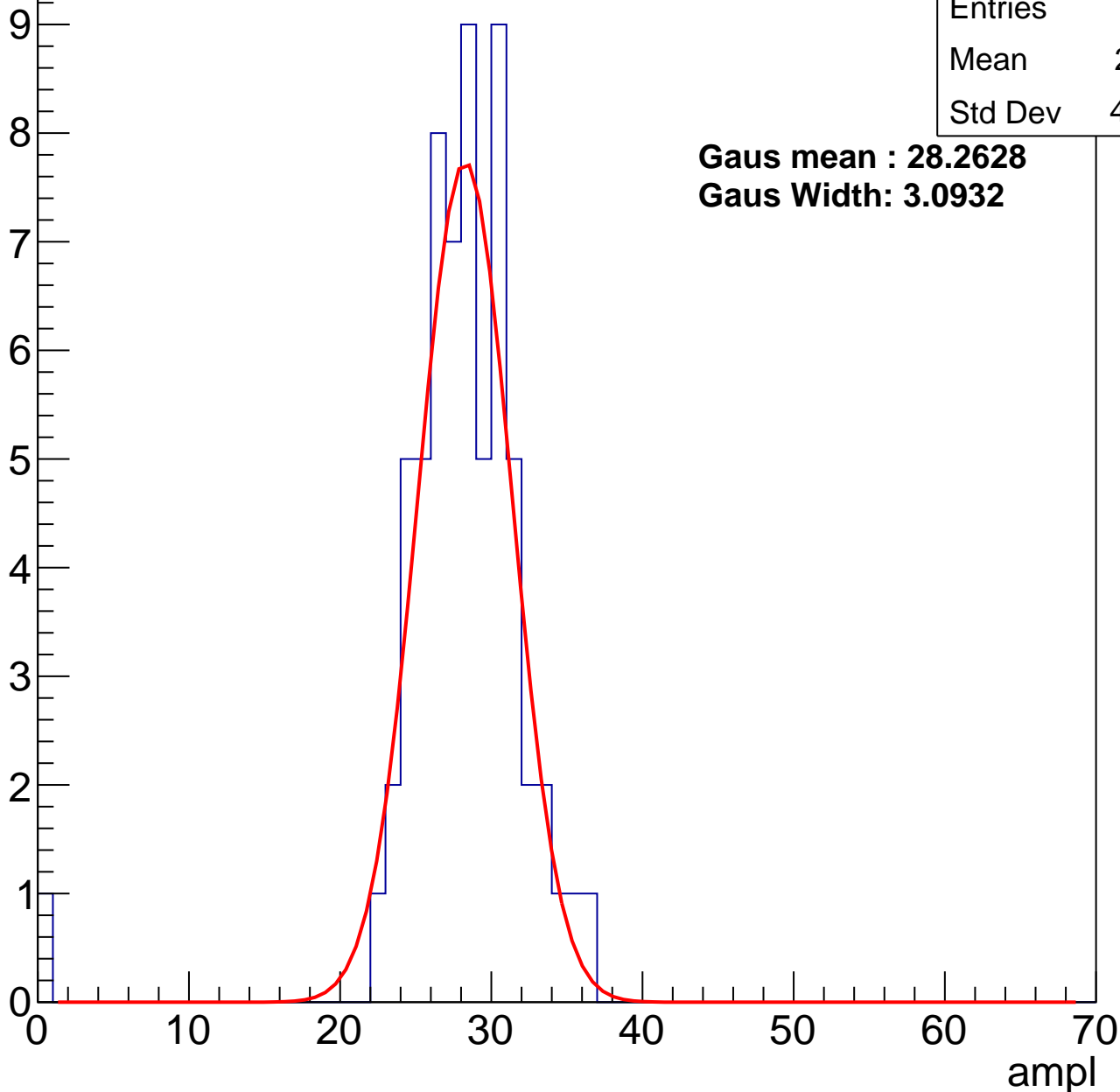
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	27.61
Std Dev	4.578

**Gaus mean : 28.2628**

**Gaus Width: 3.0932**



# B1L102S, U3-ch19, adc1

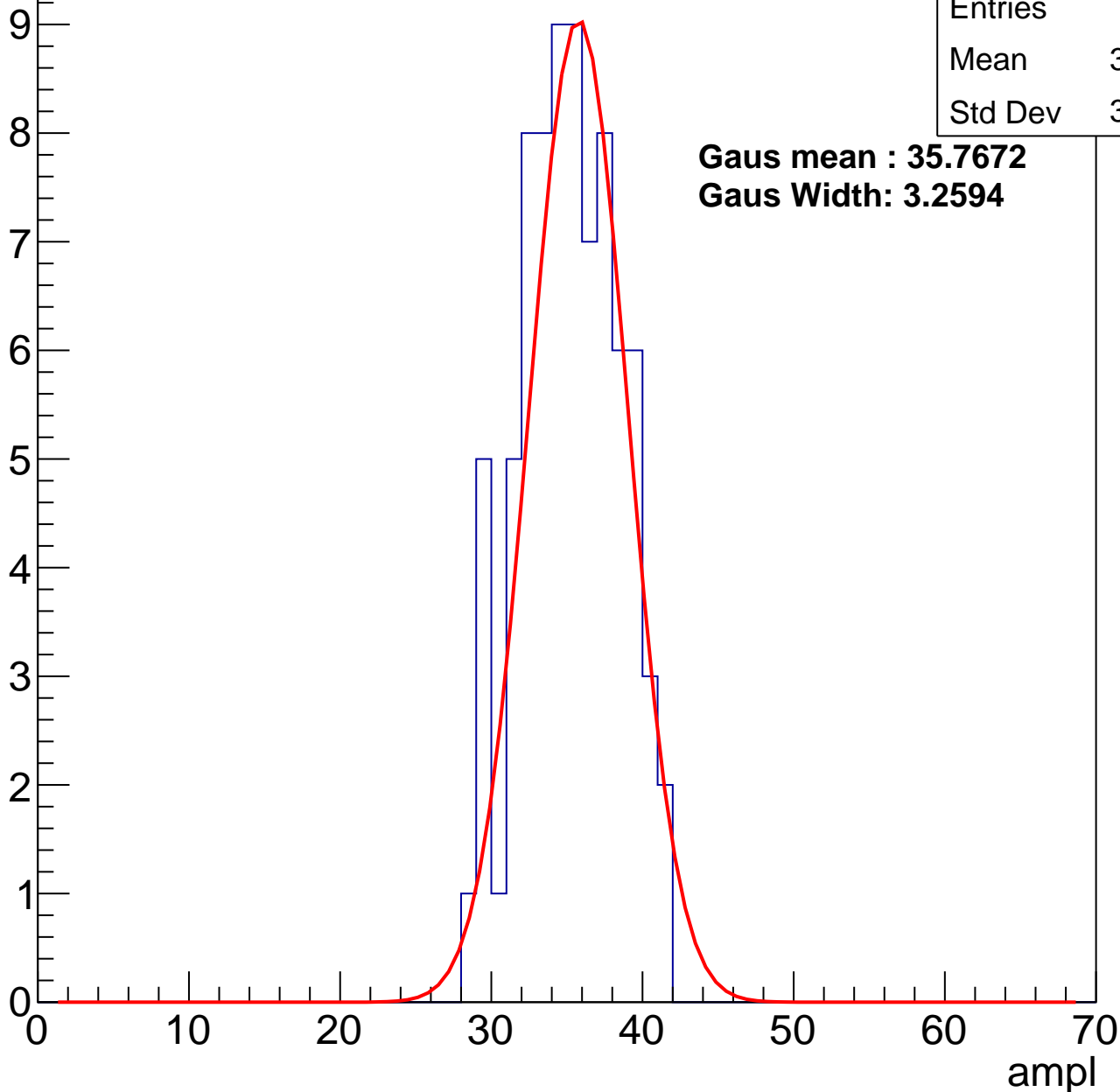
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	34.76
Std Dev	3.159

**Gaus mean : 35.7672**

**Gaus Width: 3.2594**



# B1L102S, U3-ch19, adc2

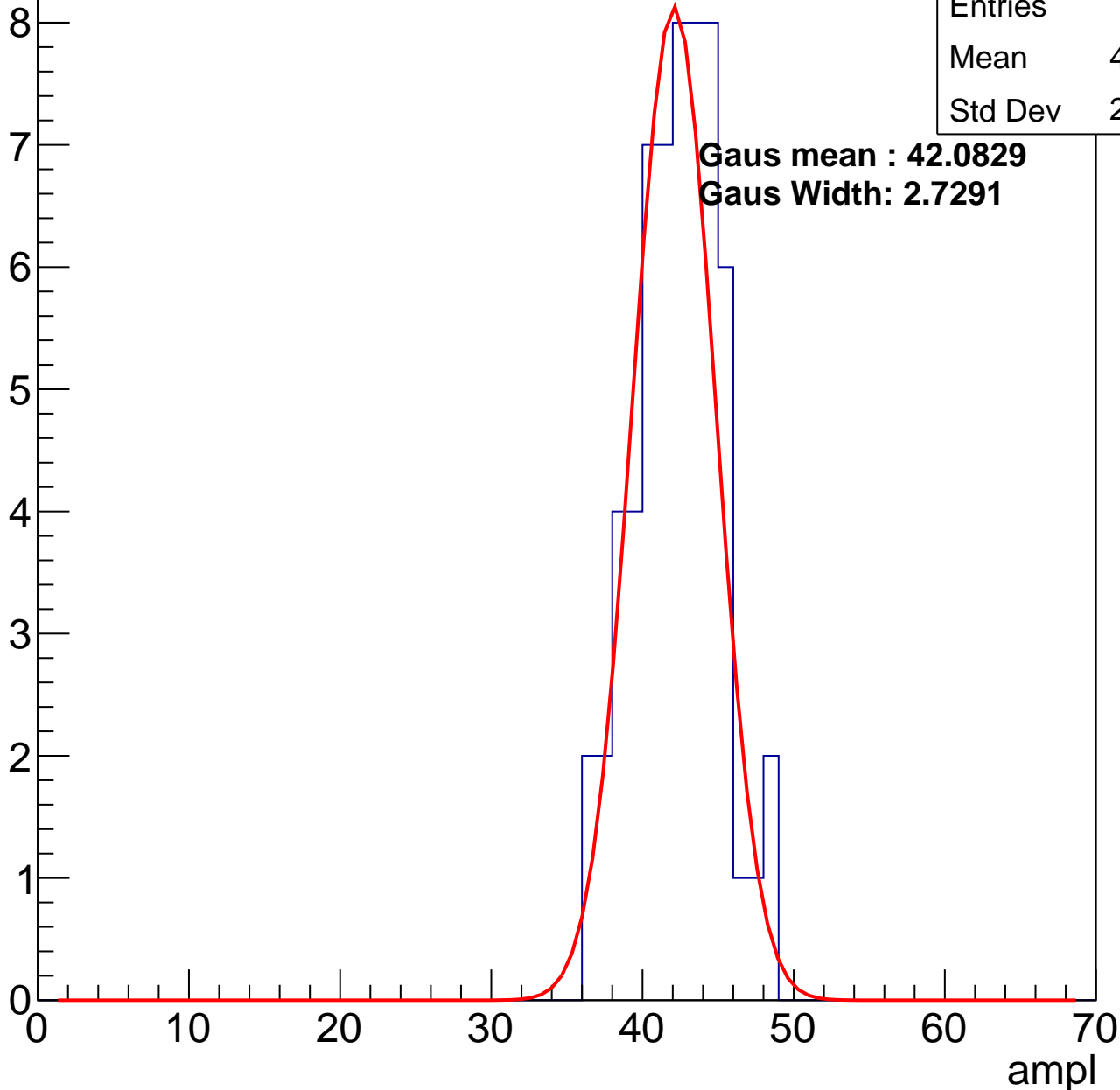
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	41.87
Std Dev	2.778

**Gaus mean : 42.0829**

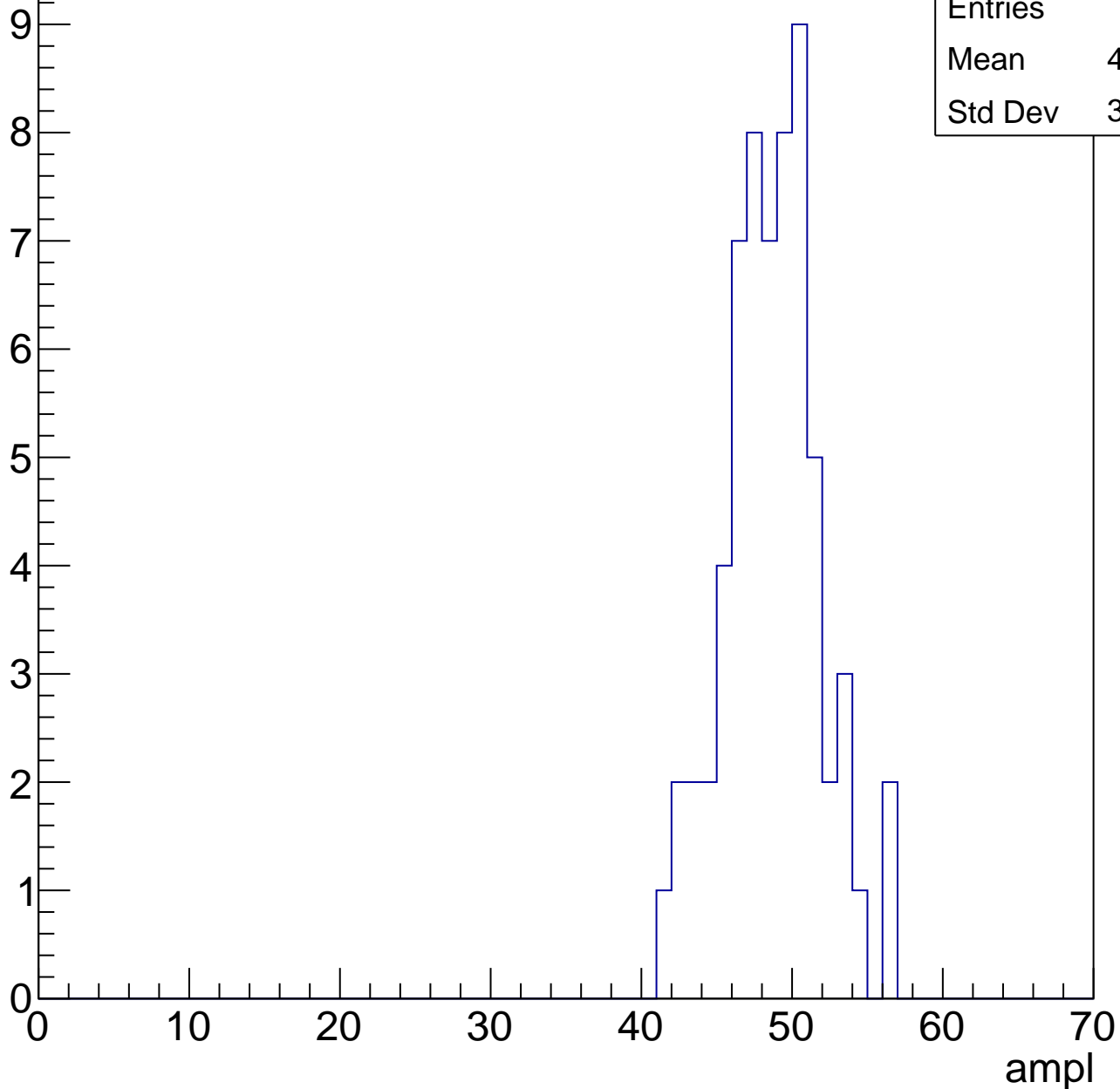
**Gaus Width: 2.7291**



# B1L102S, U3-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

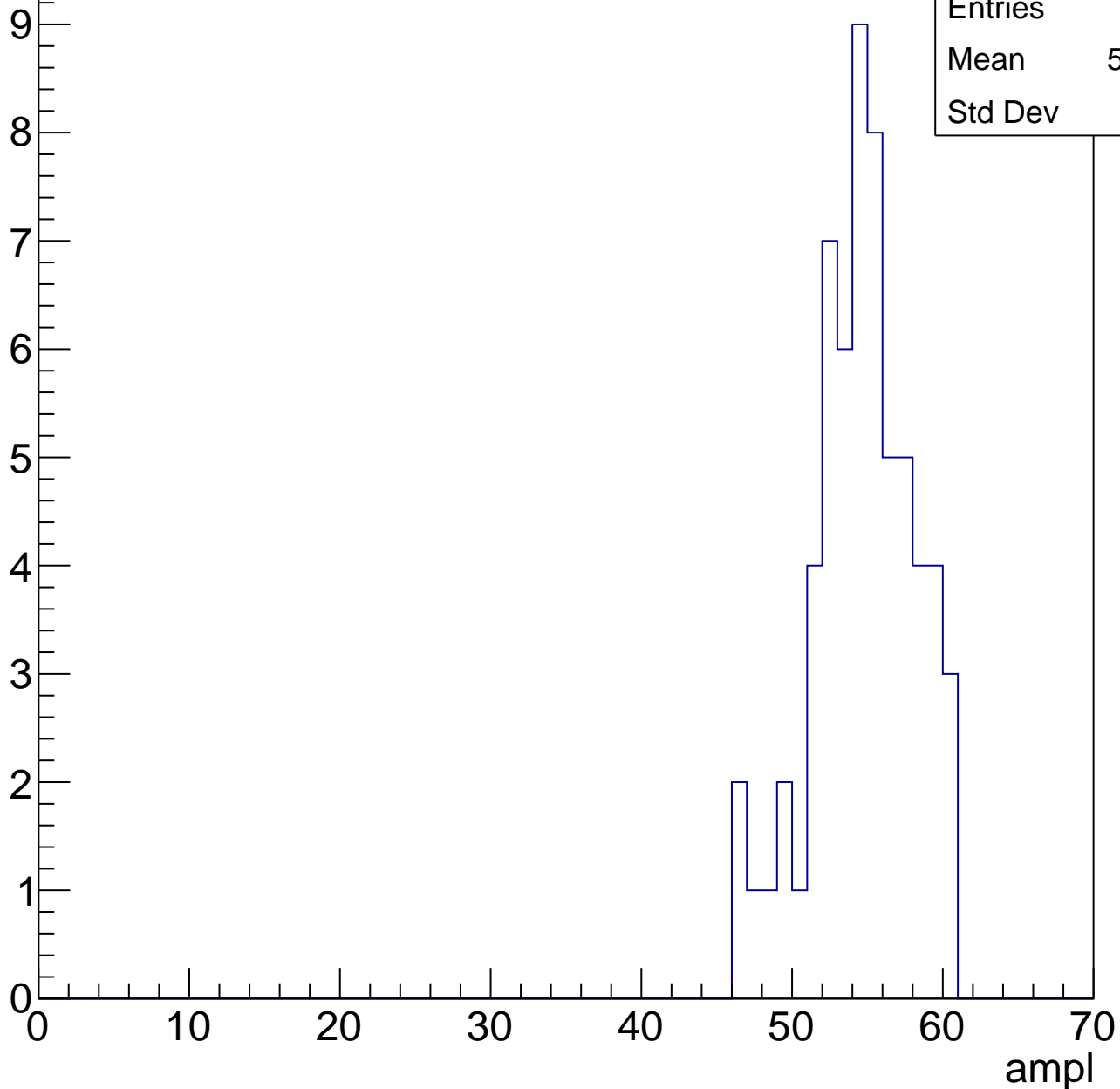


Entries	63
Mean	48.24
Std Dev	3.166

# B1L102S, U3-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



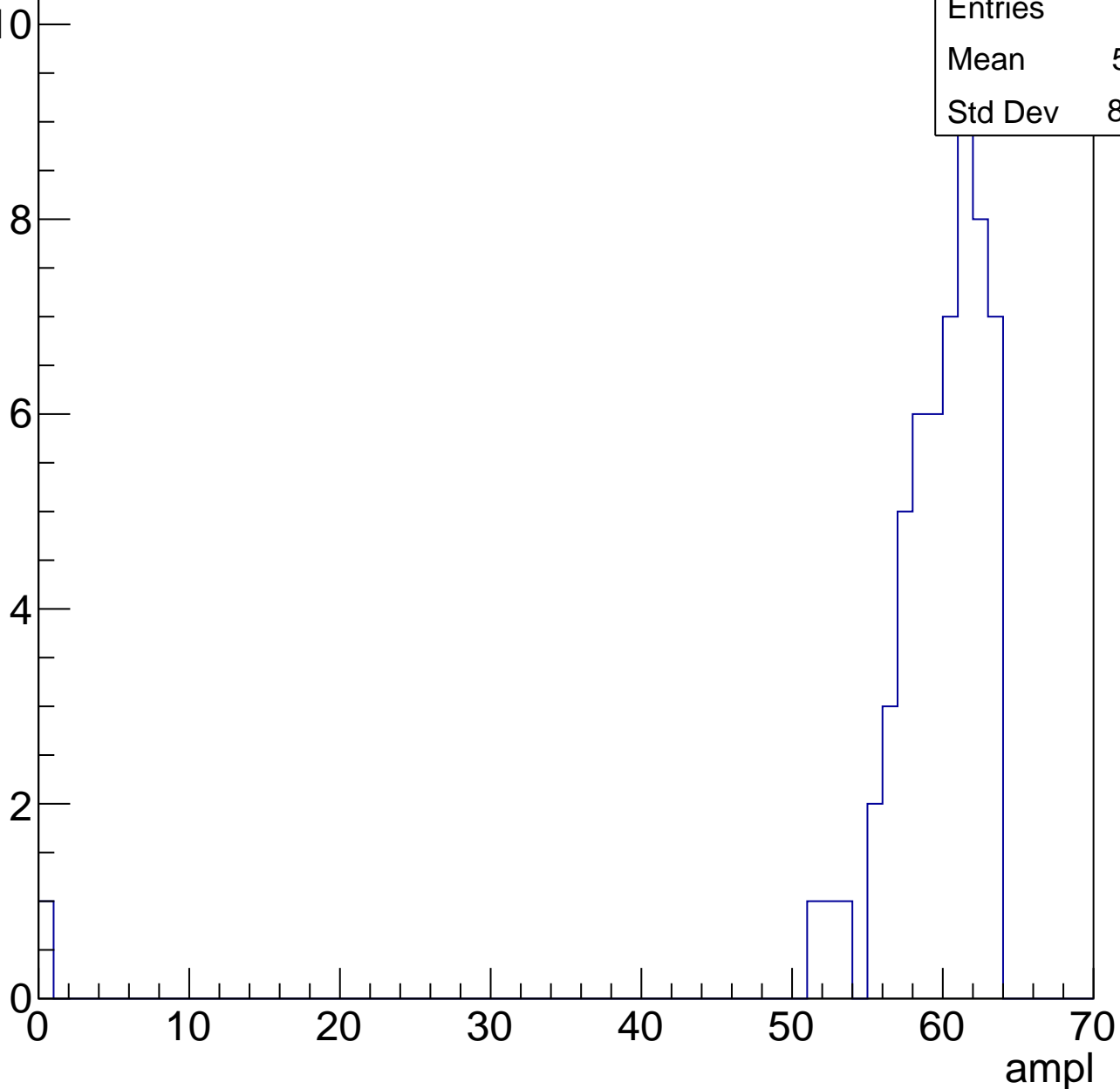
Entries	62
Mean	54.19
Std Dev	3.34

# B1L102S, U3-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	58.41
Std Dev	8.227



# B1L102S, U3-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch20, adc0

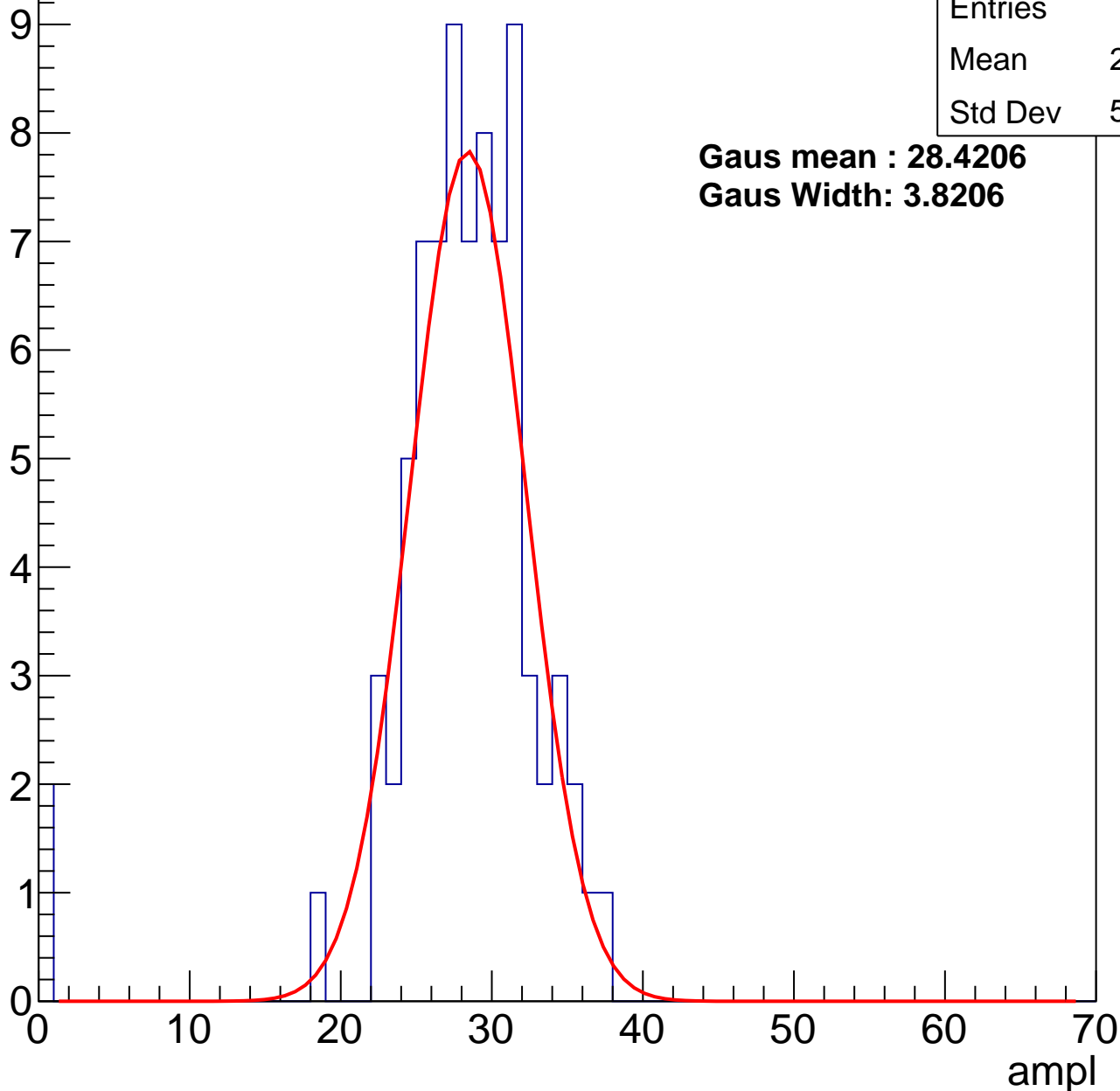
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	27.52
Std Dev	5.686

**Gaus mean : 28.4206**

**Gaus Width: 3.8206**



# B1L102S, U3-ch20, adc1

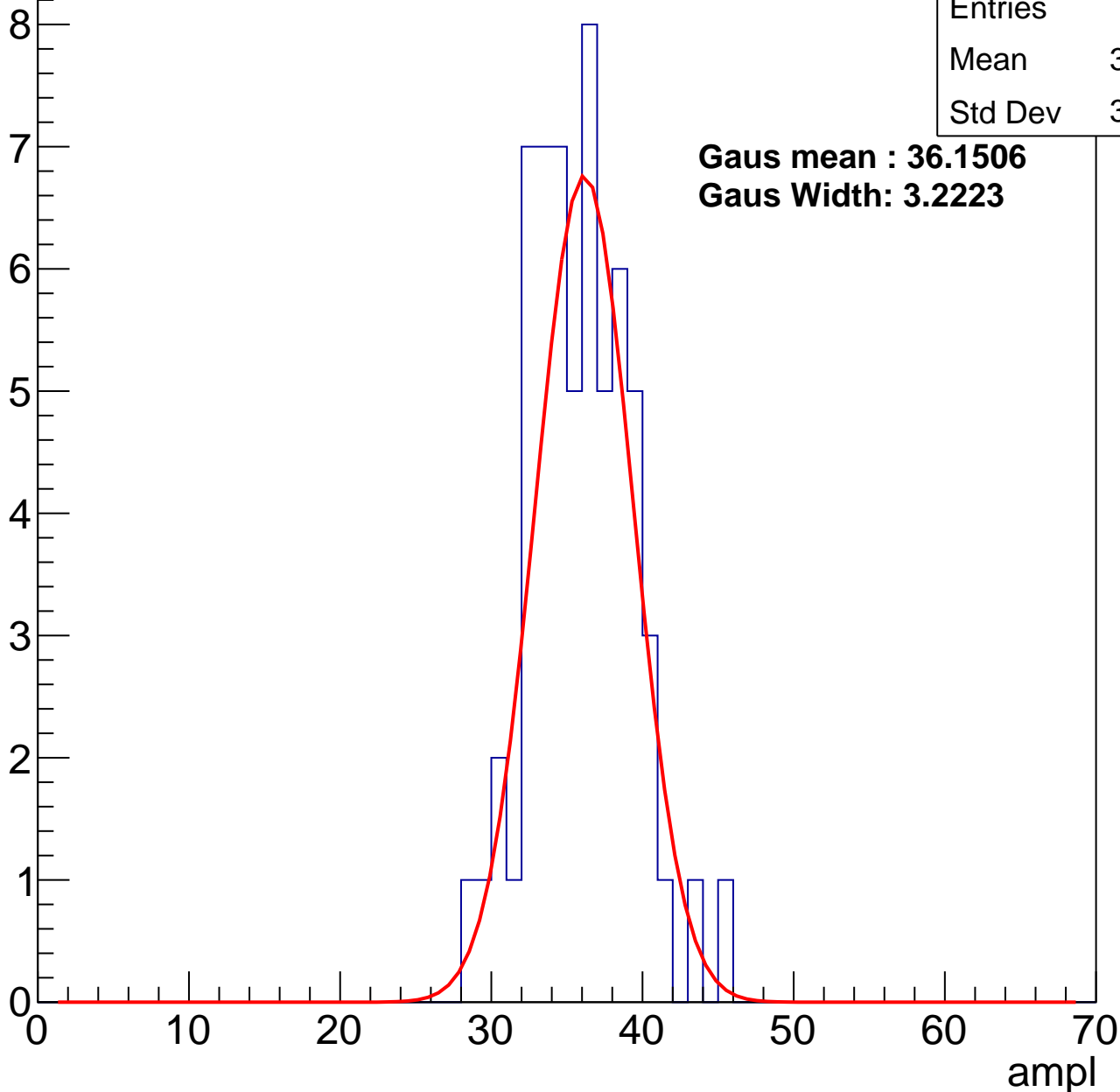
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	35.43
Std Dev	3.326

**Gaus mean : 36.1506**

**Gaus Width: 3.2223**



# B1L102S, U3-ch20, adc2

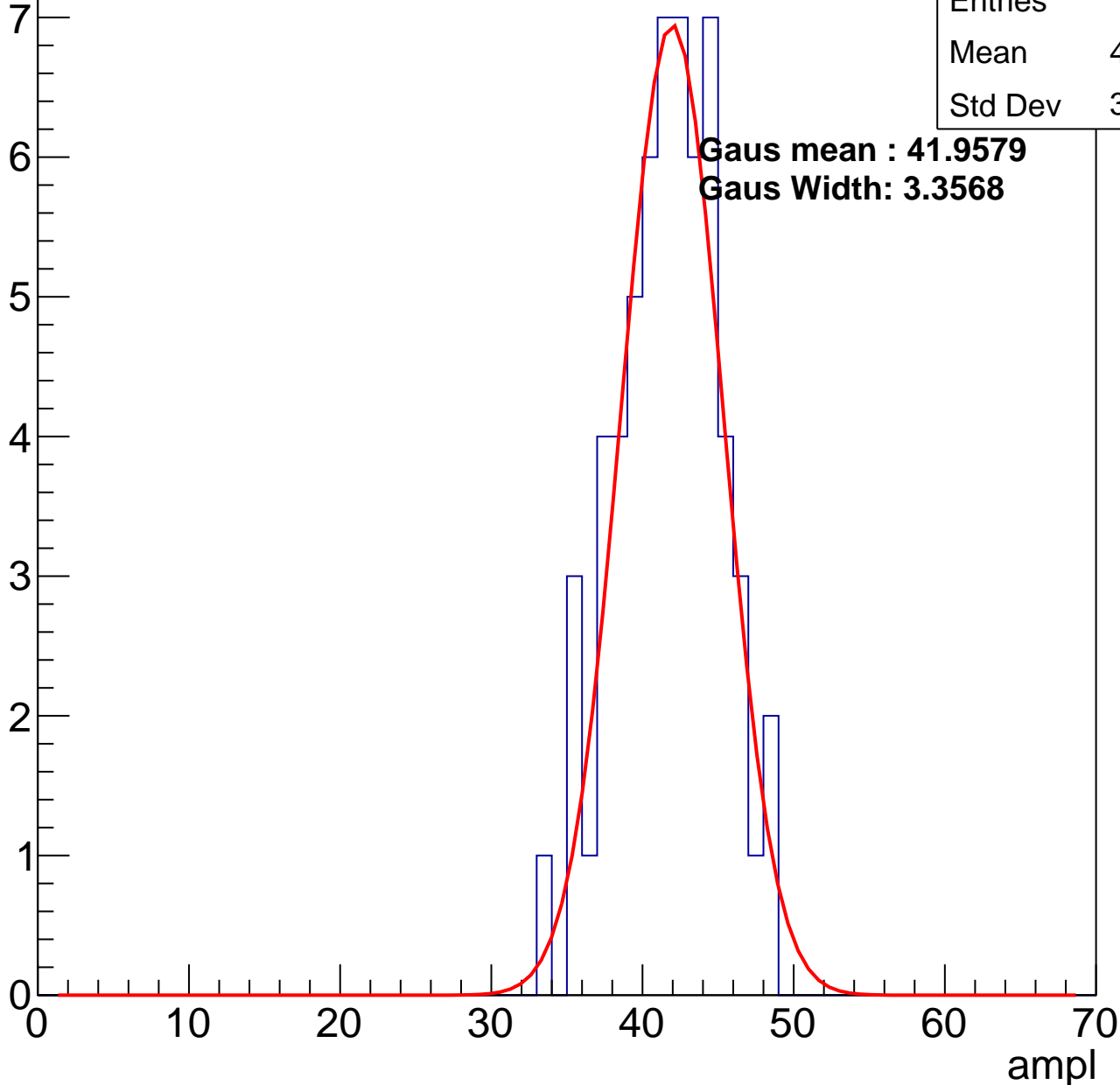
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	41.26
Std Dev	3.353

**Gaus mean : 41.9579**

**Gaus Width: 3.3568**



# B1L102S, U3-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	68
Mean	47.79
Std Dev	3.479

Entry

10

8

6

4

2

0

0

10

20

30

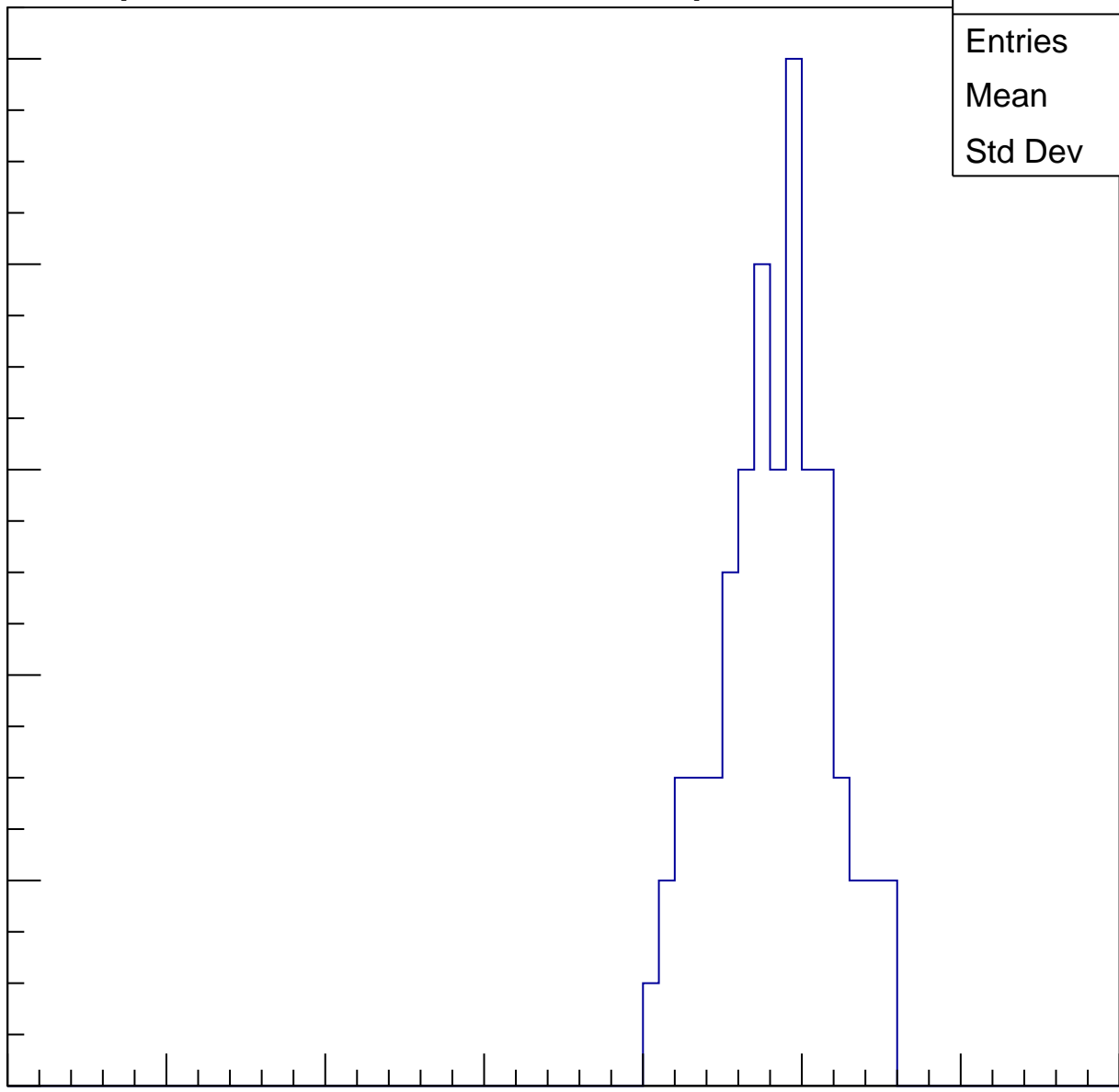
40

50

60

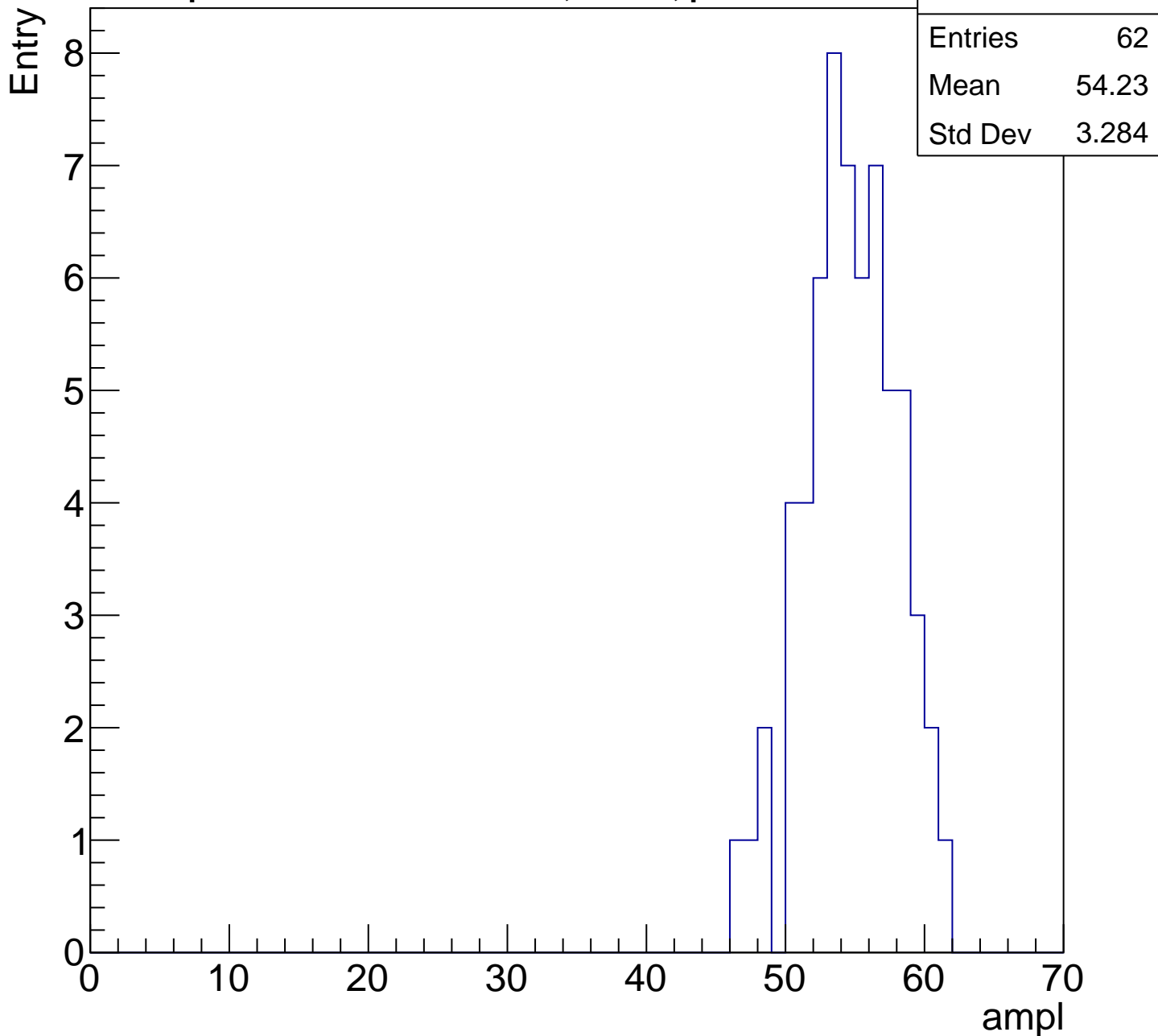
70

ampl



# B1L102S, U3-ch20, adc4

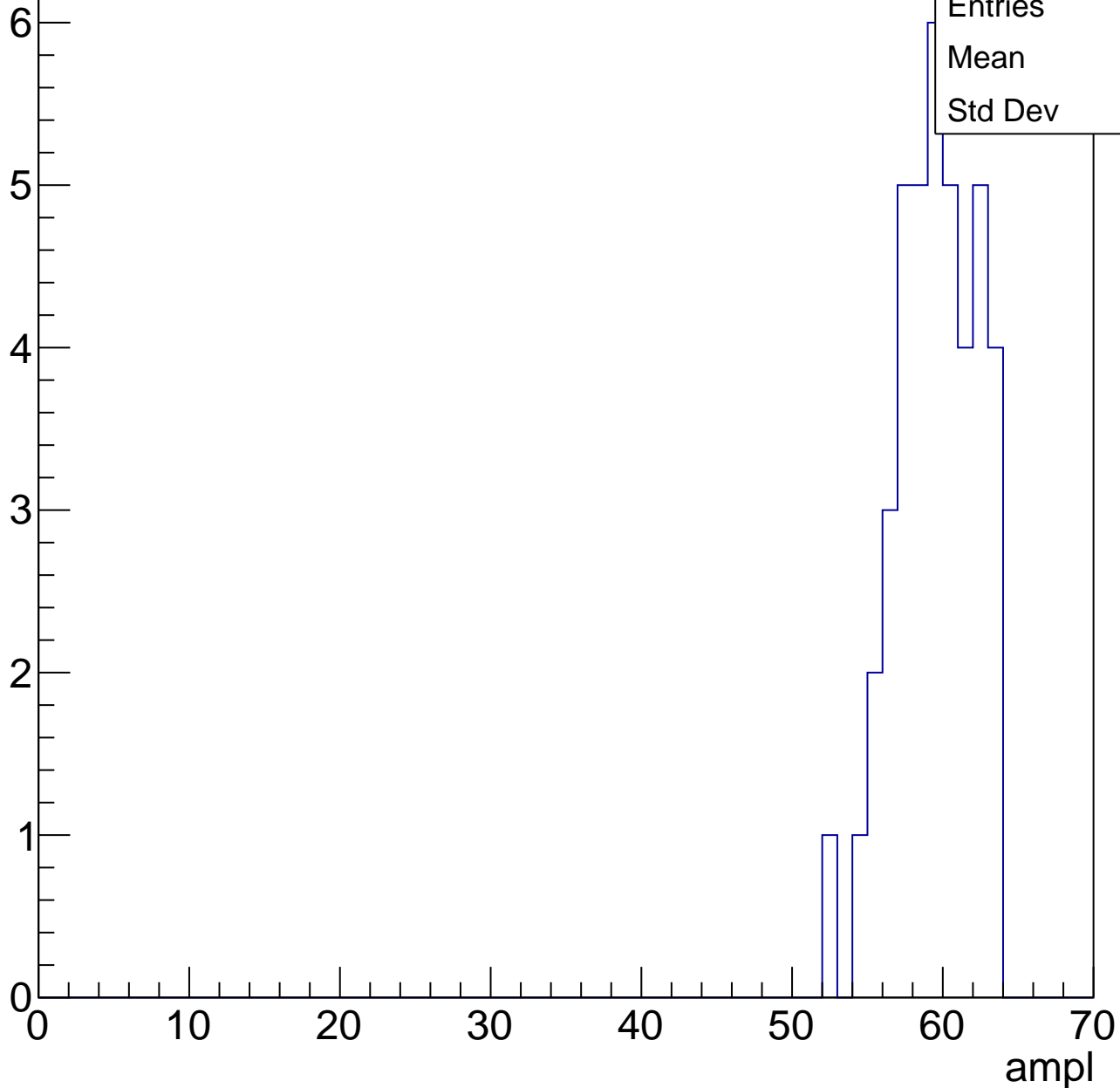
calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U3-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



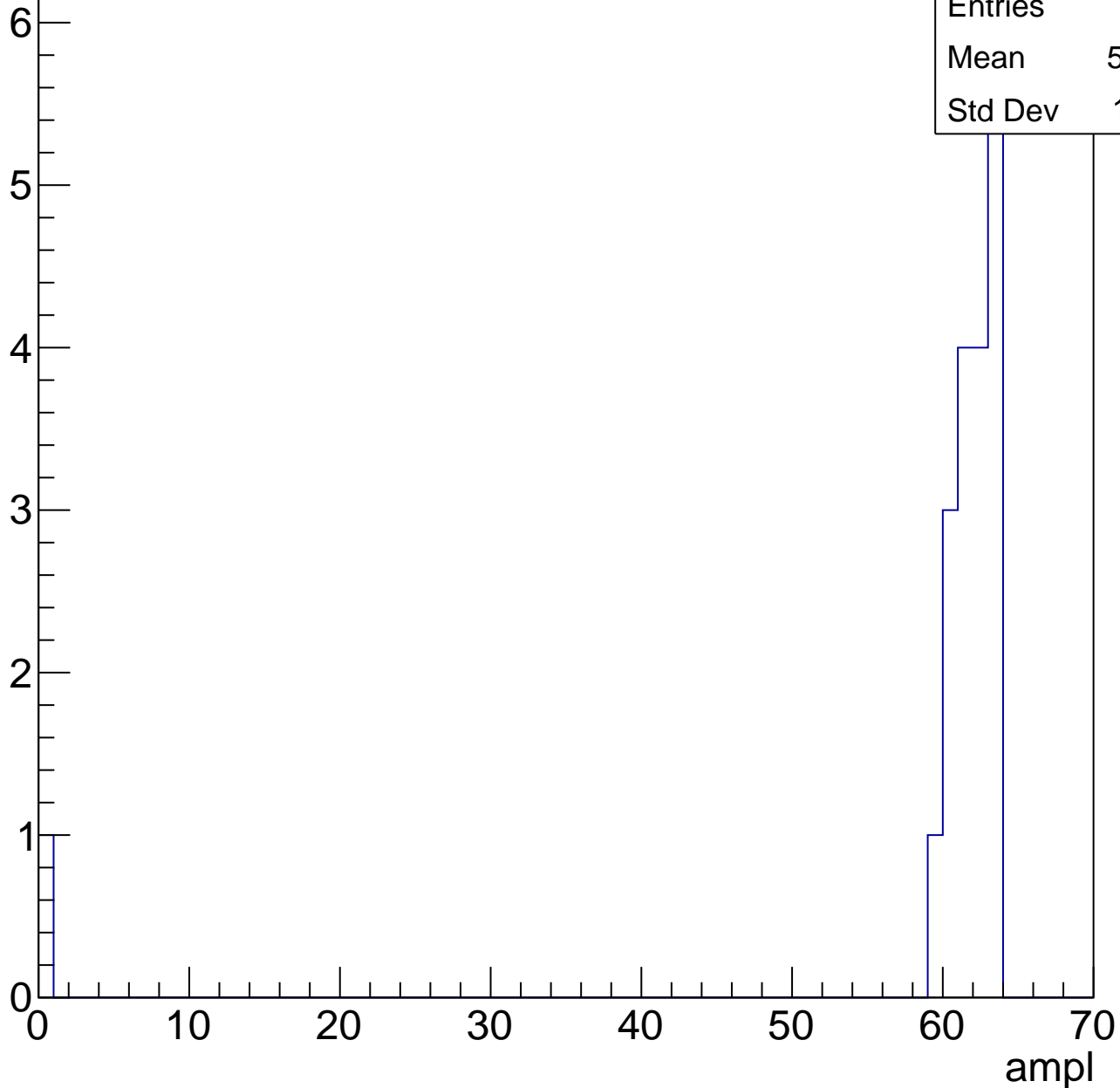
Entries	41
Mean	59
Std Dev	2.65

# B1L102S, U3-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	19
Mean	58.37
Std Dev	13.81

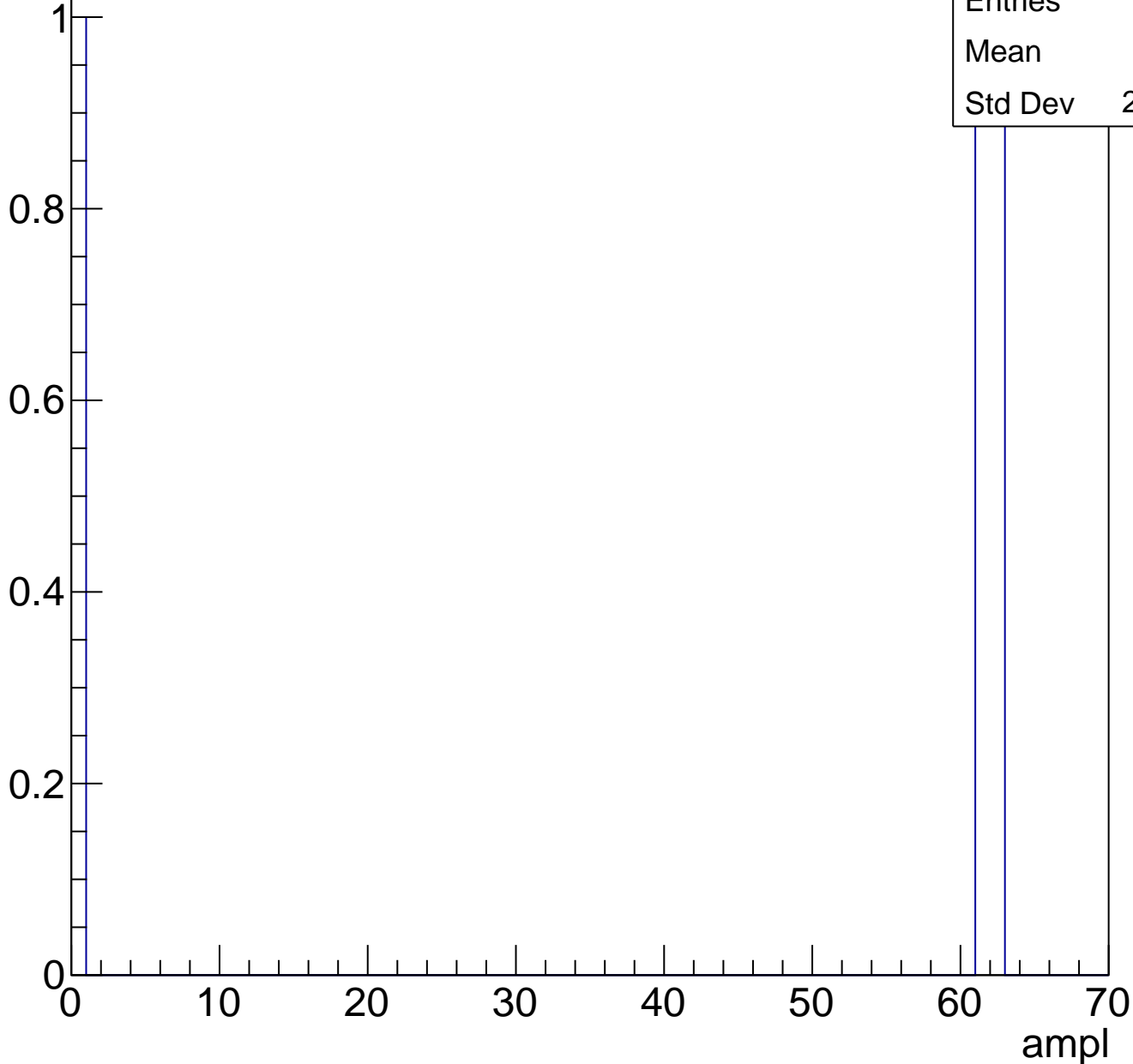




# B1L102S, U3-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch21, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	26.53
Std Dev	4.522

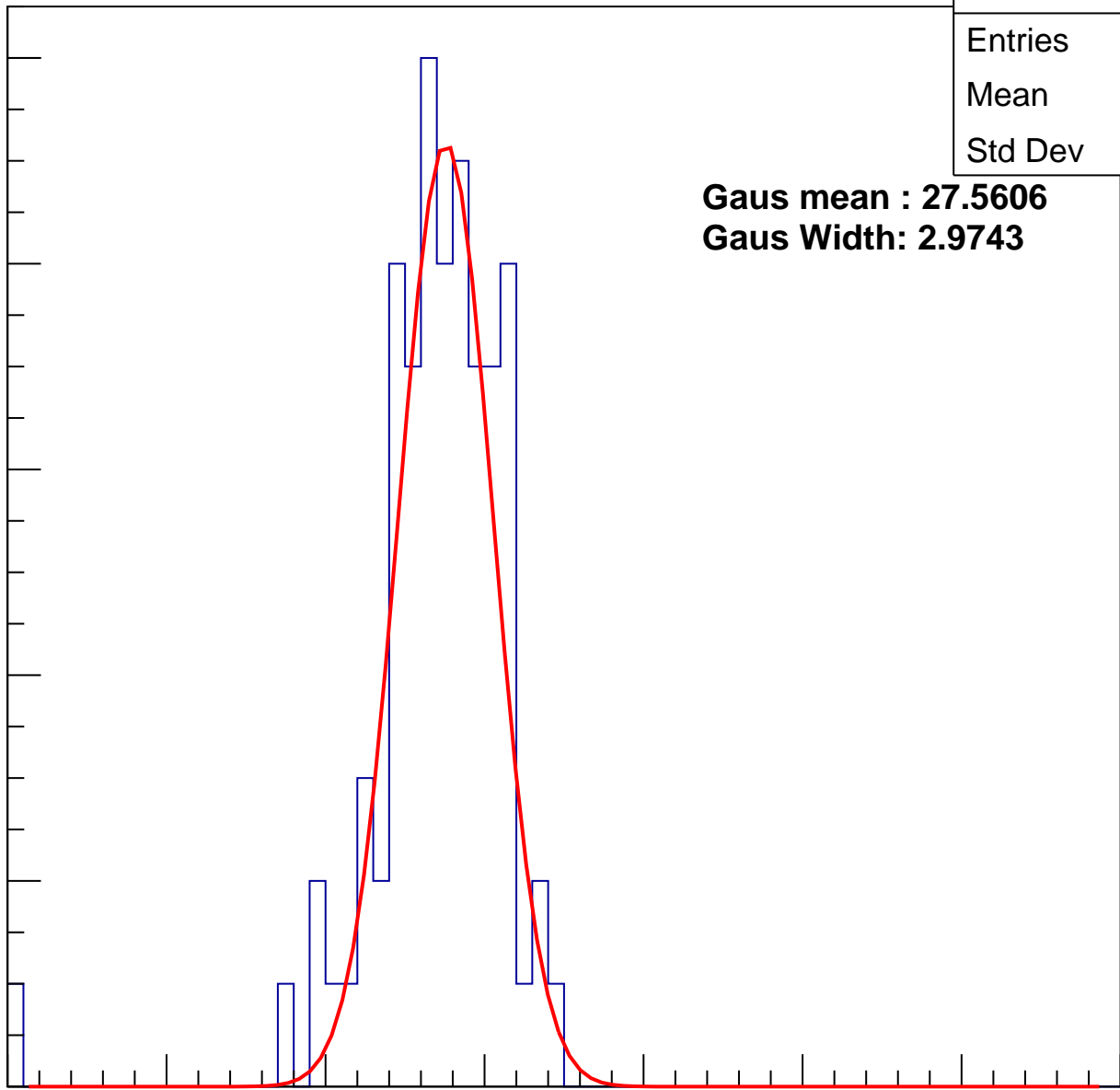
**Gaus mean : 27.5606**

**Gaus Width: 2.9743**

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U3-ch21, adc1

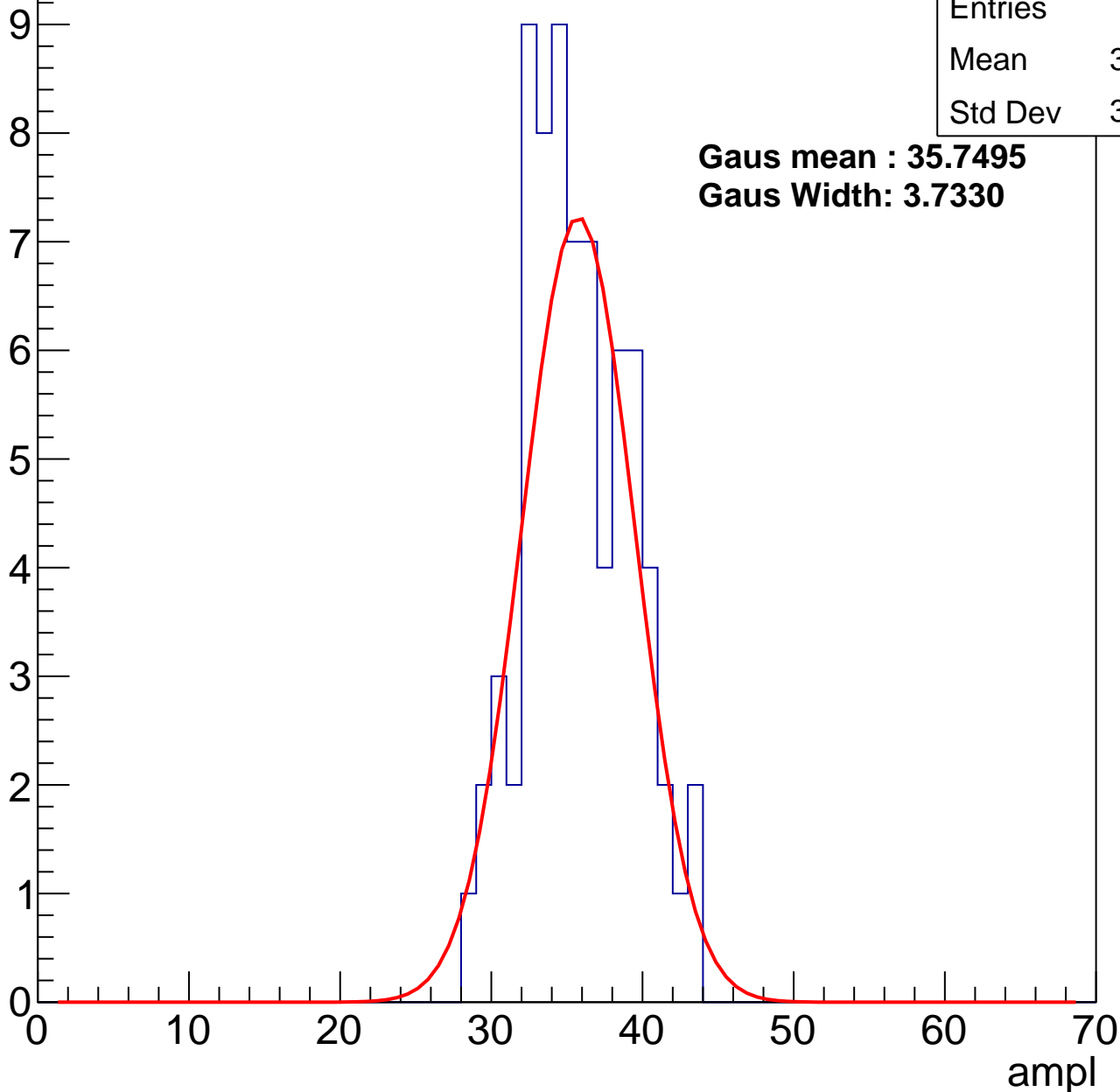
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	35.25
Std Dev	3.447

**Gaus mean : 35.7495**

**Gaus Width: 3.7330**



# B1L102S, U3-ch21, adc2

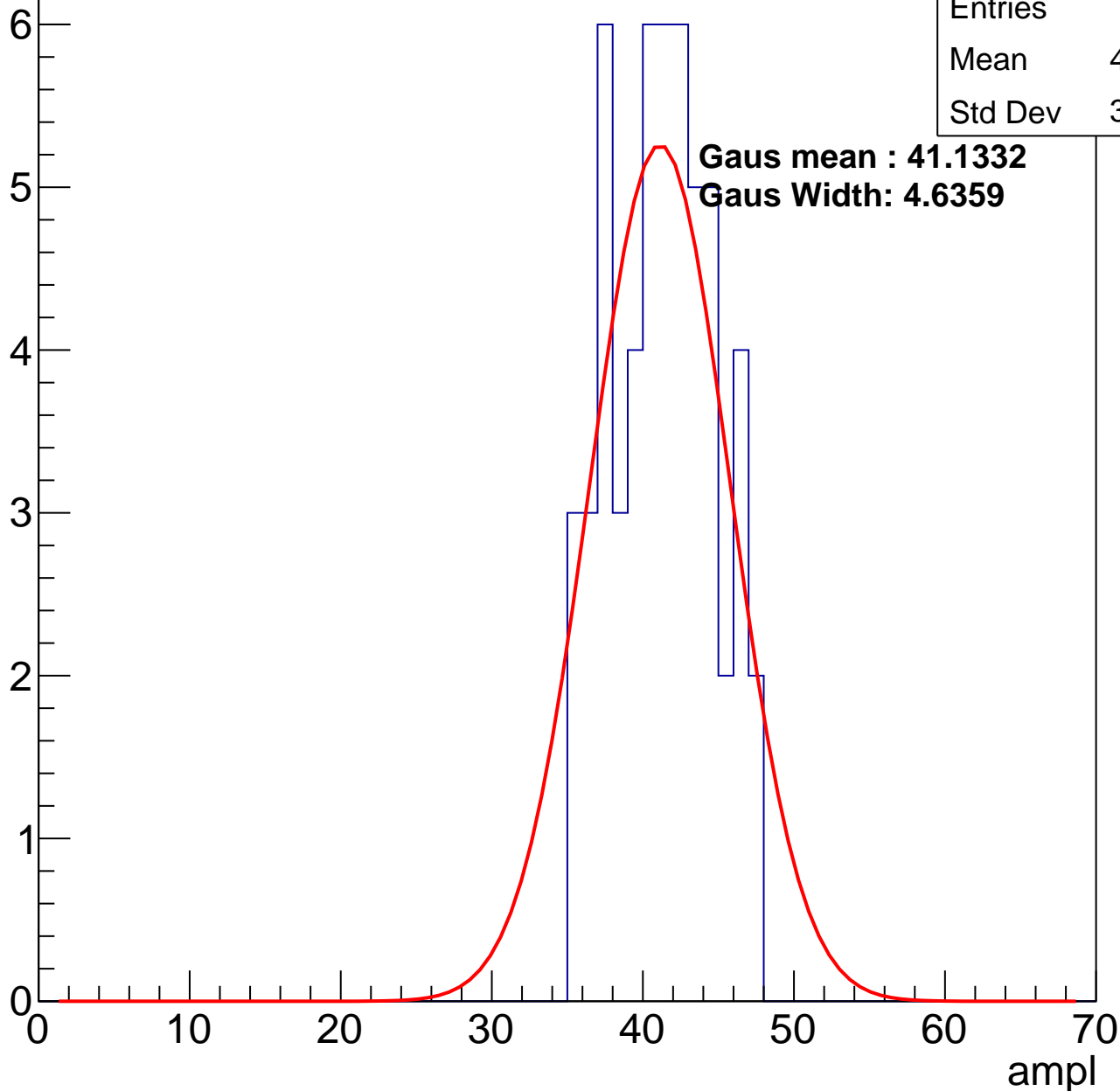
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	40.84
Std Dev	3.307

**Gaus mean : 41.1332**

**Gaus Width: 4.6359**



# B1L102S, U3-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	68
Mean	47.19
Std Dev	3.304

Entry

10

8

6

4

2

0

0

10

20

30

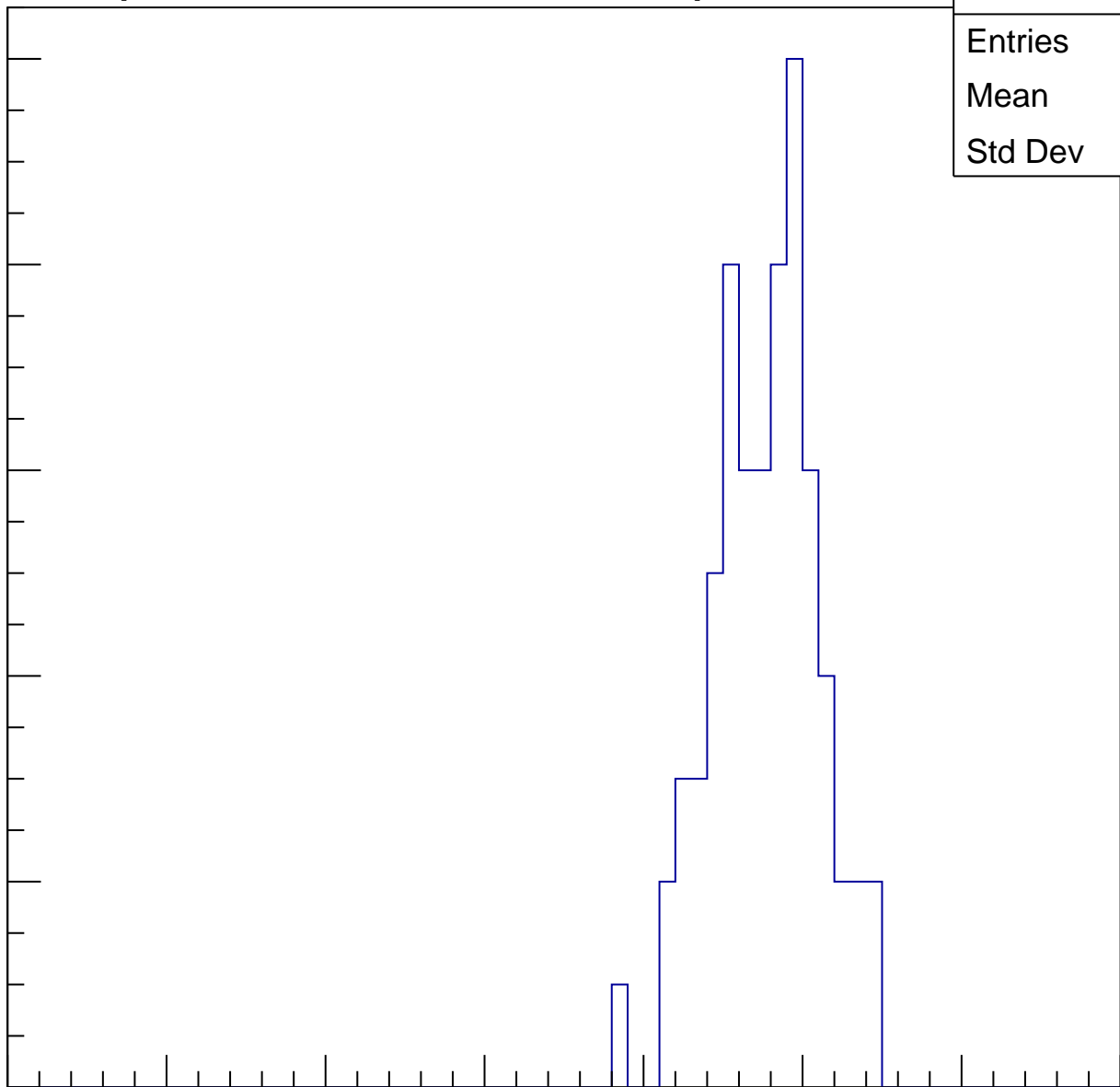
40

50

60

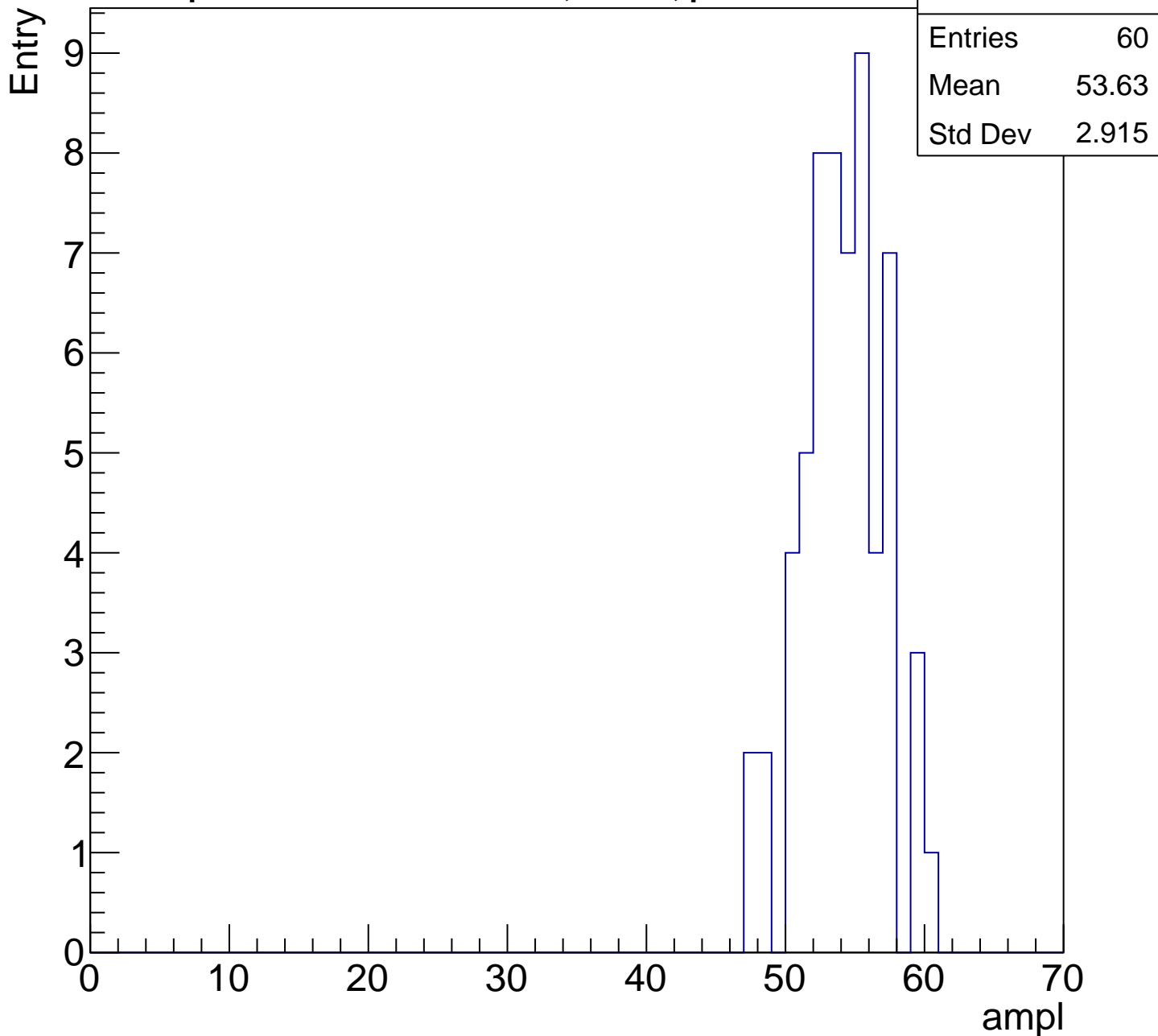
70

ampl



# B1L102S, U3-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

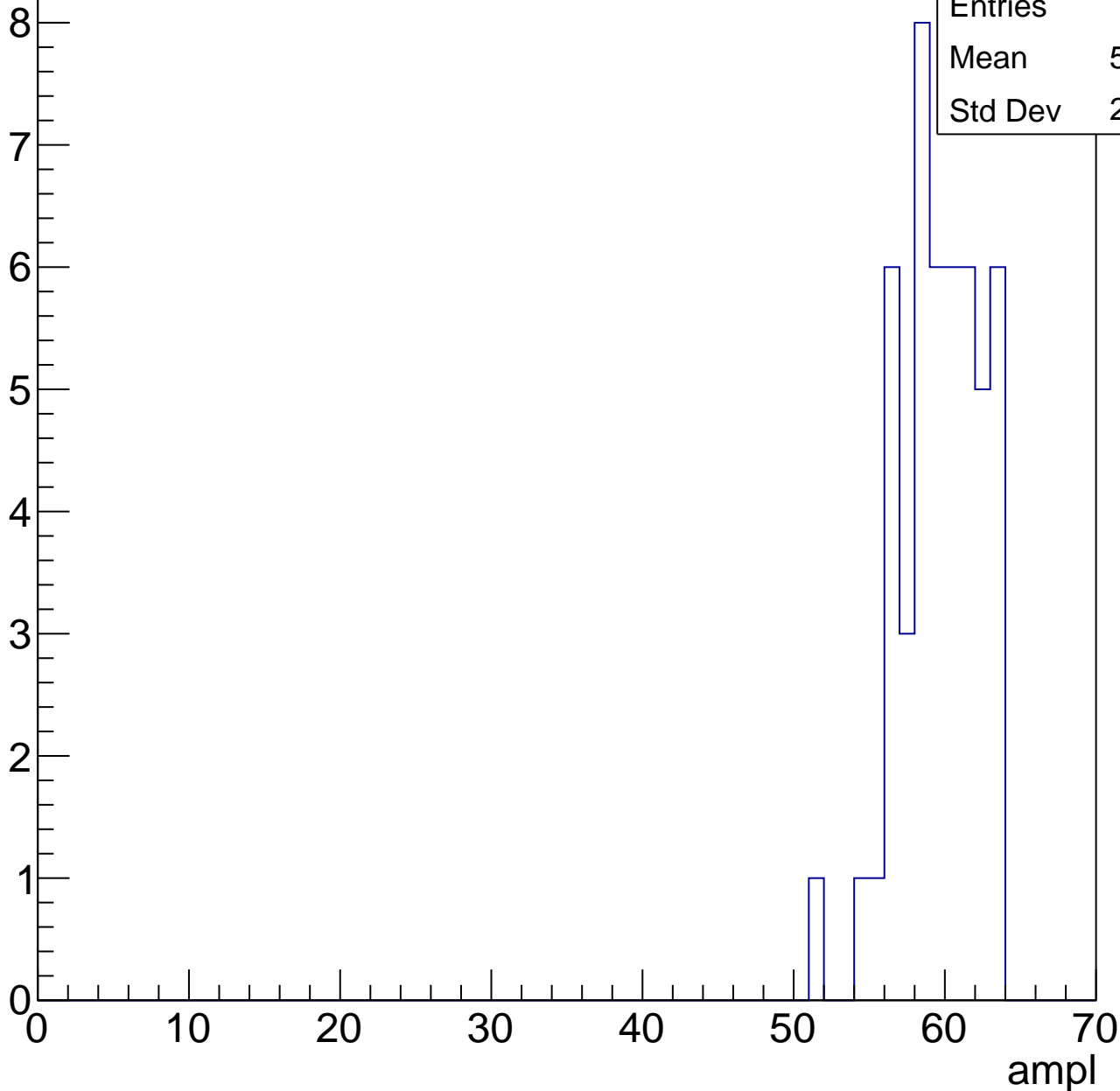


# B1L102S, U3-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

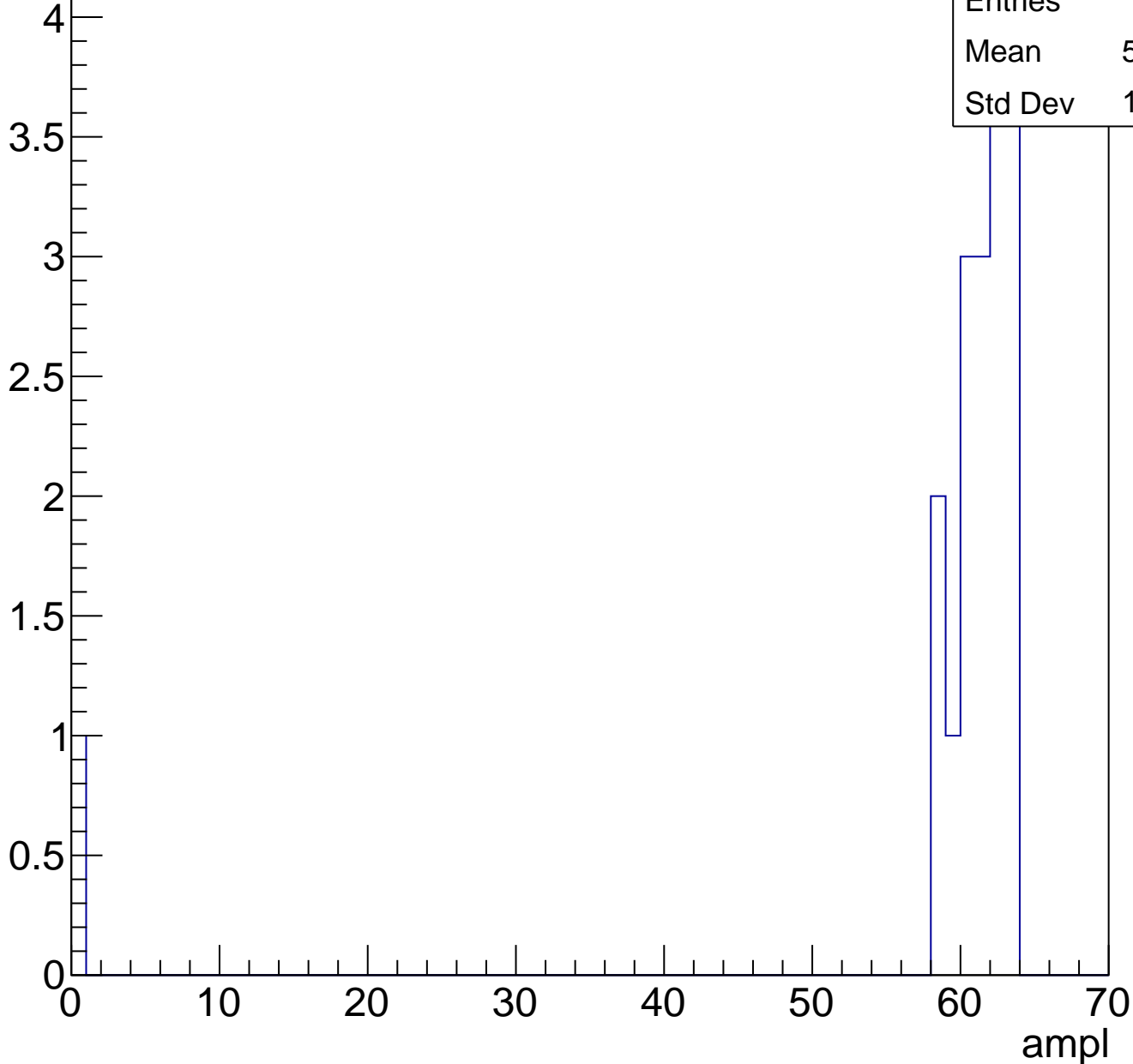
Entries	49
Mean	59.16
Std Dev	2.668



# B1L102S, U3-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

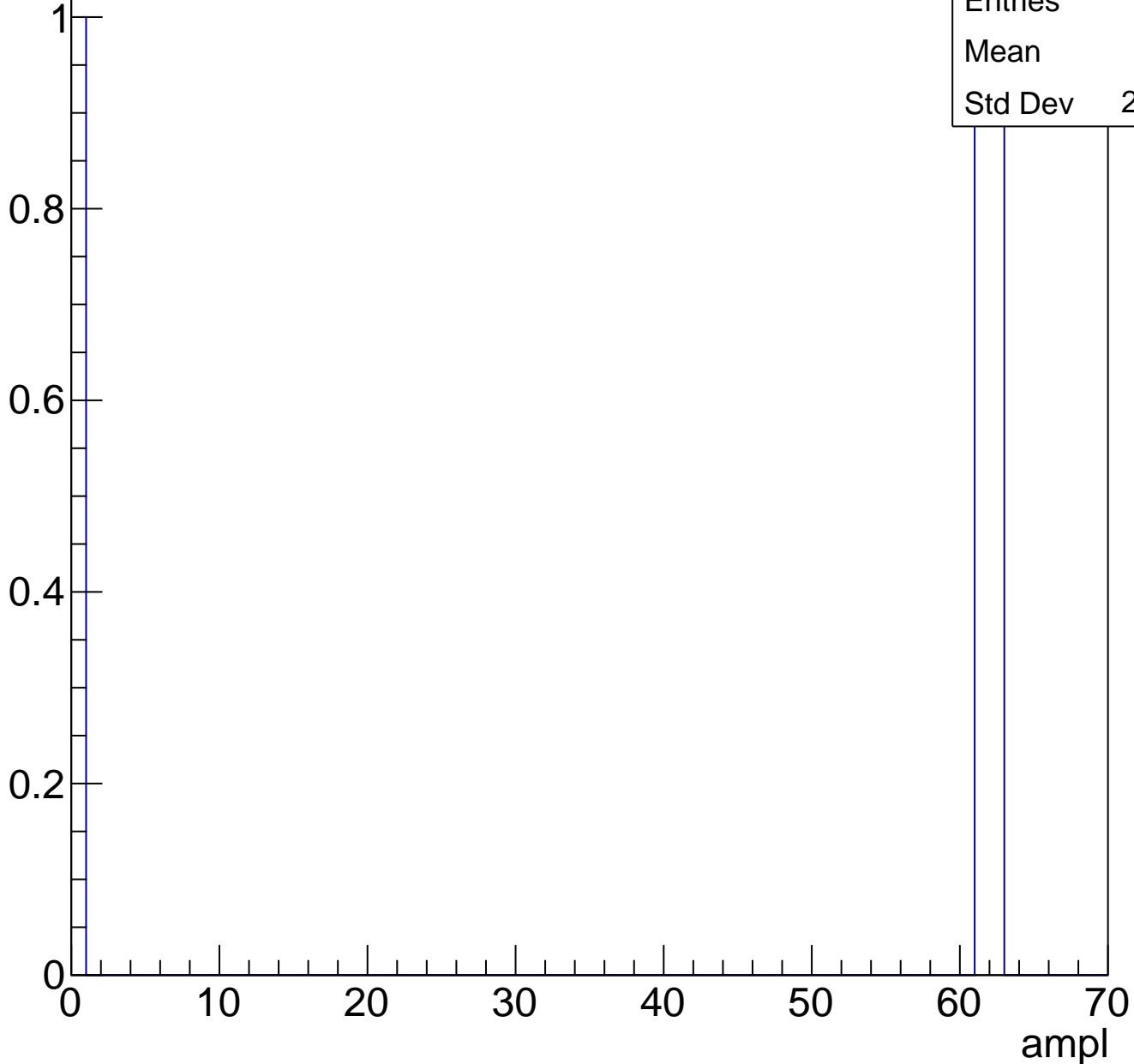




# B1L102S, U3-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch22, adc0

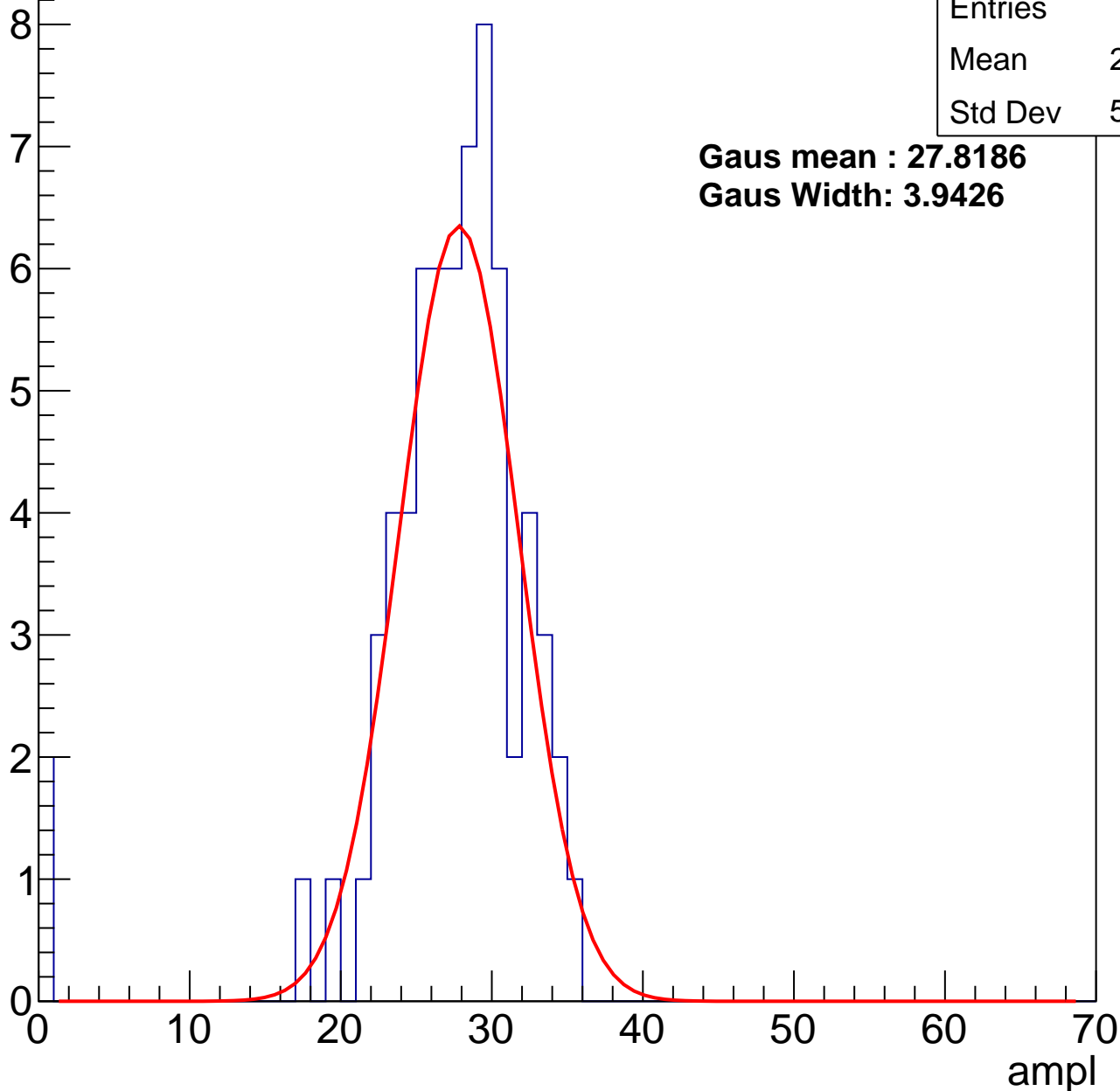
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	26.55
Std Dev	5.916

**Gaus mean : 27.8186**

**Gaus Width: 3.9426**



# B1L102S, U3-ch22, adc1

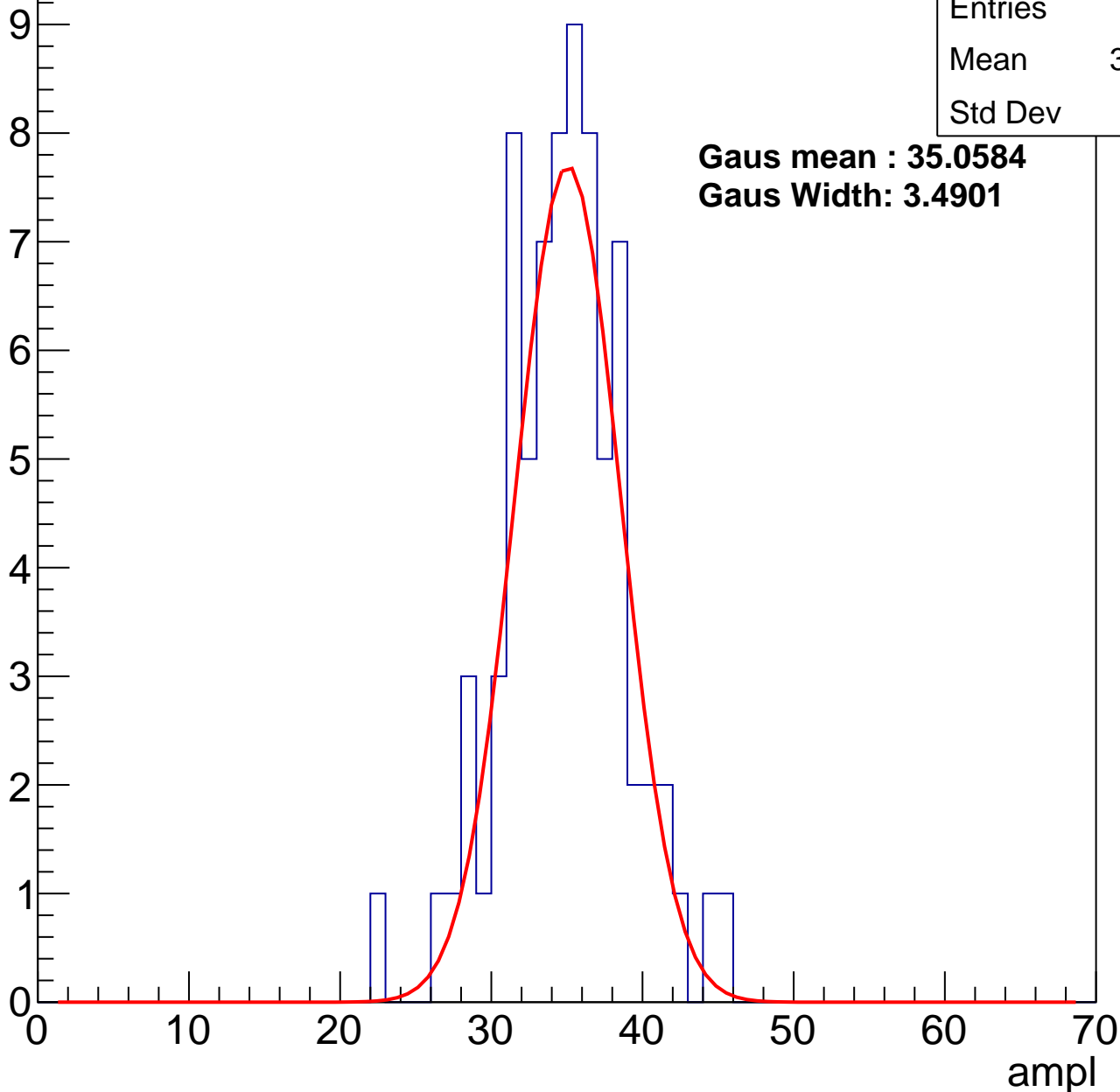
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	34.39
Std Dev	4.02

**Gaus mean : 35.0584**

**Gaus Width: 3.4901**



# B1L102S, U3-ch22, adc2

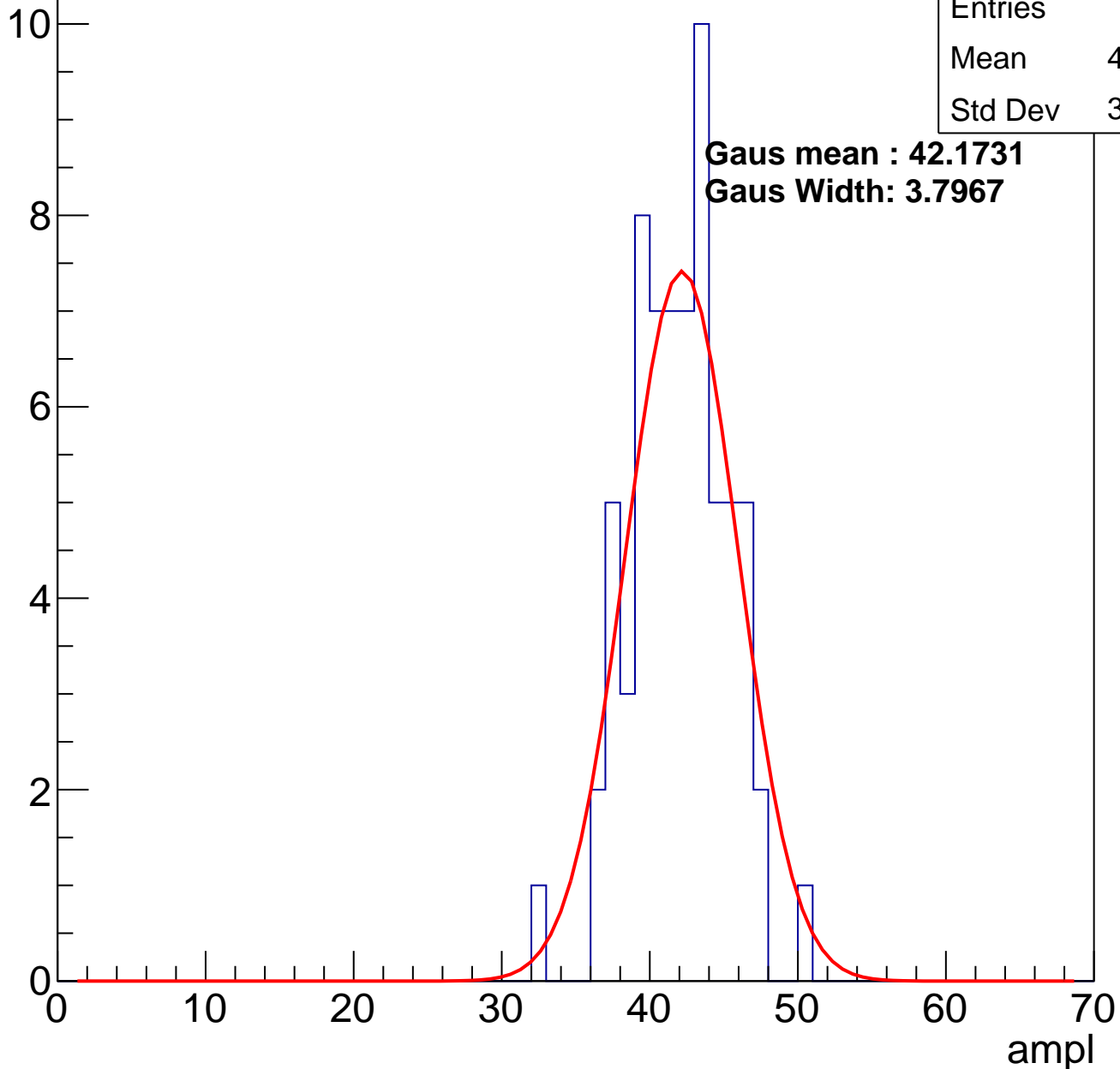
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	68
Mean	41.54
Std Dev	3.224

**Gaus mean : 42.1731**

**Gaus Width: 3.7967**

Entry

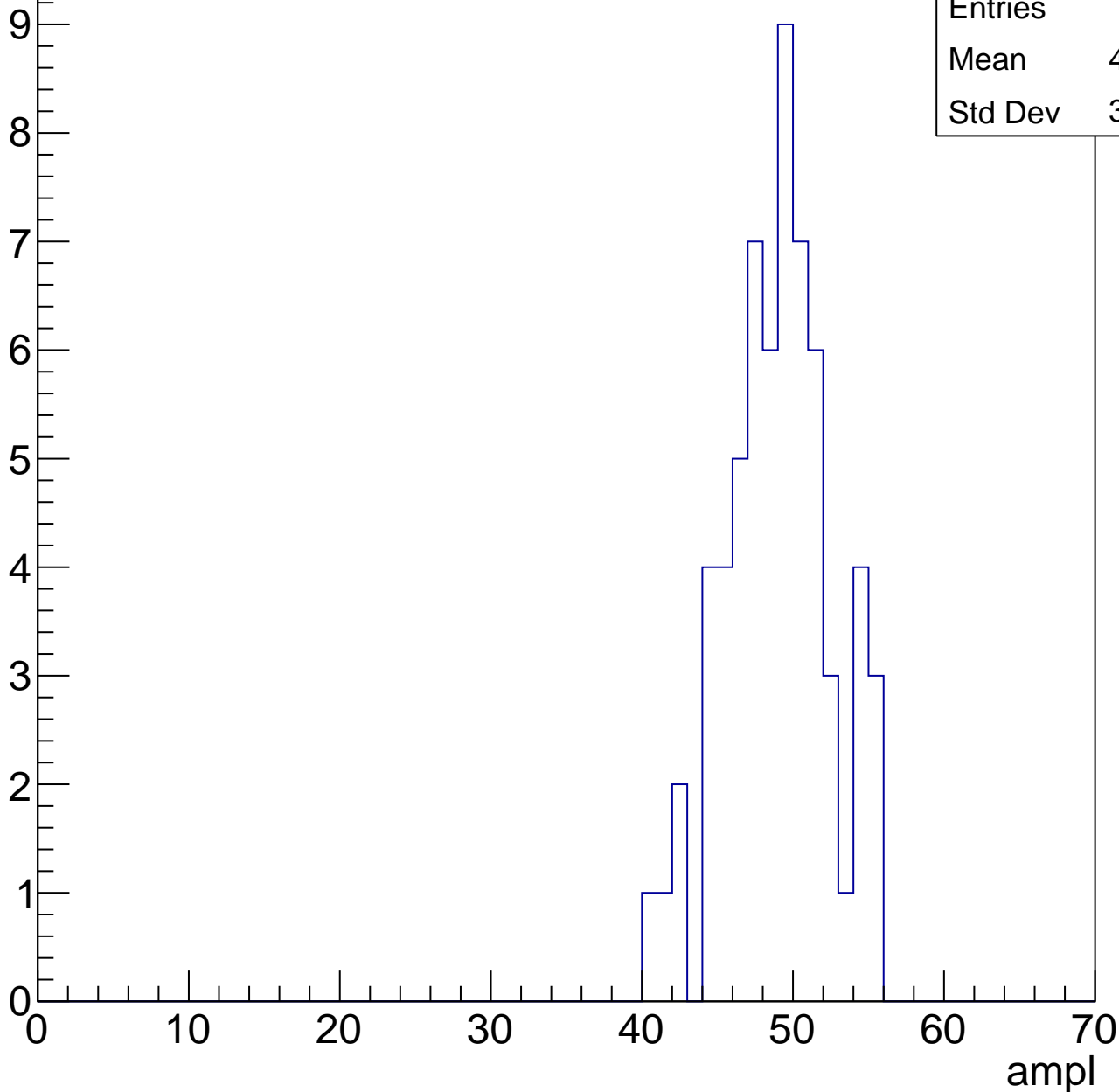


# B1L102S, U3-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	48.49
Std Dev	3.454

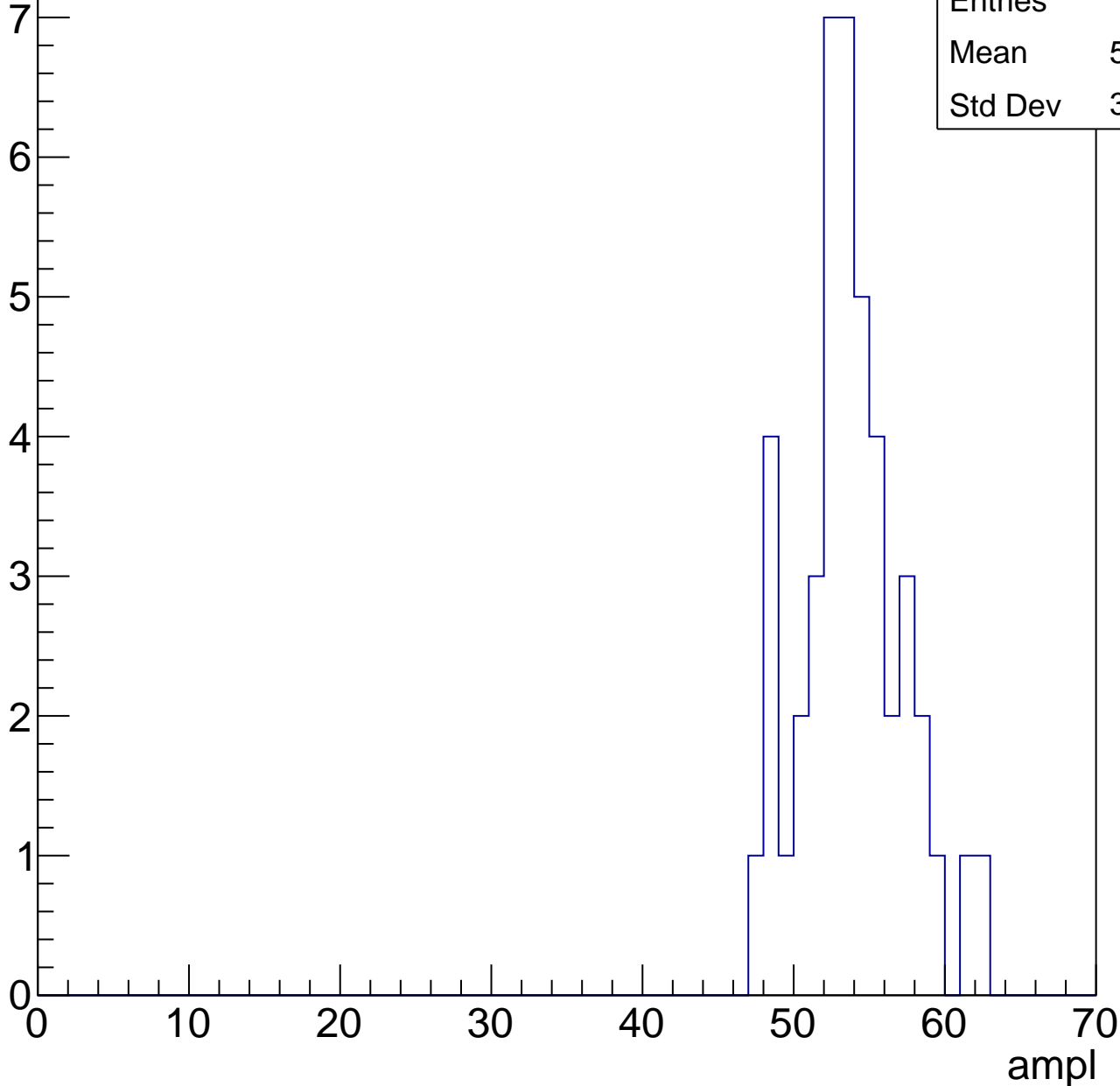


# B1L102S, U3-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	44
Mean	53.34
Std Dev	3.377

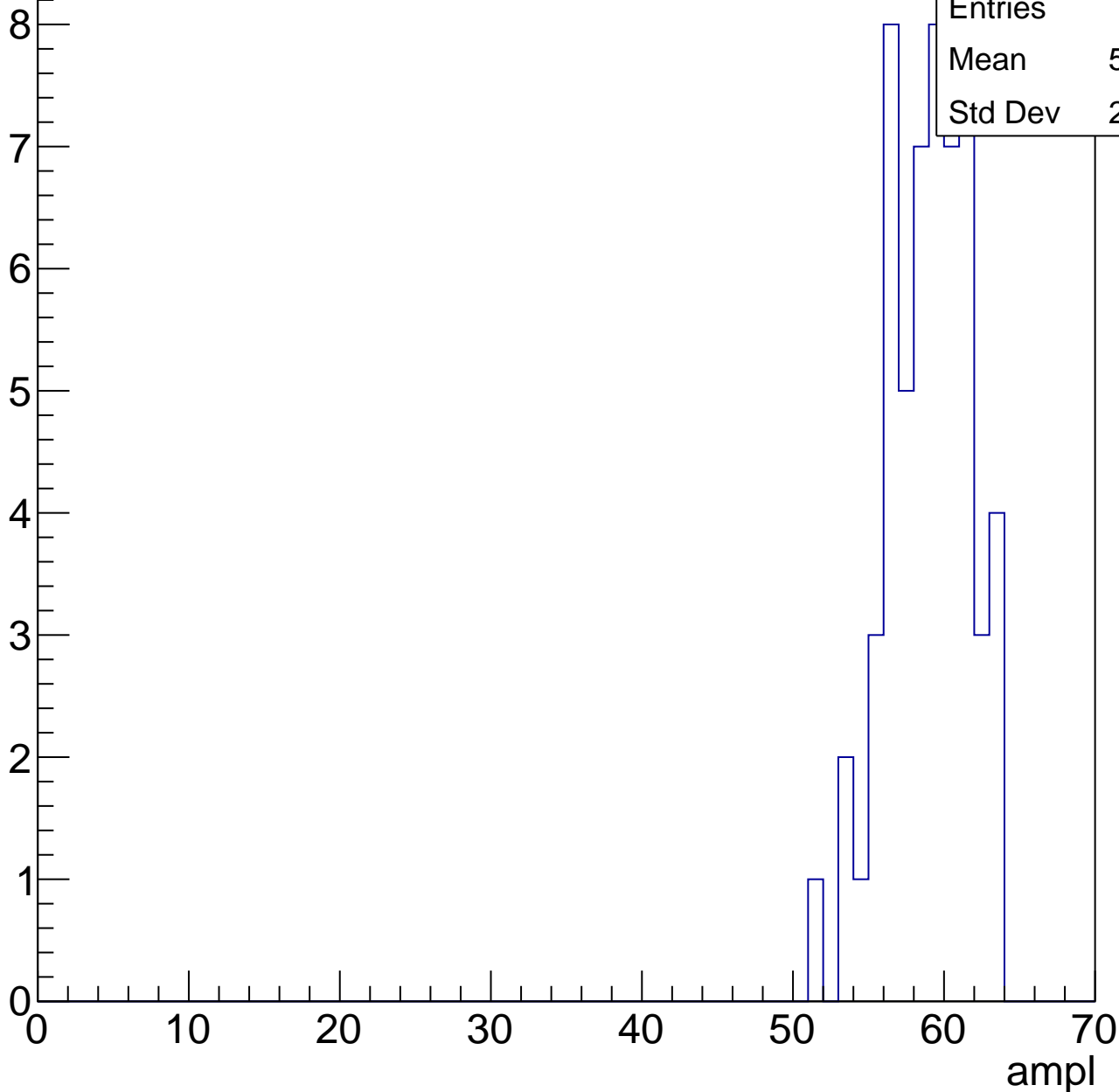


# B1L102S, U3-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	58.47
Std Dev	2.722

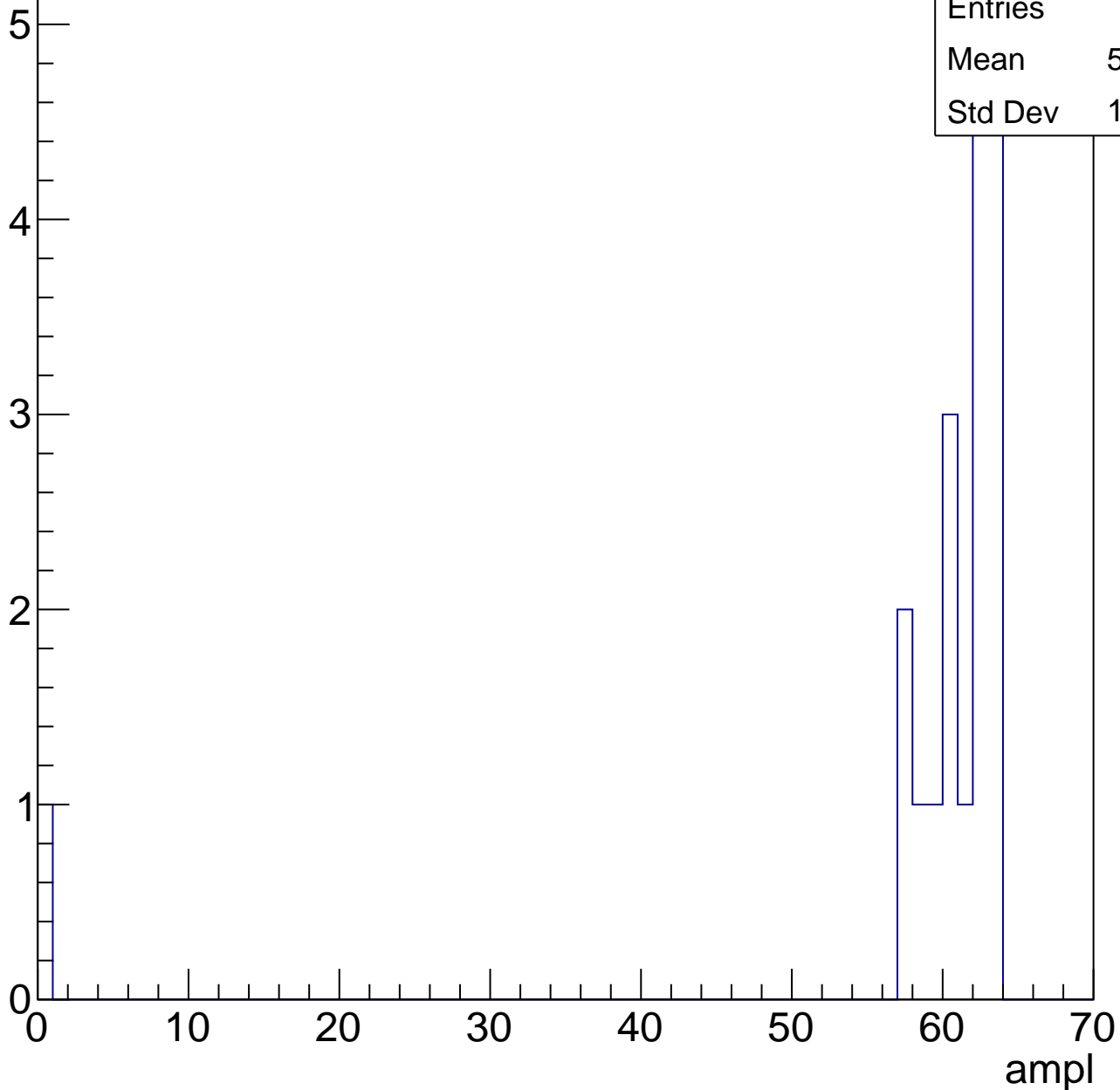


# B1L102S, U3-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	19
Mean	57.74
Std Dev	13.75

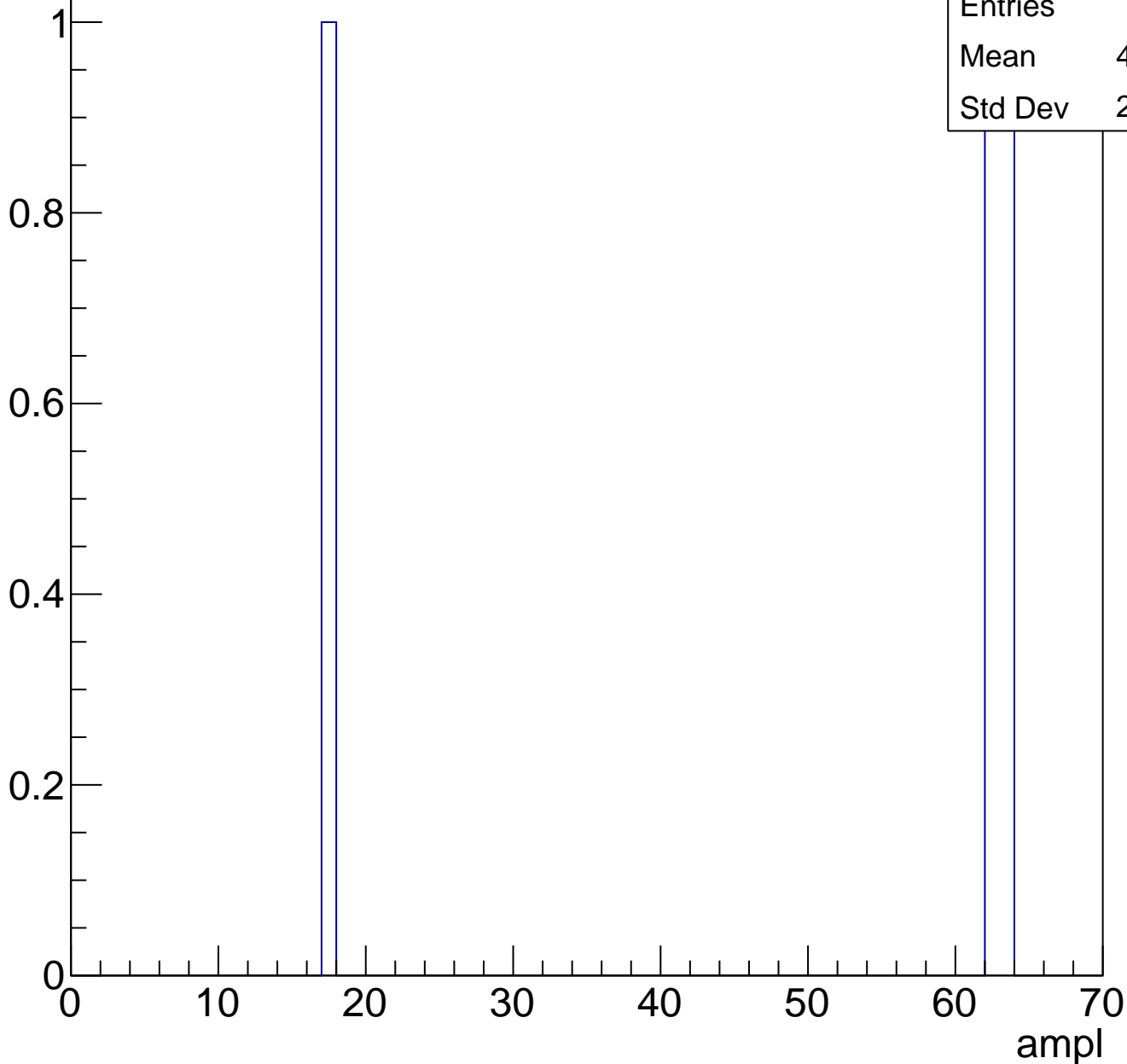




# B1L102S, U3-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch23, adc0

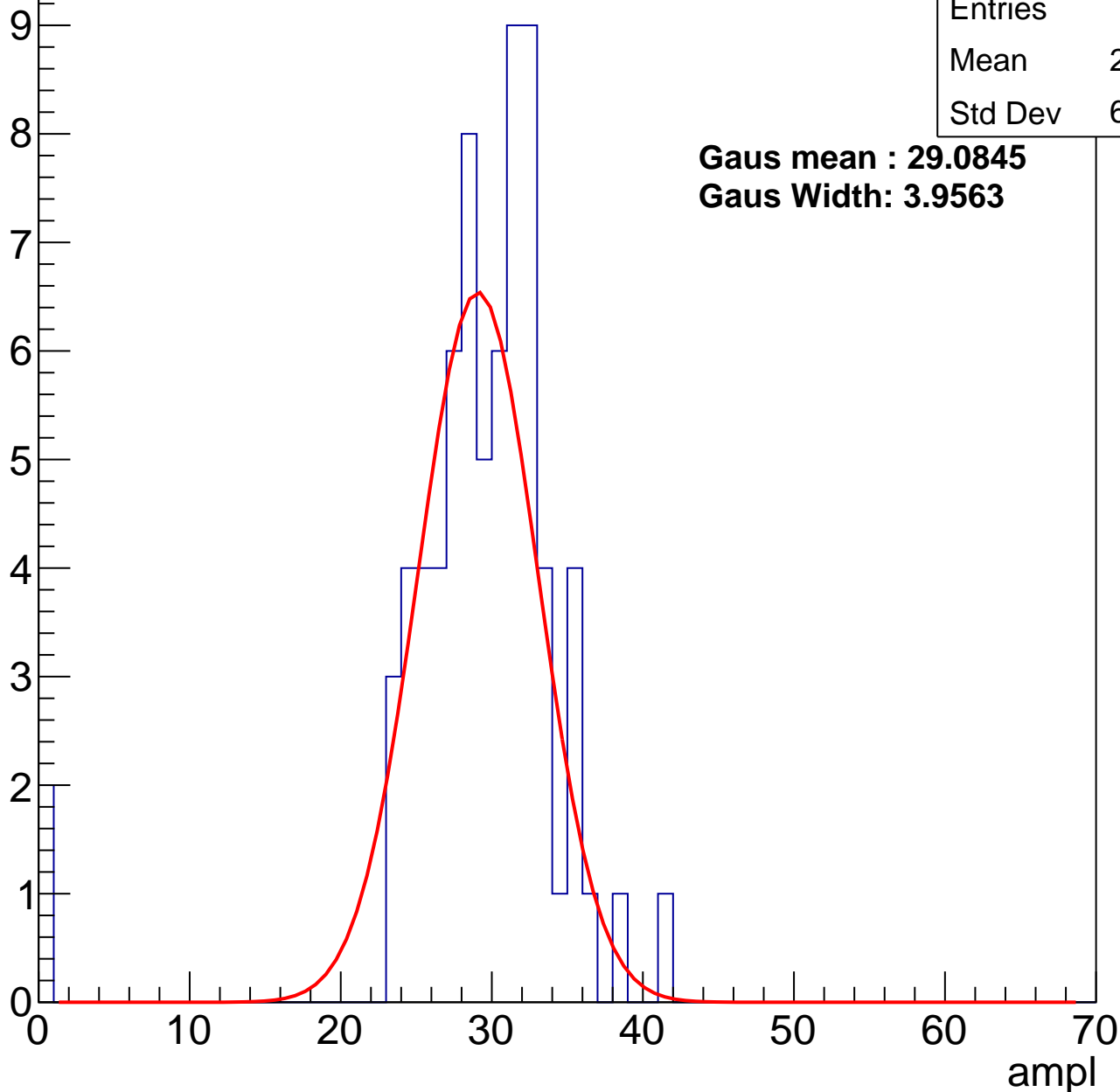
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	28.72
Std Dev	6.063

**Gaus mean : 29.0845**

**Gaus Width: 3.9563**



# B1L102S, U3-ch23, adc1

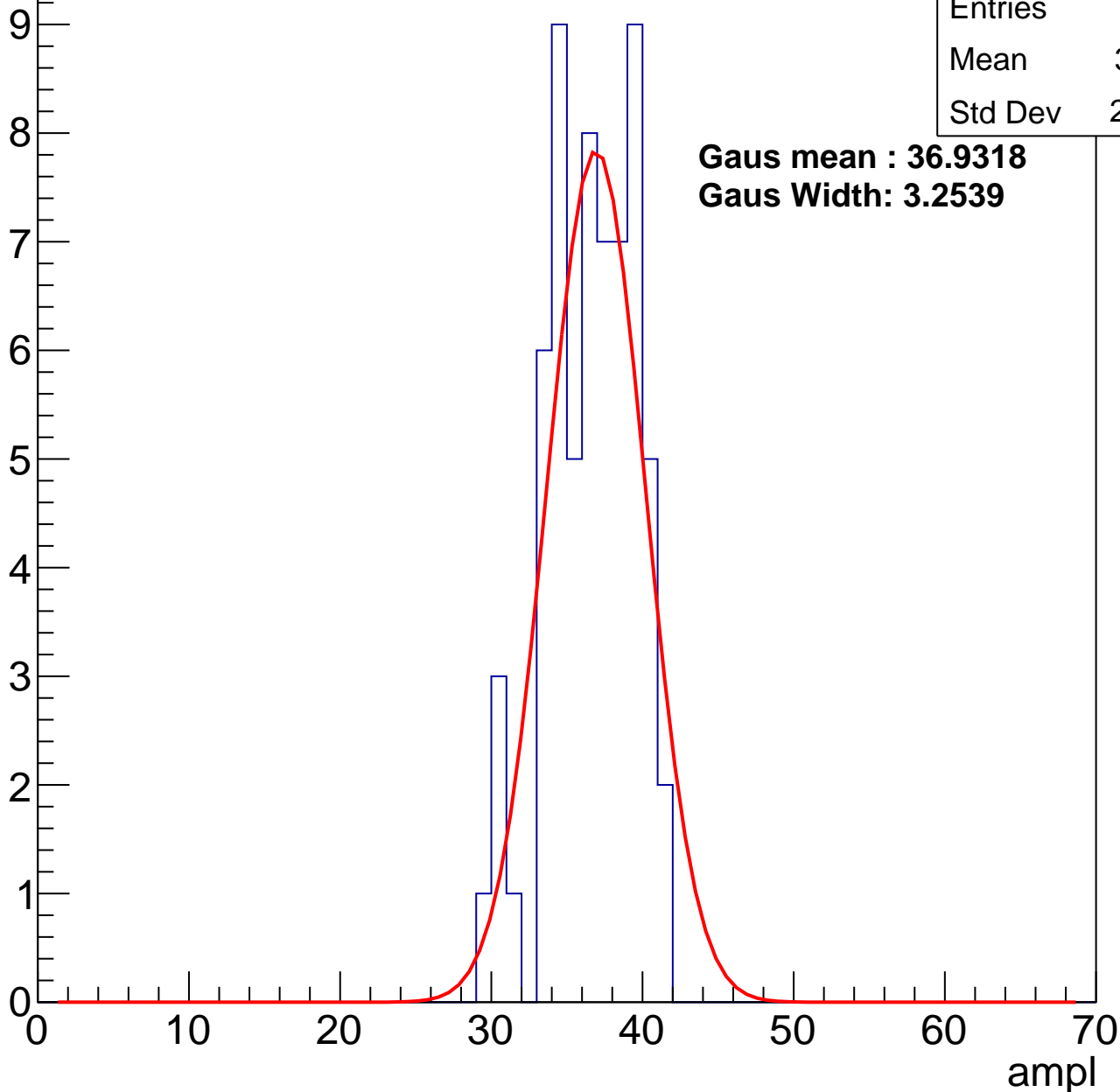
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	36.11
Std Dev	2.879

**Gaus mean : 36.9318**

**Gaus Width: 3.2539**



# B1L102S, U3-ch23, adc2

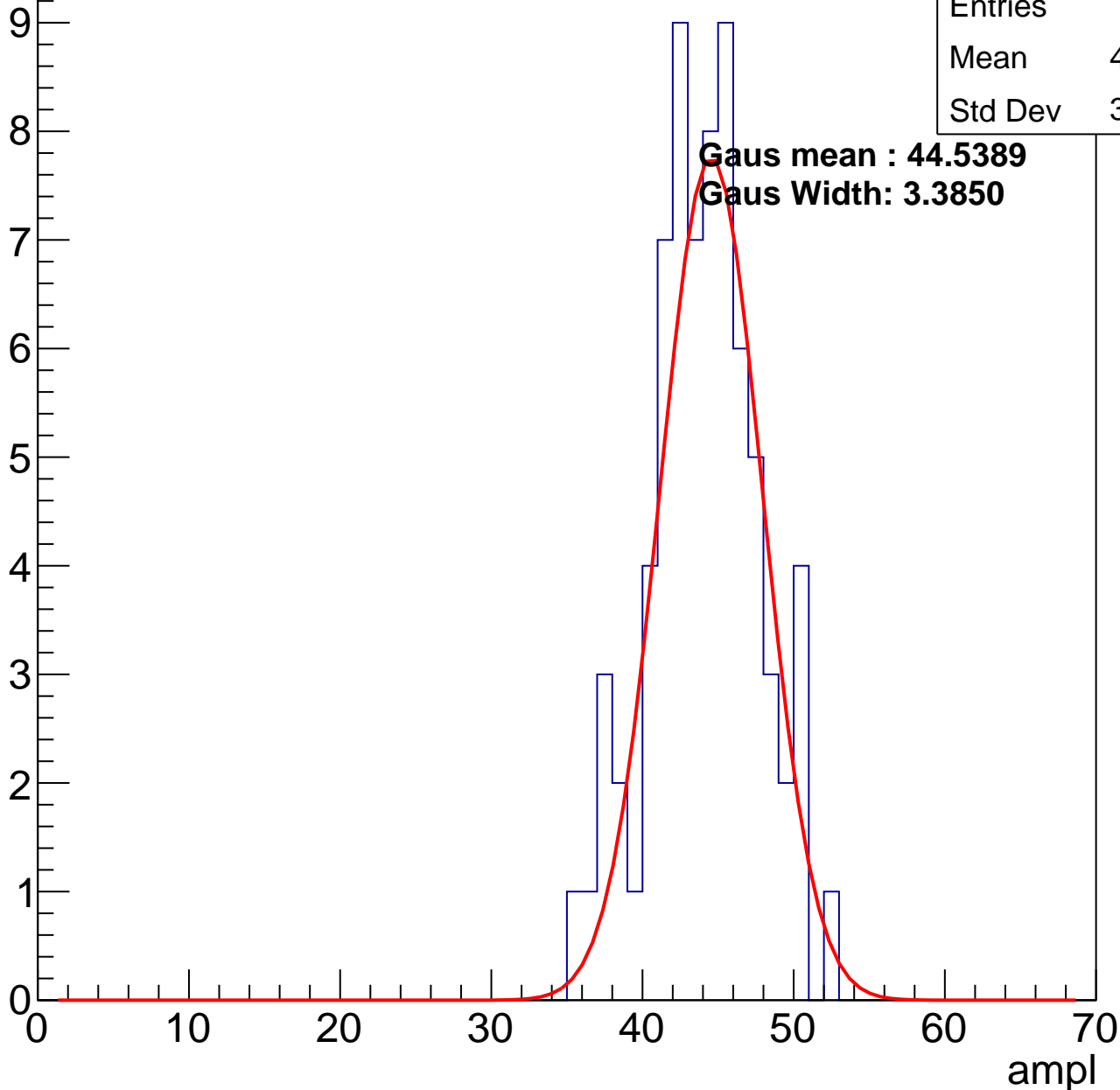
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	43.63
Std Dev	3.575

**Gaus mean : 44.5389**

**Gaus Width: 3.3850**

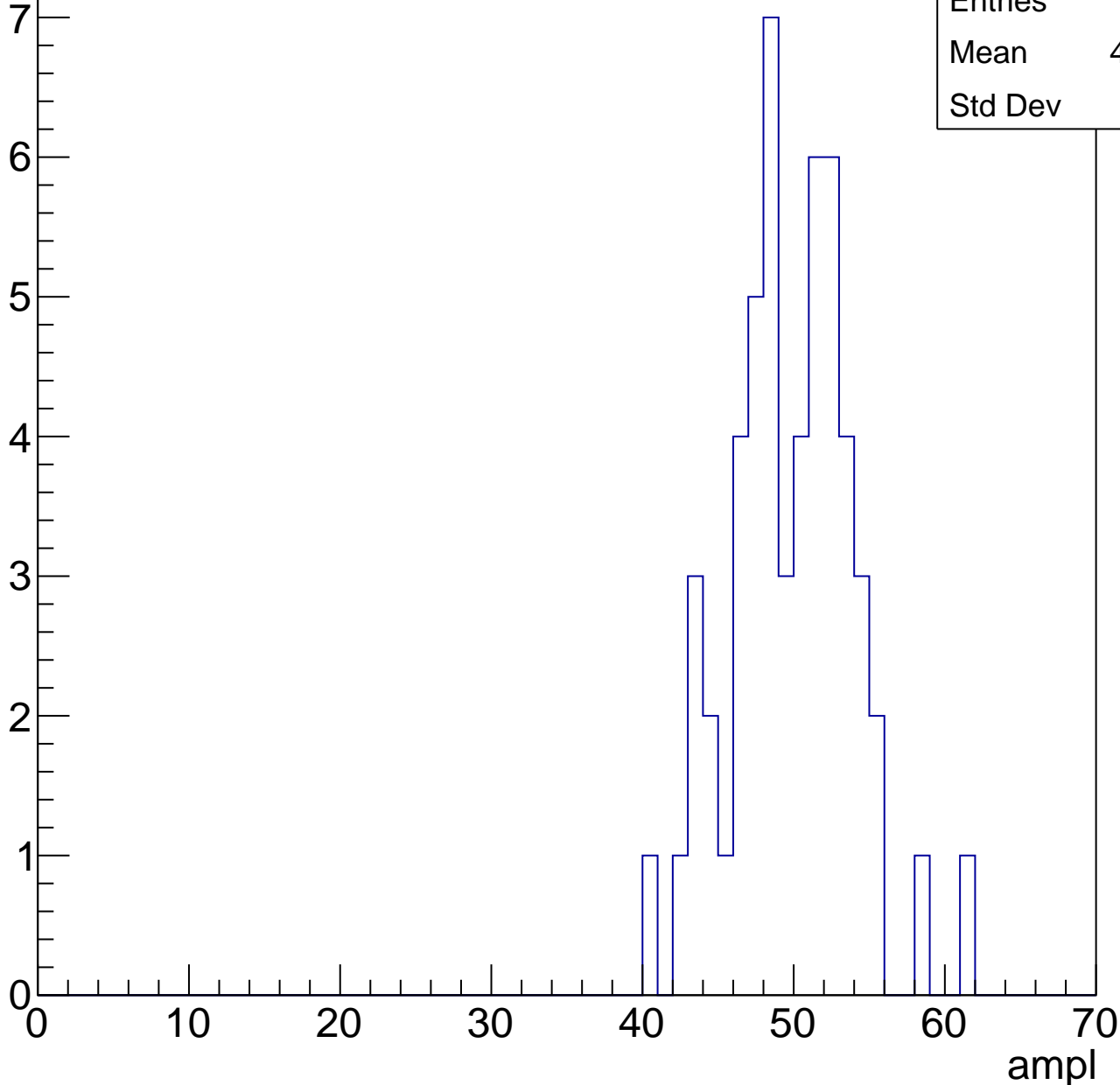


# B1L102S, U3-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

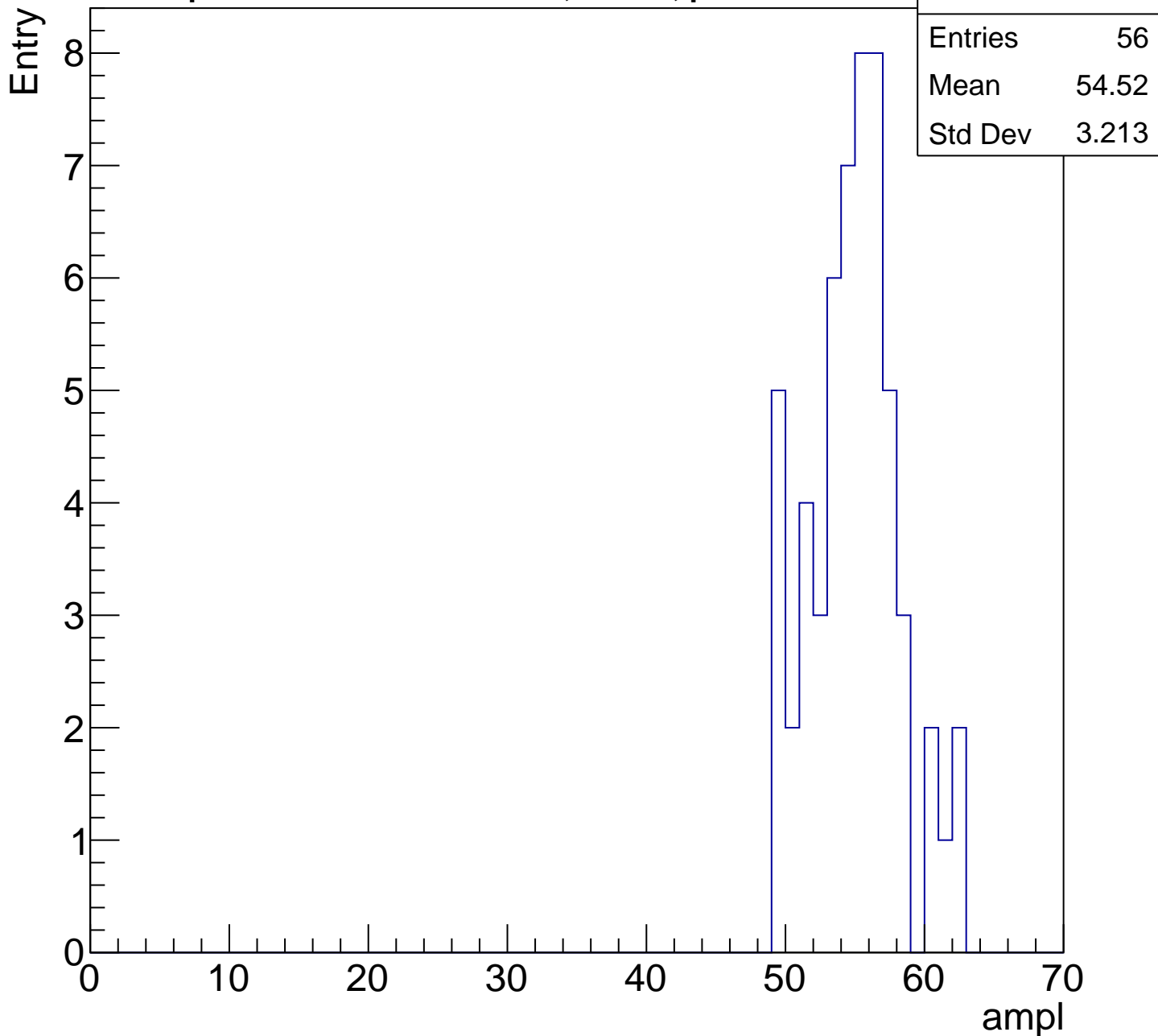
Entry

Entries	54
Mean	49.39
Std Dev	4.03



# B1L102S, U3-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

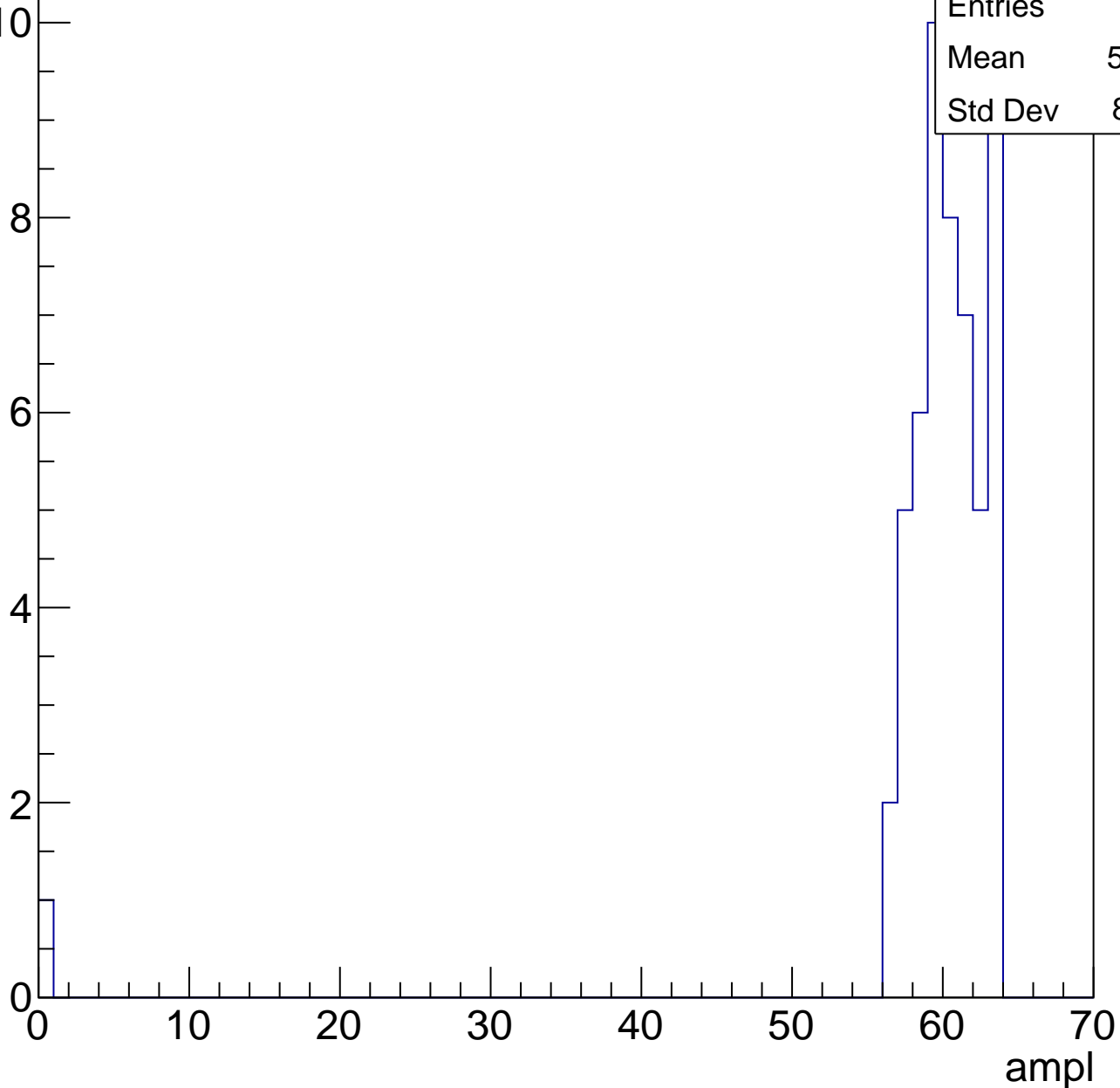


# B1L102S, U3-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	58.93
Std Dev	8.351



# B1L102S, U3-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U3-ch24, adc0

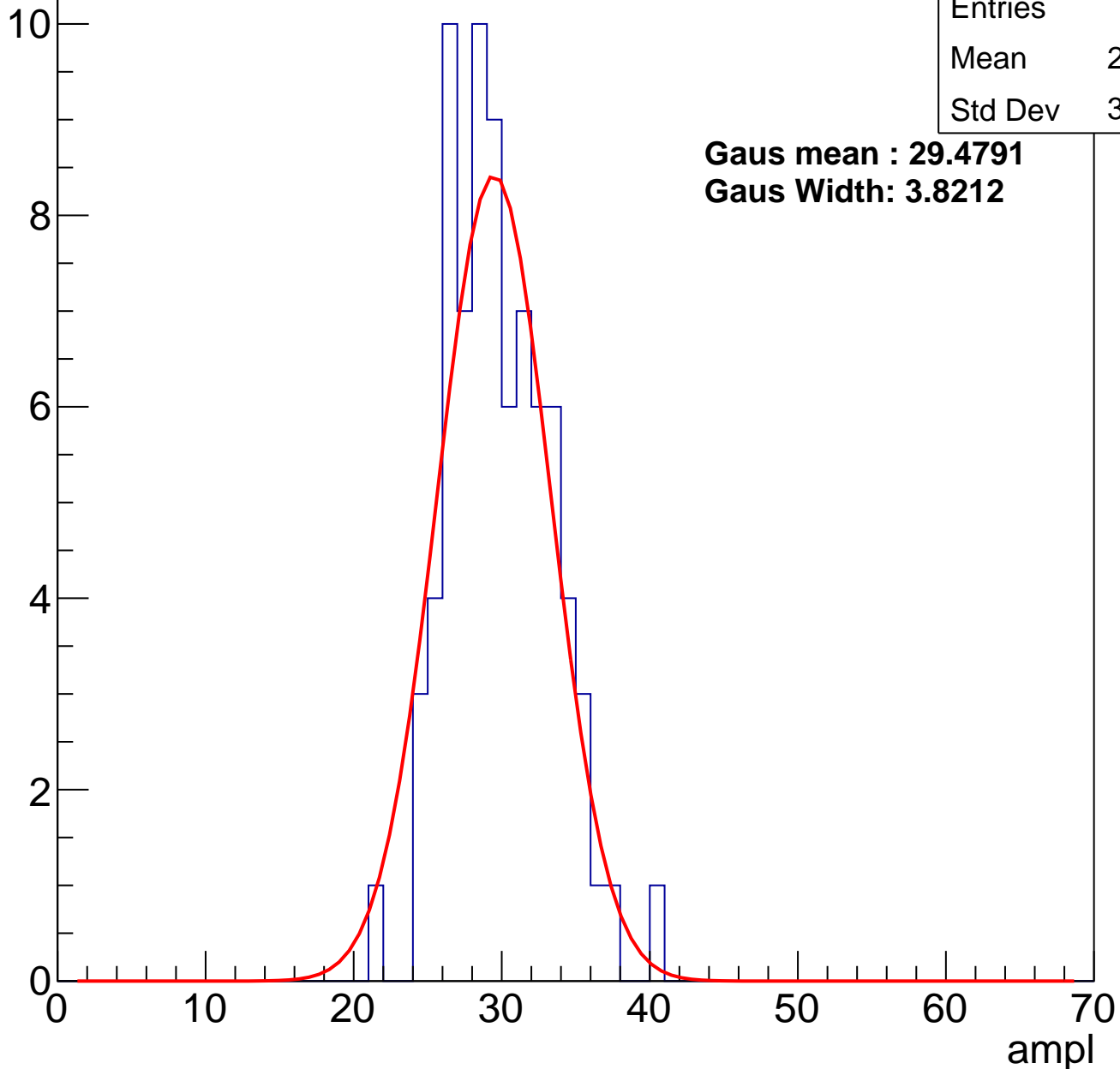
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	79
Mean	29.42
Std Dev	3.455

**Gaus mean : 29.4791**

**Gaus Width: 3.8212**

Entry



# B1L102S, U3-ch24, adc1

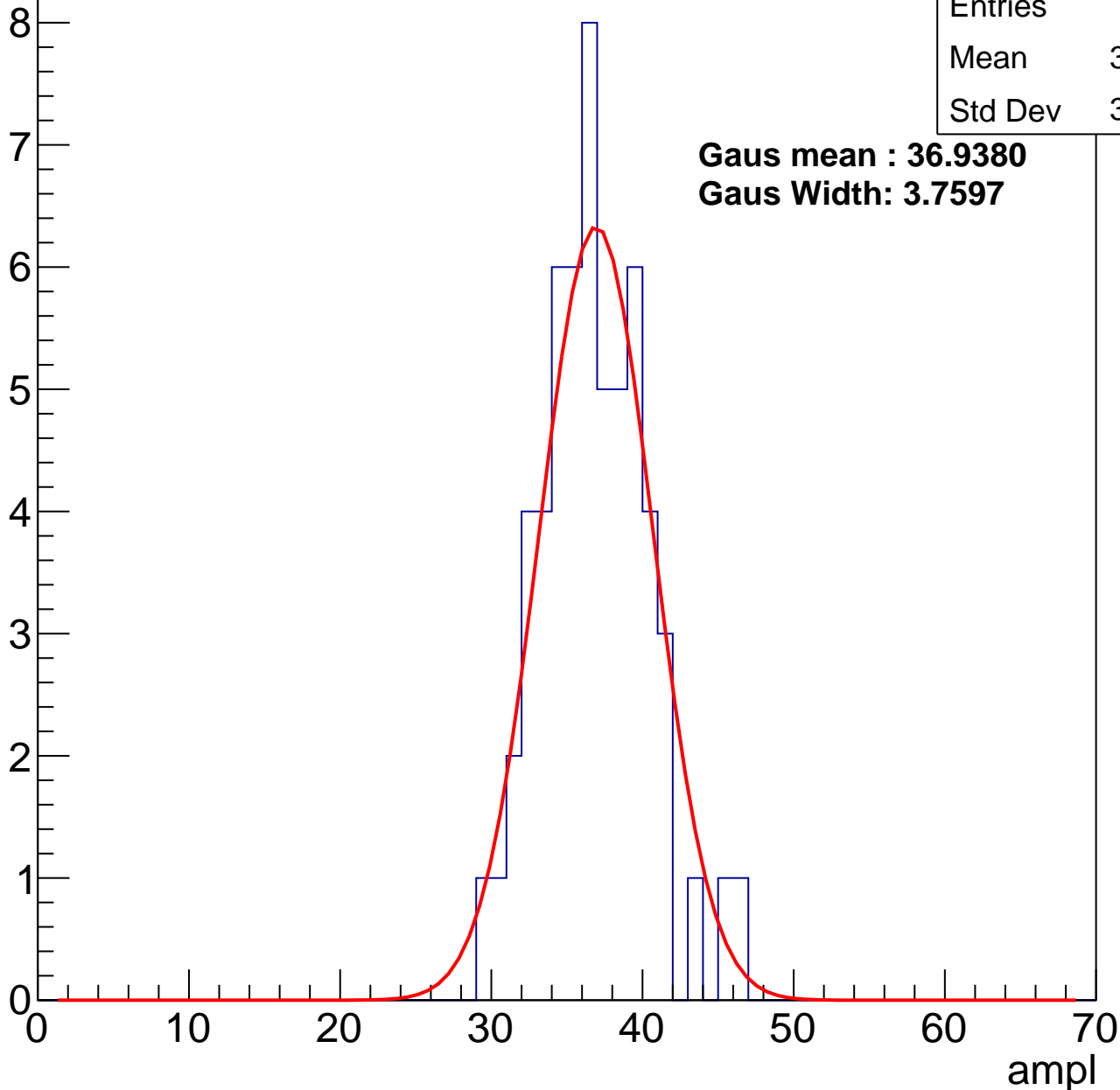
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	36.36
Std Dev	3.487

**Gaus mean : 36.9380**

**Gaus Width: 3.7597**



# B1L102S, U3-ch24, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	72
Mean	42.61
Std Dev	4.019

**Gaus mean : 43.1439**

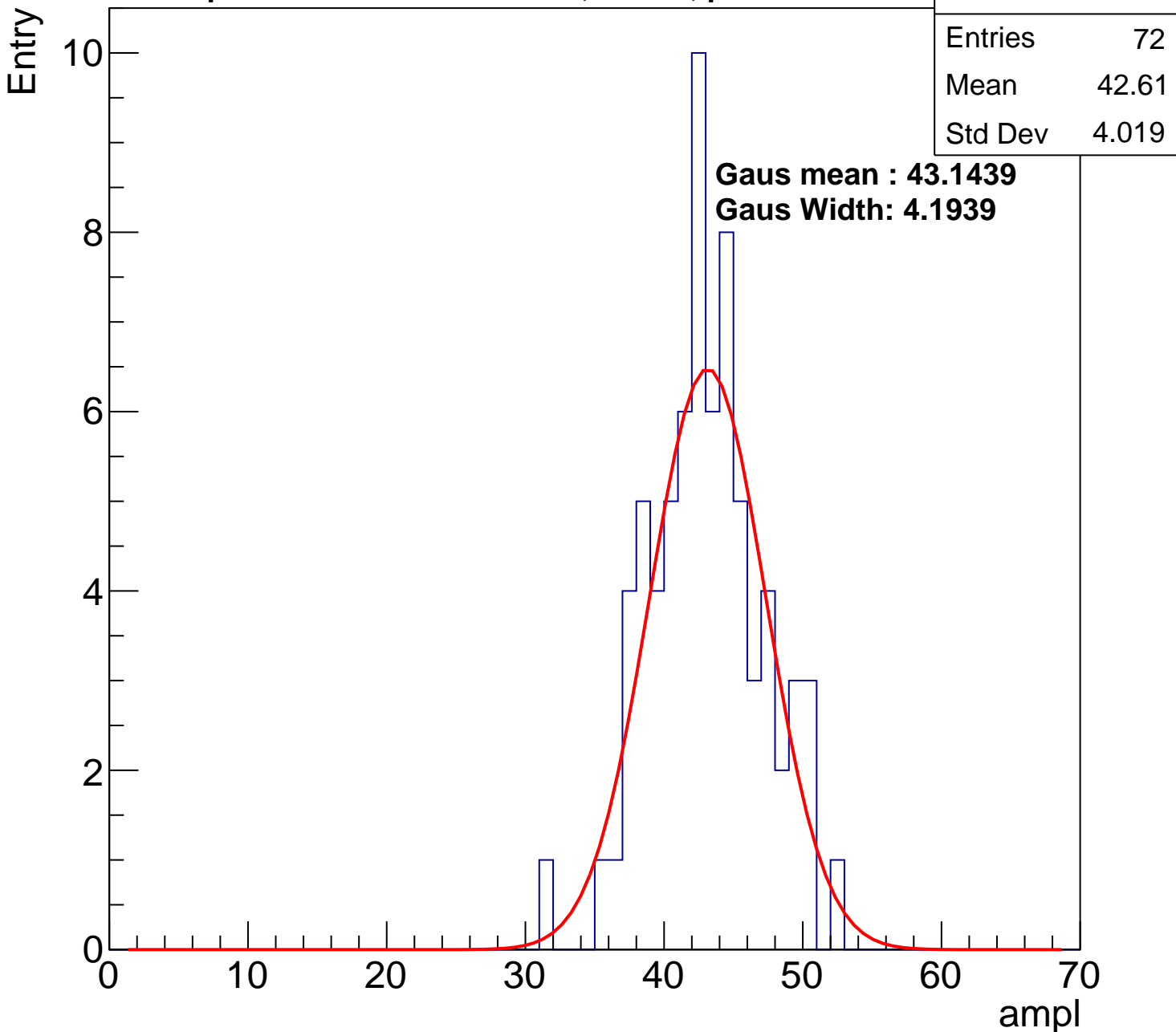
**Gaus Width: 4.1939**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

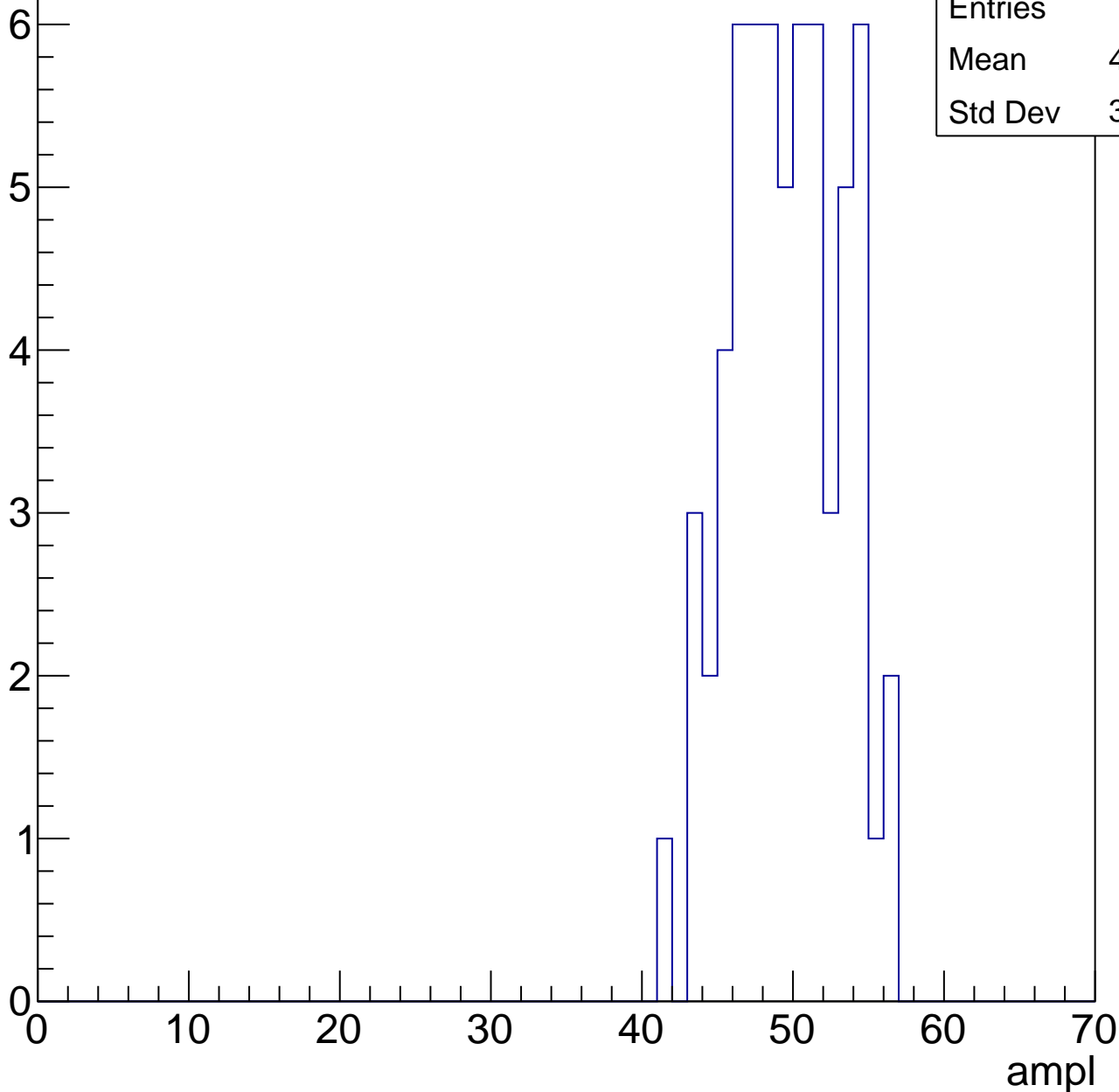


# B1L102S, U3-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	49.15
Std Dev	3.569

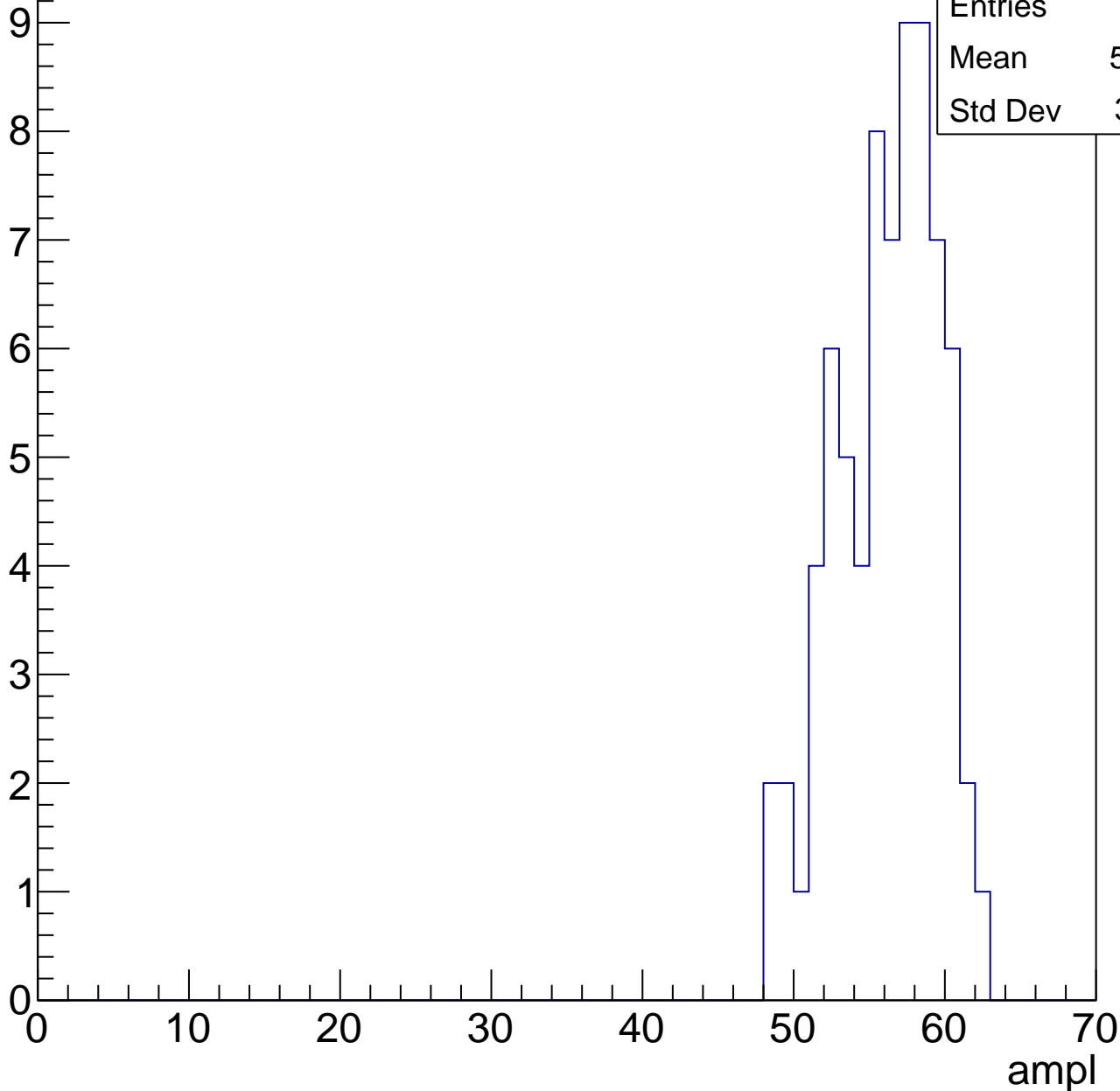


# B1L102S, U3-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	55.68
Std Dev	3.331



# B1L102S, U3-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

7

6

5

4

3

2

1

0

Entries

27

Mean

60.59

Std Dev

2.095

0

10

20

30

40

50

60

70

ampl

0

1

2

3

4

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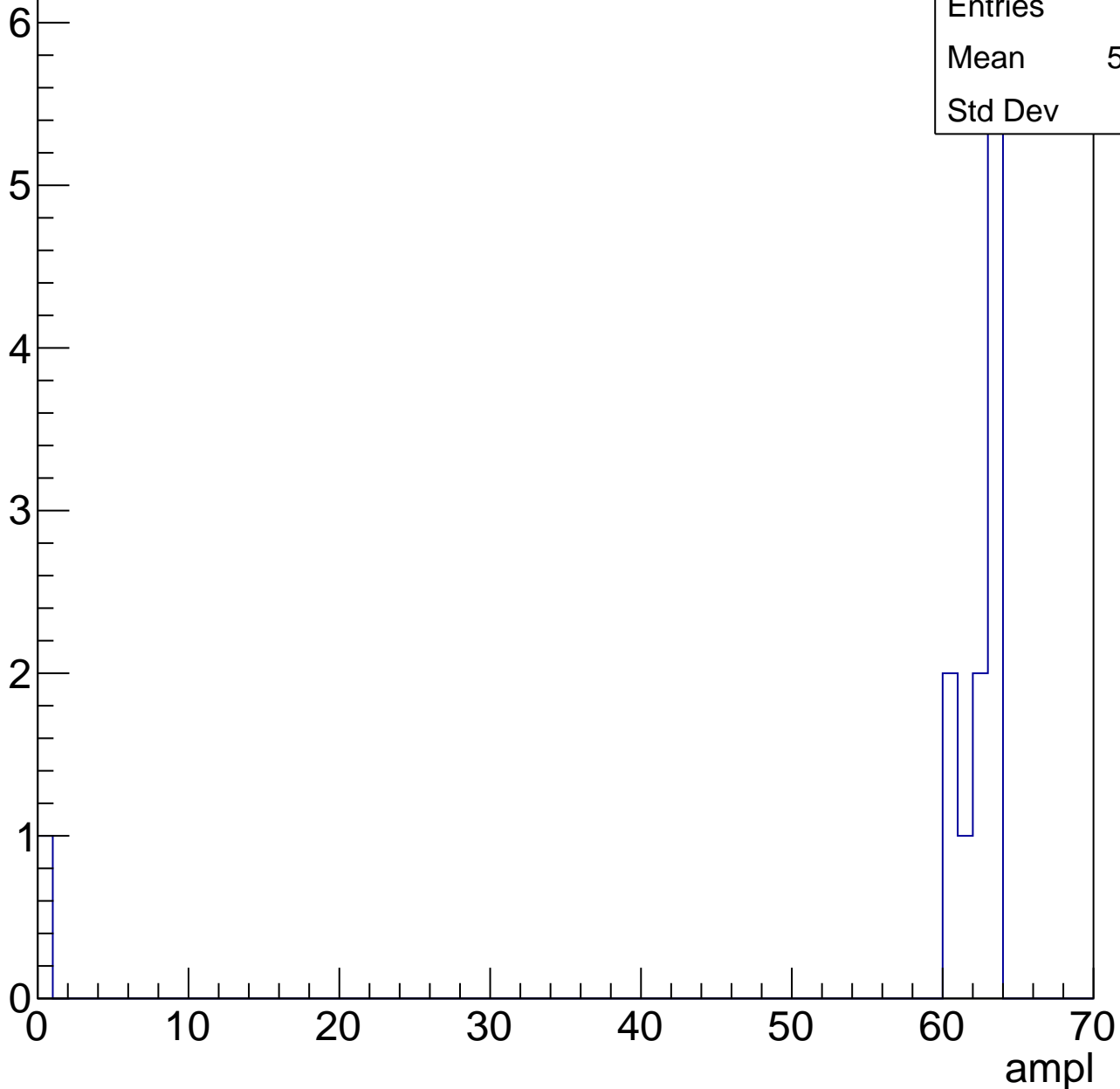
341

# B1L102S, U3-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	12
Mean	56.92
Std Dev	17.2





# B1L102S, U3-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch25, adc0

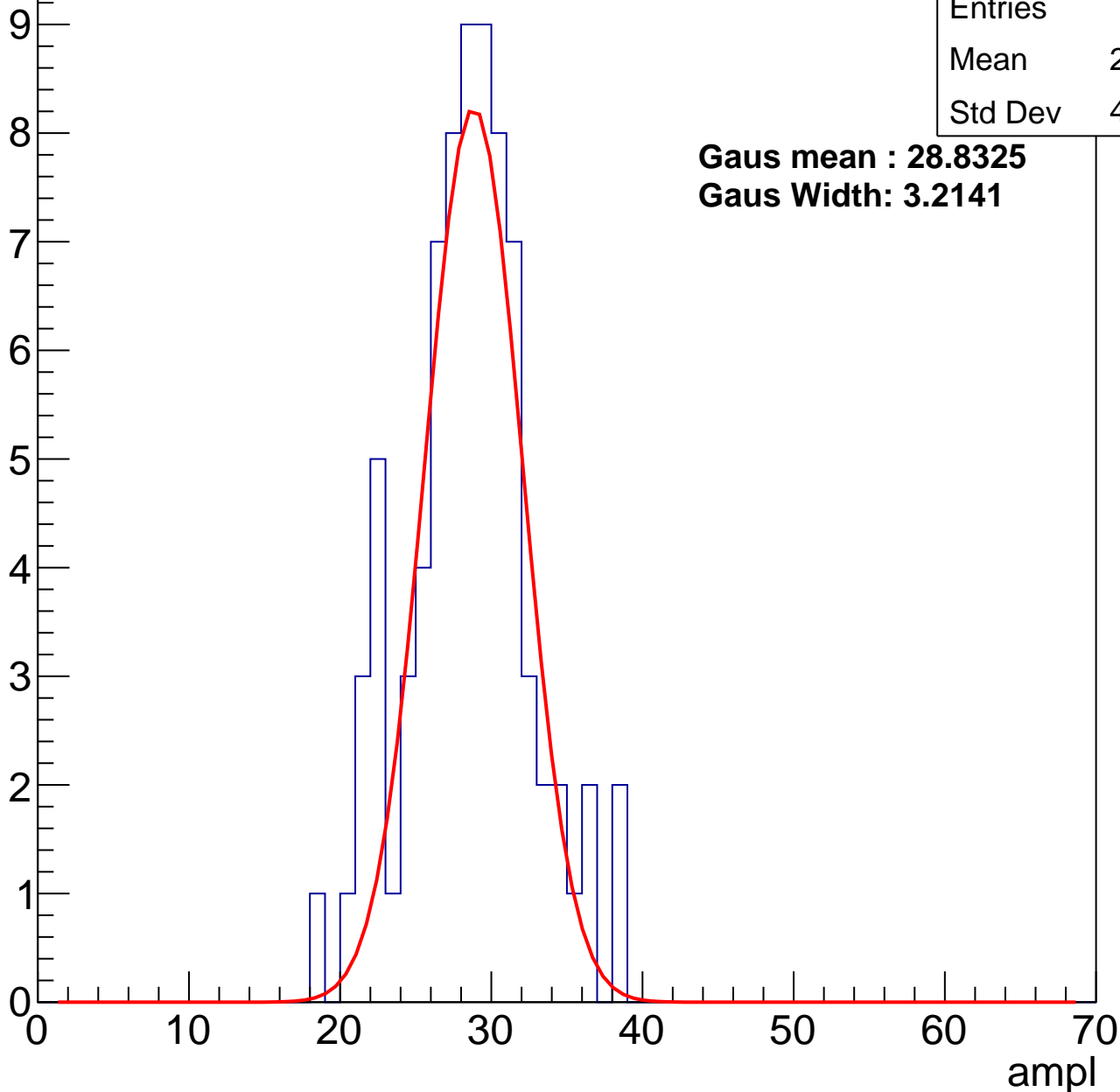
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	28.04
Std Dev	4.062

**Gaus mean : 28.8325**

**Gaus Width: 3.2141**



# B1L102S, U3-ch25, adc1

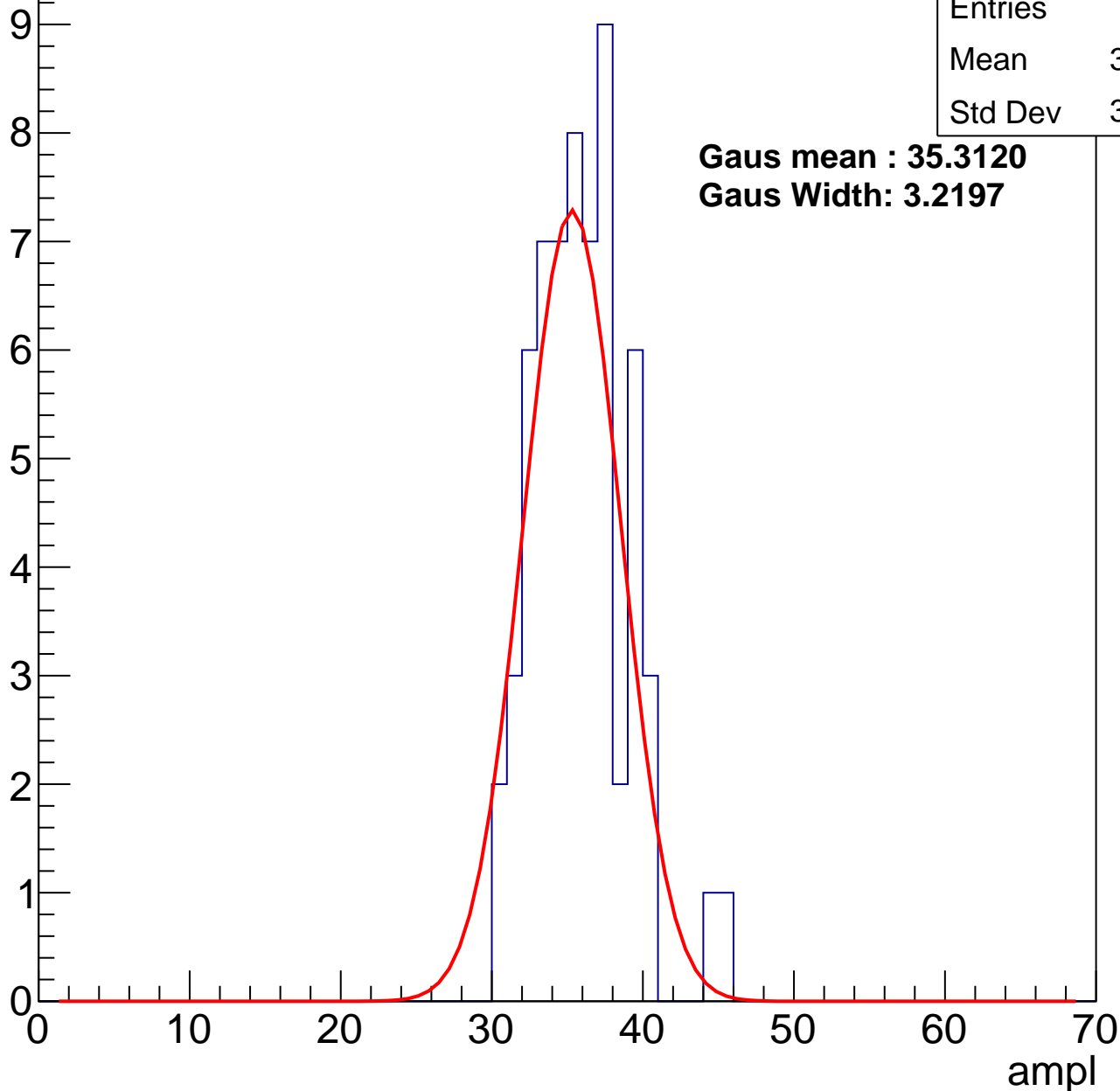
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	35.45
Std Dev	3.078

**Gaus mean : 35.3120**

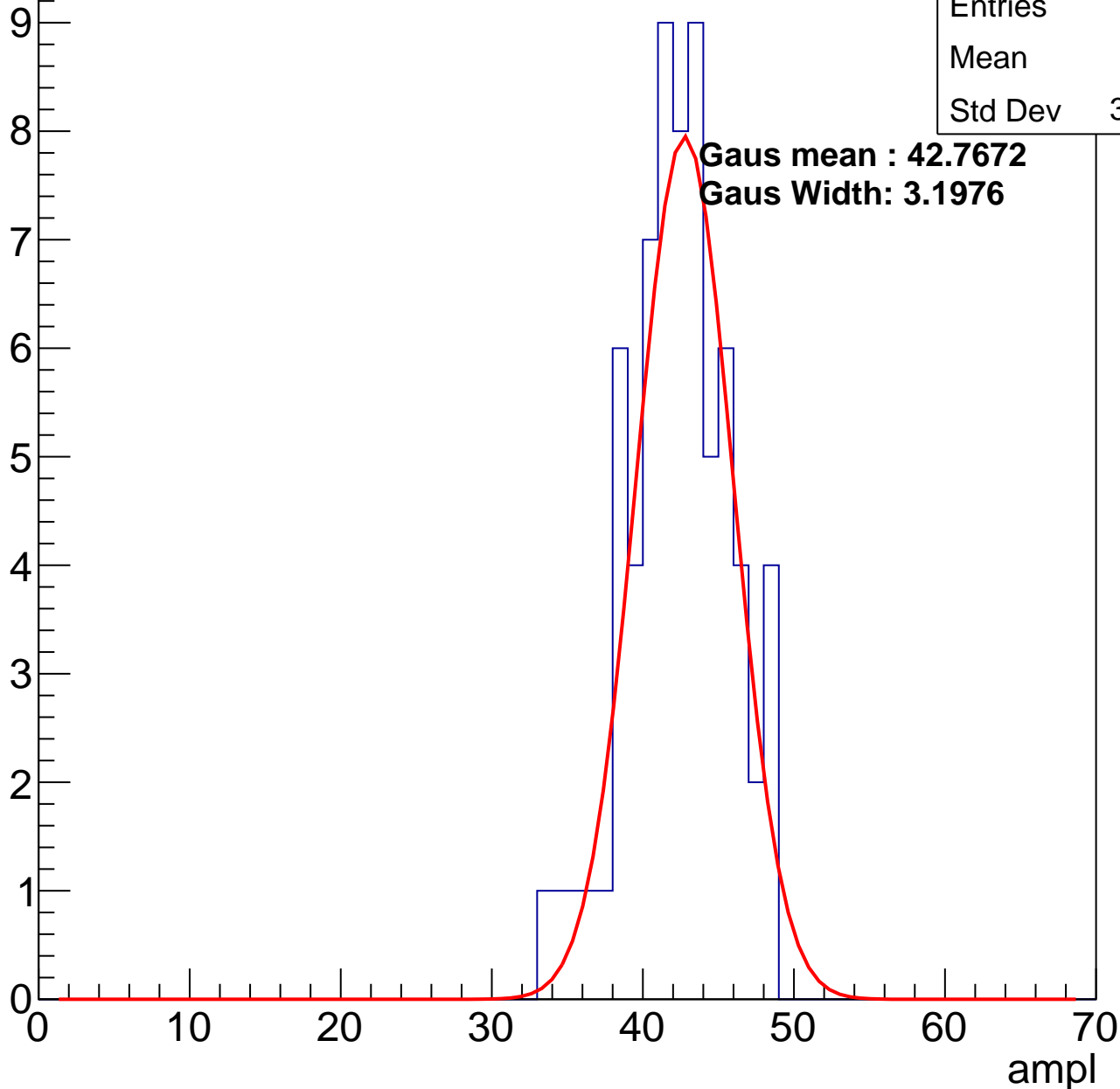
**Gaus Width: 3.2197**



# B1L102S, U3-ch25, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	71
Mean	48.82
Std Dev	3.269

Entry

10

8

6

4

2

0

0

10

20

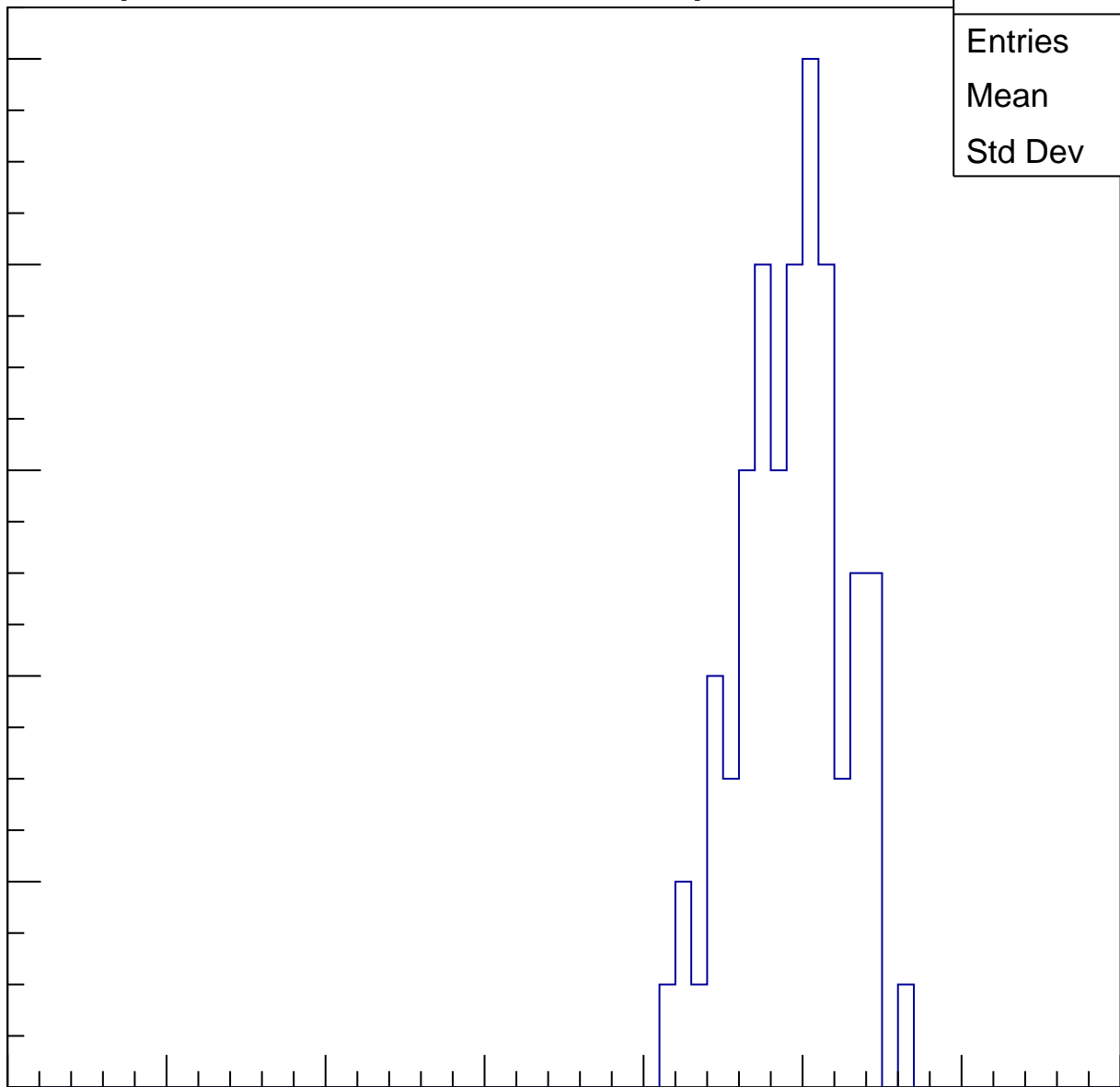
30

40

50

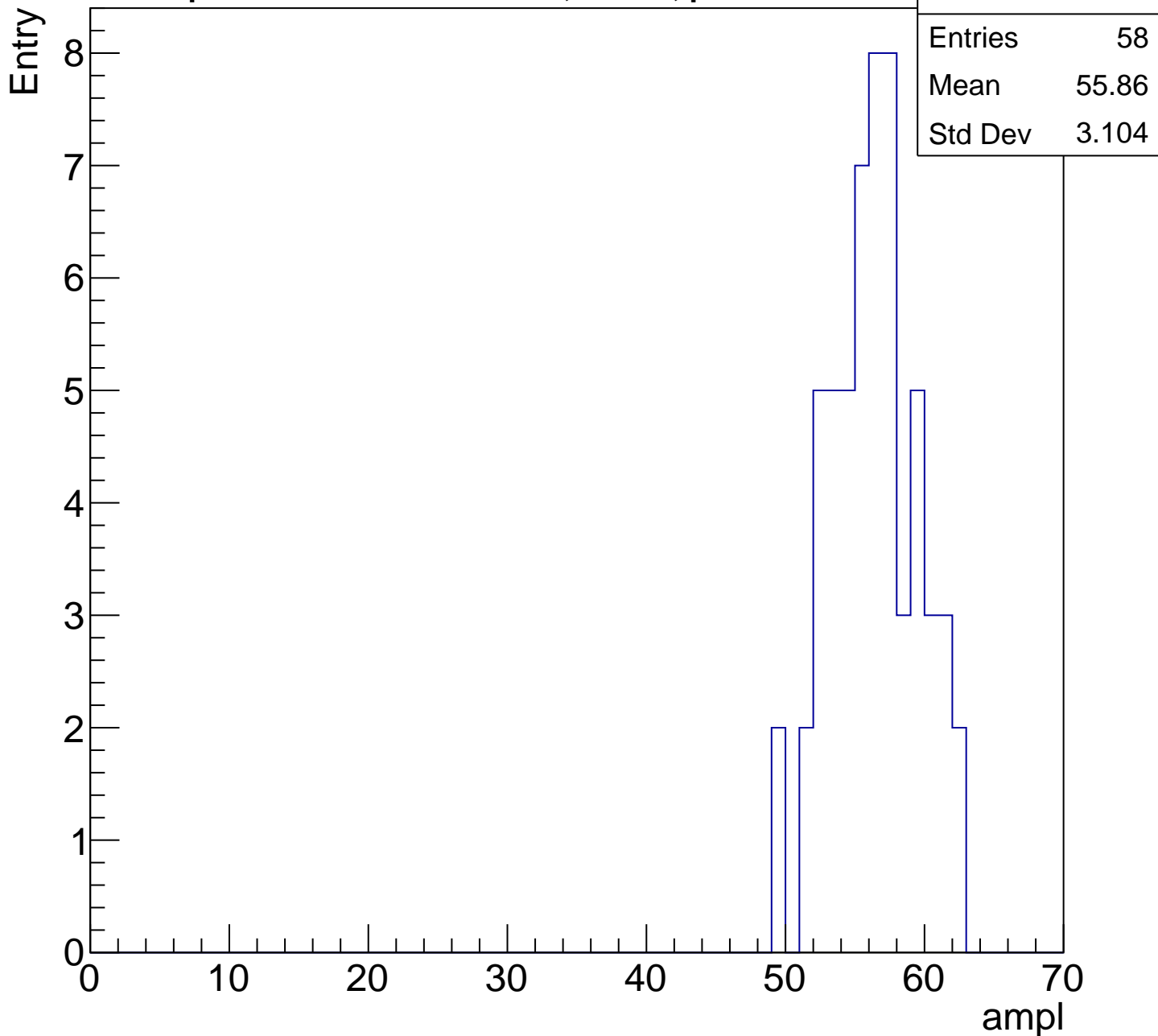
60

ampl



# B1L102S, U3-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

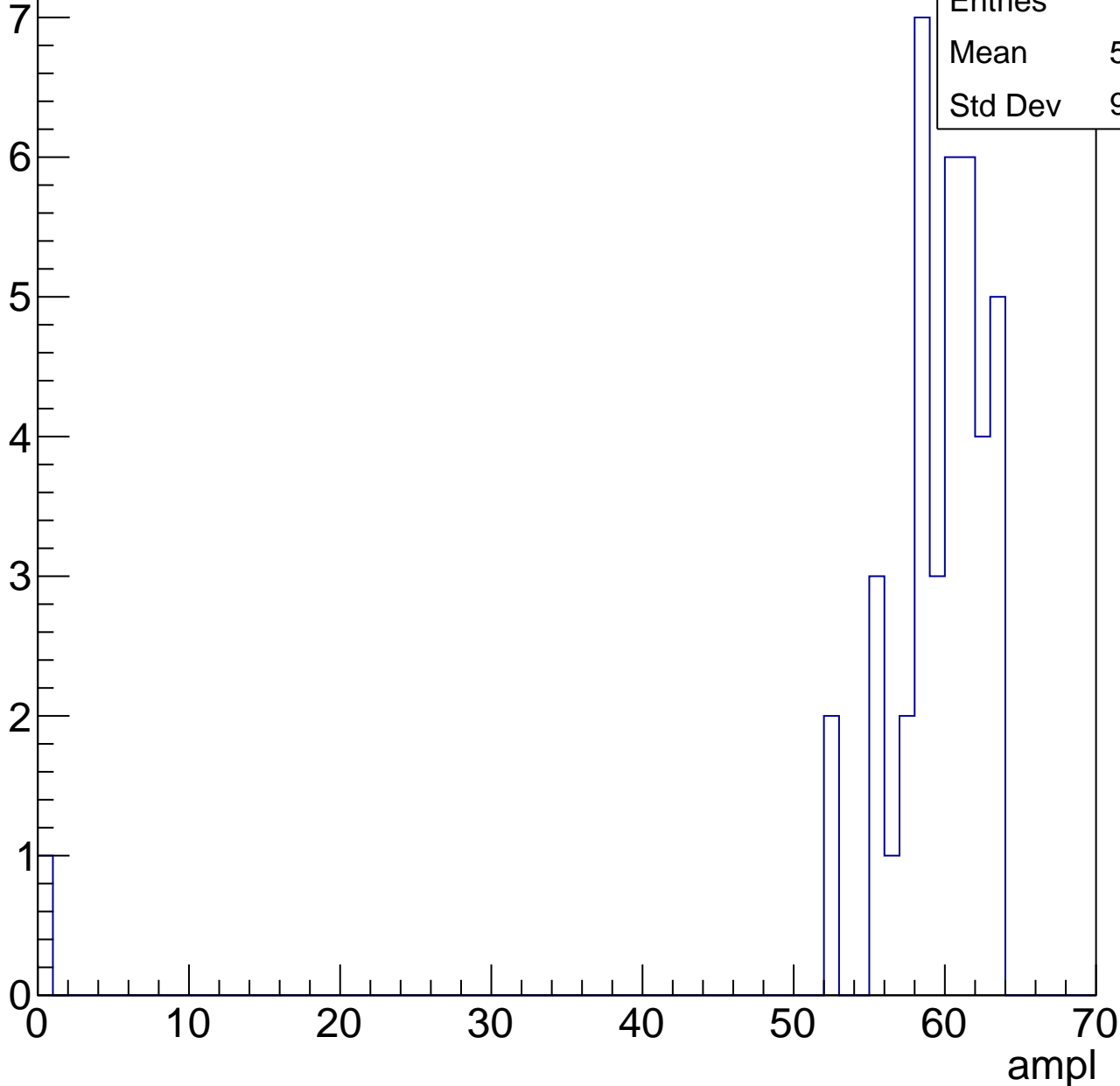


# B1L102S, U3-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	57.77
Std Dev	9.666

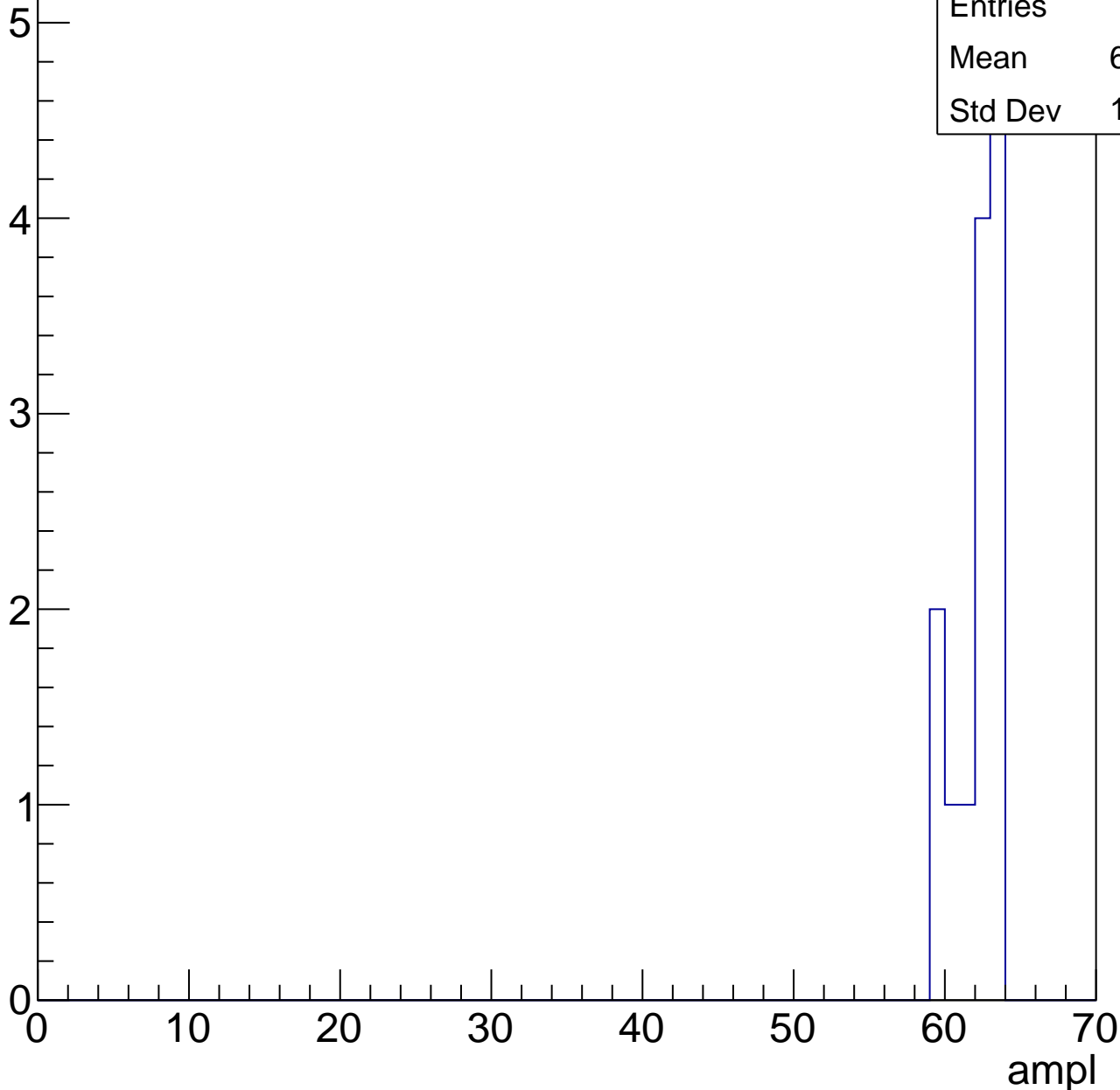


# B1L102S, U3-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	13
Mean	61.69
Std Dev	1.435





# B1L102S, U3-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L102S, U3-ch26, adc0

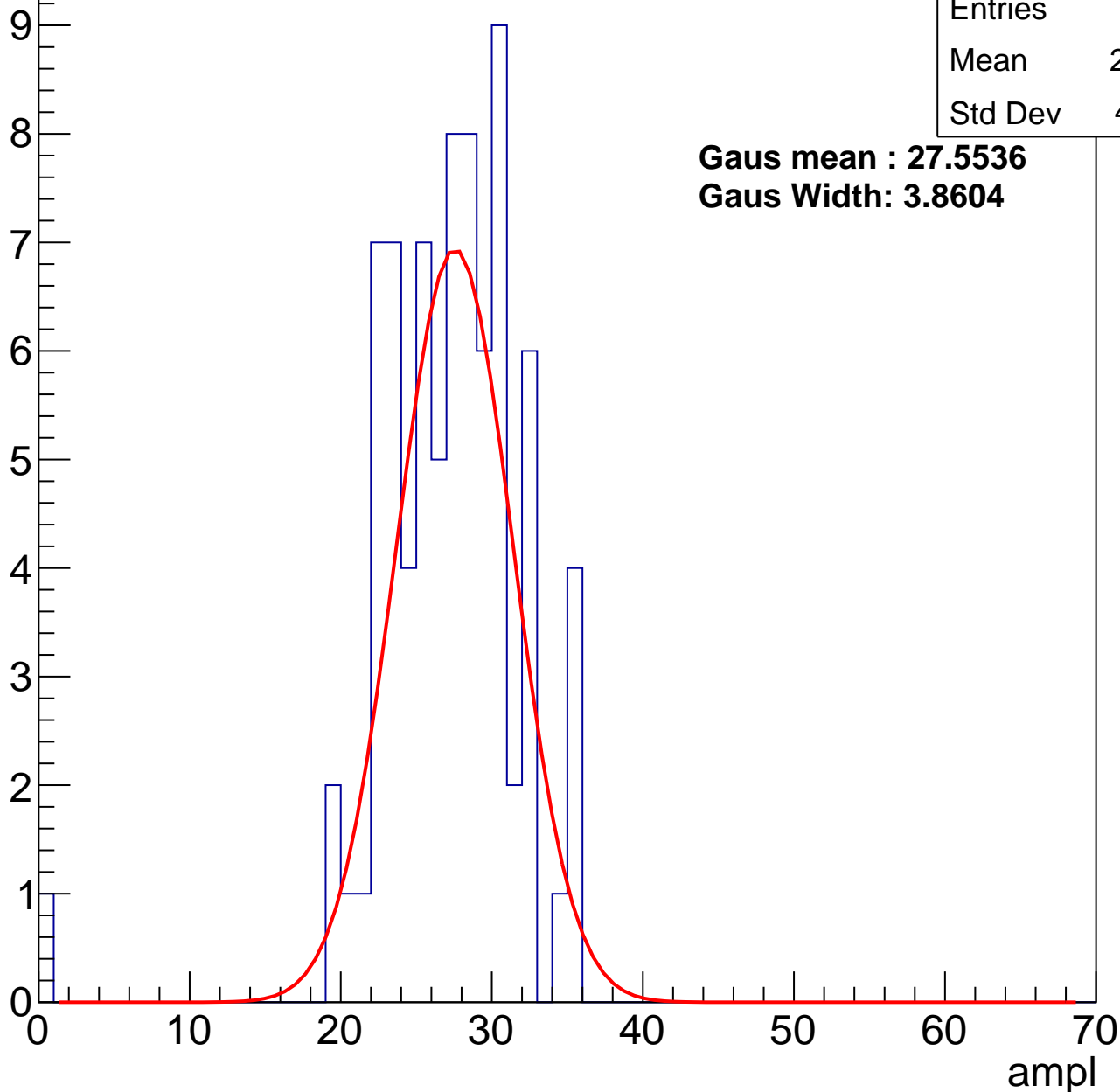
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	26.67
Std Dev	4.891

**Gaus mean : 27.5536**

**Gaus Width: 3.8604**



# B1L102S, U3-ch26, adc1

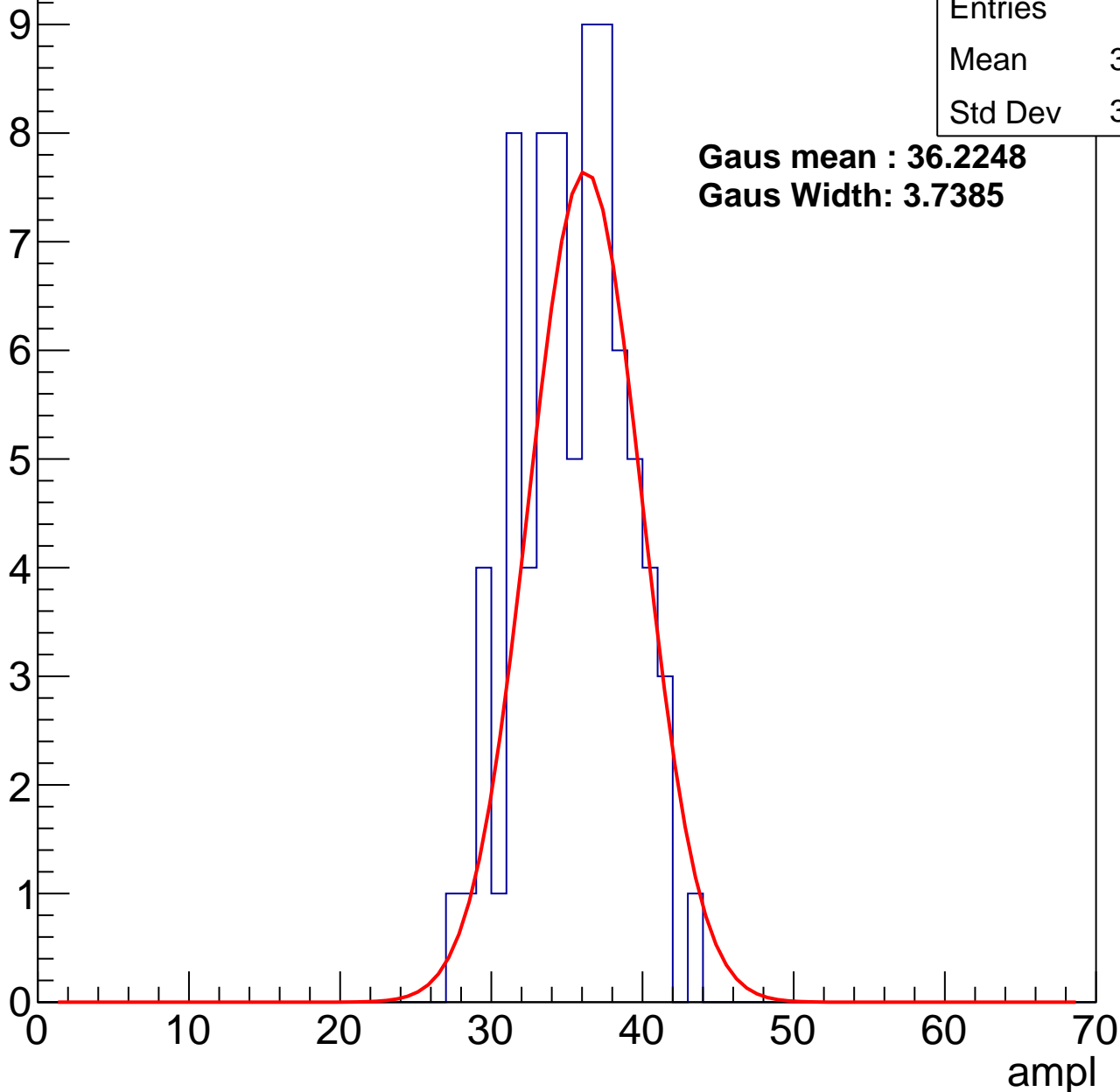
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	34.99
Std Dev	3.488

**Gaus mean : 36.2248**

**Gaus Width: 3.7385**



# B1L102S, U3-ch26, adc2

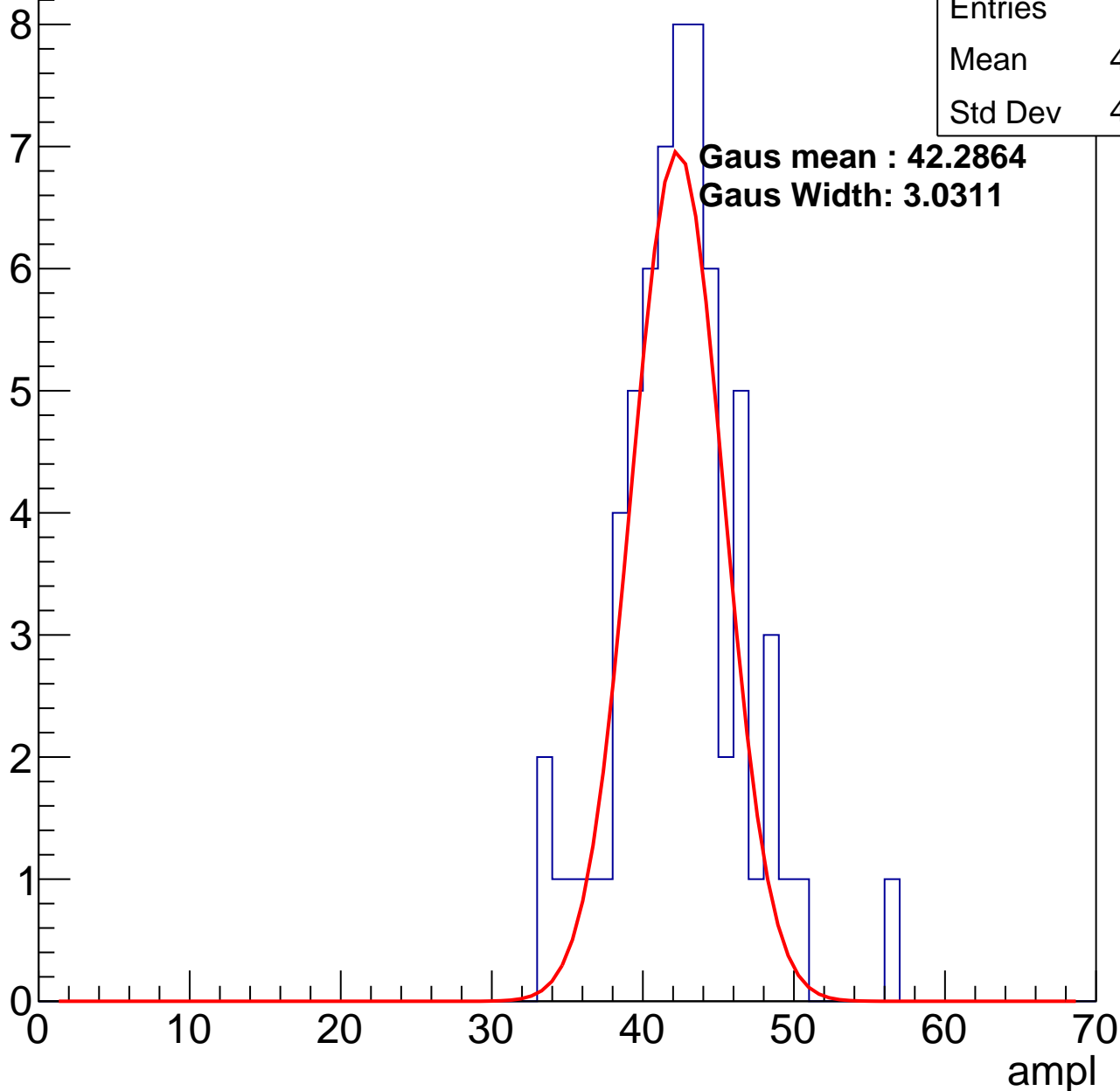
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	42.06
Std Dev	4.046

**Gaus mean : 42.2864**

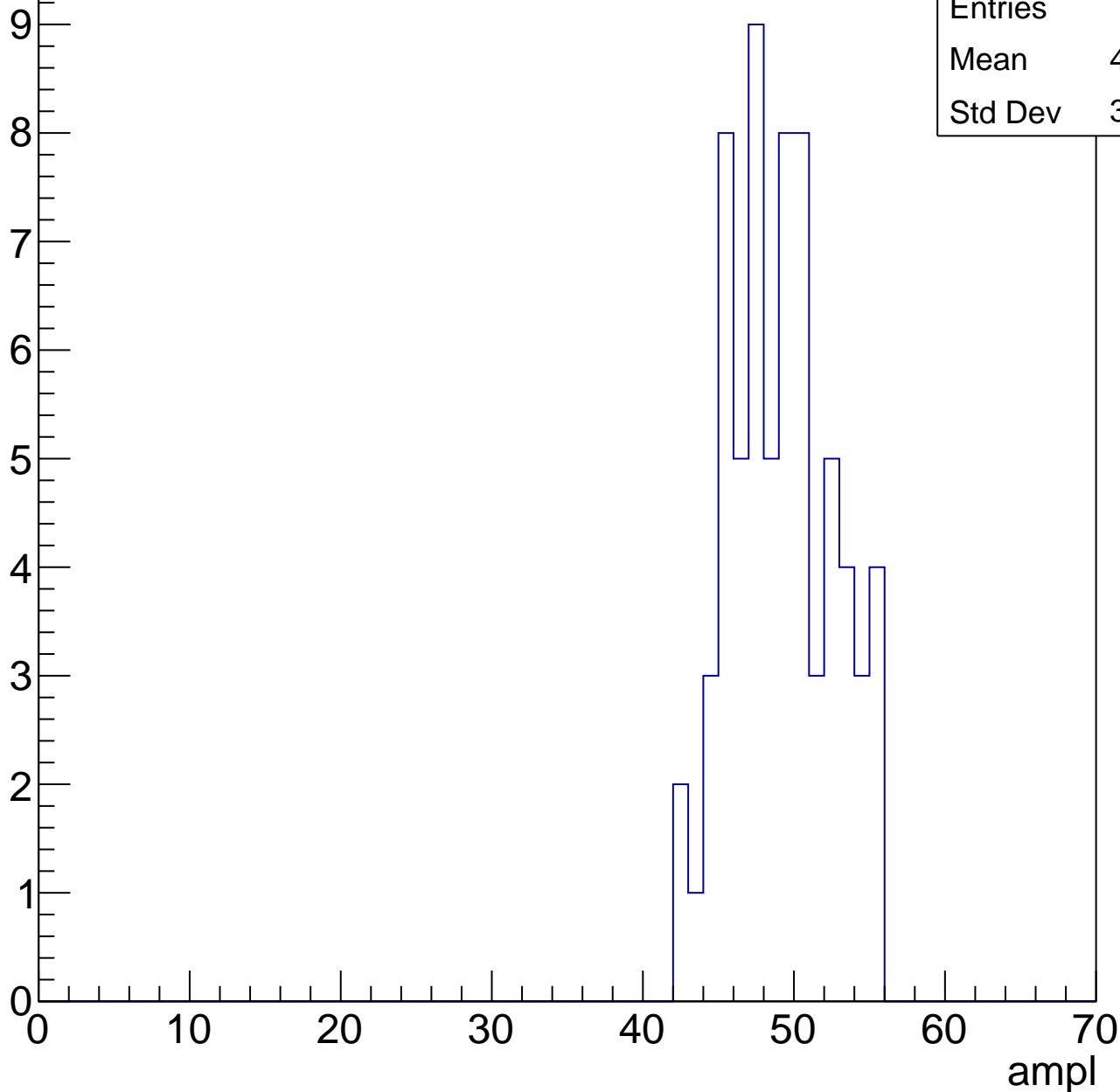
**Gaus Width: 3.0311**



# B1L102S, U3-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



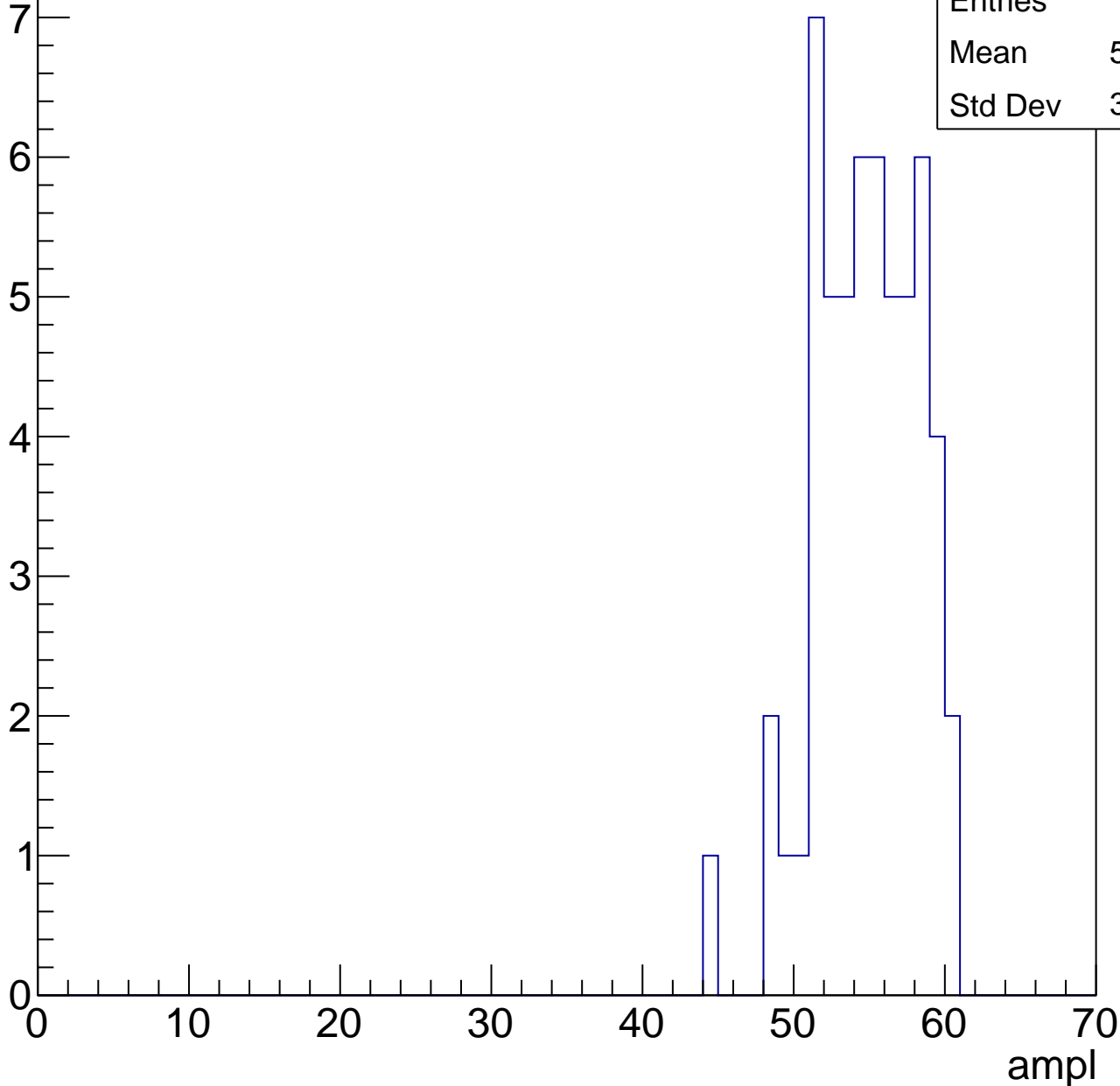
Entries	68
Mean	48.69
Std Dev	3.353

# B1L102S, U3-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	54.36
Std Dev	3.362

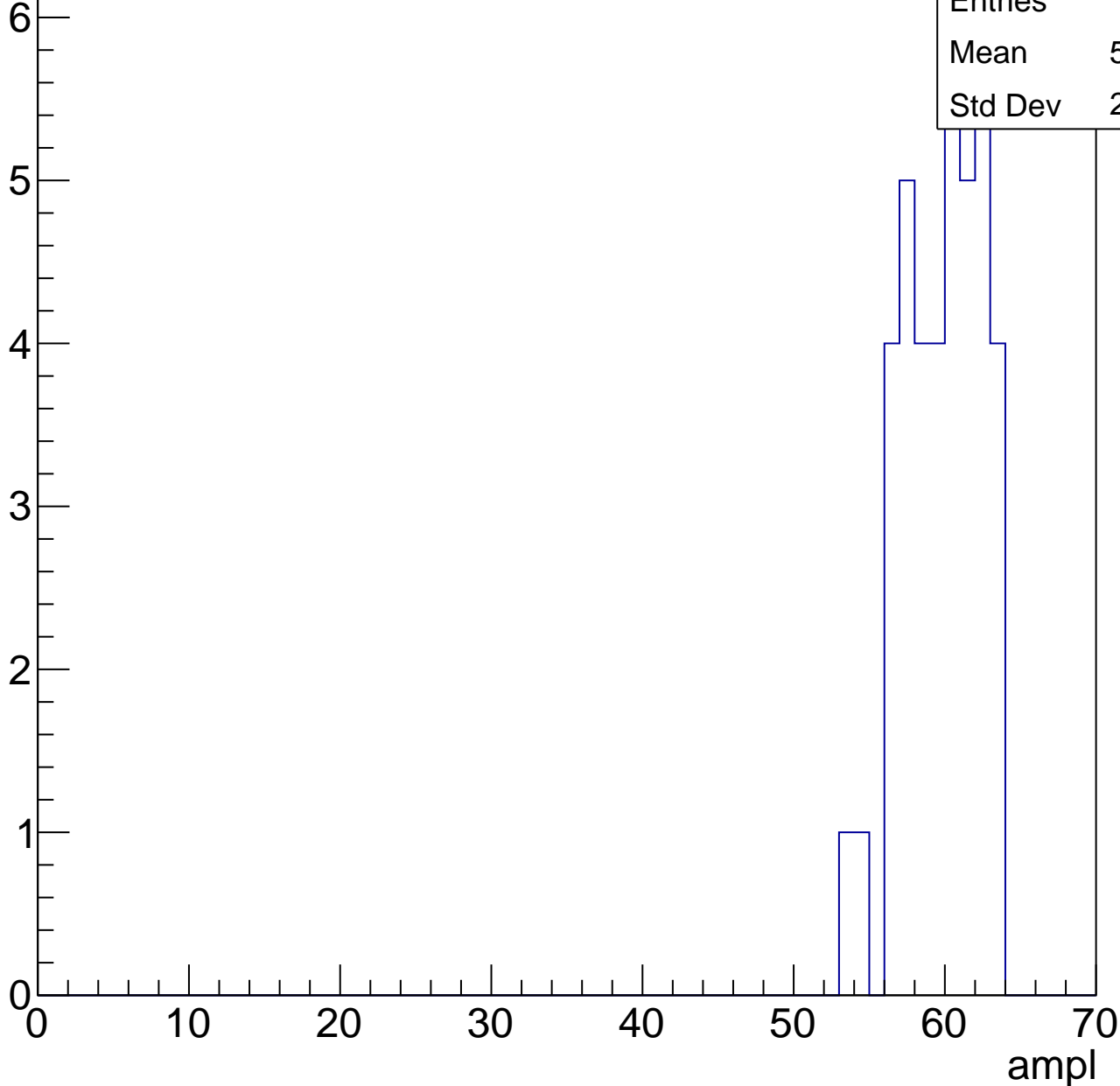


# B1L102S, U3-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	59.33
Std Dev	2.553

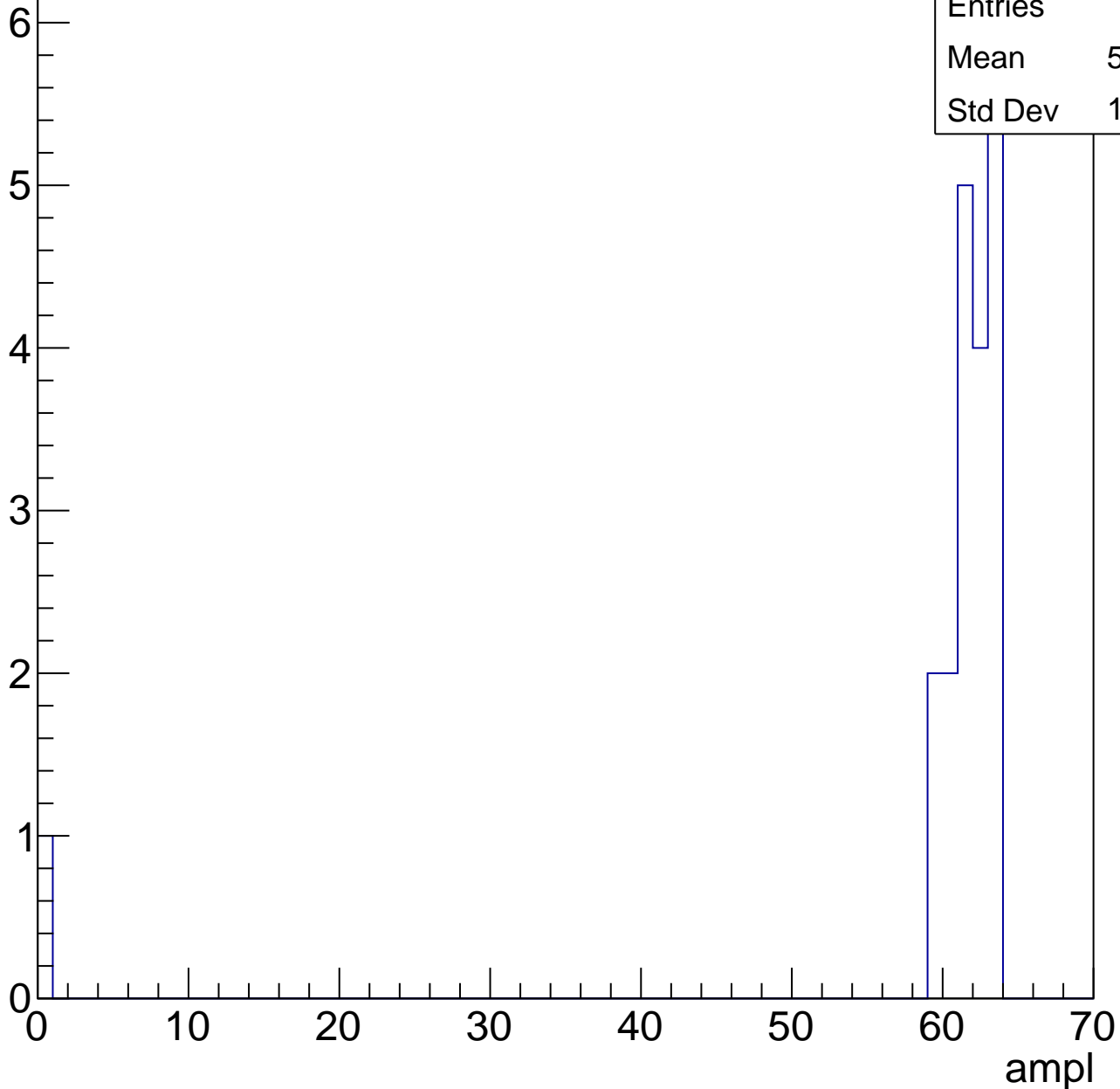


# B1L102S, U3-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	20
Mean	58.45
Std Dev	13.47





# B1L102S, U3-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U3-ch27, adc0

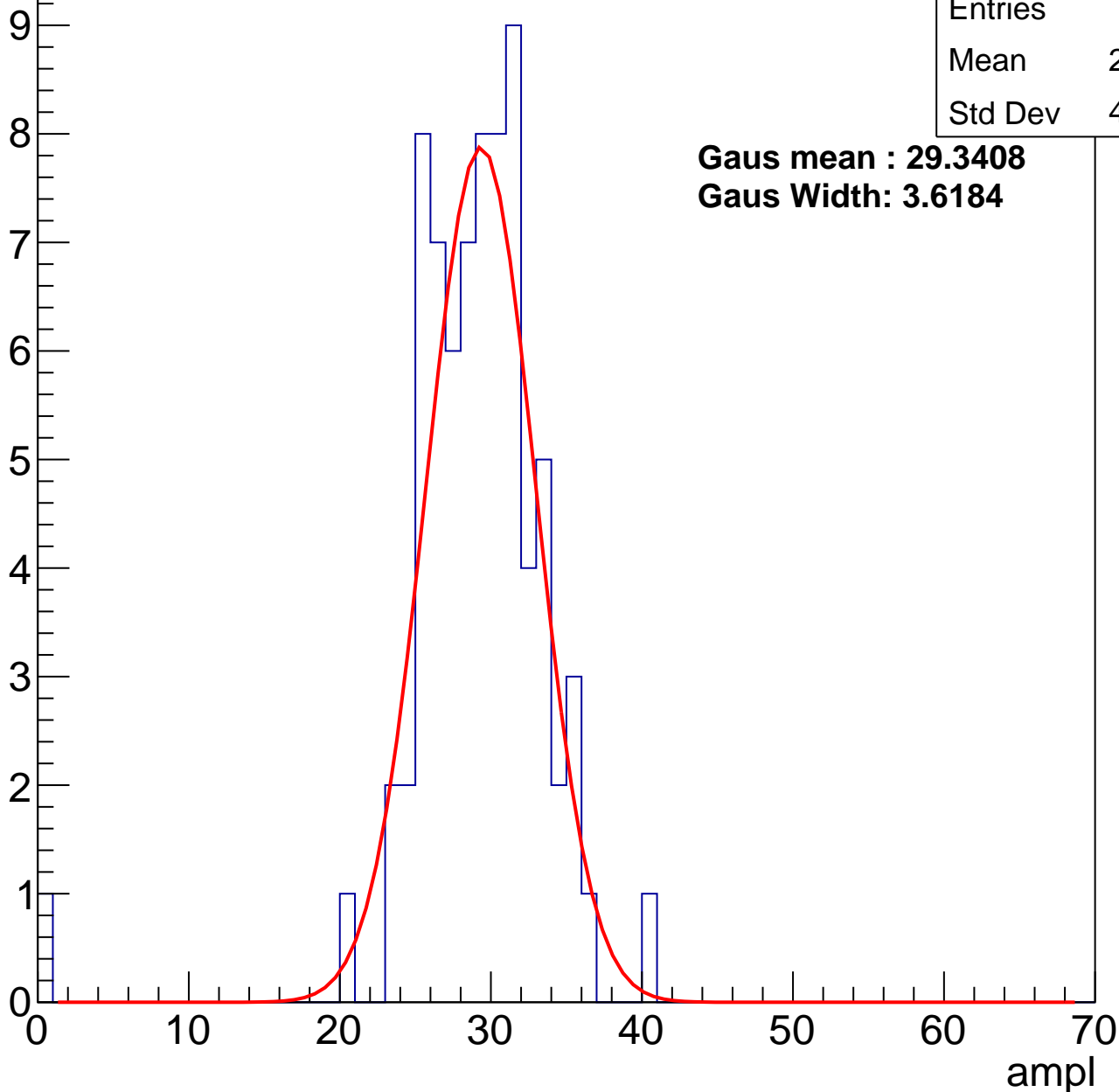
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	28.63
Std Dev	4.822

**Gaus mean : 29.3408**

**Gaus Width: 3.6184**



# B1L102S, U3-ch27, adc1

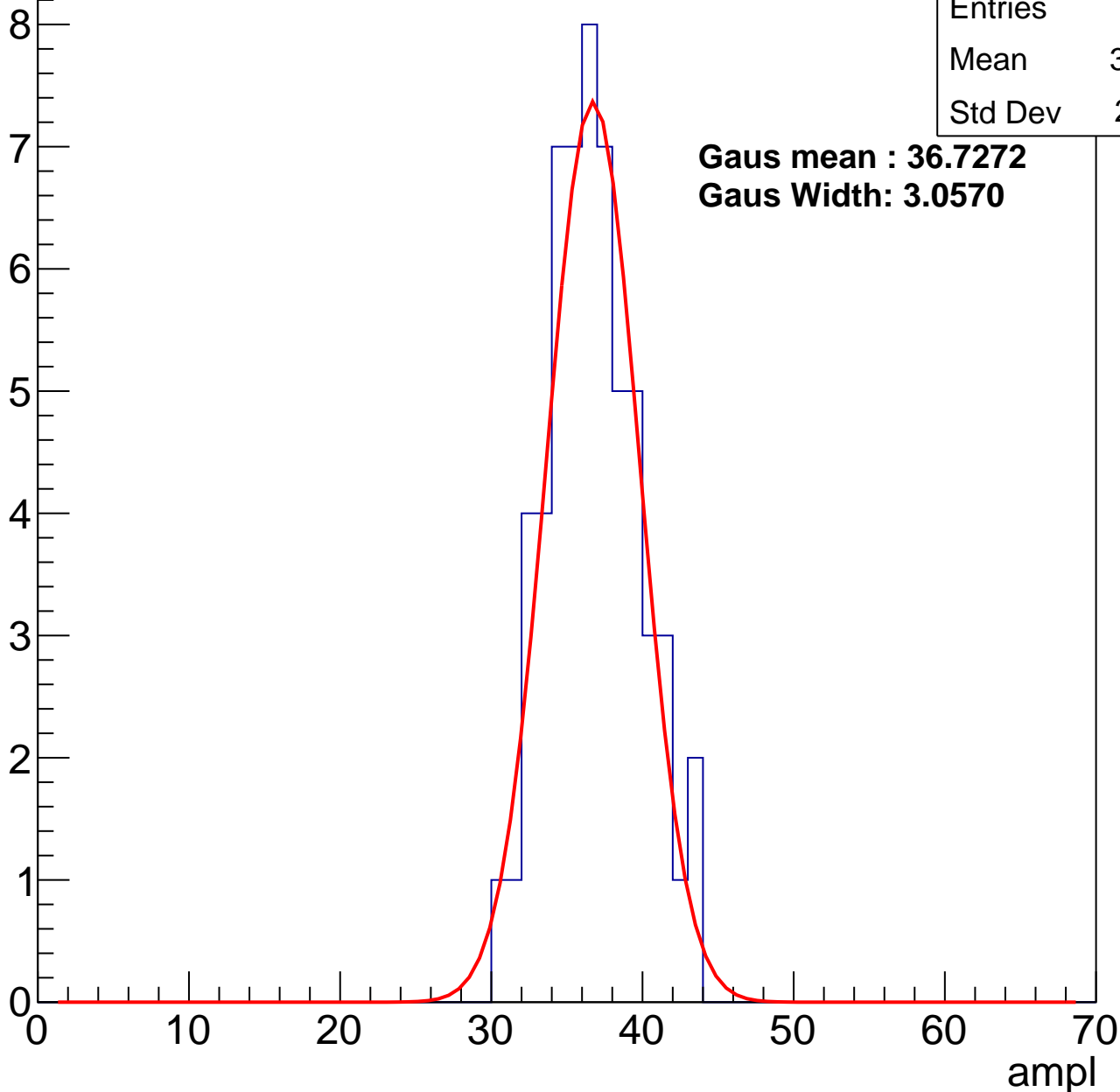
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	36.33
Std Dev	2.991

**Gaus mean : 36.7272**

**Gaus Width: 3.0570**



# B1L102S, U3-ch27, adc2

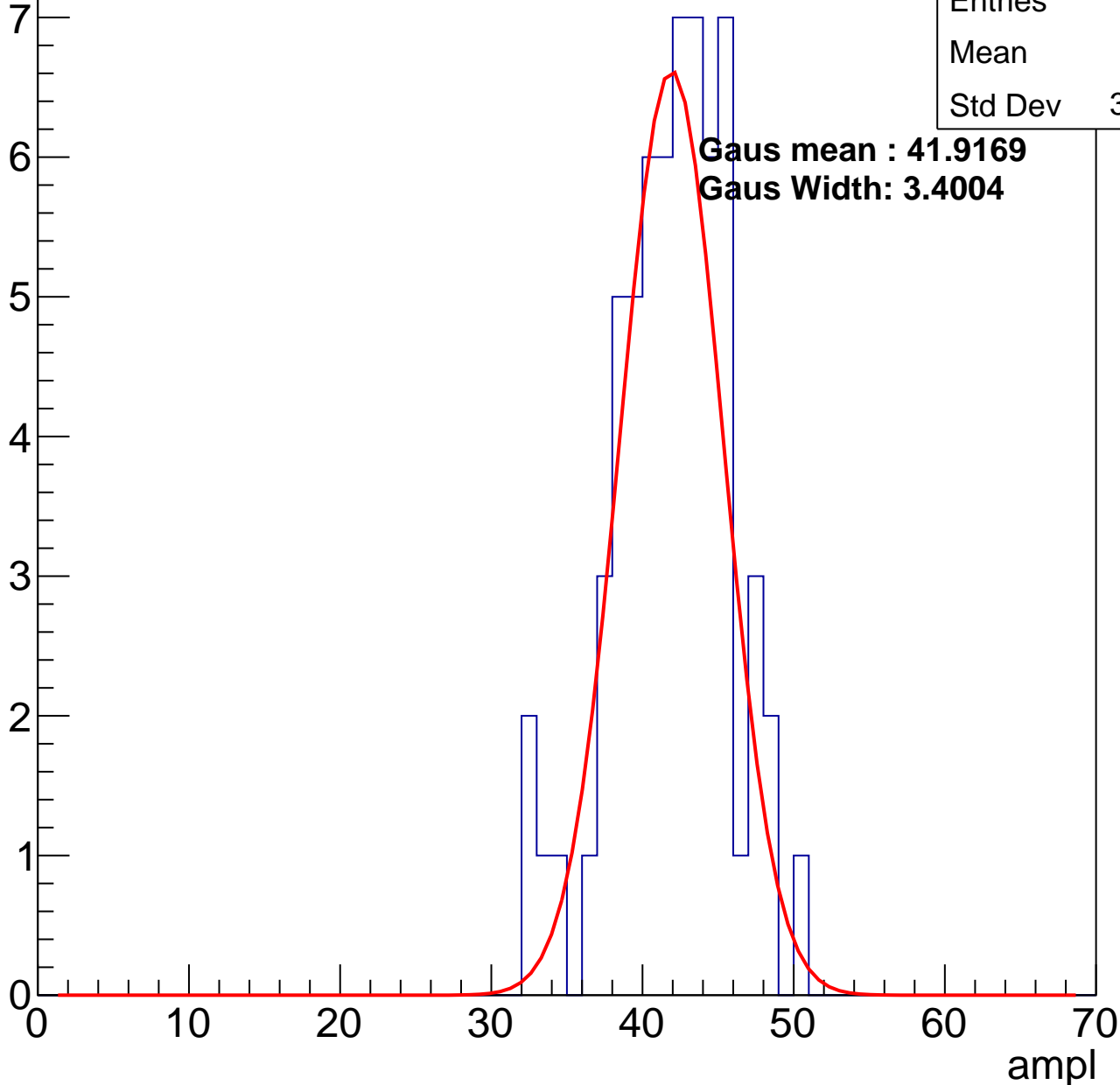
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	41.5
Std Dev	3.783

**Gaus mean : 41.9169**

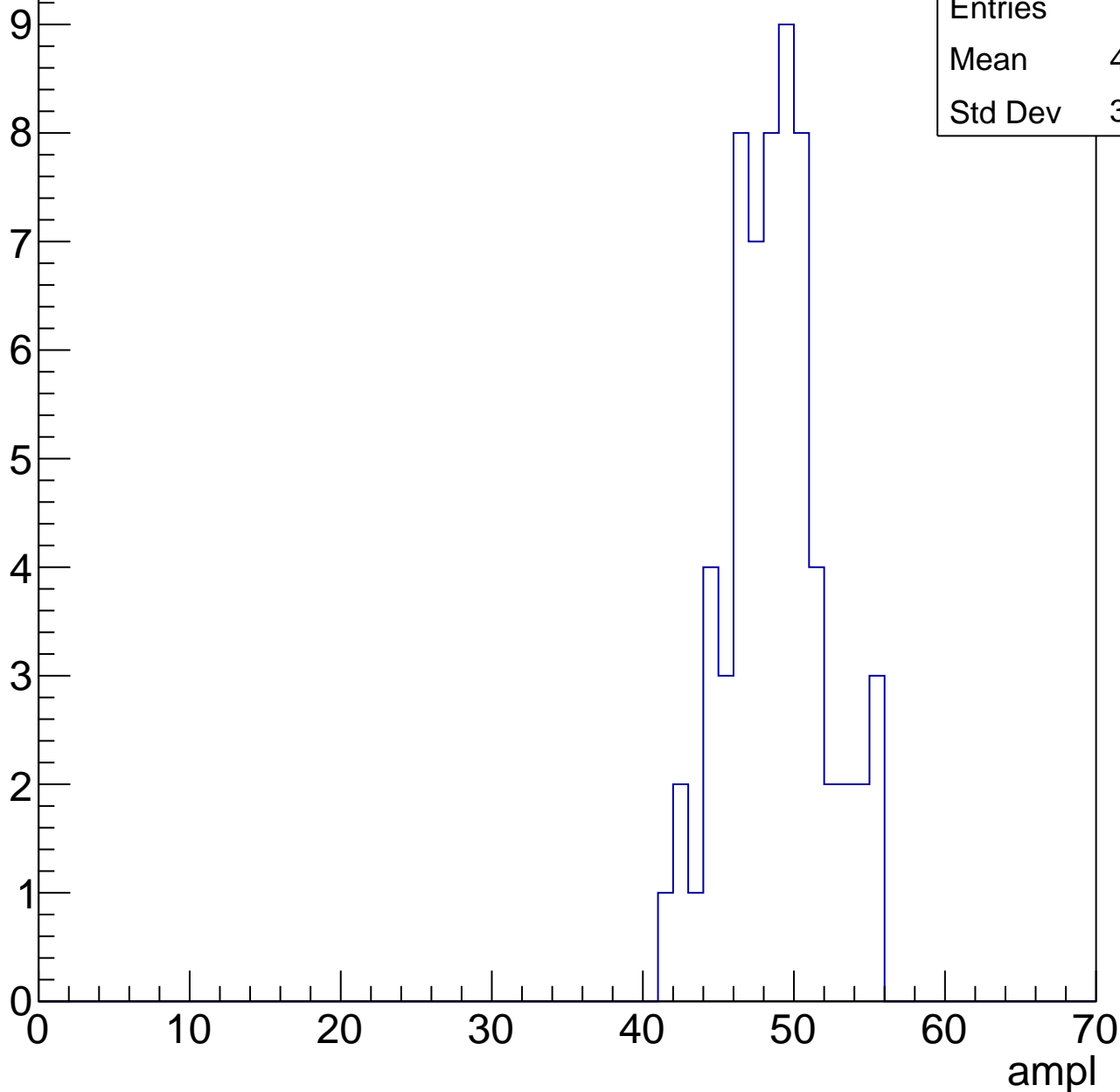
**Gaus Width: 3.4004**



# B1L102S, U3-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



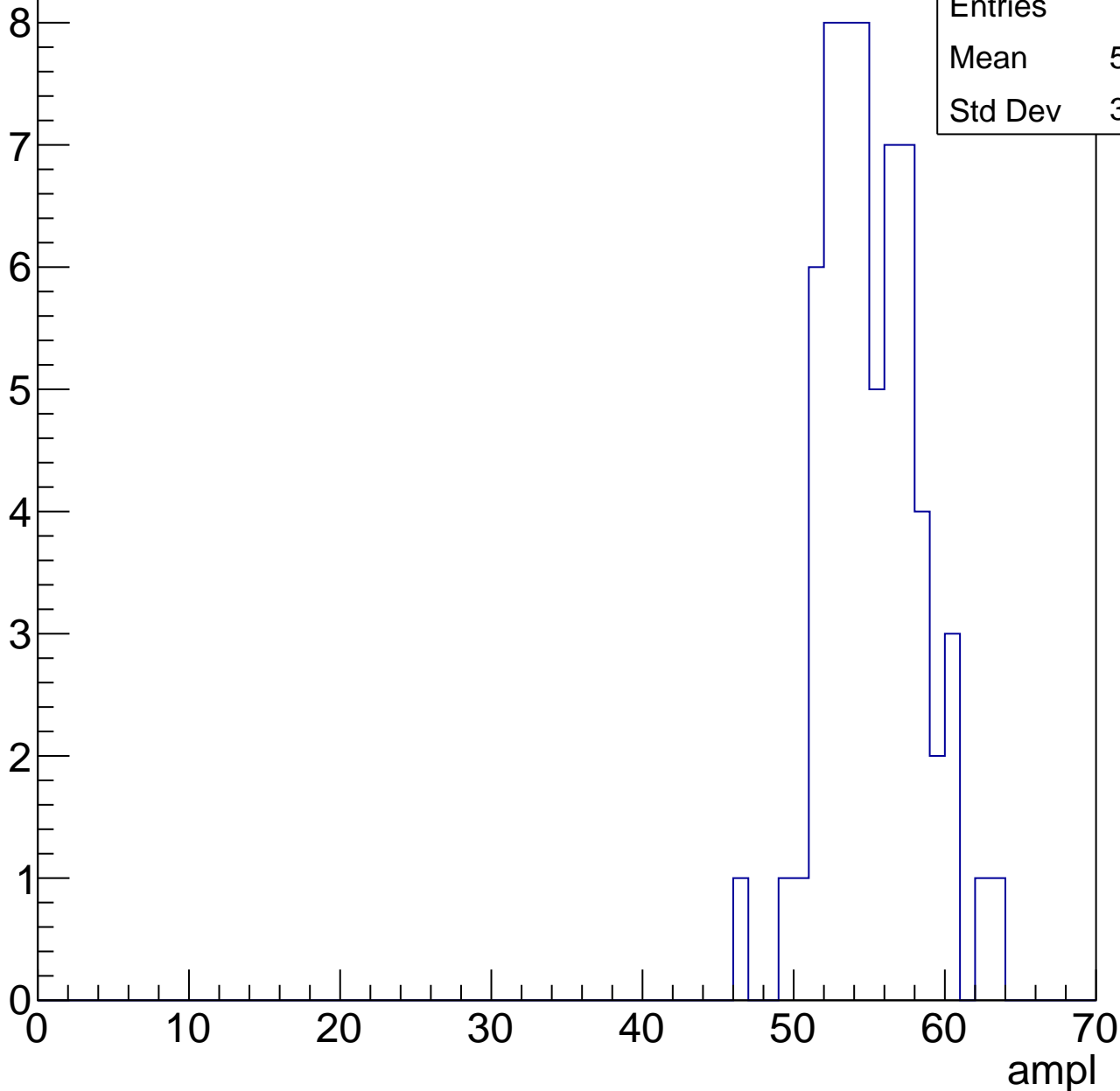
Entries	64
Mean	48.25
Std Dev	3.187

# B1L102S, U3-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	54.67
Std Dev	3.172



# B1L102S, U3-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	54
Mean	58.81
Std Dev	8.378

ampl

0

10

20

30

40

50

60

70

# B1L102S, U3-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	62
Std Dev	0.7071

ampl

0 10 20 30 40 50 60 70



# B1L102S, U3-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch28, adc0

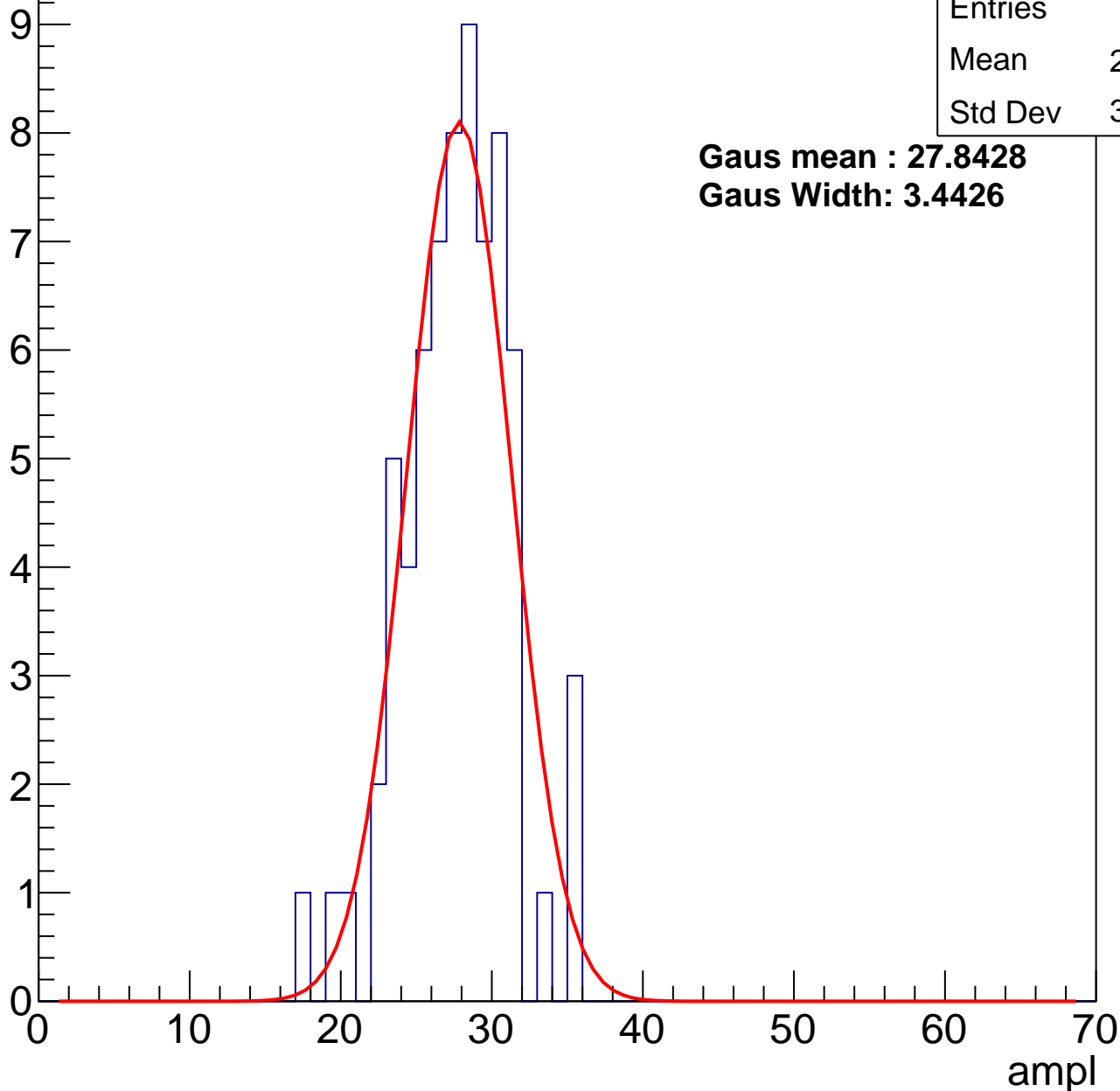
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	27.22
Std Dev	3.489

**Gaus mean : 27.8428**

**Gaus Width: 3.4426**



# B1L102S, U3-ch28, adc1

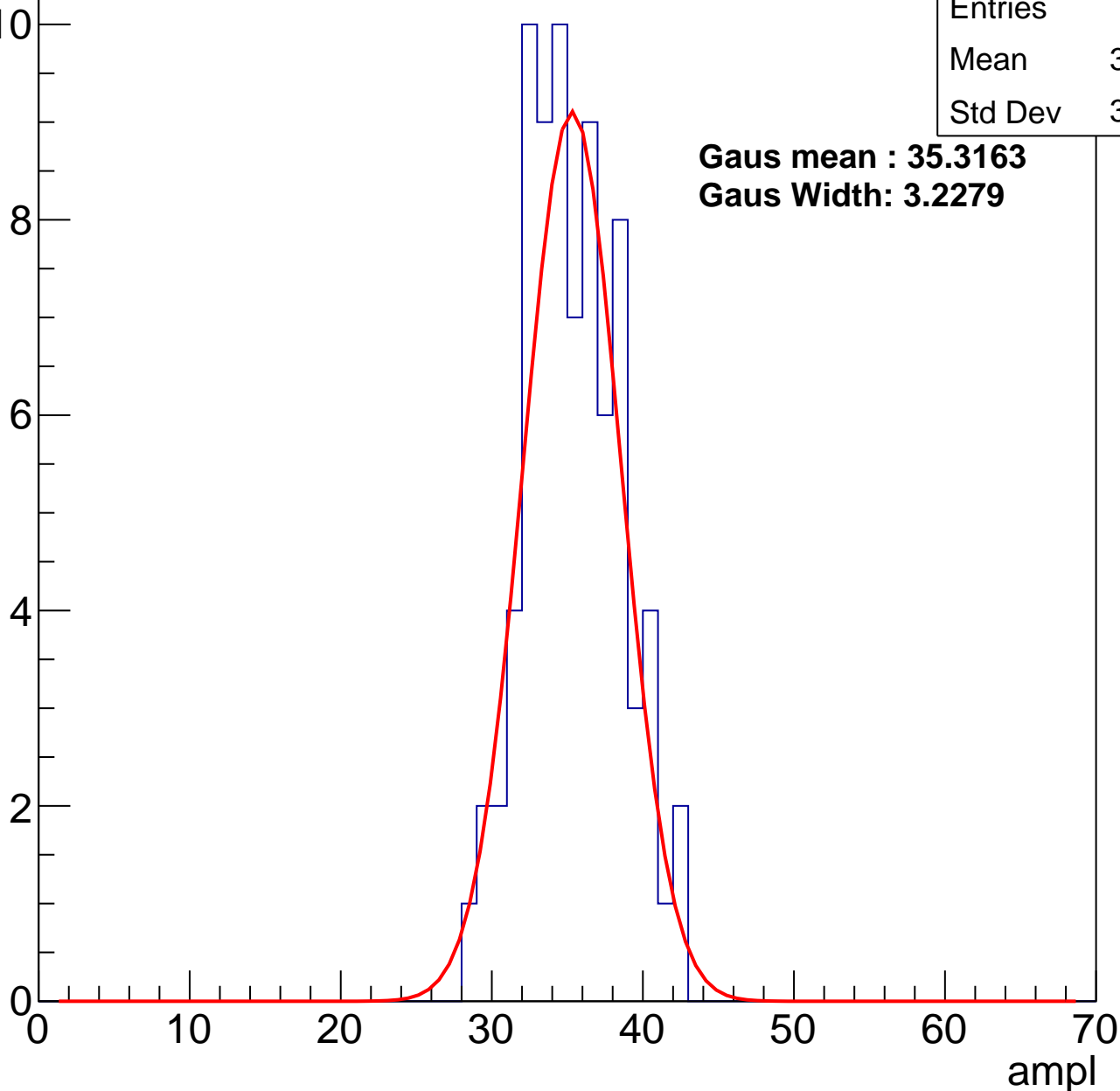
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	34.92
Std Dev	3.116

**Gaus mean : 35.3163**

**Gaus Width: 3.2279**



# B1L102S, U3-ch28, adc2

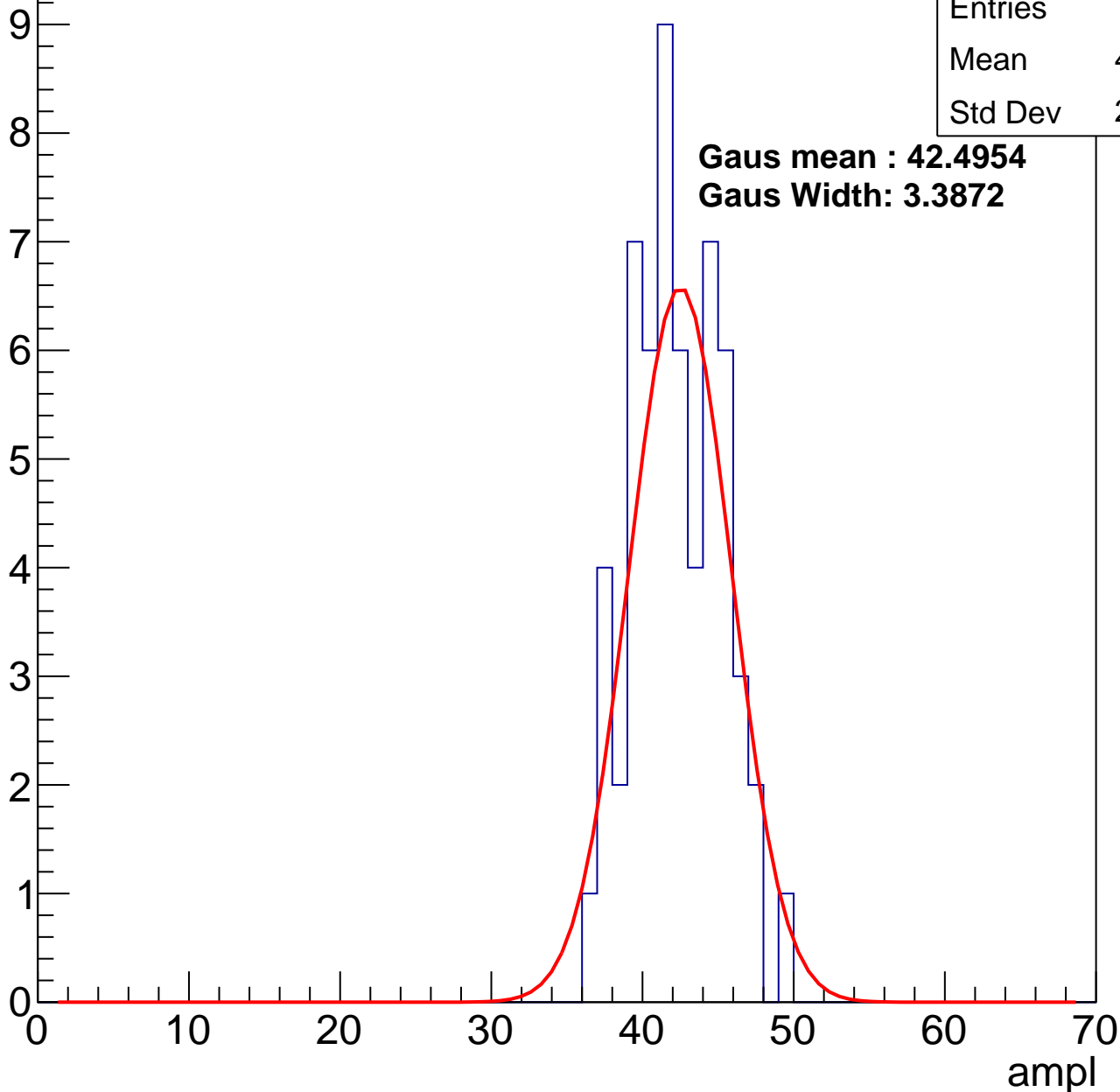
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	41.81
Std Dev	2.921

**Gaus mean : 42.4954**

**Gaus Width: 3.3872**

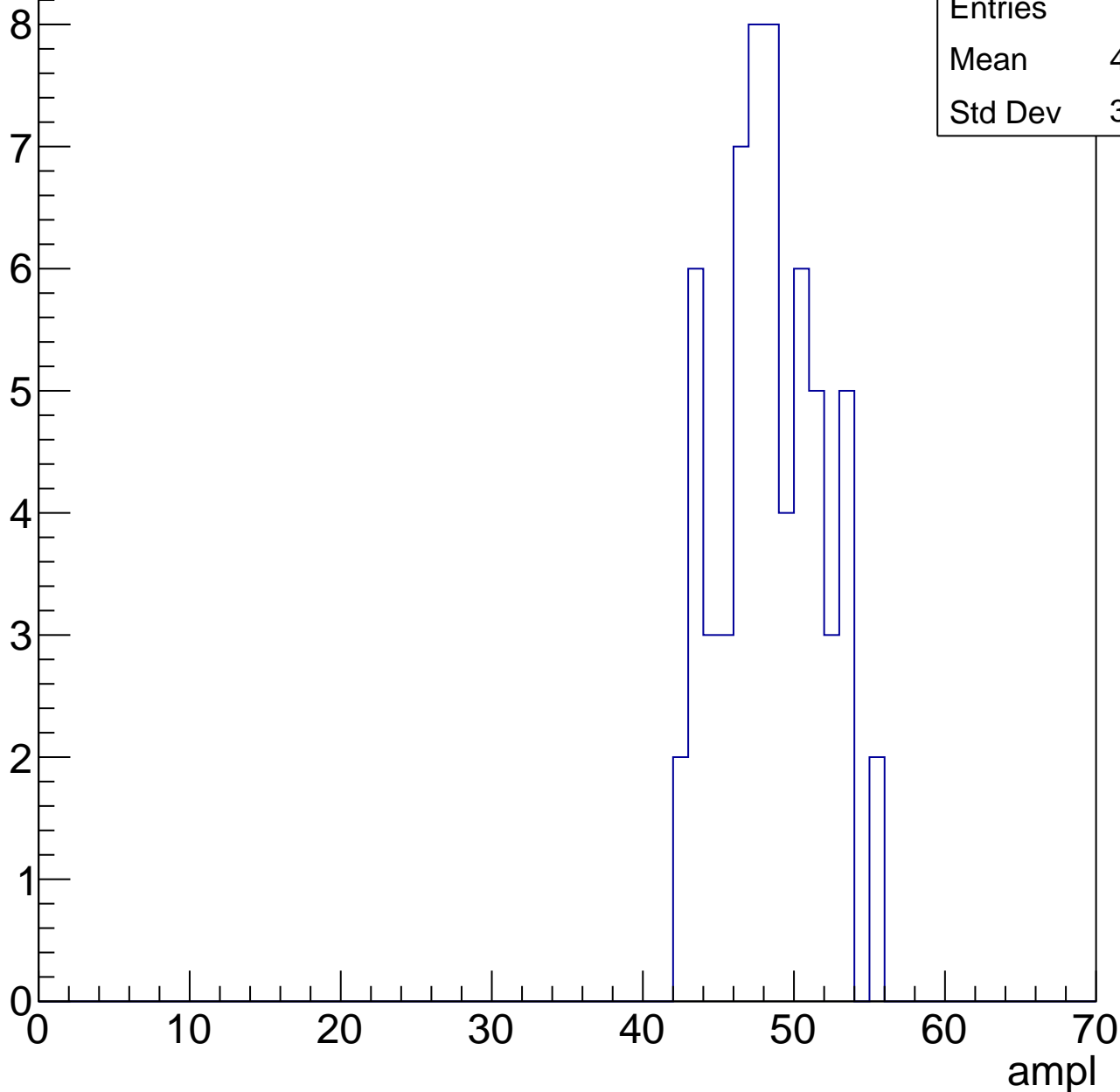


# B1L102S, U3-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	47.95
Std Dev	3.304

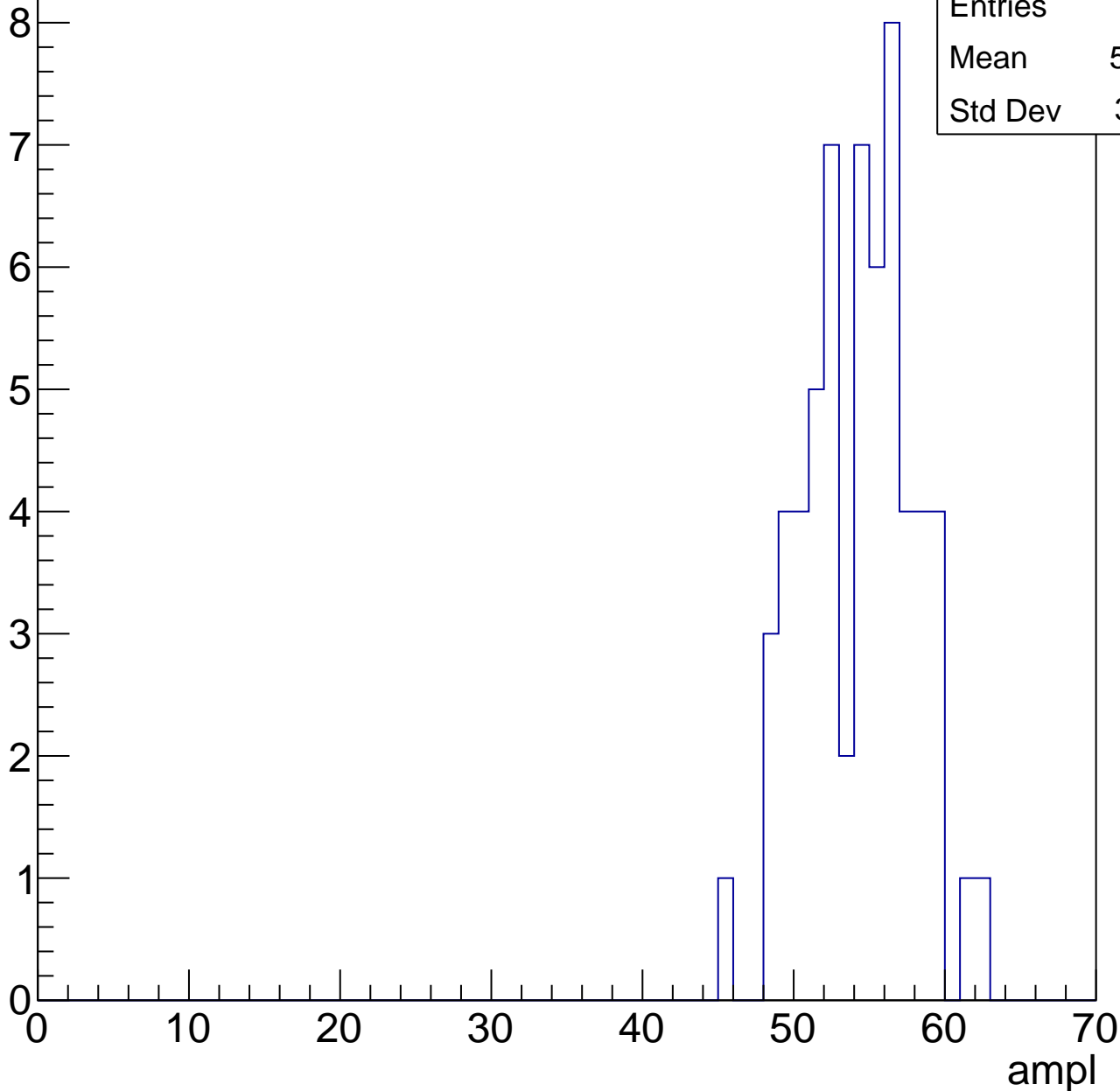


# B1L102S, U3-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	53.85
Std Dev	3.571

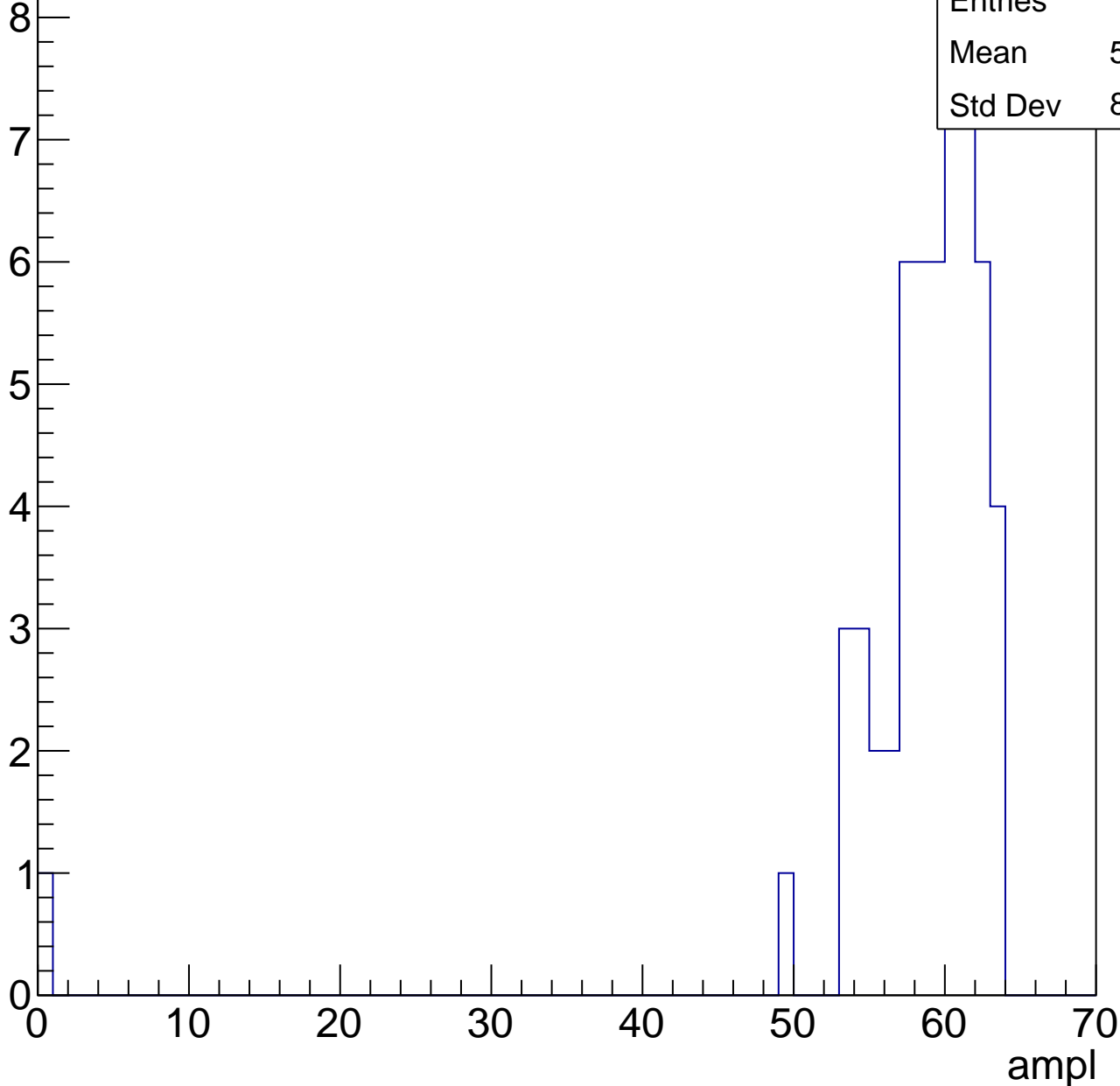


# B1L102S, U3-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	57.64
Std Dev	8.344

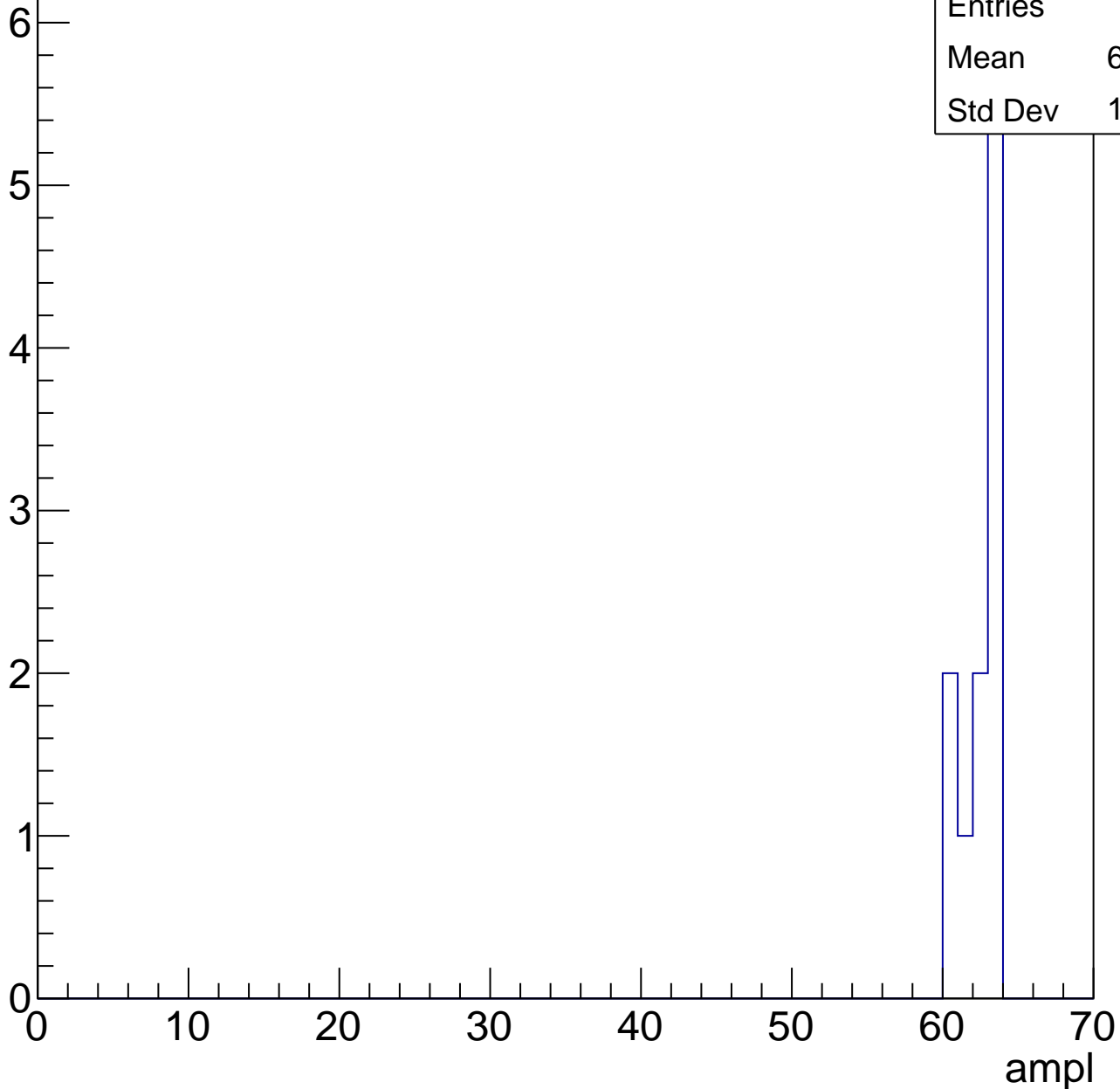


# B1L102S, U3-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	11
Mean	62.09
Std Dev	1.164

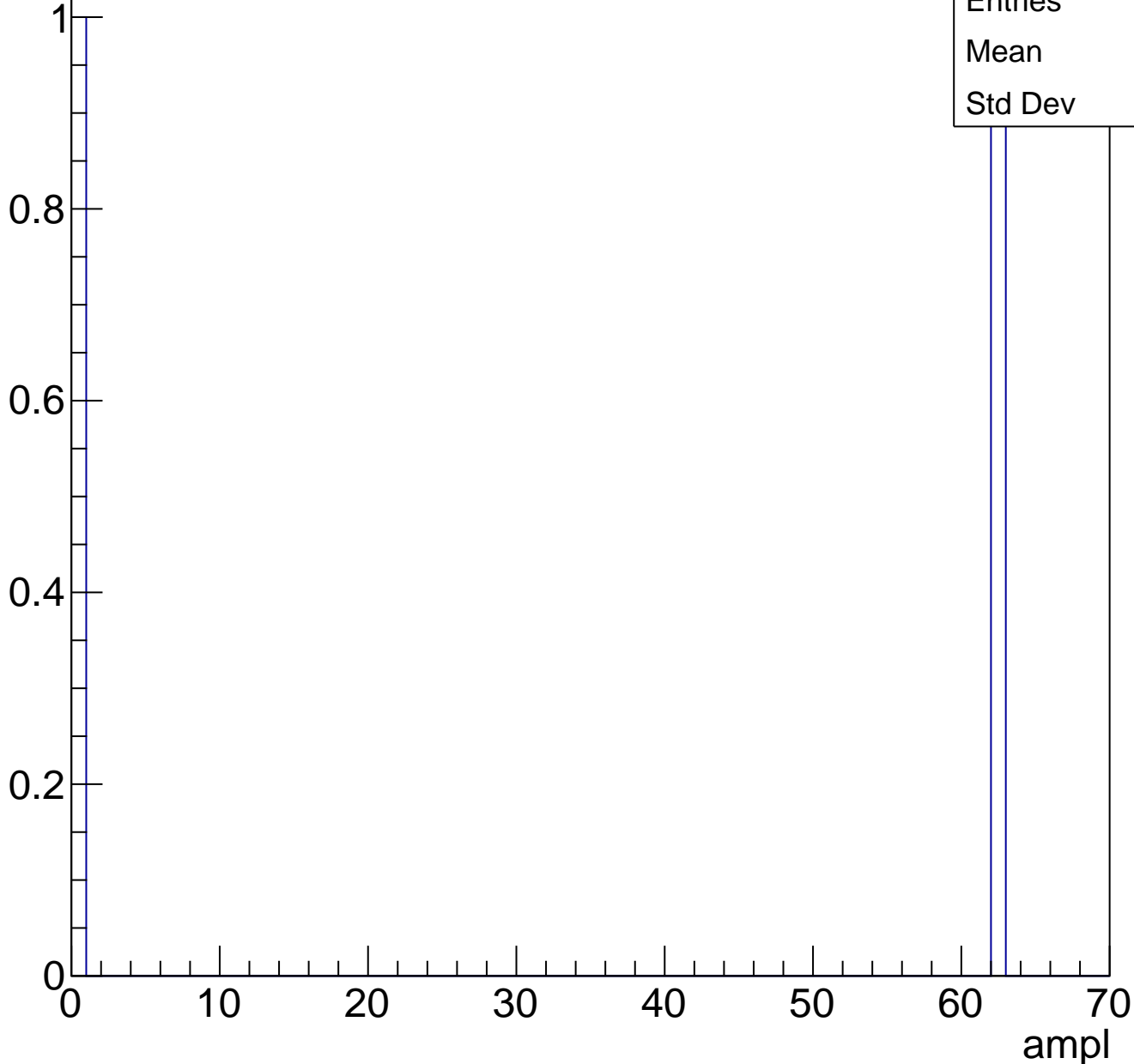




# B1L102S, U3-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch29, adc0

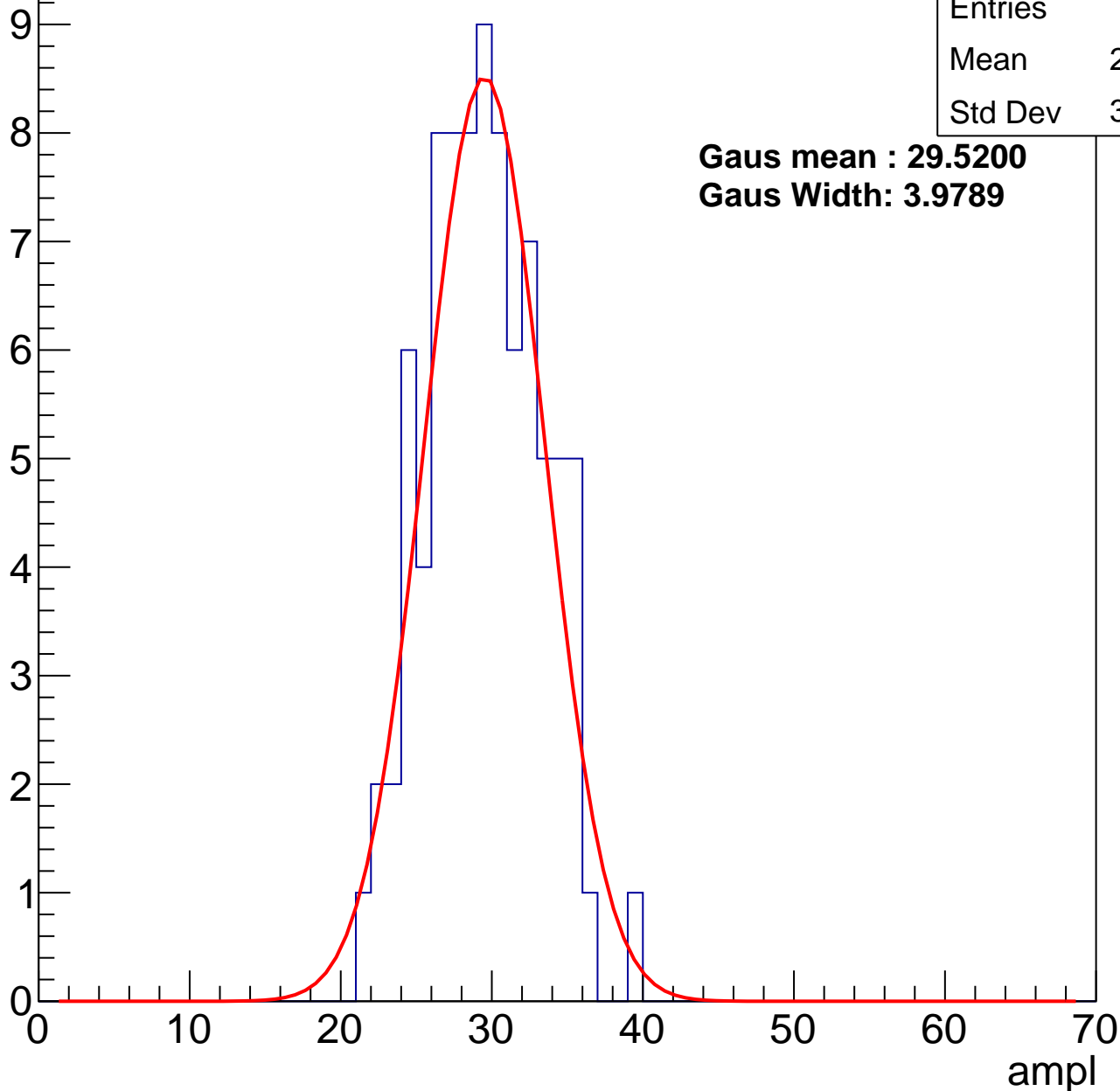
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	86
Mean	29.06
Std Dev	3.718

**Gaus mean : 29.5200**

**Gaus Width: 3.9789**



# B1L102S, U3-ch29, adc1

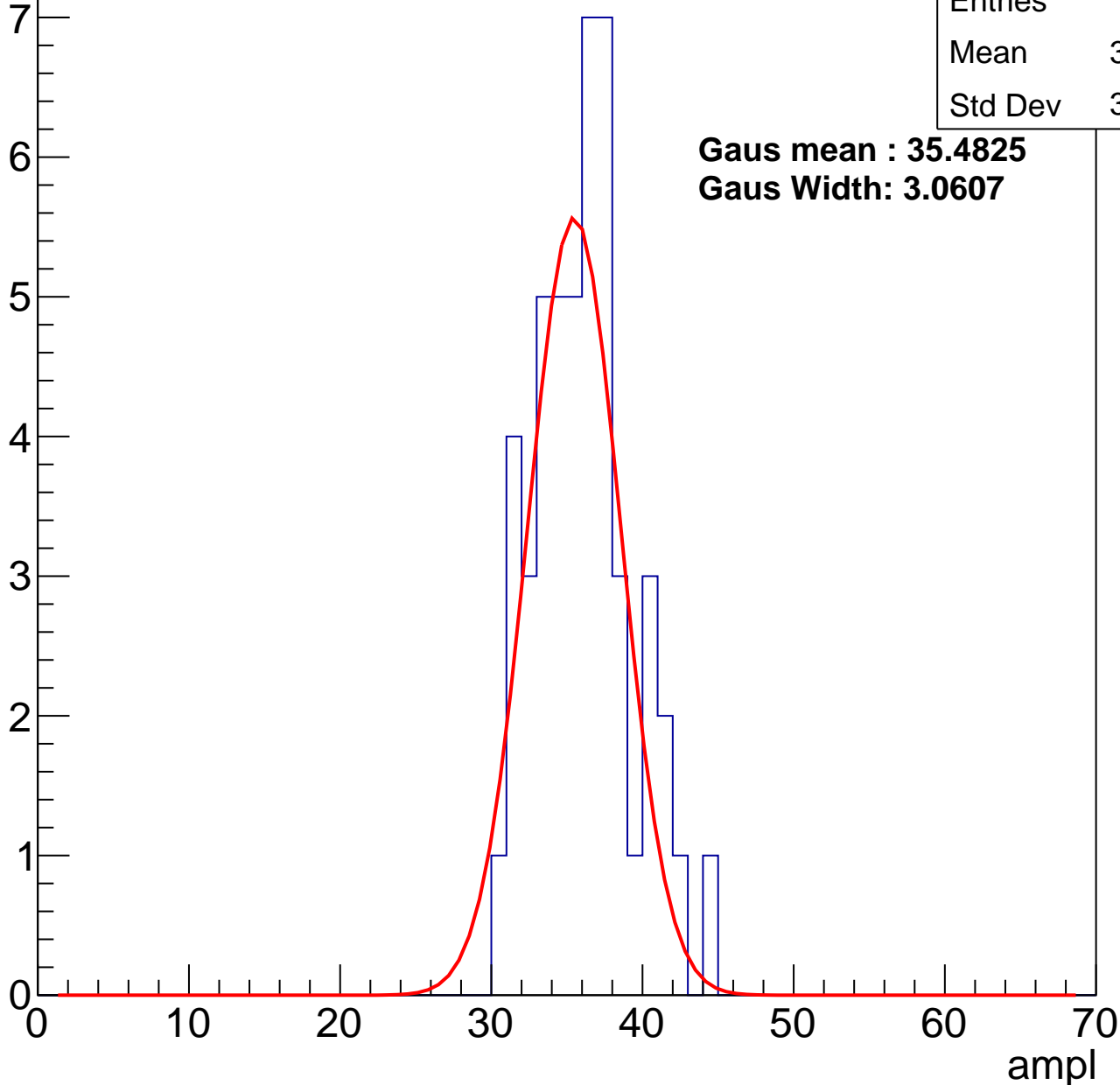
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	35.67
Std Dev	3.145

**Gaus mean : 35.4825**

**Gaus Width: 3.0607**



# B1L102S, U3-ch29, adc2

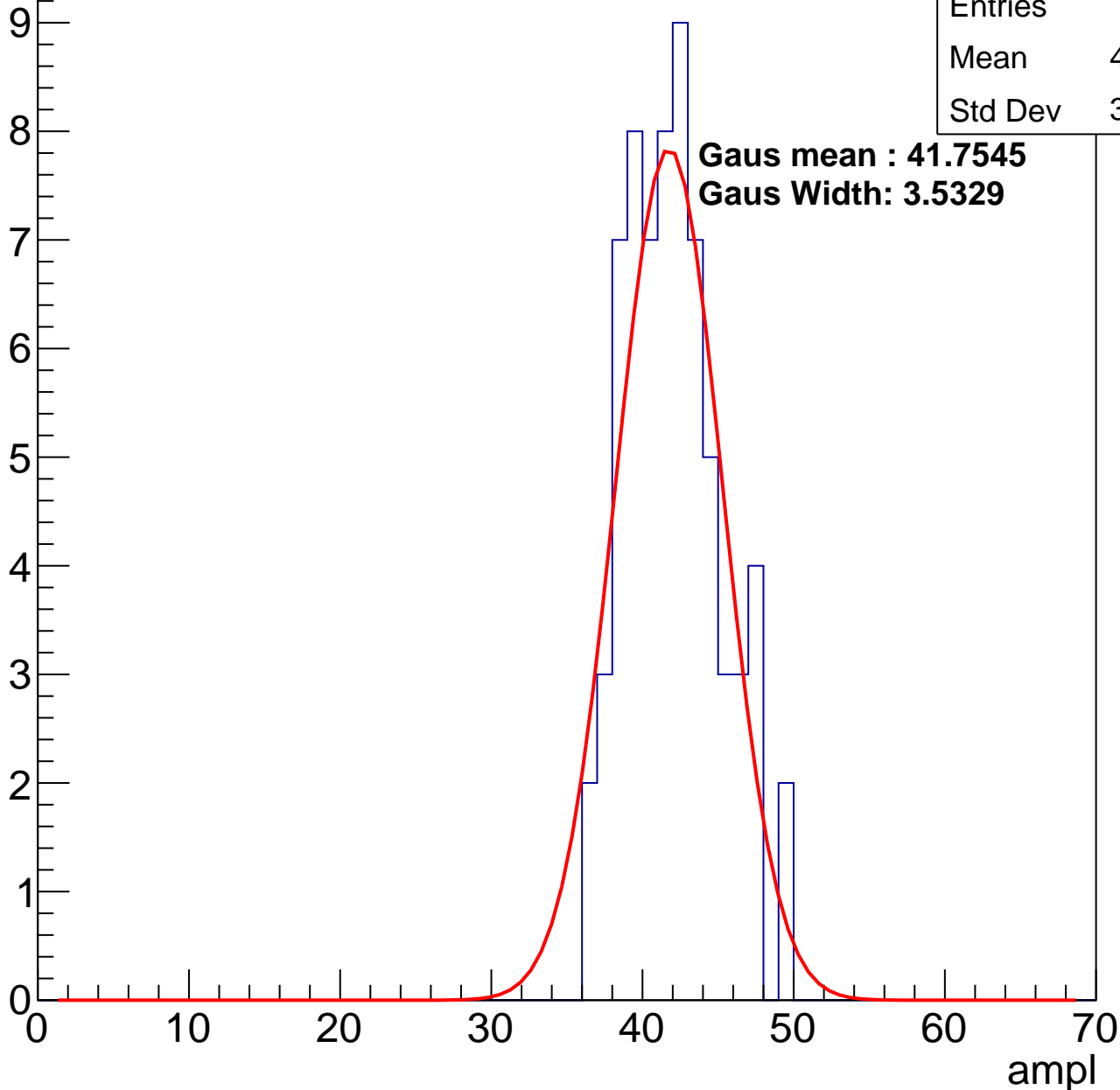
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	41.57
Std Dev	3.103

**Gaus mean : 41.7545**

**Gaus Width: 3.5329**

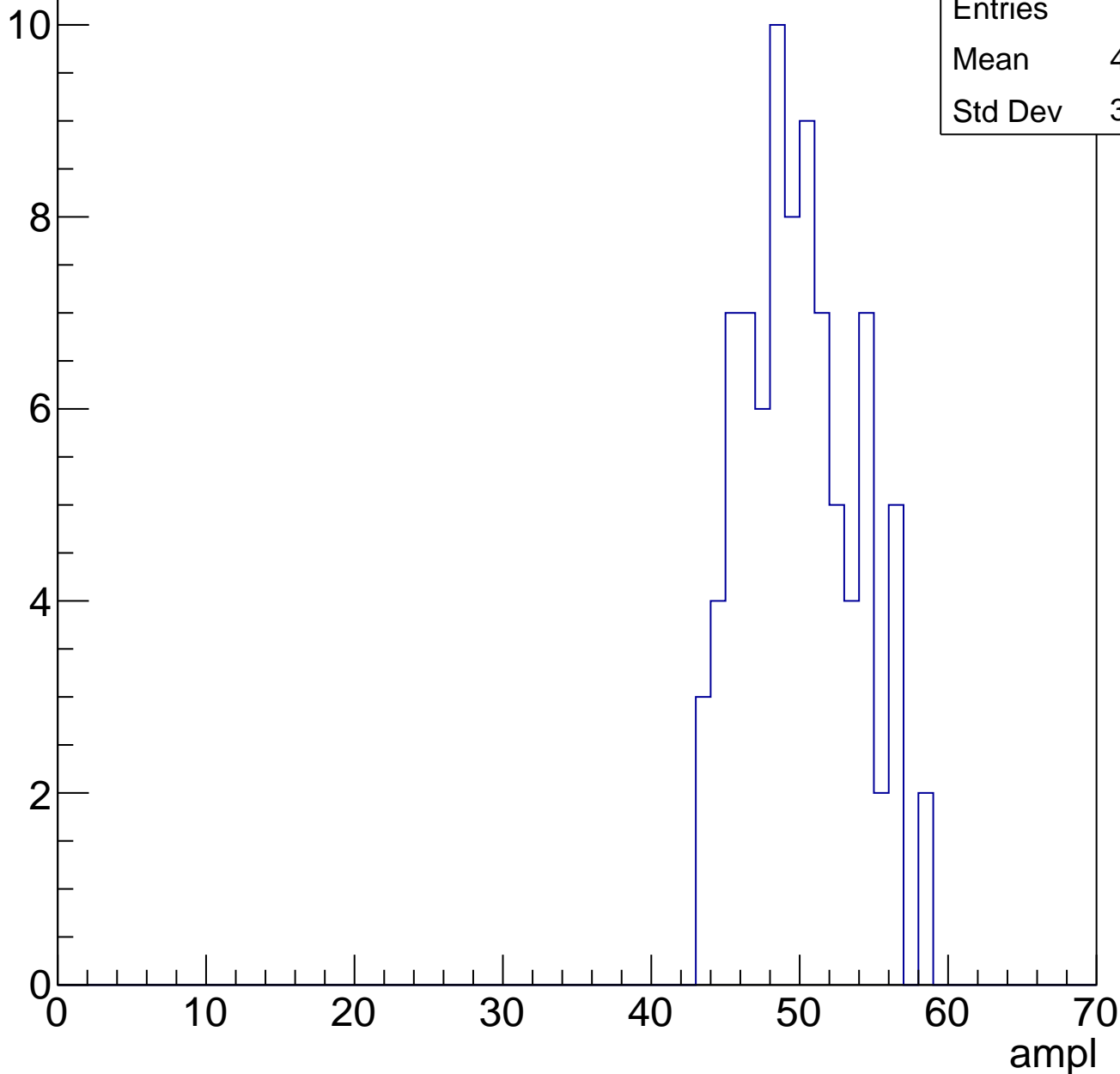


# B1L102S, U3-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	86
Mean	49.52
Std Dev	3.725

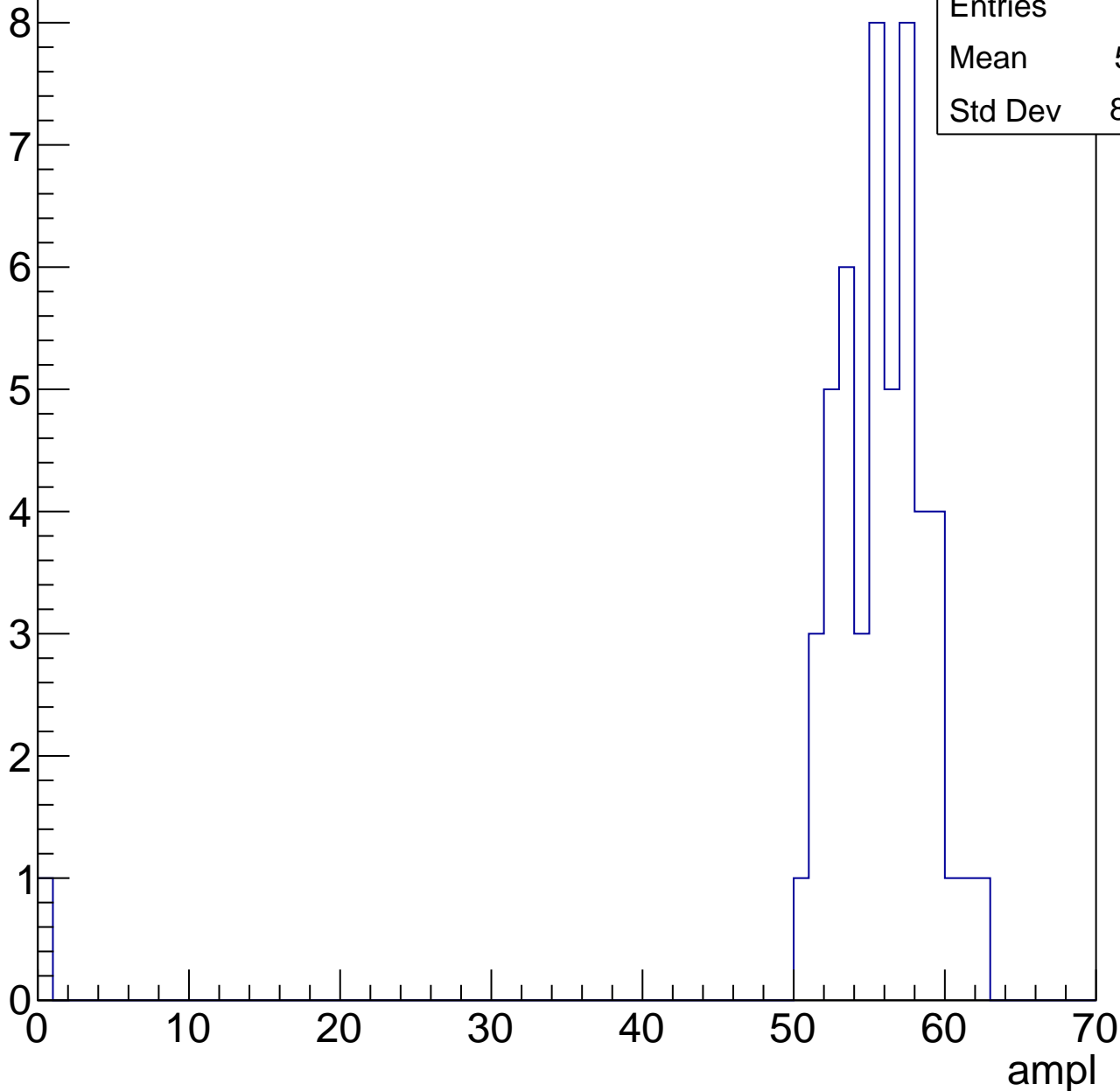


# B1L102S, U3-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

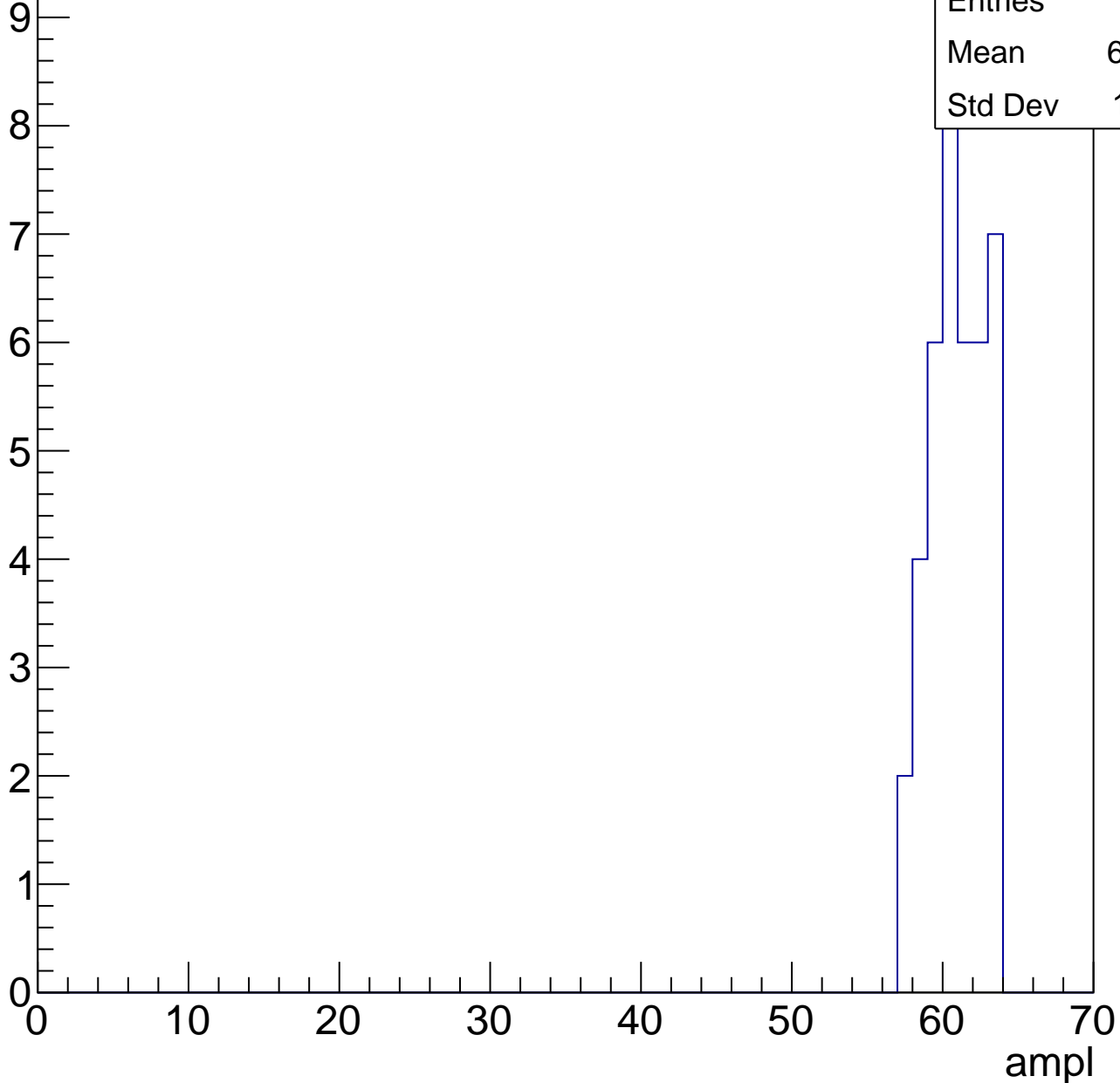
Entries	51
Mean	54.31
Std Dev	8.157



# B1L102S, U3-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	40
Mean	60.48
Std Dev	1.761

# B1L102S, U3-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

8

Mean

61.88

Std Dev

0.7806



# B1L102S, U3-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch30, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	87
Mean	28.24
Std Dev	4.878

**Gaus mean : 28.8911**

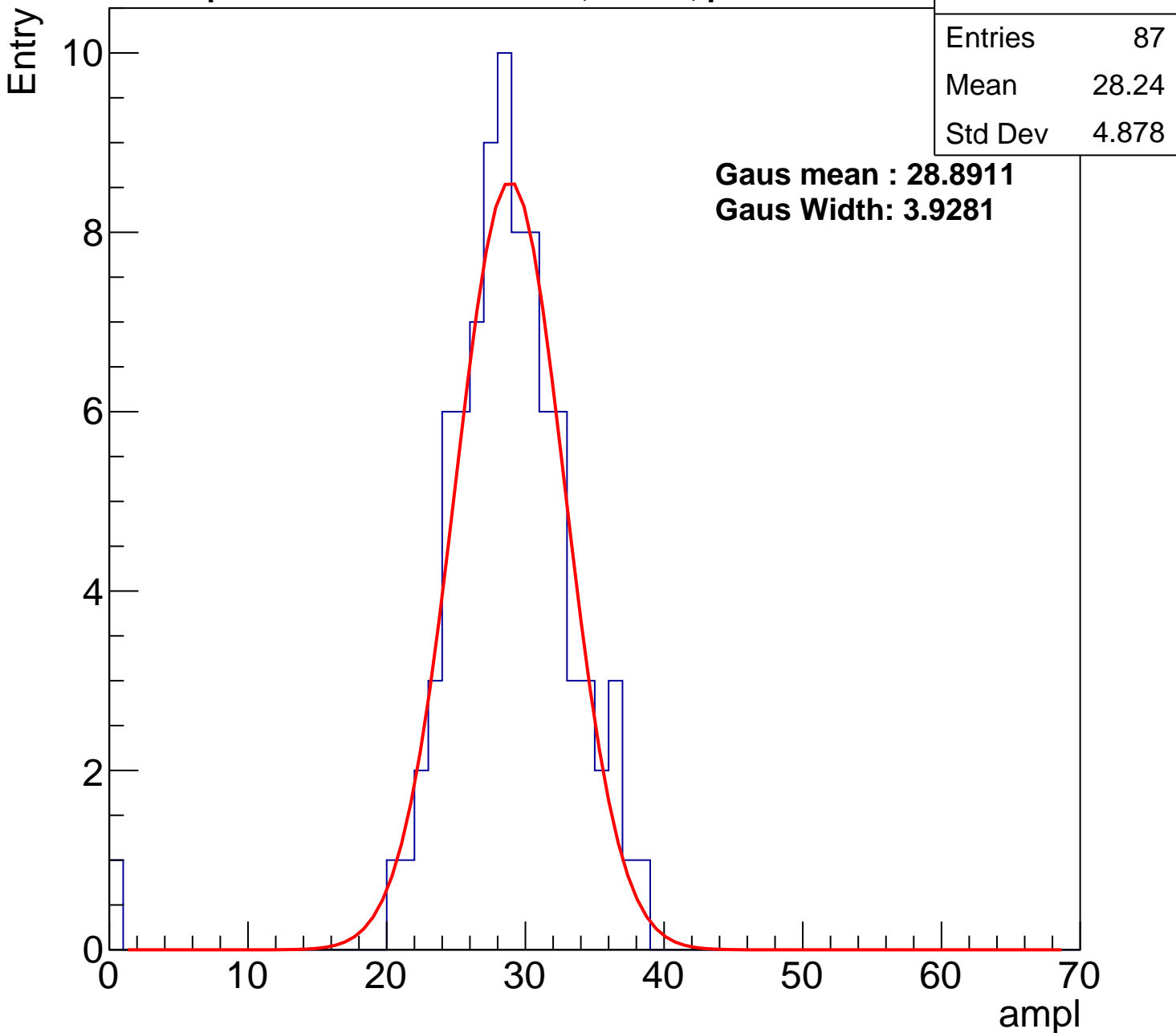
**Gaus Width: 3.9281**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U3-ch30, adc1

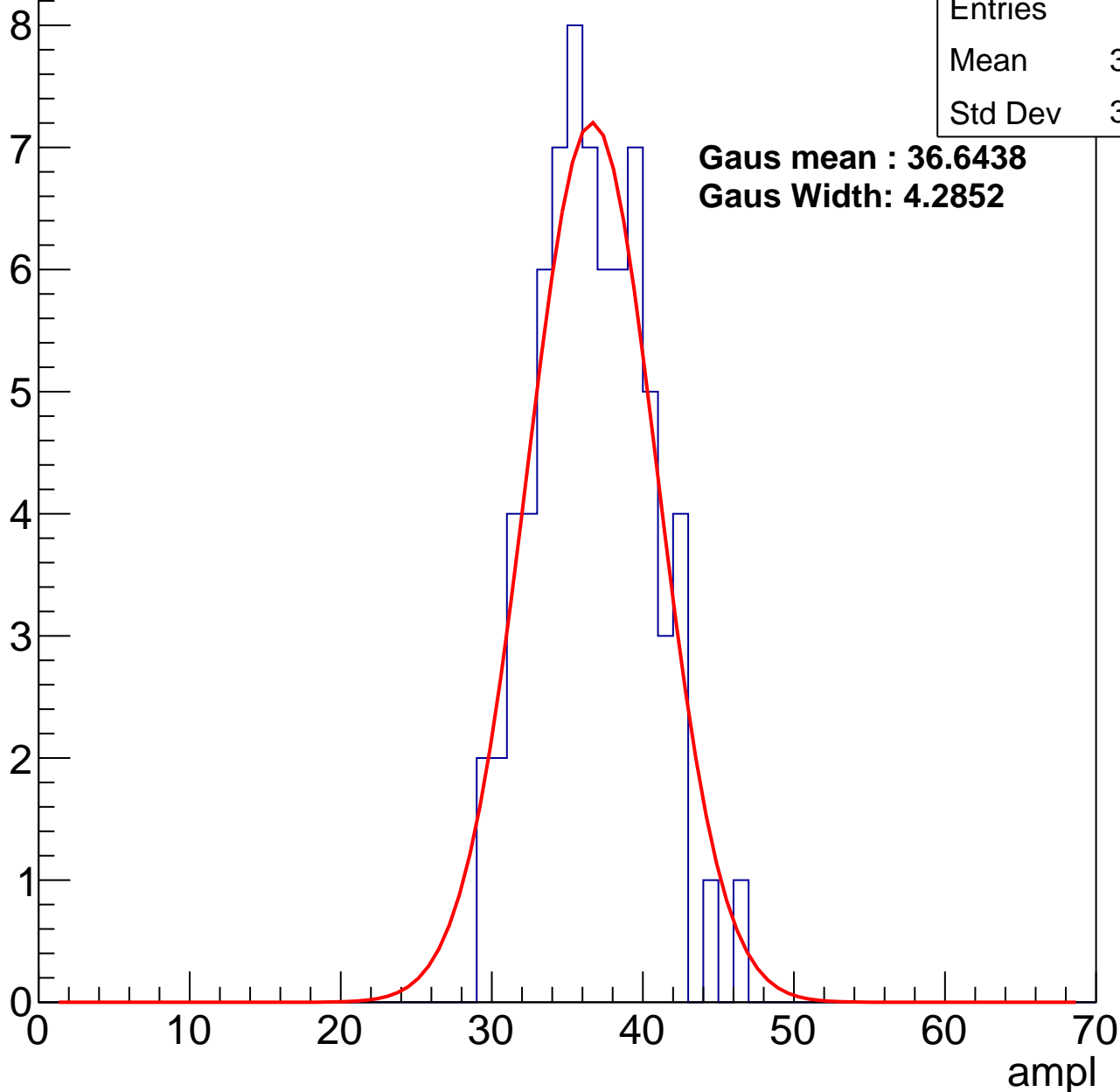
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	36.19
Std Dev	3.659

**Gaus mean : 36.6438**

**Gaus Width: 4.2852**



# B1L102S, U3-ch30, adc2

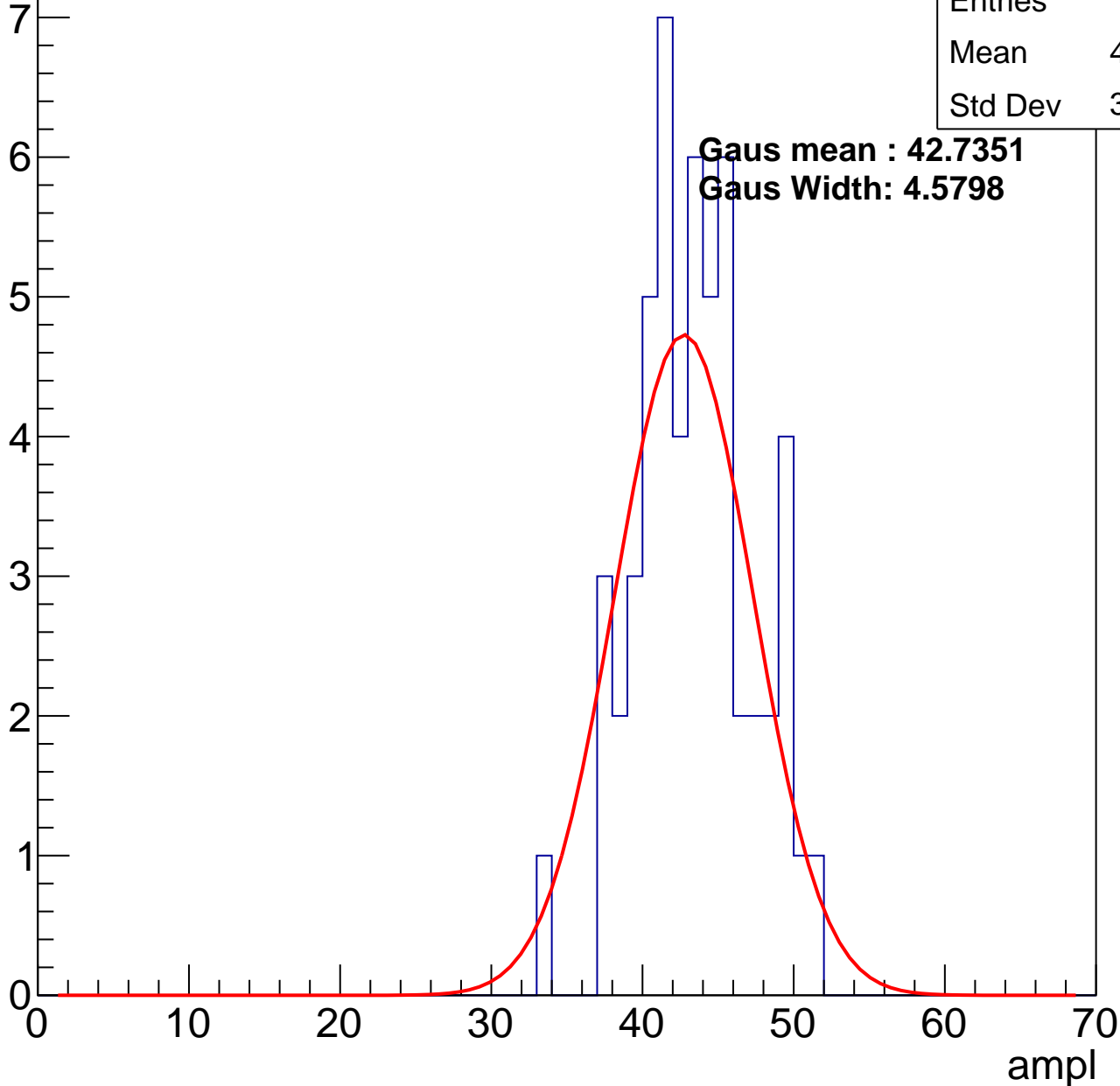
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	42.94
Std Dev	3.773

**Gaus mean : 42.7351**

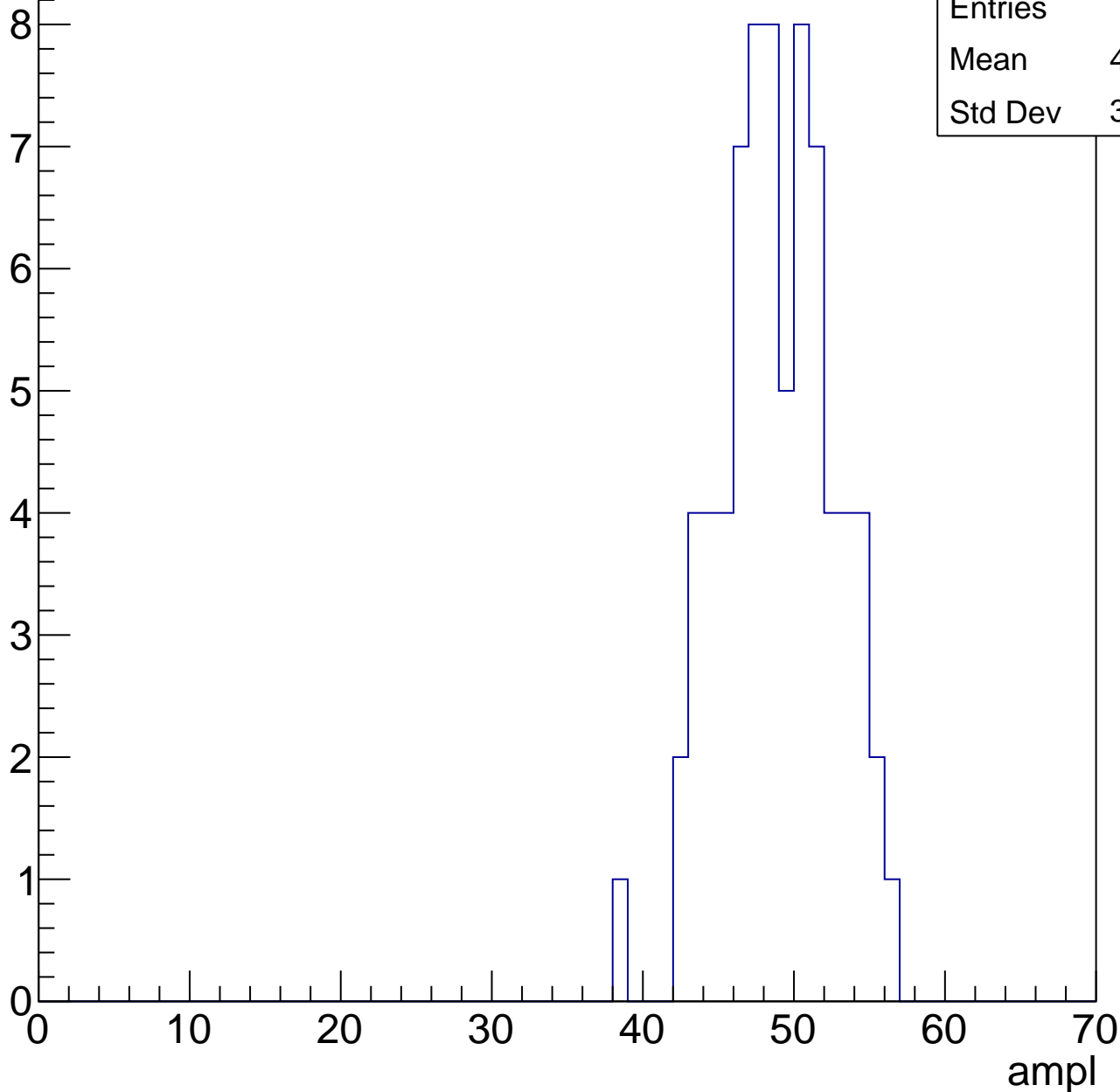
**Gaus Width: 4.5798**



# B1L102S, U3-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch30, adc4

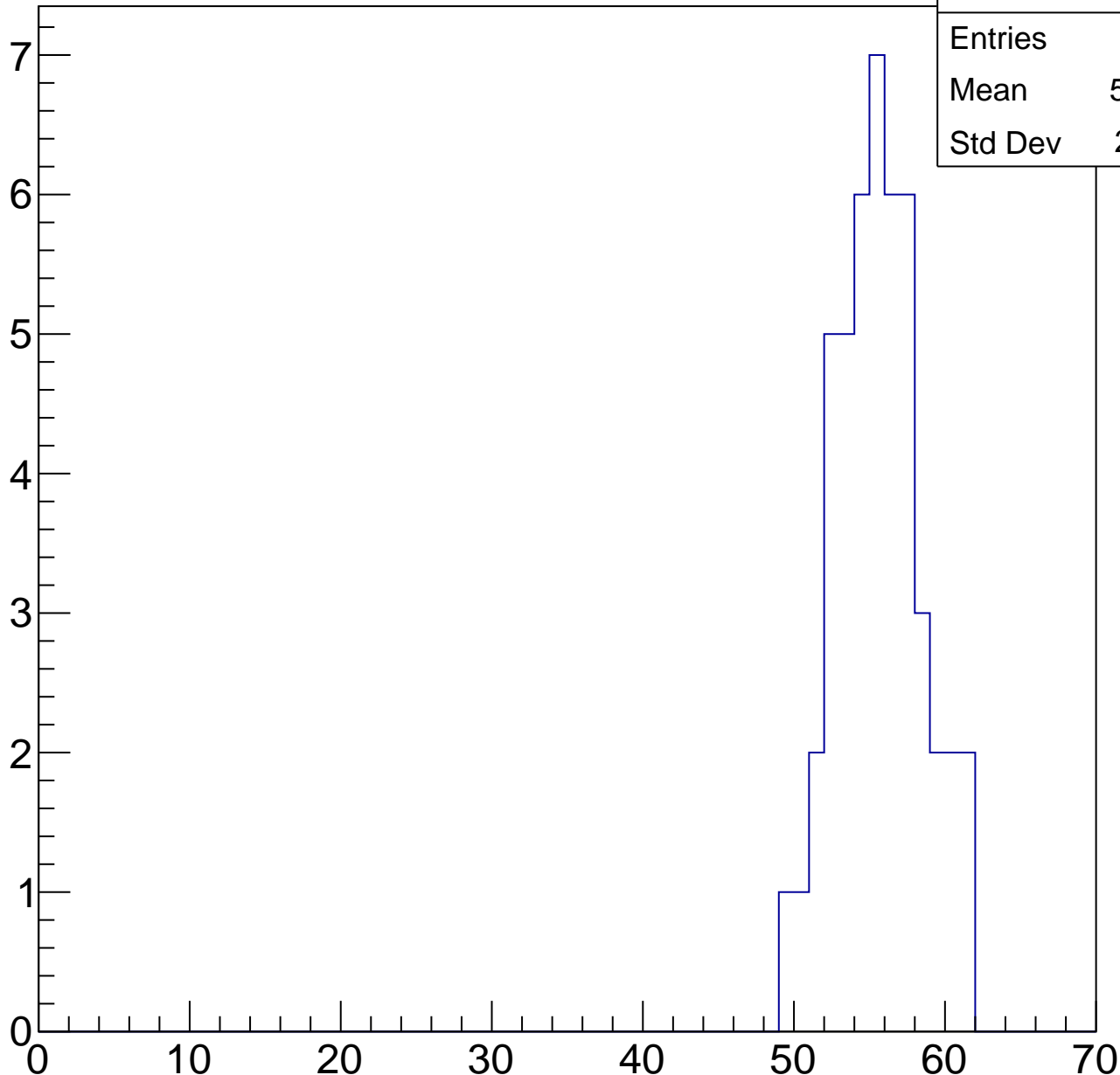
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	55.15
Std Dev	2.791

ampl

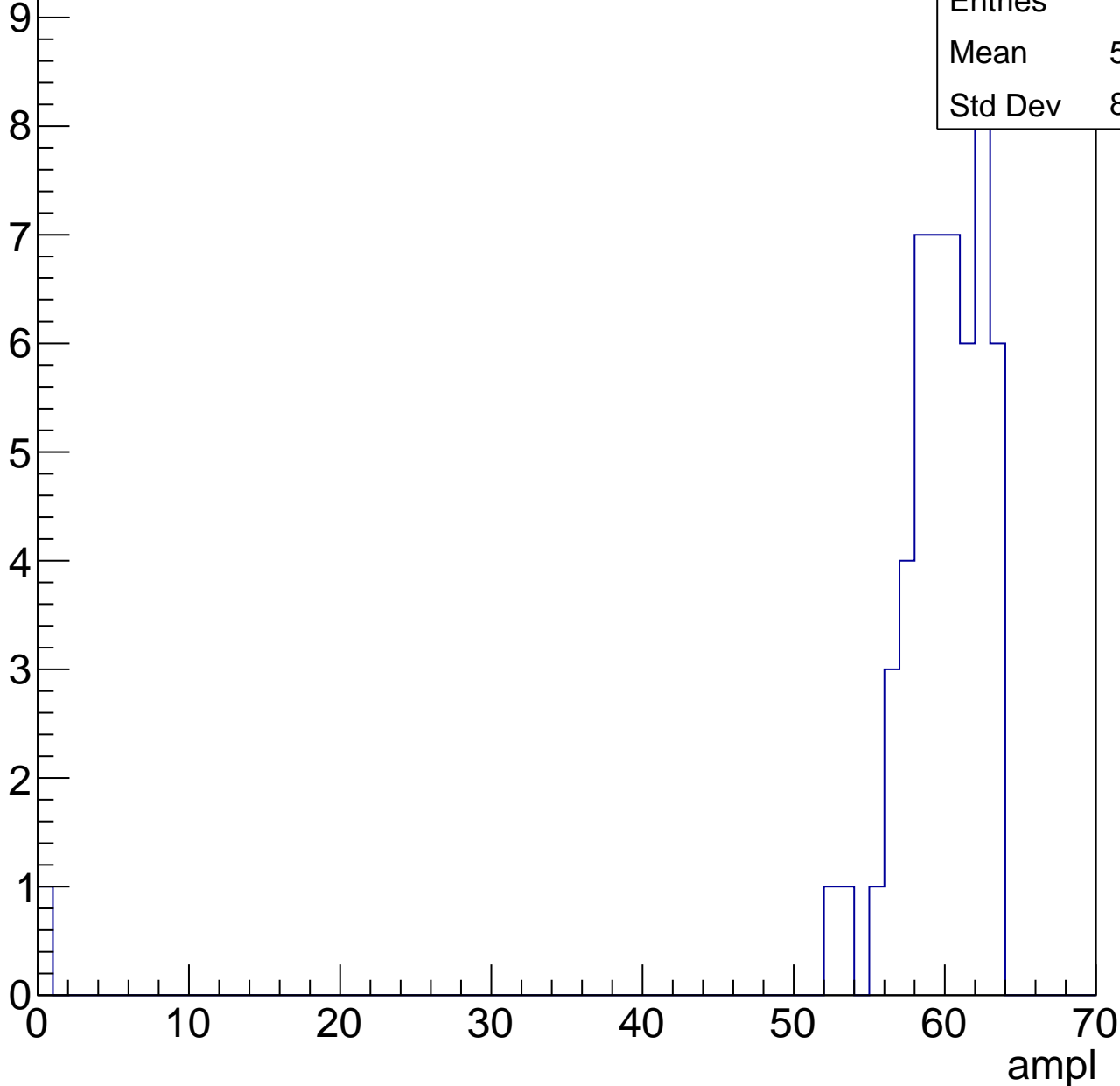


# B1L102S, U3-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	58.43
Std Dev	8.493



# B1L102S, U3-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

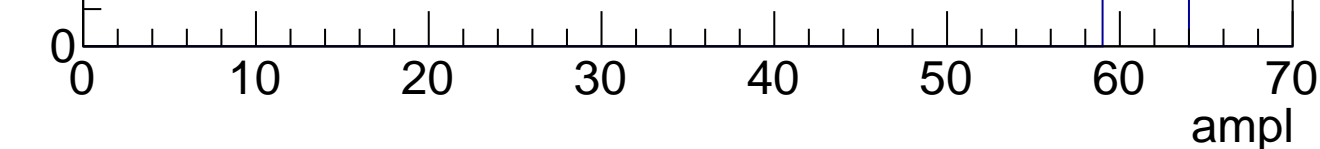
8

Mean

61.5

Std Dev

1.414





# B1L102S, U3-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch31, adc0

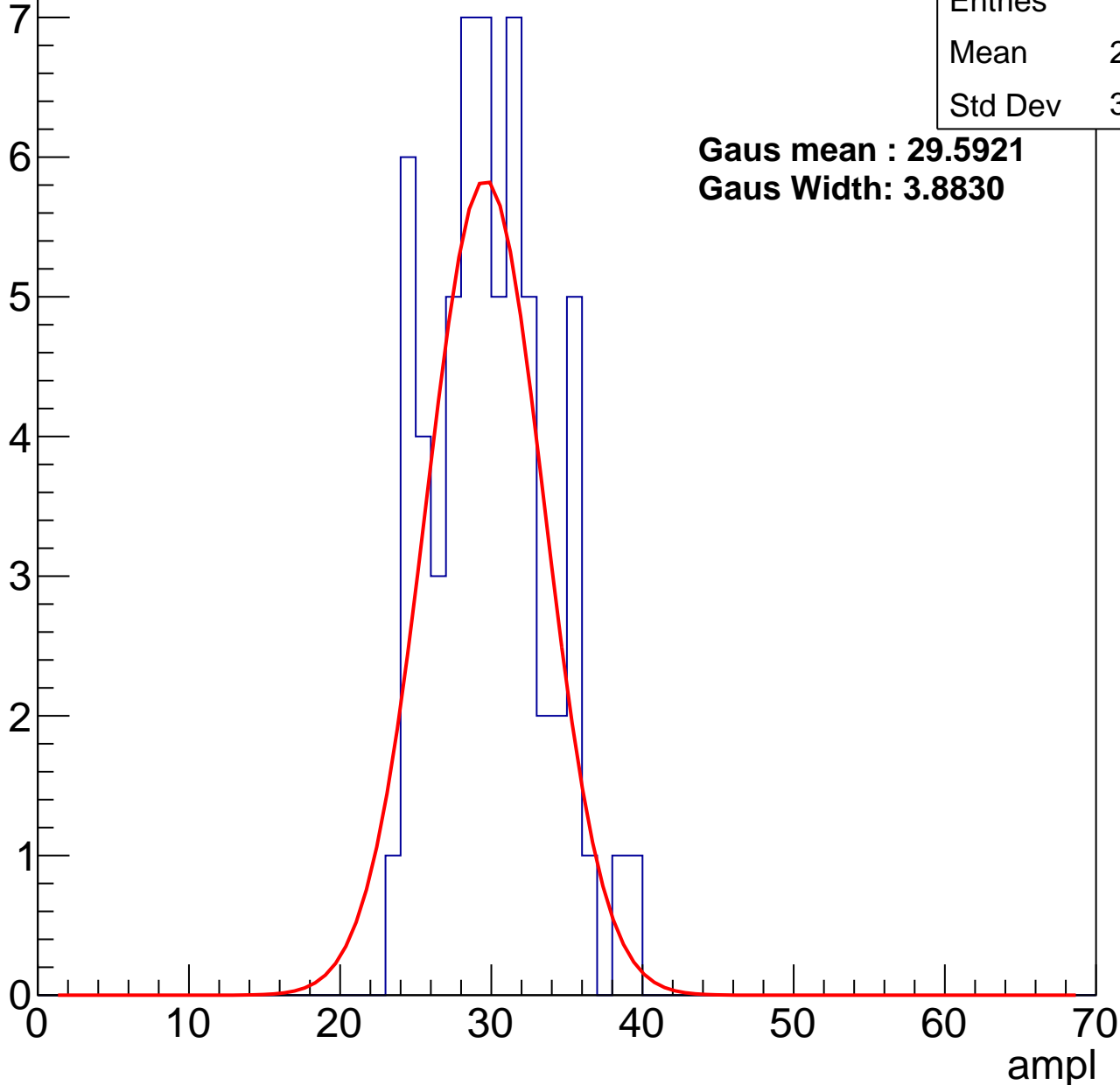
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	29.48
Std Dev	3.723

**Gaus mean : 29.5921**

**Gaus Width: 3.8830**



# B1L102S, U3-ch31, adc1

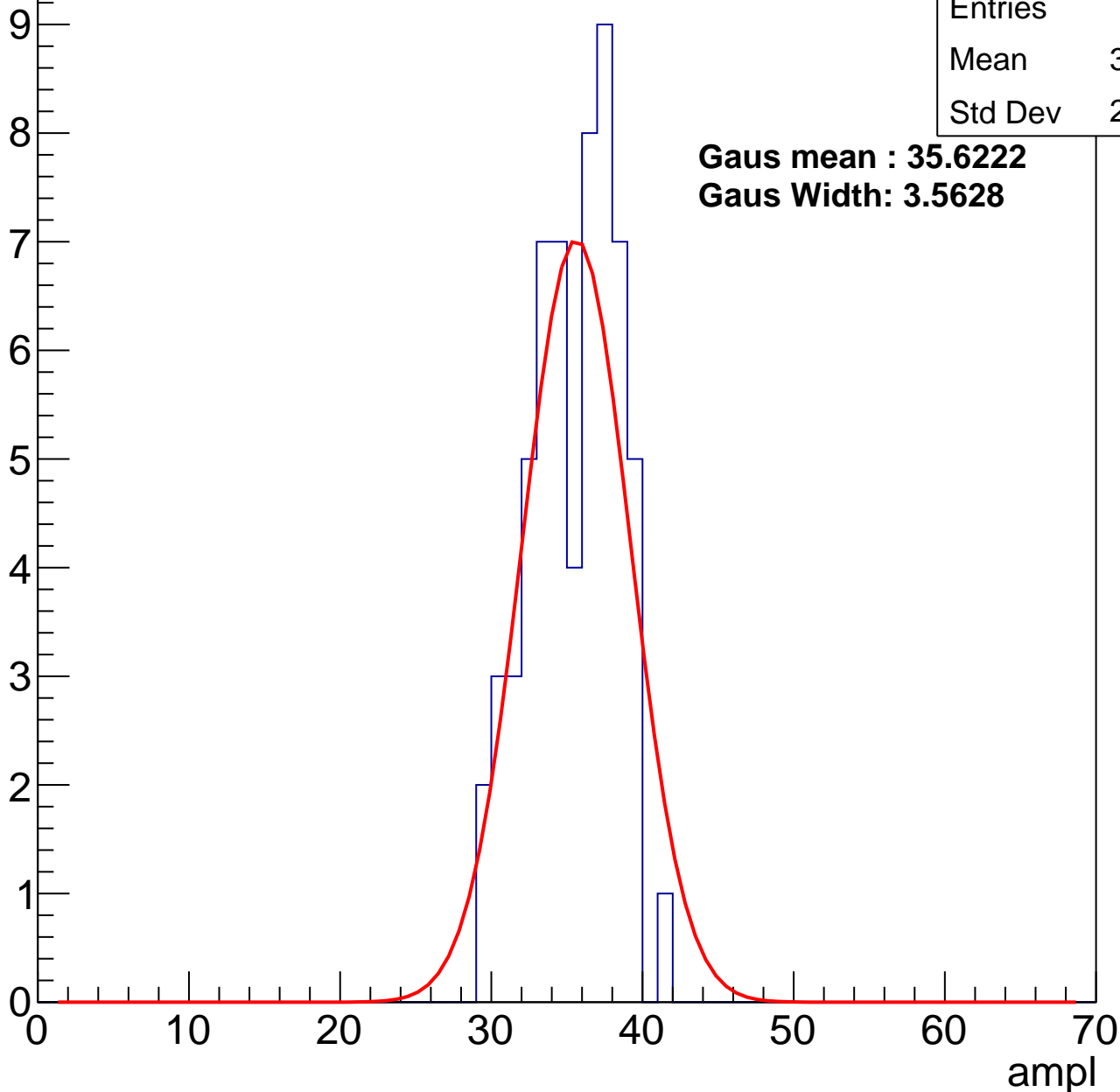
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	34.97
Std Dev	2.857

**Gaus mean : 35.6222**

**Gaus Width: 3.5628**



# B1L102S, U3-ch31, adc2

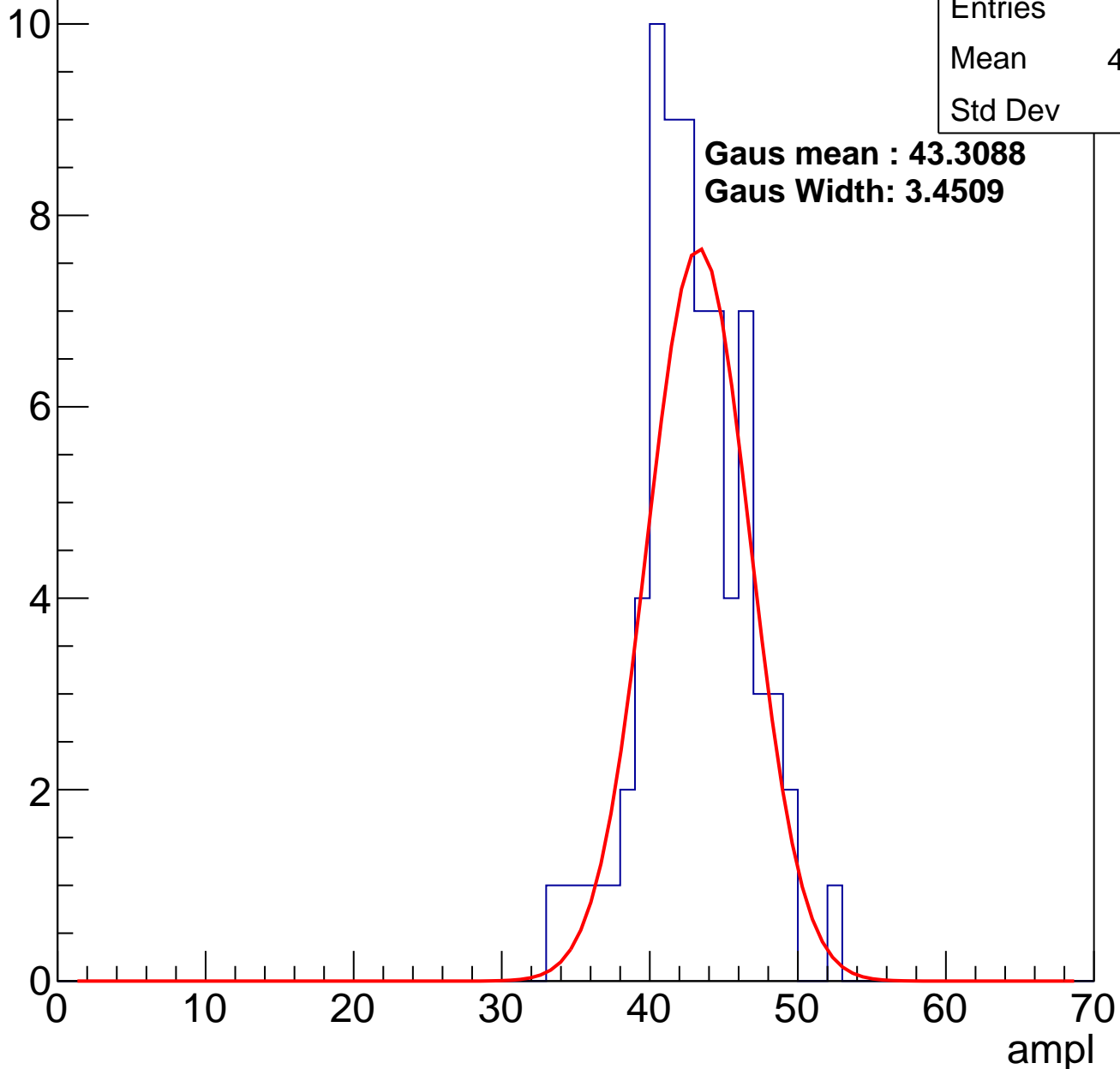
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	73
Mean	42.47
Std Dev	3.55

**Gaus mean : 43.3088**

**Gaus Width: 3.4509**

Entry

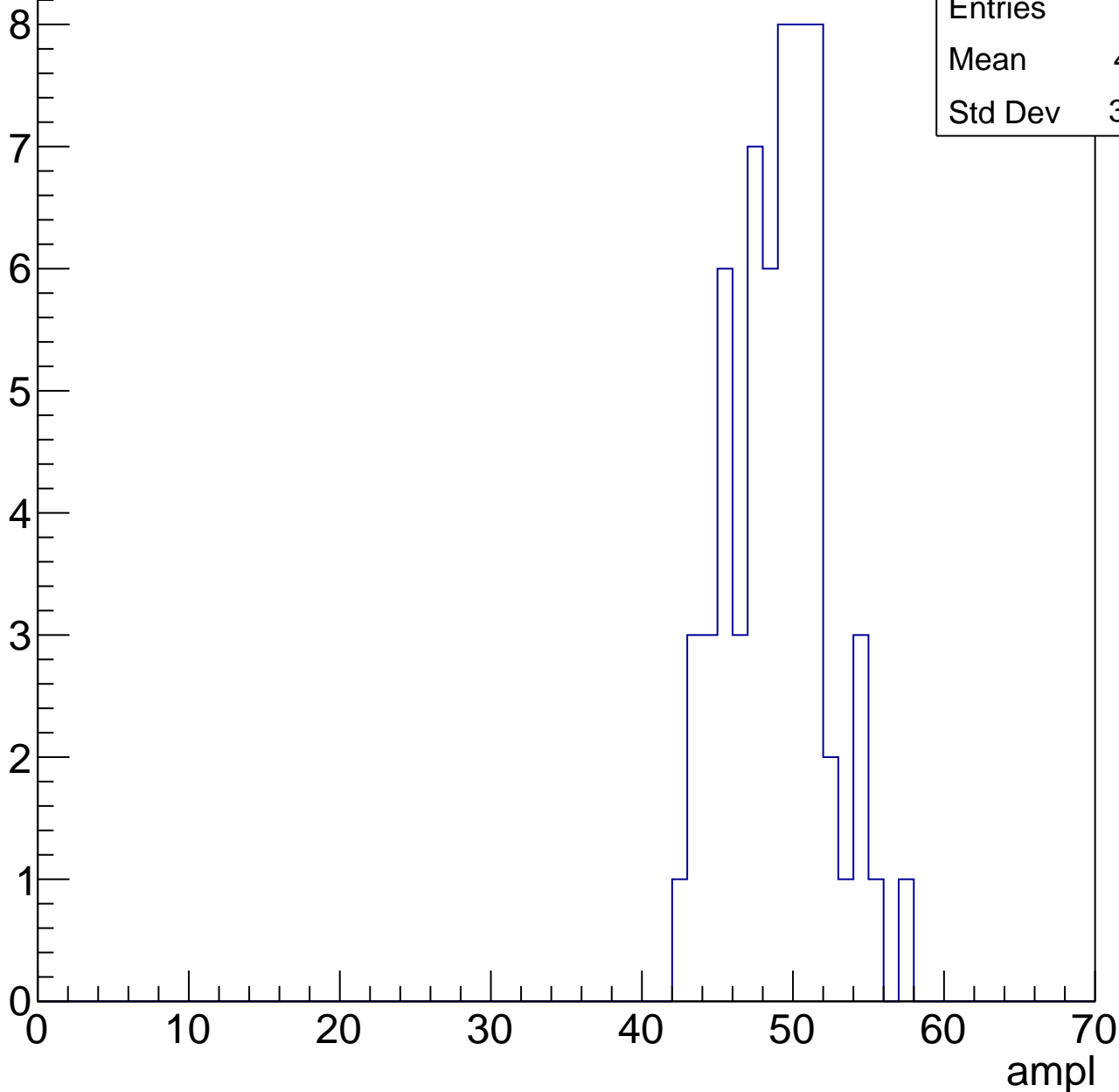


# B1L102S, U3-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	48.51
Std Dev	3.196

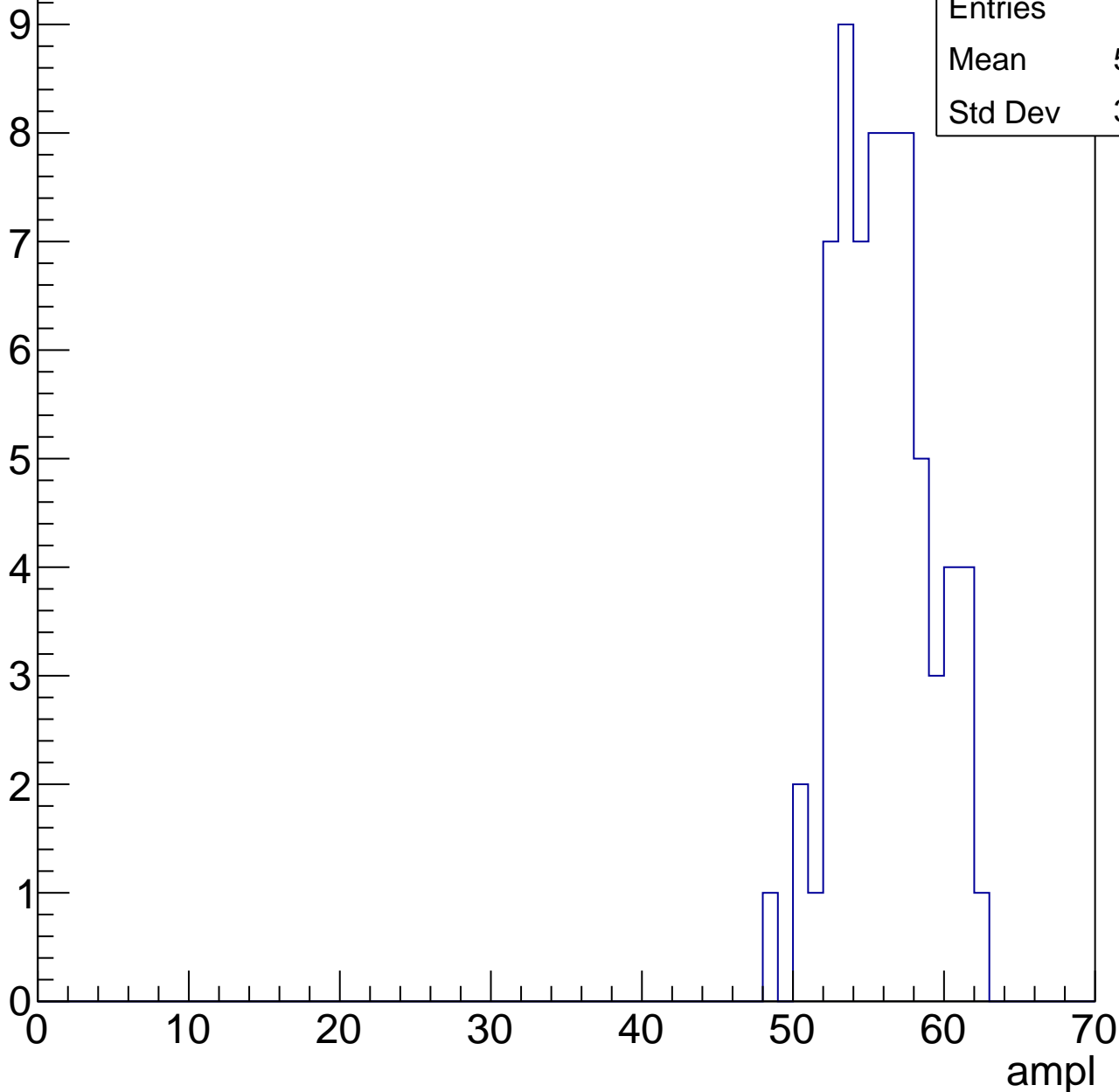


# B1L102S, U3-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	55.51
Std Dev	3.041

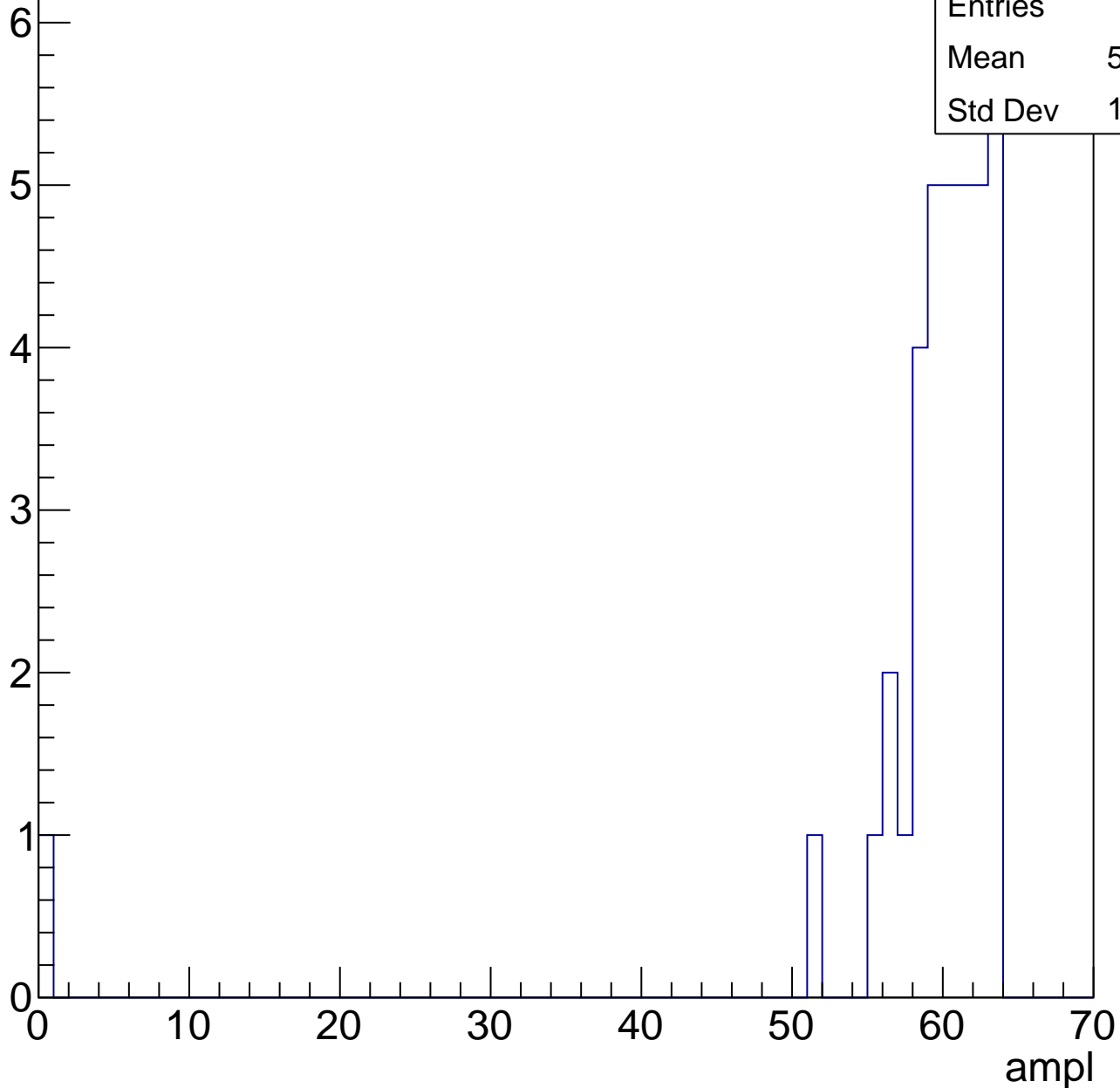


# B1L102S, U3-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

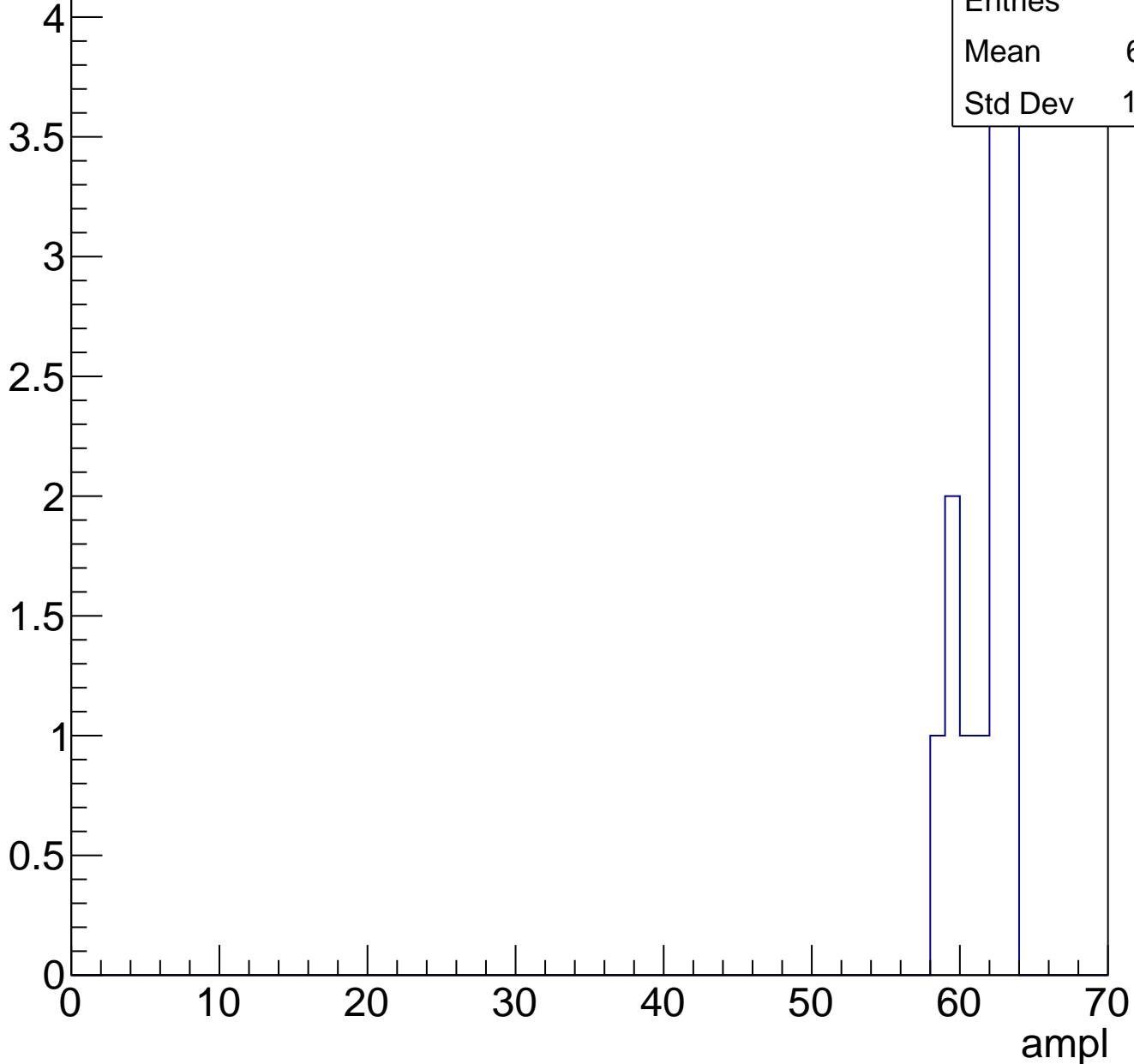
Entries	36
Mean	58.19
Std Dev	10.18



# B1L102S, U3-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch32, adc0

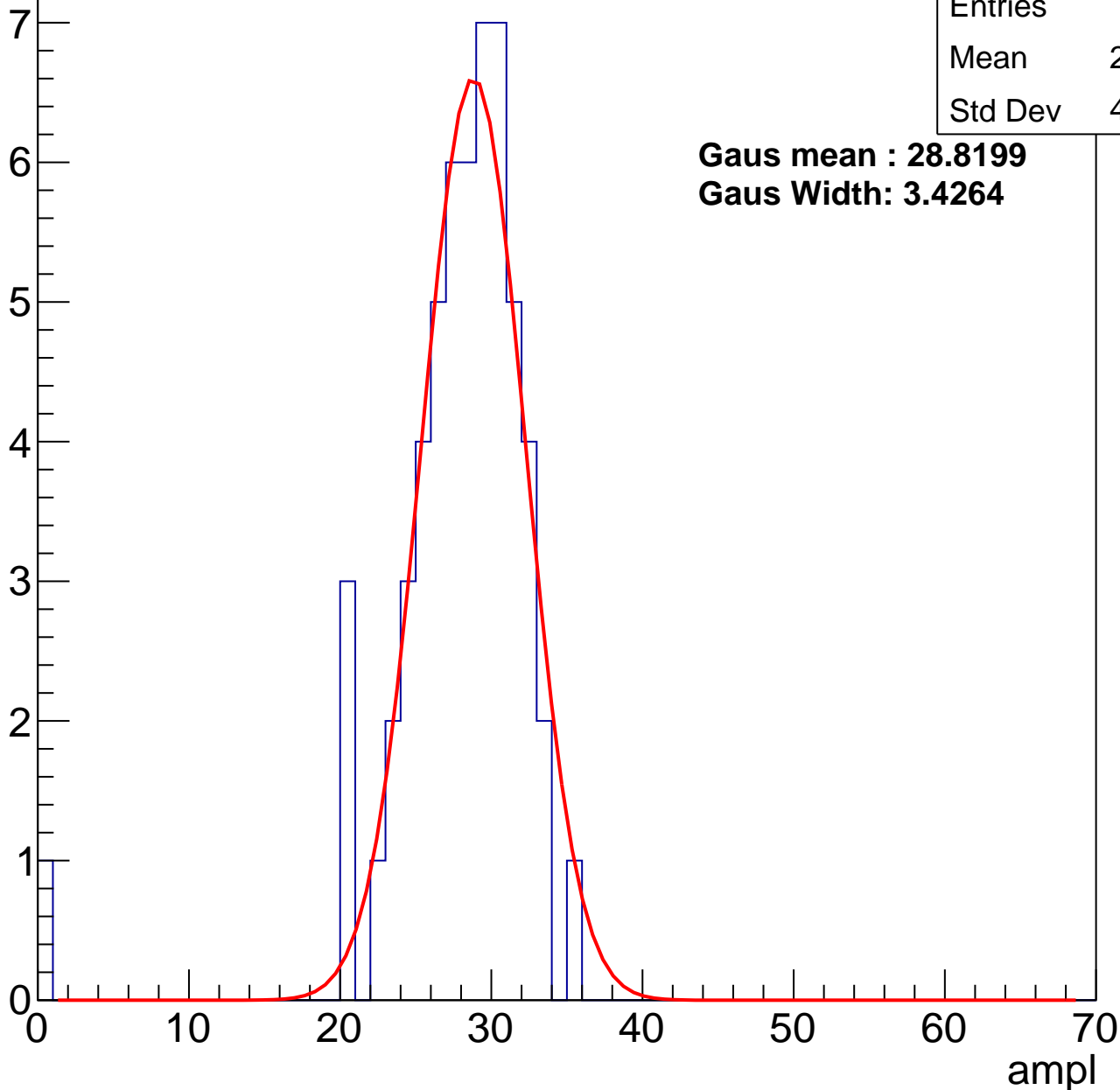
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	27.32
Std Dev	4.935

**Gaus mean : 28.8199**

**Gaus Width: 3.4264**



# B1L102S, U3-ch32, adc1

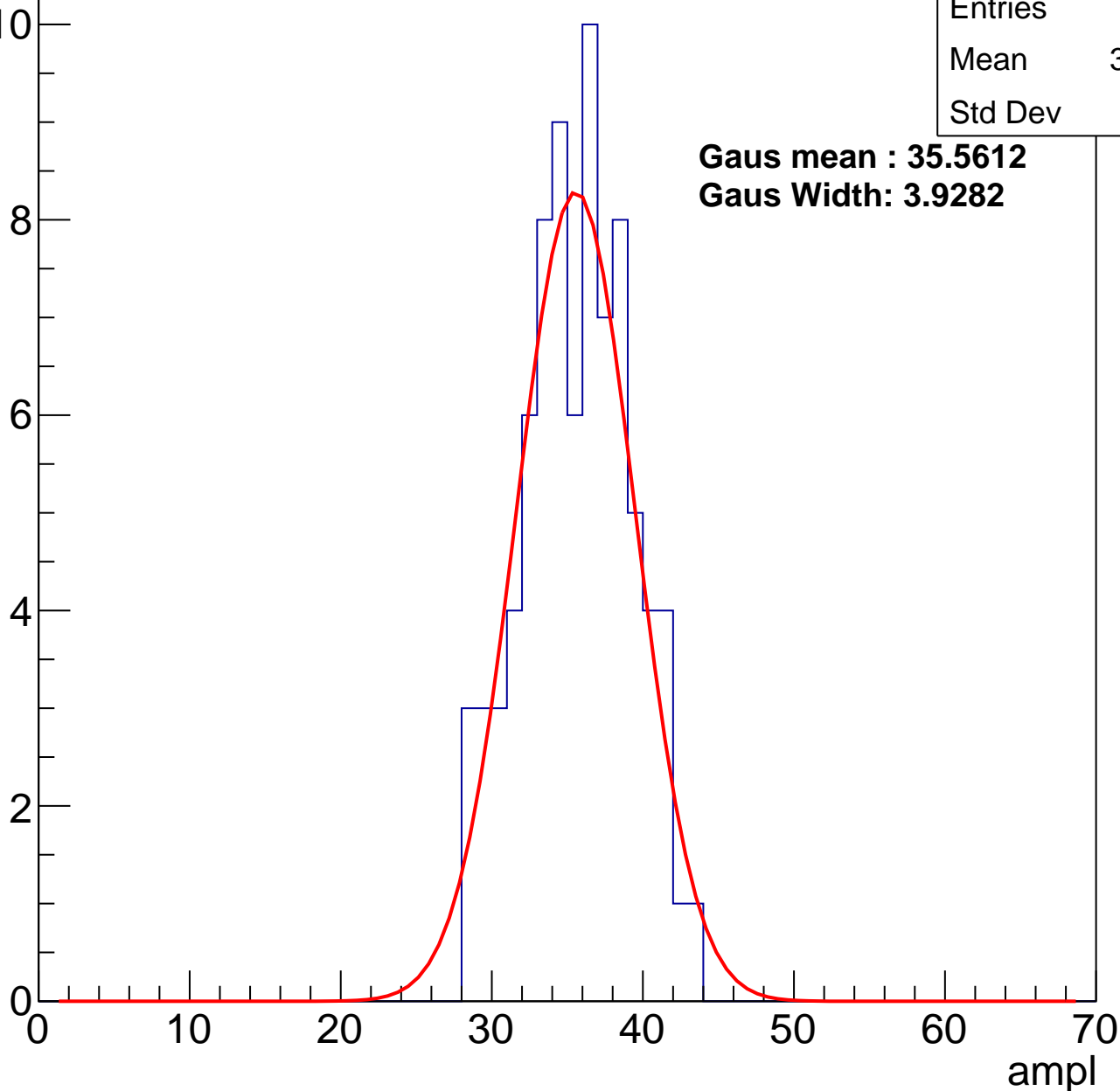
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	35.17
Std Dev	3.55

**Gaus mean : 35.5612**

**Gaus Width: 3.9282**



# B1L102S, U3-ch32, adc2

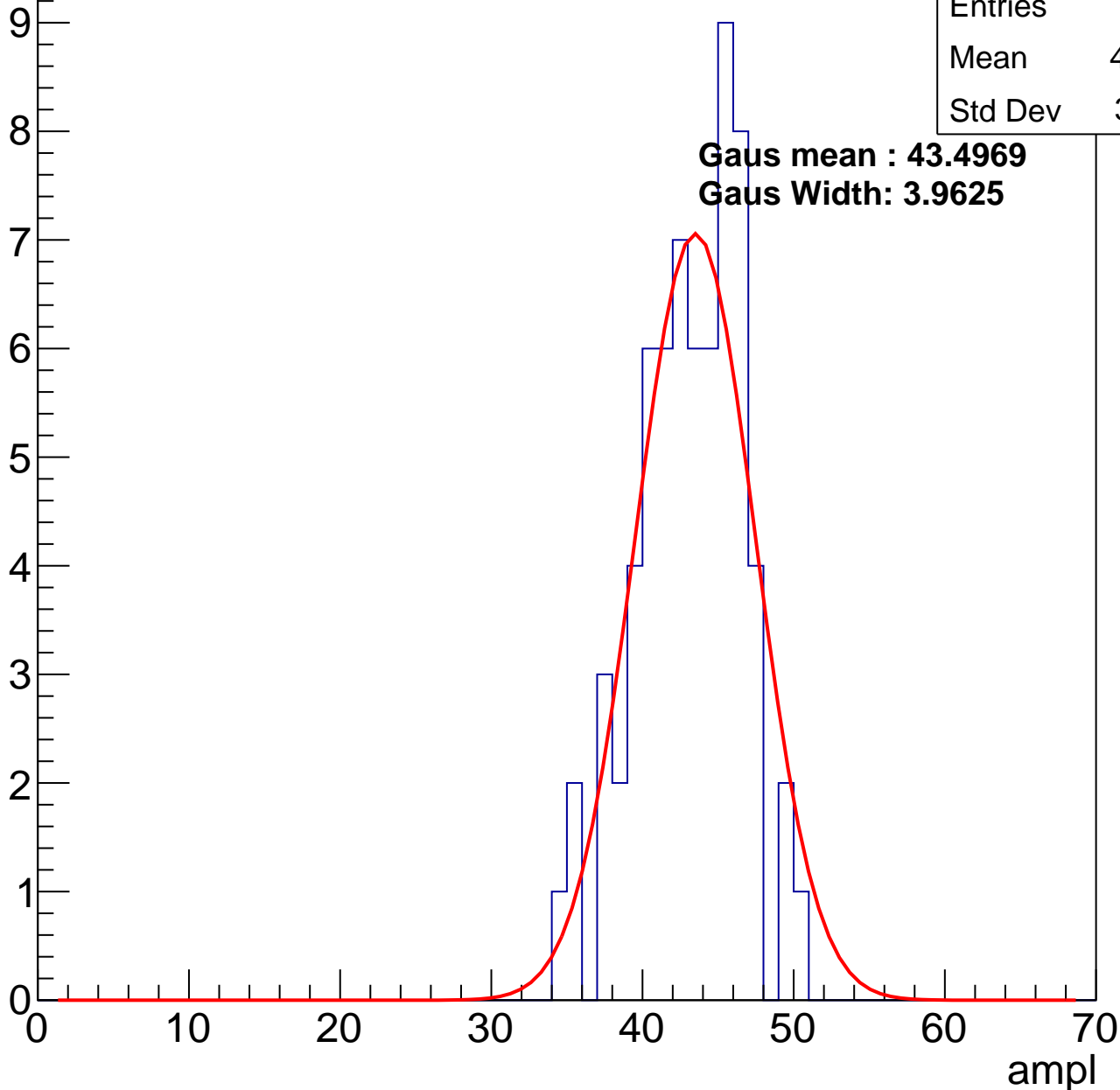
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	42.66
Std Dev	3.471

**Gaus mean : 43.4969**

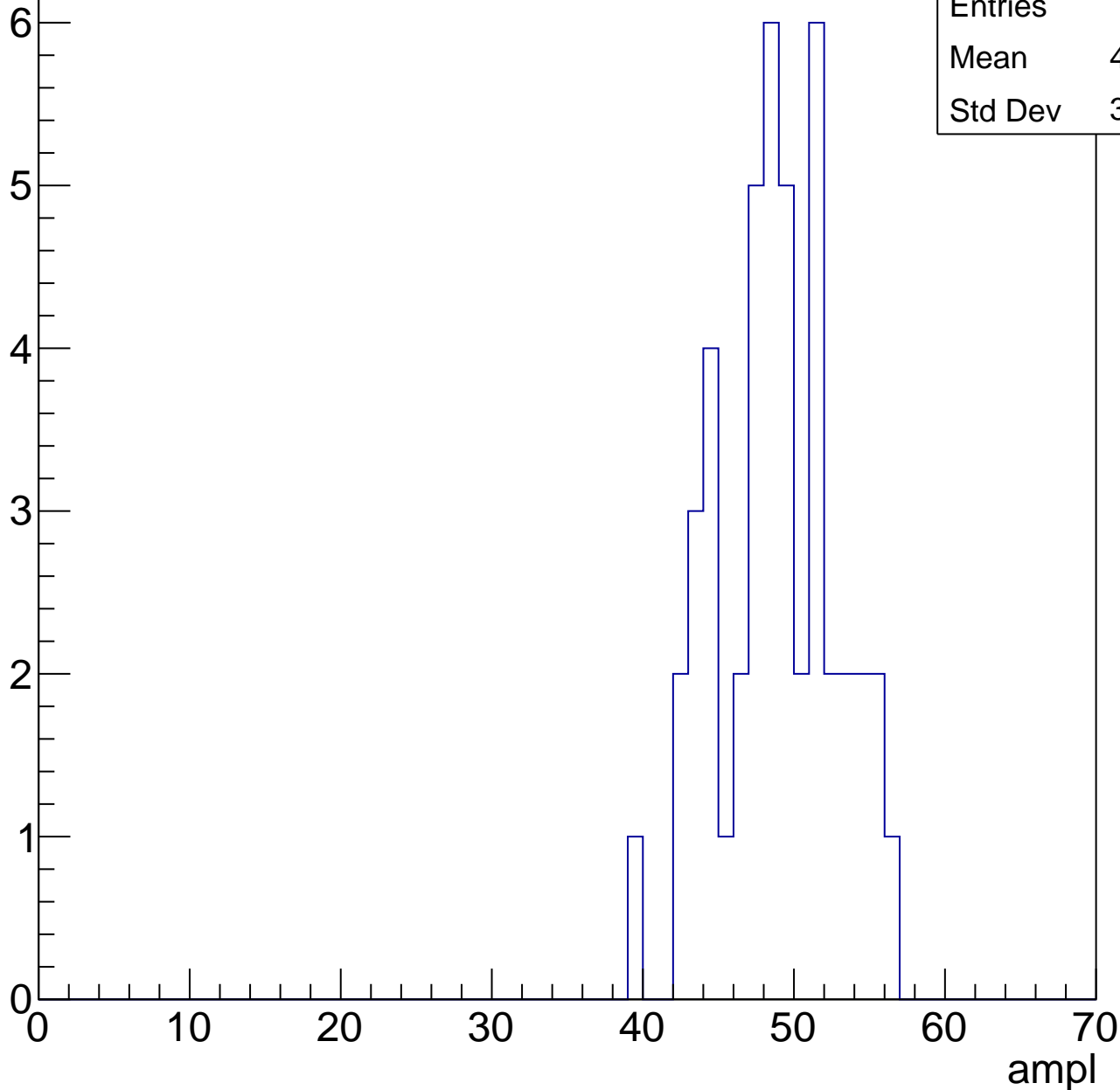
**Gaus Width: 3.9625**



# B1L102S, U3-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

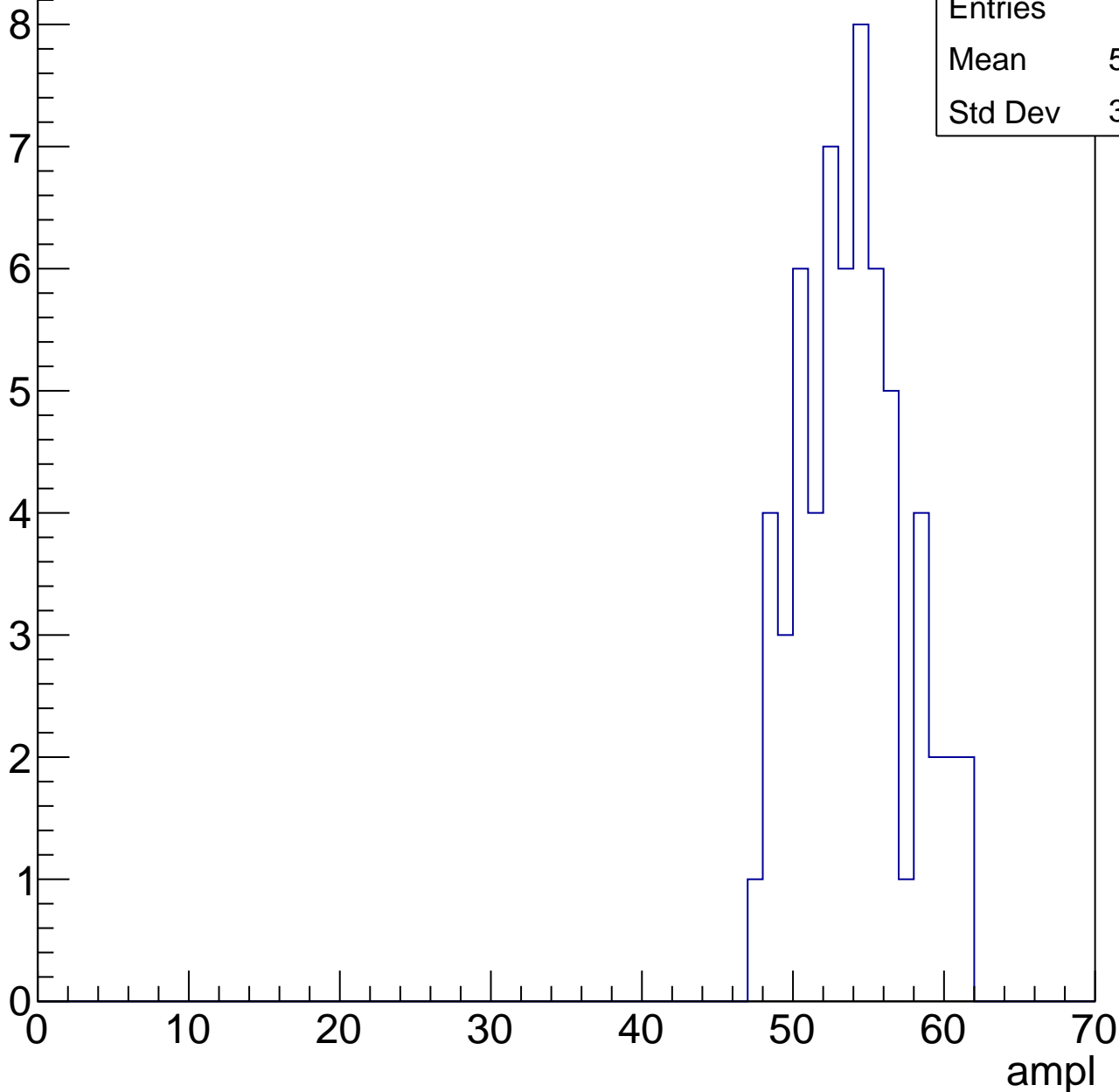


# B1L102S, U3-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

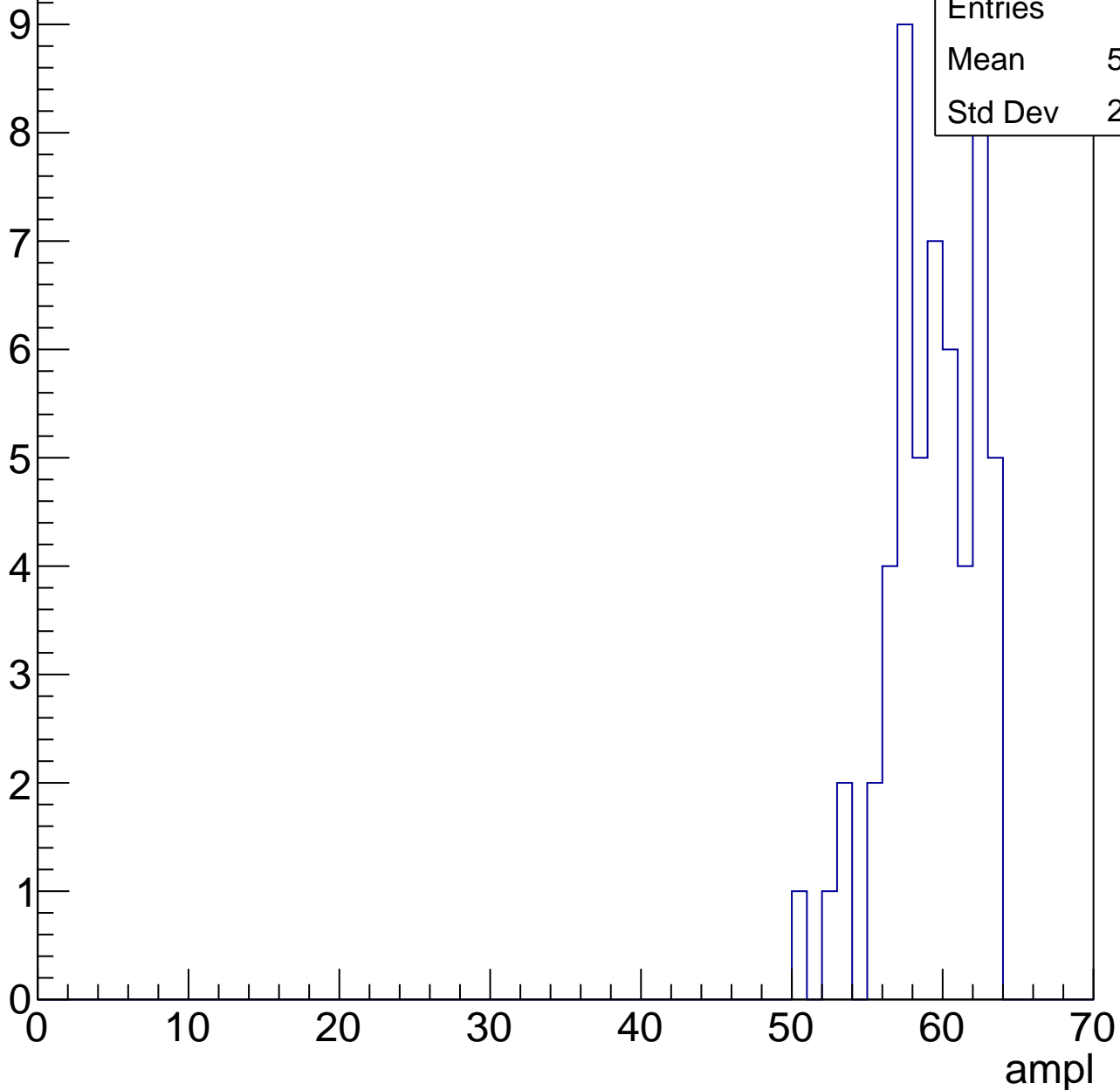
Entries	61
Mean	53.49
Std Dev	3.476



# B1L102S, U3-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

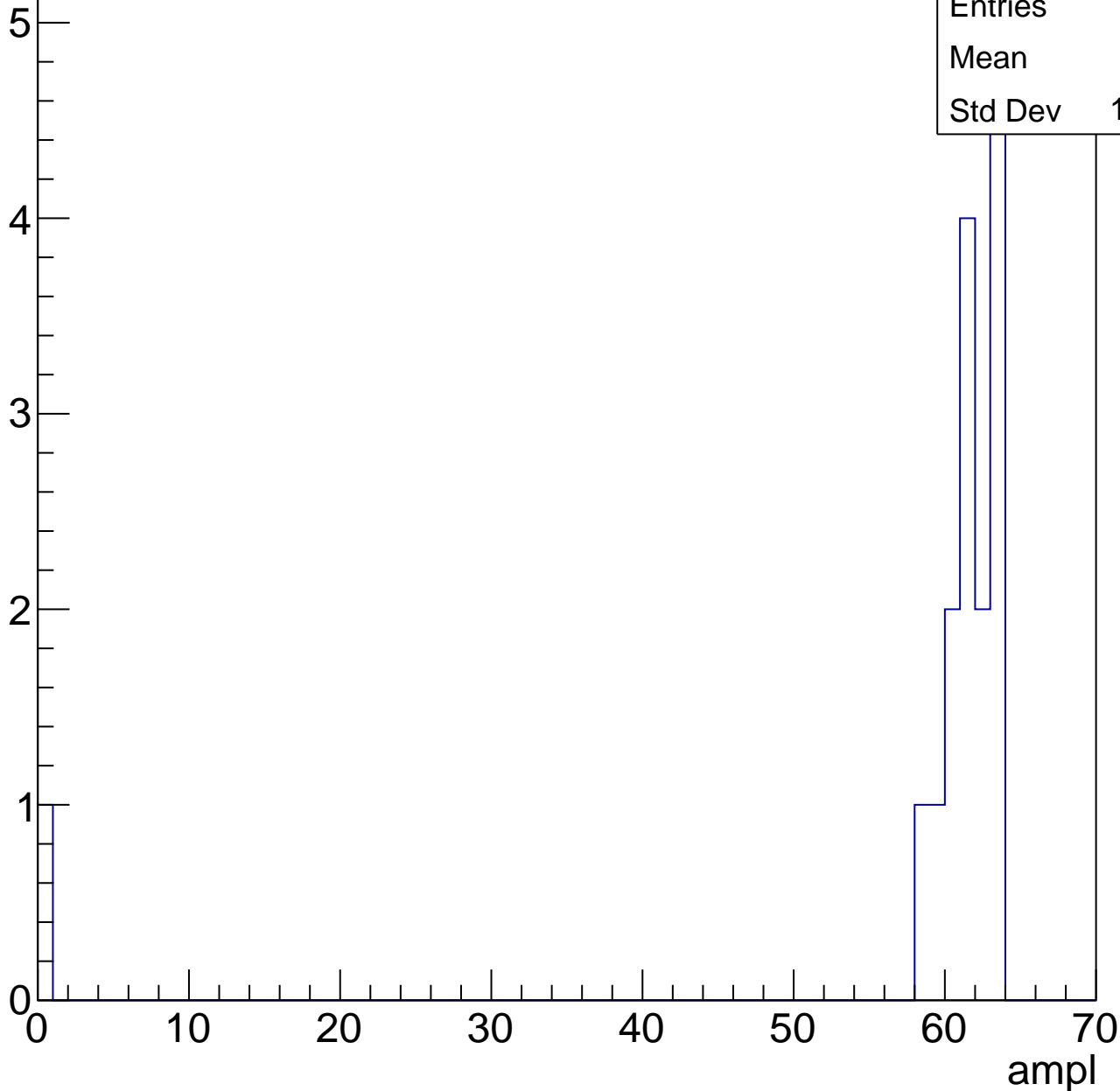


# B1L102S, U3-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	16
Mean	57.5
Std Dev	14.92





# B1L102S, U3-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U3-ch33, adc0

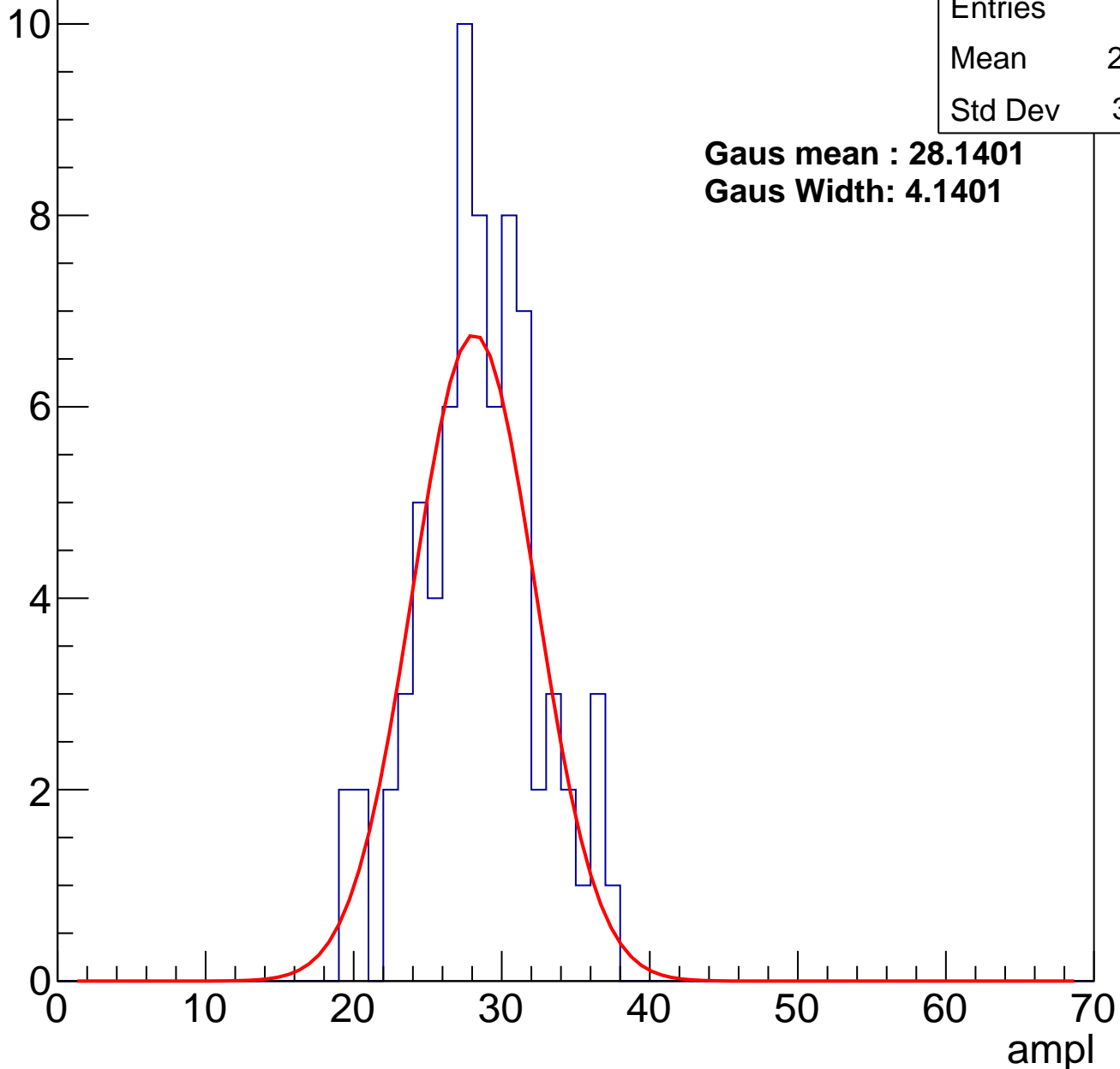
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	75
Mean	28.04
Std Dev	3.981

**Gaus mean : 28.1401**

**Gaus Width: 4.1401**

Entry



# B1L102S, U3-ch33, adc1

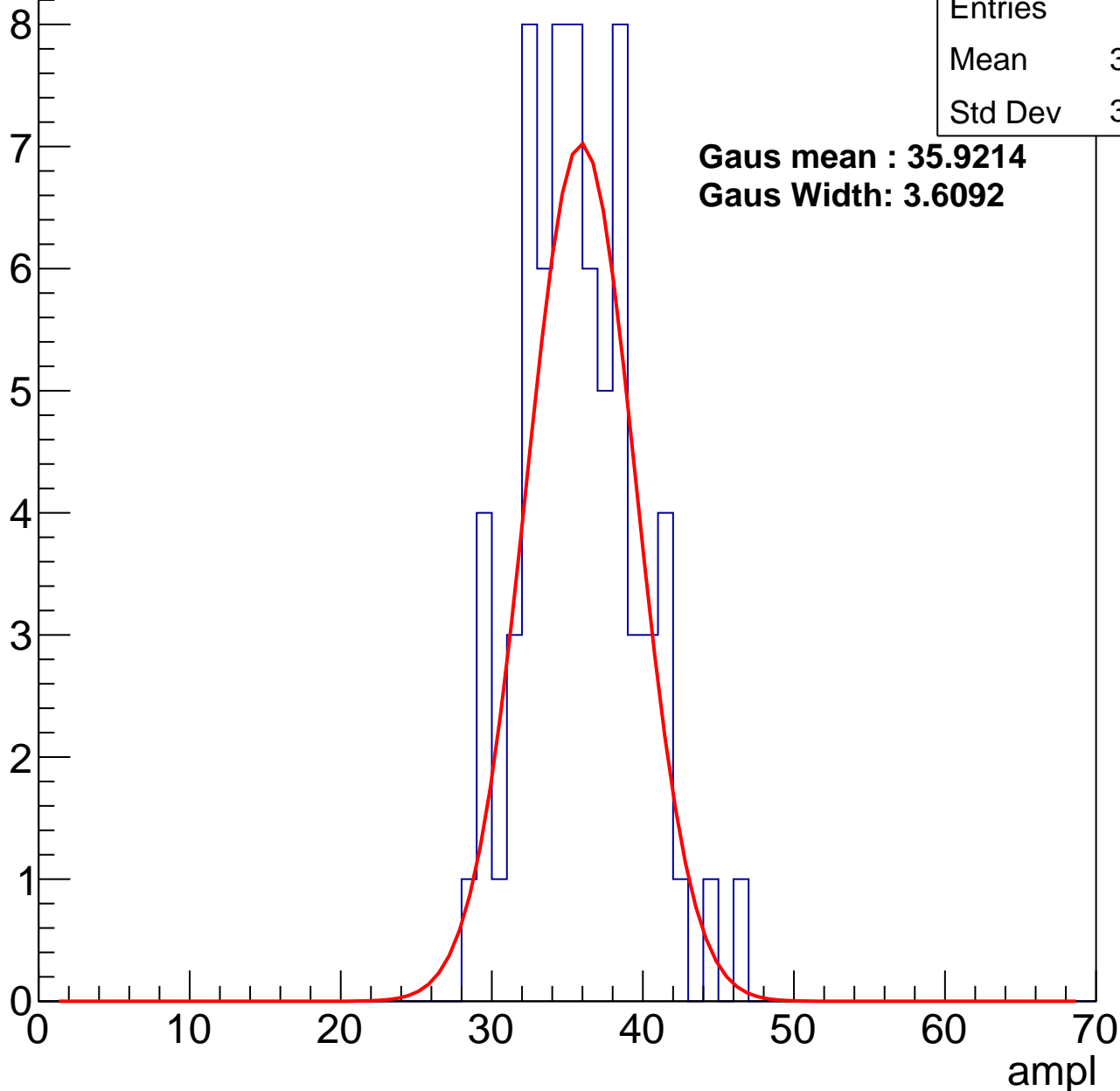
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	35.37
Std Dev	3.709

**Gaus mean : 35.9214**

**Gaus Width: 3.6092**



# B1L102S, U3-ch33, adc2

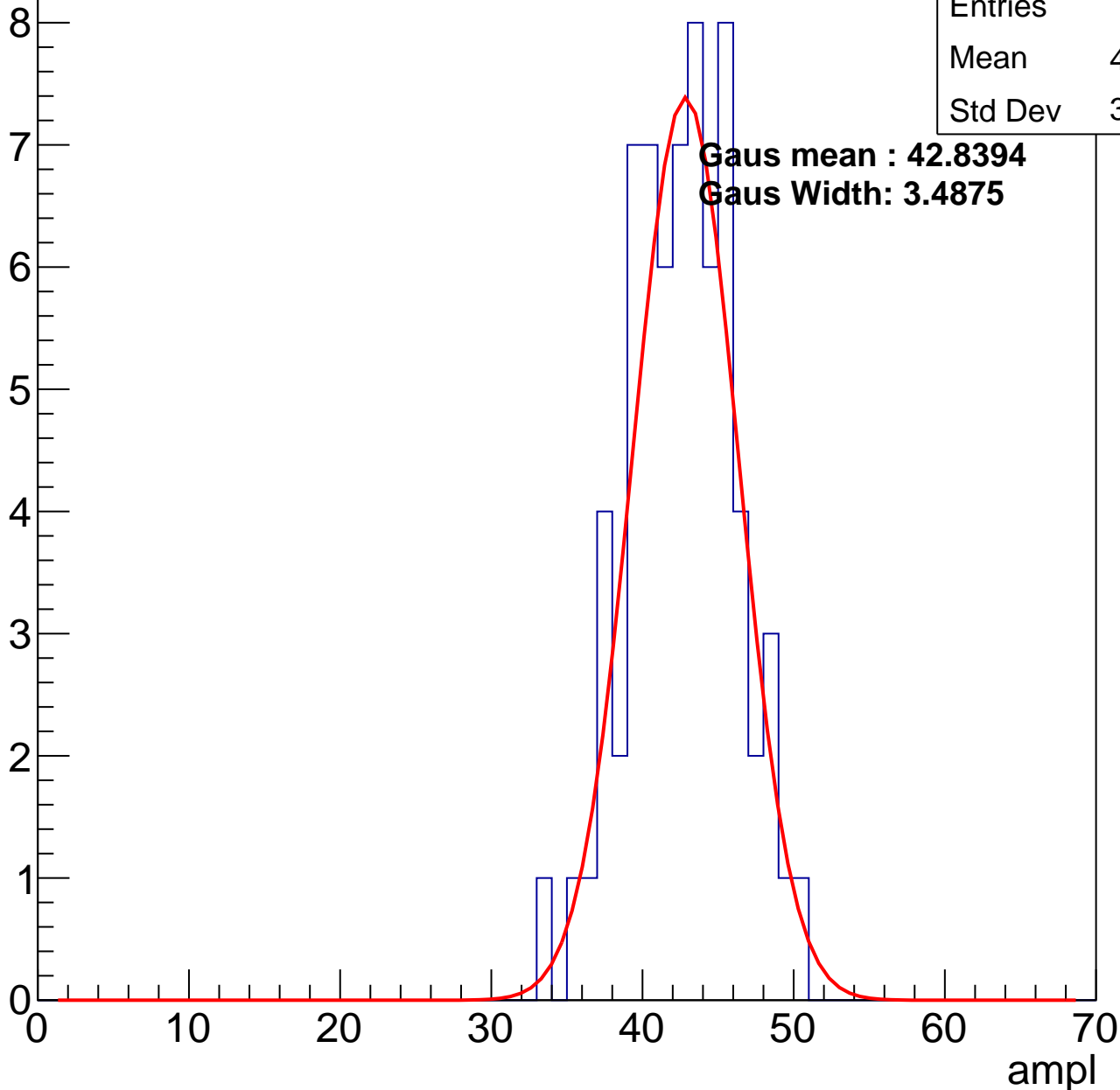
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	42.17
Std Dev	3.472

**Gaus mean : 42.8394**

**Gaus Width: 3.4875**

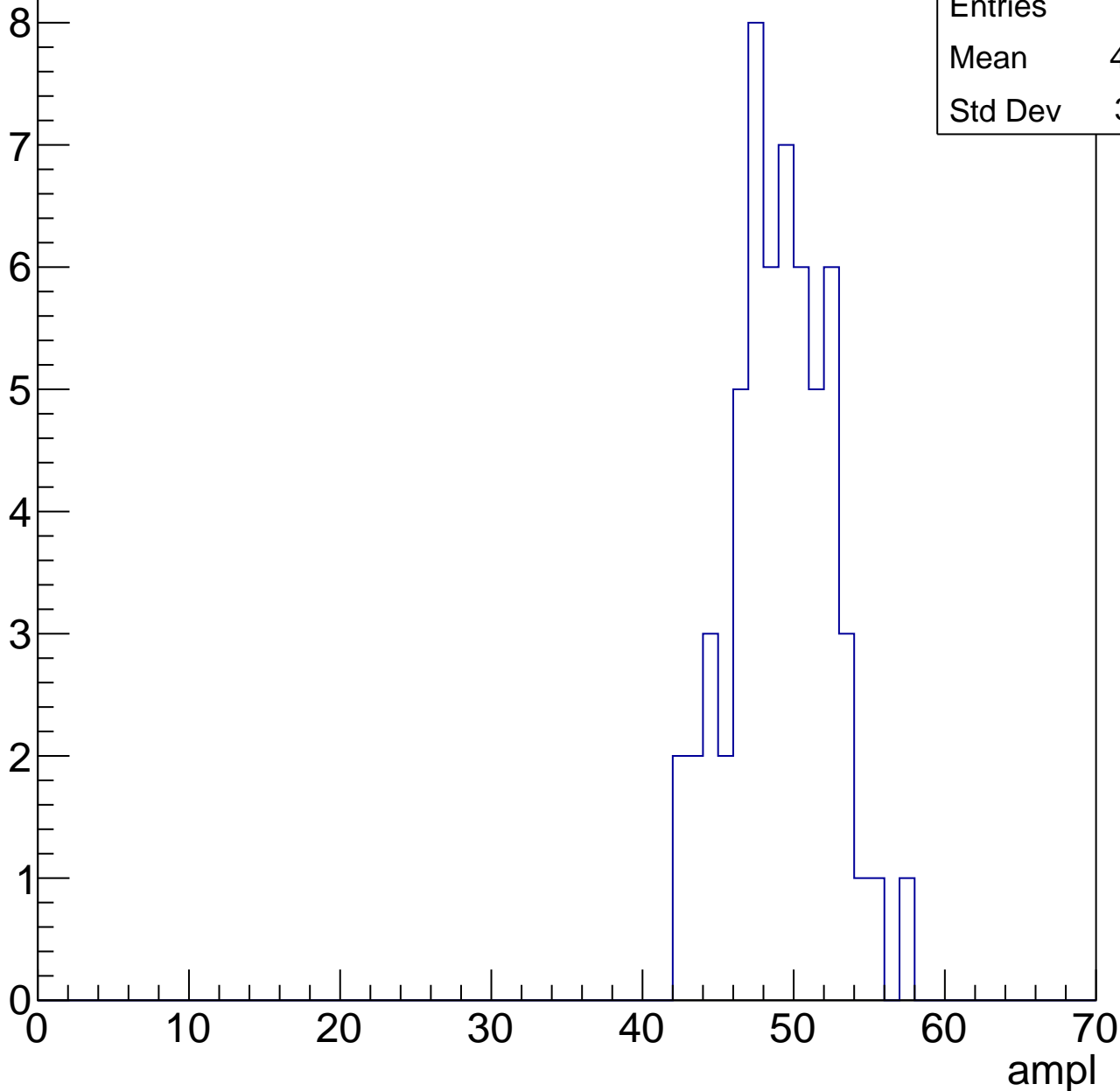


# B1L102S, U3-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	48.64
Std Dev	3.231

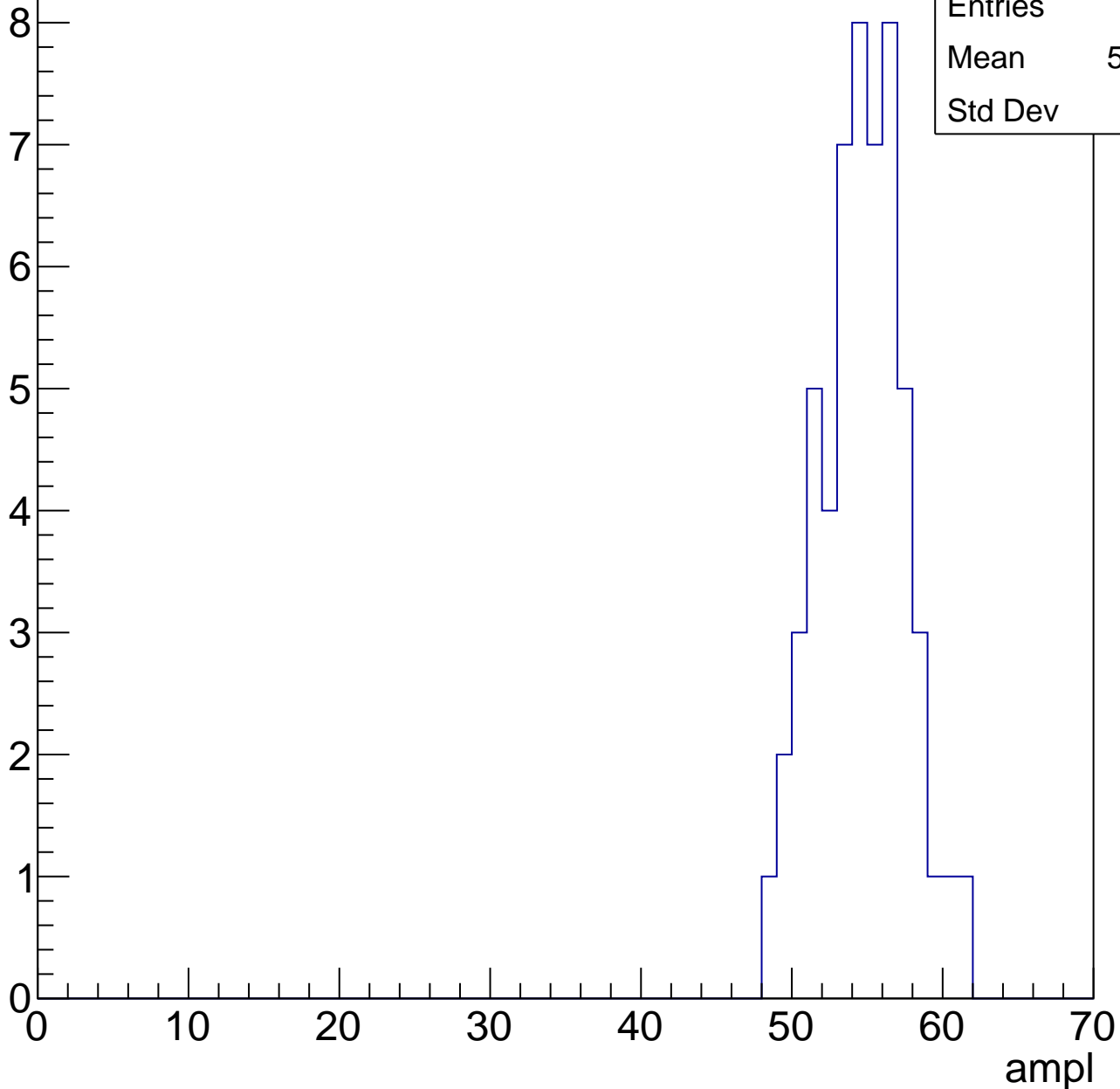


# B1L102S, U3-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	54.18
Std Dev	2.81



# B1L102S, U3-ch33, adc5

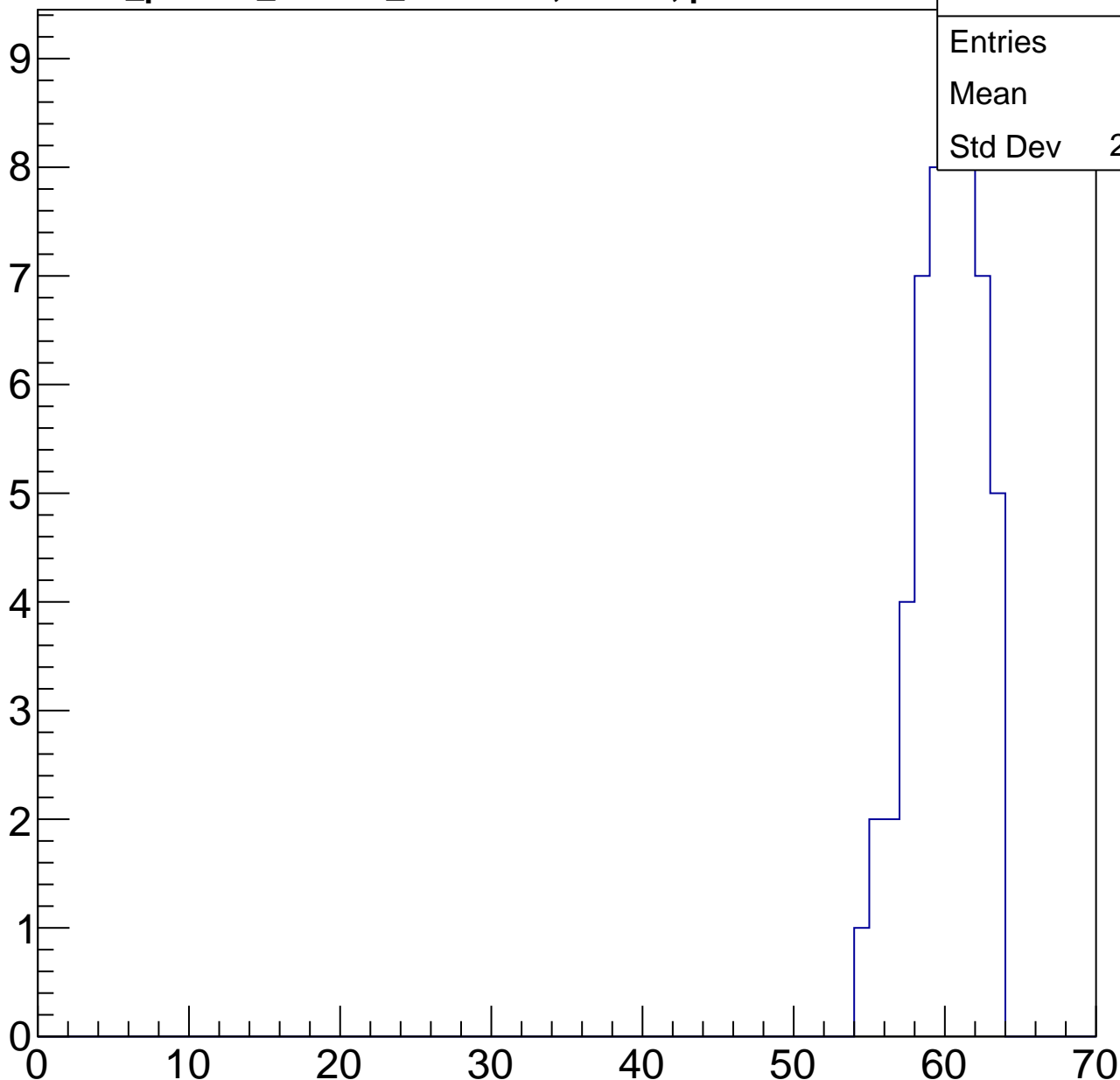
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	53
Mean	59.6
Std Dev	2.226

ampl

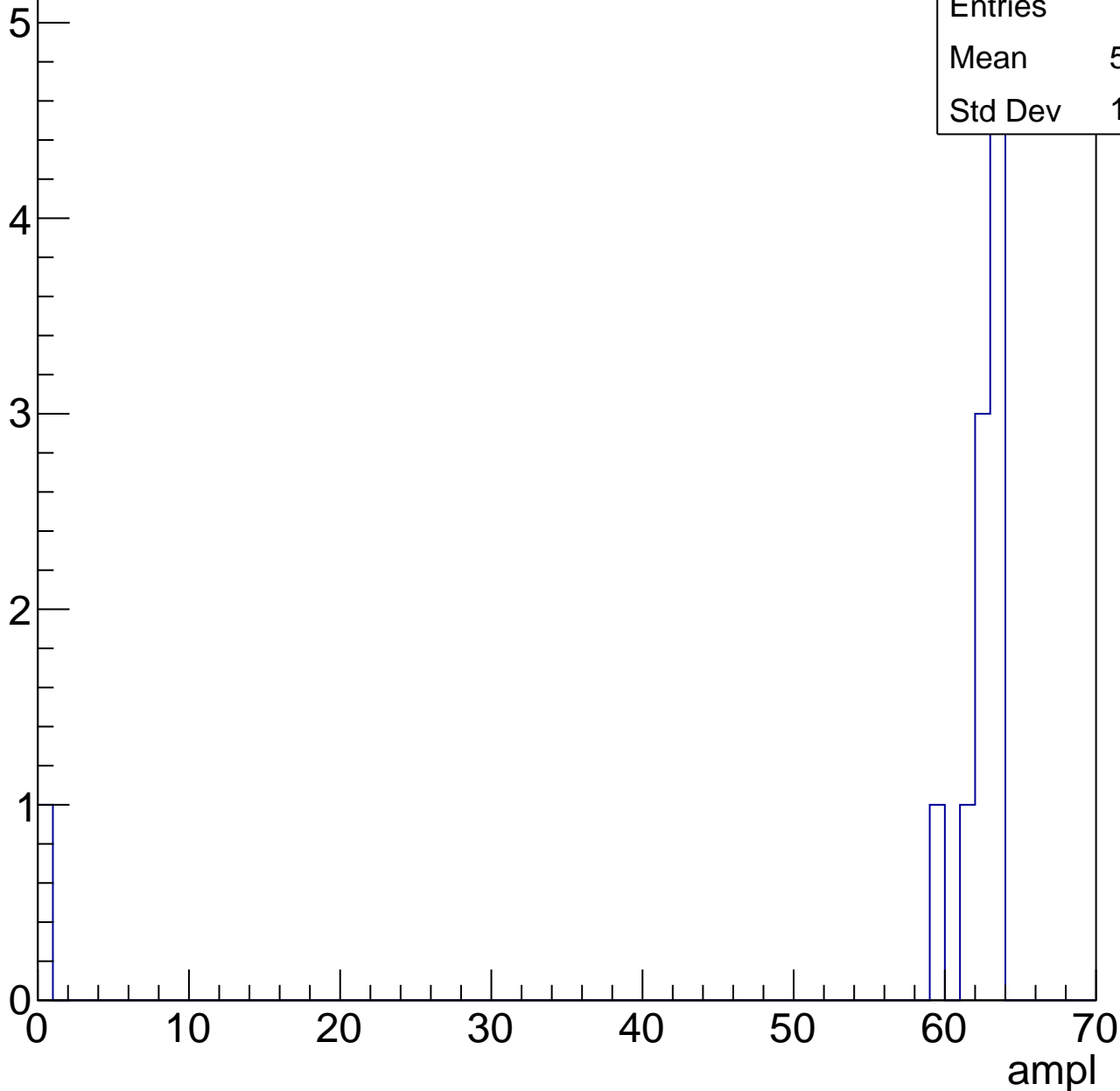


# B1L102S, U3-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	11
Mean	56.45
Std Dev	17.89





# B1L102S, U3-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch34, adc0

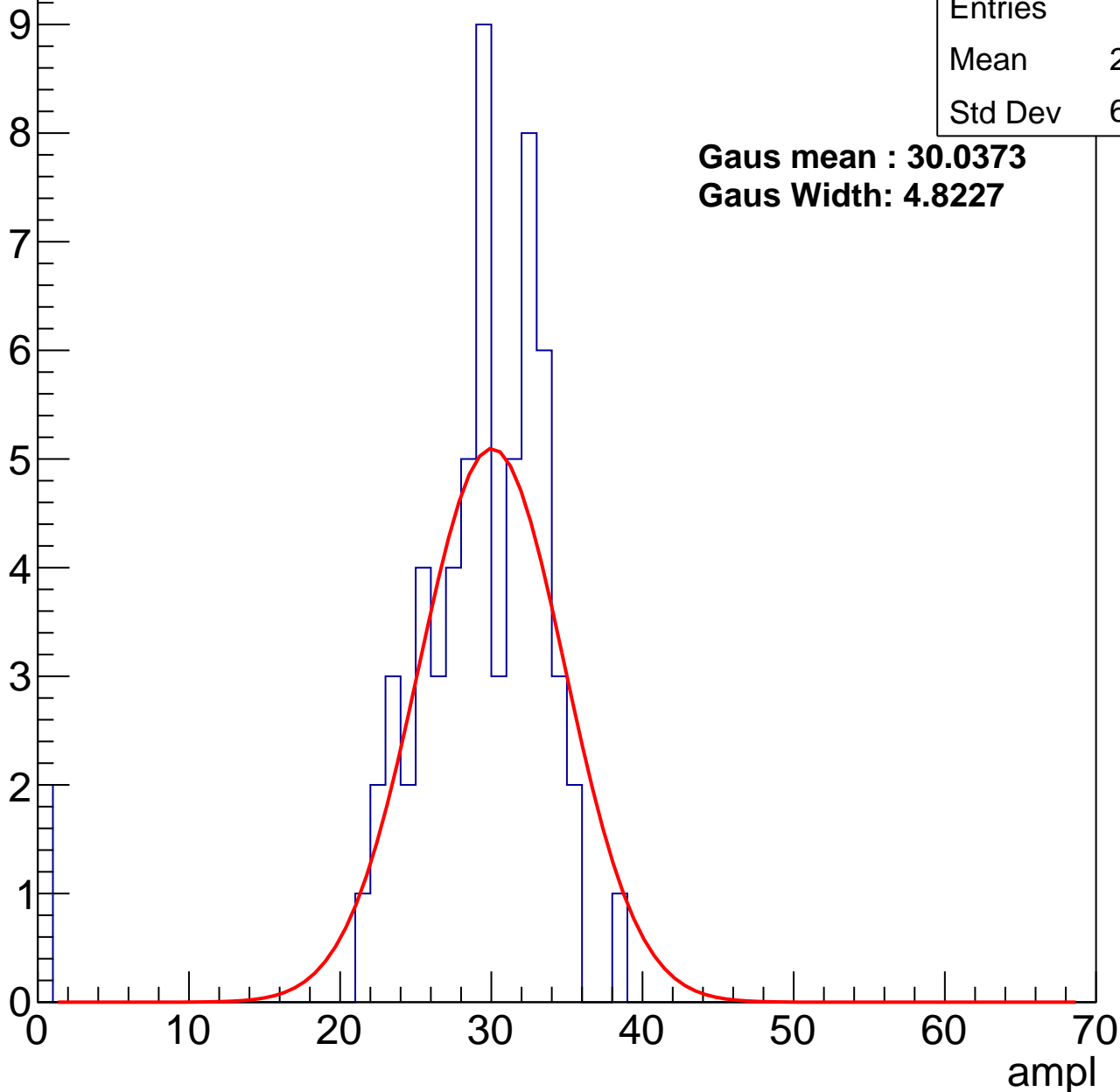
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	28.22
Std Dev	6.293

**Gaus mean : 30.0373**

**Gaus Width: 4.8227**



# B1L102S, U3-ch34, adc1

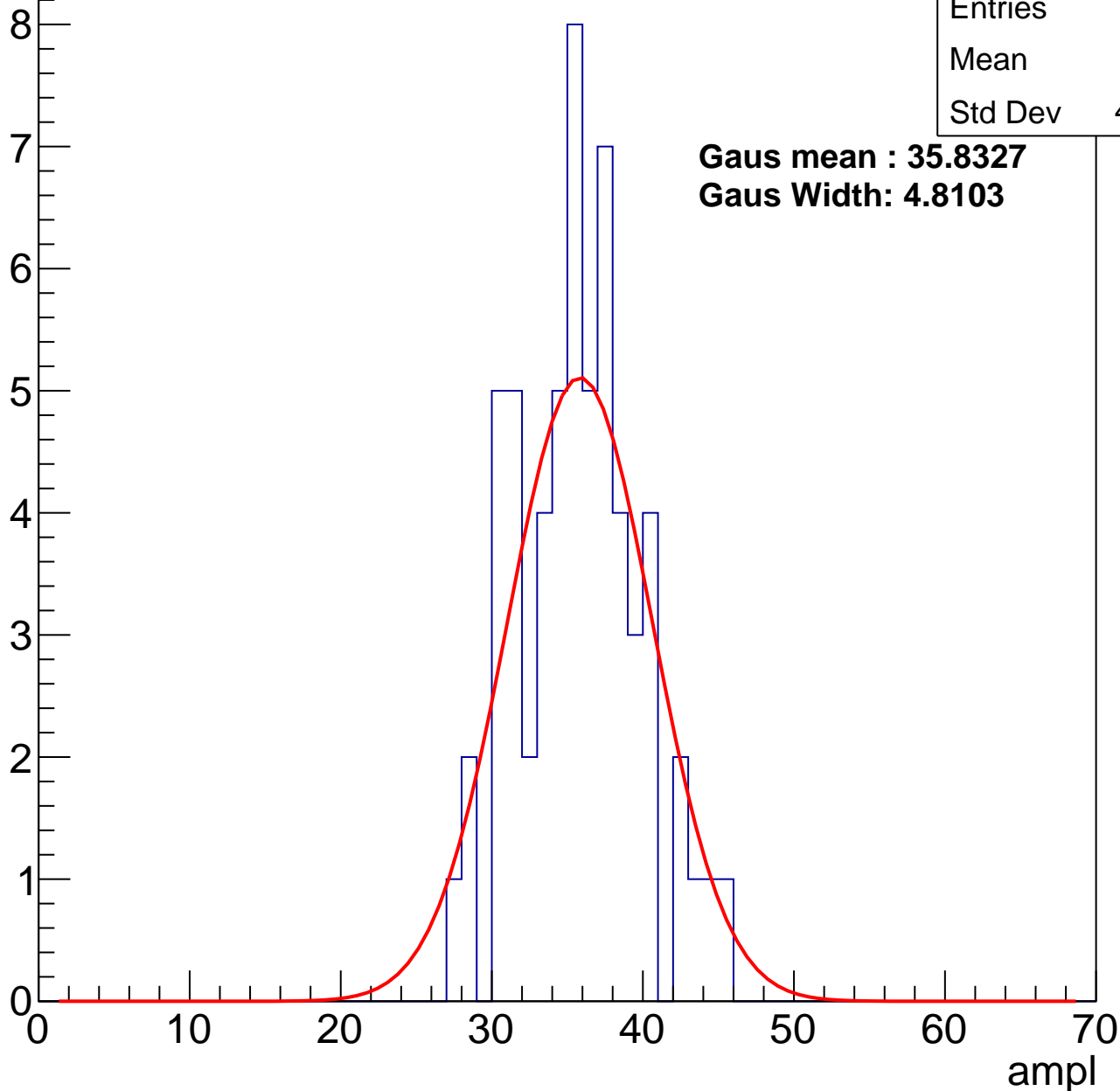
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	35.3
Std Dev	4.001

**Gaus mean : 35.8327**

**Gaus Width: 4.8103**



# B1L102S, U3-ch34, adc2

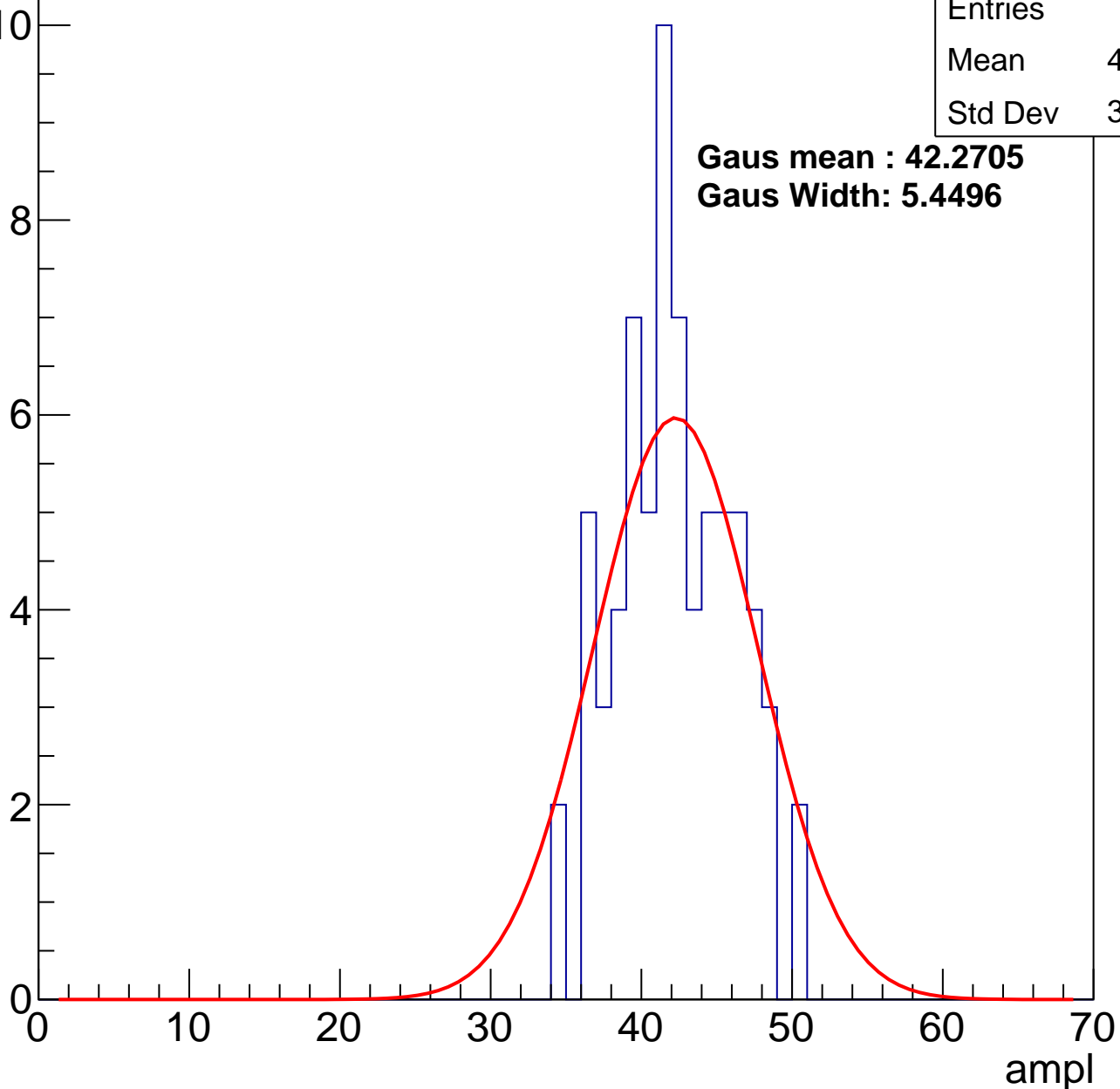
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	41.79
Std Dev	3.794

**Gaus mean : 42.2705**

**Gaus Width: 5.4496**

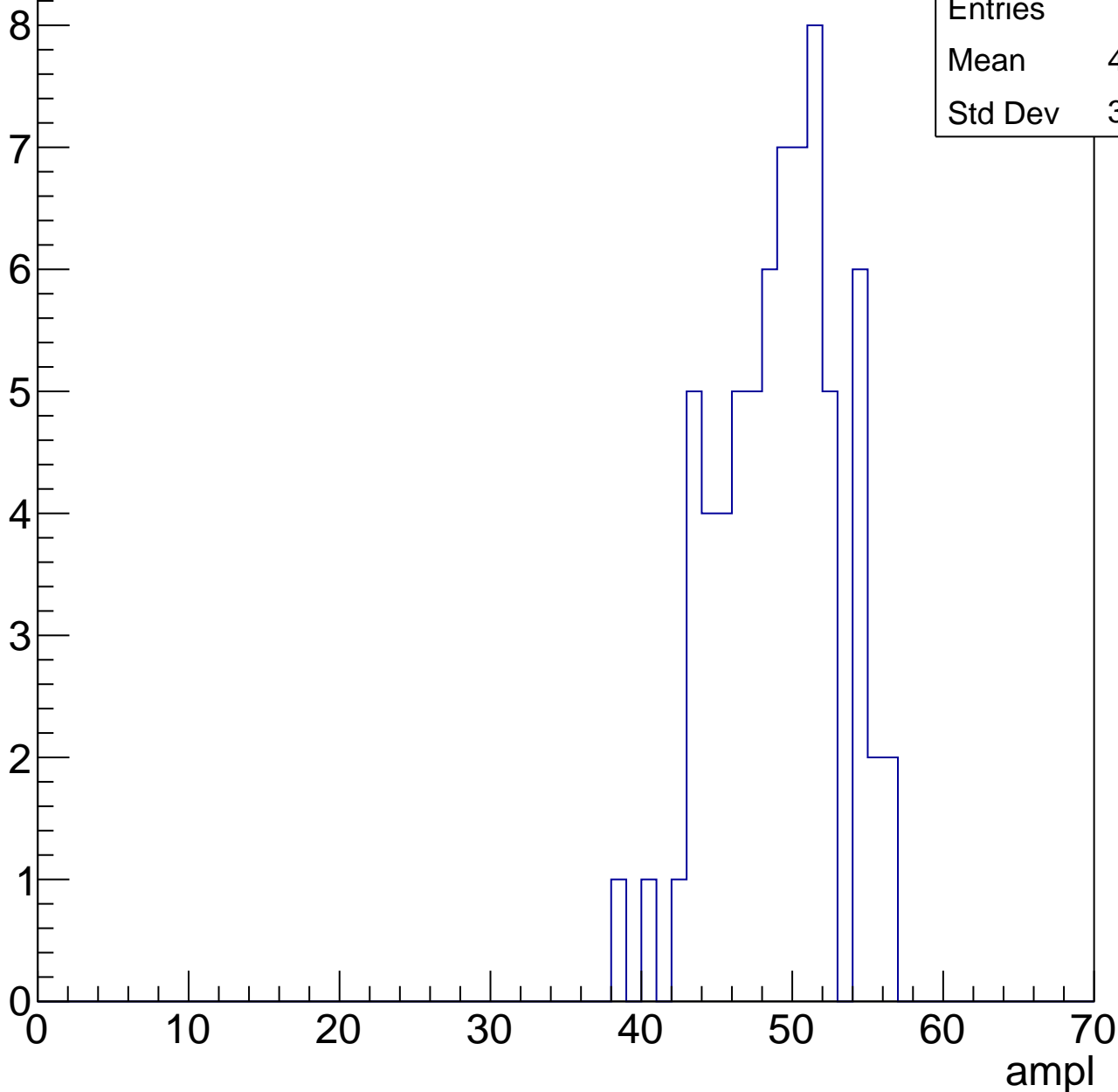


# B1L102S, U3-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	48.57
Std Dev	3.914

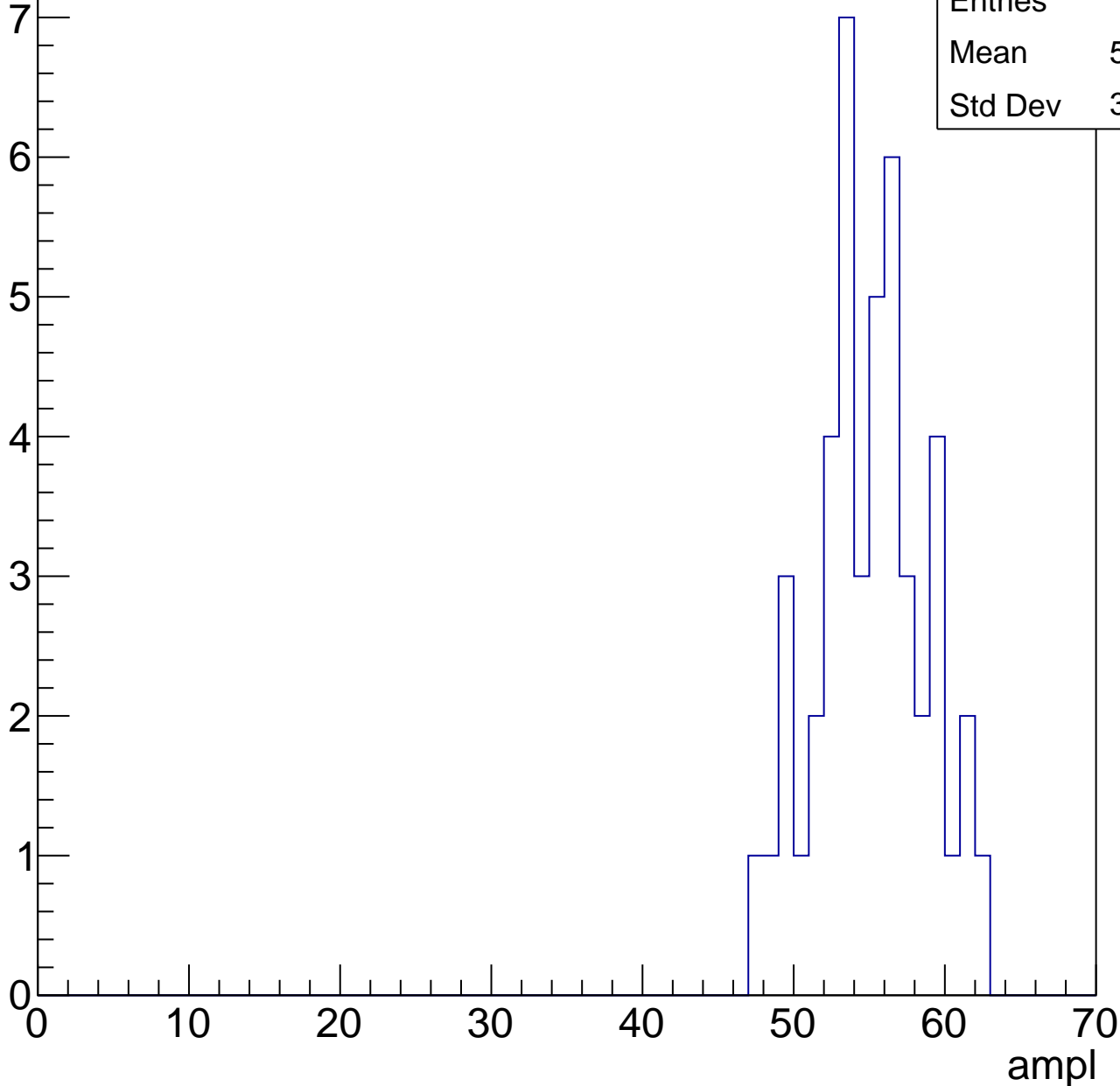


# B1L102S, U3-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	54.63
Std Dev	3.565

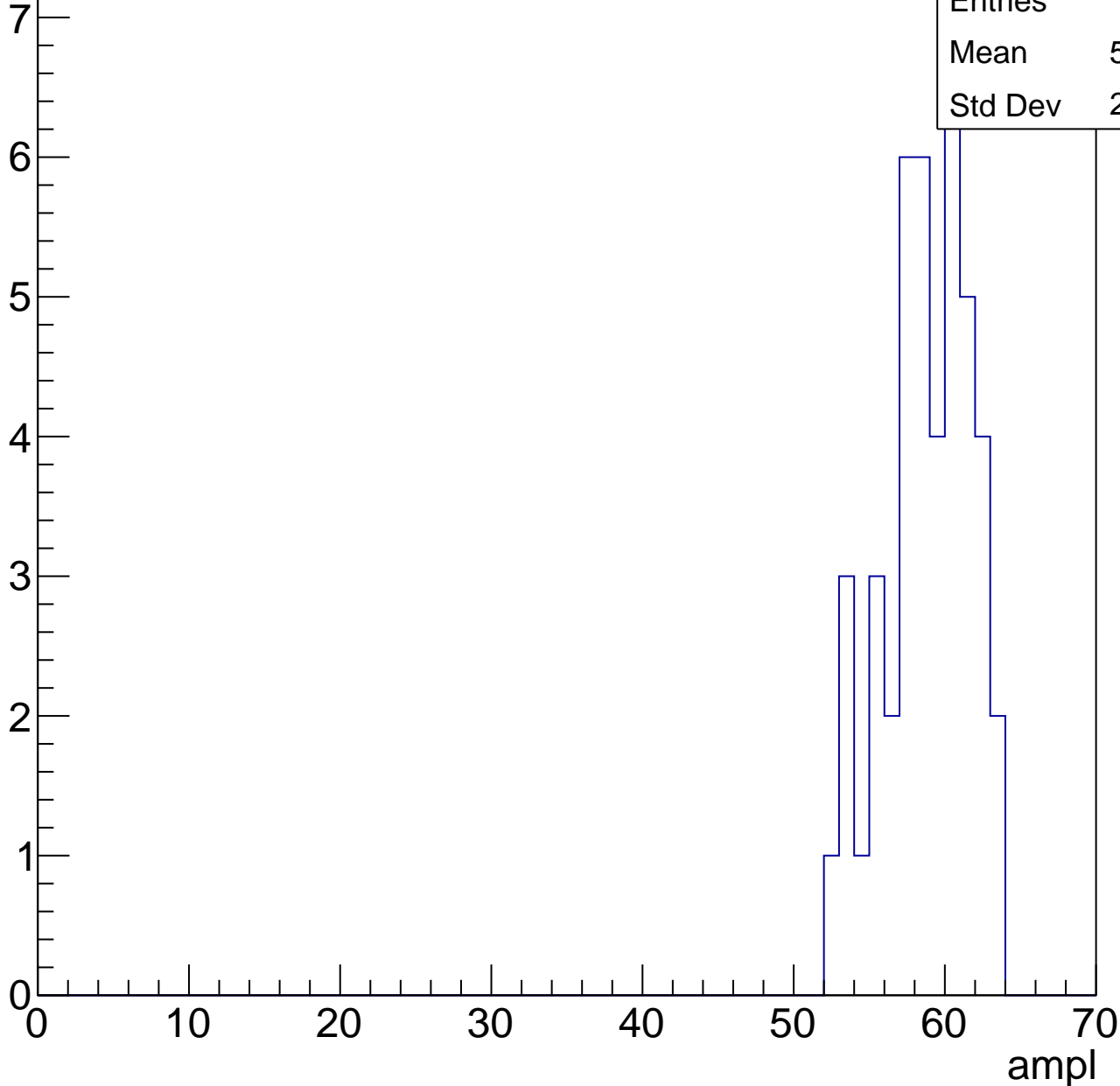


# B1L102S, U3-ch34, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	44
Mean	58.34
Std Dev	2.836

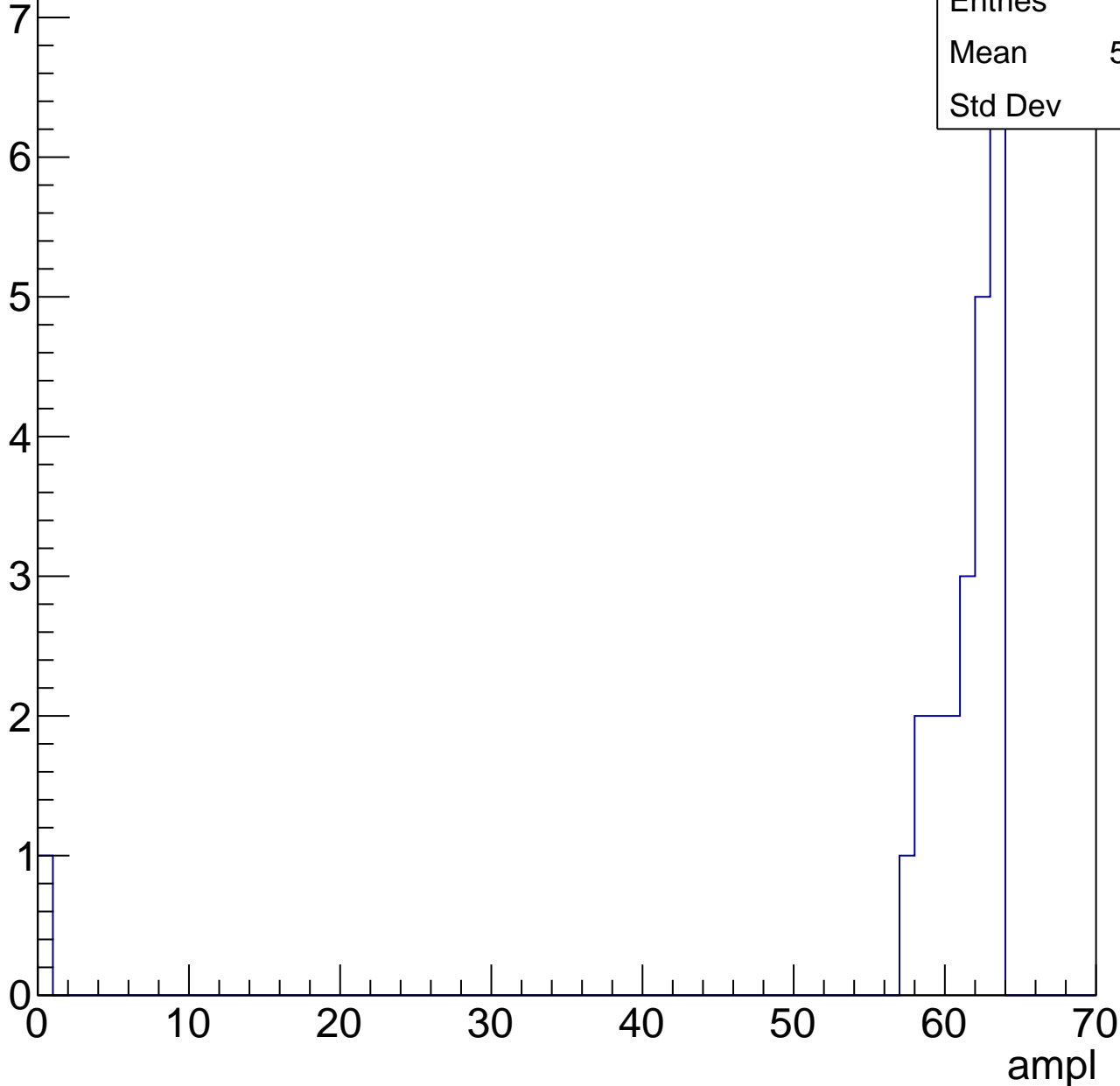


# B1L102S, U3-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	23
Mean	58.48
Std Dev	12.6





# B1L102S, U3-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch35, adc0

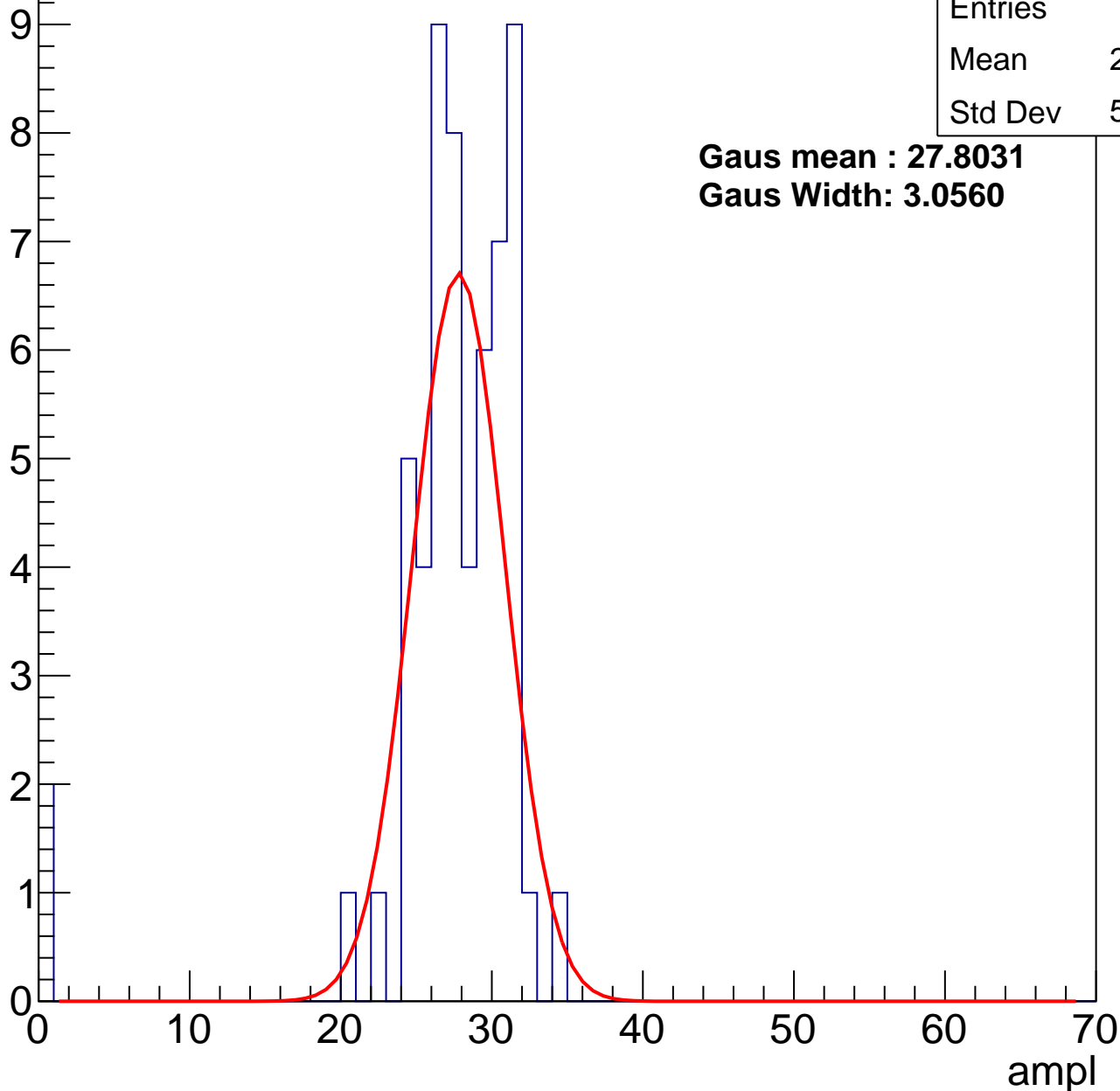
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	26.78
Std Dev	5.736

**Gaus mean : 27.8031**

**Gaus Width: 3.0560**



# B1L102S, U3-ch35, adc1

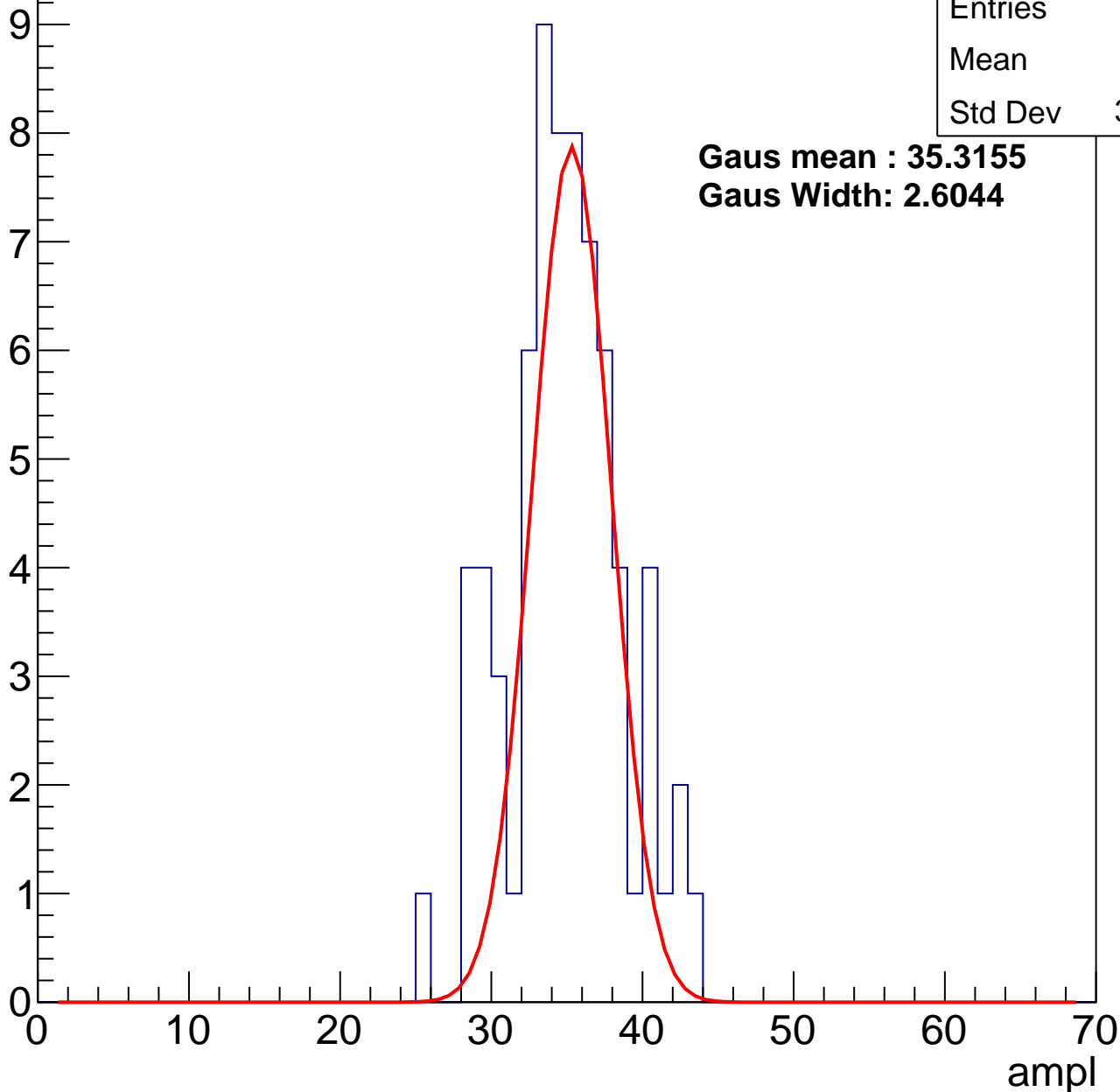
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	34.4
Std Dev	3.751

**Gaus mean : 35.3155**

**Gaus Width: 2.6044**



# B1L102S, U3-ch35, adc2

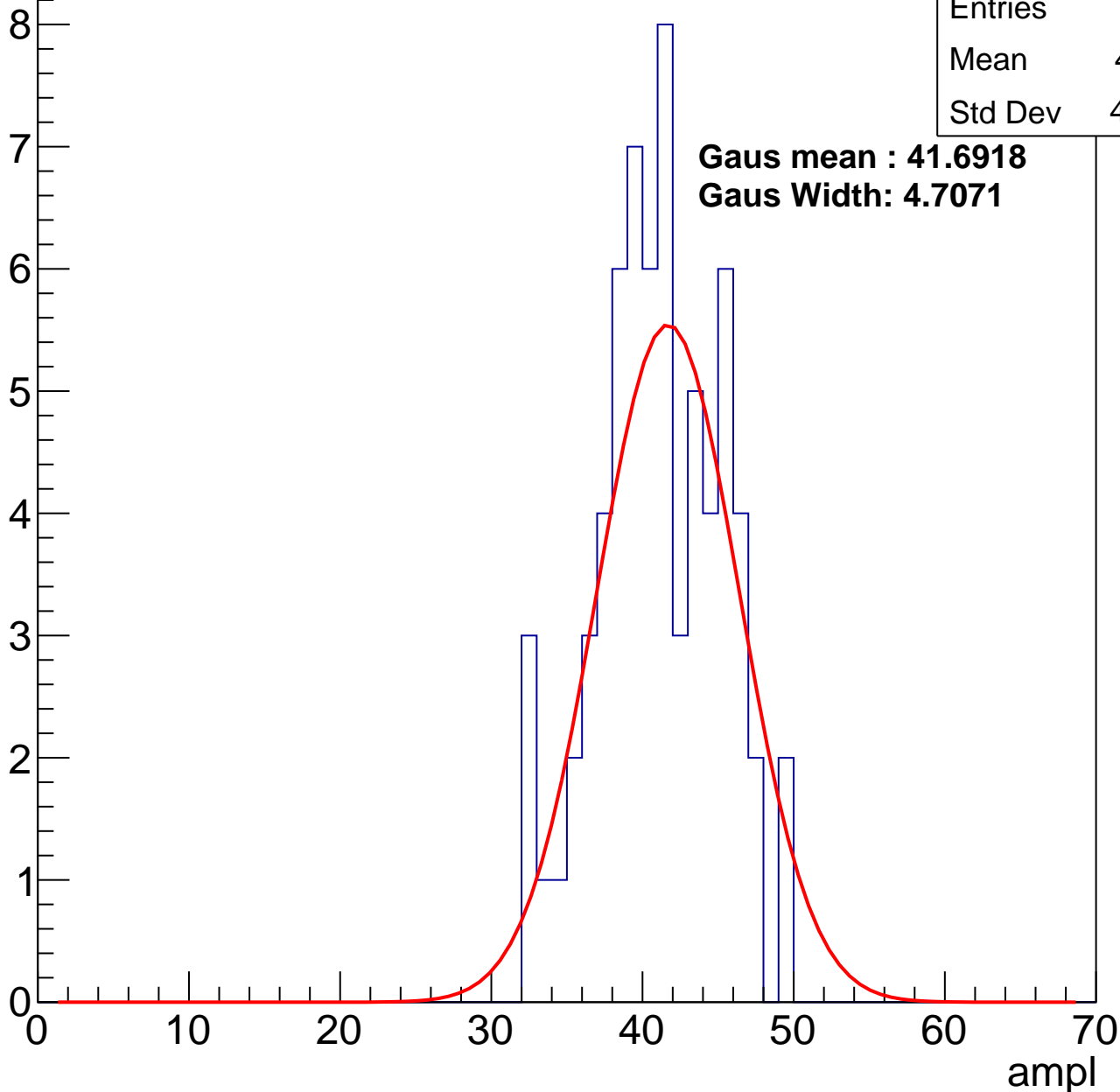
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	40.61
Std Dev	4.052

**Gaus mean : 41.6918**

**Gaus Width: 4.7071**

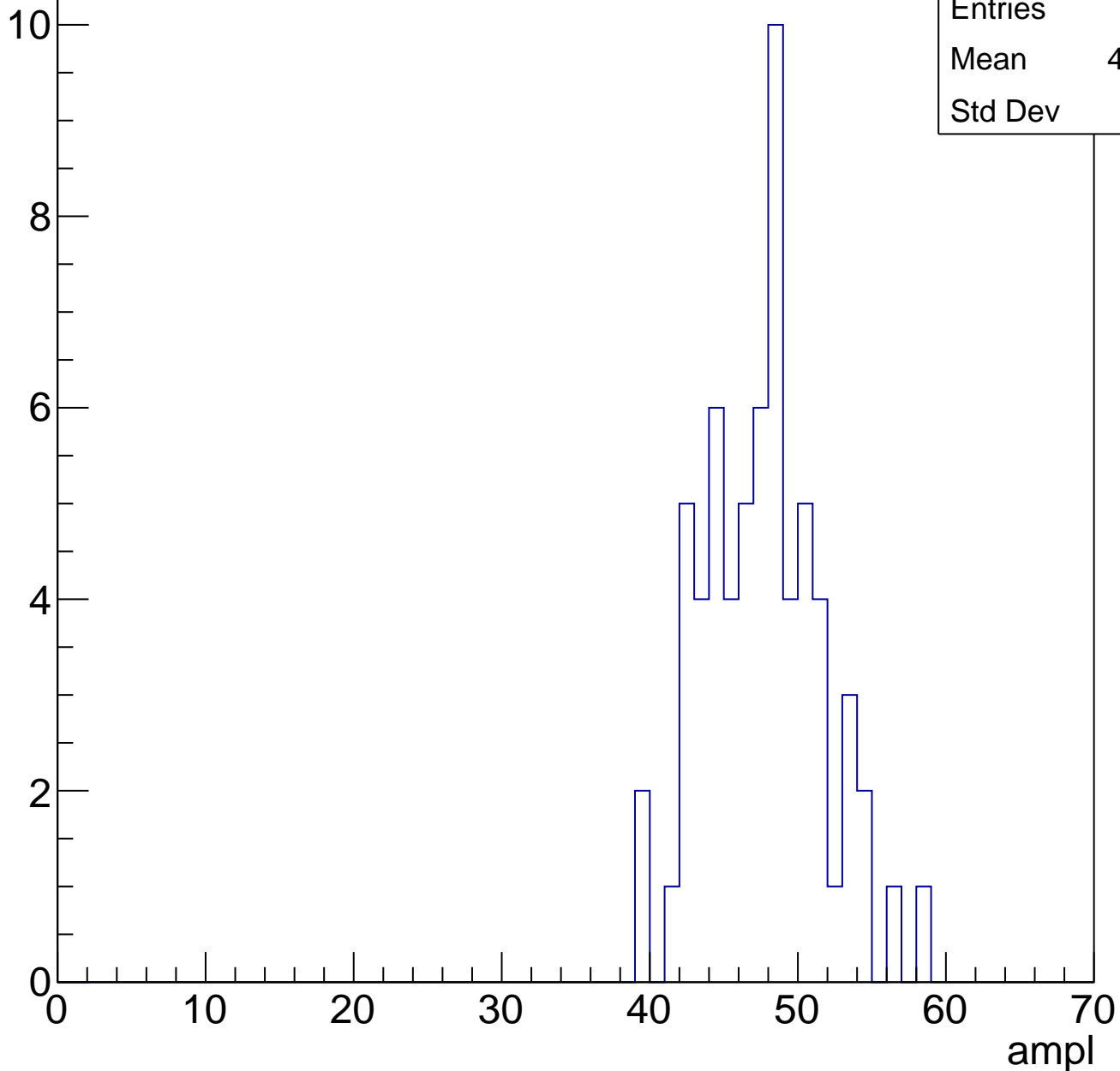


# B1L102S, U3-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	64
Mean	47.19
Std Dev	3.94

Entry

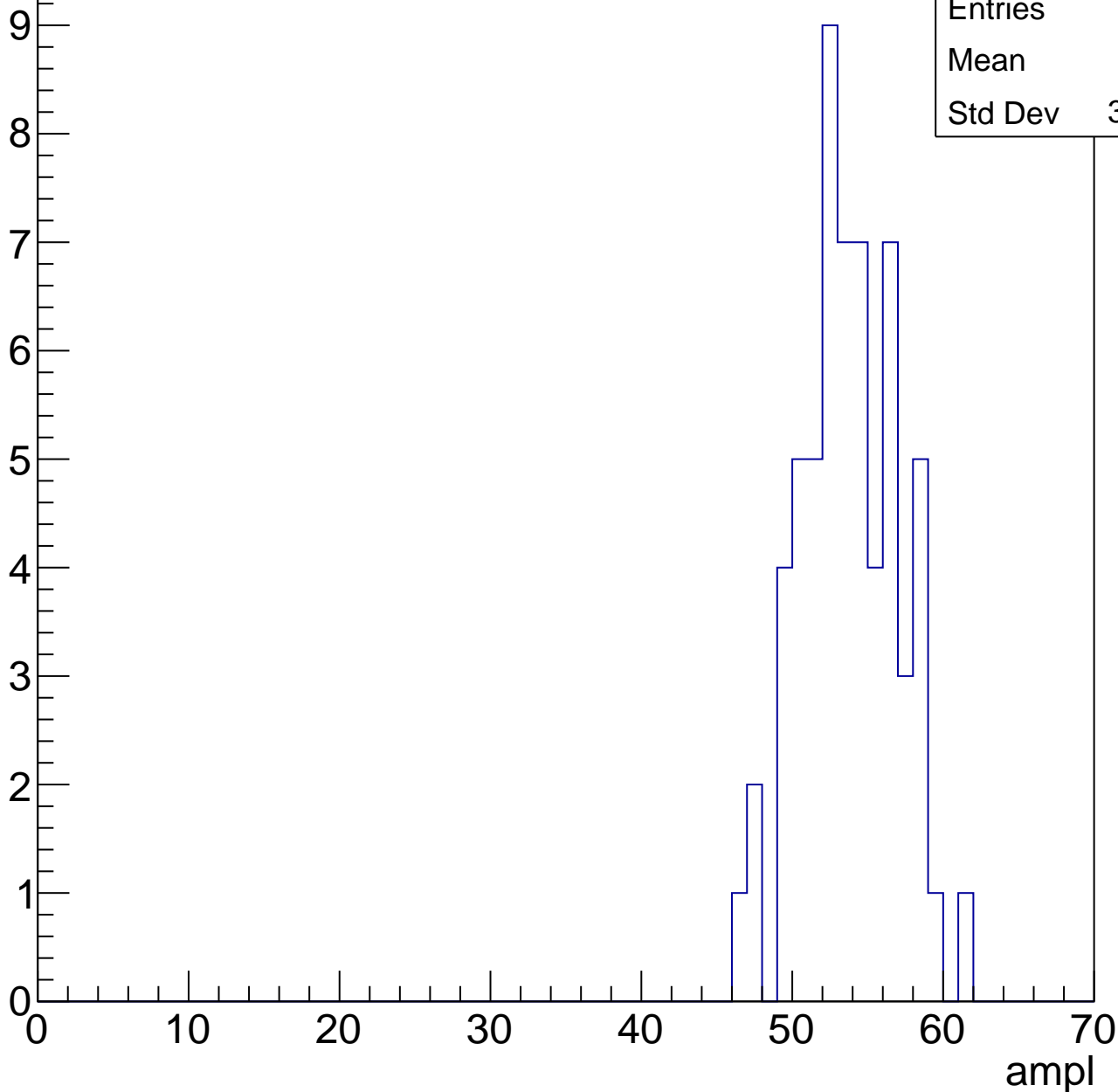


# B1L102S, U3-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	53.3
Std Dev	3.169

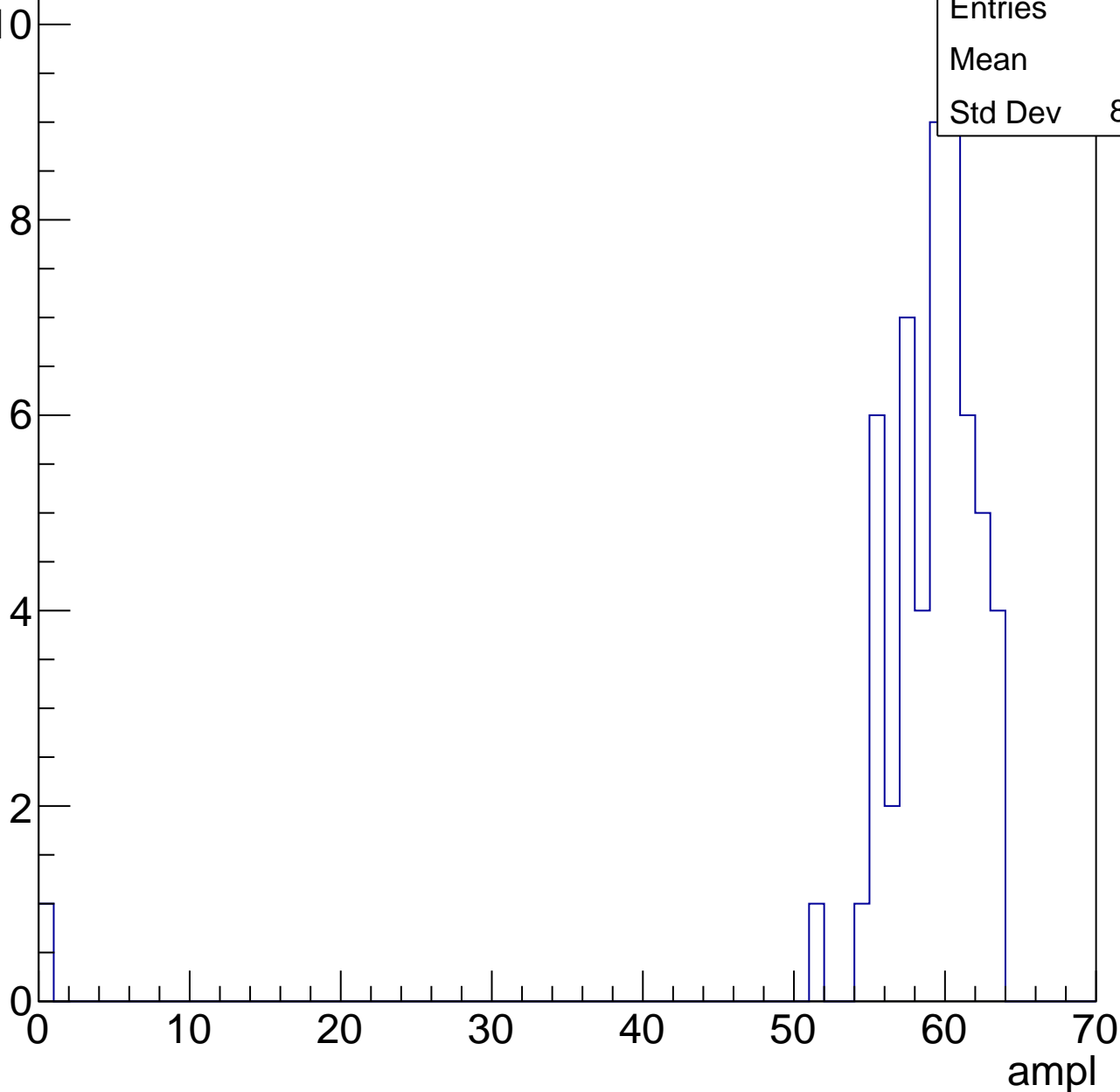


# B1L102S, U3-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	57.8
Std Dev	8.215

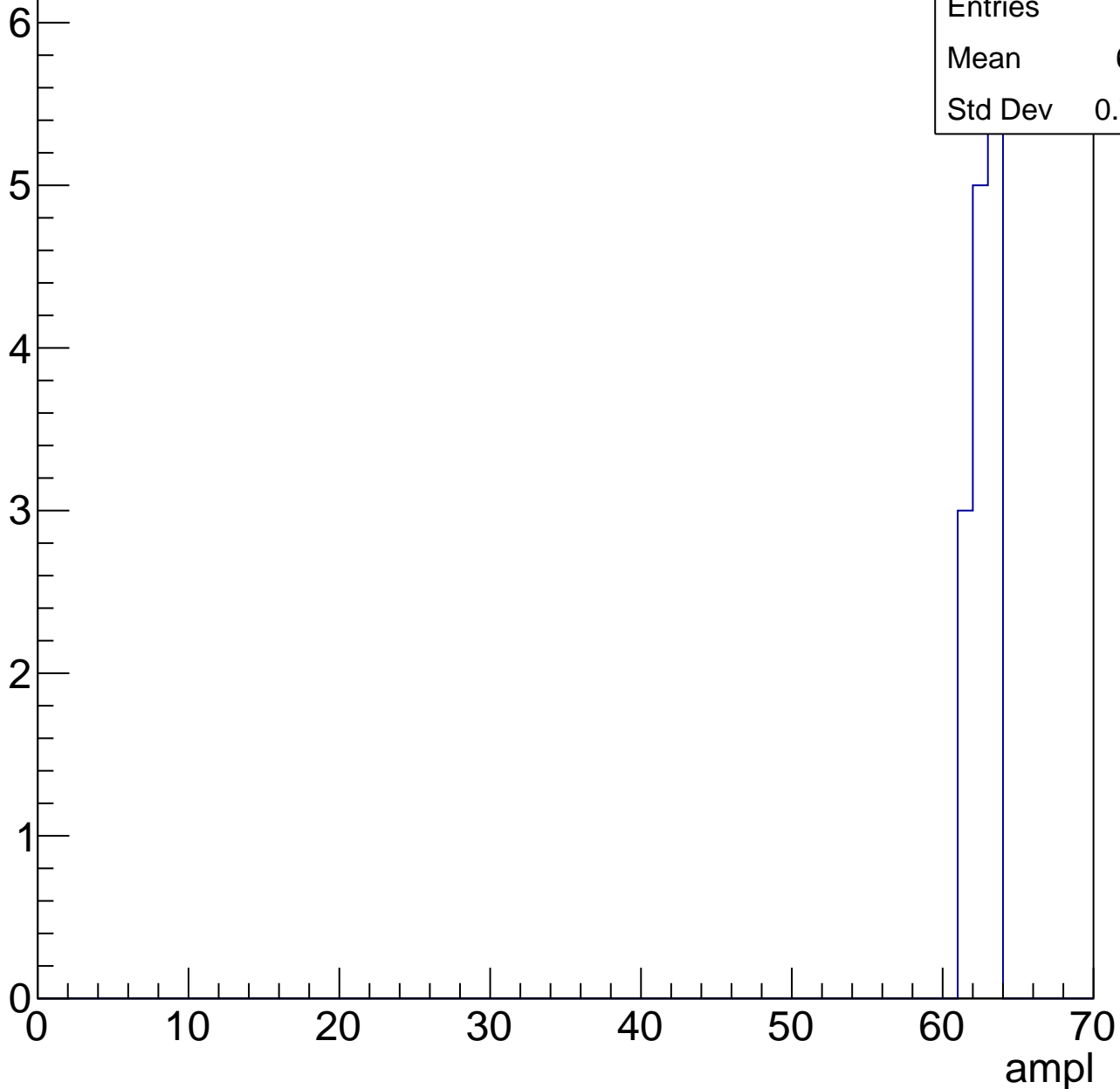


# B1L102S, U3-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	14
Mean	62.21
Std Dev	0.7726





# B1L102S, U3-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch36, adc0

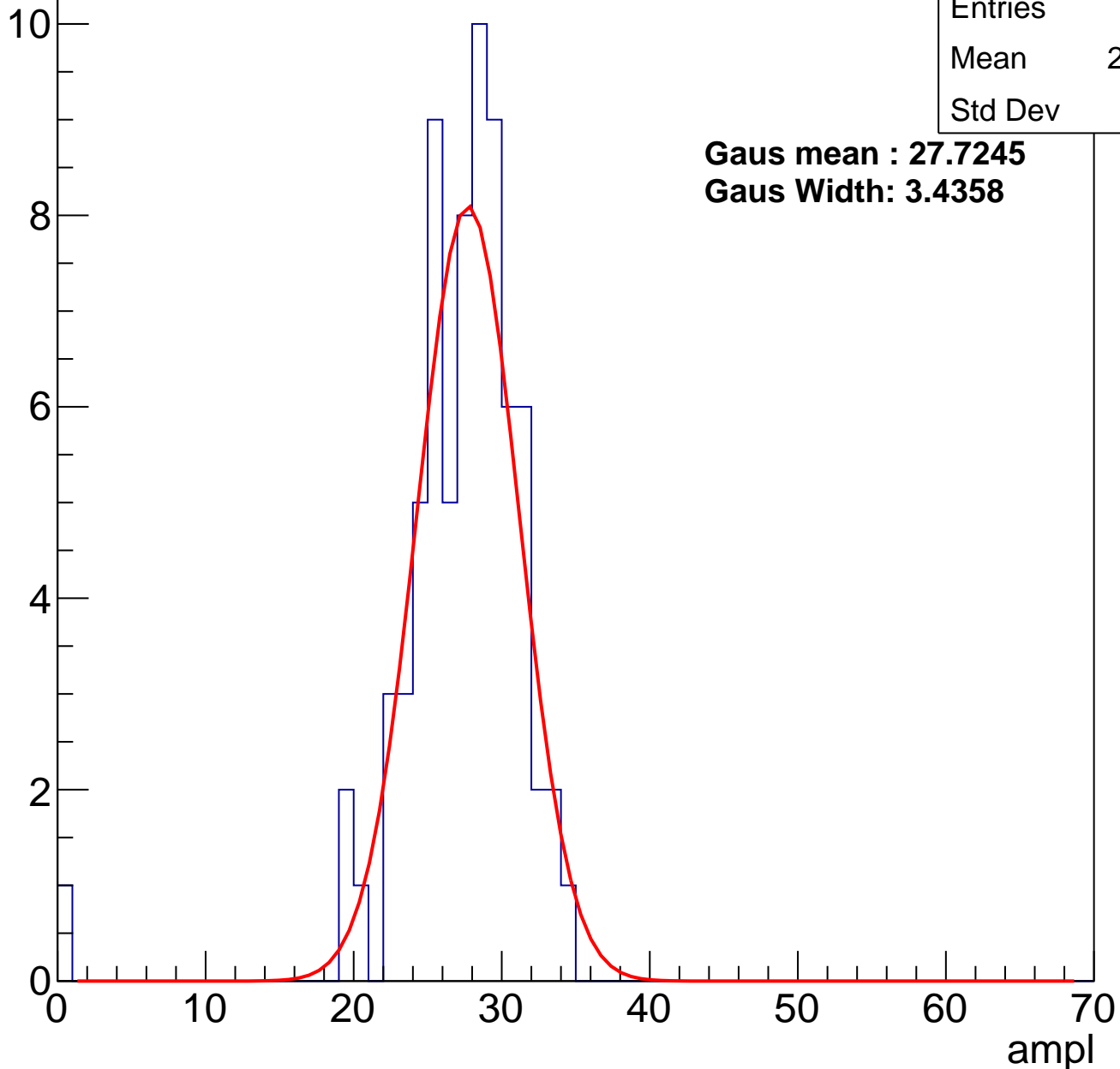
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	73
Mean	26.78
Std Dev	4.5

**Gaus mean : 27.7245**

**Gaus Width: 3.4358**

Entry



# B1L102S, U3-ch36, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	71
Mean	34.79
Std Dev	2.997

**Gaus mean : 35.6236**

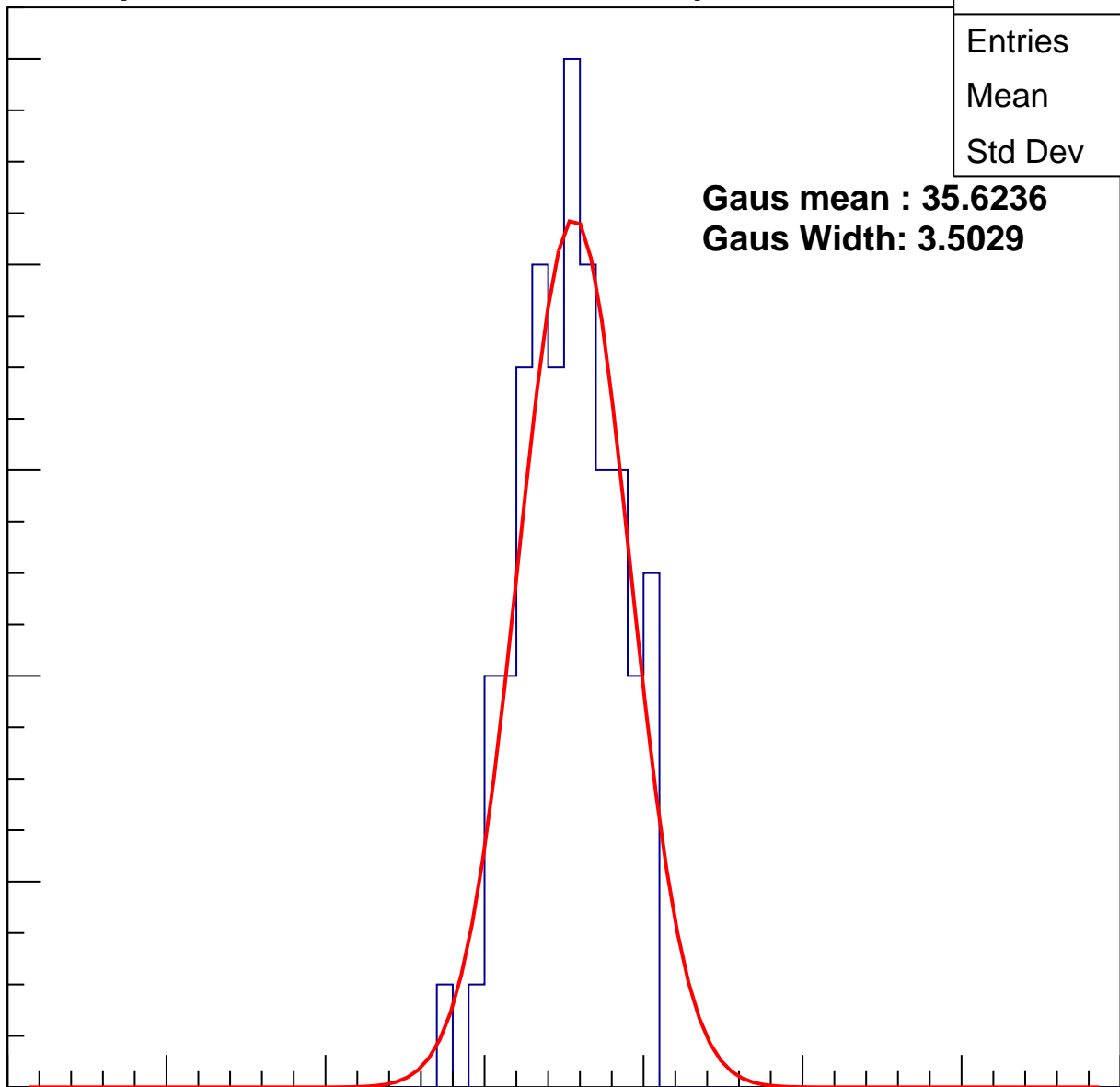
**Gaus Width: 3.5029**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L102S, U3-ch36, adc2

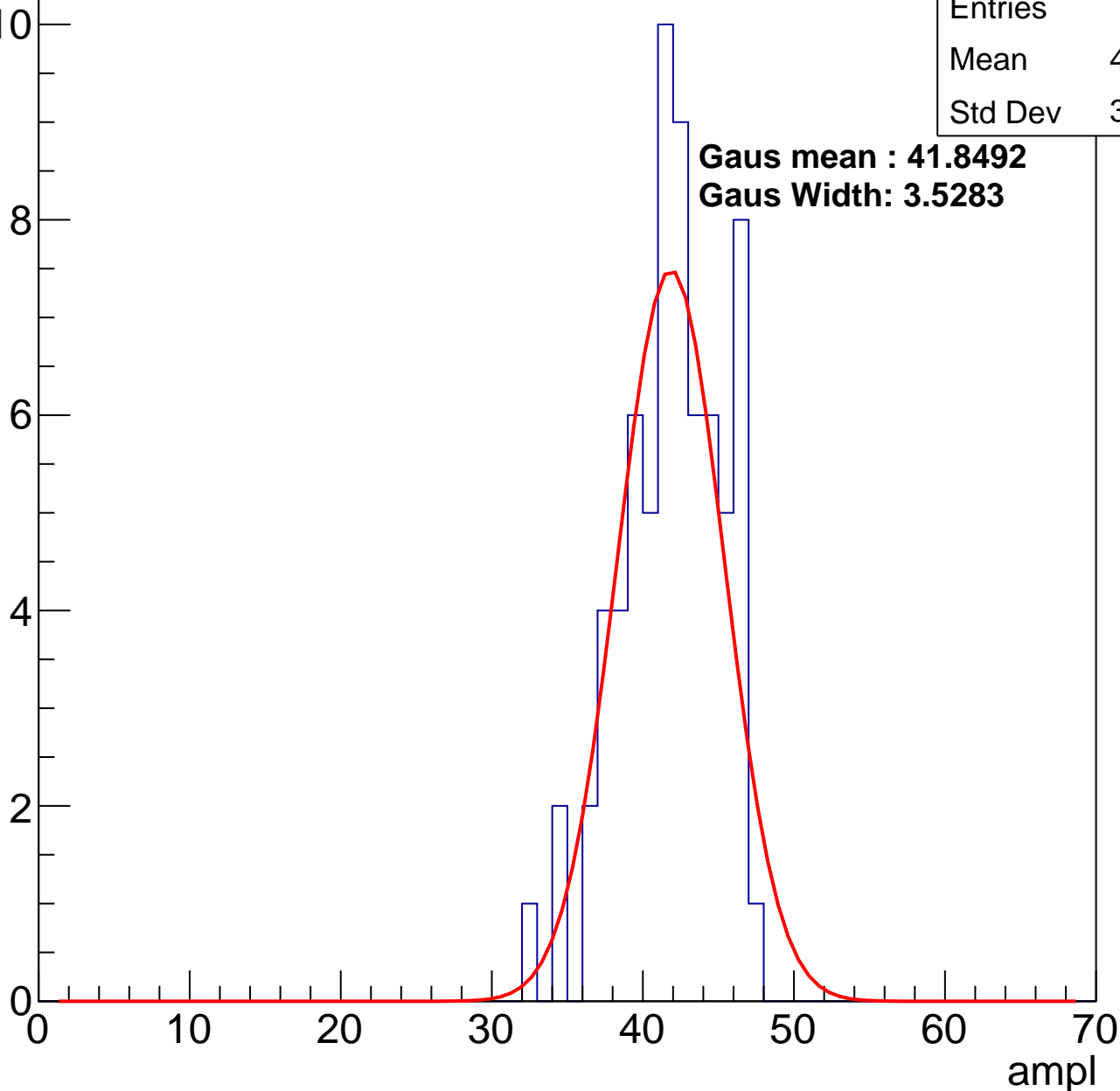
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	41.39
Std Dev	3.298

**Gaus mean : 41.8492**

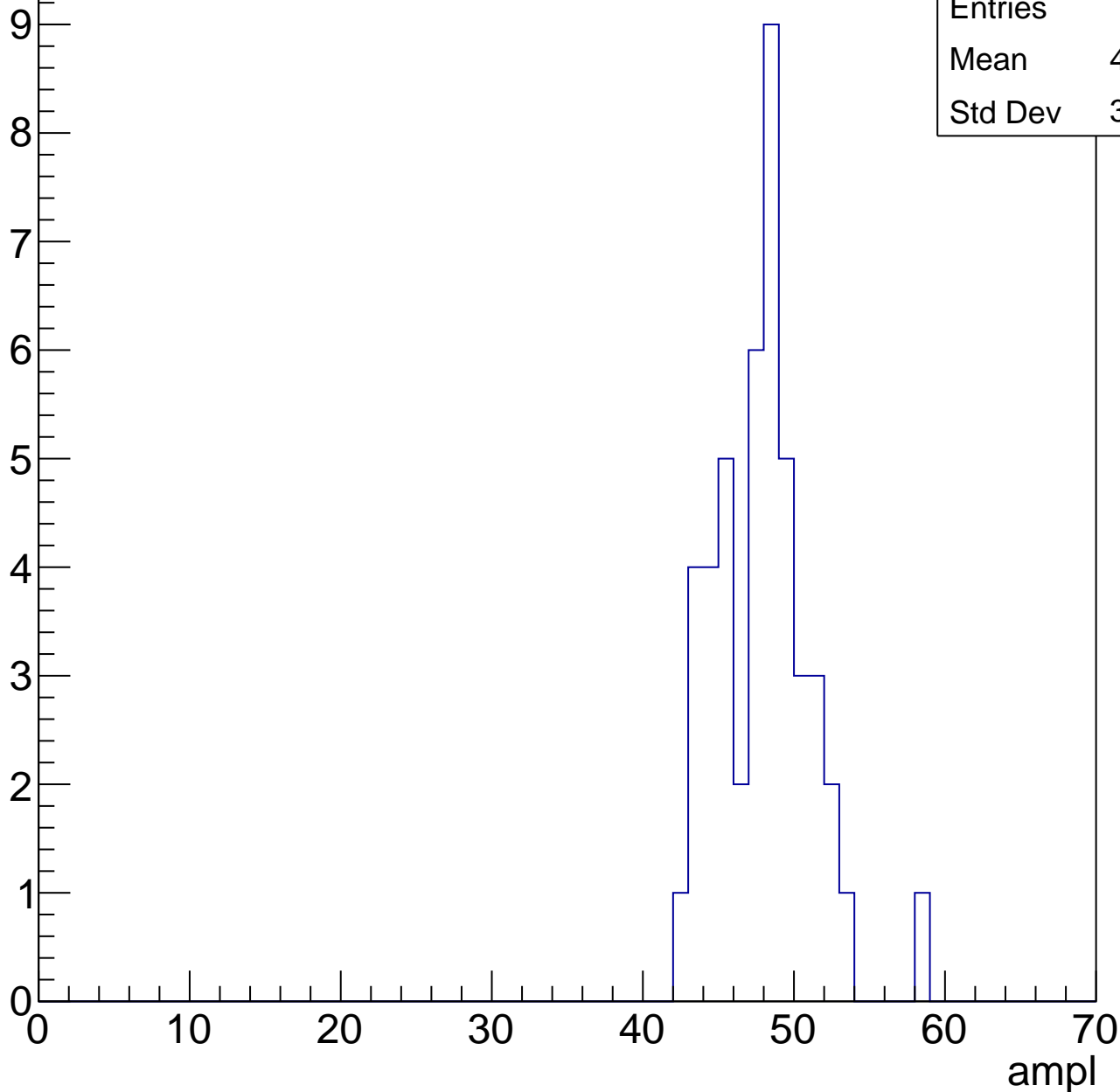
**Gaus Width: 3.5283**



# B1L102S, U3-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

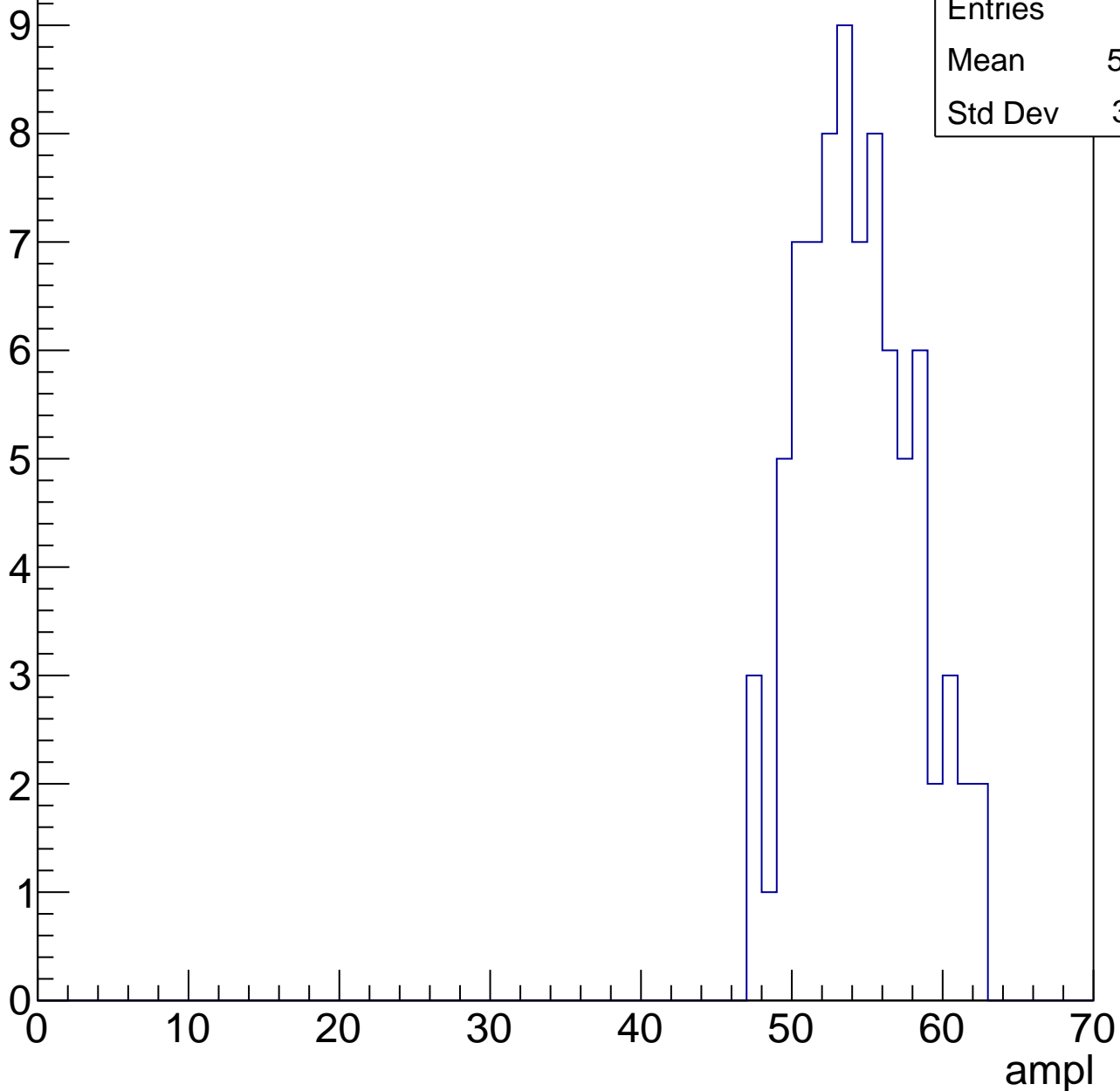


# B1L102S, U3-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	81
Mean	53.89
Std Dev	3.651



# B1L102S, U3-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

7

6

5

4

3

2

1

0

Entries

45

Mean

59.02

Std Dev

2.595

0

0

10

20

30

40

50

60

70

ampl

0

1

2

3

4

5

6

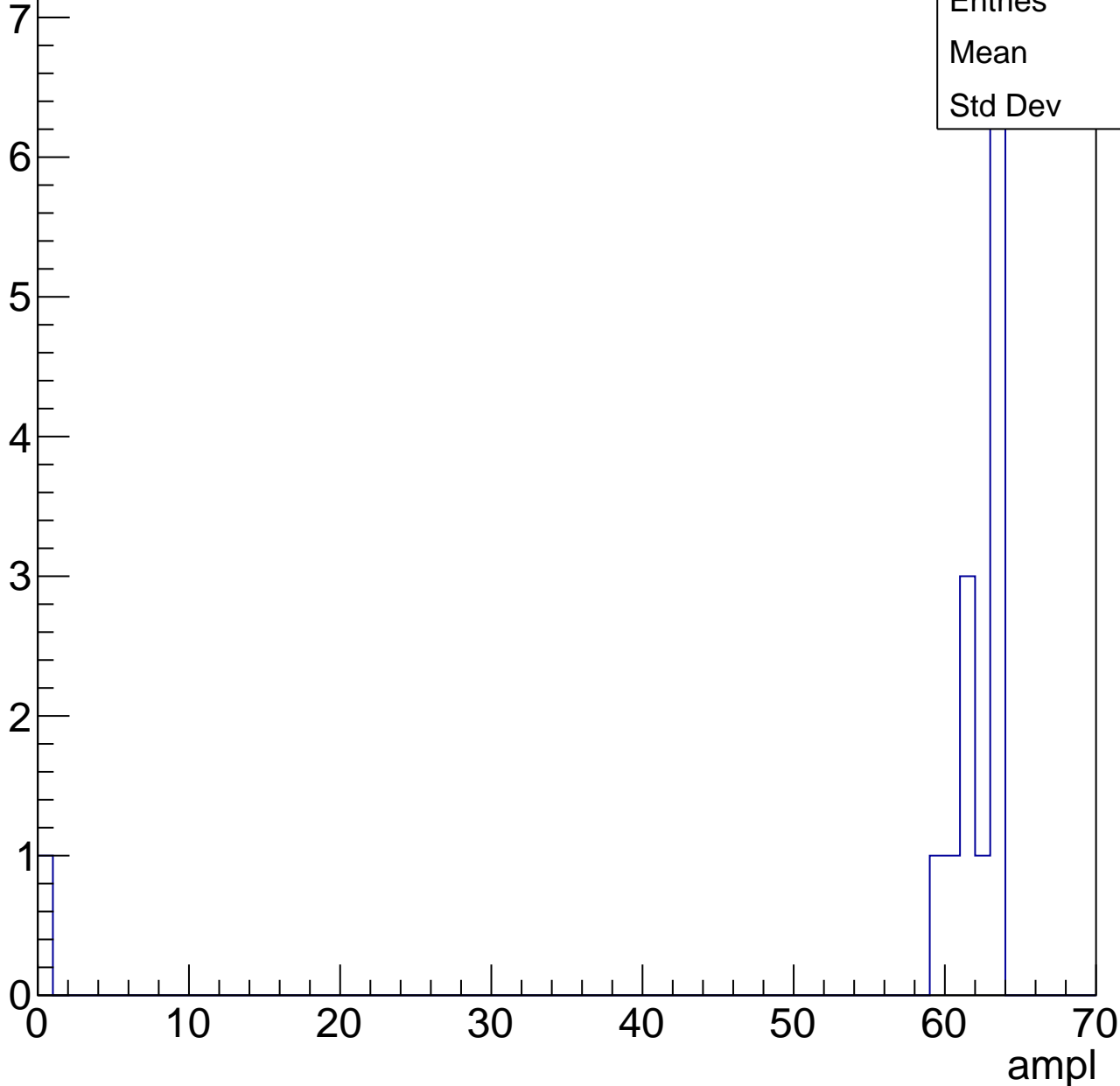
7

# B1L102S, U3-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	14
Mean	57.5
Std Dev	16





# B1L102S, U3-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U3-ch37, adc0

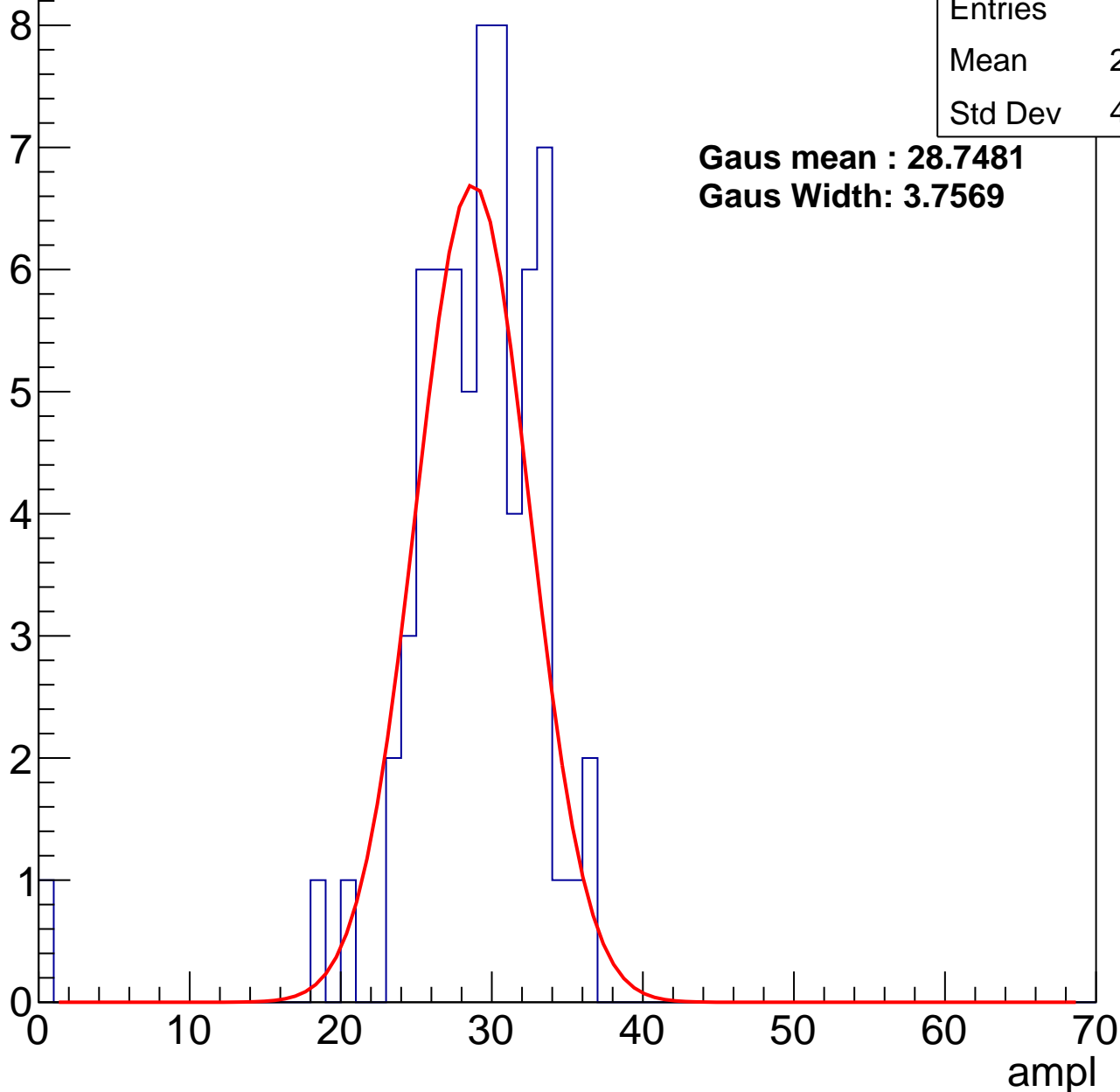
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	28.29
Std Dev	4.977

**Gaus mean : 28.7481**

**Gaus Width: 3.7569**



# B1L102S, U3-ch37, adc1

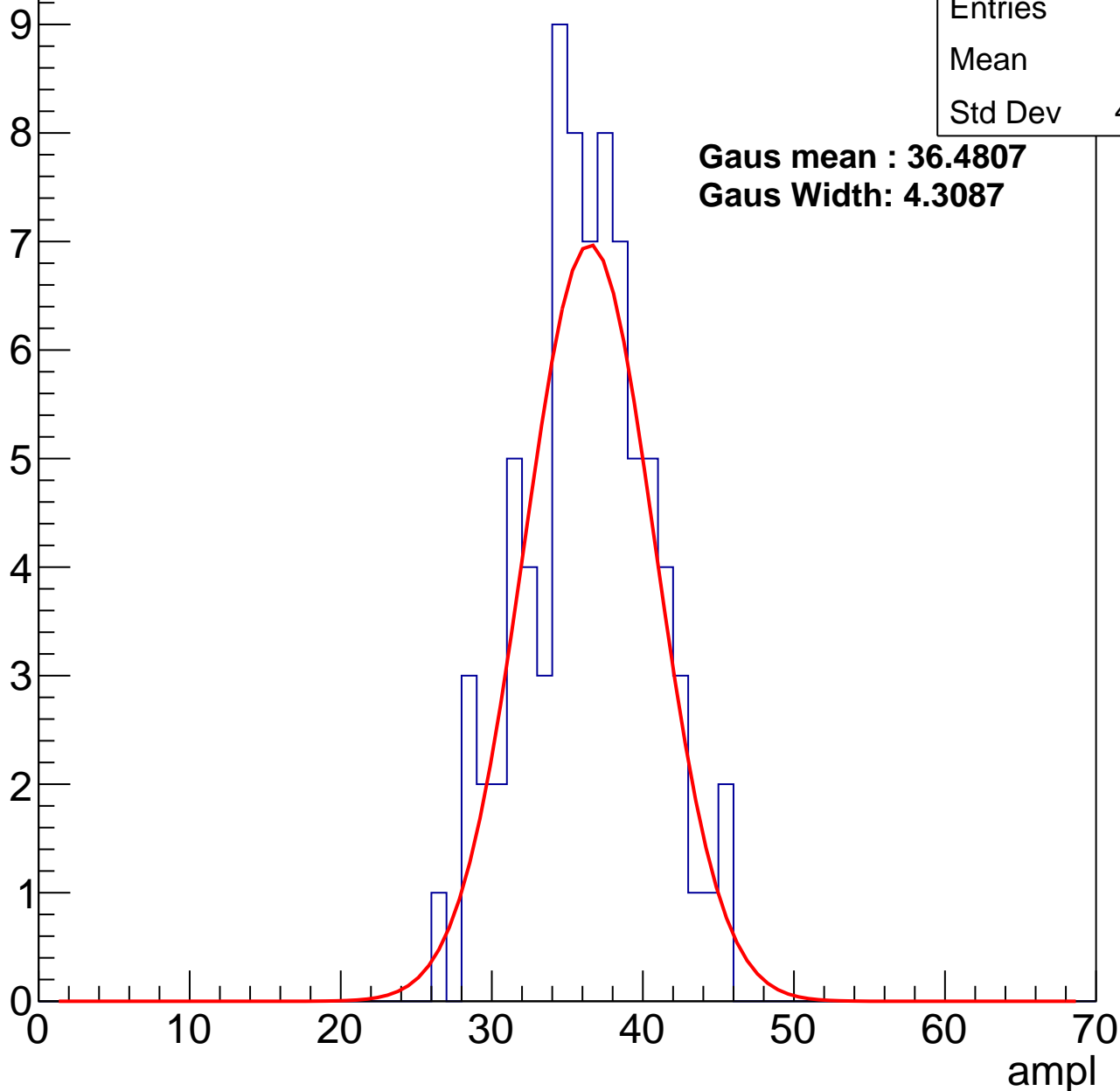
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	35.9
Std Dev	4.131

**Gaus mean : 36.4807**

**Gaus Width: 4.3087**



# B1L102S, U3-ch37, adc2

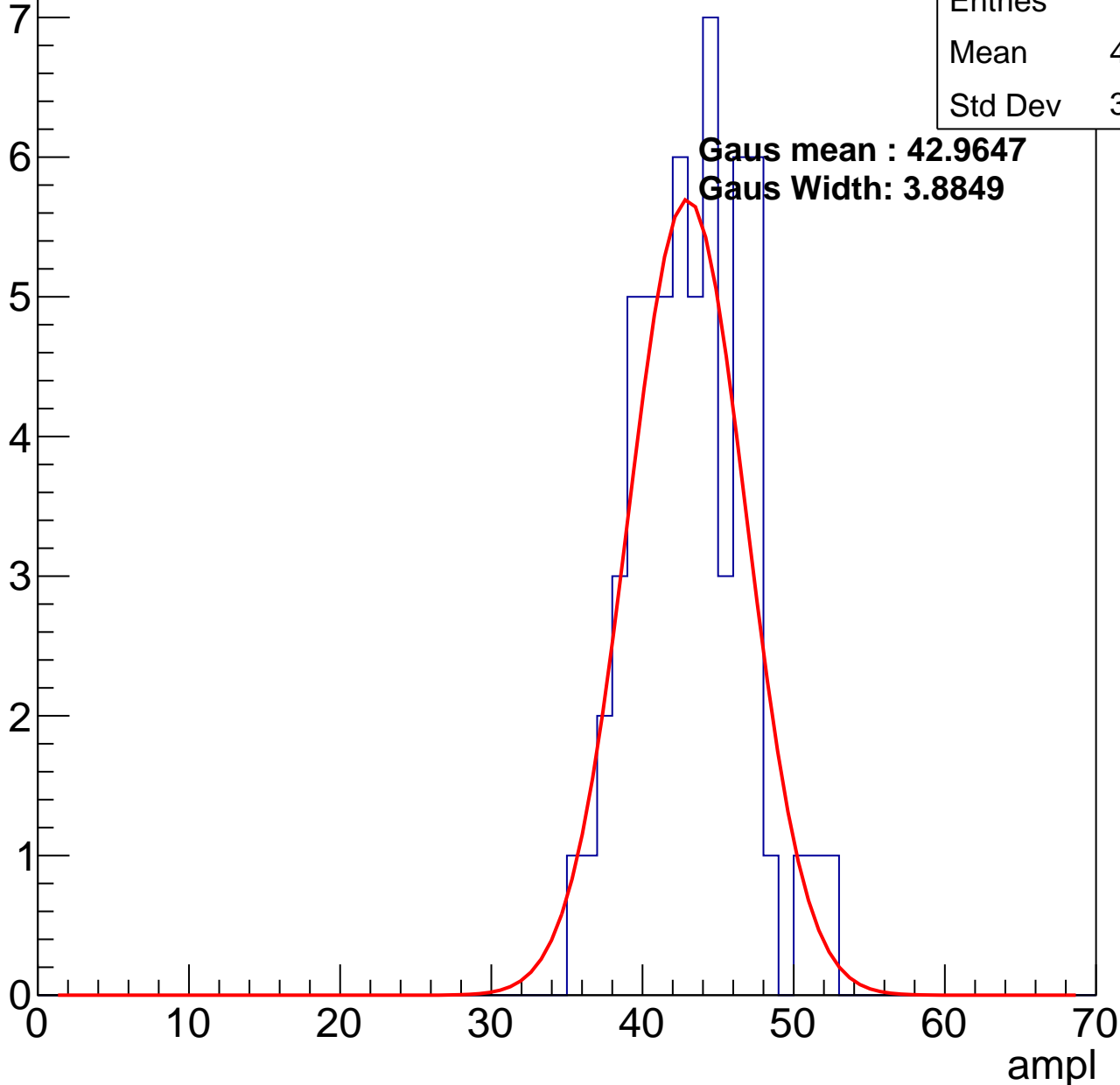
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	42.85
Std Dev	3.677

**Gaus mean : 42.9647**

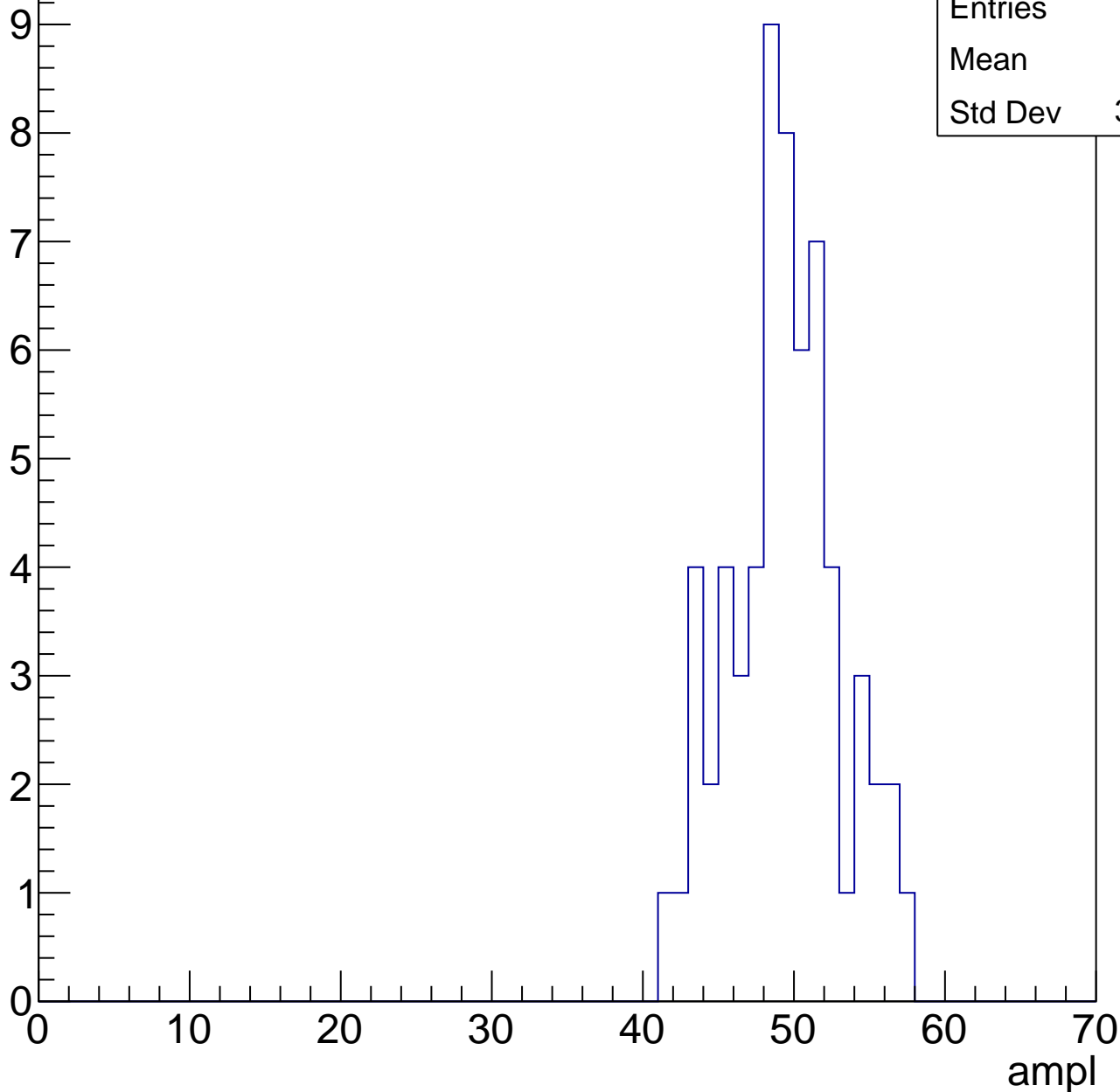
**Gaus Width: 3.8849**



# B1L102S, U3-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

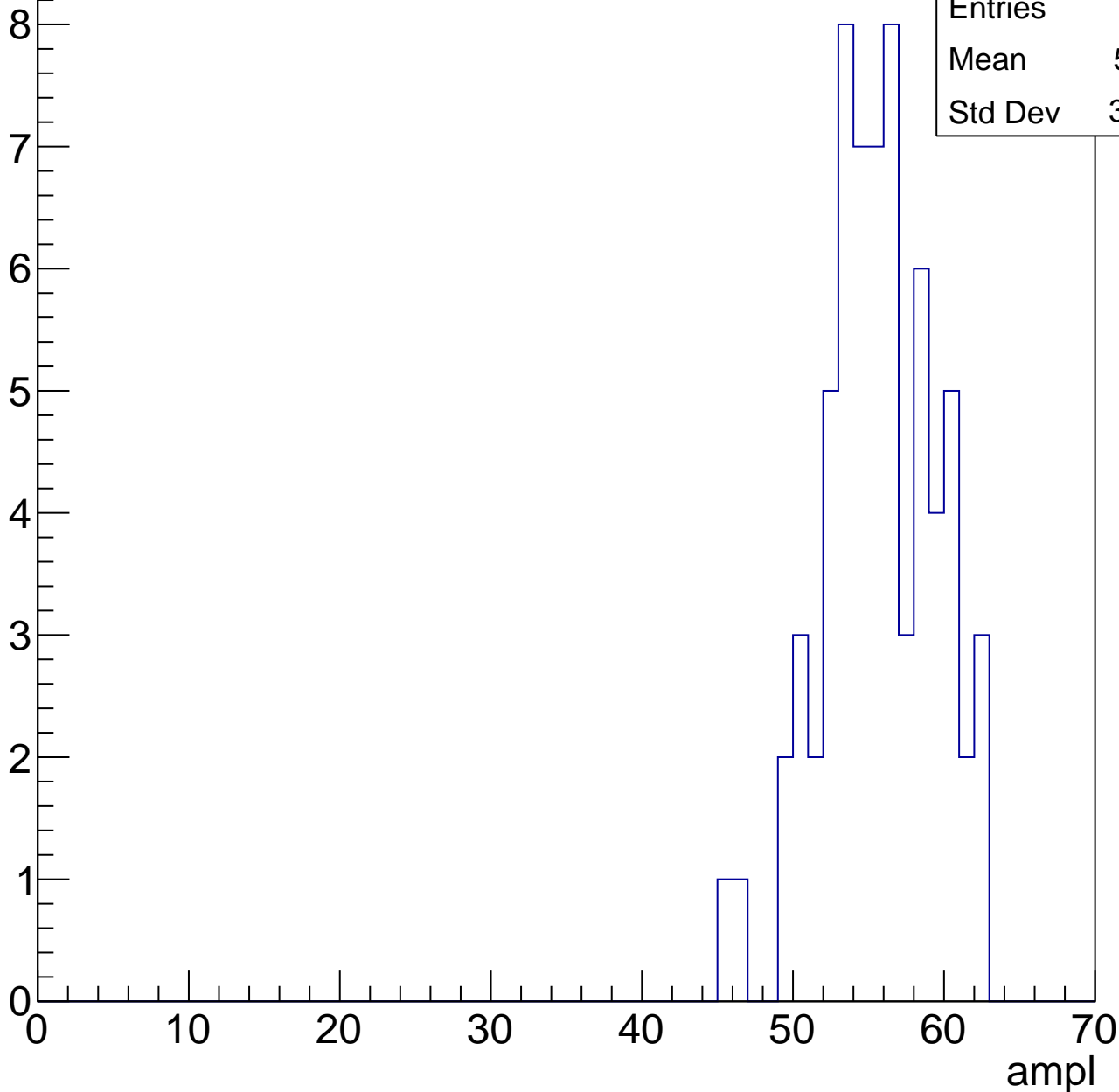


# B1L102S, U3-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	55.21
Std Dev	3.712

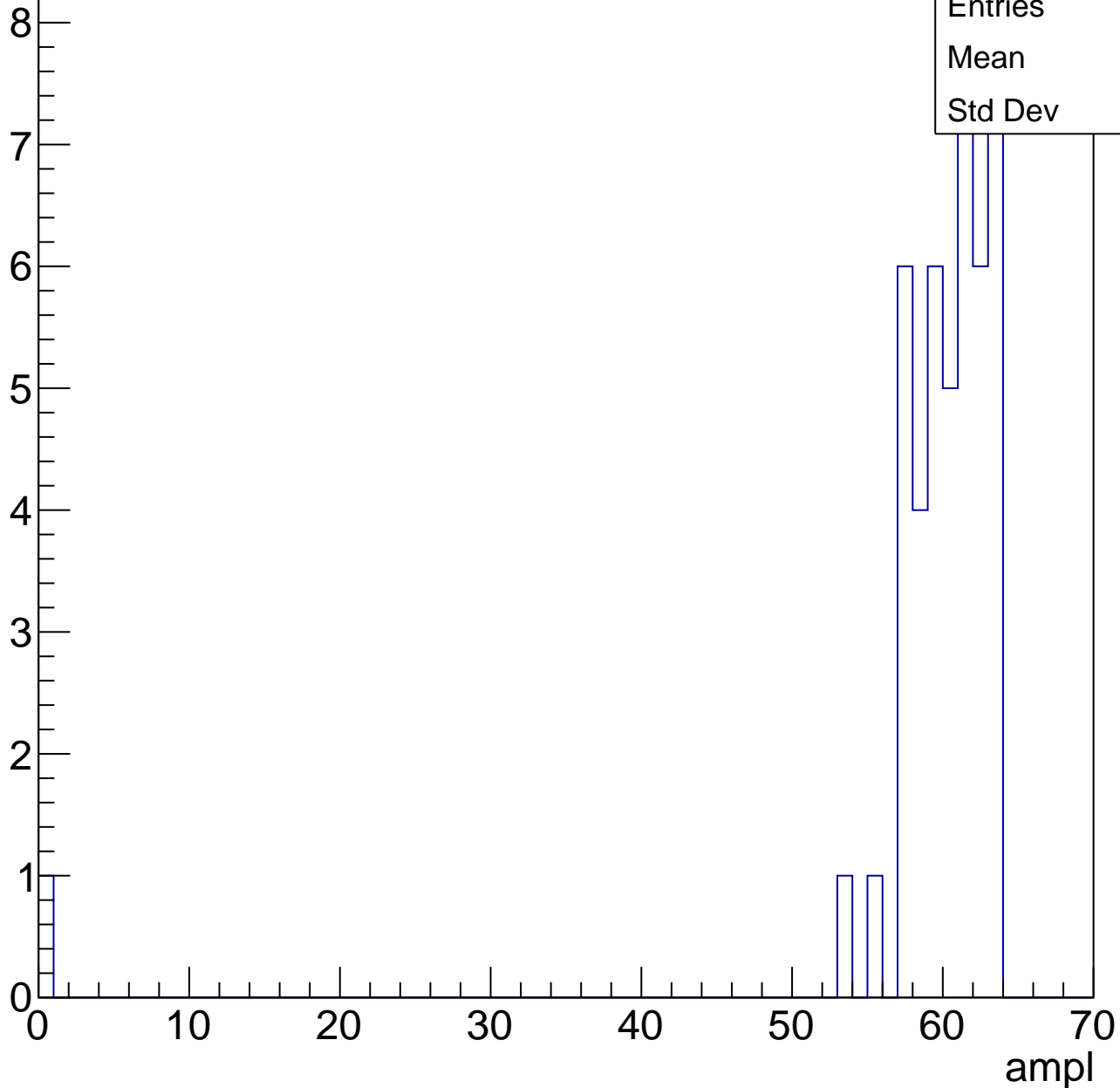


# B1L102S, U3-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

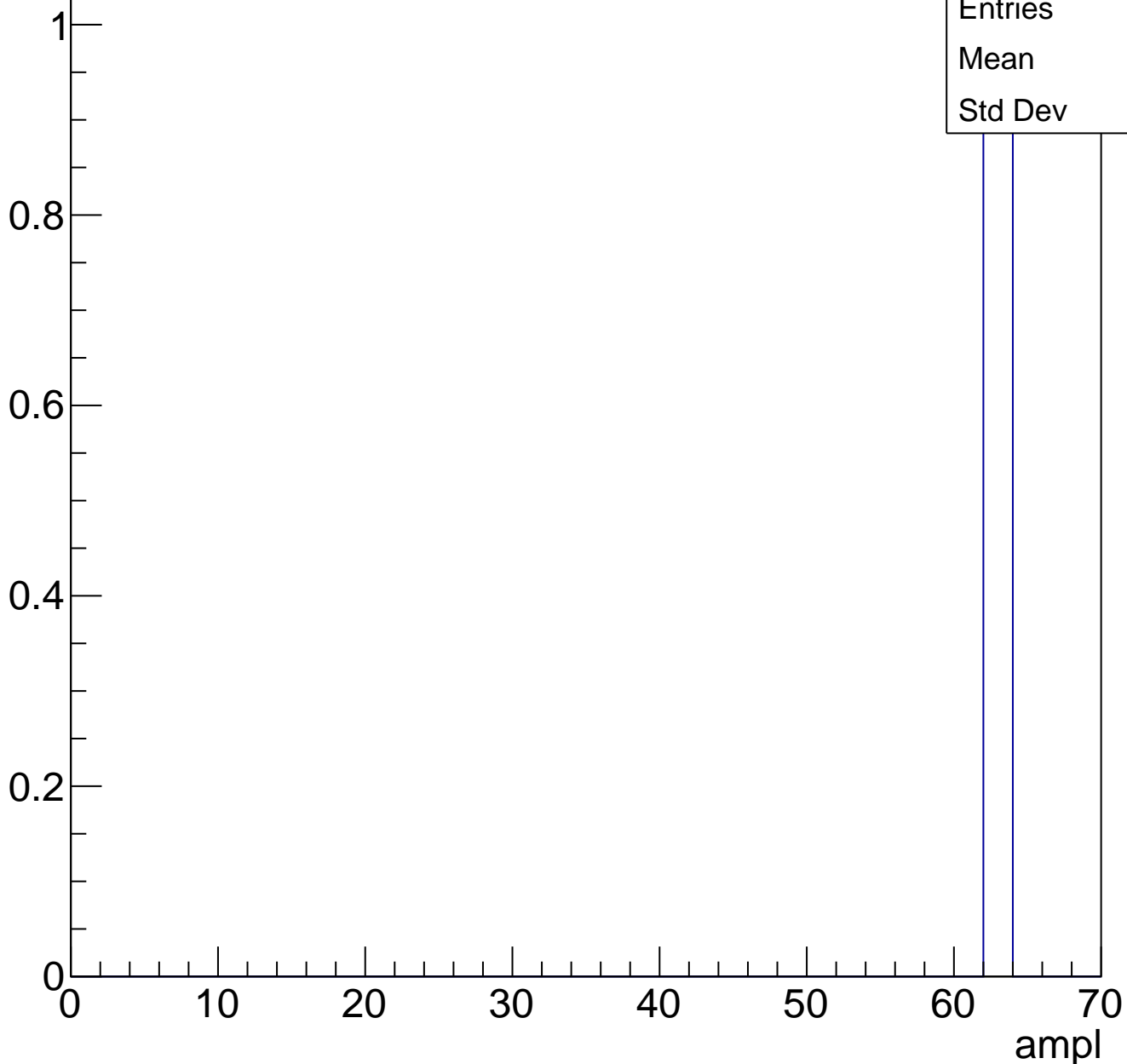
Entries	46
Mean	58.7
Std Dev	9.06



# B1L102S, U3-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch38, adc0

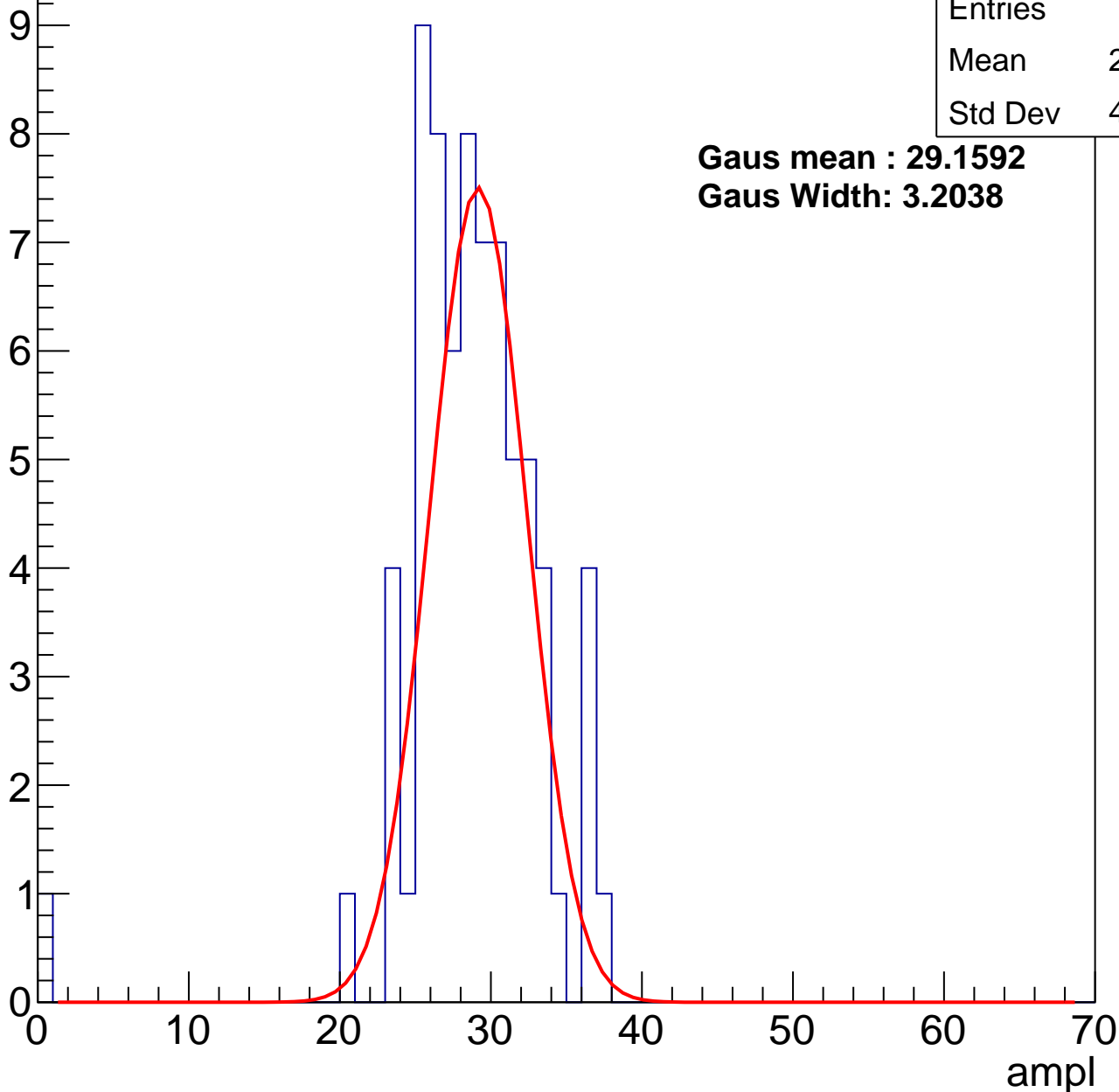
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	28.19
Std Dev	4.878

**Gaus mean : 29.1592**

**Gaus Width: 3.2038**



# B1L102S, U3-ch38, adc1

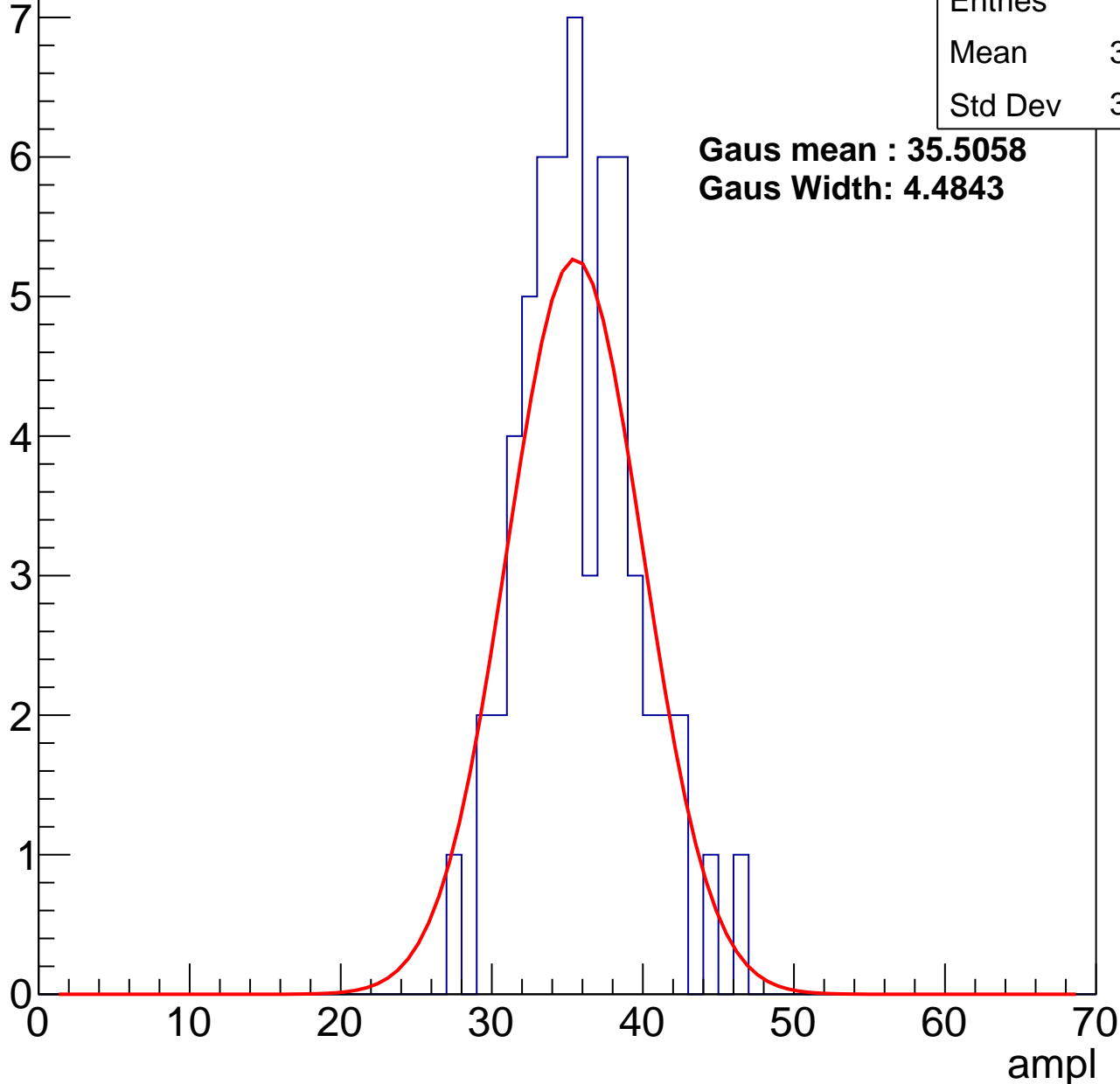
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	35.37
Std Dev	3.835

**Gaus mean : 35.5058**

**Gaus Width: 4.4843**



# B1L102S, U3-ch38, adc2

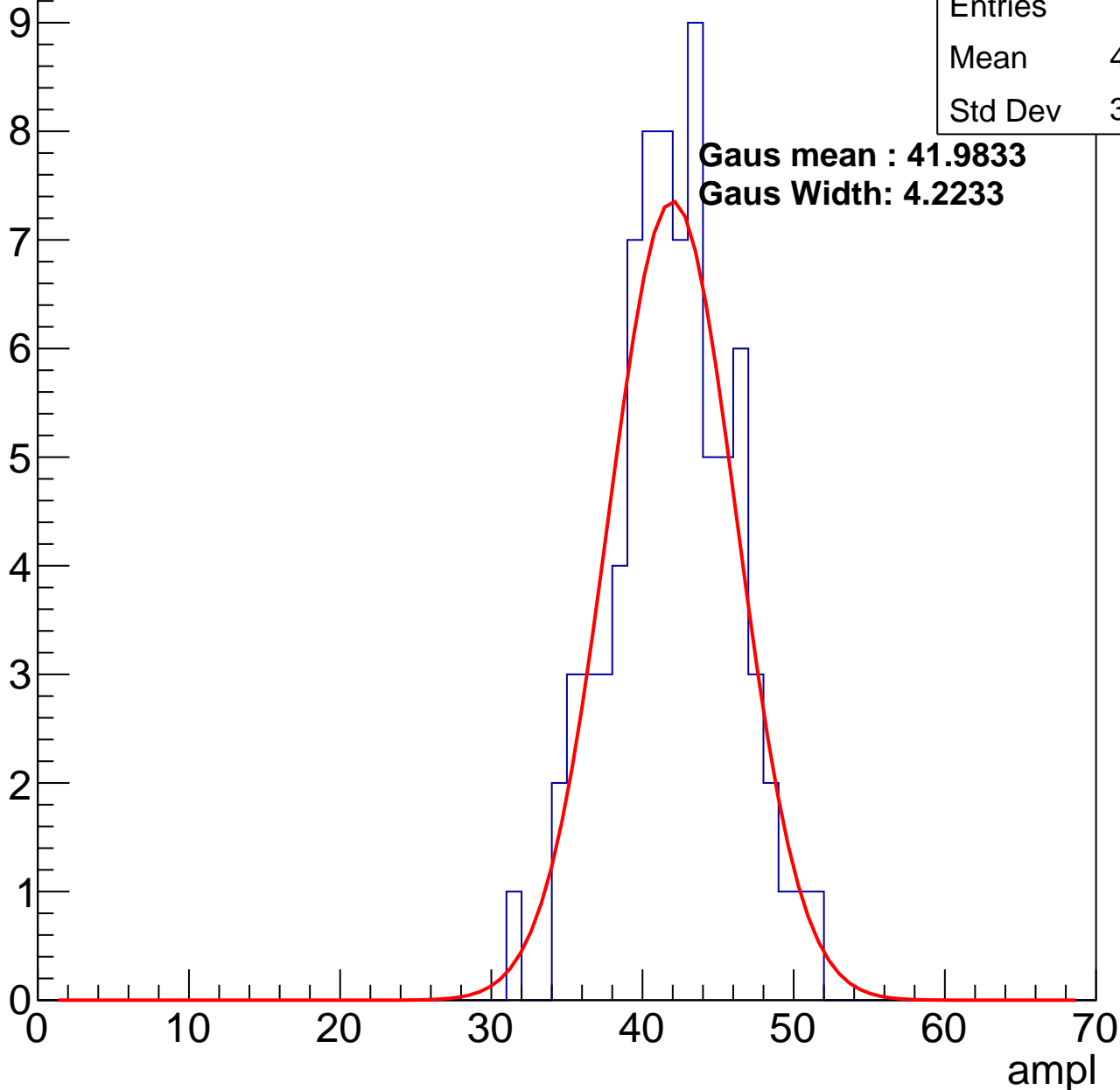
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	41.58
Std Dev	3.967

**Gaus mean : 41.9833**

**Gaus Width: 4.2233**

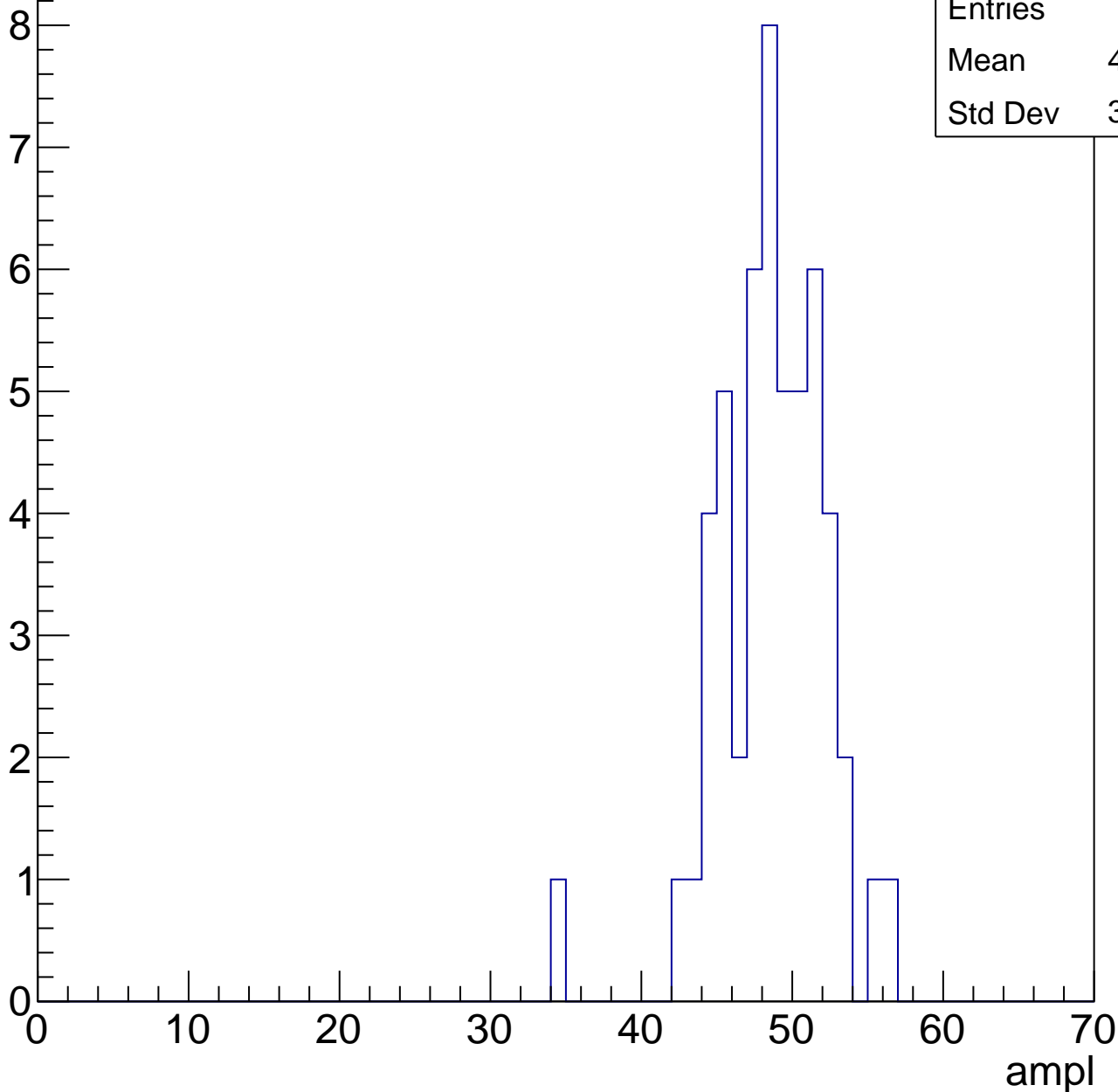


# B1L102S, U3-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	48.15
Std Dev	3.629

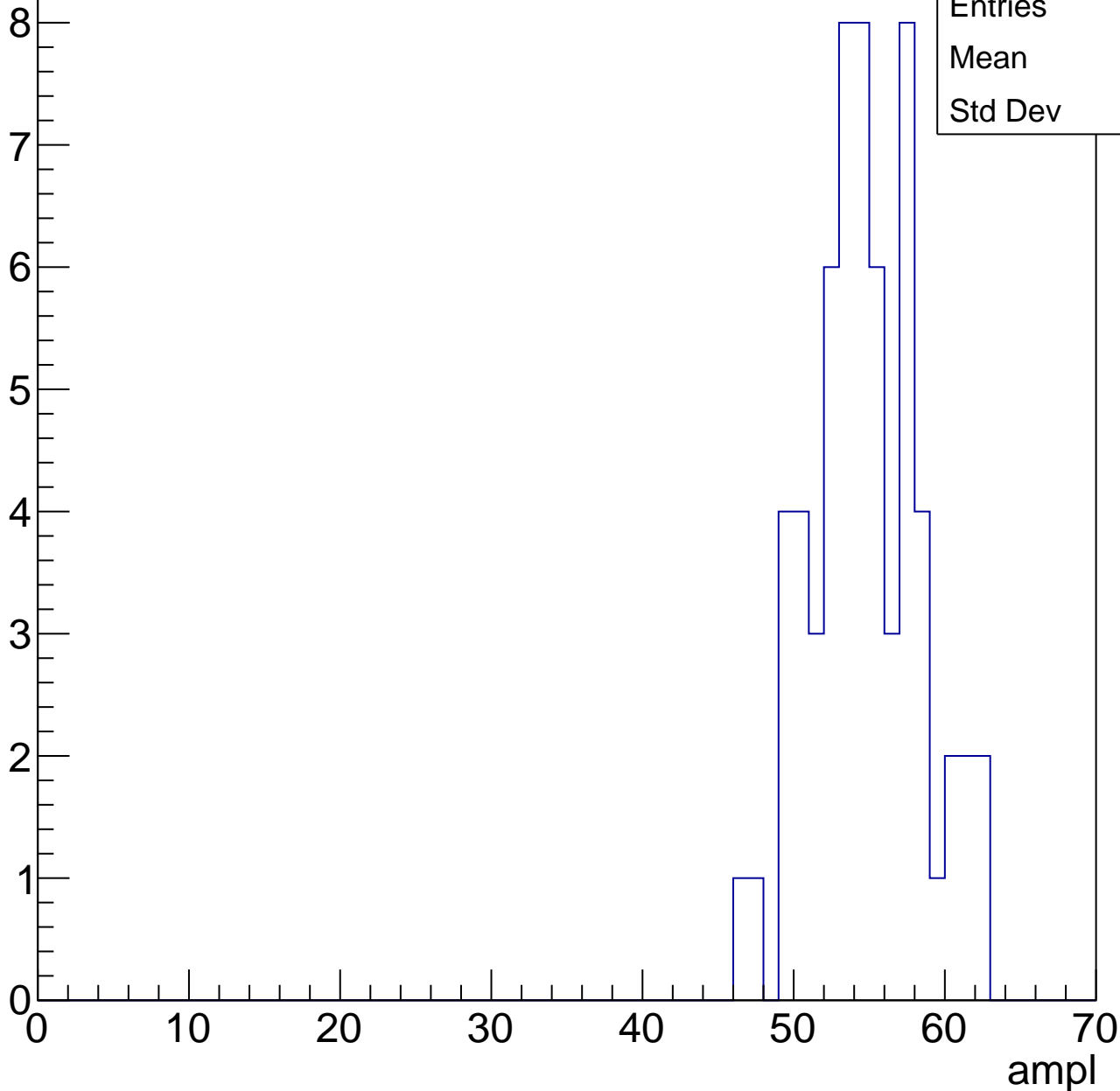


# B1L102S, U3-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	54.3
Std Dev	3.58

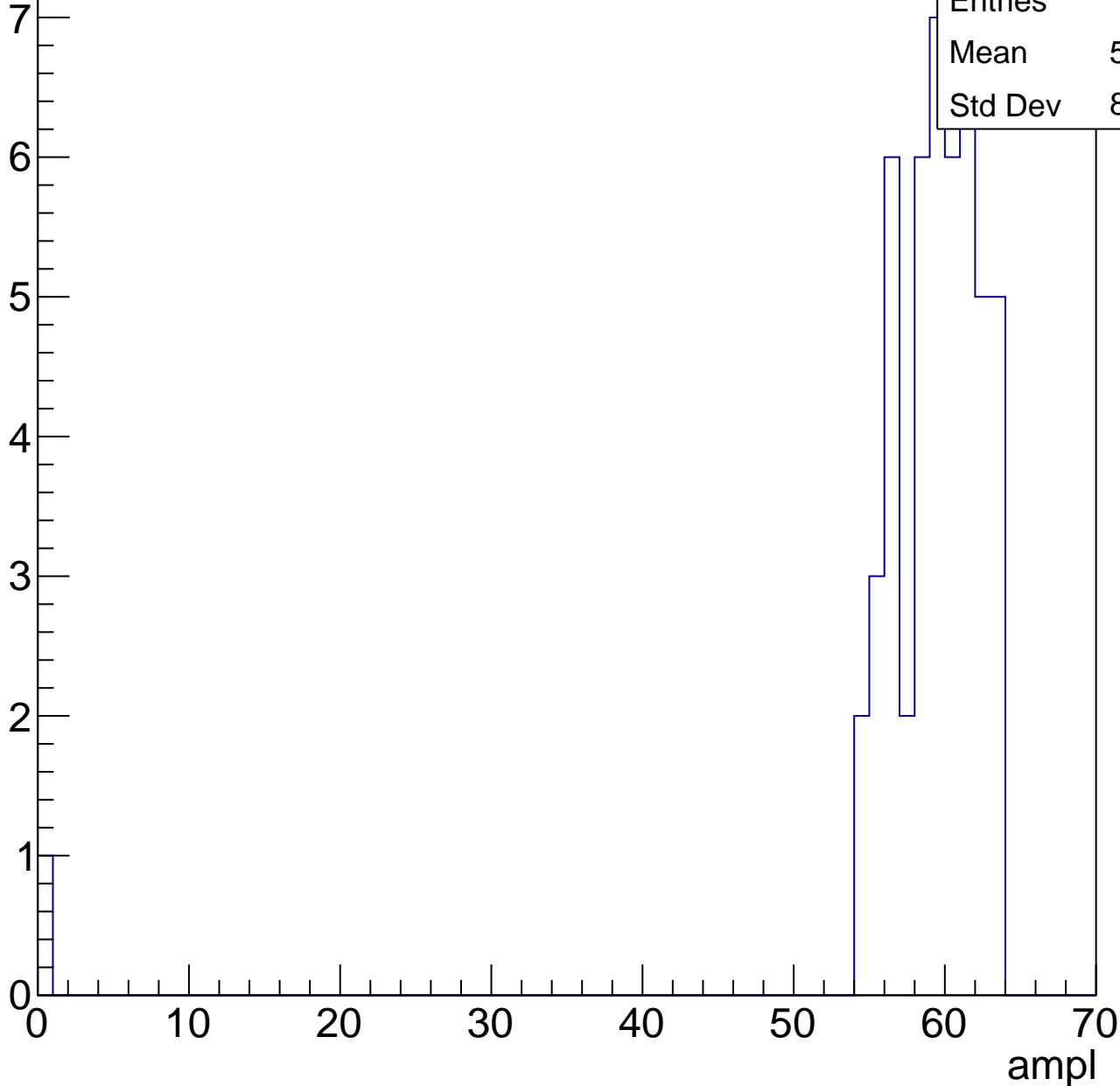


# B1L102S, U3-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	57.92
Std Dev	8.658

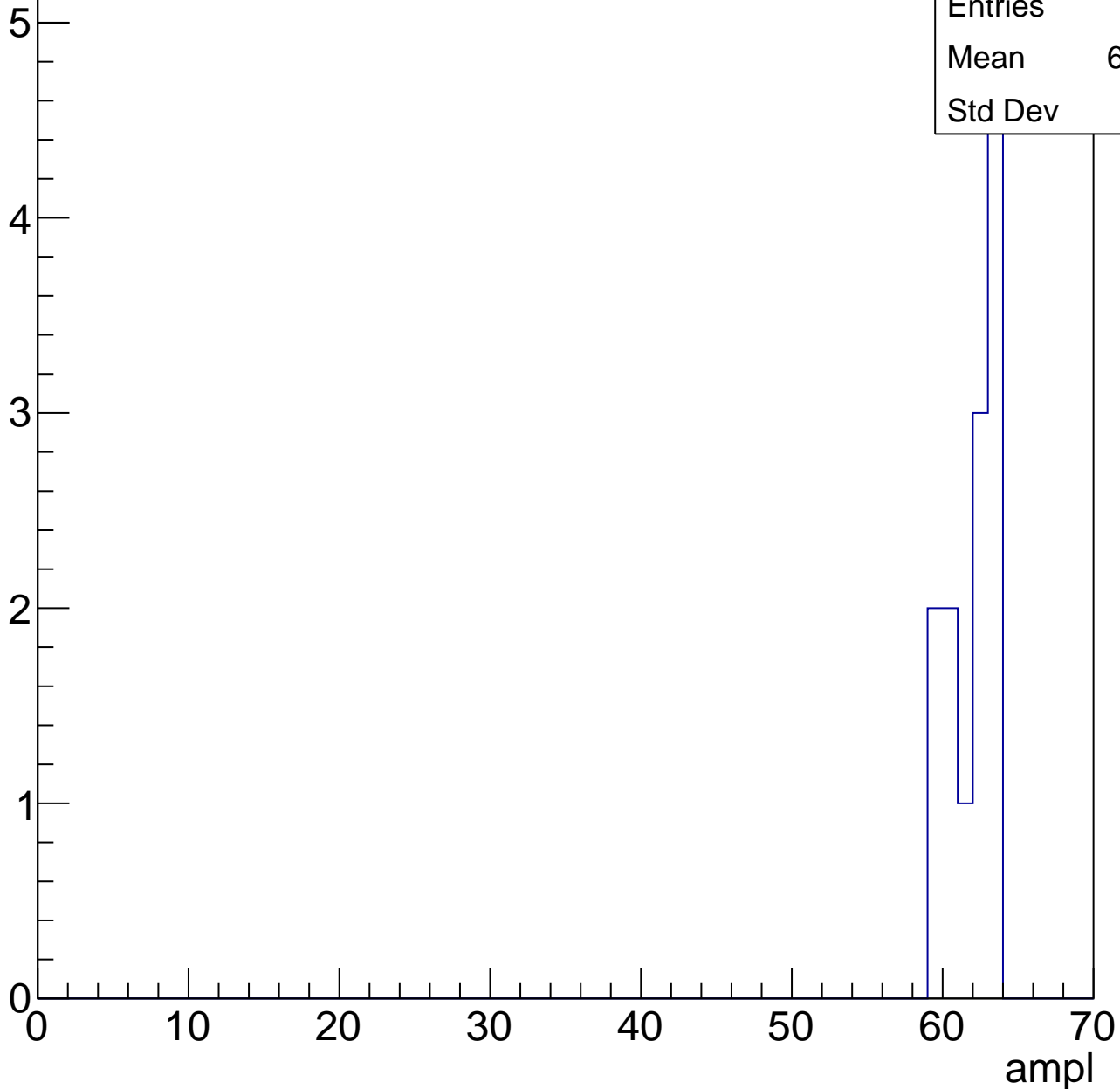


# B1L102S, U3-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	13
Mean	61.54
Std Dev	1.5





# B1L102S, U3-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch39, adc0

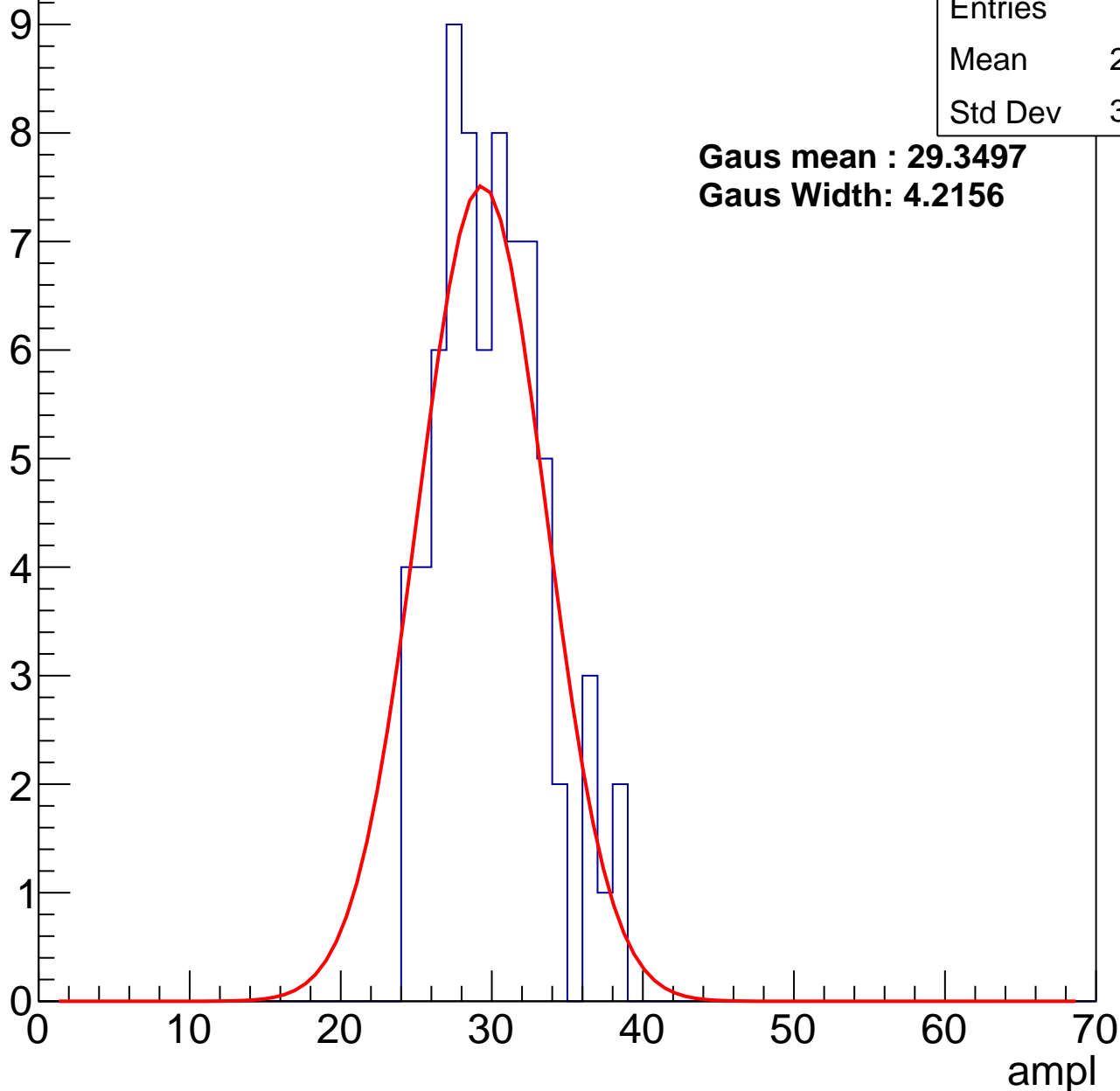
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	29.56
Std Dev	3.419

**Gaus mean : 29.3497**

**Gaus Width: 4.2156**



# B1L102S, U3-ch39, adc1

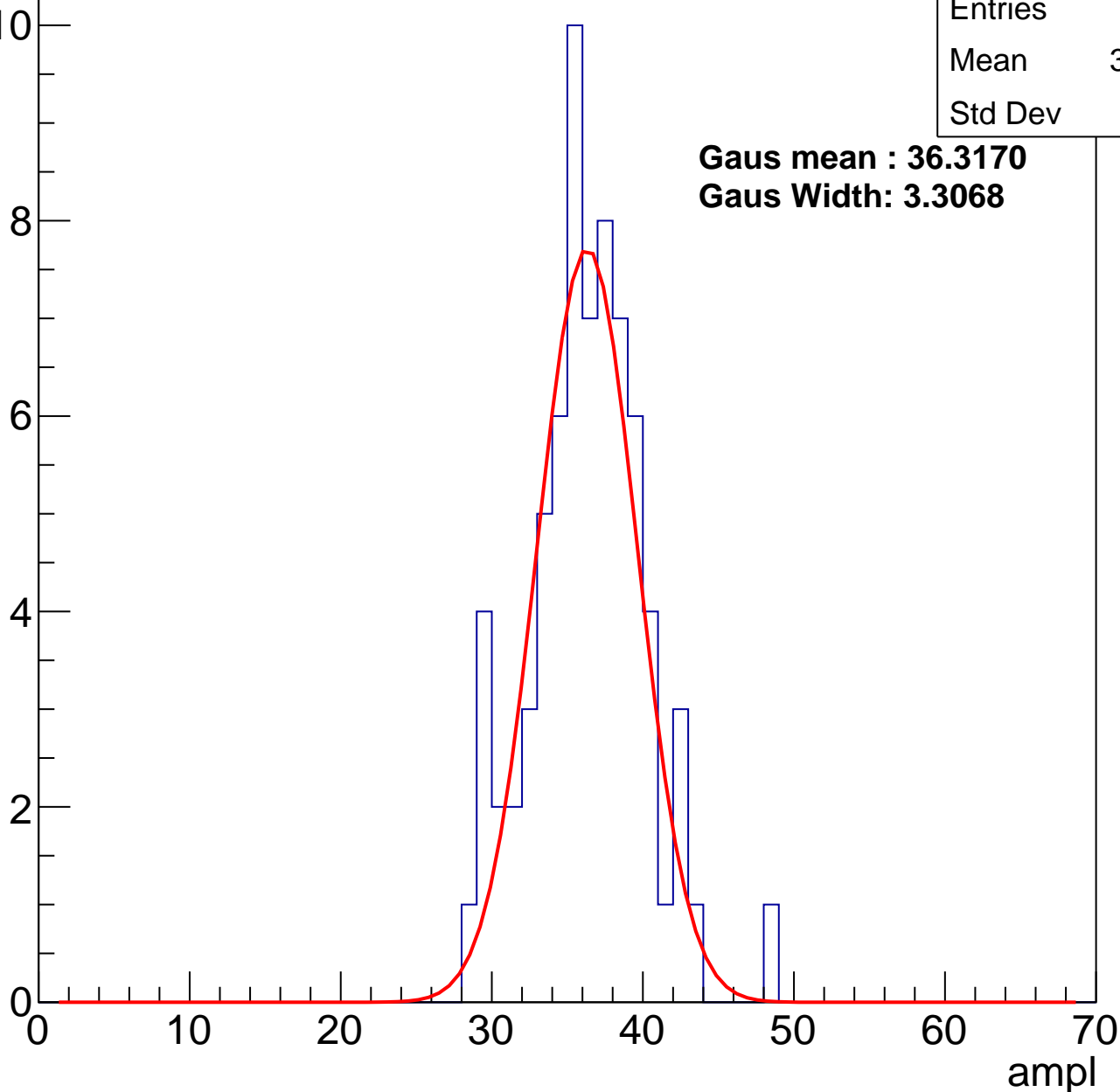
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	35.87
Std Dev	3.73

**Gaus mean : 36.3170**

**Gaus Width: 3.3068**



# B1L102S, U3-ch39, adc2

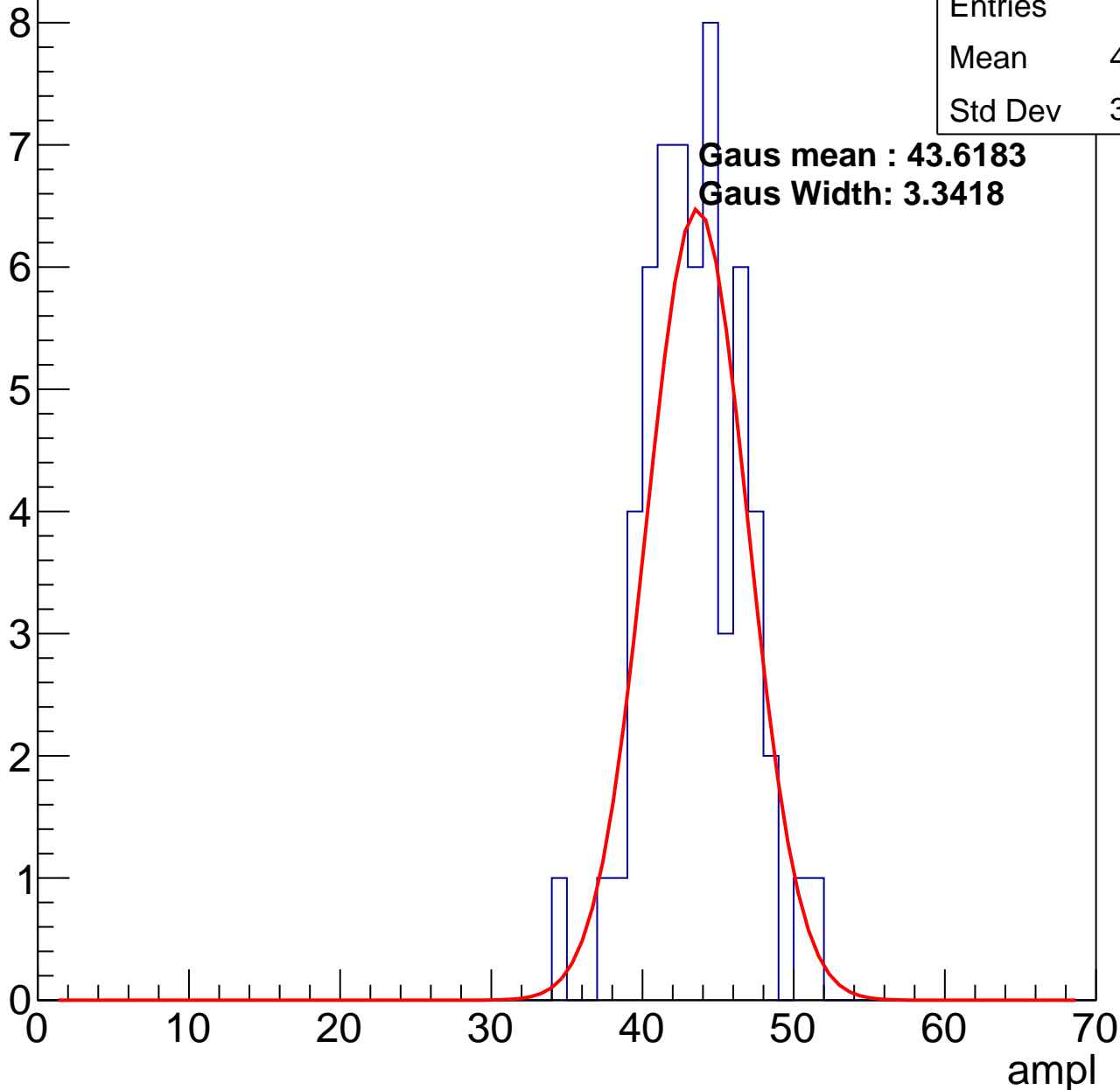
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	42.97
Std Dev	3.205

**Gaus mean : 43.6183**

**Gaus Width: 3.3418**

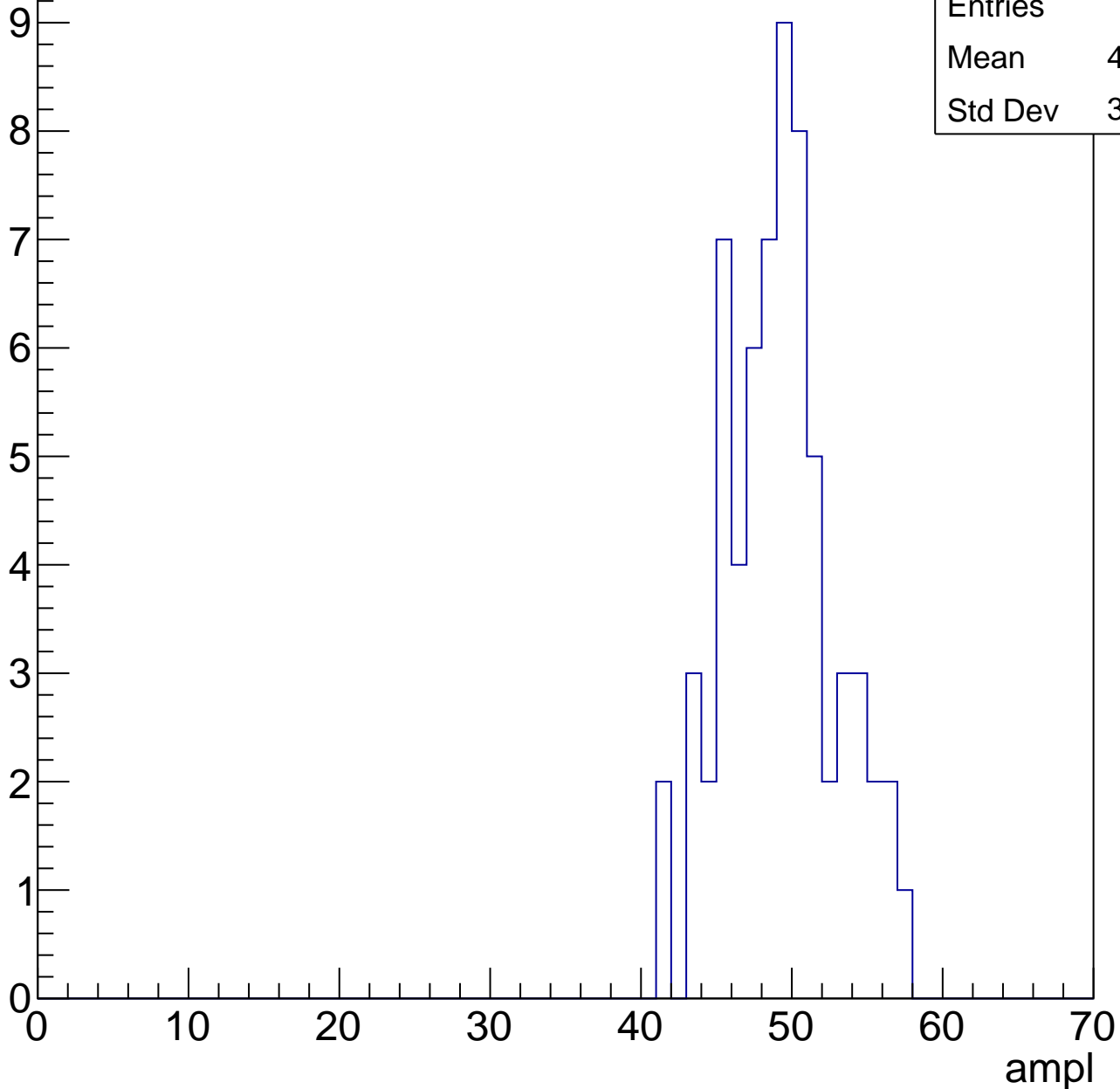


# B1L102S, U3-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

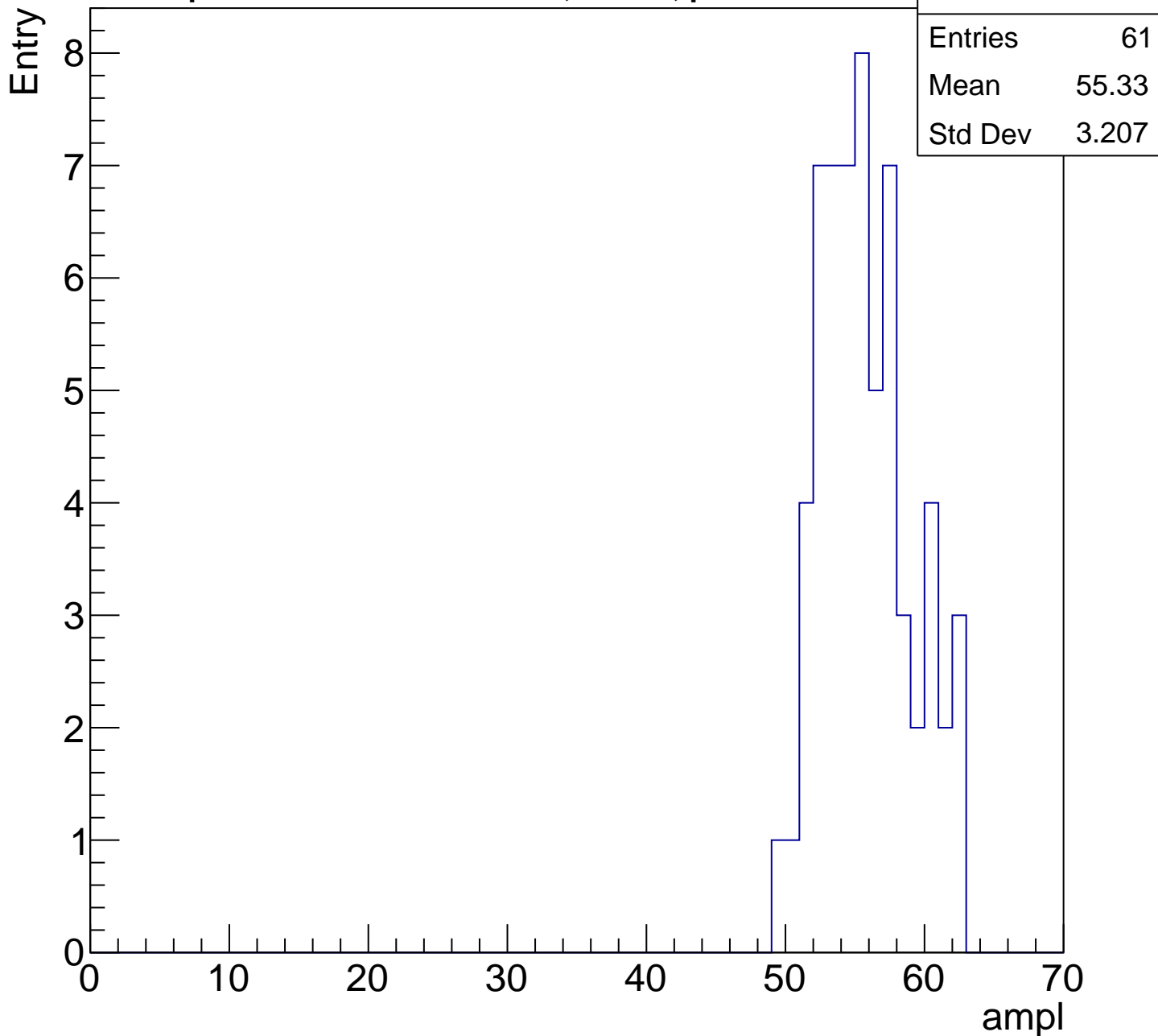
Entry

Entries	66
Mean	48.73
Std Dev	3.616



# B1L102S, U3-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

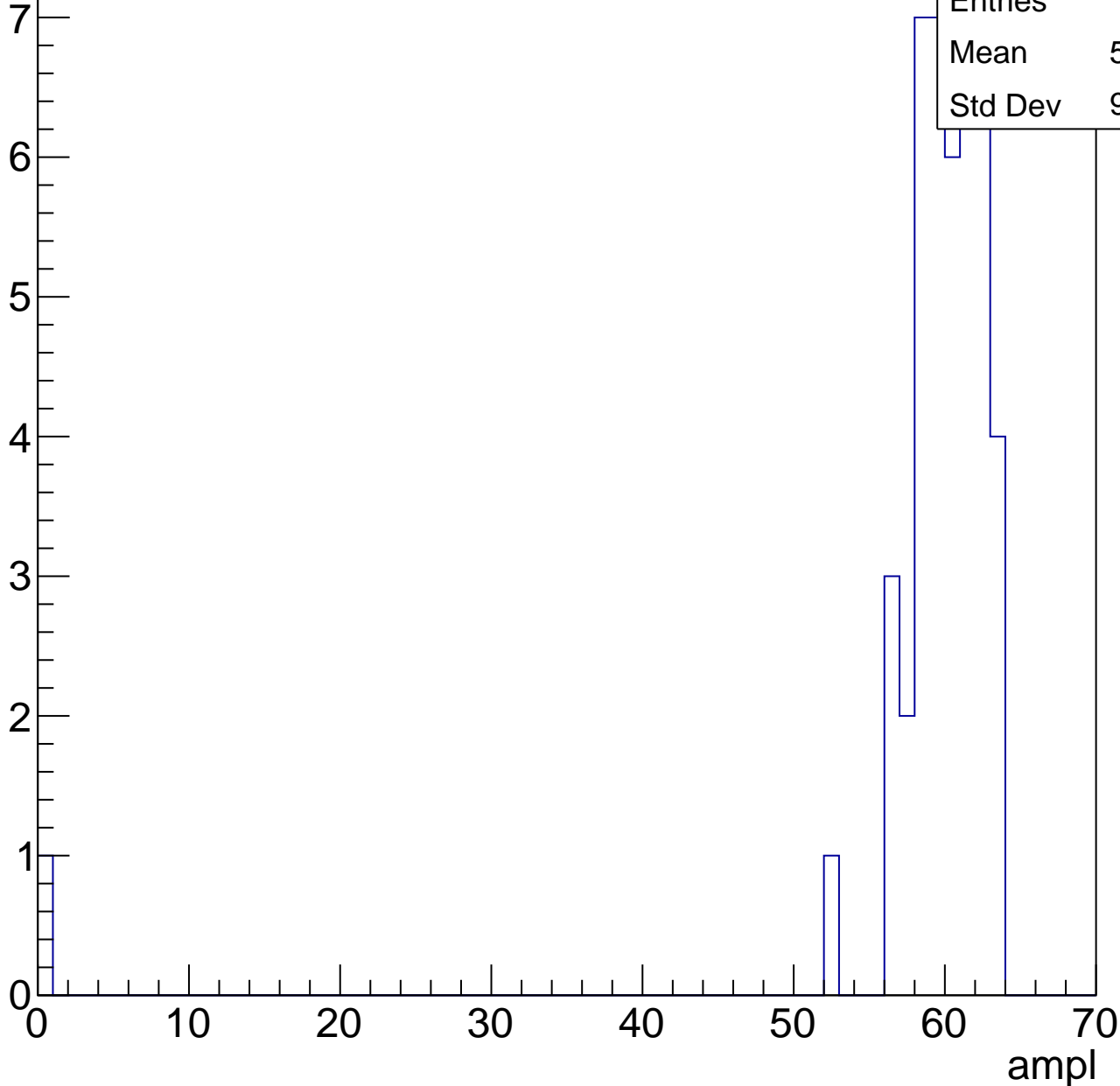


# B1L102S, U3-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	58.36
Std Dev	9.085

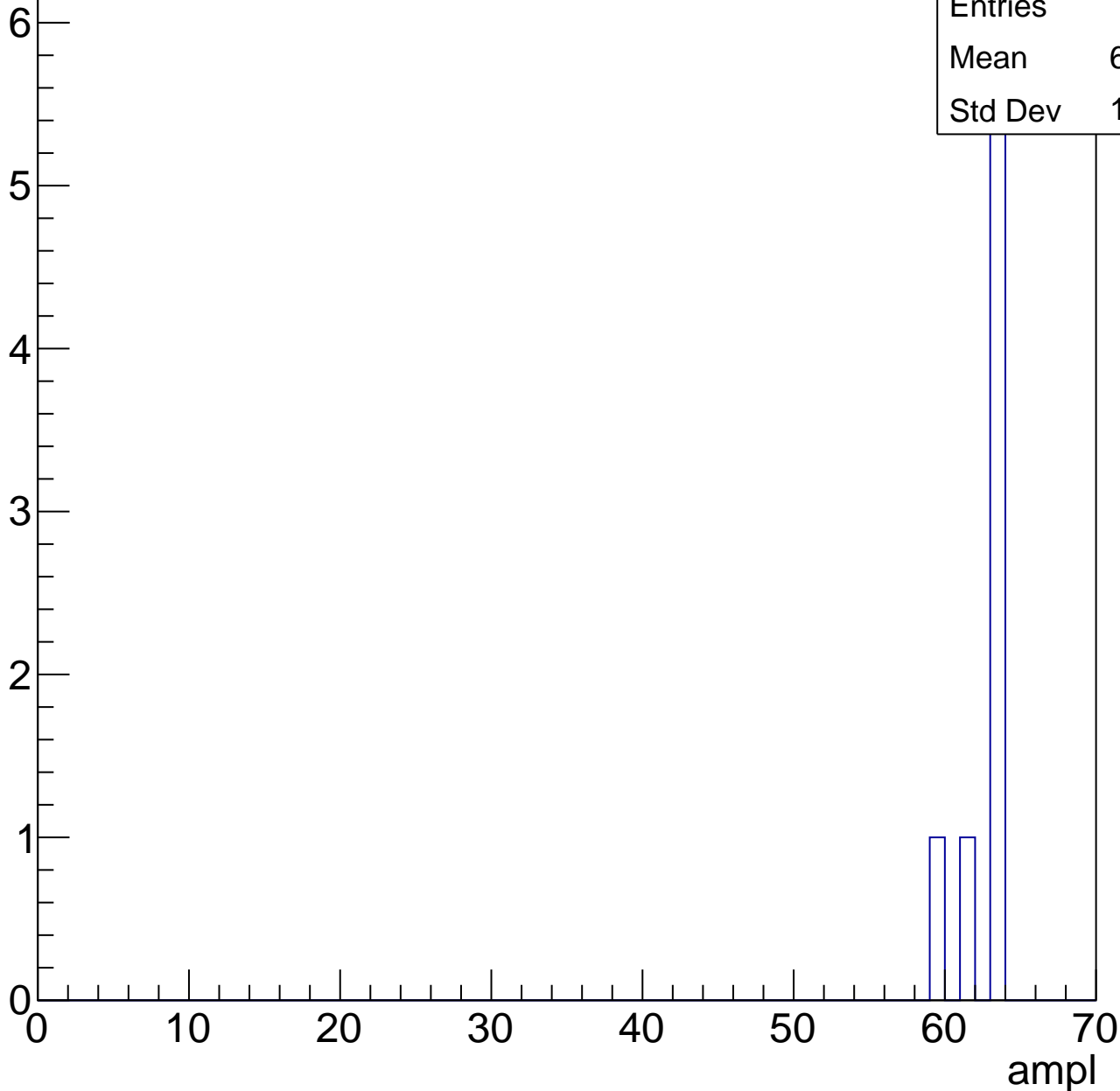


# B1L102S, U3-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	8
Mean	62.25
Std Dev	1.392





# B1L102S, U3-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U3-ch40, adc0

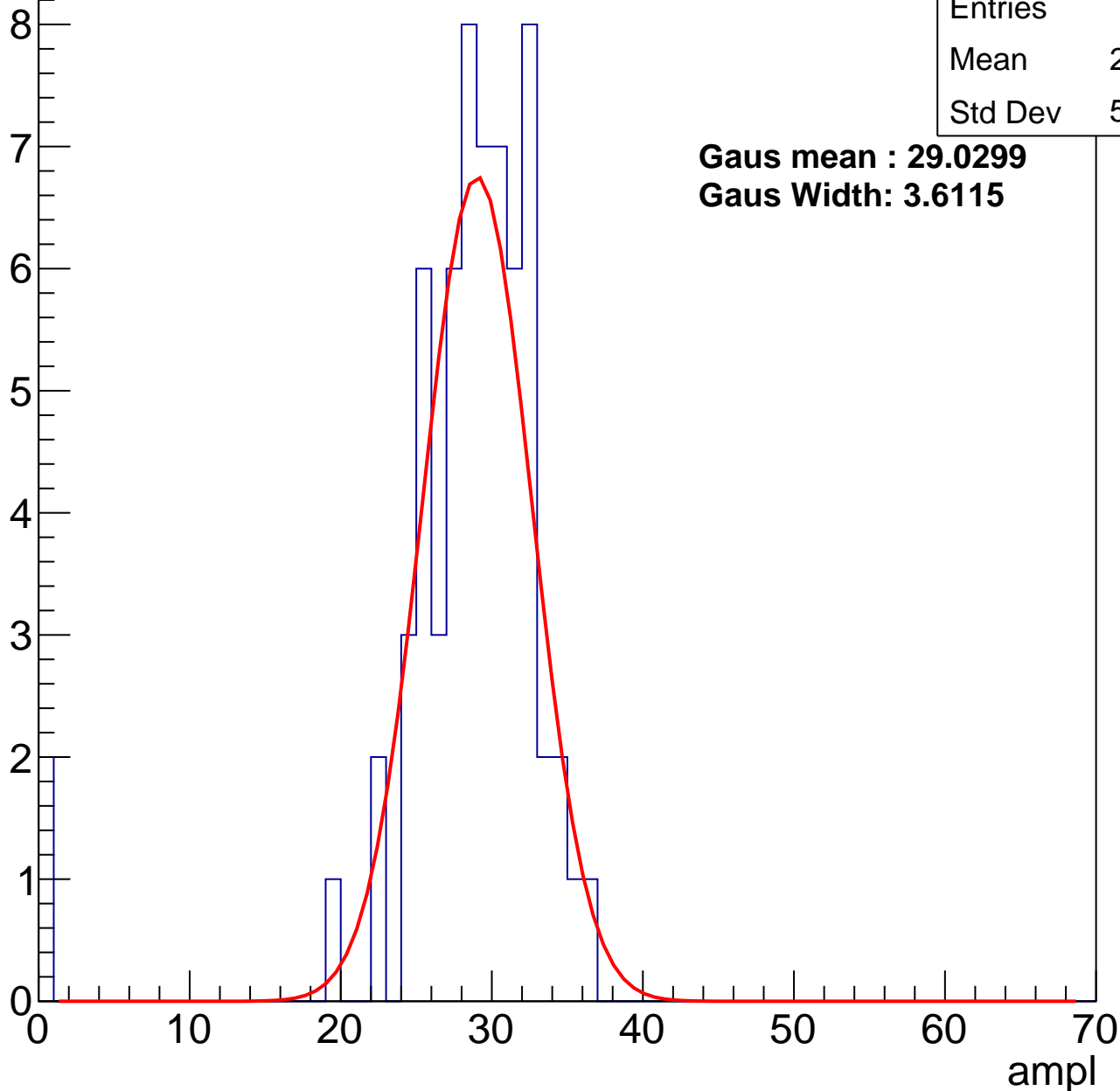
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	27.83
Std Dev	5.937

**Gaus mean : 29.0299**

**Gaus Width: 3.6115**



# B1L102S, U3-ch40, adc1

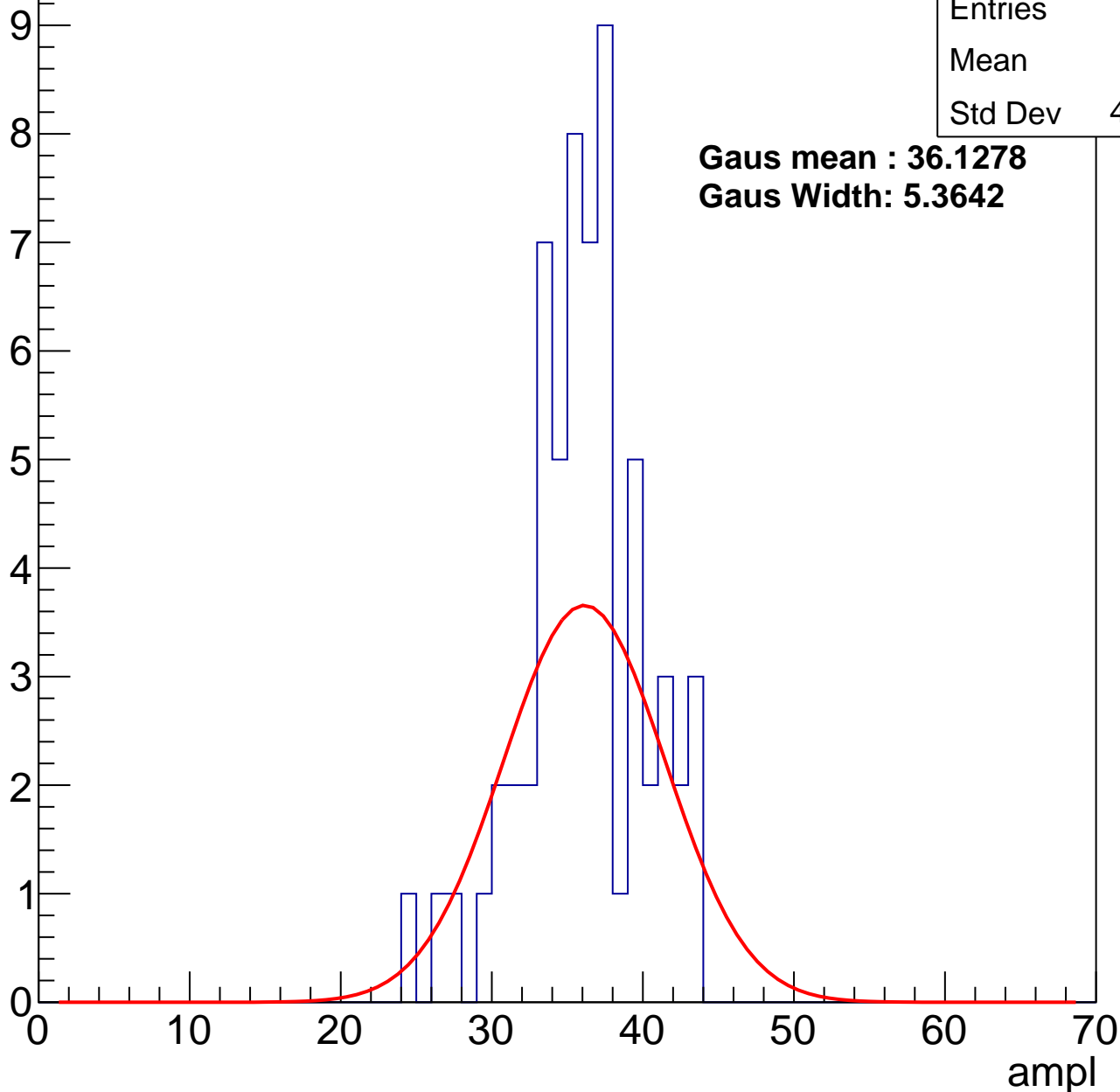
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	35.6
Std Dev	4.002

**Gaus mean : 36.1278**

**Gaus Width: 5.3642**



# B1L102S, U3-ch40, adc2

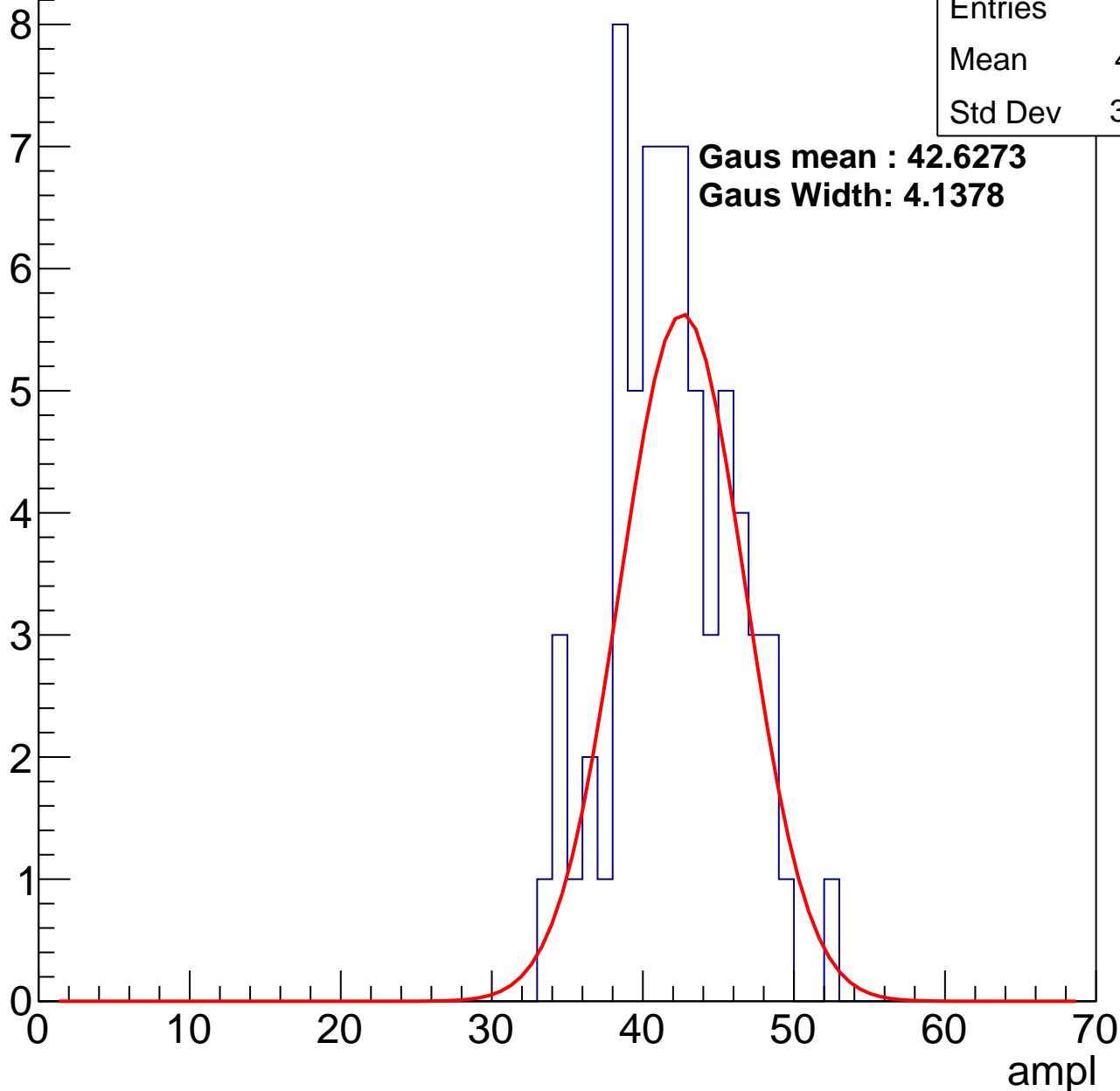
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	41.51
Std Dev	3.994

**Gaus mean : 42.6273**

**Gaus Width: 4.1378**

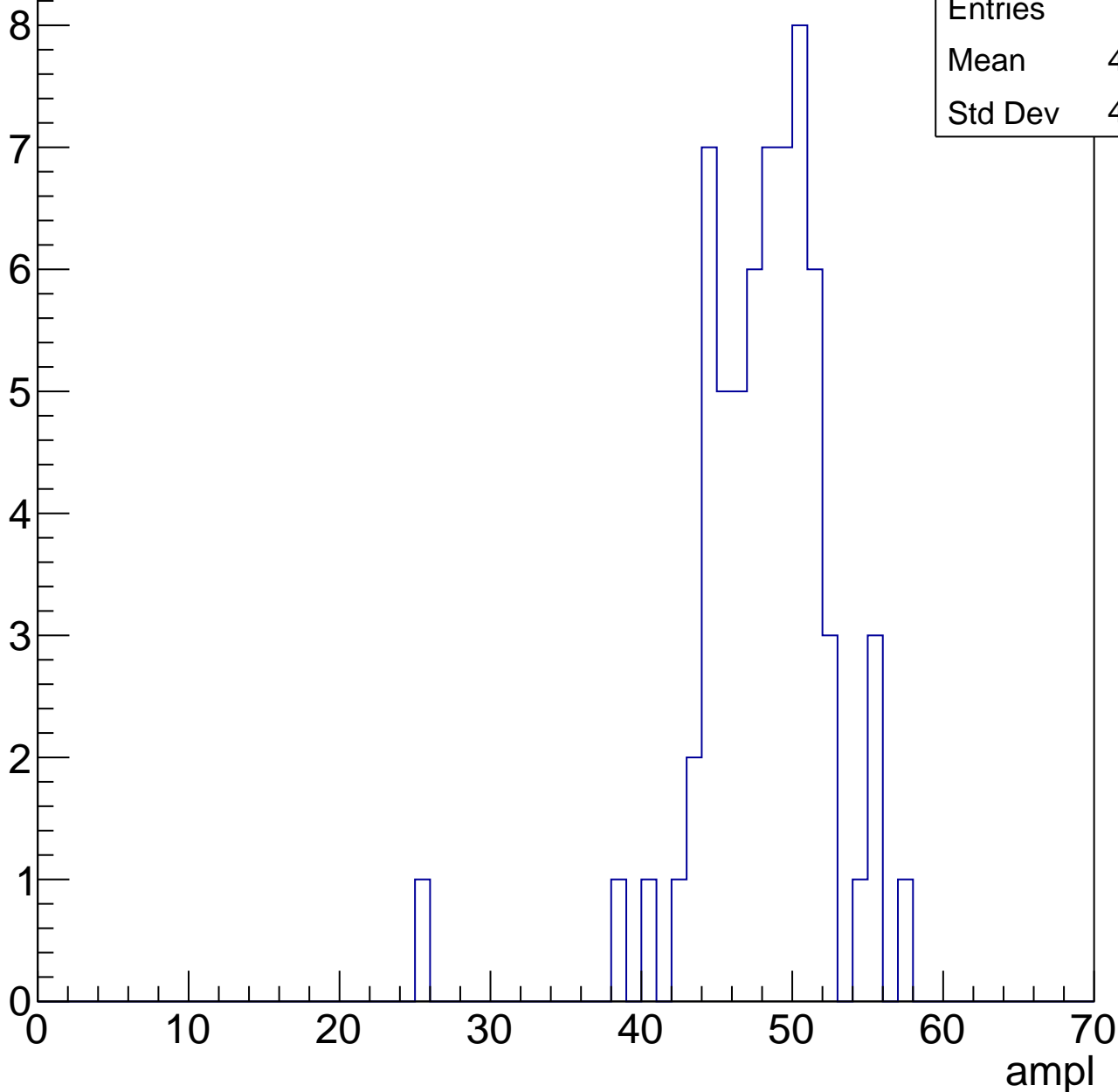


# B1L102S, U3-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

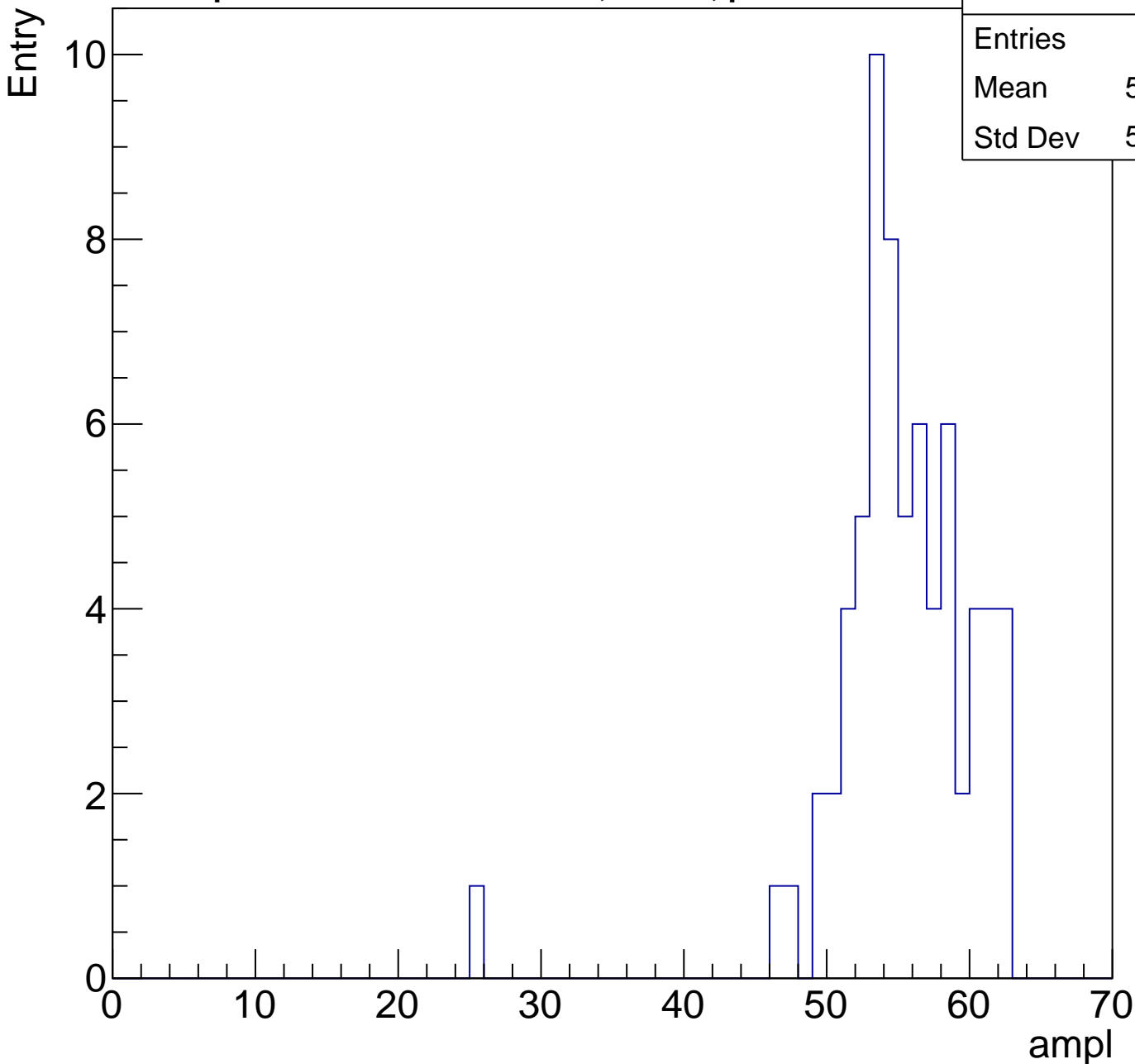
Entries	65
Mean	47.58
Std Dev	4.567



# B1L102S, U3-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

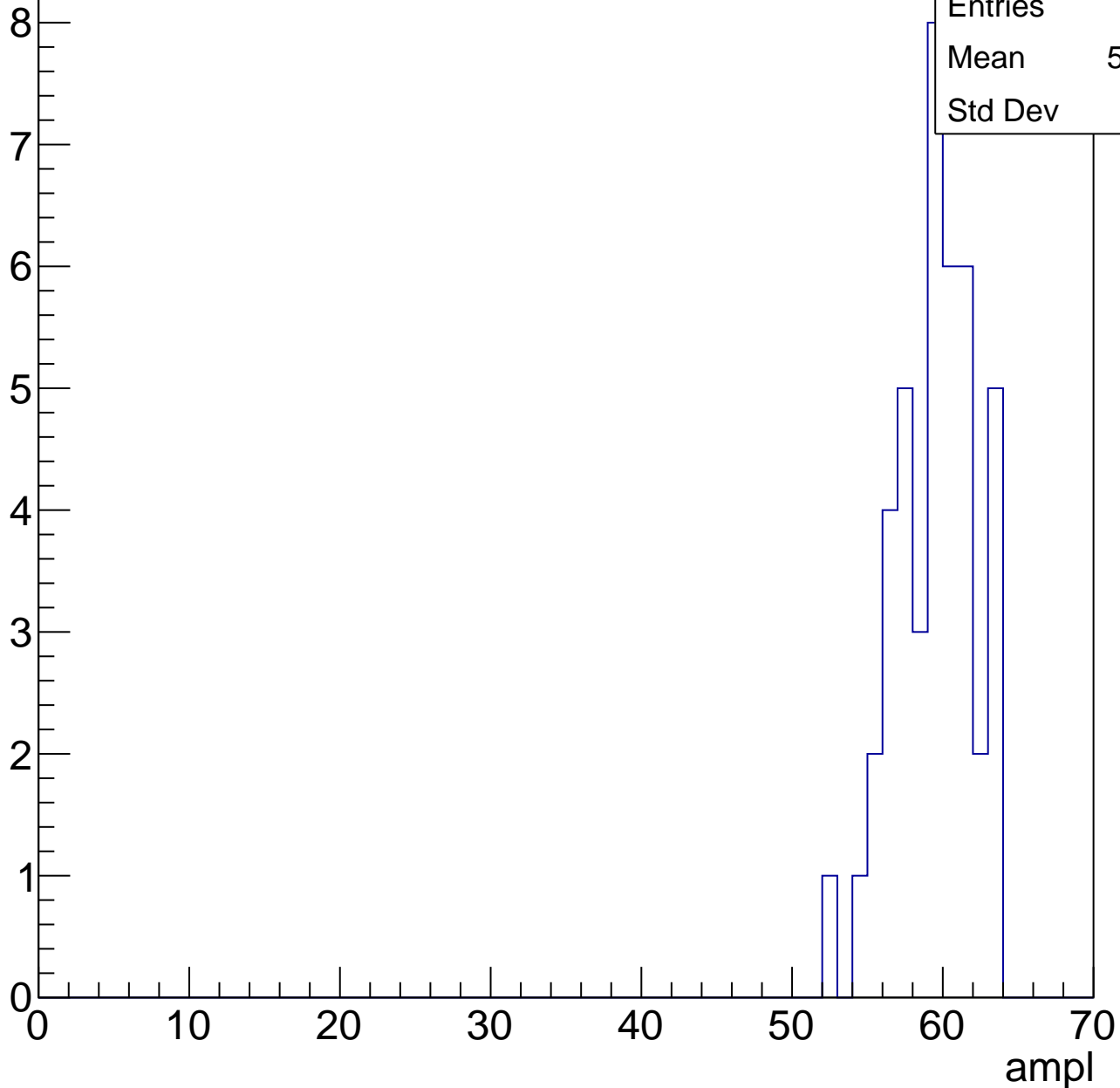
Entries	69
Mean	54.77
Std Dev	5.204



# B1L102S, U3-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

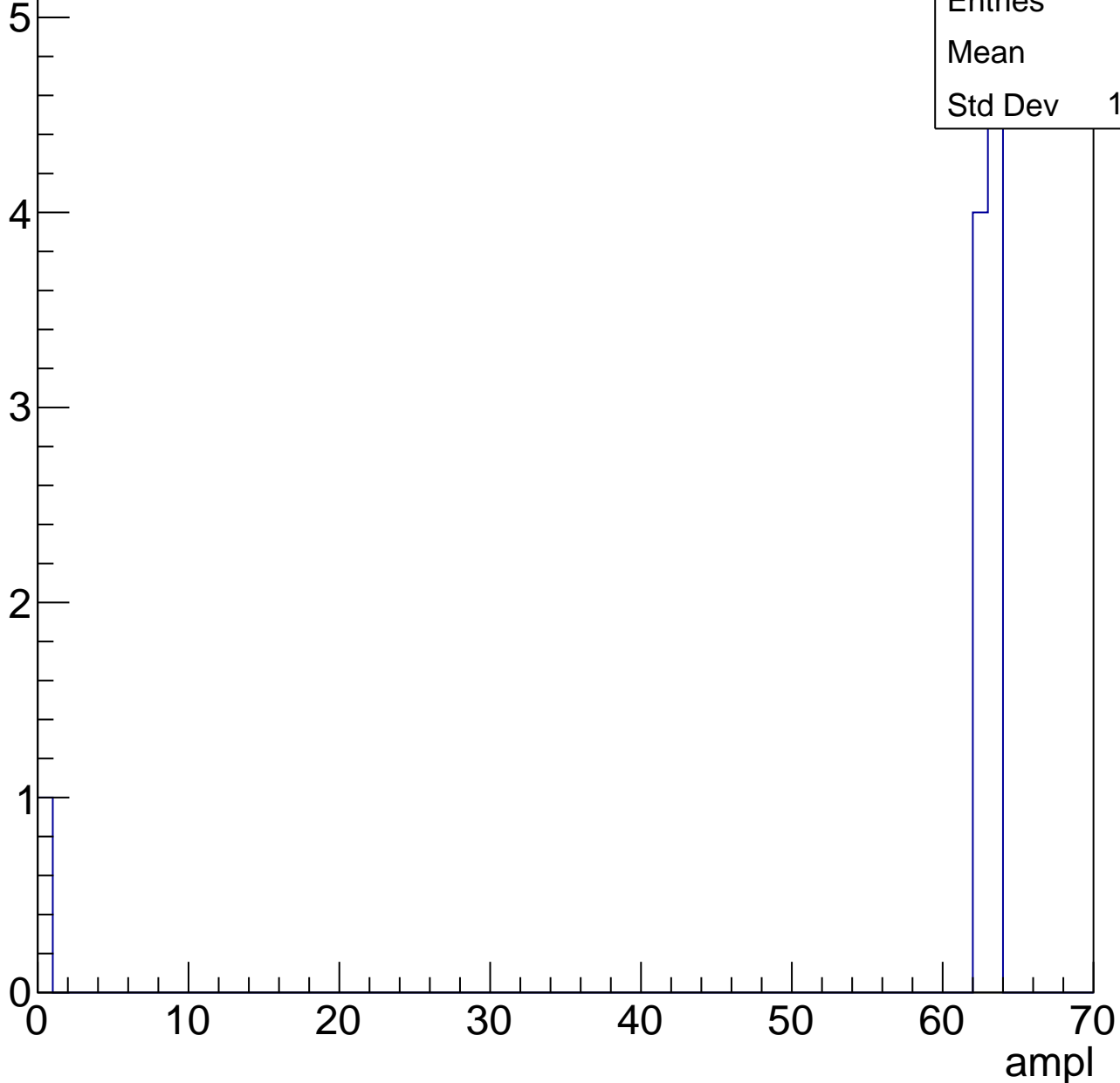


# B1L102S, U3-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	10
Mean	56.3
Std Dev	18.77

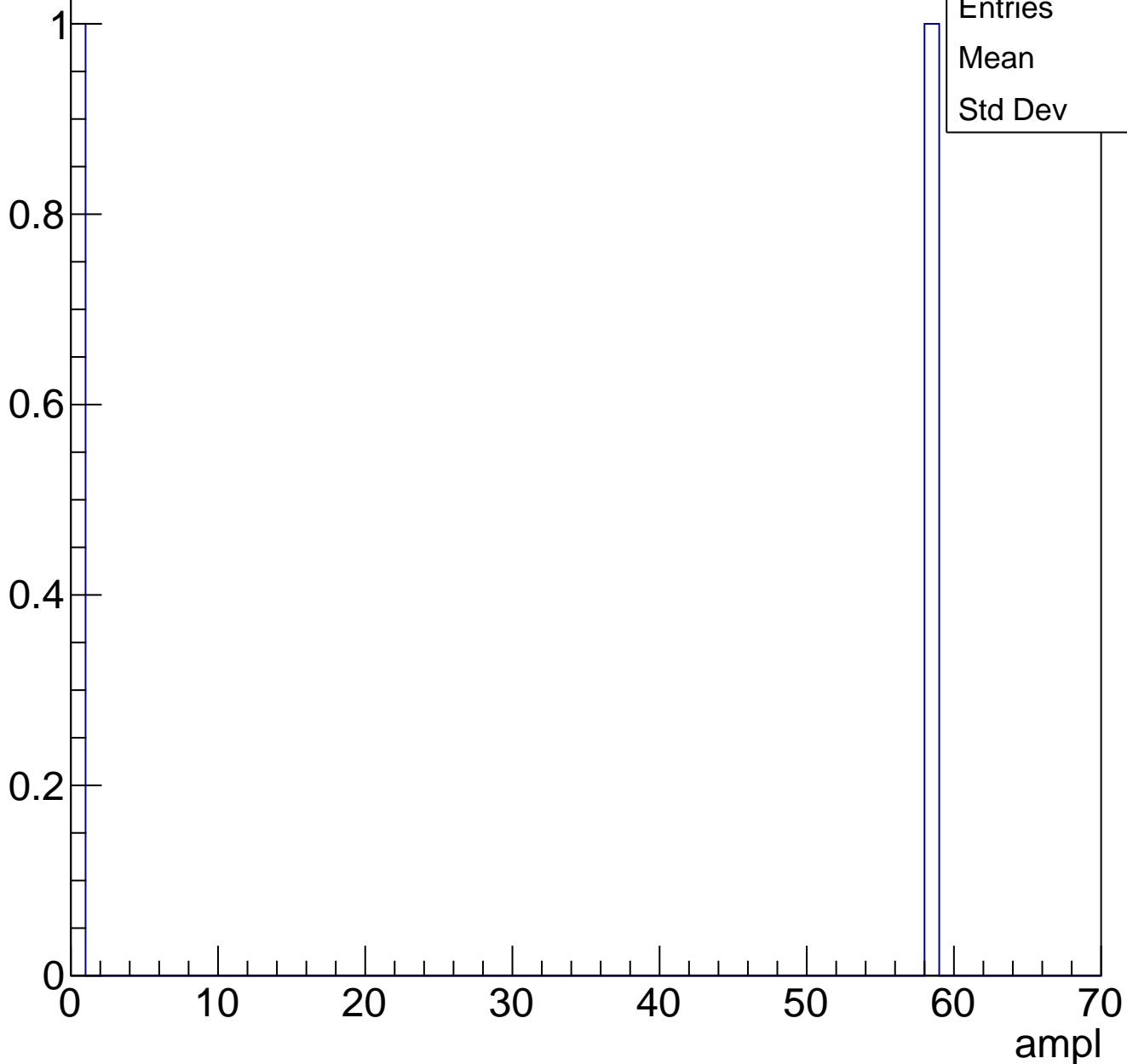




# B1L102S, U3-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch41, adc0

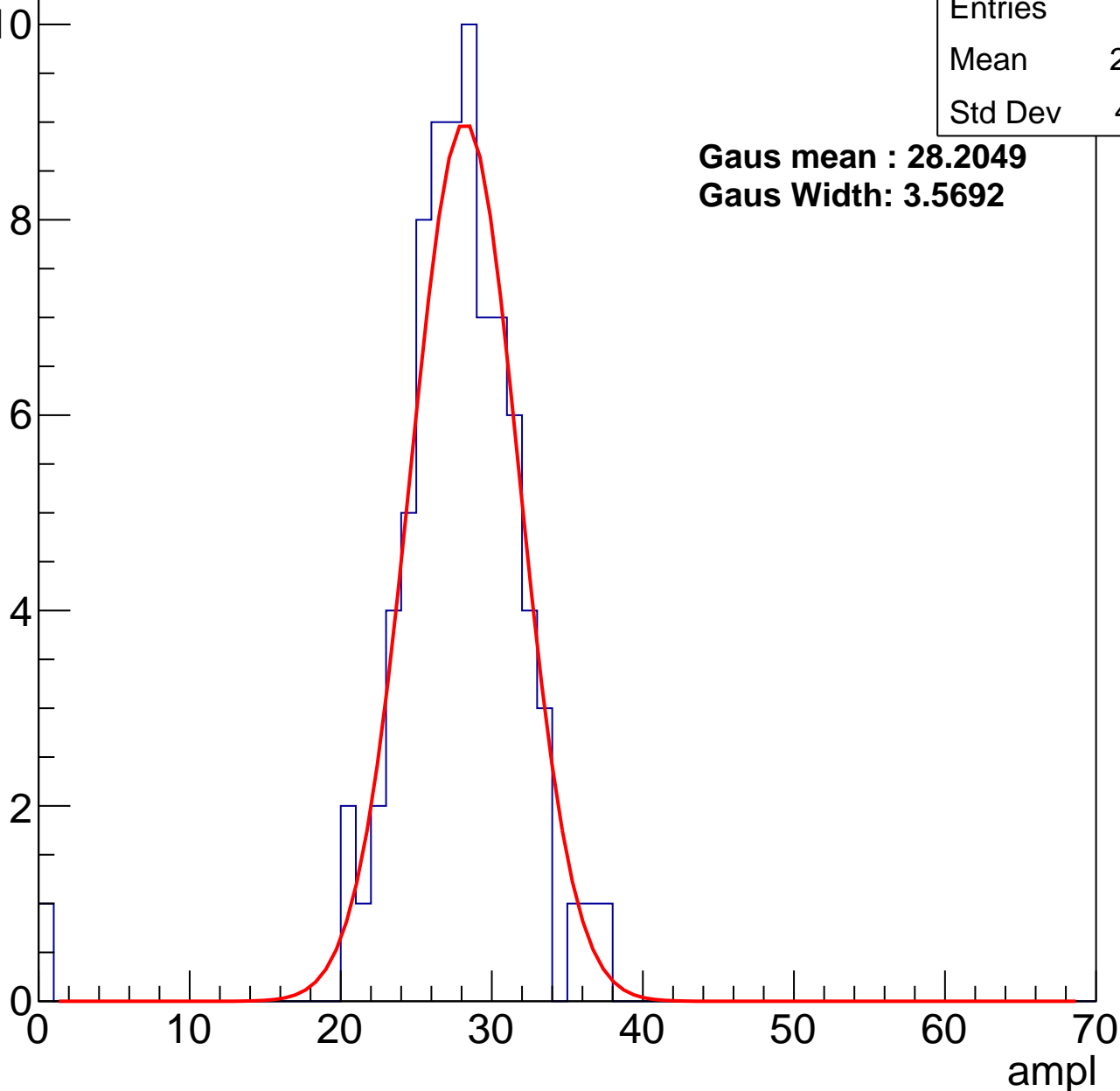
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	81
Mean	27.26
Std Dev	4.591

**Gaus mean : 28.2049**

**Gaus Width: 3.5692**



# B1L102S, U3-ch41, adc1

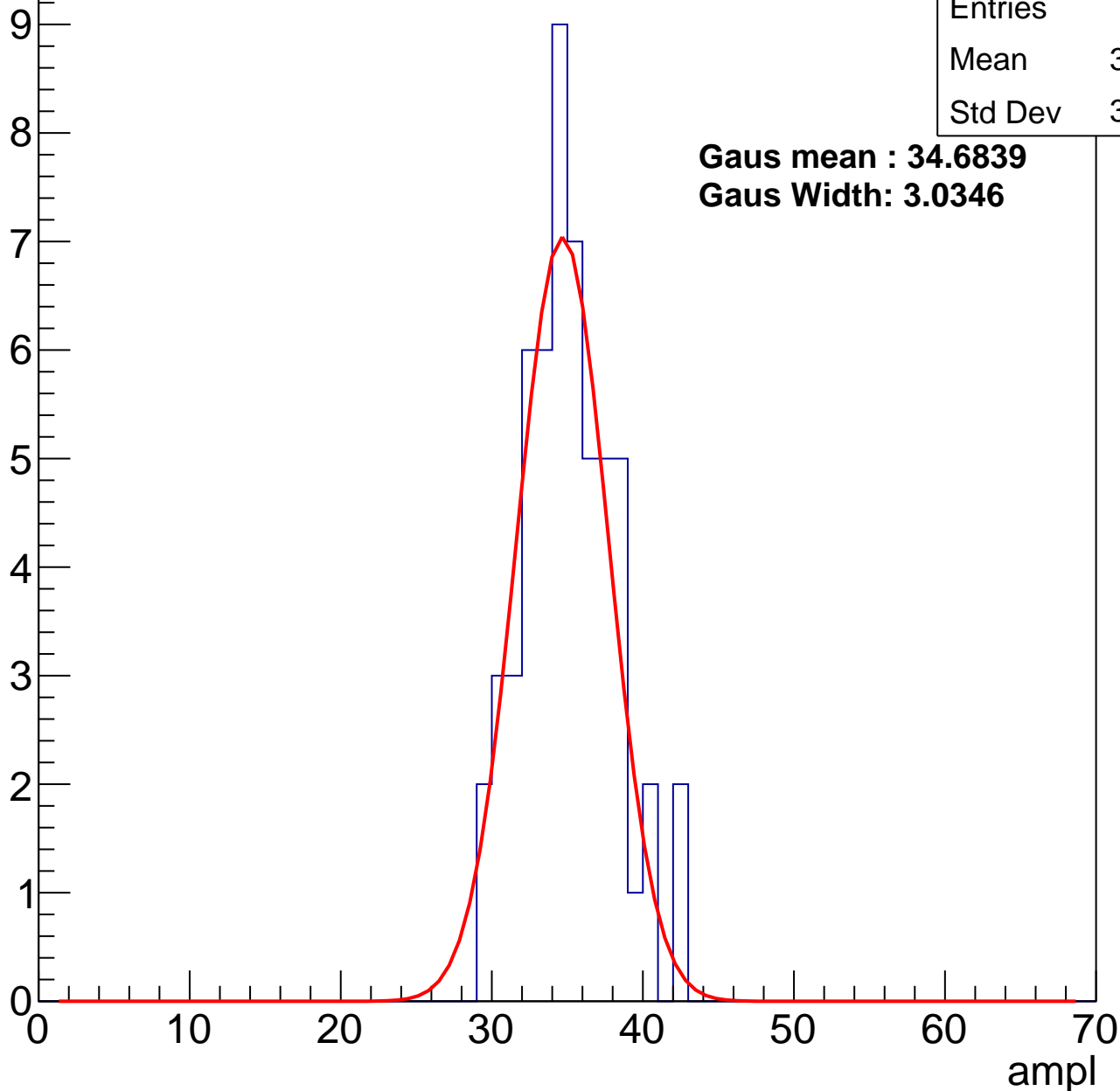
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	34.64
Std Dev	3.014

**Gaus mean : 34.6839**

**Gaus Width: 3.0346**



# B1L102S, U3-ch41, adc2

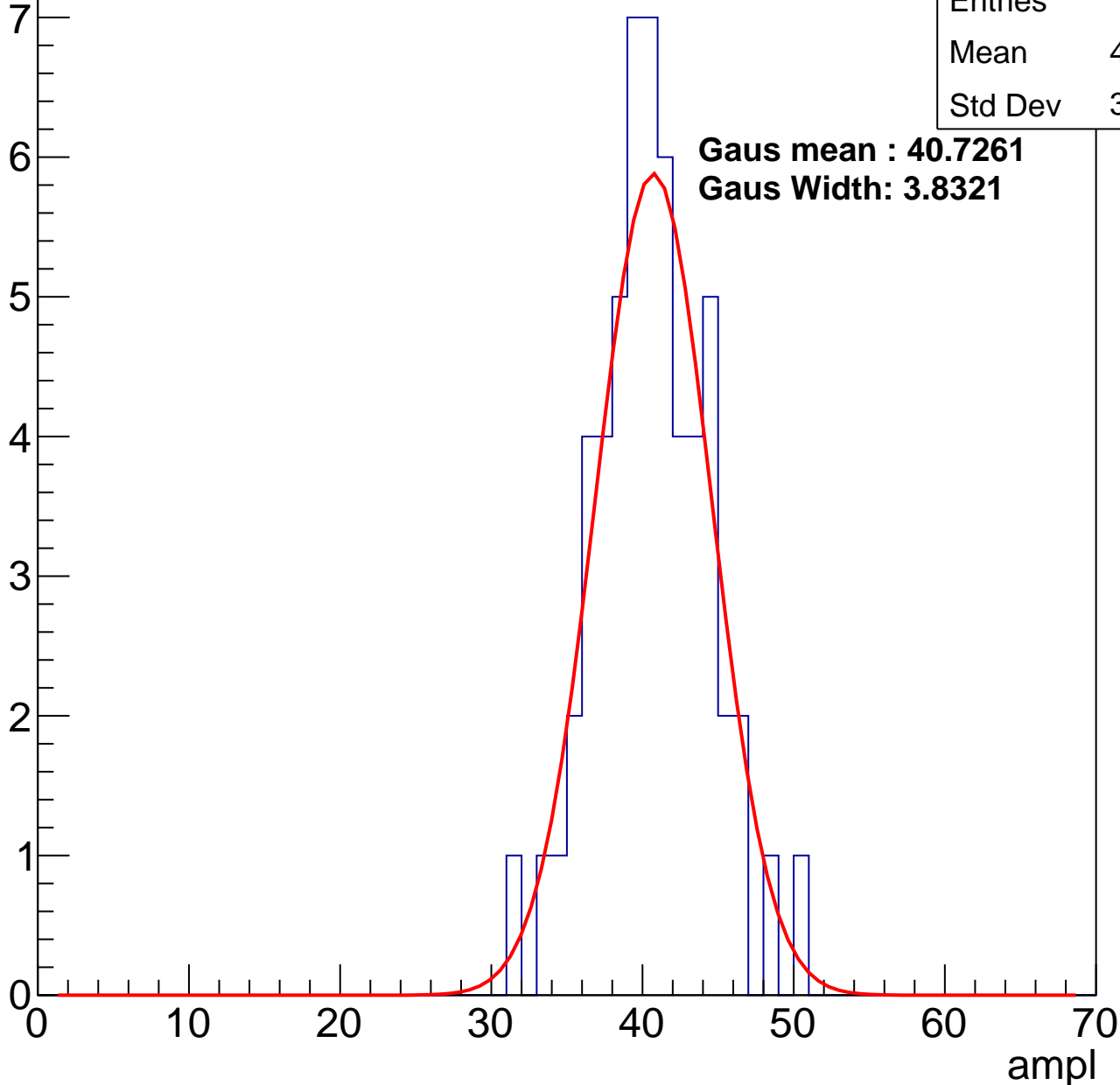
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	40.16
Std Dev	3.665

**Gaus mean : 40.7261**

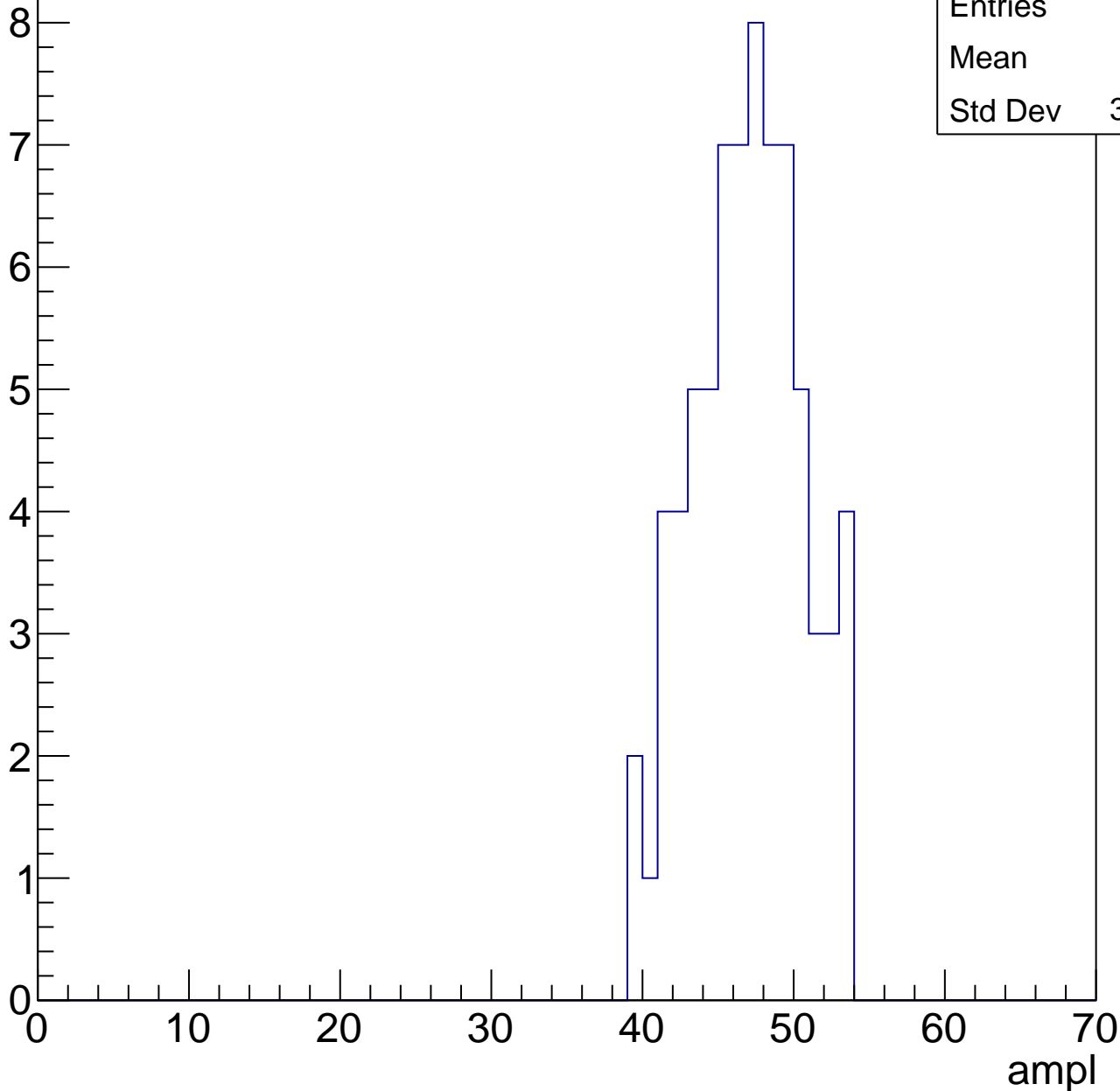
**Gaus Width: 3.8321**



# B1L102S, U3-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



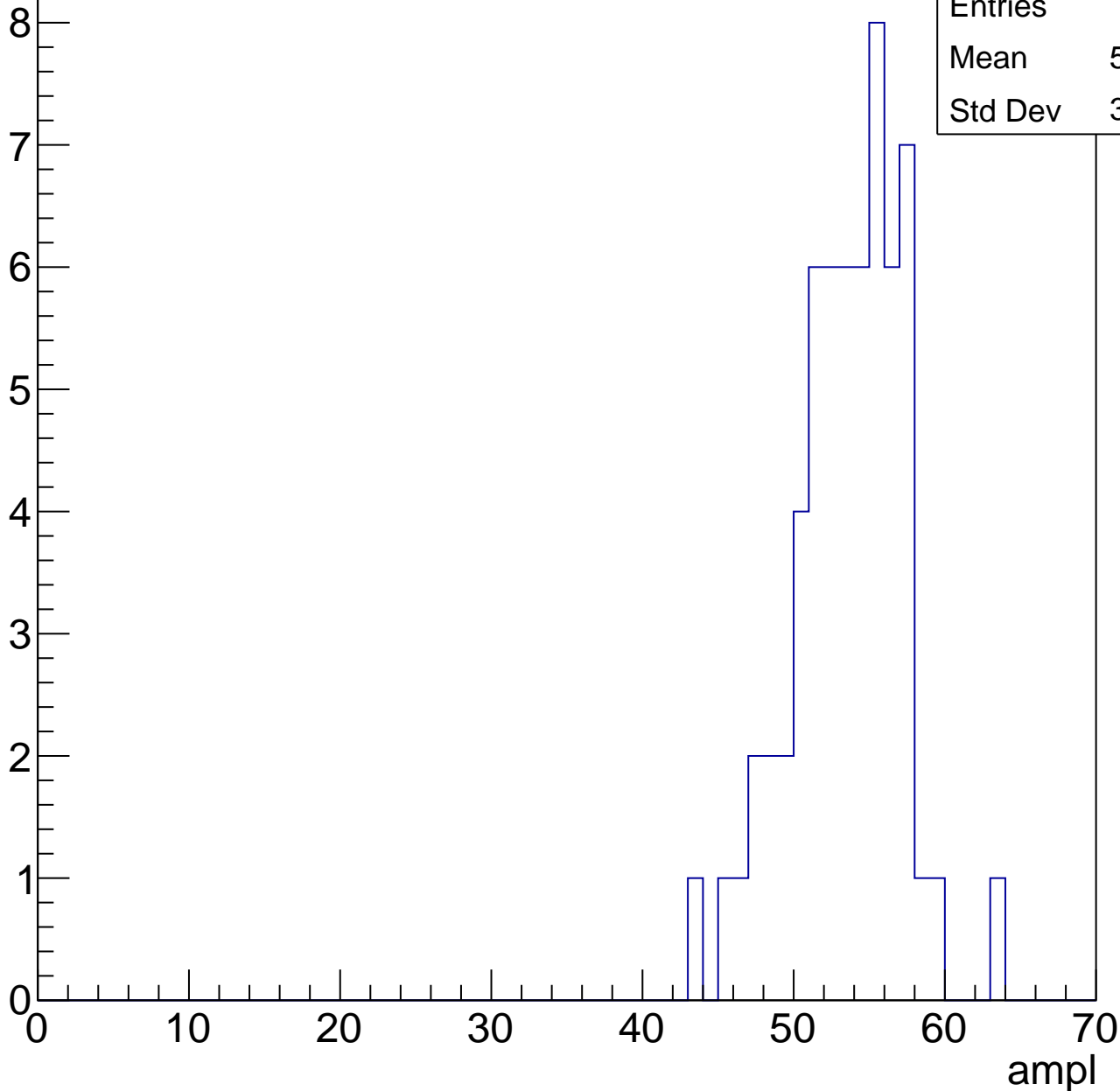
Entries	72
Mean	46.5
Std Dev	3.555

# B1L102S, U3-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	53.07
Std Dev	3.616

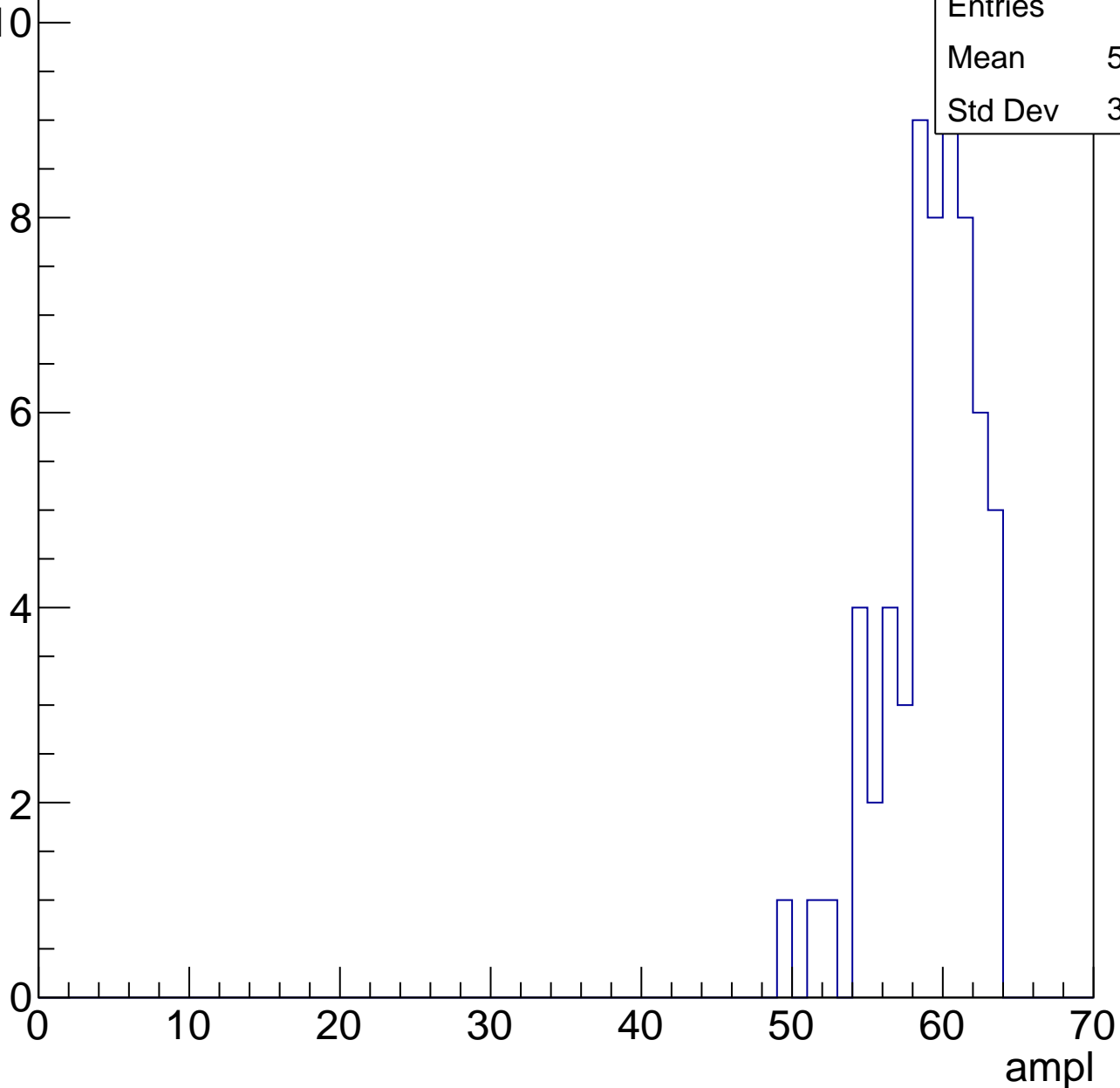


# B1L102S, U3-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

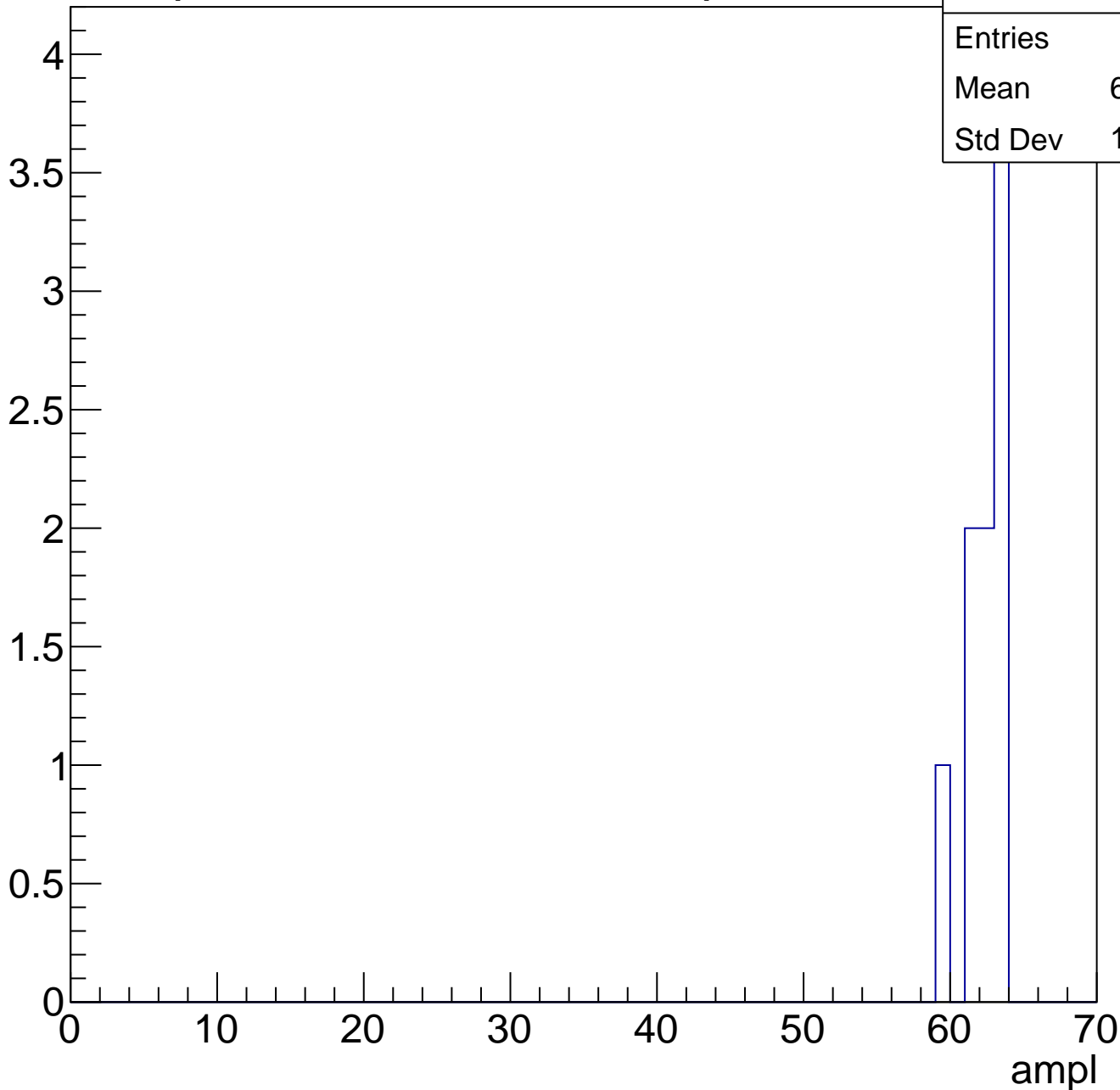
Entries	62
Mean	58.74
Std Dev	3.042



# B1L102S, U3-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

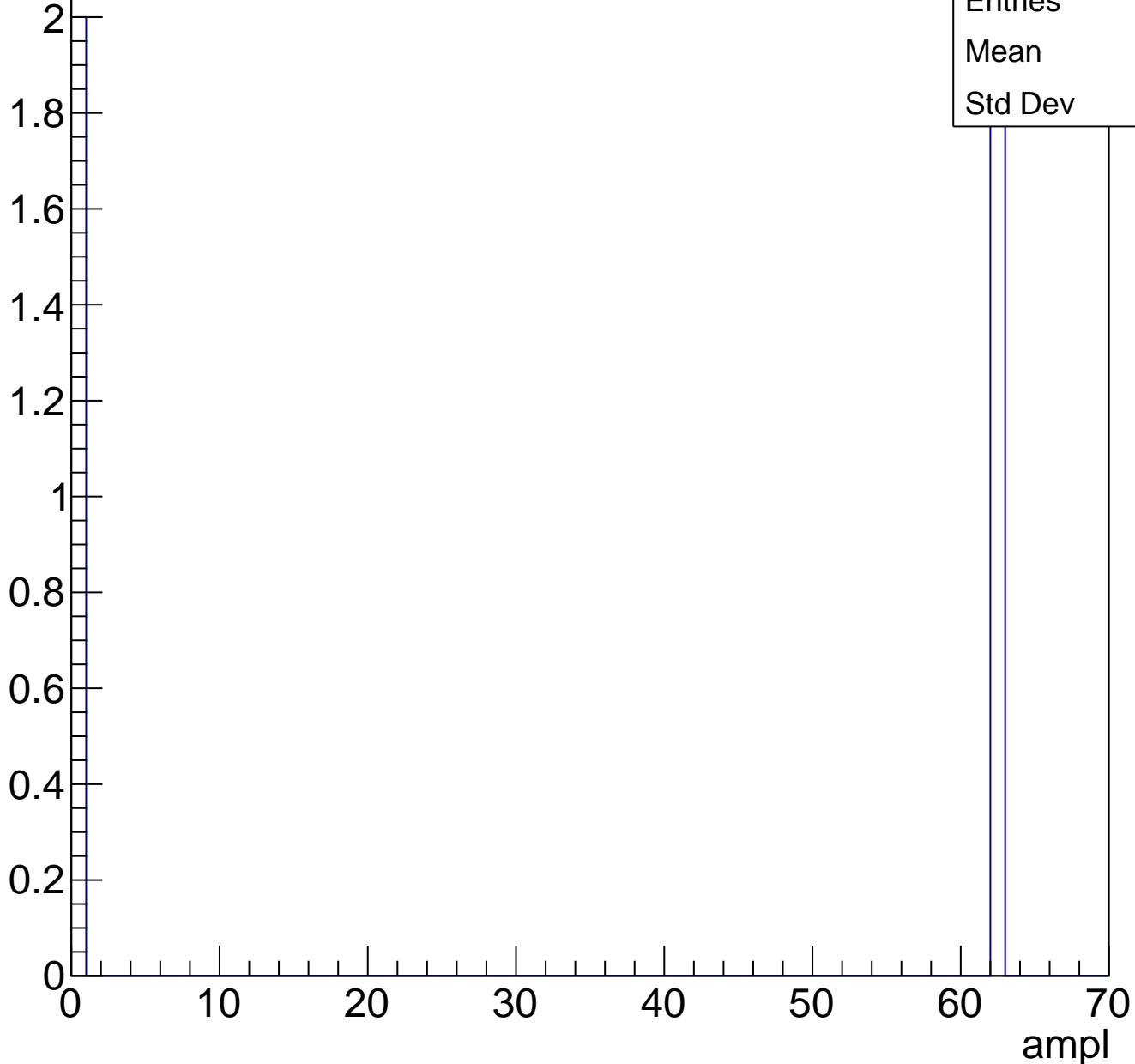




# B1L102S, U3-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch42, adc0

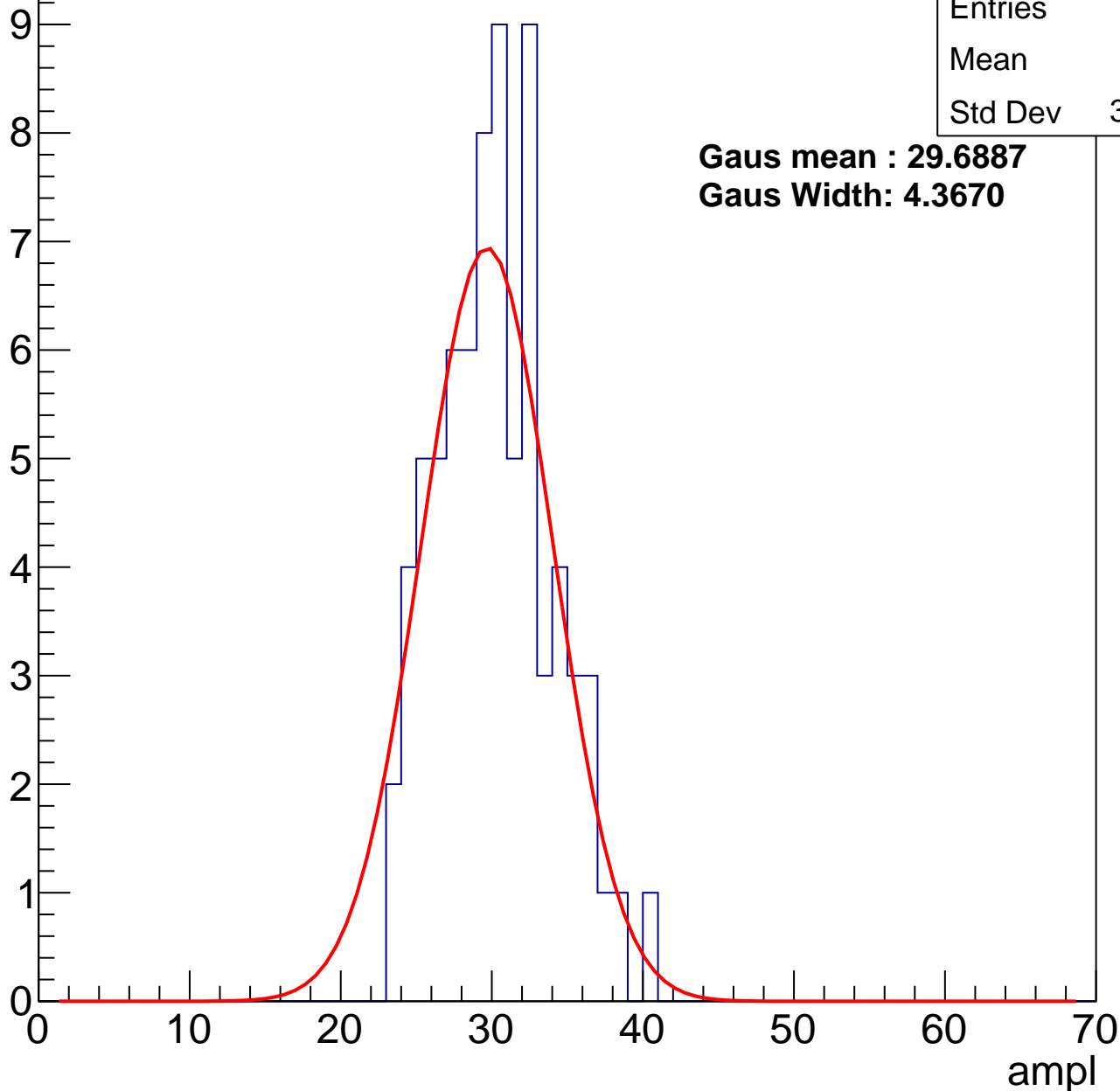
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	29.8
Std Dev	3.756

**Gaus mean : 29.6887**

**Gaus Width: 4.3670**



# B1L102S, U3-ch42, adc1

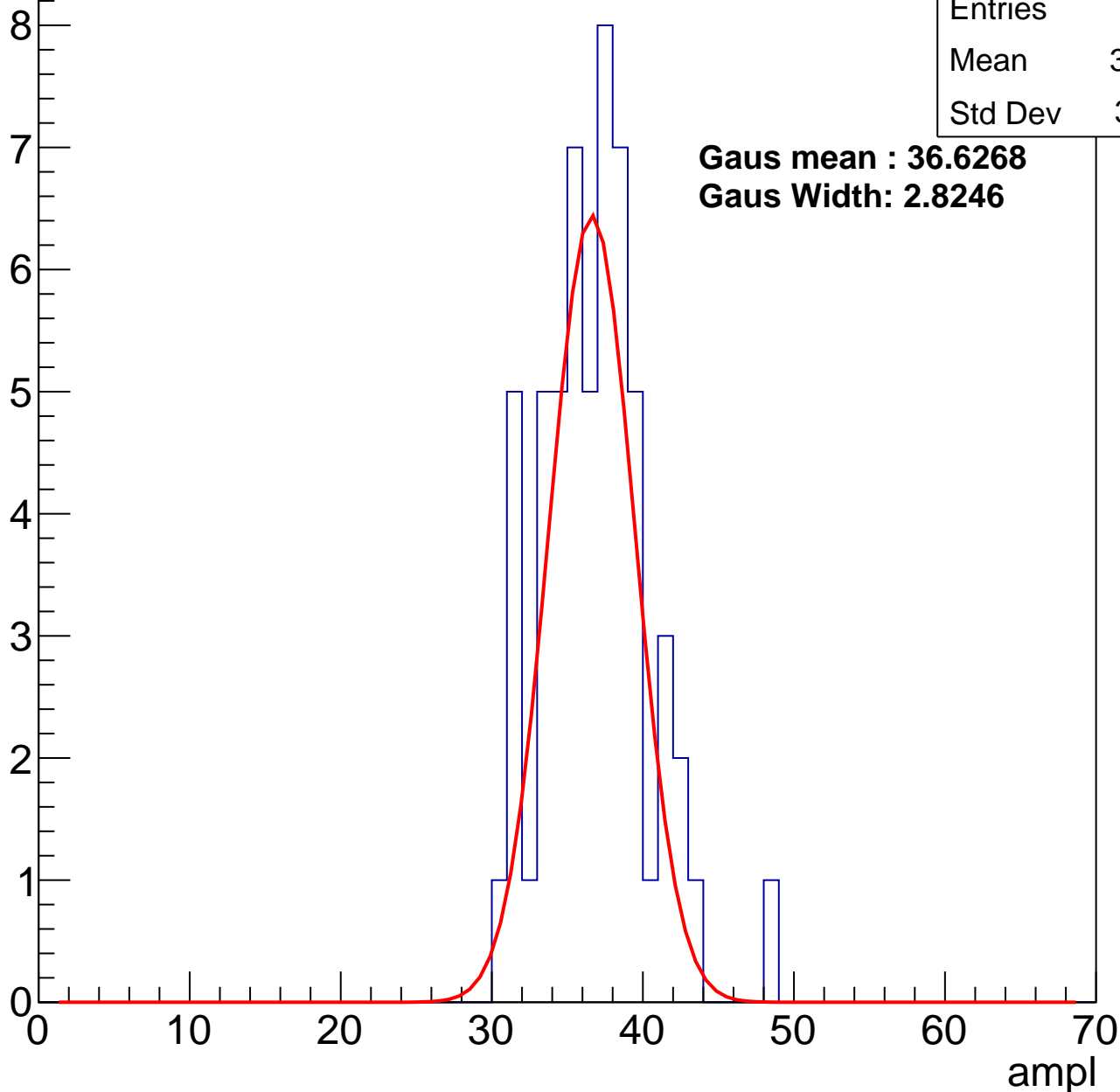
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	36.35
Std Dev	3.451

**Gaus mean : 36.6268**

**Gaus Width: 2.8246**



# B1L102S, U3-ch42, adc2

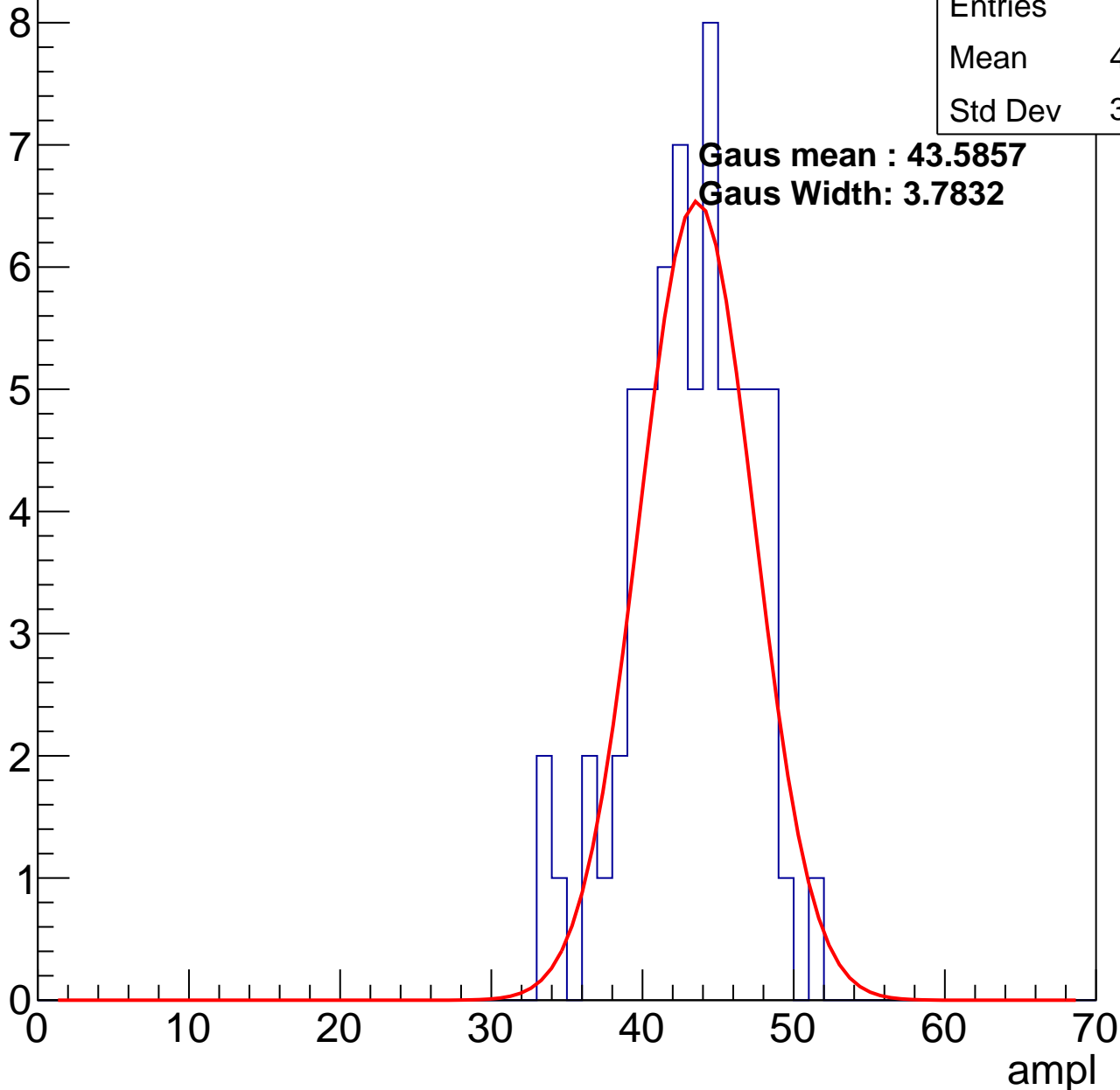
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	42.68
Std Dev	3.878

**Gaus mean : 43.5857**

**Gaus Width: 3.7832**

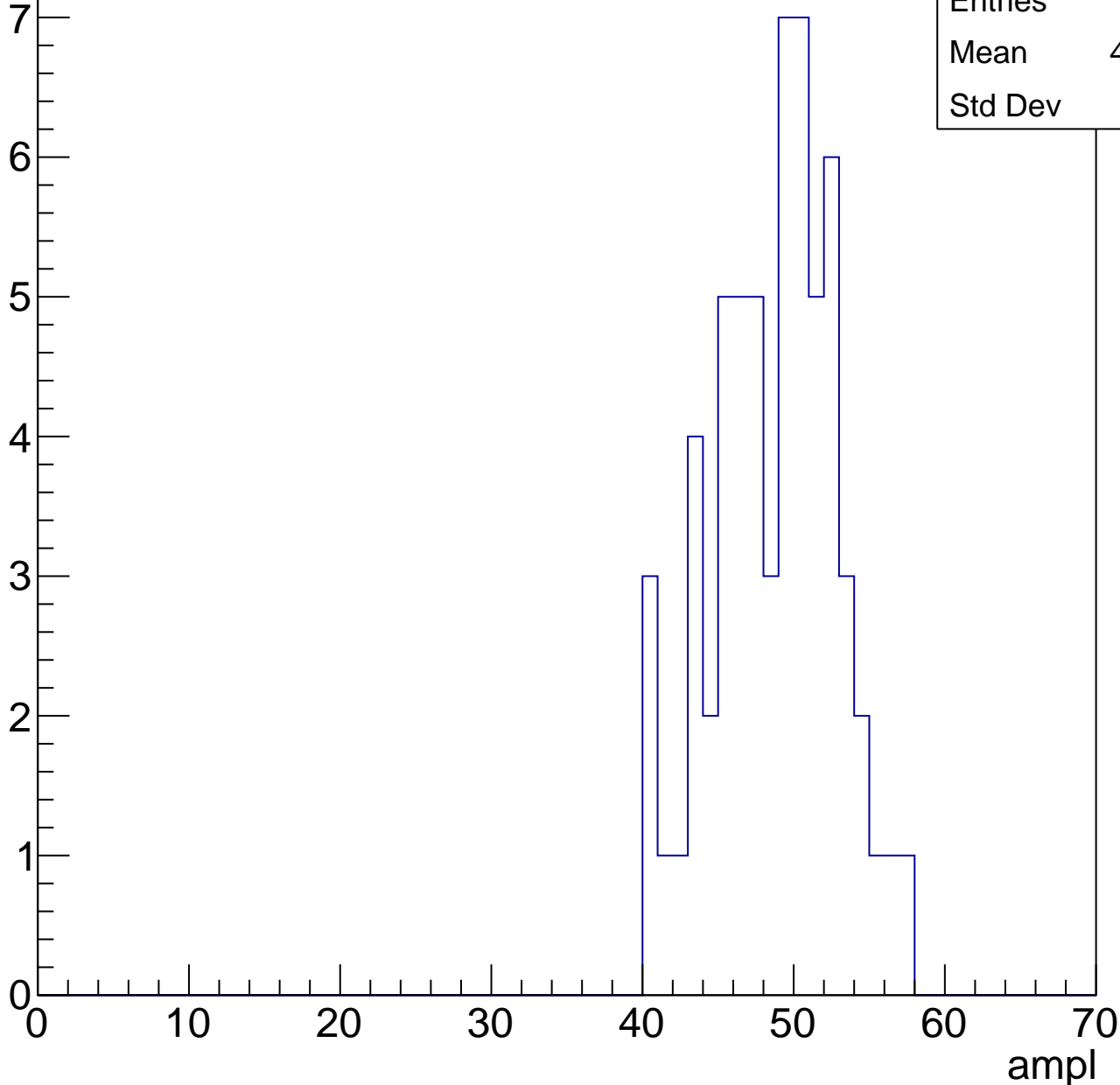


# B1L102S, U3-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	48.26
Std Dev	4

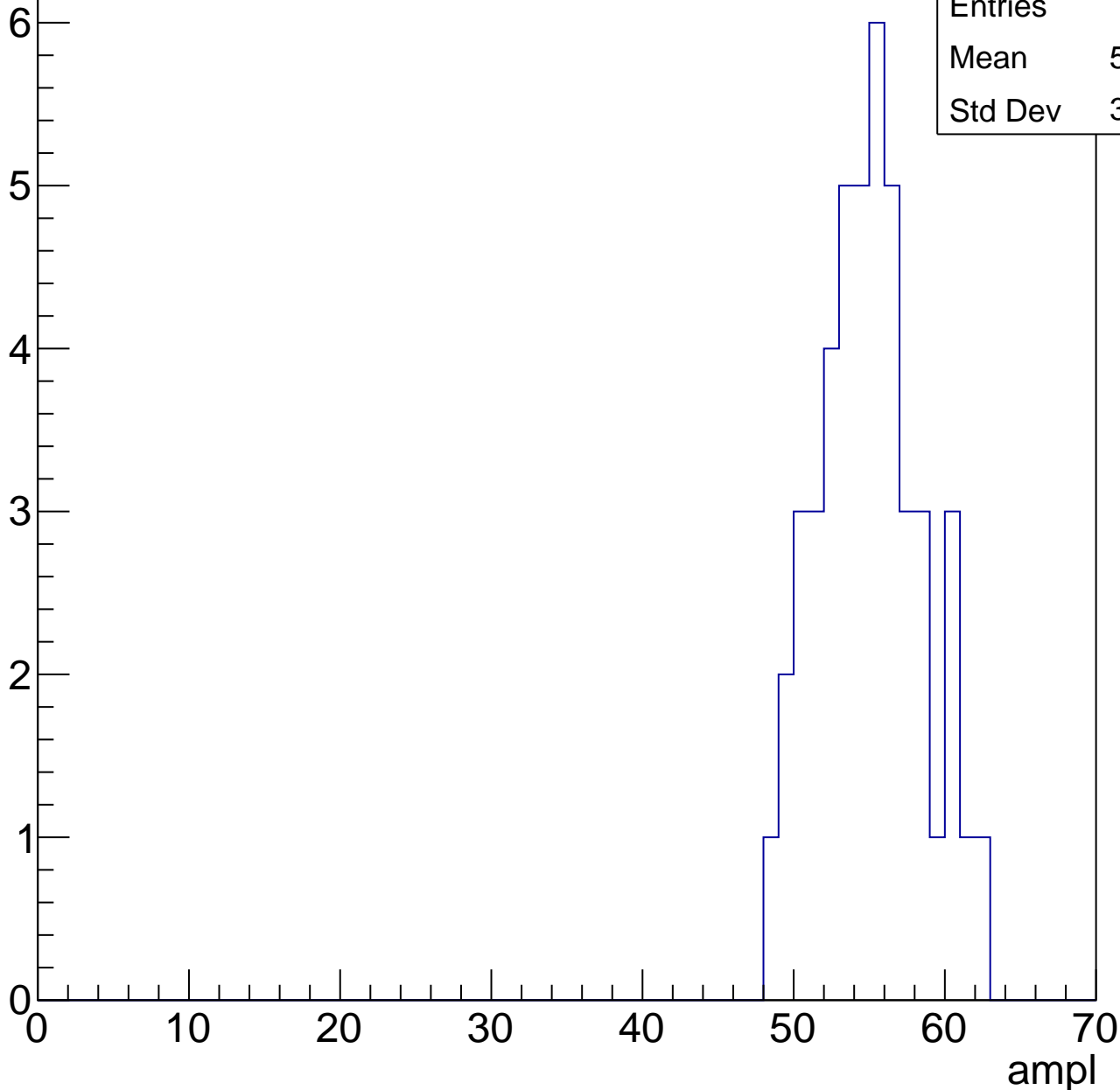


# B1L102S, U3-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	54.54
Std Dev	3.347



# B1L102S, U3-ch42, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

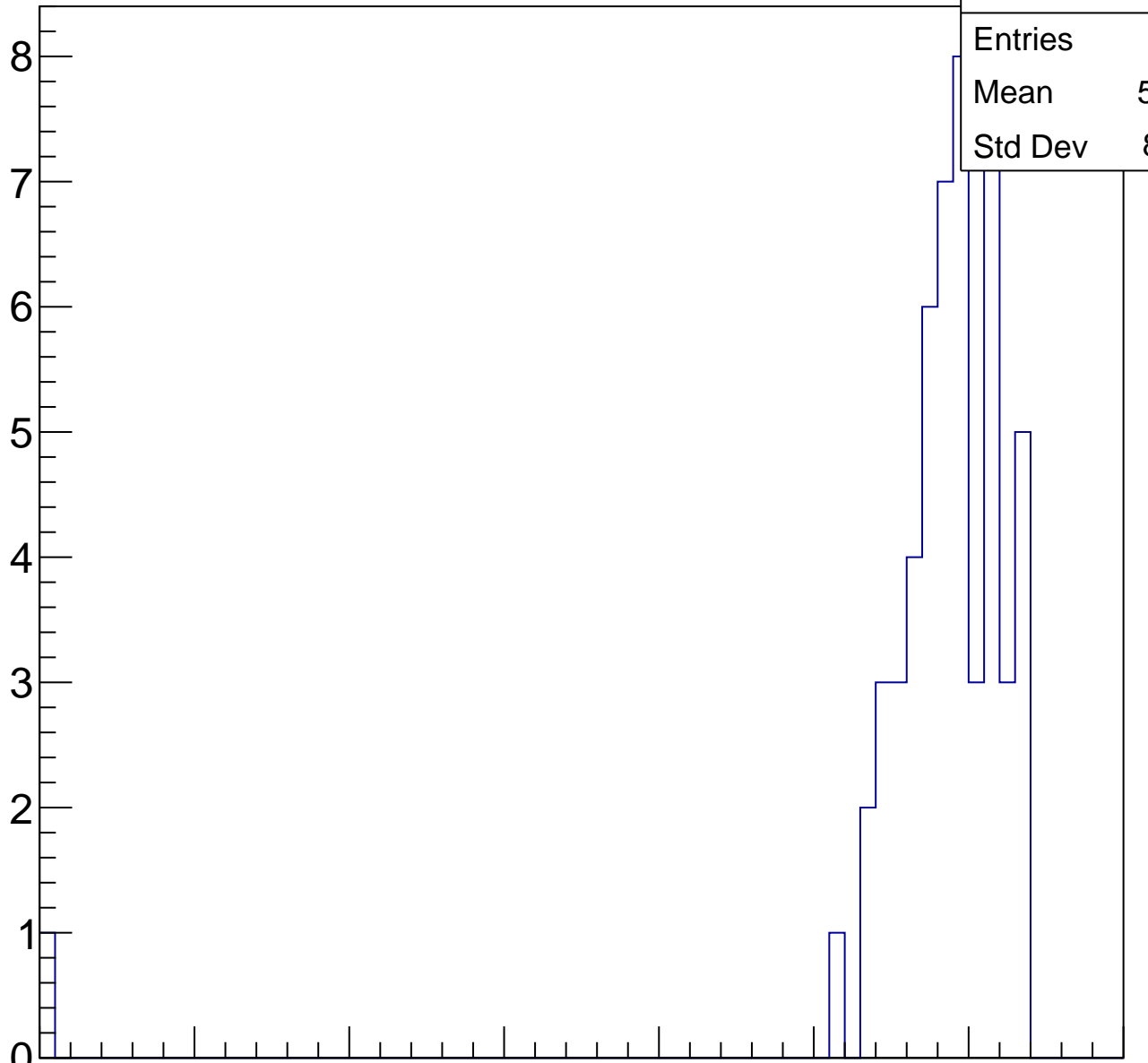
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	54
Mean	57.35
Std Dev	8.391

ampl

0 10 20 30 40 50 60 70

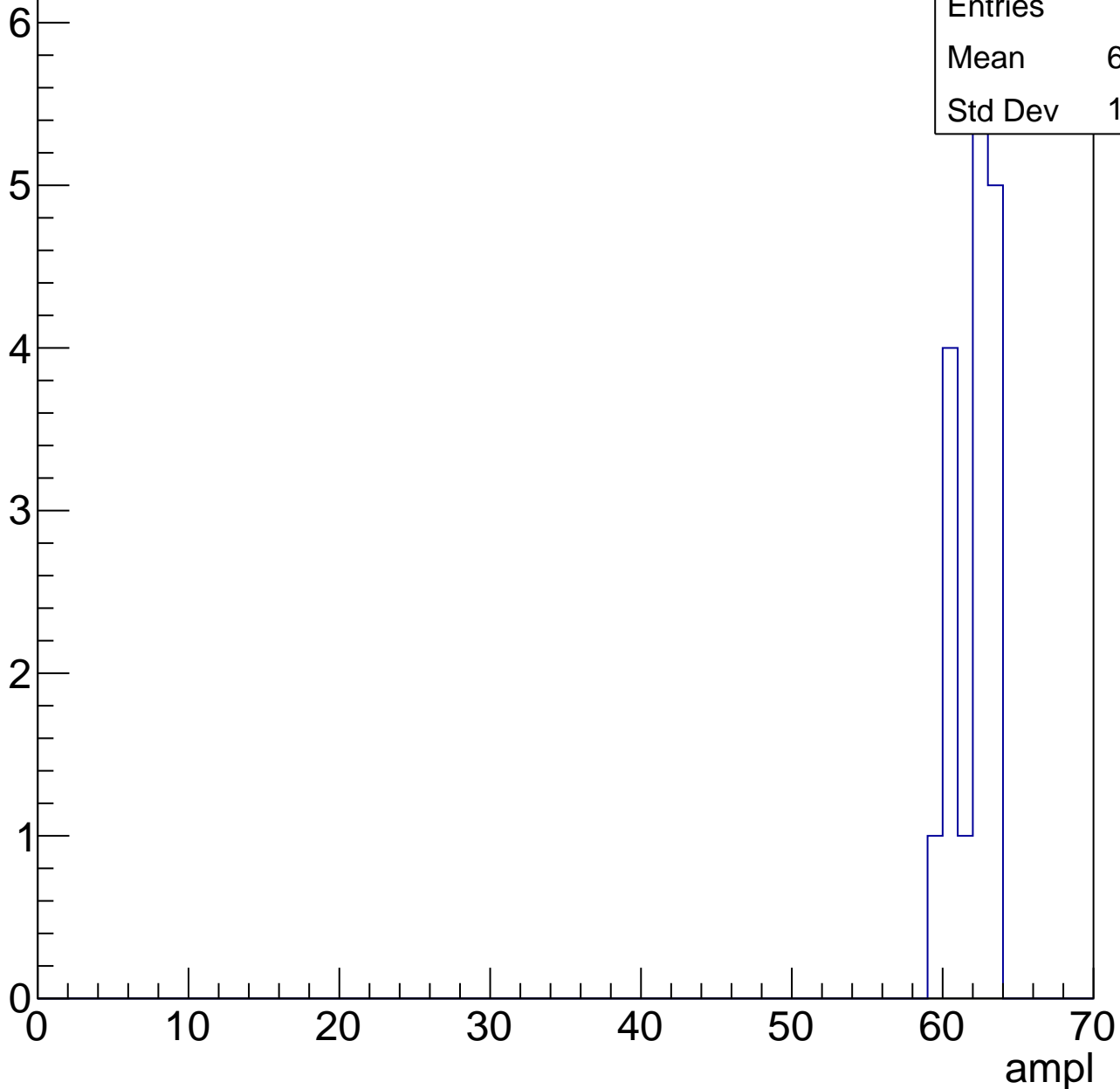


# B1L102S, U3-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	17
Mean	61.59
Std Dev	1.286





# B1L102S, U3-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch43, adc0

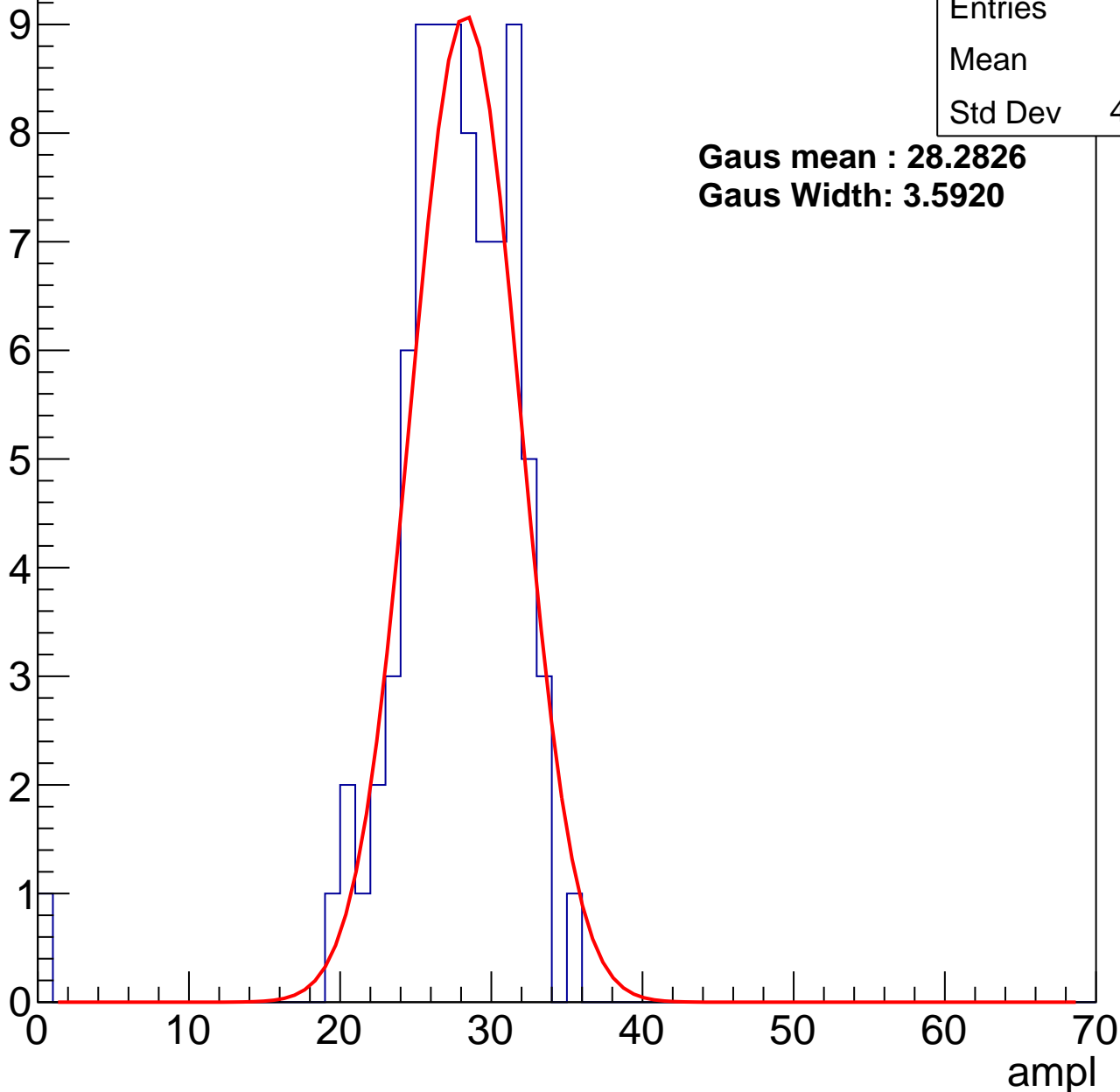
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	83
Mean	27.1
Std Dev	4.476

**Gaus mean : 28.2826**

**Gaus Width: 3.5920**



# B1L102S, U3-ch43, adc1

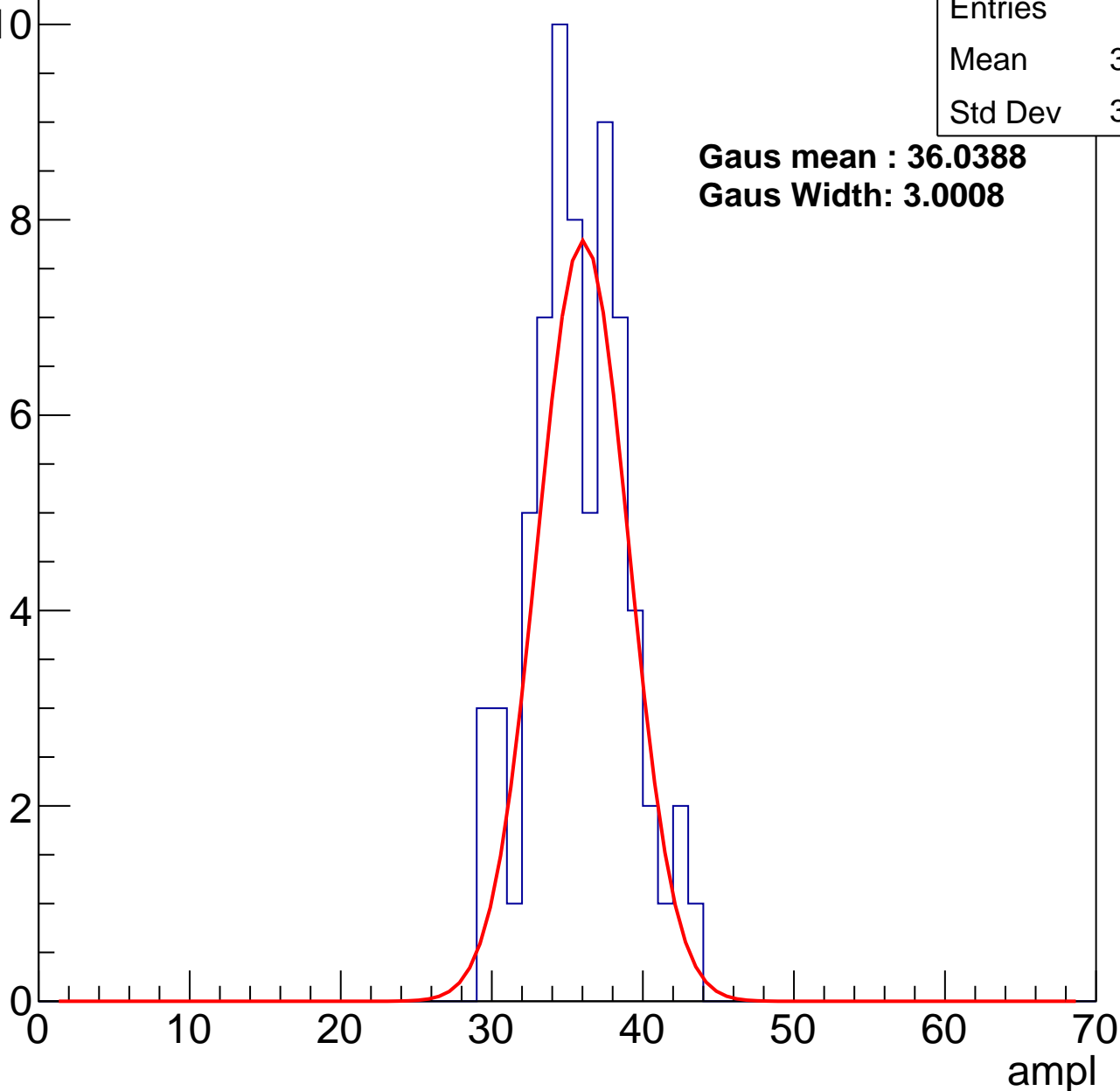
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	35.32
Std Dev	3.187

**Gaus mean : 36.0388**

**Gaus Width: 3.0008**



# B1L102S, U3-ch43, adc2

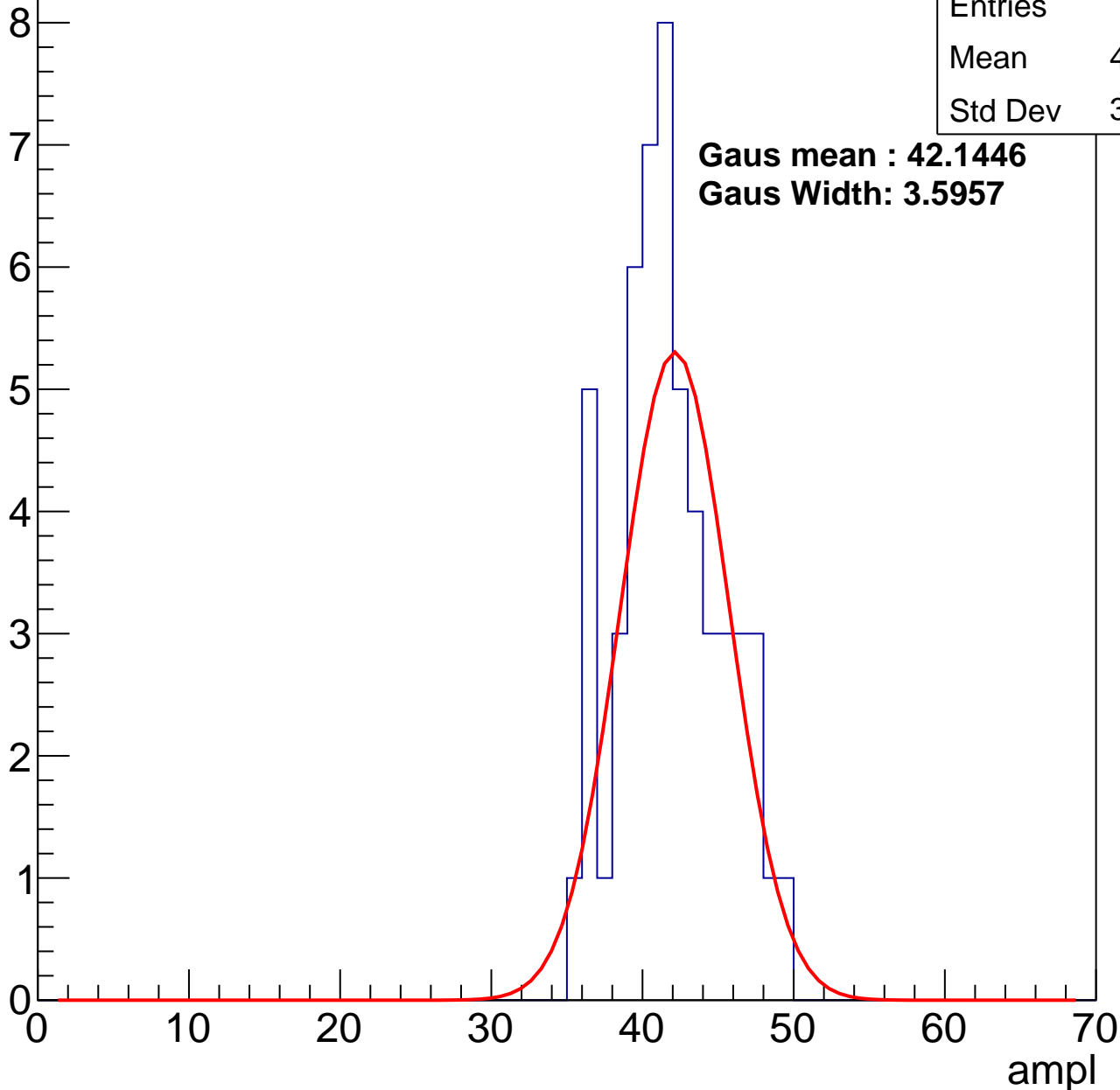
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	41.35
Std Dev	3.389

**Gaus mean : 42.1446**

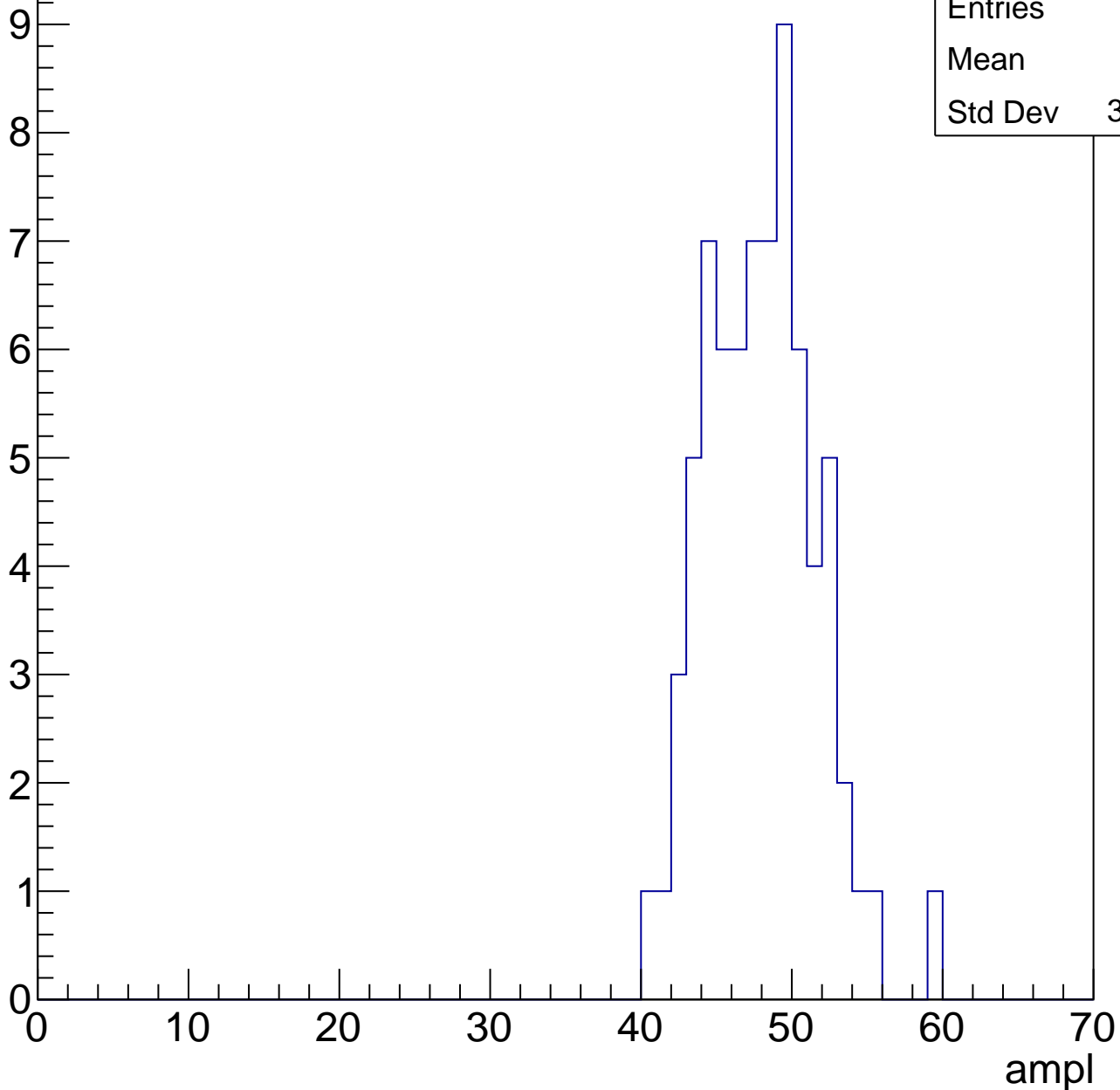
**Gaus Width: 3.5957**



# B1L102S, U3-ch43, adc3

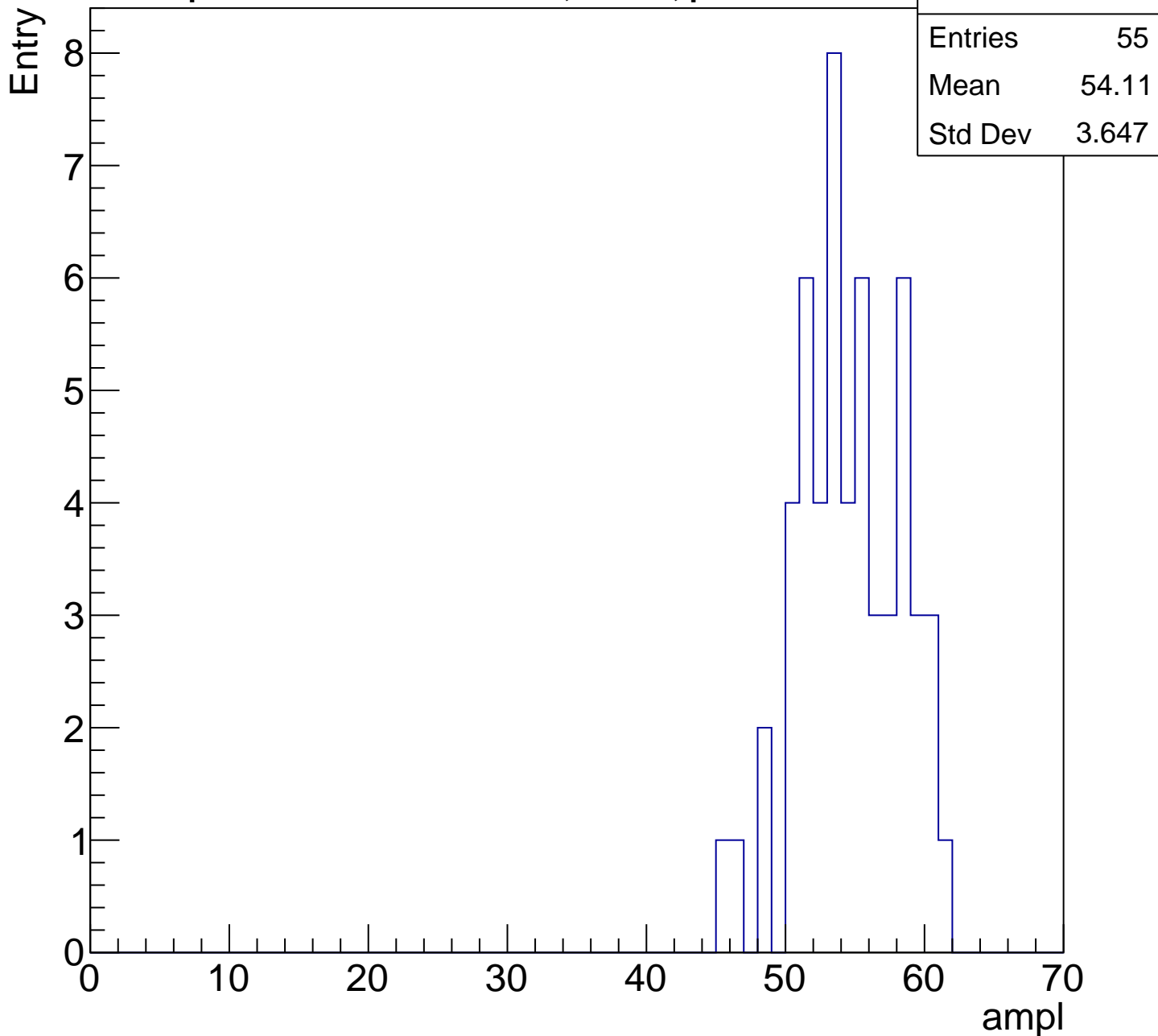
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch43, adc4

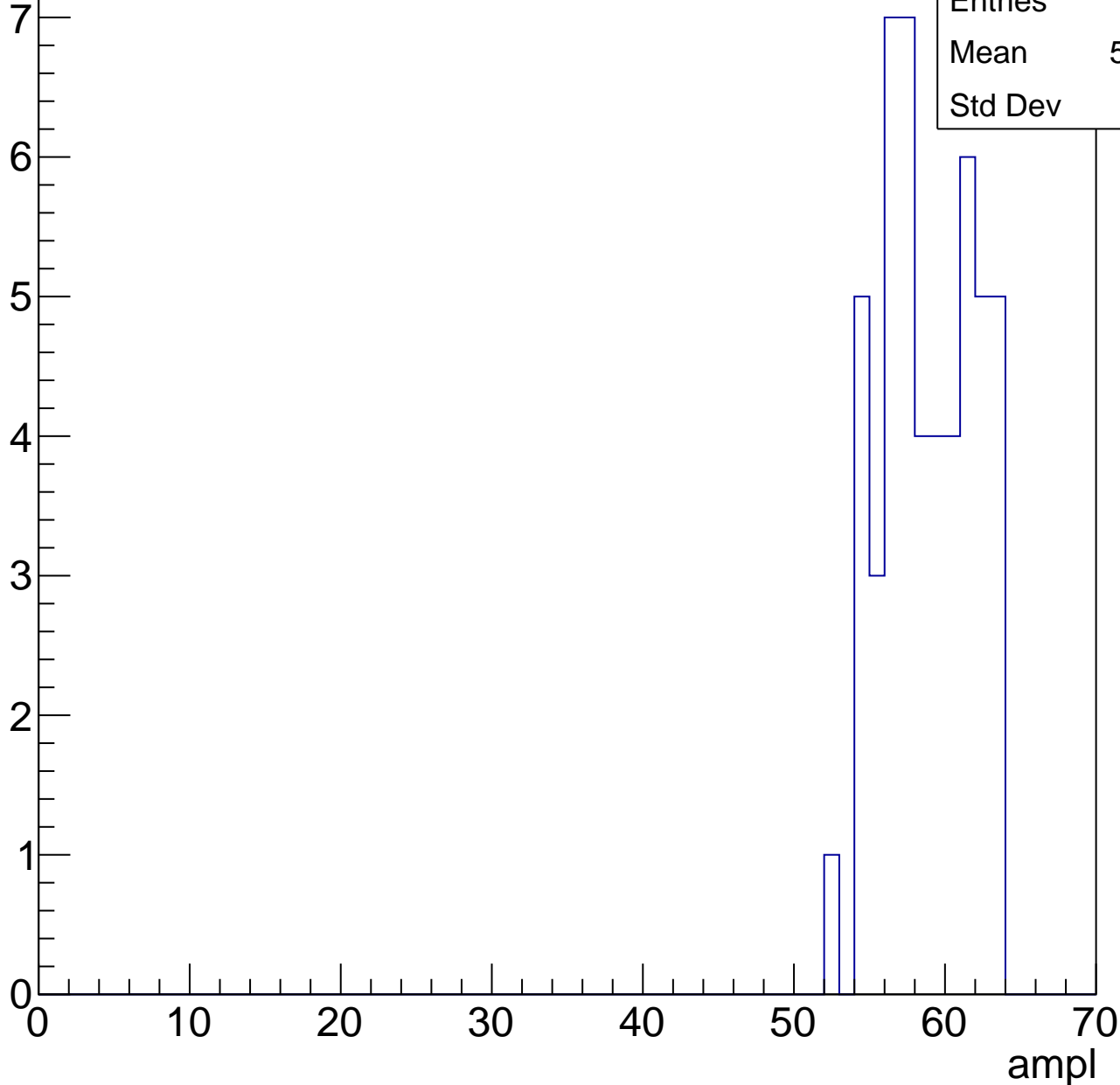
calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U3-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



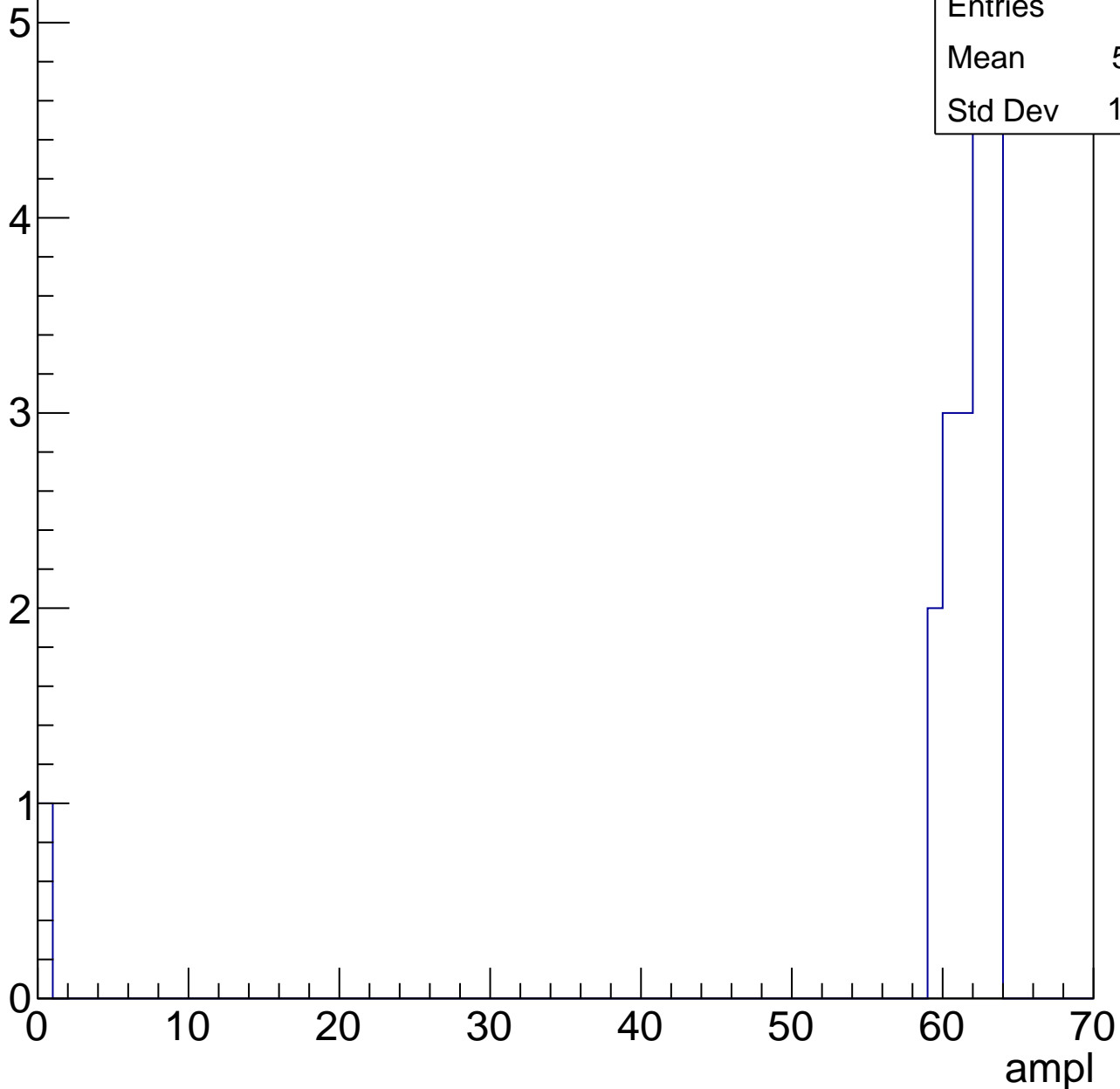
Entries	51
Mean	58.37
Std Dev	2.97

# B1L102S, U3-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	19
Mean	58.21
Std Dev	13.78





# B1L102S, U3-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	18
Std Dev	0

ampl

# B1L102S, U3-ch44, adc0

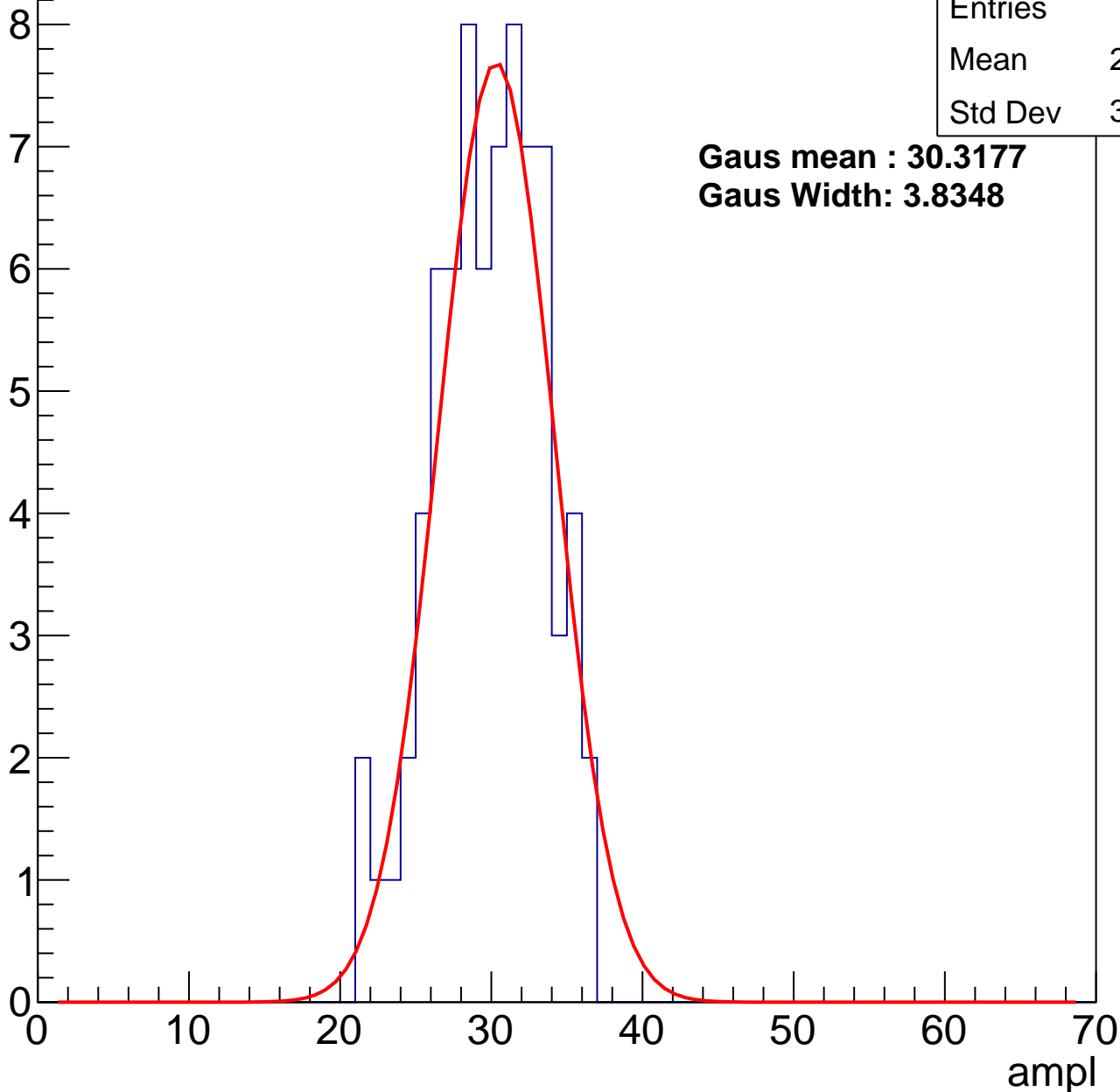
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	29.43
Std Dev	3.545

**Gaus mean : 30.3177**

**Gaus Width: 3.8348**



# B1L102S, U3-ch44, adc1

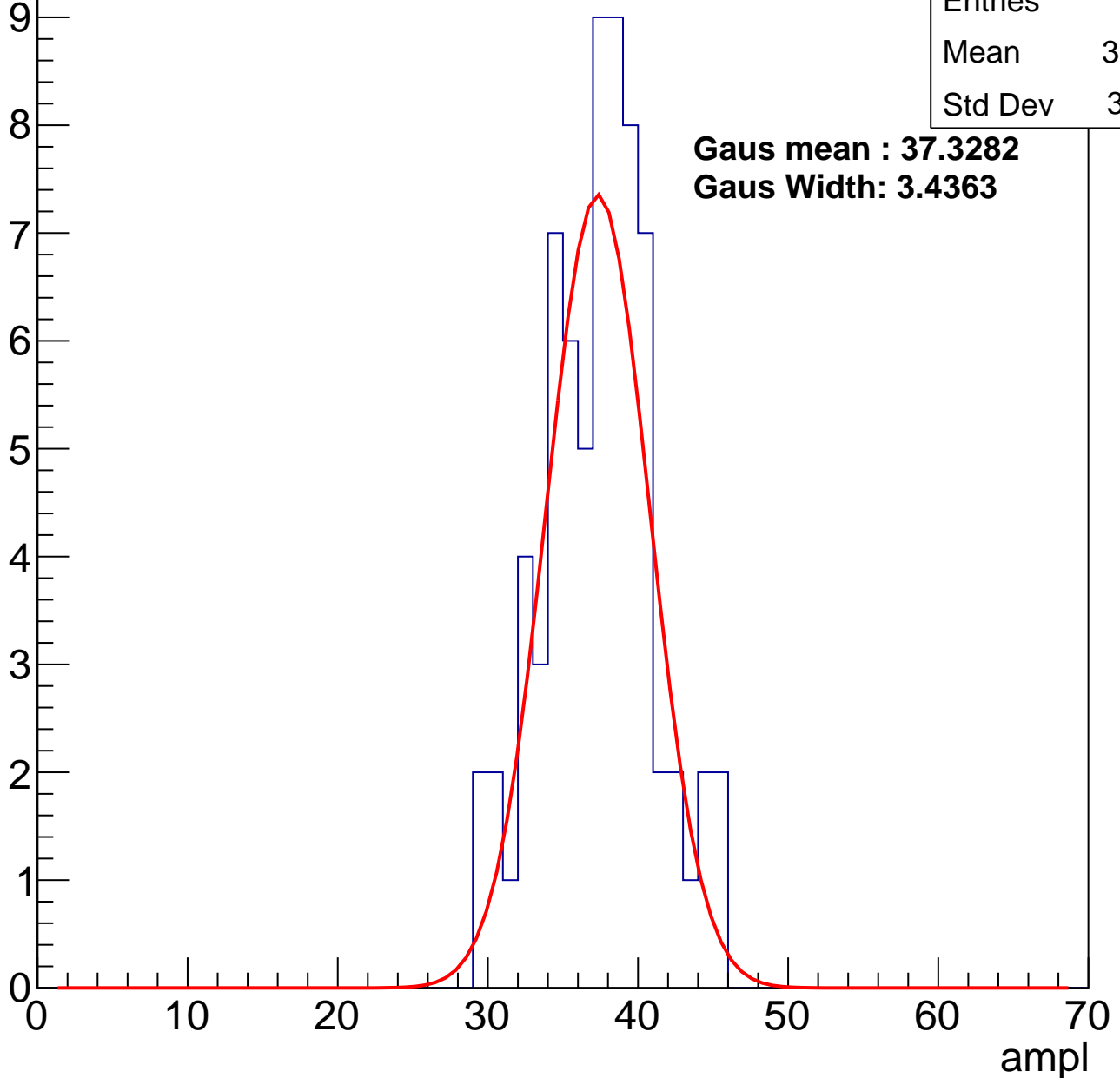
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	36.92
Std Dev	3.631

**Gaus mean : 37.3282**

**Gaus Width: 3.4363**



# B1L102S, U3-ch44, adc2

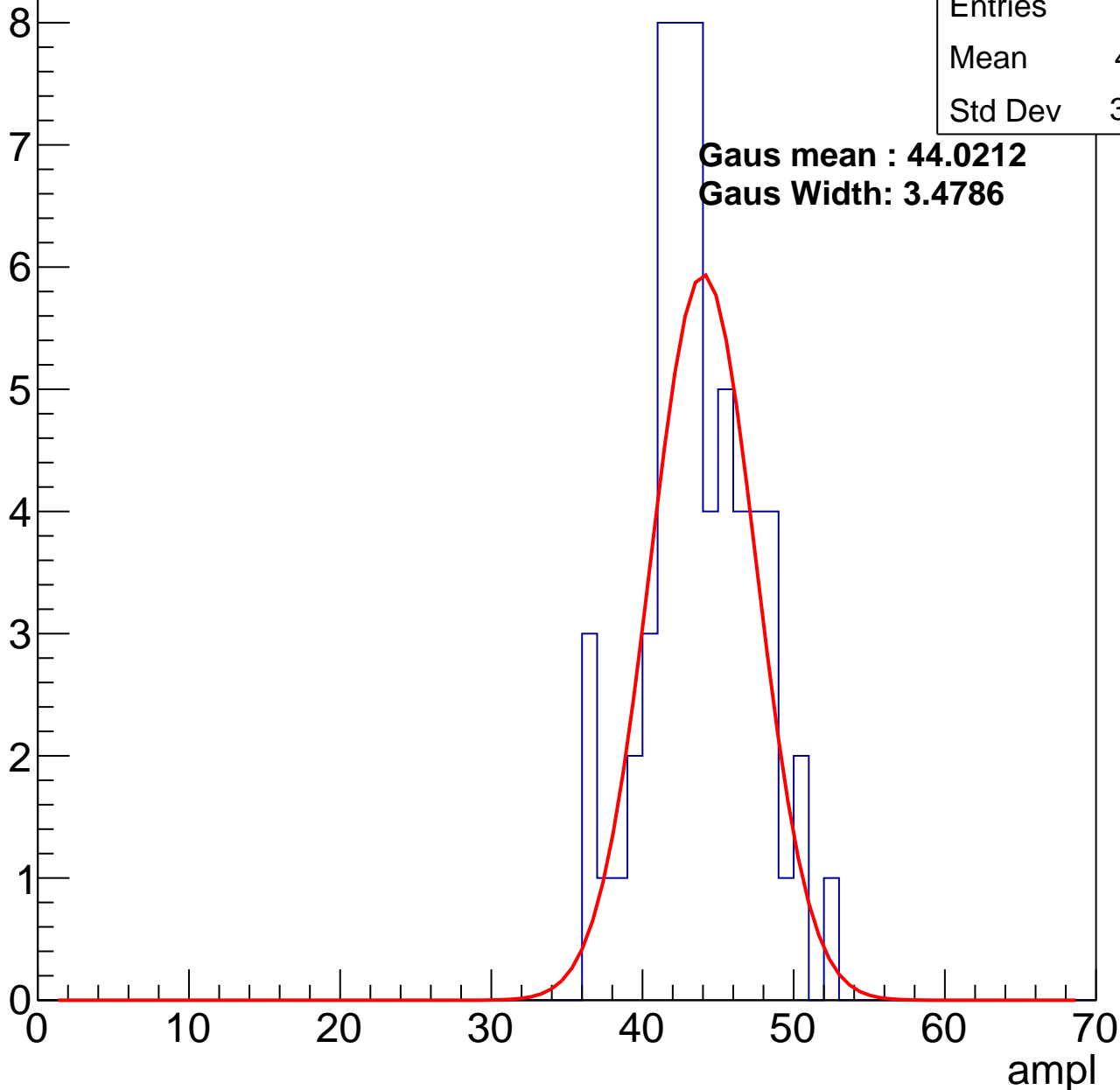
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	43.31
Std Dev	3.543

**Gaus mean : 44.0212**

**Gaus Width: 3.4786**

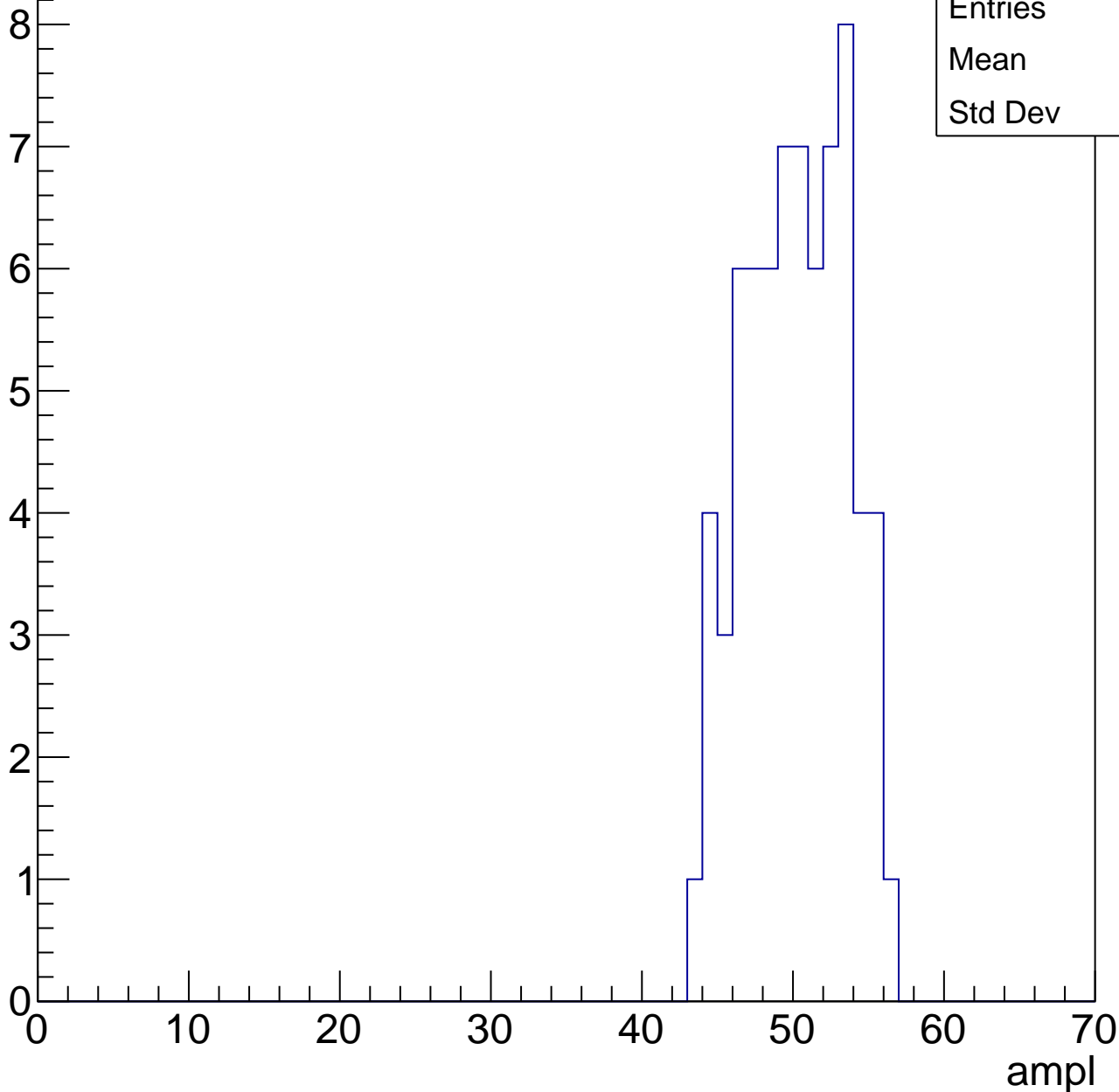


# B1L102S, U3-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	49.7
Std Dev	3.27

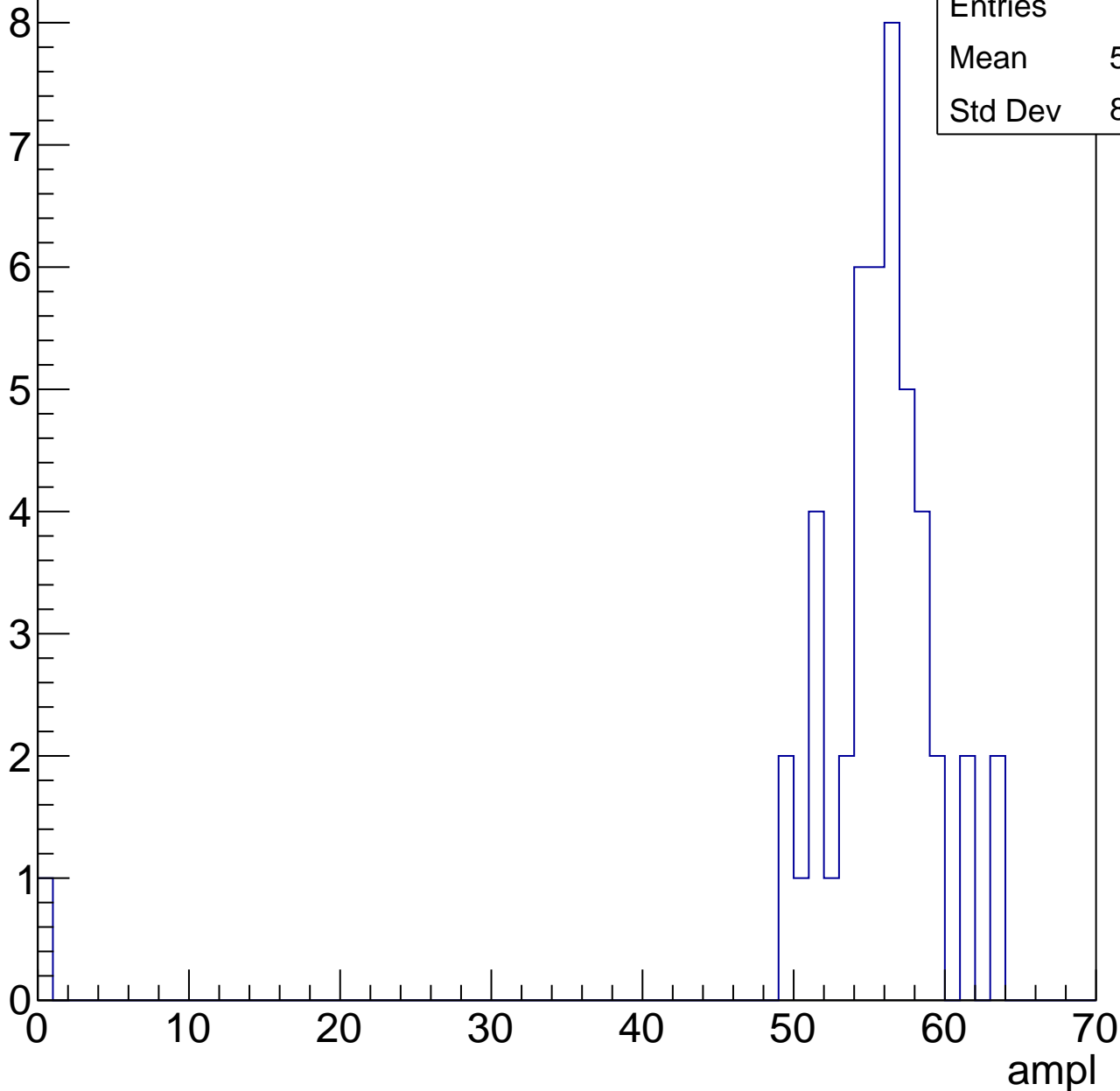


# B1L102S, U3-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	54.24
Std Dev	8.696

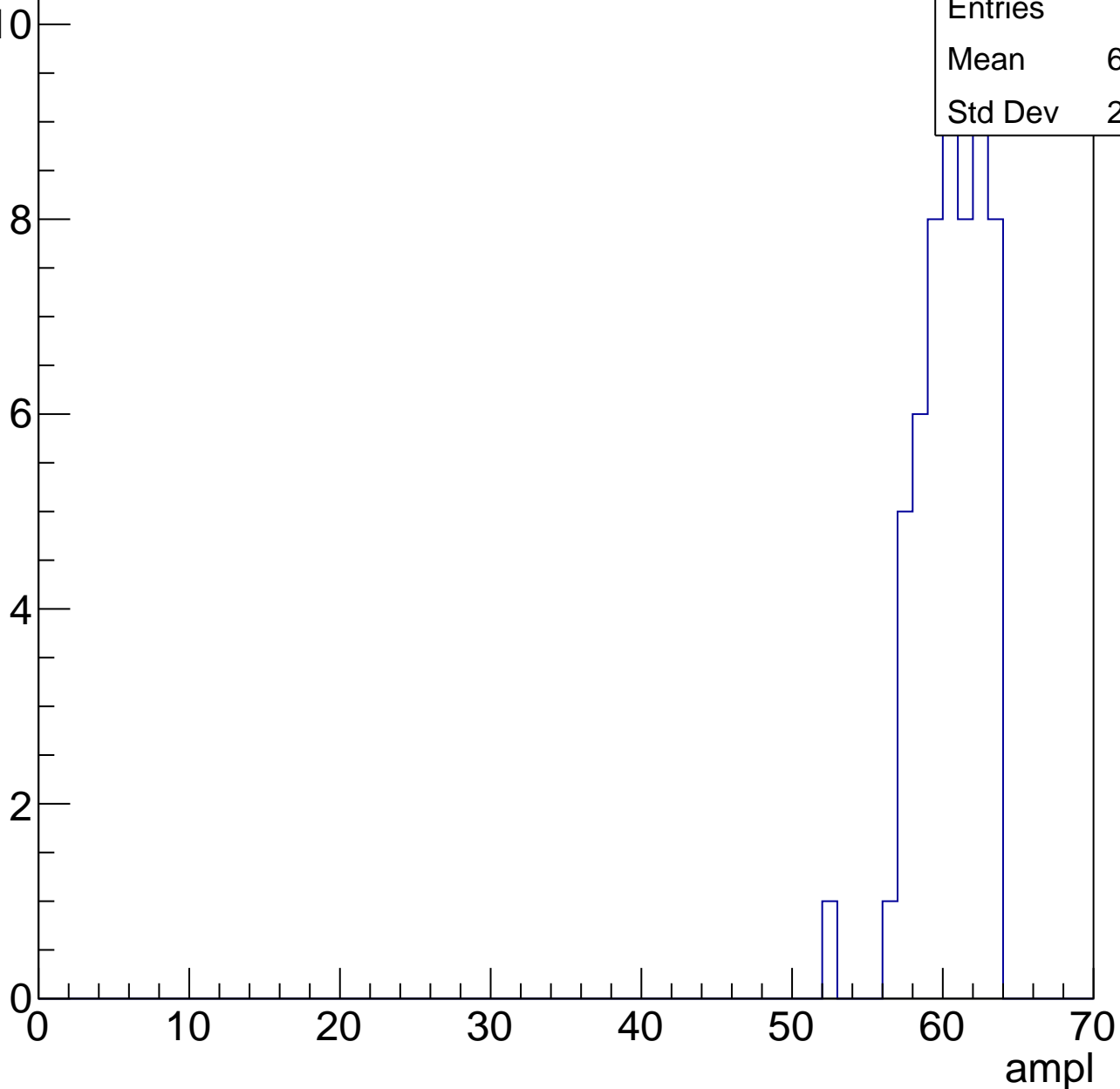


# B1L102S, U3-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	60.09
Std Dev	2.222



# B1L102S, U3-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U3-ch45, adc0

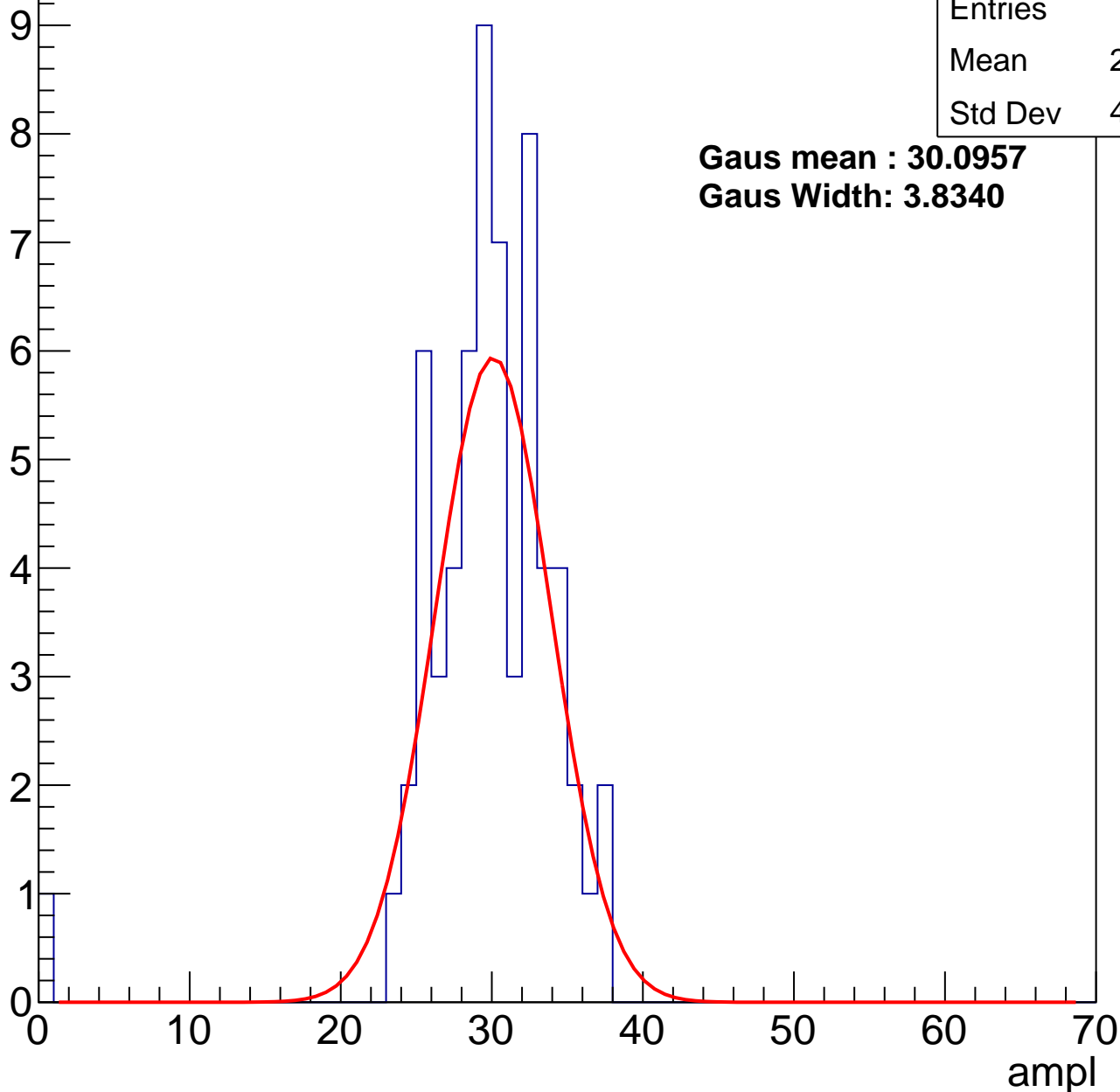
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	29.25
Std Dev	4.995

**Gaus mean : 30.0957**

**Gaus Width: 3.8340**



# B1L102S, U3-ch45, adc1

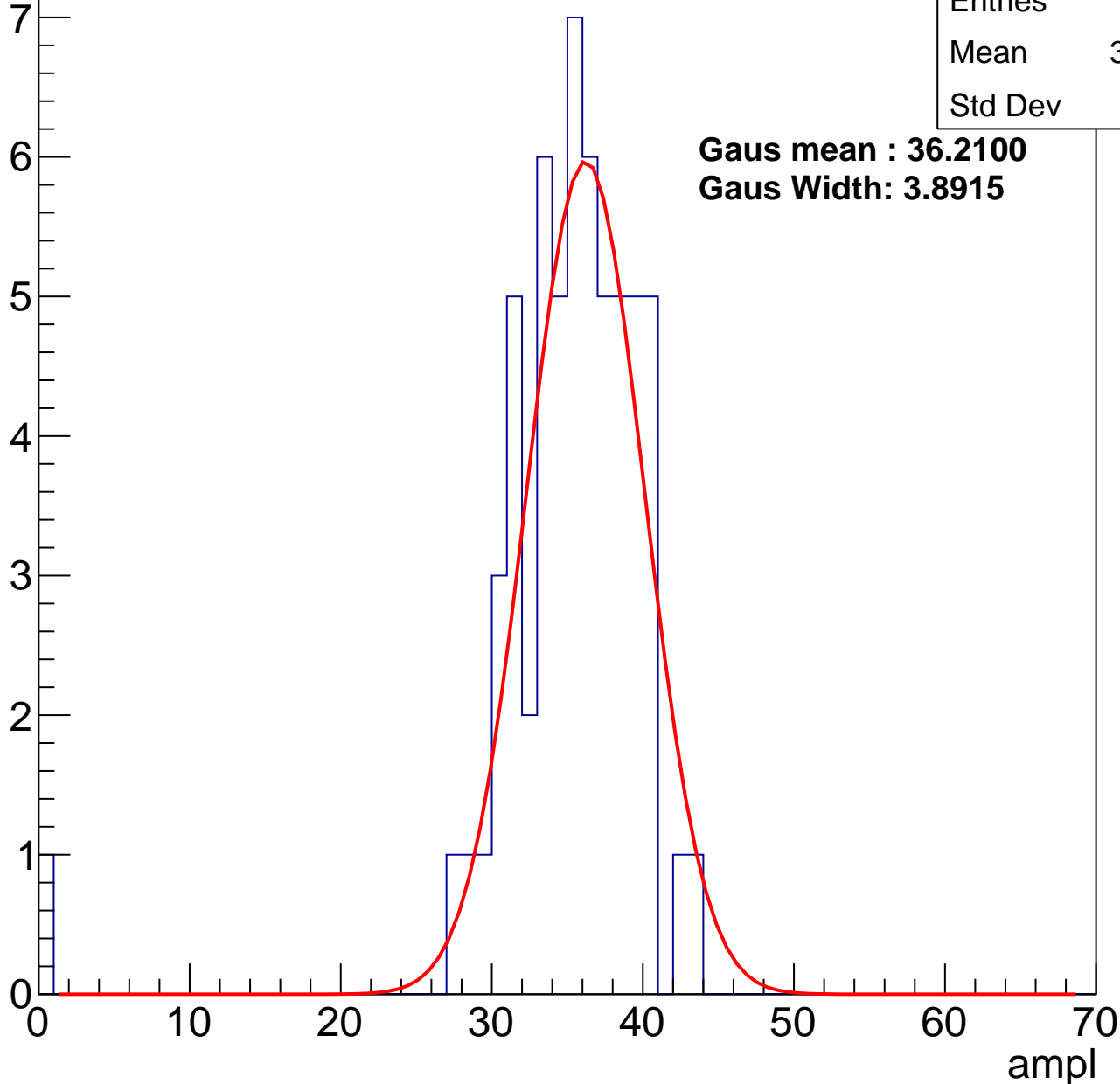
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	34.62
Std Dev	5.71

**Gaus mean : 36.2100**

**Gaus Width: 3.8915**



# B1L102S, U3-ch45, adc2

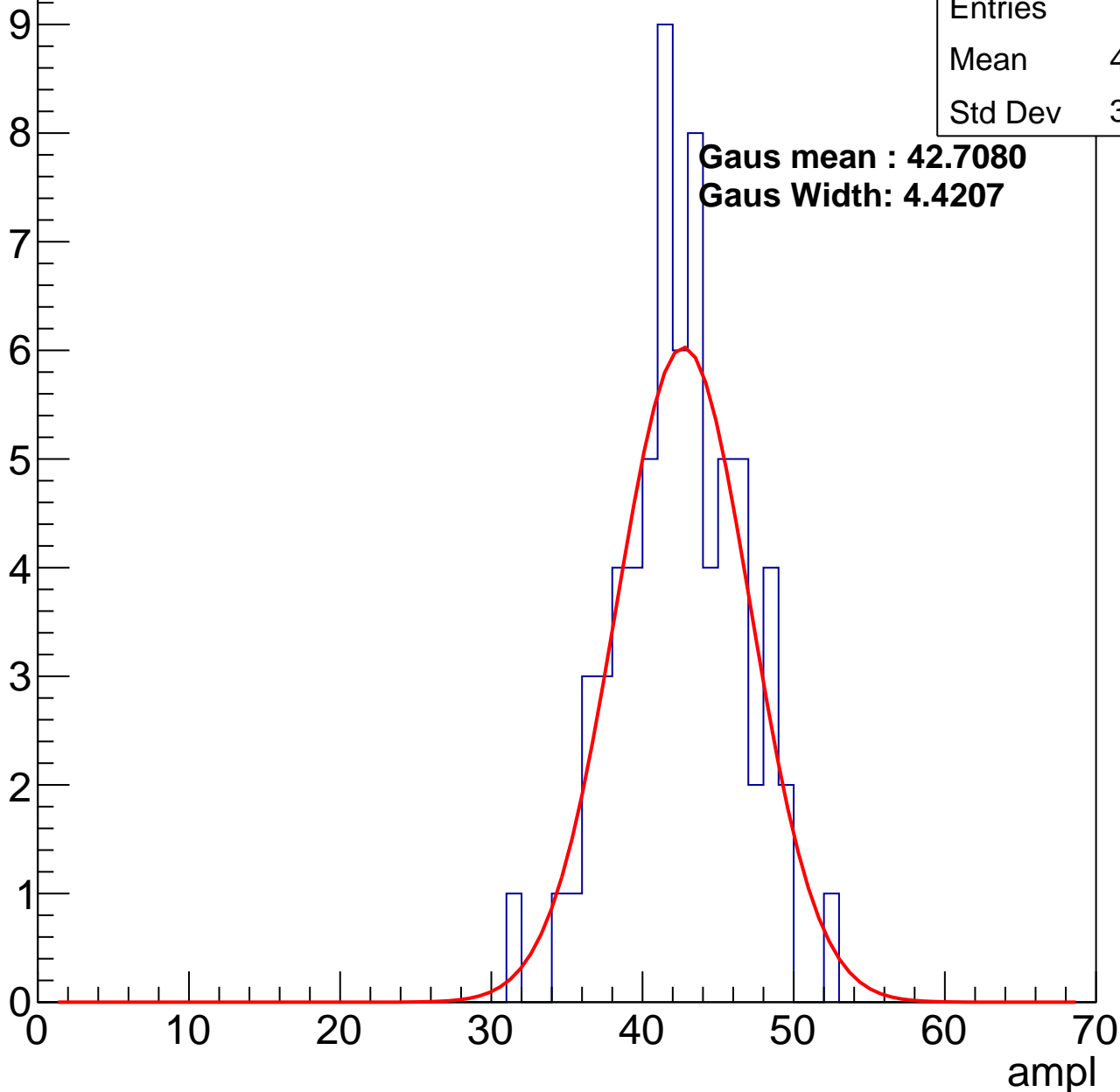
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	42.04
Std Dev	3.998

**Gaus mean : 42.7080**

**Gaus Width: 4.4207**

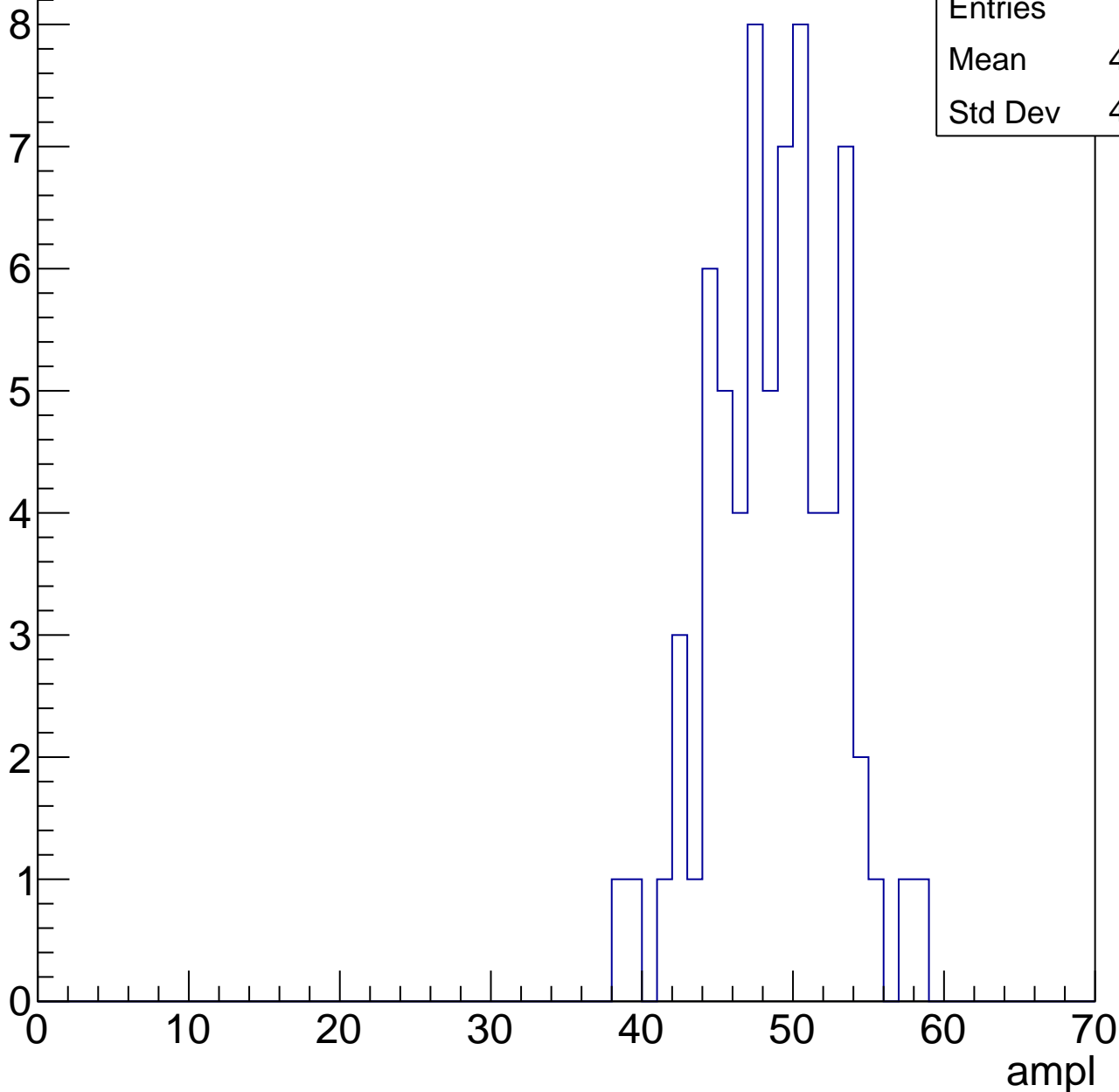


# B1L102S, U3-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

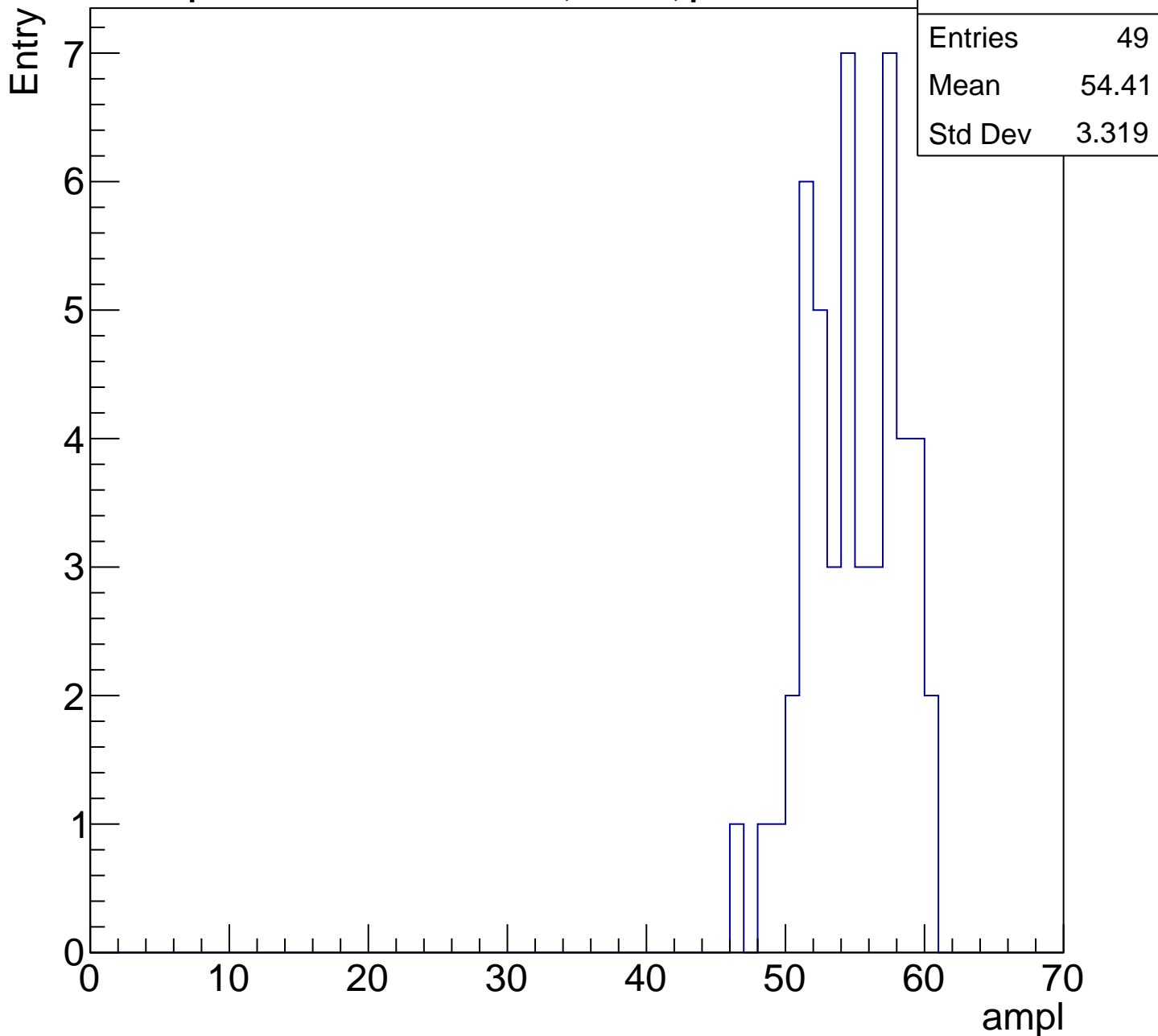
Entry

Entries	70
Mean	48.29
Std Dev	4.033



# B1L102S, U3-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U3-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

7

6

5

4

3

2

1

0

Entries	52
Mean	57.87
Std Dev	8.517

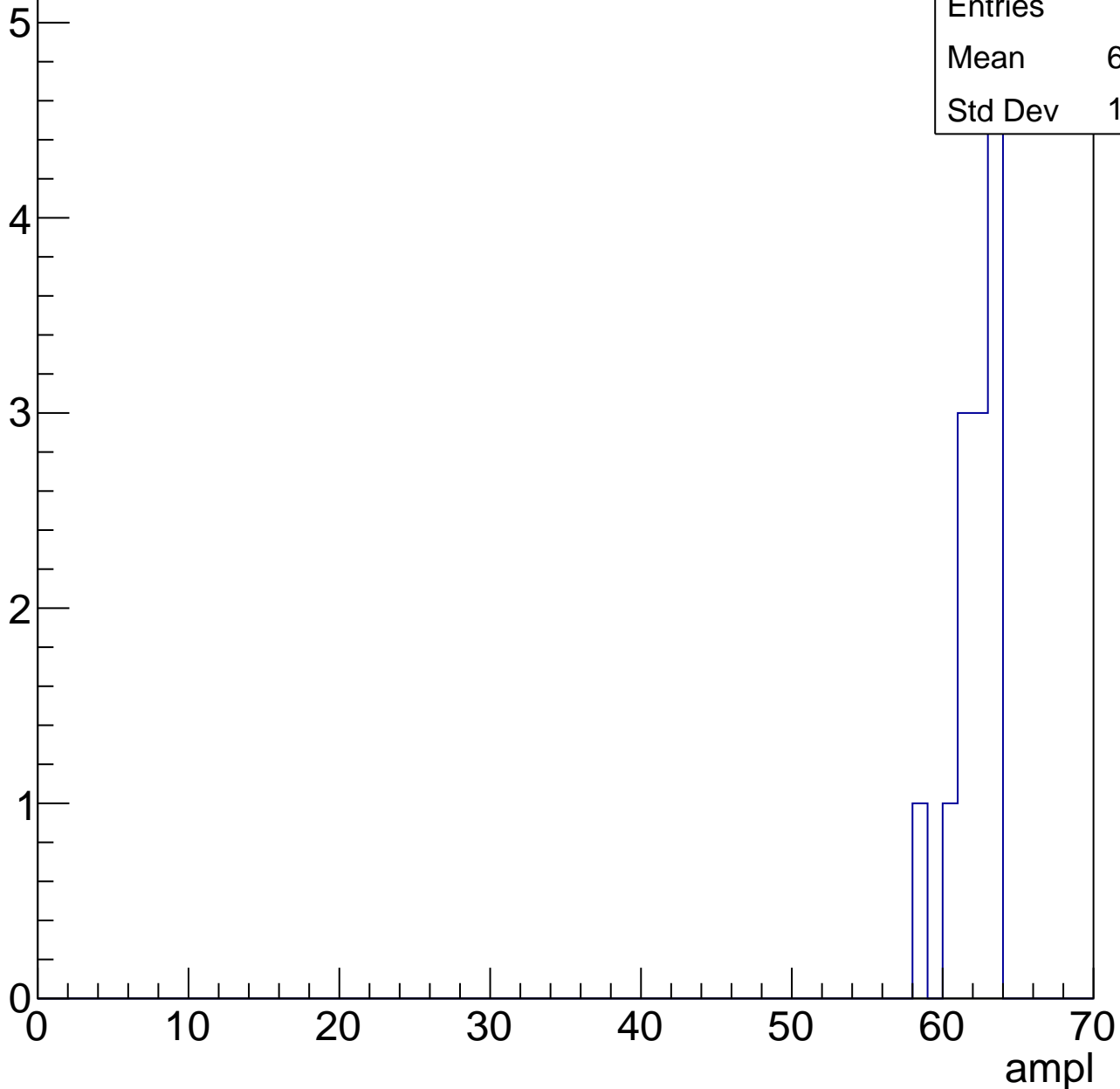
ampl

# B1L102S, U3-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	13
Mean	61.69
Std Dev	1.435





# B1L102S, U3-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	28.33
Std Dev	26.11

# B1L102S, U3-ch46, adc0

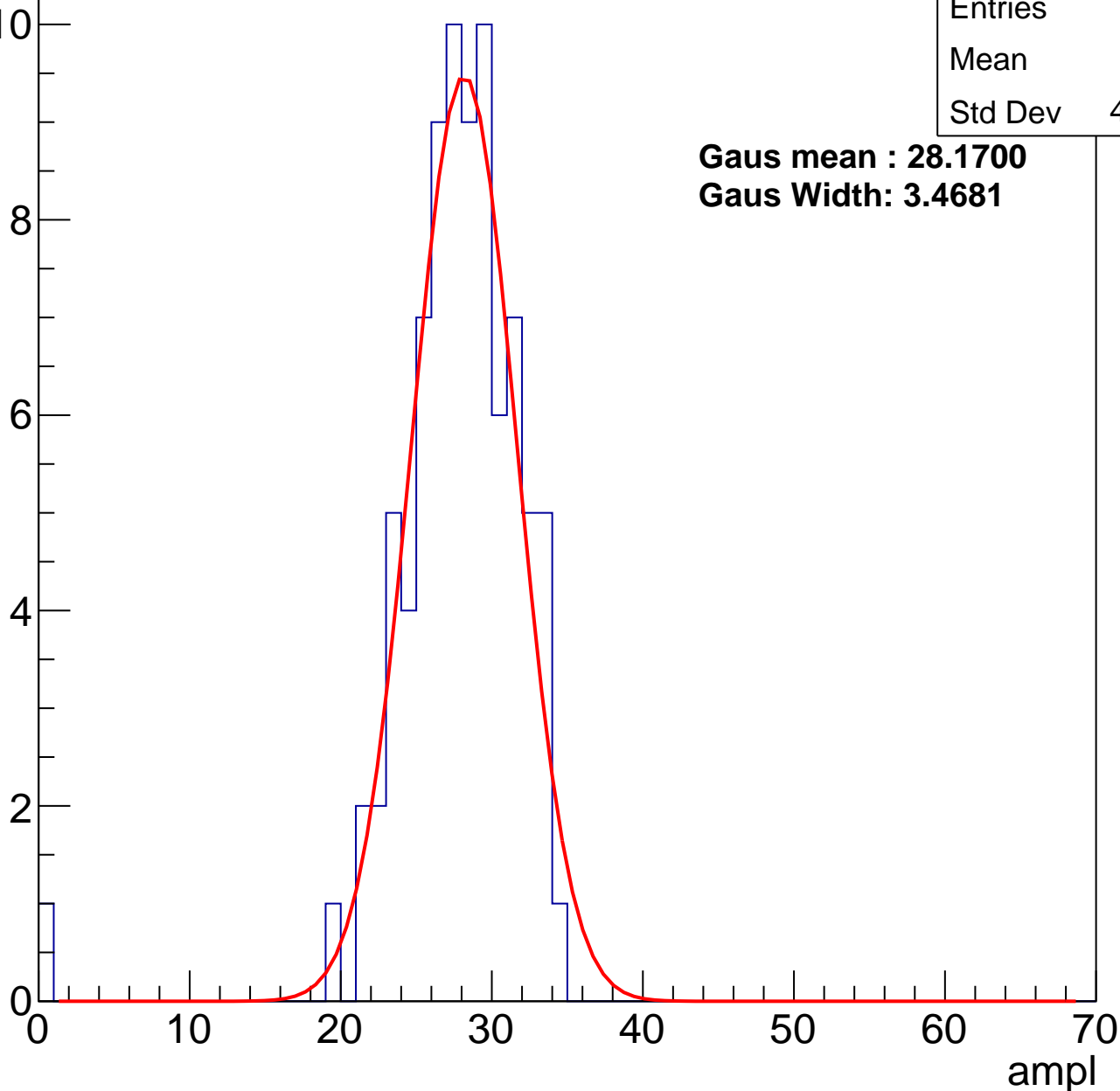
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	27.3
Std Dev	4.404

**Gaus mean : 28.1700**

**Gaus Width: 3.4681**



# B1L102S, U3-ch46, adc1

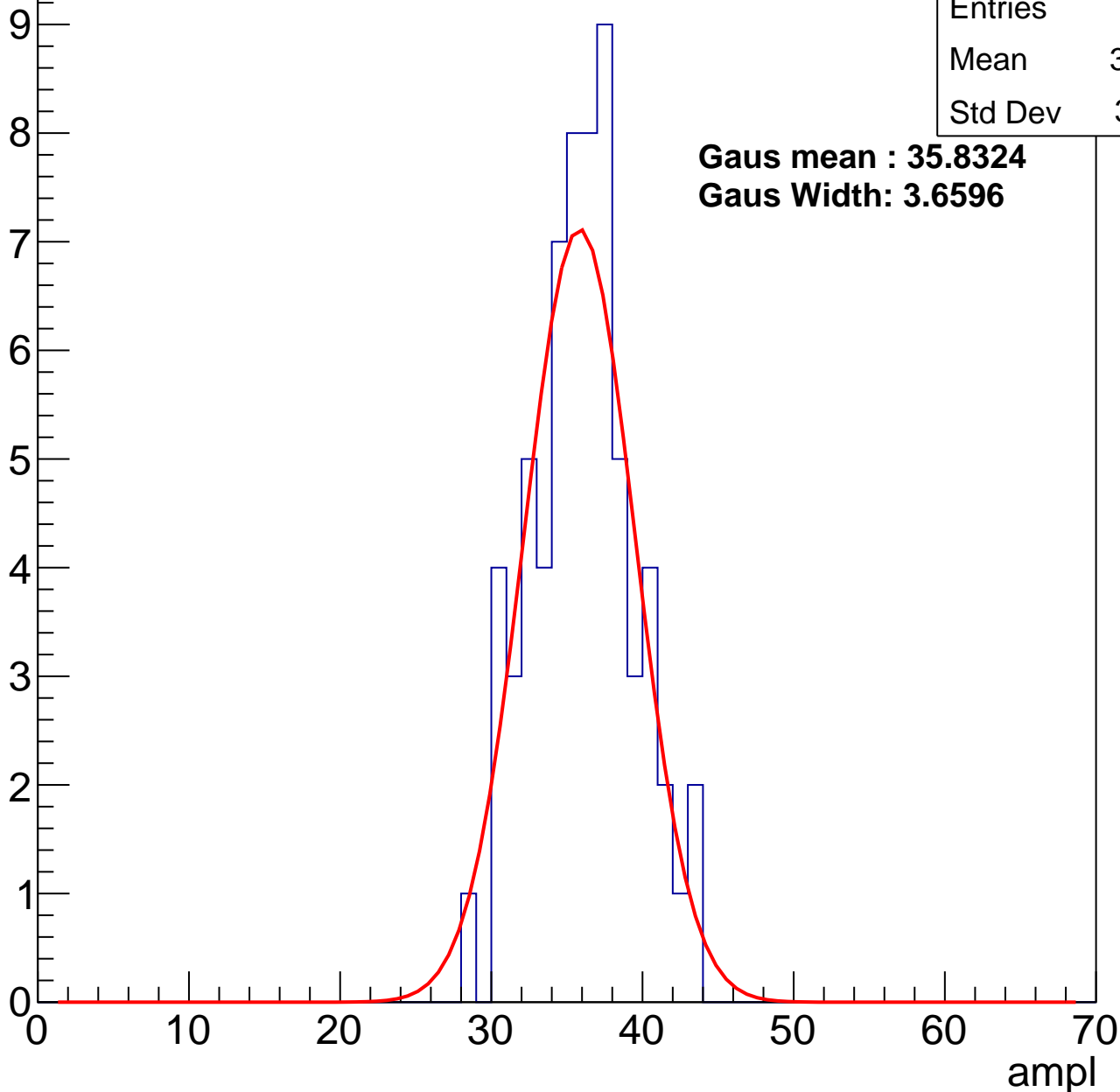
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	35.59
Std Dev	3.321

**Gaus mean : 35.8324**

**Gaus Width: 3.6596**



# B1L102S, U3-ch46, adc2

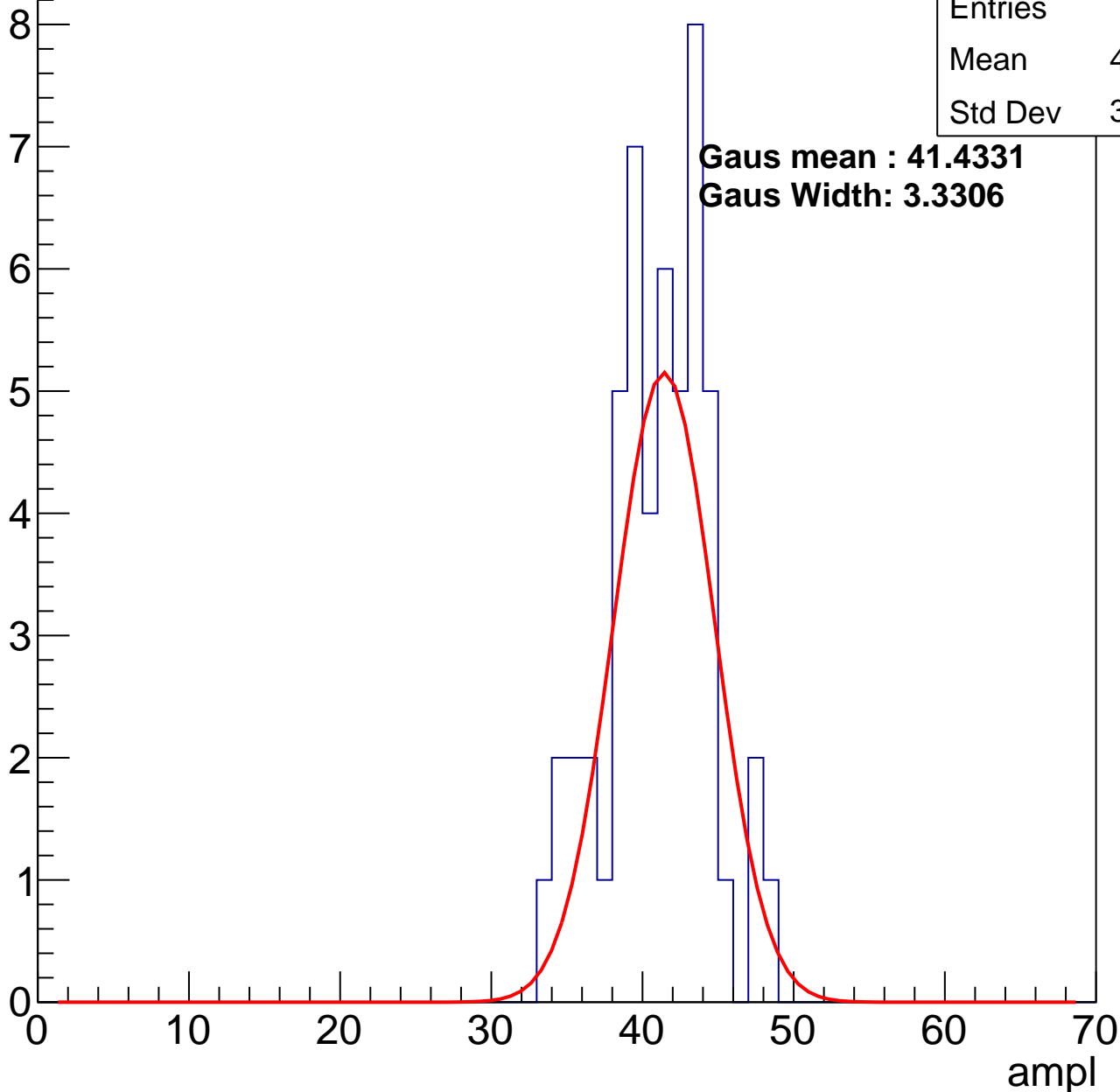
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	40.58
Std Dev	3.359

**Gaus mean : 41.4331**

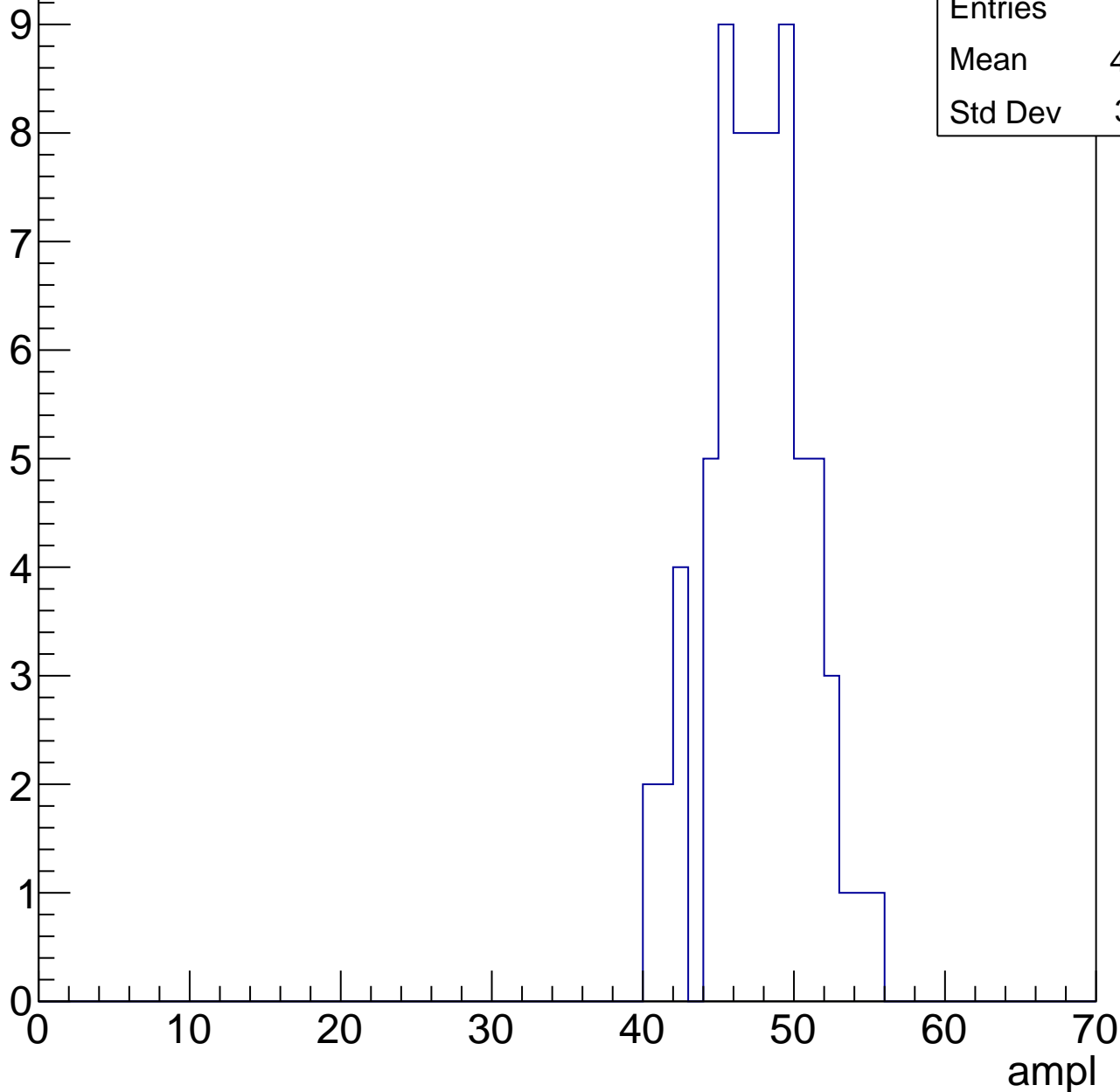
**Gaus Width: 3.3306**



# B1L102S, U3-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

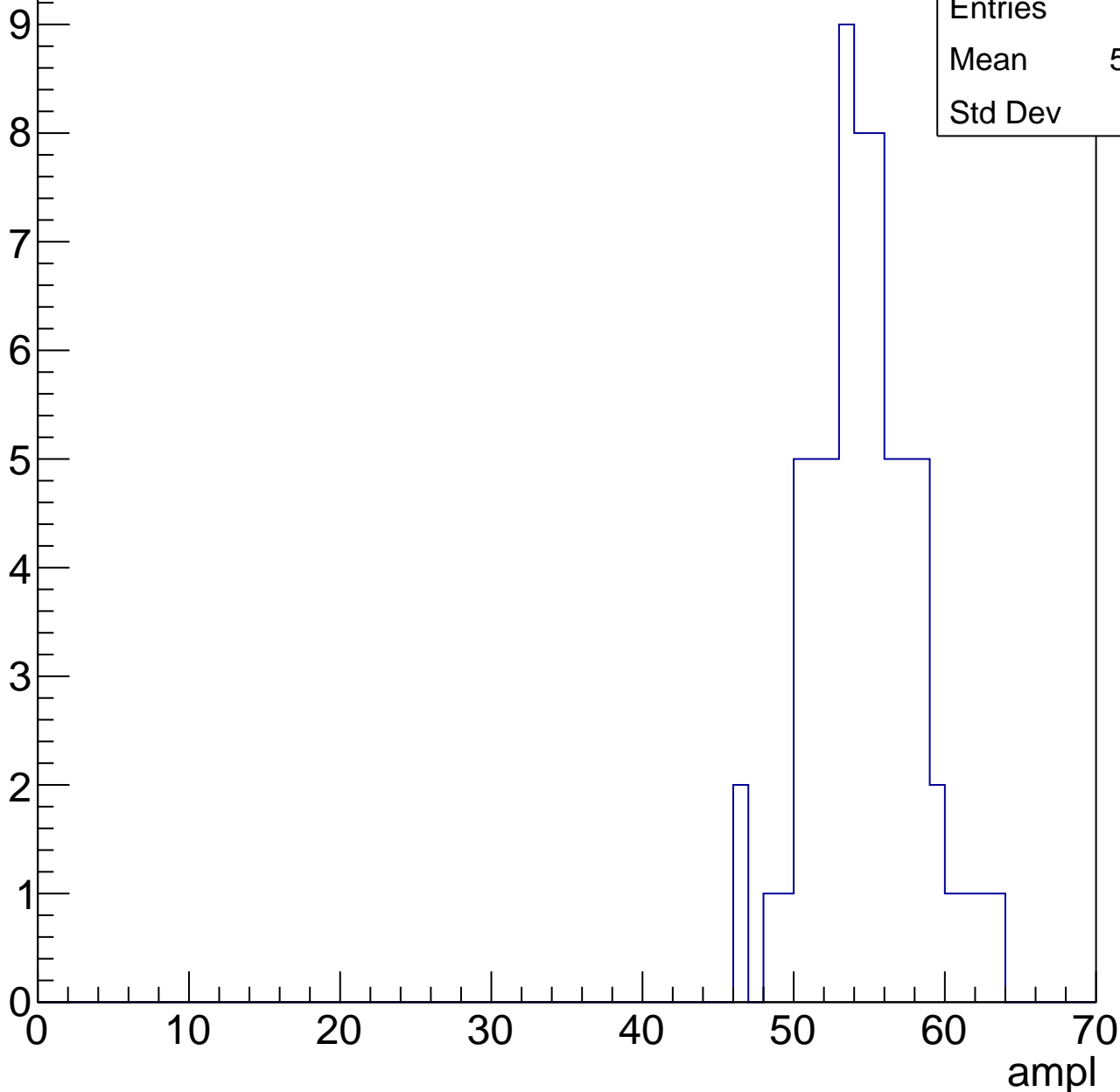


Entries	71
Mean	47.14
Std Dev	3.251

# B1L102S, U3-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	65
Mean	54.18
Std Dev	3.45

# B1L102S, U3-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

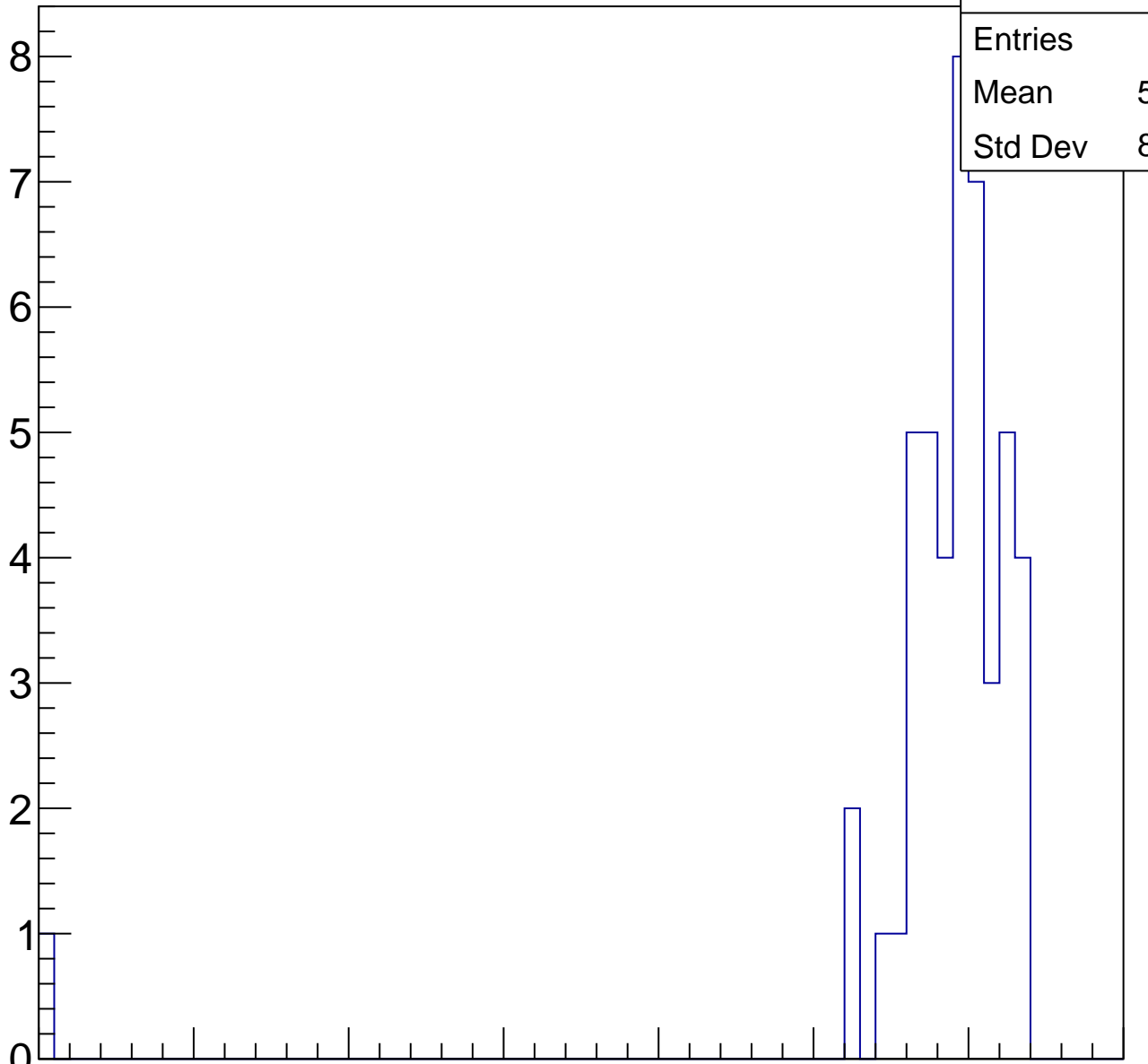
Entry

Entries	46
Mean	57.54
Std Dev	8.992

8  
7  
6  
5  
4  
3  
2  
1  
0

0 10 20 30 40 50 60 70

ampl

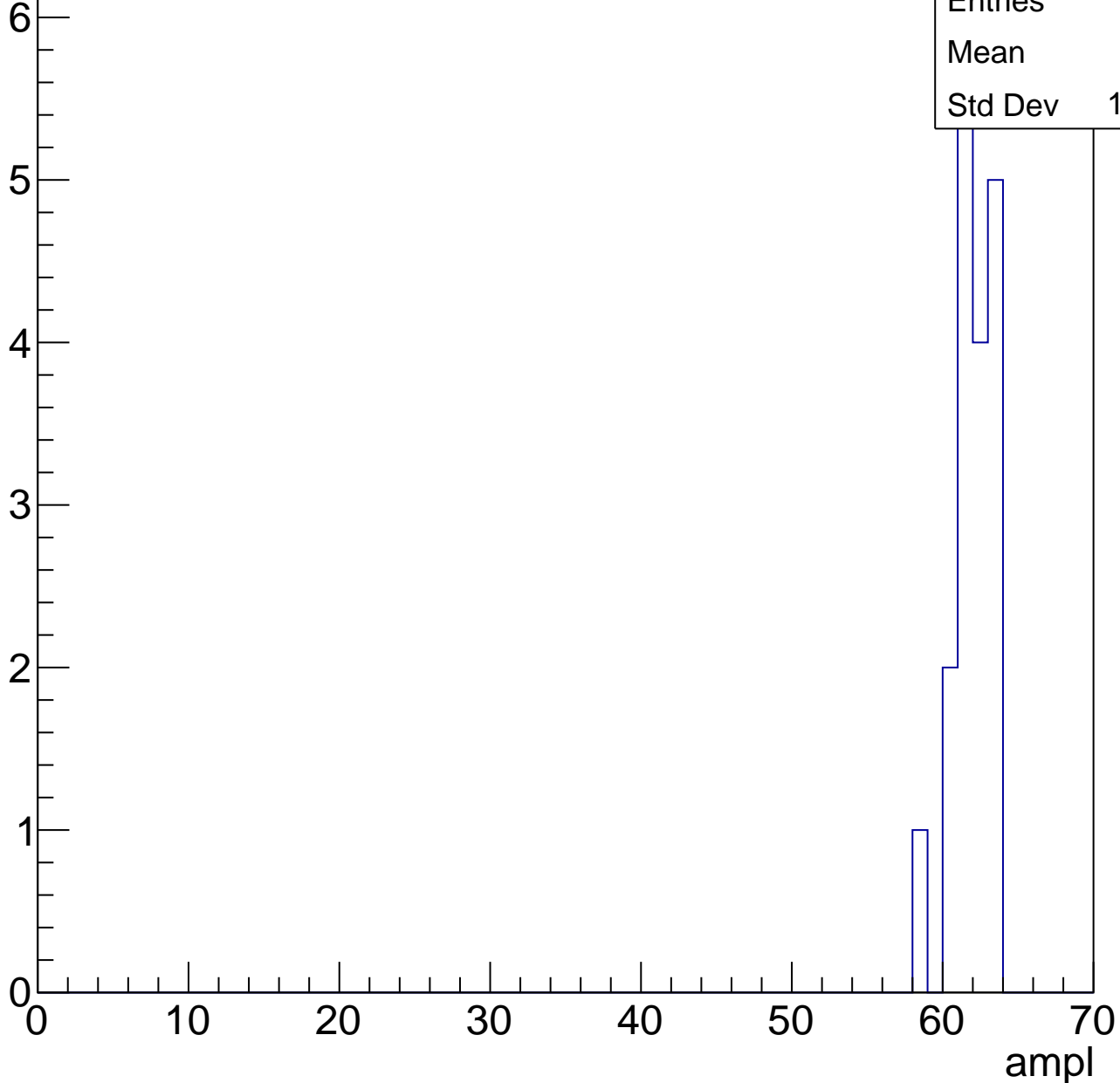


# B1L102S, U3-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	18
Mean	61.5
Std Dev	1.302





# B1L102S, U3-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U3-ch47, adc0

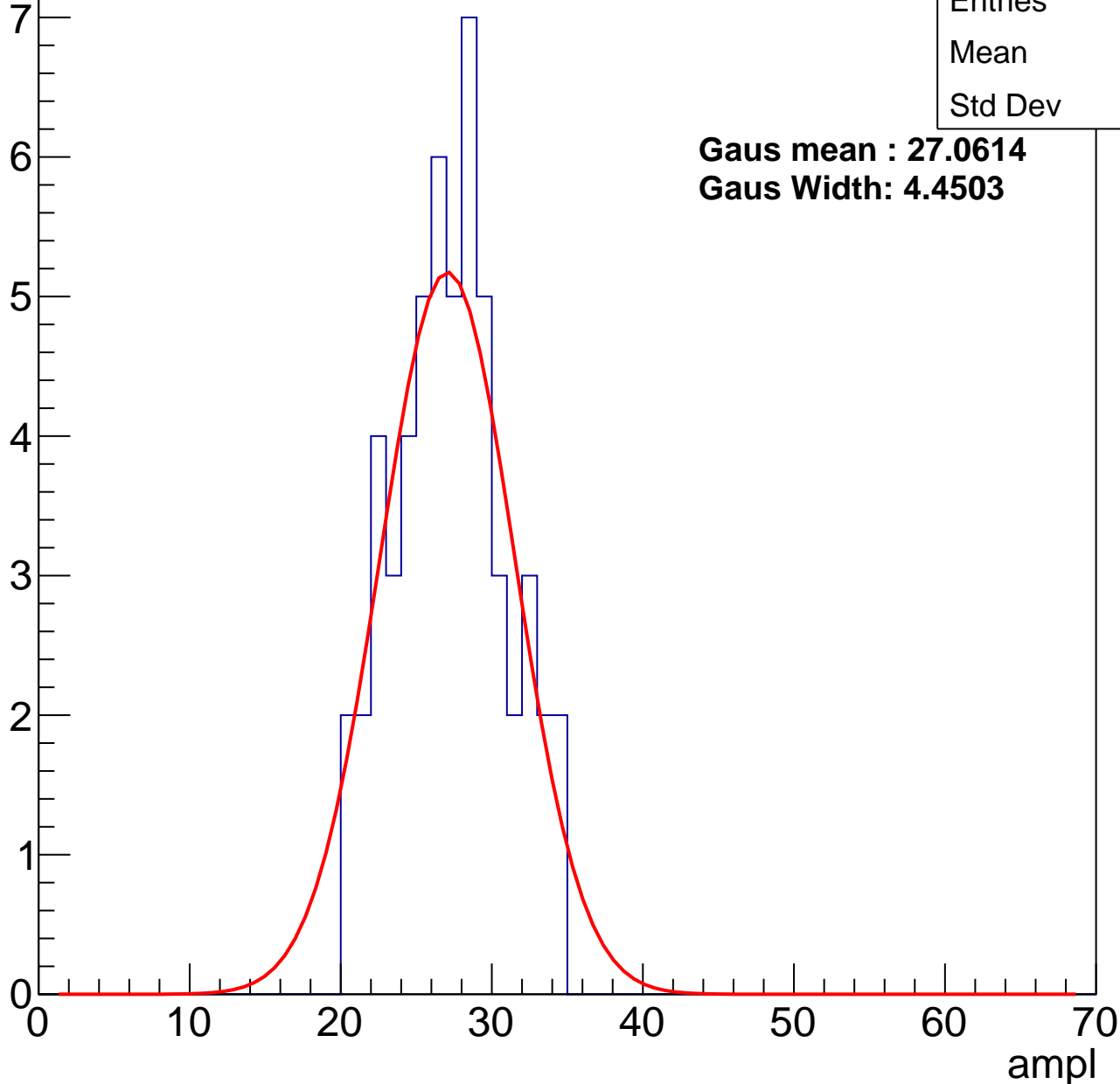
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	26.8
Std Dev	3.59

**Gaus mean : 27.0614**

**Gaus Width: 4.4503**



# B1L102S, U3-ch47, adc1

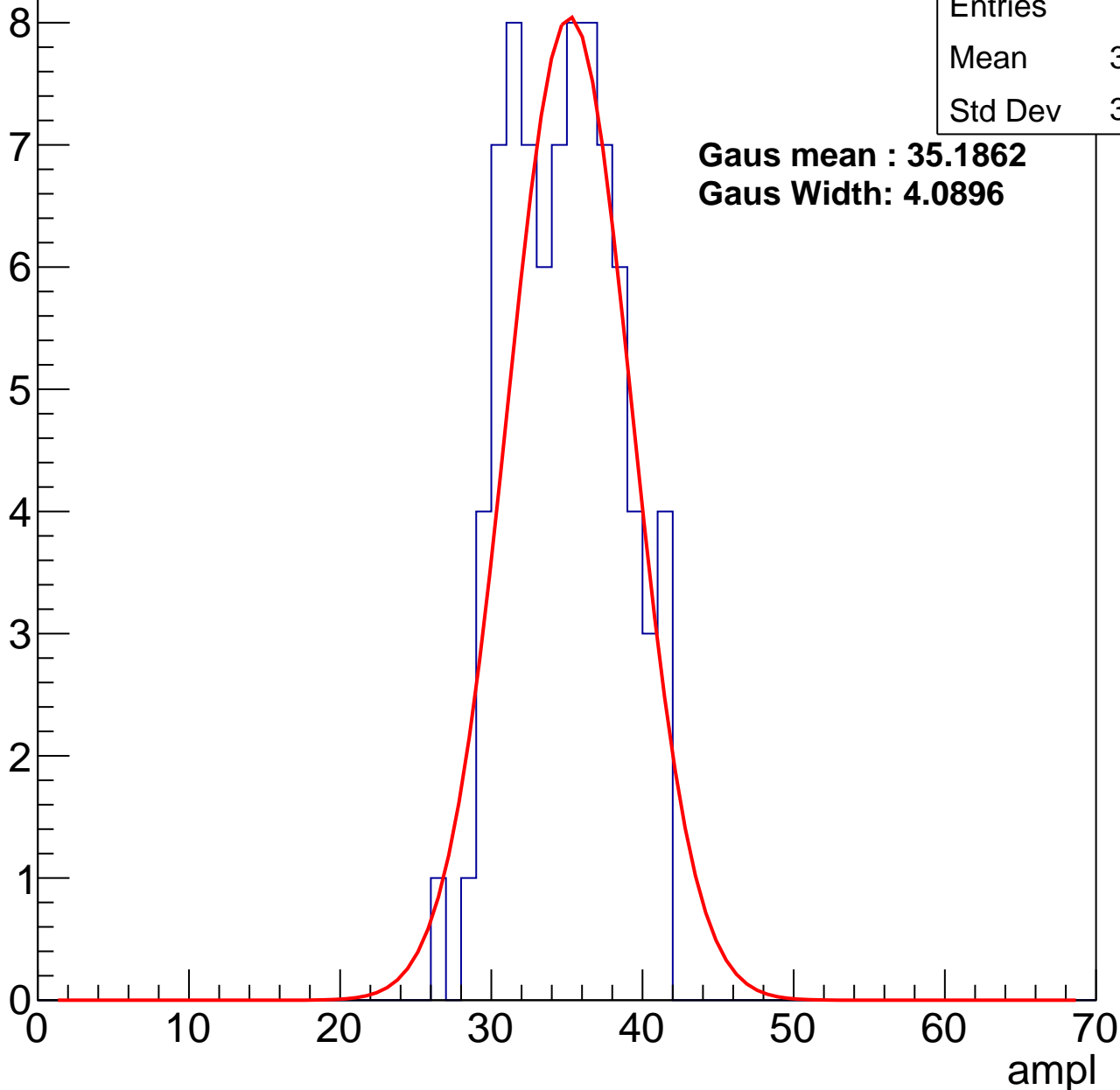
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	81
Mean	34.36
Std Dev	3.532

**Gaus mean : 35.1862**

**Gaus Width: 4.0896**



# B1L102S, U3-ch47, adc2

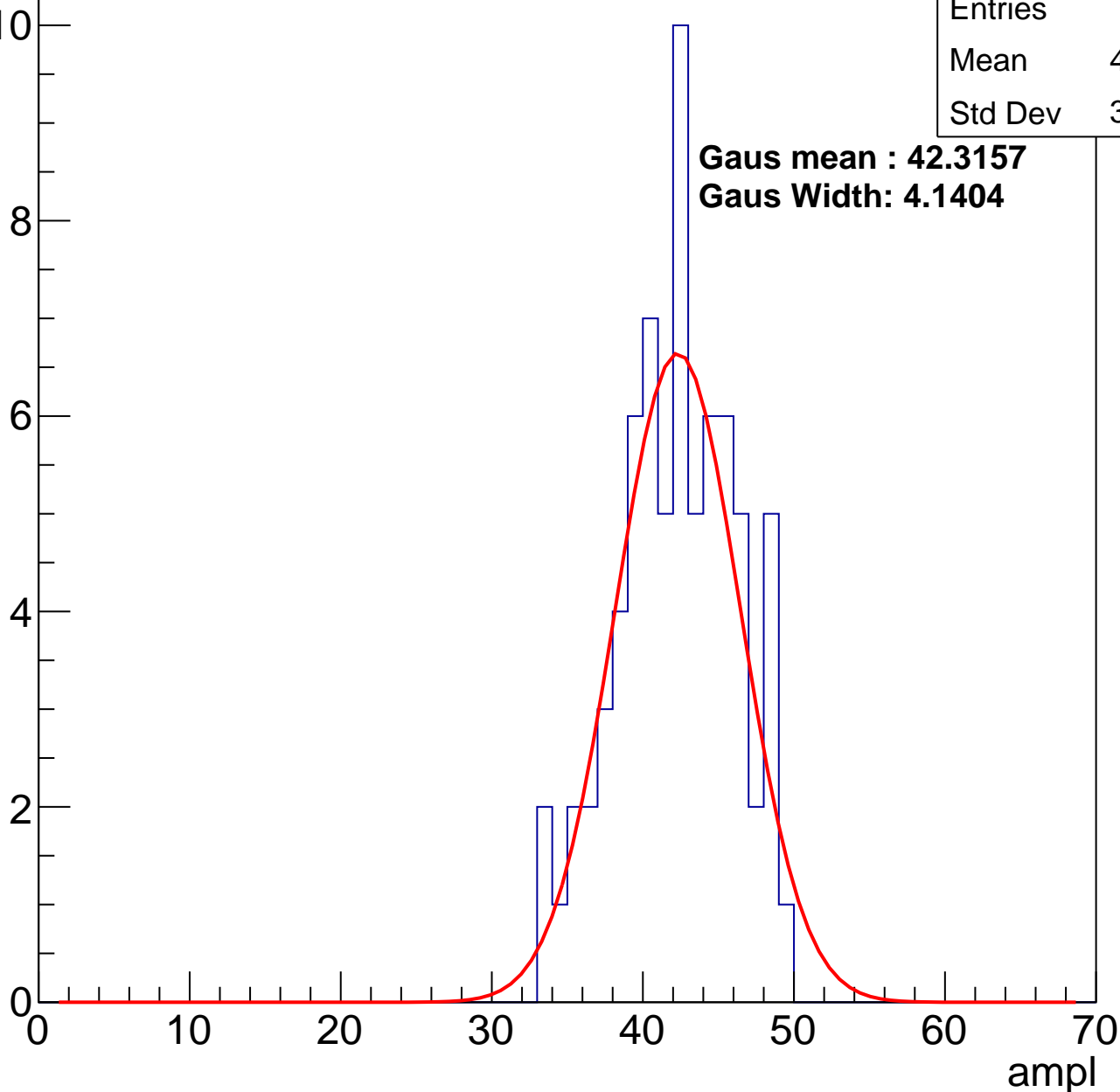
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	41.75
Std Dev	3.836

**Gaus mean : 42.3157**

**Gaus Width: 4.1404**

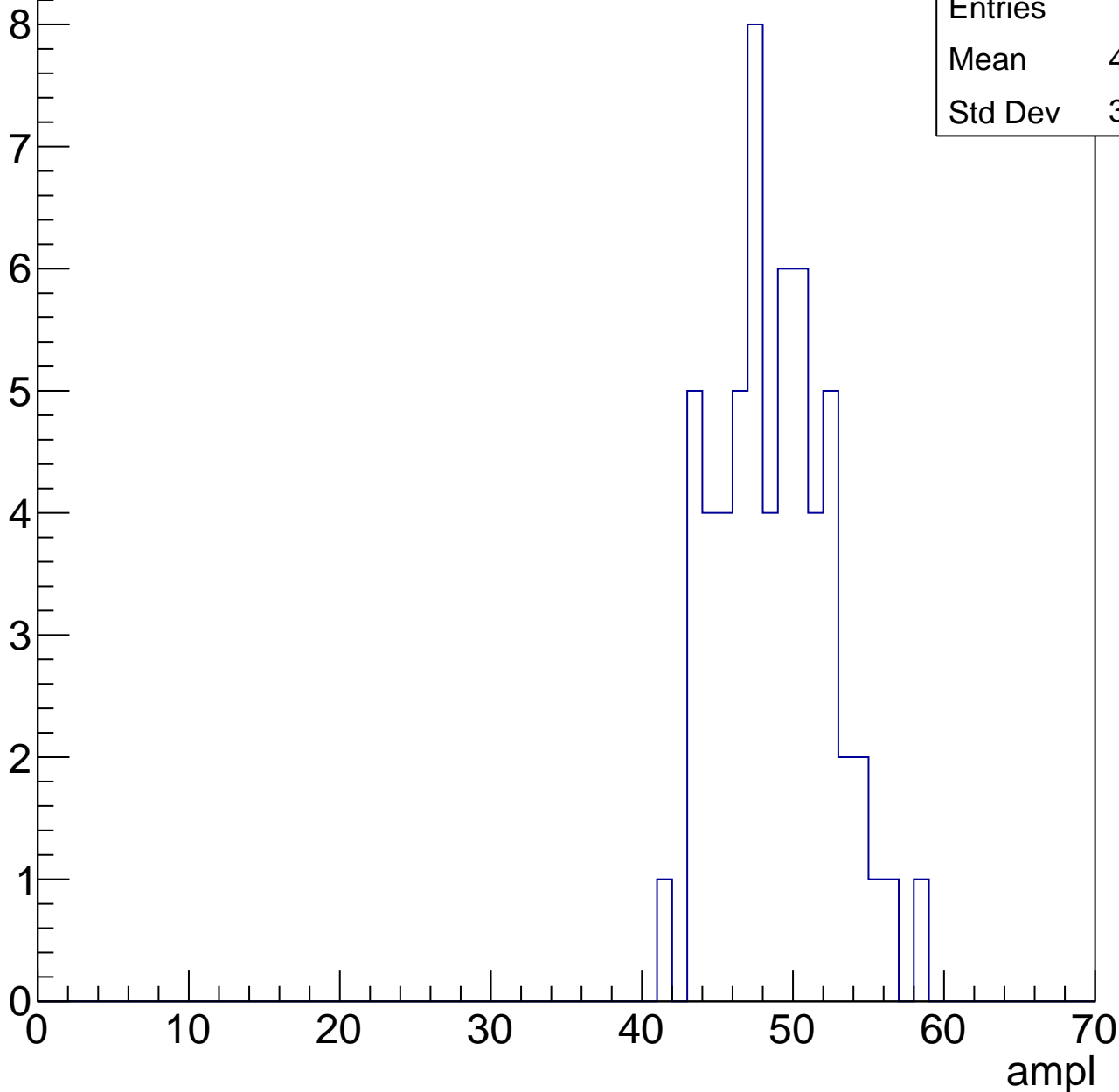


# B1L102S, U3-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	48.32
Std Dev	3.629

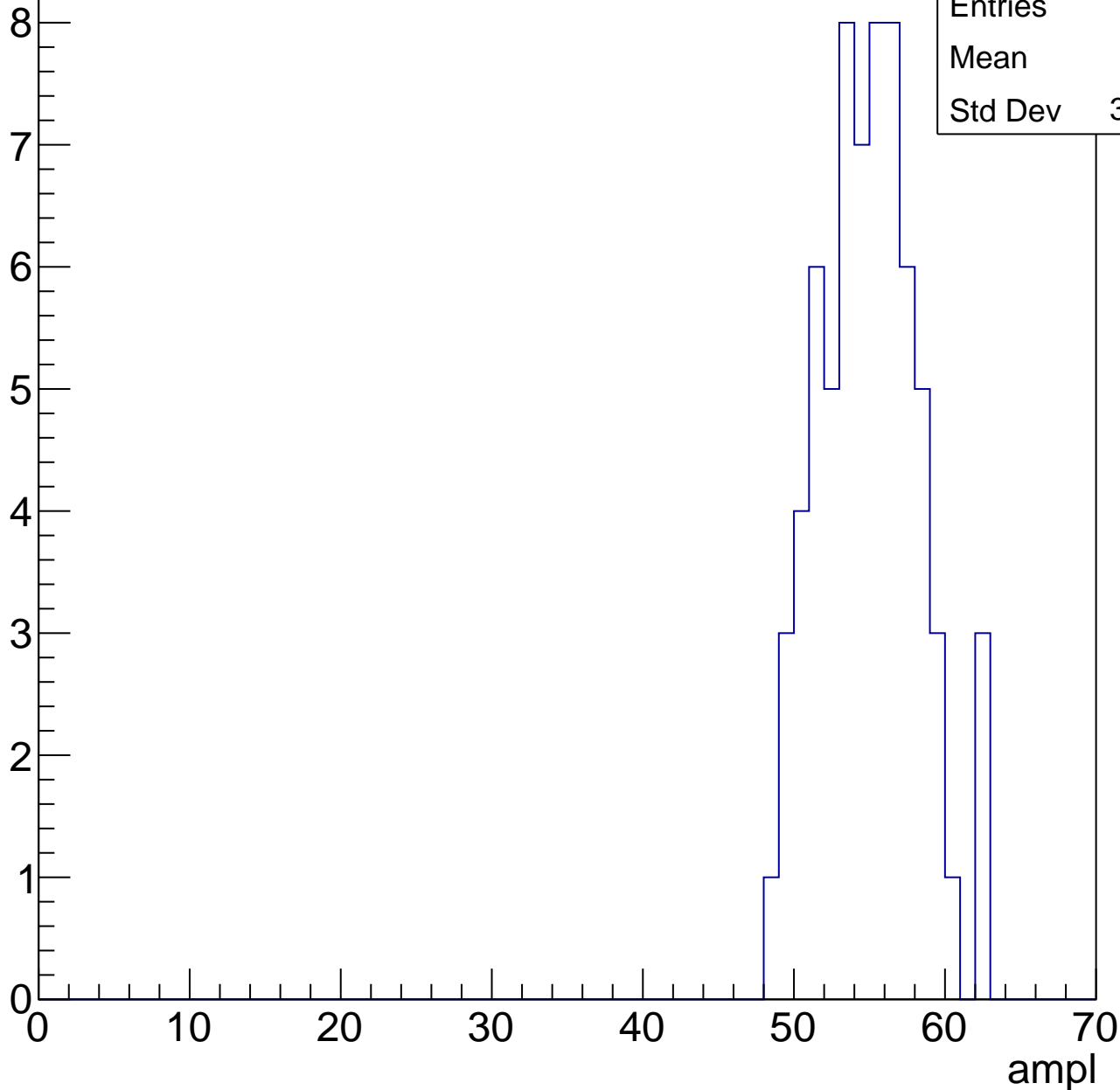


# B1L102S, U3-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	54.5
Std Dev	3.247

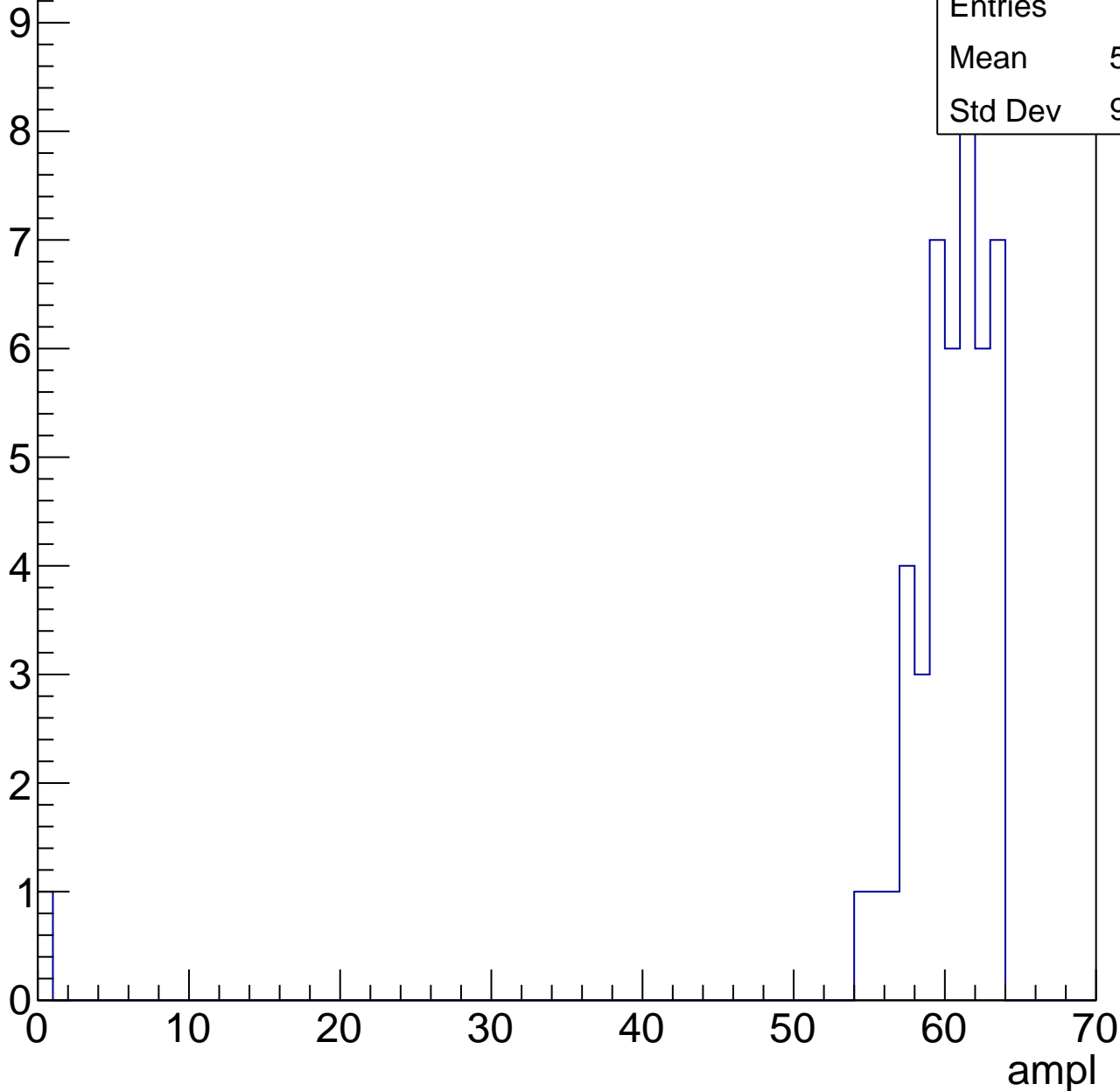


# B1L102S, U3-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	58.74
Std Dev	9.035



# B1L102S, U3-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

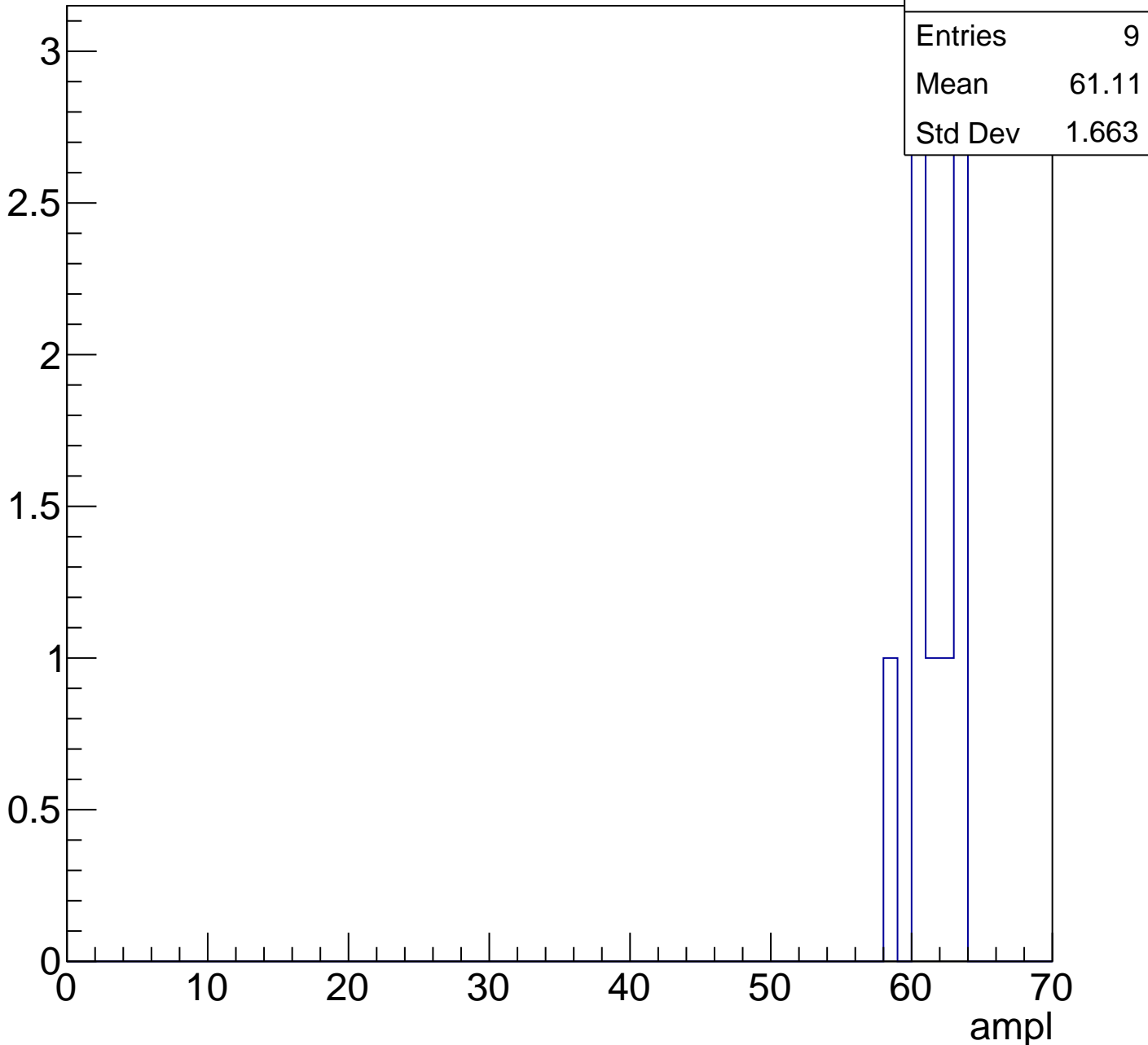
9

Mean

61.11

Std Dev

1.663





# B1L102S, U3-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U3-ch48, adc0

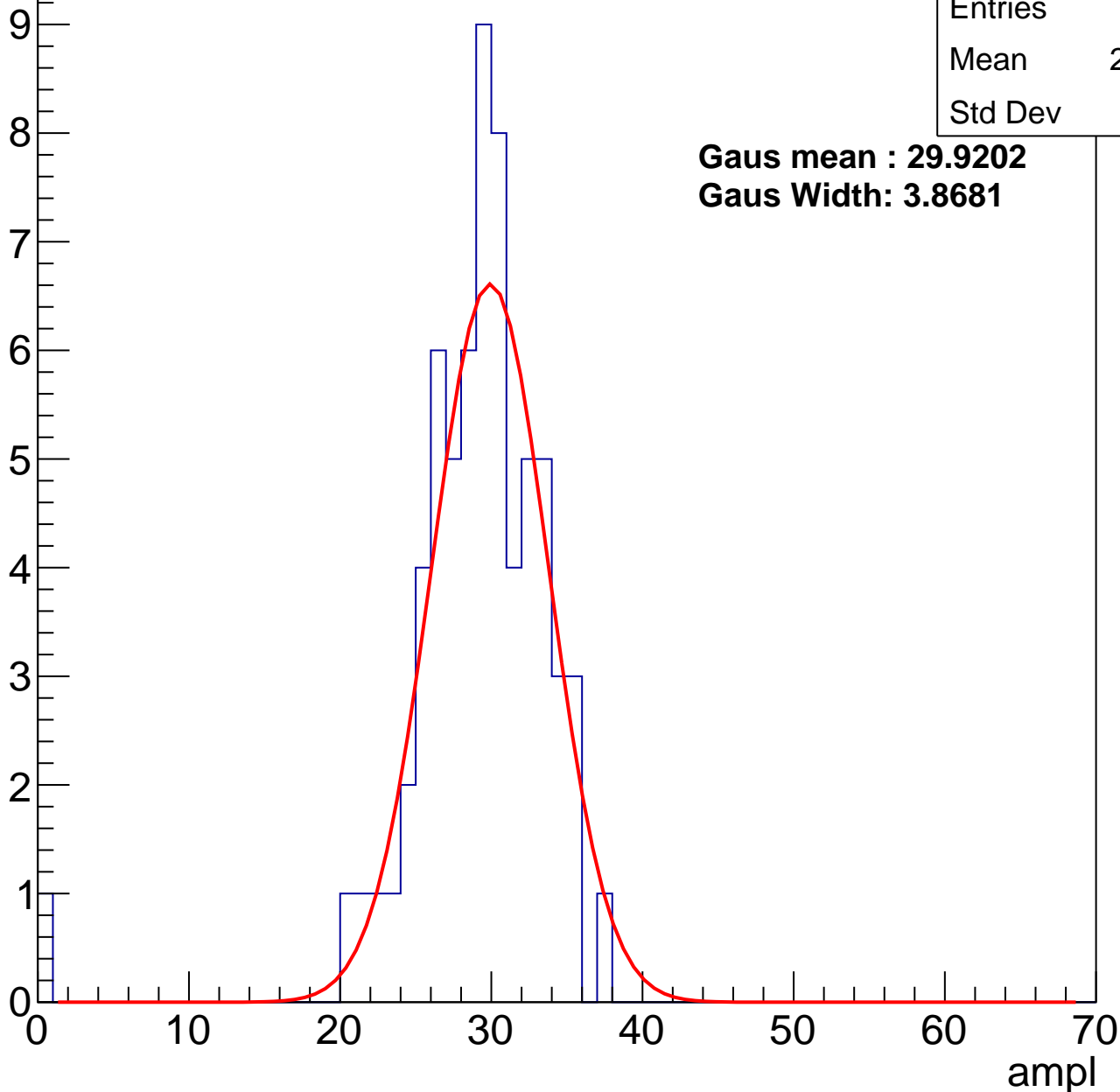
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	28.59
Std Dev	5

**Gaus mean : 29.9202**

**Gaus Width: 3.8681**



# B1L102S, U3-ch48, adc1

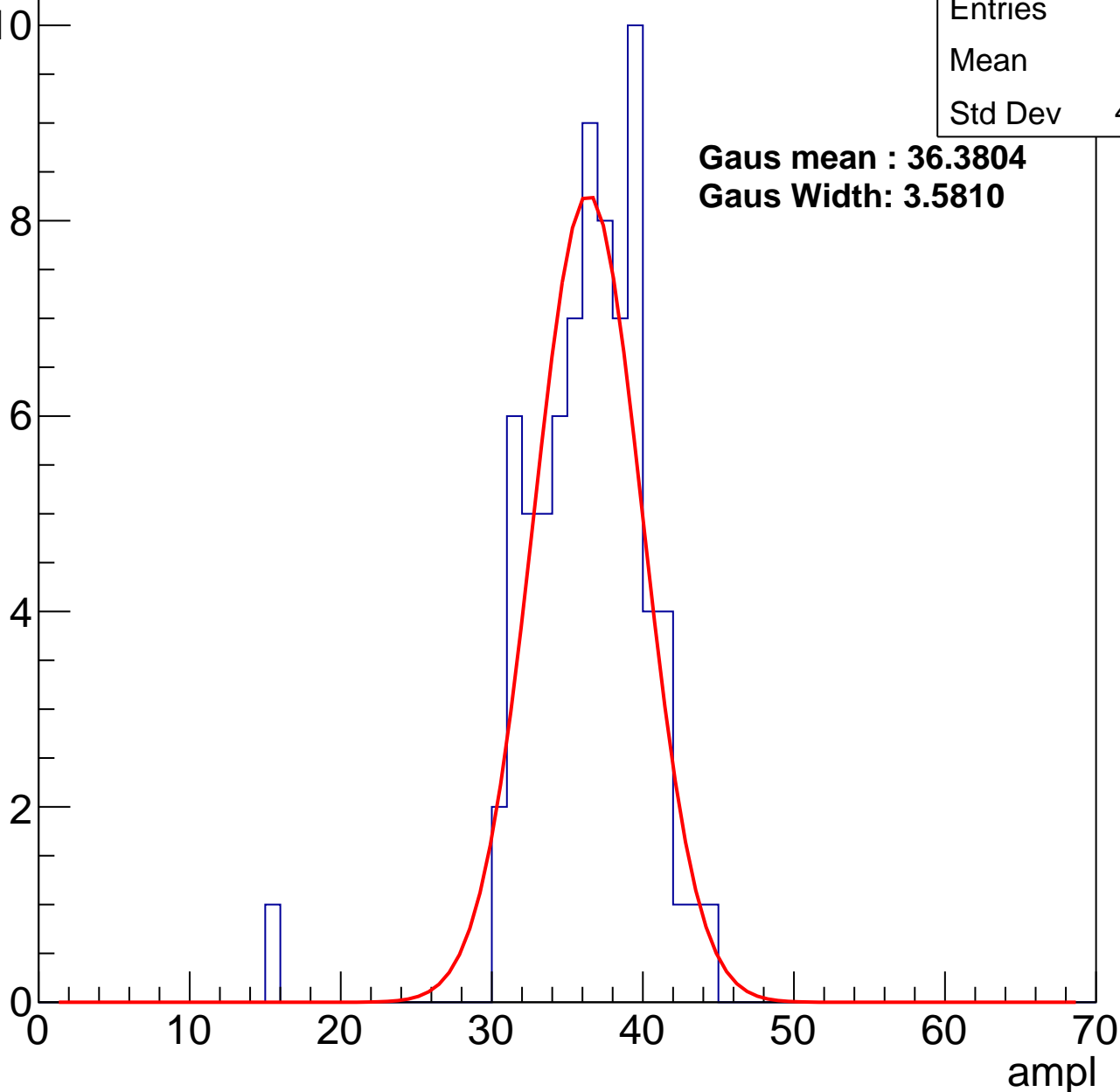
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	35.9
Std Dev	4.041

**Gaus mean : 36.3804**

**Gaus Width: 3.5810**



# B1L102S, U3-ch48, adc2

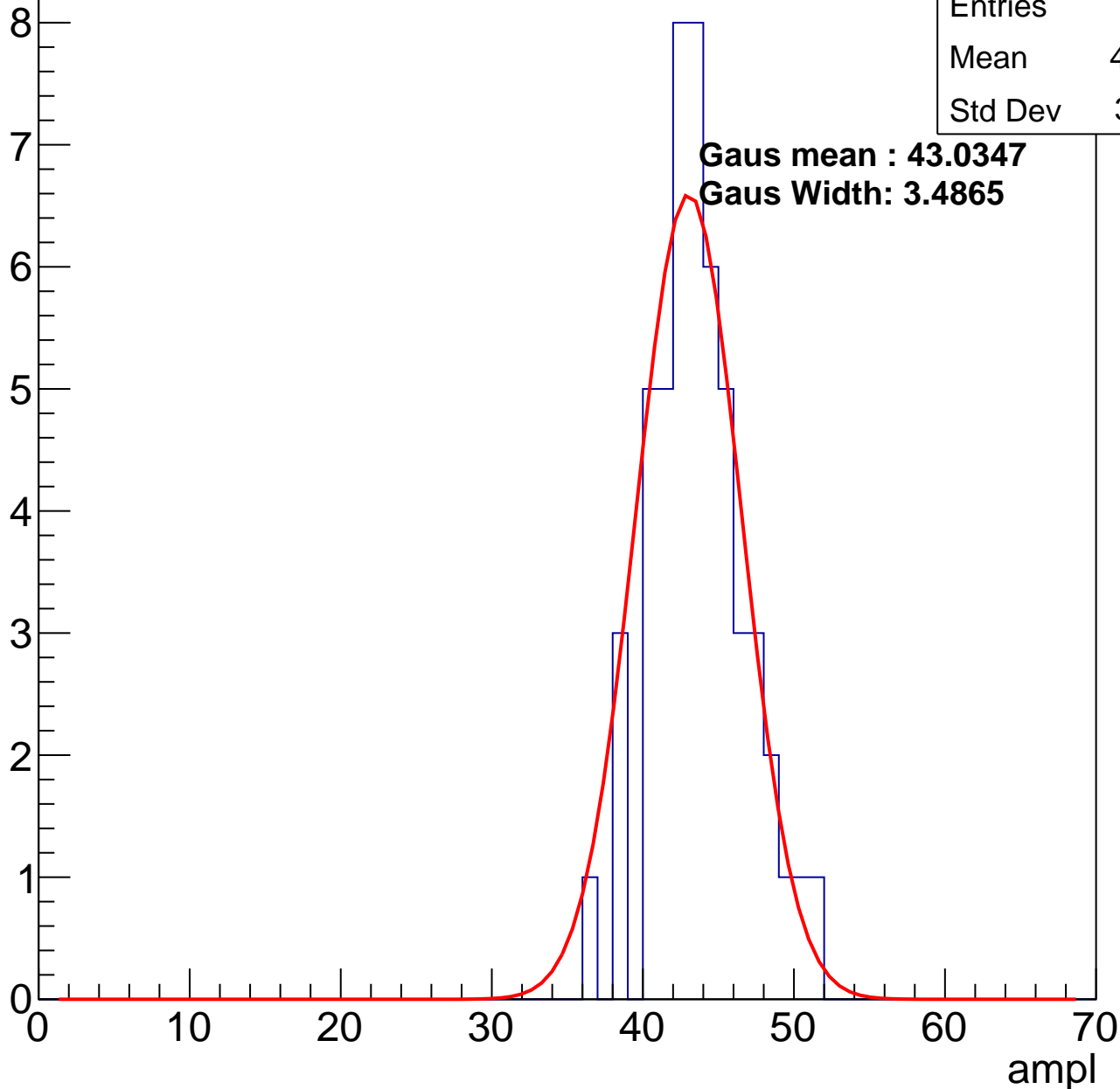
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	43.25
Std Dev	3.081

**Gaus mean : 43.0347**

**Gaus Width: 3.4865**

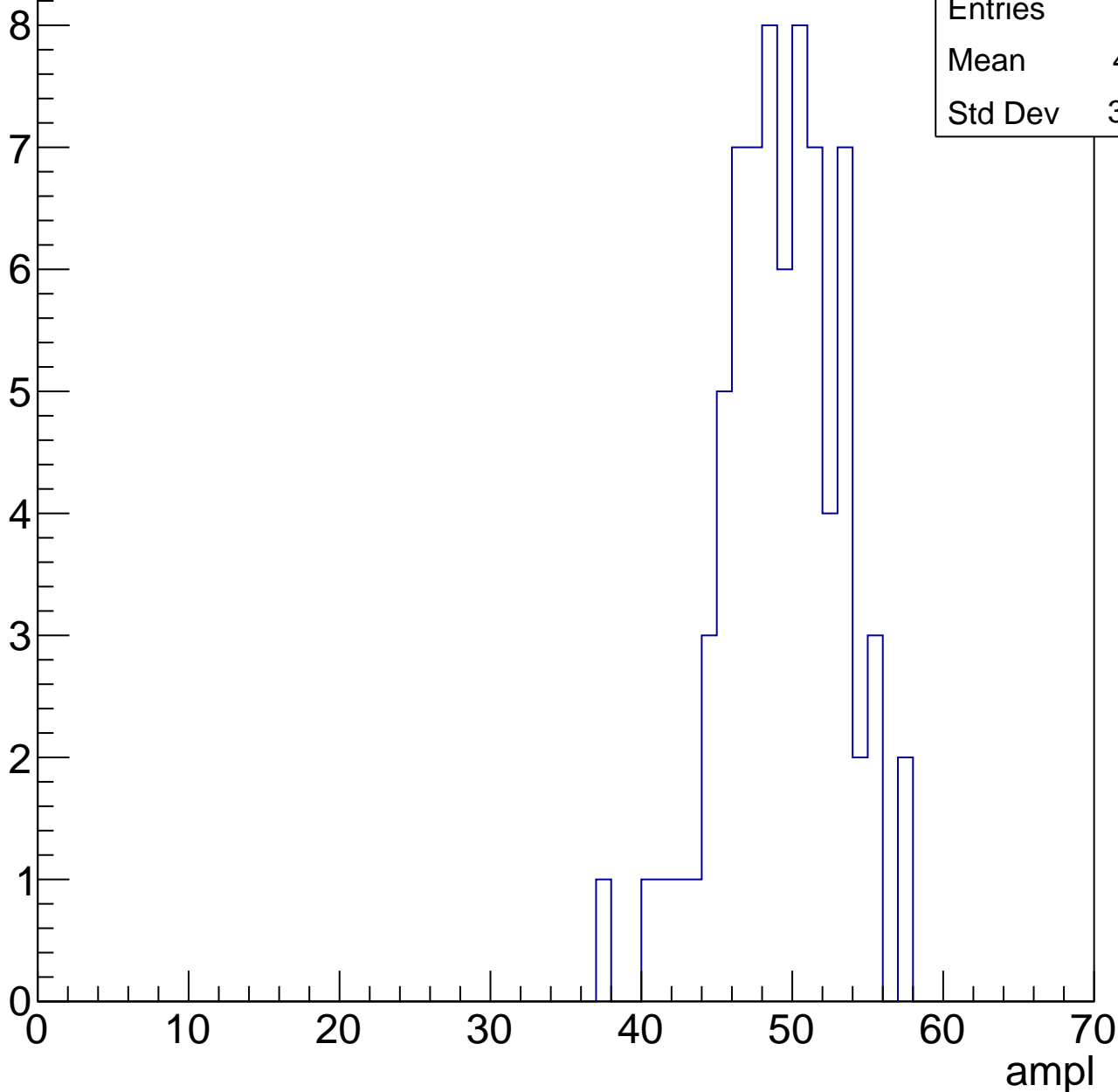


# B1L102S, U3-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

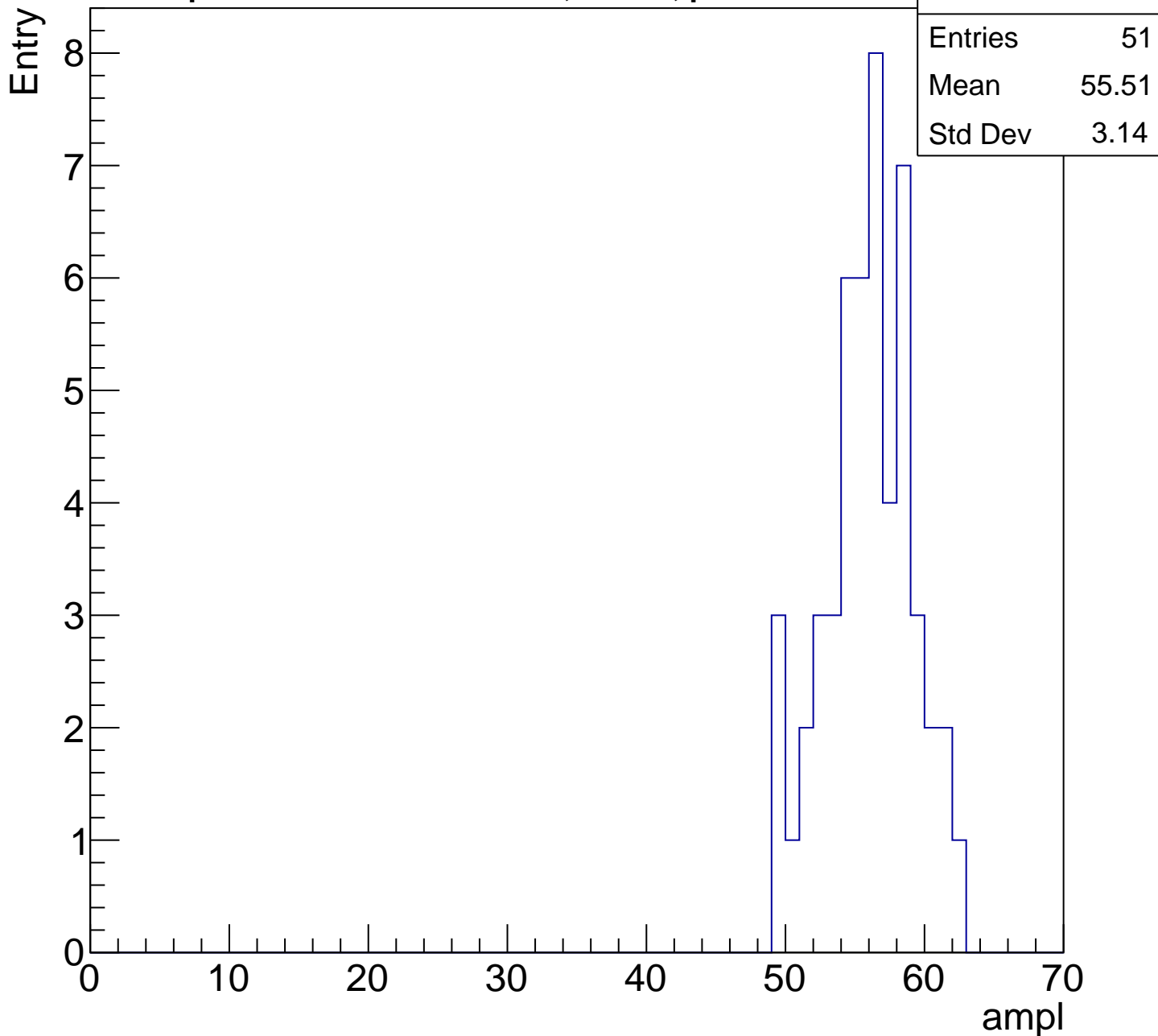
Entry

Entries	74
Mean	48.81
Std Dev	3.847



# B1L102S, U3-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U3-ch48, adc5

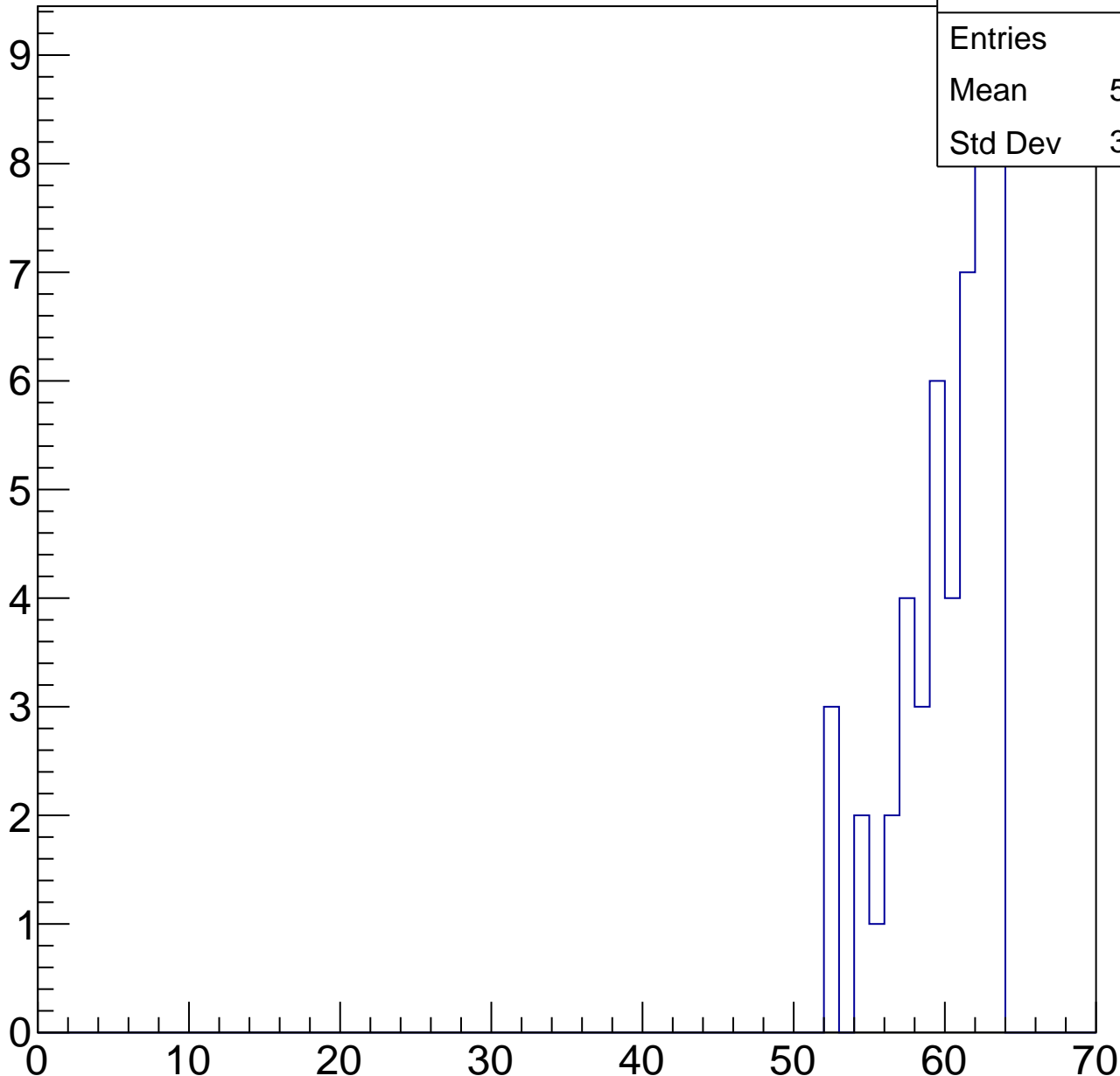
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	59.53
Std Dev	3.144

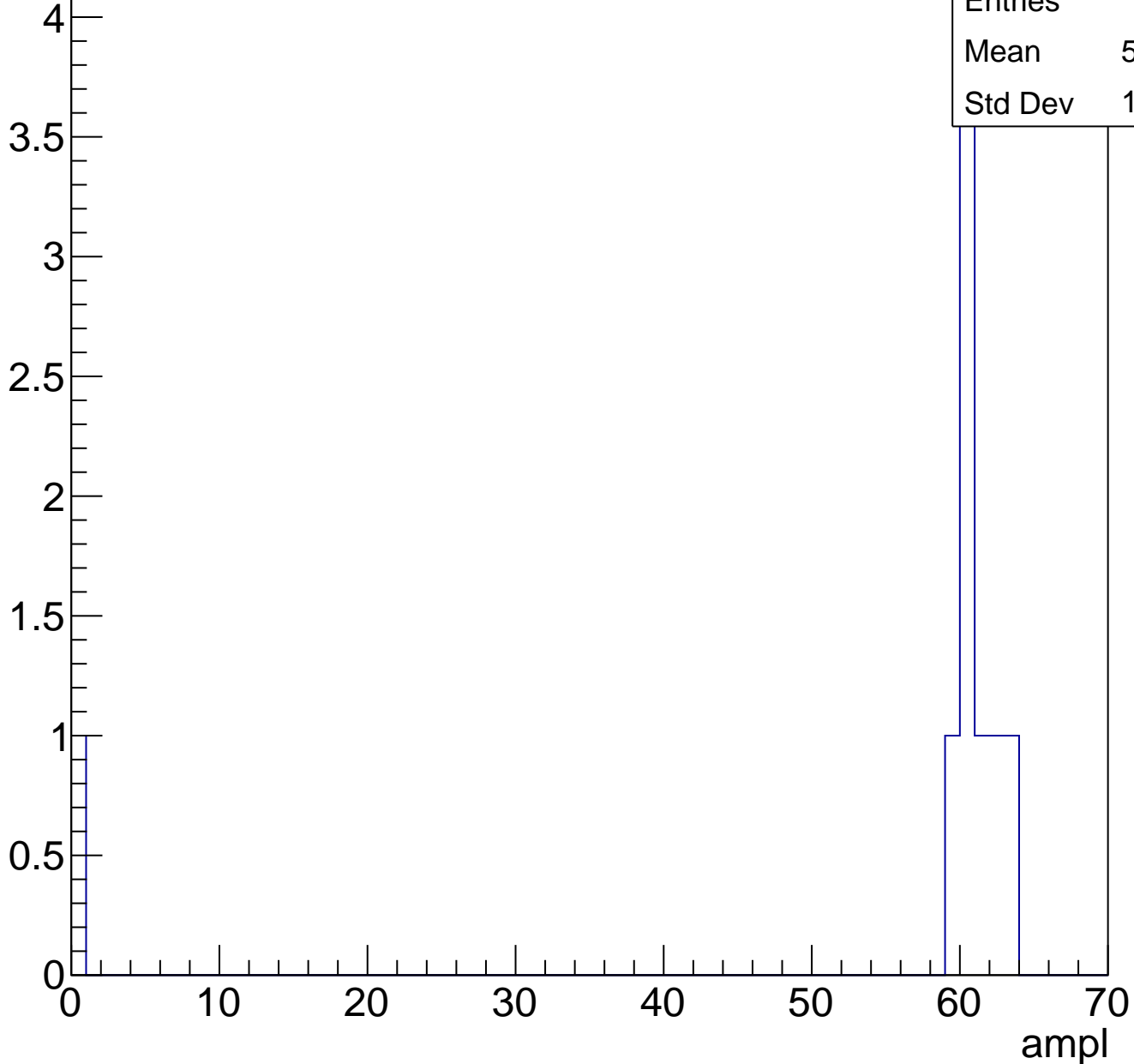
ampl



# B1L102S, U3-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U3-ch49, adc0

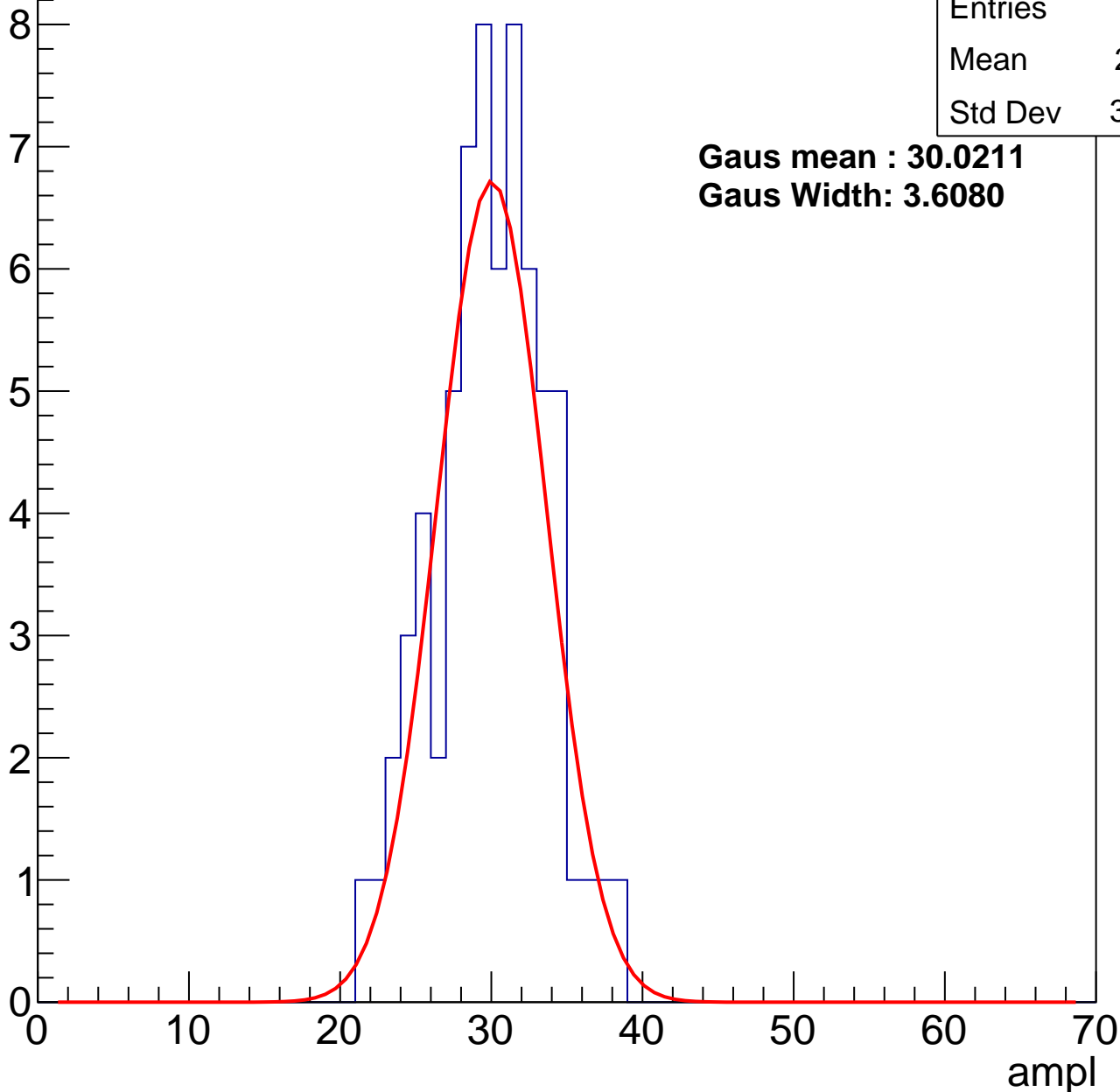
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	29.51
Std Dev	3.622

**Gaus mean : 30.0211**

**Gaus Width: 3.6080**



# B1L102S, U3-ch49, adc1

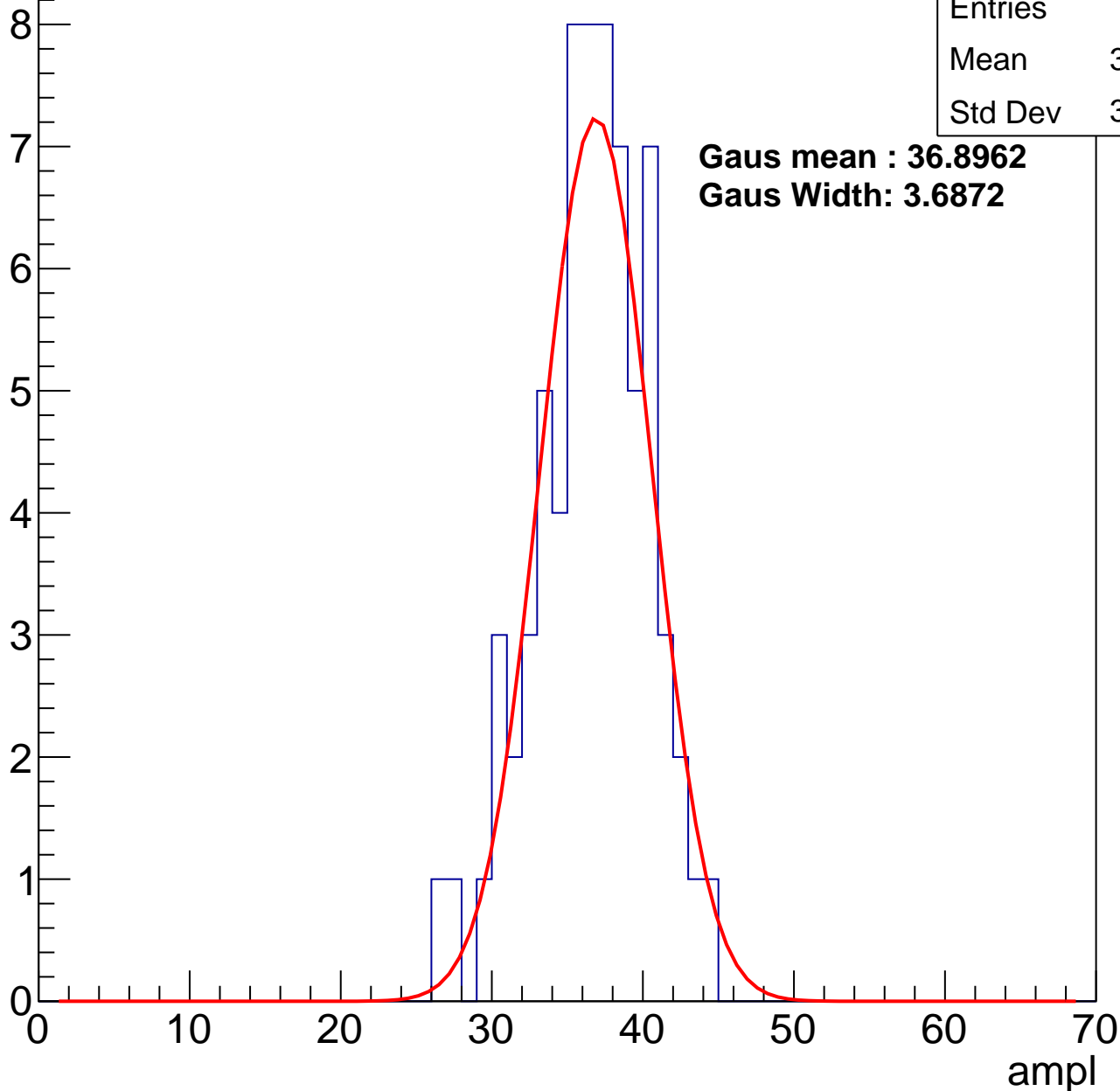
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	36.14
Std Dev	3.697

**Gaus mean : 36.8962**

**Gaus Width: 3.6872**



# B1L102S, U3-ch49, adc2

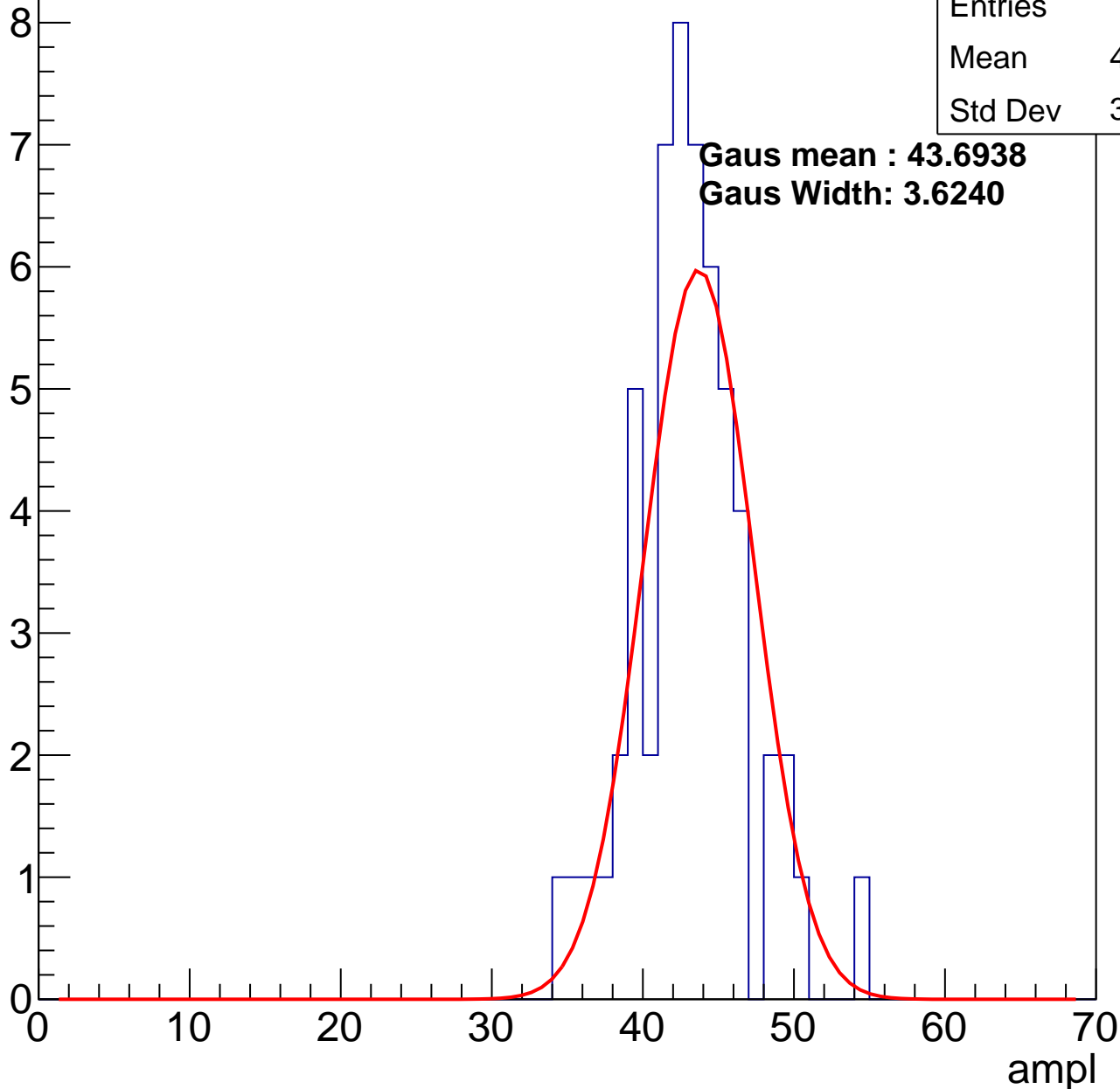
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	42.64
Std Dev	3.686

**Gaus mean : 43.6938**

**Gaus Width: 3.6240**

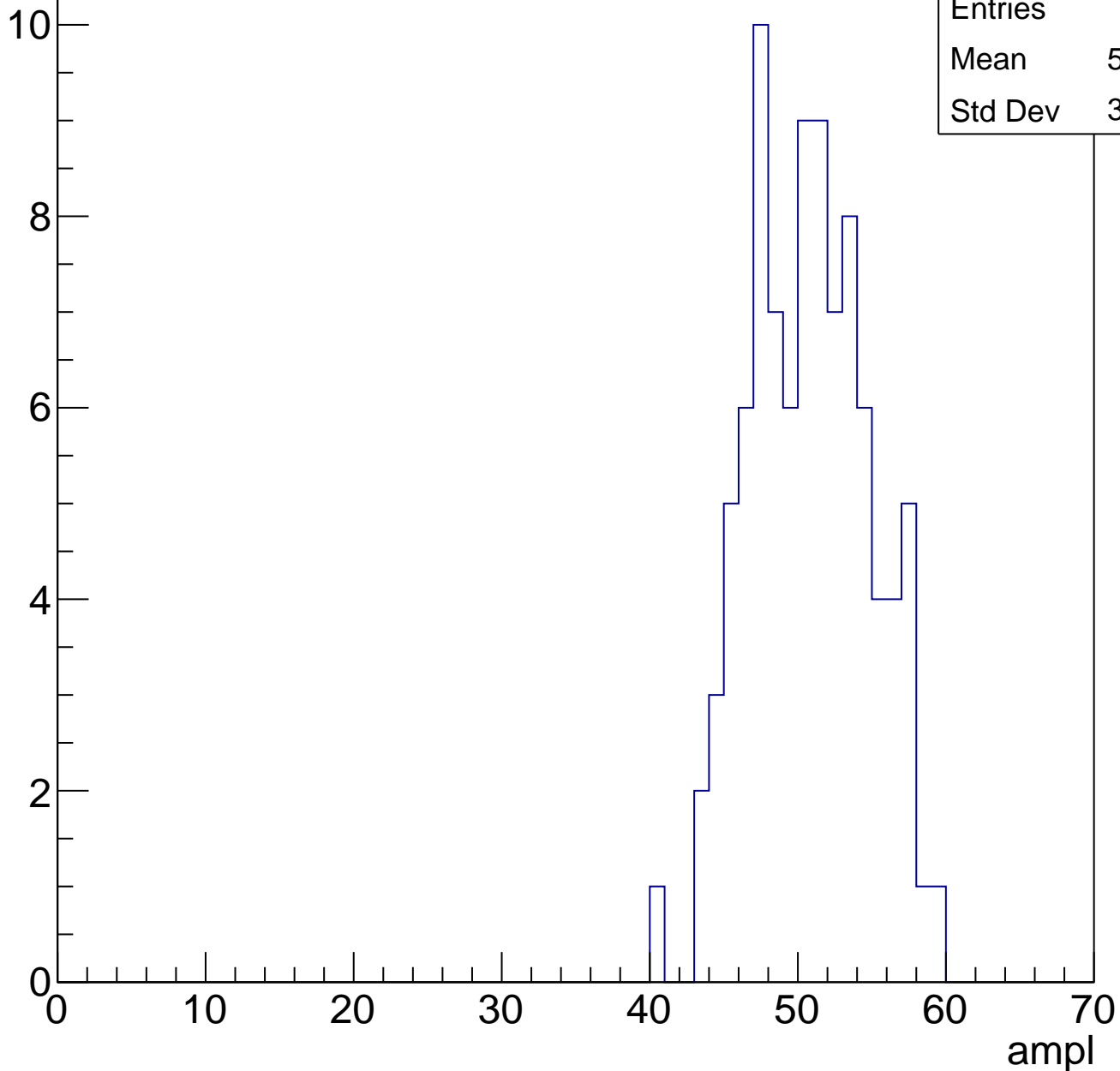


# B1L102S, U3-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	94
Mean	50.28
Std Dev	3.972

Entry



# B1L102S, U3-ch49, adc4

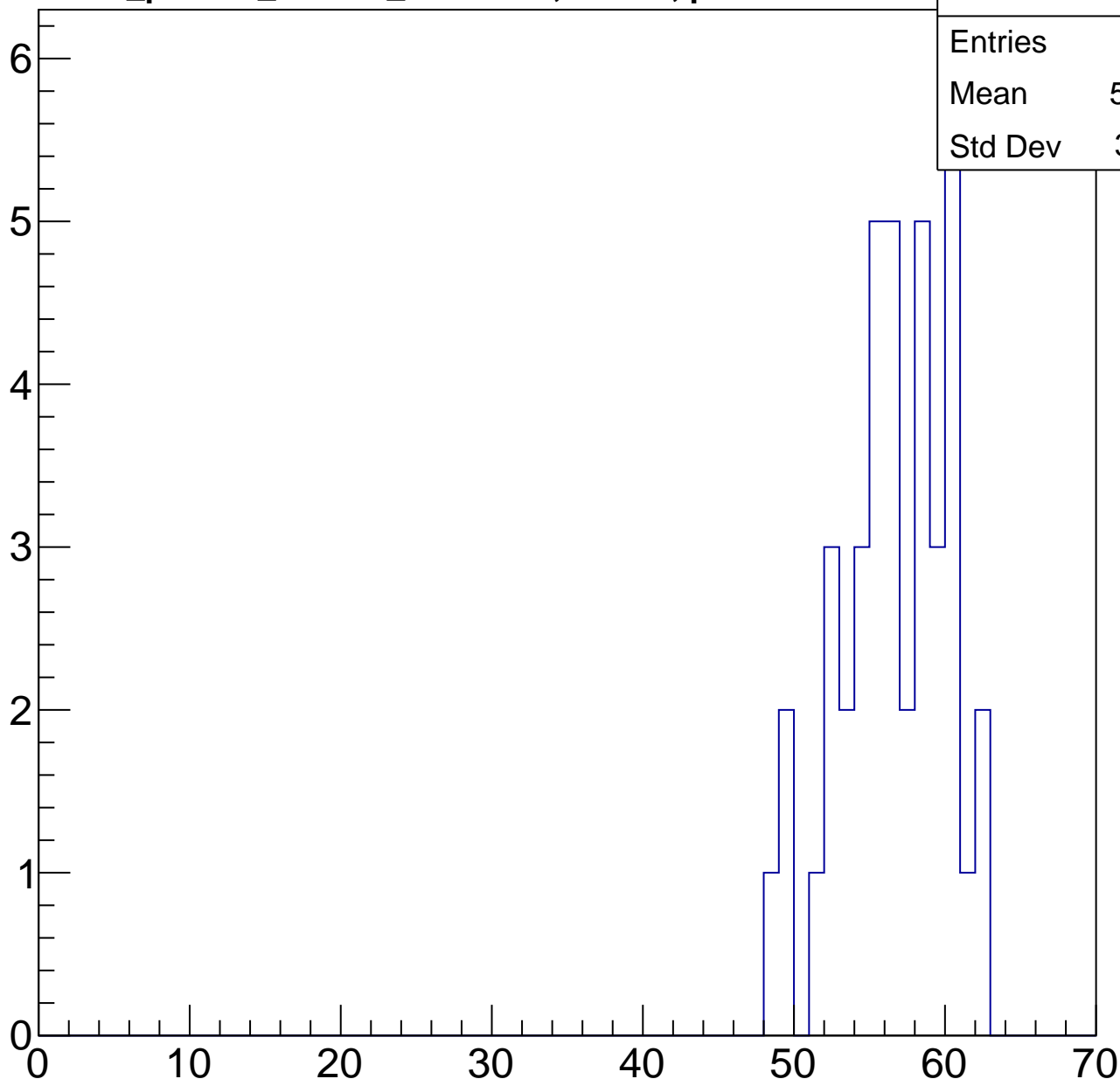
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

6  
5  
4  
3  
2  
1  
0

Entries	41
Mean	56.15
Std Dev	3.531

ampl



# B1L102S, U3-ch49, adc5

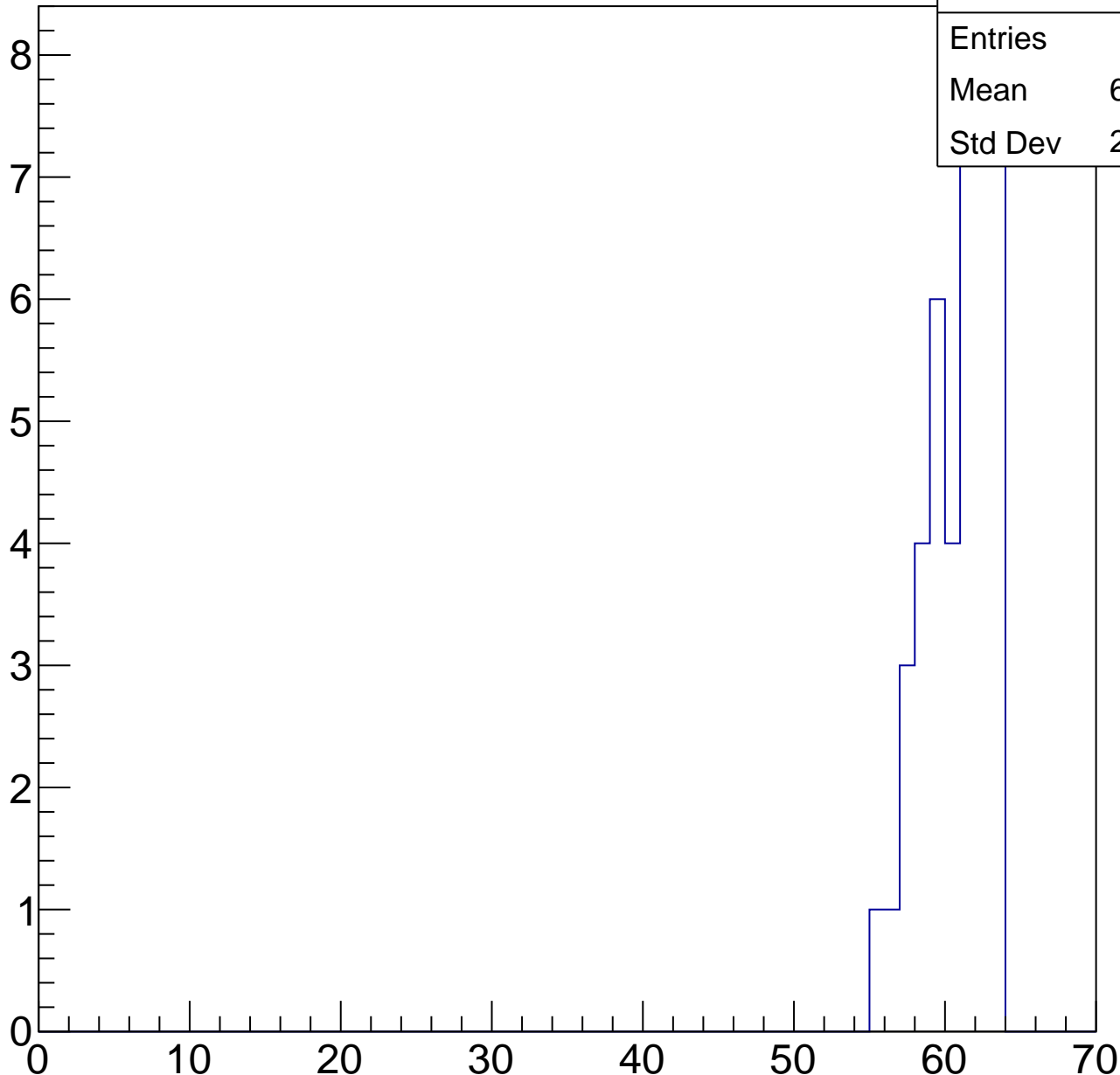
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	43
Mean	60.37
Std Dev	2.135

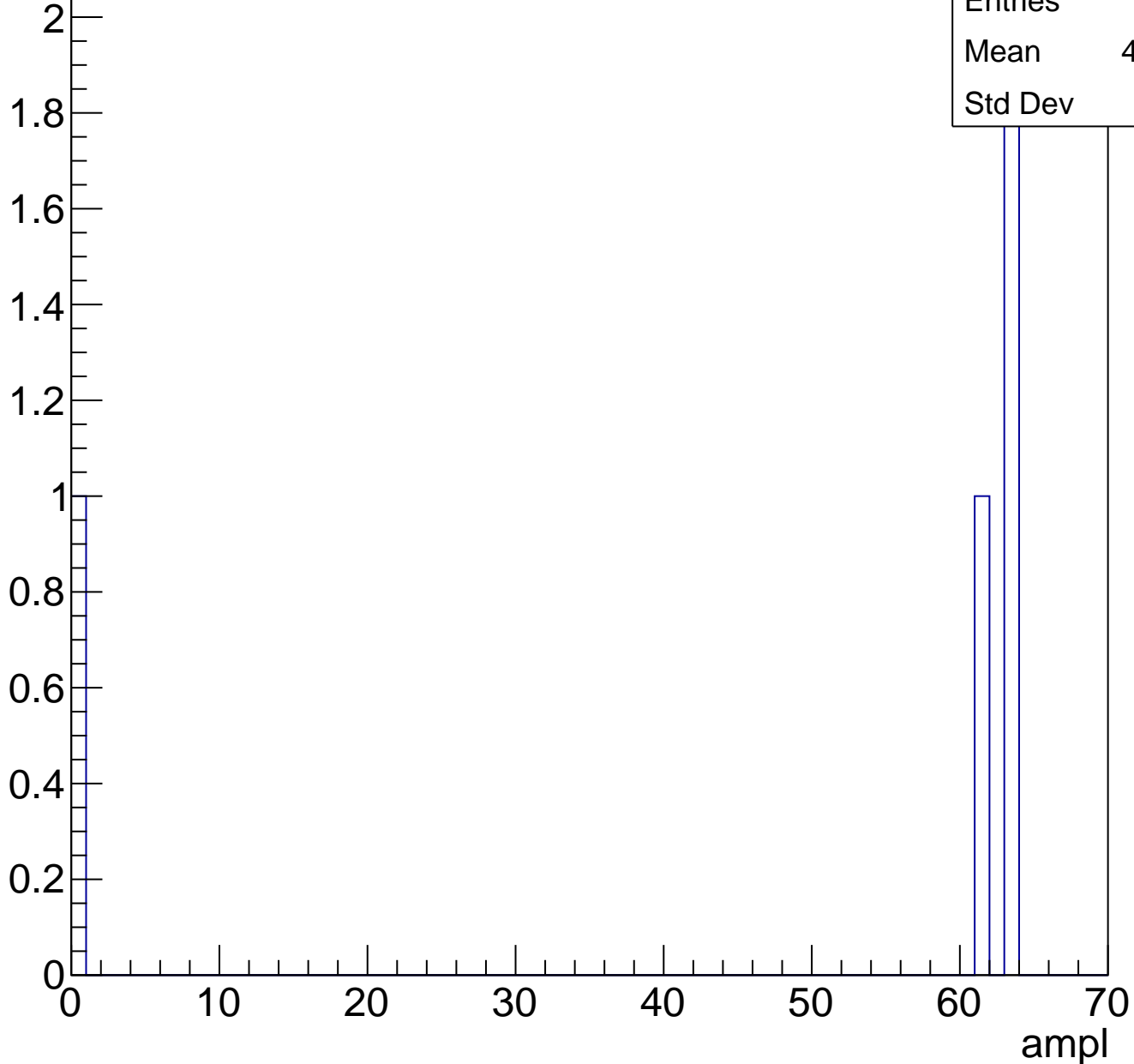
ampl



# B1L102S, U3-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch50, adc0

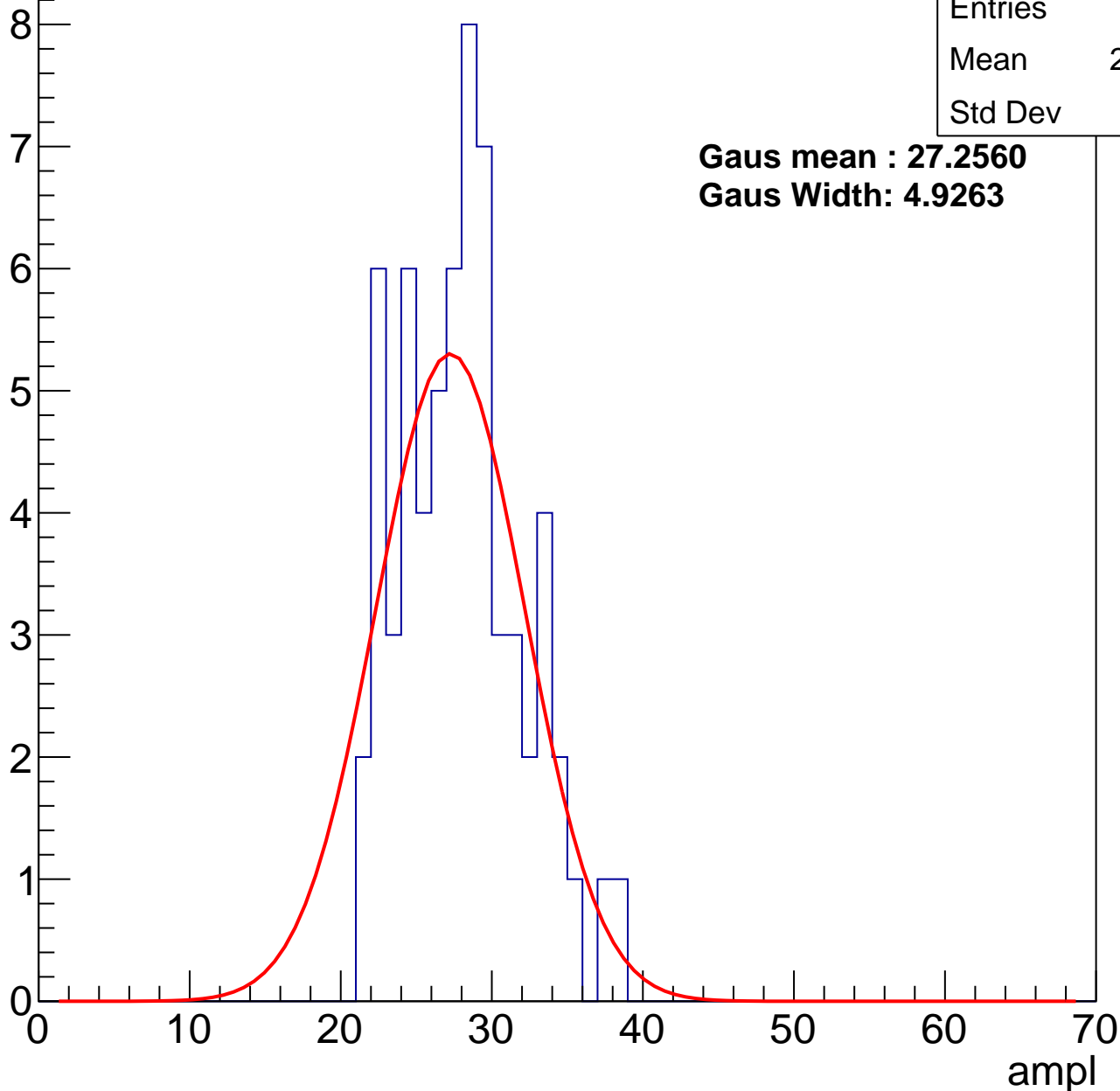
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	27.55
Std Dev	3.98

**Gaus mean : 27.2560**

**Gaus Width: 4.9263**



# B1L102S, U3-ch50, adc1

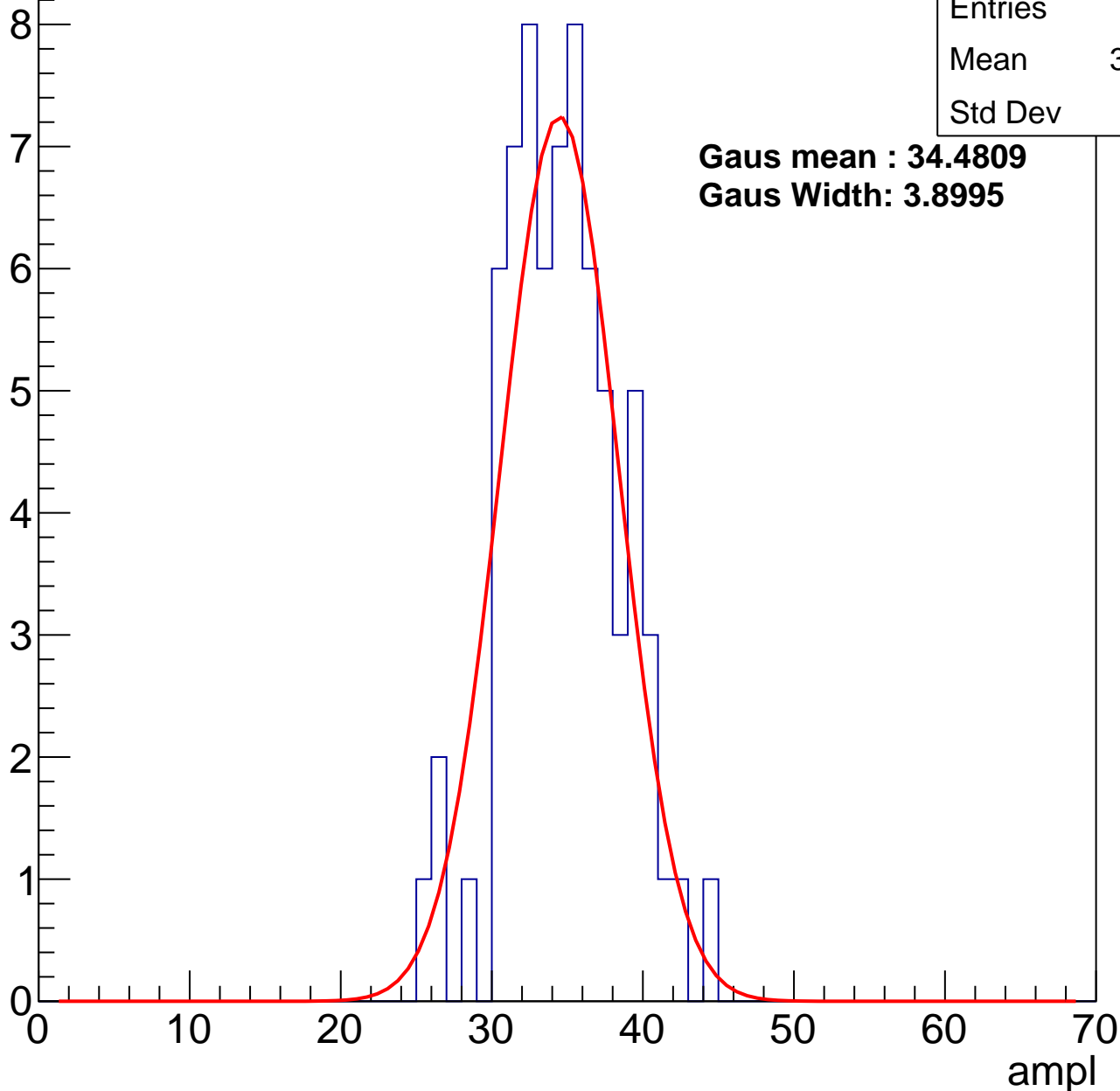
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	34.24
Std Dev	3.77

**Gaus mean : 34.4809**

**Gaus Width: 3.8995**



# B1L102S, U3-ch50, adc2

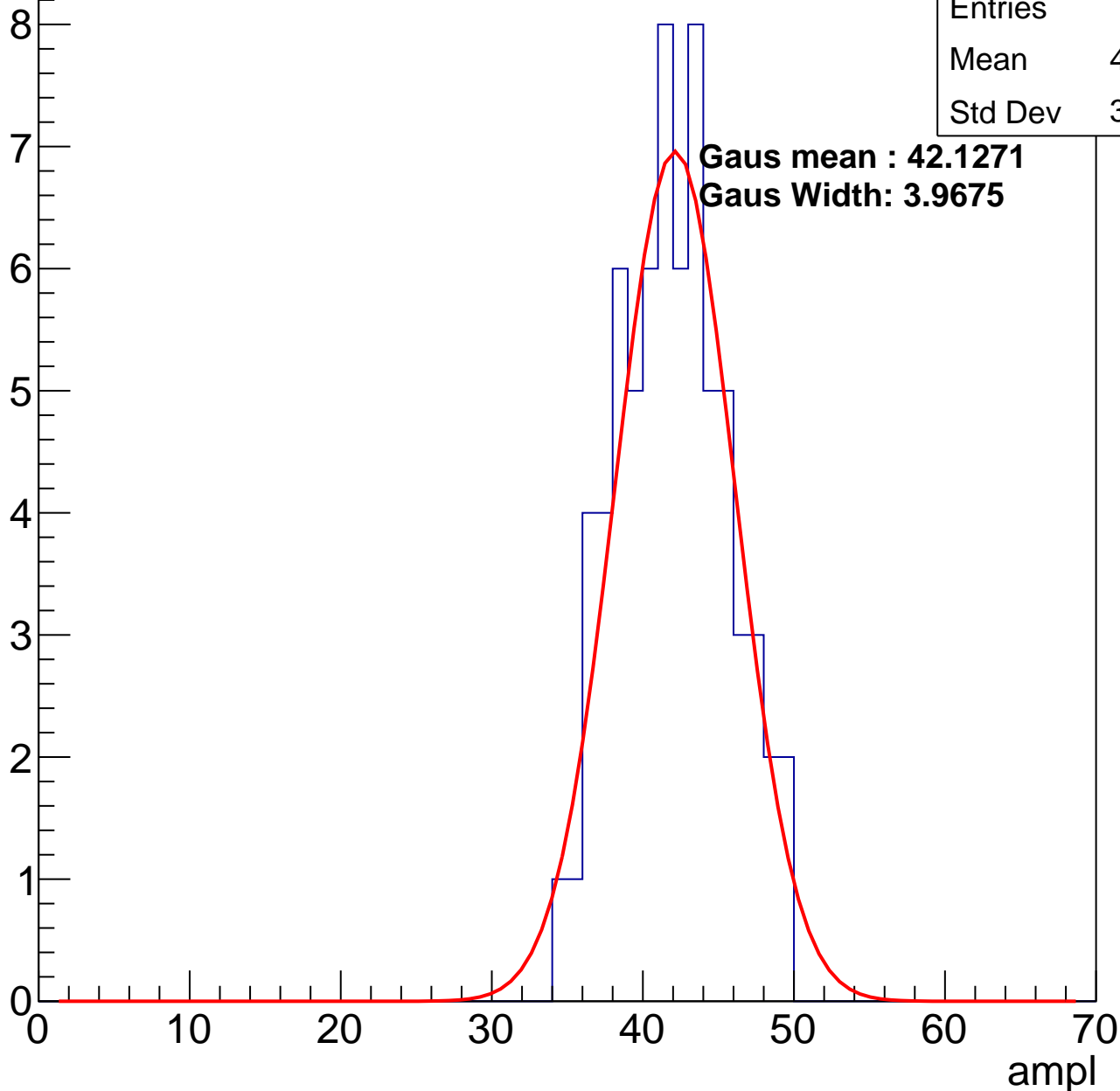
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	41.54
Std Dev	3.574

**Gaus mean : 42.1271**

**Gaus Width: 3.9675**

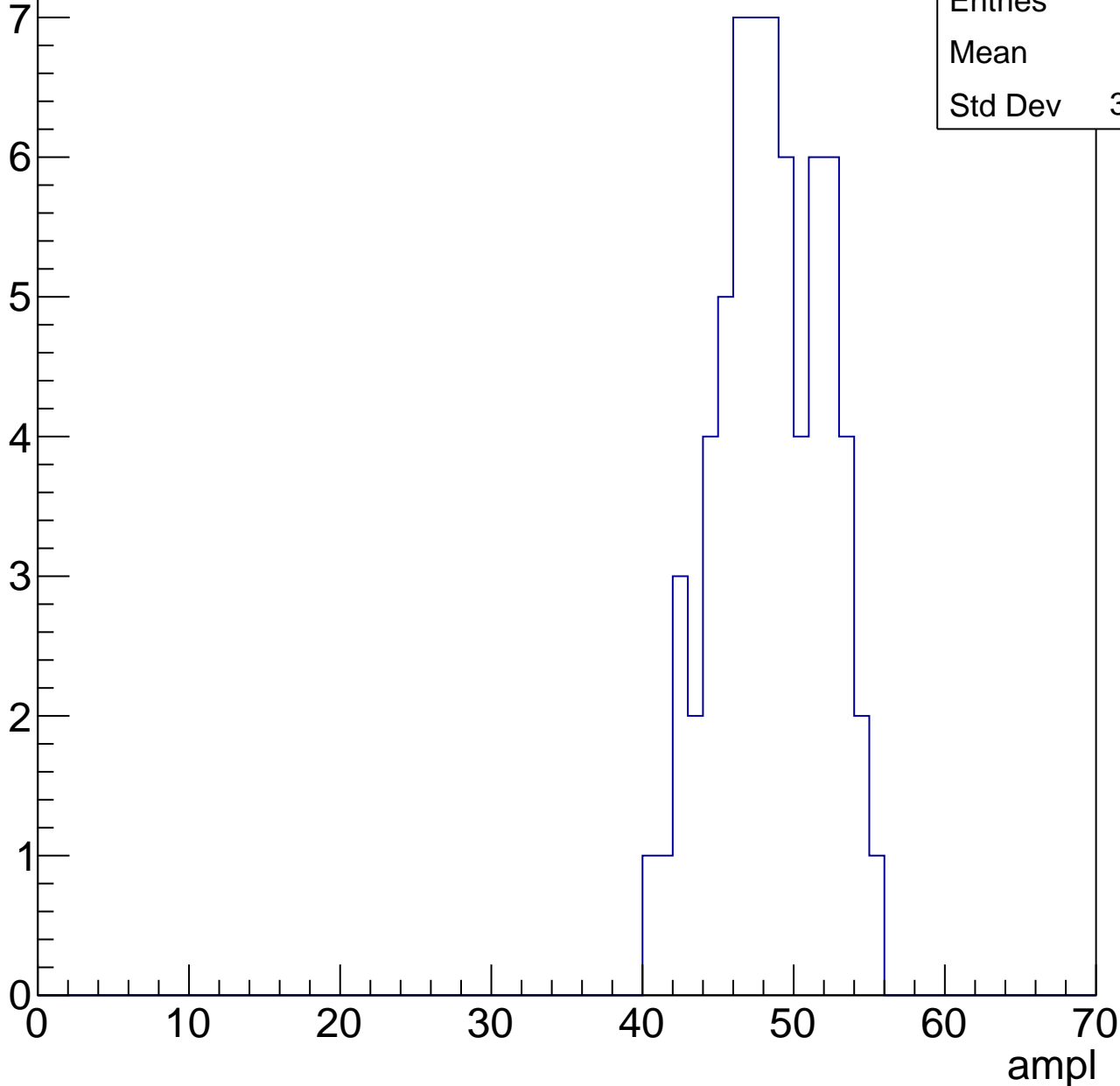


# B1L102S, U3-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	48
Std Dev	3.499

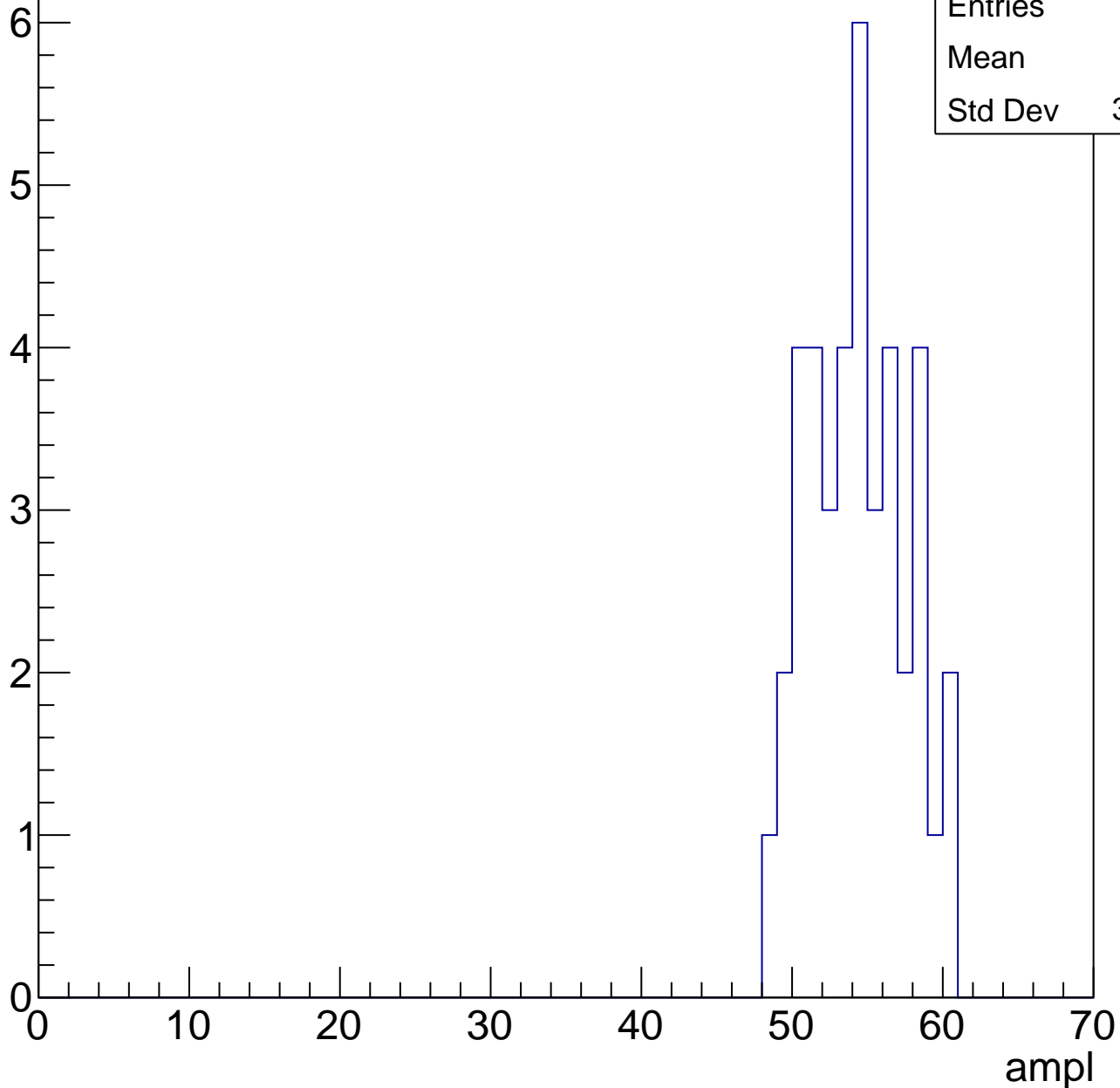


# B1L102S, U3-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

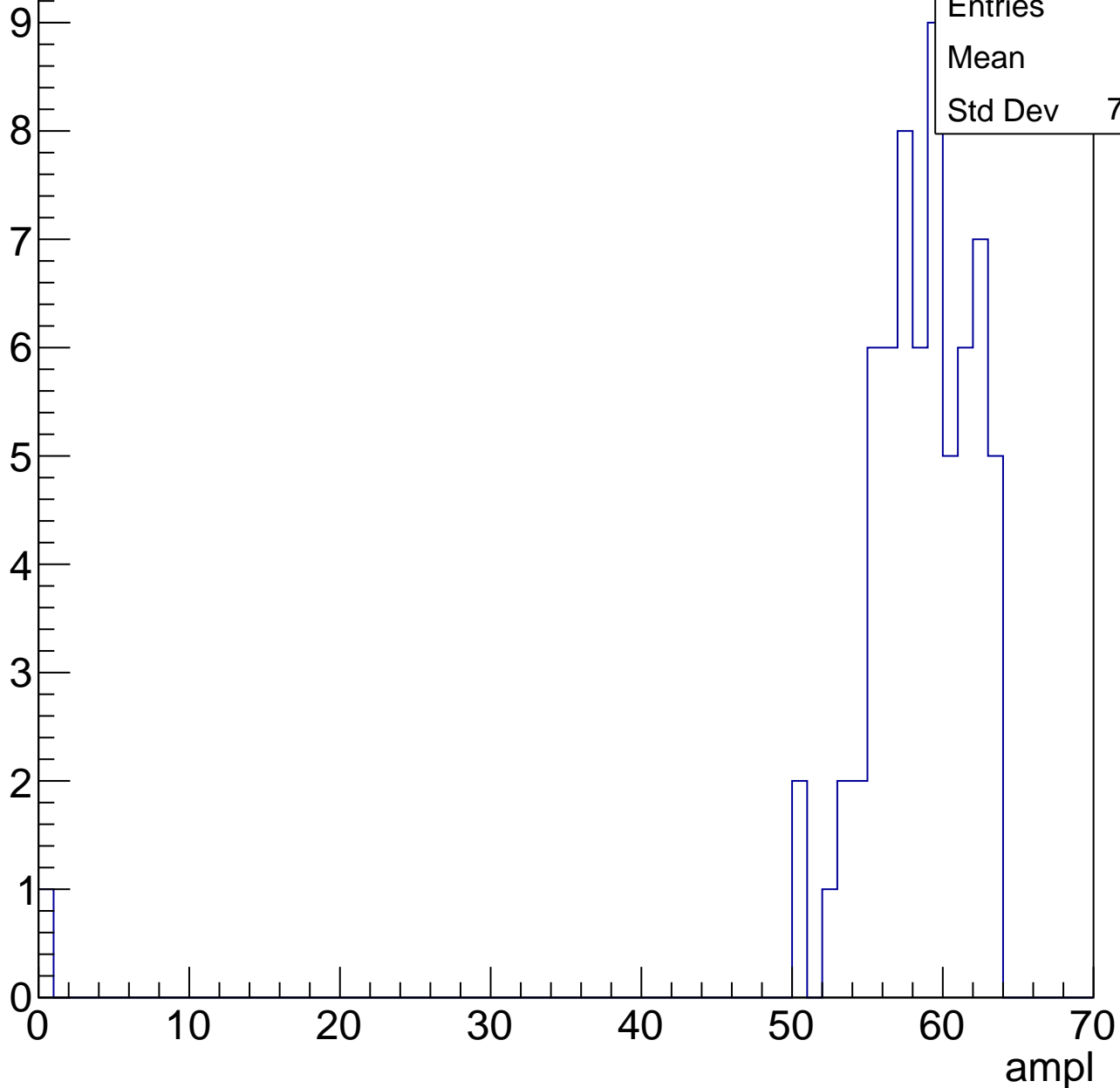
Entries	40
Mean	53.9
Std Dev	3.161



# B1L102S, U3-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

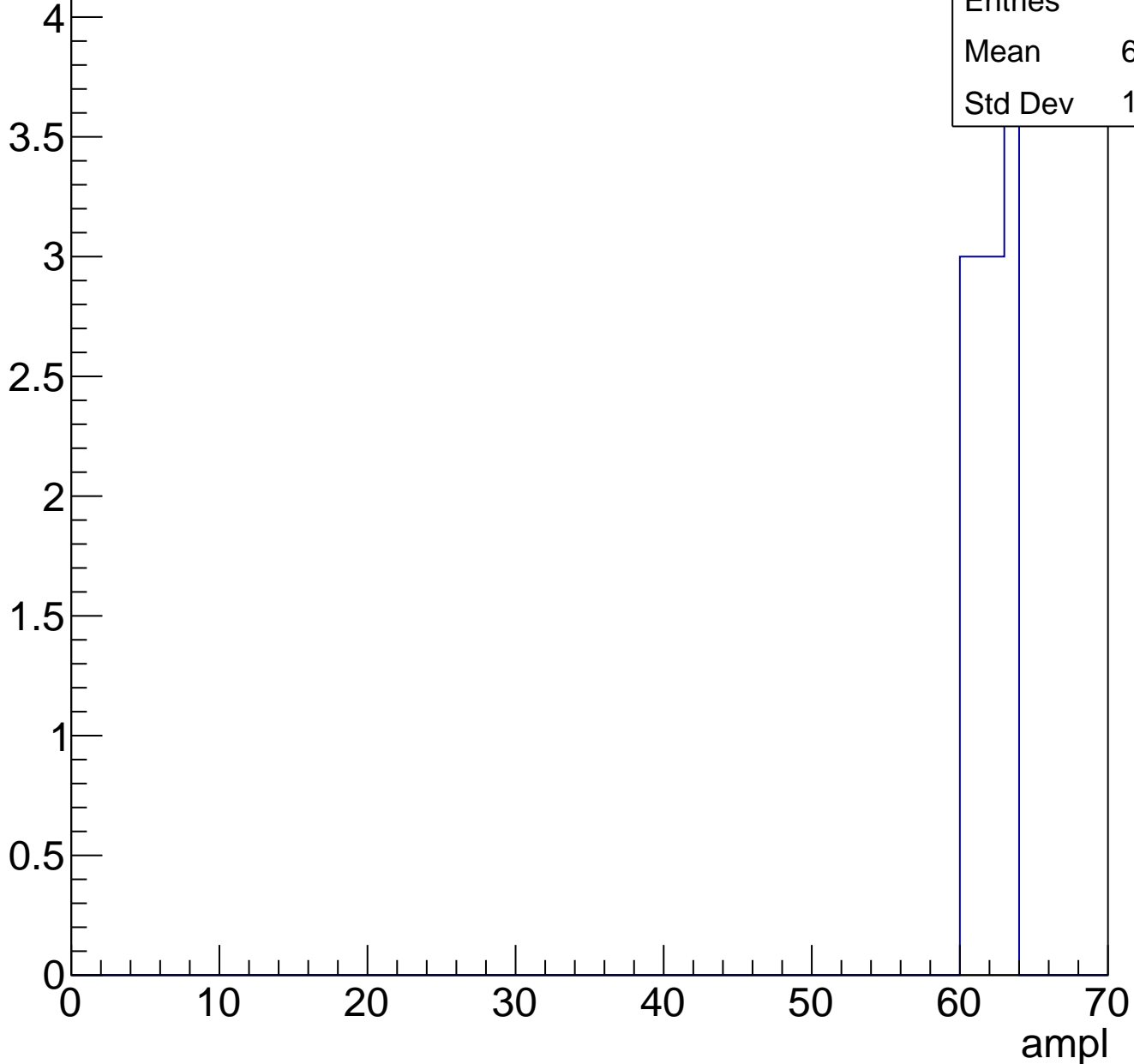
Entry



# B1L102S, U3-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

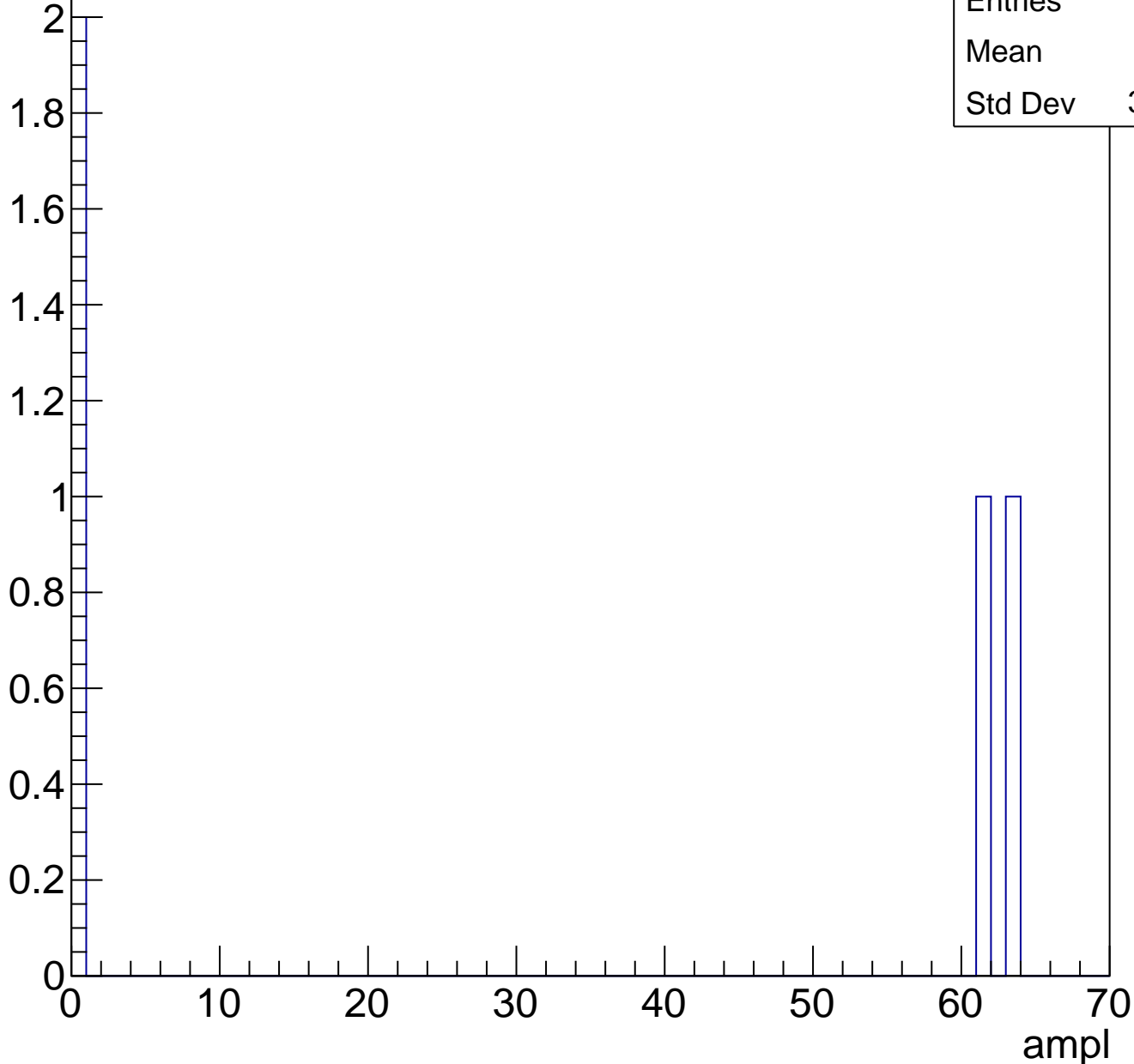




# B1L102S, U3-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch51, adc0

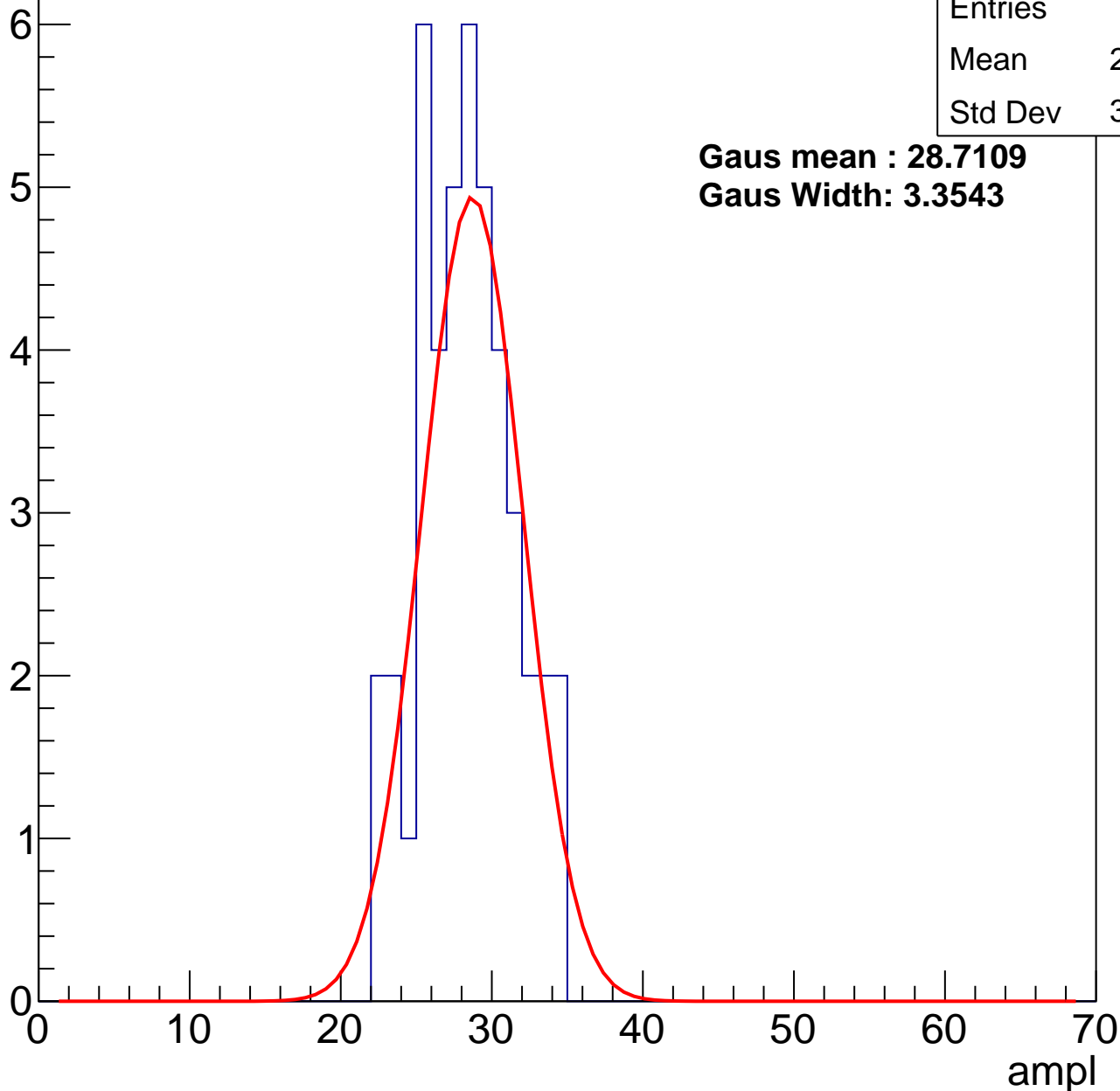
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	44
Mean	27.89
Std Dev	3.069

**Gaus mean : 28.7109**

**Gaus Width: 3.3543**



# B1L102S, U3-ch51, adc1

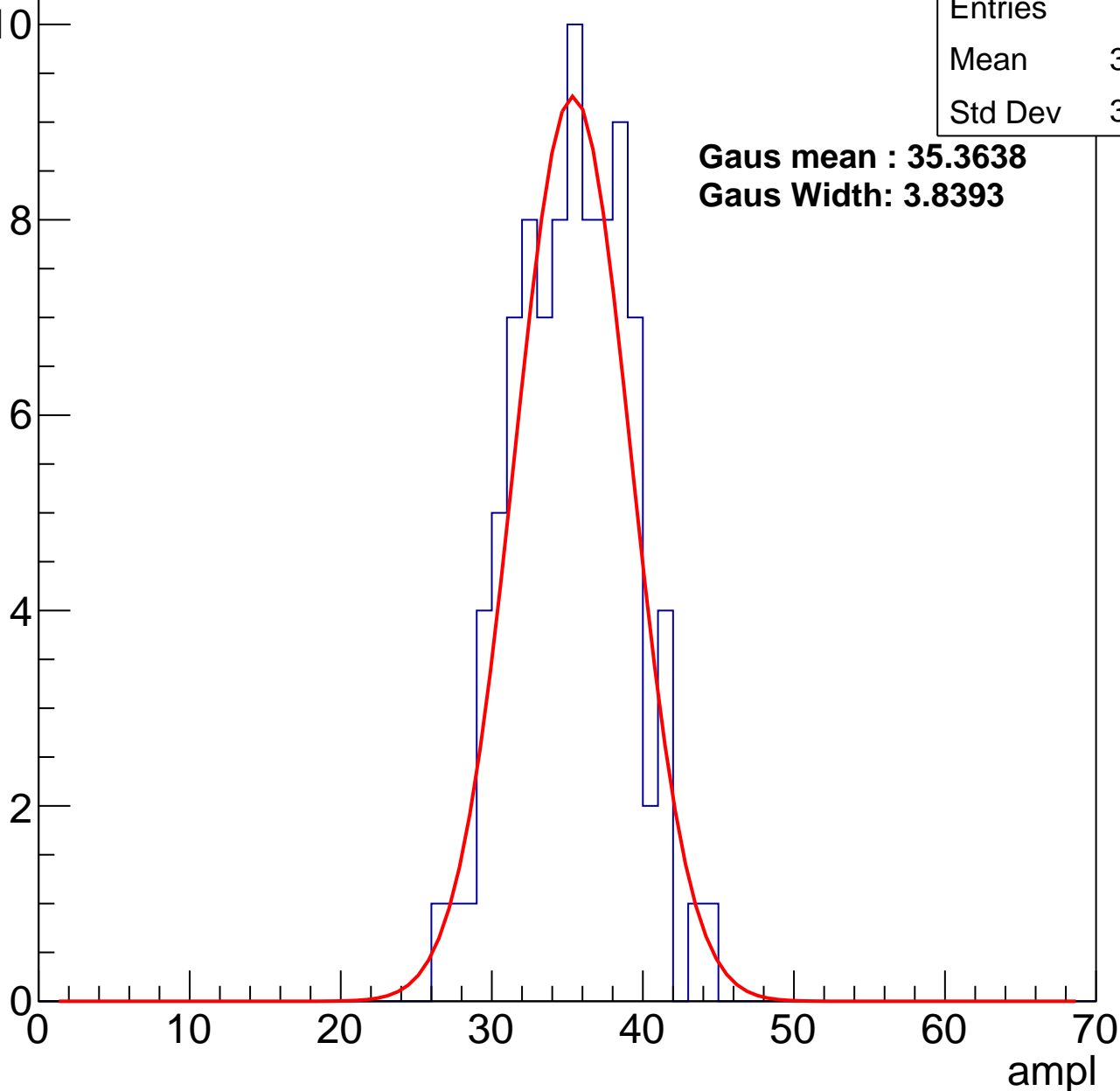
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	92
Mean	34.82
Std Dev	3.689

**Gaus mean : 35.3638**

**Gaus Width: 3.8393**



# B1L102S, U3-ch51, adc2

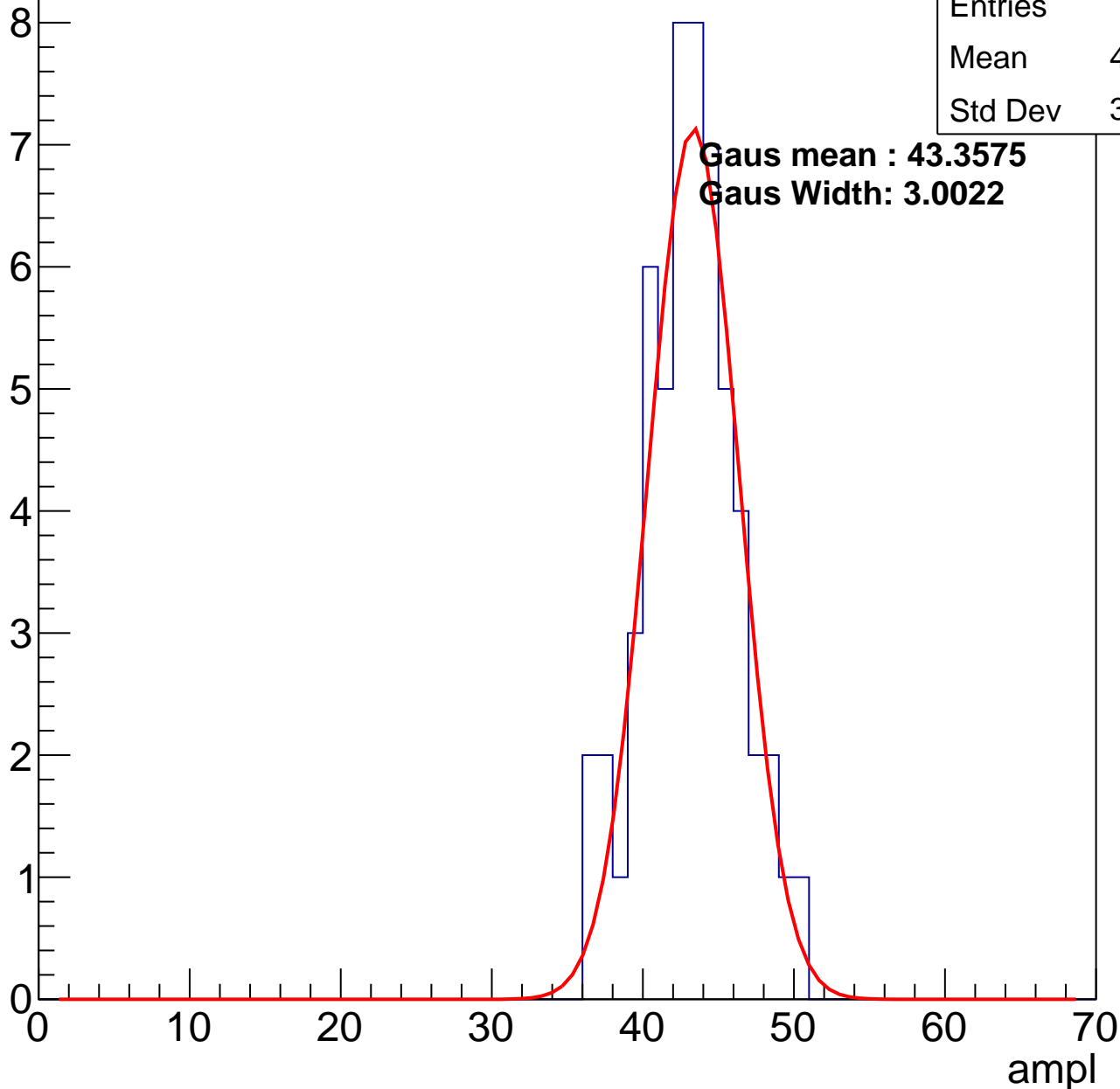
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	42.67
Std Dev	3.103

**Gaus mean : 43.3575**

**Gaus Width: 3.0022**

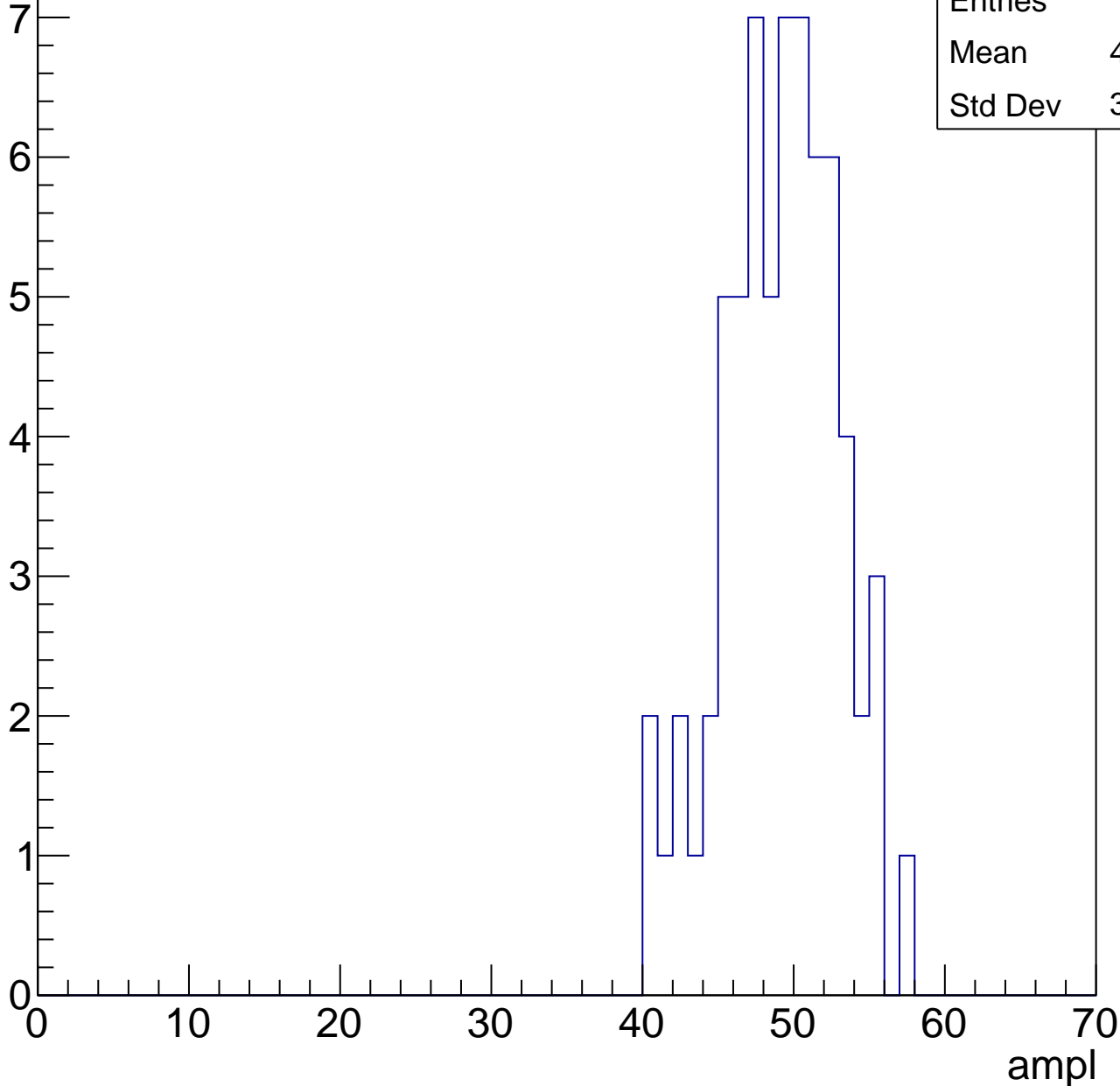


# B1L102S, U3-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	48.68
Std Dev	3.758



# B1L102S, U3-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

7

6

5

4

3

2

1

0

Entries 57

Mean 54.28

Std Dev 3.508

0

10

20

30

40

50

60

ampl

0

10

20

30

40

50

60

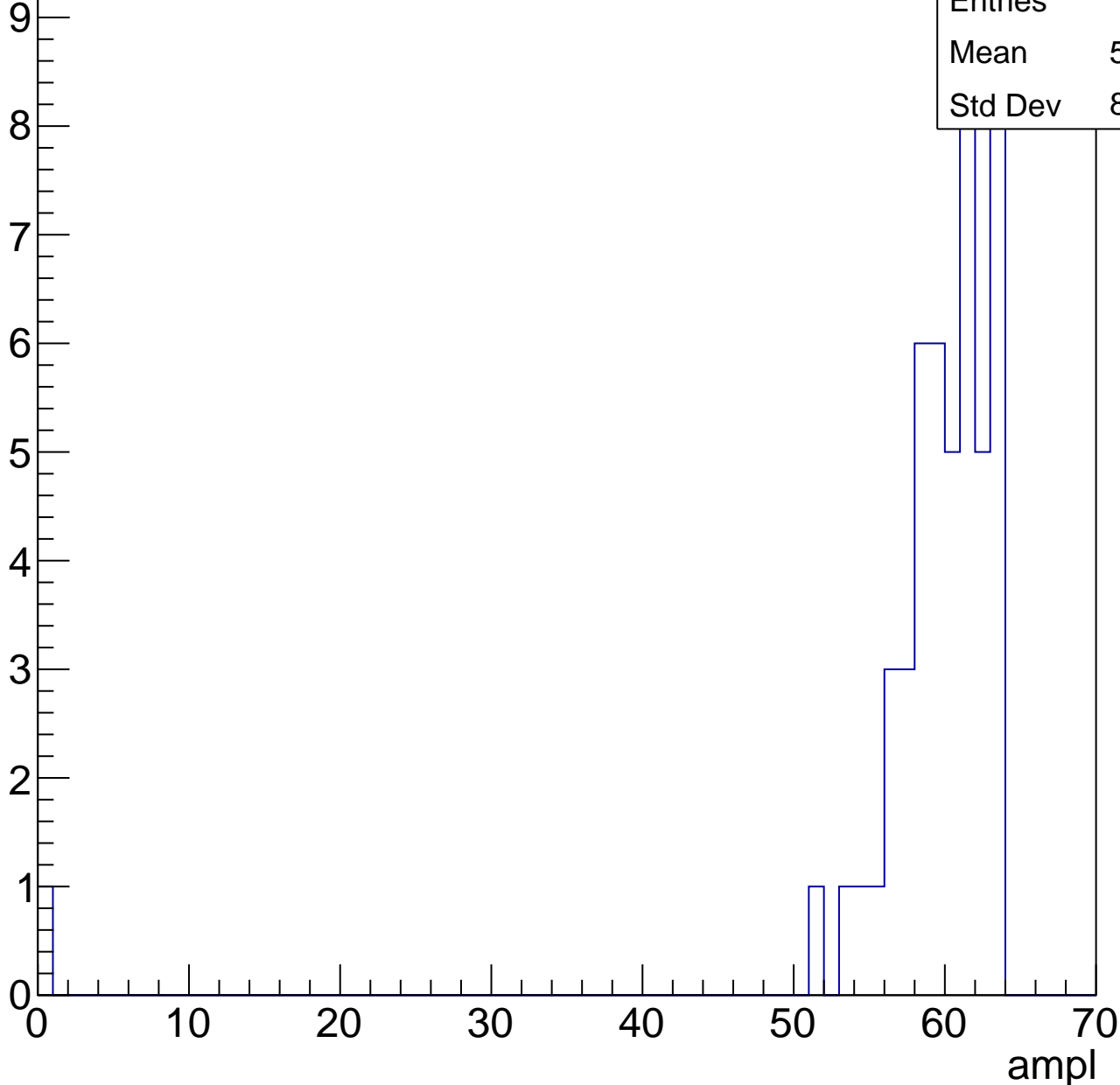
70

# B1L102S, U3-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	58.38
Std Dev	8.802

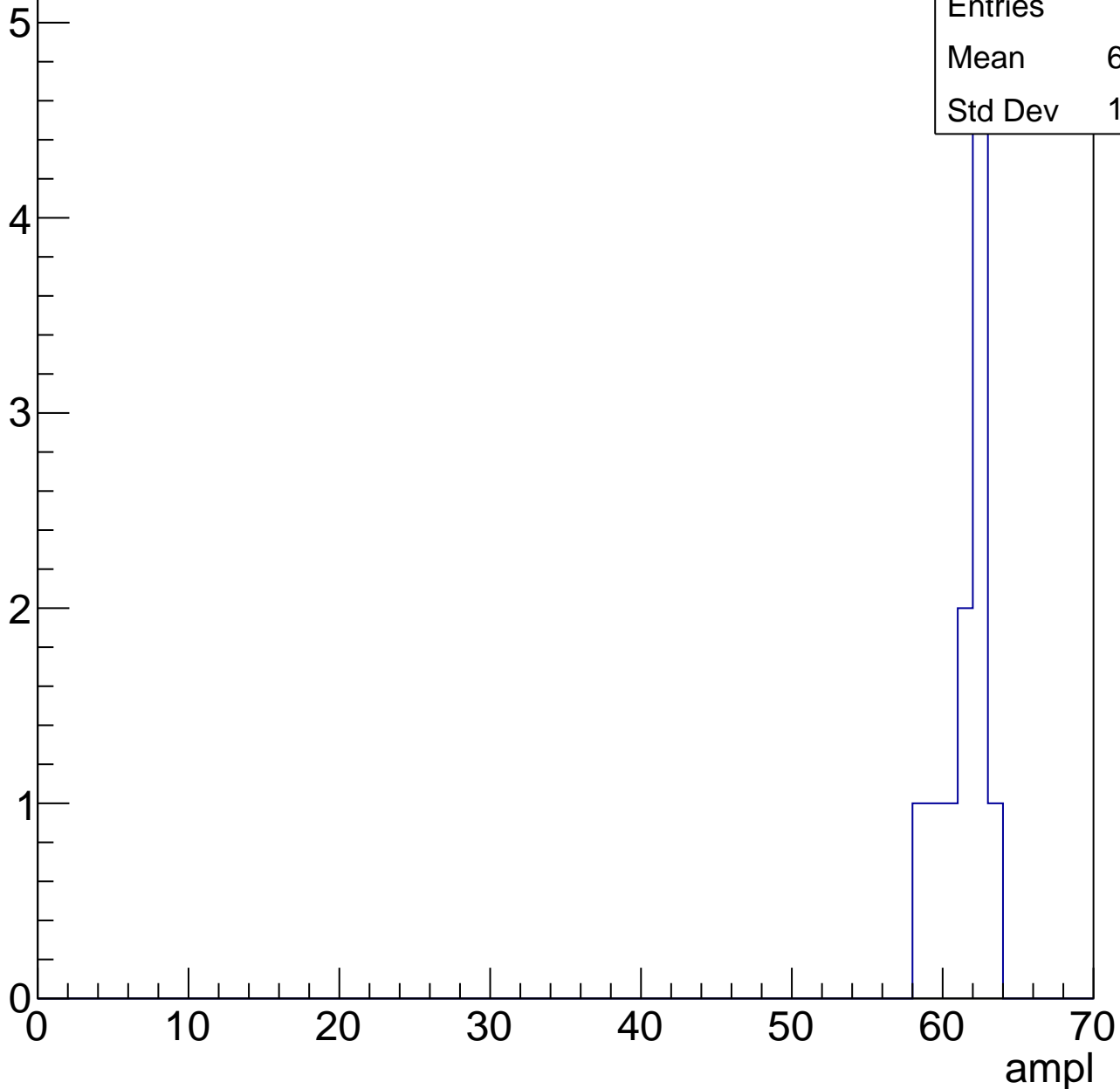


# B1L102S, U3-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	11
Mean	61.09
Std Dev	1.443





# B1L102S, U3-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U3-ch52, adc0

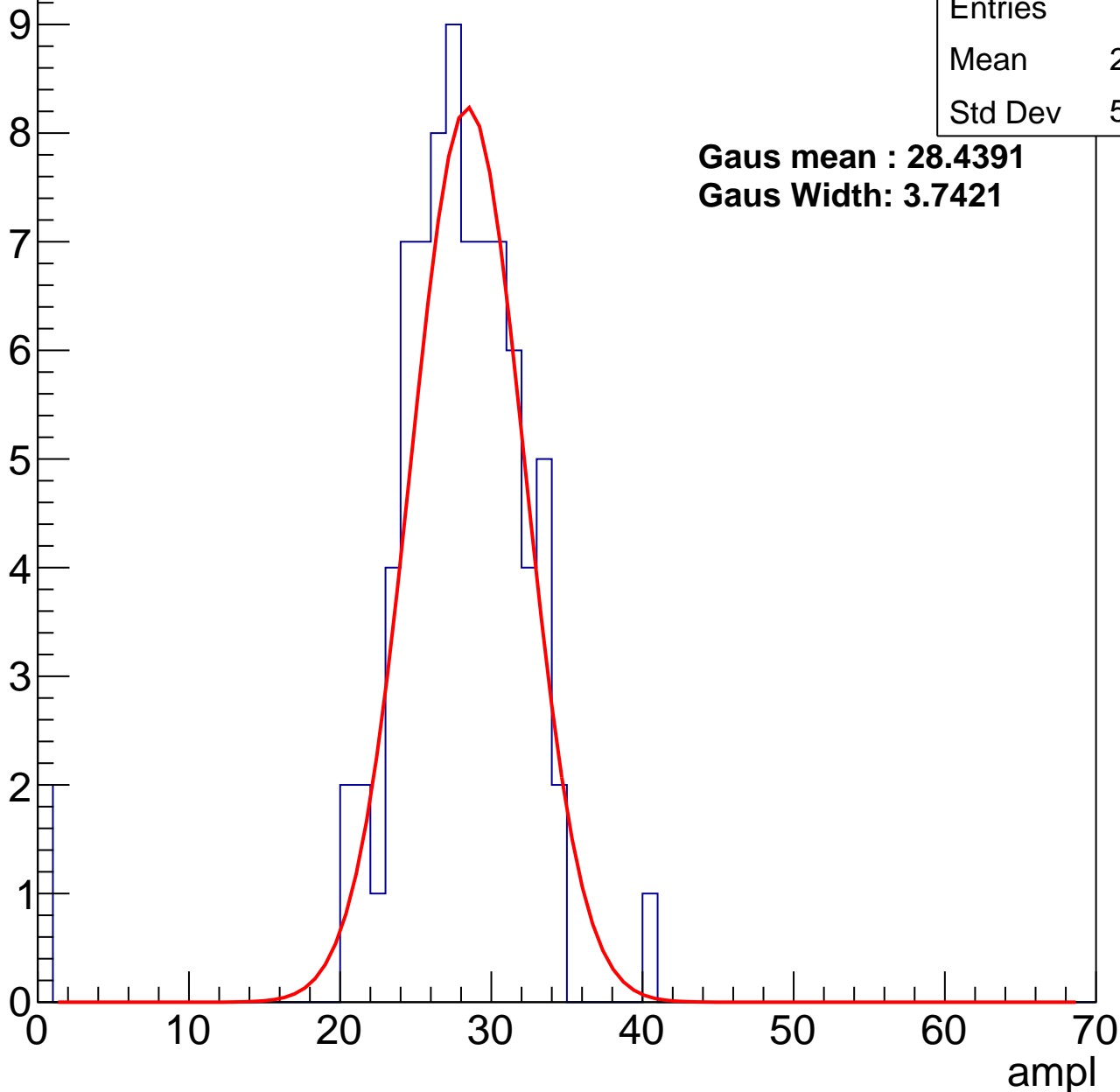
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	81
Mean	26.99
Std Dev	5.619

**Gaus mean : 28.4391**

**Gaus Width: 3.7421**



# B1L102S, U3-ch52, adc1

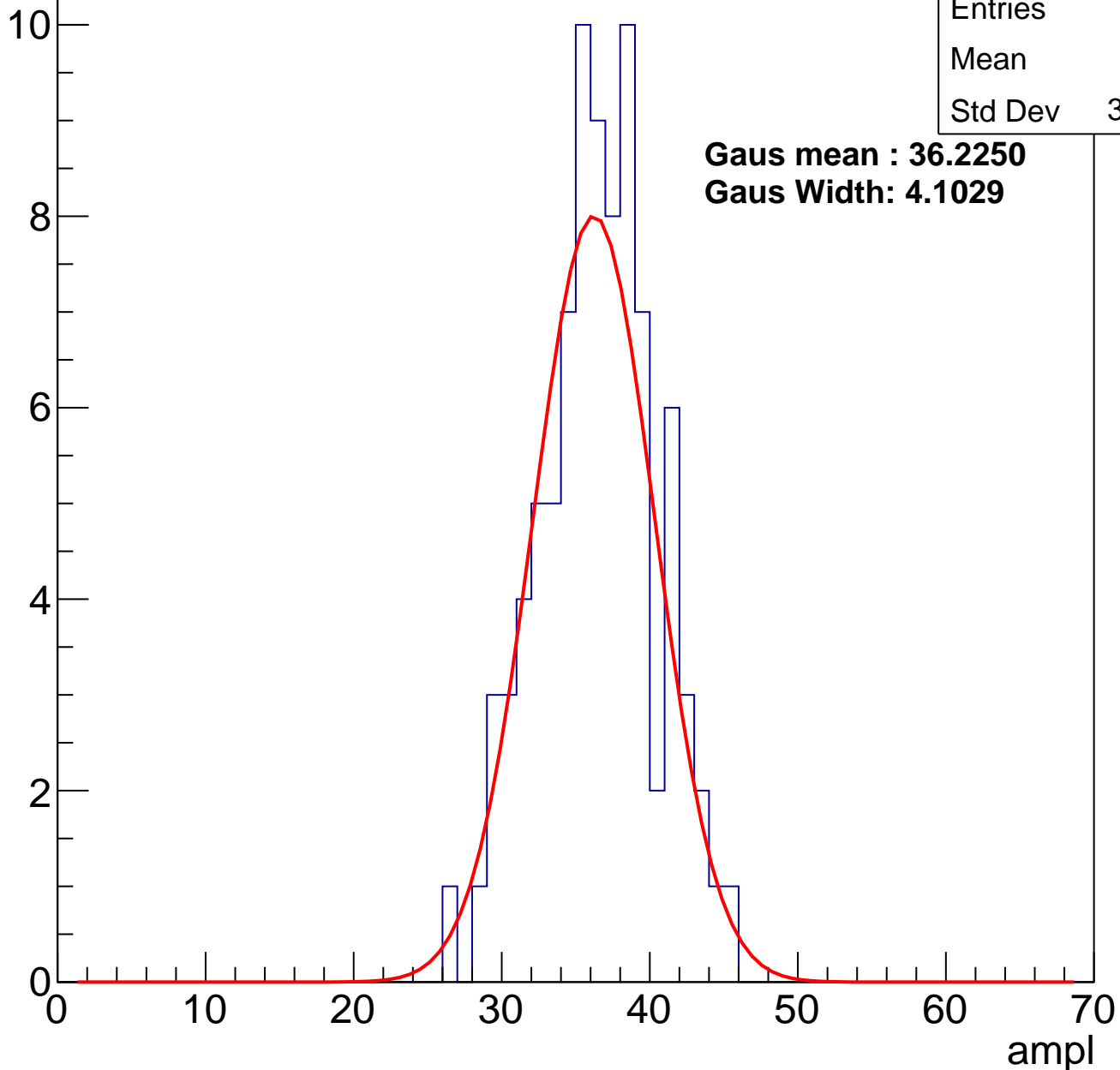
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	88
Mean	36
Std Dev	3.882

**Gaus mean : 36.2250**

**Gaus Width: 4.1029**

Entry



# B1L102S, U3-ch52, adc2

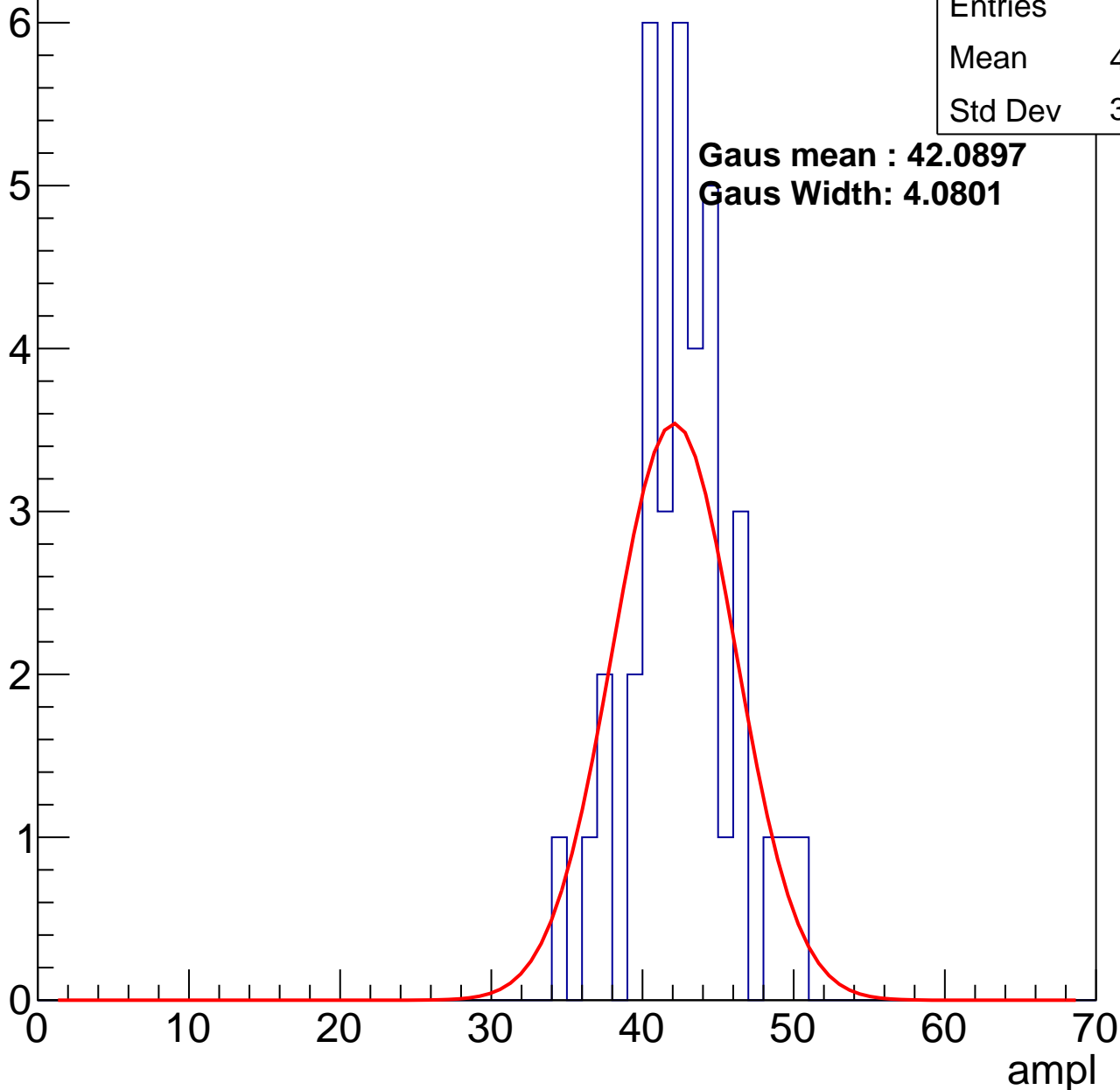
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	37
Mean	42.14
Std Dev	3.386

**Gaus mean : 42.0897**

**Gaus Width: 4.0801**

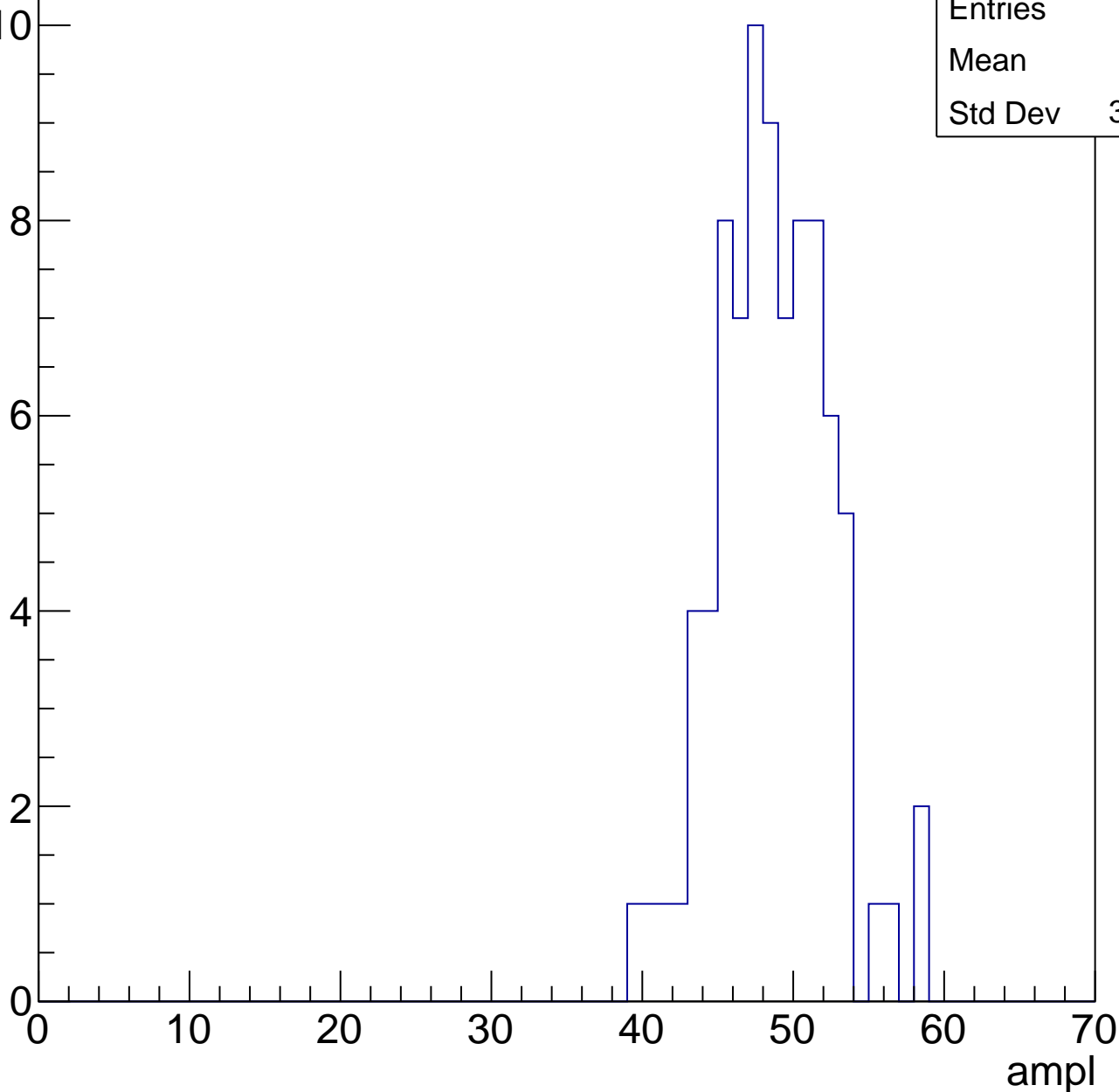


# B1L102S, U3-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	48.2
Std Dev	3.693

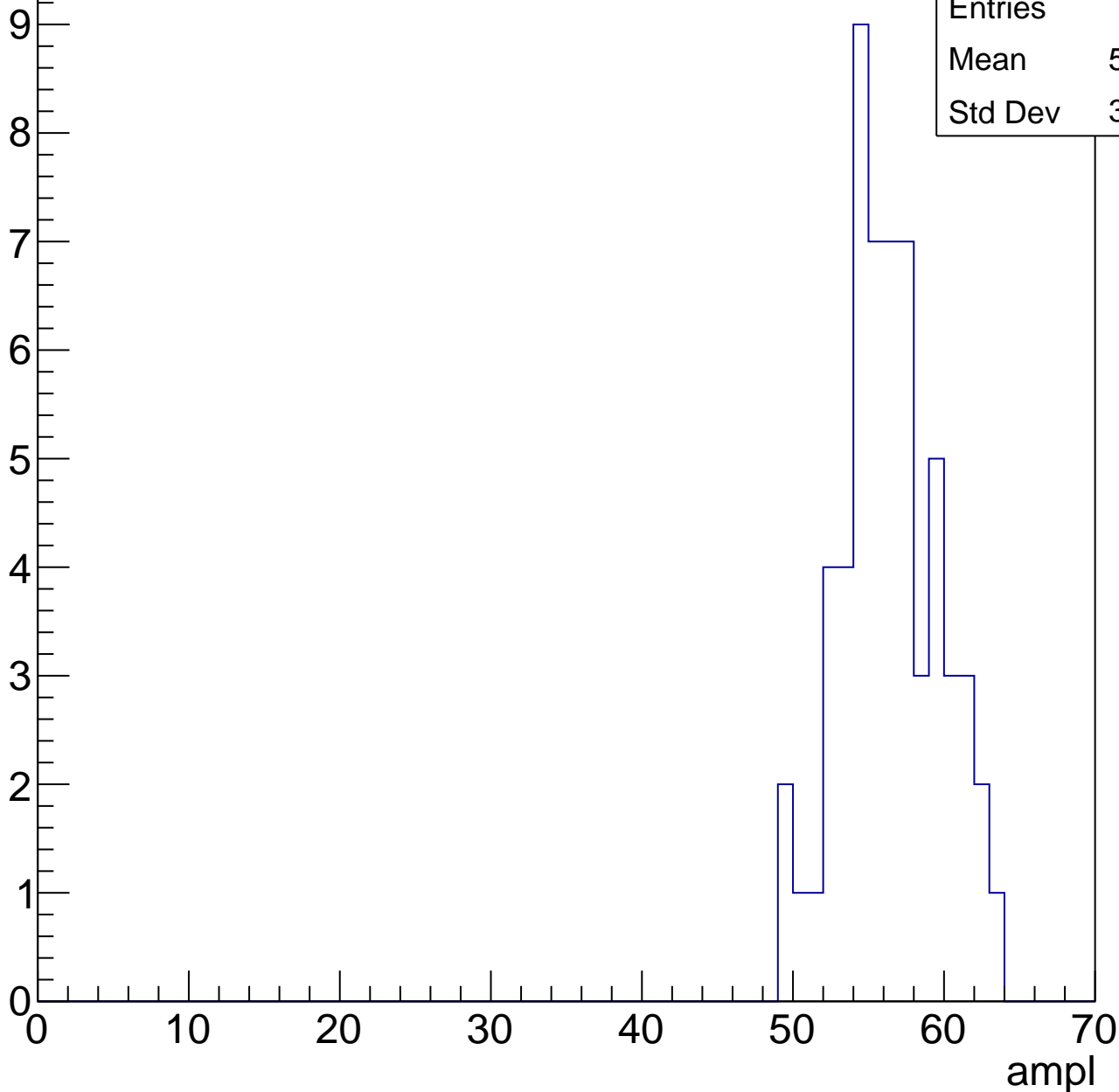


# B1L102S, U3-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	55.93
Std Dev	3.215

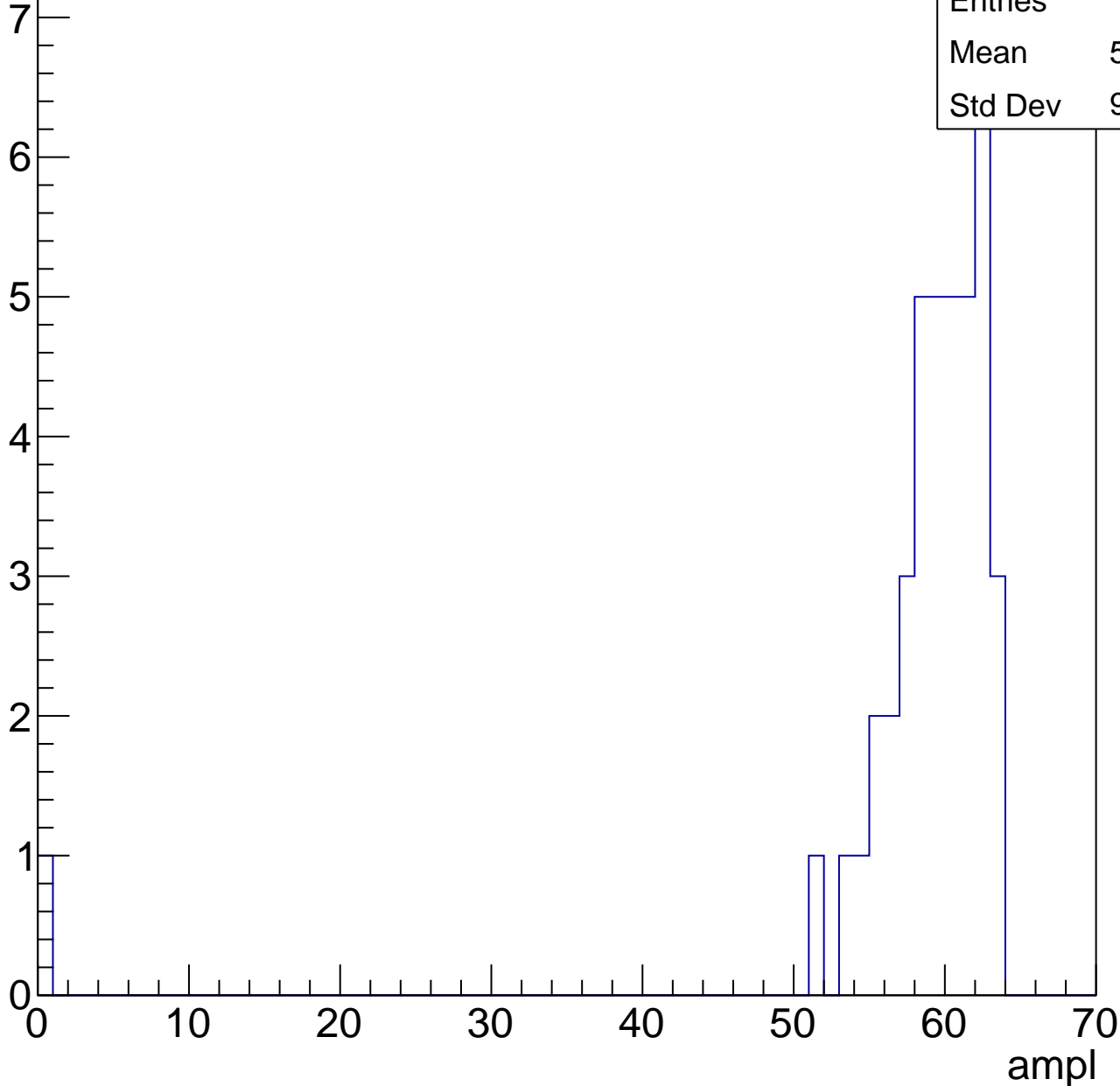


# B1L102S, U3-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	41
Mean	57.66
Std Dev	9.545

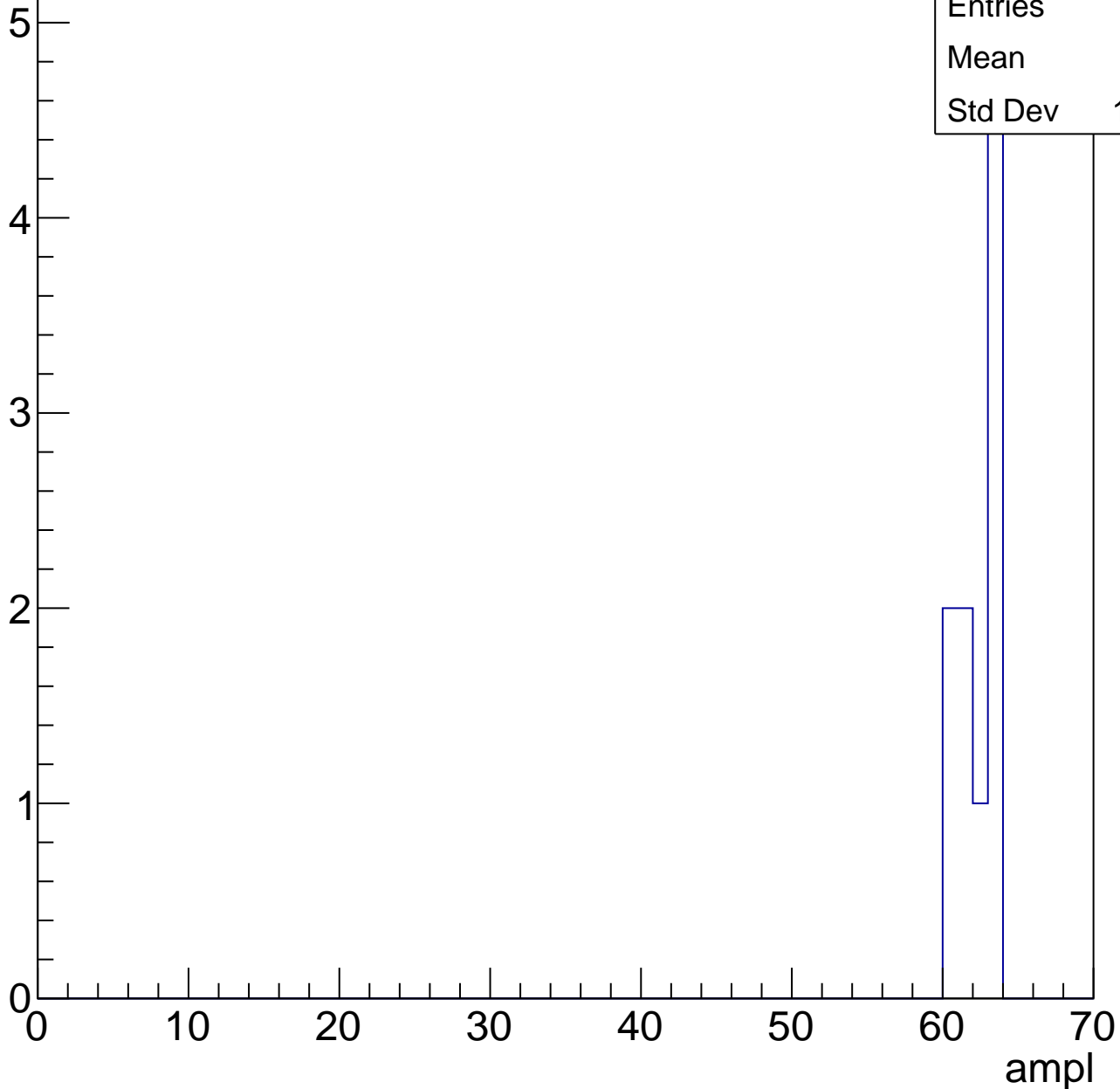


# B1L102S, U3-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	10
Mean	61.9
Std Dev	1.221





# B1L102S, U3-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch53, adc0

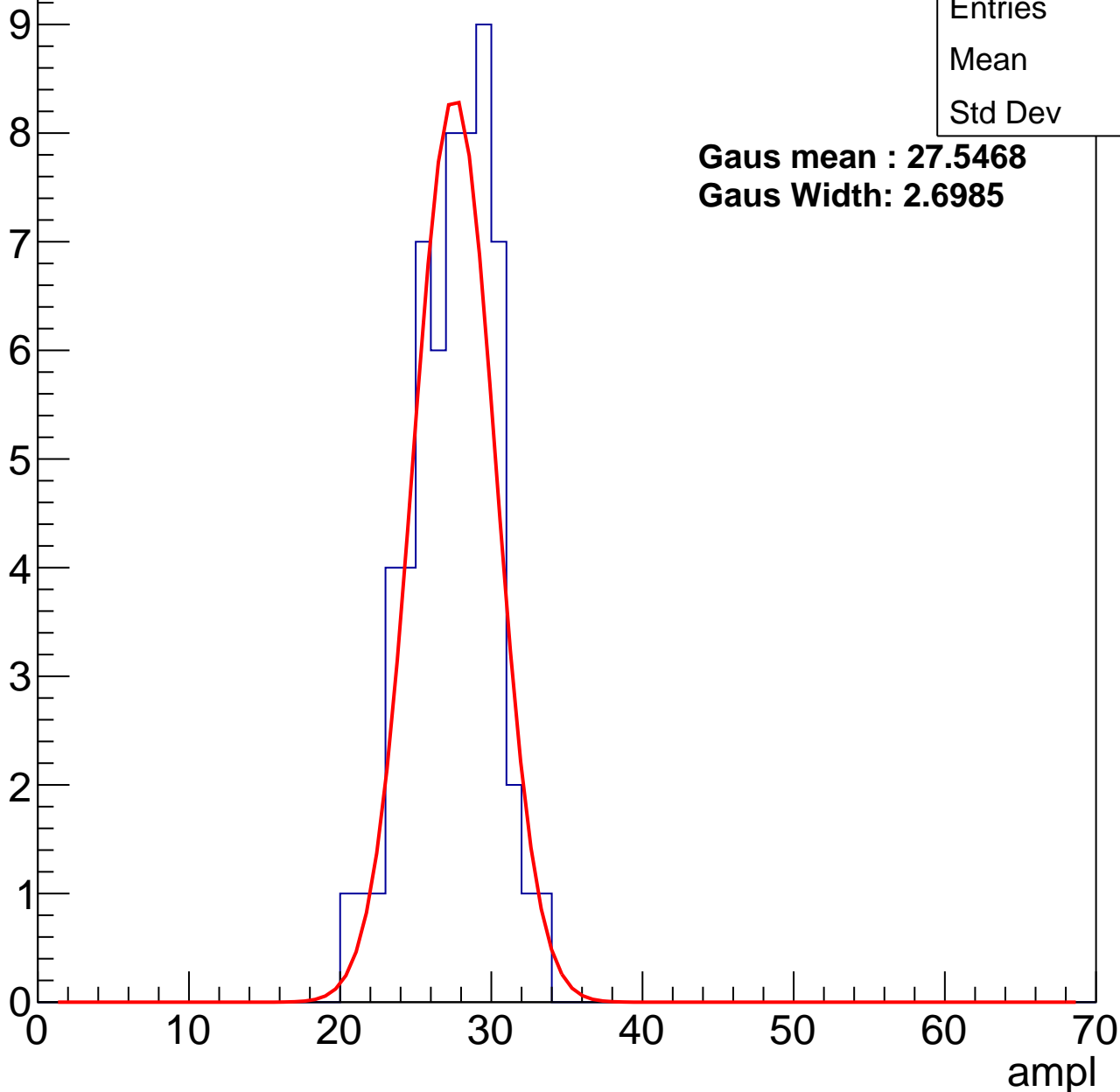
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	27
Std Dev	2.72

**Gaus mean : 27.5468**

**Gaus Width: 2.6985**



# B1L102S, U3-ch53, adc1

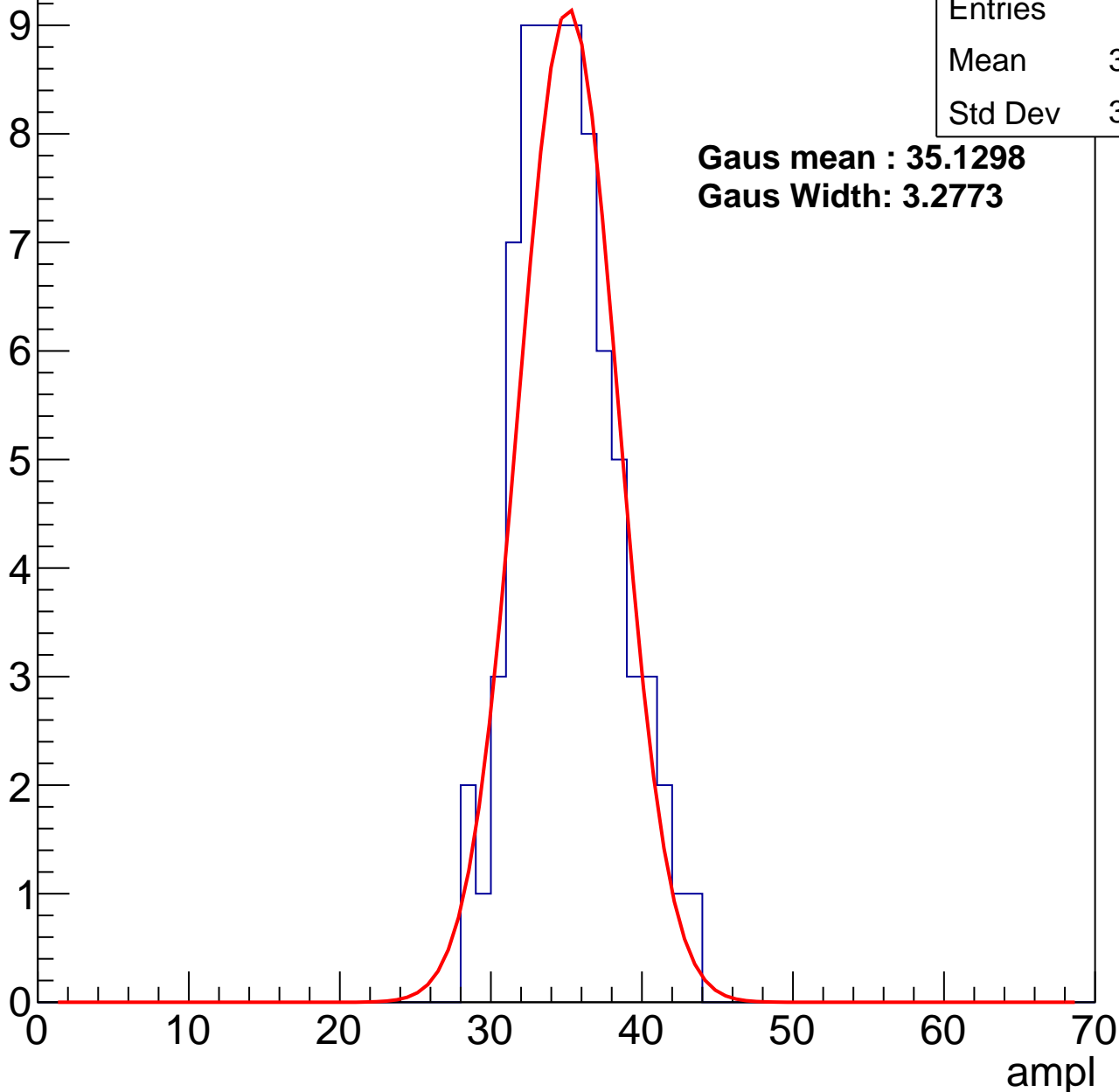
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	34.64
Std Dev	3.246

**Gaus mean : 35.1298**

**Gaus Width: 3.2773**

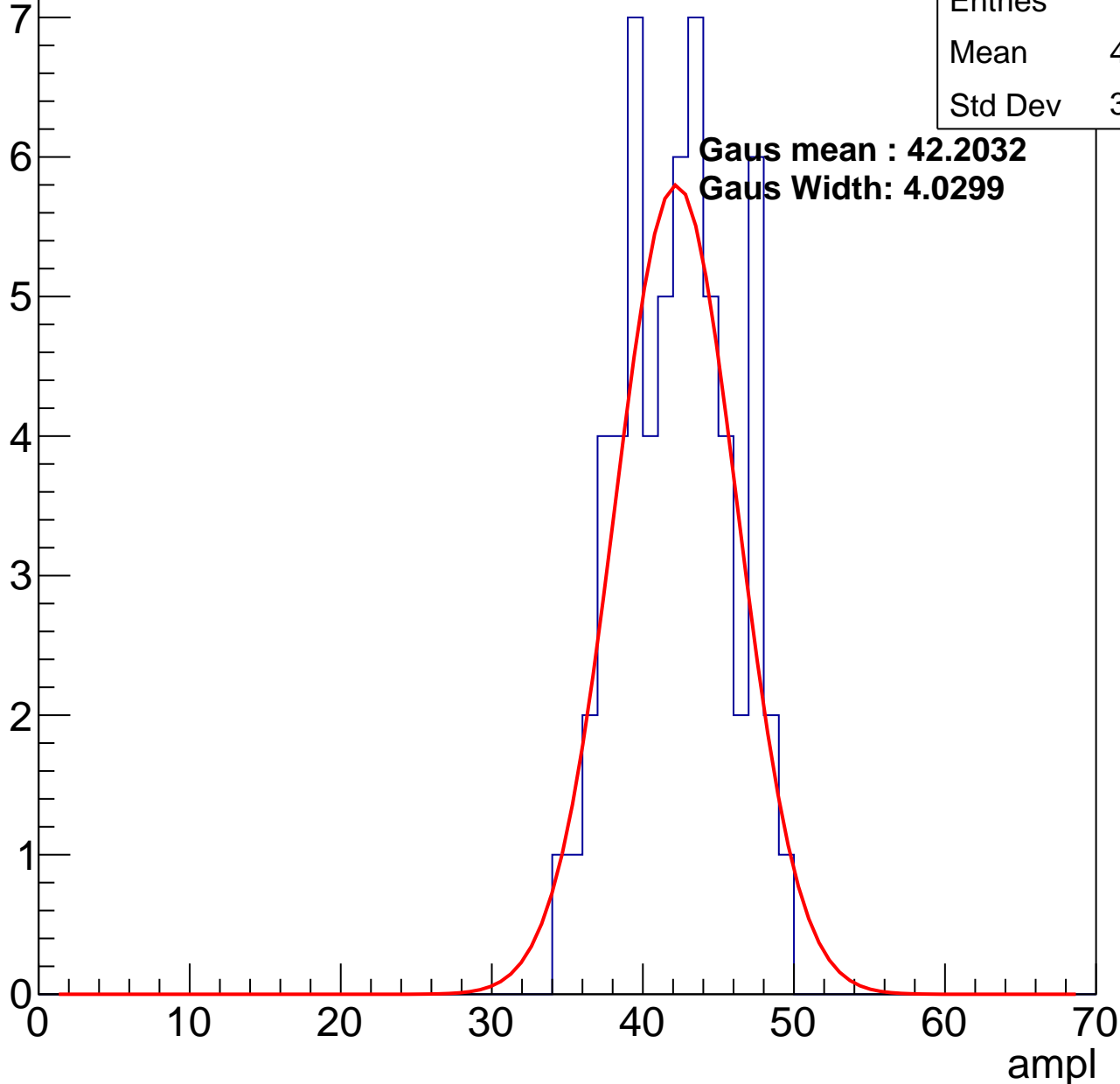


# B1L102S, U3-ch53, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	41.82
Std Dev	3.615

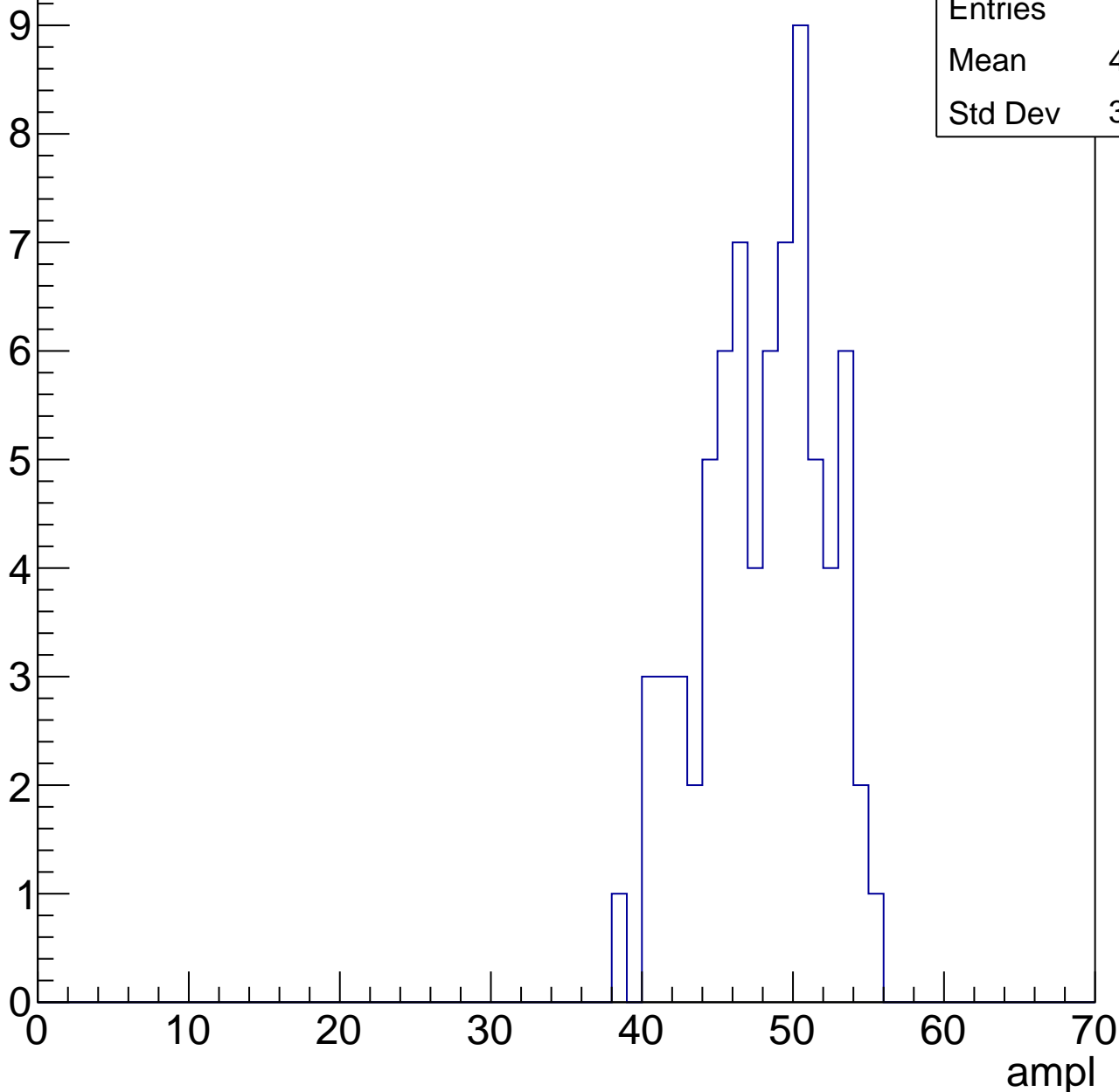


# B1L102S, U3-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	47.54
Std Dev	3.977

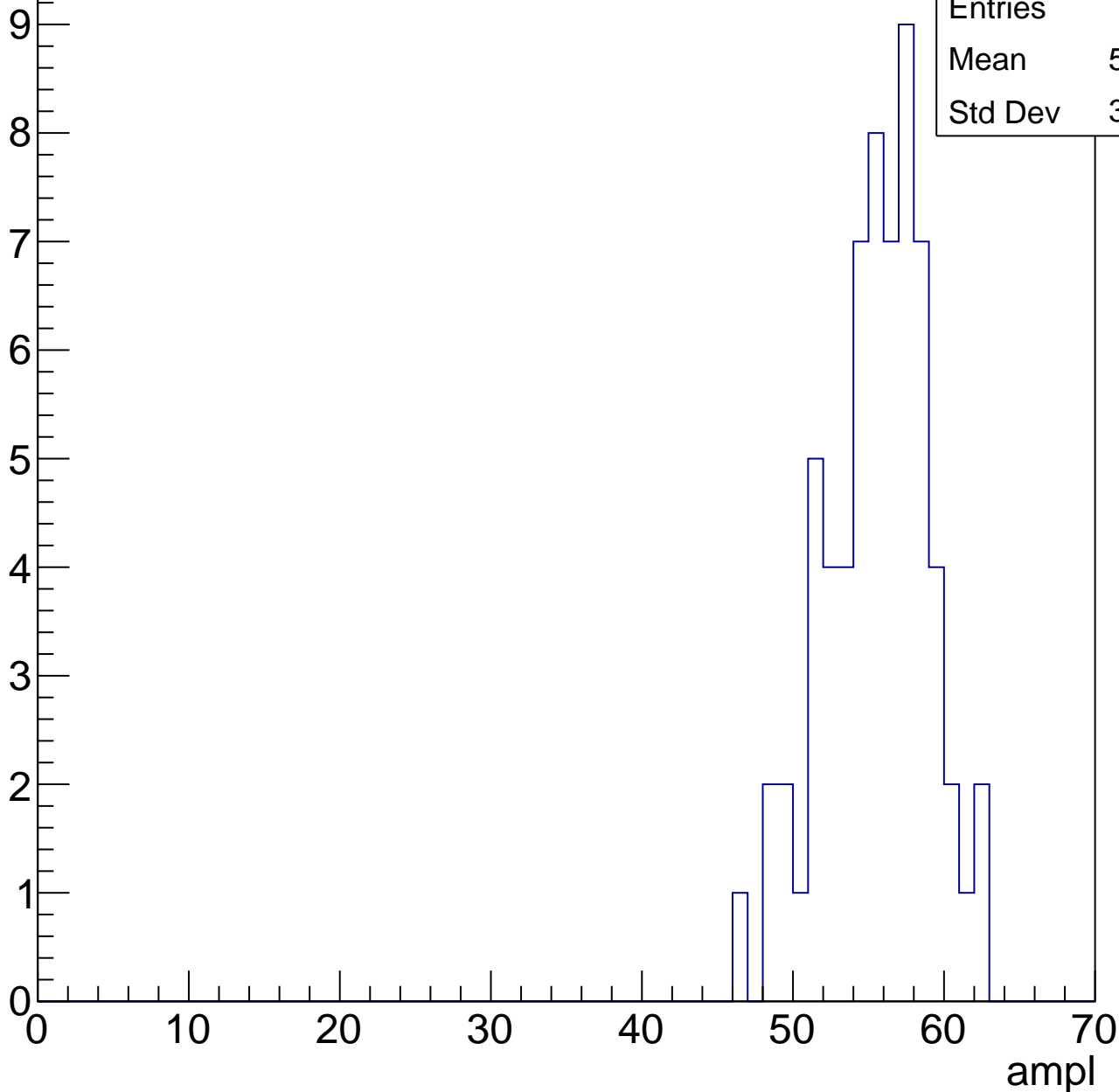


# B1L102S, U3-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	55.08
Std Dev	3.413



# B1L102S, U3-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

7

6

5

4

3

2

1

0

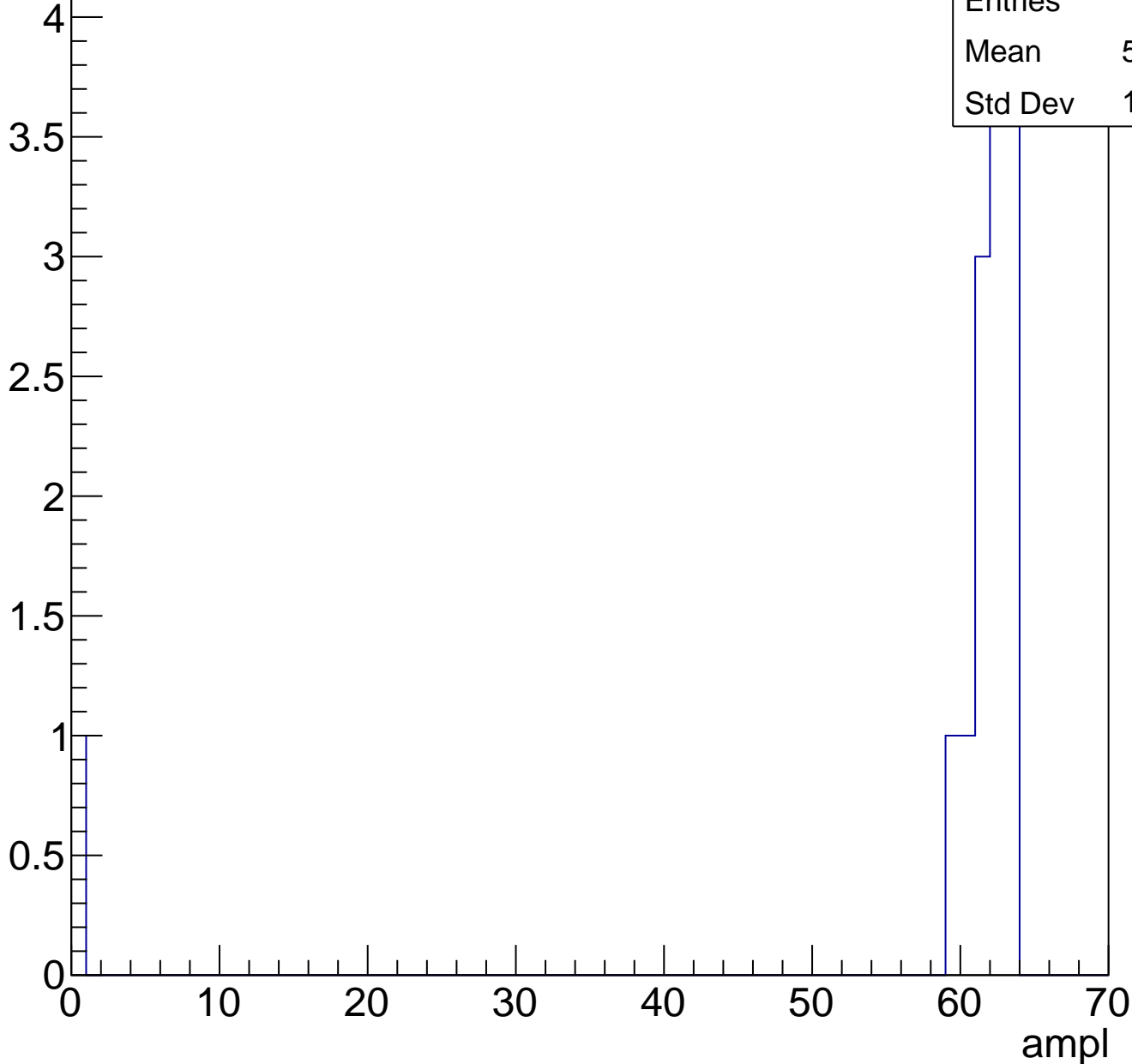
Entries	39
Mean	59.46
Std Dev	2.899

ampl

# B1L102S, U3-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch54, adc0

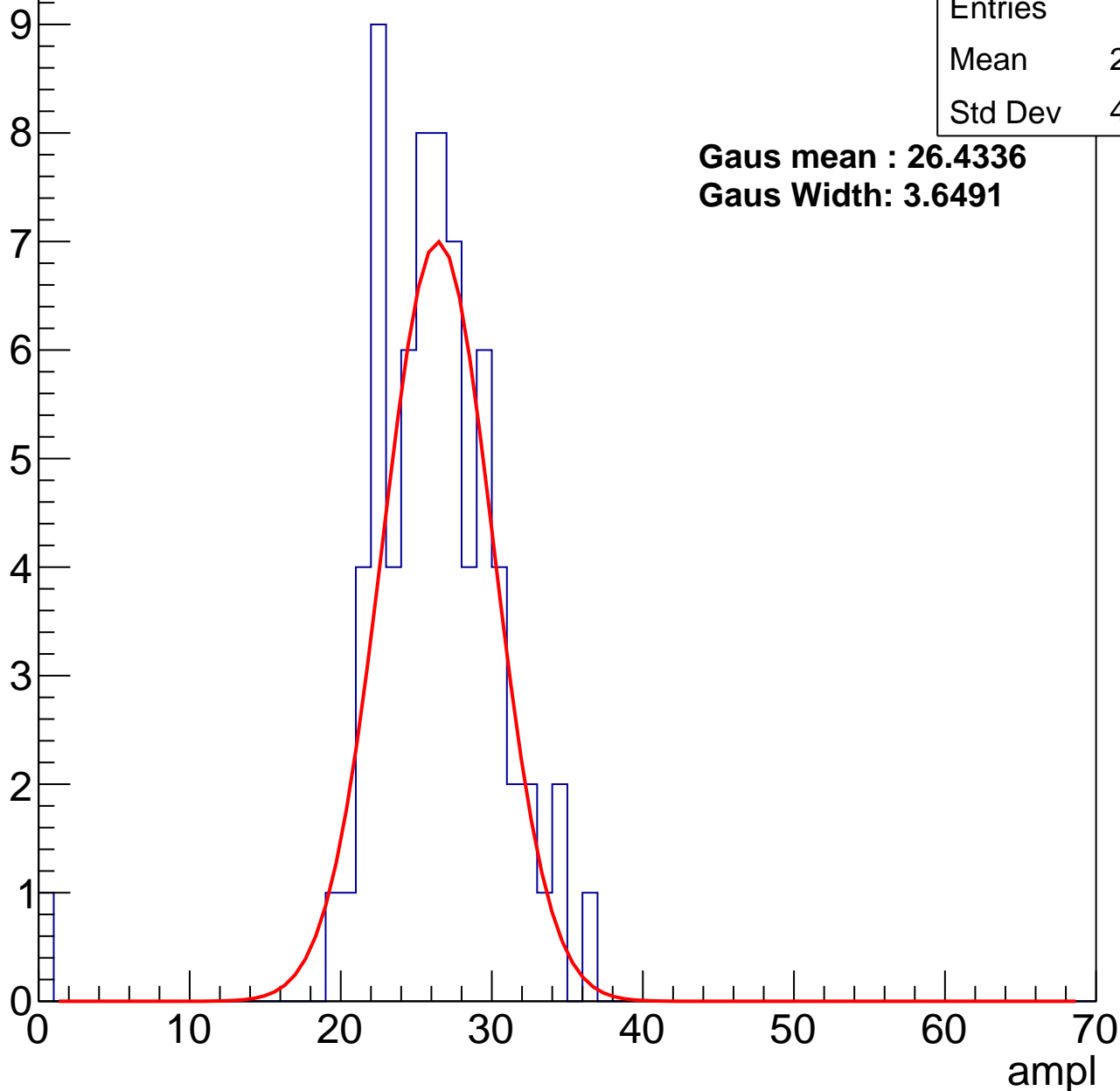
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	25.68
Std Dev	4.755

**Gaus mean : 26.4336**

**Gaus Width: 3.6491**



# B1L102S, U3-ch54, adc1

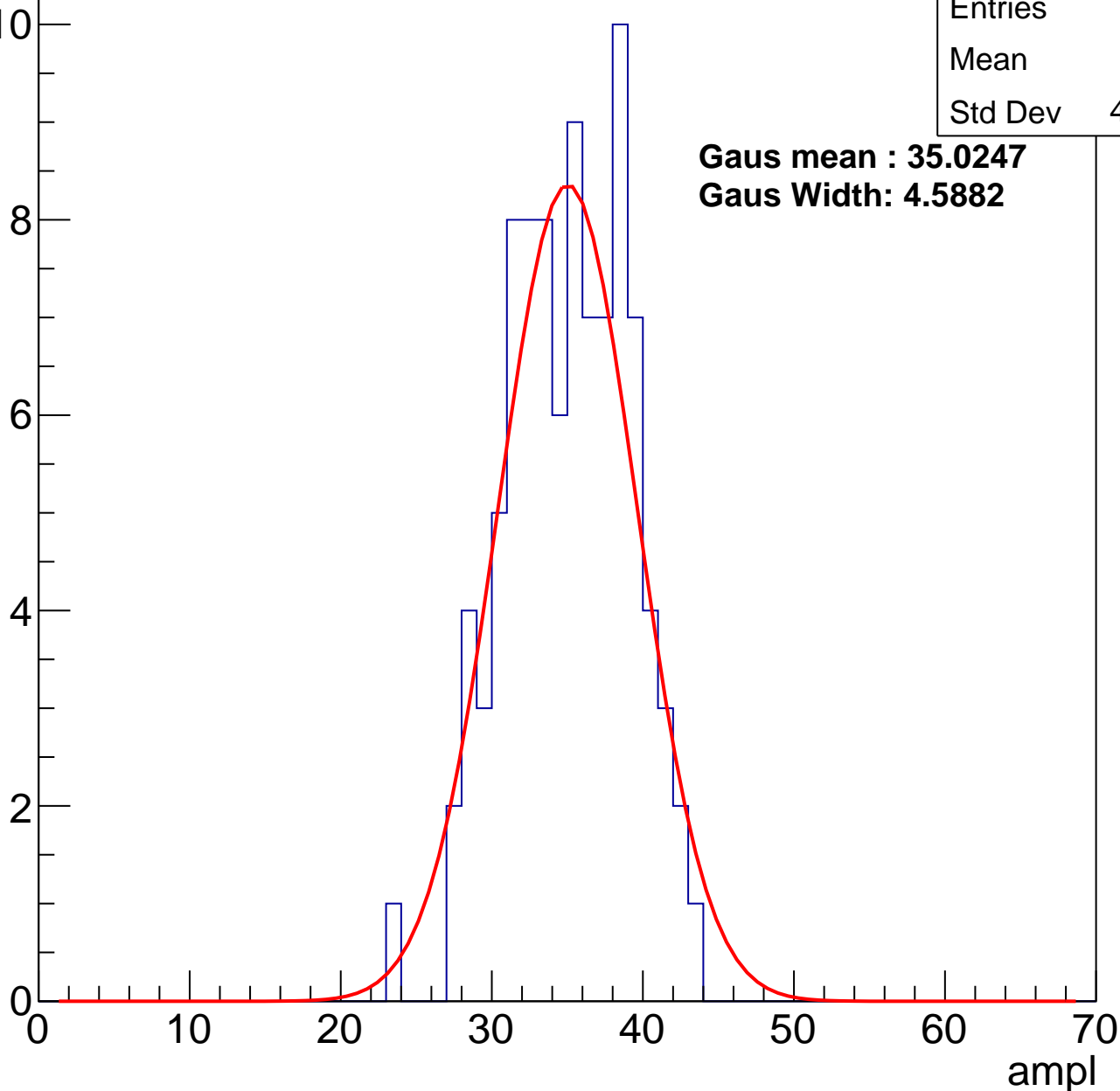
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	95
Mean	34.6
Std Dev	4.014

**Gaus mean : 35.0247**

**Gaus Width: 4.5882**



# B1L102S, U3-ch54, adc2

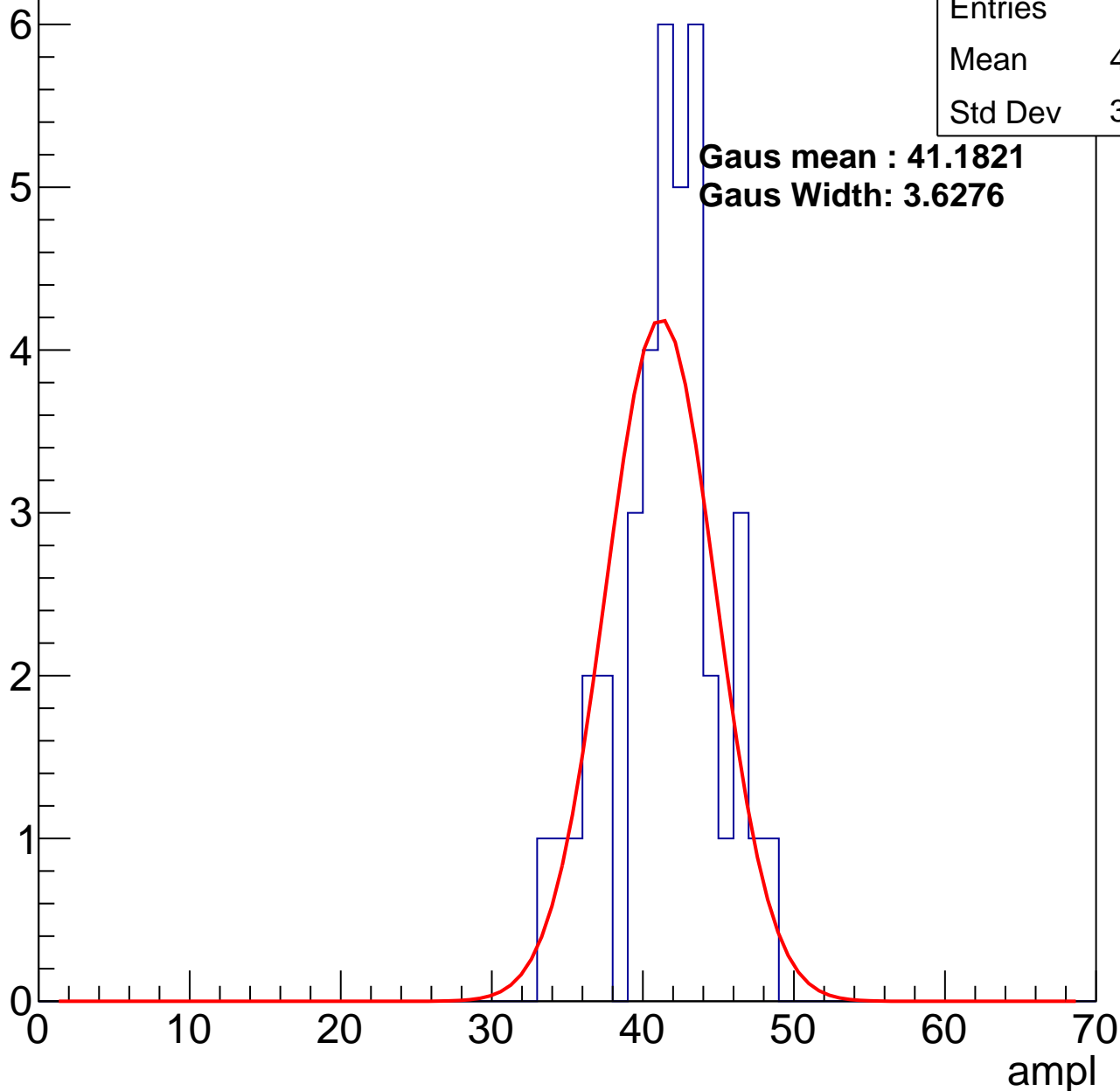
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	39
Mean	41.15
Std Dev	3.468

**Gaus mean : 41.1821**

**Gaus Width: 3.6276**

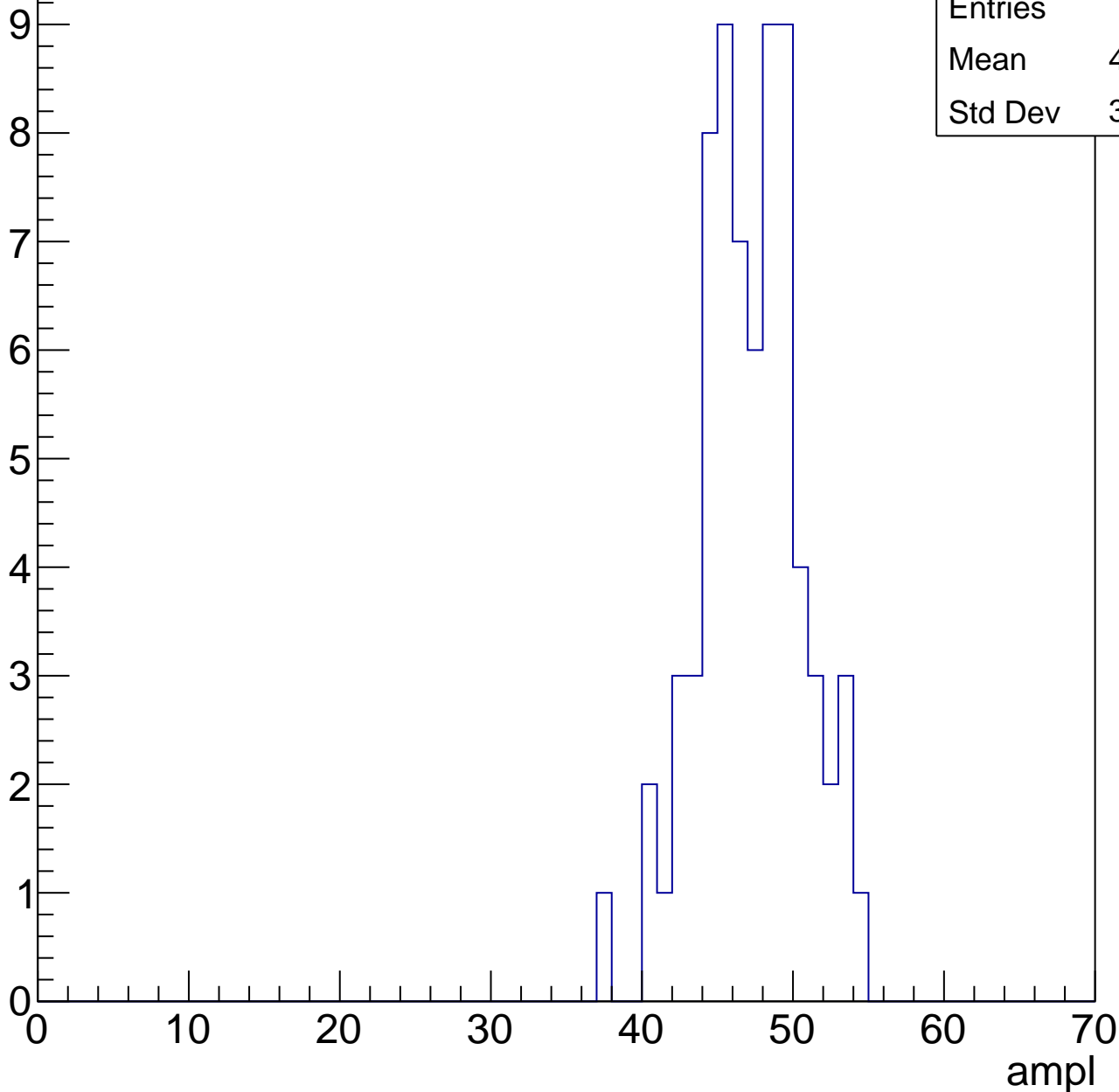


# B1L102S, U3-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

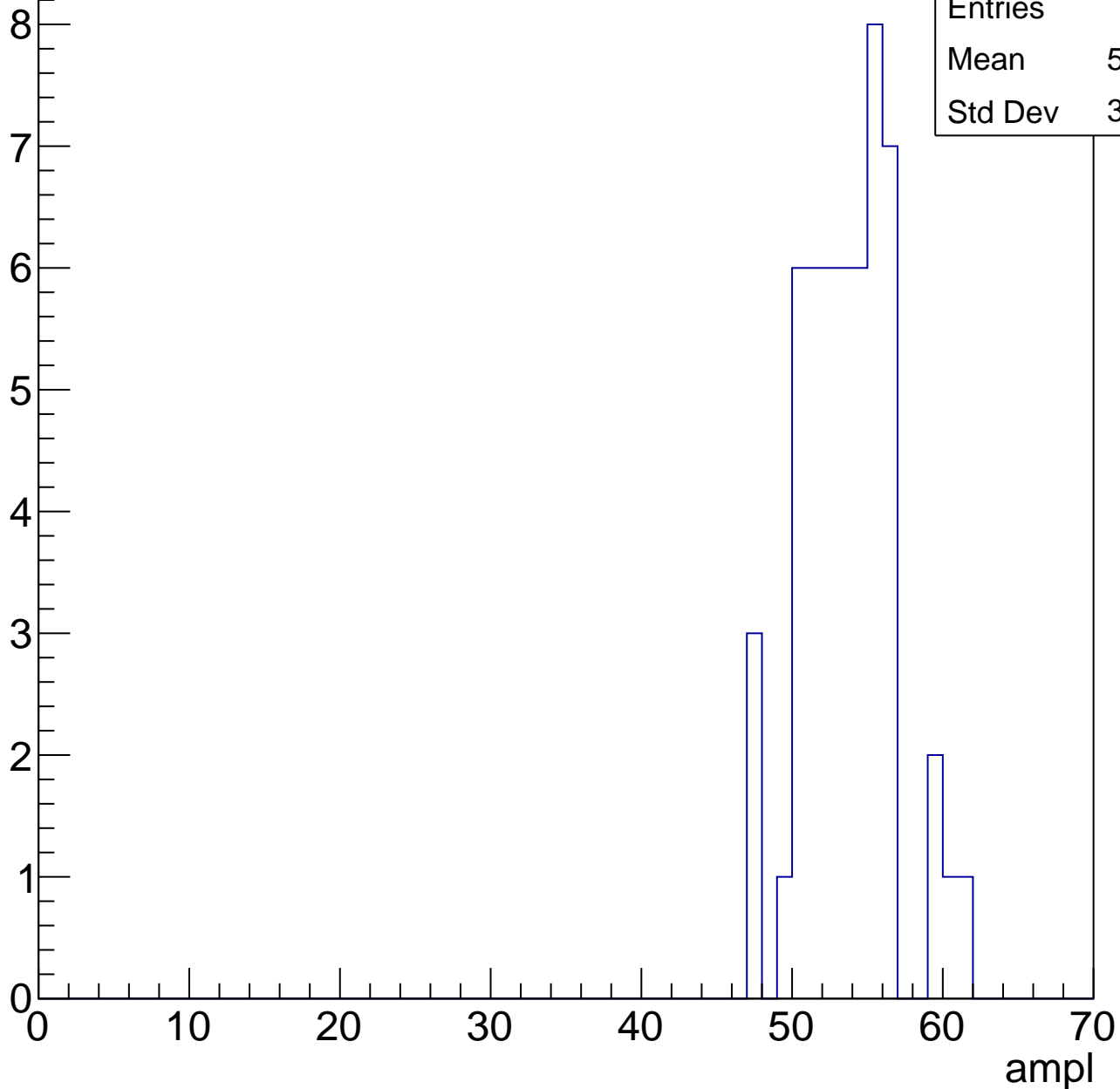
Entries	71
Mean	46.72
Std Dev	3.362



# B1L102S, U3-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

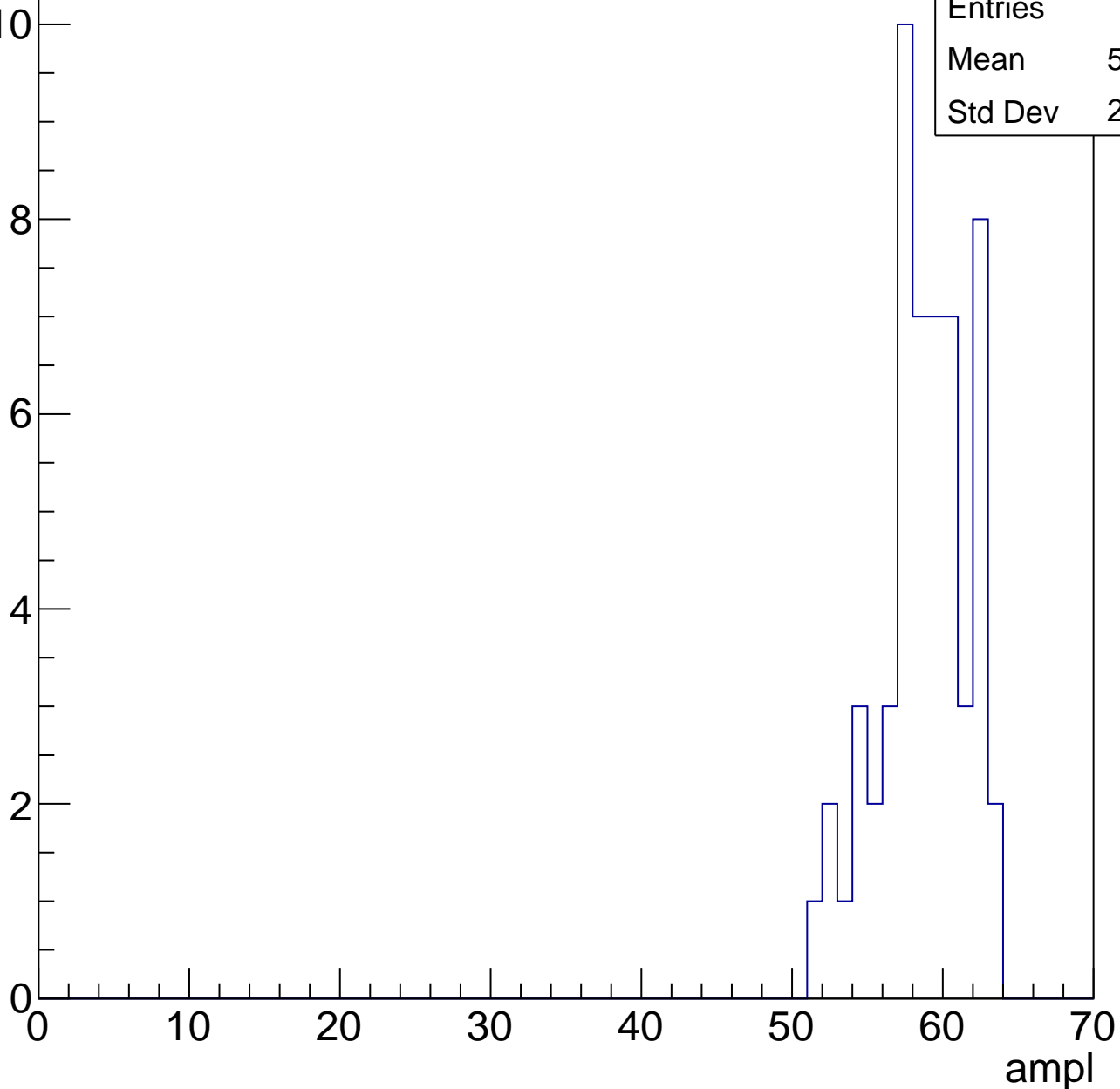


# B1L102S, U3-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	58.25
Std Dev	2.899

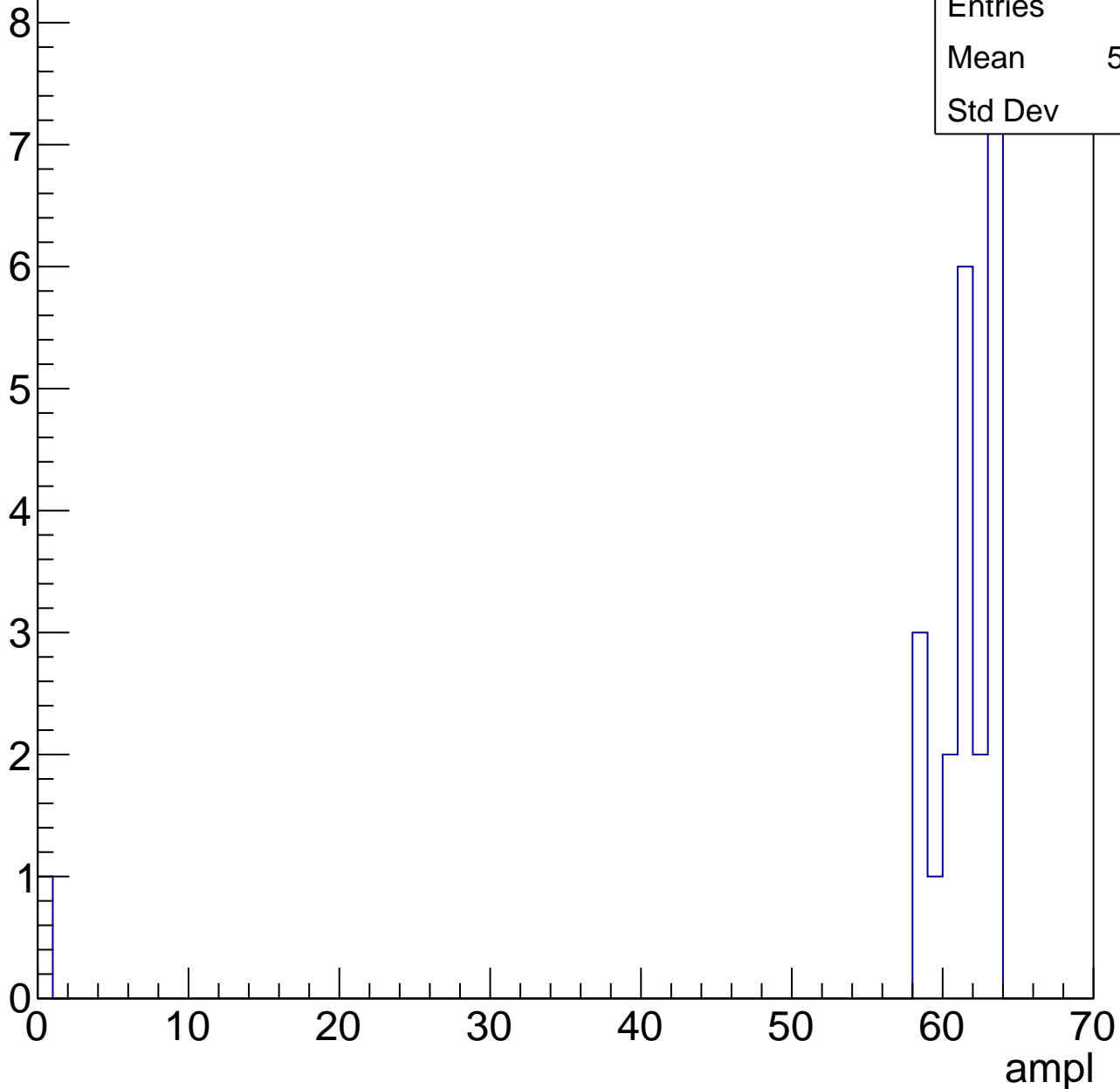


# B1L102S, U3-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	23
Mean	58.57
Std Dev	12.6





# B1L102S, U3-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch55, adc0

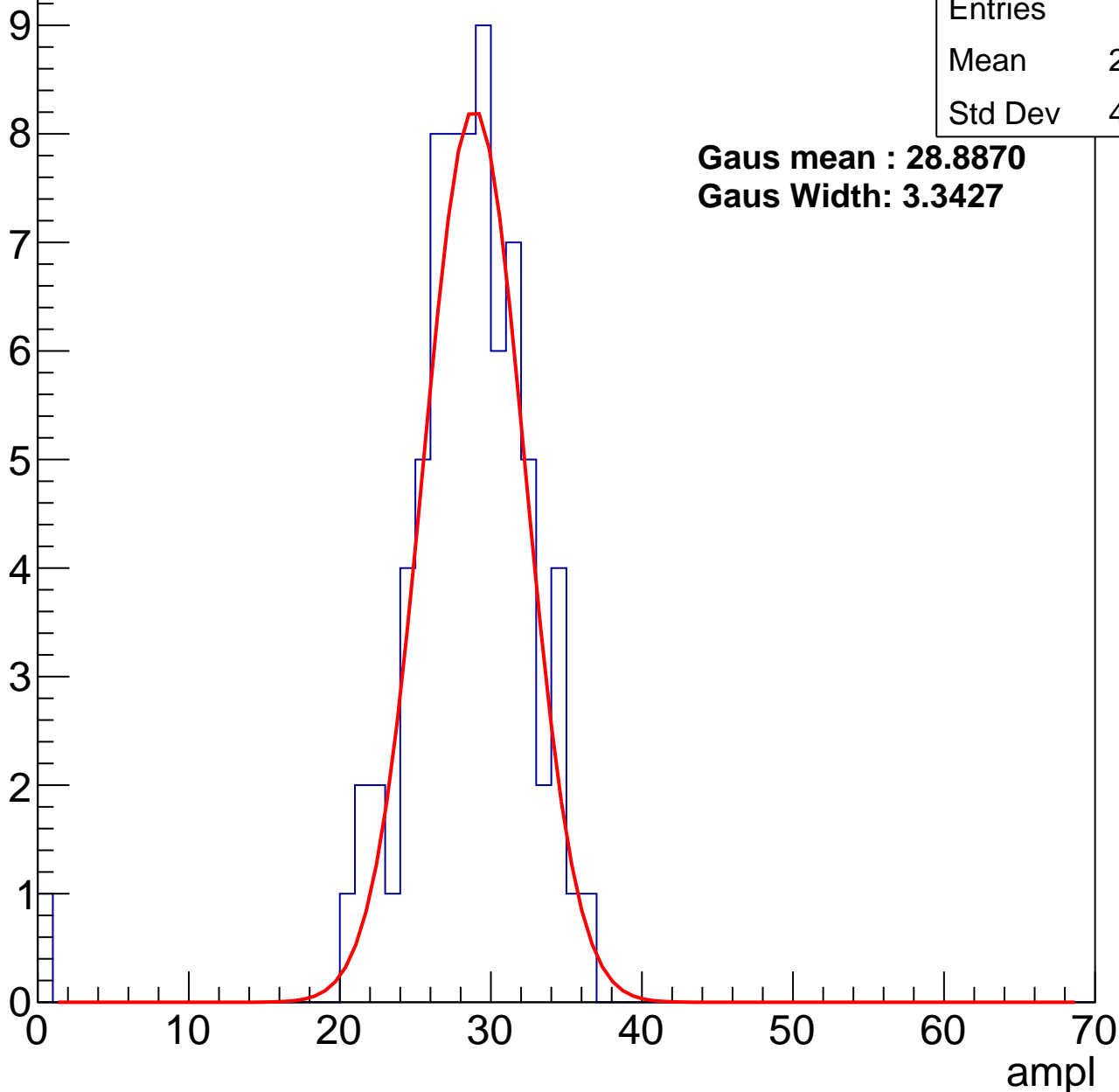
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	27.85
Std Dev	4.724

**Gaus mean : 28.8870**

**Gaus Width: 3.3427**



# B1L102S, U3-ch55, adc1

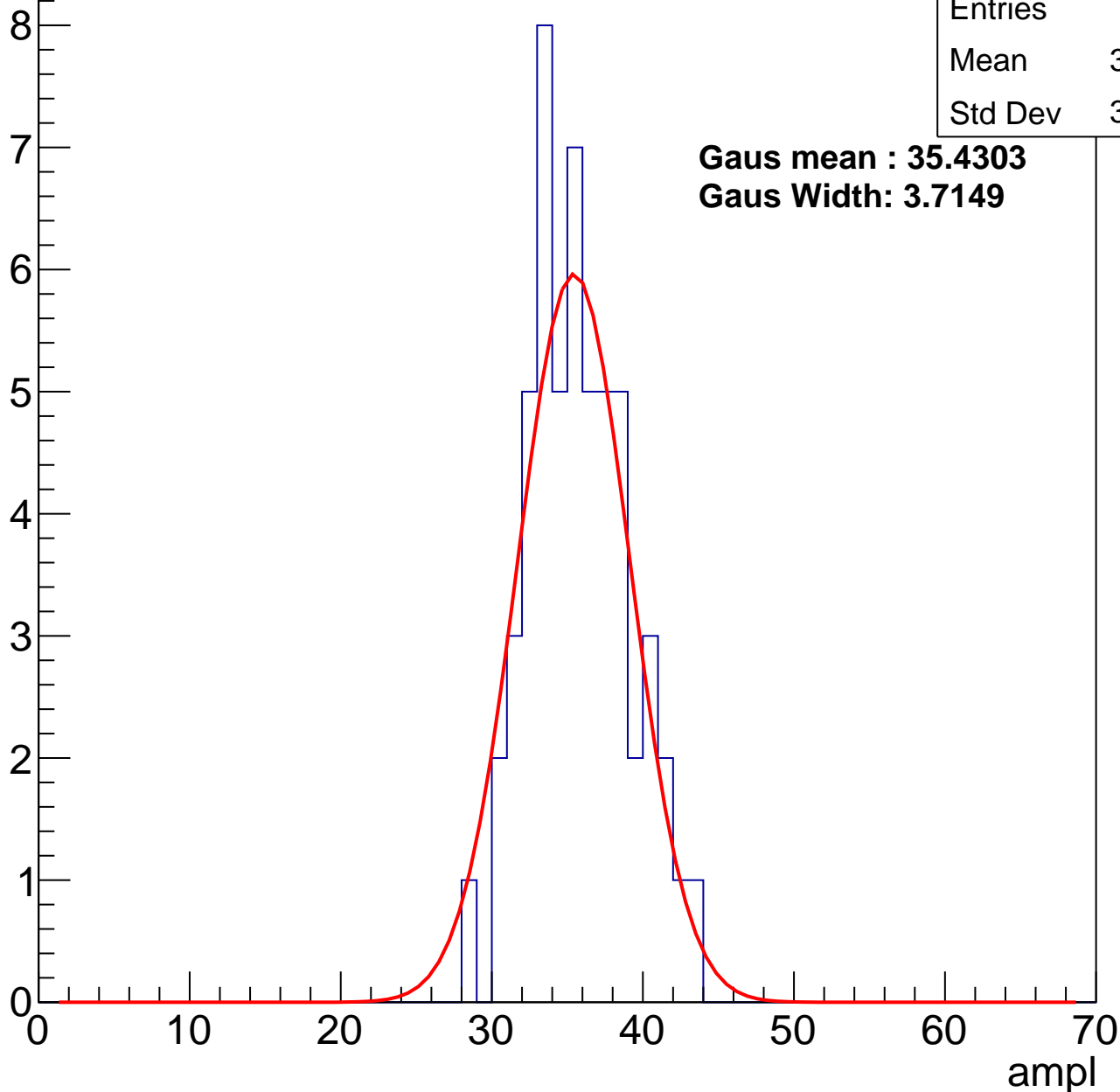
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	35.27
Std Dev	3.267

**Gaus mean : 35.4303**

**Gaus Width: 3.7149**



# B1L102S, U3-ch55, adc2

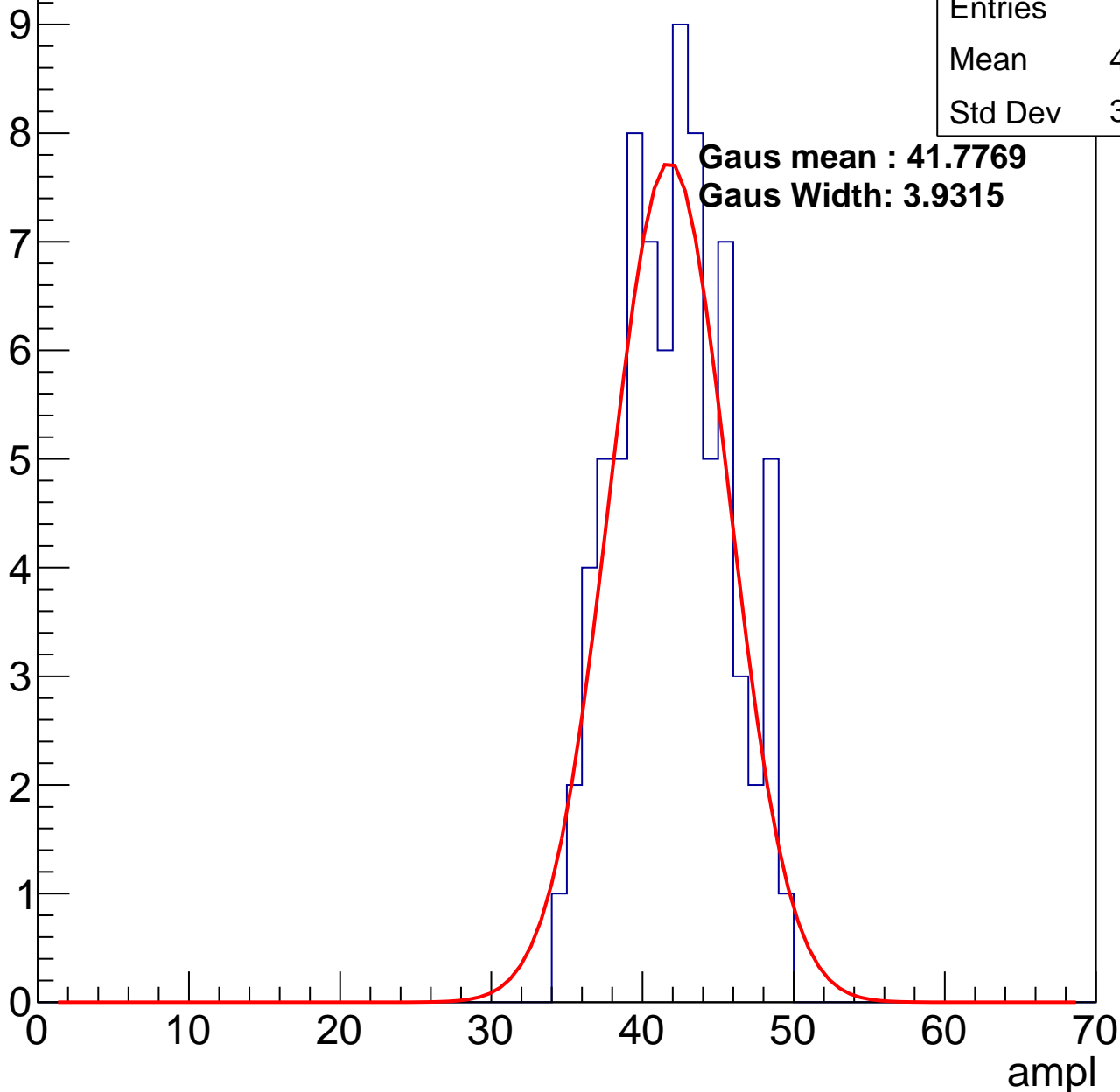
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	41.53
Std Dev	3.612

**Gaus mean : 41.7769**

**Gaus Width: 3.9315**

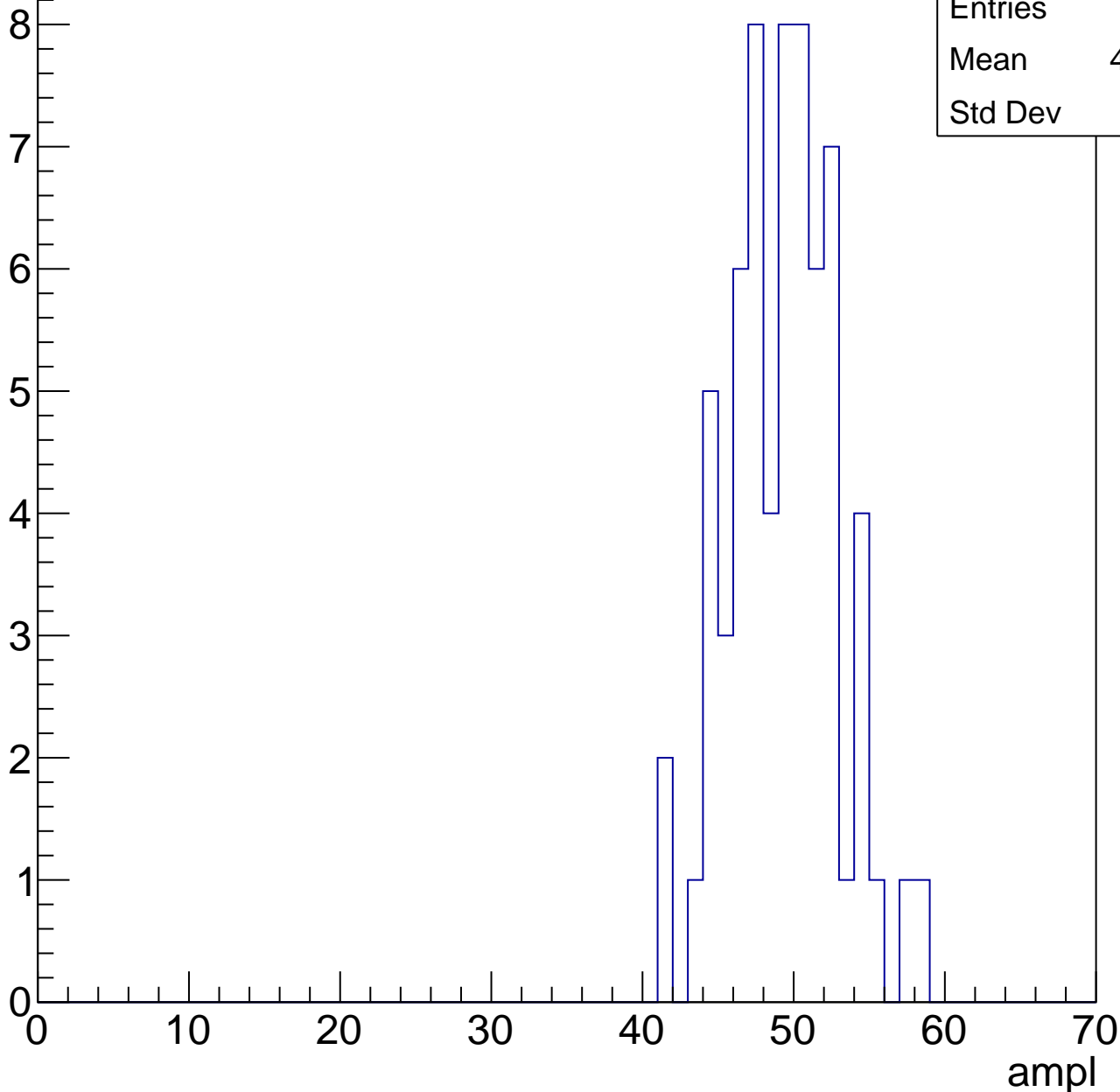


# B1L102S, U3-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	48.86
Std Dev	3.52

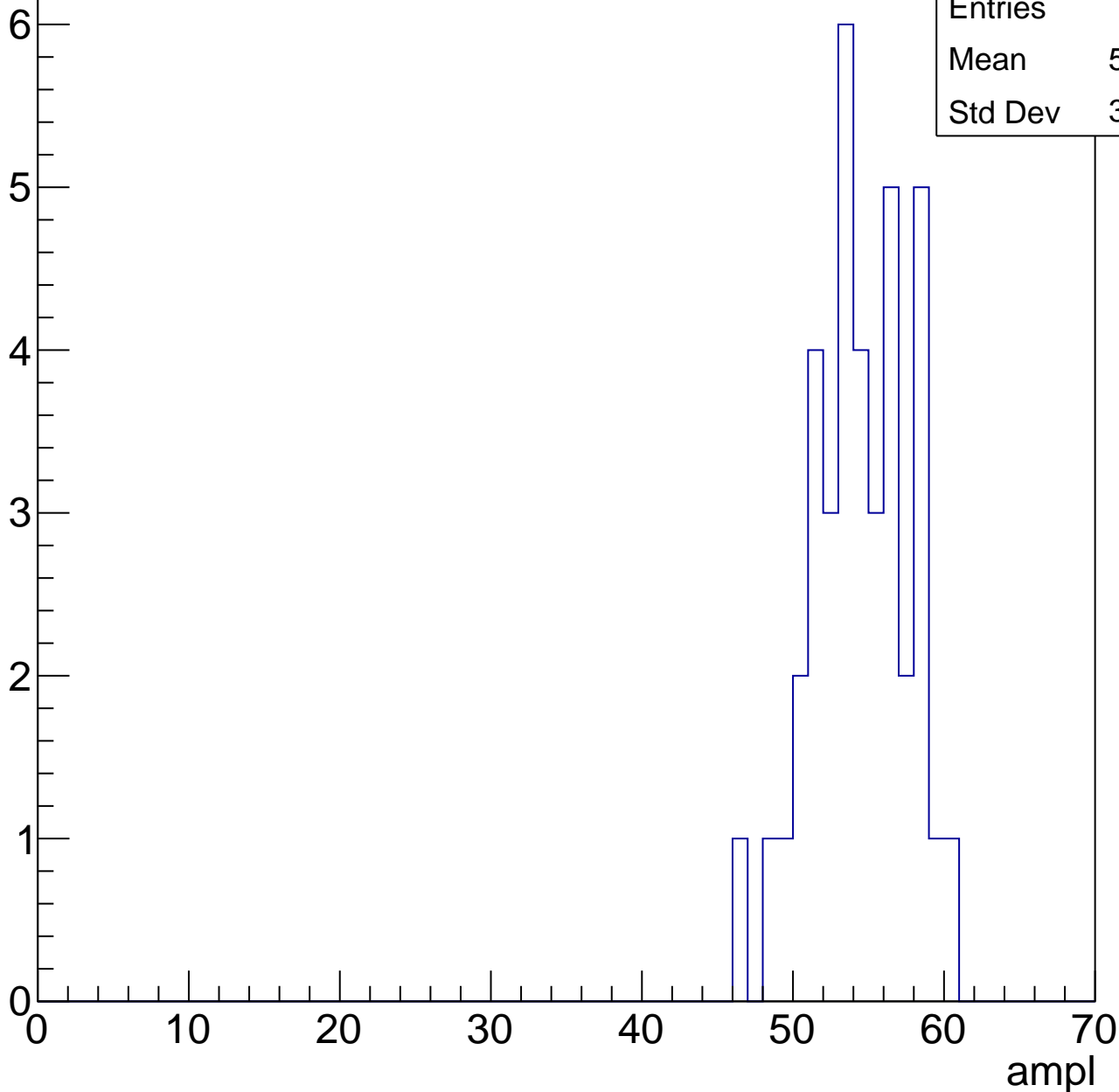


# B1L102S, U3-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	39
Mean	53.97
Std Dev	3.174



# B1L102S, U3-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

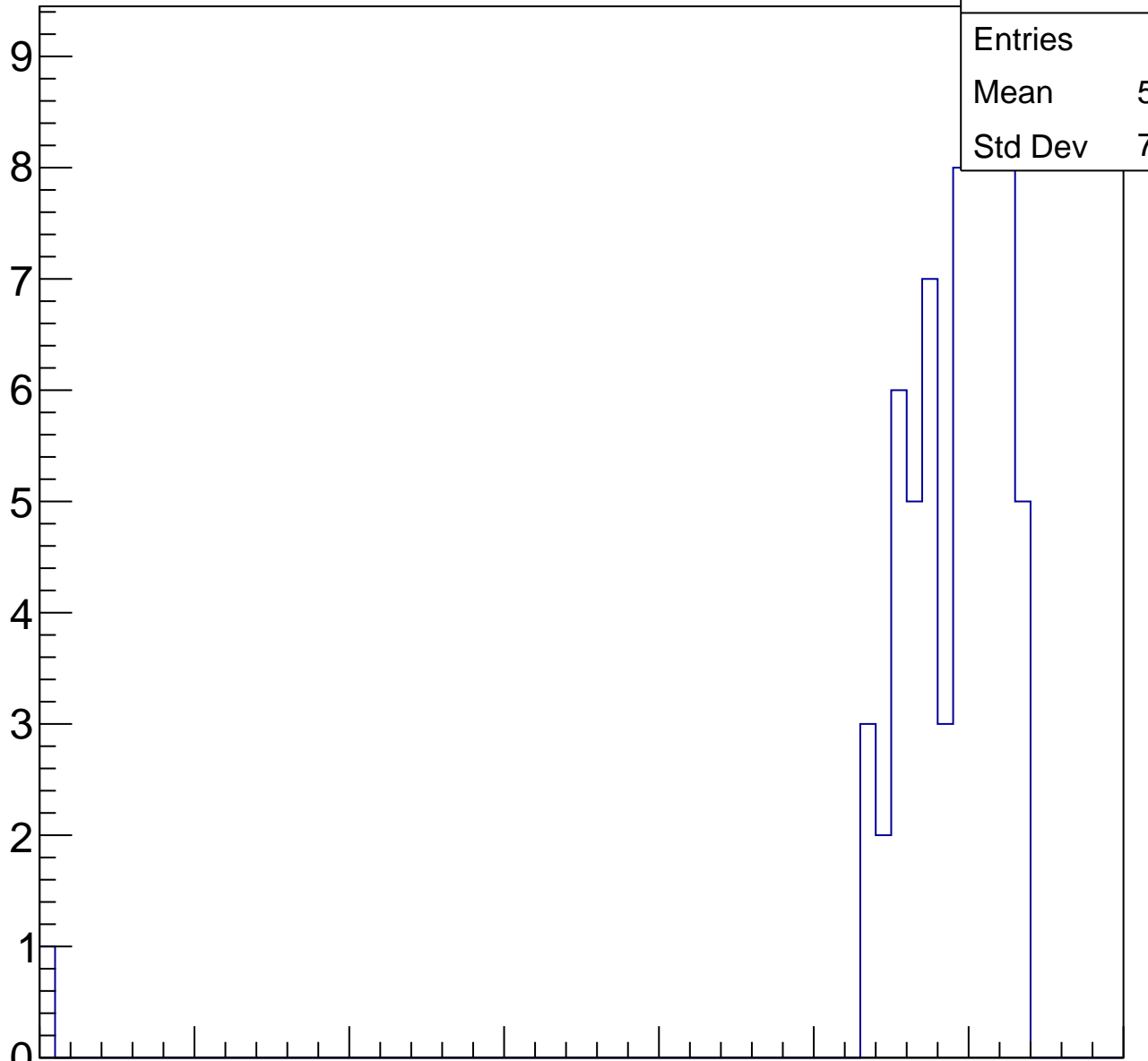
Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	65
Mean	57.86
Std Dev	7.766

ampl

0 10 20 30 40 50 60 70

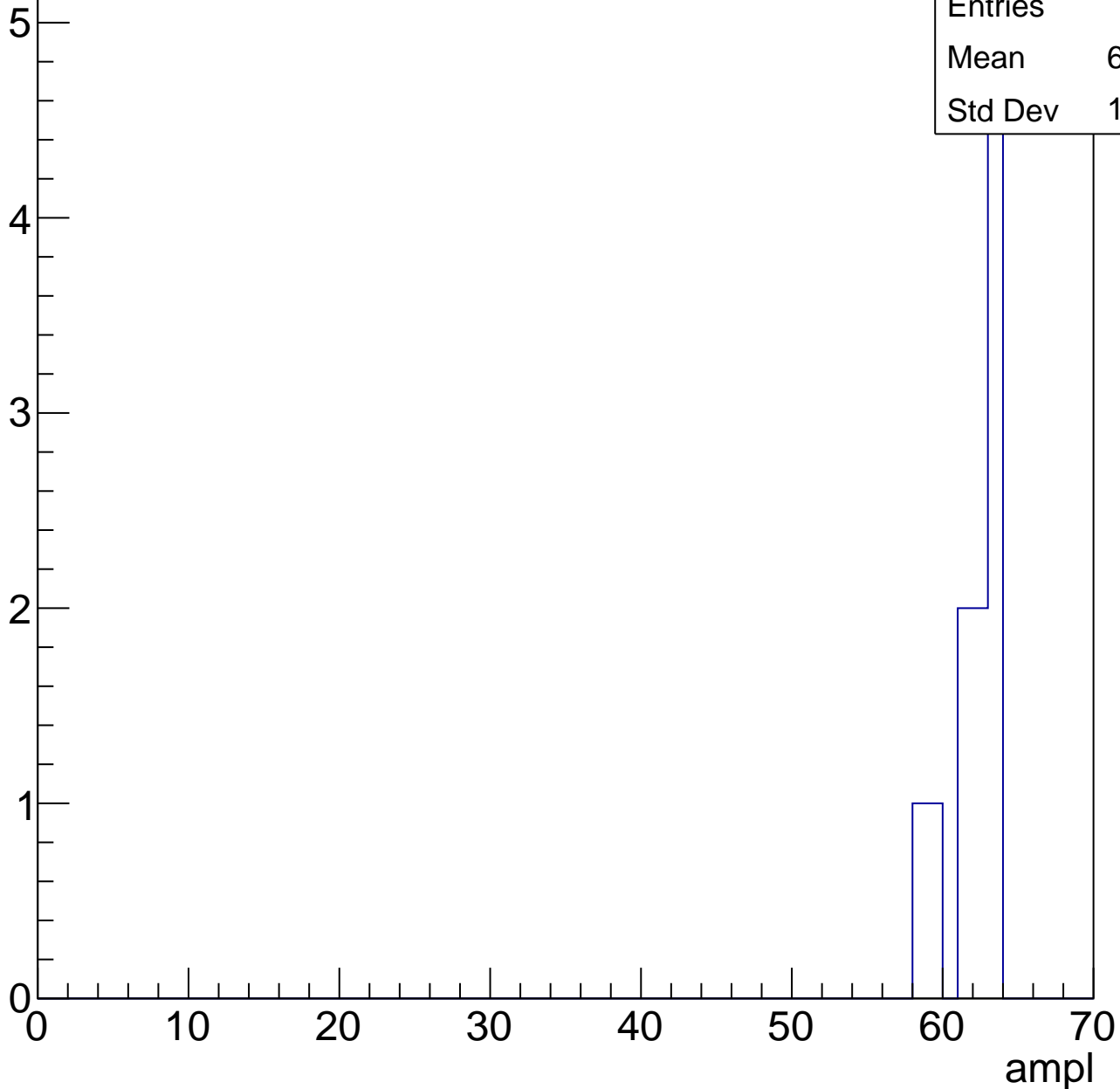


# B1L102S, U3-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	11
Mean	61.64
Std Dev	1.666





# B1L102S, U3-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U3-ch56, adc0

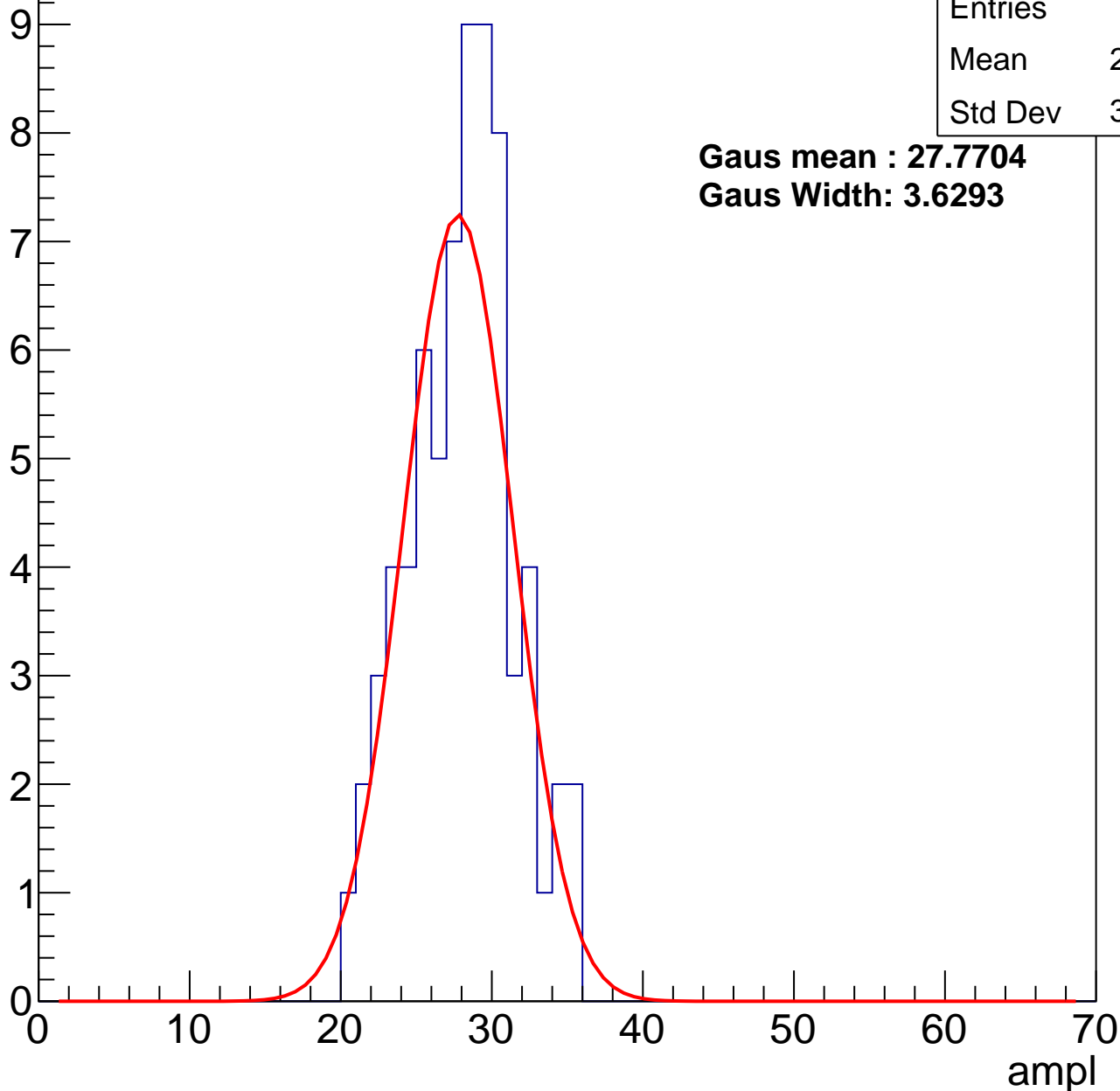
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	27.57
Std Dev	3.442

**Gaus mean : 27.7704**

**Gaus Width: 3.6293**



# B1L102S, U3-ch56, adc1

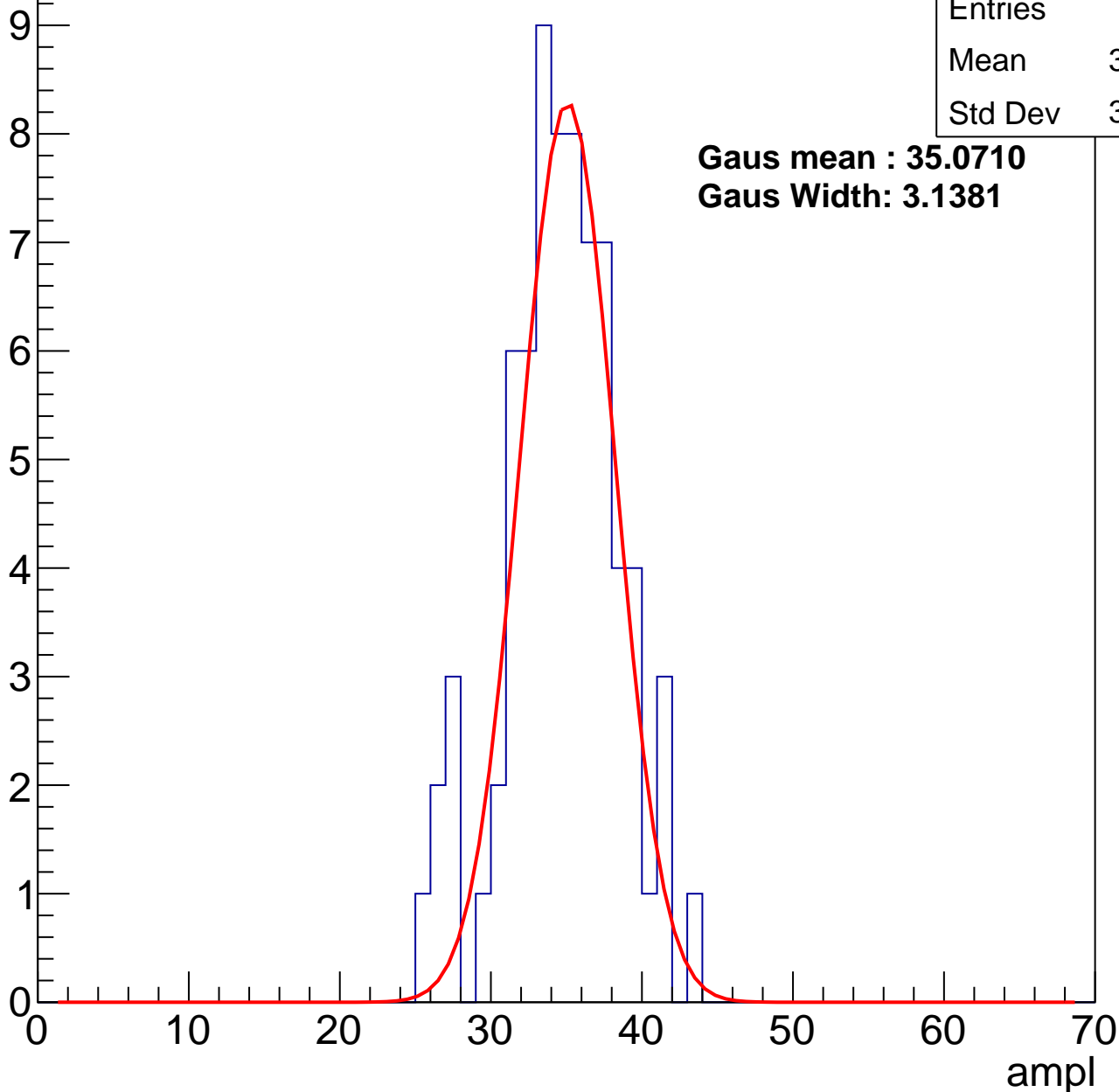
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	34.23
Std Dev	3.744

**Gaus mean : 35.0710**

**Gaus Width: 3.1381**



# B1L102S, U3-ch56, adc2

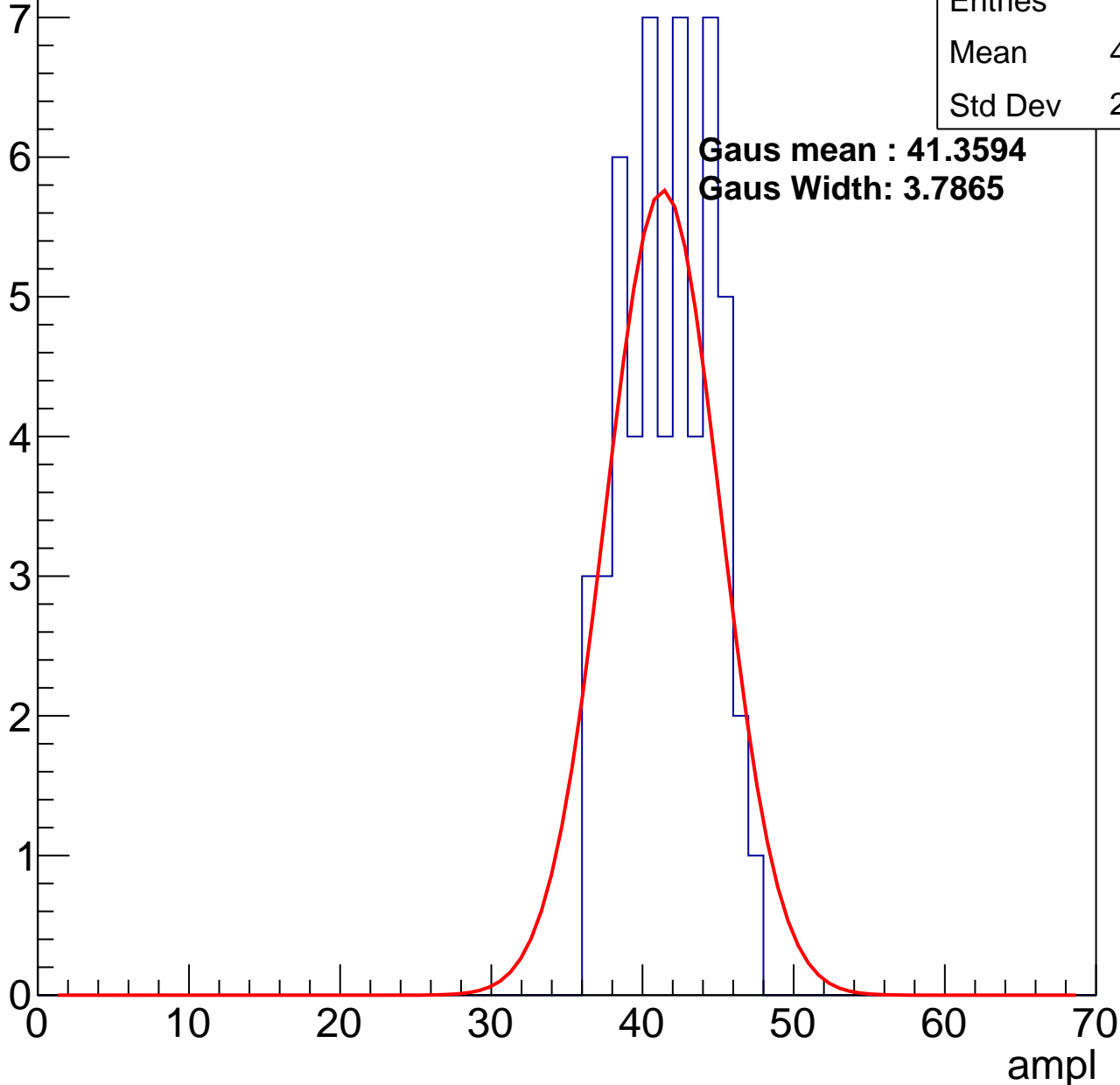
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	41.23
Std Dev	2.912

**Gaus mean : 41.3594**

**Gaus Width: 3.7865**

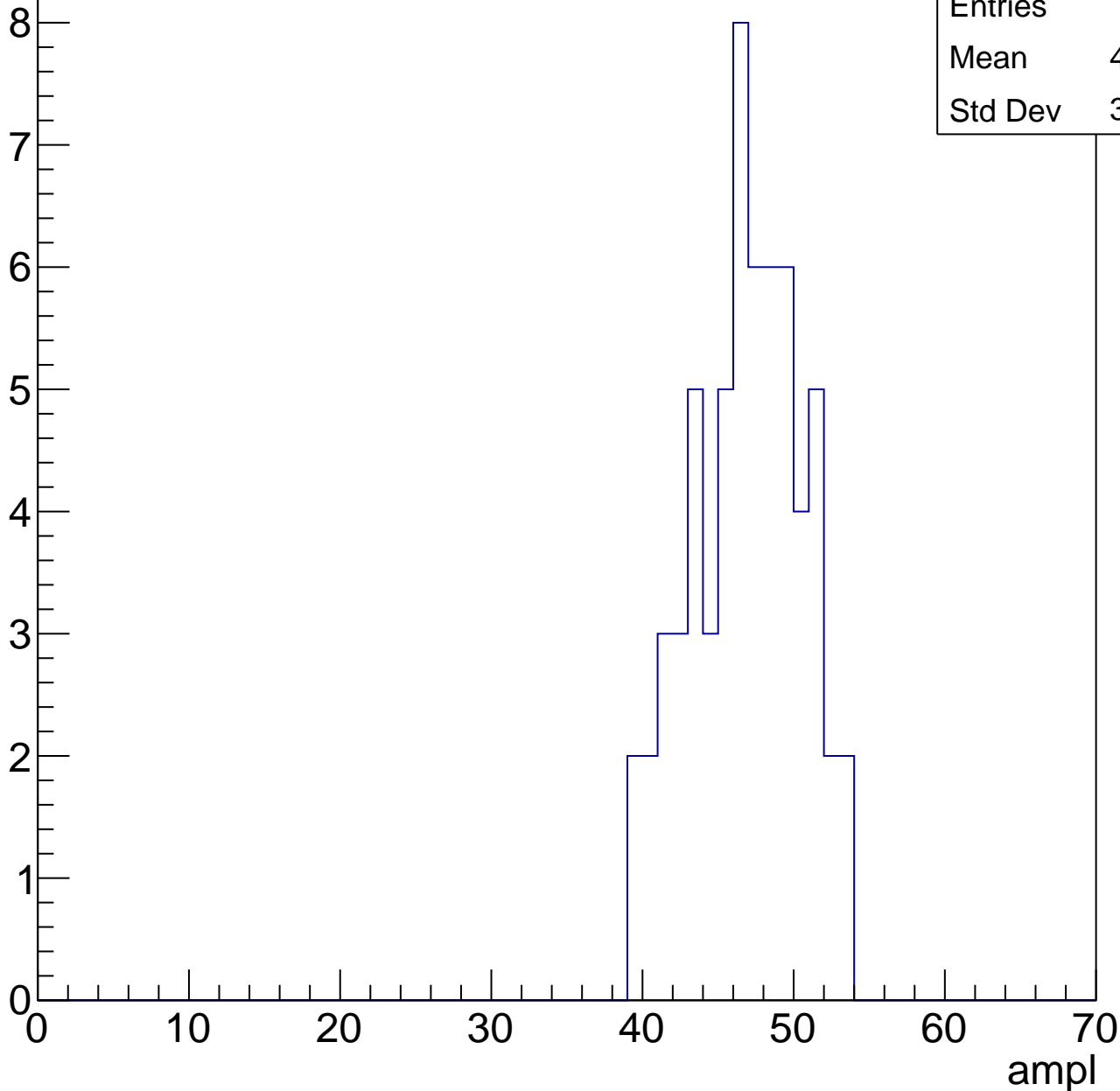


# B1L102S, U3-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

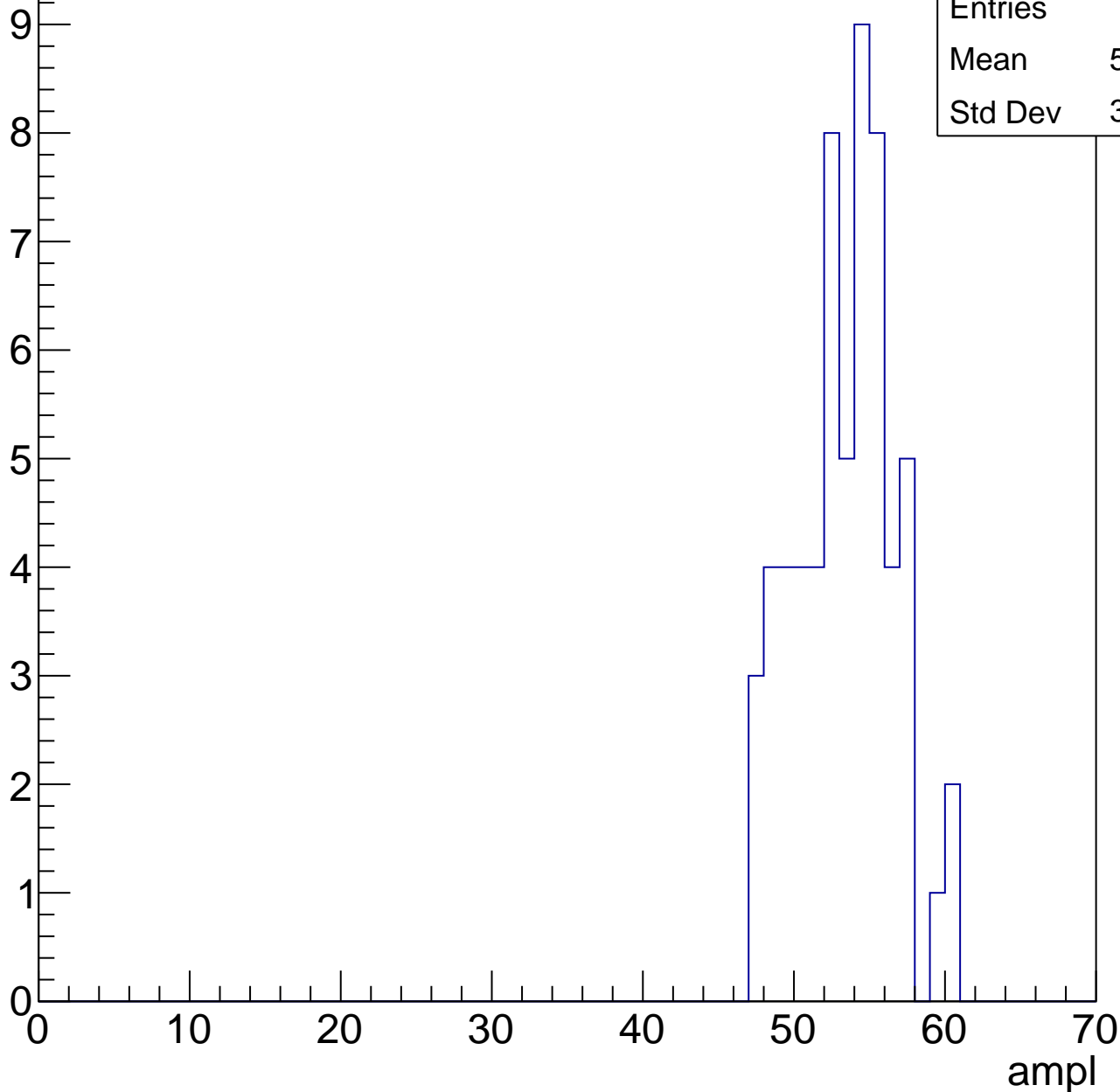
Entries	62
Mean	46.39
Std Dev	3.567



# B1L102S, U3-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

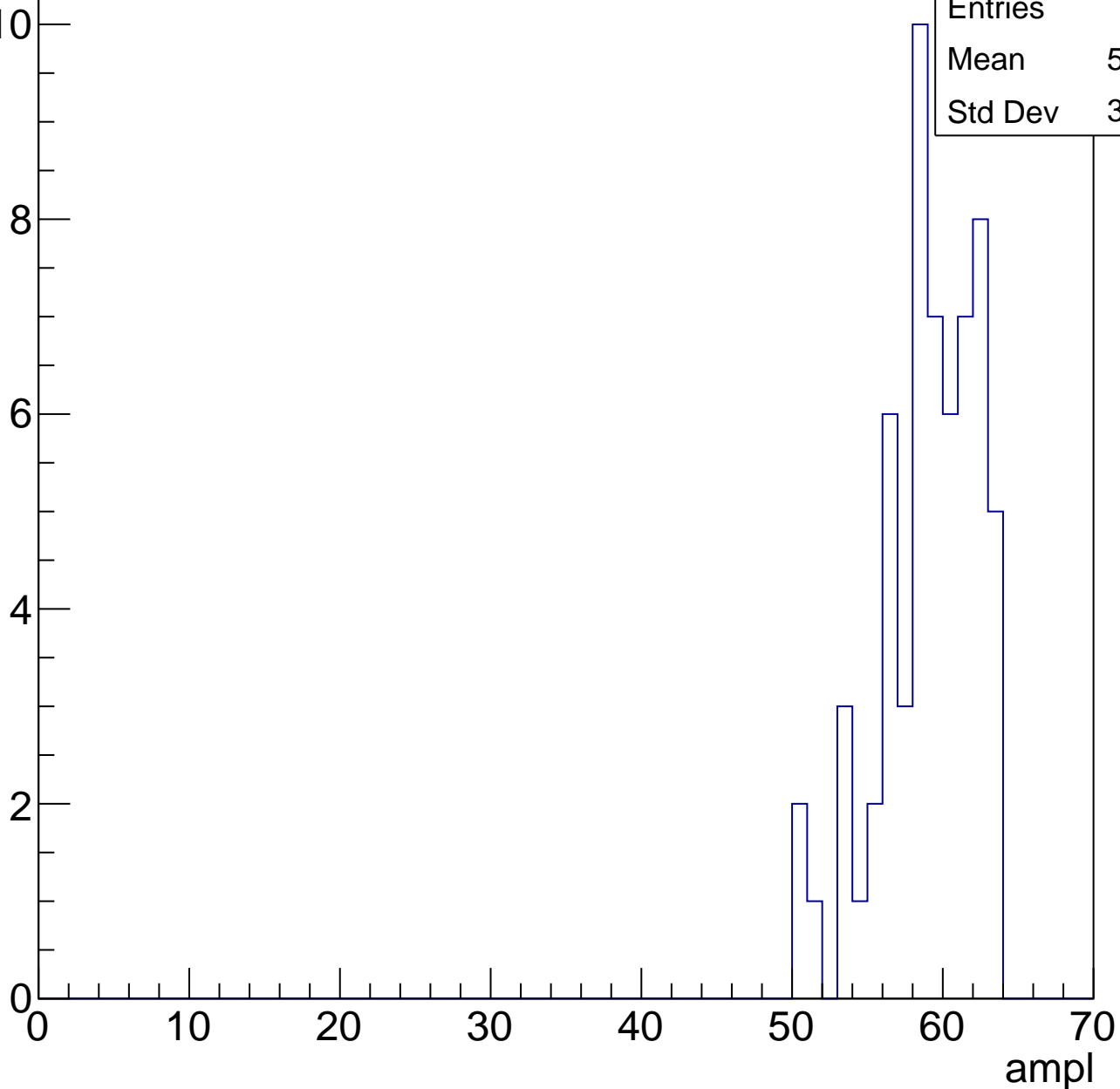


# B1L102S, U3-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

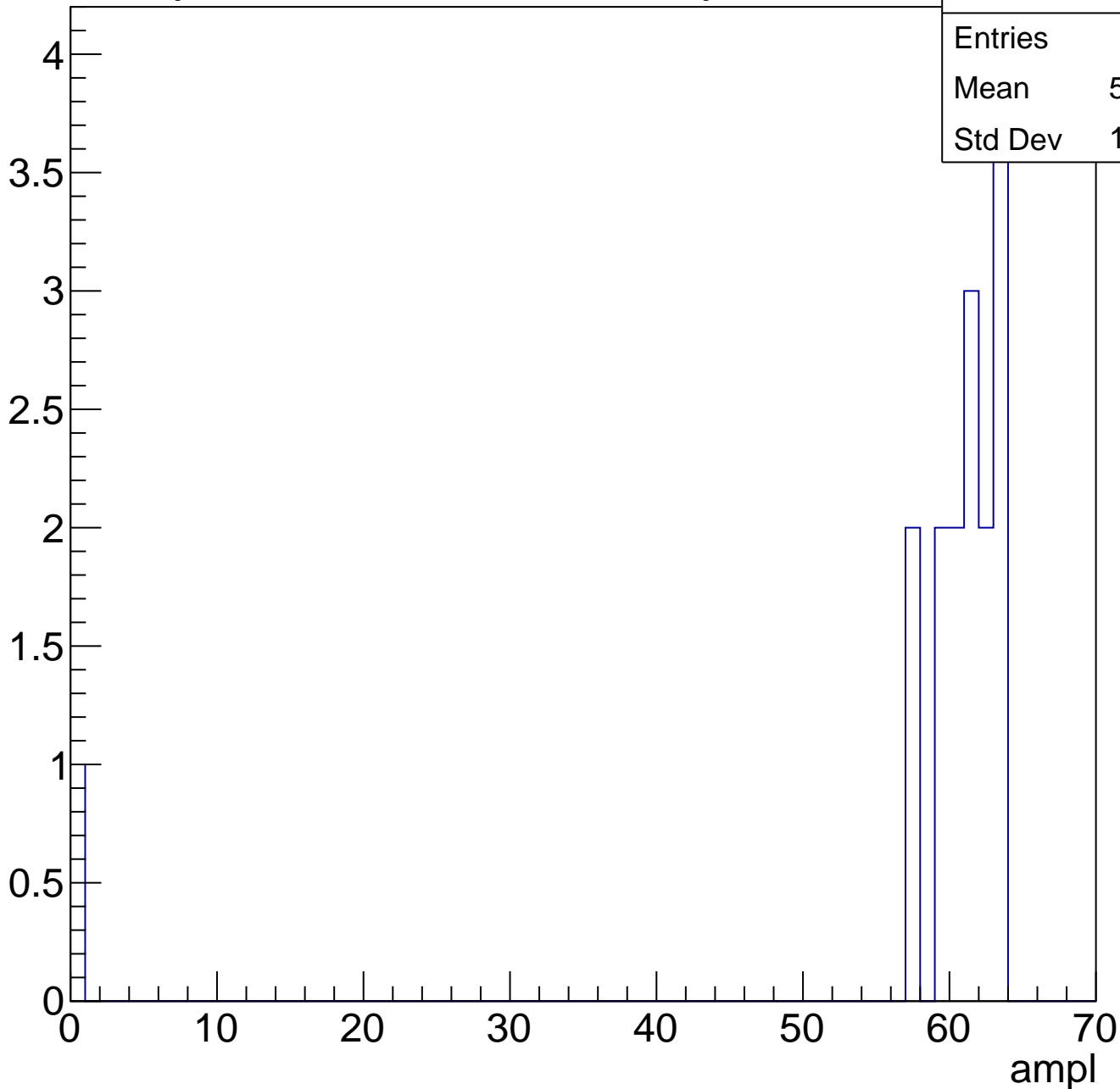
Entries	61
Mean	58.56
Std Dev	3.242



# B1L102S, U3-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch57, adc0

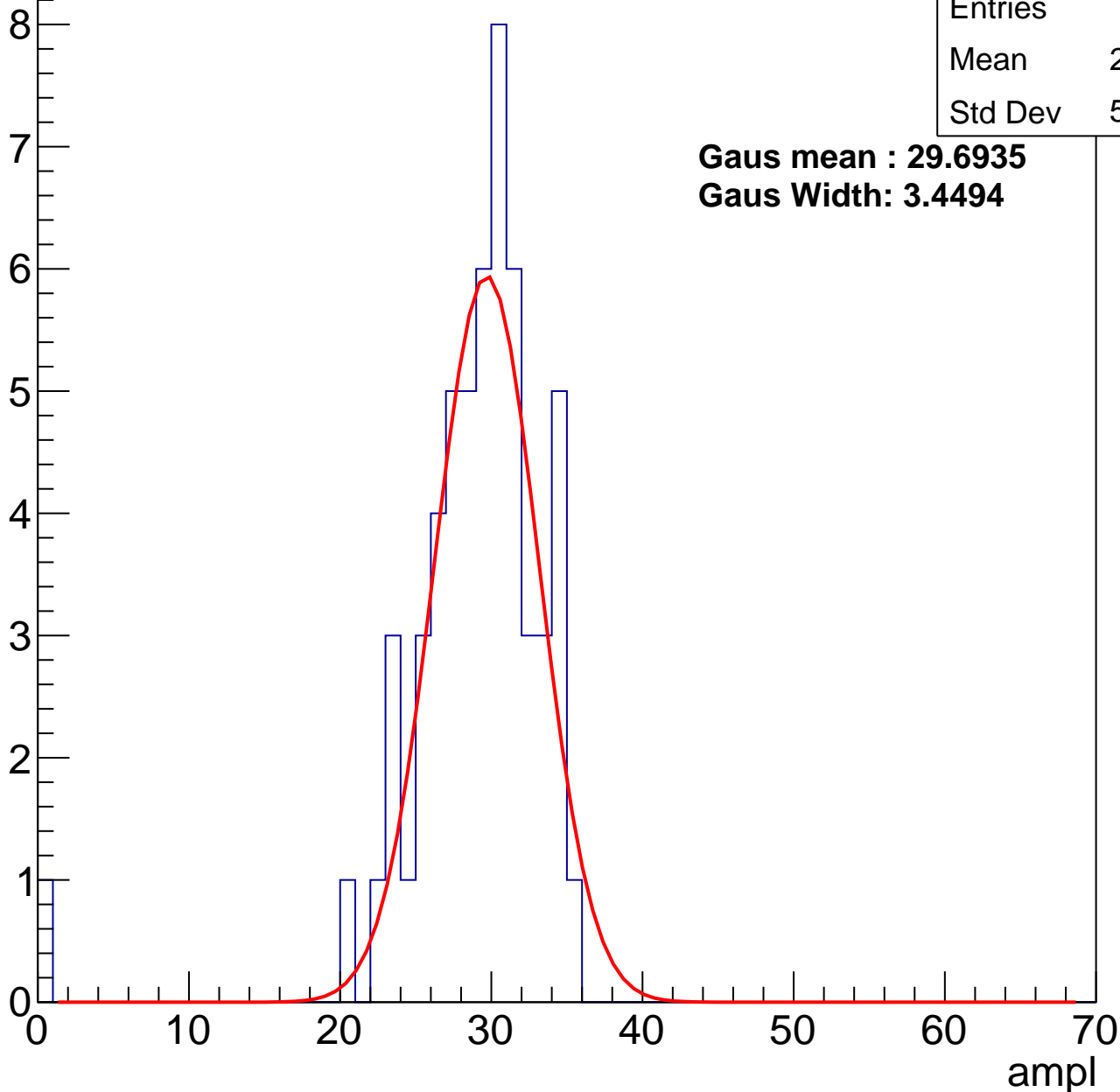
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	28.38
Std Dev	5.104

**Gaus mean : 29.6935**

**Gaus Width: 3.4494**



# B1L102S, U3-ch57, adc1

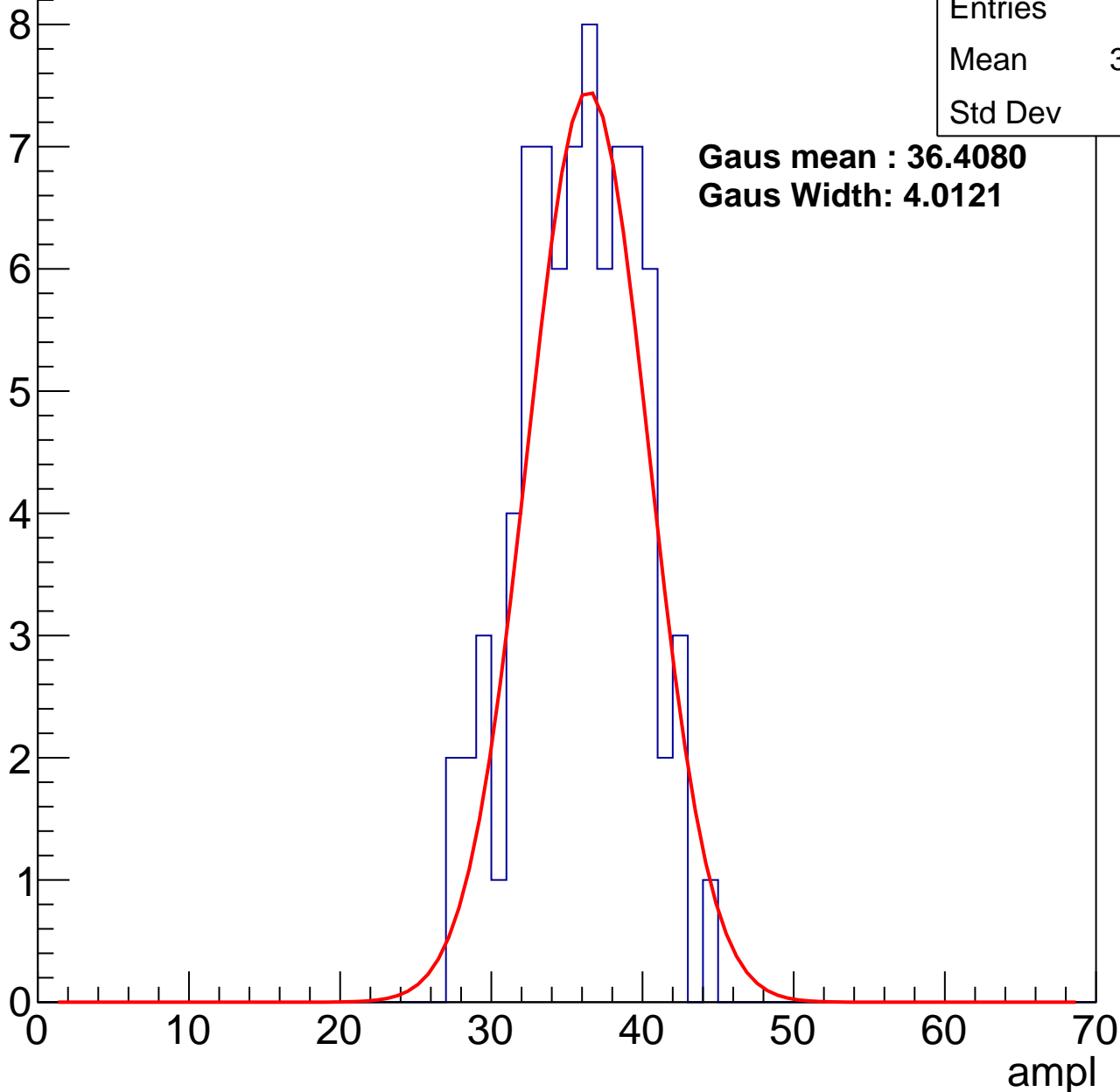
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	35.39
Std Dev	3.84

**Gaus mean : 36.4080**

**Gaus Width: 4.0121**



# B1L102S, U3-ch57, adc2

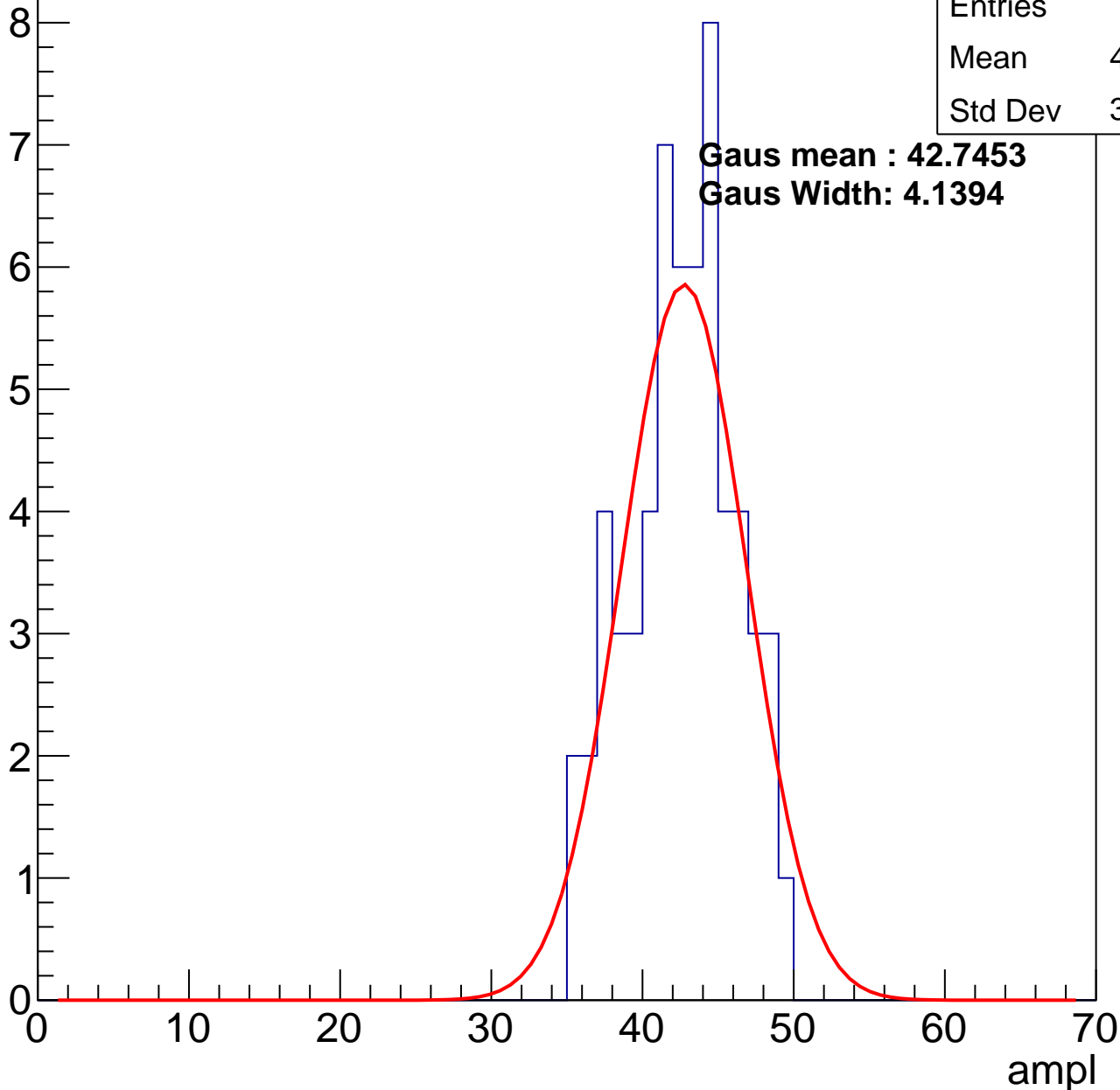
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	42.13
Std Dev	3.505

**Gaus mean : 42.7453**

**Gaus Width: 4.1394**

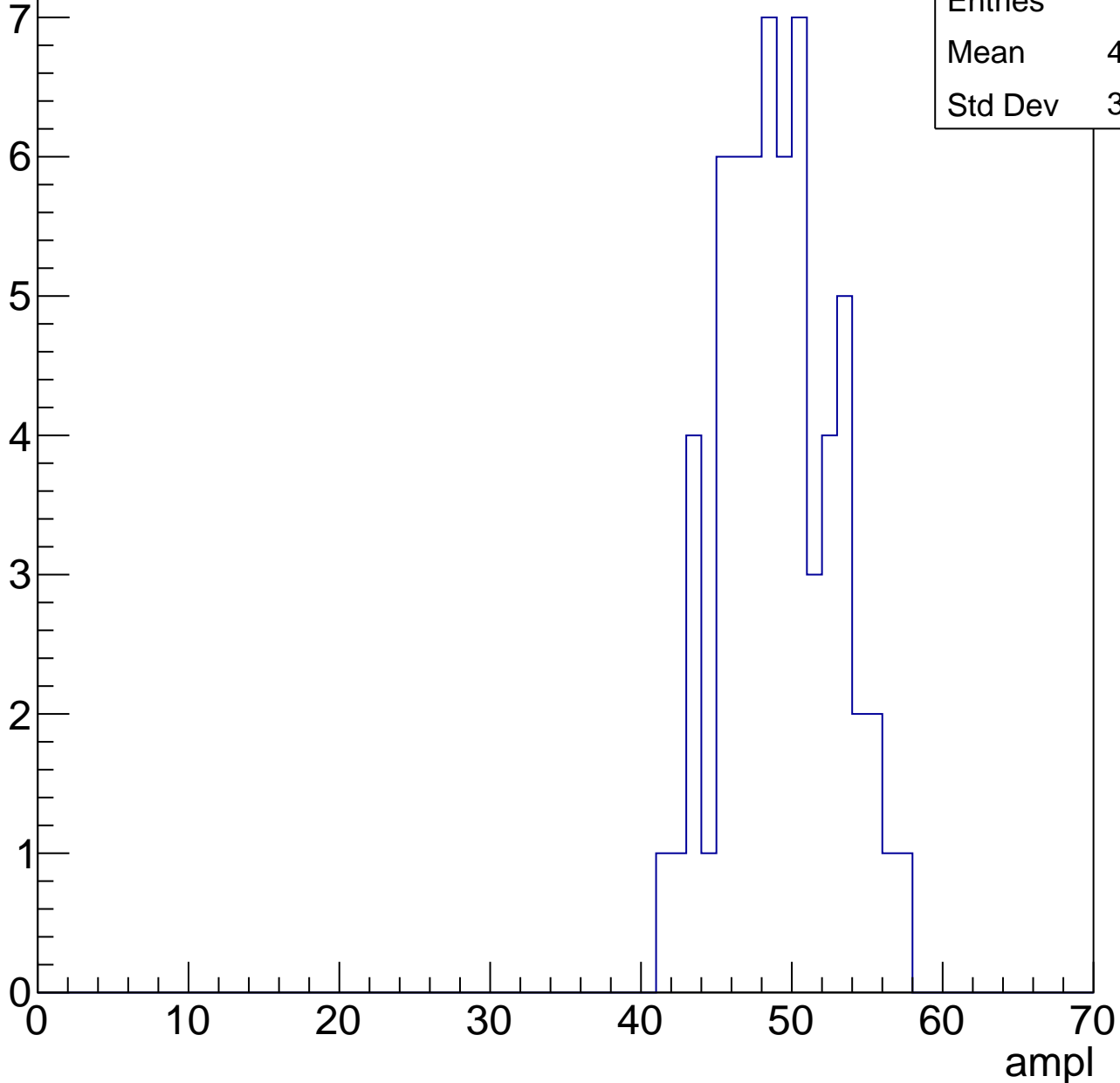


# B1L102S, U3-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	48.63
Std Dev	3.618



# B1L102S, U3-ch57, adc4

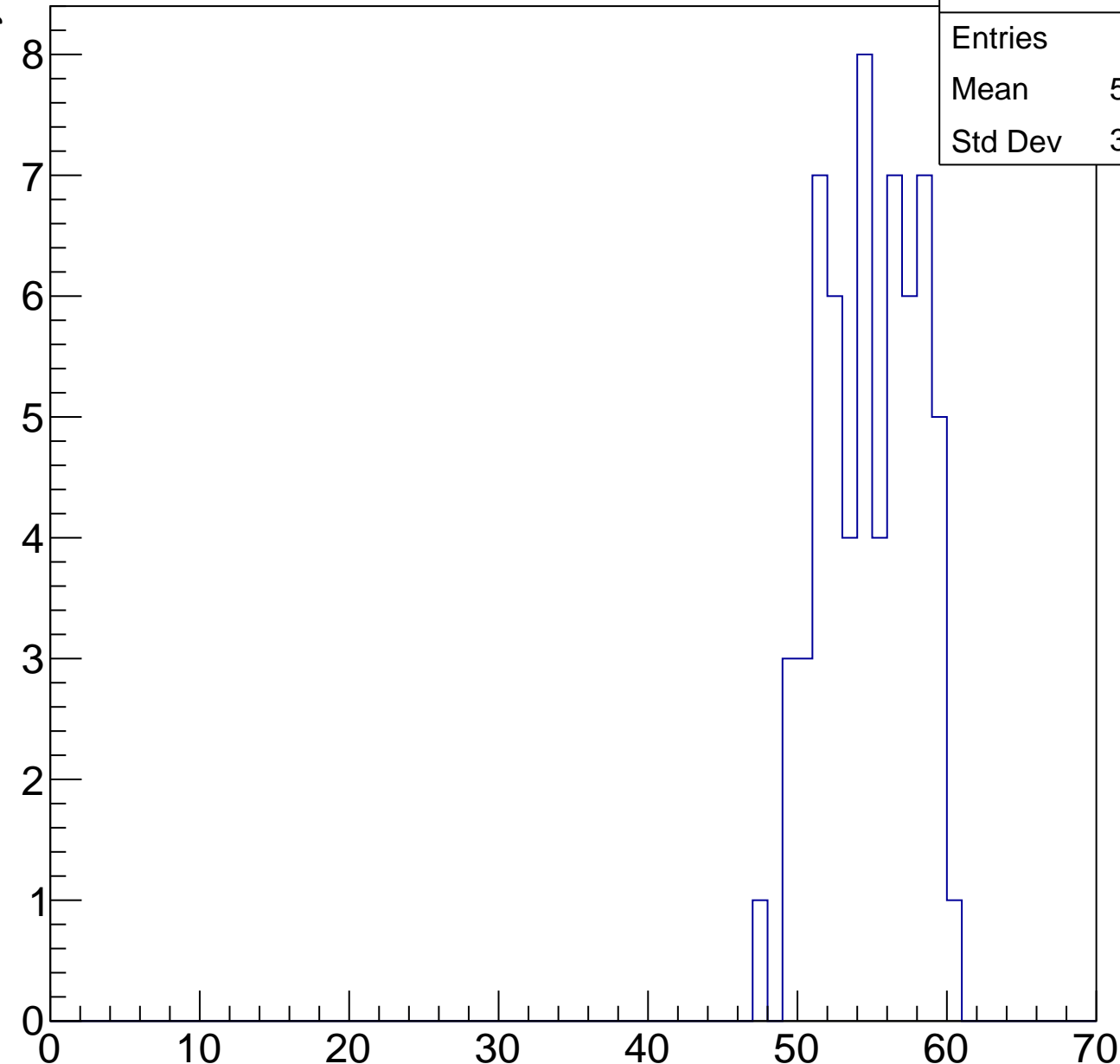
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	62
Mean	54.39
Std Dev	3.144

ampl

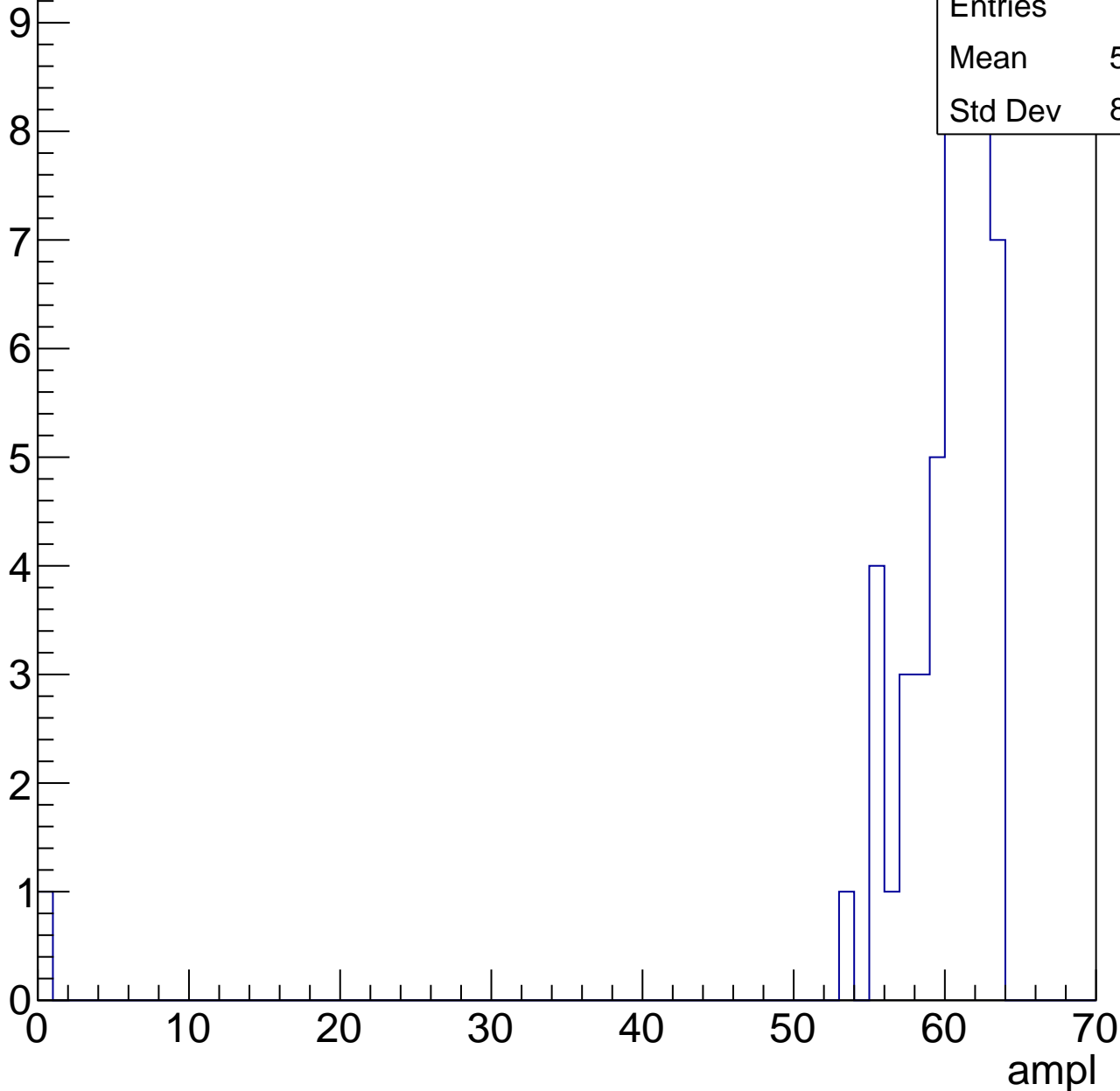


# B1L102S, U3-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

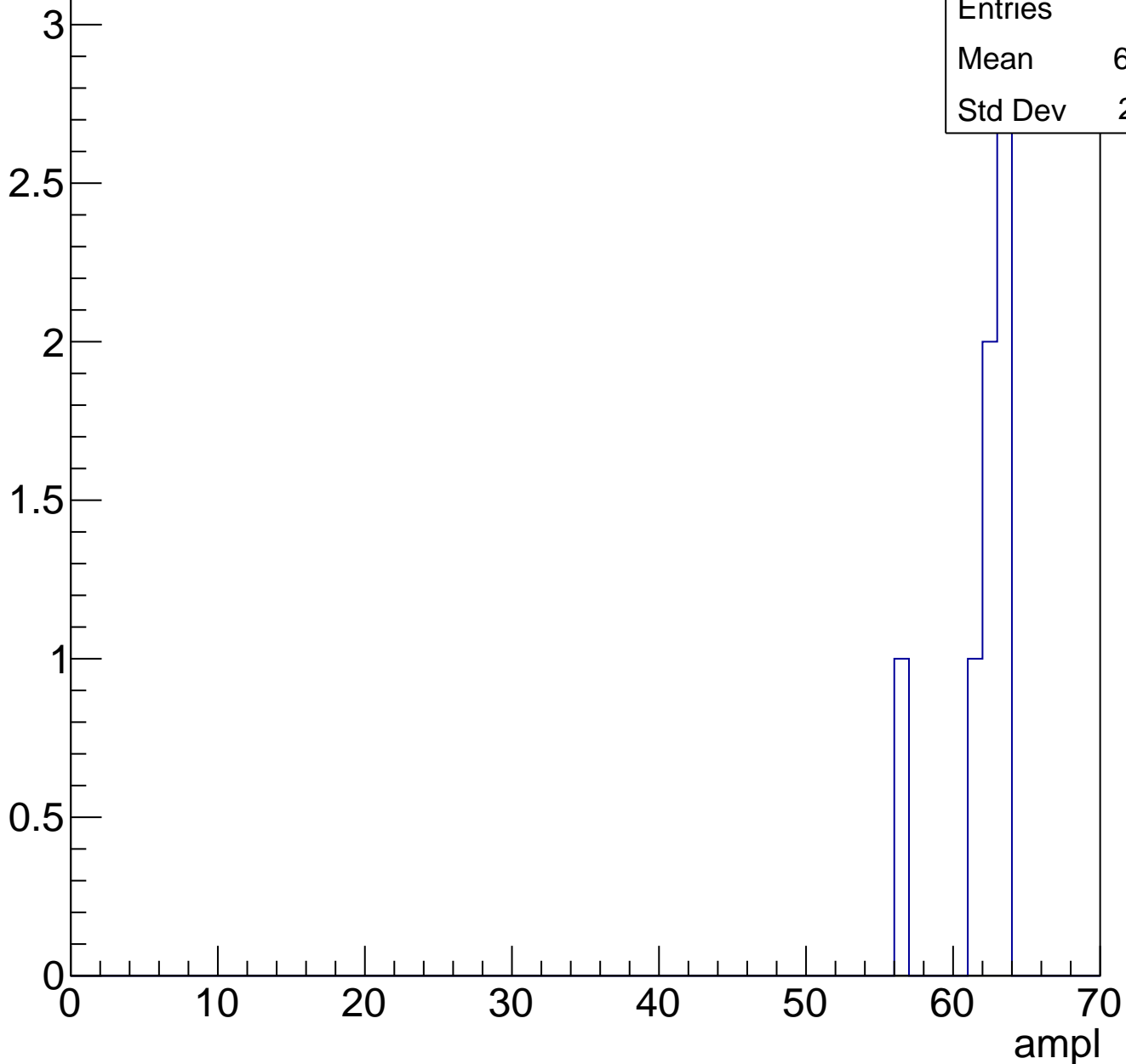
Entries	51
Mean	58.73
Std Dev	8.666



# B1L102S, U3-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U3-ch58, adc0

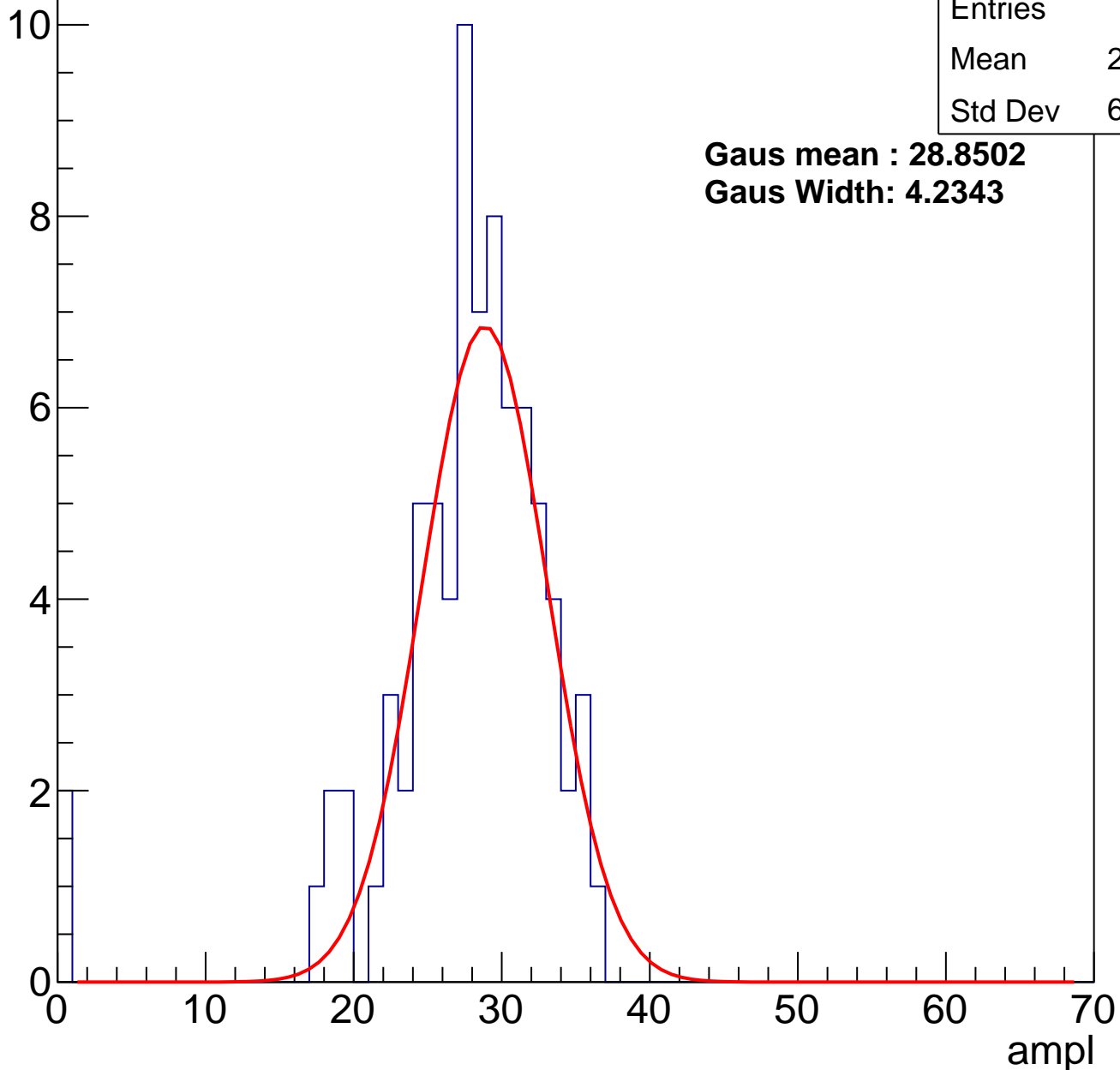
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	79
Mean	27.06
Std Dev	6.047

**Gaus mean : 28.8502**

**Gaus Width: 4.2343**

Entry



# B1L102S, U3-ch58, adc1

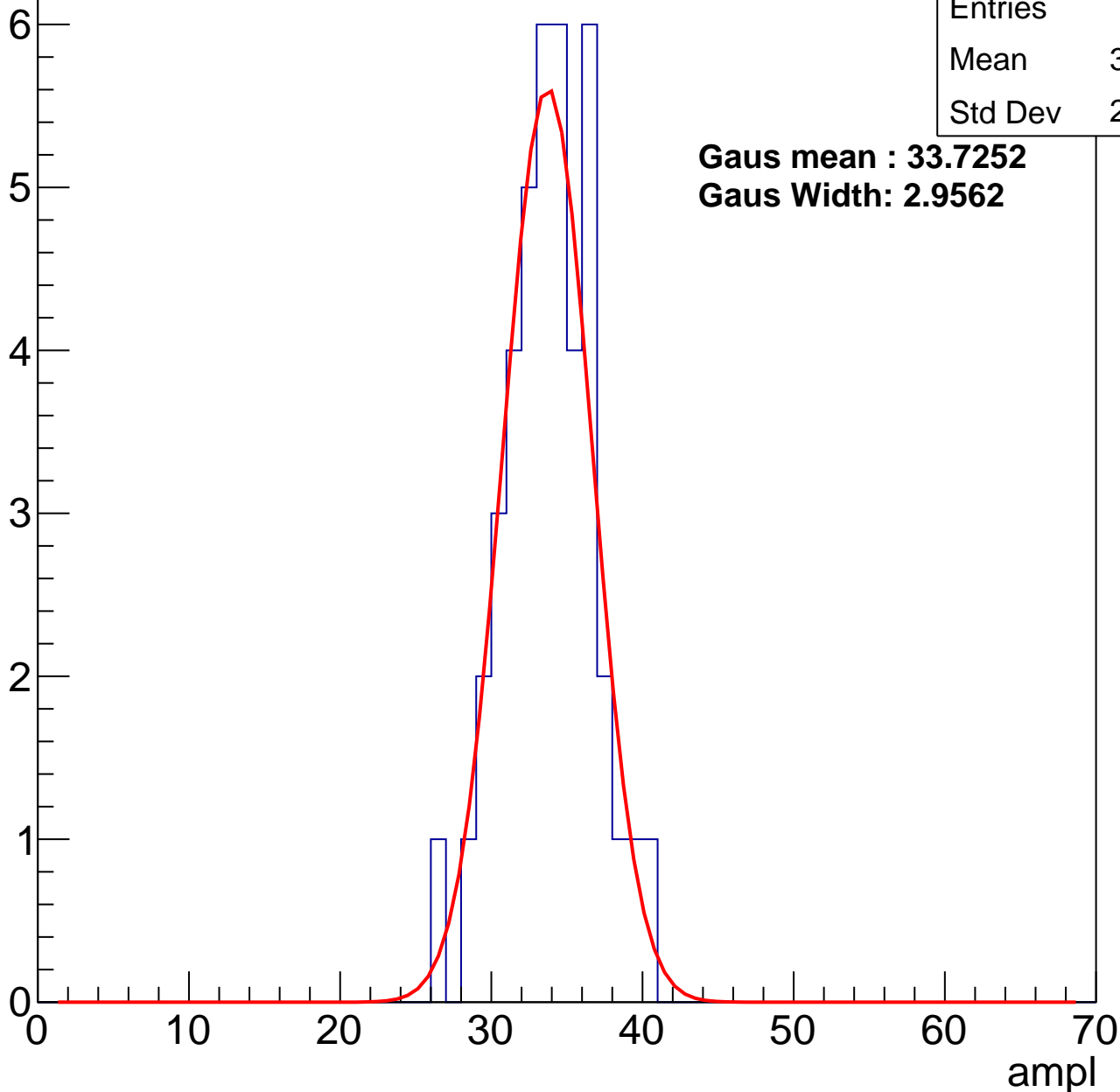
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	43
Mean	33.37
Std Dev	2.918

**Gaus mean : 33.7252**

**Gaus Width: 2.9562**



# B1L102S, U3-ch58, adc2

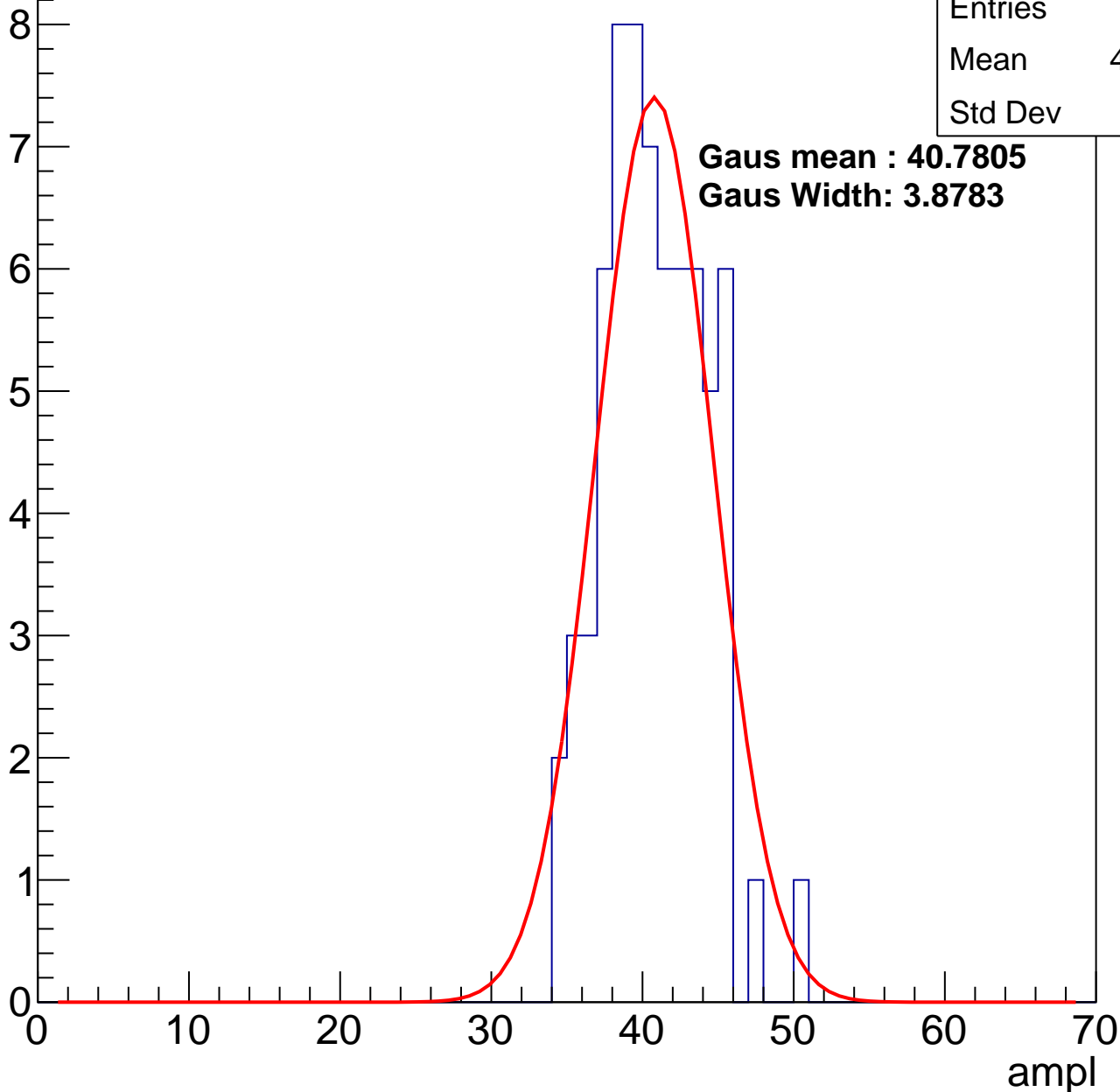
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	40.32
Std Dev	3.31

**Gaus mean : 40.7805**

**Gaus Width: 3.8783**

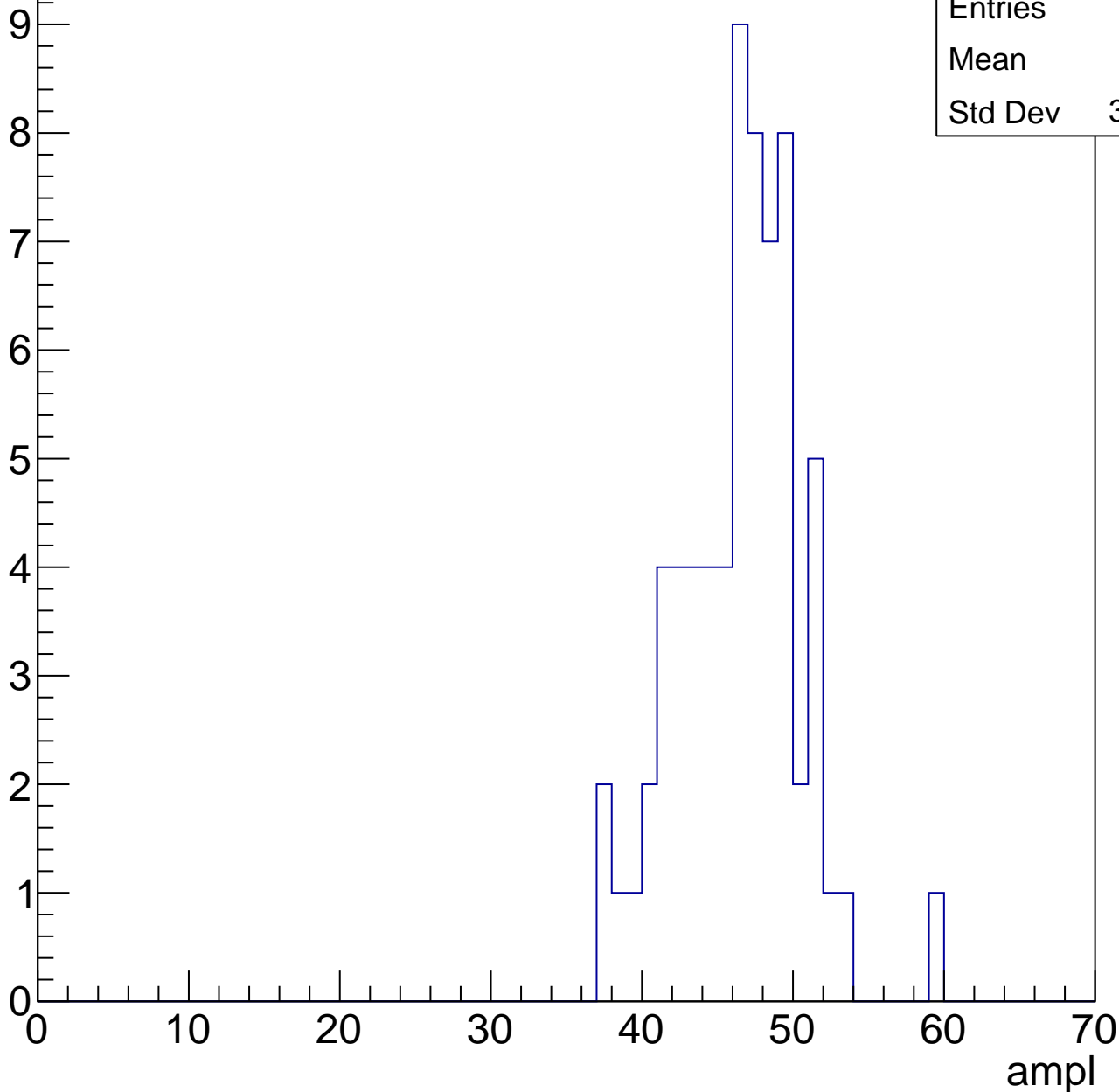


# B1L102S, U3-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	46
Std Dev	3.996

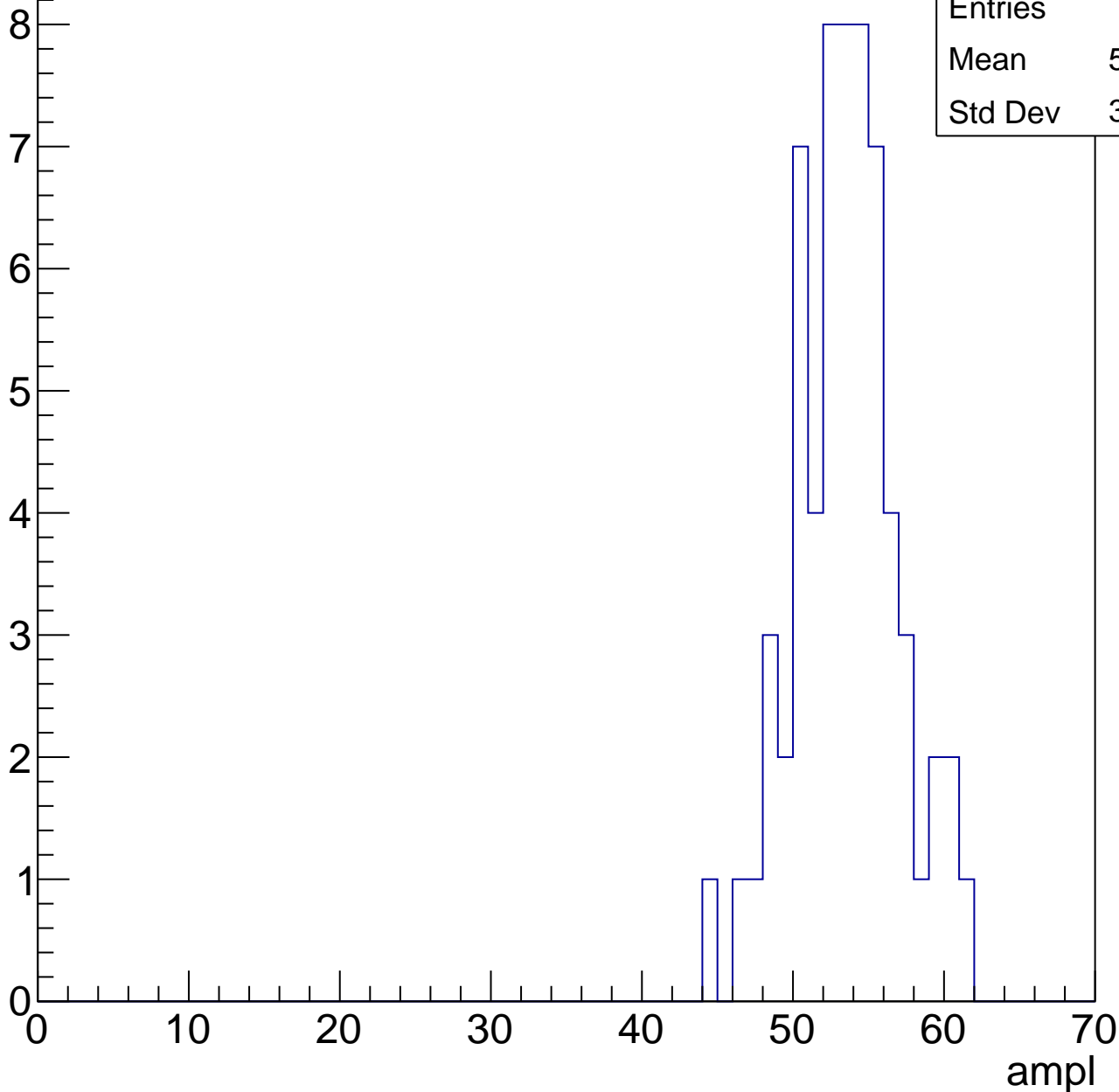


# B1L102S, U3-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

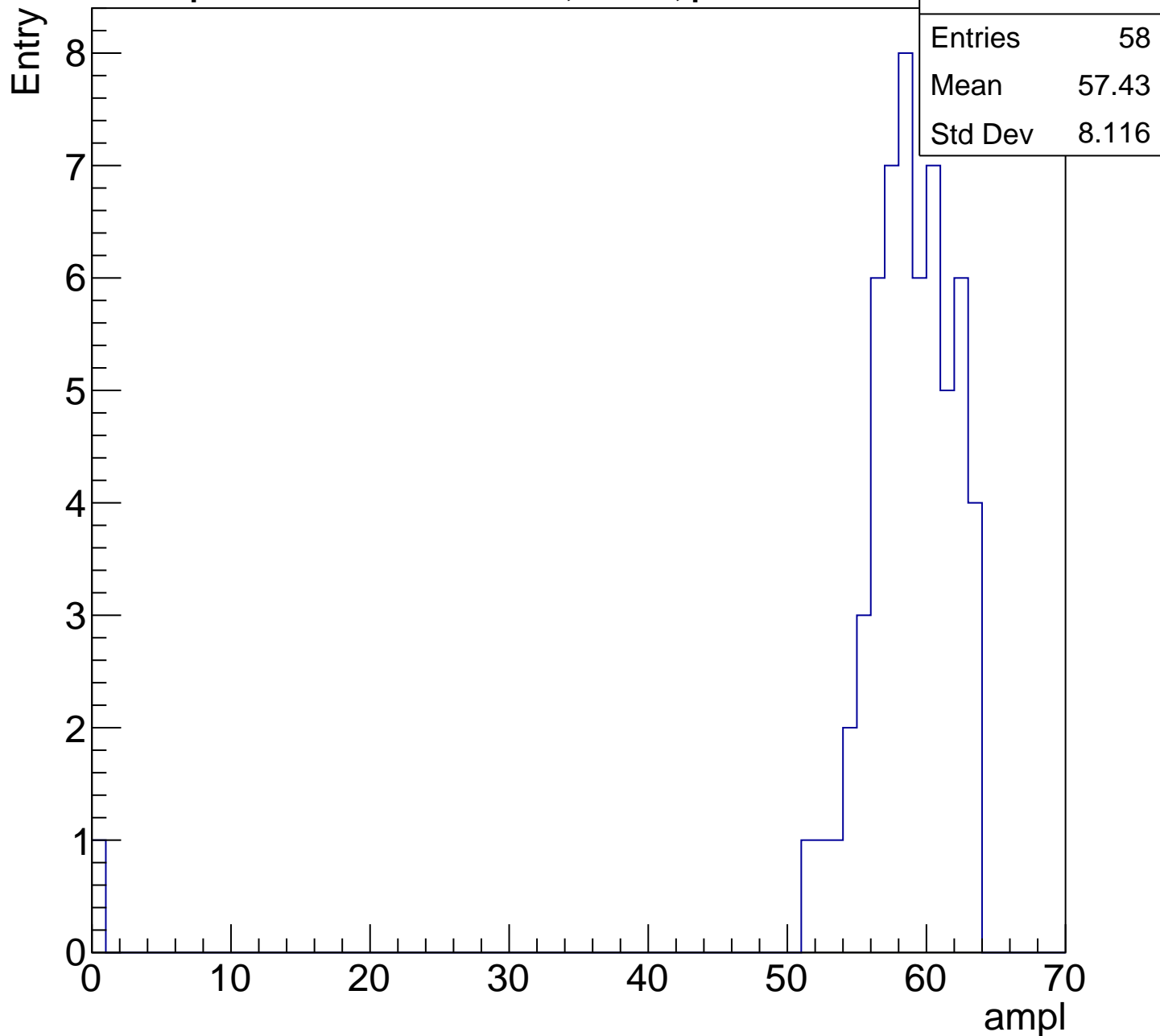
Entry

Entries	63
Mean	53.05
Std Dev	3.425



# B1L102S, U3-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U3-ch58, adc6

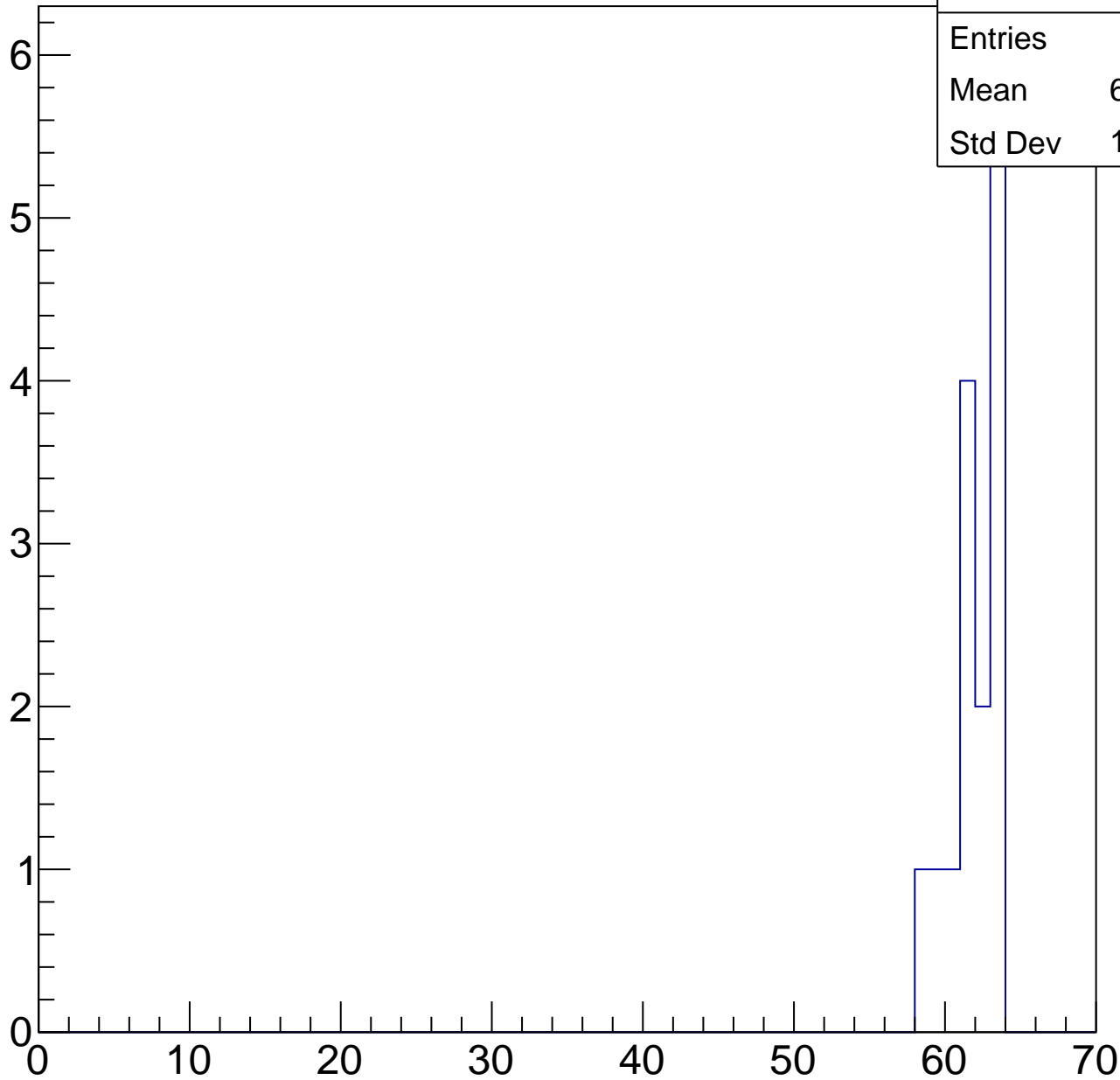
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

6  
5  
4  
3  
2  
1  
0

Entries	15
Mean	61.53
Std Dev	1.543

ampl





# B1L102S, U3-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch59, adc0

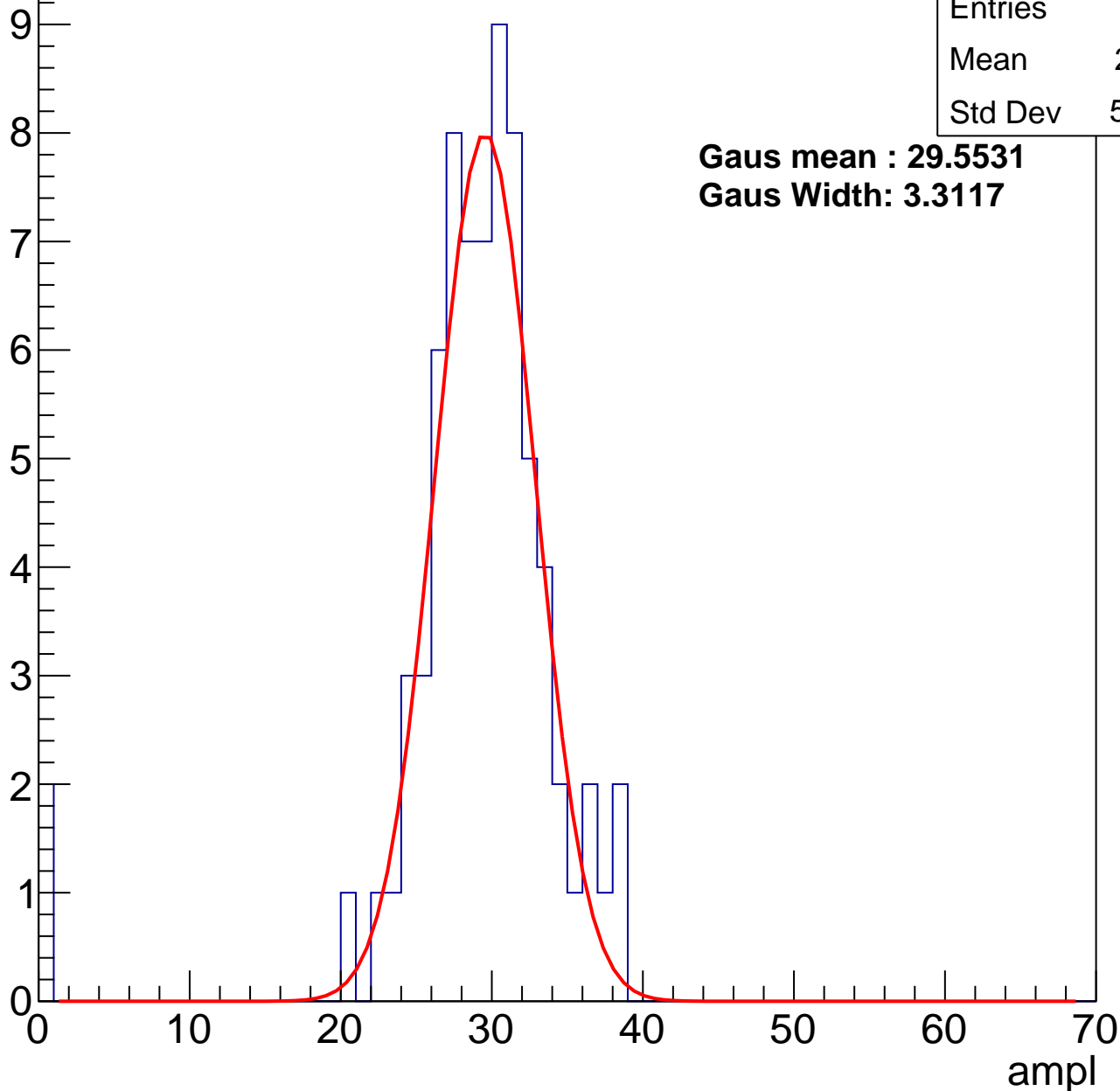
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	28.51
Std Dev	5.975

**Gaus mean : 29.5531**

**Gaus Width: 3.3117**



# B1L102S, U3-ch59, adc1

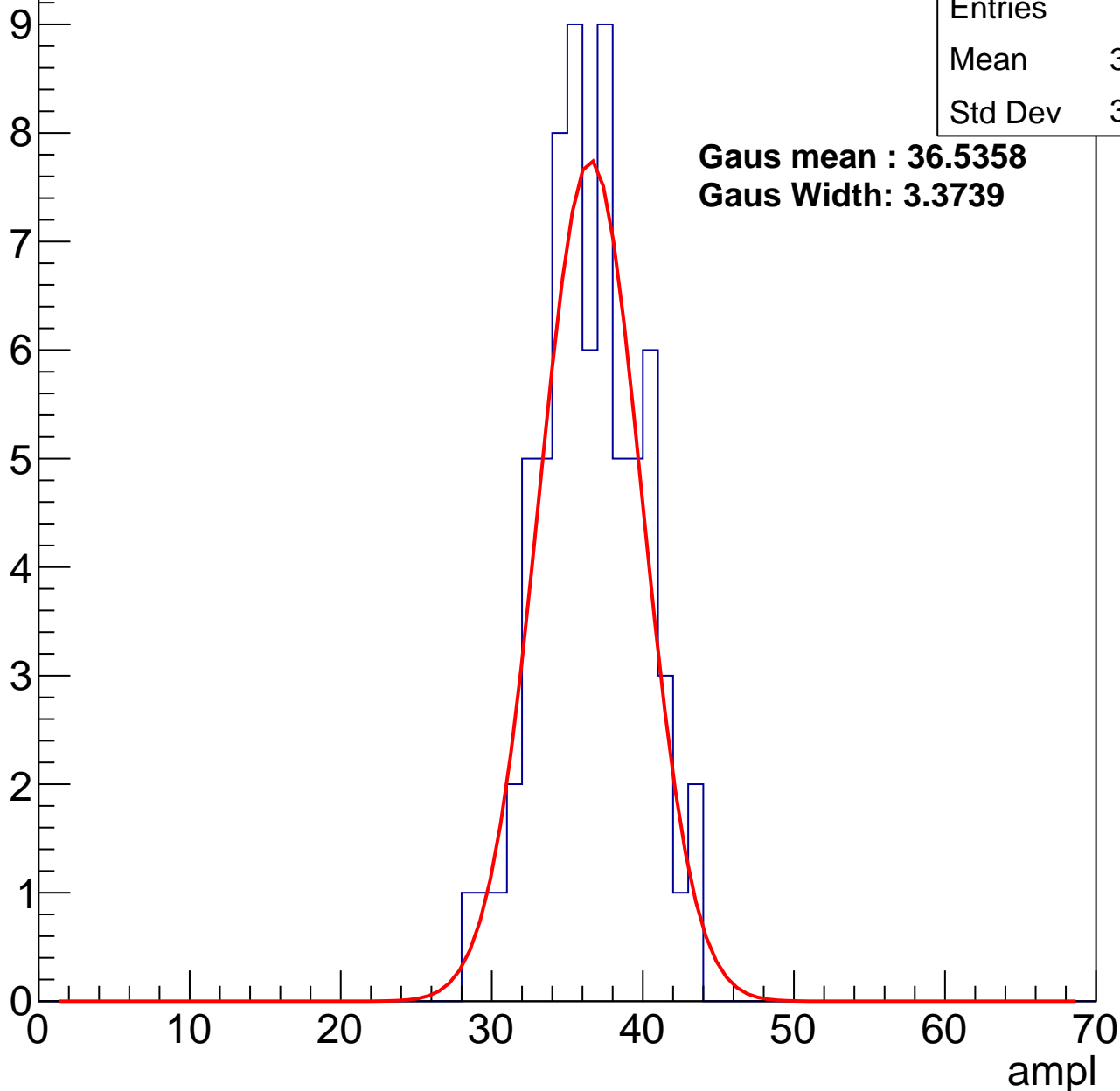
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	36.03
Std Dev	3.284

**Gaus mean : 36.5358**

**Gaus Width: 3.3739**



# B1L102S, U3-ch59, adc2

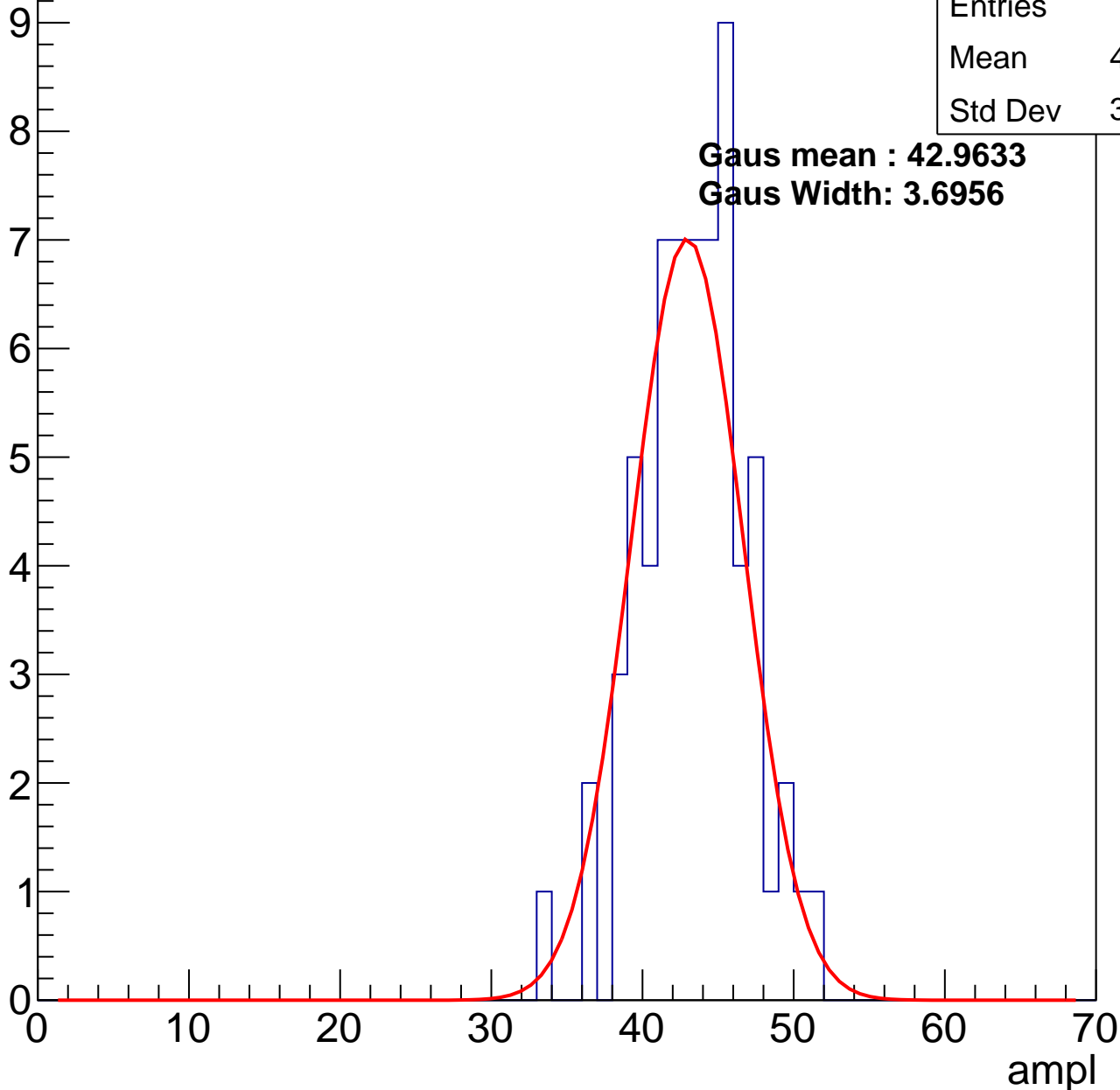
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	42.95
Std Dev	3.466

**Gaus mean : 42.9633**

**Gaus Width: 3.6956**

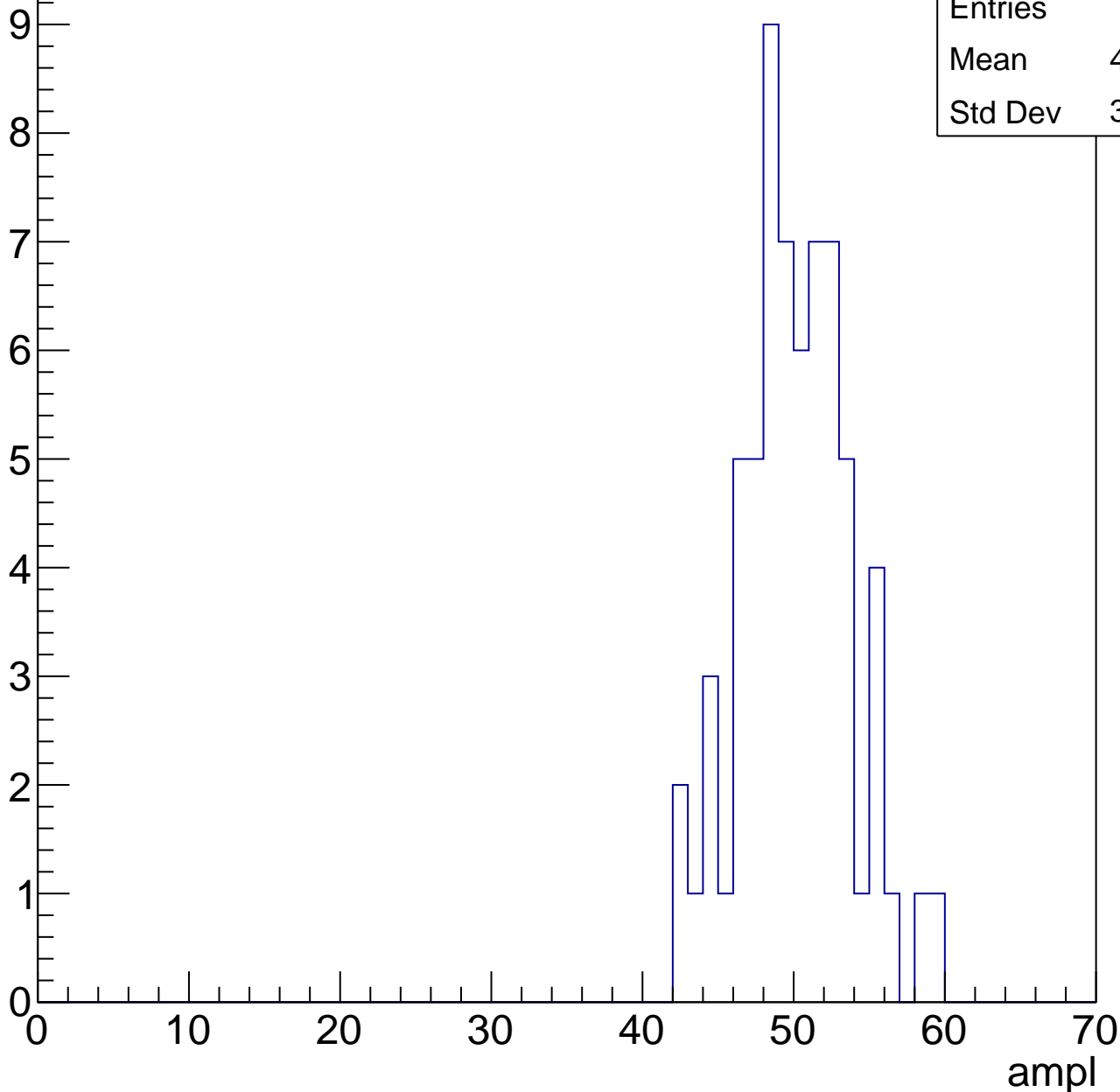


# B1L102S, U3-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

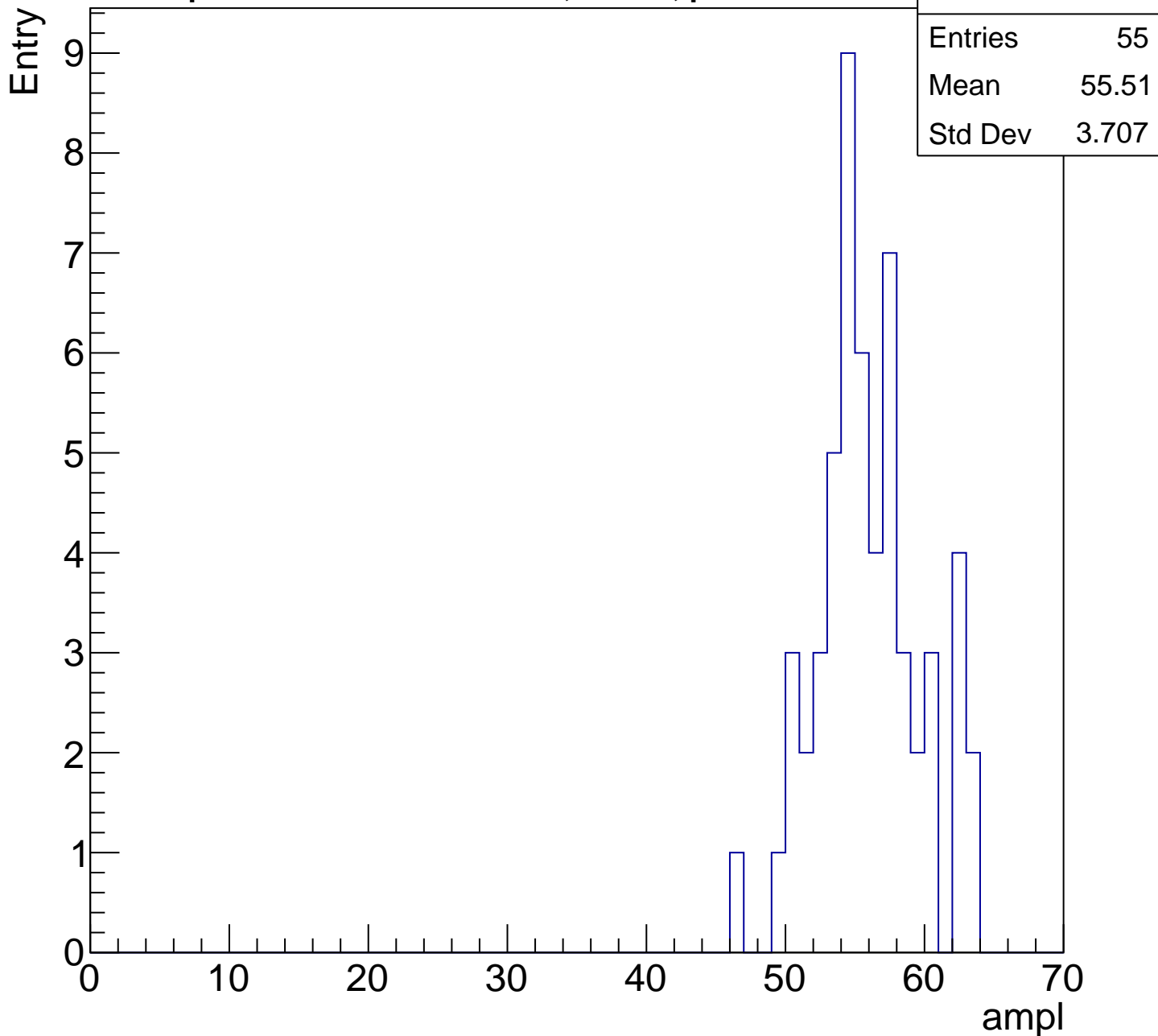
Entry

Entries	66
Mean	49.65
Std Dev	3.582



# B1L102S, U3-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

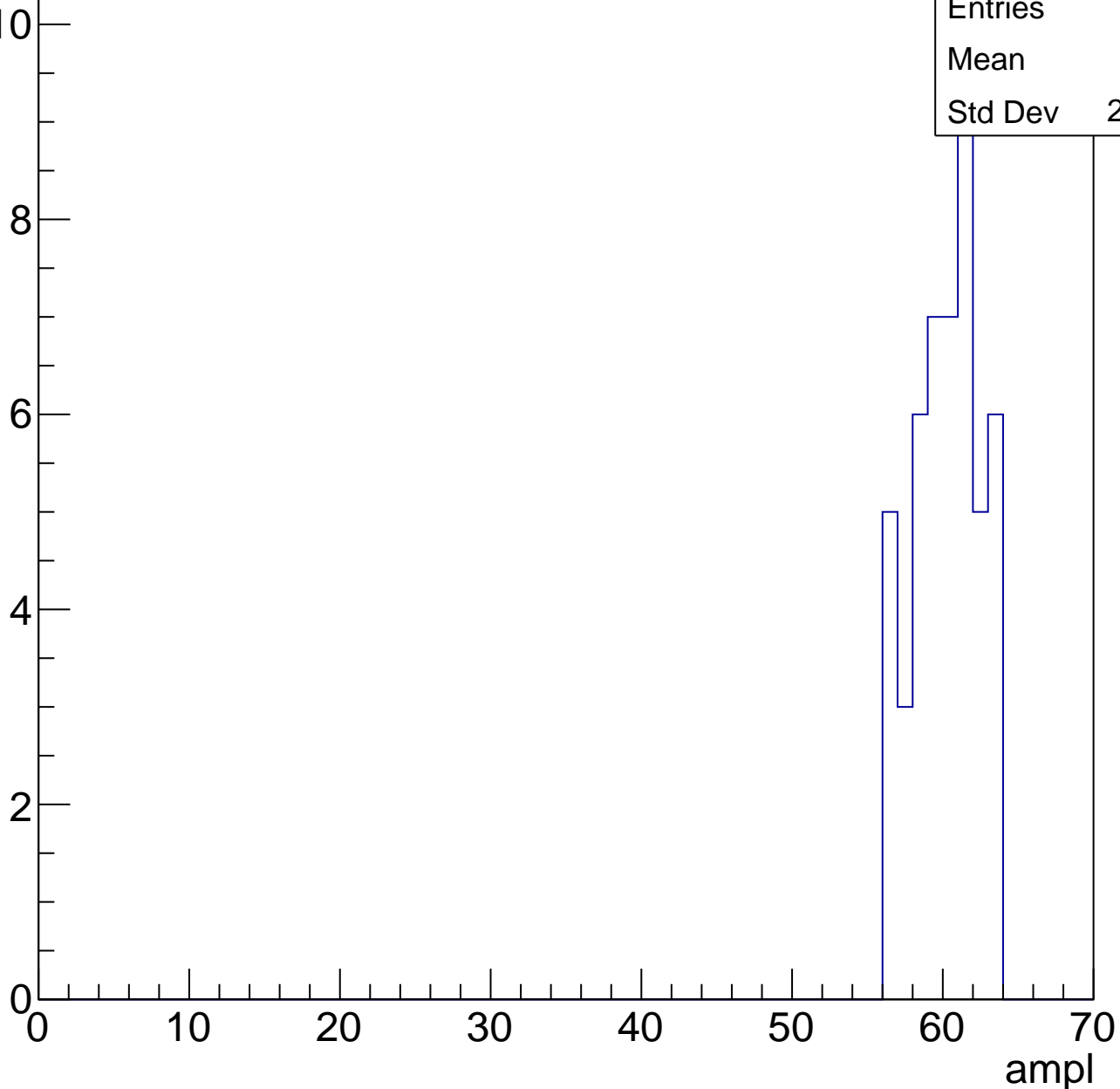


# B1L102S, U3-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	59.8
Std Dev	2.119



# B1L102S, U3-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	19
Std Dev	0

ampl

# B1L102S, U3-ch60, adc0

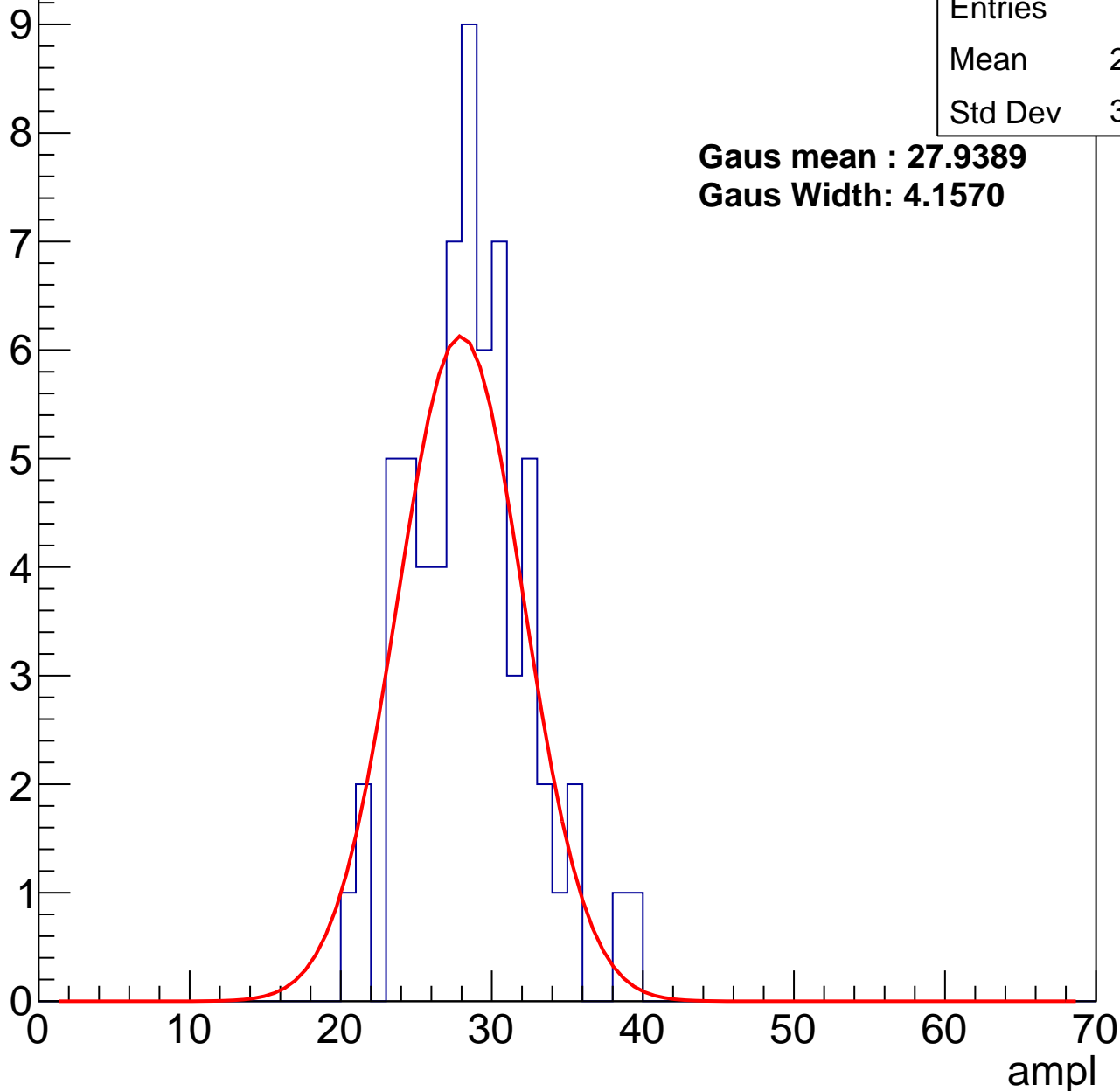
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	28.09
Std Dev	3.866

**Gaus mean : 27.9389**

**Gaus Width: 4.1570**



# B1L102S, U3-ch60, adc1

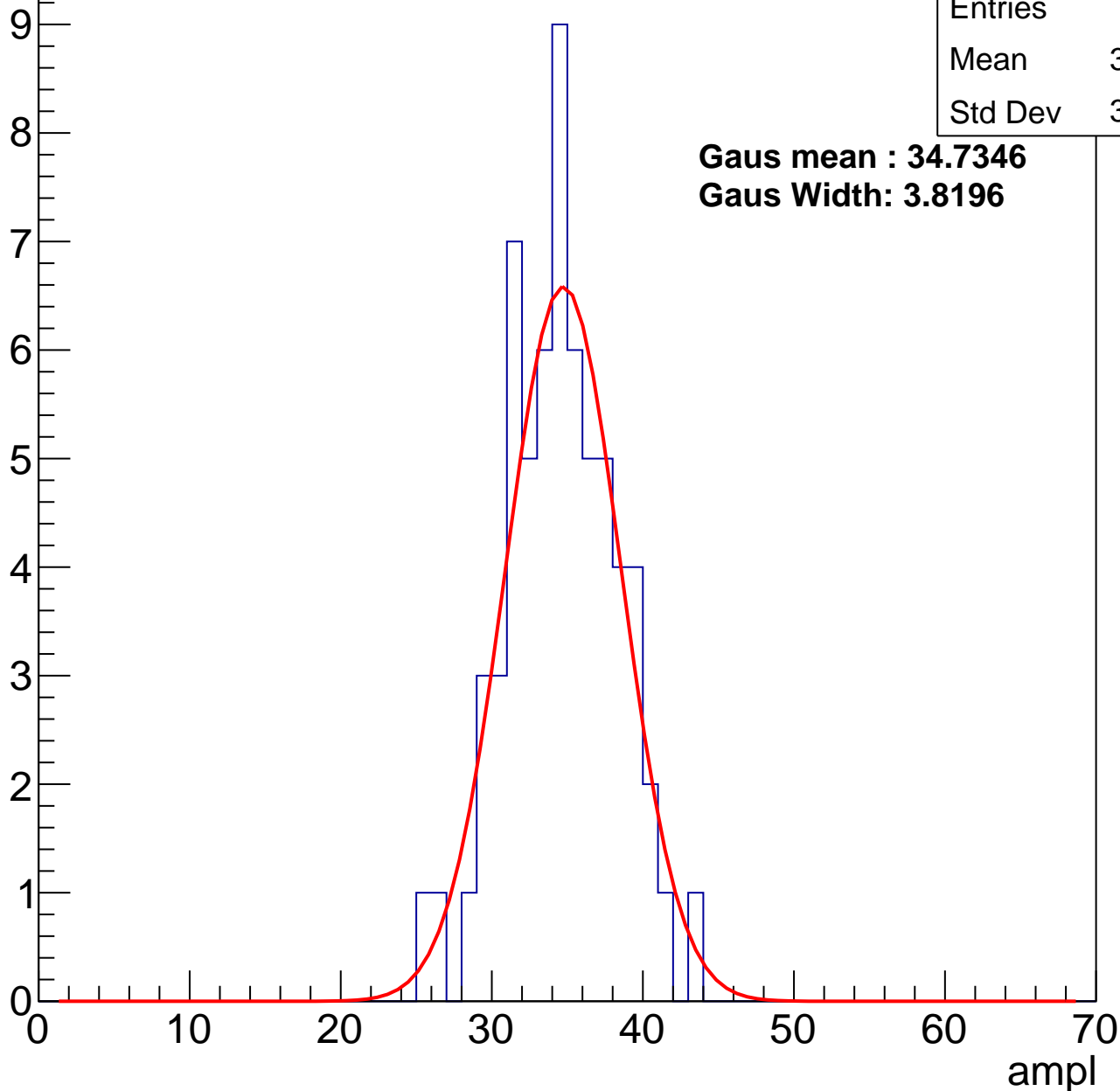
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	34.12
Std Dev	3.599

**Gaus mean : 34.7346**

**Gaus Width: 3.8196**



# B1L102S, U3-ch60, adc2

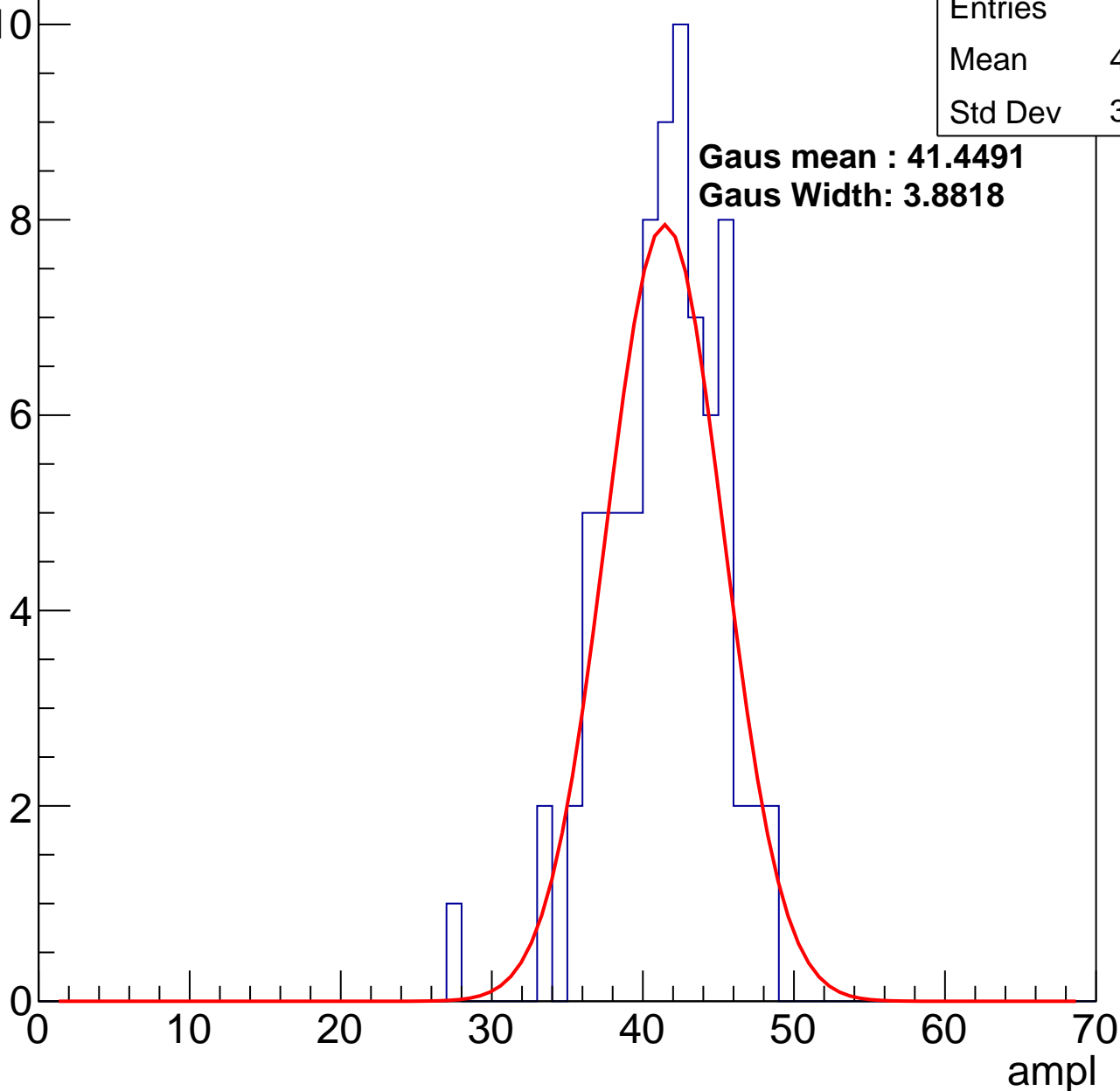
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	40.87
Std Dev	3.753

**Gaus mean : 41.4491**

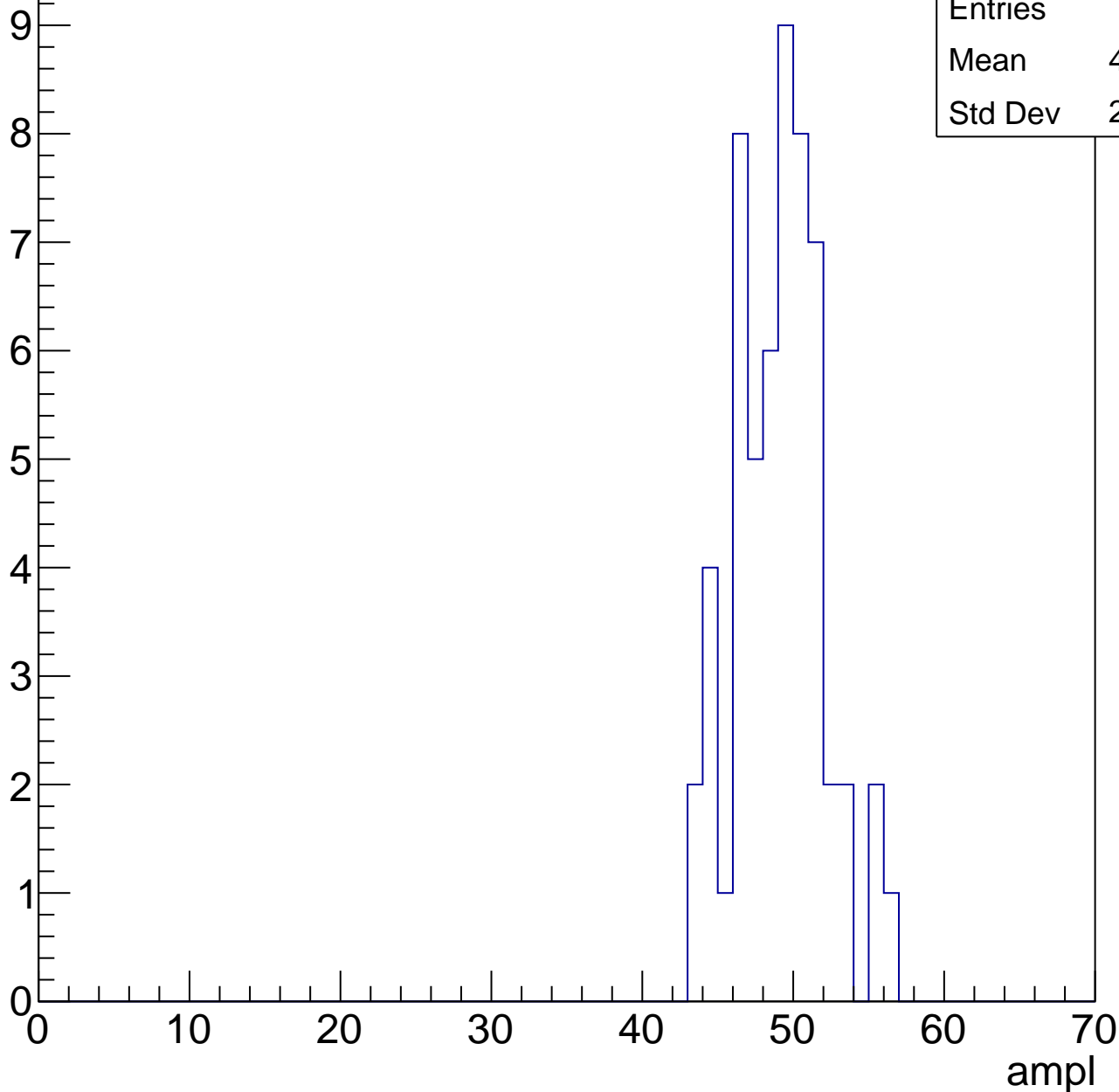
**Gaus Width: 3.8818**



# B1L102S, U3-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

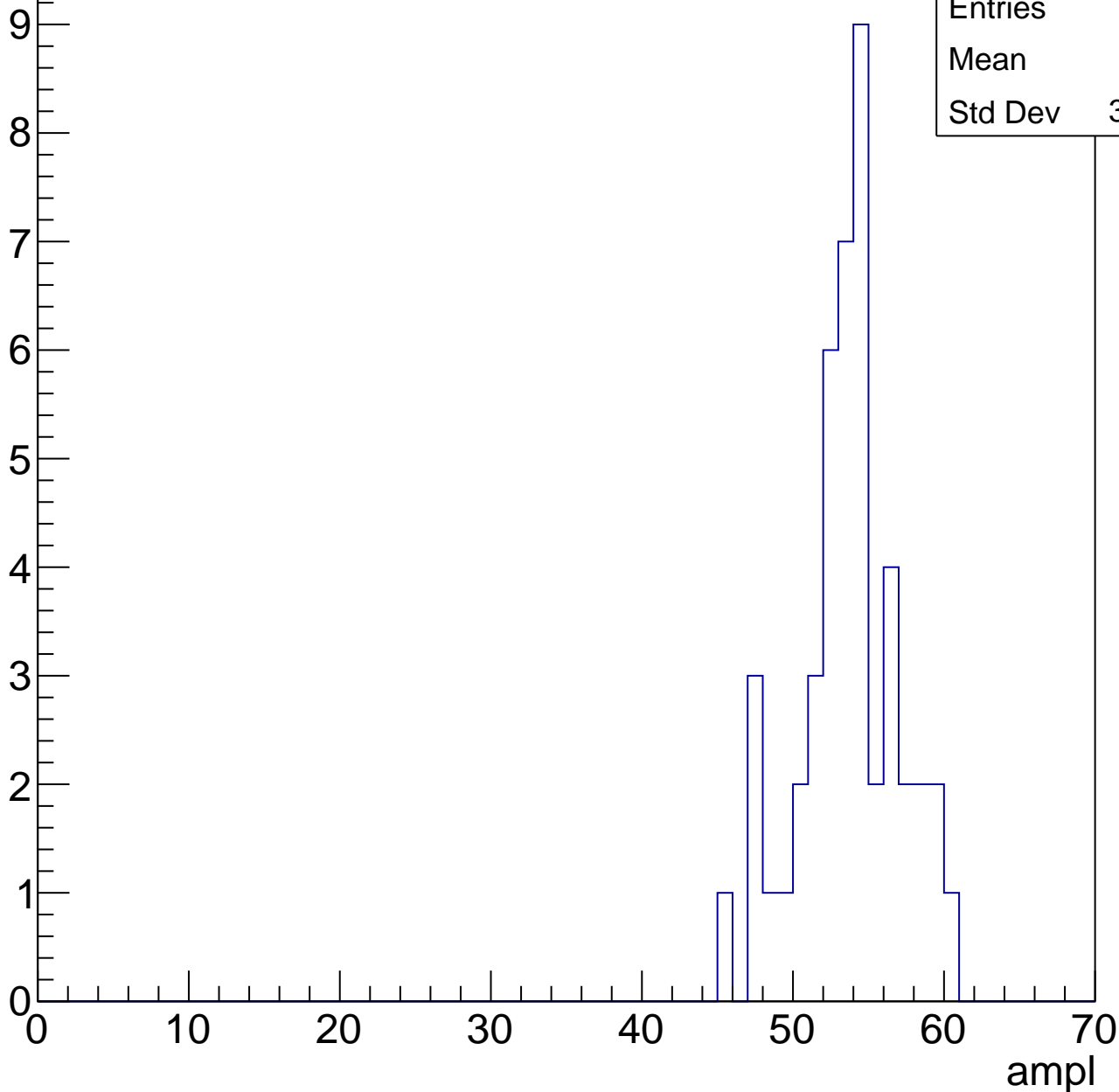


# B1L102S, U3-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	53.2
Std Dev	3.308

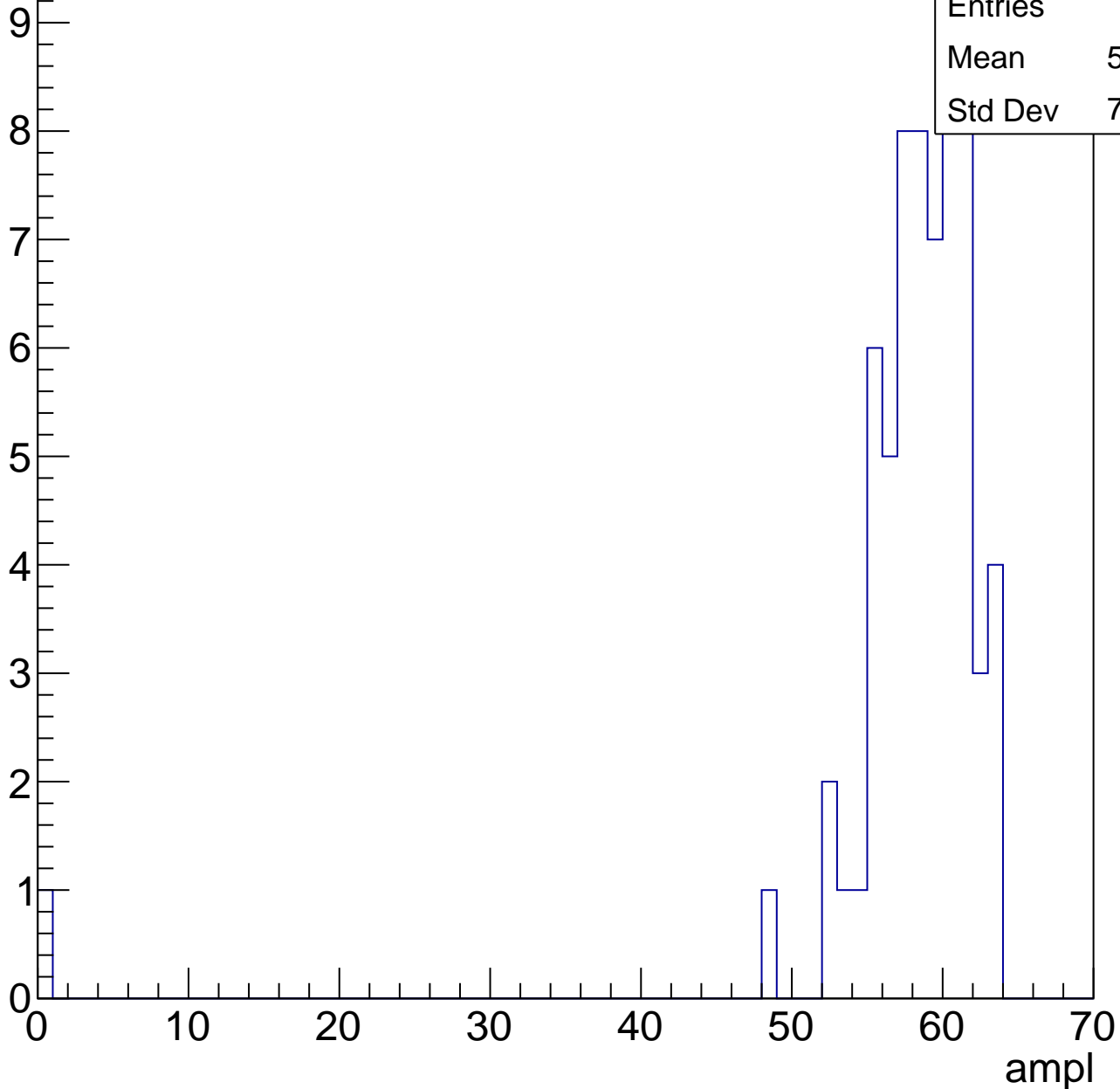


# B1L102S, U3-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	57.33
Std Dev	7.804

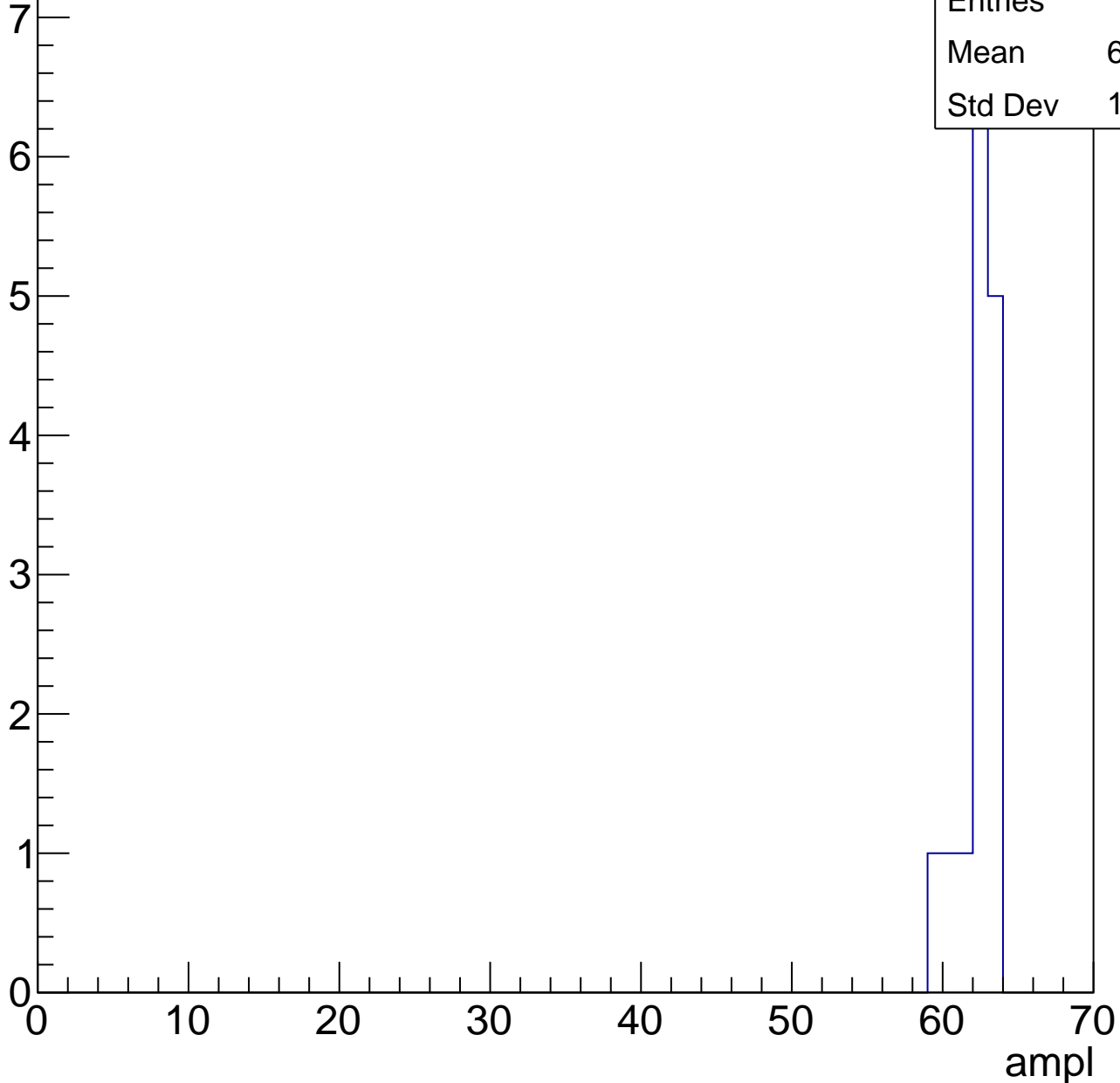


# B1L102S, U3-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	15
Mean	61.93
Std Dev	1.123

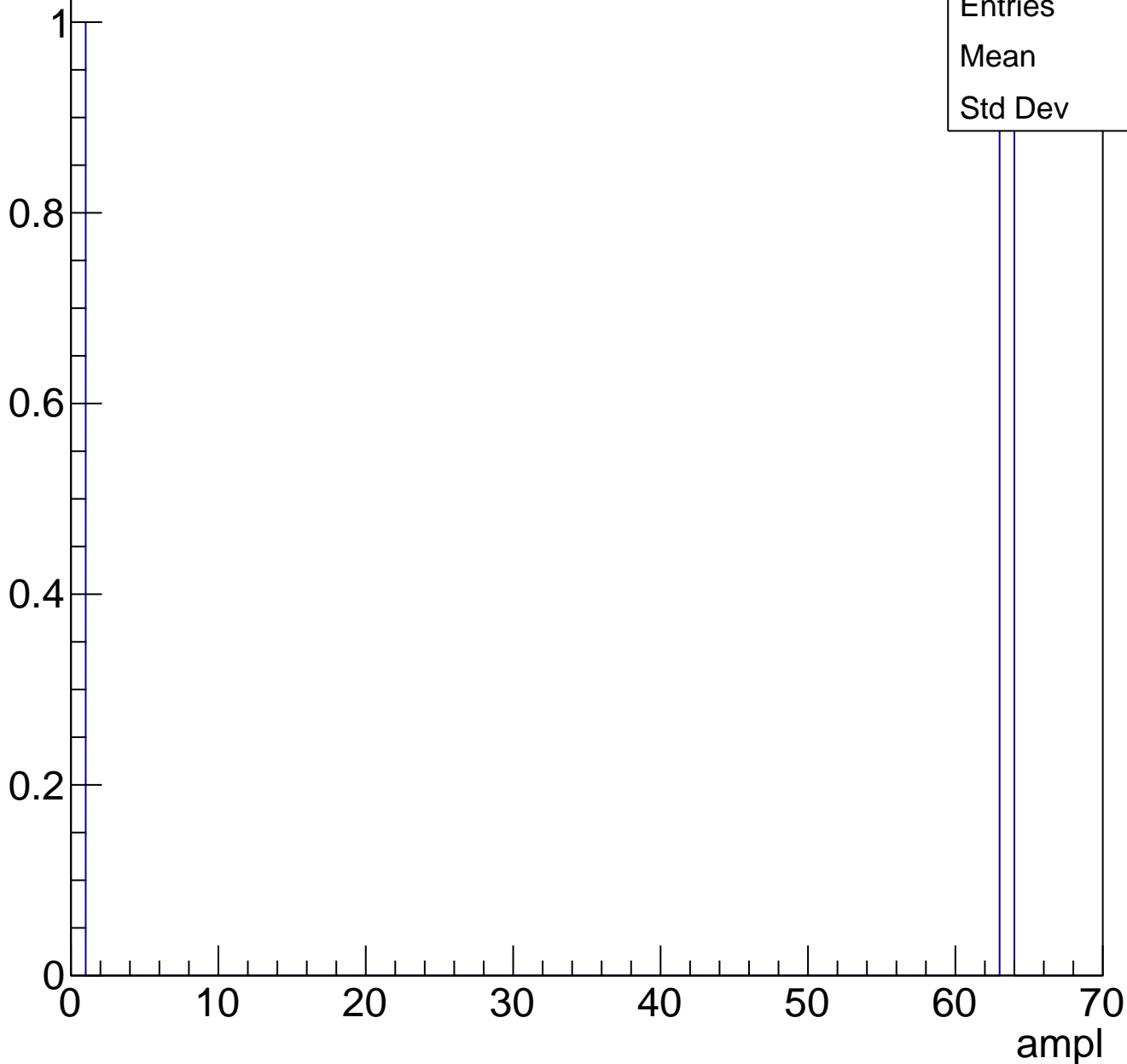




# B1L102S, U3-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch61, adc0

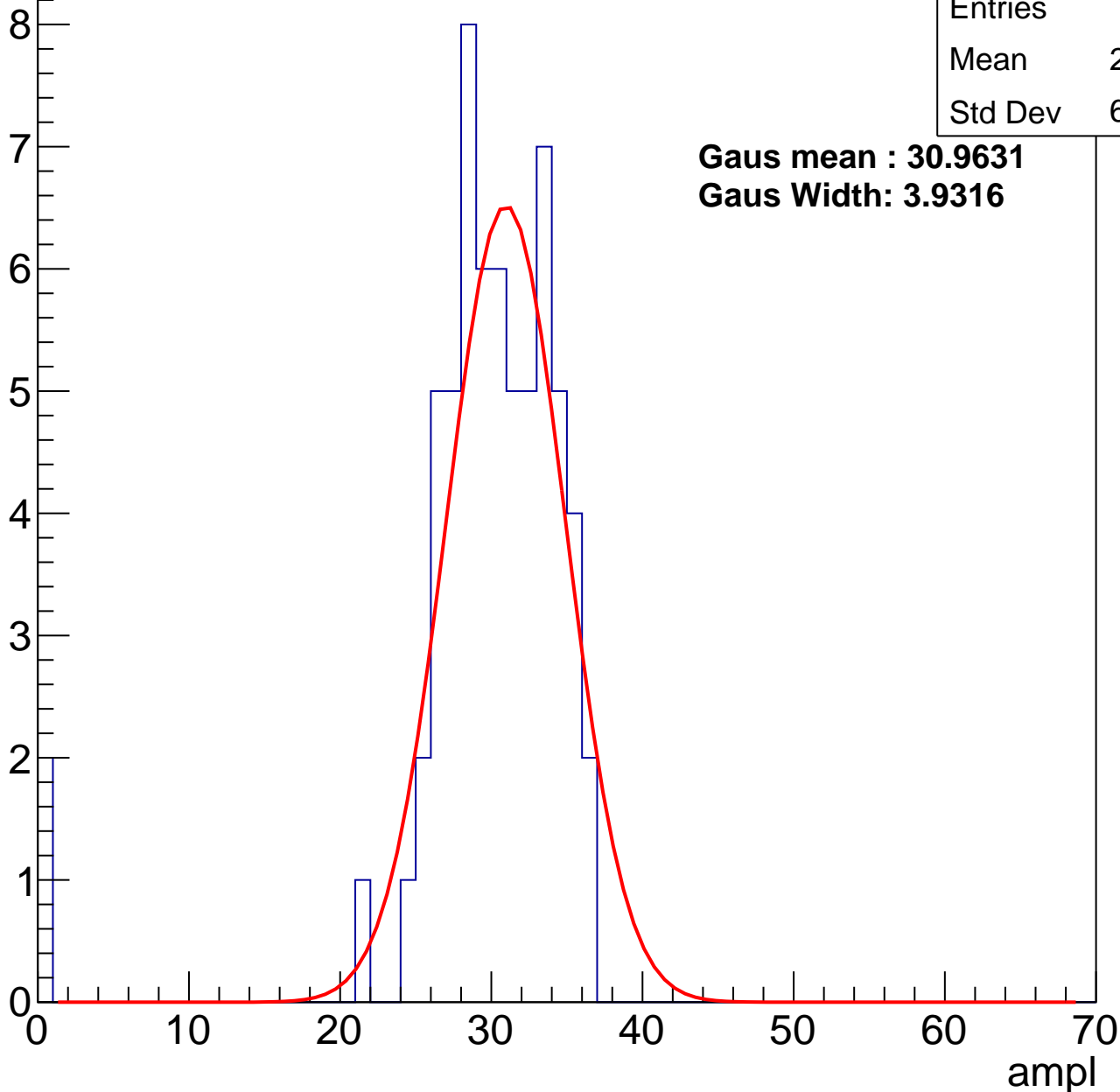
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	29.16
Std Dev	6.155

**Gaus mean : 30.9631**

**Gaus Width: 3.9316**



# B1L102S, U3-ch61, adc1

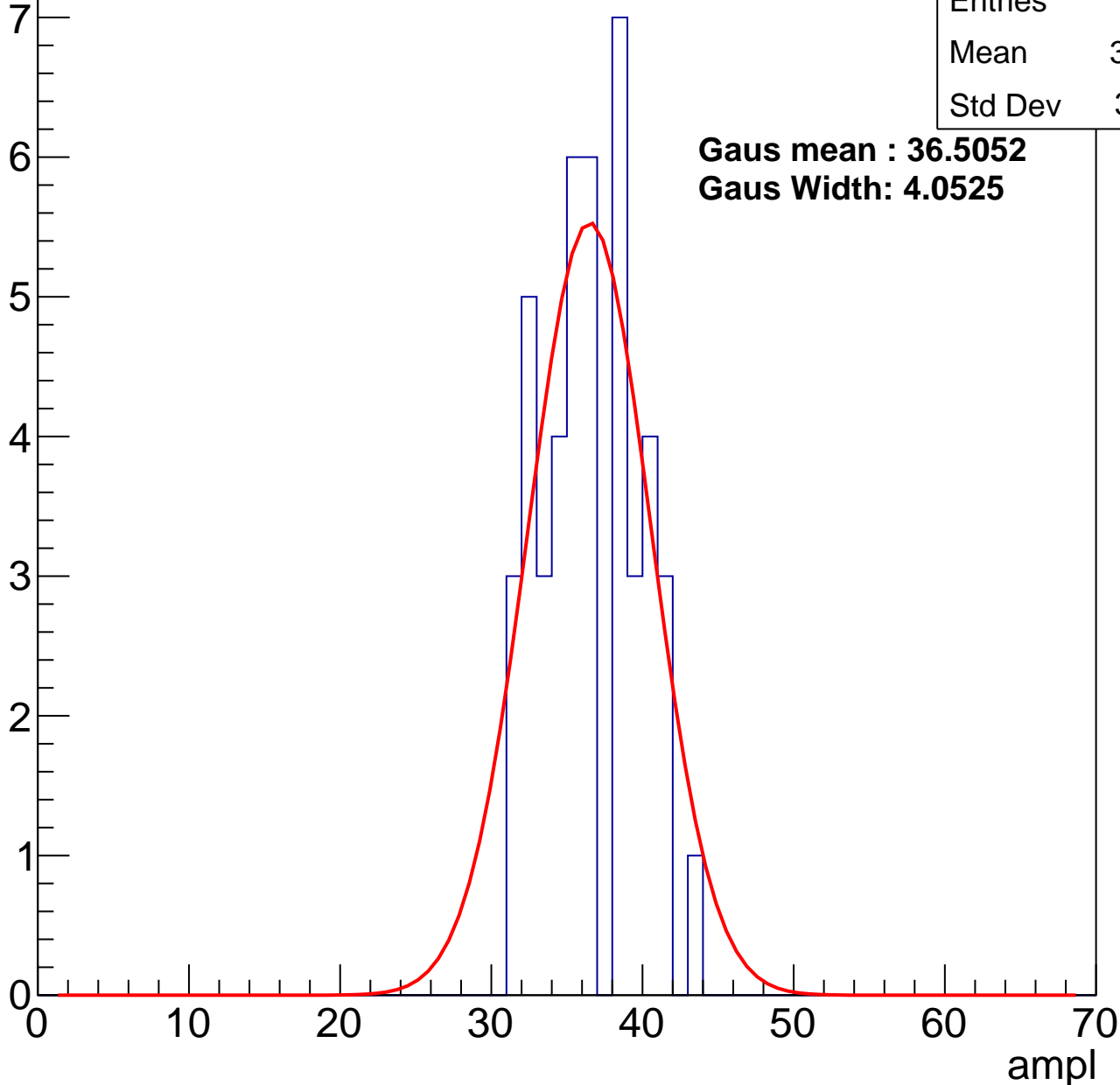
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	36.07
Std Dev	3.151

**Gaus mean : 36.5052**

**Gaus Width: 4.0525**



# B1L102S, U3-ch61, adc2

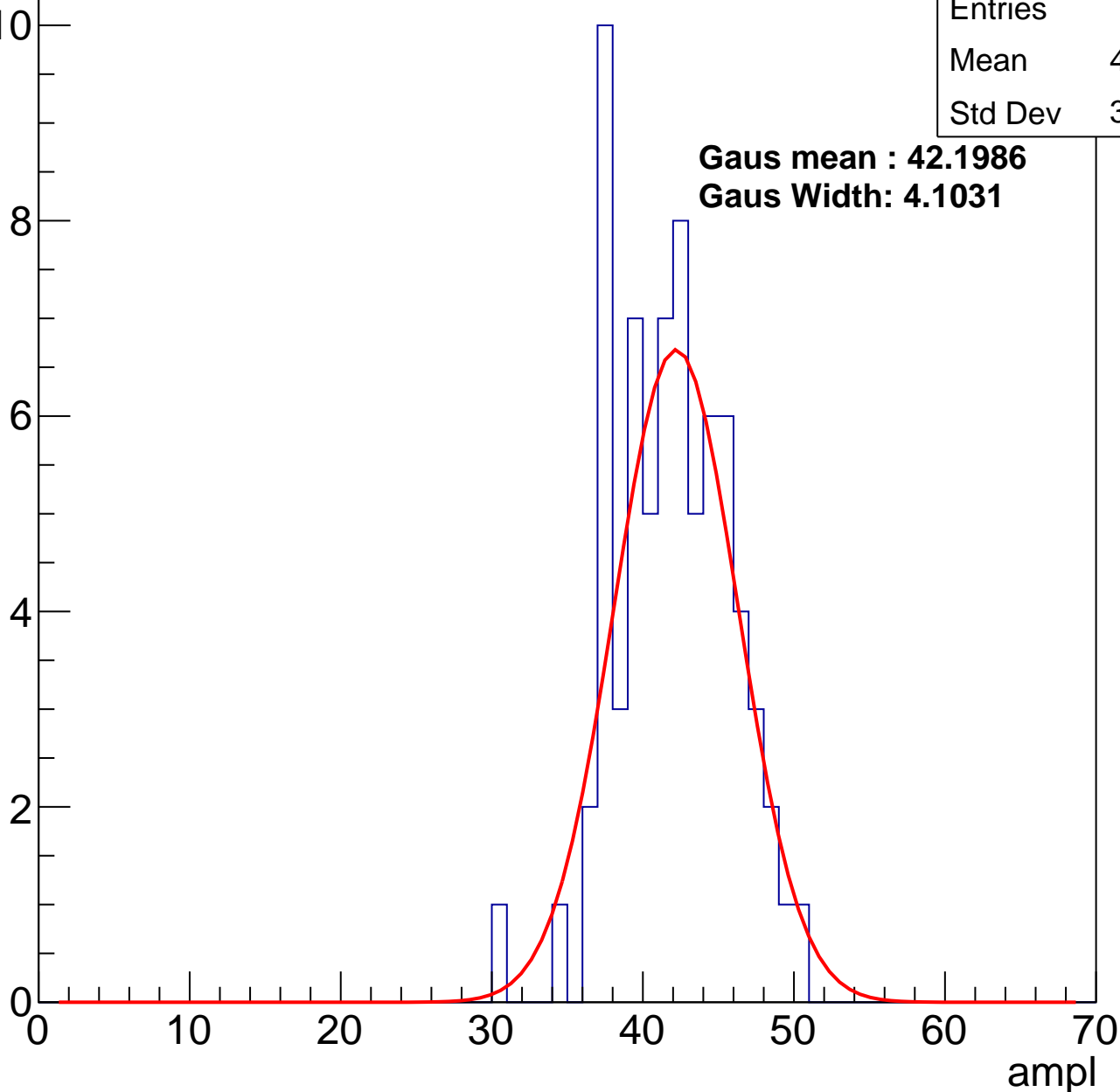
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	41.46
Std Dev	3.826

**Gaus mean : 42.1986**

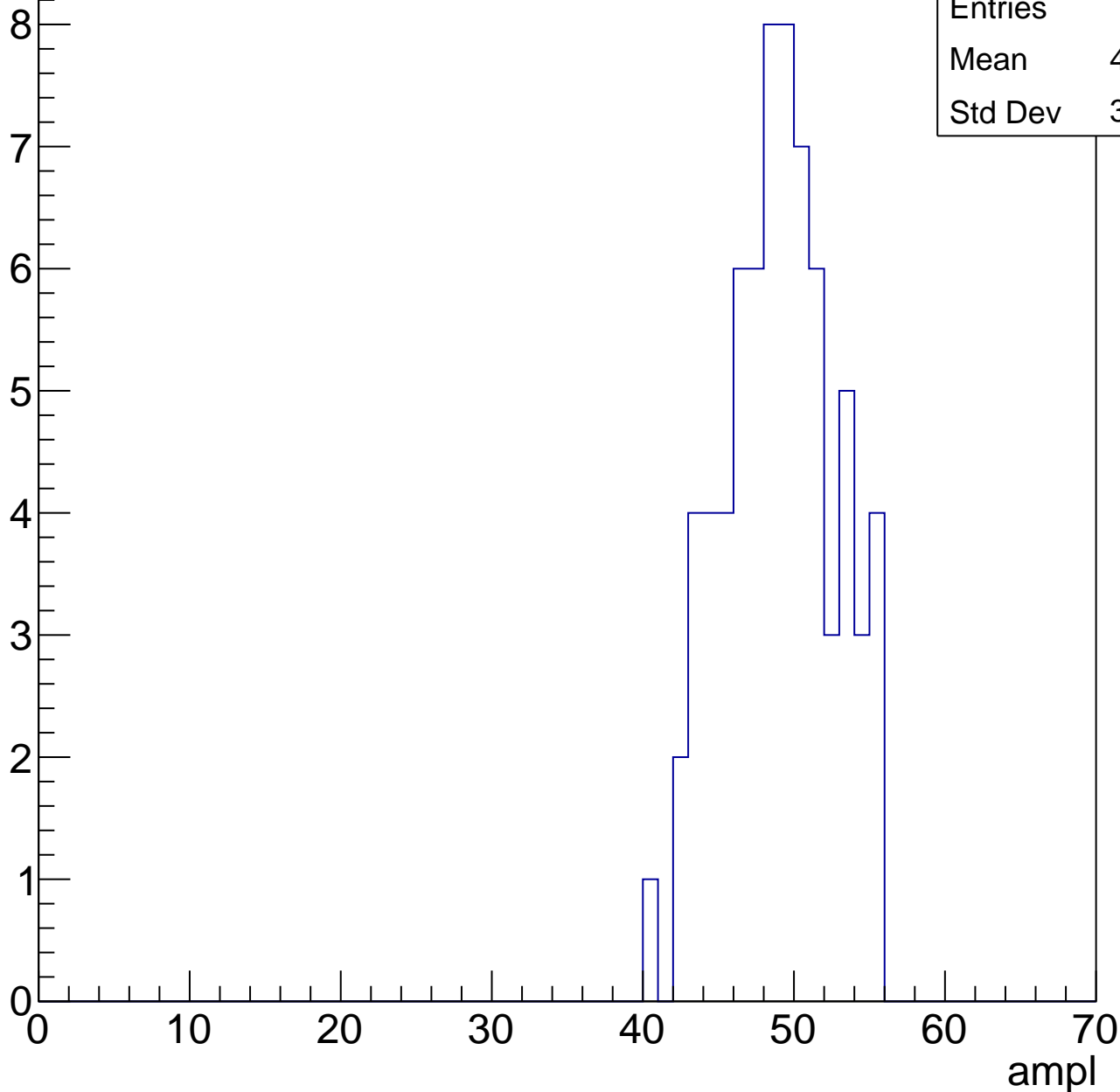
**Gaus Width: 4.1031**



# B1L102S, U3-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

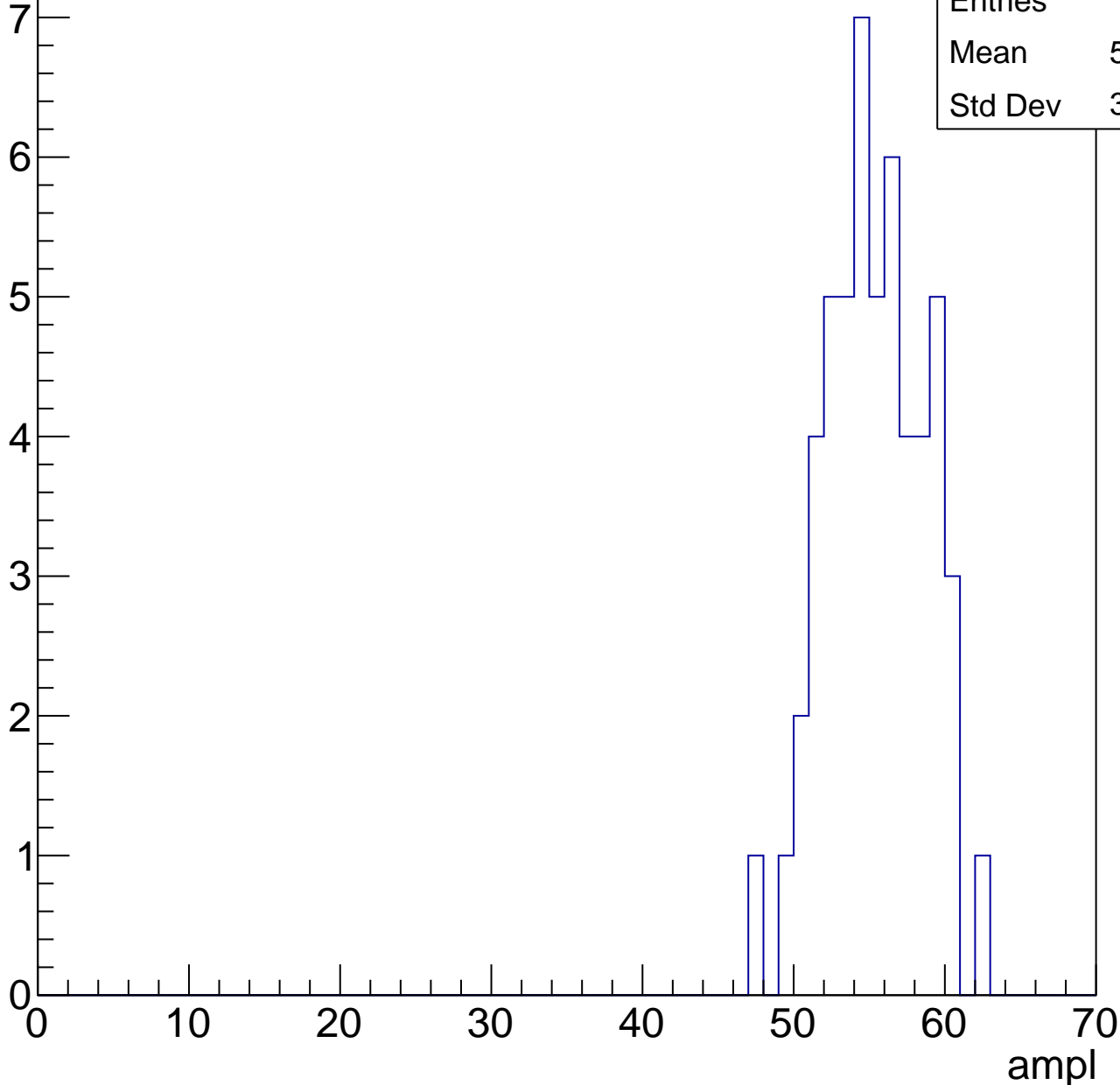


# B1L102S, U3-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	54.92
Std Dev	3.215

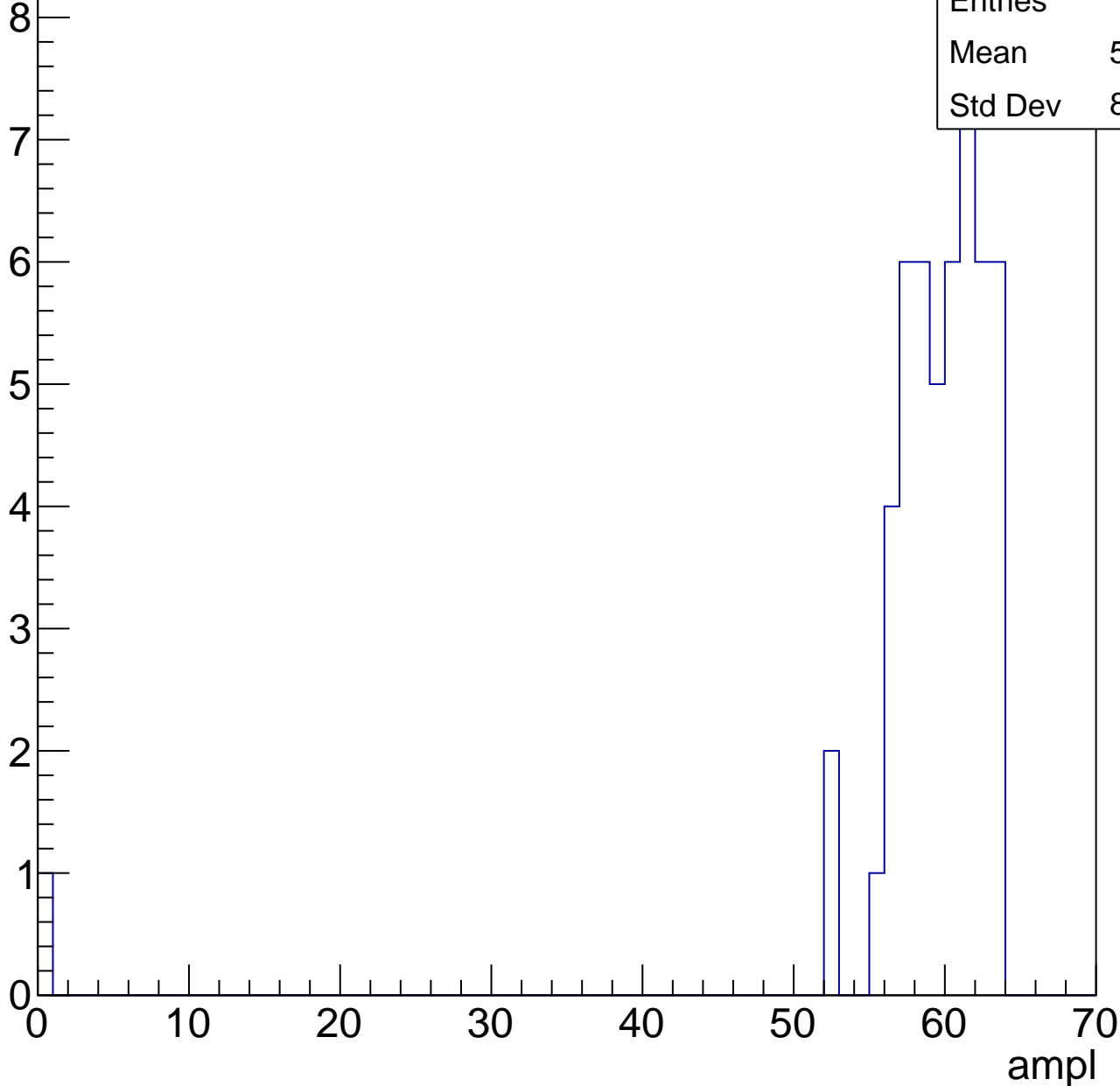


# B1L102S, U3-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	58.16
Std Dev	8.646



# B1L102S, U3-ch61, adc6

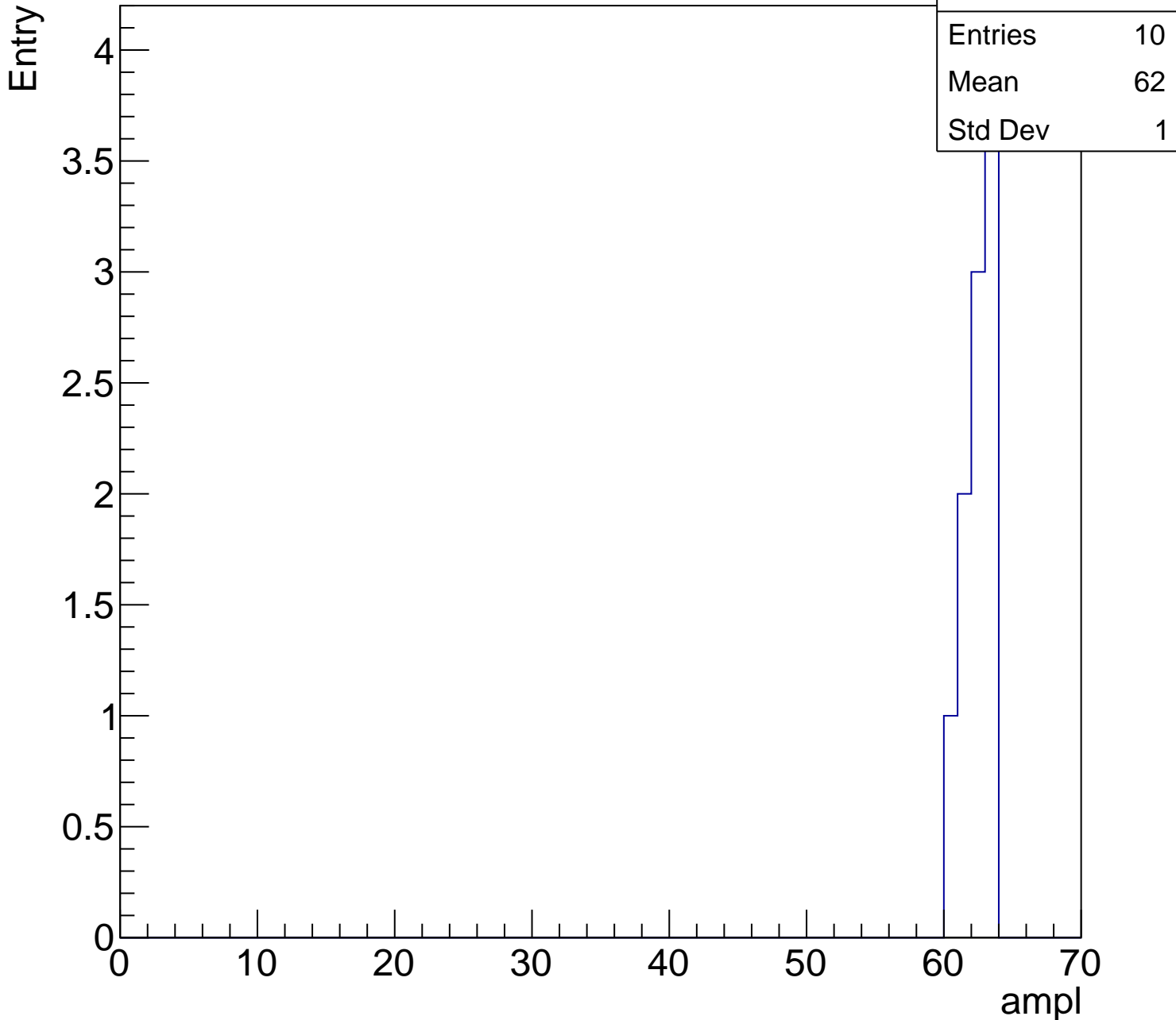
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

4  
3.5  
3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	10
Mean	62
Std Dev	1

ampl





# B1L102S, U3-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch62, adc0

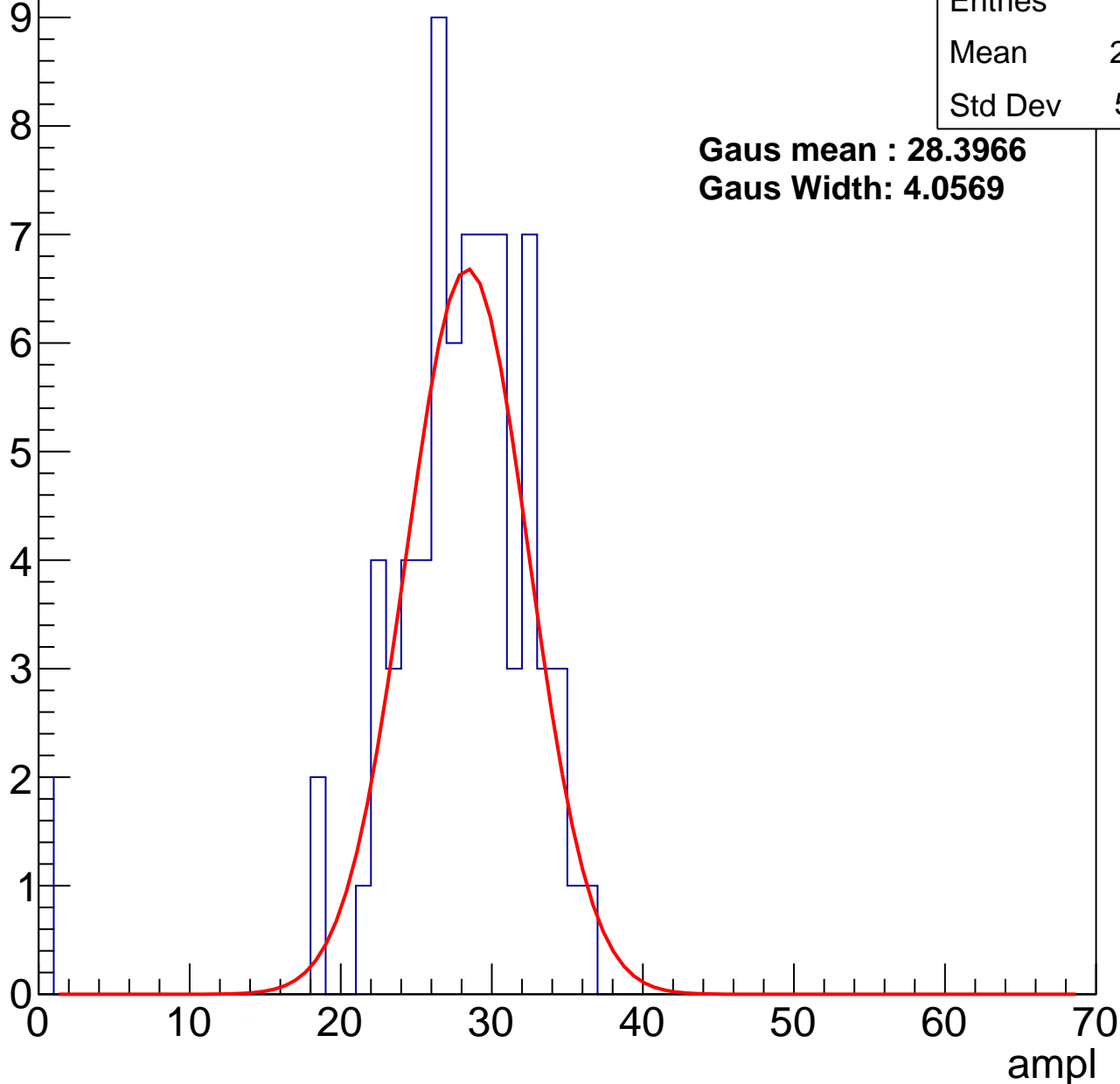
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	27.08
Std Dev	5.911

**Gaus mean : 28.3966**

**Gaus Width: 4.0569**



# B1L102S, U3-ch62, adc1

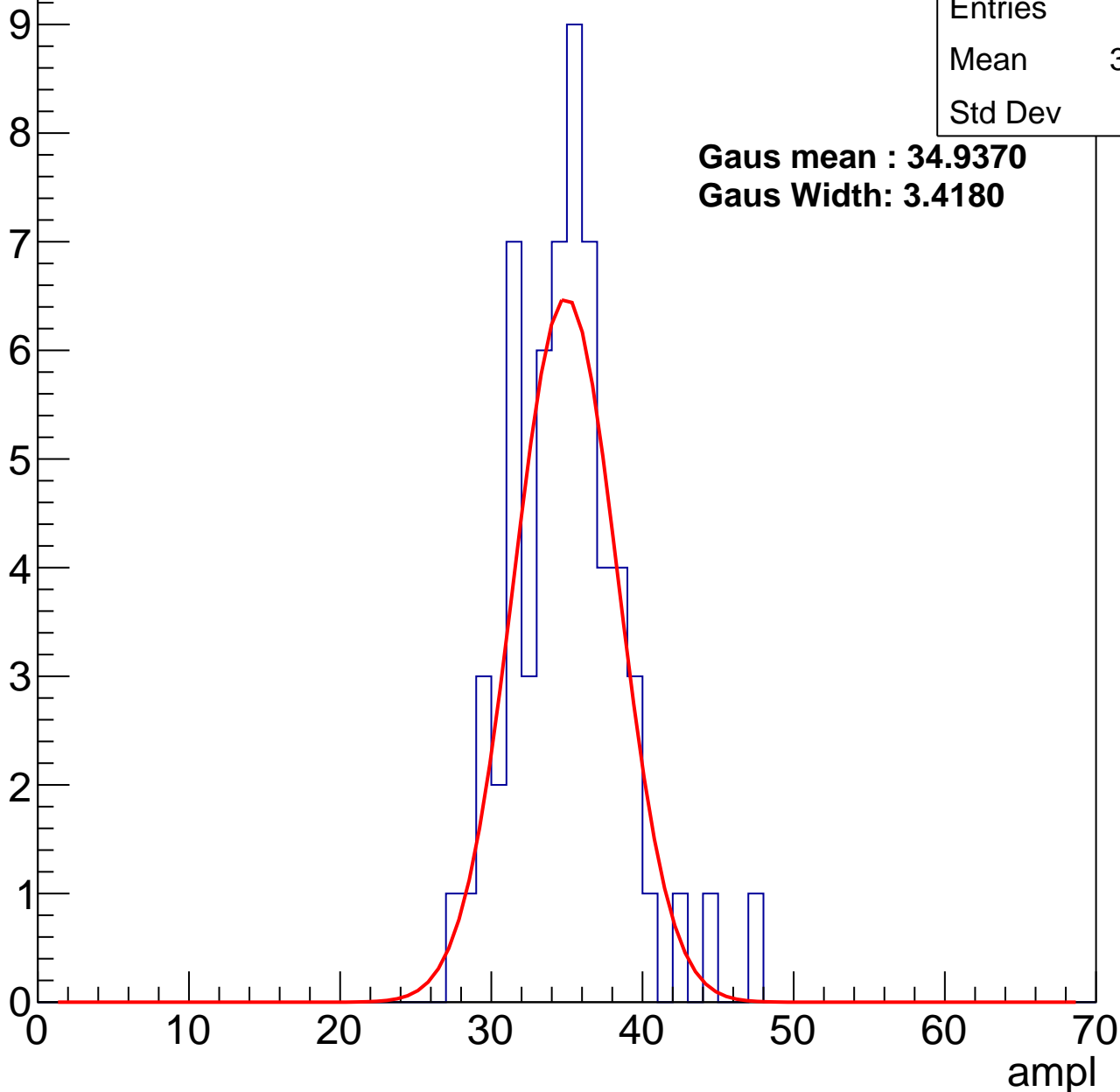
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	34.56
Std Dev	3.7

**Gaus mean : 34.9370**

**Gaus Width: 3.4180**



# B1L102S, U3-ch62, adc2

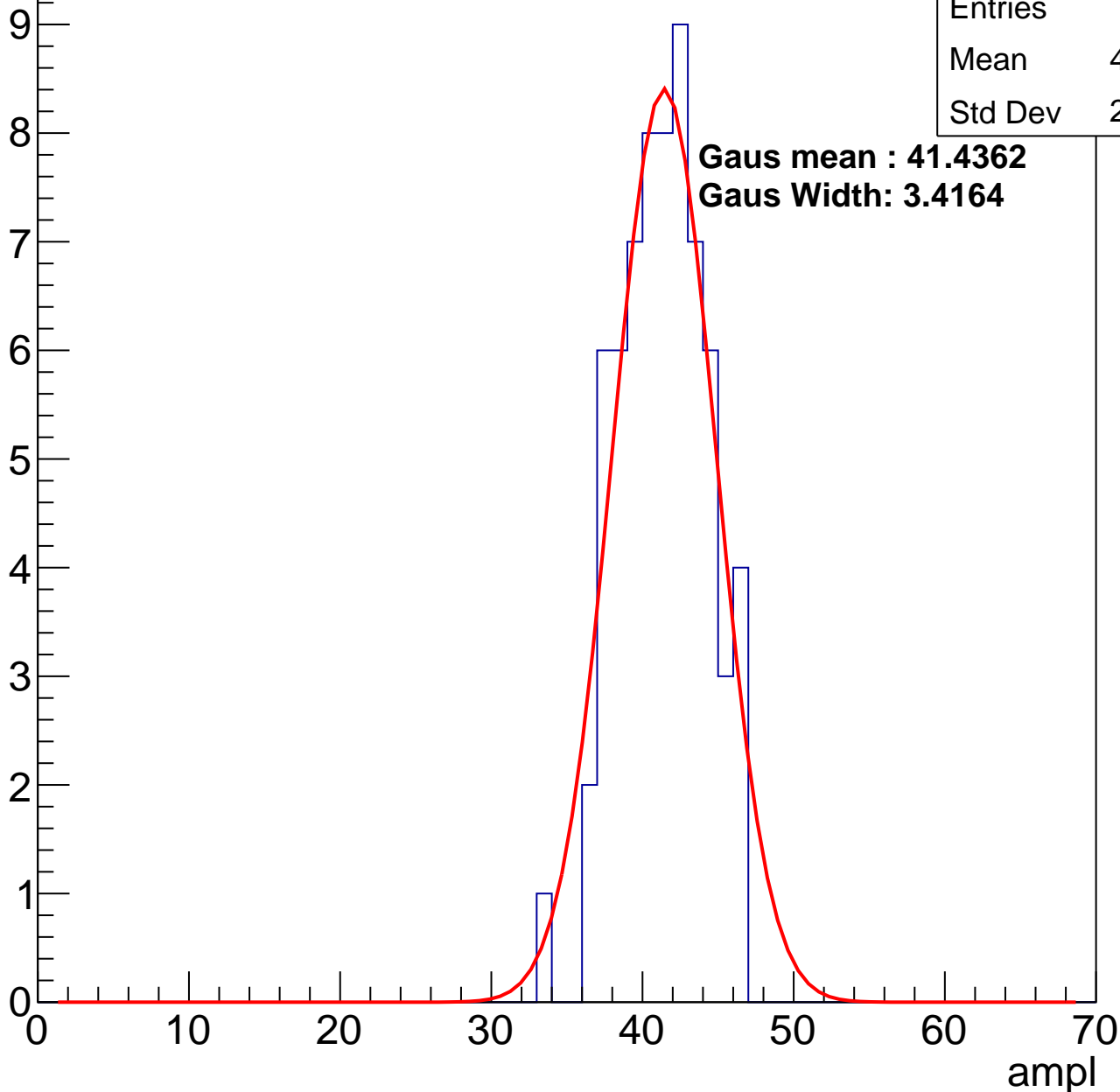
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	40.87
Std Dev	2.833

**Gaus mean : 41.4362**

**Gaus Width: 3.4164**

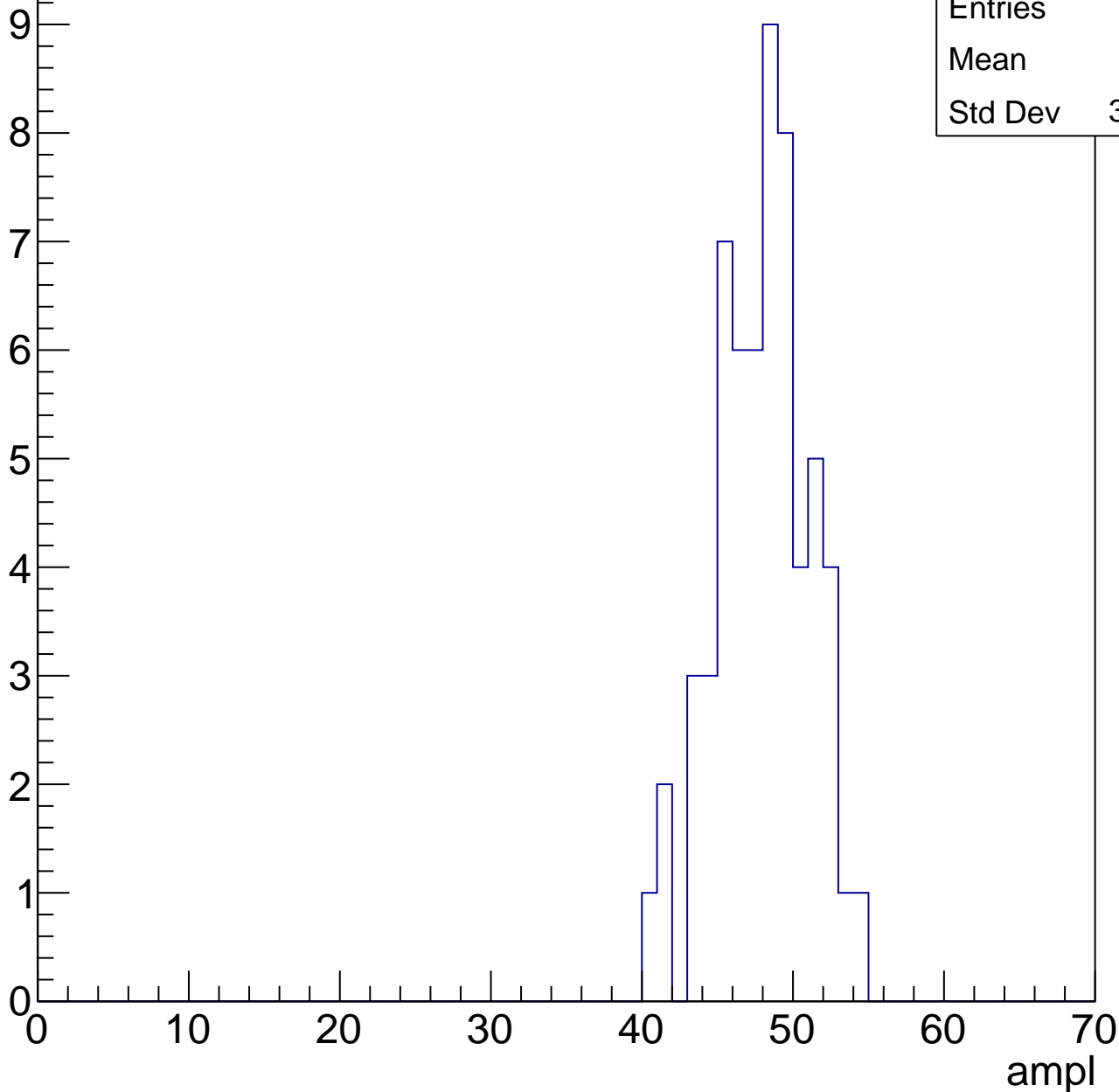


# B1L102S, U3-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

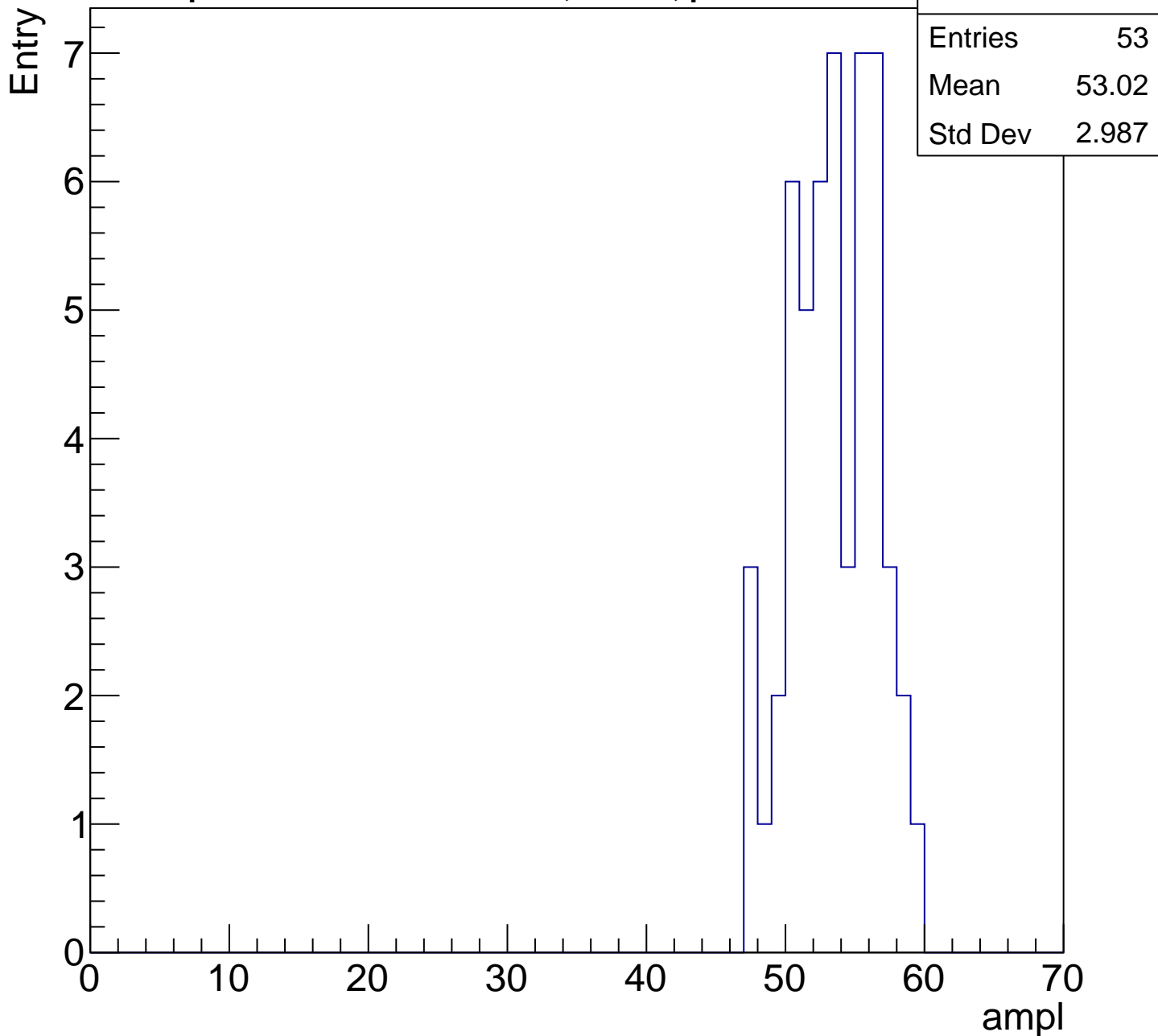
Entry

Entries	60
Mean	47.5
Std Dev	3.047



# B1L102S, U3-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U3-ch62, adc5

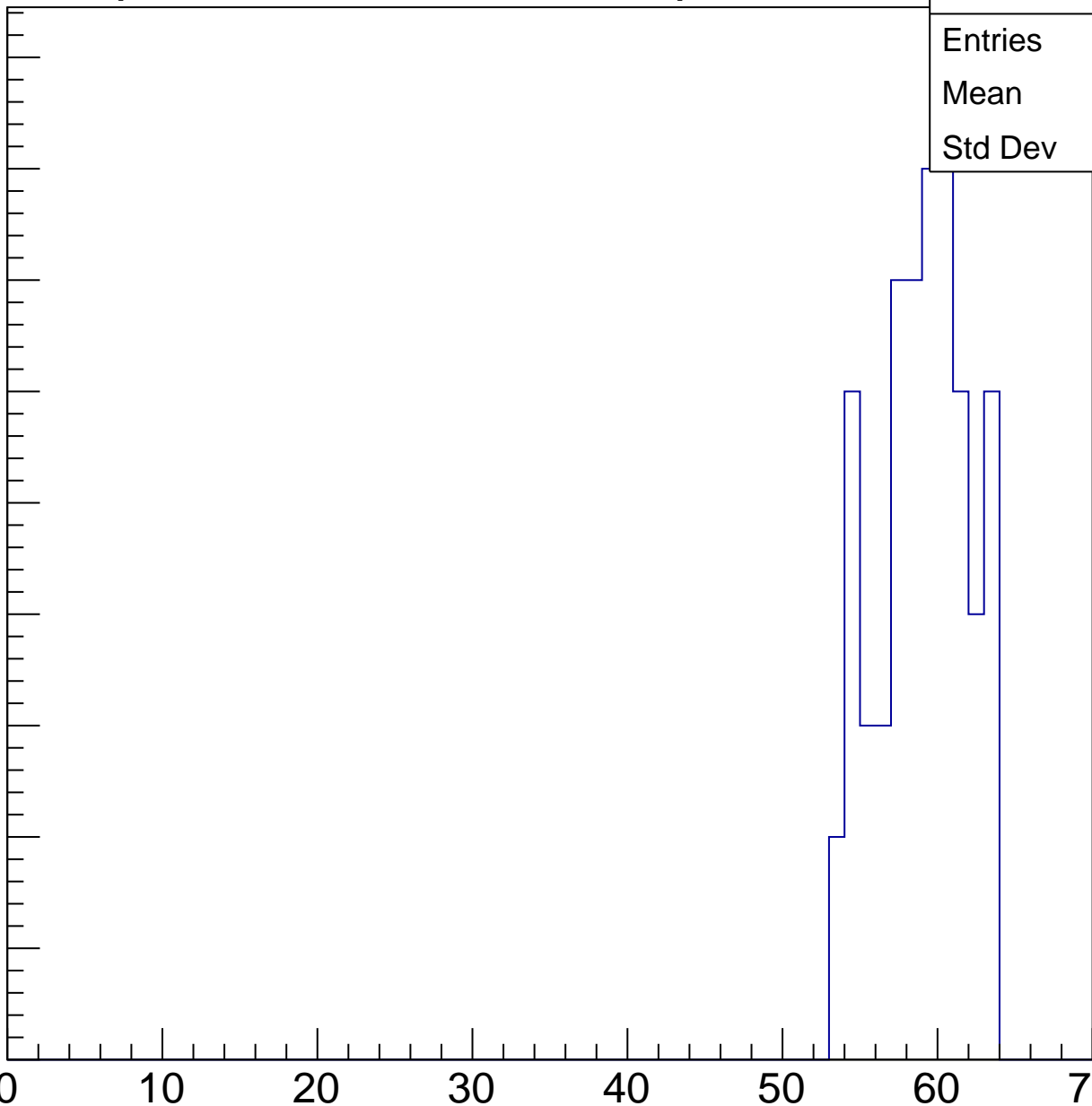
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	61
Mean	58.56
Std Dev	2.82

ampl

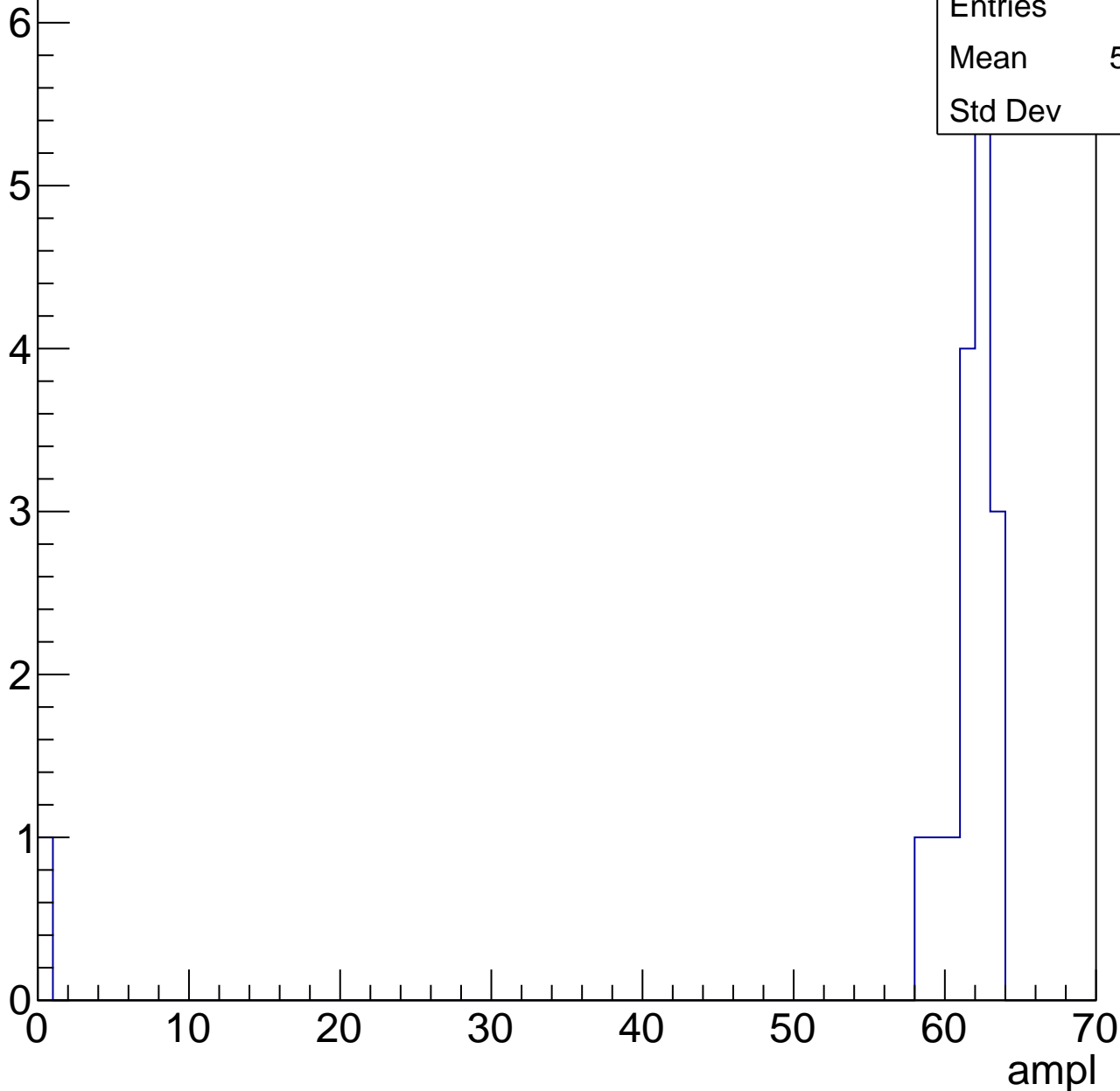


# B1L102S, U3-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	17
Mean	57.76
Std Dev	14.5





# B1L102S, U3-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch63, adc0

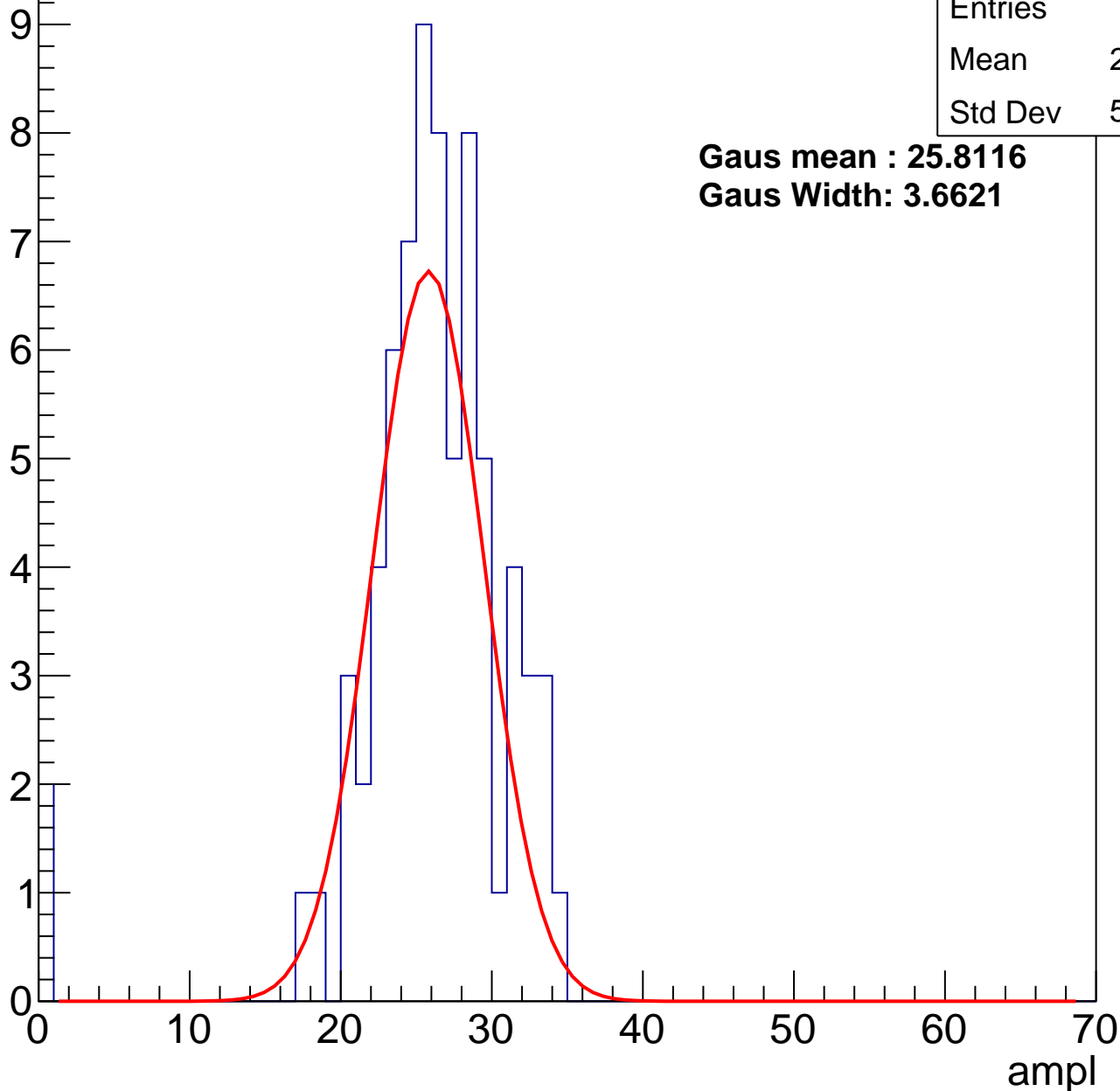
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	25.36
Std Dev	5.609

**Gaus mean : 25.8116**

**Gaus Width: 3.6621**



# B1L102S, U3-ch63, adc1

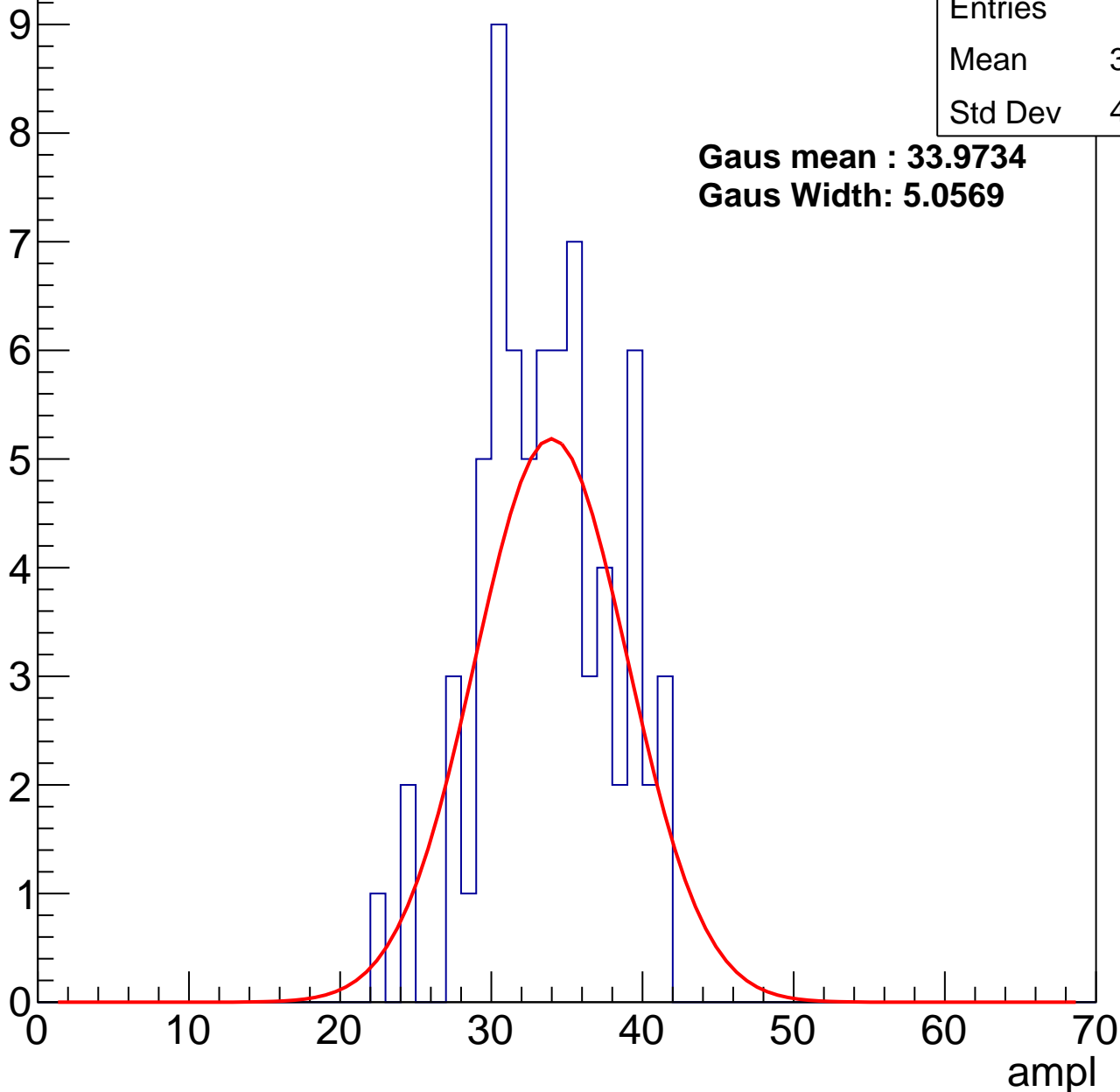
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	33.18
Std Dev	4.254

**Gaus mean : 33.9734**

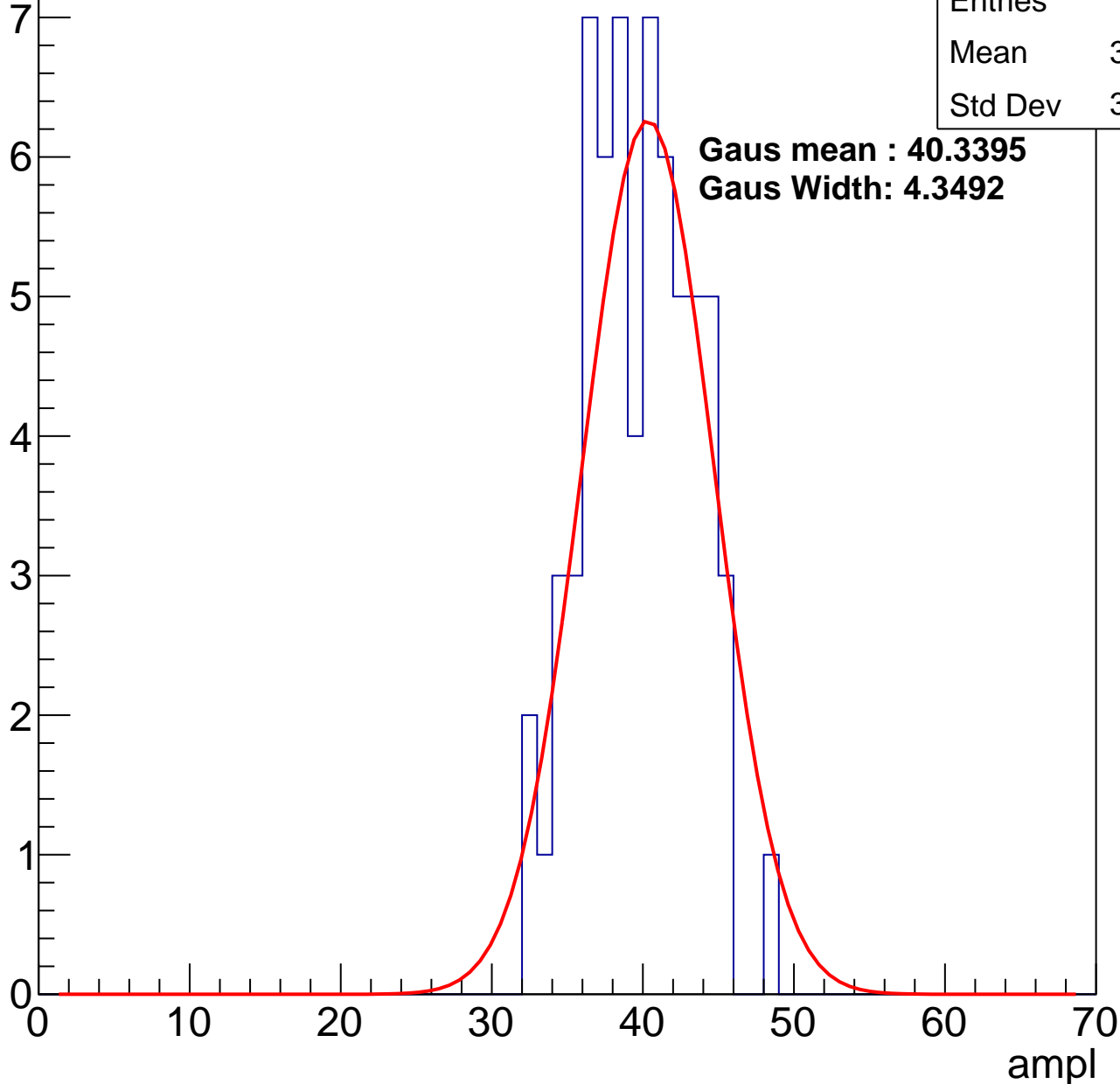
**Gaus Width: 5.0569**



# B1L102S, U3-ch63, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

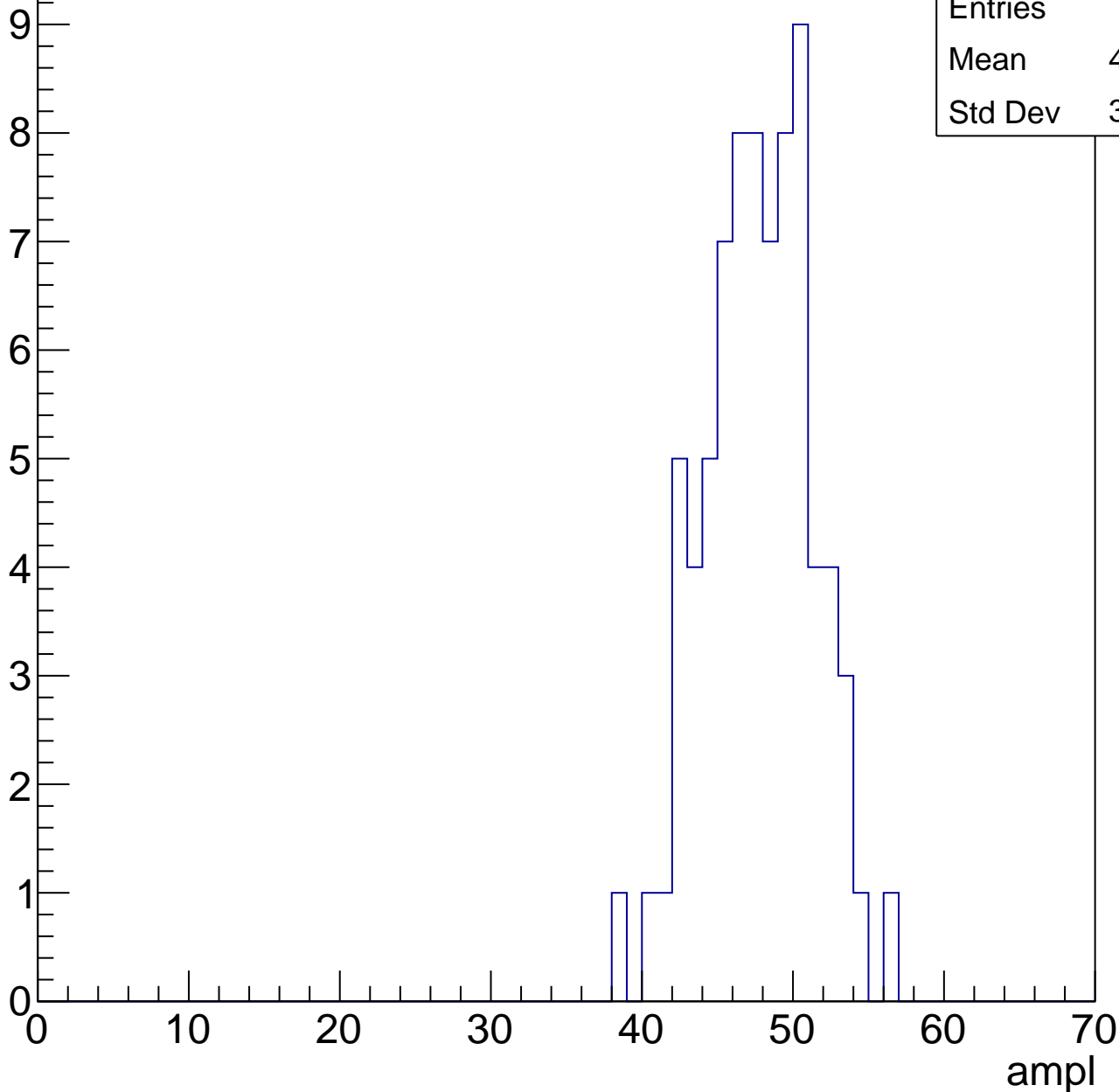


# B1L102S, U3-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	47.26
Std Dev	3.518

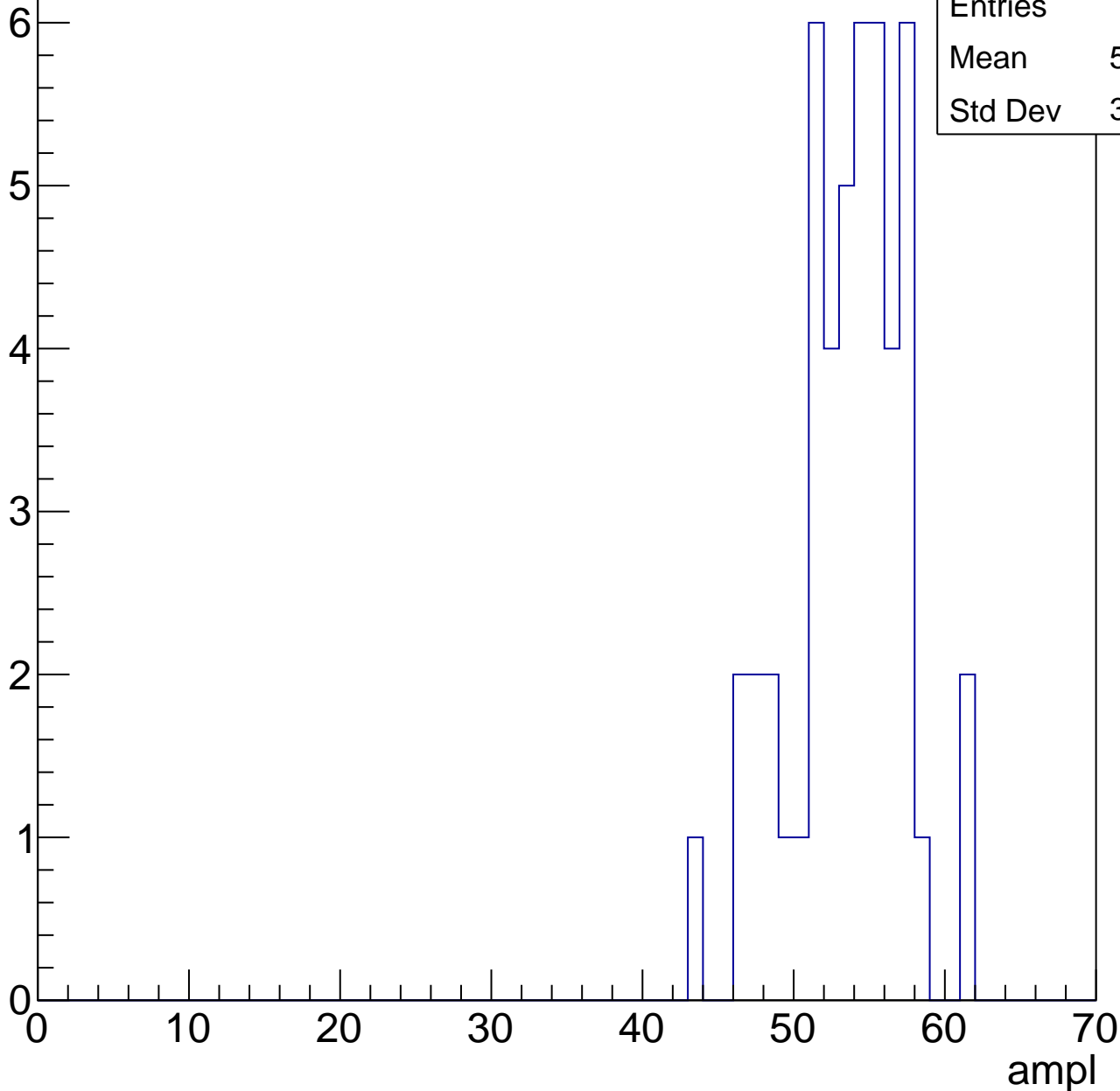


# B1L102S, U3-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	53.12
Std Dev	3.745



# B1L102S, U3-ch63, adc5

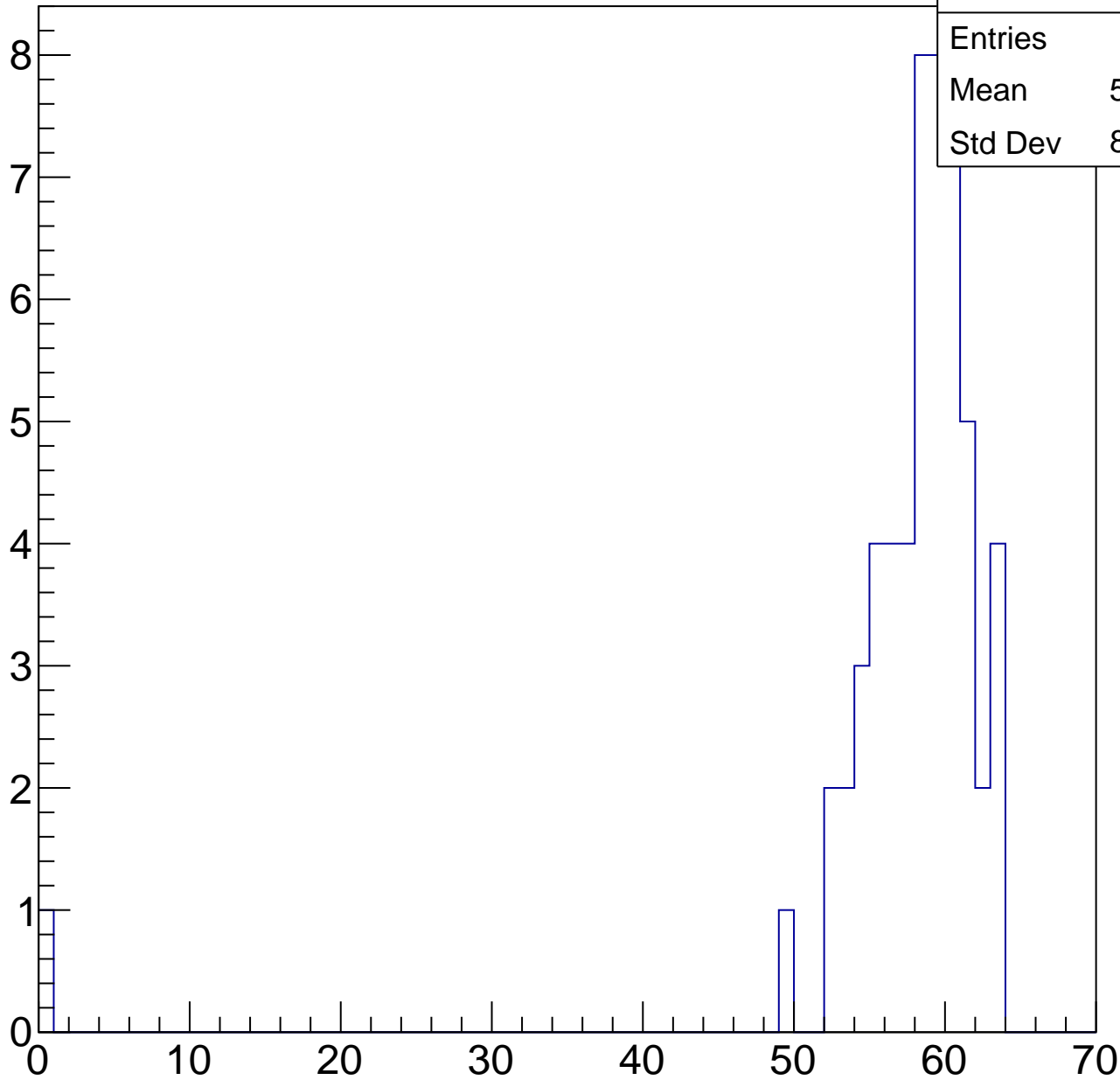
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	56
Mean	56.96
Std Dev	8.268

ampl

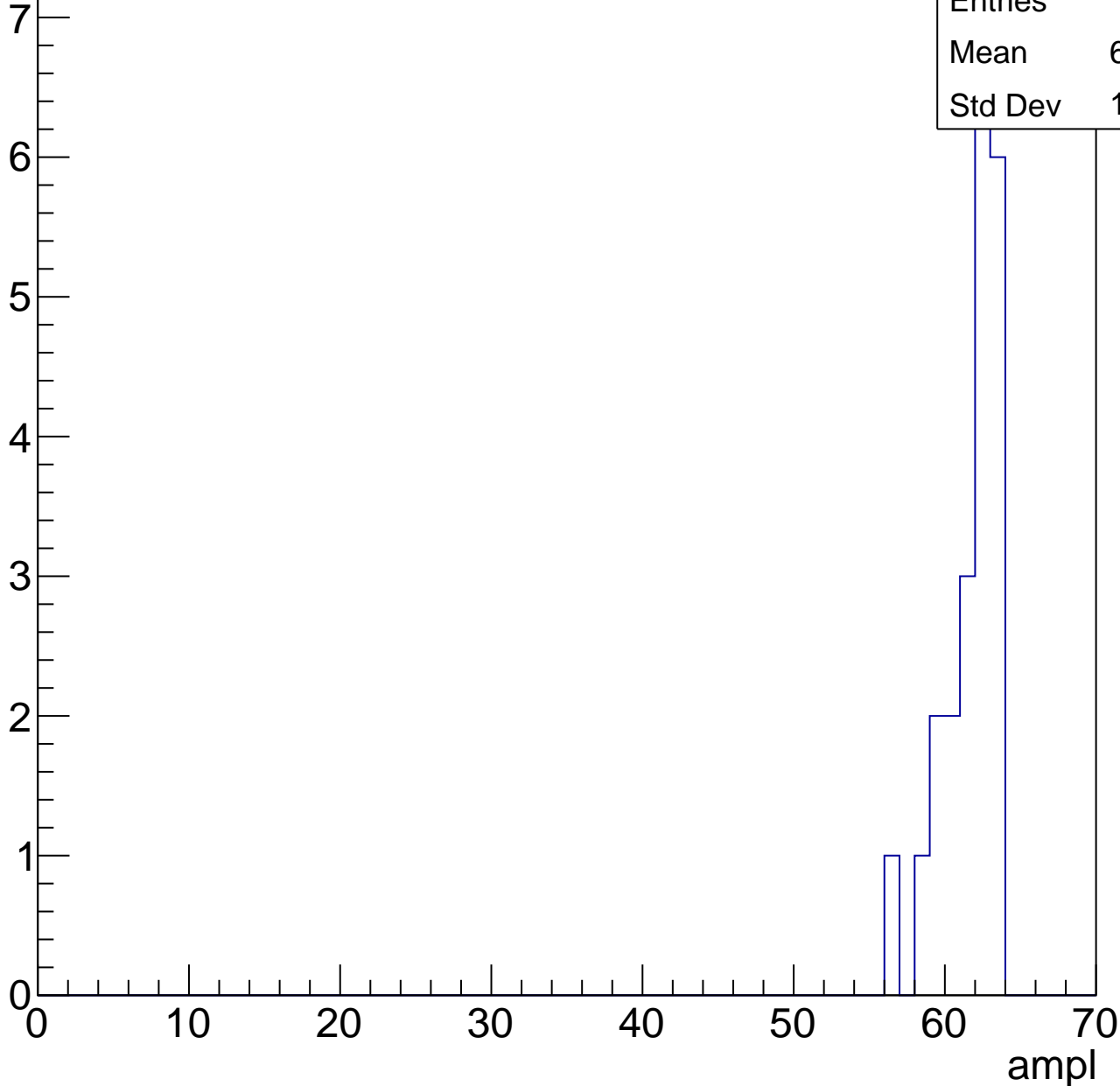


# B1L102S, U3-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	22
Mean	61.23
Std Dev	1.832

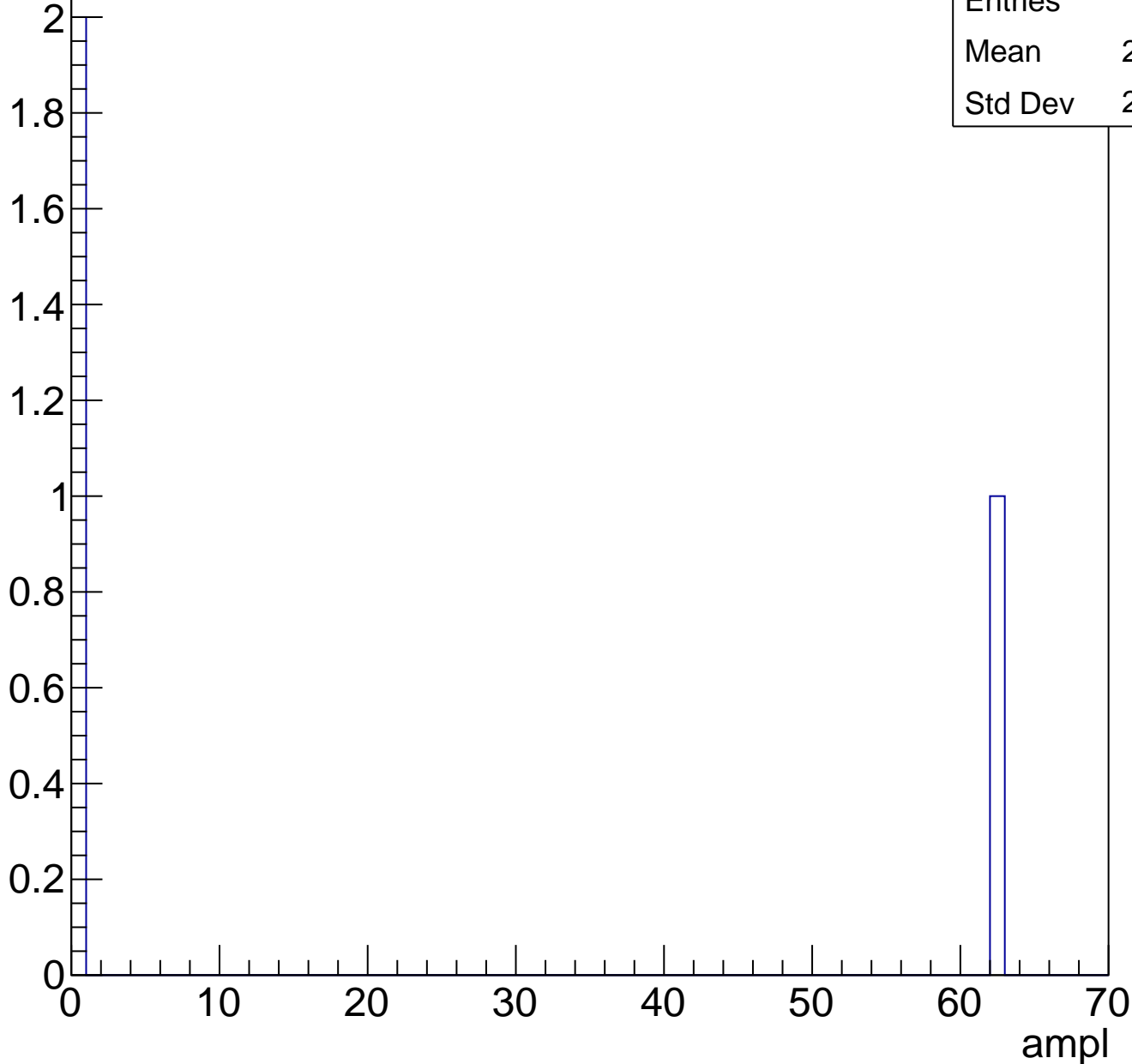




# B1L102S, U3-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch64, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	74
Mean	29.12
Std Dev	3.393

**Gaus mean : 29.5518**

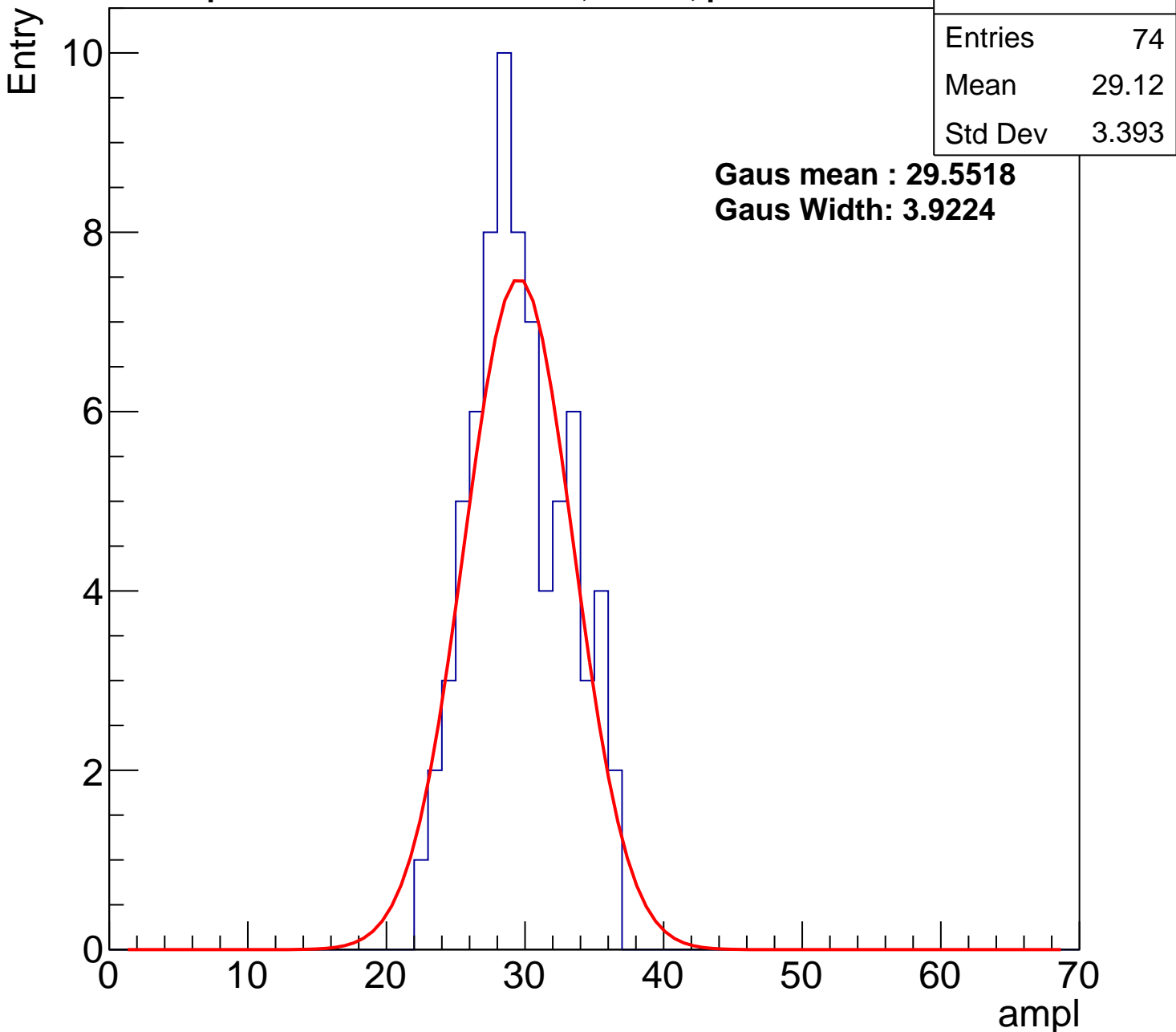
**Gaus Width: 3.9224**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U3-ch64, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	69
Mean	36.13
Std Dev	3.31

**Gaus mean : 36.5335**

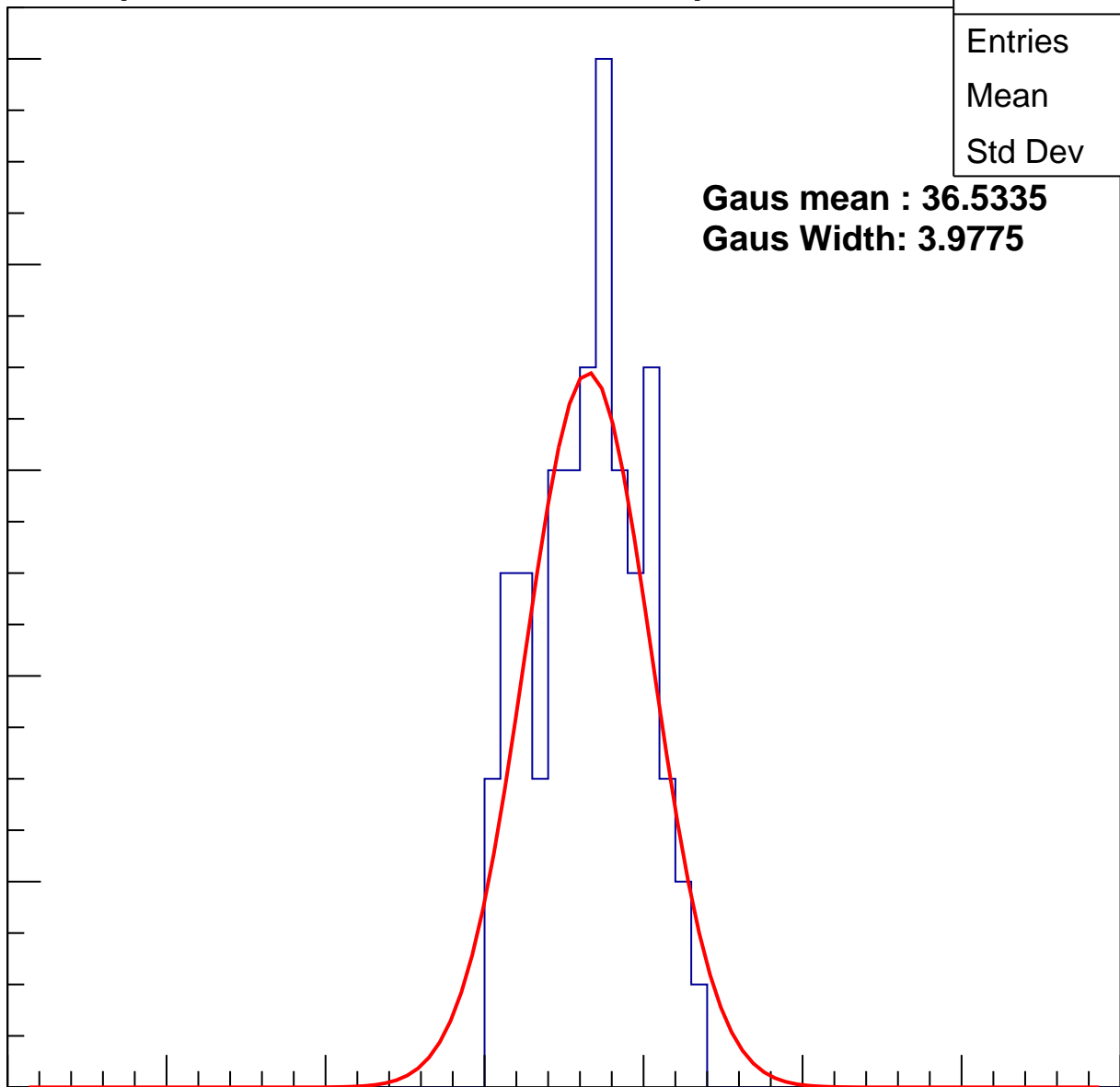
**Gaus Width: 3.9775**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U3-ch64, adc2

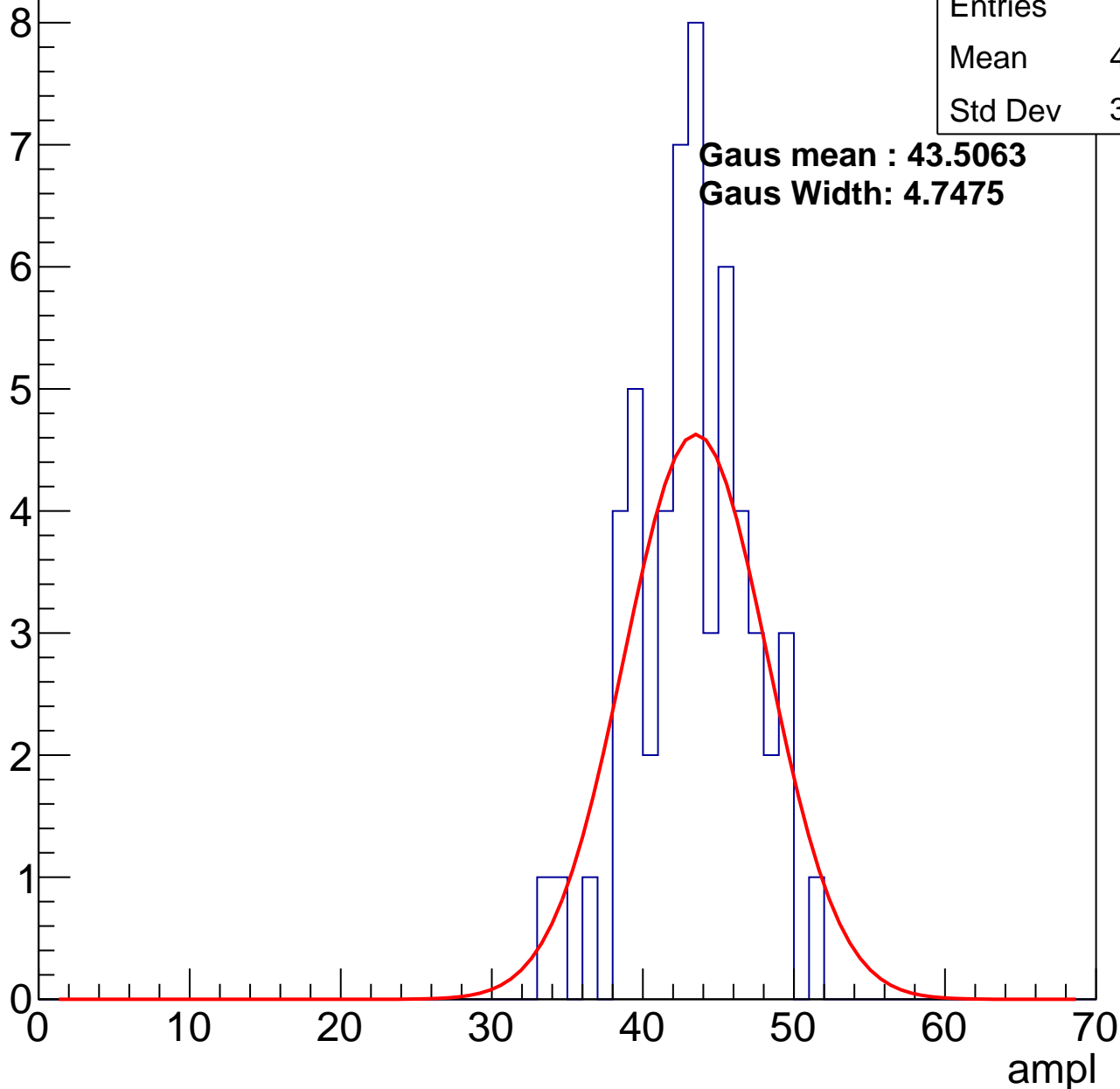
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	42.78
Std Dev	3.769

**Gaus mean : 43.5063**

**Gaus Width: 4.7475**

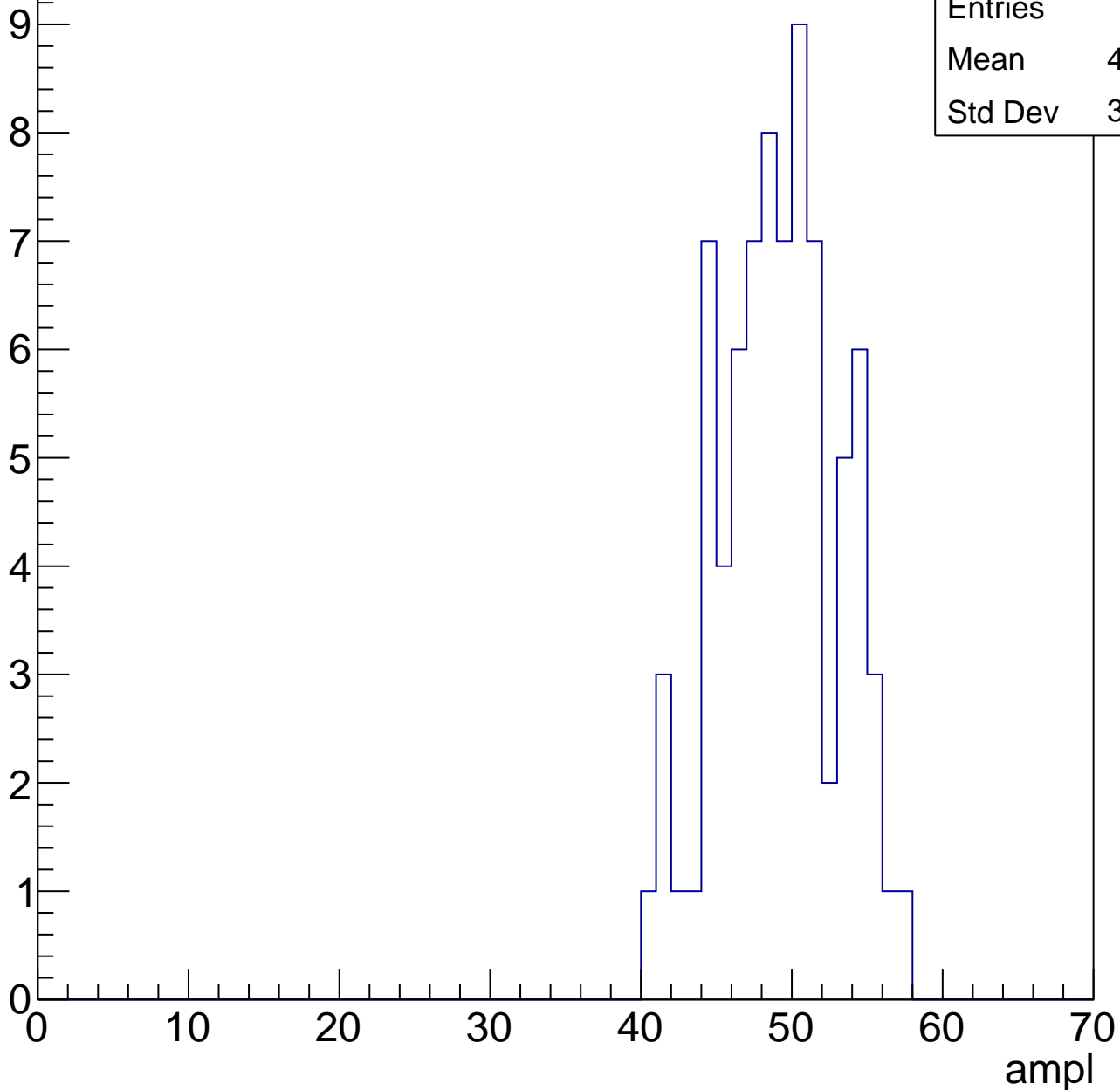


# B1L102S, U3-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	48.68
Std Dev	3.873

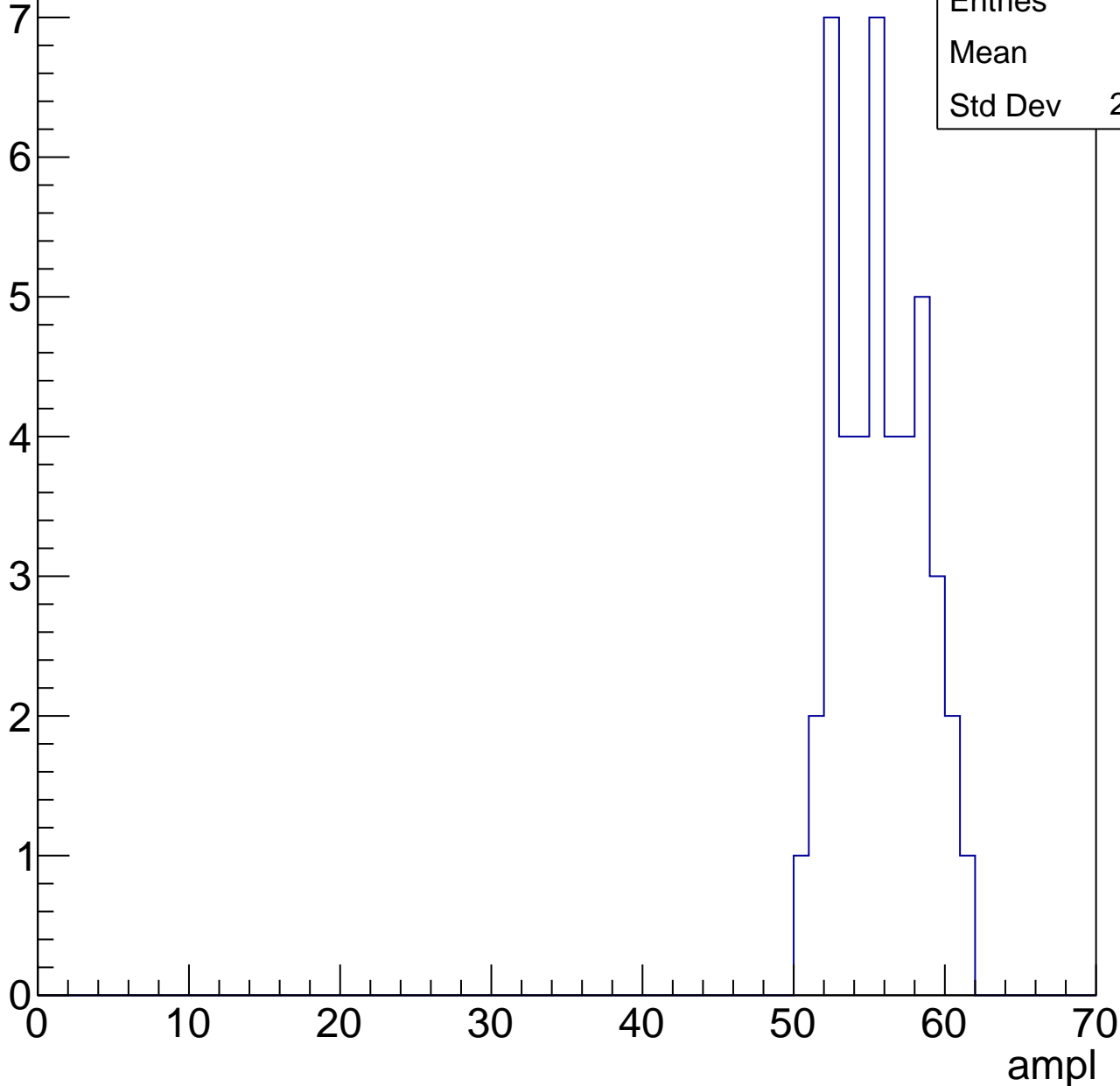


# B1L102S, U3-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	44
Mean	55.2
Std Dev	2.768

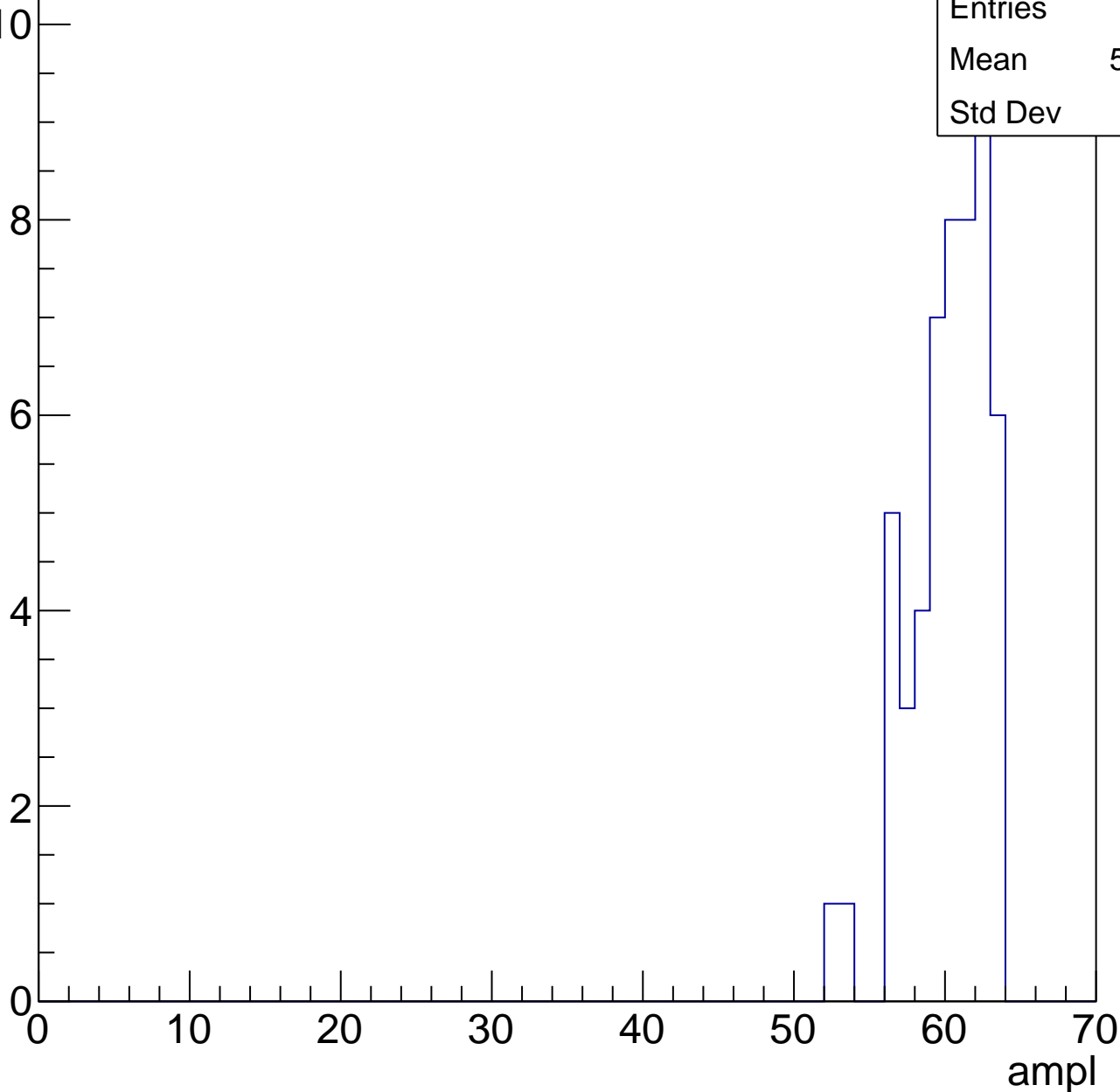


# B1L102S, U3-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

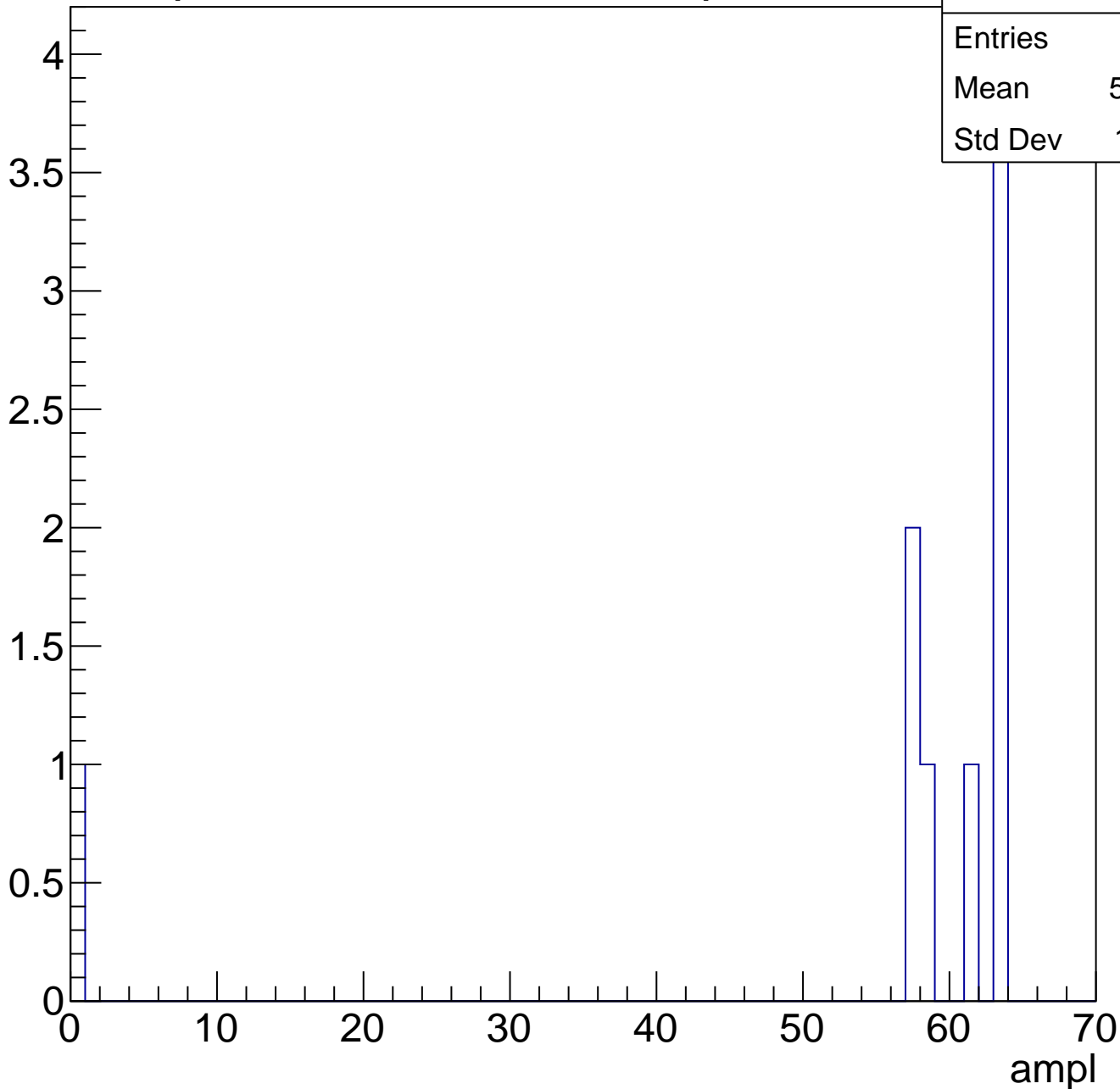
Entries	53
Mean	59.75
Std Dev	2.54



# B1L102S, U3-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

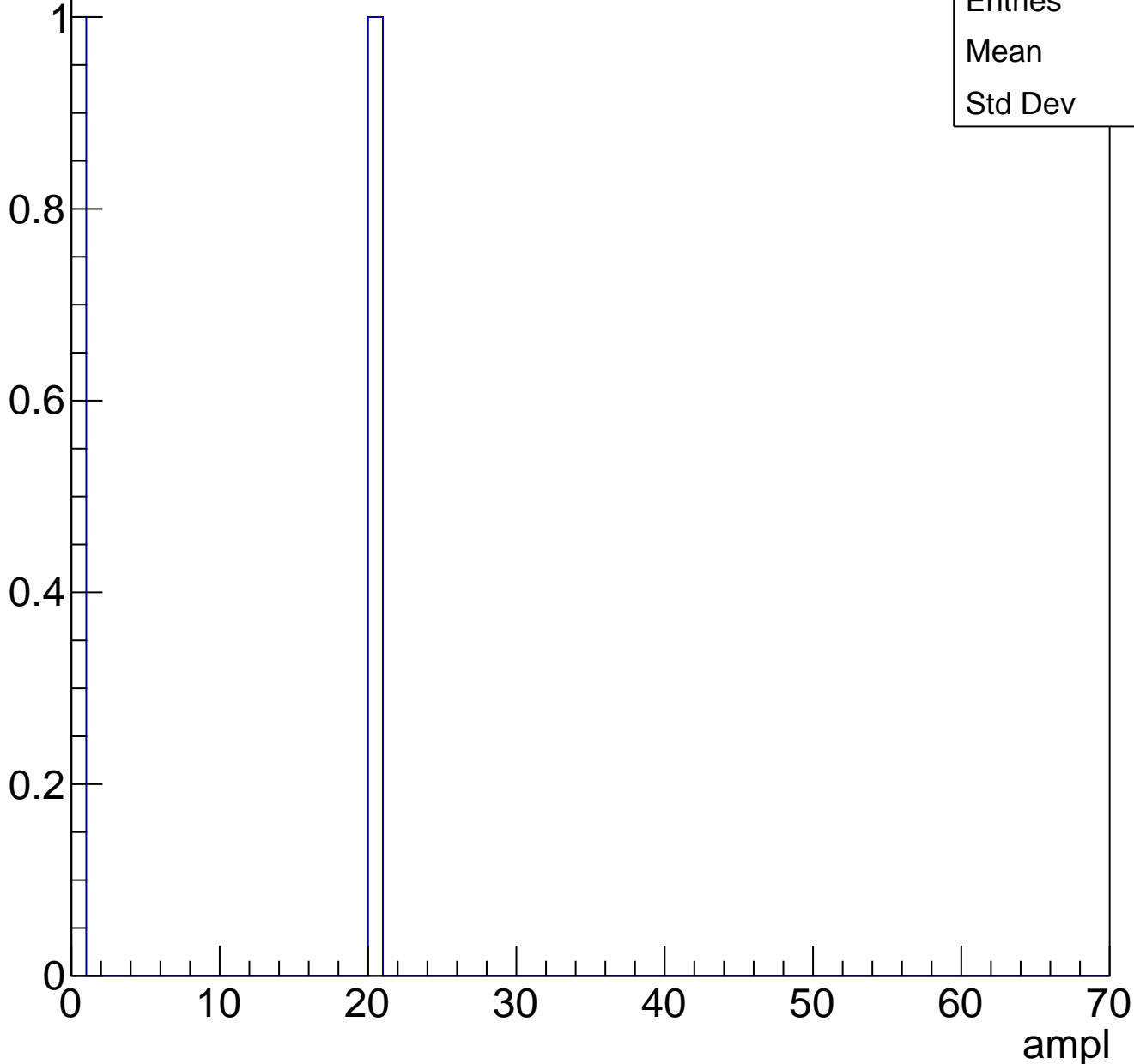




# B1L102S, U3-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	10
Std Dev	10

# B1L102S, U3-ch65, adc0

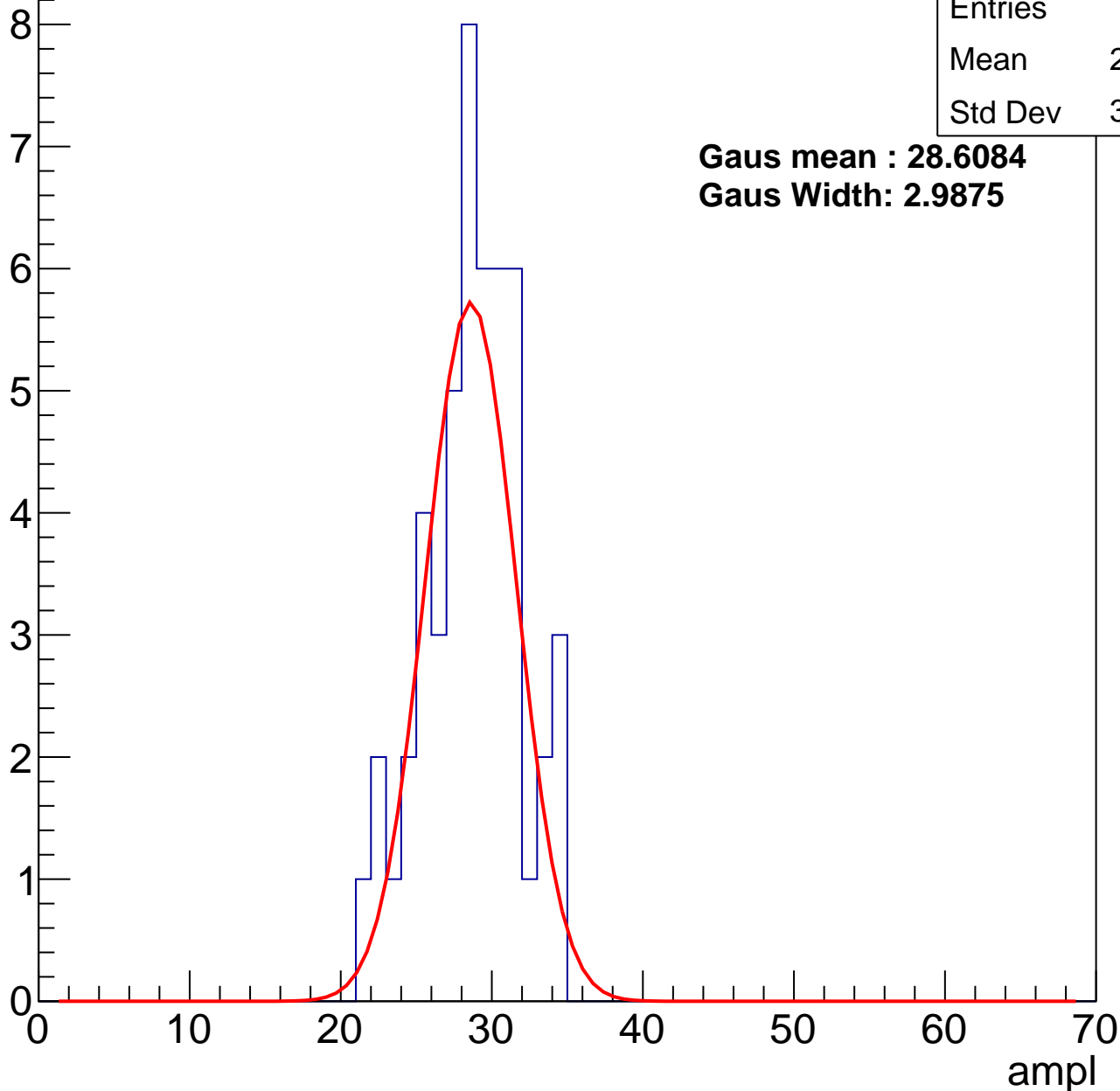
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	28.26
Std Dev	3.116

**Gaus mean : 28.6084**

**Gaus Width: 2.9875**



# B1L102S, U3-ch65, adc1

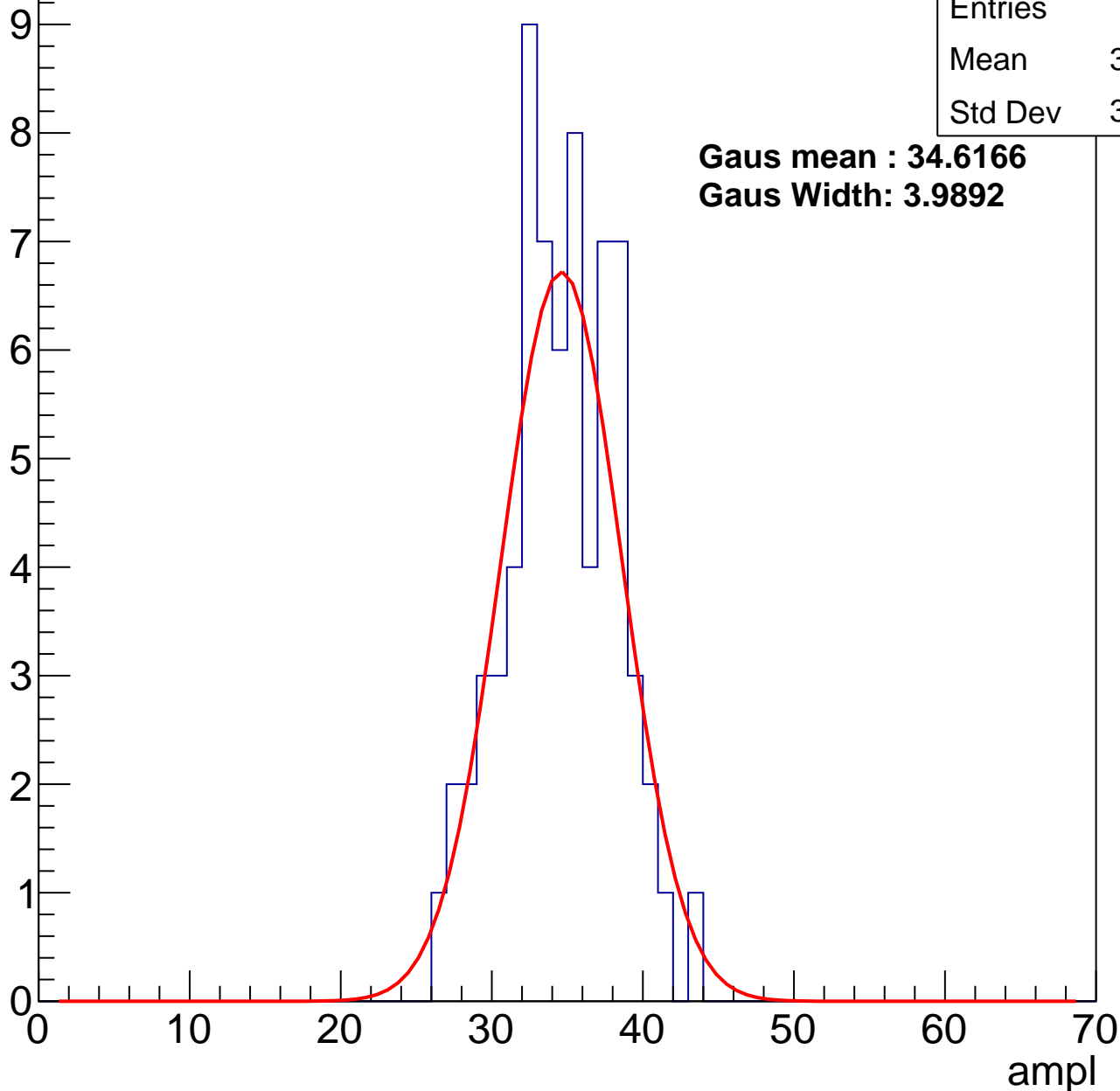
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	34.14
Std Dev	3.607

**Gaus mean : 34.6166**

**Gaus Width: 3.9892**



# B1L102S, U3-ch65, adc2

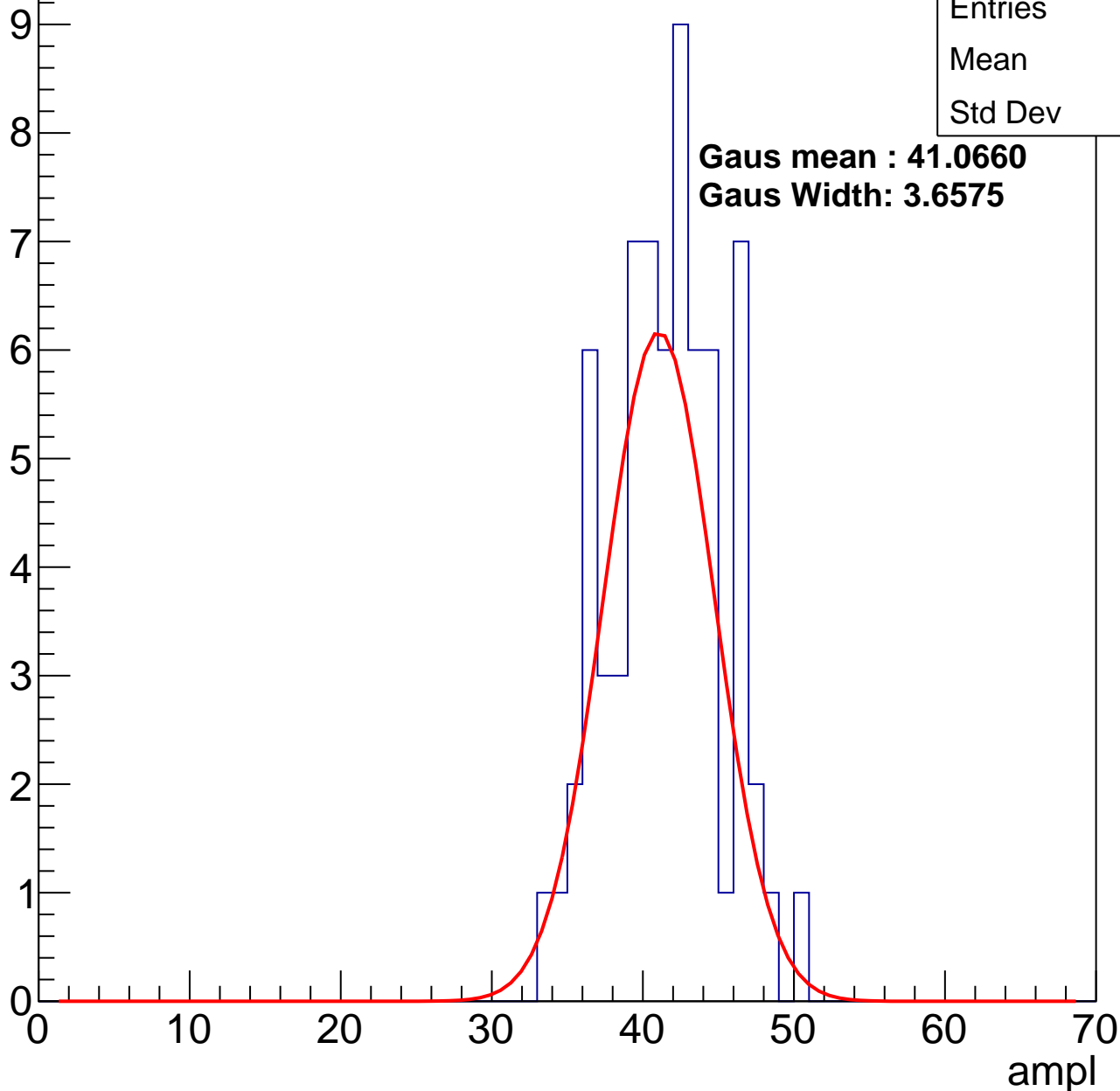
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	41.1
Std Dev	3.66

**Gaus mean : 41.0660**

**Gaus Width: 3.6575**

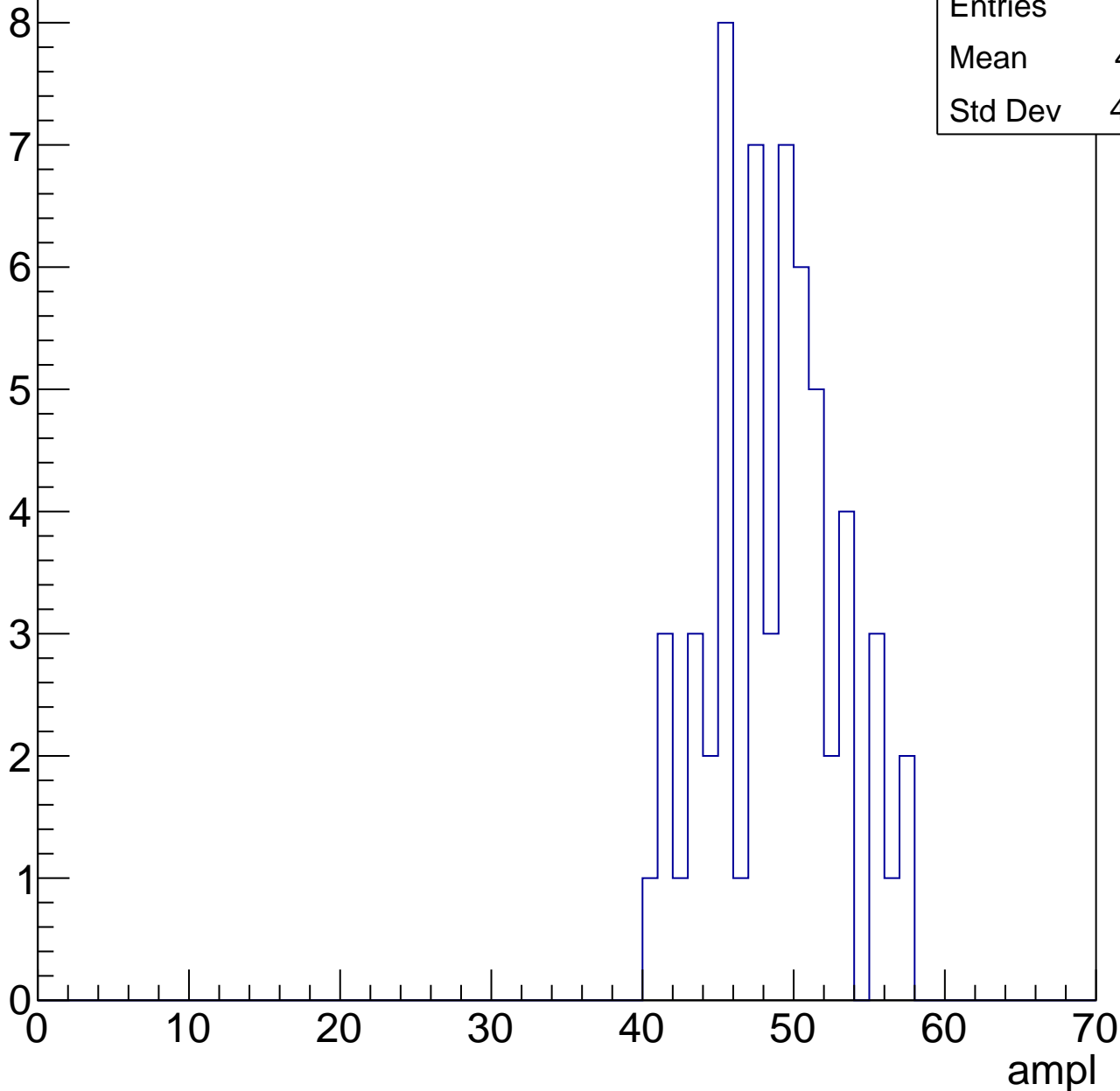


# B1L102S, U3-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	48.31
Std Dev	4.143

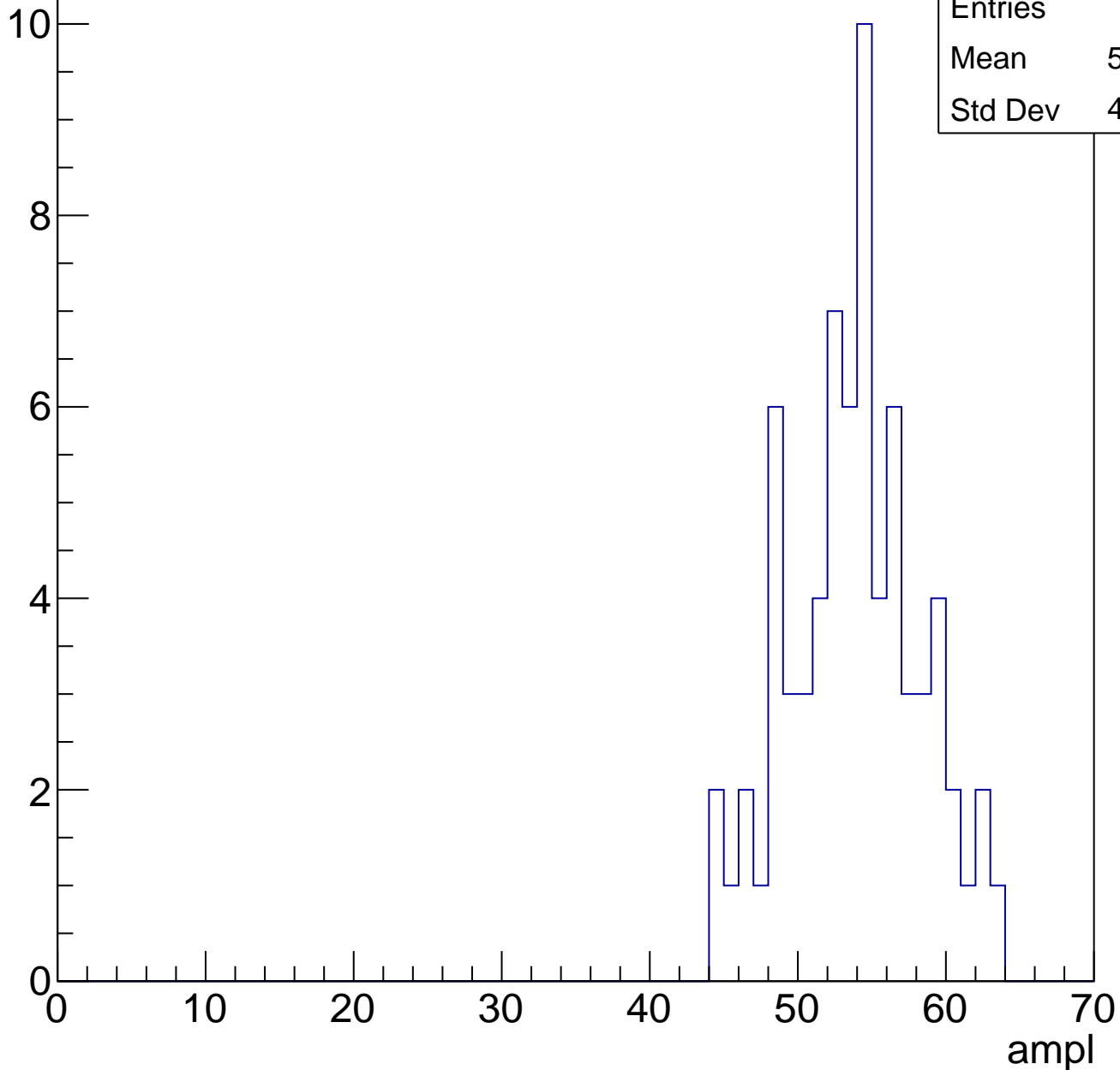


# B1L102S, U3-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	71
Mean	53.35
Std Dev	4.393

Entry

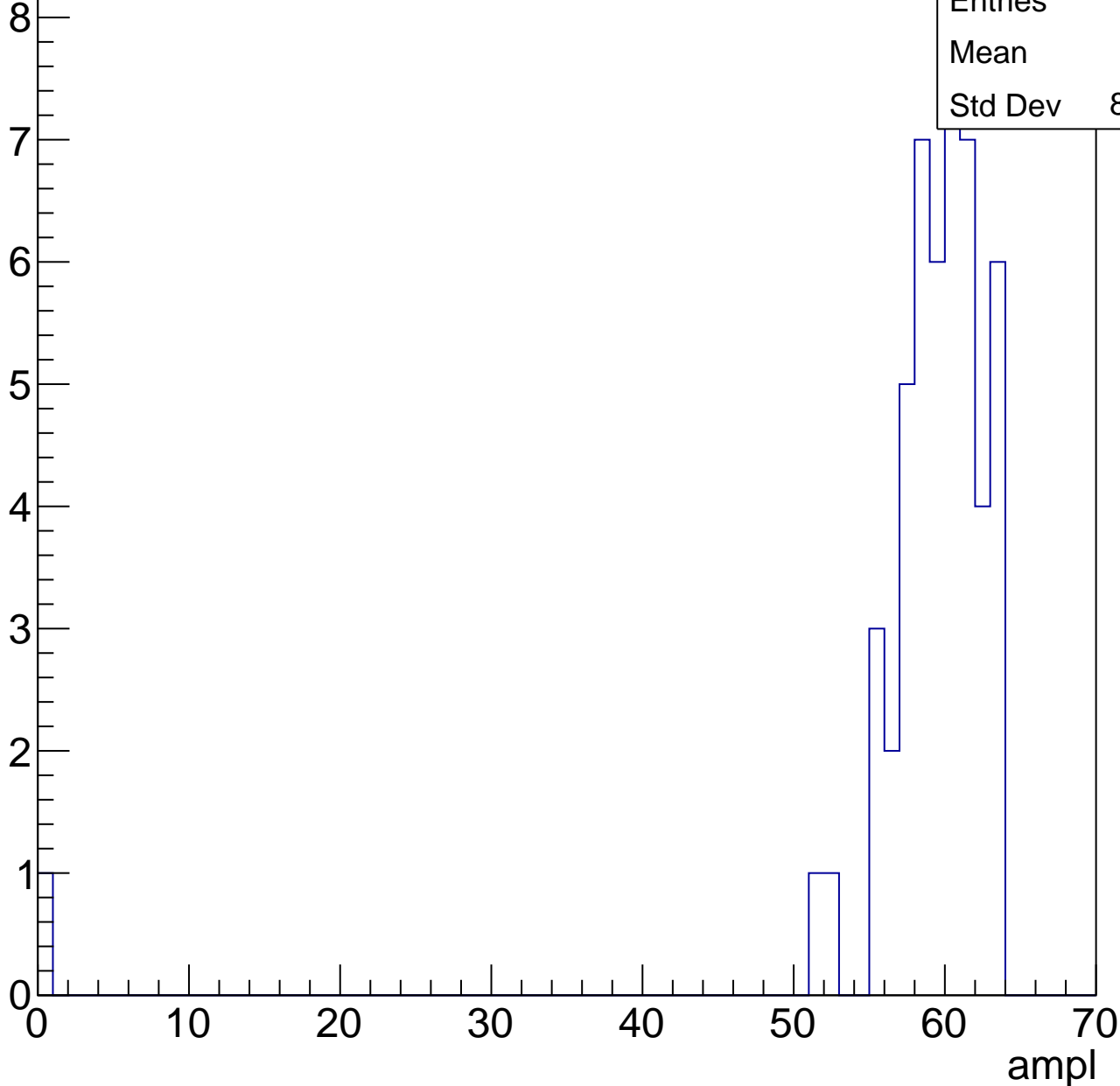


# B1L102S, U3-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

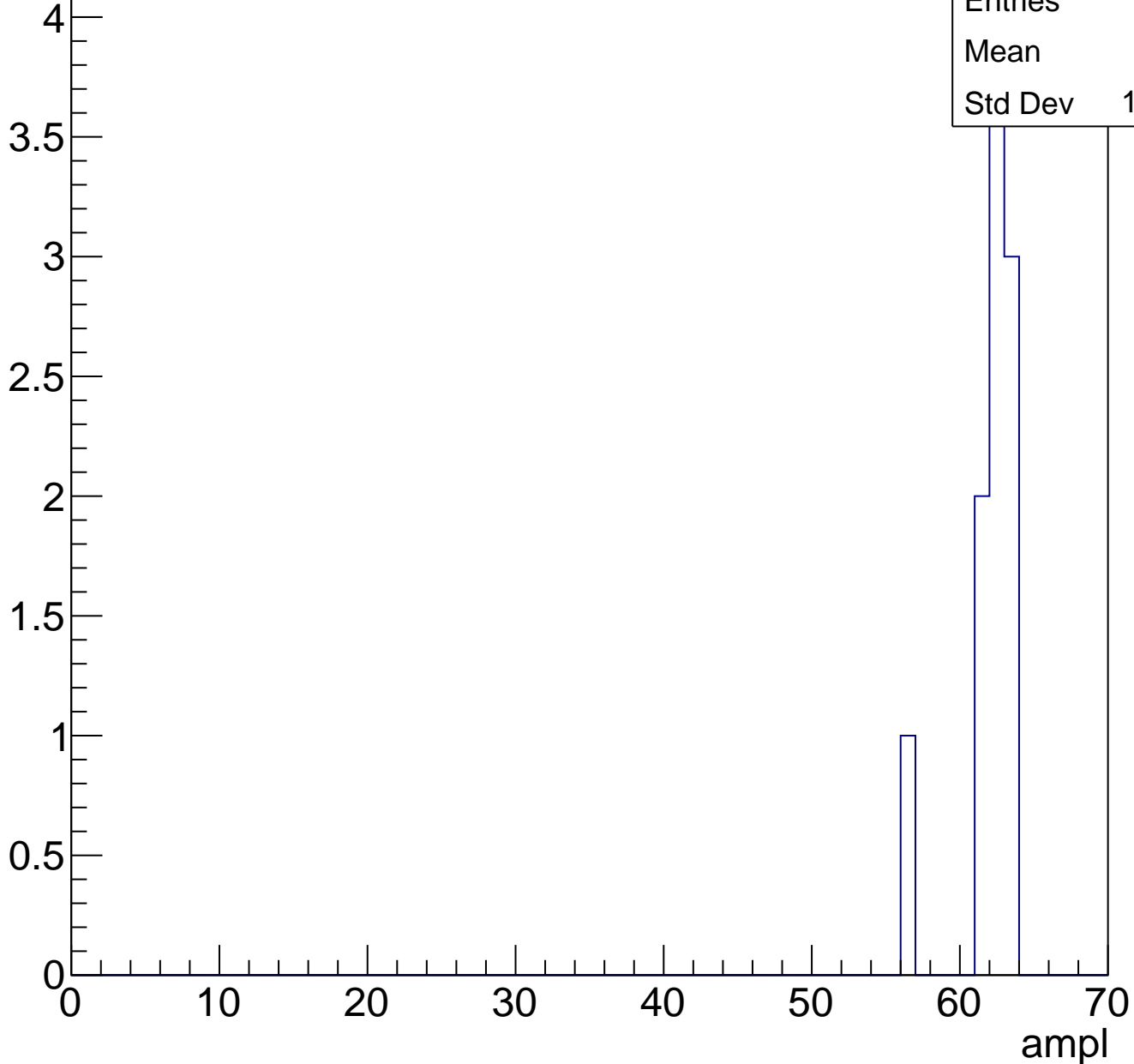
Entries	51
Mean	58
Std Dev	8.636



# B1L102S, U3-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch66, adc0

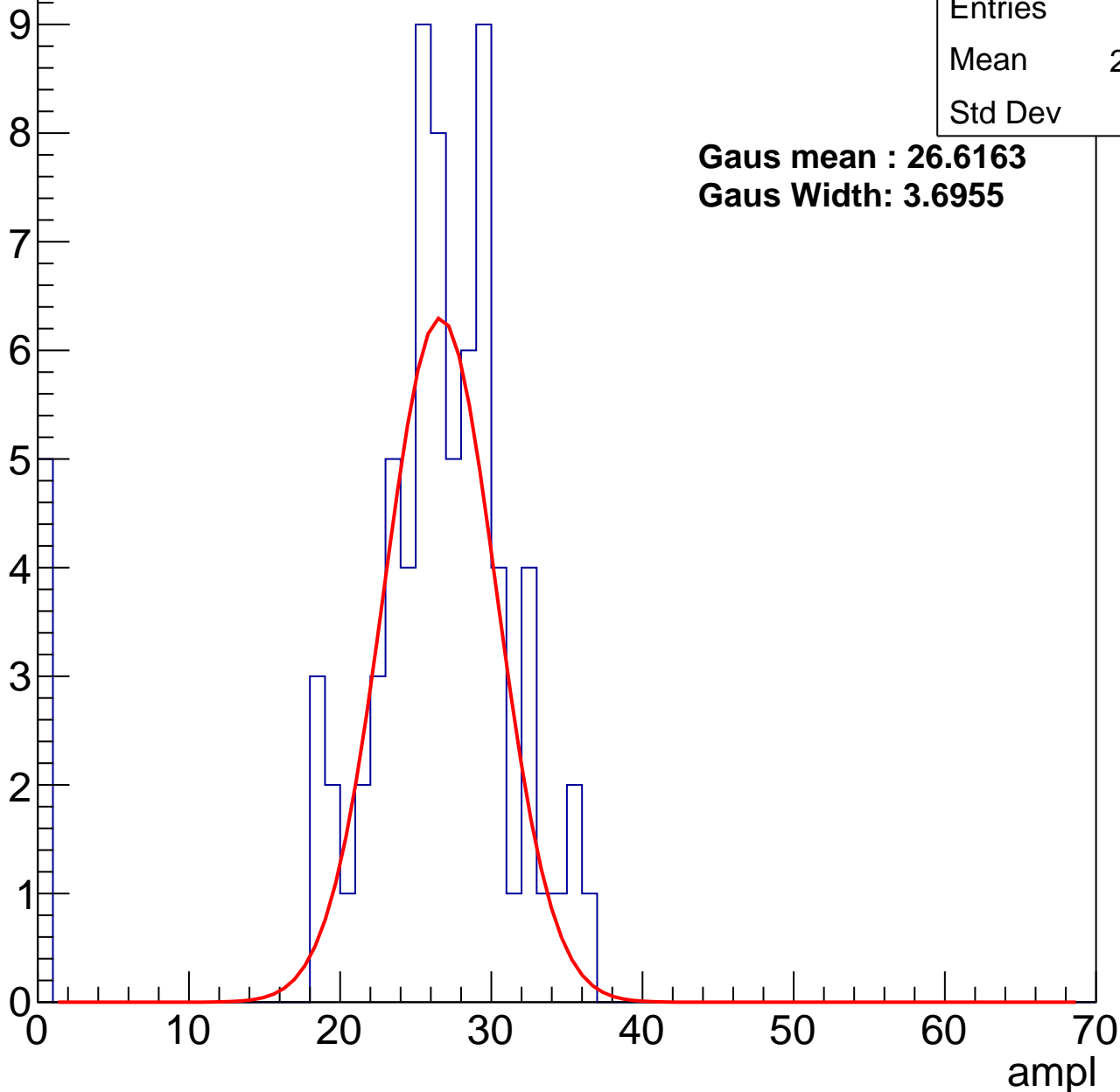
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	24.74
Std Dev	7.67

**Gaus mean : 26.6163**

**Gaus Width: 3.6955**



# B1L102S, U3-ch66, adc1

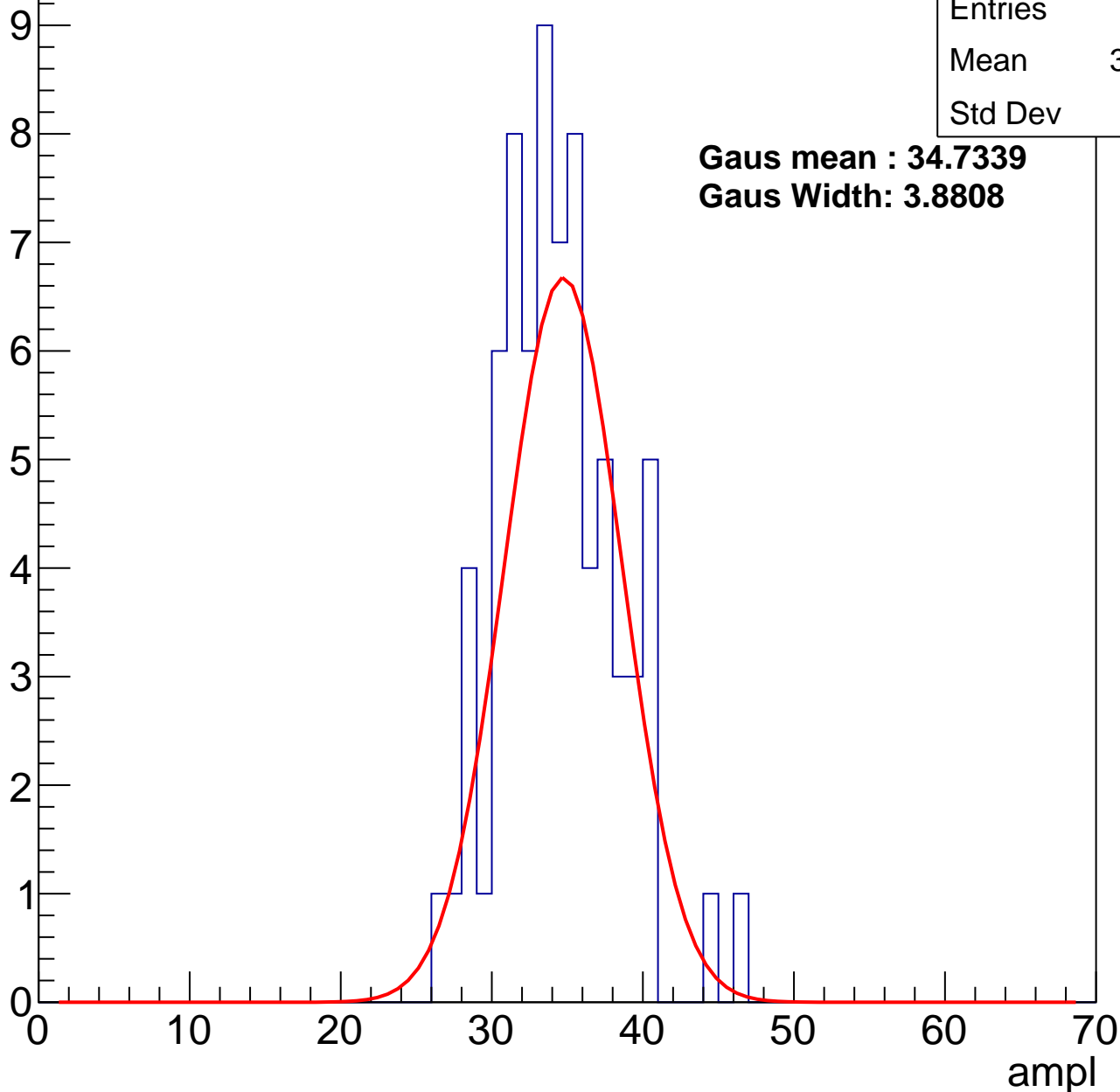
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	33.96
Std Dev	3.88

**Gaus mean : 34.7339**

**Gaus Width: 3.8808**



# B1L102S, U3-ch66, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	54
Mean	40.07
Std Dev	3.31

**Gaus mean : 39.7572**

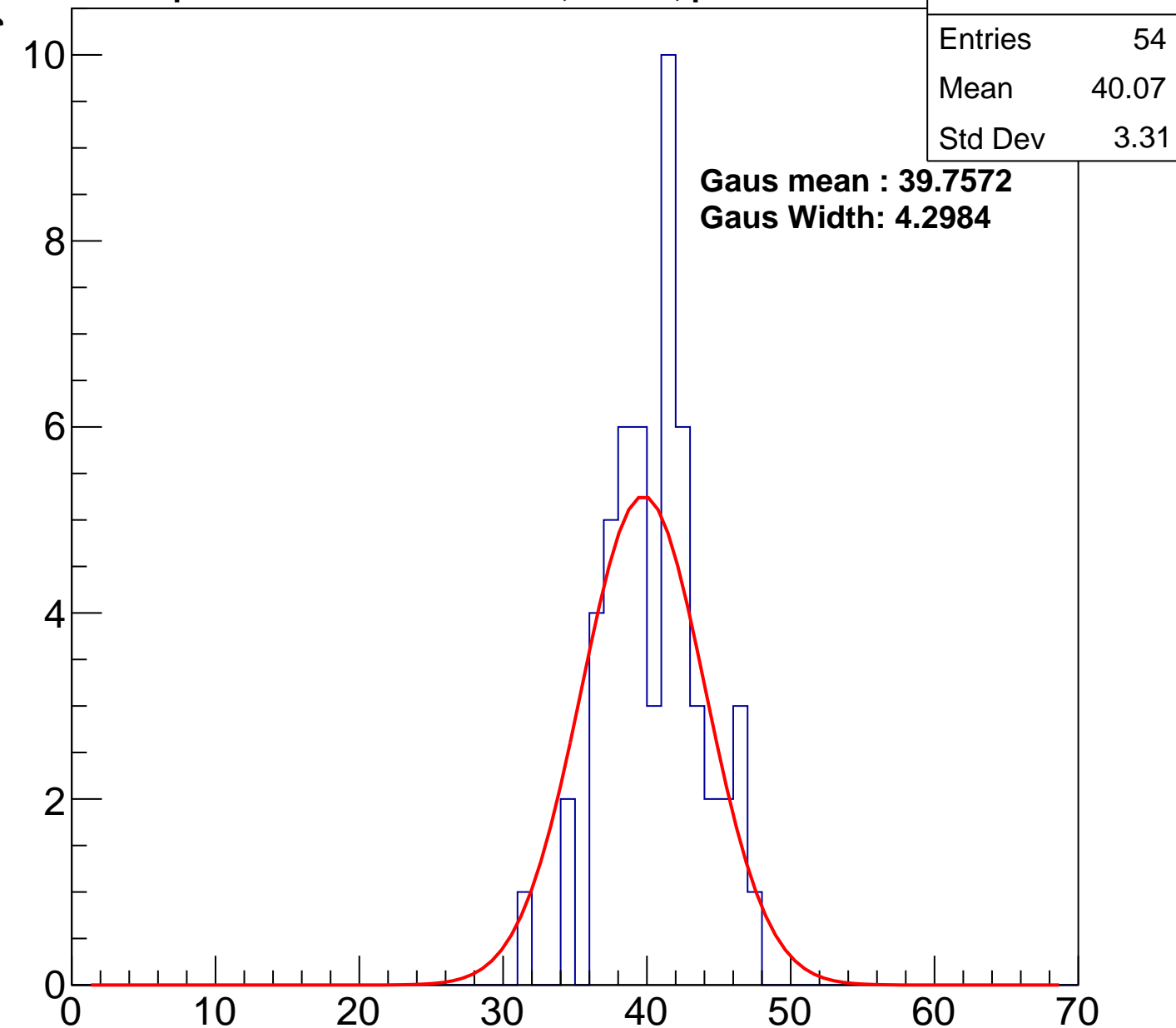
**Gaus Width: 4.2984**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

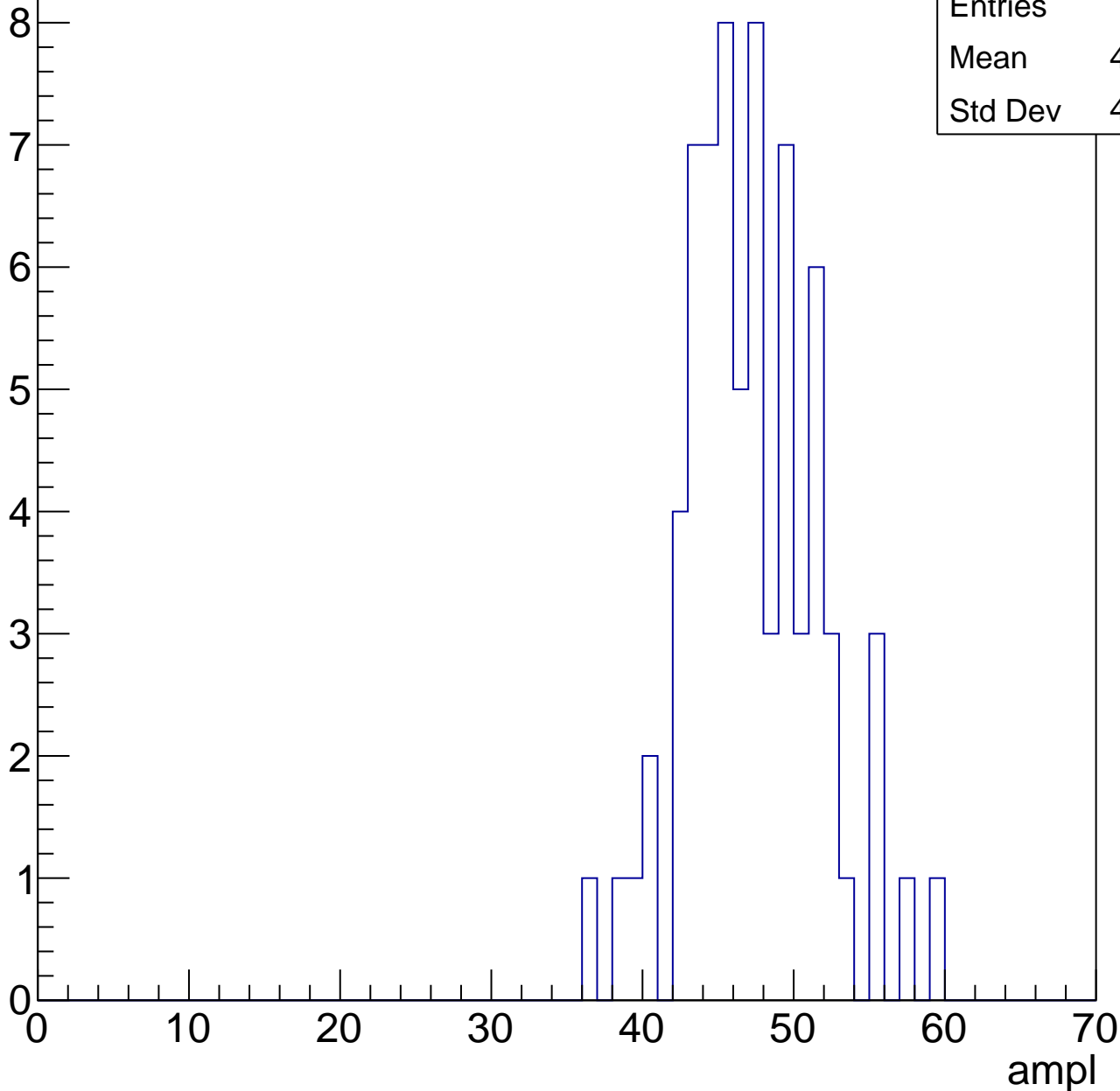


# B1L102S, U3-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	46.79
Std Dev	4.368

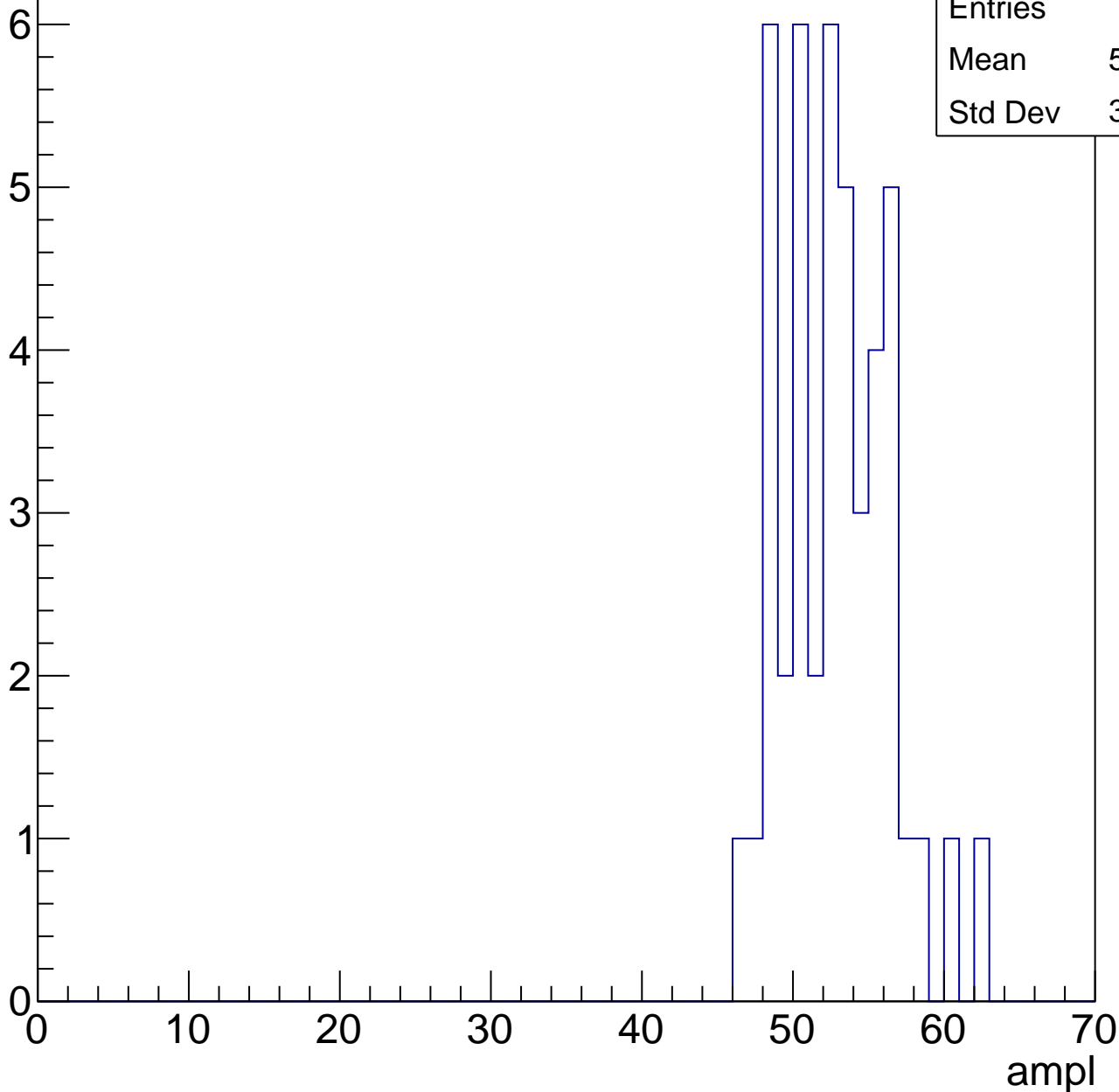


# B1L102S, U3-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	52.38
Std Dev	3.504

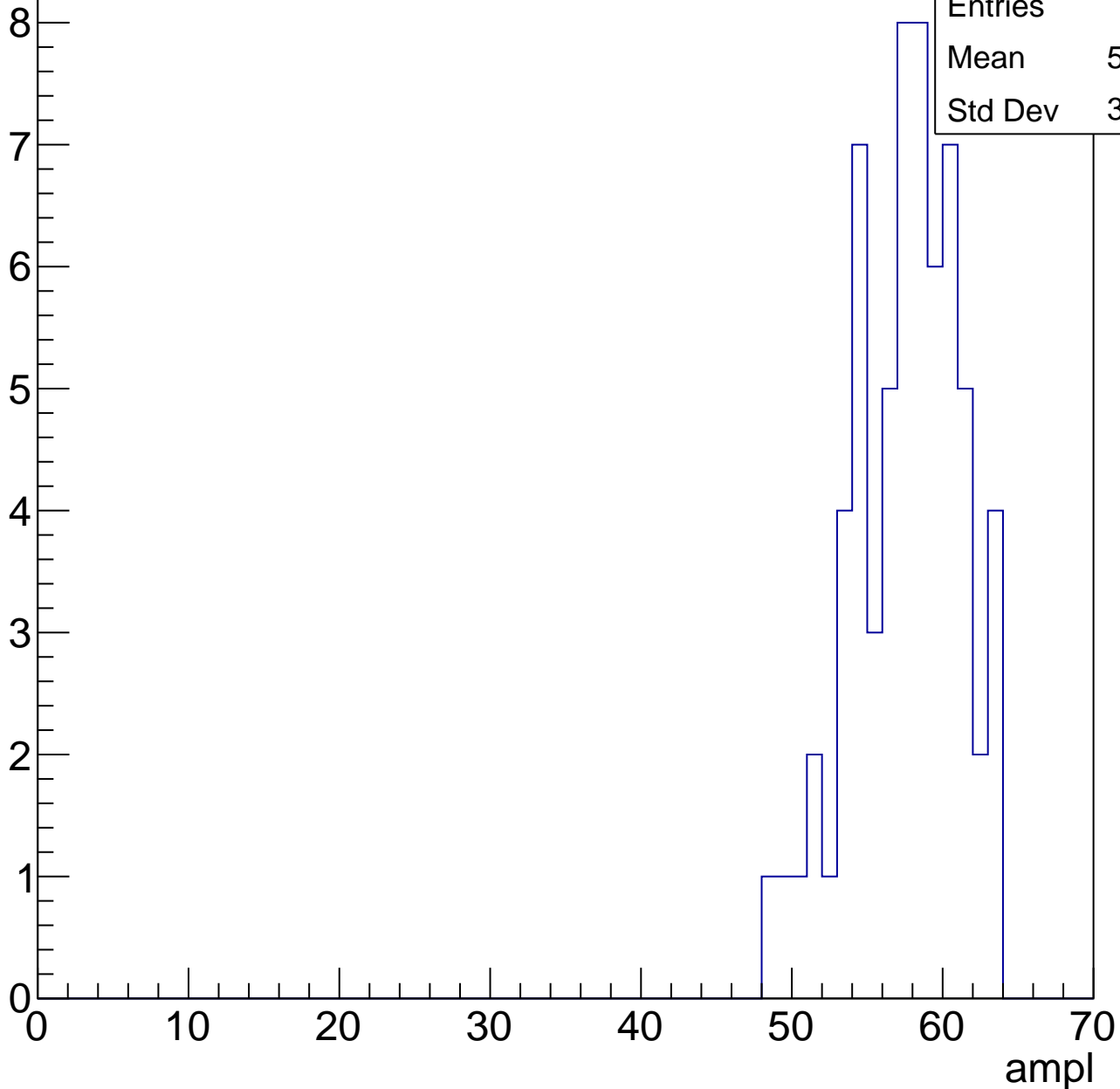


# B1L102S, U3-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	57.09
Std Dev	3.516

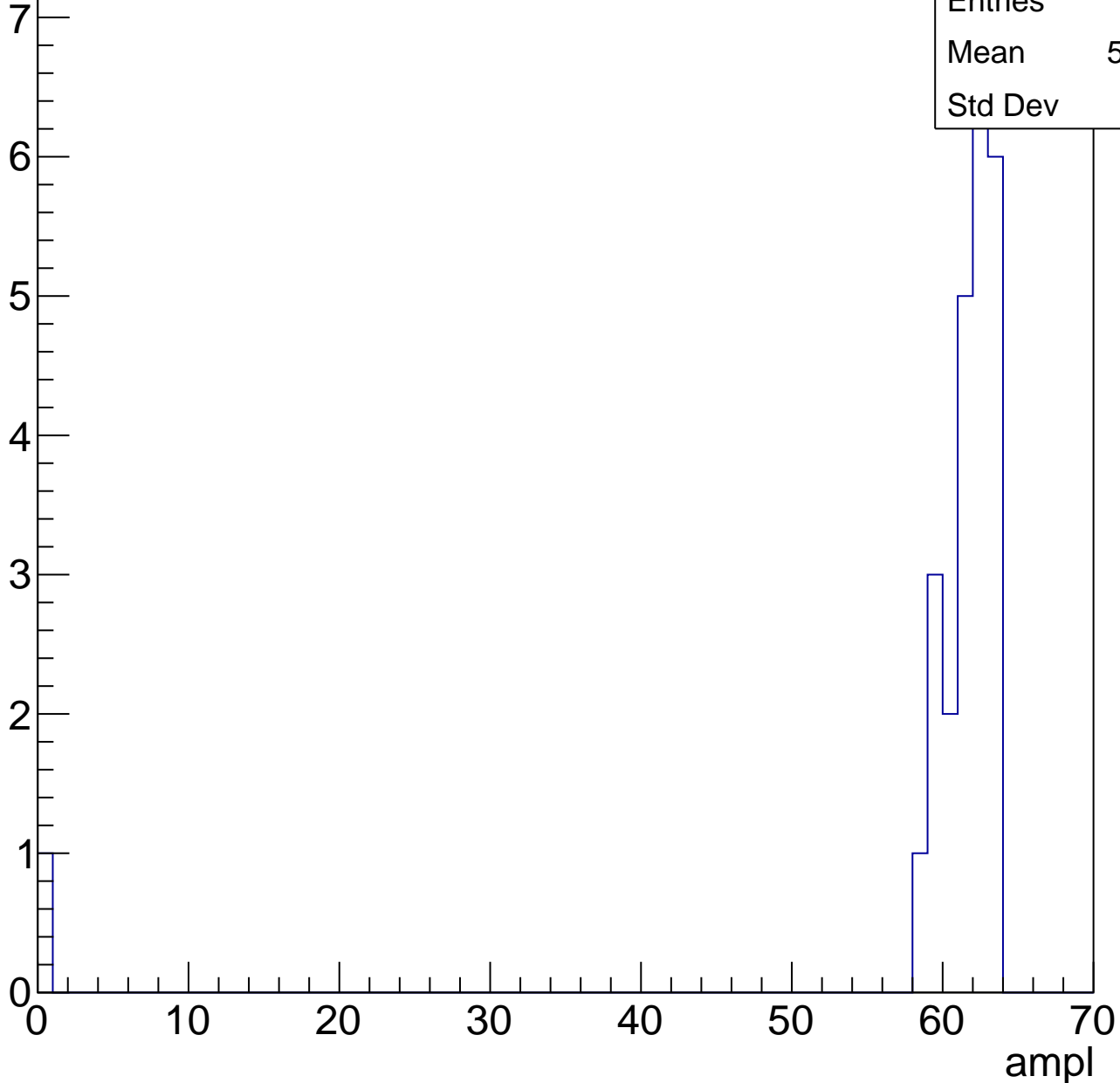


# B1L102S, U3-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	25
Mean	58.88
Std Dev	12.1





# B1L102S, U3-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch67, adc0

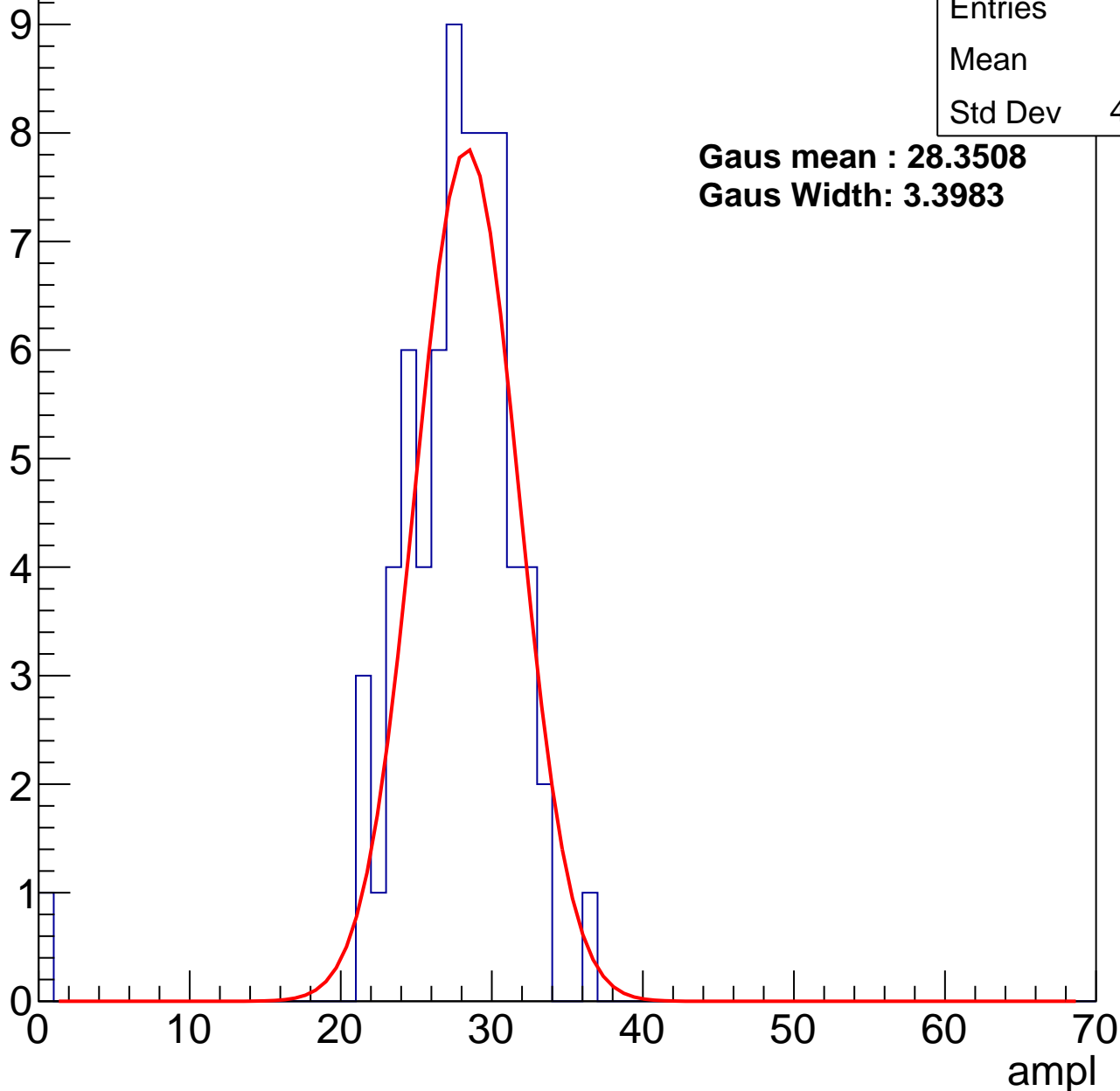
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	27.1
Std Dev	4.553

**Gaus mean : 28.3508**

**Gaus Width: 3.3983**



# B1L102S, U3-ch67, adc1

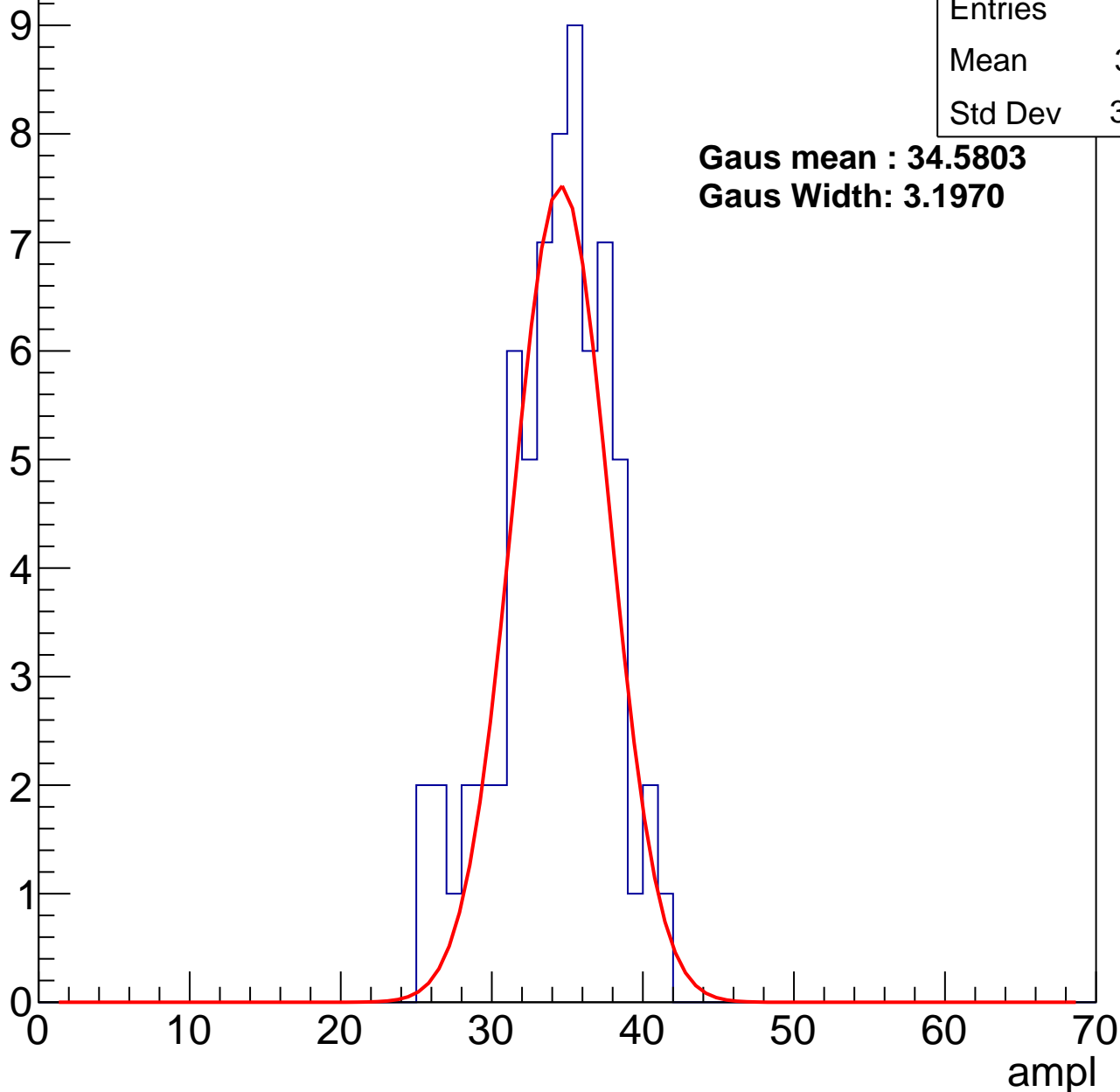
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	33.71
Std Dev	3.618

**Gaus mean : 34.5803**

**Gaus Width: 3.1970**



# B1L102S, U3-ch67, adc2

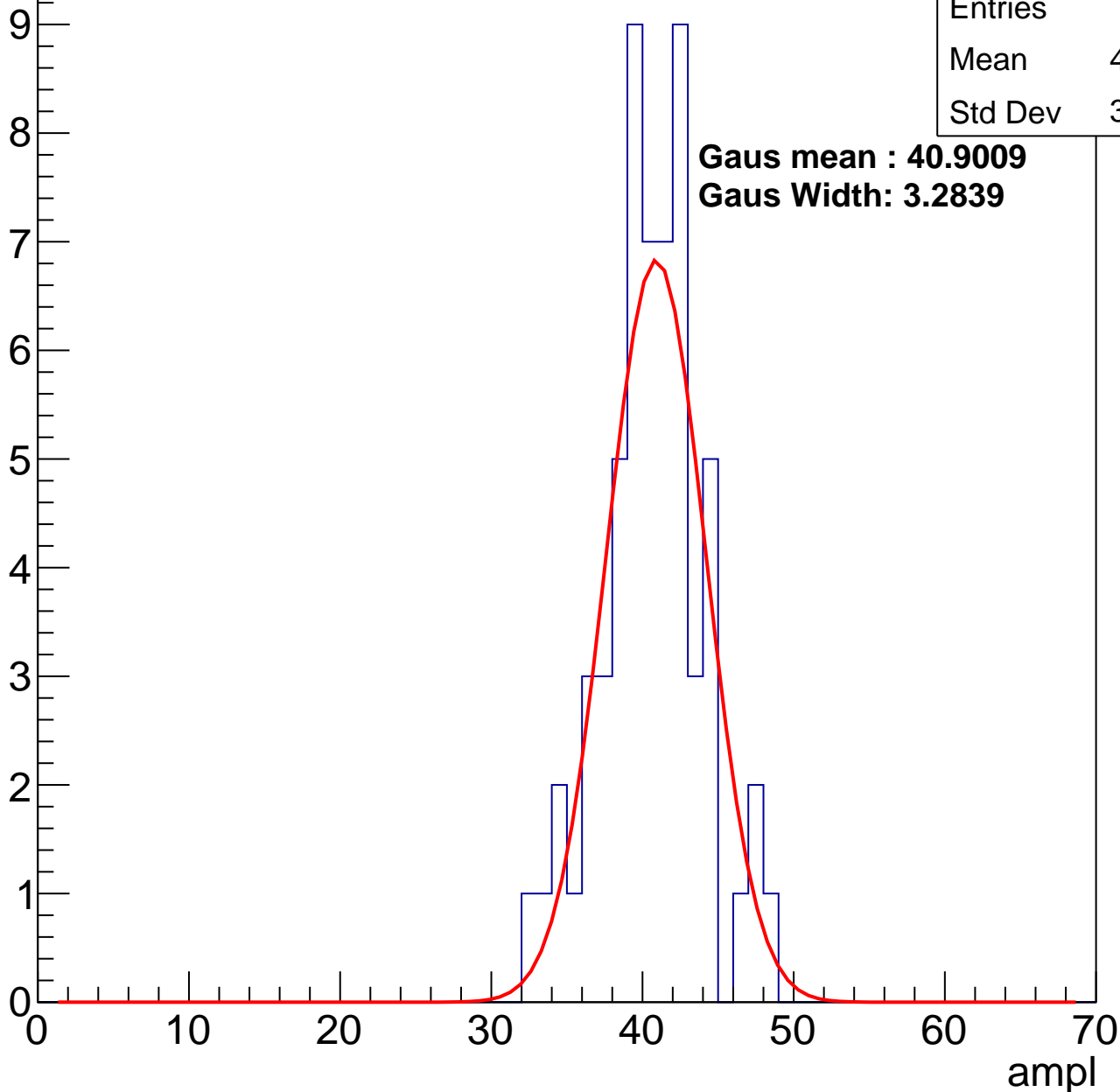
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	40.17
Std Dev	3.317

**Gaus mean : 40.9009**

**Gaus Width: 3.2839**



# B1L102S, U3-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

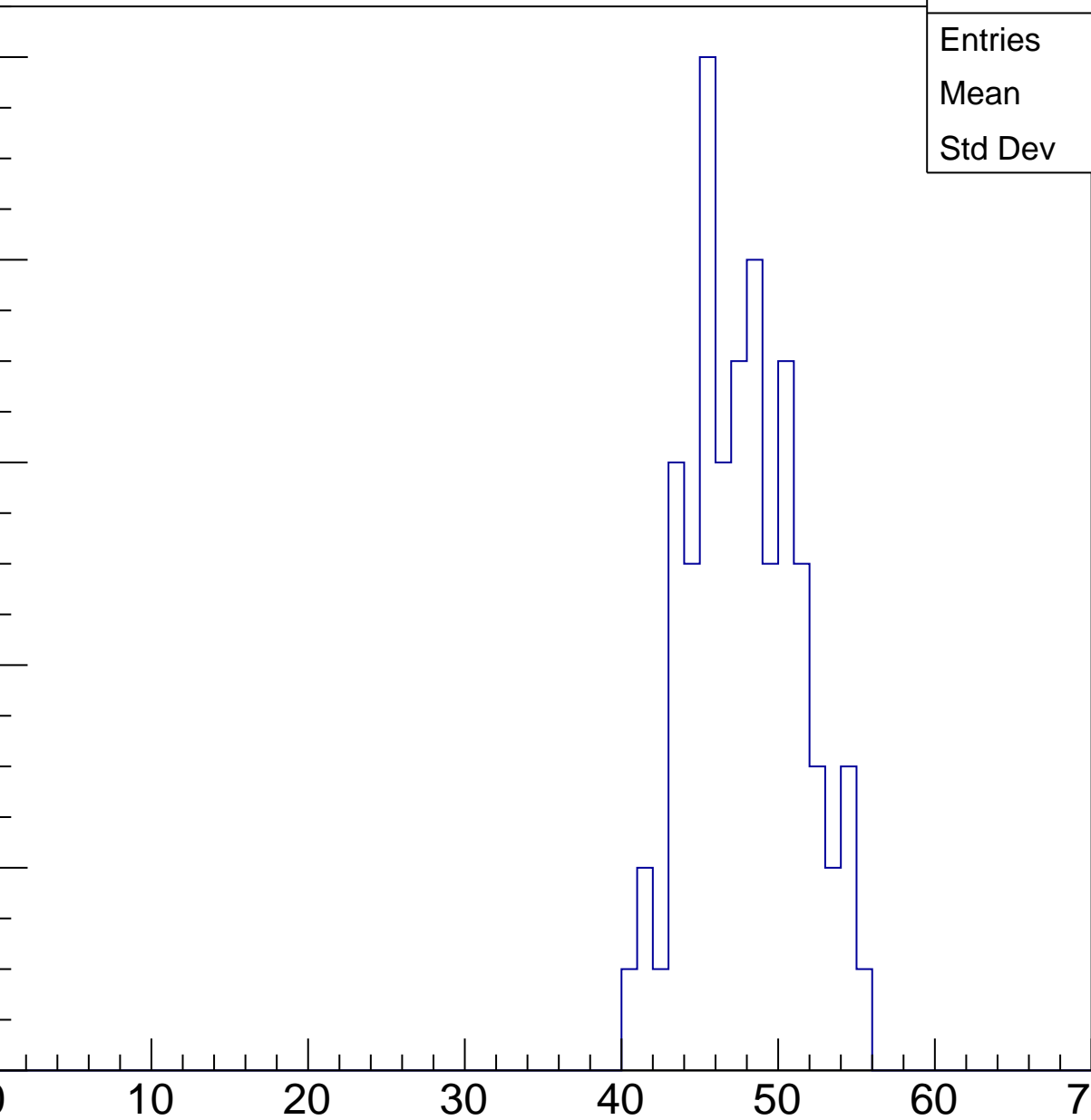
Entries	72
Mean	47.36
Std Dev	3.441

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

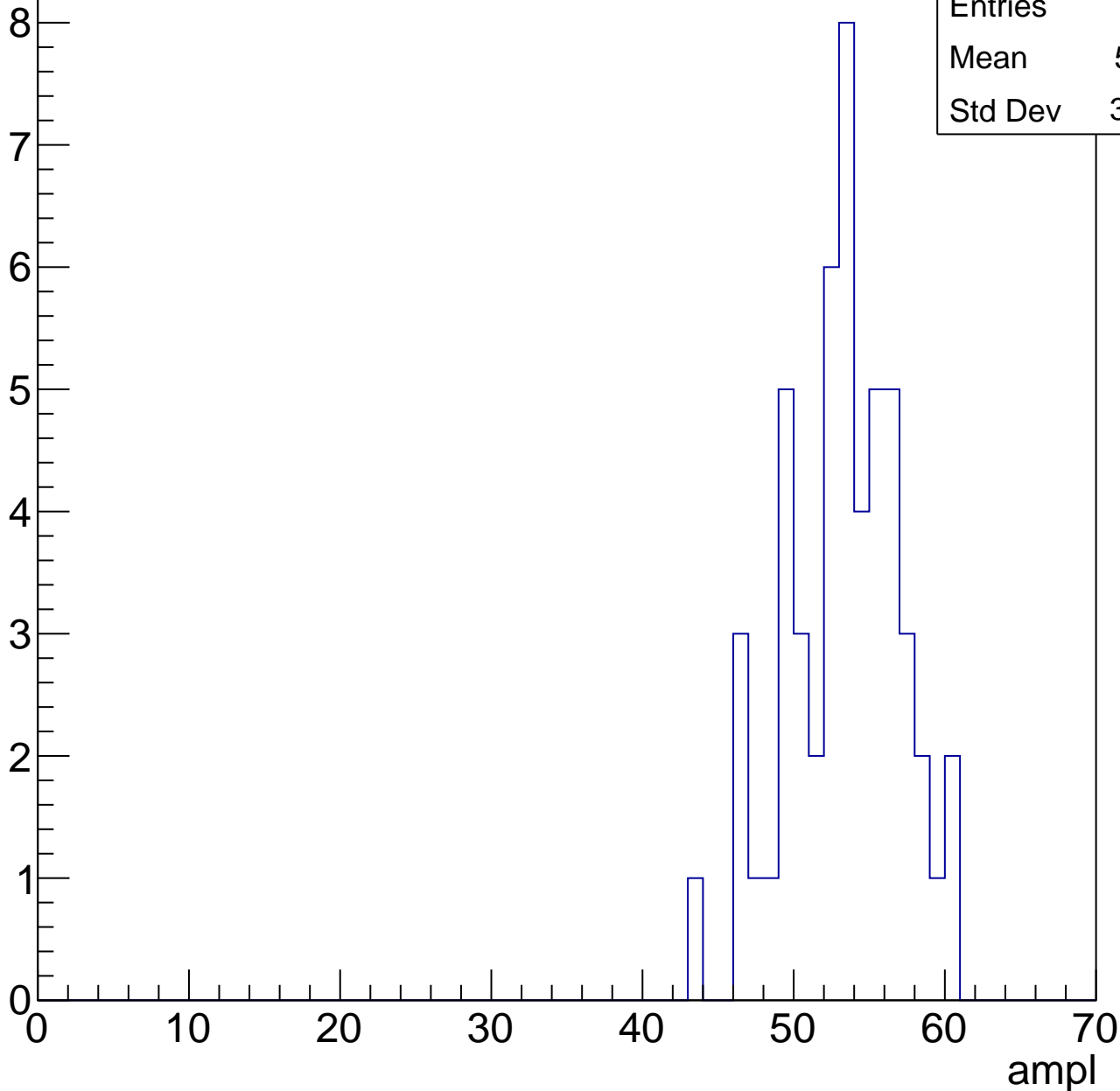


# B1L102S, U3-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	52.81
Std Dev	3.742

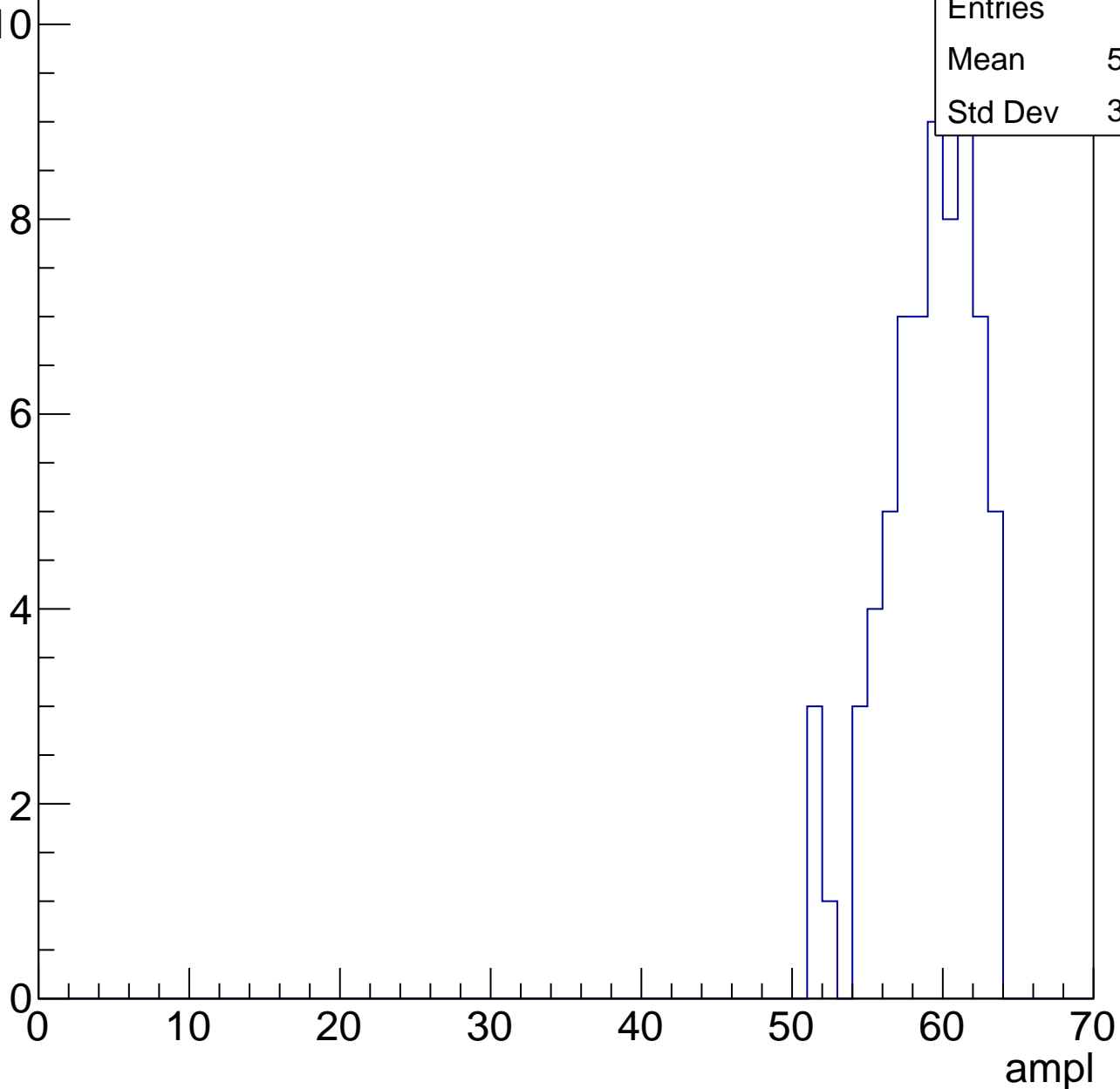


# B1L102S, U3-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

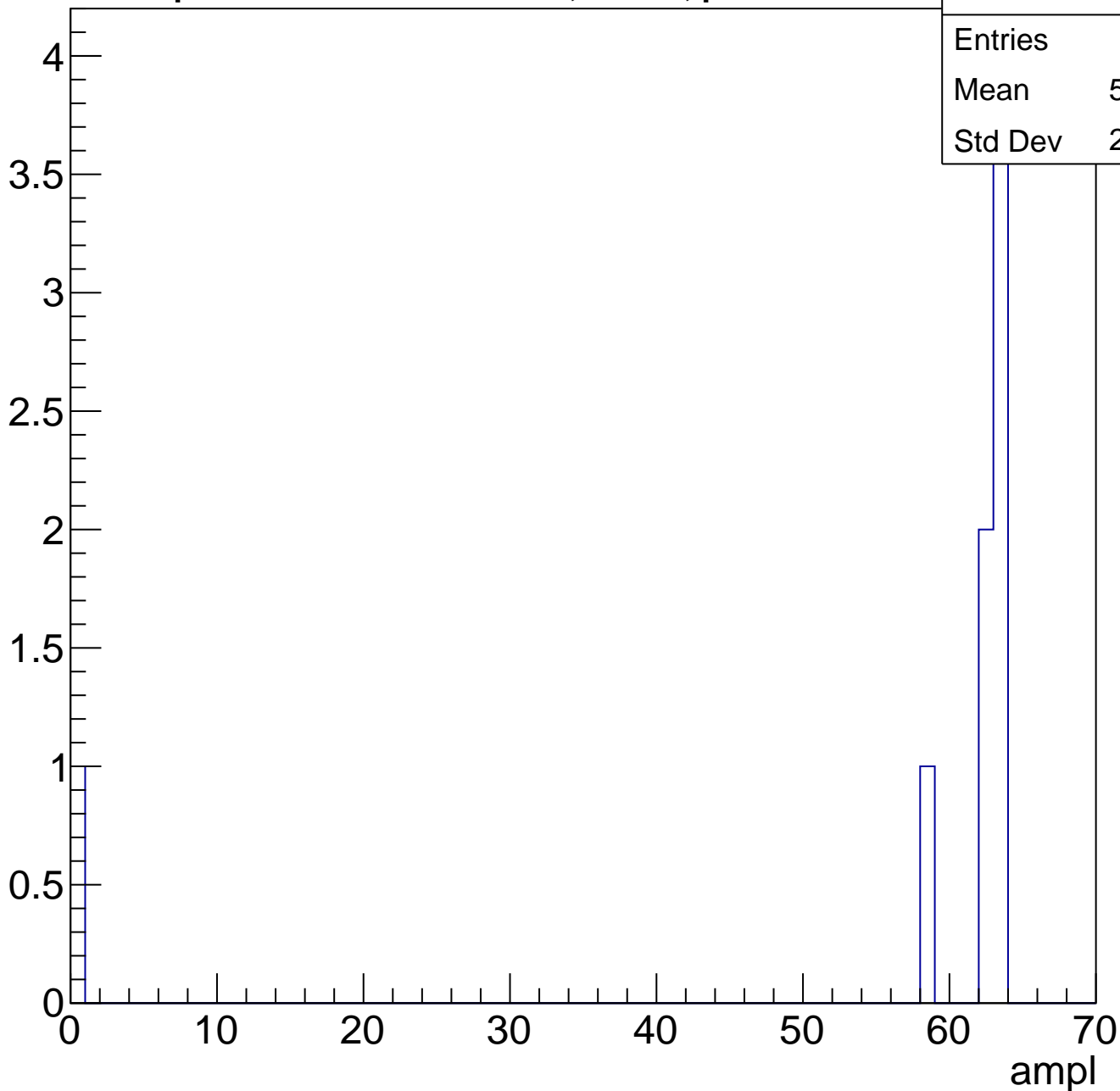
Entries	69
Mean	58.58
Std Dev	3.043



# B1L102S, U3-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch68, adc0

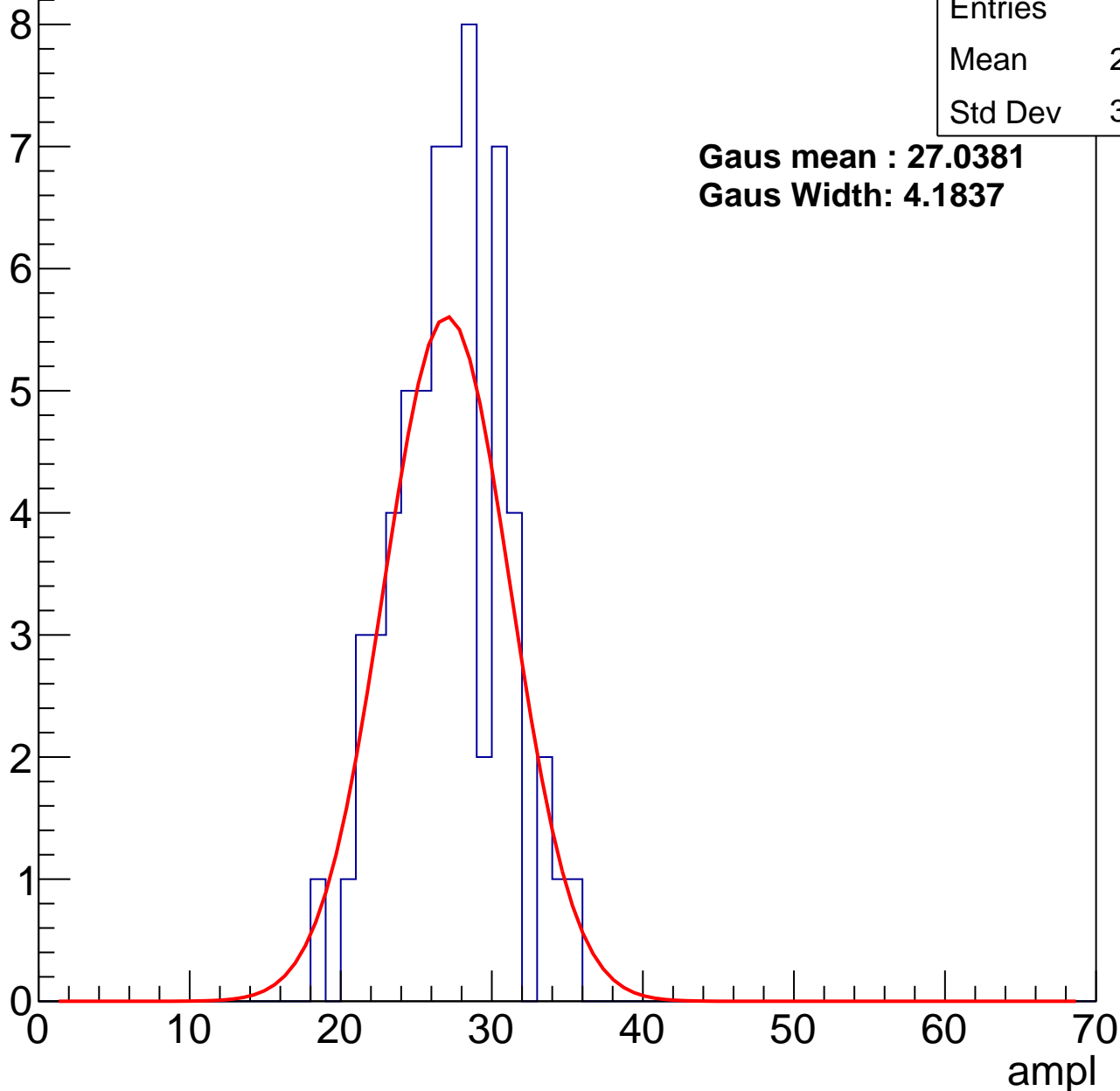
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	26.66
Std Dev	3.552

**Gaus mean : 27.0381**

**Gaus Width: 4.1837**



# B1L102S, U3-ch68, adc1

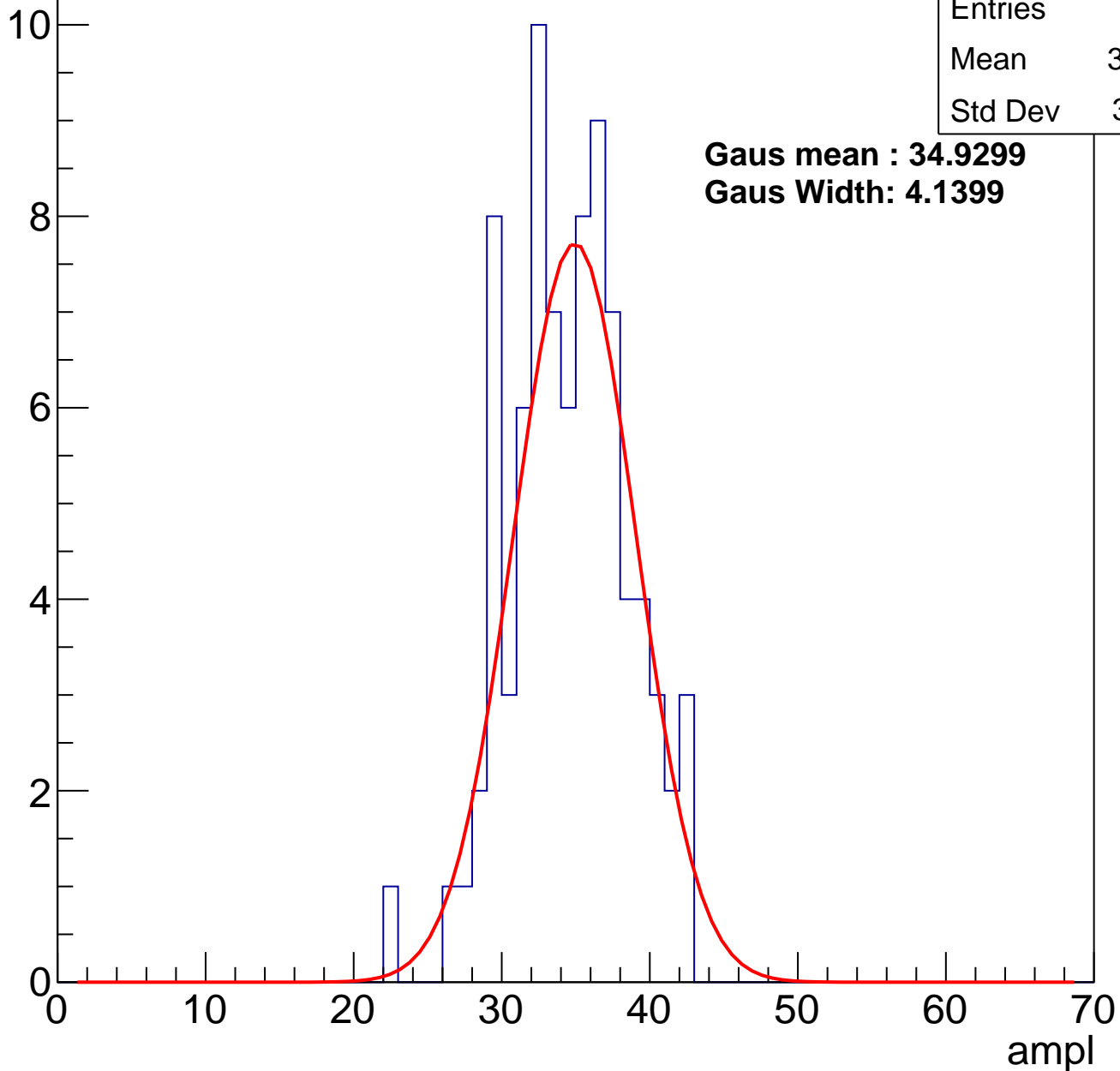
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	85
Mean	34.04
Std Dev	3.981

**Gaus mean : 34.9299**

**Gaus Width: 4.1399**

Entry



# B1L102S, U3-ch68, adc2

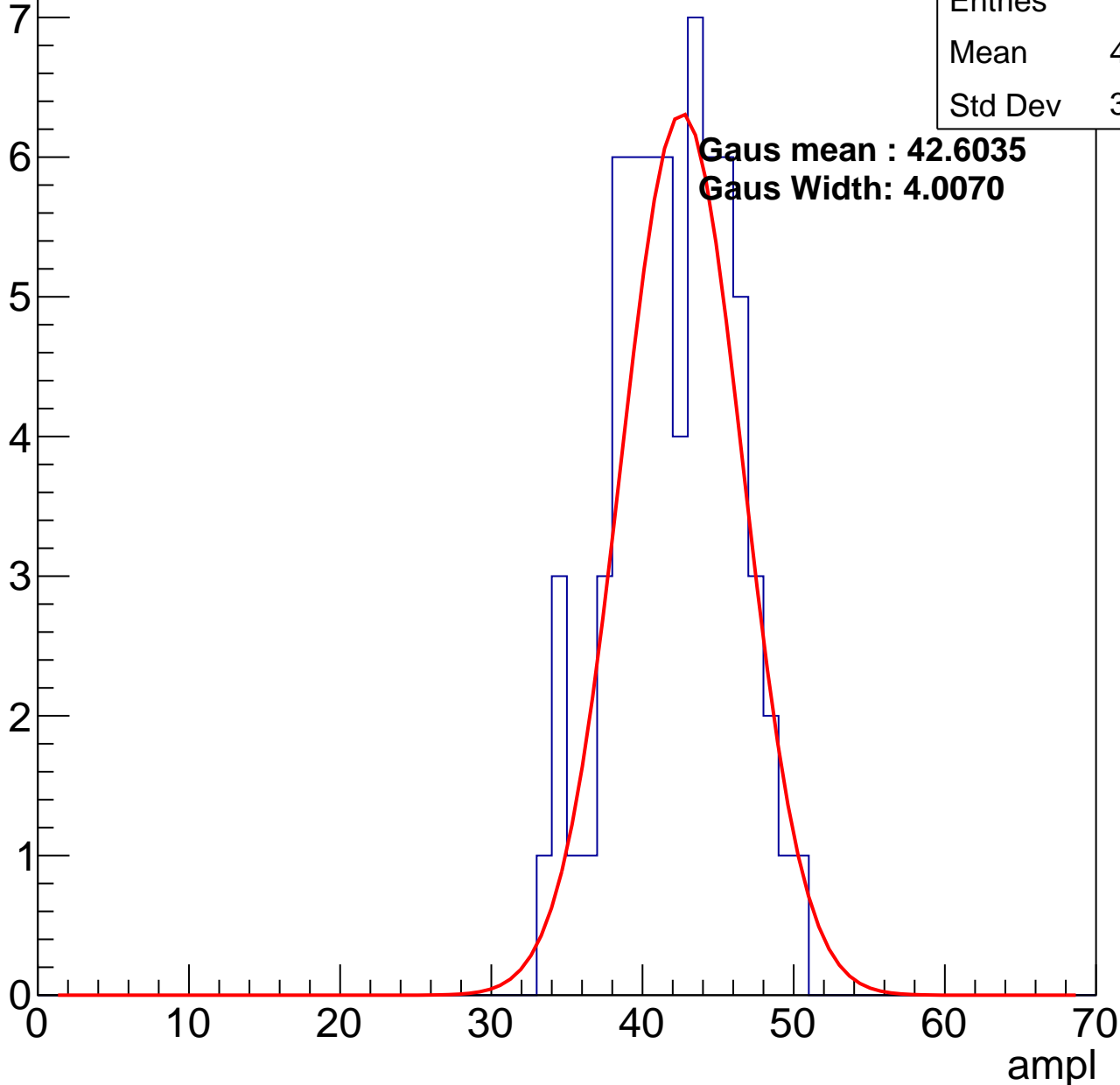
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	41.68
Std Dev	3.894

**Gaus mean : 42.6035**

**Gaus Width: 4.0070**

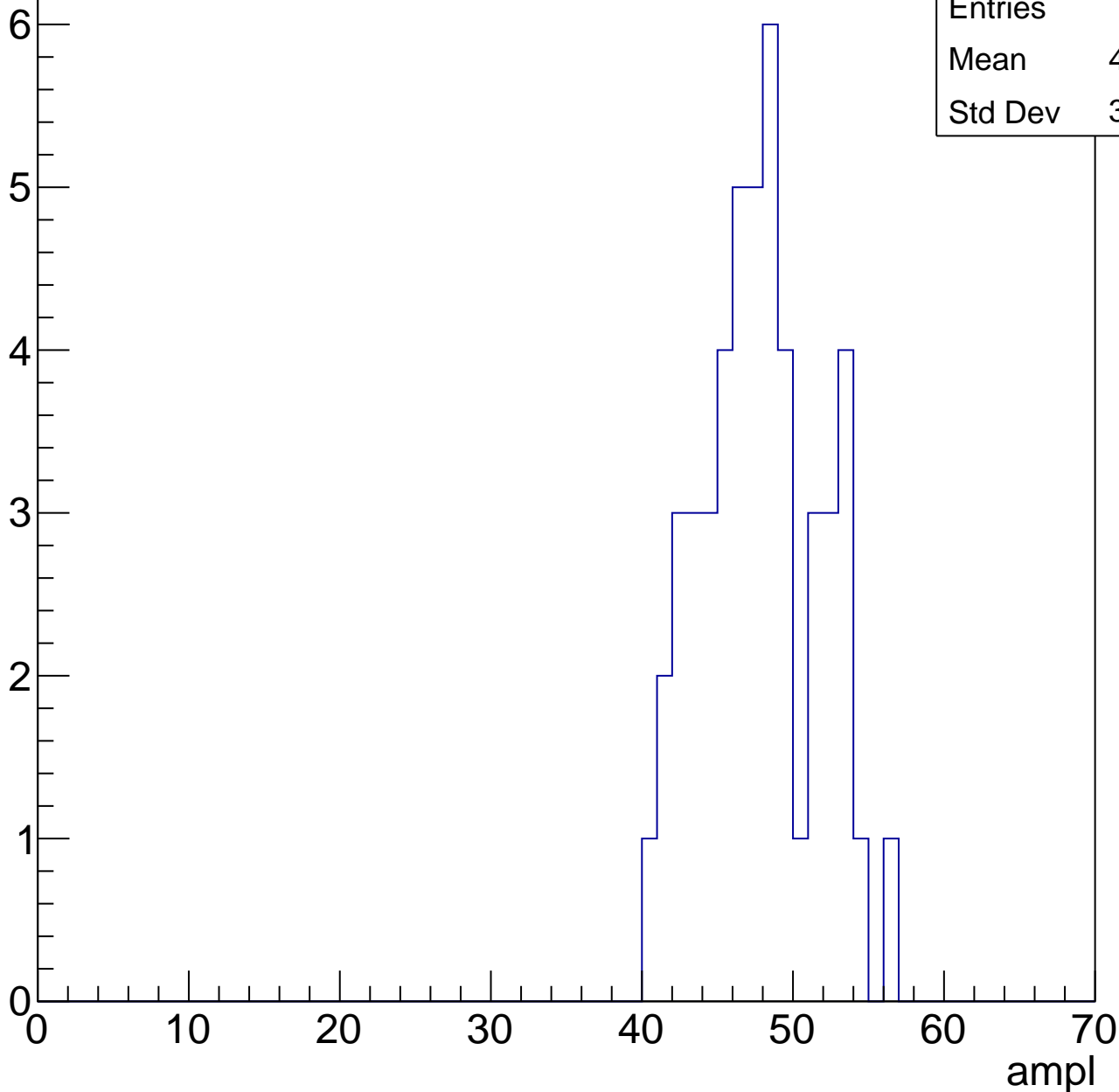


# B1L102S, U3-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	47.33
Std Dev	3.819

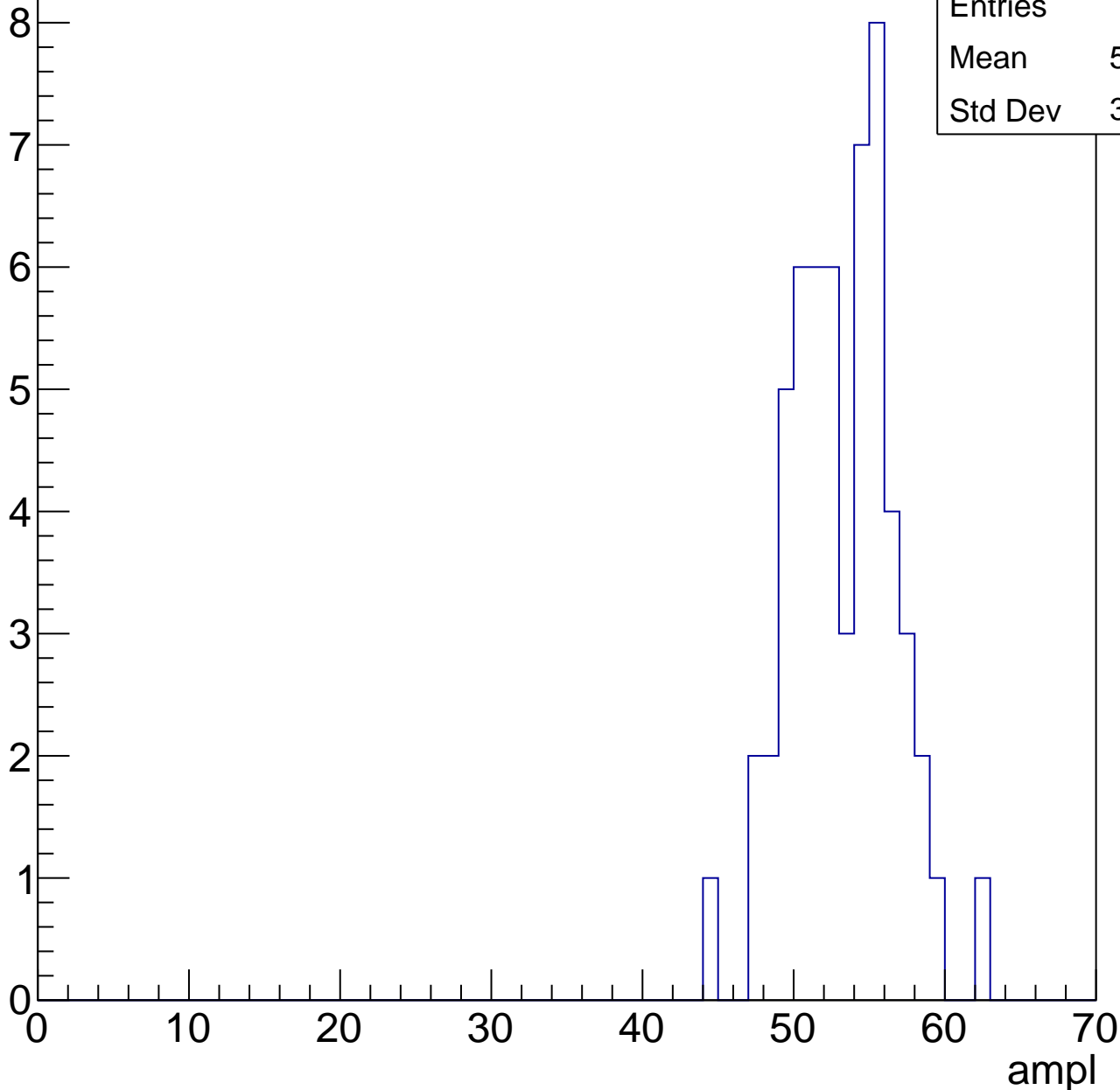


# B1L102S, U3-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	52.74
Std Dev	3.385

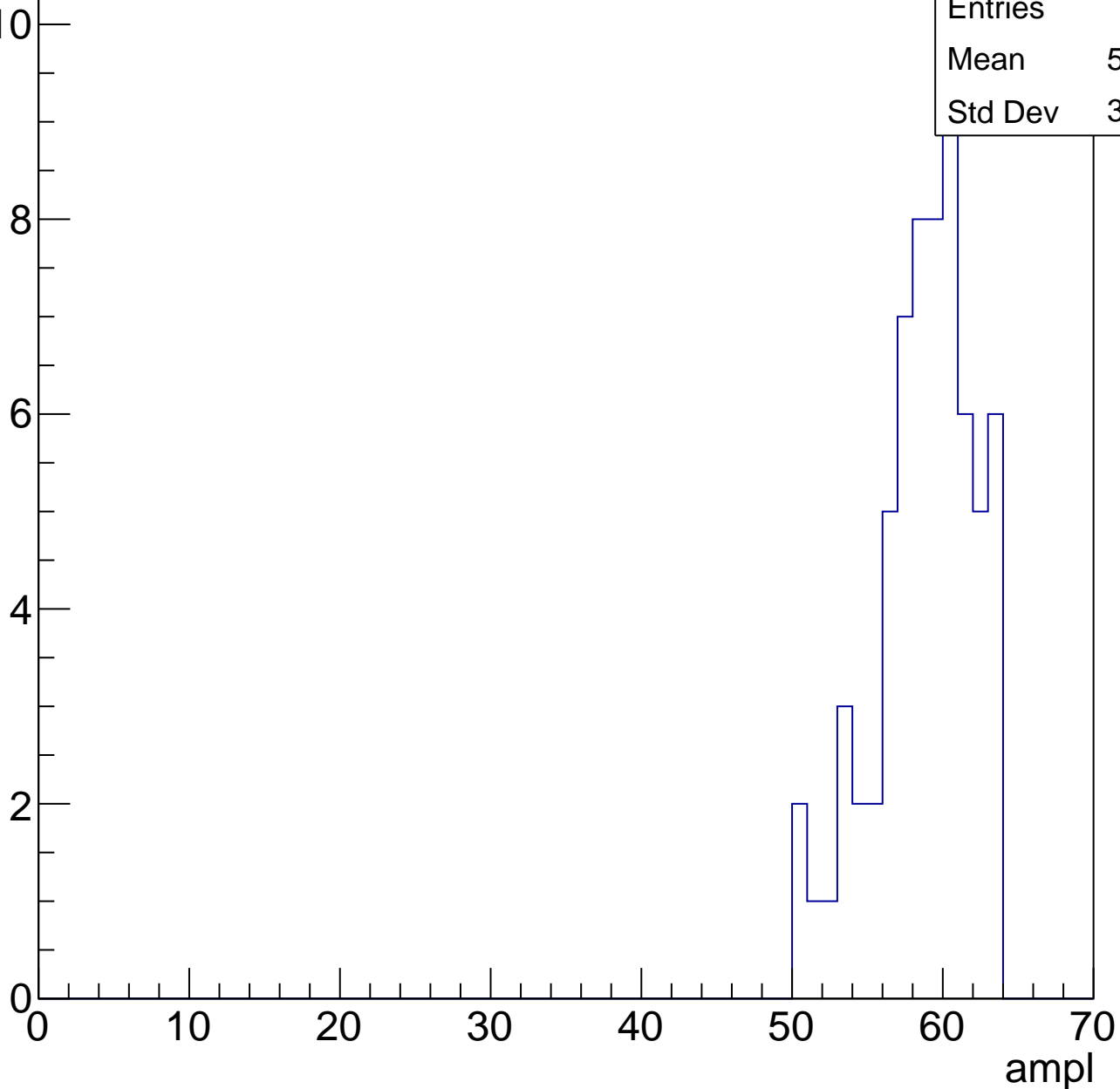


# B1L102S, U3-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

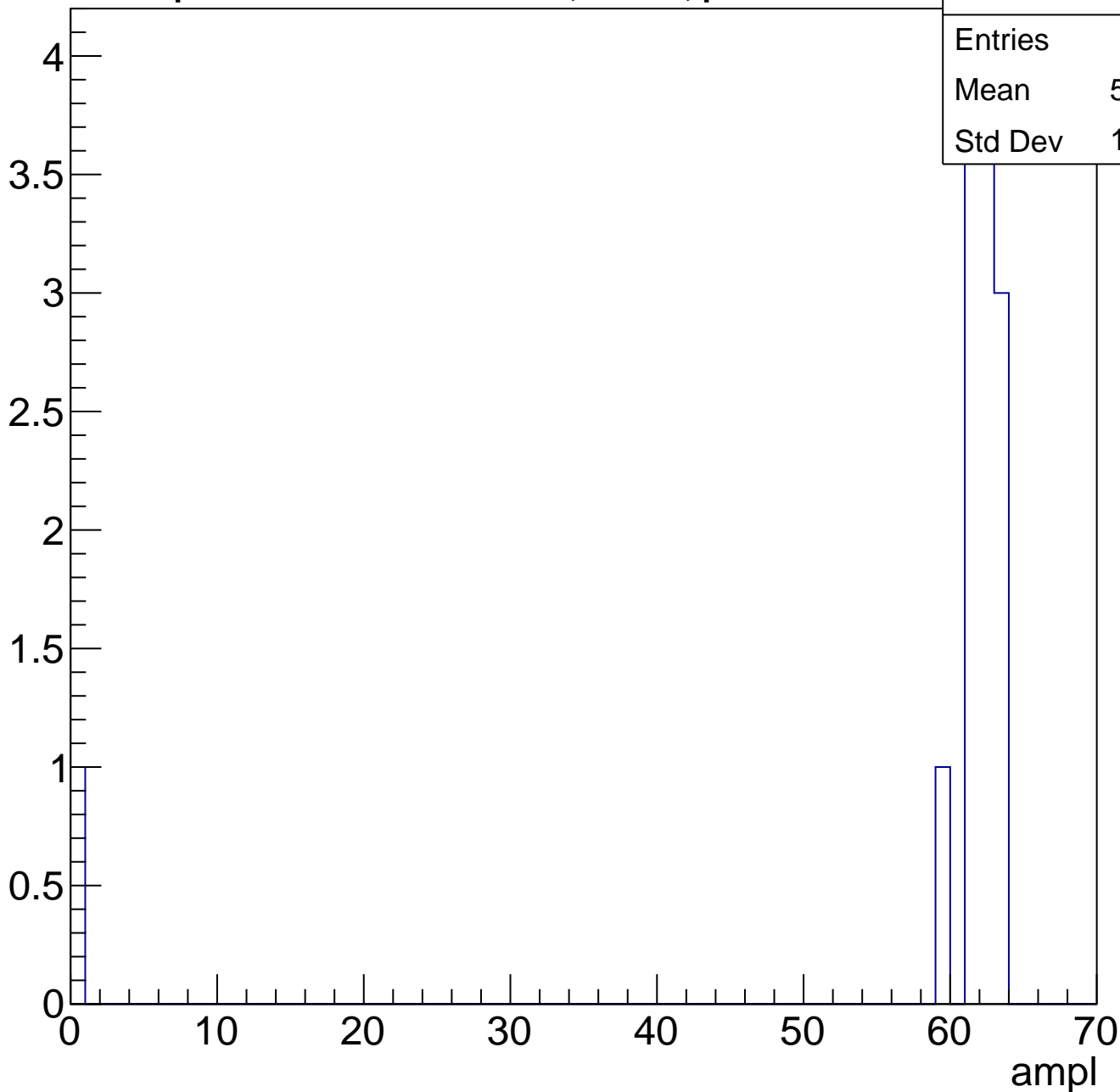
Entries	66
Mean	58.32
Std Dev	3.234



# B1L102S, U3-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L102S, U3-ch69, adc0

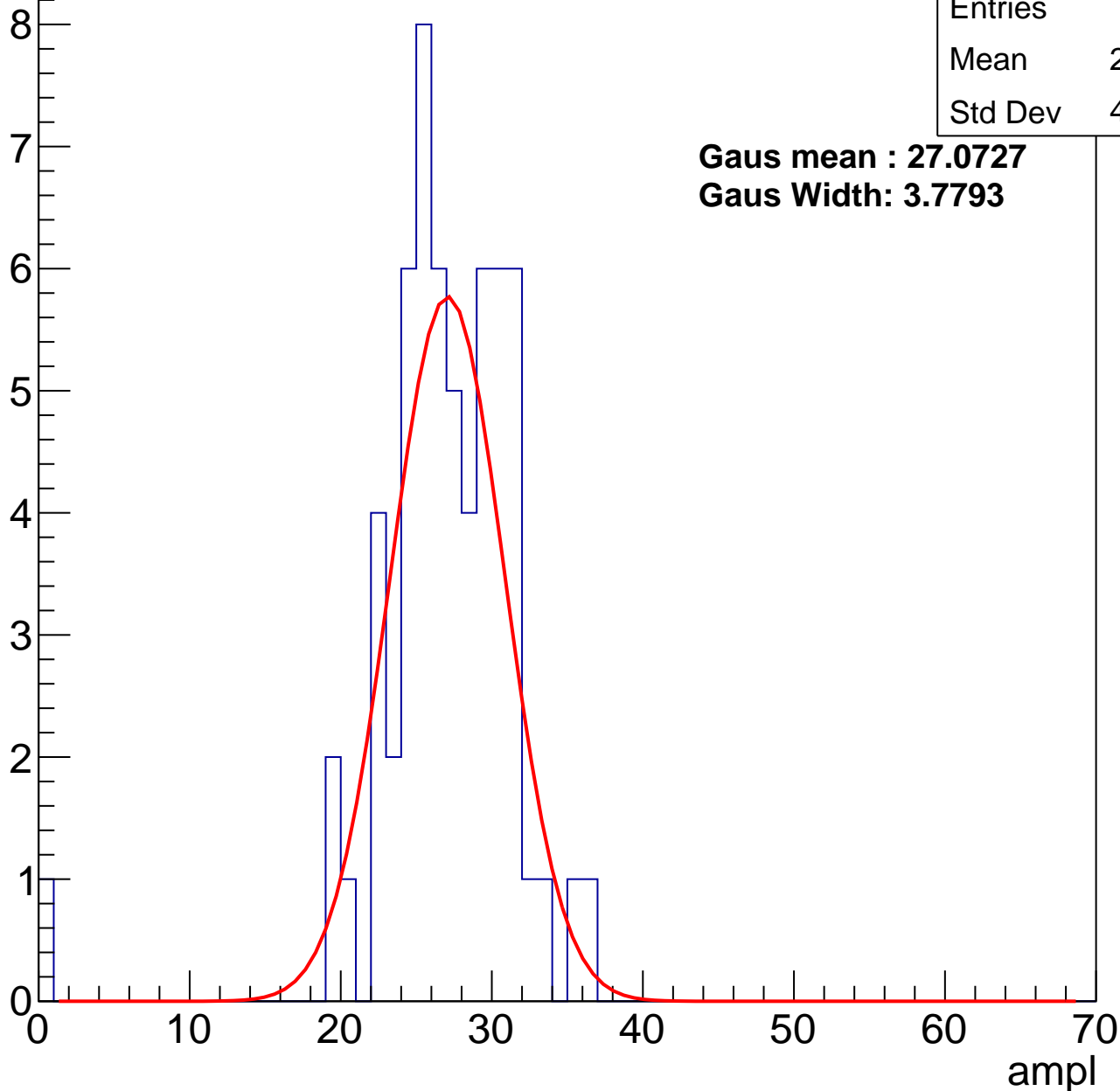
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	26.48
Std Dev	4.954

**Gaus mean : 27.0727**

**Gaus Width: 3.7793**



# B1L102S, U3-ch69, adc1

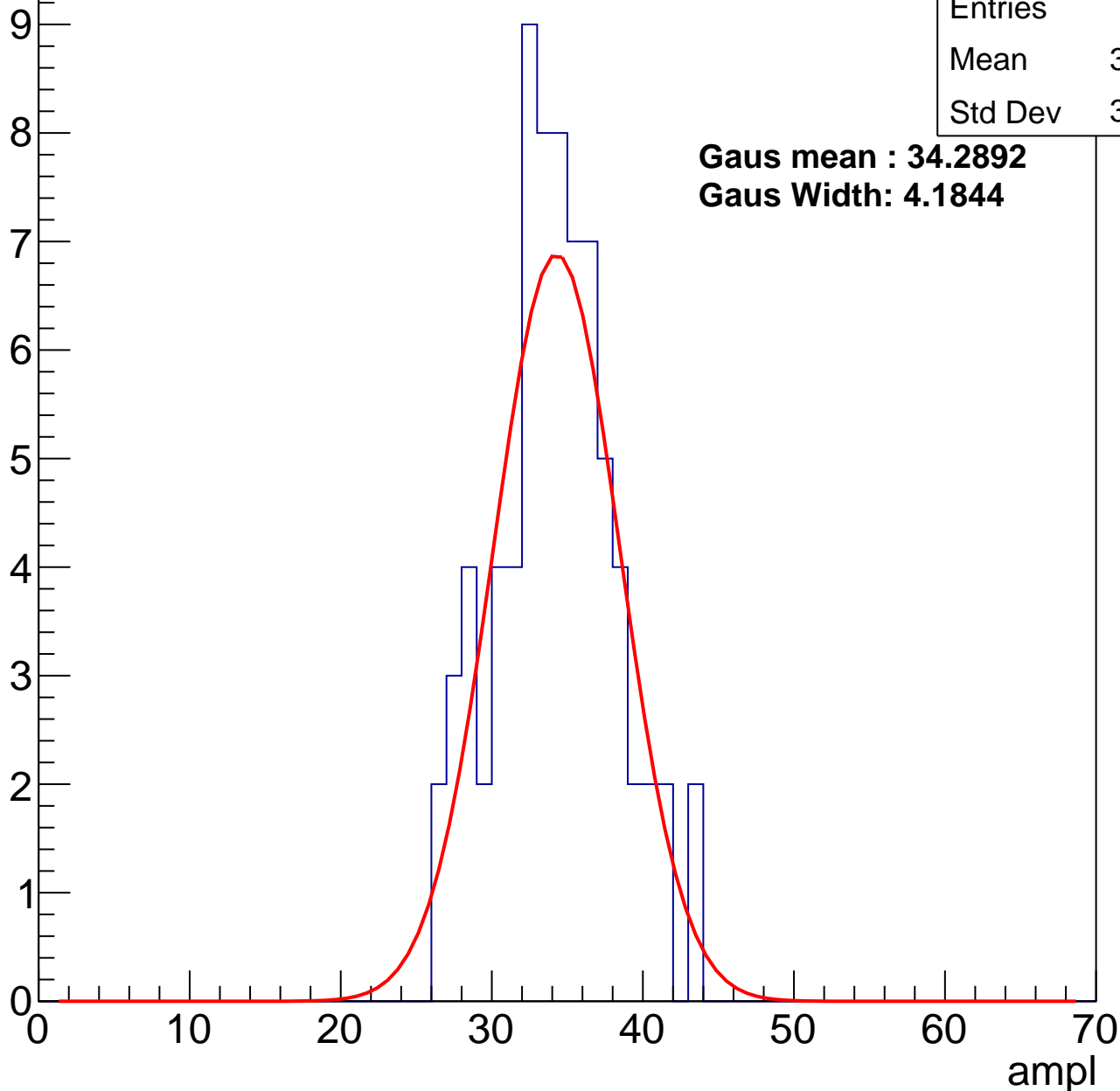
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	33.75
Std Dev	3.889

**Gaus mean : 34.2892**

**Gaus Width: 4.1844**



# B1L102S, U3-ch69, adc2

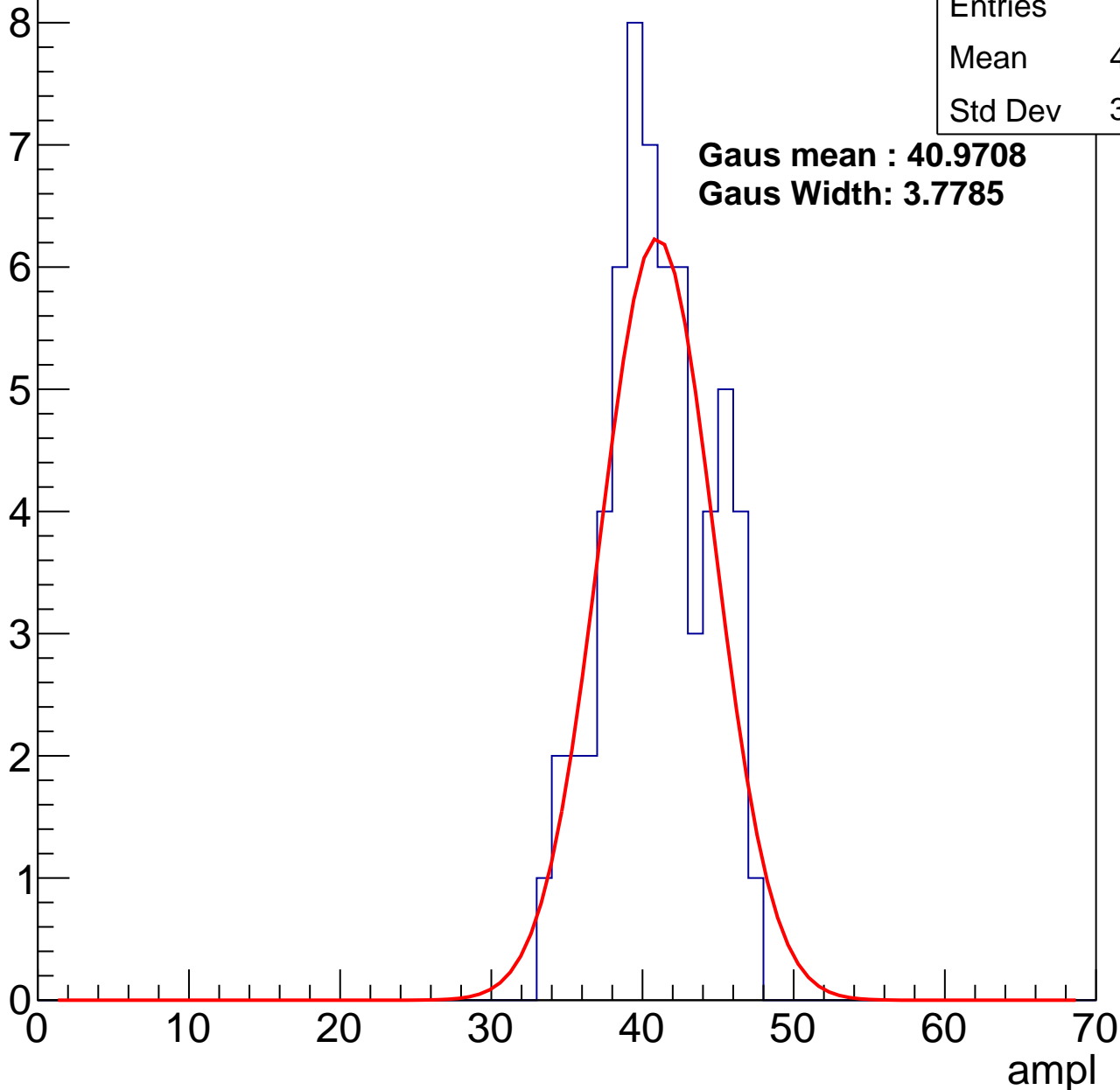
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	40.49
Std Dev	3.376

**Gaus mean : 40.9708**

**Gaus Width: 3.7785**

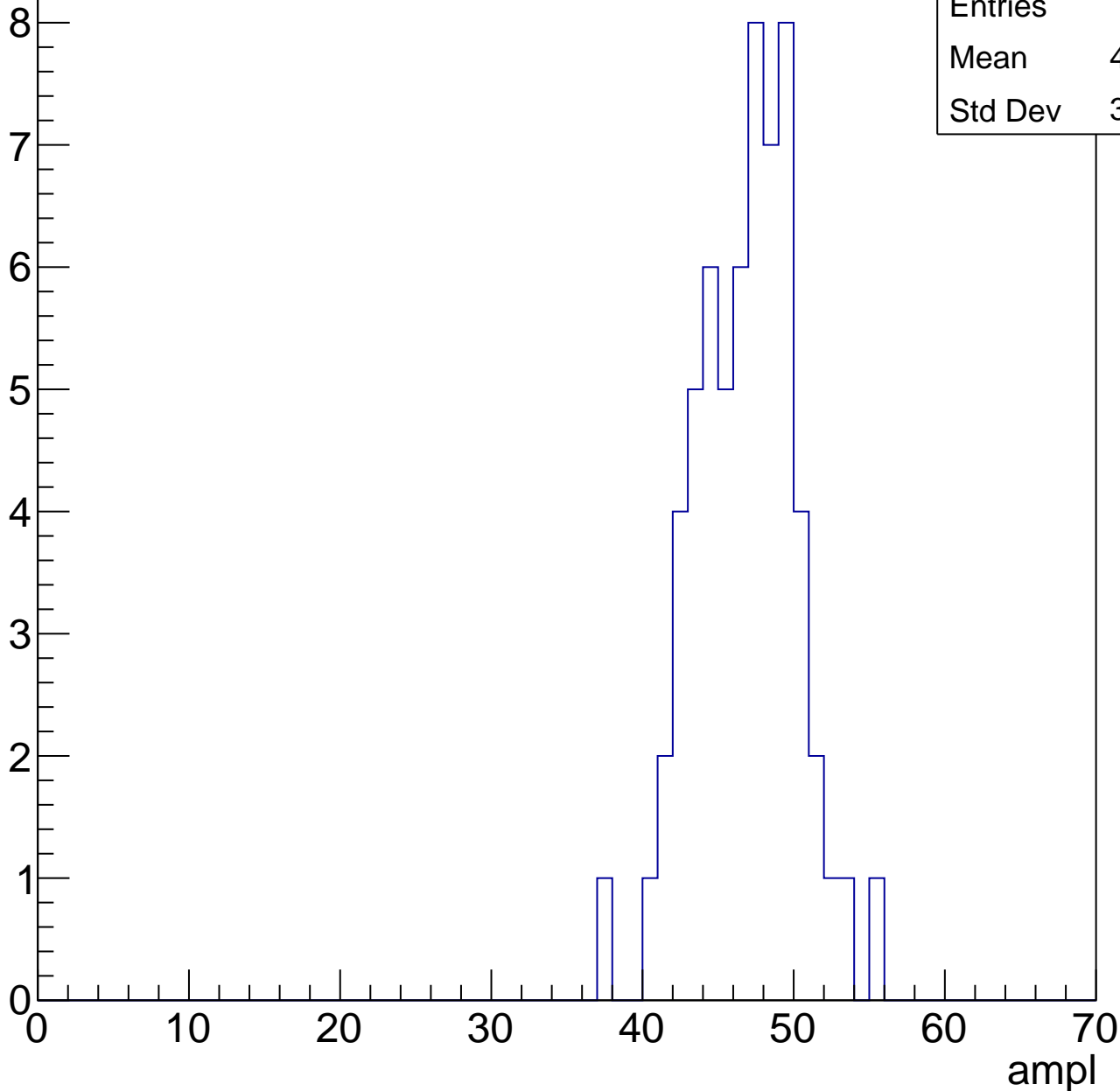


# B1L102S, U3-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	46.34
Std Dev	3.326

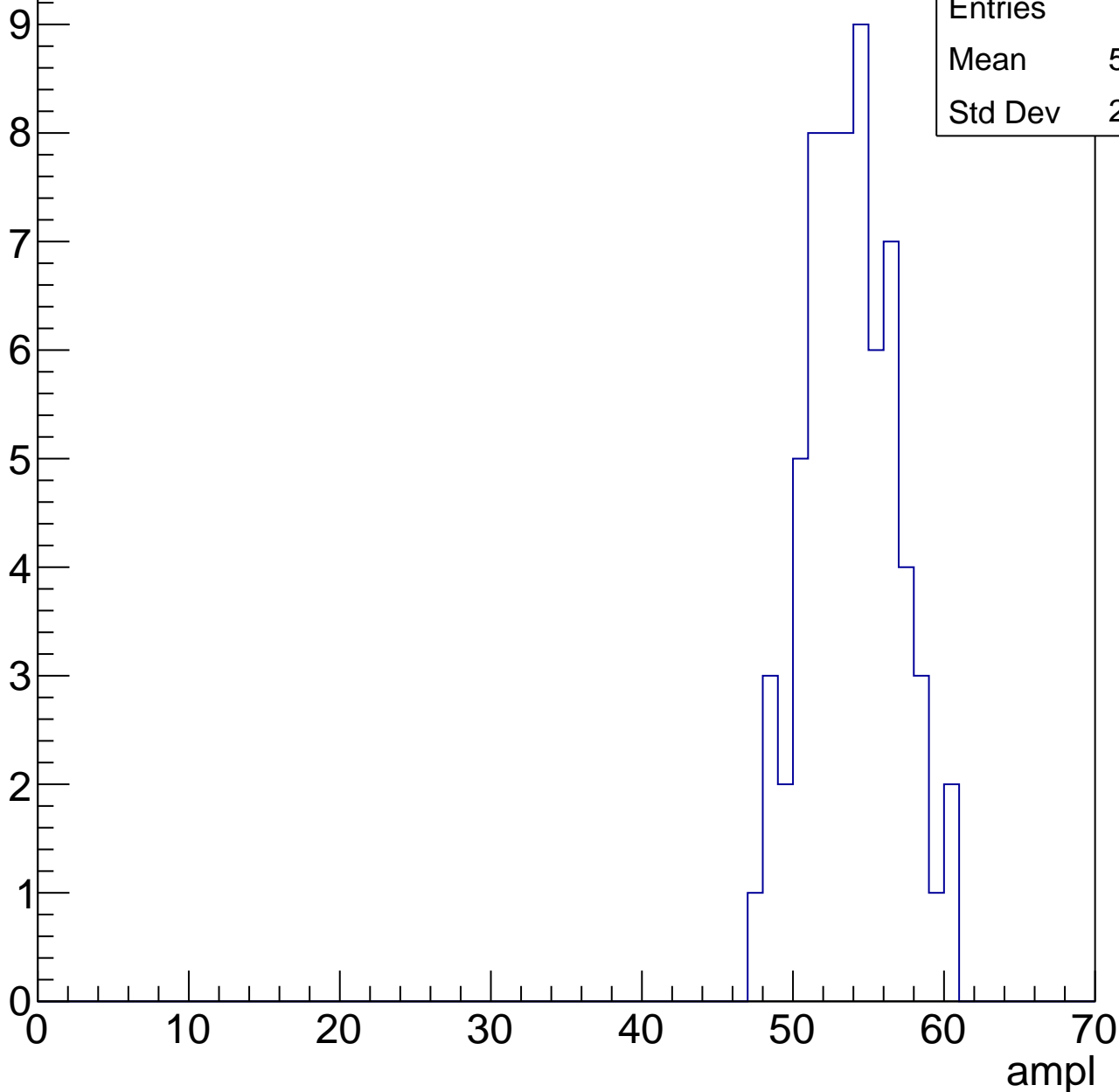


# B1L102S, U3-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	53.37
Std Dev	2.962

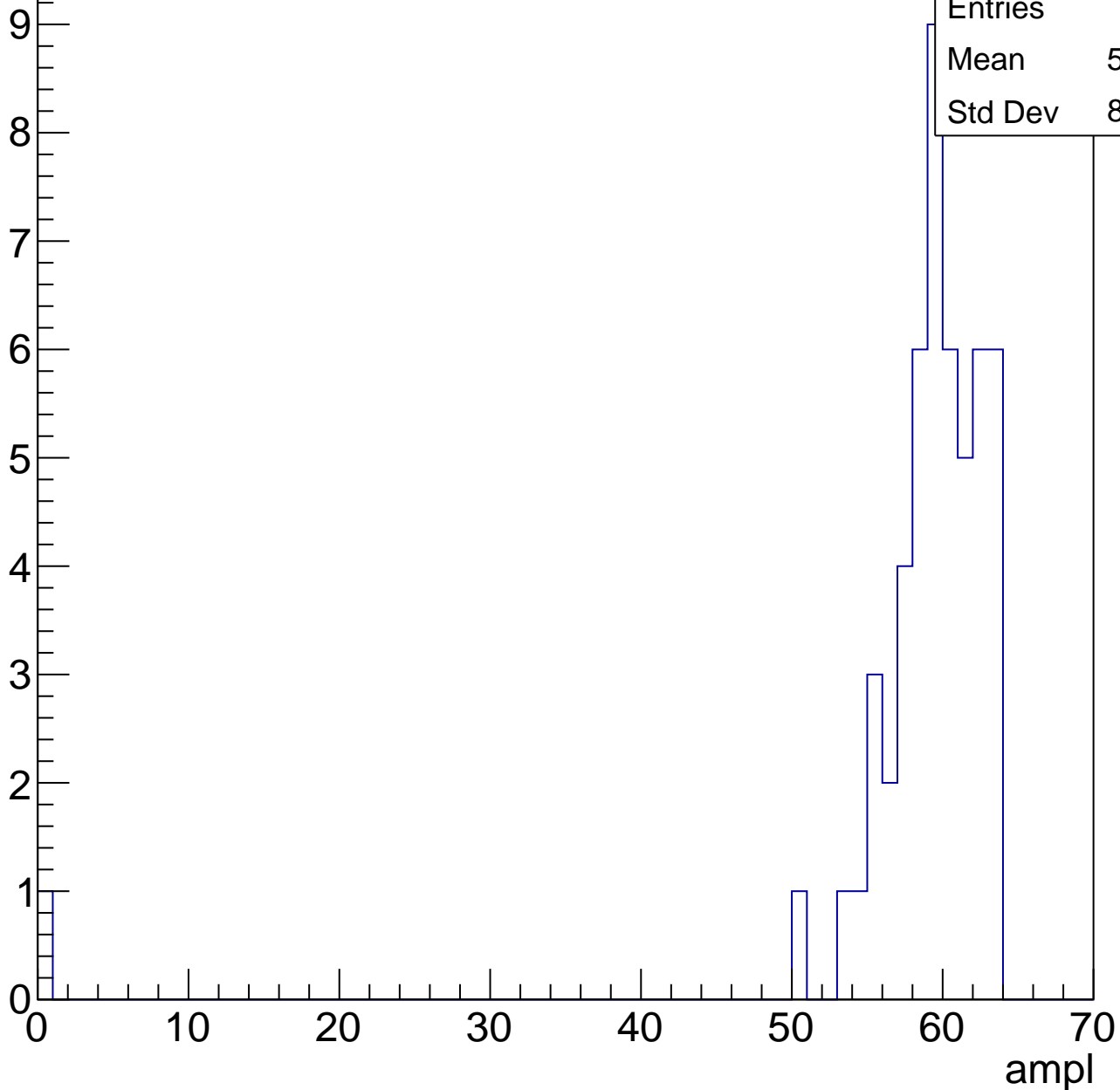


# B1L102S, U3-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	57.96
Std Dev	8.668

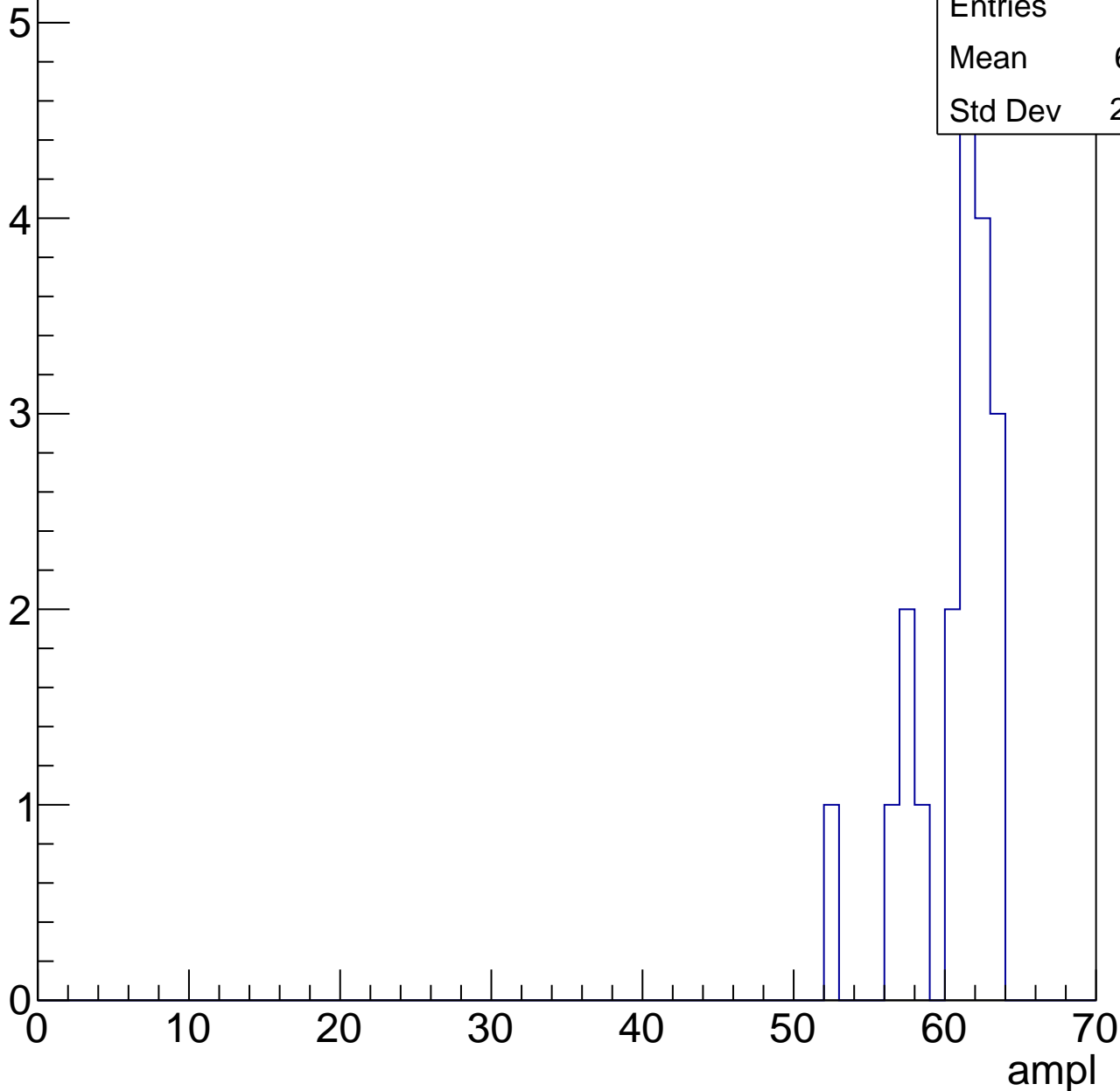


# B1L102S, U3-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	19
Mean	60.11
Std Dev	2.808





# B1L102S, U3-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch70, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	83
Mean	27.12
Std Dev	4.963

**Gaus mean : 28.3159**

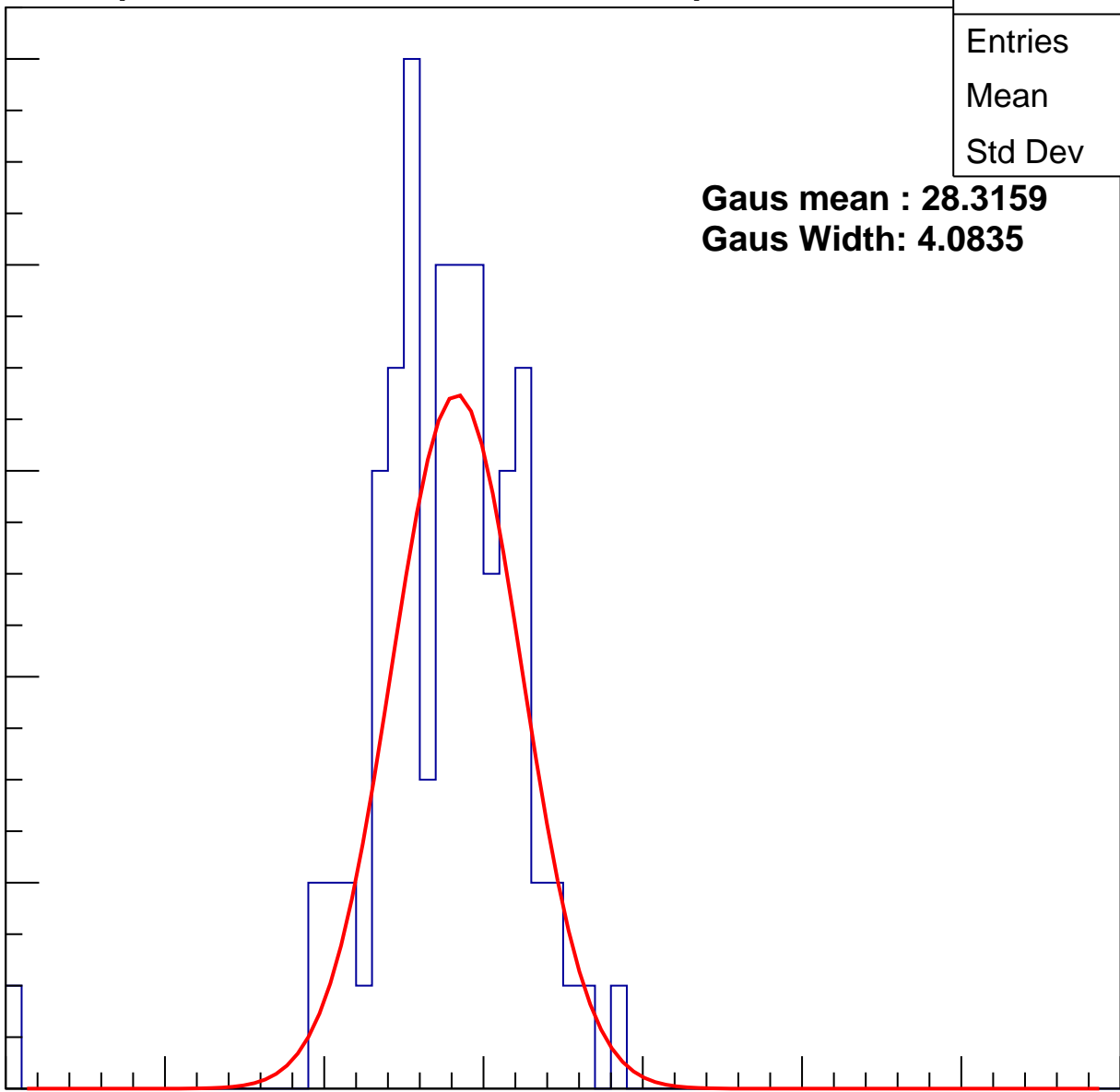
**Gaus Width: 4.0835**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U3-ch70, adc1

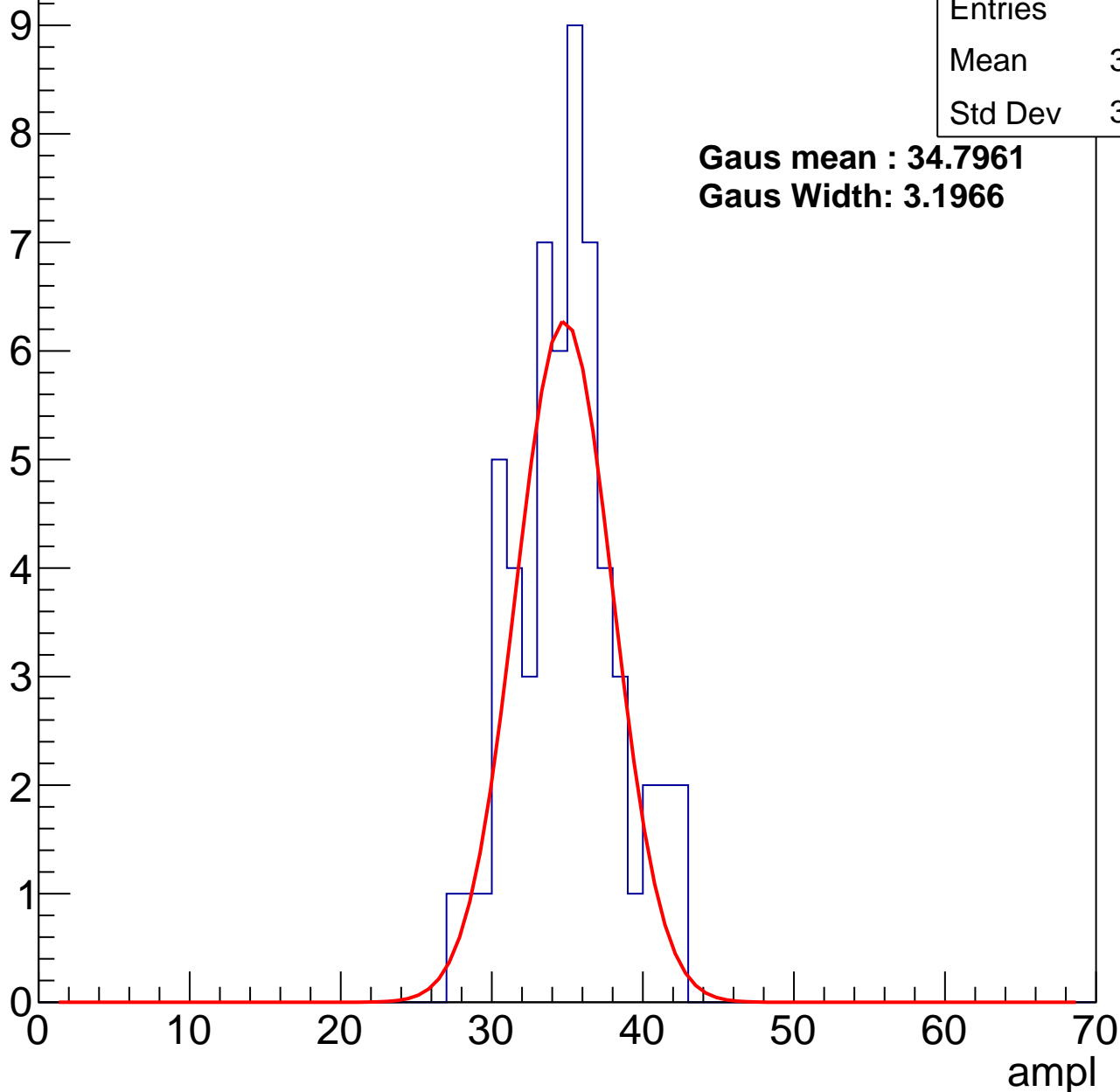
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	34.53
Std Dev	3.405

**Gaus mean : 34.7961**

**Gaus Width: 3.1966**



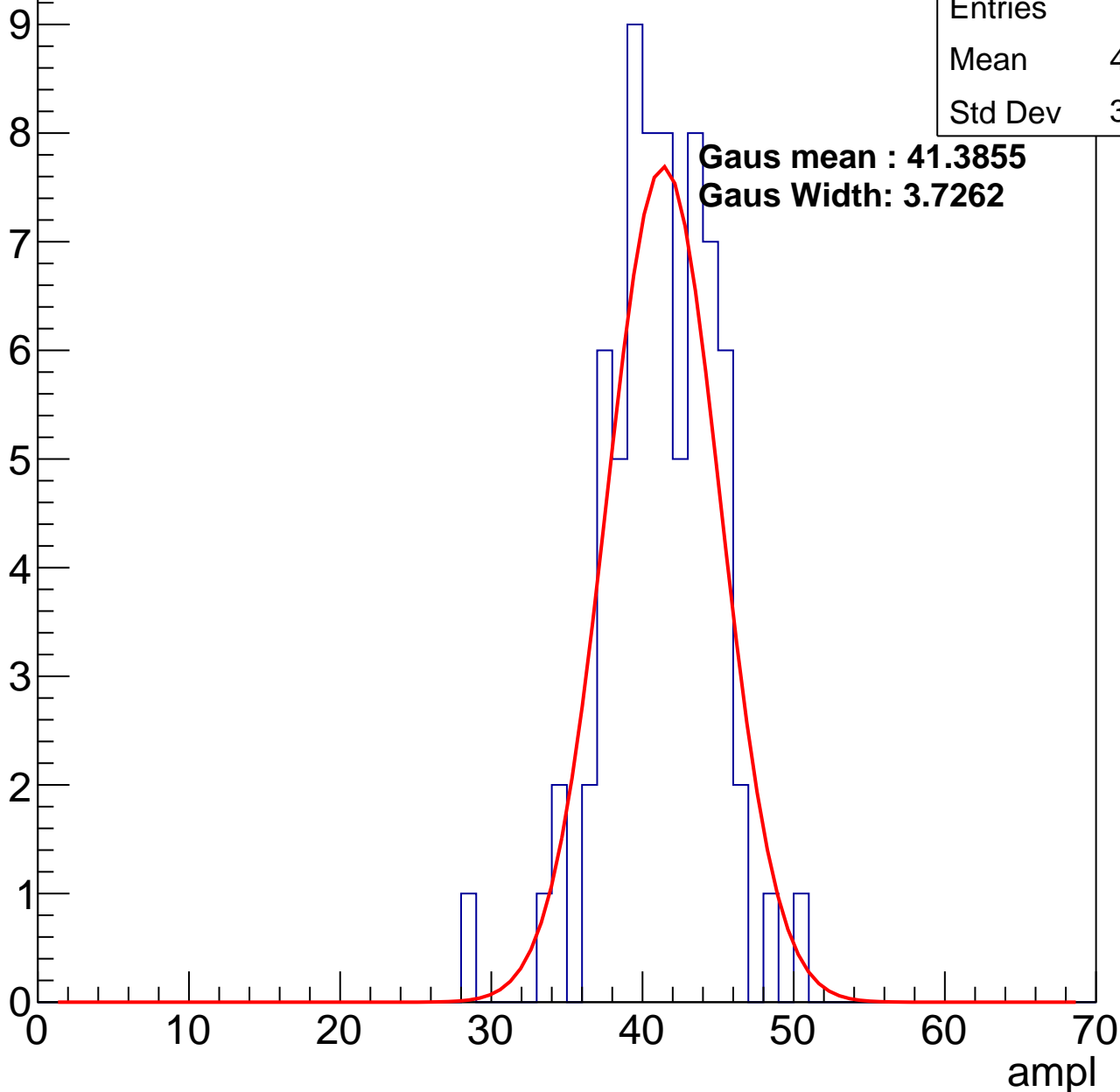
# B1L102S, U3-ch70, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	40.75
Std Dev	3.608

**Gaus mean : 41.3855**  
**Gaus Width: 3.7262**

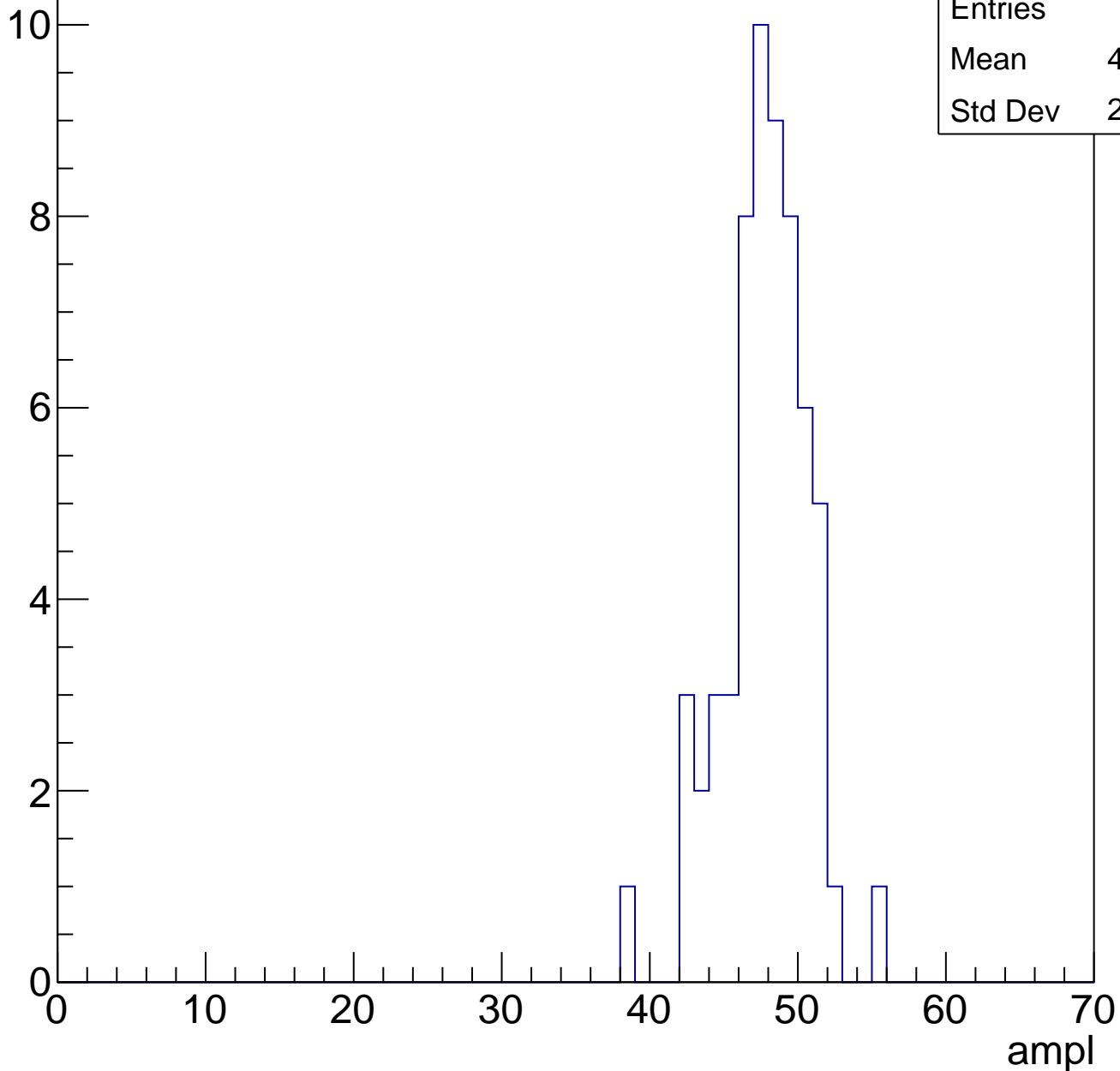


# B1L102S, U3-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	60
Mean	47.35
Std Dev	2.863

Entry

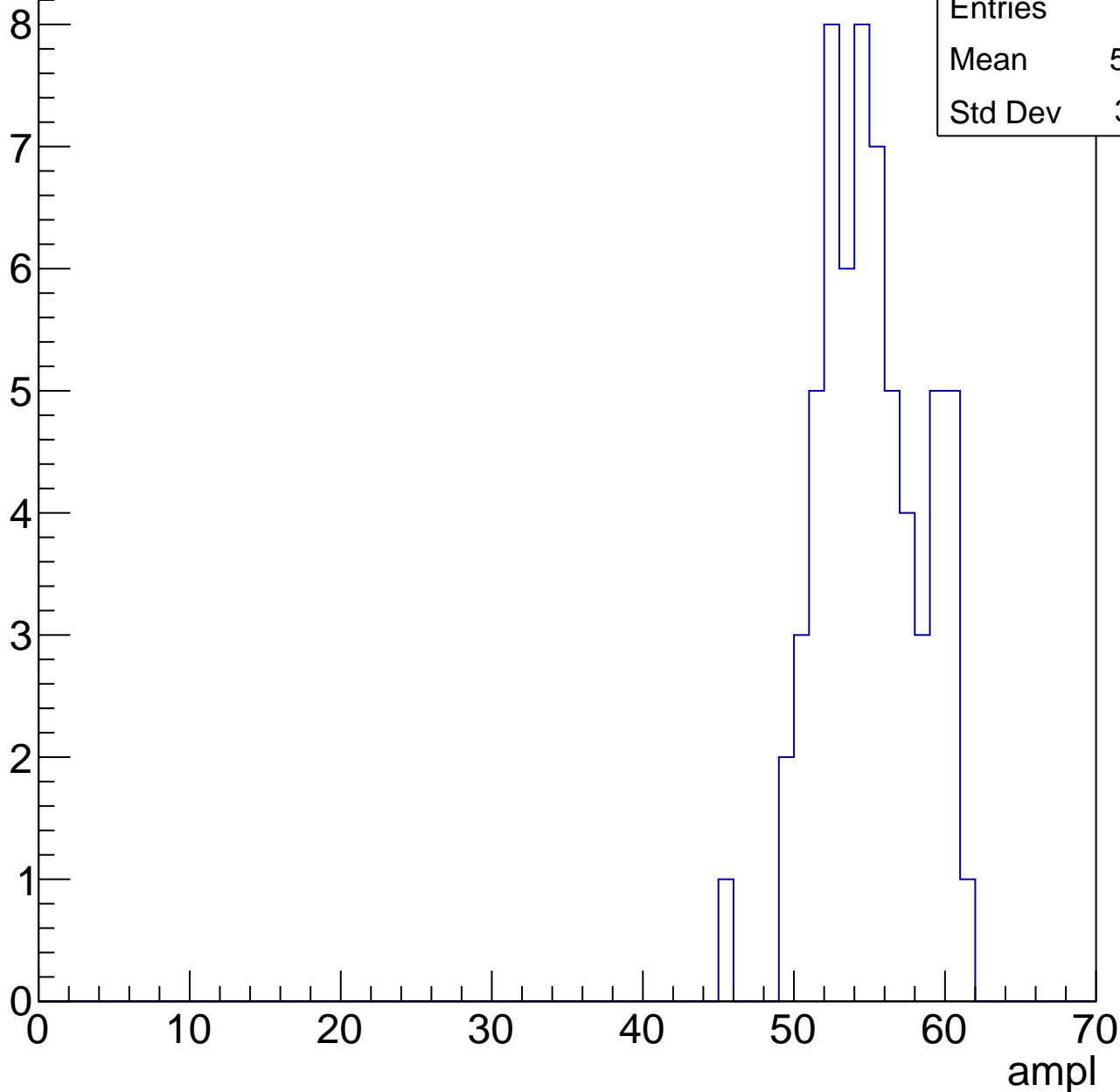


# B1L102S, U3-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	54.56
Std Dev	3.351

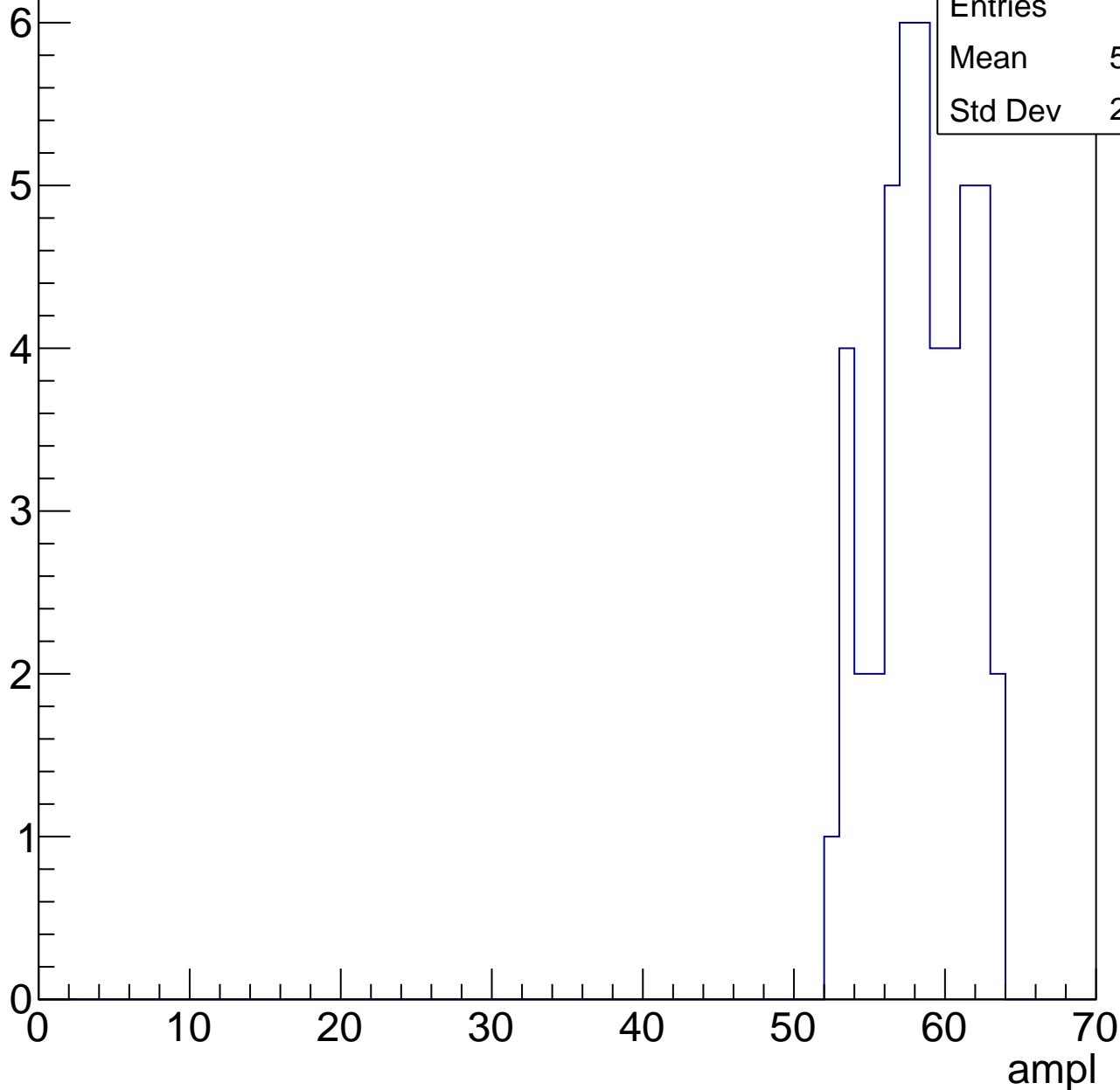


# B1L102S, U3-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	58.02
Std Dev	2.974

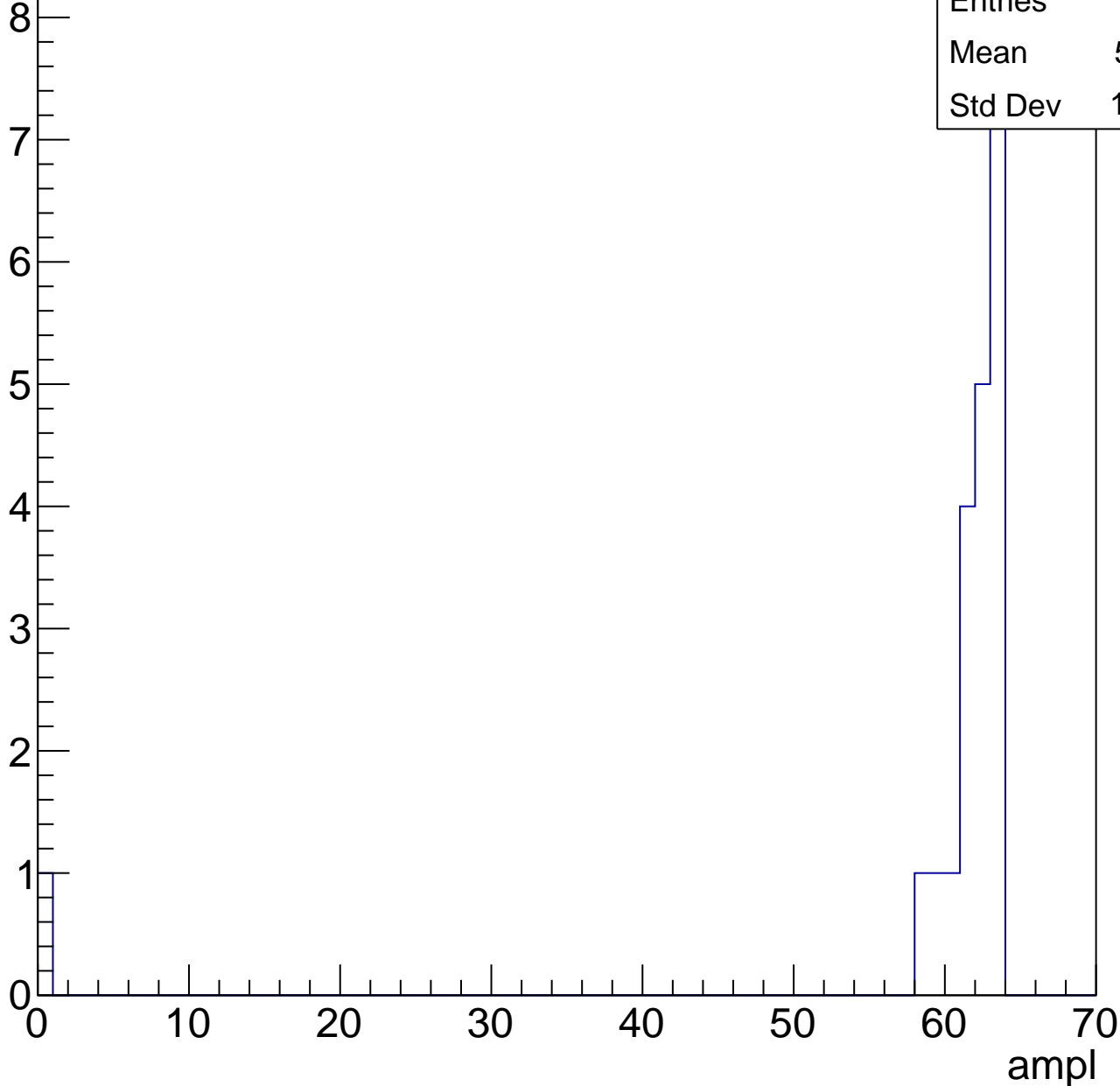


# B1L102S, U3-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	21
Mean	58.81
Std Dev	13.22





# B1L102S, U3-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U3-ch71, adc0

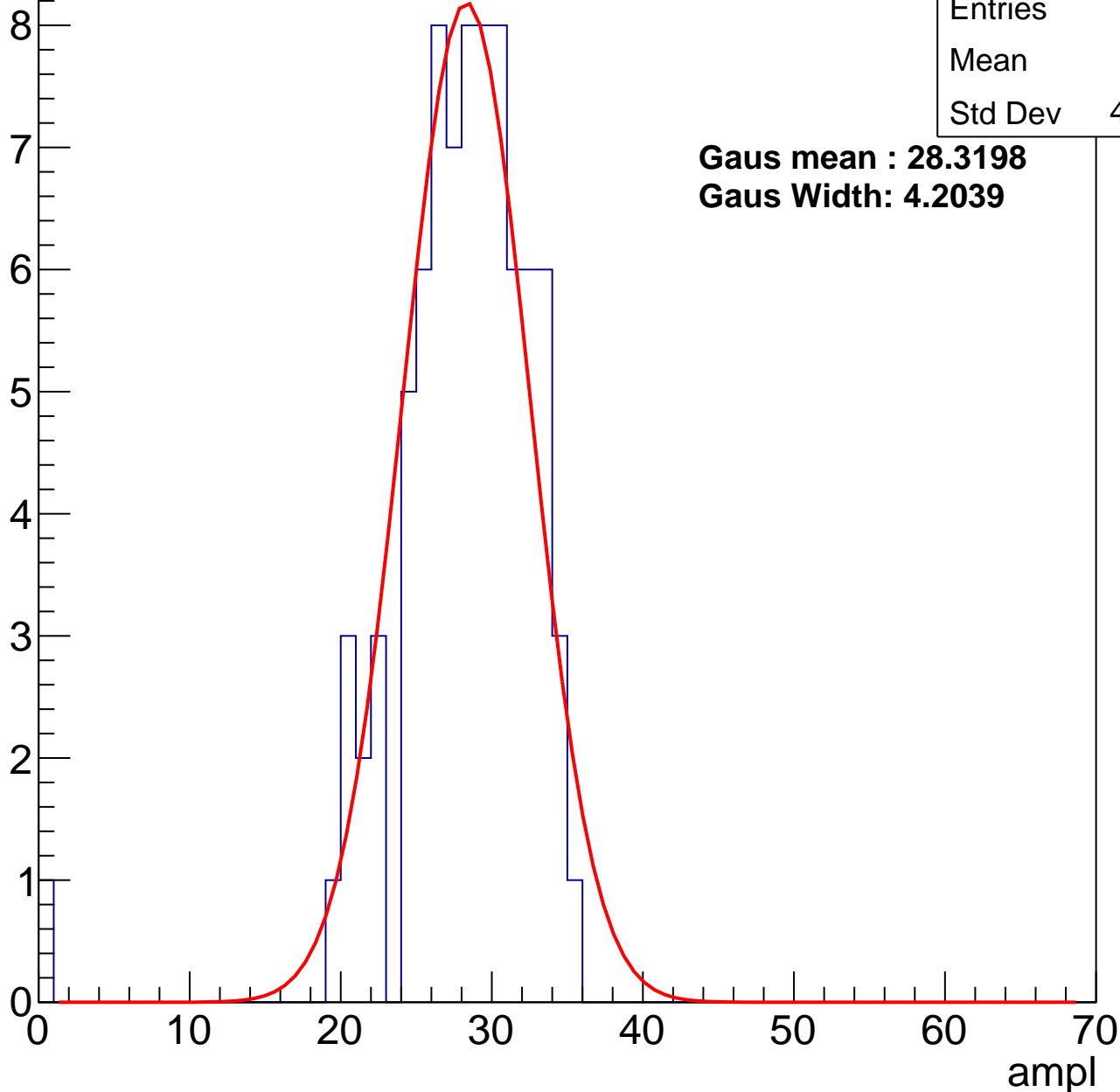
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	27.6
Std Dev	4.839

**Gaus mean : 28.3198**

**Gaus Width: 4.2039**



# B1L102S, U3-ch71, adc1

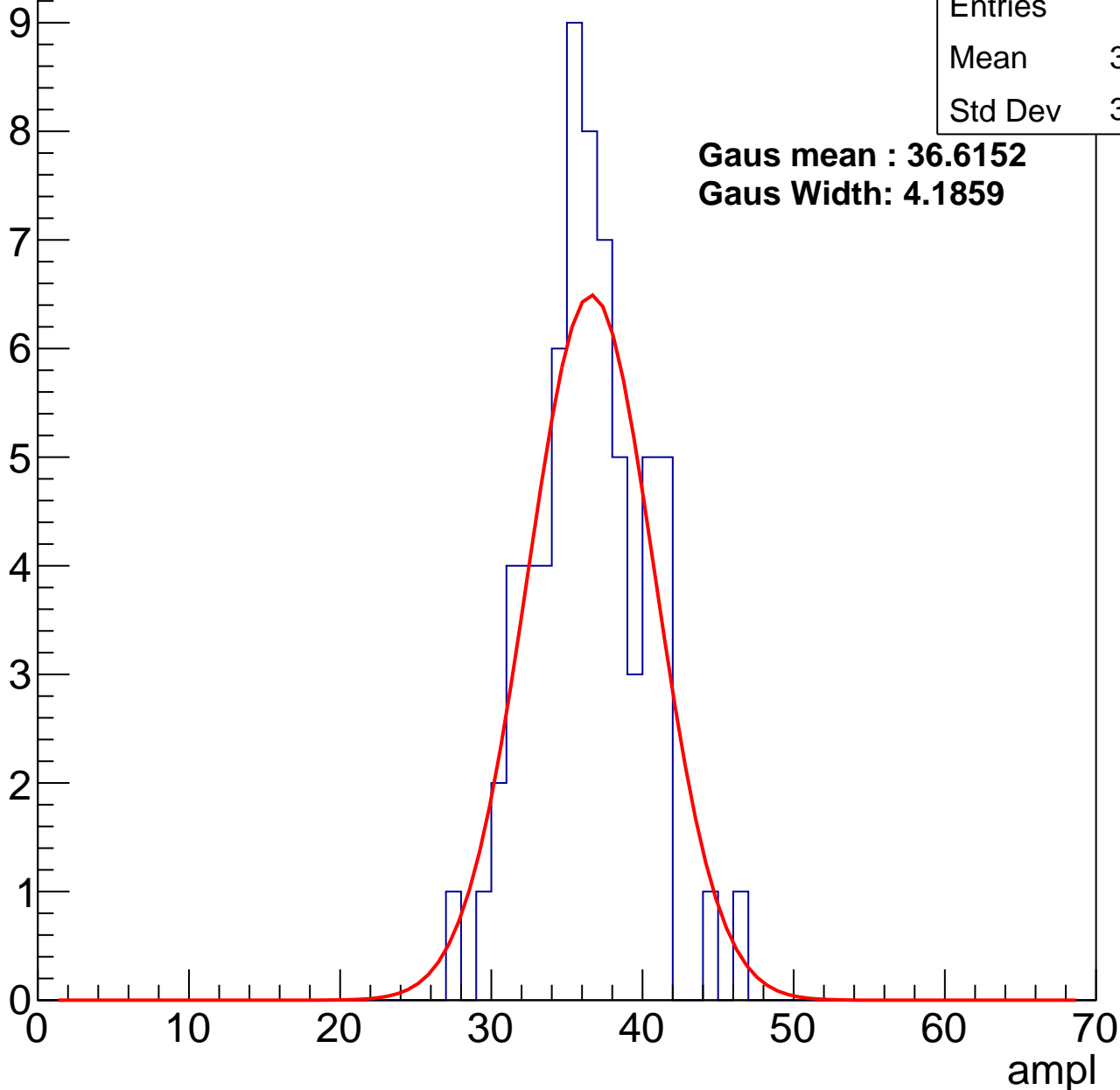
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	35.88
Std Dev	3.604

**Gaus mean : 36.6152**

**Gaus Width: 4.1859**



# B1L102S, U3-ch71, adc2

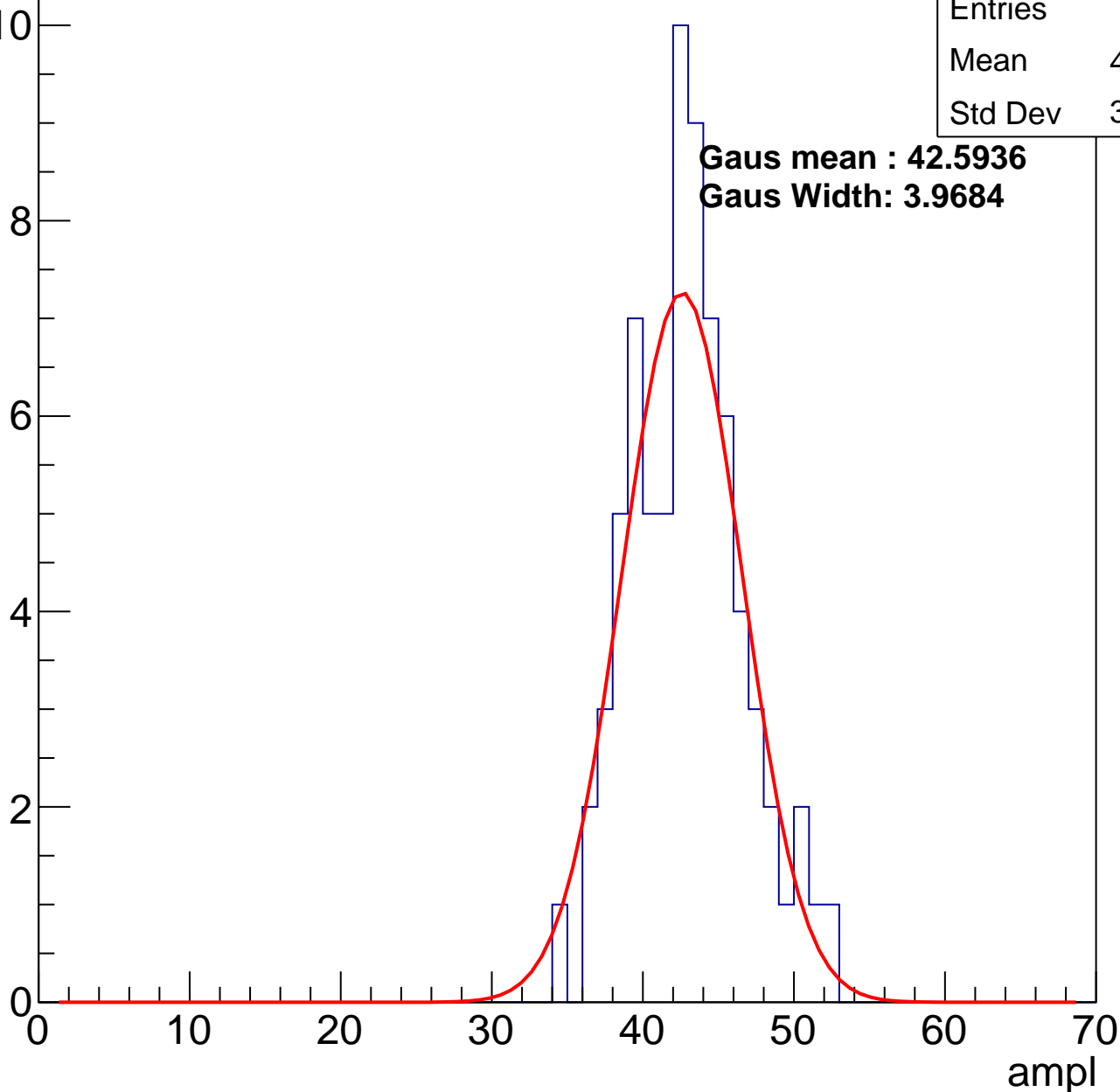
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	42.47
Std Dev	3.717

**Gaus mean : 42.5936**

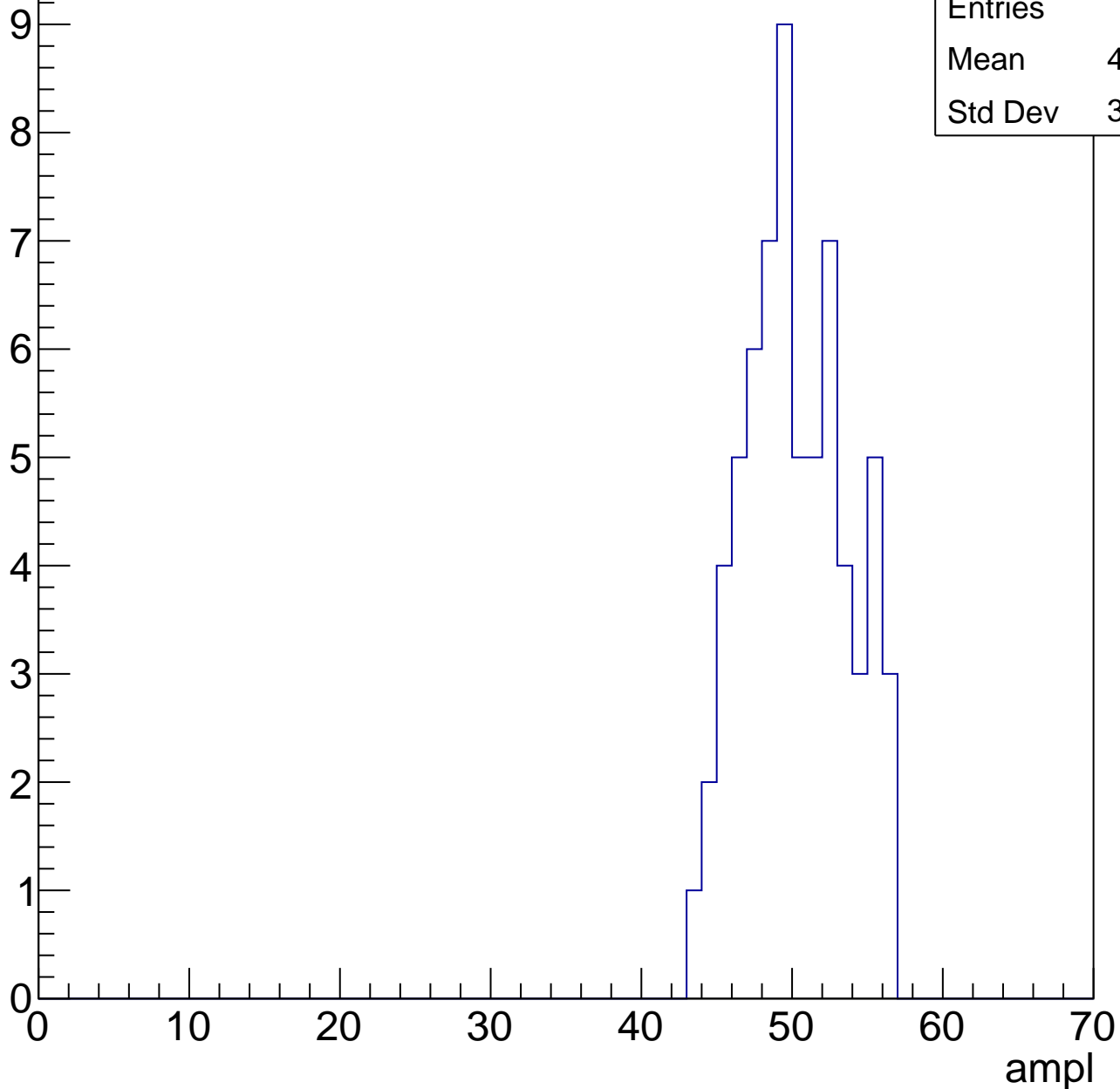
**Gaus Width: 3.9684**



# B1L102S, U3-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

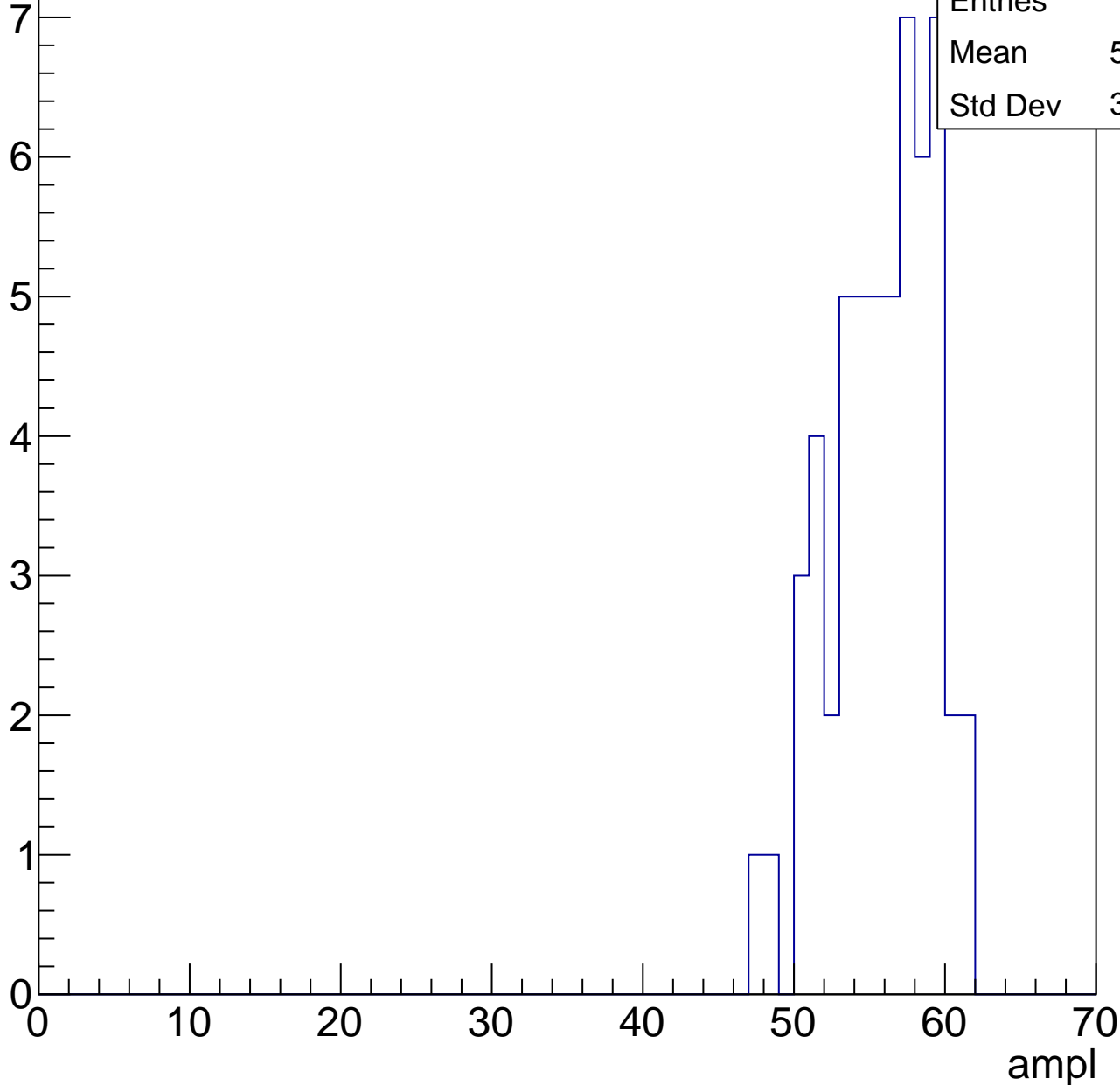


Entries	66
Mean	49.79
Std Dev	3.346

# B1L102S, U3-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch71, adc5

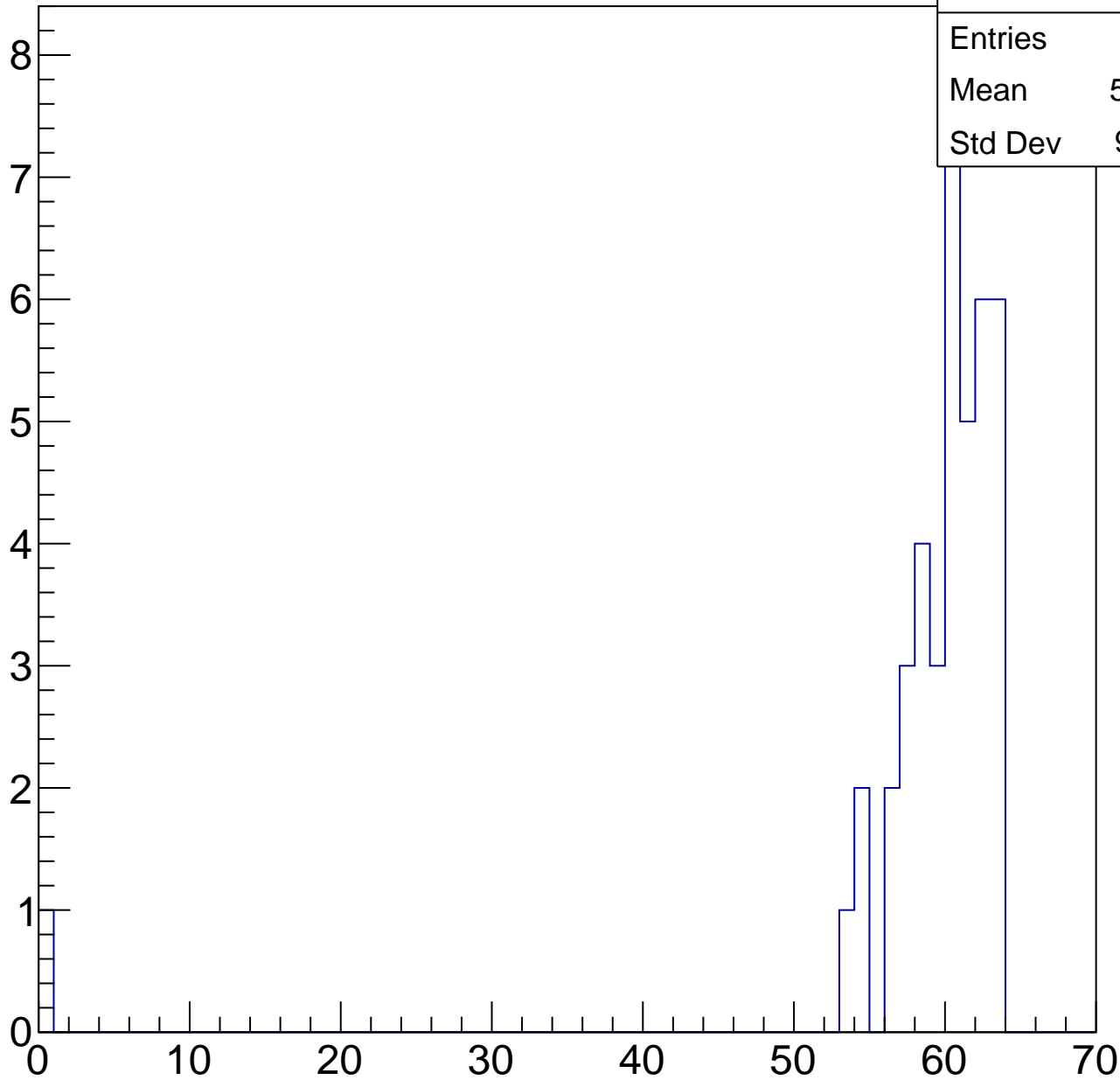
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	41
Mean	58.24
Std Dev	9.571

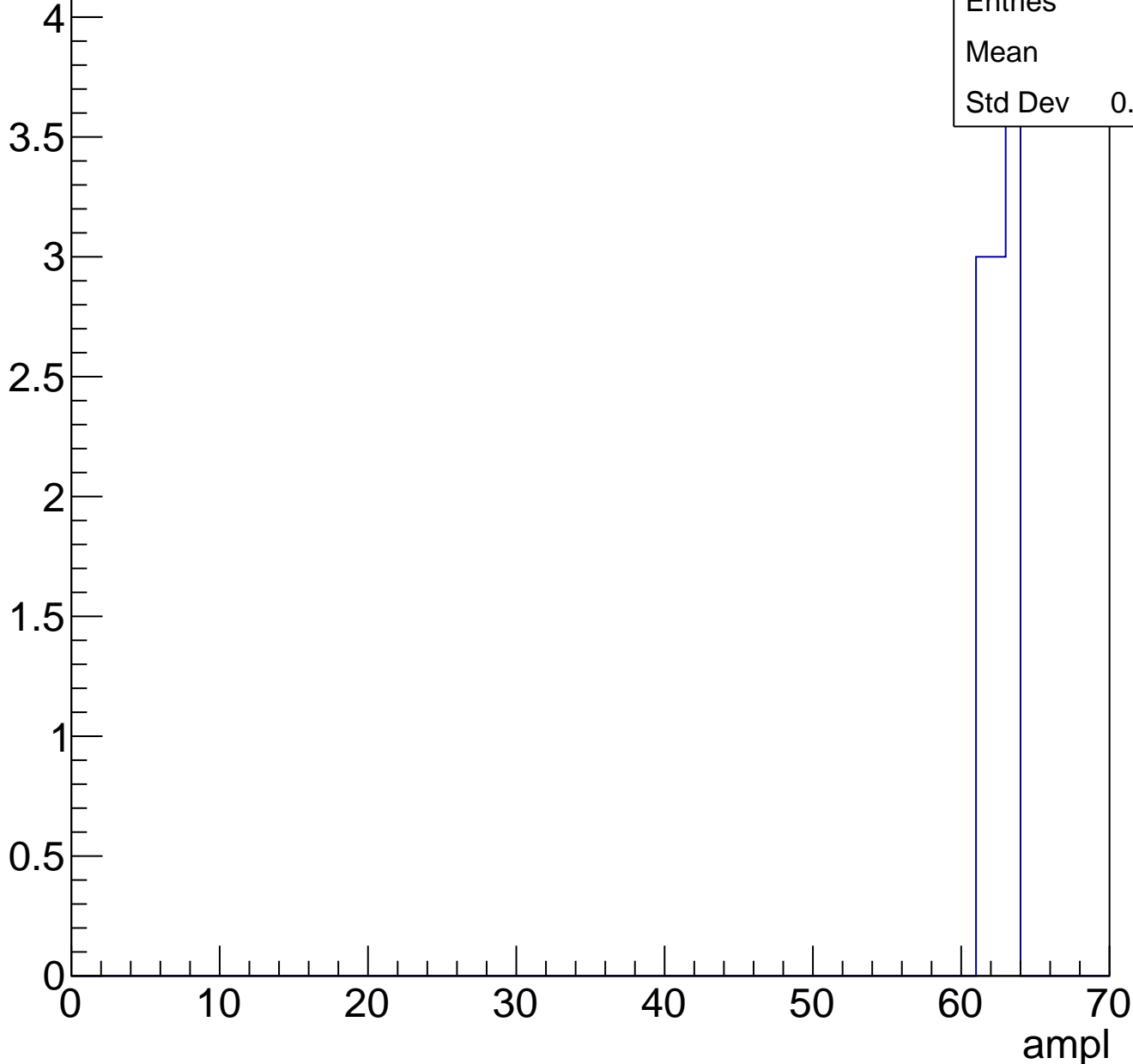
ampl



# B1L102S, U3-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch72, adc0

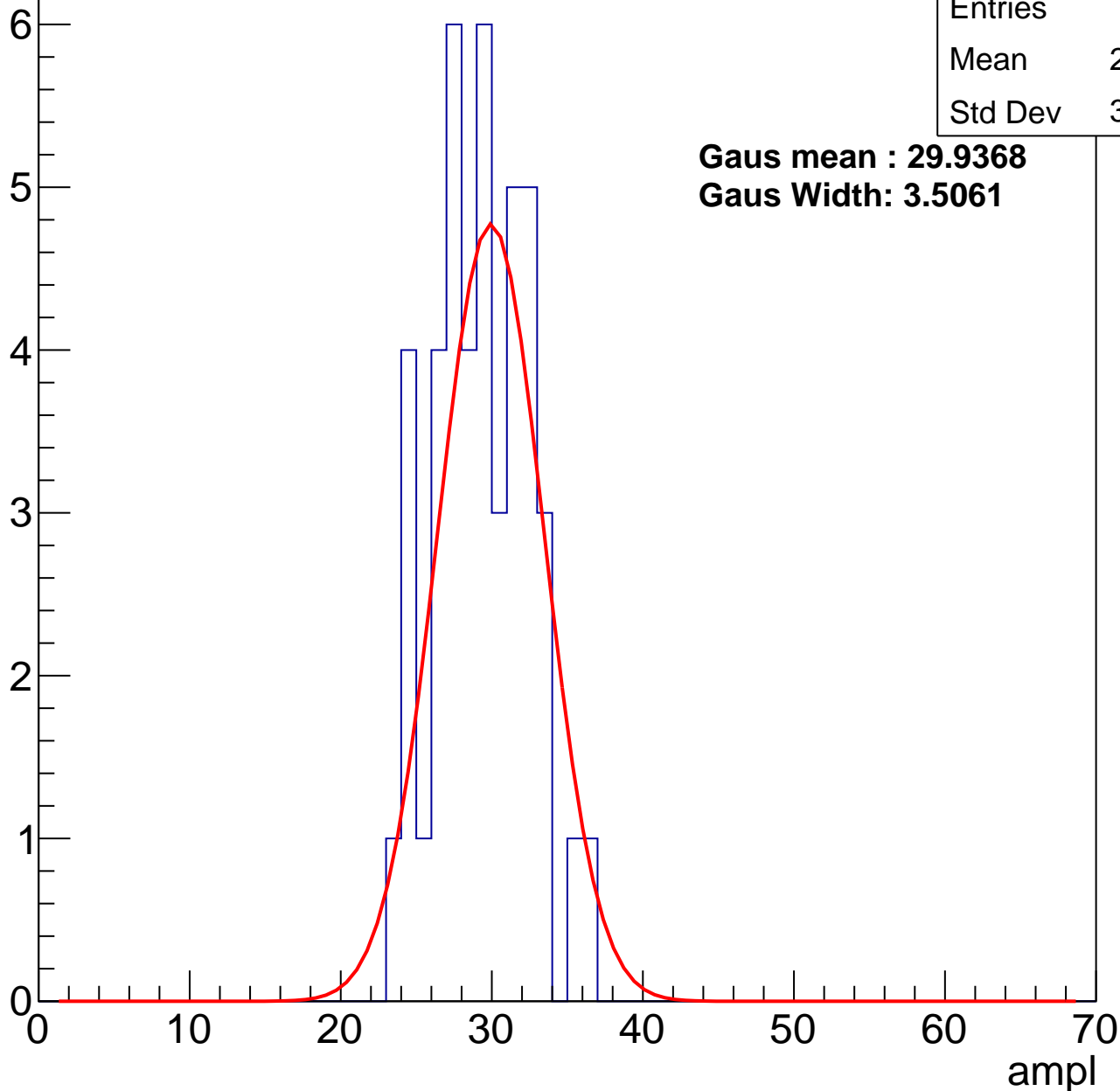
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	44
Mean	28.89
Std Dev	3.076

**Gaus mean : 29.9368**

**Gaus Width: 3.5061**



# B1L102S, U3-ch72, adc1

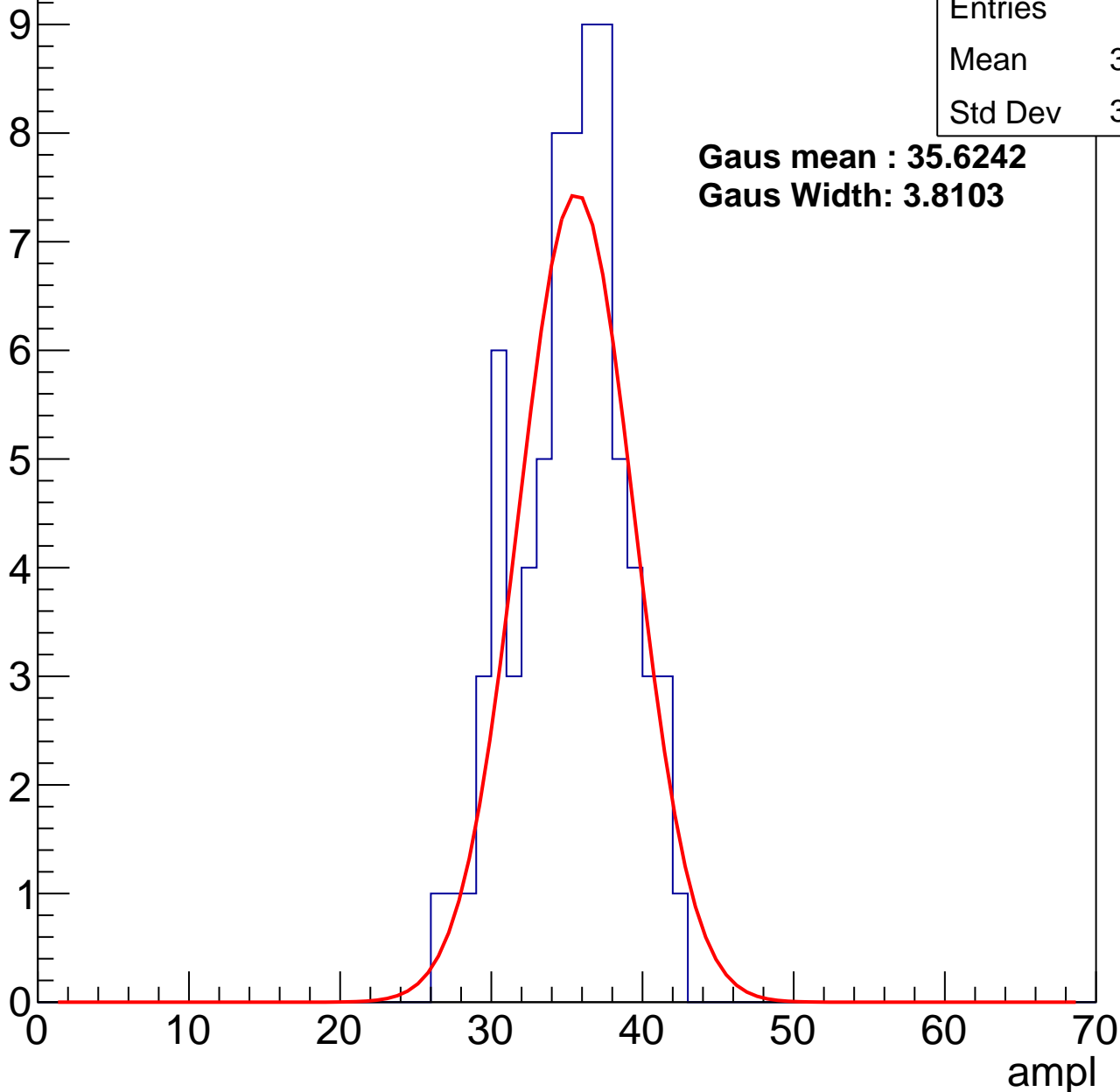
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	34.78
Std Dev	3.576

**Gaus mean : 35.6242**

**Gaus Width: 3.8103**



# B1L102S, U3-ch72, adc2

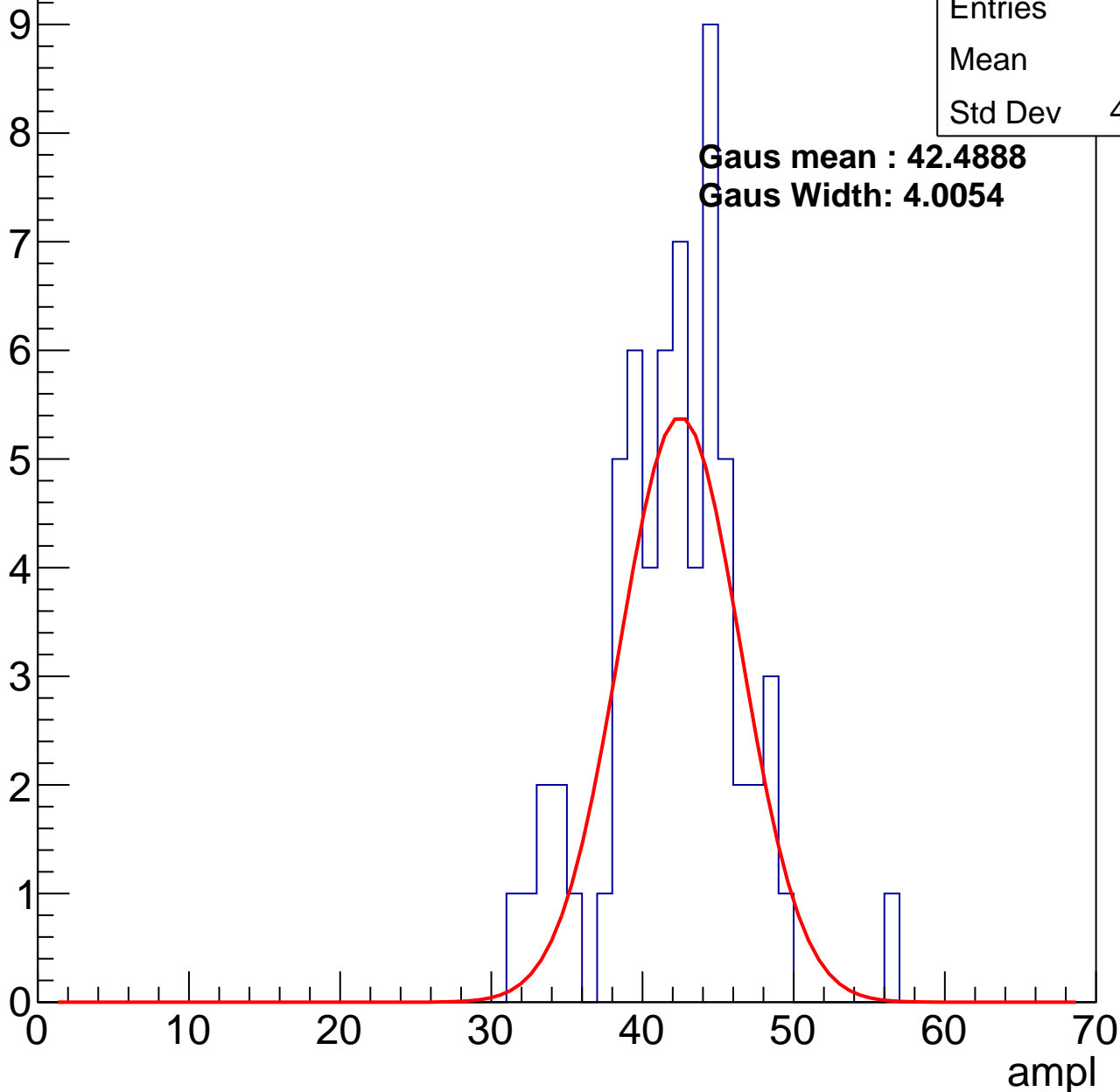
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	41.6
Std Dev	4.456

**Gaus mean : 42.4888**

**Gaus Width: 4.0054**

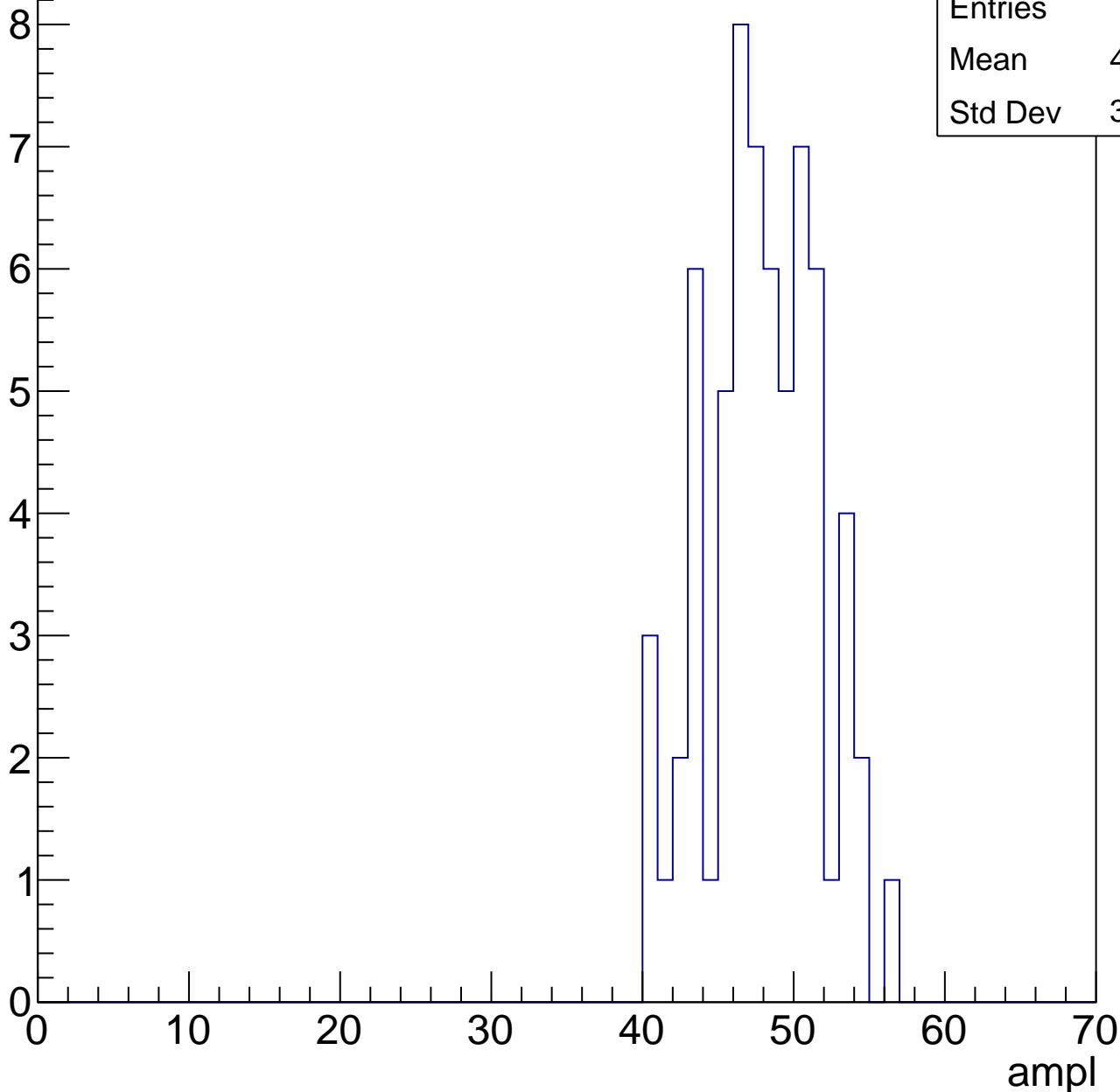


# B1L102S, U3-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	47.48
Std Dev	3.688



# B1L102S, U3-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	59
Mean	53.81
Std Dev	2.914

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

7

8

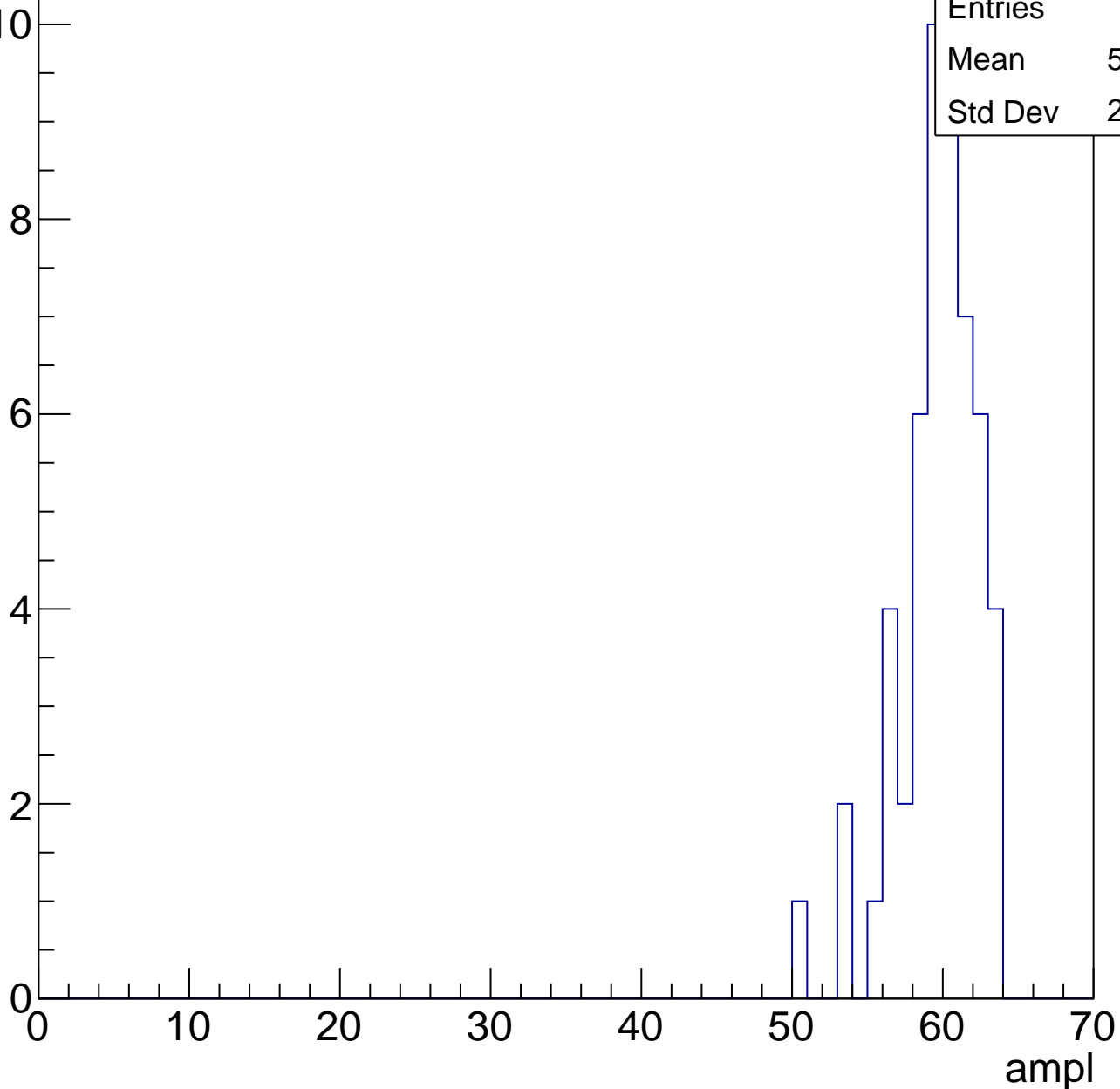
9

# B1L102S, U3-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	59.19
Std Dev	2.675

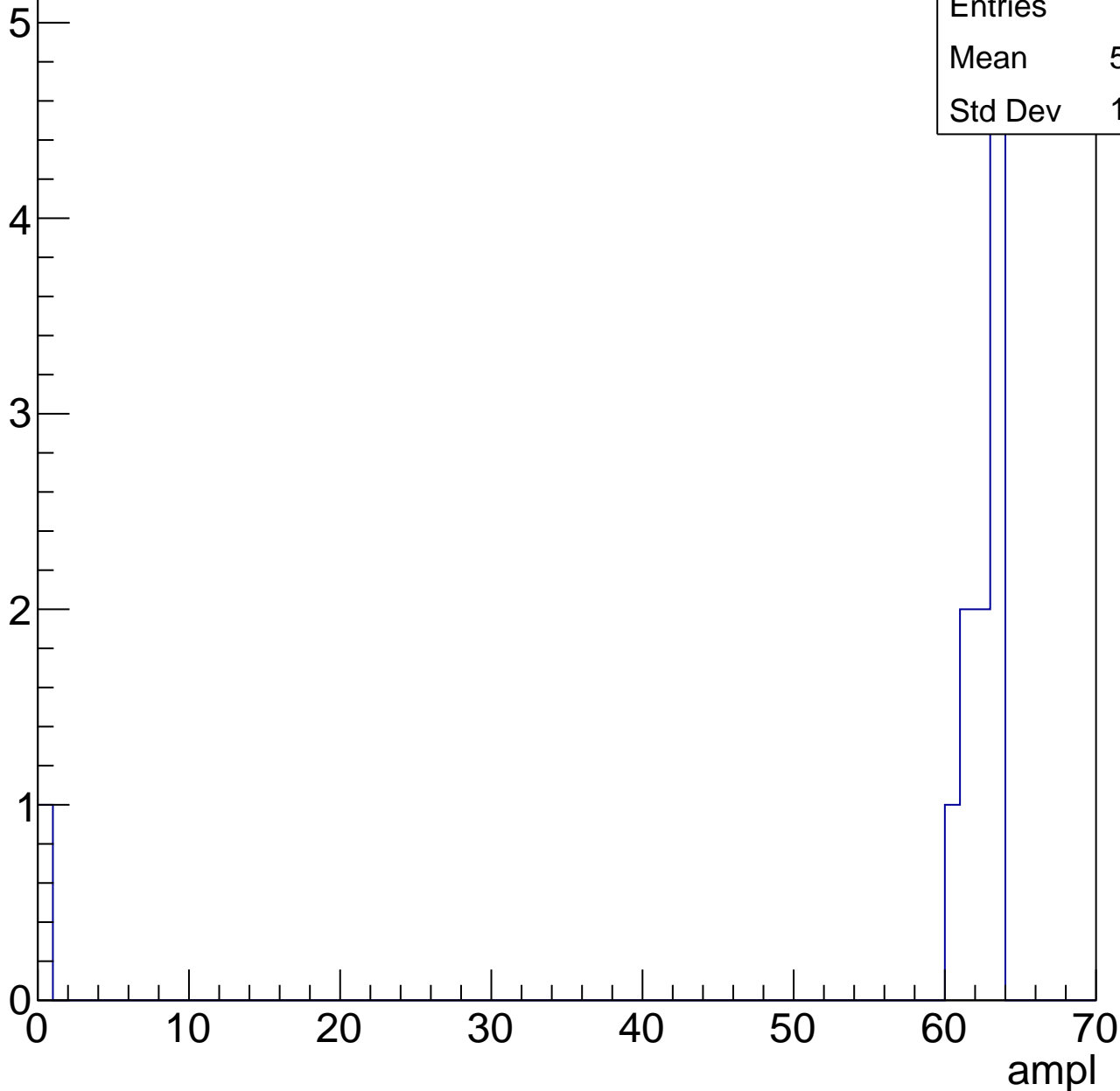


# B1L102S, U3-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	11
Mean	56.45
Std Dev	17.88

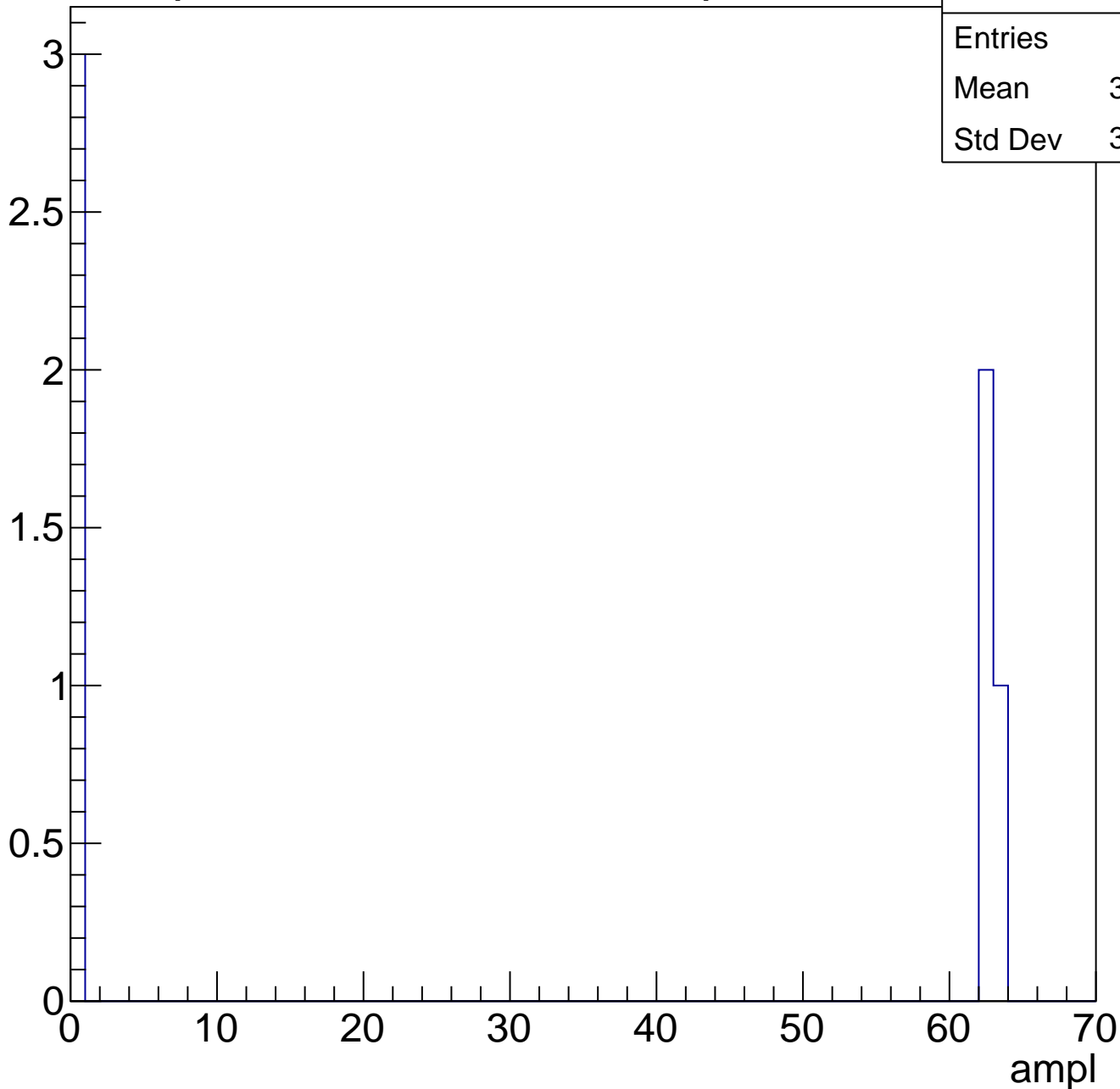




# B1L102S, U3-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	6
Mean	31.17
Std Dev	31.17

# B1L102S, U3-ch73, adc0

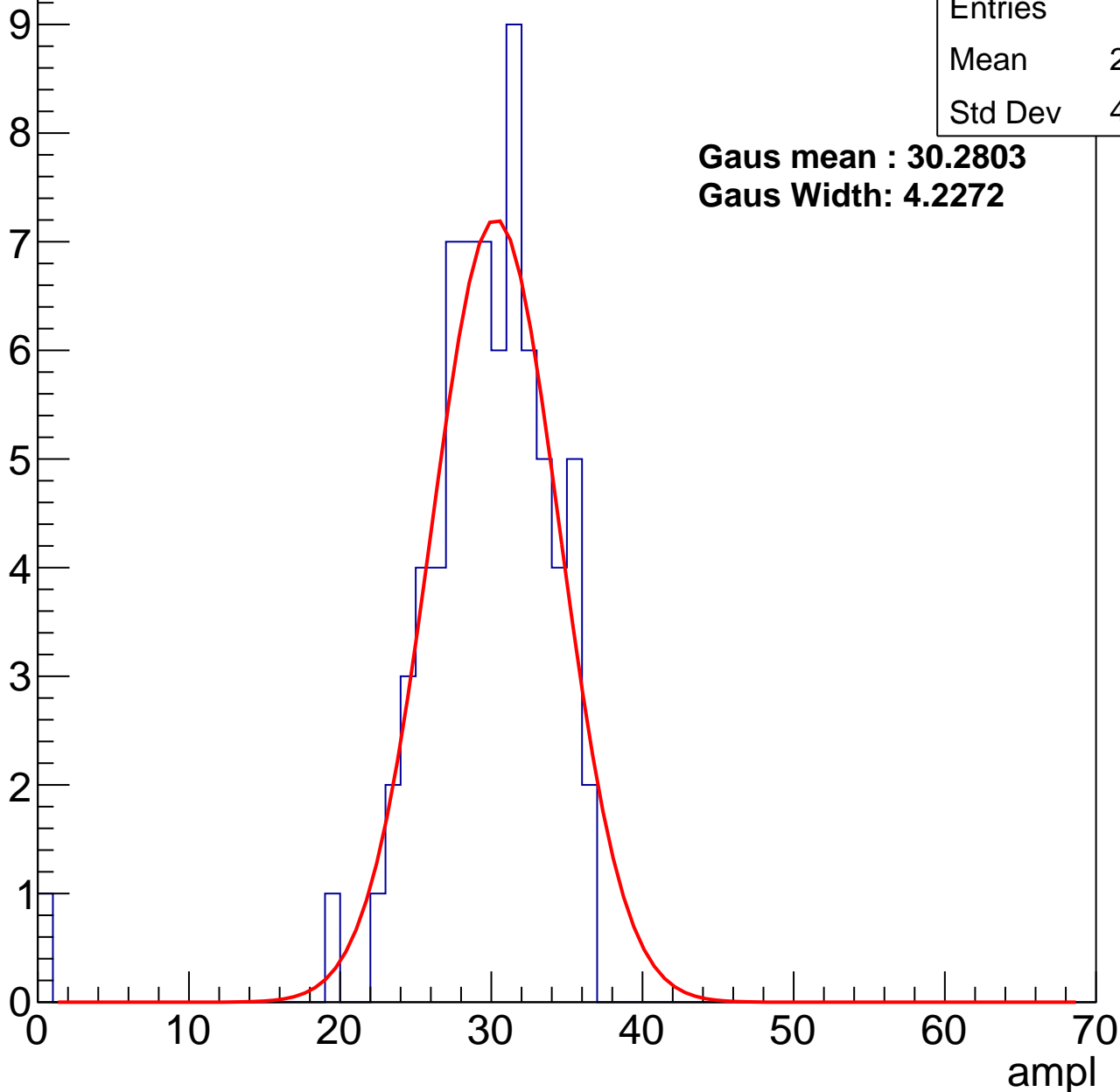
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	29.05
Std Dev	4.967

**Gaus mean : 30.2803**

**Gaus Width: 4.2272**



# B1L102S, U3-ch73, adc1

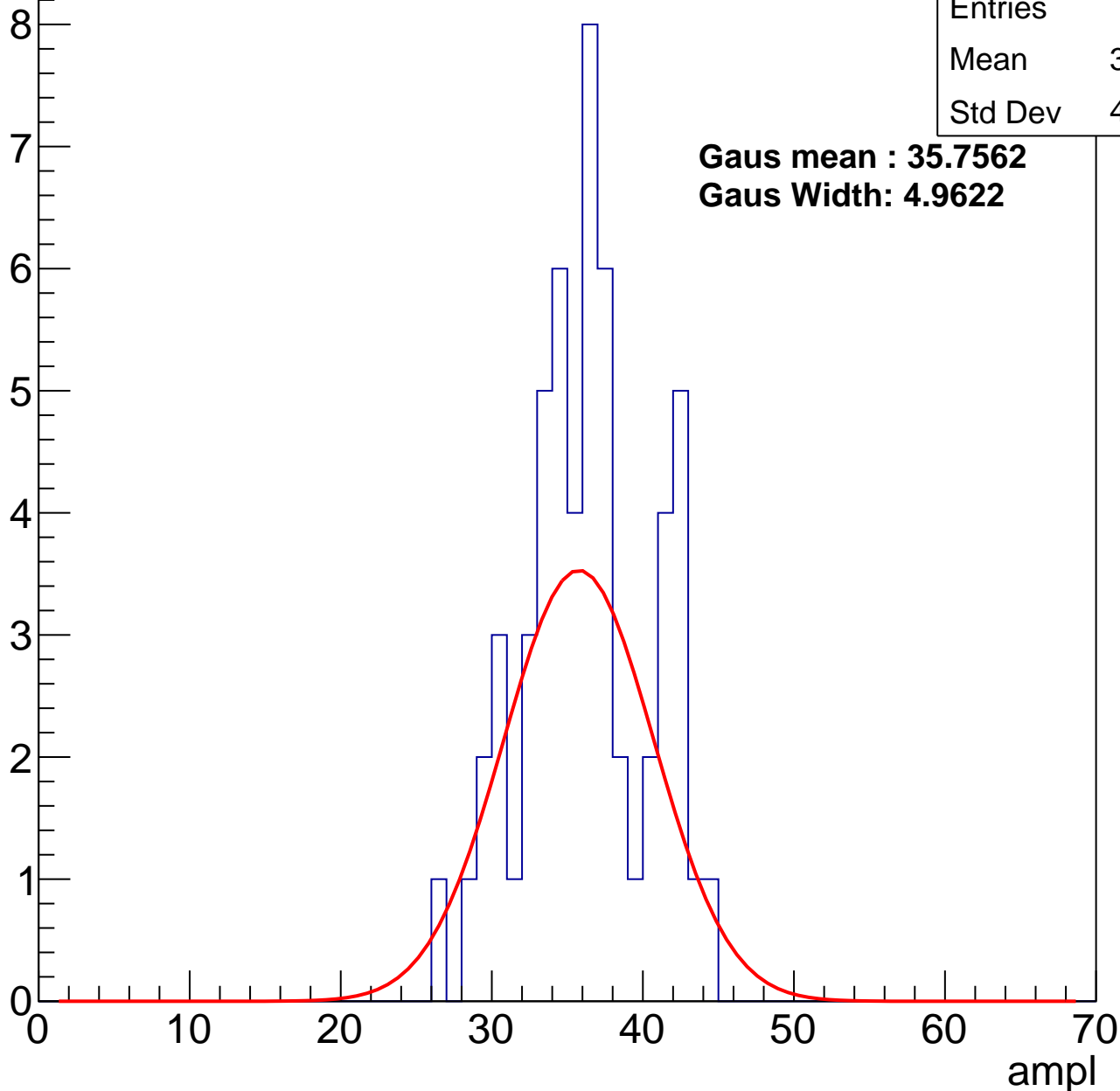
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	35.79
Std Dev	4.143

**Gaus mean : 35.7562**

**Gaus Width: 4.9622**



# B1L102S, U3-ch73, adc2

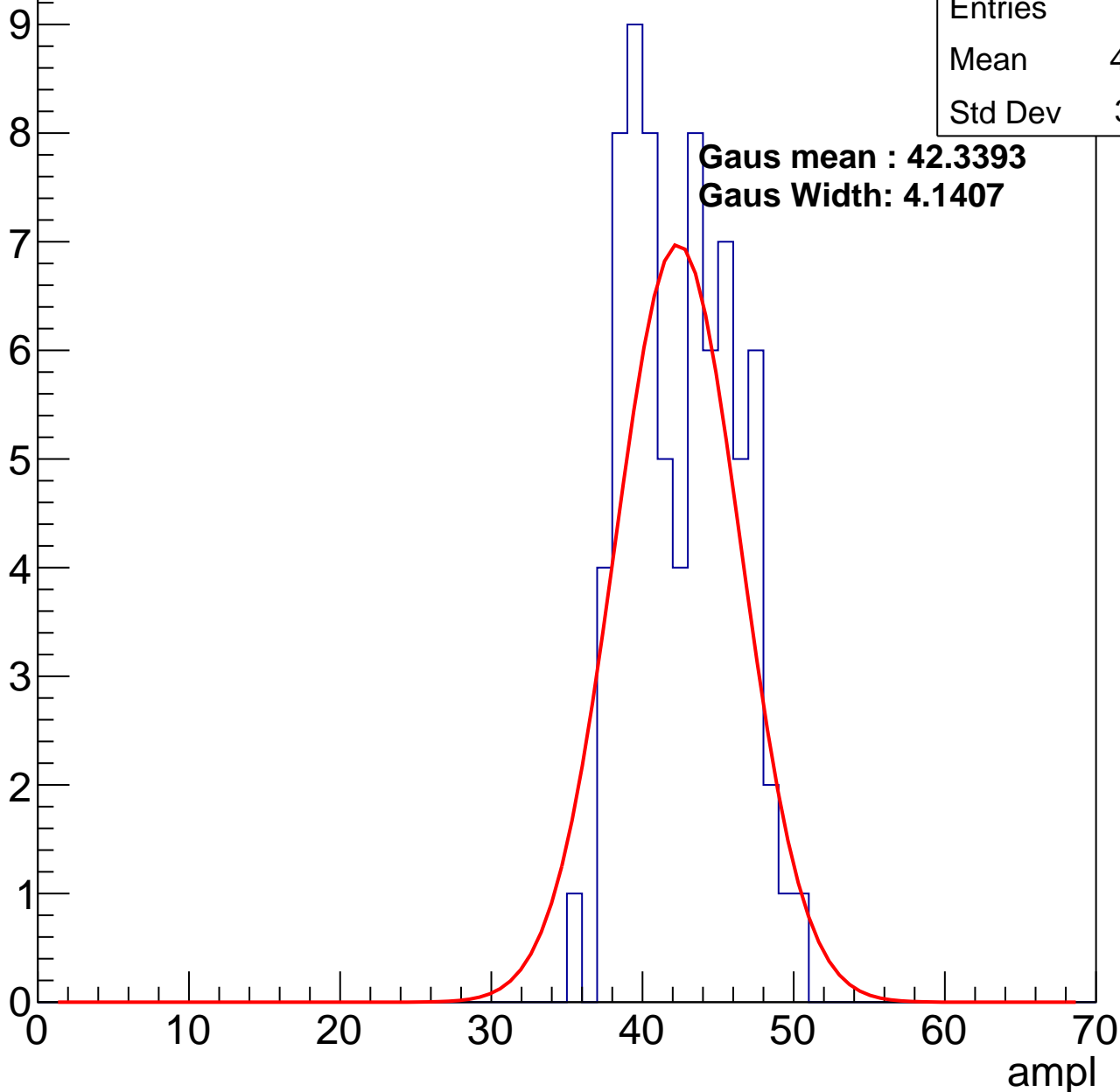
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	42.15
Std Dev	3.471

**Gaus mean : 42.3393**

**Gaus Width: 4.1407**

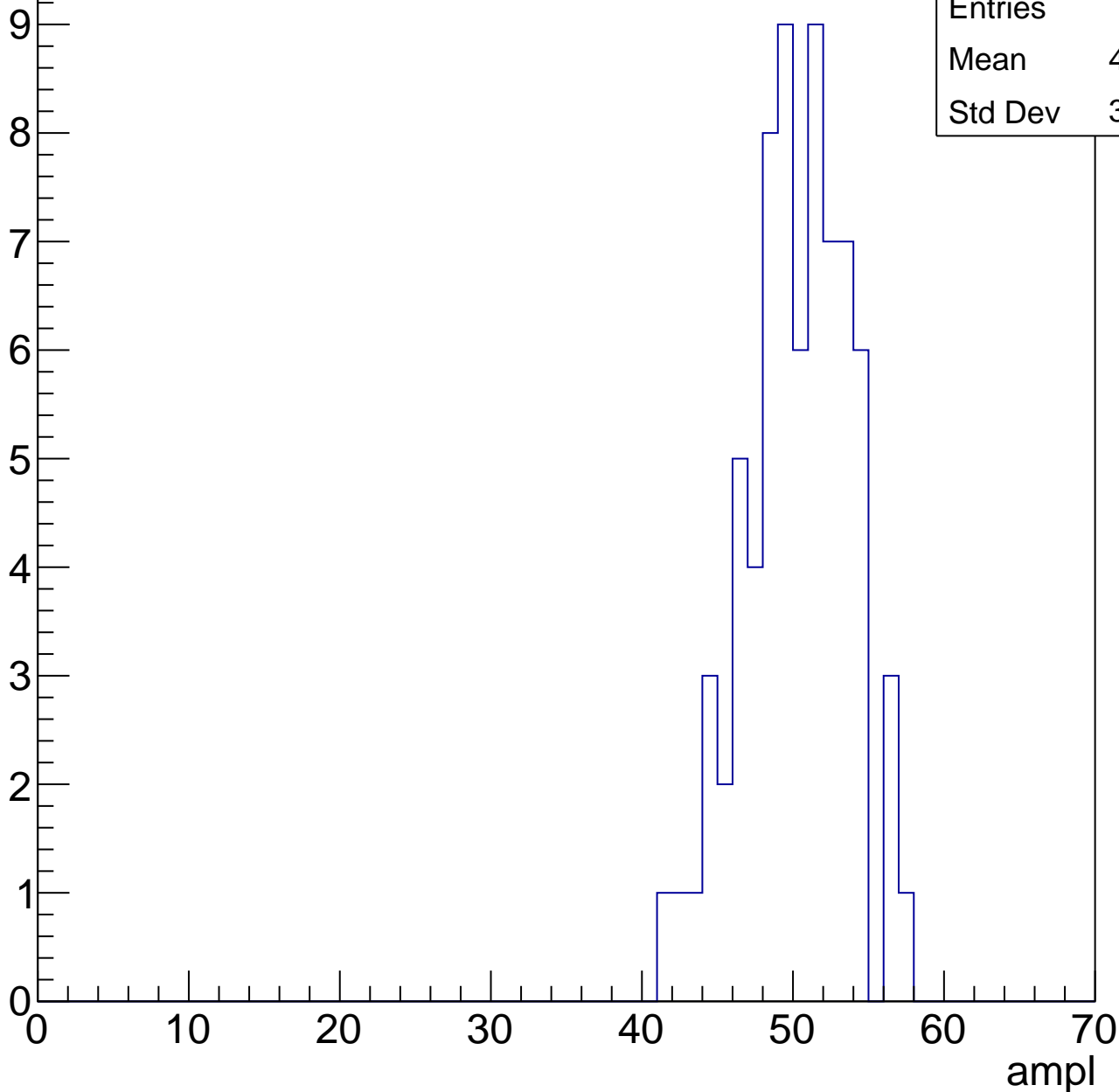


# B1L102S, U3-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	49.78
Std Dev	3.429

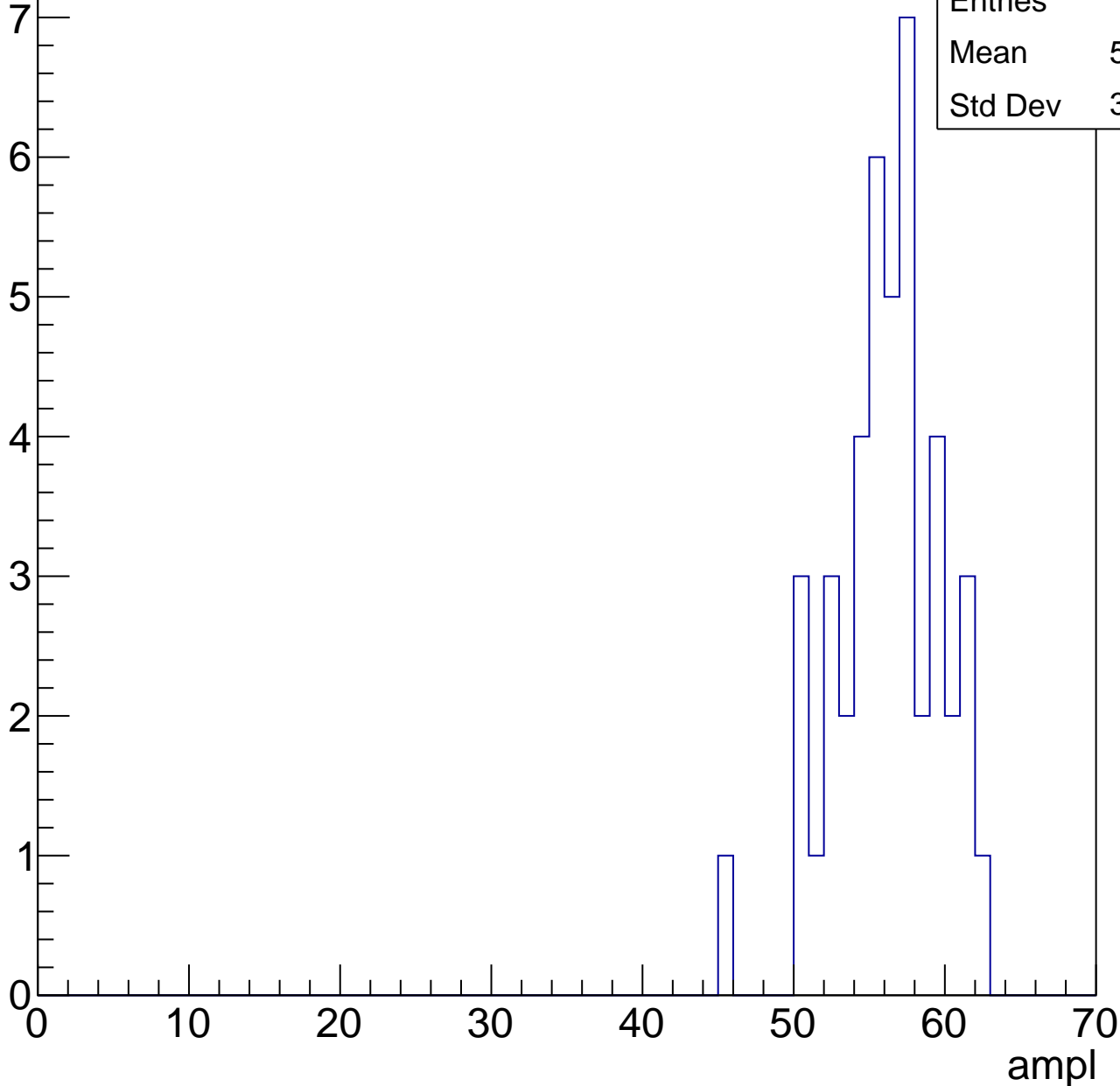


# B1L102S, U3-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

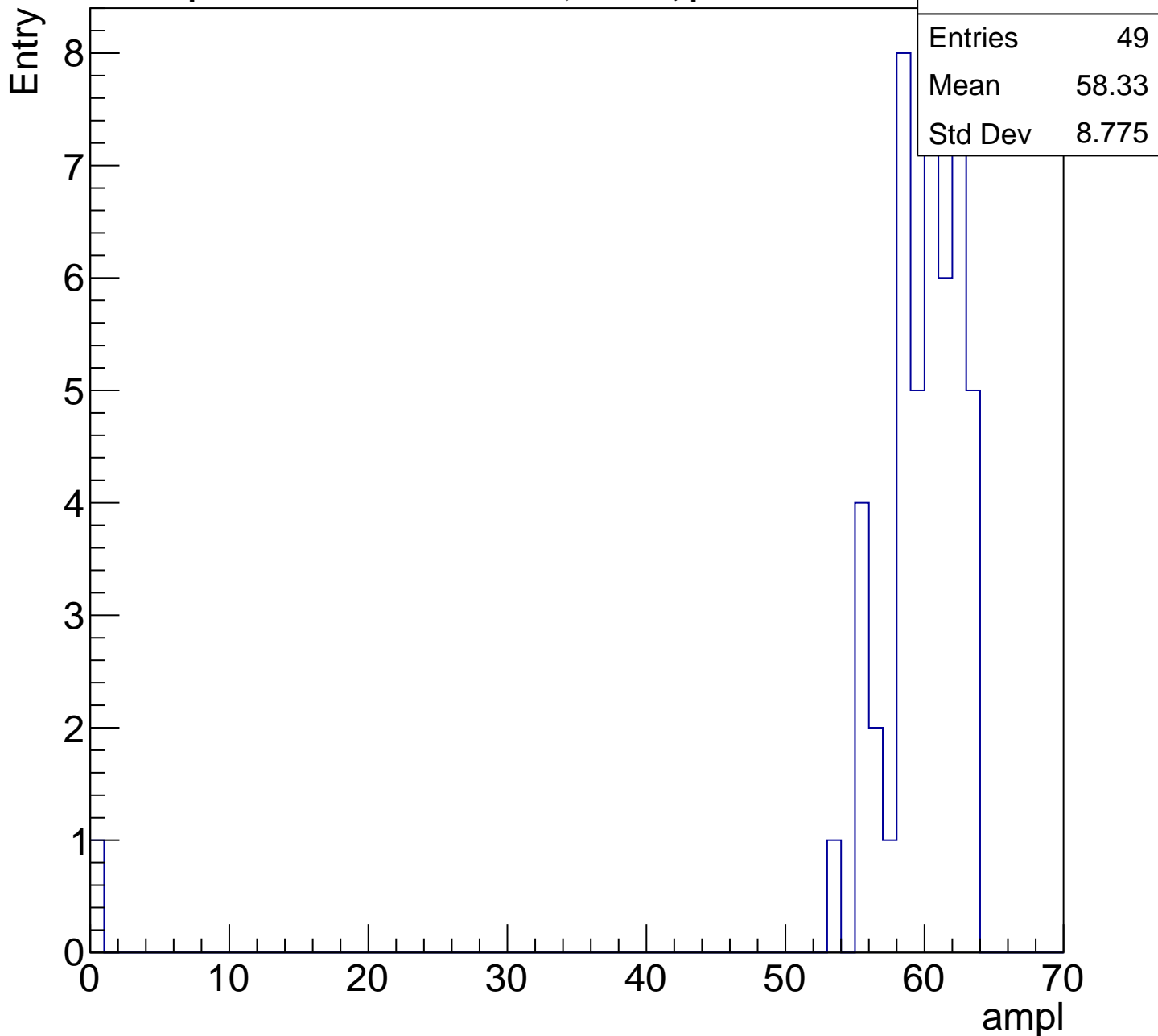
Entry

Entries	44
Mean	55.68
Std Dev	3.476



# B1L102S, U3-ch73, adc5

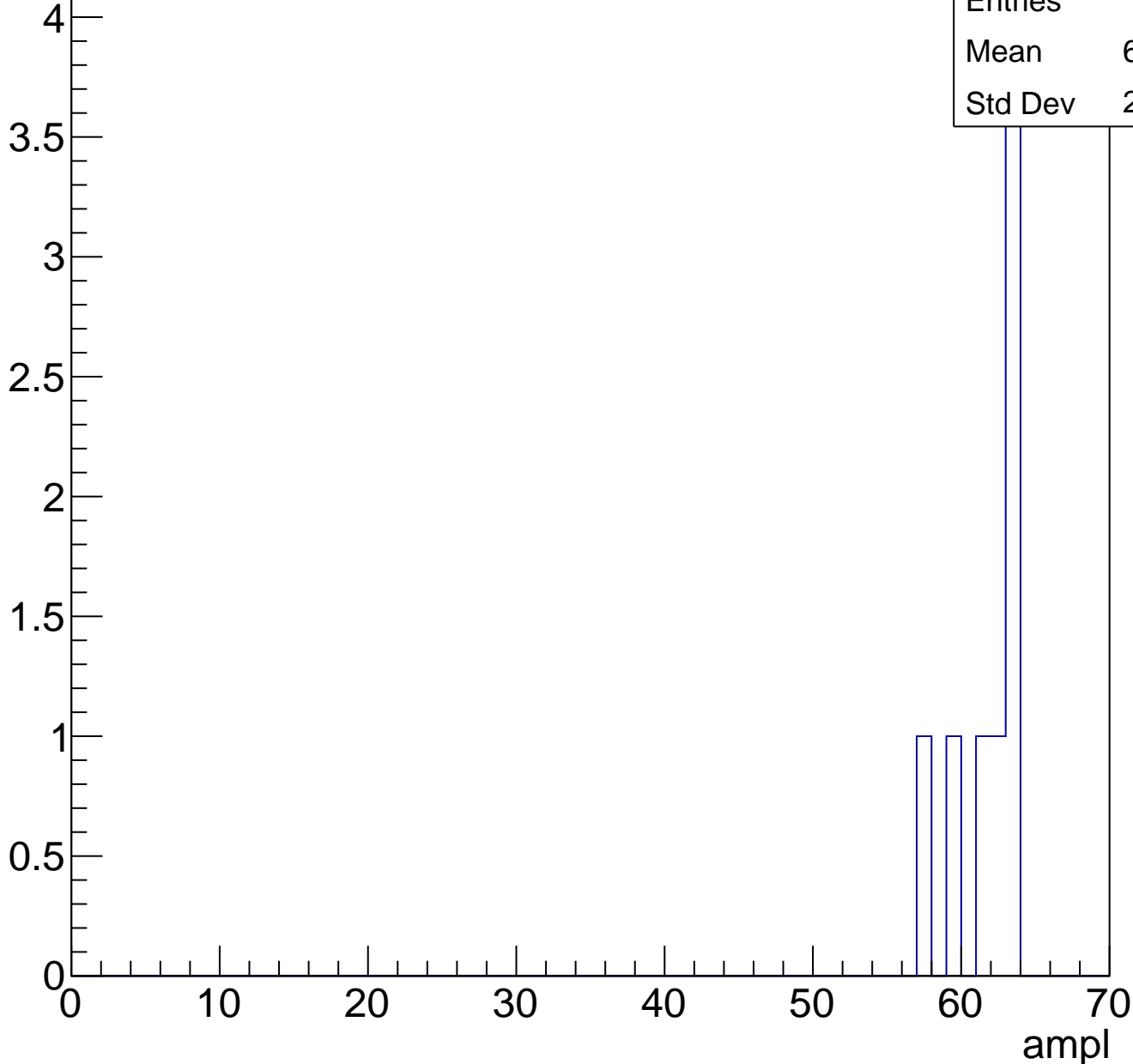
calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U3-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

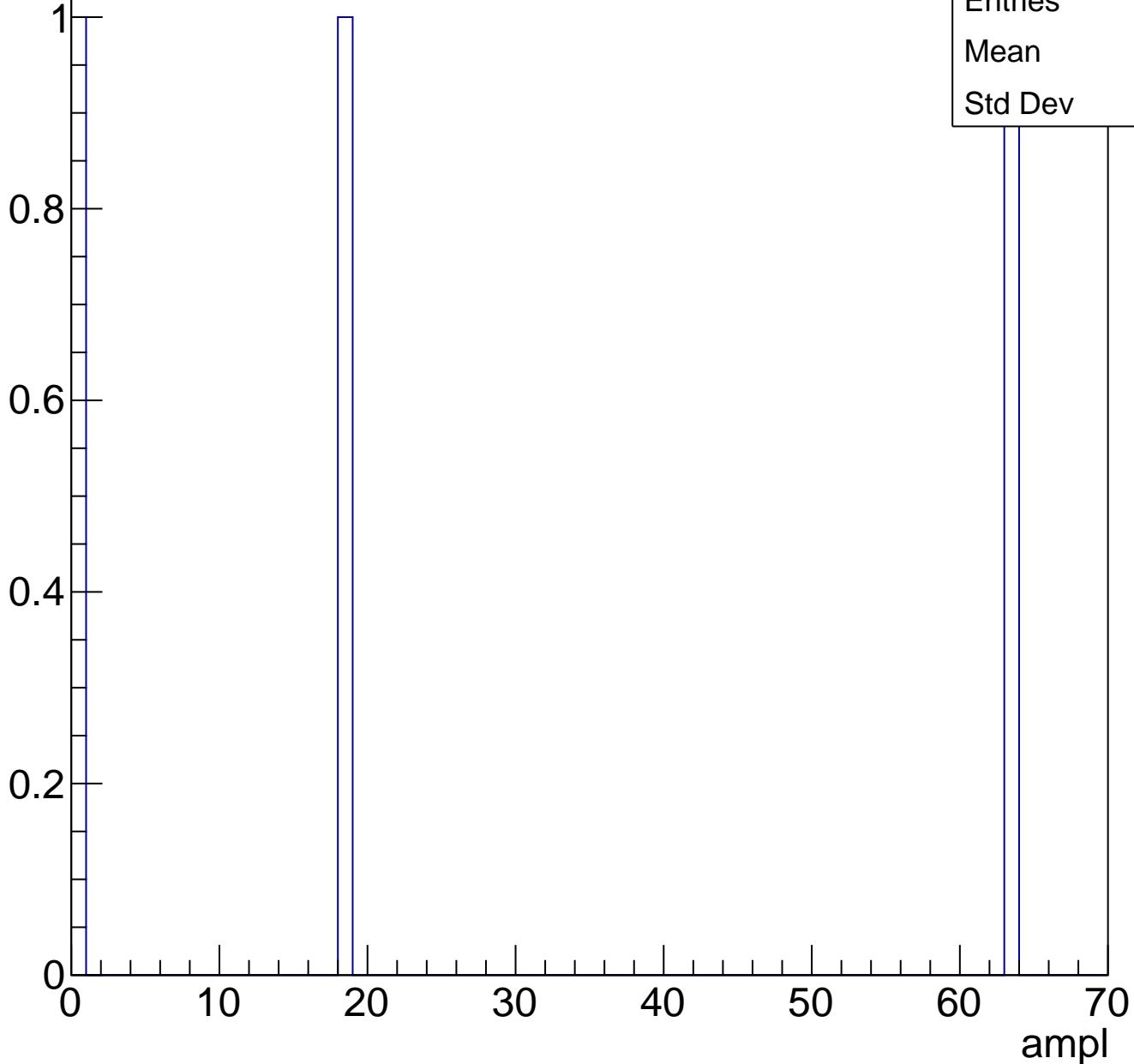




# B1L102S, U3-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch74, adc0

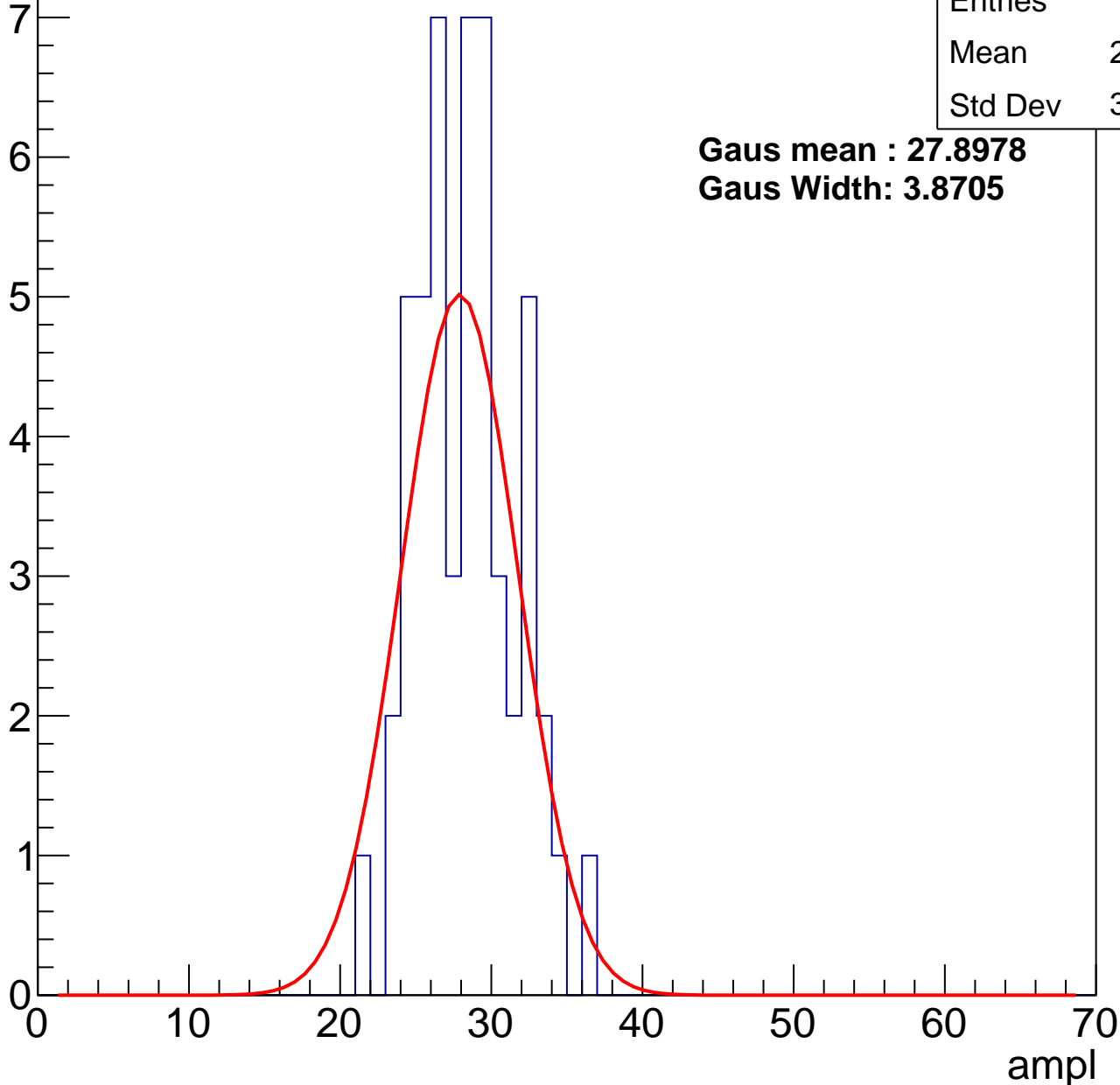
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	27.88
Std Dev	3.197

**Gaus mean : 27.8978**

**Gaus Width: 3.8705**



# B1L102S, U3-ch74, adc1

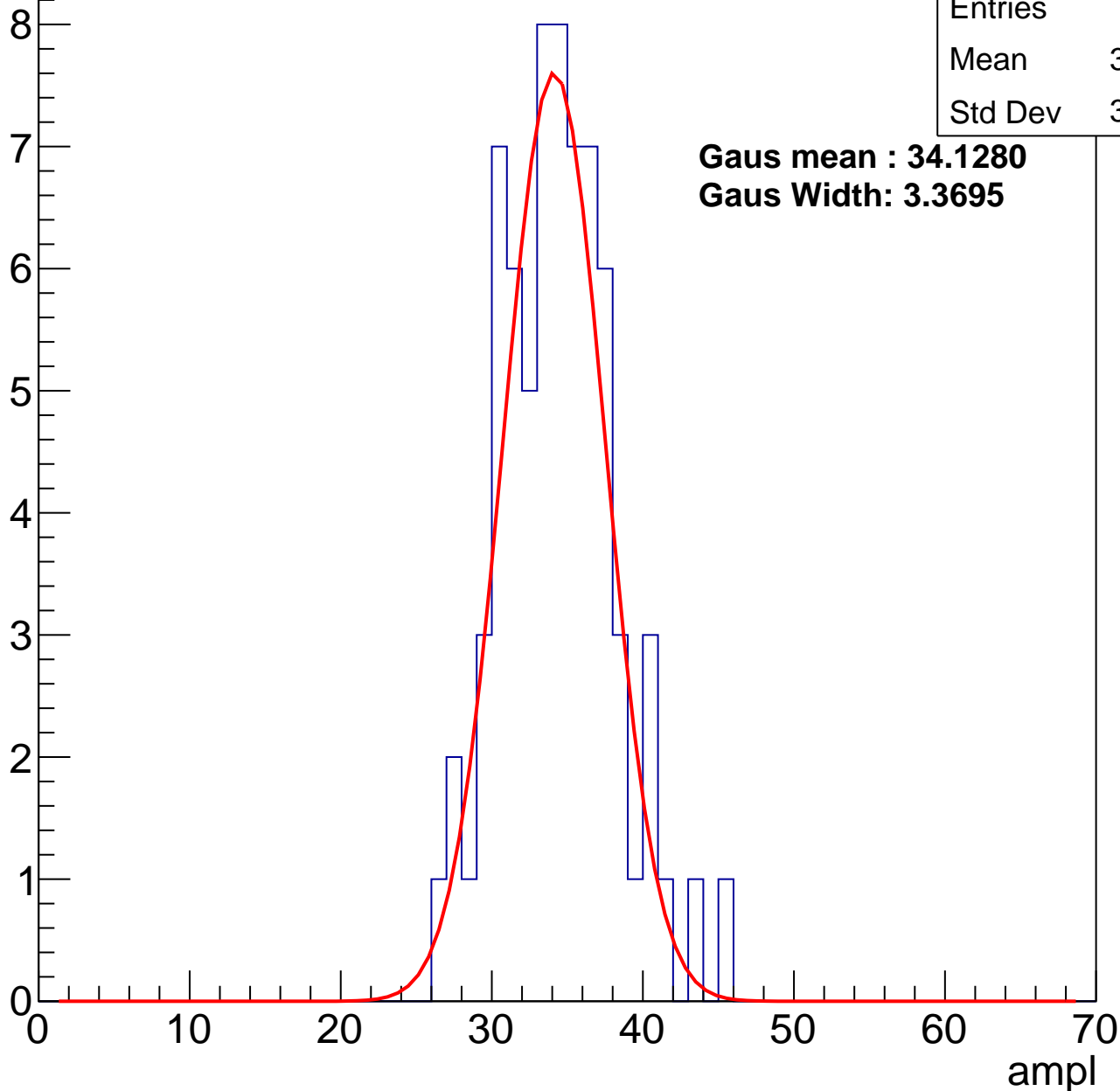
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	33.92
Std Dev	3.729

**Gaus mean : 34.1280**

**Gaus Width: 3.3695**



# B1L102S, U3-ch74, adc2

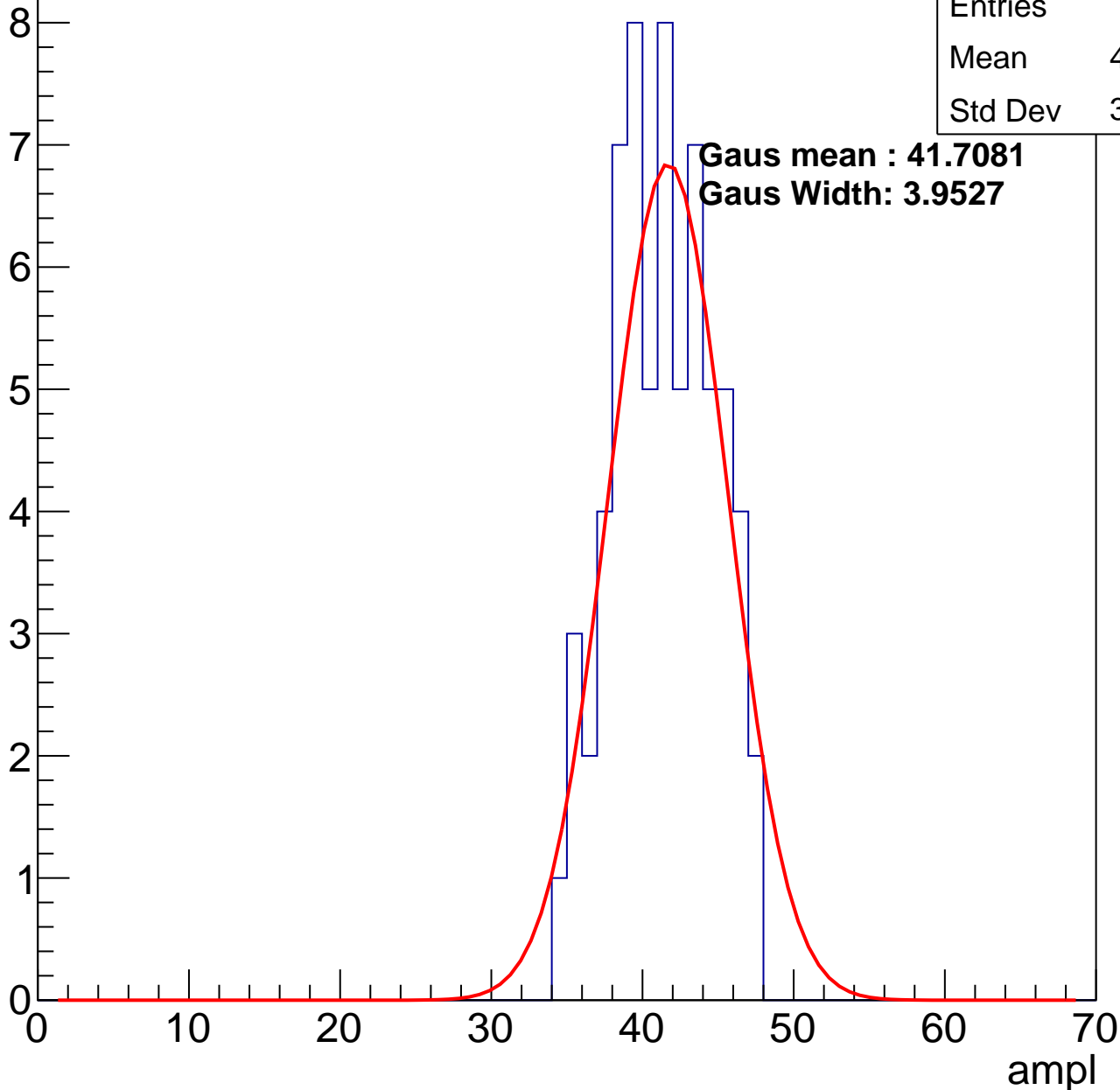
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	40.89
Std Dev	3.257

**Gaus mean : 41.7081**

**Gaus Width: 3.9527**

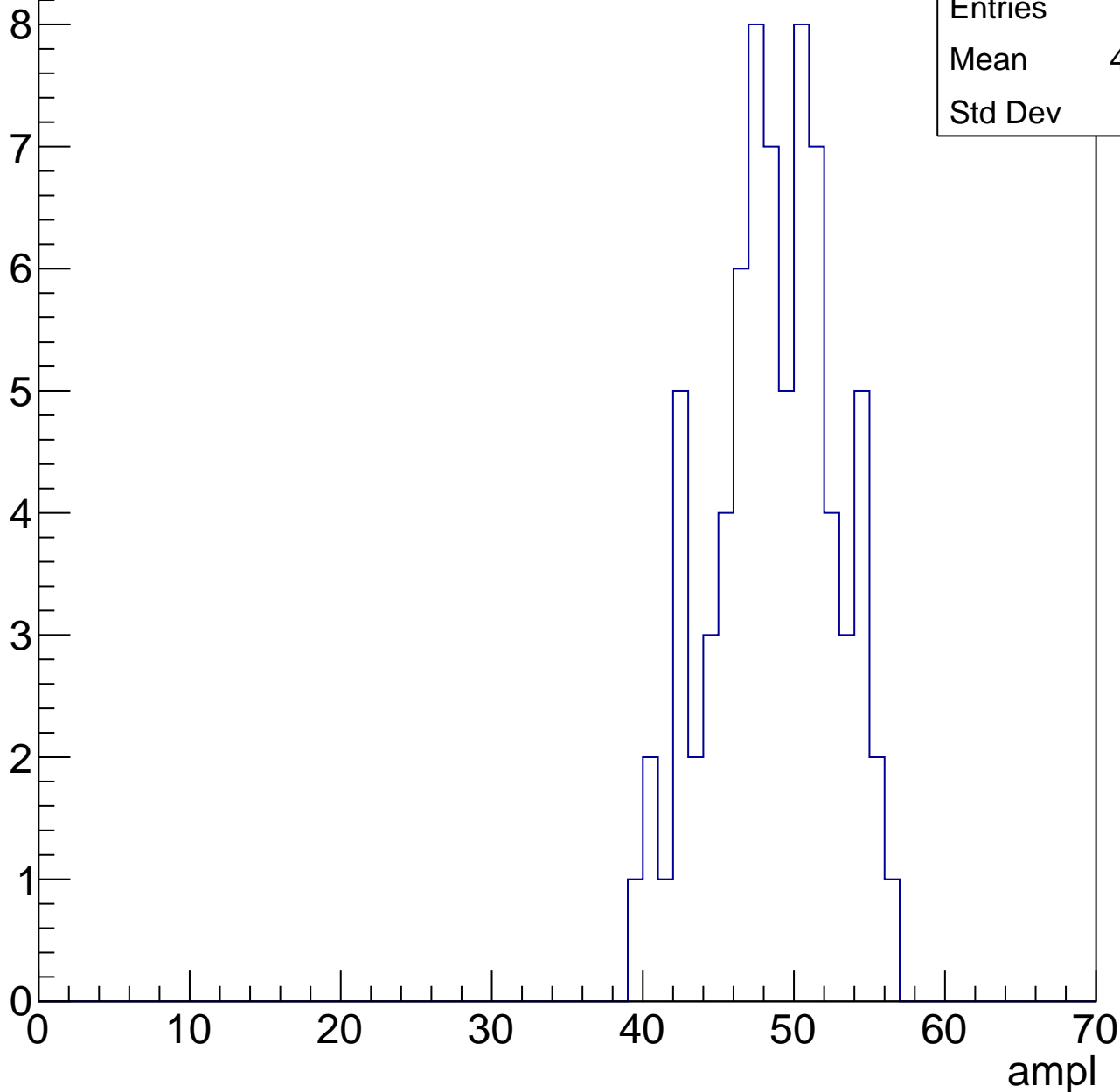


# B1L102S, U3-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	48.12
Std Dev	4

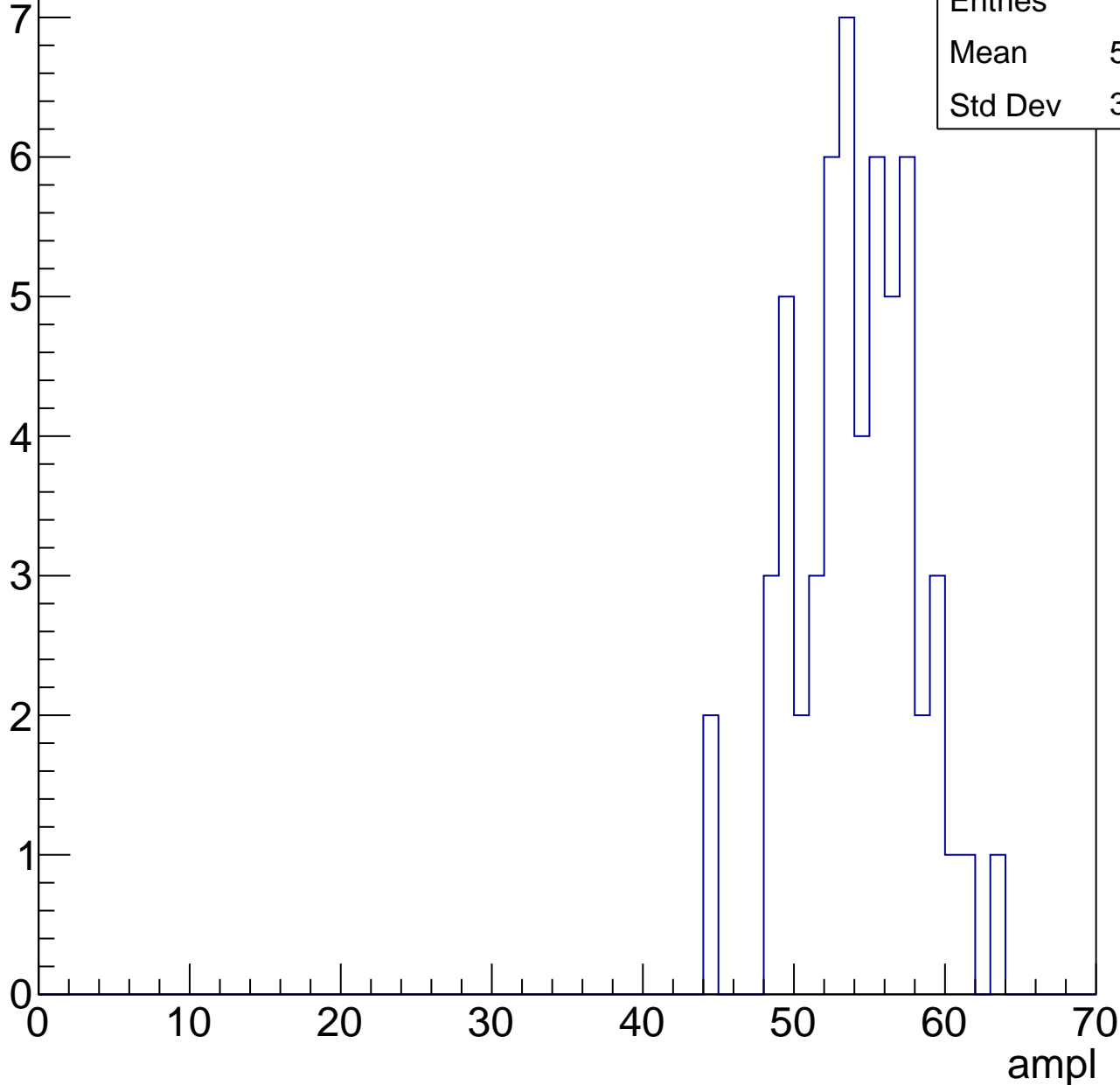


# B1L102S, U3-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	53.65
Std Dev	3.905



# B1L102S, U3-ch74, adc5

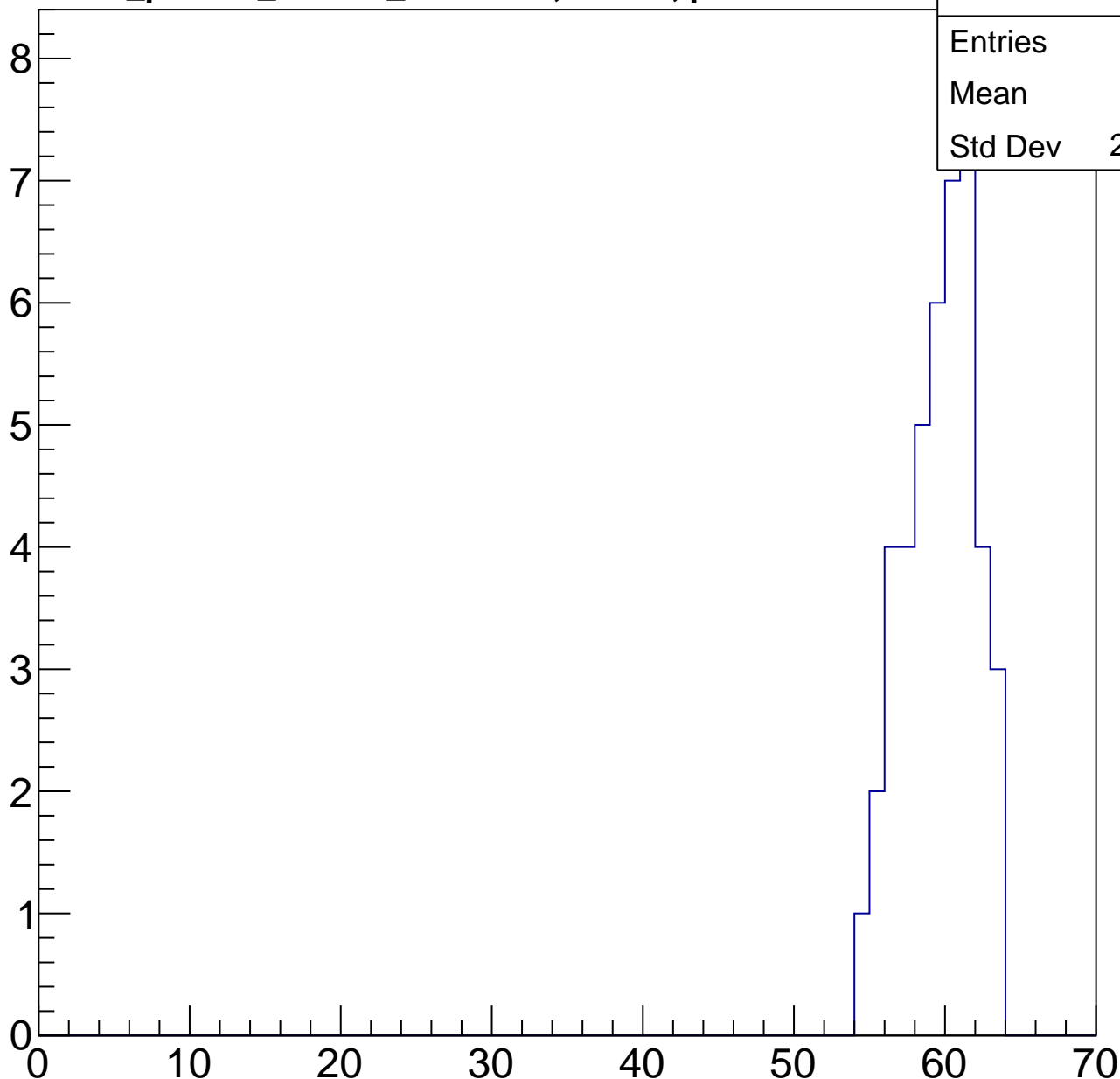
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	44
Mean	59.2
Std Dev	2.312

ampl

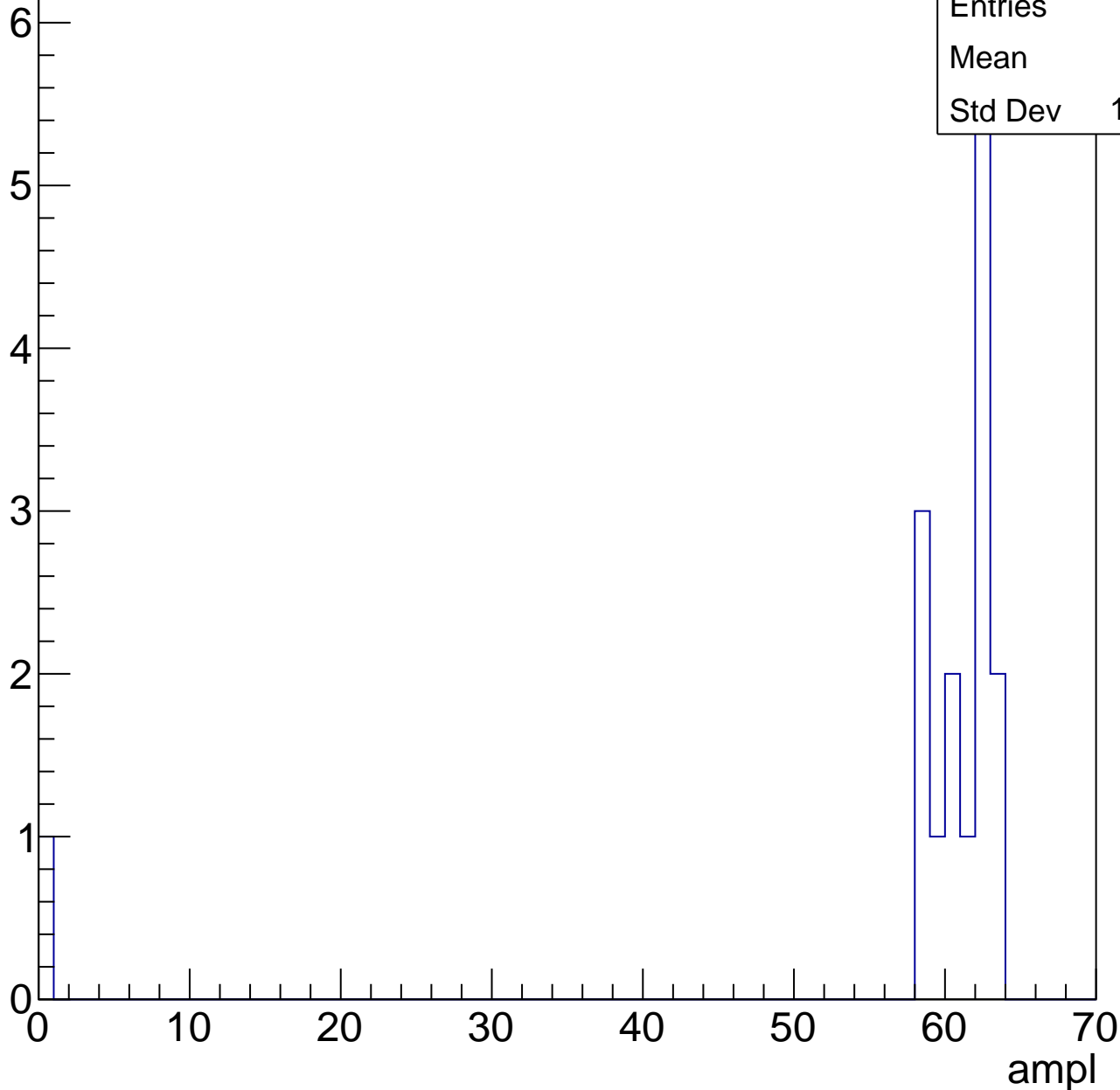


# B1L102S, U3-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	16
Mean	57
Std Dev	14.82

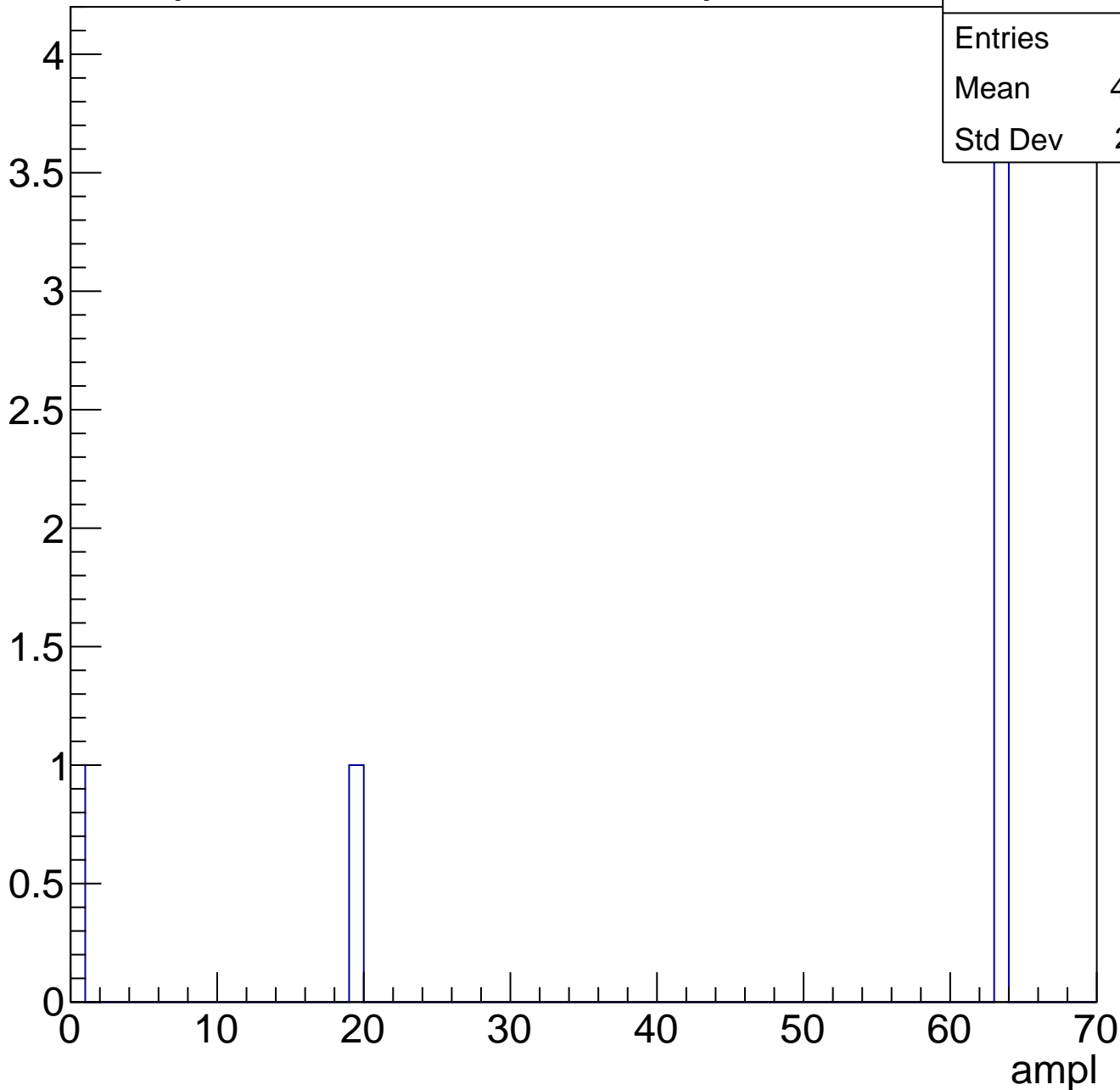




# B1L102S, U3-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	6
Mean	45.17
Std Dev	25.81

# B1L102S, U3-ch75, adc0

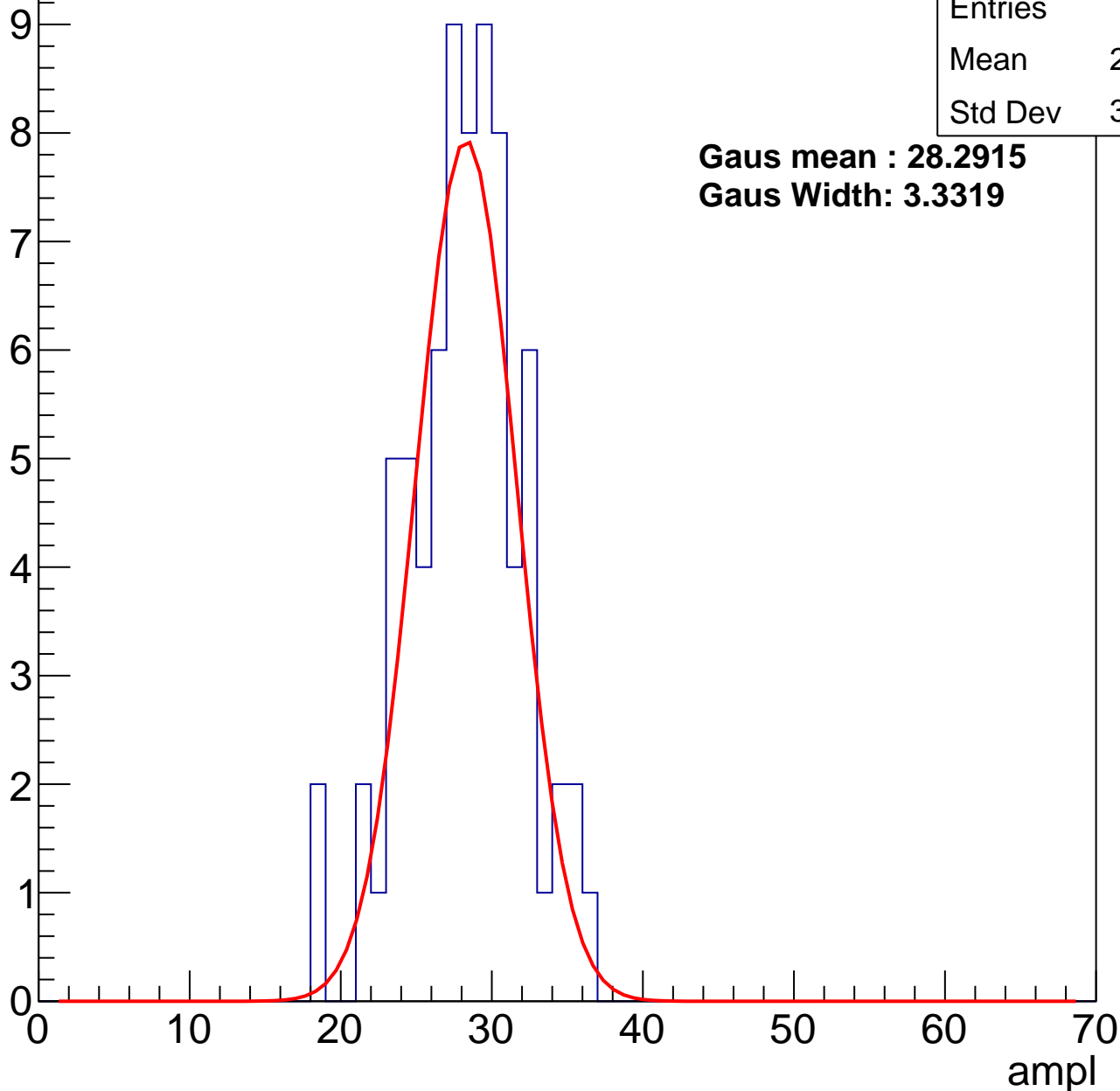
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	27.76
Std Dev	3.716

**Gaus mean : 28.2915**

**Gaus Width: 3.3319**



# B1L102S, U3-ch75, adc1

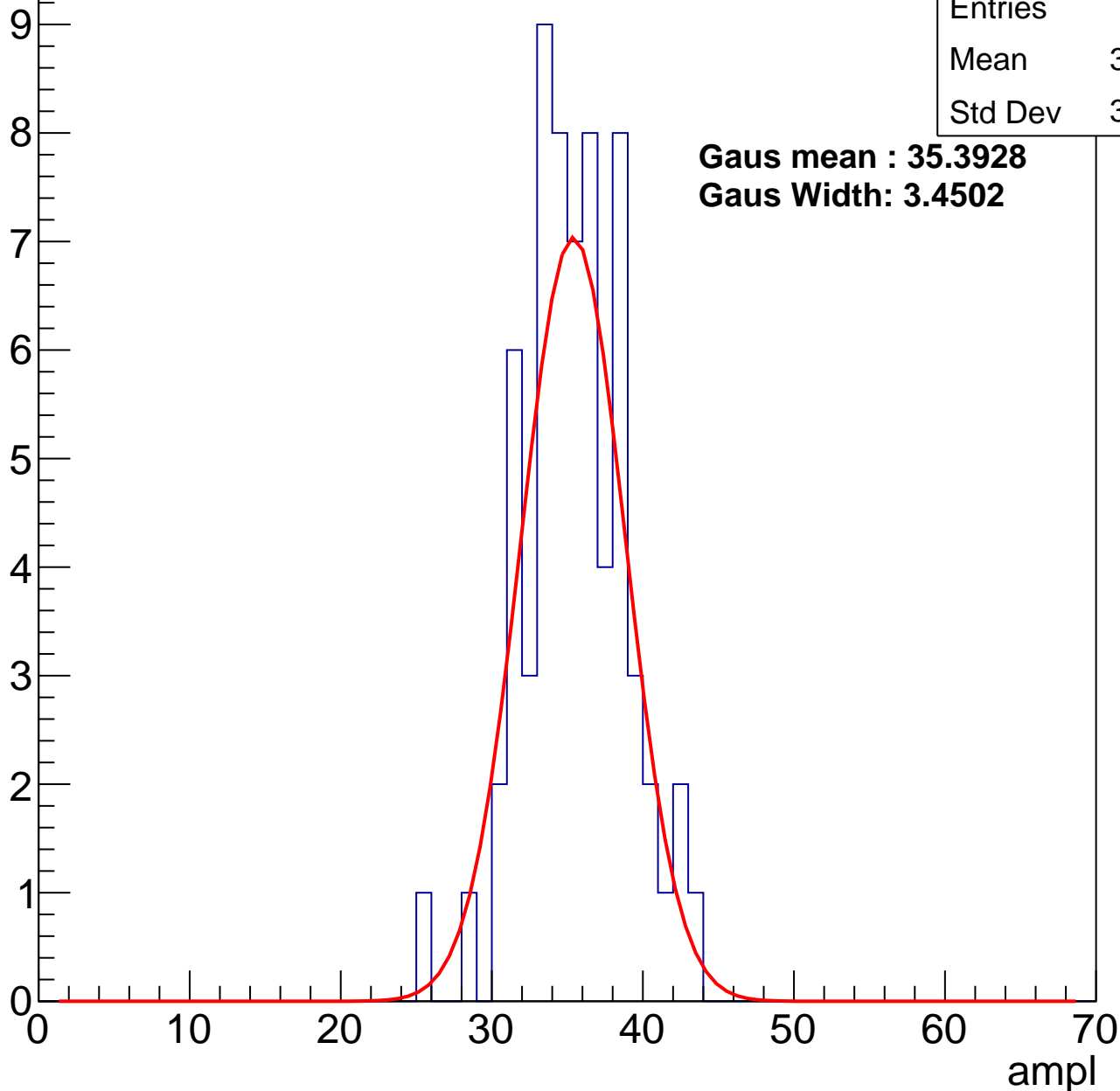
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	35.06
Std Dev	3.388

**Gaus mean : 35.3928**

**Gaus Width: 3.4502**



# B1L102S, U3-ch75, adc2

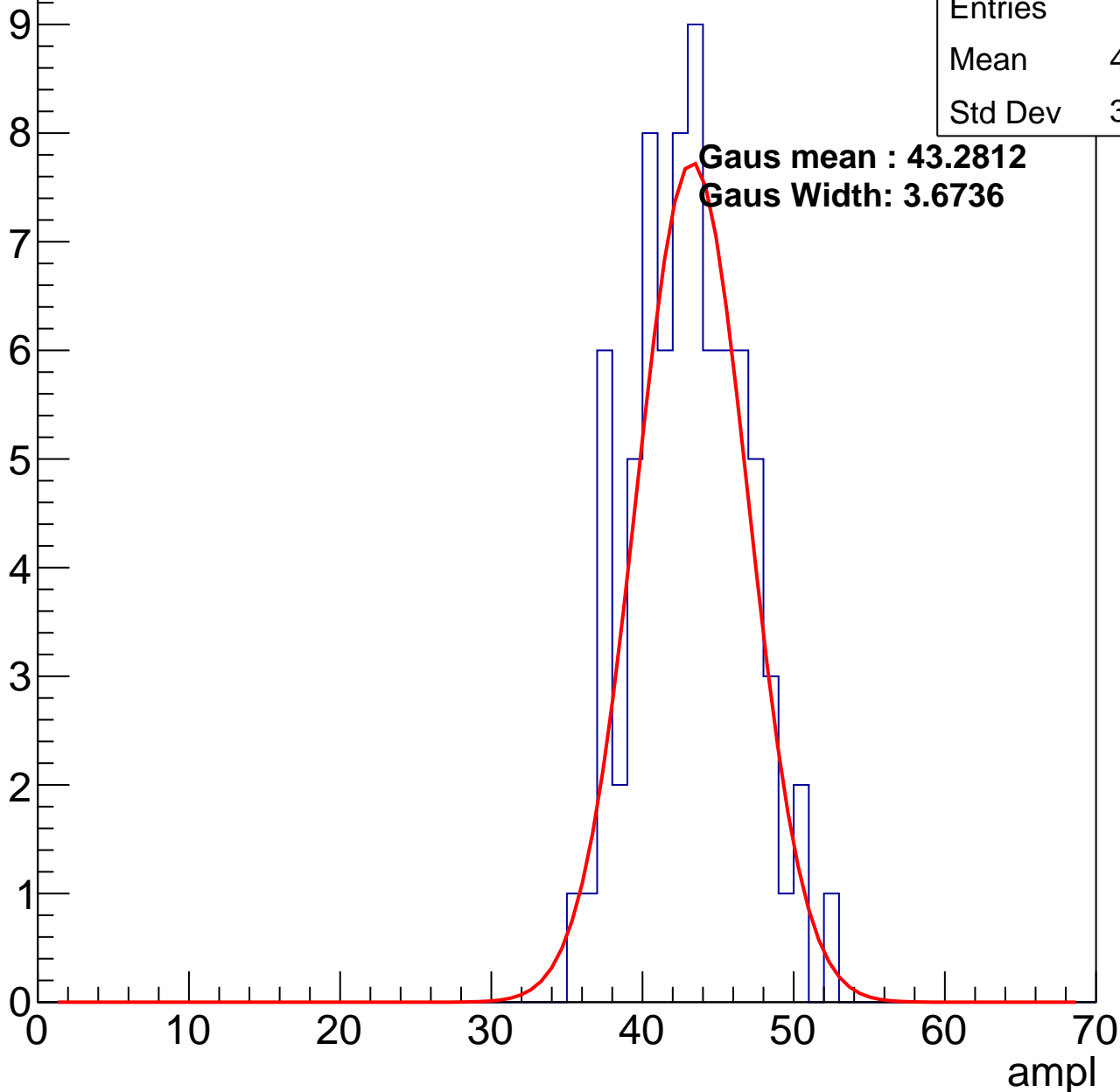
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	42.67
Std Dev	3.643

**Gaus mean : 43.2812**

**Gaus Width: 3.6736**

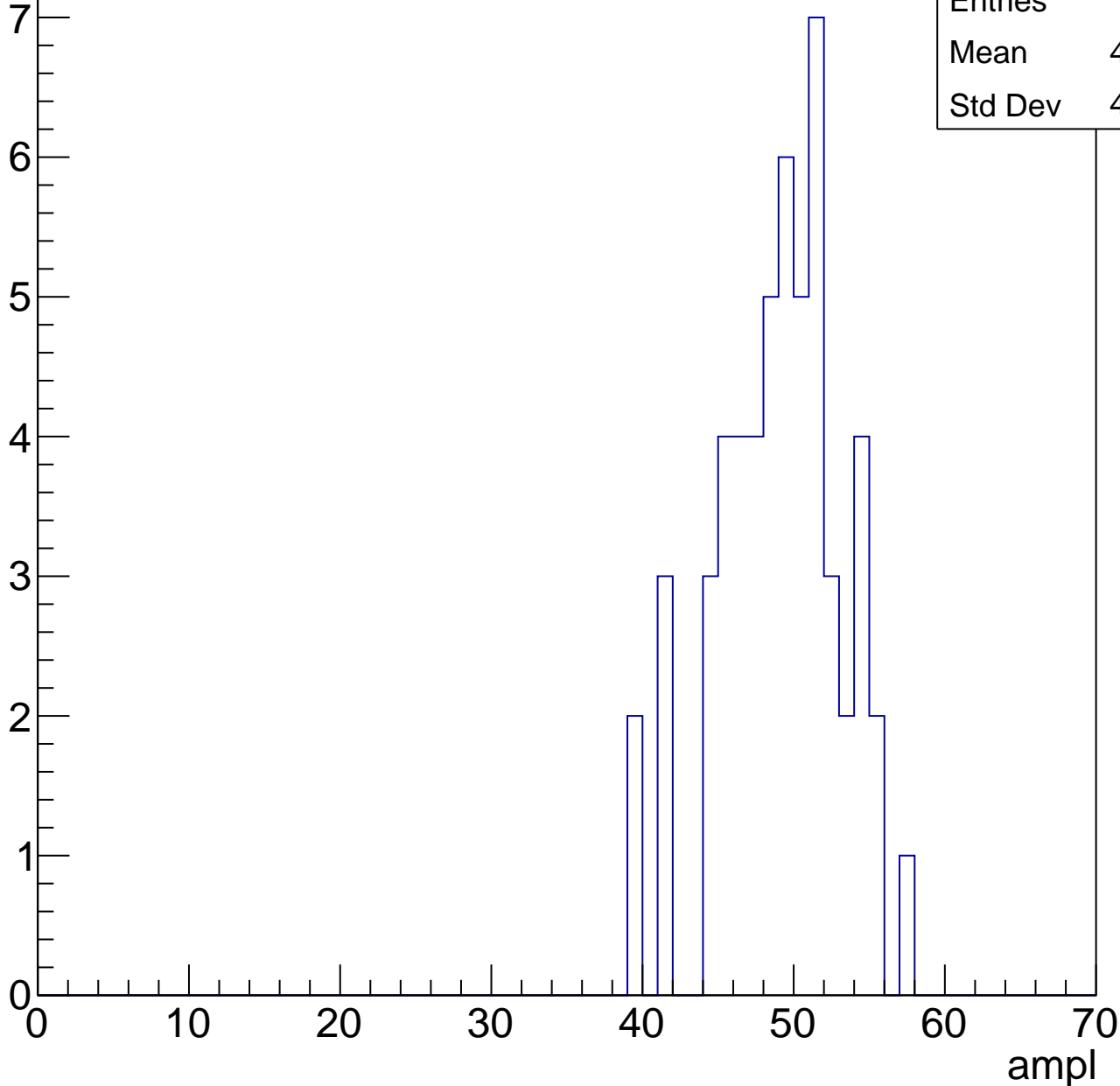


# B1L102S, U3-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	48.56
Std Dev	4.058



# B1L102S, U3-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

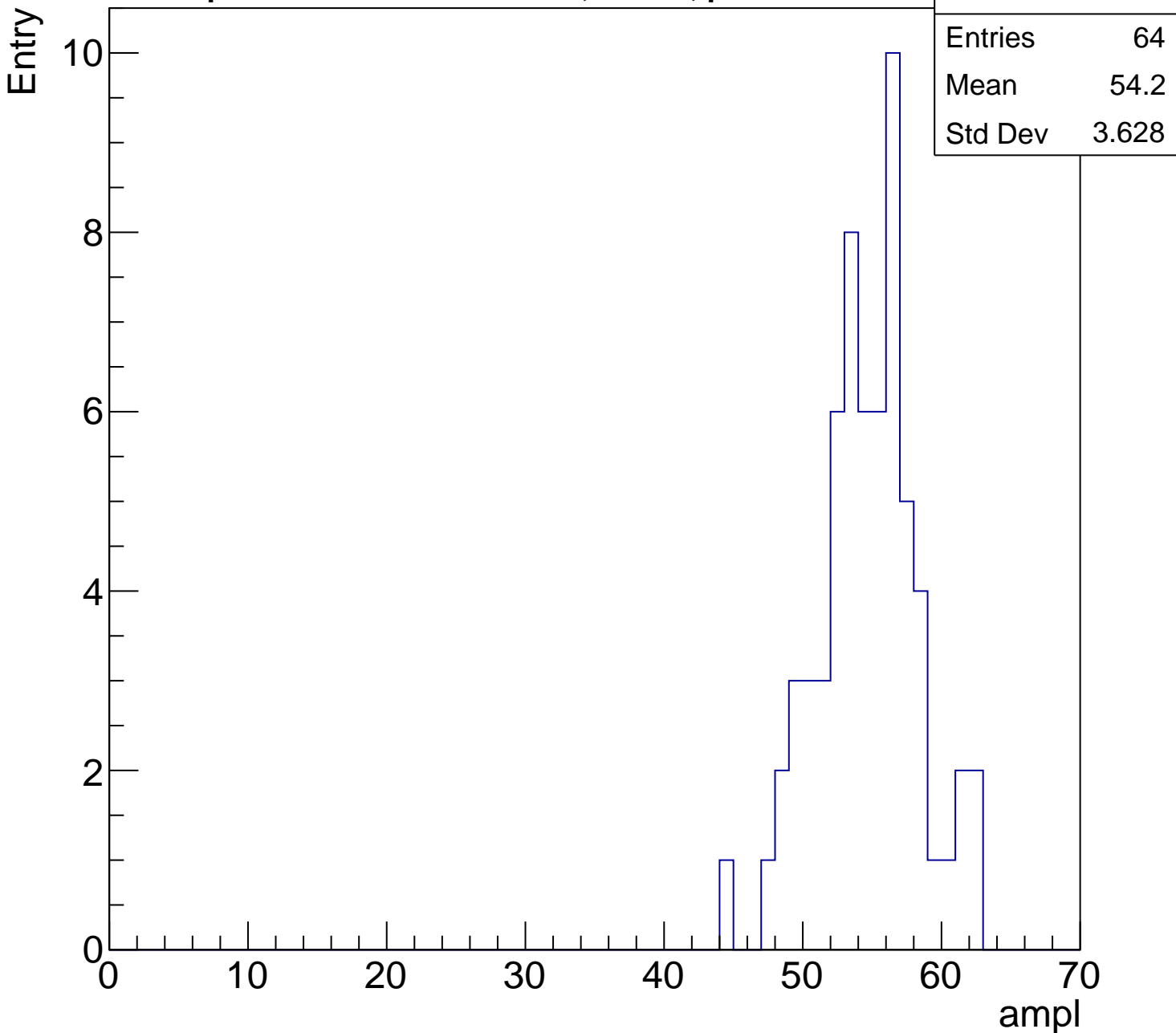
Entries	64
Mean	54.2
Std Dev	3.628

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

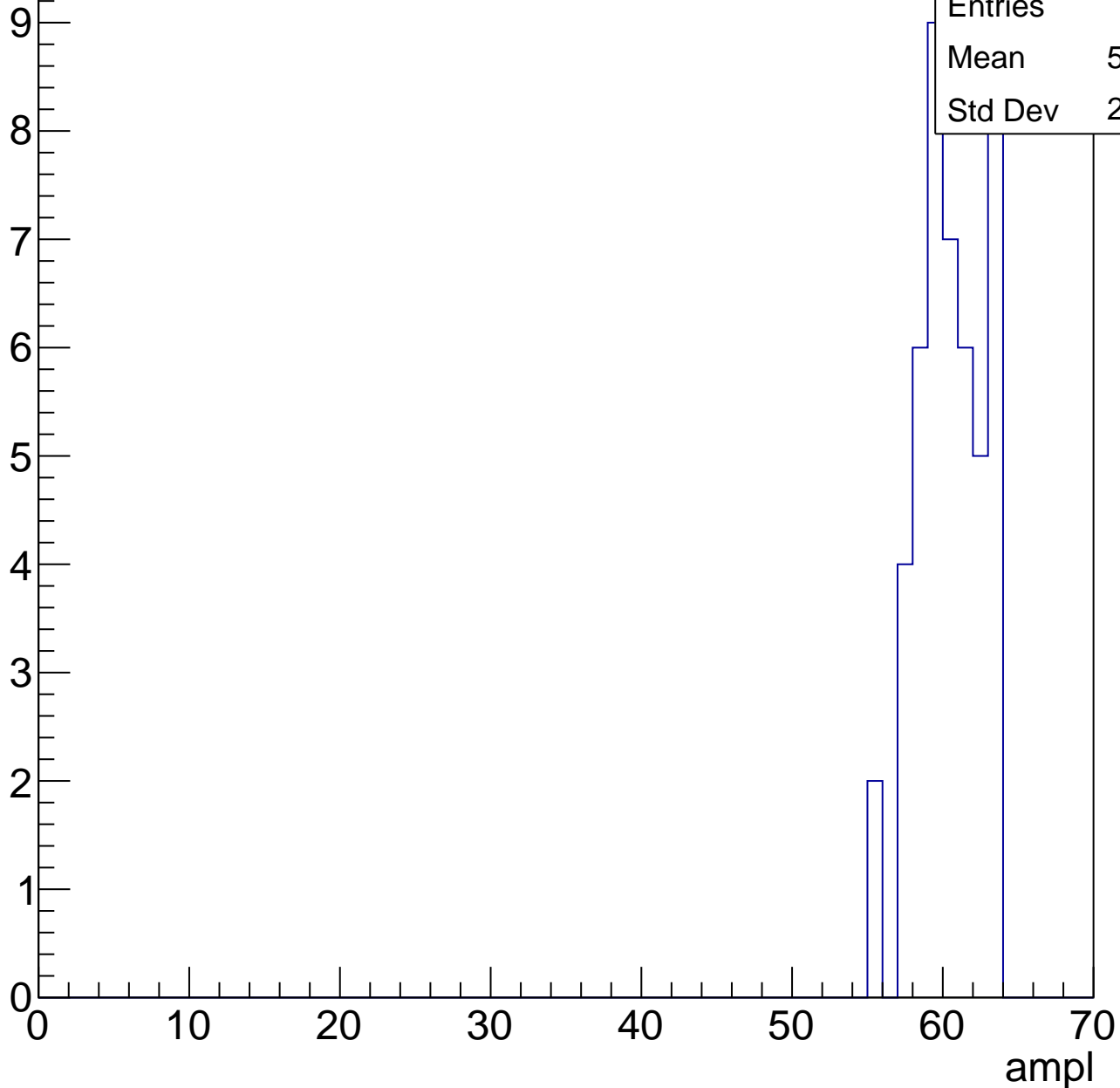
ampl



# B1L102S, U3-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	8
Mean	53.62
Std Dev	20.29

ampl



# B1L102S, U3-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch76, adc0

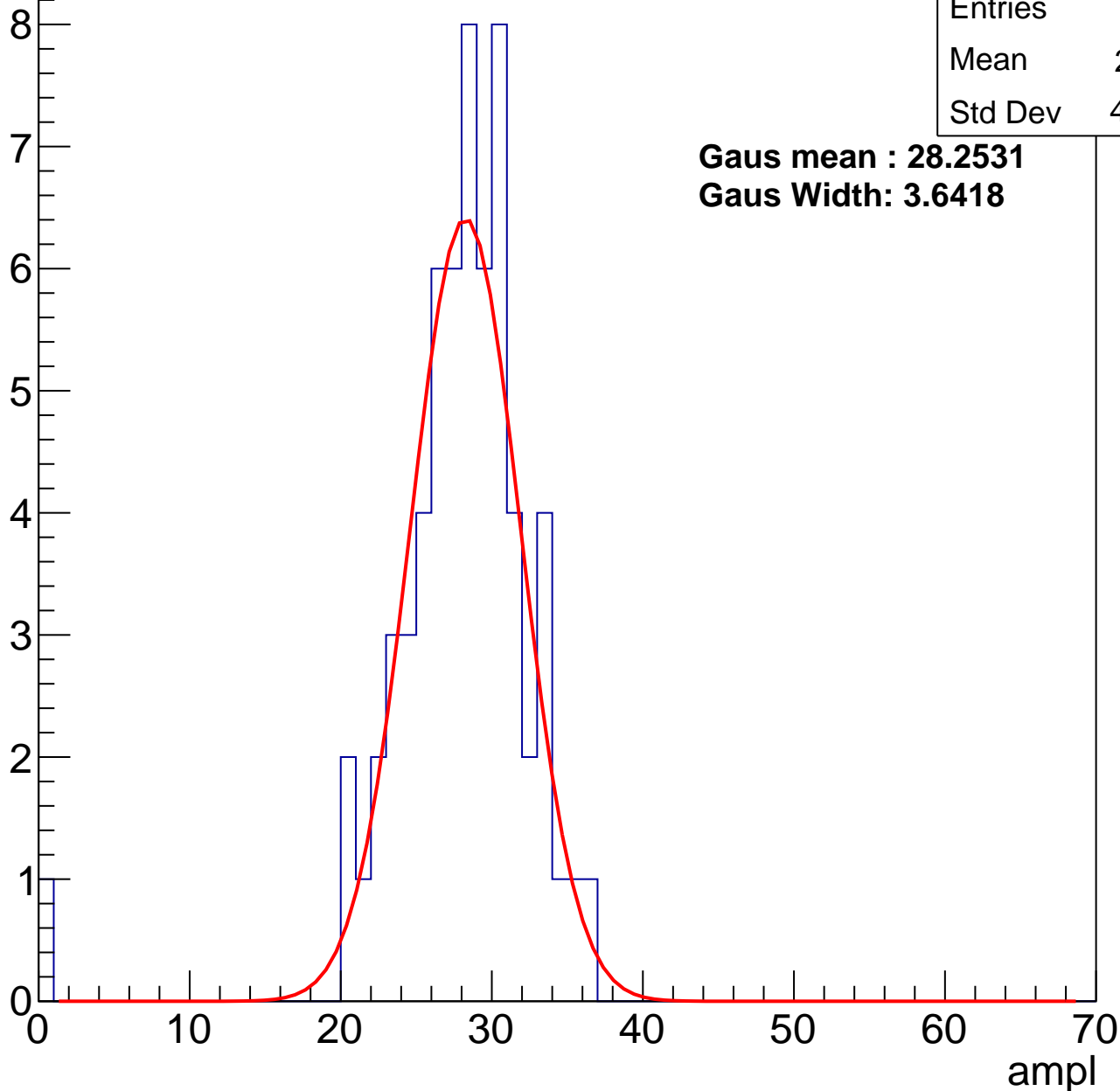
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	27.41
Std Dev	4.969

**Gaus mean : 28.2531**

**Gaus Width: 3.6418**



# B1L102S, U3-ch76, adc1

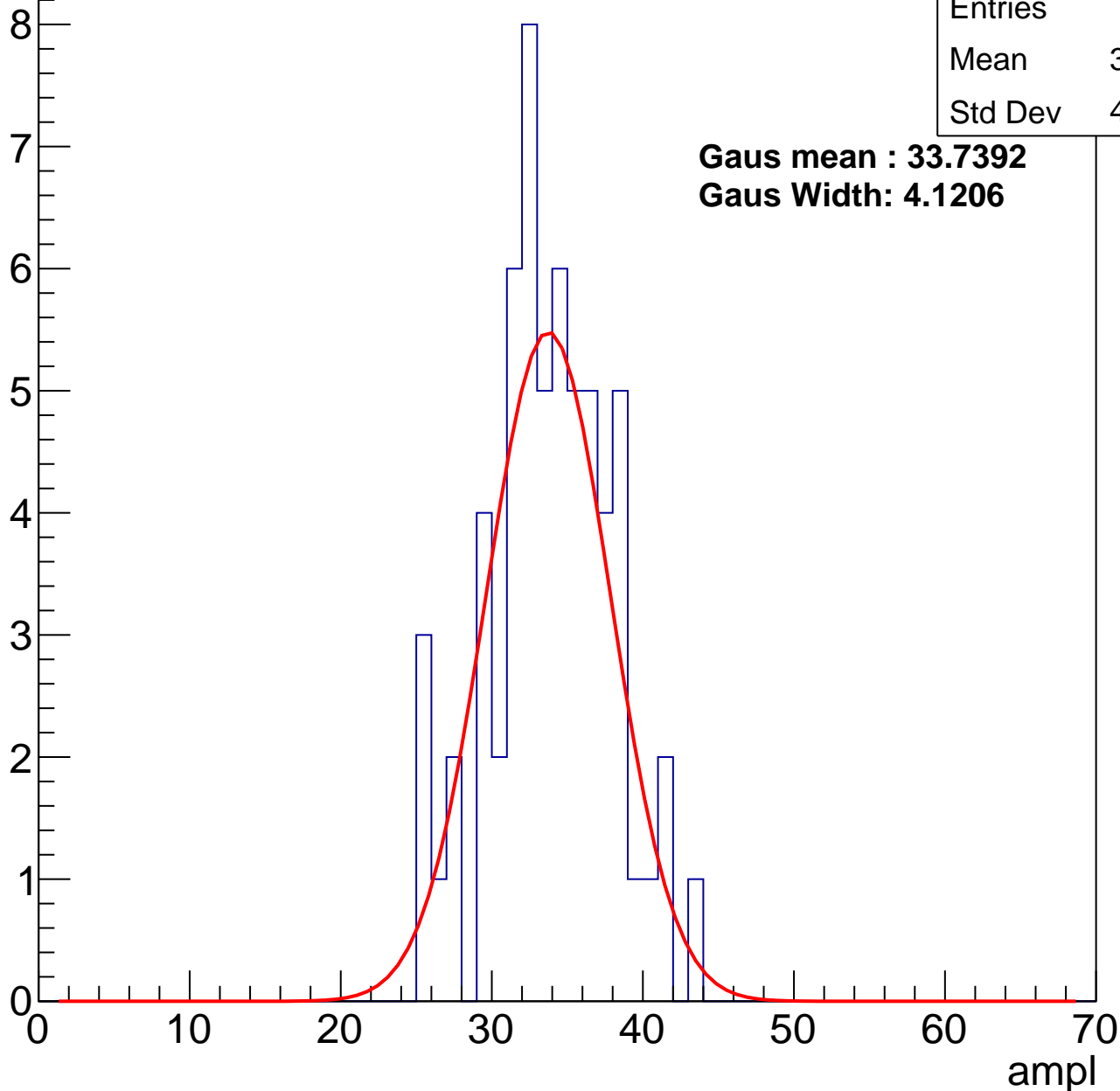
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	33.43
Std Dev	4.026

**Gaus mean : 33.7392**

**Gaus Width: 4.1206**



# B1L102S, U3-ch76, adc2

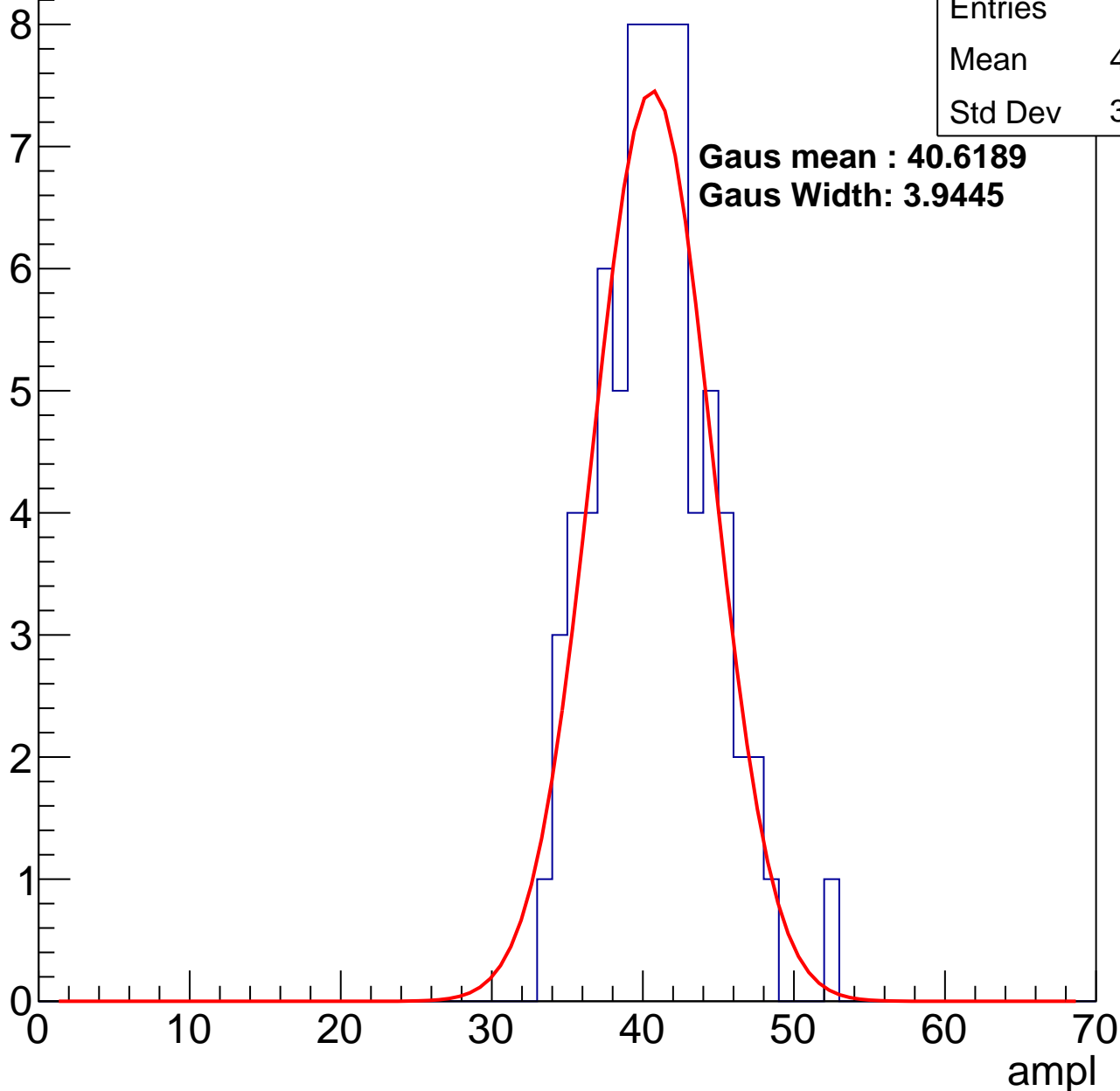
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	40.34
Std Dev	3.728

**Gaus mean : 40.6189**

**Gaus Width: 3.9445**

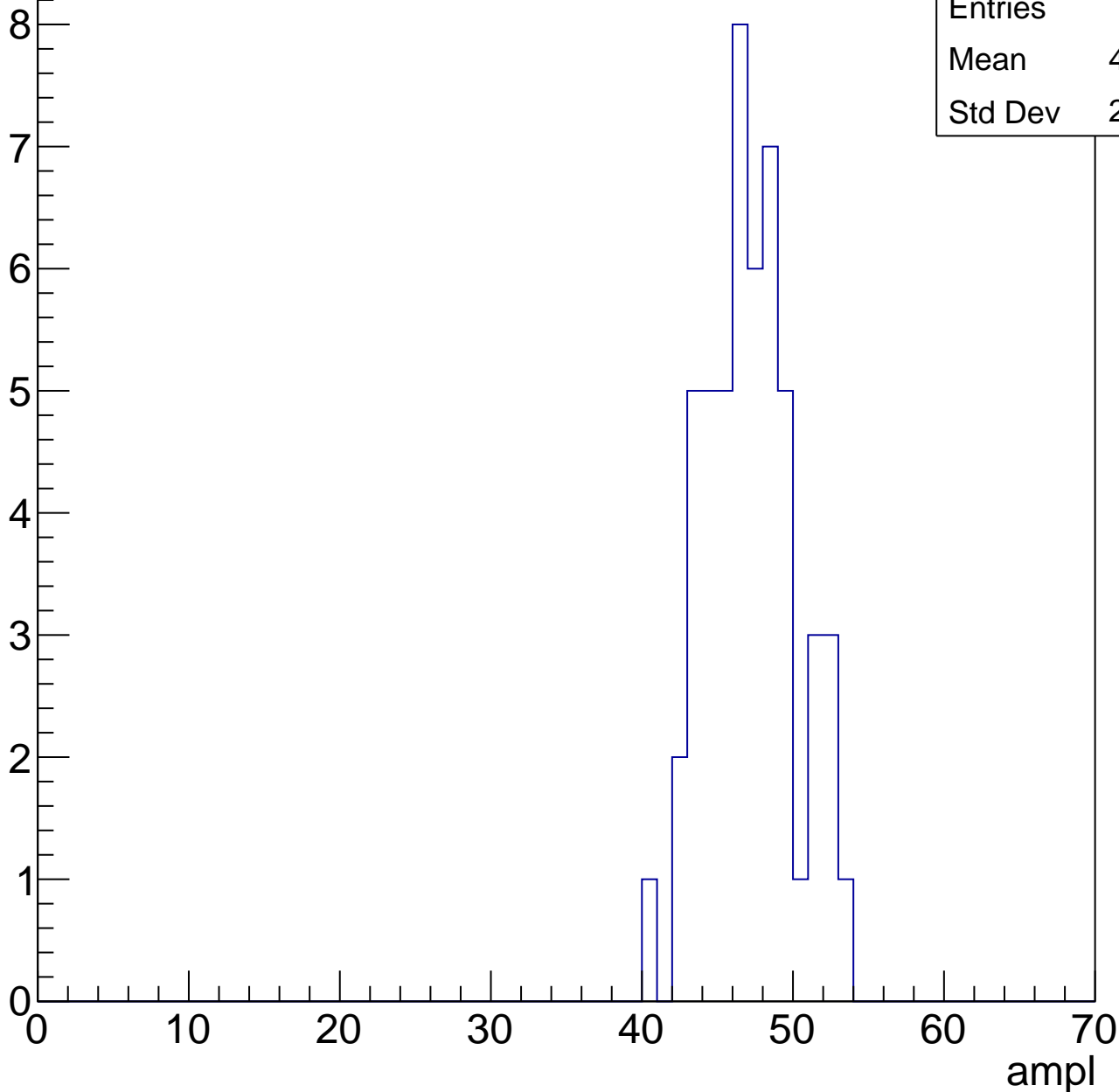


# B1L102S, U3-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	46.67
Std Dev	2.914

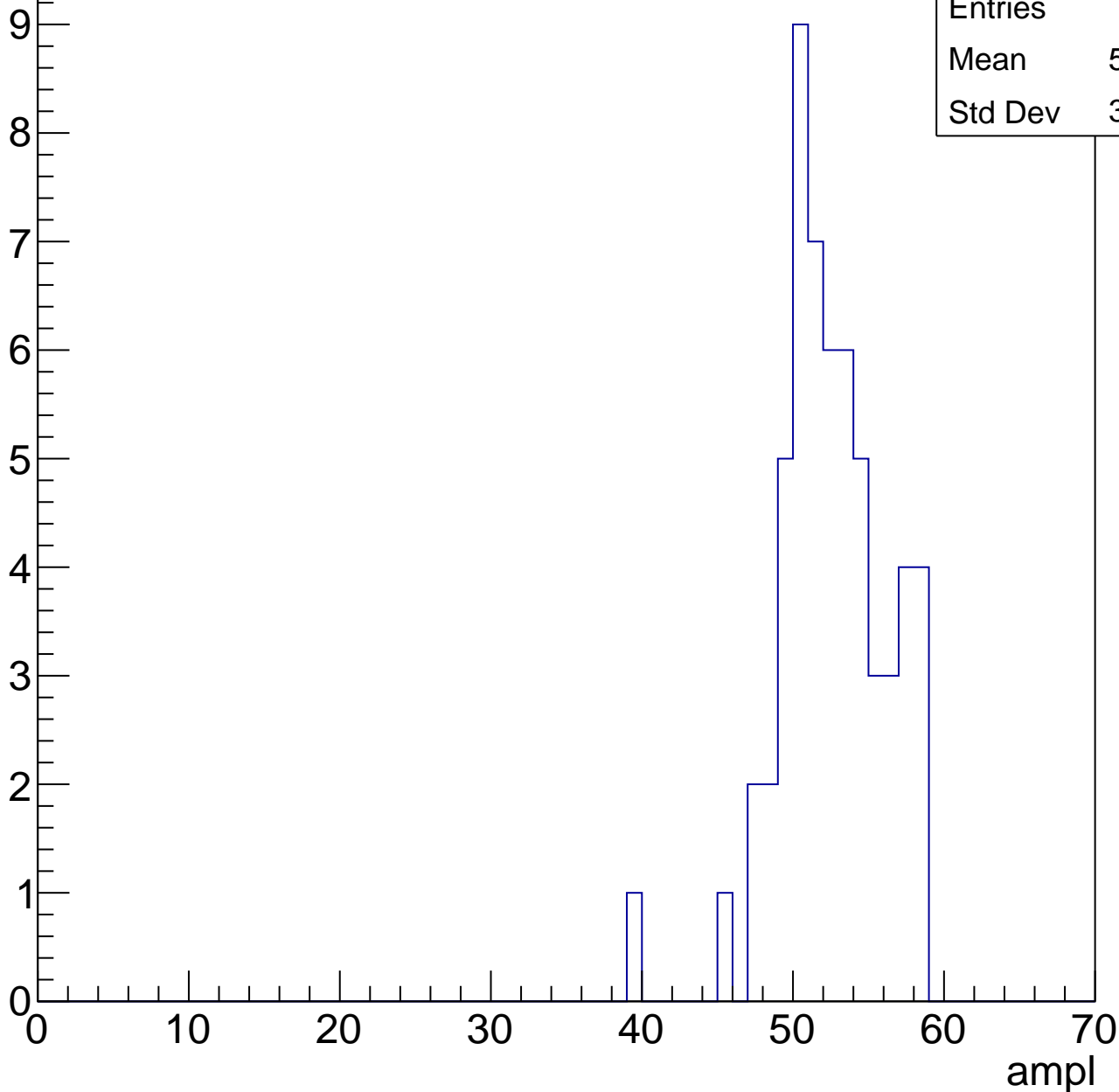


# B1L102S, U3-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	52.05
Std Dev	3.555

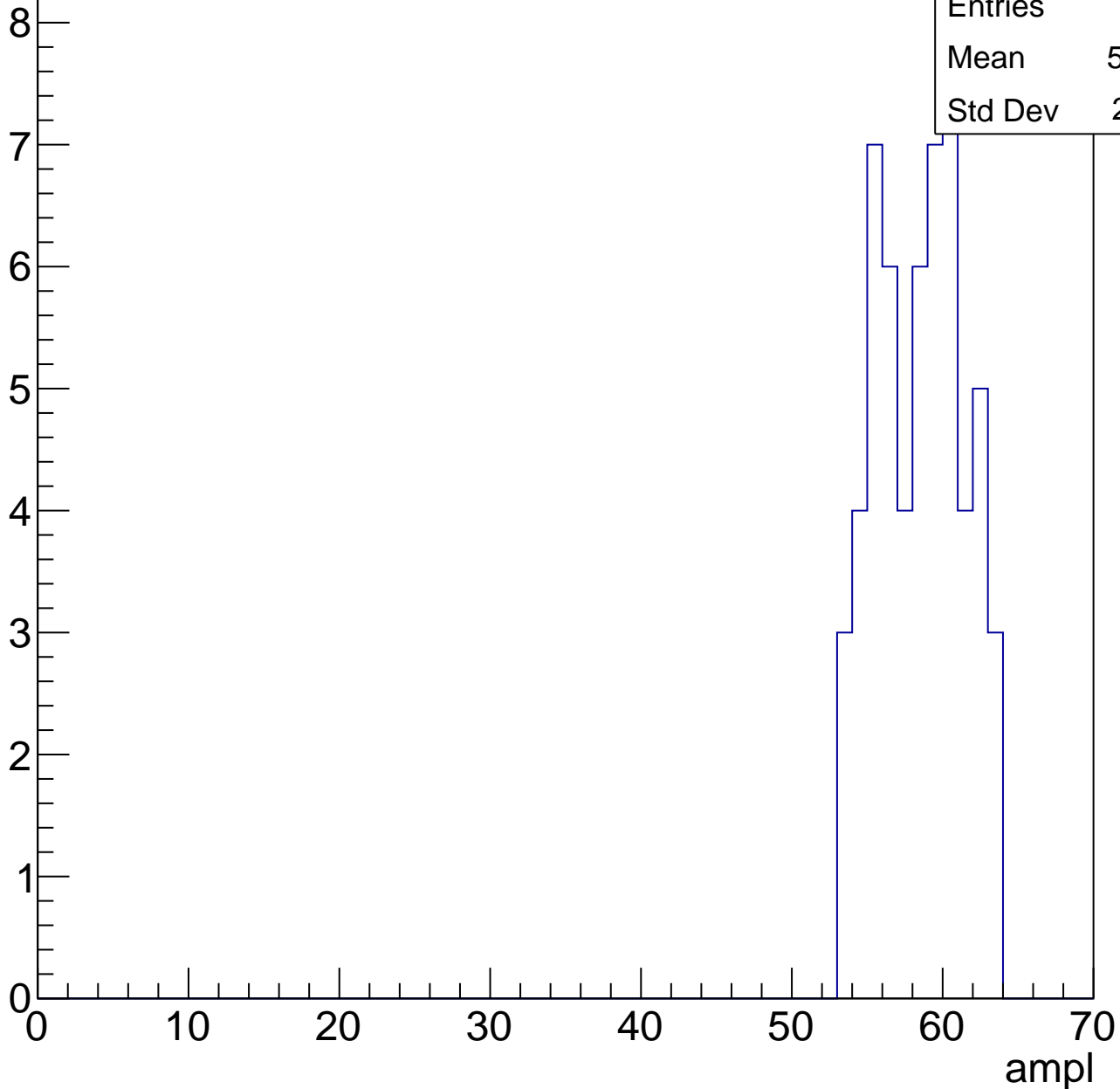


# B1L102S, U3-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	58.04
Std Dev	2.841

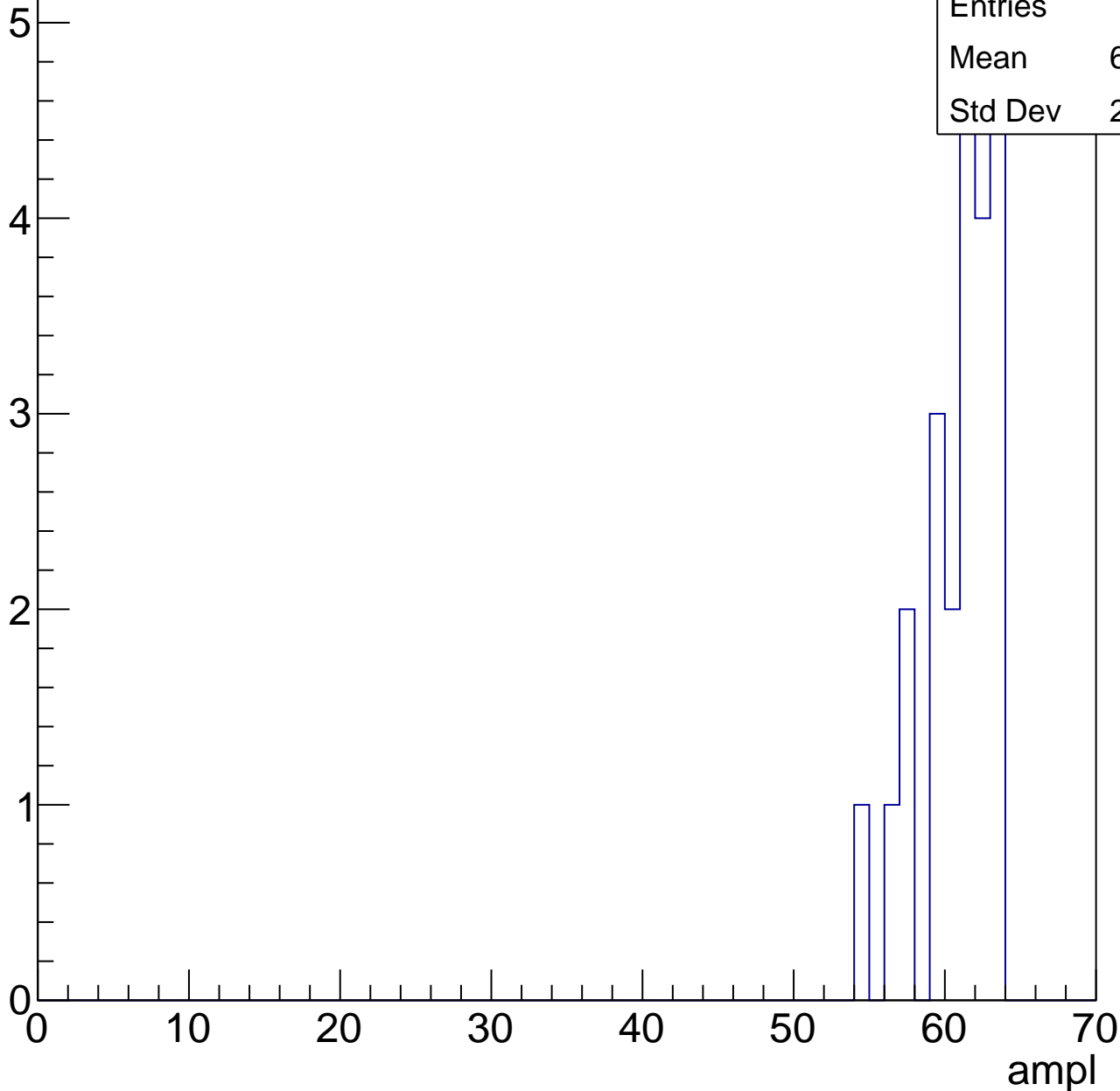


# B1L102S, U3-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	23
Mean	60.39
Std Dev	2.427

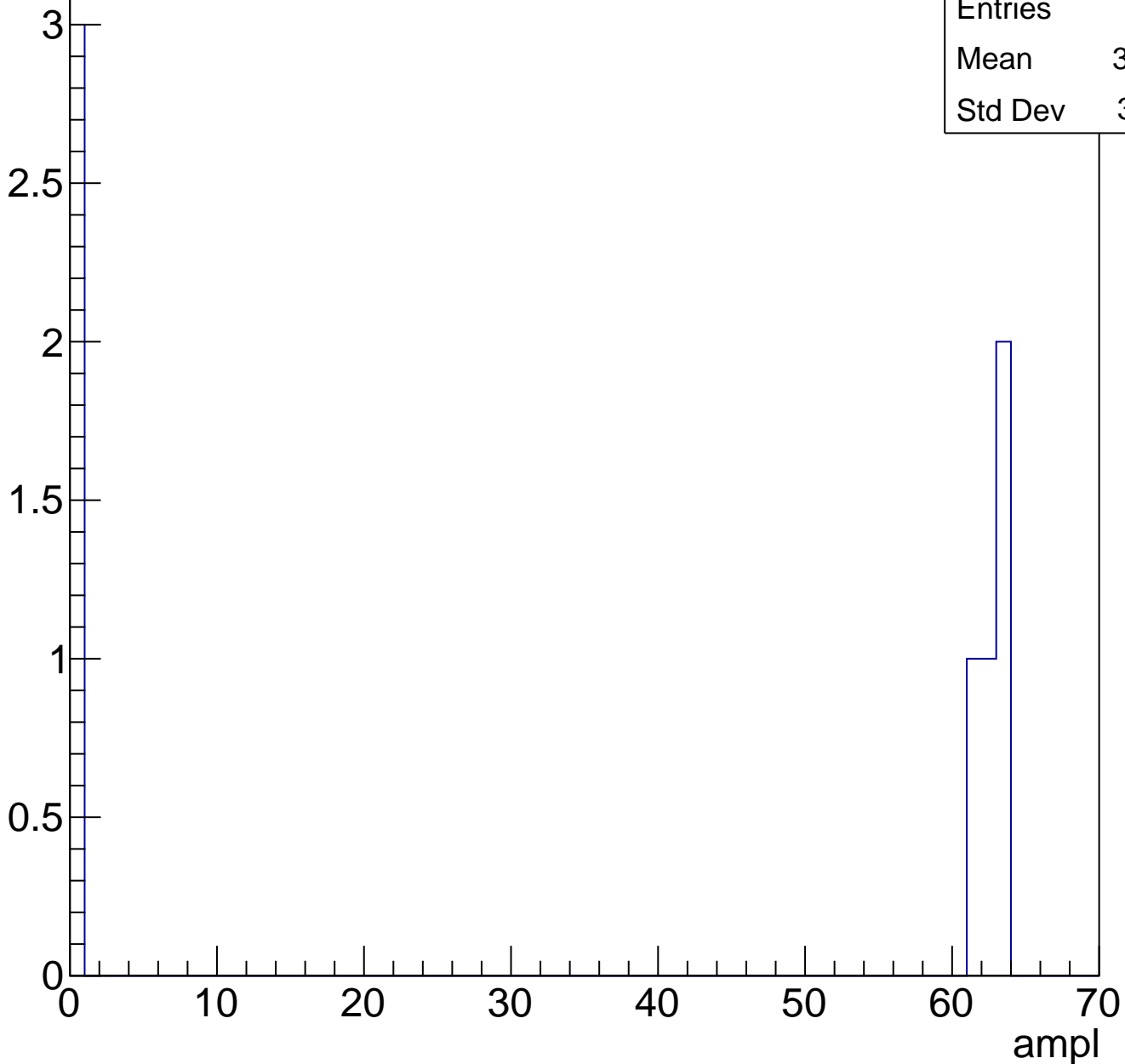




# B1L102S, U3-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch77, adc0

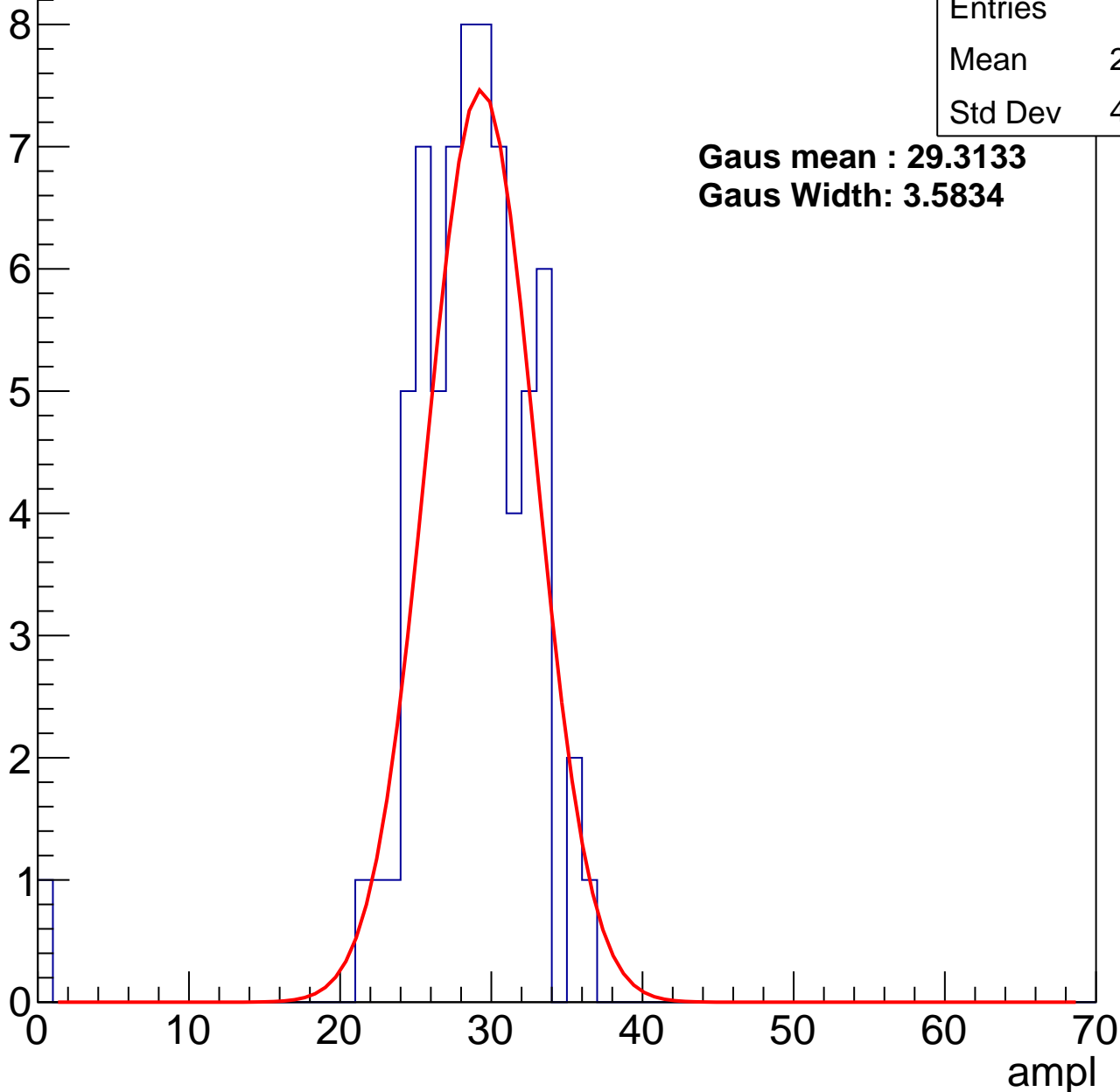
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	28.03
Std Dev	4.706

**Gaus mean : 29.3133**

**Gaus Width: 3.5834**



# B1L102S, U3-ch77, adc1

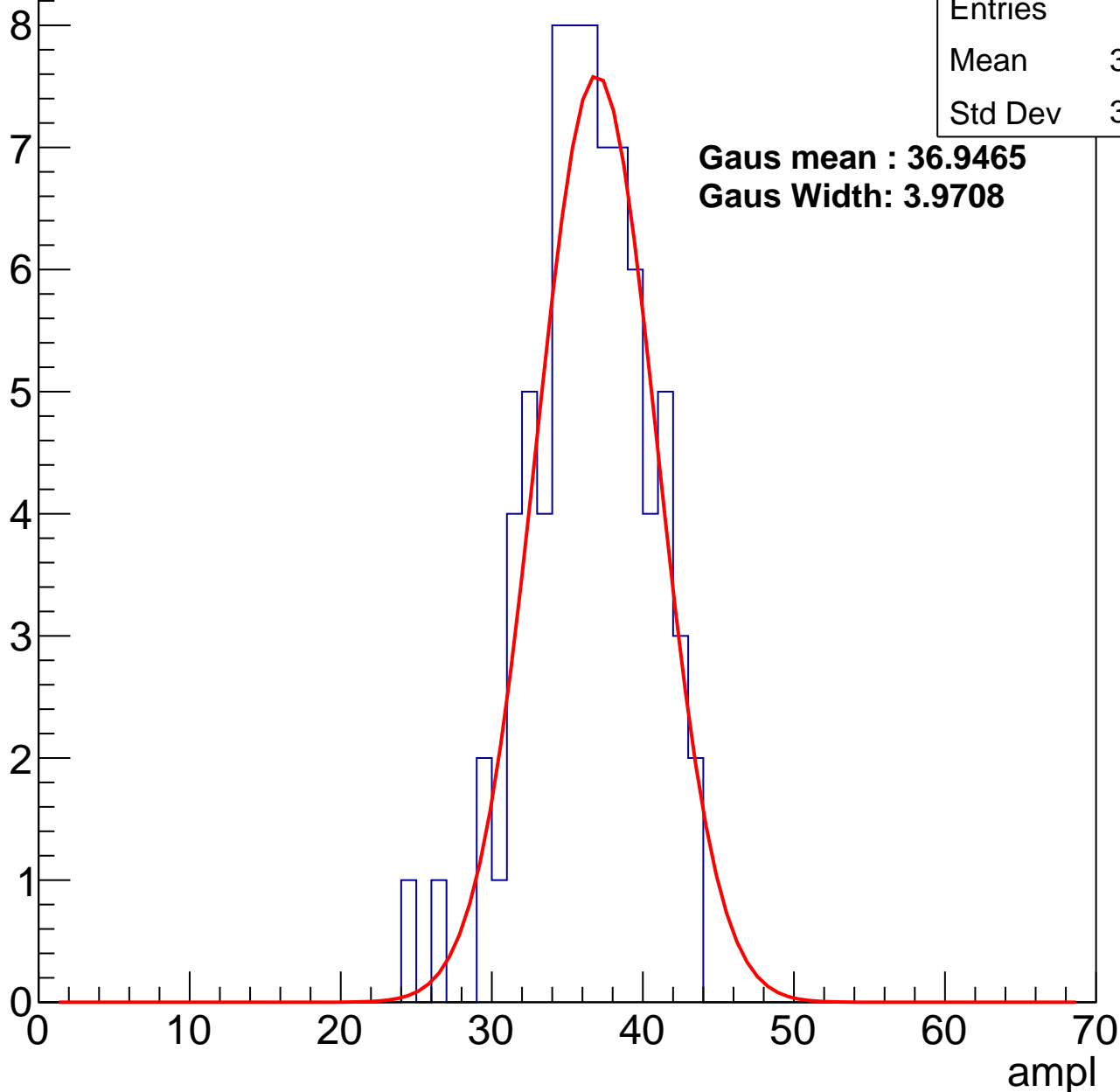
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	35.92
Std Dev	3.835

**Gaus mean : 36.9465**

**Gaus Width: 3.9708**



# B1L102S, U3-ch77, adc2

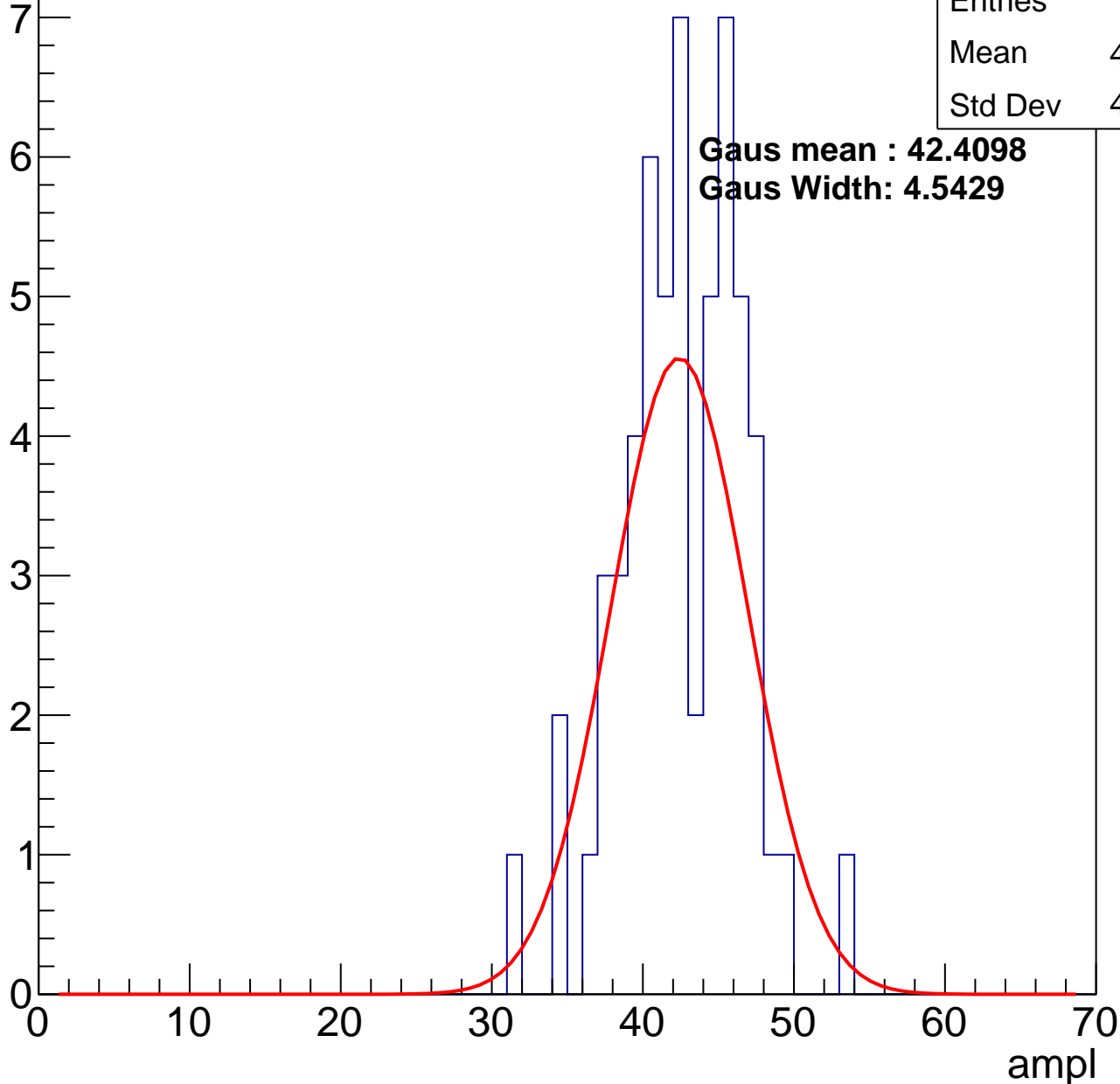
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	42.14
Std Dev	4.032

**Gaus mean : 42.4098**

**Gaus Width: 4.5429**

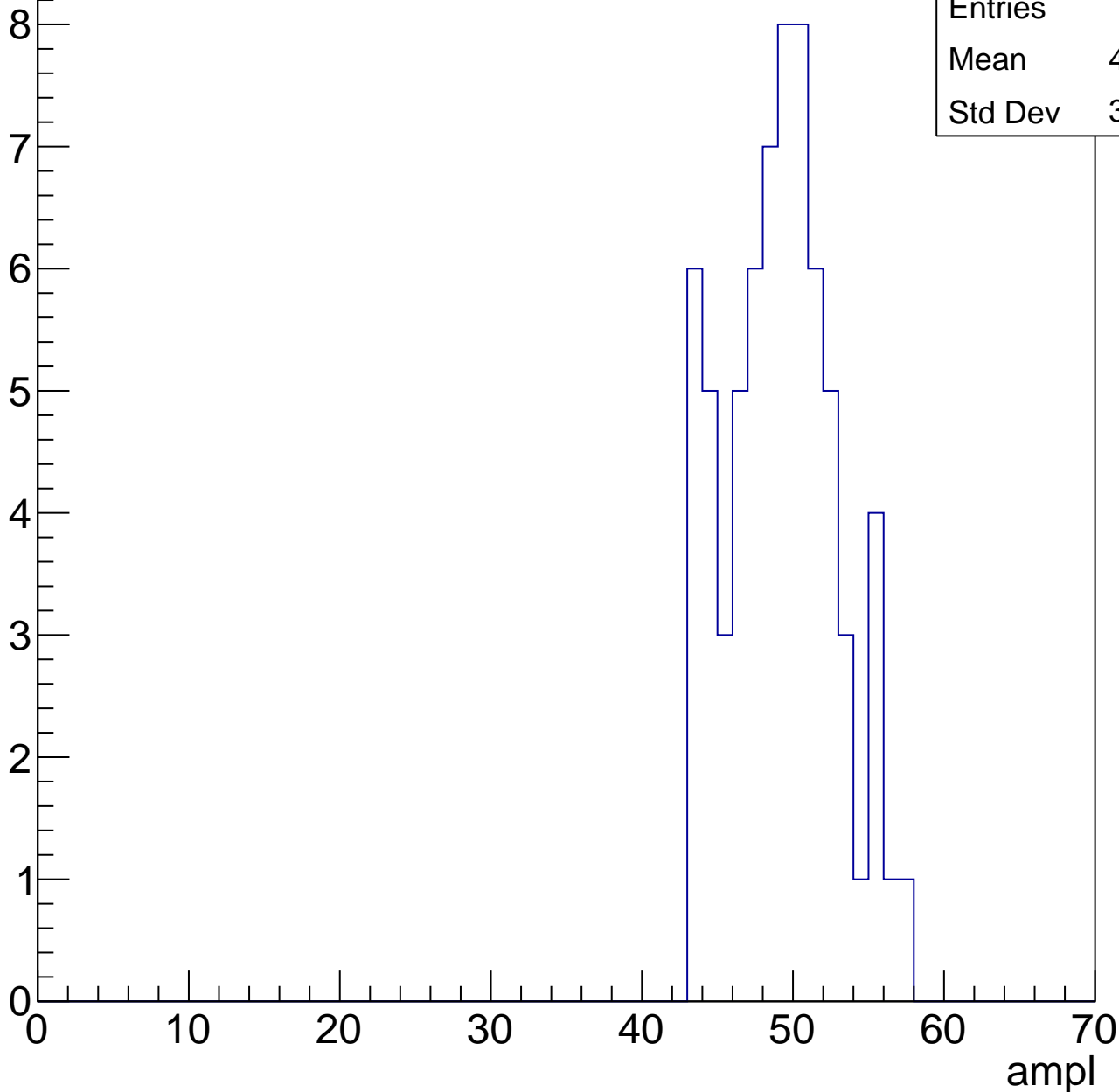


# B1L102S, U3-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

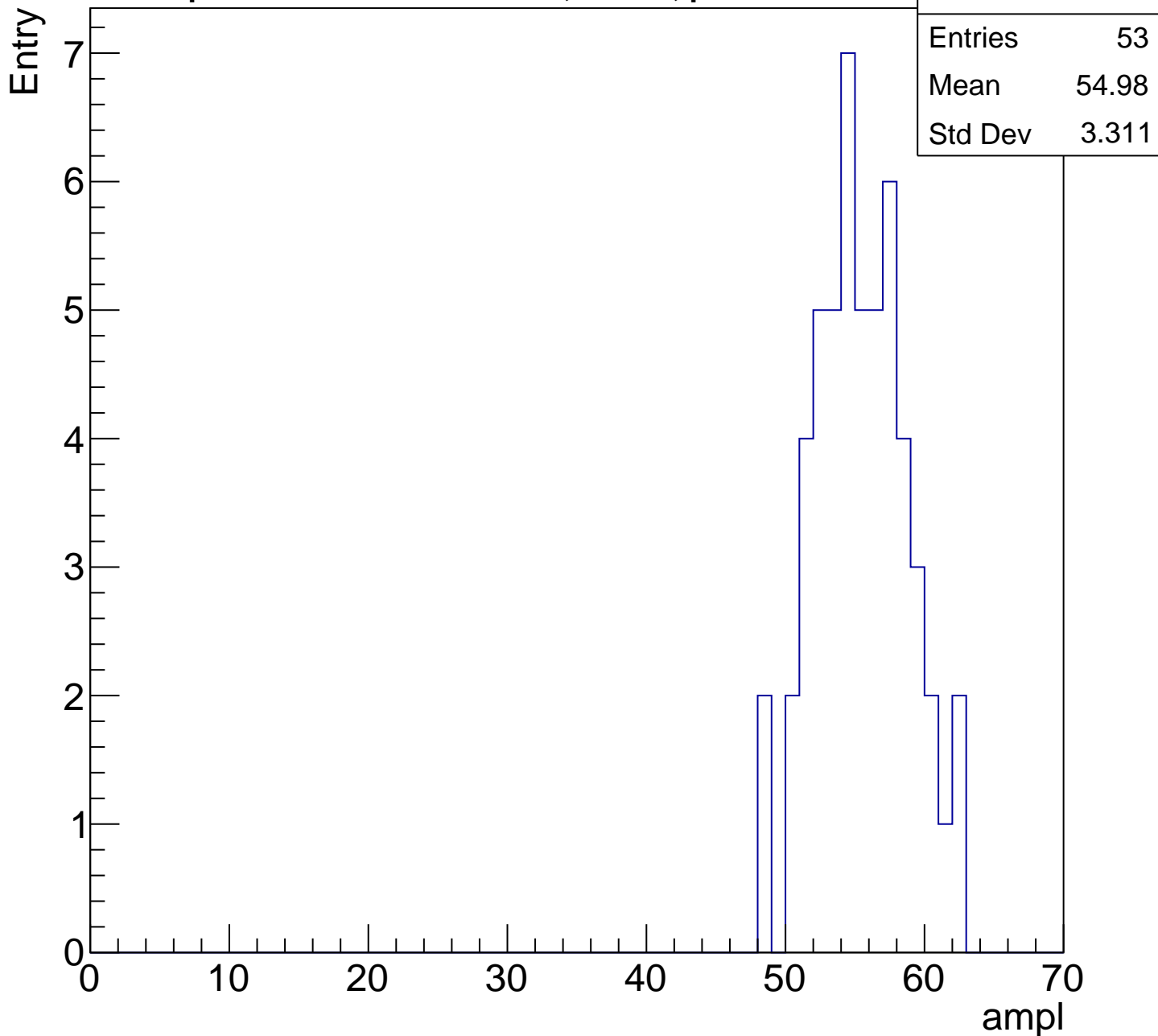
Entry

Entries	69
Mean	48.77
Std Dev	3.547



# B1L102S, U3-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

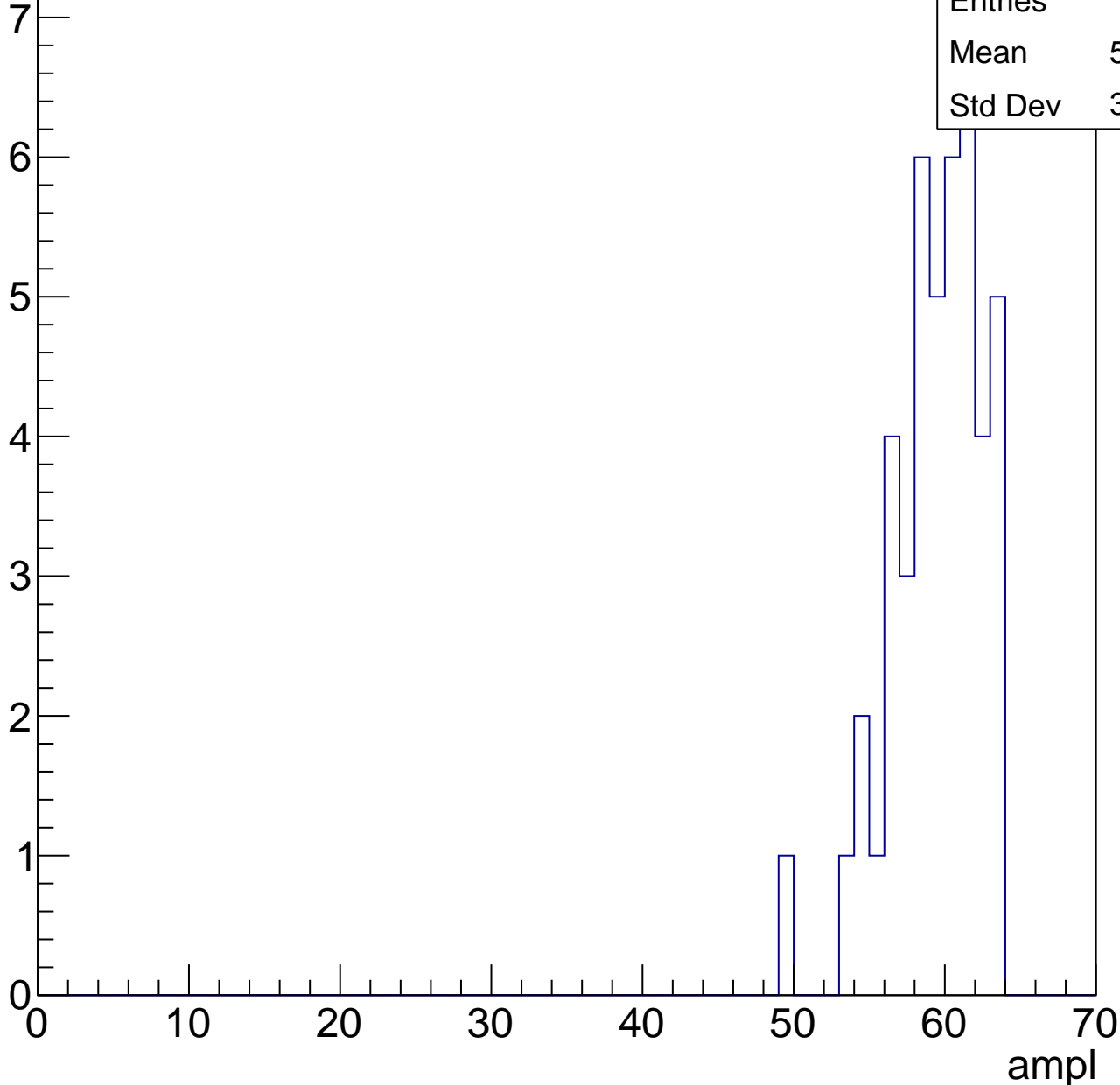


# B1L102S, U3-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	58.96
Std Dev	3.003

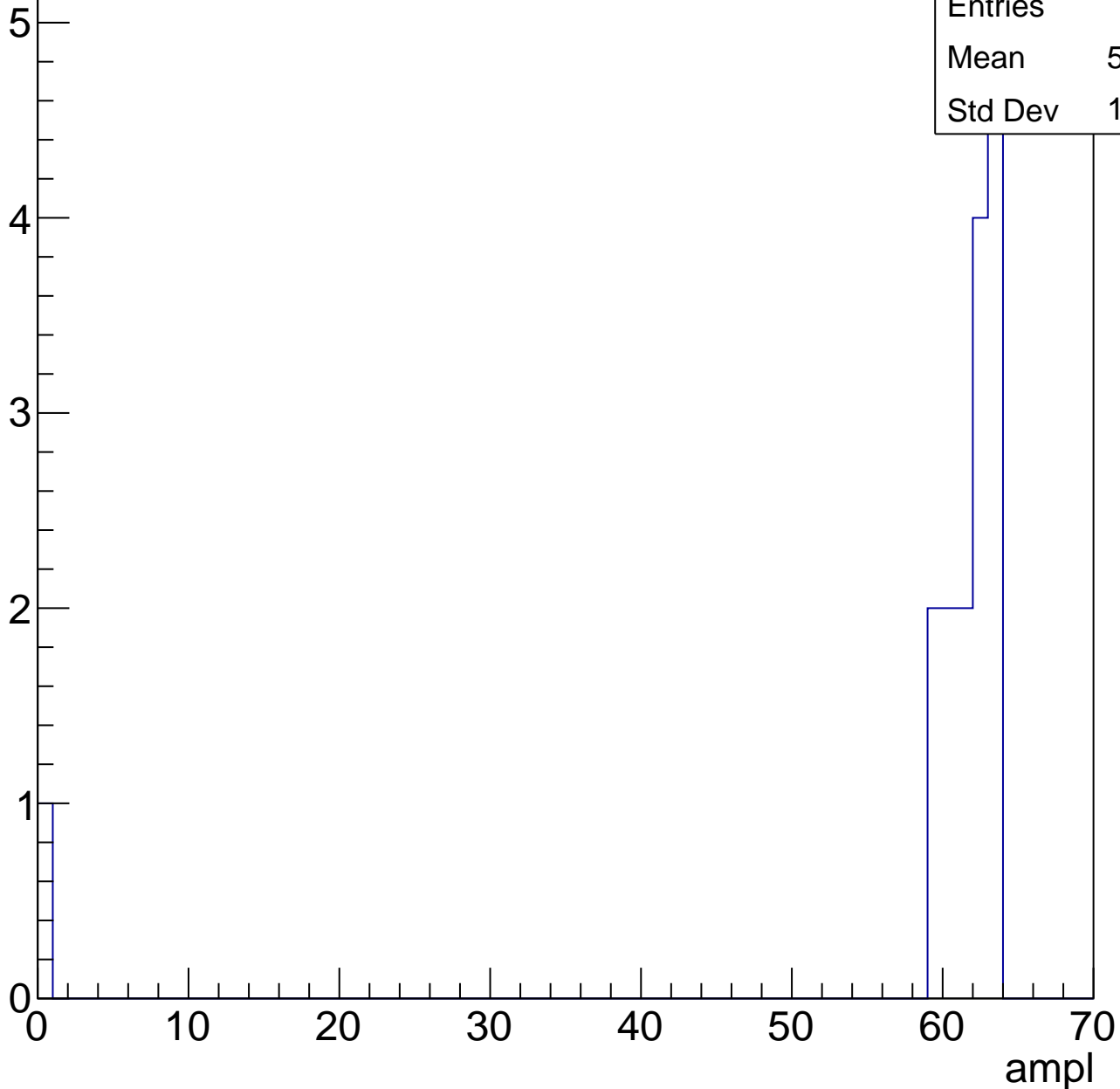


# B1L102S, U3-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	16
Mean	57.69
Std Dev	14.96





# B1L102S, U3-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U3-ch78, adc0

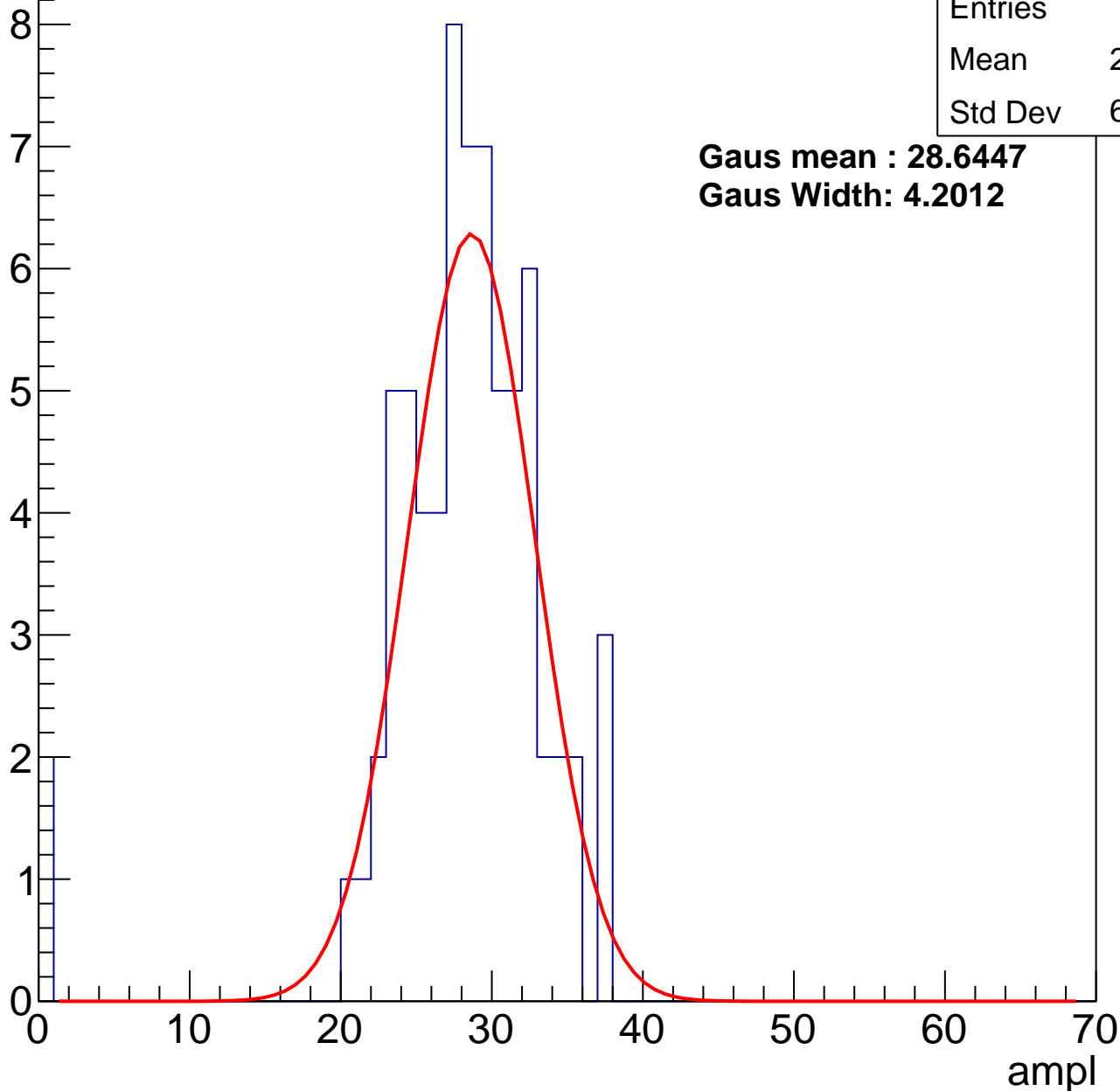
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	27.48
Std Dev	6.086

**Gaus mean : 28.6447**

**Gaus Width: 4.2012**



# B1L102S, U3-ch78, adc1

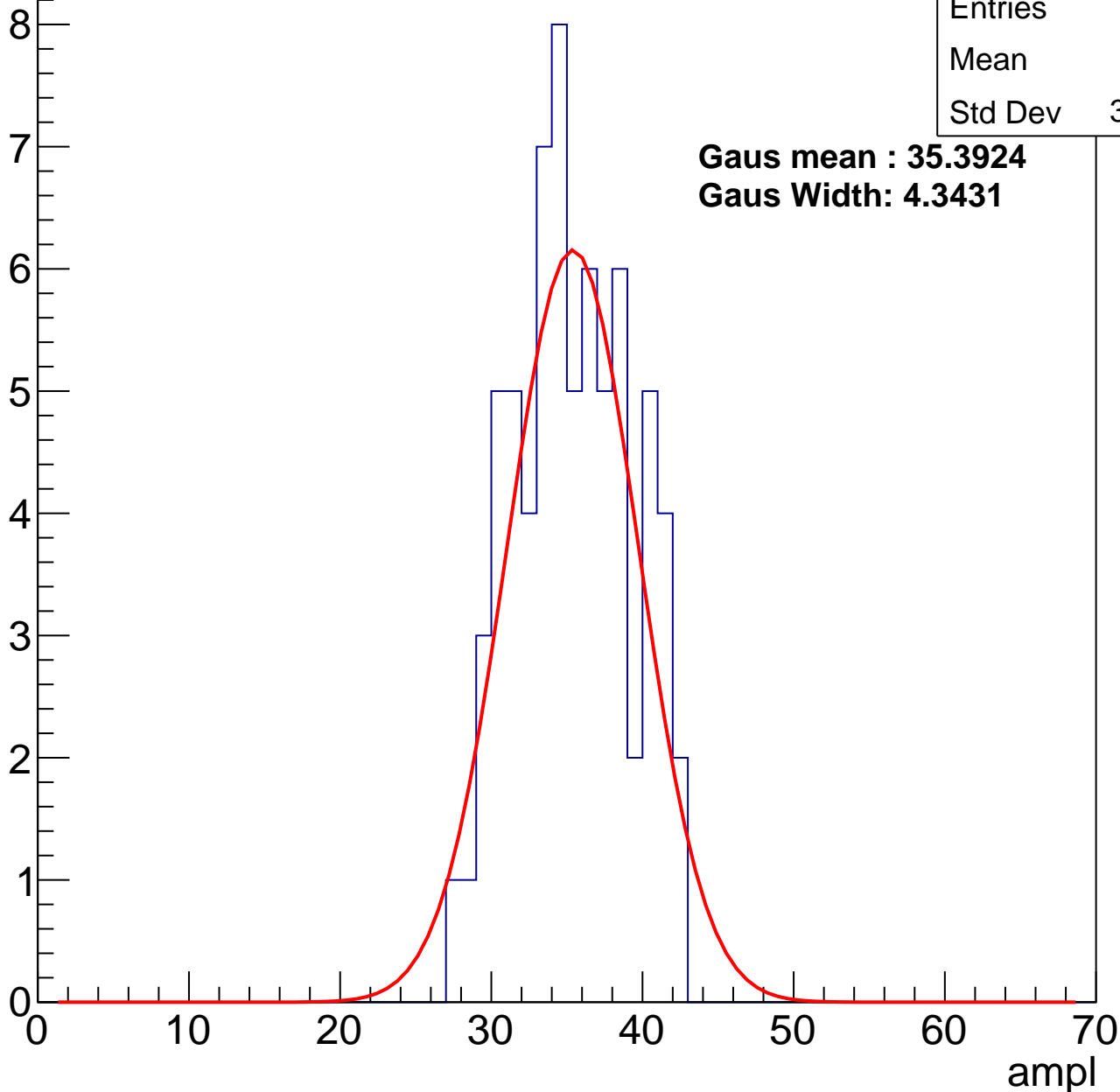
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	34.9
Std Dev	3.762

**Gaus mean : 35.3924**

**Gaus Width: 4.3431**



# B1L102S, U3-ch78, adc2

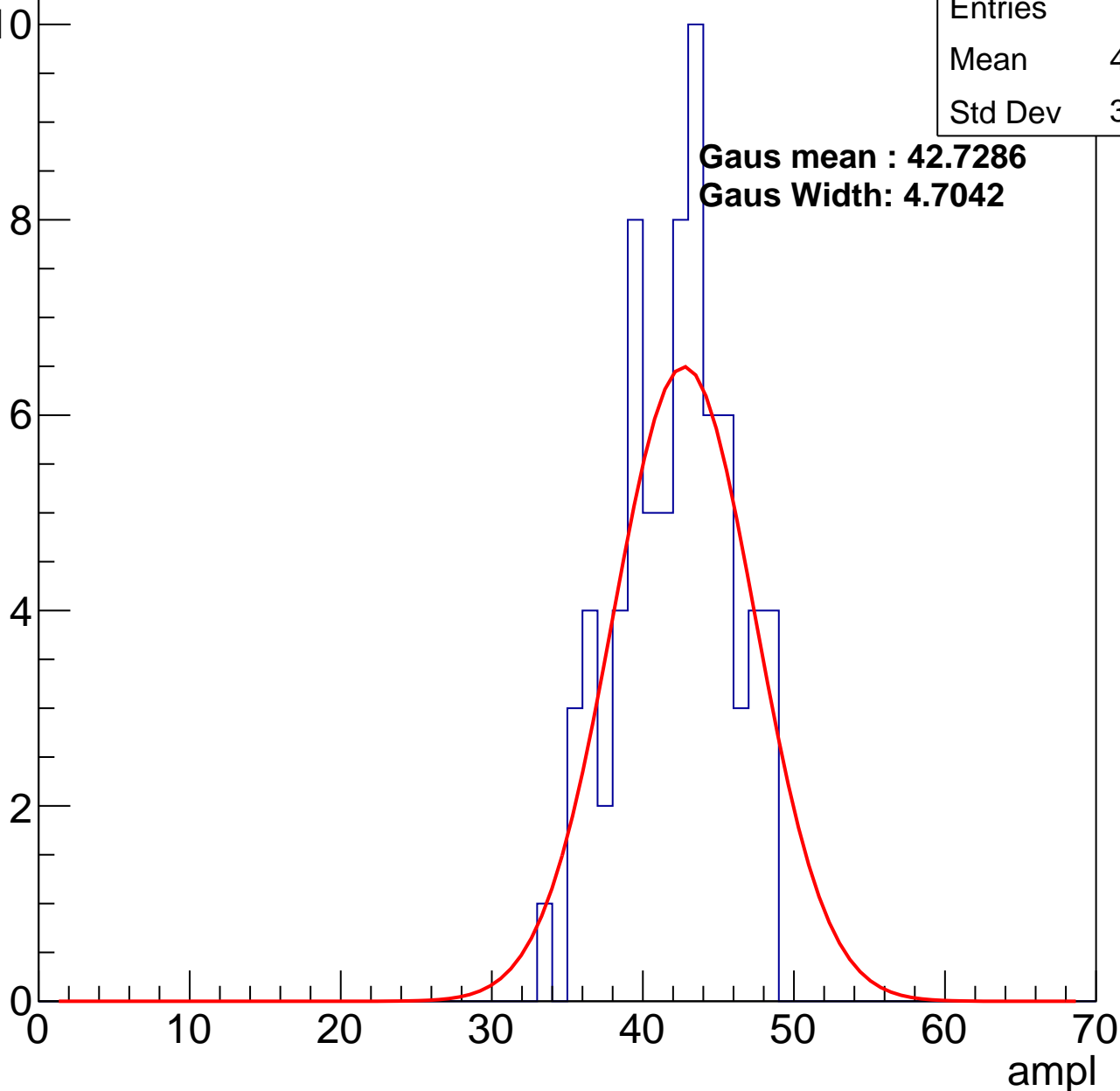
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	41.68
Std Dev	3.618

**Gaus mean : 42.7286**

**Gaus Width: 4.7042**

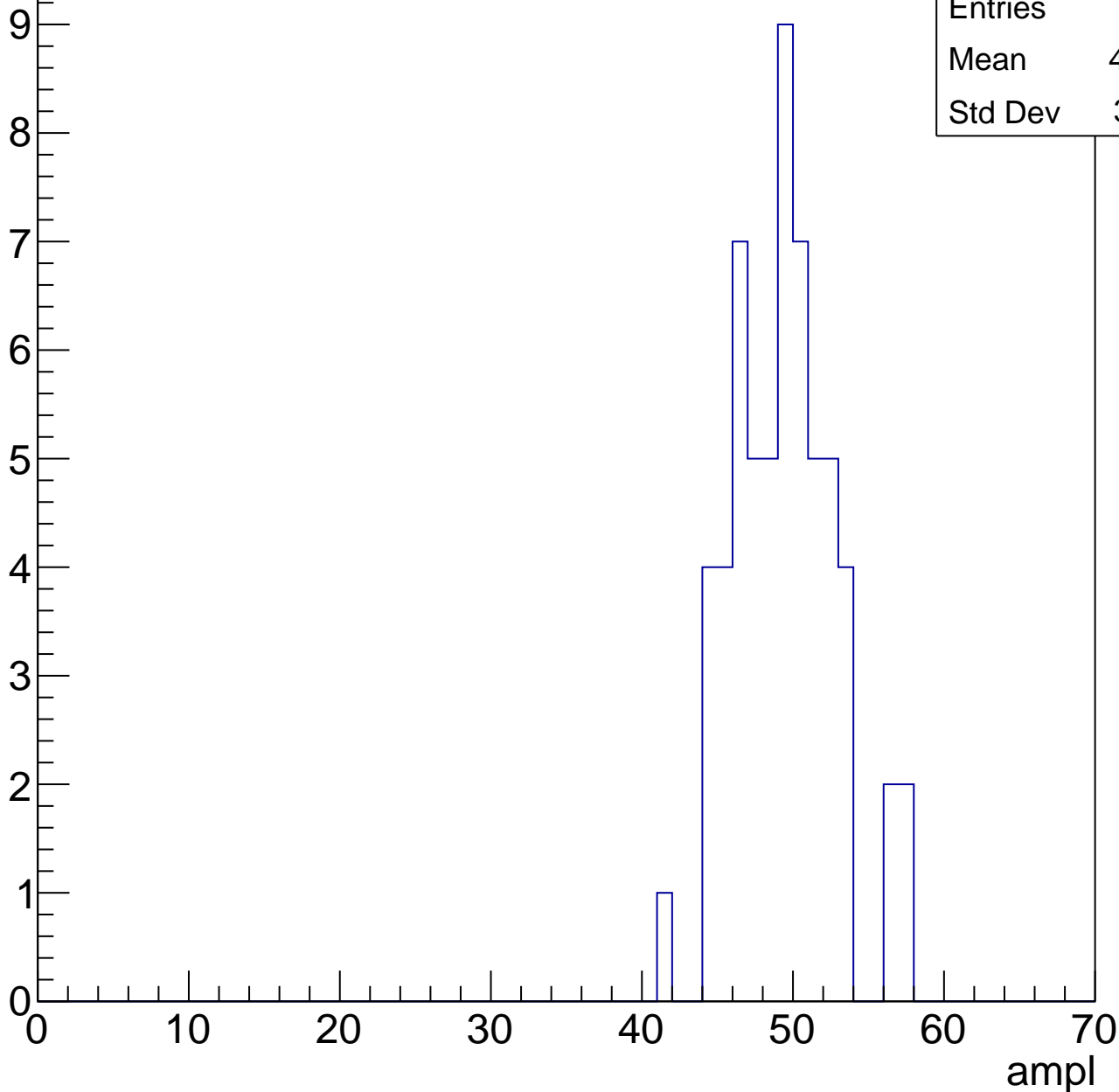


# B1L102S, U3-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	48.97
Std Dev	3.361

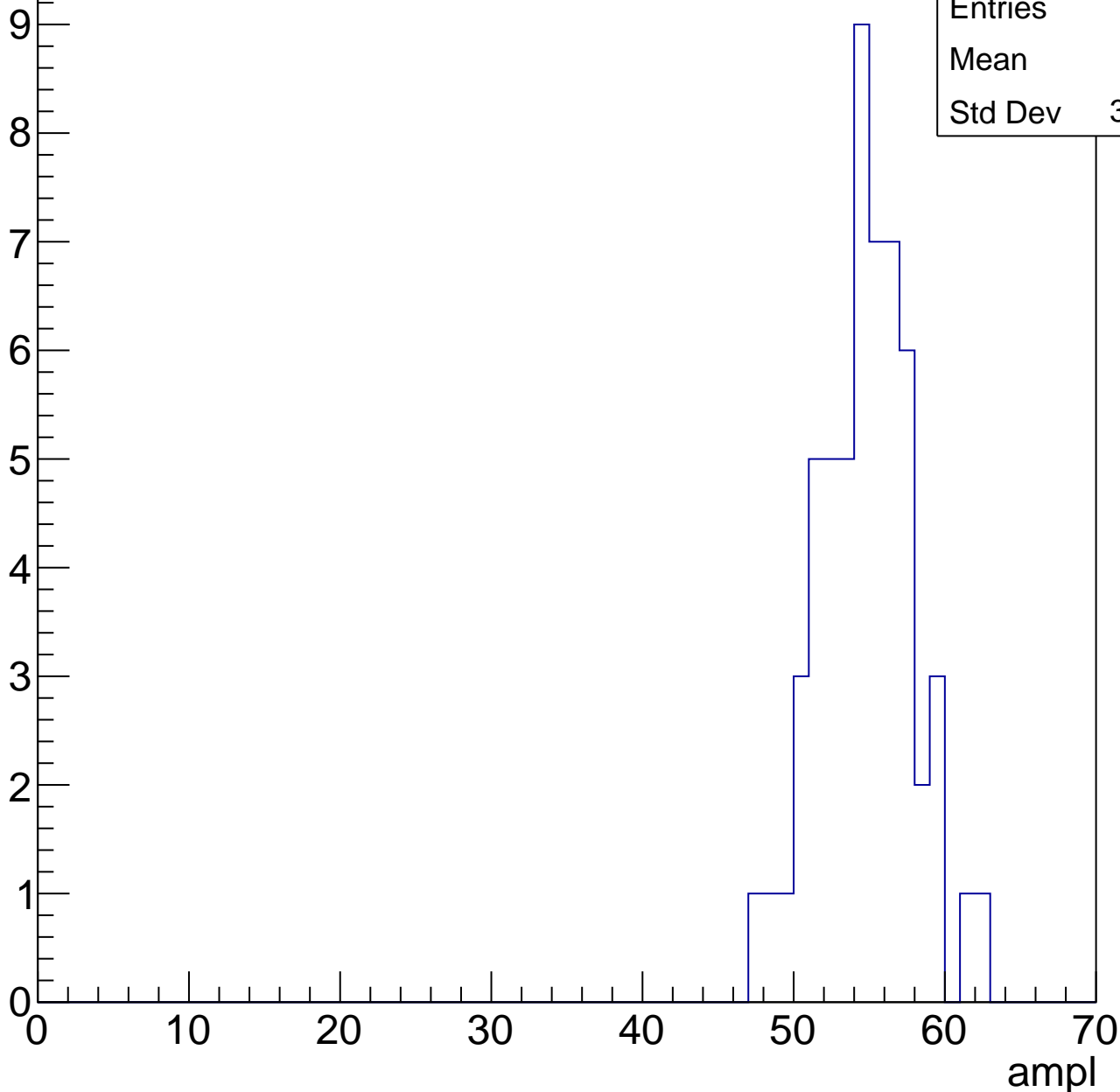


# B1L102S, U3-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	54.3
Std Dev	3.055



# B1L102S, U3-ch78, adc5

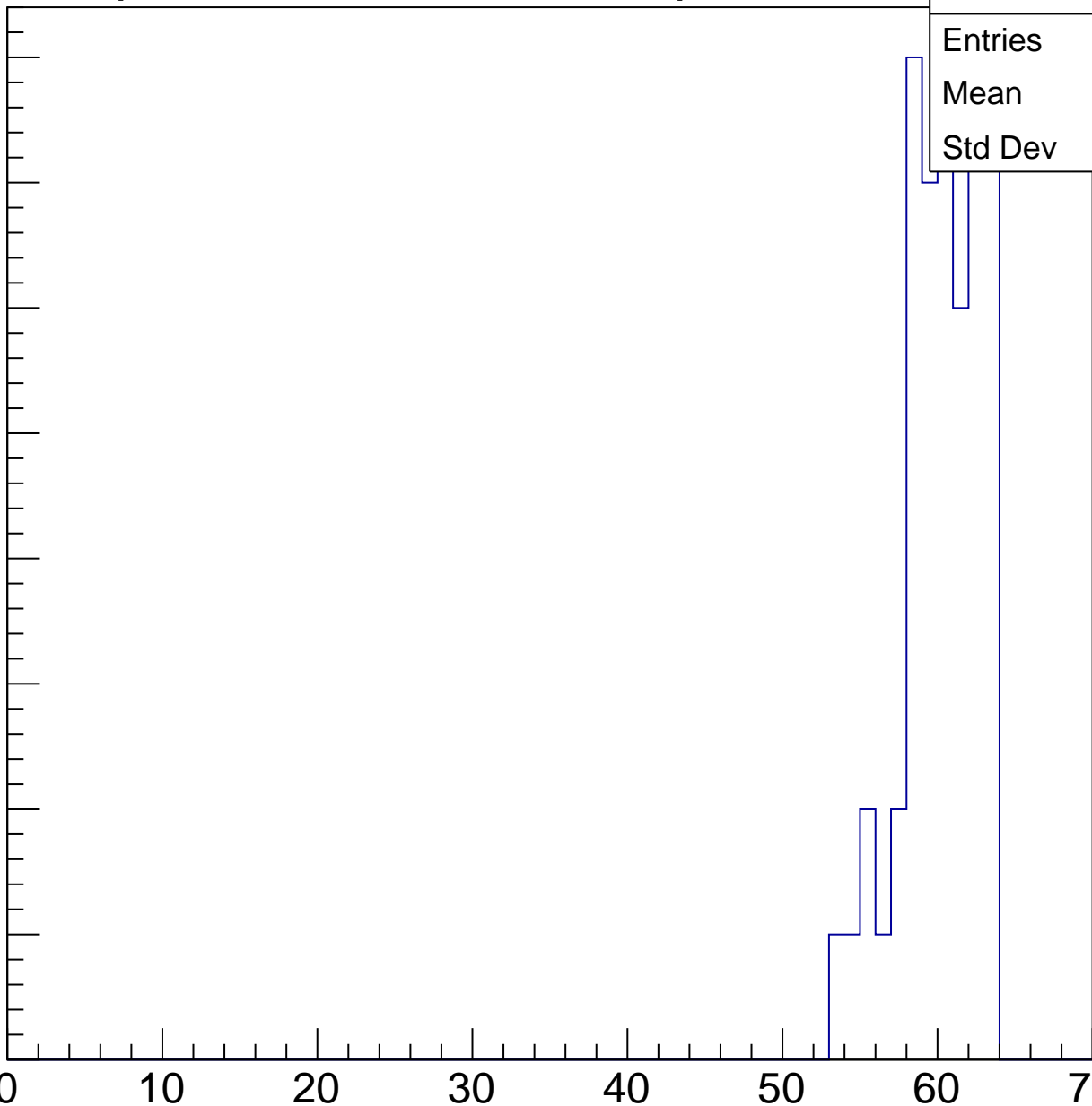
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	52
Mean	59.81
Std Dev	2.465

ampl



# B1L102S, U3-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

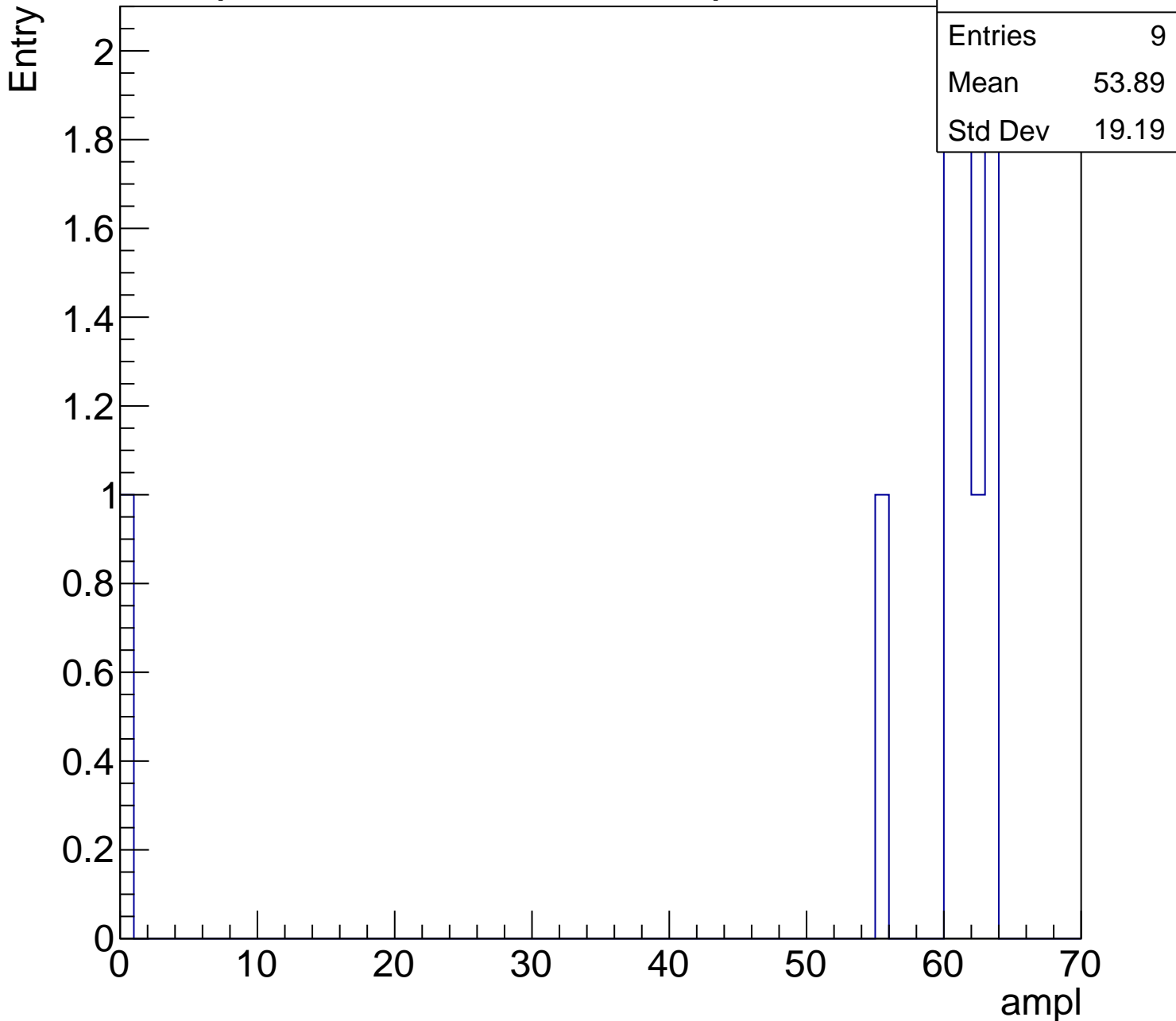
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	9
Mean	53.89
Std Dev	19.19

0 10 20 30 40 50 60 70

ampl





# B1L102S, U3-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch79, adc0

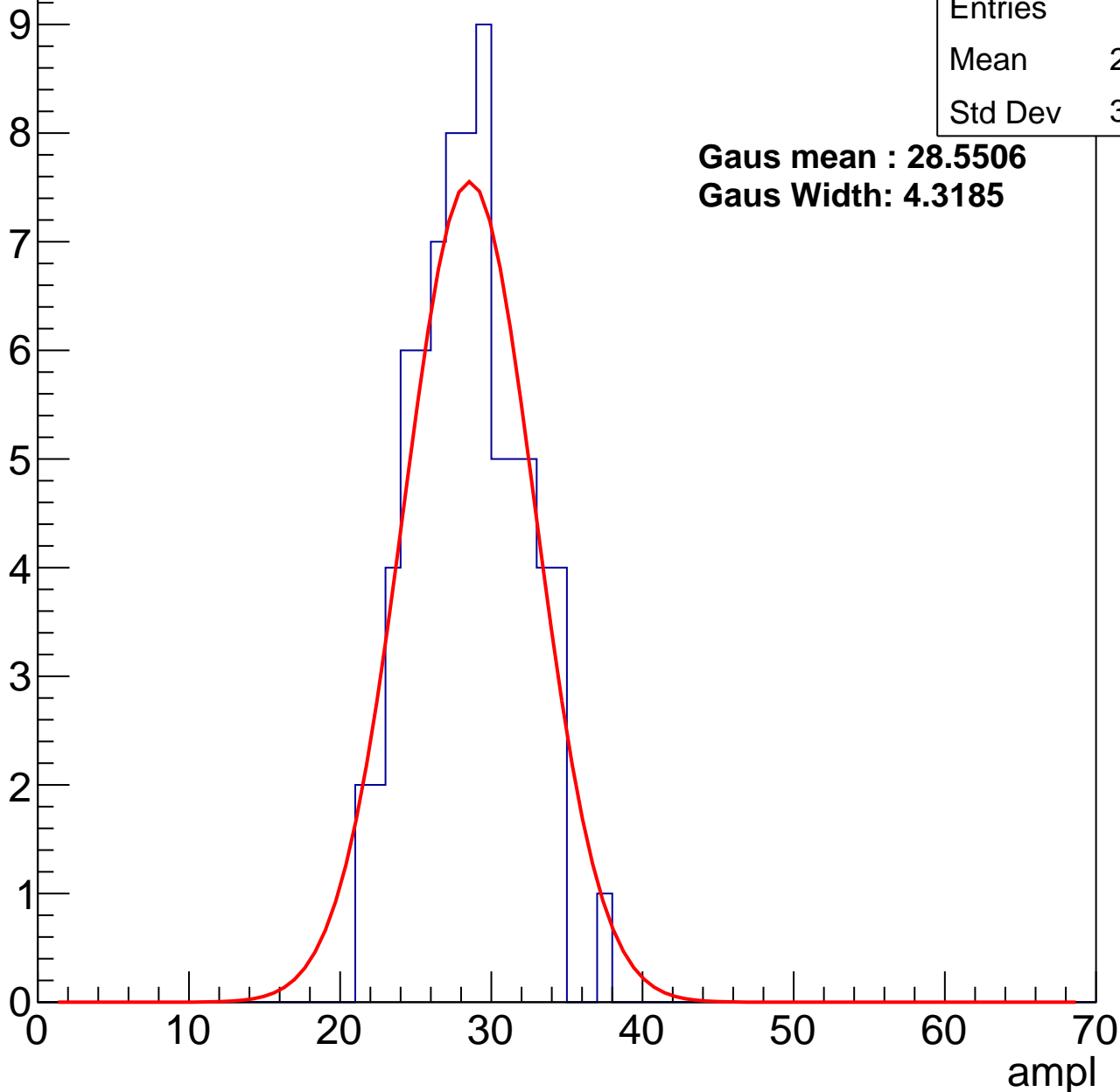
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	27.96
Std Dev	3.507

**Gaus mean : 28.5506**

**Gaus Width: 4.3185**



# B1L102S, U3-ch79, adc1

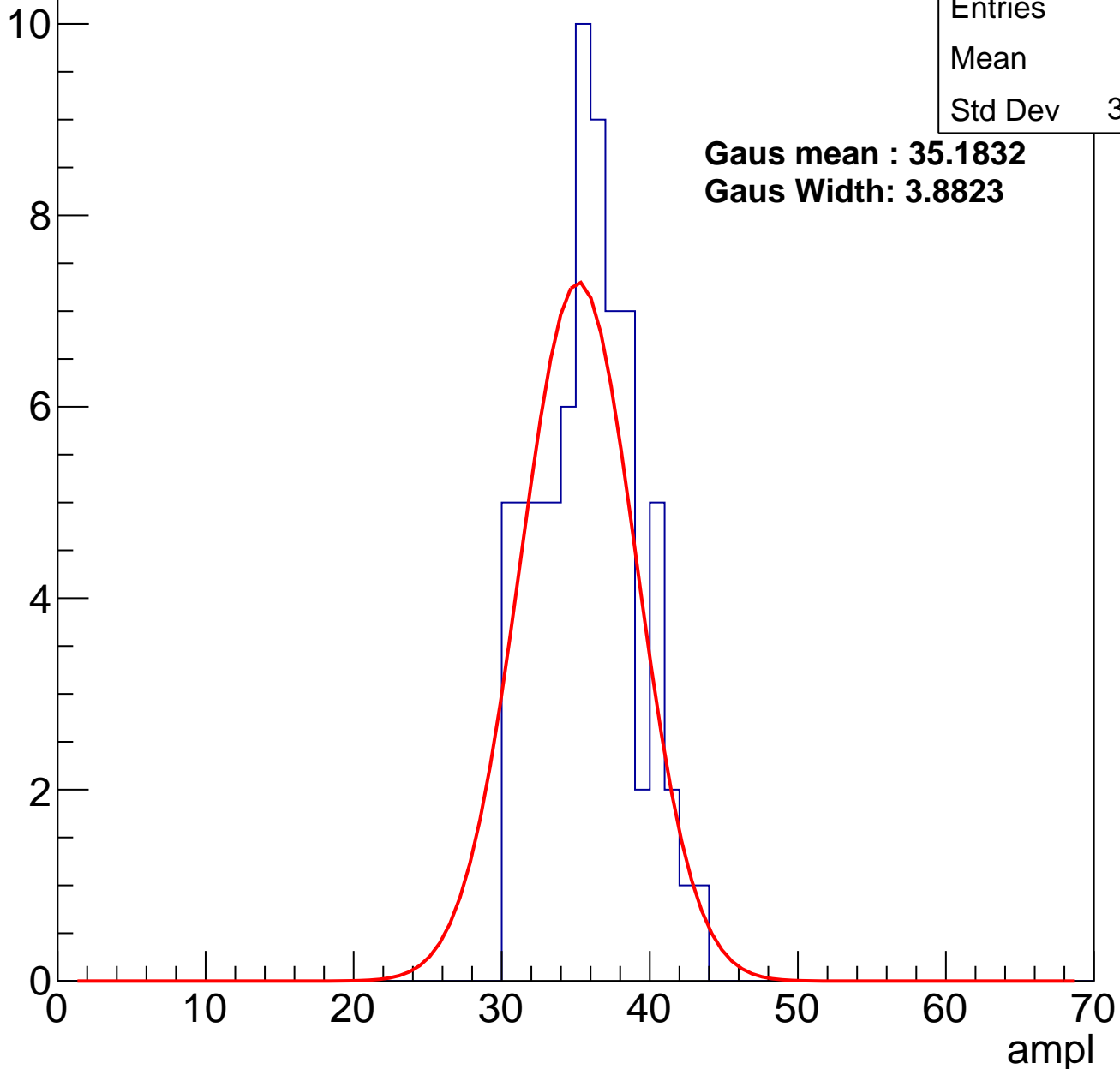
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	70
Mean	35.4
Std Dev	3.178

**Gaus mean : 35.1832**

**Gaus Width: 3.8823**

Entry



# B1L102S, U3-ch79, adc2

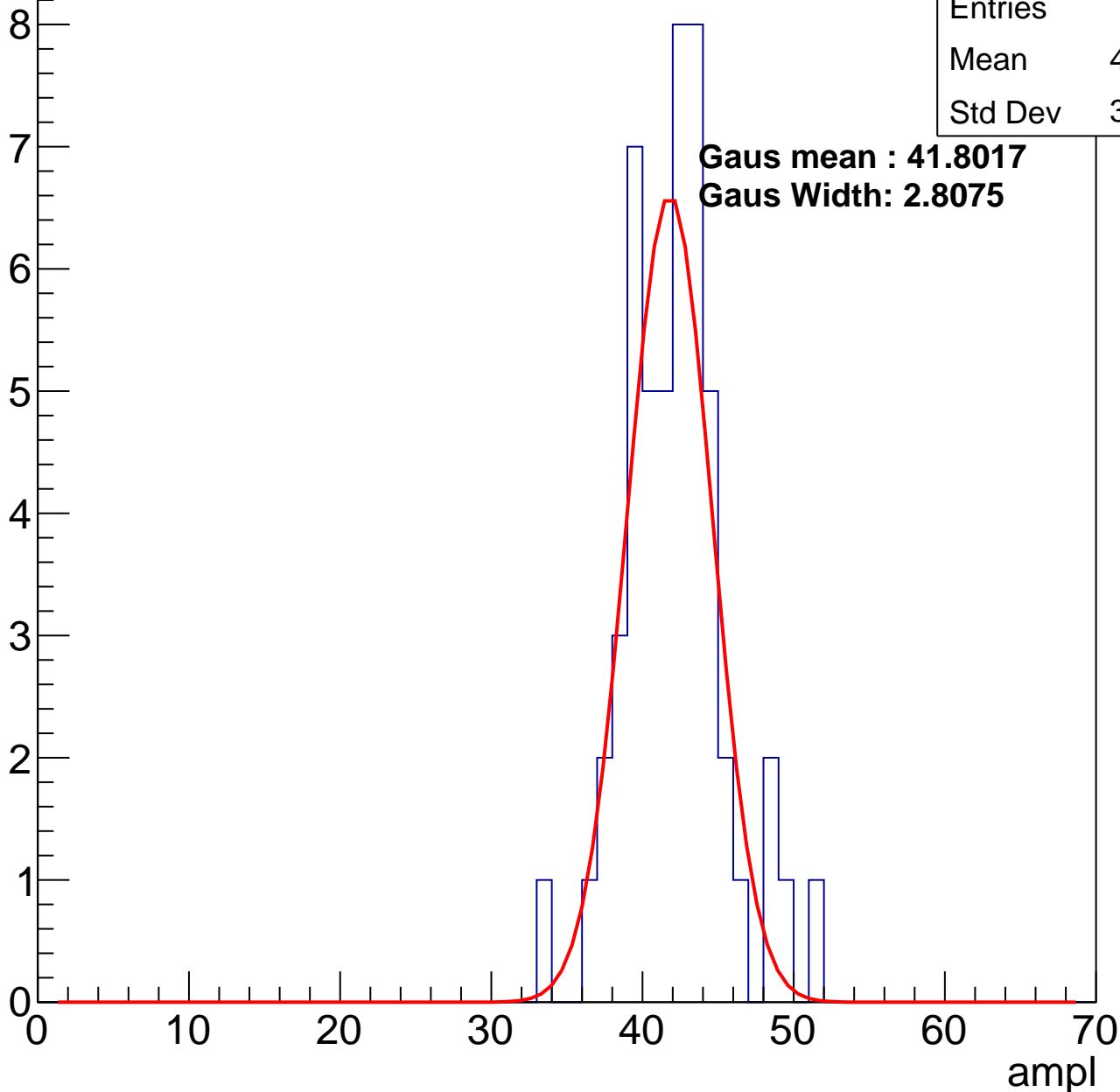
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	41.67
Std Dev	3.286

**Gaus mean : 41.8017**

**Gaus Width: 2.8075**

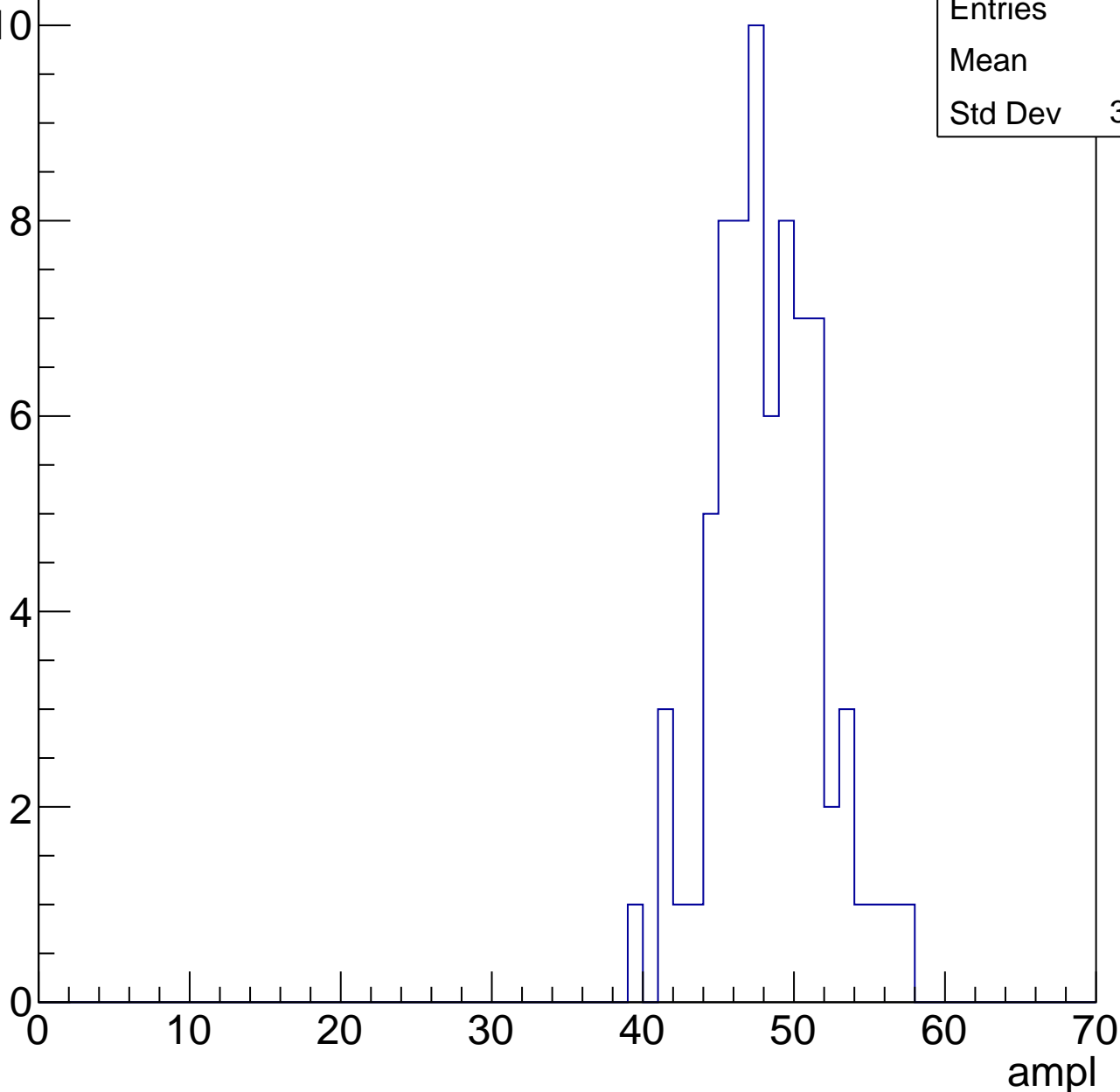


# B1L102S, U3-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	47.8
Std Dev	3.518

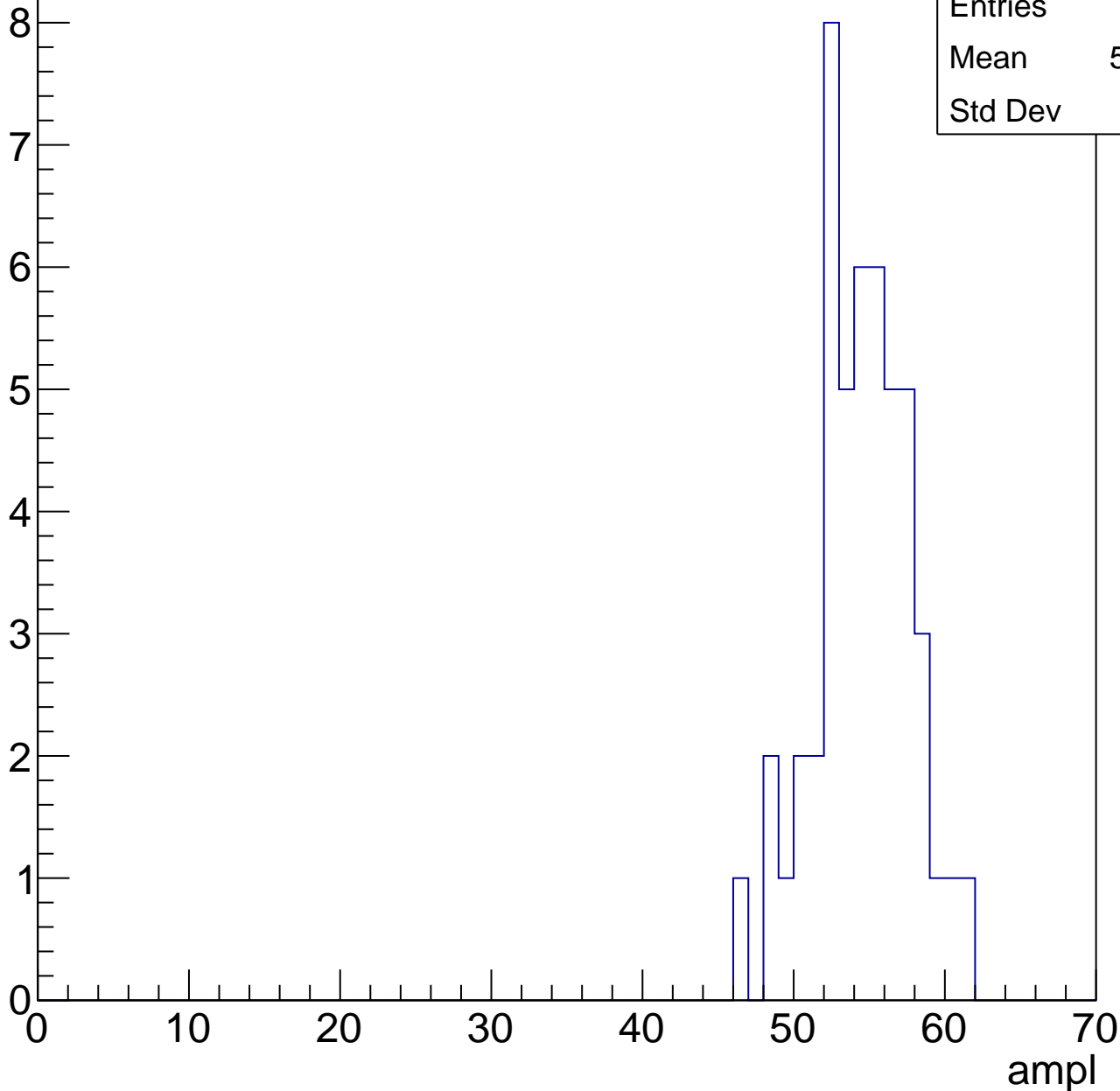


# B1L102S, U3-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

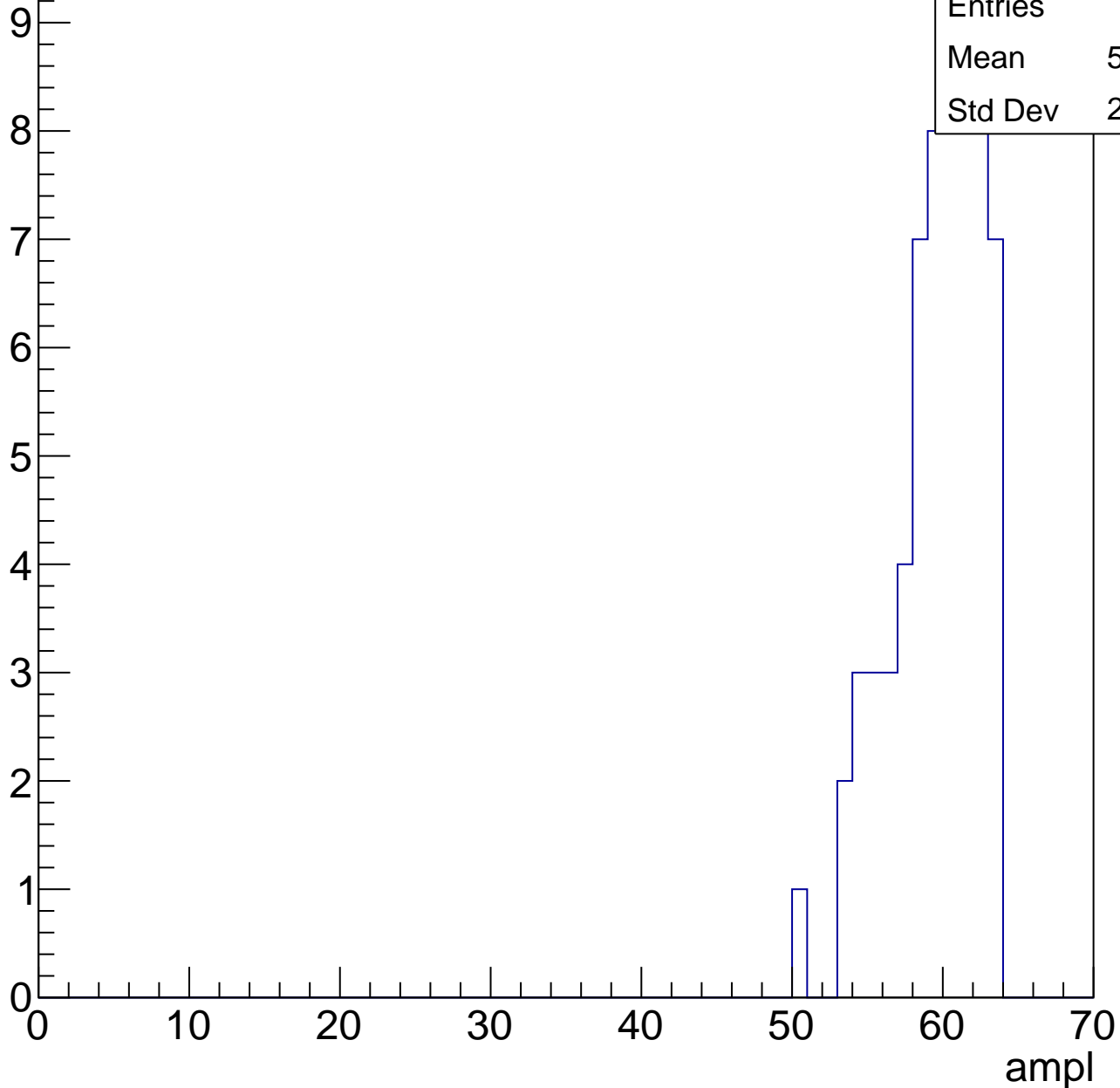
Entries	49
Mean	54.02
Std Dev	3.12



# B1L102S, U3-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

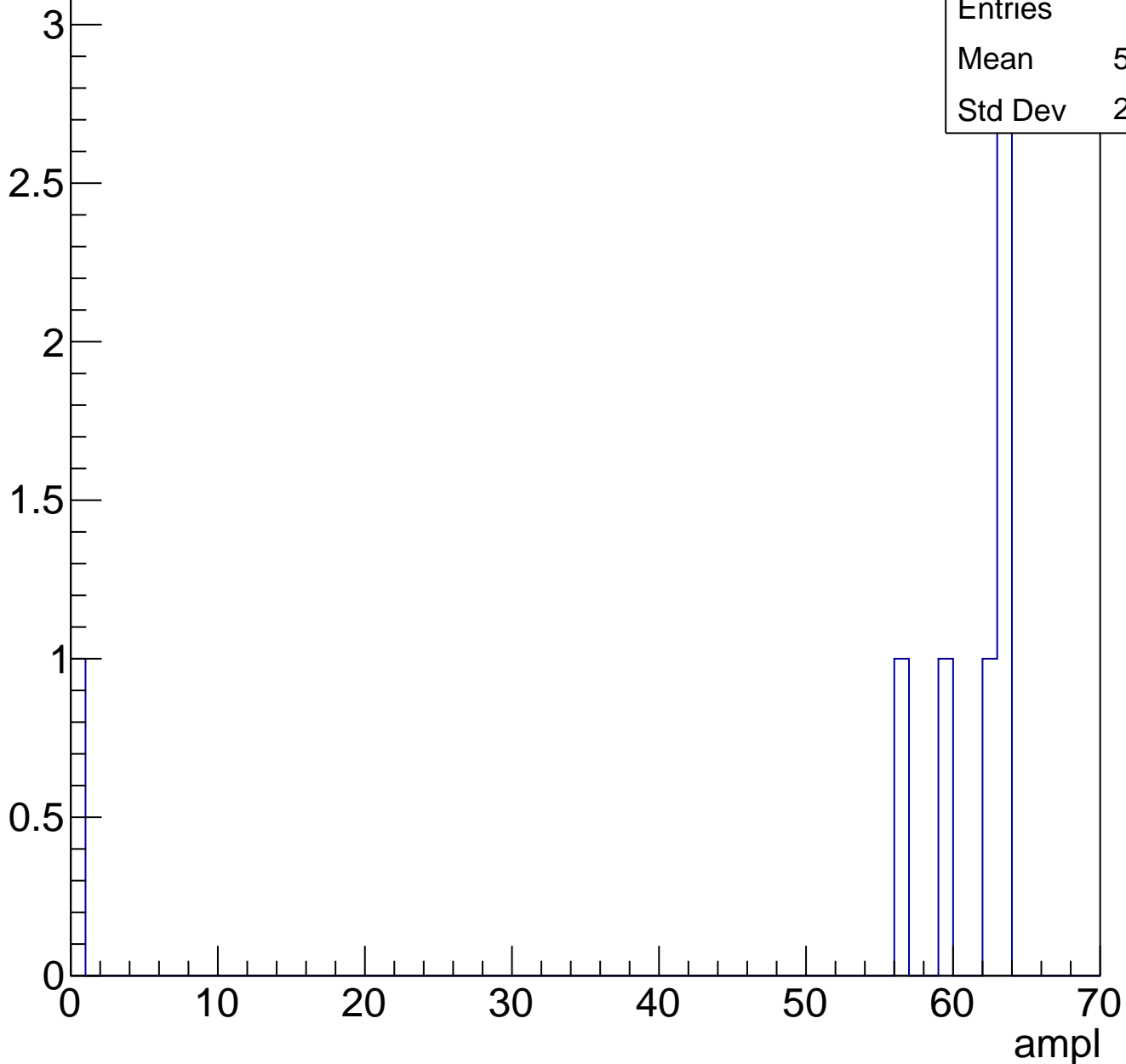
Entry



# B1L102S, U3-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U3-ch80, adc0

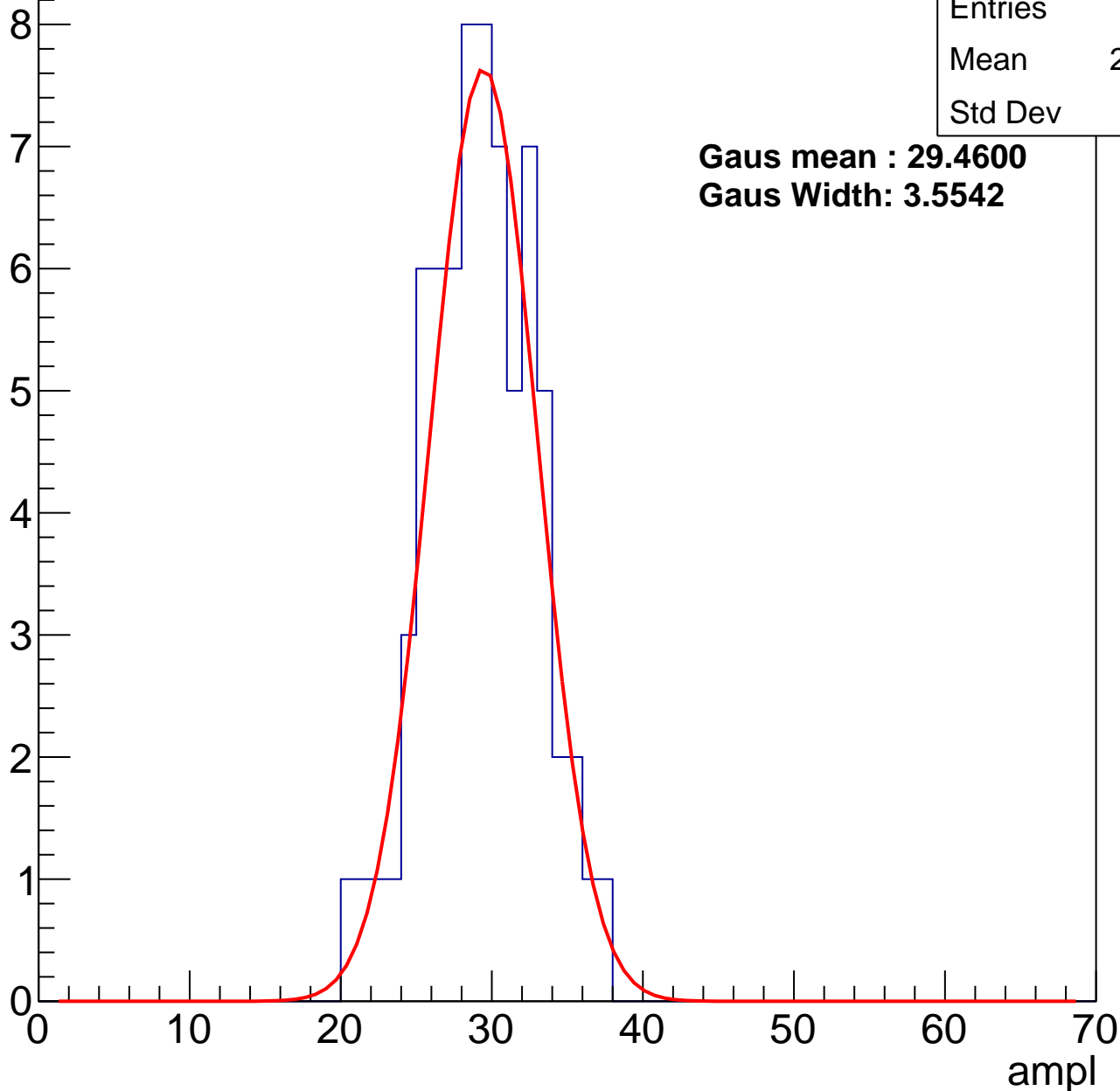
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	28.83
Std Dev	3.54

**Gaus mean : 29.4600**

**Gaus Width: 3.5542**



# B1L102S, U3-ch80, adc1

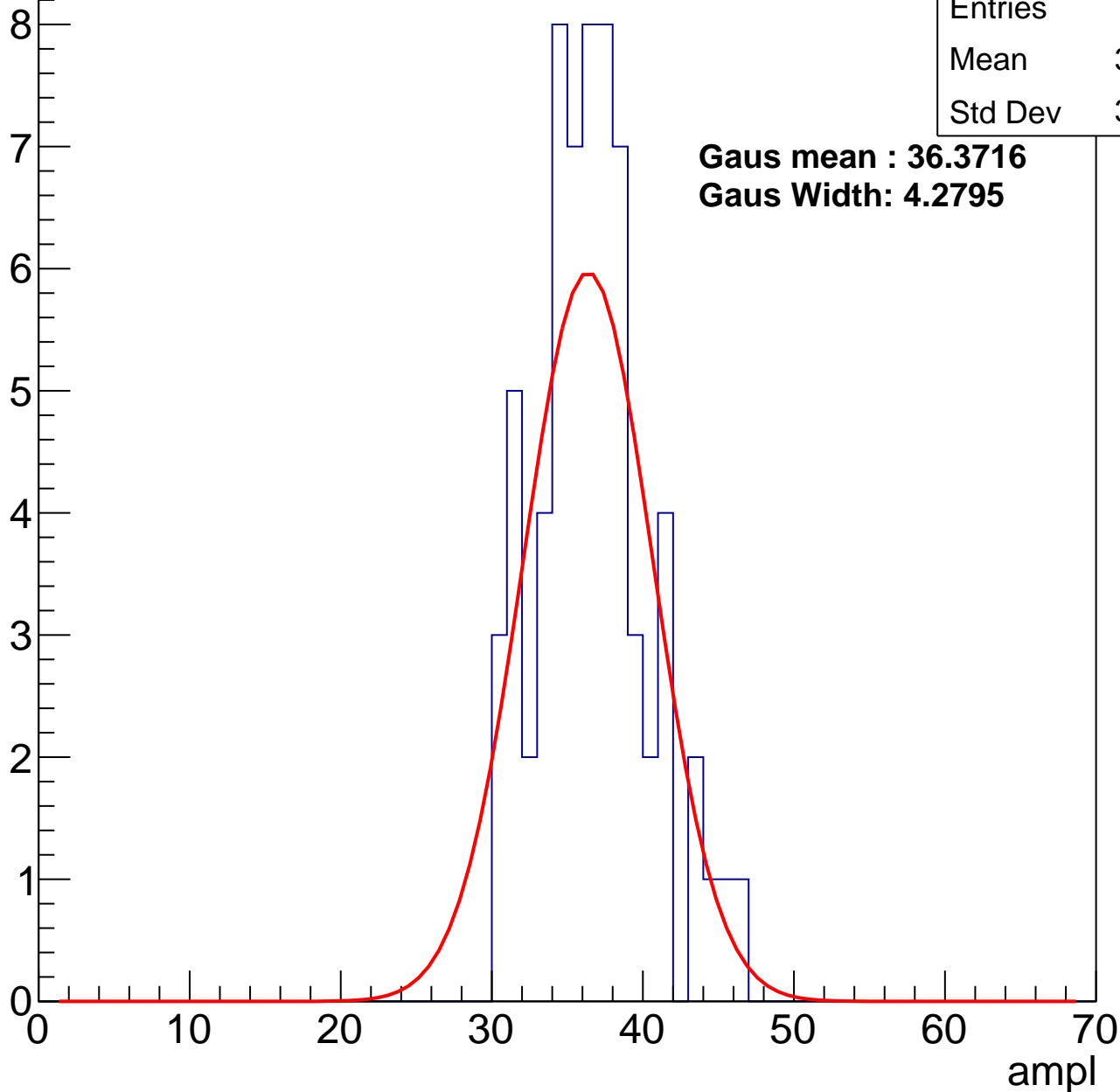
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	36.21
Std Dev	3.641

**Gaus mean : 36.3716**

**Gaus Width: 4.2795**



# B1L102S, U3-ch80, adc2

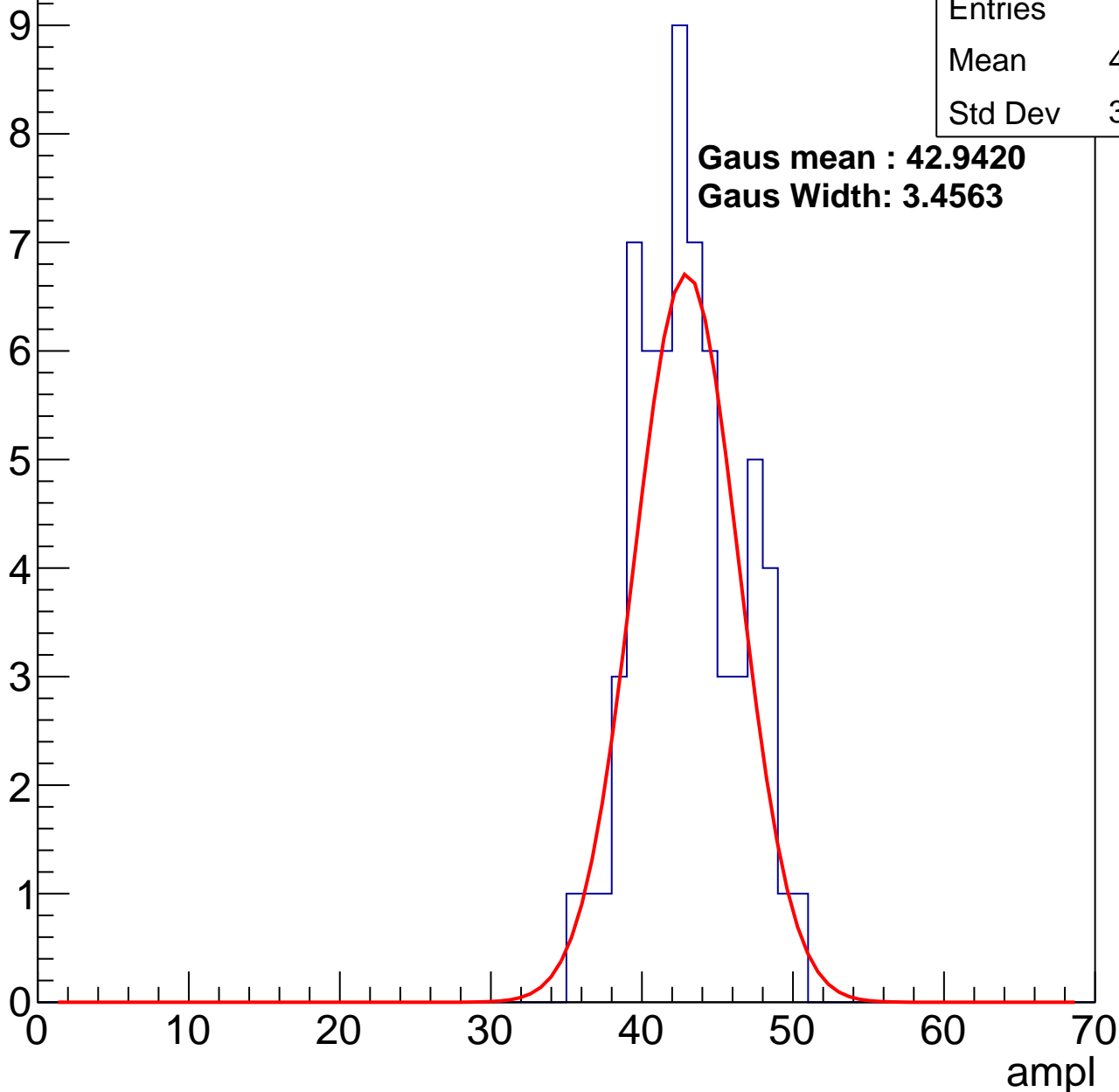
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	42.55
Std Dev	3.354

**Gaus mean : 42.9420**

**Gaus Width: 3.4563**

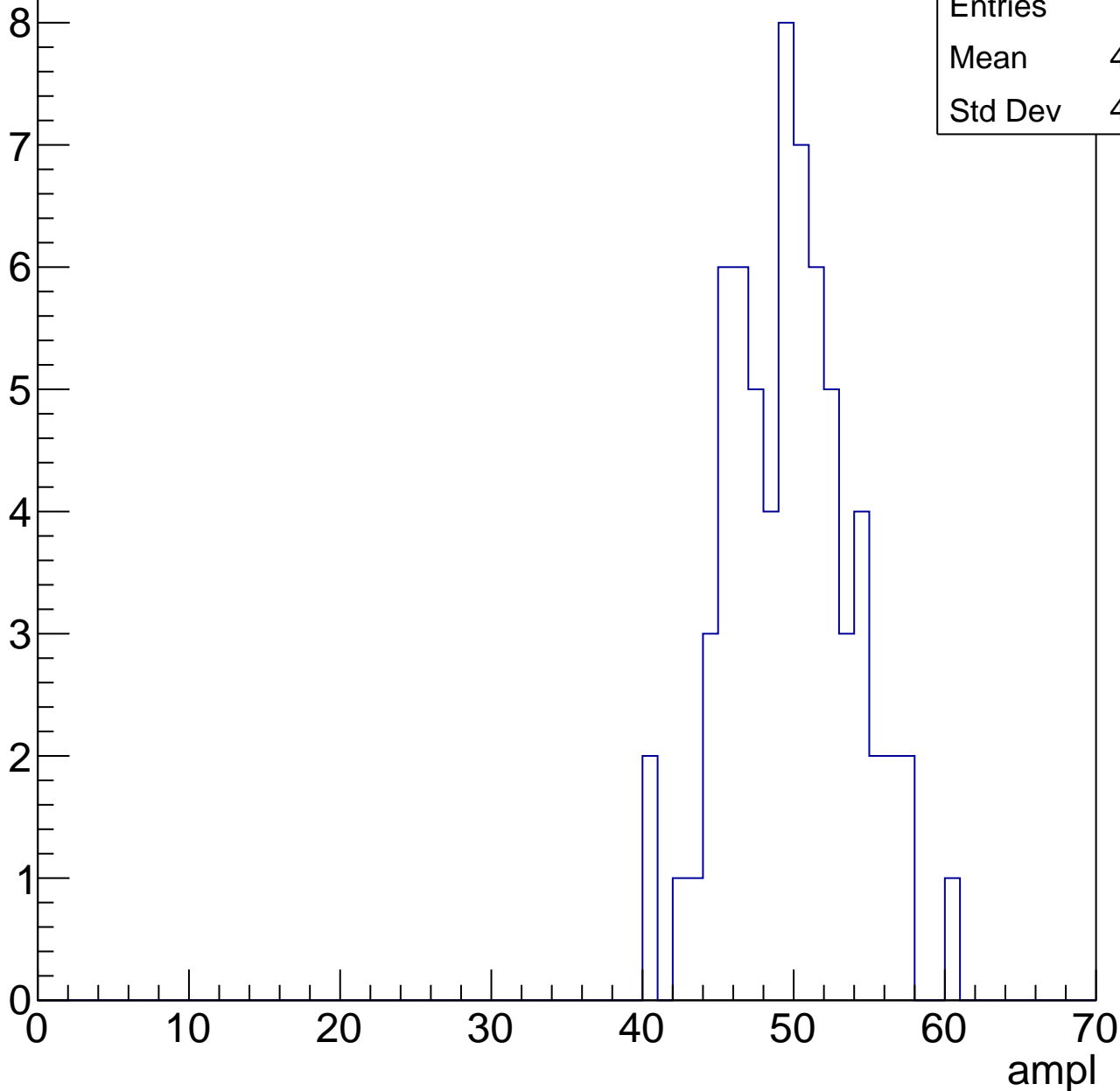


# B1L102S, U3-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	49.25
Std Dev	4.085

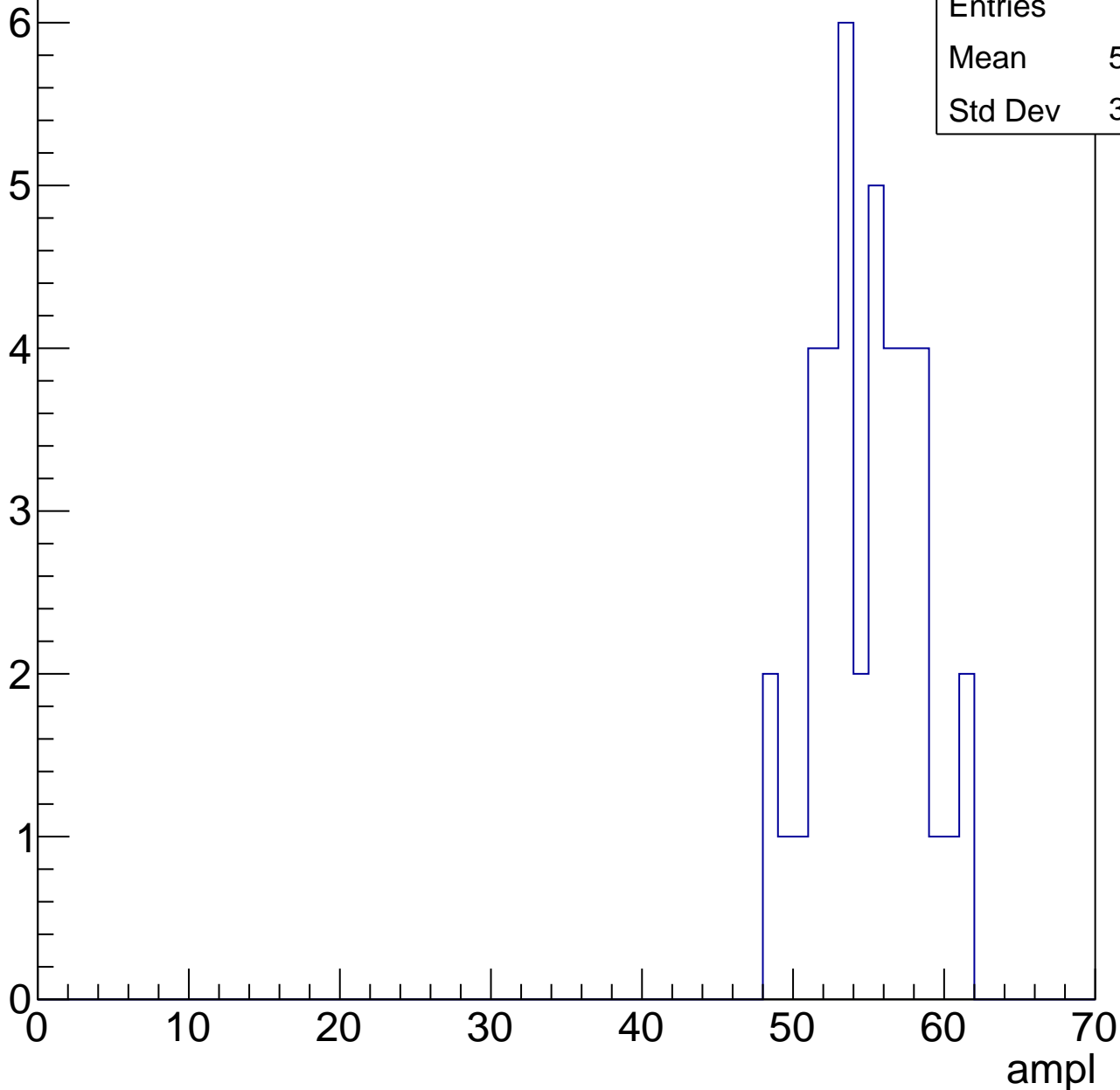


# B1L102S, U3-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	41
Mean	54.46
Std Dev	3.284



# B1L102S, U3-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	61
Mean	57.89
Std Dev	8.086

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

7

8

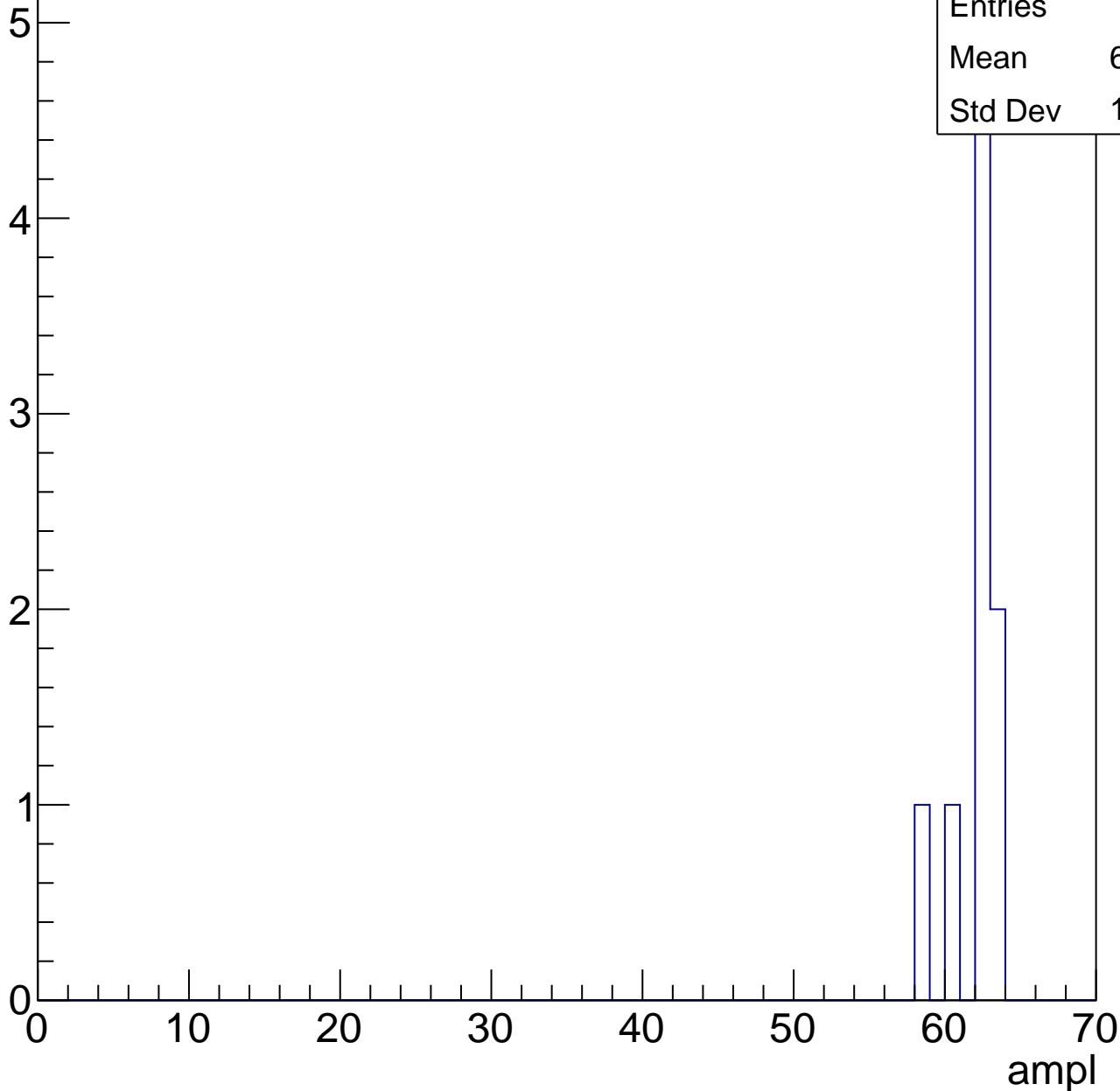
9

# B1L102S, U3-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	9
Mean	61.56
Std Dev	1.499





# B1L102S, U3-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U3-ch81, adc0

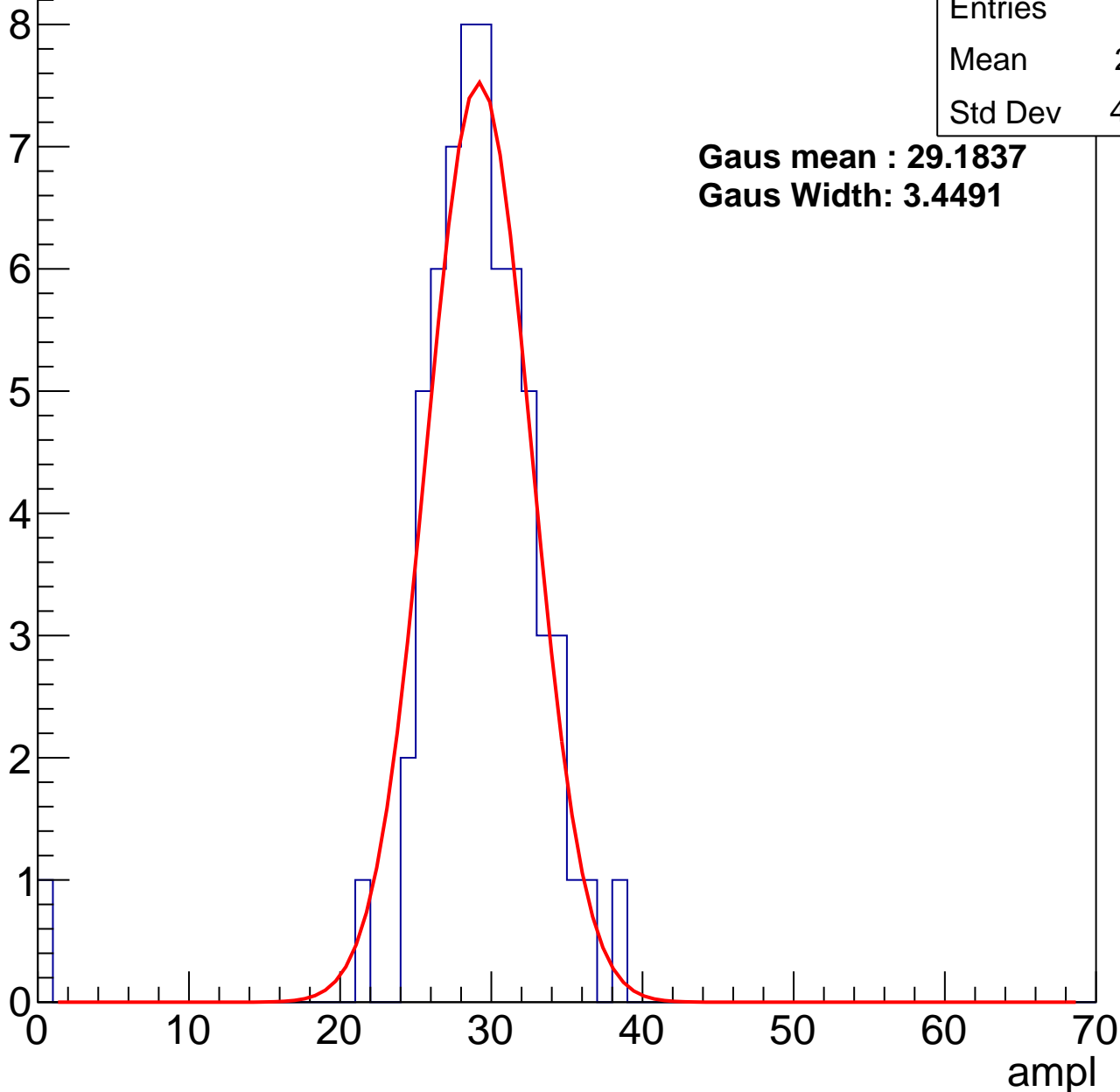
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	28.61
Std Dev	4.808

**Gaus mean : 29.1837**

**Gaus Width: 3.4491**



# B1L102S, U3-ch81, adc1

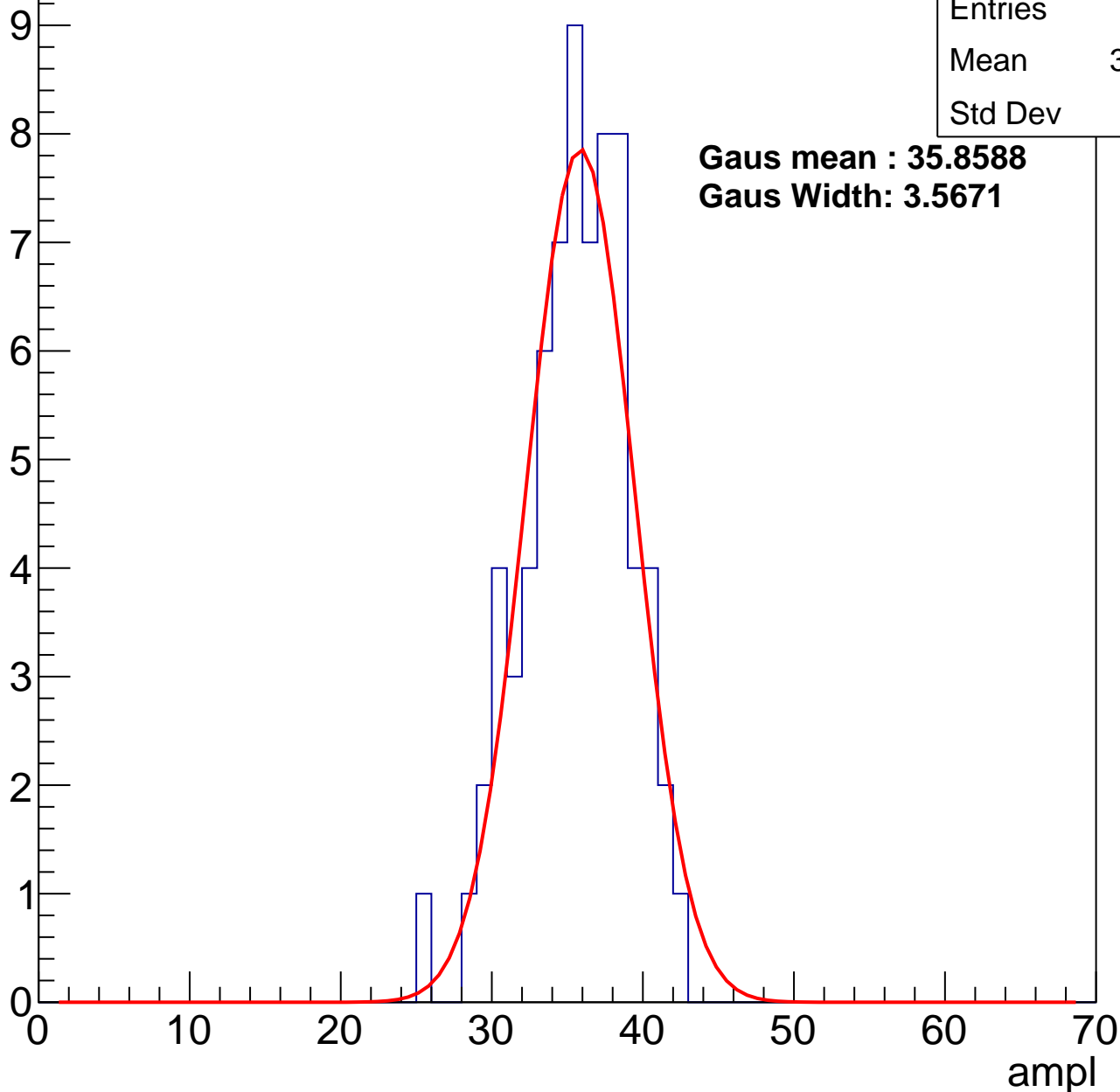
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	35.14
Std Dev	3.42

**Gaus mean : 35.8588**

**Gaus Width: 3.5671**



# B1L102S, U3-ch81, adc2

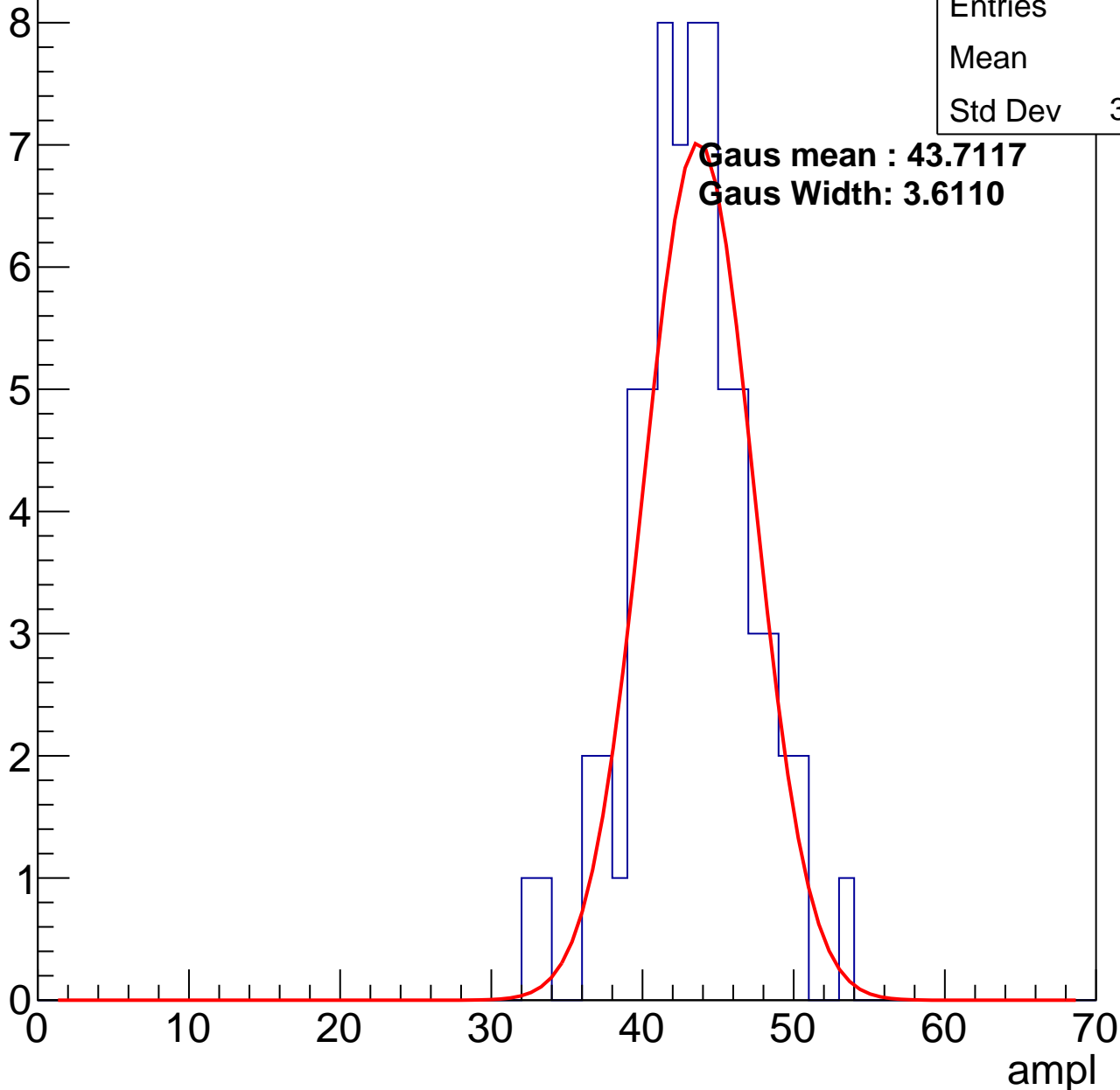
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	42.8
Std Dev	3.888

**Gaus mean : 43.7117**

**Gaus Width: 3.6110**

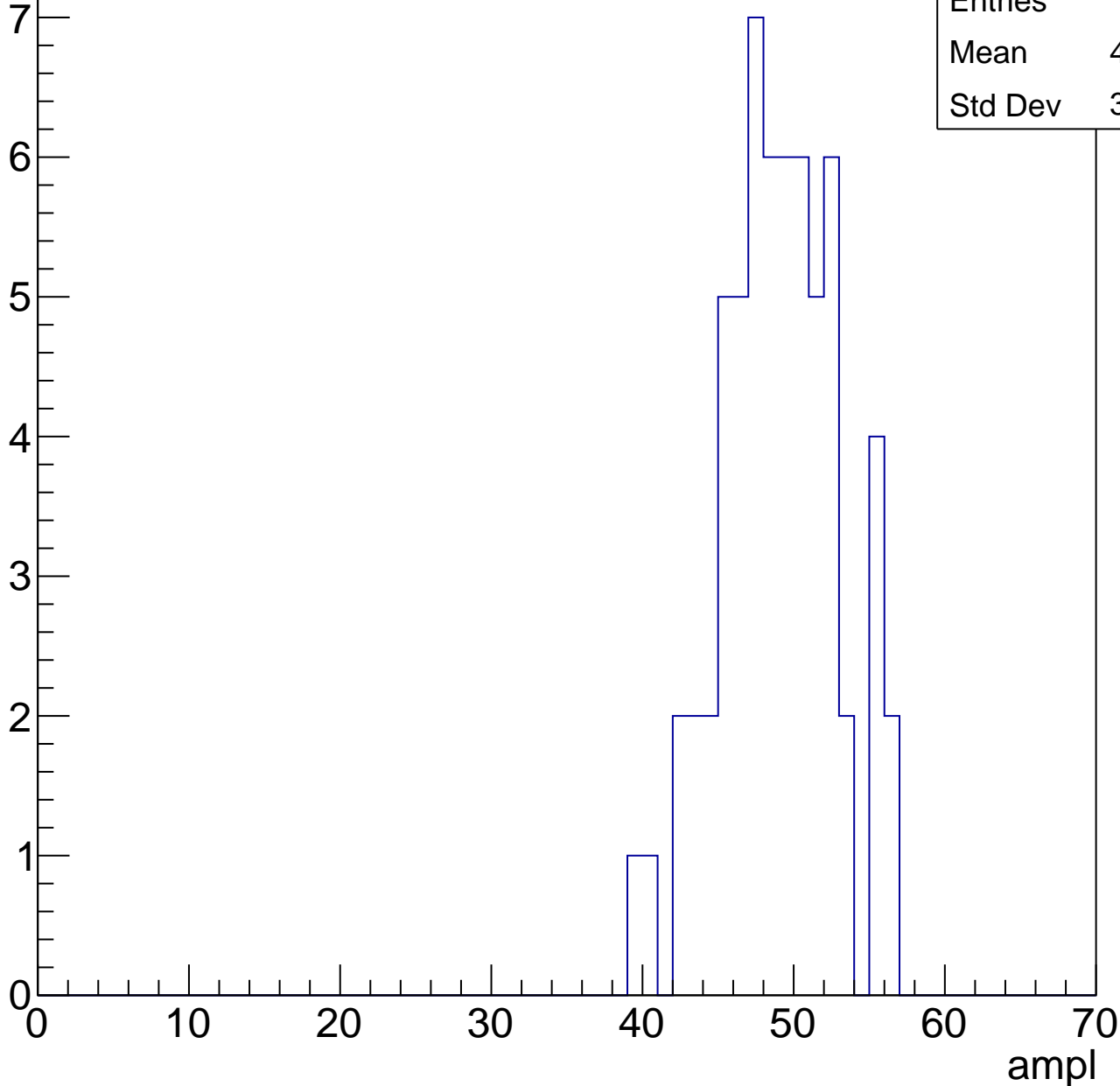


# B1L102S, U3-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	48.52
Std Dev	3.809



# B1L102S, U3-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	55
Mean	54.53
Std Dev	3.127

Entry

10

8

6

4

2

0

0

10

20

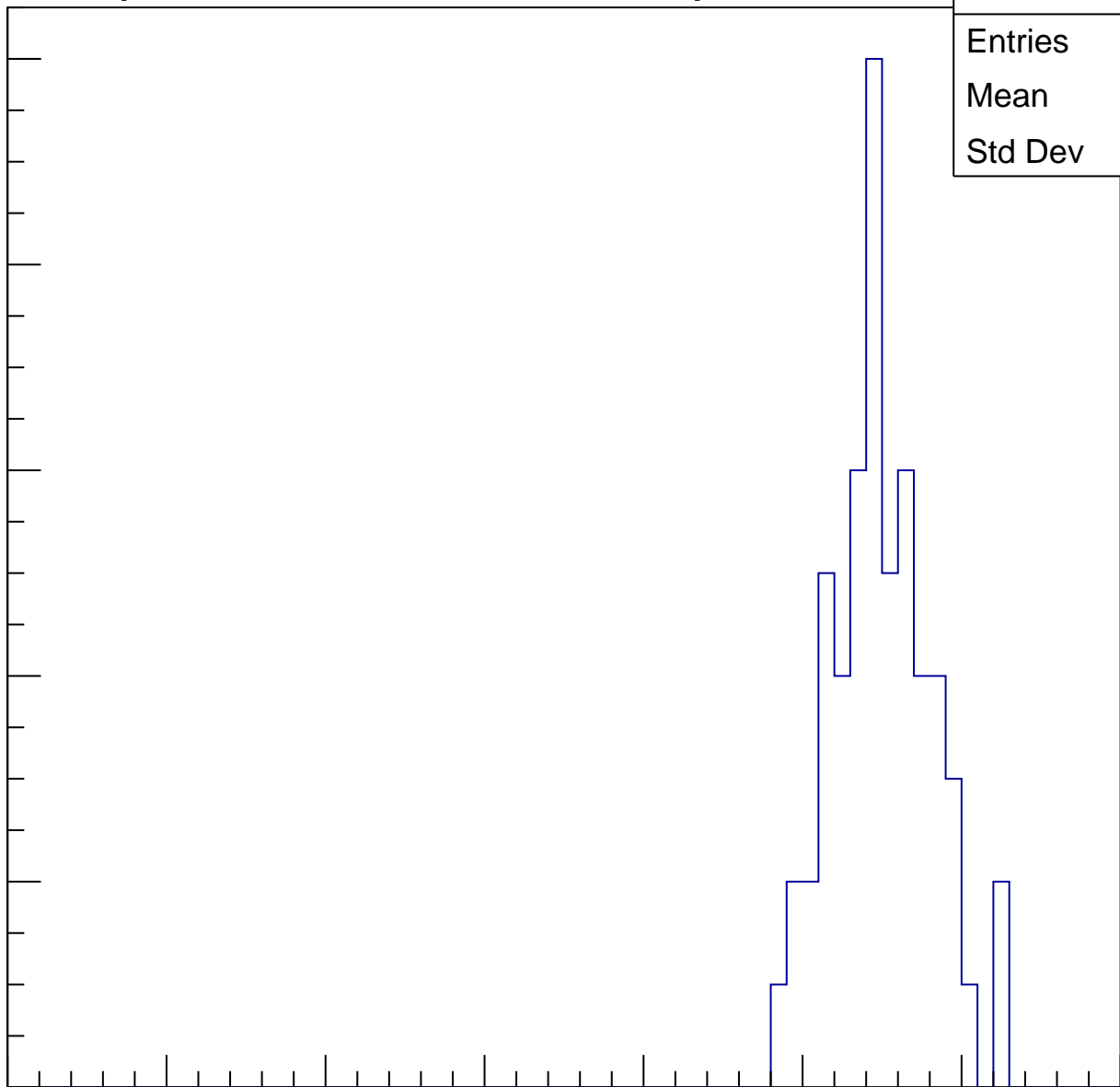
30

40

50

60

ampl

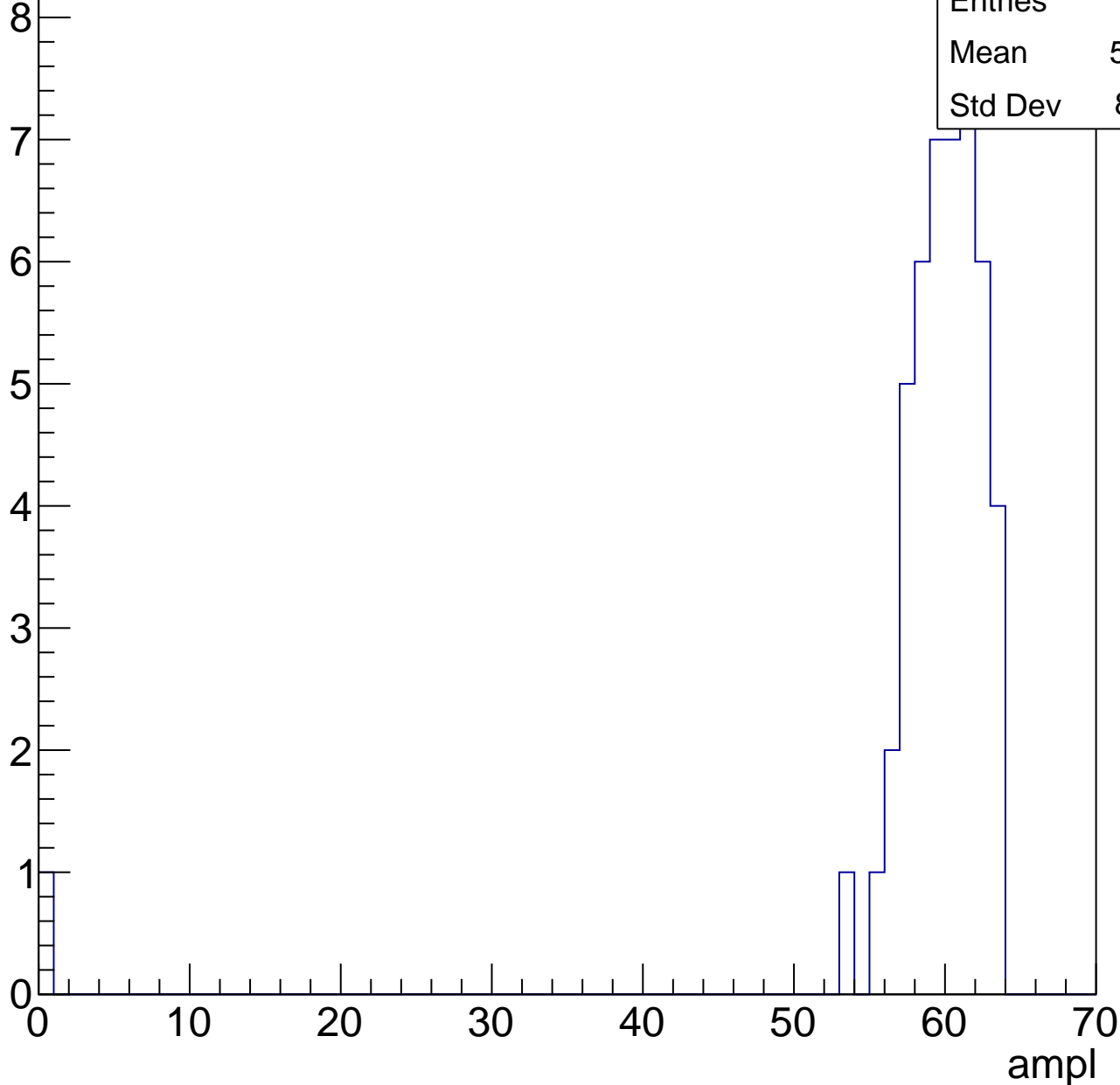


# B1L102S, U3-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	58.29
Std Dev	8.791

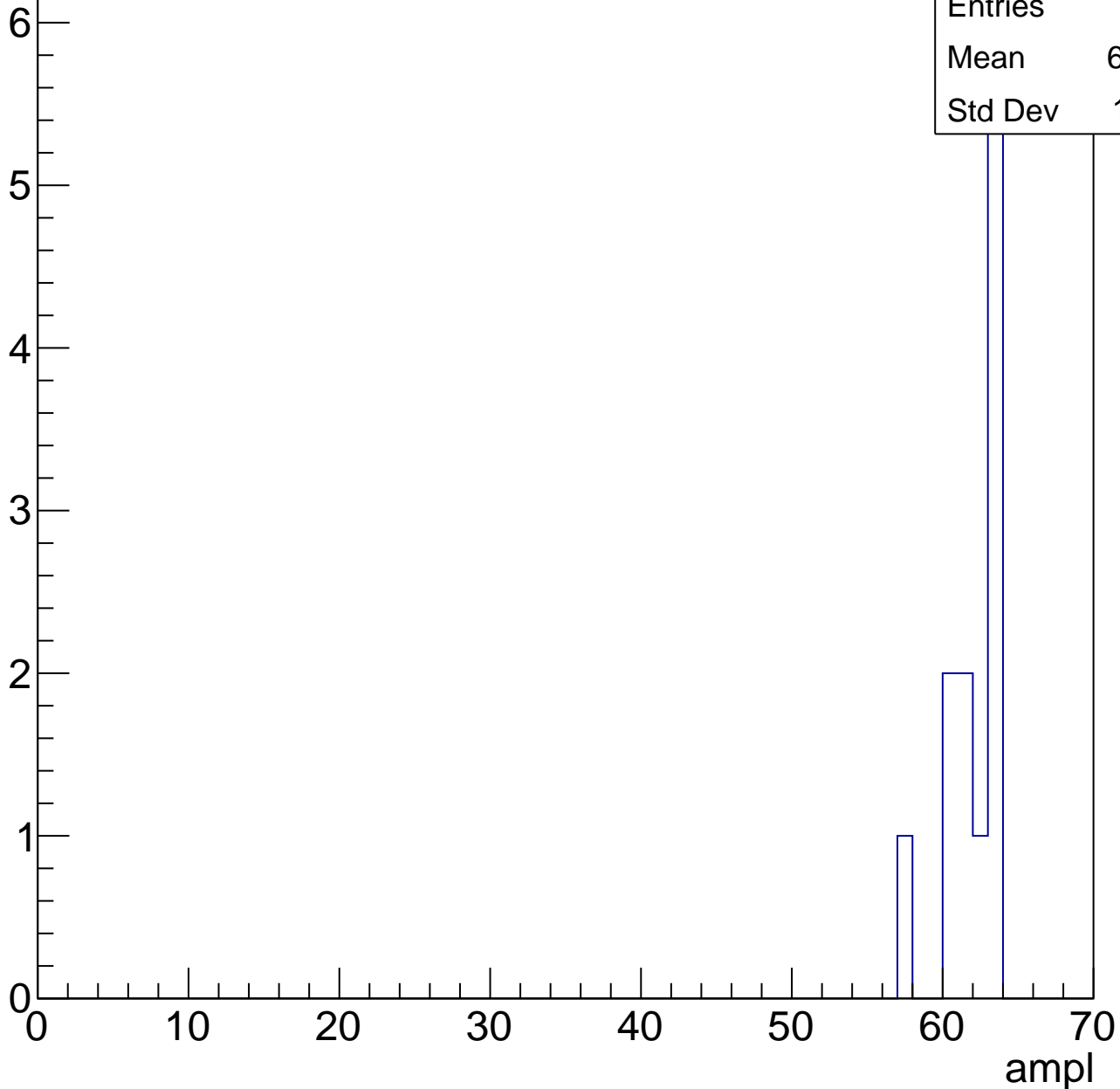


# B1L102S, U3-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	12
Mean	61.58
Std Dev	1.801





# B1L102S, U3-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch82, adc0

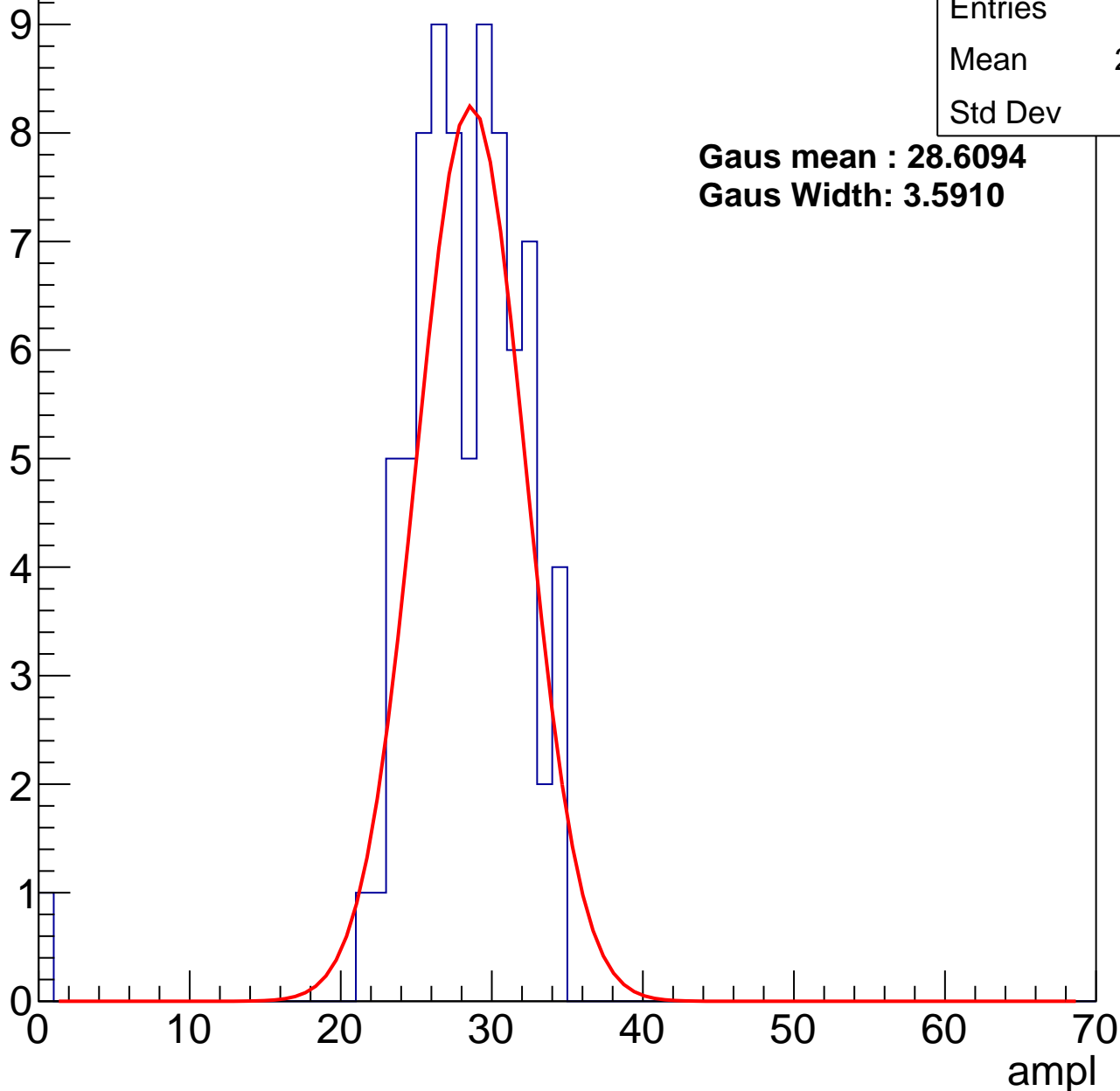
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	27.61
Std Dev	4.47

**Gaus mean : 28.6094**

**Gaus Width: 3.5910**



# B1L102S, U3-ch82, adc1

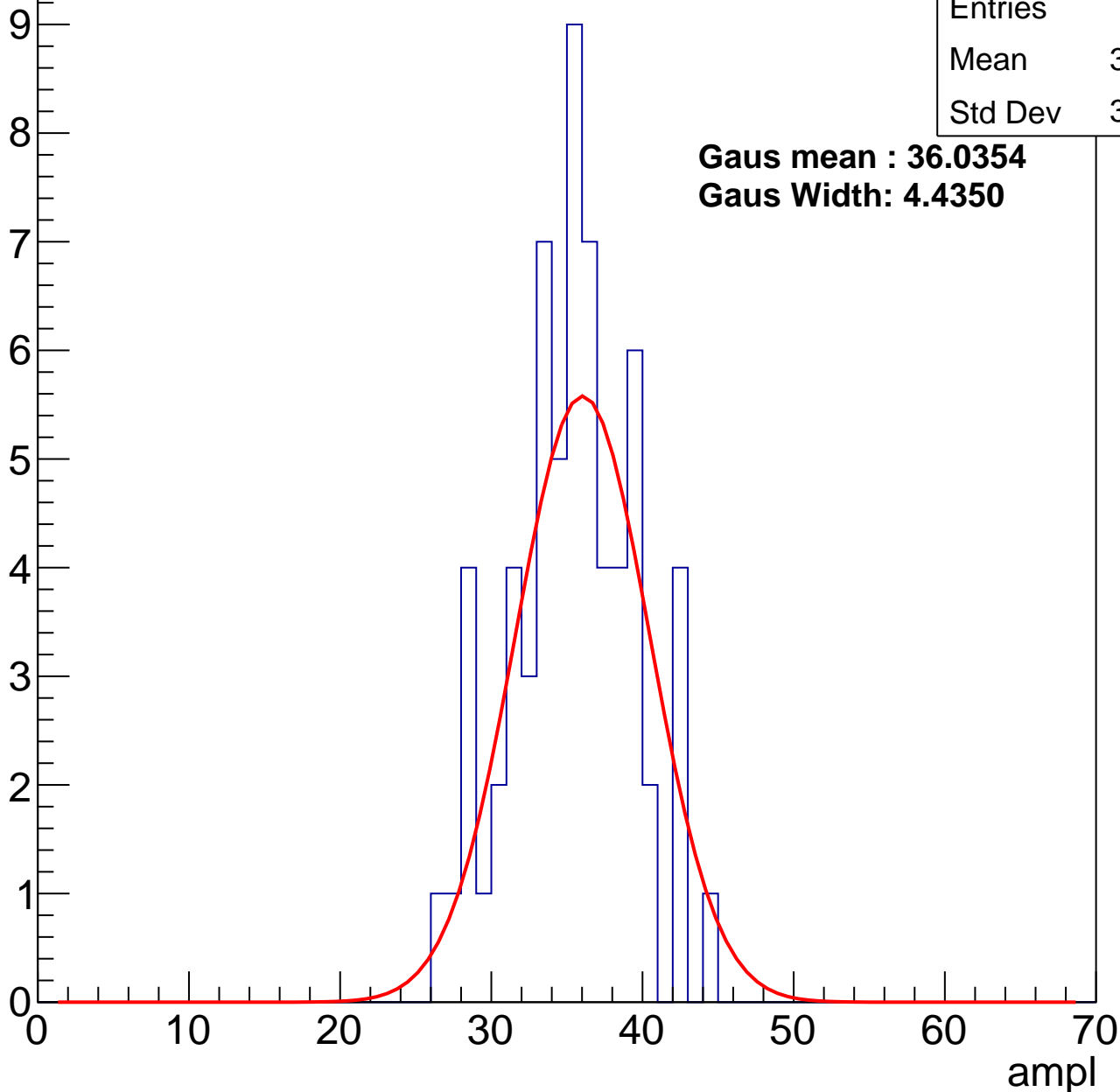
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	34.89
Std Dev	3.985

**Gaus mean : 36.0354**

**Gaus Width: 4.4350**



# B1L102S, U3-ch82, adc2

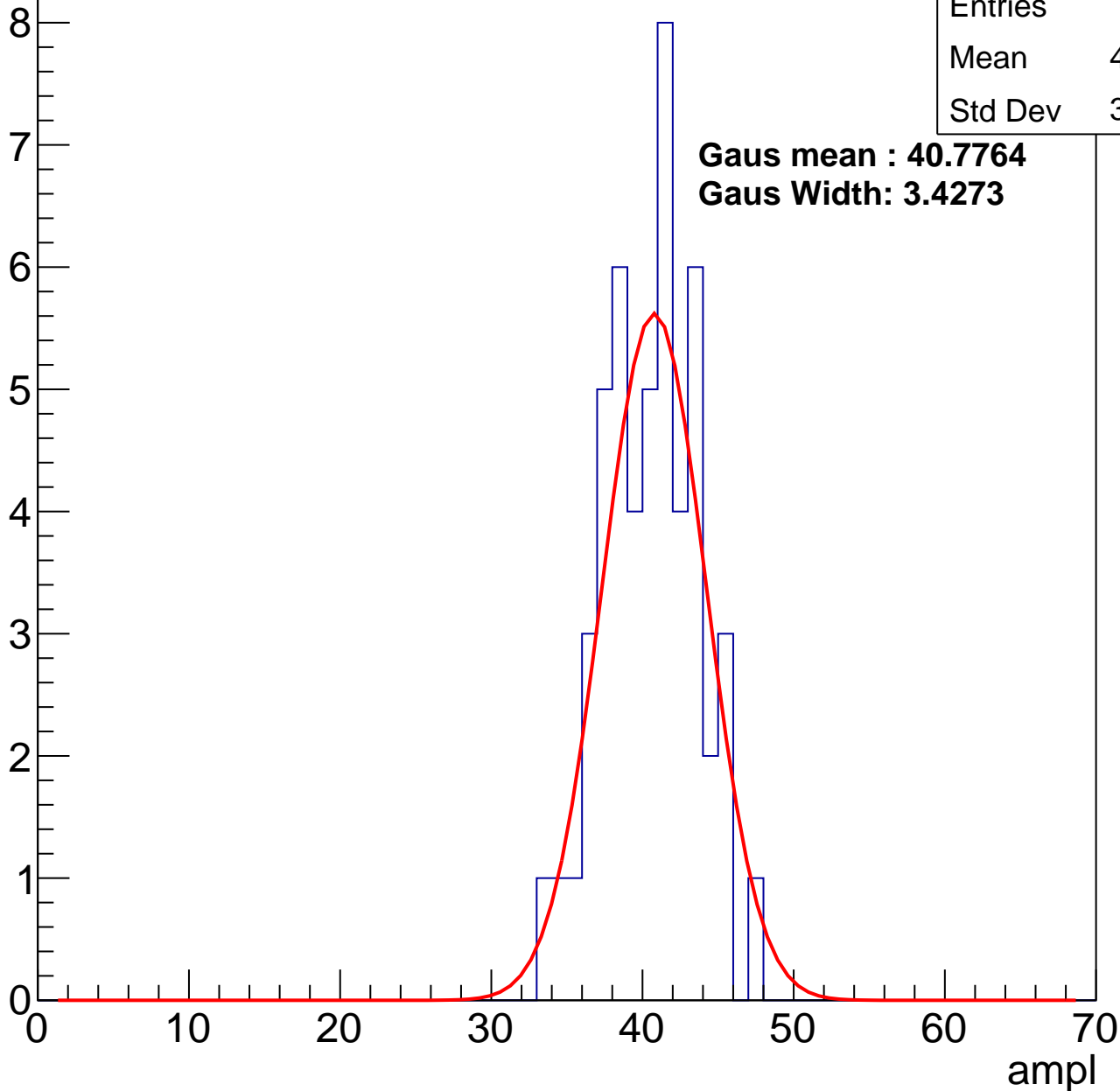
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	40.06
Std Dev	3.049

**Gaus mean : 40.7764**

**Gaus Width: 3.4273**



# B1L102S, U3-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

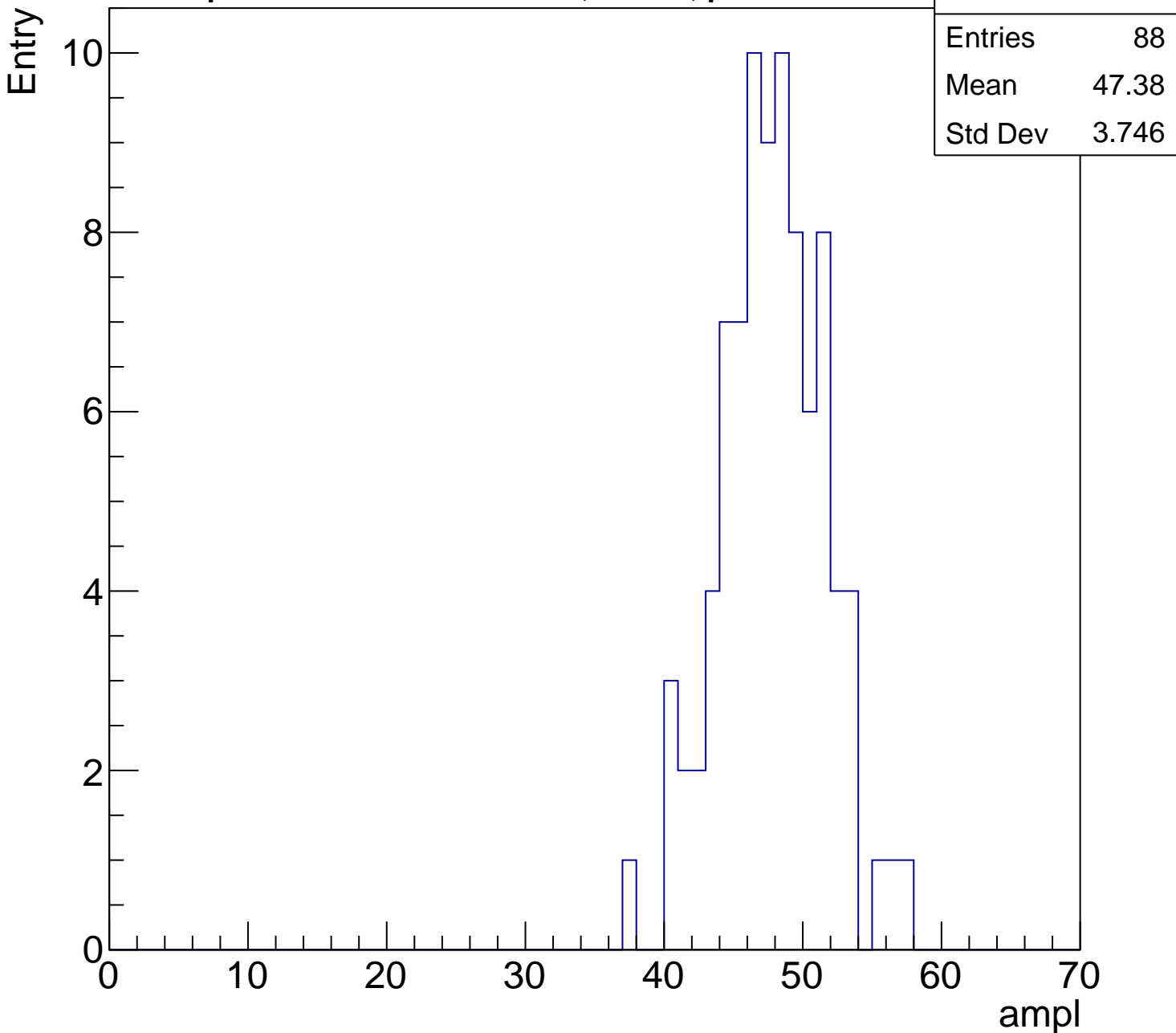
Entries	88
Mean	47.38
Std Dev	3.746

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

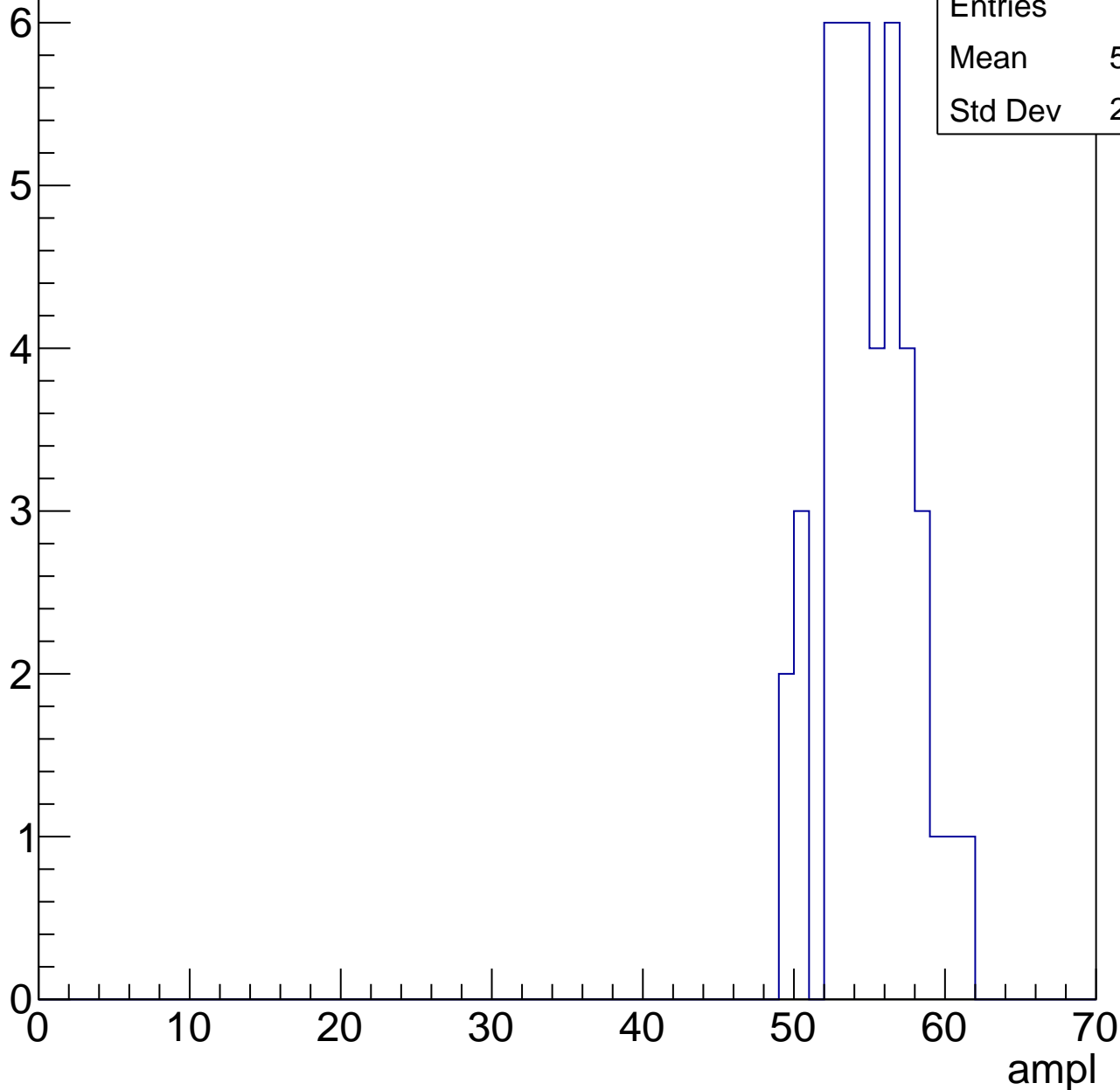
ampl



# B1L102S, U3-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



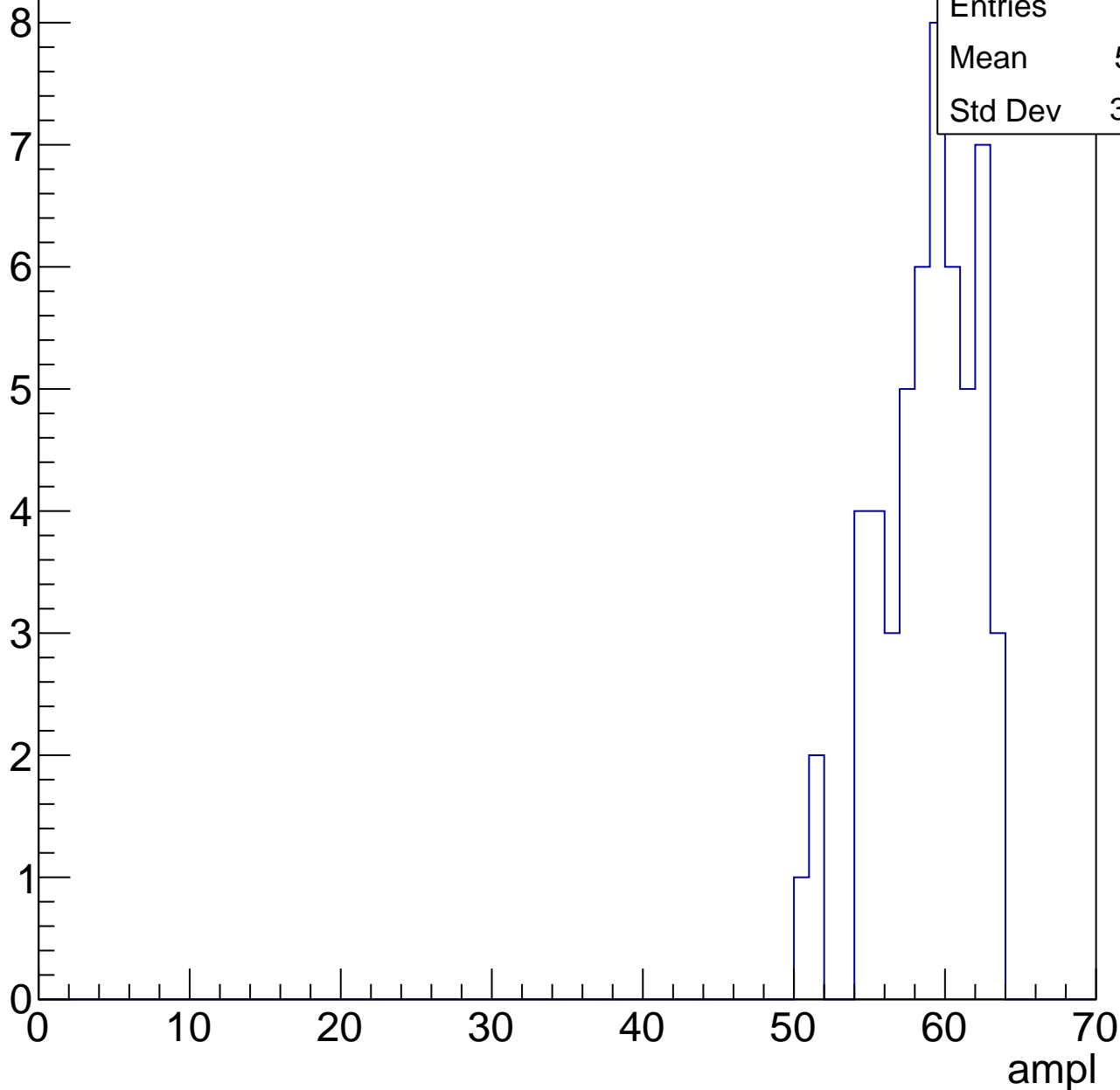
Entries	43
Mean	54.42
Std Dev	2.822

# B1L102S, U3-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	58.31
Std Dev	3.155

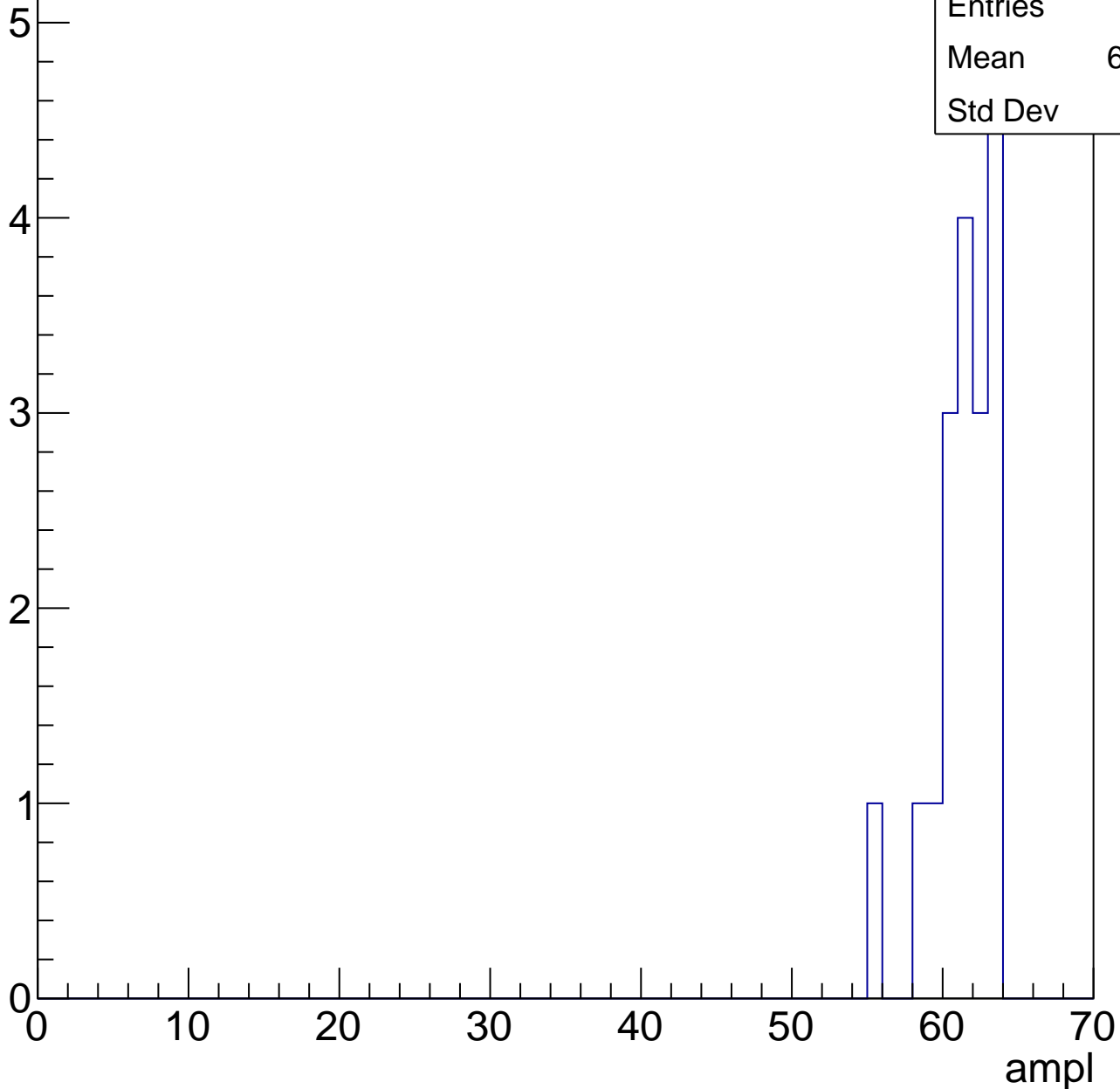


# B1L102S, U3-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	18
Mean	60.94
Std Dev	2.04

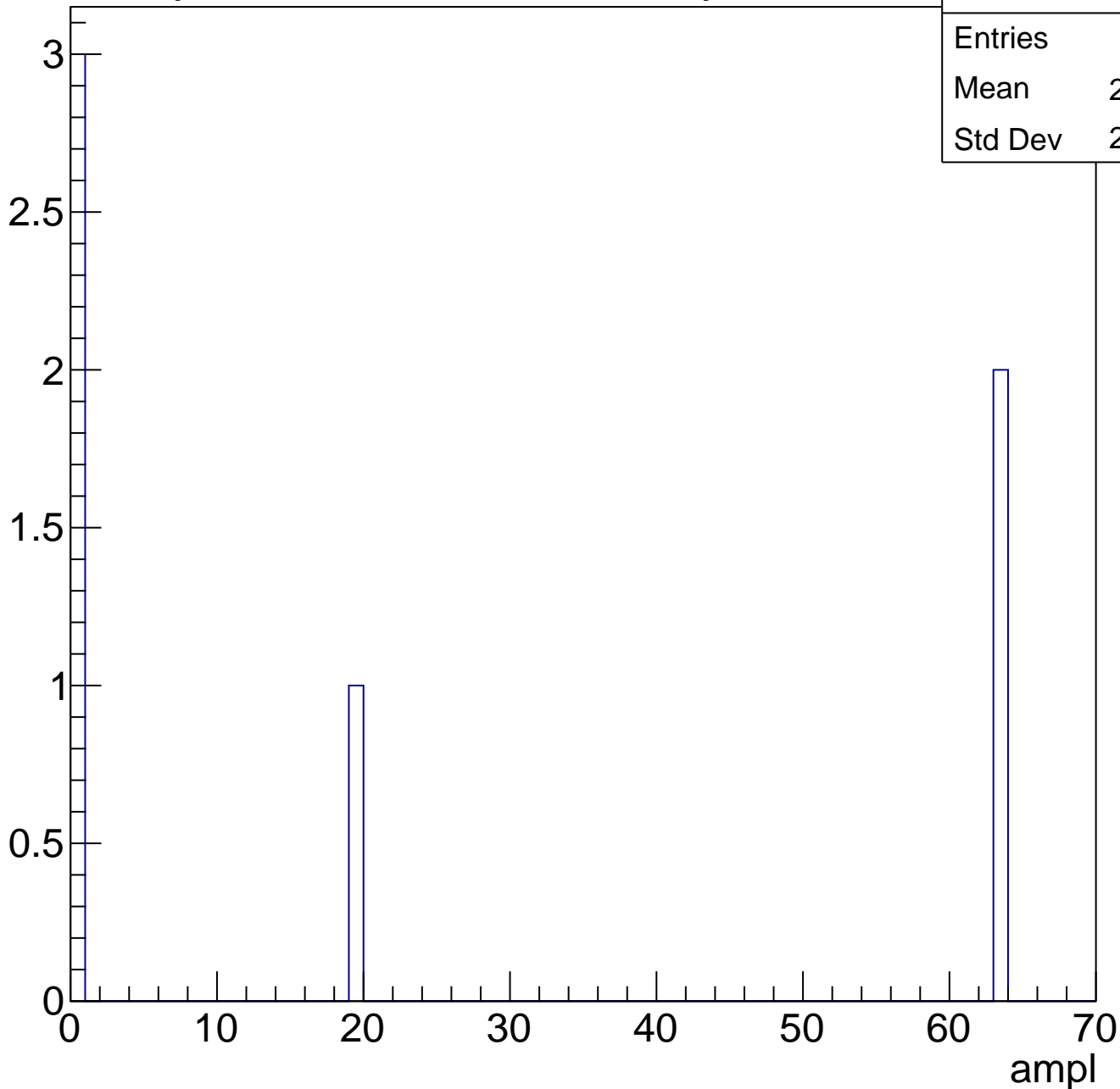




# B1L102S, U3-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	6
Mean	24.17
Std Dev	28.27

# B1L102S, U3-ch83, adc0

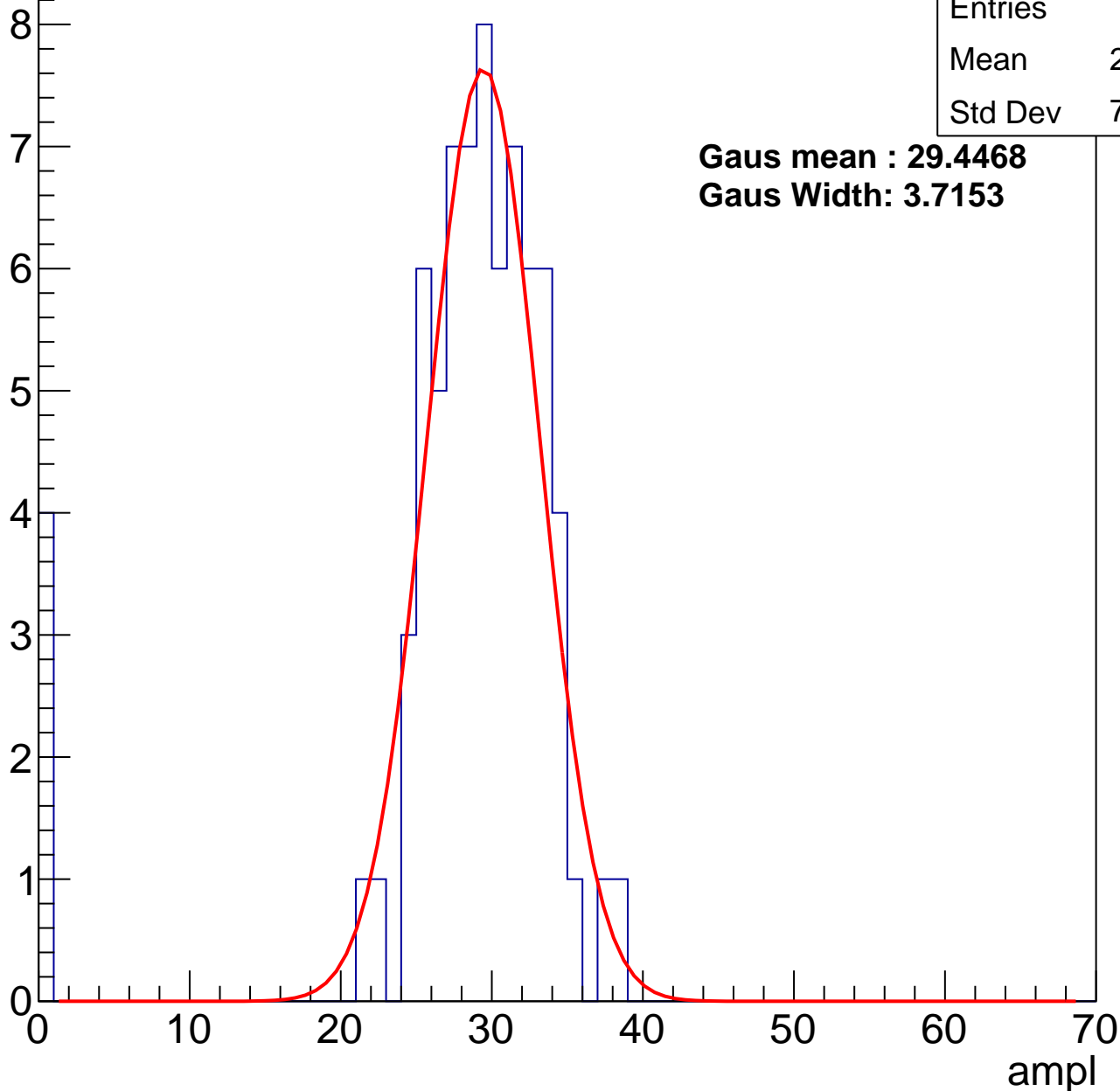
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	27.64
Std Dev	7.403

**Gaus mean : 29.4468**

**Gaus Width: 3.7153**



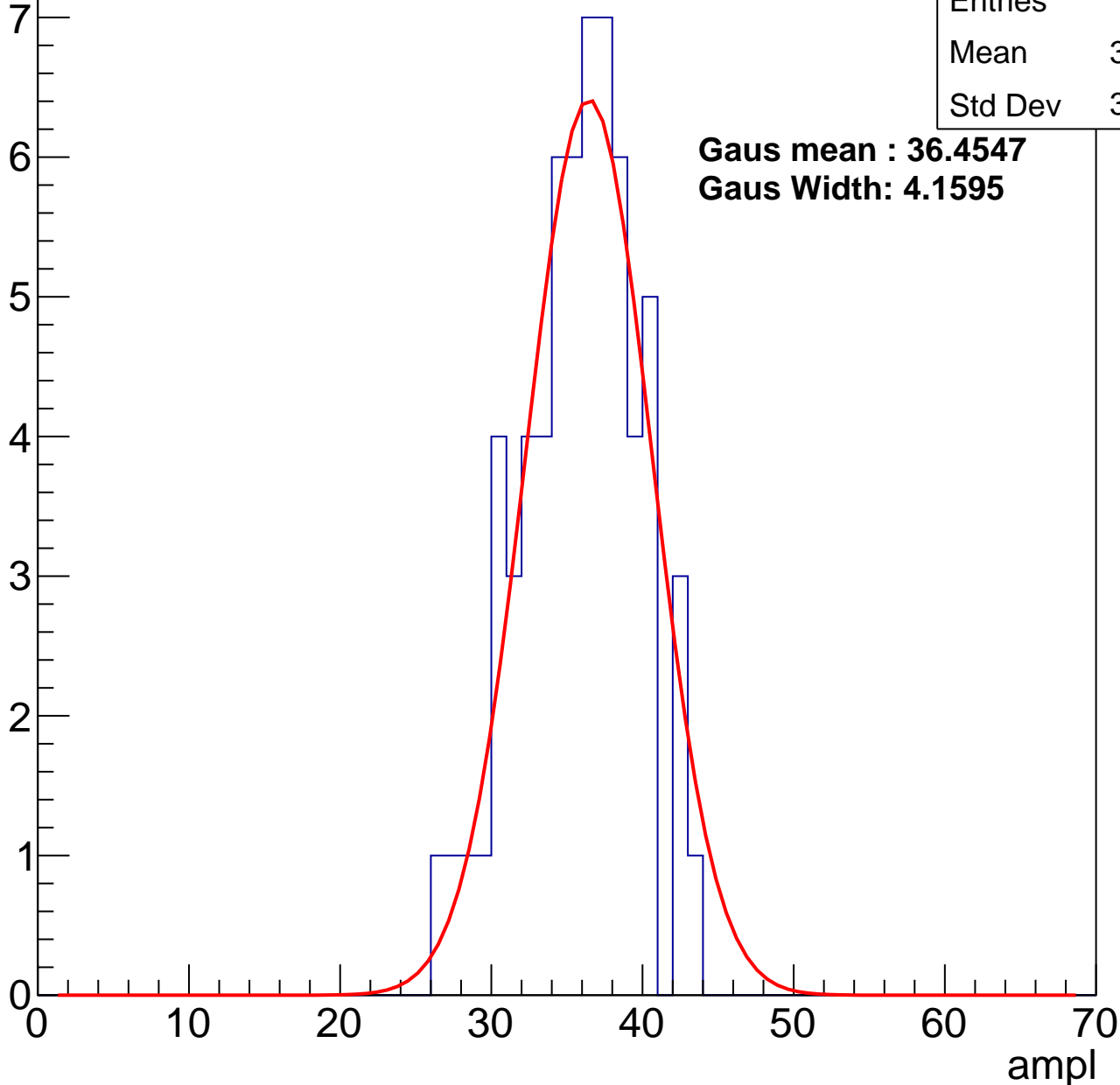
# B1L102S, U3-ch83, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	35.33
Std Dev	3.788

**Gaus mean : 36.4547**  
**Gaus Width: 4.1595**



# B1L102S, U3-ch83, adc2

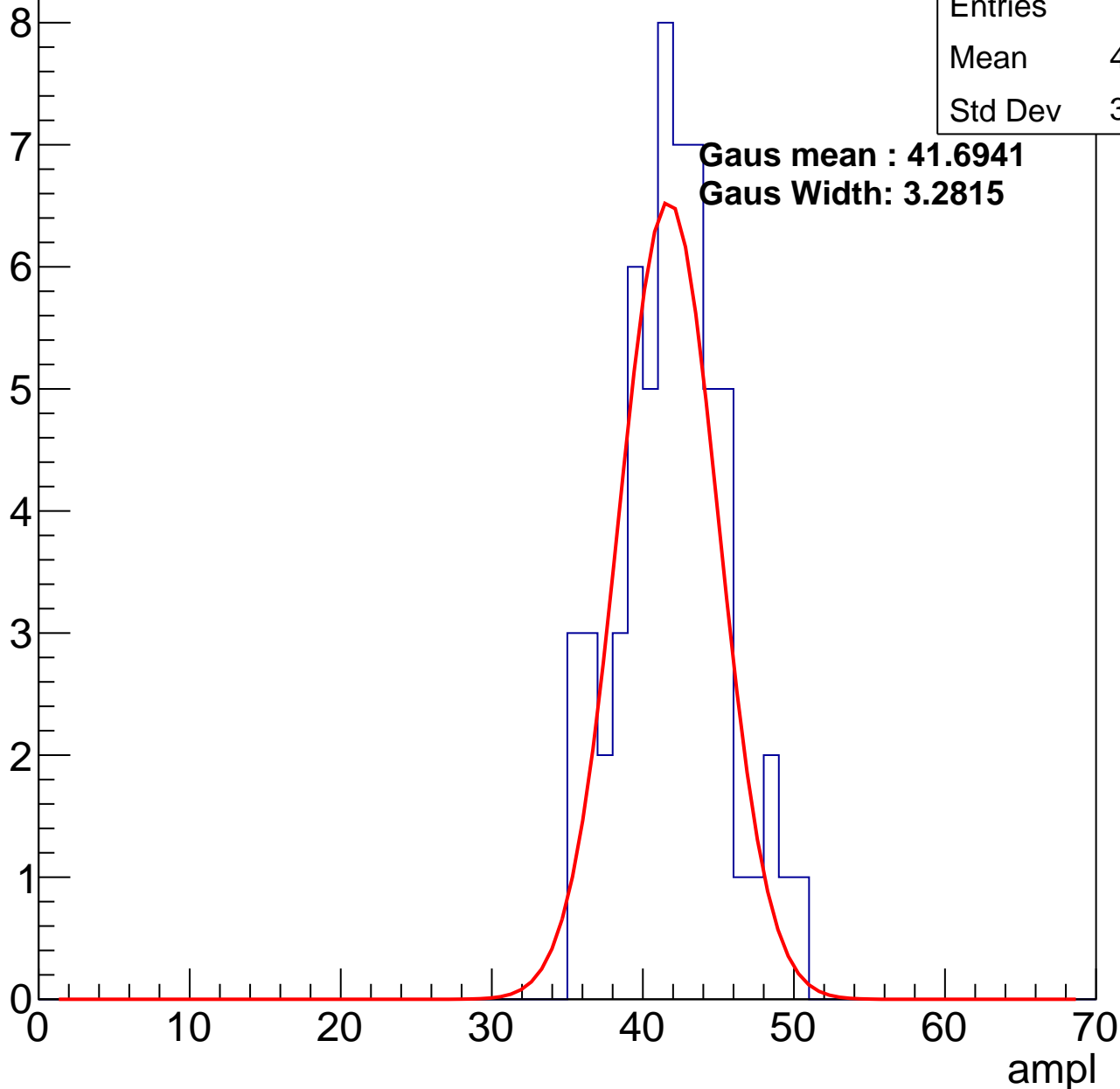
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	41.52
Std Dev	3.462

**Gaus mean : 41.6941**

**Gaus Width: 3.2815**

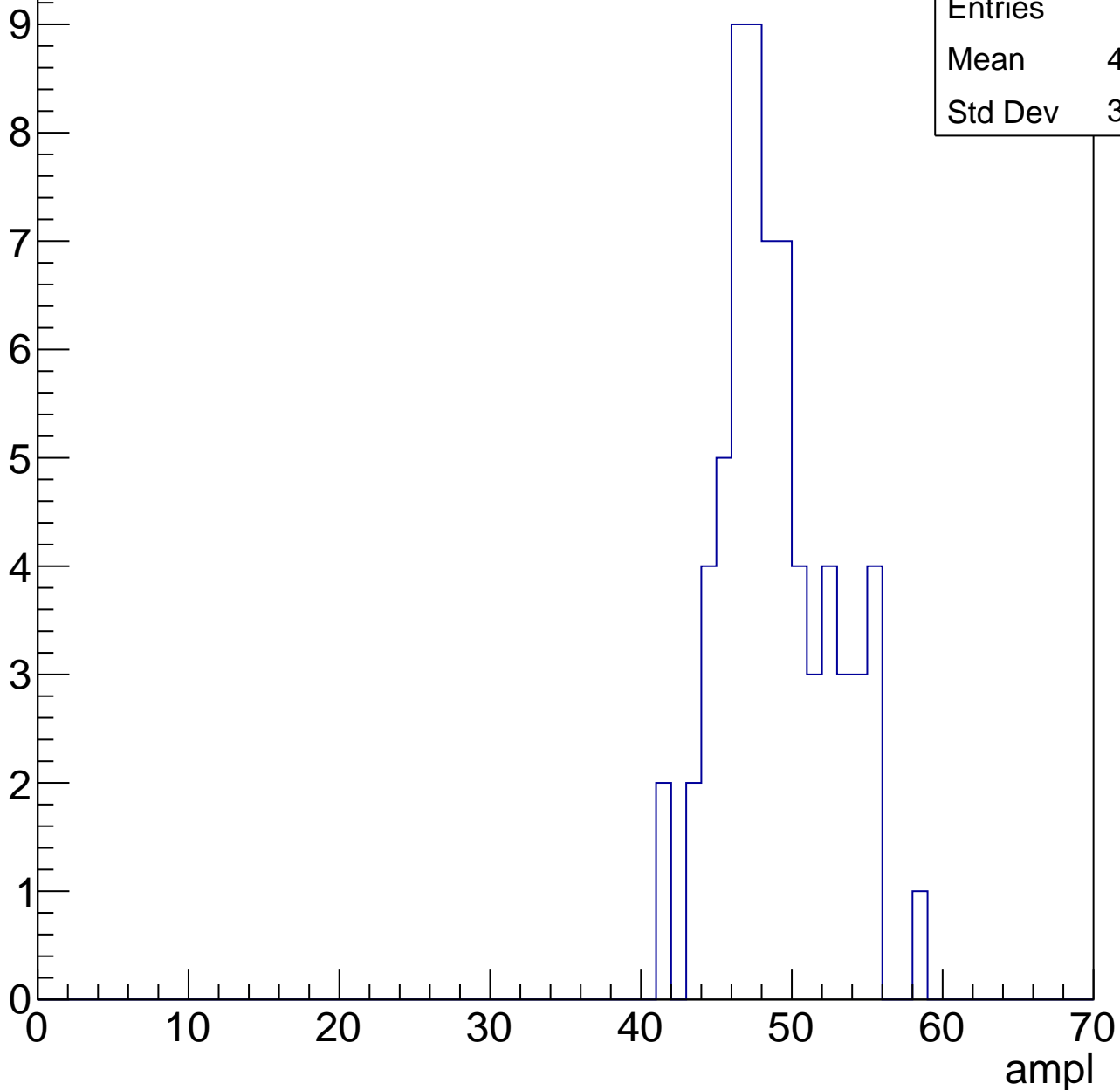


# B1L102S, U3-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	48.43
Std Dev	3.629

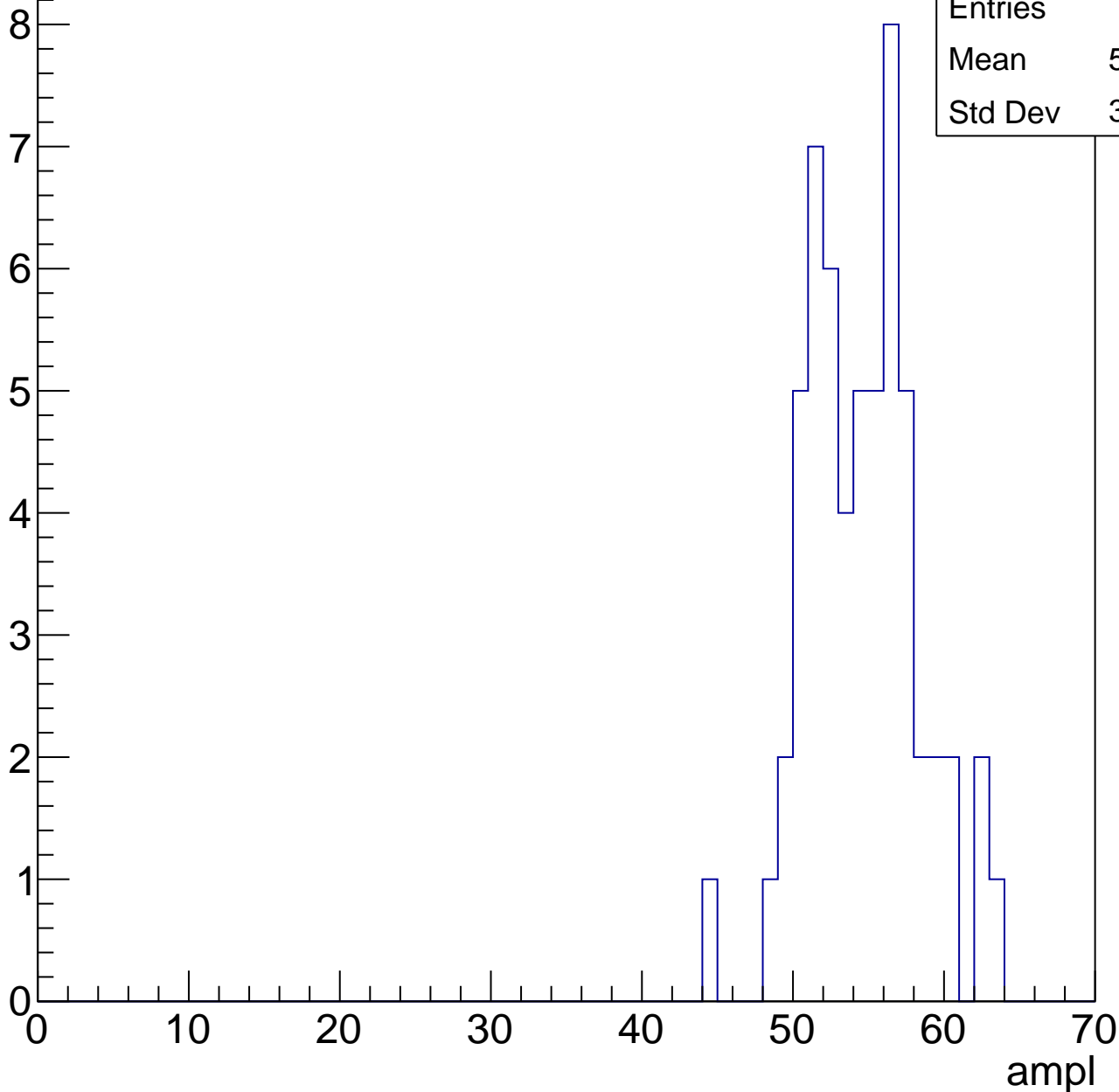


# B1L102S, U3-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	54.14
Std Dev	3.716

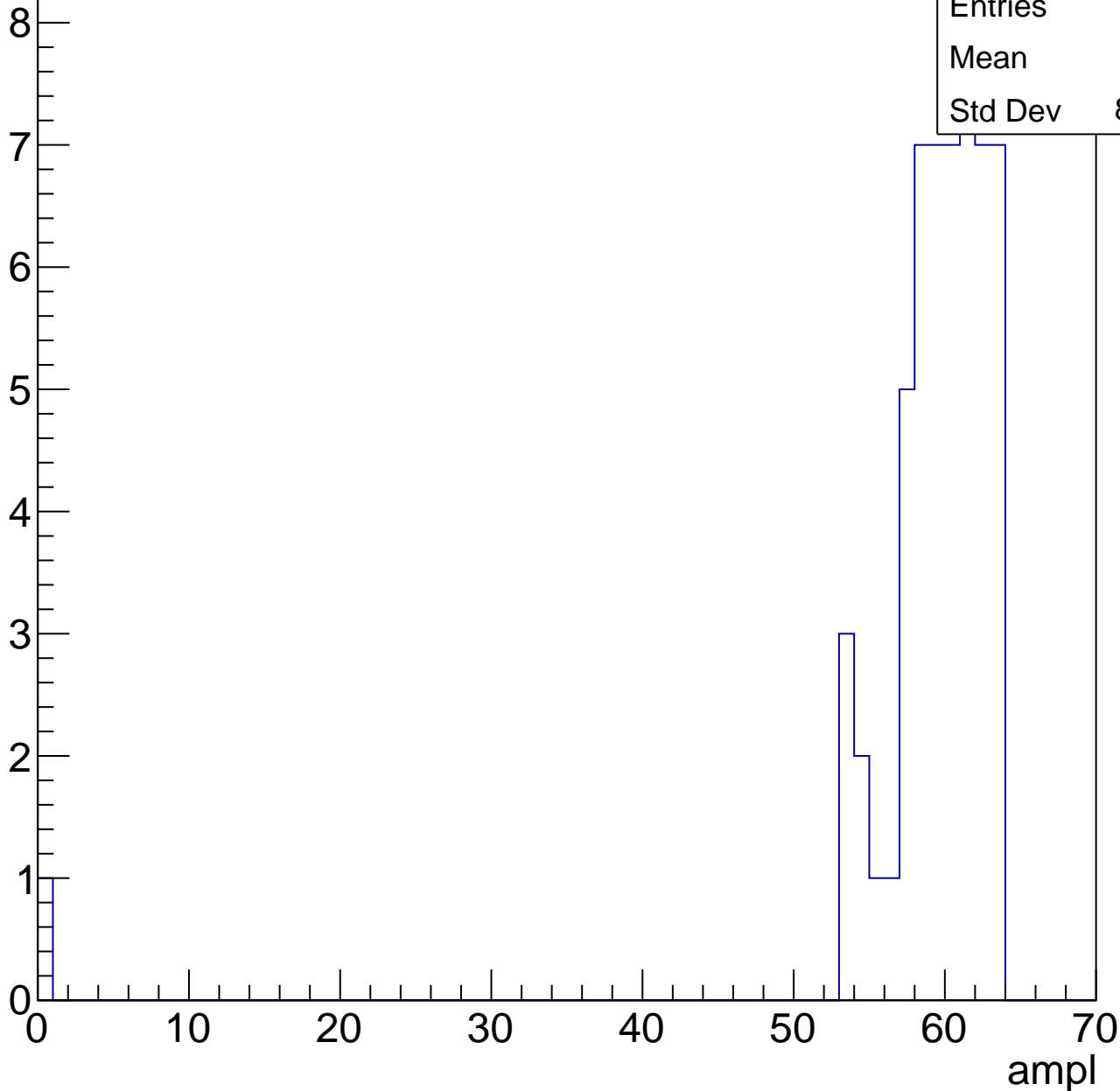


# B1L102S, U3-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	58.3
Std Dev	8.321



# B1L102S, U3-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

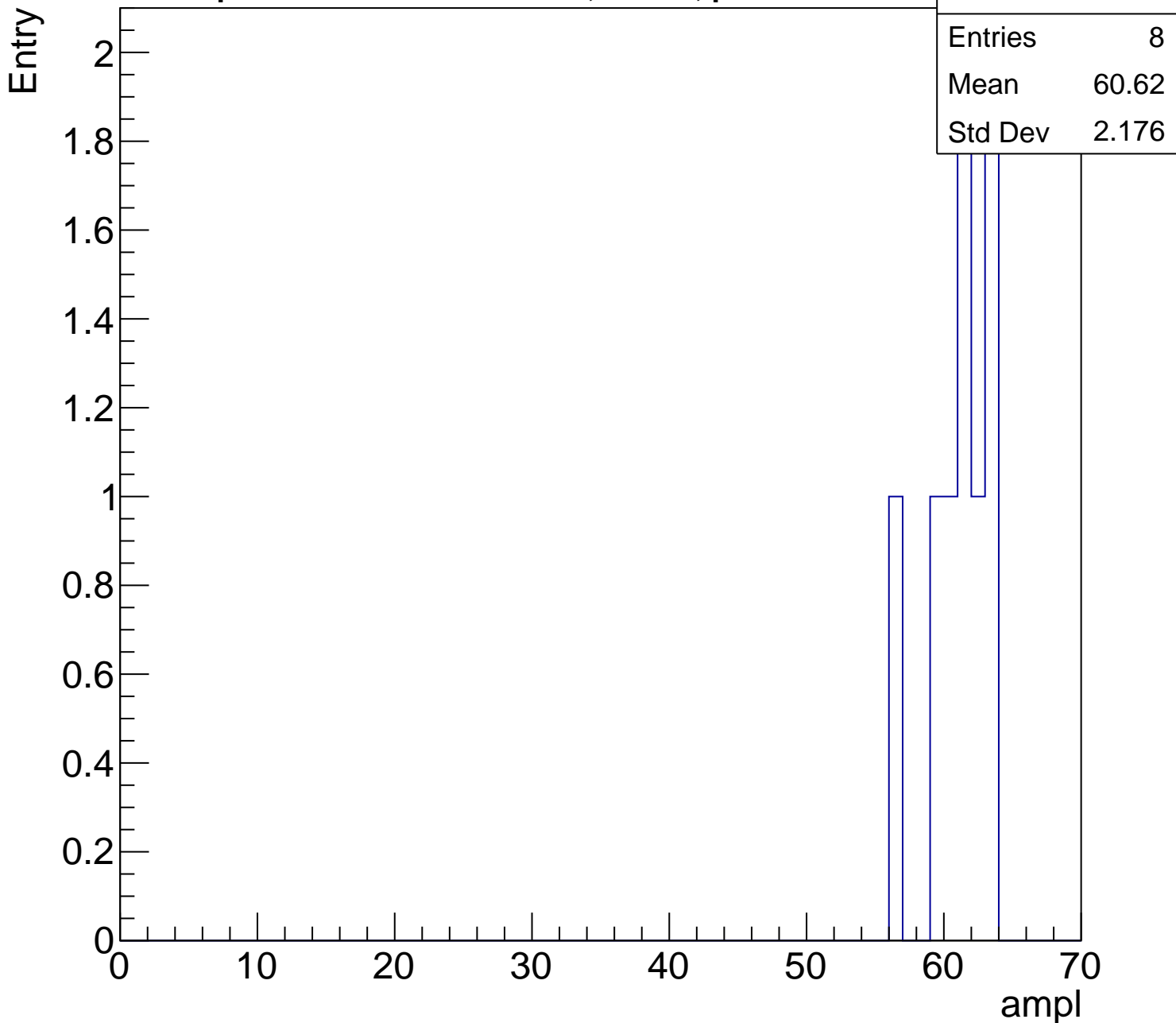
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	8
Mean	60.62
Std Dev	2.176

0 10 20 30 40 50 60 70

ampl





# B1L102S, U3-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U3-ch84, adc0

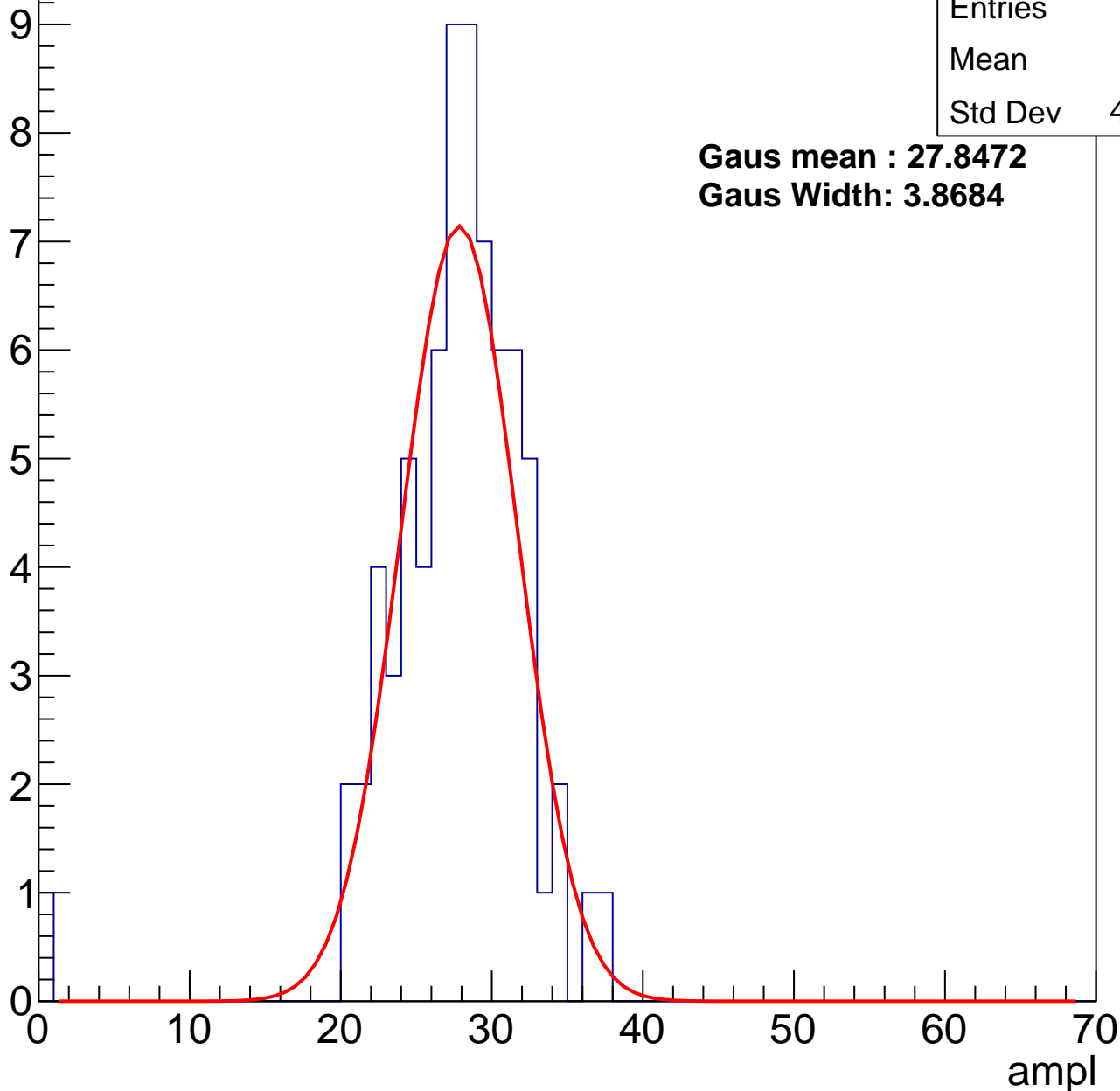
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	27.2
Std Dev	4.846

**Gaus mean : 27.8472**

**Gaus Width: 3.8684**



# B1L102S, U3-ch84, adc1

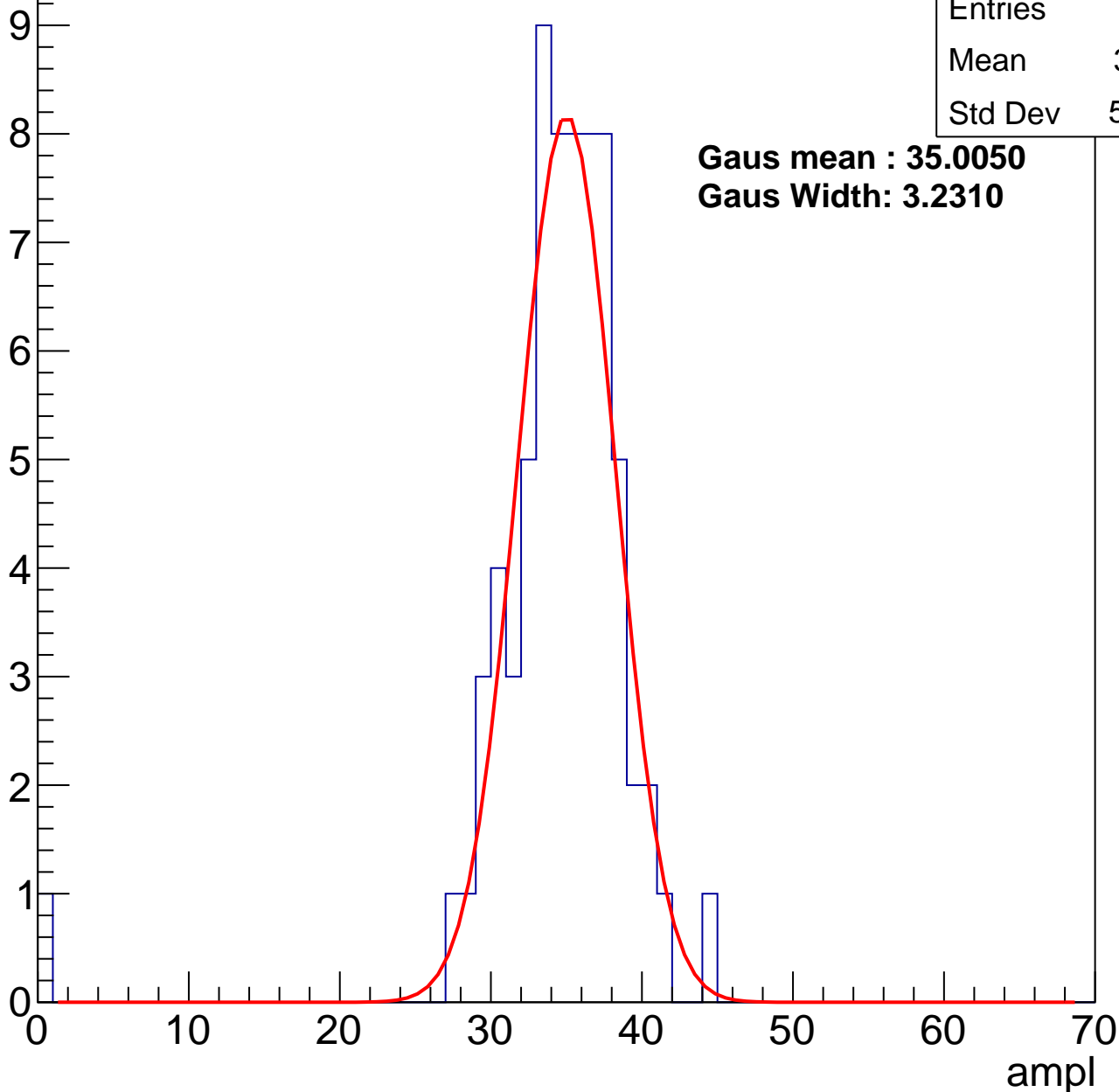
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	34.01
Std Dev	5.208

**Gaus mean : 35.0050**

**Gaus Width: 3.2310**



# B1L102S, U3-ch84, adc2

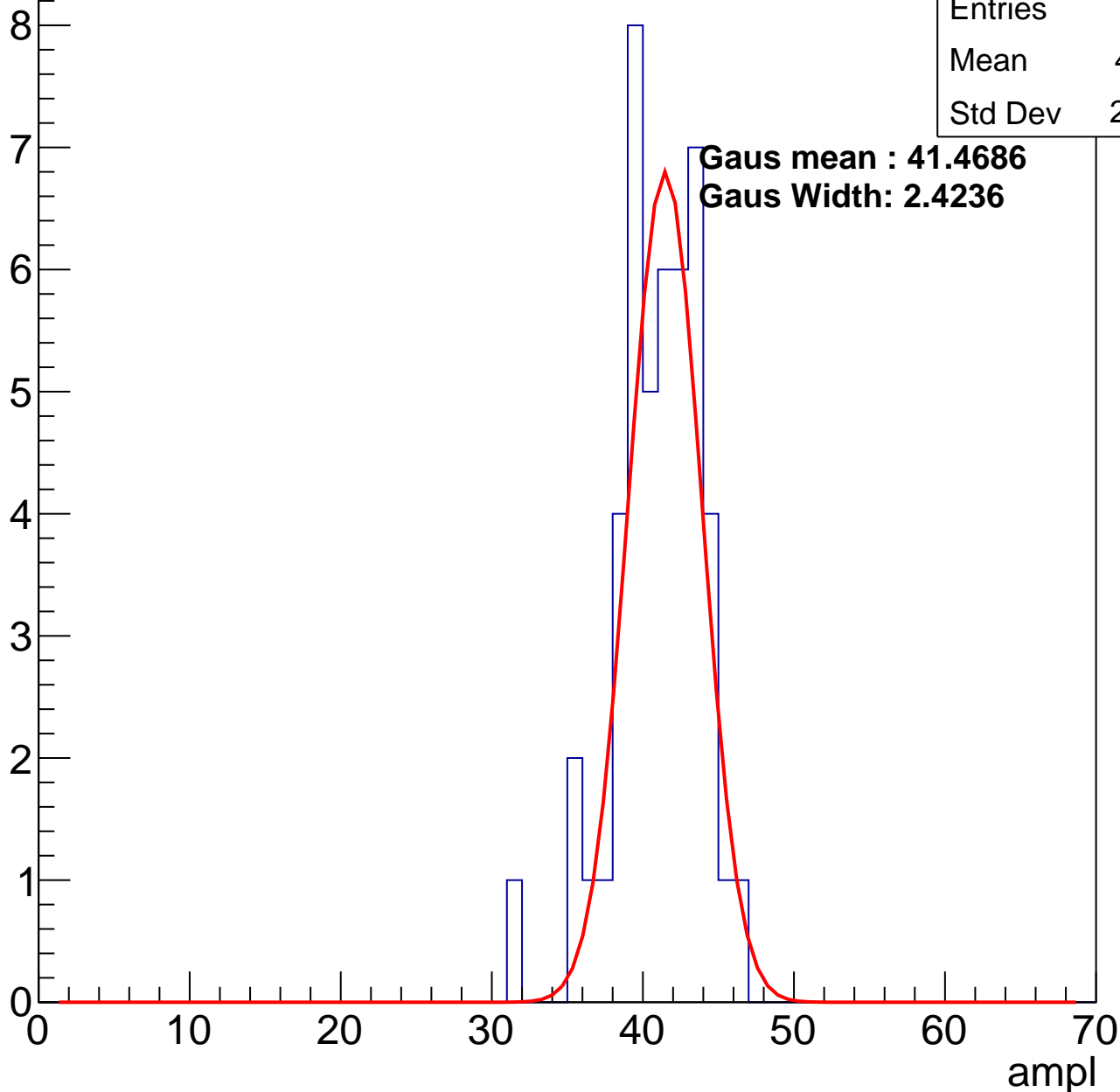
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	40.51
Std Dev	2.865

**Gaus mean : 41.4686**

**Gaus Width: 2.4236**



# B1L102S, U3-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	70
Mean	46.37
Std Dev	3.419

Entry

10

8

6

4

2

0

0

10

20

30

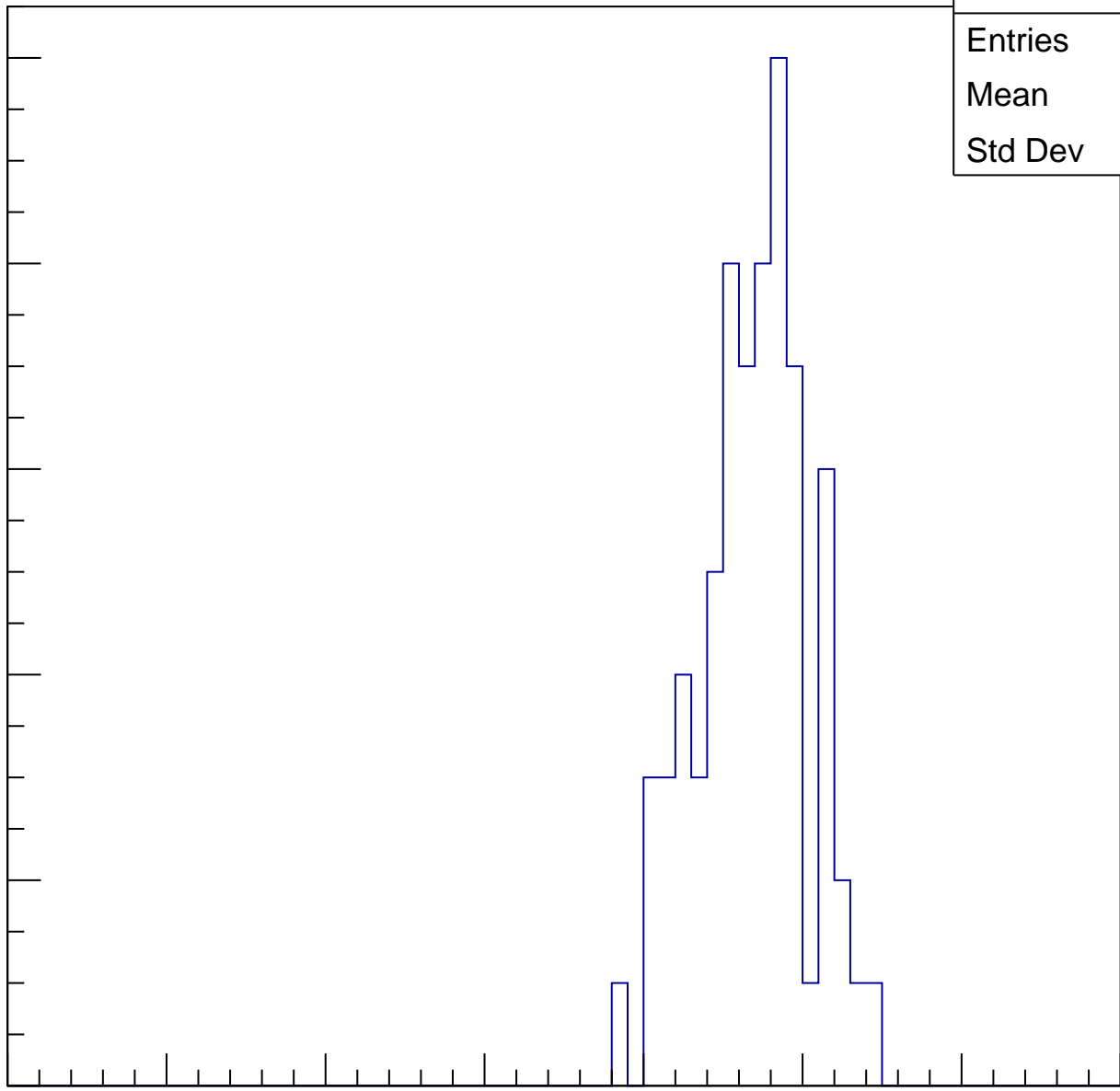
40

50

60

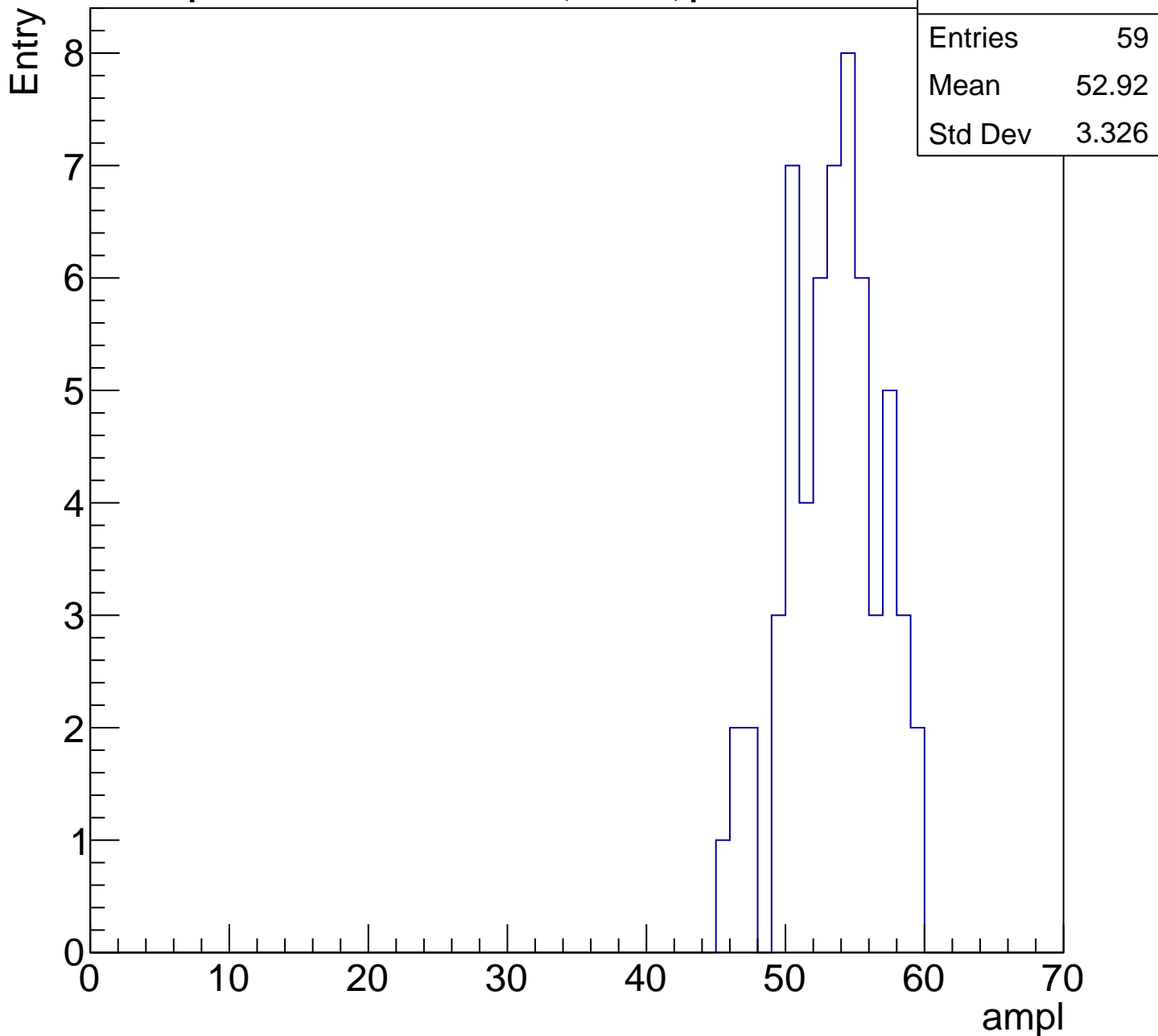
70

ampl



# B1L102S, U3-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

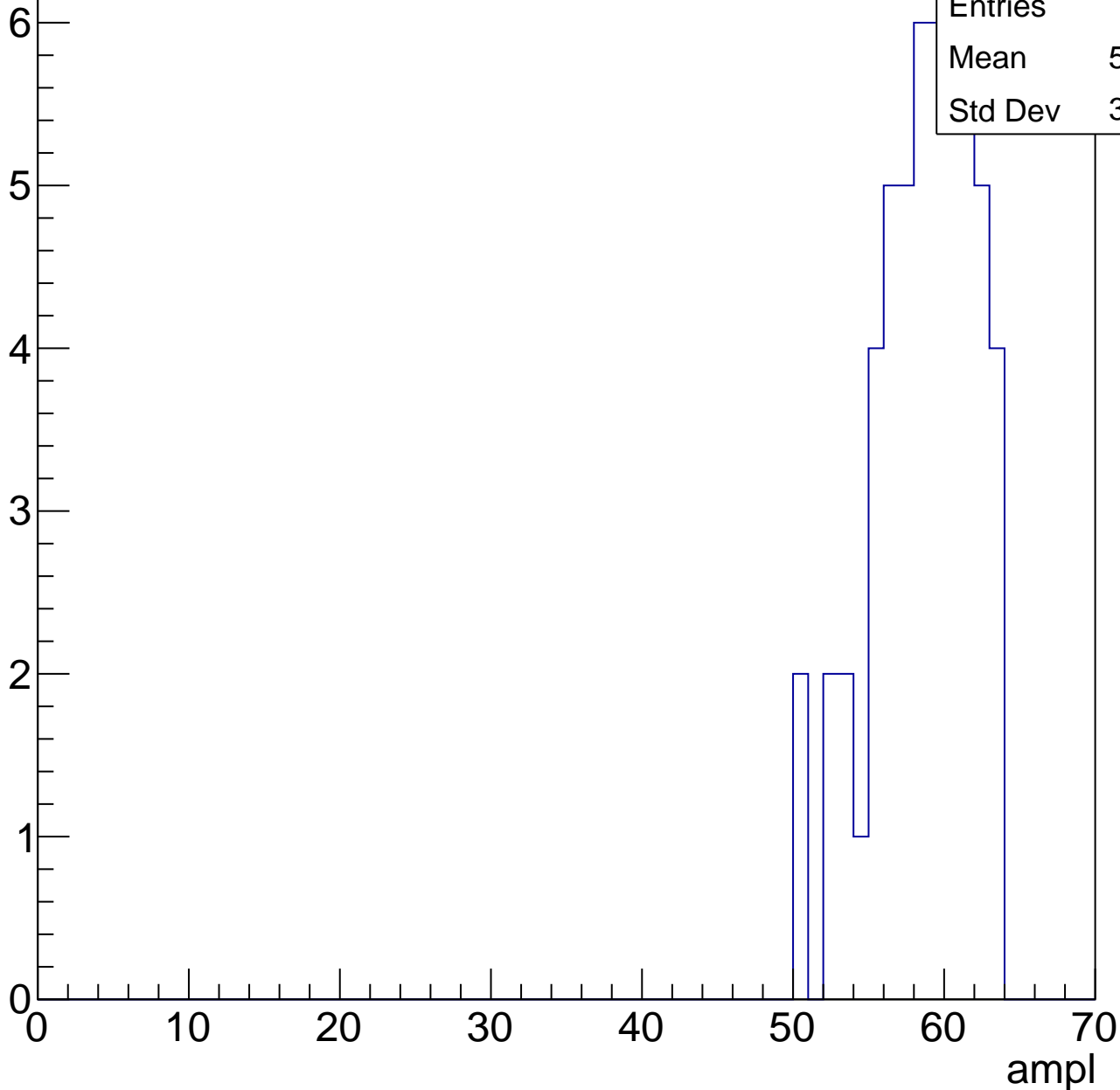


# B1L102S, U3-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	58.13
Std Dev	3.306

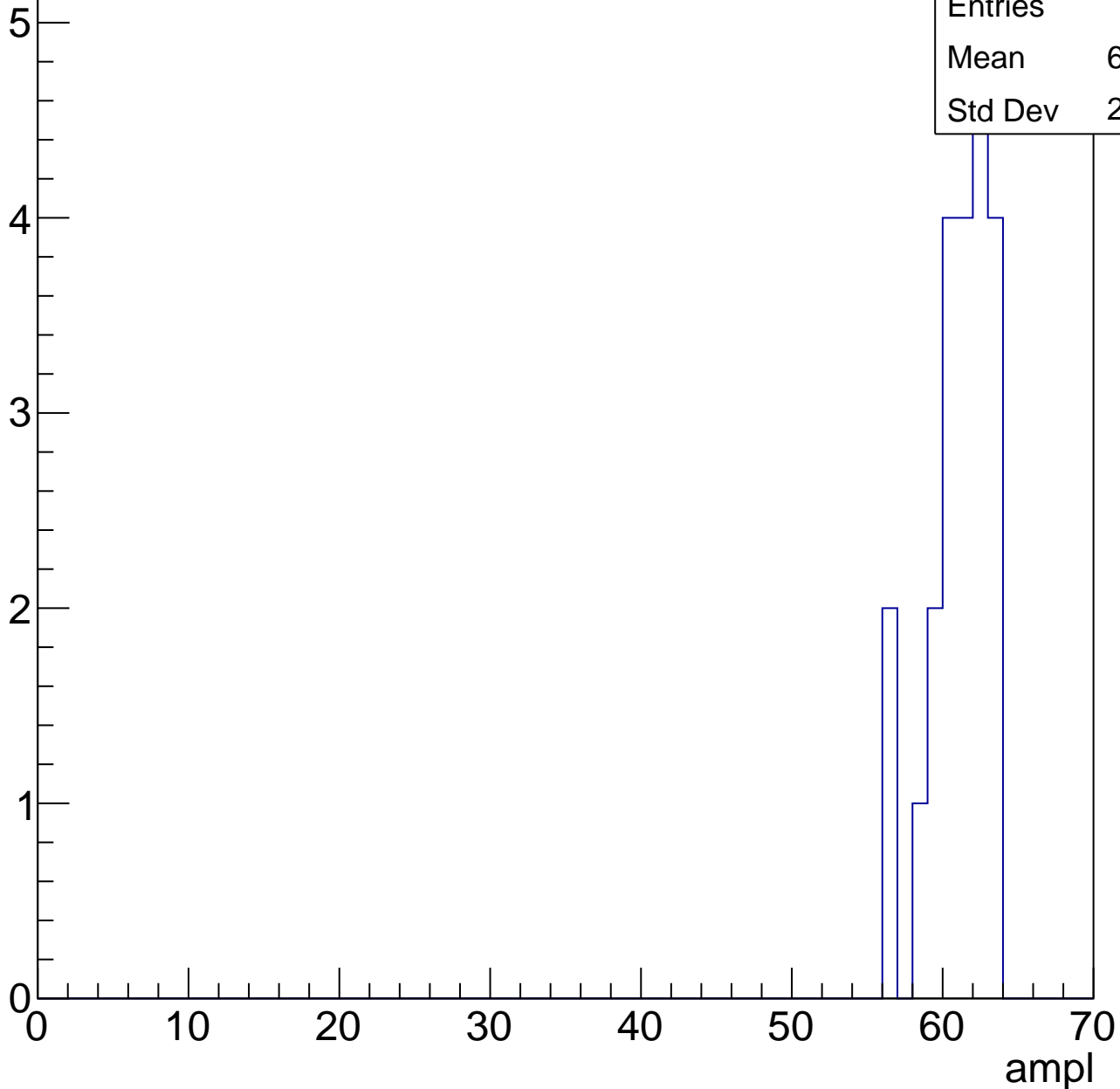


# B1L102S, U3-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	22
Mean	60.64
Std Dev	2.012





# B1L102S, U3-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch85, adc0

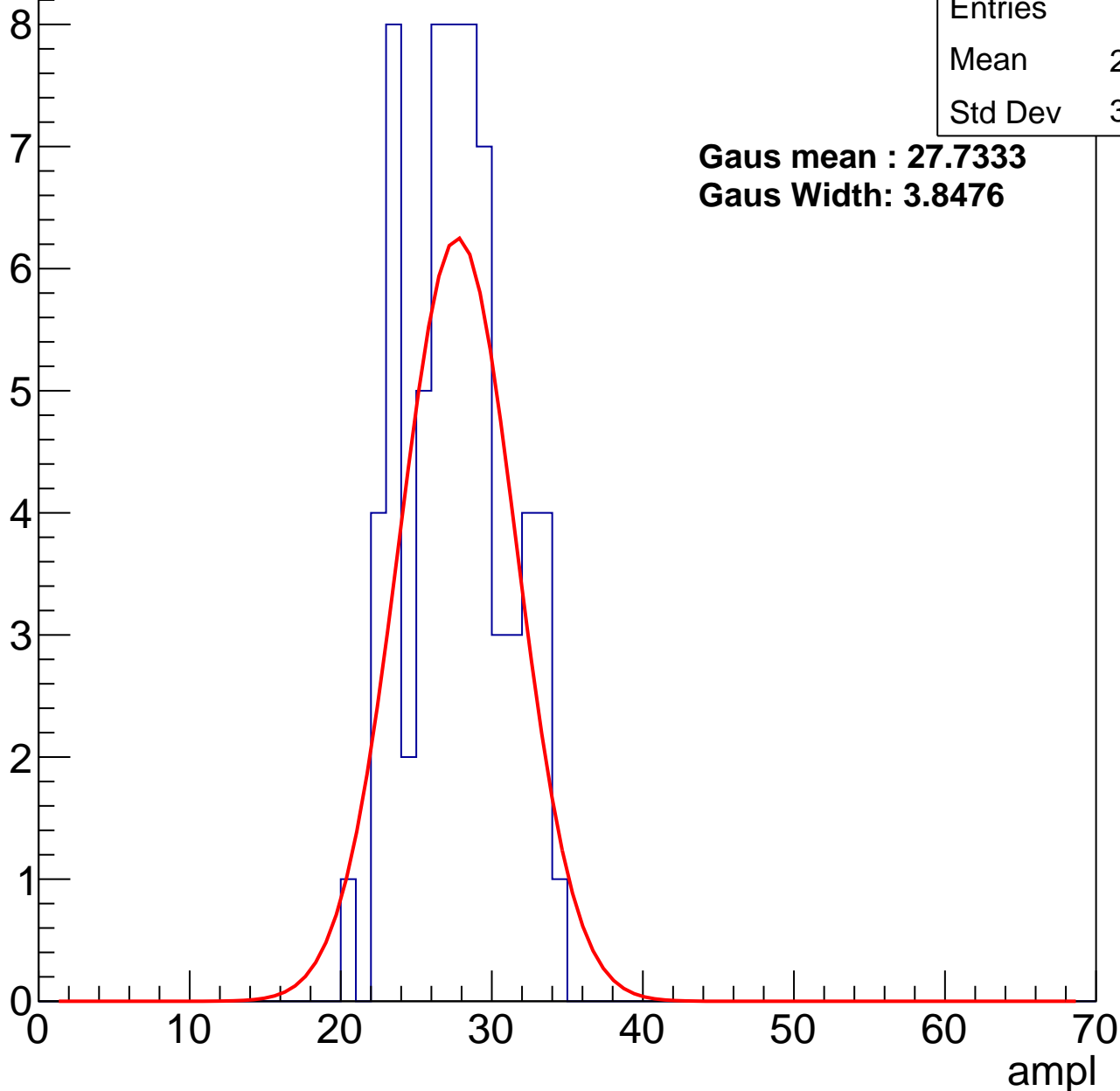
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	27.17
Std Dev	3.315

**Gaus mean : 27.7333**

**Gaus Width: 3.8476**



# B1L102S, U3-ch85, adc1

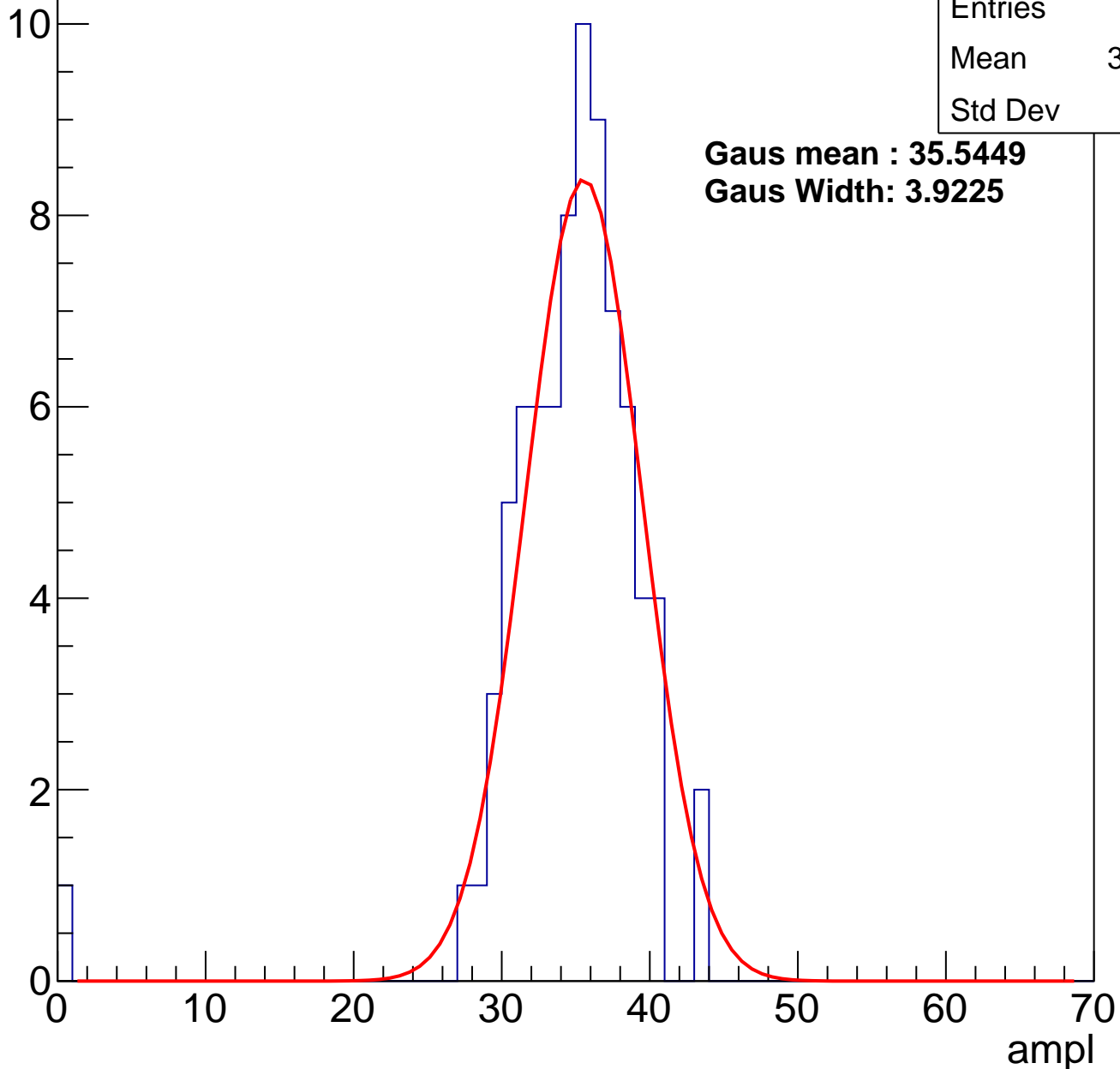
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	79
Mean	34.22
Std Dev	5.14

**Gaus mean : 35.5449**

**Gaus Width: 3.9225**

Entry



# B1L102S, U3-ch85, adc2

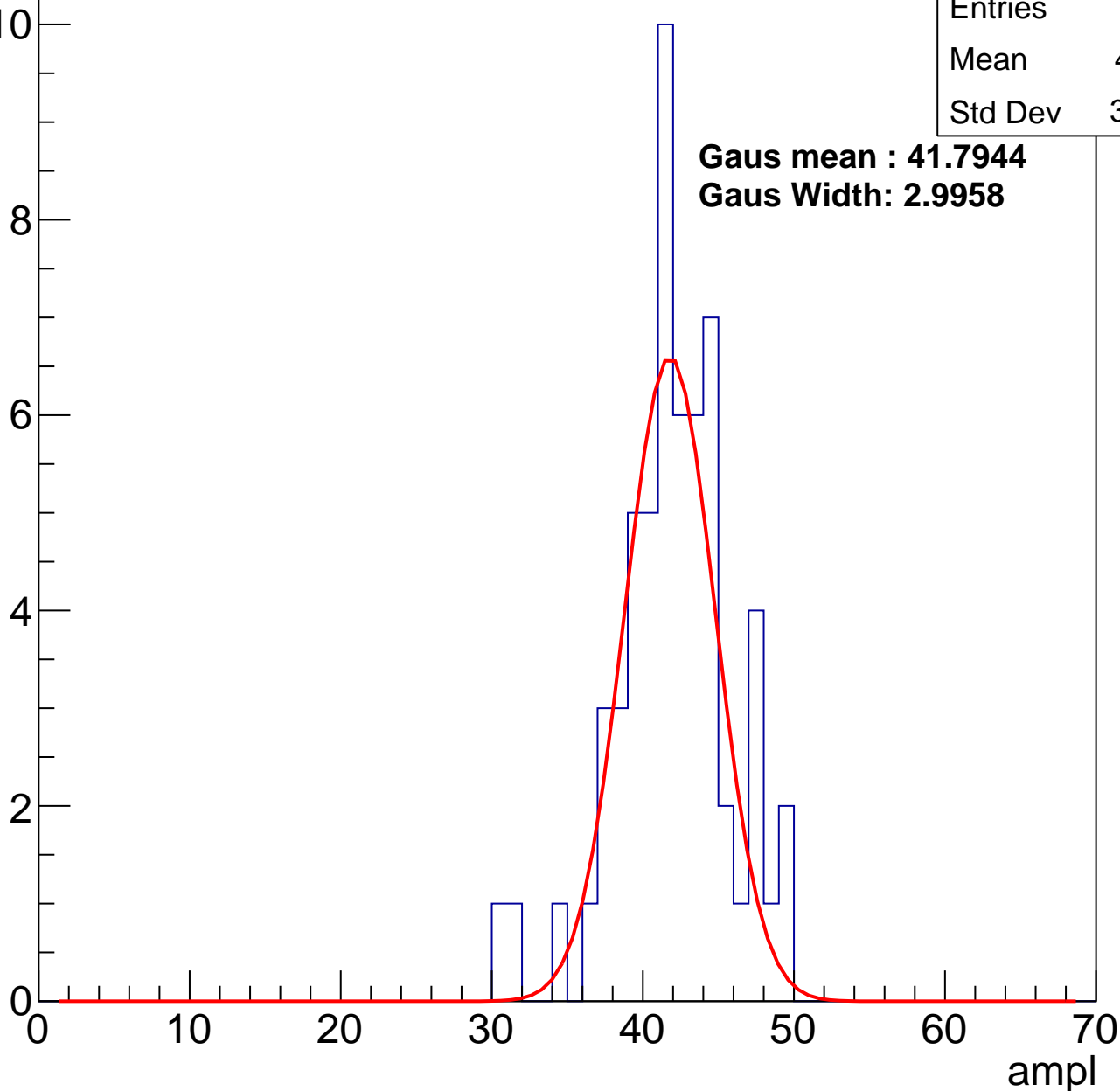
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	41.51
Std Dev	3.797

**Gaus mean : 41.7944**

**Gaus Width: 2.9958**

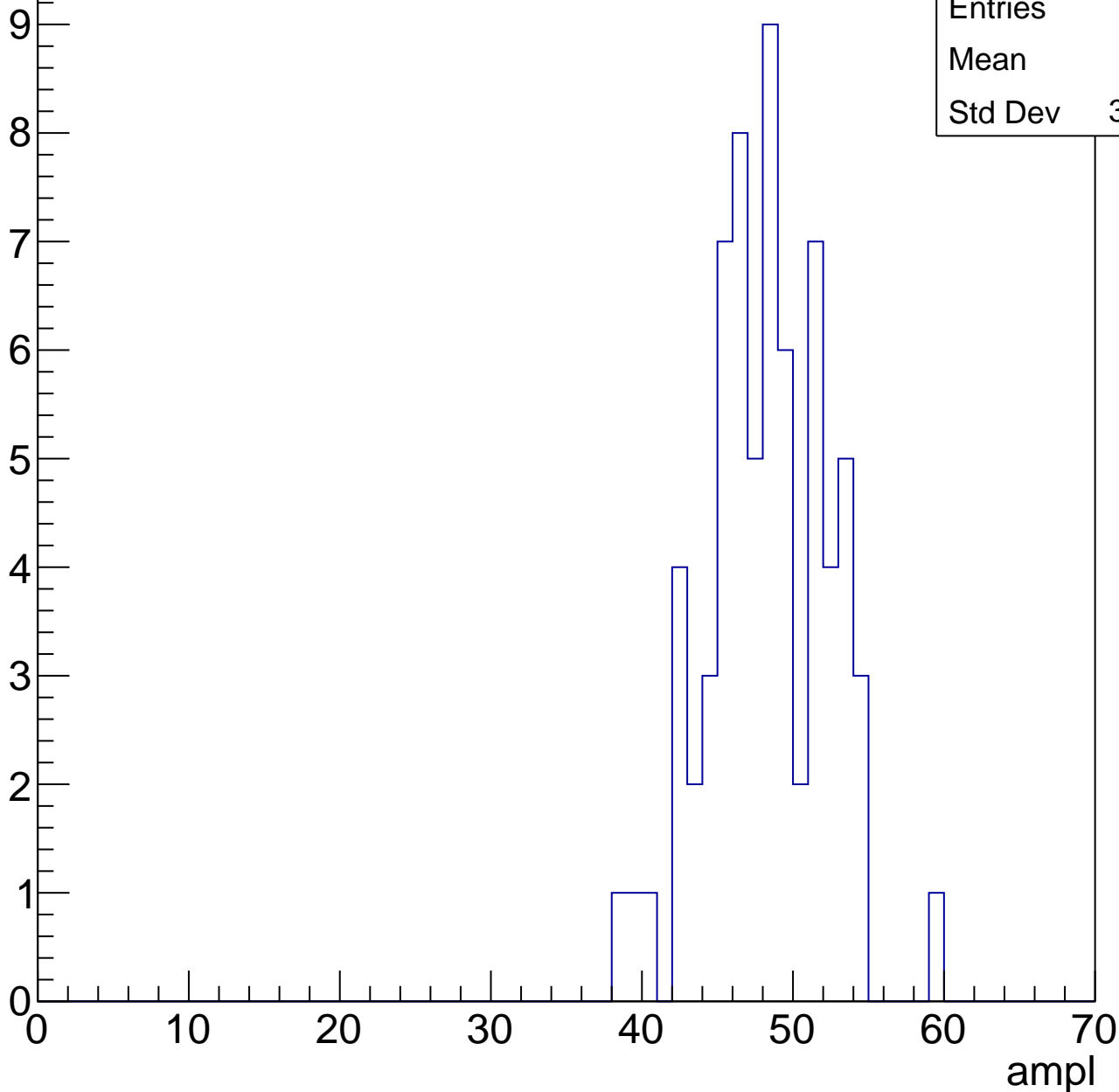


# B1L102S, U3-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	47.8
Std Dev	3.955

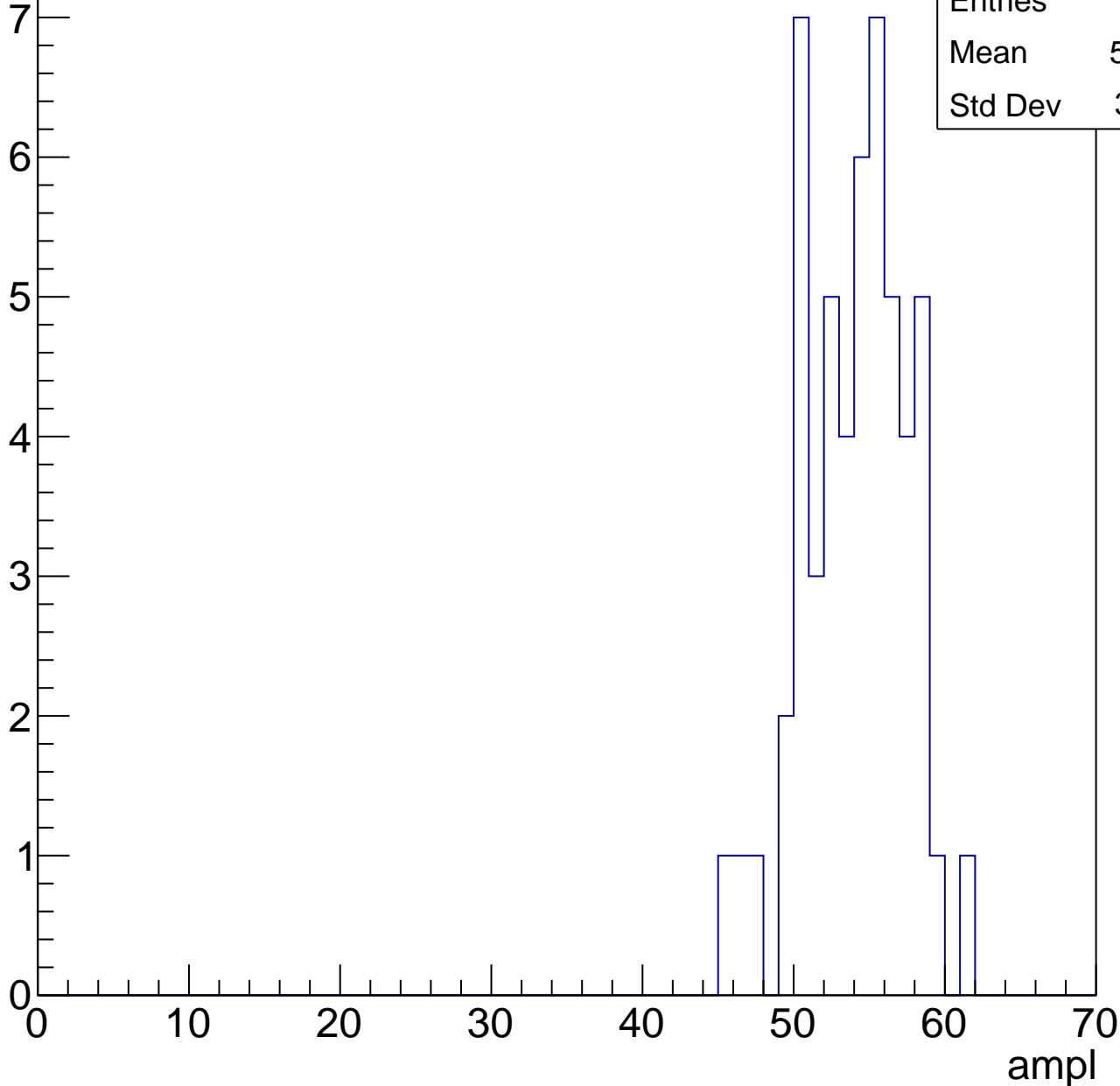


# B1L102S, U3-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	53.55
Std Dev	3.401



# B1L102S, U3-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

7

6

5

4

3

2

1

0

Entries 49

Mean 58.61

Std Dev 2.926

ampl

0

10

20

30

40

50

60

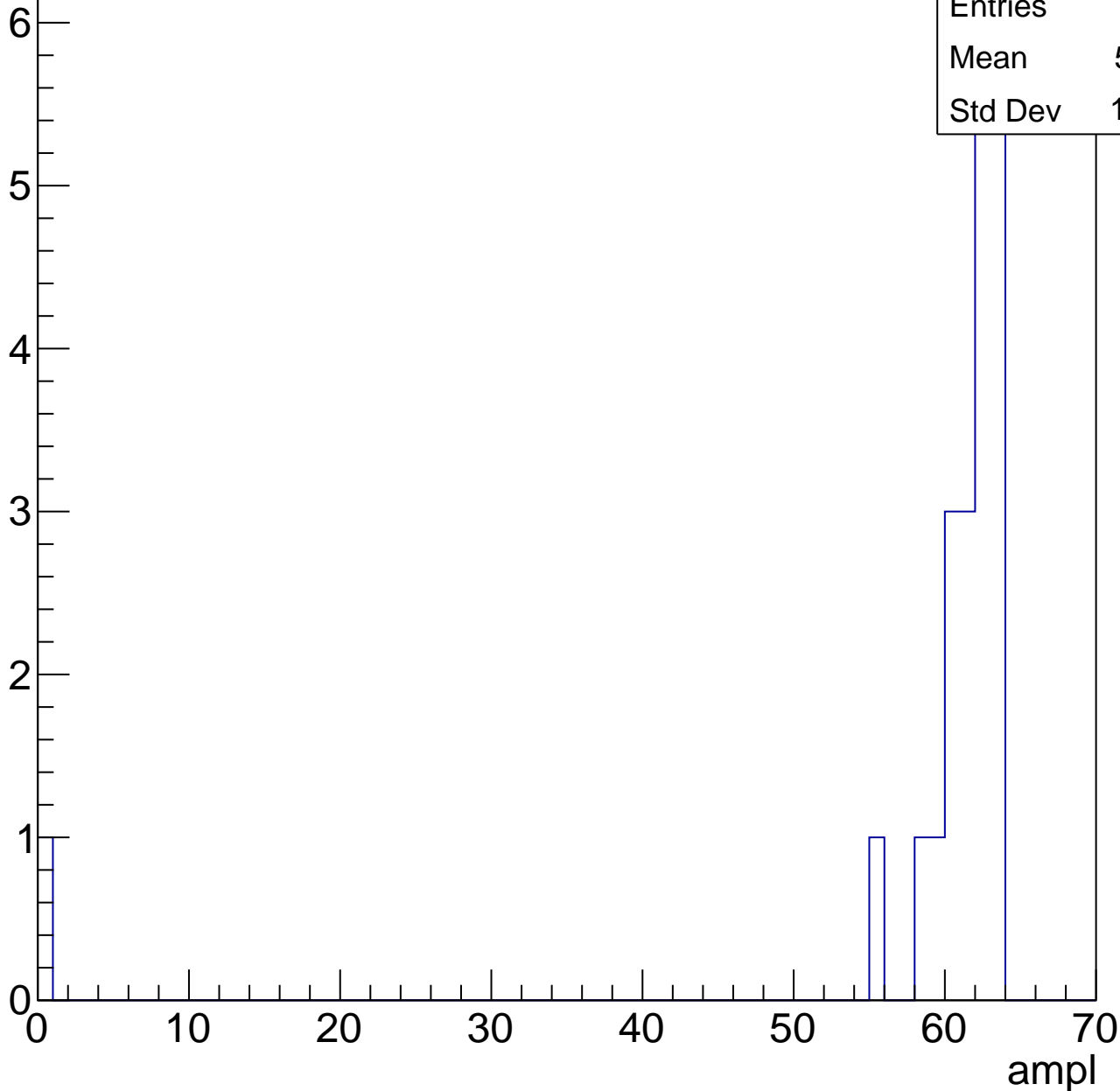
70

# B1L102S, U3-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	22
Mean	58.41
Std Dev	12.89





# B1L102S, U3-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch86, adc0

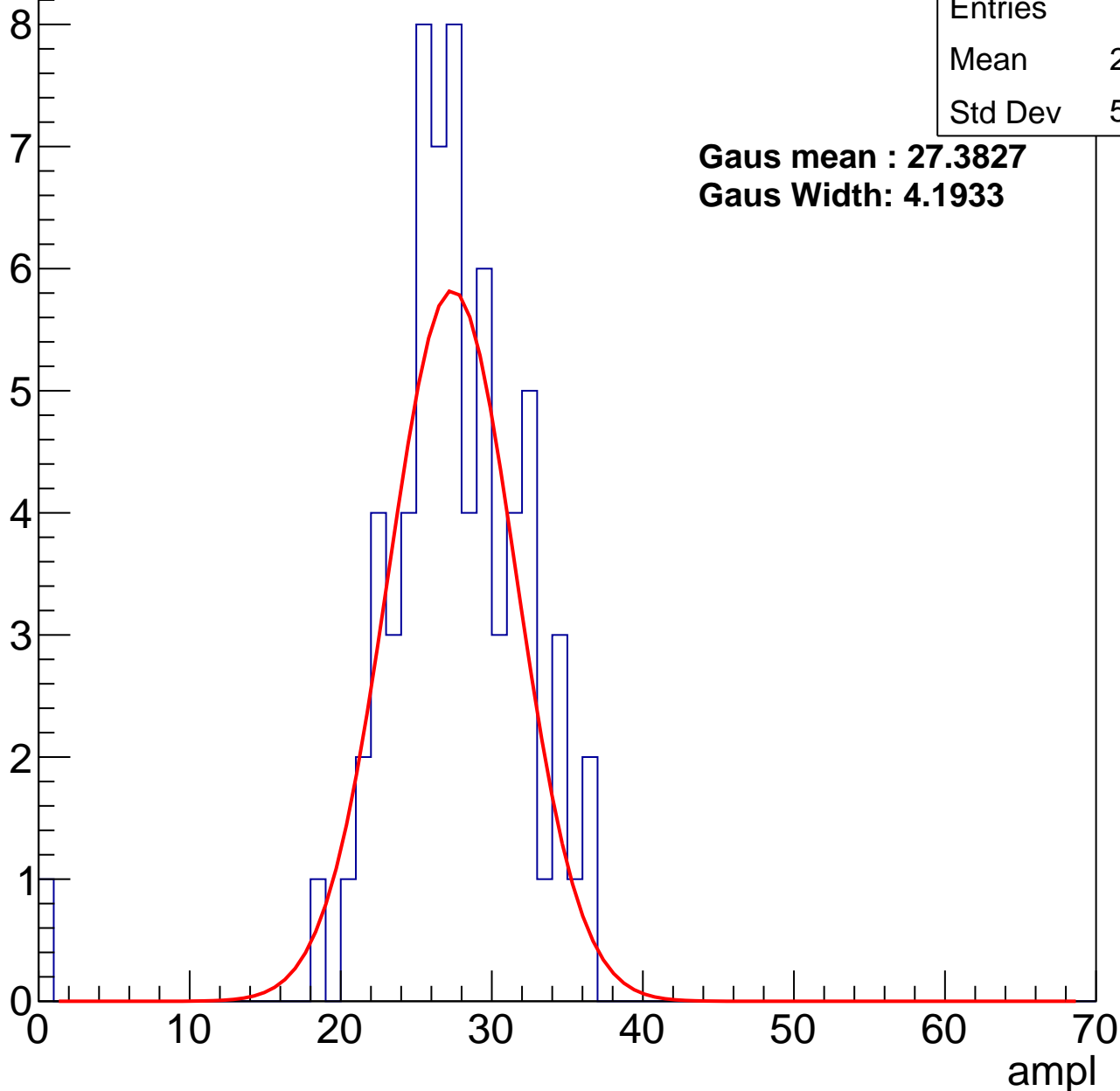
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	26.96
Std Dev	5.155

**Gaus mean : 27.3827**

**Gaus Width: 4.1933**



# B1L102S, U3-ch86, adc1

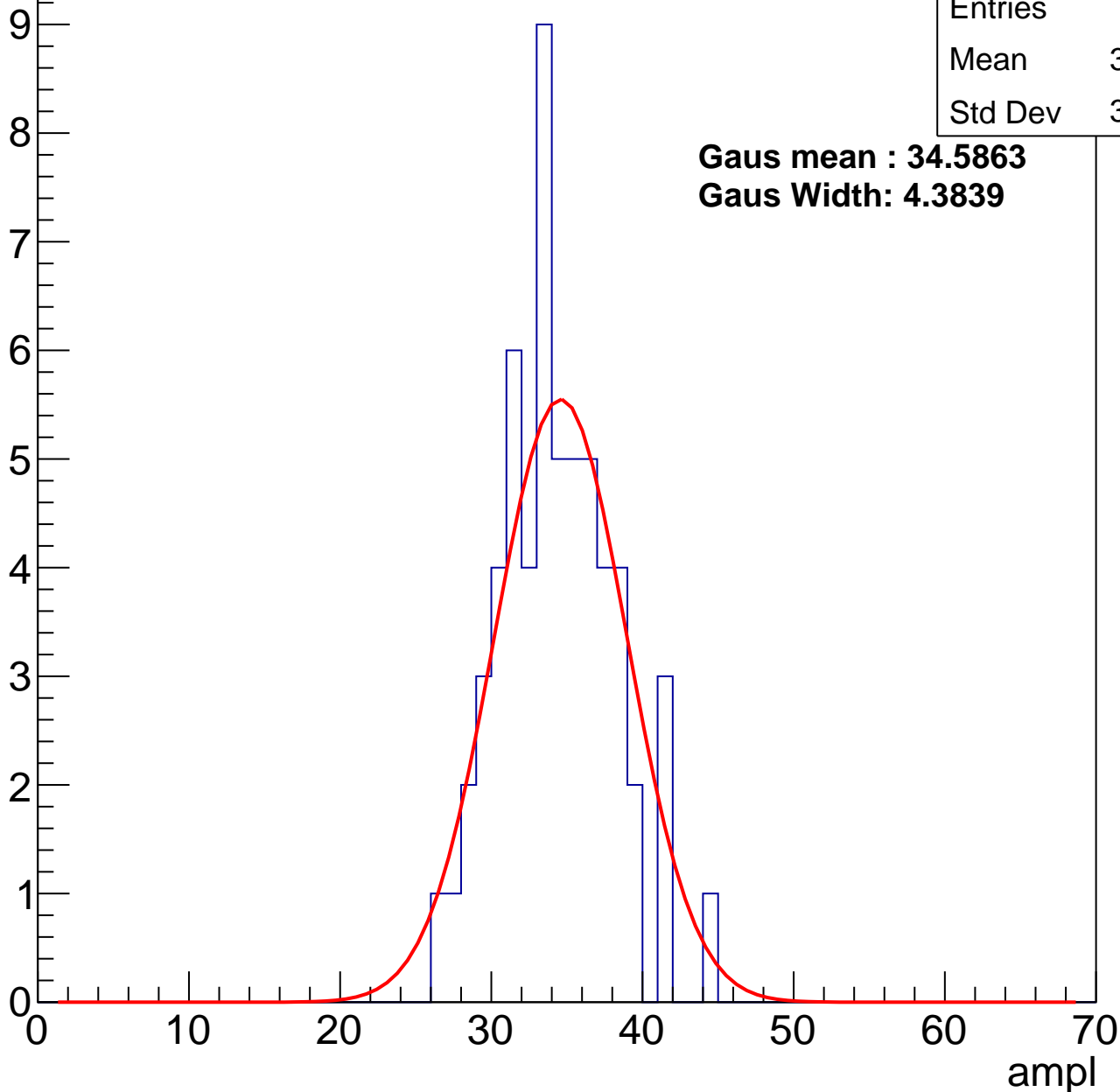
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	33.85
Std Dev	3.736

**Gaus mean : 34.5863**

**Gaus Width: 4.3839**



# B1L102S, U3-ch86, adc2

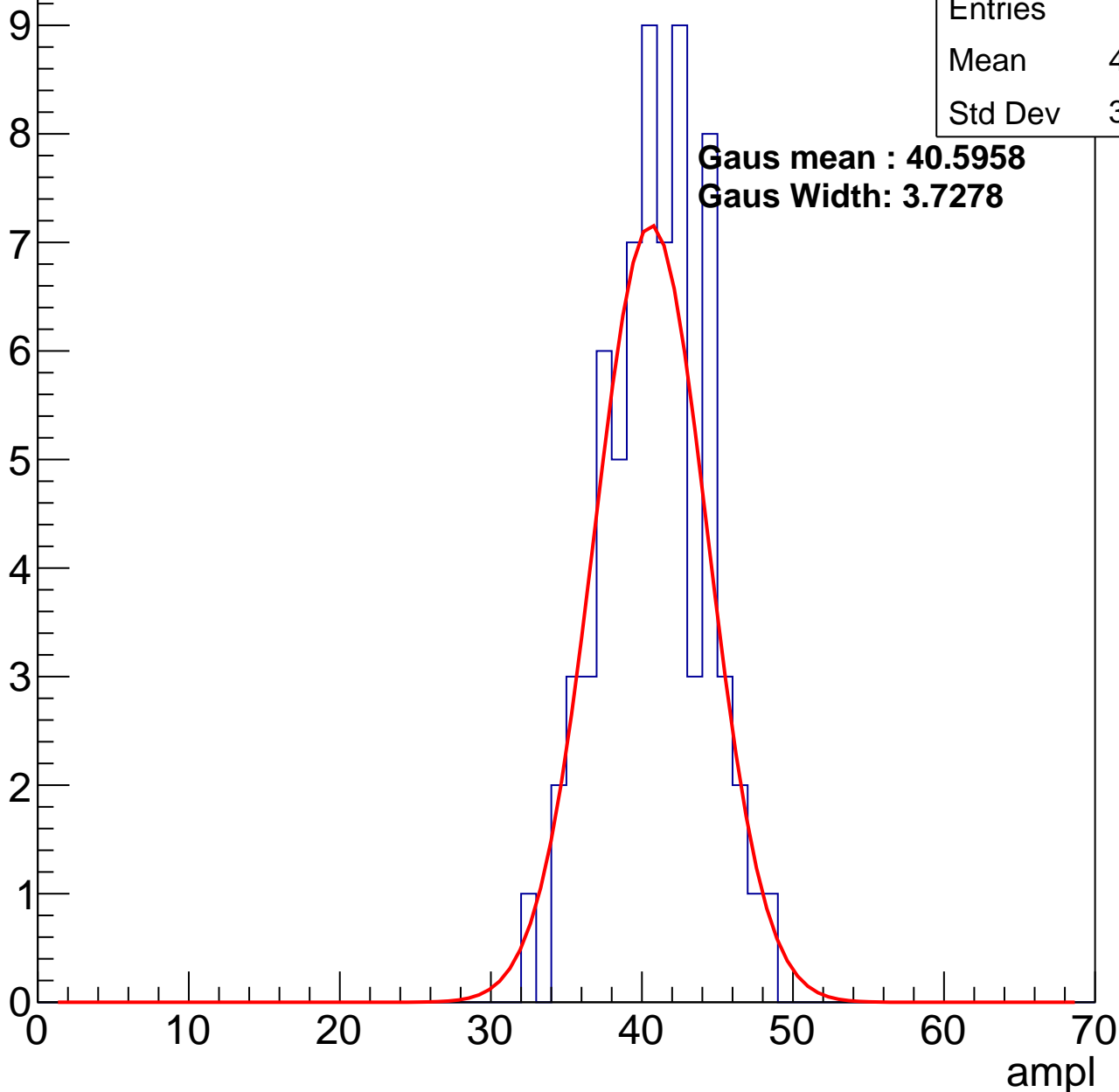
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	40.37
Std Dev	3.356

**Gaus mean : 40.5958**

**Gaus Width: 3.7278**

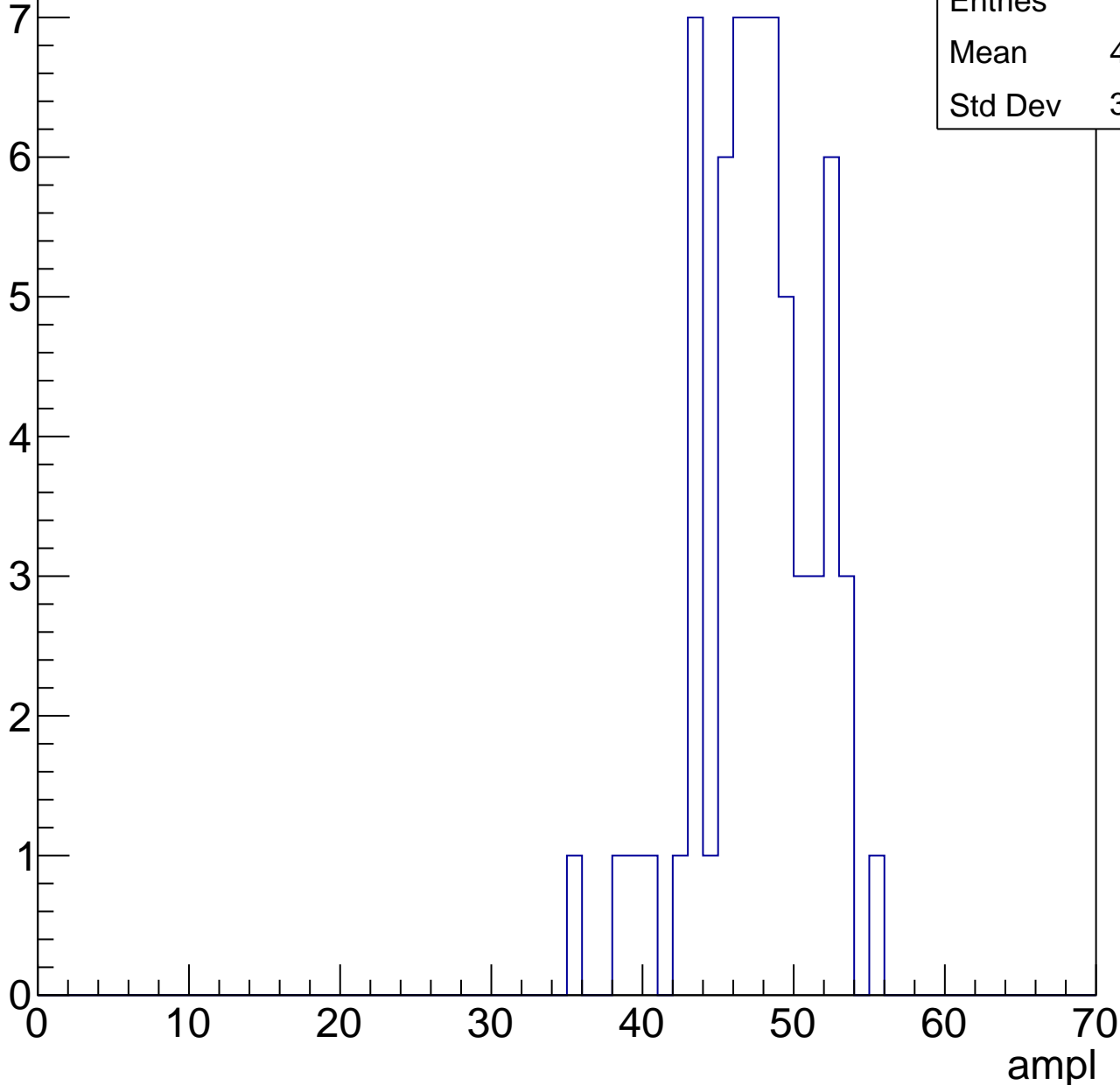


# B1L102S, U3-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	47.05
Std Dev	3.923

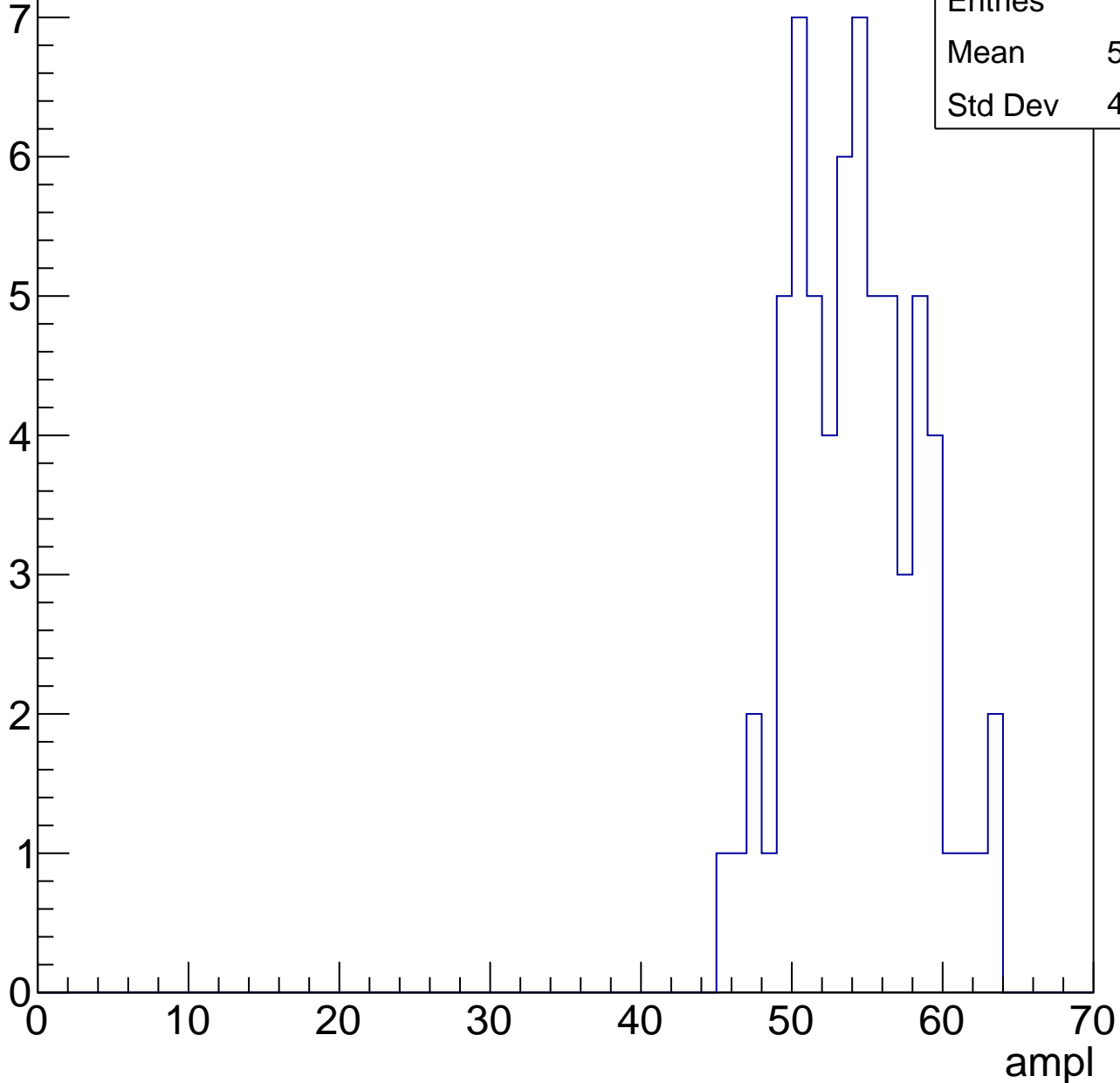


# B1L102S, U3-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	53.76
Std Dev	4.123

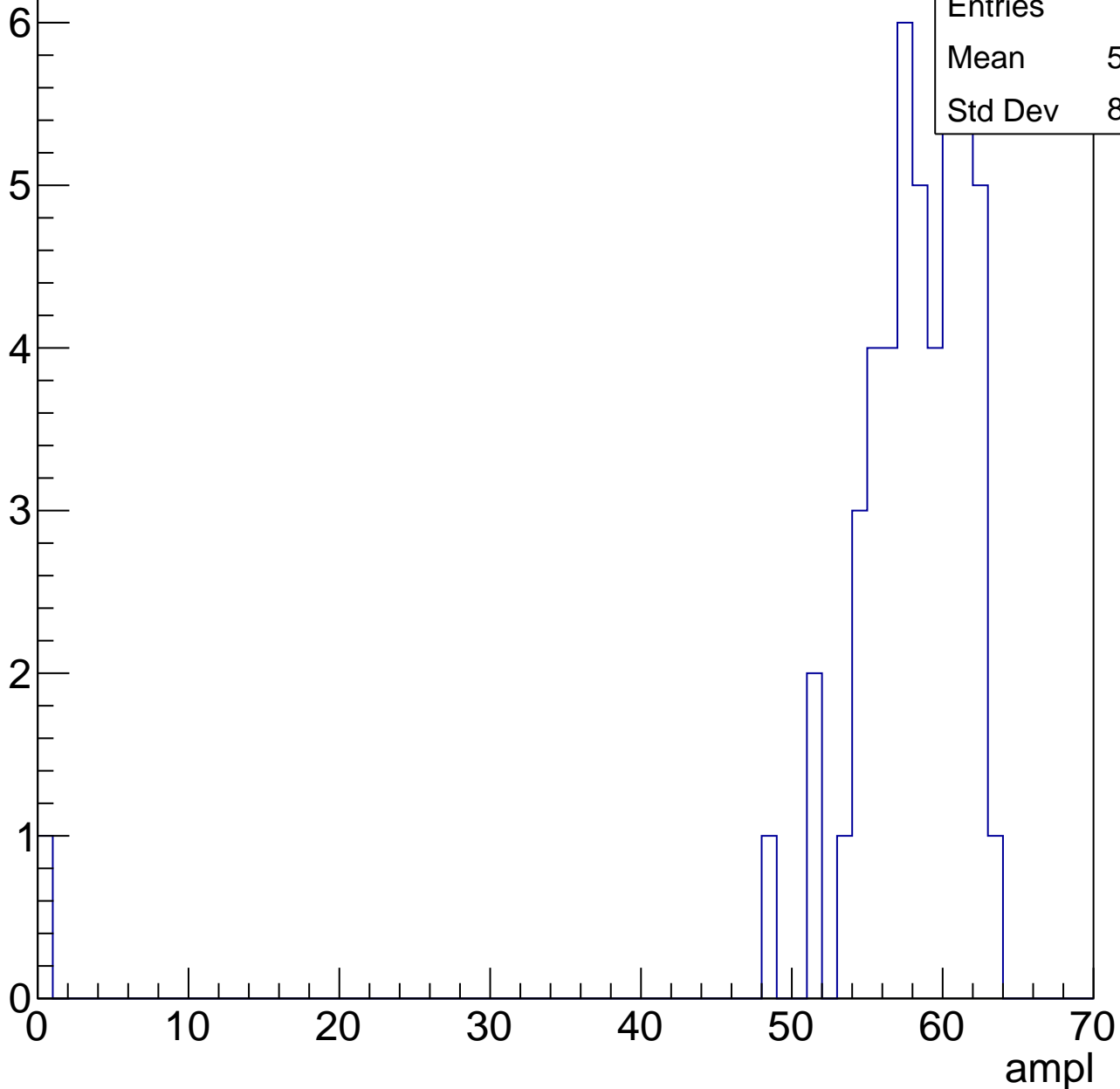


# B1L102S, U3-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	56.65
Std Dev	8.796

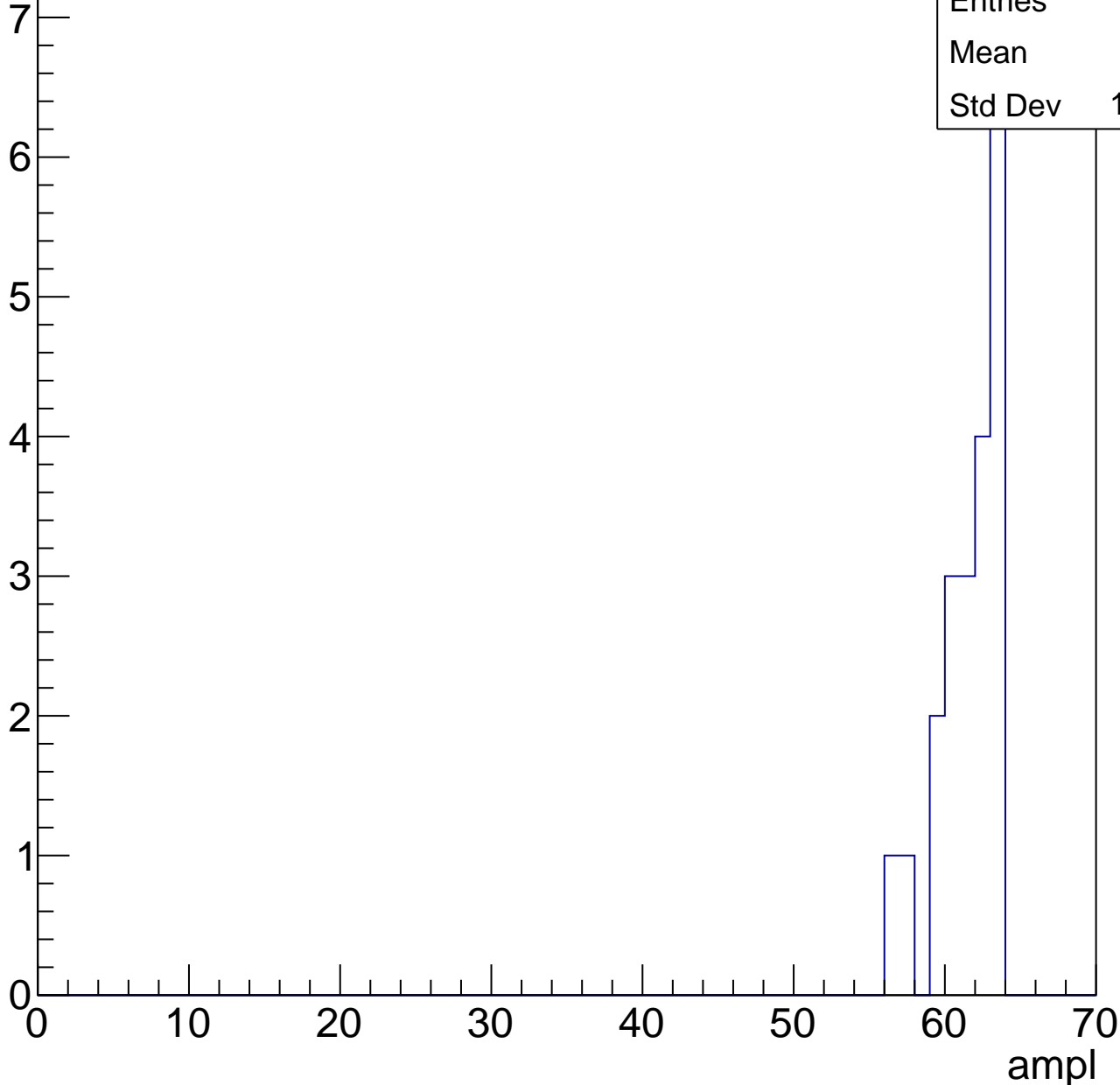


# B1L102S, U3-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	21
Mean	61.1
Std Dev	1.998





# B1L102S, U3-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch87, adc0

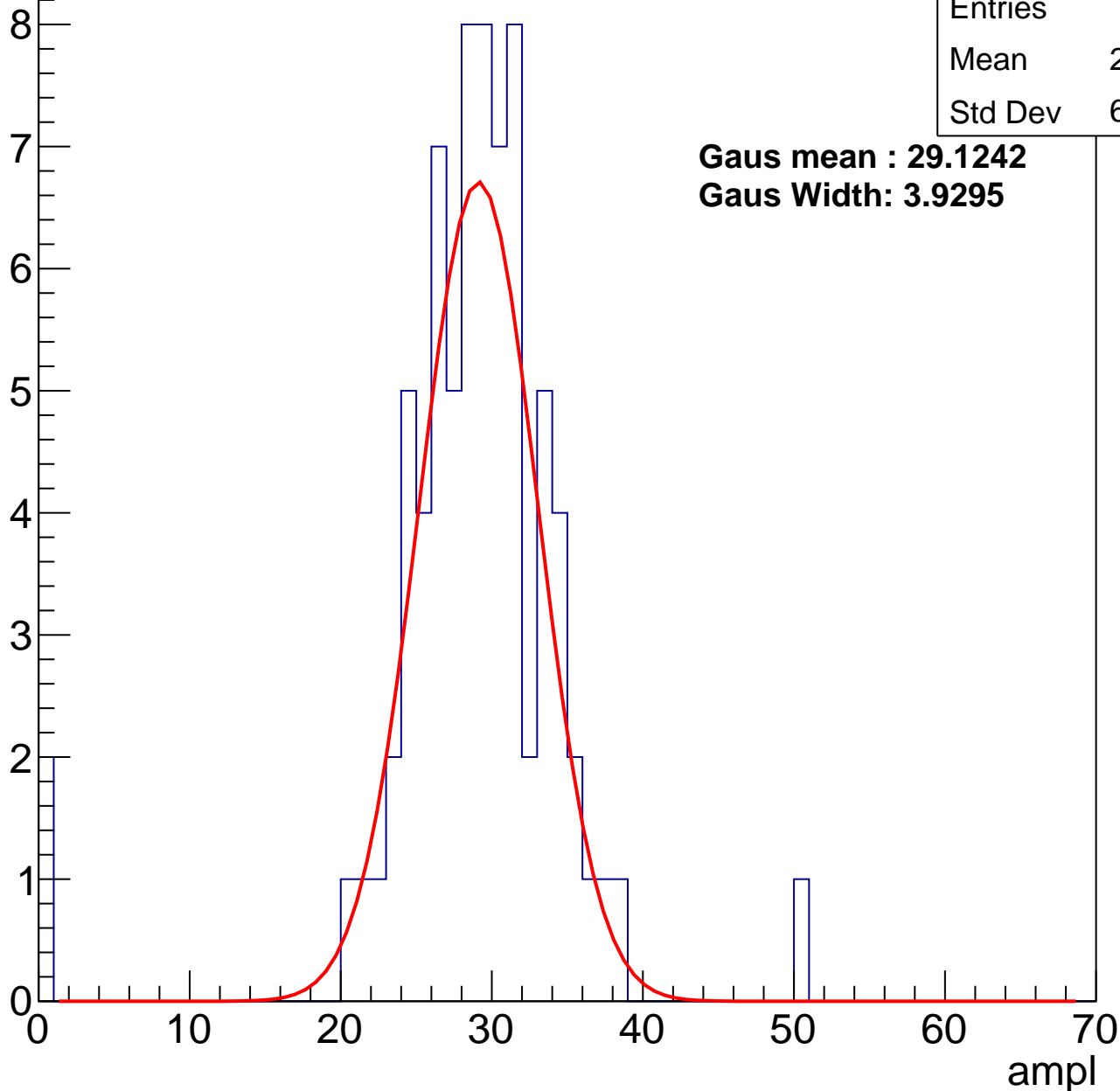
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	28.37
Std Dev	6.429

**Gaus mean : 29.1242**

**Gaus Width: 3.9295**



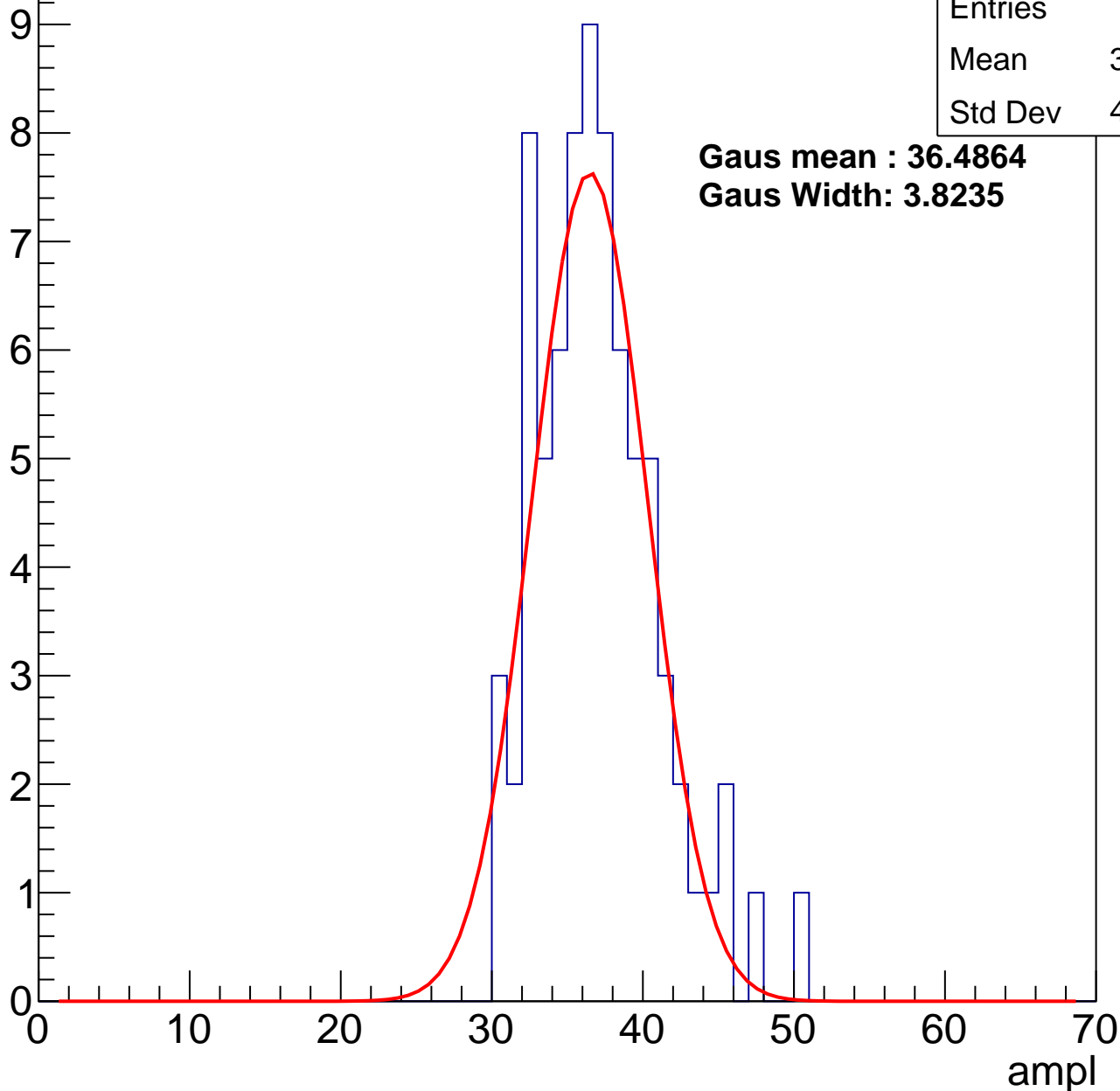
# B1L102S, U3-ch87, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	36.59
Std Dev	4.027

**Gaus mean : 36.4864**  
**Gaus Width: 3.8235**



# B1L102S, U3-ch87, adc2

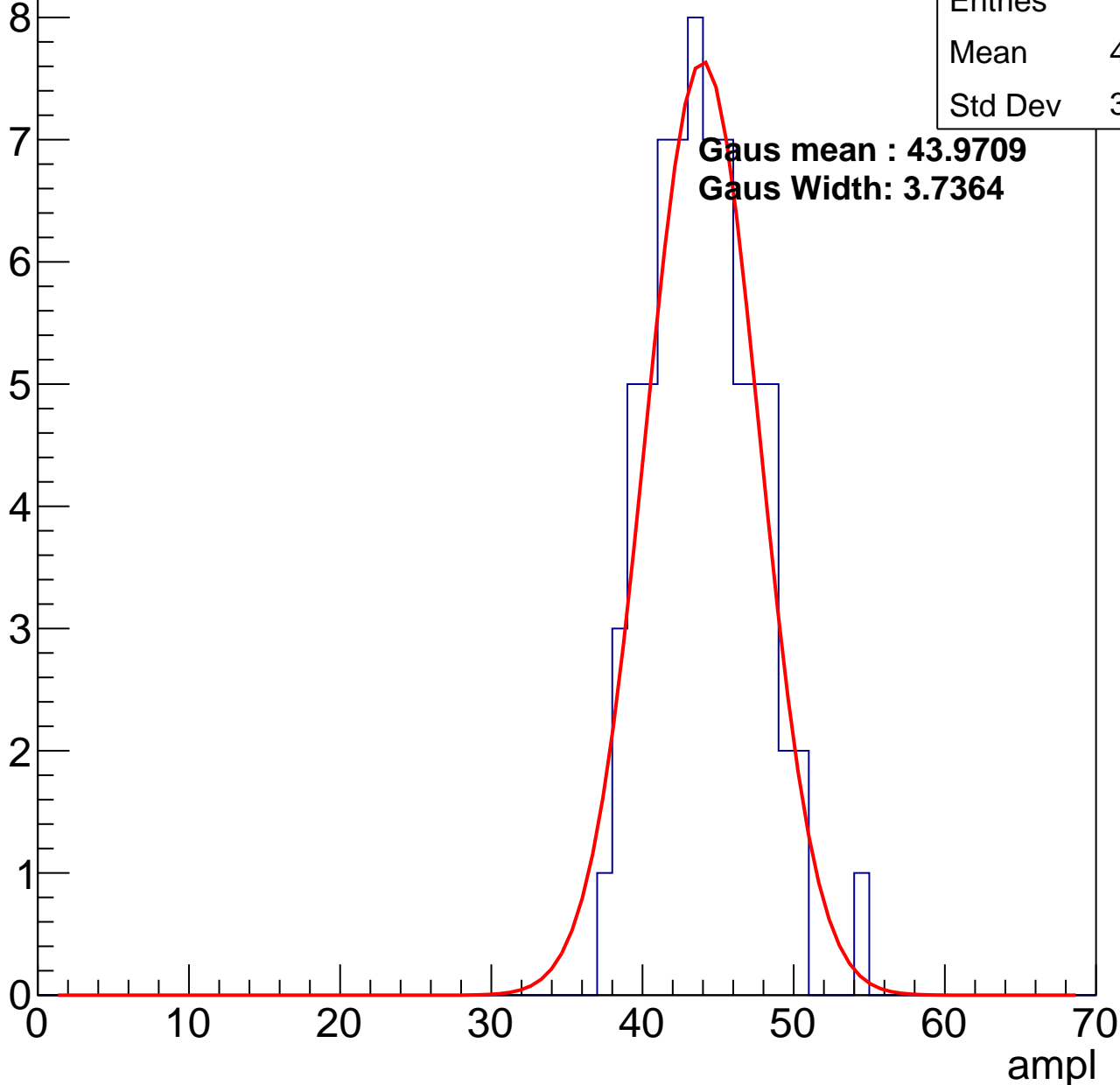
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	43.59
Std Dev	3.429

**Gaus mean : 43.9709**

**Gaus Width: 3.7364**

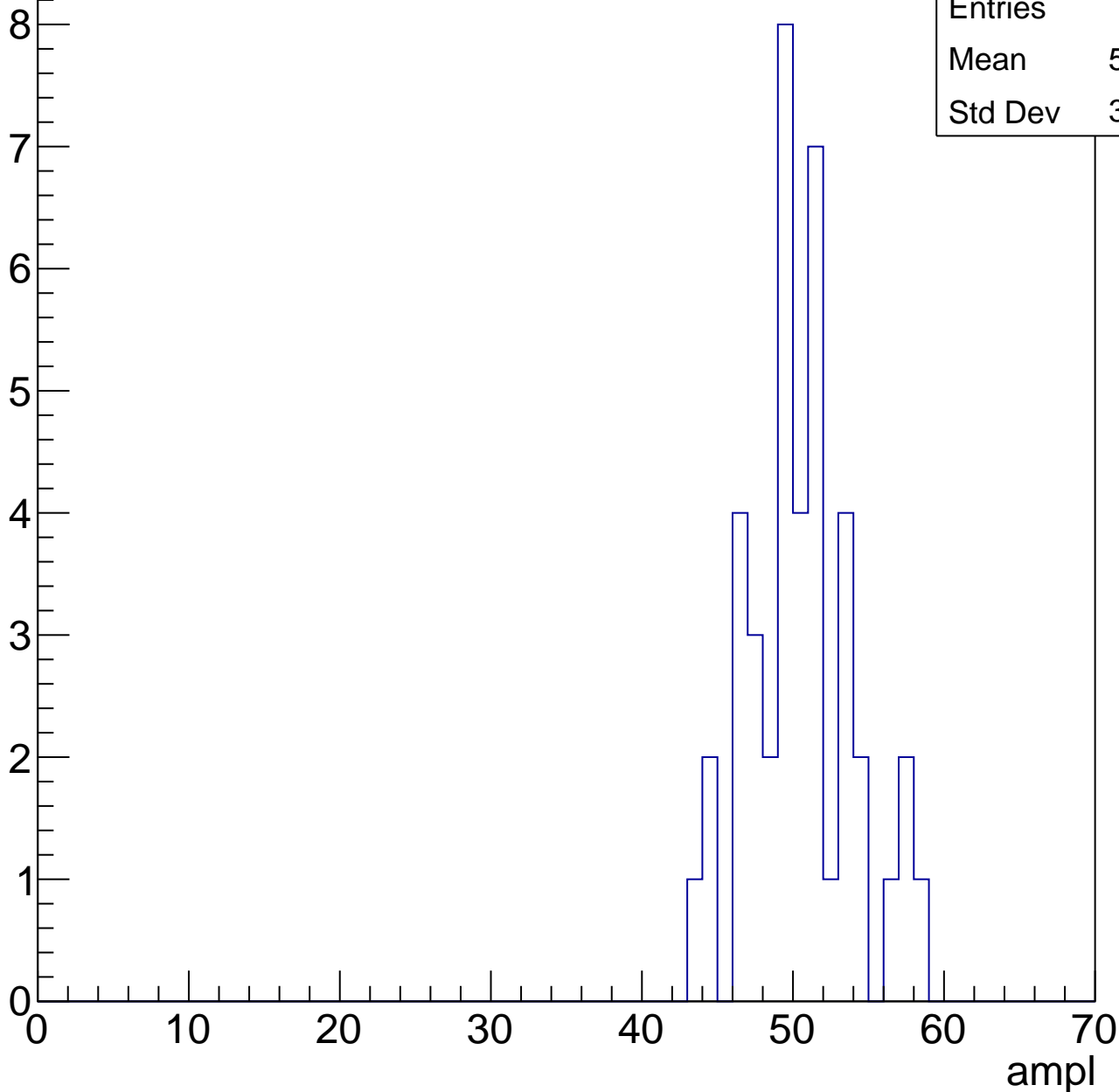


# B1L102S, U3-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	42
Mean	50.02
Std Dev	3.467

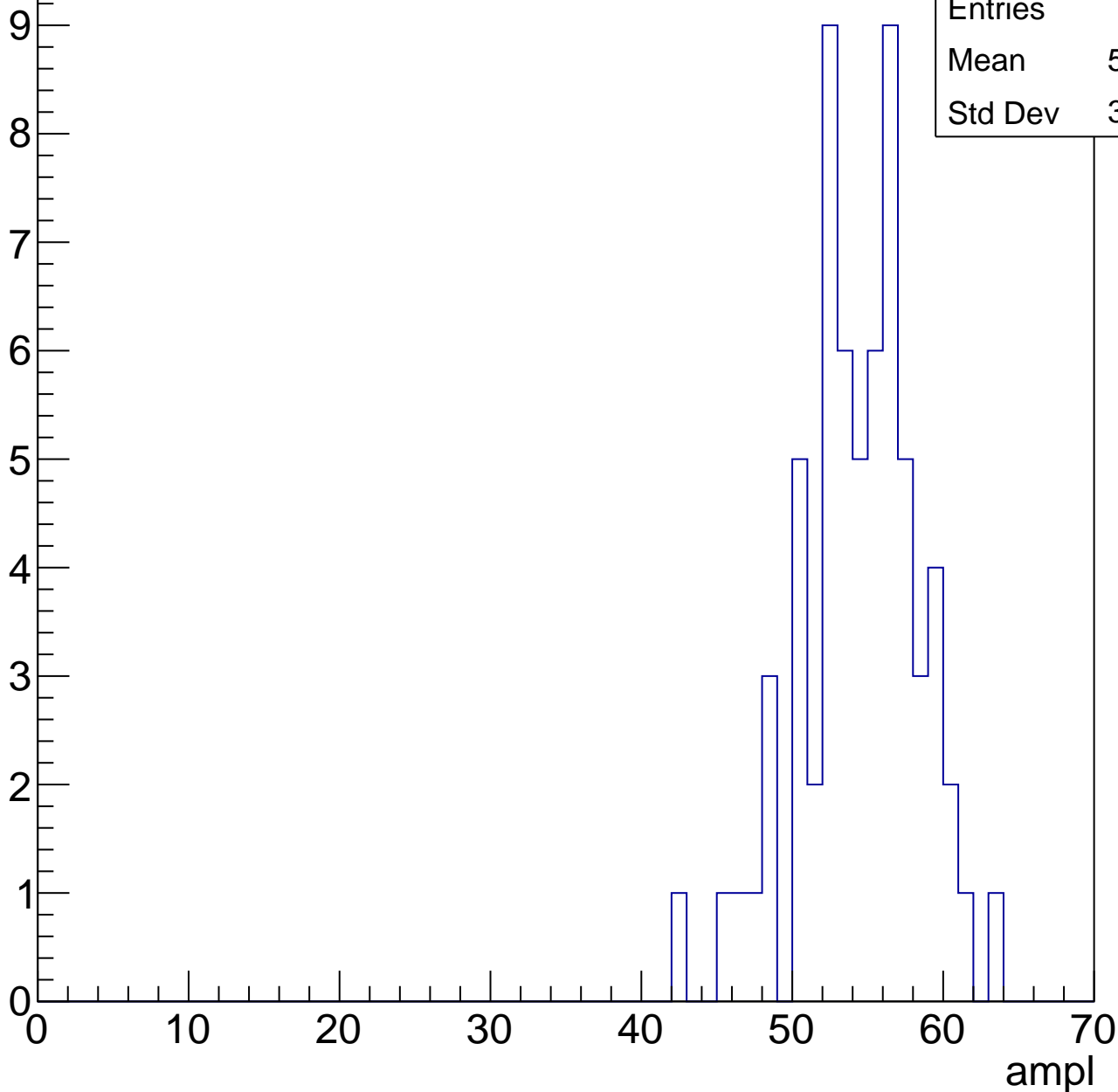


# B1L102S, U3-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	53.92
Std Dev	3.966

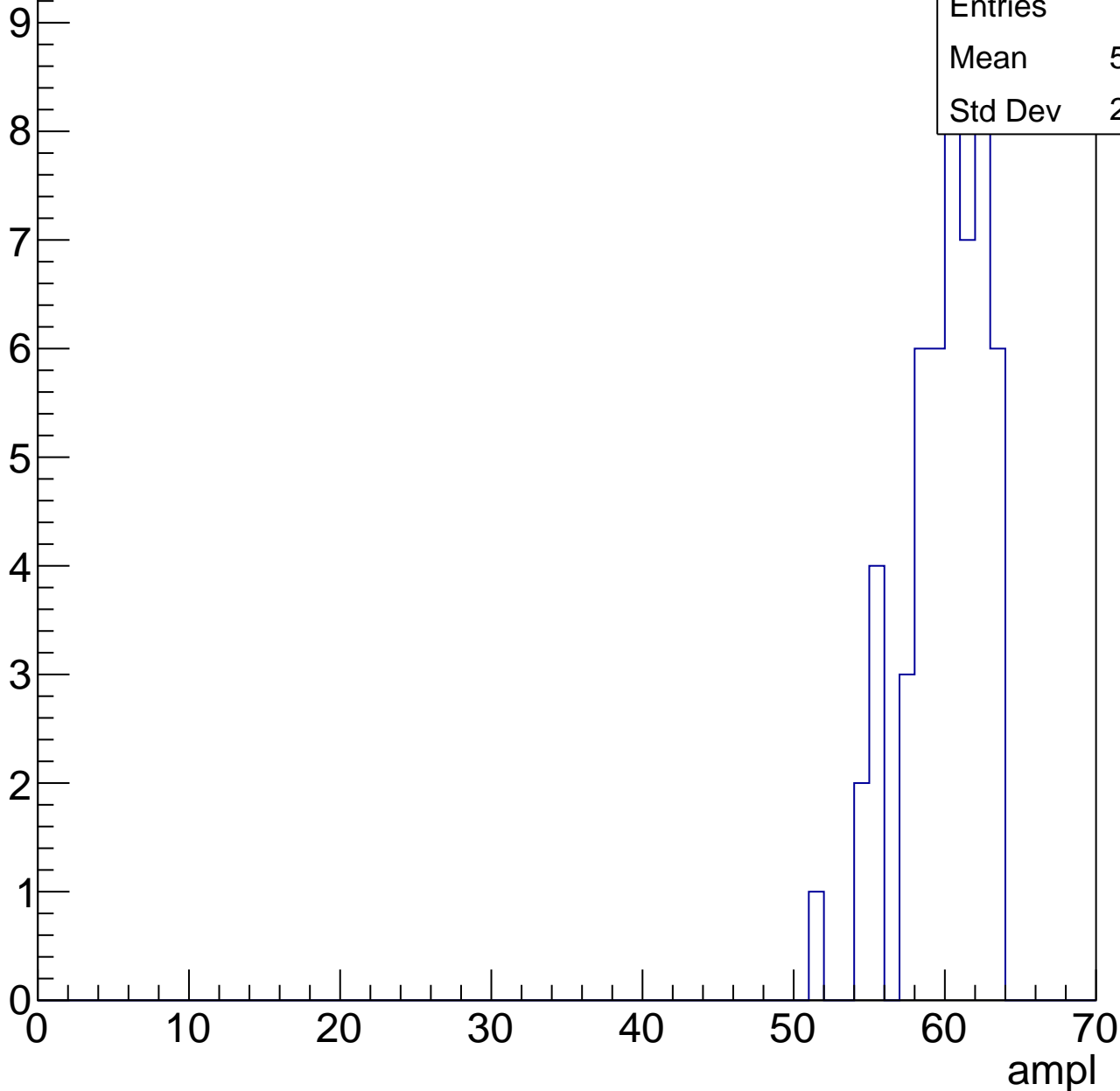


# B1L102S, U3-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

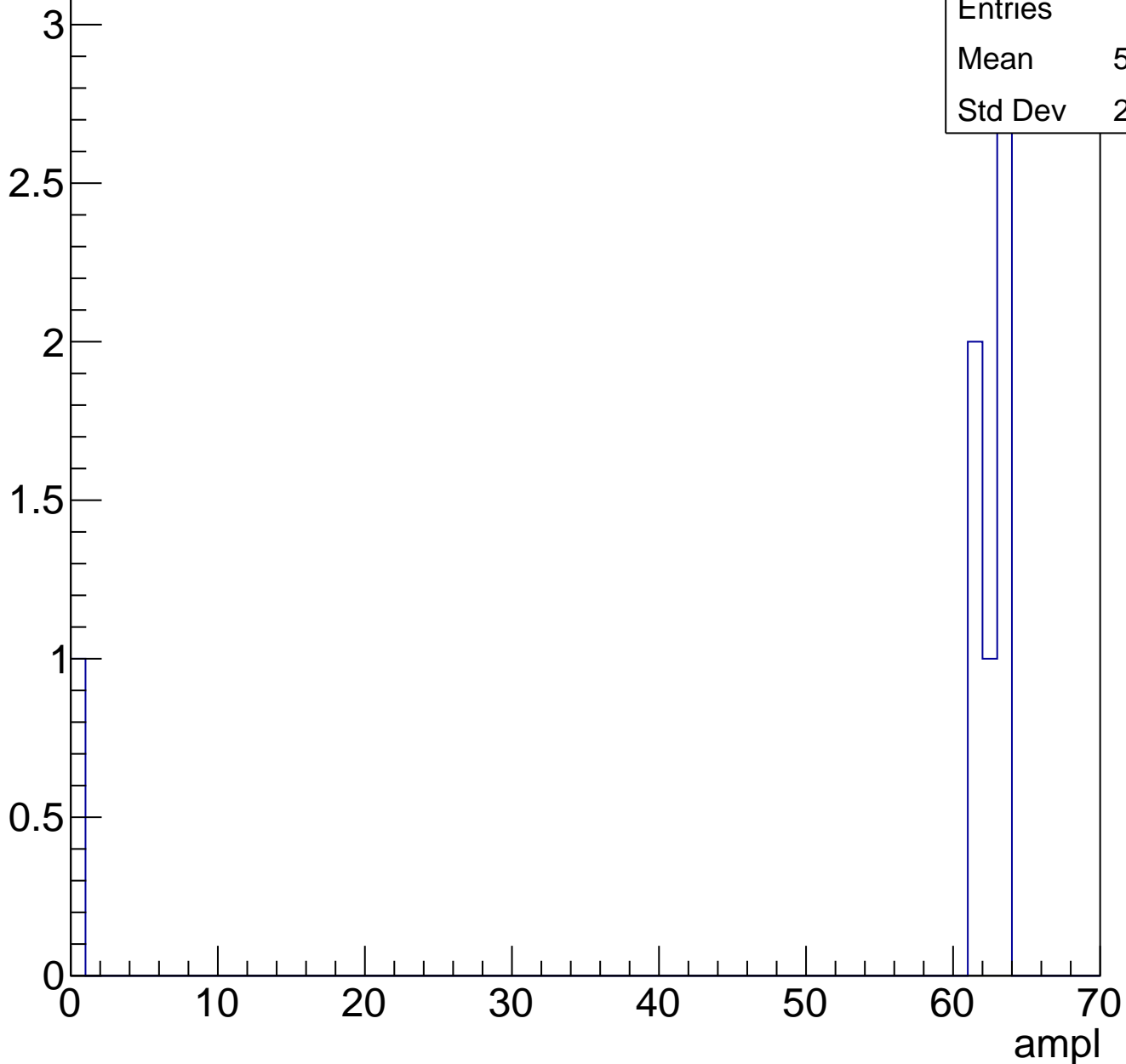
Entries	52
Mean	59.52
Std Dev	2.756



# B1L102S, U3-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch88, adc0

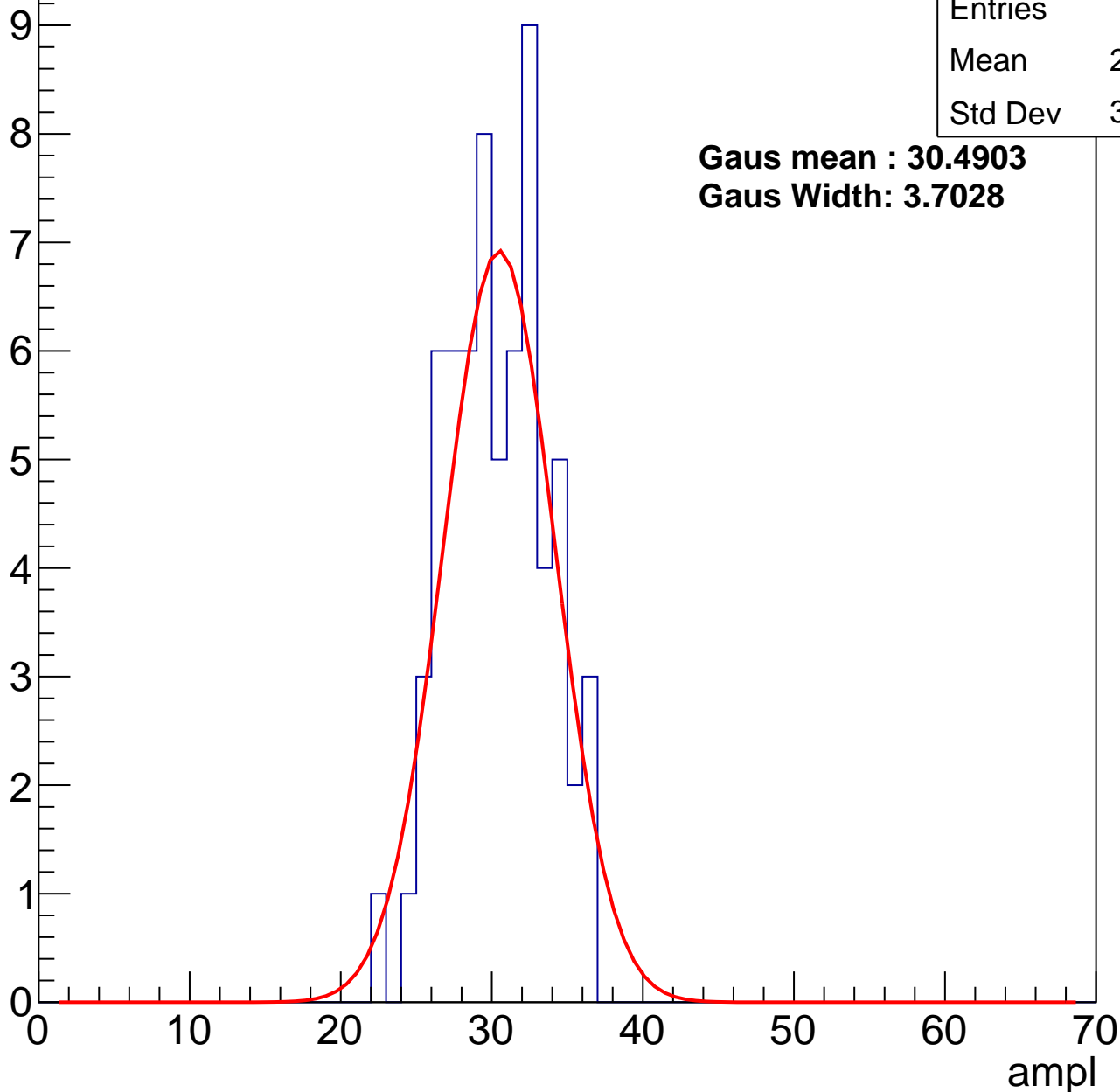
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	29.89
Std Dev	3.216

**Gaus mean : 30.4903**

**Gaus Width: 3.7028**



# B1L102S, U3-ch88, adc1

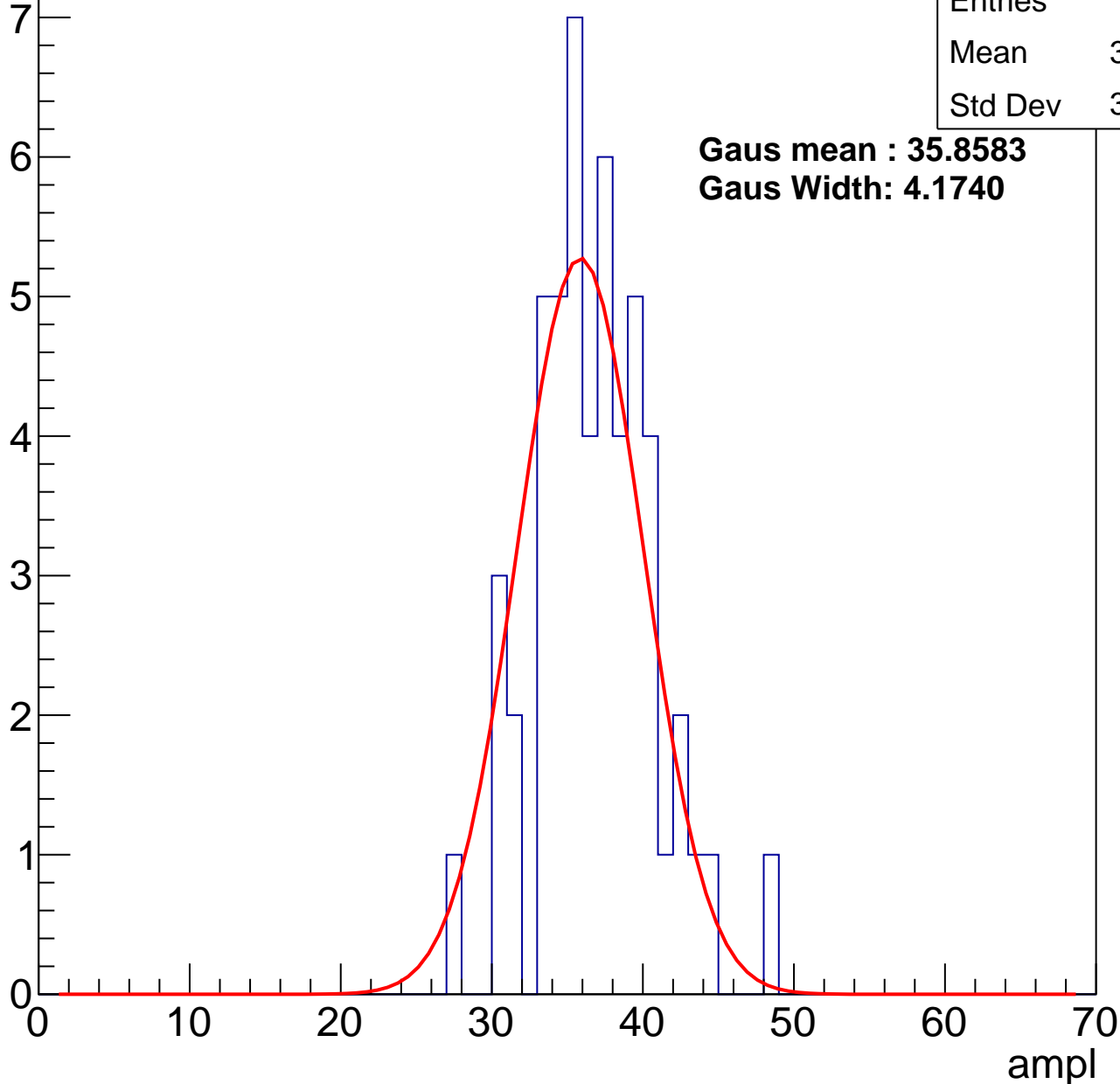
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	36.38
Std Dev	3.894

**Gaus mean : 35.8583**

**Gaus Width: 4.1740**



# B1L102S, U3-ch88, adc2

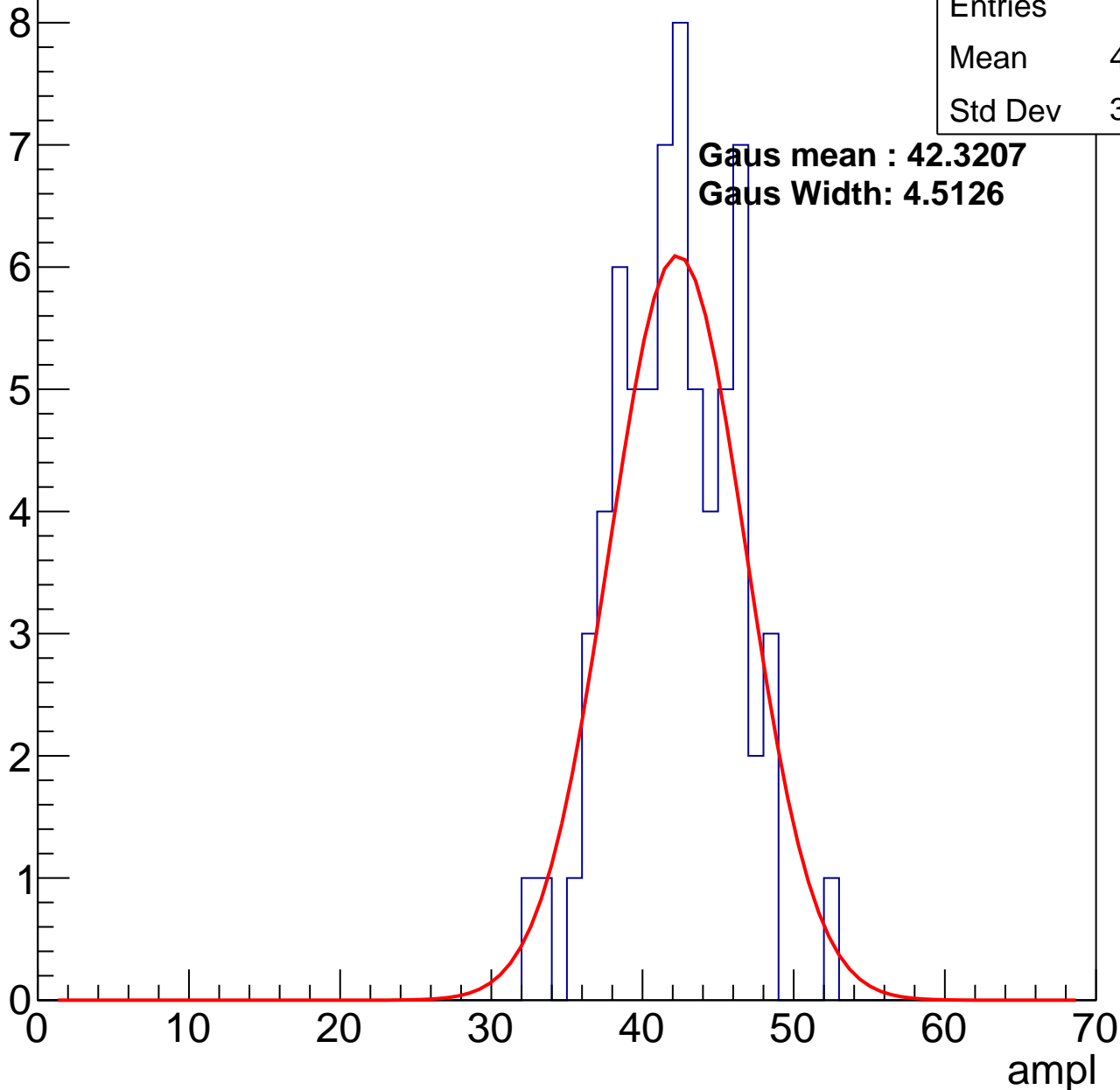
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	41.62
Std Dev	3.896

**Gaus mean : 42.3207**

**Gaus Width: 4.5126**

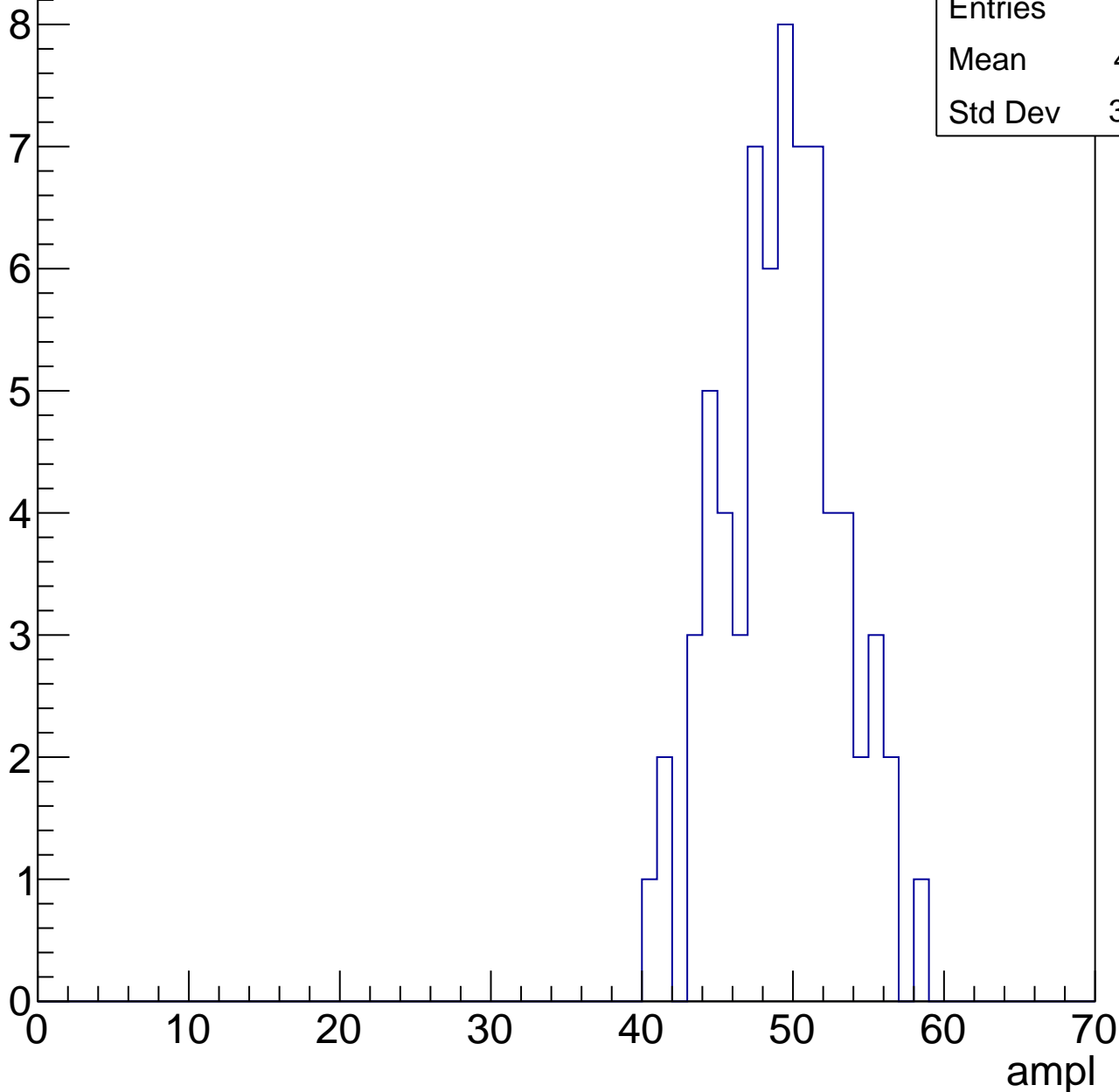


# B1L102S, U3-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	48.81
Std Dev	3.876

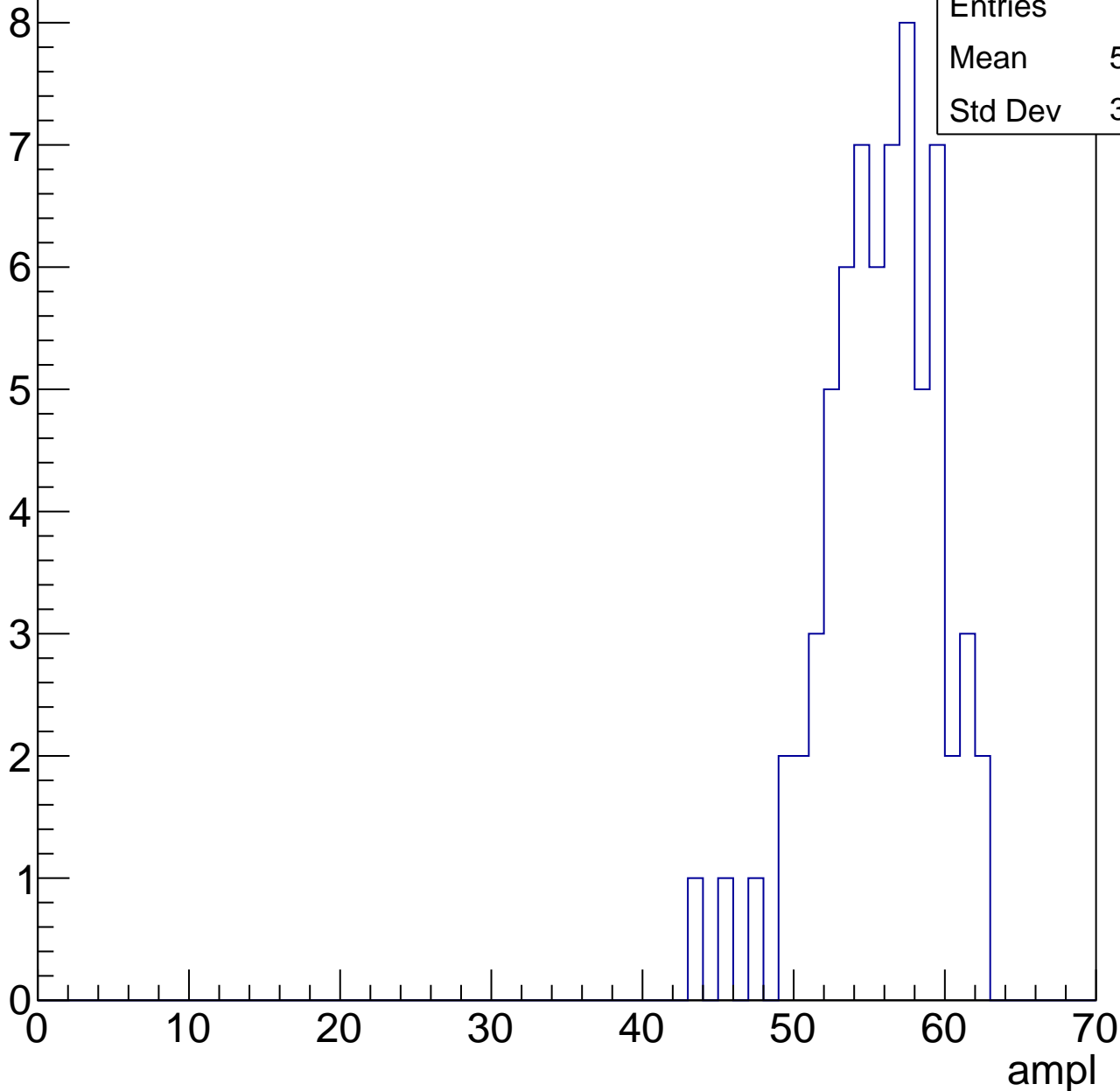


# B1L102S, U3-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	55.15
Std Dev	3.843

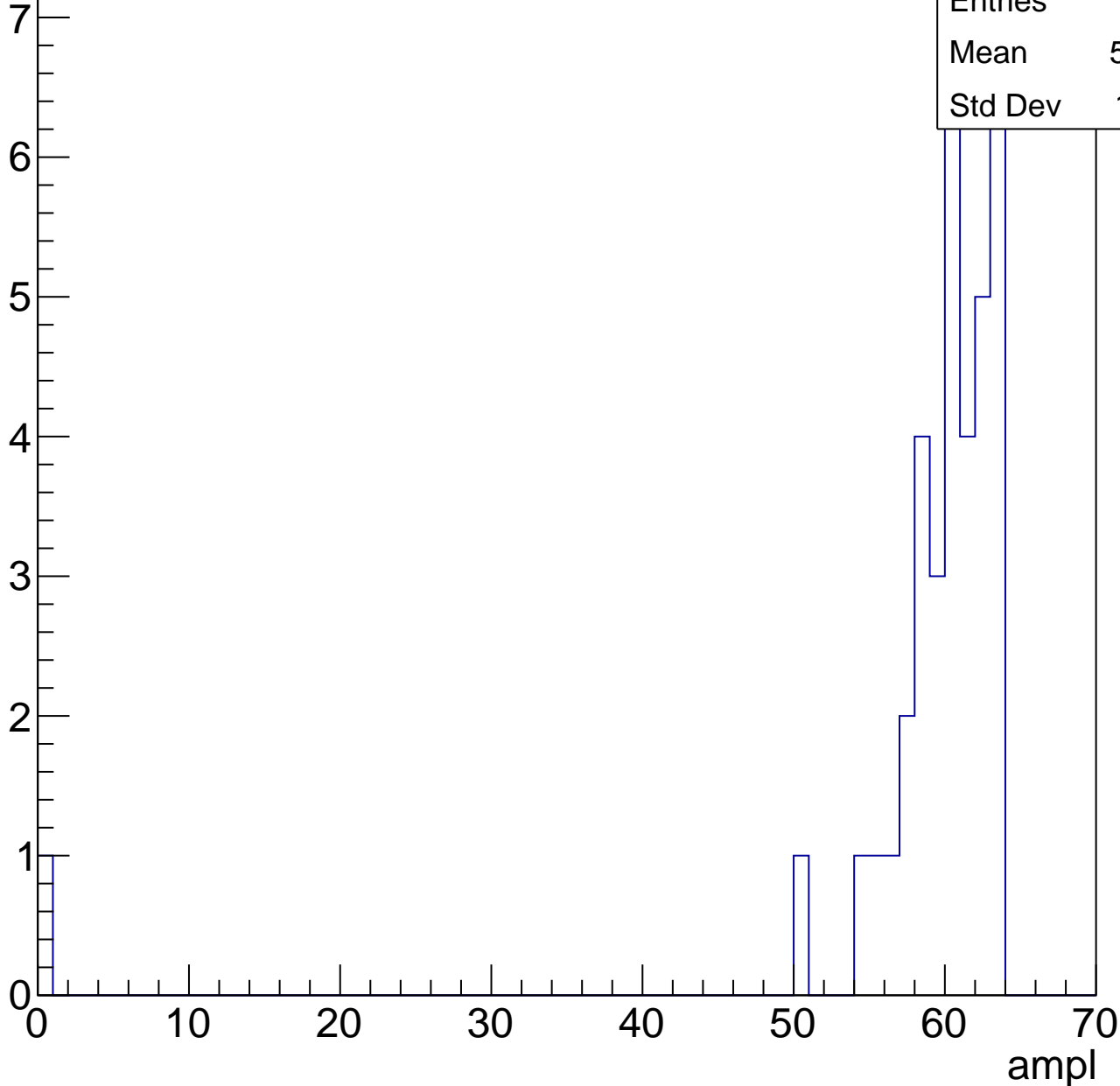


# B1L102S, U3-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	37
Mean	58.19
Std Dev	10.11



# B1L102S, U3-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

10

Mean

61.8

Std Dev

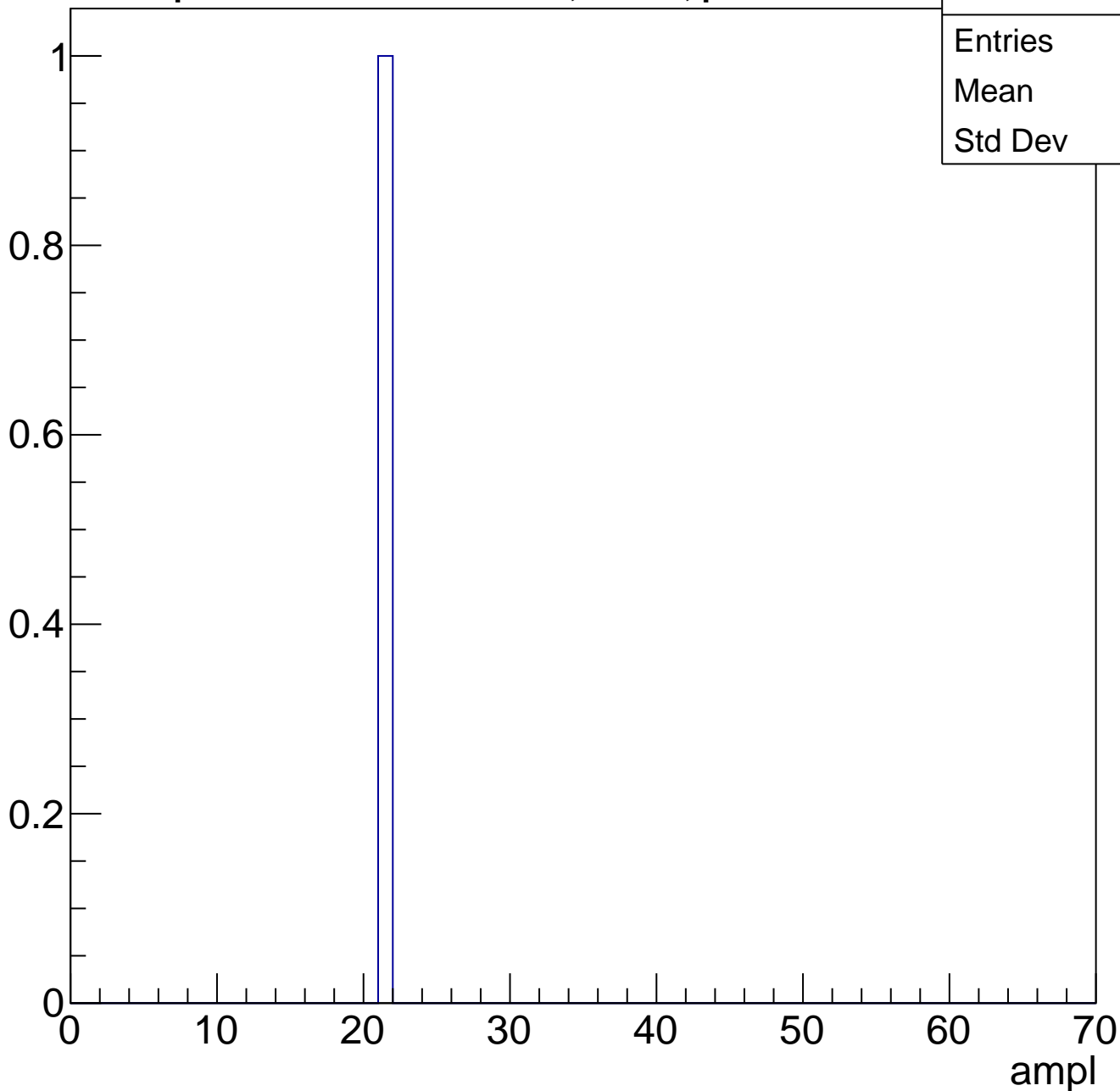
0.9798



# B1L102S, U3-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch89, adc0

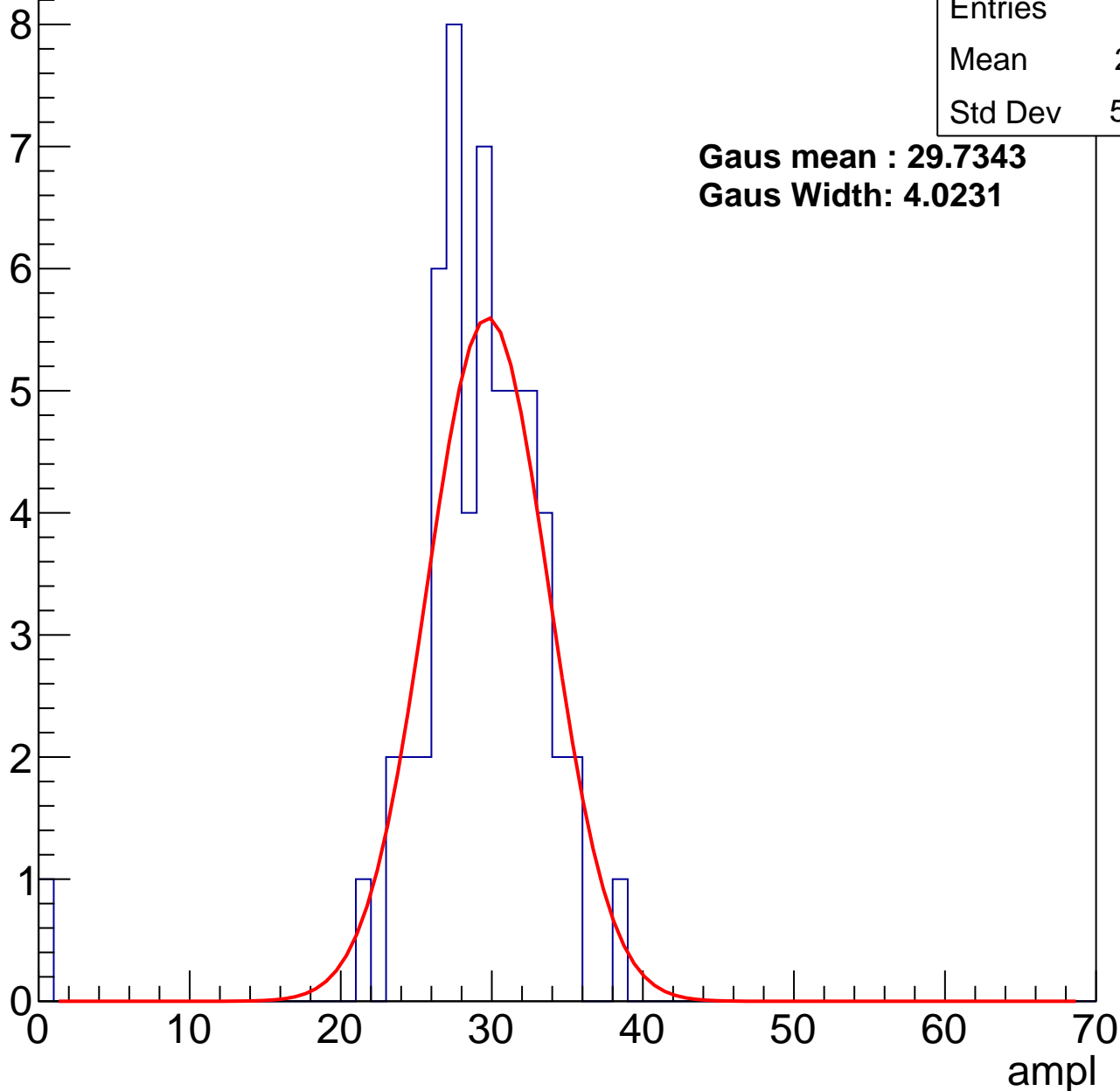
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	28.51
Std Dev	5.082

**Gaus mean : 29.7343**

**Gaus Width: 4.0231**



# B1L102S, U3-ch89, adc1

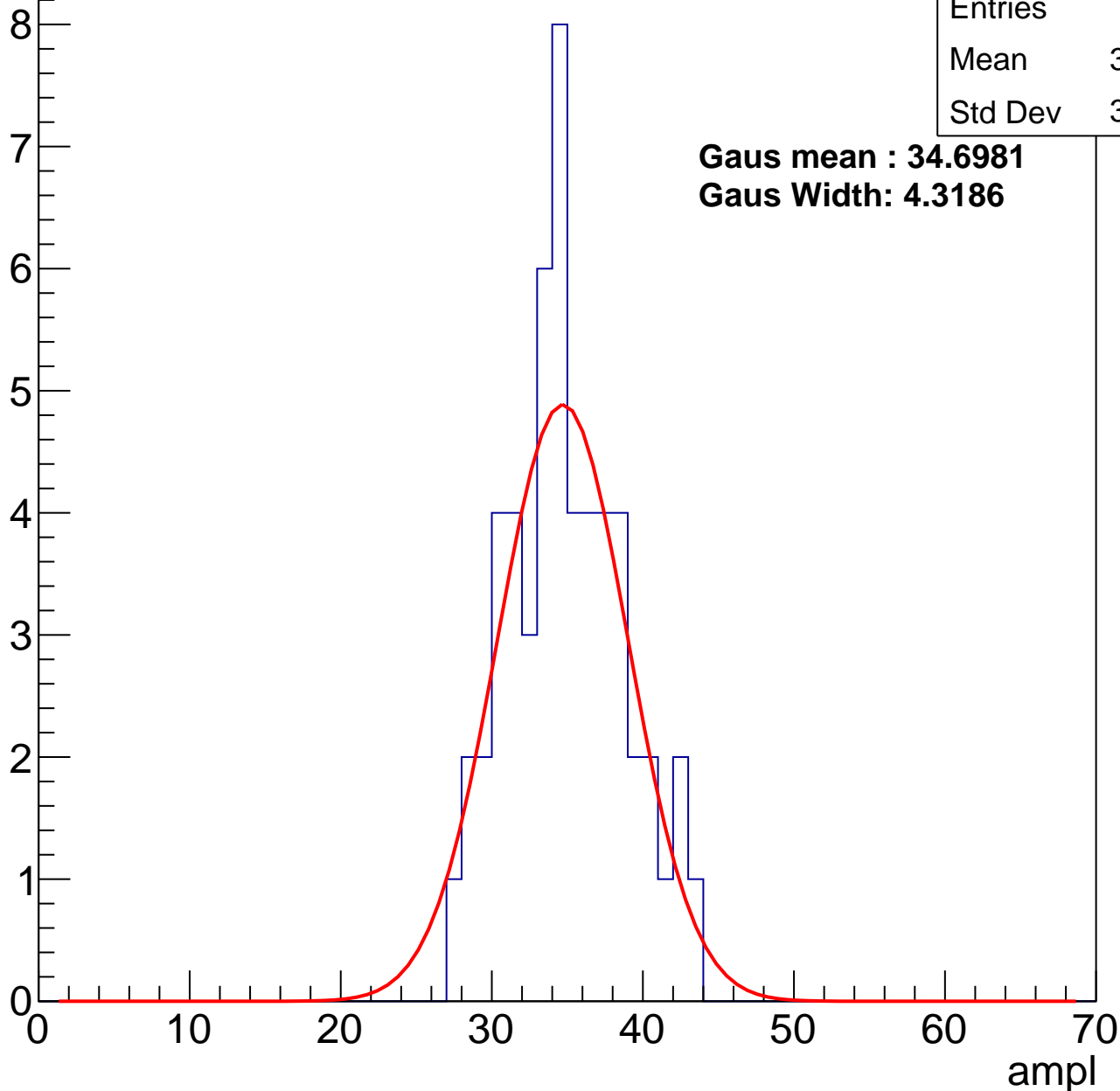
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	34.46
Std Dev	3.794

**Gaus mean : 34.6981**

**Gaus Width: 4.3186**



# B1L102S, U3-ch89, adc2

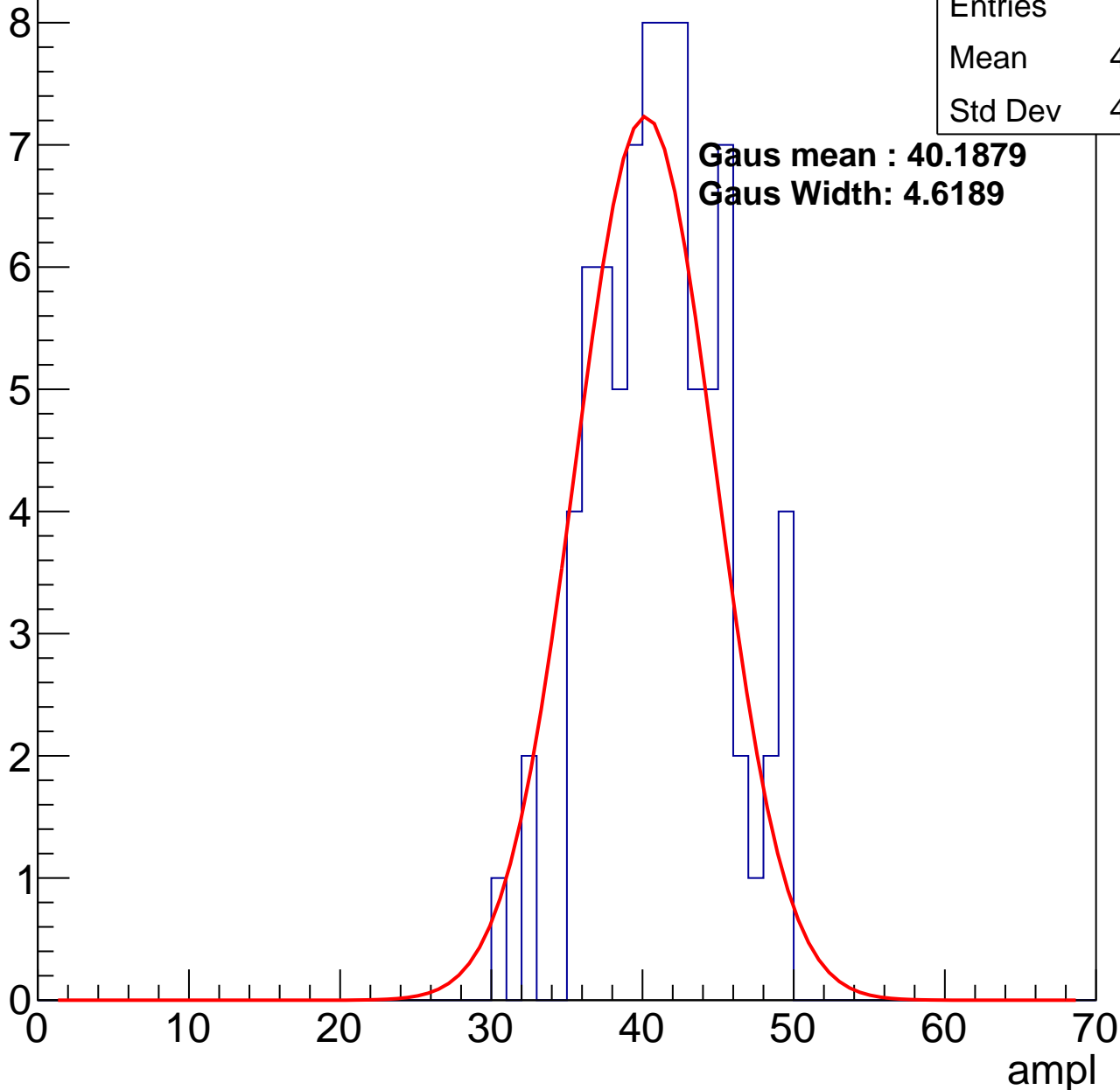
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	81
Mean	40.74
Std Dev	4.118

**Gaus mean : 40.1879**

**Gaus Width: 4.6189**

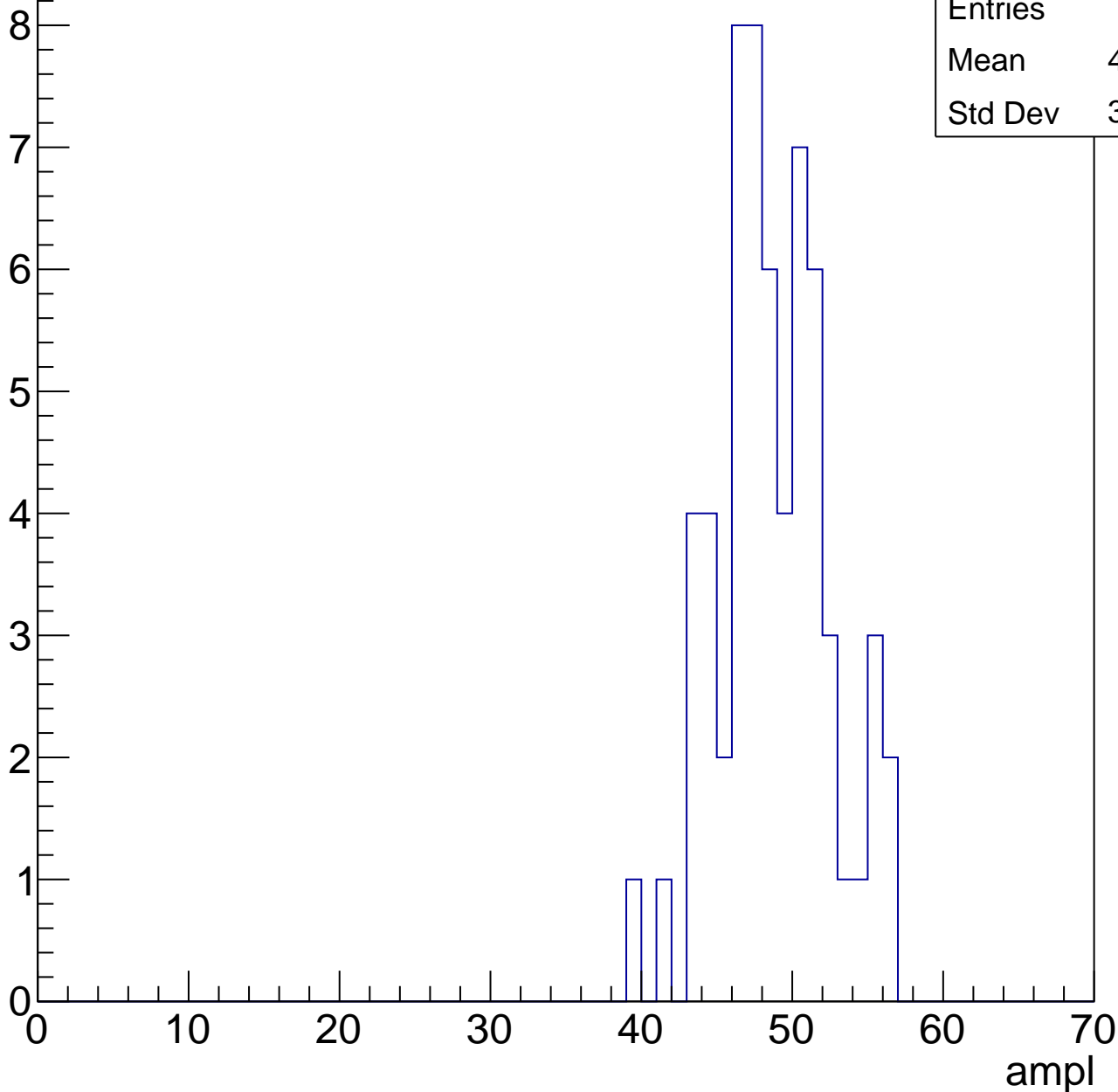


# B1L102S, U3-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	48.23
Std Dev	3.664

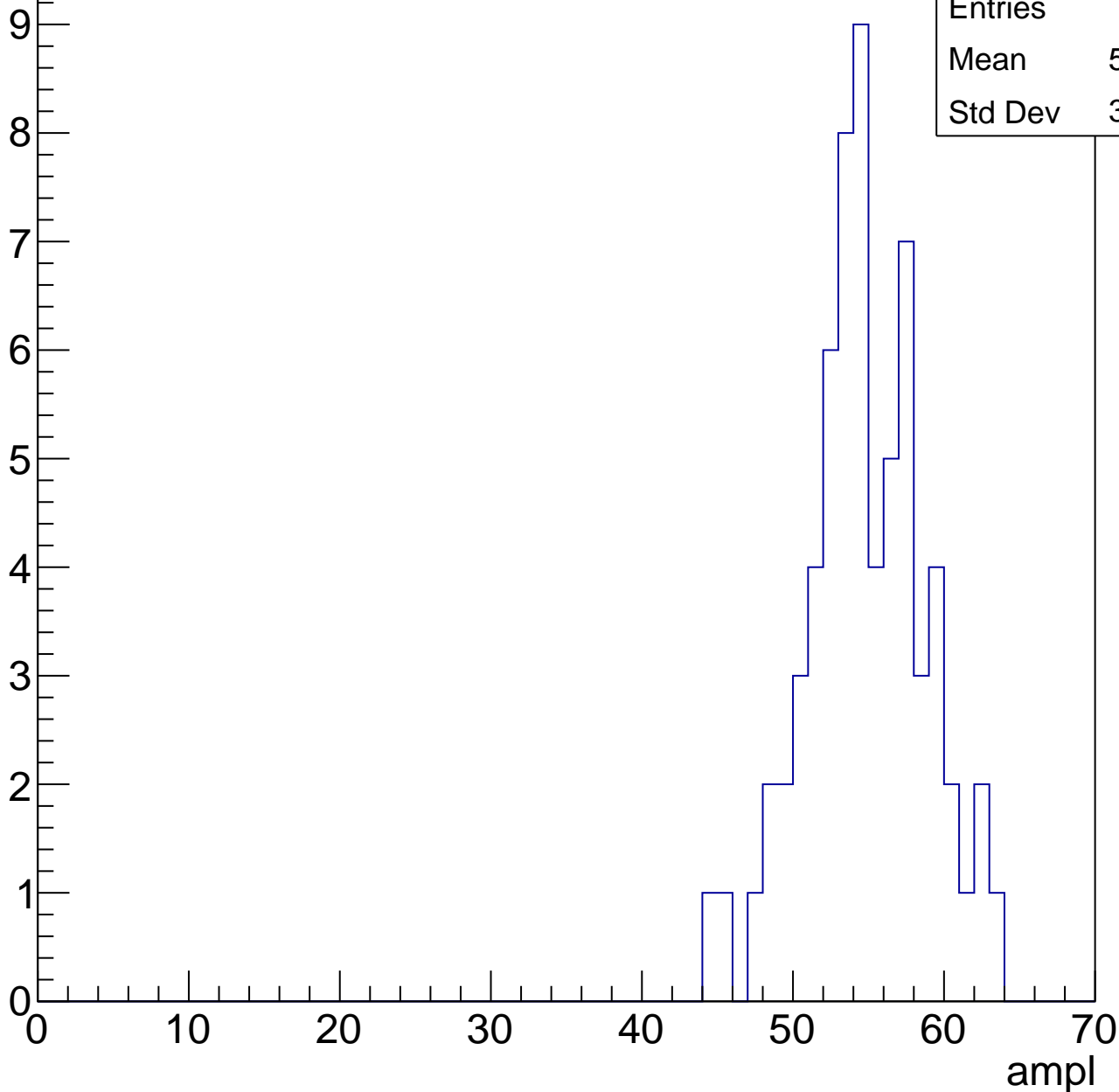


# B1L102S, U3-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	54.29
Std Dev	3.946

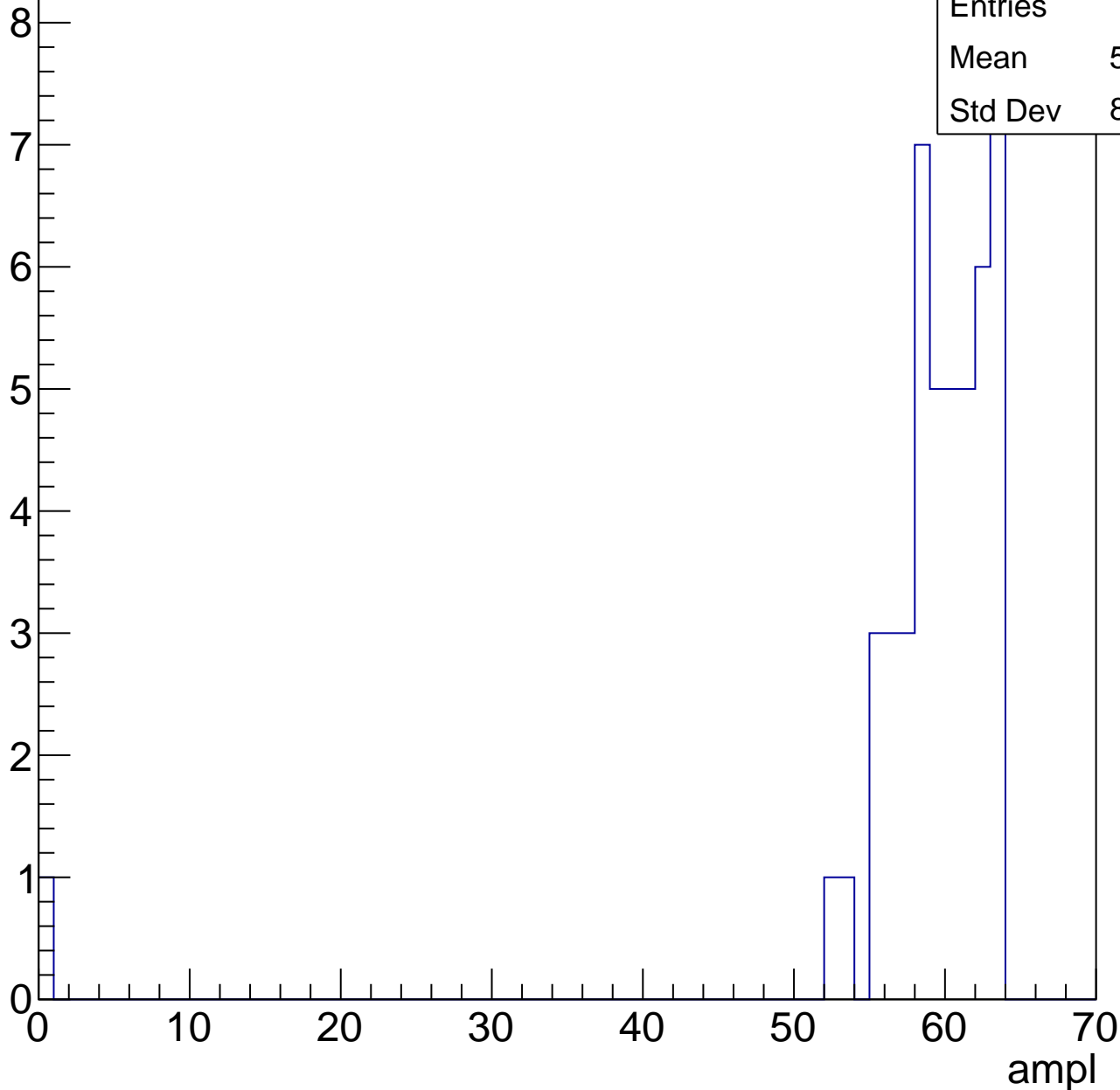


# B1L102S, U3-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

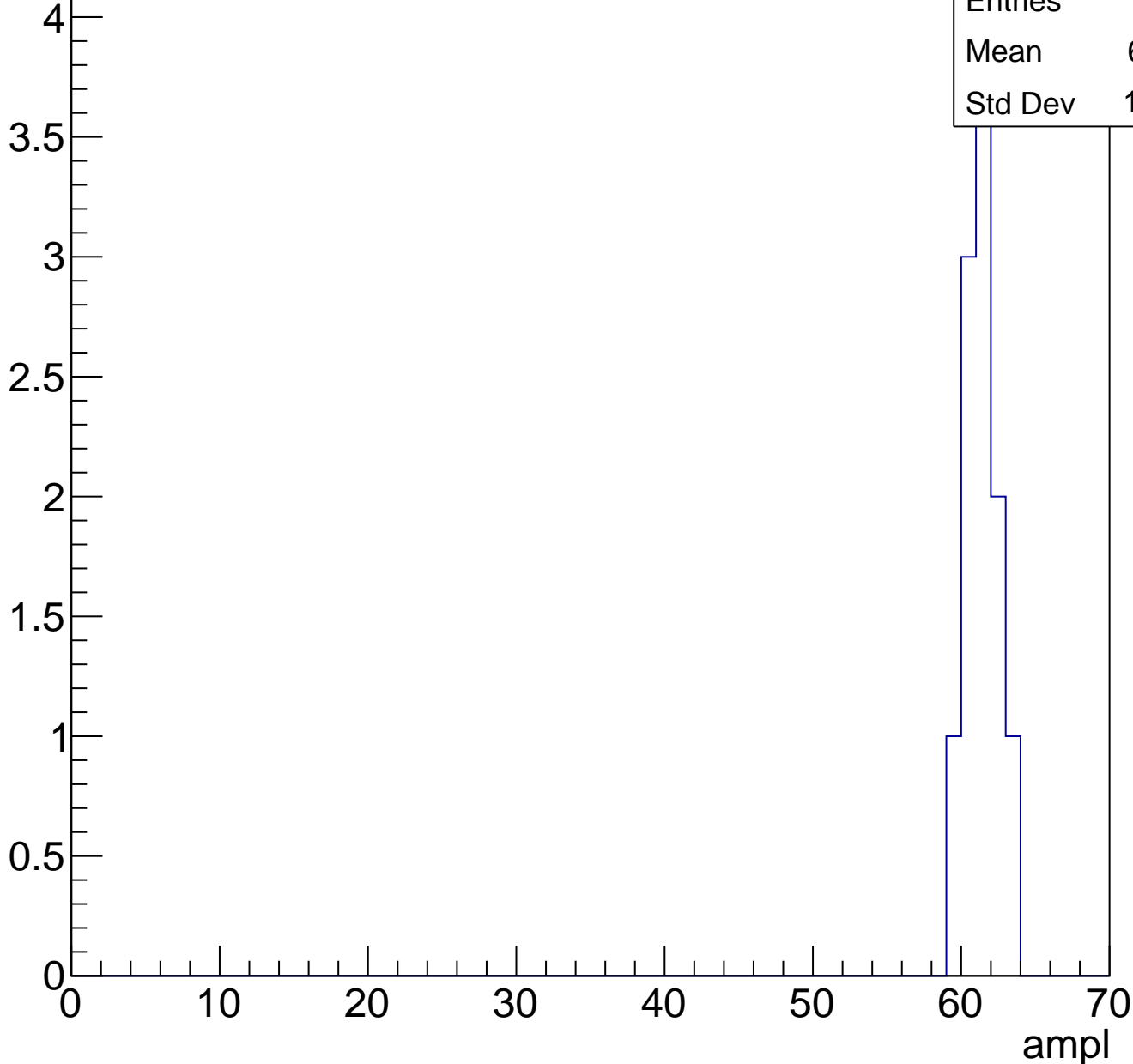
Entries	48
Mean	58.15
Std Dev	8.935



# B1L102S, U3-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch90, adc0

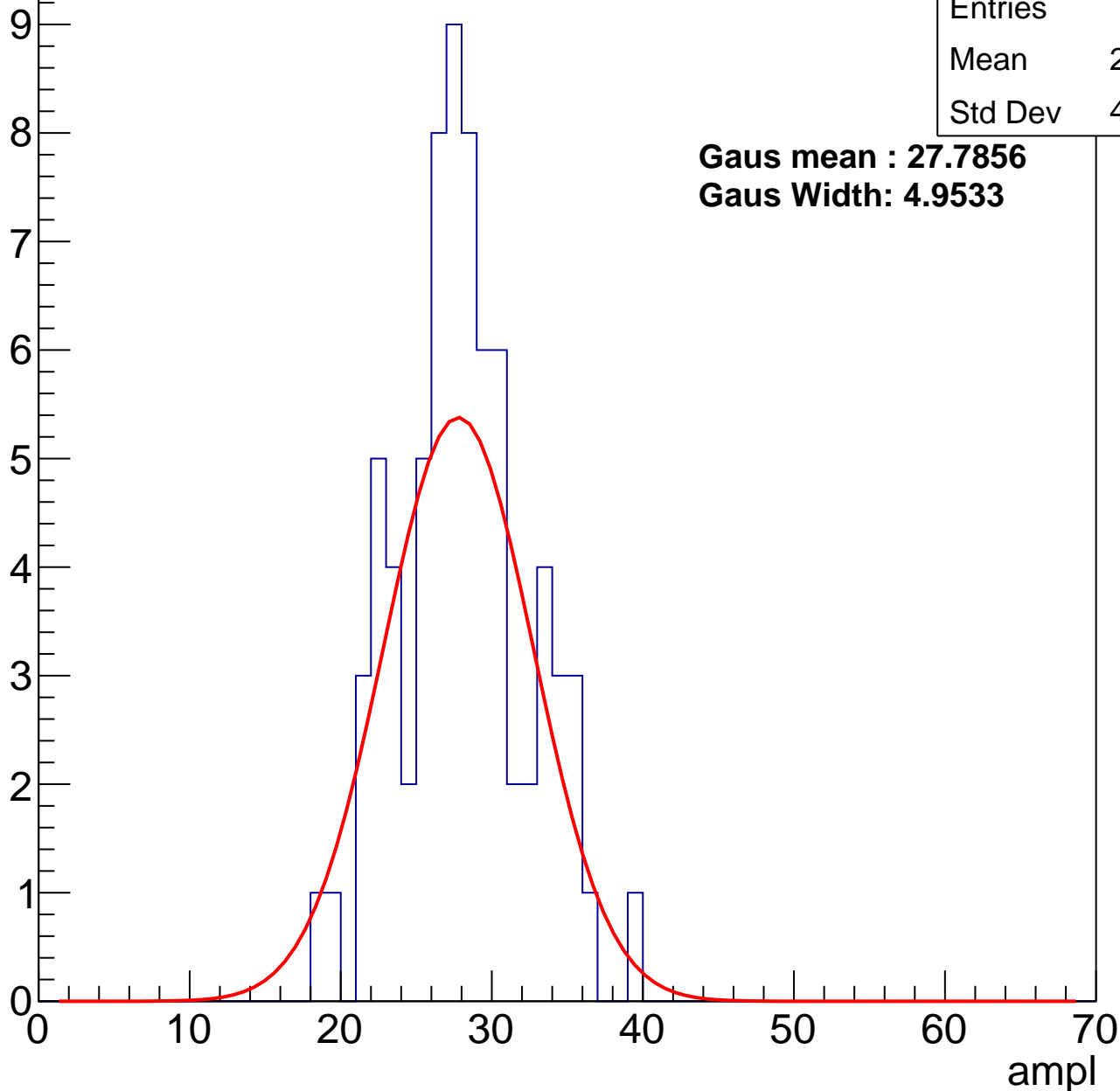
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	27.62
Std Dev	4.248

**Gaus mean : 27.7856**

**Gaus Width: 4.9533**



# B1L102S, U3-ch90, adc1

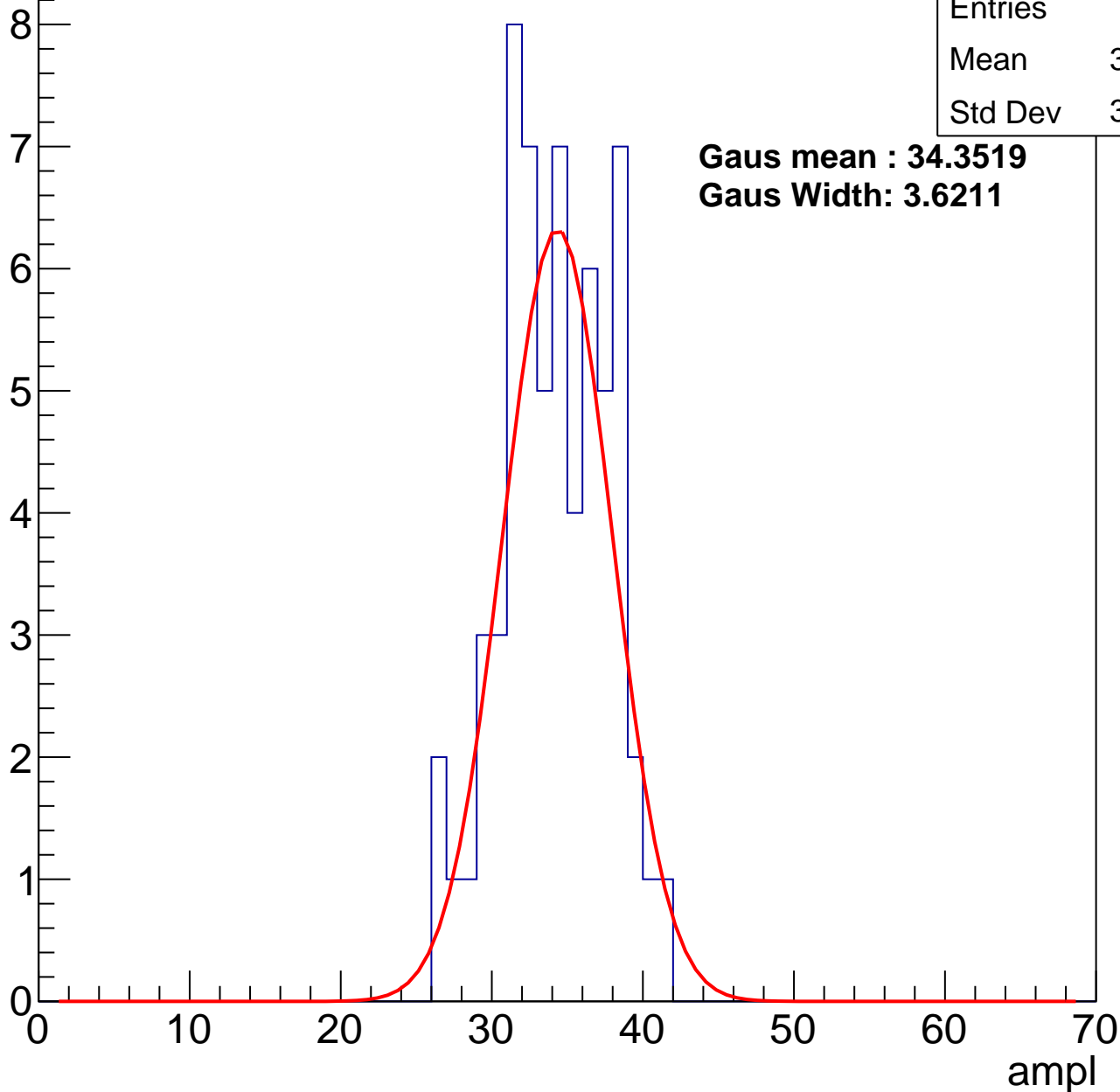
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	33.73
Std Dev	3.465

**Gaus mean : 34.3519**

**Gaus Width: 3.6211**



# B1L102S, U3-ch90, adc2

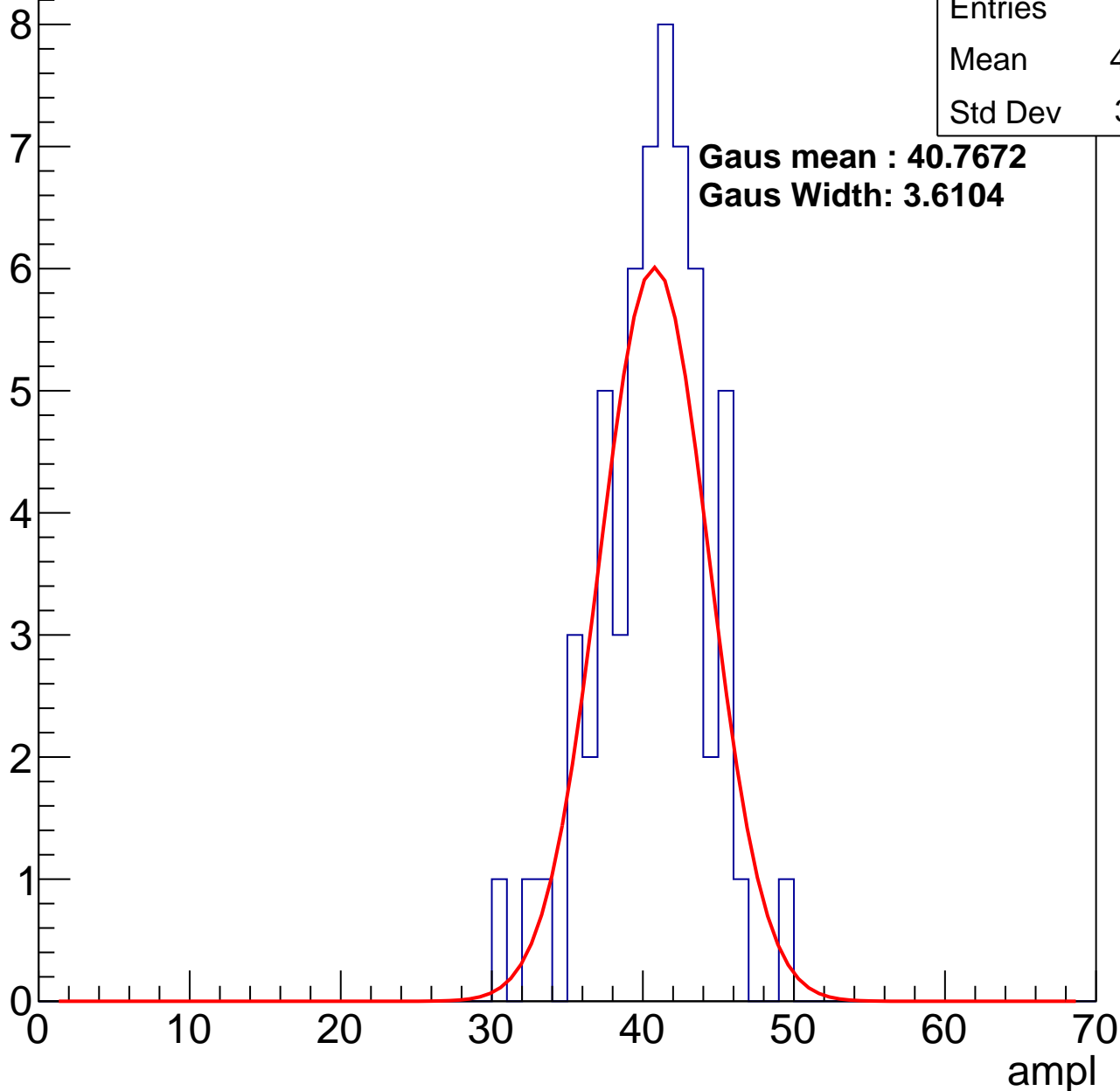
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	40.22
Std Dev	3.551

**Gaus mean : 40.7672**

**Gaus Width: 3.6104**

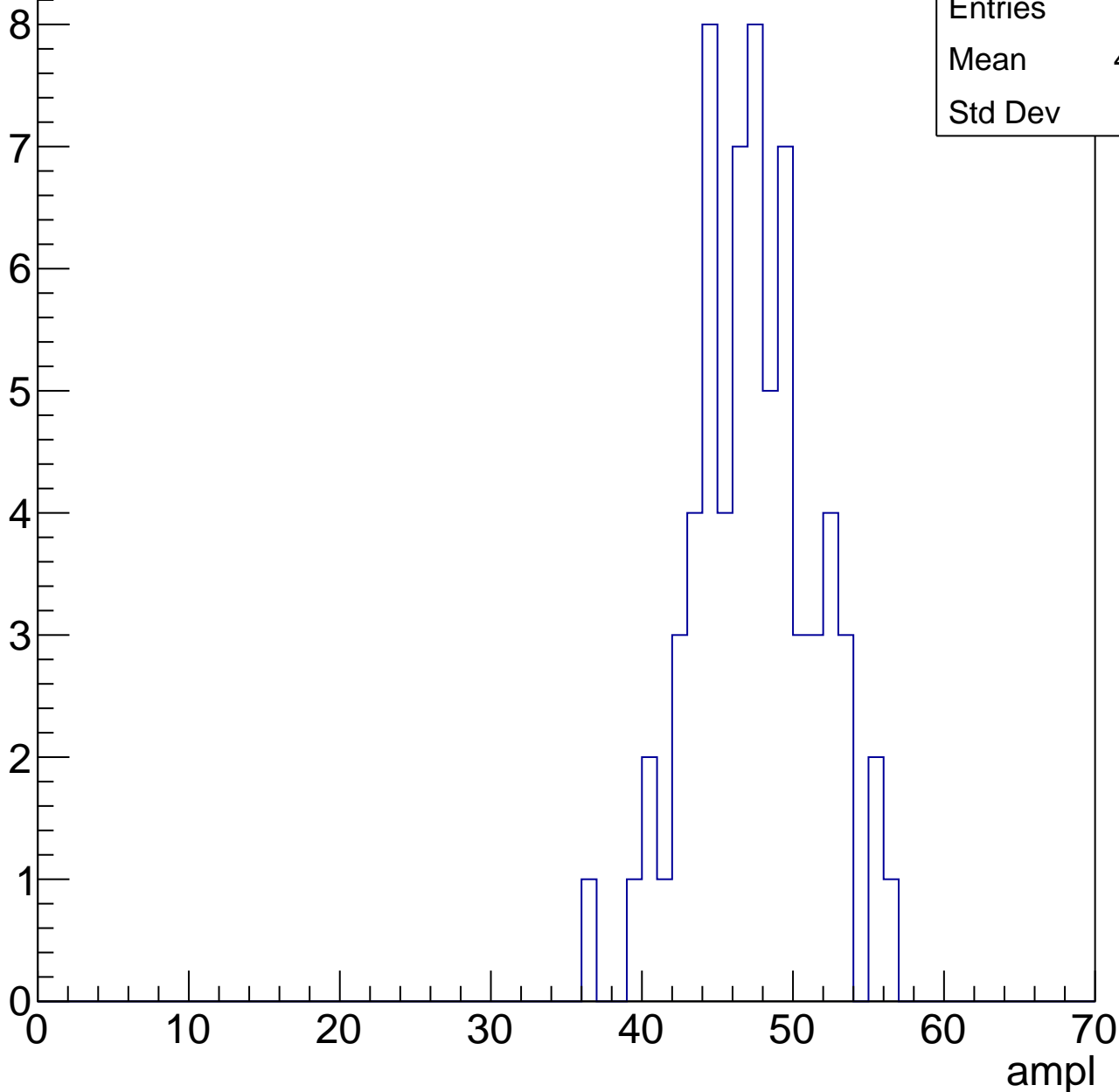


# B1L102S, U3-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	46.91
Std Dev	4.01

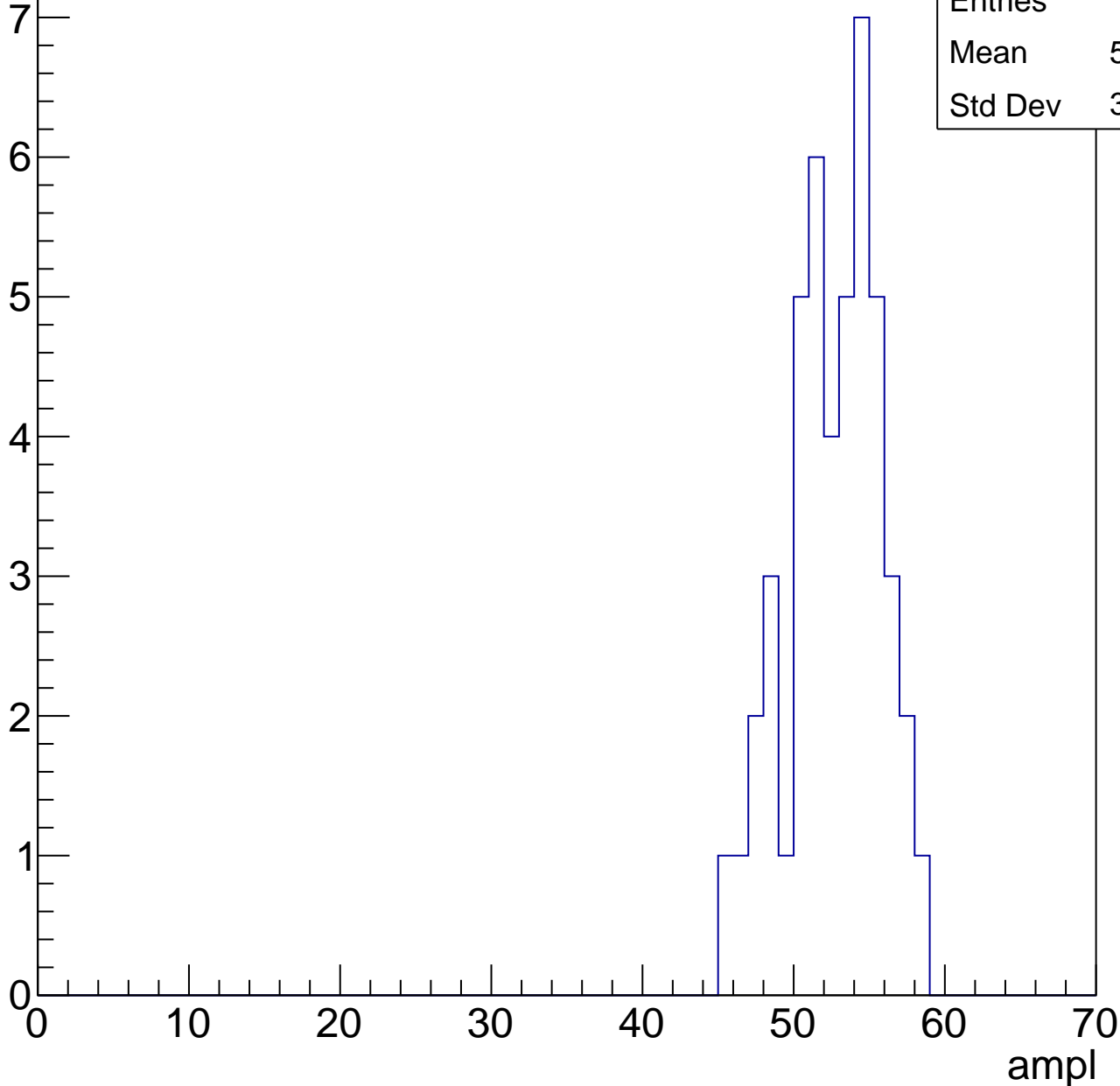


# B1L102S, U3-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	52.17
Std Dev	3.052

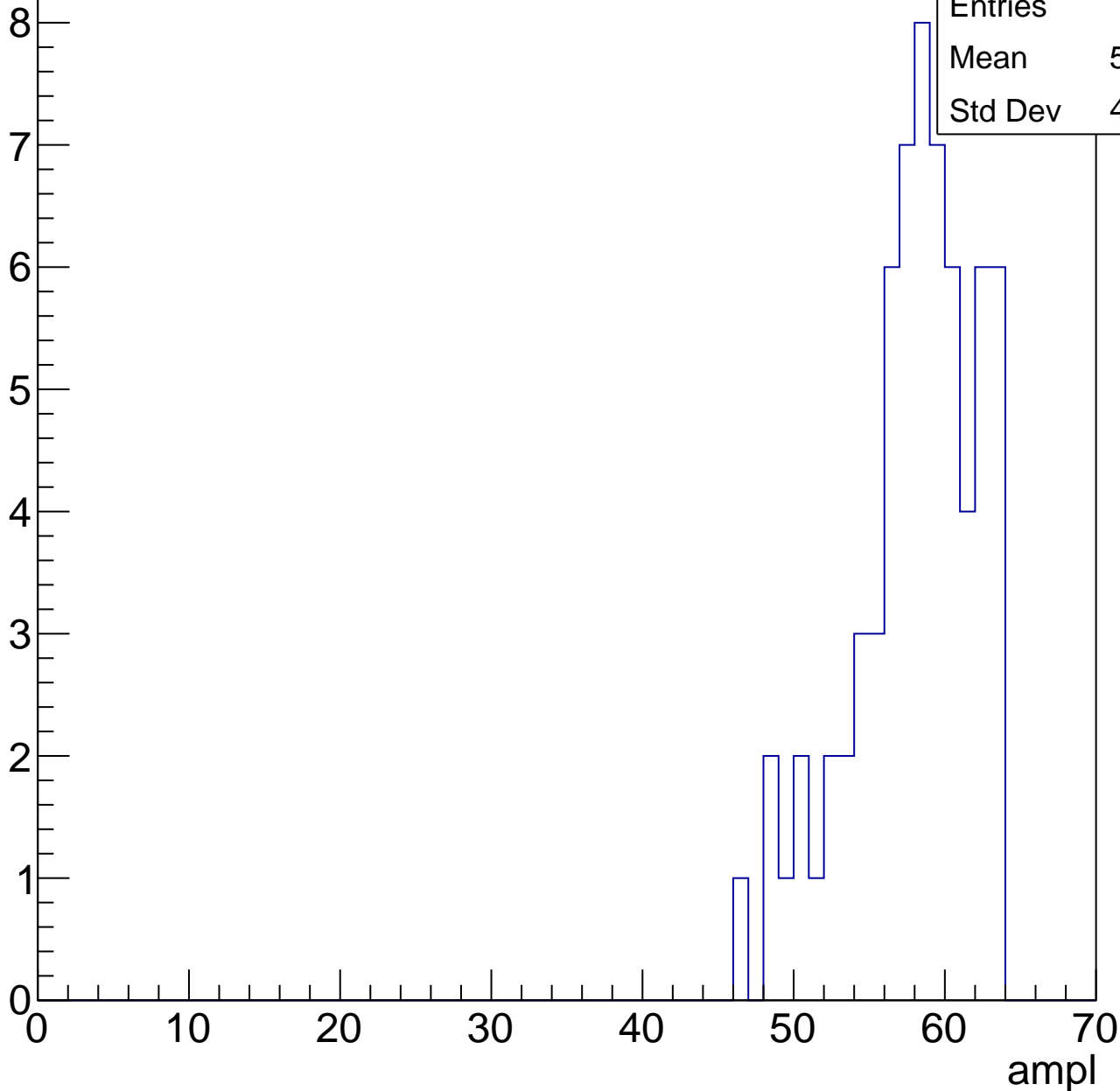


# B1L102S, U3-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	57.39
Std Dev	4.085

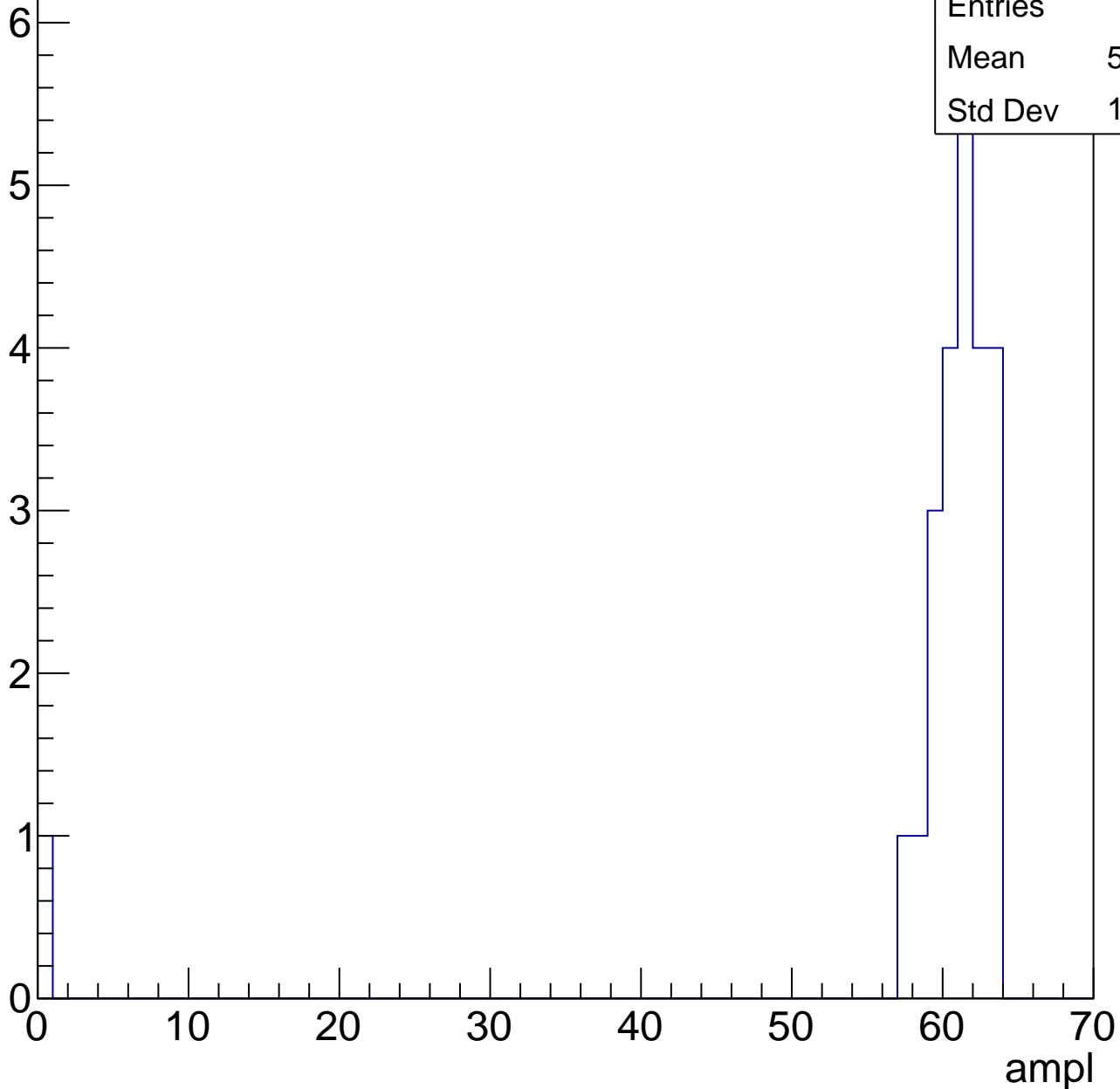


# B1L102S, U3-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	24
Mean	58.25
Std Dev	12.25





# B1L102S, U3-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch91, adc0

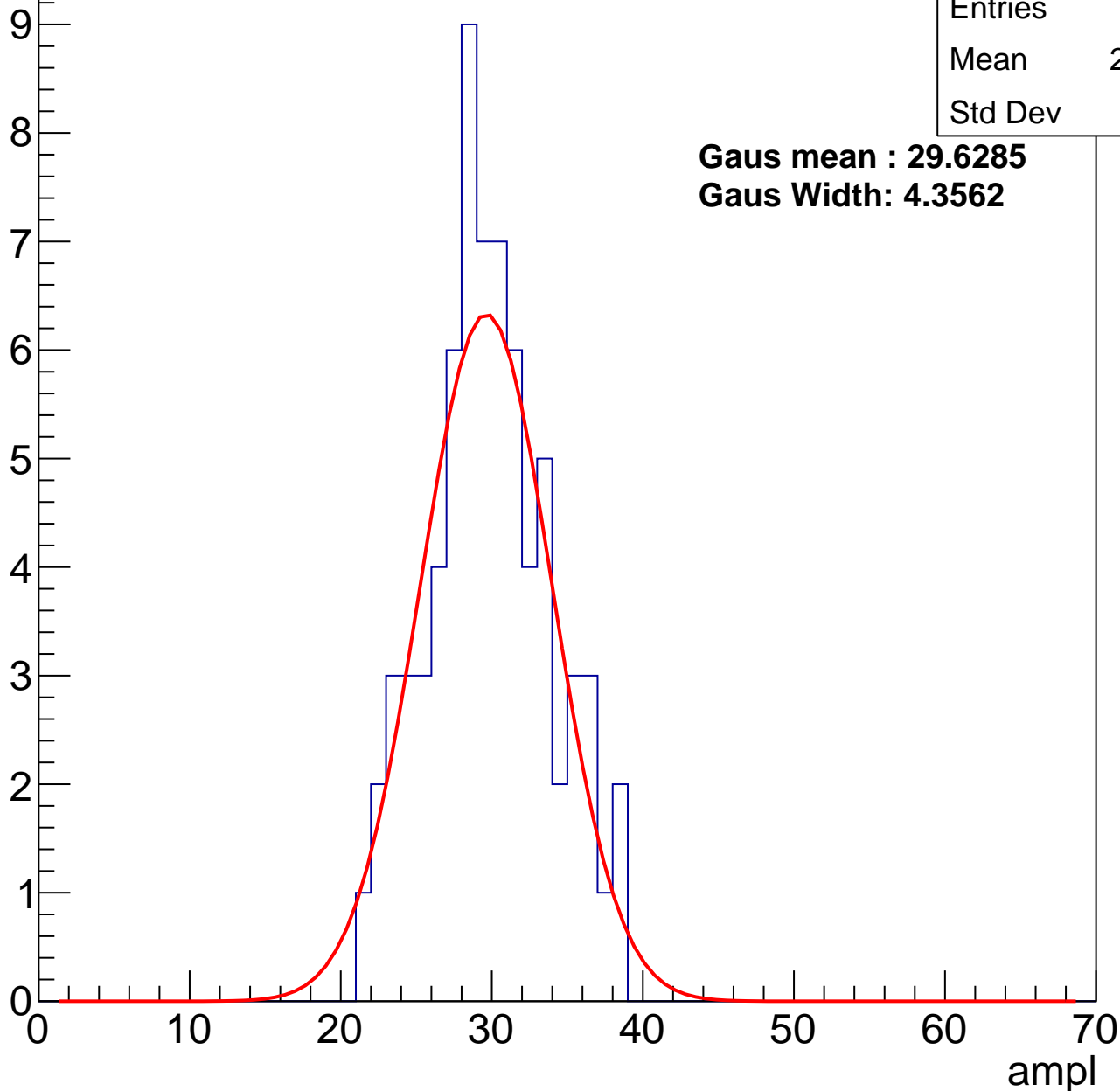
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	29.37
Std Dev	3.99

**Gaus mean : 29.6285**

**Gaus Width: 4.3562**



# B1L102S, U3-ch91, adc1

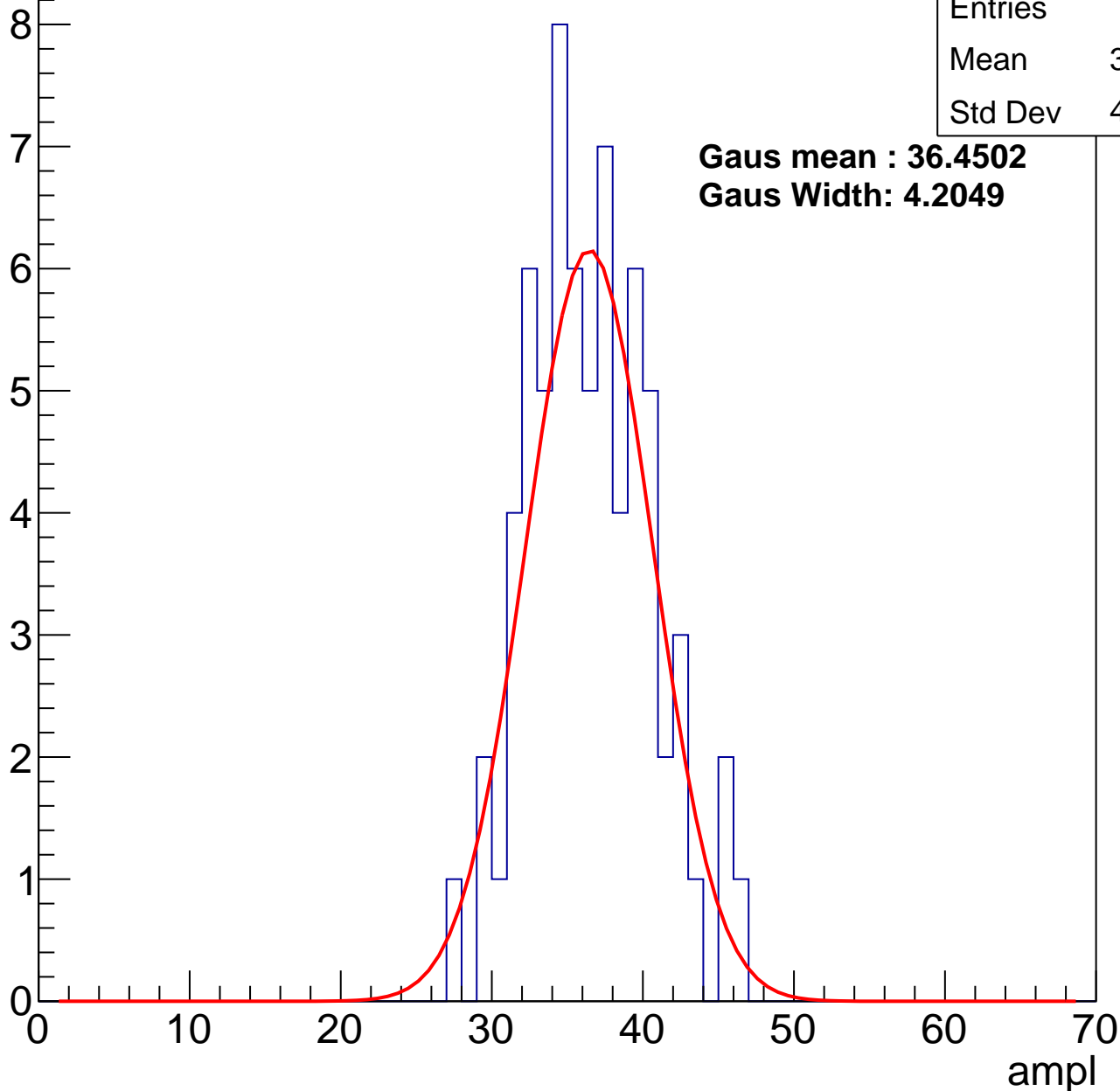
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	36.09
Std Dev	4.028

**Gaus mean : 36.4502**

**Gaus Width: 4.2049**



# B1L102S, U3-ch91, adc2

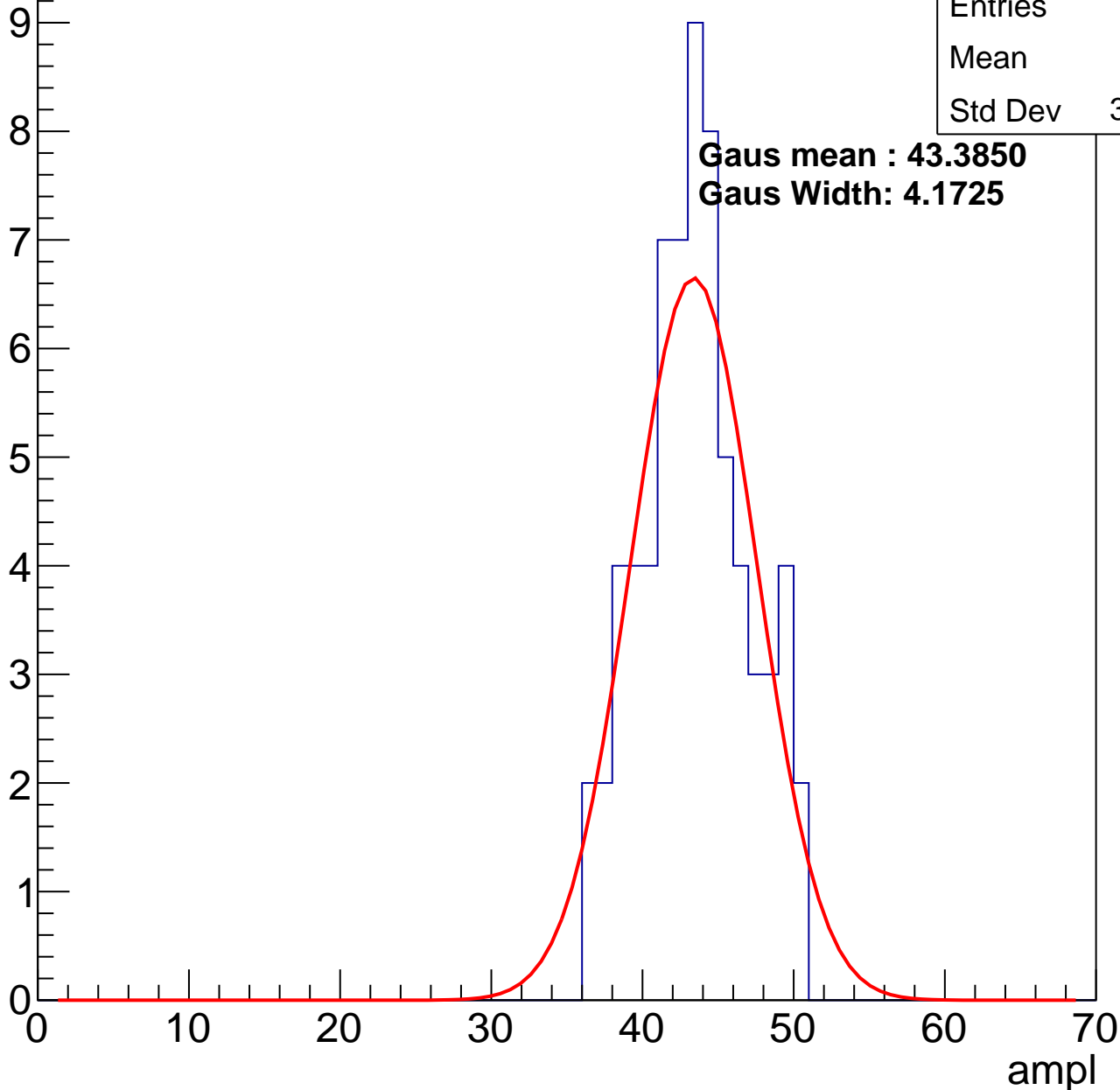
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	43
Std Dev	3.502

**Gaus mean : 43.3850**

**Gaus Width: 4.1725**

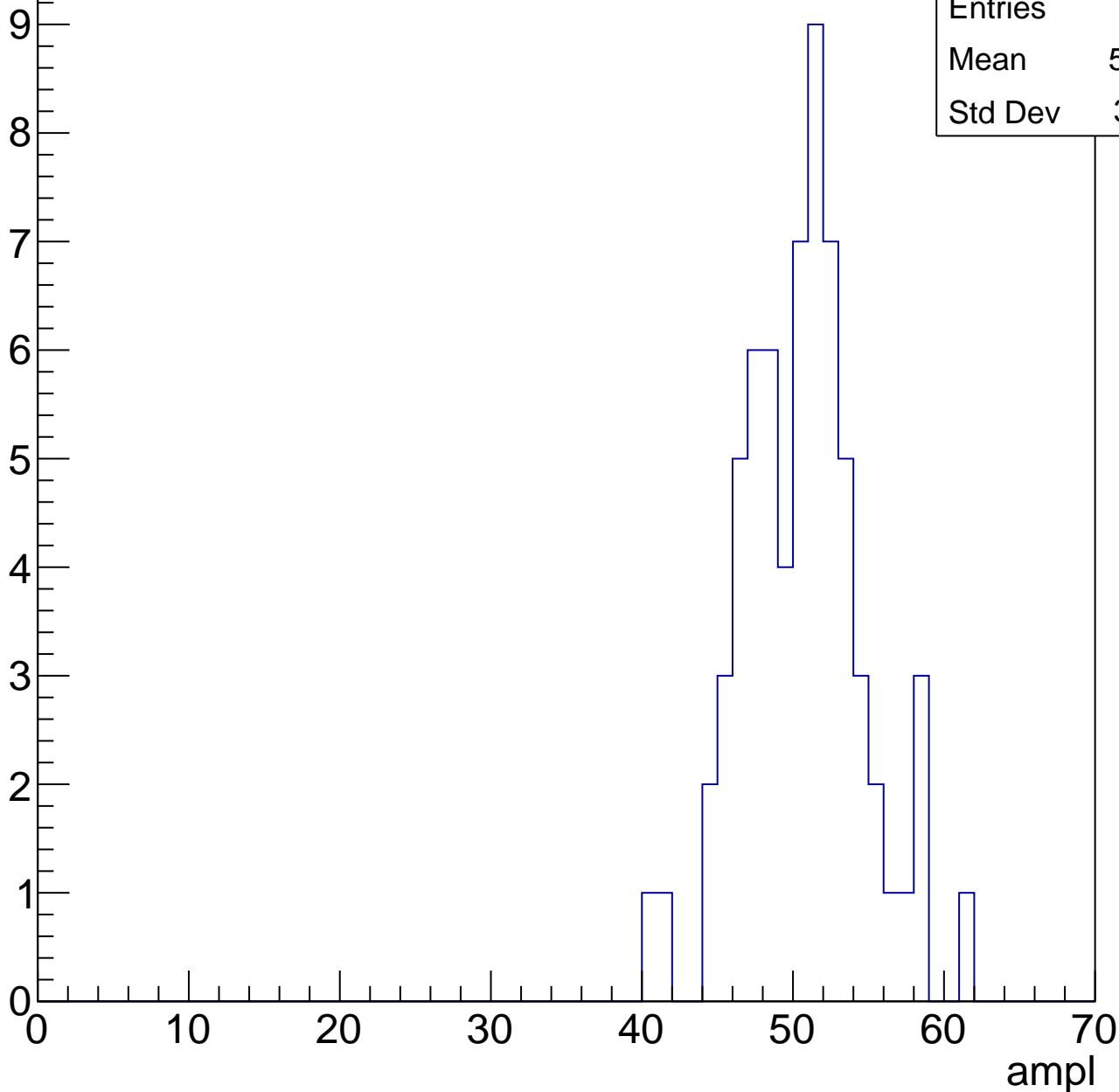


# B1L102S, U3-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

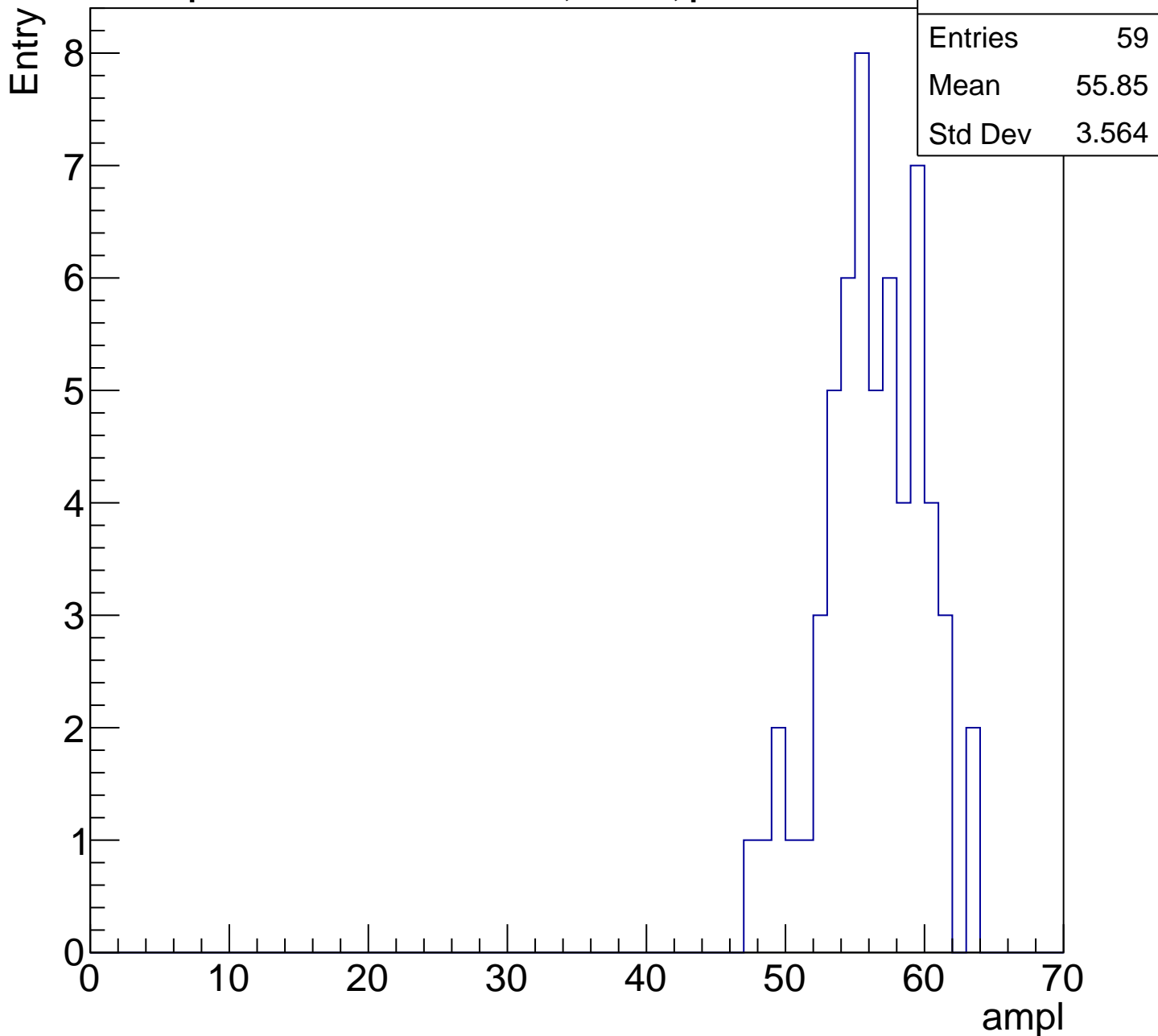
Entry

Entries	67
Mean	50.12
Std Dev	3.991



# B1L102S, U3-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

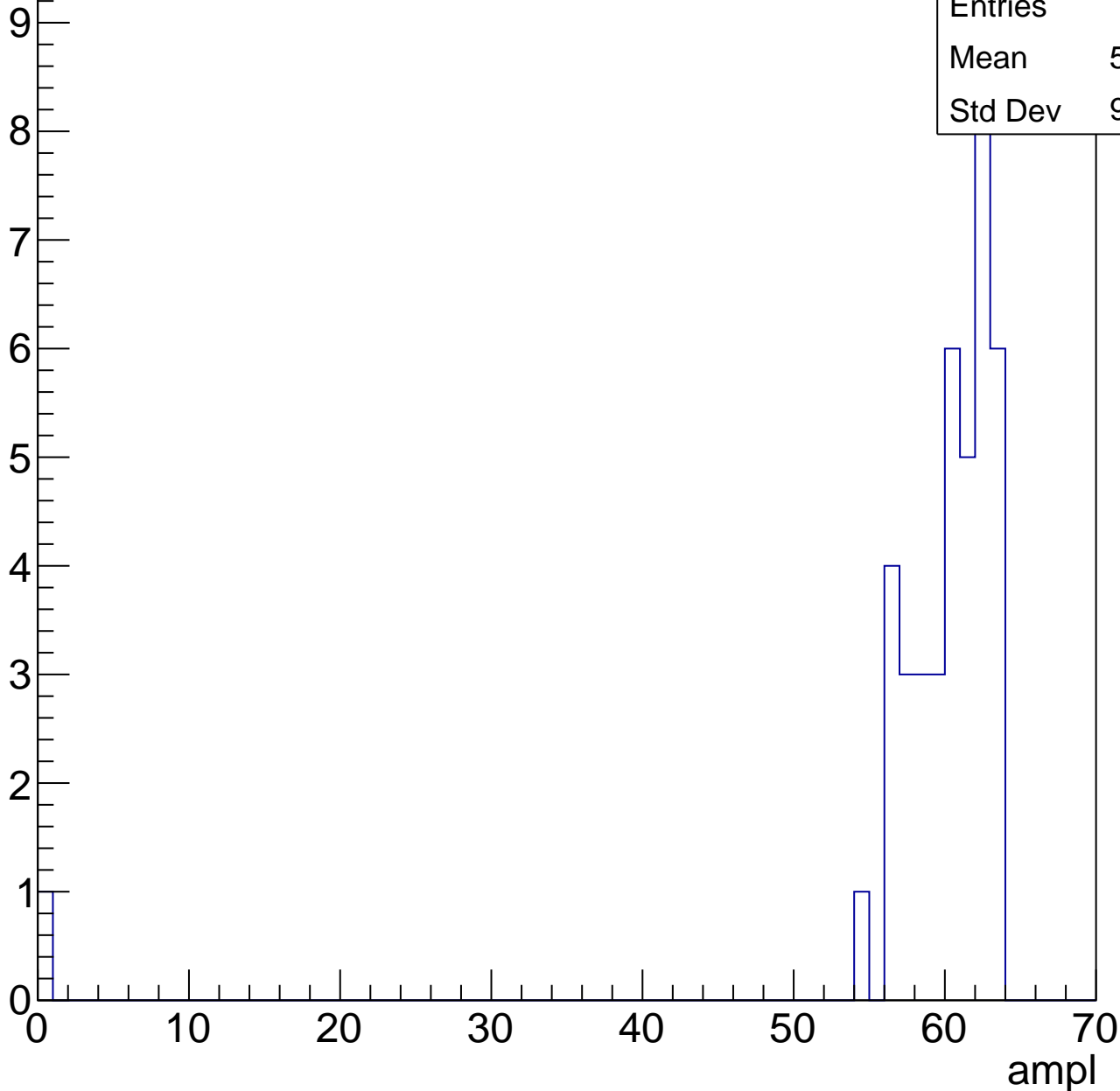


# B1L102S, U3-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	41
Mean	58.56
Std Dev	9.566



# B1L102S, U3-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U3-ch92, adc0

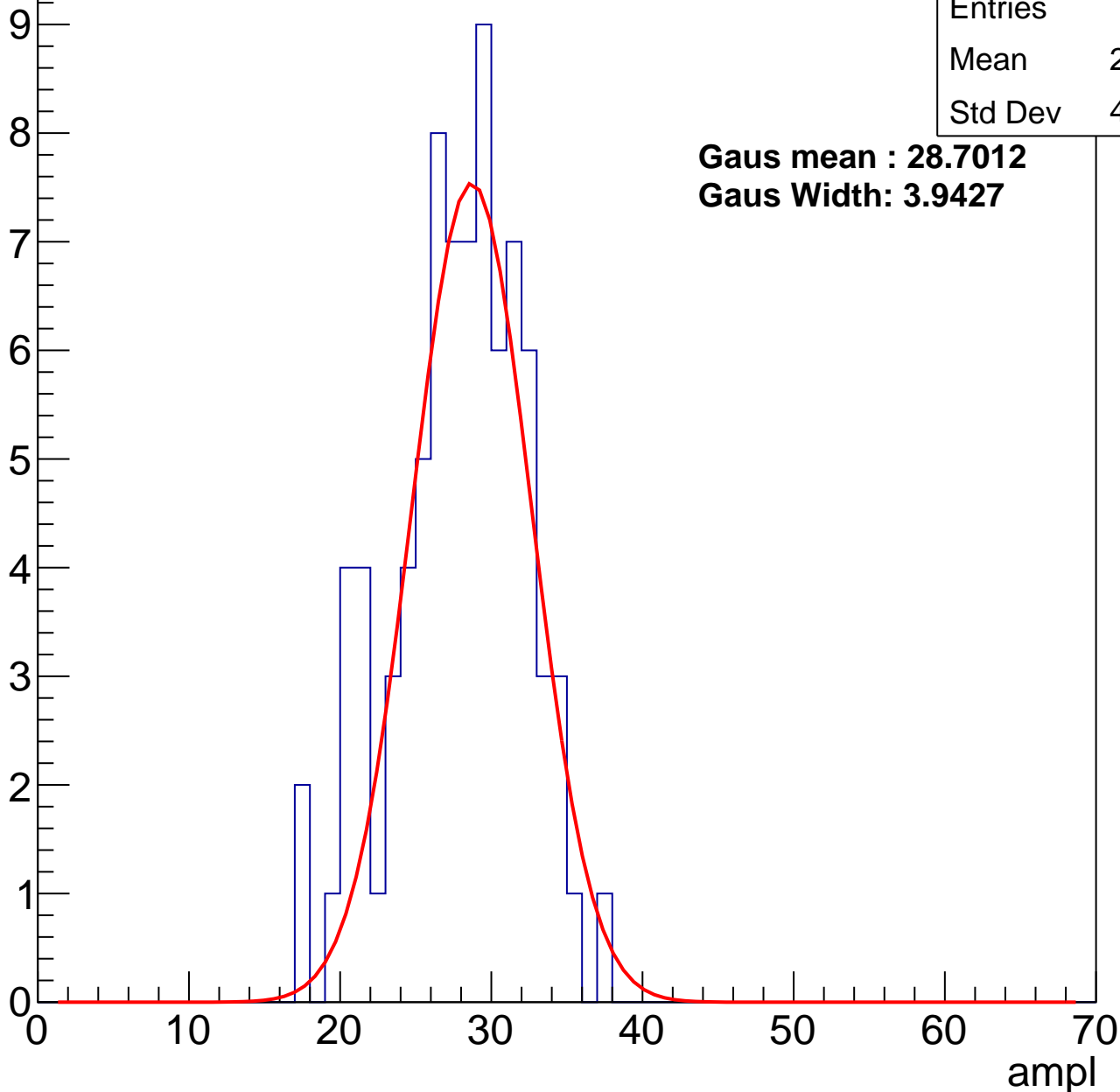
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	27.38
Std Dev	4.287

**Gaus mean : 28.7012**

**Gaus Width: 3.9427**



# B1L102S, U3-ch92, adc1

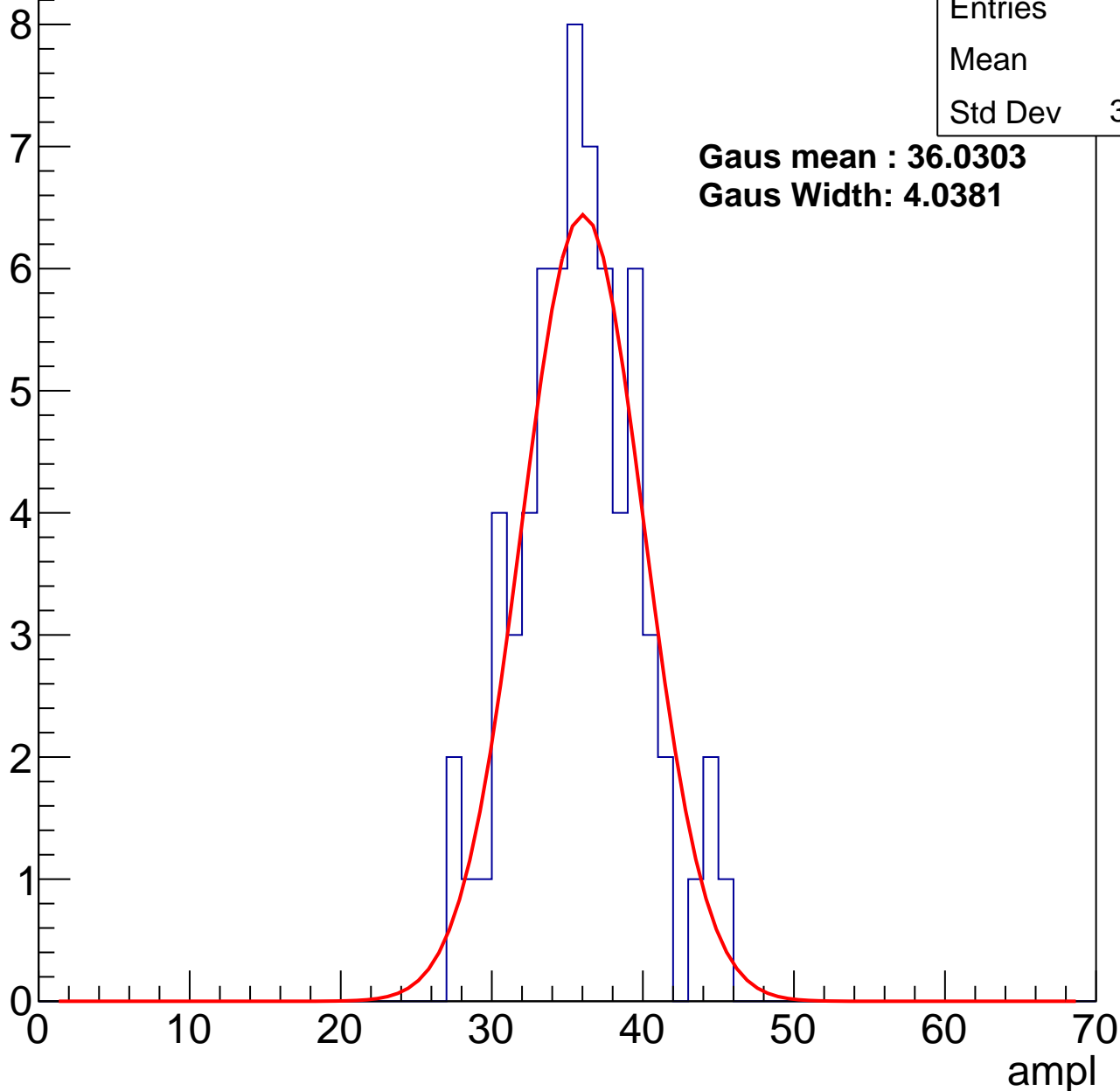
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	35.4
Std Dev	3.963

**Gaus mean : 36.0303**

**Gaus Width: 4.0381**



# B1L102S, U3-ch92, adc2

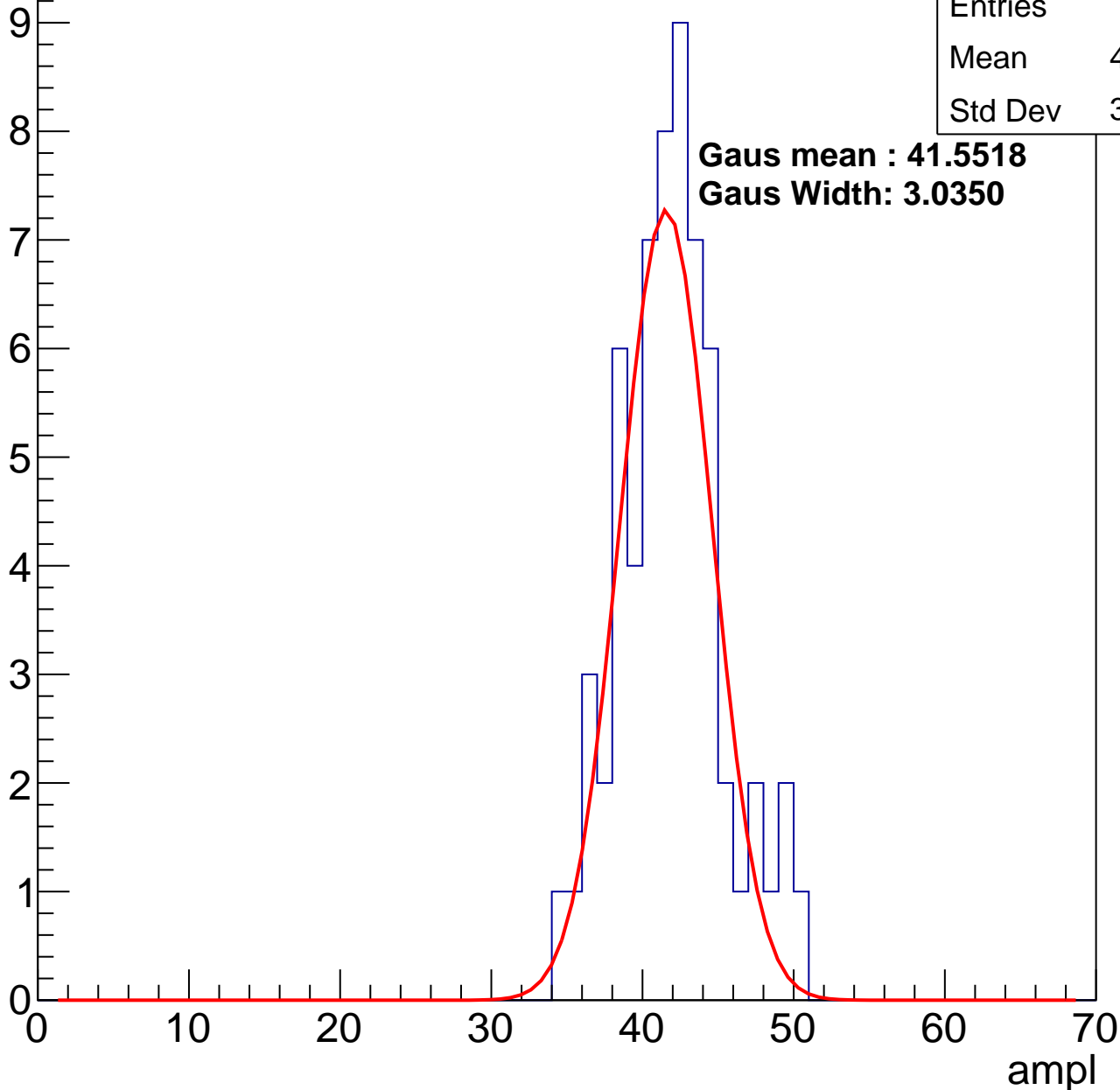
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	41.46
Std Dev	3.413

**Gaus mean : 41.5518**

**Gaus Width: 3.0350**

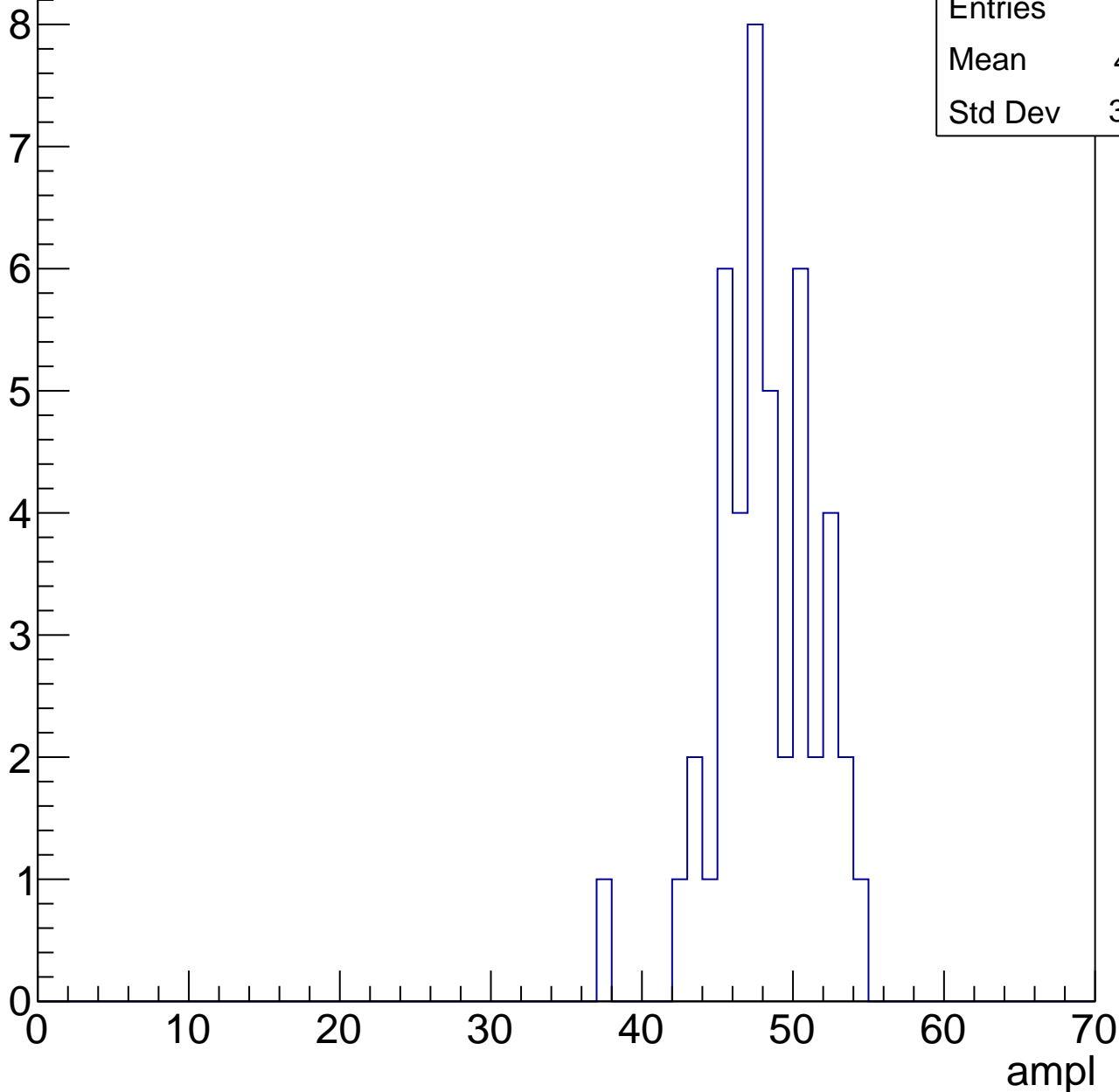


# B1L102S, U3-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	47.71
Std Dev	3.304

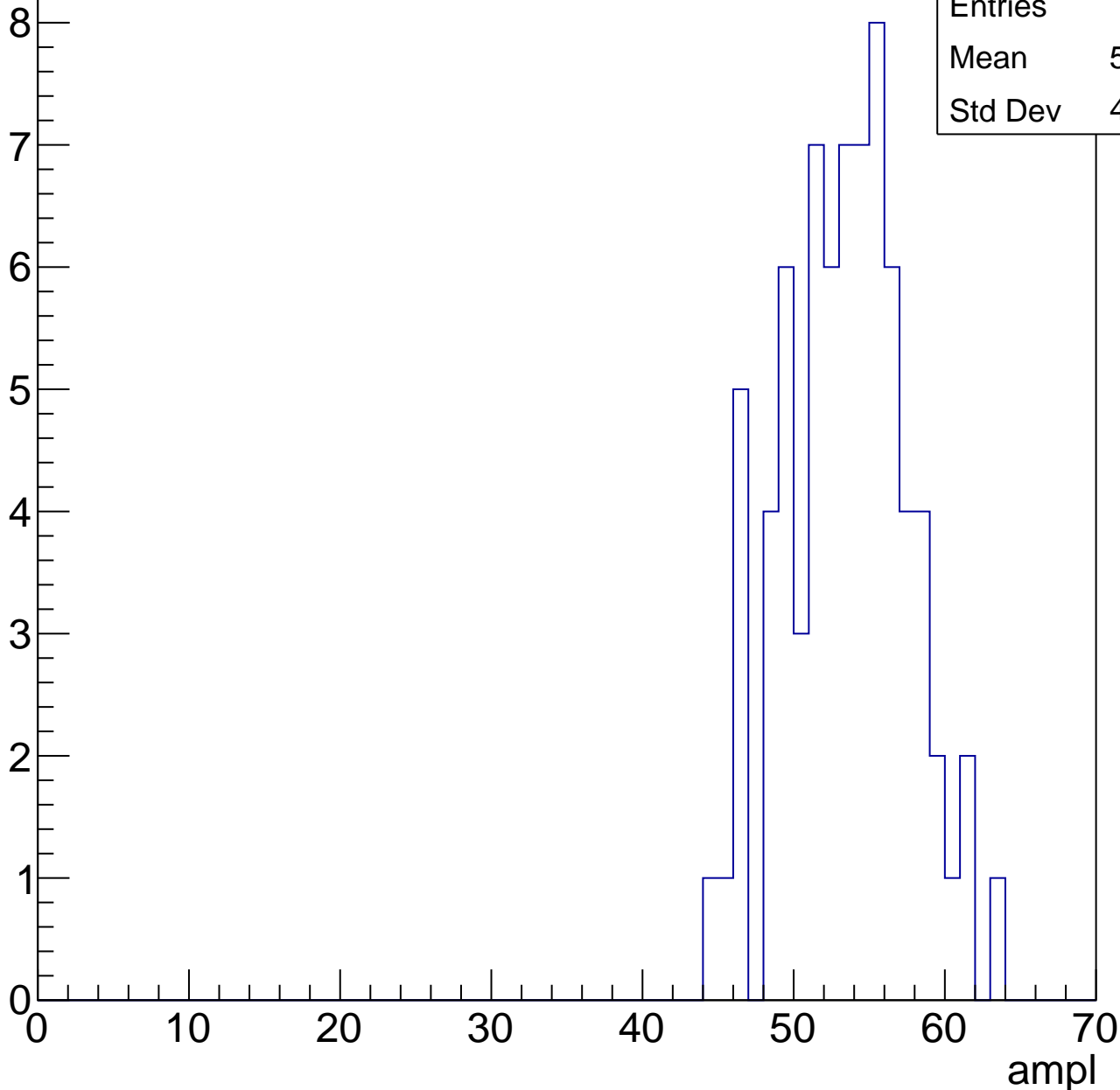


# B1L102S, U3-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	52.96
Std Dev	4.087

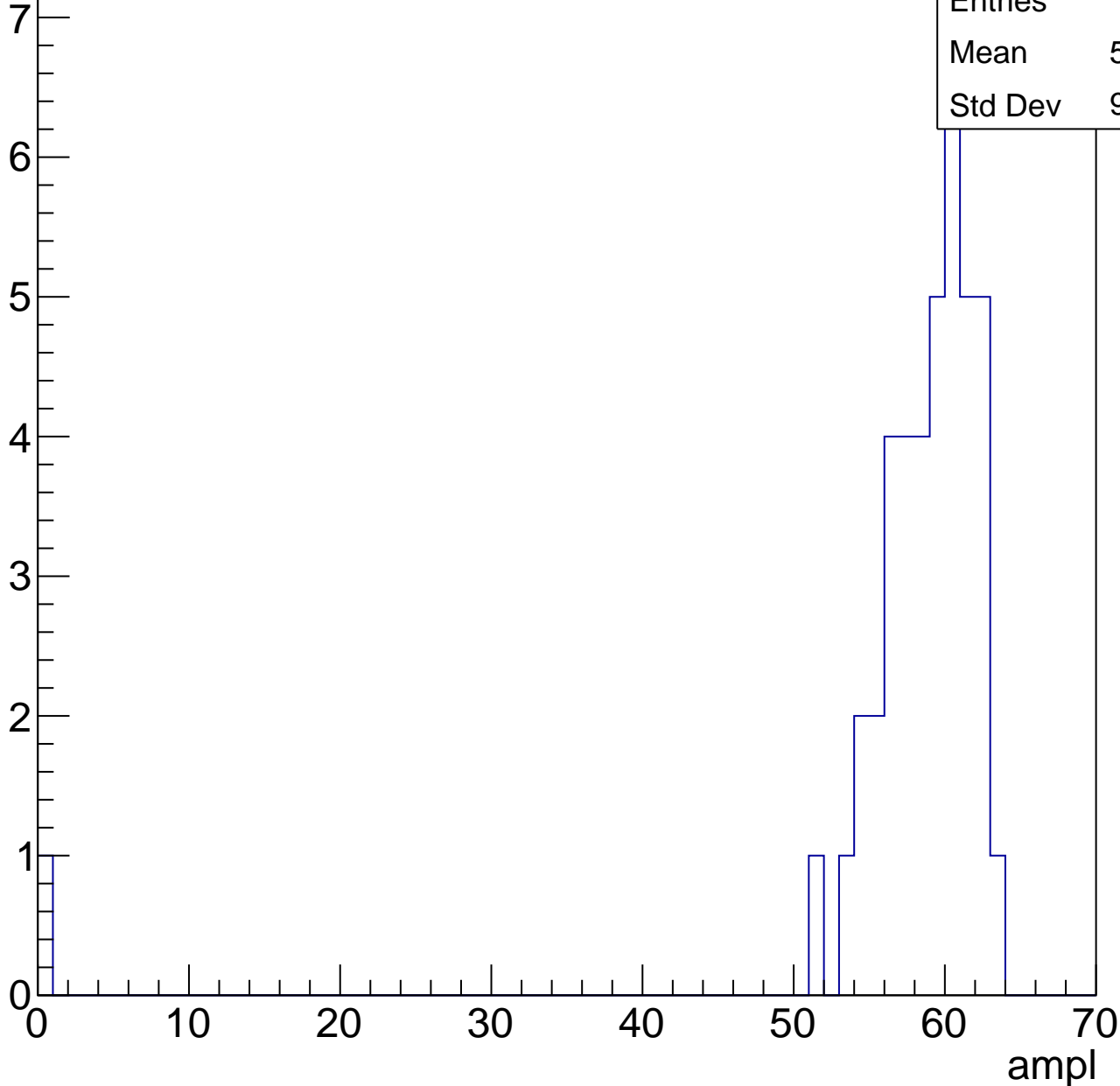


# B1L102S, U3-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	42
Mean	57.12
Std Dev	9.333

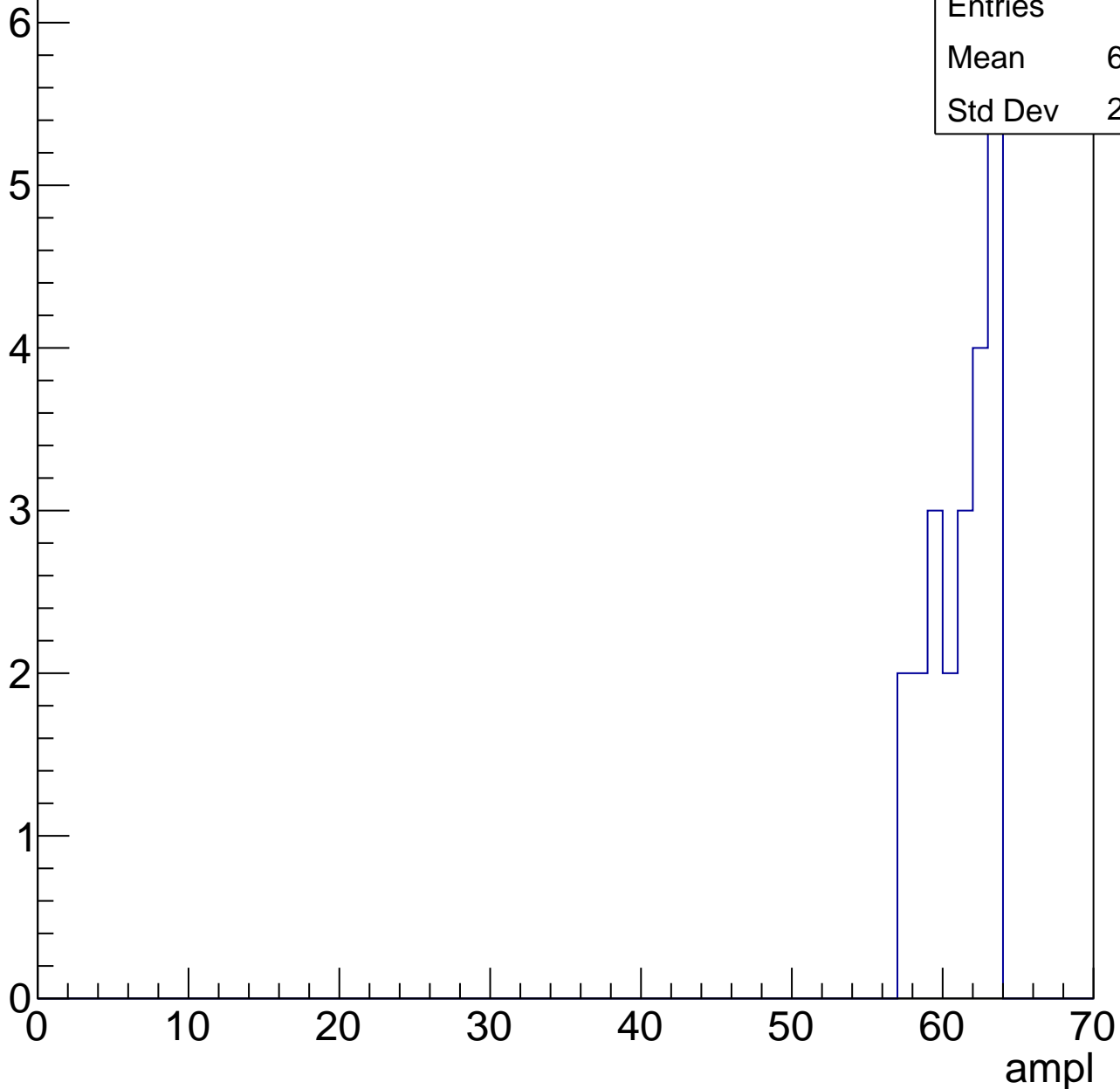


# B1L102S, U3-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	22
Mean	60.73
Std Dev	2.027

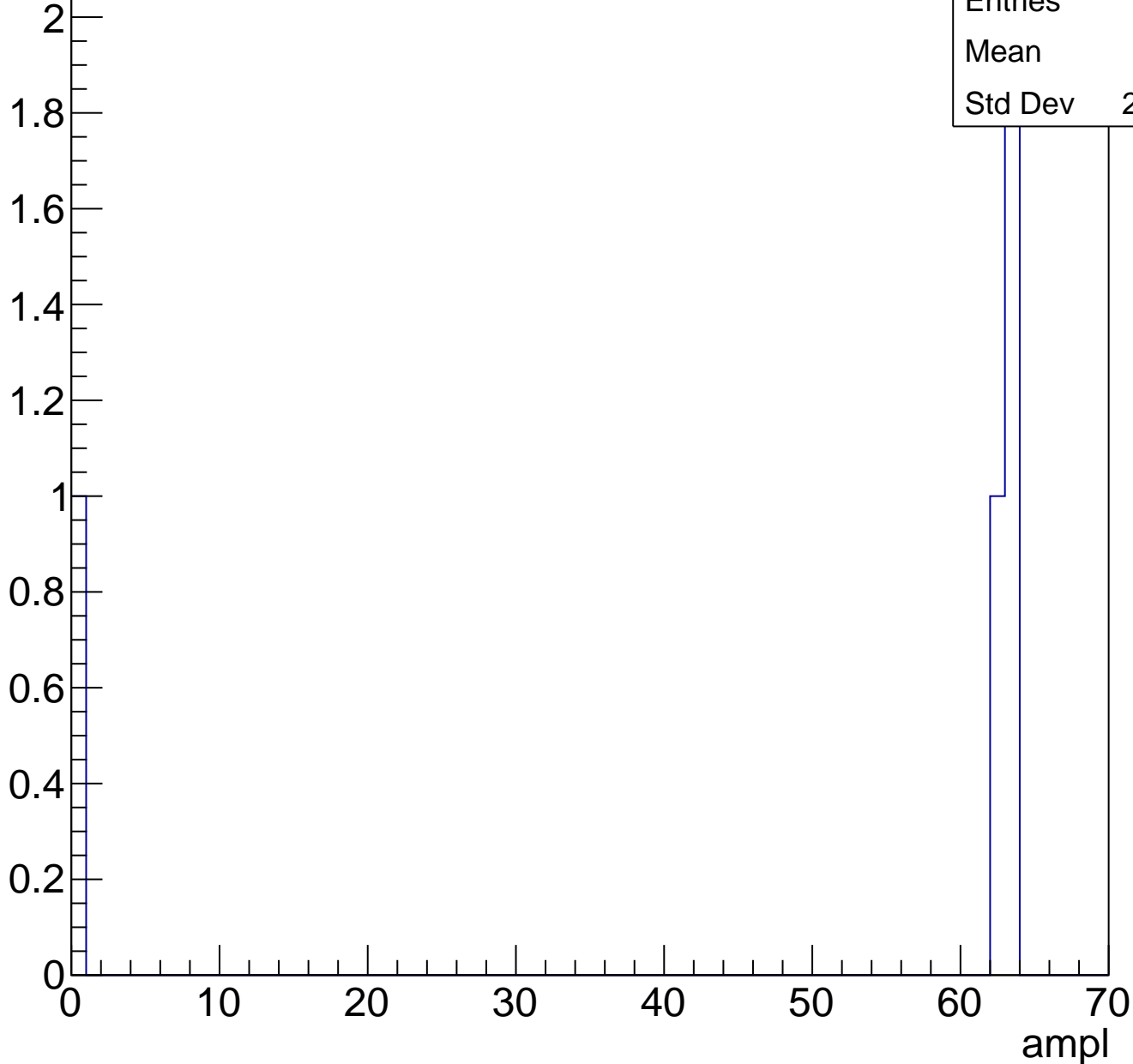




# B1L102S, U3-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch93, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	76
Mean	27.05
Std Dev	5.062

**Gaus mean : 27.7076**

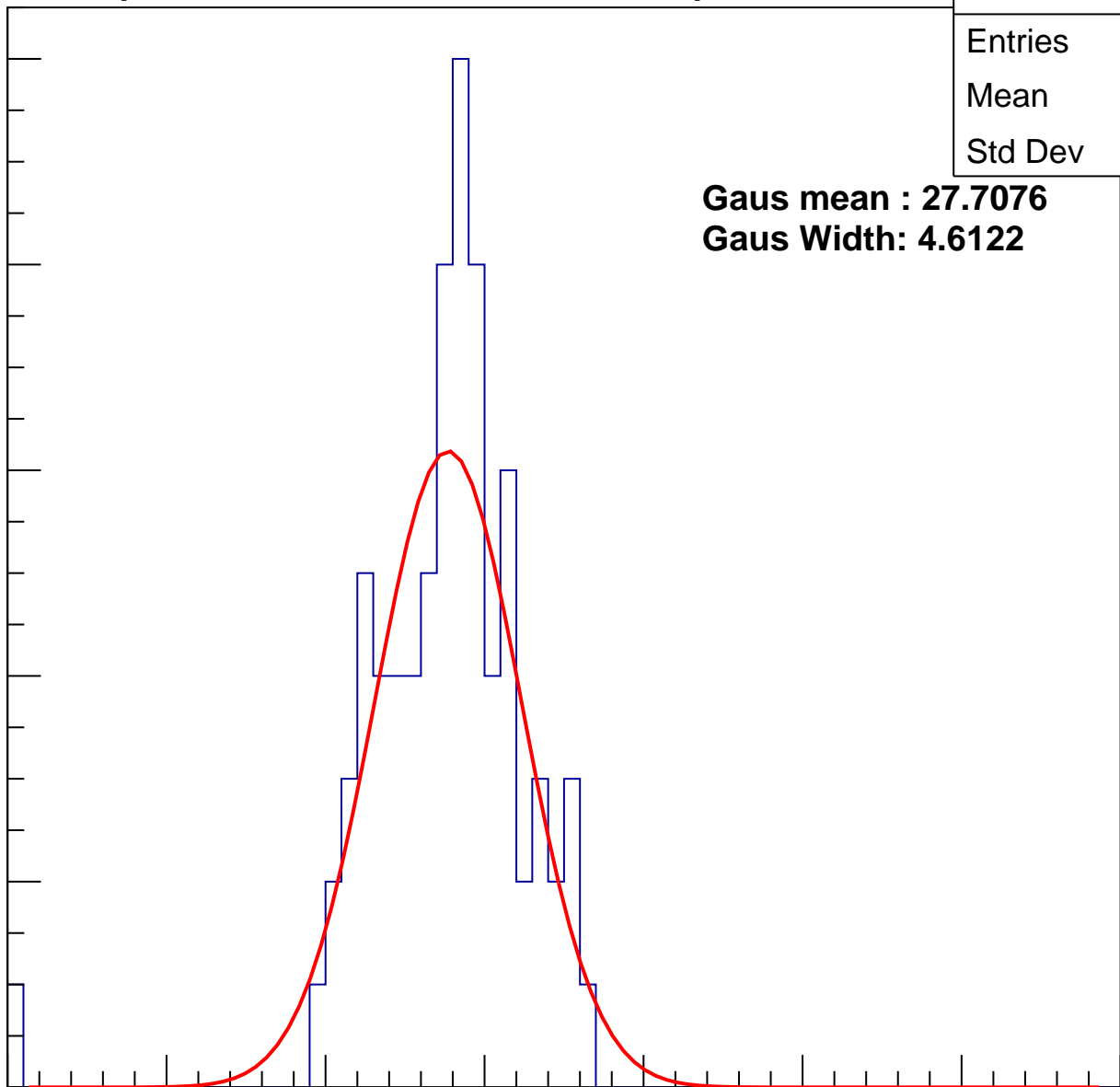
**Gaus Width: 4.6122**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U3-ch93, adc1

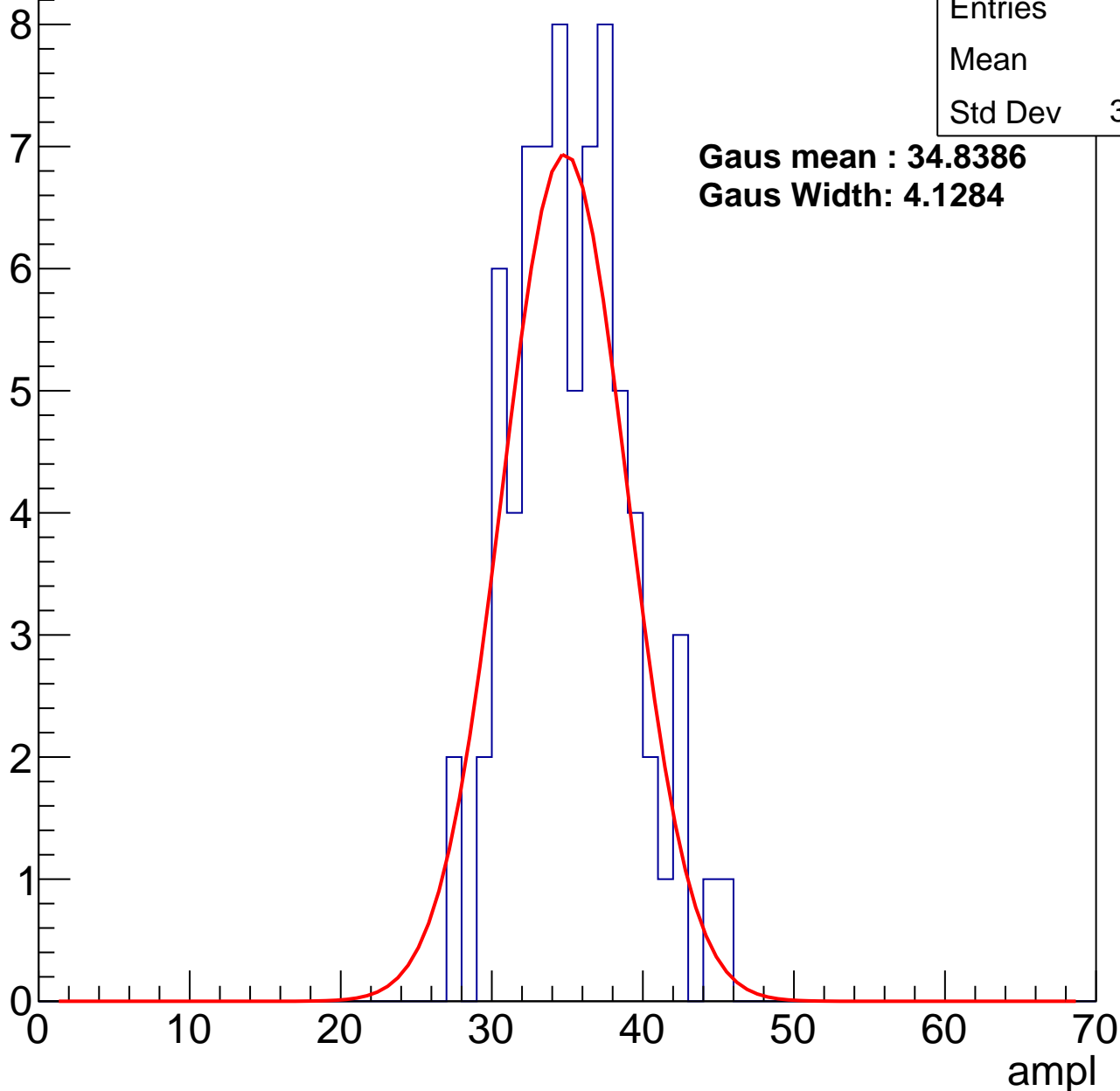
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	34.9
Std Dev	3.836

**Gaus mean : 34.8386**

**Gaus Width: 4.1284**



# B1L102S, U3-ch93, adc2

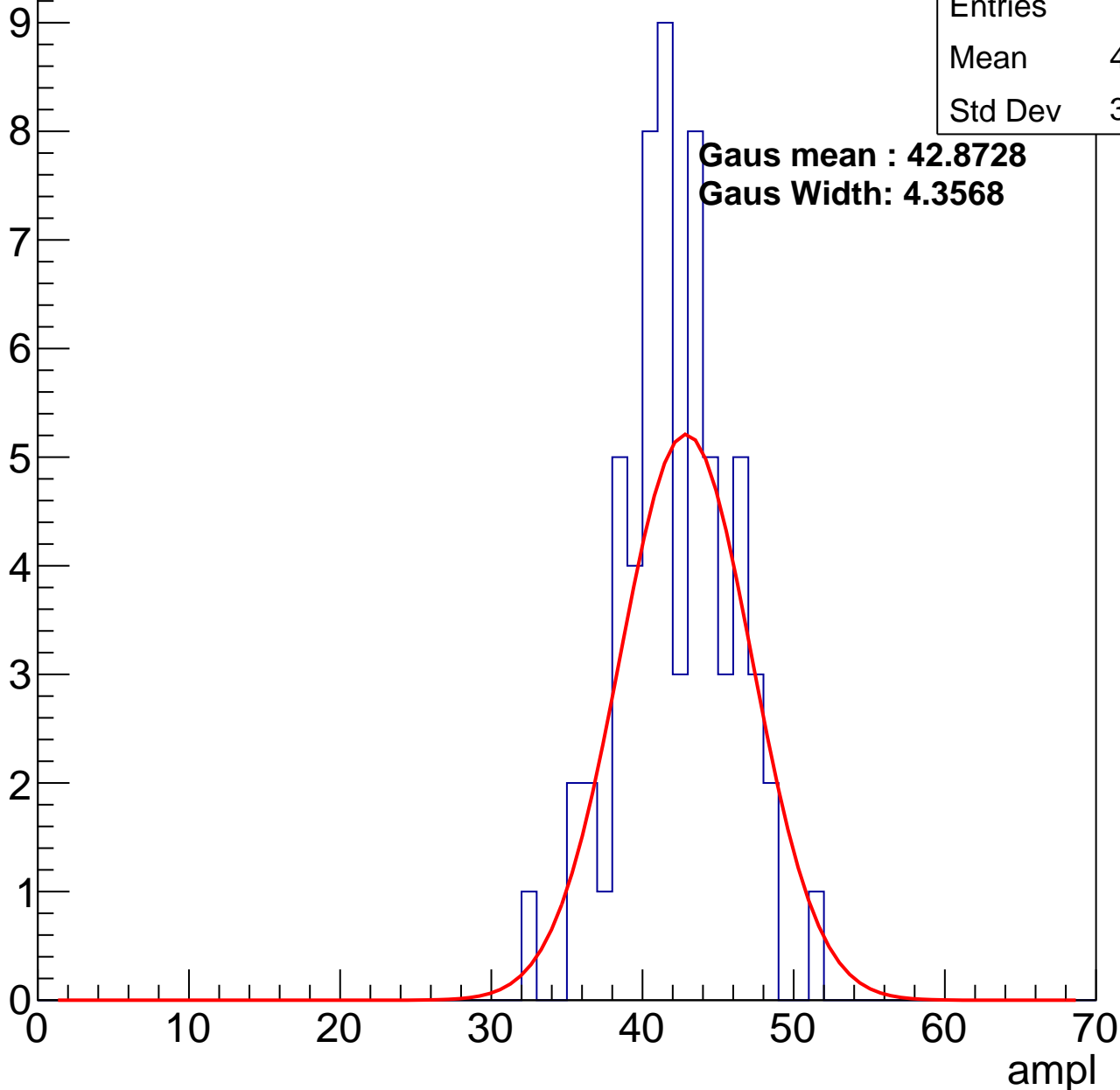
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	41.76
Std Dev	3.618

**Gaus mean : 42.8728**

**Gaus Width: 4.3568**

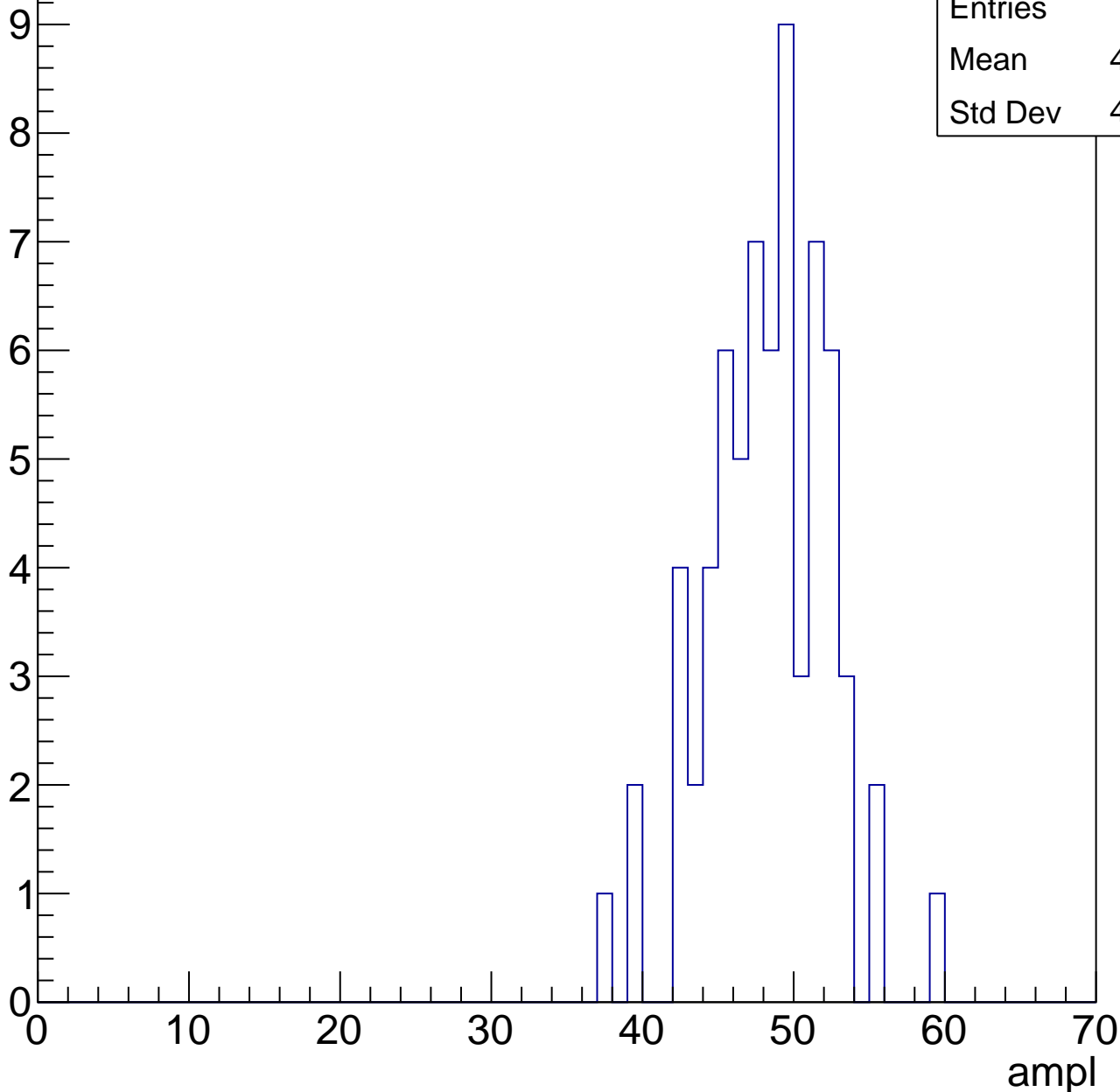


# B1L102S, U3-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

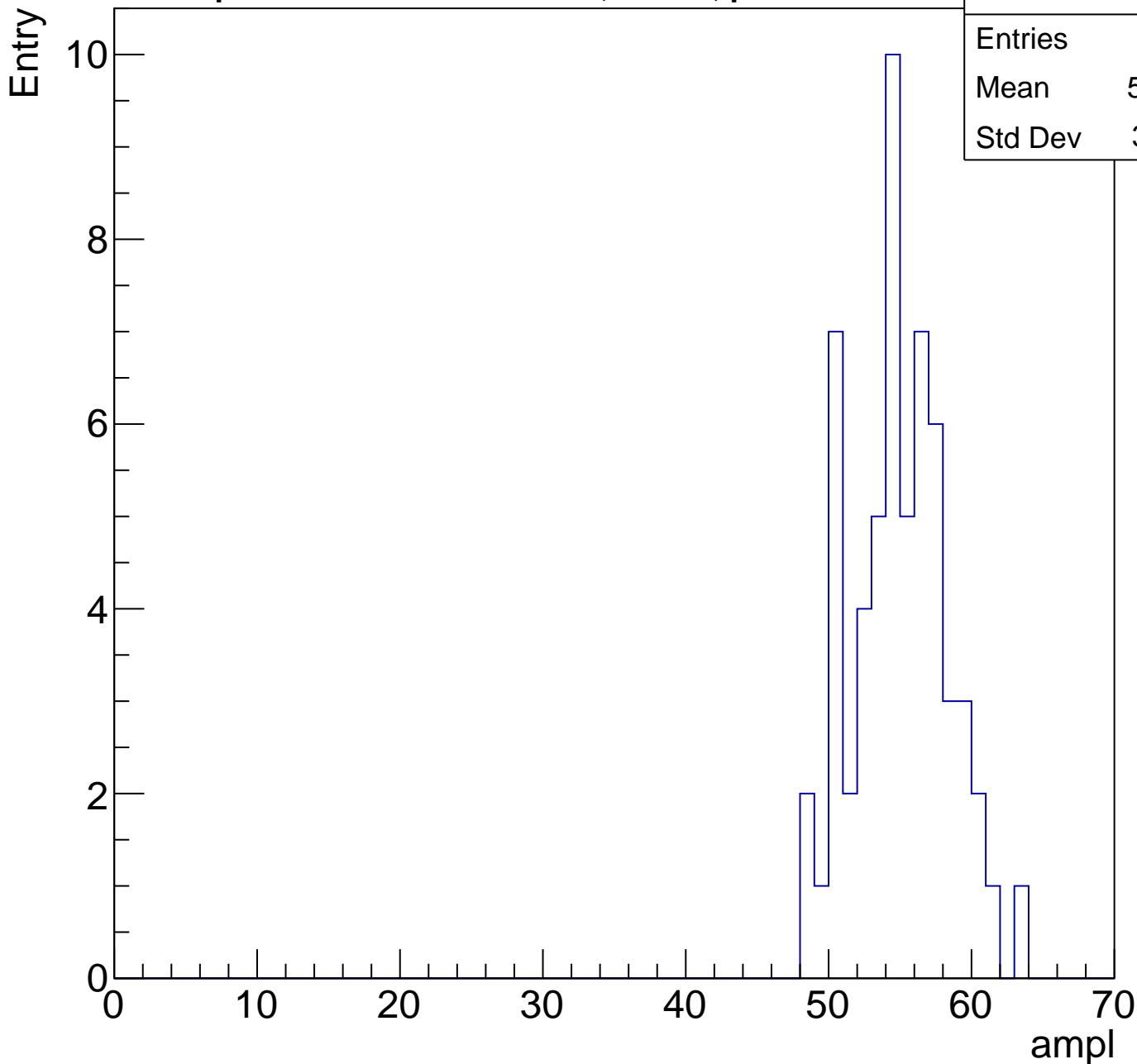
Entries	68
Mean	47.79
Std Dev	4.009



# B1L102S, U3-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	59
Mean	54.47
Std Dev	3.311

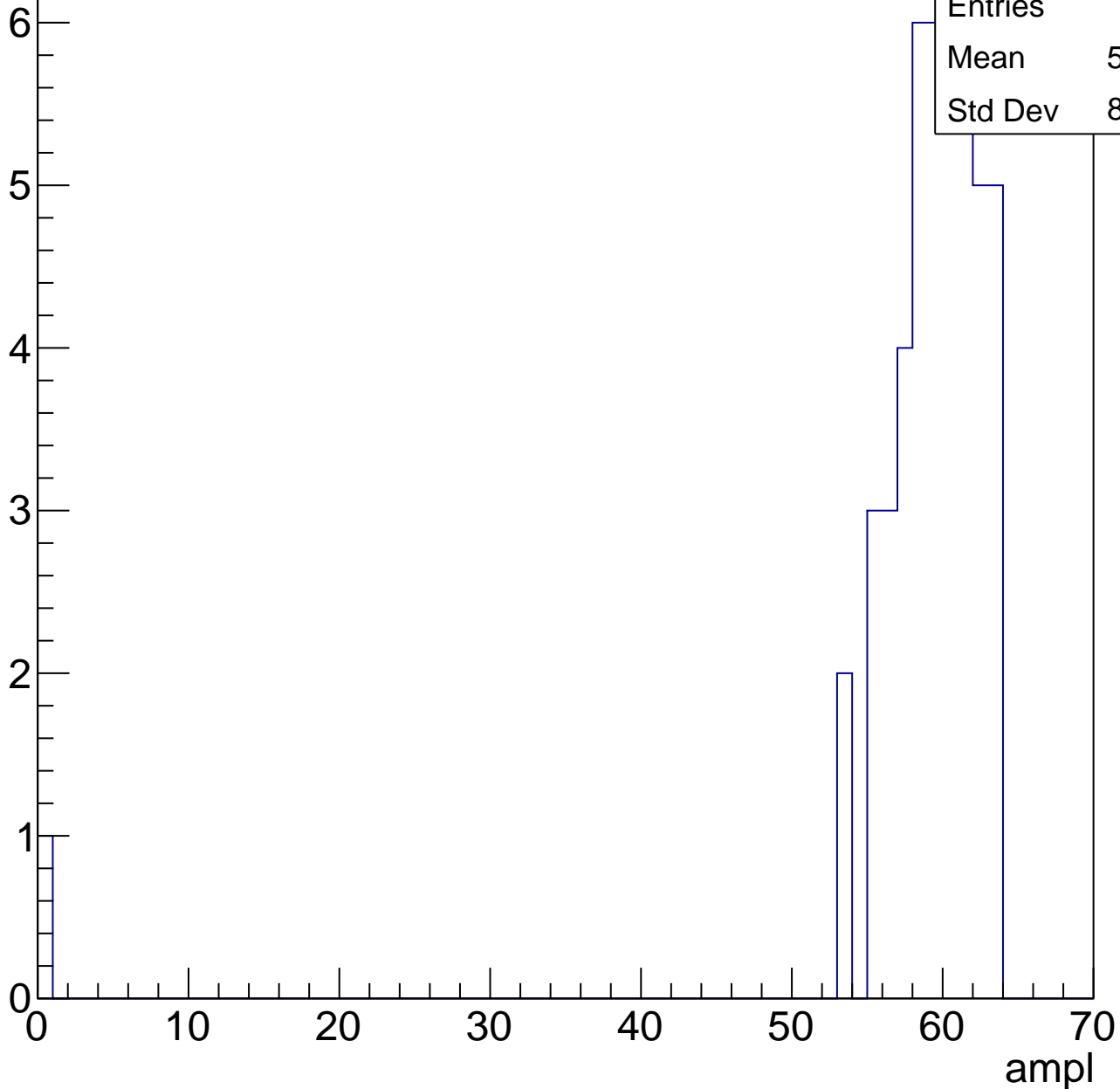


# B1L102S, U3-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	57.87
Std Dev	8.927

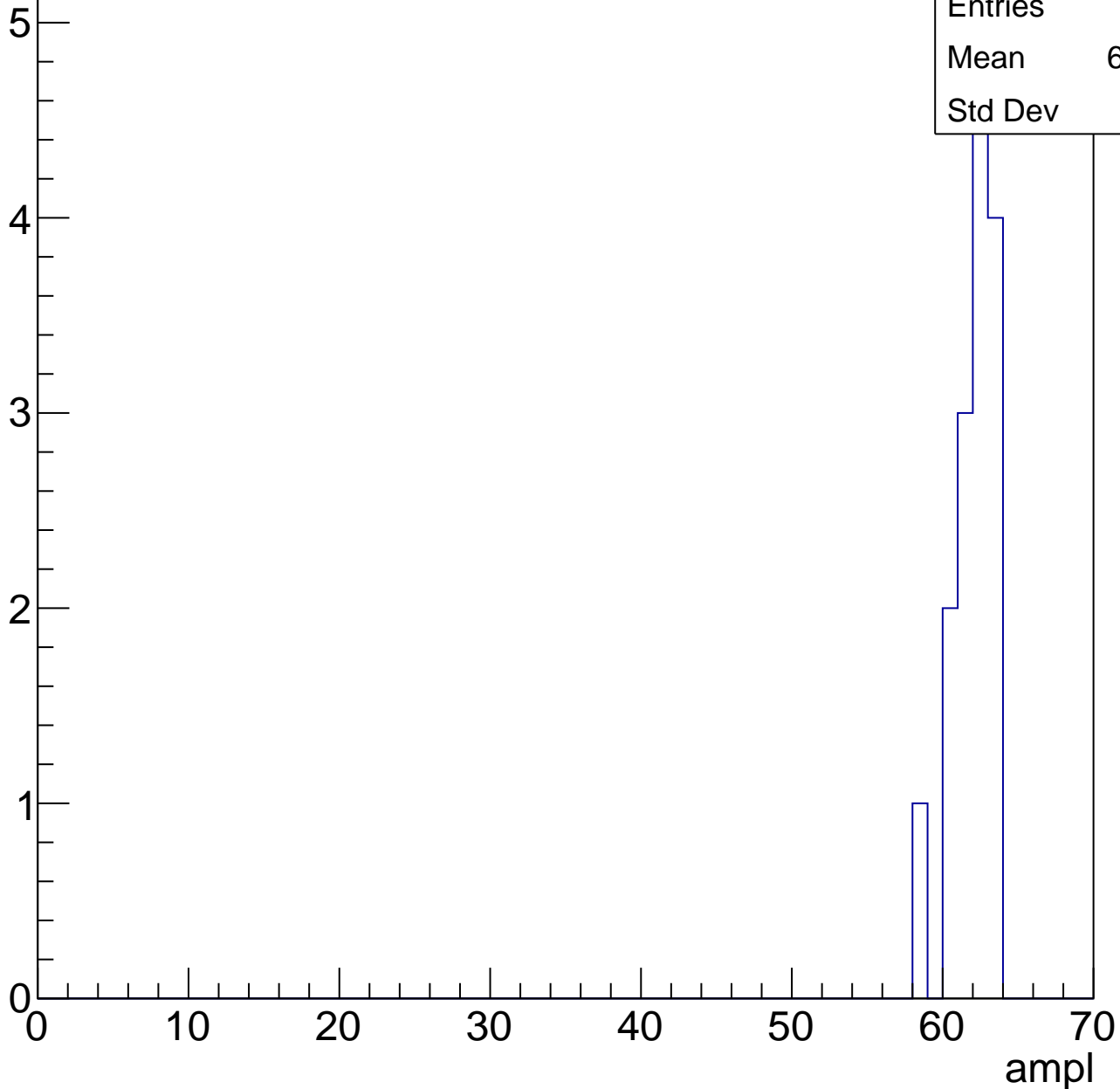


# B1L102S, U3-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	15
Mean	61.53
Std Dev	1.36





# B1L102S, U3-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U3-ch94, adc0

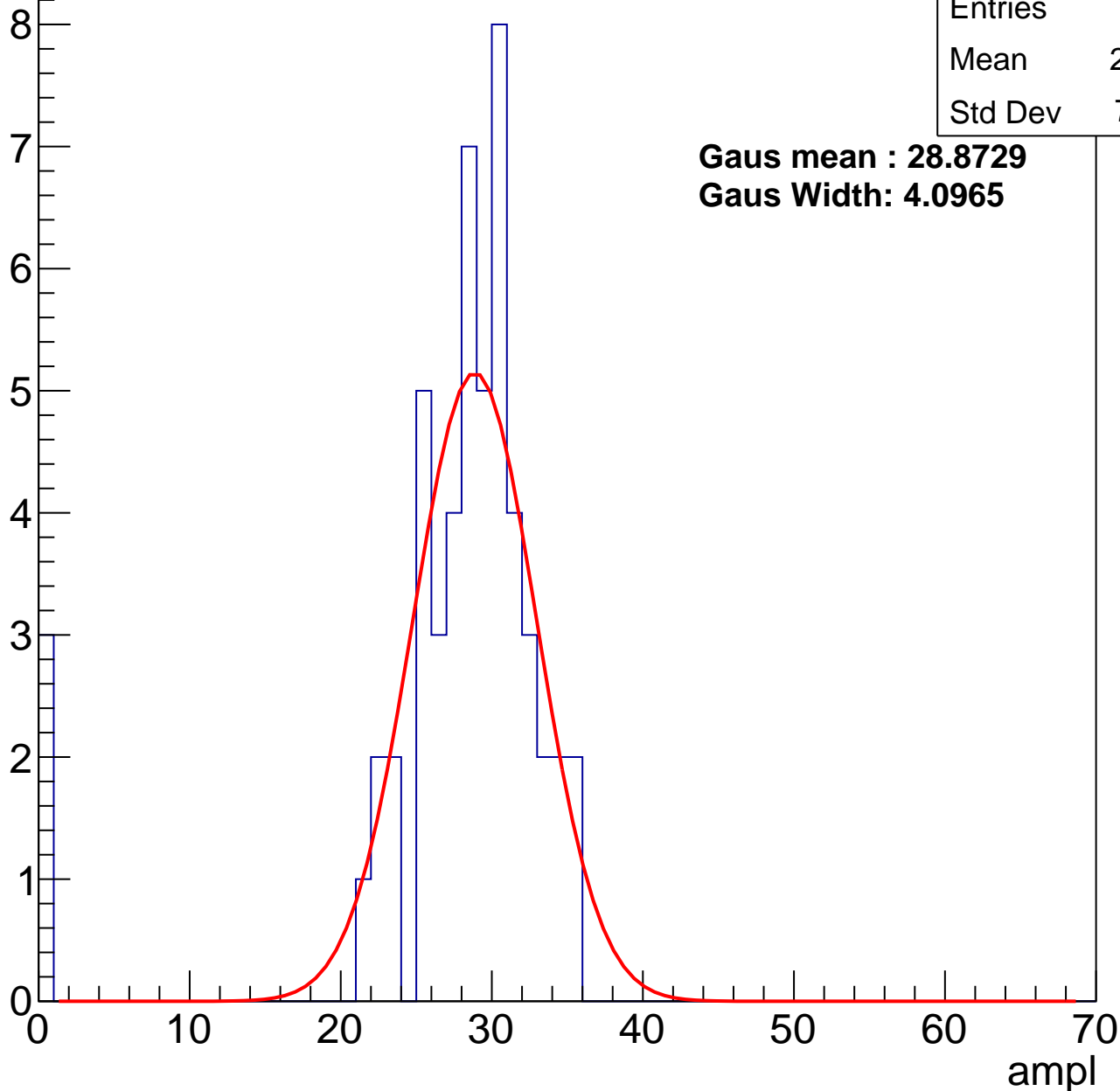
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	26.92
Std Dev	7.351

**Gaus mean : 28.8729**

**Gaus Width: 4.0965**



# B1L102S, U3-ch94, adc1

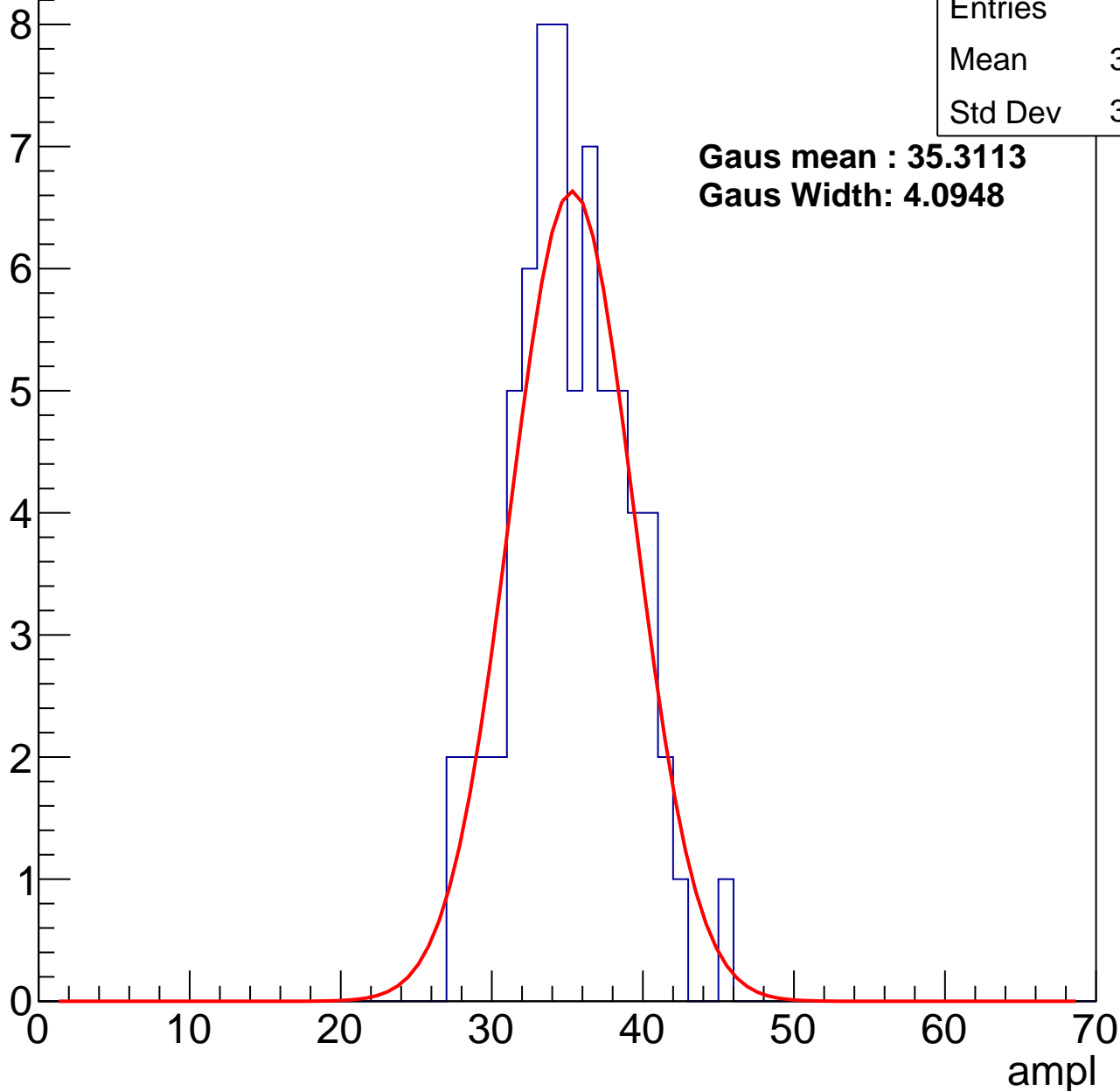
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	34.75
Std Dev	3.759

**Gaus mean : 35.3113**

**Gaus Width: 4.0948**



# B1L102S, U3-ch94, adc2

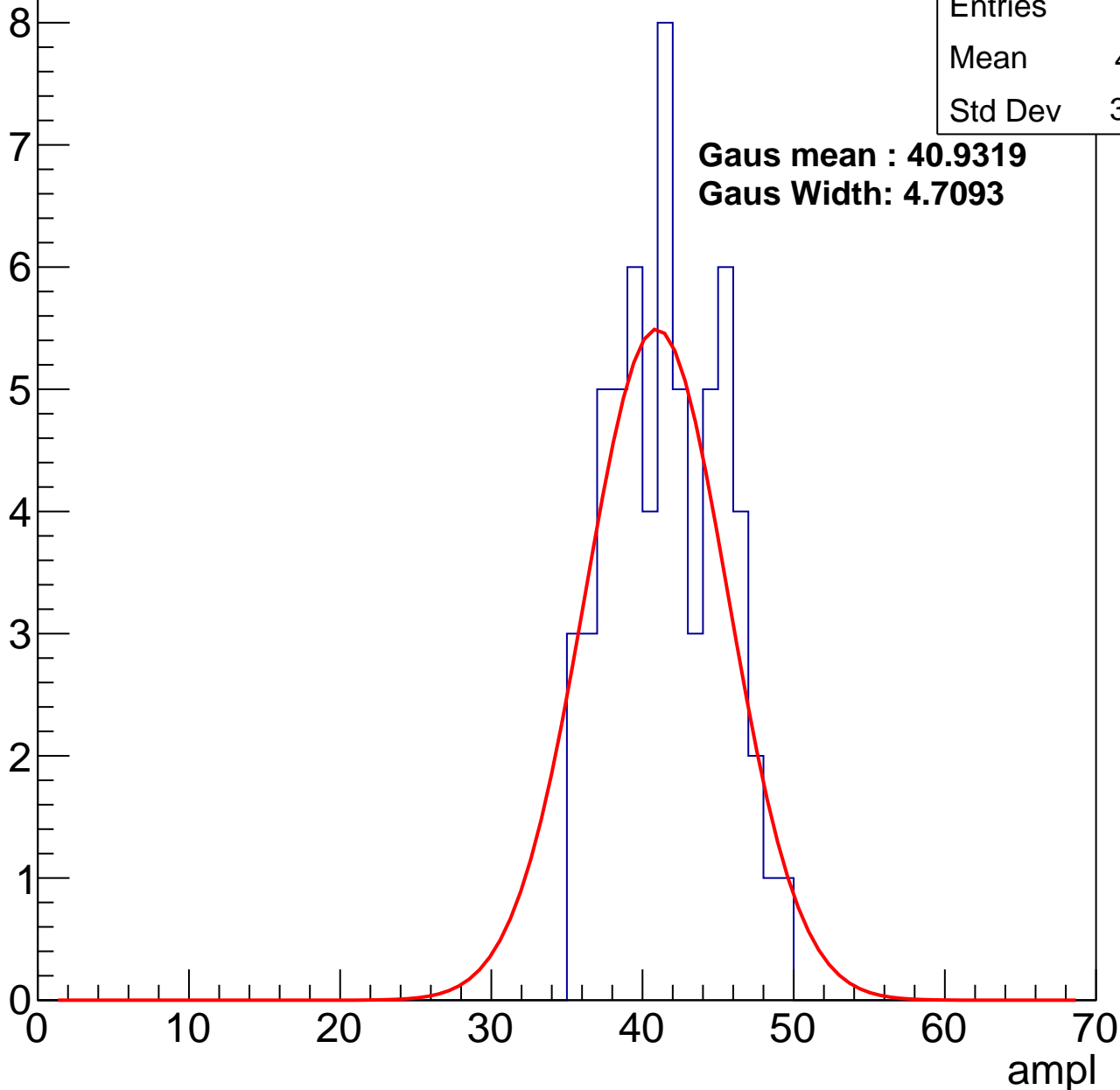
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	41.21
Std Dev	3.567

**Gaus mean : 40.9319**

**Gaus Width: 4.7093**

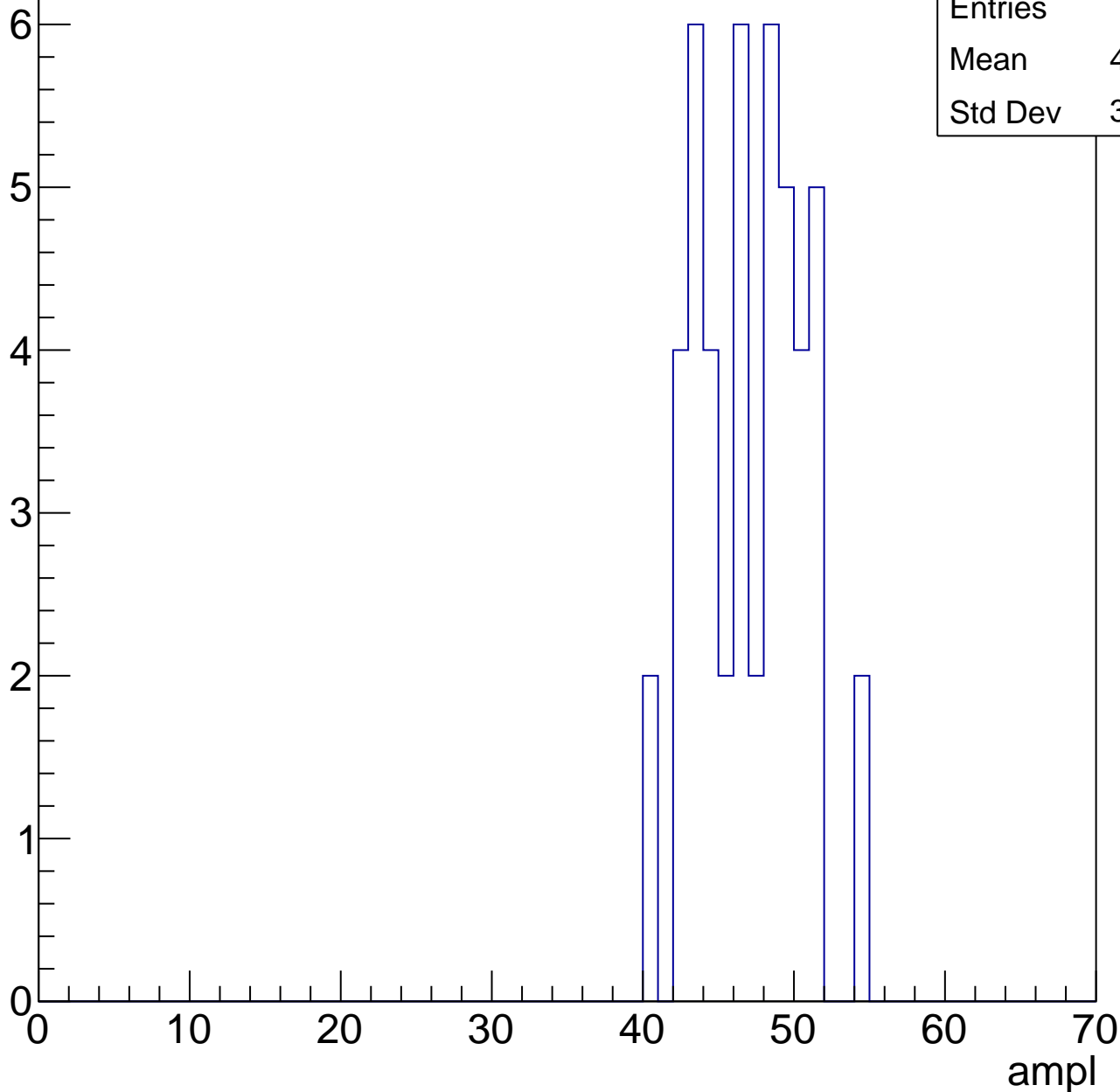


# B1L102S, U3-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	46.62
Std Dev	3.468



# B1L102S, U3-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	75
Mean	52.41
Std Dev	3.67

Entry

10

8

6

4

2

0

0

10

20

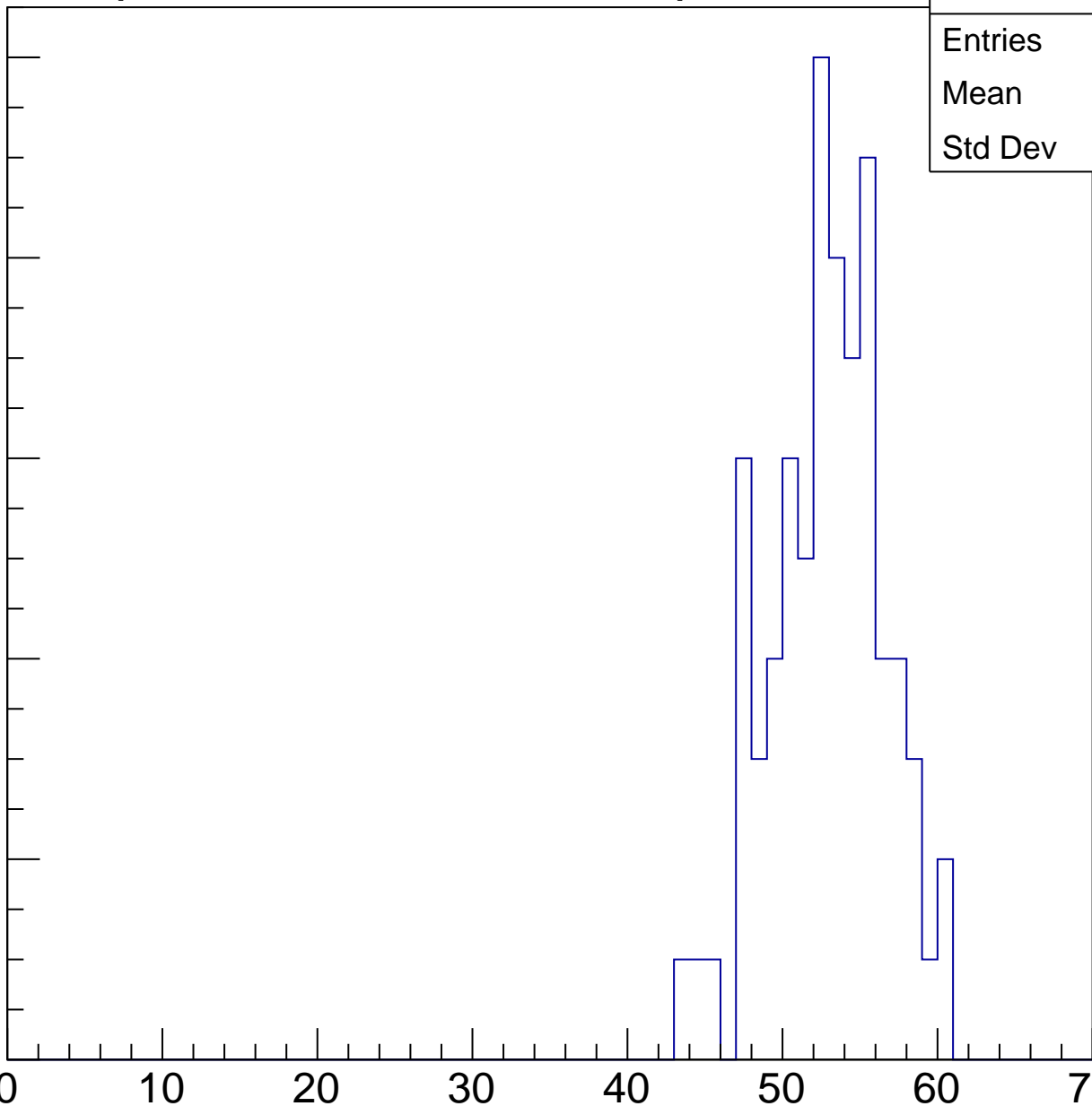
30

40

50

60

ampl



# B1L102S, U3-ch94, adc5

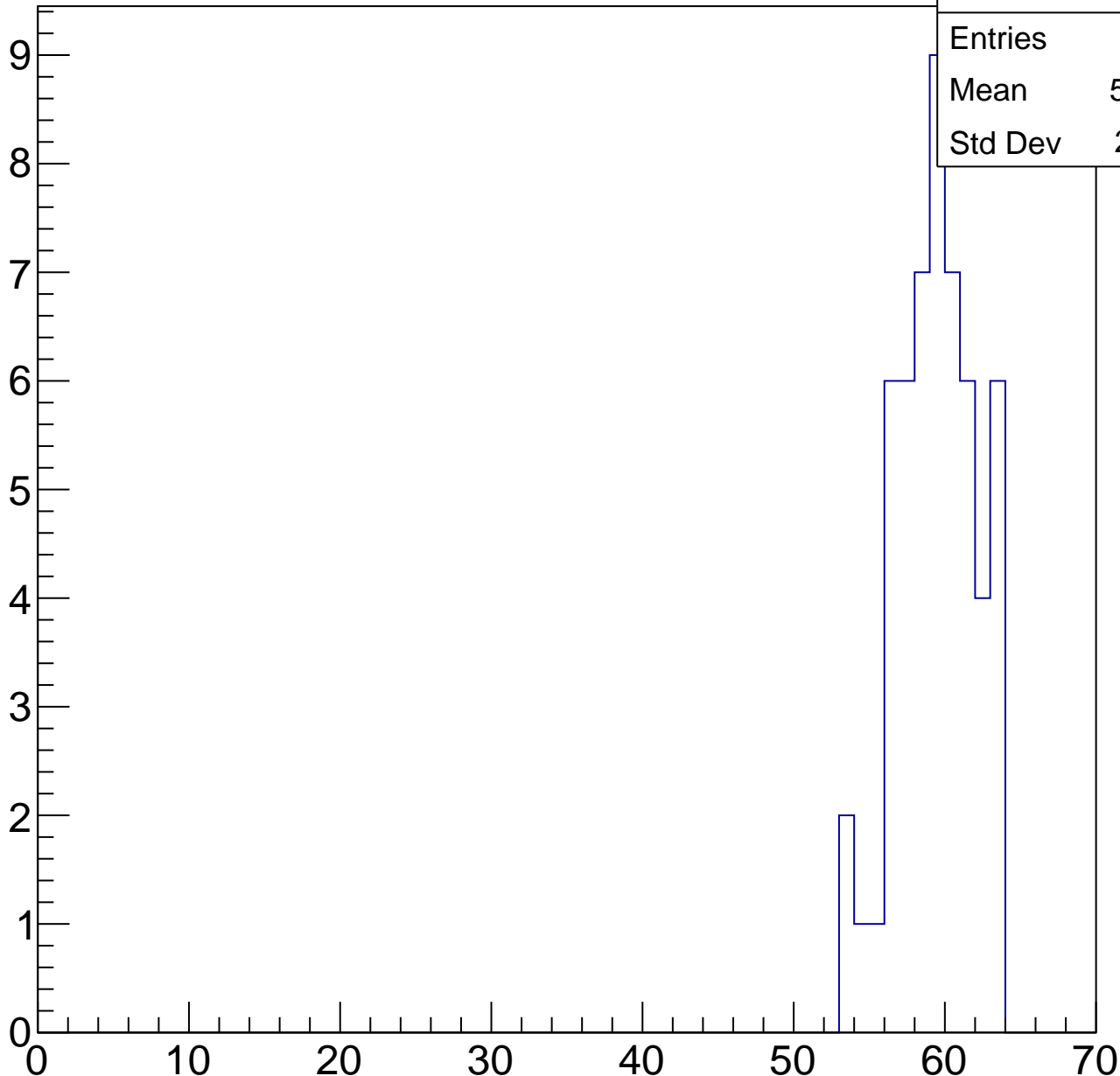
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	55
Mean	58.95
Std Dev	2.561

ampl

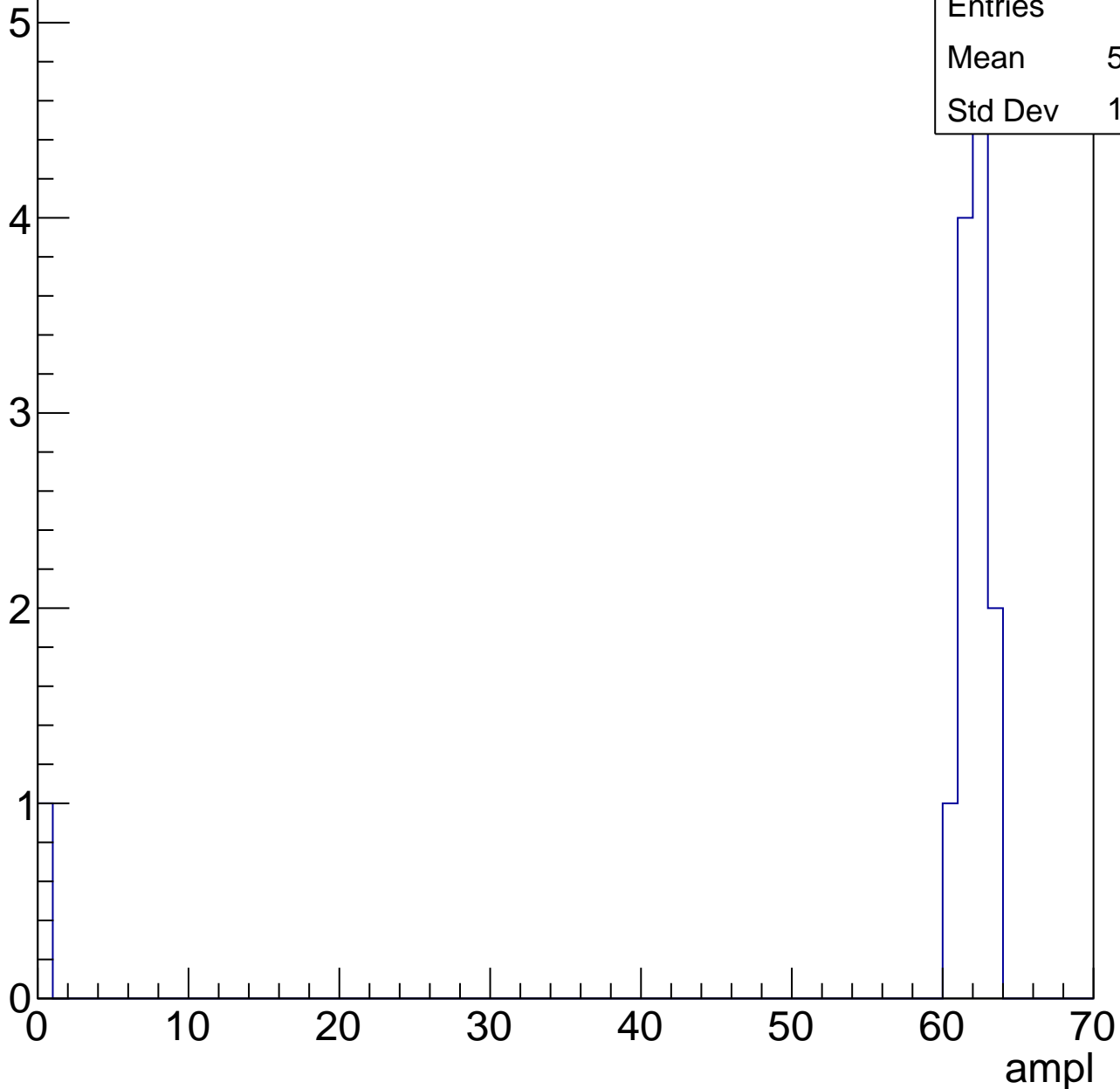


# B1L102S, U3-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	13
Mean	56.92
Std Dev	16.45

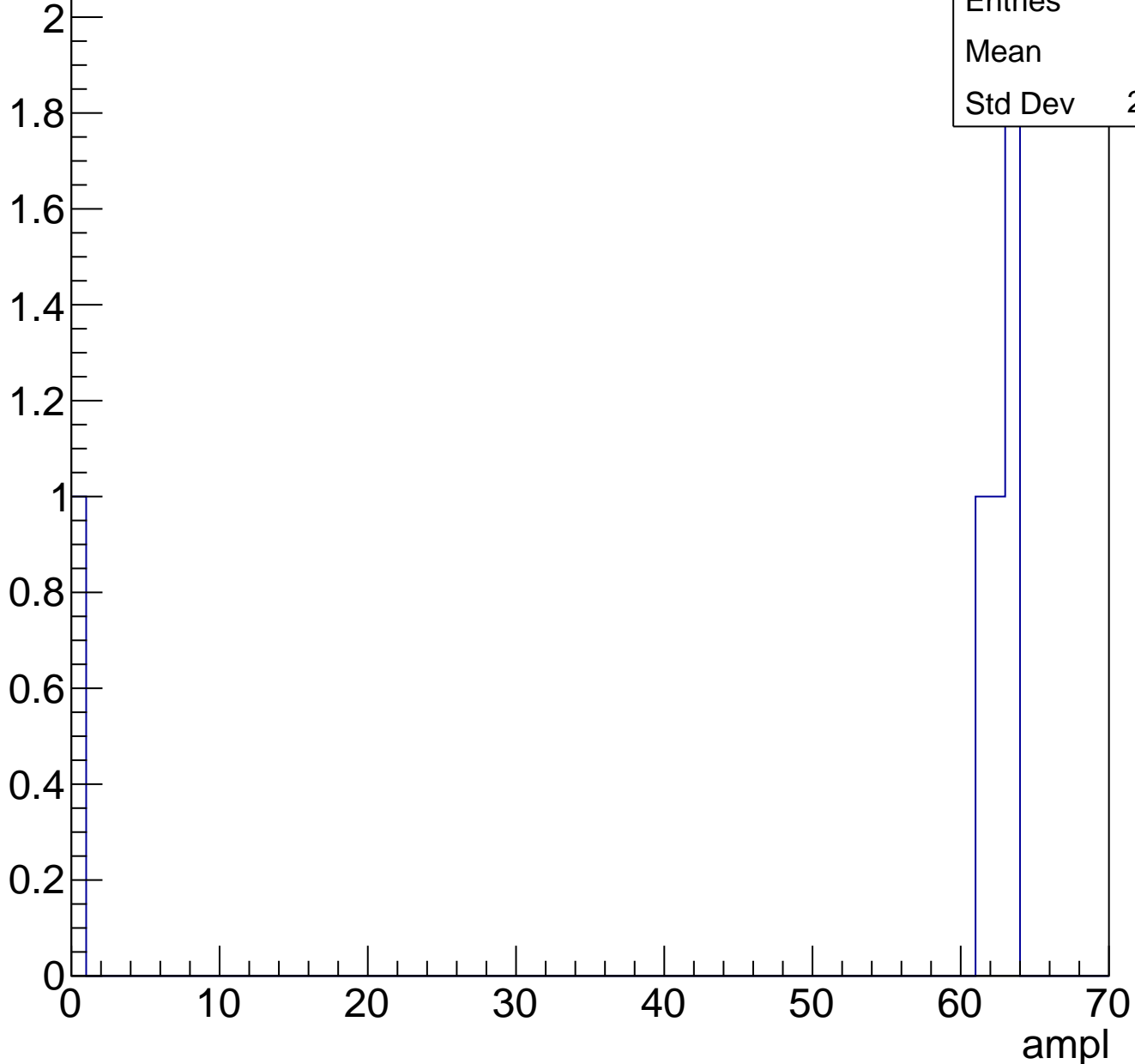




# B1L102S, U3-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch95, adc0

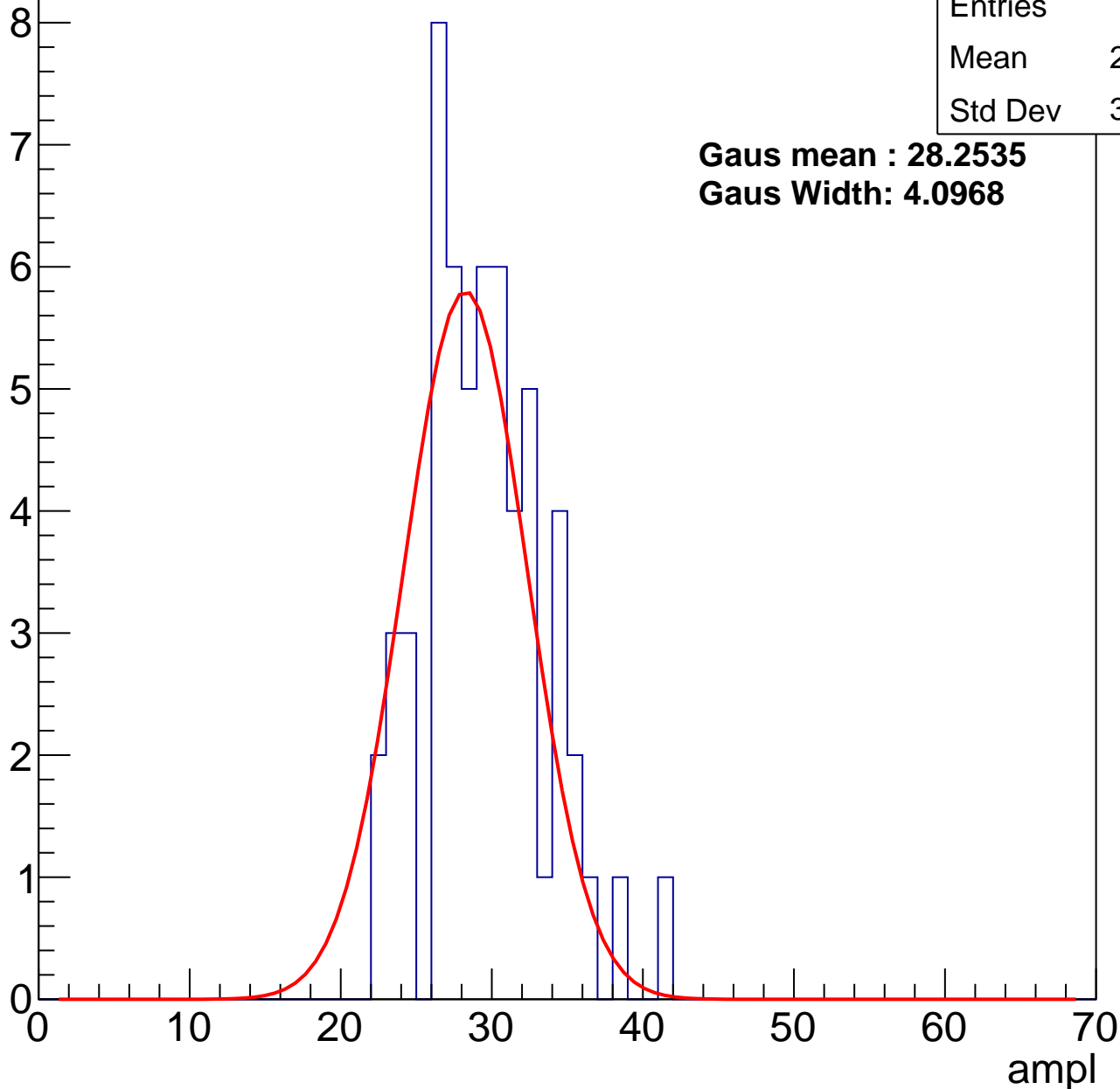
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	29.09
Std Dev	3.962

**Gaus mean : 28.2535**

**Gaus Width: 4.0968**



# B1L102S, U3-ch95, adc1

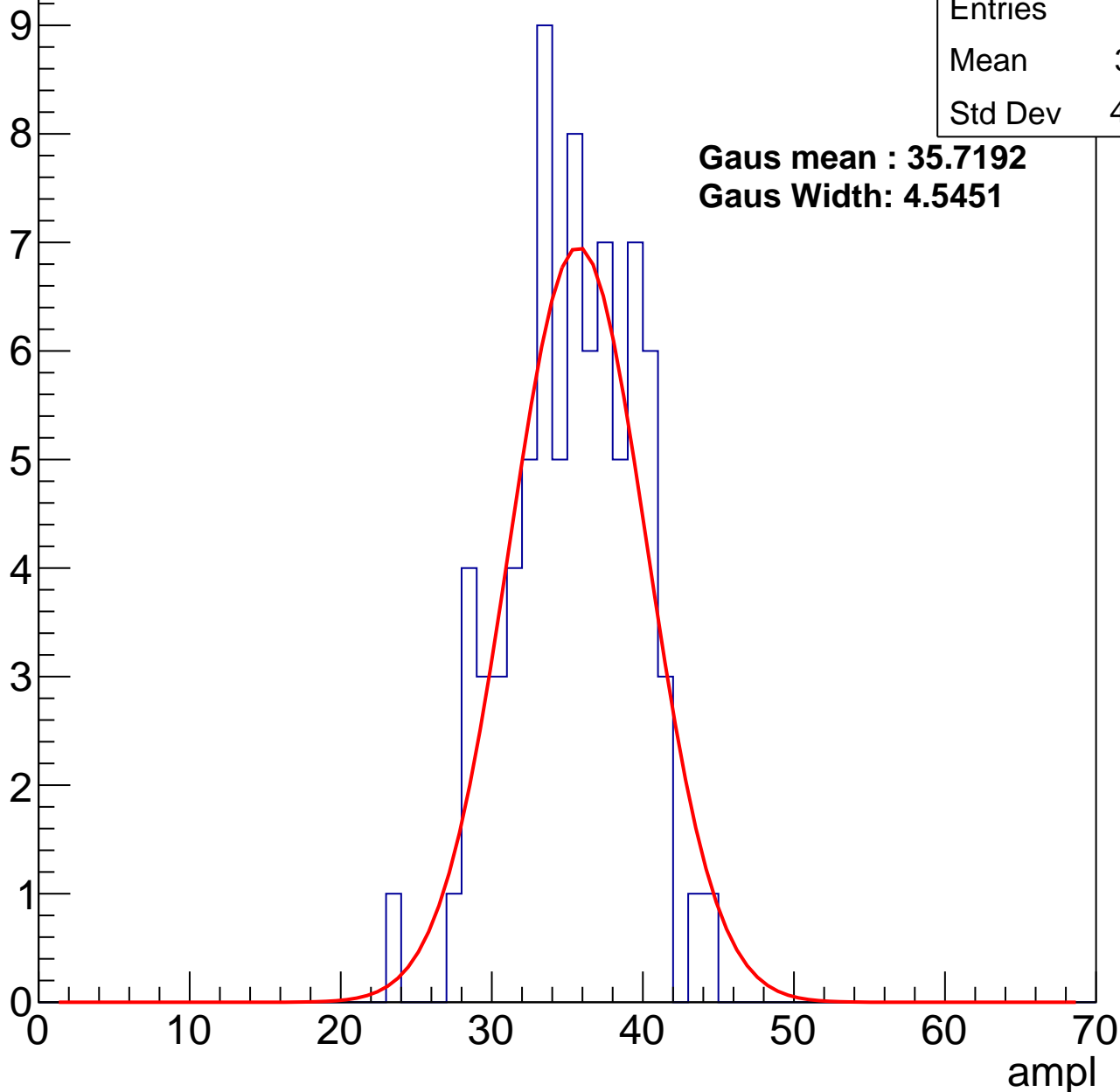
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	34.91
Std Dev	4.104

**Gaus mean : 35.7192**

**Gaus Width: 4.5451**



# B1L102S, U3-ch95, adc2

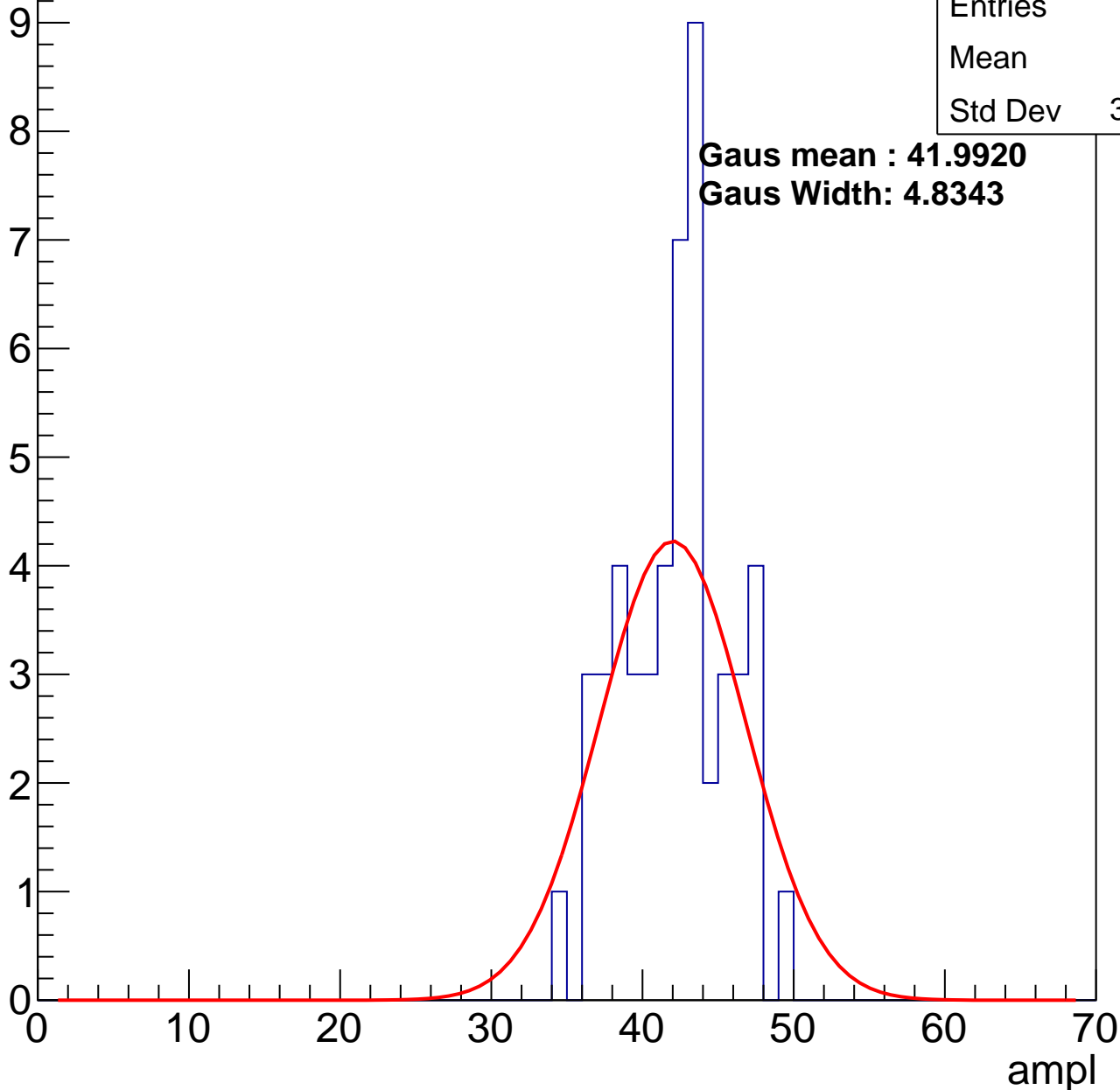
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	41.7
Std Dev	3.437

**Gaus mean : 41.9920**

**Gaus Width: 4.8343**



# B1L102S, U3-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	86
Mean	48.52
Std Dev	3.672

Entry

10

8

6

4

2

0

0

10

20

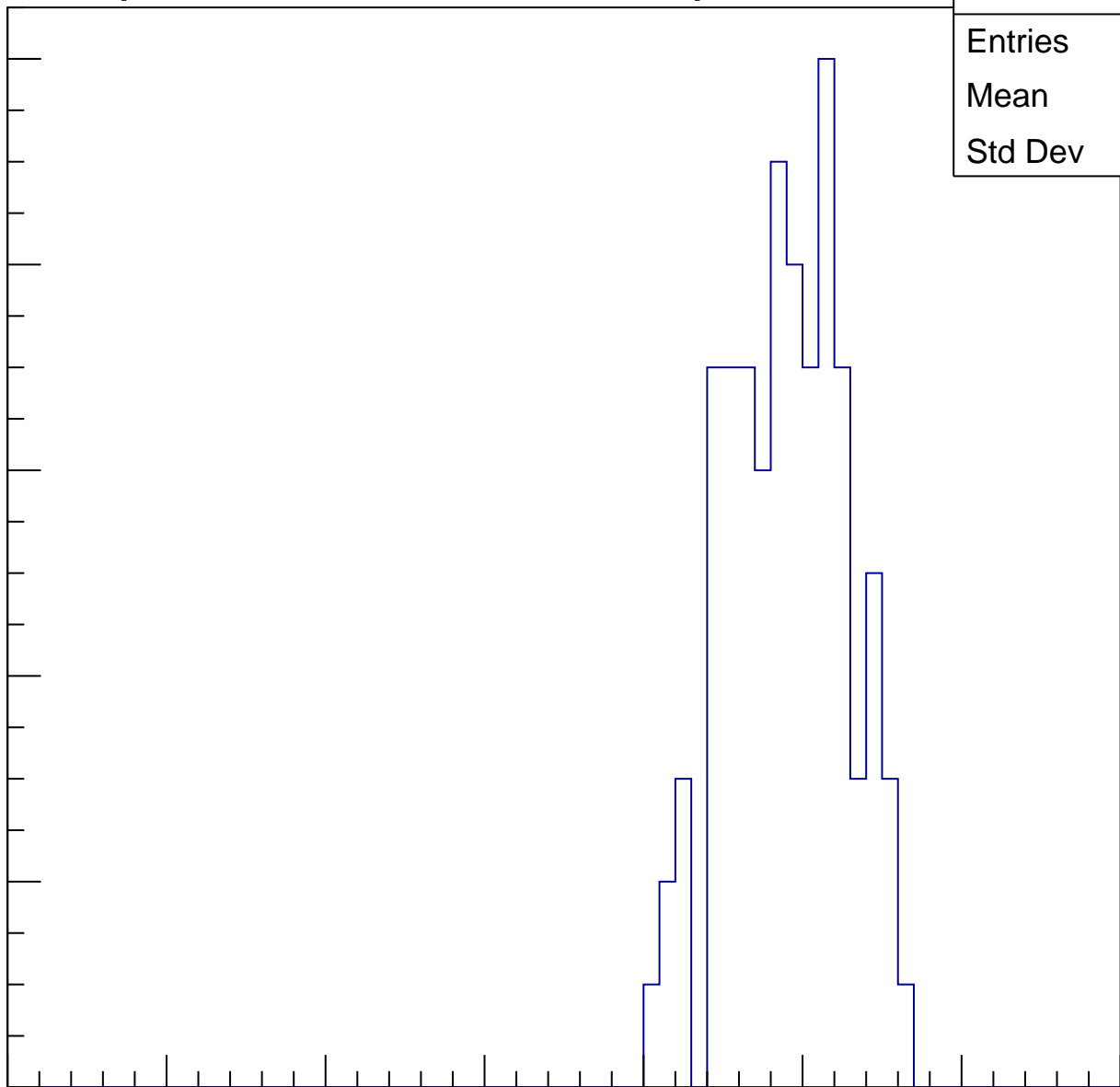
30

40

50

60

ampl

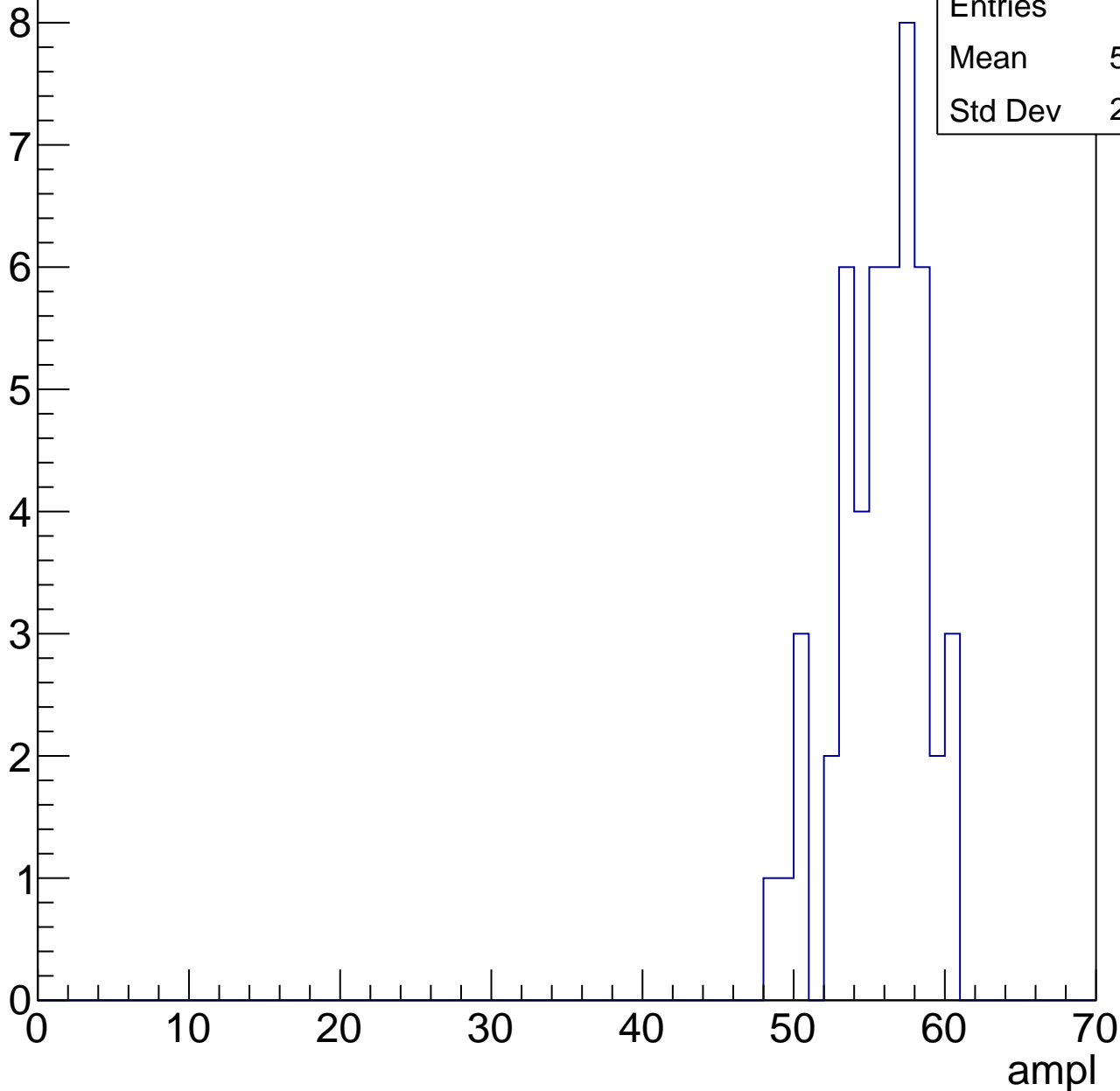


# B1L102S, U3-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	55.27
Std Dev	2.892



# B1L102S, U3-ch95, adc5

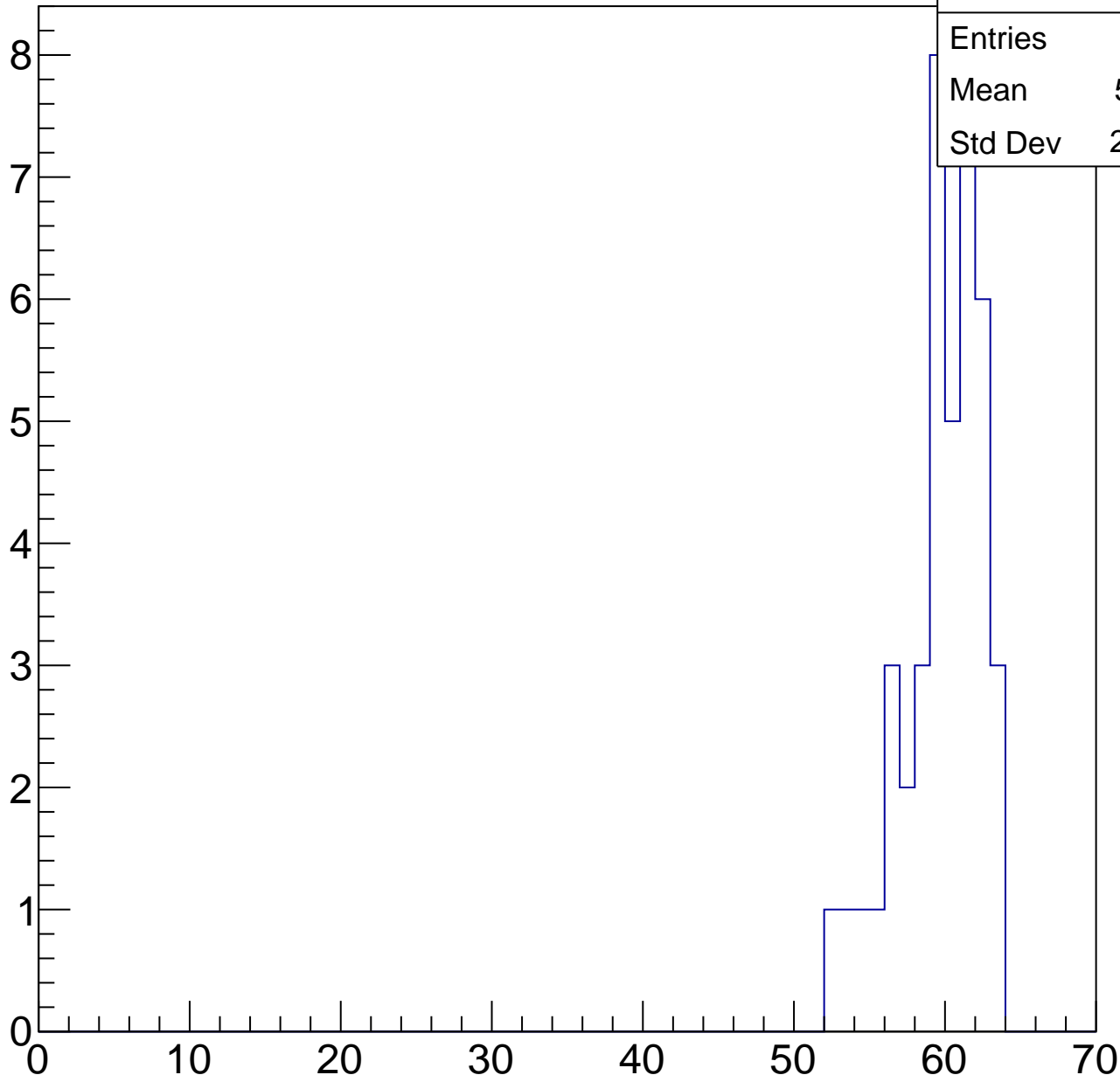
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	42
Mean	59.31
Std Dev	2.668

ampl

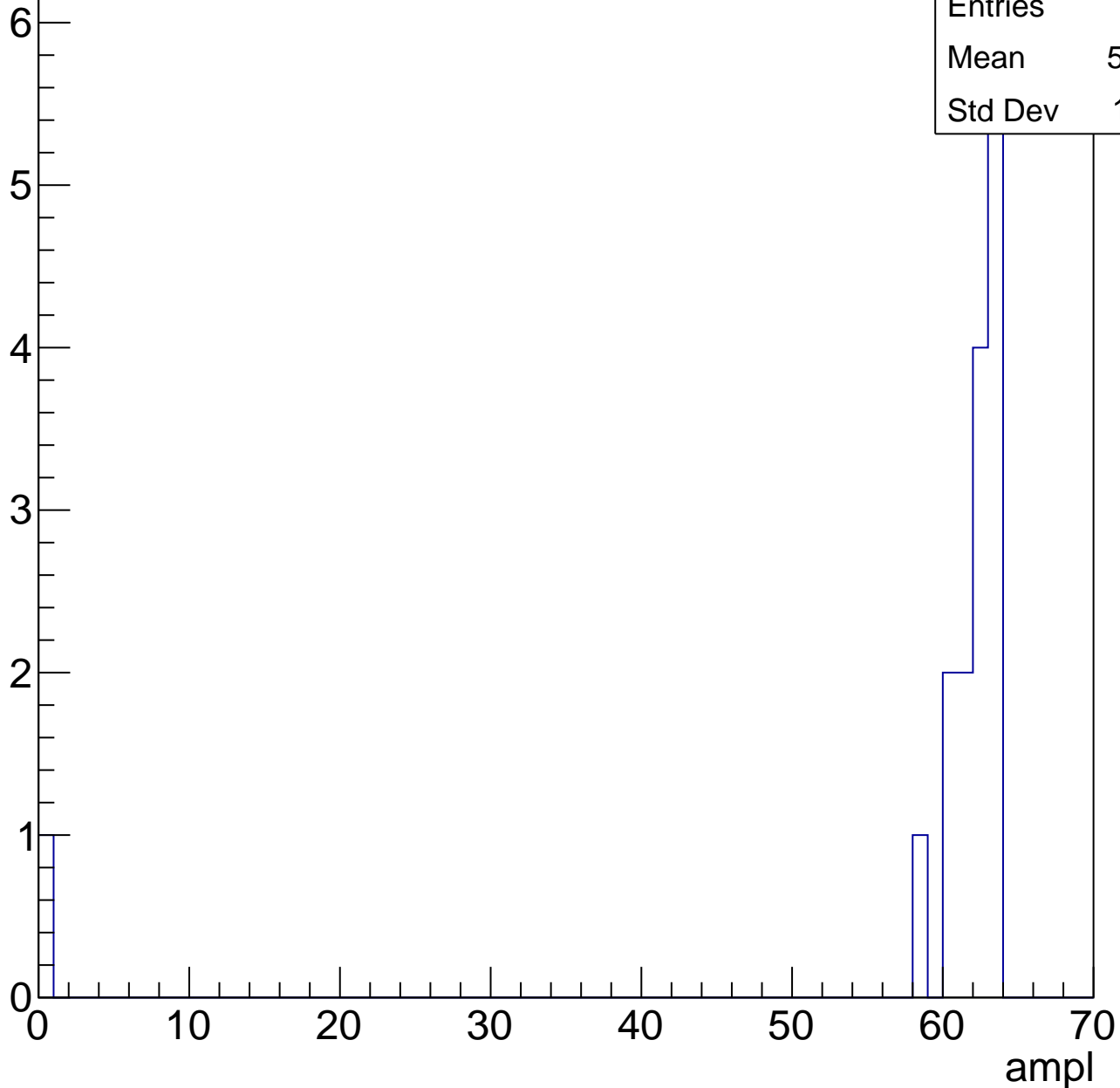


# B1L102S, U3-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	16
Mean	57.88
Std Dev	15.01





# B1L102S, U3-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch96, adc0

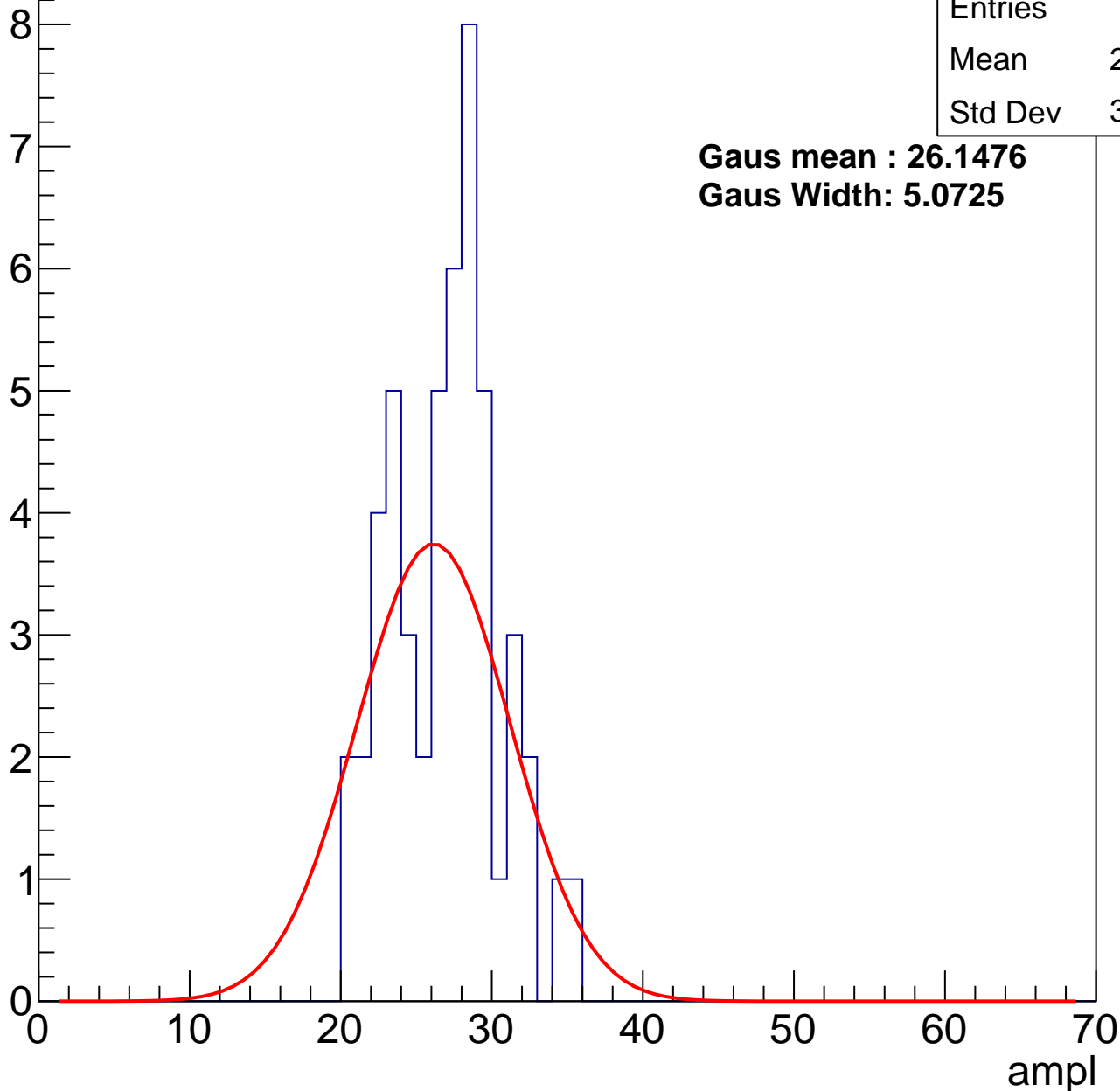
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	26.48
Std Dev	3.534

**Gaus mean : 26.1476**

**Gaus Width: 5.0725**



# B1L102S, U3-ch96, adc1

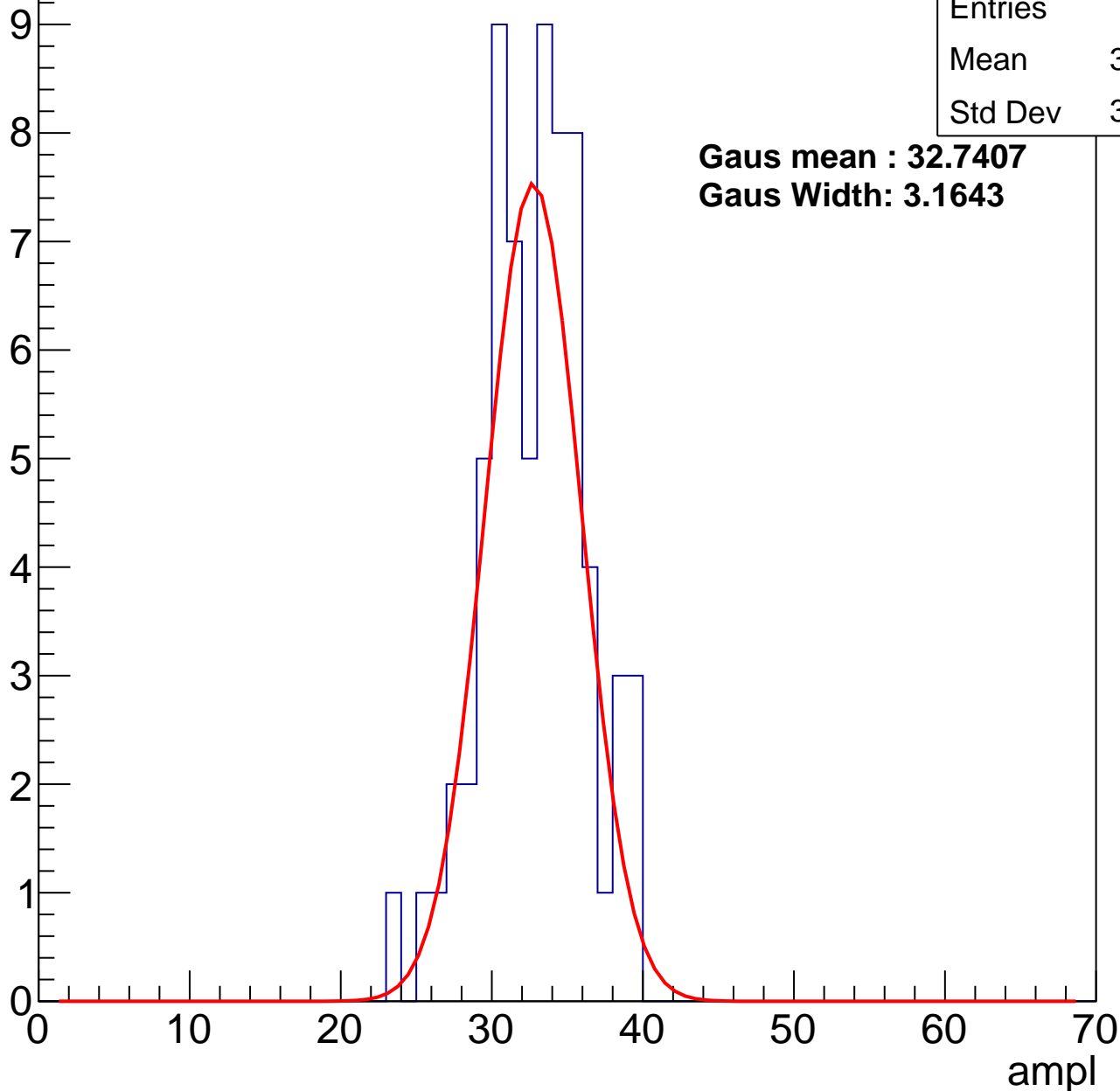
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	32.42
Std Dev	3.364

**Gaus mean : 32.7407**

**Gaus Width: 3.1643**



# B1L102S, U3-ch96, adc2

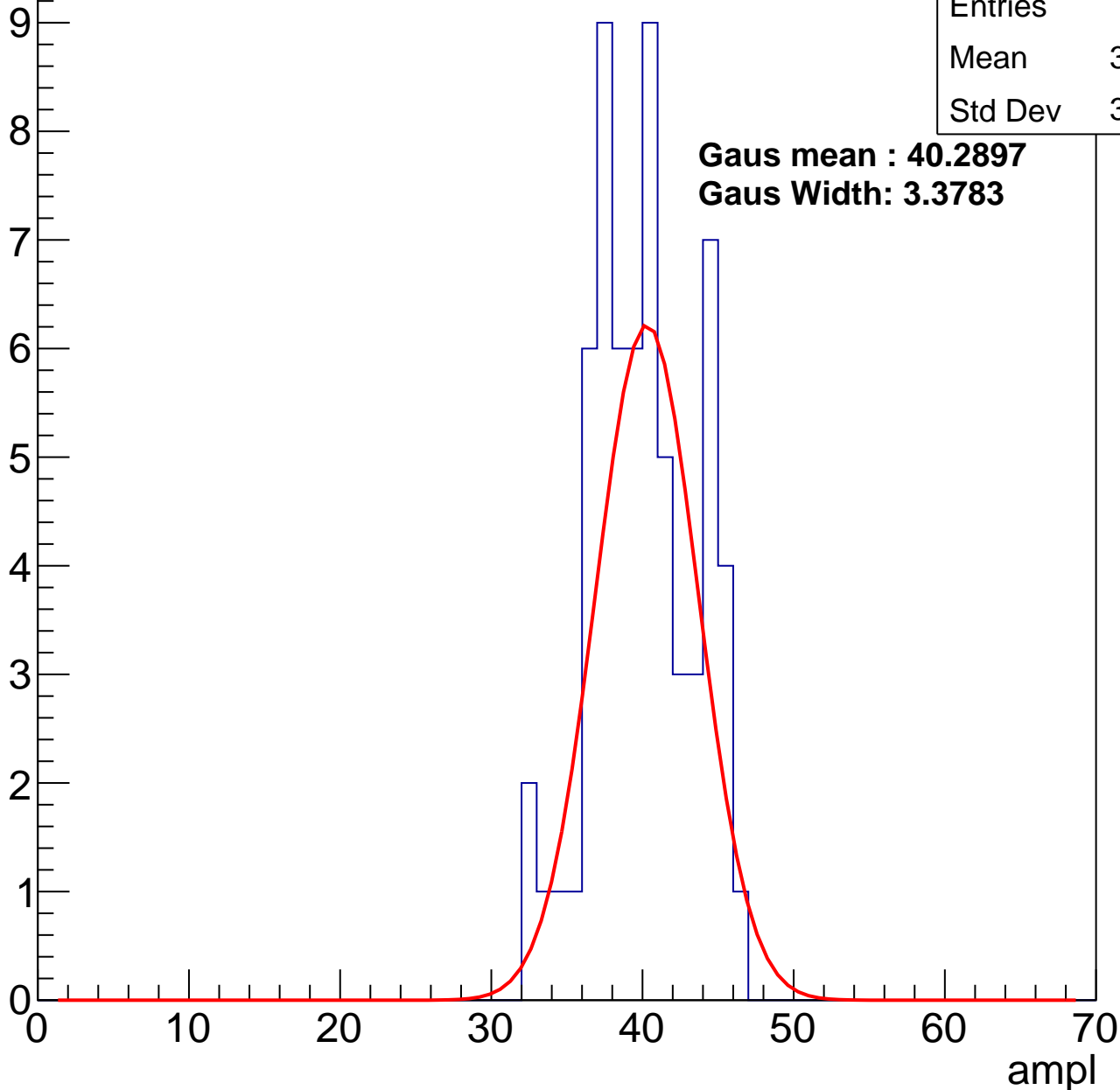
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	39.55
Std Dev	3.363

**Gaus mean : 40.2897**

**Gaus Width: 3.3783**

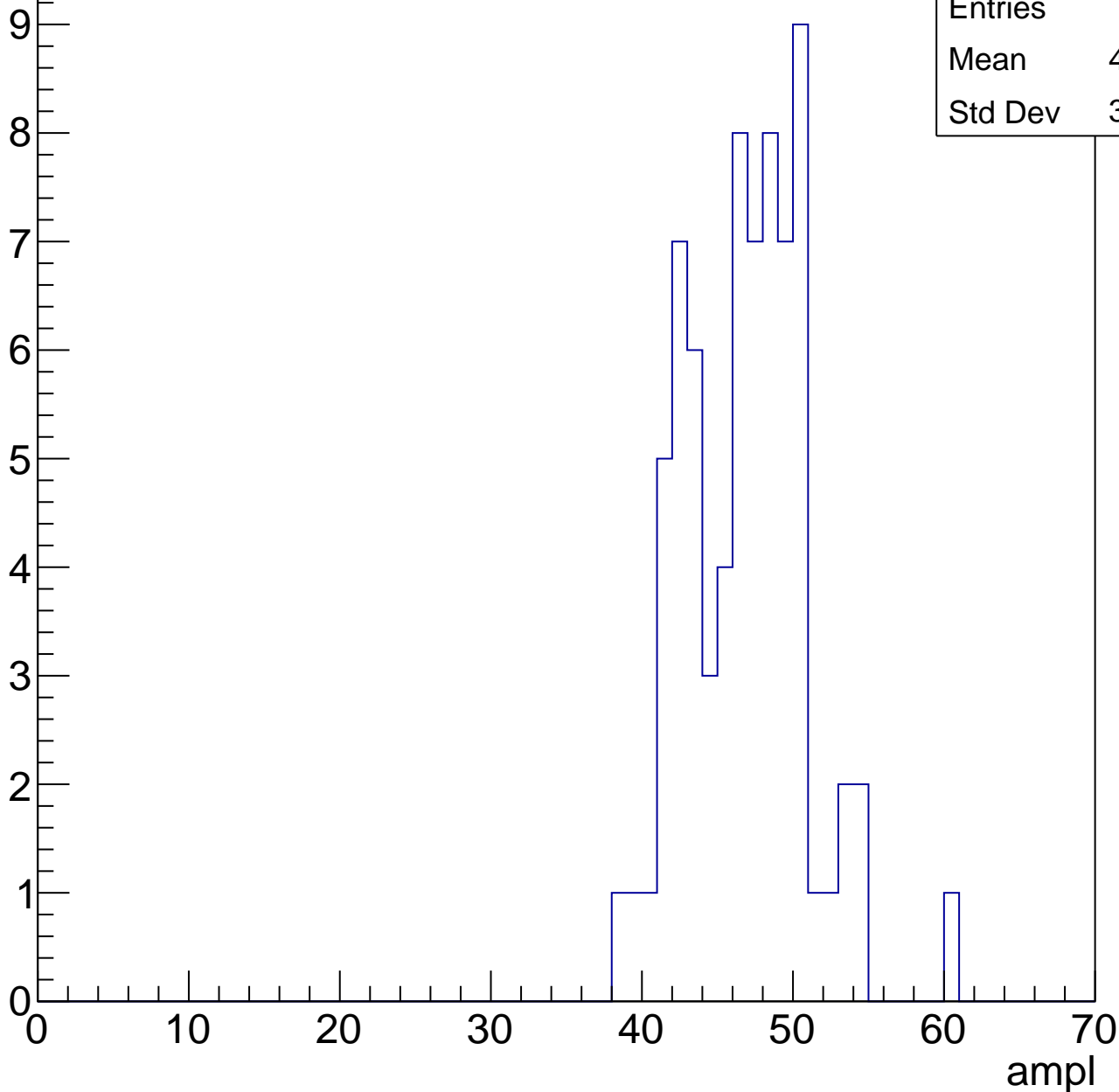


# B1L102S, U3-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	46.45
Std Dev	3.977

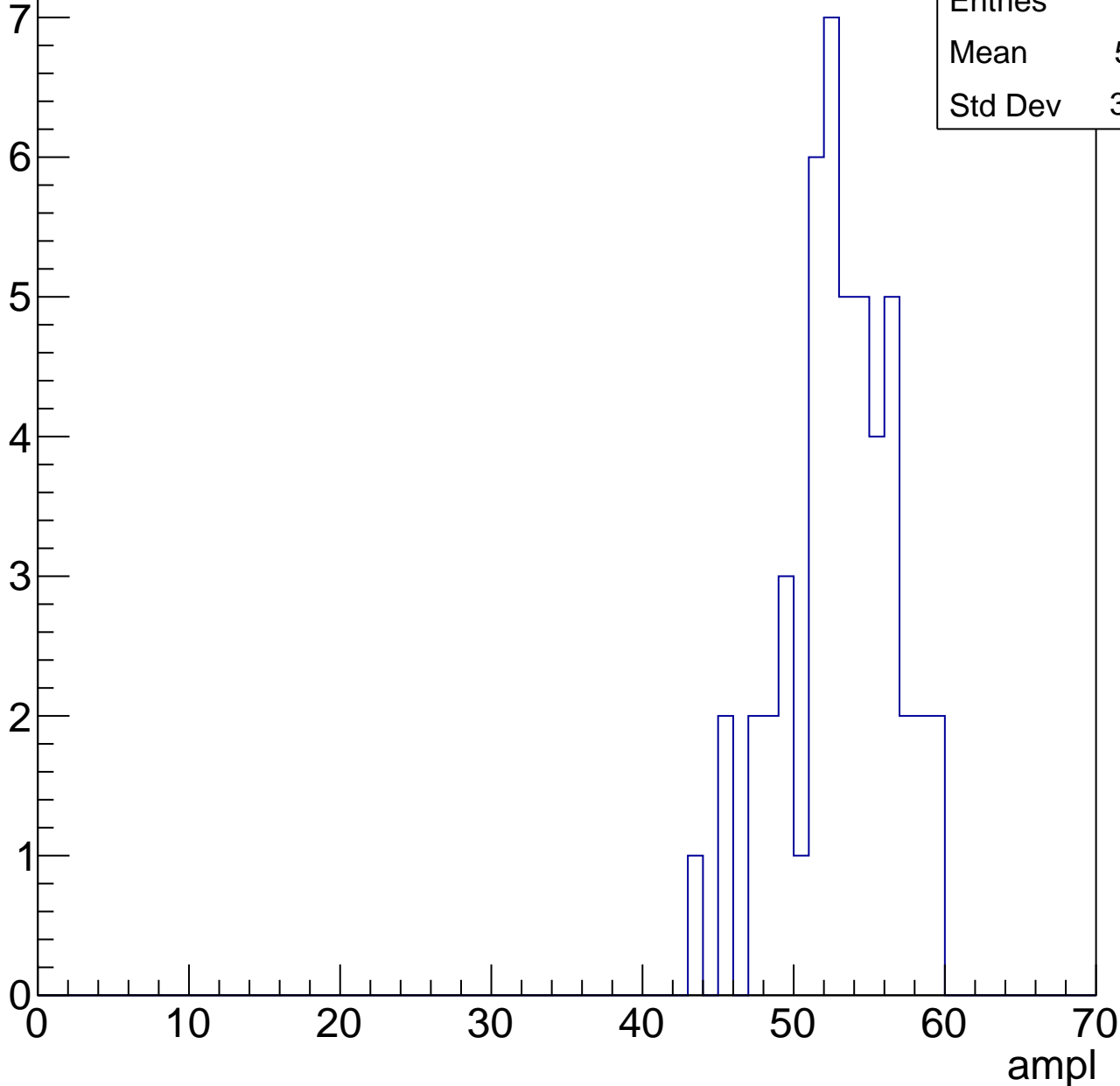


# B1L102S, U3-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	52.51
Std Dev	3.632

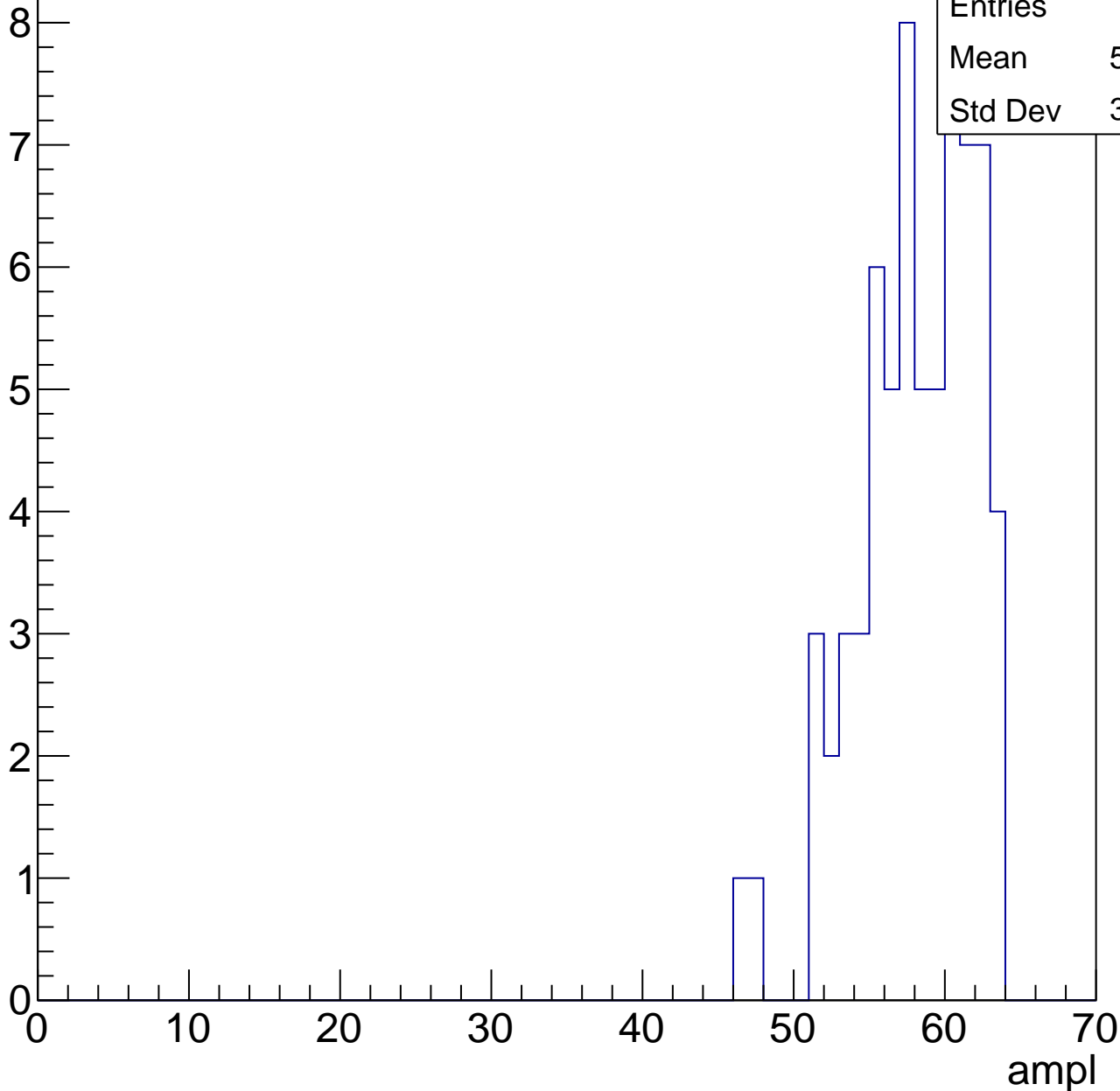


# B1L102S, U3-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	57.57
Std Dev	3.813

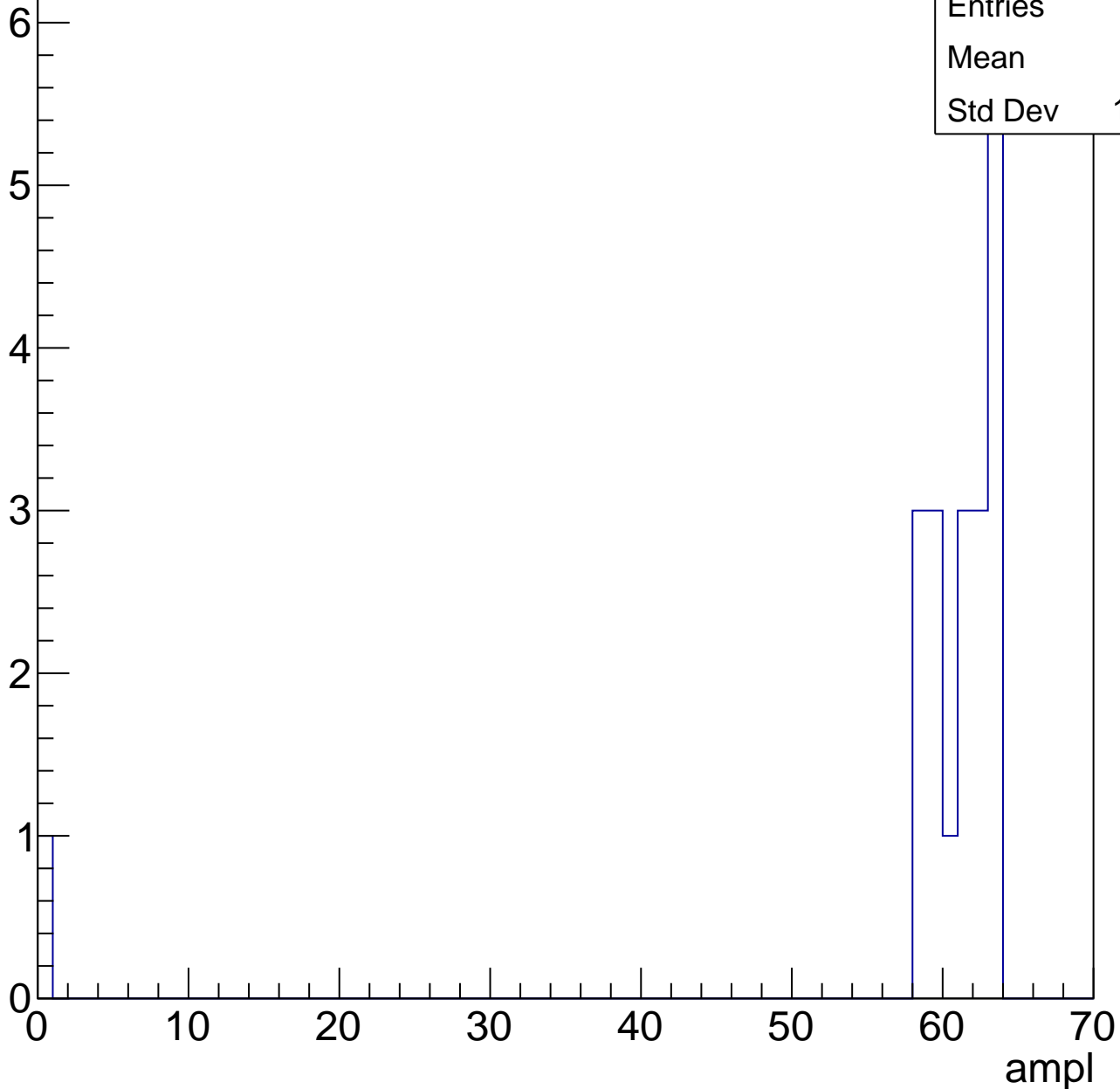


# B1L102S, U3-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	20
Mean	57.9
Std Dev	13.41





# B1L102S, U3-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

0

10

20

30

40

50

60

70

ampl

Entries	1
Mean	19
Std Dev	0

# B1L102S, U3-ch97, adc0

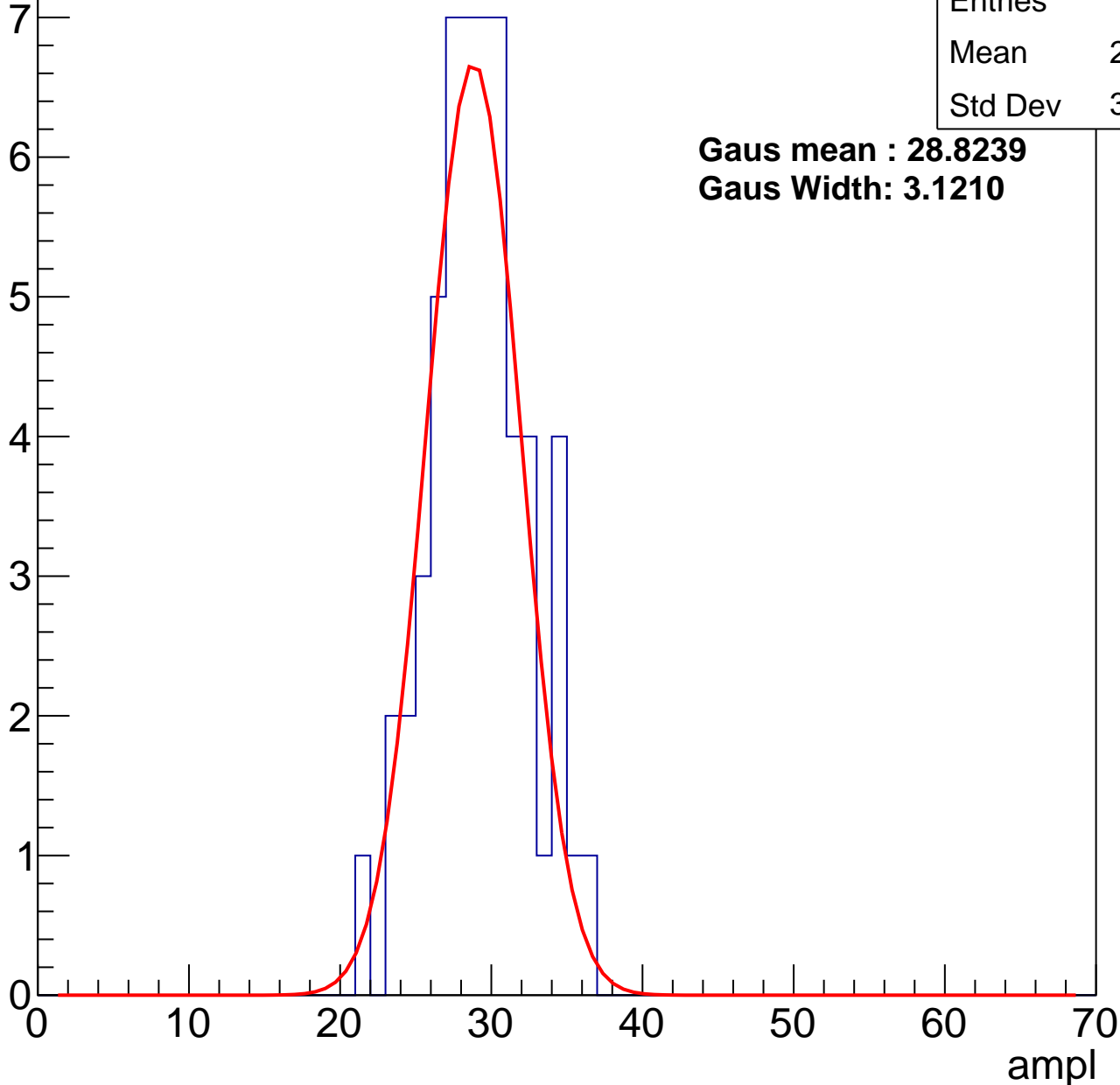
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	28.75
Std Dev	3.192

**Gaus mean : 28.8239**

**Gaus Width: 3.1210**



# B1L102S, U3-ch97, adc1

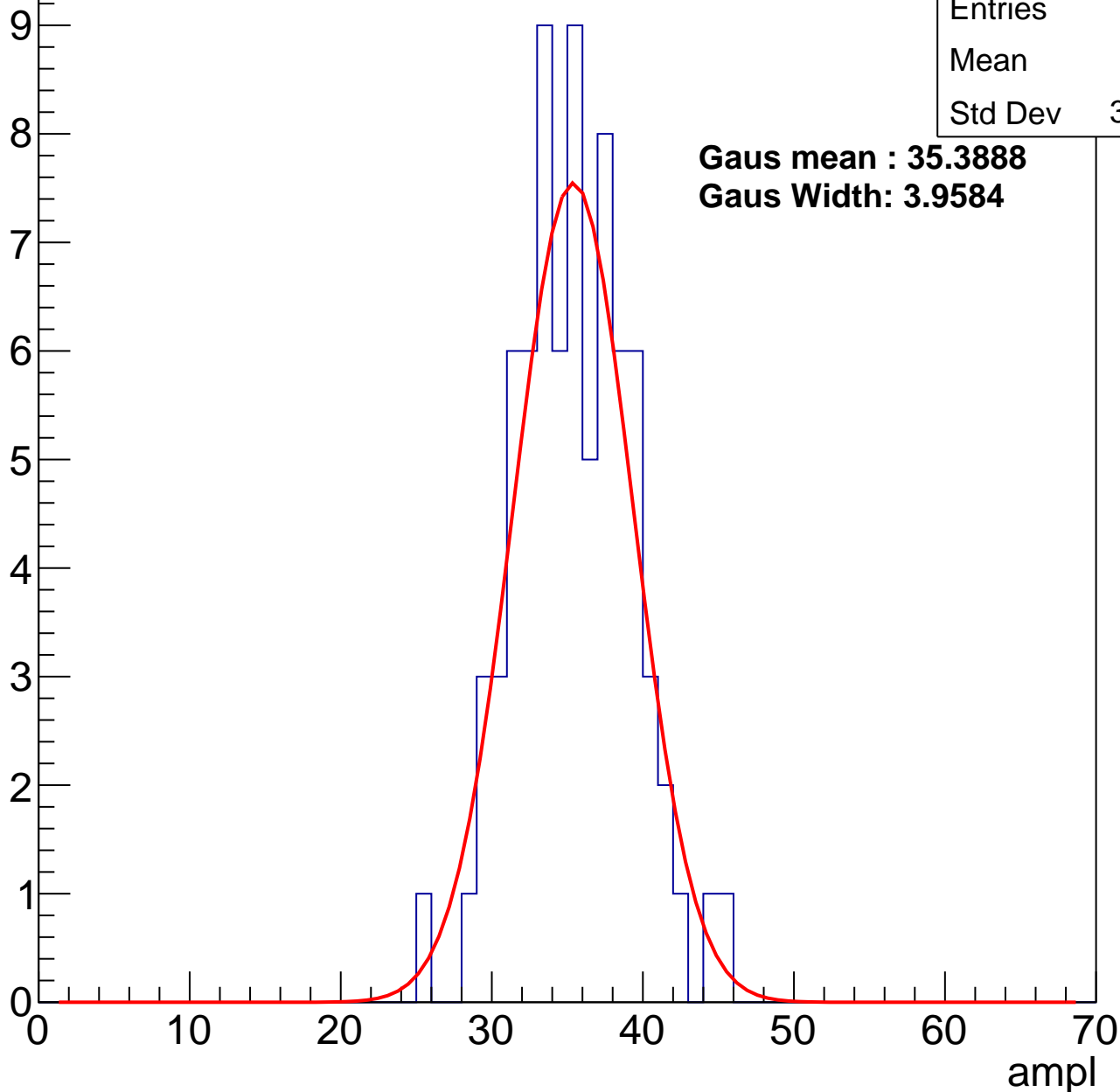
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	35
Std Dev	3.759

**Gaus mean : 35.3888**

**Gaus Width: 3.9584**



# B1L102S, U3-ch97, adc2

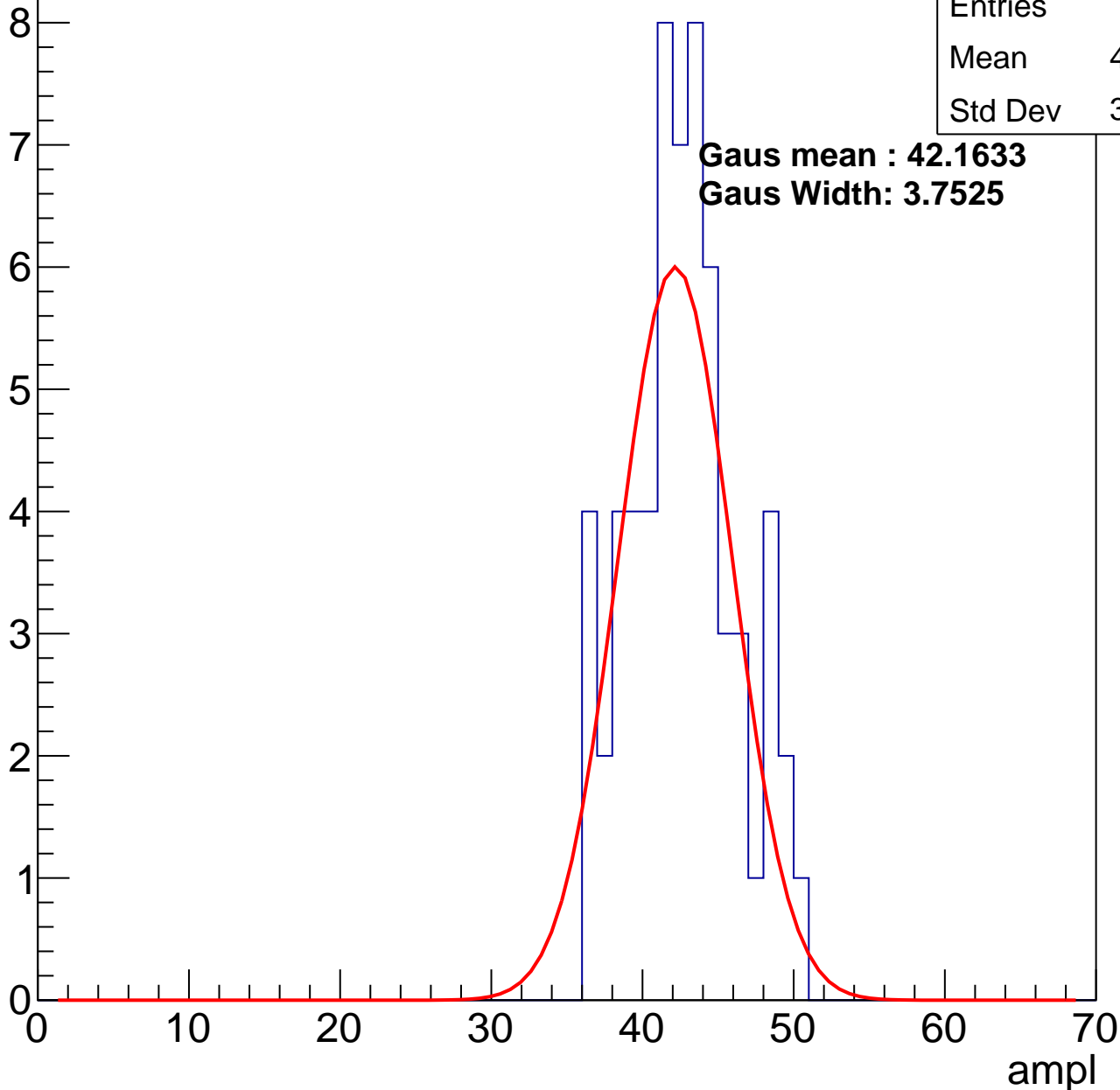
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	42.23
Std Dev	3.513

**Gaus mean : 42.1633**

**Gaus Width: 3.7525**

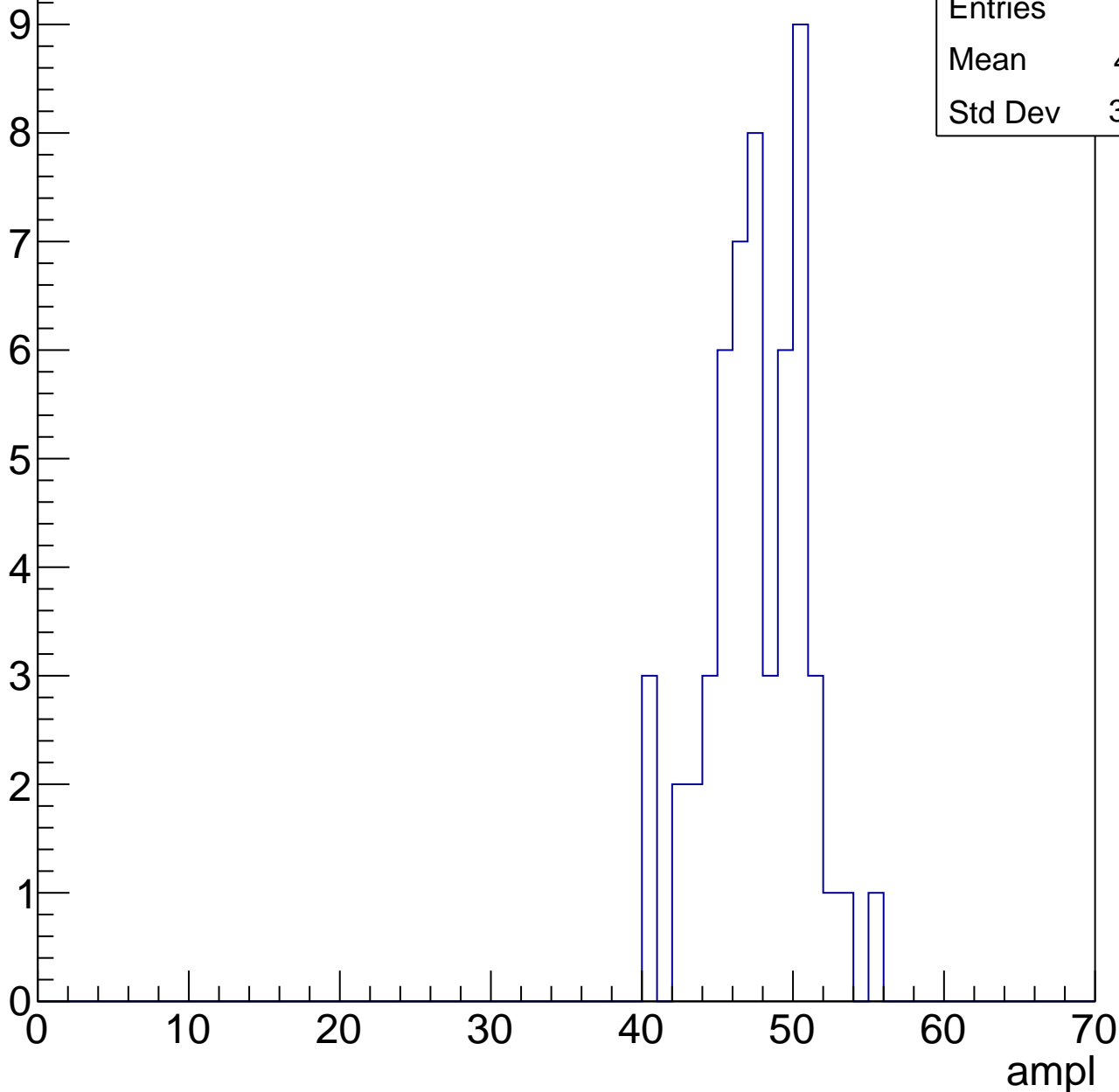


# B1L102S, U3-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	47.11
Std Dev	3.212

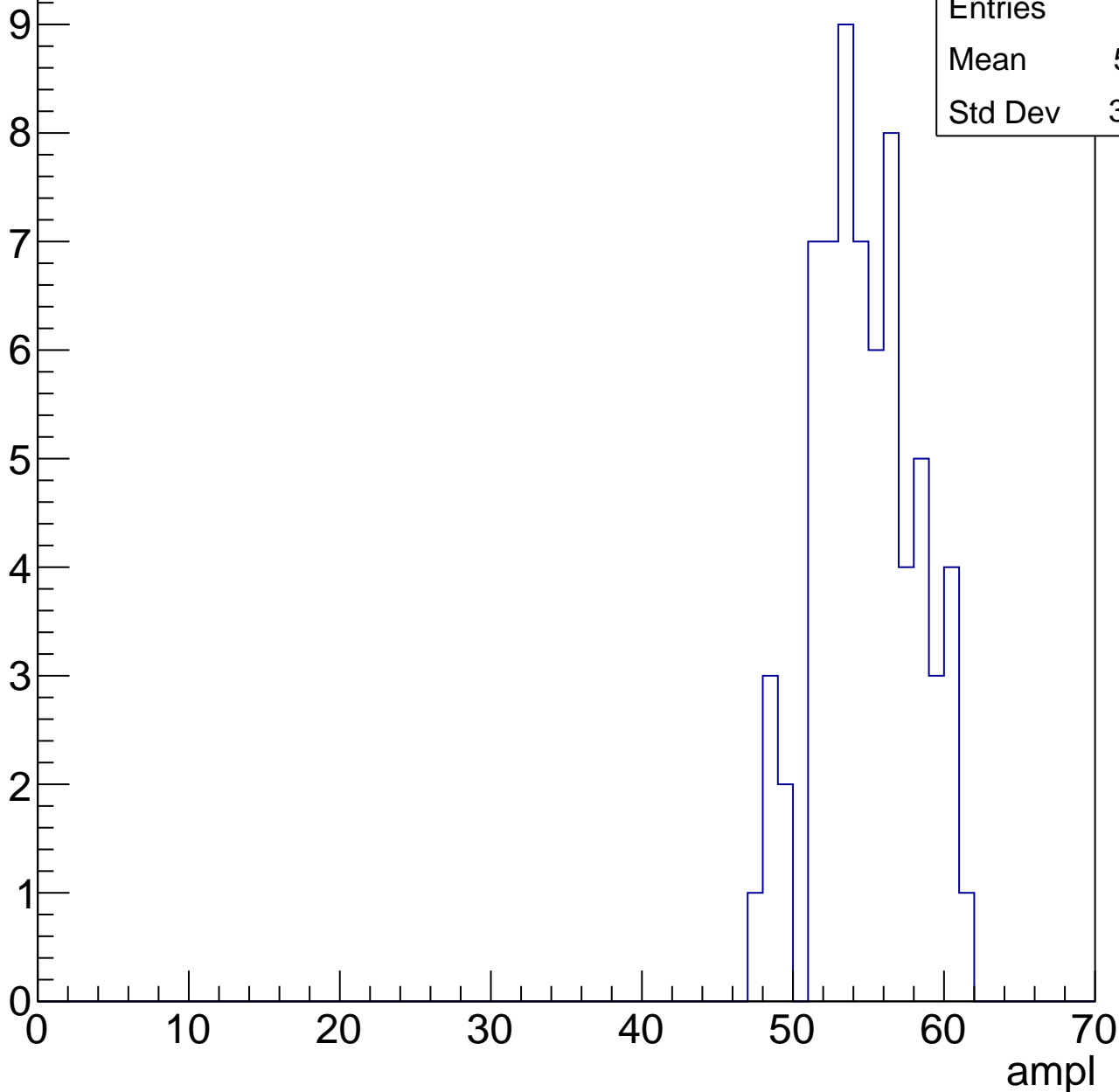


# B1L102S, U3-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	54.31
Std Dev	3.284

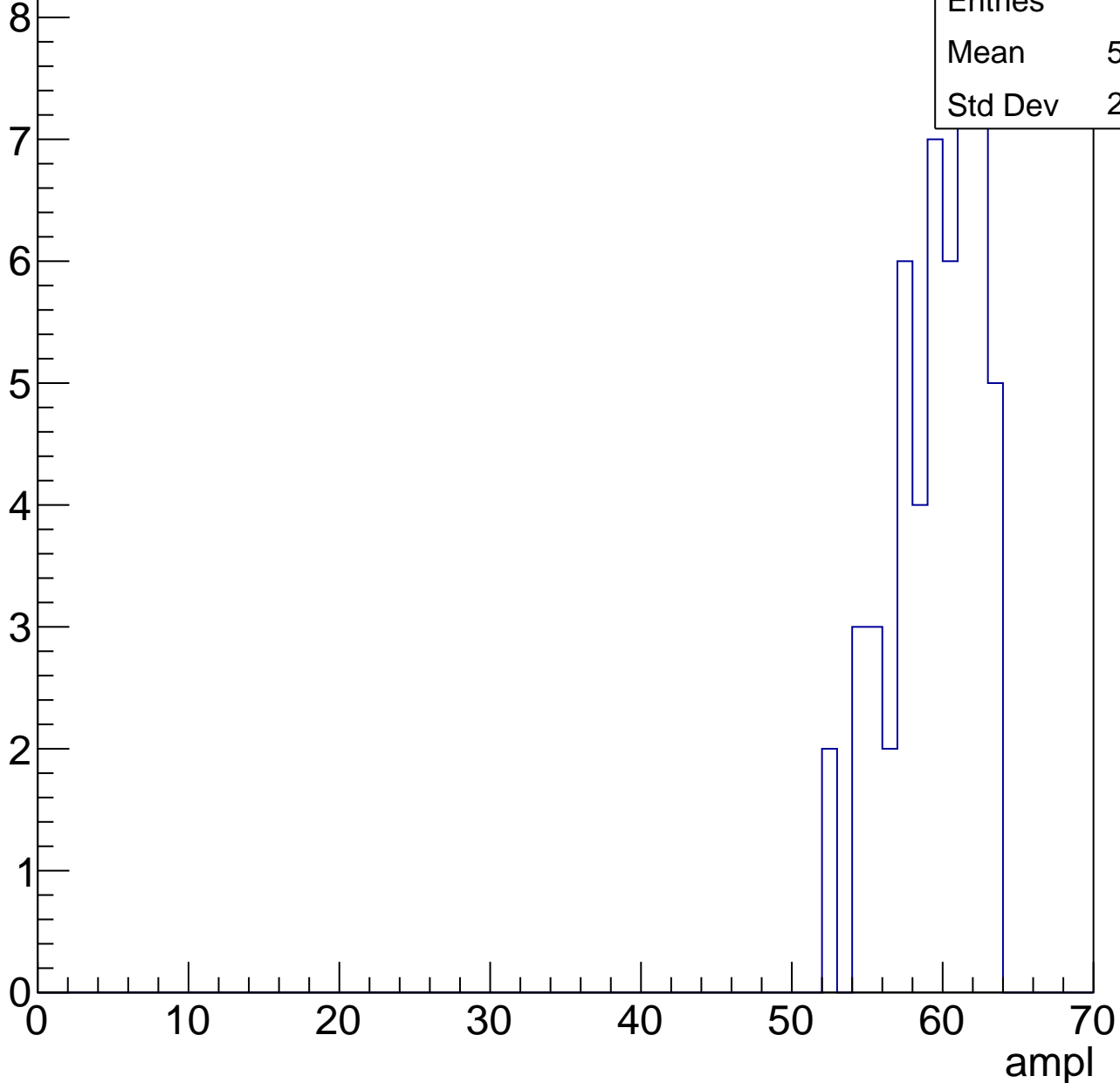


# B1L102S, U3-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	59.06
Std Dev	2.909



# B1L102S, U3-ch97, adc6

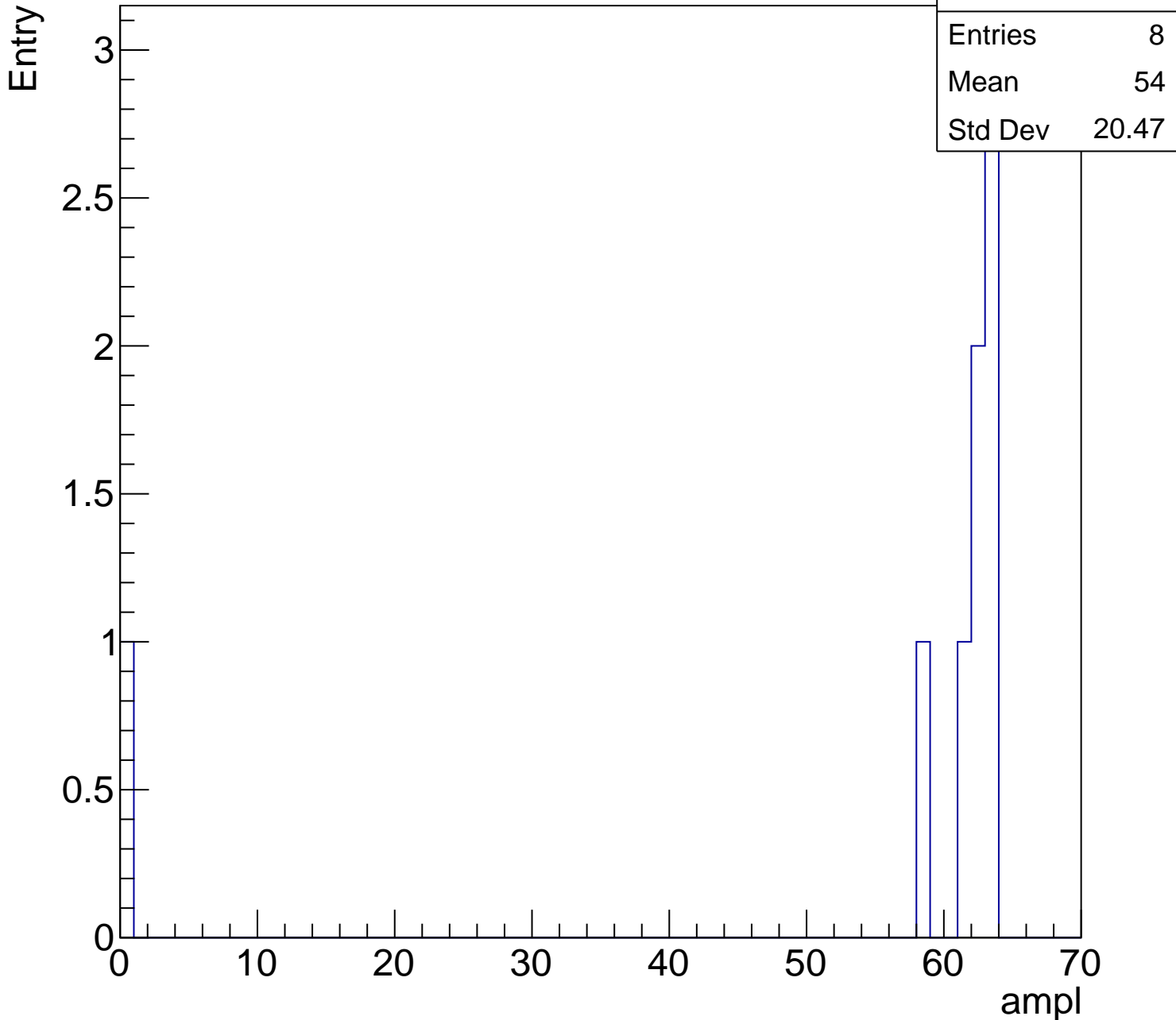
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	8
Mean	54
Std Dev	20.47

ampl





# B1L102S, U3-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch98, adc0

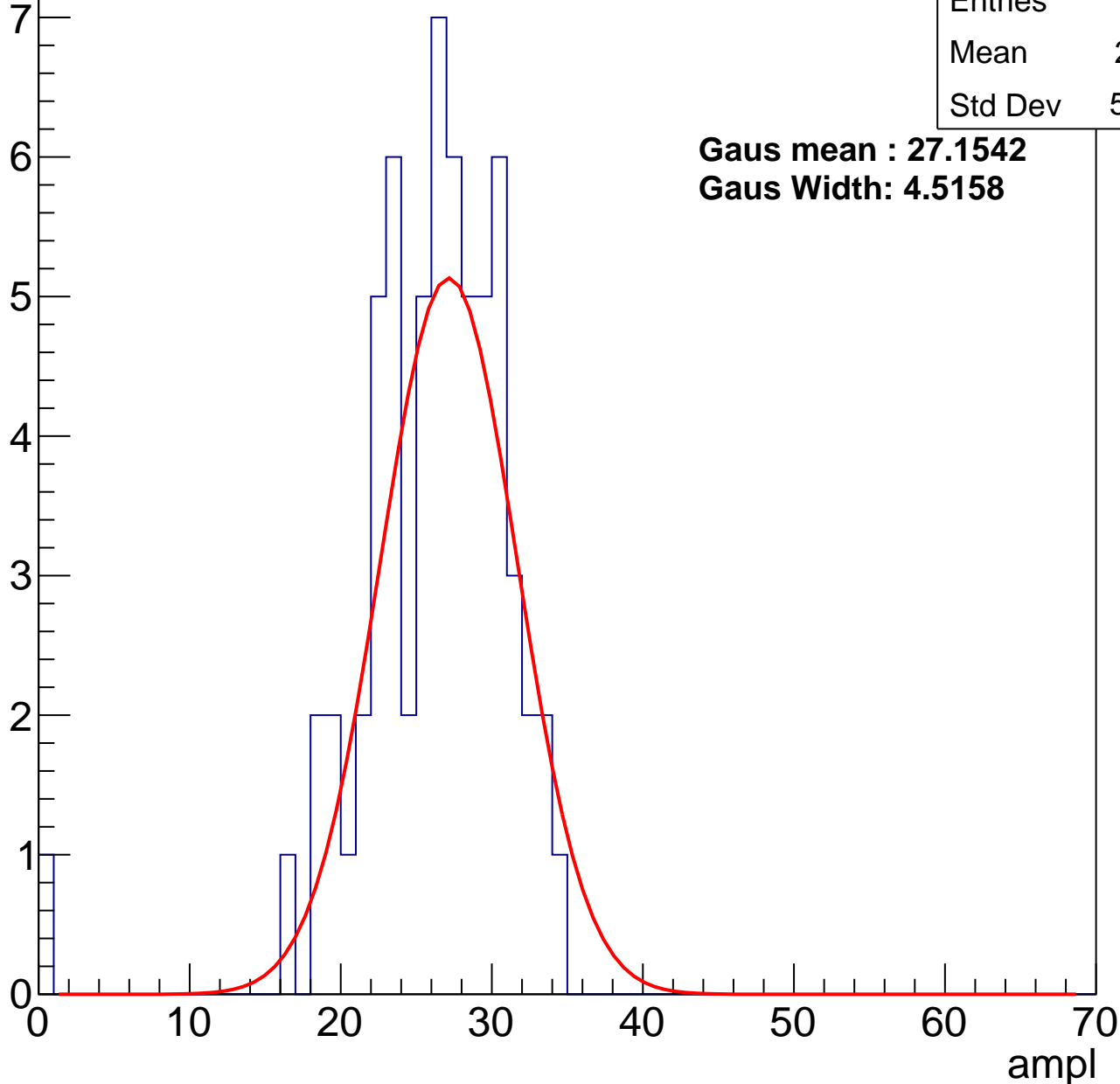
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	25.61
Std Dev	5.156

**Gaus mean : 27.1542**

**Gaus Width: 4.5158**



# B1L102S, U3-ch98, adc1

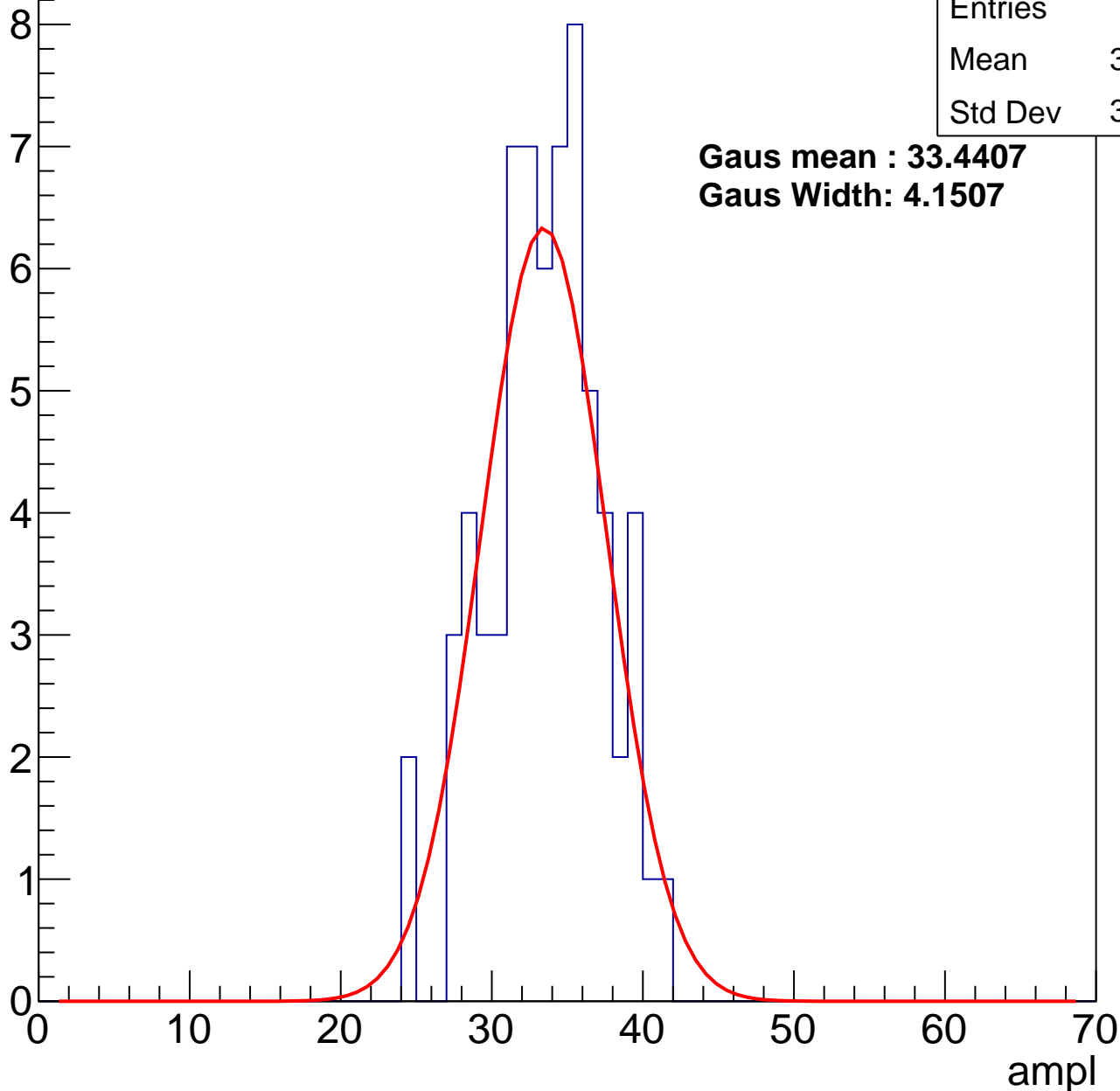
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	33.07
Std Dev	3.735

**Gaus mean : 33.4407**

**Gaus Width: 4.1507**



# B1L102S, U3-ch98, adc2

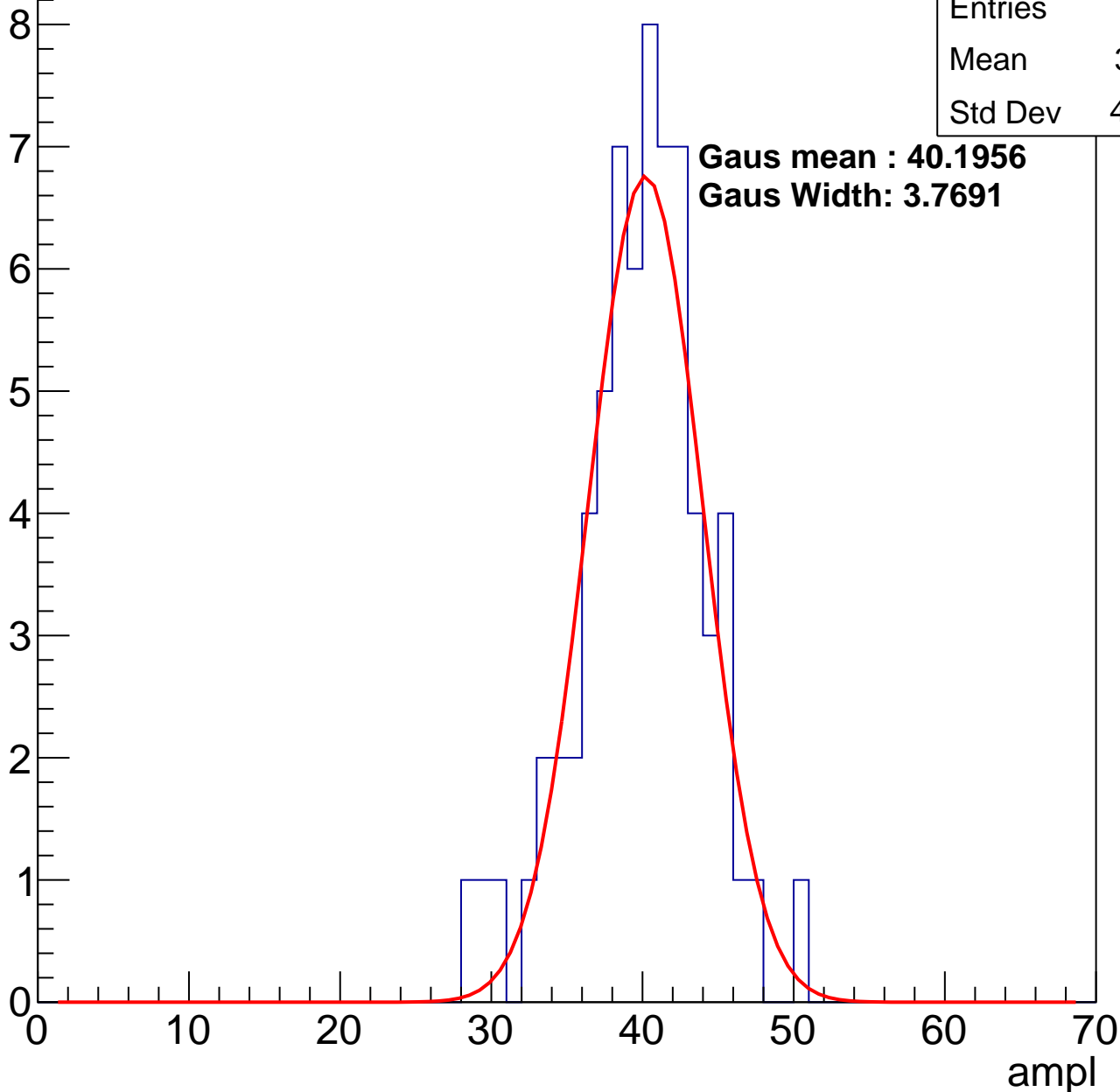
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	39.41
Std Dev	4.152

**Gaus mean : 40.1956**

**Gaus Width: 3.7691**

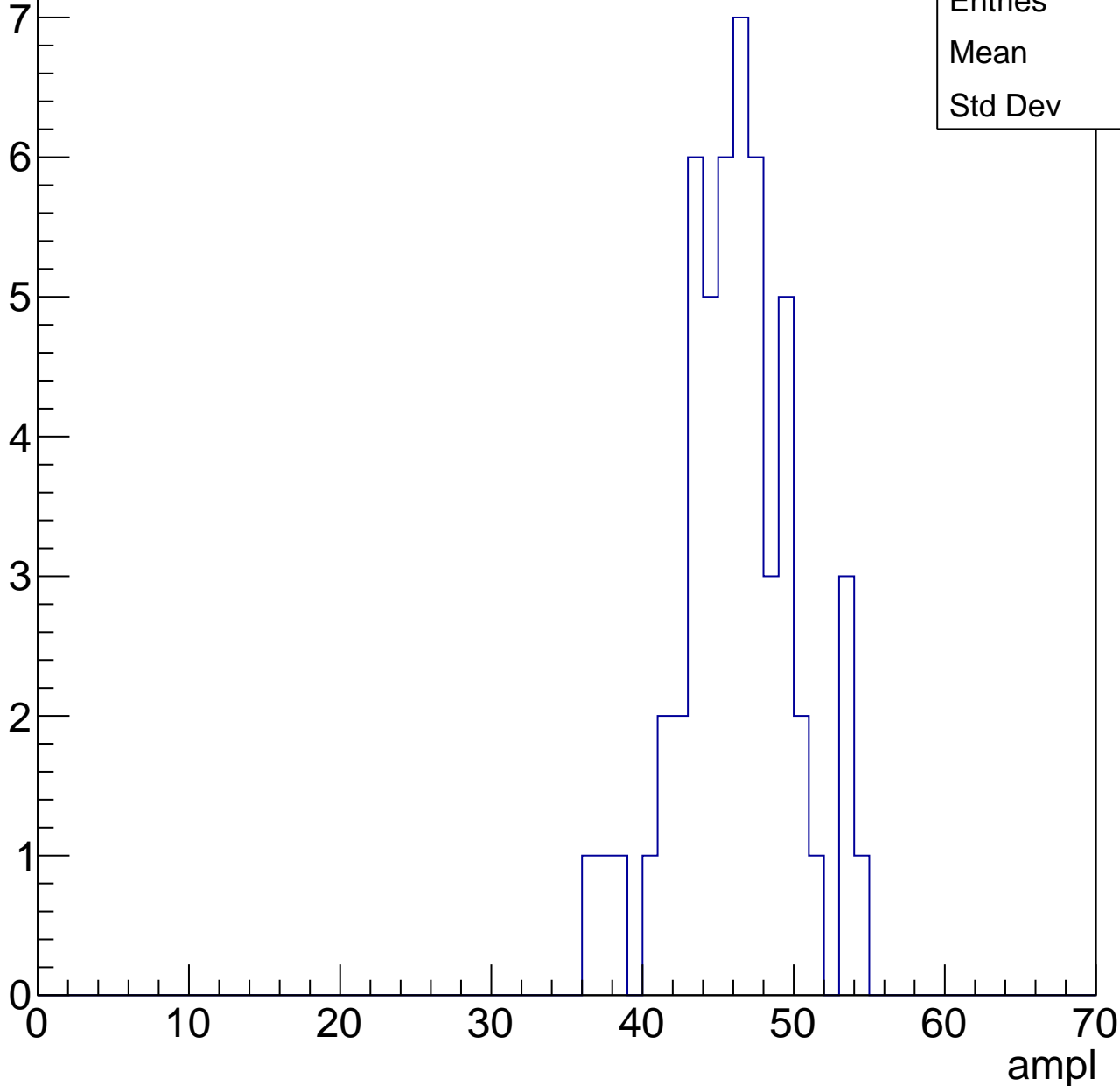


# B1L102S, U3-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	45.7
Std Dev	3.81

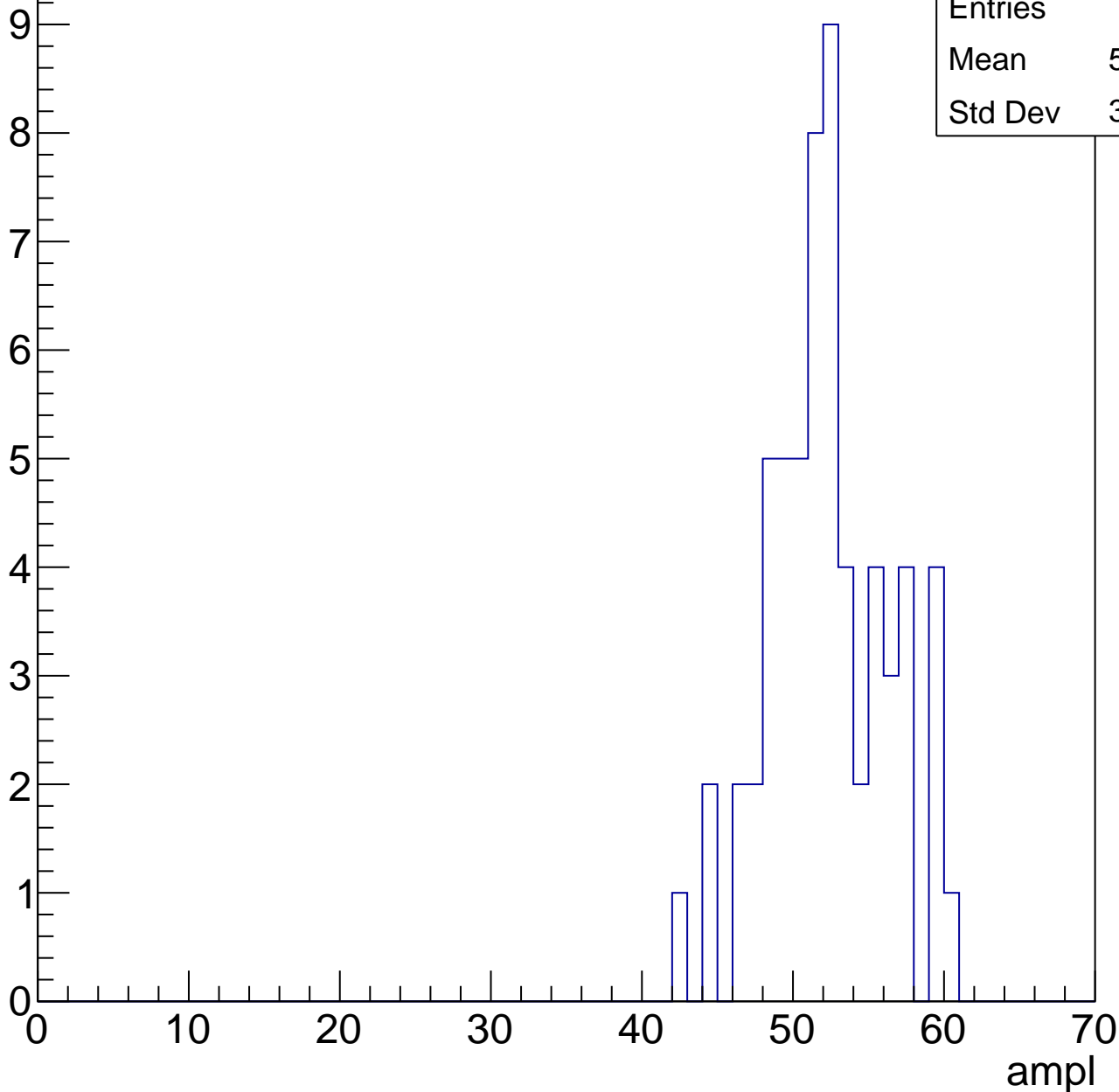


# B1L102S, U3-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	51.79
Std Dev	3.959

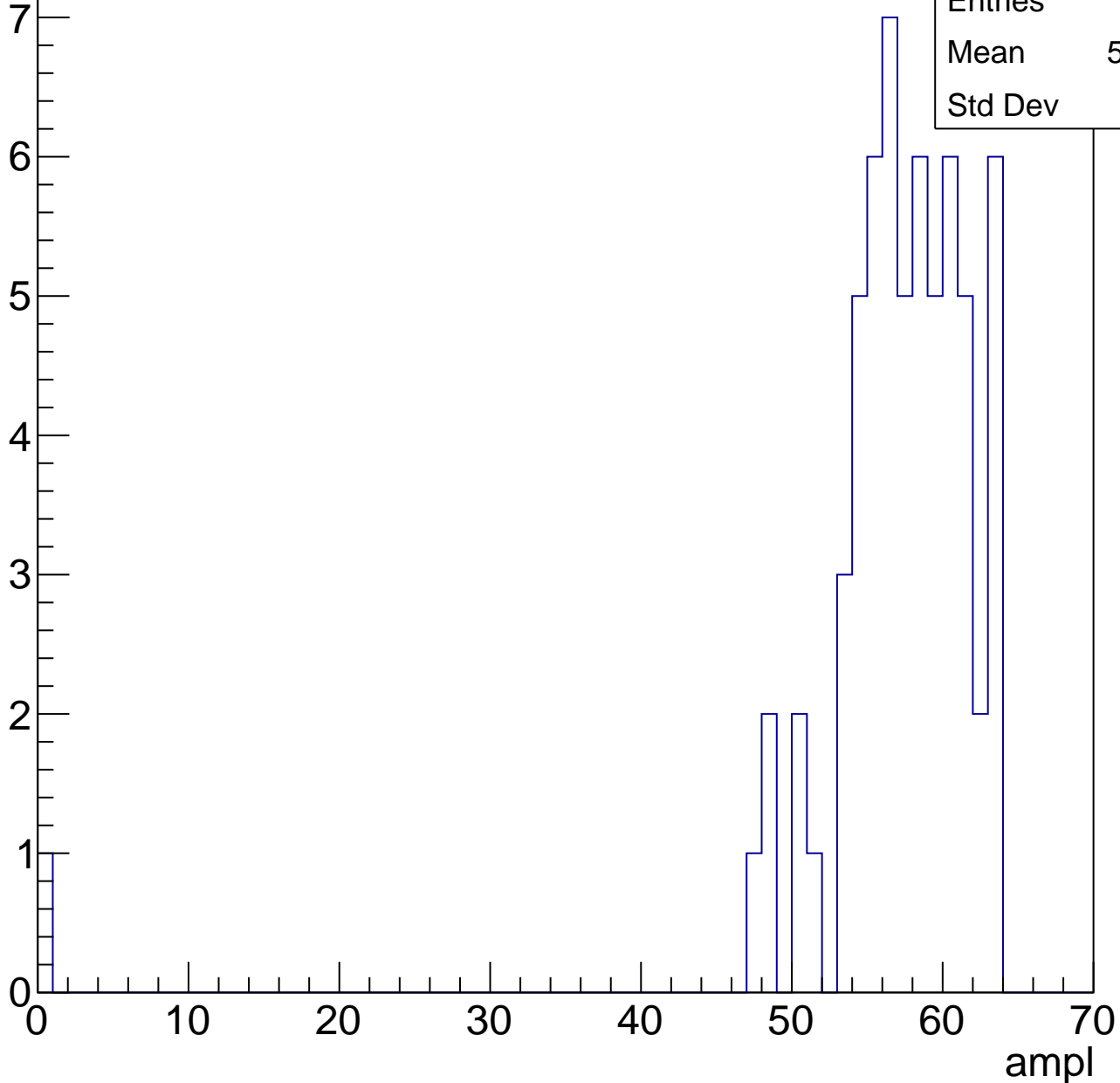


# B1L102S, U3-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	56.19
Std Dev	8.12

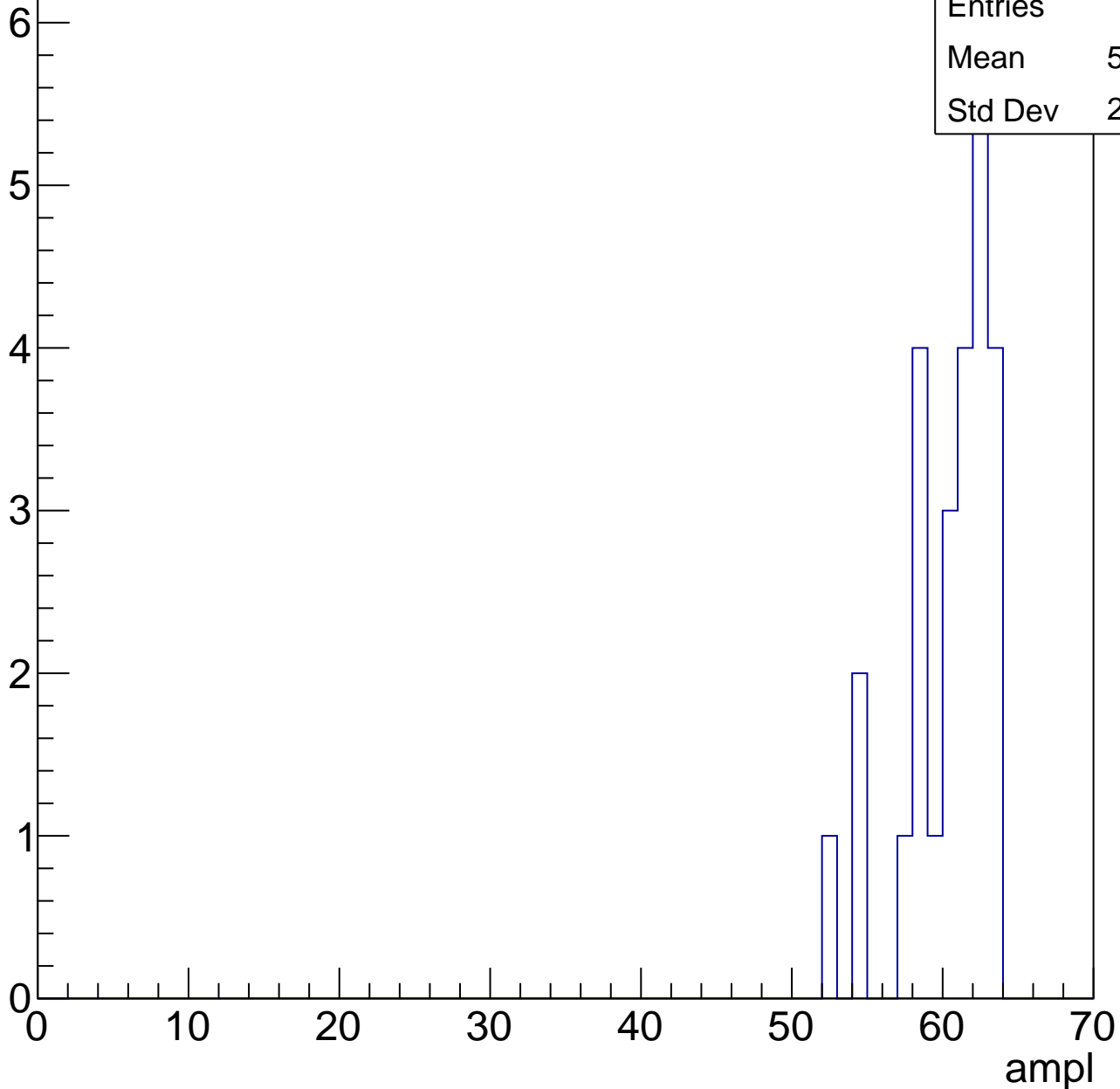


# B1L102S, U3-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	26
Mean	59.85
Std Dev	2.944

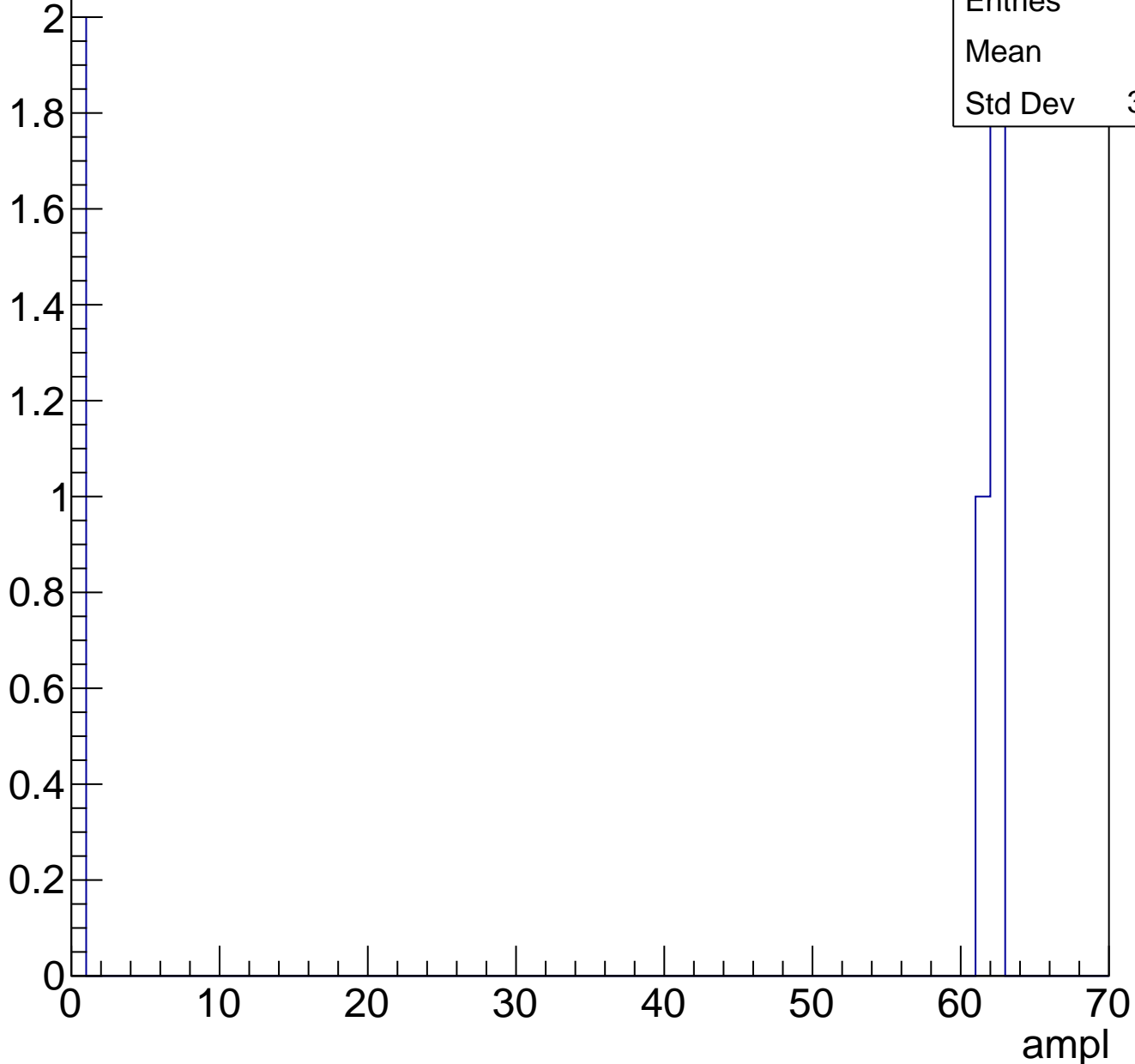




# B1L102S, U3-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch99, adc0

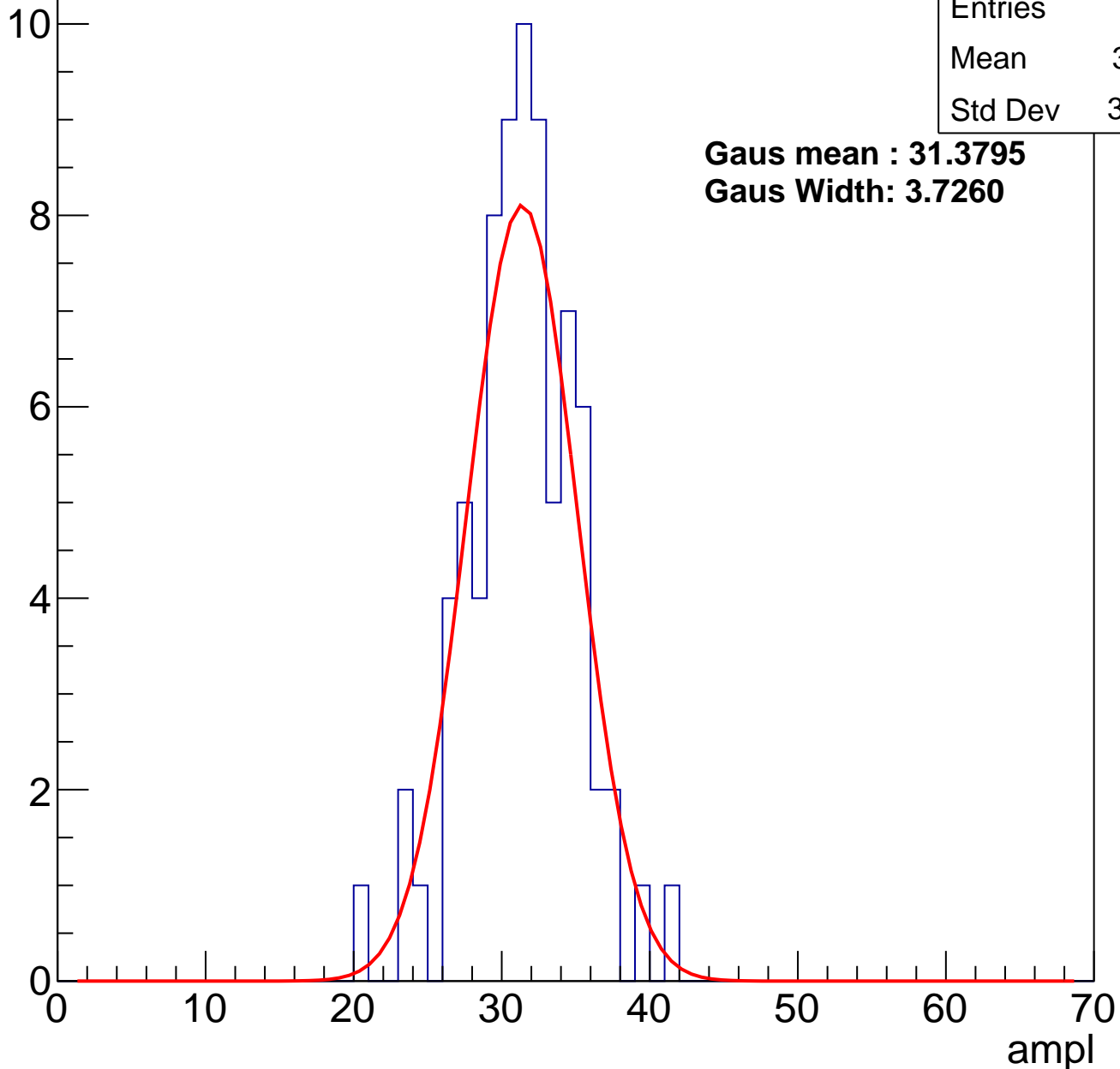
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	77
Mean	30.91
Std Dev	3.655

**Gaus mean : 31.3795**

**Gaus Width: 3.7260**

Entry



# B1L102S, U3-ch99, adc1

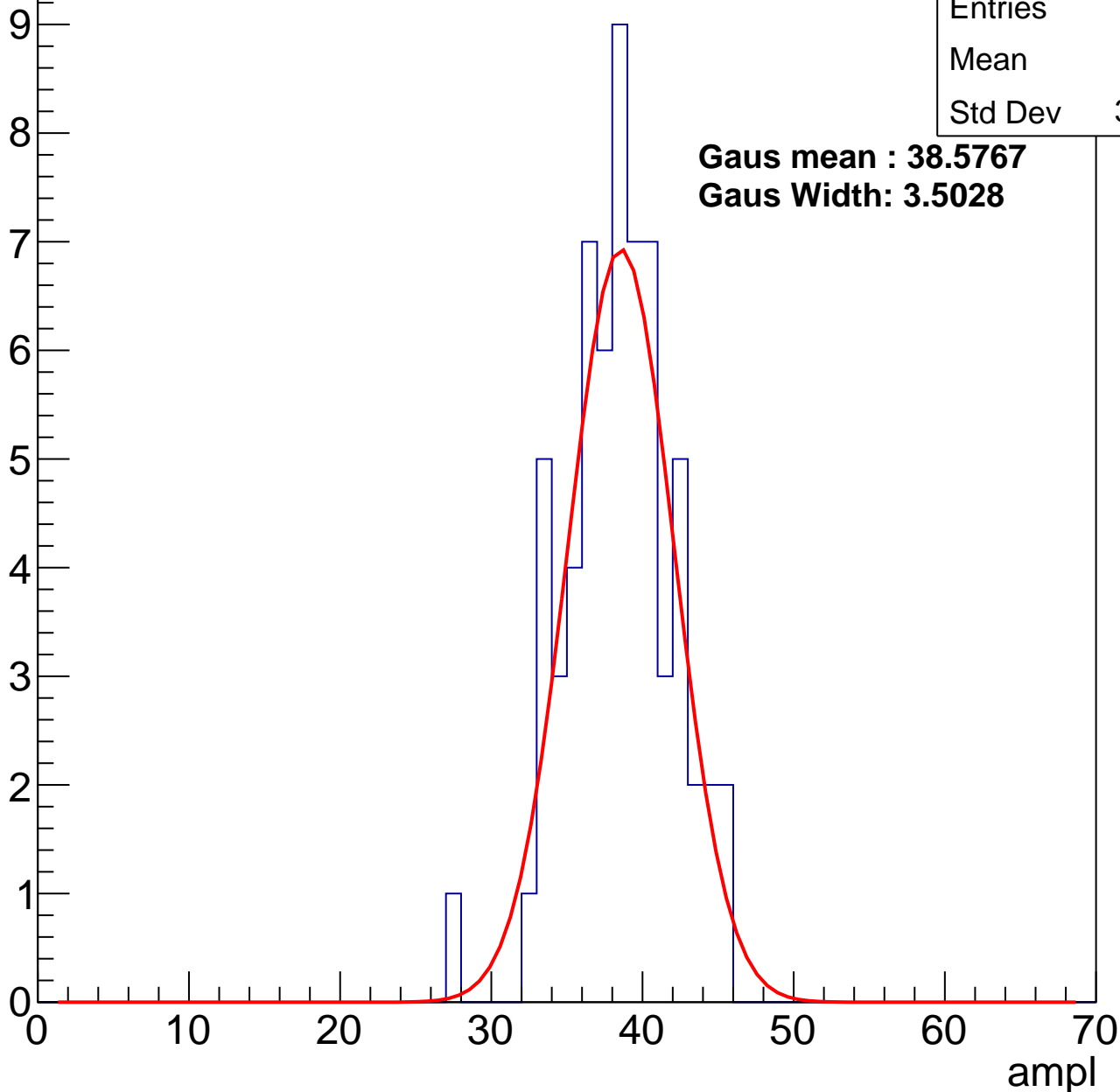
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	38
Std Dev	3.451

**Gaus mean : 38.5767**

**Gaus Width: 3.5028**



# B1L102S, U3-ch99, adc2

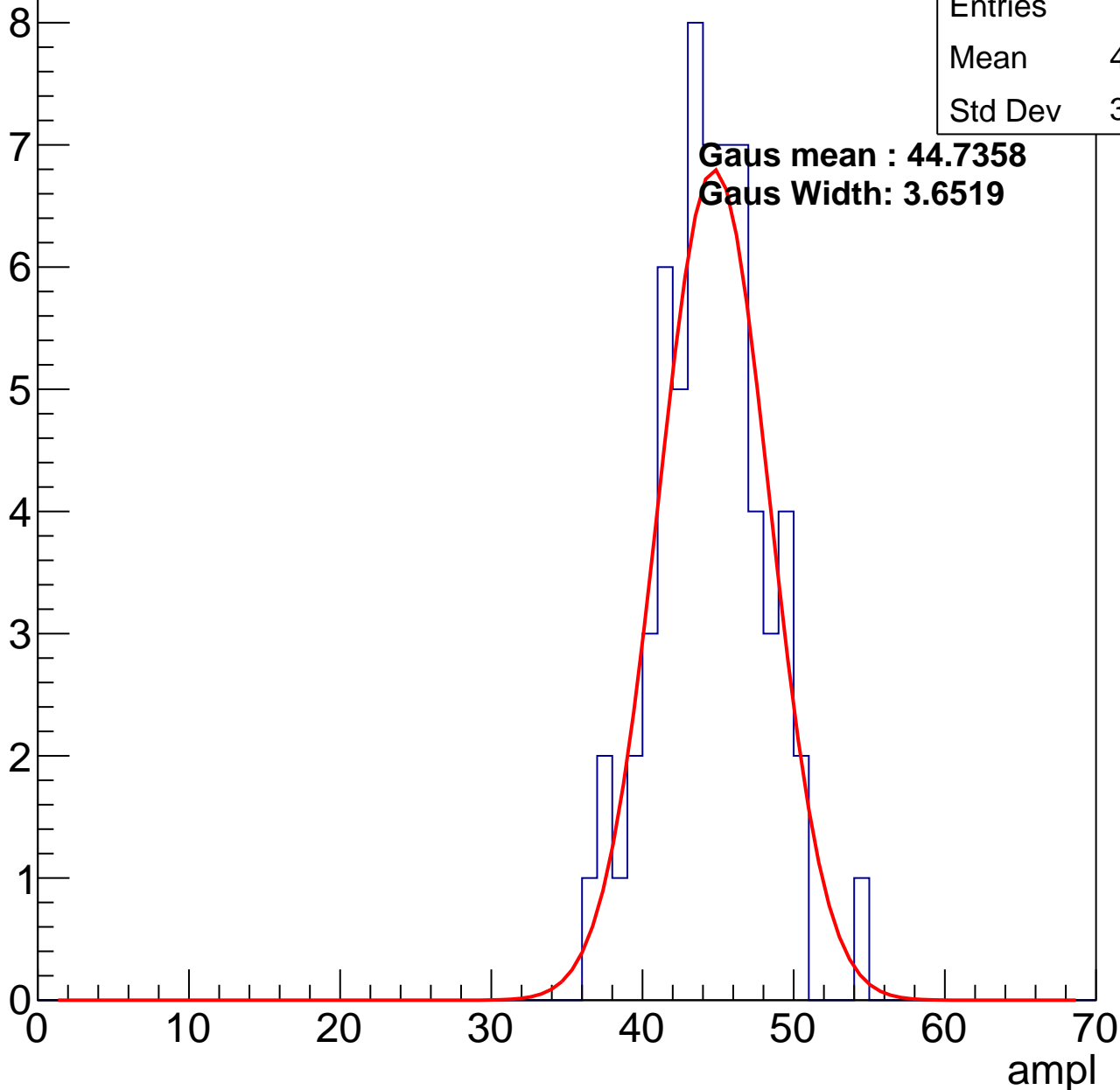
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	44.02
Std Dev	3.494

**Gaus mean : 44.7358**

**Gaus Width: 3.6519**

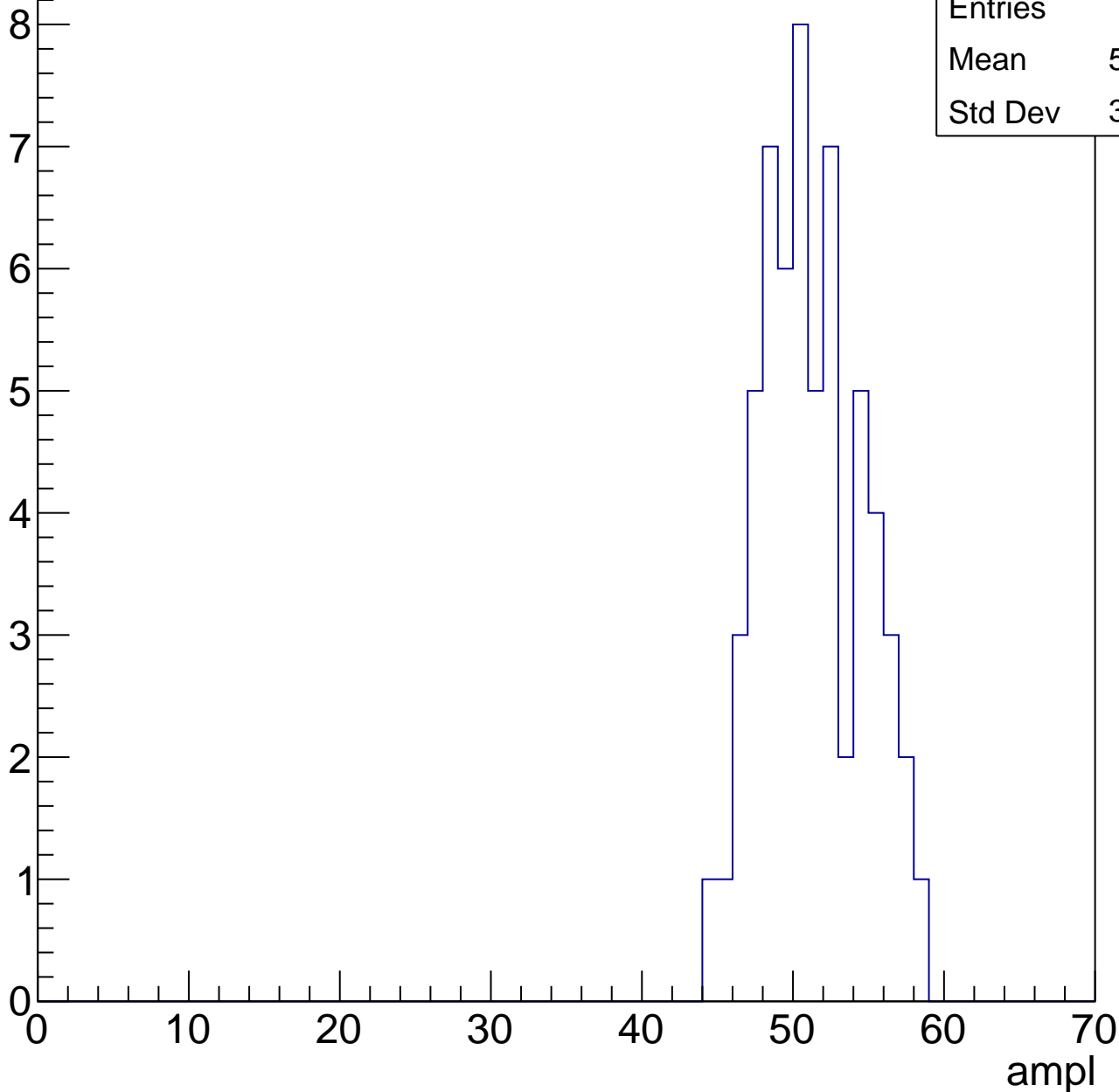


# B1L102S, U3-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	50.78
Std Dev	3.297

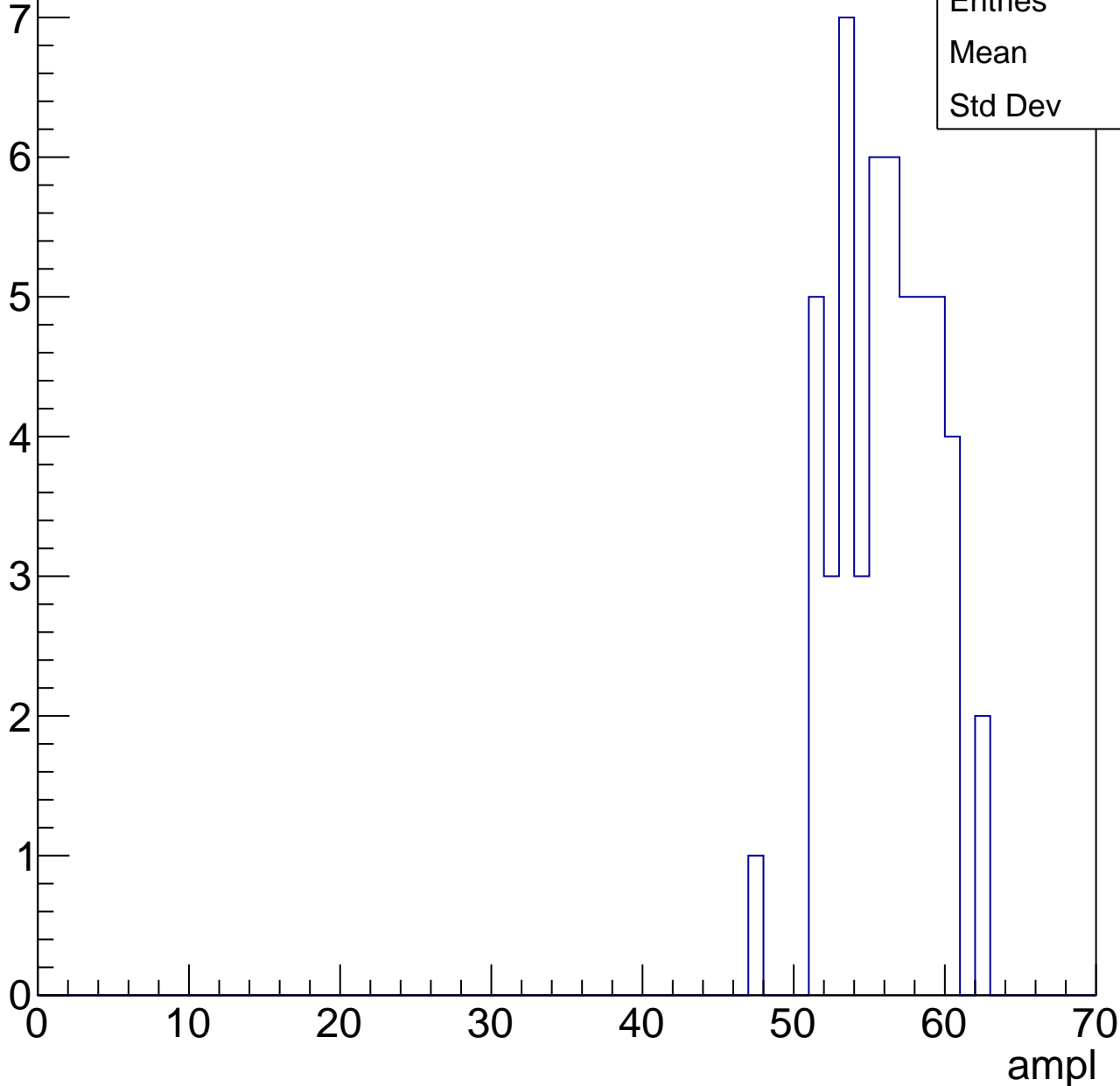


# B1L102S, U3-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	55.6
Std Dev	3.2

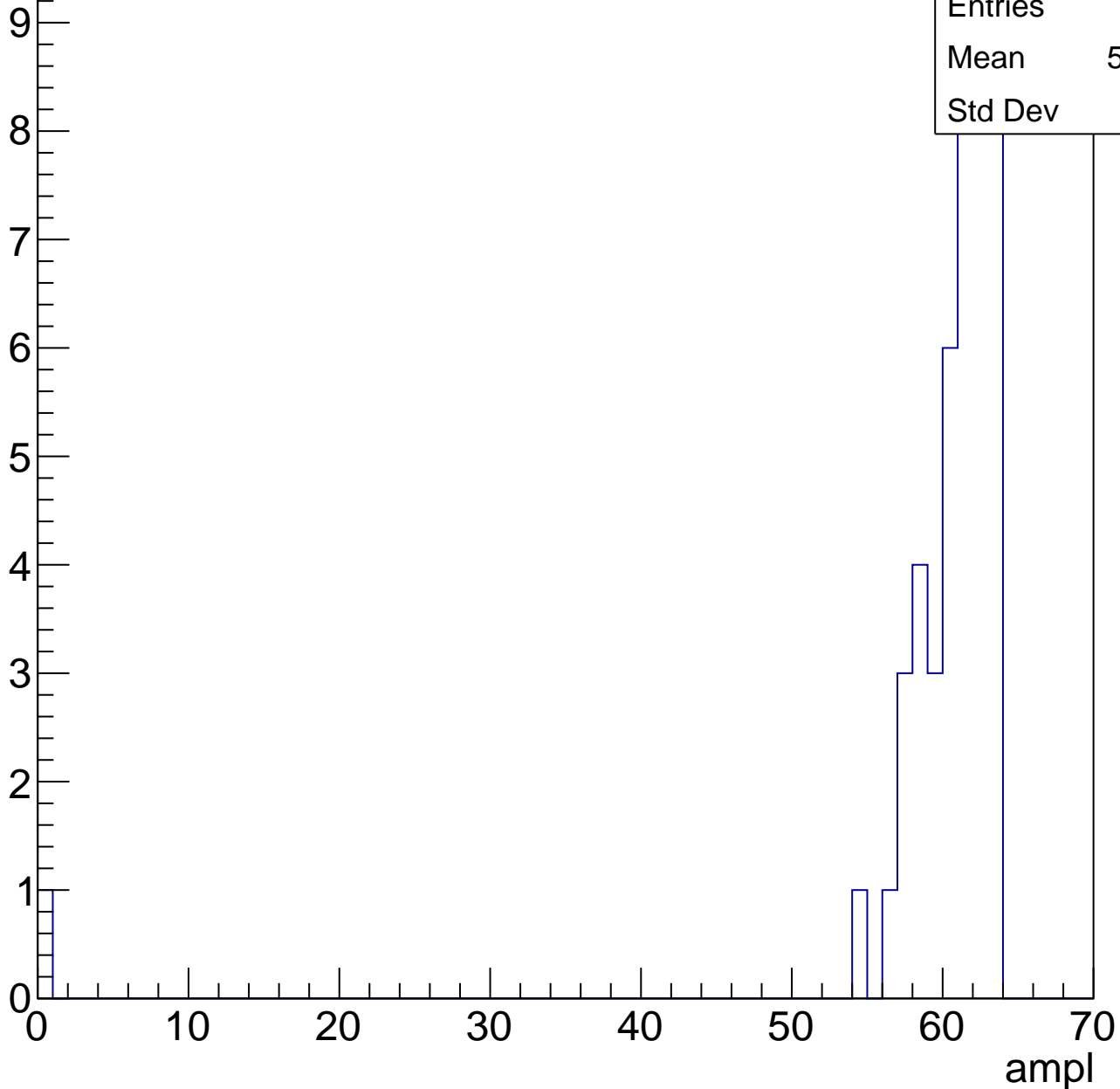


# B1L102S, U3-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	44
Mean	59.07
Std Dev	9.26



# B1L102S, U3-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

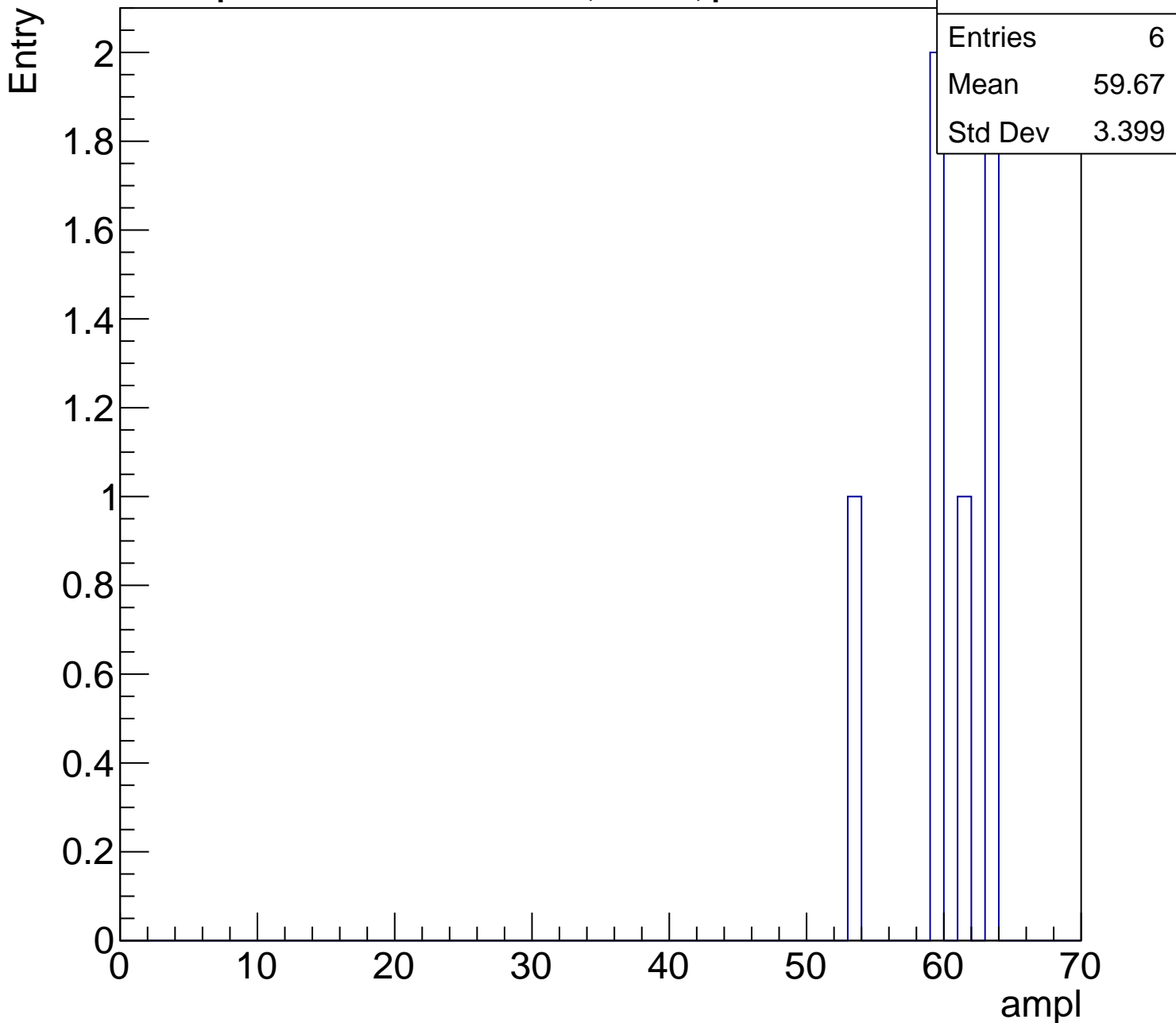
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	59.67
Std Dev	3.399

0 10 20 30 40 50 60 70

ampl





# B1L102S, U3-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch100, adc0

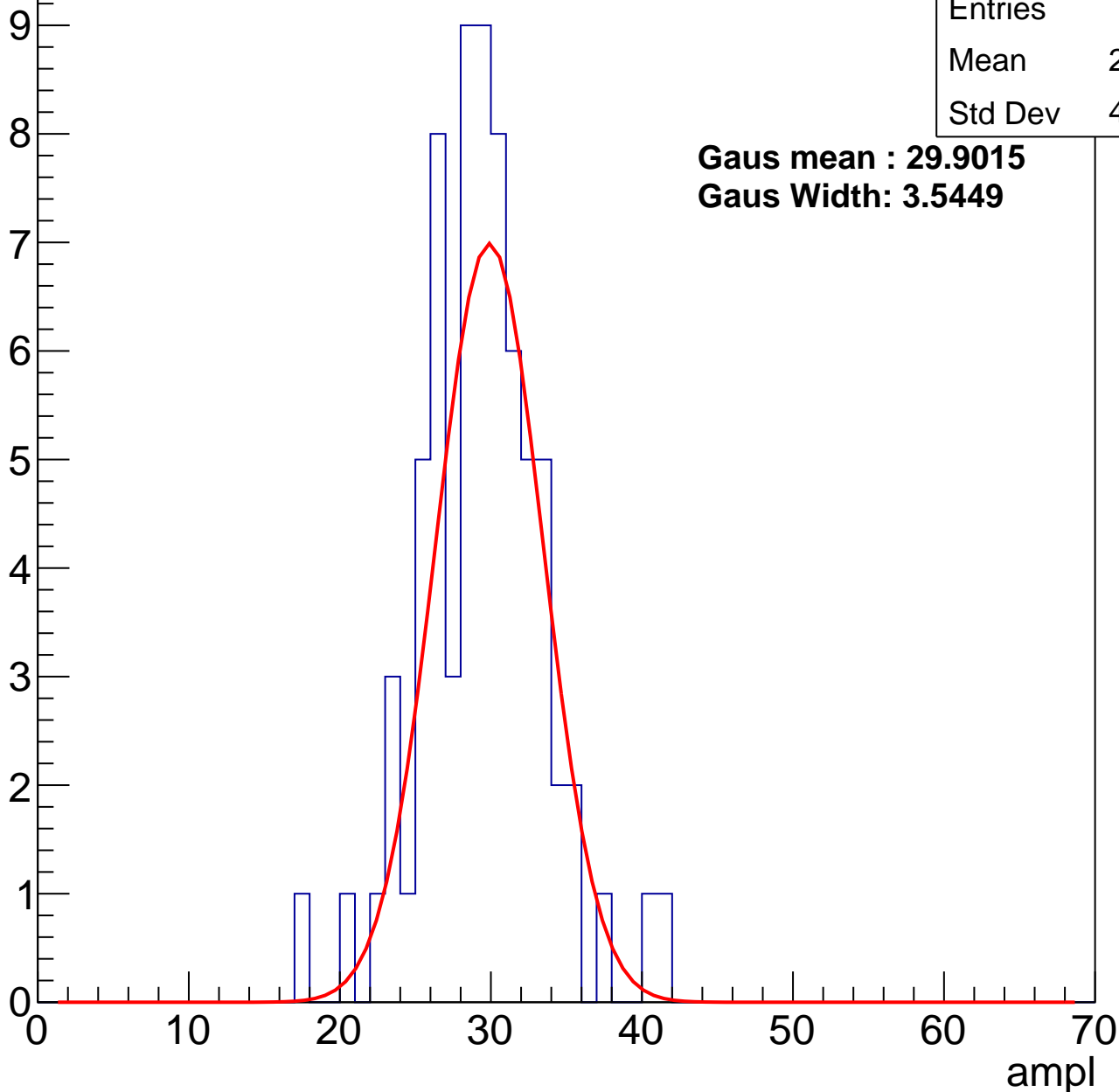
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	28.97
Std Dev	4.062

**Gaus mean : 29.9015**

**Gaus Width: 3.5449**



# B1L102S, U3-ch100, adc1

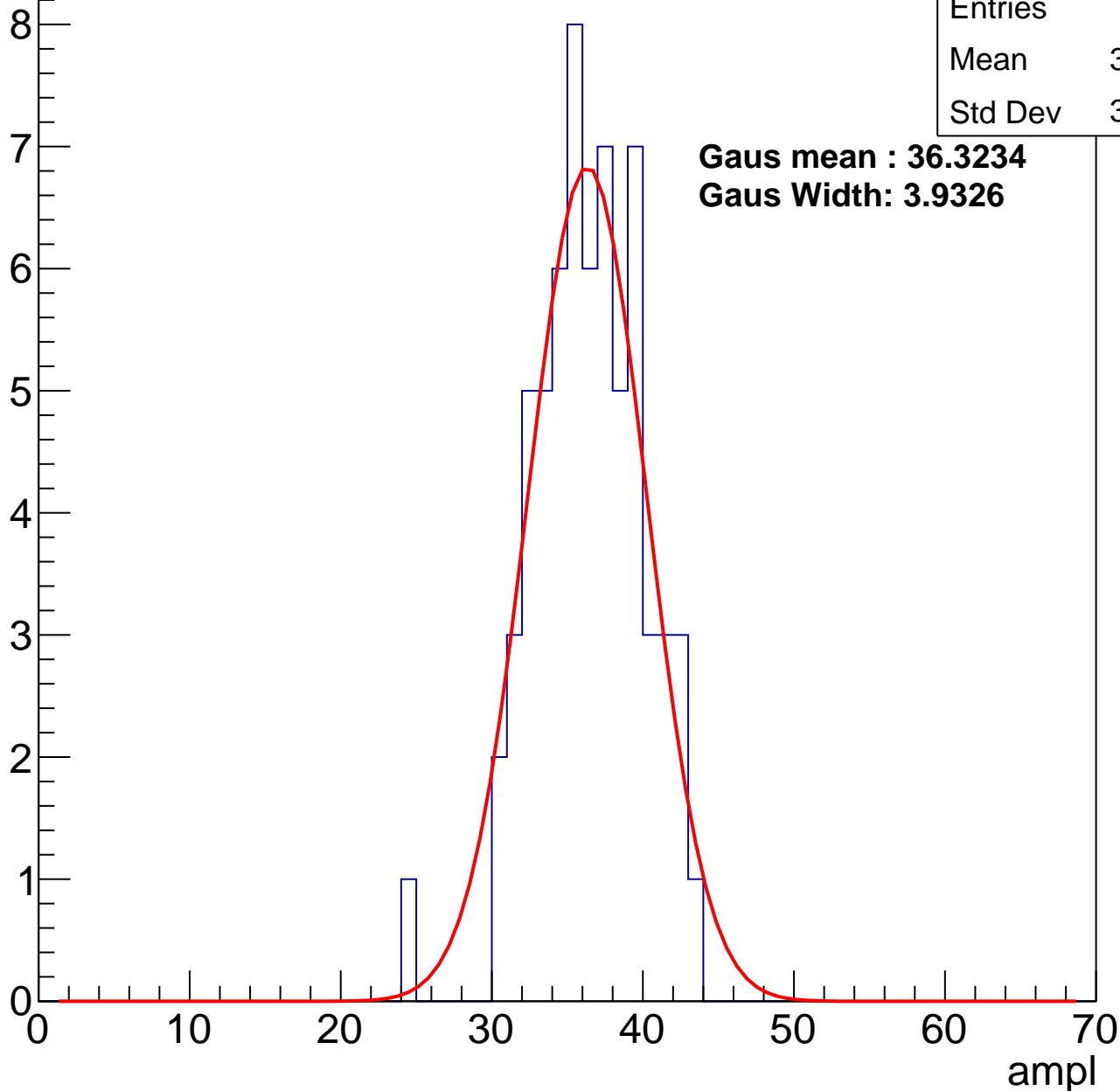
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	35.94
Std Dev	3.547

**Gaus mean : 36.3234**

**Gaus Width: 3.9326**



# B1L102S, U3-ch100, adc2

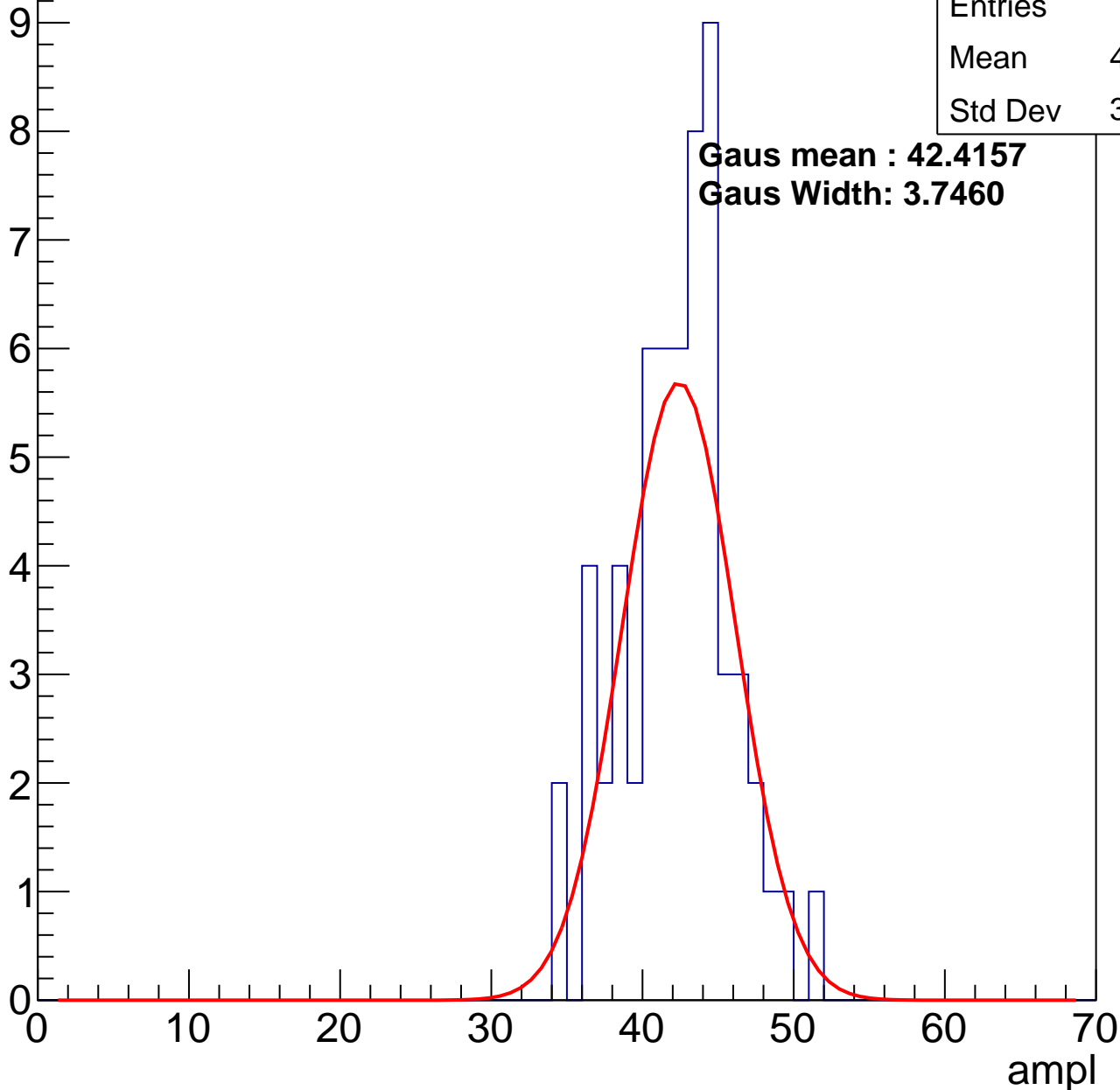
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	41.82
Std Dev	3.575

**Gaus mean : 42.4157**

**Gaus Width: 3.7460**

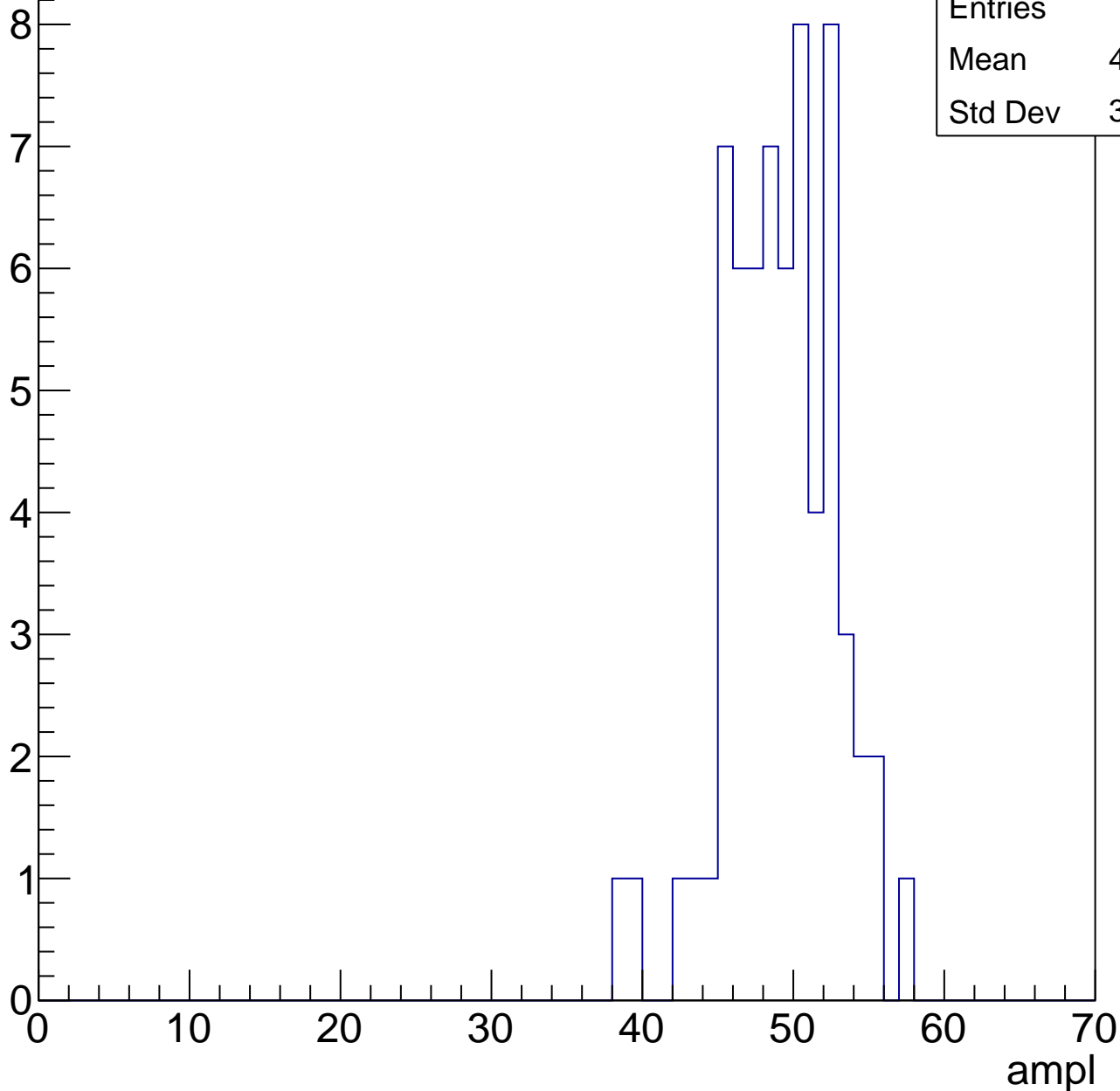


# B1L102S, U3-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	48.66
Std Dev	3.617

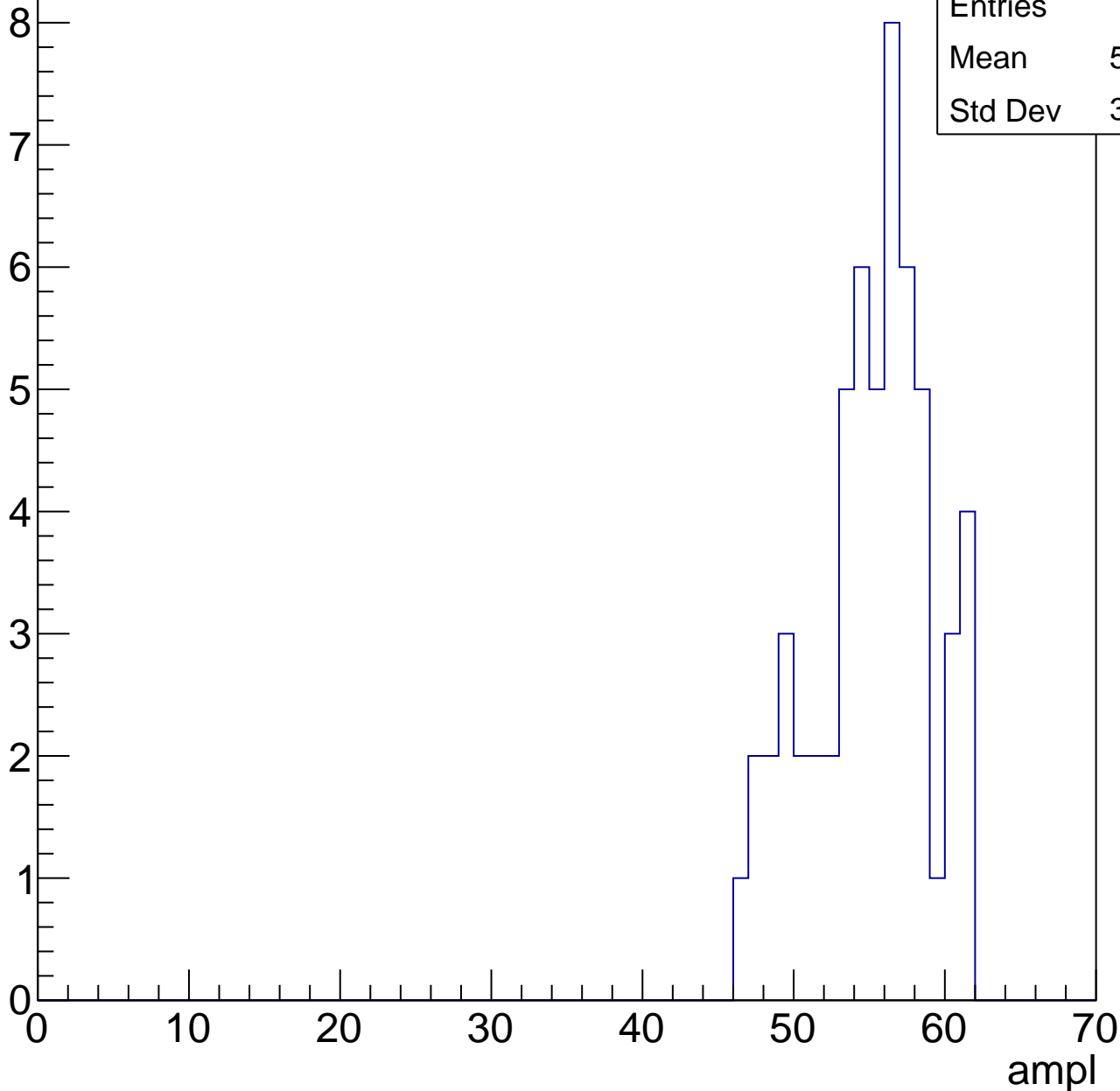


# B1L102S, U3-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	54.67
Std Dev	3.854

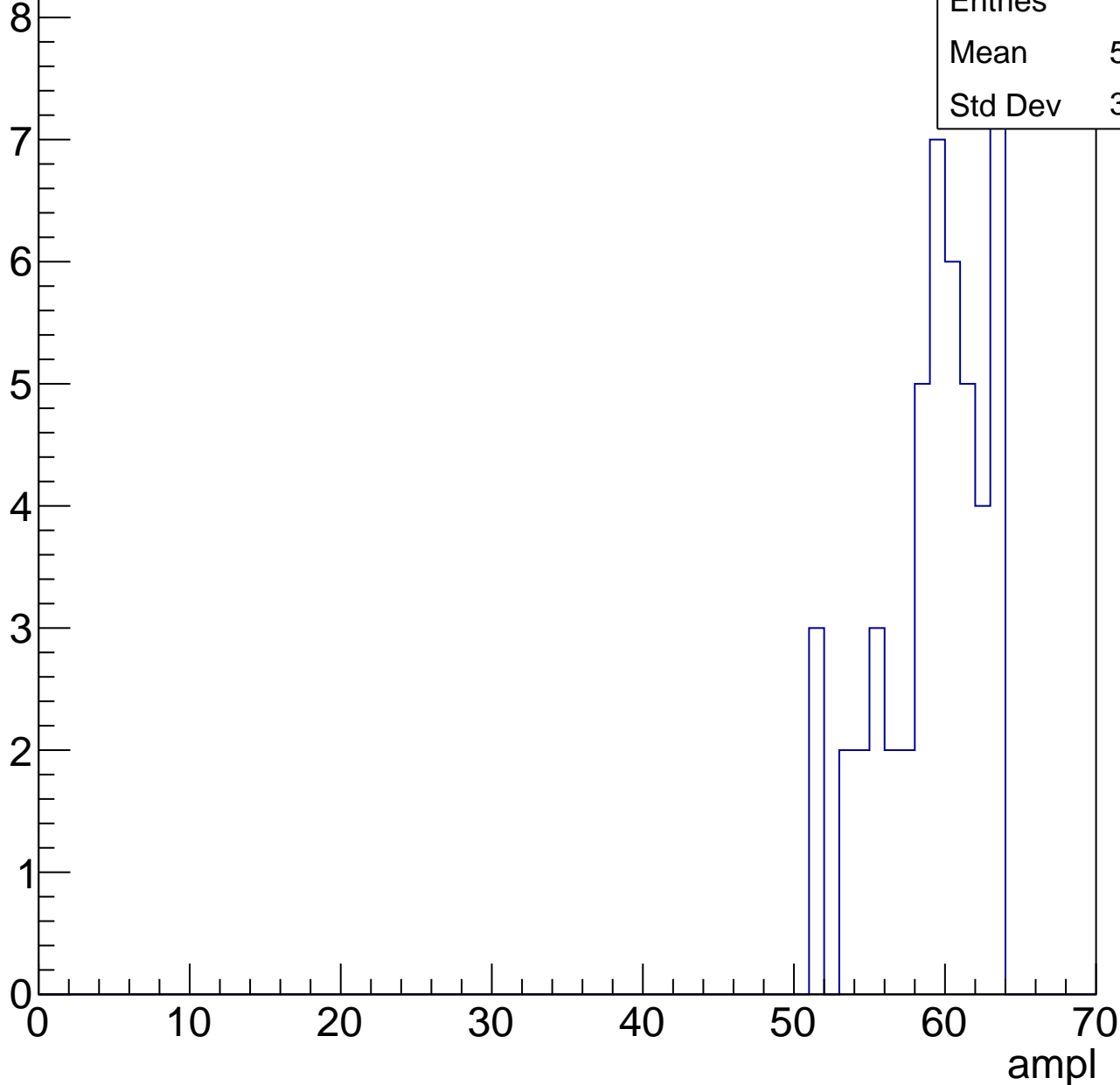


# B1L102S, U3-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	58.73
Std Dev	3.439

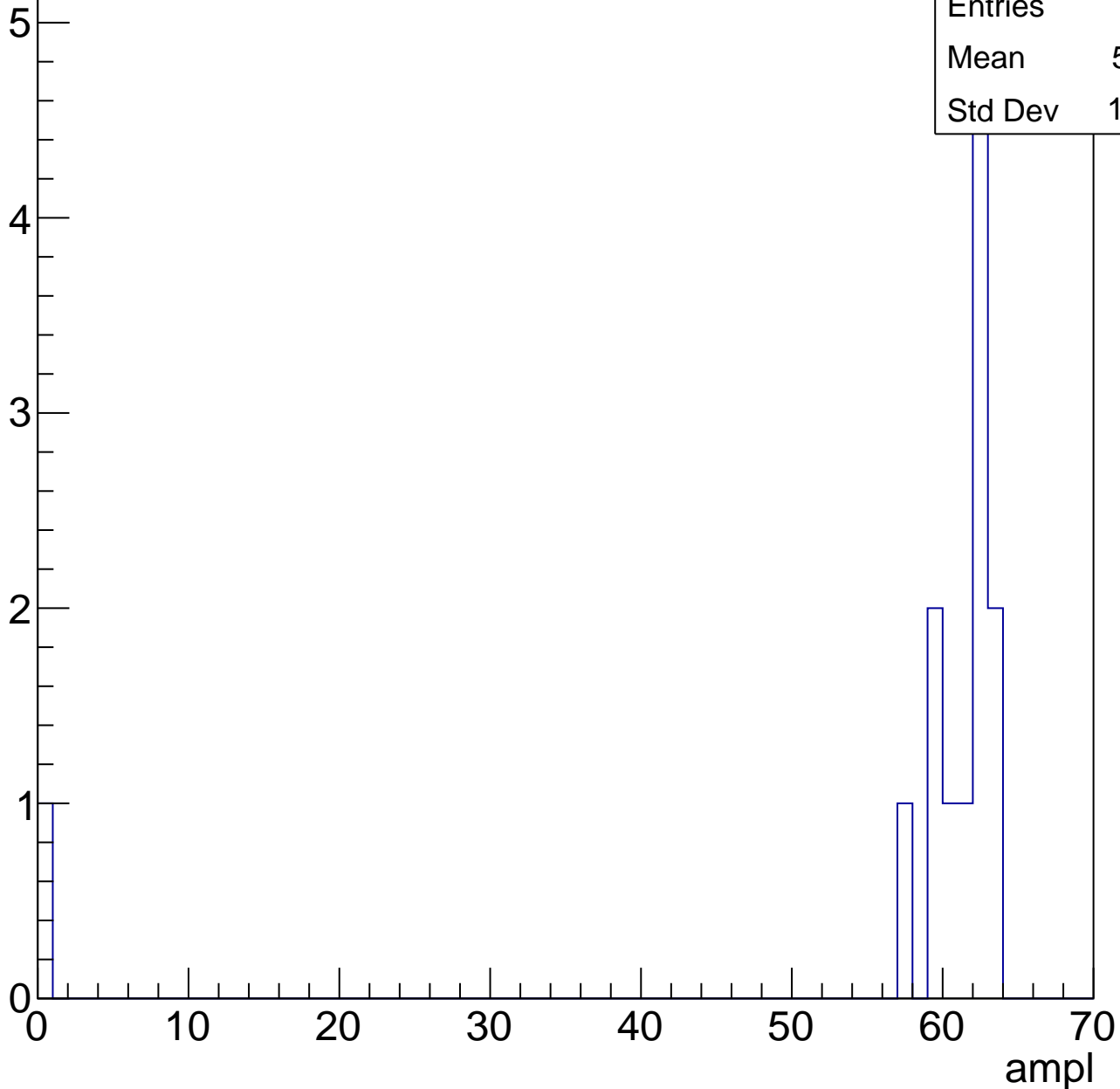


# B1L102S, U3-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	13
Mean	56.31
Std Dev	16.34





# B1L102S, U3-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch101, adc0

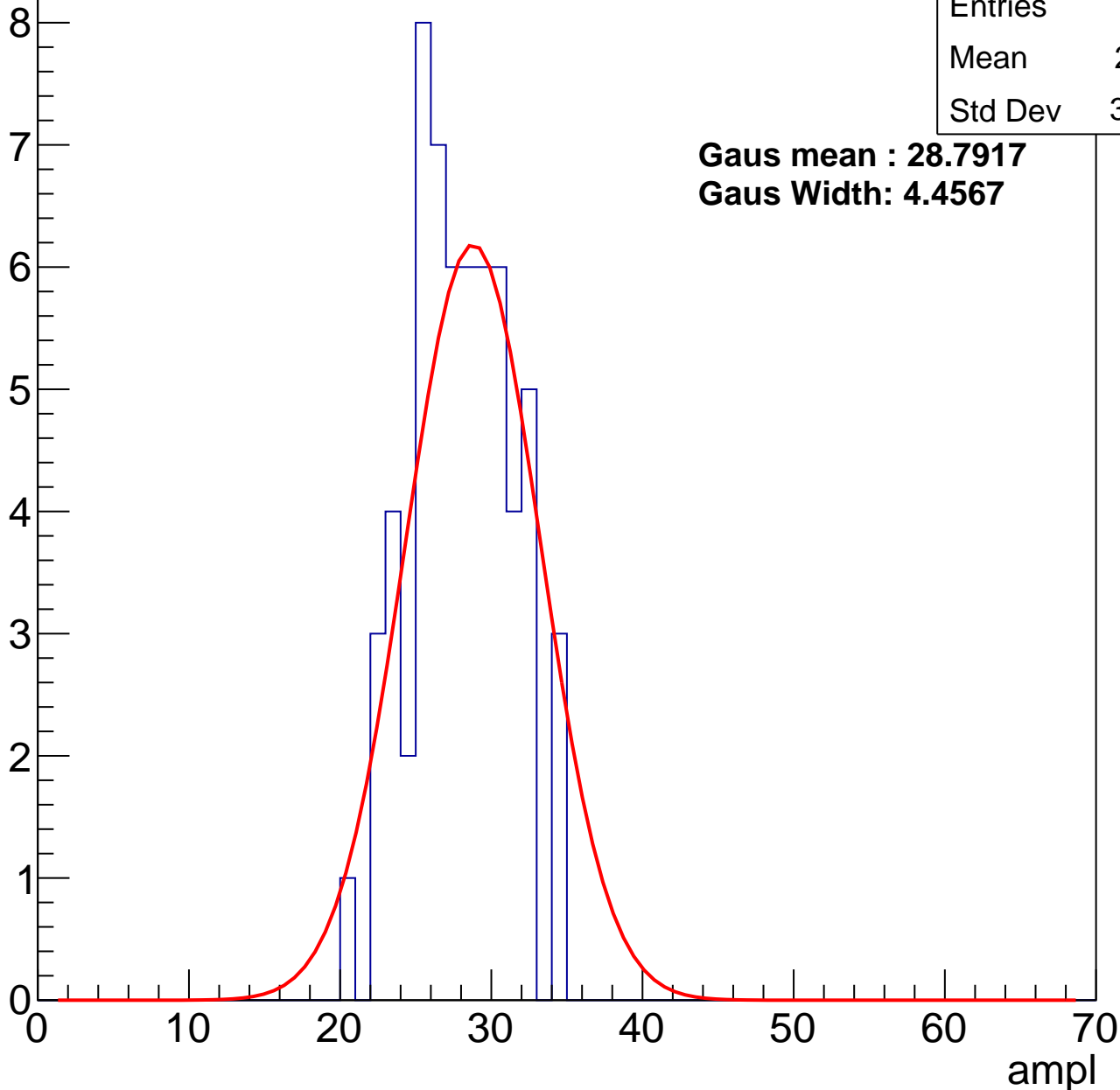
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	27.51
Std Dev	3.262

**Gaus mean : 28.7917**

**Gaus Width: 4.4567**



# B1L102S, U3-ch101, adc1

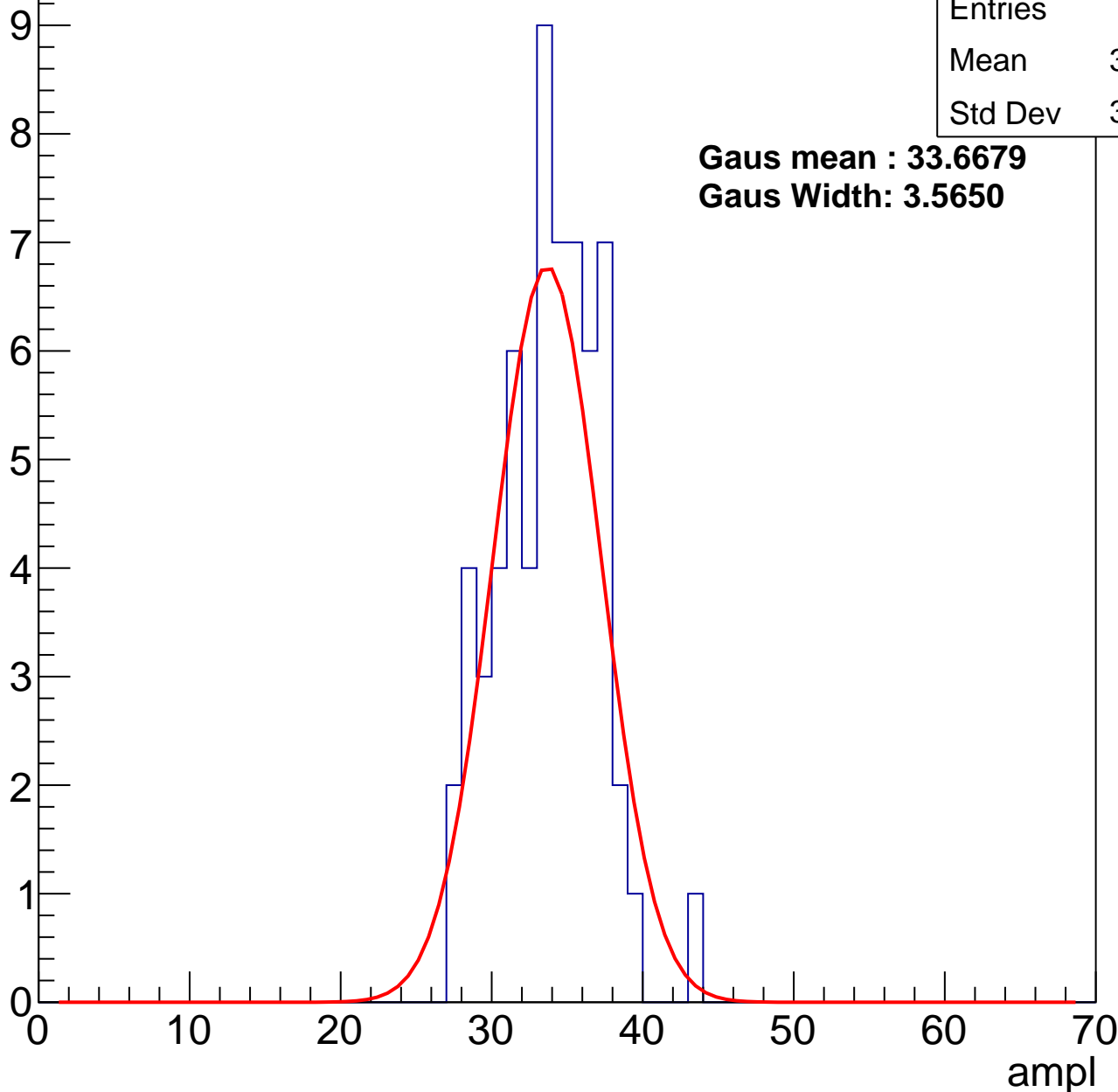
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	33.33
Std Dev	3.246

**Gaus mean : 33.6679**

**Gaus Width: 3.5650**



# B1L102S, U3-ch101, adc2

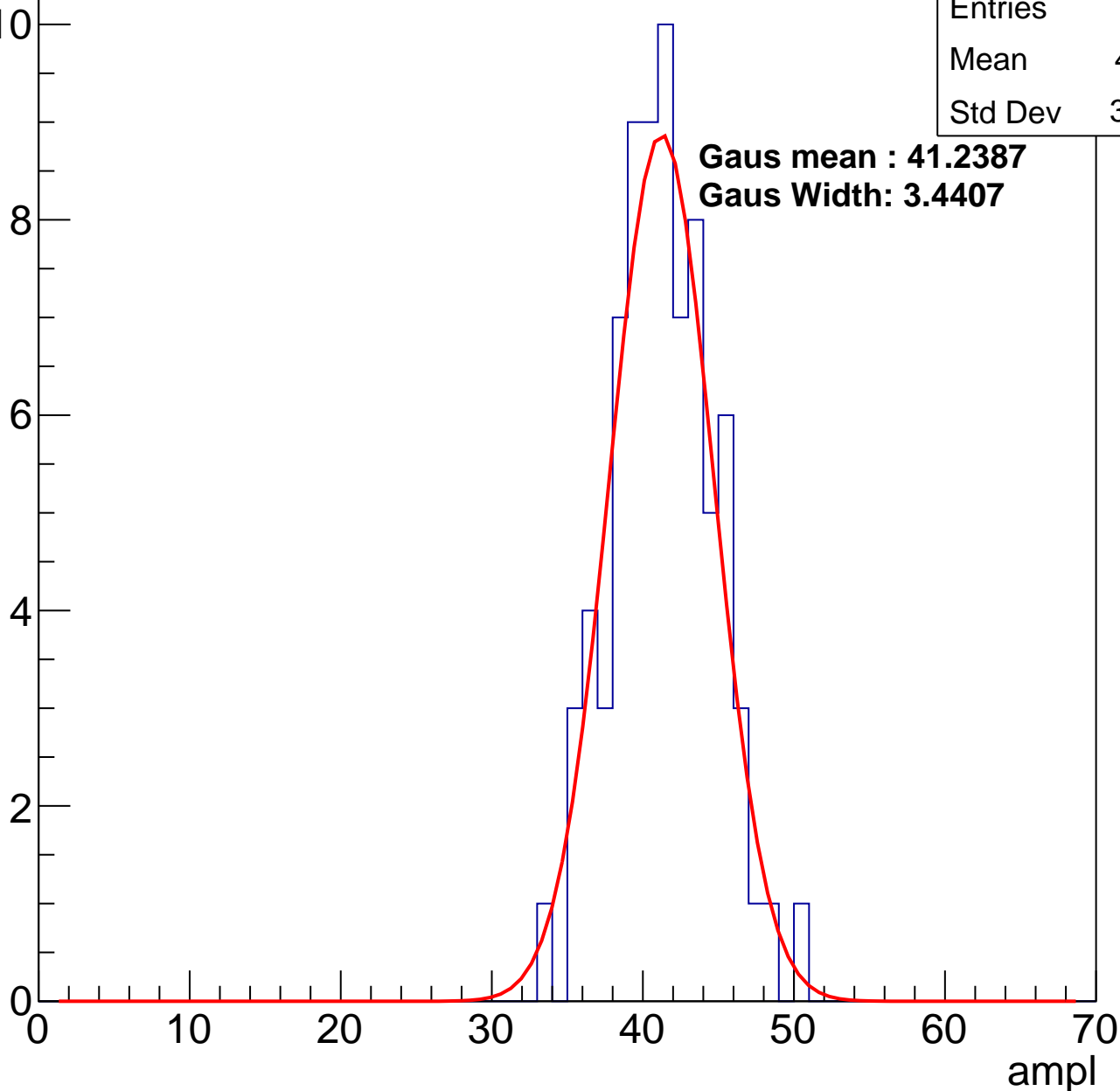
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	40.91
Std Dev	3.298

**Gaus mean : 41.2387**

**Gaus Width: 3.4407**

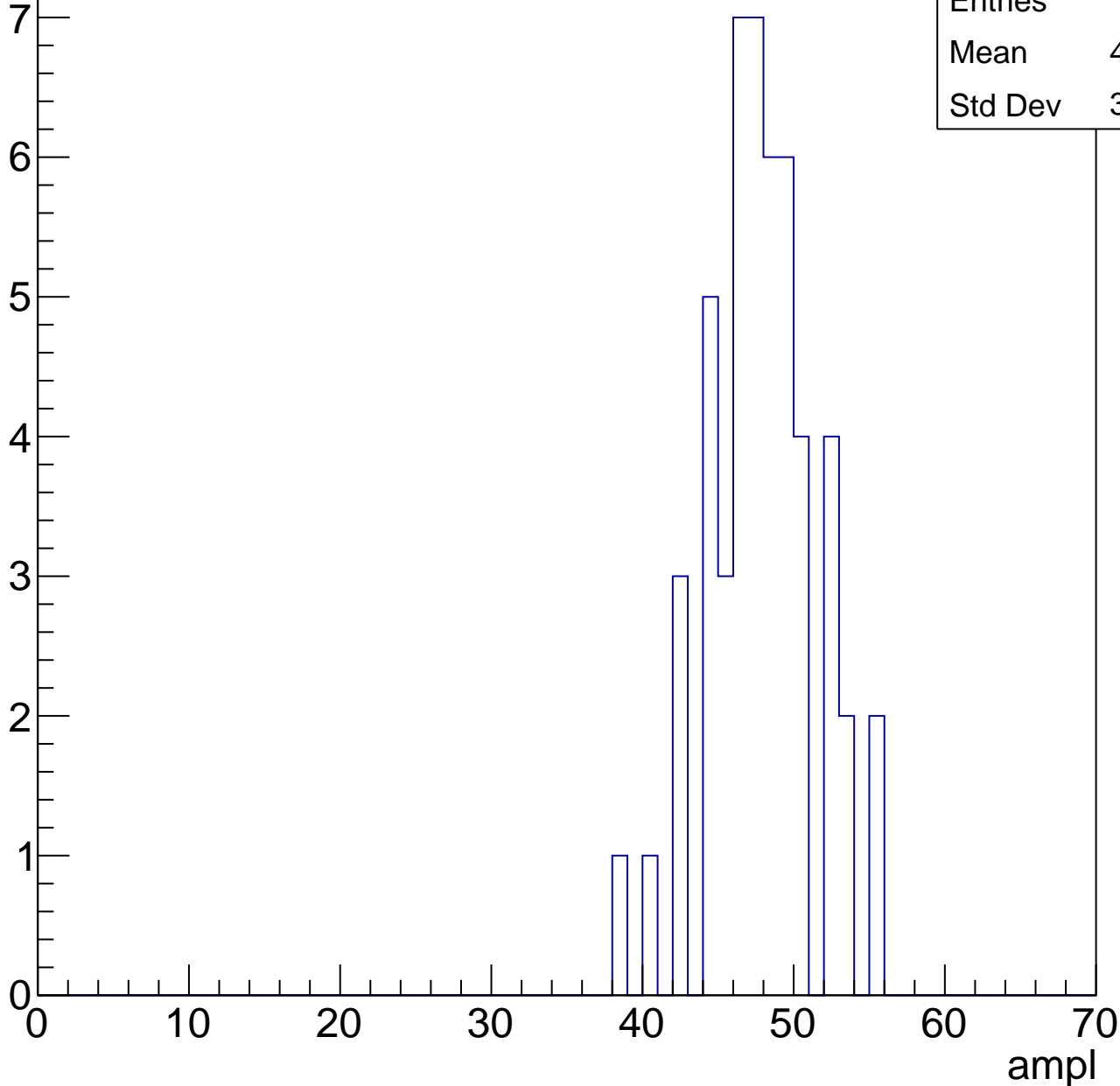


# B1L102S, U3-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	47.37
Std Dev	3.509

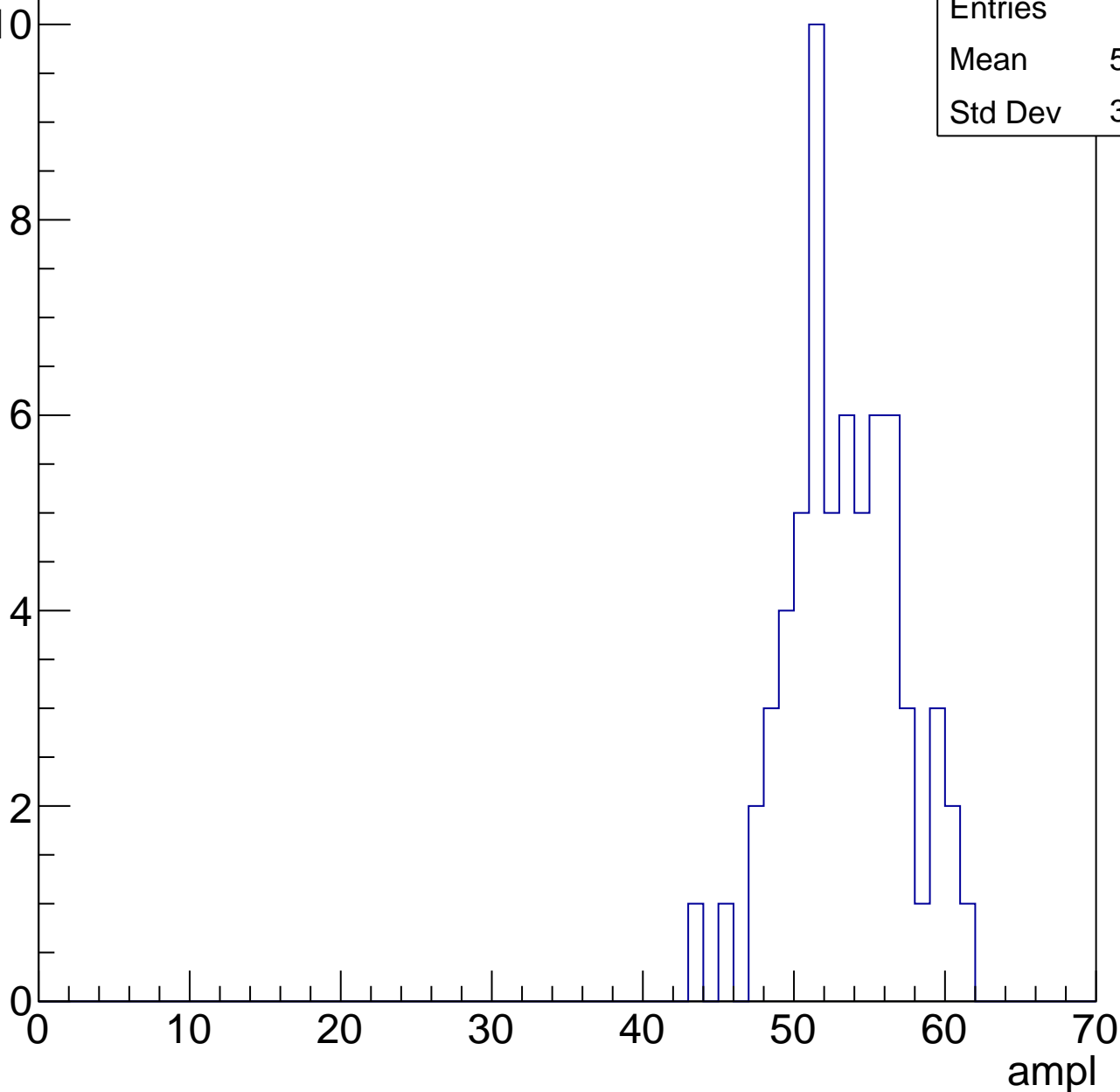


# B1L102S, U3-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	52.86
Std Dev	3.729

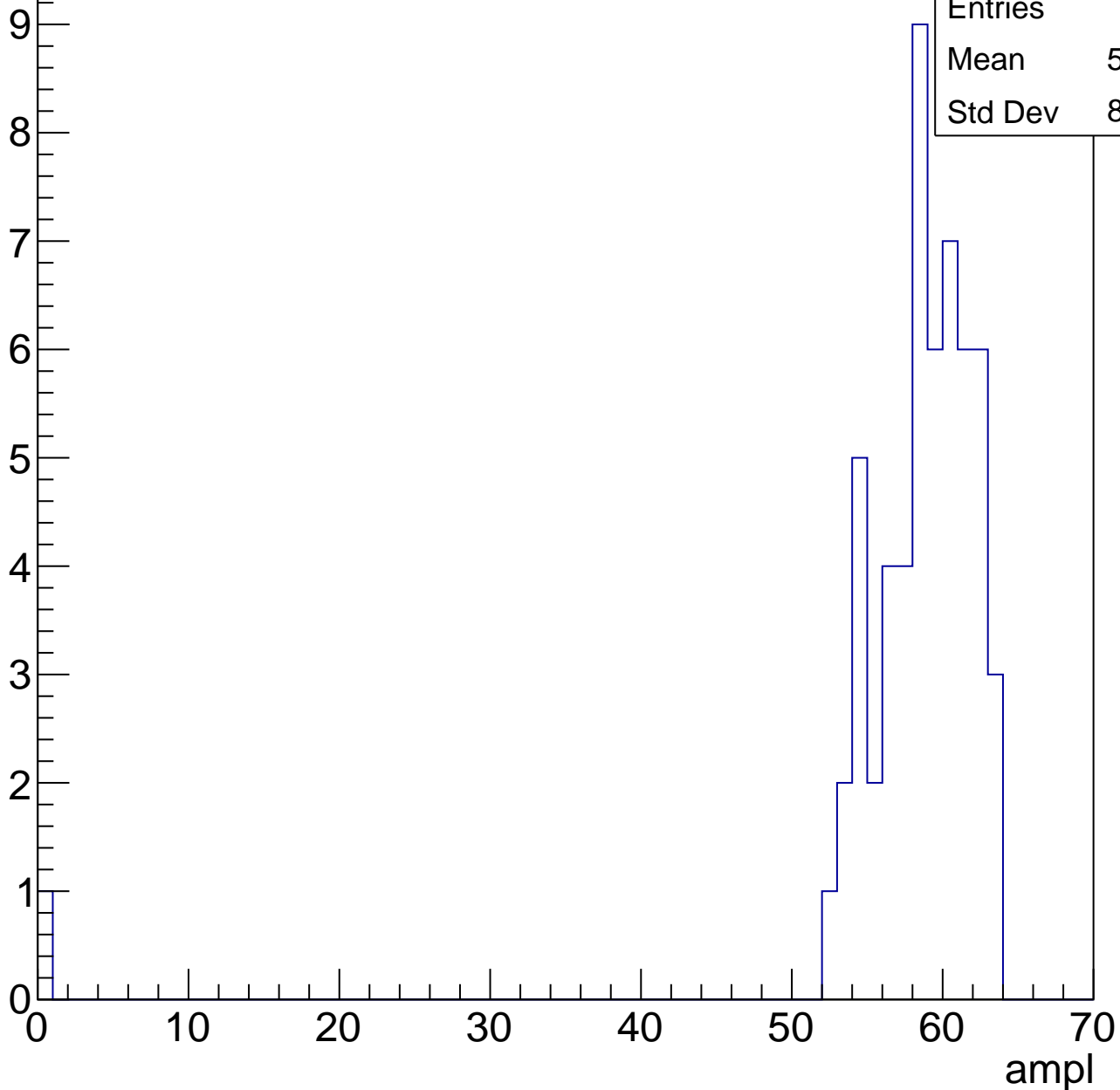


# B1L102S, U3-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	57.38
Std Dev	8.243

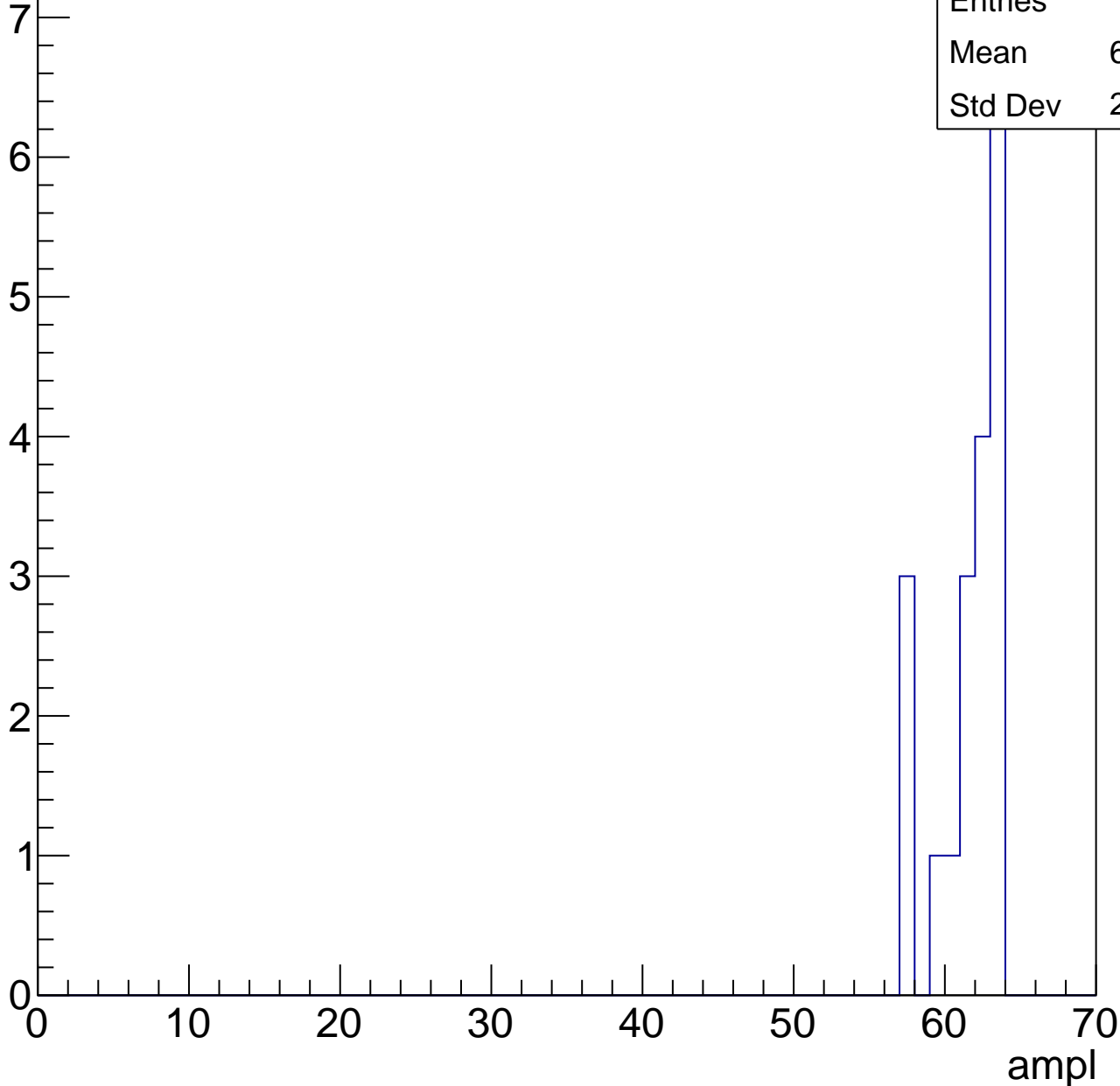


# B1L102S, U3-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	19
Mean	61.16
Std Dev	2.109

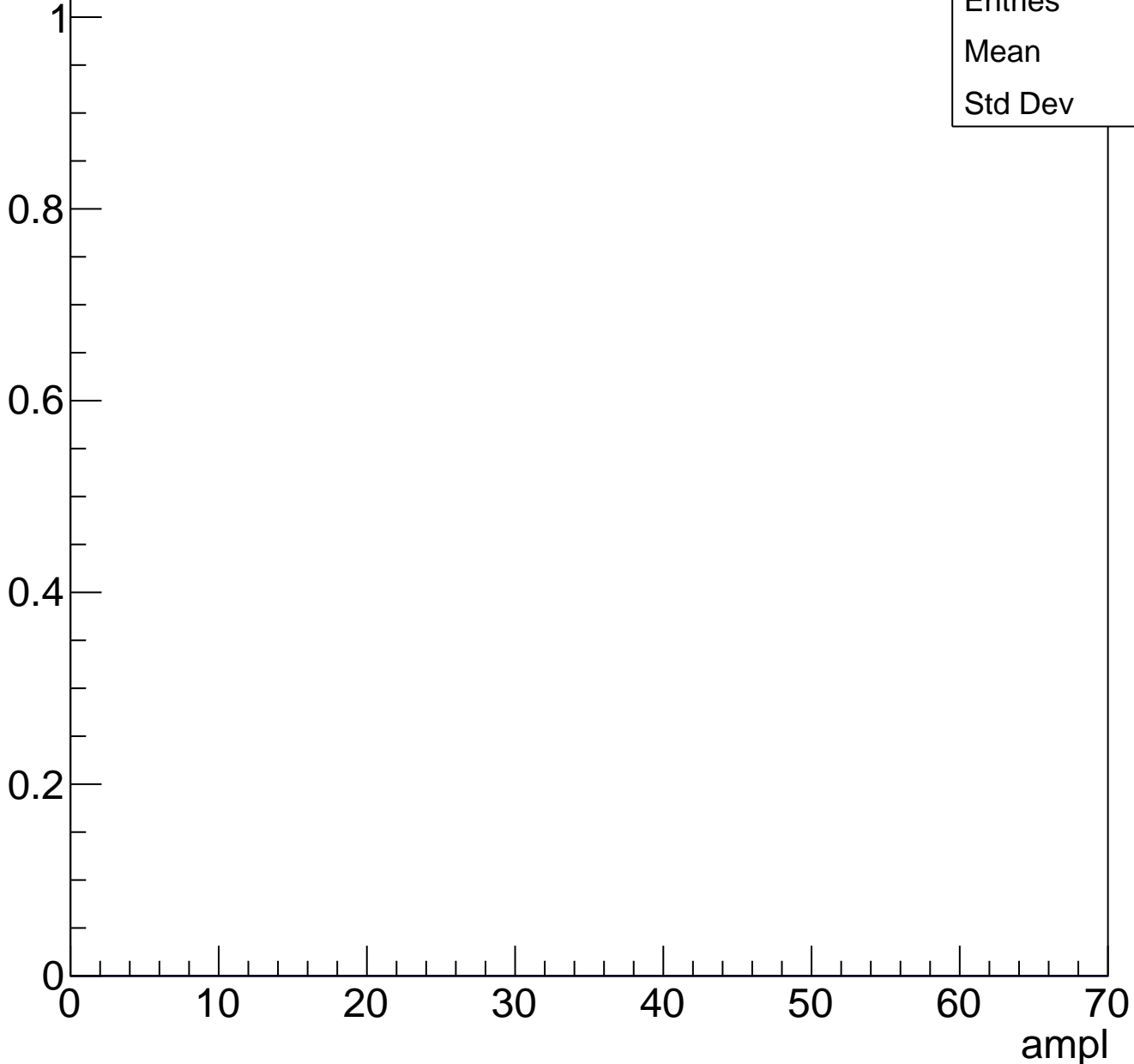




# B1L102S, U3-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U3-ch102, adc0

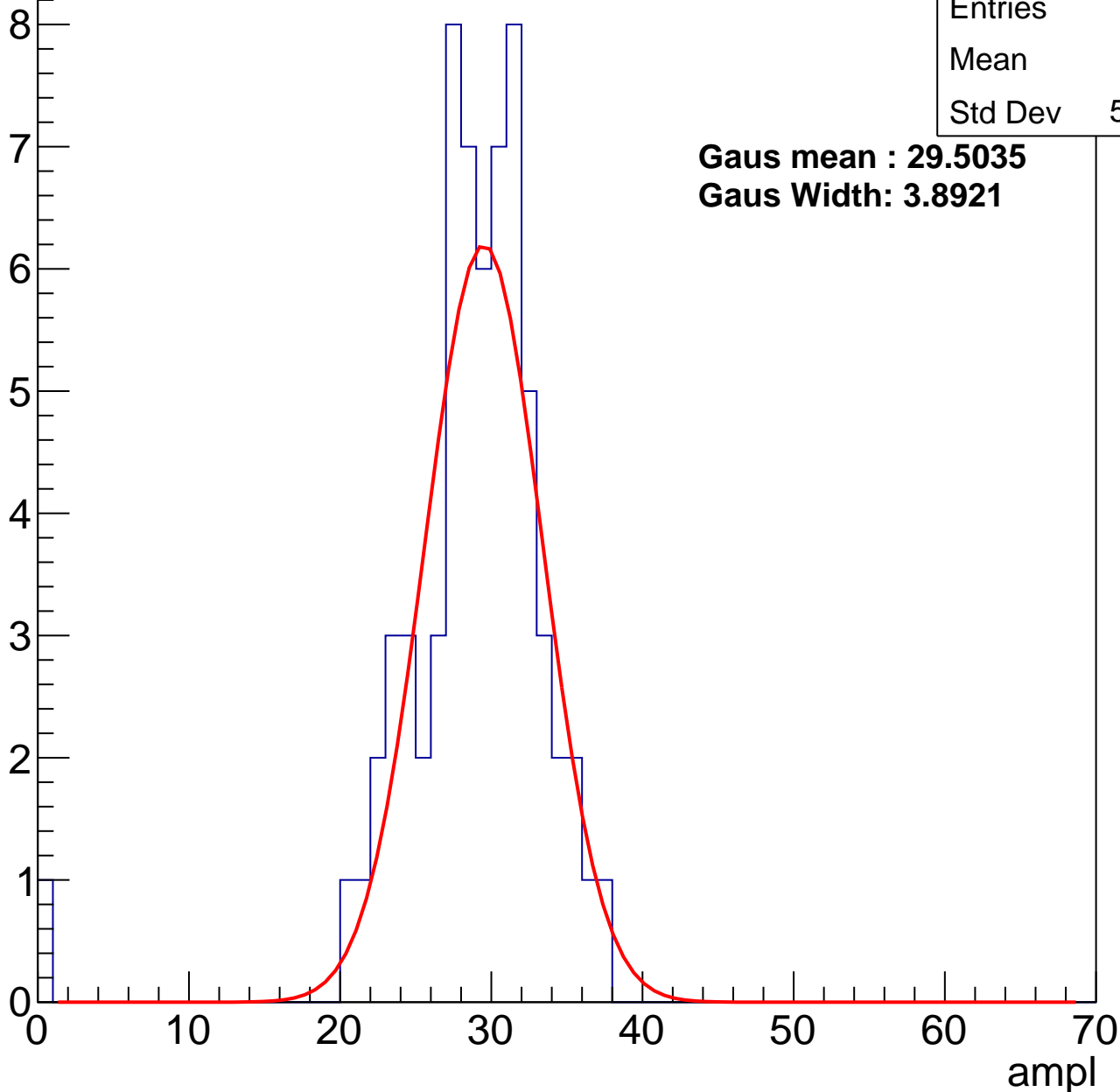
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	28.3
Std Dev	5.075

**Gaus mean : 29.5035**

**Gaus Width: 3.8921**



# B1L102S, U3-ch102, adc1

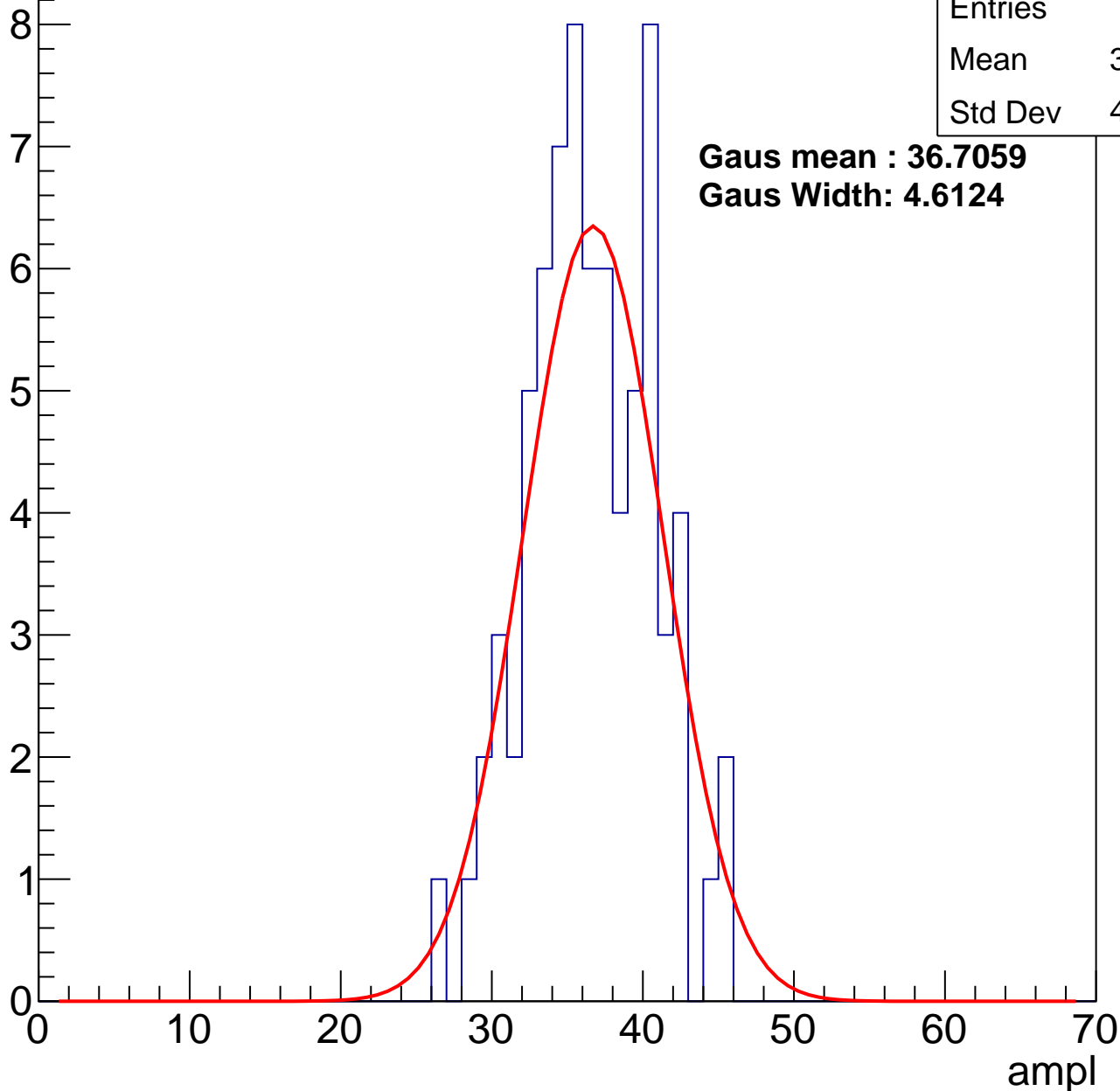
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	36.08
Std Dev	4.076

**Gaus mean : 36.7059**

**Gaus Width: 4.6124**



# B1L102S, U3-ch102, adc2

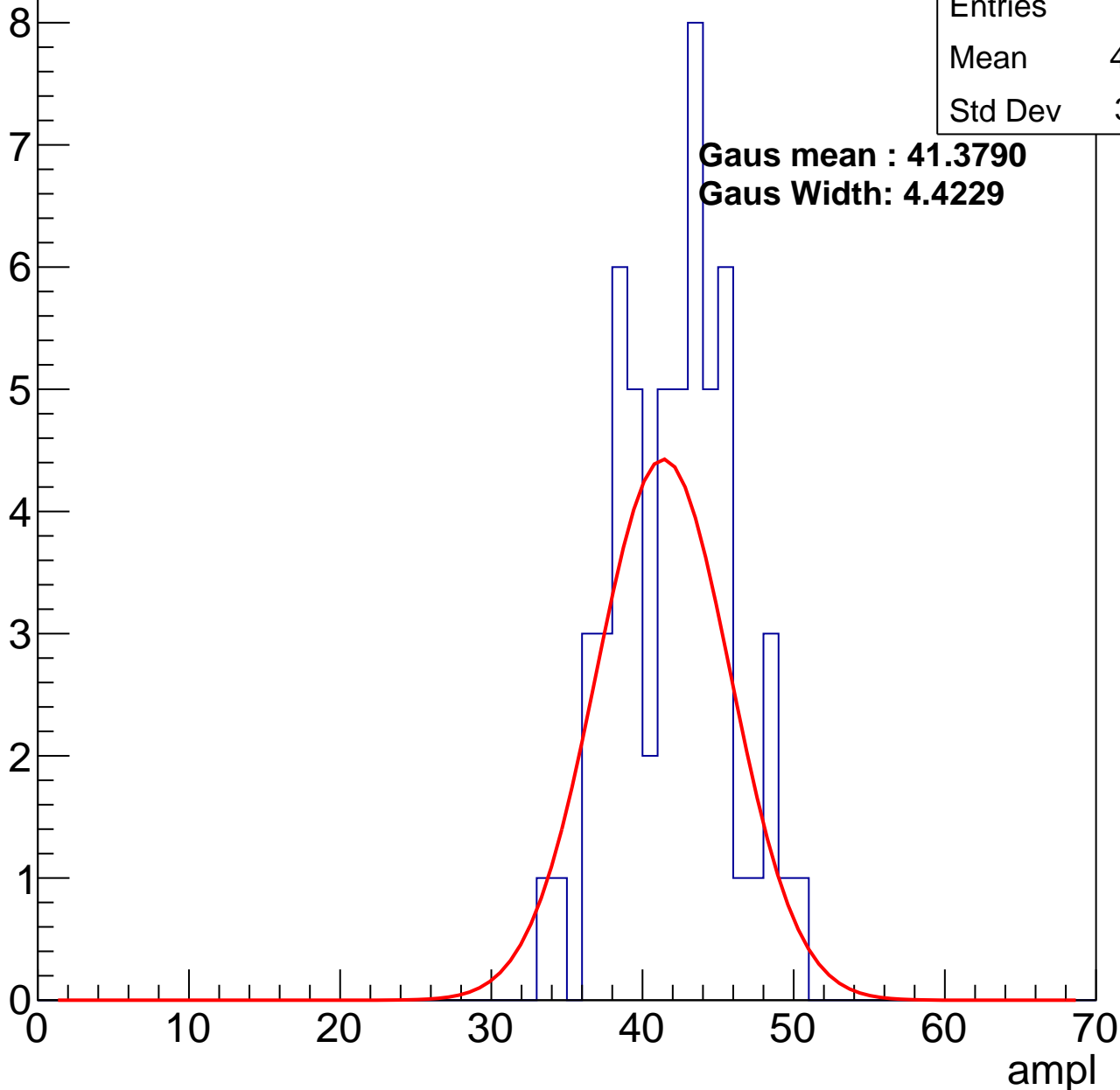
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	41.65
Std Dev	3.791

**Gaus mean : 41.3790**

**Gaus Width: 4.4229**

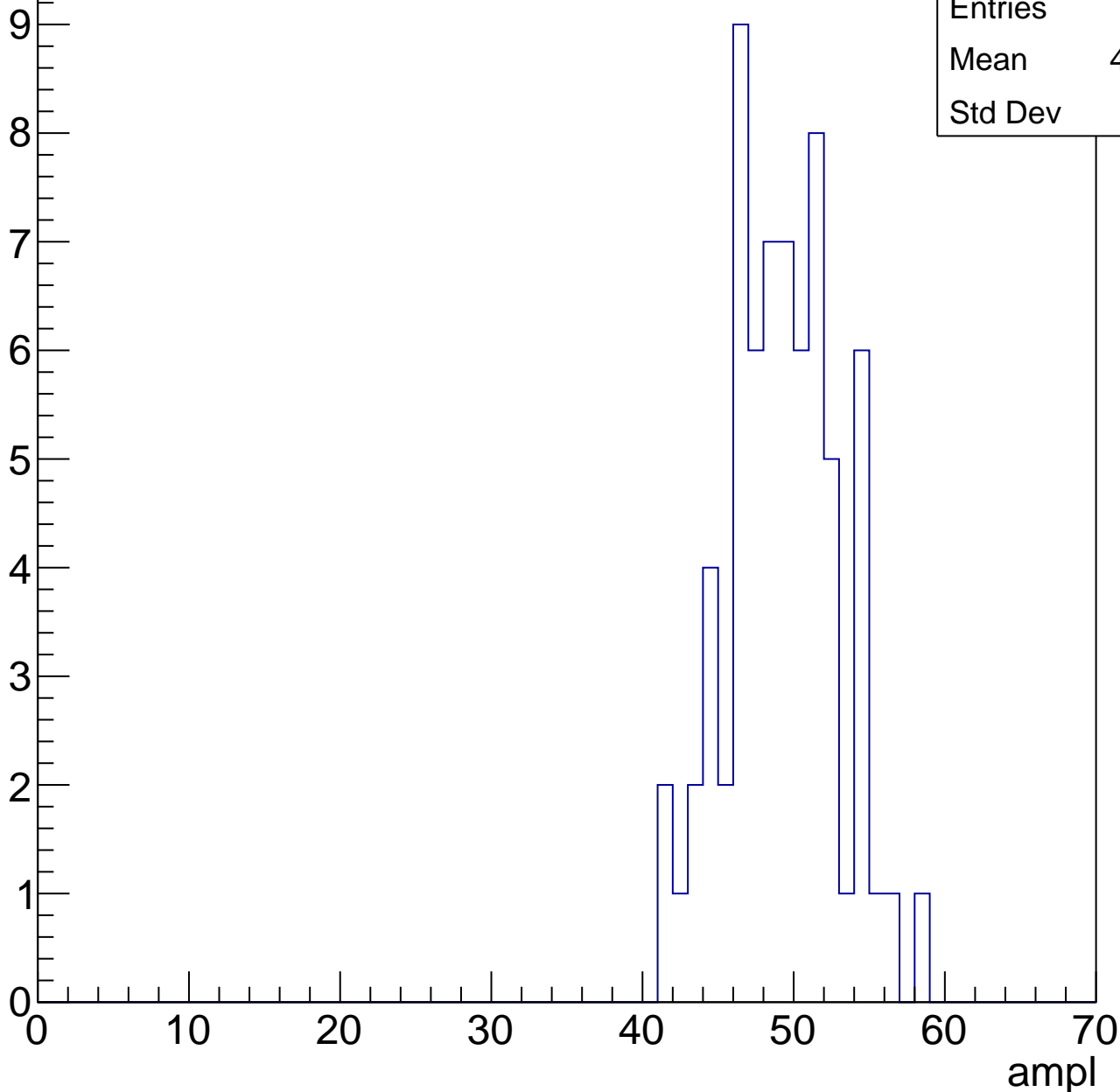


# B1L102S, U3-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	48.77
Std Dev	3.62

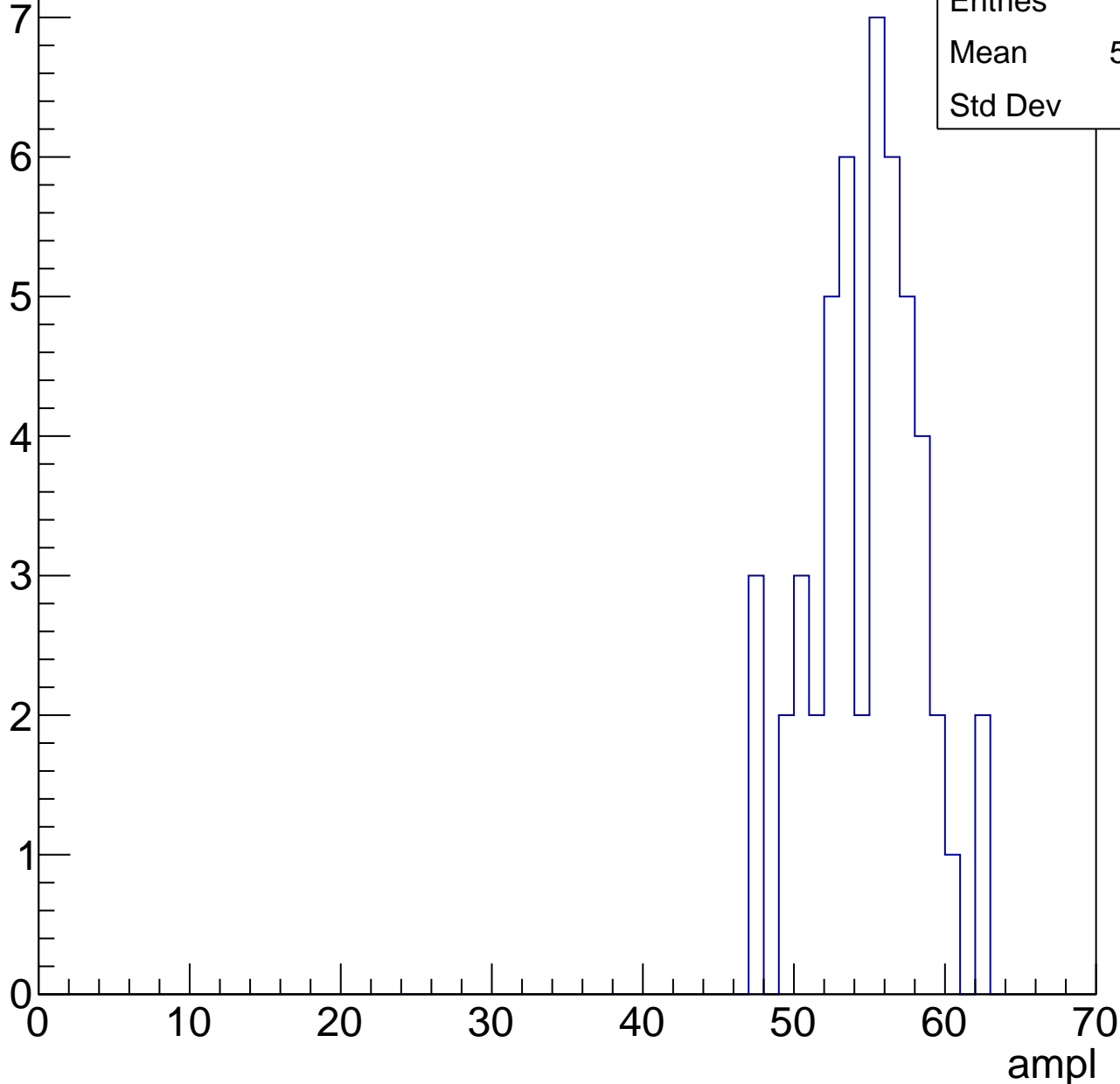


# B1L102S, U3-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	54.34
Std Dev	3.57



# B1L102S, U3-ch102, adc5

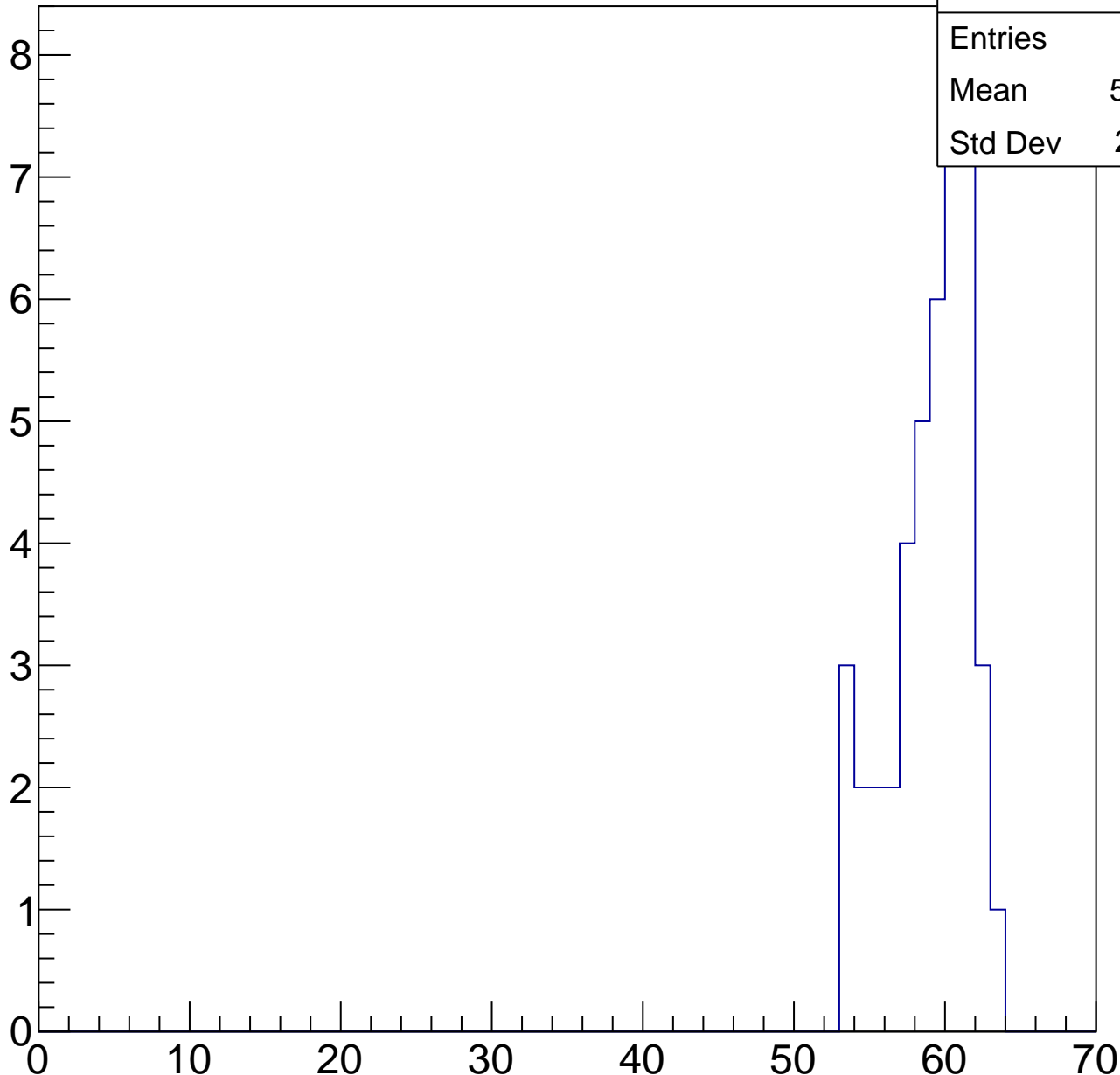
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	44
Mean	58.59
Std Dev	2.631

ampl

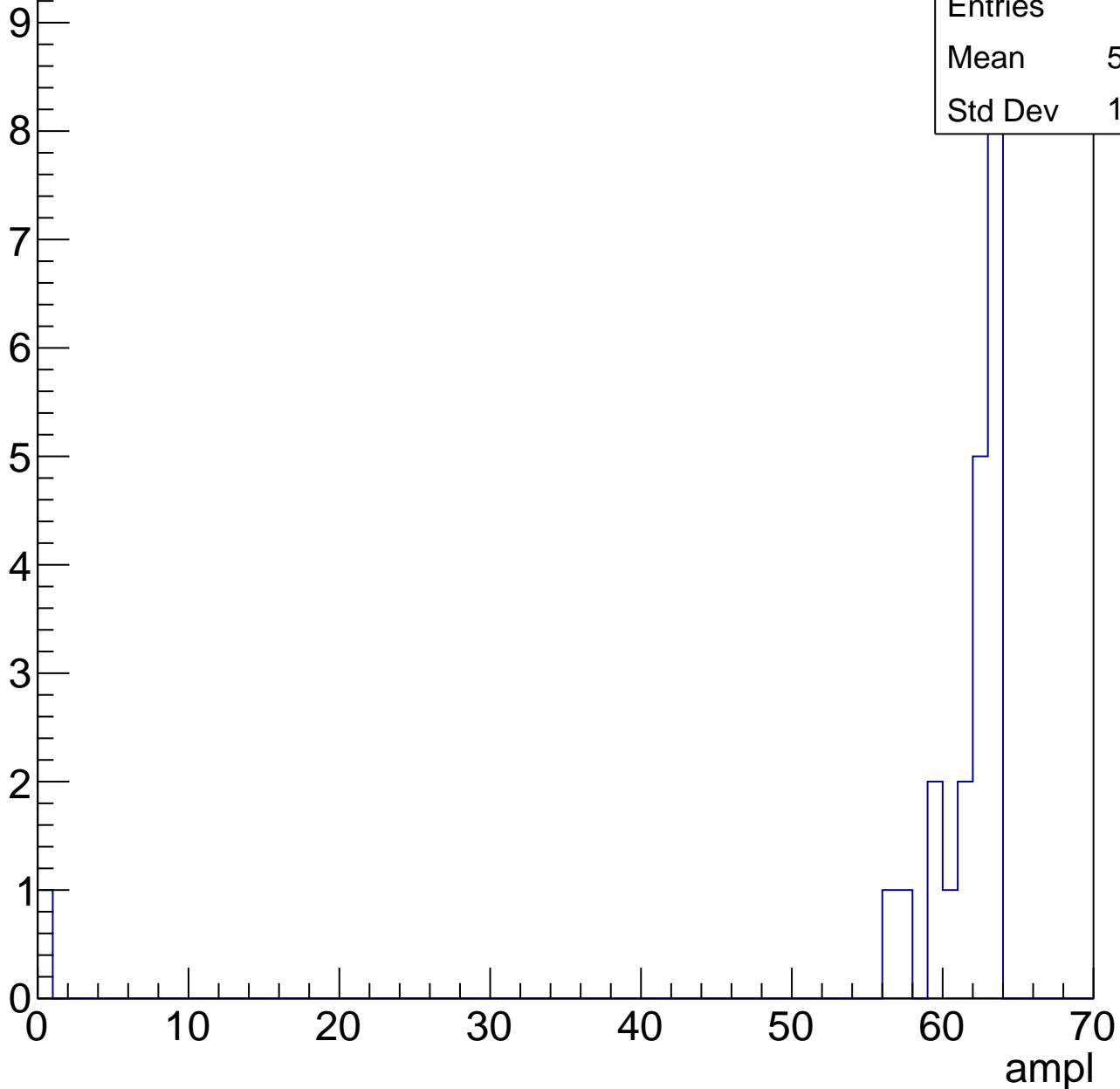


# B1L102S, U3-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	22
Mean	58.64
Std Dev	12.95





# B1L102S, U3-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U3-ch103, adc0

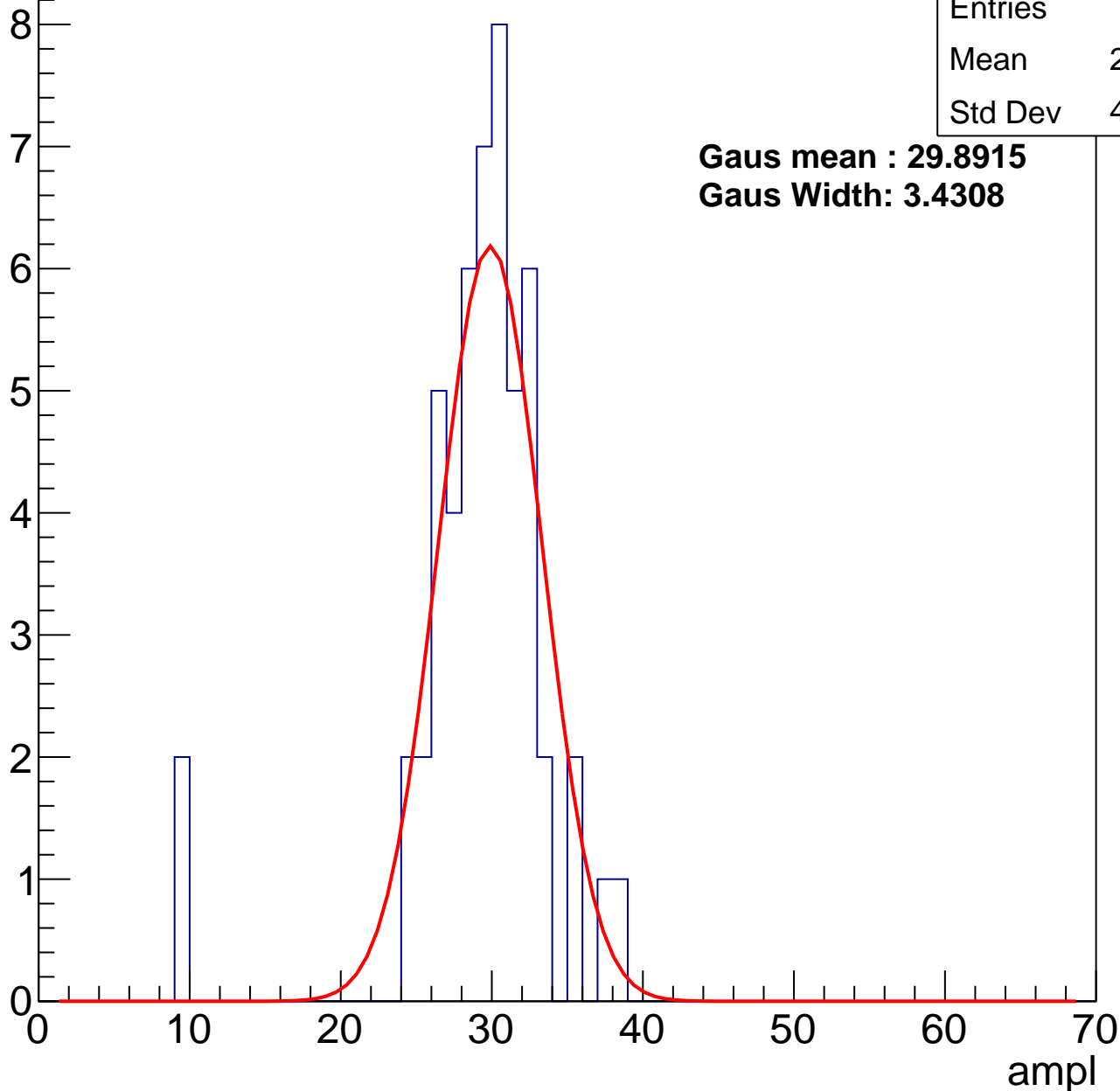
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	28.74
Std Dev	4.907

**Gaus mean : 29.8915**

**Gaus Width: 3.4308**



# B1L102S, U3-ch103, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	61
Mean	34.92
Std Dev	3.048

**Gaus mean : 35.1166**

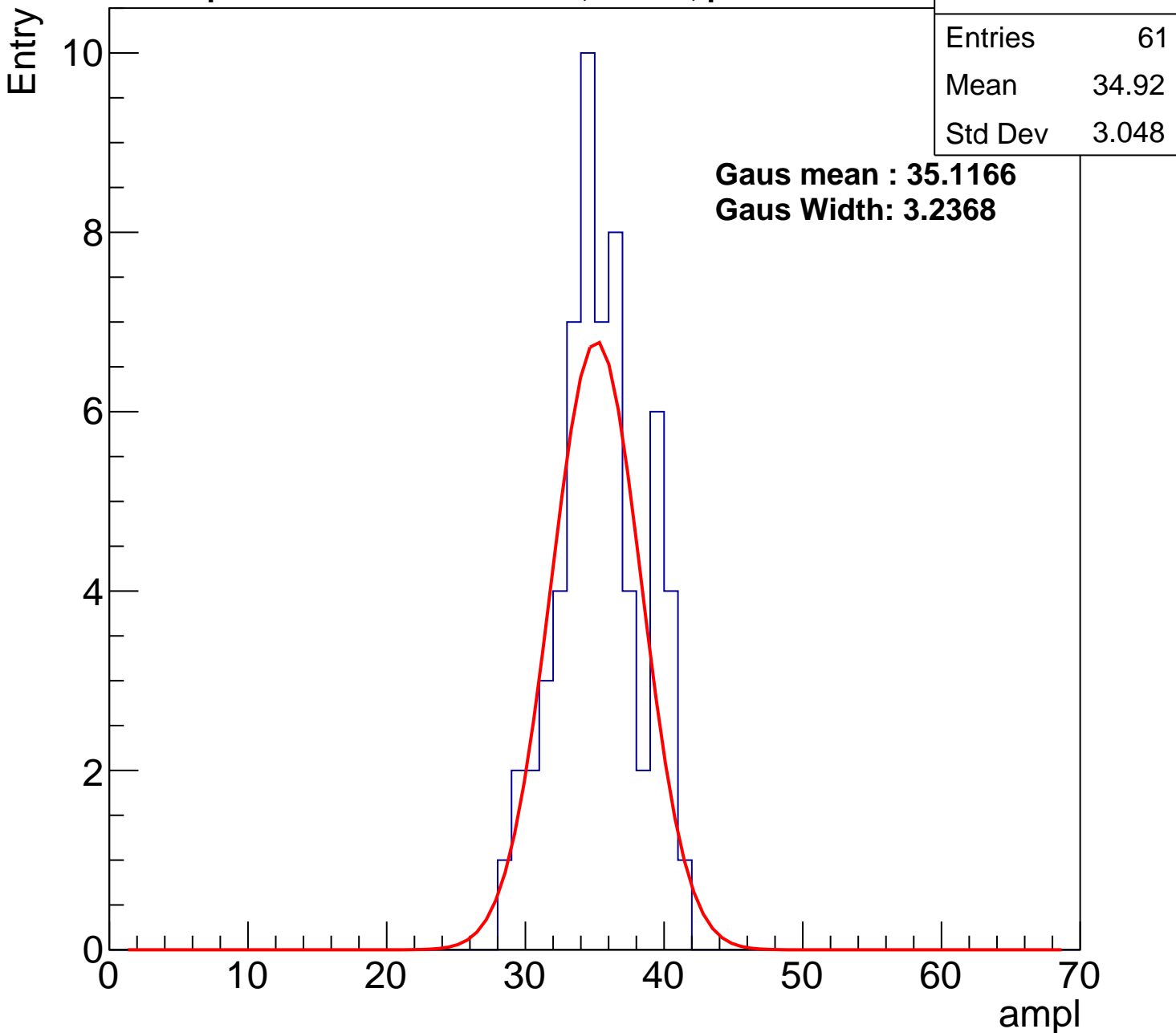
**Gaus Width: 3.2368**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U3-ch103, adc2

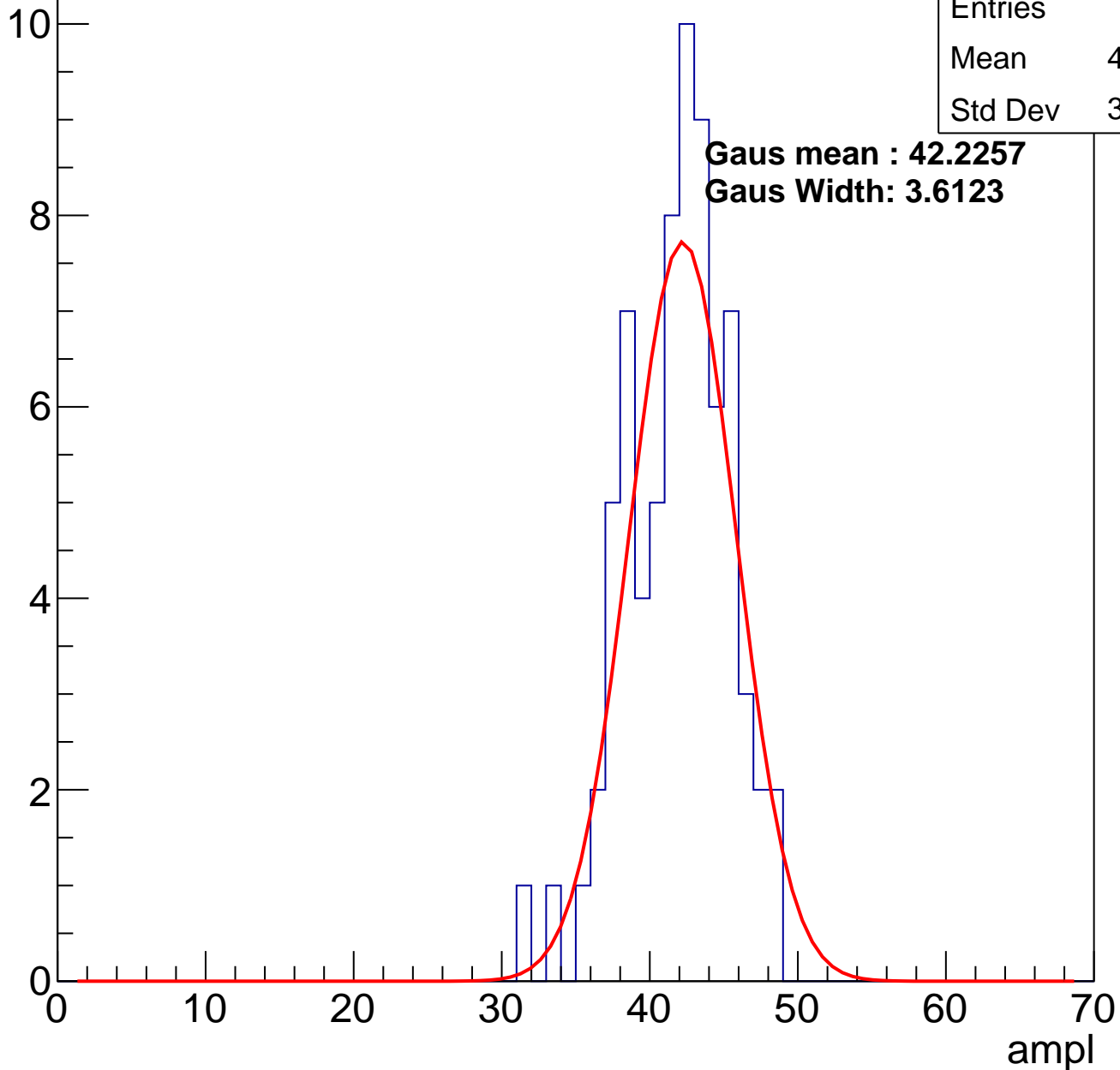
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	73
Mean	41.37
Std Dev	3.434

**Gaus mean : 42.2257**

**Gaus Width: 3.6123**

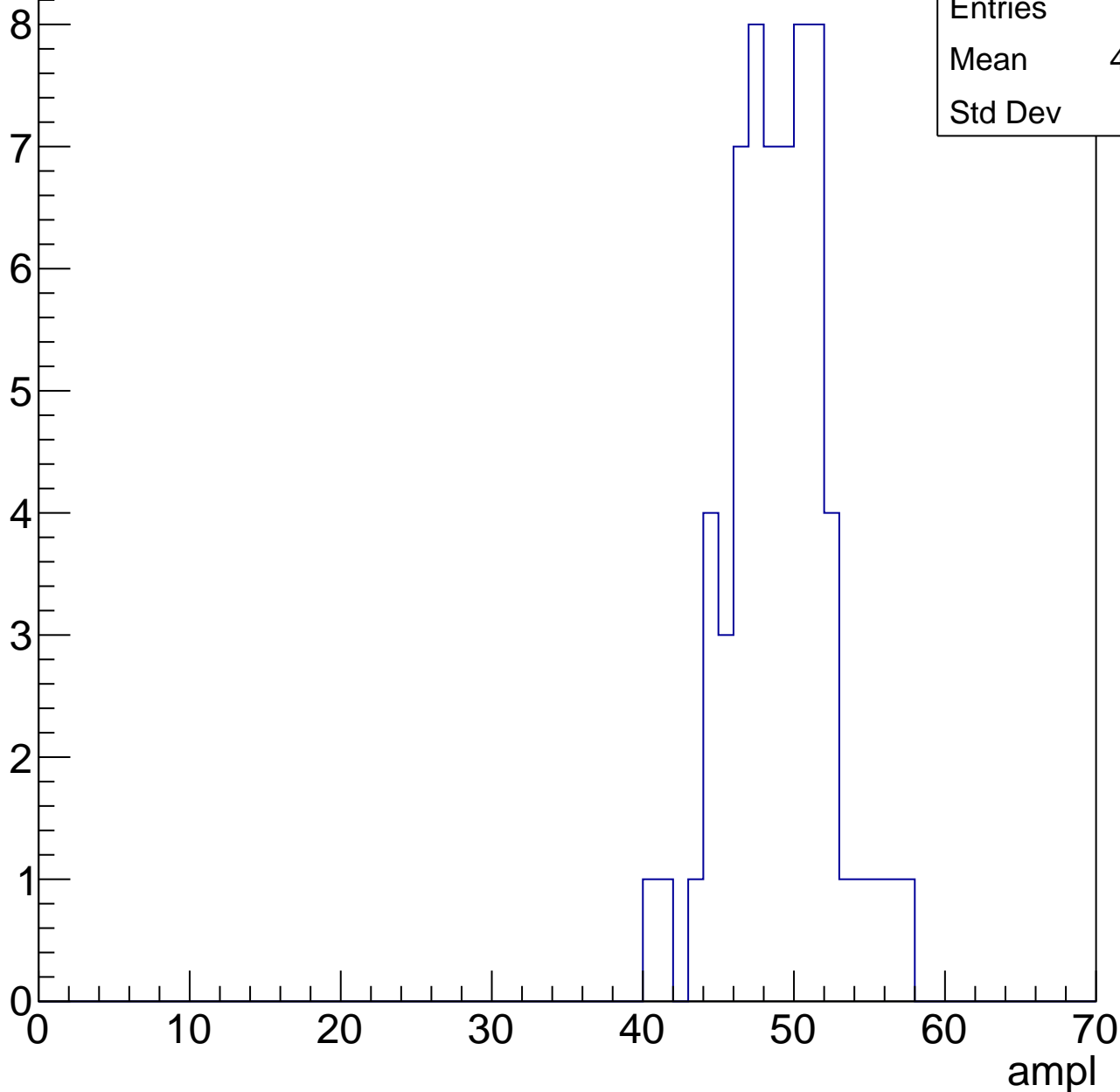
Entry



# B1L102S, U3-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

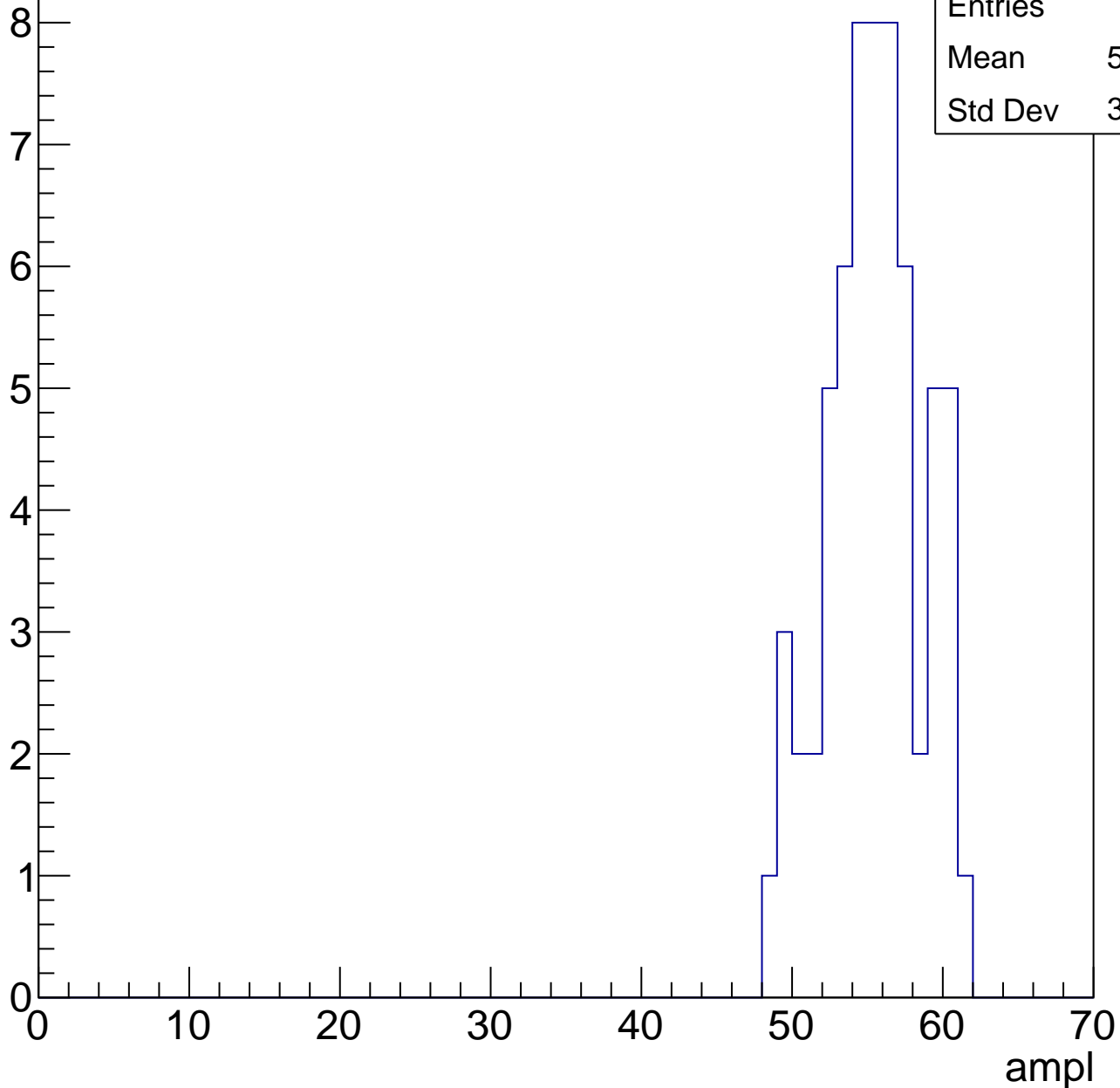


Entries	64
Mean	48.48
Std Dev	3.26

# B1L102S, U3-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

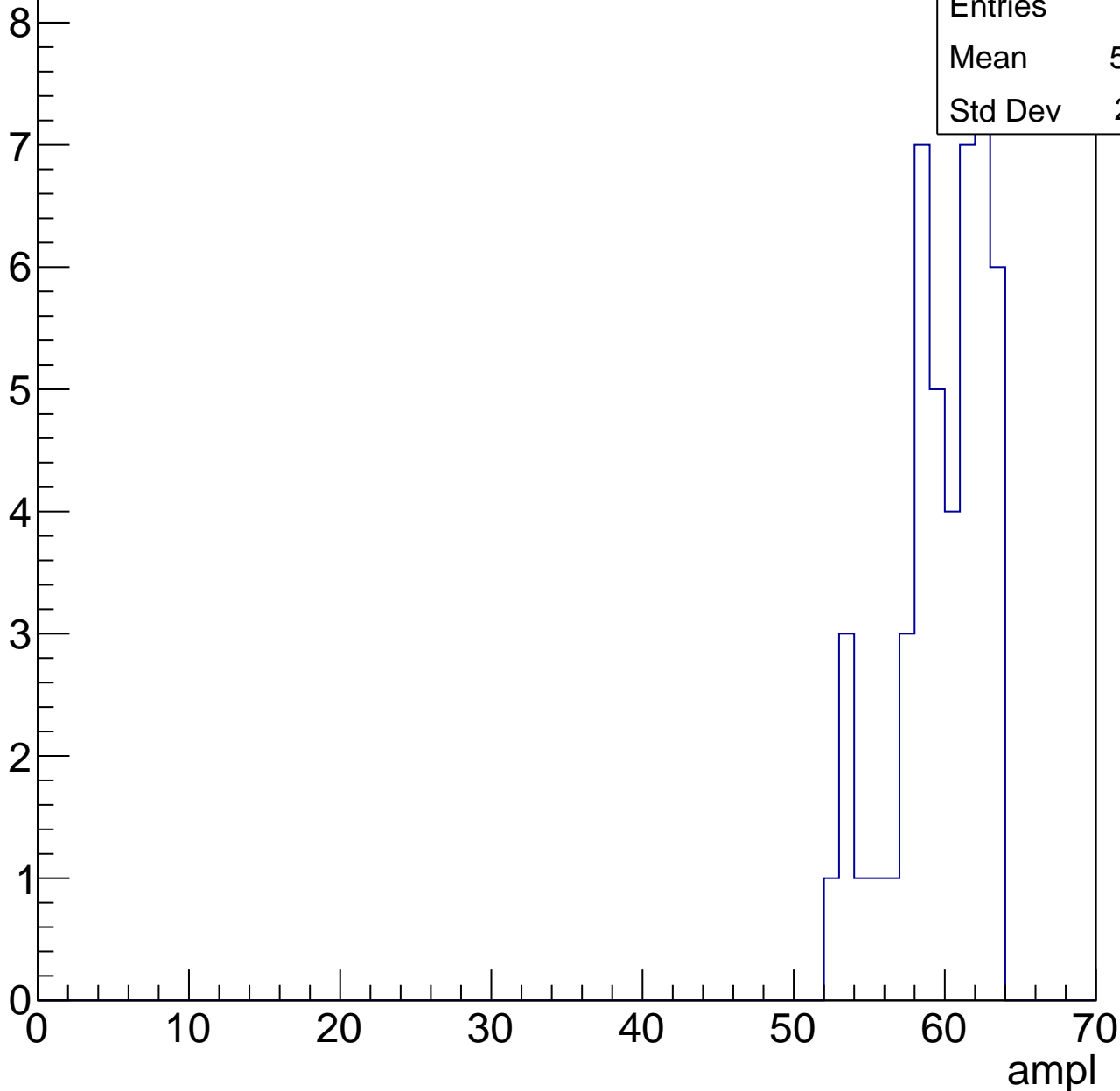


# B1L102S, U3-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

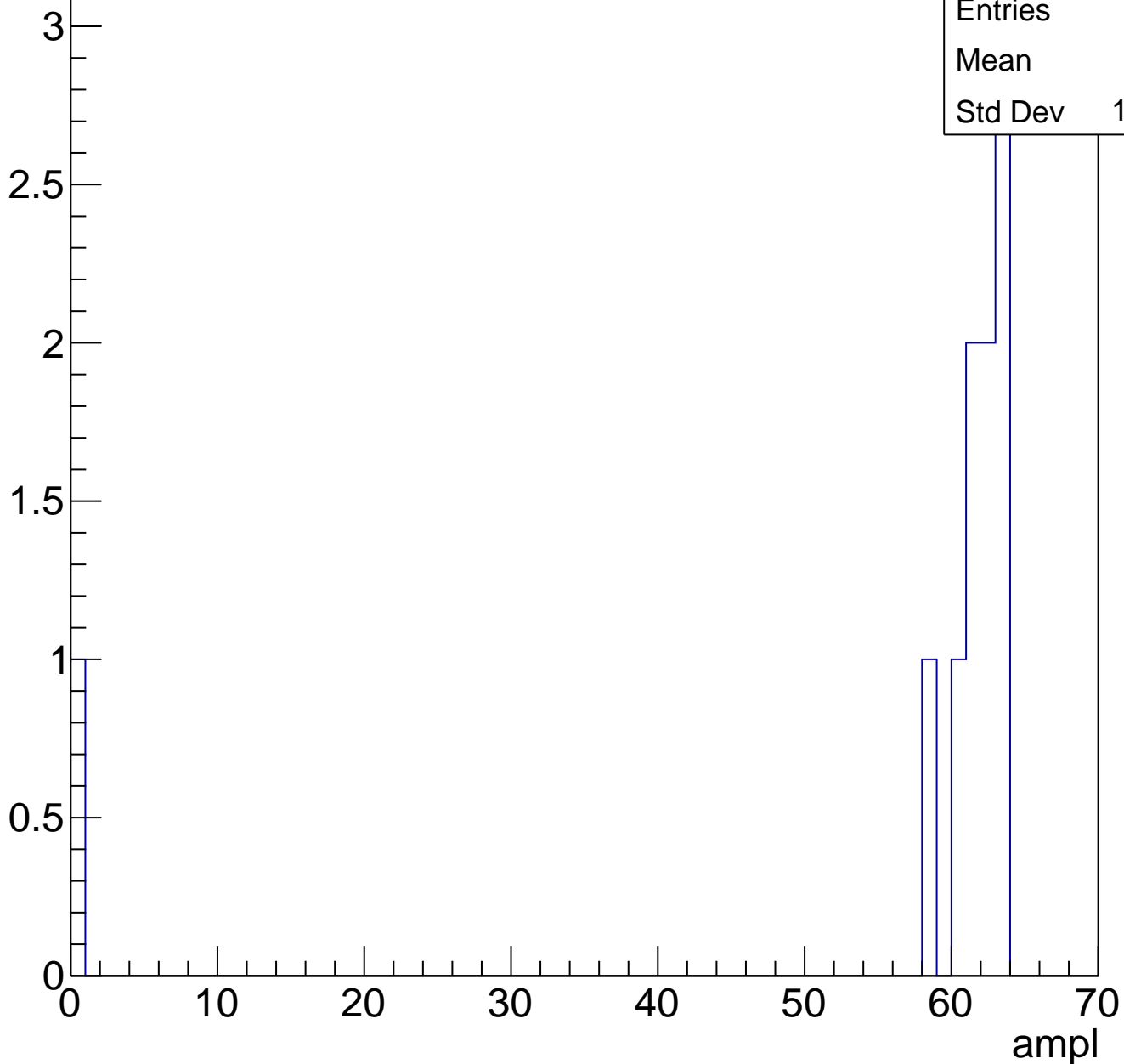
Entries	47
Mean	59.34
Std Dev	2.991



# B1L102S, U3-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

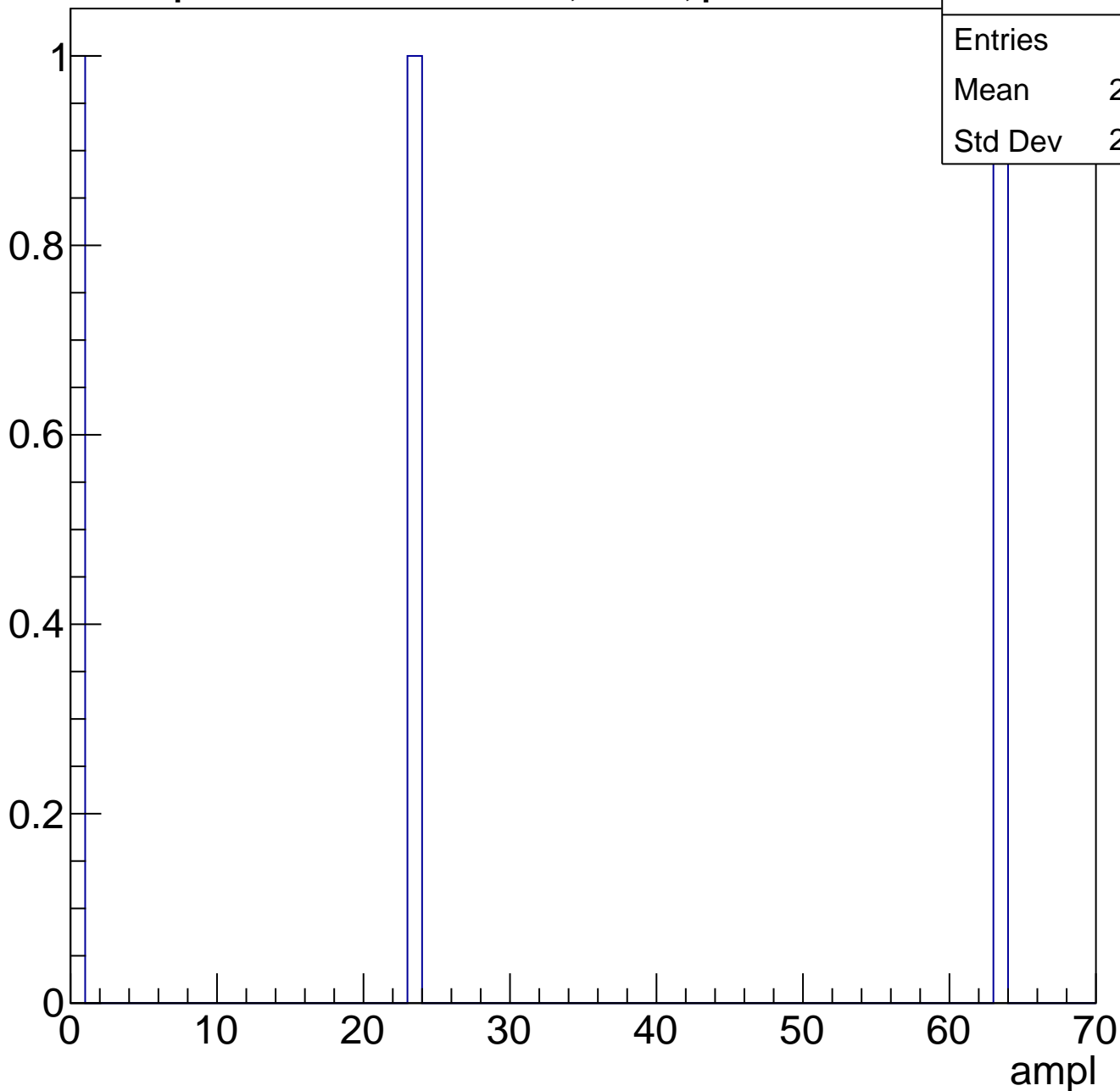




# B1L102S, U3-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	28.67
Std Dev	26.03

# B1L102S, U3-ch104, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	66
Mean	26.56
Std Dev	5.716

**Gaus mean : 27.9274**

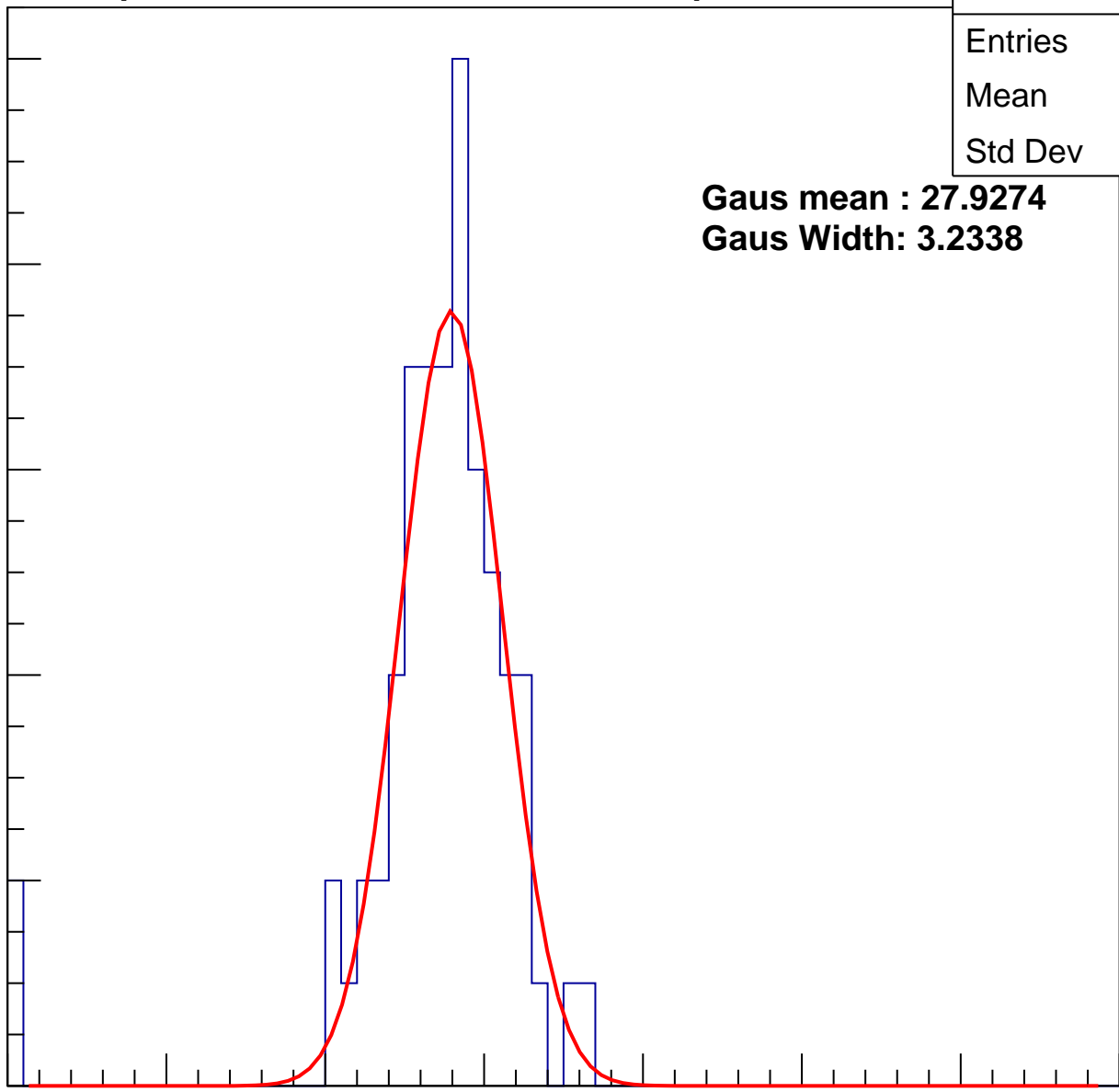
**Gaus Width: 3.2338**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U3-ch104, adc1

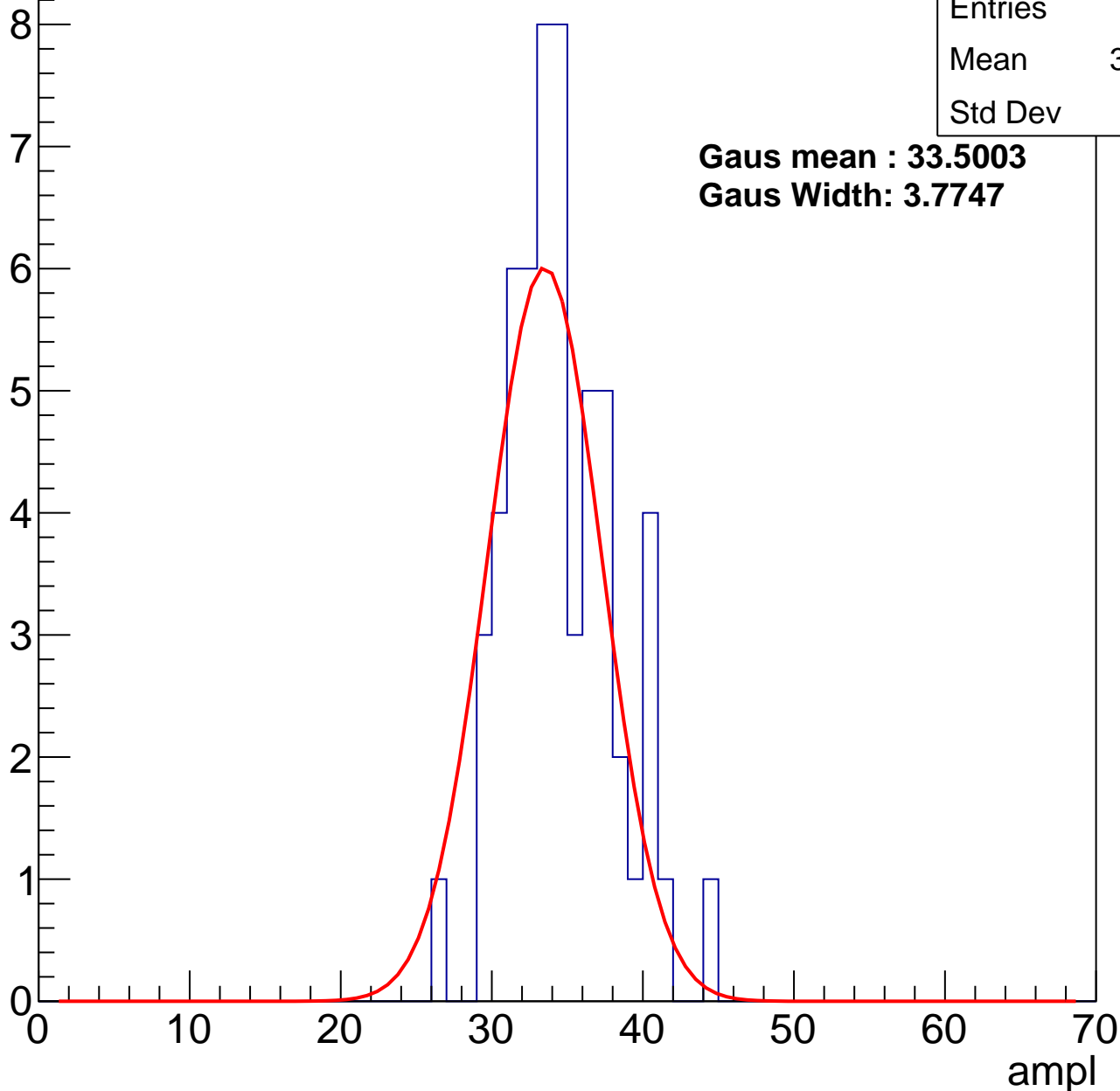
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	34.09
Std Dev	3.49

**Gaus mean : 33.5003**

**Gaus Width: 3.7747**



# B1L102S, U3-ch104, adc2

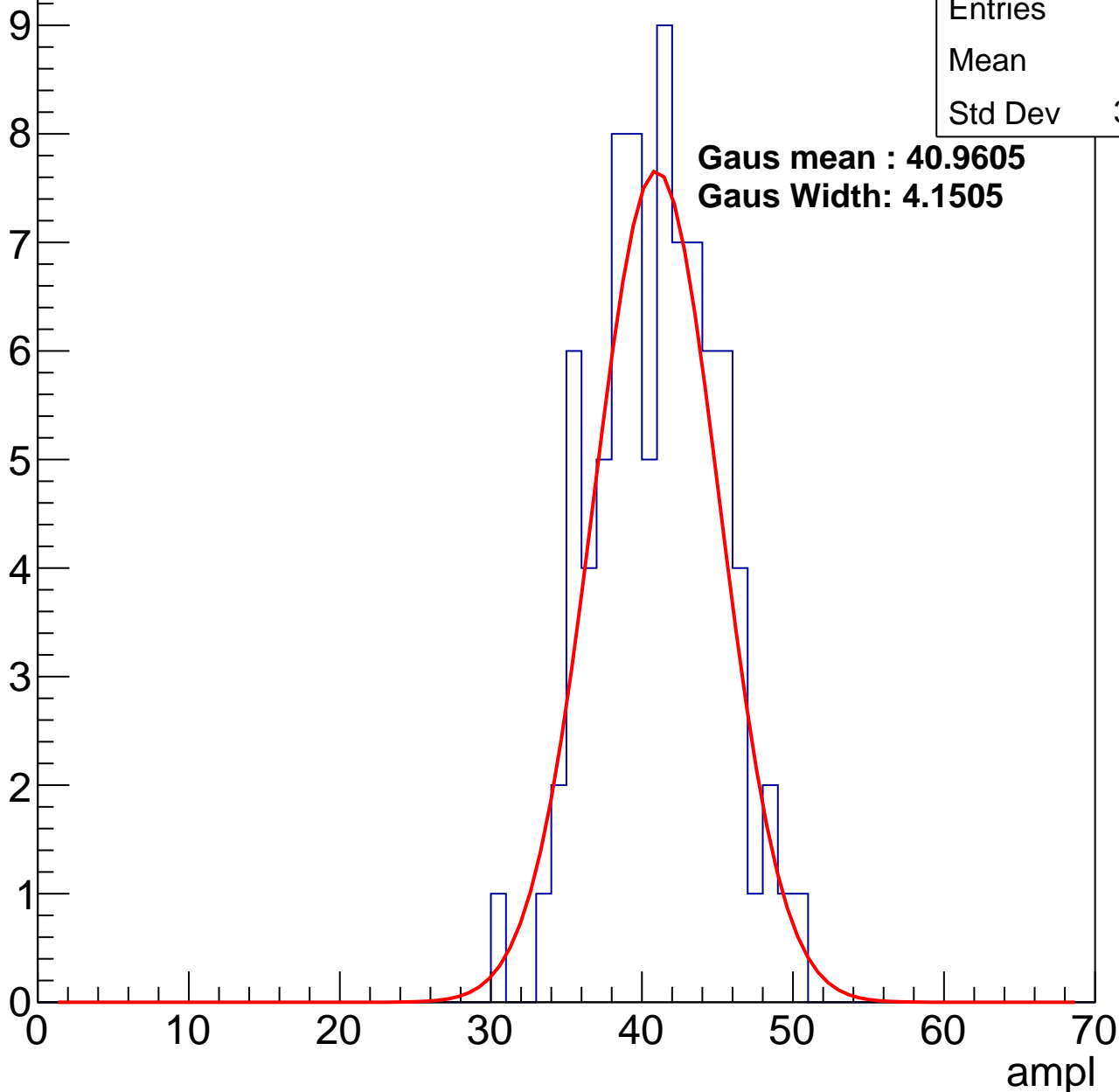
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	40.6
Std Dev	3.991

**Gaus mean : 40.9605**

**Gaus Width: 4.1505**

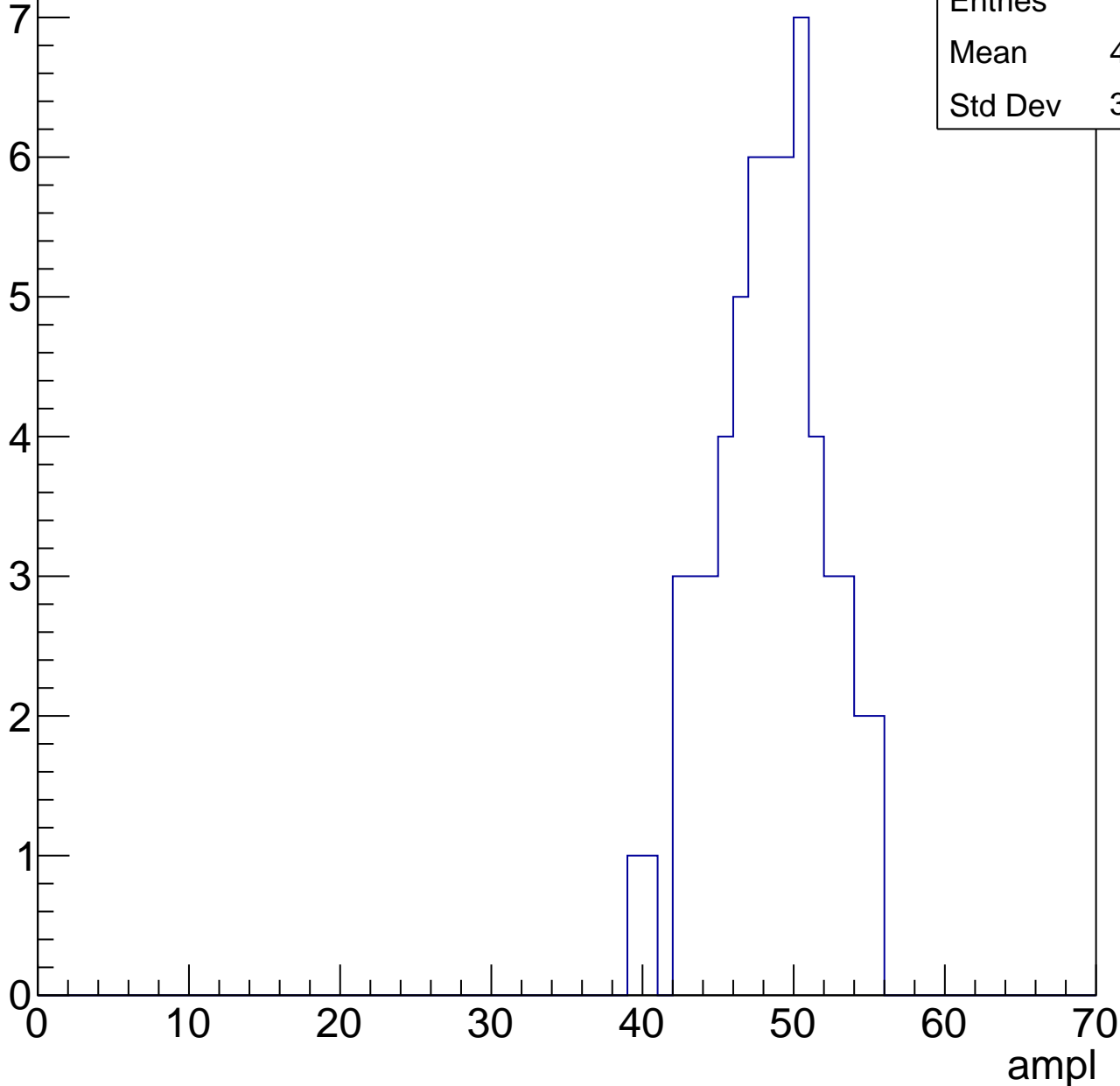


# B1L102S, U3-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	47.92
Std Dev	3.684

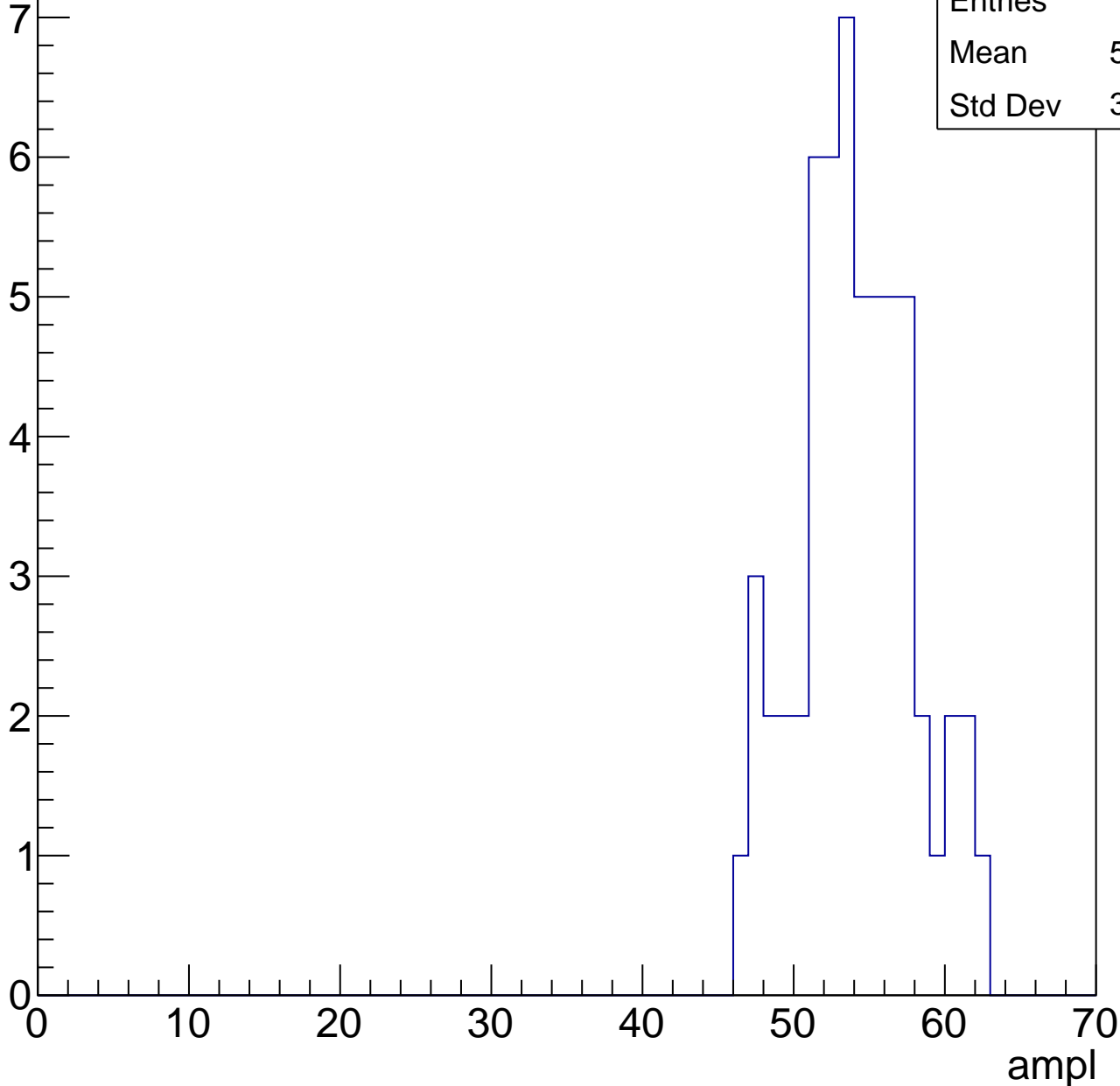


# B1L102S, U3-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	53.67
Std Dev	3.757

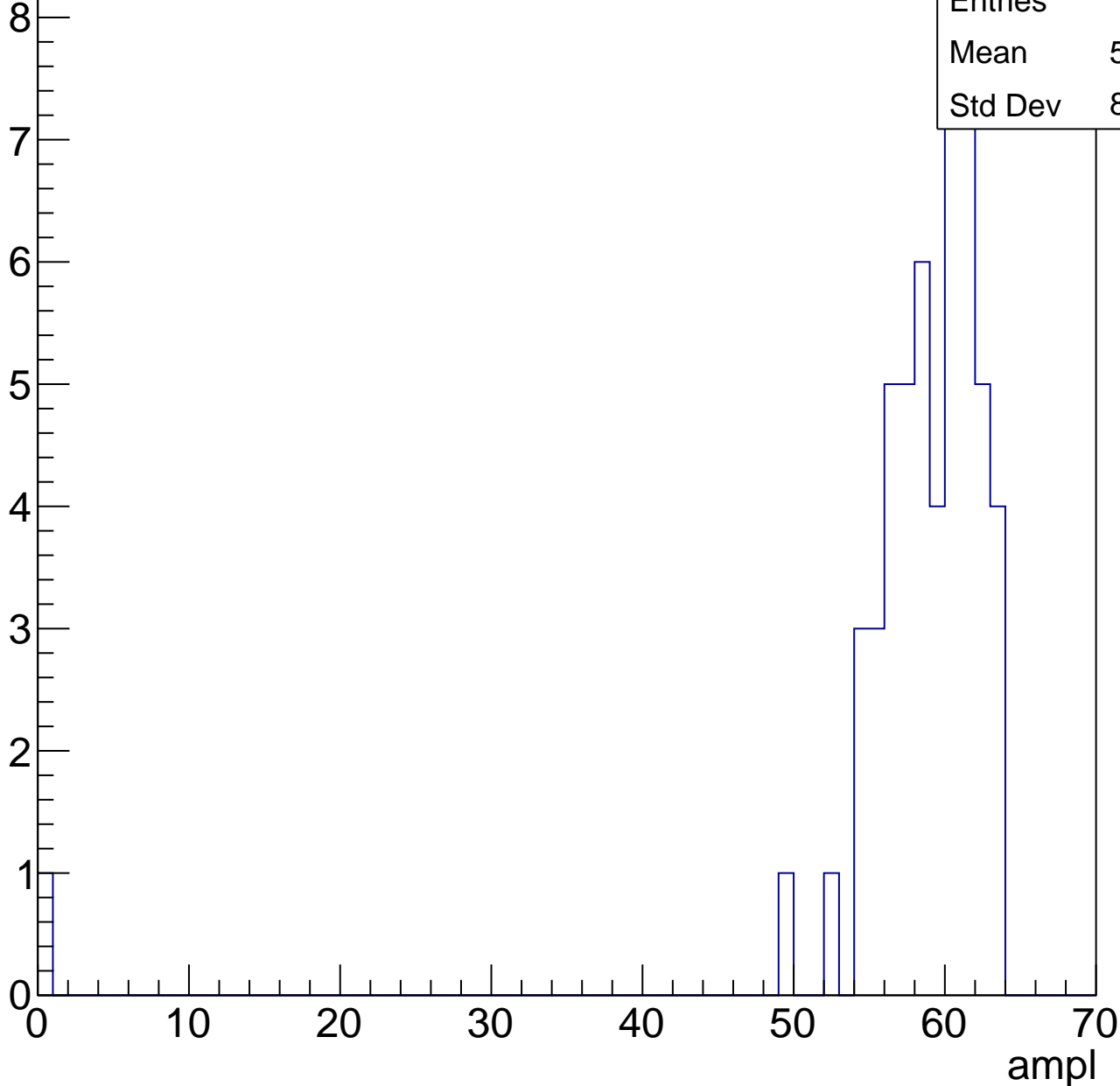


# B1L102S, U3-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	57.54
Std Dev	8.452

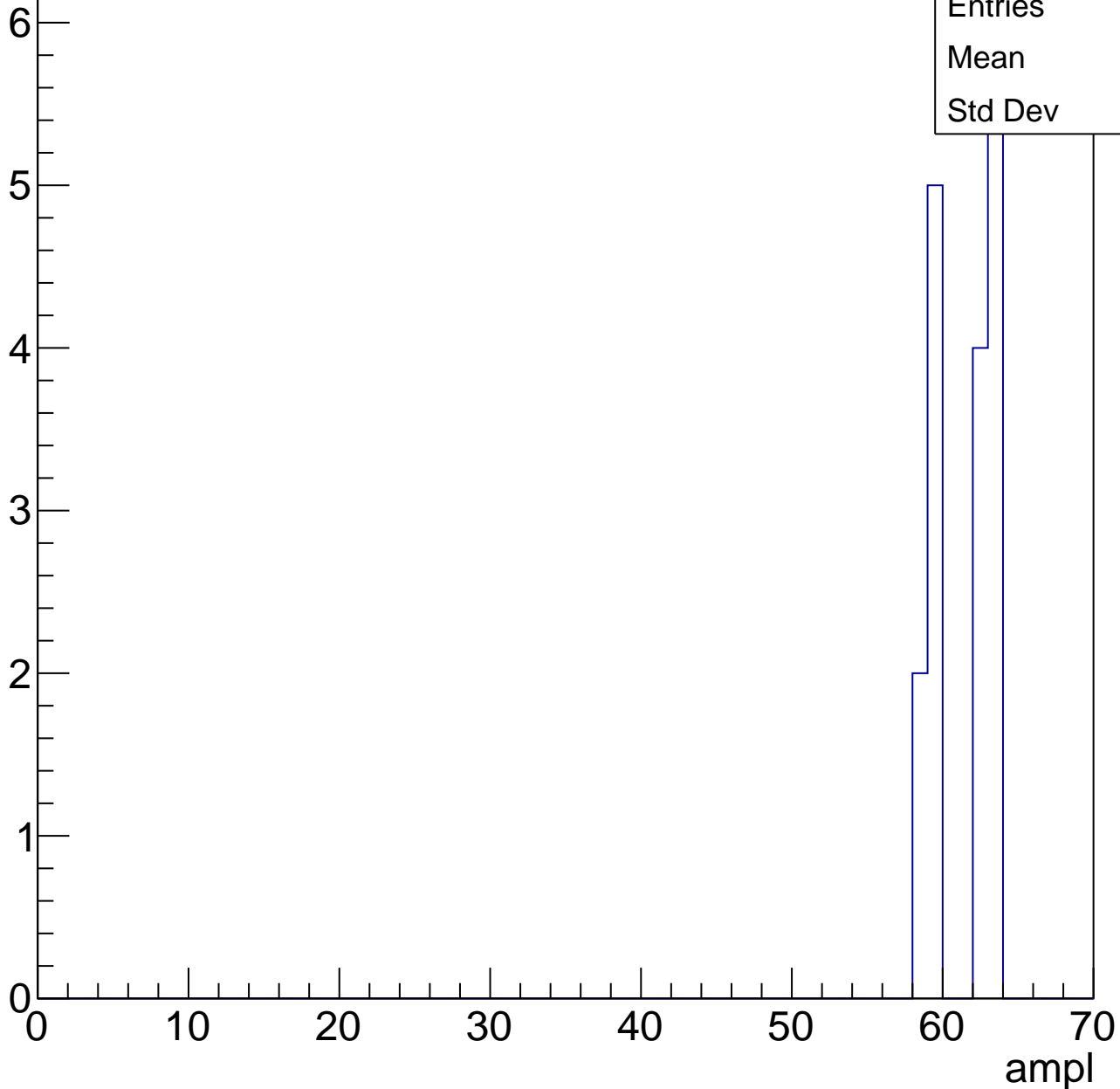


# B1L102S, U3-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	17
Mean	61
Std Dev	1.97





# B1L102S, U3-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch105, adc0

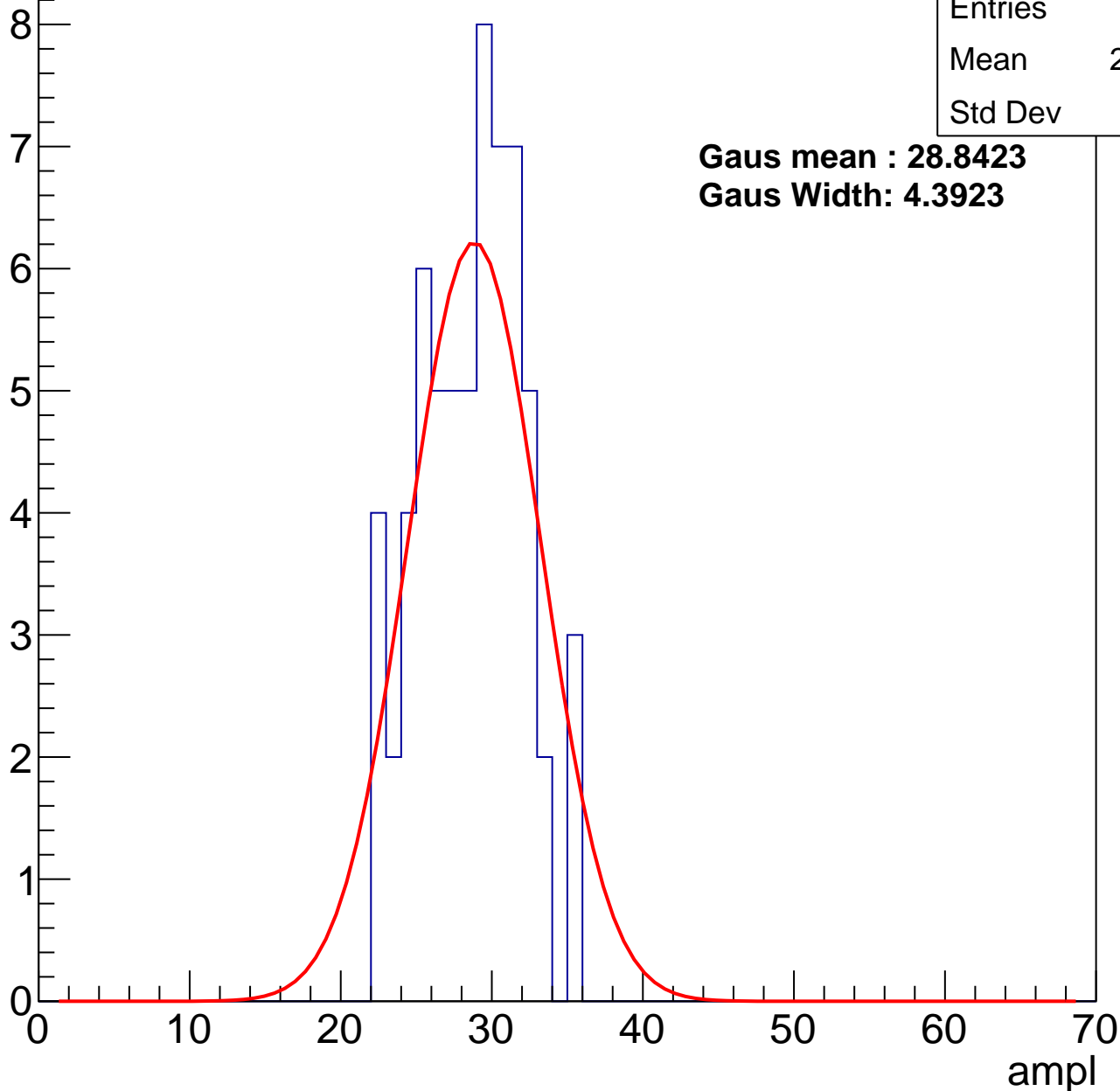
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	28.17
Std Dev	3.36

**Gaus mean : 28.8423**

**Gaus Width: 4.3923**



# B1L102S, U3-ch105, adc1

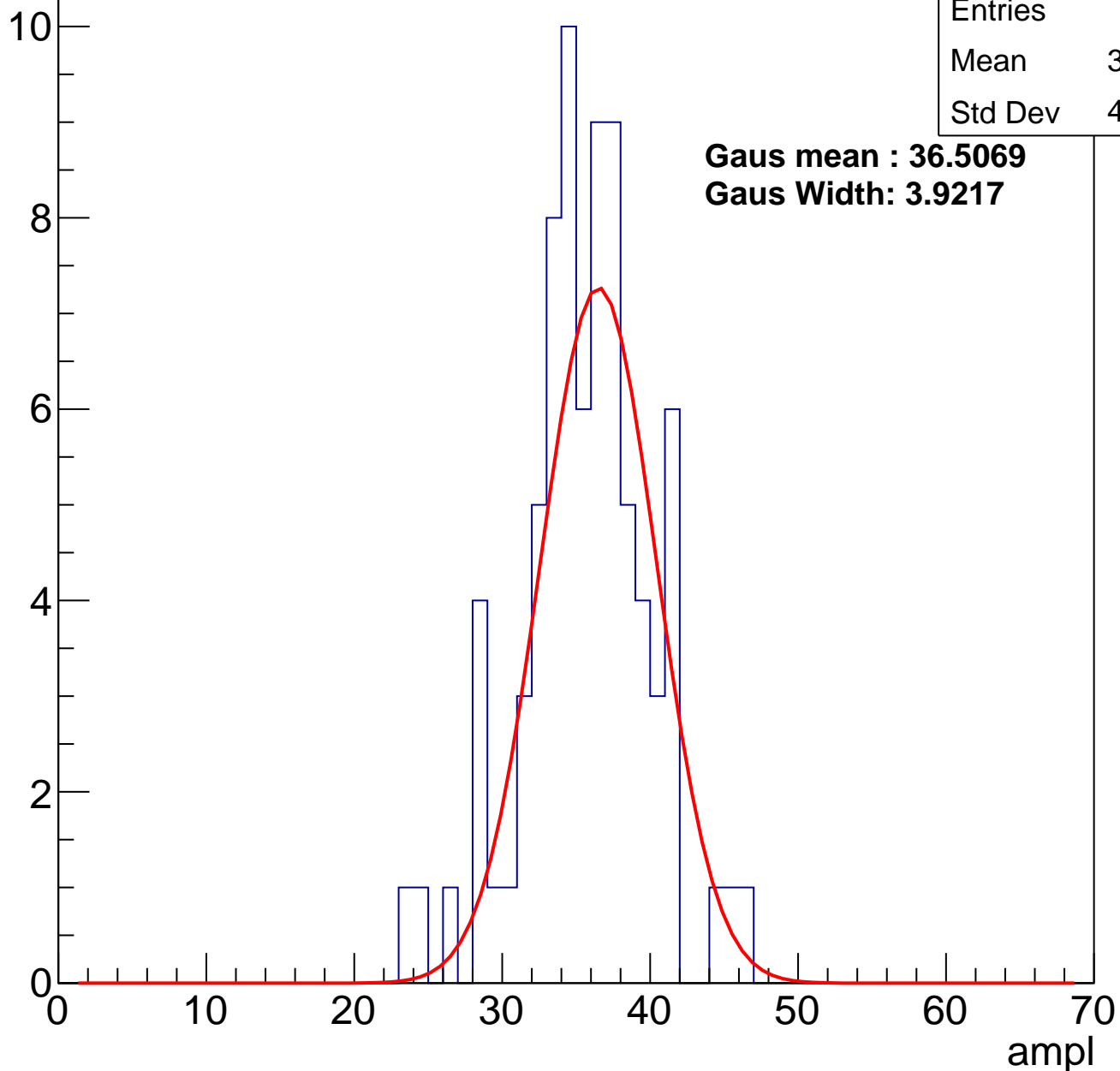
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	80
Mean	35.19
Std Dev	4.304

**Gaus mean : 36.5069**

**Gaus Width: 3.9217**

Entry



# B1L102S, U3-ch105, adc2

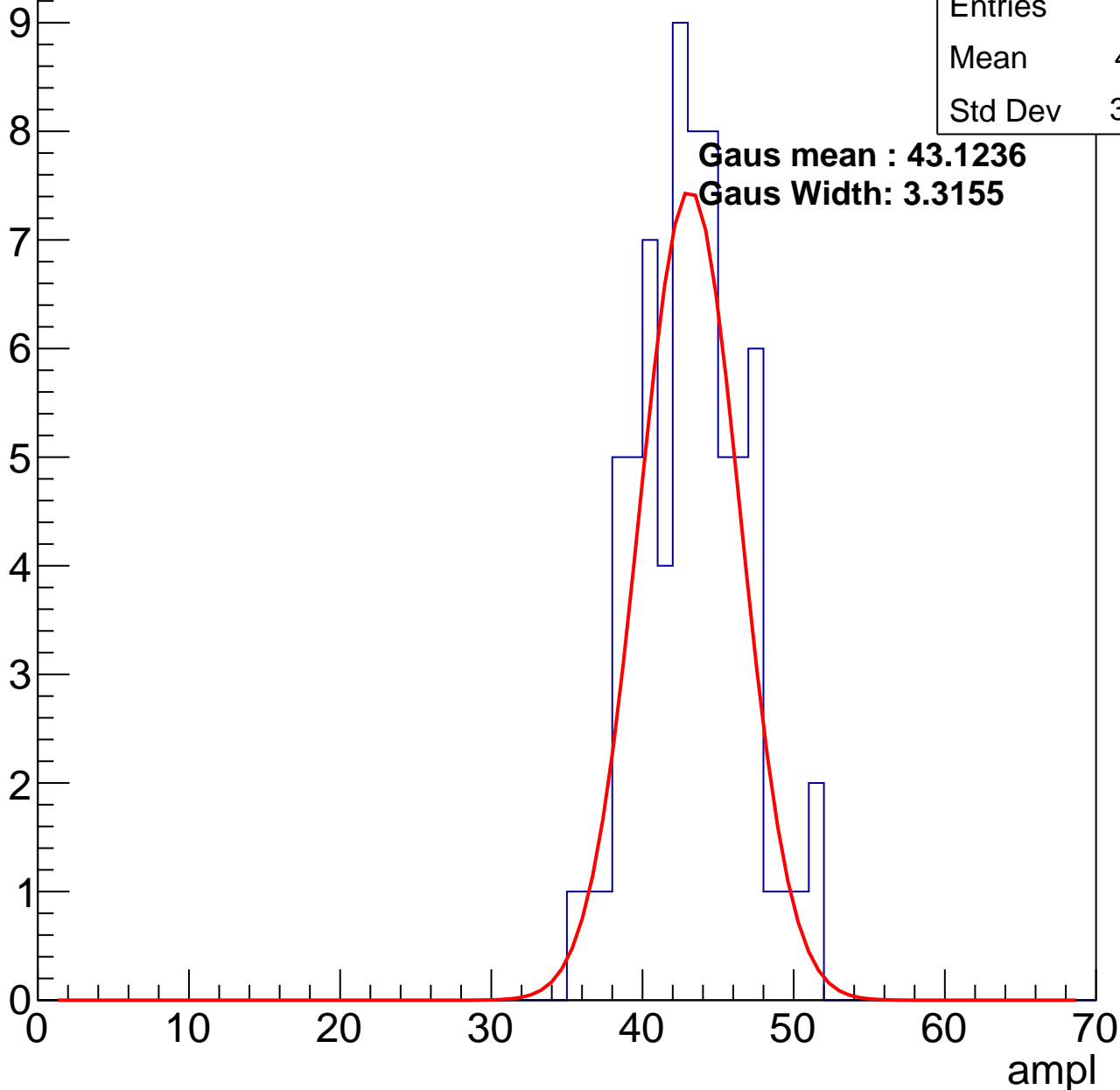
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	42.81
Std Dev	3.478

**Gaus mean : 43.1236**

**Gaus Width: 3.3155**

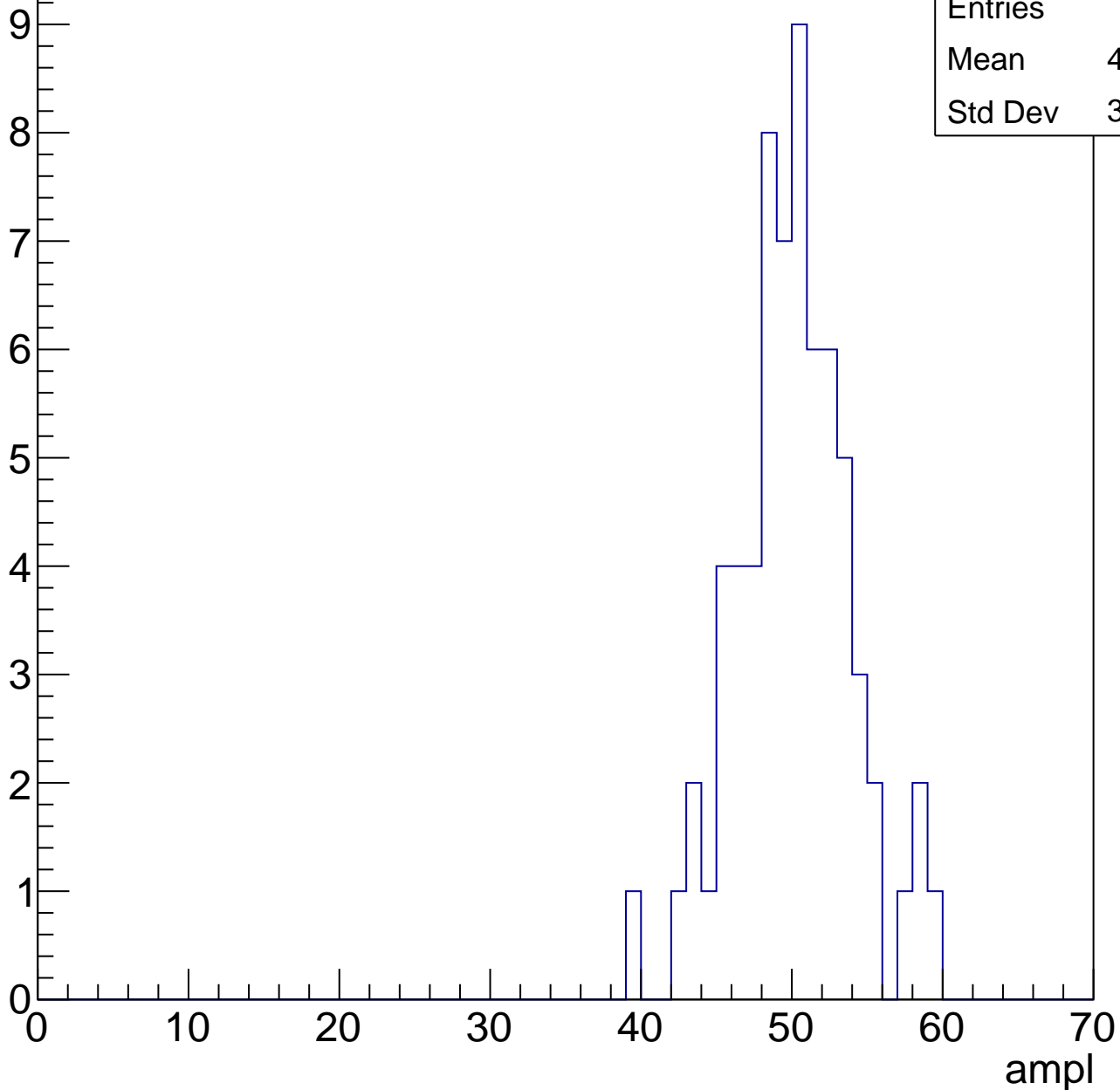


# B1L102S, U3-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	49.66
Std Dev	3.827

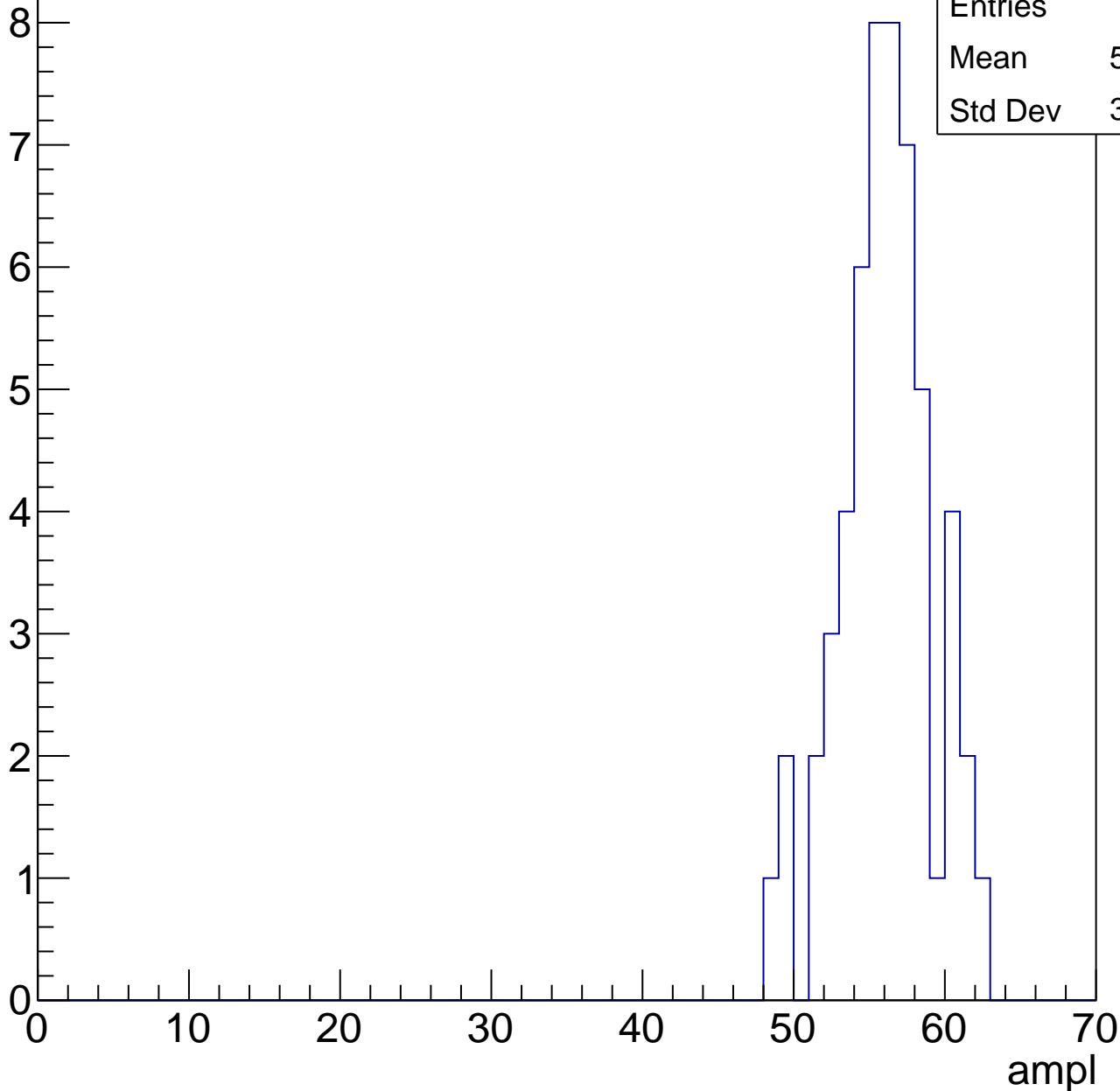


# B1L102S, U3-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	55.56
Std Dev	3.053

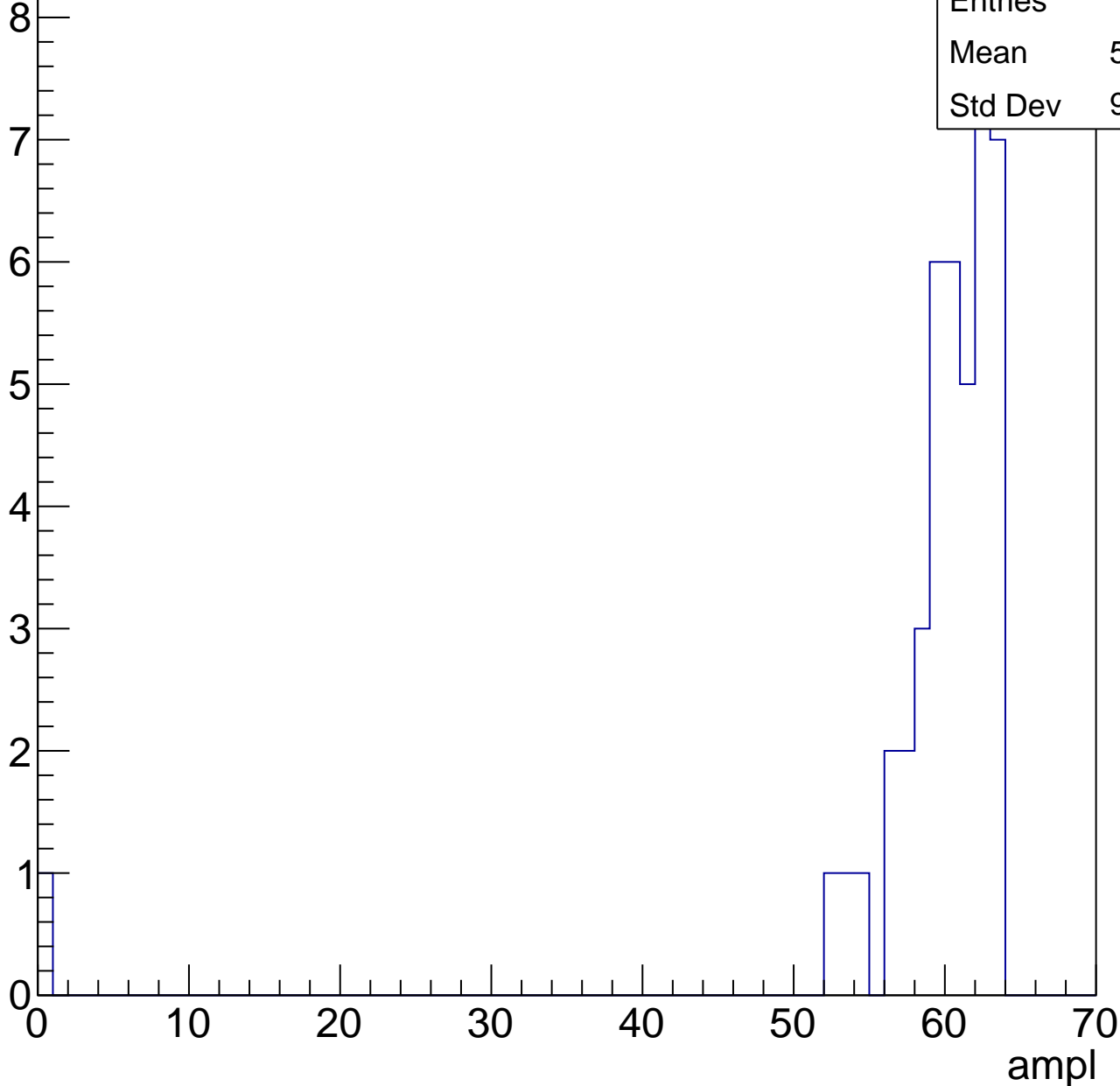


# B1L102S, U3-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

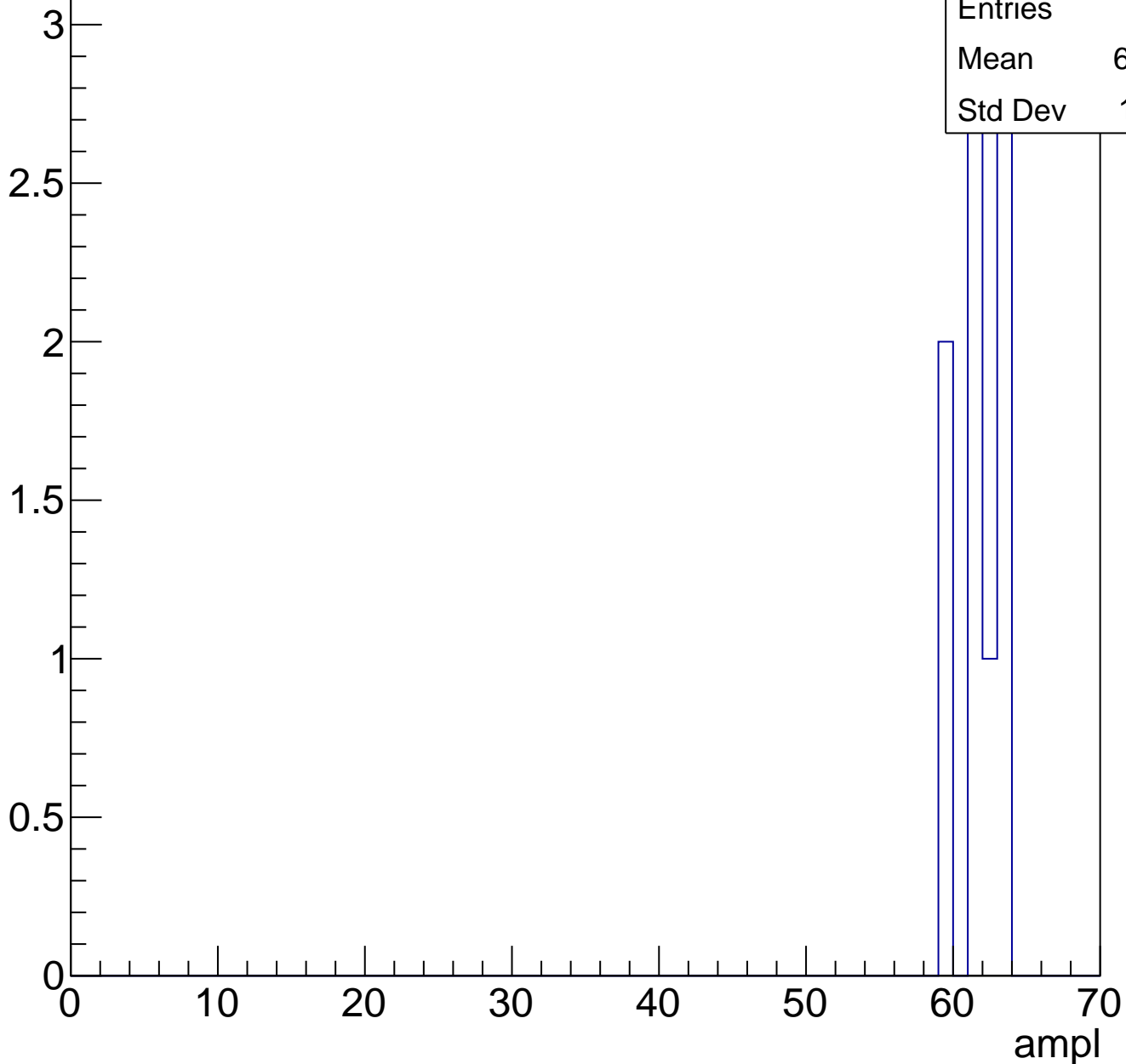
Entries	43
Mean	58.49
Std Dev	9.424



# B1L102S, U3-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U3-ch106, adc0

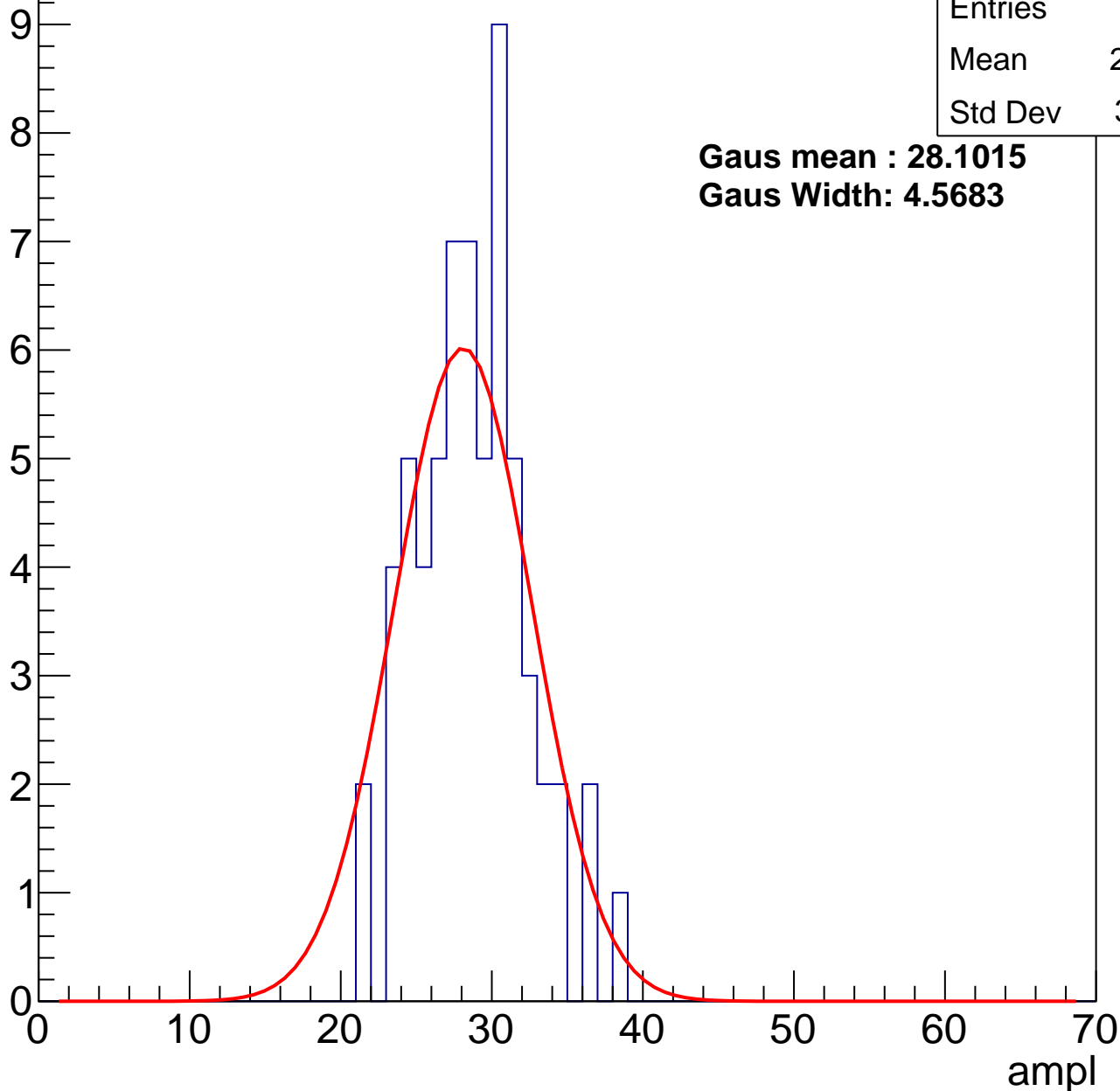
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	28.24
Std Dev	3.611

**Gaus mean : 28.1015**

**Gaus Width: 4.5683**



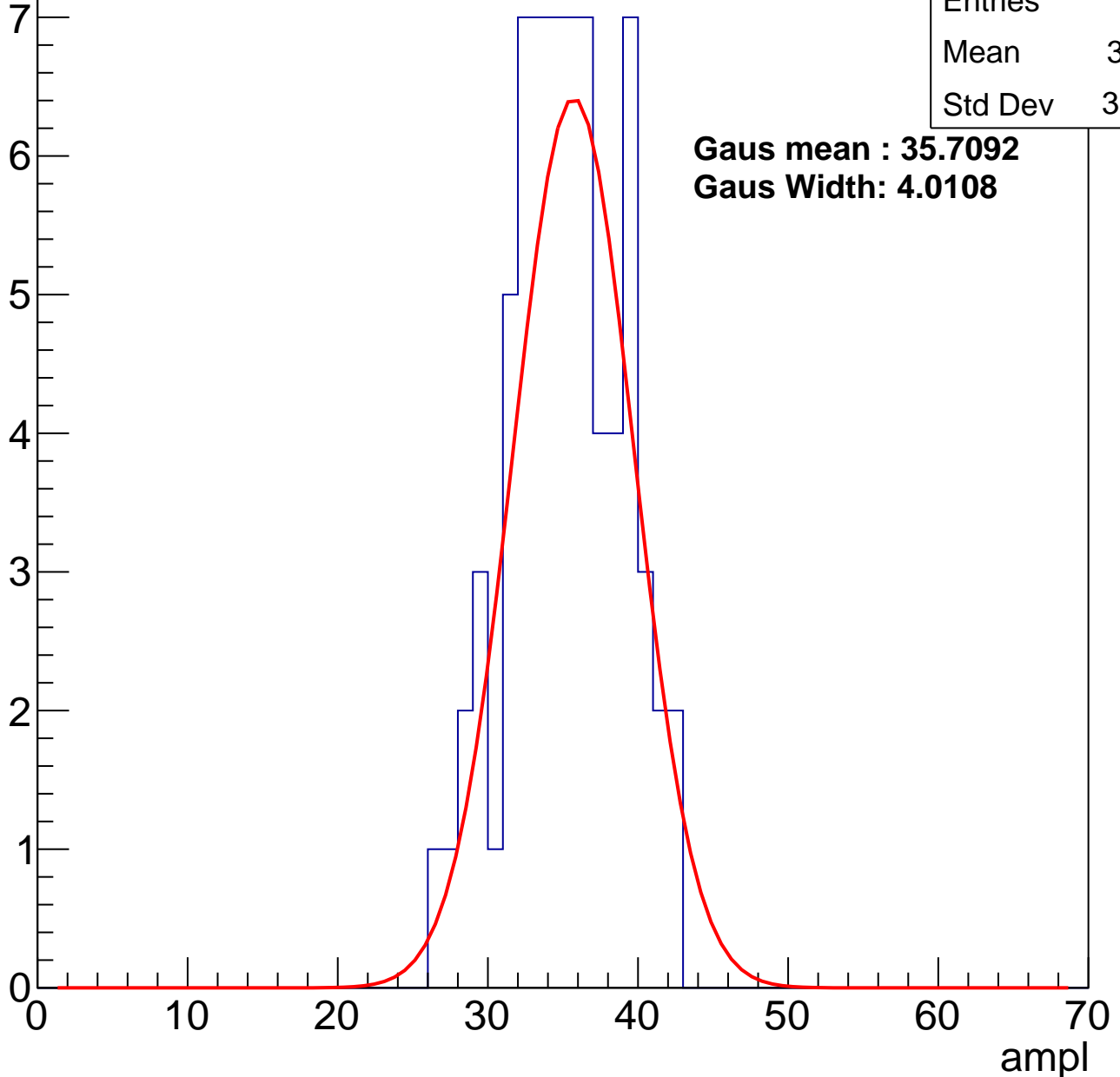
# B1L102S, U3-ch106, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	34.71
Std Dev	3.712

**Gaus mean : 35.7092**  
**Gaus Width: 4.0108**

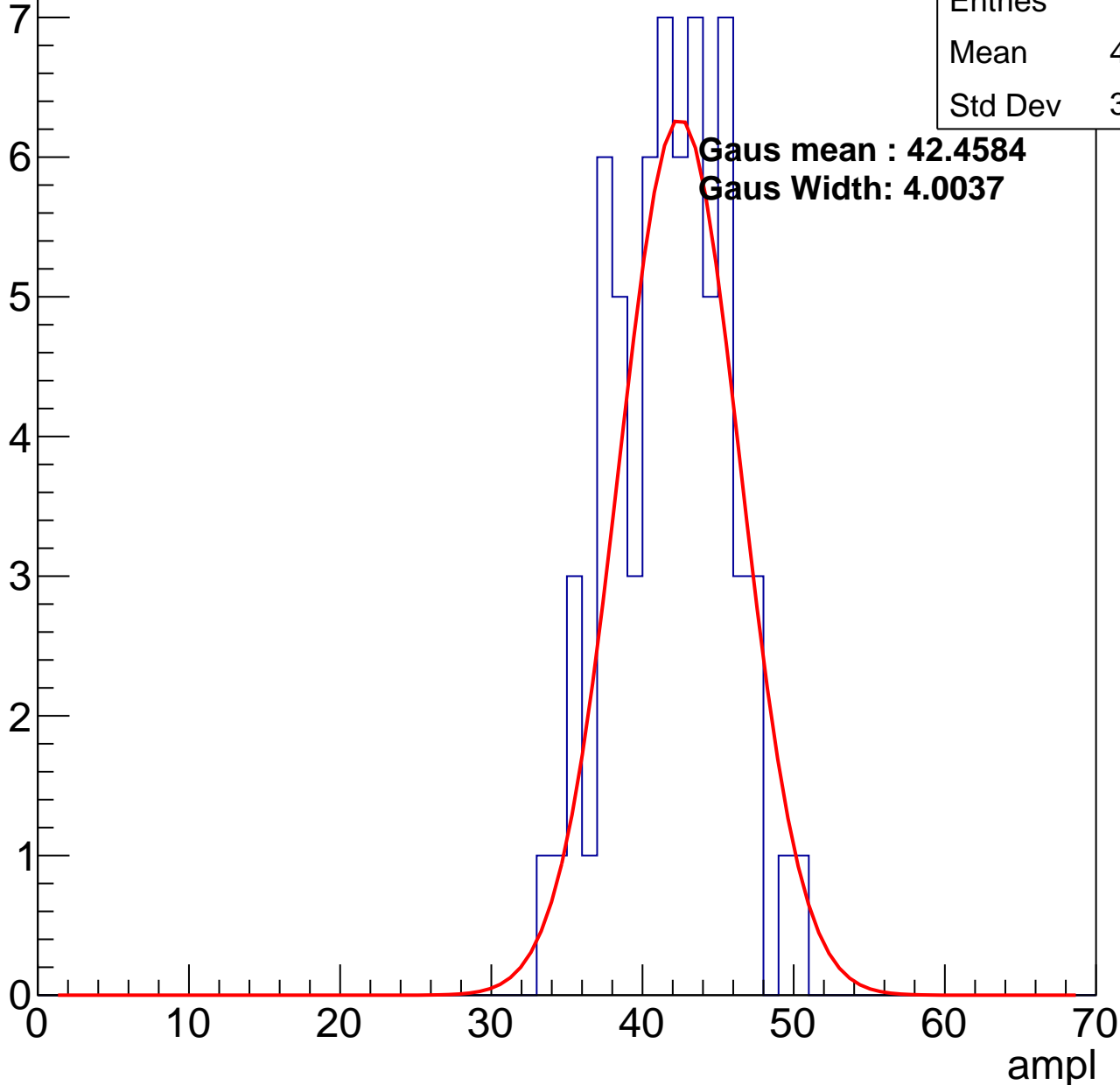


# B1L102S, U3-ch106, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	41.36
Std Dev	3.724

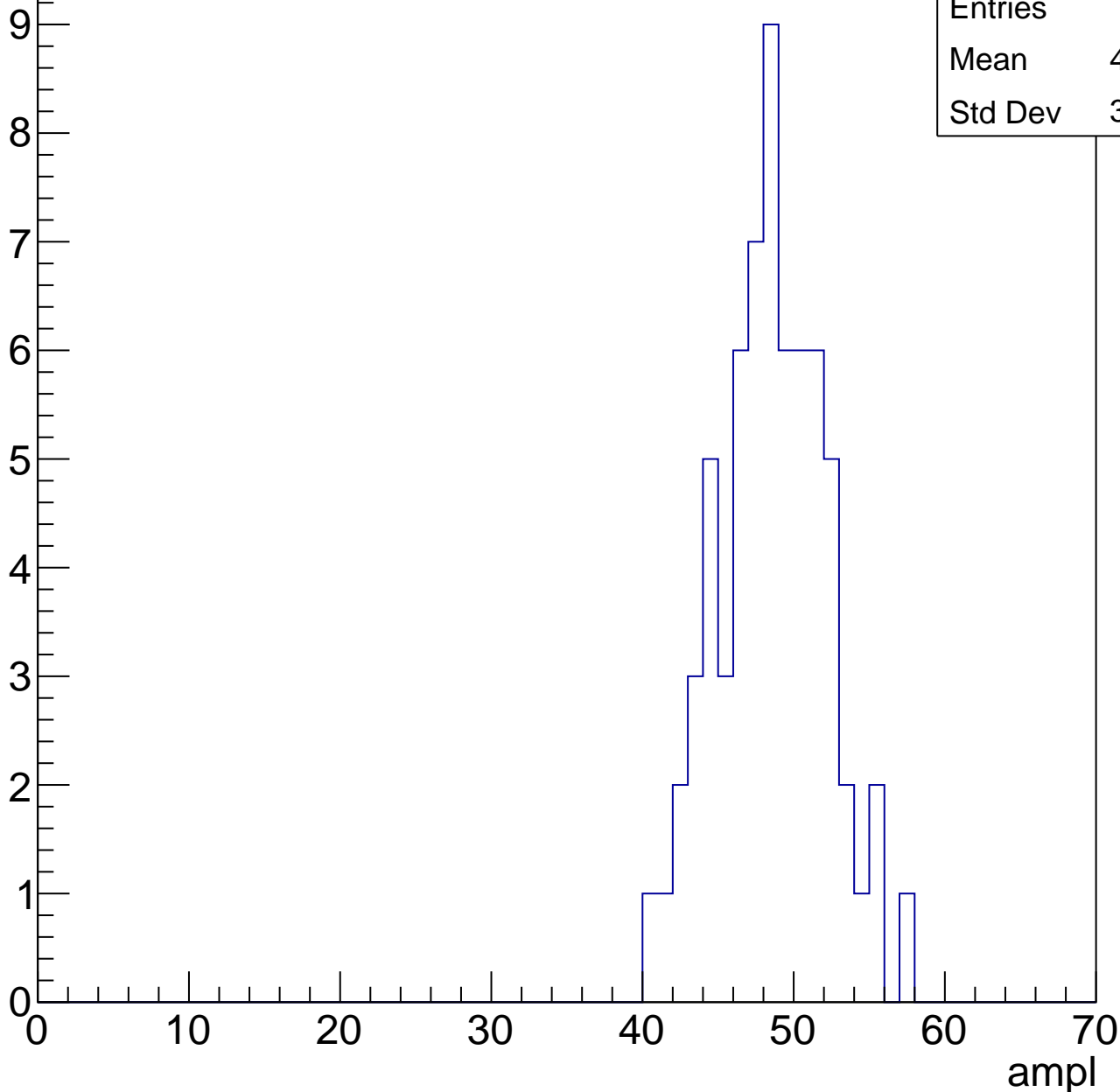


# B1L102S, U3-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	48.08
Std Dev	3.539

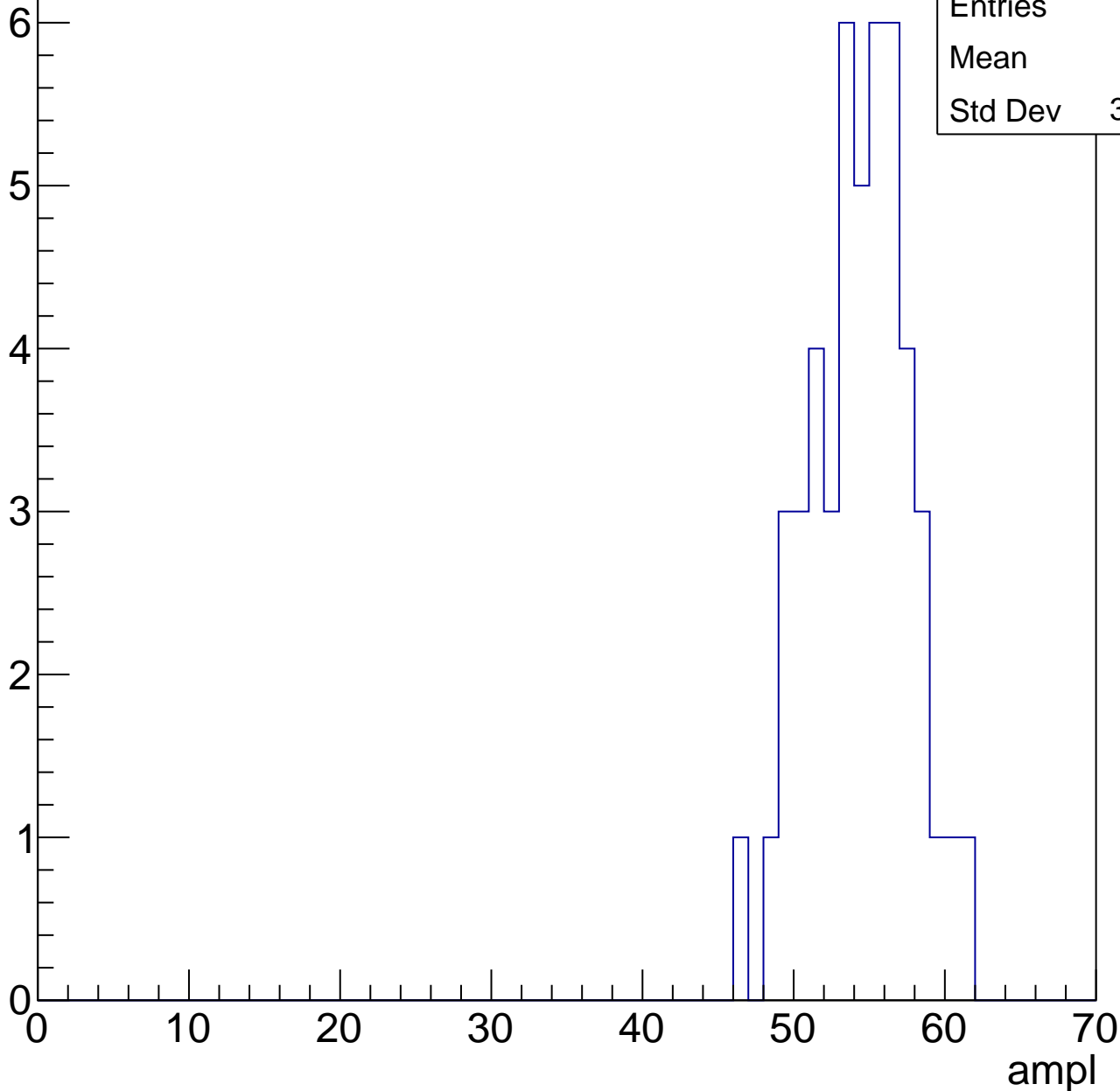


# B1L102S, U3-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

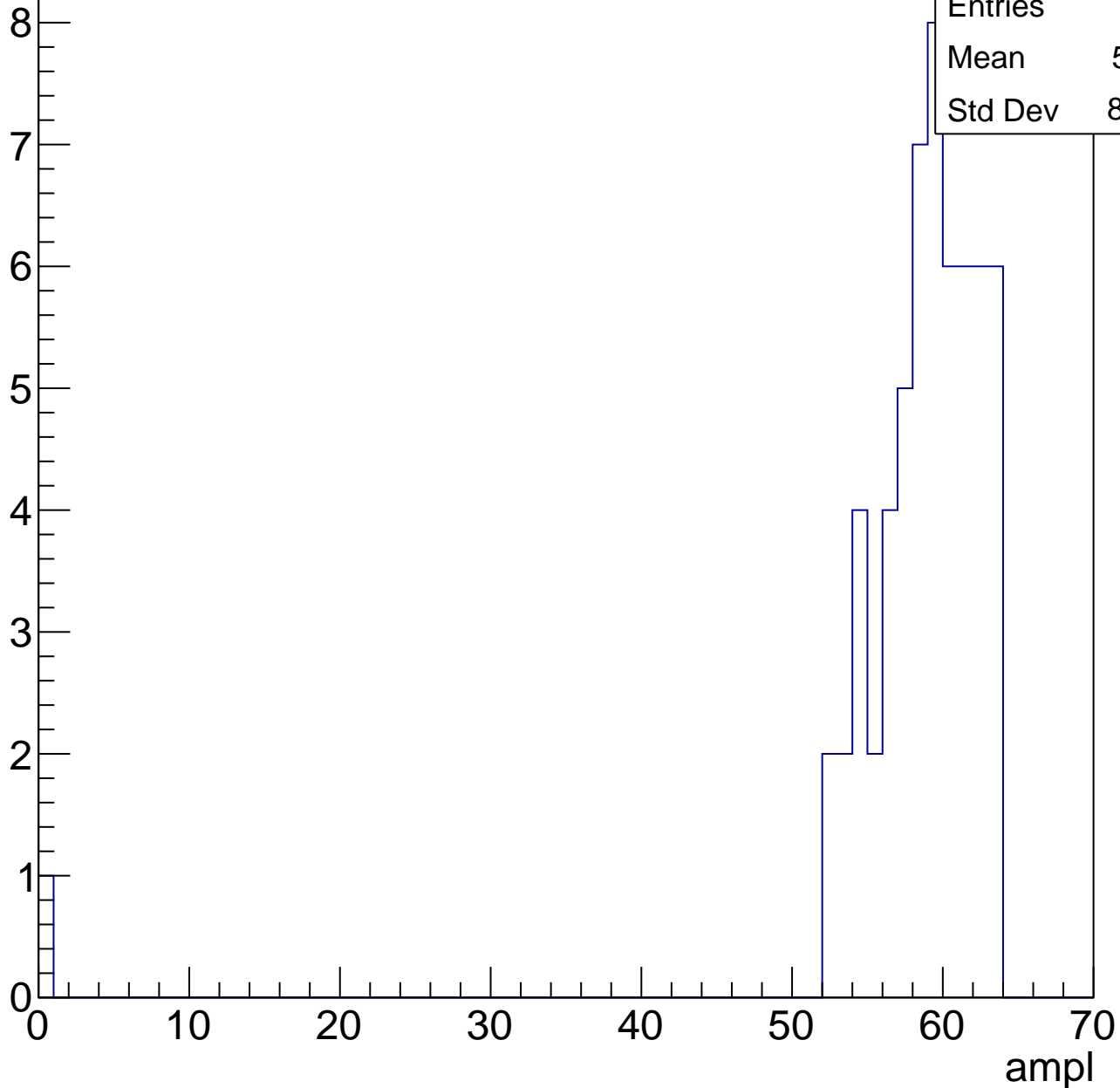
Entries	48
Mean	53.9
Std Dev	3.229



# B1L102S, U3-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

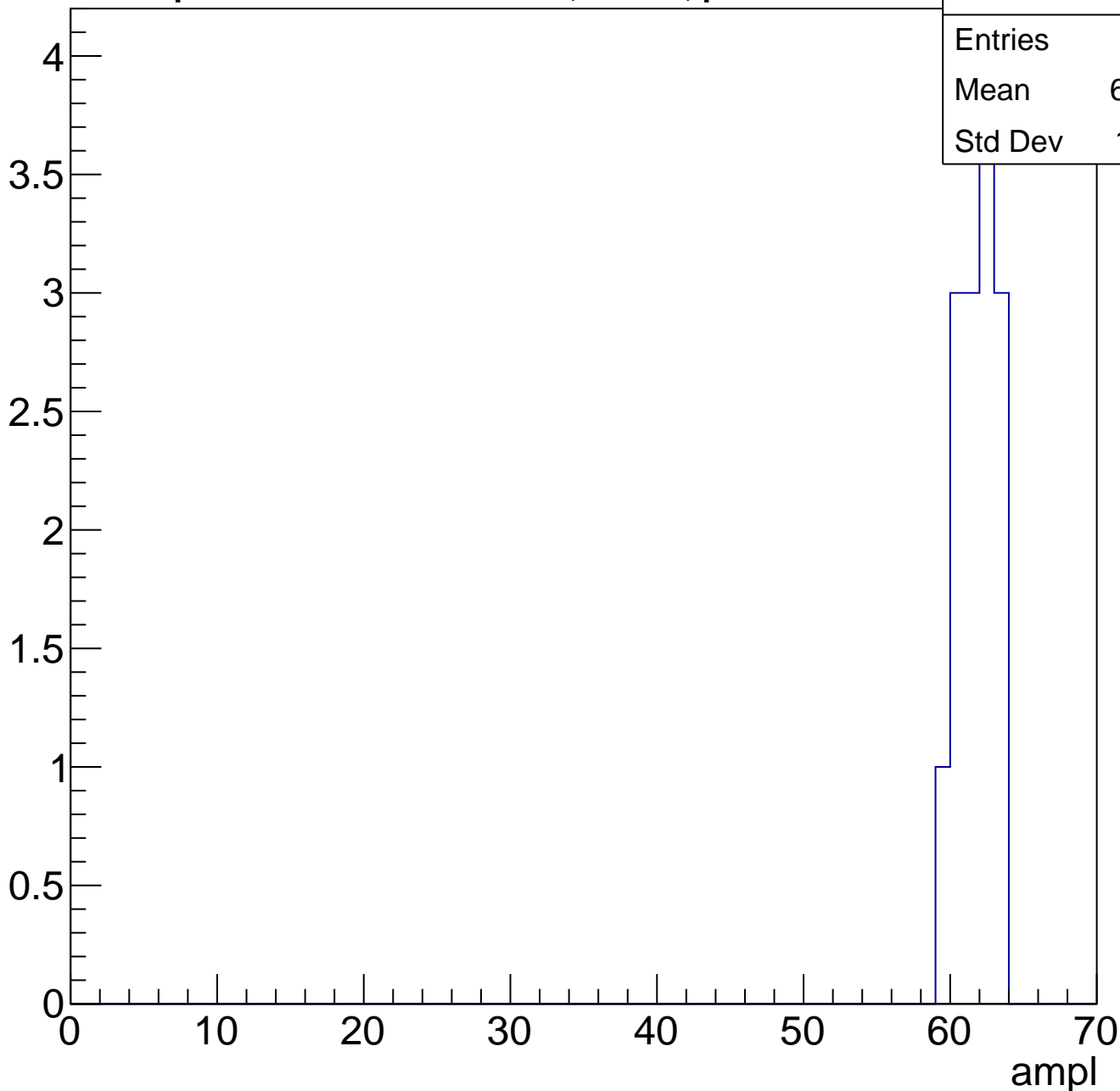
Entry



# B1L102S, U3-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

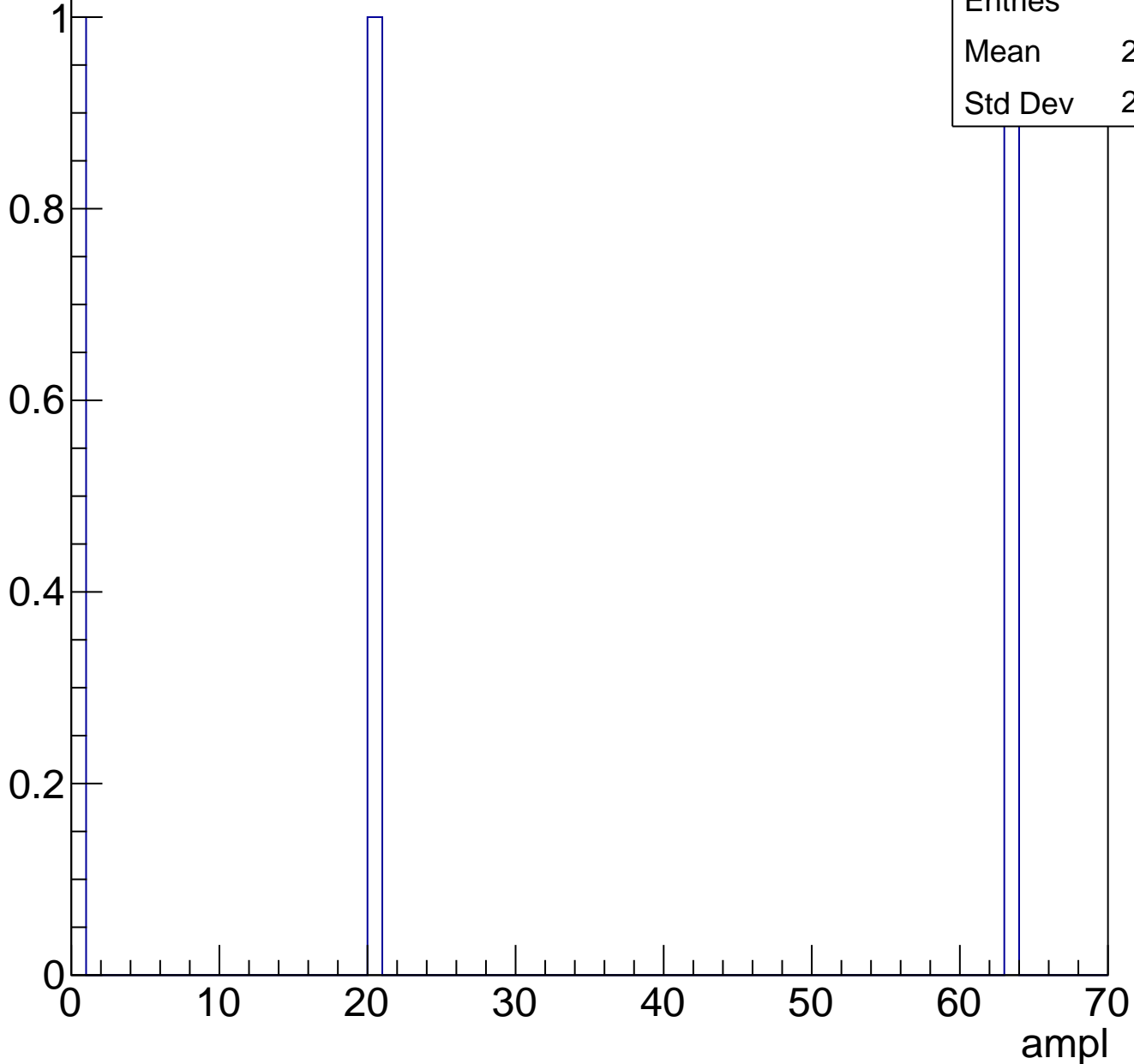




# B1L102S, U3-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	27.67
Std Dev	26.28

# B1L102S, U3-ch107, adc0

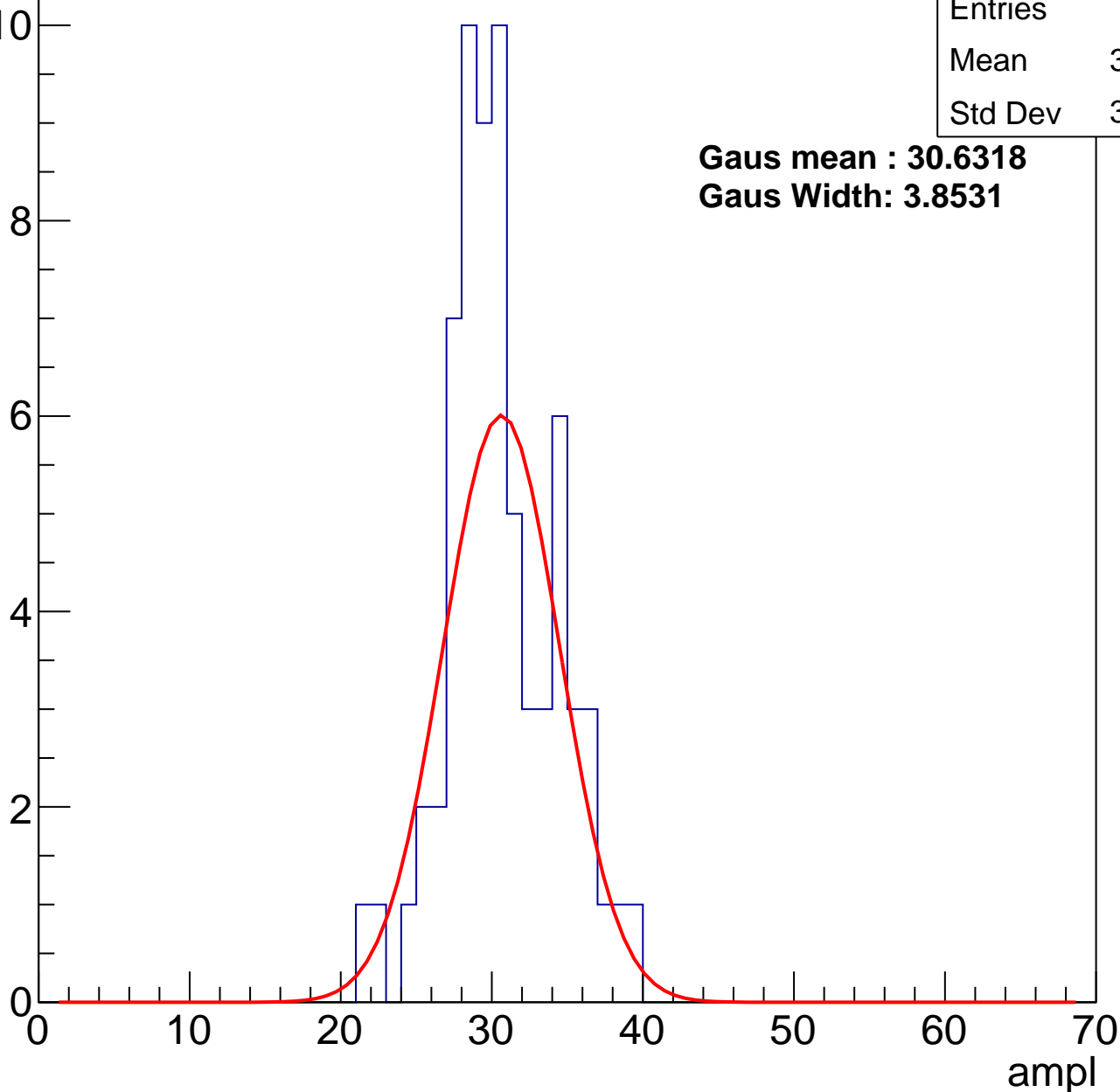
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	30.14
Std Dev	3.593

**Gaus mean : 30.6318**

**Gaus Width: 3.8531**



# B1L102S, U3-ch107, adc1

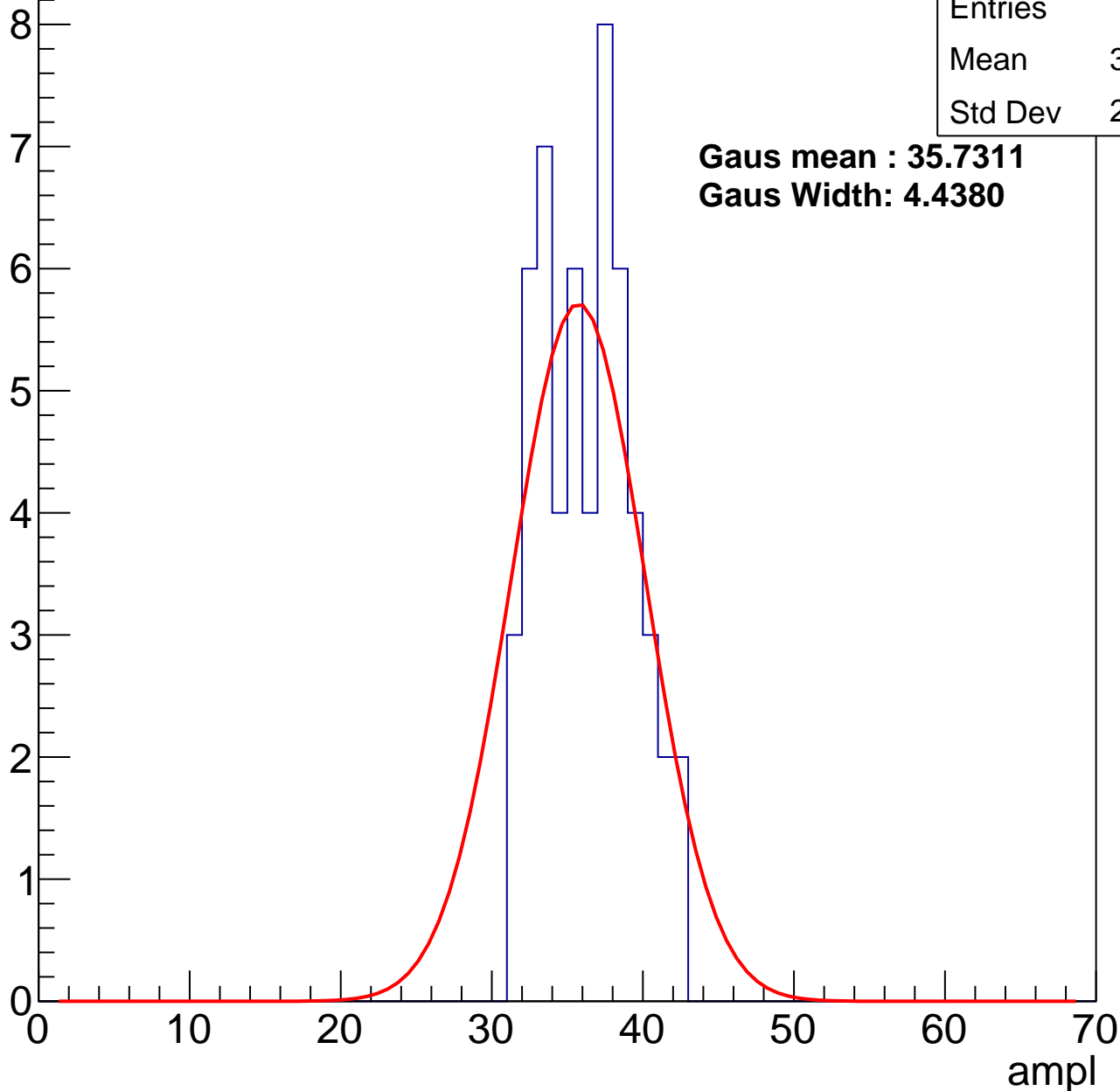
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	35.85
Std Dev	2.993

**Gaus mean : 35.7311**

**Gaus Width: 4.4380**



# B1L102S, U3-ch107, adc2

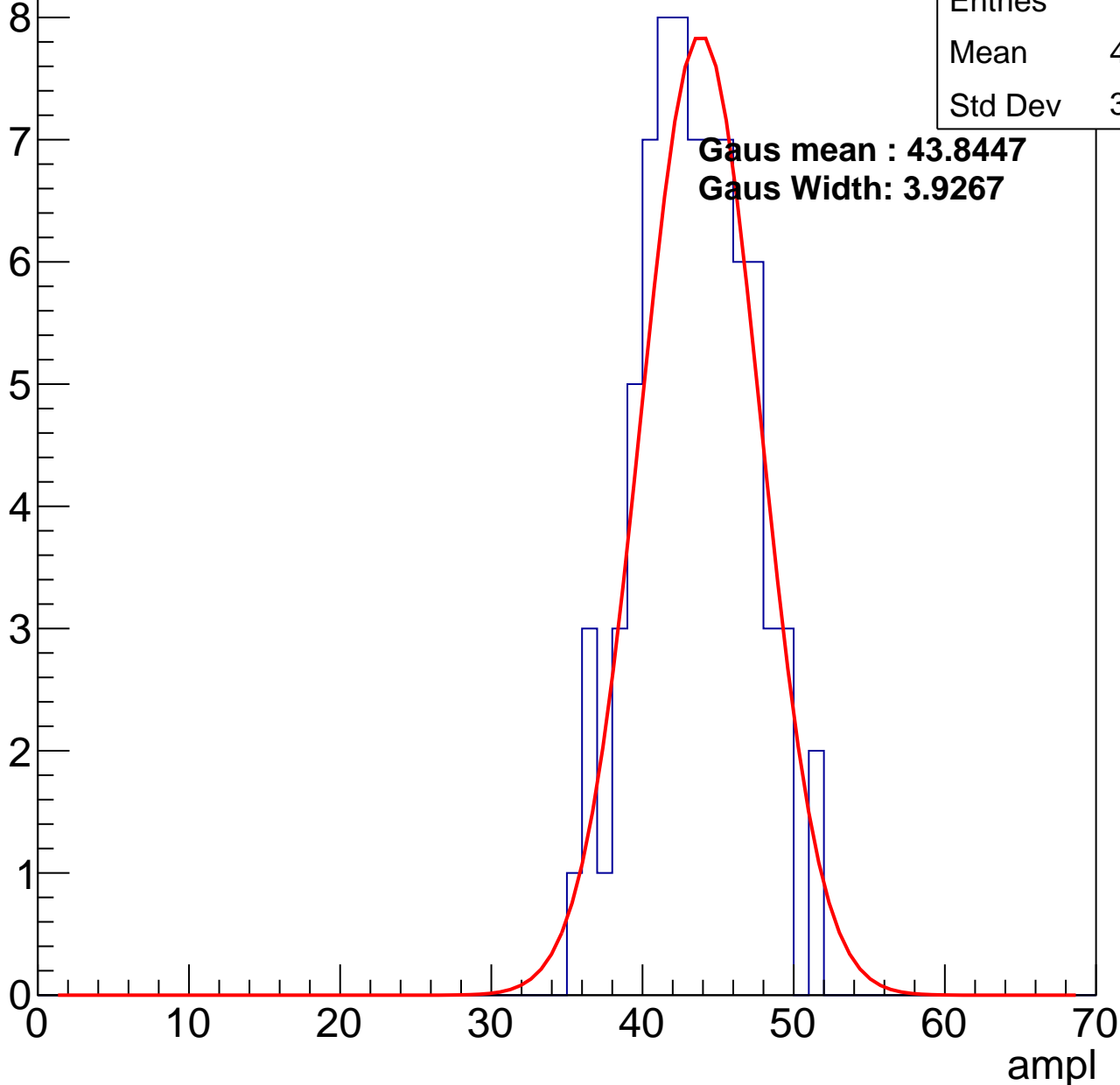
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	42.96
Std Dev	3.605

**Gaus mean : 43.8447**

**Gaus Width: 3.9267**

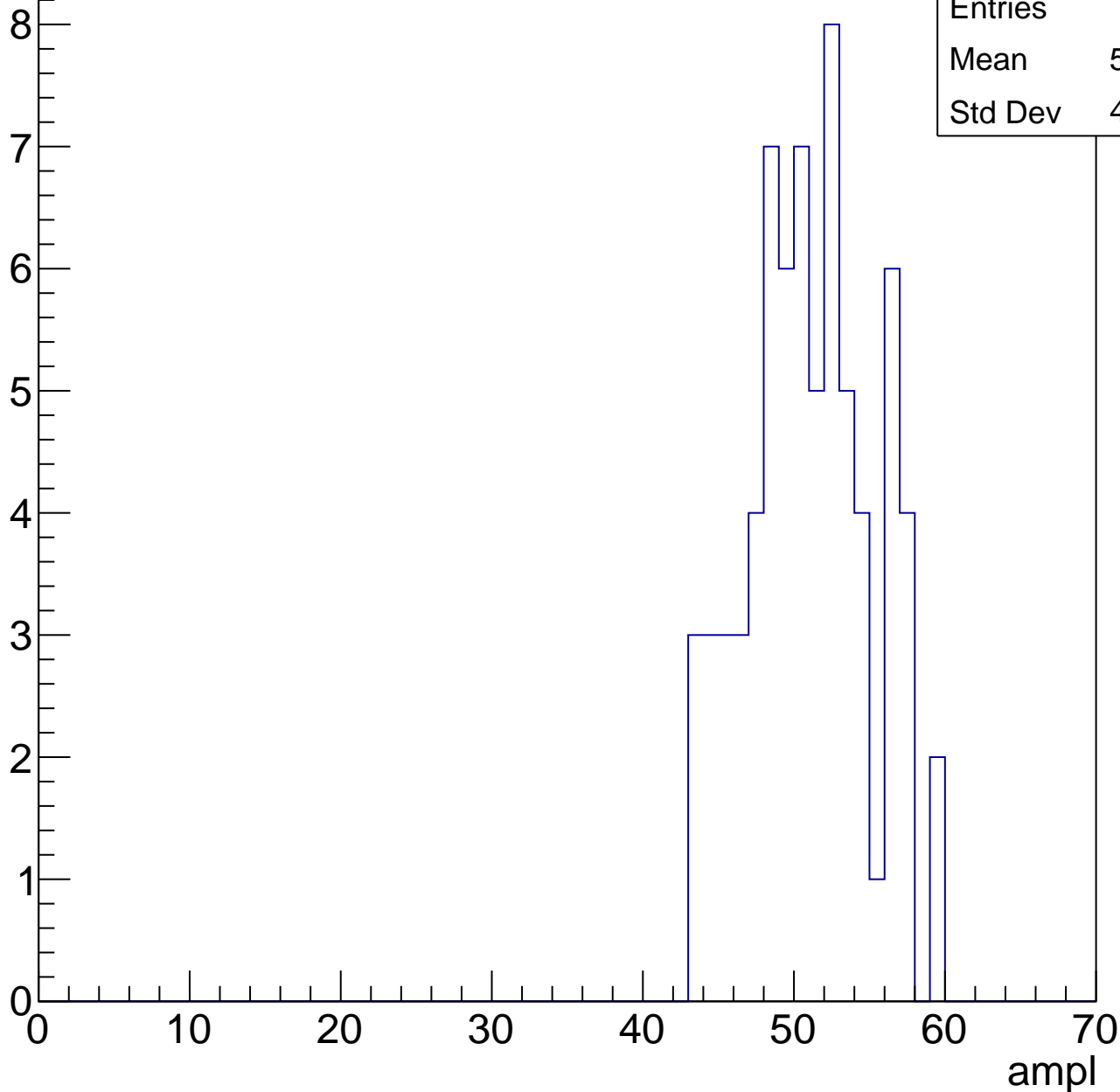


# B1L102S, U3-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	50.58
Std Dev	4.058

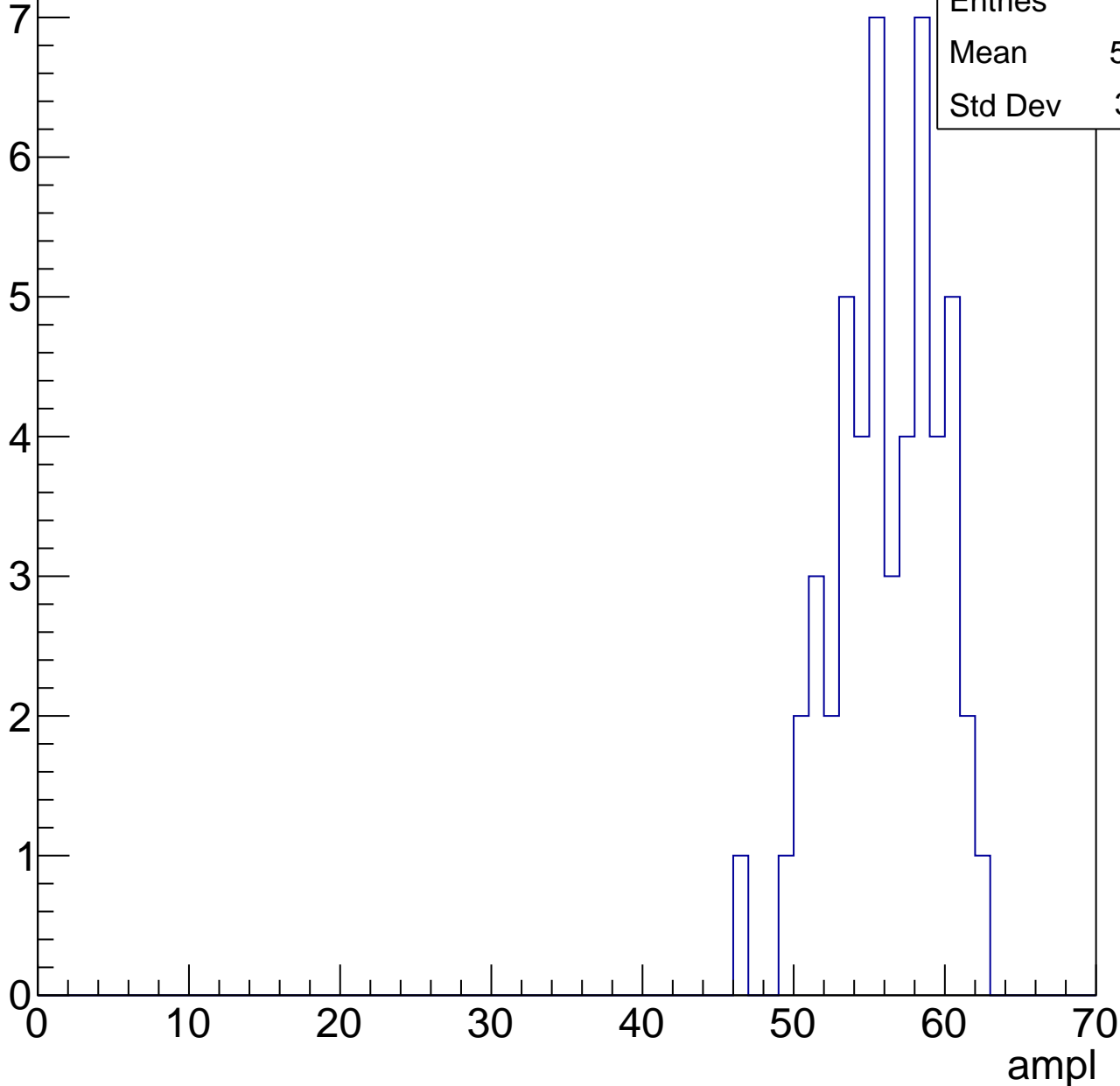


# B1L102S, U3-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	55.69
Std Dev	3.501

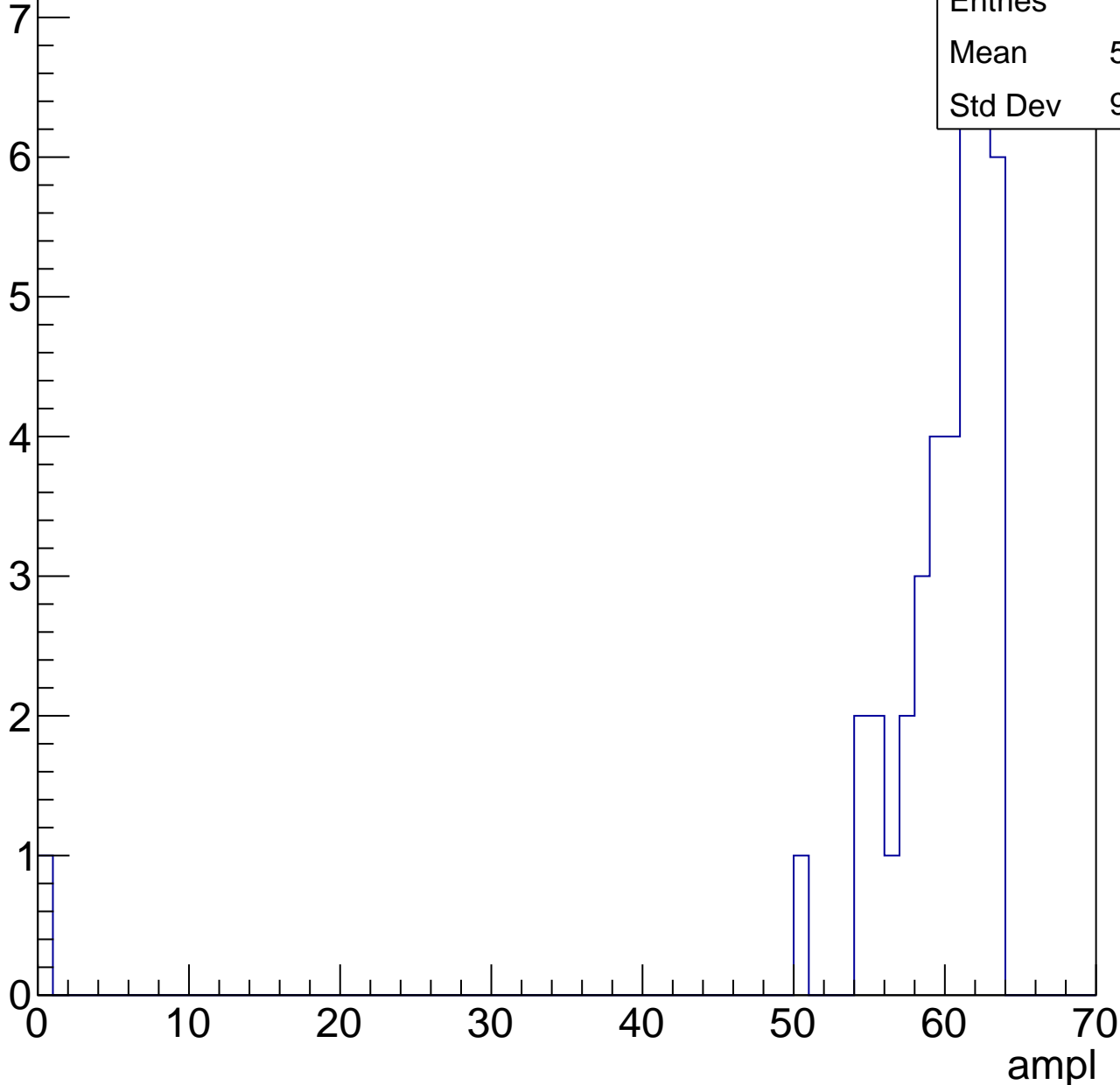


# B1L102S, U3-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	58.17
Std Dev	9.782



# B1L102S, U3-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U3-ch108, adc0

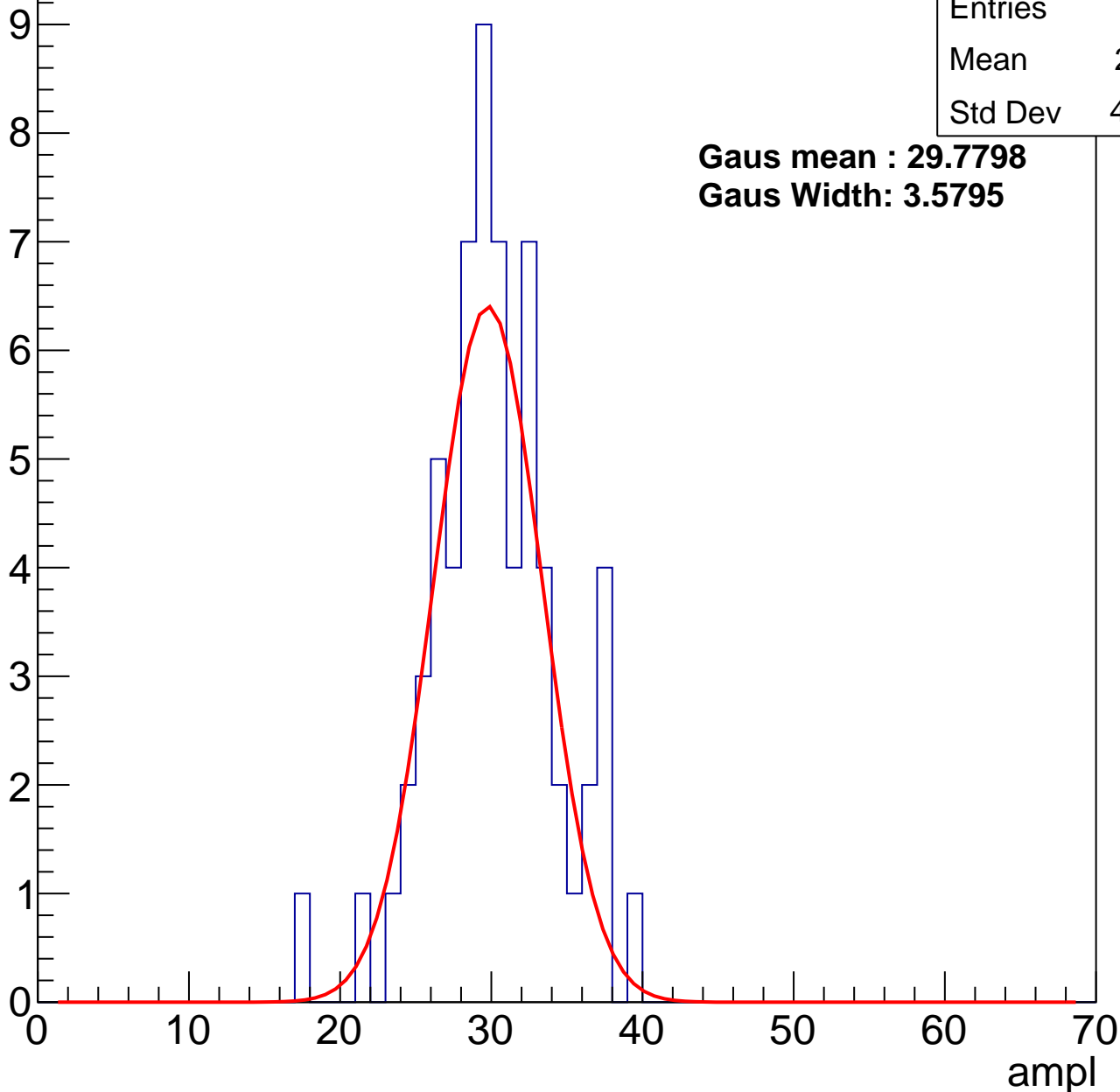
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	29.71
Std Dev	4.052

**Gaus mean : 29.7798**

**Gaus Width: 3.5795**



# B1L102S, U3-ch108, adc1

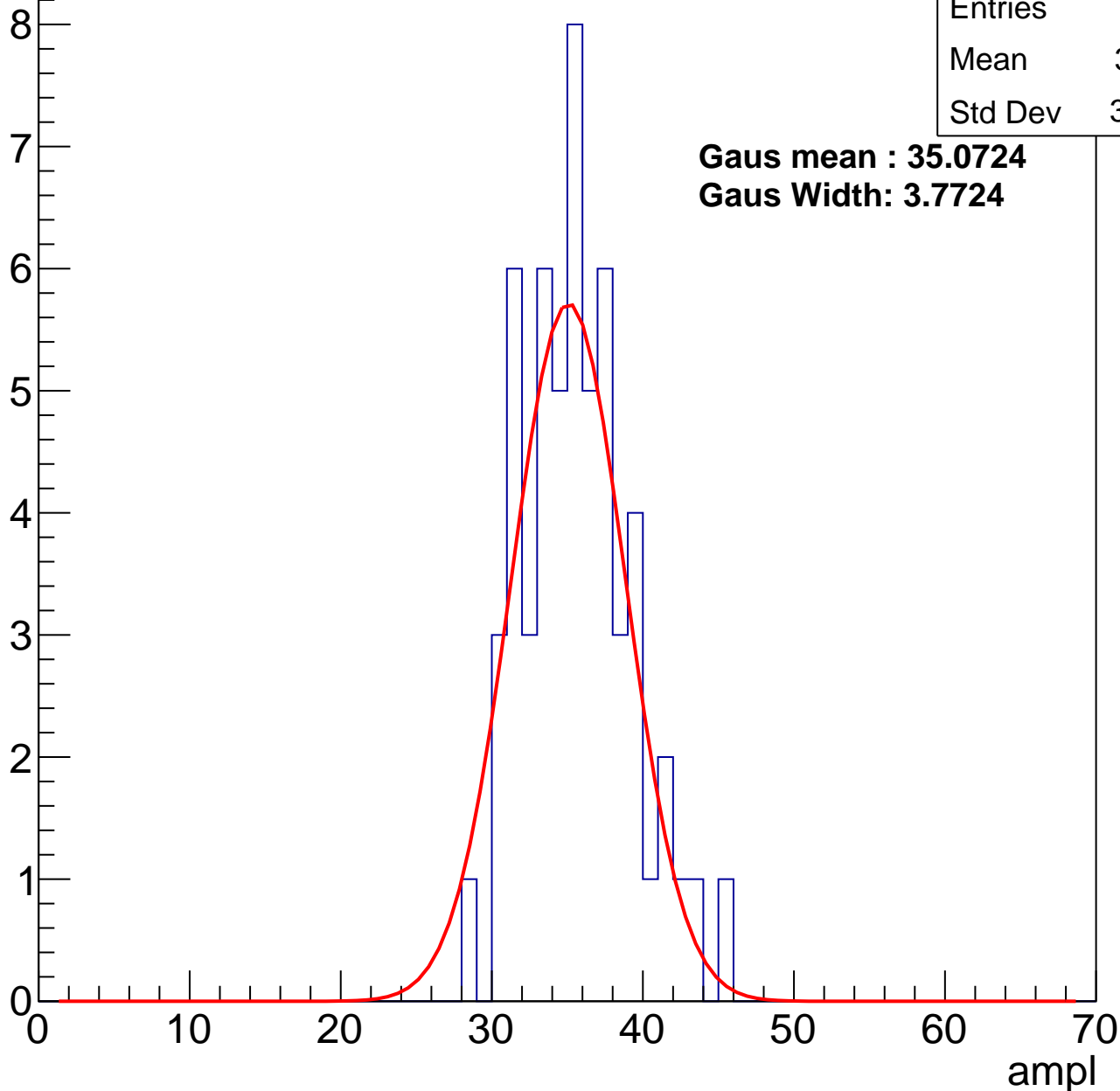
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	35.21
Std Dev	3.544

**Gaus mean : 35.0724**

**Gaus Width: 3.7724**



# B1L102S, U3-ch108, adc2

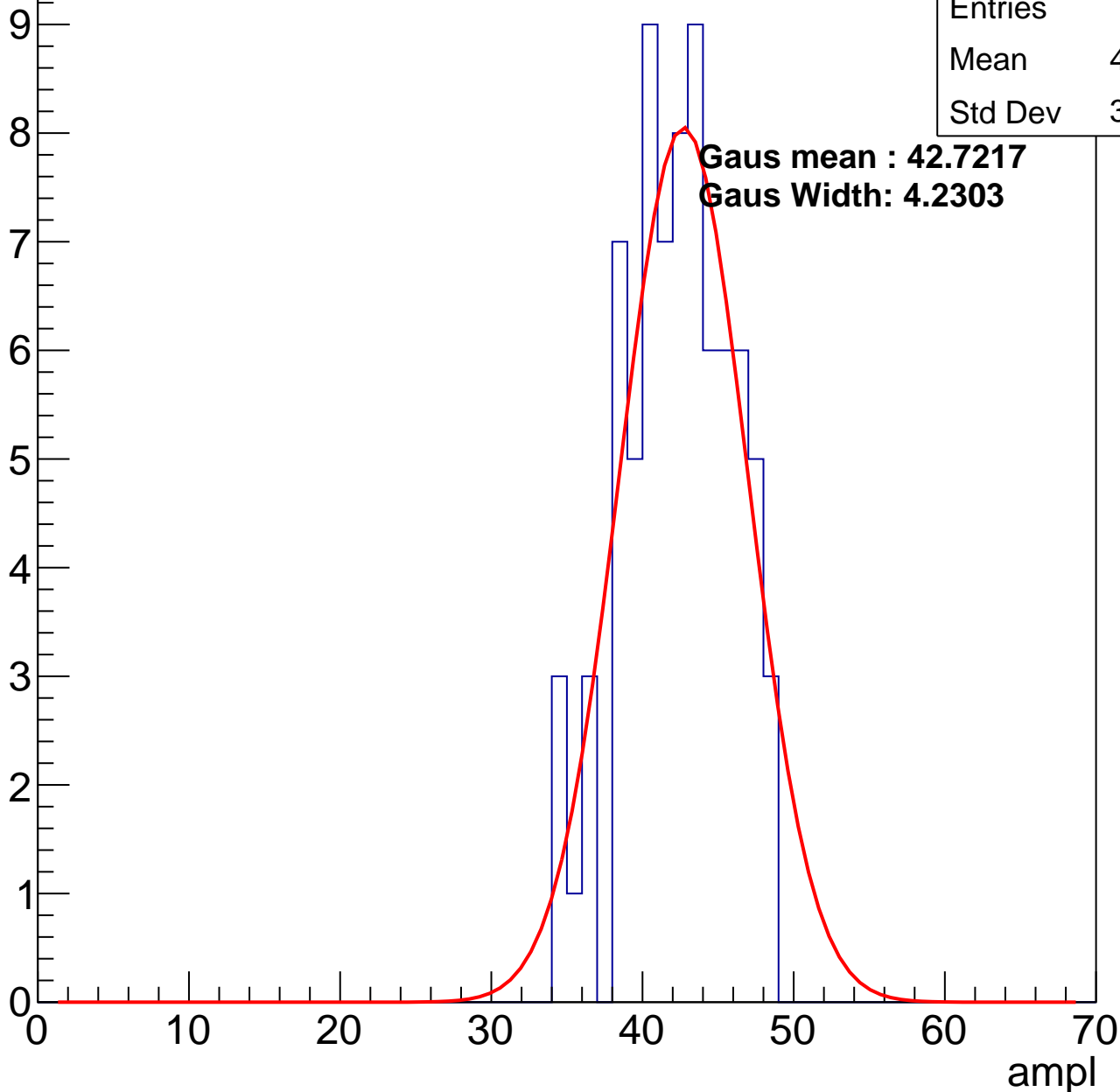
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	41.86
Std Dev	3.515

**Gaus mean : 42.7217**

**Gaus Width: 4.2303**

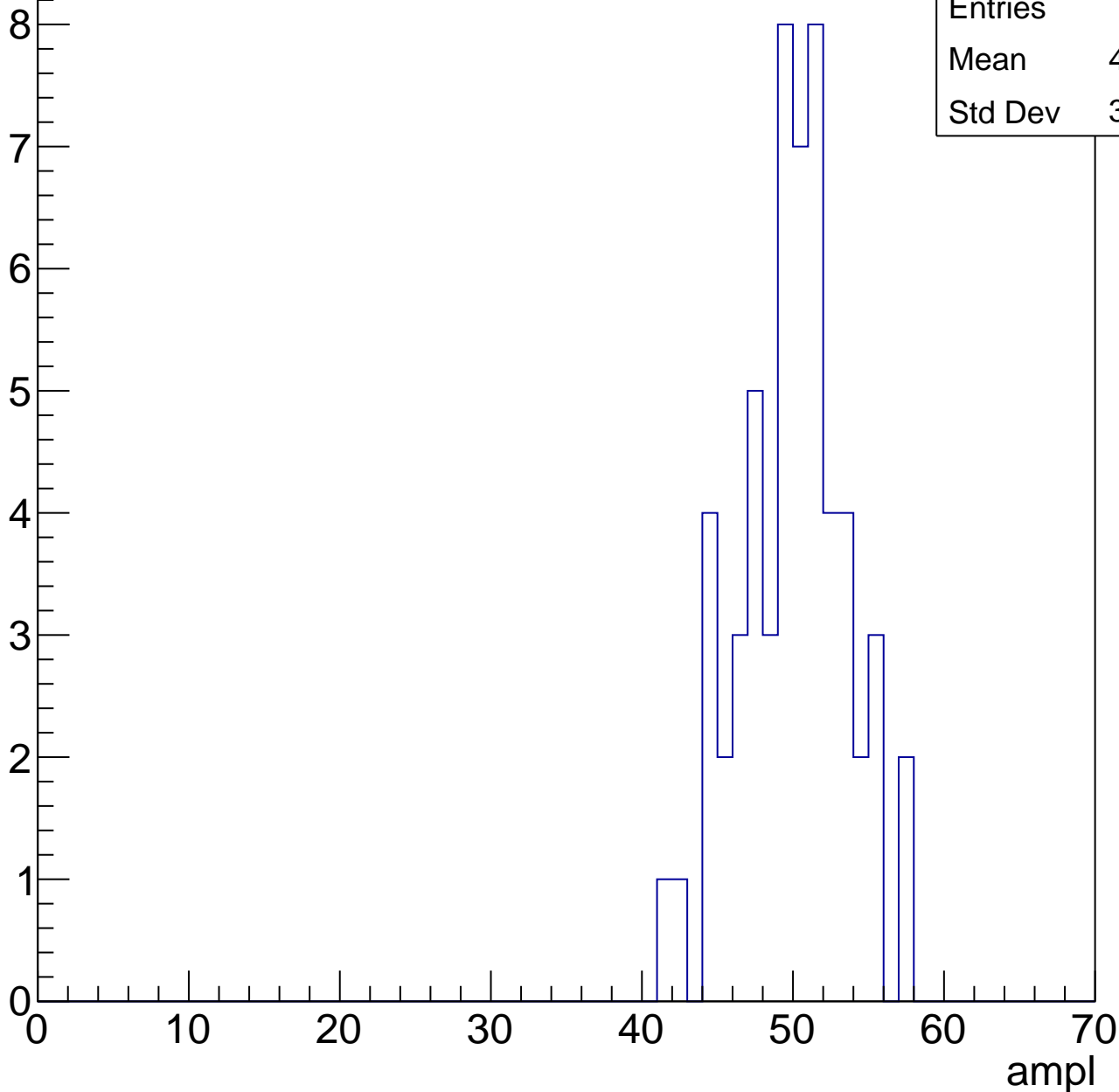


# B1L102S, U3-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	49.53
Std Dev	3.515

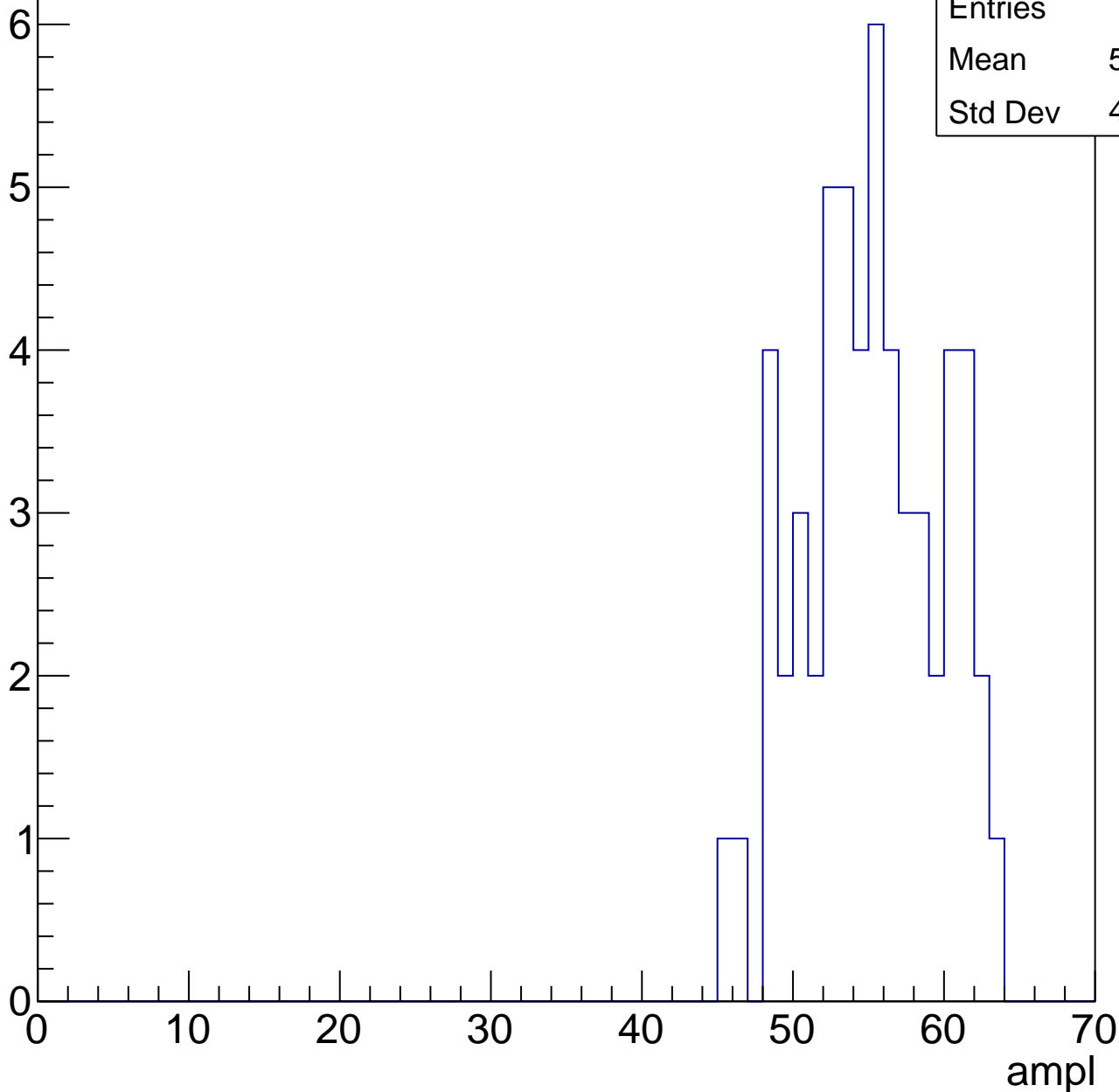


# B1L102S, U3-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	54.68
Std Dev	4.432



# B1L102S, U3-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	54
Mean	57.59
Std Dev	8.405

ampl

0 10 20 30 40 50 60 70

1

2

3

4

5

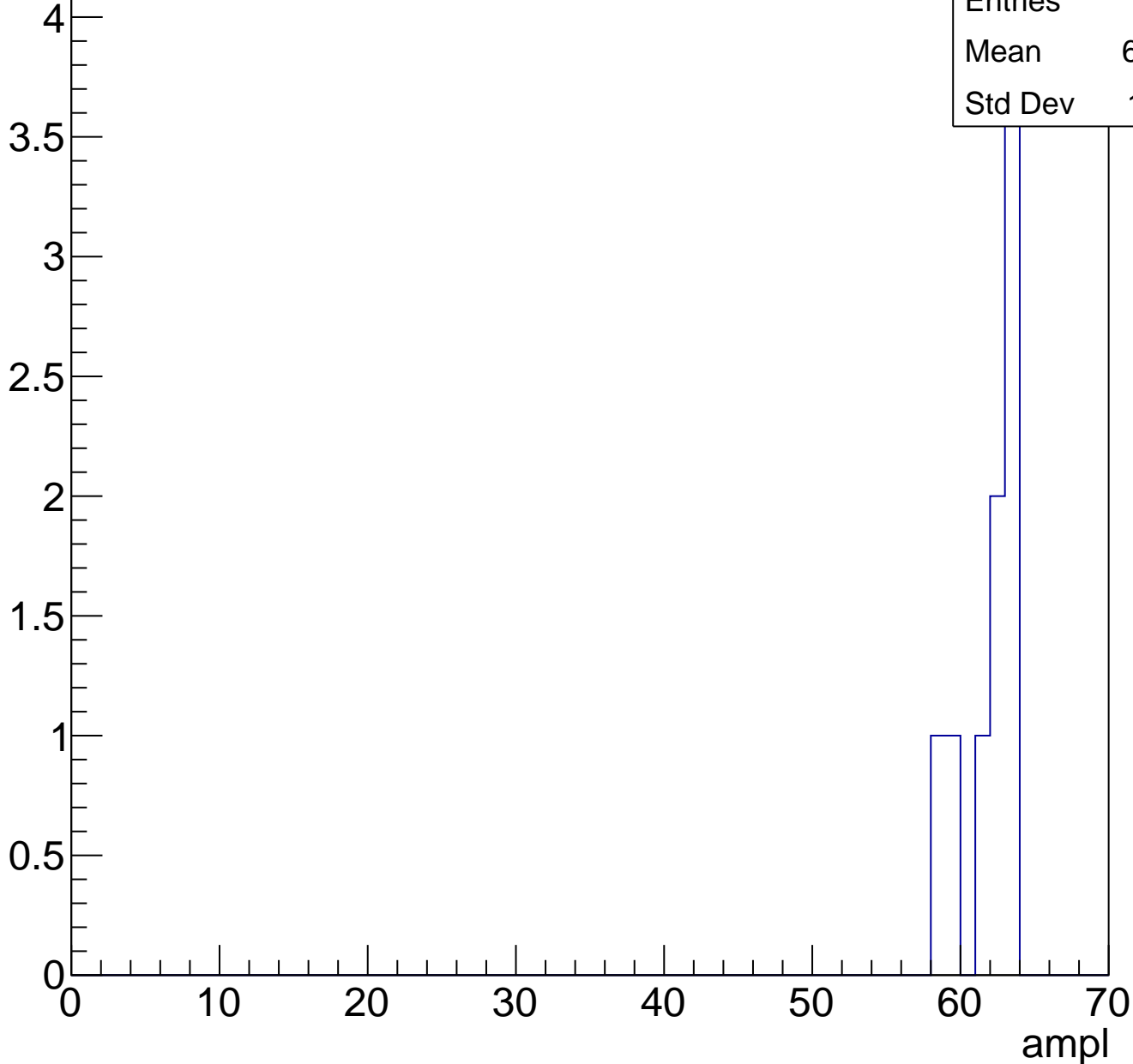
6

7

# B1L102S, U3-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U3-ch109, adc0

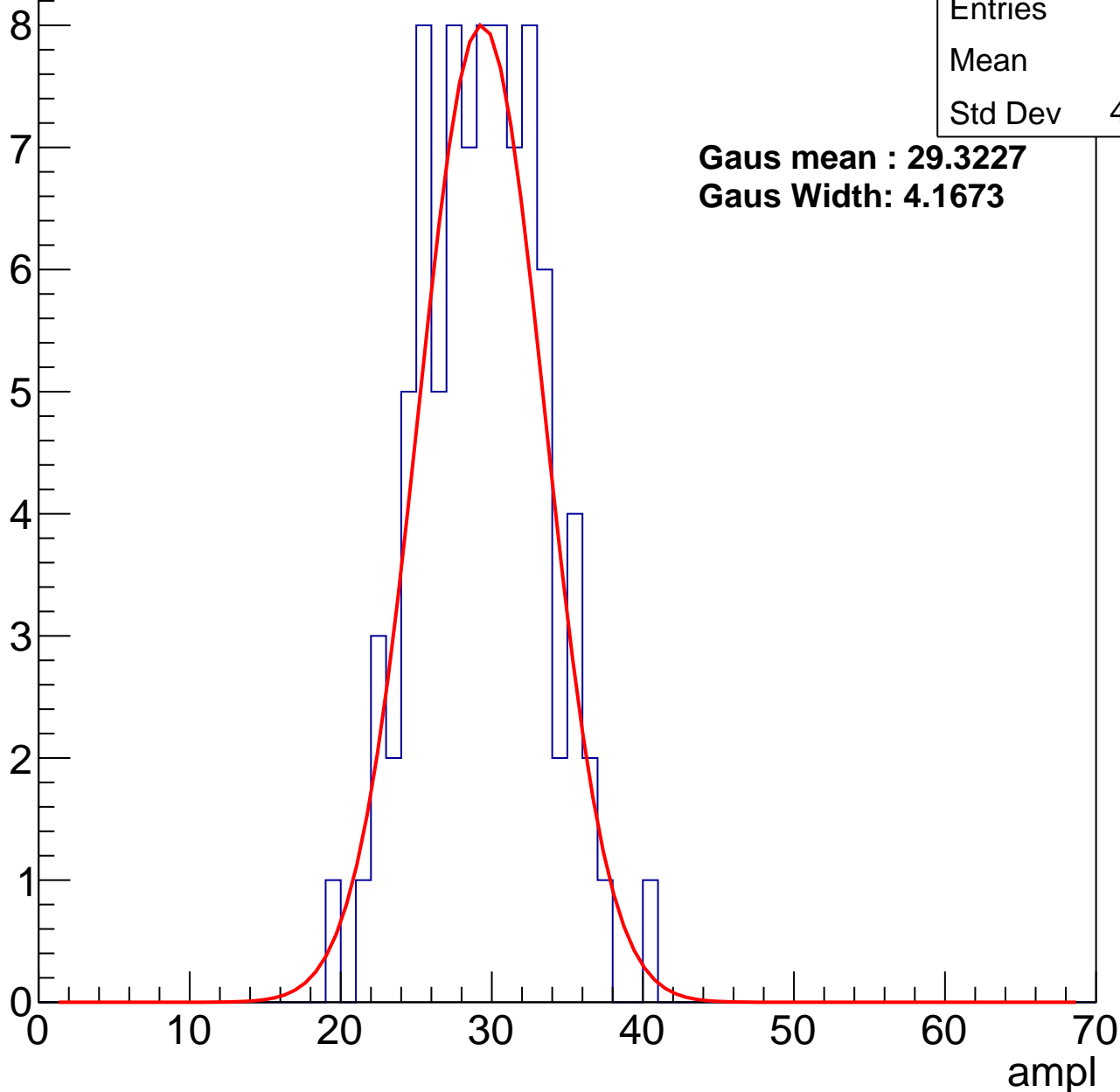
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	87
Mean	28.9
Std Dev	4.012

**Gaus mean : 29.3227**

**Gaus Width: 4.1673**



# B1L102S, U3-ch109, adc1

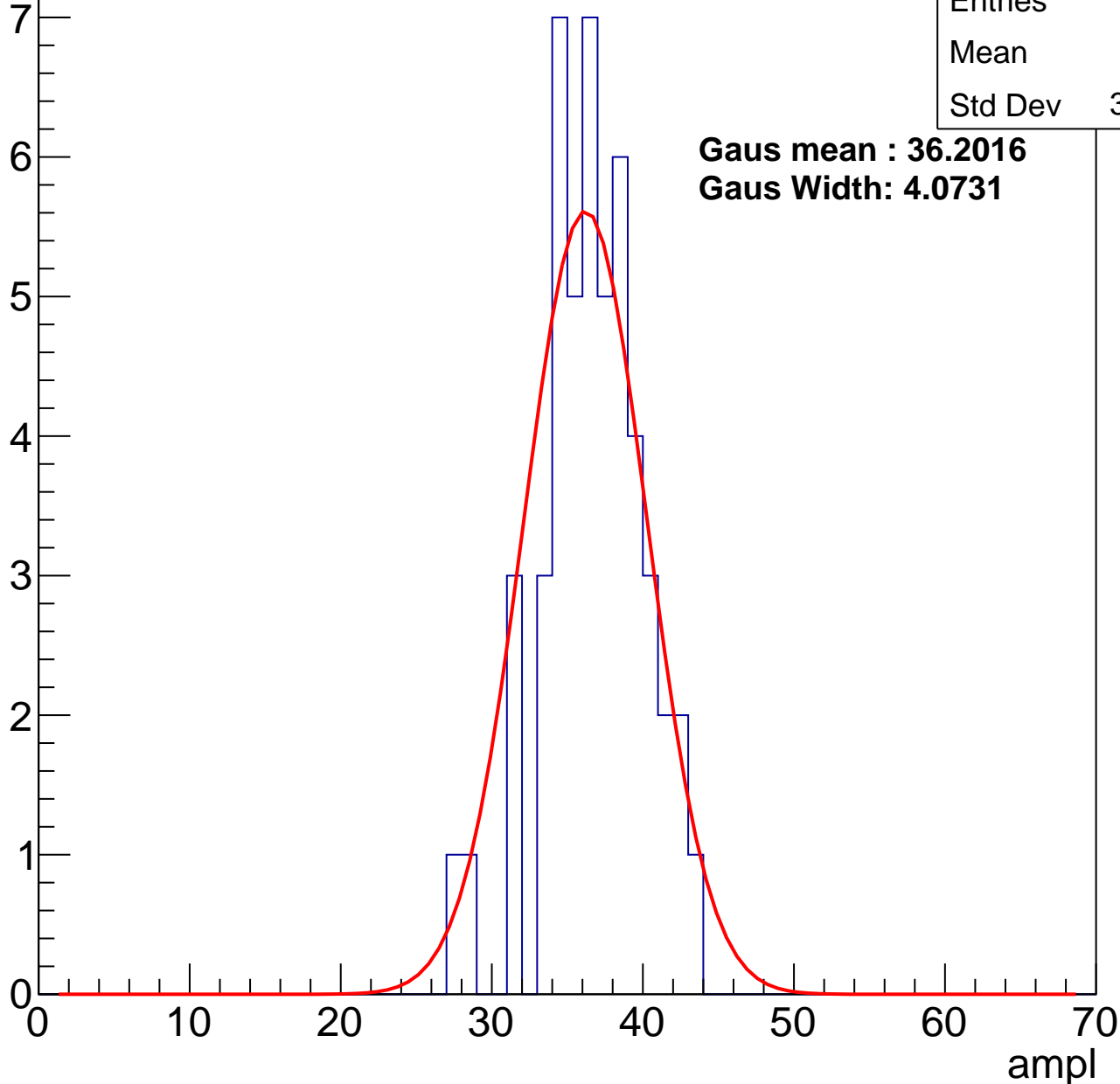
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	36.2
Std Dev	3.353

**Gaus mean : 36.2016**

**Gaus Width: 4.0731**



# B1L102S, U3-ch109, adc2

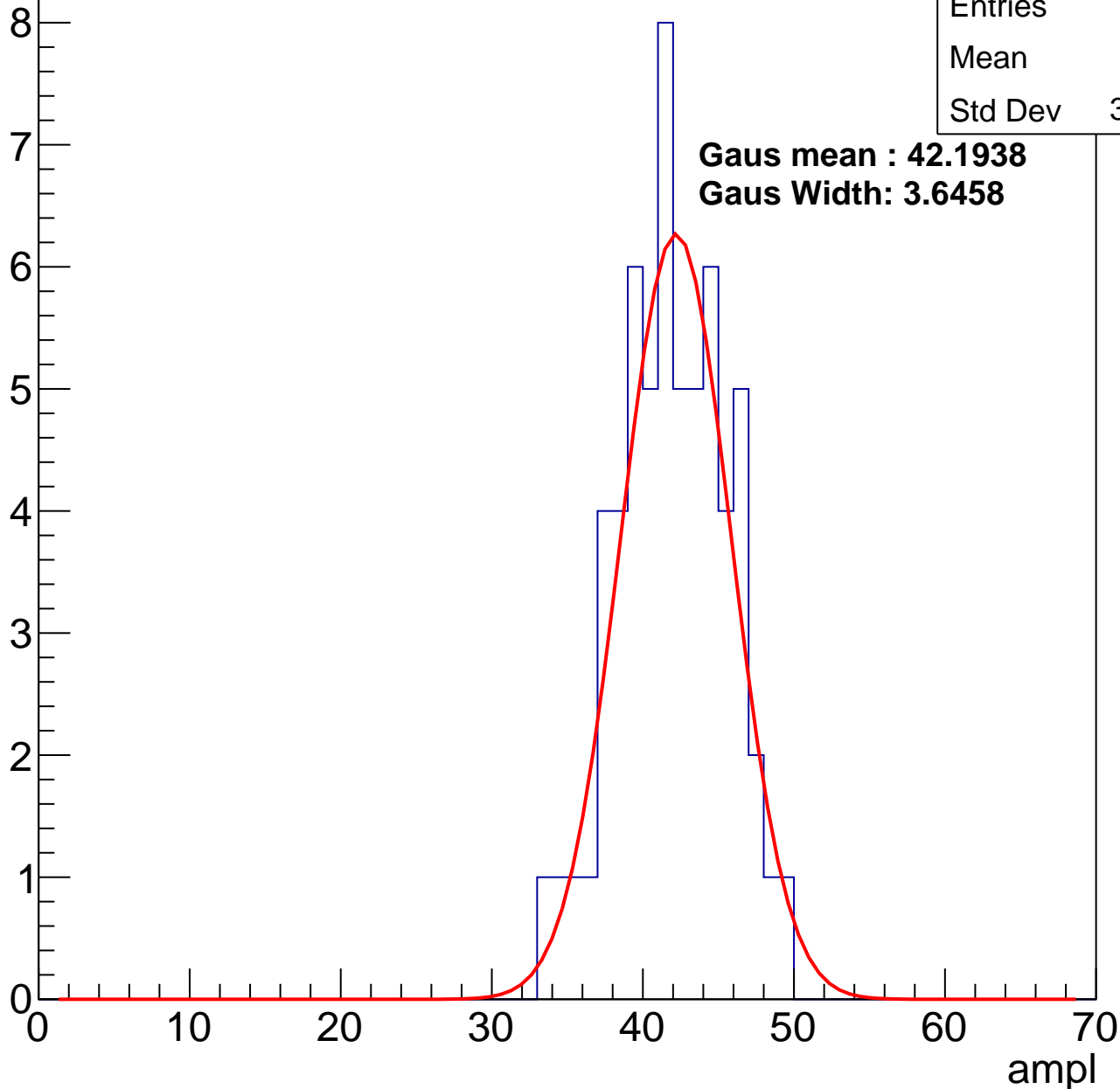
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	41.5
Std Dev	3.514

**Gaus mean : 42.1938**

**Gaus Width: 3.6458**

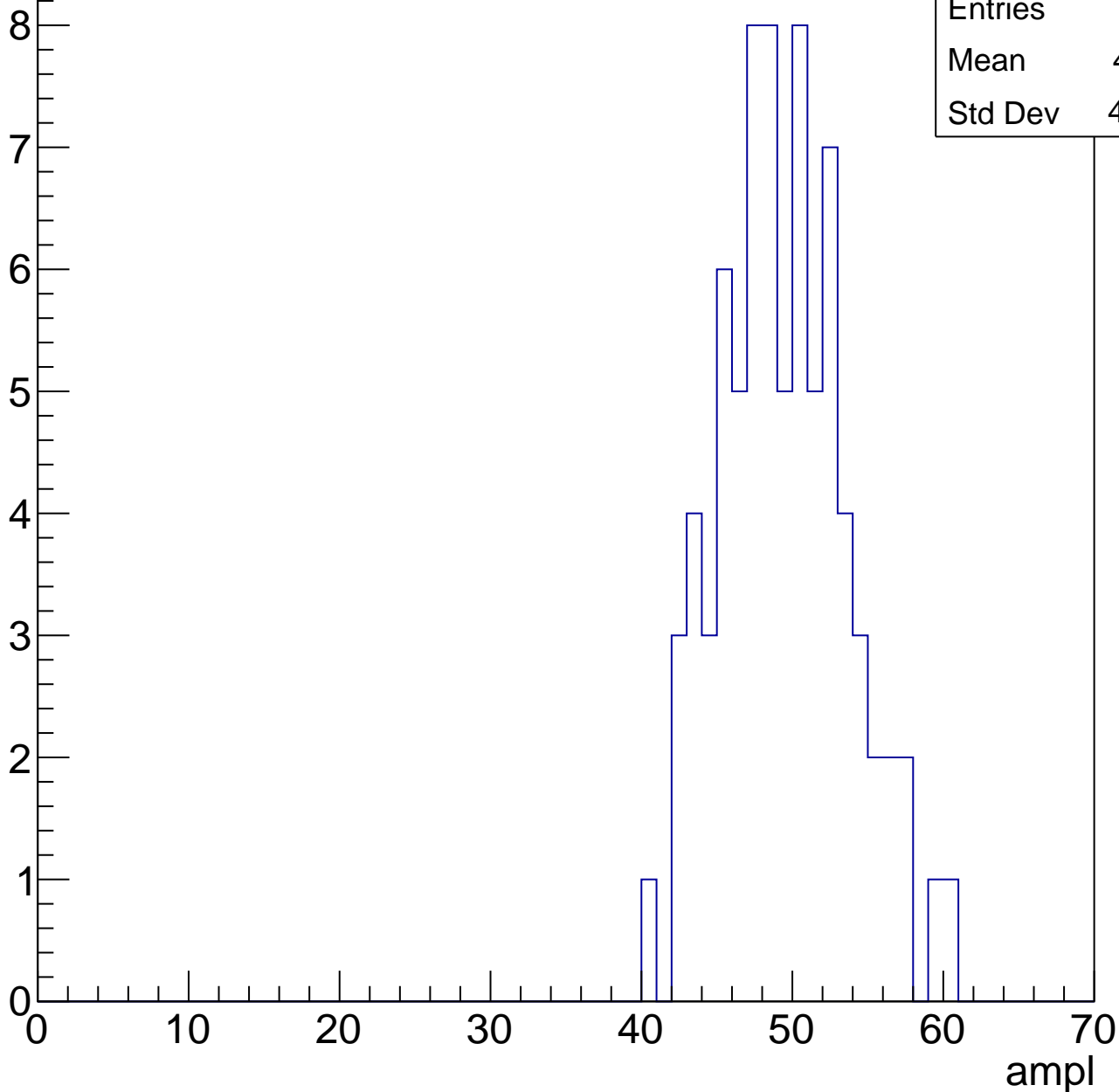


# B1L102S, U3-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	49.01
Std Dev	4.202

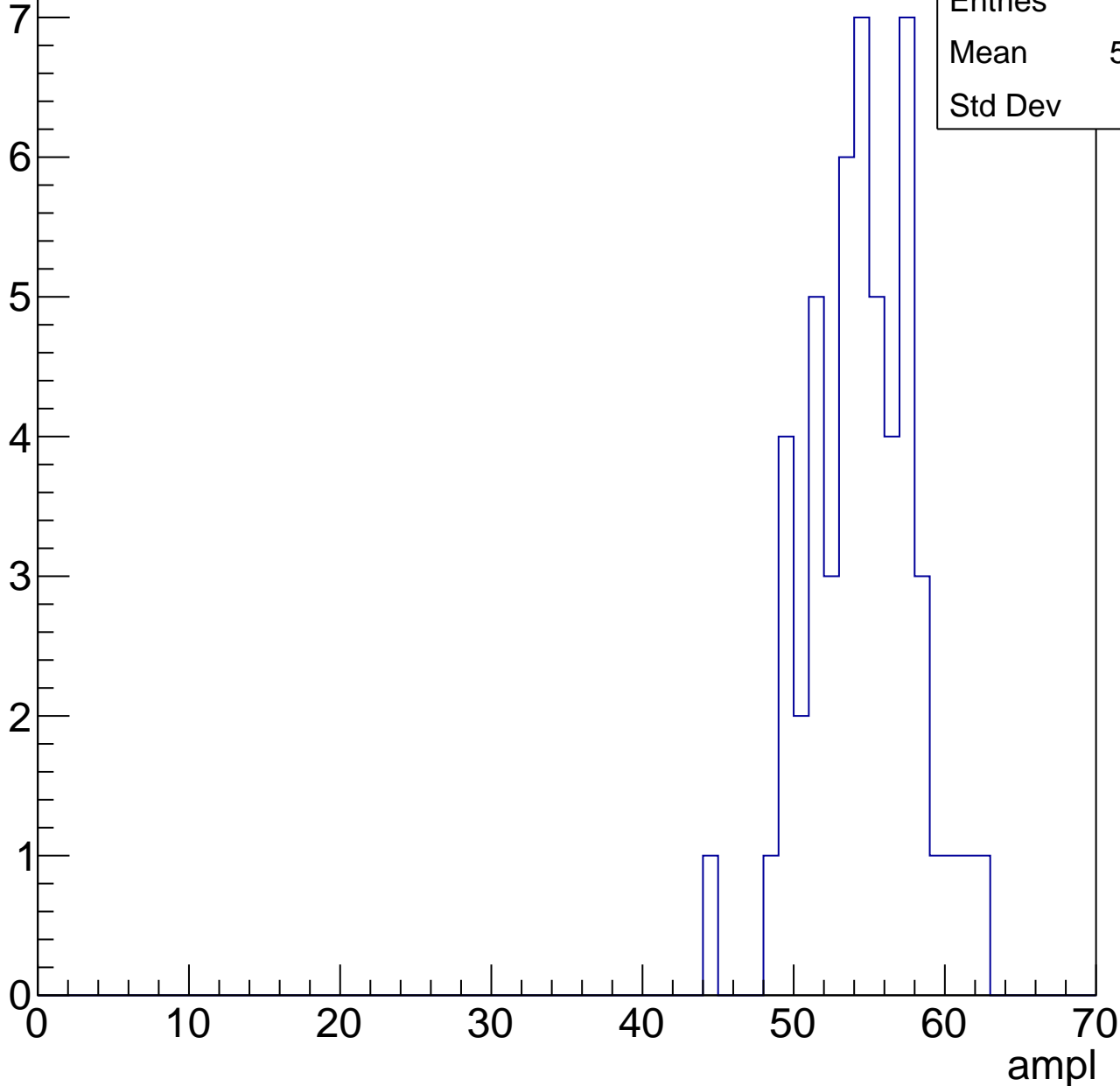


# B1L102S, U3-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	54.02
Std Dev	3.5

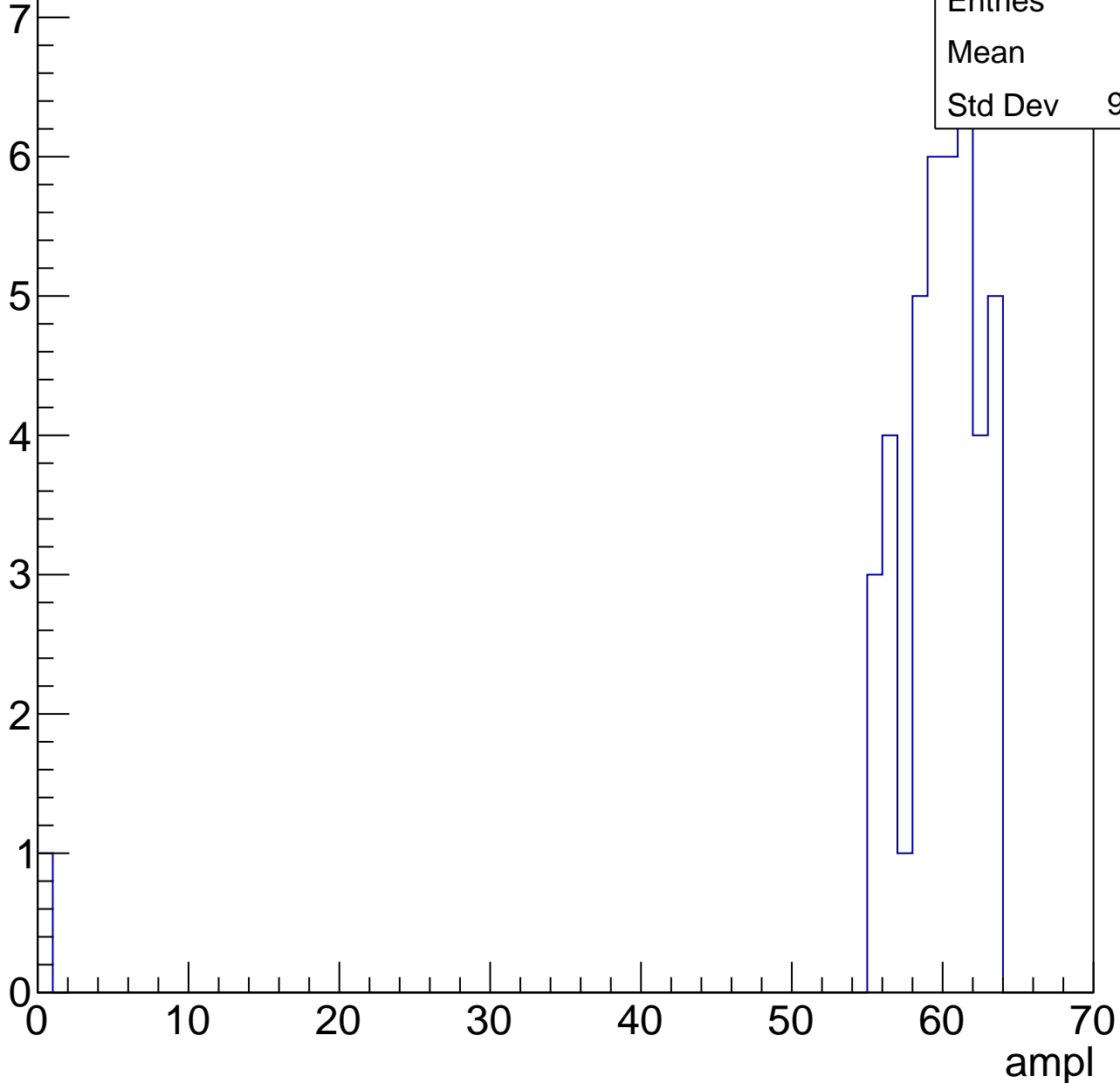


# B1L102S, U3-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

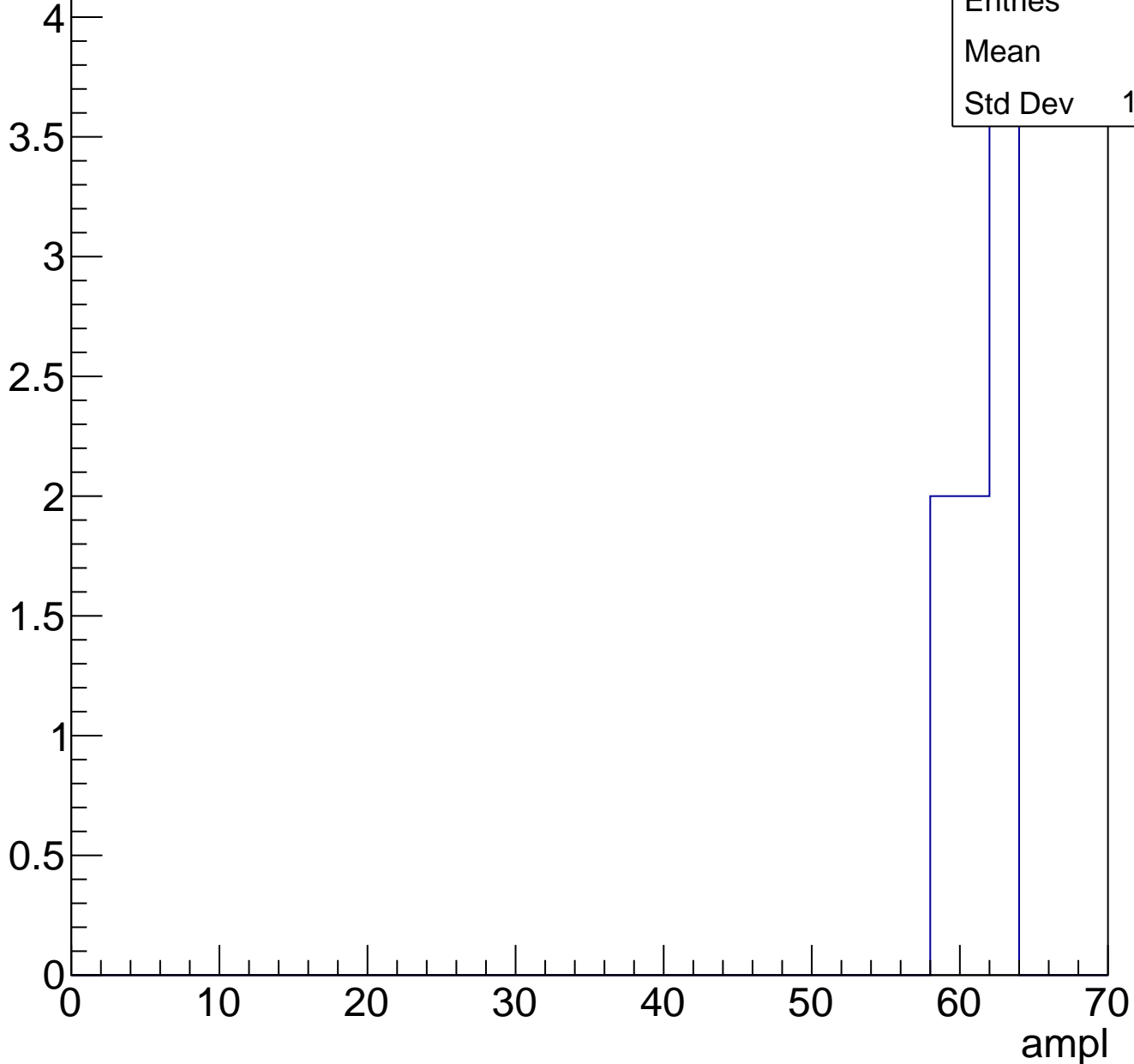
Entries	42
Mean	58.1
Std Dev	9.373



# B1L102S, U3-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

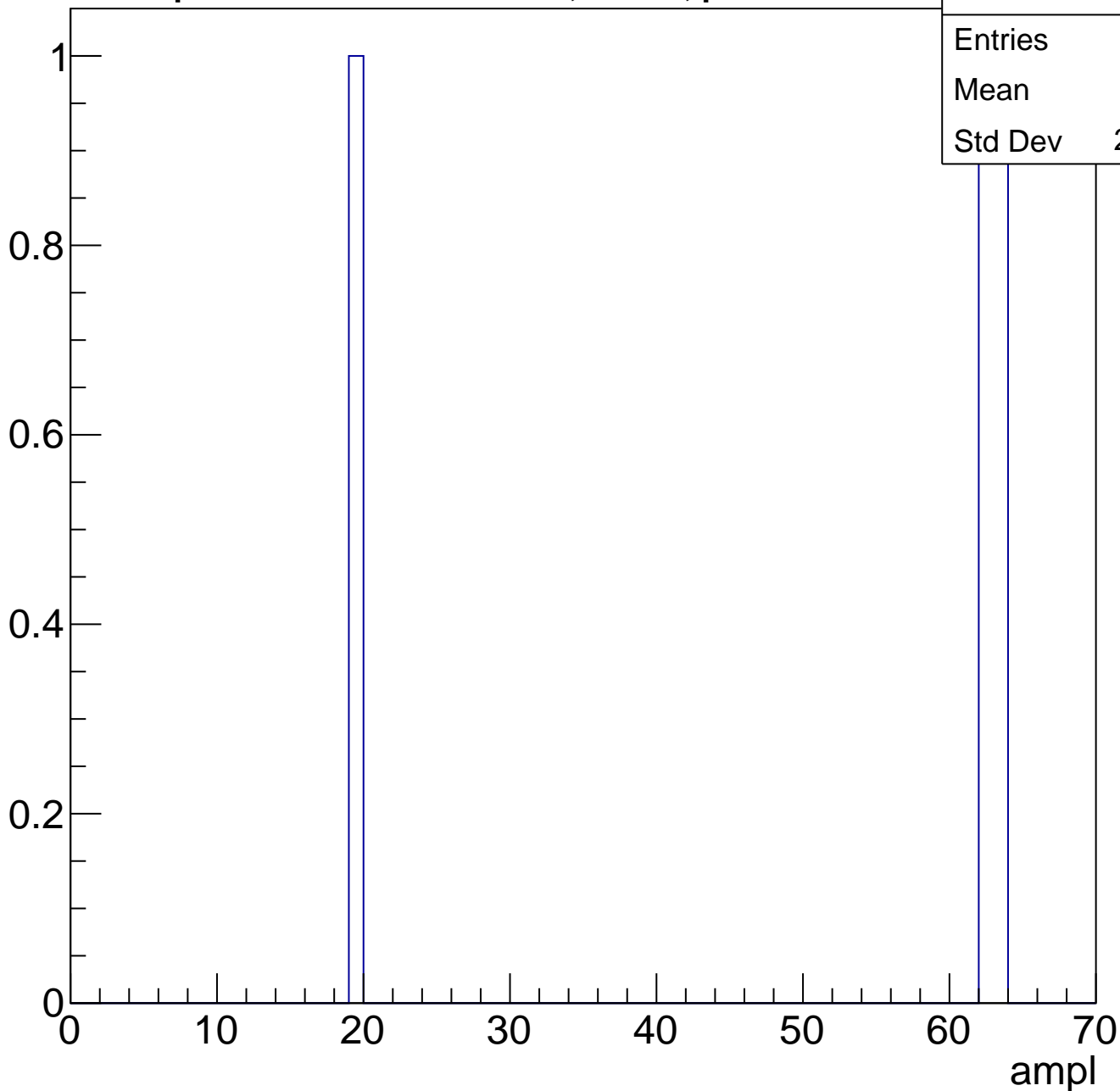




# B1L102S, U3-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch110, adc0

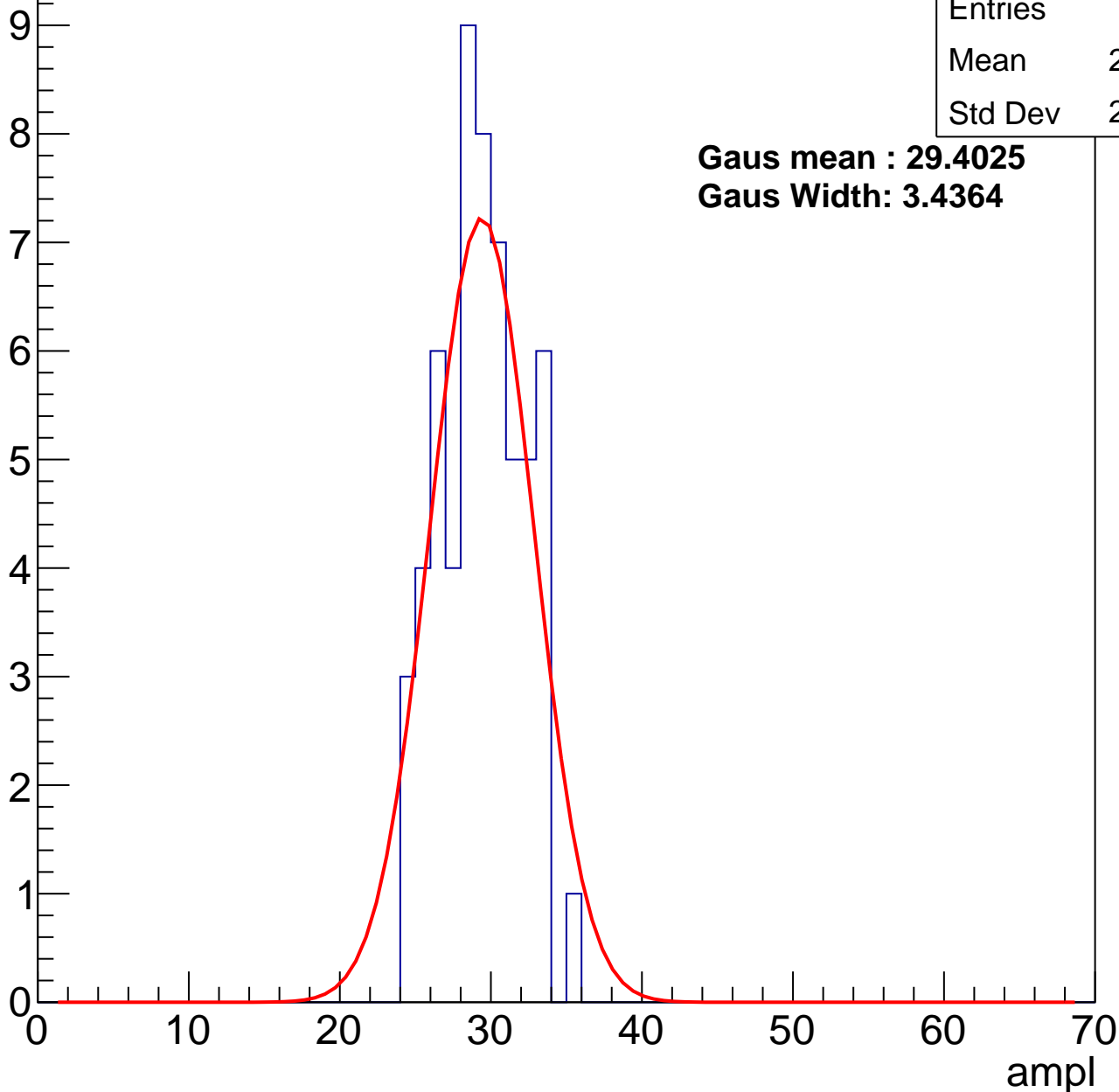
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	28.93
Std Dev	2.696

**Gaus mean : 29.4025**

**Gaus Width: 3.4364**



# B1L102S, U3-ch110, adc1

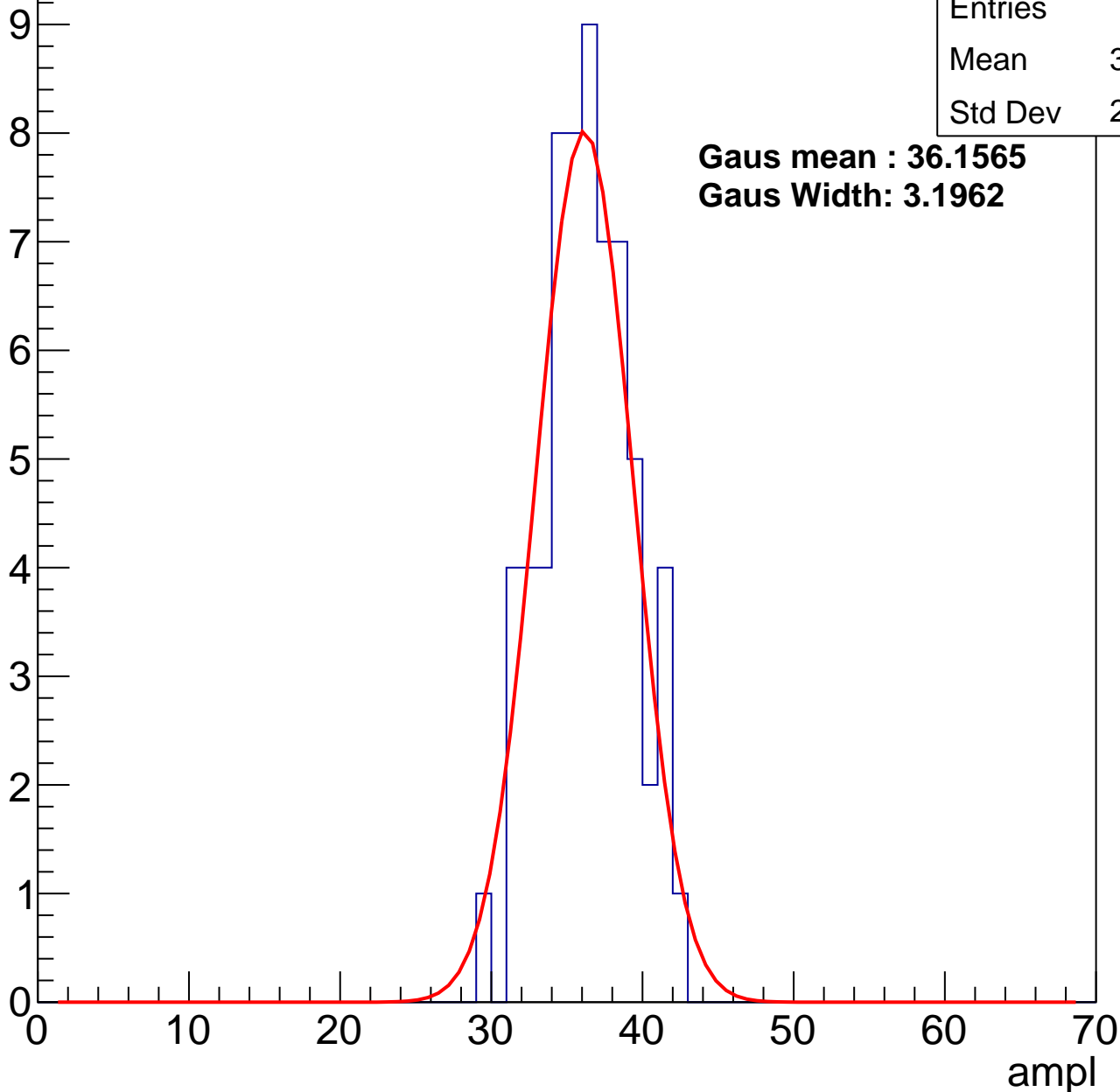
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	35.86
Std Dev	2.893

**Gaus mean : 36.1565**

**Gaus Width: 3.1962**



# B1L102S, U3-ch110, adc2

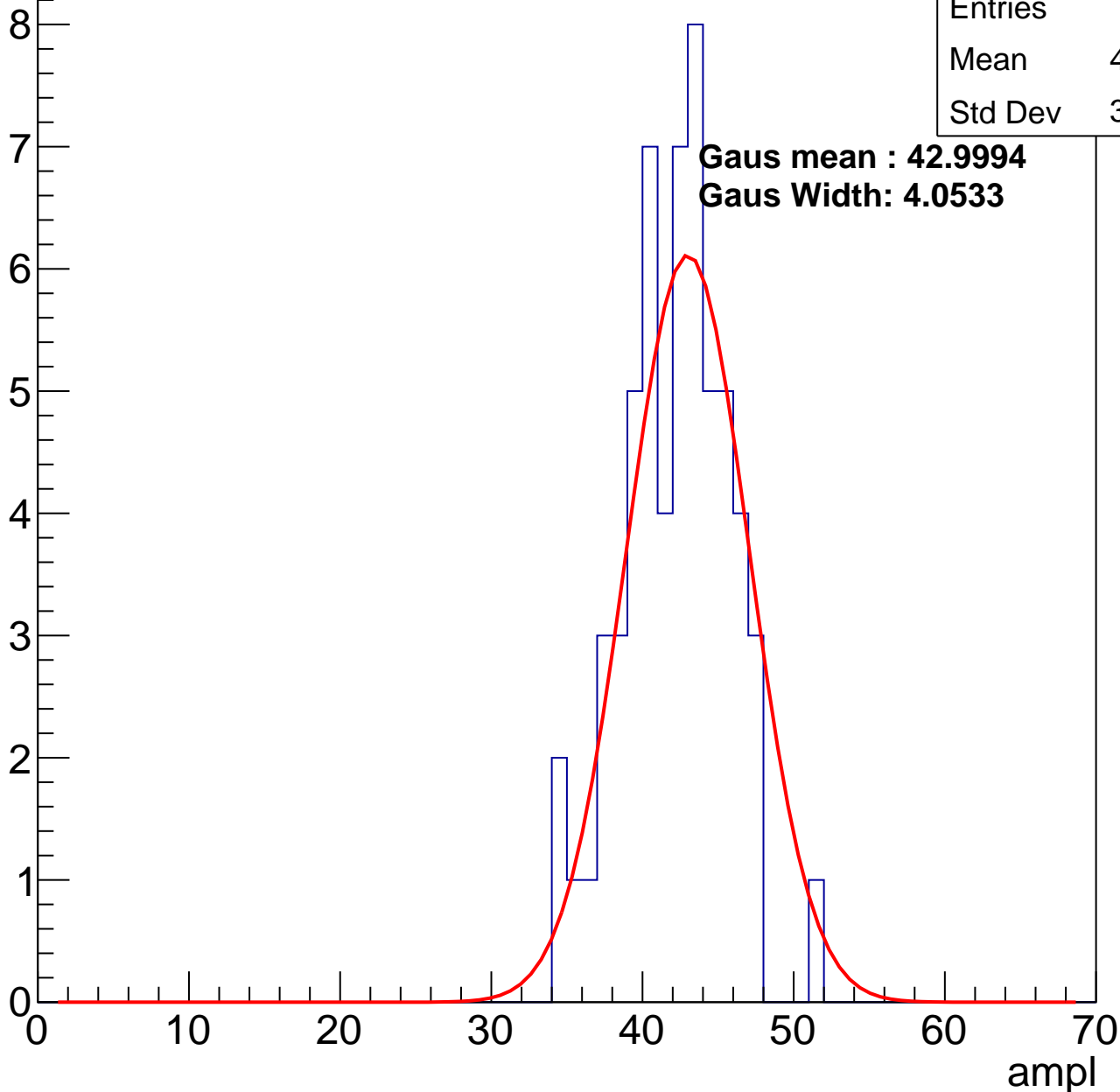
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	41.73
Std Dev	3.449

**Gaus mean : 42.9994**

**Gaus Width: 4.0533**



# B1L102S, U3-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	73
Mean	48.07
Std Dev	3.52

Entry

10

8

6

4

2

0

0

10

20

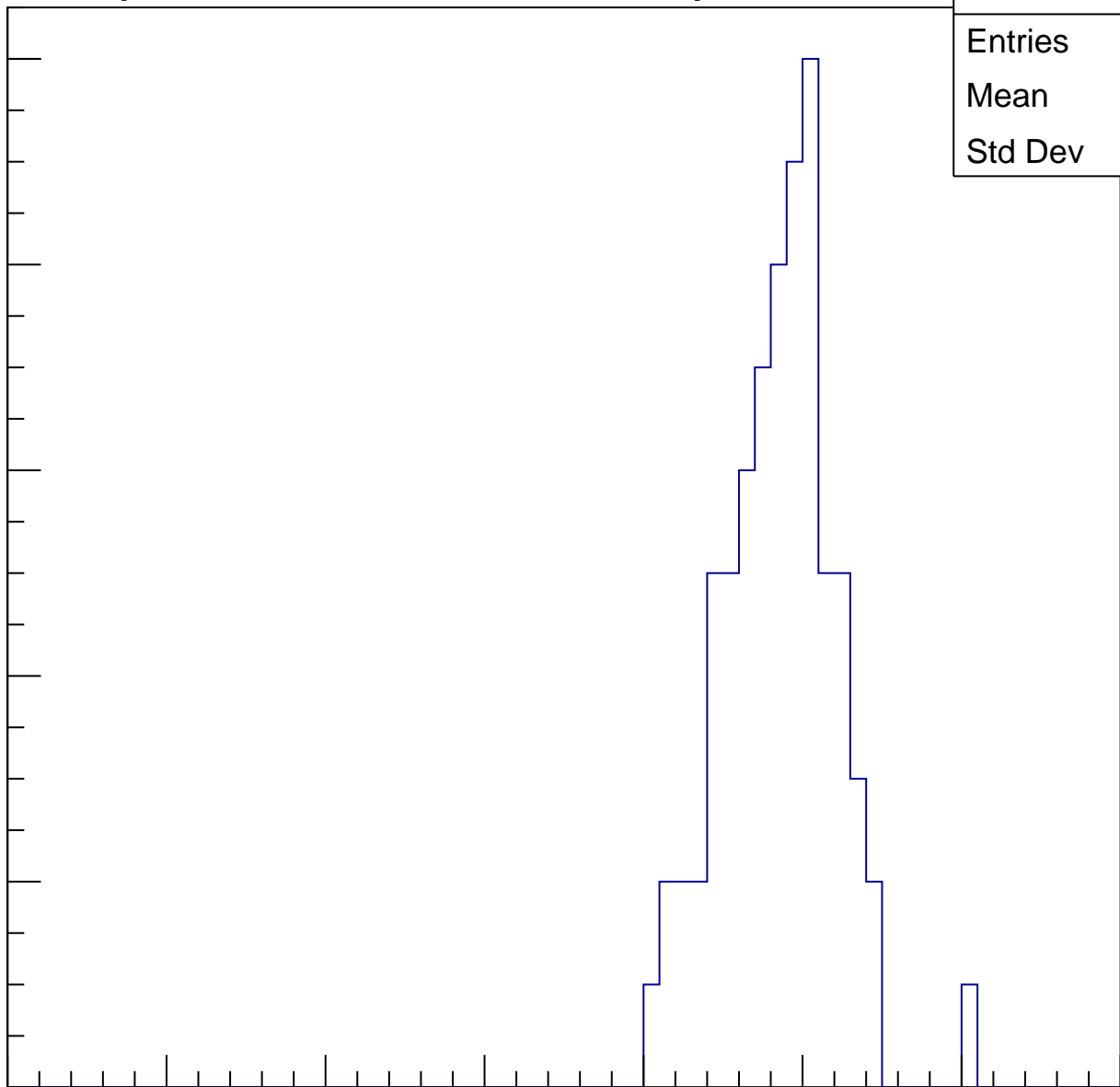
30

40

50

60

ampl

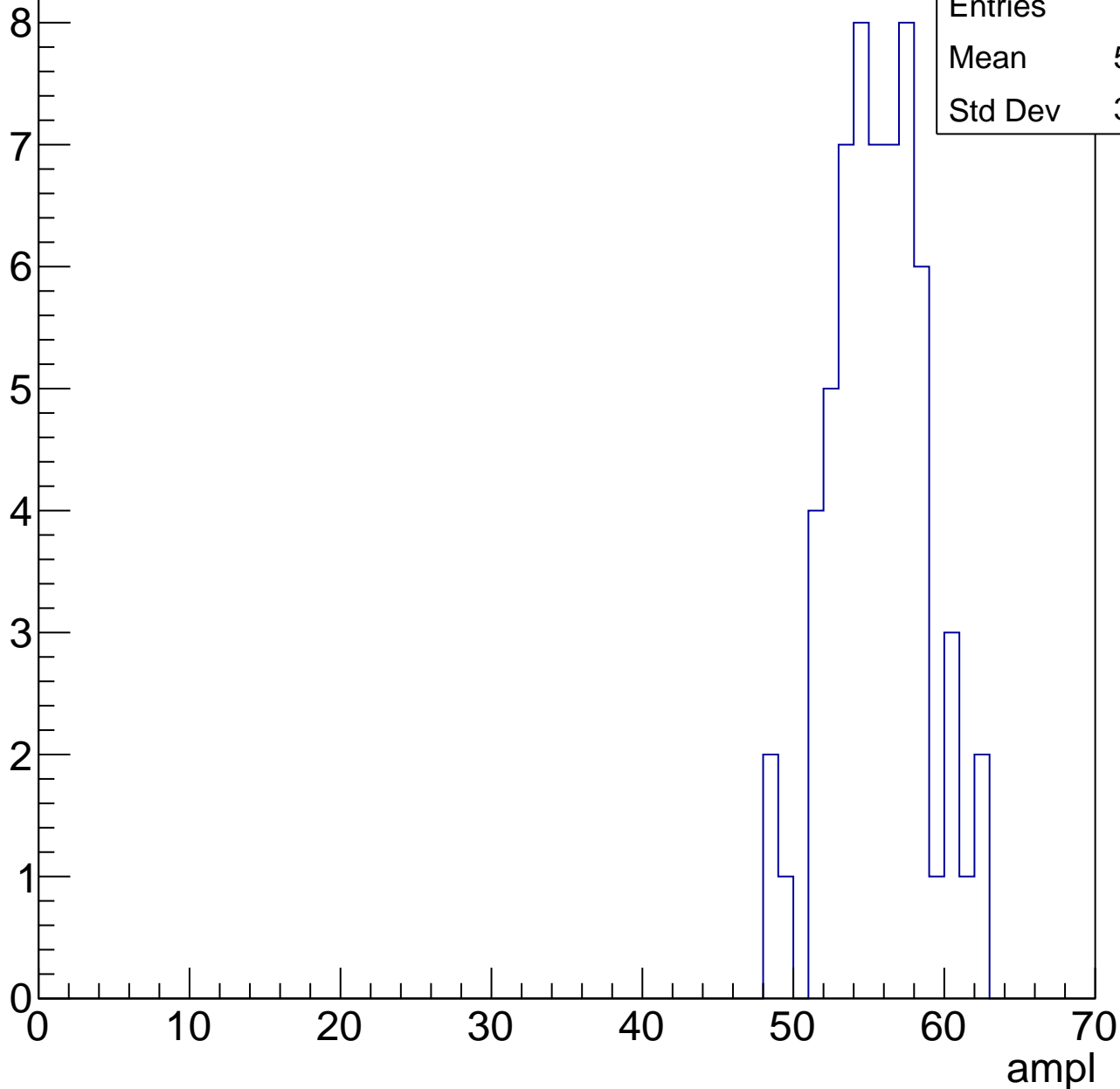


# B1L102S, U3-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	55.11
Std Dev	3.101

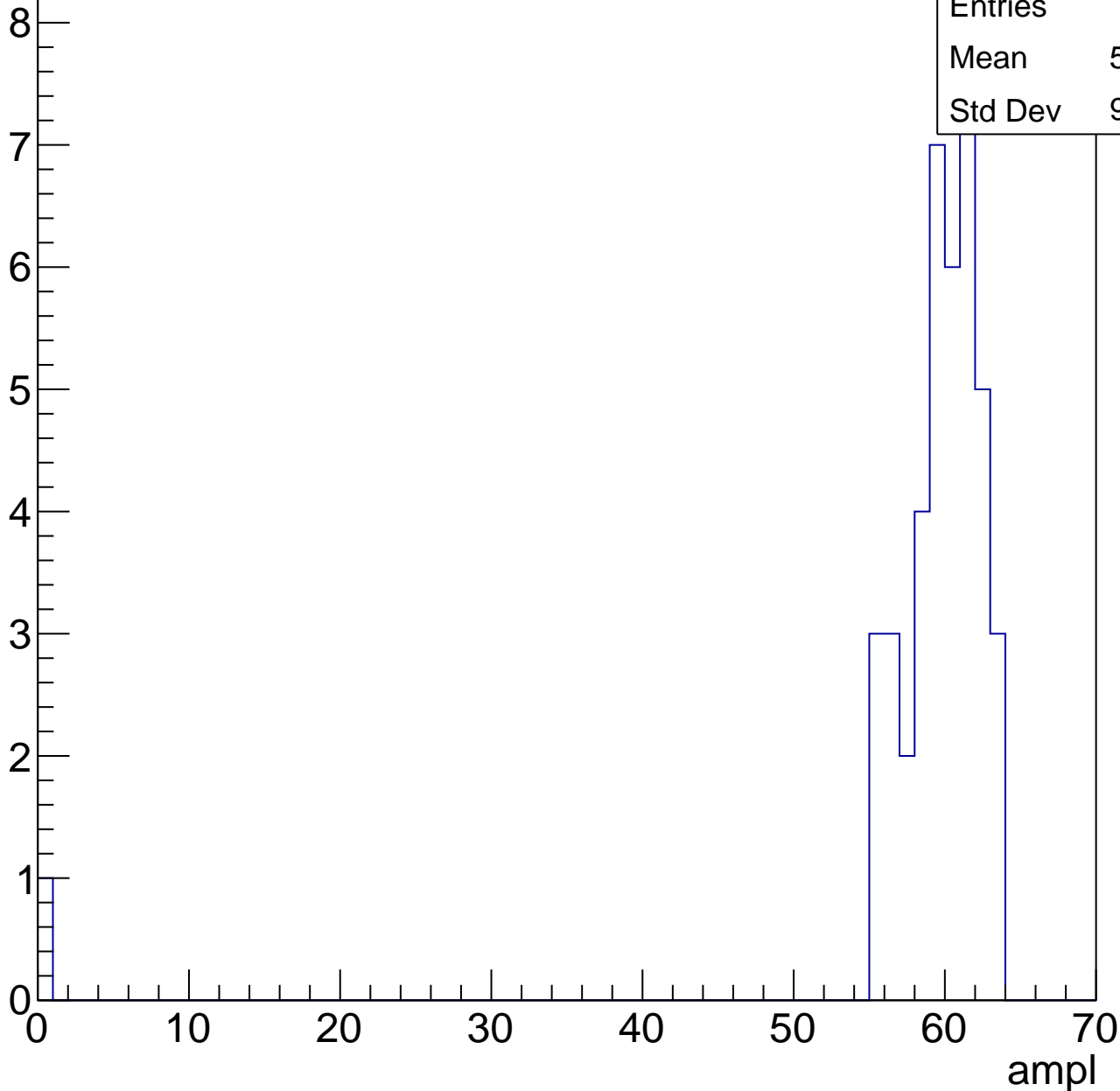


# B1L102S, U3-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	42
Mean	58.07
Std Dev	9.339

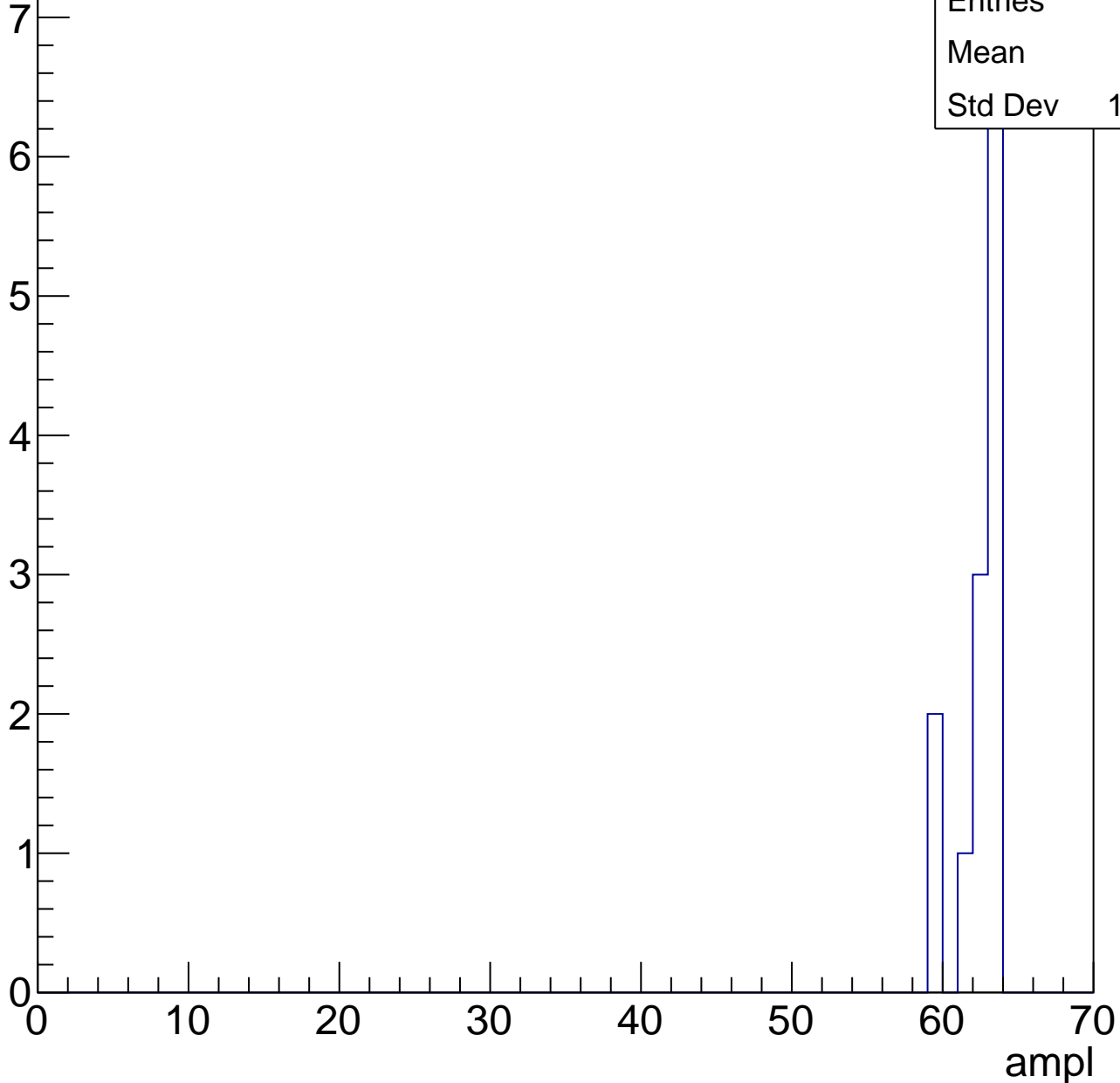


# B1L102S, U3-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	13
Mean	62
Std Dev	1.414





# B1L102S, U3-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U3-ch111, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	77
Mean	29.51
Std Dev	5.181

**Gaus mean : 29.4188**

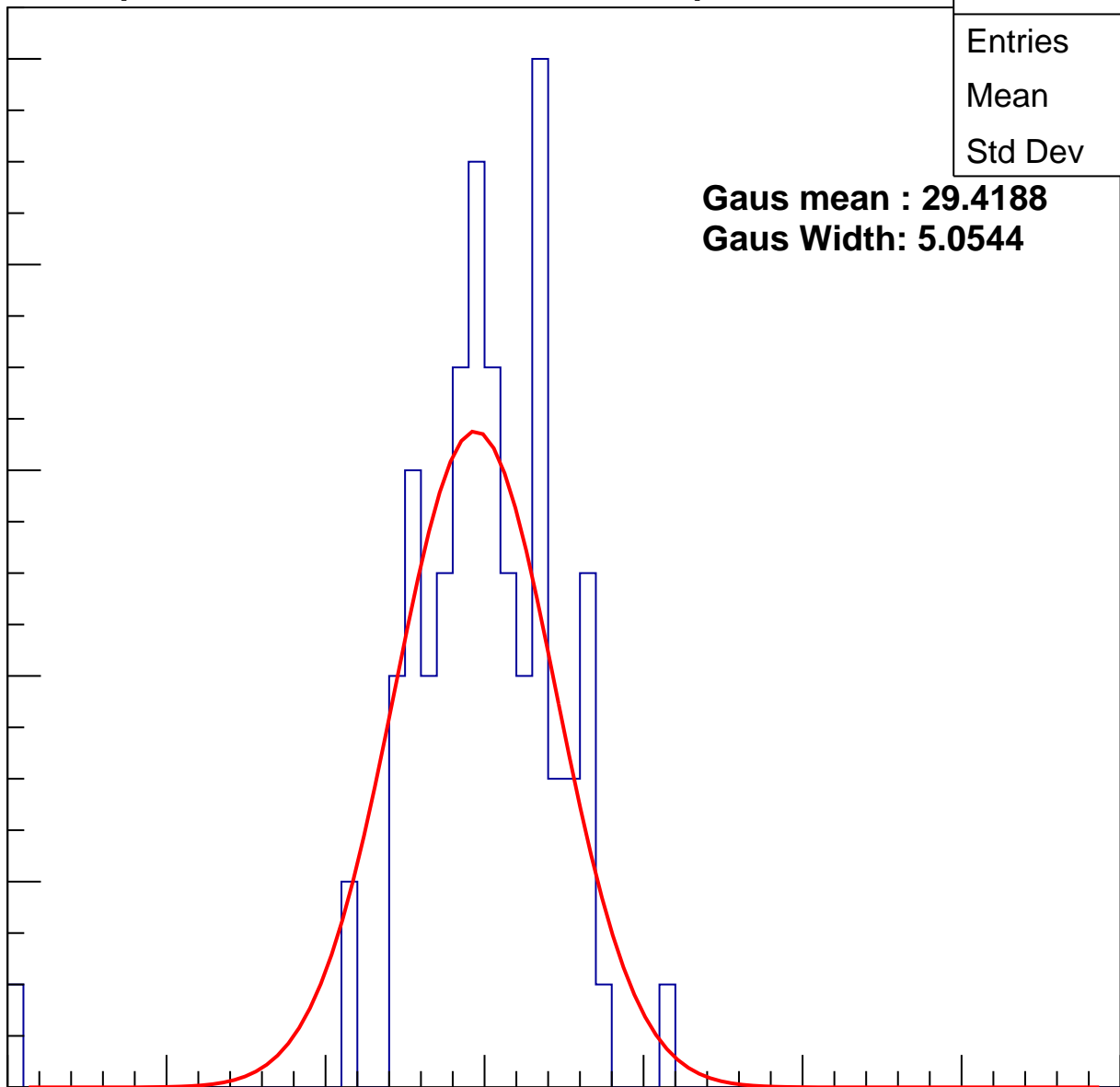
**Gaus Width: 5.0544**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U3-ch111, adc1

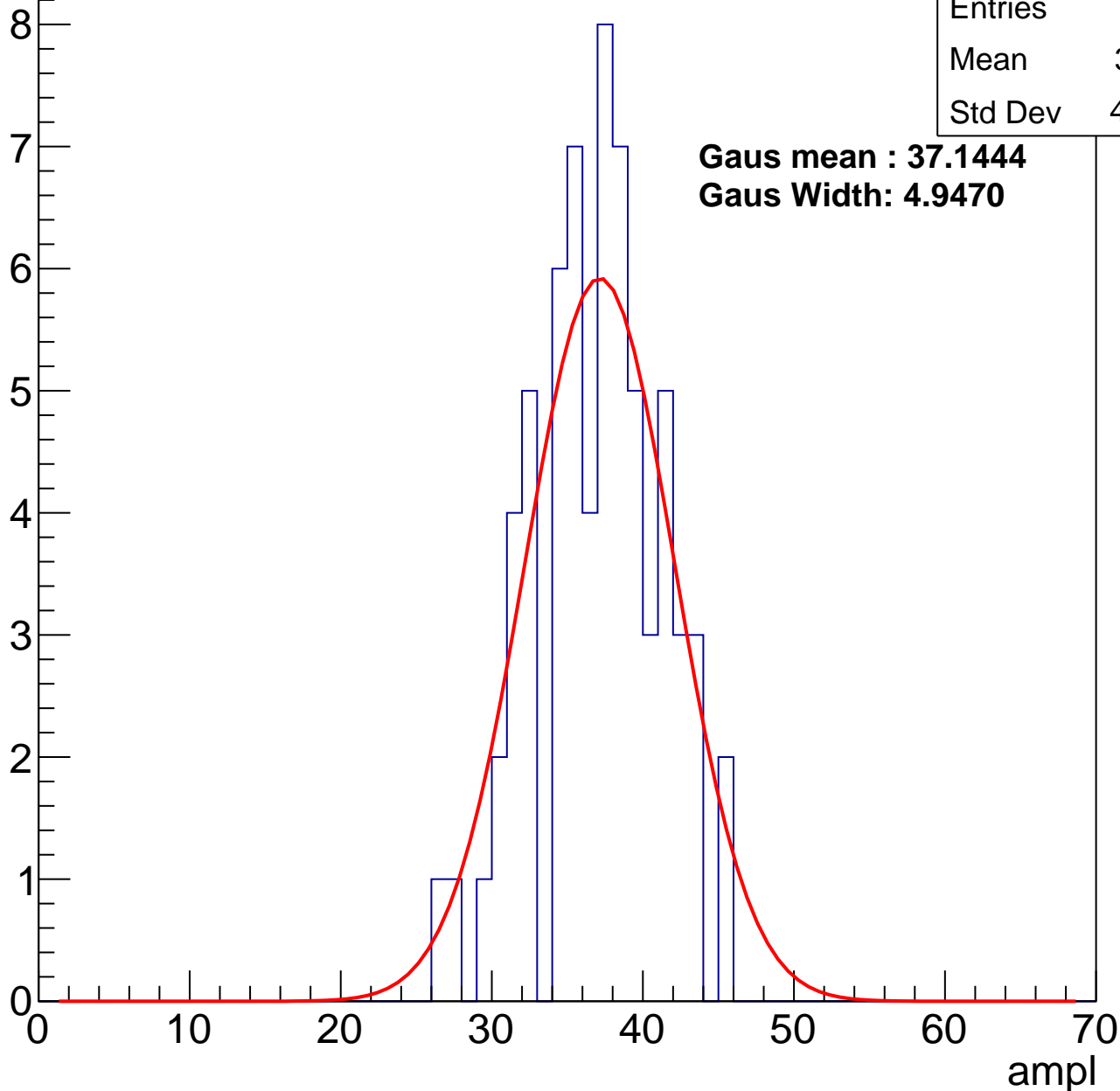
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	36.51
Std Dev	4.173

**Gaus mean : 37.1444**

**Gaus Width: 4.9470**



# B1L102S, U3-ch111, adc2

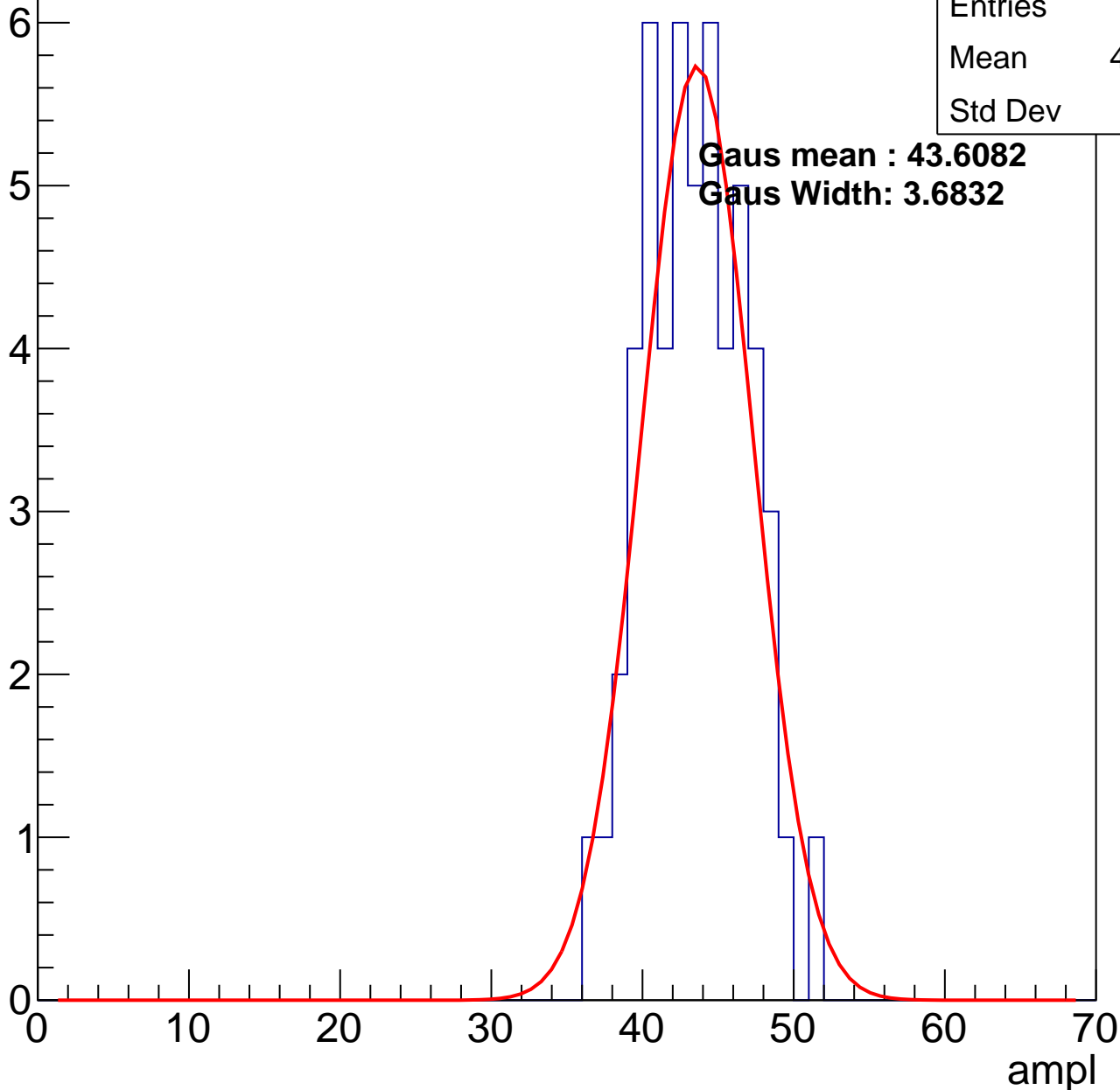
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	43.06
Std Dev	3.31

**Gaus mean : 43.6082**

**Gaus Width: 3.6832**

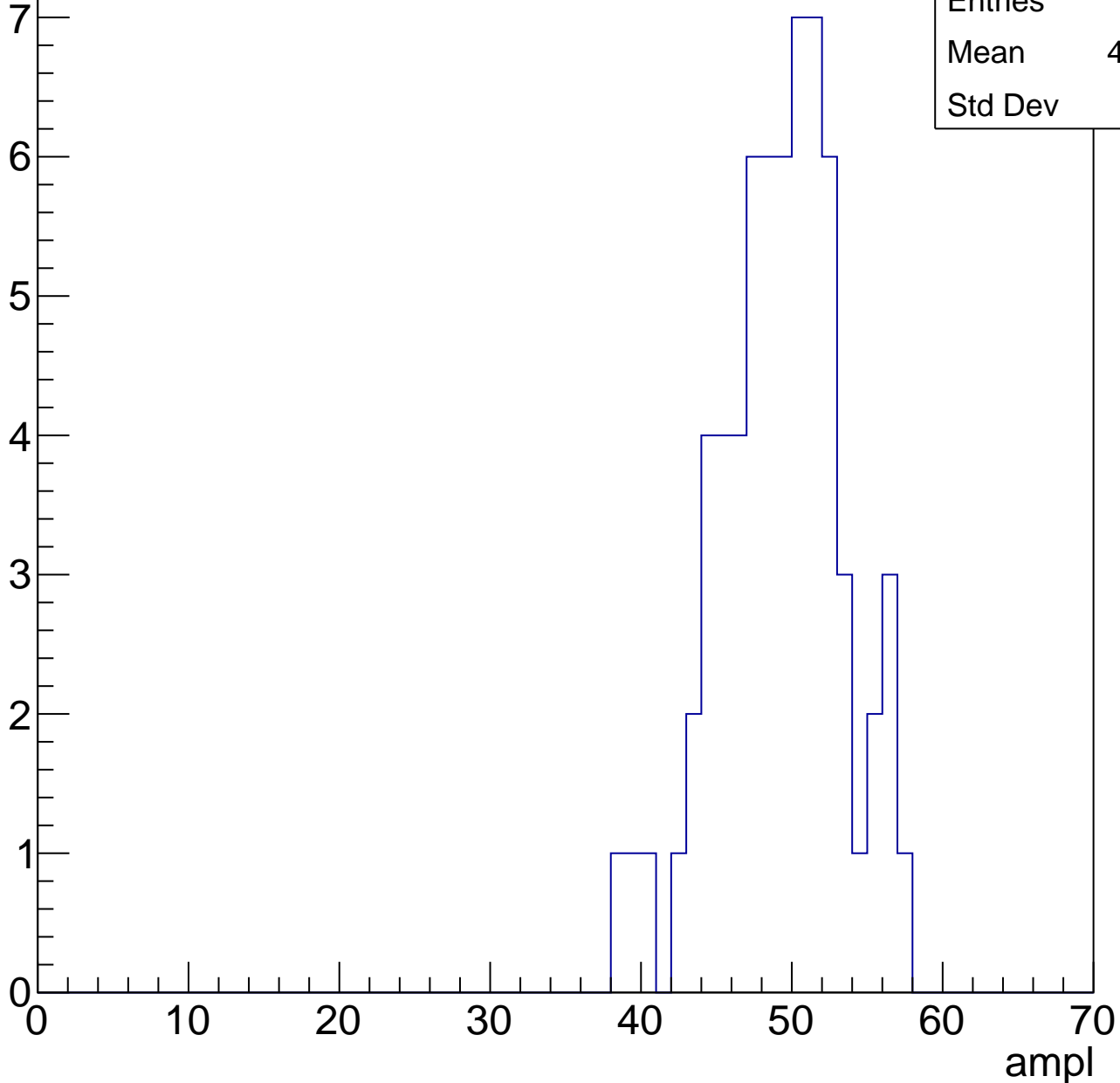


# B1L102S, U3-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	48.73
Std Dev	4.07

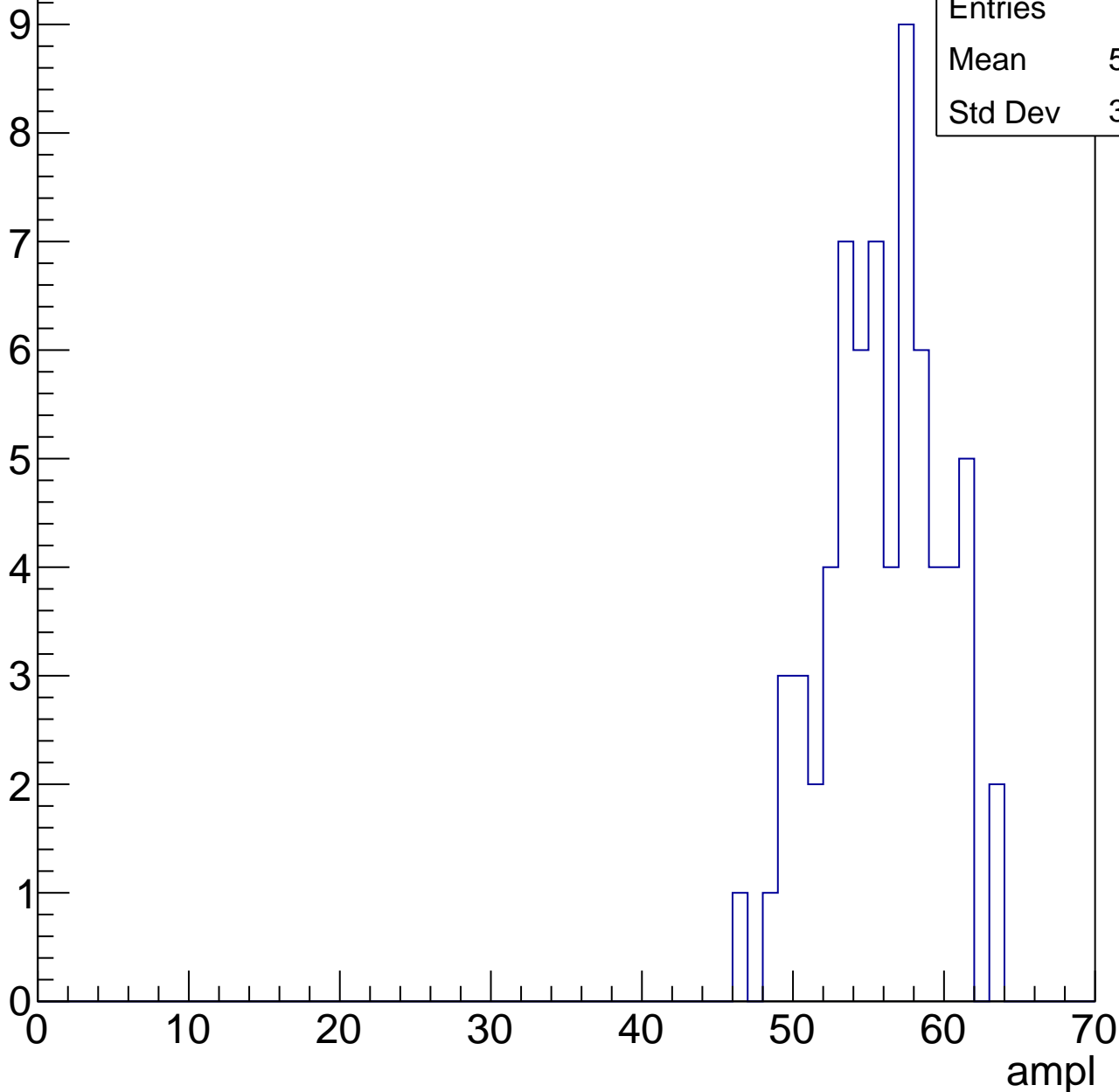


# B1L102S, U3-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	55.49
Std Dev	3.767

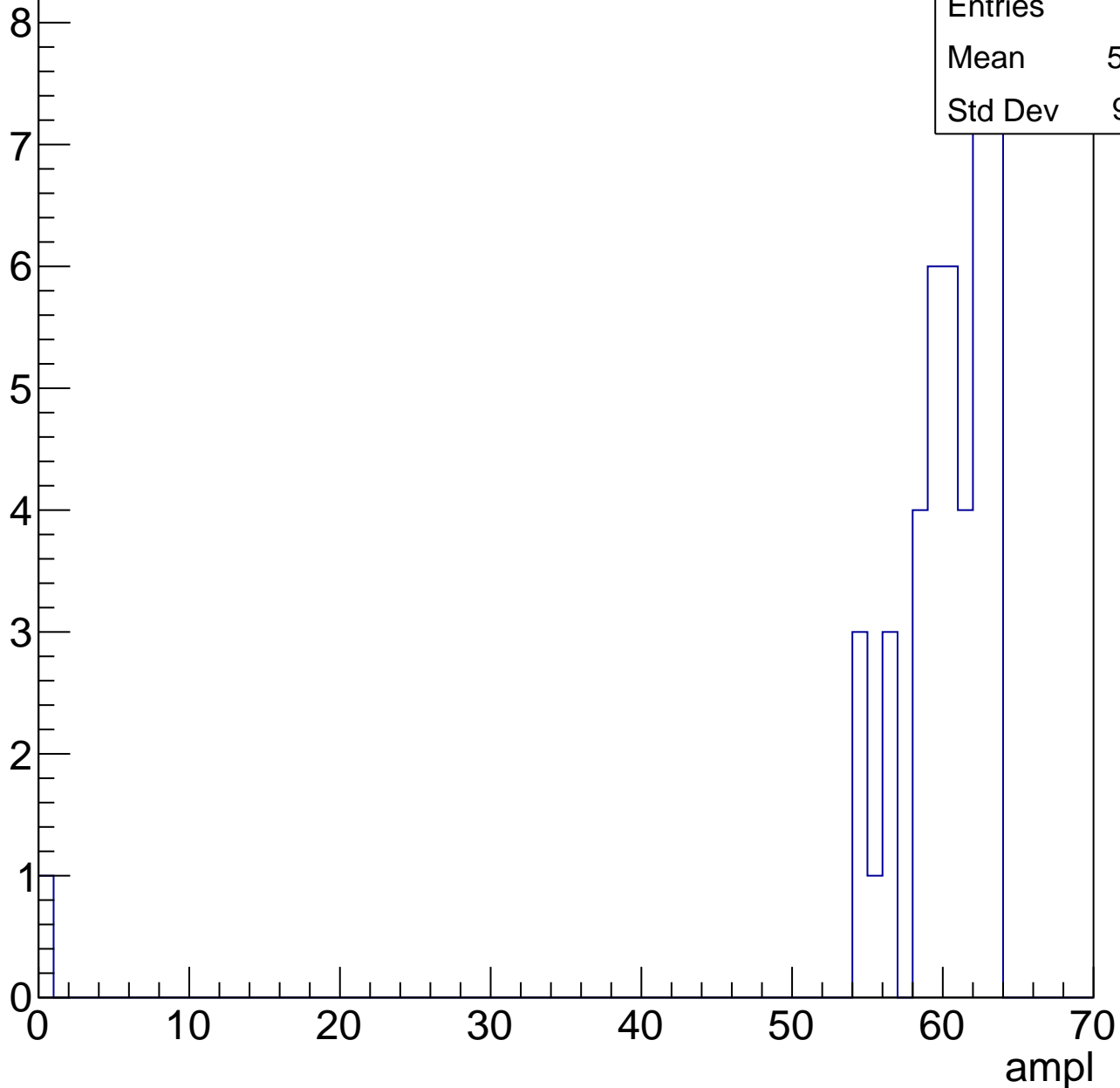


# B1L102S, U3-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	44
Mean	58.52
Std Dev	9.311



# B1L102S, U3-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

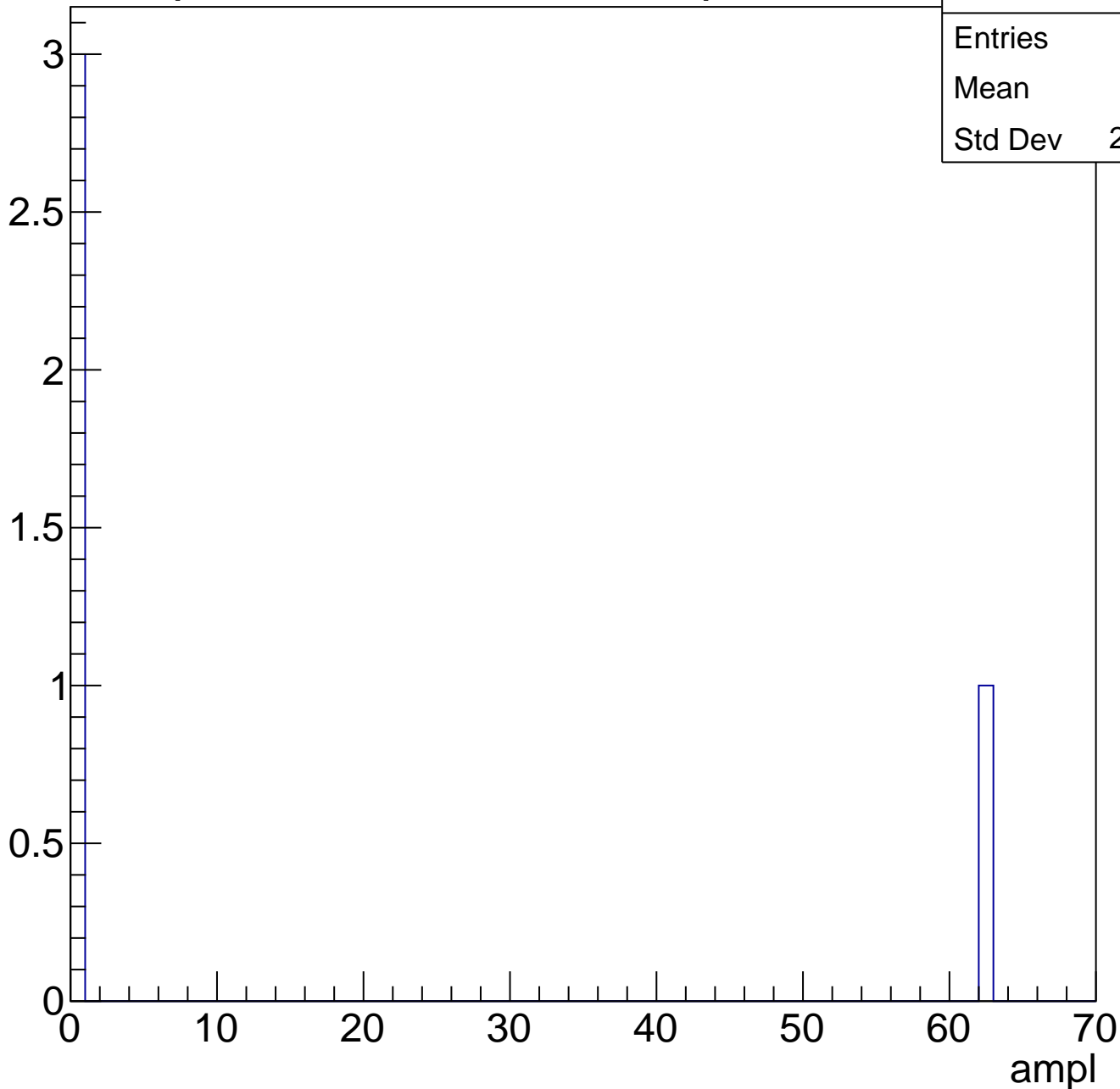




# B1L102S, U3-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch112, adc0

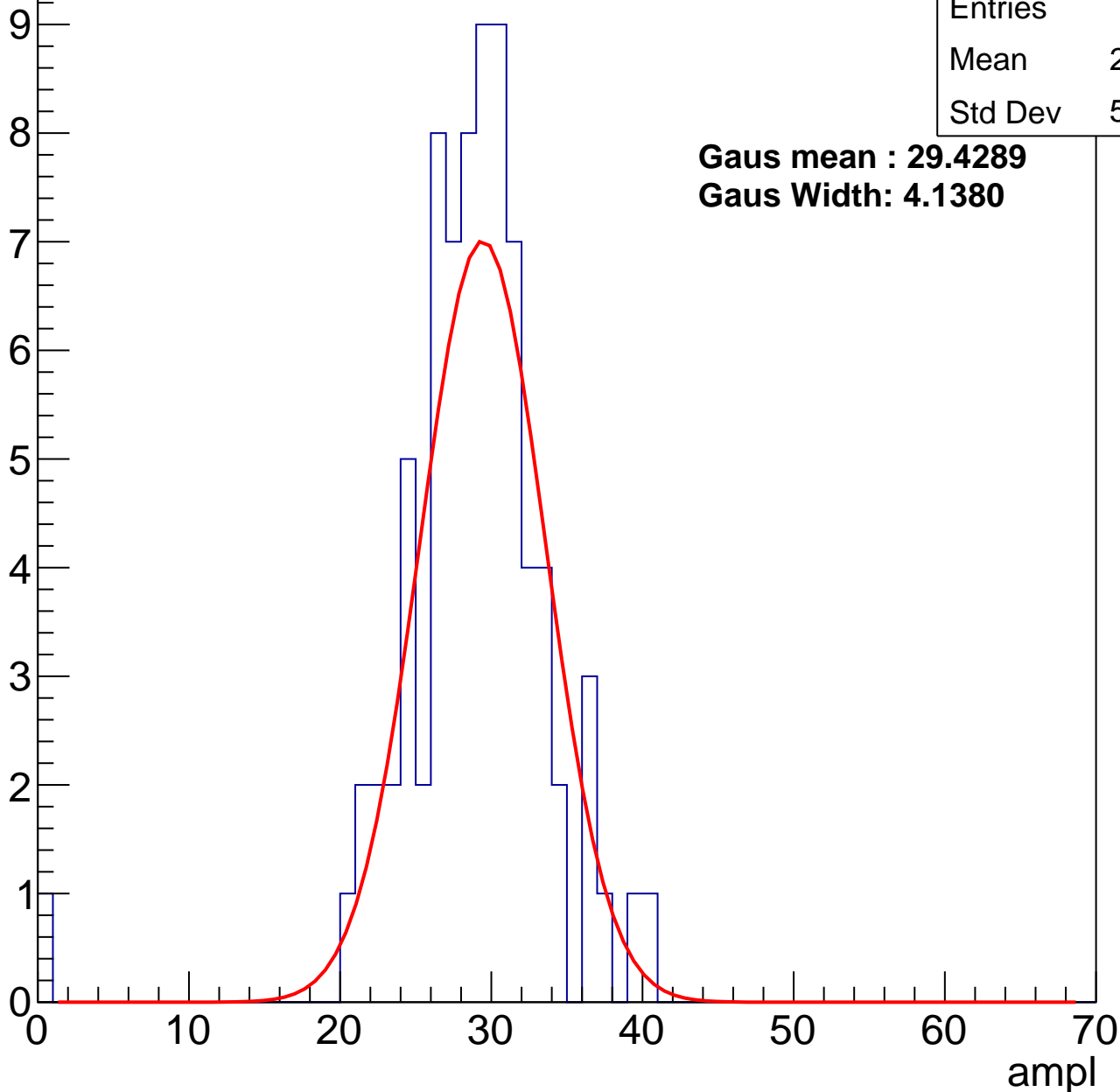
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	28.39
Std Dev	5.125

**Gaus mean : 29.4289**

**Gaus Width: 4.1380**



# B1L102S, U3-ch112, adc1

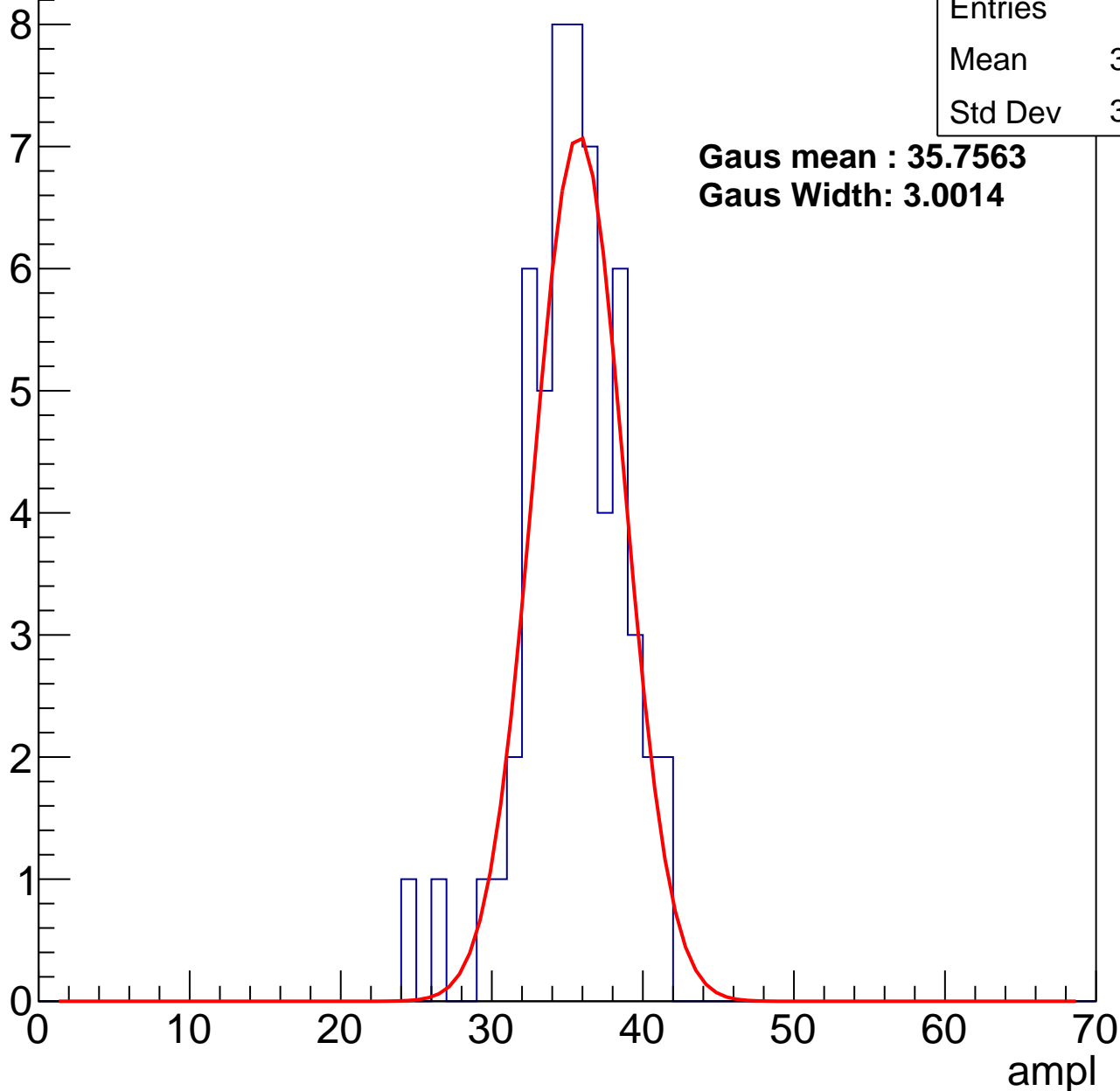
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	34.86
Std Dev	3.306

**Gaus mean : 35.7563**

**Gaus Width: 3.0014**



# B1L102S, U3-ch112, adc2

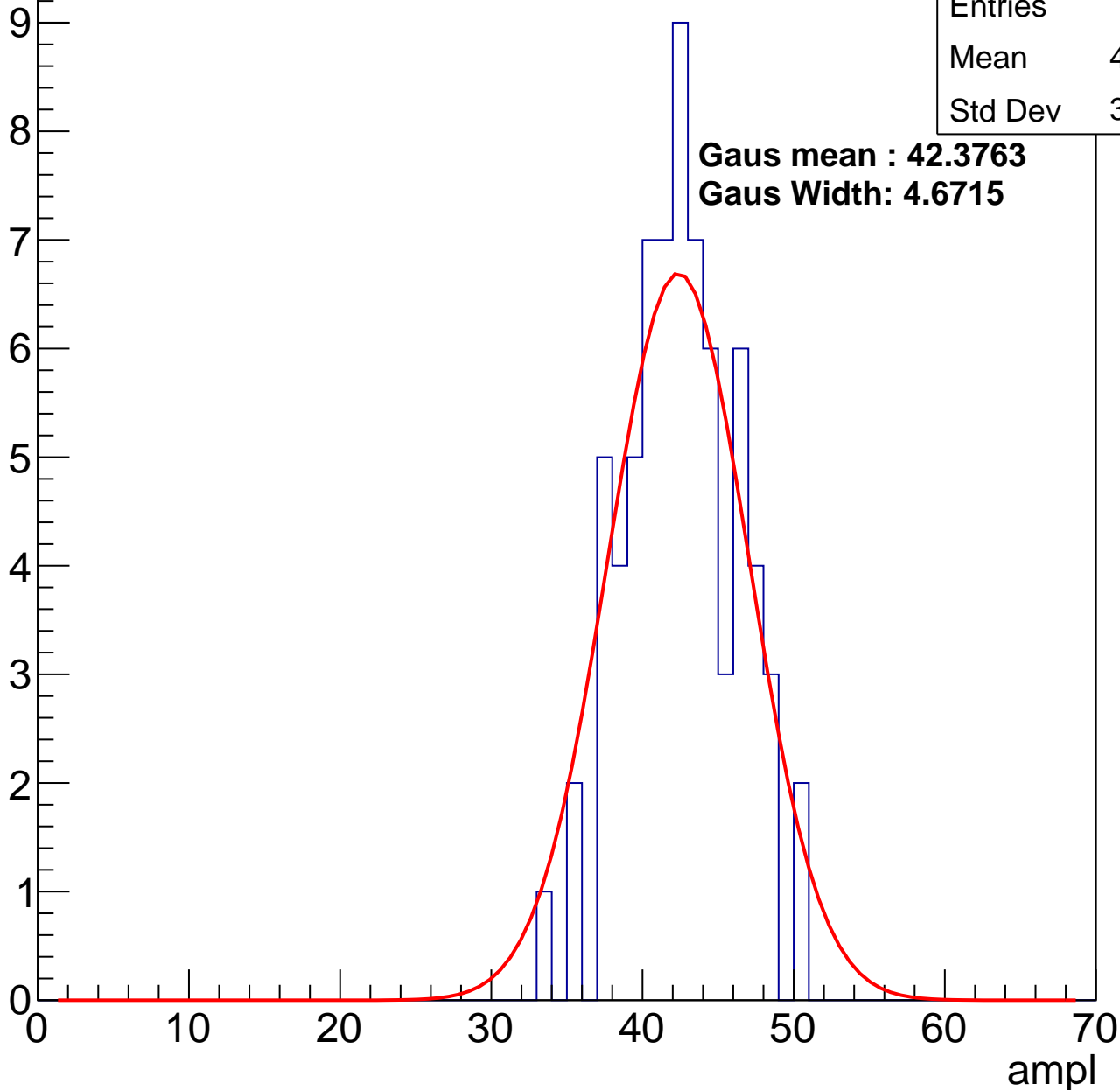
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	42.08
Std Dev	3.634

**Gaus mean : 42.3763**

**Gaus Width: 4.6715**

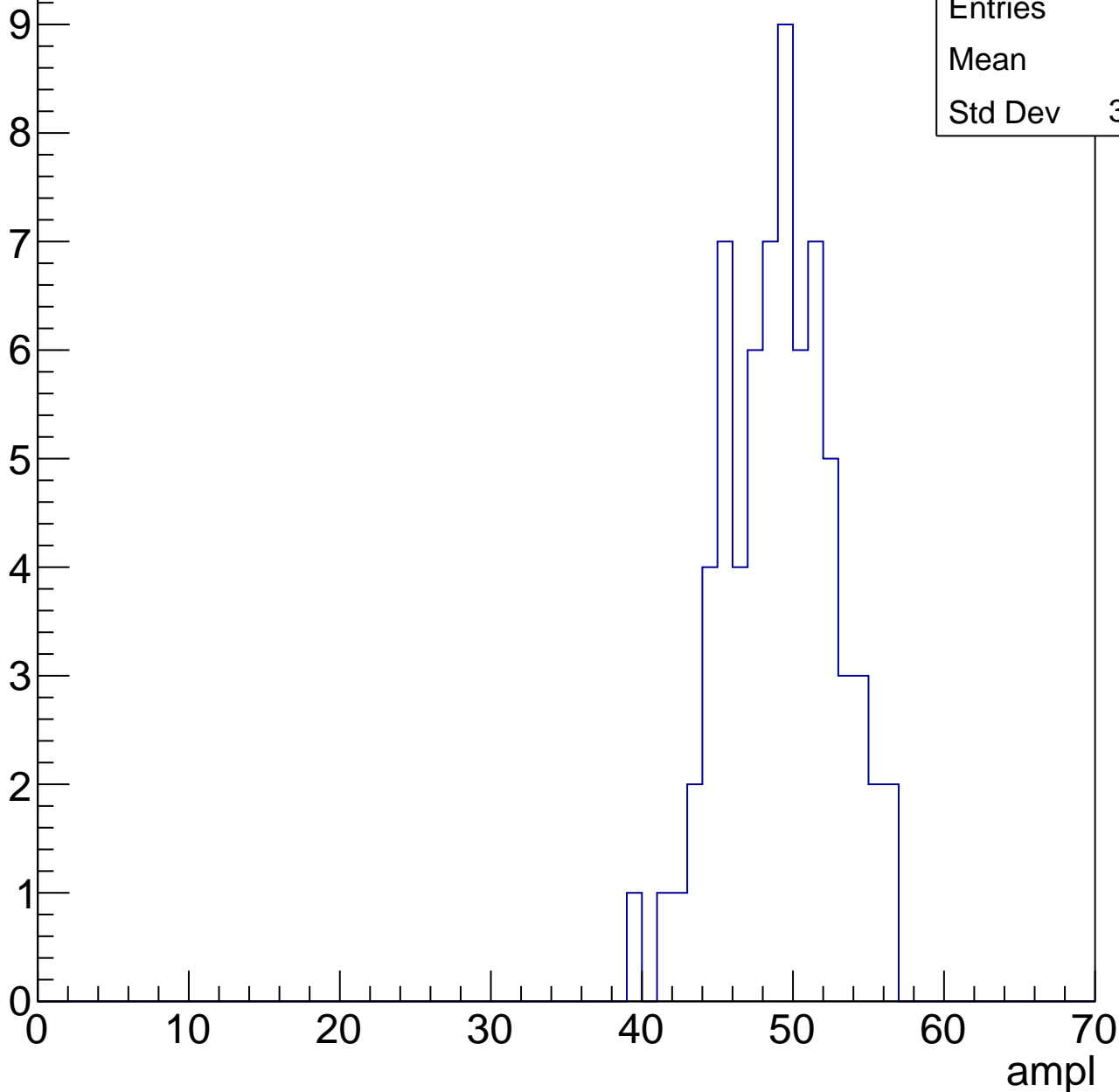


# B1L102S, U3-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	48.6
Std Dev	3.635

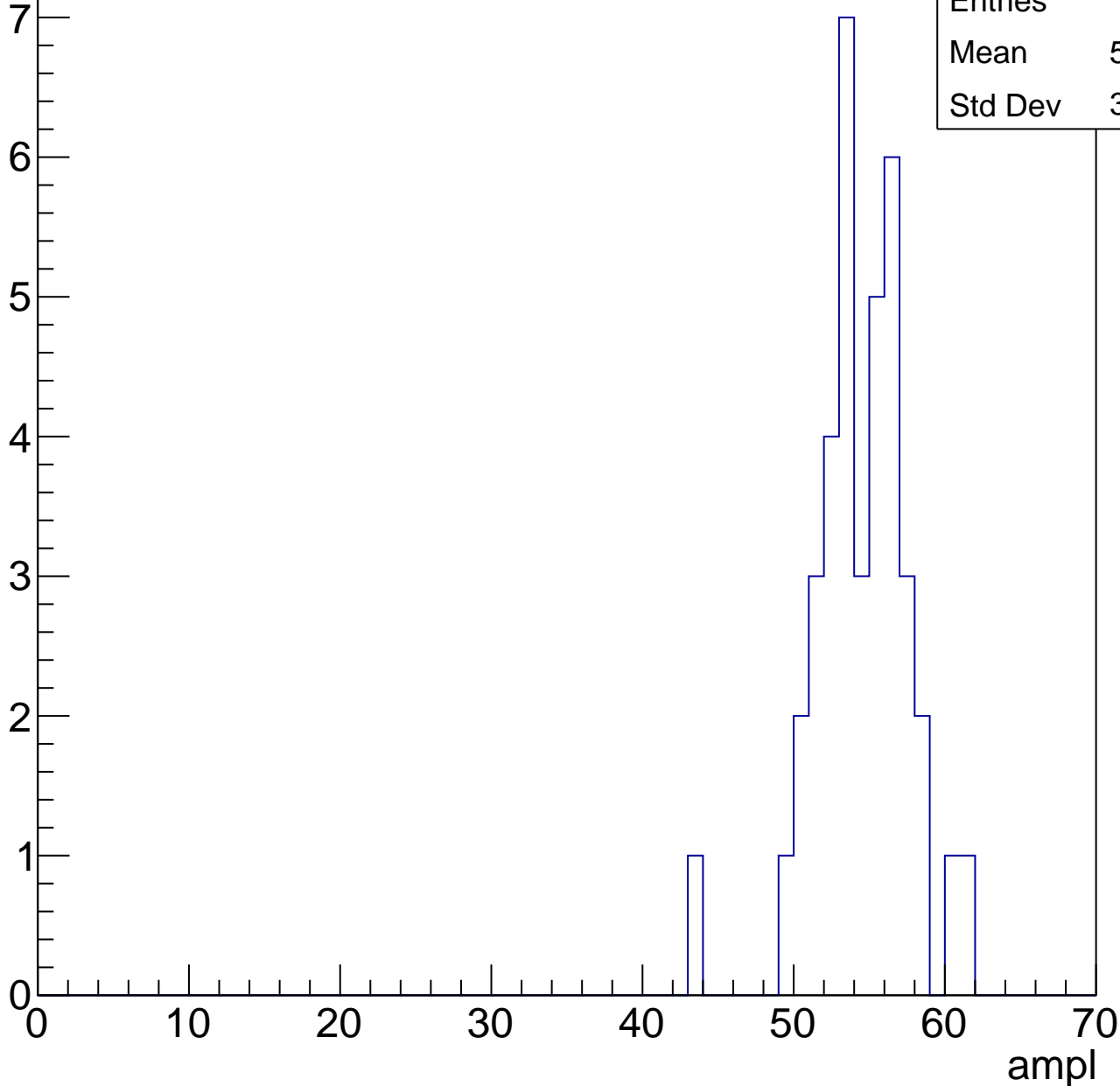


# B1L102S, U3-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	39
Mean	53.97
Std Dev	3.206

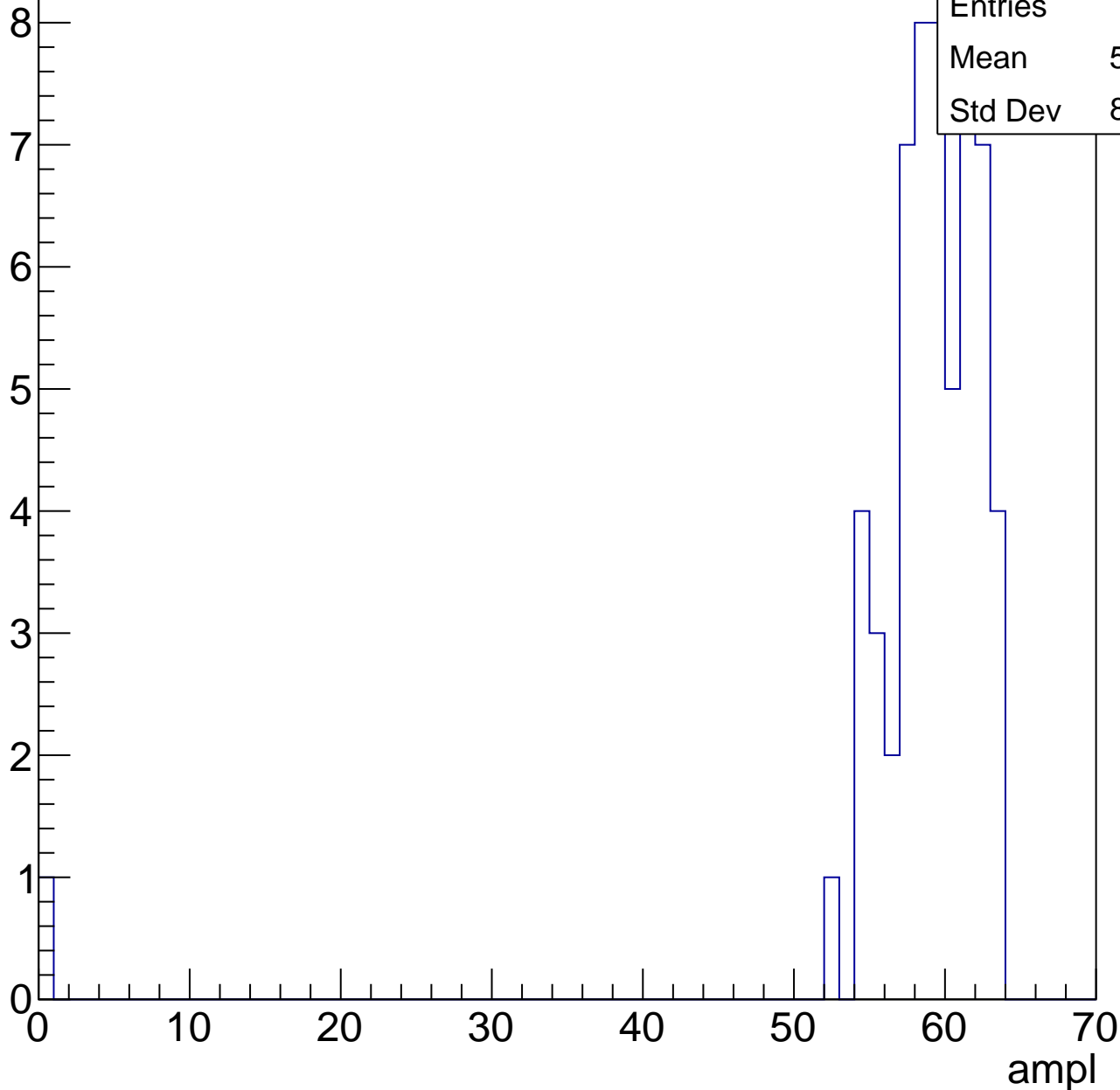


# B1L102S, U3-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	57.83
Std Dev	8.112

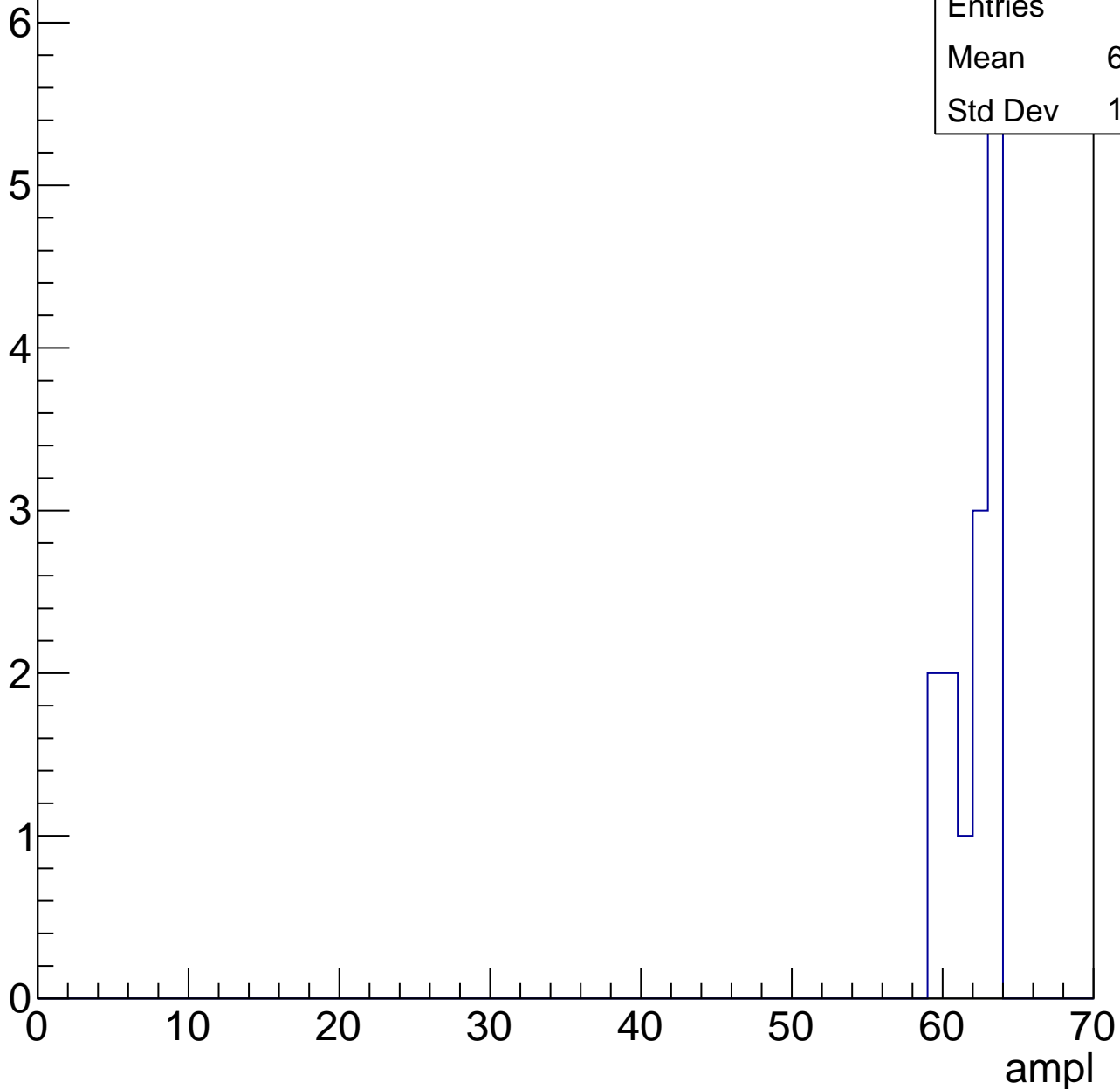


# B1L102S, U3-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	14
Mean	61.64
Std Dev	1.493

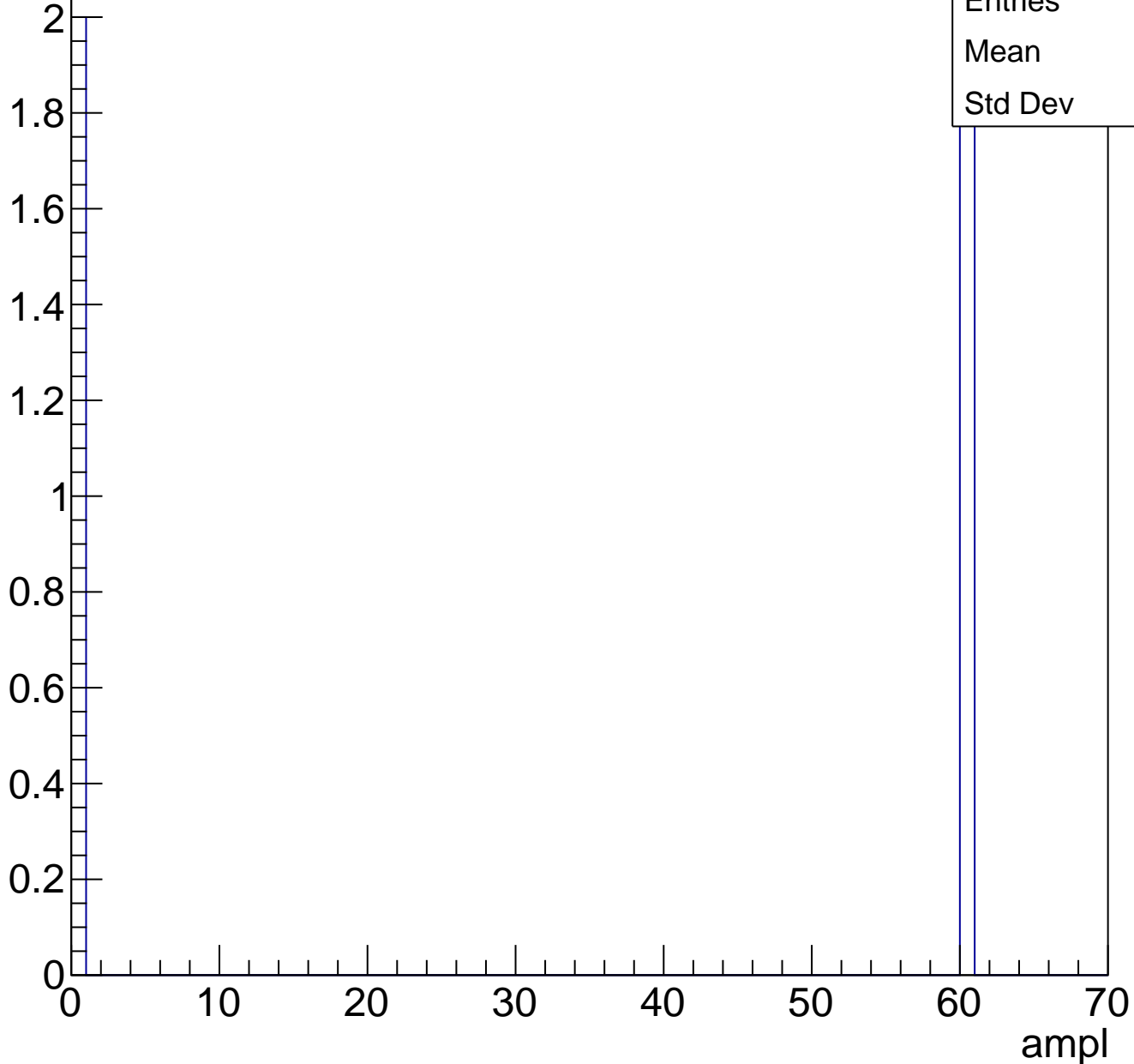




# B1L102S, U3-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch113, adc0

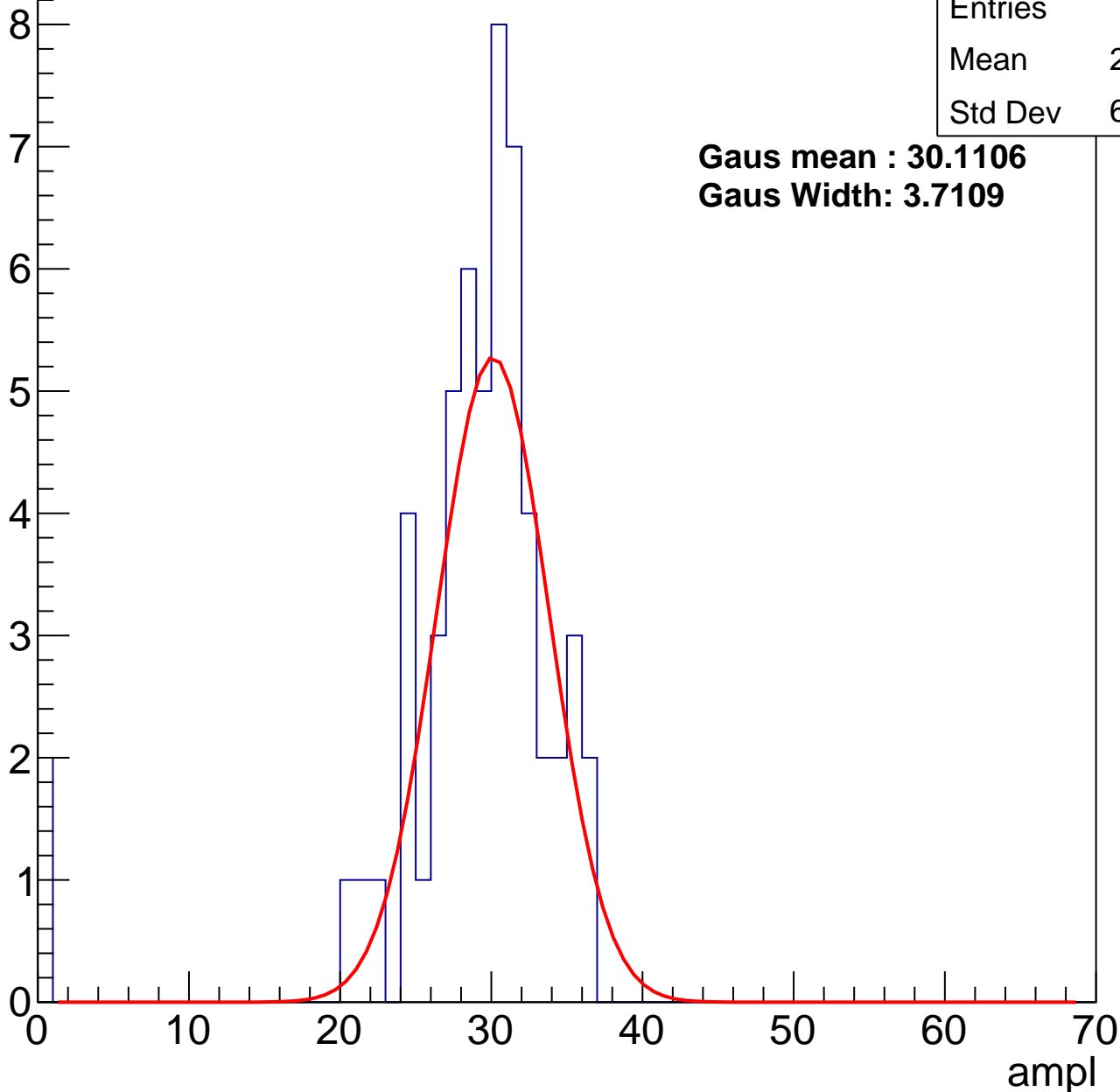
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	28.18
Std Dev	6.443

**Gaus mean : 30.1106**

**Gaus Width: 3.7109**



# B1L102S, U3-ch113, adc1

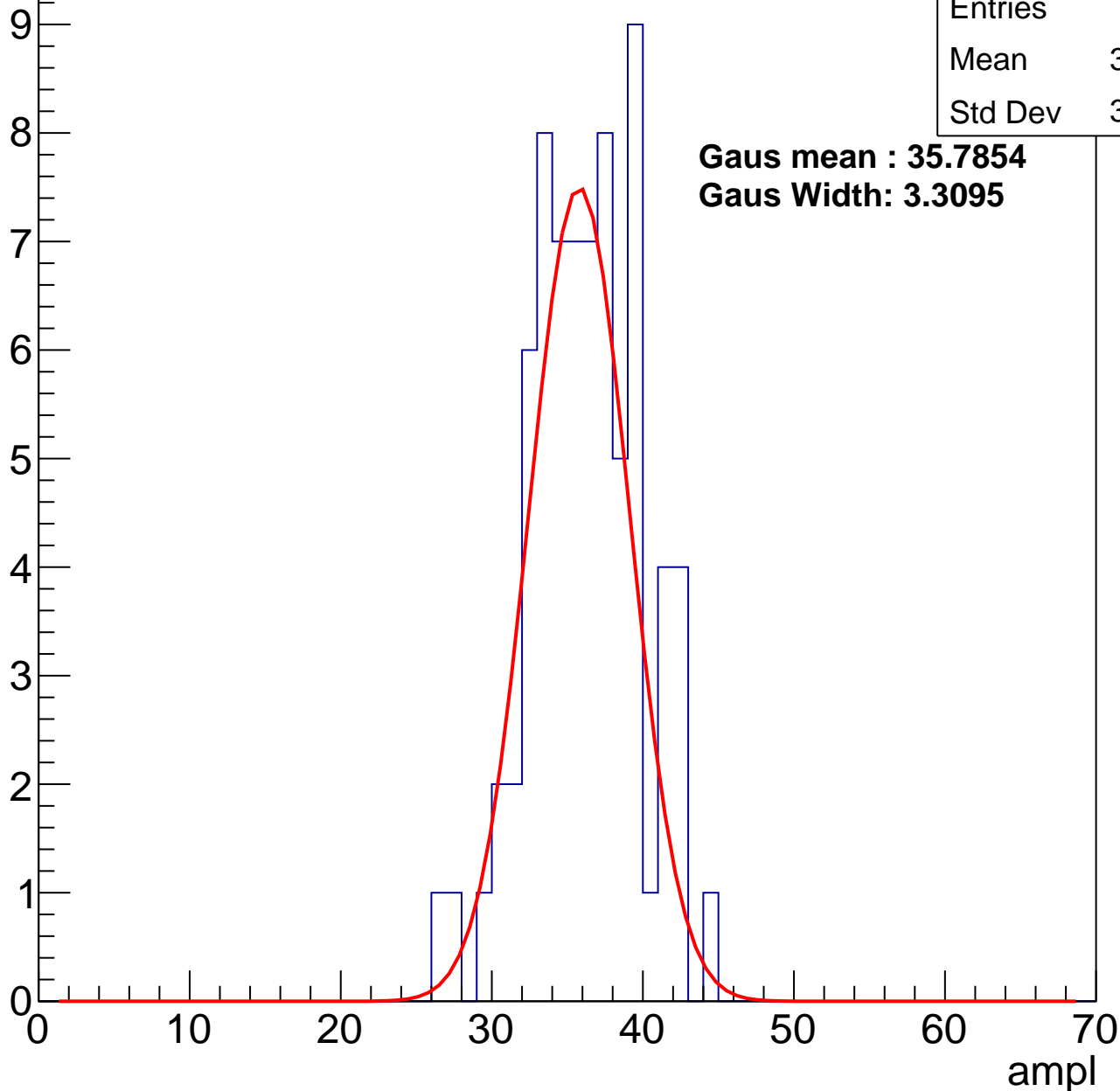
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	35.78
Std Dev	3.648

**Gaus mean : 35.7854**

**Gaus Width: 3.3095**



# B1L102S, U3-ch113, adc2

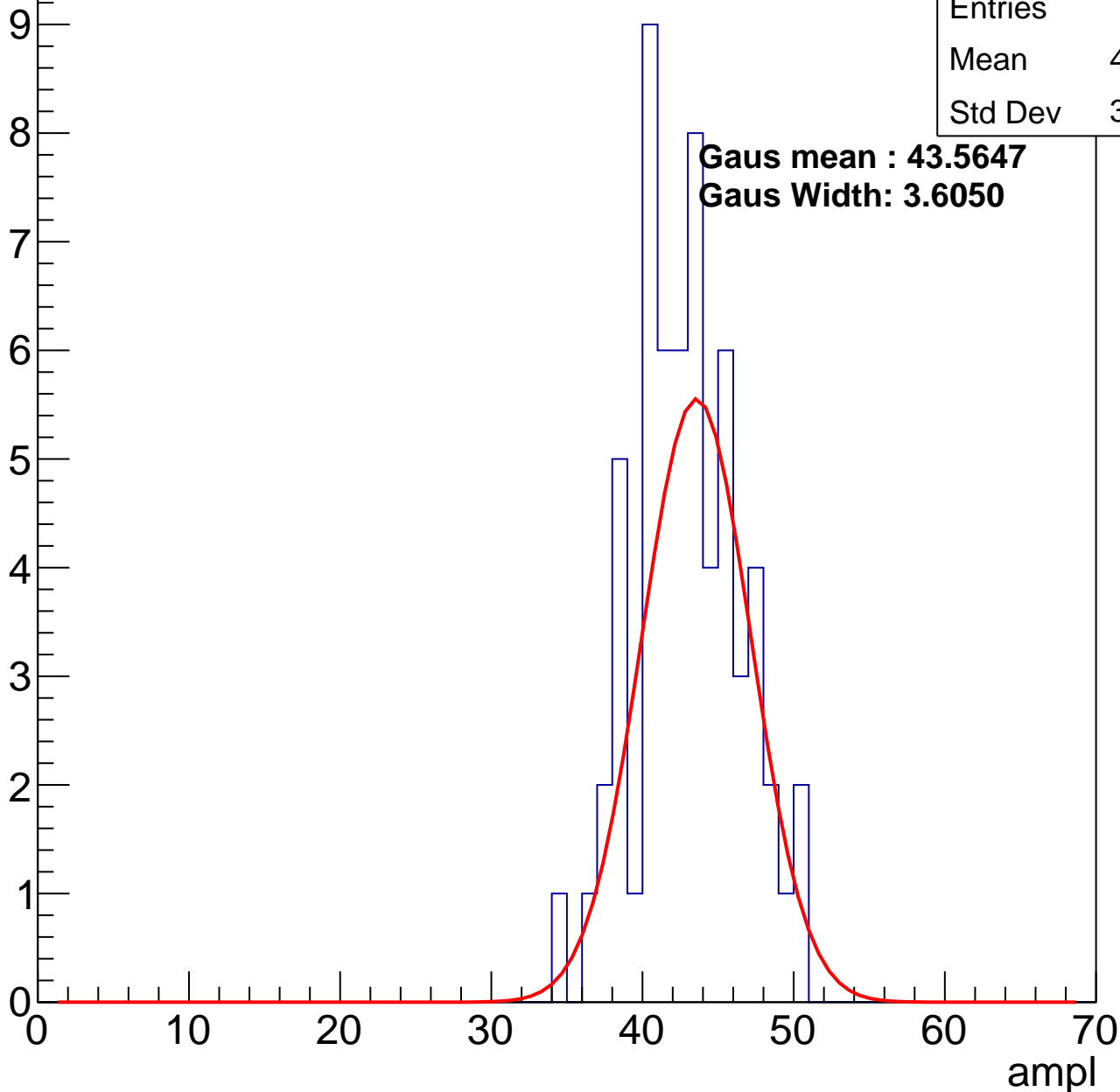
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	42.49
Std Dev	3.486

**Gaus mean : 43.5647**

**Gaus Width: 3.6050**

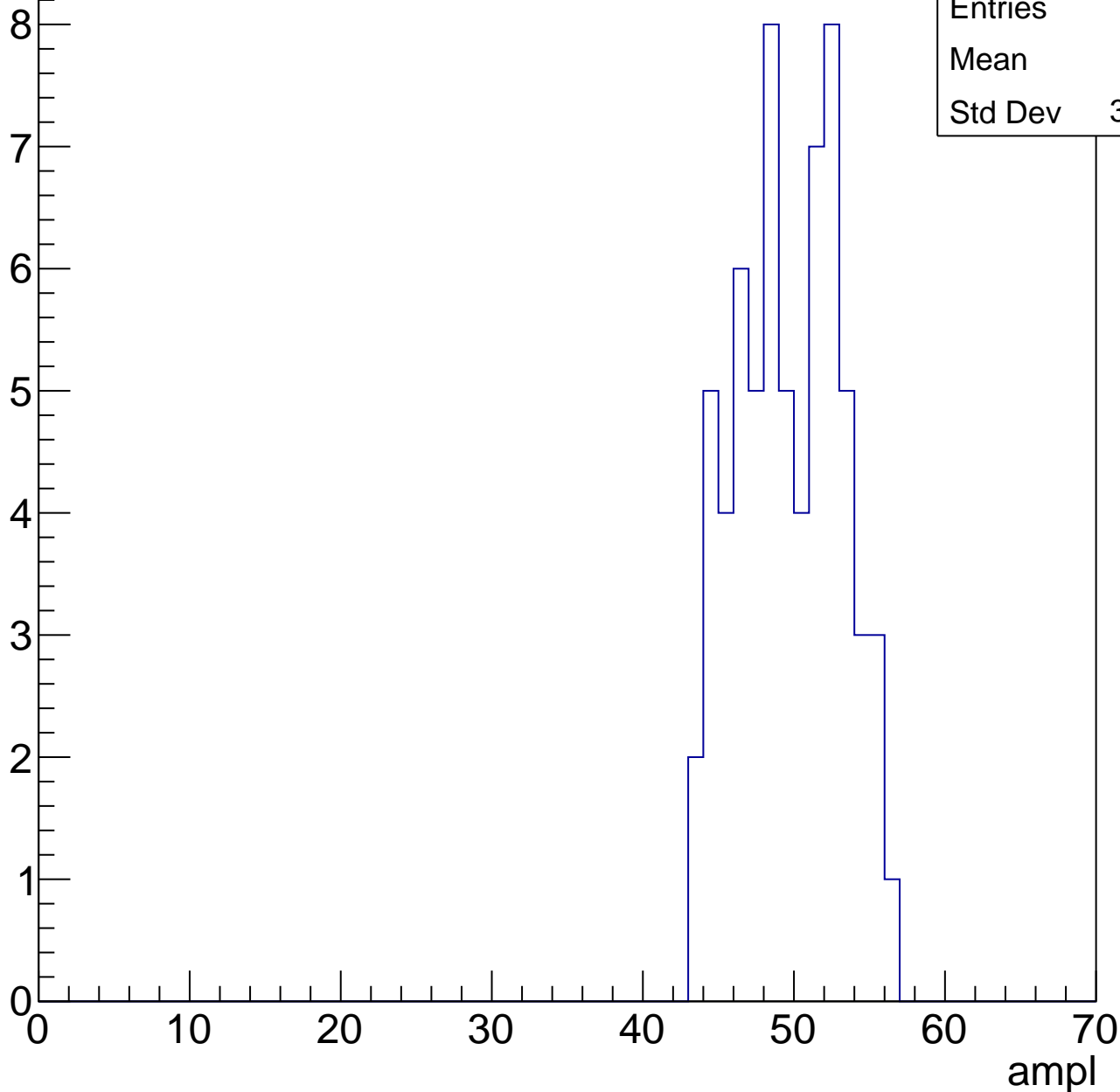


# B1L102S, U3-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	49.2
Std Dev	3.385

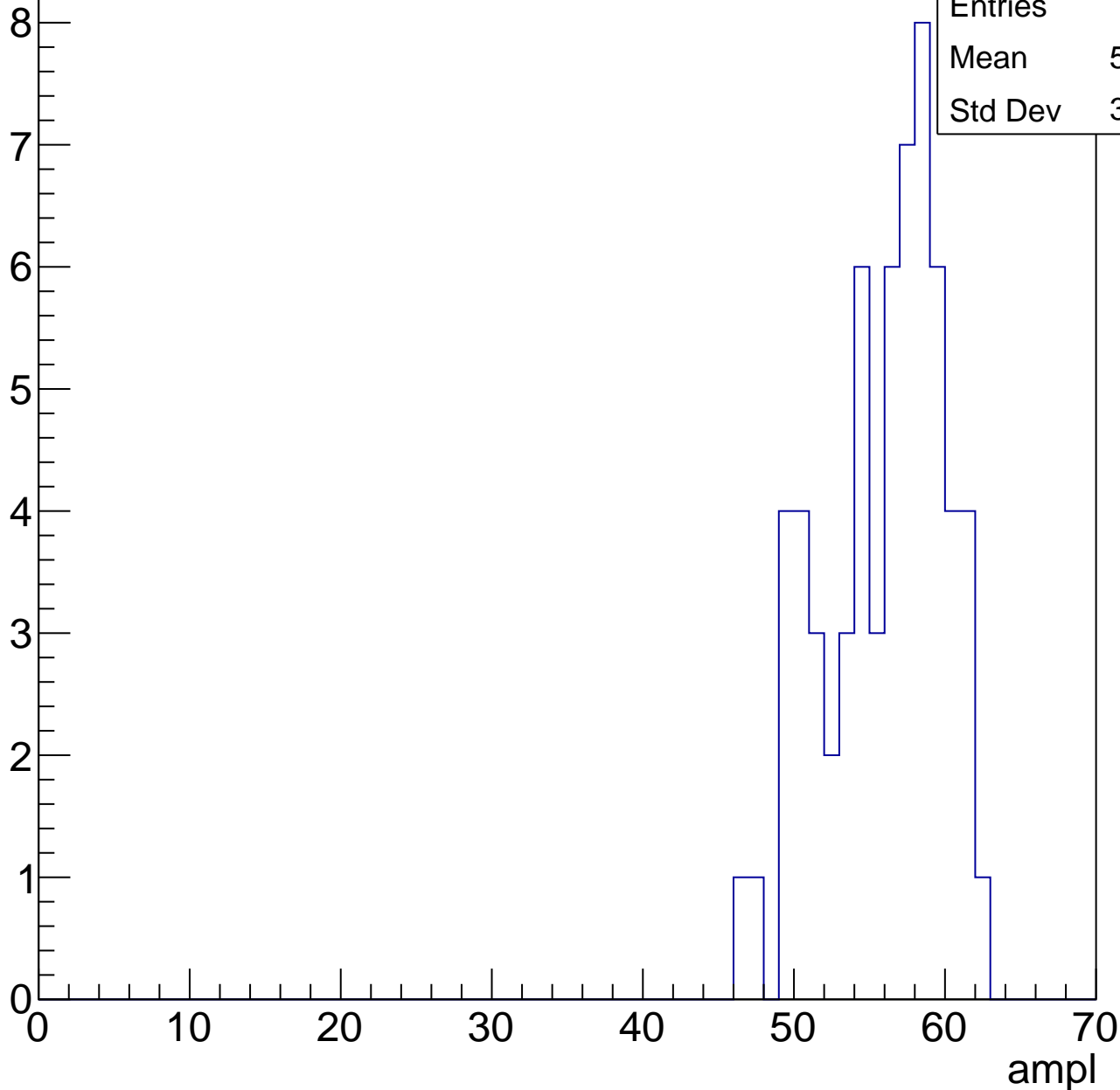


# B1L102S, U3-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	55.44
Std Dev	3.895

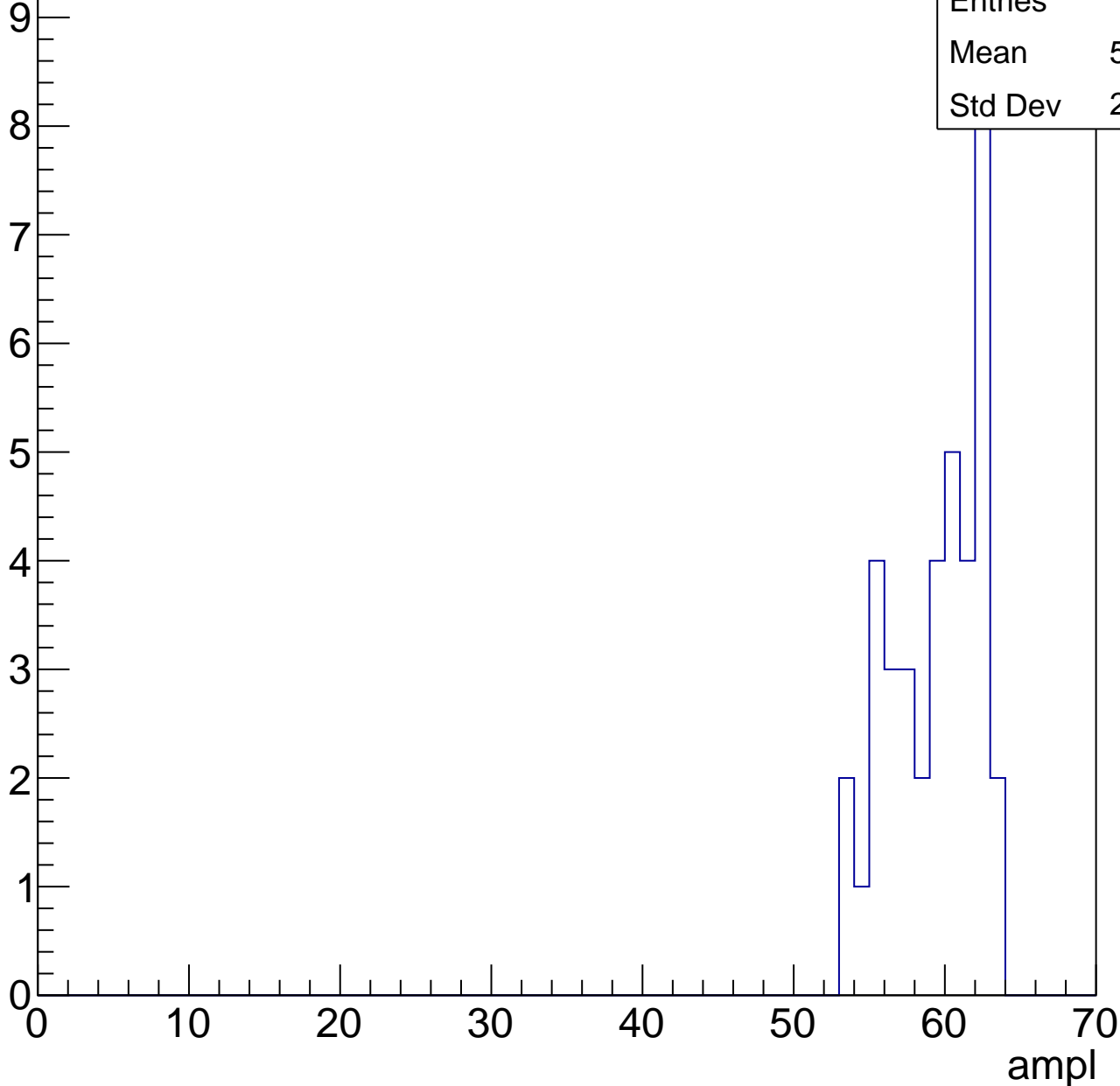


# B1L102S, U3-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	39
Mean	58.95
Std Dev	2.935

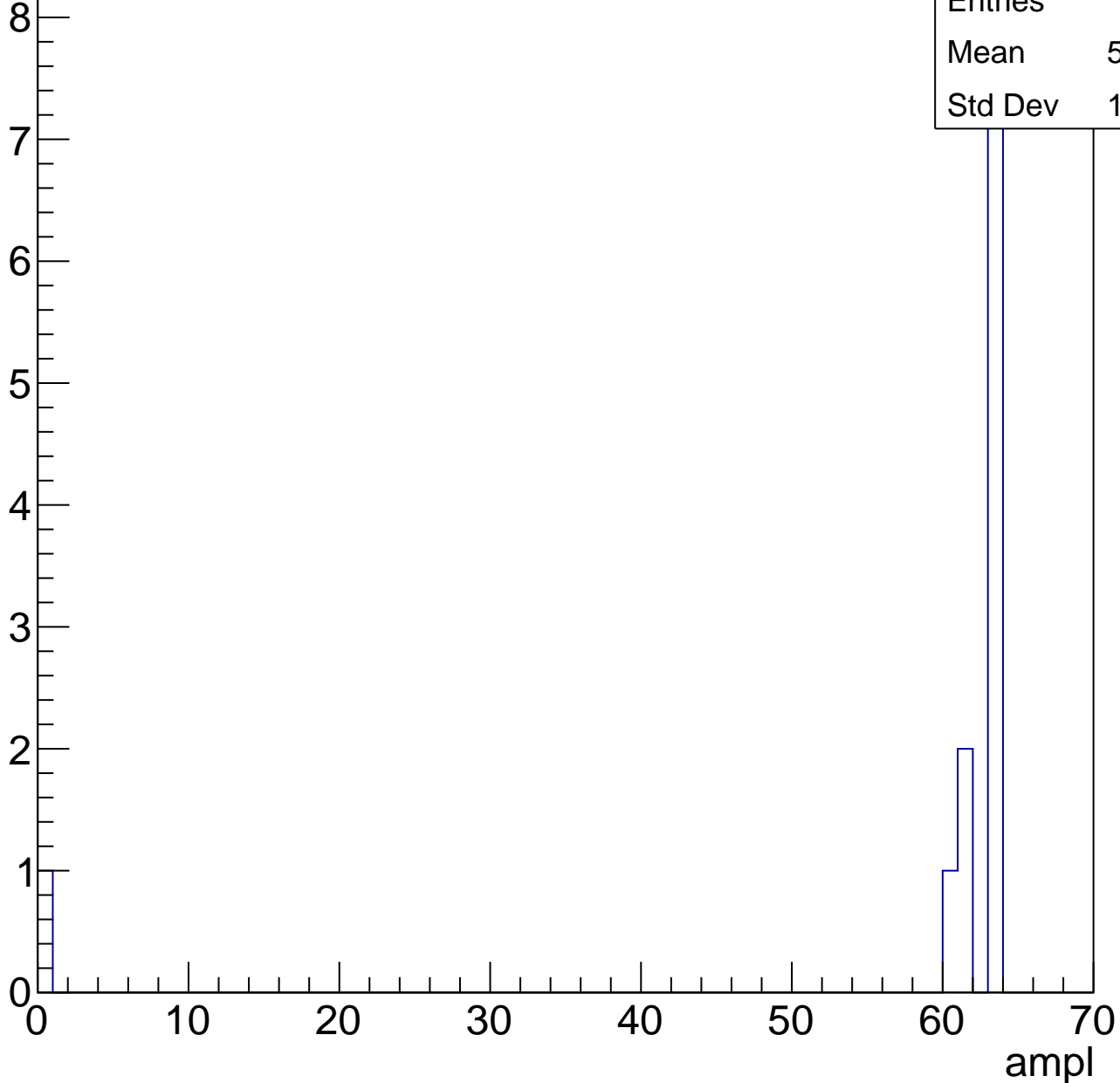


# B1L102S, U3-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	12
Mean	57.17
Std Dev	17.27





# B1L102S, U3-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U3-ch114, adc0

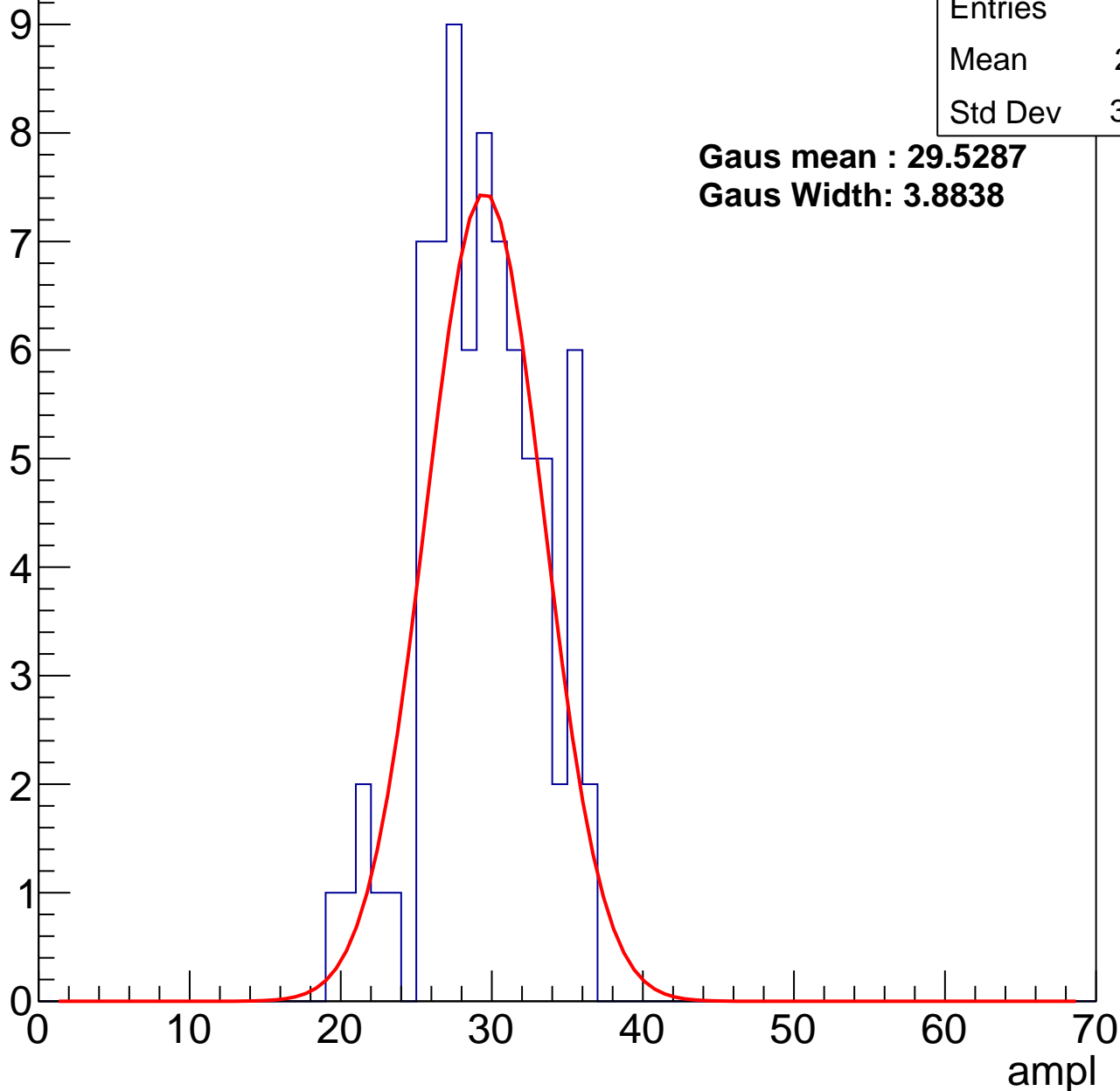
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	28.91
Std Dev	3.857

**Gaus mean : 29.5287**

**Gaus Width: 3.8838**



# B1L102S, U3-ch114, adc1

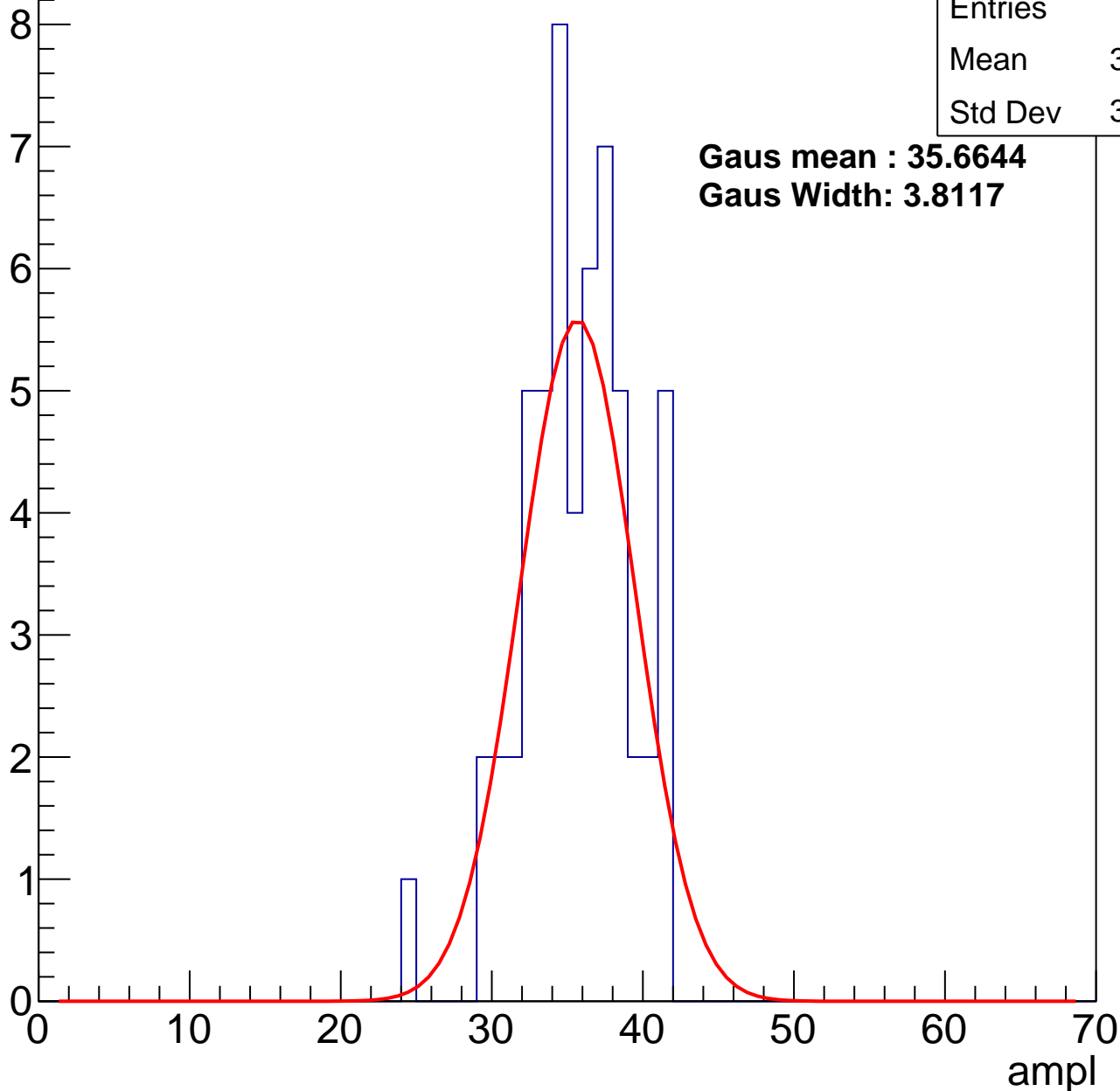
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	35.16
Std Dev	3.504

**Gaus mean : 35.6644**

**Gaus Width: 3.8117**



# B1L102S, U3-ch114, adc2

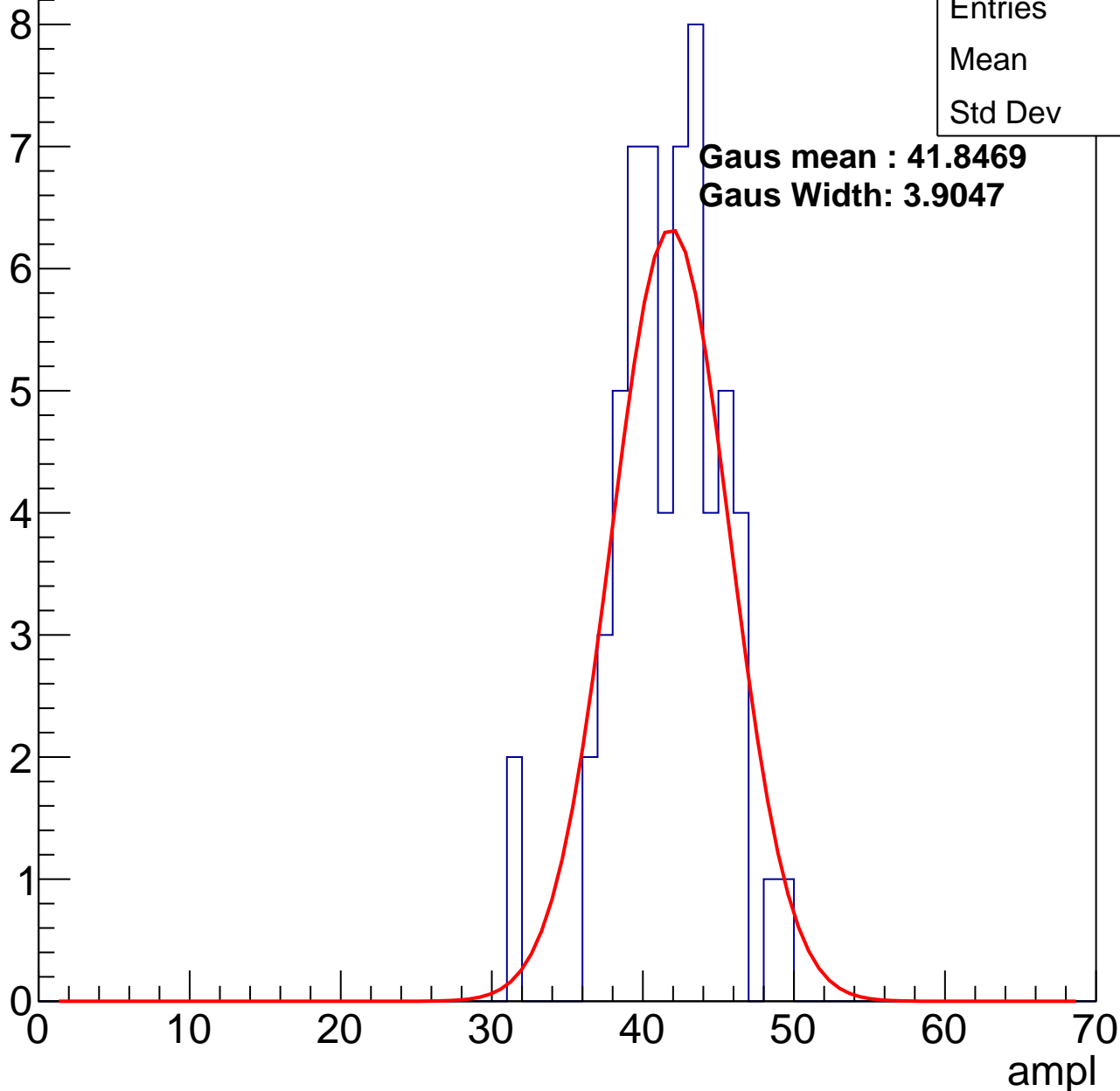
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	41.2
Std Dev	3.52

**Gaus mean : 41.8469**

**Gaus Width: 3.9047**

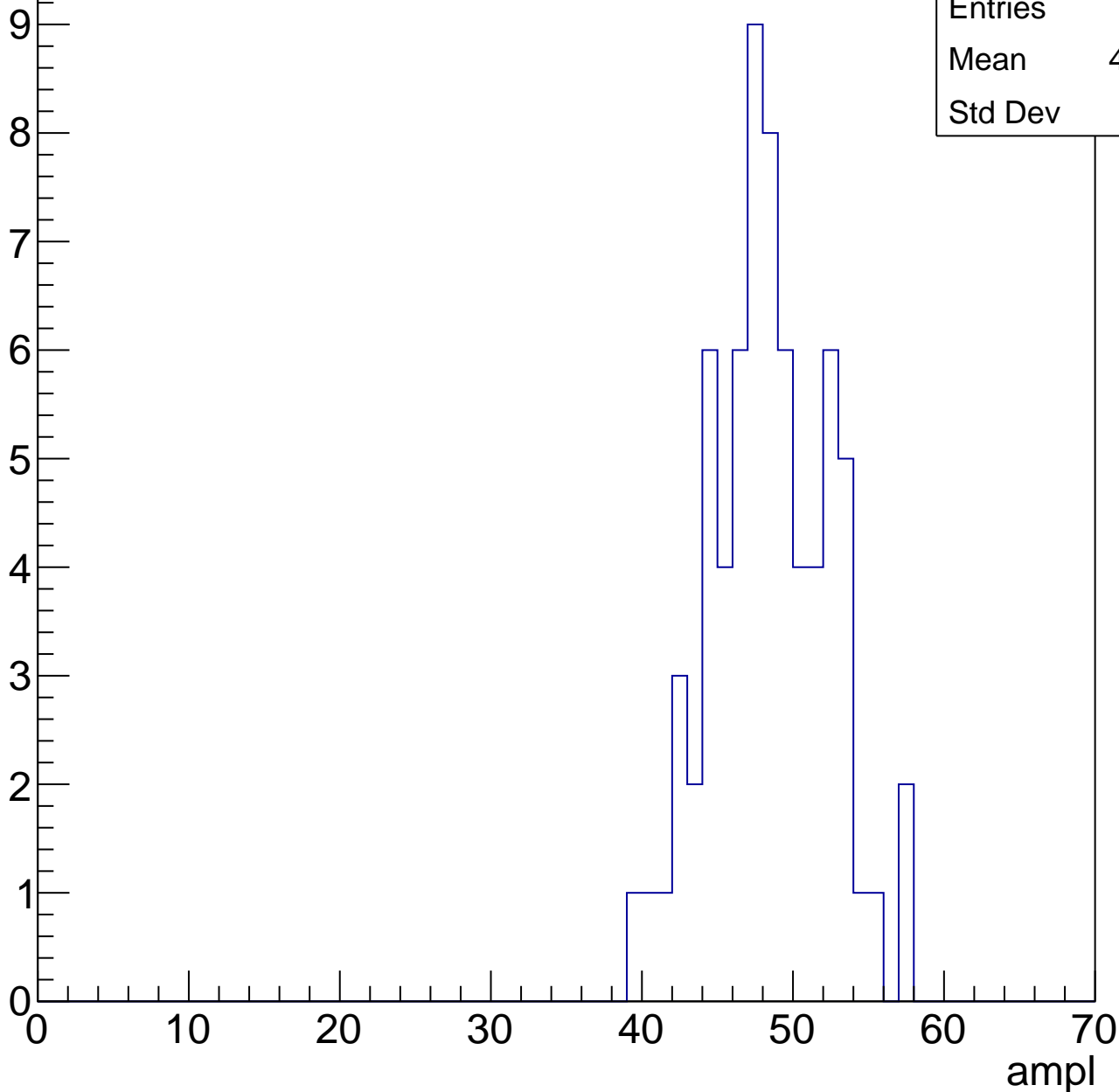


# B1L102S, U3-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	47.96
Std Dev	3.86

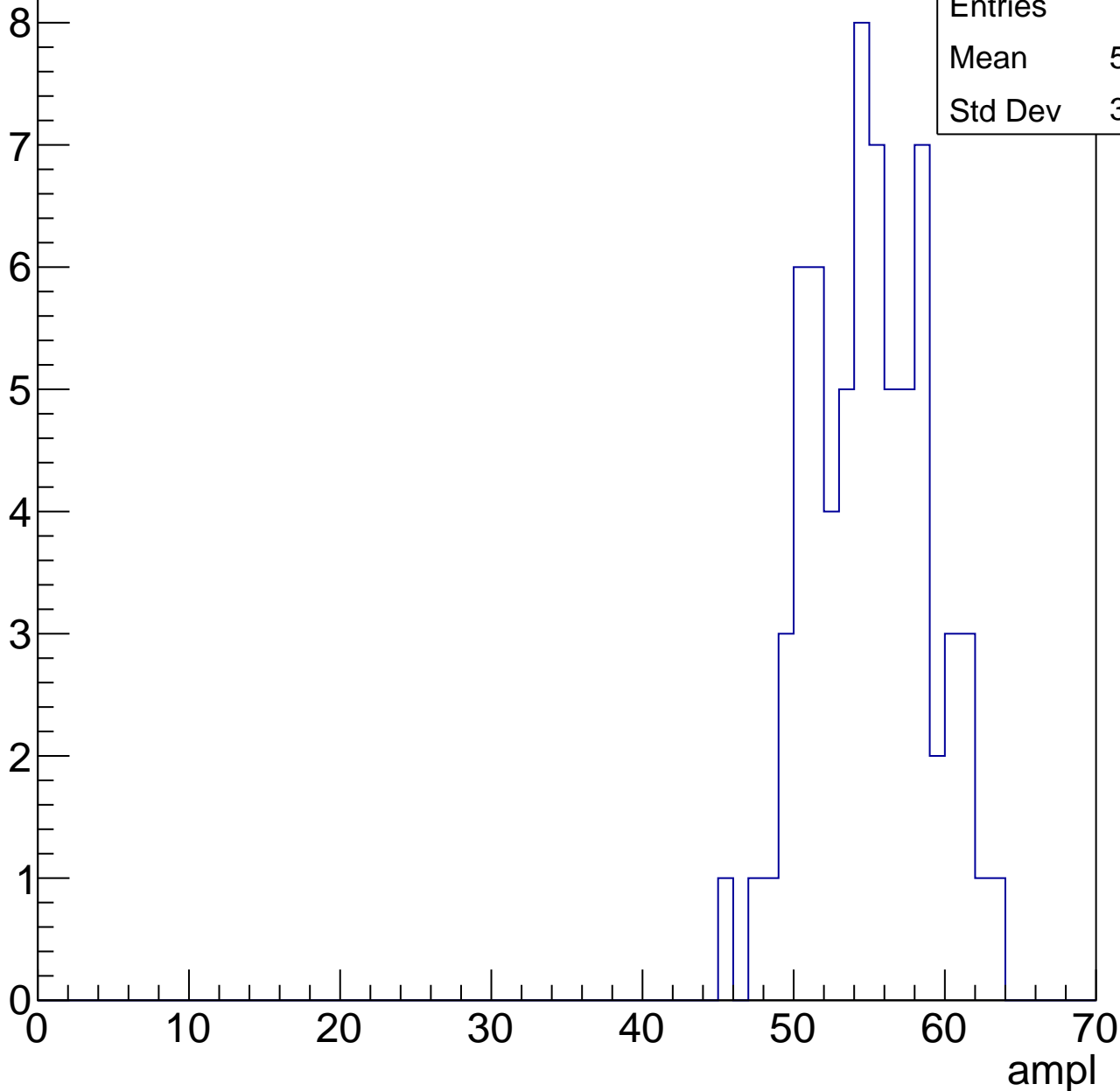


# B1L102S, U3-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	54.49
Std Dev	3.862

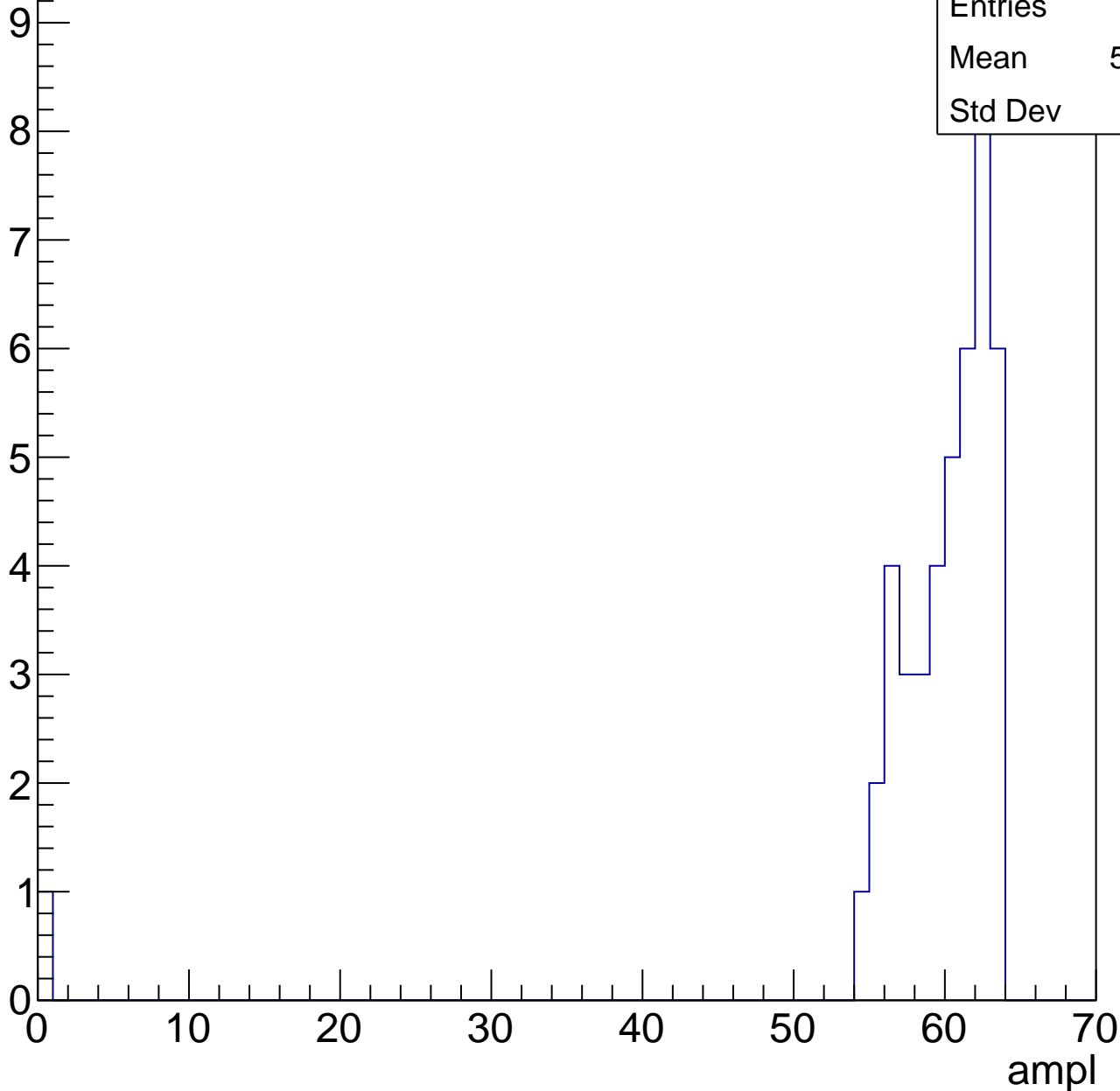


# B1L102S, U3-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

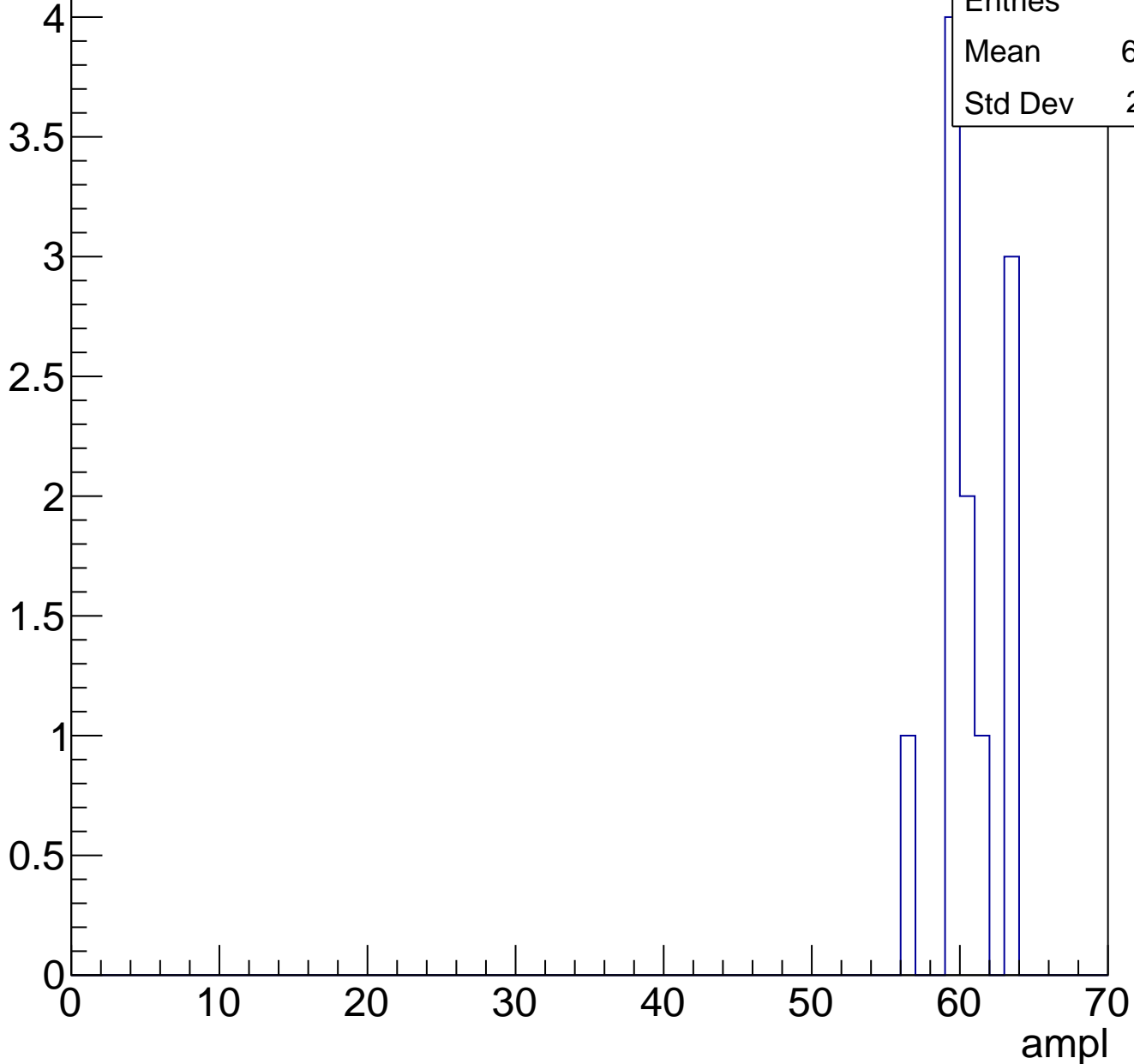
Entries	44
Mean	58.43
Std Dev	9.27



# B1L102S, U3-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch115, adc0

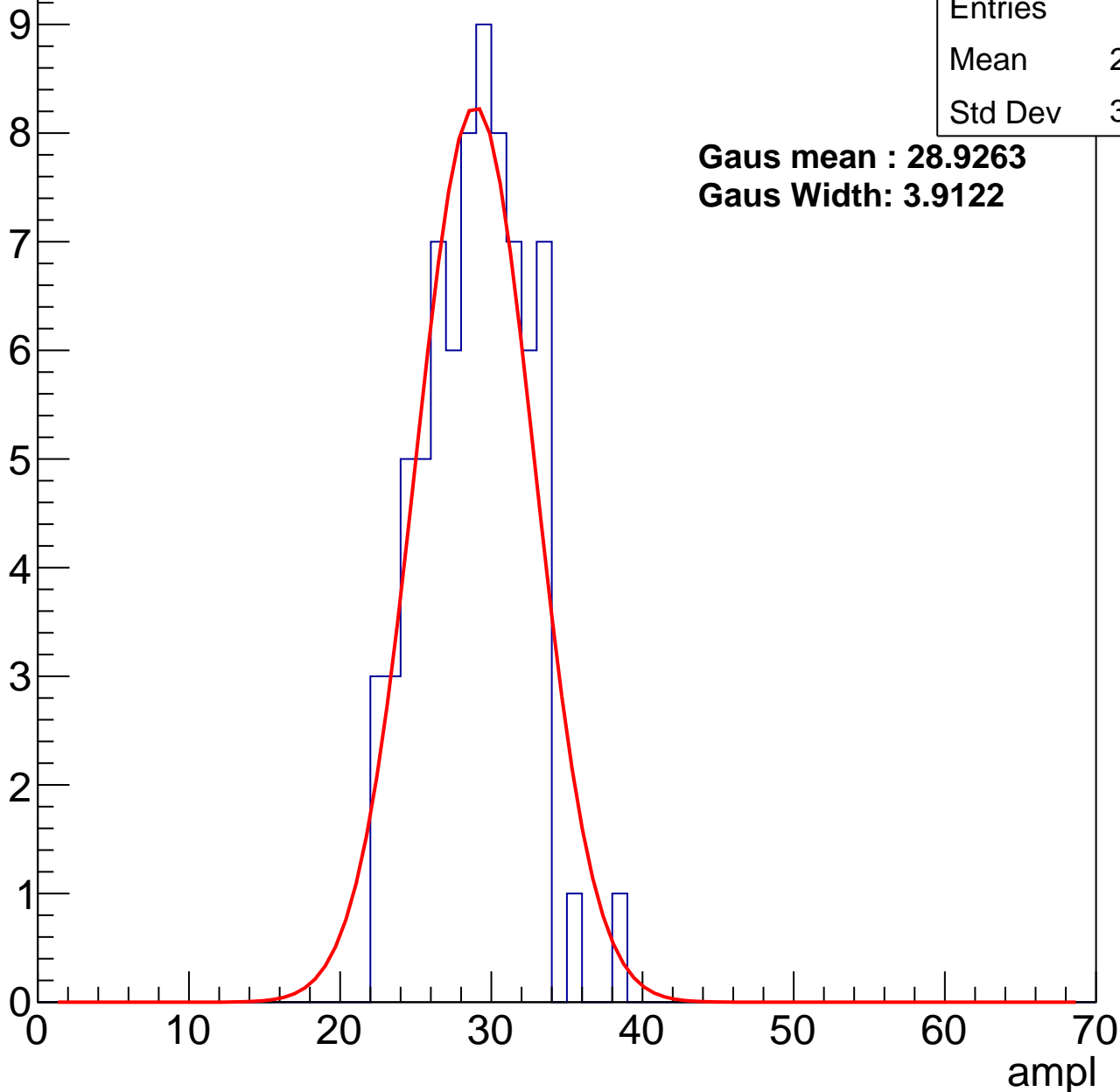
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	28.45
Std Dev	3.346

**Gaus mean : 28.9263**

**Gaus Width: 3.9122**



# B1L102S, U3-ch115, adc1

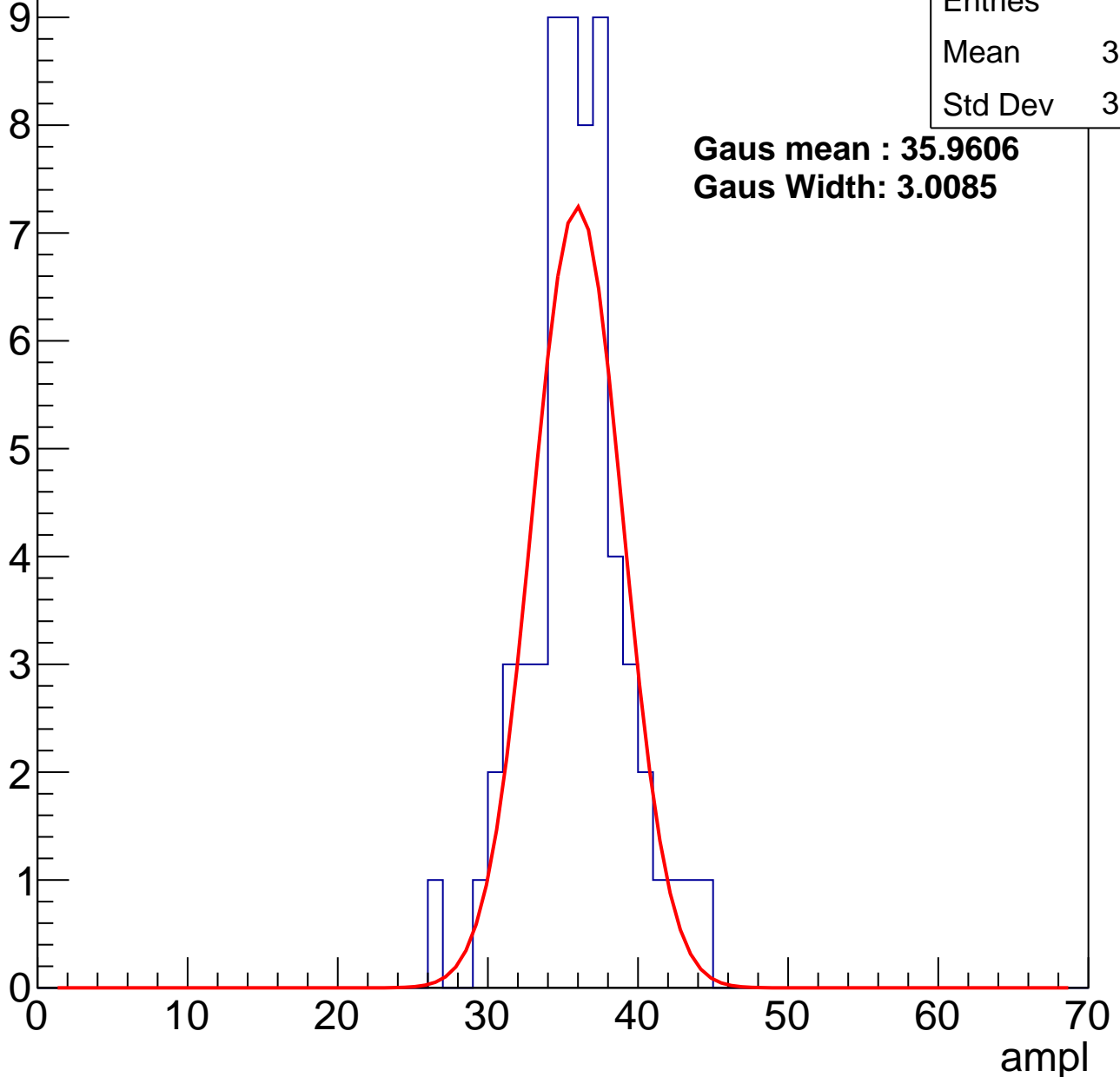
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	35.48
Std Dev	3.282

**Gaus mean : 35.9606**

**Gaus Width: 3.0085**



# B1L102S, U3-ch115, adc2

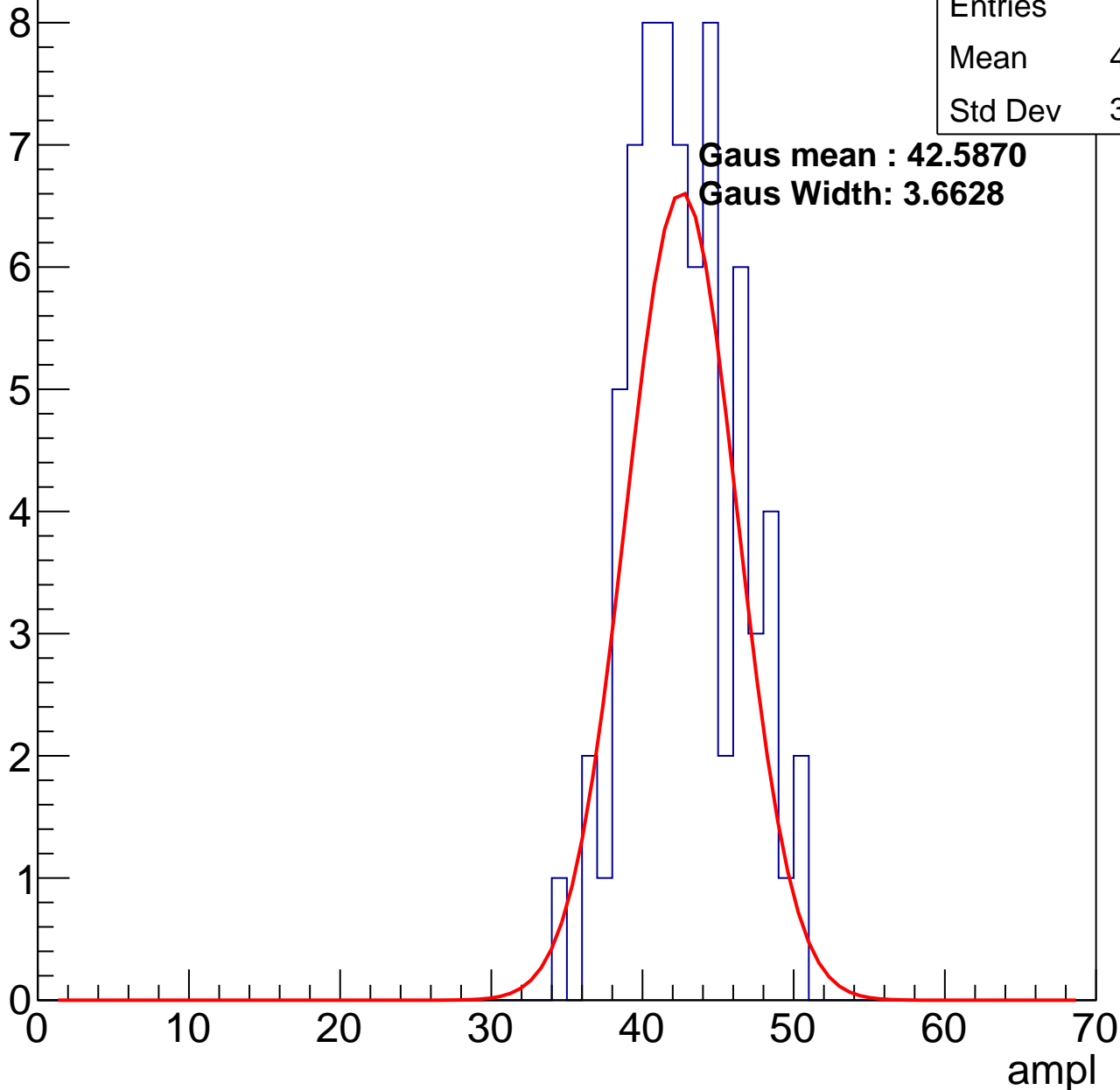
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	42.34
Std Dev	3.528

**Gaus mean : 42.5870**

**Gaus Width: 3.6628**

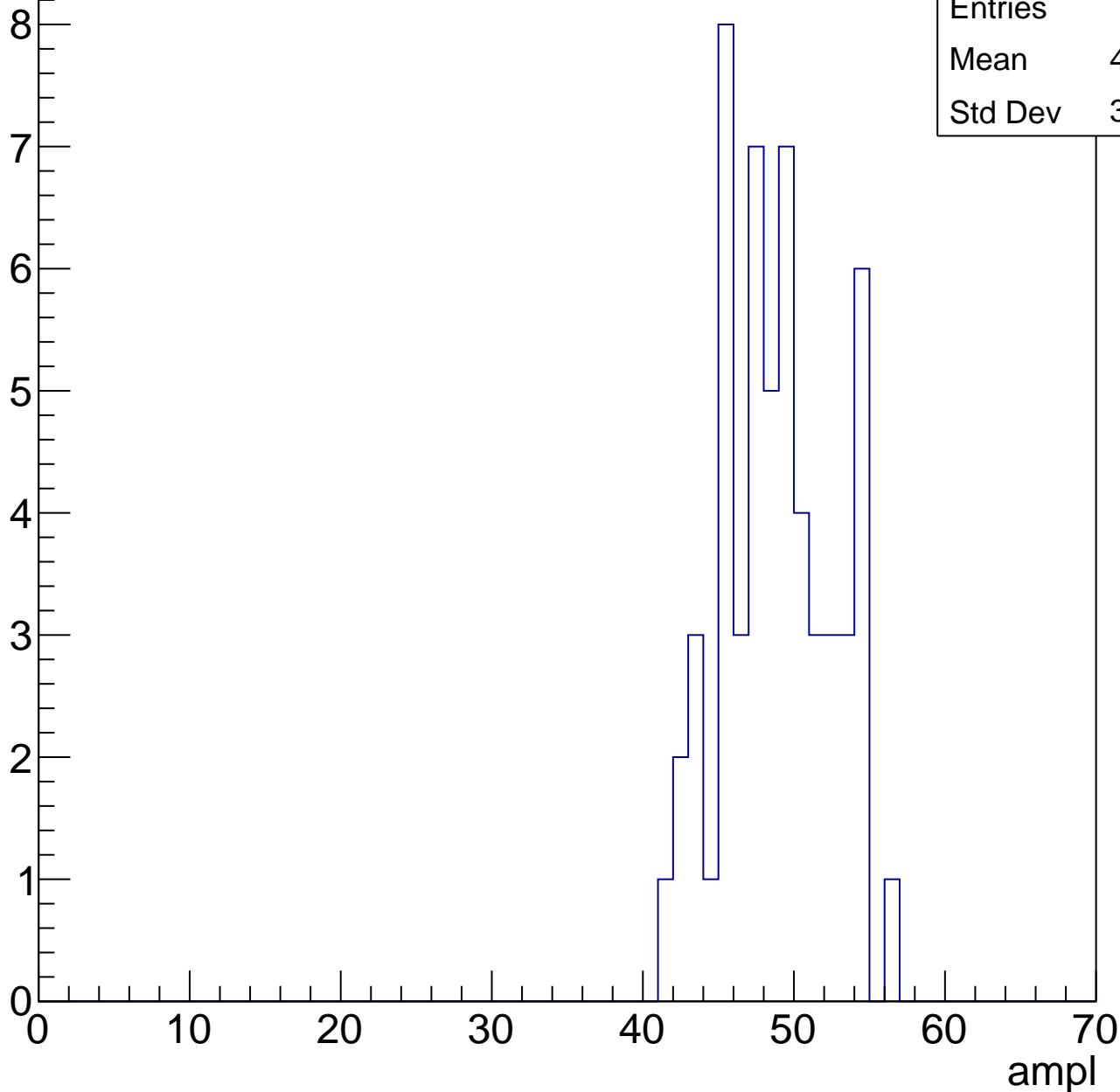


# B1L102S, U3-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	48.35
Std Dev	3.625

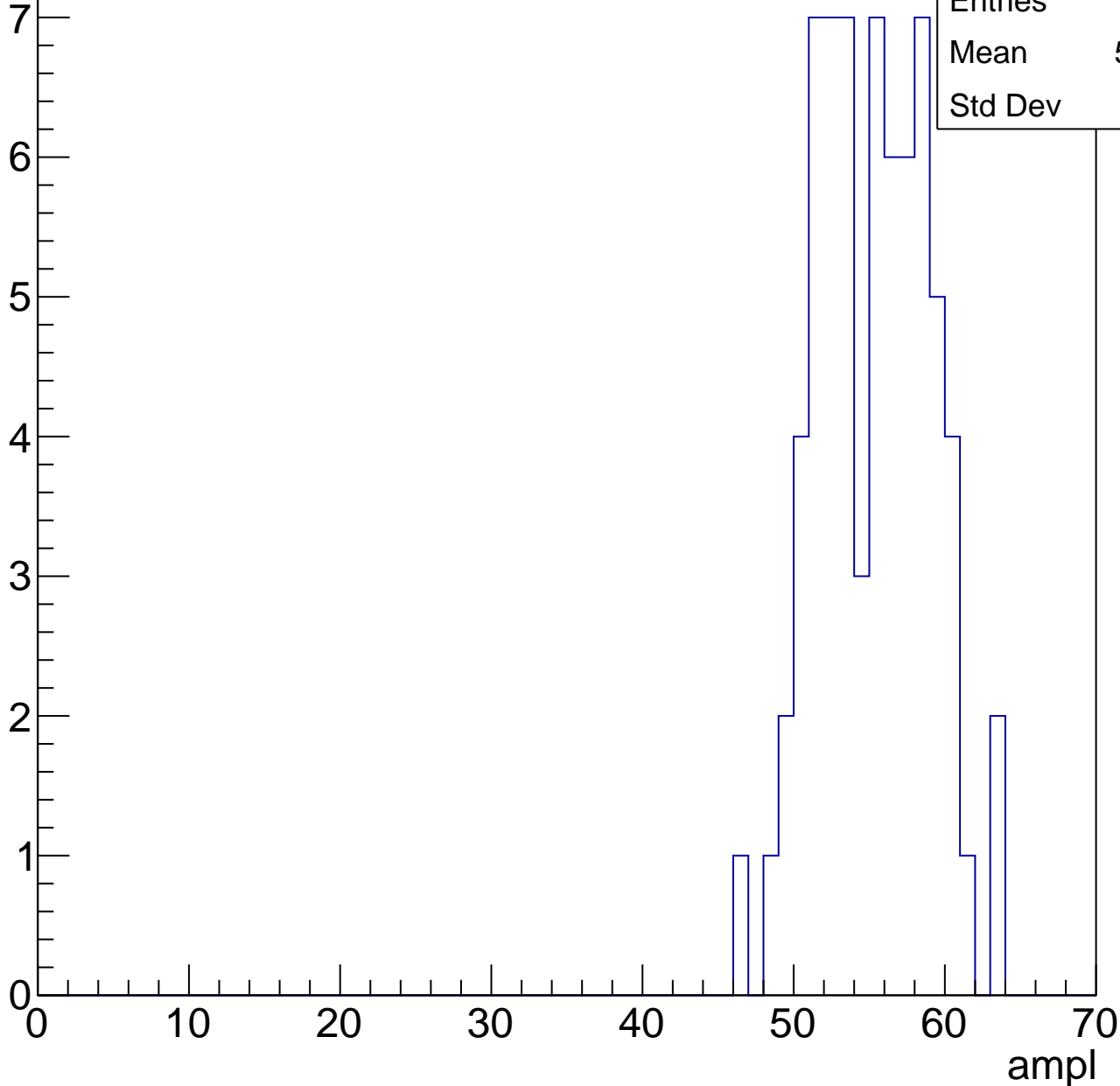


# B1L102S, U3-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	54.81
Std Dev	3.67

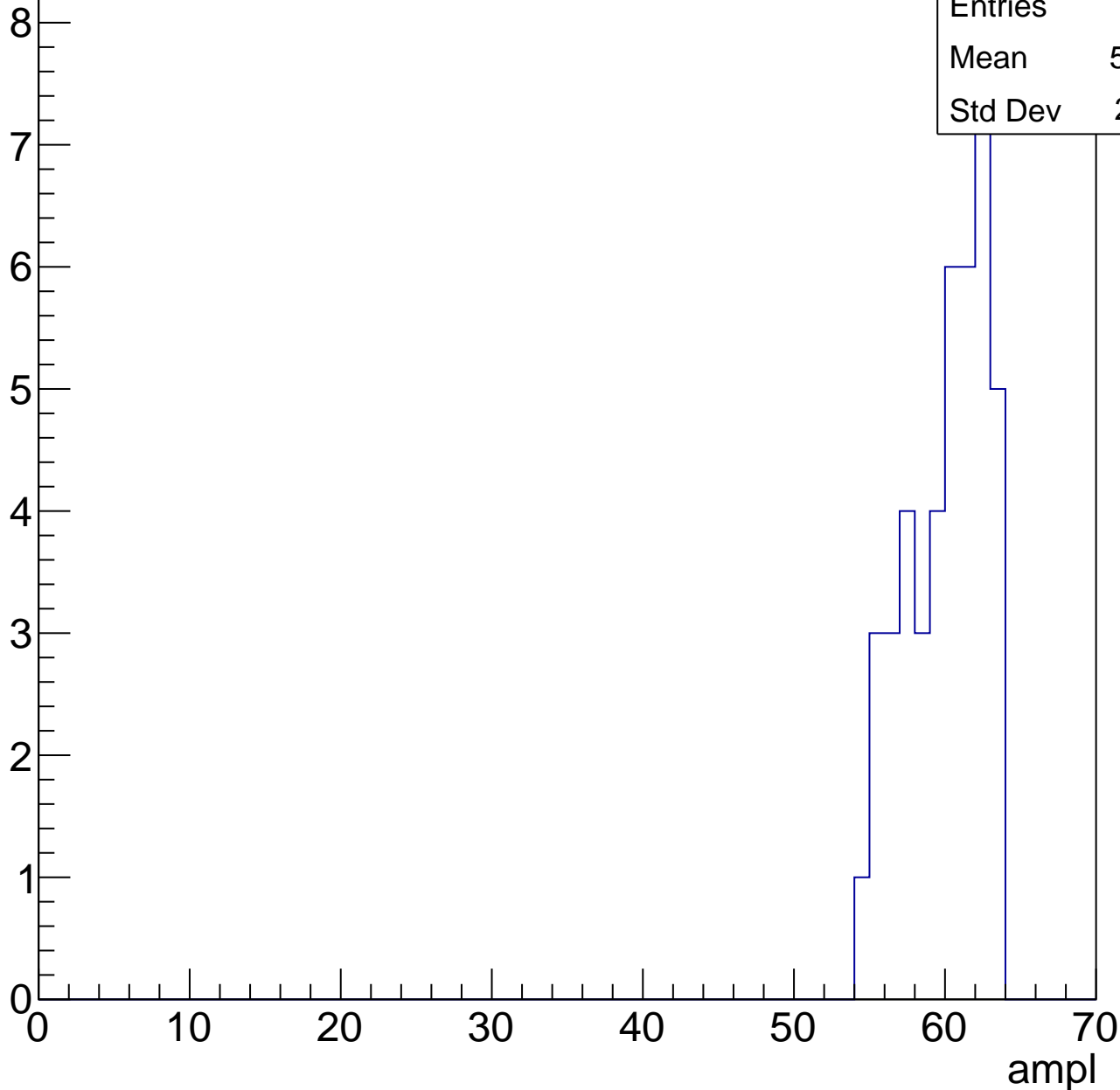


# B1L102S, U3-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

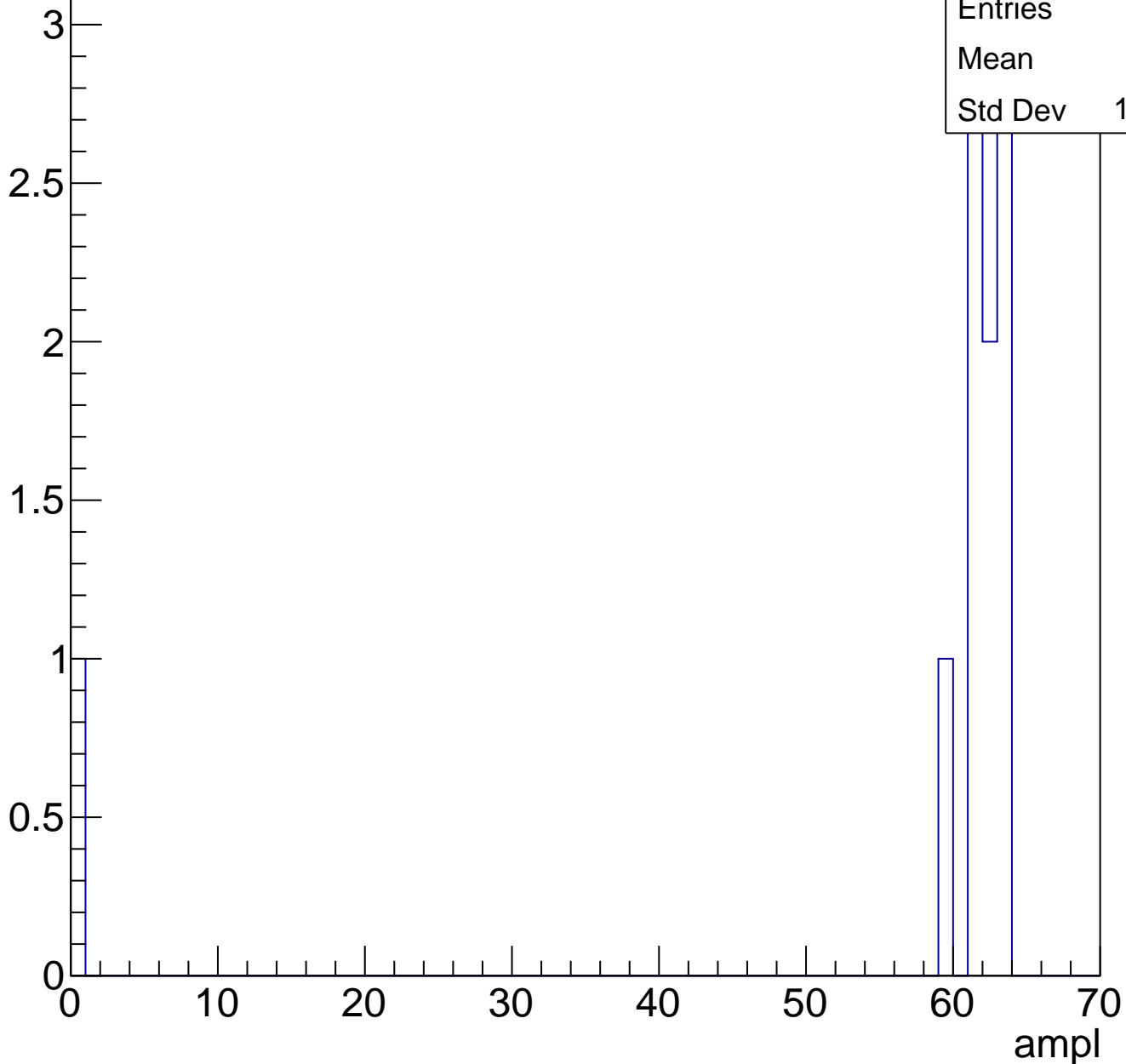
Entries	43
Mean	59.58
Std Dev	2.581



# B1L102S, U3-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L102S, U3-ch116, adc0

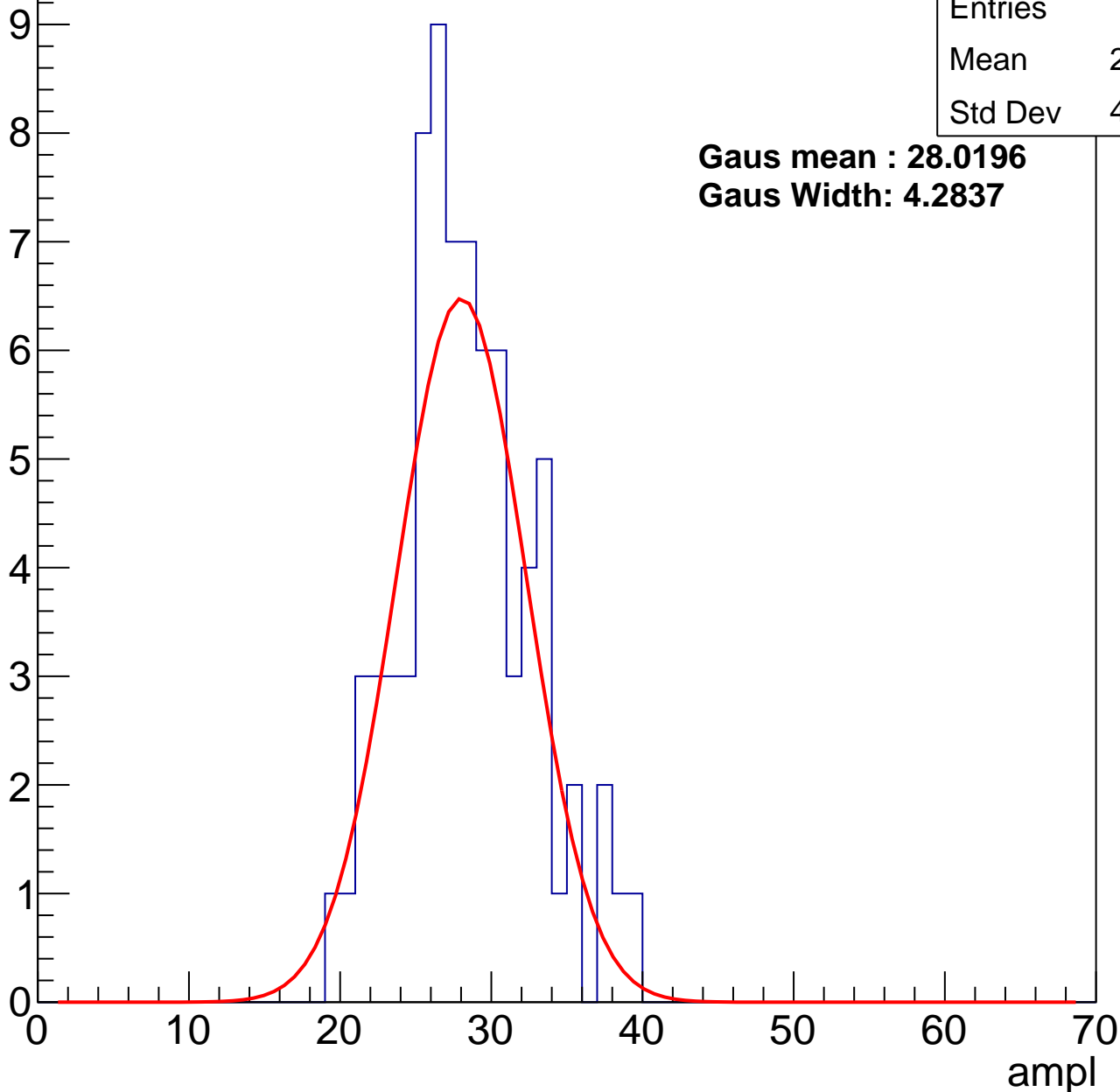
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	27.93
Std Dev	4.293

**Gaus mean : 28.0196**

**Gaus Width: 4.2837**



# B1L102S, U3-ch116, adc1

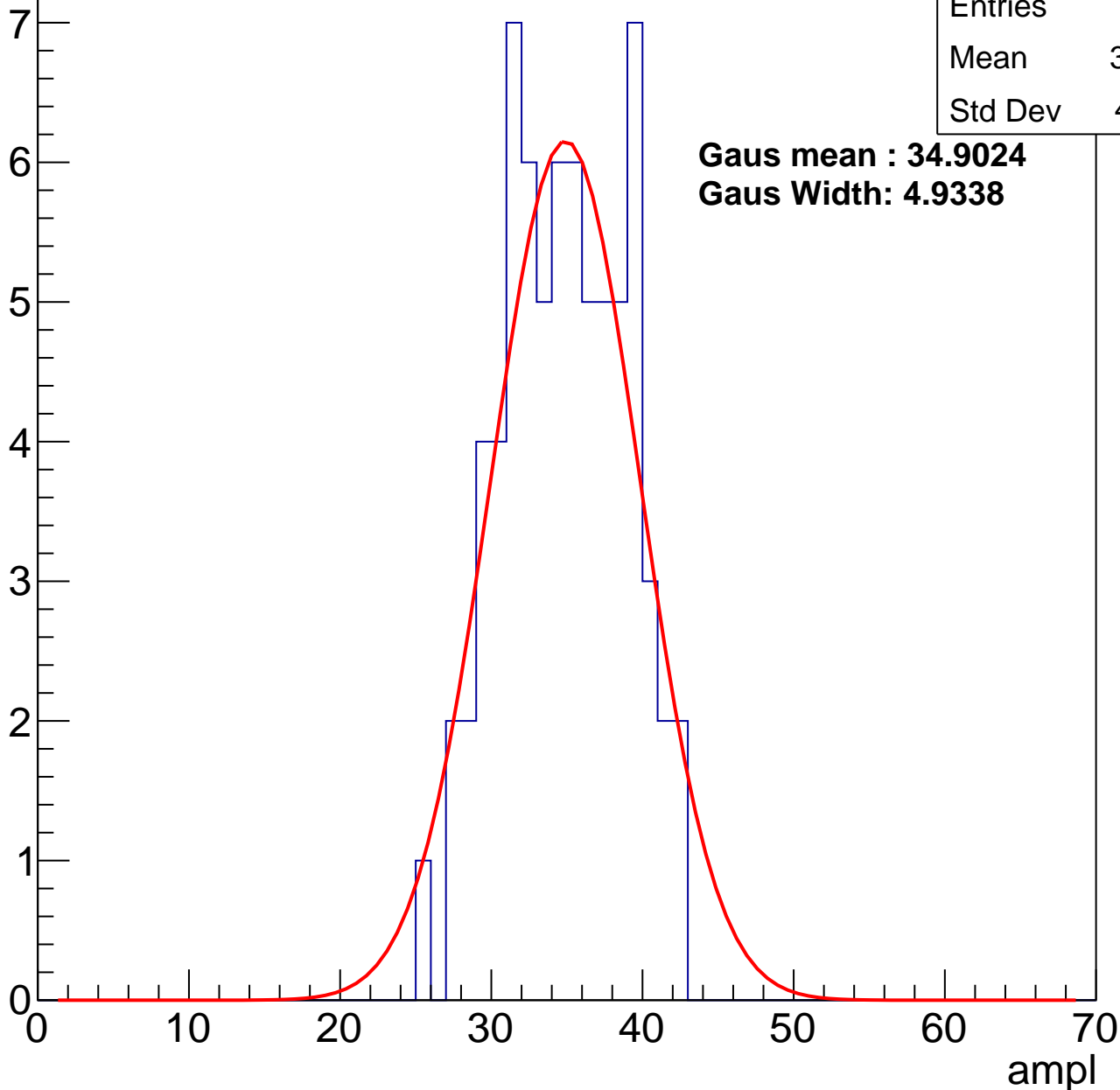
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	34.35
Std Dev	4.011

**Gaus mean : 34.9024**

**Gaus Width: 4.9338**



# B1L102S, U3-ch116, adc2

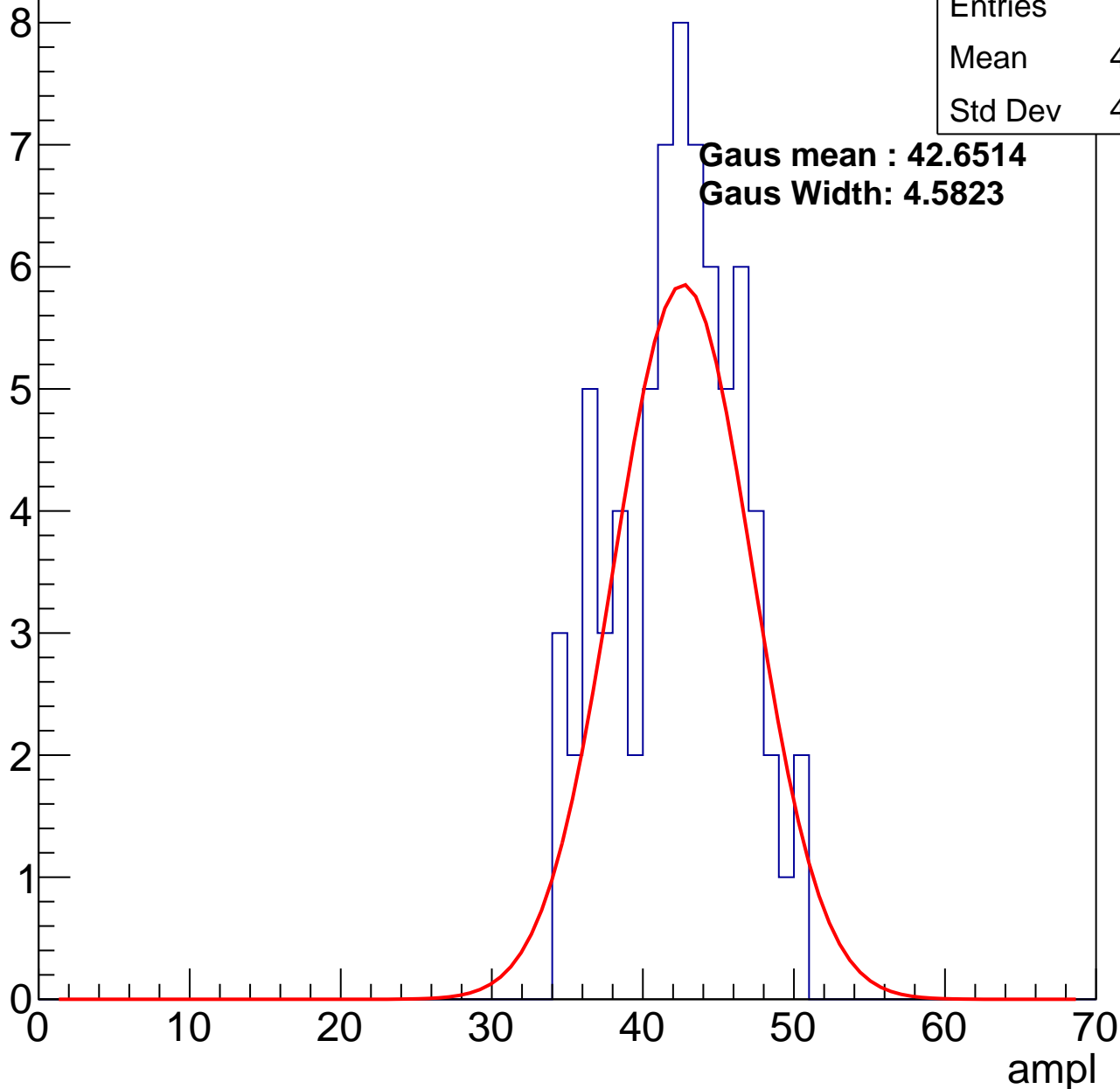
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	41.88
Std Dev	4.038

**Gaus mean : 42.6514**

**Gaus Width: 4.5823**

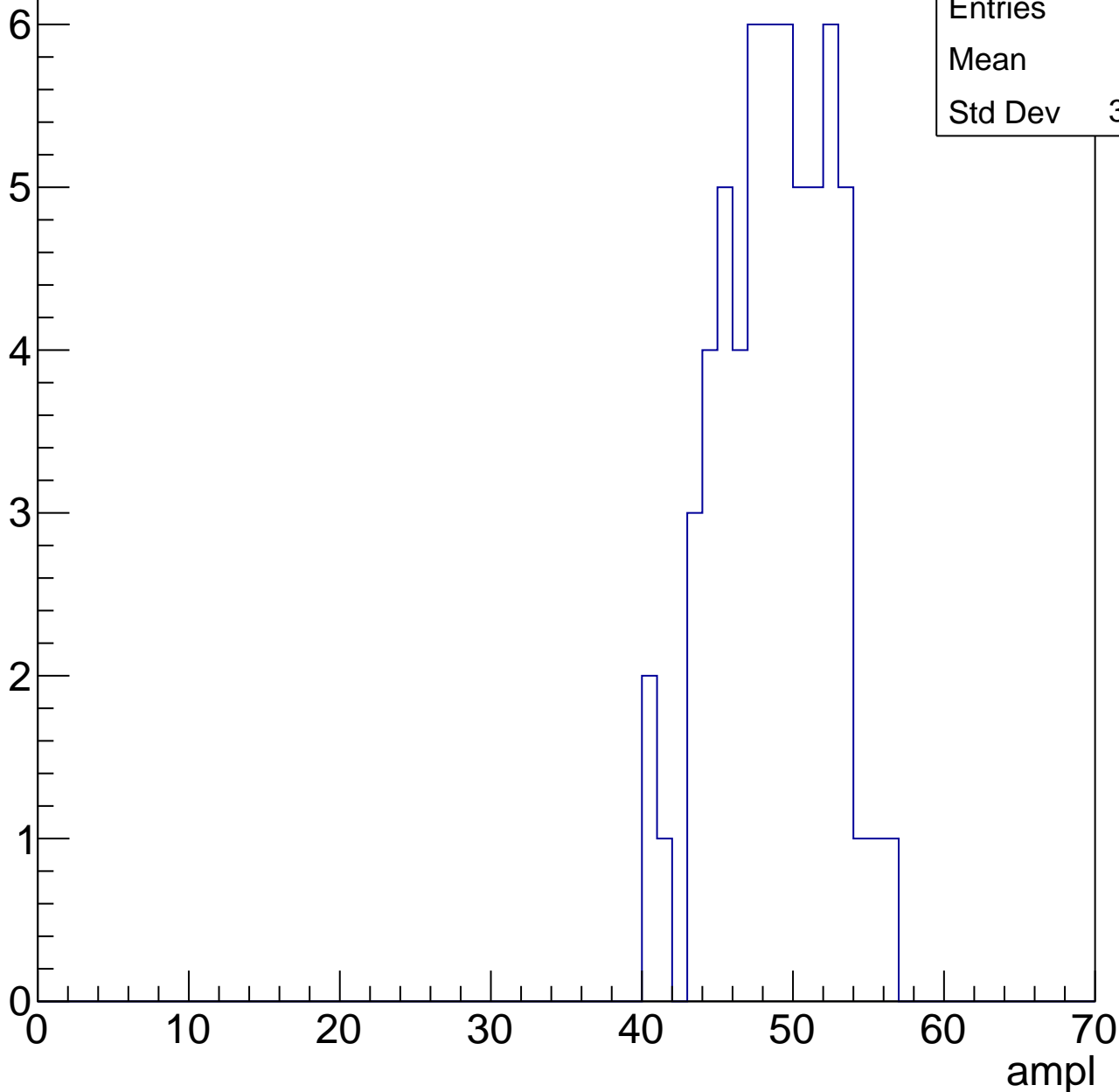


# B1L102S, U3-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	48.3
Std Dev	3.663

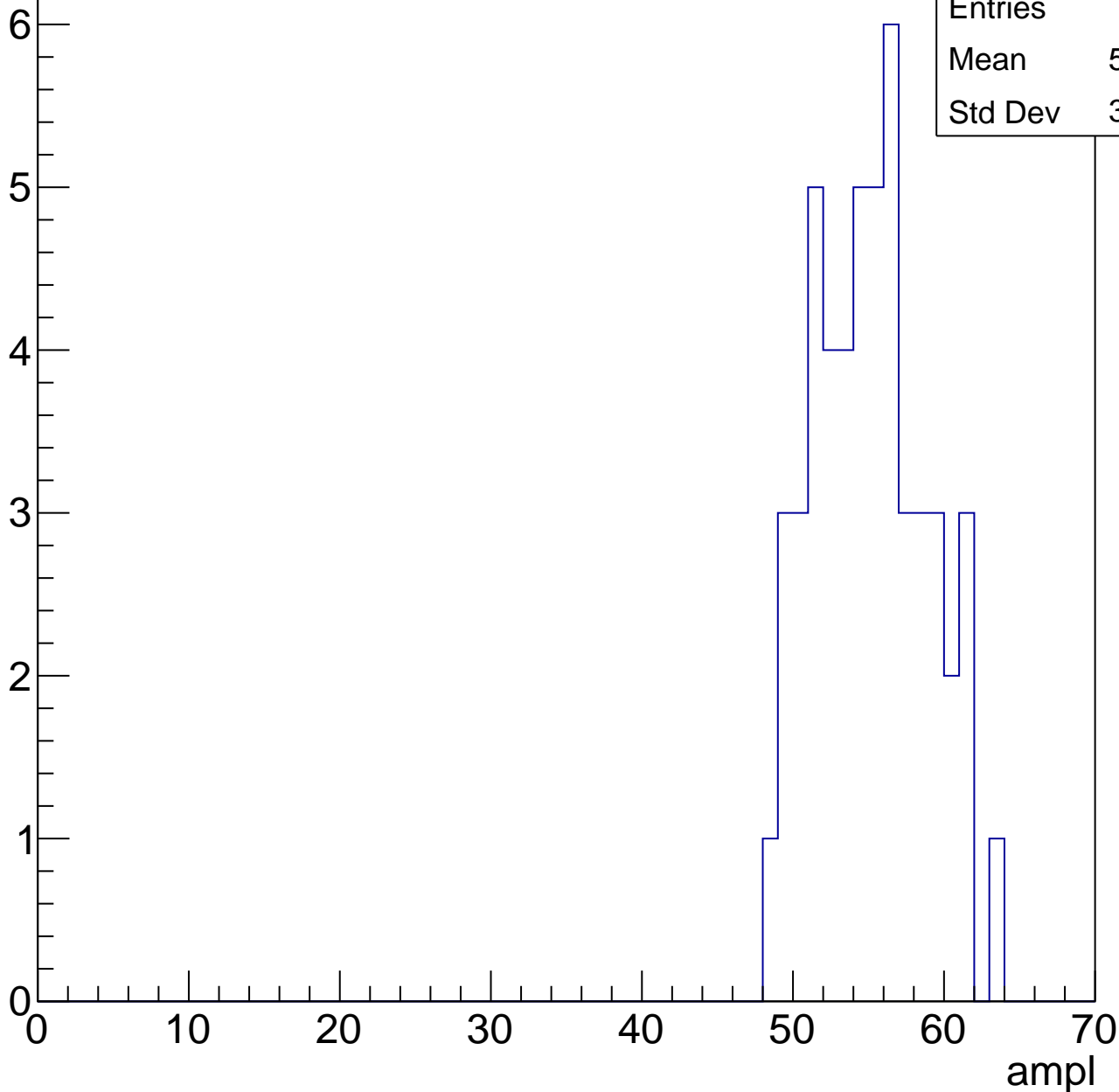


# B1L102S, U3-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	54.69
Std Dev	3.649

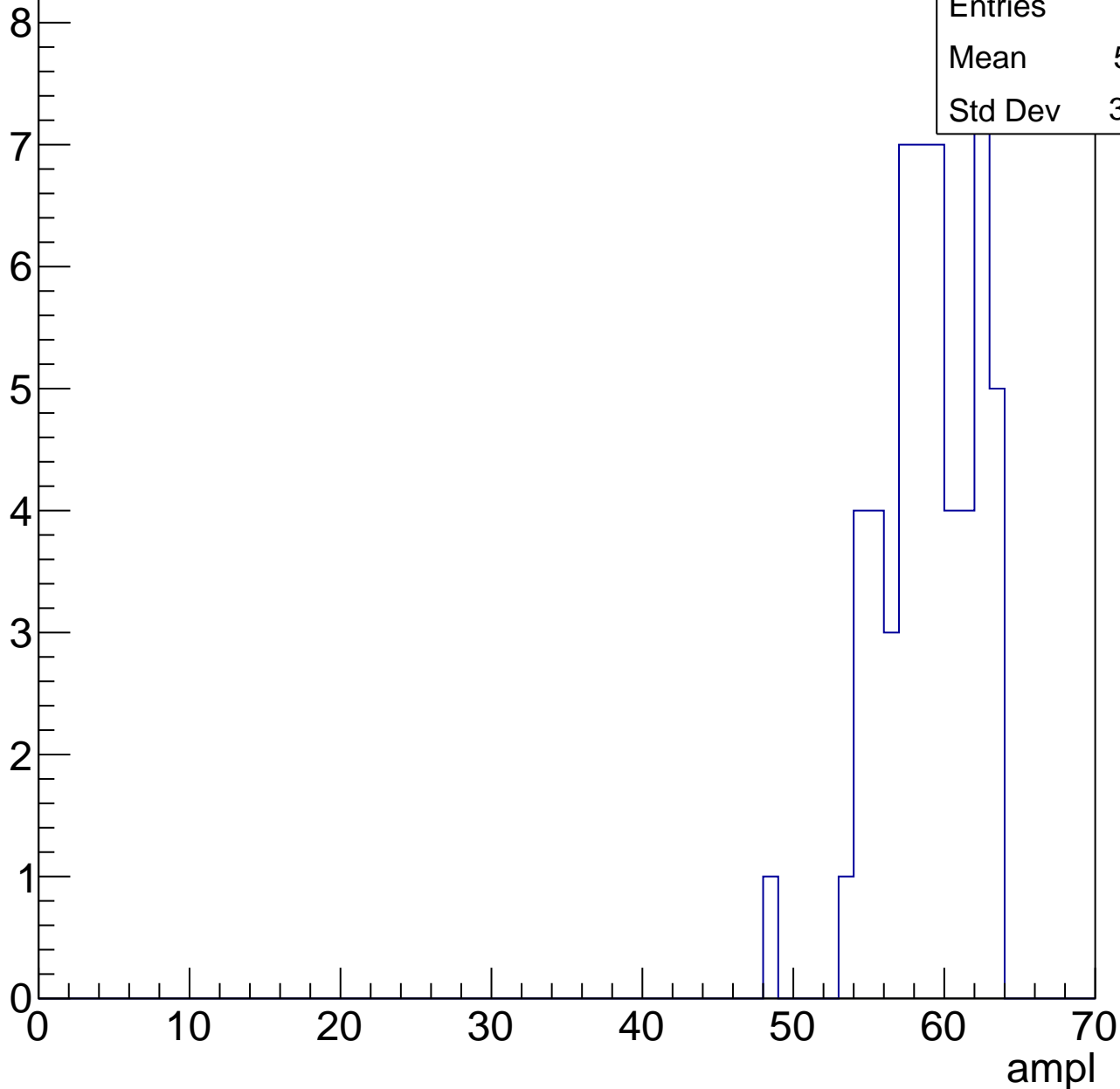


# B1L102S, U3-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

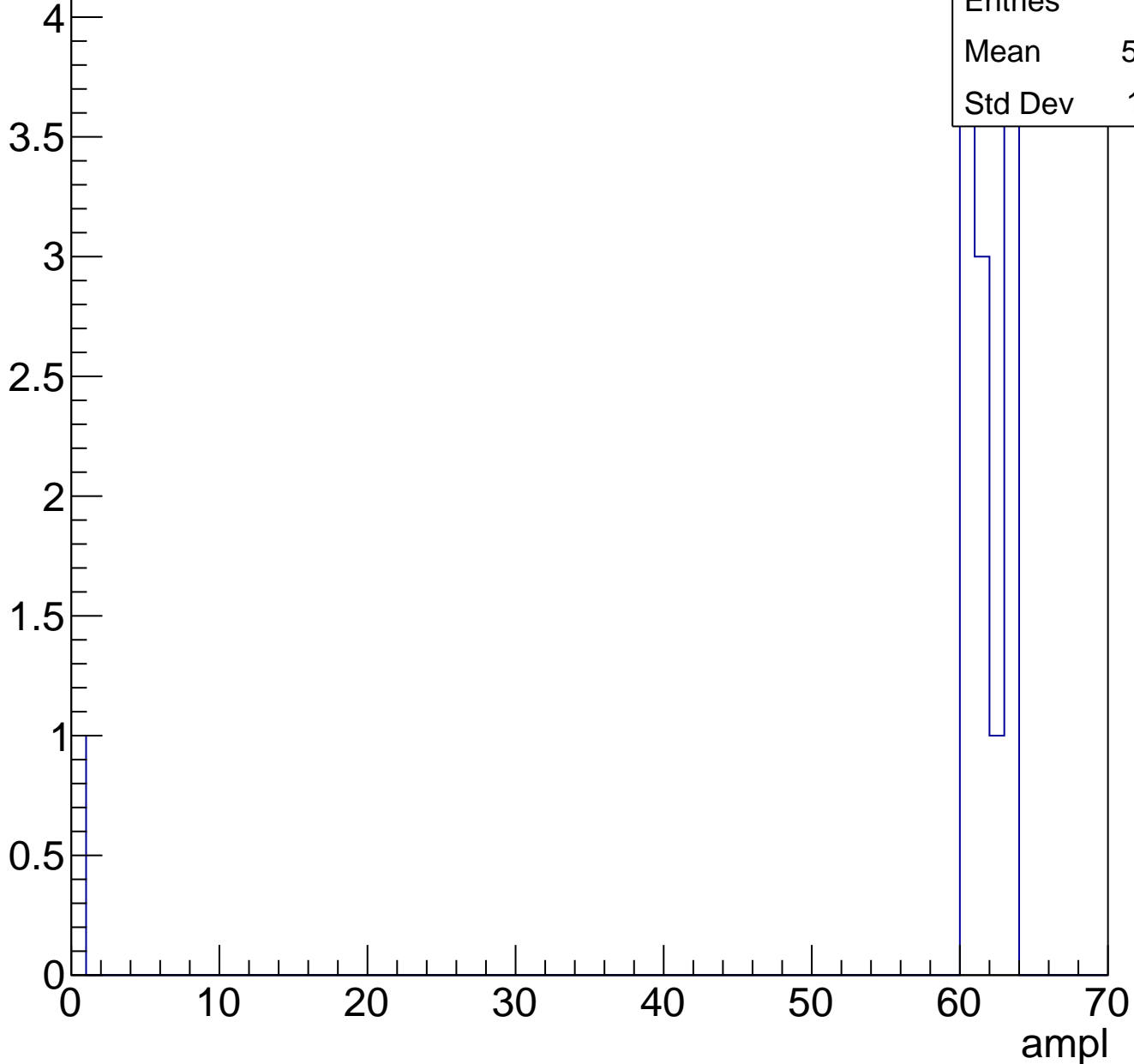
Entries	55
Mean	58.51
Std Dev	3.138



# B1L102S, U3-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

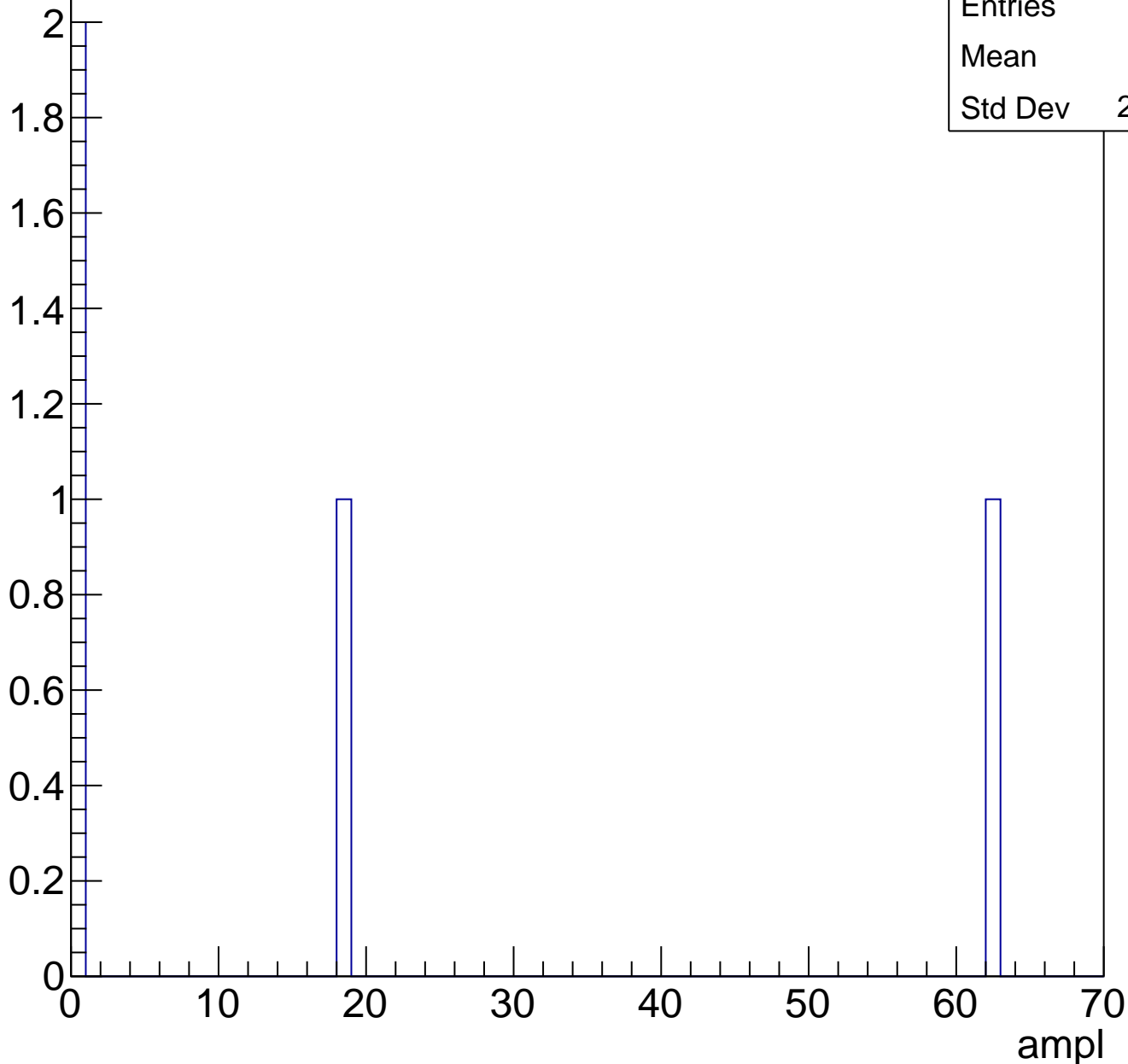




# B1L102S, U3-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	4
Mean	20
Std Dev	25.34

# B1L102S, U3-ch117, adc0

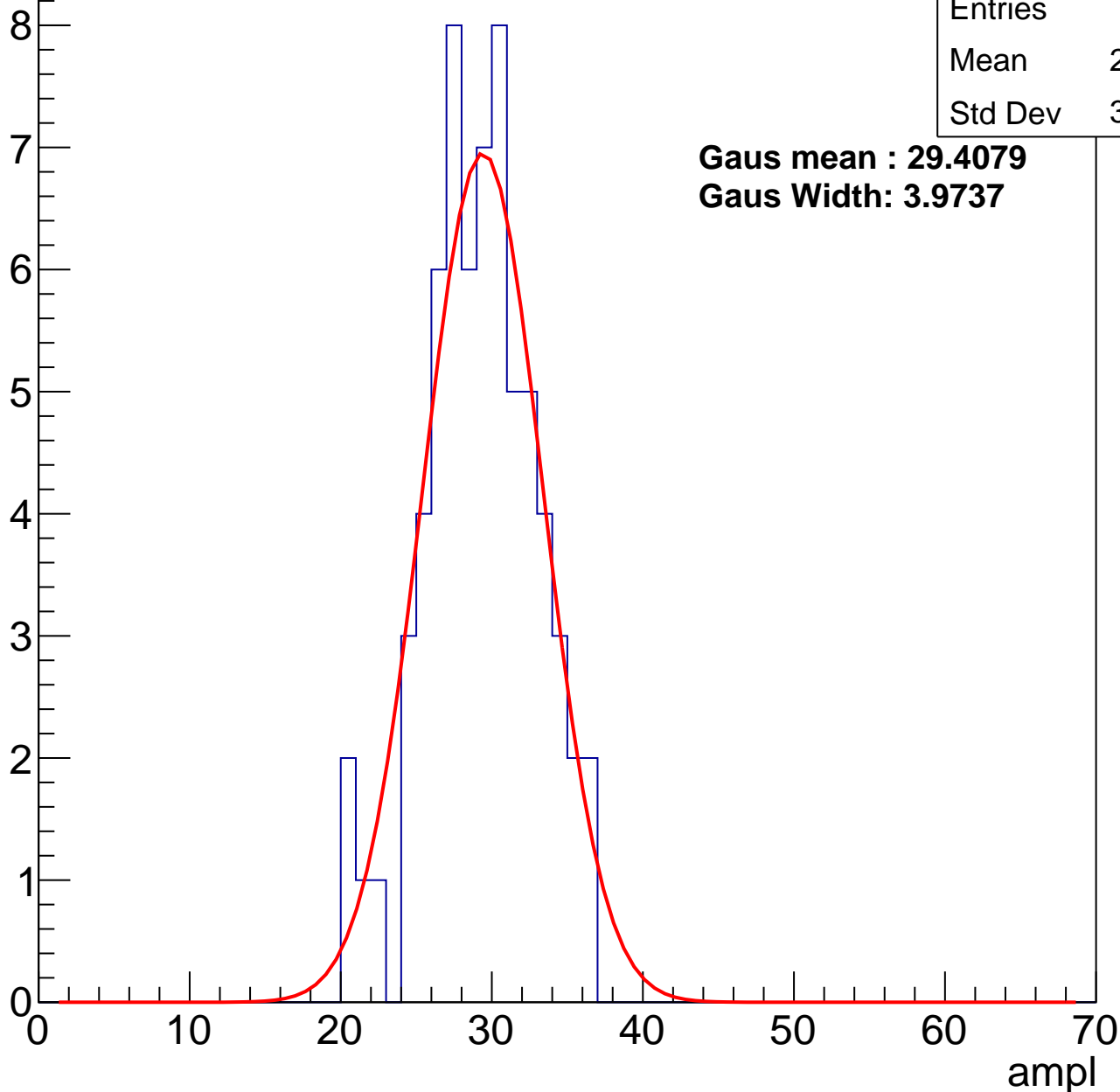
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	28.79
Std Dev	3.635

**Gaus mean : 29.4079**

**Gaus Width: 3.9737**



# B1L102S, U3-ch117, adc1

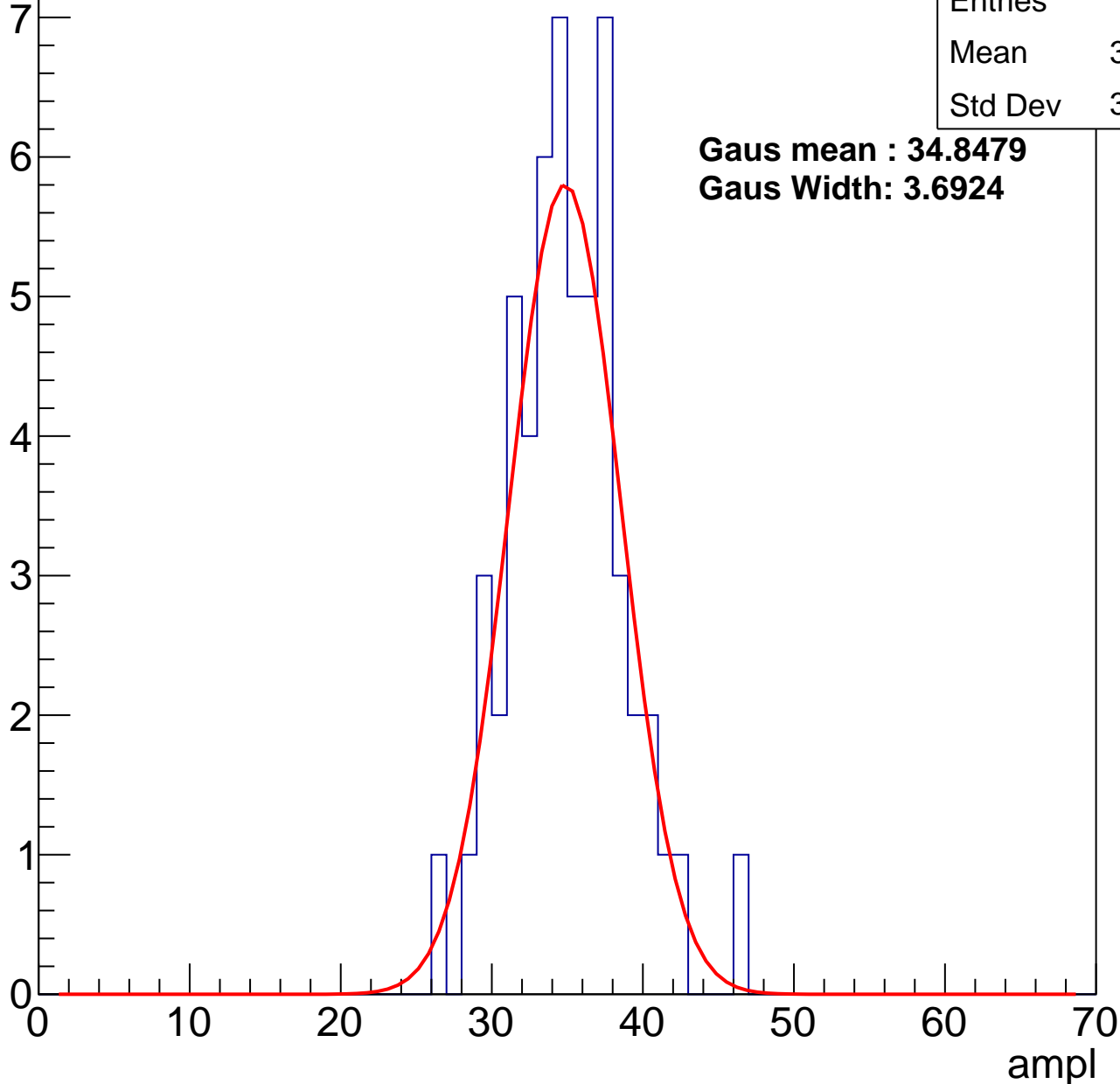
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	34.55
Std Dev	3.713

**Gaus mean : 34.8479**

**Gaus Width: 3.6924**



# B1L102S, U3-ch117, adc2

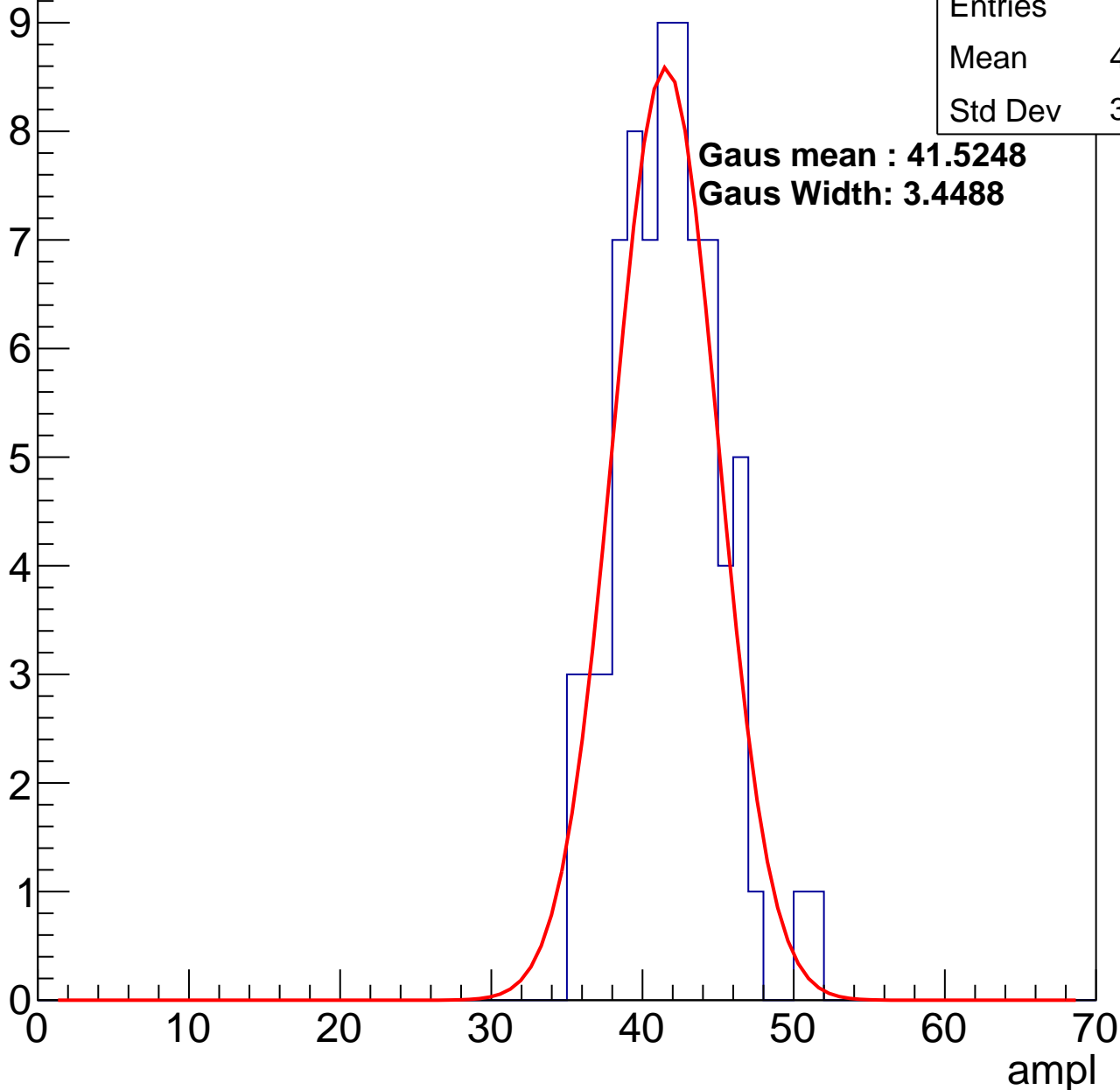
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	41.28
Std Dev	3.333

**Gaus mean : 41.5248**

**Gaus Width: 3.4488**

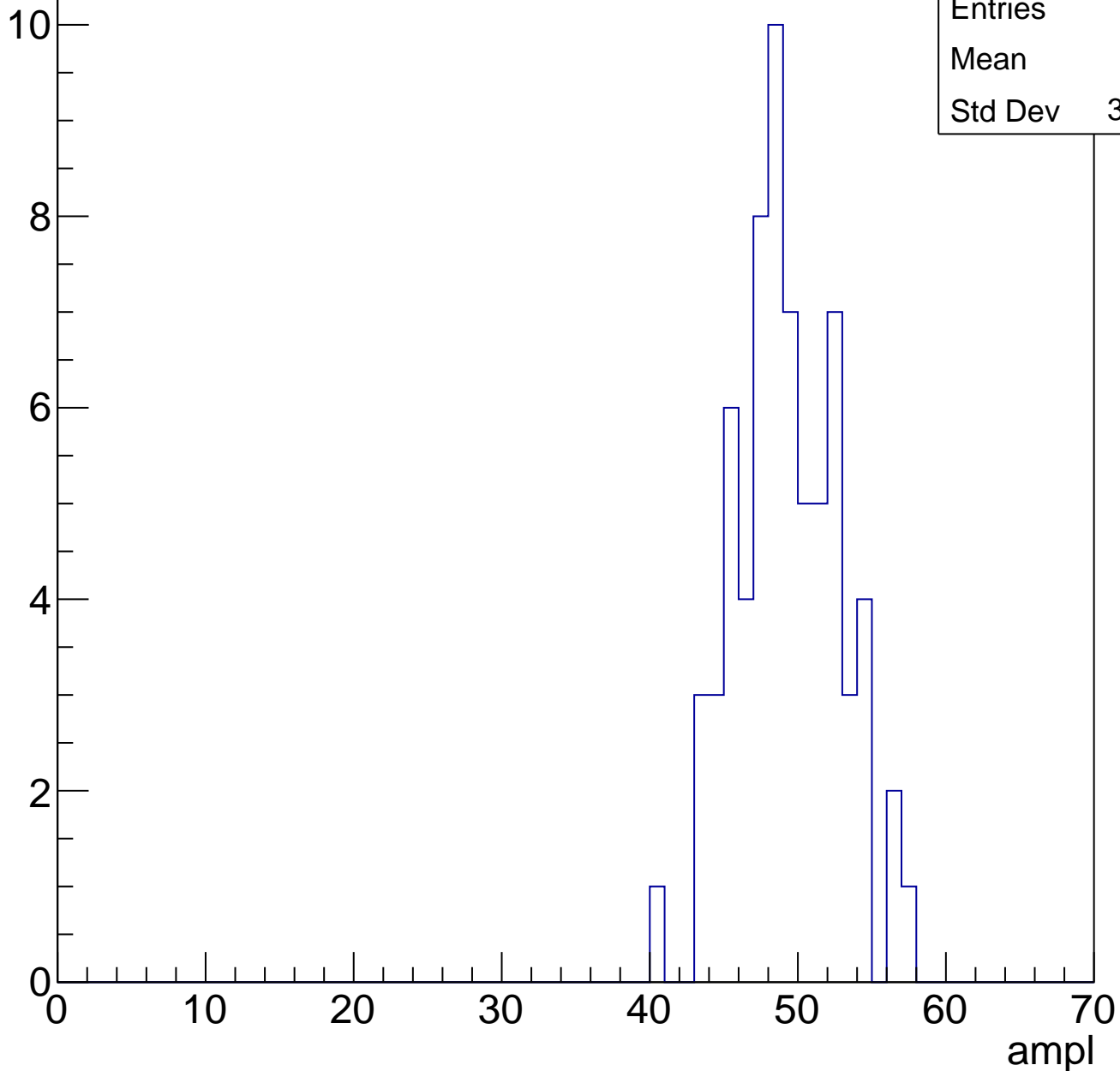


# B1L102S, U3-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	69
Mean	48.8
Std Dev	3.475

Entry

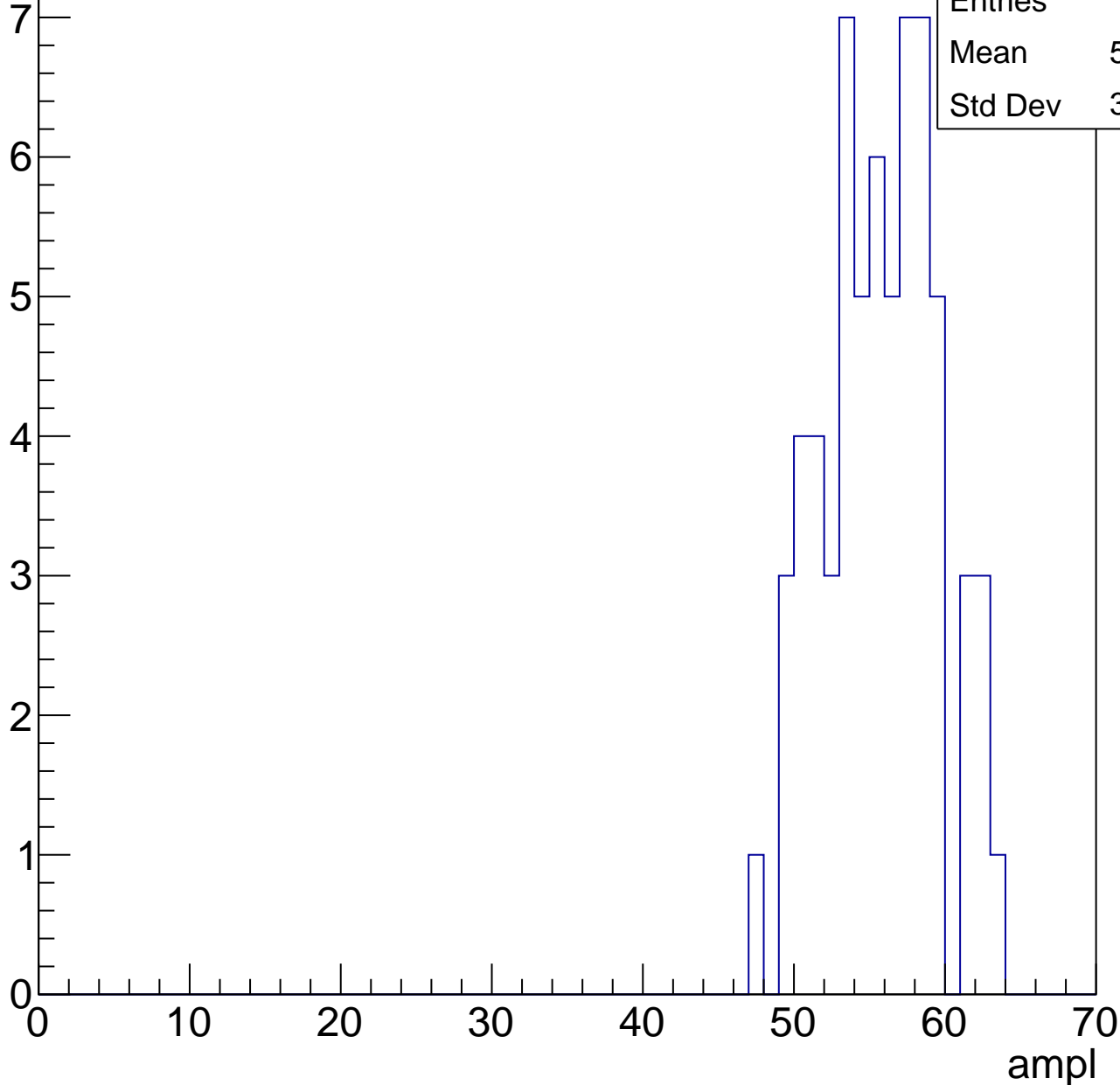


# B1L102S, U3-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

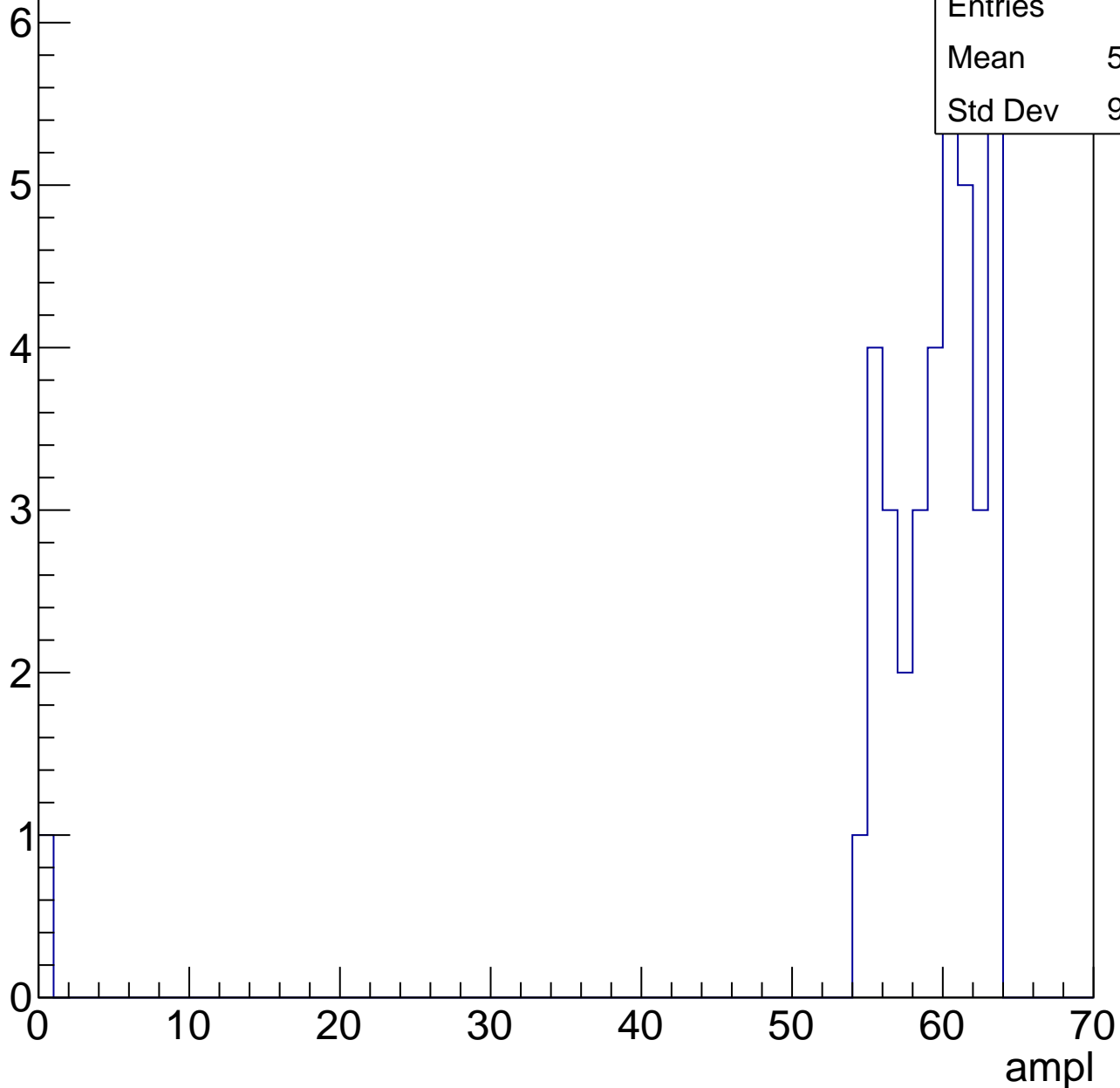
Entries	64
Mean	55.27
Std Dev	3.722



# B1L102S, U3-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

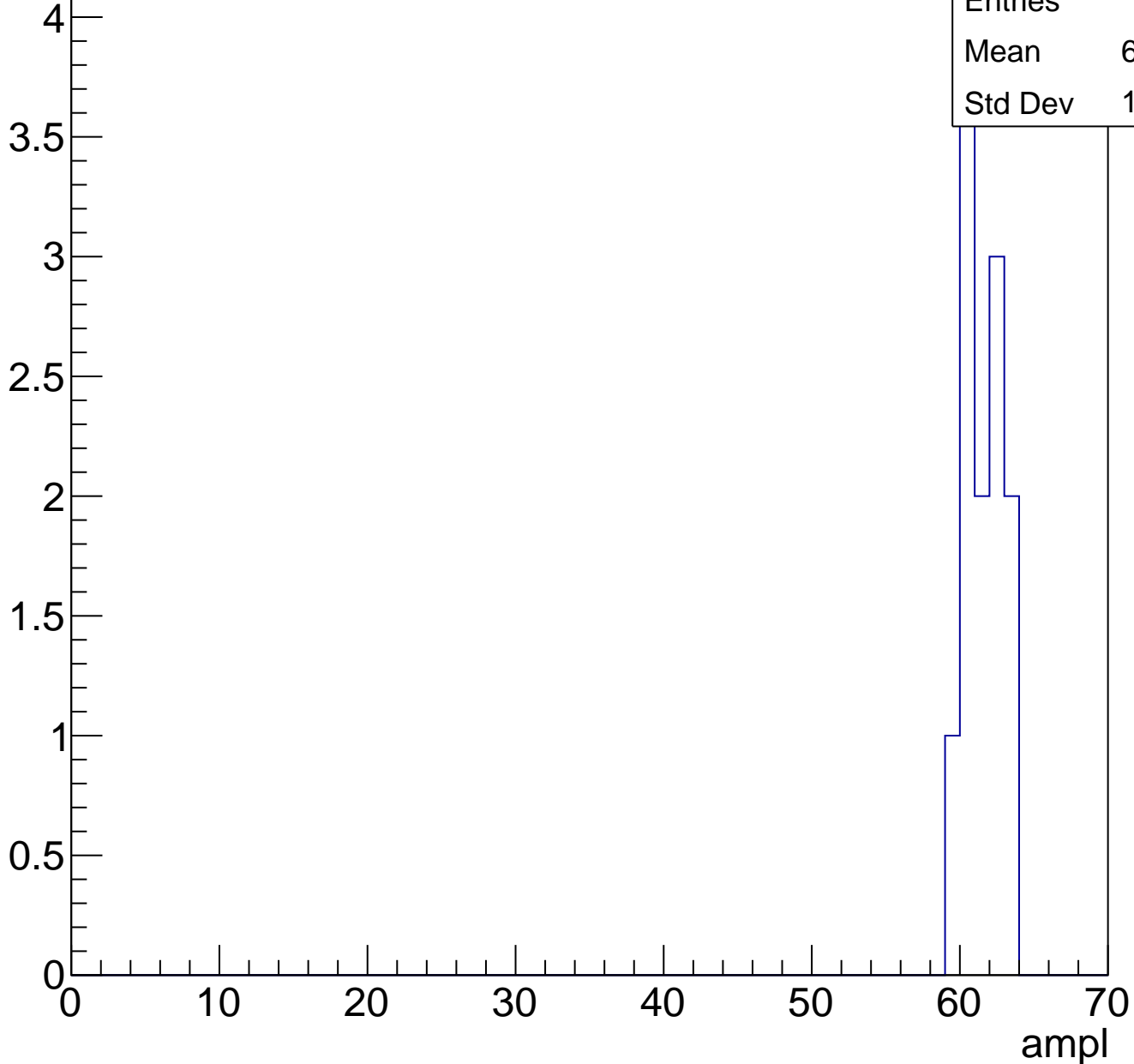
Entry



# B1L102S, U3-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

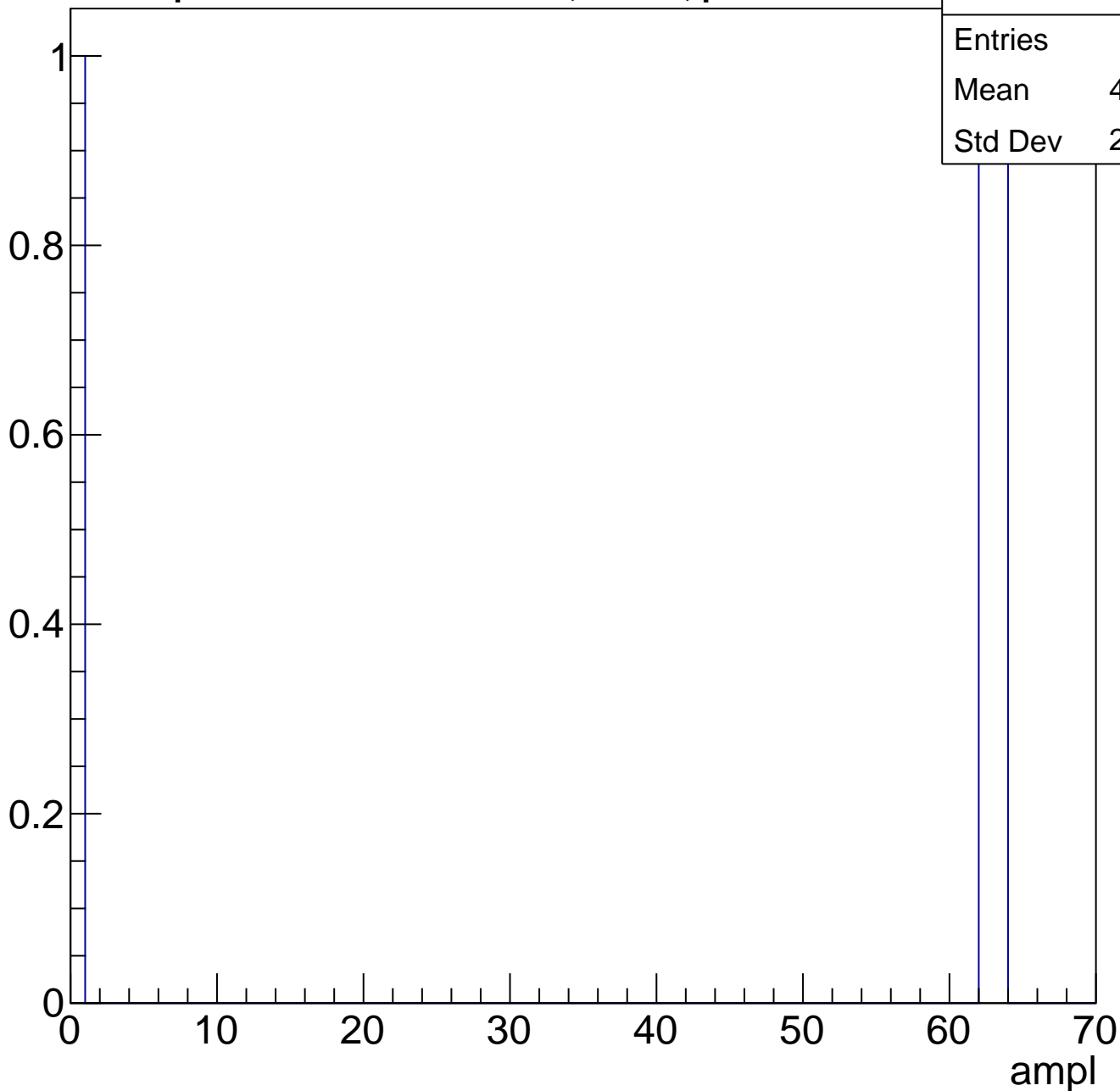




# B1L102S, U3-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch118, adc0

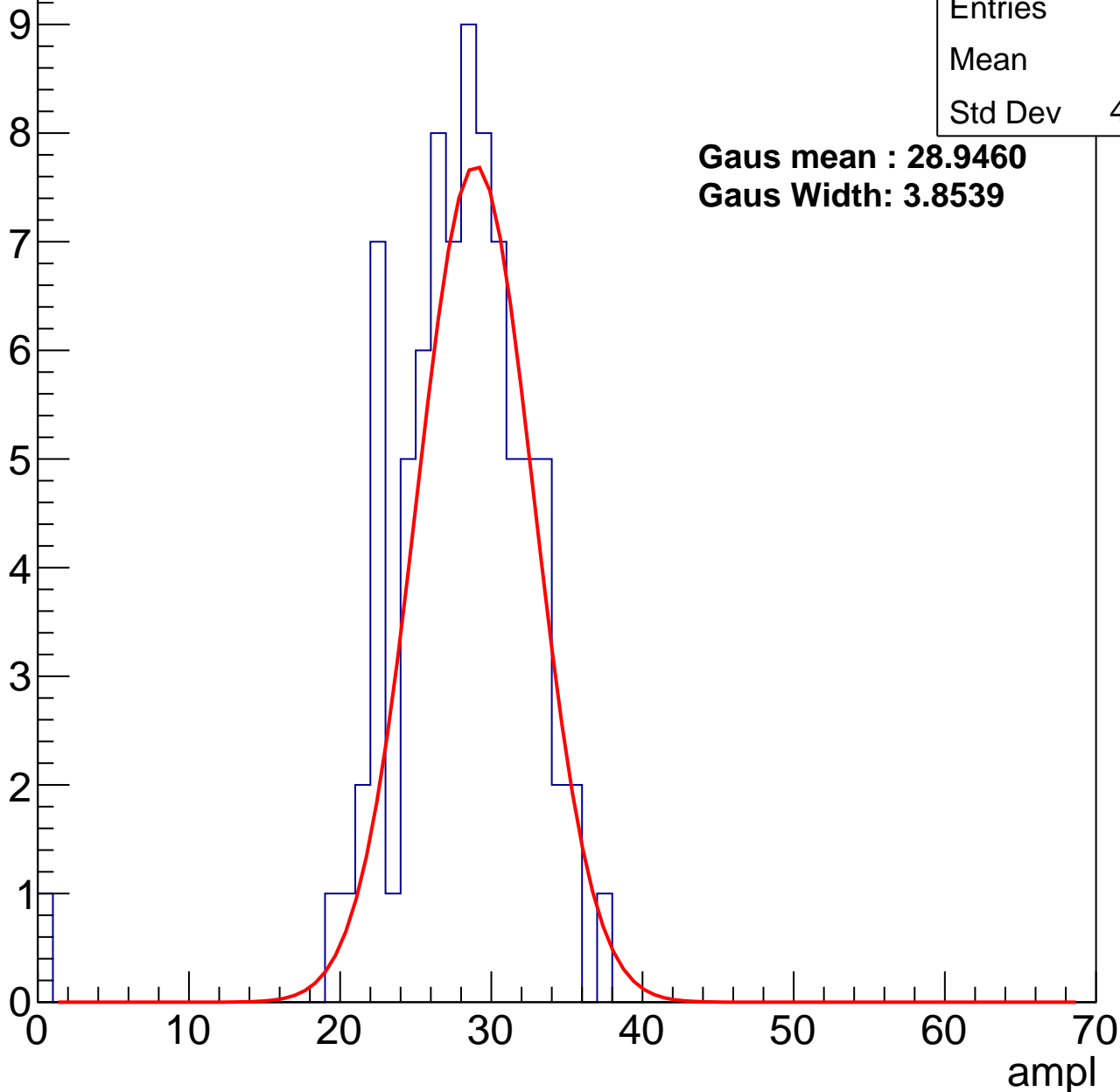
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	83
Mean	27.4
Std Dev	4.889

**Gaus mean : 28.9460**

**Gaus Width: 3.8539**



# B1L102S, U3-ch118, adc1

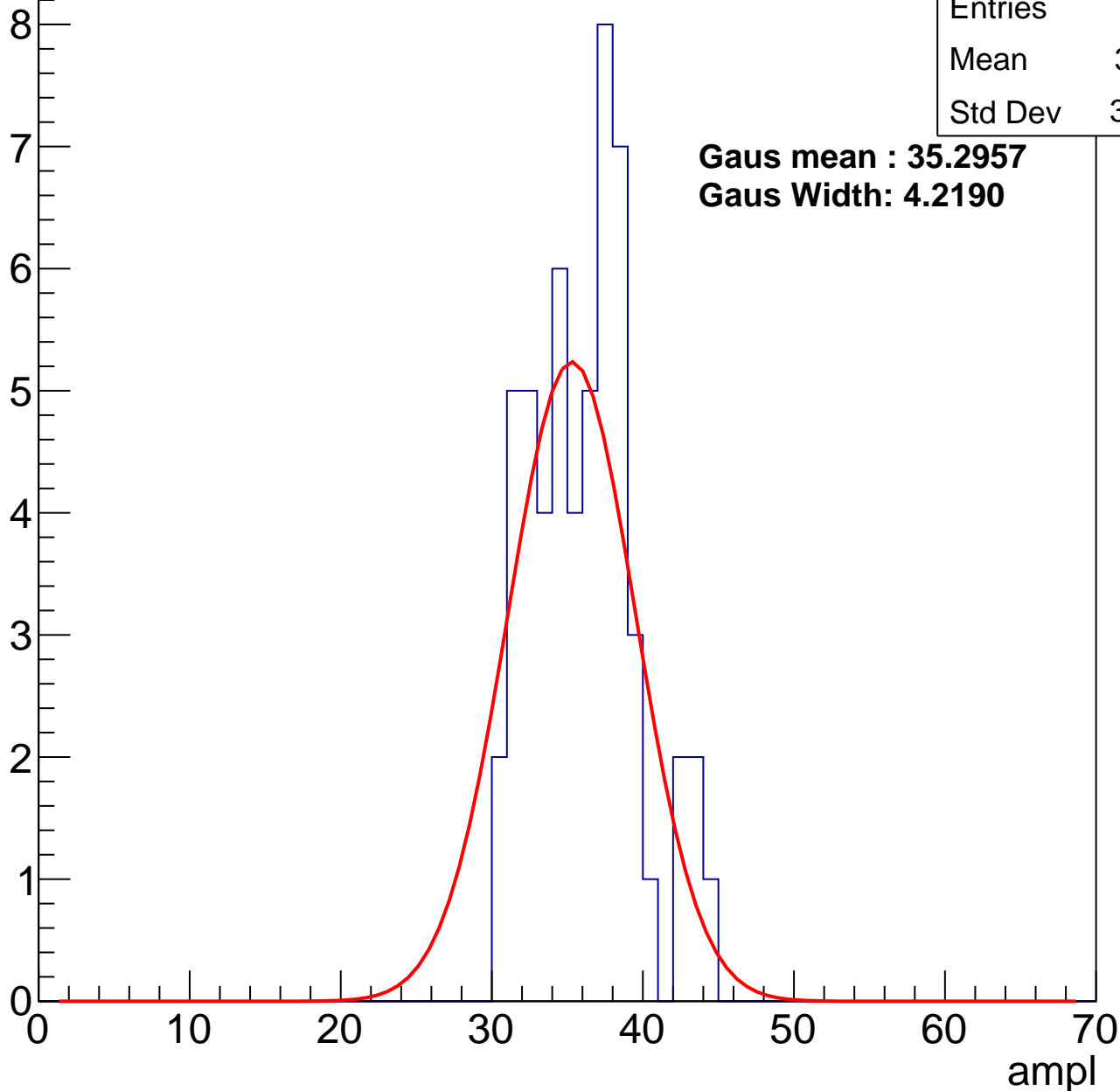
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	35.71
Std Dev	3.436

**Gaus mean : 35.2957**

**Gaus Width: 4.2190**



# B1L102S, U3-ch118, adc2

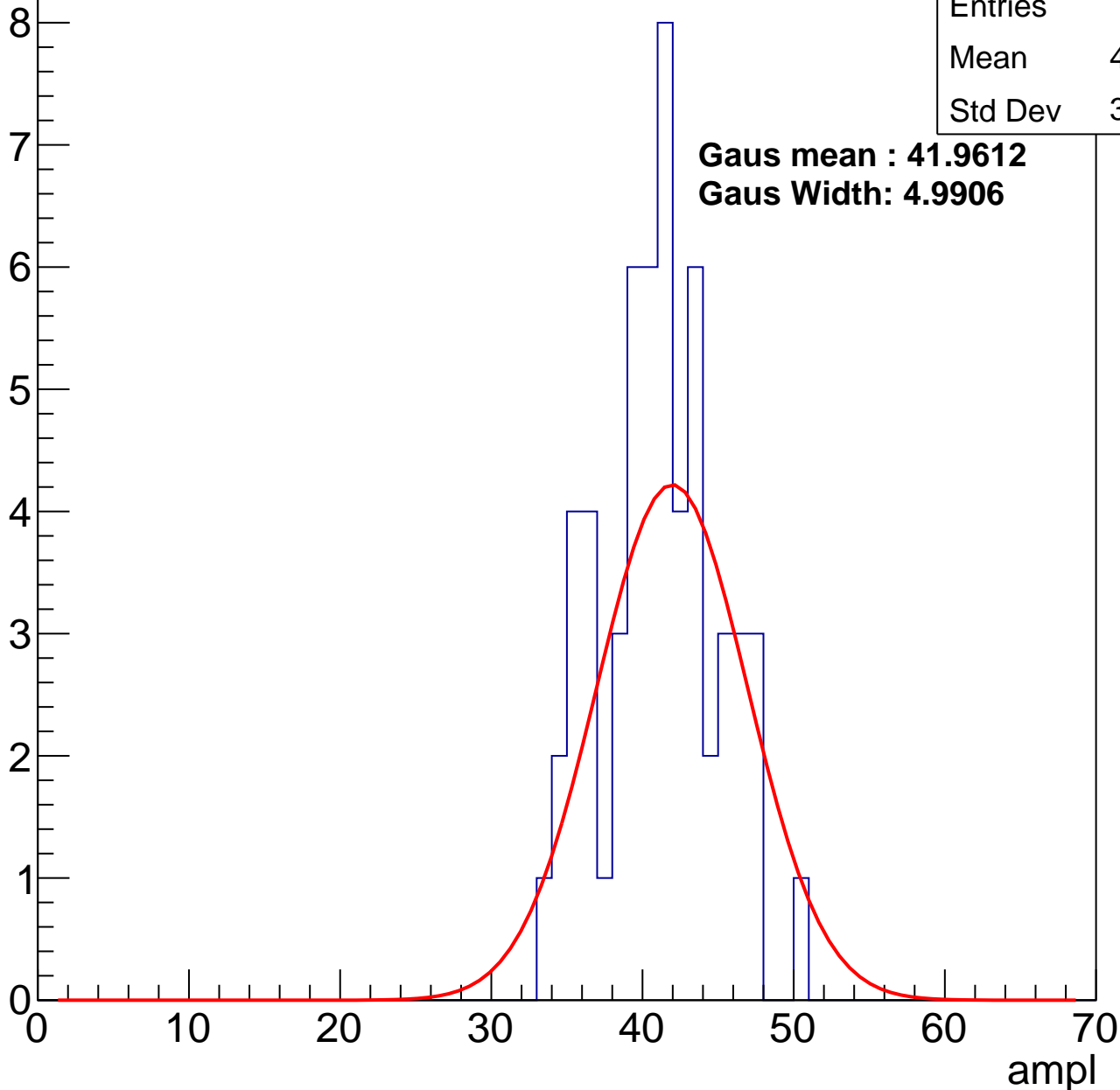
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	40.63
Std Dev	3.814

**Gaus mean : 41.9612**

**Gaus Width: 4.9906**

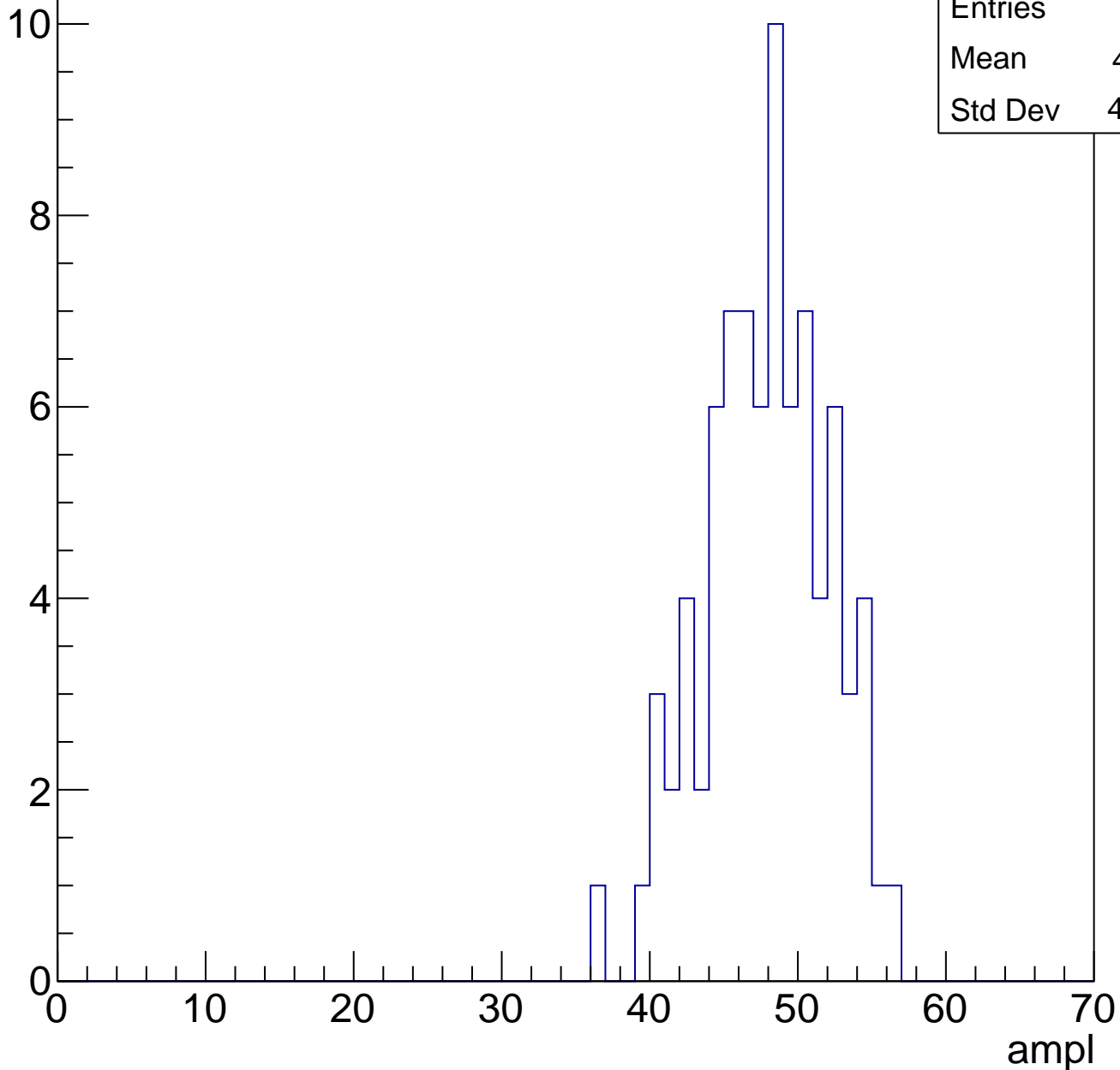


# B1L102S, U3-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	81
Mean	47.41
Std Dev	4.115

Entry

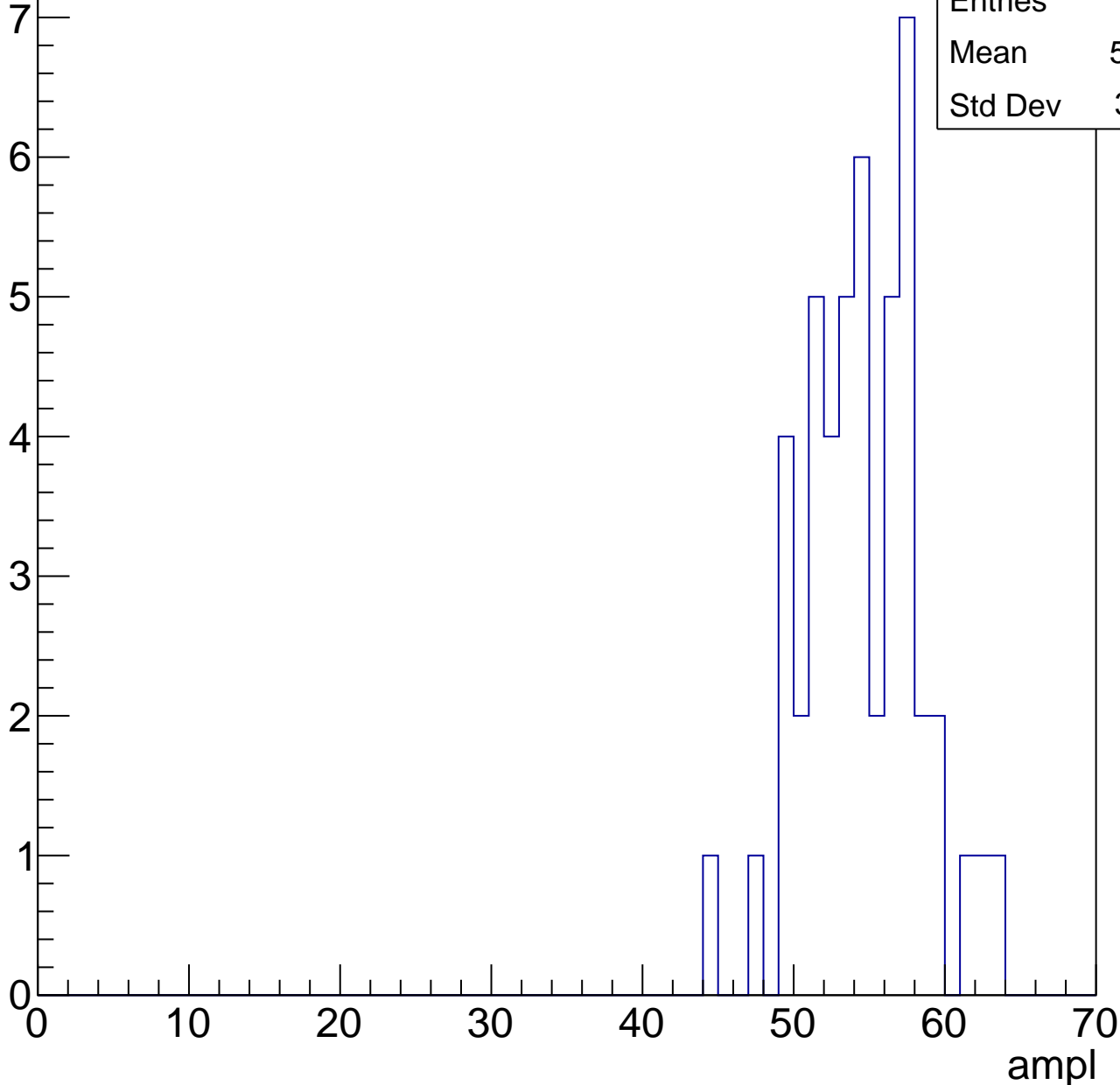


# B1L102S, U3-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	54.04
Std Dev	3.801

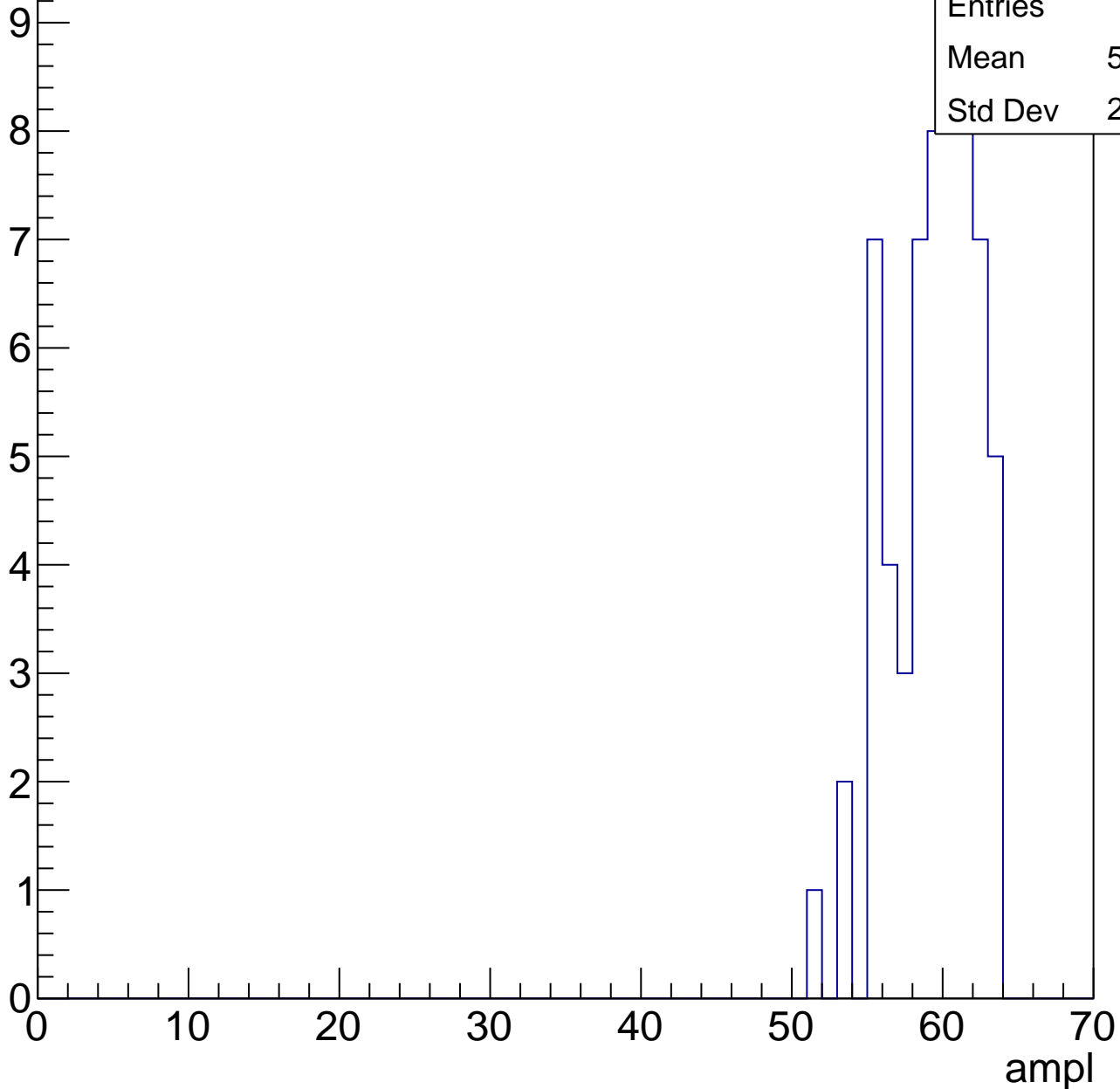


# B1L102S, U3-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

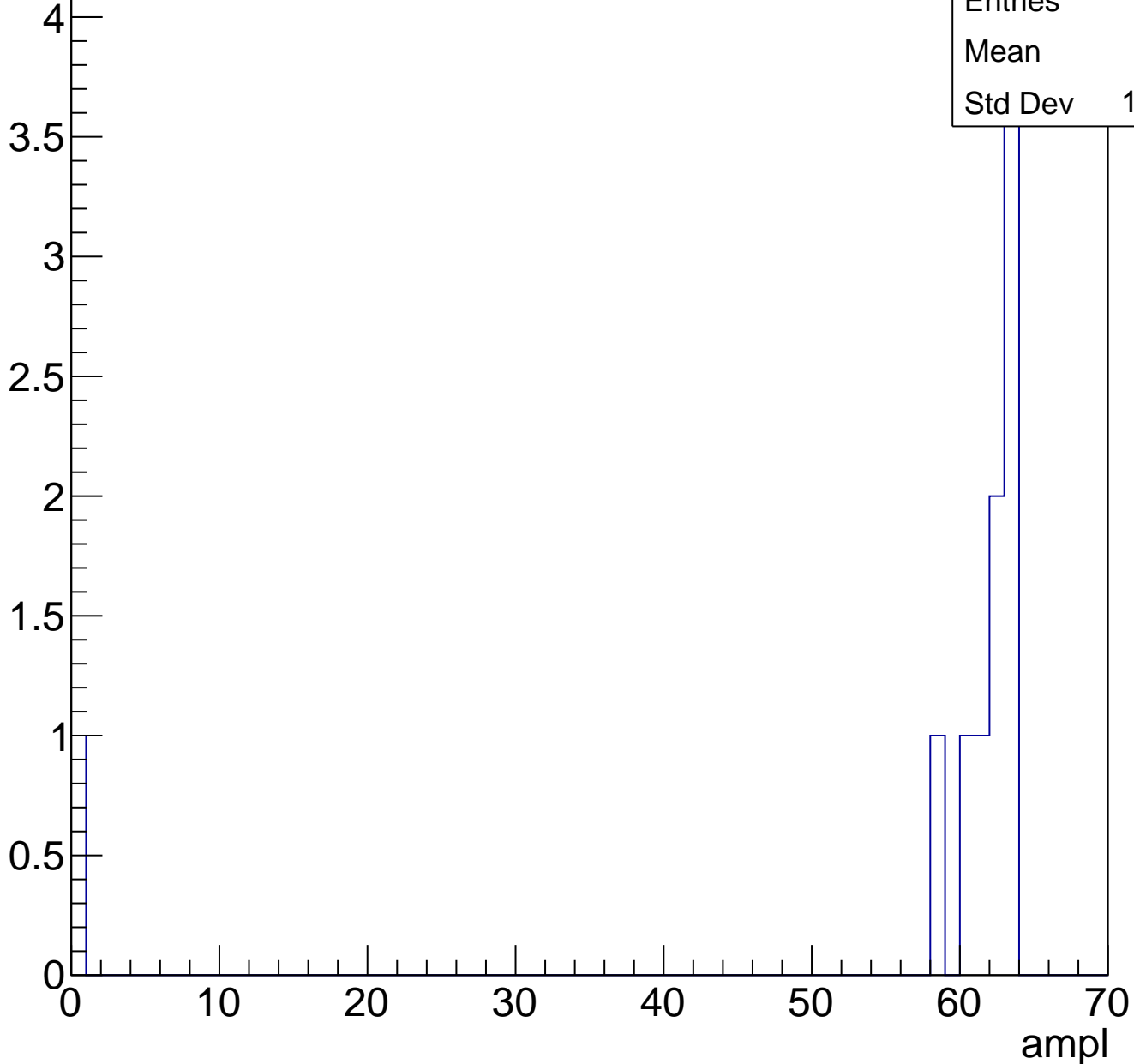
Entries	61
Mean	58.89
Std Dev	2.823



# B1L102S, U3-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch119, adc0

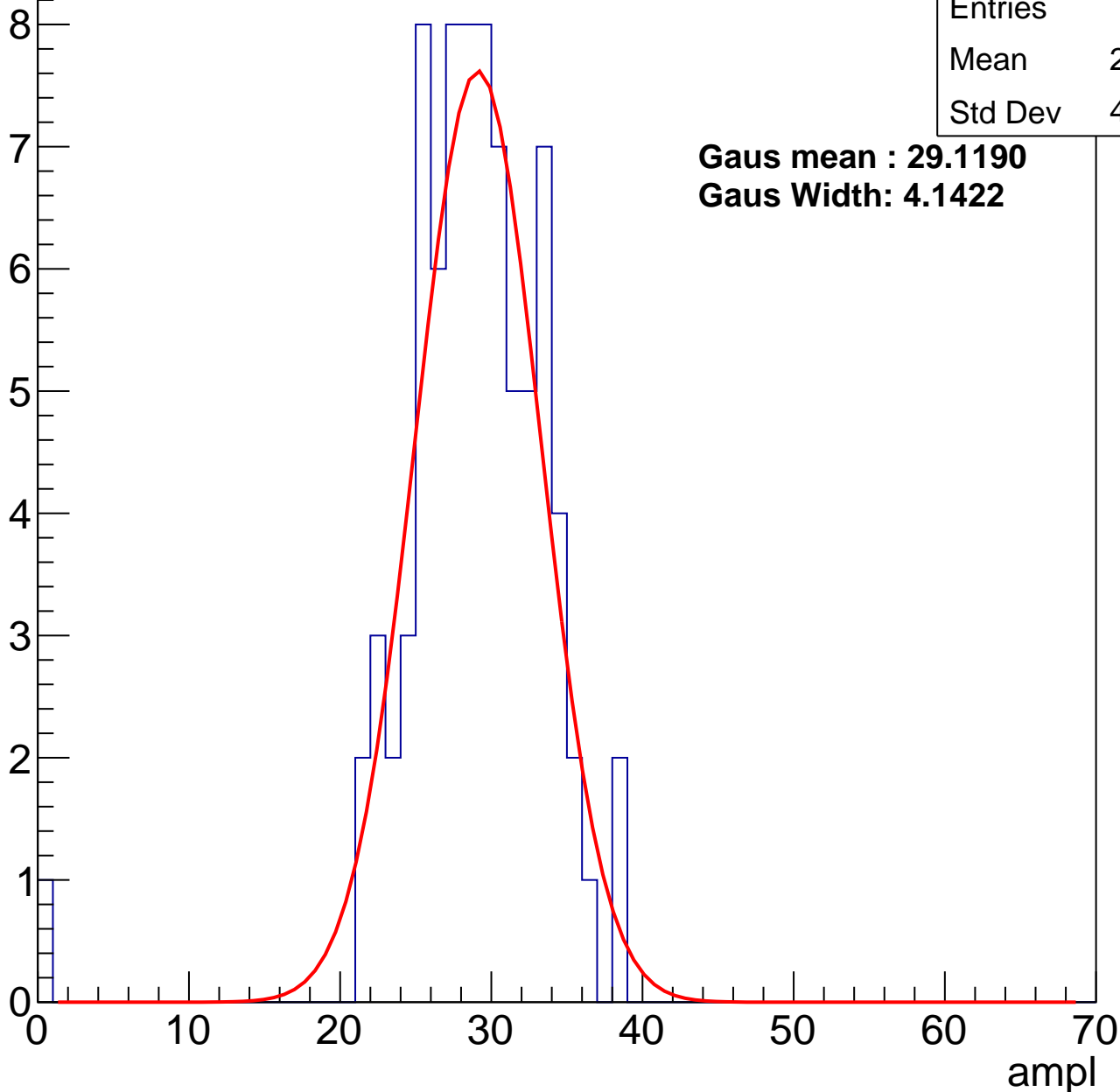
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	28.39
Std Dev	4.965

**Gaus mean : 29.1190**

**Gaus Width: 4.1422**



# B1L102S, U3-ch119, adc1

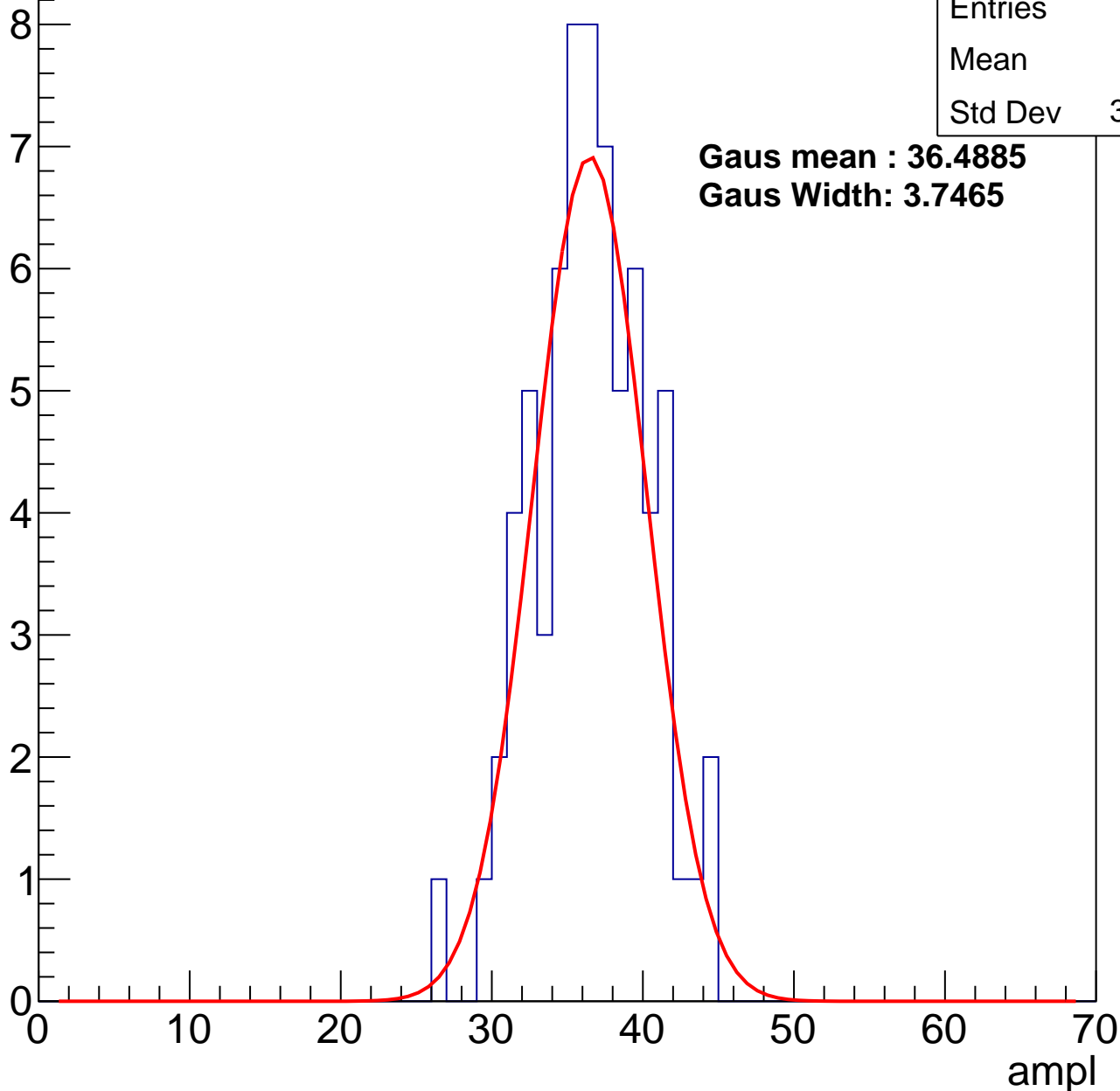
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	36.1
Std Dev	3.695

**Gaus mean : 36.4885**

**Gaus Width: 3.7465**



# B1L102S, U3-ch119, adc2

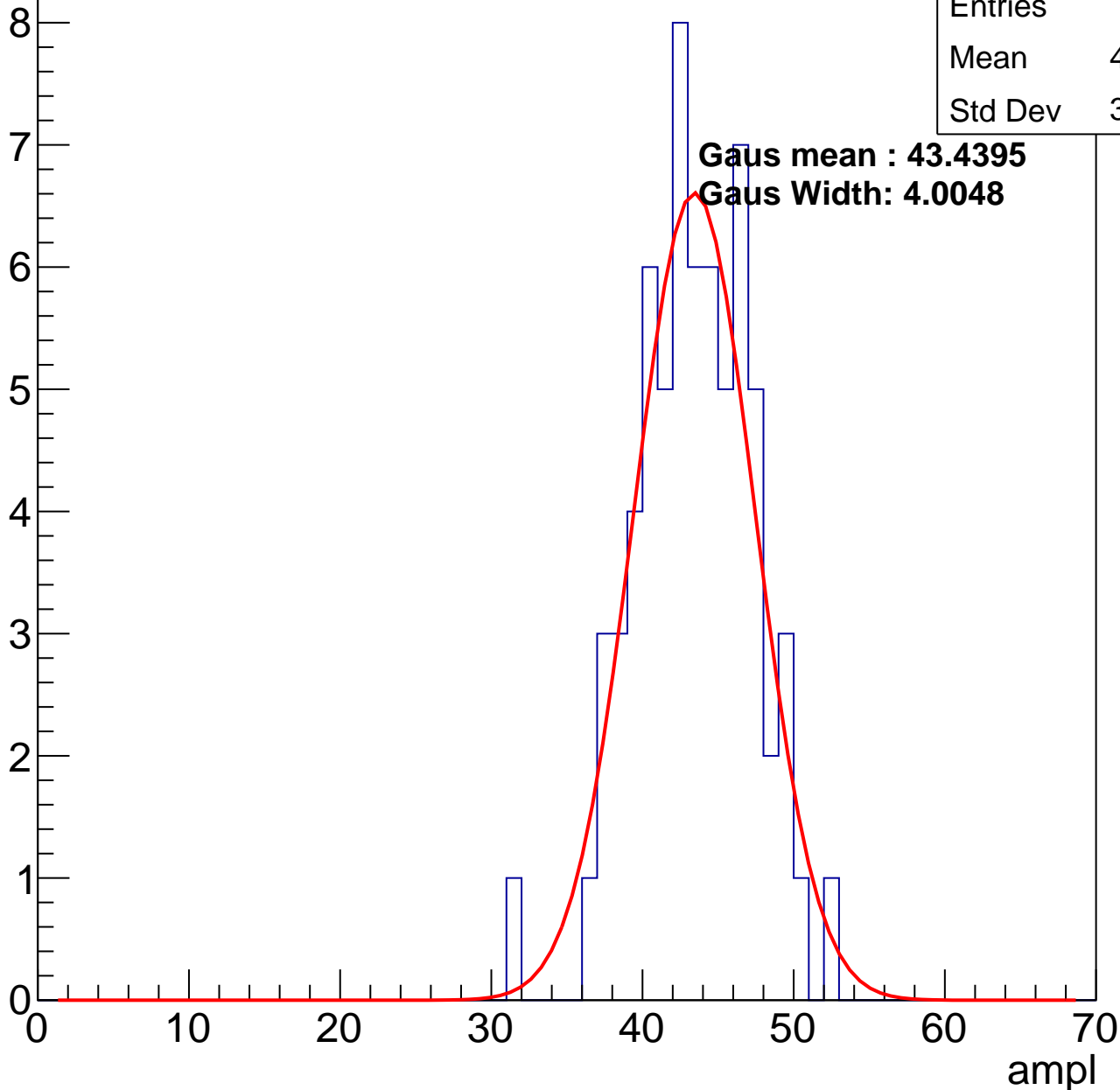
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	42.96
Std Dev	3.822

**Gaus mean : 43.4395**

**Gaus Width: 4.0048**



# B1L102S, U3-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

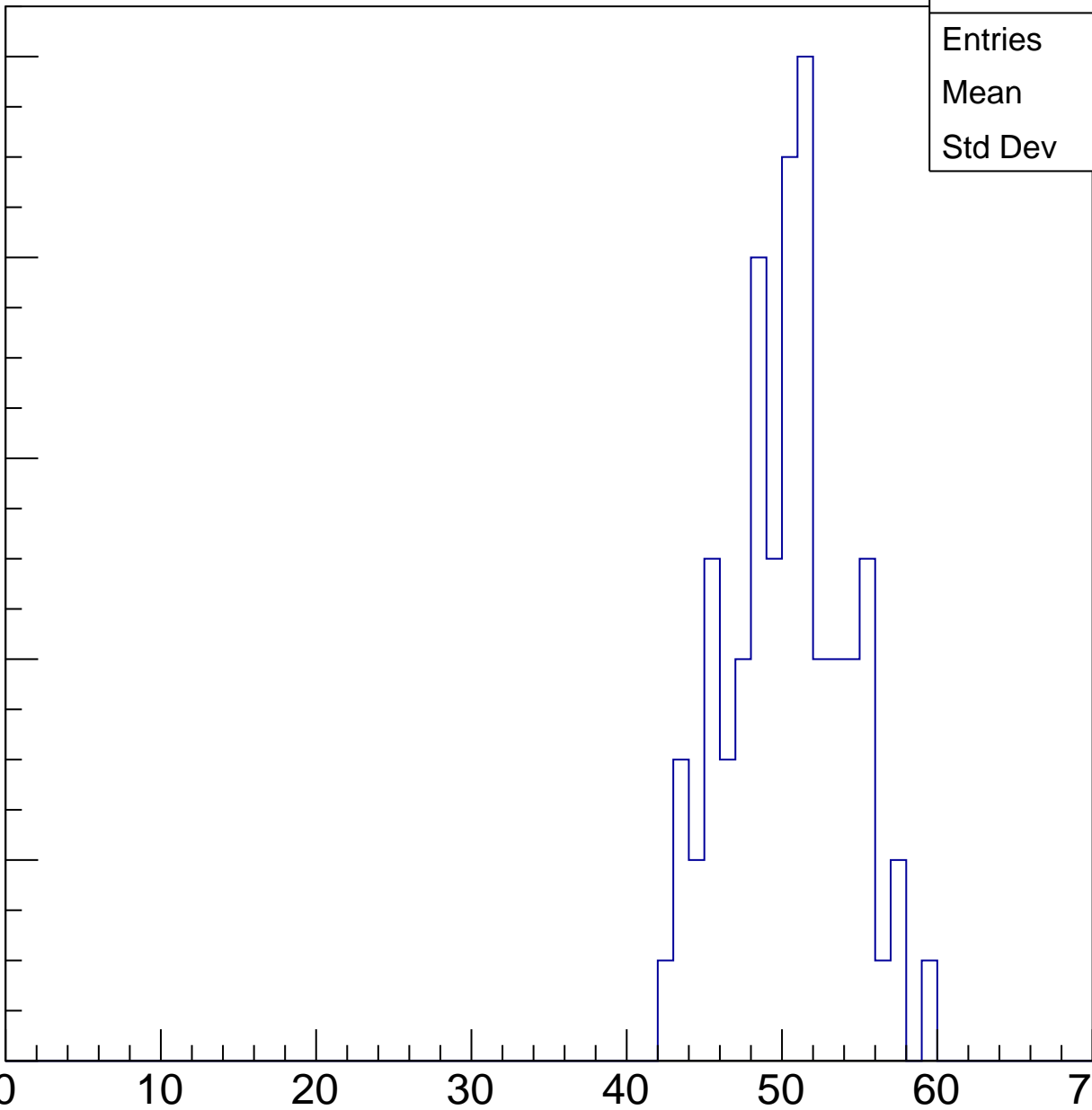
Entries	71
Mean	49.85
Std Dev	3.74

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

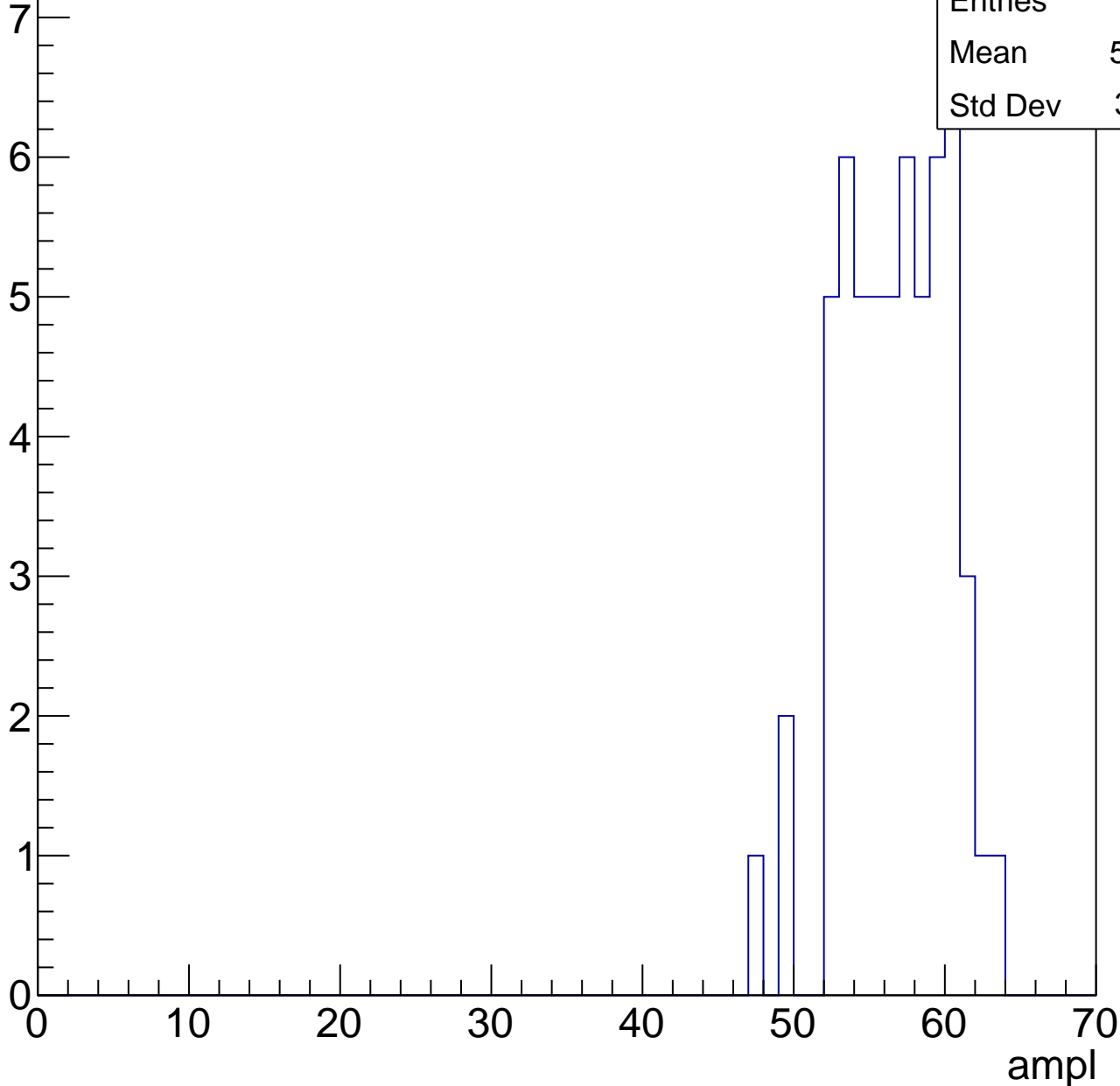


# B1L102S, U3-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	56.24
Std Dev	3.441

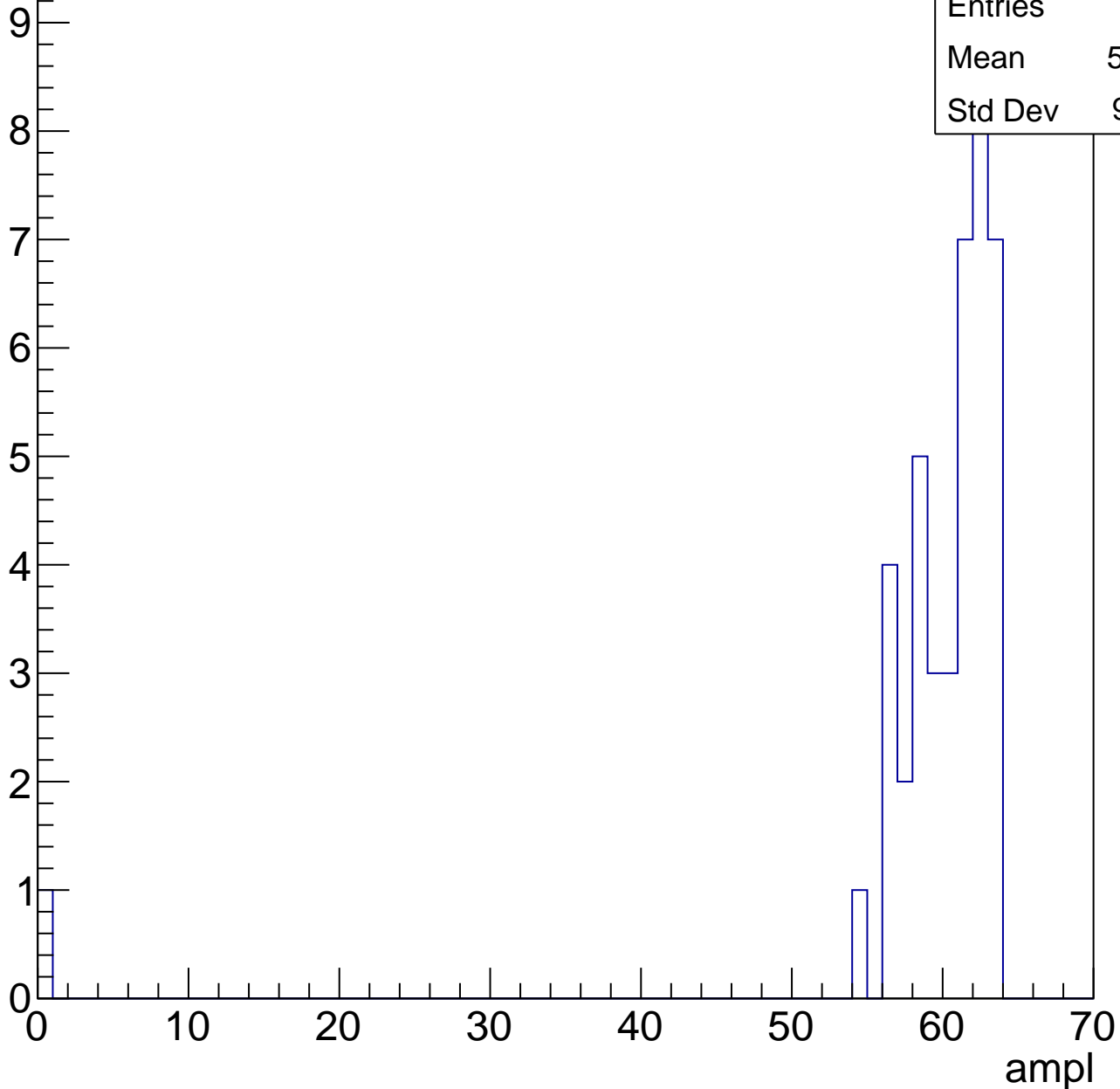


# B1L102S, U3-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	42
Mean	58.69
Std Dev	9.481



# B1L102S, U3-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U3-ch120, adc0

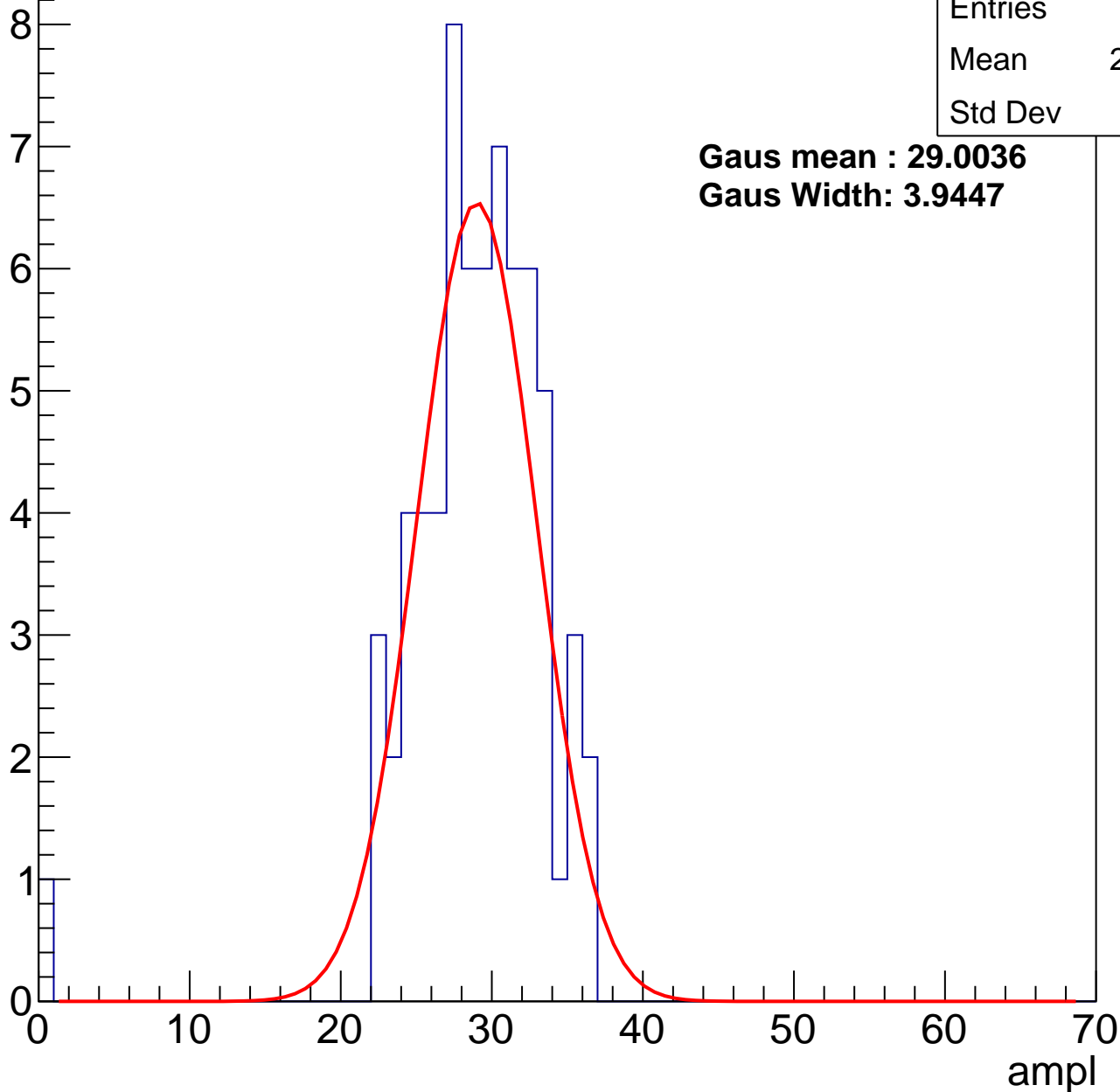
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	28.44
Std Dev	4.96

**Gaus mean : 29.0036**

**Gaus Width: 3.9447**



# B1L102S, U3-ch120, adc1

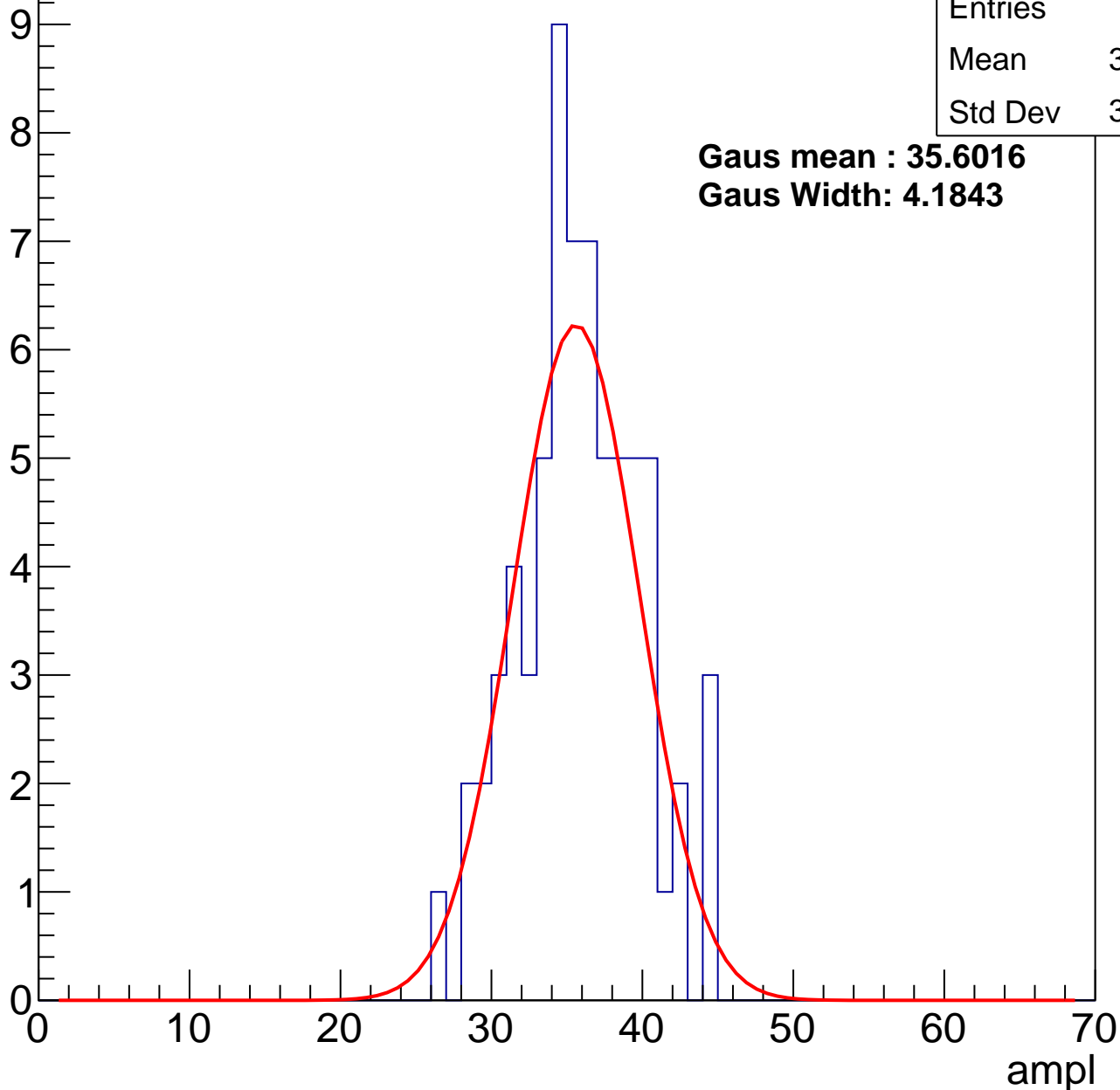
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	35.43
Std Dev	3.969

**Gaus mean : 35.6016**

**Gaus Width: 4.1843**



# B1L102S, U3-ch120, adc2

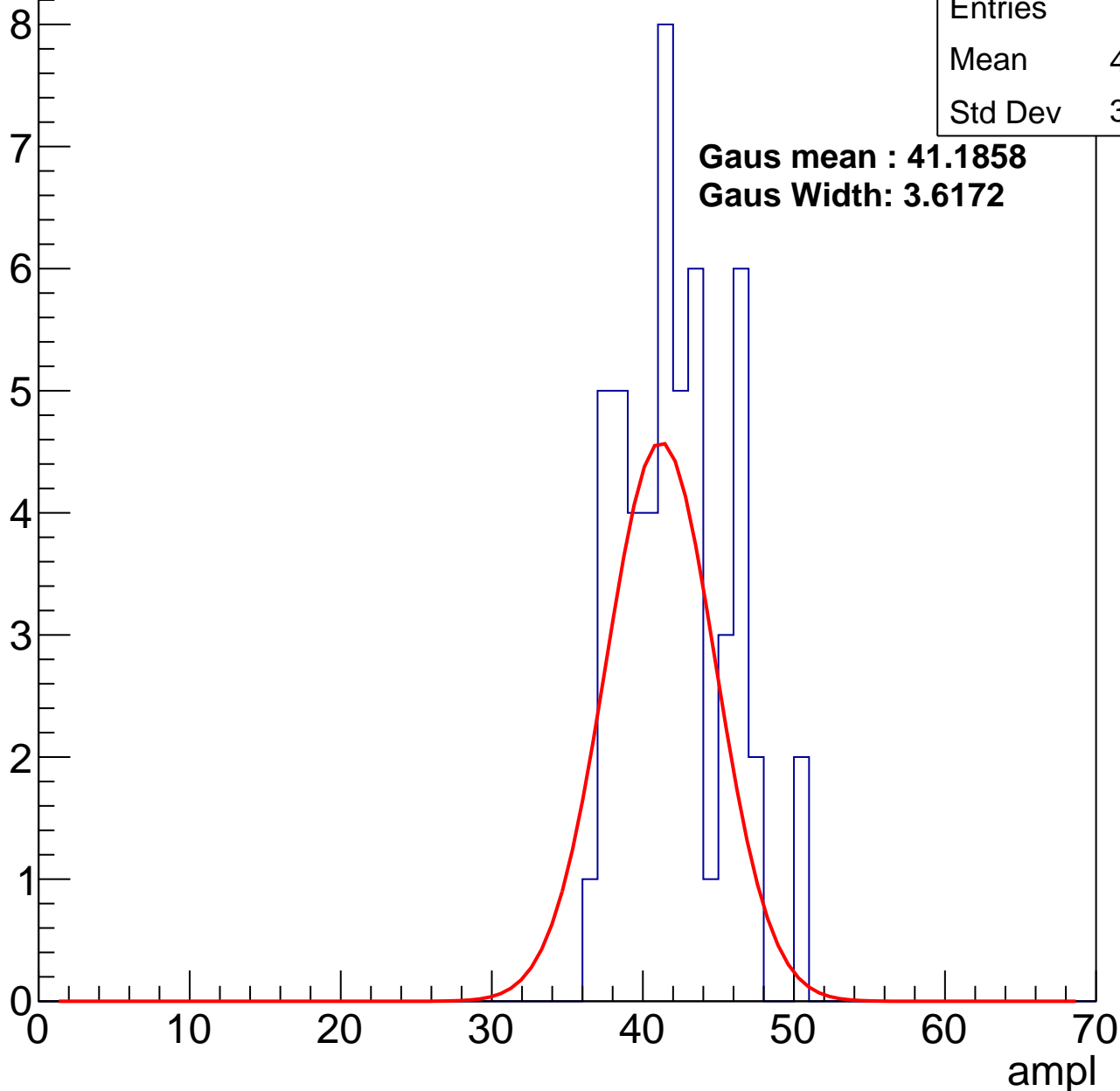
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	41.77
Std Dev	3.423

**Gaus mean : 41.1858**

**Gaus Width: 3.6172**

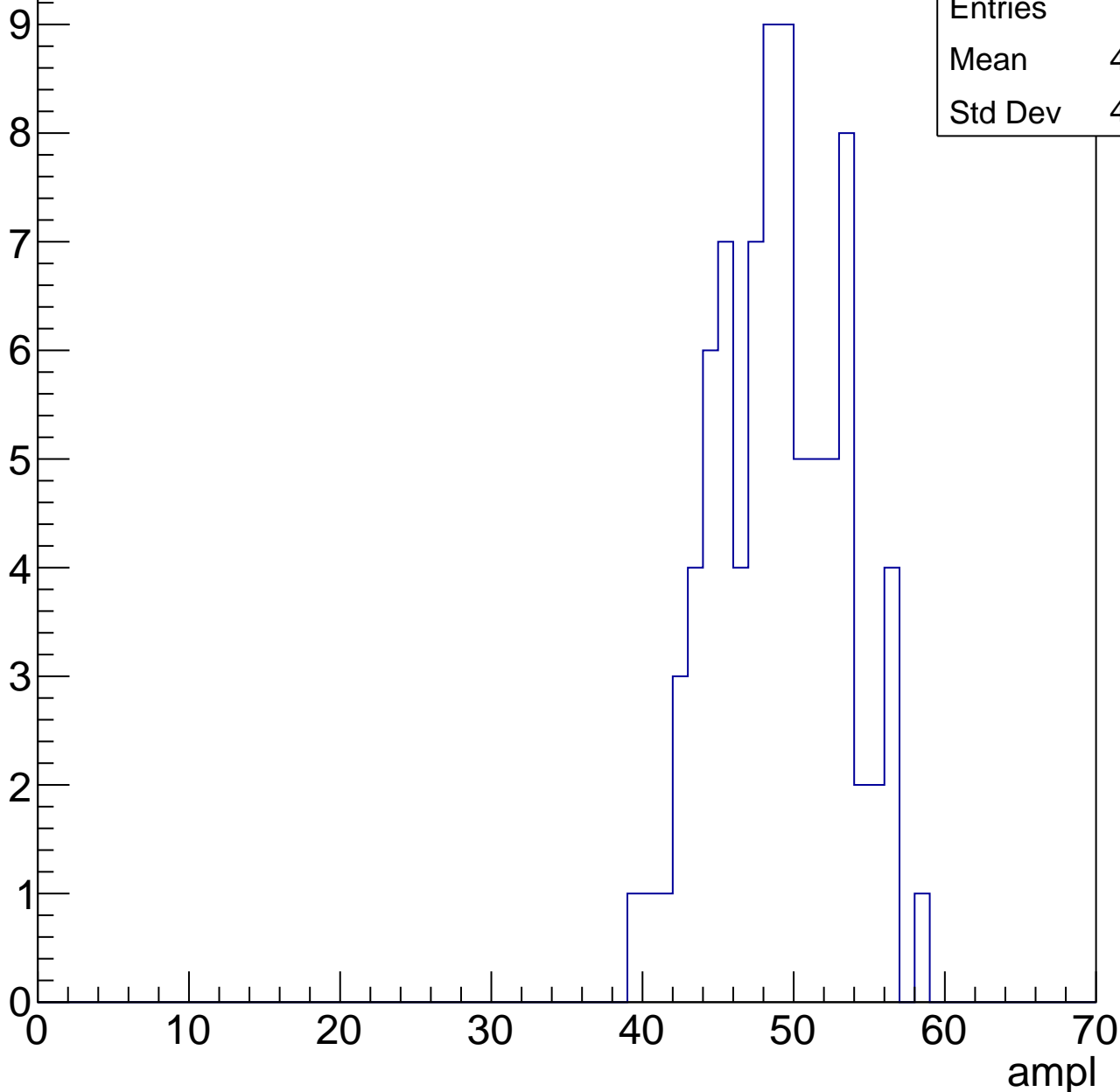


# B1L102S, U3-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	48.48
Std Dev	4.148

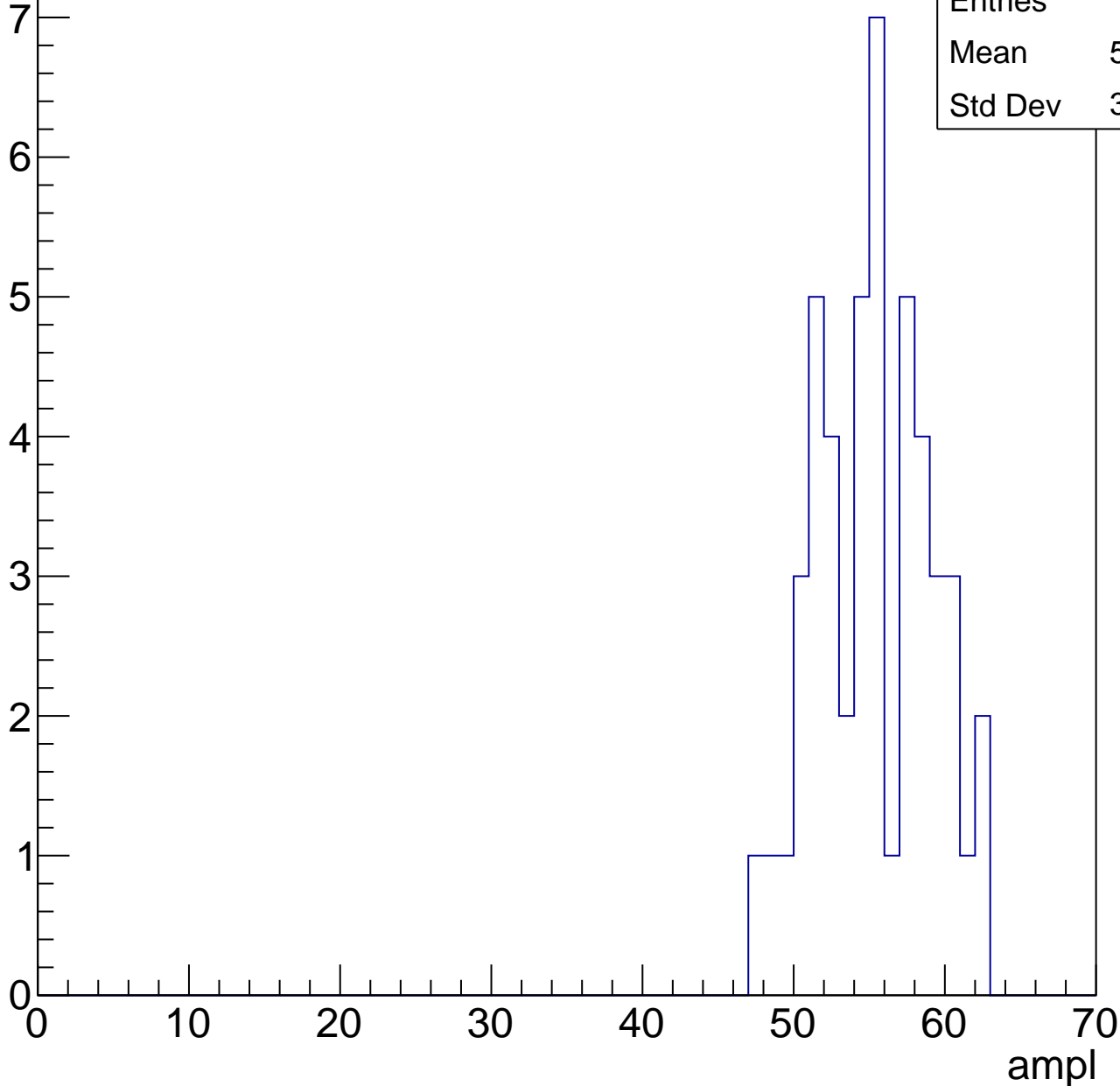


# B1L102S, U3-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	54.85
Std Dev	3.725

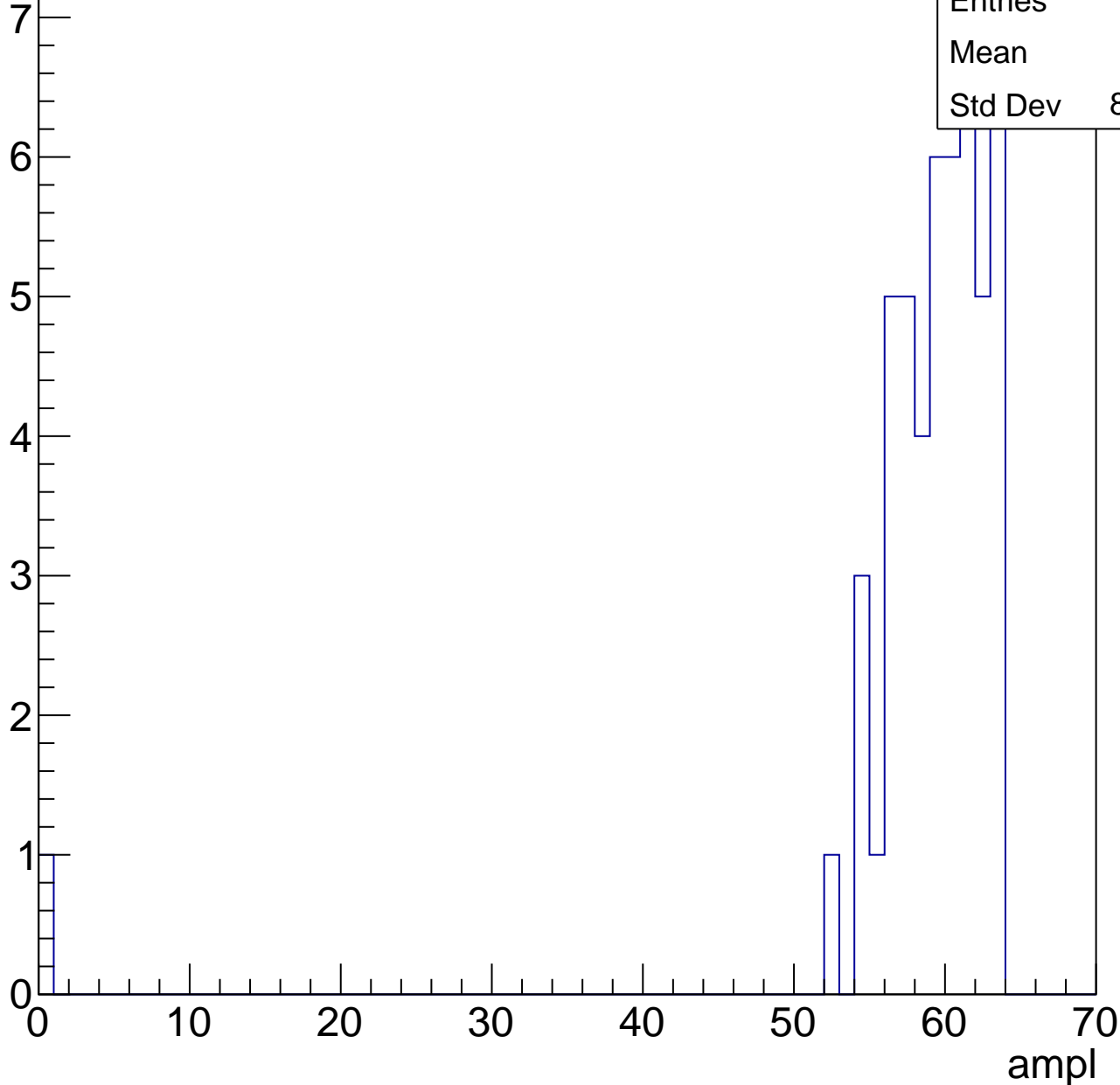


# B1L102S, U3-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	58
Std Dev	8.666



# B1L102S, U3-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries	11
Mean	61.27
Std Dev	1.601



# B1L102S, U3-ch120, adc7

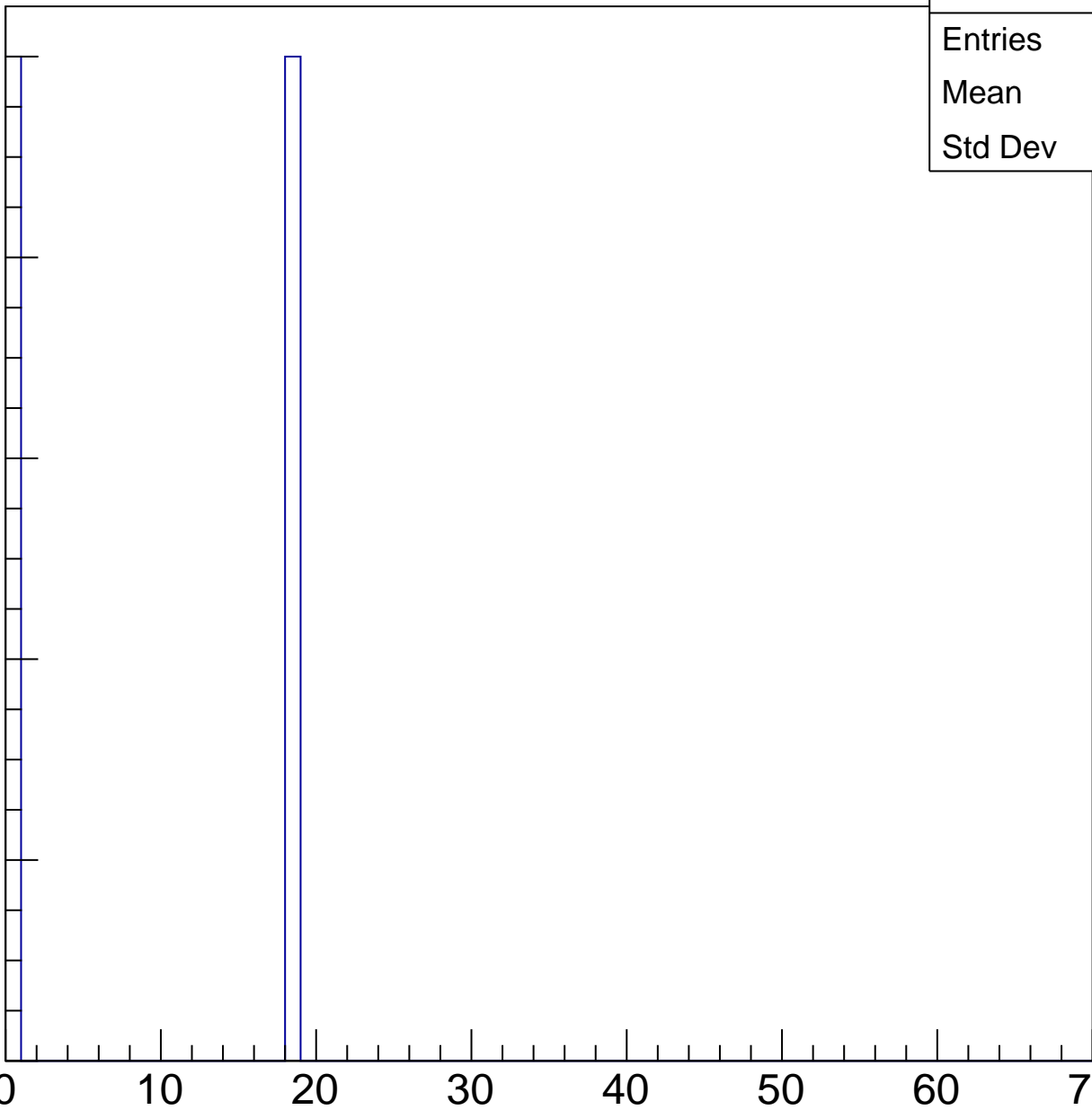
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	9
Std Dev	9

ampl



# B1L102S, U3-ch121, adc0

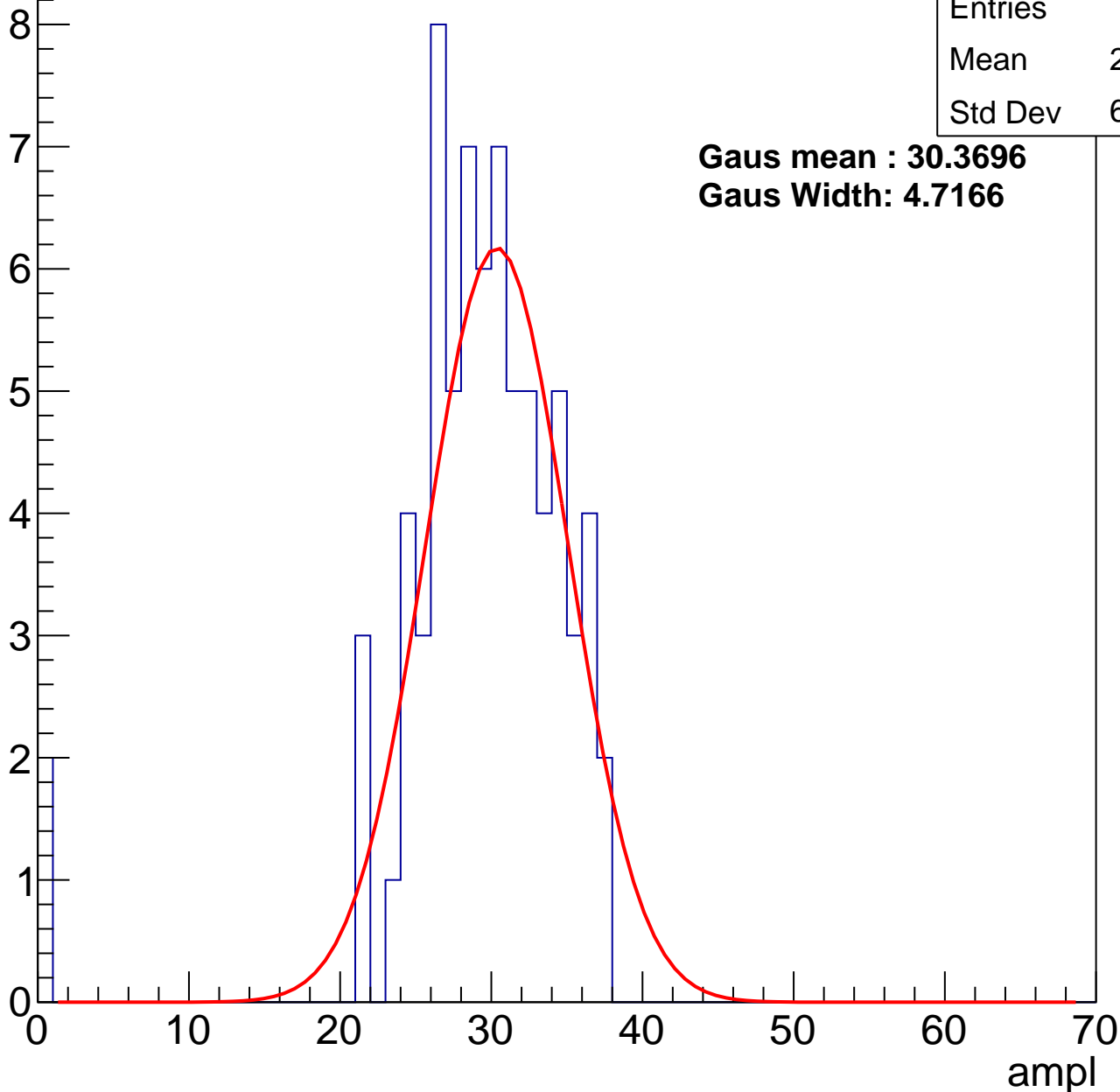
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	28.65
Std Dev	6.196

**Gaus mean : 30.3696**

**Gaus Width: 4.7166**



# B1L102S, U3-ch121, adc1

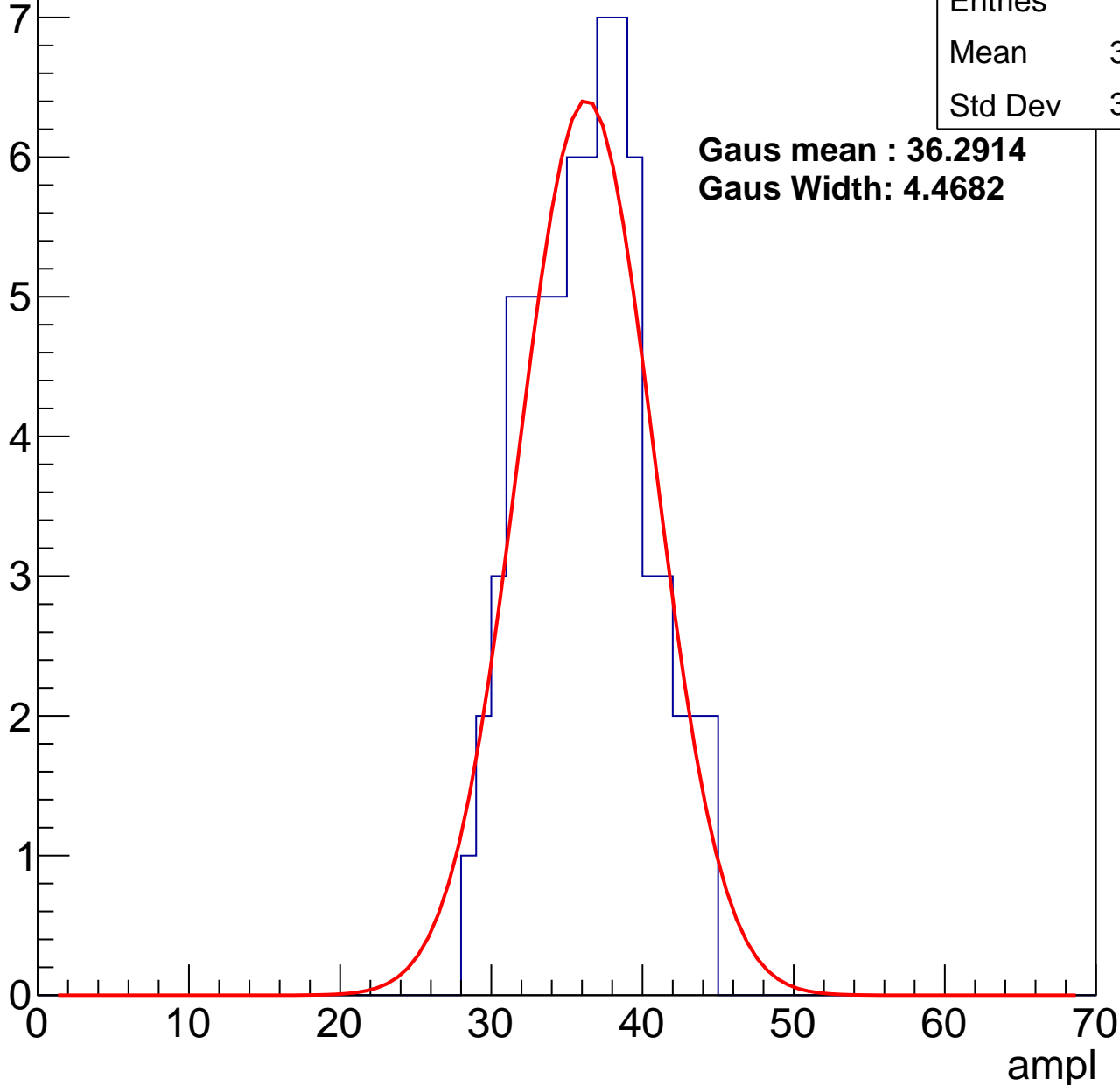
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	35.89
Std Dev	3.882

**Gaus mean : 36.2914**

**Gaus Width: 4.4682**



# B1L102S, U3-ch121, adc2

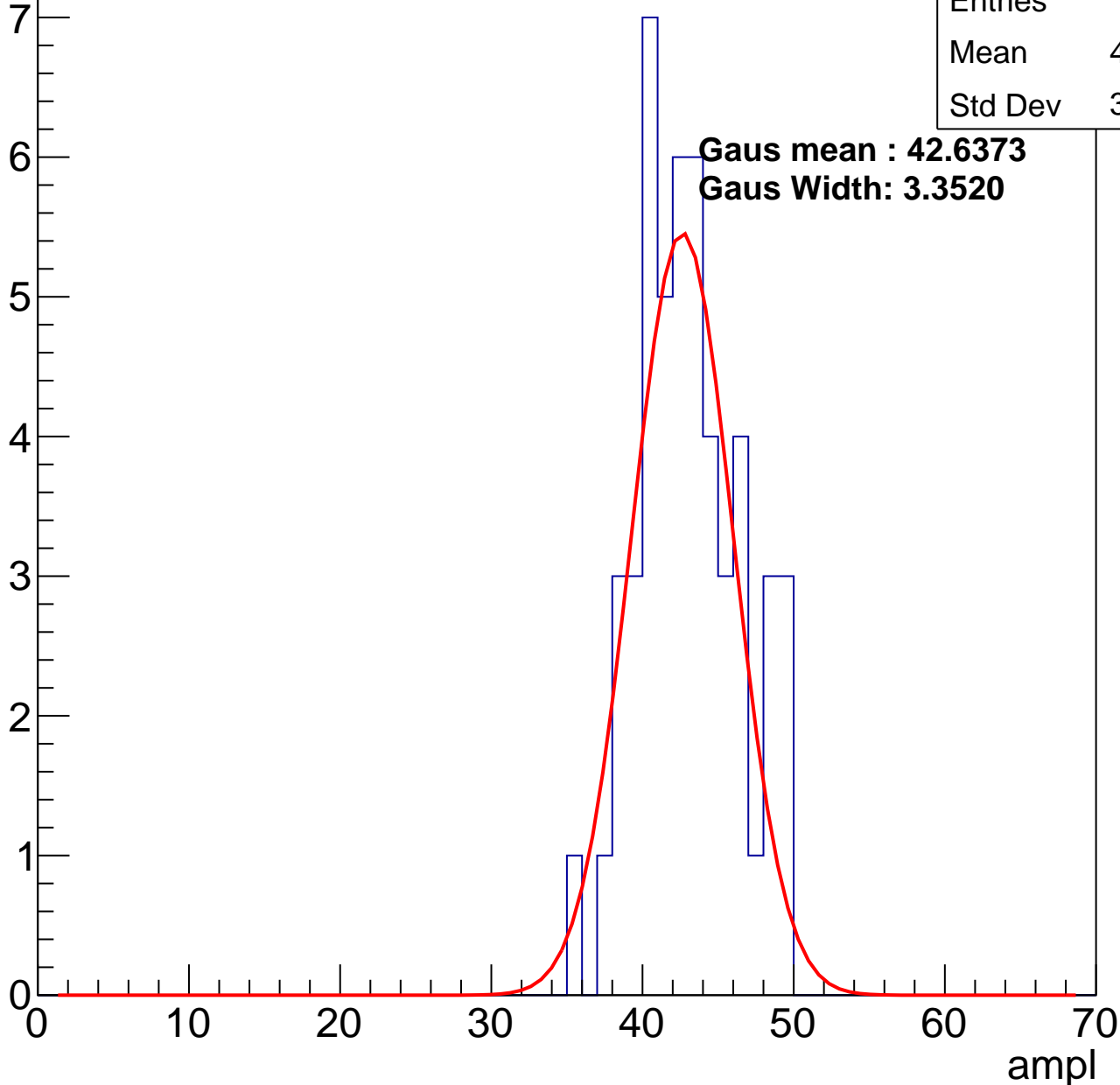
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	42.62
Std Dev	3.334

**Gaus mean : 42.6373**

**Gaus Width: 3.3520**

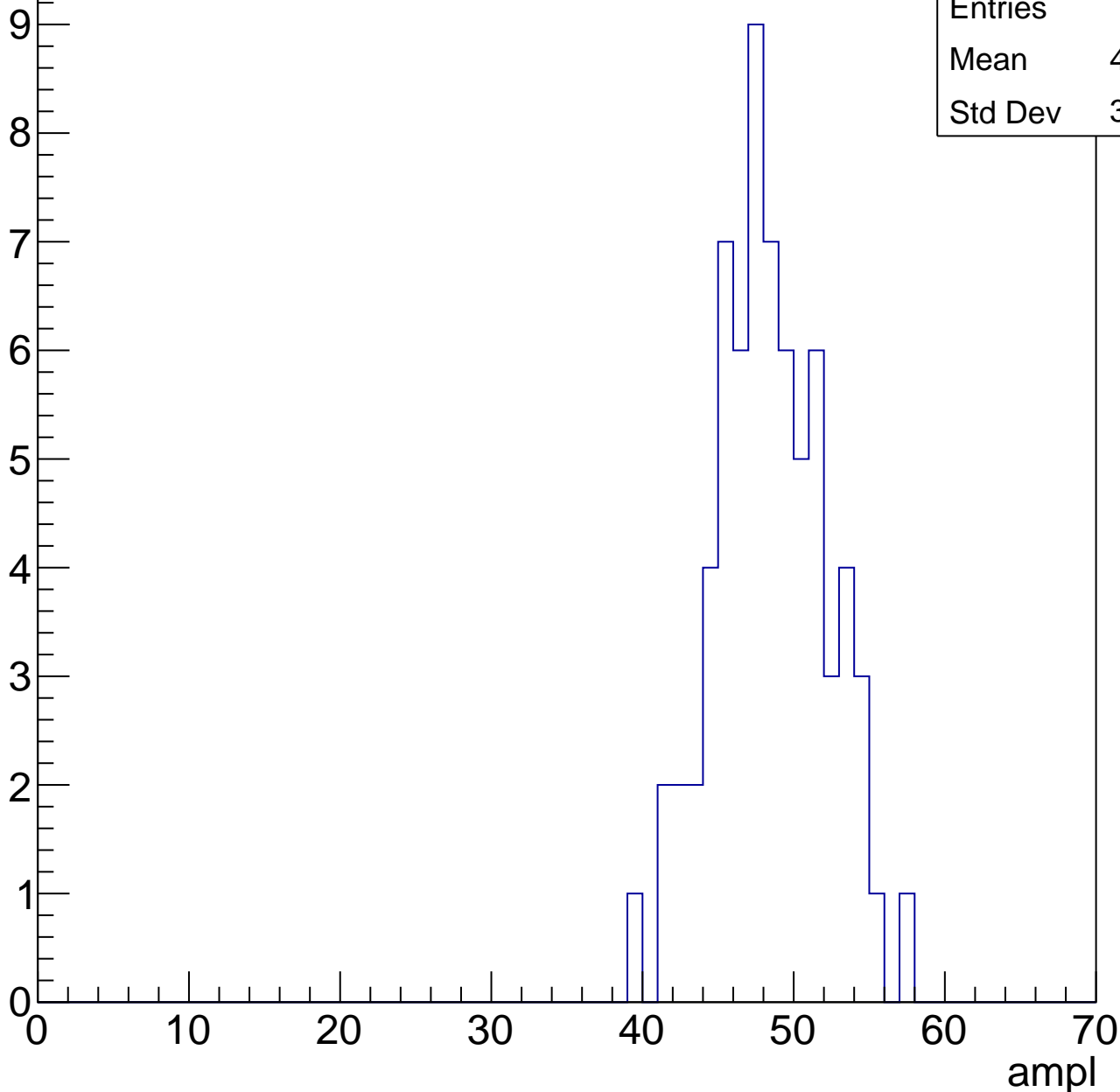


# B1L102S, U3-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	47.96
Std Dev	3.665

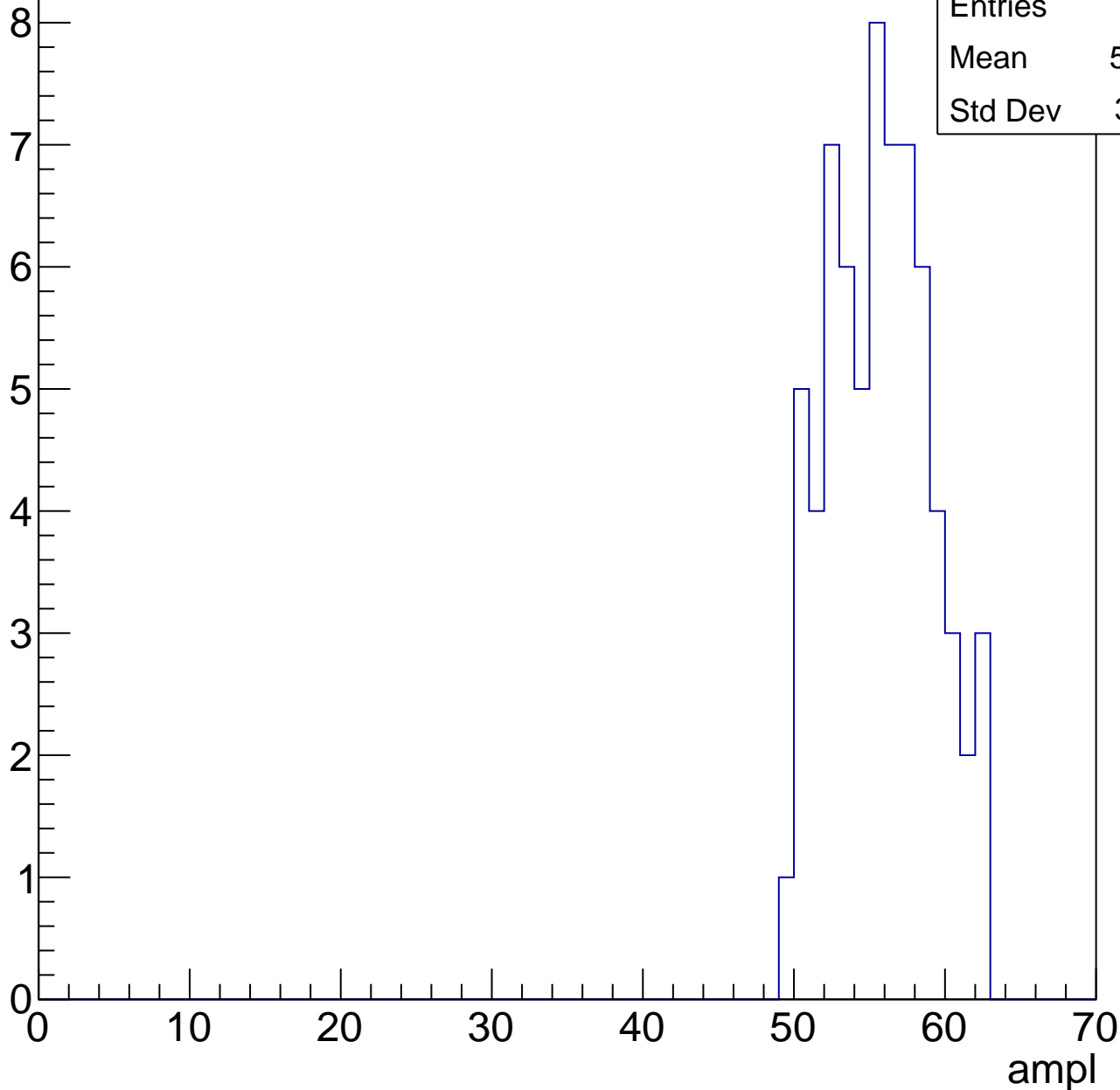


# B1L102S, U3-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	55.26
Std Dev	3.341

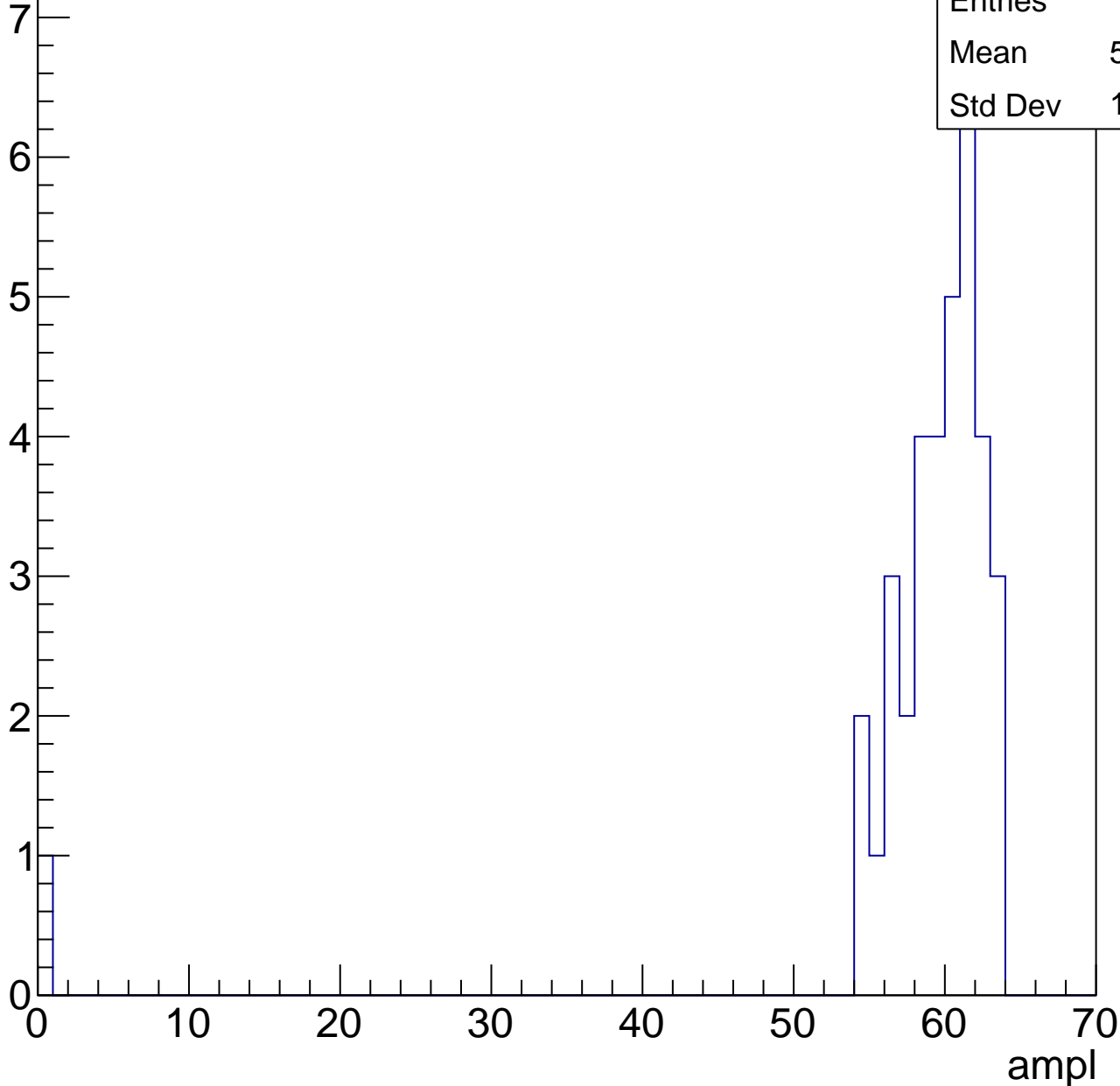


# B1L102S, U3-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	36
Mean	57.69
Std Dev	10.06

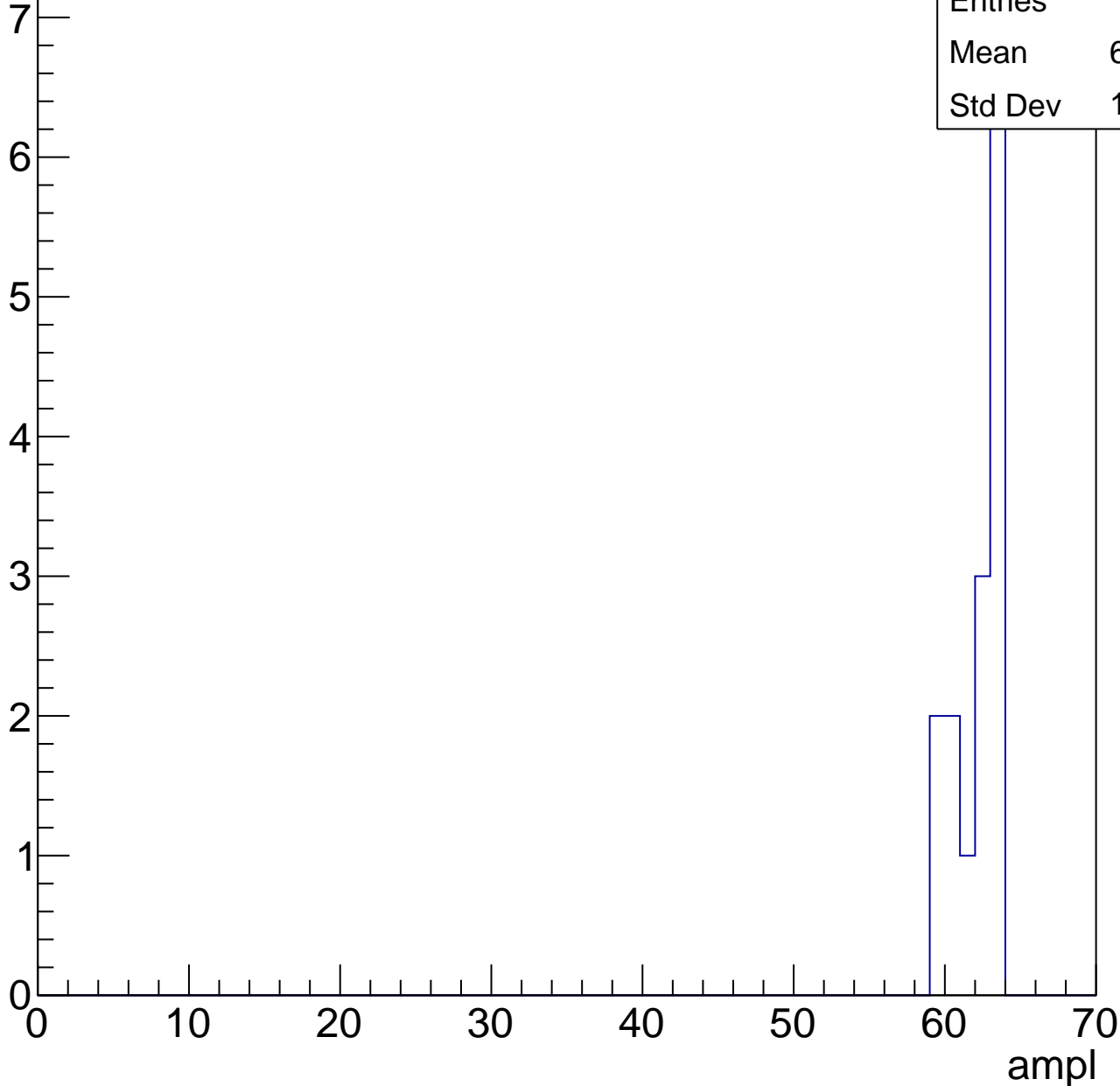


# B1L102S, U3-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	15
Mean	61.73
Std Dev	1.482





# B1L102S, U3-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U3-ch122, adc0

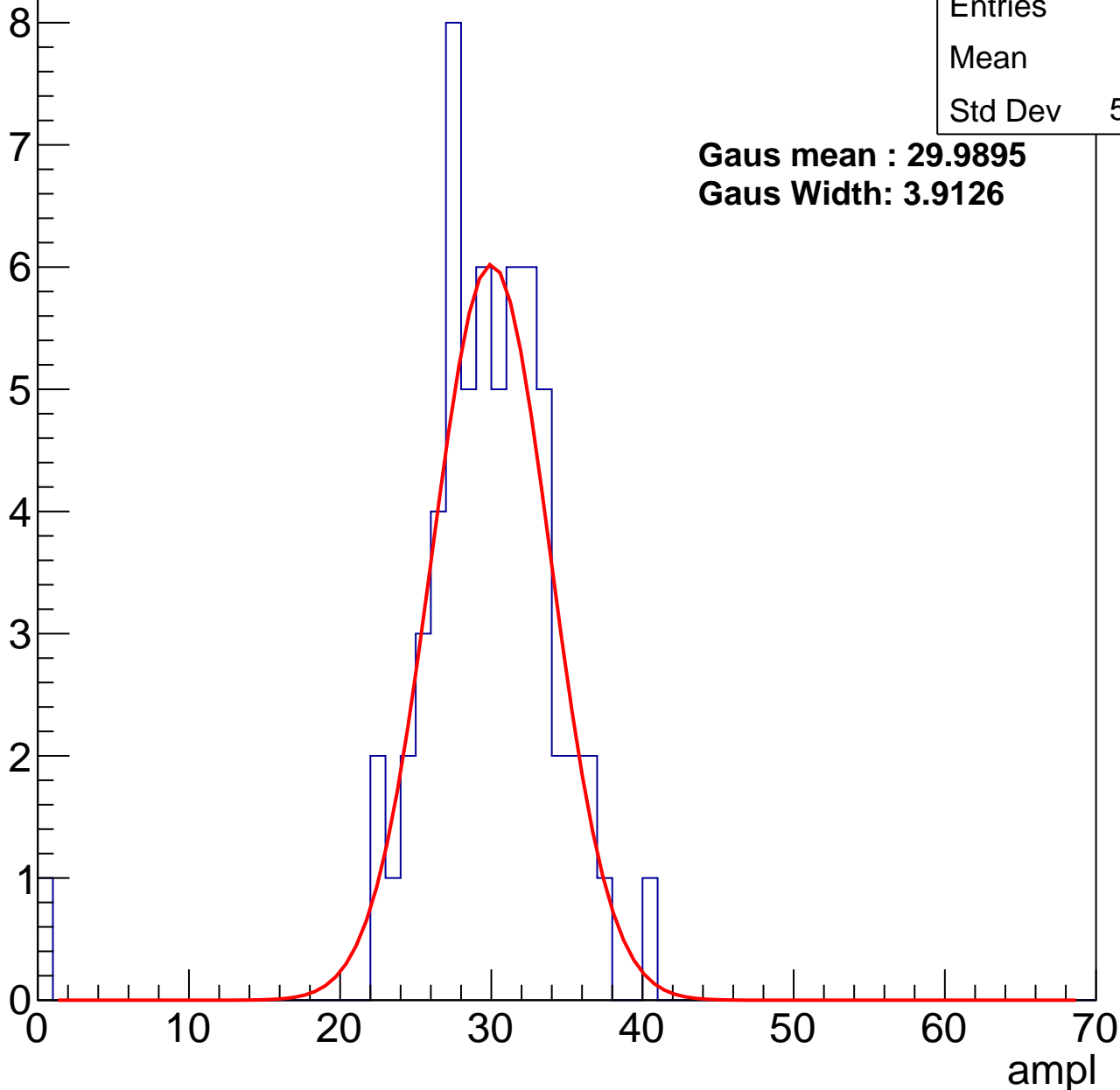
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	29.1
Std Dev	5.257

**Gaus mean : 29.9895**

**Gaus Width: 3.9126**



# B1L102S, U3-ch122, adc1

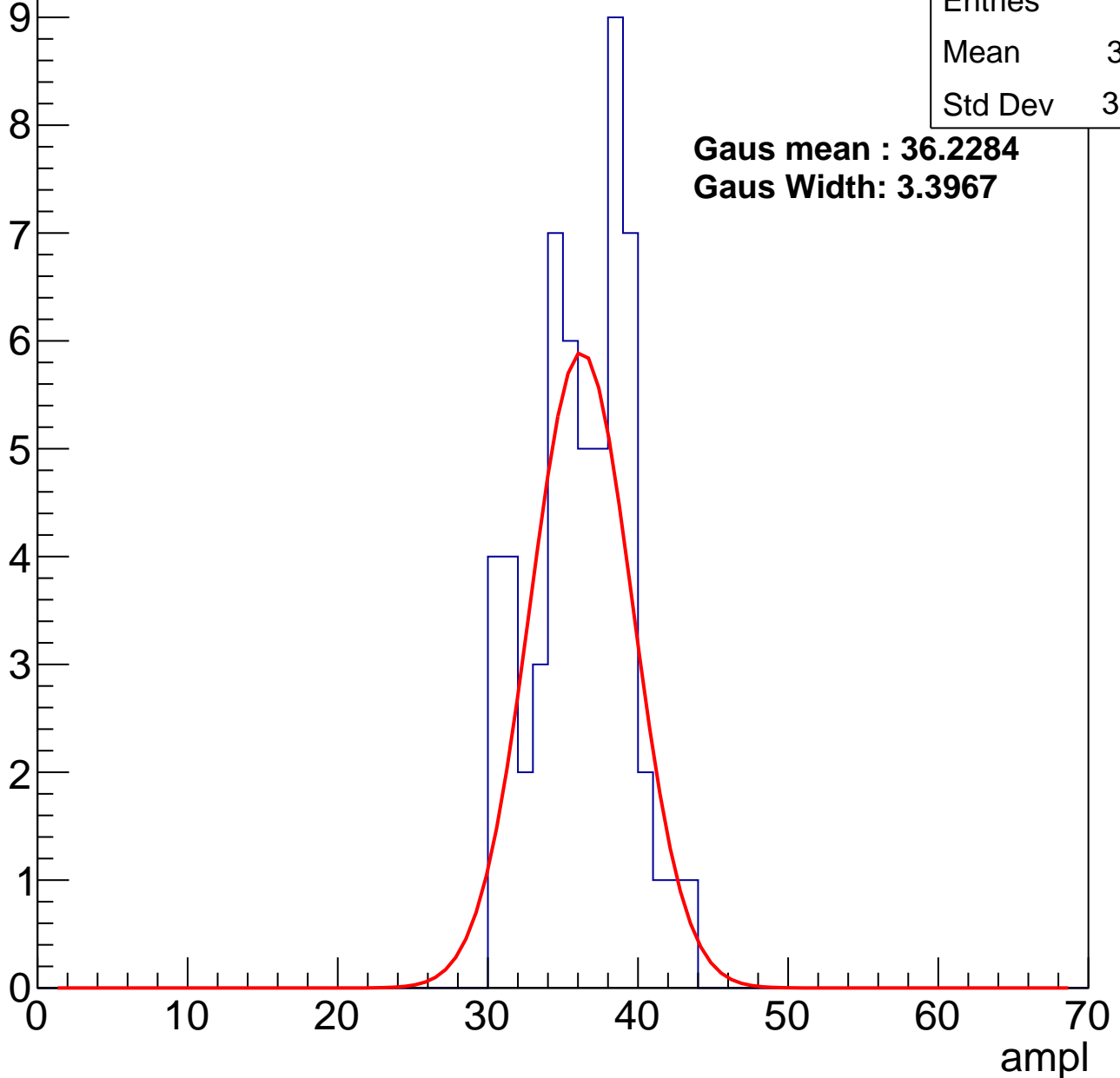
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	35.81
Std Dev	3.192

**Gaus mean : 36.2284**

**Gaus Width: 3.3967**



# B1L102S, U3-ch122, adc2

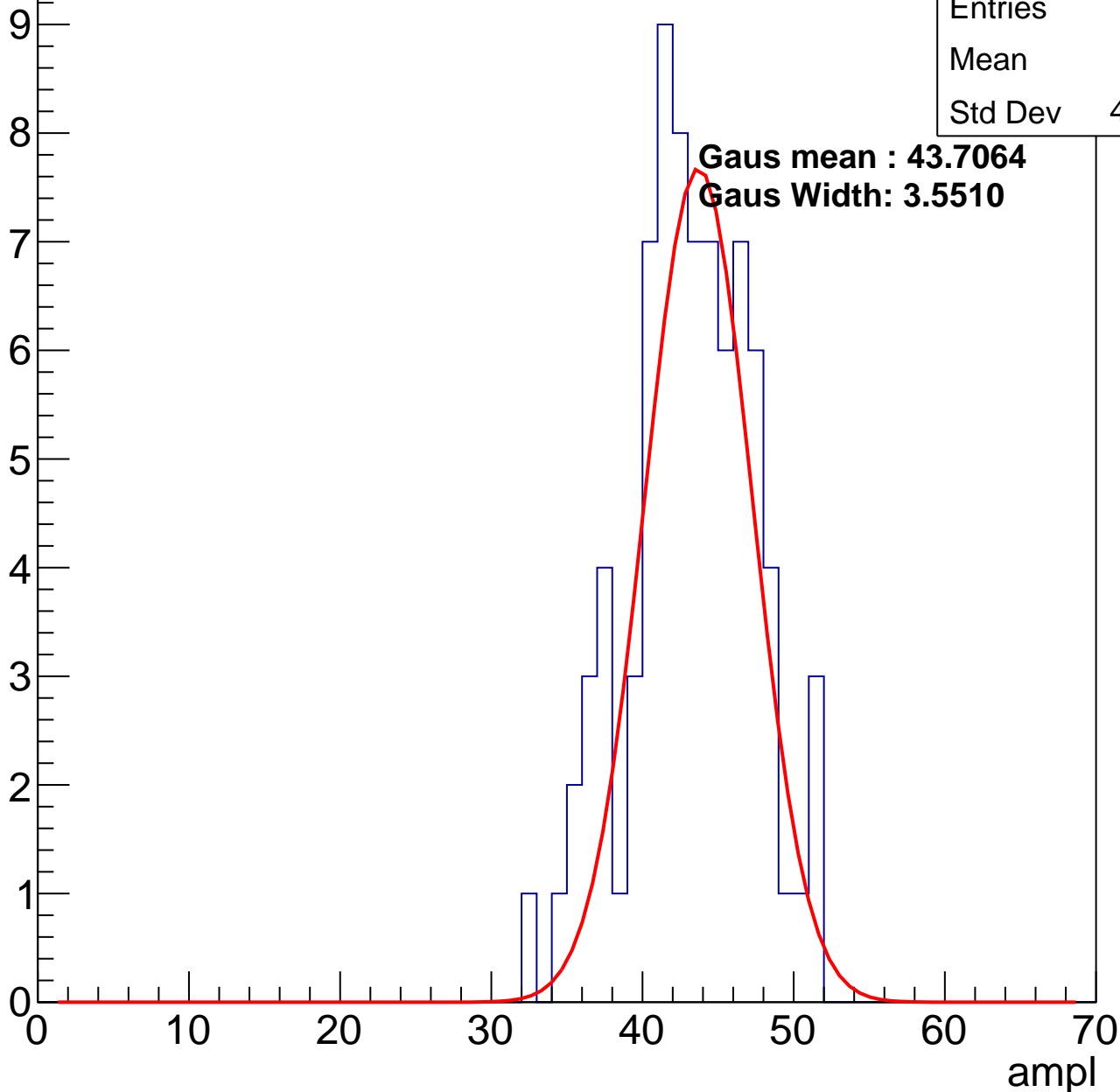
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	81
Mean	42.7
Std Dev	4.099

**Gaus mean : 43.7064**

**Gaus Width: 3.5510**

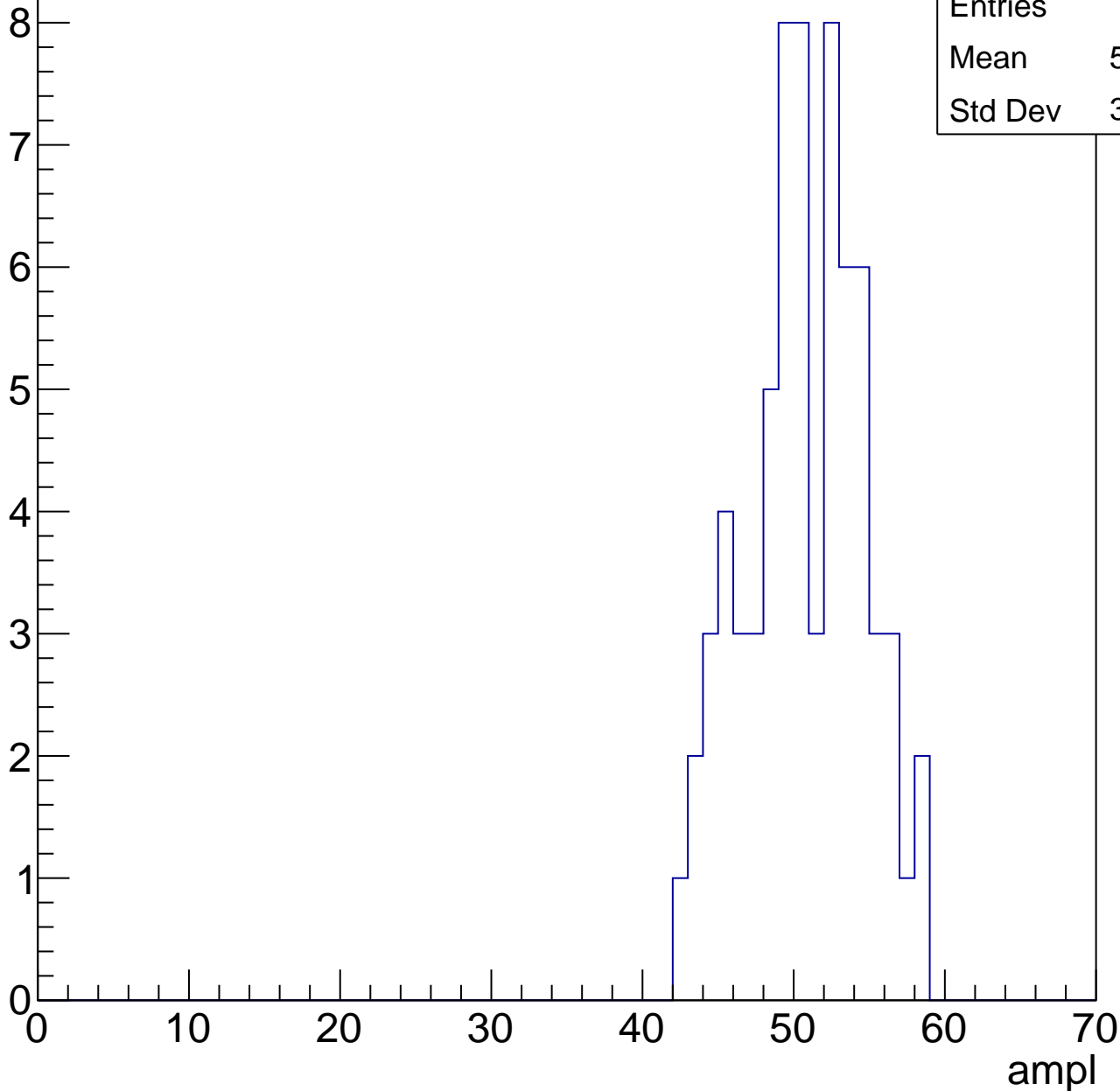


# B1L102S, U3-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	50.26
Std Dev	3.832



# B1L102S, U3-ch122, adc4

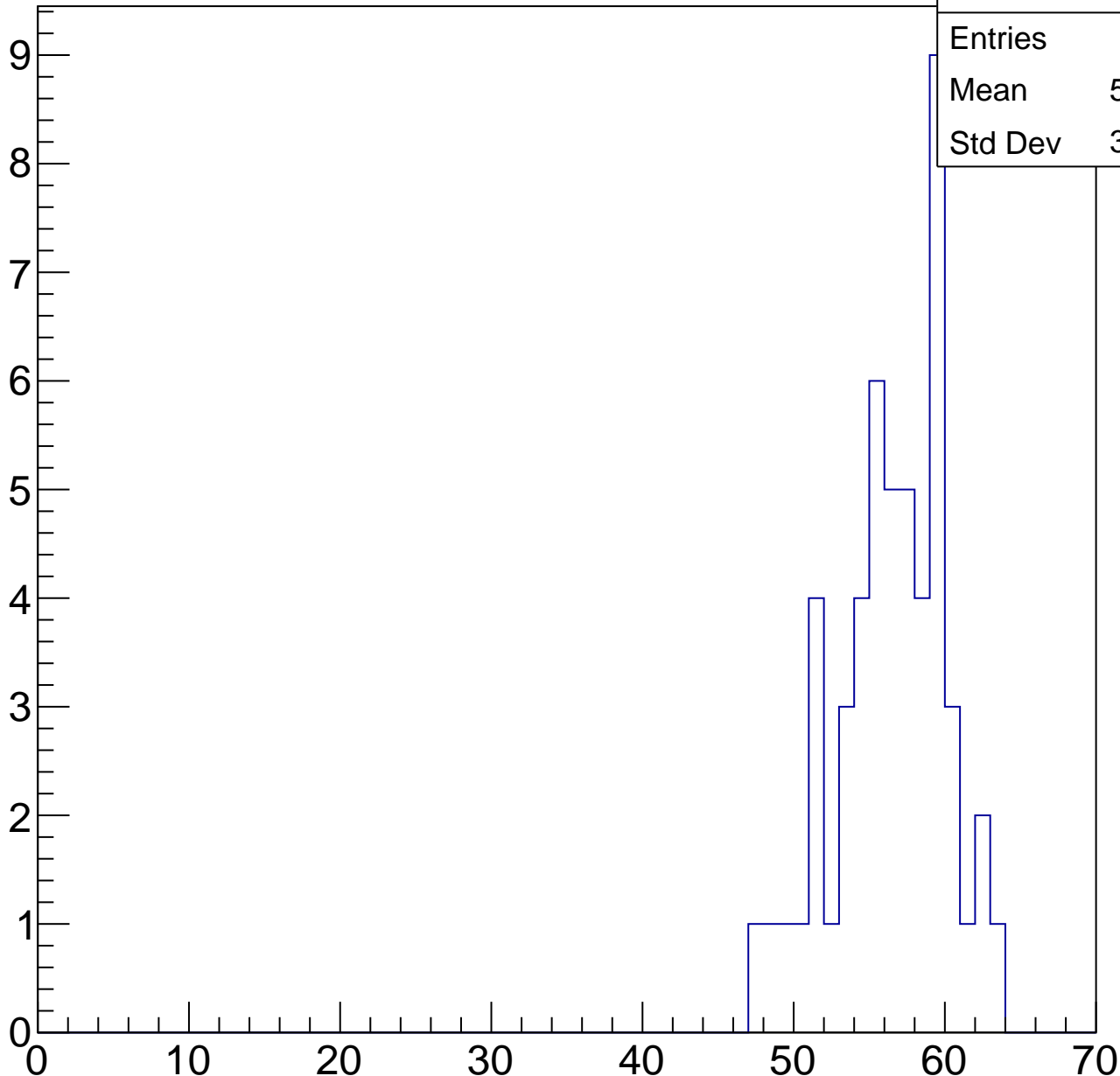
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	52
Mean	55.98
Std Dev	3.645

ampl



# B1L102S, U3-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	35
Mean	57.91
Std Dev	10.32

ampl

0

10

20

30

40

50

60

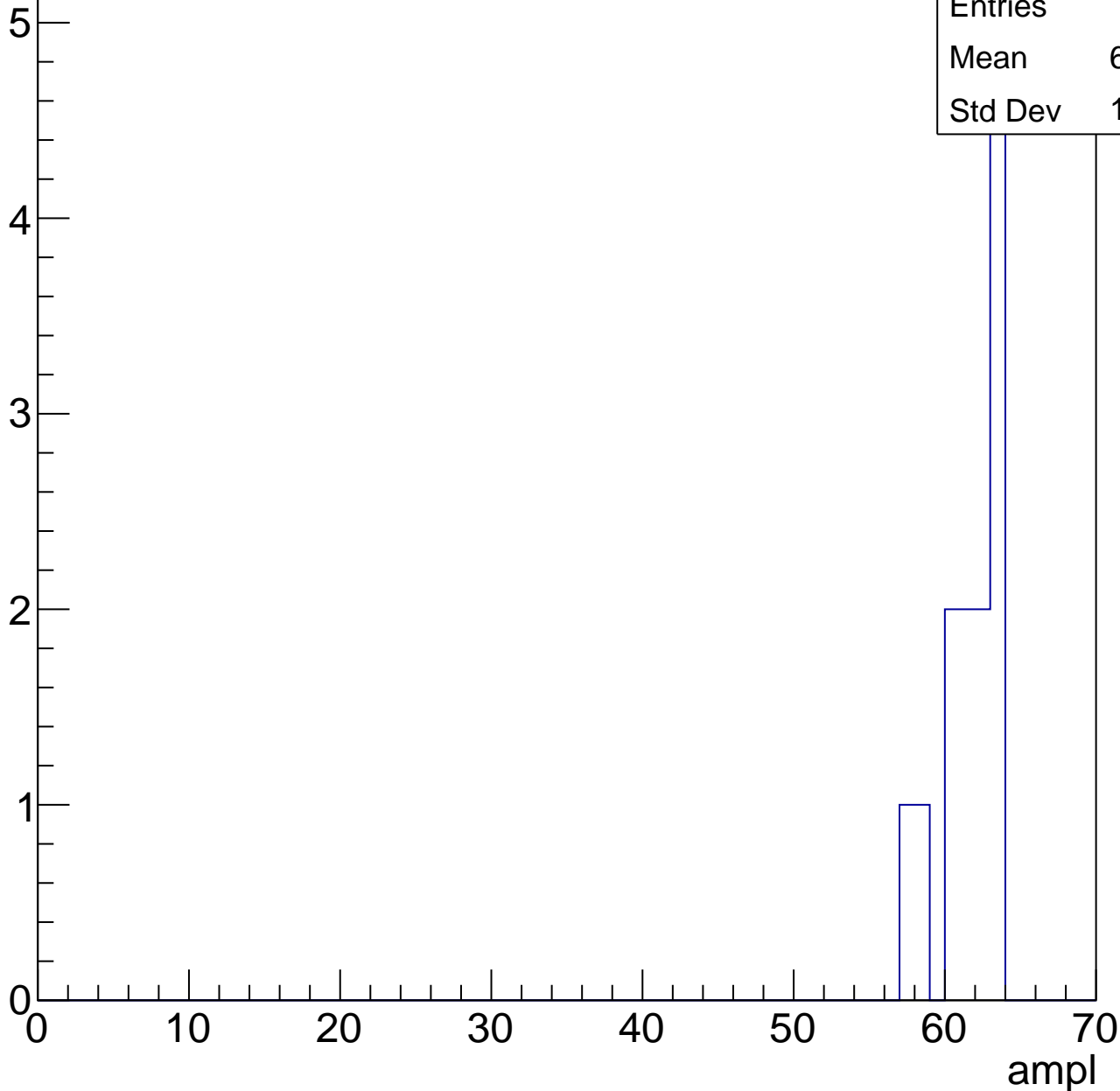
70

# B1L102S, U3-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	13
Mean	61.23
Std Dev	1.928





# B1L102S, U3-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	9.5
Std Dev	9.5

# B1L102S, U3-ch123, adc0

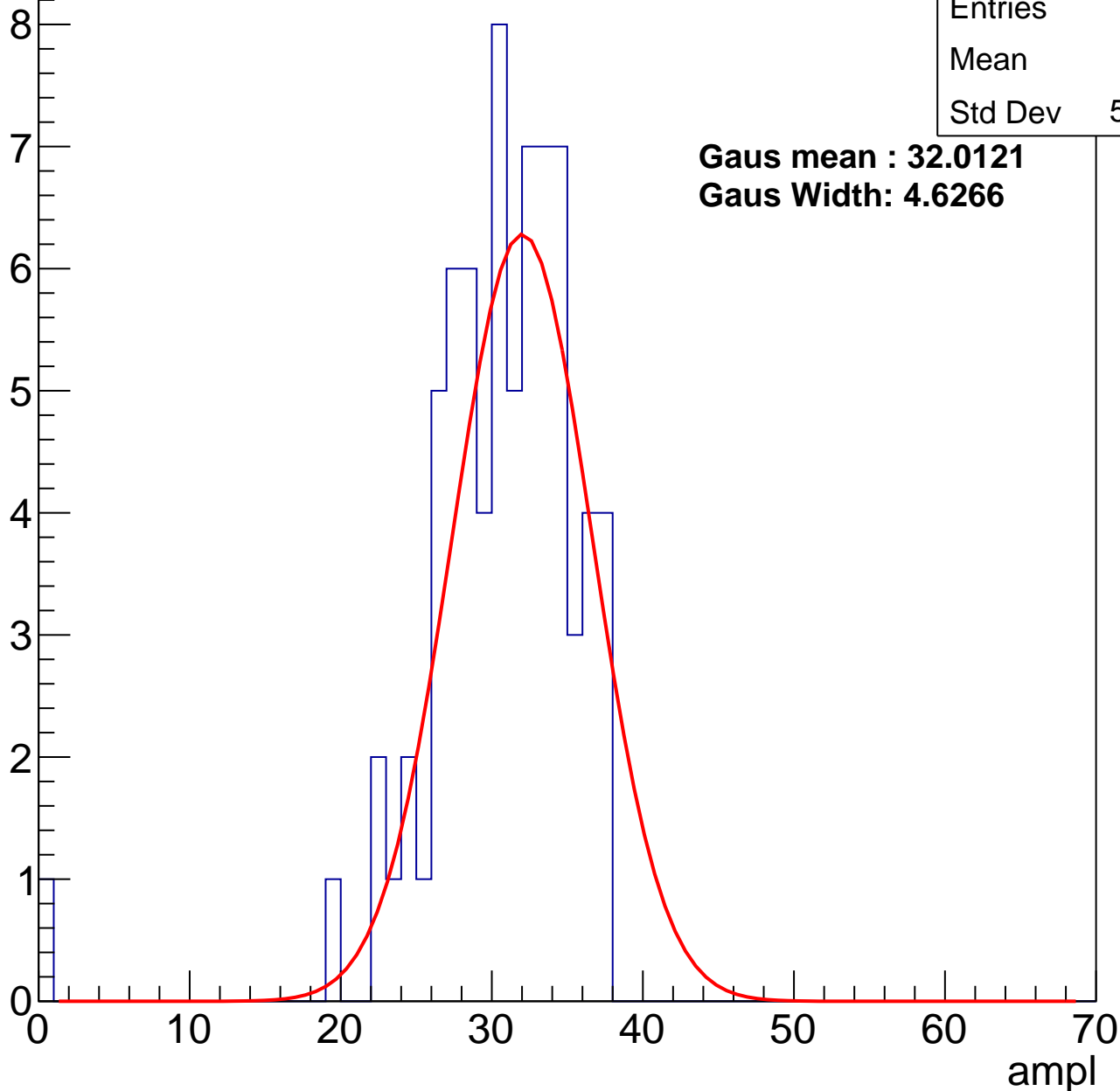
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	30
Std Dev	5.302

**Gaus mean : 32.0121**

**Gaus Width: 4.6266**



# B1L102S, U3-ch123, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	62
Mean	36.6
Std Dev	3.833

**Gaus mean : 36.8305**

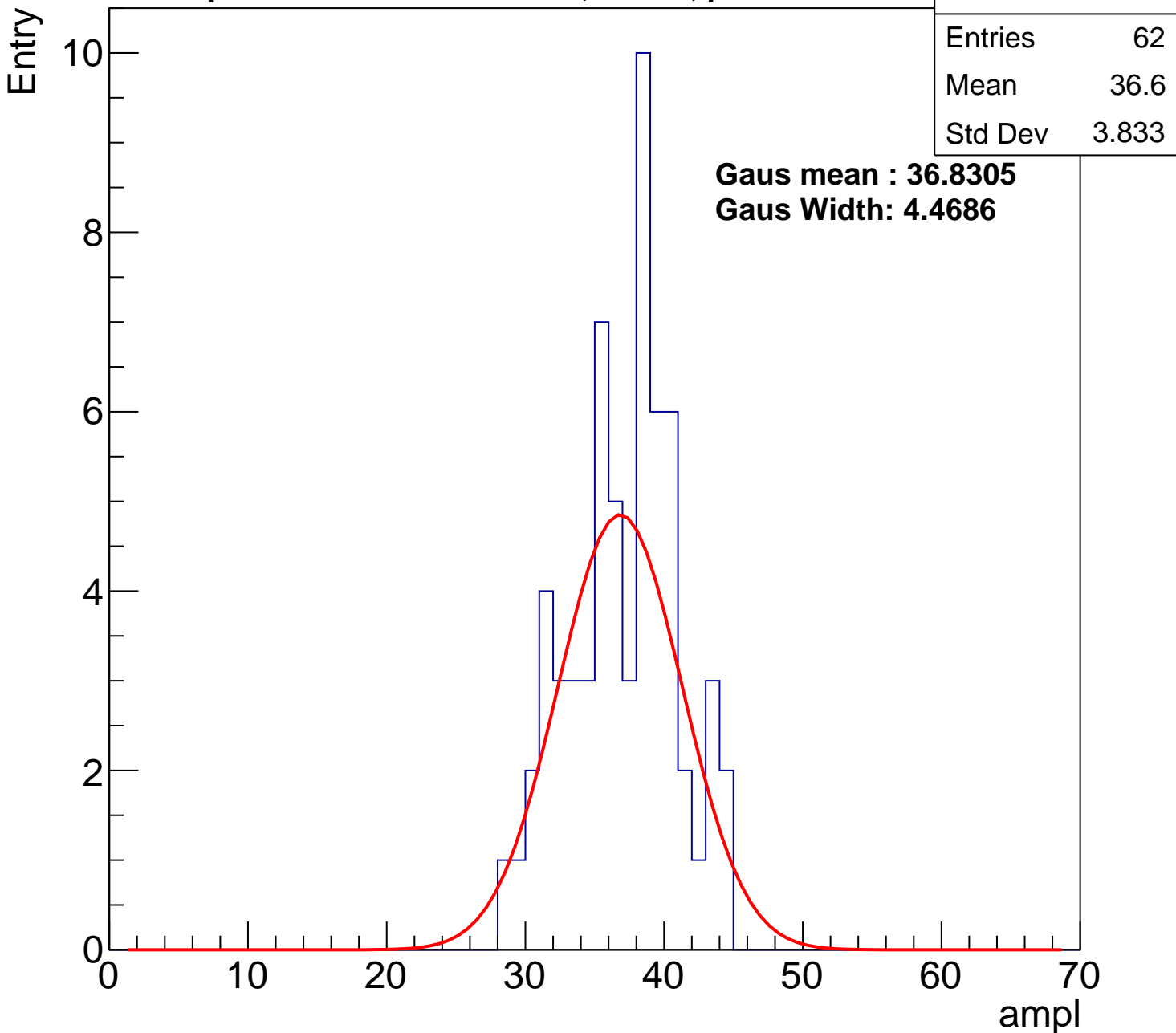
**Gaus Width: 4.4686**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U3-ch123, adc2

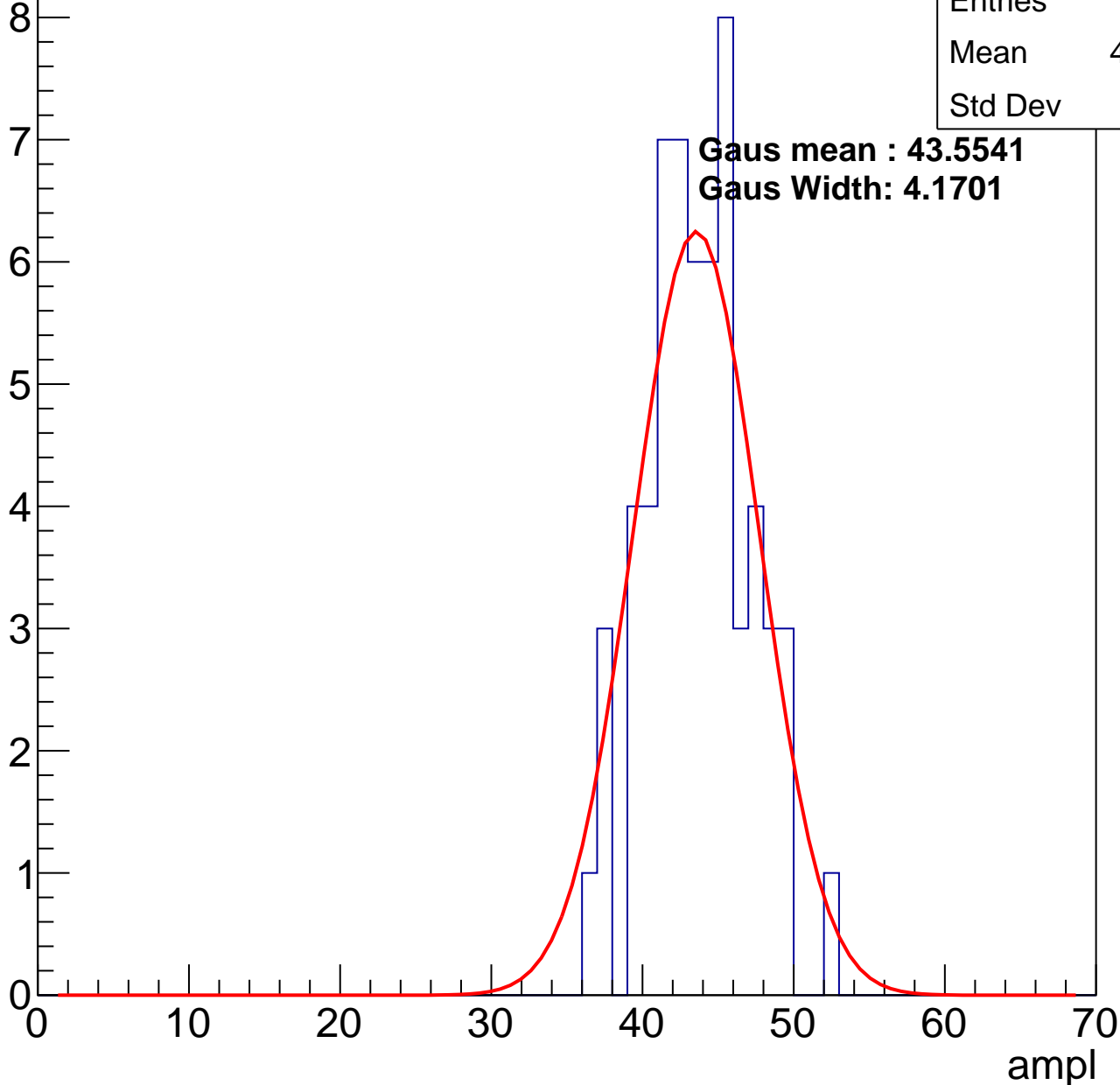
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	43.25
Std Dev	3.37

**Gaus mean : 43.5541**

**Gaus Width: 4.1701**

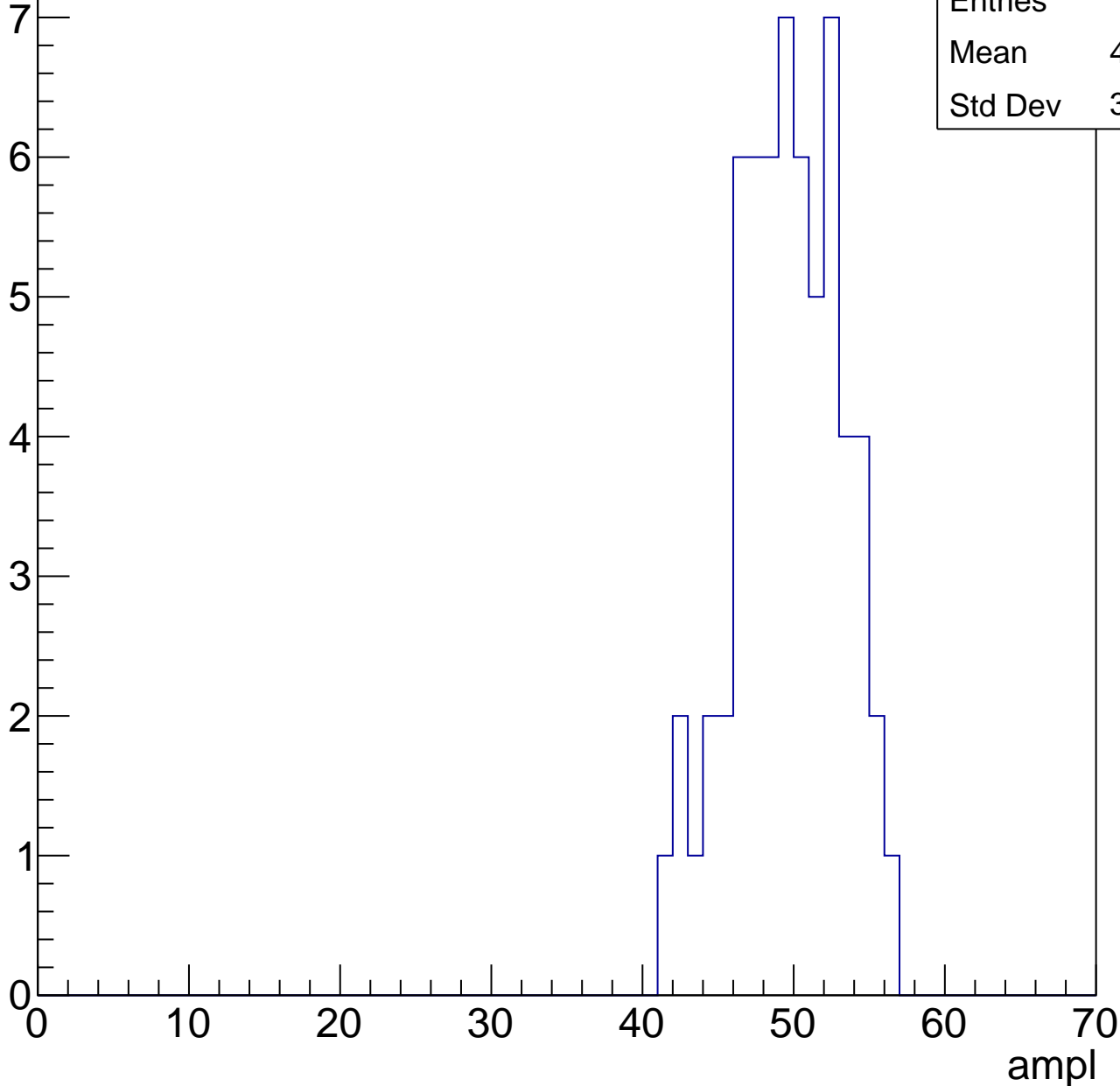


# B1L102S, U3-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

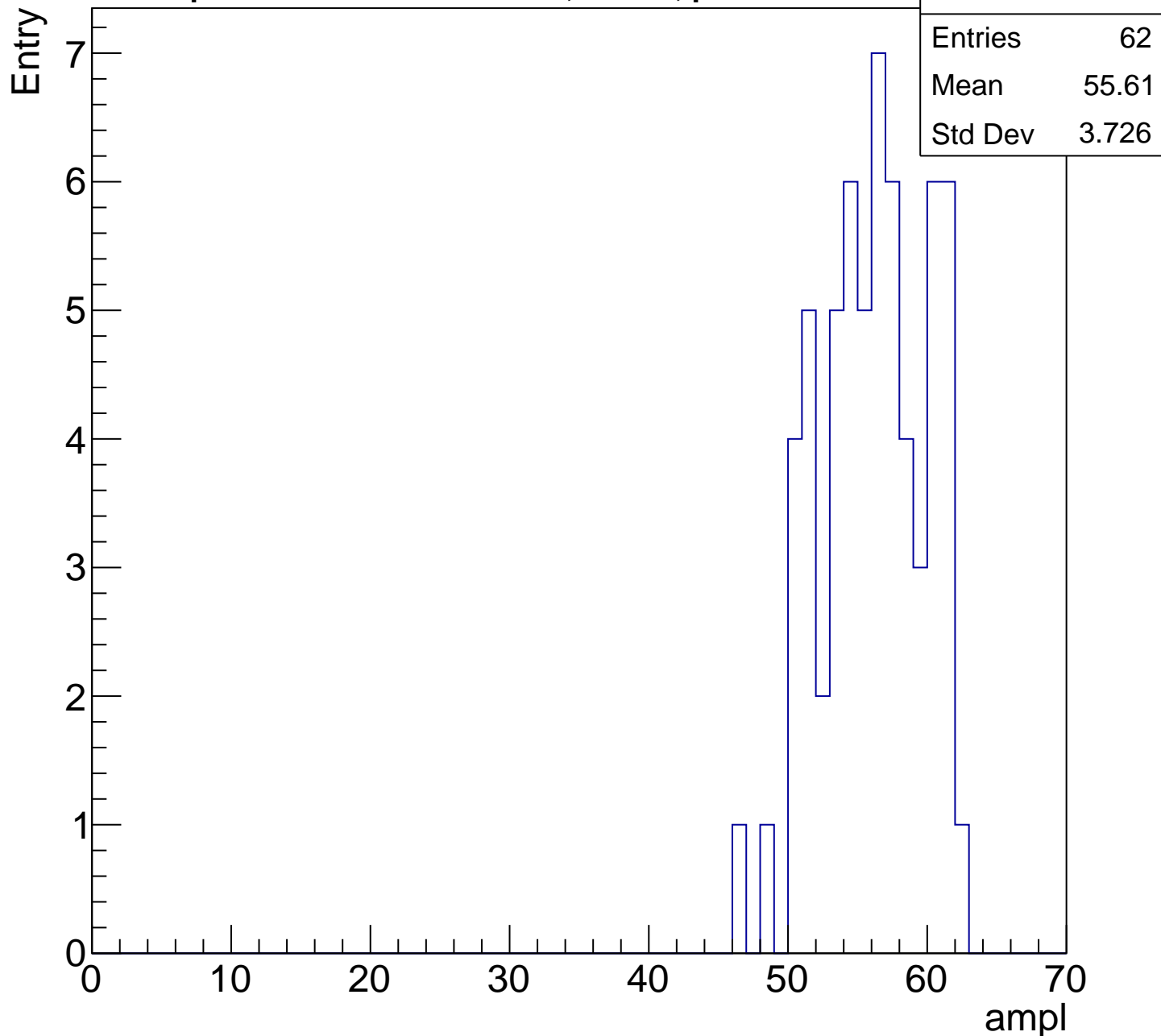
Entry

Entries	62
Mean	49.16
Std Dev	3.446



# B1L102S, U3-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

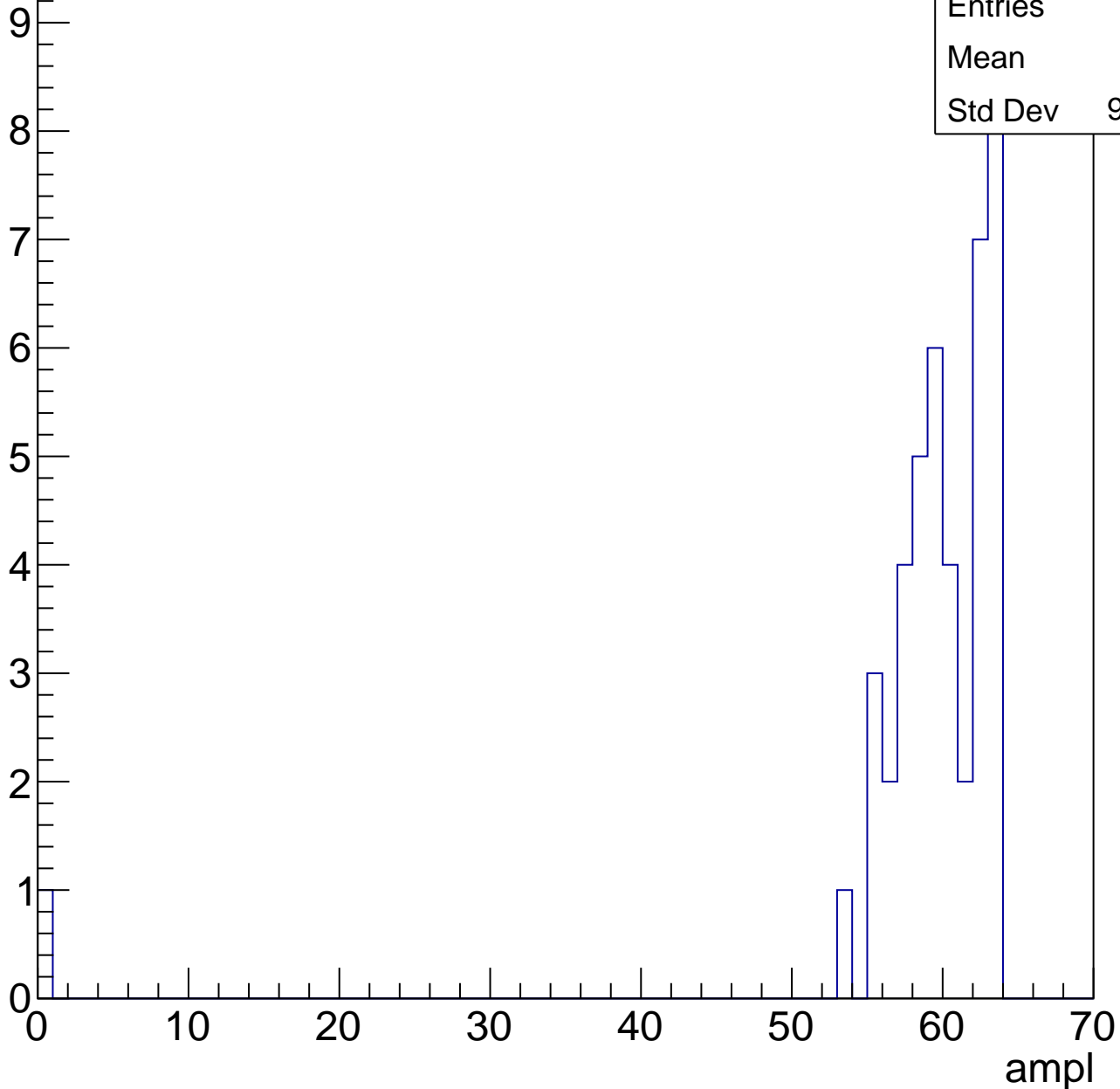


# B1L102S, U3-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

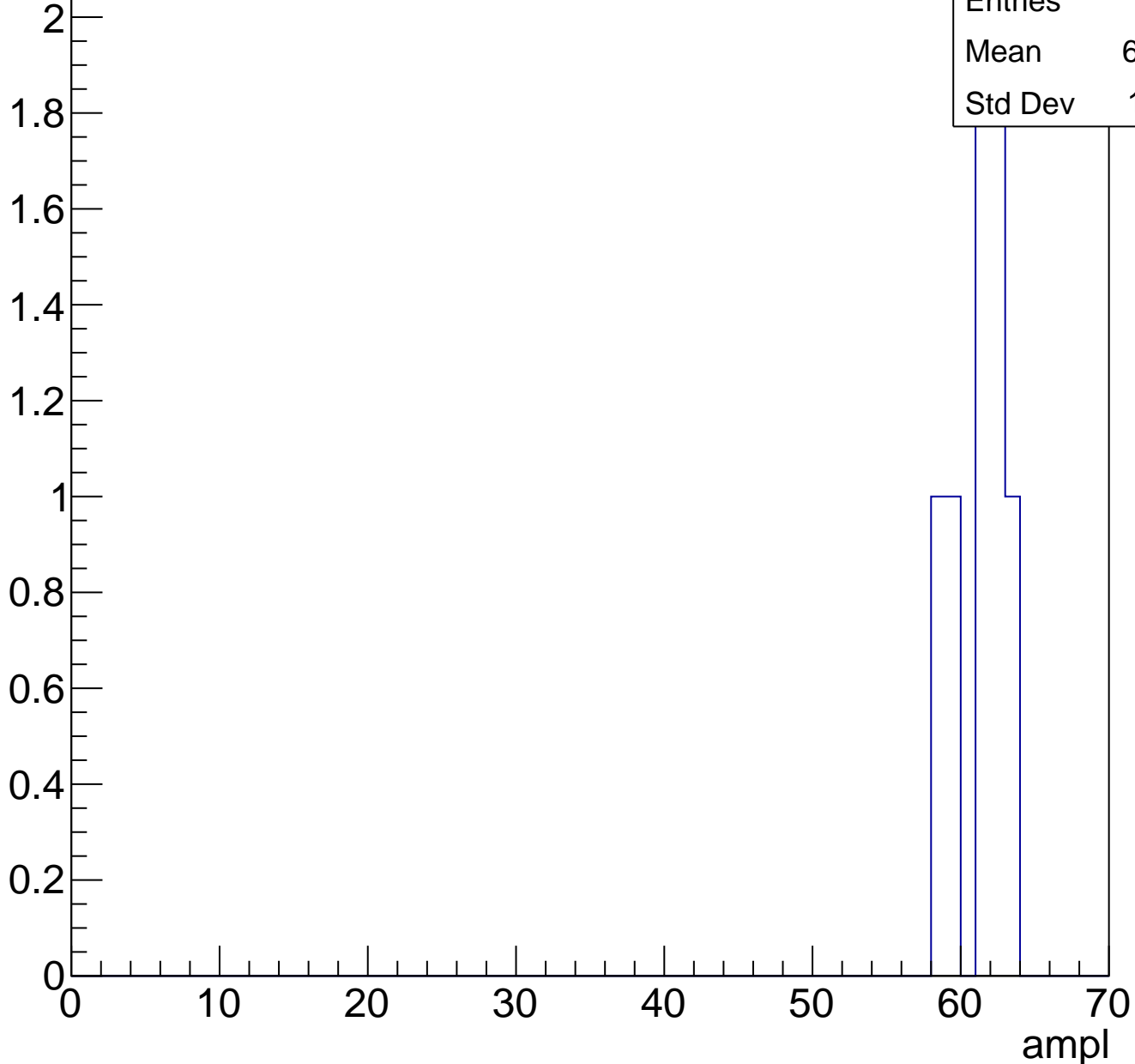
Entries	44
Mean	58.3
Std Dev	9.295



# B1L102S, U3-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch124, adc0

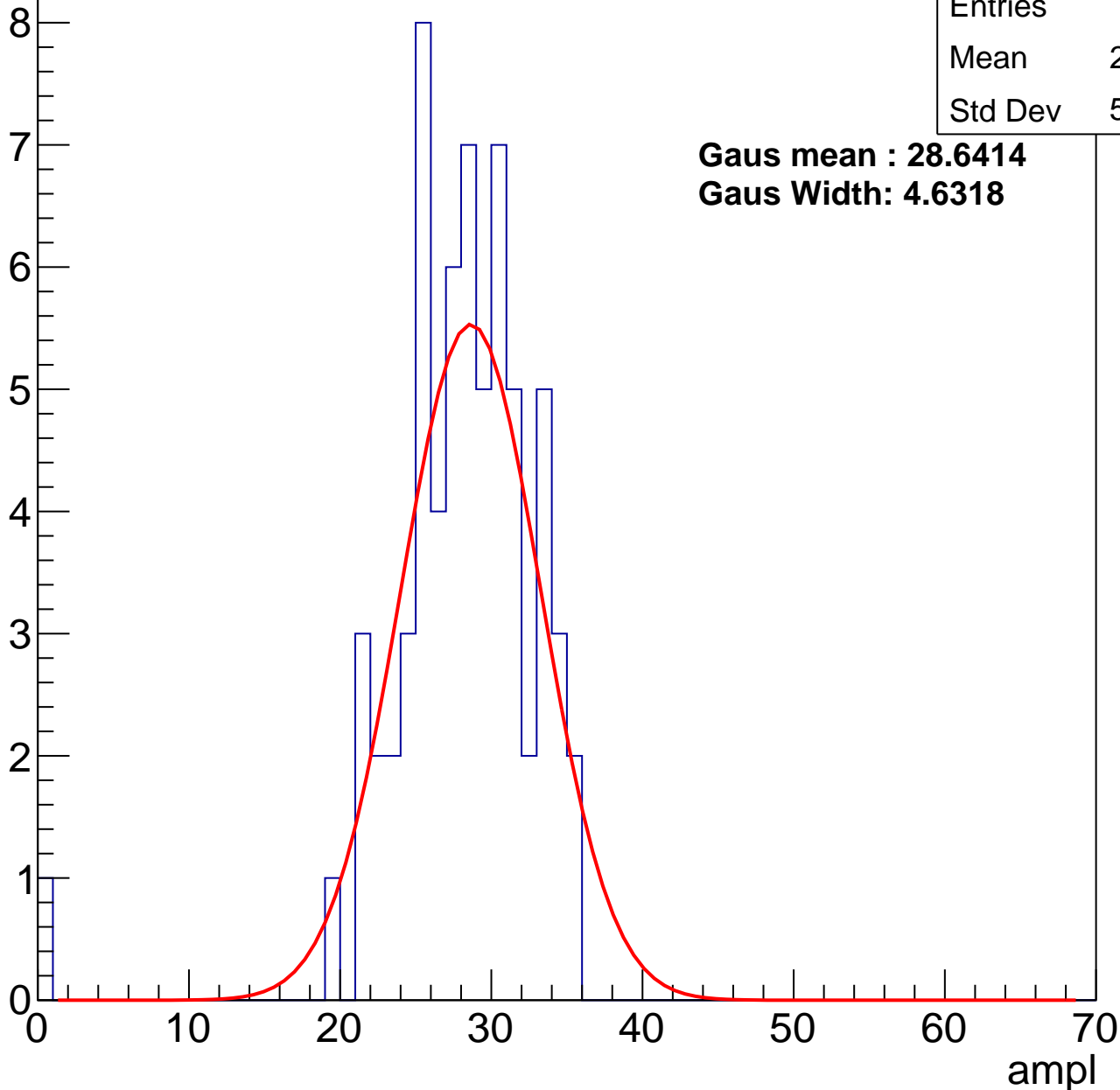
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	27.53
Std Dev	5.079

**Gaus mean : 28.6414**

**Gaus Width: 4.6318**



# B1L102S, U3-ch124, adc1

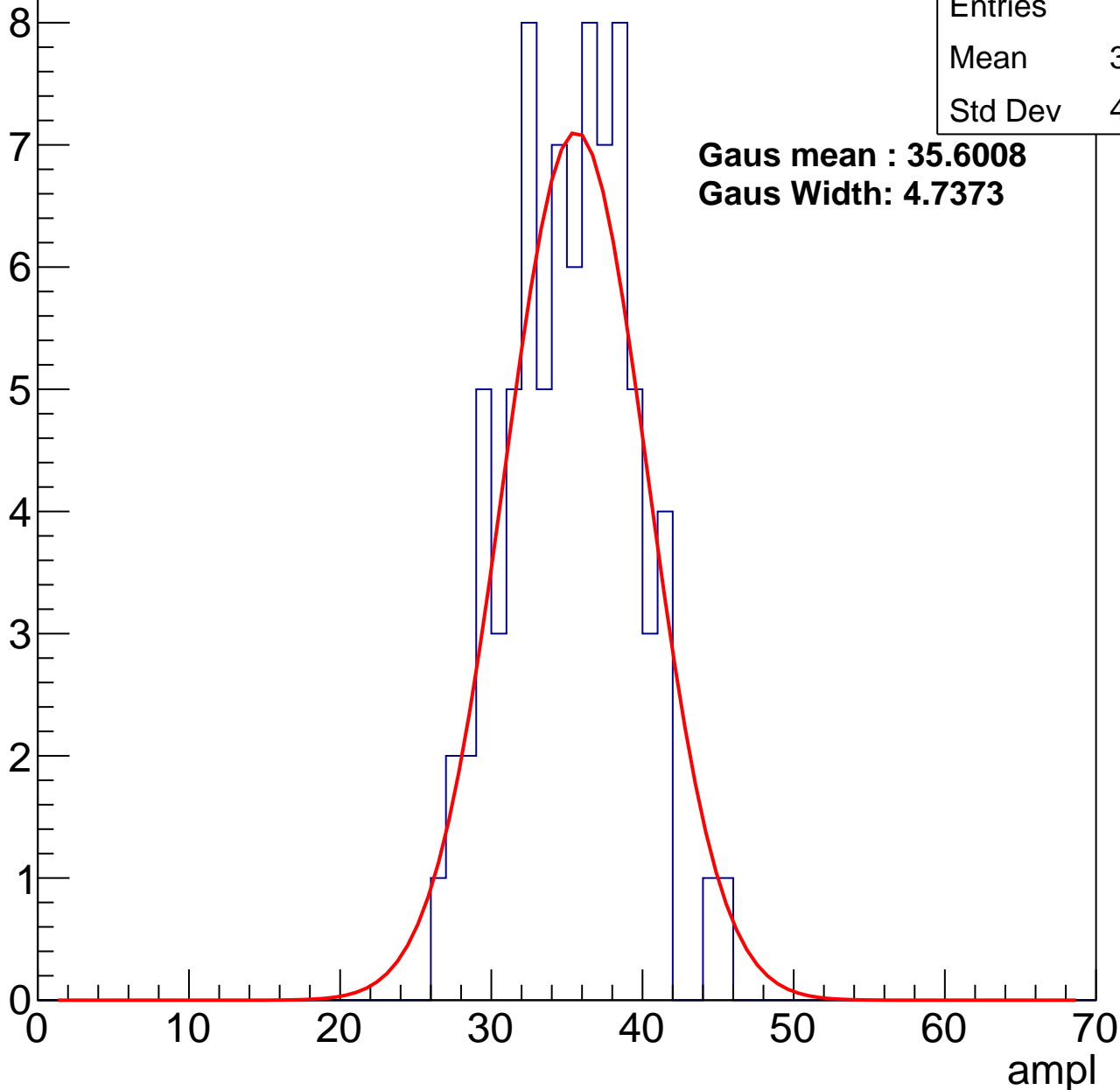
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	81
Mean	34.74
Std Dev	4.042

**Gaus mean : 35.6008**

**Gaus Width: 4.7373**



# B1L102S, U3-ch124, adc2

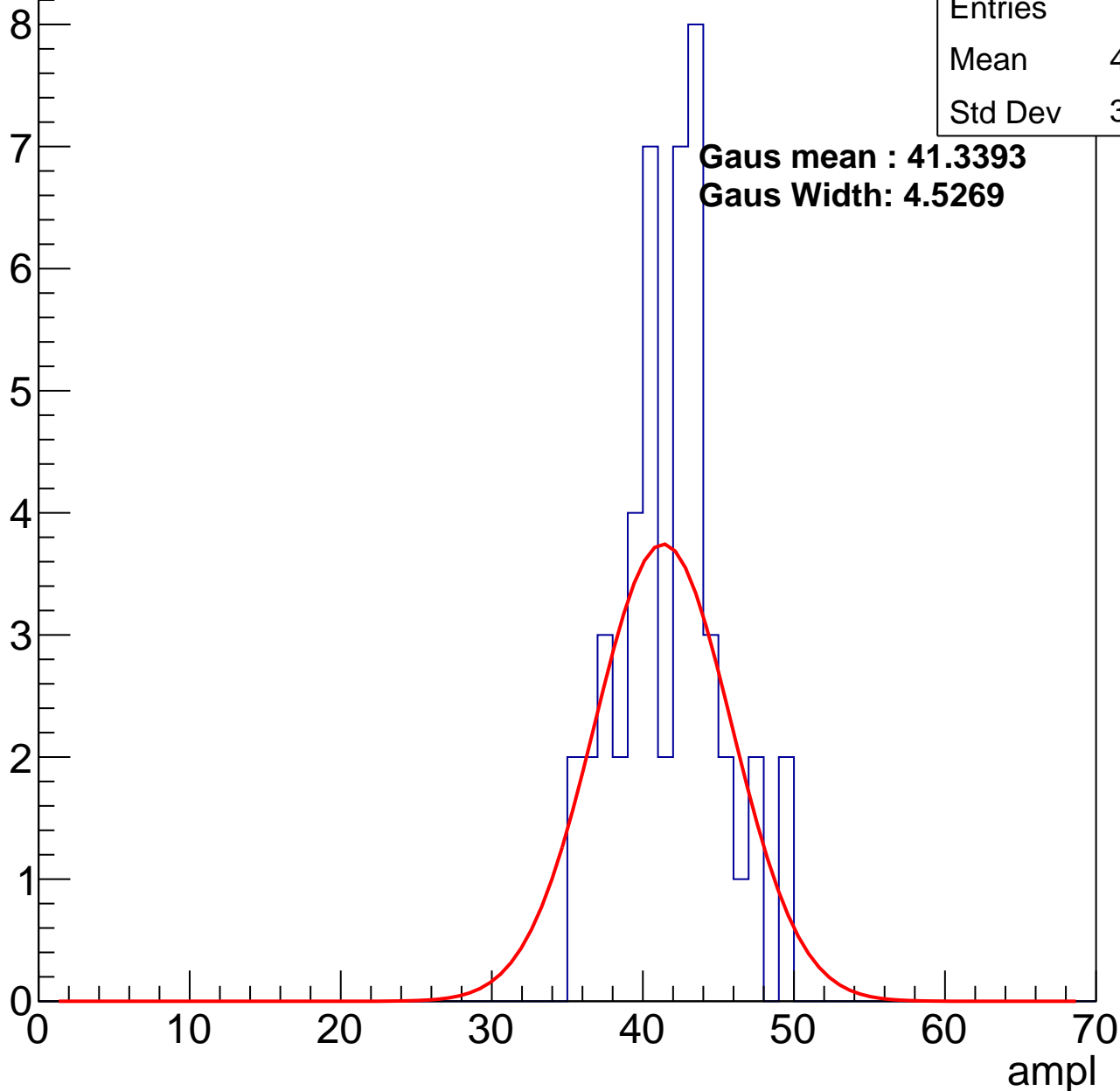
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	41.38
Std Dev	3.349

**Gaus mean : 41.3393**

**Gaus Width: 4.5269**



# B1L102S, U3-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	75
Mean	47.59
Std Dev	3.984

Entry

10

8

6

4

2

0

0

10

20

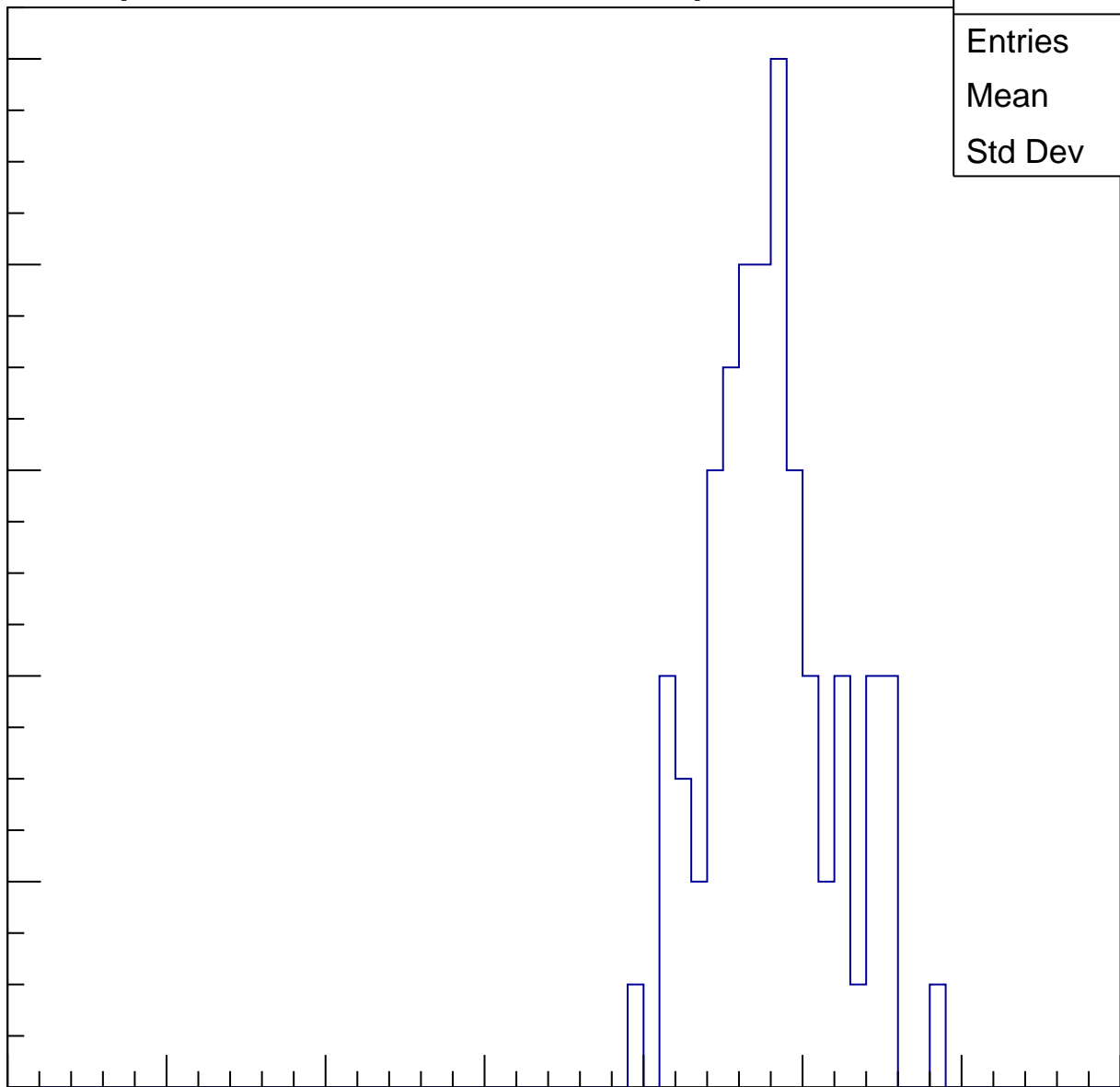
30

40

50

60

ampl

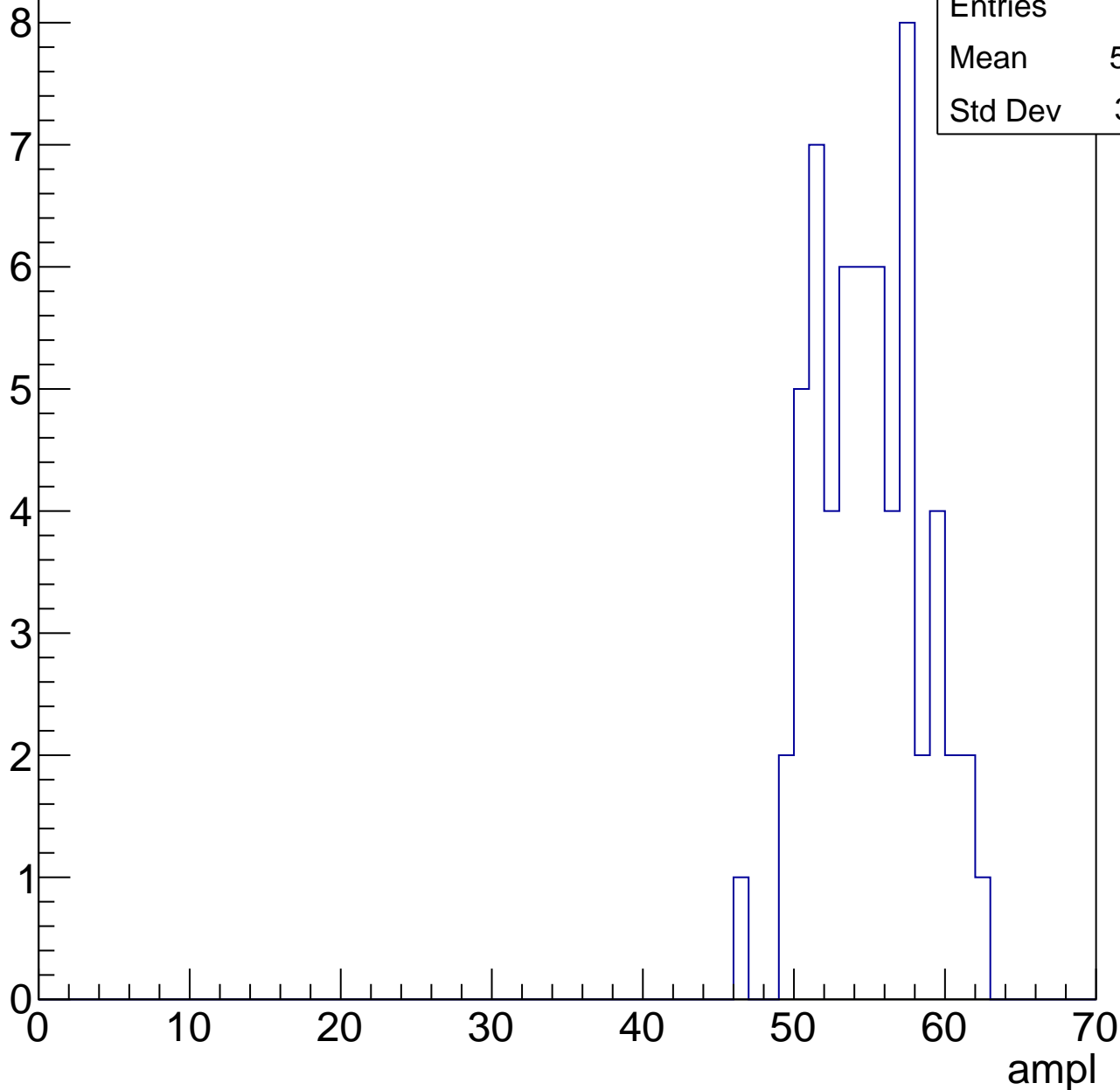


# B1L102S, U3-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	54.45
Std Dev	3.481

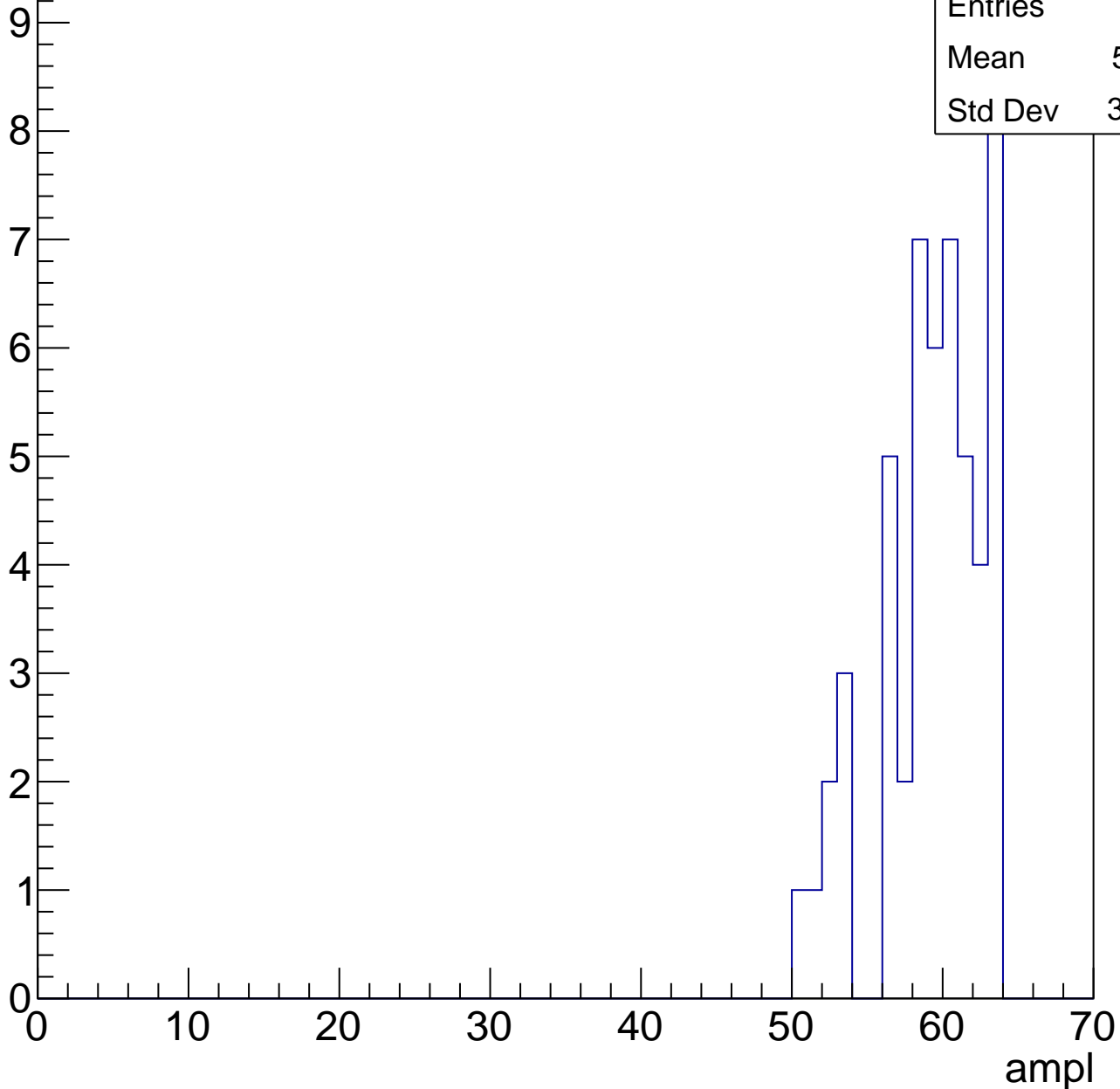


# B1L102S, U3-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	58.81
Std Dev	3.442

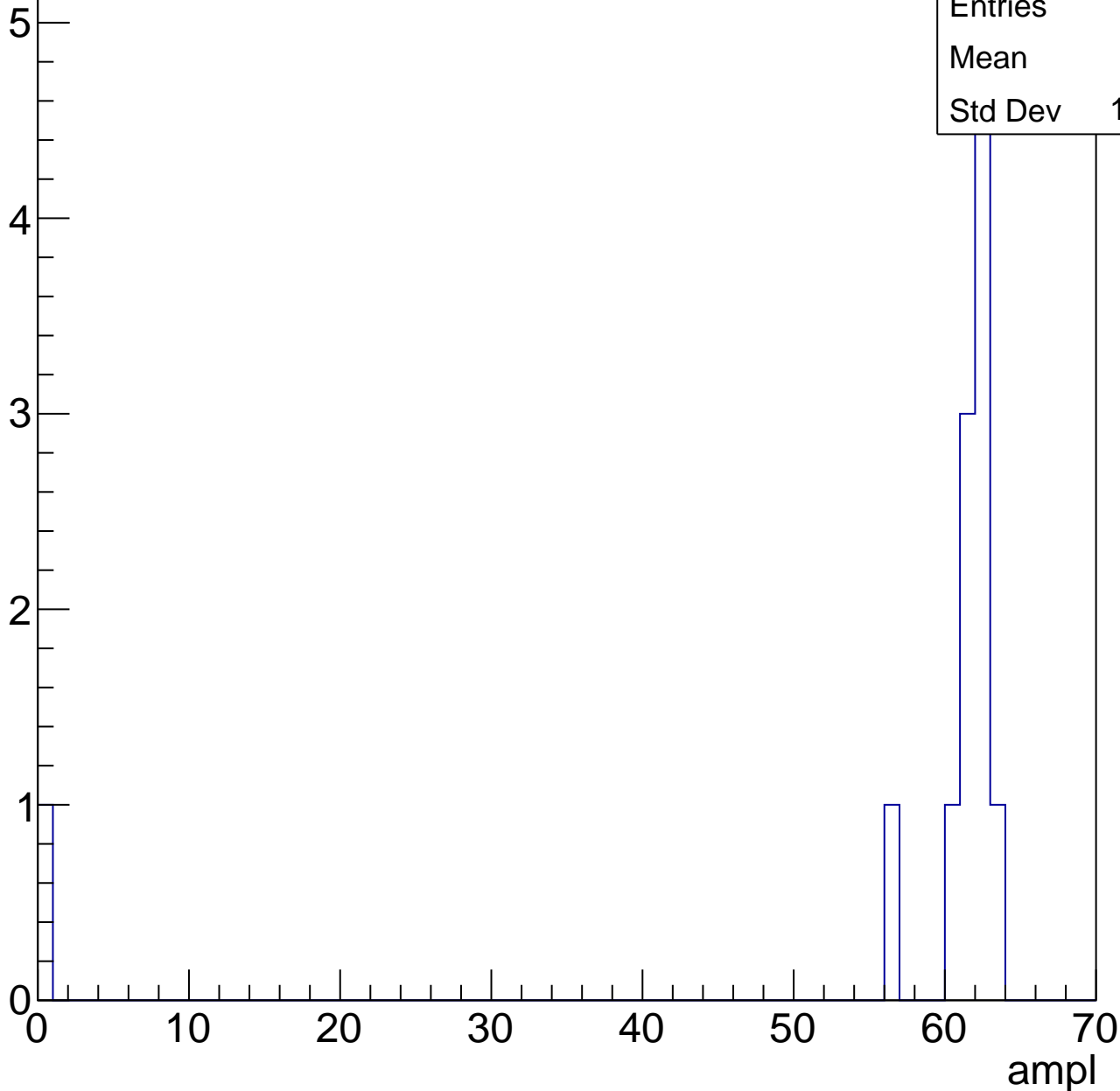


# B1L102S, U3-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	12
Mean	56
Std Dev	16.97





# B1L102S, U3-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch125, adc0

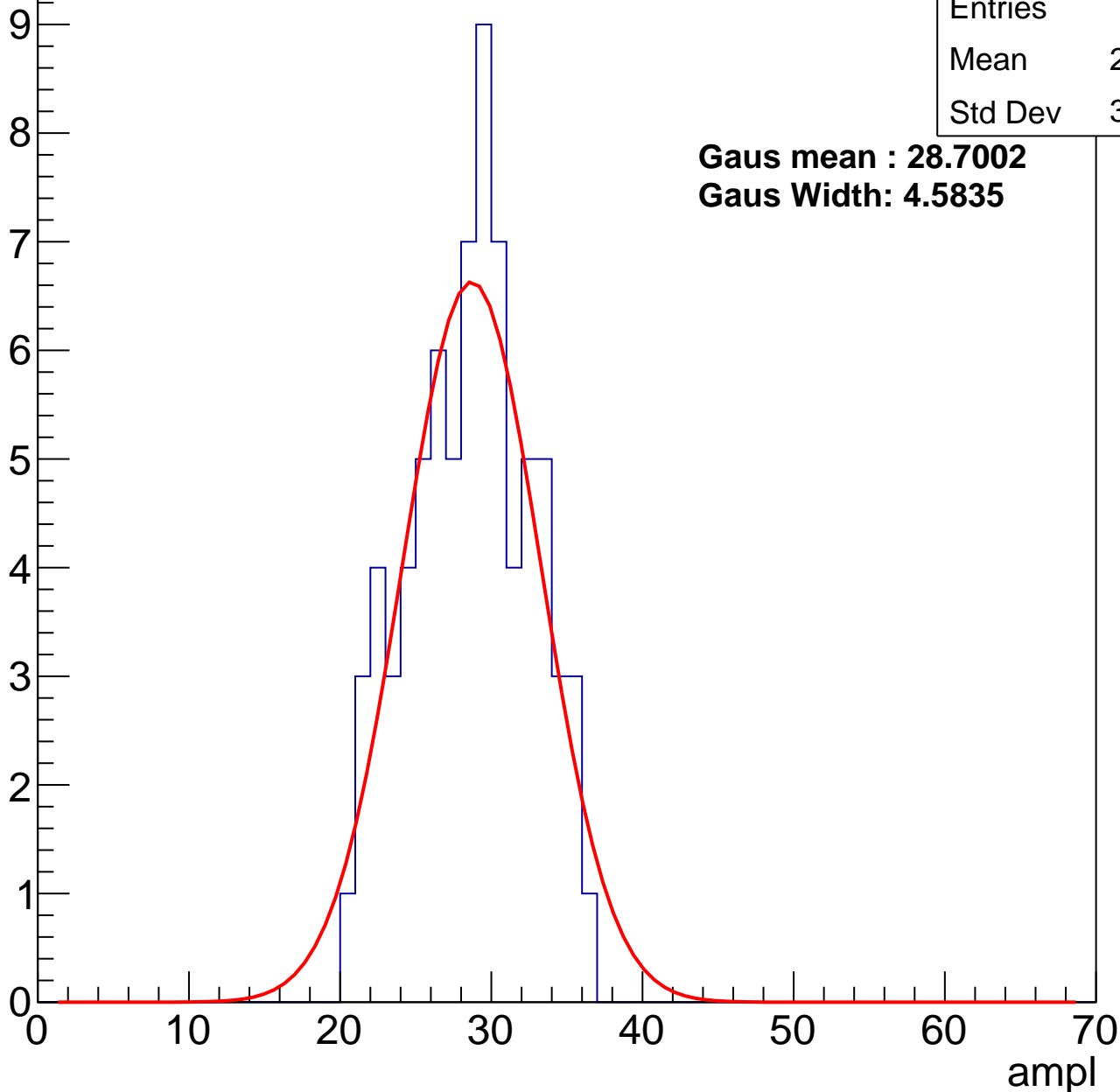
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	28.15
Std Dev	3.939

**Gaus mean : 28.7002**

**Gaus Width: 4.5835**



# B1L102S, U3-ch125, adc1

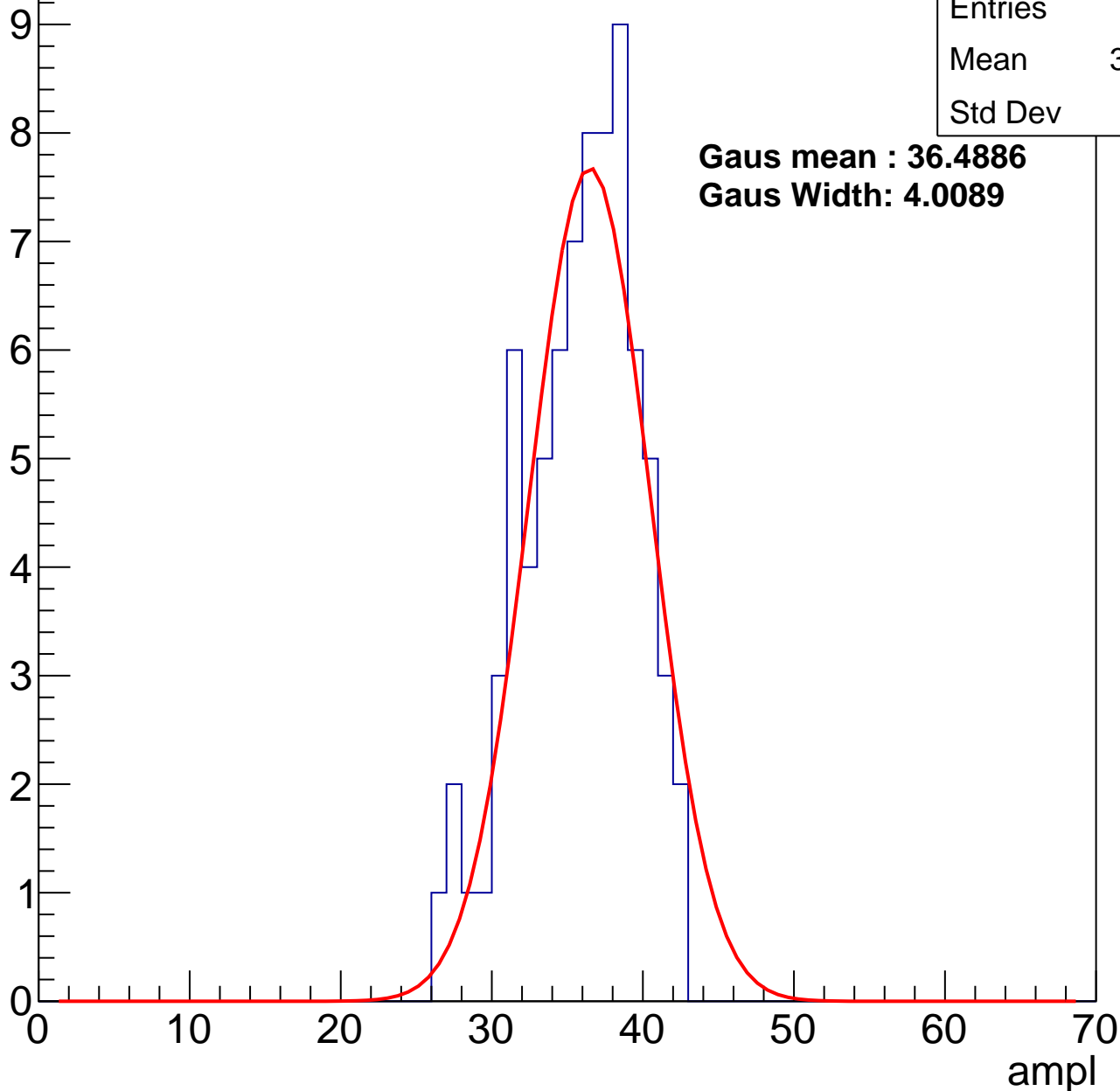
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	35.35
Std Dev	3.72

**Gaus mean : 36.4886**

**Gaus Width: 4.0089**



# B1L102S, U3-ch125, adc2

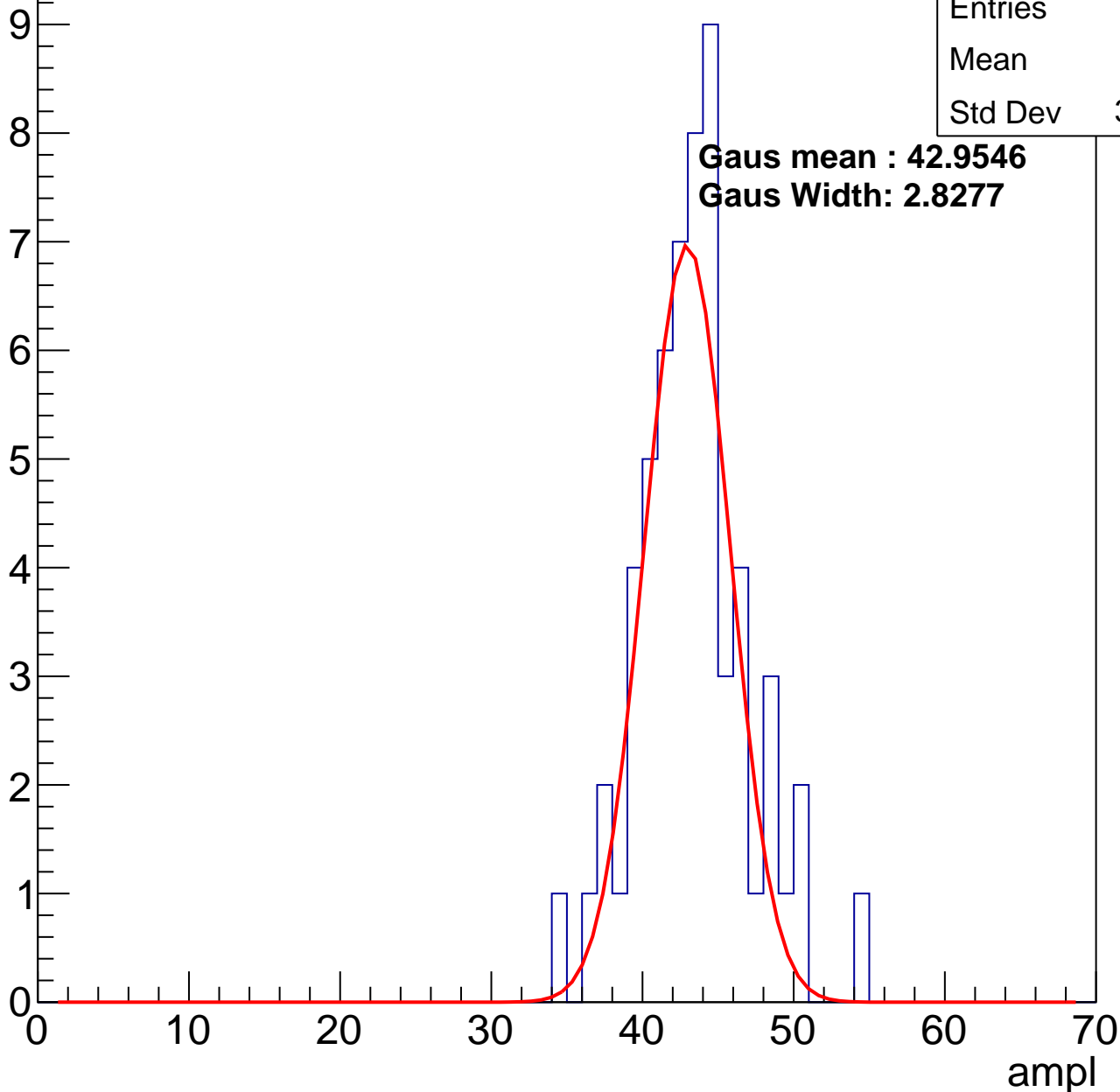
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	42.9
Std Dev	3.611

**Gaus mean : 42.9546**

**Gaus Width: 2.8277**

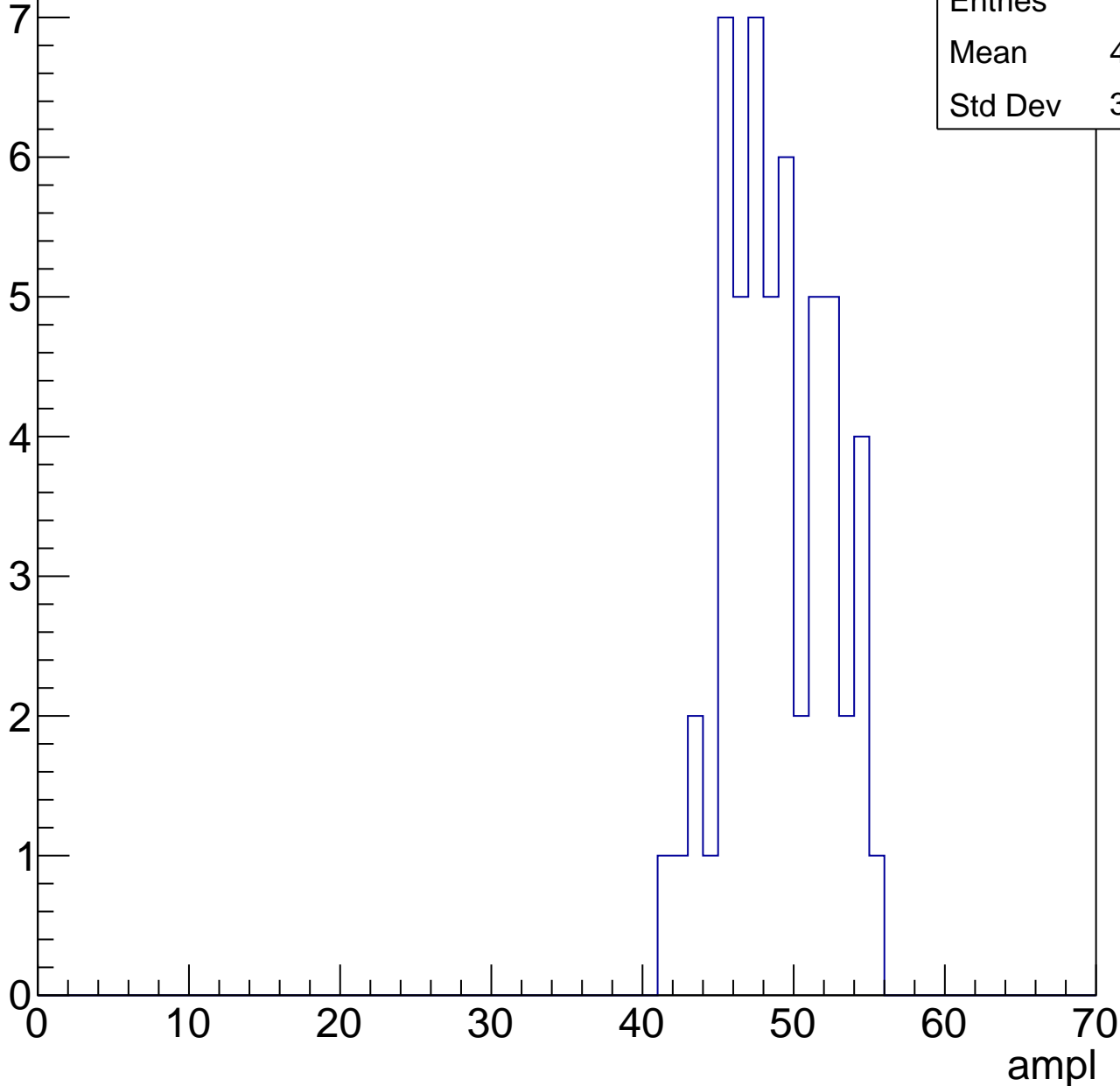


# B1L102S, U3-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	48.39
Std Dev	3.374

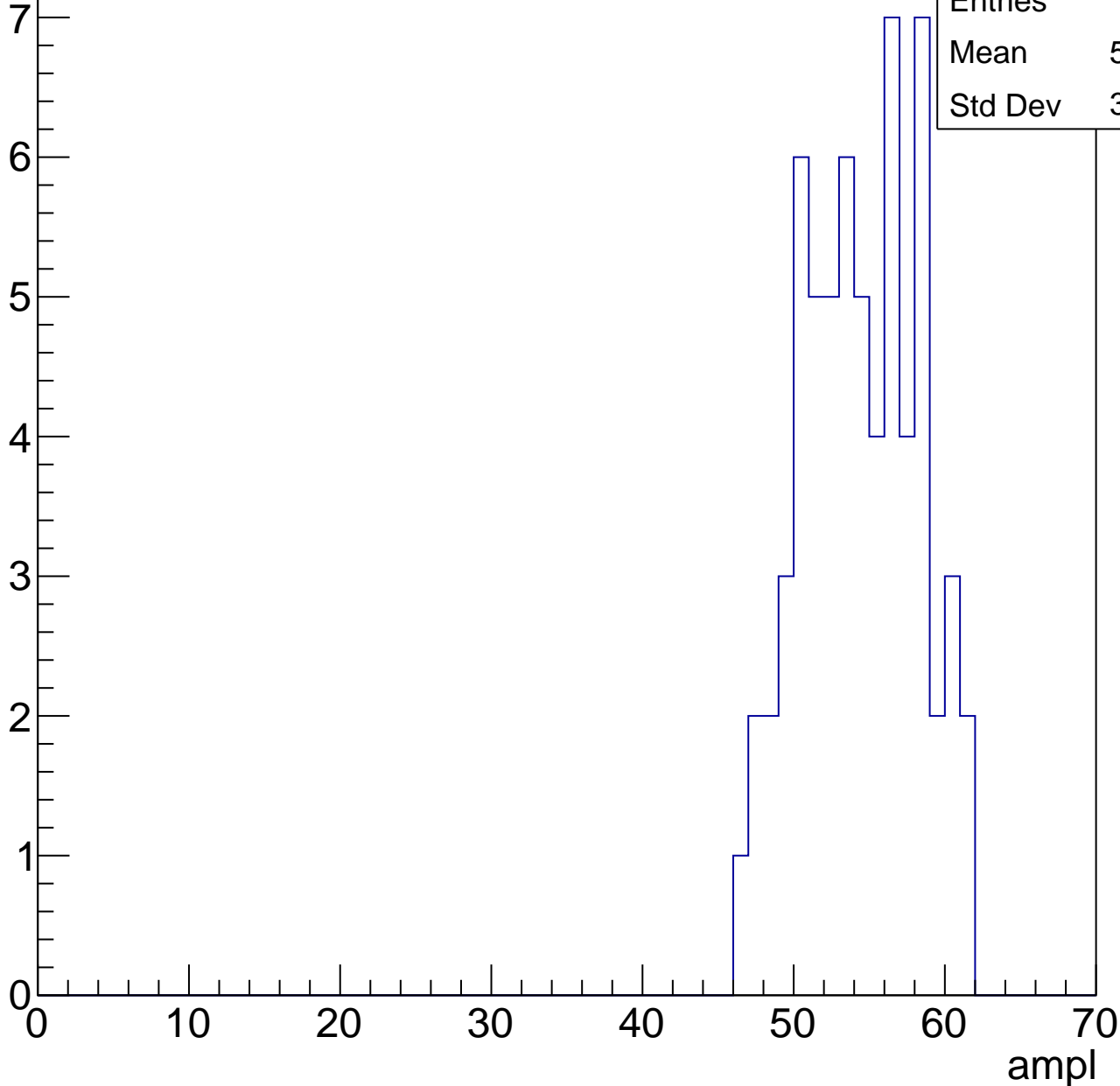


# B1L102S, U3-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	53.94
Std Dev	3.774



# B1L102S, U3-ch125, adc5

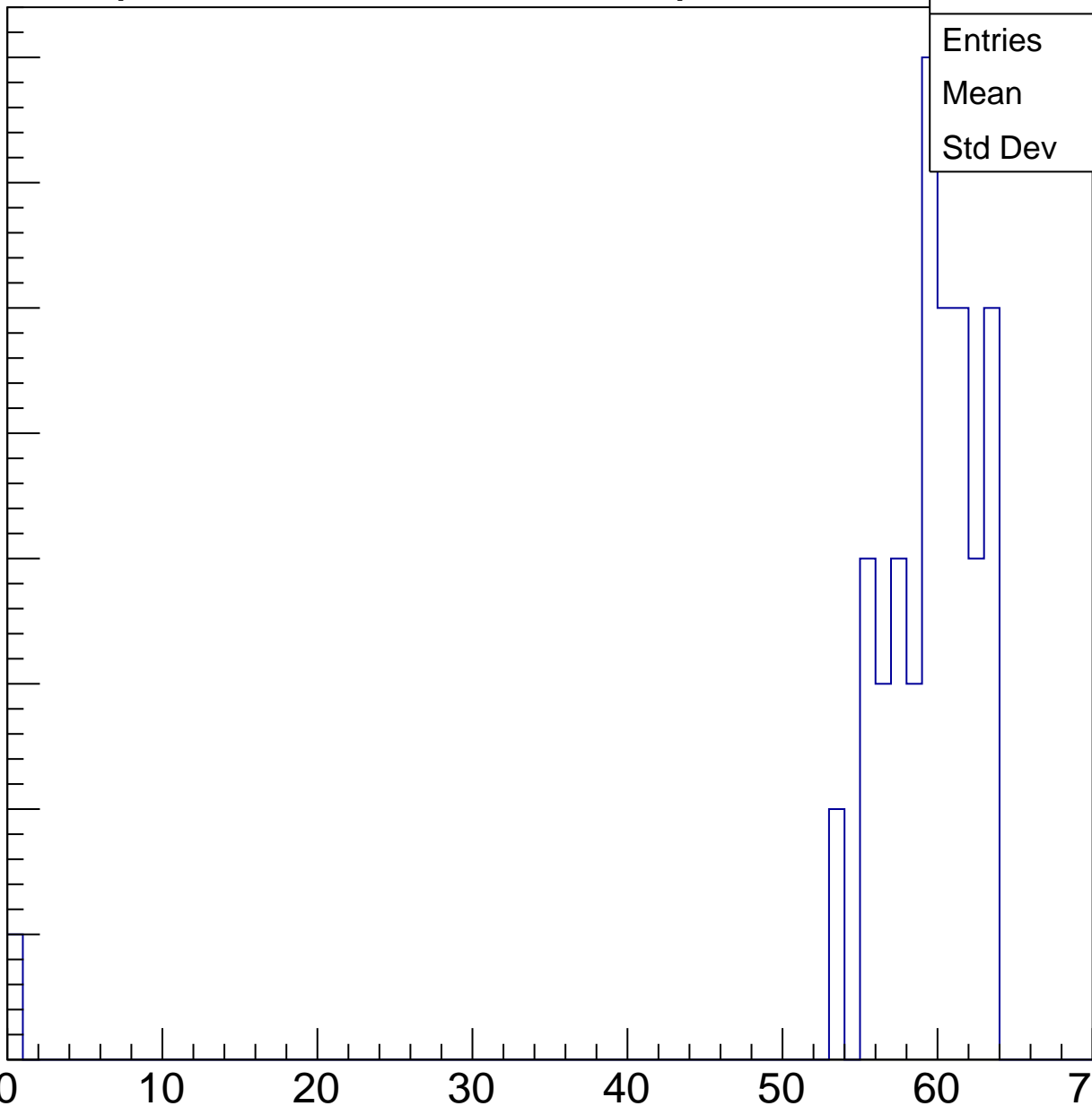
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	47
Mean	57.87
Std Dev	8.95

ampl

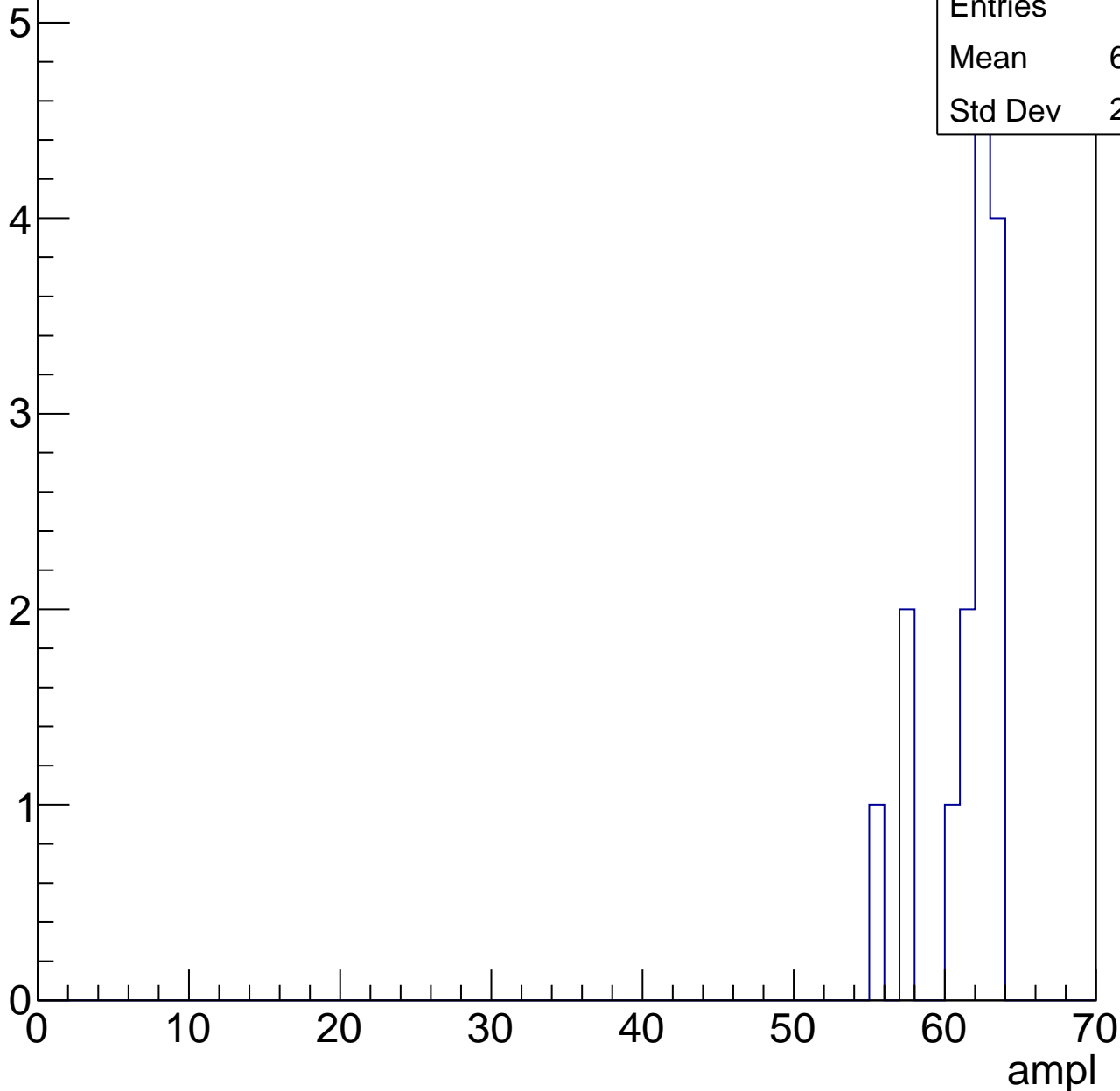


# B1L102S, U3-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	15
Mean	60.87
Std Dev	2.446





# B1L102S, U3-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	62
Std Dev	0

# B1L102S, U3-ch126, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	92
Mean	27.37
Std Dev	4.532

**Gaus mean : 27.6570**

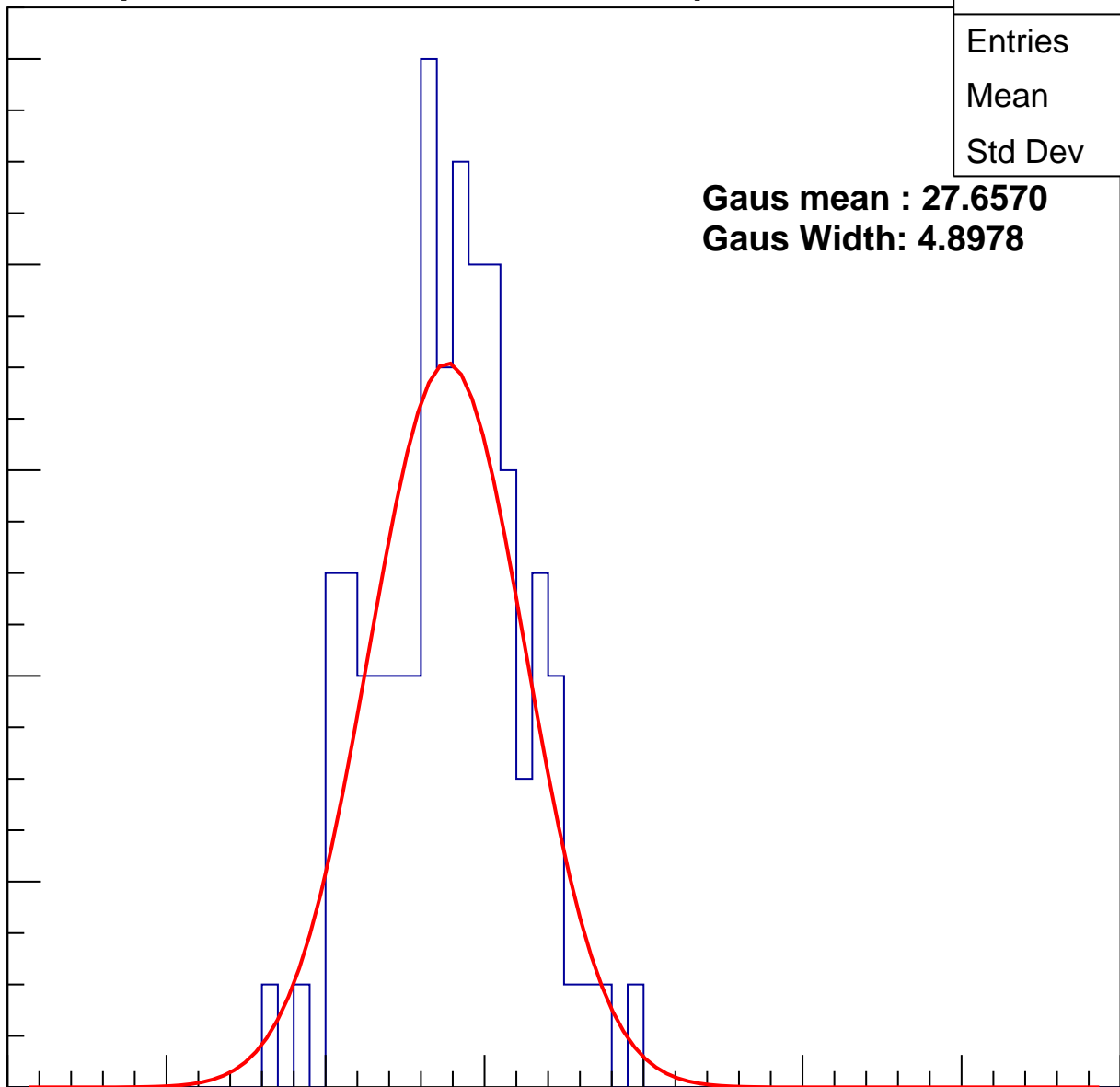
**Gaus Width: 4.8978**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



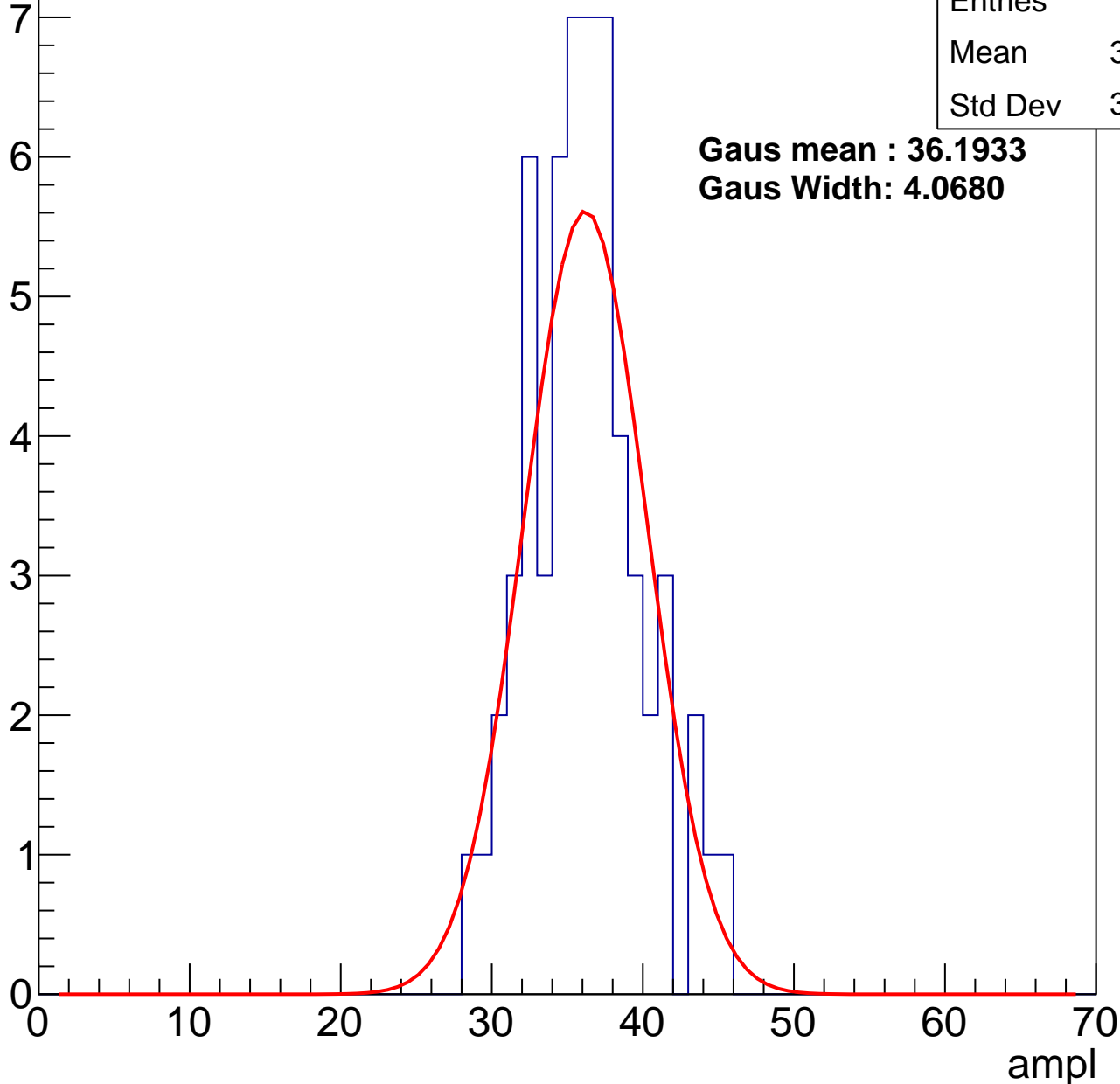
# B1L102S, U3-ch126, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	35.73
Std Dev	3.704

**Gaus mean : 36.1933**  
**Gaus Width: 4.0680**



# B1L102S, U3-ch126, adc2

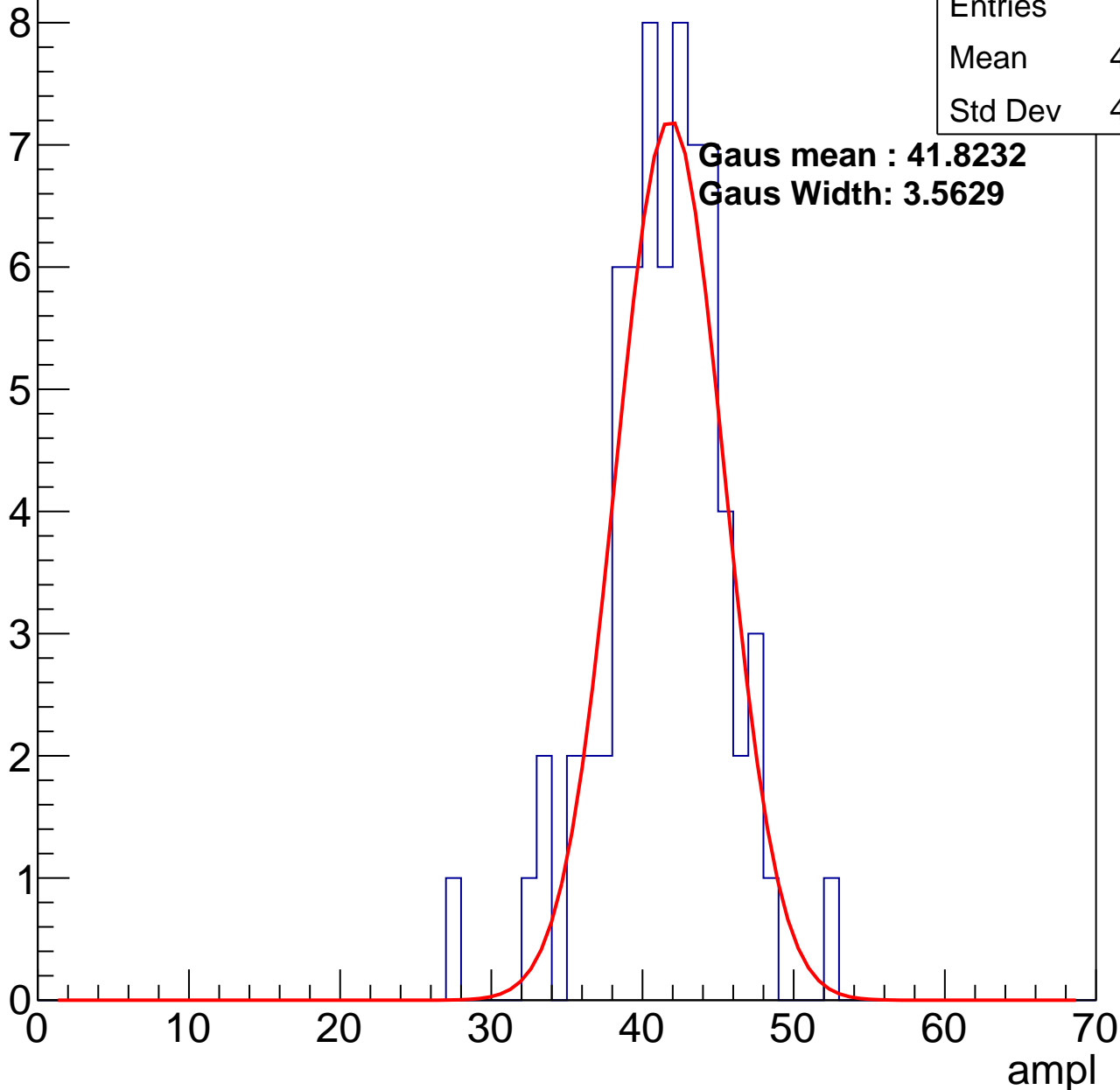
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	40.97
Std Dev	4.057

**Gaus mean : 41.8232**

**Gaus Width: 3.5629**

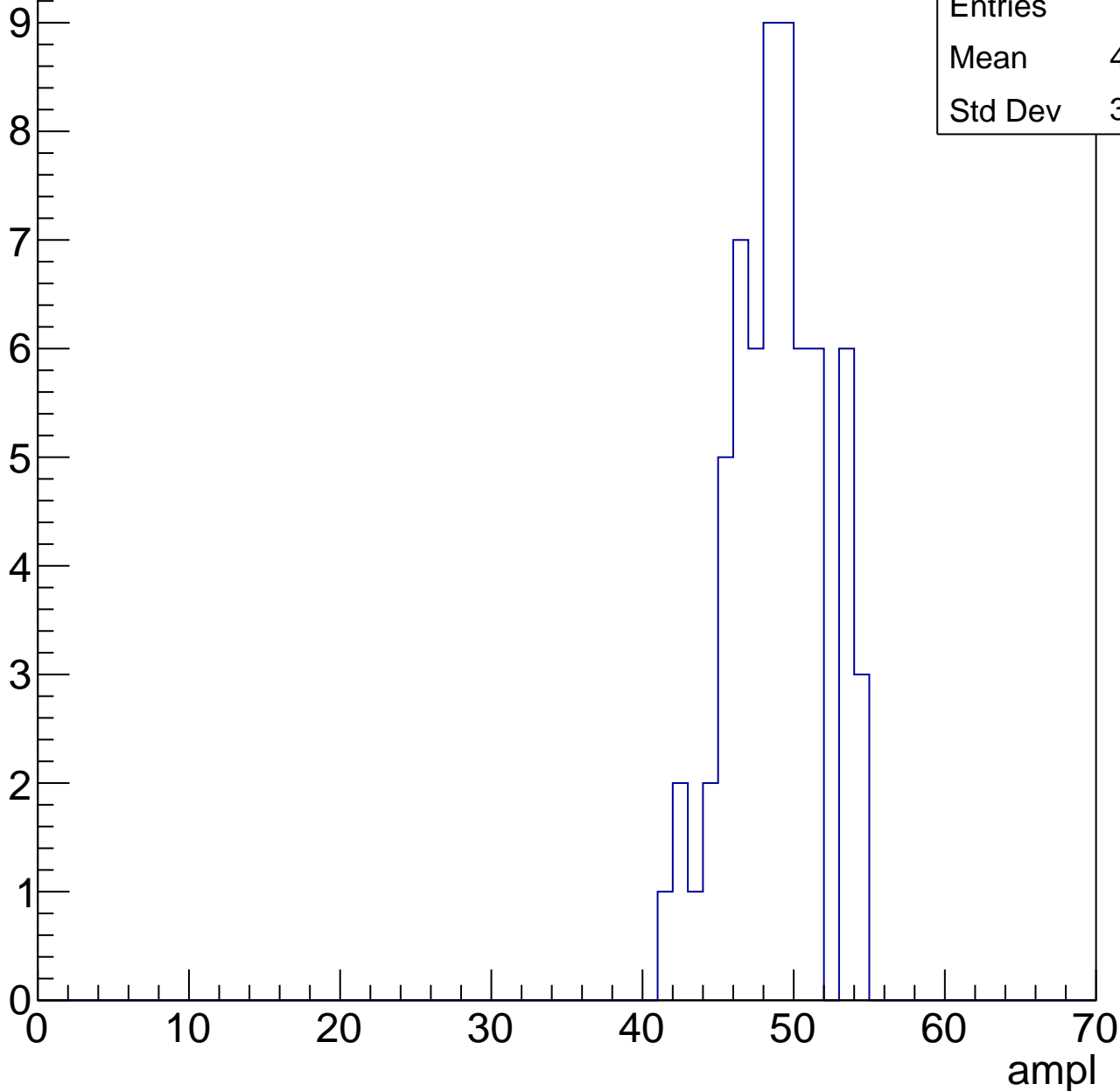


# B1L102S, U3-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	48.32
Std Dev	3.075

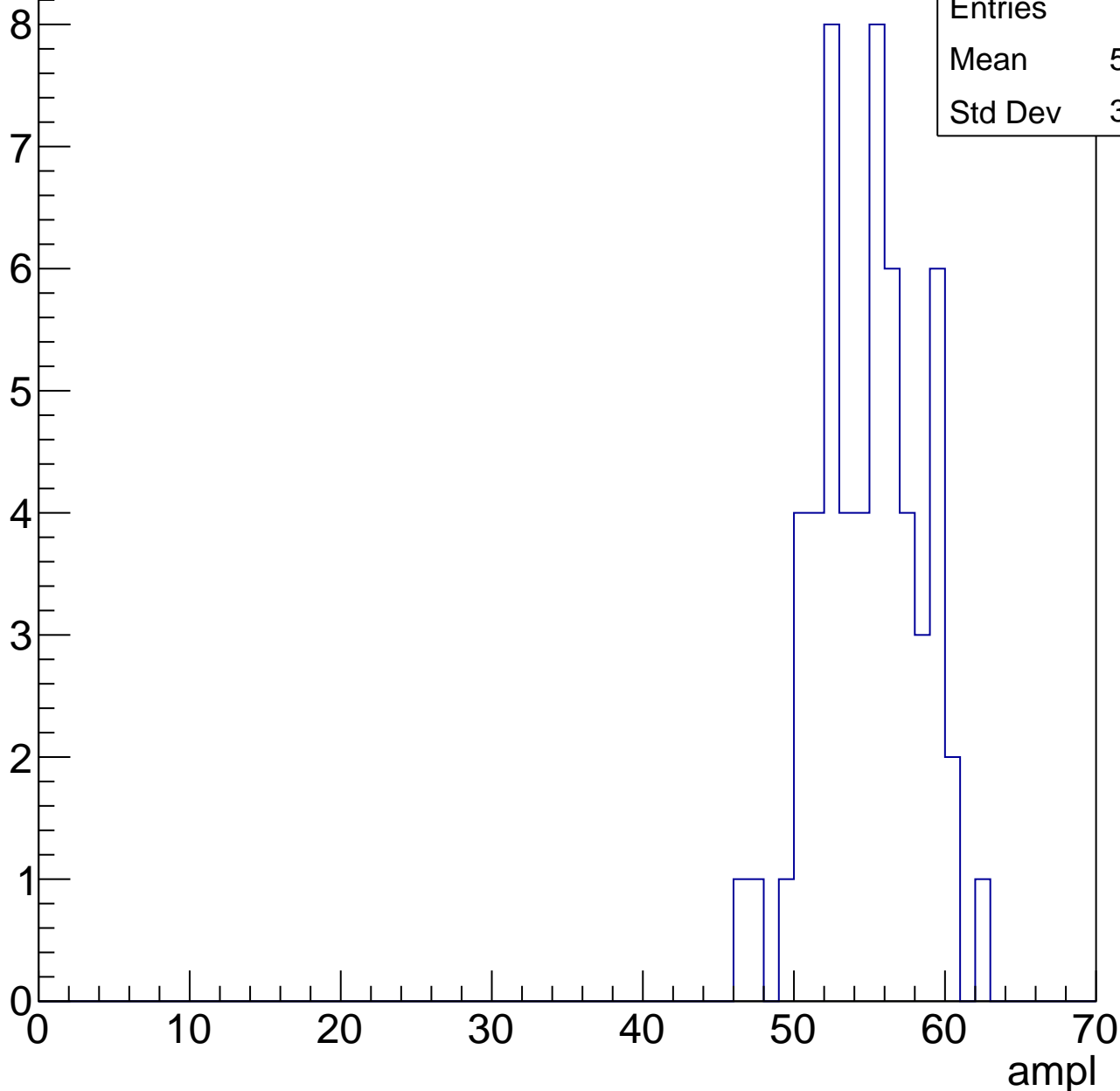


# B1L102S, U3-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

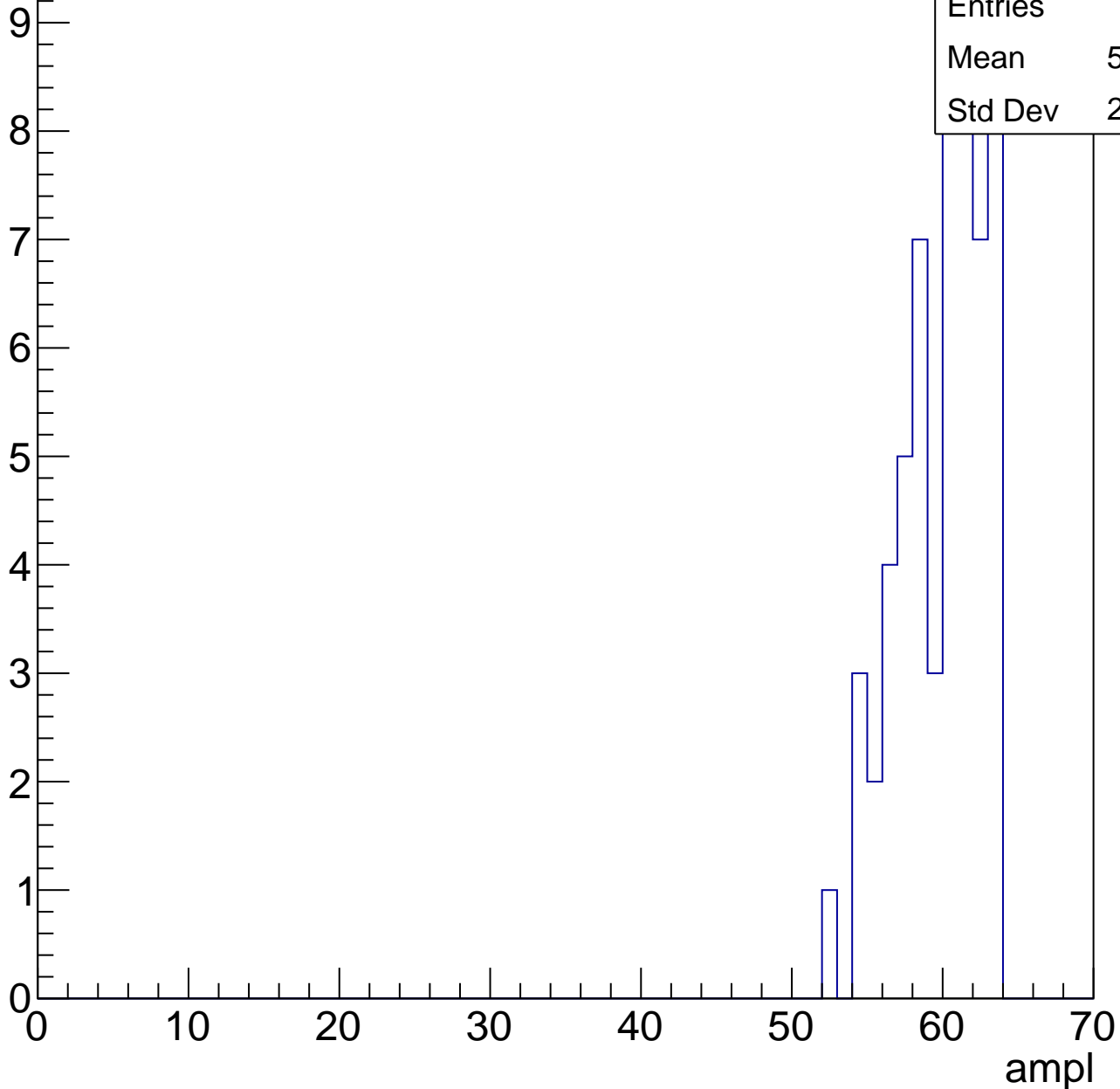
Entries	57
Mean	54.46
Std Dev	3.413



# B1L102S, U3-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

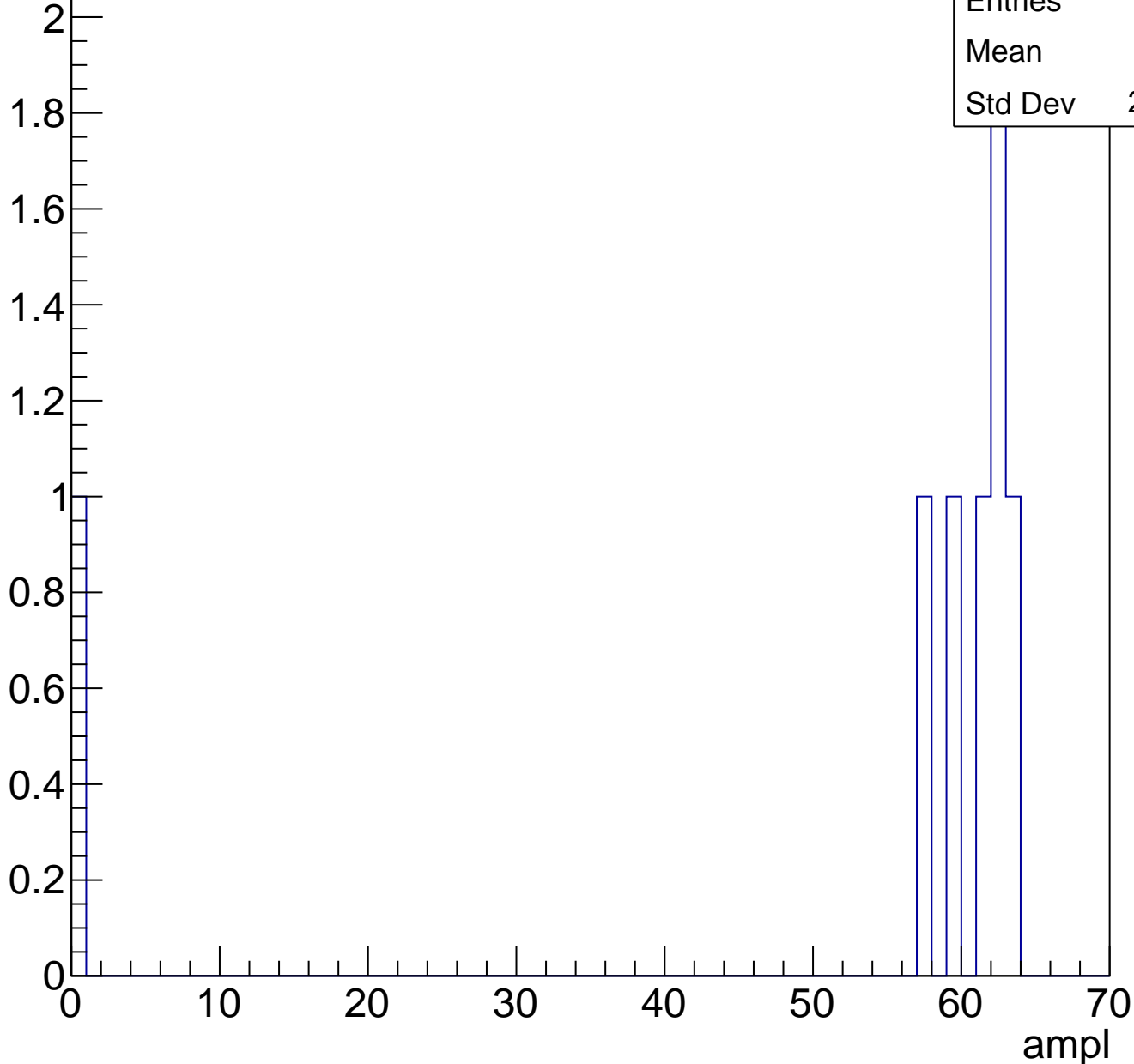
Entry



# B1L102S, U3-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

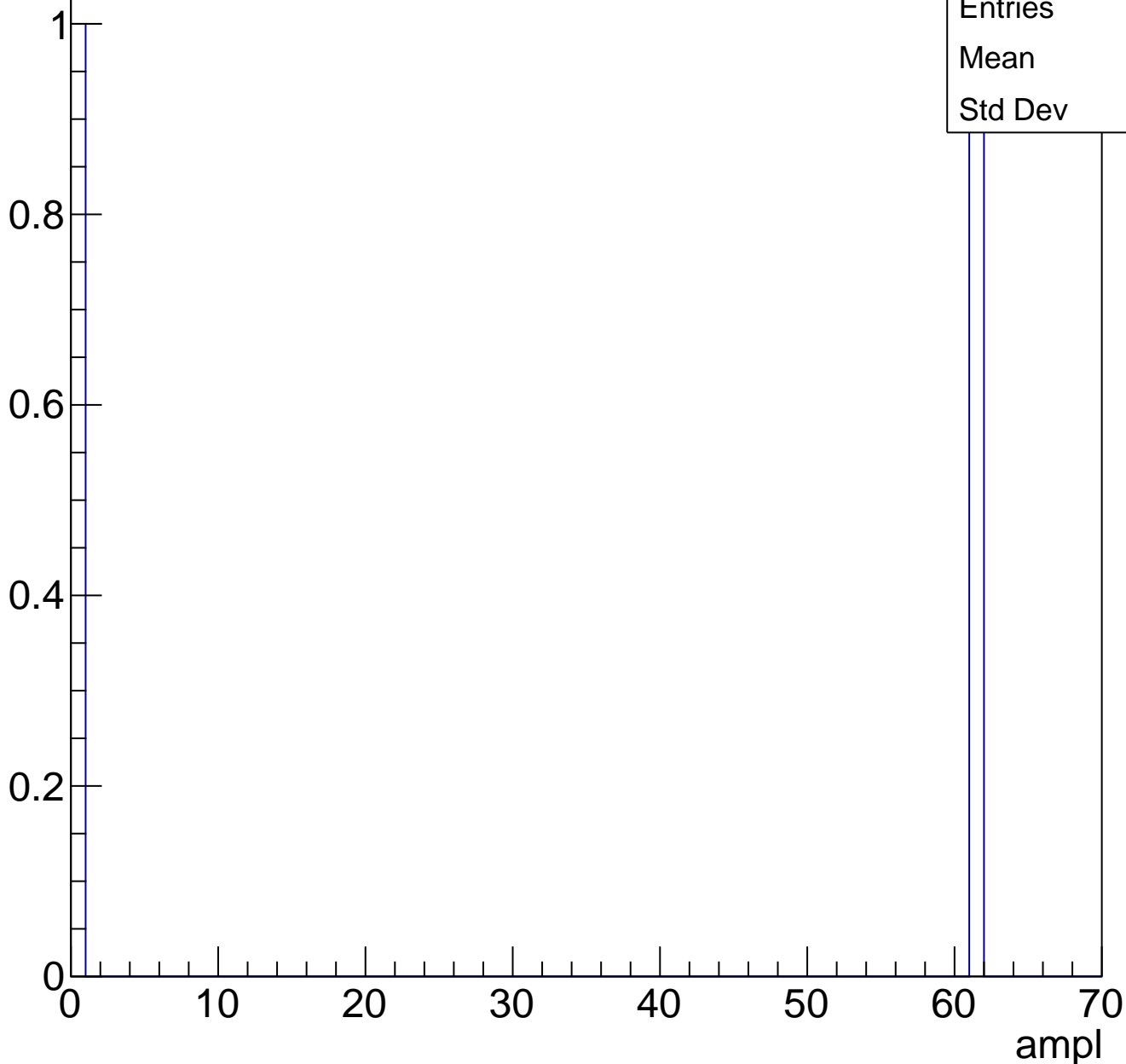




# B1L102S, U3-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U3-ch127, adc0

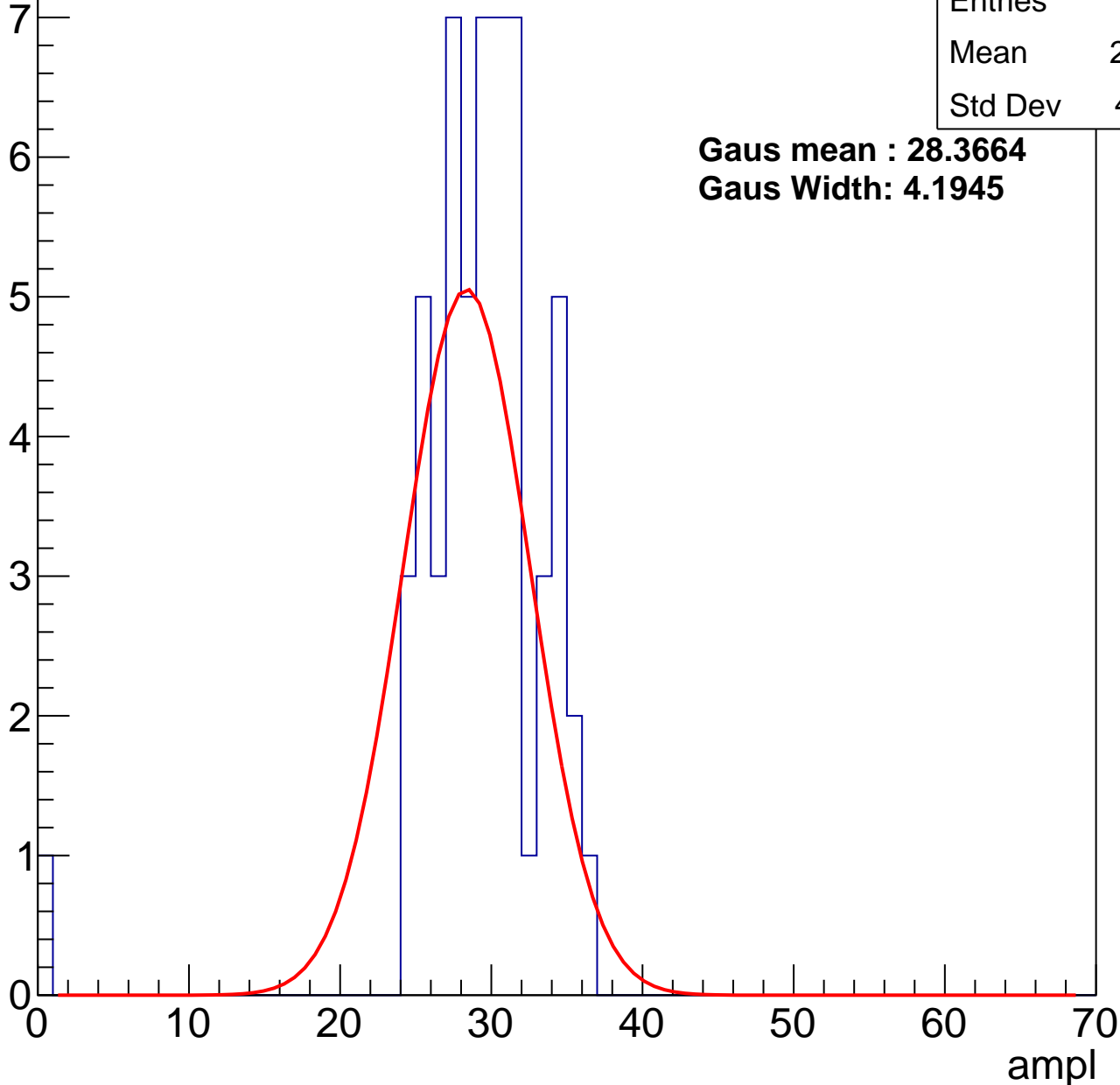
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	28.79
Std Dev	4.941

**Gaus mean : 28.3664**

**Gaus Width: 4.1945**



# B1L102S, U3-ch127, adc1

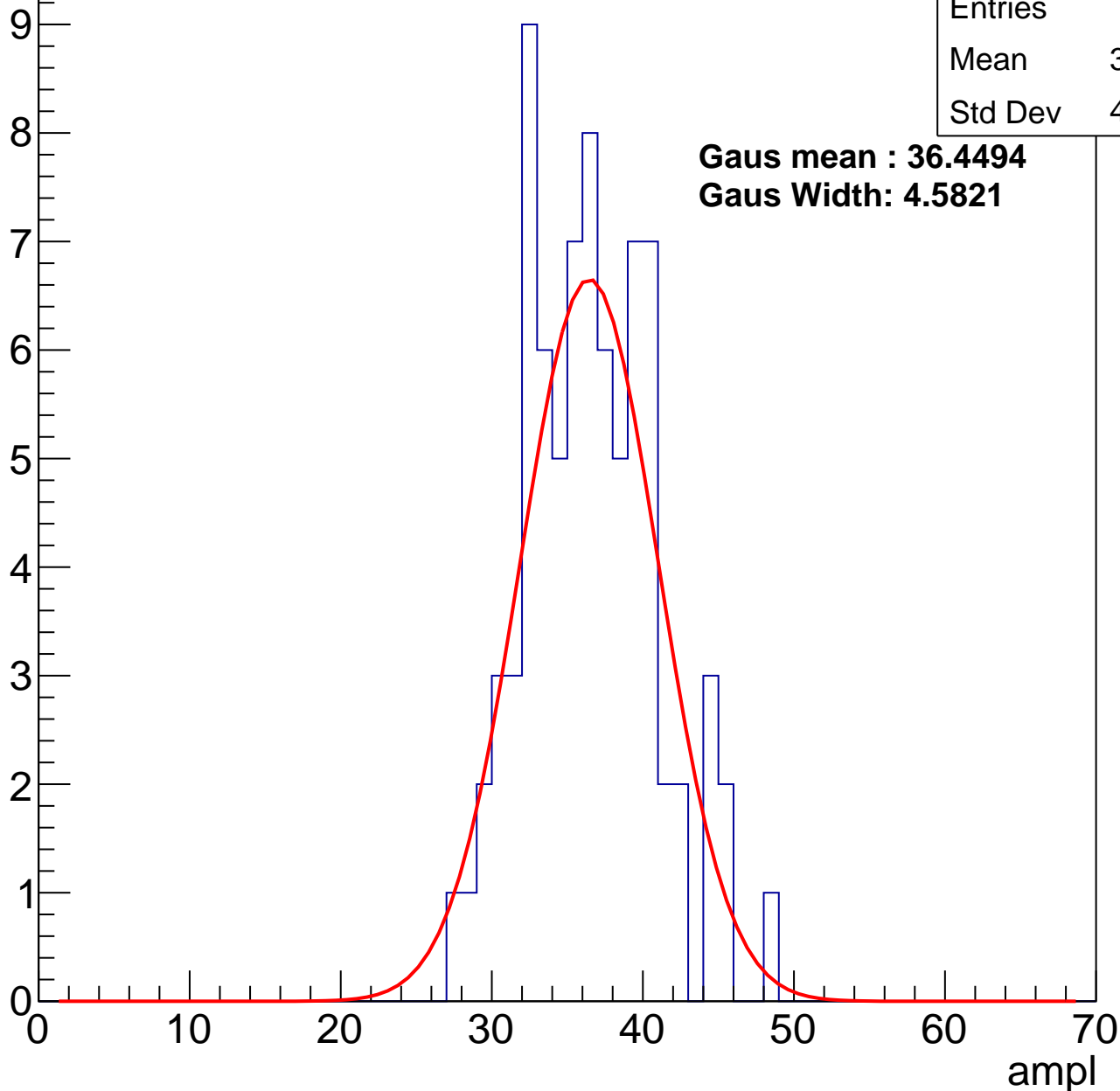
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	36.08
Std Dev	4.289

**Gaus mean : 36.4494**

**Gaus Width: 4.5821**



# B1L102S, U3-ch127, adc2

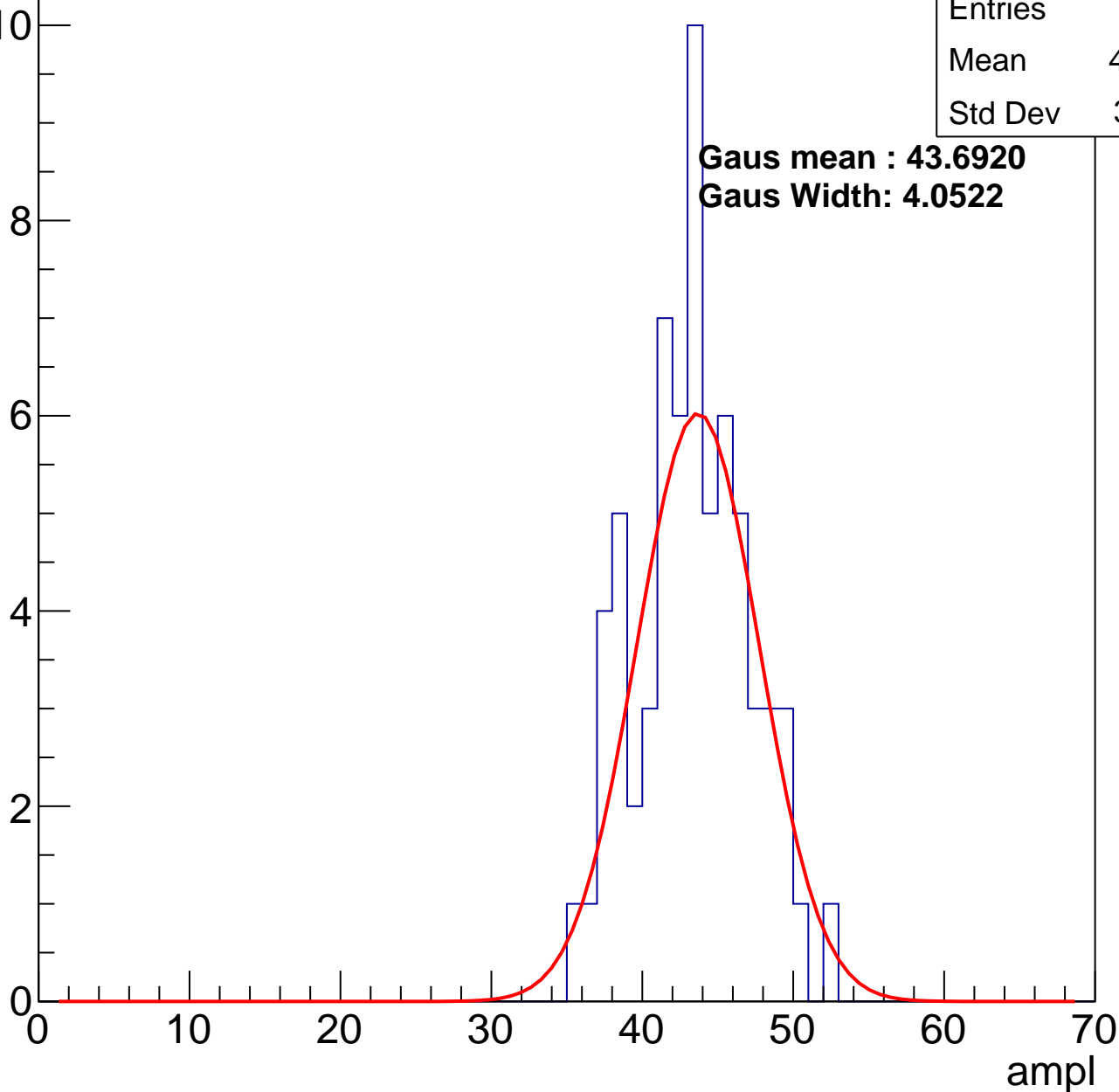
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	42.88
Std Dev	3.711

**Gaus mean : 43.6920**

**Gaus Width: 4.0522**

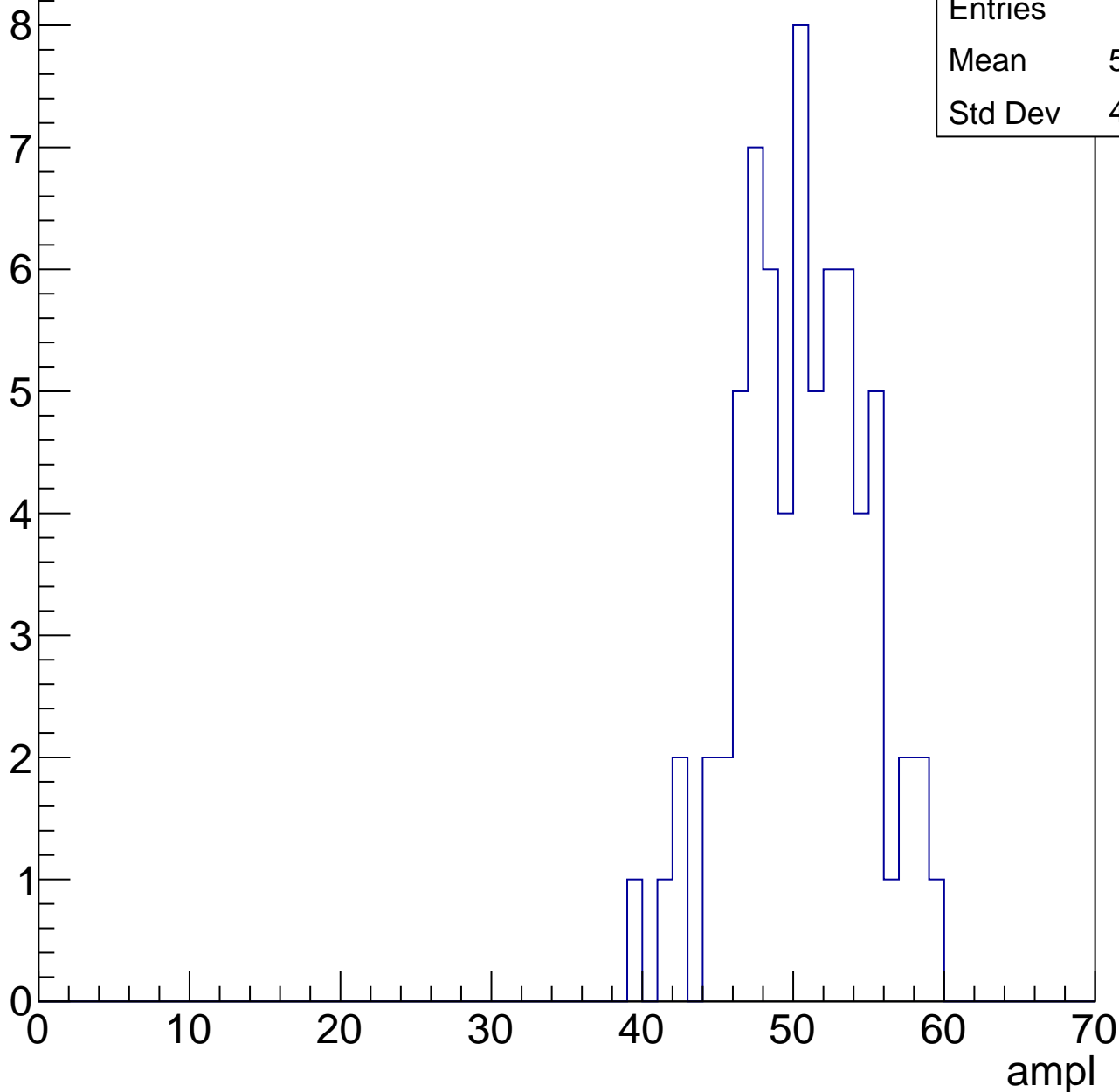


# B1L102S, U3-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

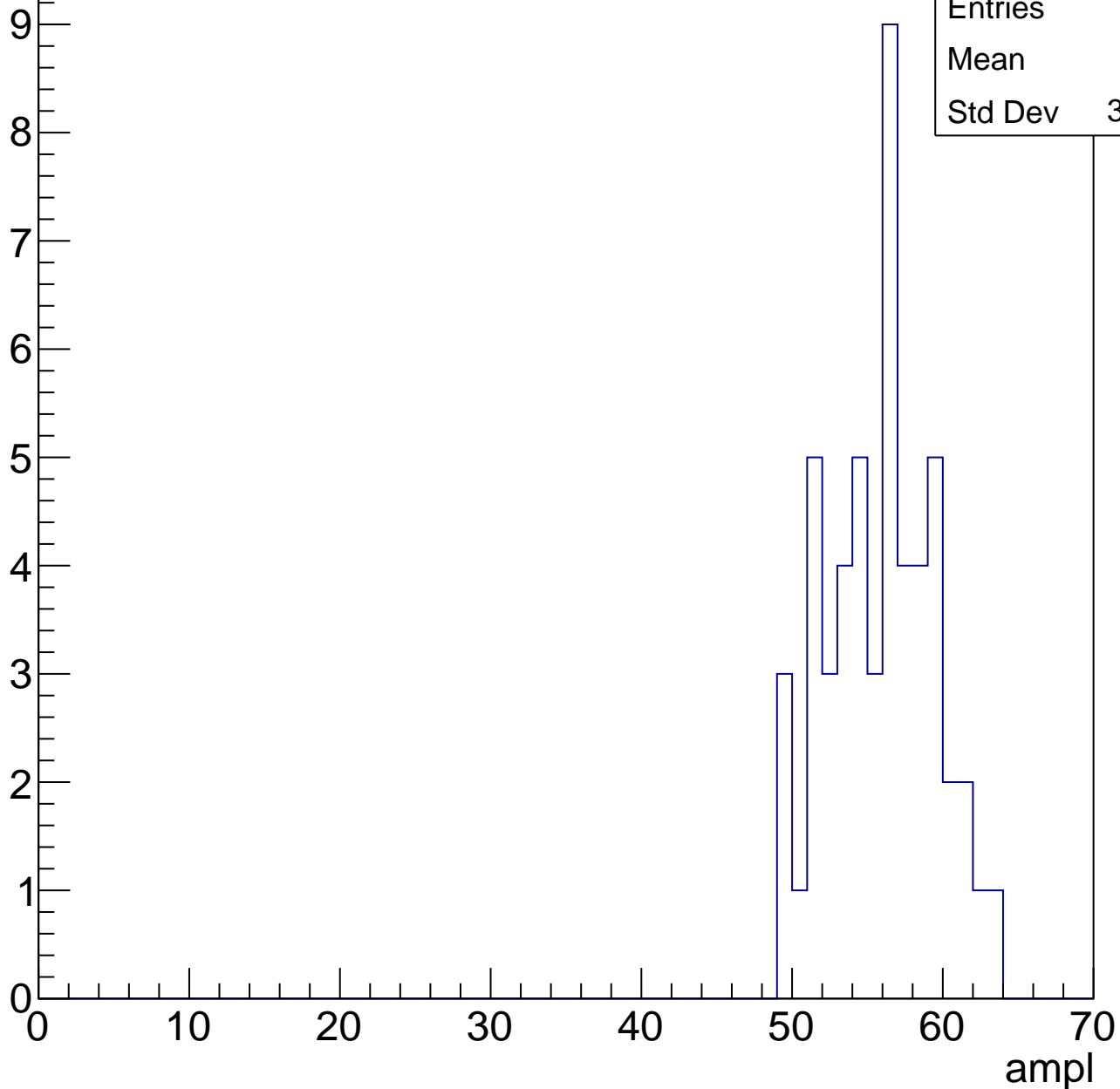
Entries	70
Mean	50.09
Std Dev	4.205



# B1L102S, U3-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

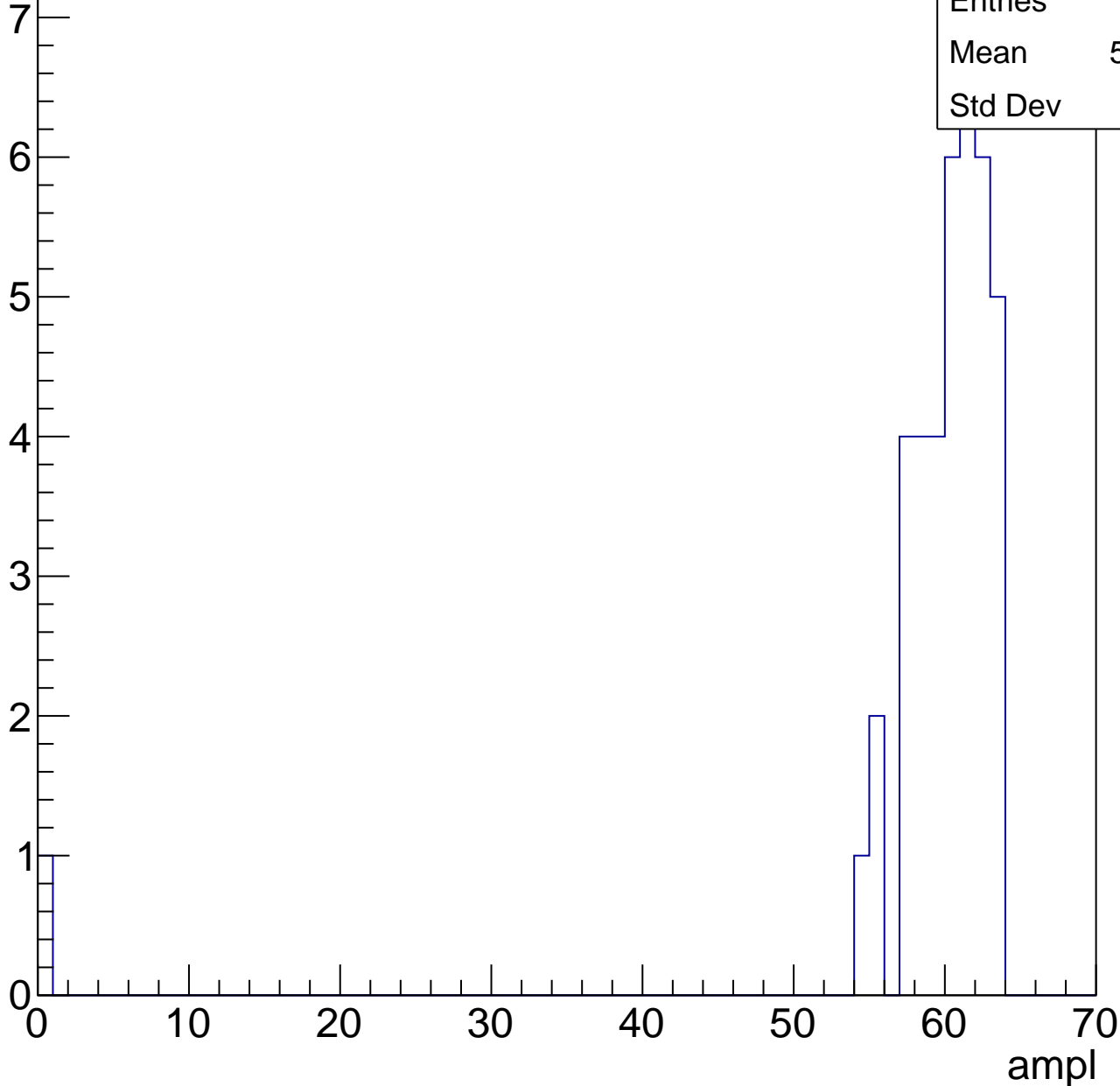


# B1L102S, U3-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

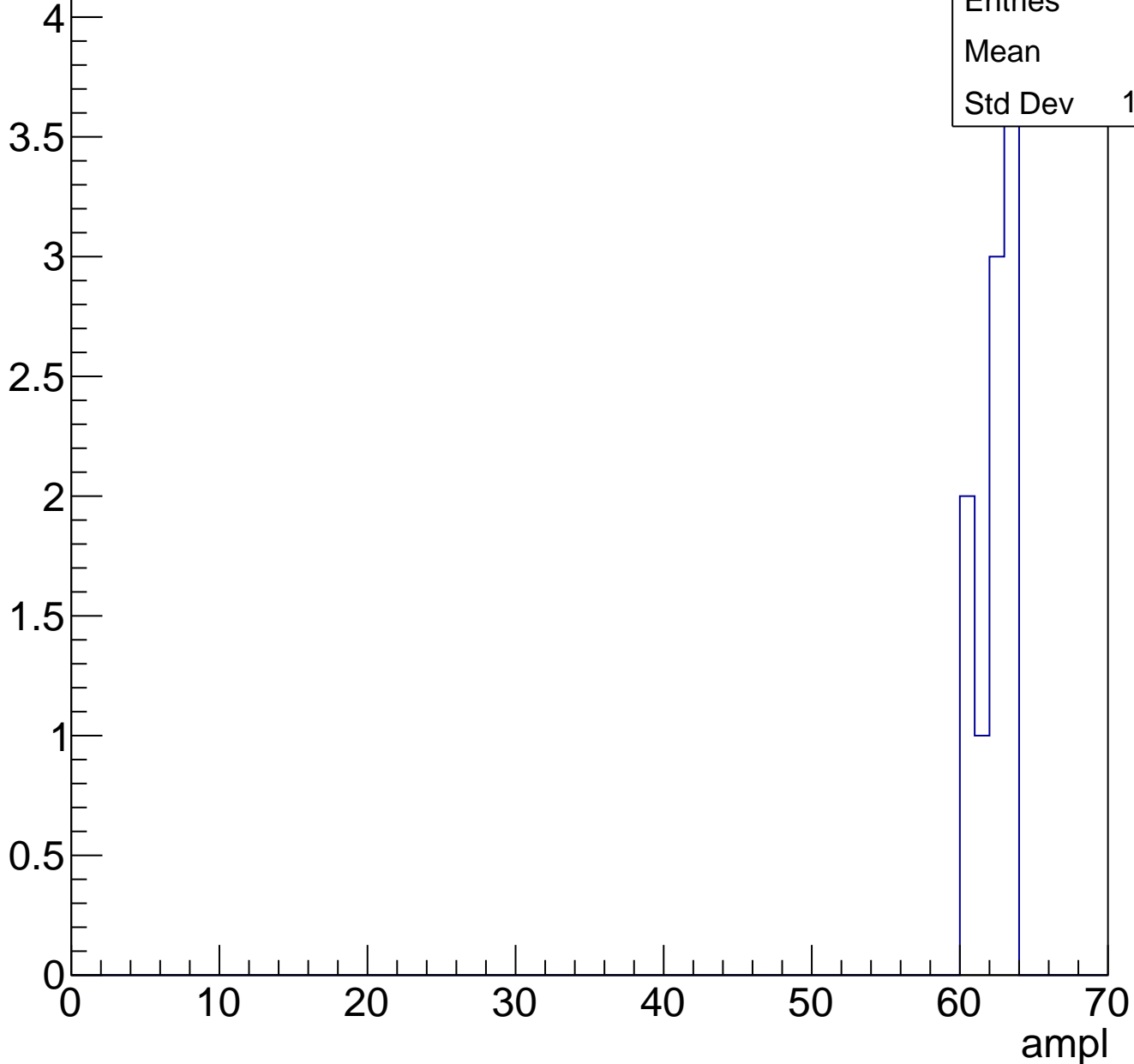
Entries	40
Mean	58.35
Std Dev	9.63



# B1L102S, U3-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U3-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U3-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

