

B0L100S, U15-ch0

calib_packv5_042523_0143.root, FC#6, port A1

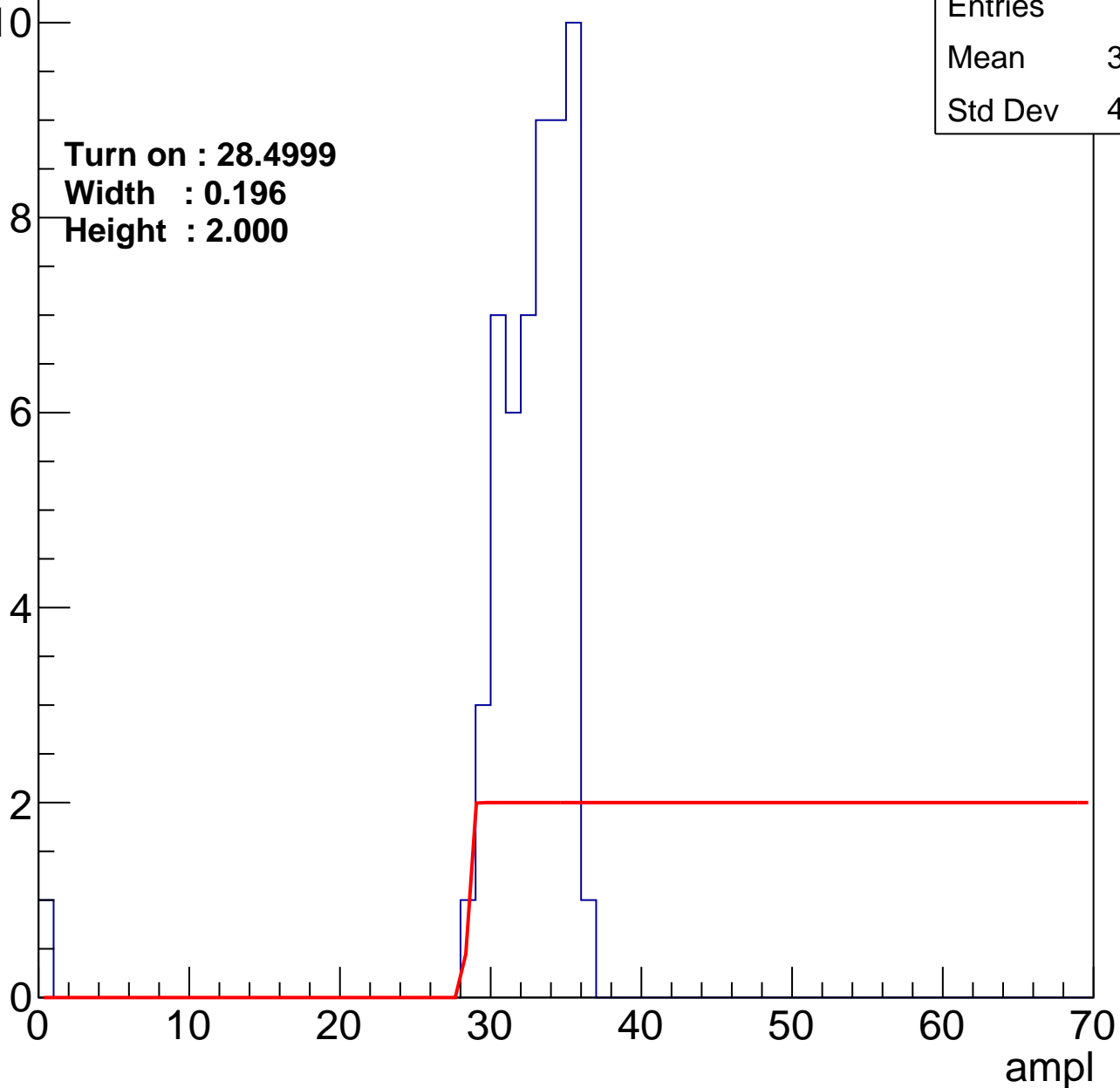
Entry

Entries	54
Mean	31.93
Std Dev	4.815

Turn on : 28.4999

Width : 0.196

Height : 2.000



B0L100S, U15-ch1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch8

calib_packv5_042523_0143.root, FC#6, port A1

Entries	337
Mean	46.52
Std Dev	10.07

Turn on : 29.9451

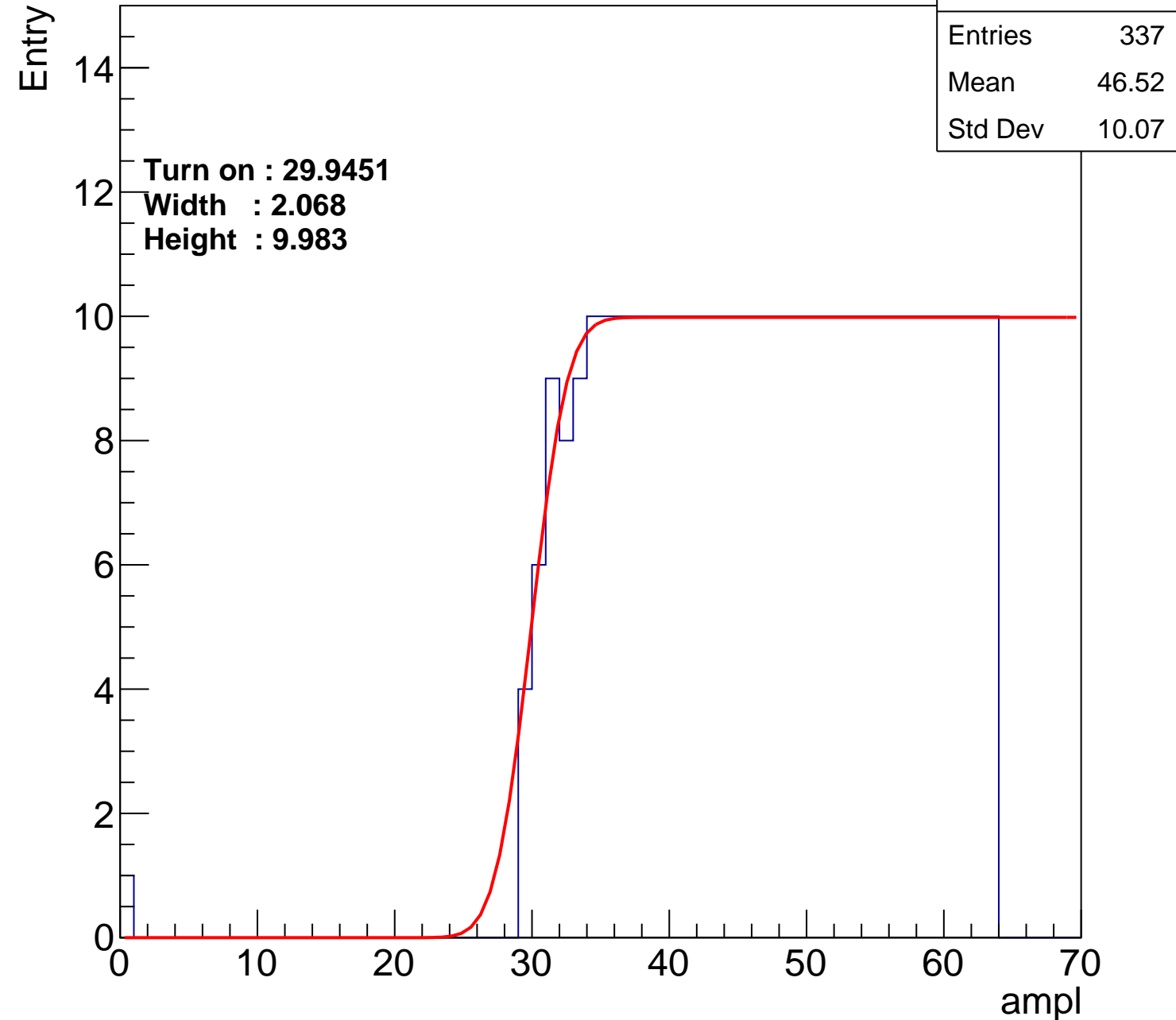
Width : 2.068

Height : 9.983

Entry

14
12
10
8
6
4
2
0

ampl



B0L100S, U15-ch9

calib_packv5_042523_0143.root, FC#6, port A1

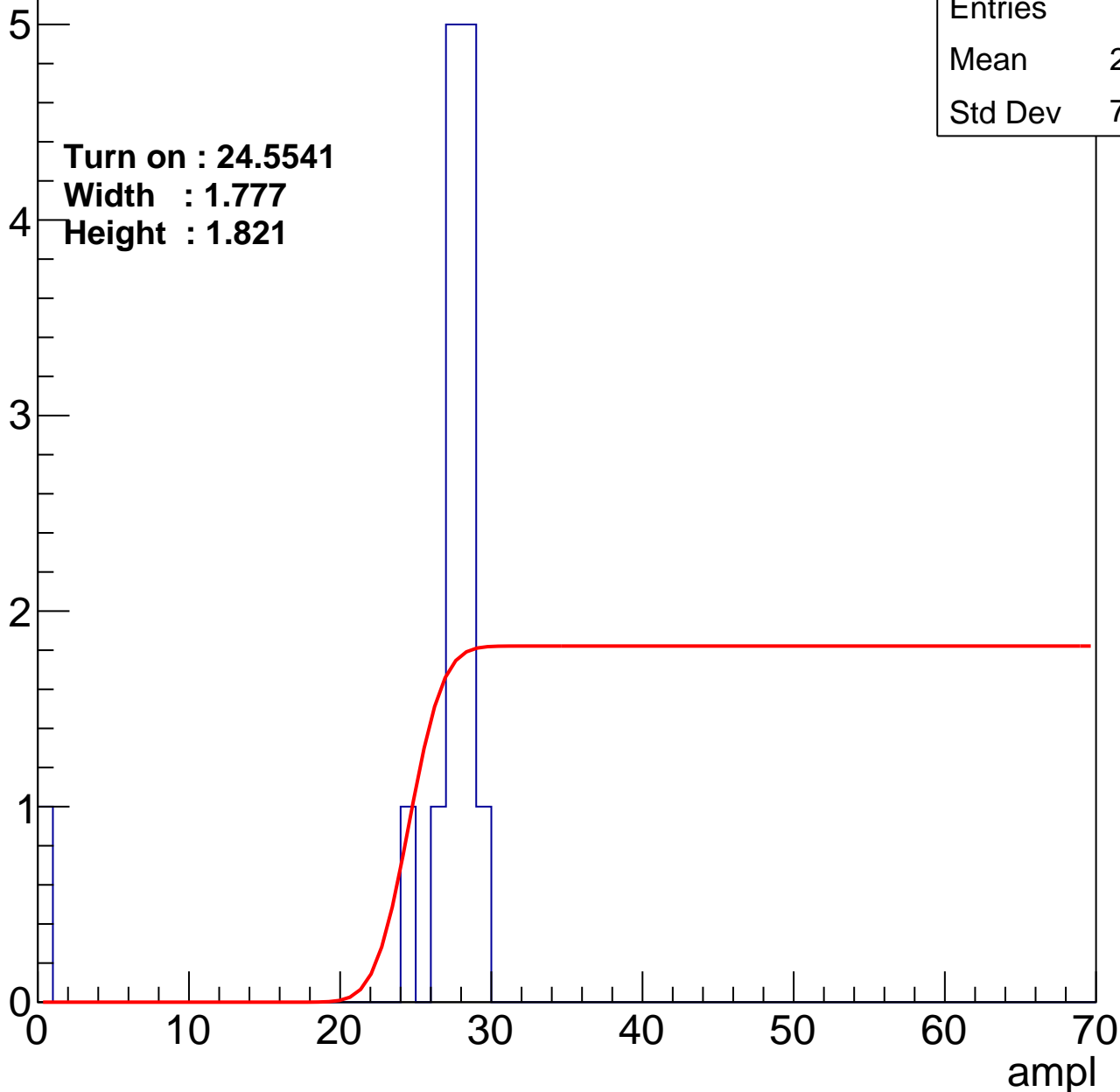
Entry

Entries	14
Mean	25.29
Std Dev	7.106

Turn on : 24.5541

Width : 1.777

Height : 1.821



B0L100S, U15-ch10

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch11

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch12

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U15-ch13

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

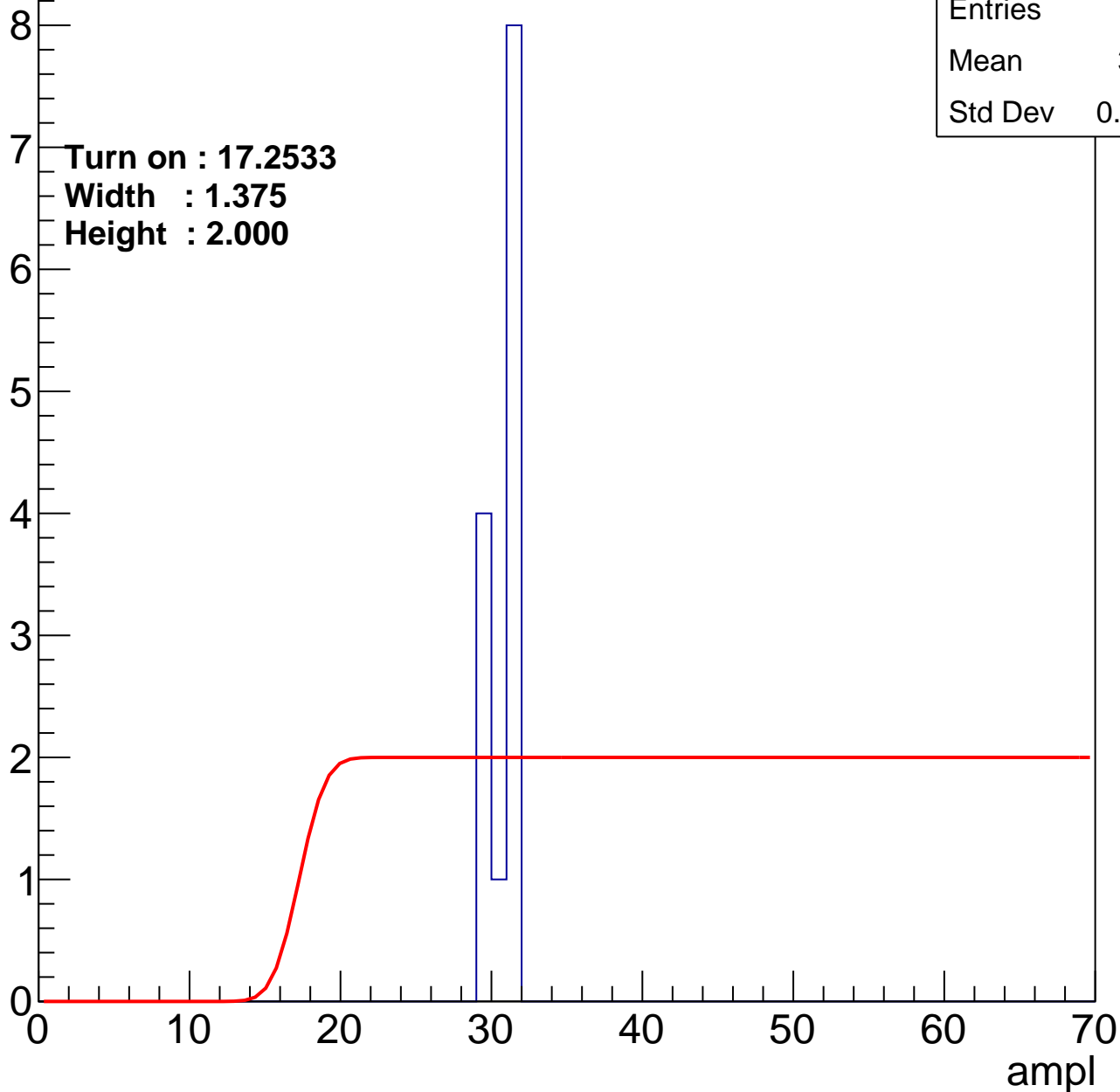
B0L100S, U15-ch14

calib_packv5_042523_0143.root, FC#6, port A1

Entry

Entries	13
Mean	30.31
Std Dev	0.9102

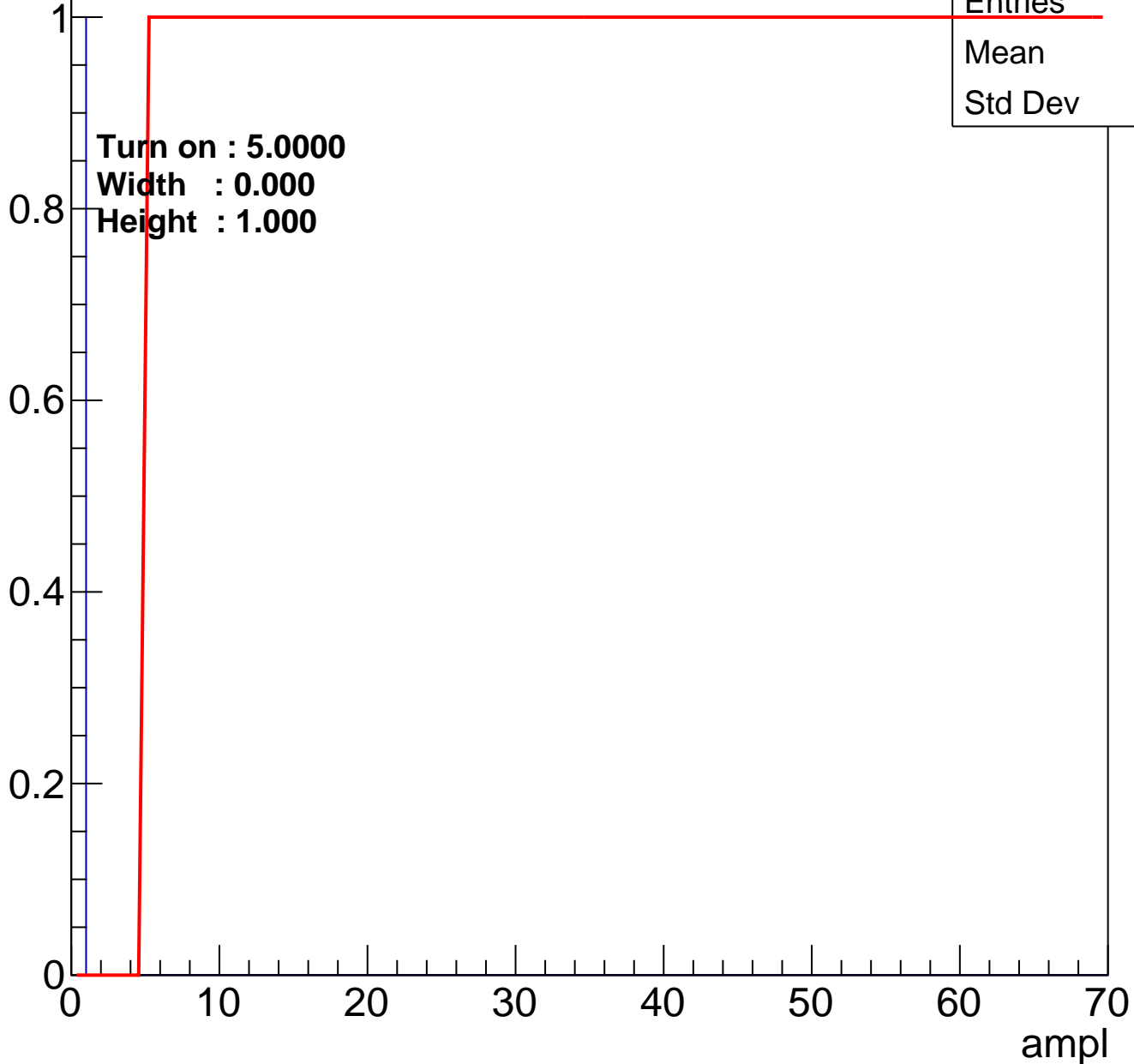
Turn on : 17.2533
Width : 1.375
Height : 2.000



B0L100S, U15-ch15

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	1
Mean	0
Std Dev	0

B0L100S, U15-ch16

calib_packv5_042523_0143.root, FC#6, port A1

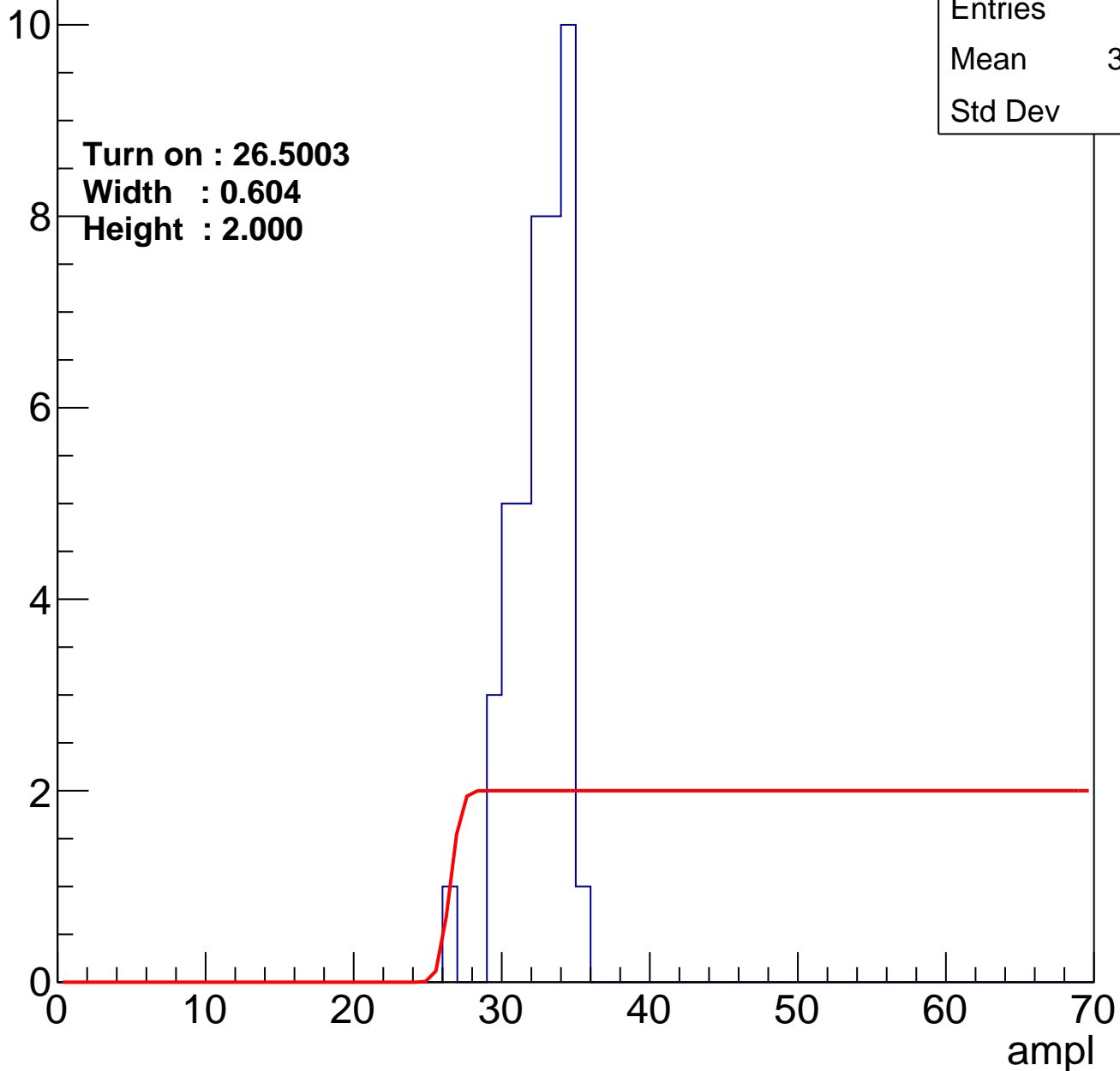
Entries	41
Mean	32.02
Std Dev	1.88

Turn on : 26.5003

Width : 0.604

Height : 2.000

Entry



B0L100S, U15-ch17

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch18

calib_packv5_042523_0143.root, FC#6, port A1

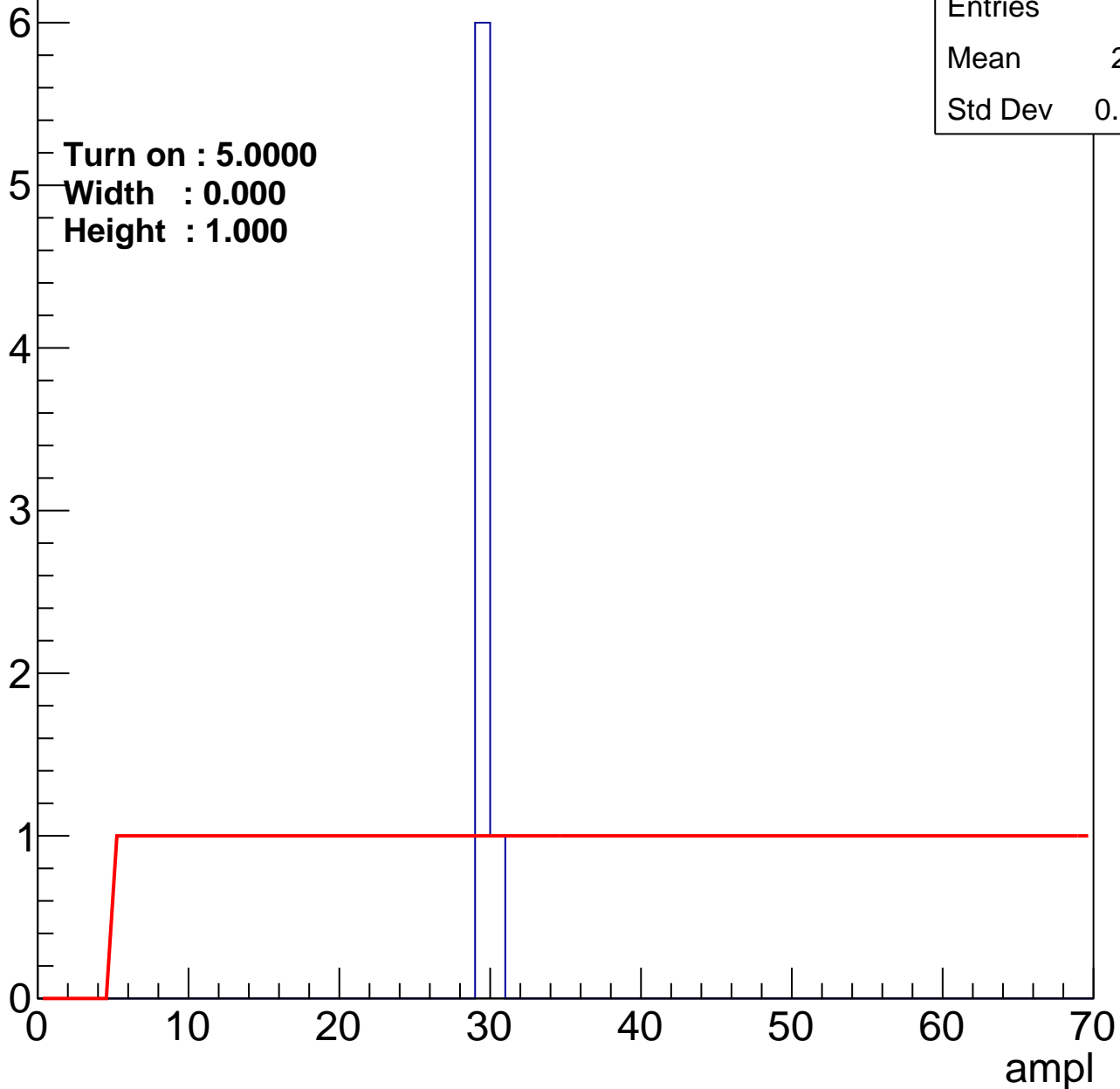
Entry

Entries	7
Mean	29.14
Std Dev	0.3499

Turn on : 5.0000

Width : 0.000

Height : 1.000



B0L100S, U15-ch19

calib_packv5_042523_0143.root, FC#6, port A1

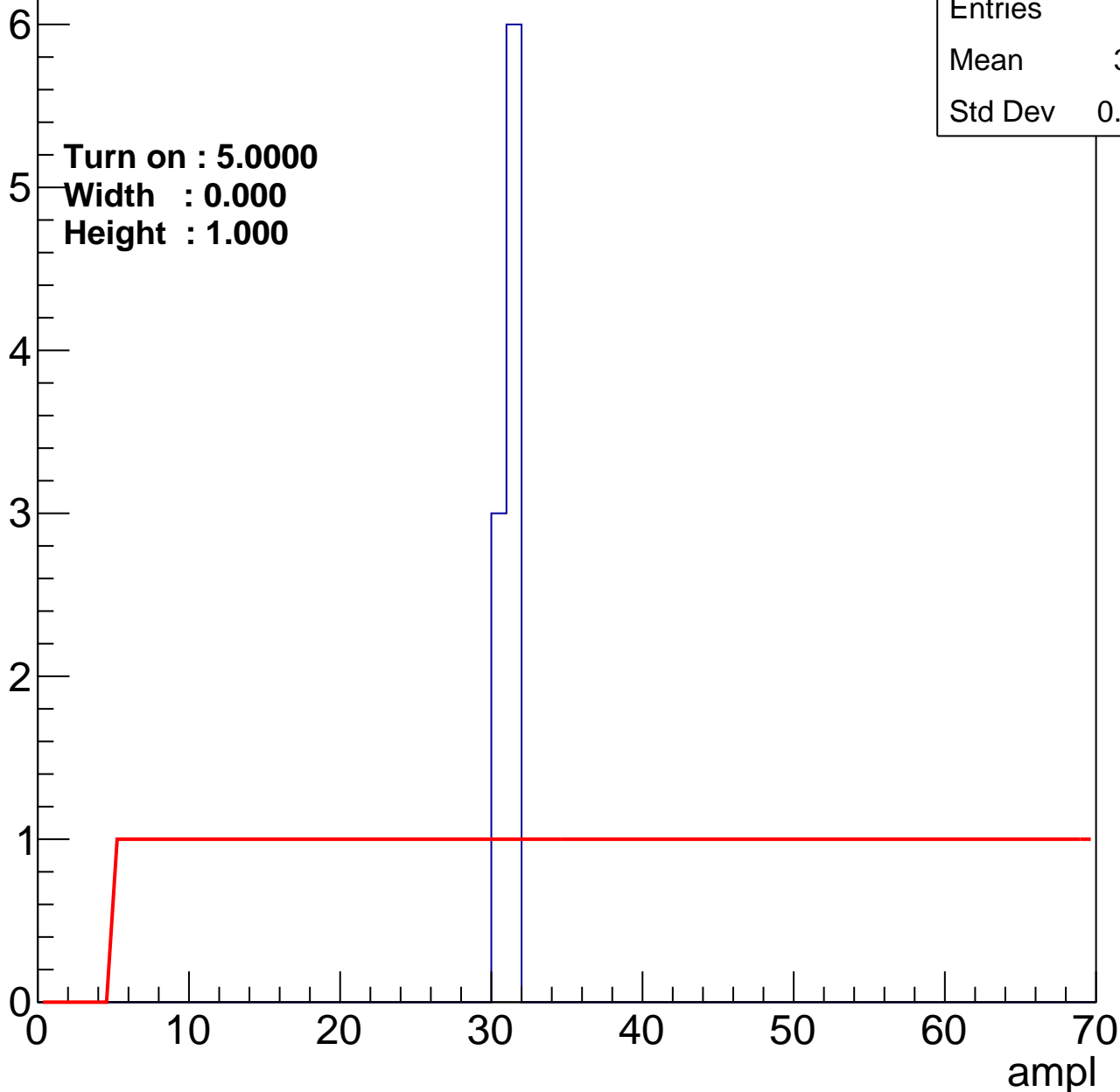
Entry

Entries	9
Mean	30.67
Std Dev	0.4714

Turn on : 5.0000

Width : 0.000

Height : 1.000



B0L100S, U15-ch20

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch21

calib_packv5_042523_0143.root, FC#6, port A1

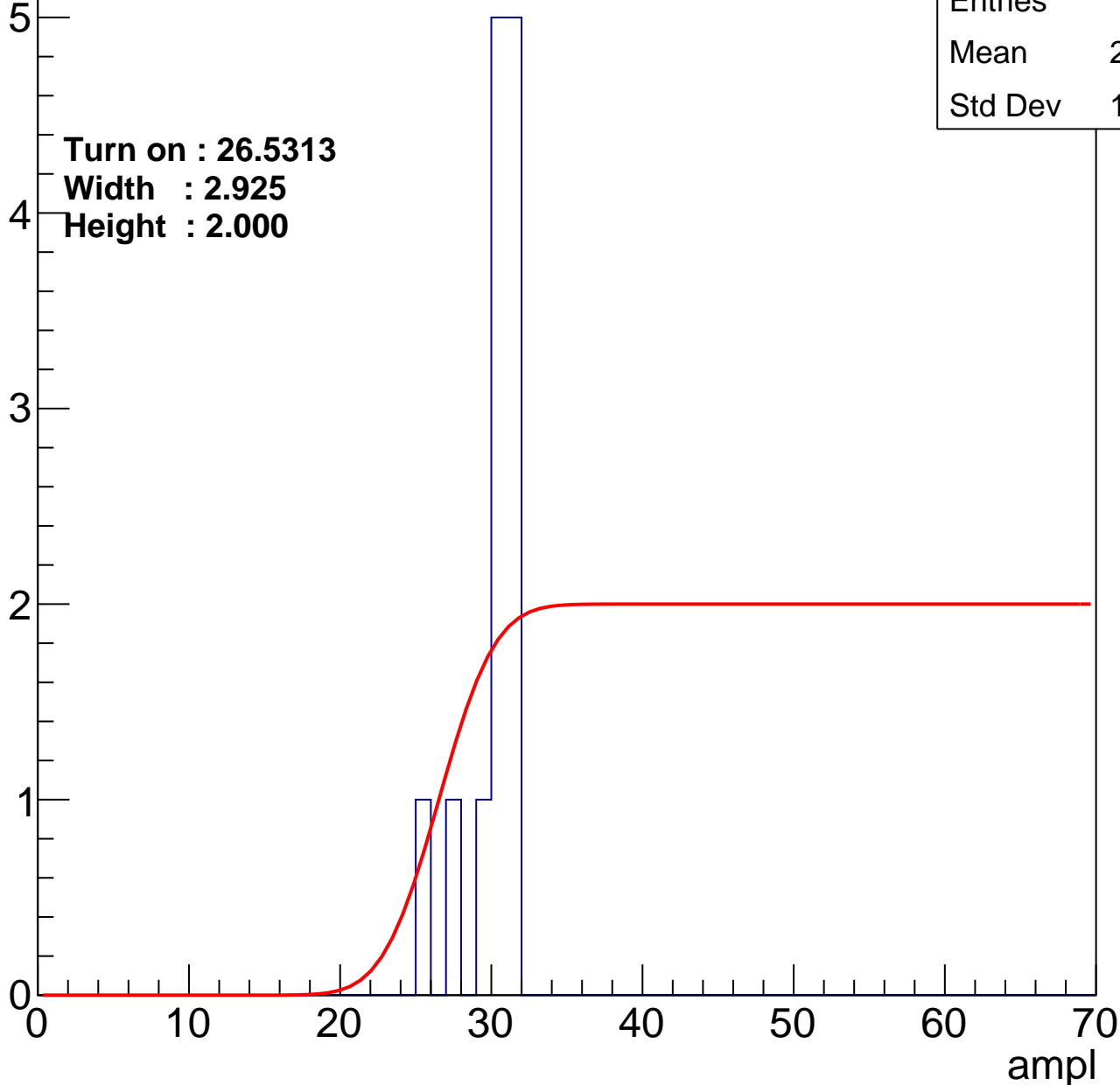
Entry

Entries	13
Mean	29.69
Std Dev	1.727

Turn on : 26.5313

Width : 2.925

Height : 2.000



B0L100S, U15-ch22

calib_packv5_042523_0143.root, FC#6, port A1

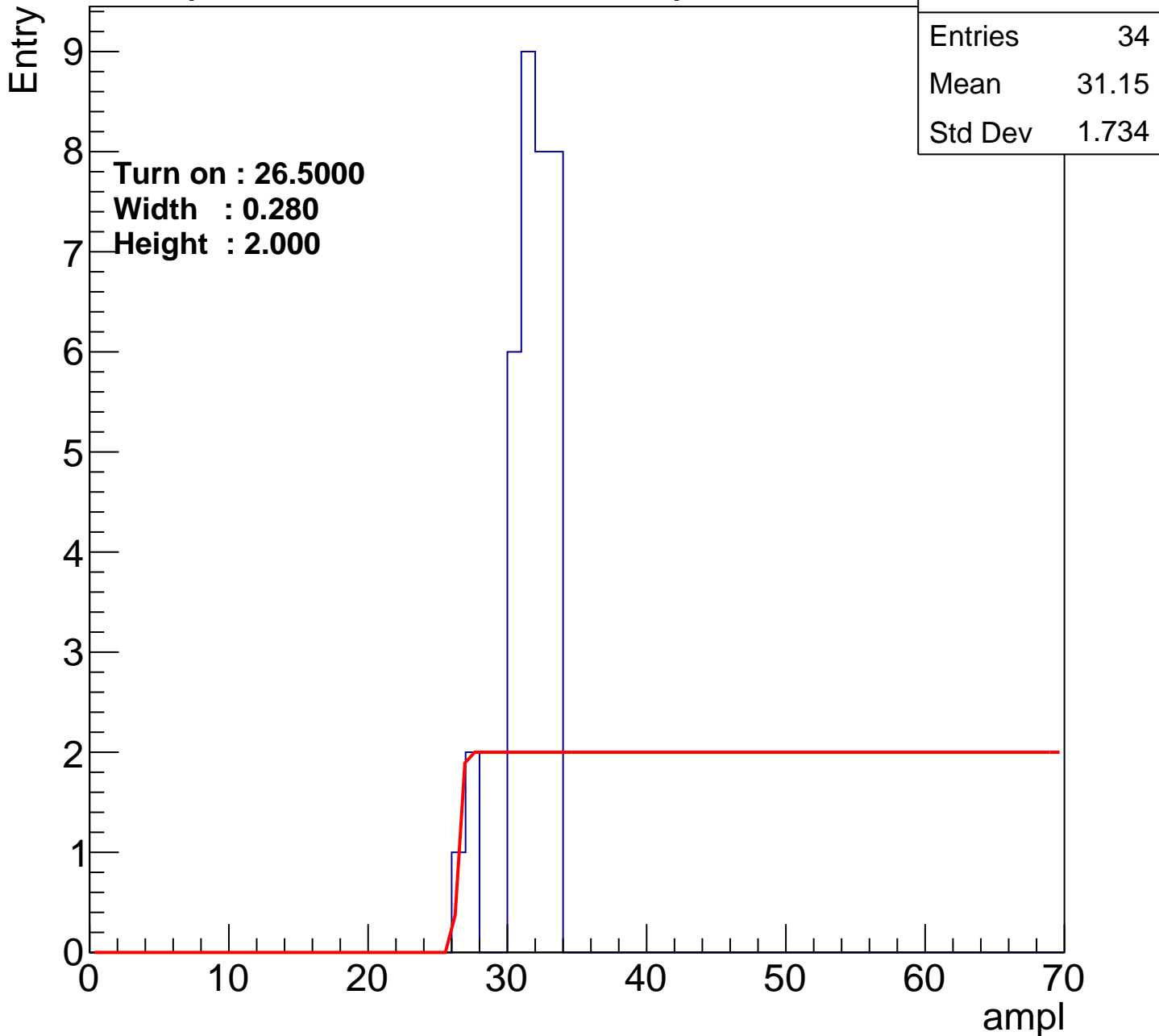
Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch23

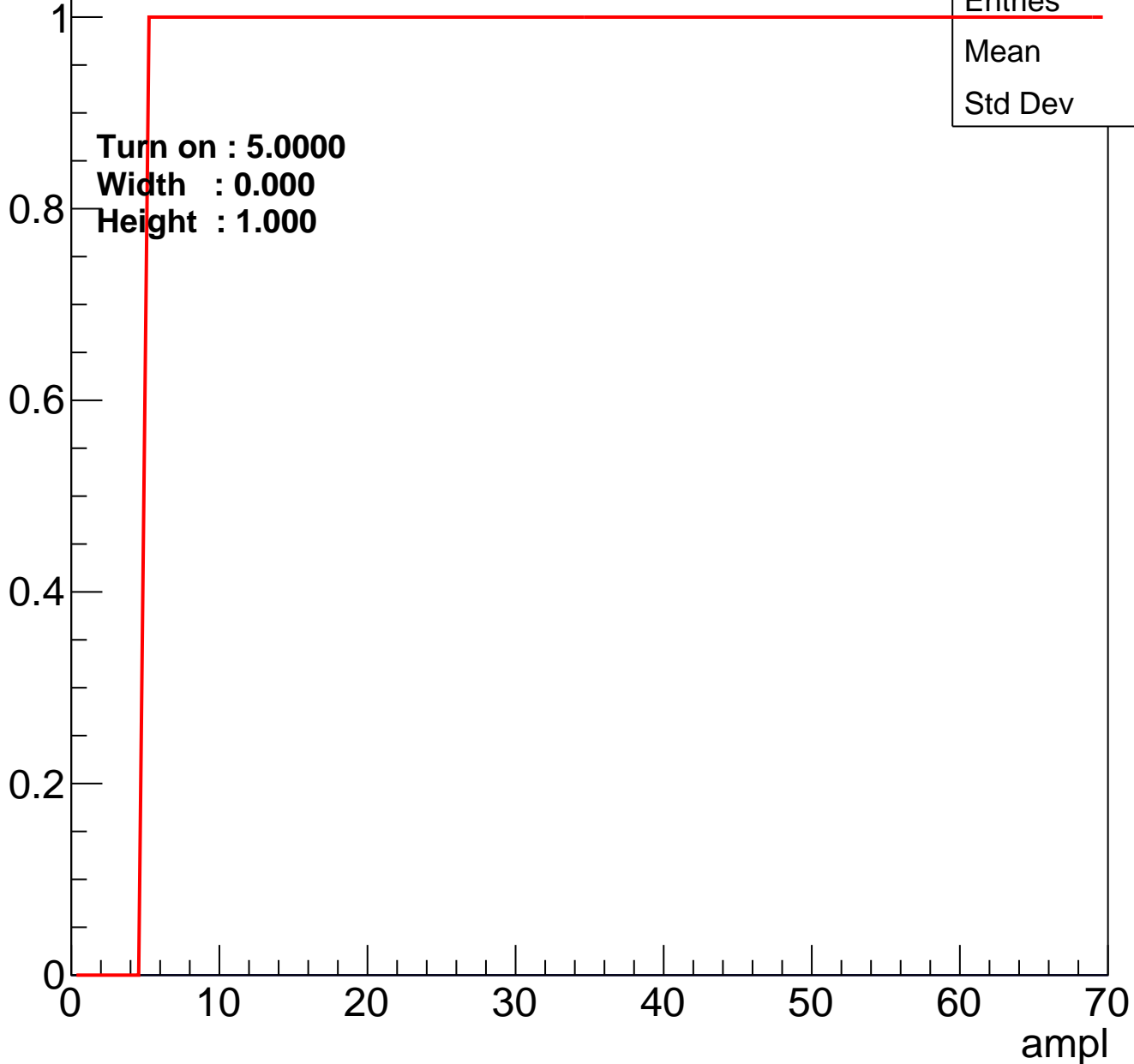
calib_packv5_042523_0143.root, FC#6, port A1



B0L100S, U15-ch24

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch25

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch26

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	1
Mean	0
Std Dev	0

B0L100S, U15-ch27

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch28

calib_packv5_042523_0143.root, FC#6, port A1

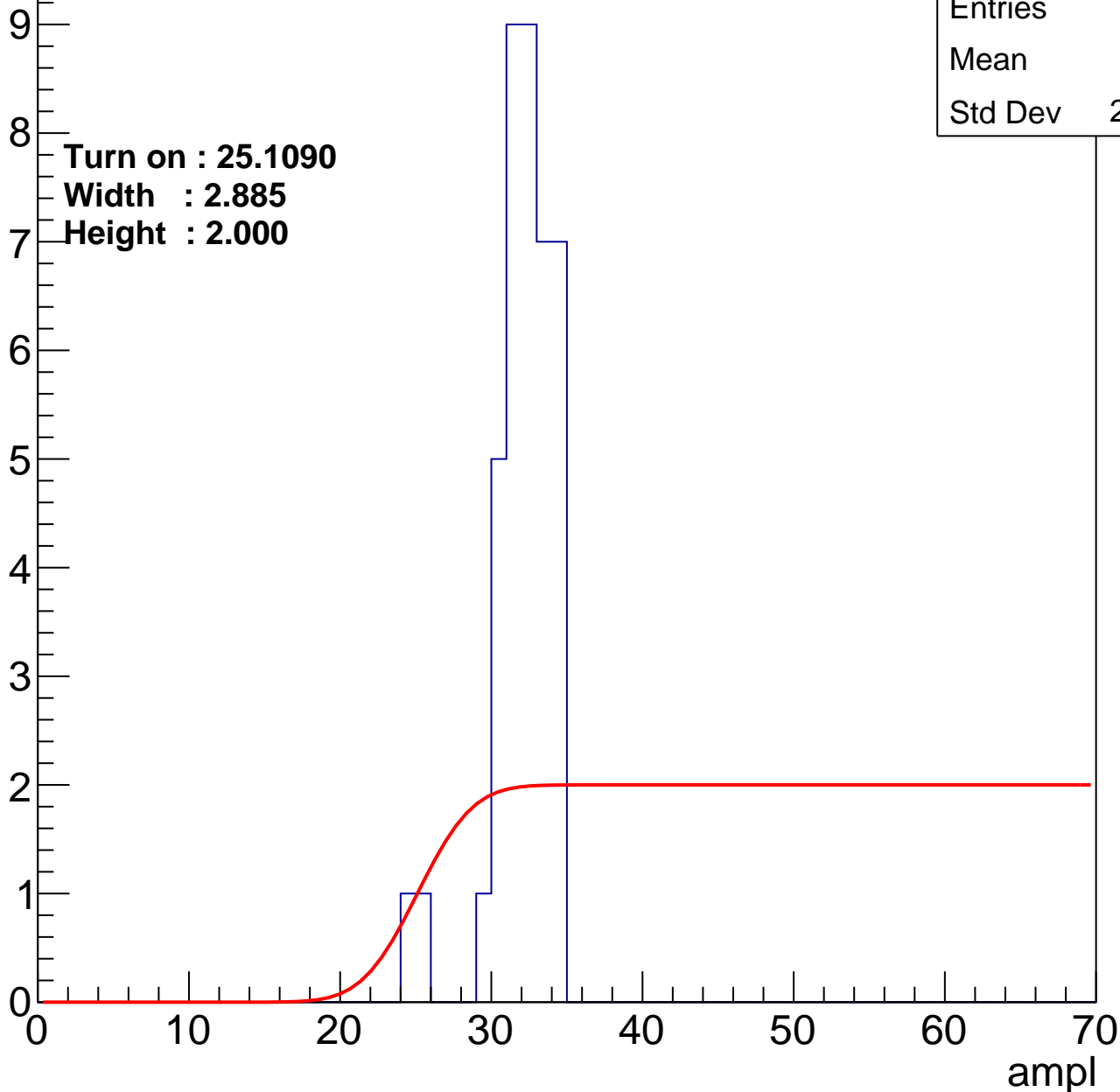
Entry

Entries	40
Mean	31.6
Std Dev	2.119

Turn on : 25.1090

Width : 2.885

Height : 2.000



B0L100S, U15-ch29

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch30

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

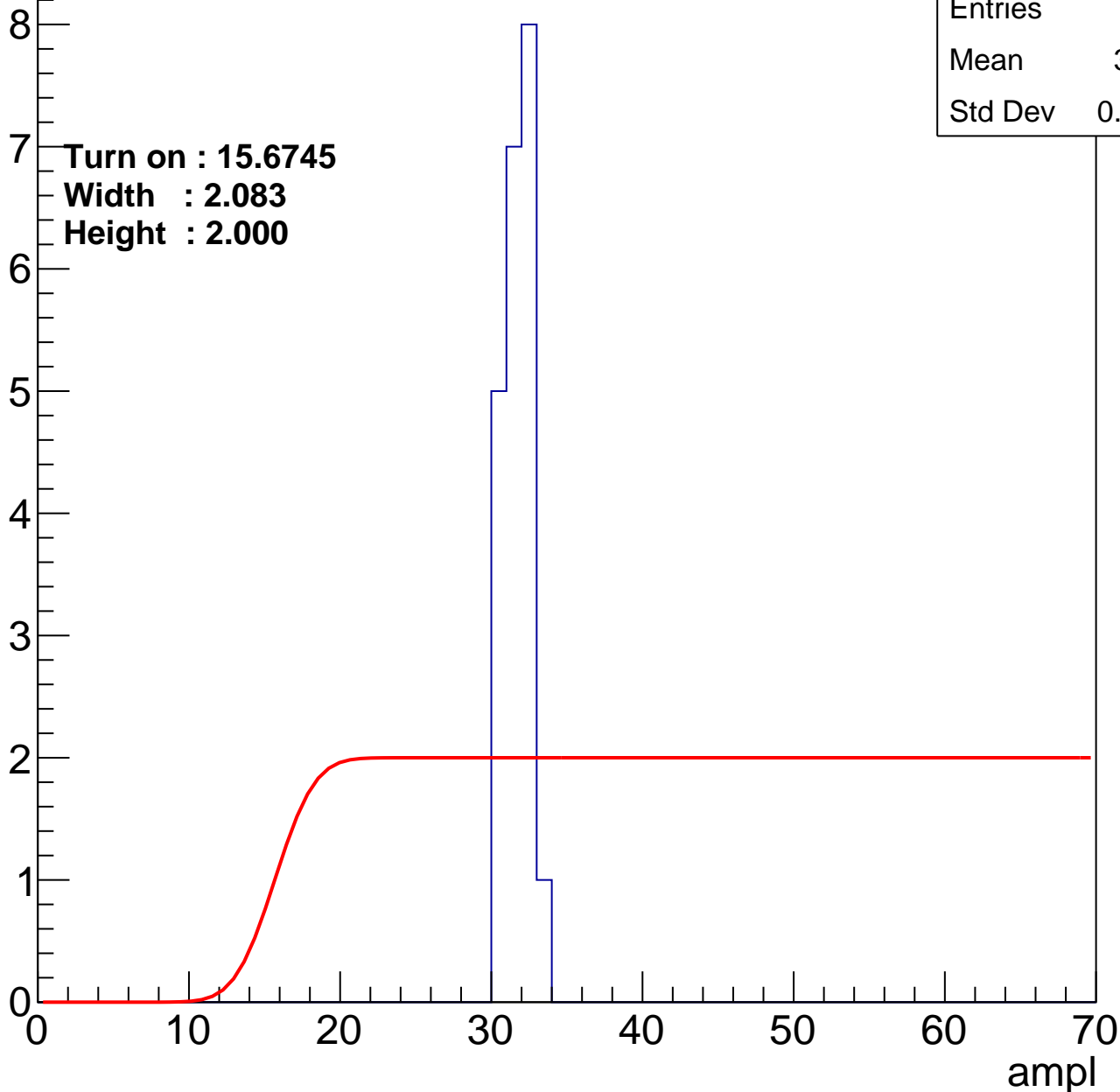
B0L100S, U15-ch31

calib_packv5_042523_0143.root, FC#6, port A1

Entry

Entries	21
Mean	31.24
Std Dev	0.8677

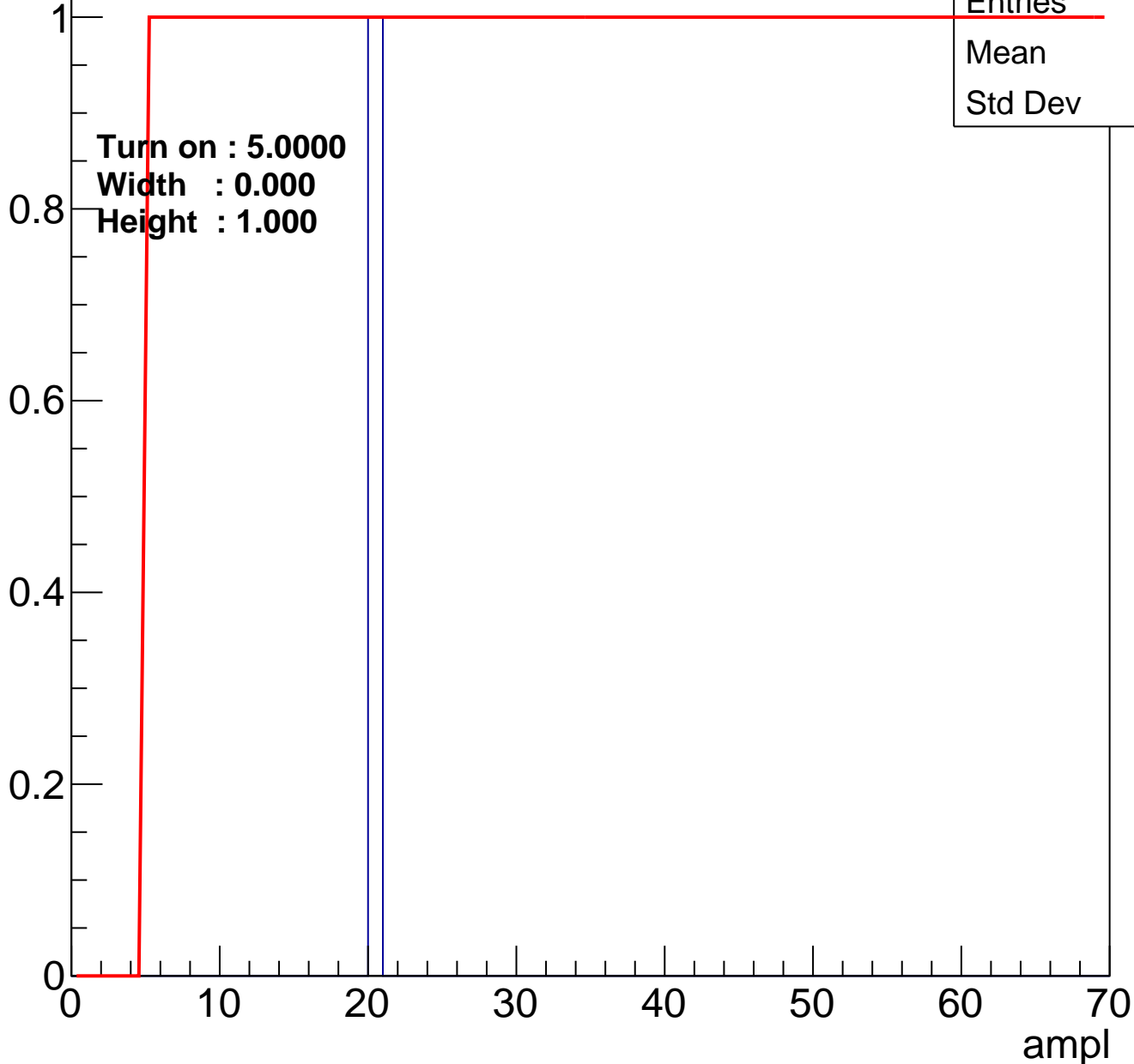
Turn on : 15.6745
Width : 2.083
Height : 2.000



B0L100S, U15-ch32

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	1
Mean	20
Std Dev	0

B0L100S, U15-ch33

calib_packv5_042523_0143.root, FC#6, port A1

Entry

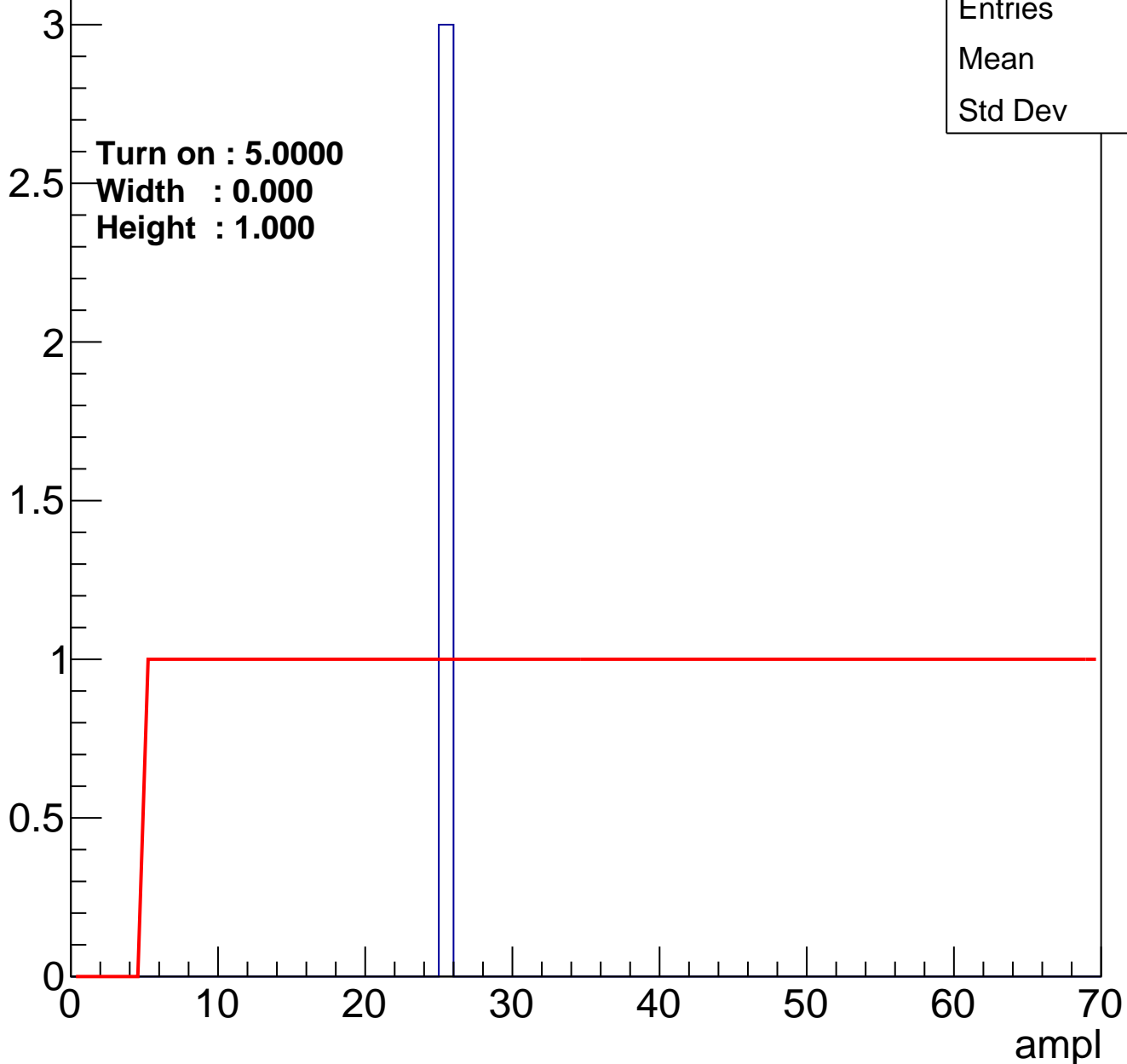


Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch34

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	3
Mean	25
Std Dev	0

B0L100S, U15-ch35

calib_packv5_042523_0143.root, FC#6, port A1

Entry

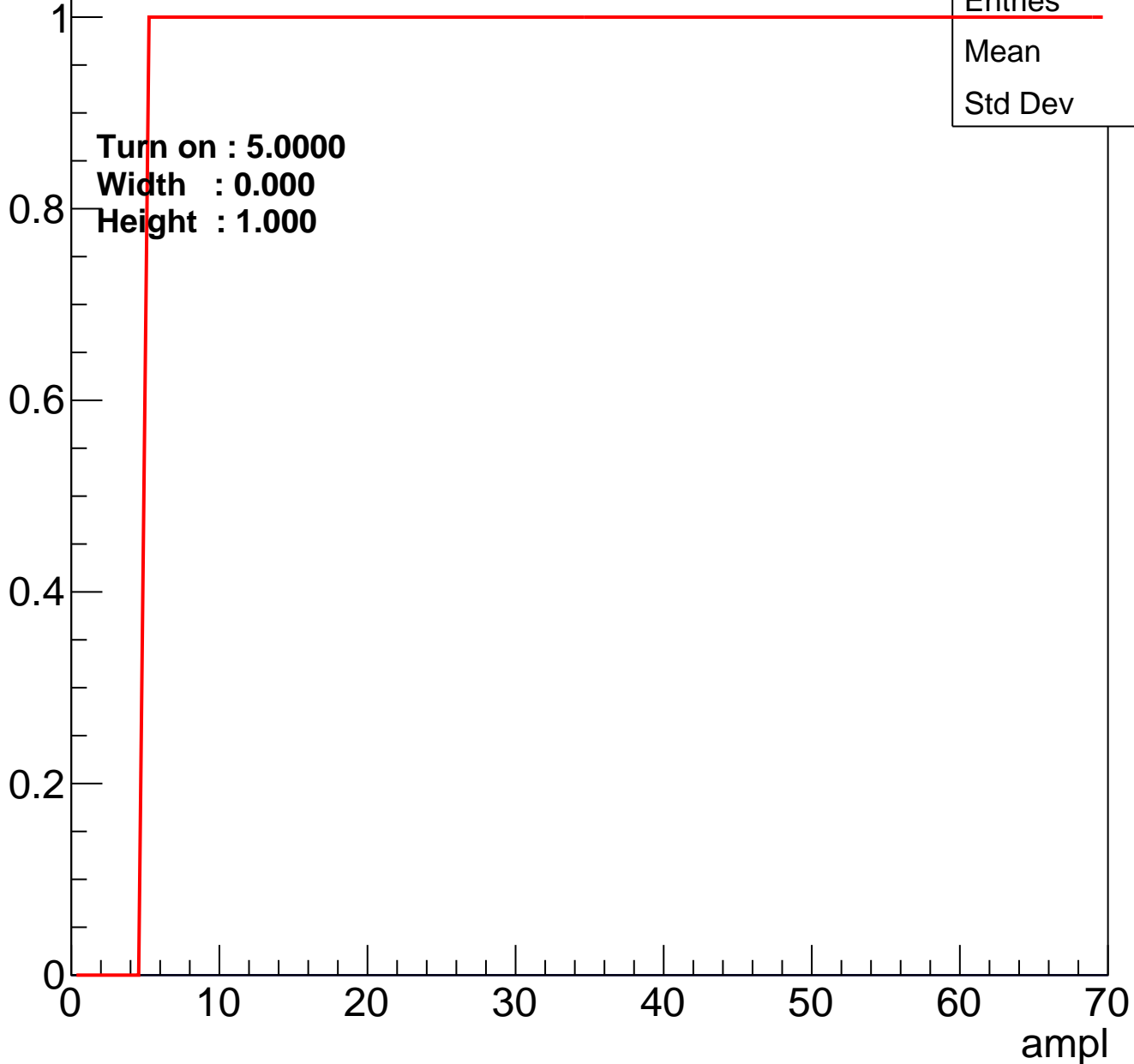


Entries	1
Mean	0
Std Dev	0

B0L100S, U15-ch36

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch37

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch38

calib_packv5_042523_0143.root, FC#6, port A1

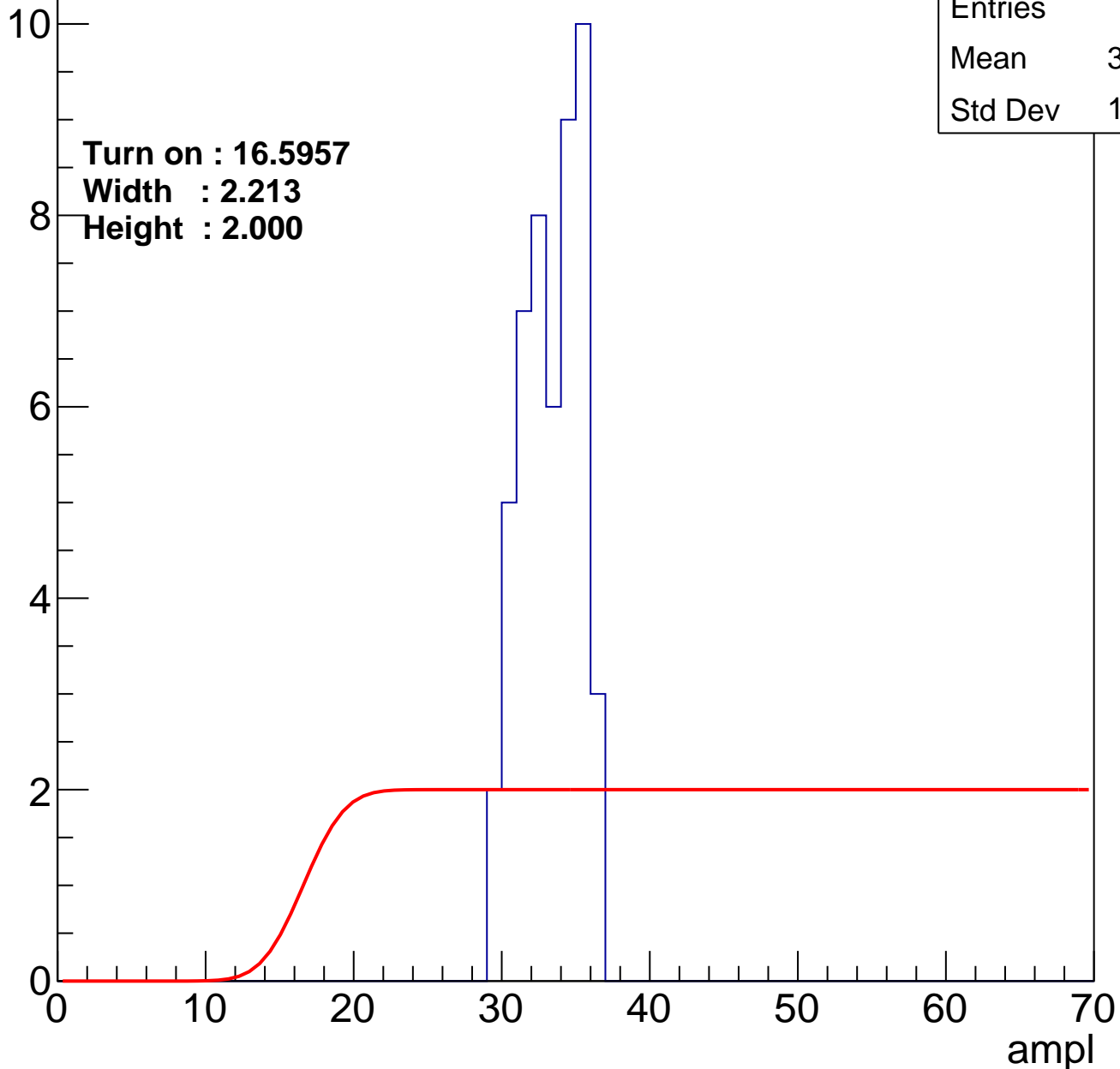
Entries	50
Mean	32.86
Std Dev	1.939

Turn on : 16.5957

Width : 2.213

Height : 2.000

Entry



B0L100S, U15-ch39

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch40

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch41

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch42

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch43

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch44

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch45

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

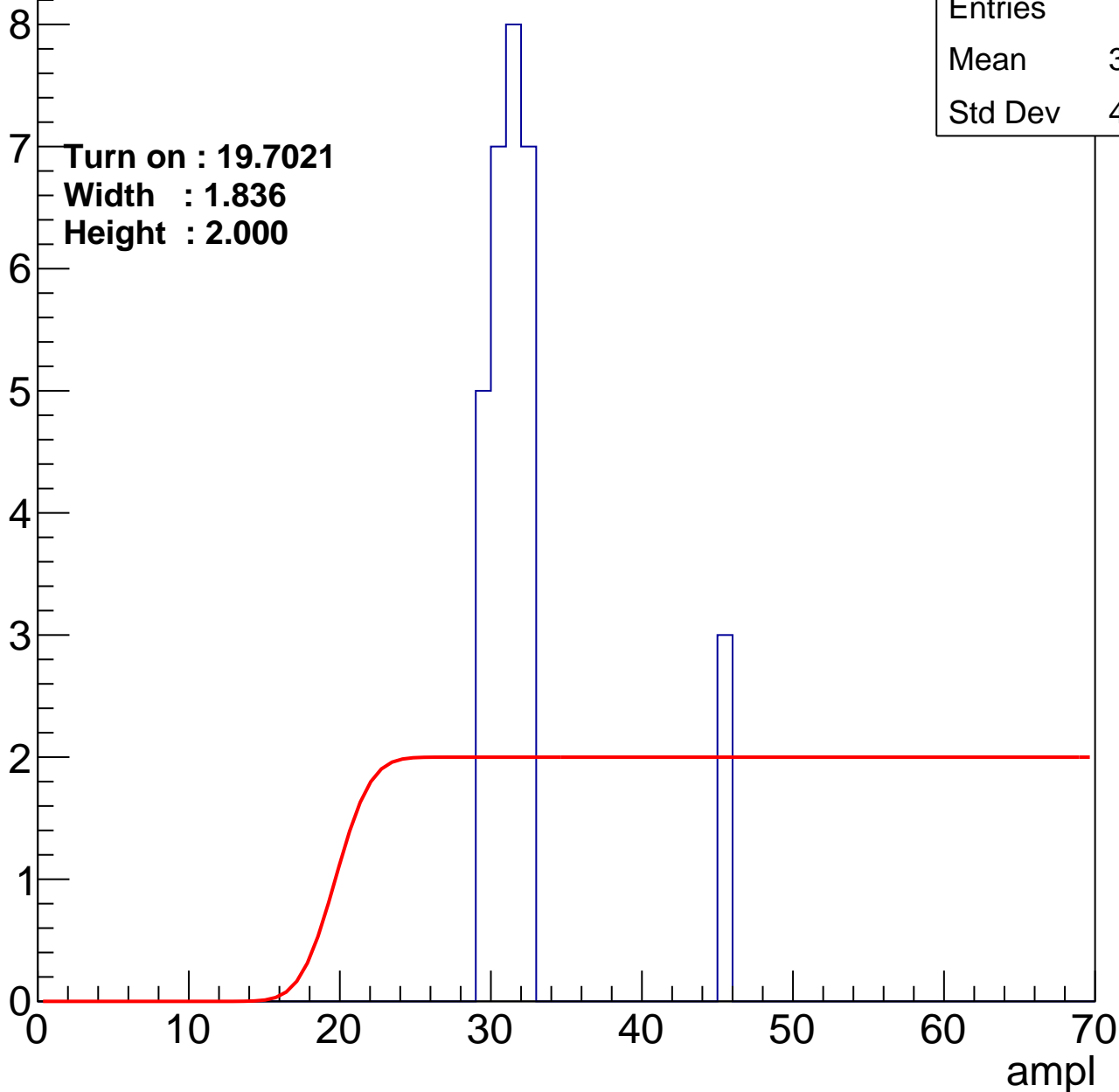
B0L100S, U15-ch46

calib_packv5_042523_0143.root, FC#6, port A1

Entry

Entries	30
Mean	32.07
Std Dev	4.427

Turn on : 19.7021
Width : 1.836
Height : 2.000



B0L100S, U15-ch47

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch48

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch49

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch50

calib_packv5_042523_0143.root, FC#6, port A1

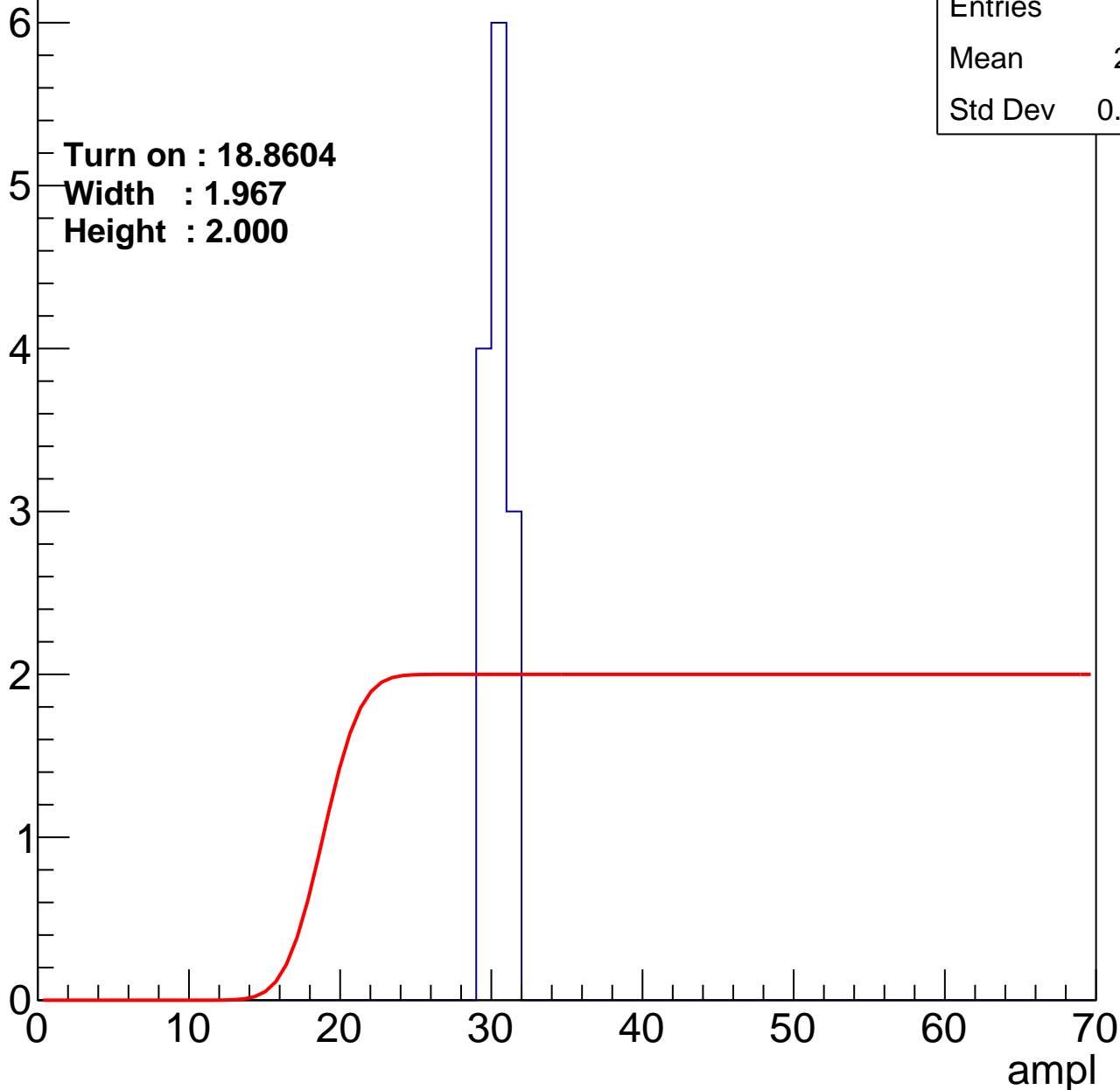
Entry

Entries	13
Mean	29.92
Std Dev	0.7298

Turn on : 18.8604

Width : 1.967

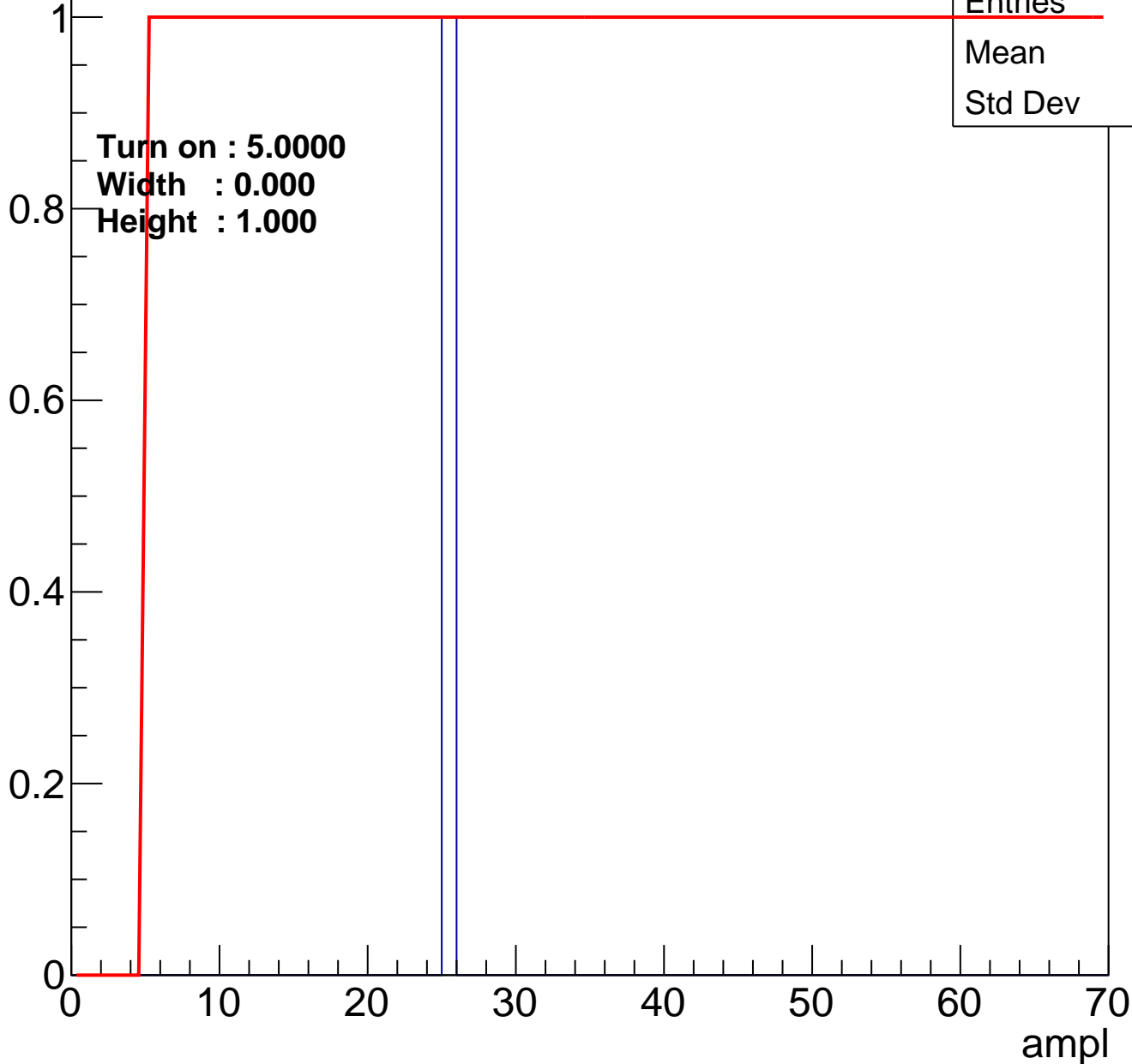
Height : 2.000



B0L100S, U15-ch51

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U15-ch52

calib_packv5_042523_0143.root, FC#6, port A1

Entry

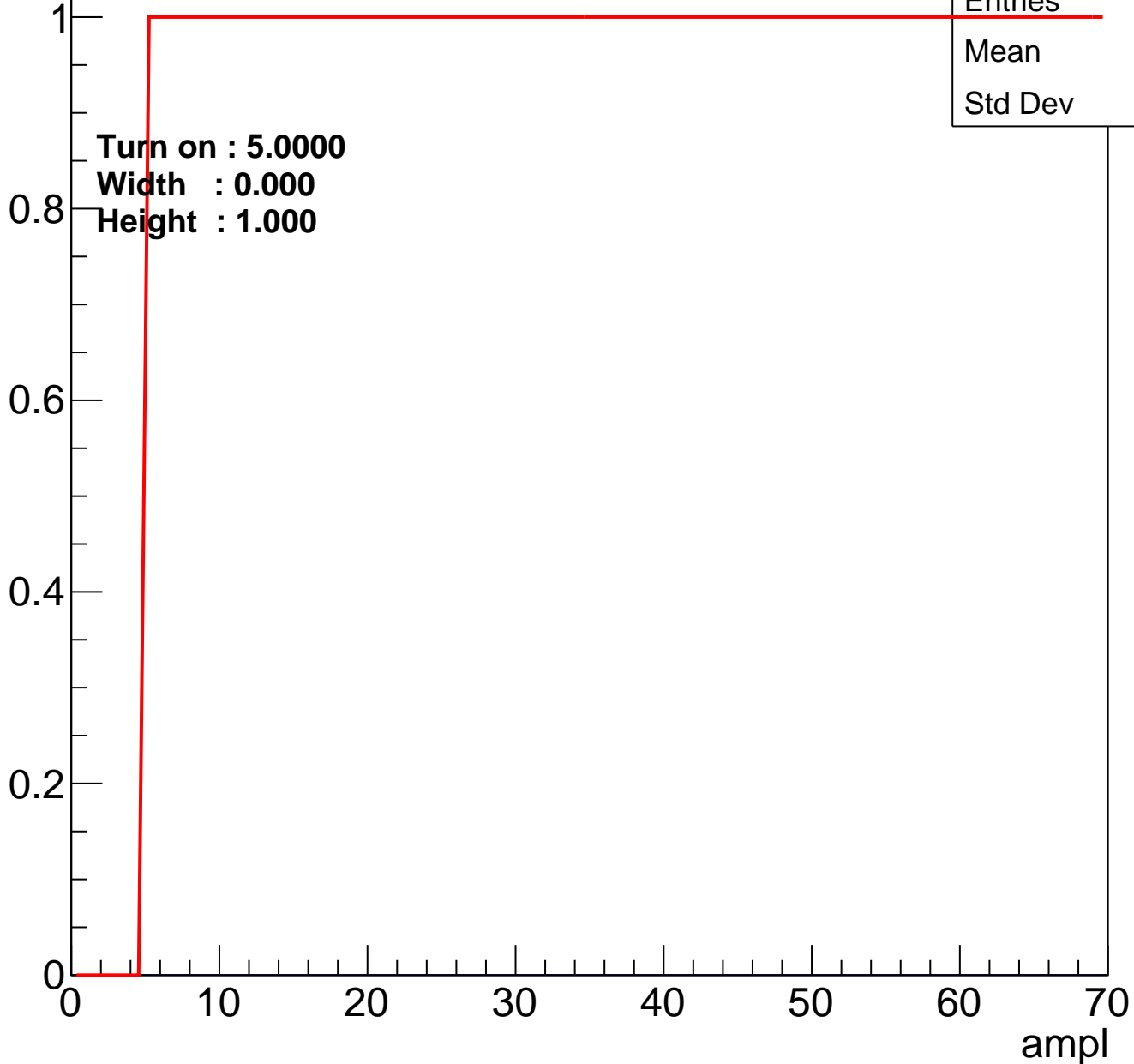


Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch53

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch54

calib_packv5_042523_0143.root, FC#6, port A1

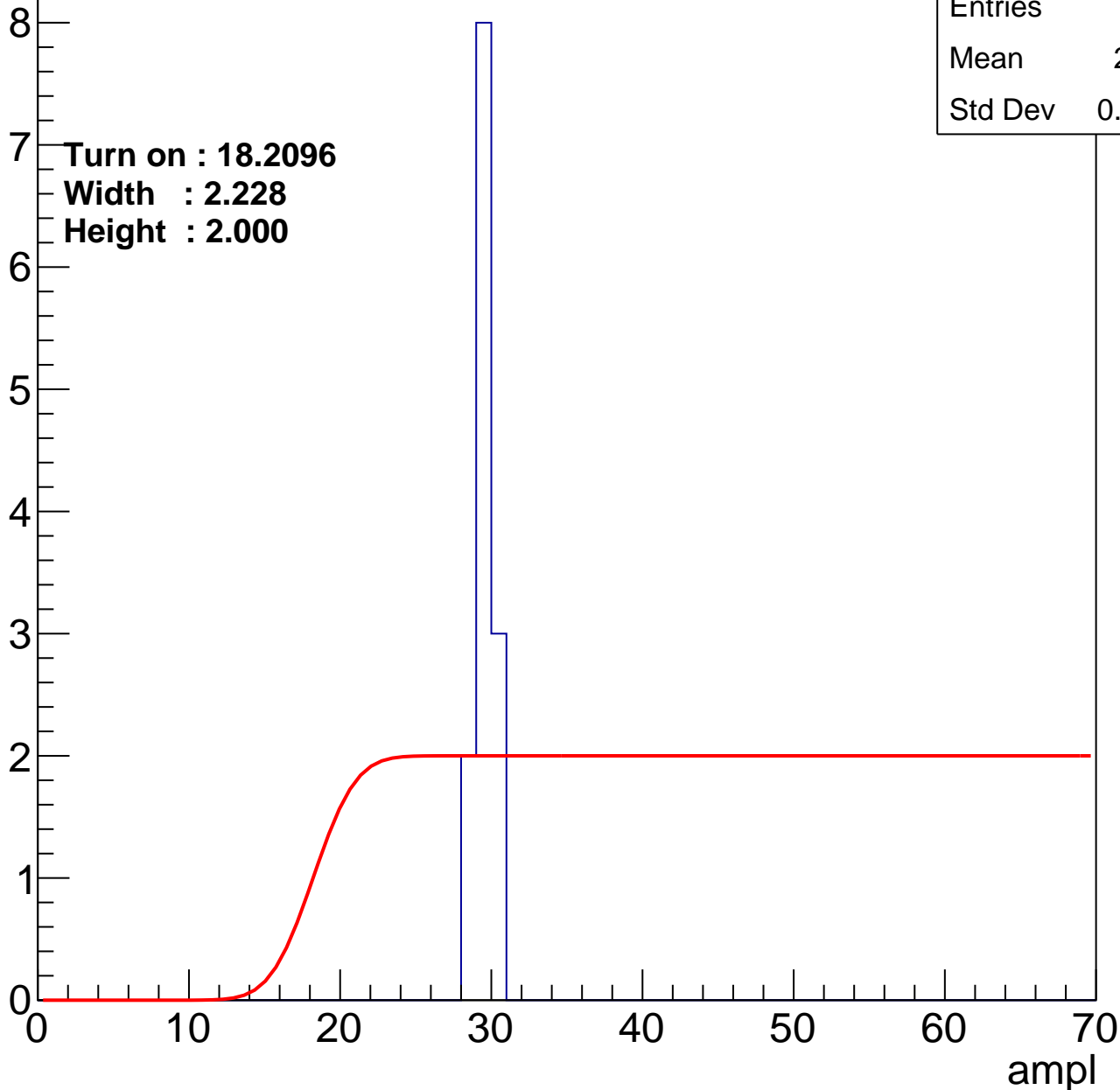
Entry

Entries	13
Mean	29.08
Std Dev	0.6154

Turn on : 18.2096

Width : 2.228

Height : 2.000



B0L100S, U15-ch55

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch56

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch57

calib_packv5_042523_0143.root, FC#6, port A1

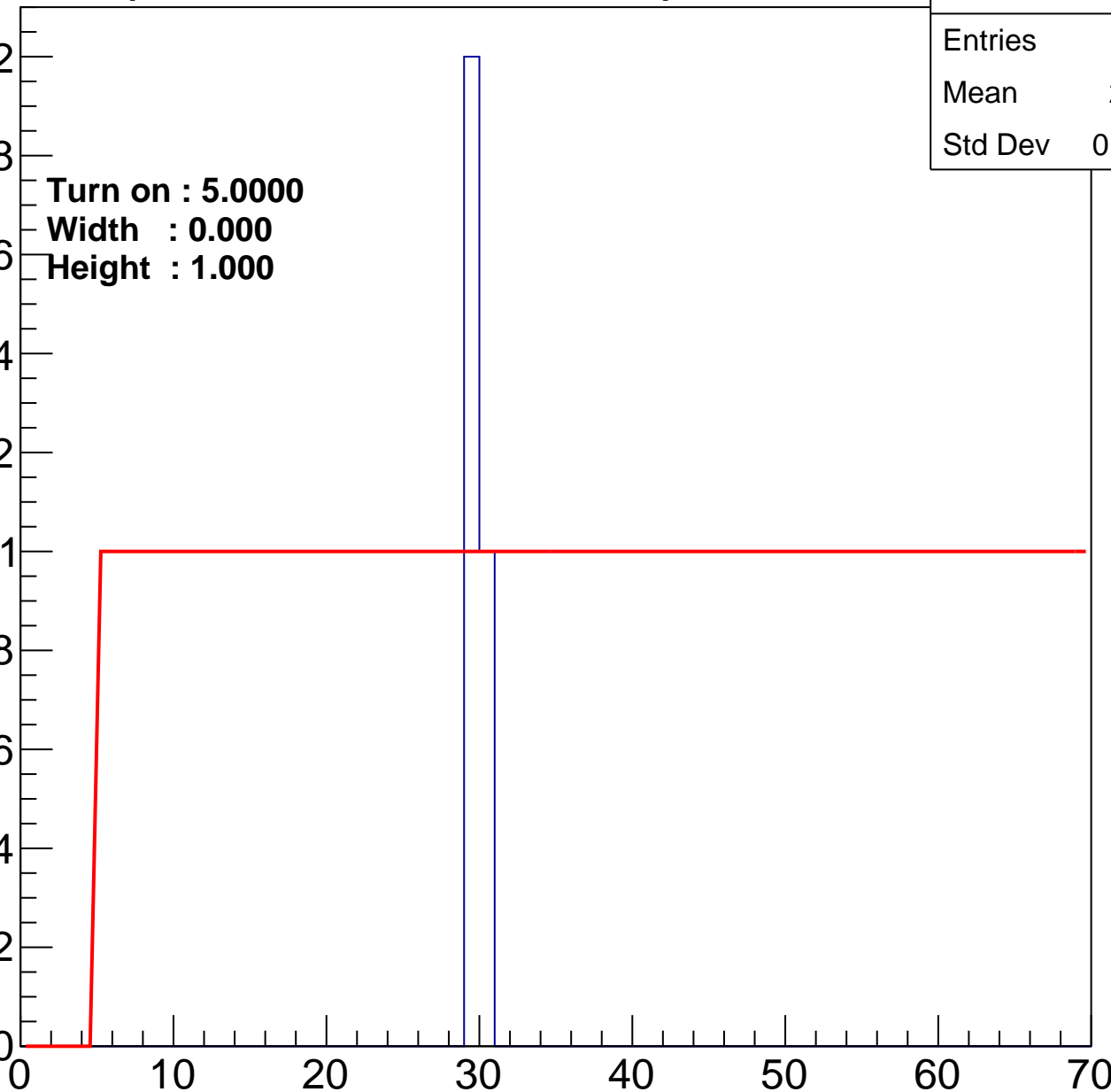
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Turn on : 5.0000
Width : 0.000
Height : 1.000

Entries	3
Mean	29.33
Std Dev	0.4714

ampl



B0L100S, U15-ch58

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch59

calib_packv5_042523_0143.root, FC#6, port A1

Entry

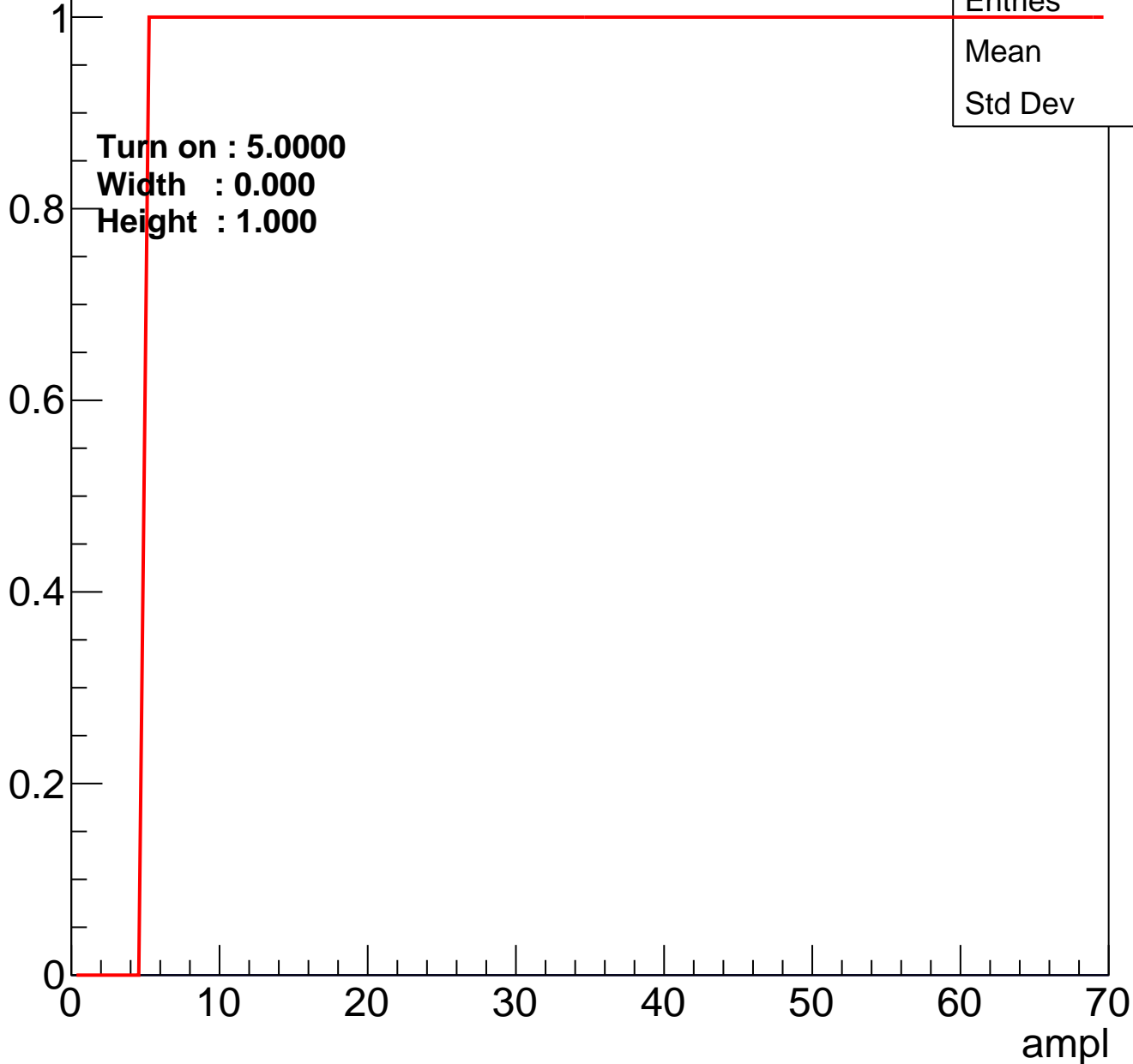


Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch60

calib_packv5_042523_0143.root, FC#6, port A1

Entry

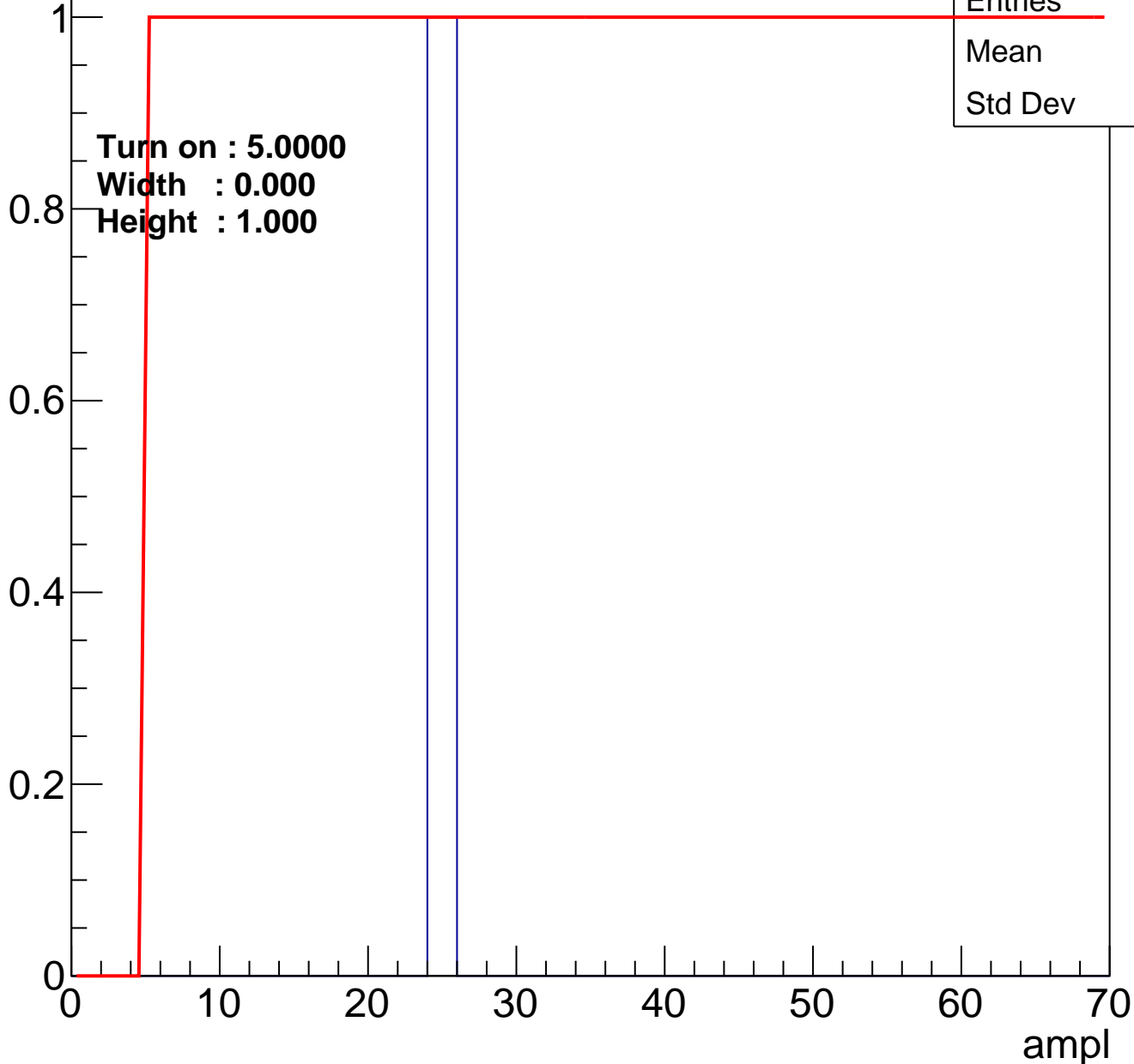


Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch61

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U15-ch62

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch63

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch64

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch65

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch66

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch67

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch68

calib_packv5_042523_0143.root, FC#6, port A1

Entry

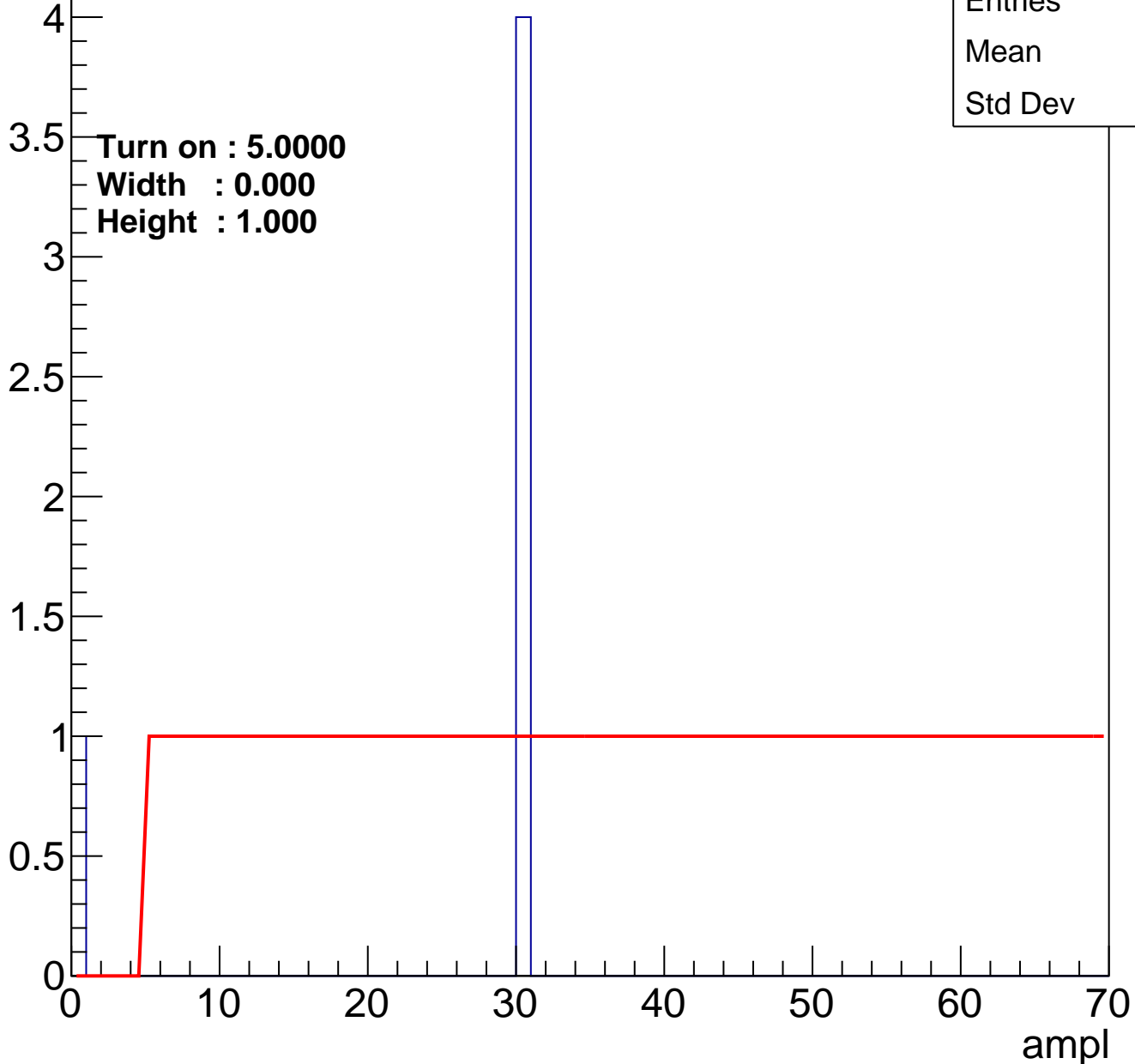


Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch69

calib_packv5_042523_0143.root, FC#6, port A1

Entry



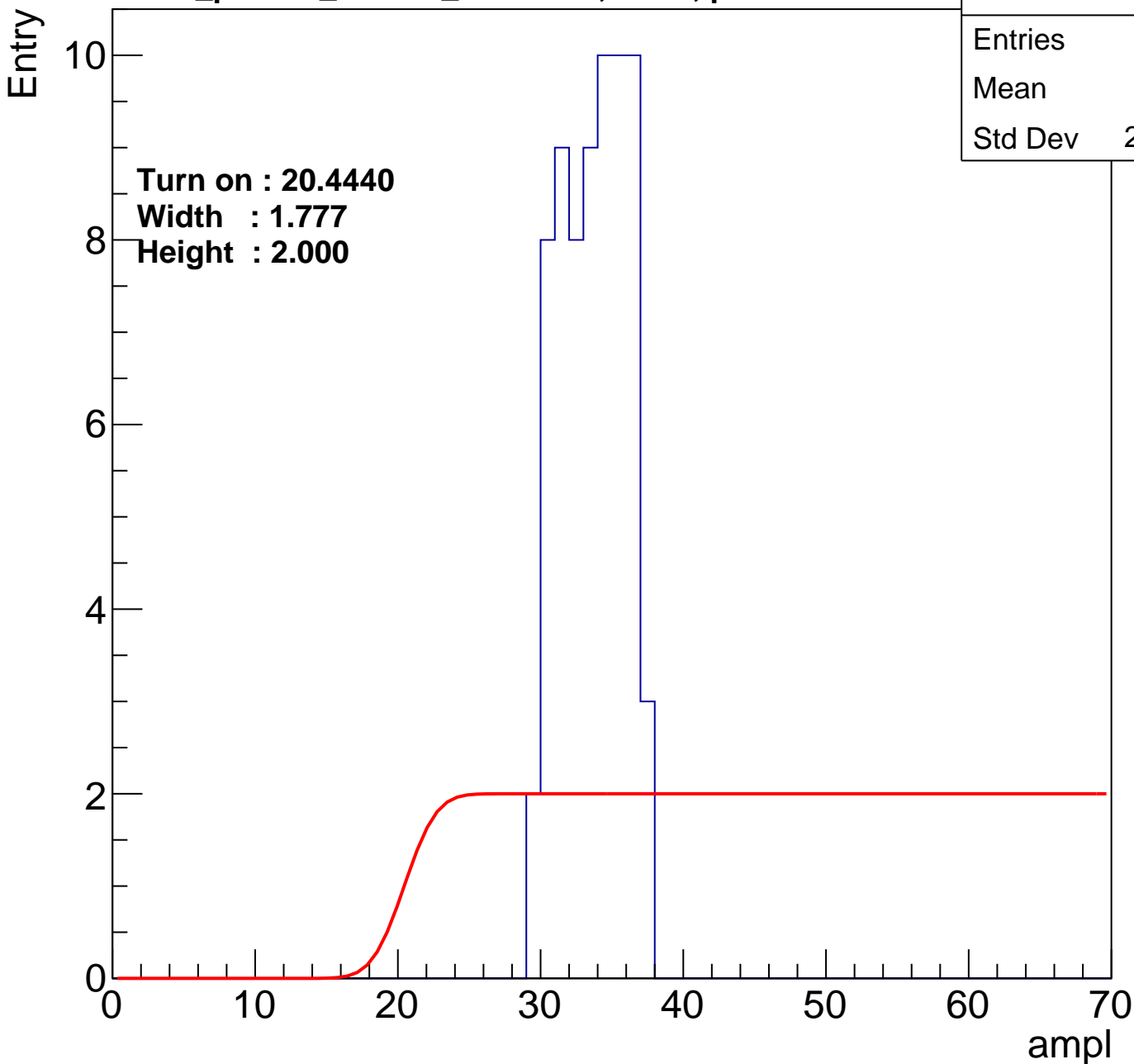
Entries	5
Mean	24
Std Dev	12

B0L100S, U15-ch70

calib_packv5_042523_0143.root, FC#6, port A1

Entries	69
Mean	33.2
Std Dev	2.197

Turn on : 20.4440
Width : 1.777
Height : 2.000



B0L100S, U15-ch71

calib_packv5_042523_0143.root, FC#6, port A1

Entry

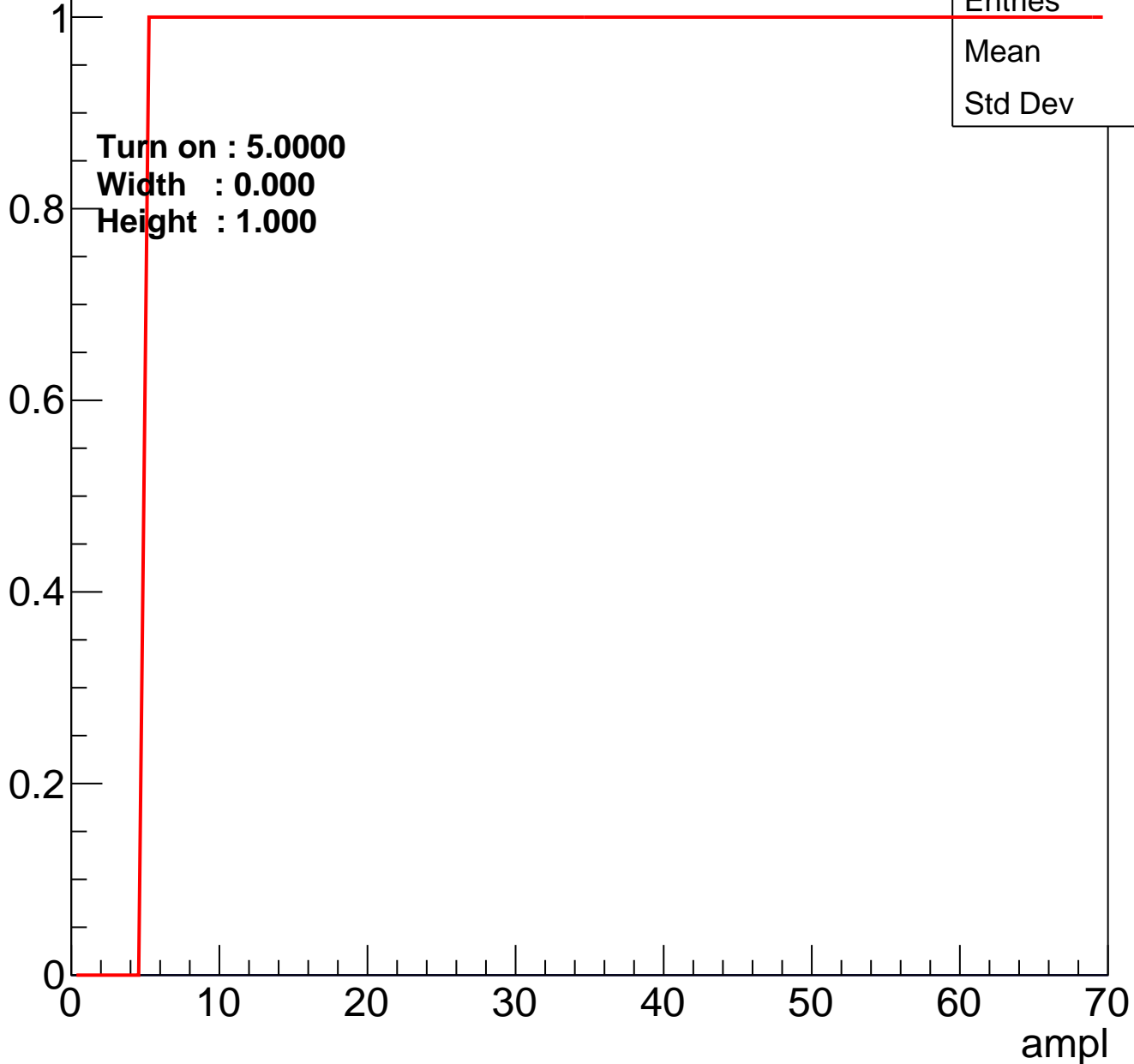


Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch72

calib_packv5_042523_0143.root, FC#6, port A1

Entry

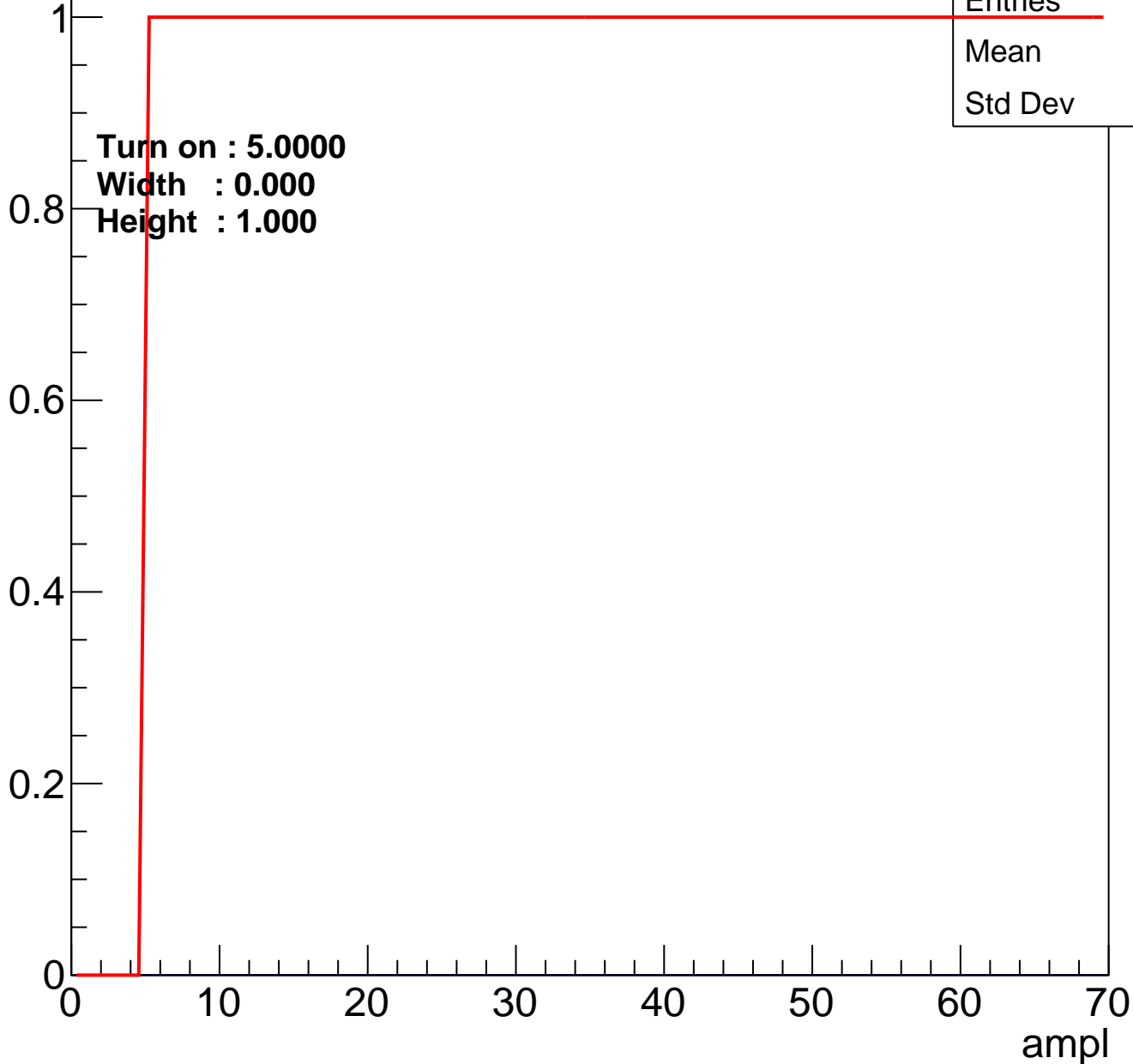


Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch73

calib_packv5_042523_0143.root, FC#6, port A1

Entry

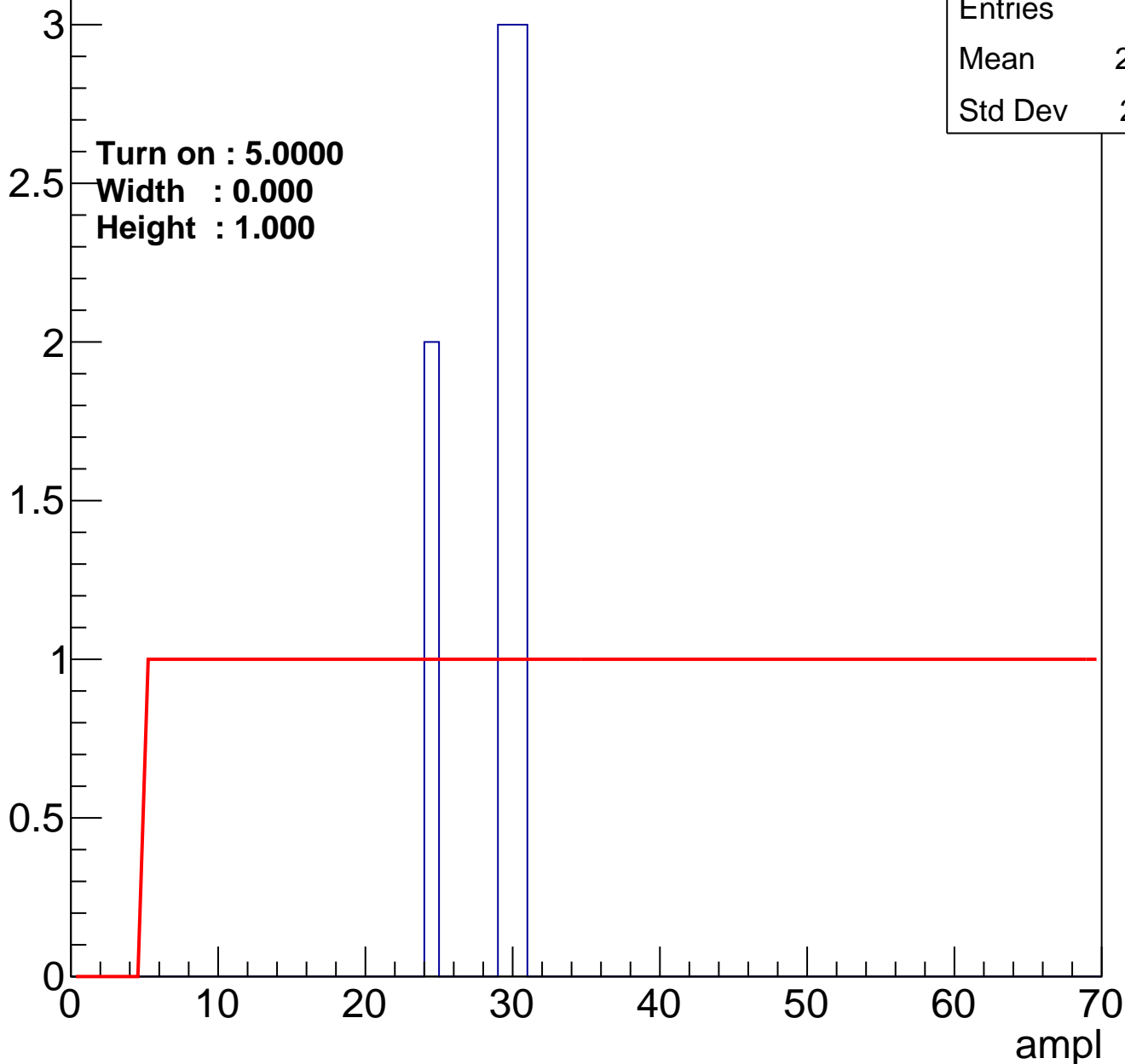


Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch74

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	8
Mean	28.12
Std Dev	2.421

B0L100S, U15-ch75

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch76

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch77

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch78

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch79

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch80

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch81

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U15-ch82

calib_packv5_042523_0143.root, FC#6, port A1

Entry



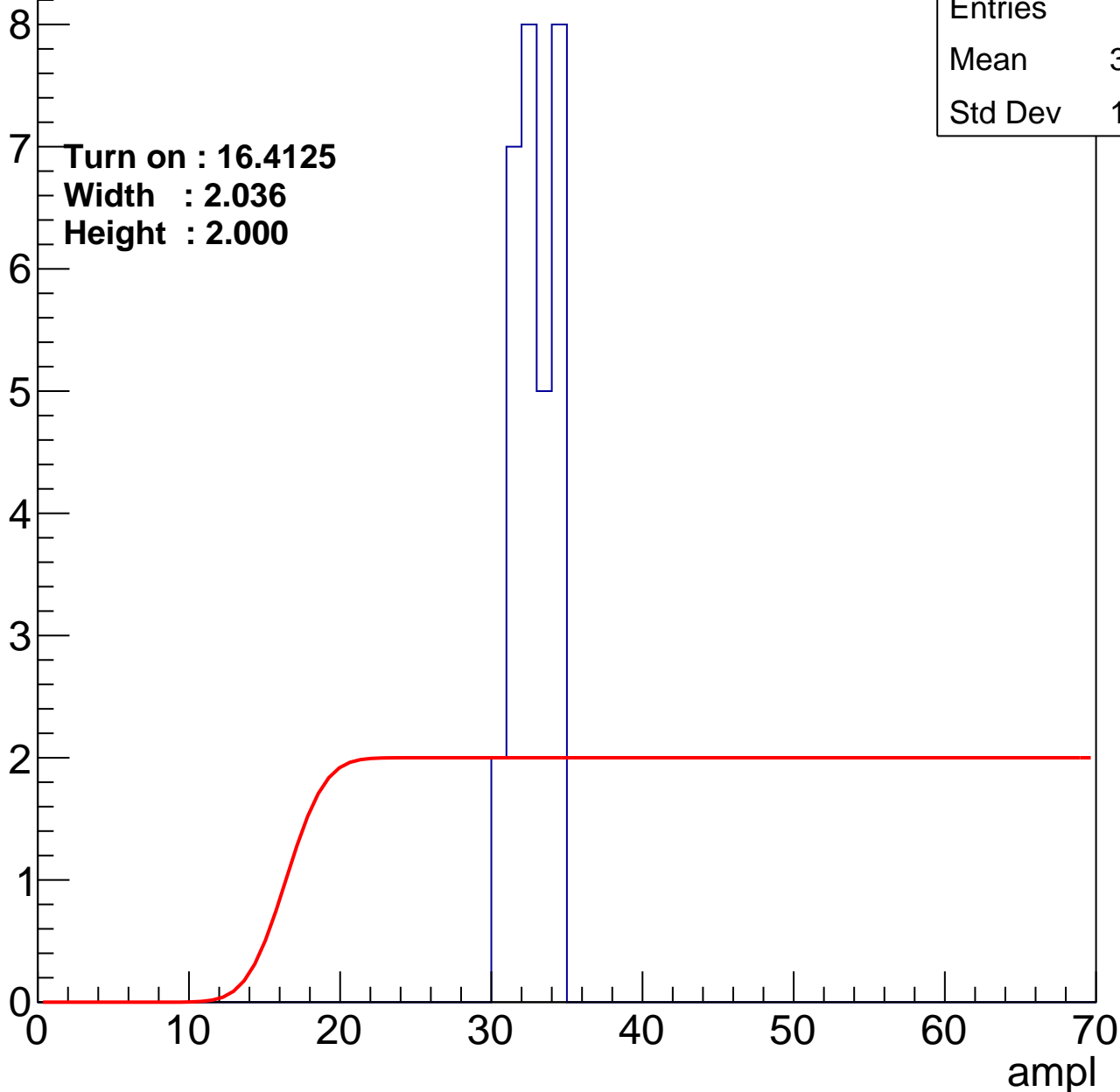
B0L100S, U15-ch83

calib_packv5_042523_0143.root, FC#6, port A1

Entry

Entries	30
Mean	32.33
Std Dev	1.274

Turn on : 16.4125
Width : 2.036
Height : 2.000



B0L100S, U15-ch84

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch85

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch86

calib_packv5_042523_0143.root, FC#6, port A1

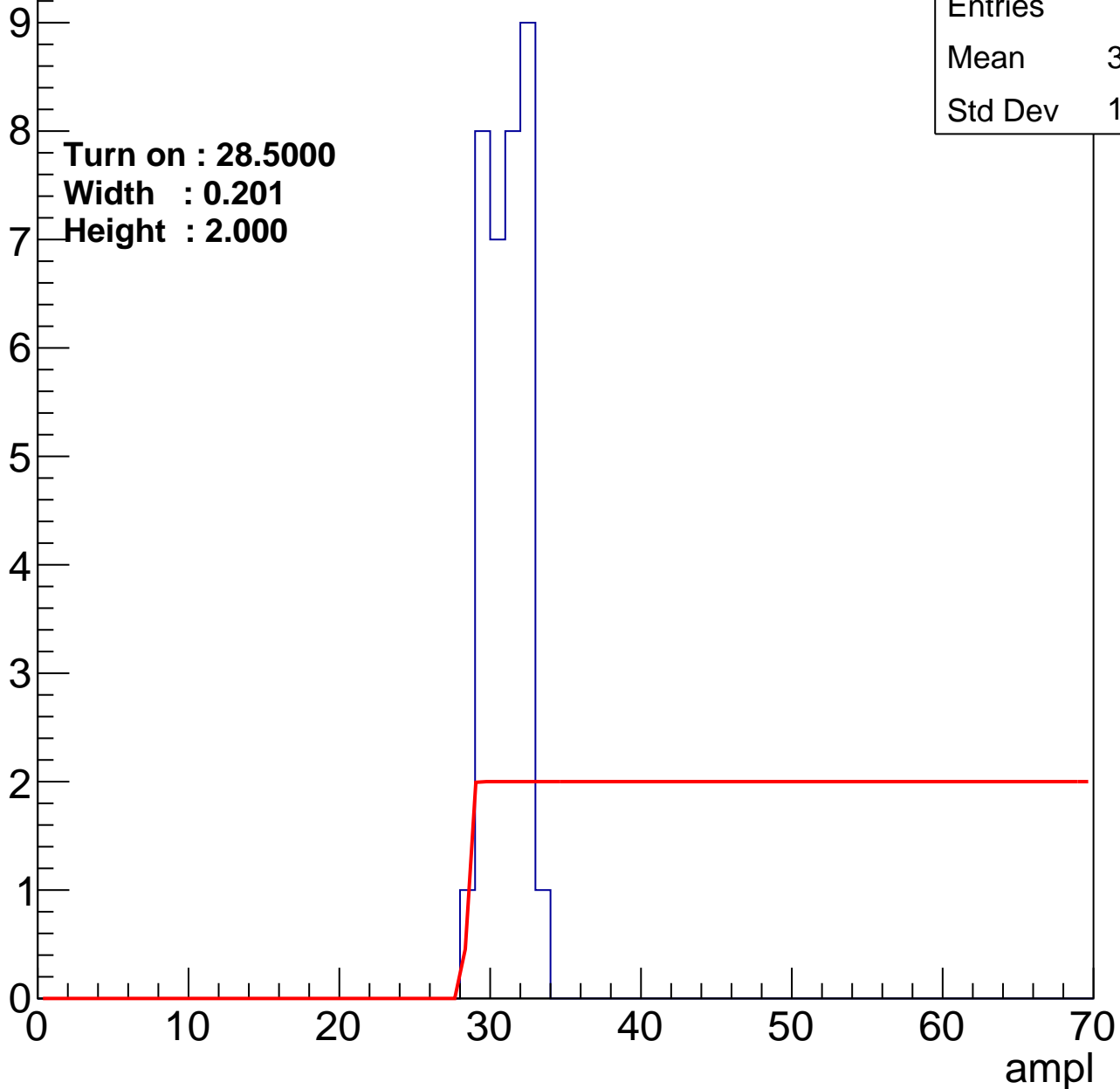
Entry

Entries	34
Mean	30.56
Std Dev	1.265

Turn on : 28.5000

Width : 0.201

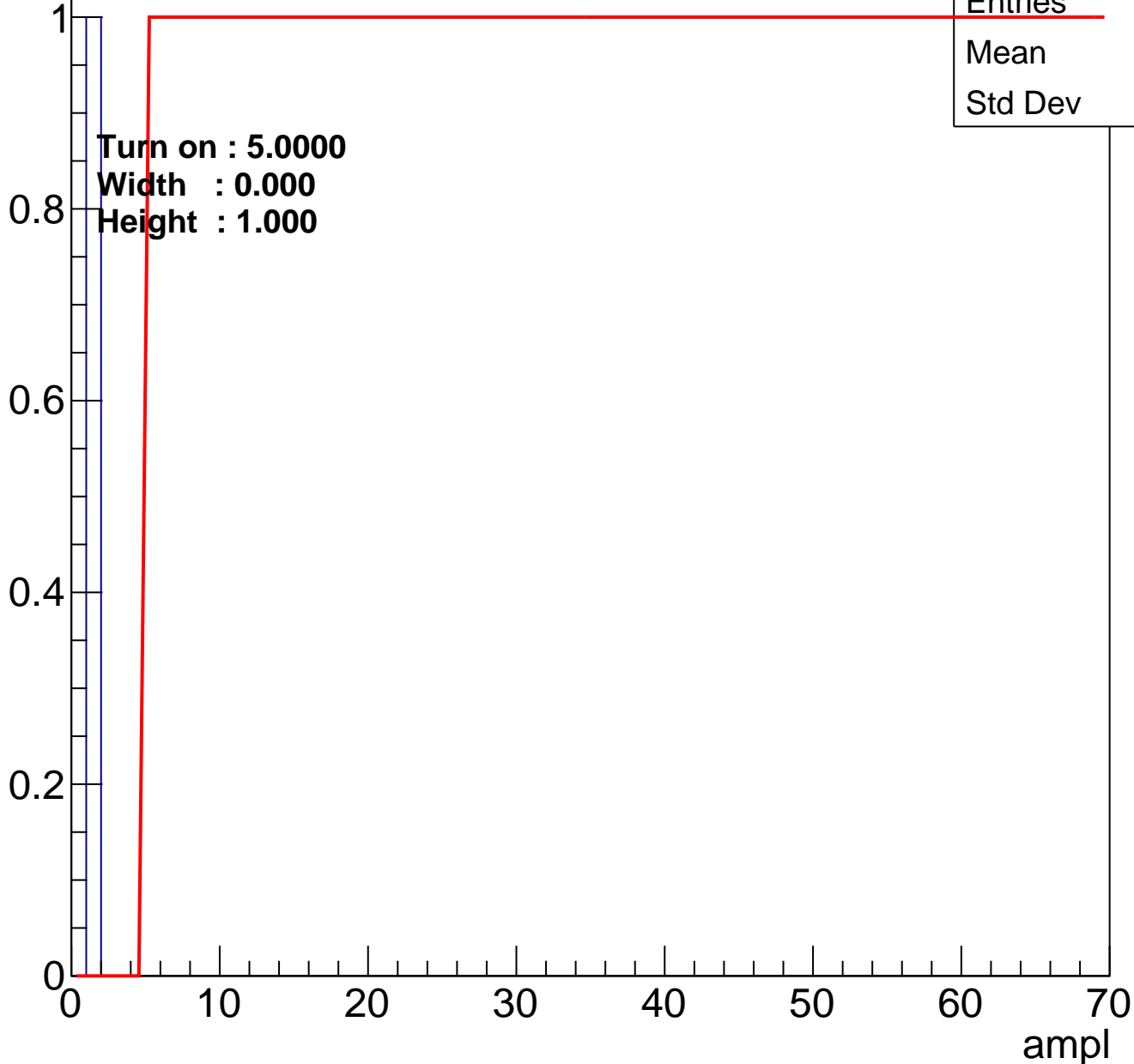
Height : 2.000



B0L100S, U15-ch87

calib_packv5_042523_0143.root, FC#6, port A1

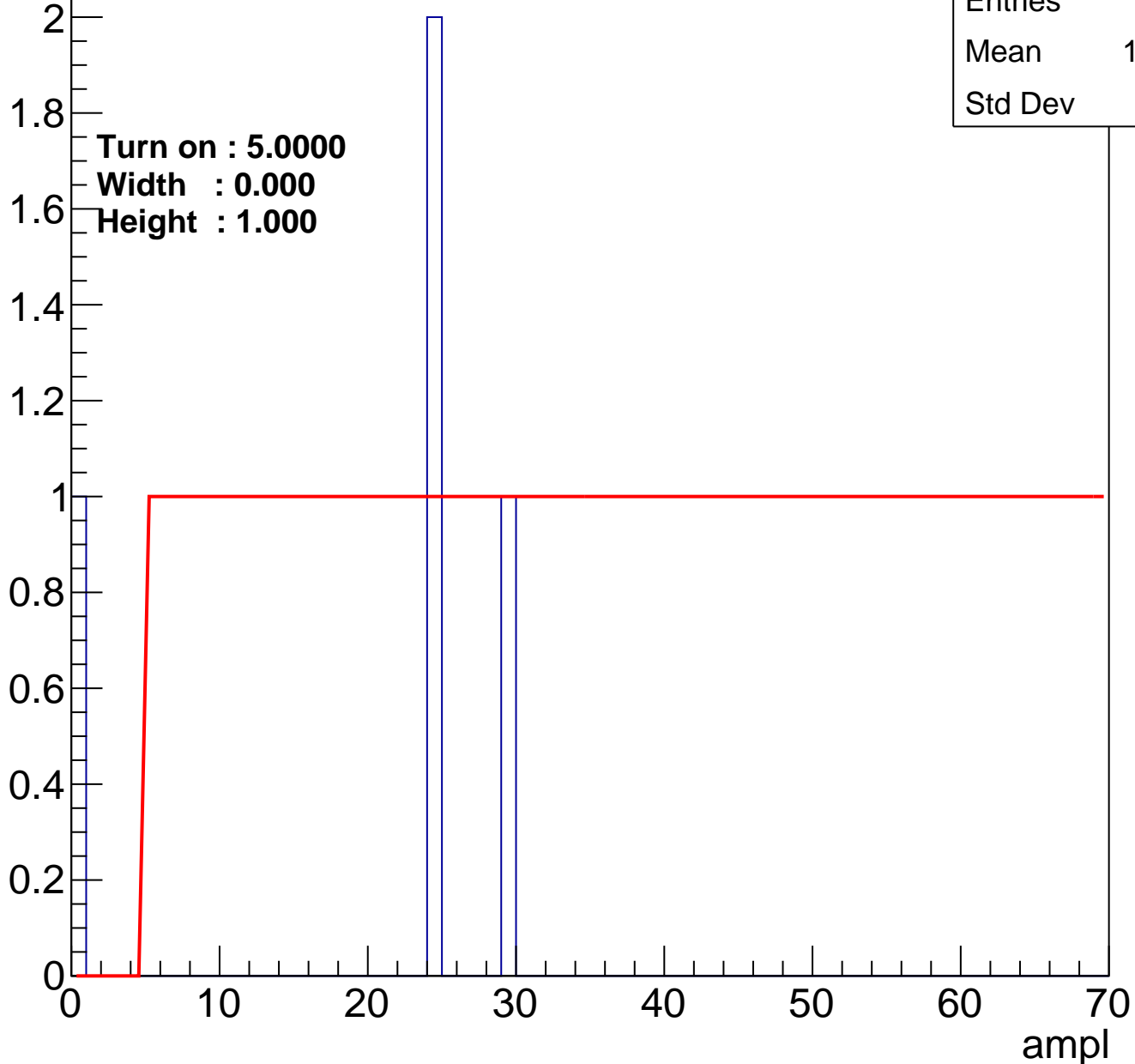
Entry



B0L100S, U15-ch88

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Turn on : 5.0000

Width : 0.000

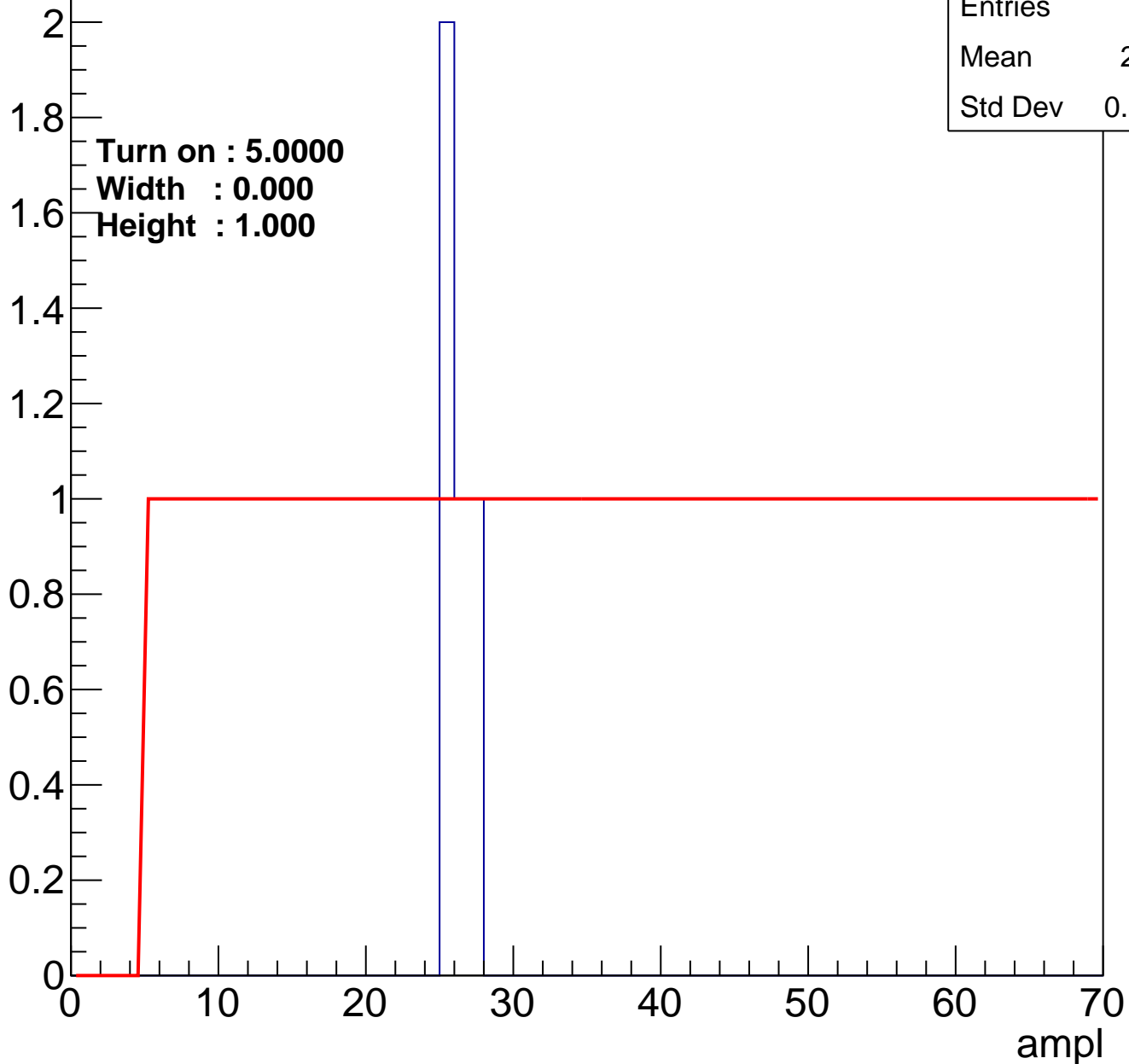
Height : 1.000

Entries	4
Mean	19.25
Std Dev	11.3

B0L100S, U15-ch89

calib_packv5_042523_0143.root, FC#6, port A1

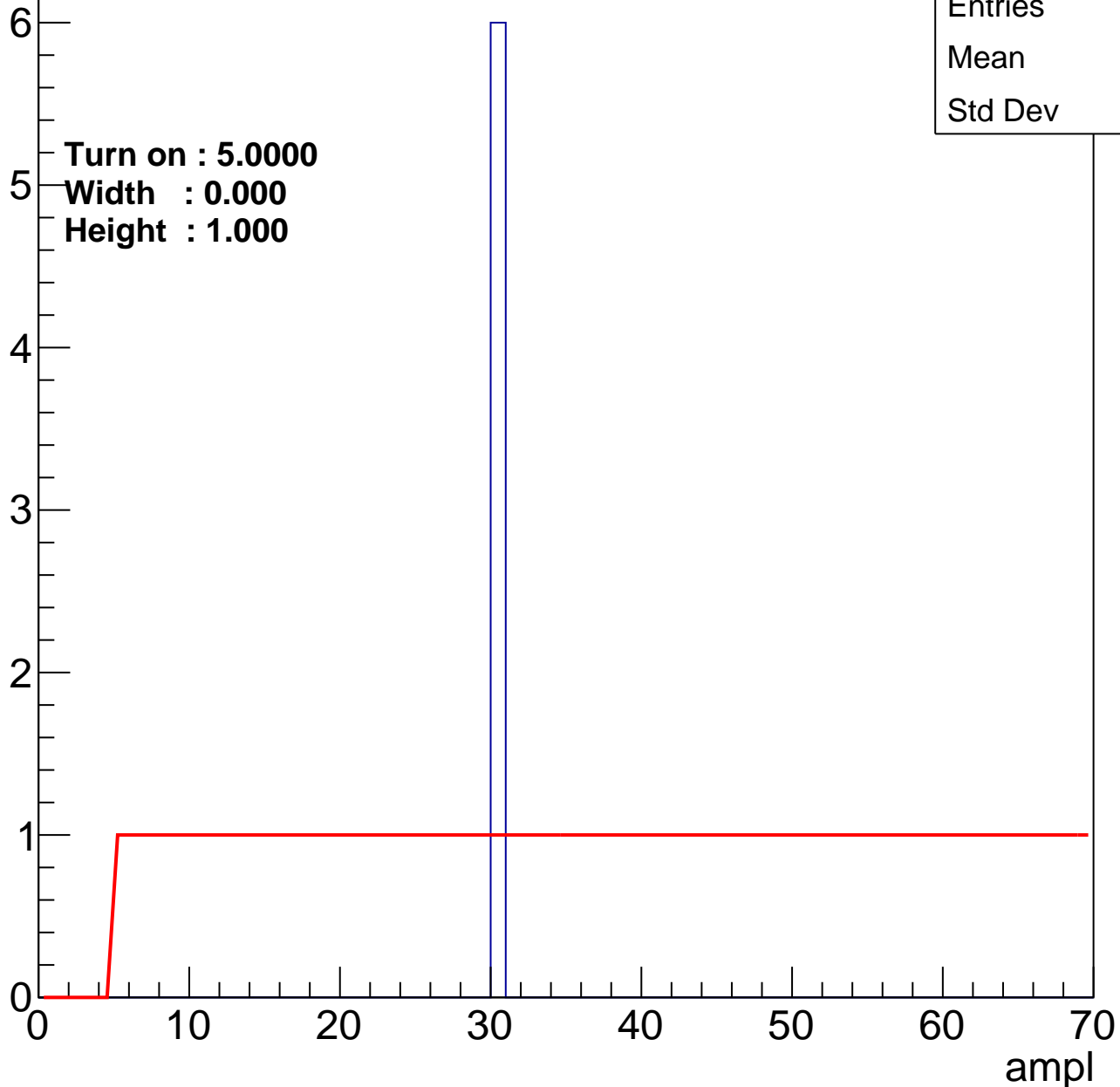
Entry



B0L100S, U15-ch90

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U15-ch91

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch92

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch93

calib_packv5_042523_0143.root, FC#6, port A1

Entry

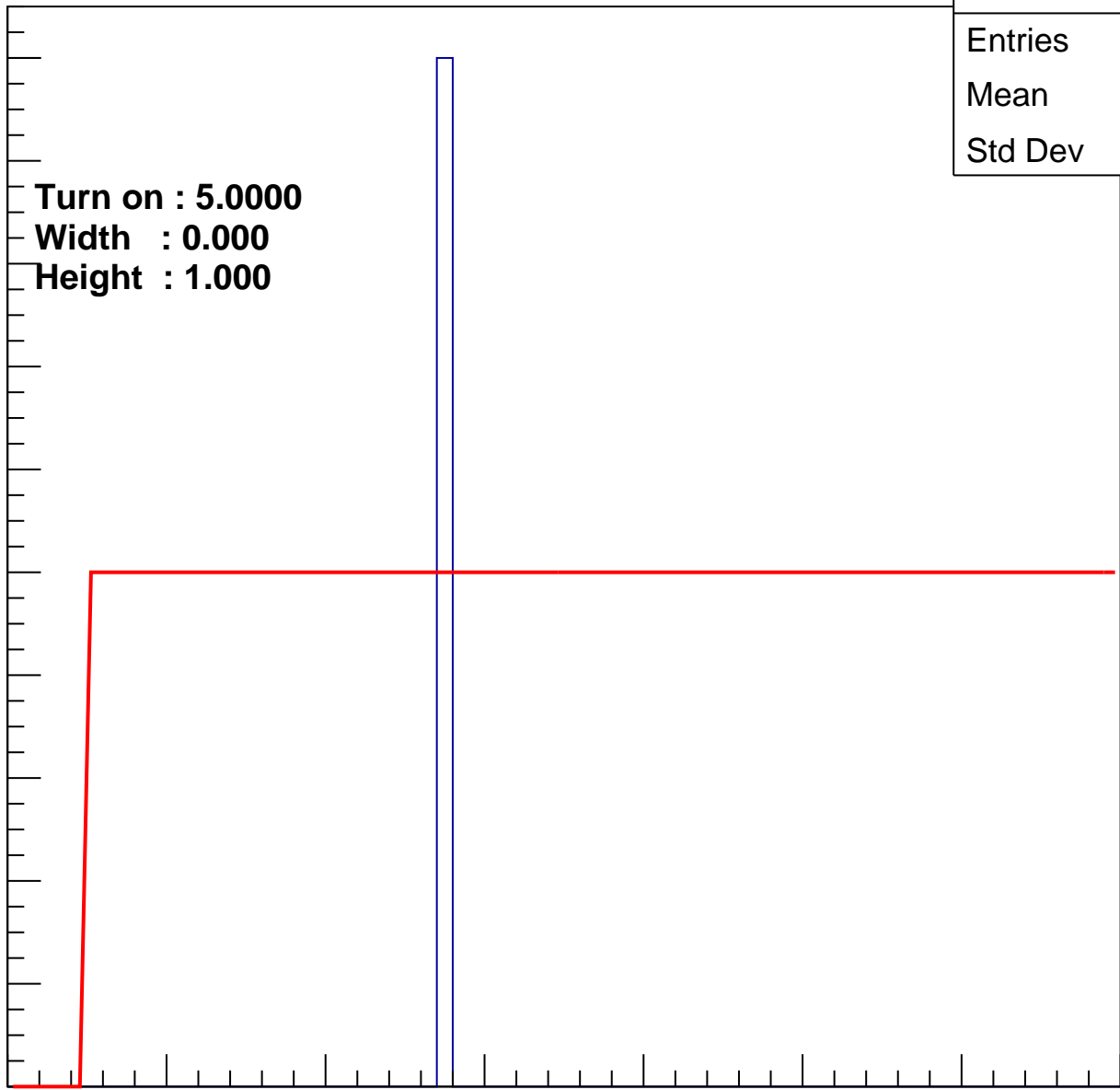
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Turn on : 5.0000
Width : 0.000
Height : 1.000

Entries	2
Mean	27
Std Dev	0

0 10 20 30 40 50 60 70

ampl



B0L100S, U15-ch94

calib_packv5_042523_0143.root, FC#6, port A1

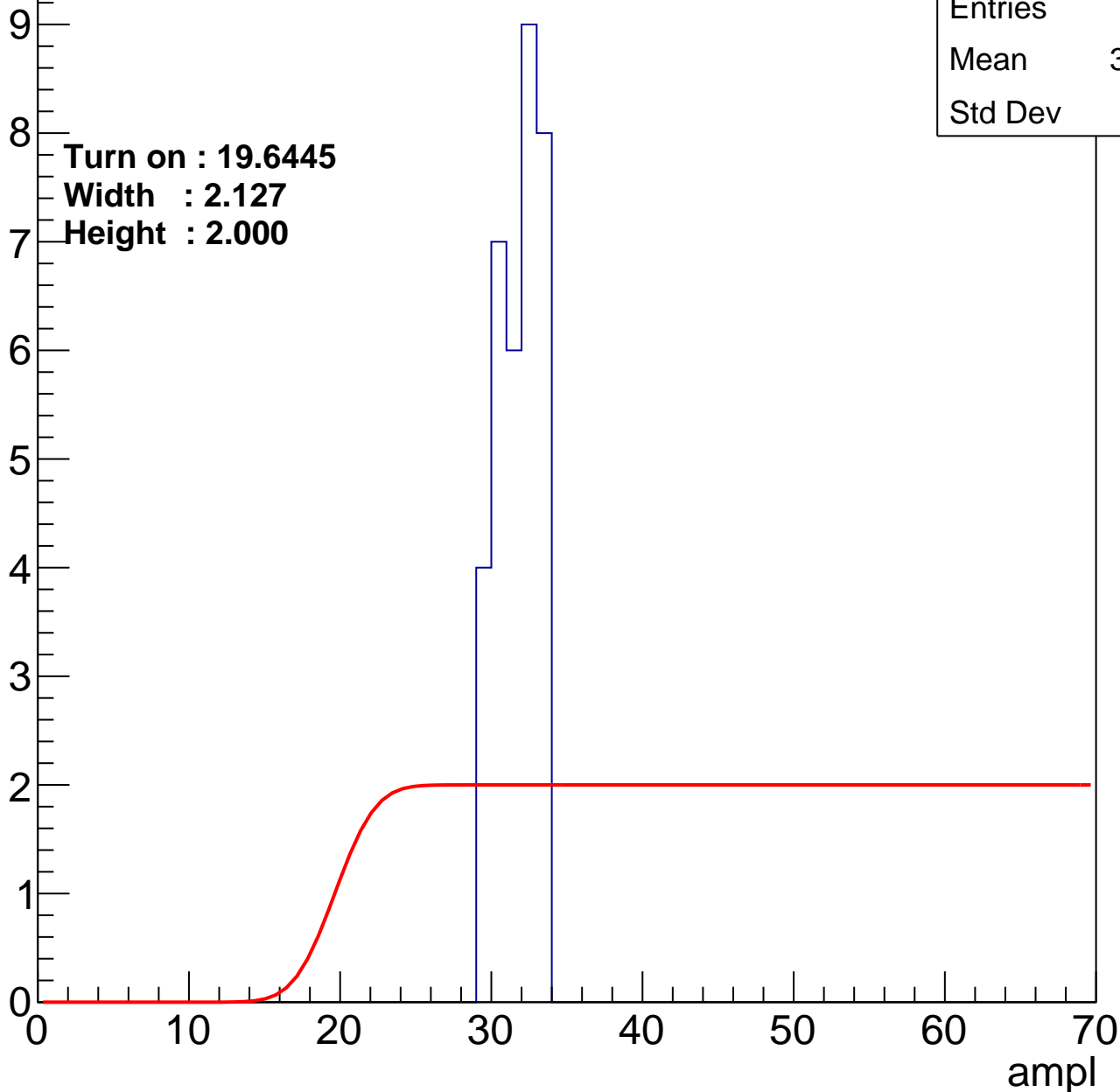
Entry

Entries	34
Mean	31.29
Std Dev	1.34

Turn on : 19.6445

Width : 2.127

Height : 2.000



B0L100S, U15-ch95

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

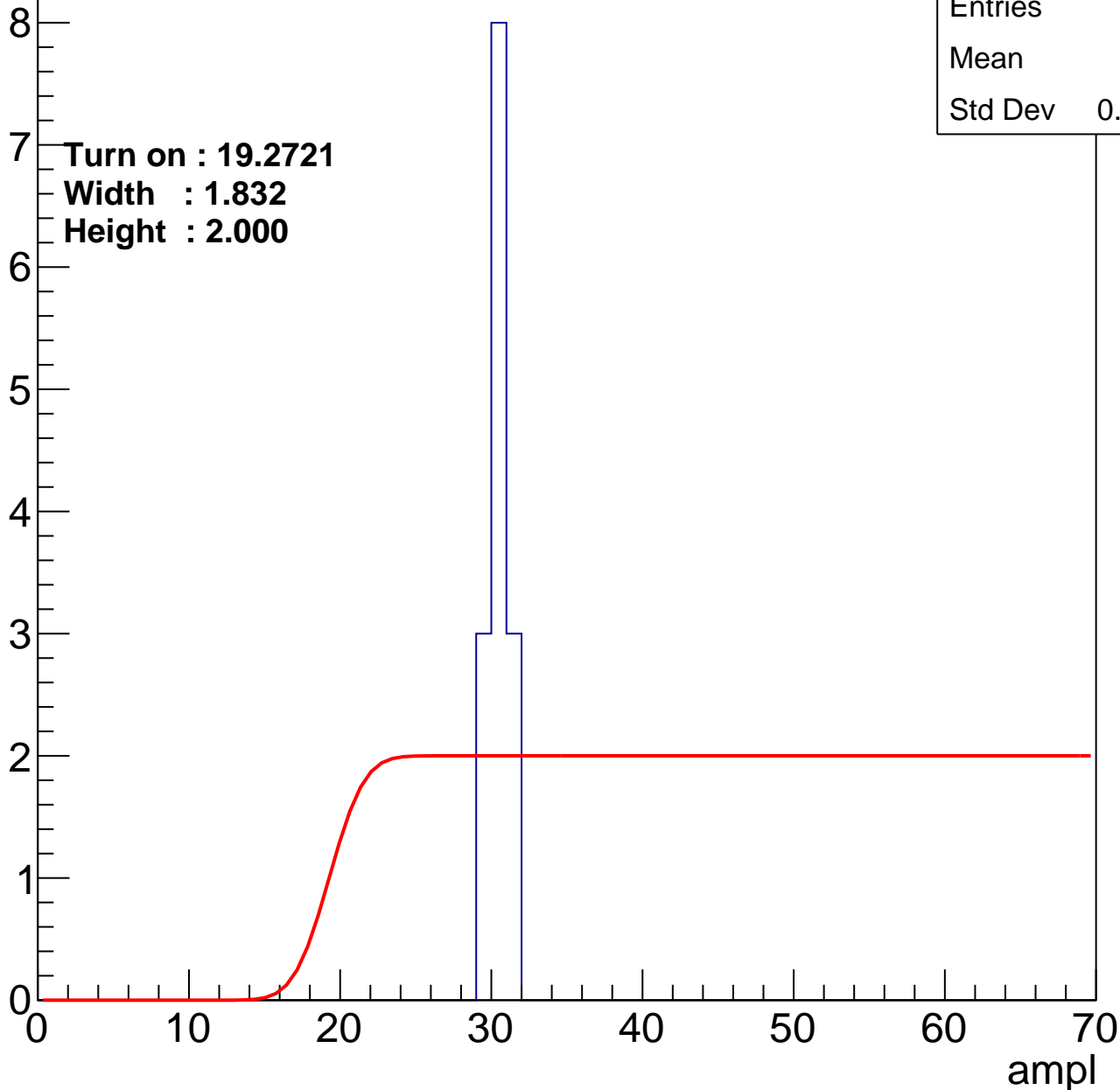
B0L100S, U15-ch96

calib_packv5_042523_0143.root, FC#6, port A1

Entry

Entries	14
Mean	30
Std Dev	0.6547

Turn on : 19.2721
Width : 1.832
Height : 2.000



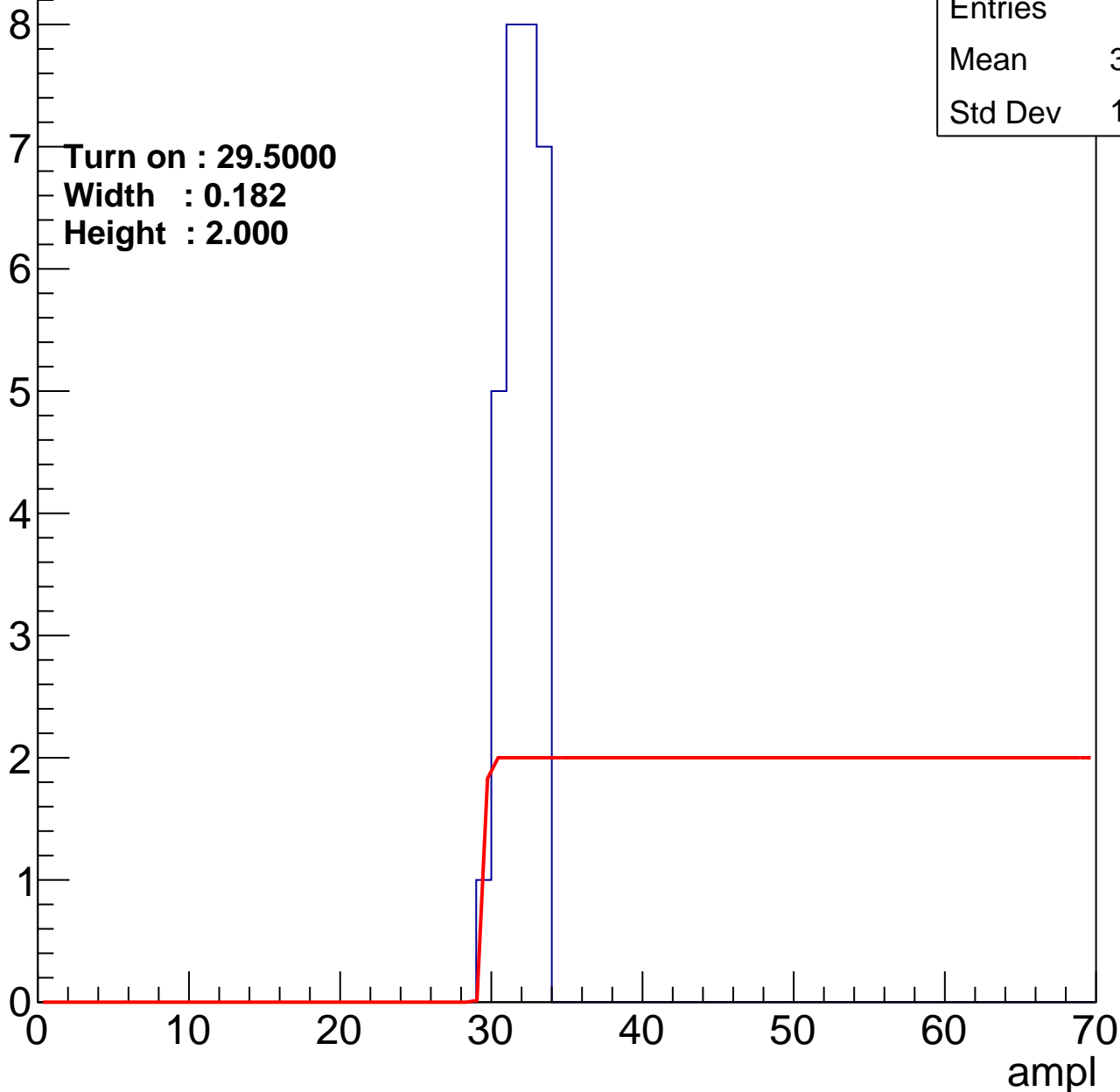
B0L100S, U15-ch97

calib_packv5_042523_0143.root, FC#6, port A1

Entry

Entries	29
Mean	31.52
Std Dev	1.133

Turn on : 29.5000
Width : 0.182
Height : 2.000



B0L100S, U15-ch98

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U15-ch99

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	2
Mean	0
Std Dev	0

B0L100S, U15-ch100

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch101

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch102

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch103

calib_packv5_042523_0143.root, FC#6, port A1

Entry



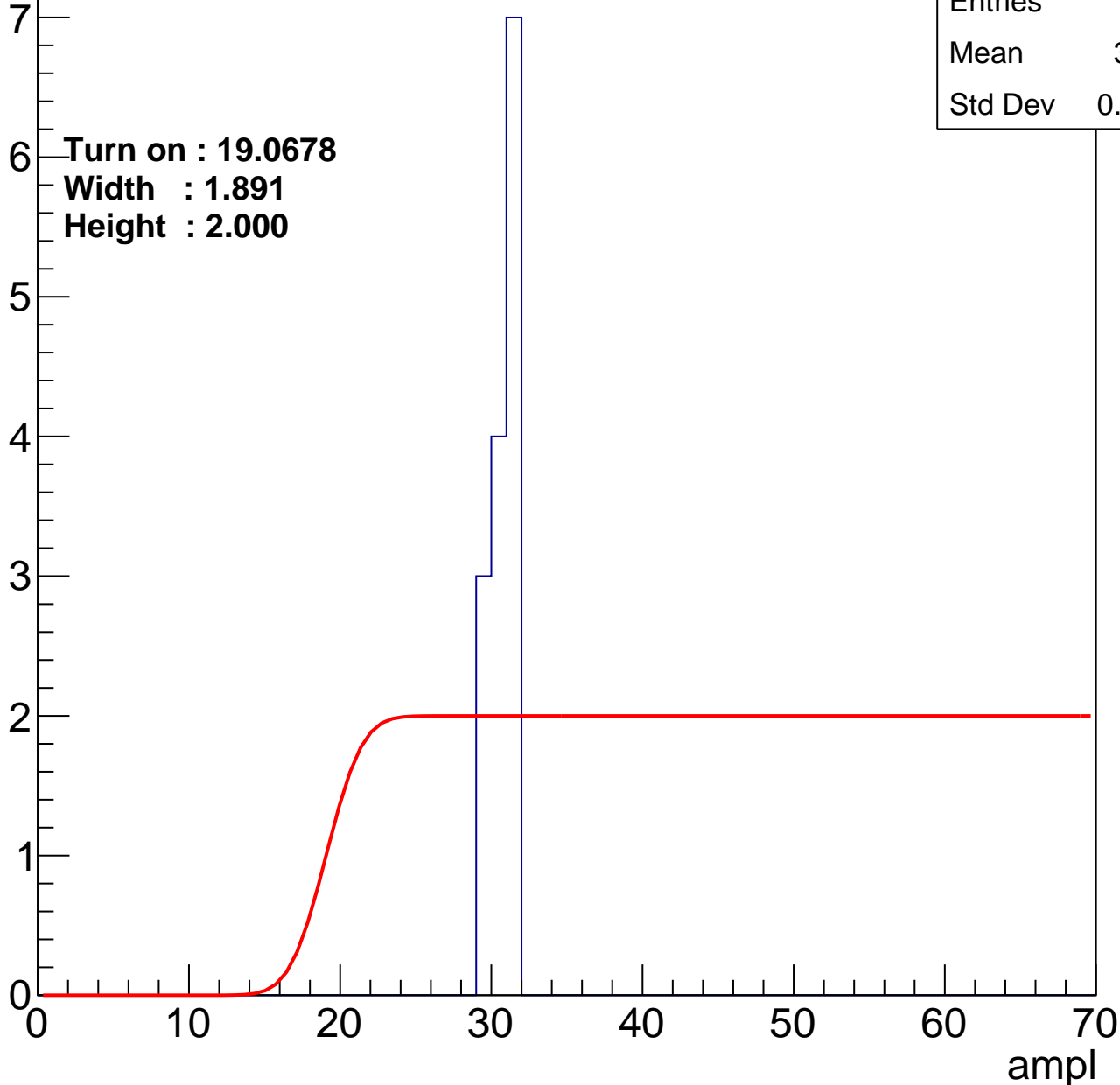
B0L100S, U15-ch104

calib_packv5_042523_0143.root, FC#6, port A1

Entry

Entries	14
Mean	30.29
Std Dev	0.7954

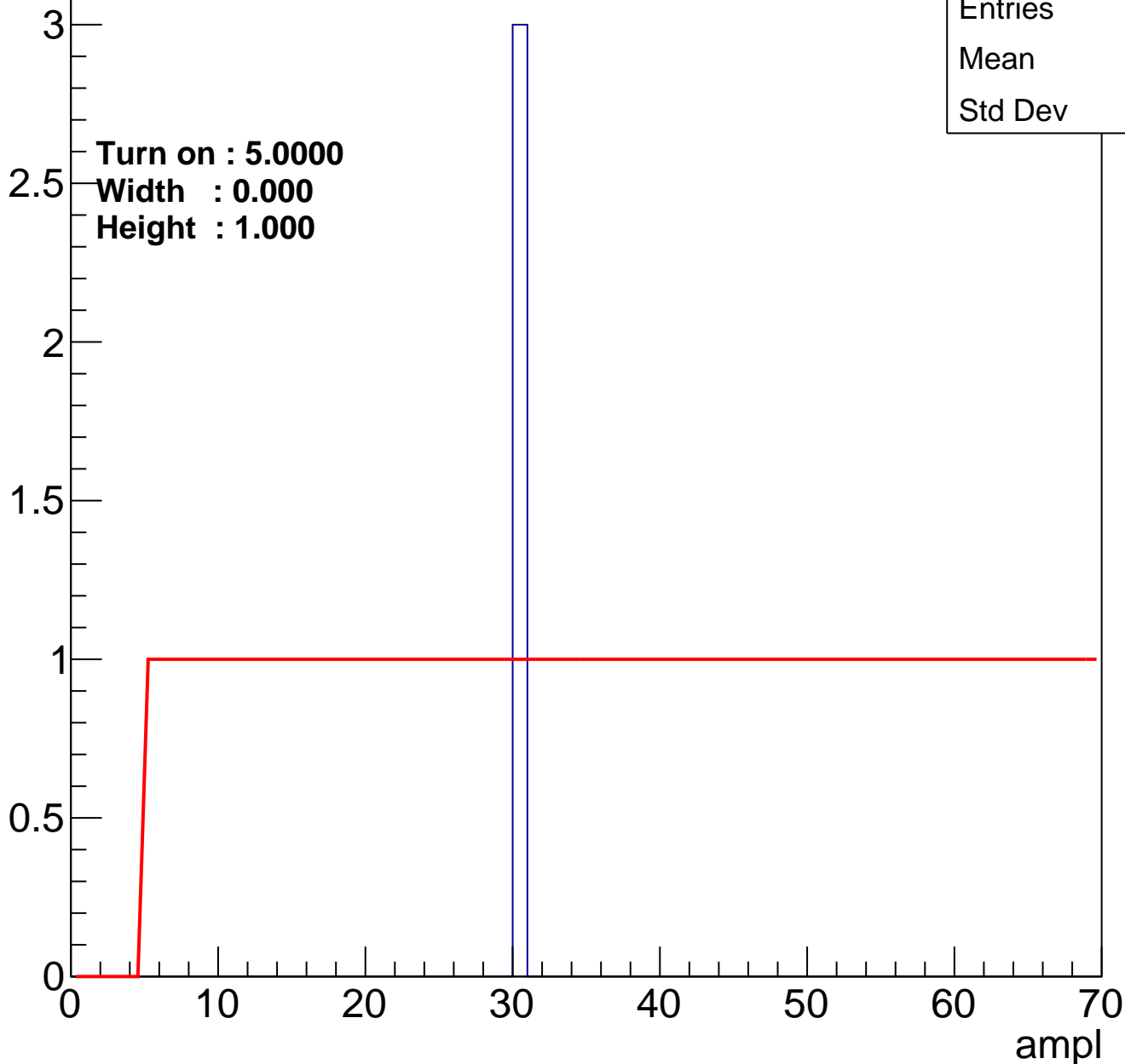
Turn on : 19.0678
Width : 1.891
Height : 2.000



B0L100S, U15-ch105

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U15-ch106

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U15-ch107

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U15-ch108

calib_packv5_042523_0143.root, FC#6, port A1

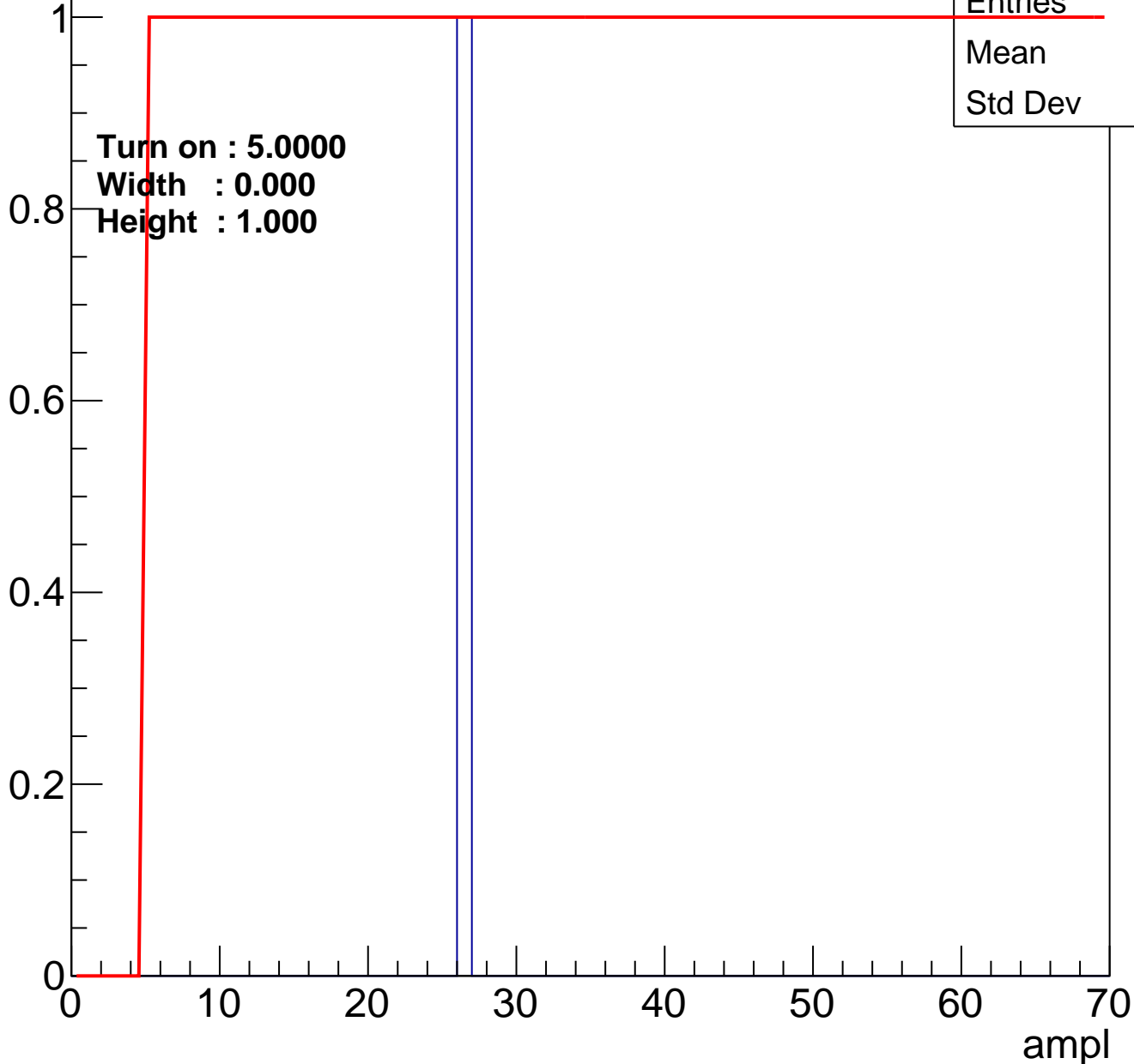
Entry



B0L100S, U15-ch109

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U15-ch110

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch111

calib_packv5_042523_0143.root, FC#6, port A1

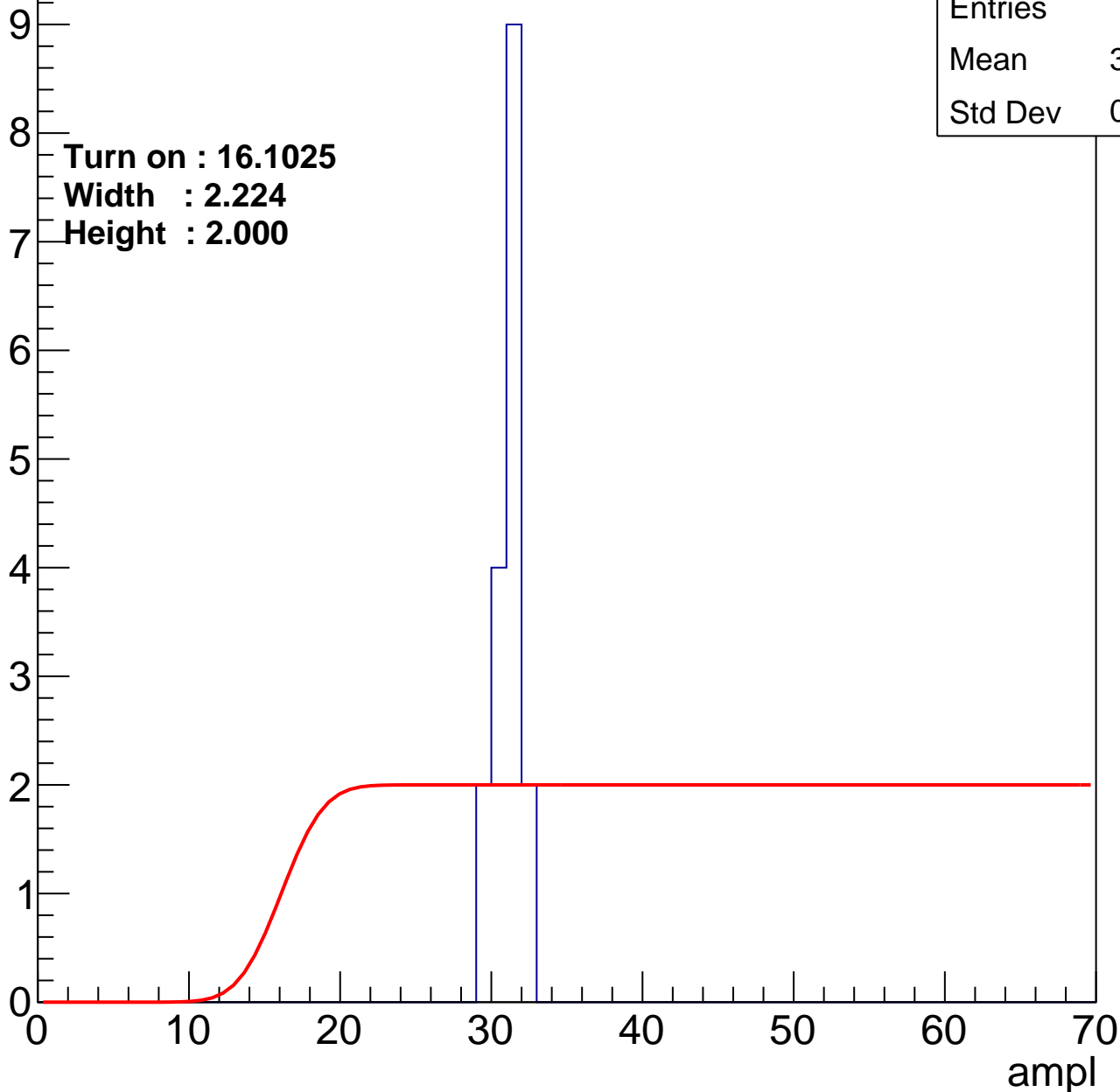
Entry

Entries	17
Mean	30.65
Std Dev	0.836

Turn on : 16.1025

Width : 2.224

Height : 2.000



B0L100S, U15-ch112

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U15-ch113

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U15-ch114

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch115

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U15-ch116

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	1
Mean	0
Std Dev	0

B0L100S, U15-ch117

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch118

calib_packv5_042523_0143.root, FC#6, port A1

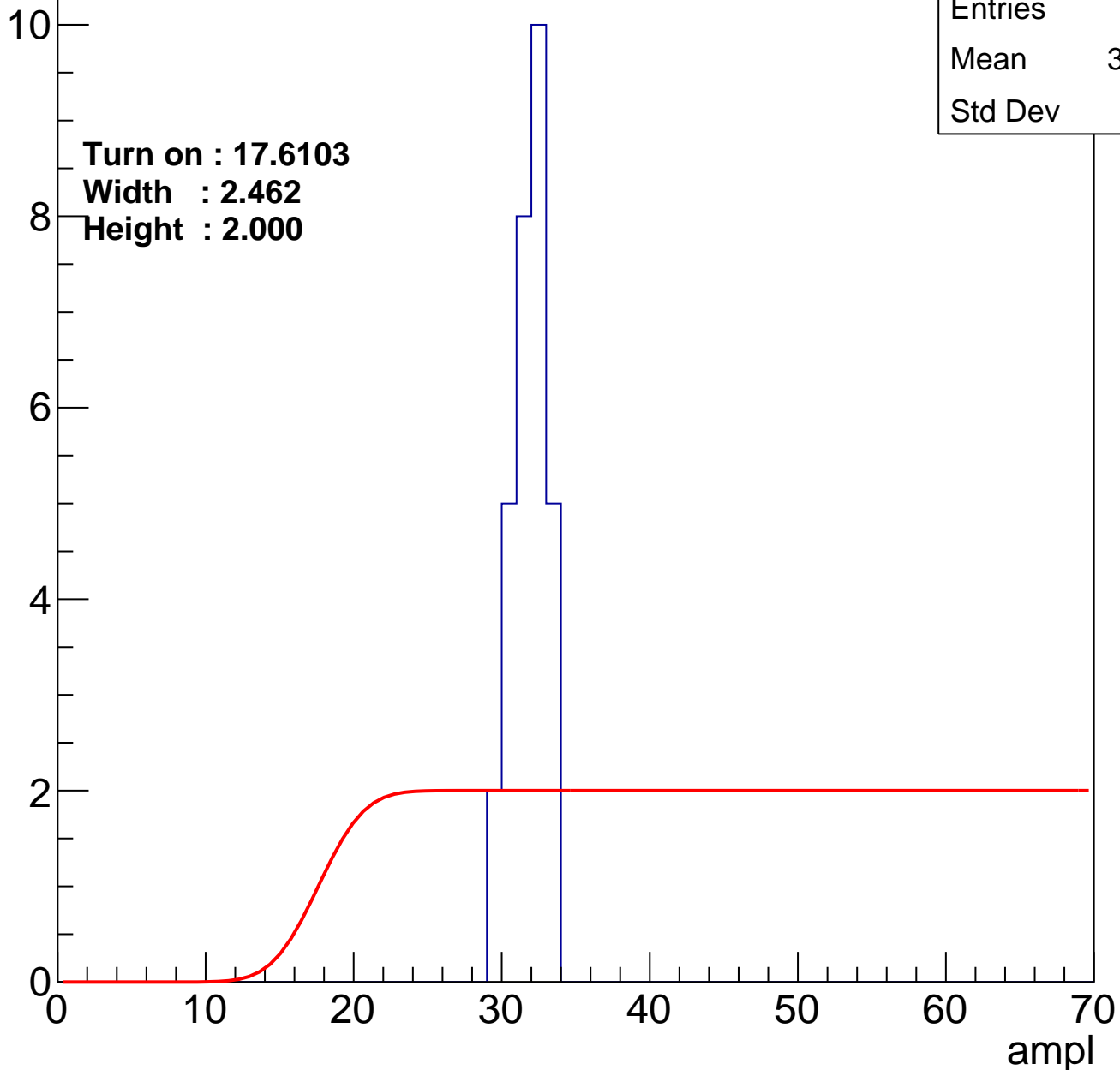
Entries	30
Mean	31.37
Std Dev	1.14

Turn on : 17.6103

Width : 2.462

Height : 2.000

Entry



B0L100S, U15-ch119

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U15-ch120

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch121

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U15-ch122

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch123

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch124

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U15-ch125

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch126

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch127

calib_packv5_042523_0143.root, FC#6, port A1

Entry

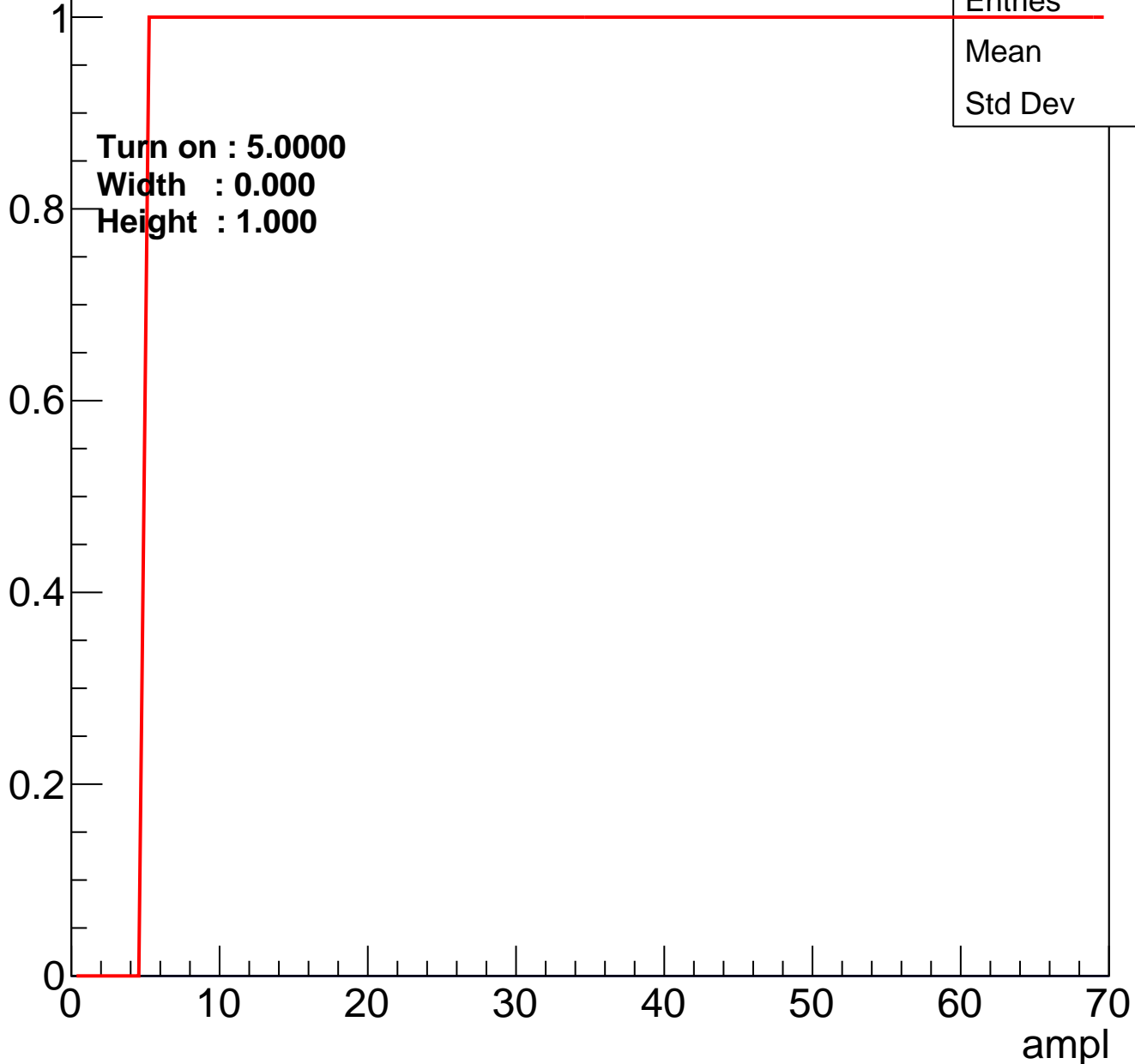


Entries	0
Mean	0
Std Dev	0

B0L100S, U15-ch127

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0