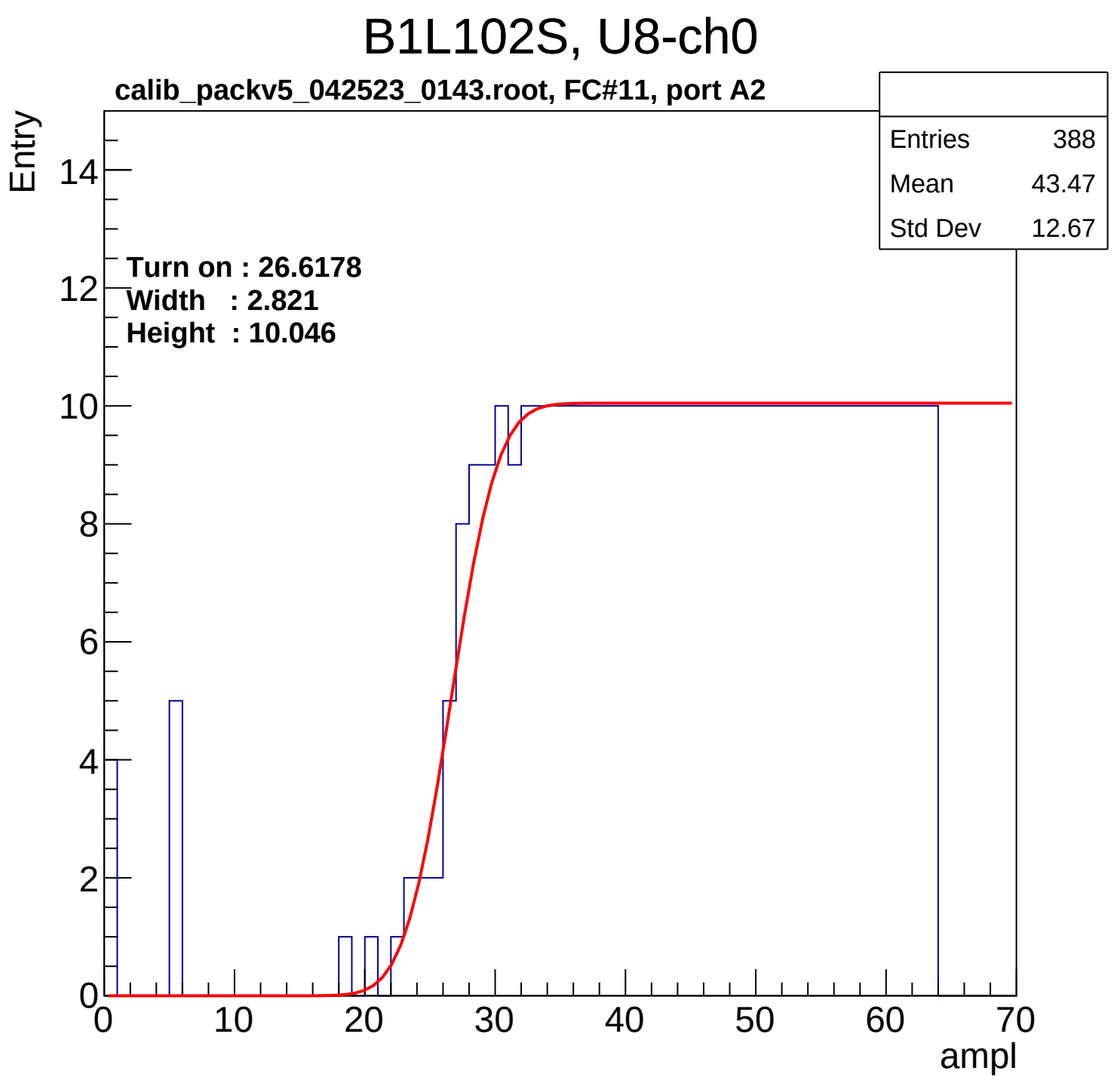
B1L102S, U8-ch0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.47
Std Dev 12.67
Turn on : 26.6178
Width : 2.821
Height : 10.046
Entry
ampl
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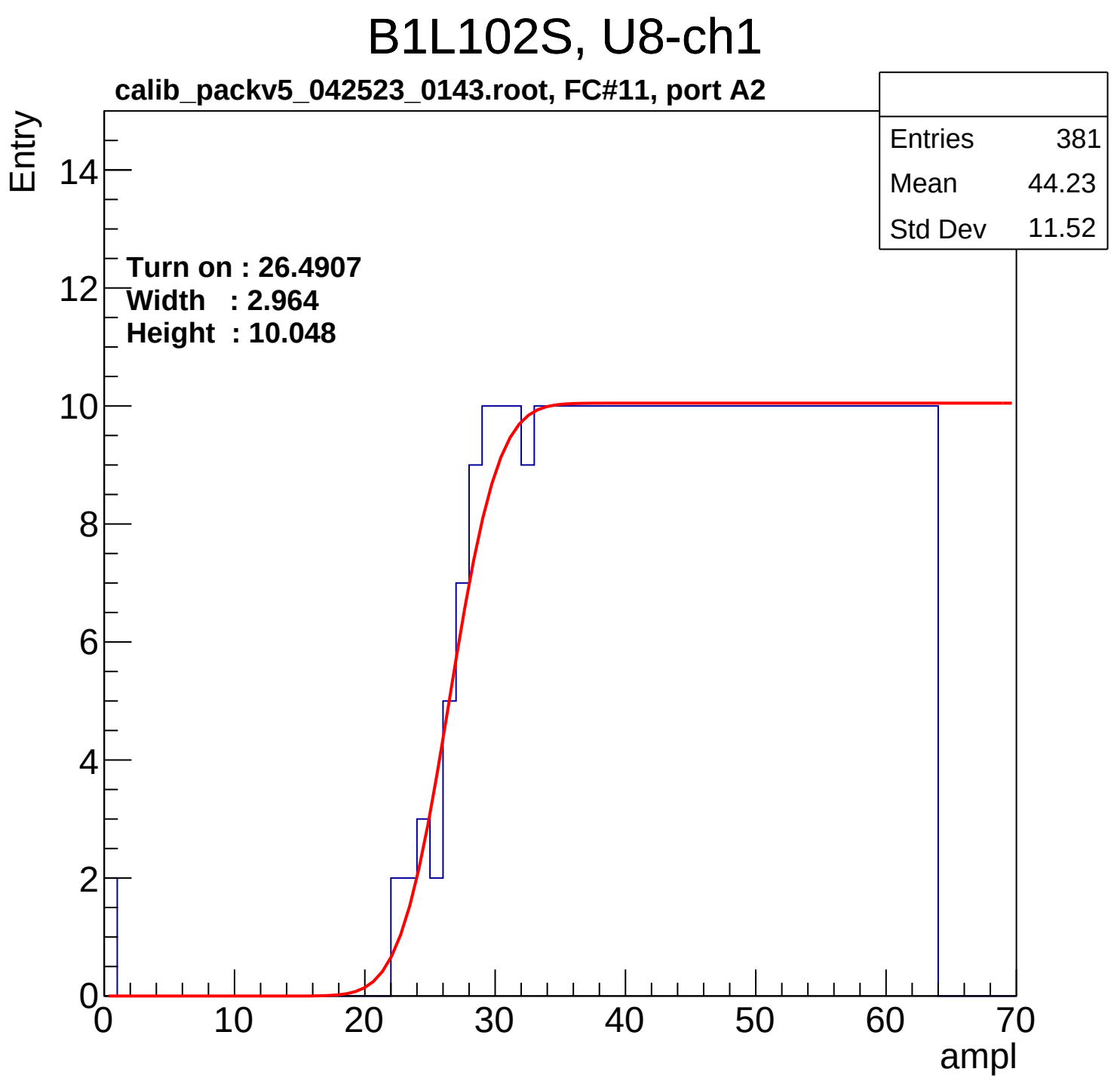
B1L102S, U8-ch1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.23
Std Dev 11.52
Turn on : 26.4907
Width : 2.964
Height : 10.048
Entry
ampl
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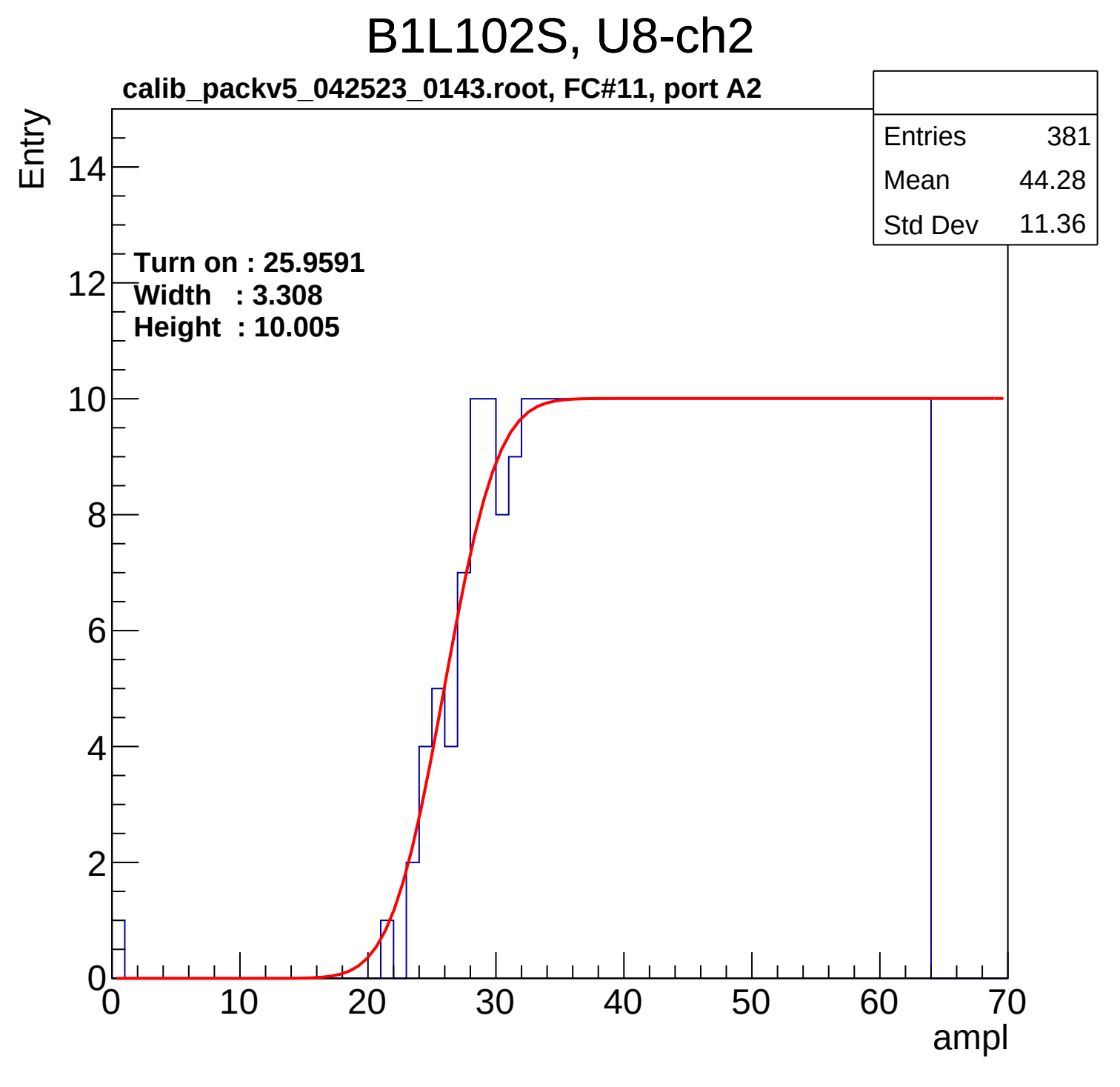
B1L102S, U8-ch2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.28
Std Dev 11.36
Turn on : 25.9591
Width : 3.308
Height : 10.005
Entry
ampl
0
2
4
6
8
10
12
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0
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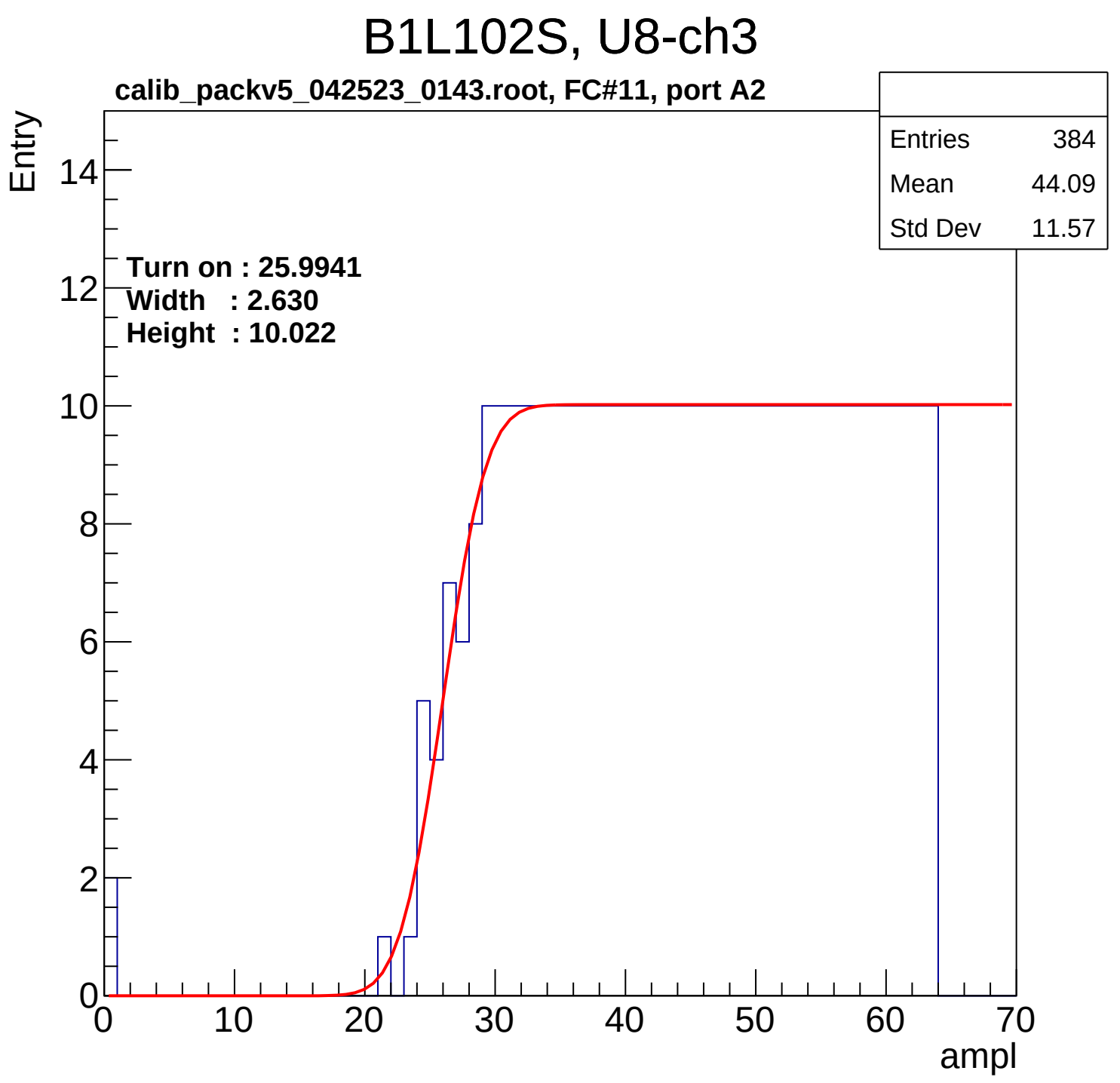
B1L102S, U8-ch3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.09
Std Dev 11.57
Turn on : 25.9941
Width : 2.630
Height : 10.022
Entry
ampl
0
2
4
6
8
10
12
14
0
10
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40
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60
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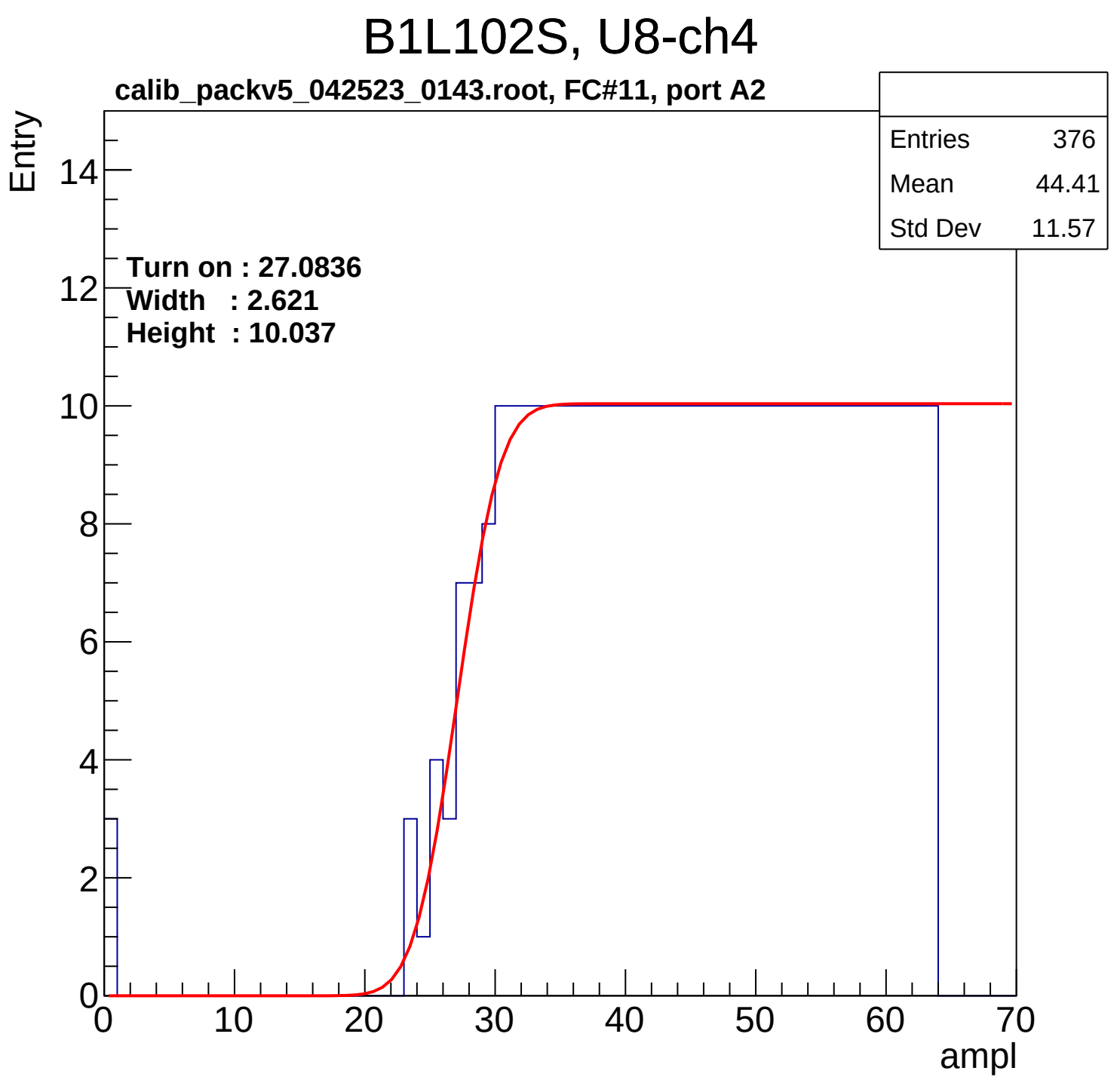
B1L102S, U8-ch4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.41
Std Dev 11.57
Turn on : 27.0836
Width : 2.621
Height : 10.037
Entry
ampl
0
2
4
6
8
10
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0
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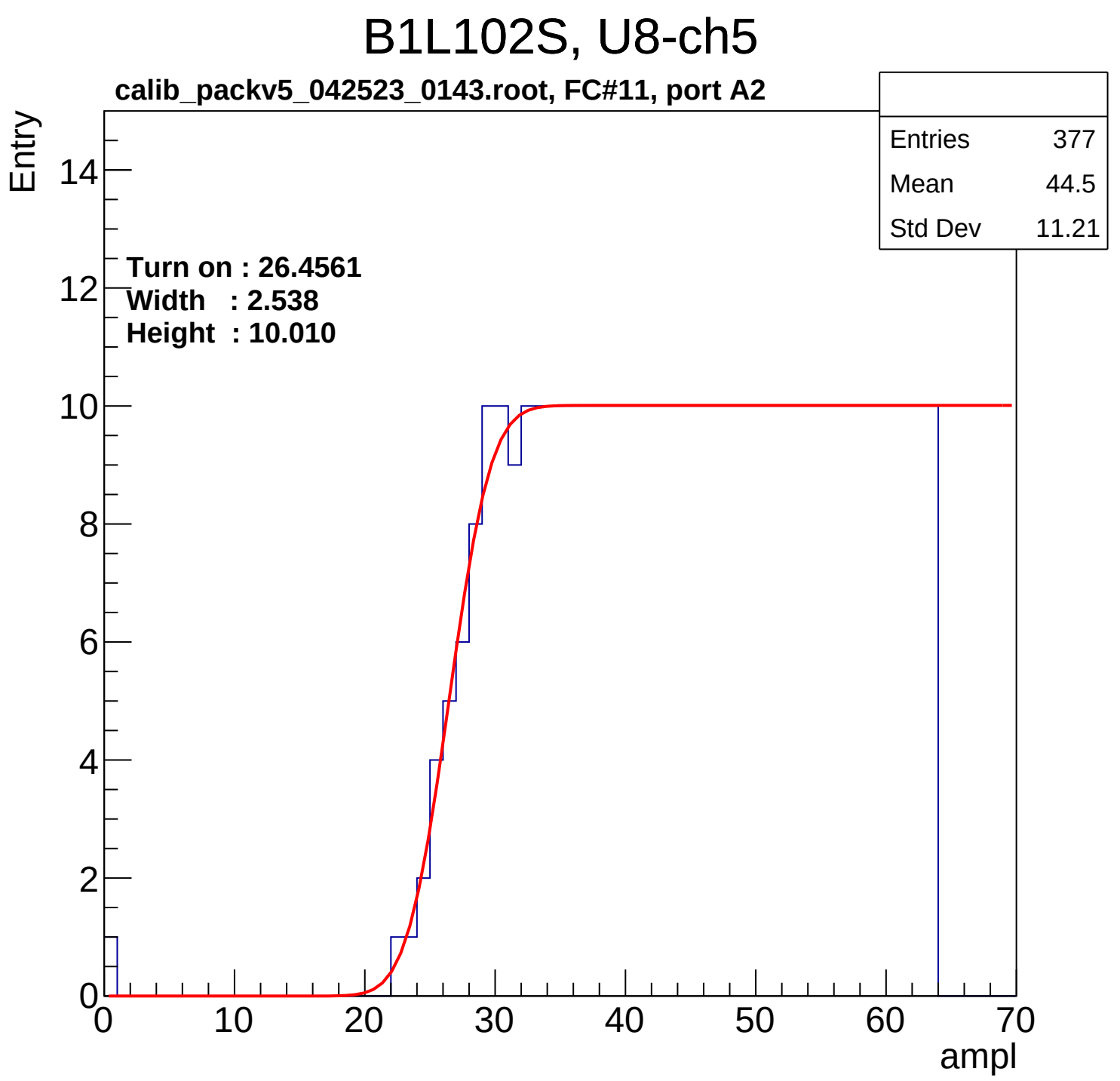
B1L102S, U8-ch5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.5
Std Dev 11.21
Turn on : 26.4561
Width : 2.538
Height : 10.010
Entry
ampl
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2
4
6
8
10
12
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0
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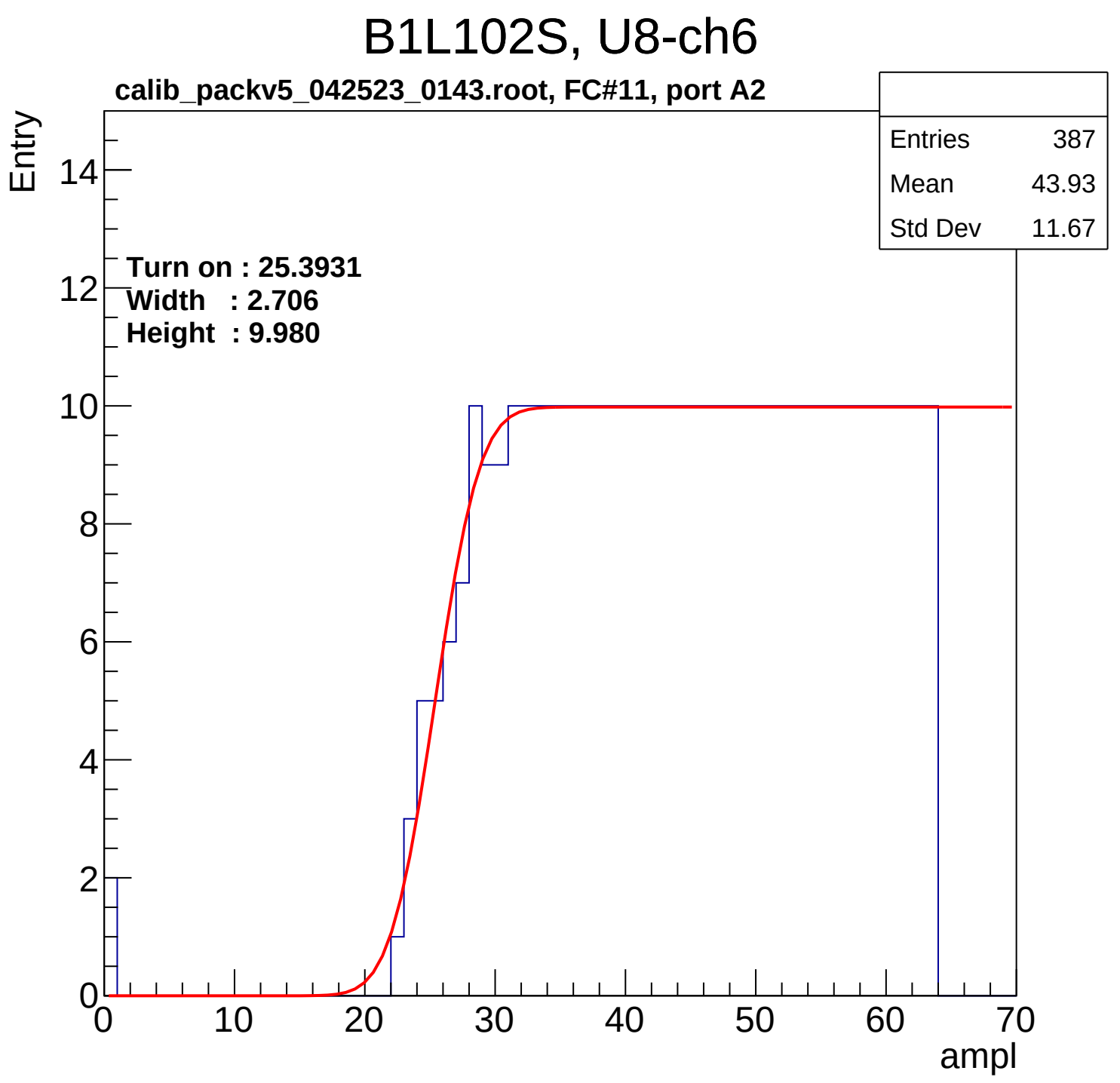
B1L102S, U8-ch6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.93
Std Dev 11.67
Turn on : 25.3931
Width : 2.706
Height : 9.980
Entry
ampl
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2
4
6
8
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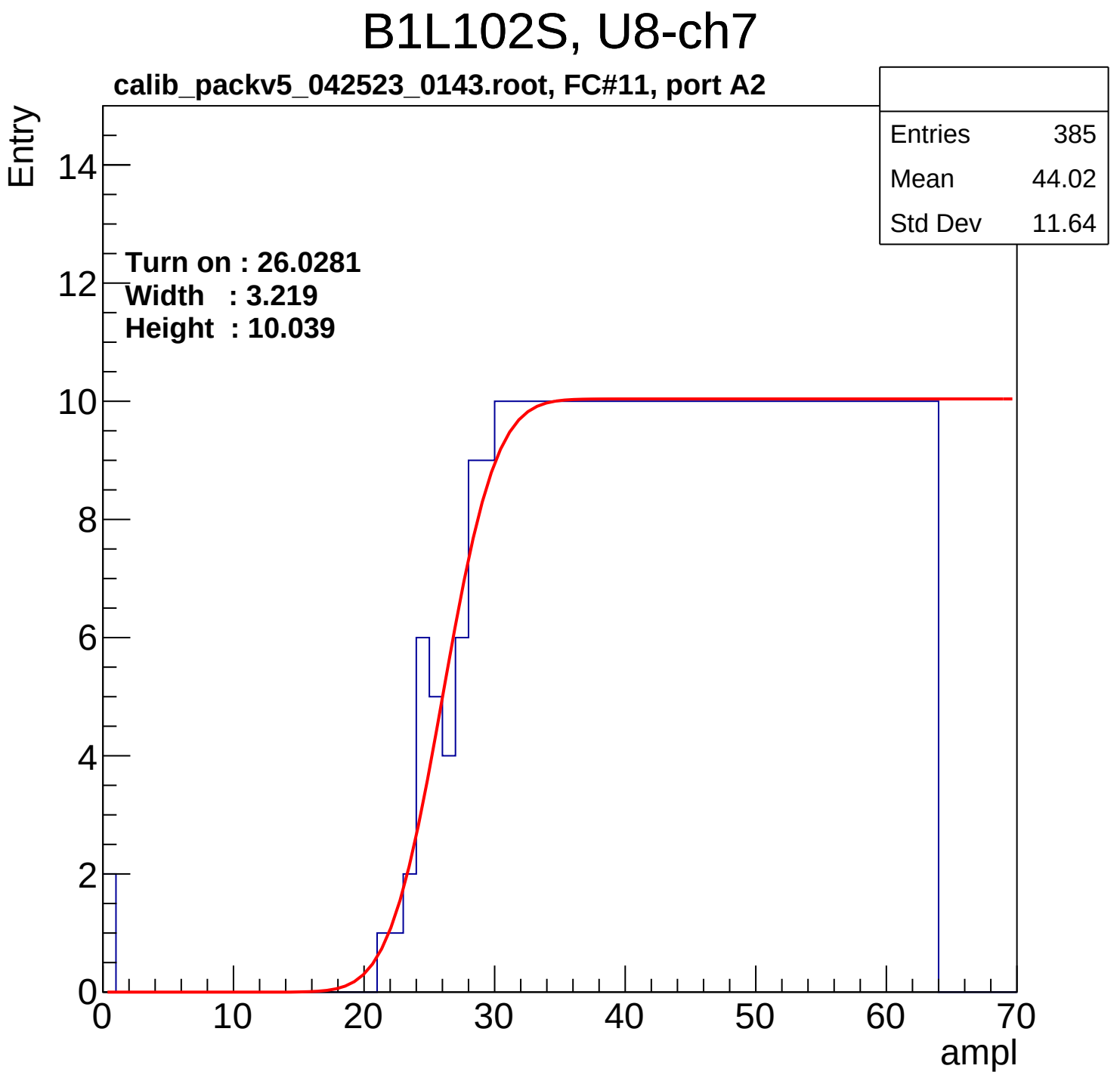
B1L102S, U8-ch7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 44.02
Std Dev 11.64
Turn on : 26.0281
Width : 3.219
Height : 10.039
Entry
ampl
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2
4
6
8
10
12
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0
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20
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60
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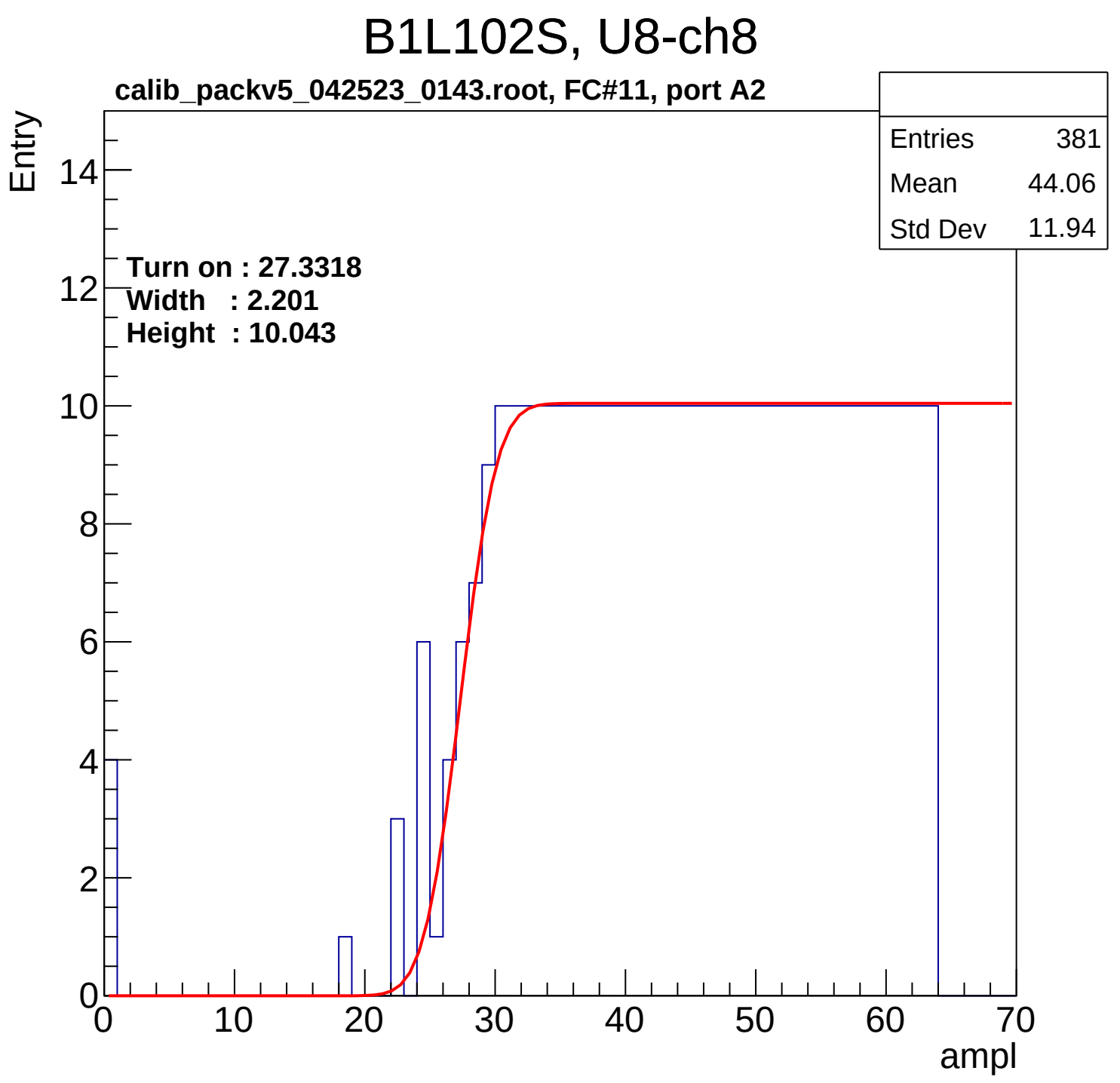
B1L102S, U8-ch8
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.06
Std Dev 11.94
Turn on : 27.3318
Width : 2.201
Height : 10.043
Entry
ampl
0
2
4
6
8
10
12
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0
10
20
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40
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60
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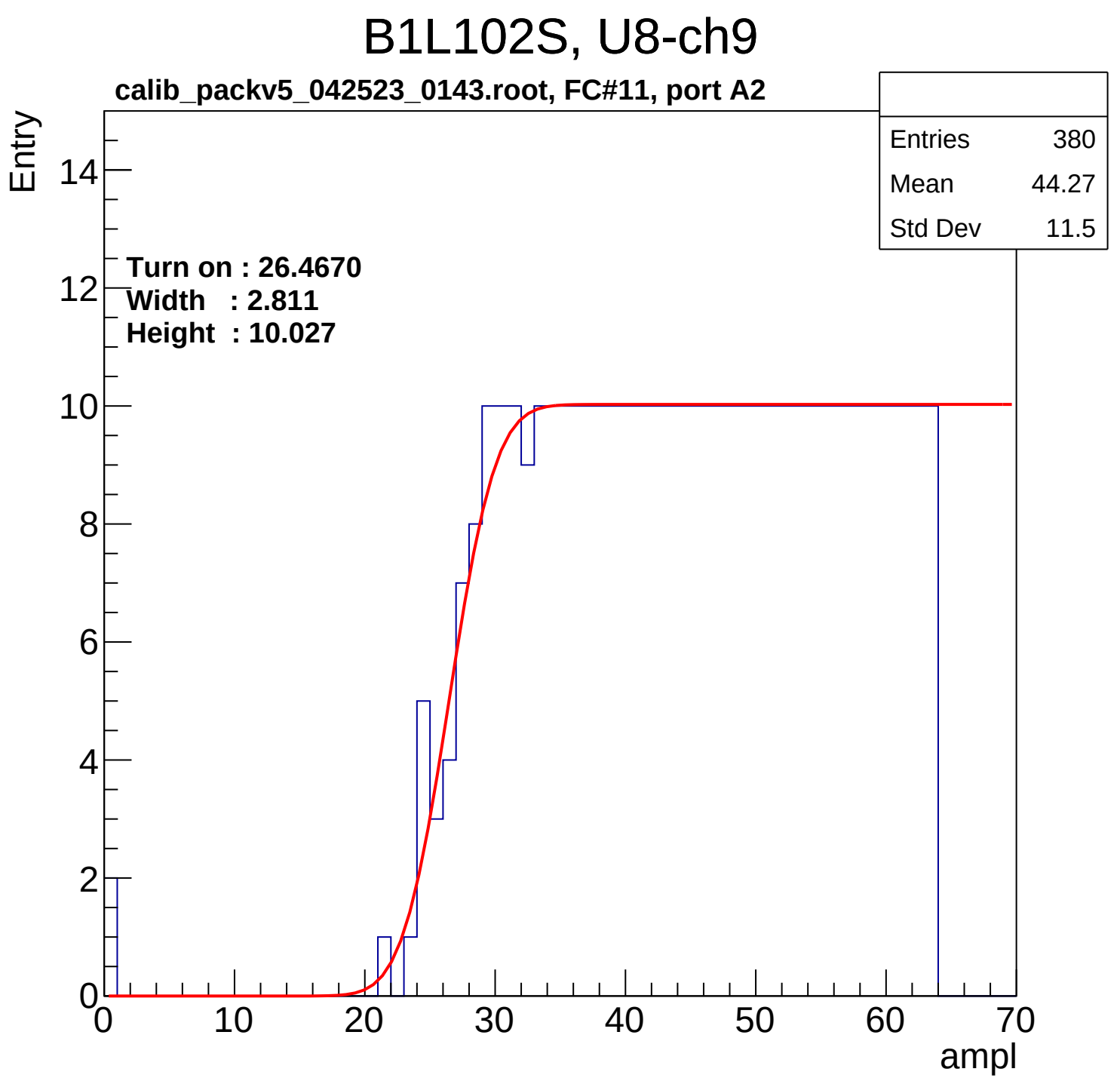
B1L102S, U8-ch9
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.27
Std Dev 11.5
Turn on : 26.4670
Width : 2.811
Height : 10.027
Entry
ampl
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6
8
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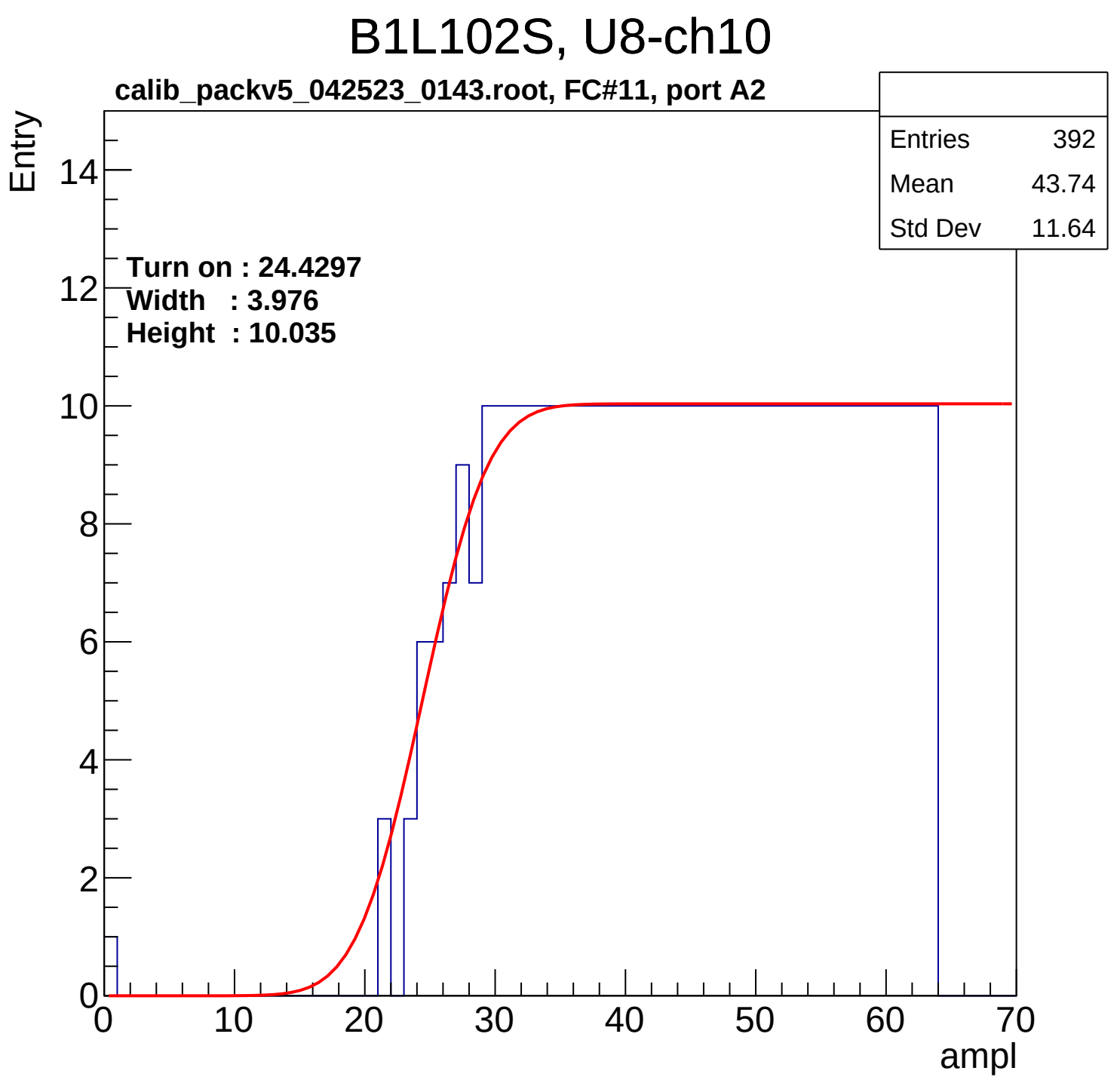
B1L102S, U8-ch10
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.74
Std Dev 11.64
Turn on : 24.4297
Width : 3.976
Height : 10.035
Entry
ampl
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4
6
8
10
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0
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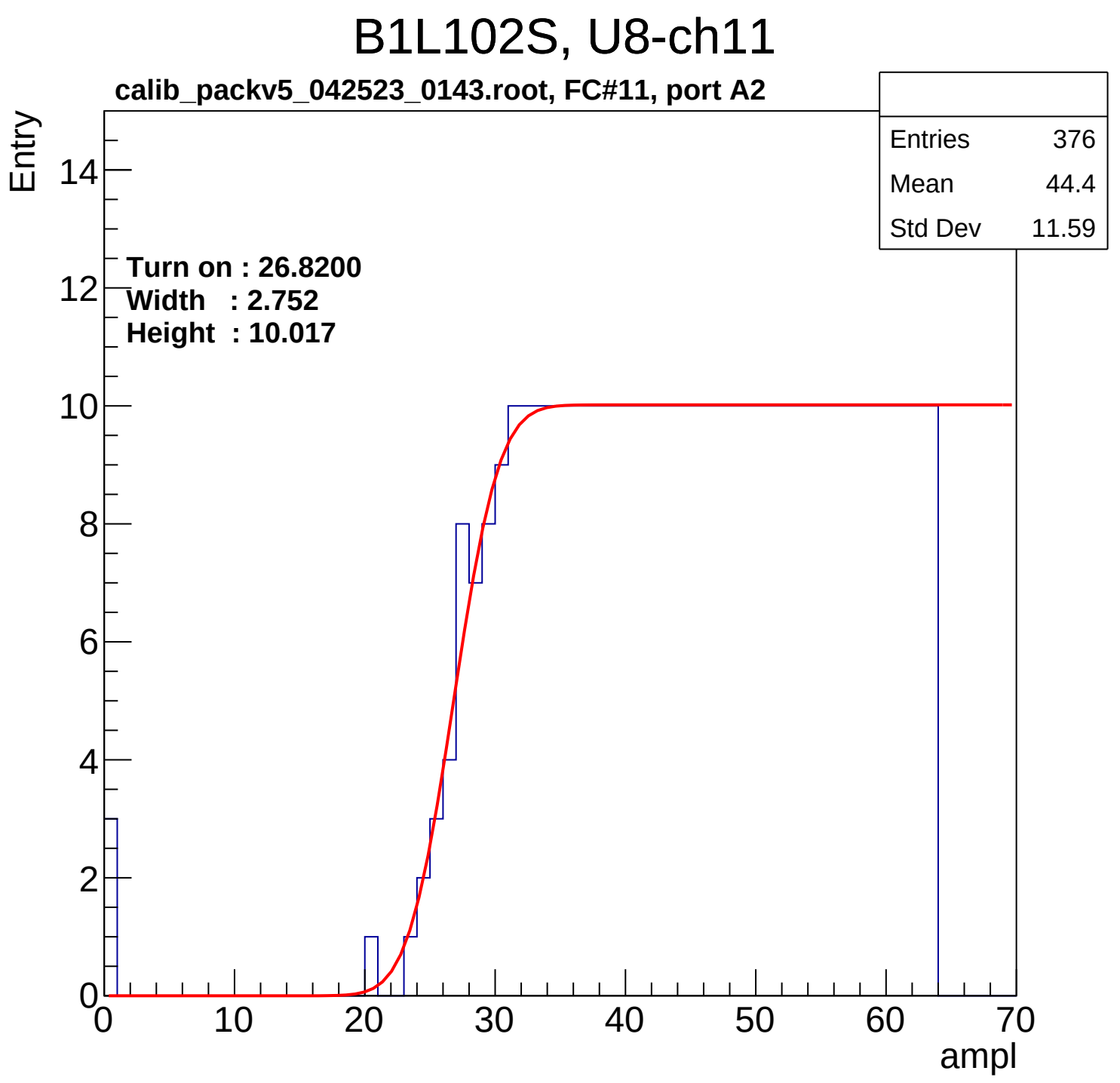
B1L102S, U8-ch11
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.4
Std Dev 11.59
Turn on : 26.8200
Width : 2.752
Height : 10.017
Entry
ampl
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4
6
8
10
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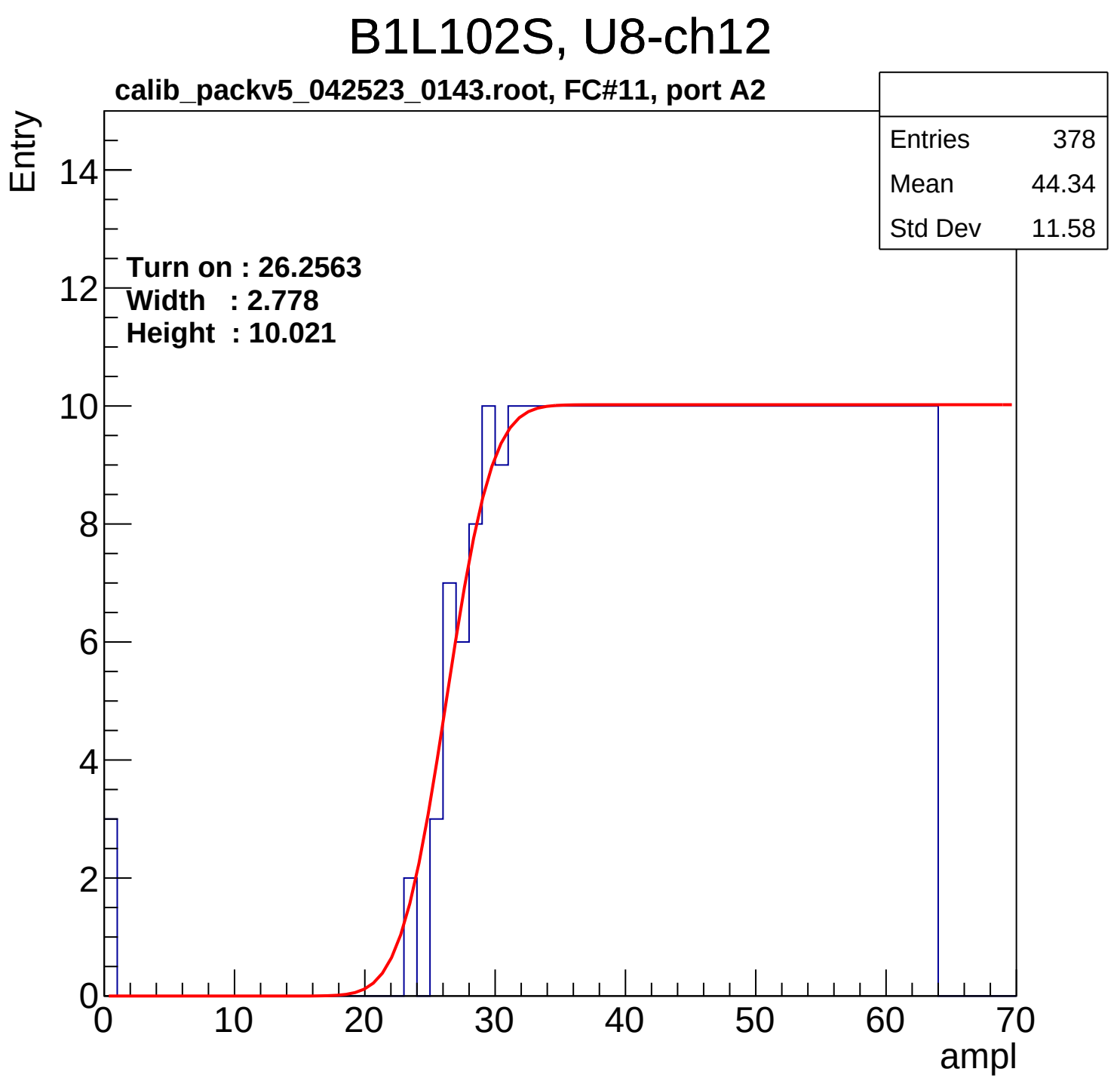
B1L102S, U8-ch12
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.34
Std Dev 11.58
Turn on : 26.2563
Width : 2.778
Height : 10.021
Entry
ampl
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2
4
6
8
10
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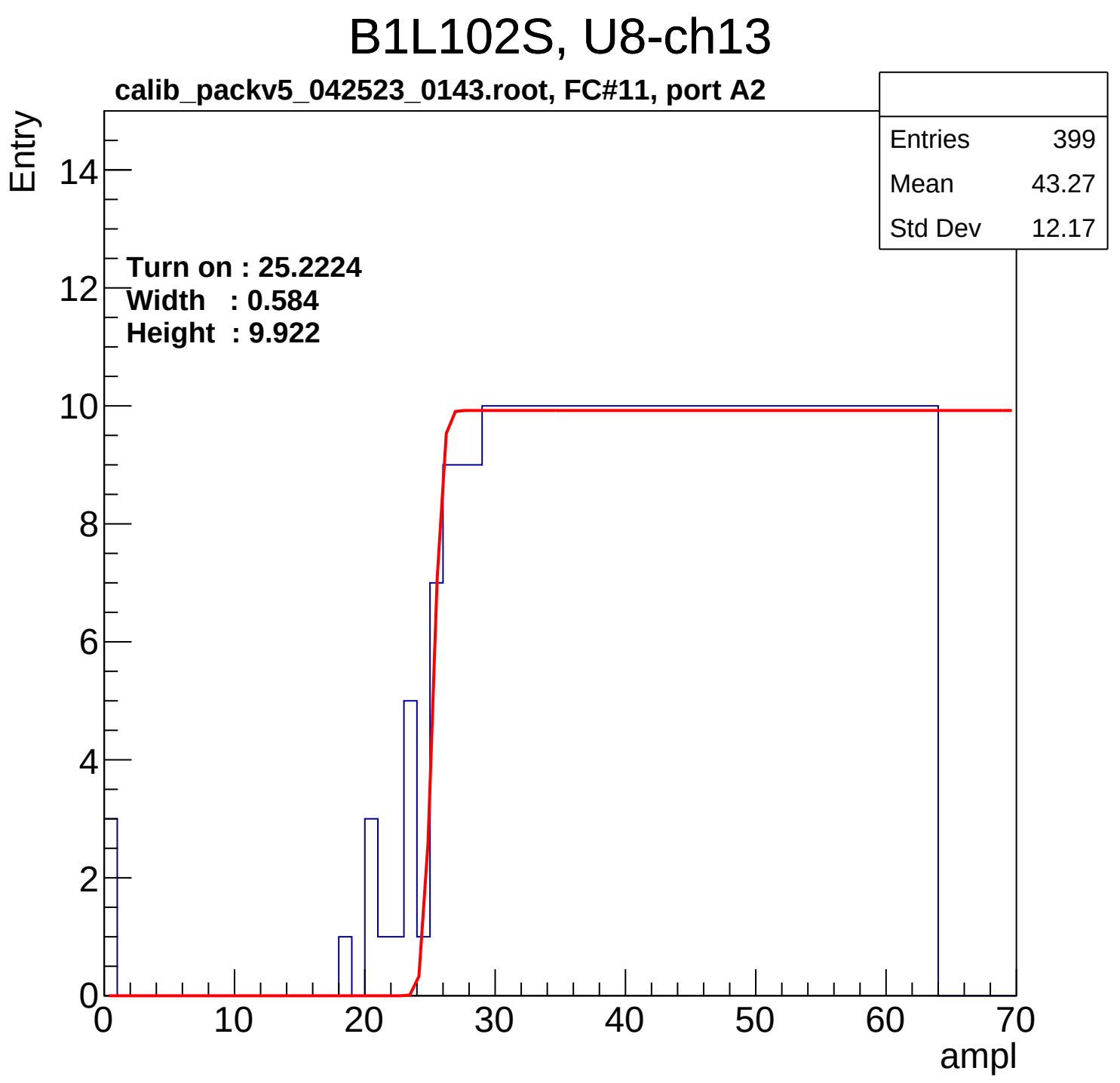
B1L102S, U8-ch13
calib_packv5_042523_0143.root, FC#11, port A2
Entries 399
Mean 43.27
Std Dev 12.17
Turn on : 25.2224
Width : 0.584
Height : 9.922
Entry
ampl
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2
4
6
8
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0
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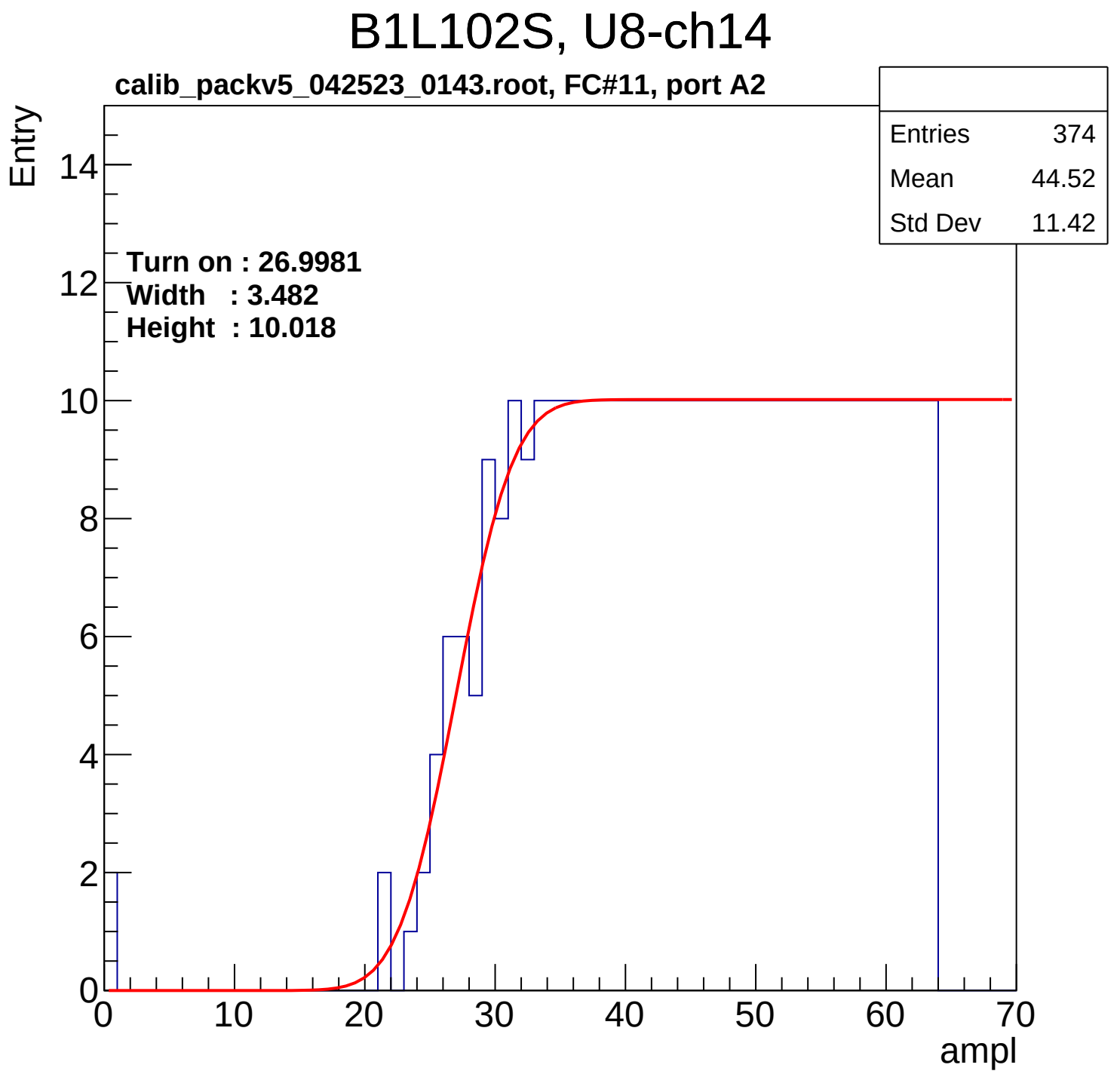
B1L102S, U8-ch14
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.52
Std Dev 11.42
Turn on : 26.9981
Width : 3.482
Height : 10.018
Entry
ampl
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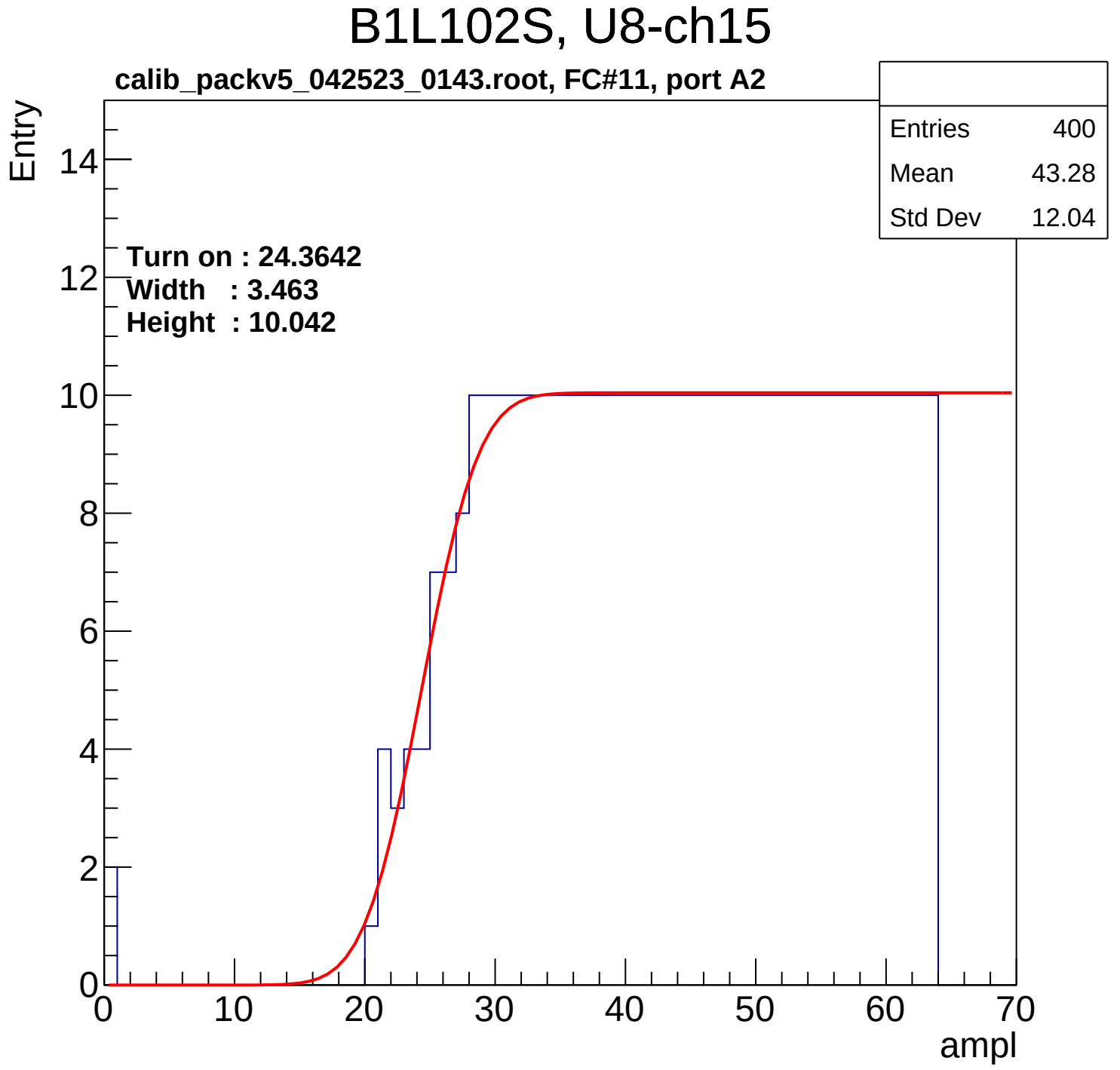
B1L102S, U8-ch15
calib_packv5_042523_0143.root, FC#11, port A2
Entries 400
Mean 43.28
Std Dev 12.04
Turn on : 24.3642
Width : 3.463
Height : 10.042
Entry
ampl
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4
6
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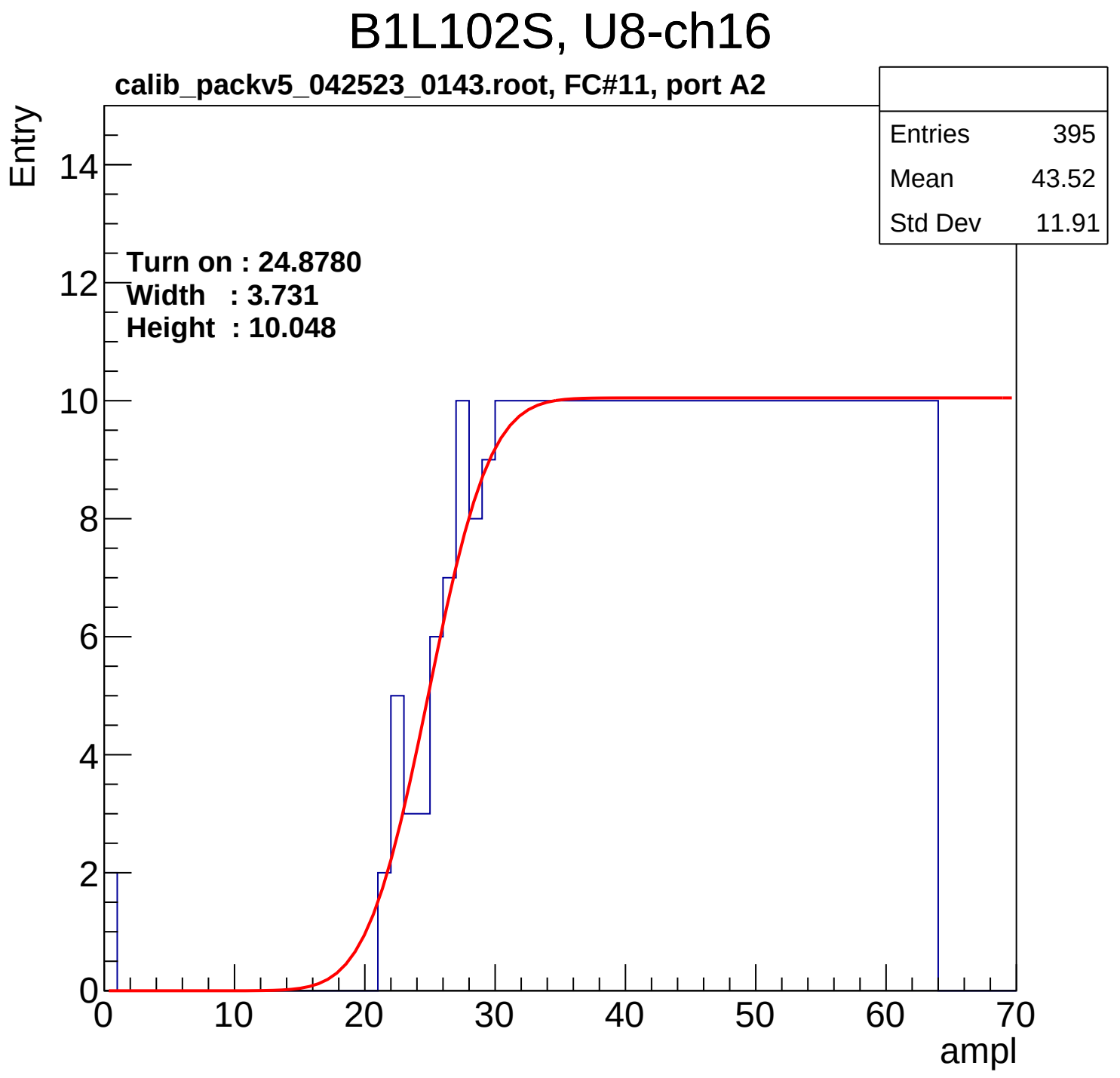
B1L102S, U8-ch16
calib_packv5_042523_0143.root, FC#11, port A2
Entries 395
Mean 43.52
Std Dev 11.91
Turn on : 24.8780
Width : 3.731
Height : 10.048
Entry
ampl
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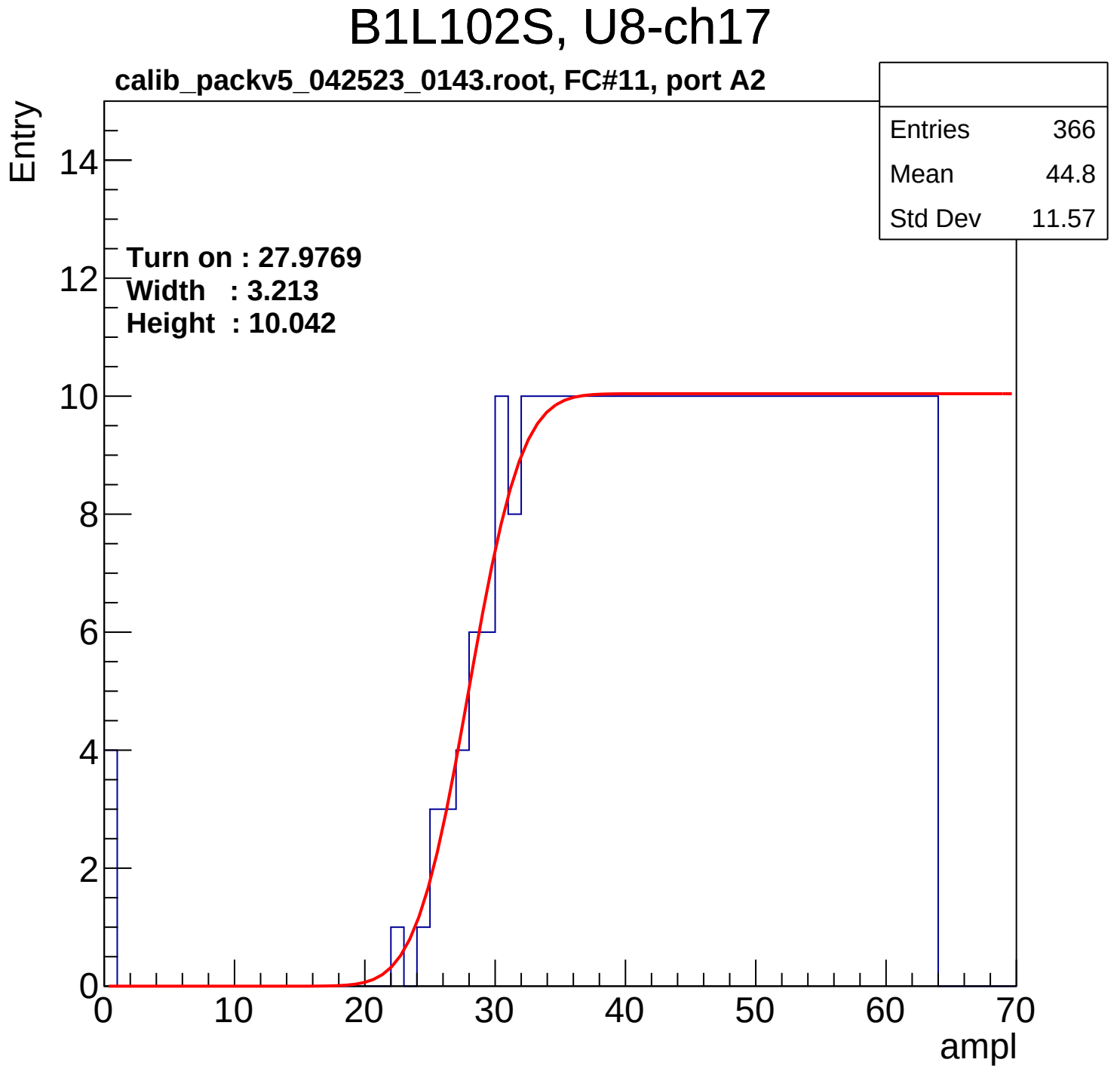
B1L102S, U8-ch17
calib_packv5_042523_0143.root, FC#11, port A2
Entries 366
Mean 44.8
Std Dev 11.57
Turn on : 27.9769
Width : 3.213
Height : 10.042
Entry
ampl
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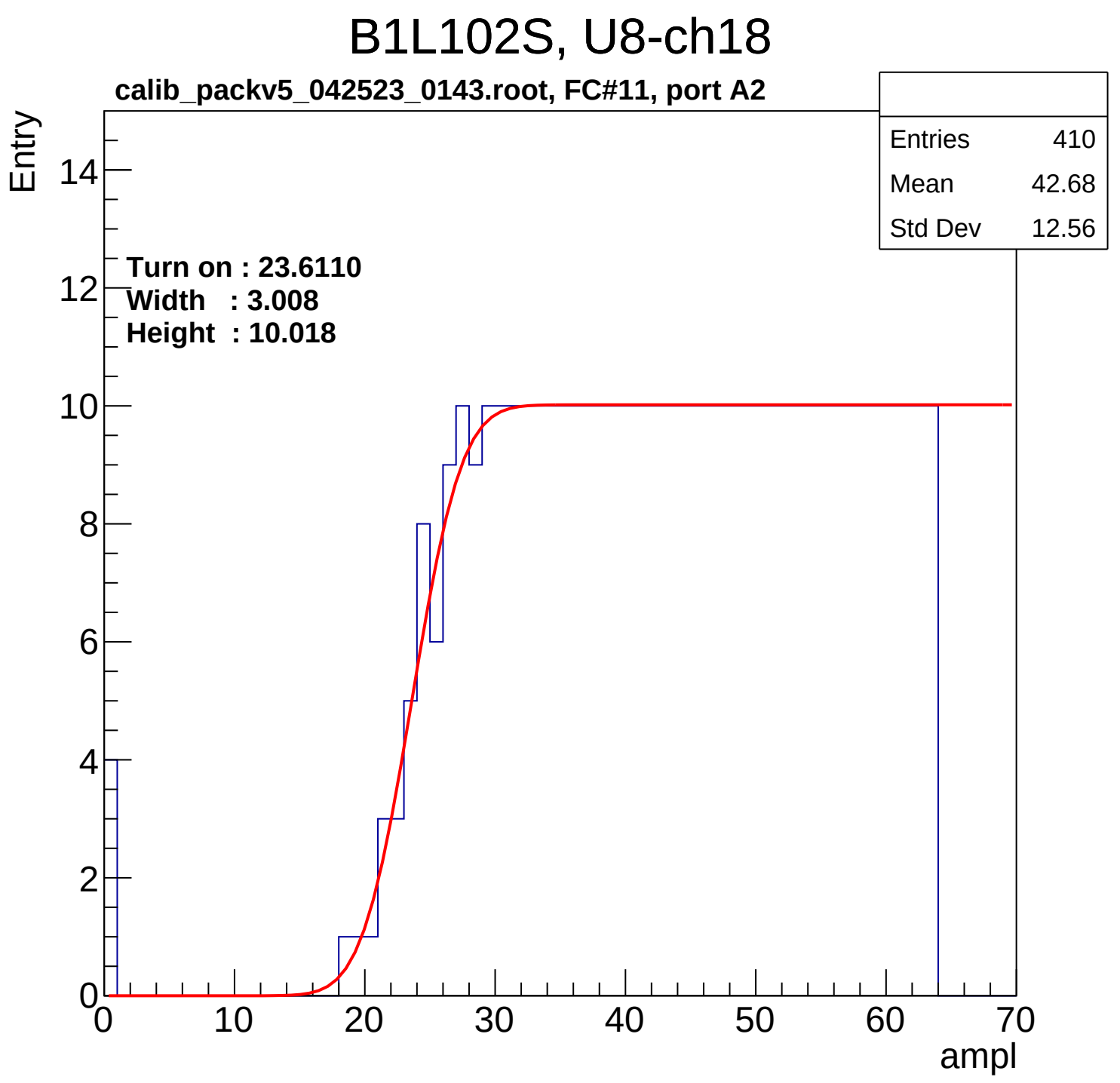
B1L102S, U8-ch18
calib_packv5_042523_0143.root, FC#11, port A2
Entries 410
Mean 42.68
Std Dev 12.56
Turn on : 23.6110
Width : 3.008
Height : 10.018
Entry
ampl
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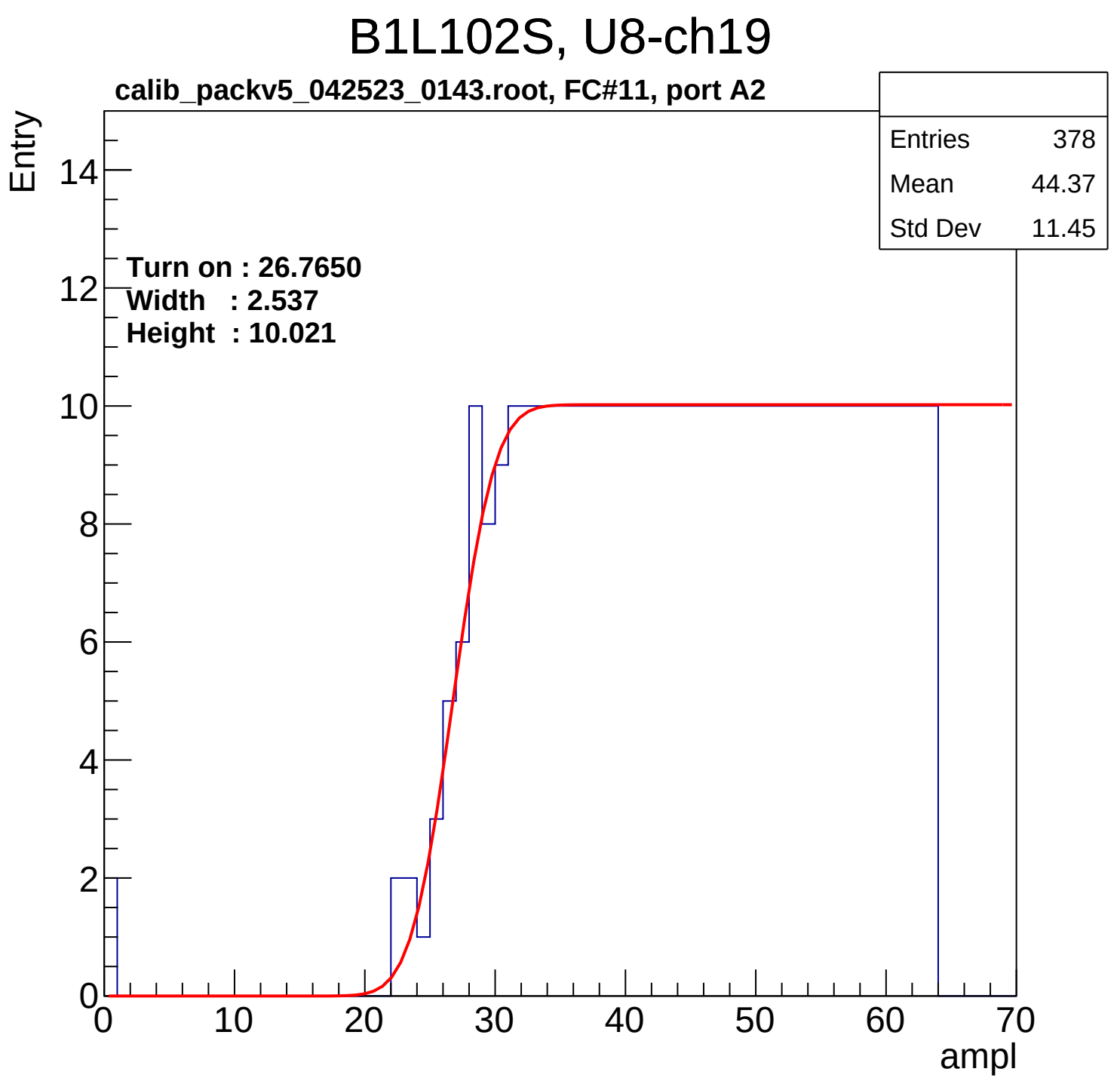
B1L102S, U8-ch19
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.37
Std Dev 11.45
Turn on : 26.7650
Width : 2.537
Height : 10.021
Entry
ampl
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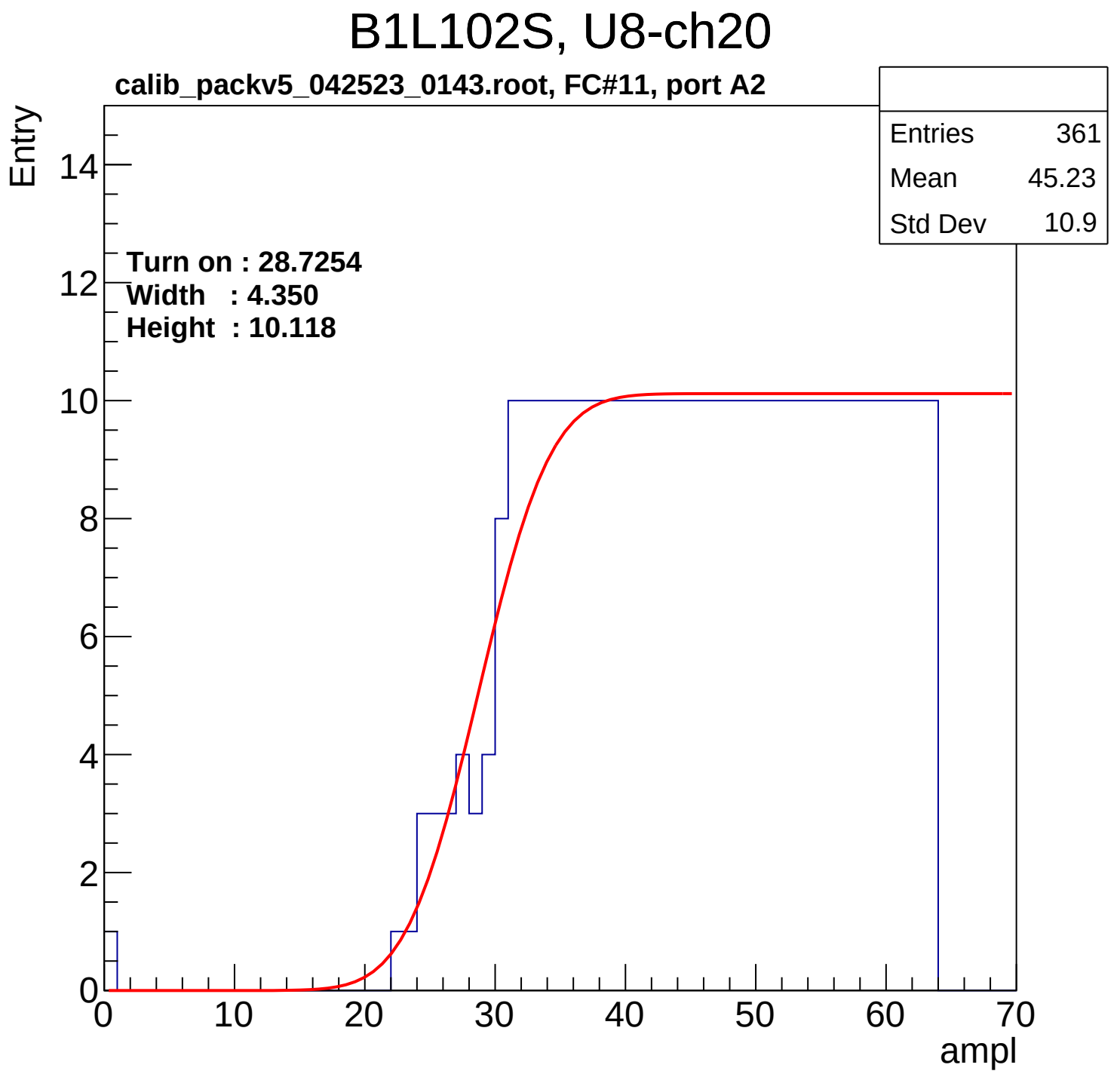
B1L102S, U8-ch20
calib_packv5_042523_0143.root, FC#11, port A2
Entries 361
Mean 45.23
Std Dev 10.9
Turn on : 28.7254
Width : 4.350
Height : 10.118
Entry
ampl
0
2
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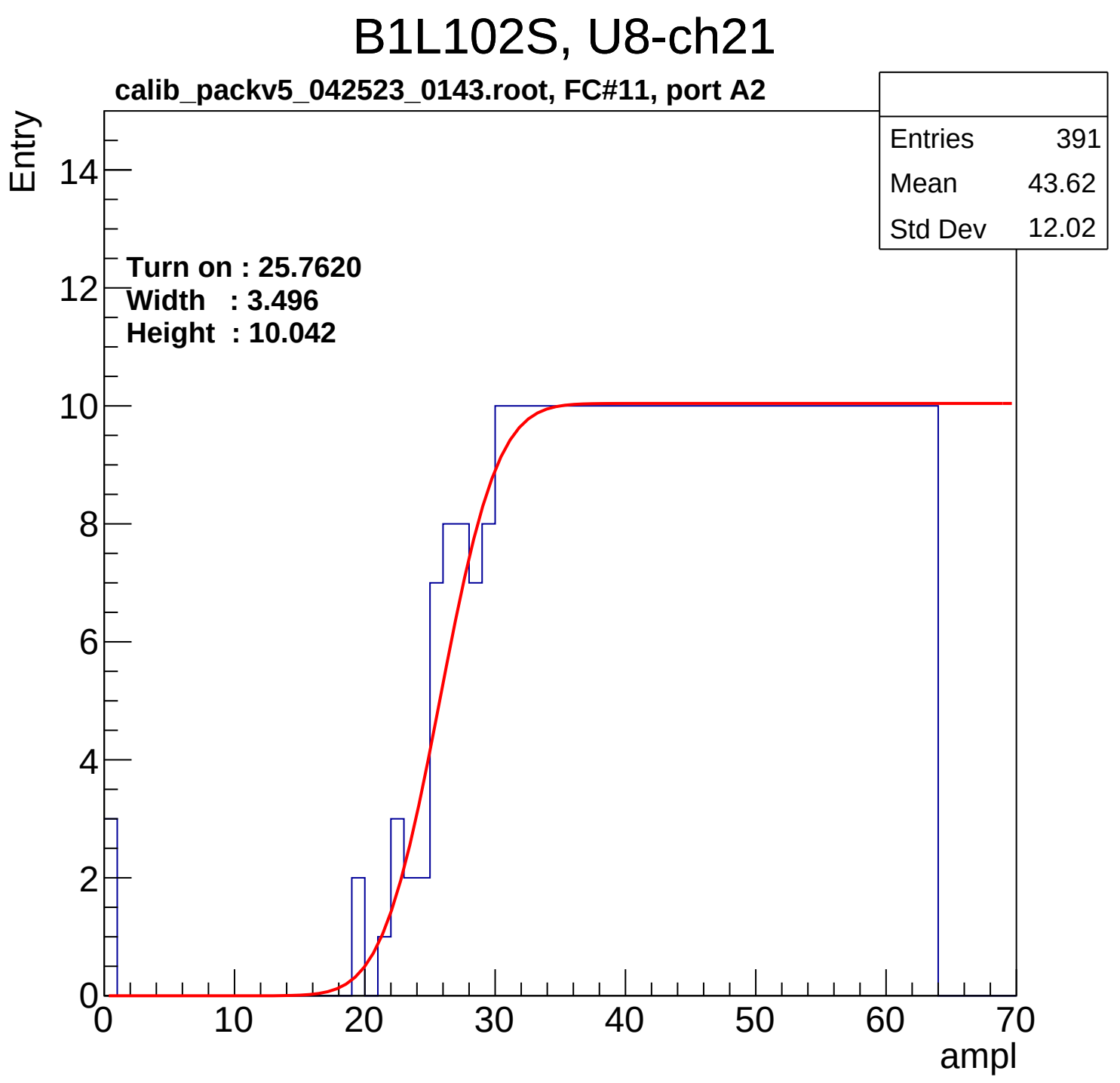
B1L102S, U8-ch21
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.62
Std Dev 12.02
Turn on : 25.7620
Width : 3.496
Height : 10.042
Entry
ampl
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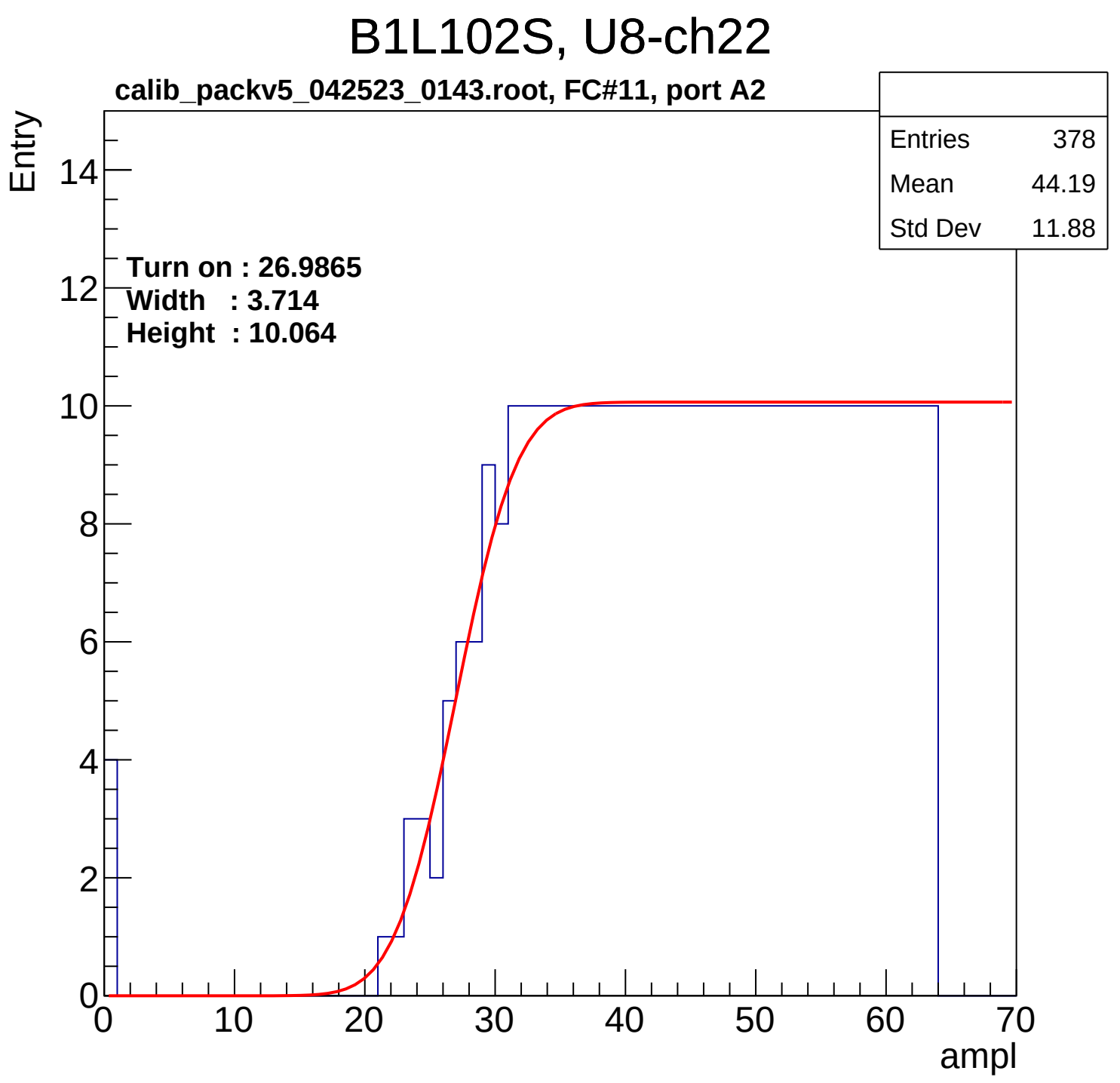
B1L102S, U8-ch22
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.19
Std Dev 11.88
Turn on : 26.9865
Width : 3.714
Height : 10.064
Entry
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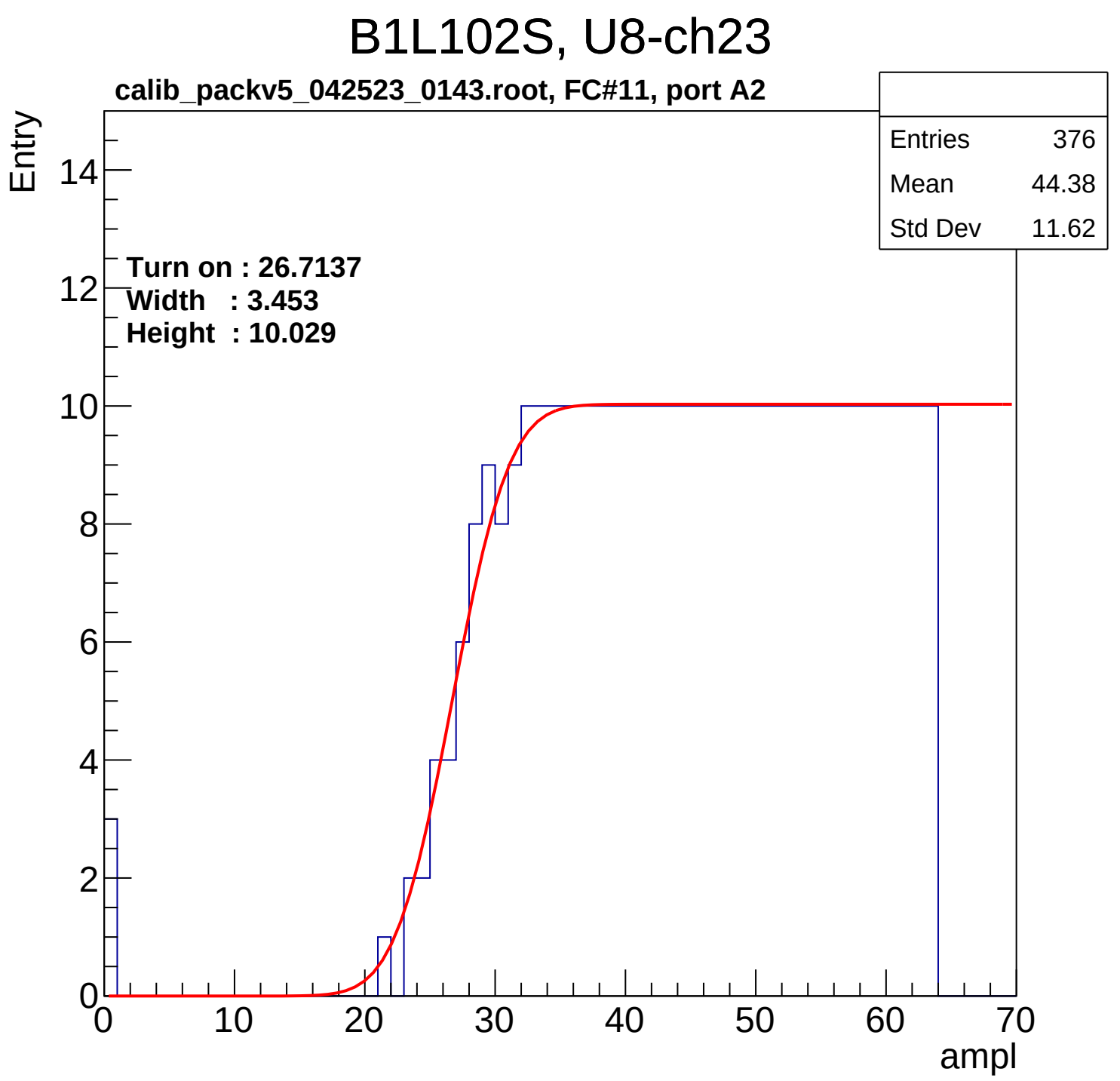
B1L102S, U8-ch23
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.38
Std Dev 11.62
Turn on : 26.7137
Width : 3.453
Height : 10.029
Entry
ampl
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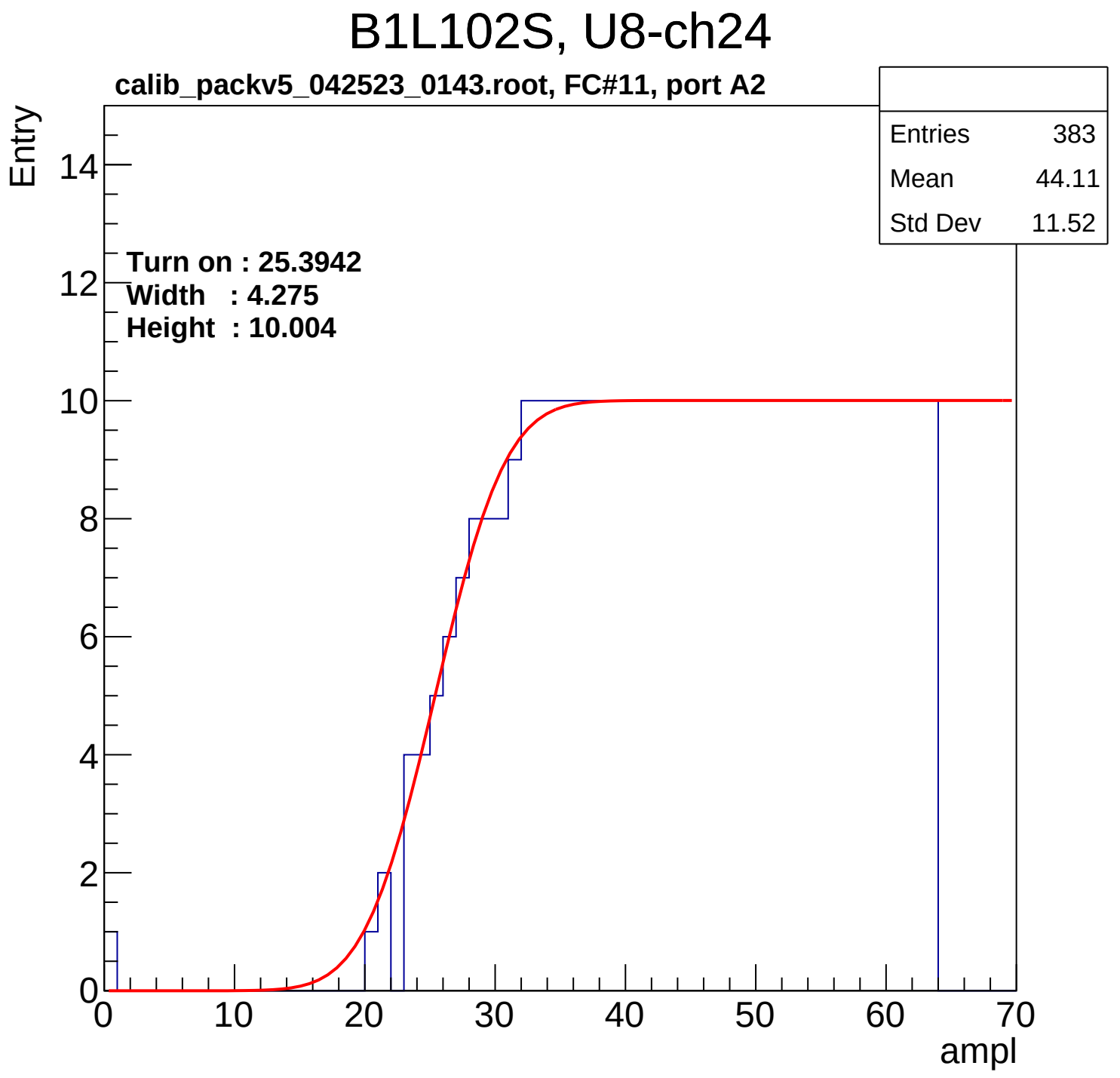
B1L102S, U8-ch24
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.11
Std Dev 11.52
Turn on : 25.3942
Width : 4.275
Height : 10.004
Entry
ampl
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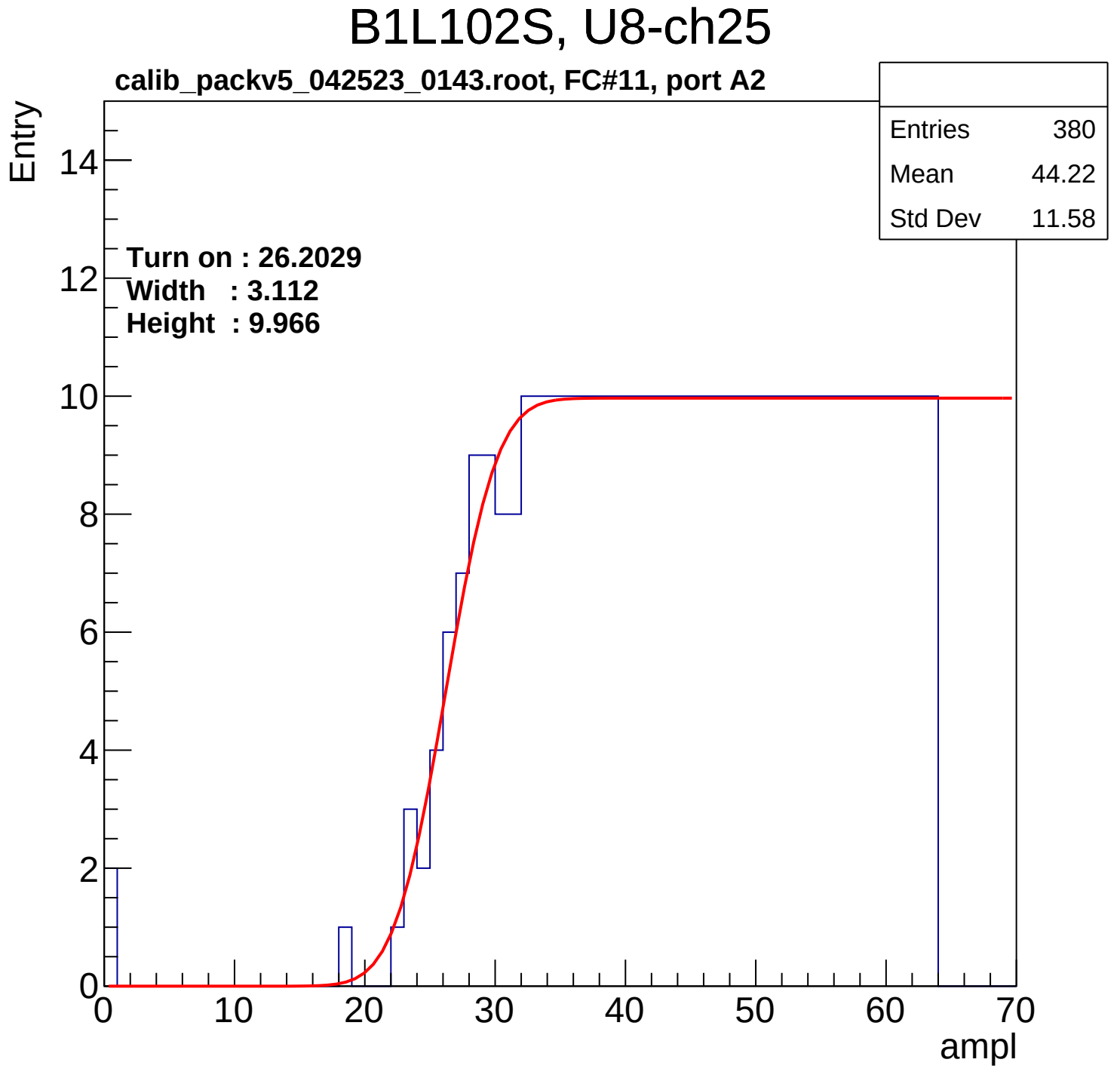
B1L102S, U8-ch25
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.22
Std Dev 11.58
Turn on : 26.2029
Width : 3.112
Height : 9.966
Entry
ampl
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6
8
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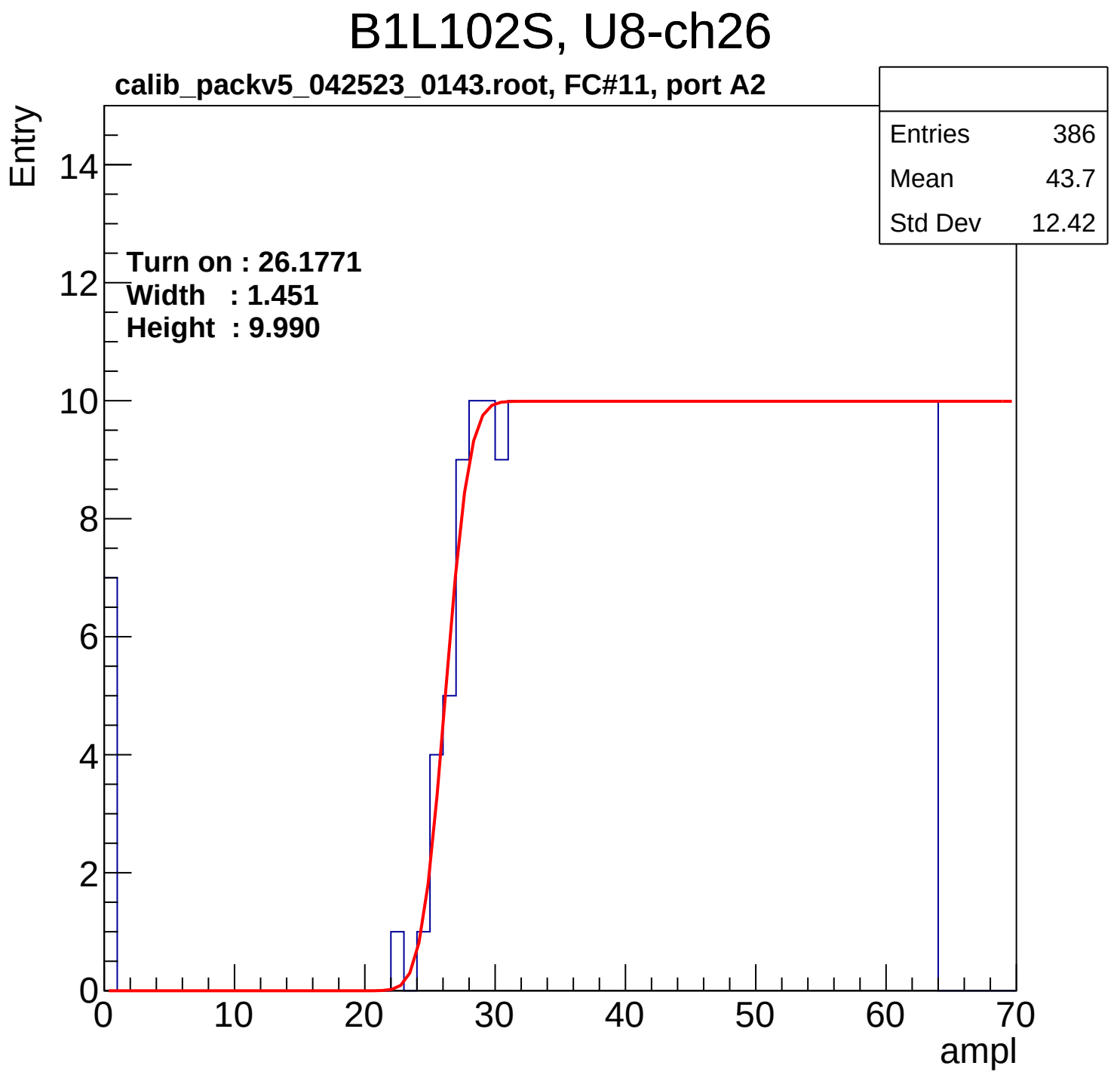
B1L102S, U8-ch26
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.7
Std Dev 12.42
Turn on : 26.1771
Width : 1.451
Height : 9.990
Entry
ampl
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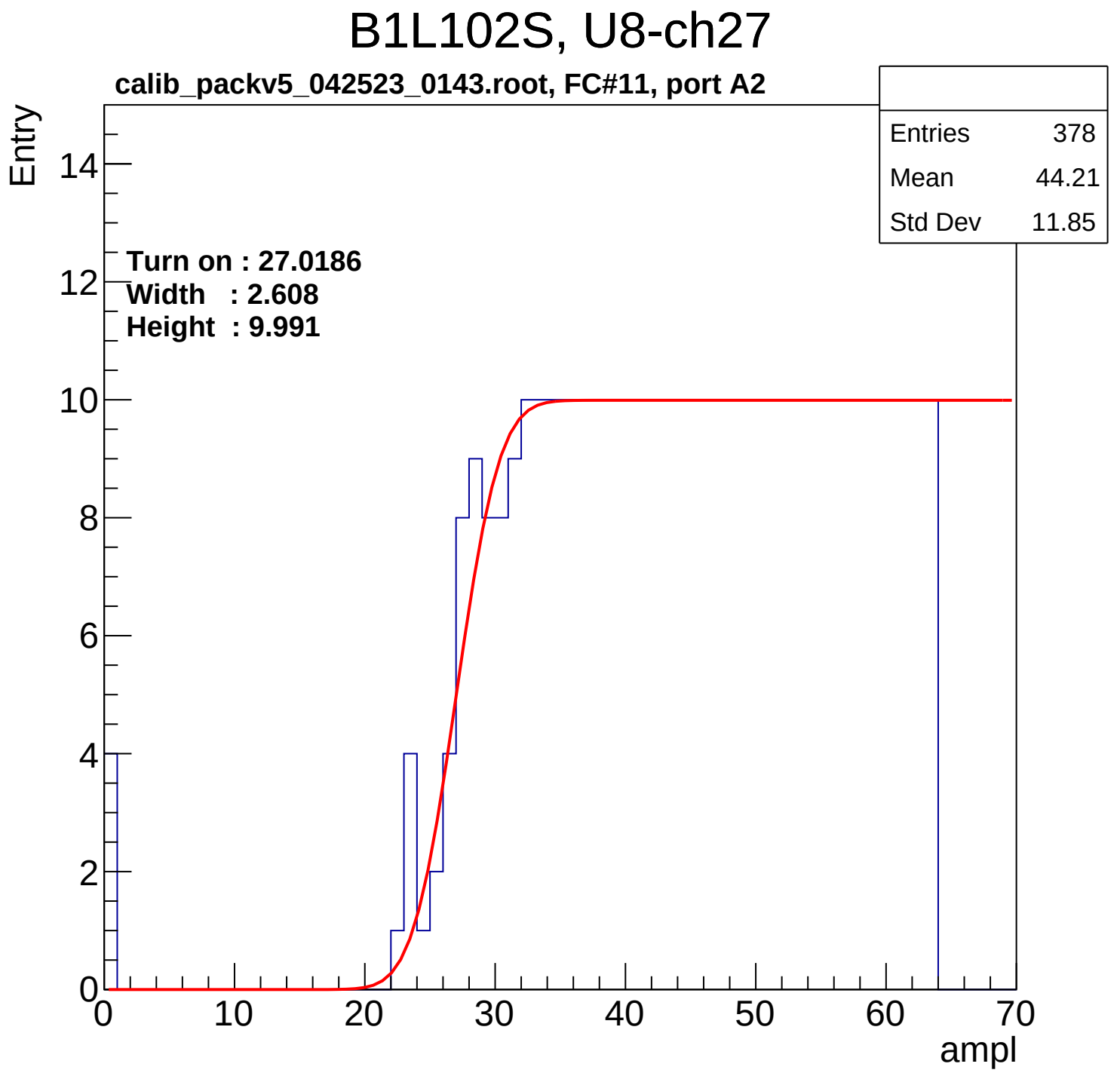
B1L102S, U8-ch27
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.21
Std Dev 11.85
Turn on : 27.0186
Width : 2.608
Height : 9.991
Entry
ampl
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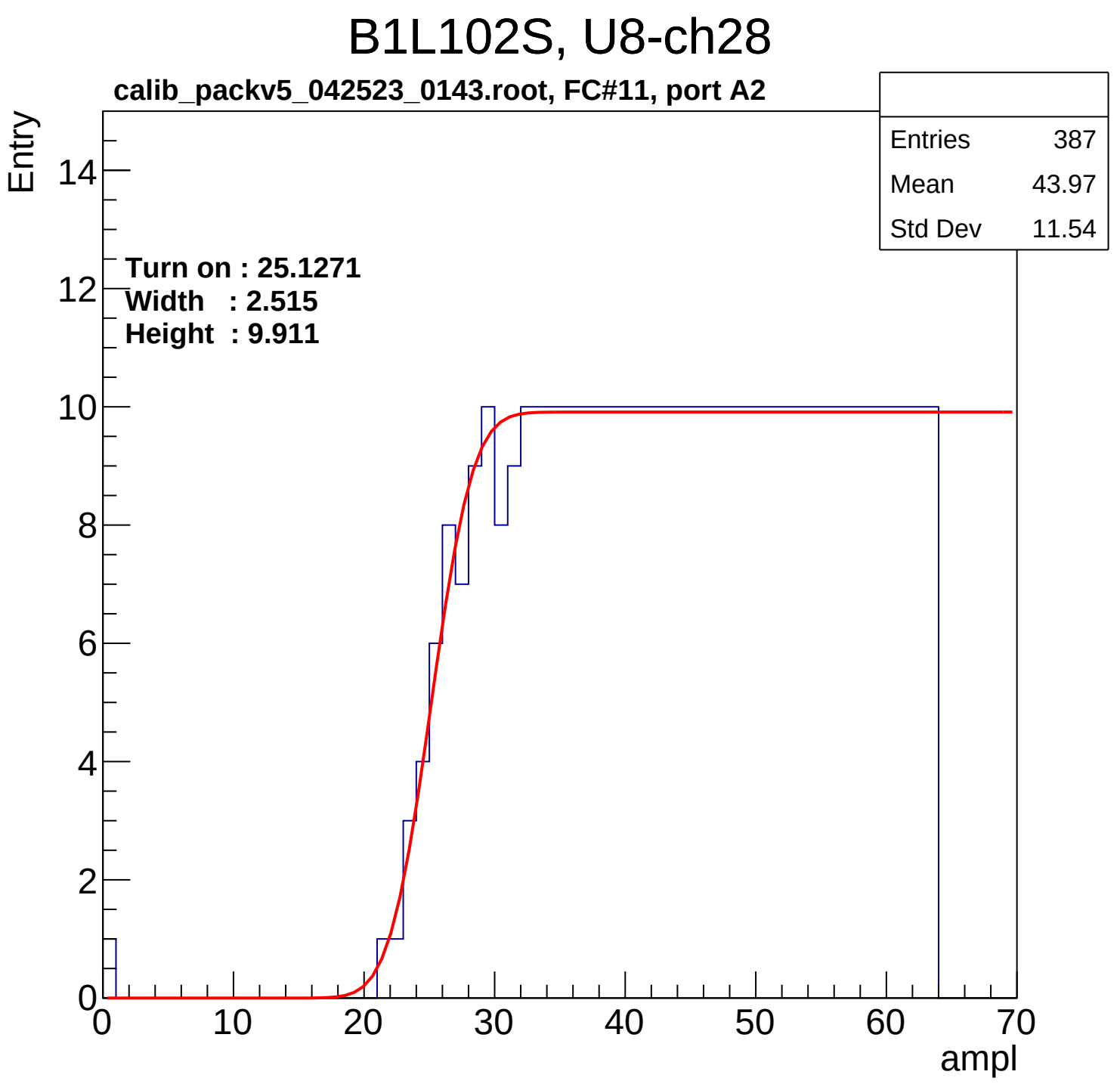
B1L102S, U8-ch28
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.97
Std Dev 11.54
Turn on : 25.1271
Width : 2.515
Height : 9.911
Entry
ampl
0
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4
6
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12
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20
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50
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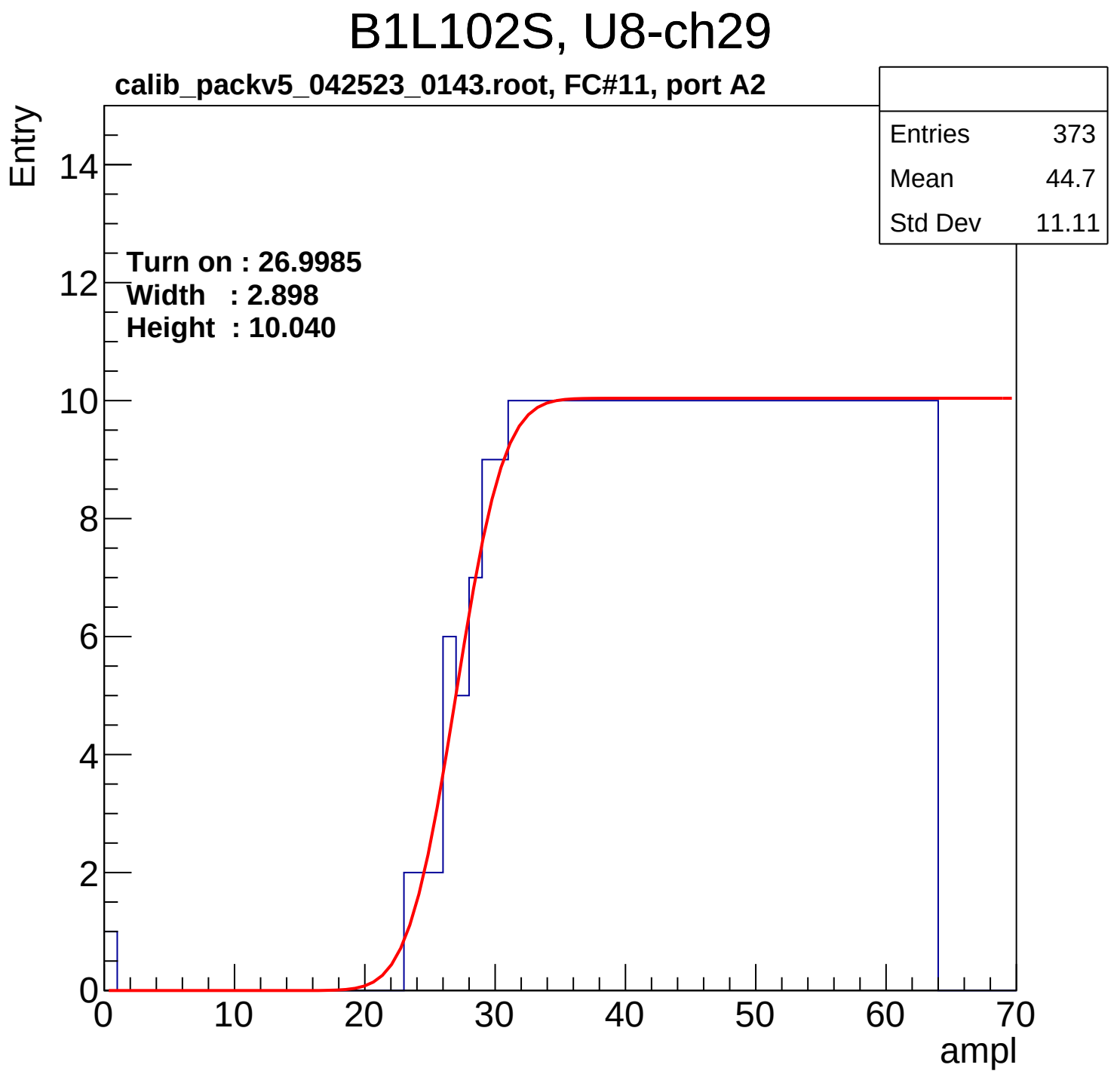
B1L102S, U8-ch29
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.7
Std Dev 11.11
Turn on : 26.9985
Width : 2.898
Height : 10.040
Entry
ampl
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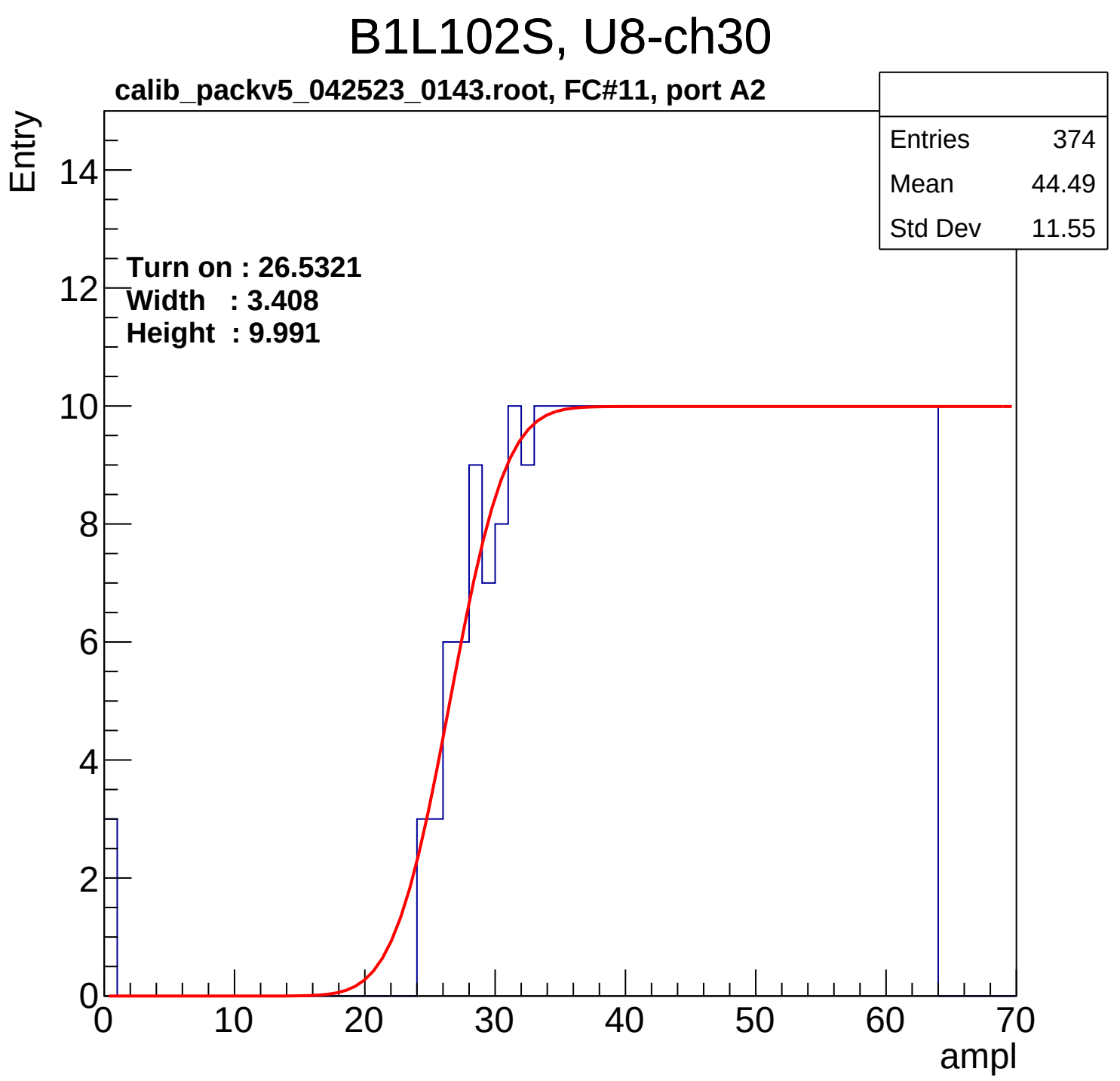
B1L102S, U8-ch30
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.49
Std Dev 11.55
Turn on : 26.5321
Width : 3.408
Height : 9.991
Entry
ampl
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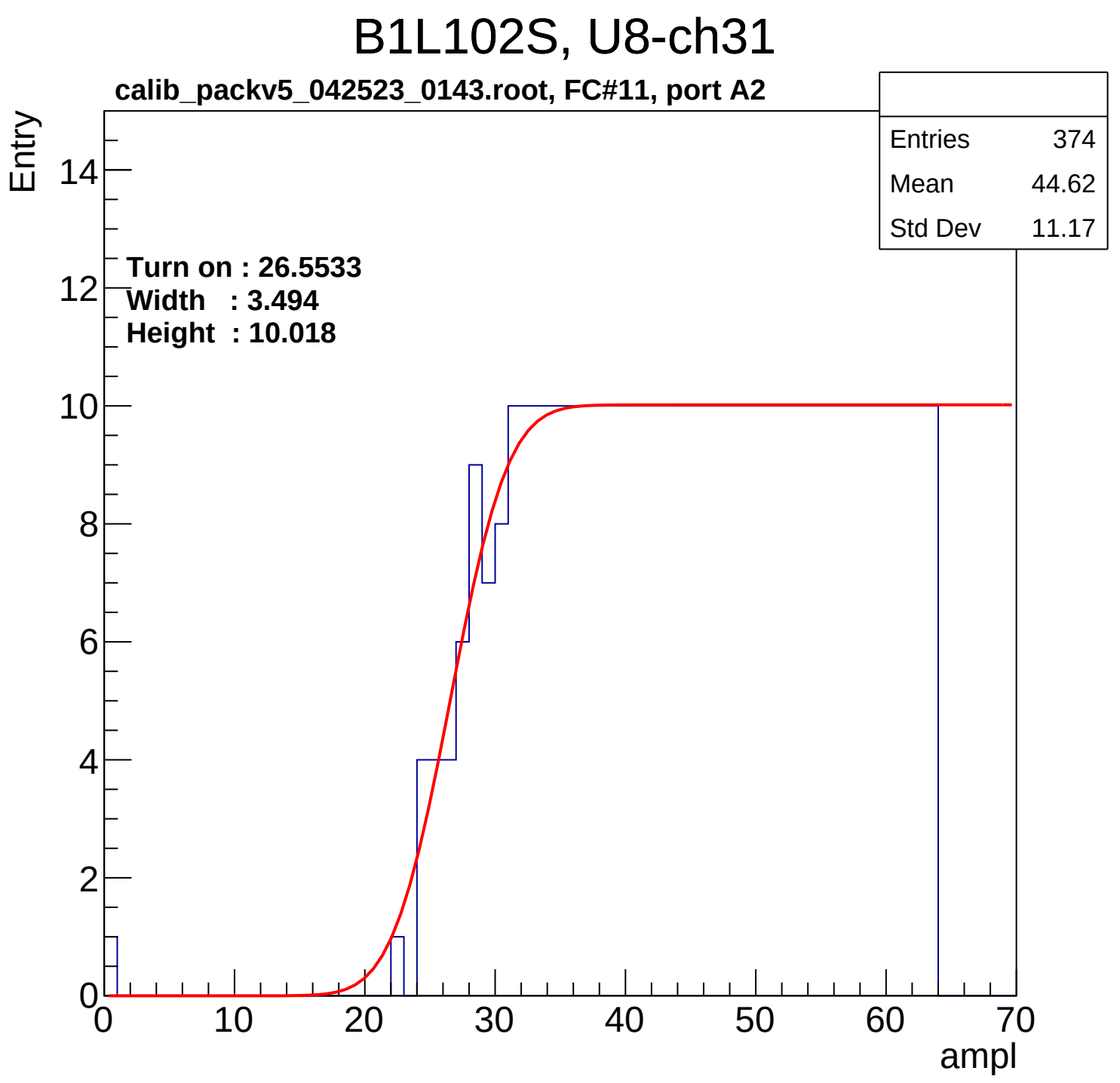
B1L102S, U8-ch31
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.62
Std Dev 11.17
Turn on : 26.5533
Width : 3.494
Height : 10.018
Entry
ampl
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4
6
8
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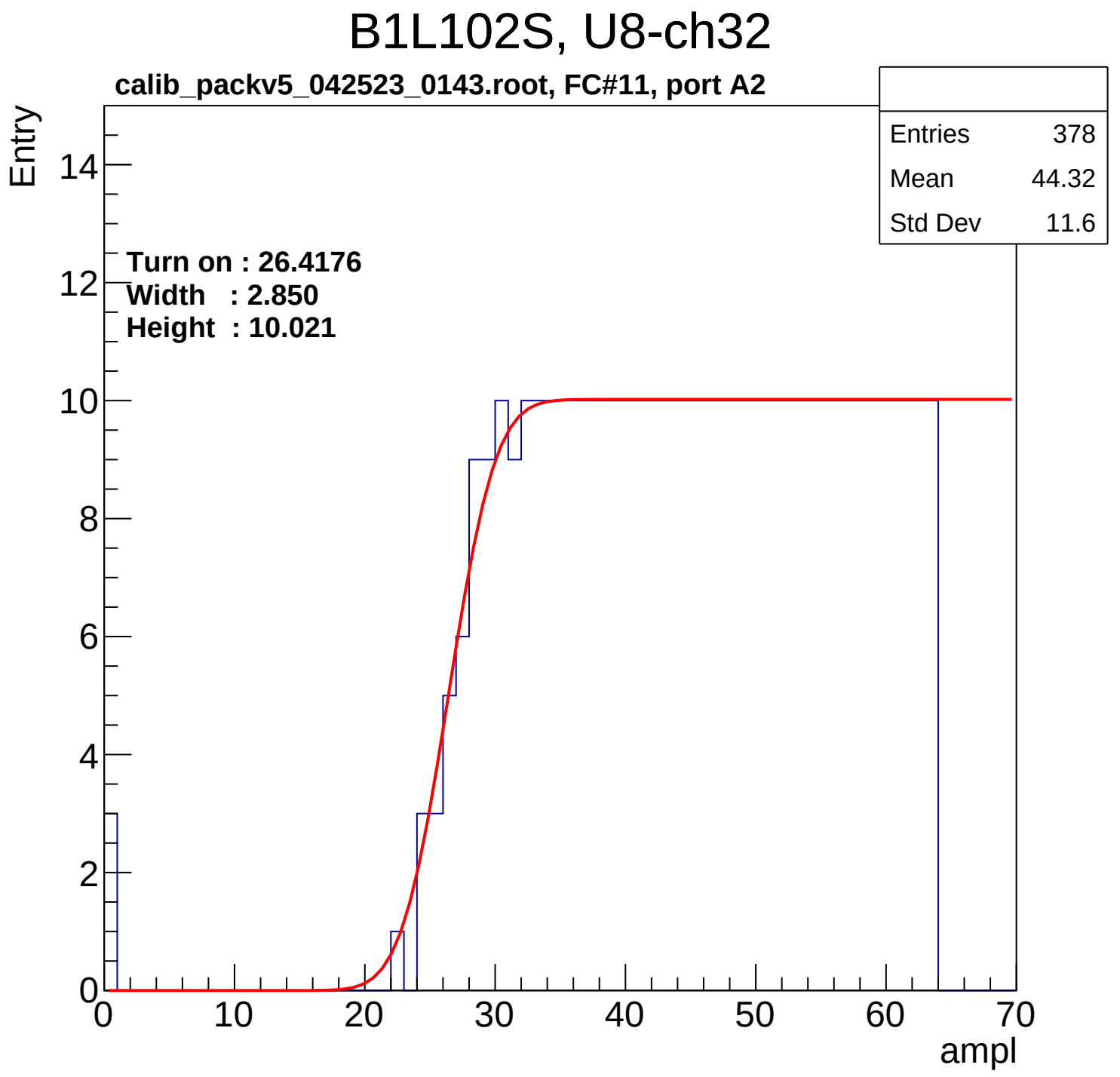
B1L102S, U8-ch32
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.32
Std Dev 11.6
Turn on : 26.4176
Width : 2.850
Height : 10.021
Entry
ampl
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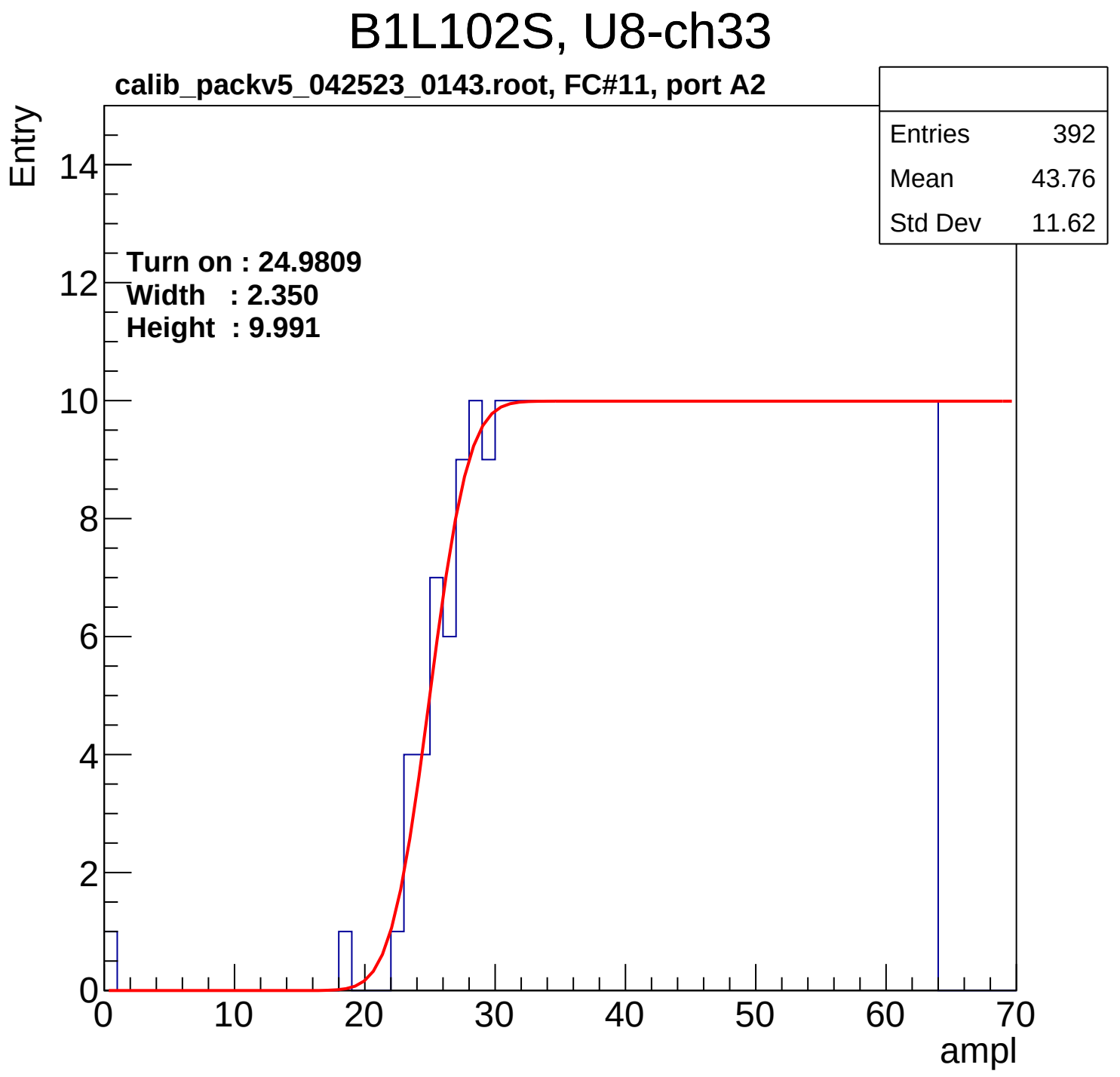
B1L102S, U8-ch33
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.76
Std Dev 11.62
Turn on : 24.9809
Width : 2.350
Height : 9.991
Entry
ampl
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6
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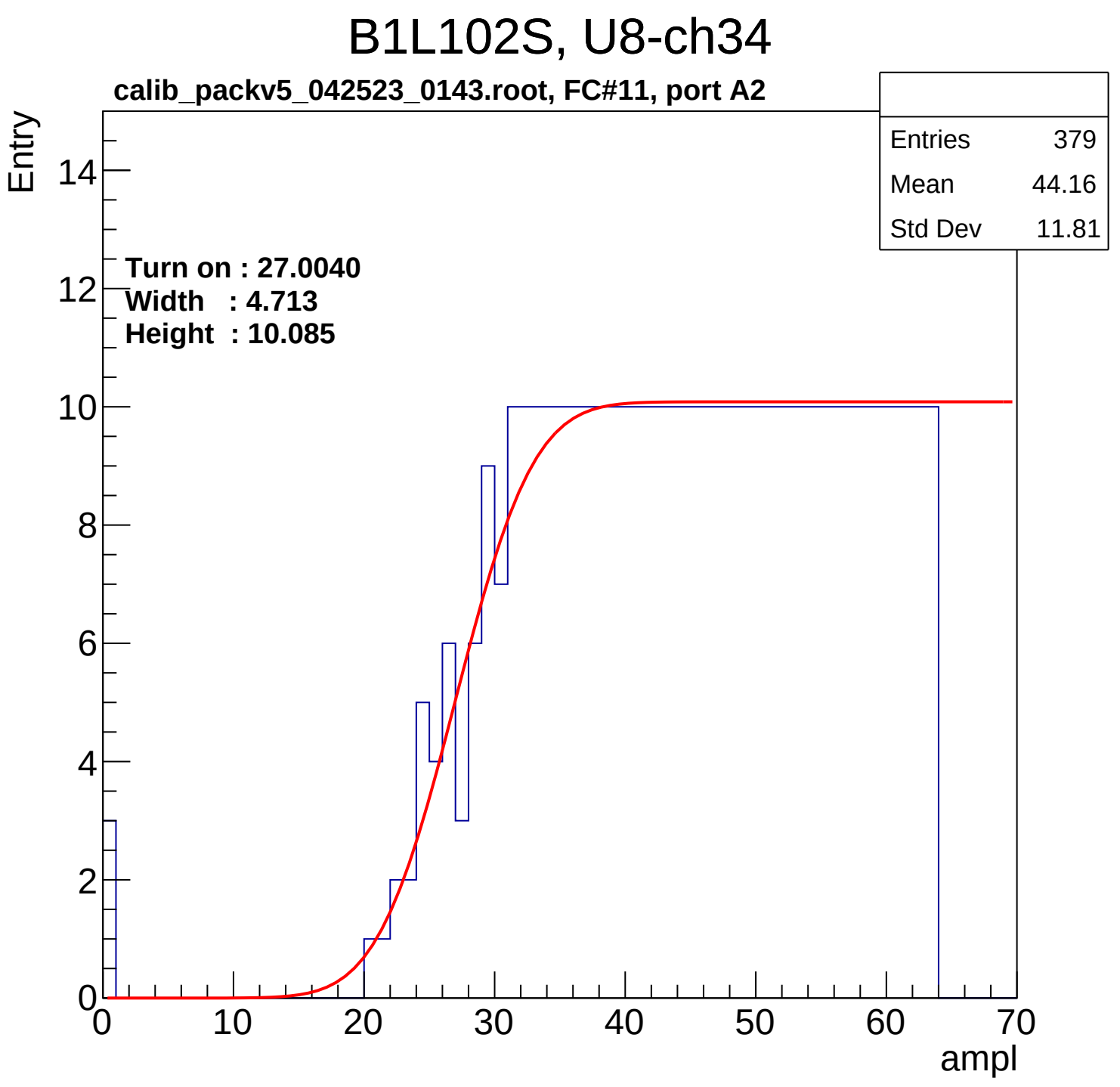
B1L102S, U8-ch34
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.16
Std Dev 11.81
Turn on : 27.0040
Width : 4.713
Height : 10.085
Entry
ampl
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2
4
6
8
10
12
14
0
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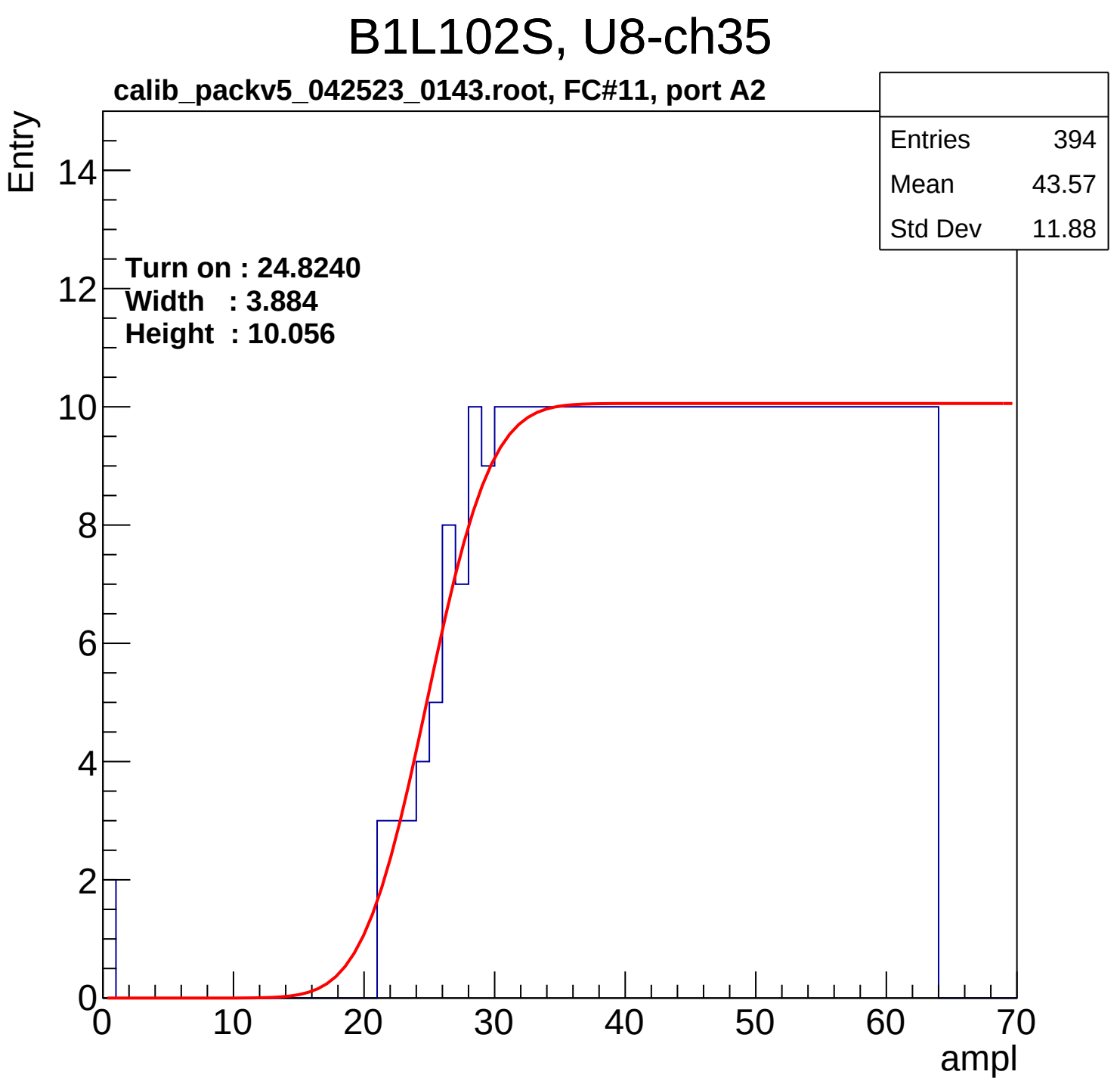
B1L102S, U8-ch35
calib_packv5_042523_0143.root, FC#11, port A2
Entries 394
Mean 43.57
Std Dev 11.88
Turn on : 24.8240
Width : 3.884
Height : 10.056
Entry
ampl
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6
8
10
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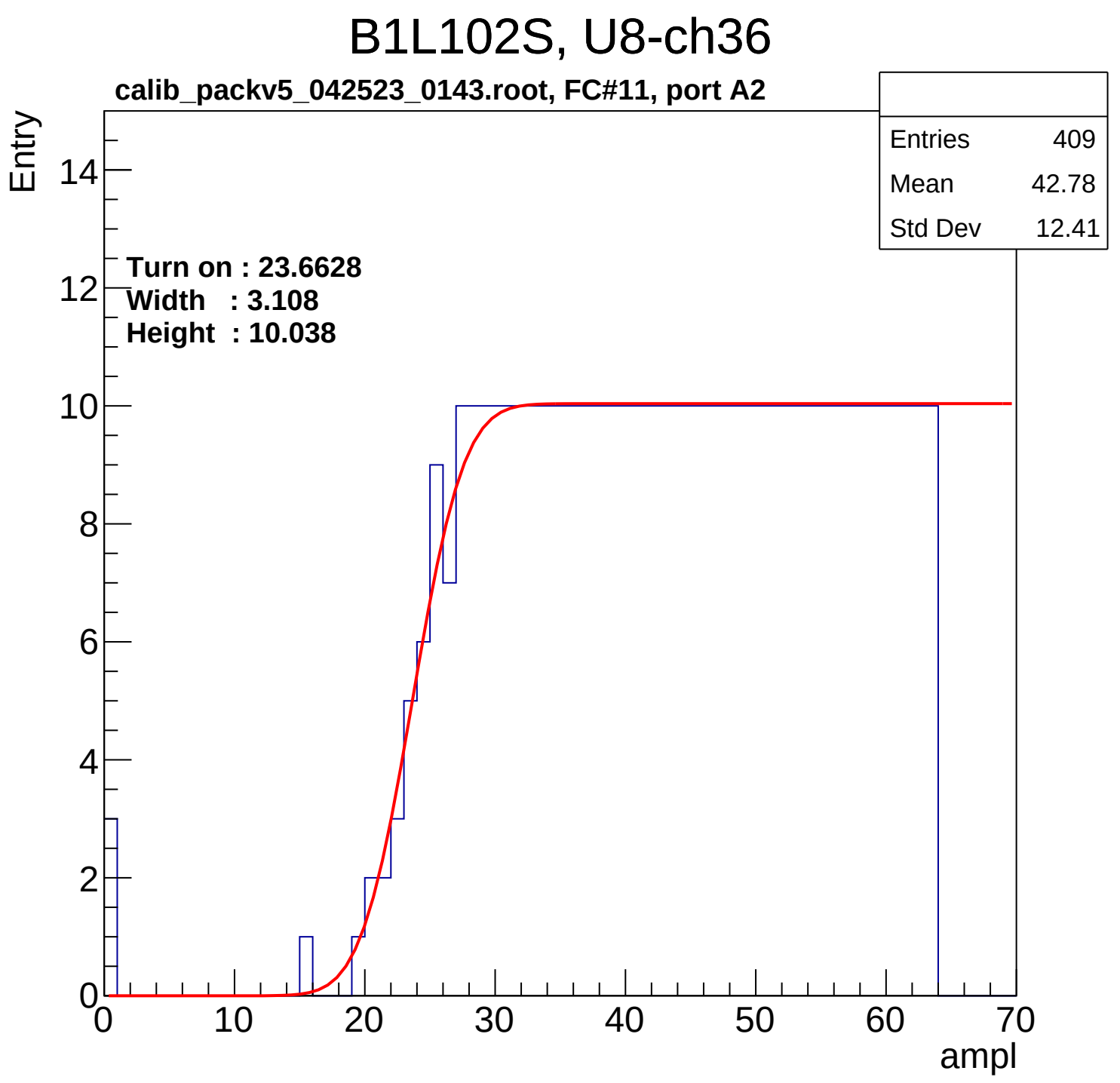
B1L102S, U8-ch36
calib_packv5_042523_0143.root, FC#11, port A2
Entries 409
Mean 42.78
Std Dev 12.41
Turn on : 23.6628
Width : 3.108
Height : 10.038
Entry
ampl
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2
4
6
8
10
12
14
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10
20
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60
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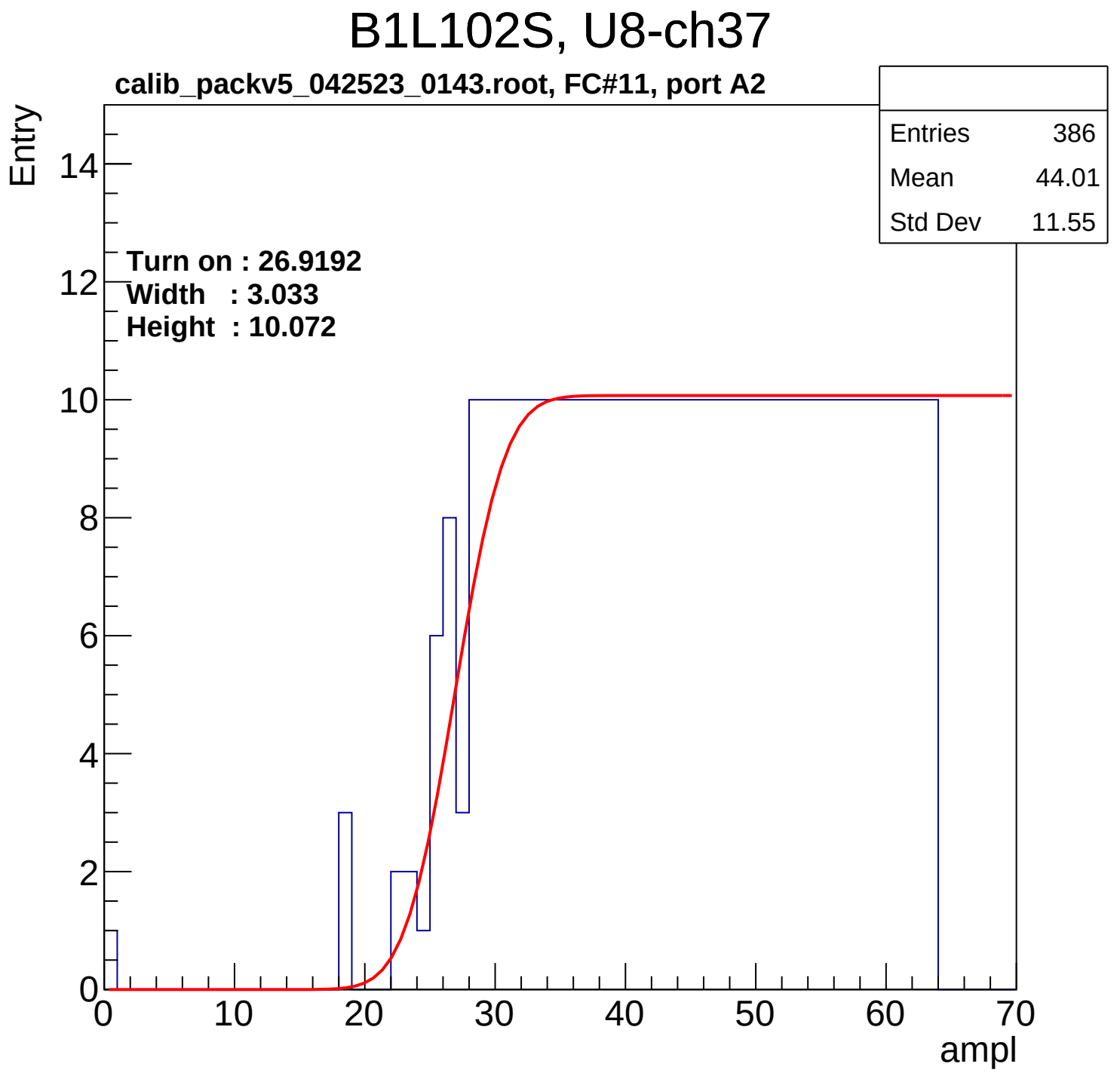
B1L102S, U8-ch37
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 44.01
Std Dev 11.55
Turn on : 26.9192
Width : 3.033
Height : 10.072
Entry
ampl
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4
6
8
10
12
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20
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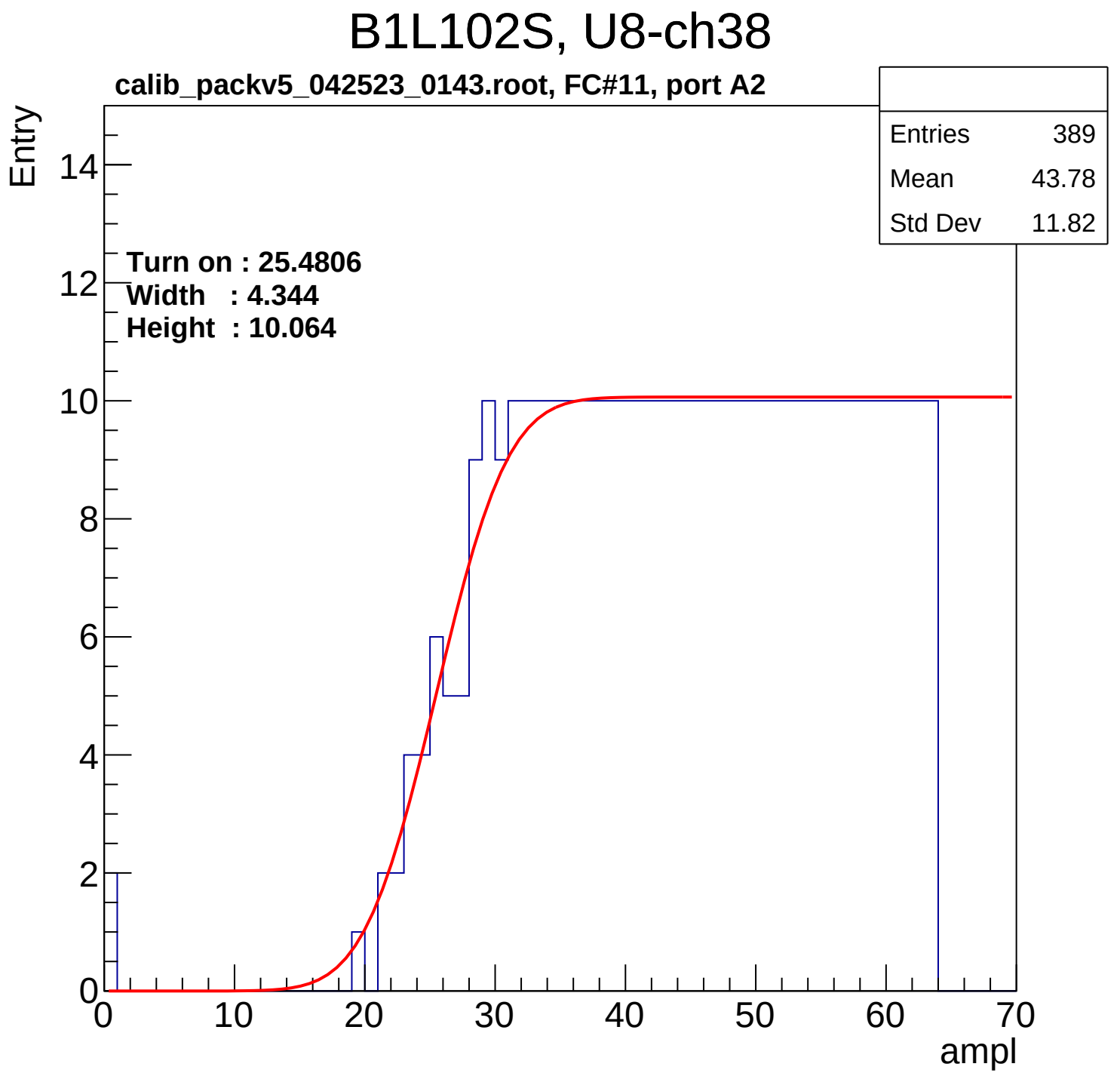
B1L102S, U8-ch38
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.78
Std Dev 11.82
Turn on : 25.4806
Width : 4.344
Height : 10.064
Entry
ampl
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6
8
10
12
14
0
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20
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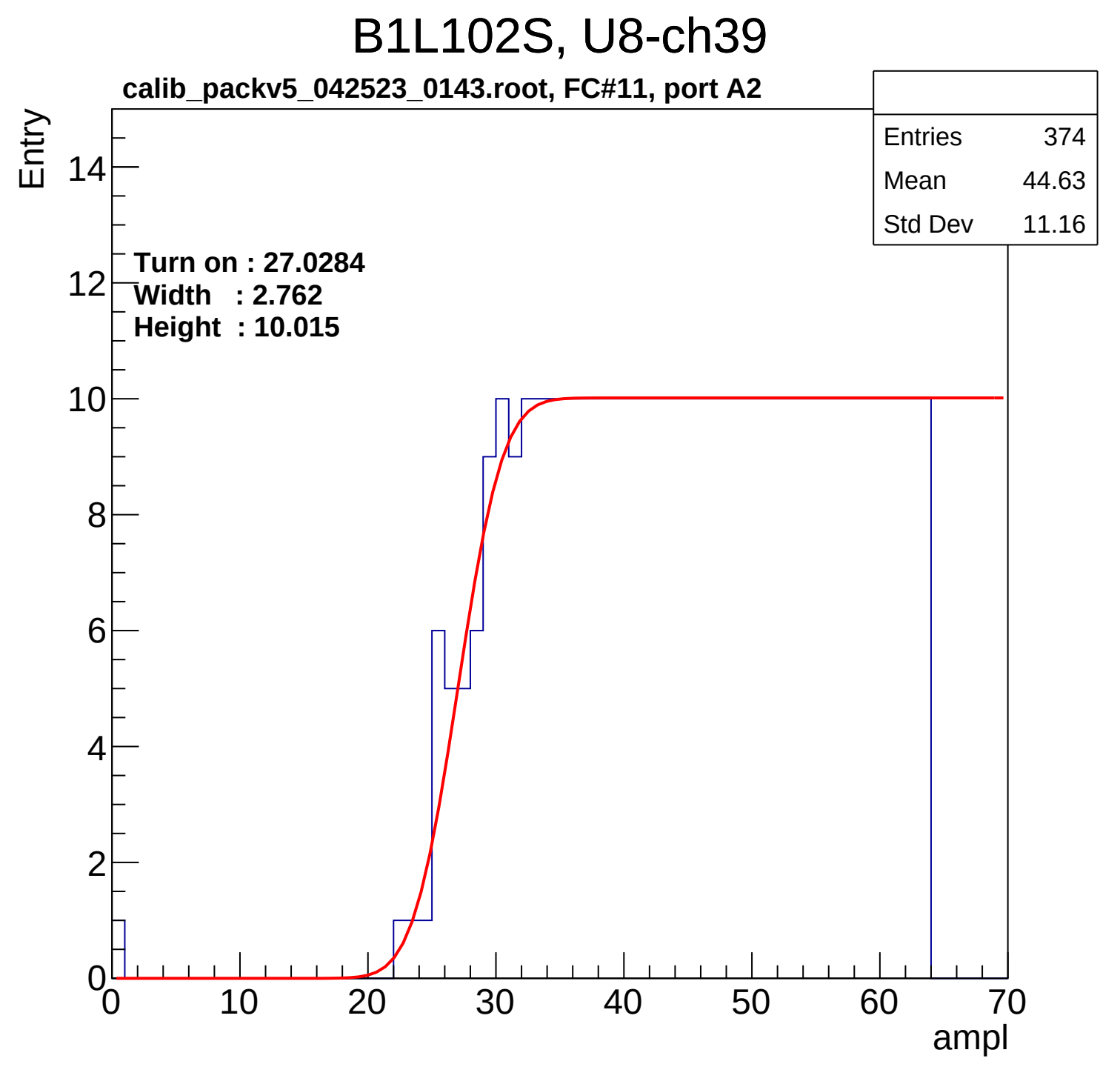
B1L102S, U8-ch39
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.63
Std Dev 11.16
Turn on : 27.0284
Width : 2.762
Height : 10.015
Entry
ampl
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2
4
6
8
10
12
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0
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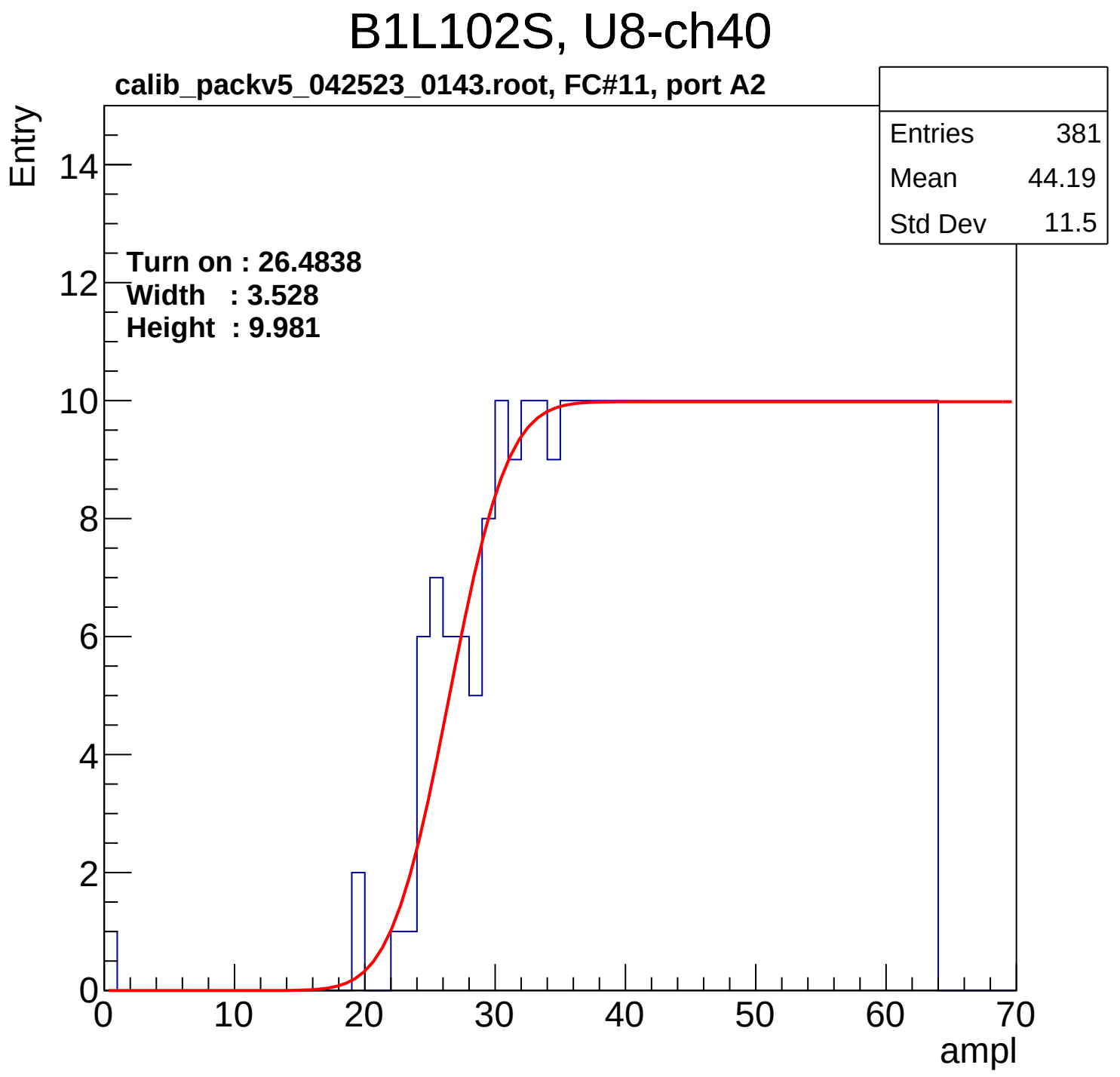
B1L102S, U8-ch40
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.19
Std Dev 11.5
Turn on : 26.4838
Width : 3.528
Height : 9.981
Entry
ampl
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4
6
8
10
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0
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20
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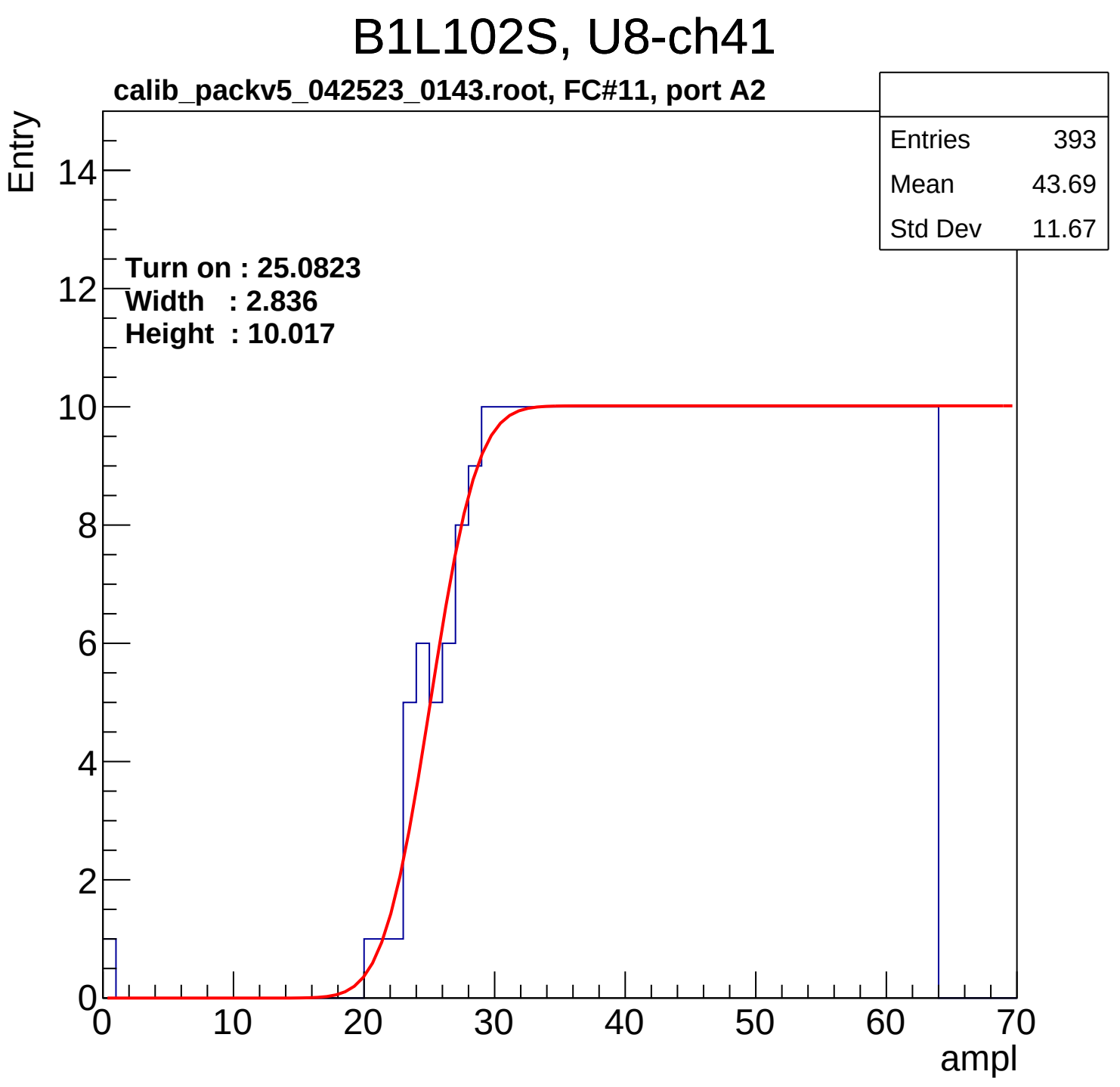
B1L102S, U8-ch41
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.69
Std Dev 11.67
Turn on : 25.0823
Width : 2.836
Height : 10.017
Entry
ampl
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6
8
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12
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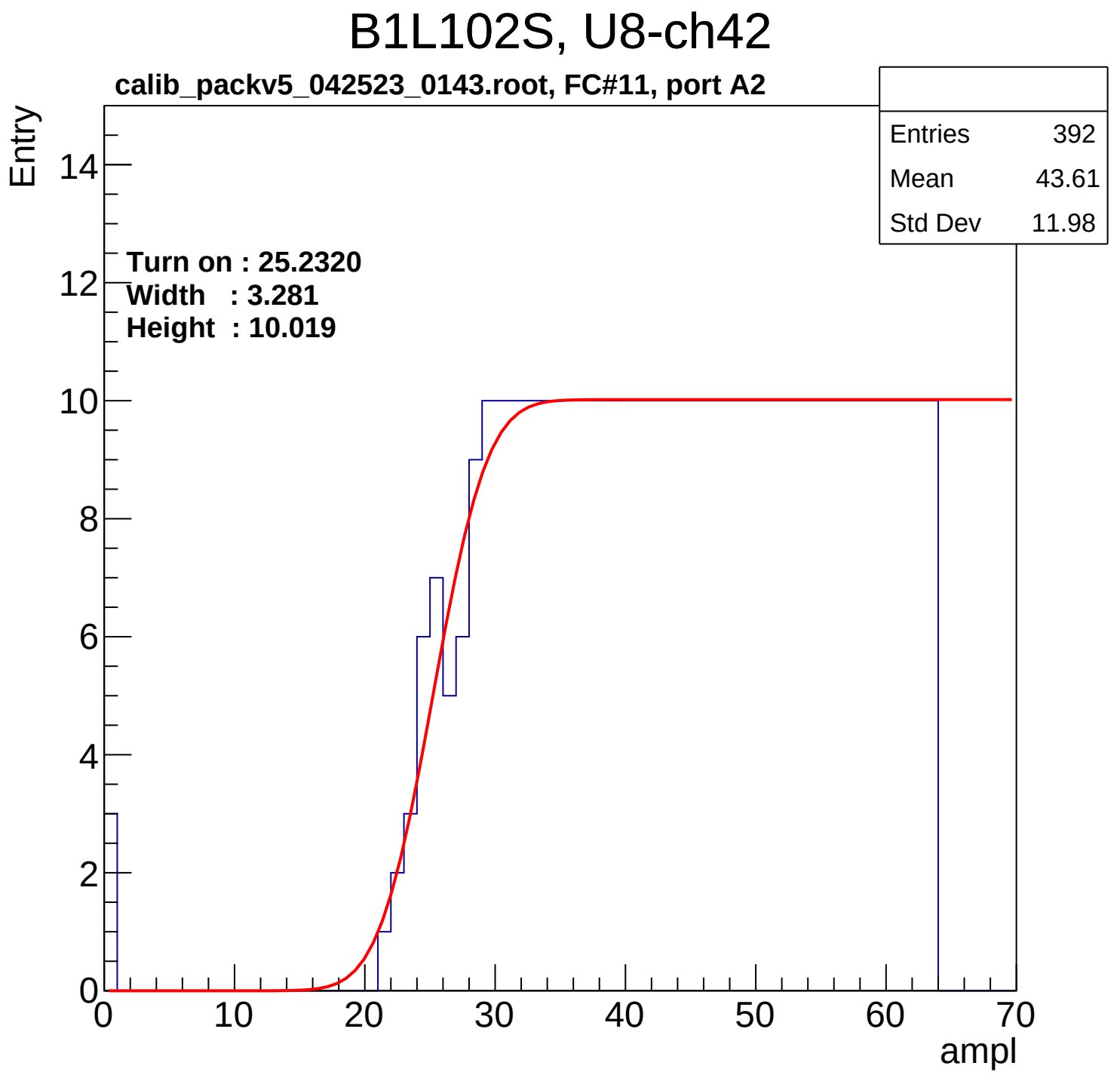
B1L102S, U8-ch42
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.61
Std Dev 11.98
Turn on : 25.2320
Width : 3.281
Height : 10.019
Entry
ampl
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4
6
8
10
12
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0
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60
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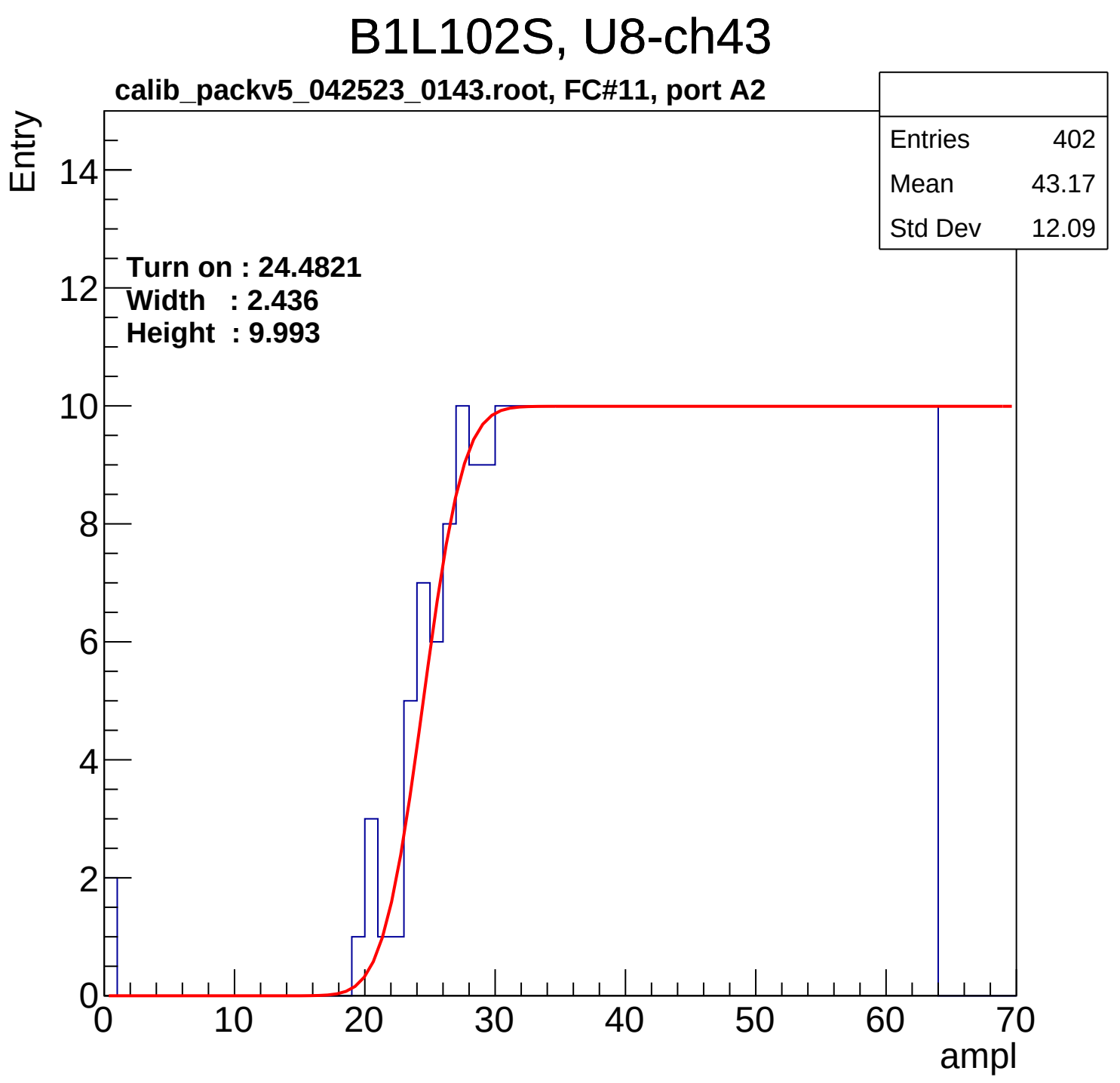
B1L102S, U8-ch43
calib_packv5_042523_0143.root, FC#11, port A2
Entries 402
Mean 43.17
Std Dev 12.09
Turn on : 24.4821
Width : 2.436
Height : 9.993
Entry
ampl
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6
8
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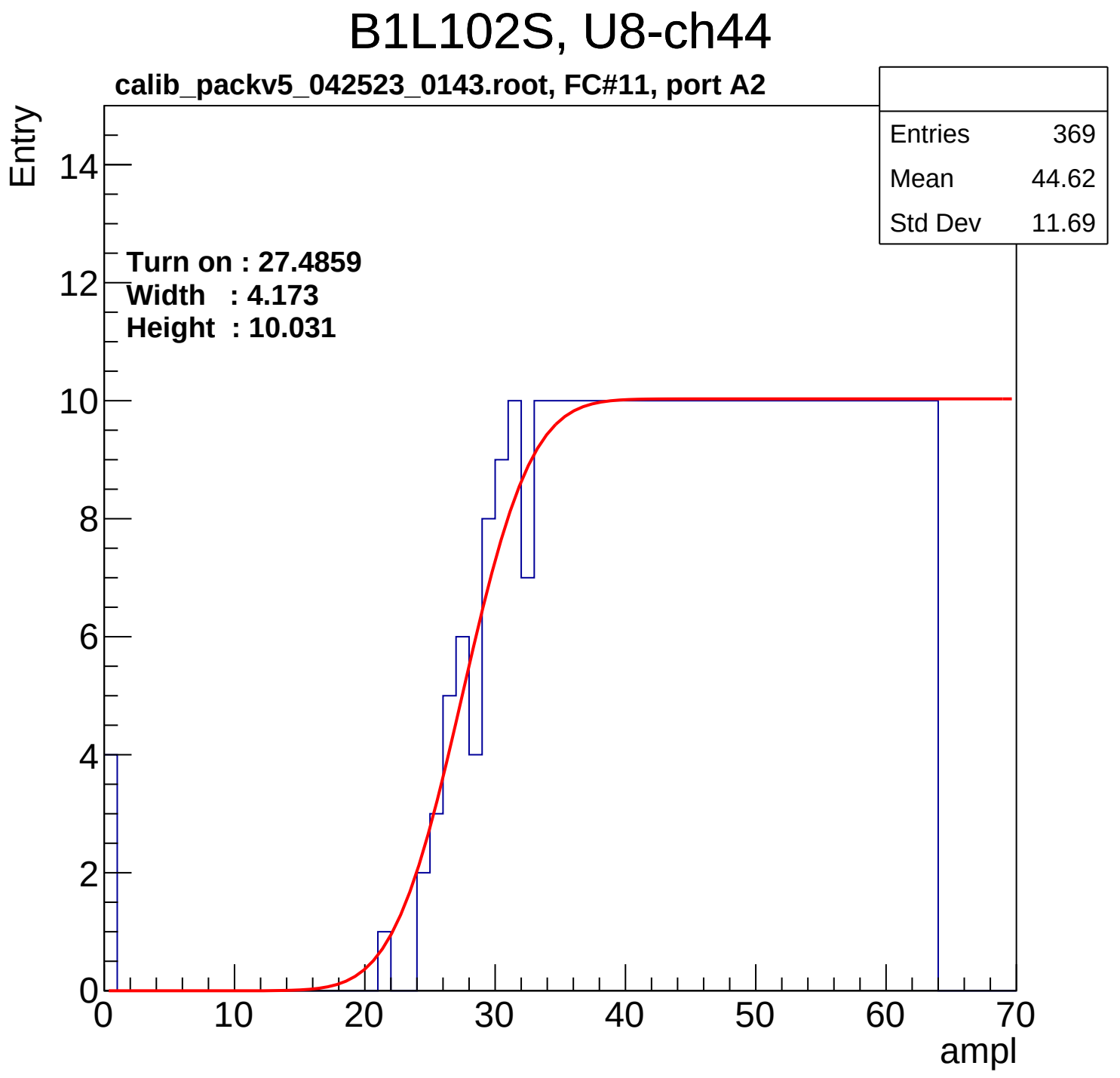
B1L102S, U8-ch44
calib_packv5_042523_0143.root, FC#11, port A2
Entries 369
Mean 44.62
Std Dev 11.69
Turn on : 27.4859
Width : 4.173
Height : 10.031
Entry
ampl
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6
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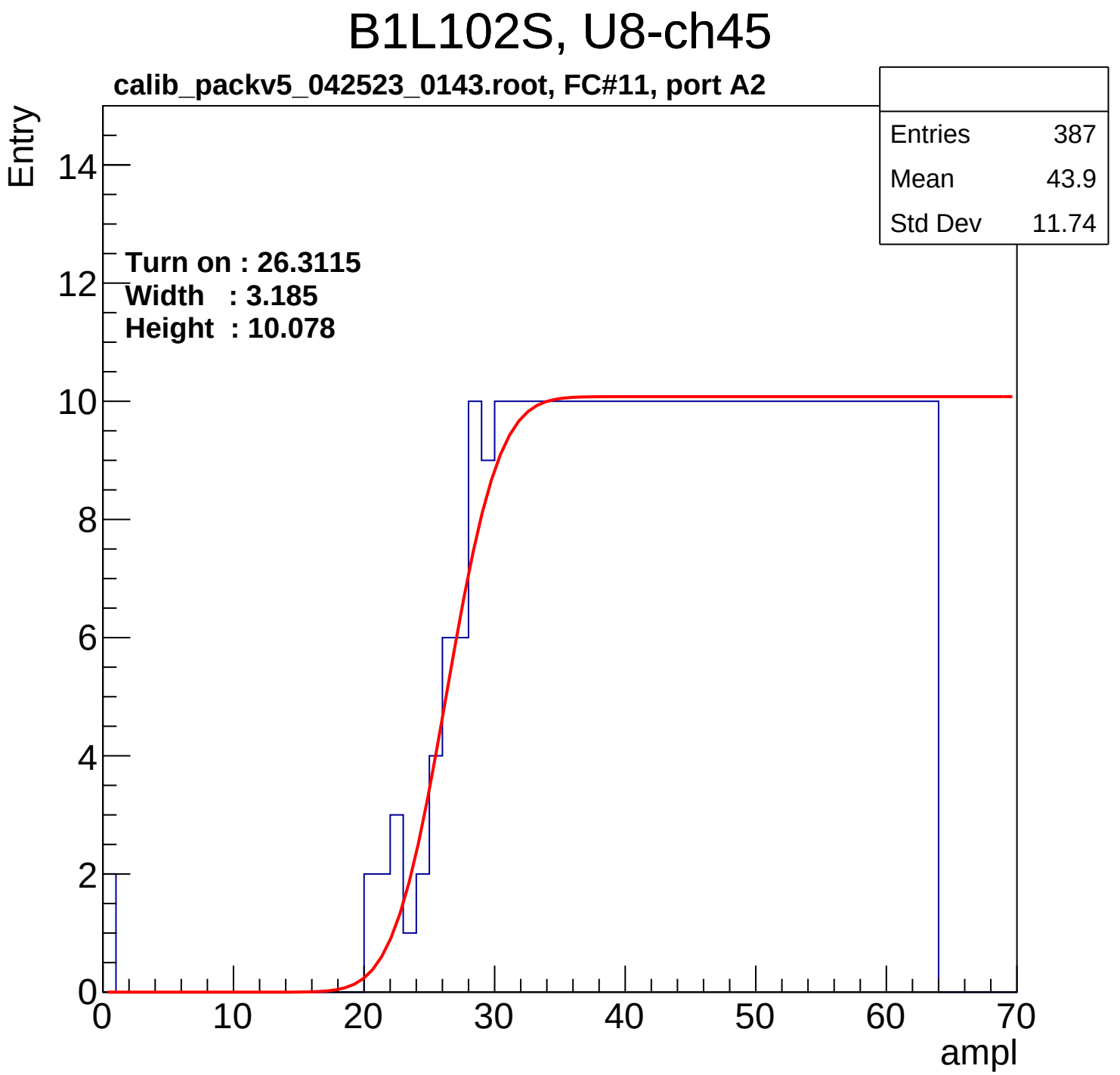
B1L102S, U8-ch45
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.9
Std Dev 11.74
Turn on : 26.3115
Width : 3.185
Height : 10.078
Entry
ampl
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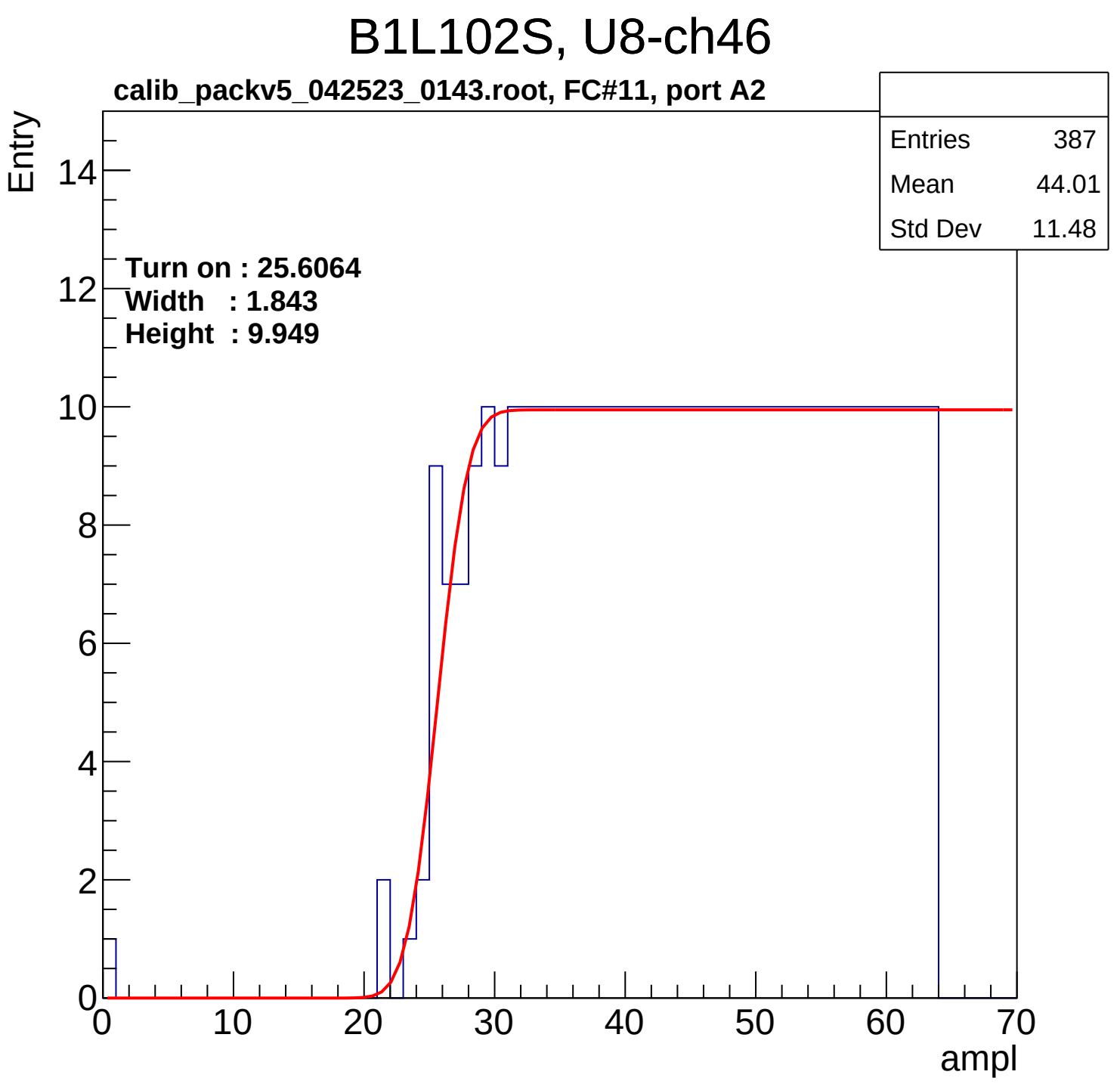
B1L102S, U8-ch46
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 44.01
Std Dev 11.48
Turn on : 25.6064
Width : 1.843
Height : 9.949
Entry
ampl
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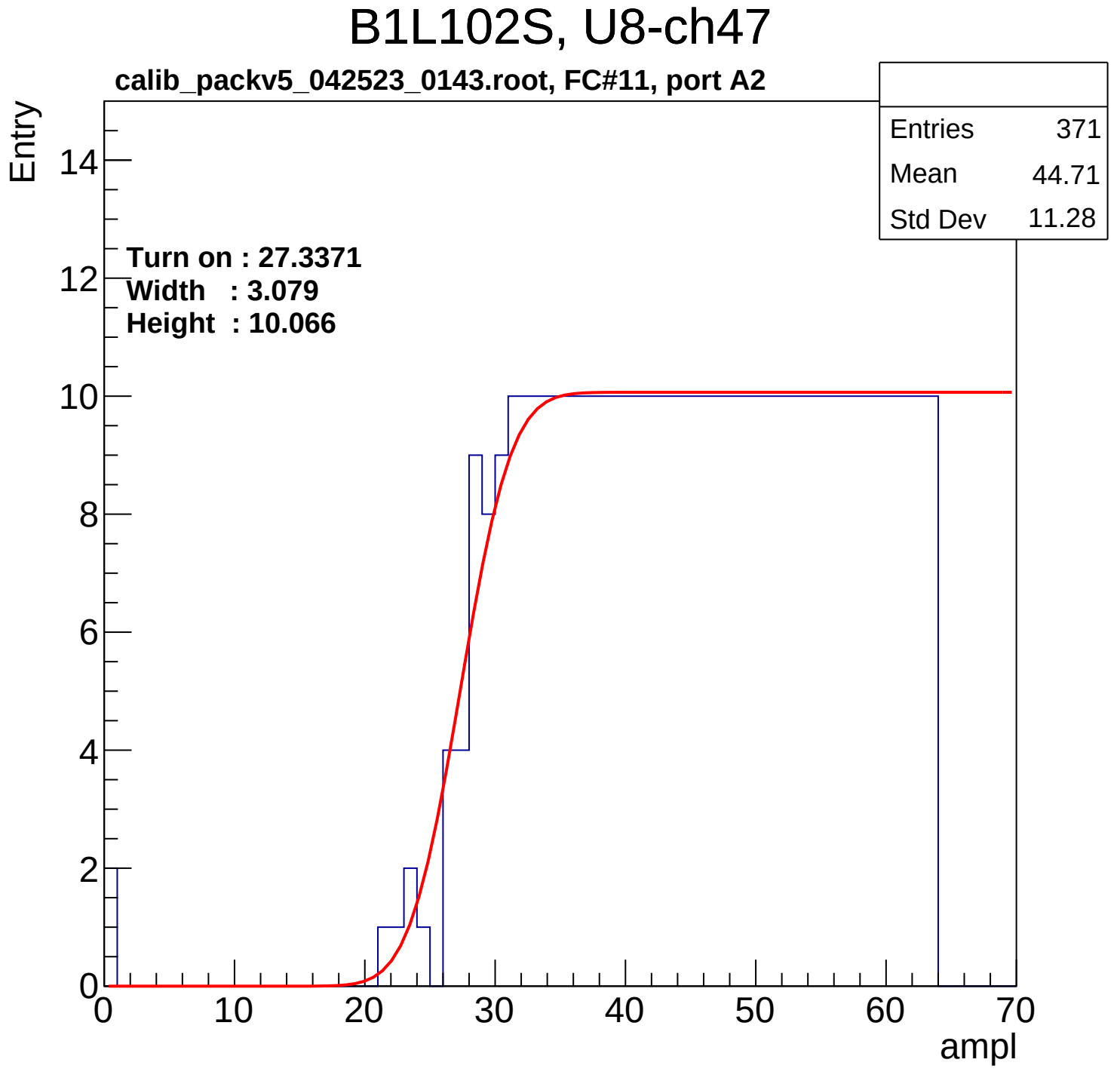
B1L102S, U8-ch47
calib_packv5_042523_0143.root, FC#11, port A2
Entries 371
Mean 44.71
Std Dev 11.28
Turn on : 27.3371
Width : 3.079
Height : 10.066
Entry
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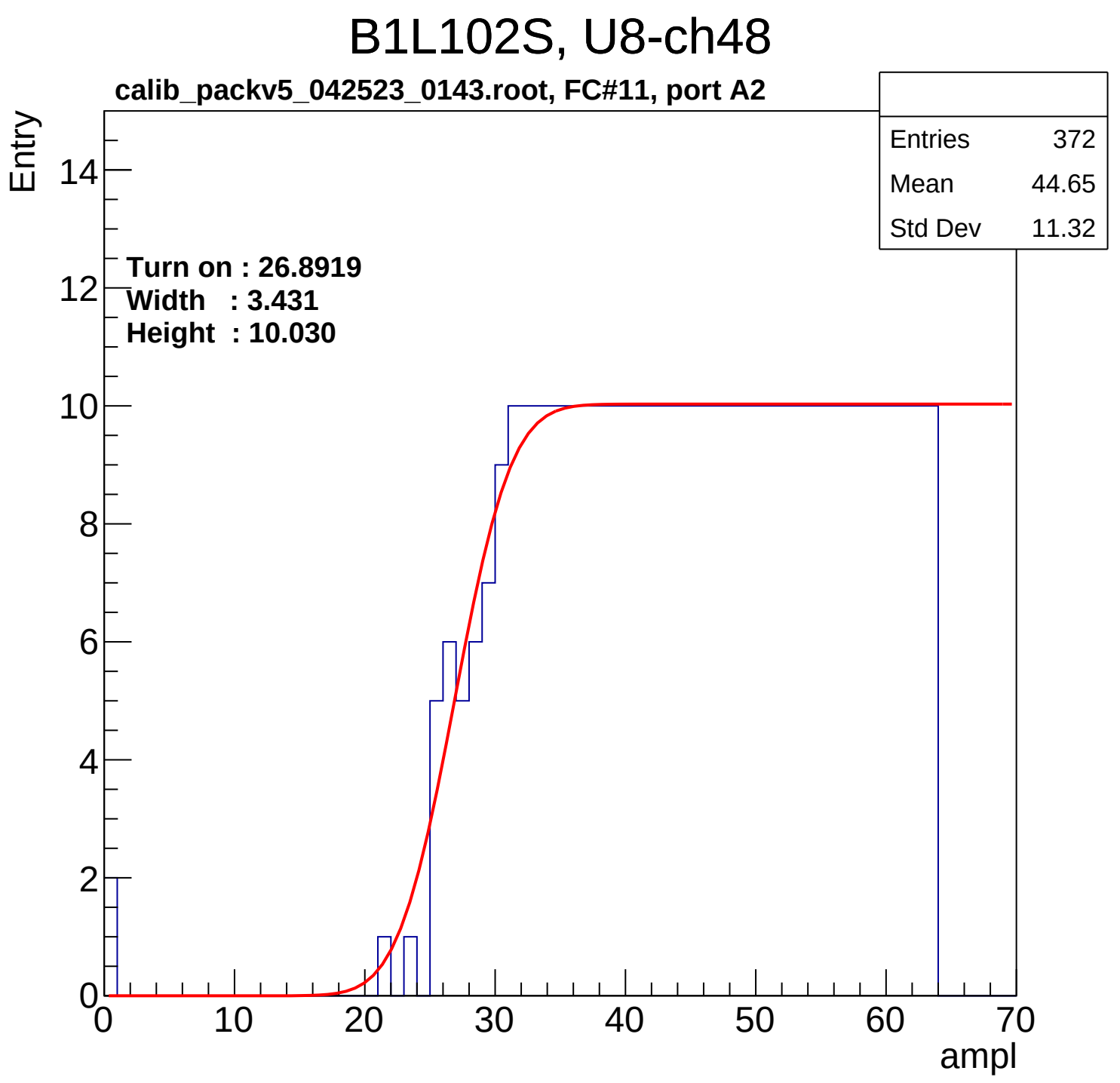
B1L102S, U8-ch48
calib_packv5_042523_0143.root, FC#11, port A2
Entries 372
Mean 44.65
Std Dev 11.32
Turn on : 26.8919
Width : 3.431
Height : 10.030
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ampl
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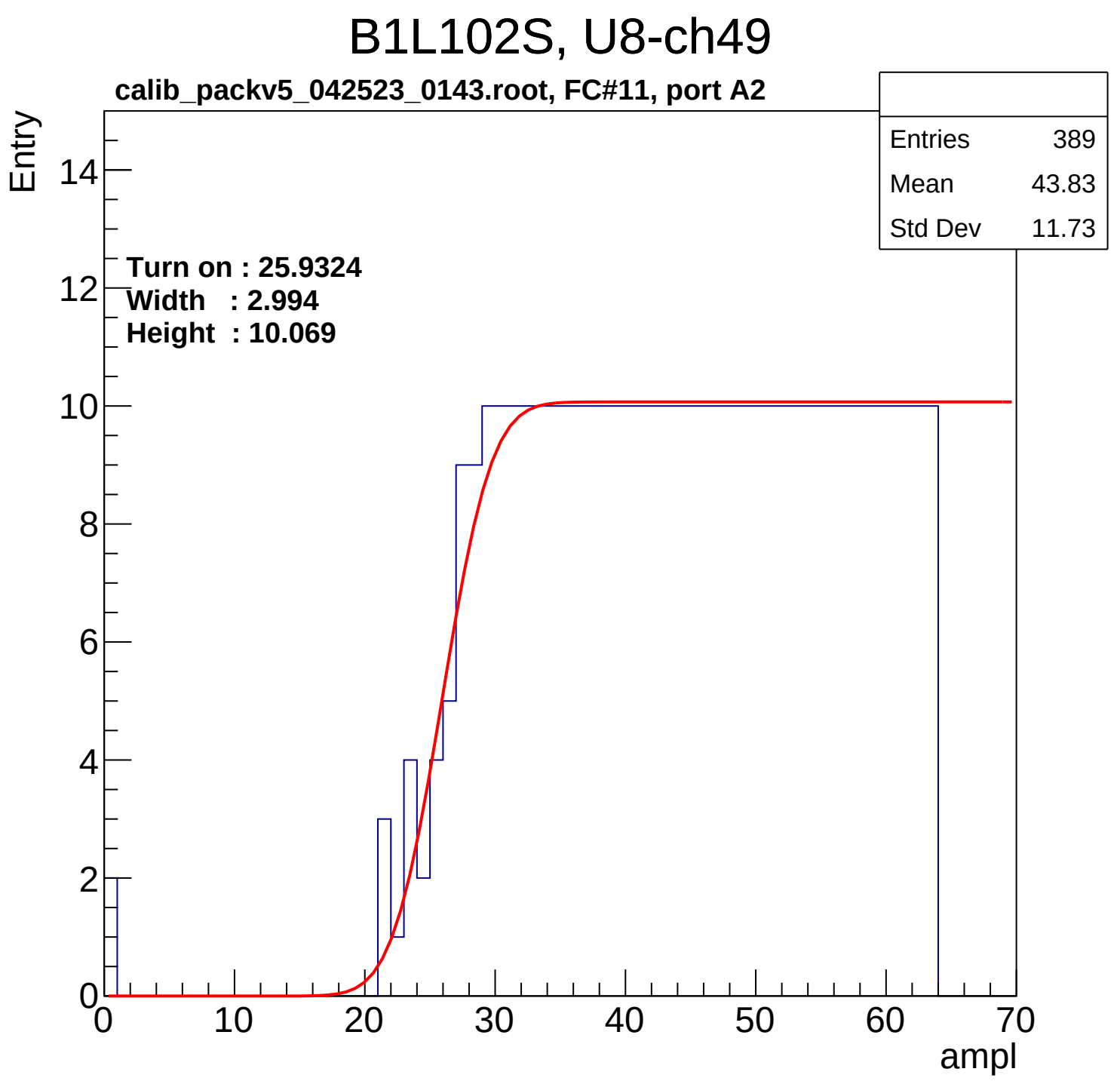
B1L102S, U8-ch49
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.83
Std Dev 11.73
Turn on : 25.9324
Width : 2.994
Height : 10.069
Entry
ampl
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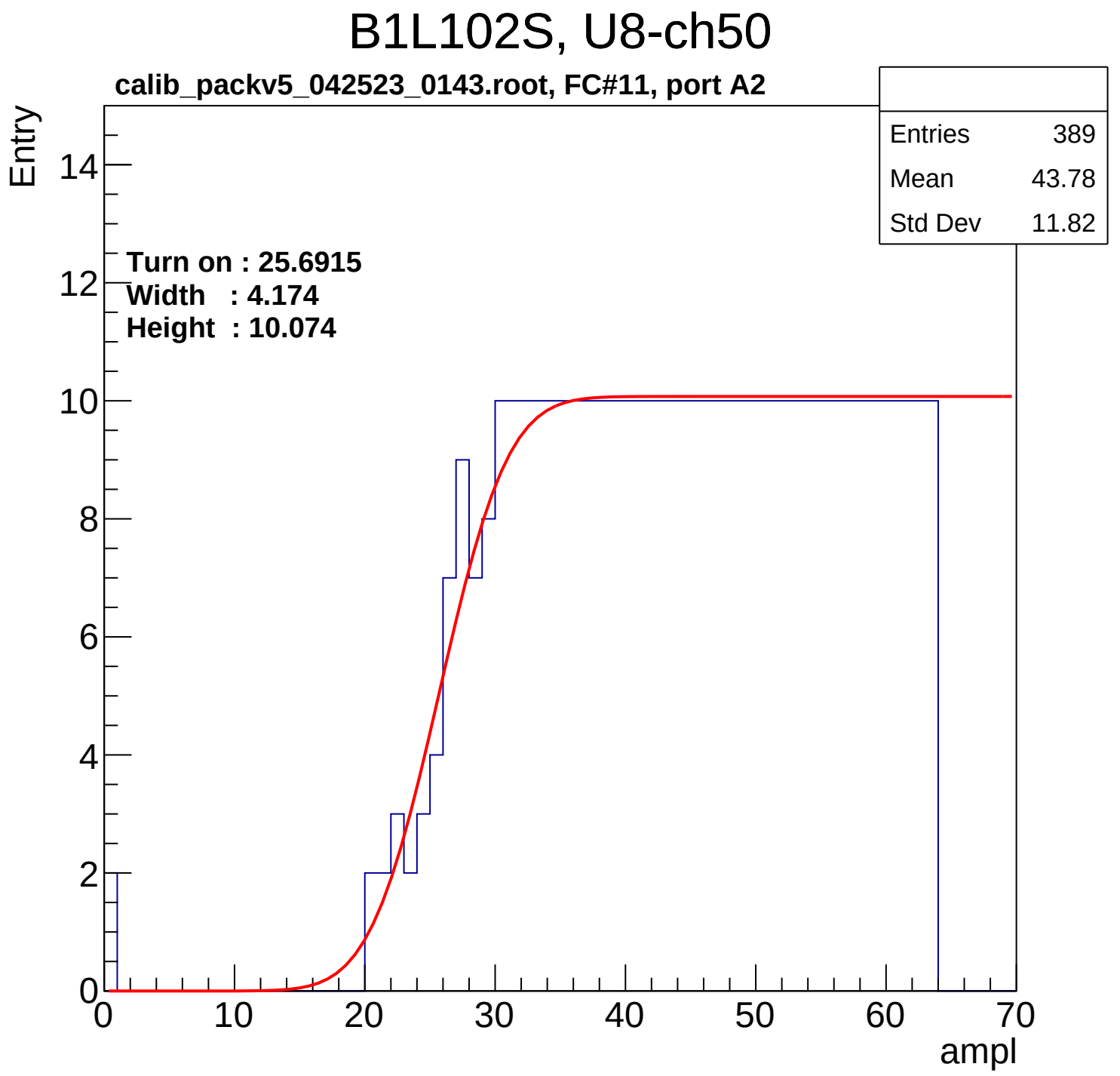
B1L102S, U8-ch50
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.78
Std Dev 11.82
Turn on : 25.6915
Width : 4.174
Height : 10.074
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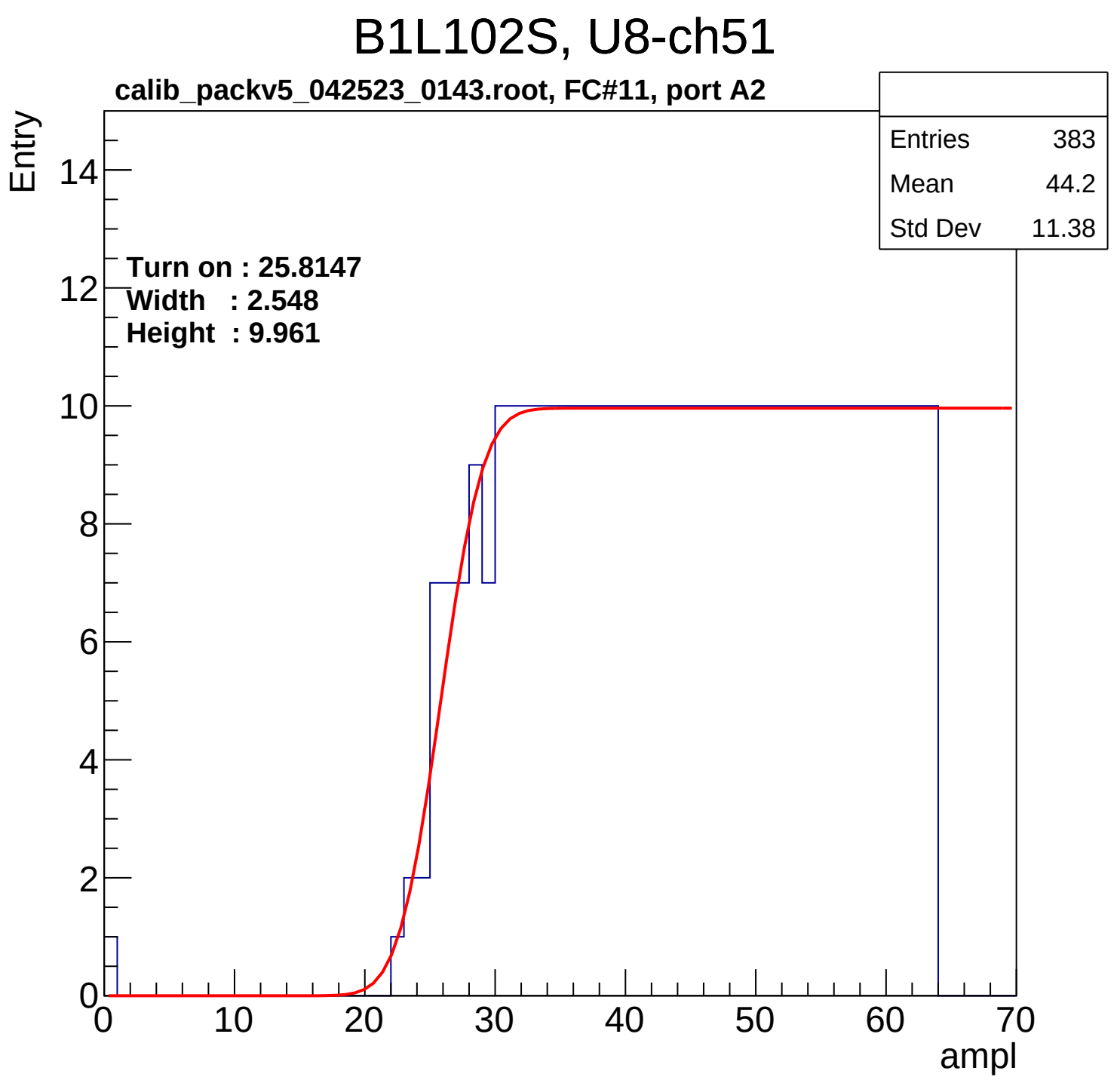
B1L102S, U8-ch51
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.2
Std Dev 11.38
Turn on : 25.8147
Width : 2.548
Height : 9.961
Entry
ampl
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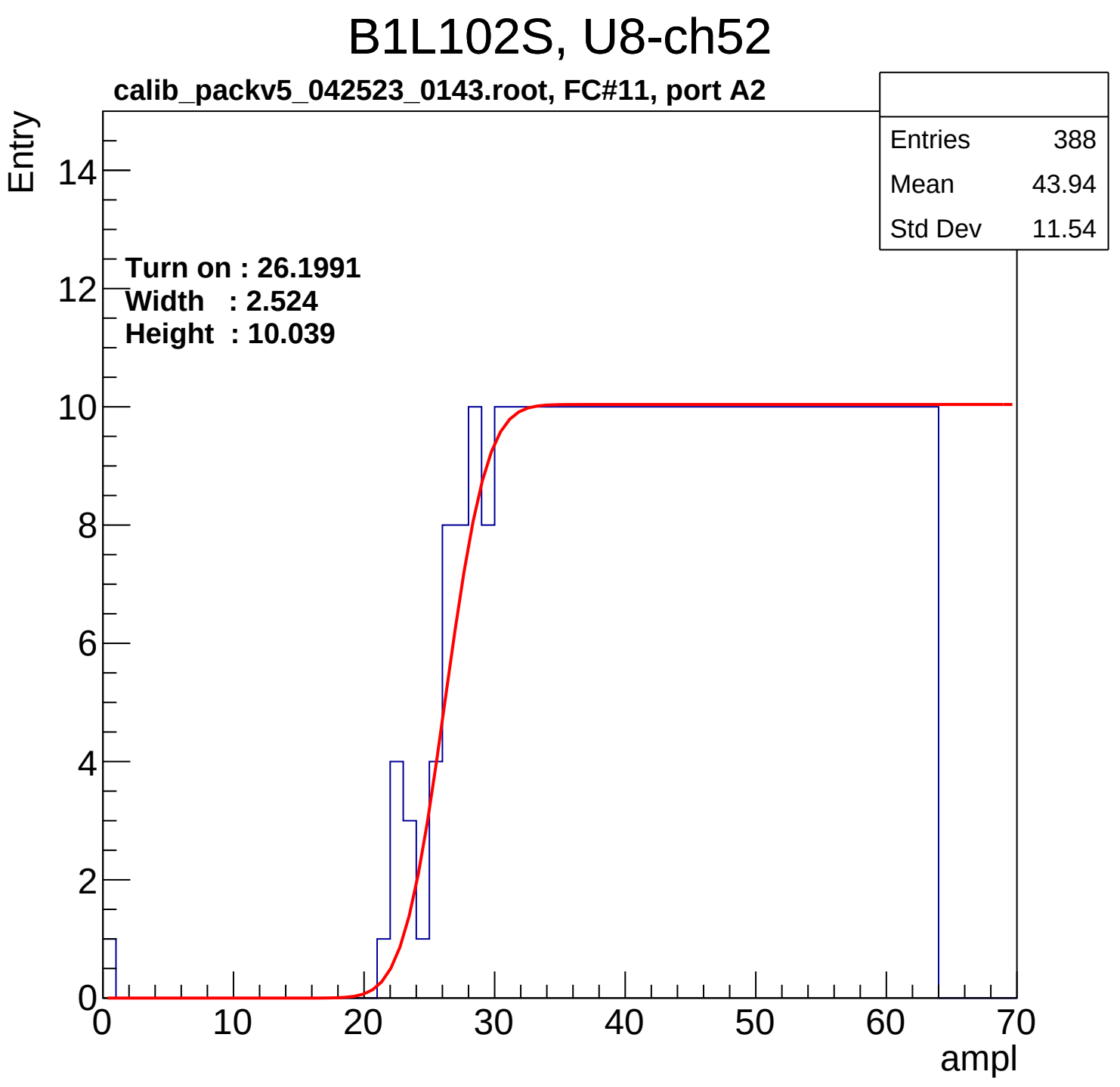
B1L102S, U8-ch52
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.94
Std Dev 11.54
Turn on : 26.1991
Width : 2.524
Height : 10.039
Entry
ampl
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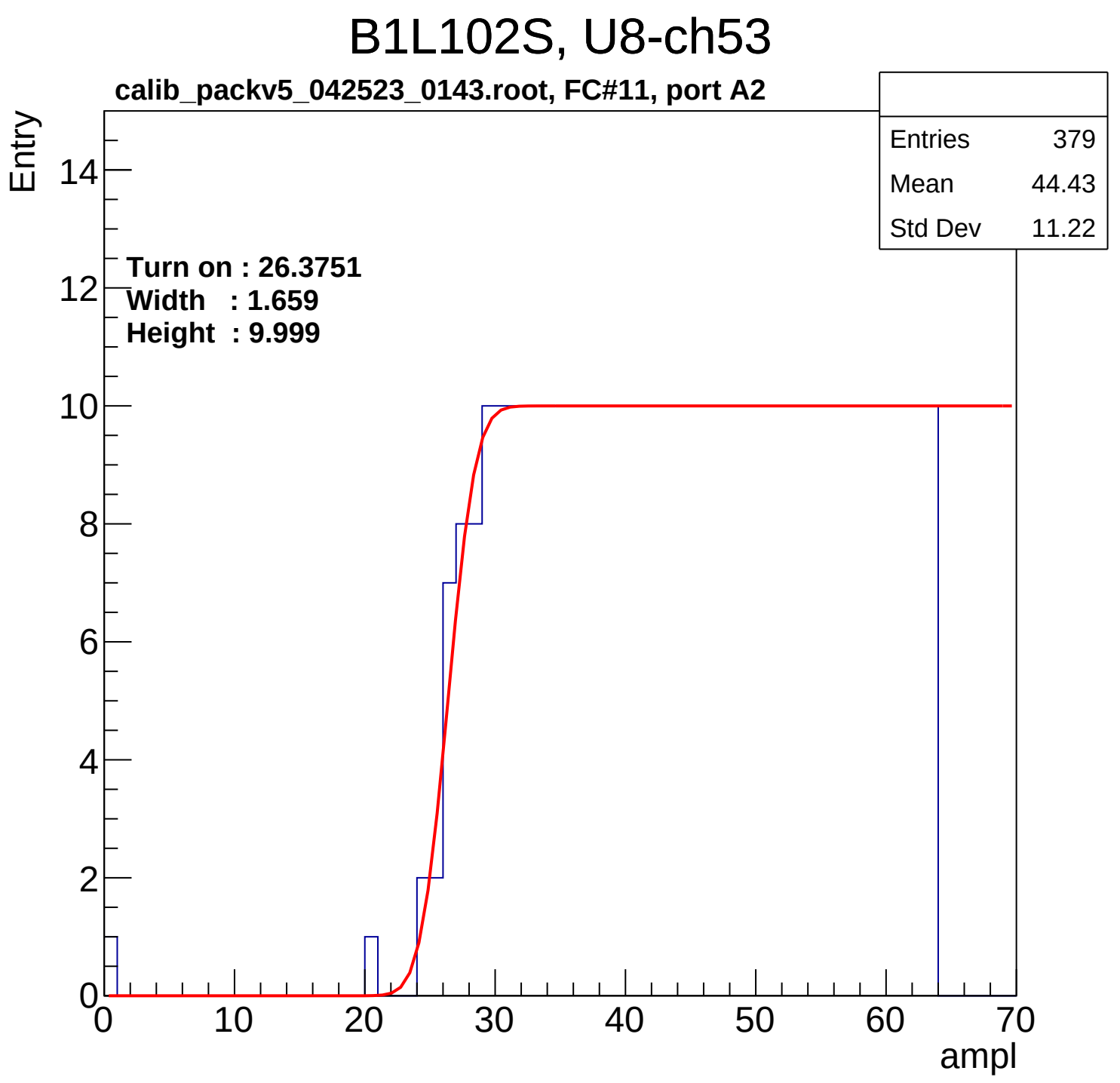
B1L102S, U8-ch53
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.43
Std Dev 11.22
Turn on : 26.3751
Width : 1.659
Height : 9.999
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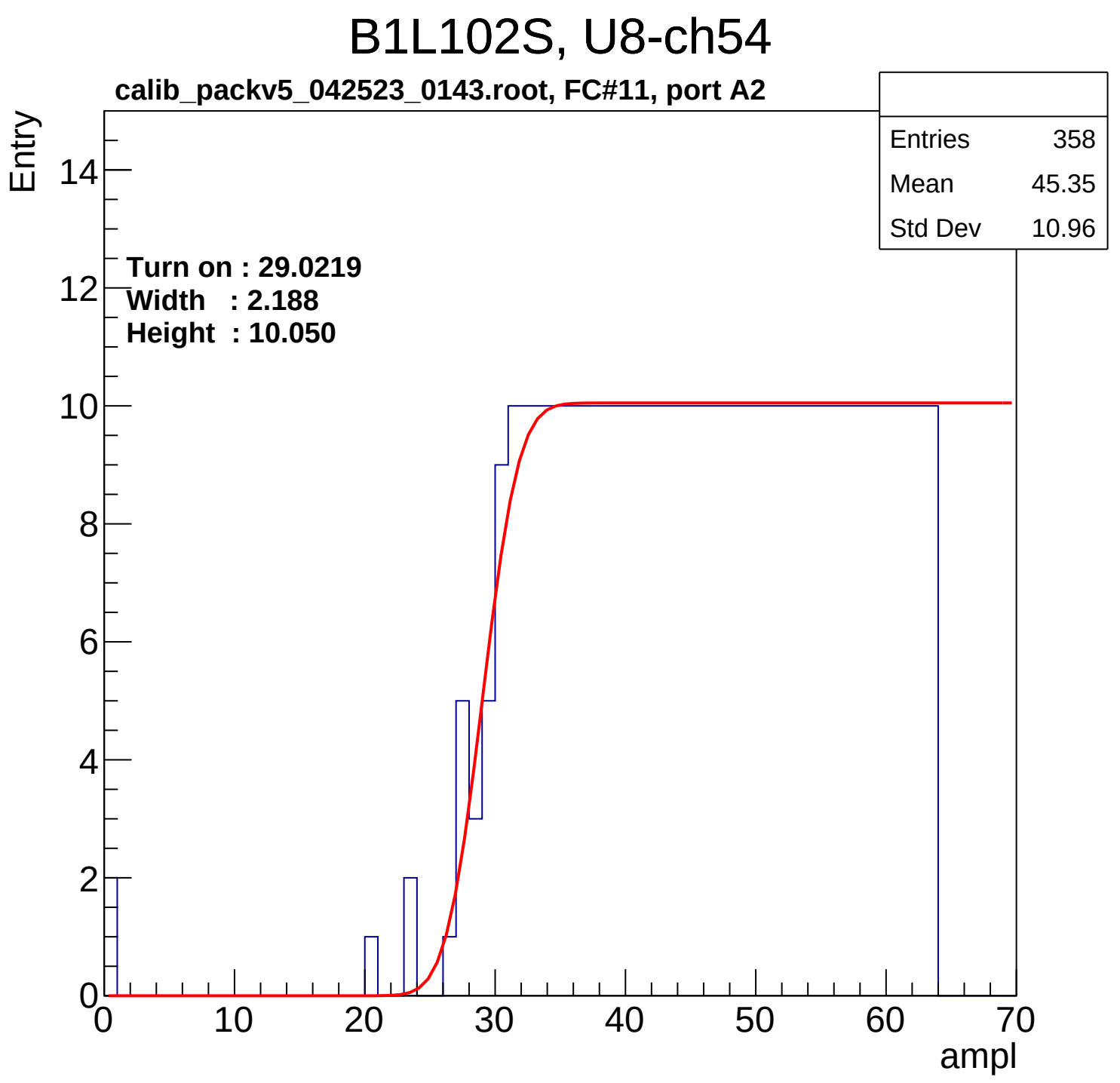
B1L102S, U8-ch54
calib_packv5_042523_0143.root, FC#11, port A2
Entries 358
Mean 45.35
Std Dev 10.96
Turn on : 29.0219
Width : 2.188
Height : 10.050
Entry
ampl
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2
4
6
8
10
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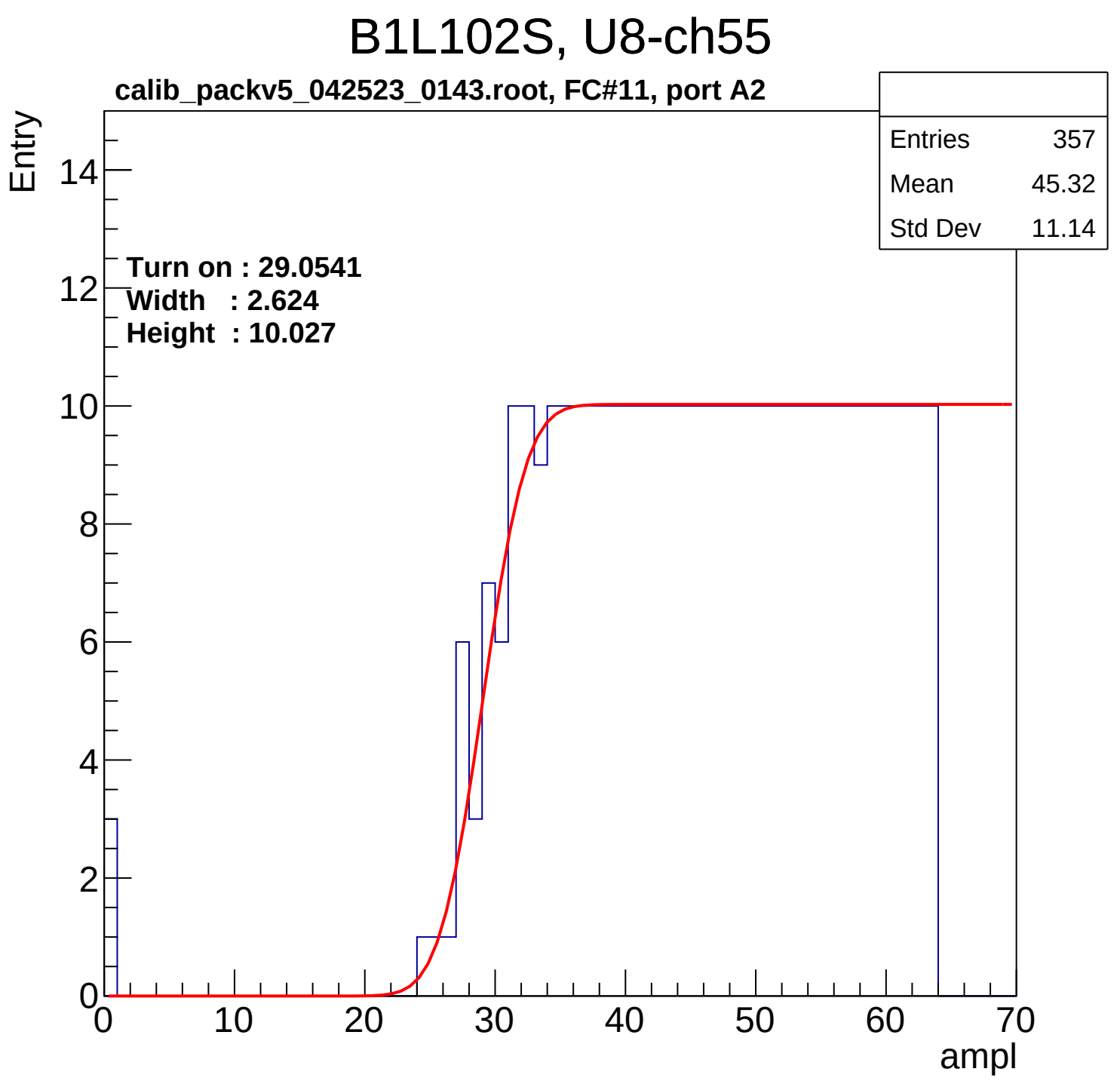
B1L102S, U8-ch55
calib_packv5_042523_0143.root, FC#11, port A2
Entries 357
Mean 45.32
Std Dev 11.14
Turn on : 29.0541
Width : 2.624
Height : 10.027
Entry
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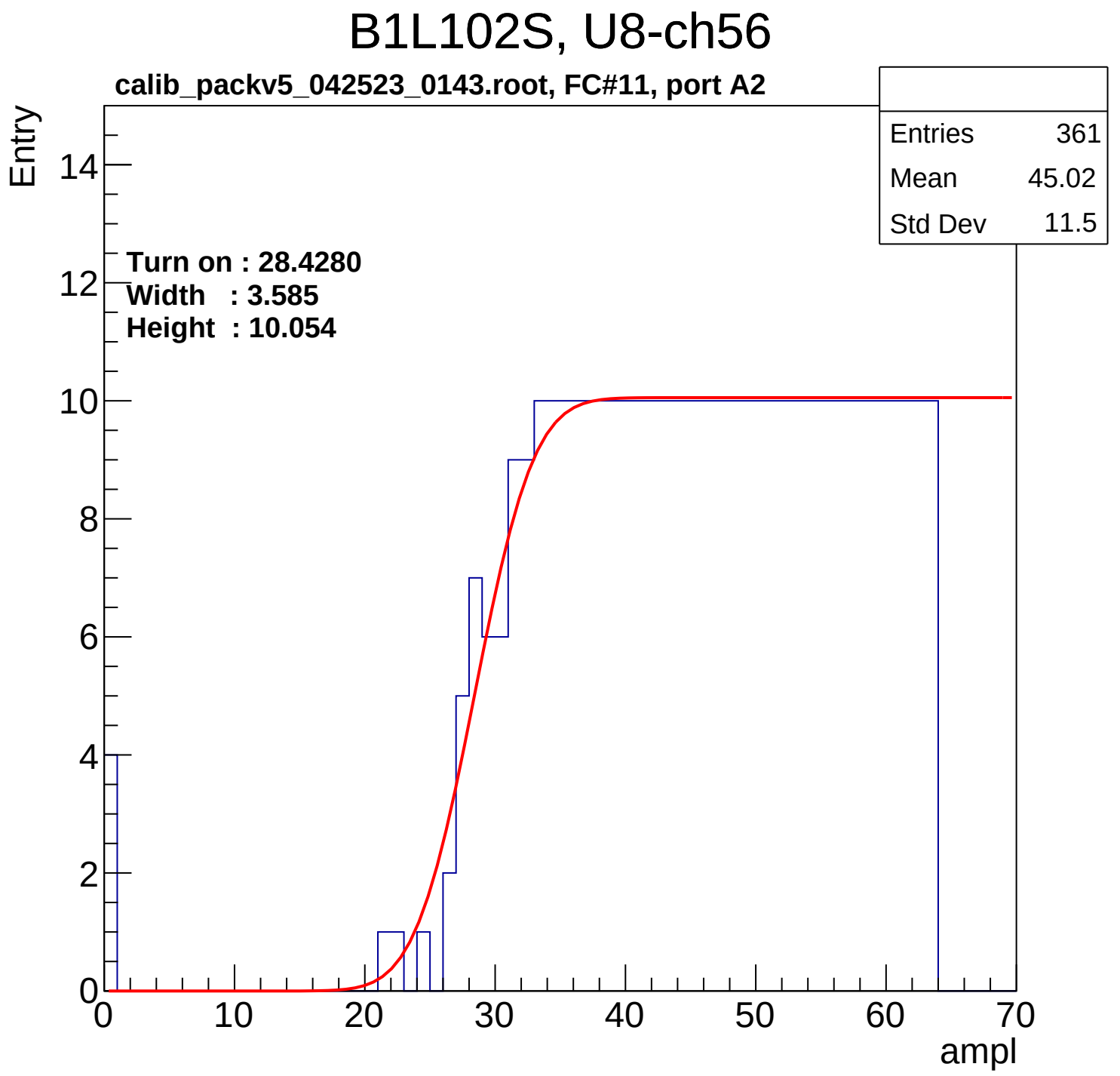
B1L102S, U8-ch56
calib_packv5_042523_0143.root, FC#11, port A2
Entries 361
Mean 45.02
Std Dev 11.5
Turn on : 28.4280
Width : 3.585
Height : 10.054
Entry
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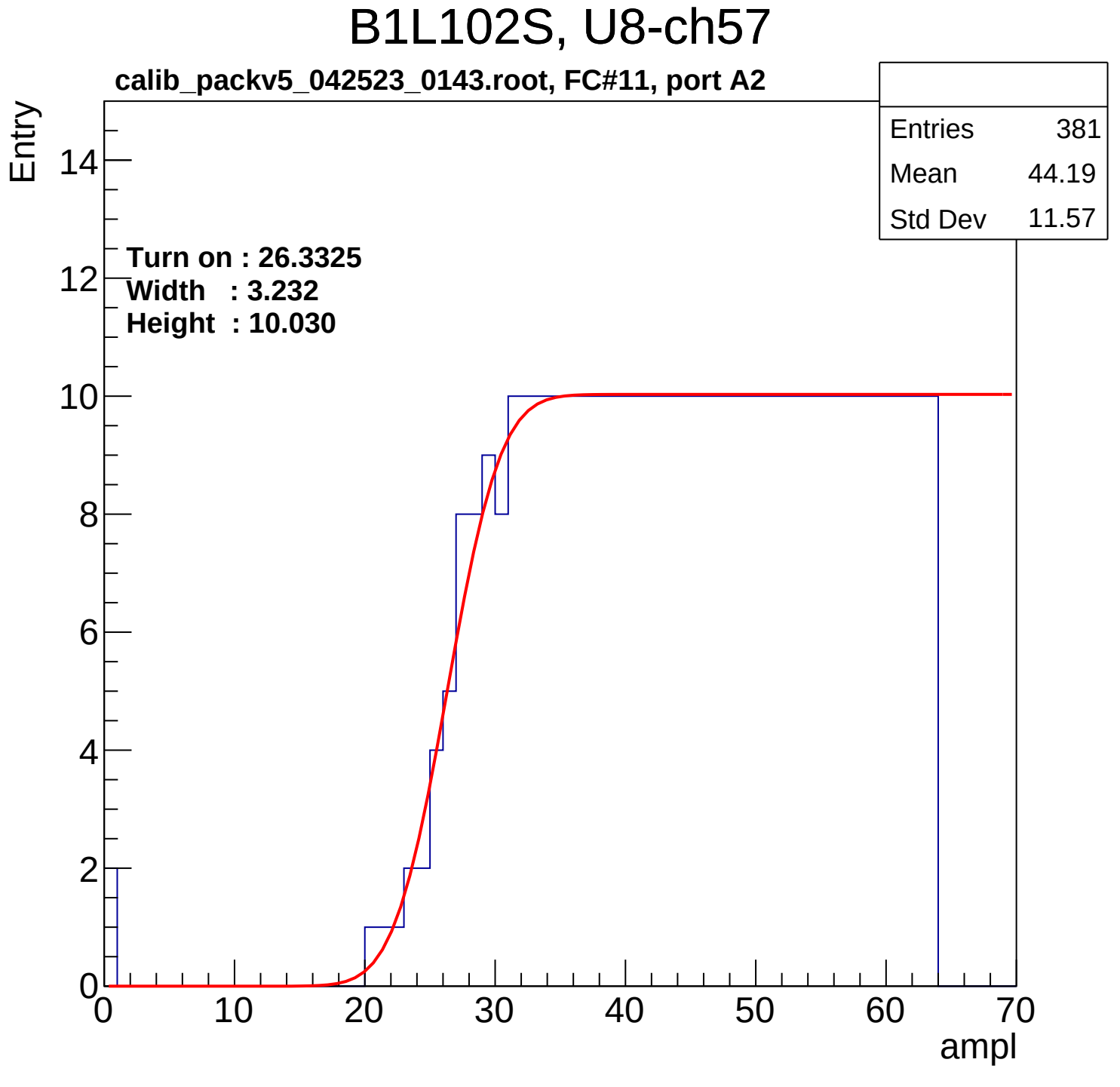
B1L102S, U8-ch57
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.19
Std Dev 11.57
Turn on : 26.3325
Width : 3.232
Height : 10.030
Entry
ampl
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4
6
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12
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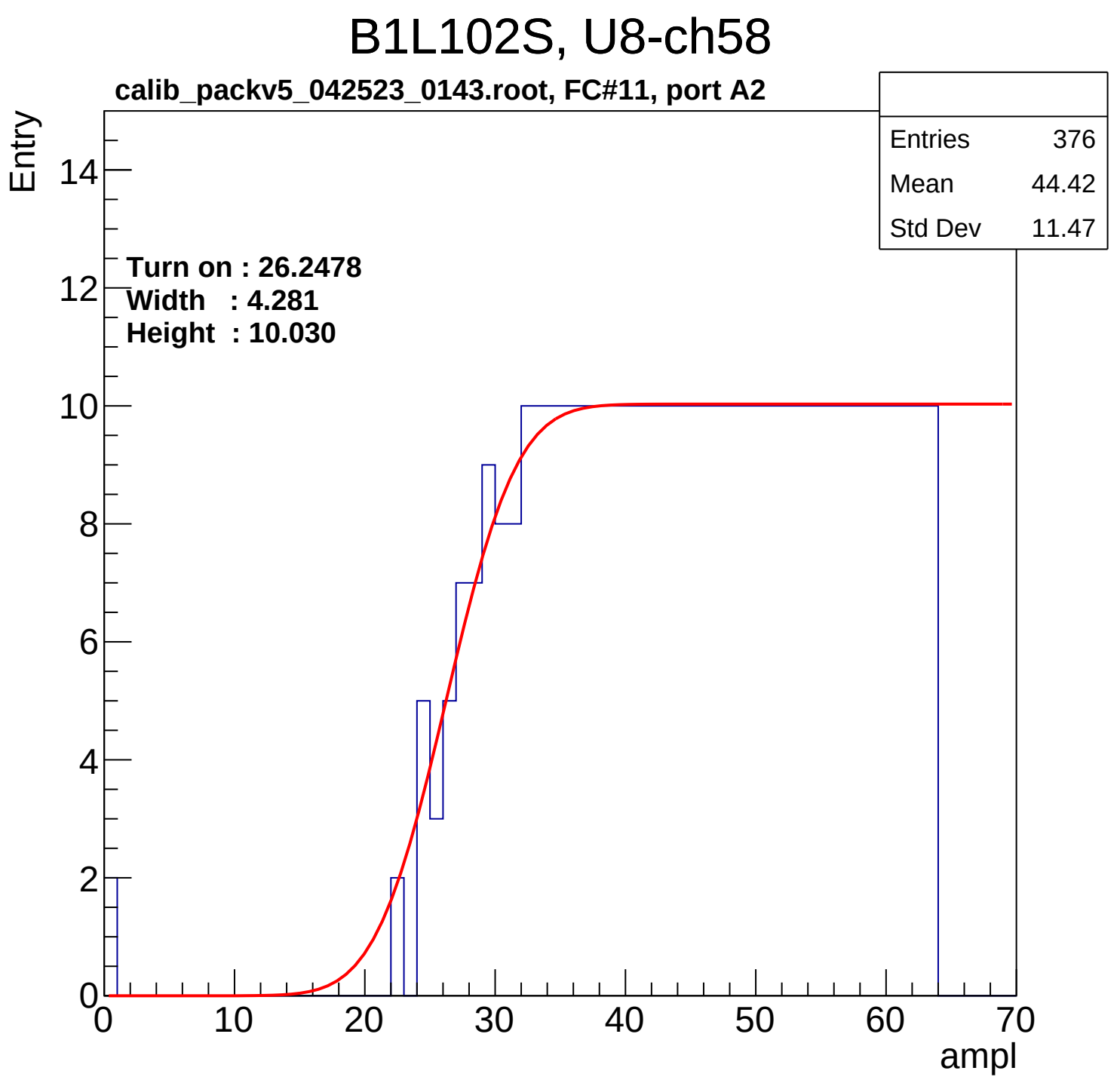
B1L102S, U8-ch58
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.42
Std Dev 11.47
Turn on : 26.2478
Width : 4.281
Height : 10.030
Entry
ampl
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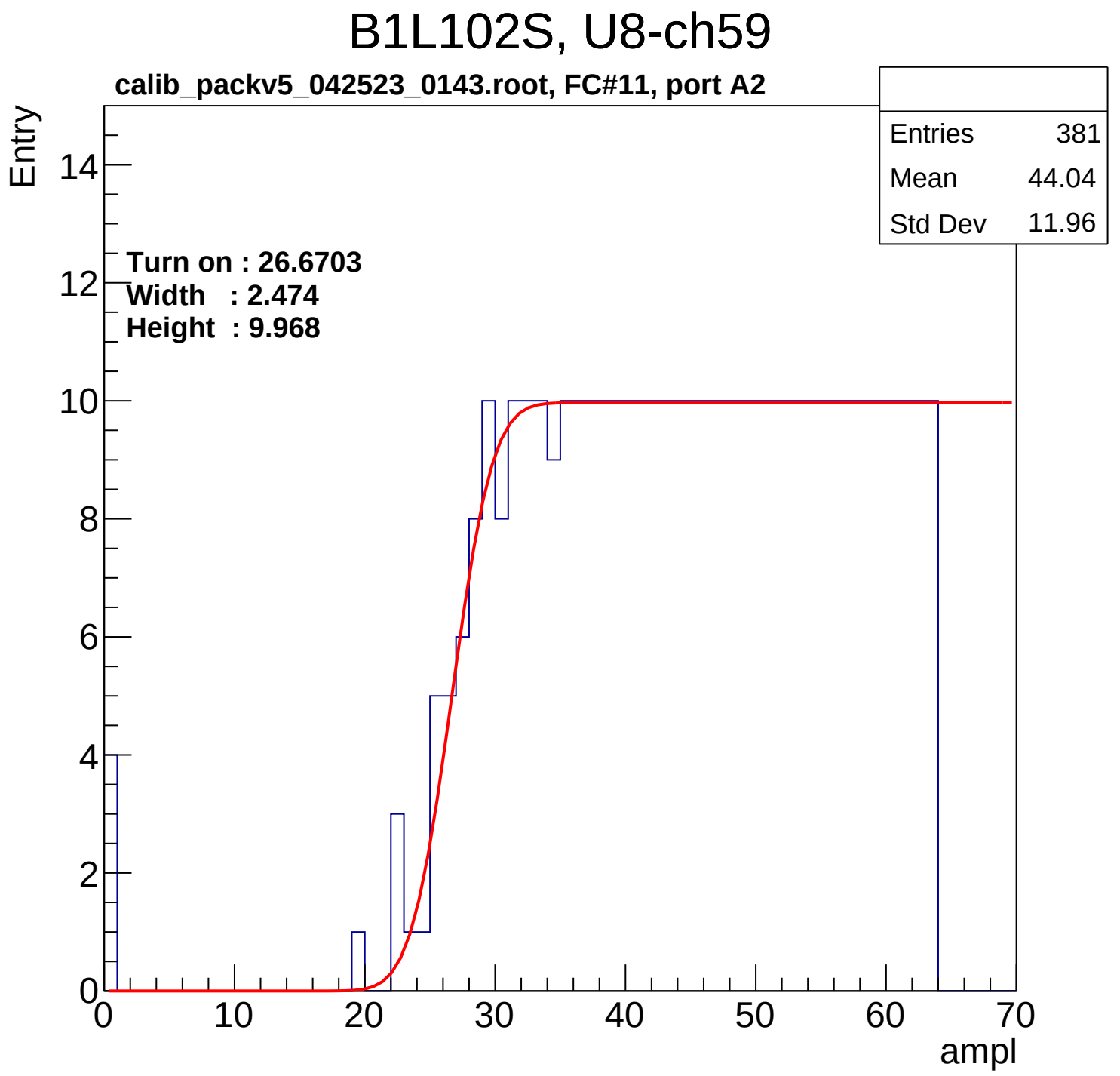
B1L102S, U8-ch59
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.04
Std Dev 11.96
Turn on : 26.6703
Width : 2.474
Height : 9.968
Entry
ampl
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2
4
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8
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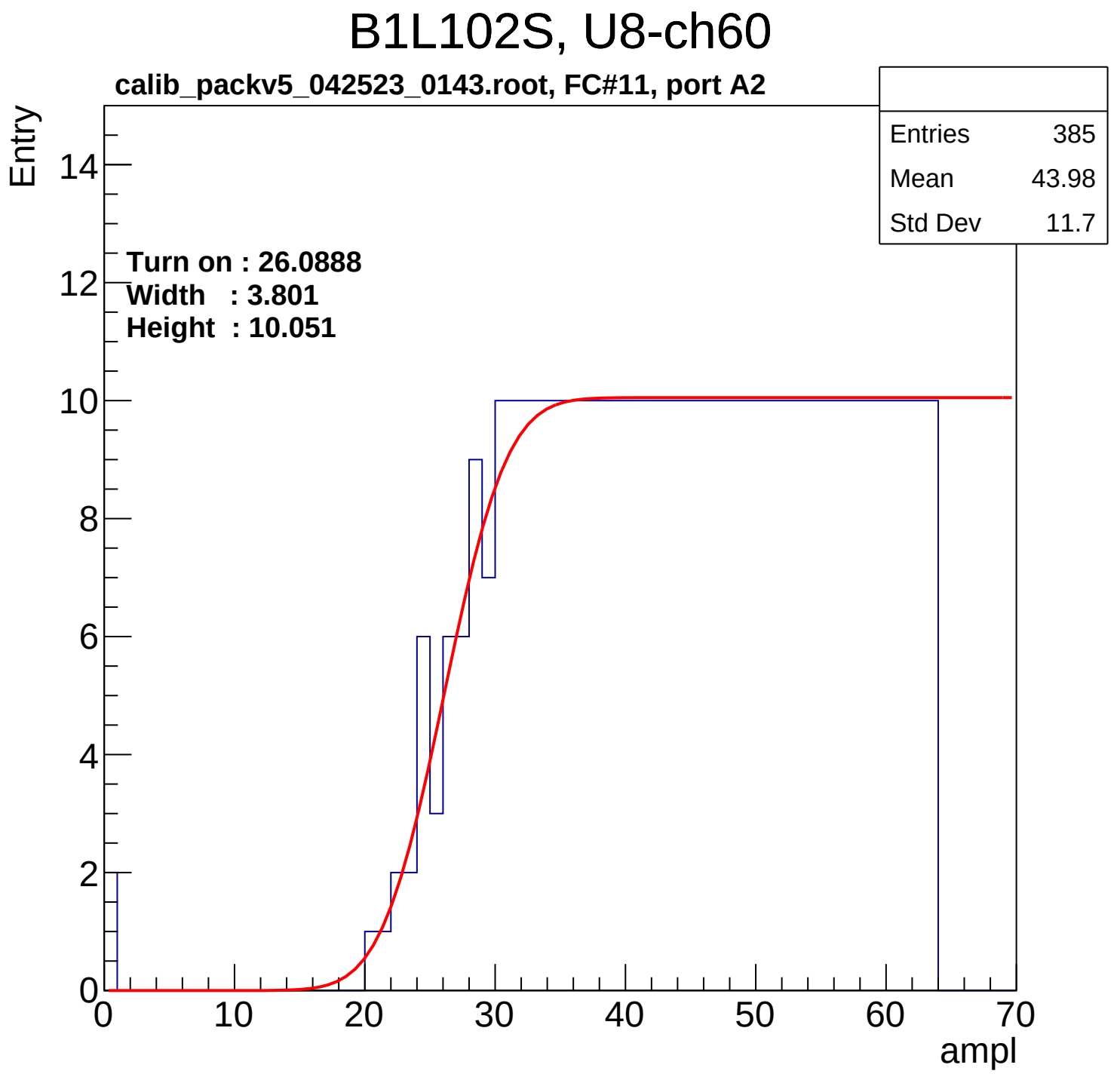
B1L102S, U8-ch60
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.98
Std Dev 11.7
Turn on : 26.0888
Width : 3.801
Height : 10.051
Entry
ampl
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2
4
6
8
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60
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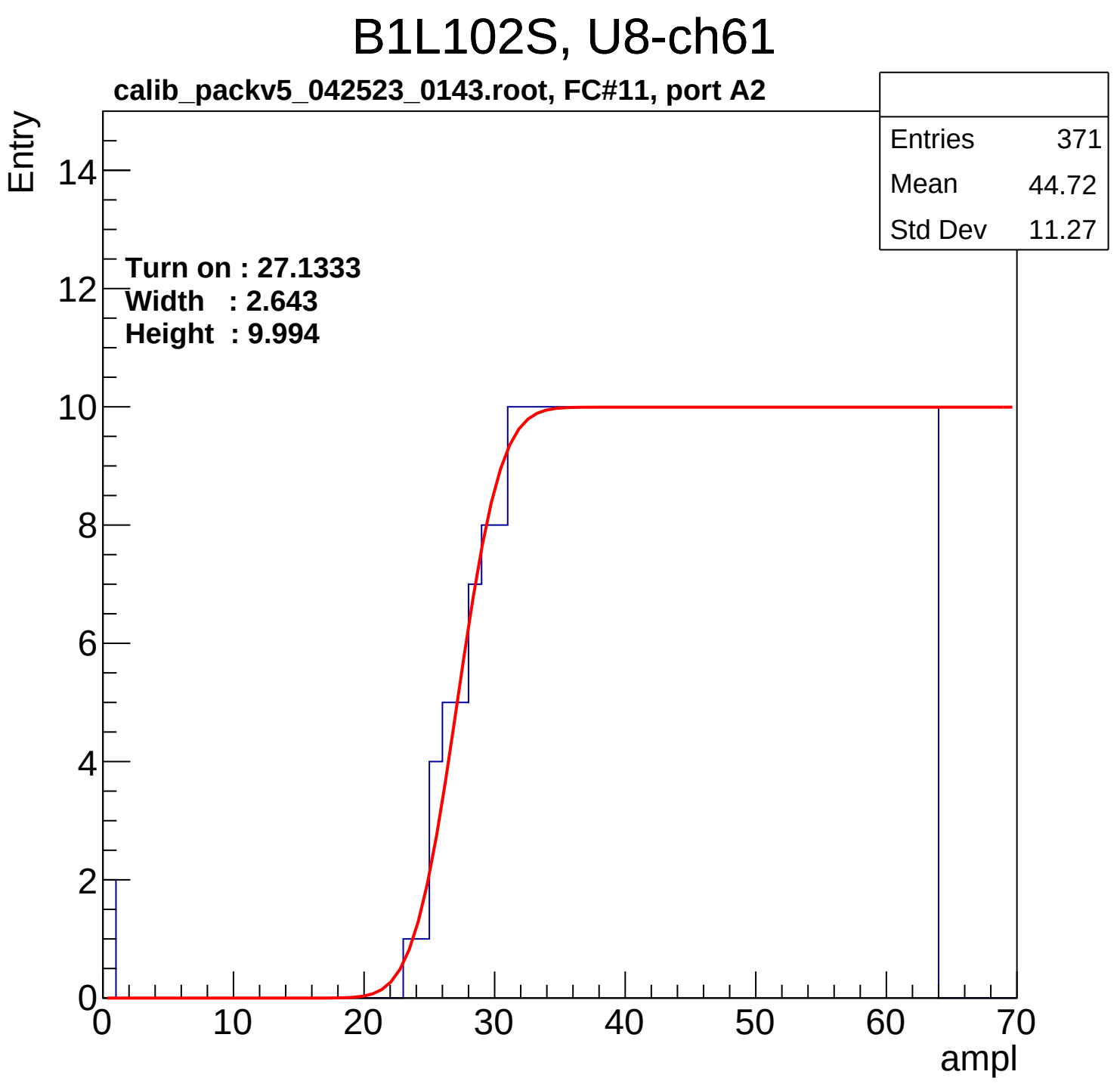
B1L102S, U8-ch61
calib_packv5_042523_0143.root, FC#11, port A2
Entries 371
Mean 44.72
Std Dev 11.27
Turn on : 27.1333
Width : 2.643
Height : 9.994
Entry
ampl
0
2
4
6
8
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12
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0
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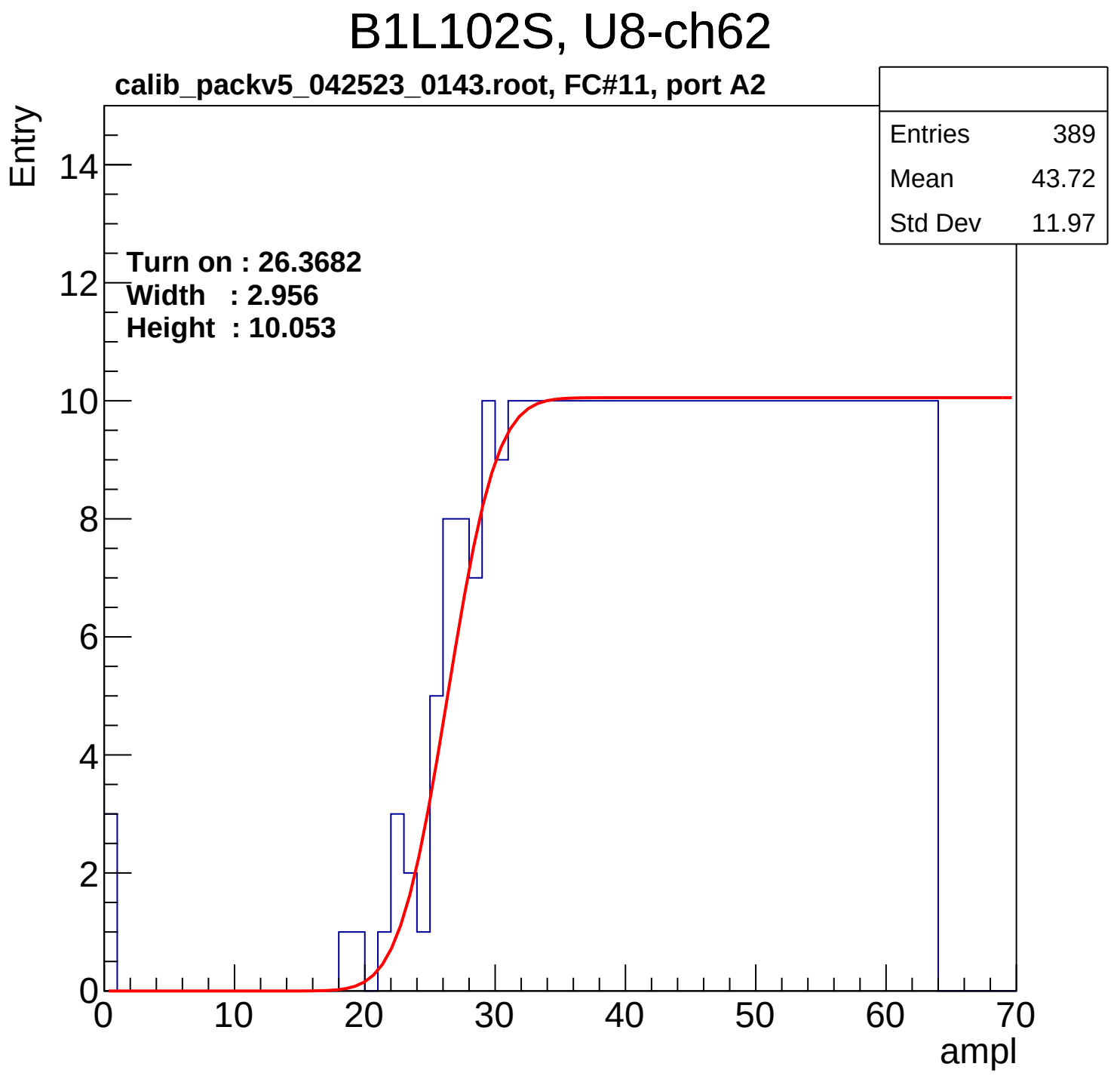
B1L102S, U8-ch62
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.72
Std Dev 11.97
Turn on : 26.3682
Width : 2.956
Height : 10.053
Entry
ampl
0
2
4
6
8
10
12
14
0
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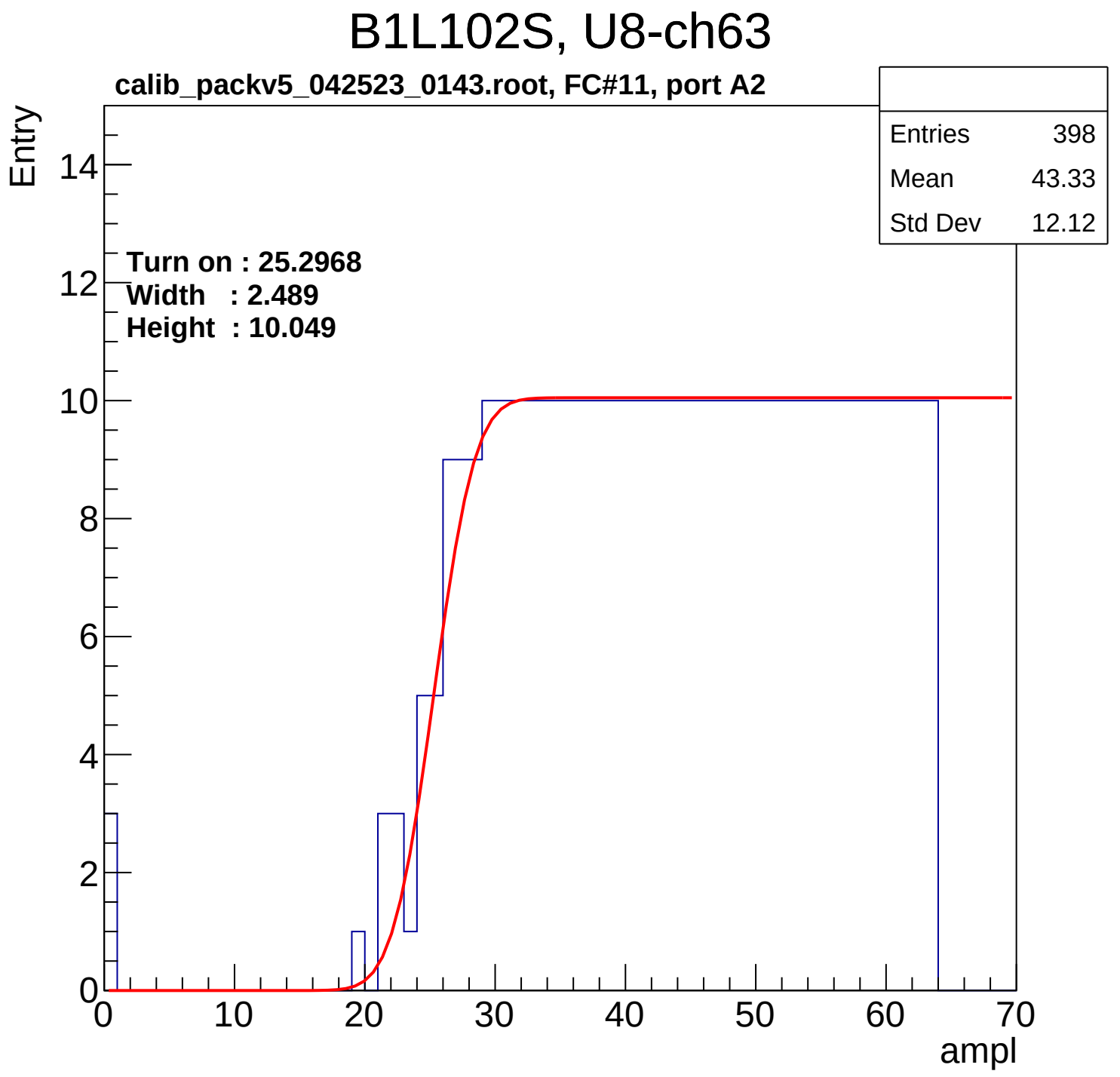
B1L102S, U8-ch63
calib_packv5_042523_0143.root, FC#11, port A2
Entries 398
Mean 43.33
Std Dev 12.12
Turn on : 25.2968
Width : 2.489
Height : 10.049
Entry
ampl
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2
4
6
8
10
12
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0
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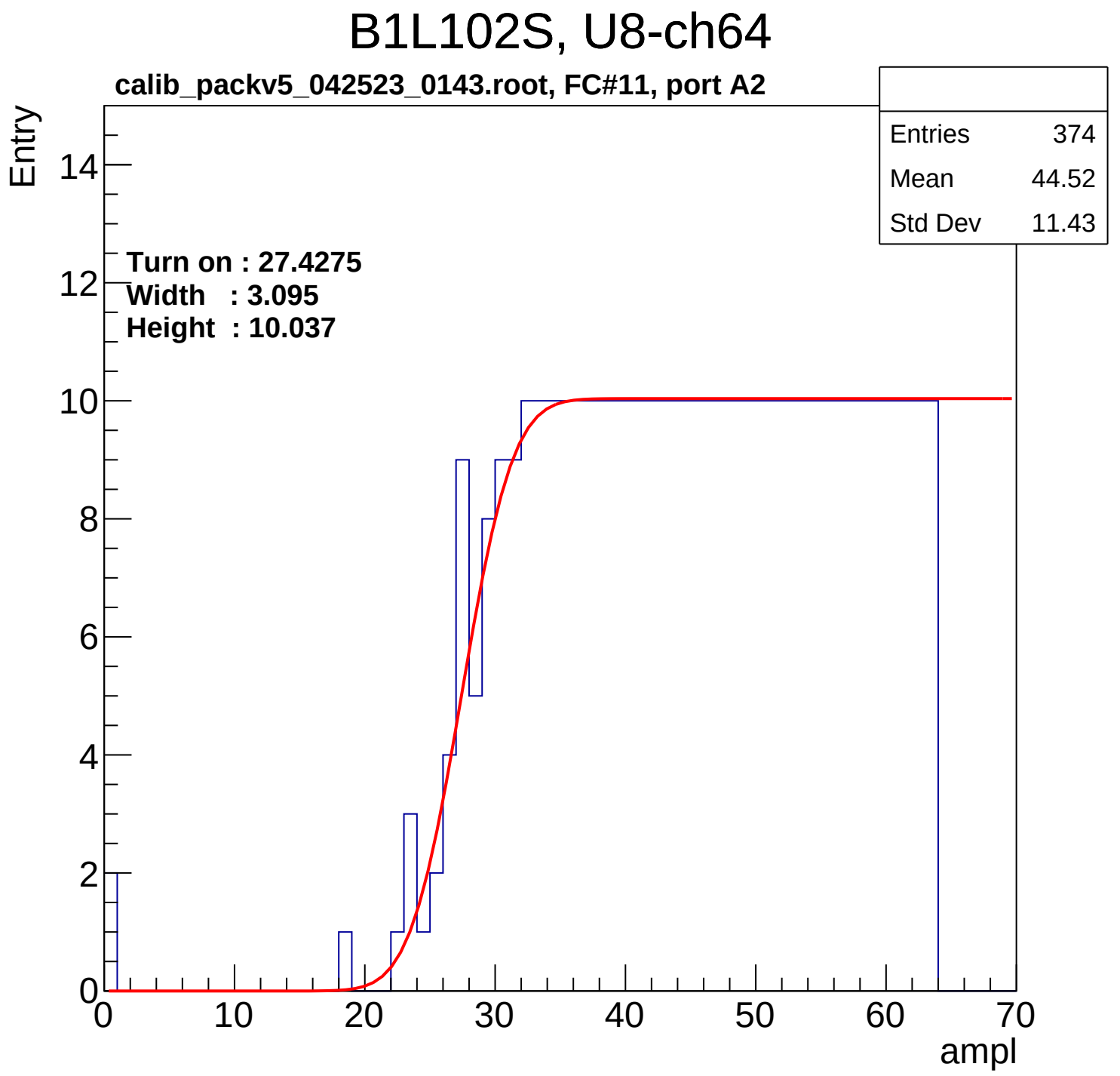
B1L102S, U8-ch64
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.52
Std Dev 11.43
Turn on : 27.4275
Width : 3.095
Height : 10.037
Entry
ampl
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4
6
8
10
12
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0
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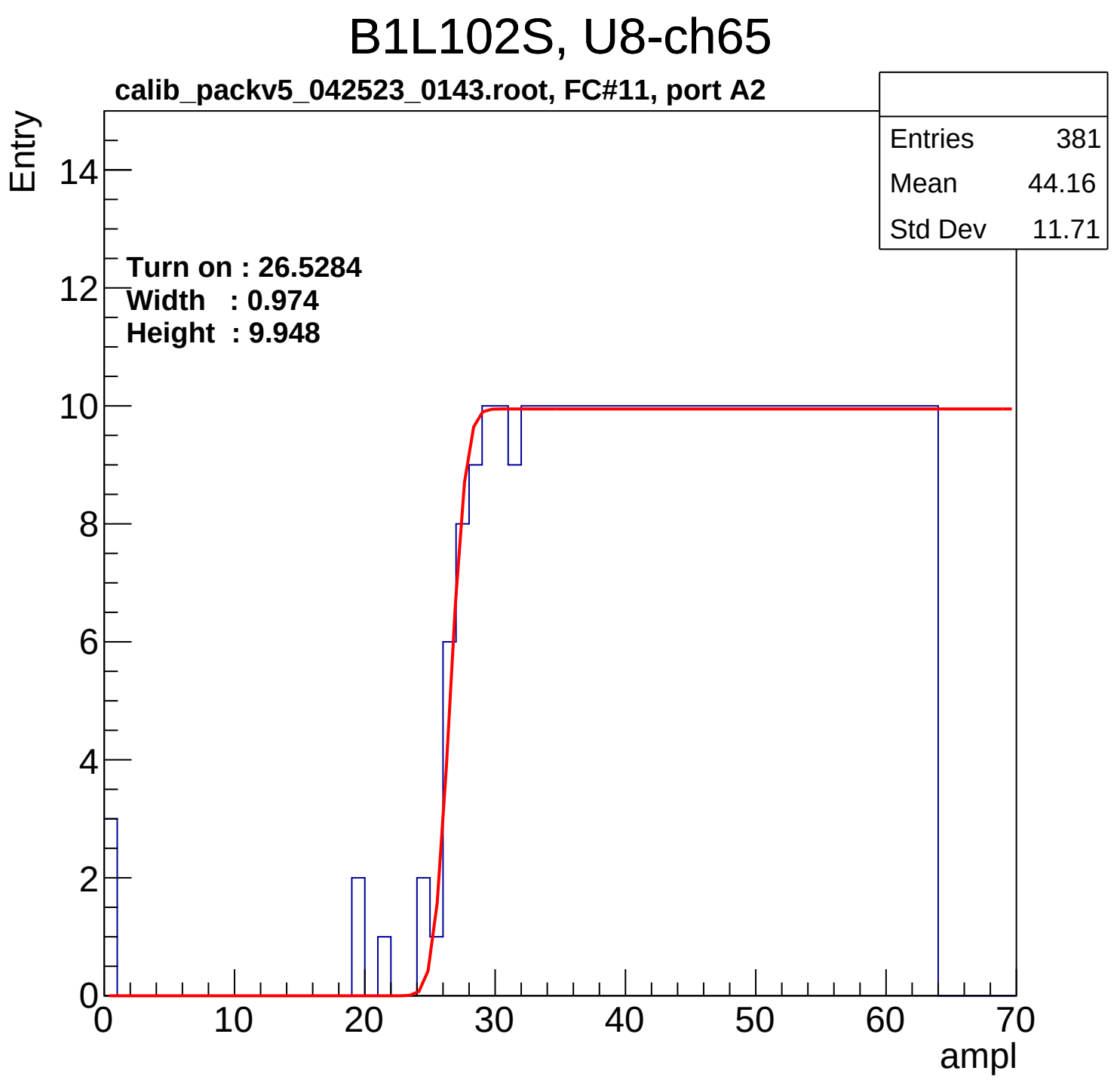
B1L102S, U8-ch65
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.16
Std Dev 11.71
Turn on : 26.5284
Width : 0.974
Height : 9.948
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
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60
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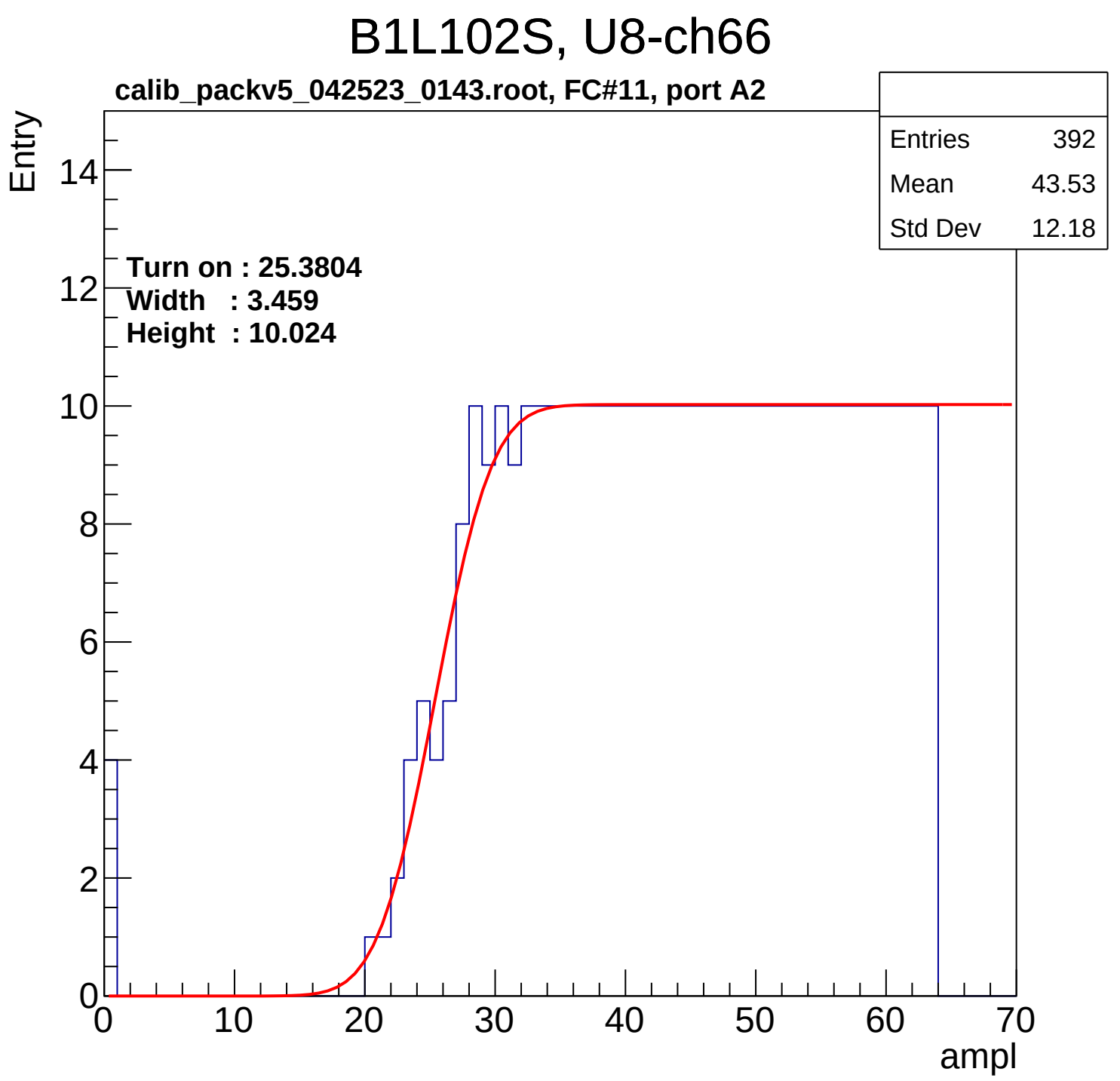
B1L102S, U8-ch66
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.53
Std Dev 12.18
Turn on : 25.3804
Width : 3.459
Height : 10.024
Entry
ampl
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6
8
10
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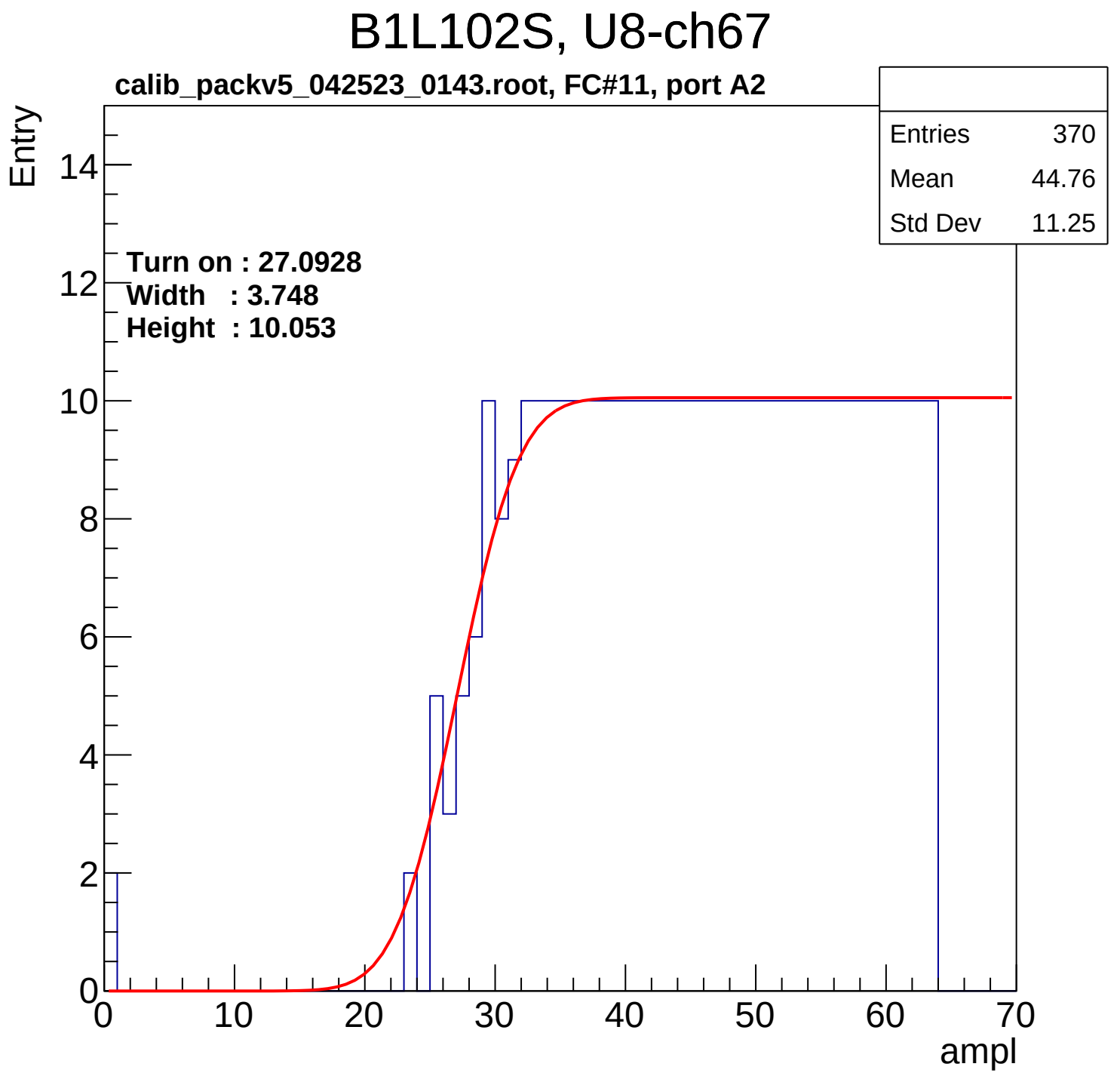
B1L102S, U8-ch67
calib_packv5_042523_0143.root, FC#11, port A2
Entries 370
Mean 44.76
Std Dev 11.25
Turn on : 27.0928
Width : 3.748
Height : 10.053
Entry
ampl
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2
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6
8
10
12
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0
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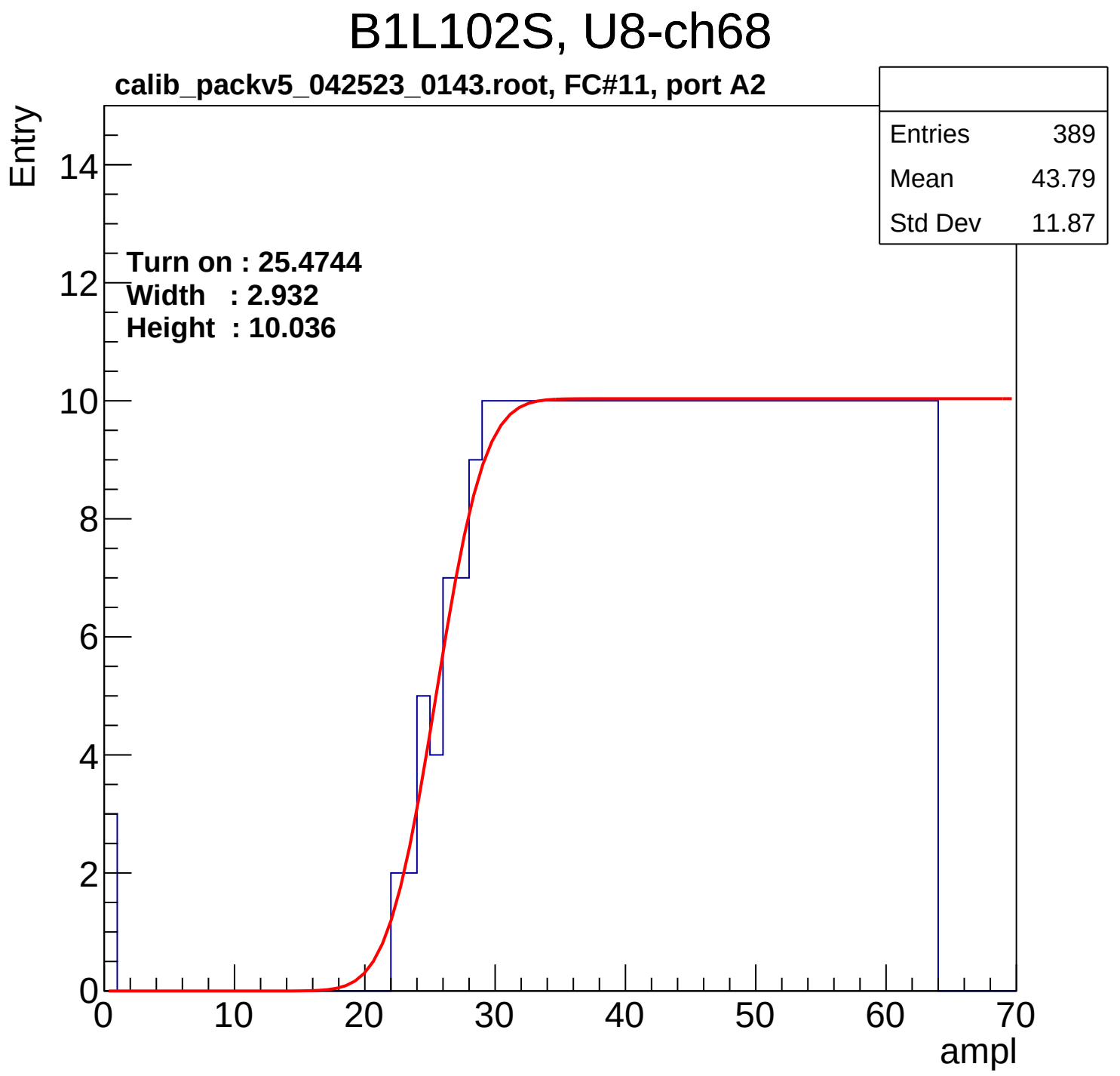
B1L102S, U8-ch68
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.79
Std Dev 11.87
Turn on : 25.4744
Width : 2.932
Height : 10.036
Entry
ampl
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6
8
10
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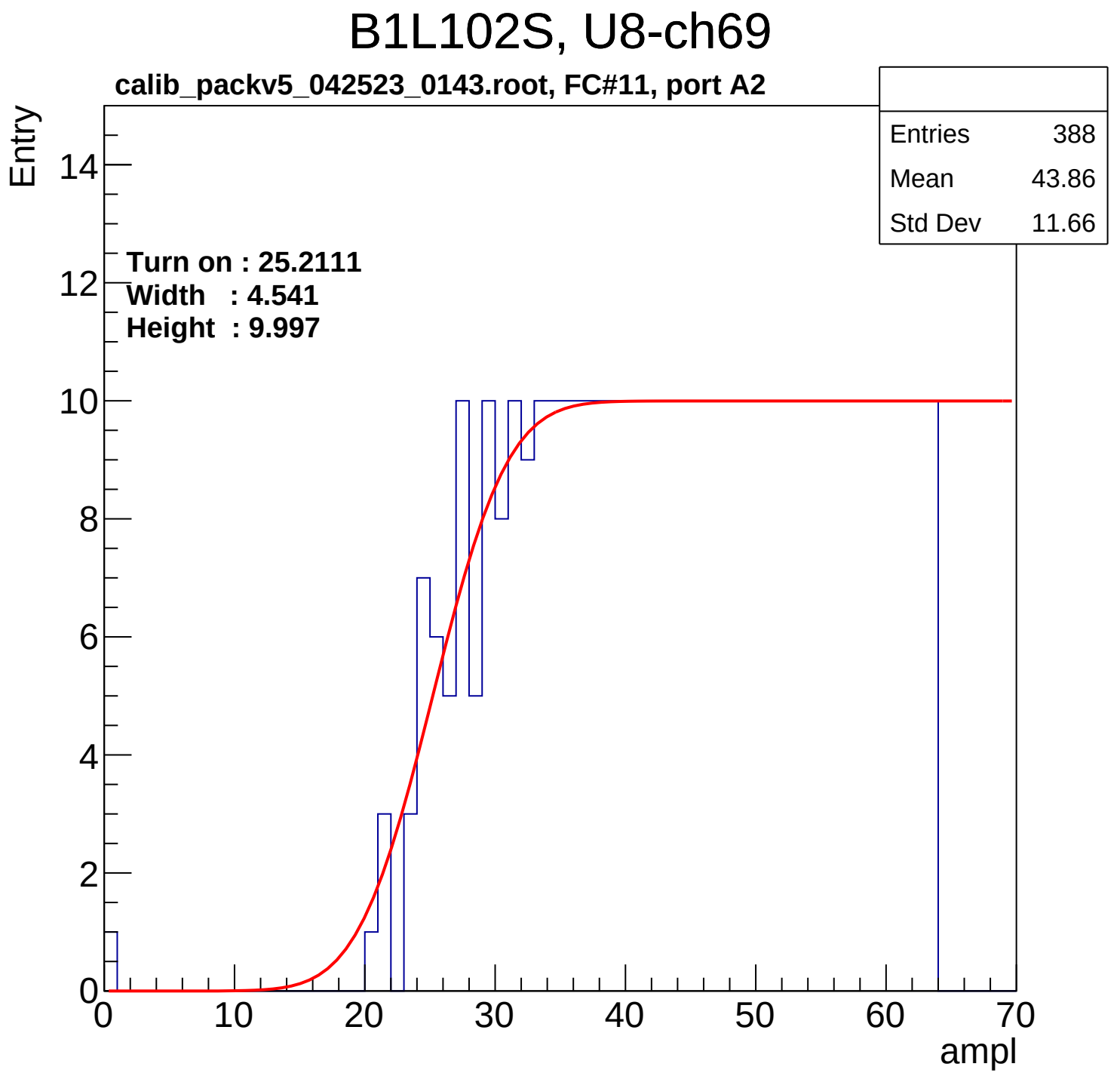
B1L102S, U8-ch69
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.86
Std Dev 11.66
Turn on : 25.2111
Width : 4.541
Height : 9.997
Entry
ampl
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4
6
8
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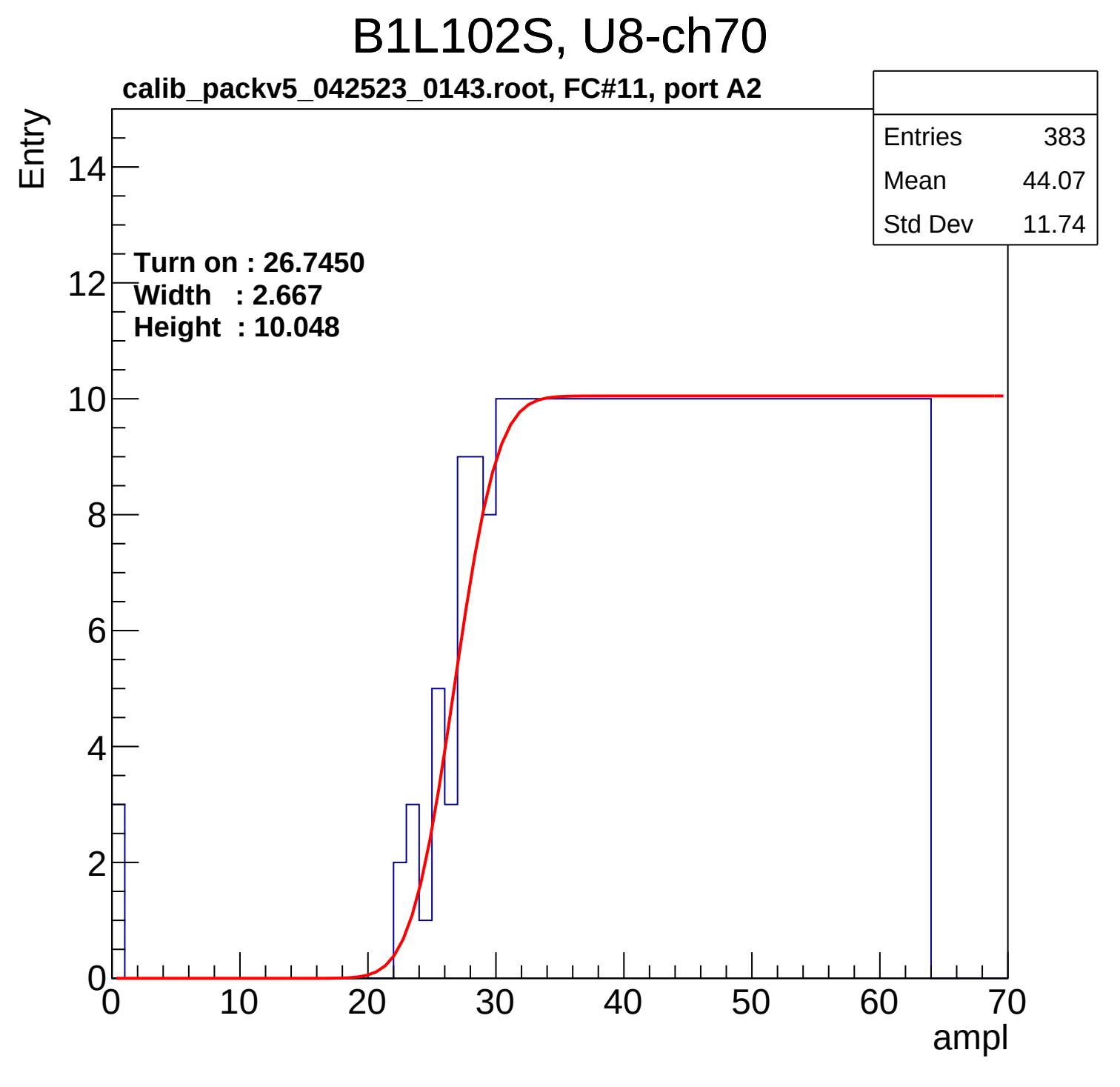
B1L102S, U8-ch70
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.07
Std Dev 11.74
Turn on : 26.7450
Width : 2.667
Height : 10.048
Entry
ampl
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8
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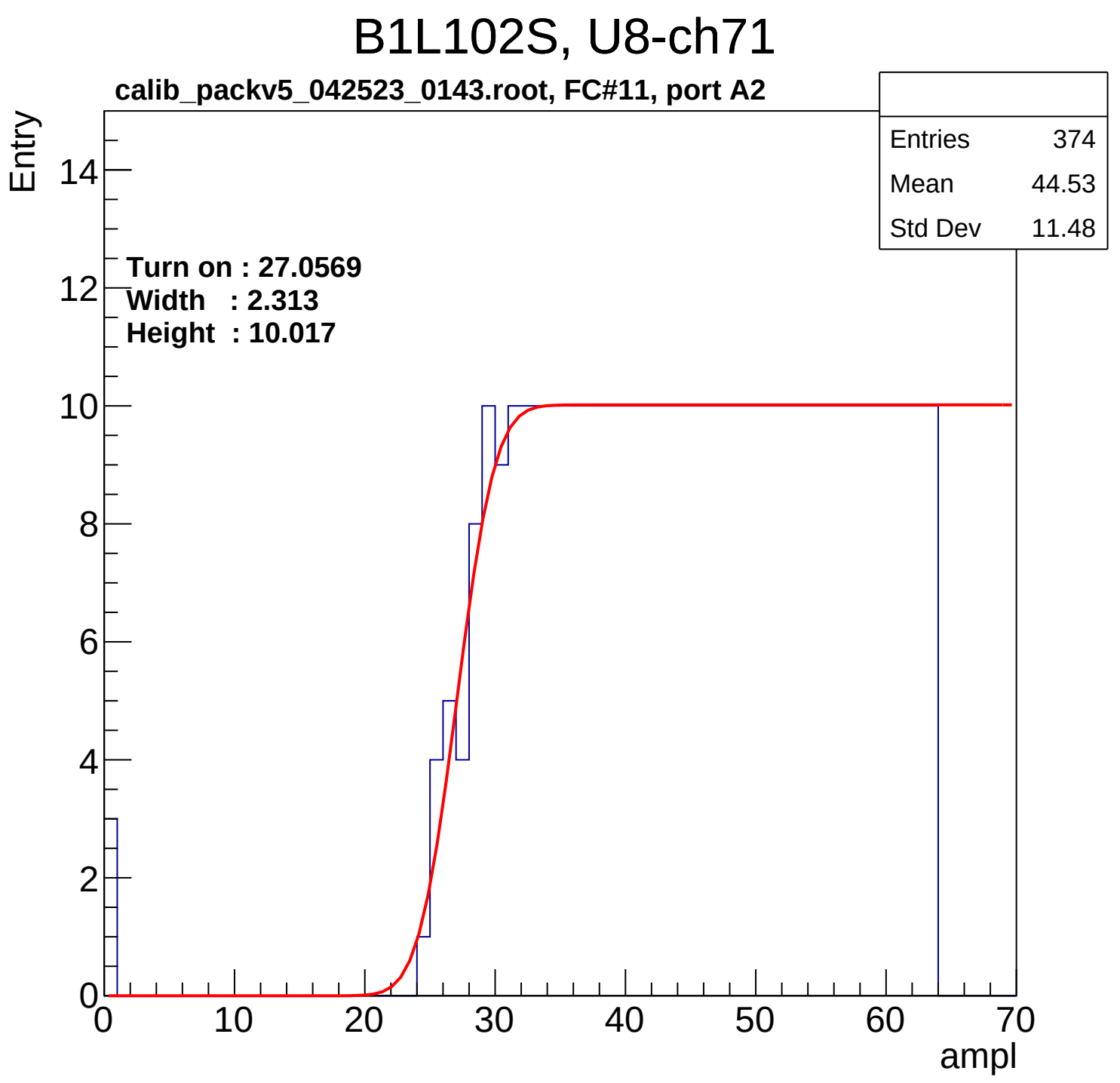
B1L102S, U8-ch71
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.53
Std Dev 11.48
Turn on : 27.0569
Width : 2.313
Height : 10.017
Entry
ampl
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8
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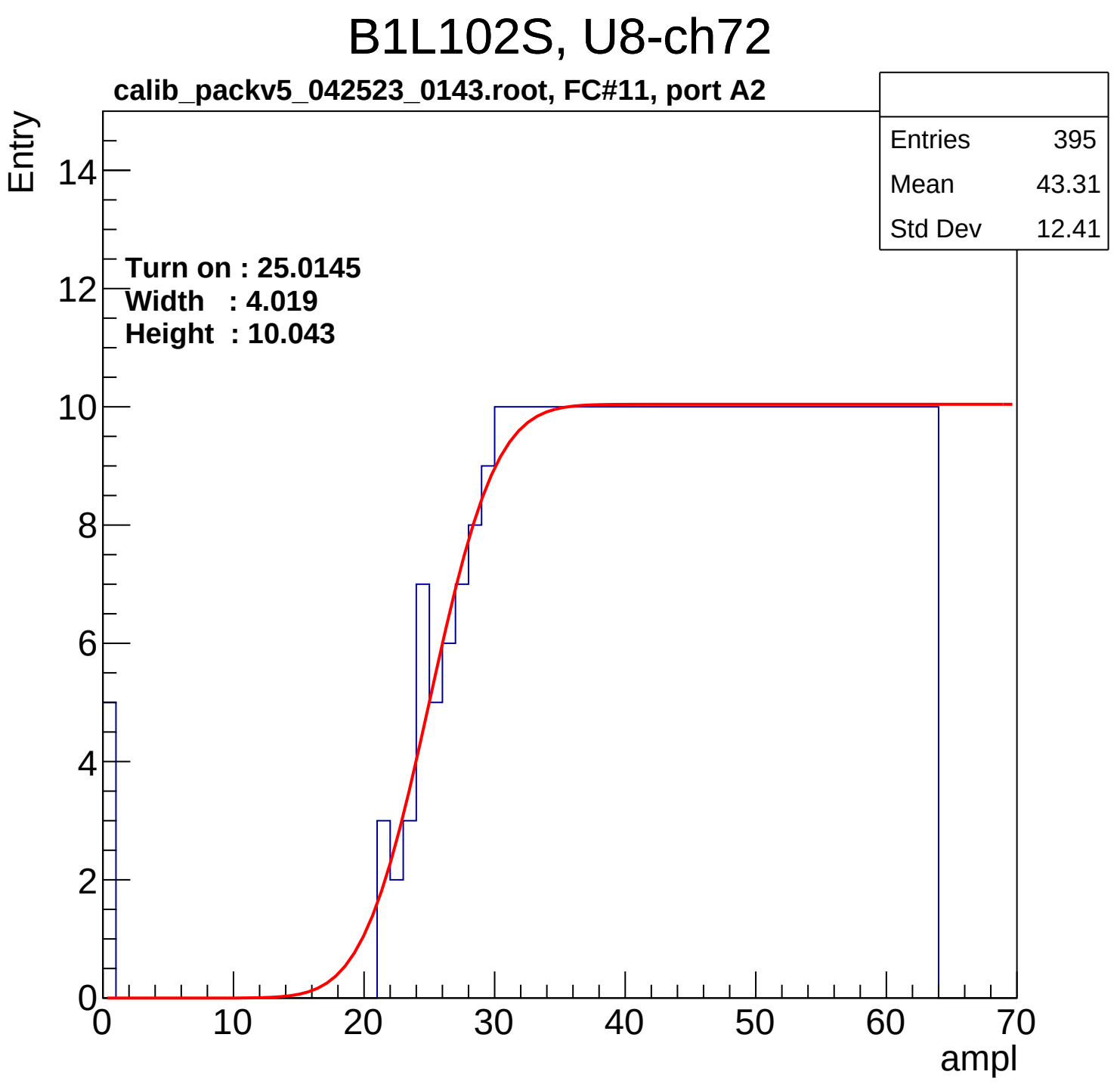
B1L102S, U8-ch72
calib_packv5_042523_0143.root, FC#11, port A2
Entries 395
Mean 43.31
Std Dev 12.41
Turn on : 25.0145
Width : 4.019
Height : 10.043
Entry
ampl
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6
8
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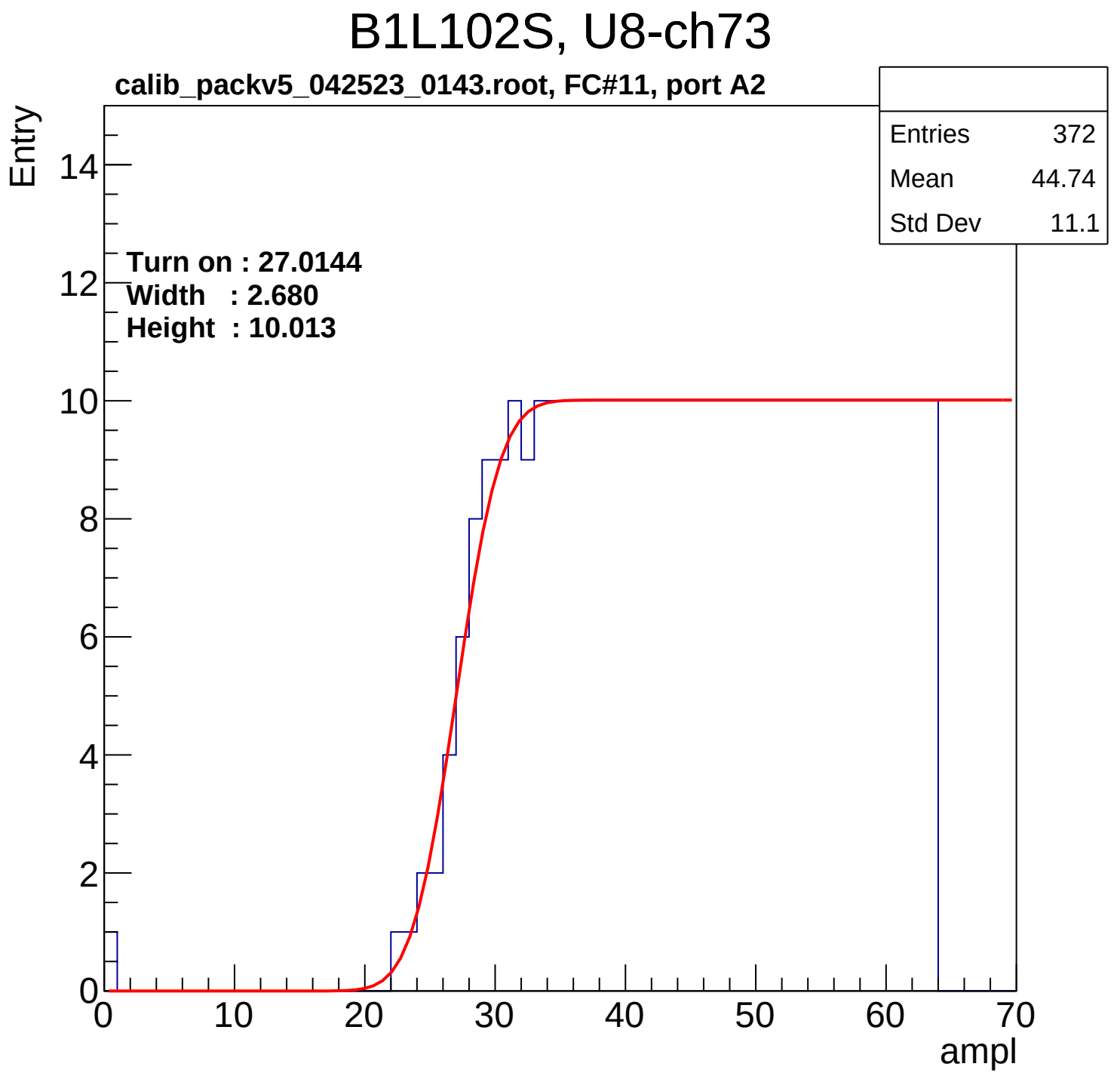
B1L102S, U8-ch73
calib_packv5_042523_0143.root, FC#11, port A2
Entries 372
Mean 44.74
Std Dev 11.1
Turn on : 27.0144
Width : 2.680
Height : 10.013
Entry
ampl
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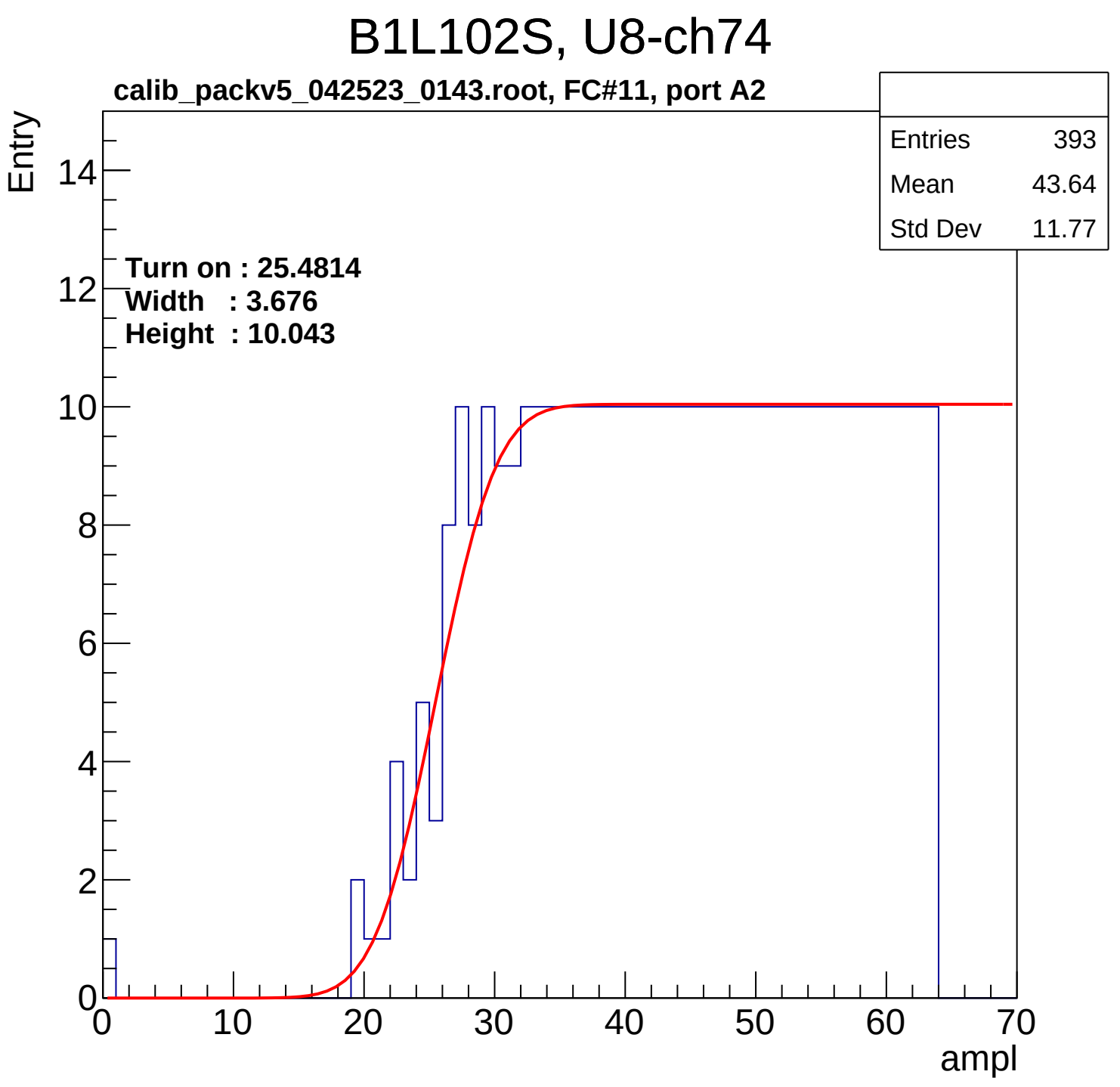
B1L102S, U8-ch74
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.64
Std Dev 11.77
Turn on : 25.4814
Width : 3.676
Height : 10.043
Entry
ampl
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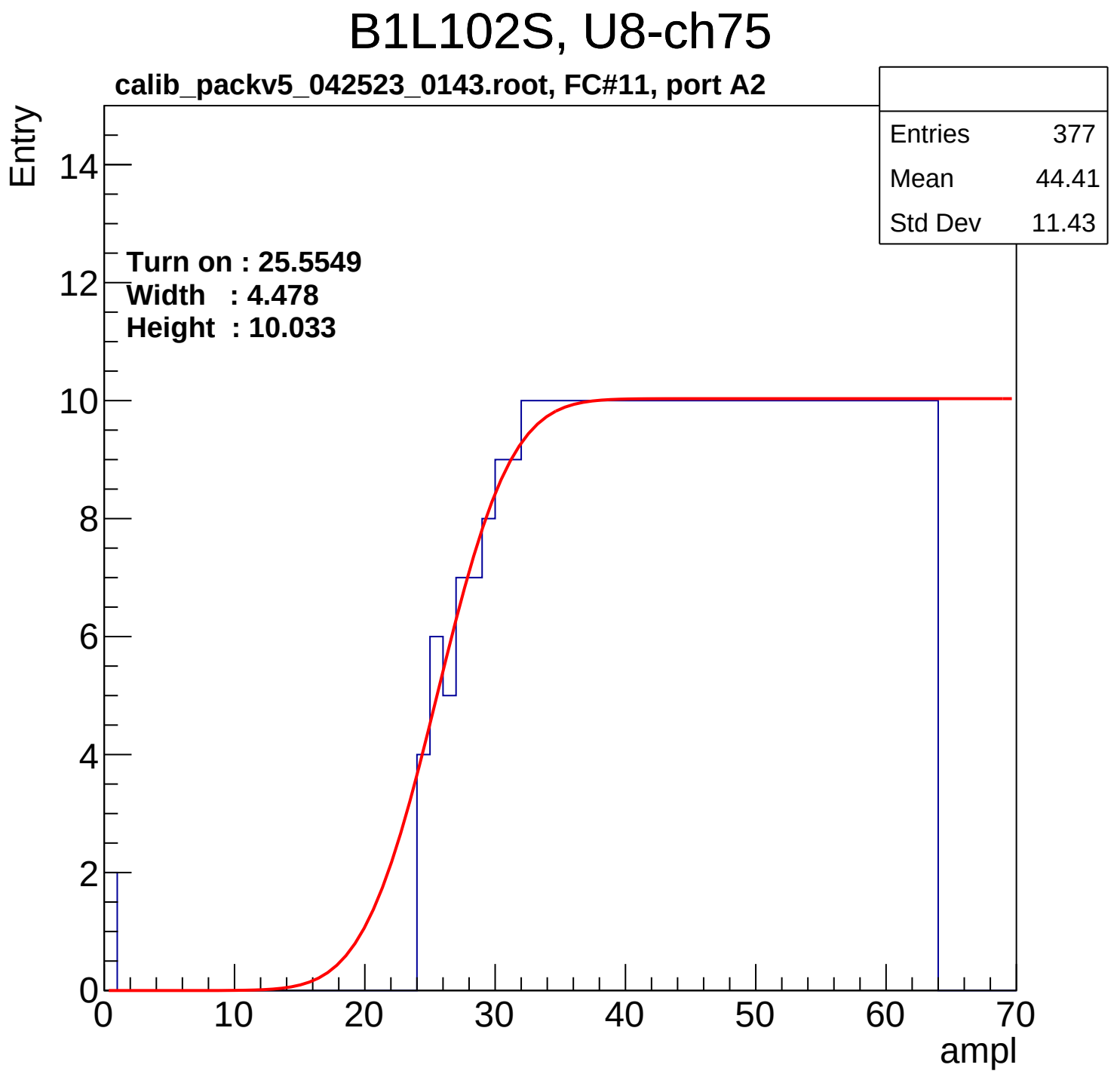
B1L102S, U8-ch75
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.41
Std Dev 11.43
Turn on : 25.5549
Width : 4.478
Height : 10.033
Entry
ampl
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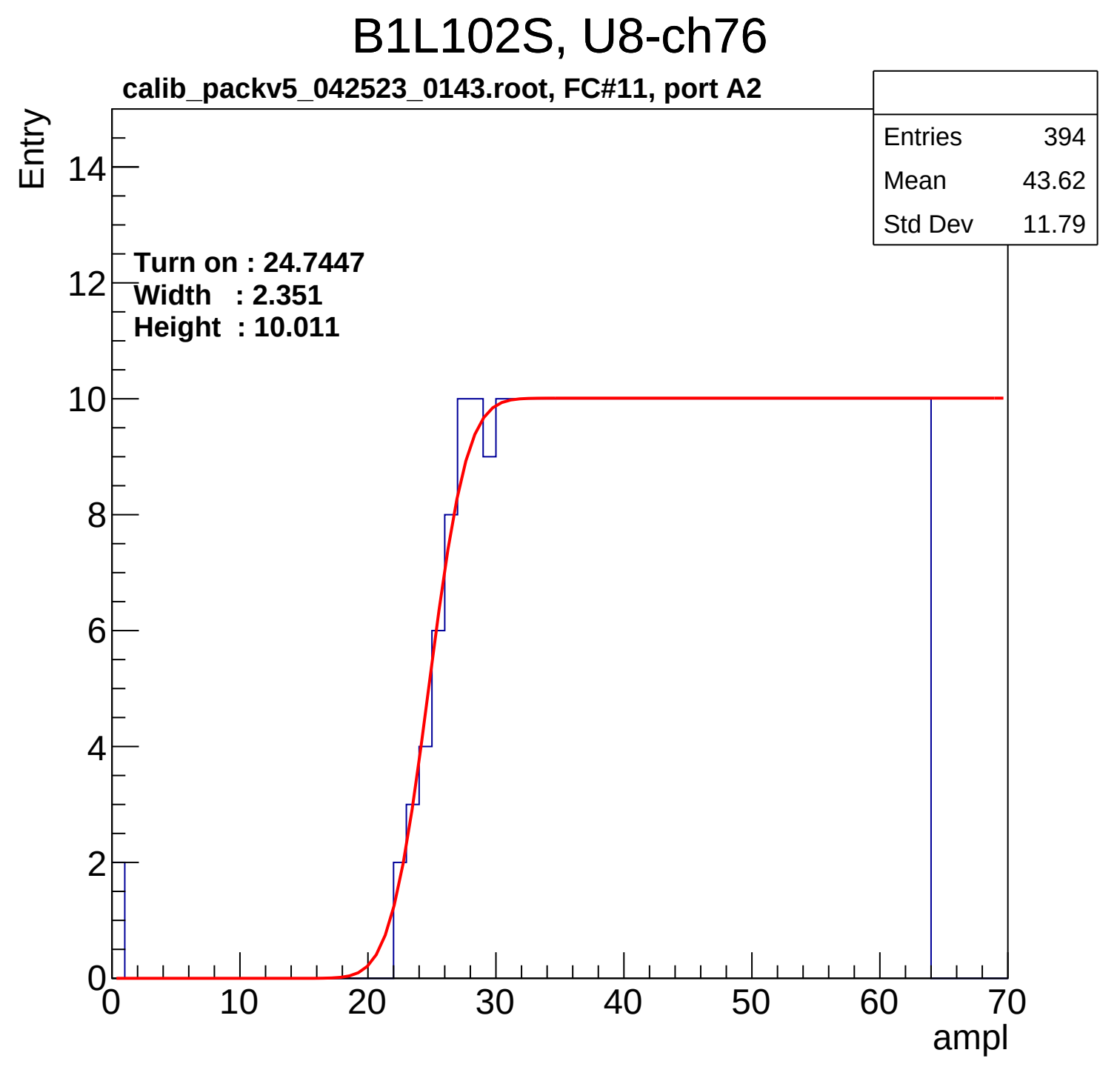
B1L102S, U8-ch76
calib_packv5_042523_0143.root, FC#11, port A2
Entries 394
Mean 43.62
Std Dev 11.79
Turn on : 24.7447
Width : 2.351
Height : 10.011
Entry
ampl
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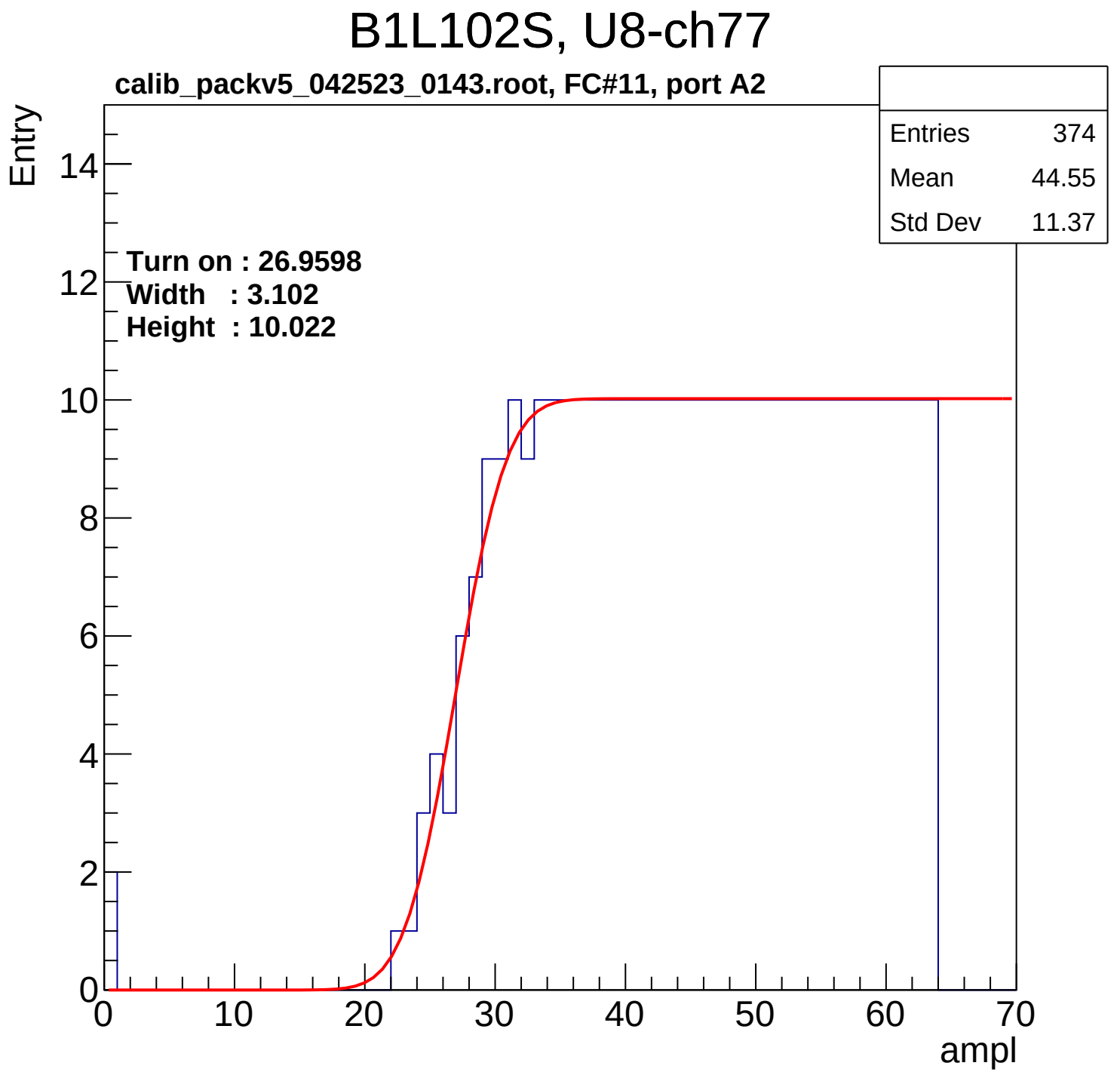
B1L102S, U8-ch77
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.55
Std Dev 11.37
Turn on : 26.9598
Width : 3.102
Height : 10.022
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ampl
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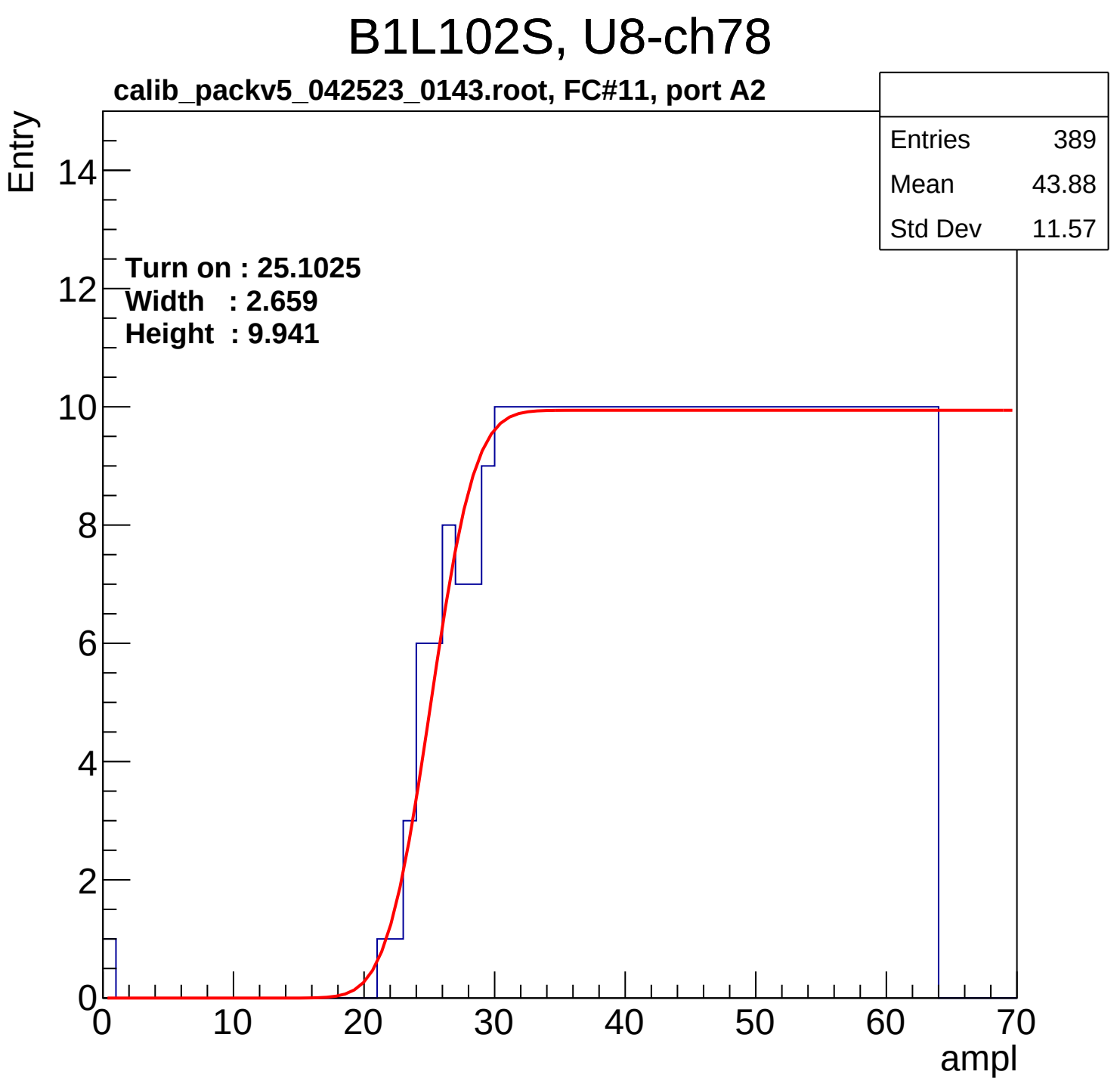
B1L102S, U8-ch78
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.88
Std Dev 11.57
Turn on : 25.1025
Width : 2.659
Height : 9.941
Entry
ampl
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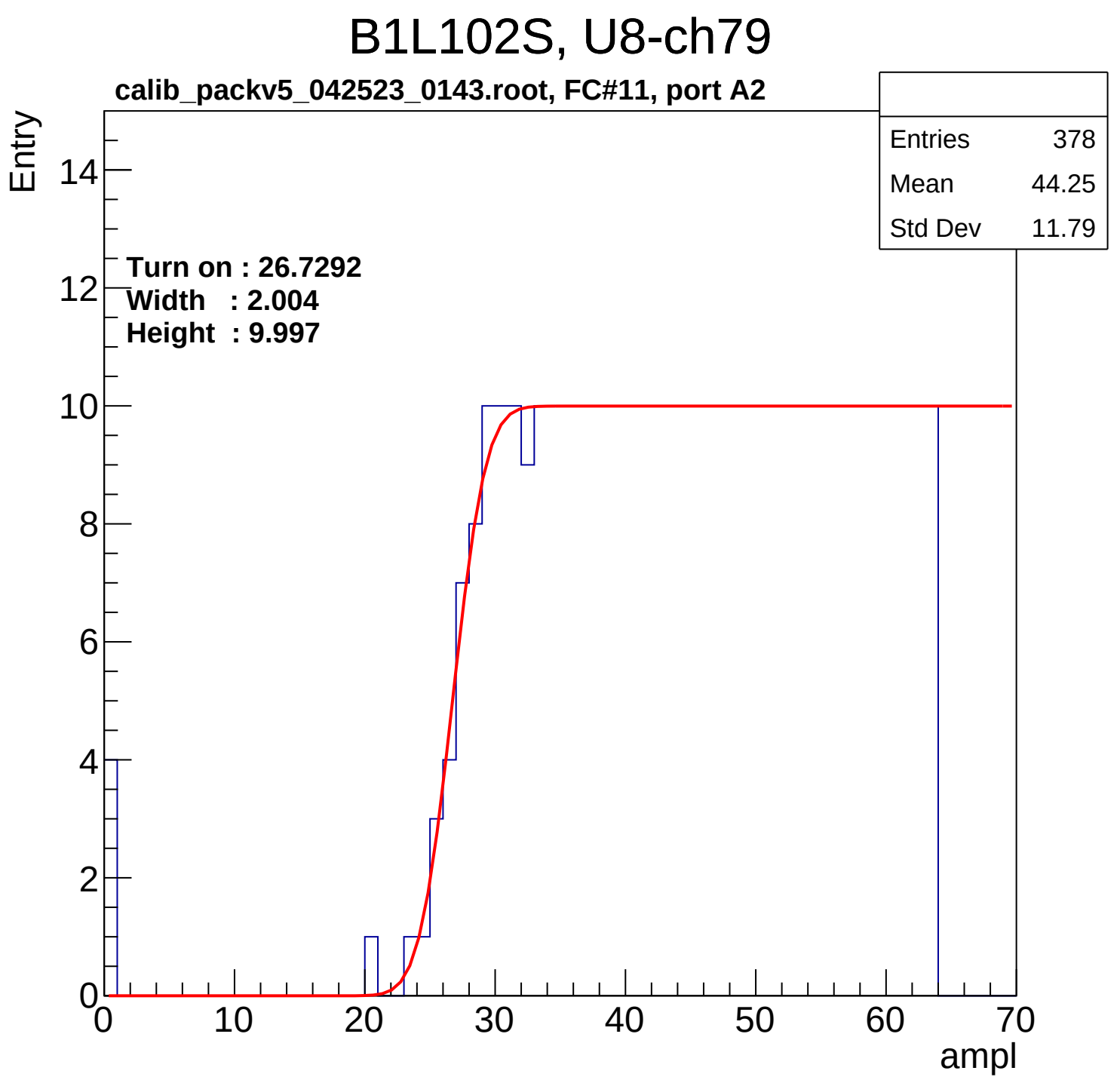
B1L102S, U8-ch79
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.25
Std Dev 11.79
Turn on : 26.7292
Width : 2.004
Height : 9.997
Entry
ampl
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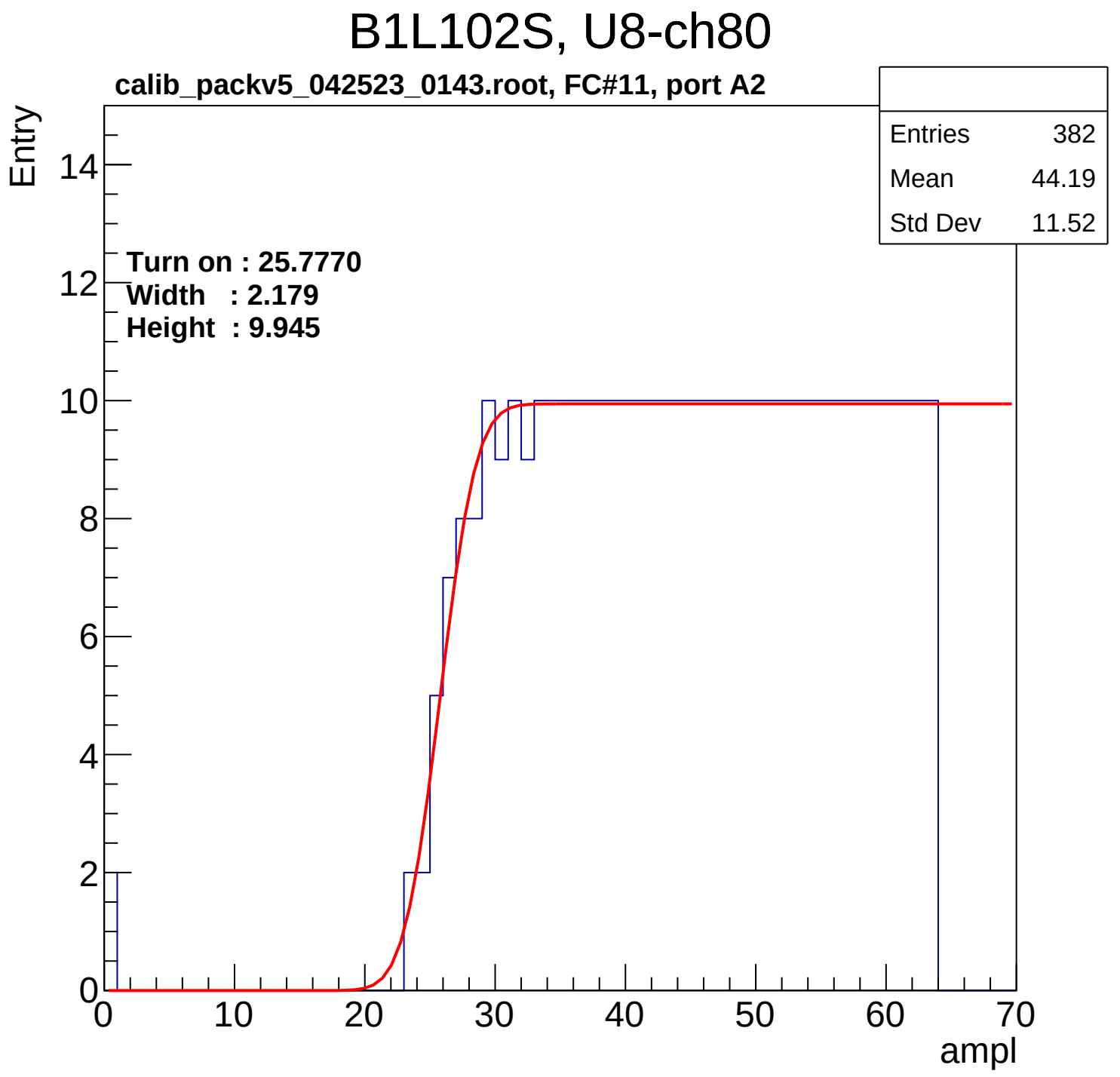
B1L102S, U8-ch80
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.19
Std Dev 11.52
Turn on : 25.7770
Width : 2.179
Height : 9.945
Entry
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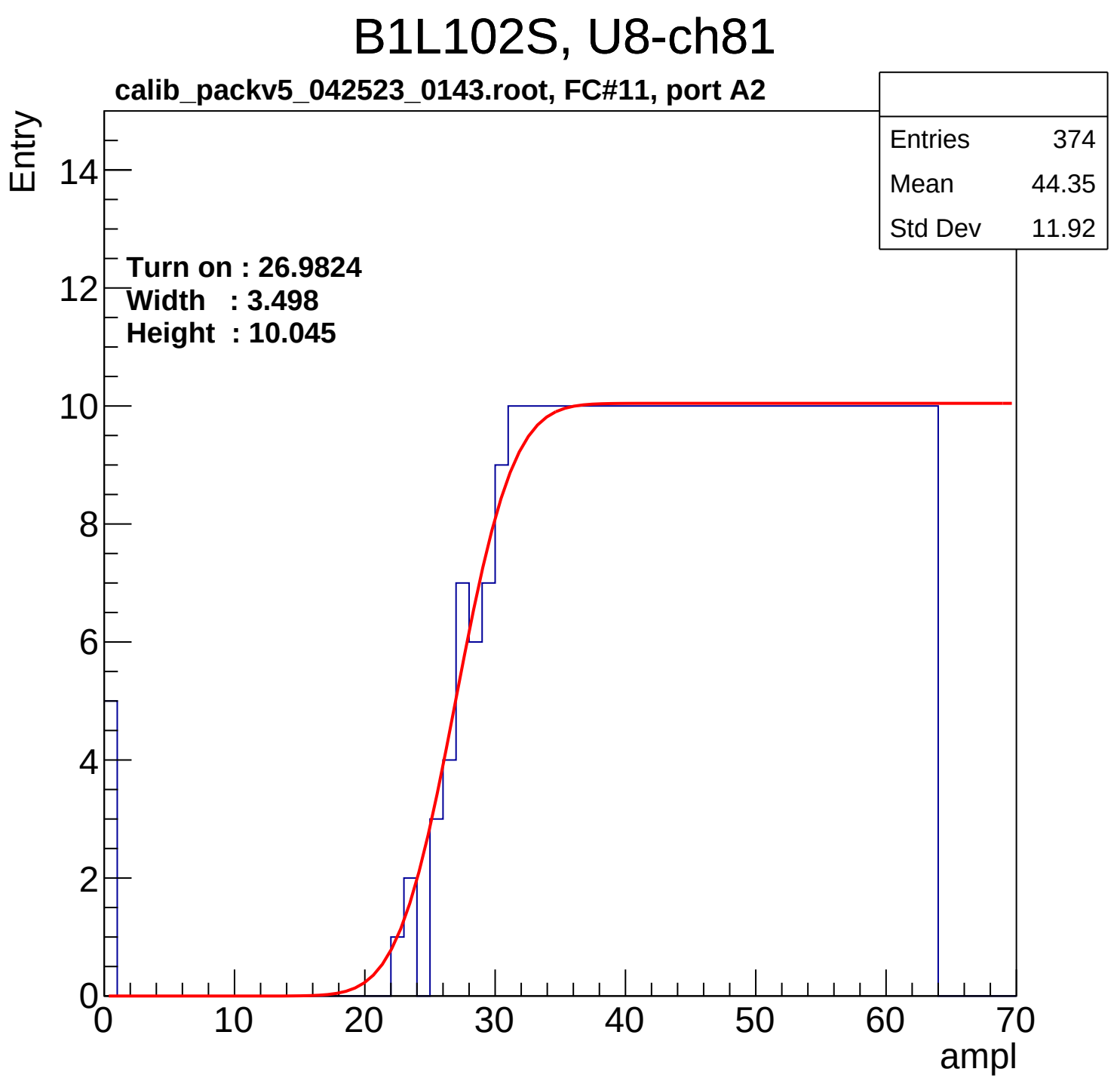
B1L102S, U8-ch81
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.35
Std Dev 11.92
Turn on : 26.9824
Width : 3.498
Height : 10.045
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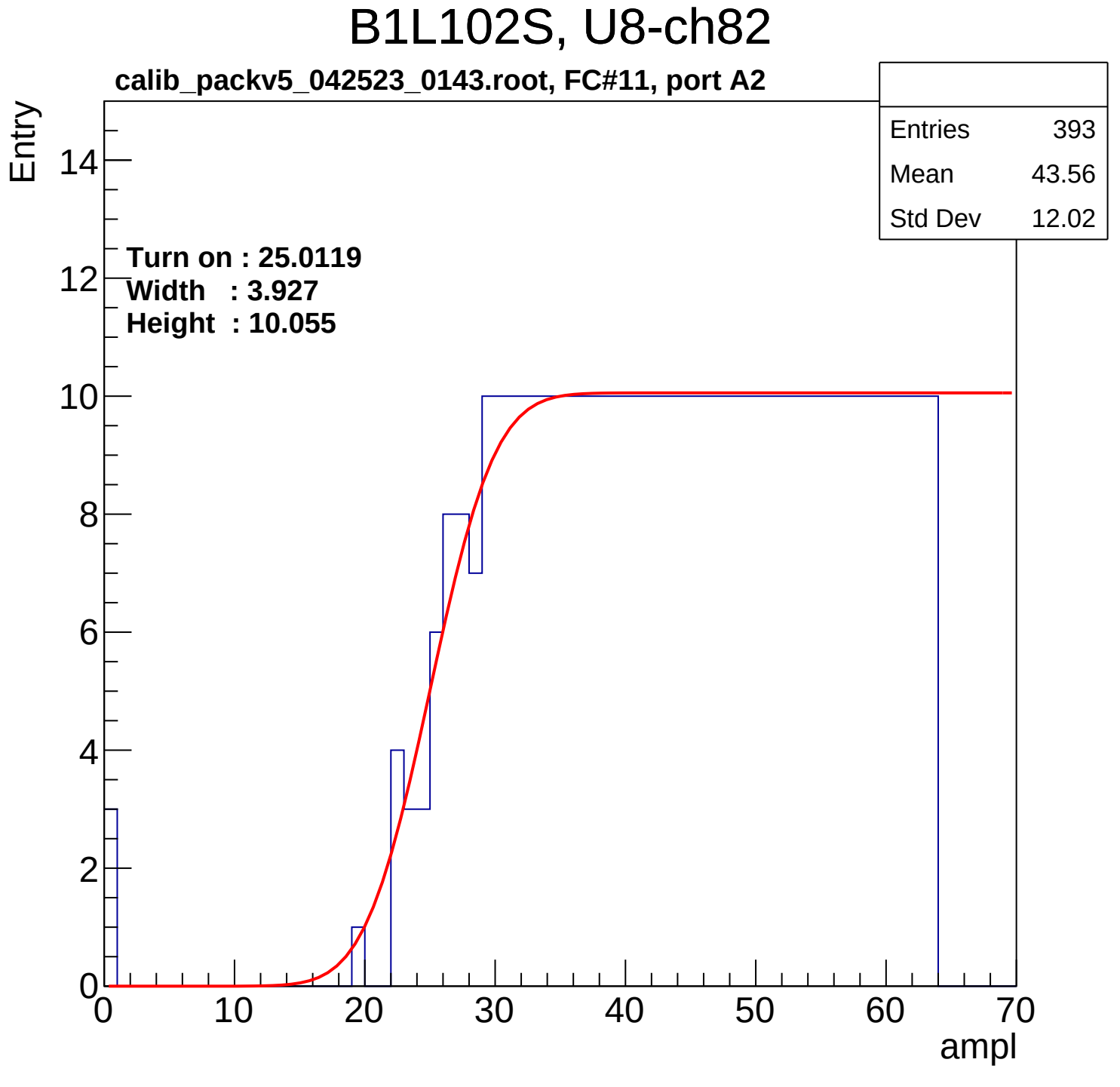
B1L102S, U8-ch82
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.56
Std Dev 12.02
Turn on : 25.0119
Width : 3.927
Height : 10.055
Entry
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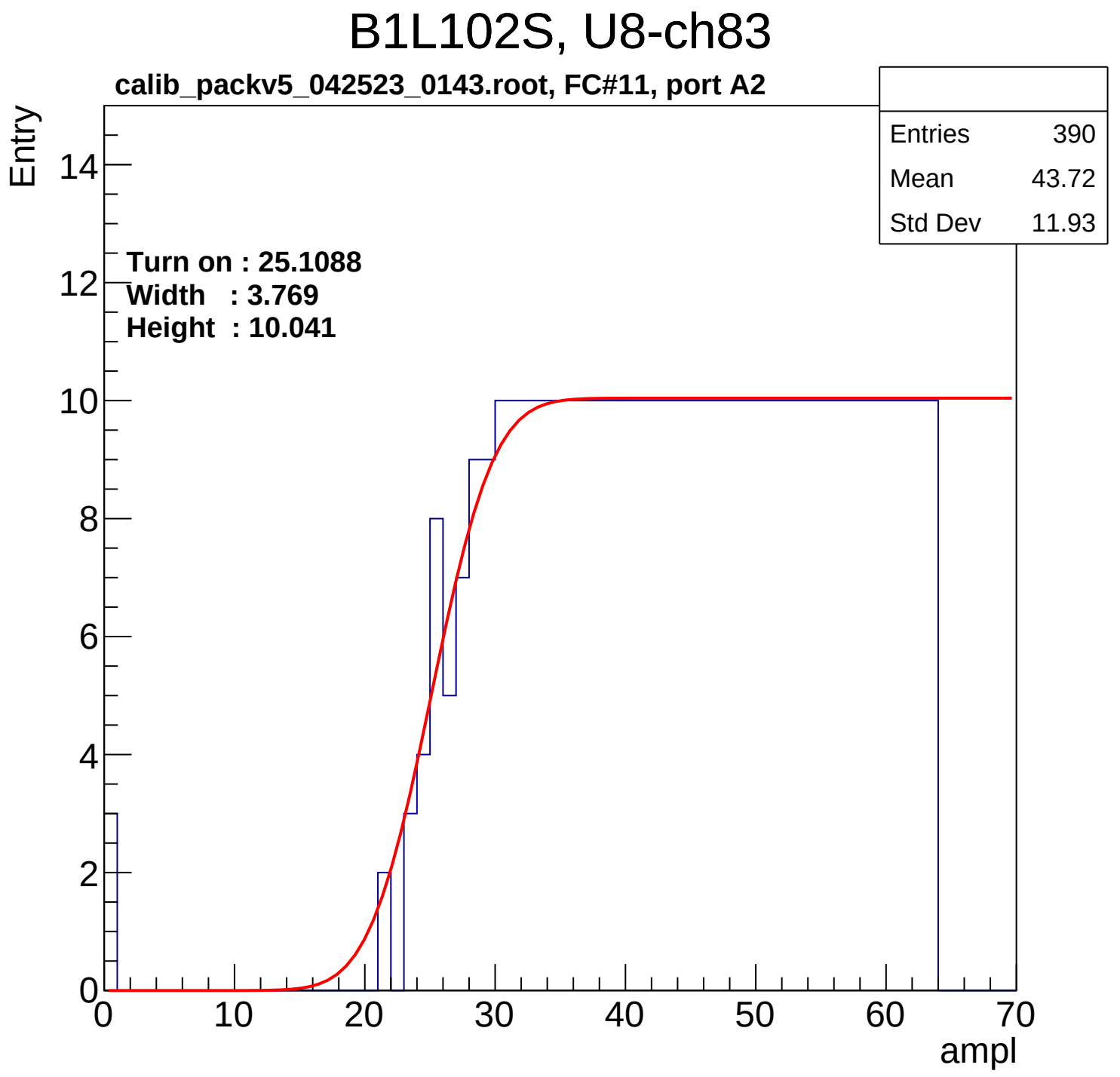
B1L102S, U8-ch83
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.72
Std Dev 11.93
Turn on : 25.1088
Width : 3.769
Height : 10.041
Entry
ampl
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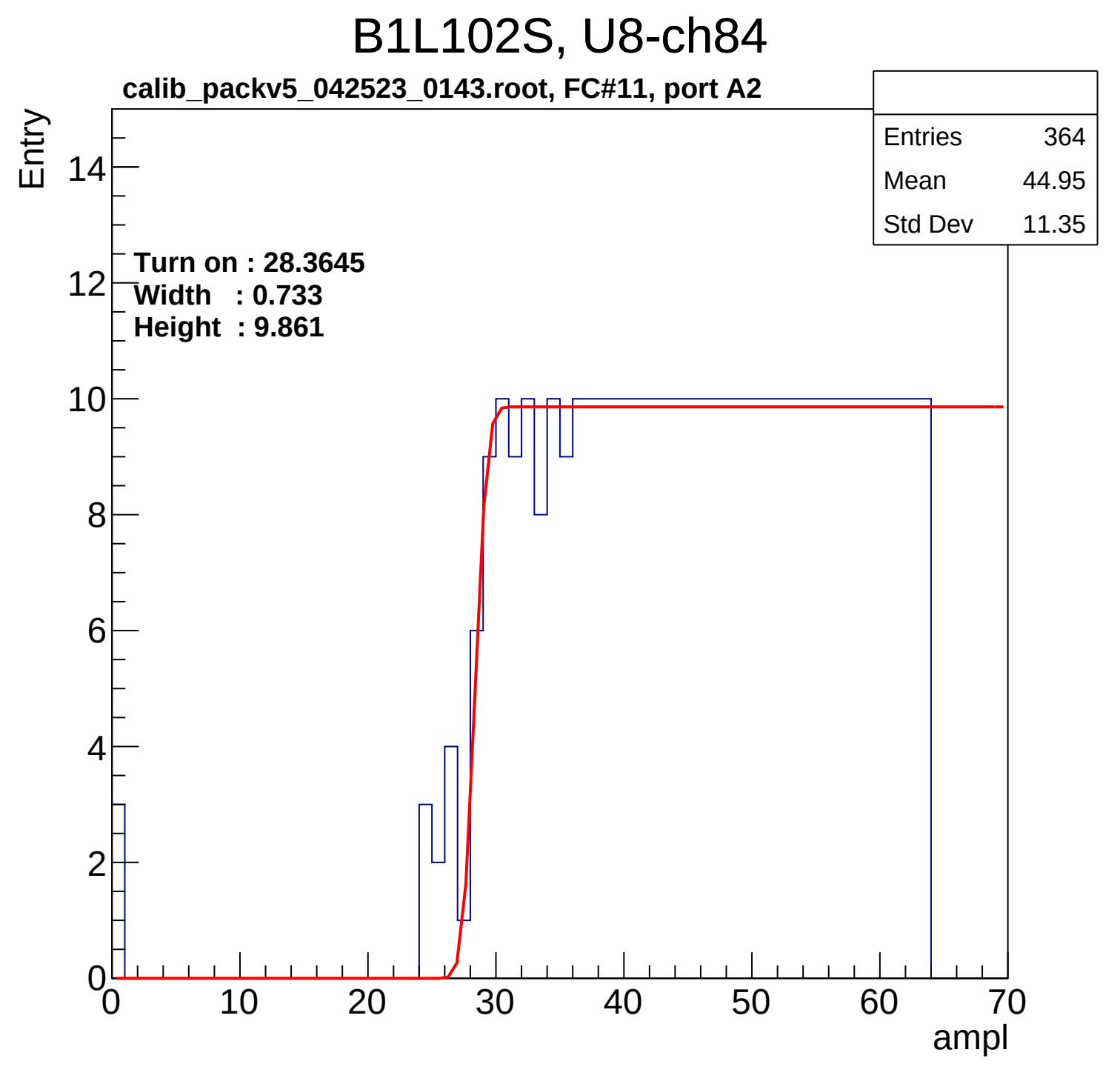
B1L102S, U8-ch84
calib_packv5_042523_0143.root, FC#11, port A2
Entries 364
Mean 44.95
Std Dev 11.35
Turn on : 28.3645
Width : 0.733
Height : 9.861
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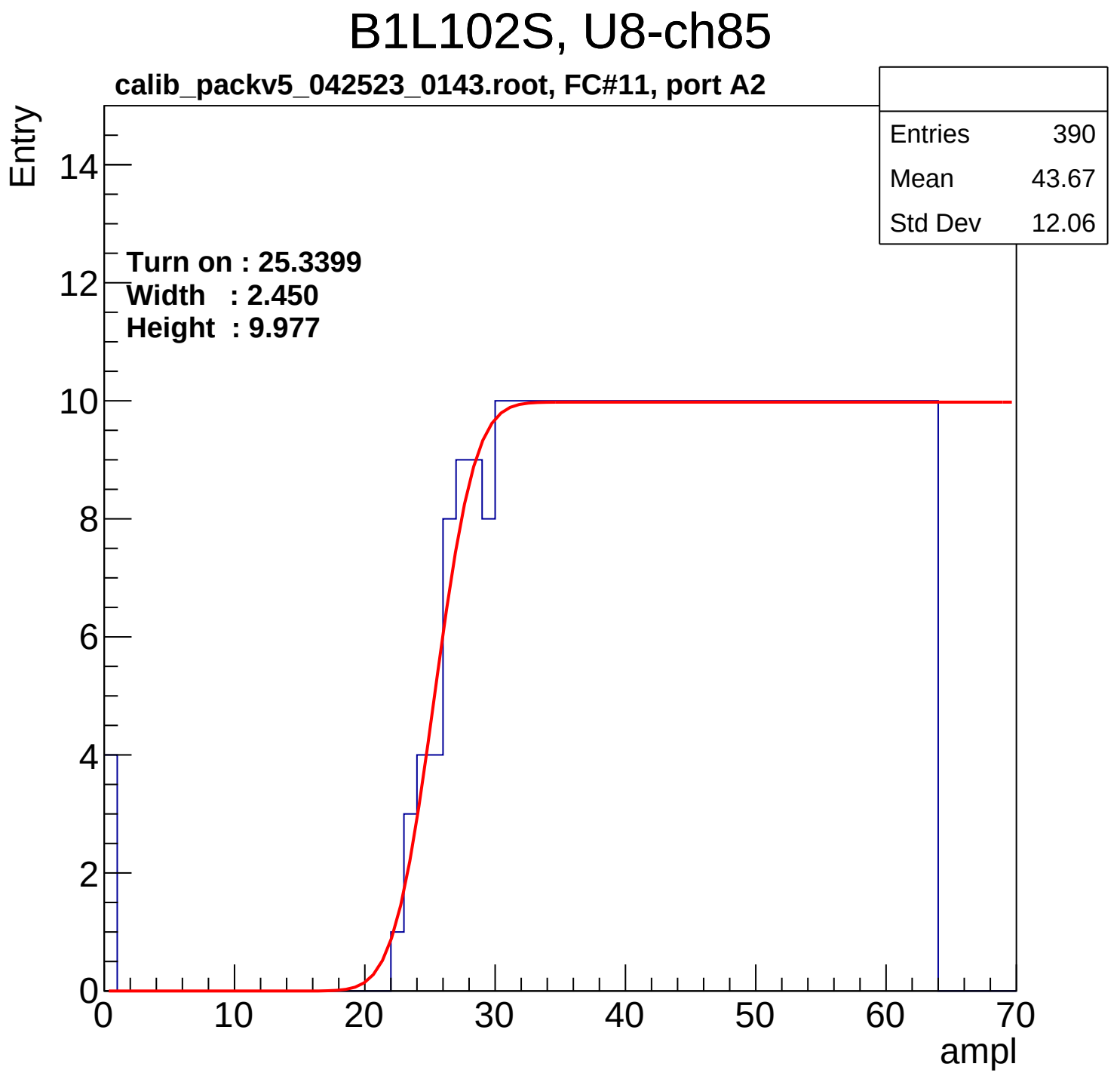
B1L102S, U8-ch85
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.67
Std Dev 12.06
Turn on : 25.3399
Width : 2.450
Height : 9.977
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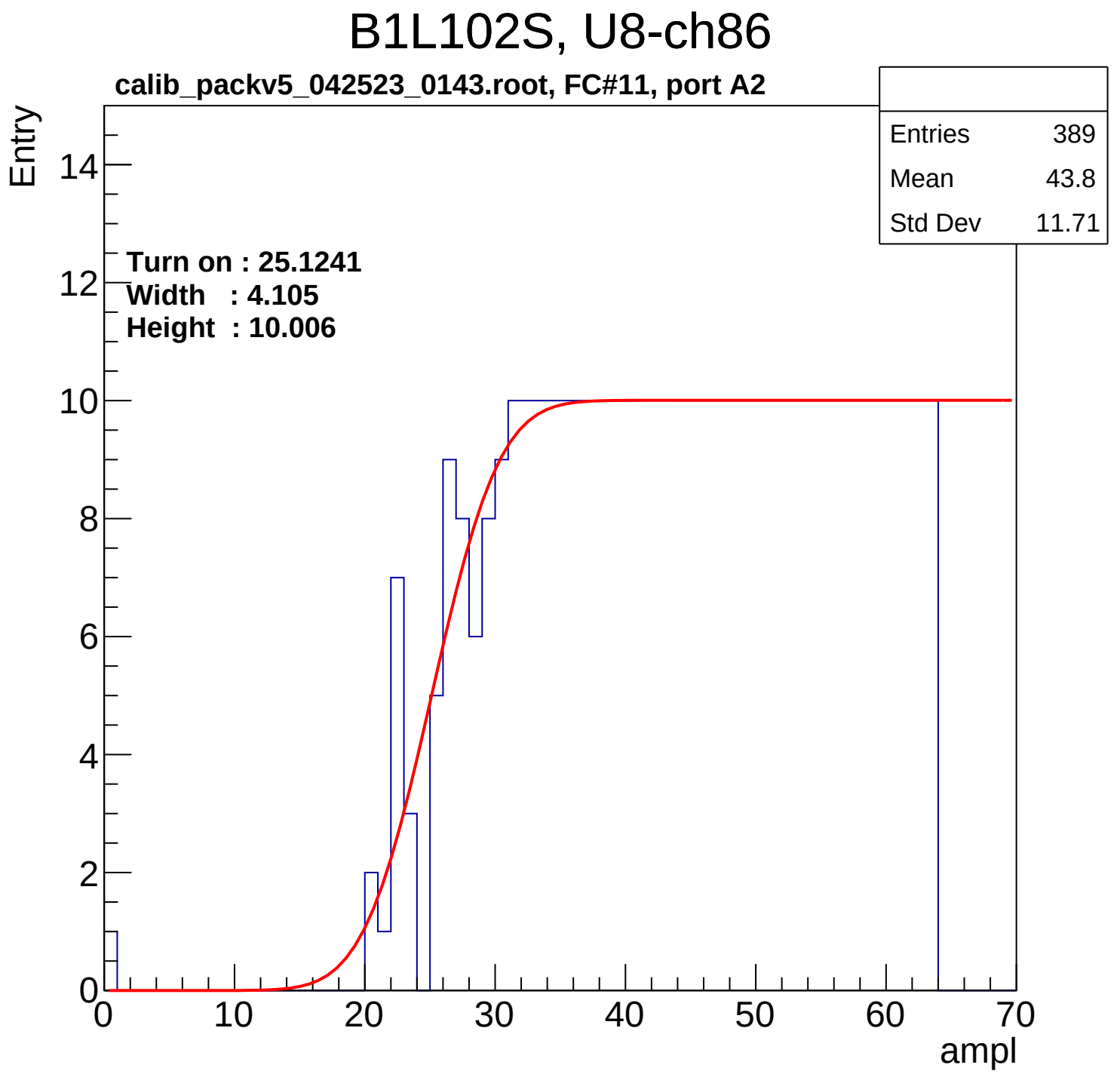
B1L102S, U8-ch86
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.8
Std Dev 11.71
Turn on : 25.1241
Width : 4.105
Height : 10.006
Entry
ampl
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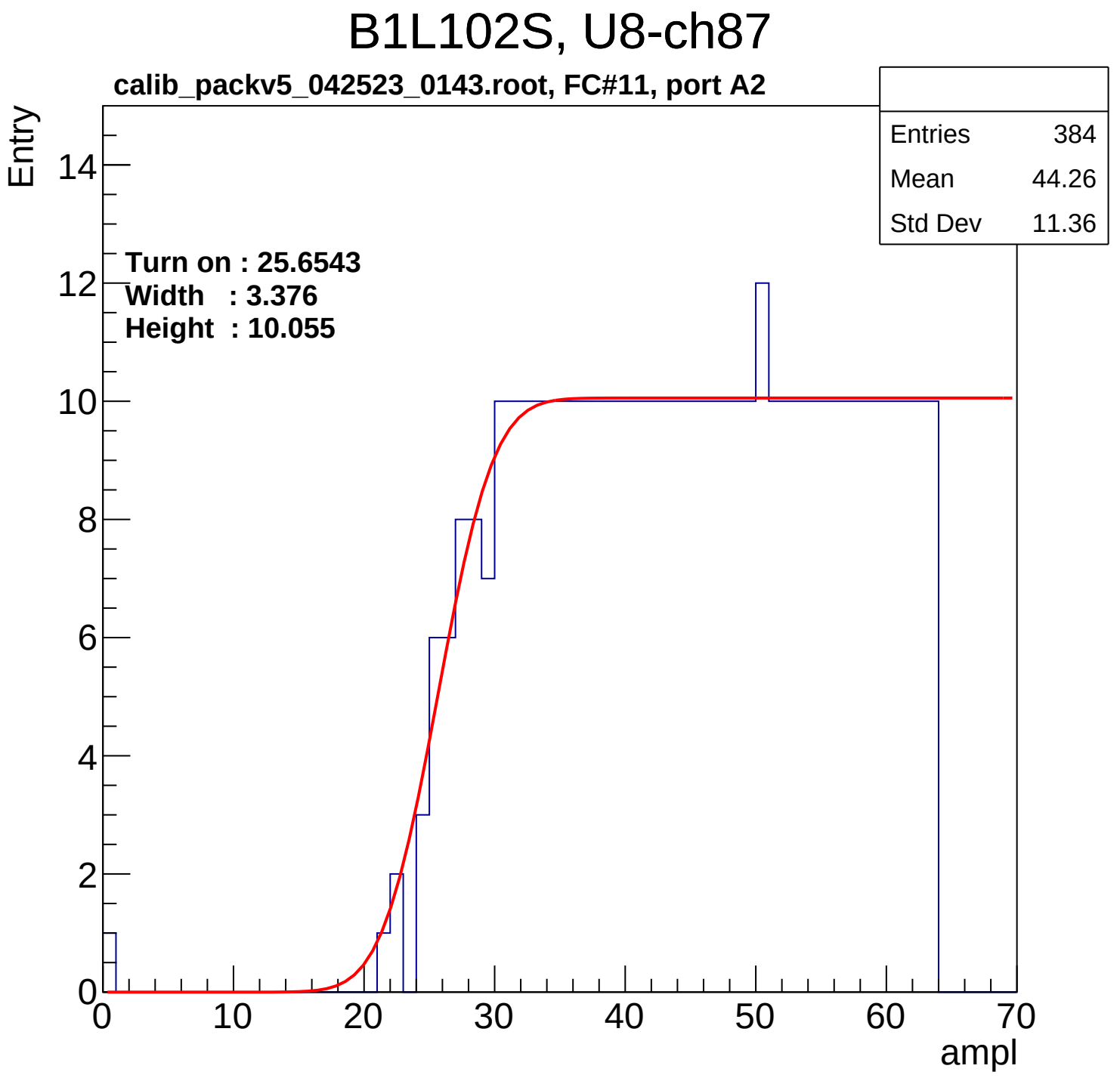
B1L102S, U8-ch87
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.26
Std Dev 11.36
Turn on : 25.6543
Width : 3.376
Height : 10.055
Entry
ampl
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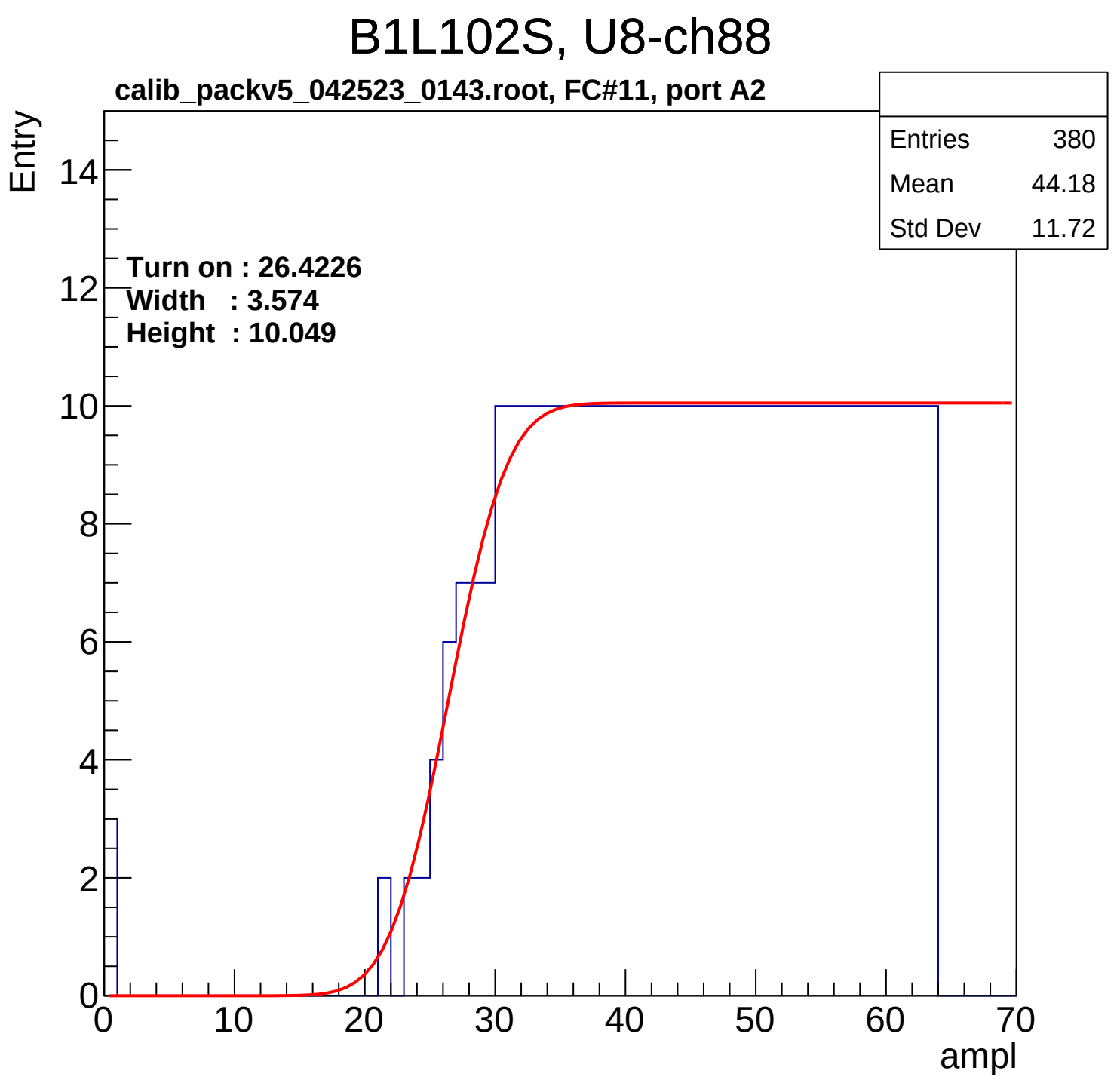
B1L102S, U8-ch88
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.18
Std Dev 11.72
Turn on : 26.4226
Width : 3.574
Height : 10.049
Entry
ampl
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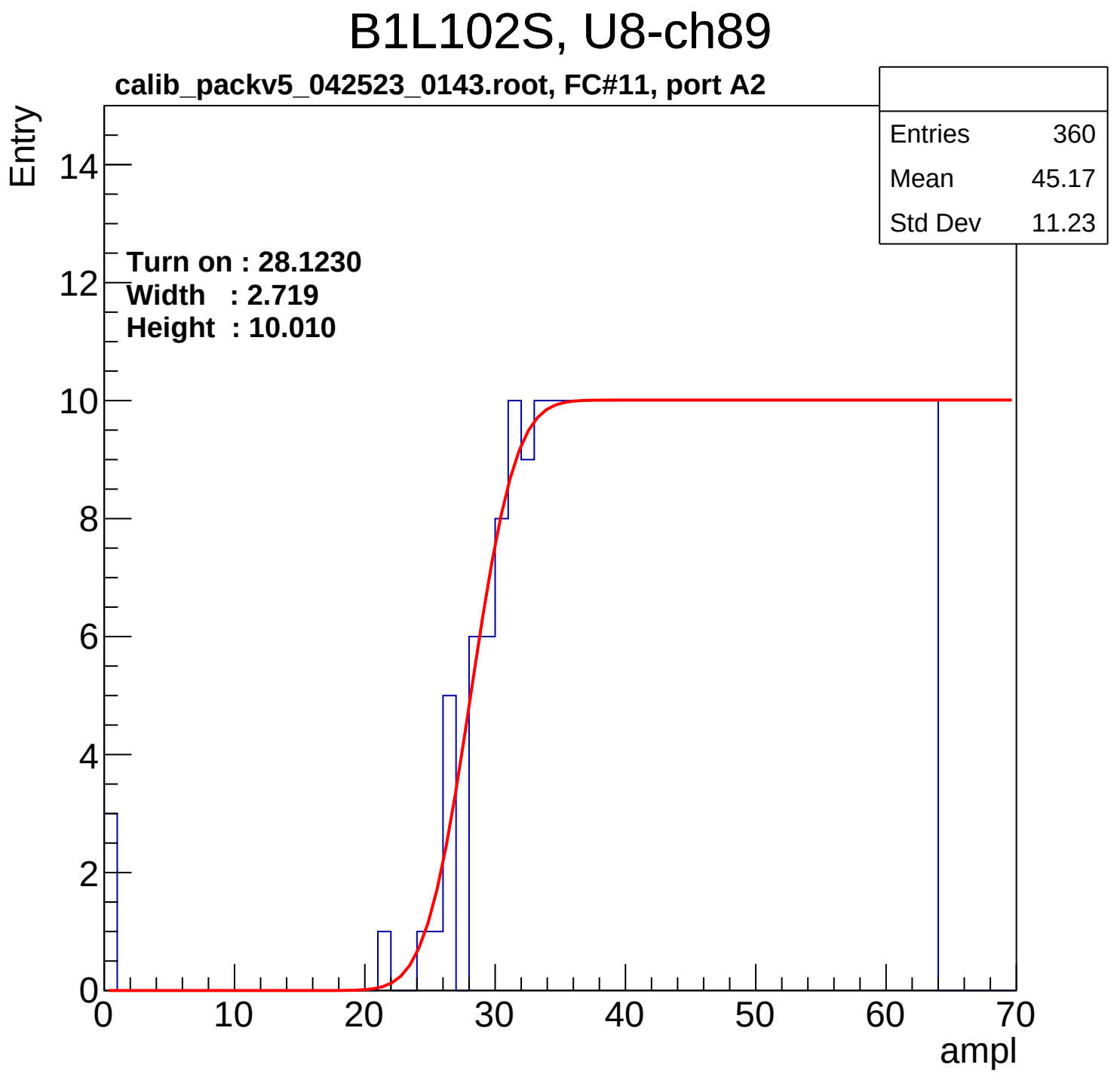
B1L102S, U8-ch89
calib_packv5_042523_0143.root, FC#11, port A2
Entries 360
Mean 45.17
Std Dev 11.23
Turn on : 28.1230
Width : 2.719
Height : 10.010
Entry
ampl
0
2
4
6
8
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0
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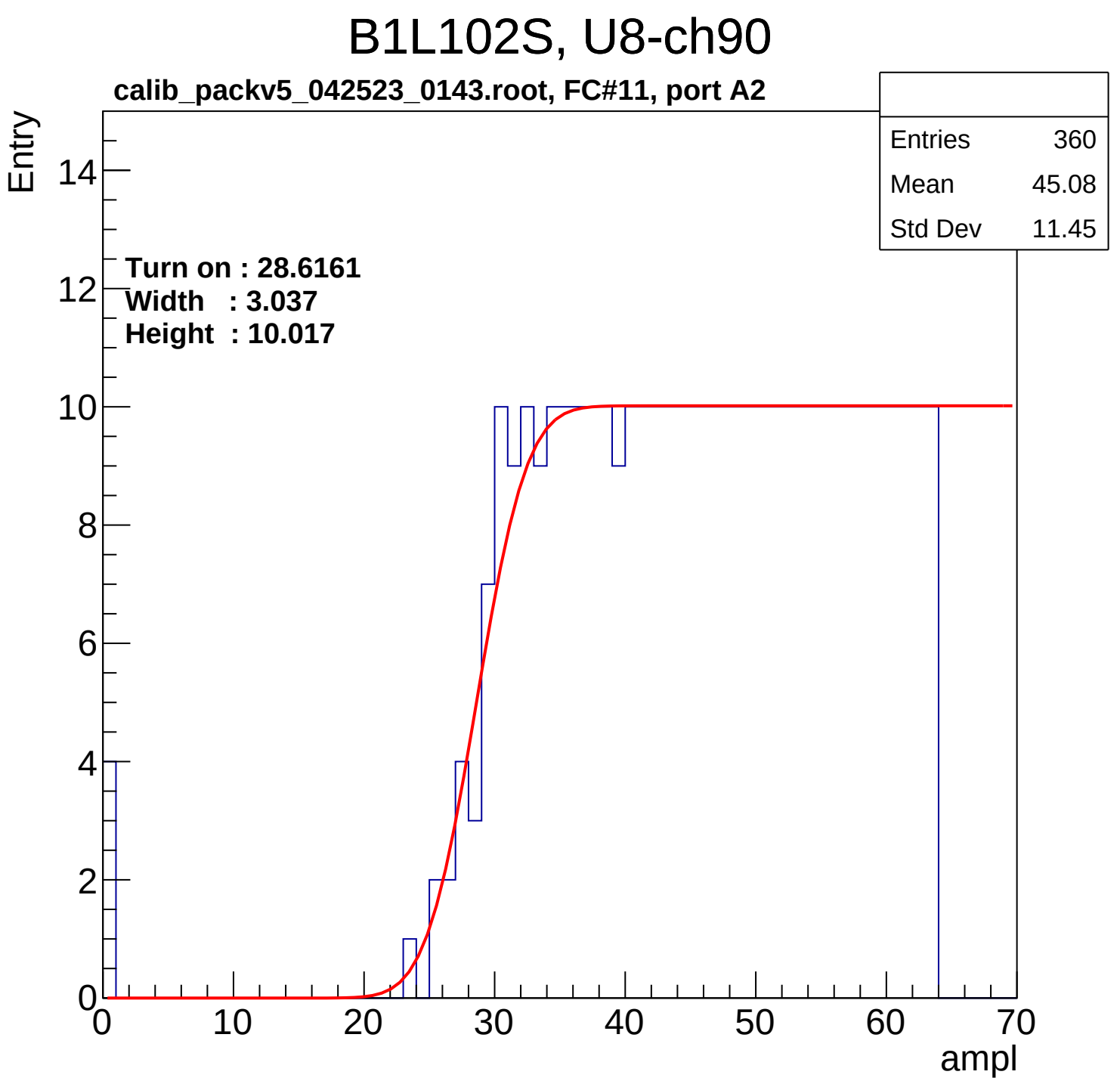
B1L102S, U8-ch90
calib_packv5_042523_0143.root, FC#11, port A2
Entries 360
Mean 45.08
Std Dev 11.45
Turn on : 28.6161
Width : 3.037
Height : 10.017
Entry
ampl
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2
4
6
8
10
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0
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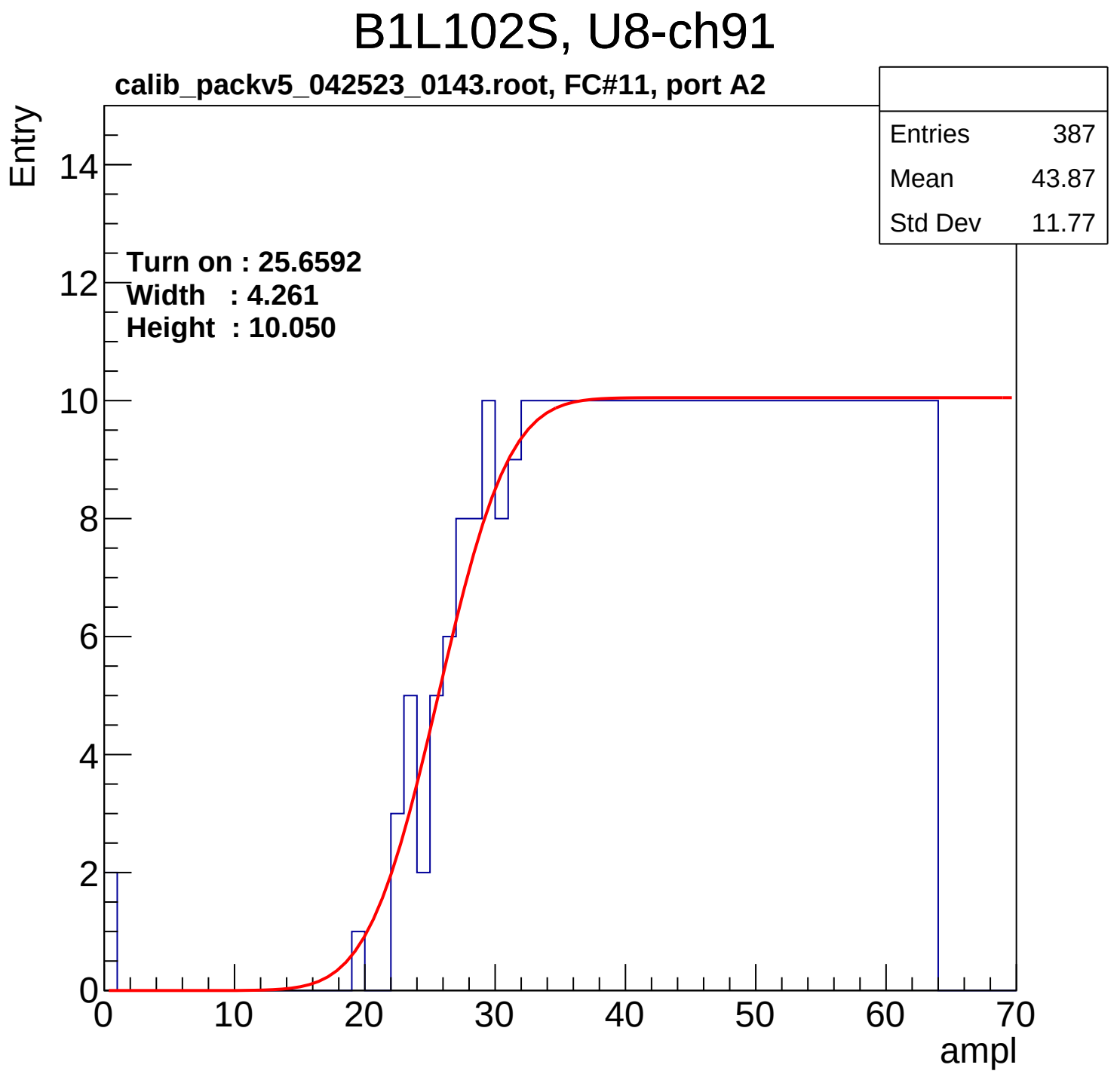
B1L102S, U8-ch91
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.87
Std Dev 11.77
Turn on : 25.6592
Width : 4.261
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
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0
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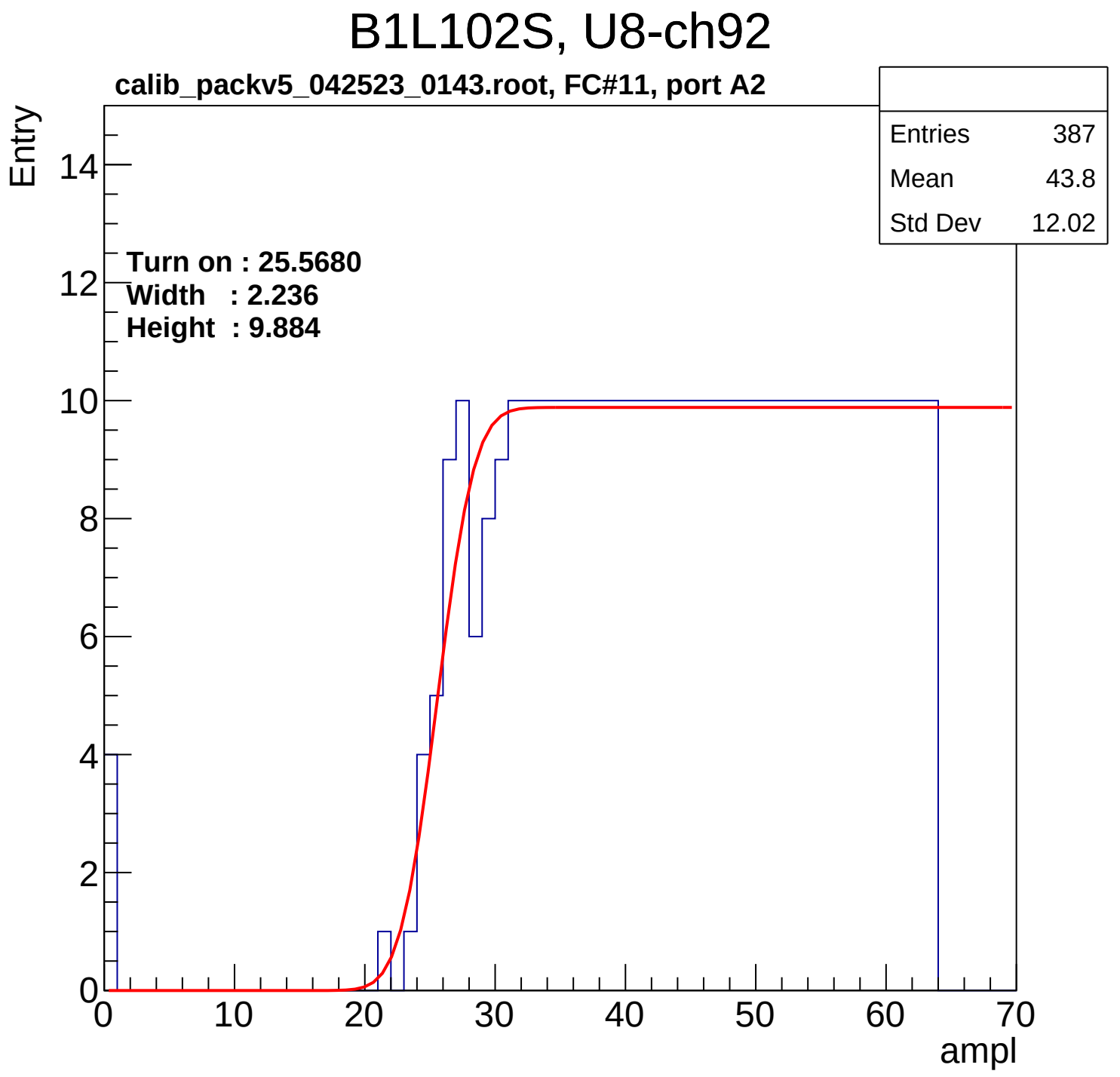
B1L102S, U8-ch92
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.8
Std Dev 12.02
Turn on : 25.5680
Width : 2.236
Height : 9.884
Entry
ampl
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2
4
6
8
10
12
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0
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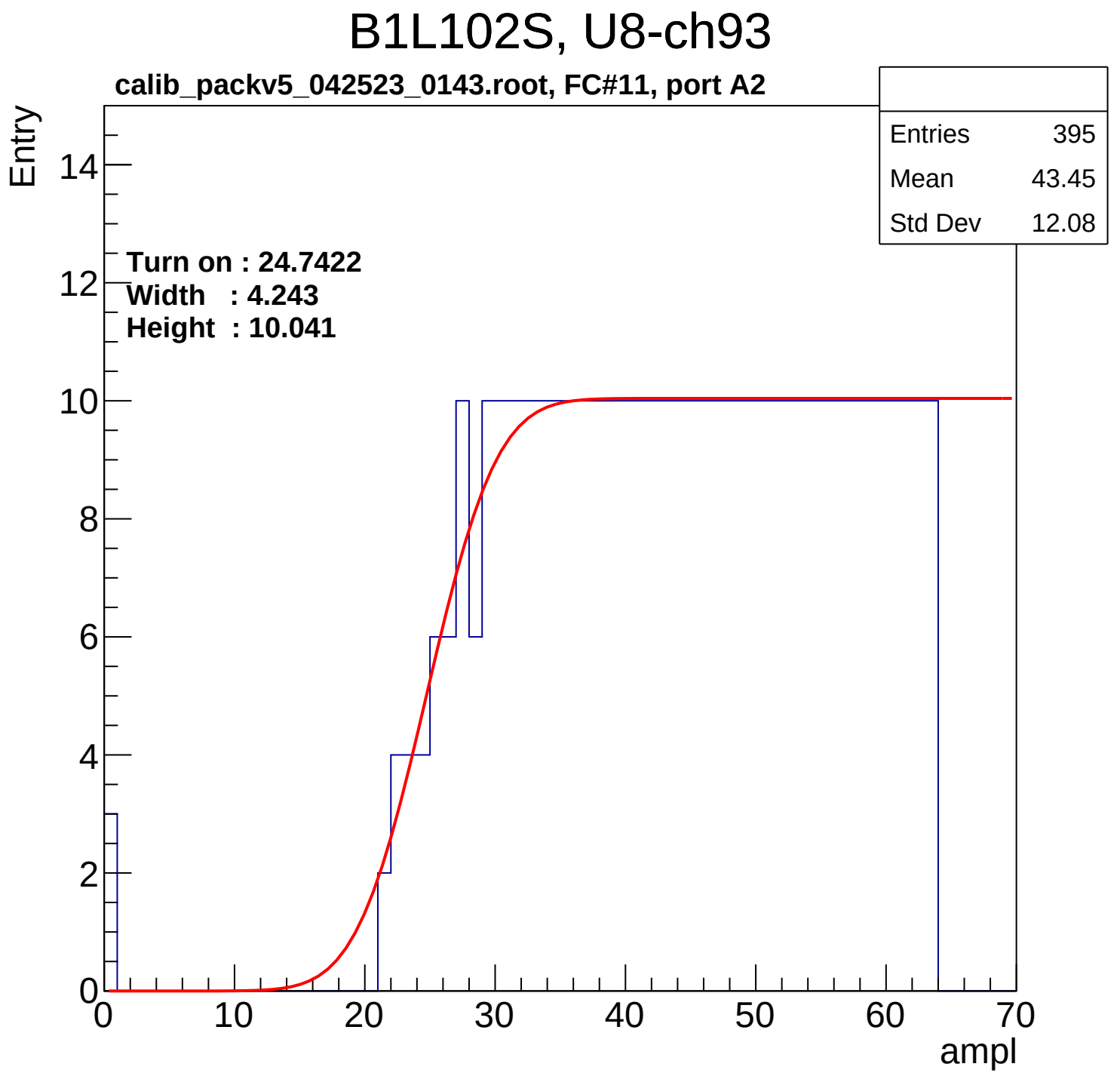
B1L102S, U8-ch93
calib_packv5_042523_0143.root, FC#11, port A2
Entries 395
Mean 43.45
Std Dev 12.08
Turn on : 24.7422
Width : 4.243
Height : 10.041
Entry
ampl
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2
4
6
8
10
12
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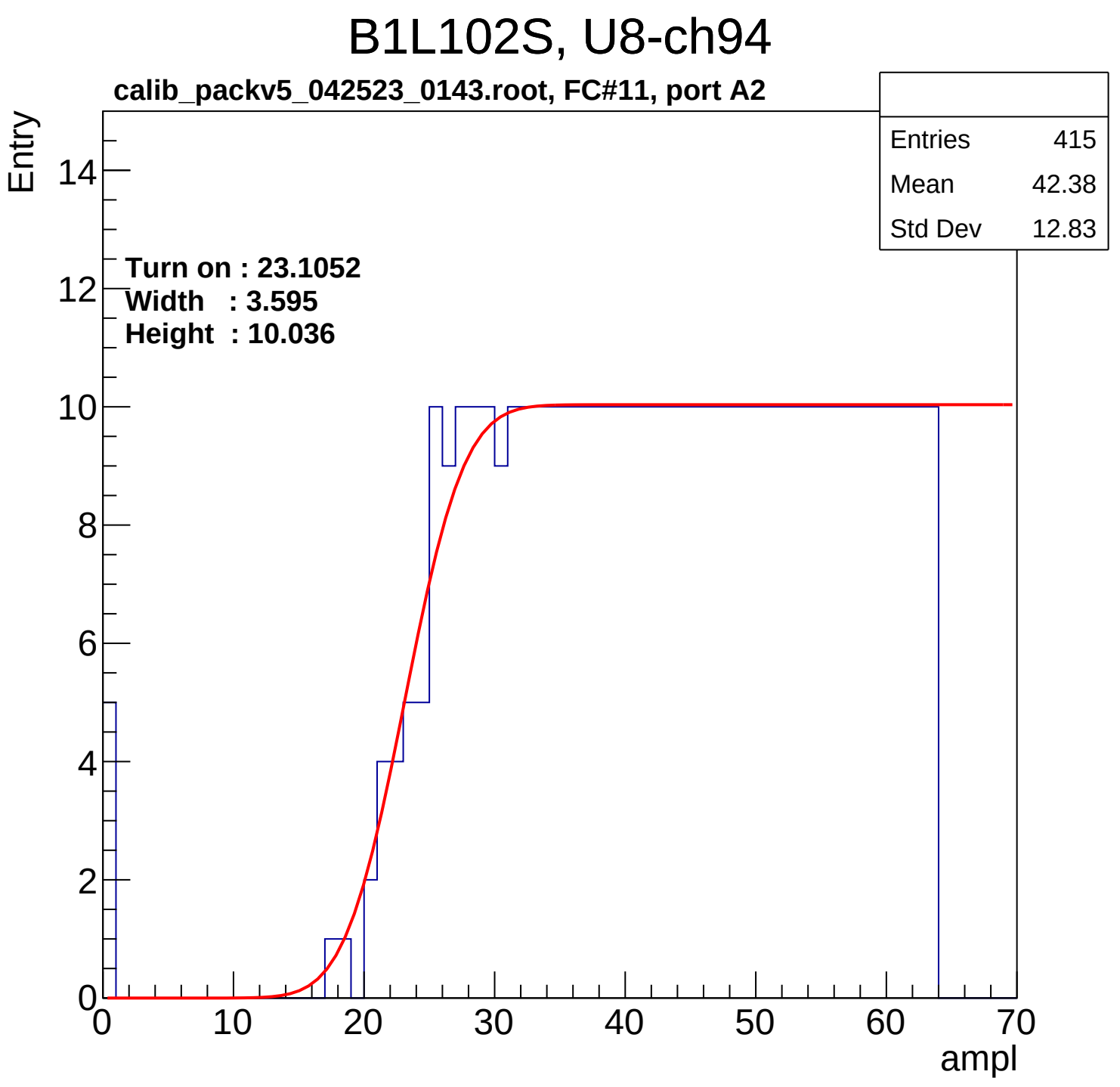
B1L102S, U8-ch94
calib_packv5_042523_0143.root, FC#11, port A2
Entries 415
Mean 42.38
Std Dev 12.83
Turn on : 23.1052
Width : 3.595
Height : 10.036
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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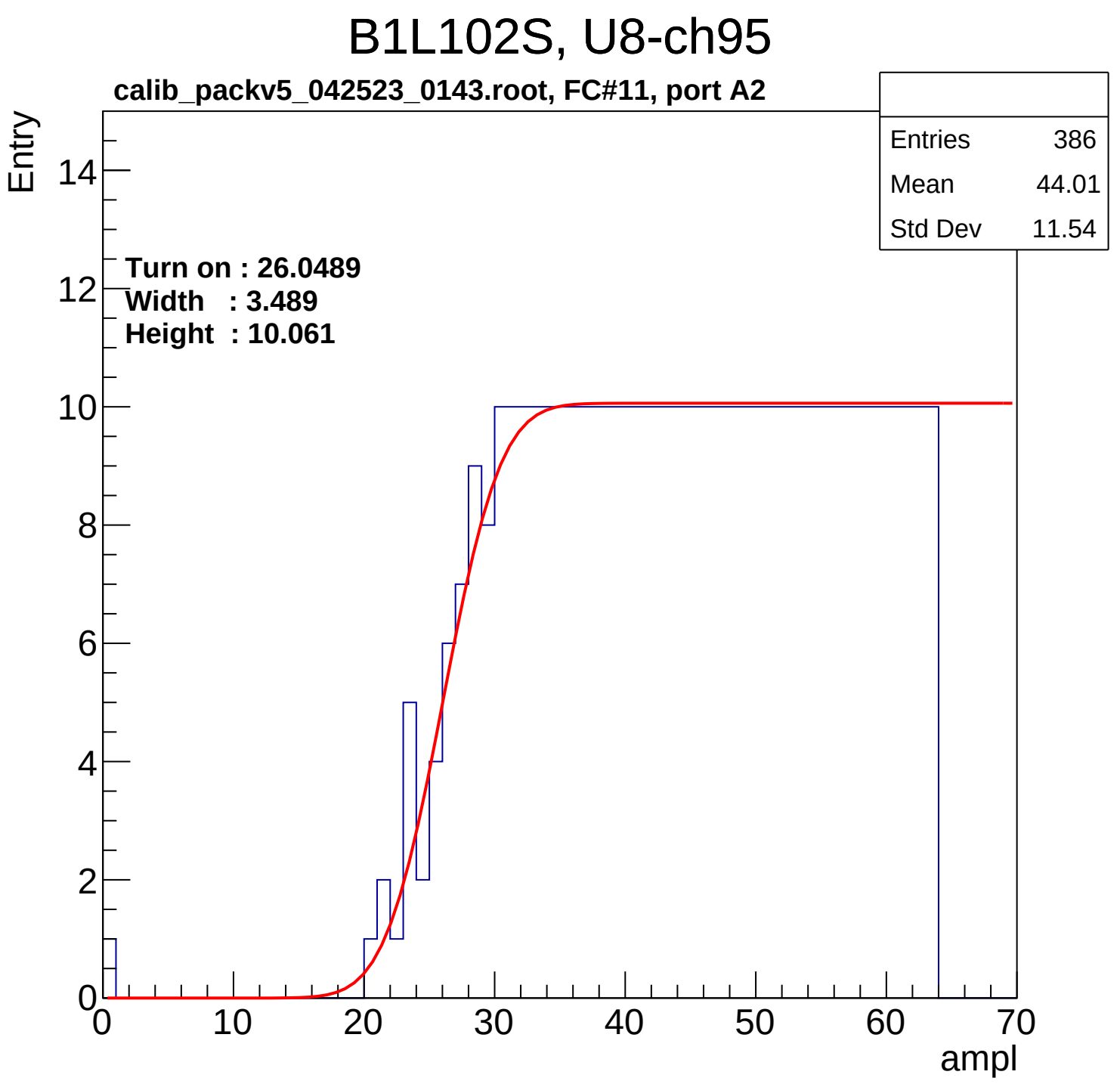
B1L102S, U8-ch95
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 44.01
Std Dev 11.54
Turn on : 26.0489
Width : 3.489
Height : 10.061
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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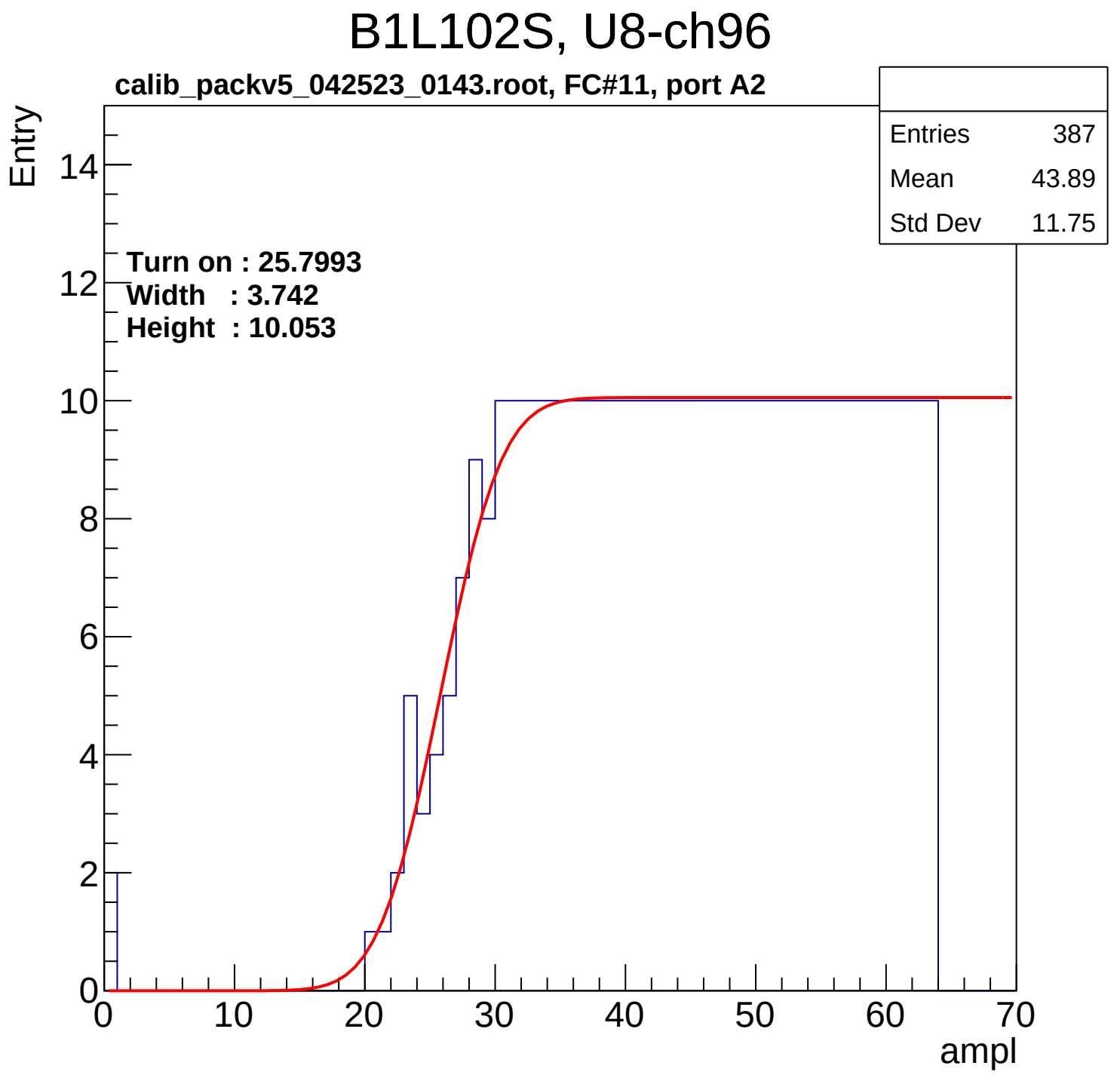
B1L102S, U8-ch96
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.89
Std Dev 11.75
Turn on : 25.7993
Width : 3.742
Height : 10.053
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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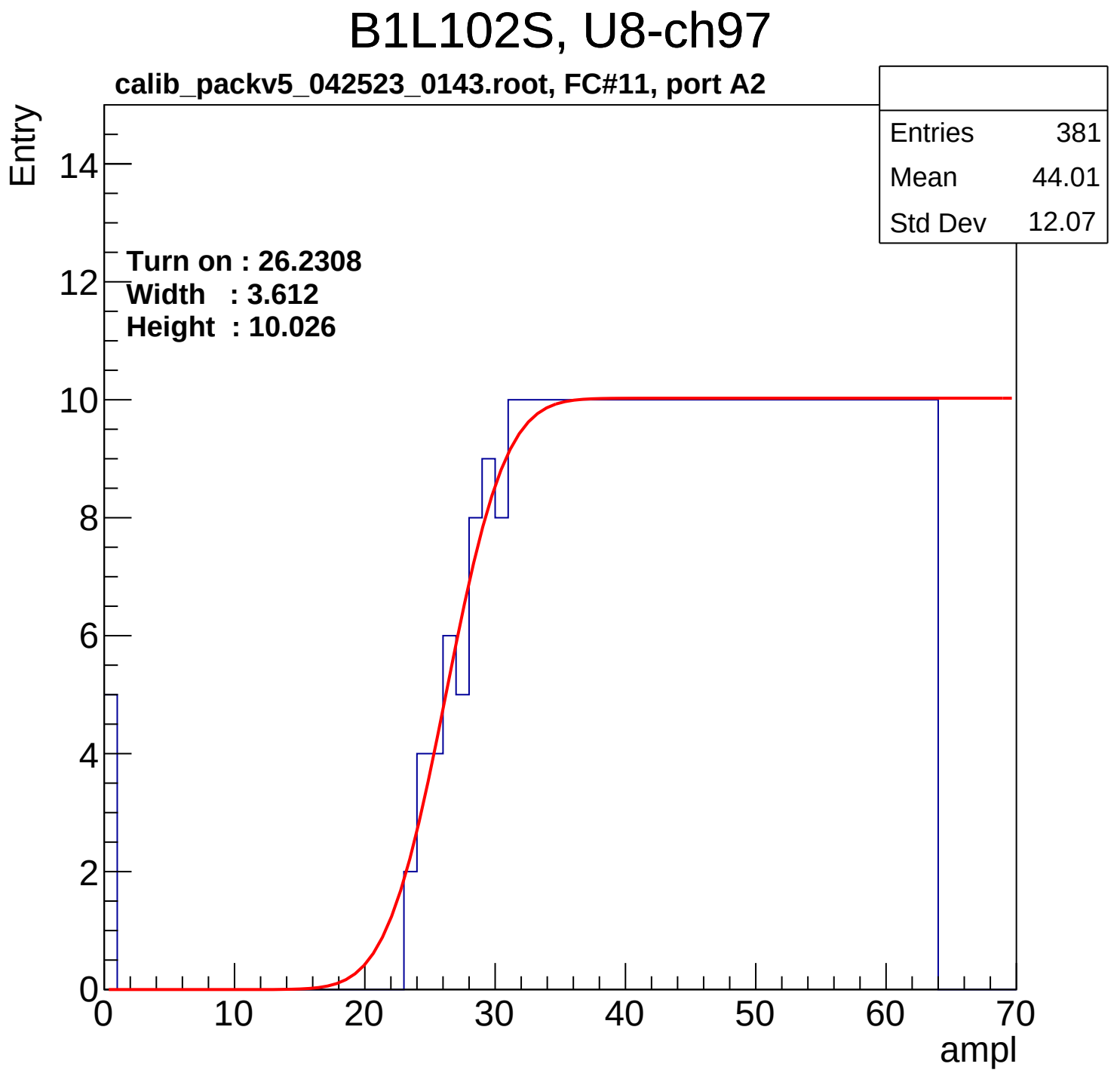
B1L102S, U8-ch97
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.01
Std Dev 12.07
Turn on : 26.2308
Width : 3.612
Height : 10.026
Entry
ampl
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2
4
6
8
10
12
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0
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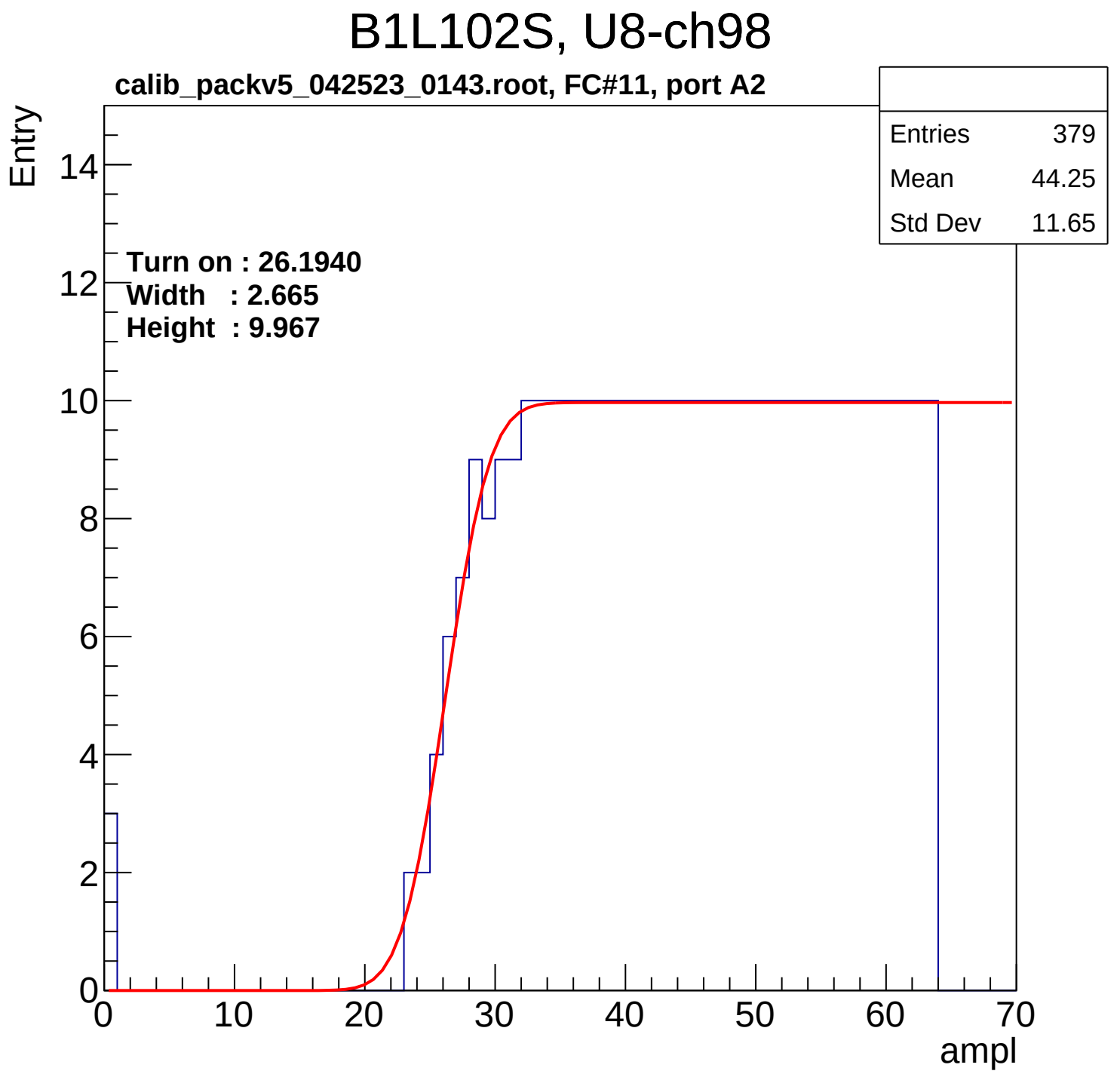
B1L102S, U8-ch98
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.25
Std Dev 11.65
Turn on : 26.1940
Width : 2.665
Height : 9.967
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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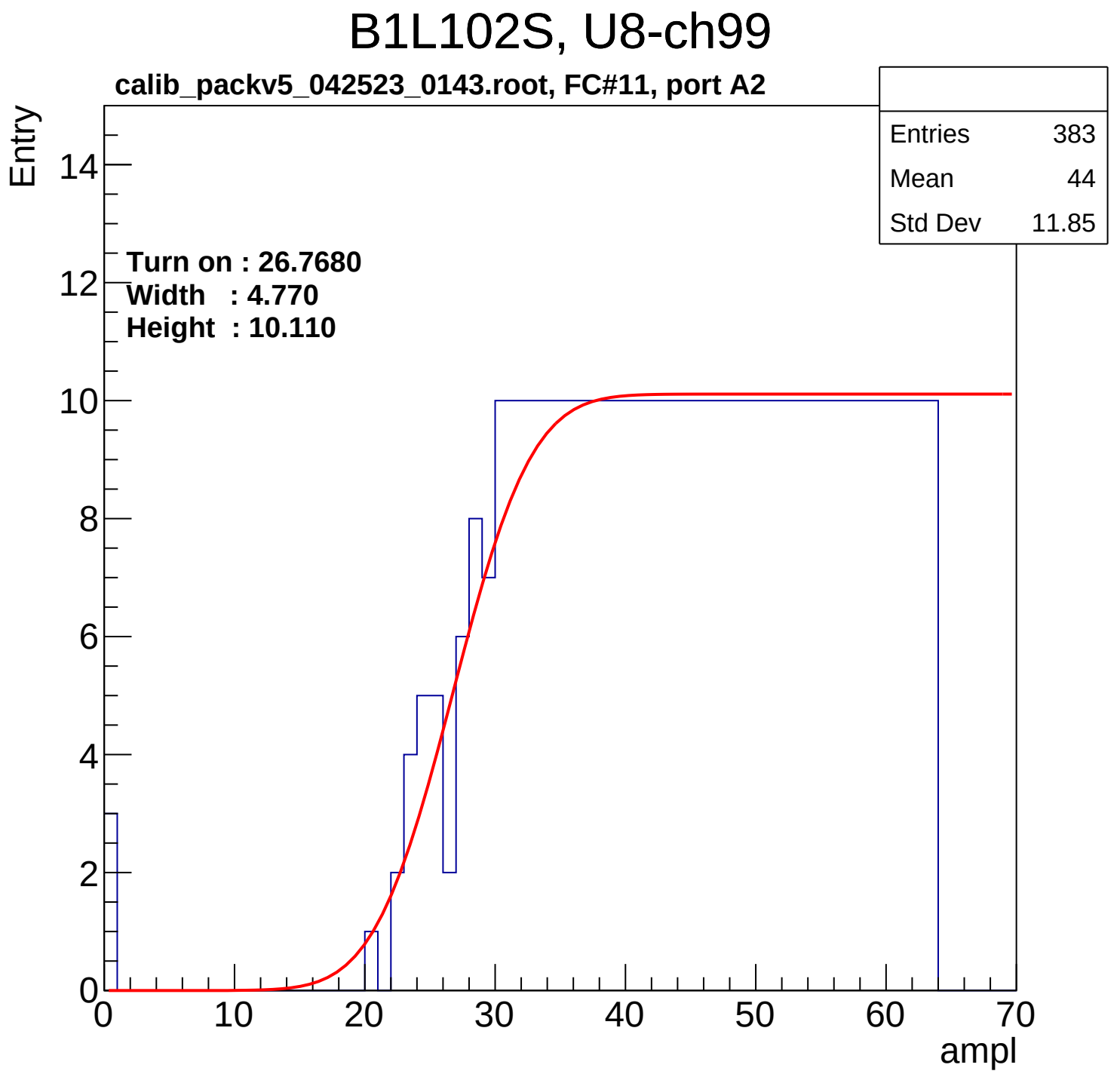
B1L102S, U8-ch99
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44
Std Dev 11.85
Turn on : 26.7680
Width : 4.770
Height : 10.110
Entry
ampl
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4
6
8
10
12
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0
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60
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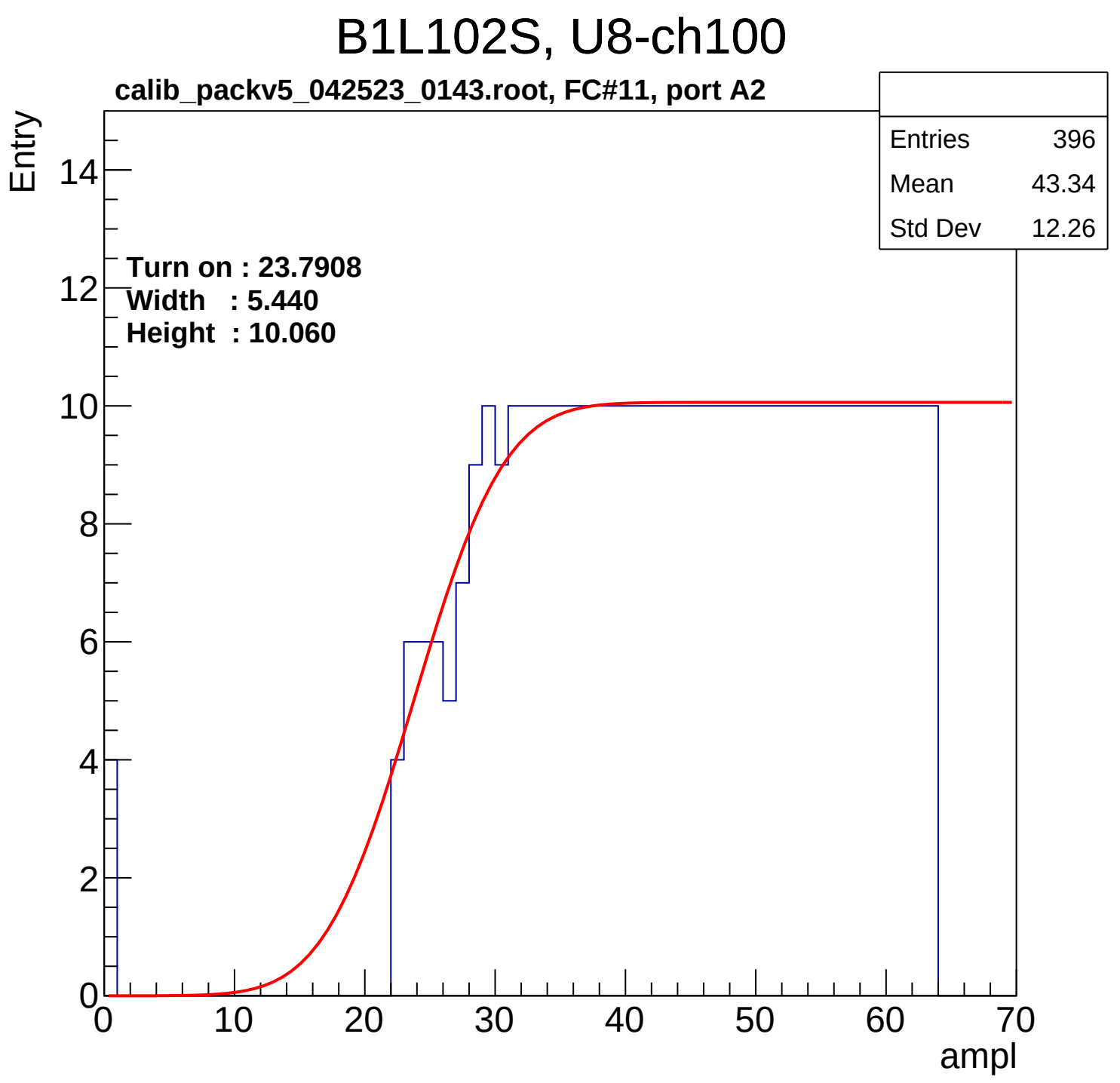
B1L102S, U8-ch100
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.34
Std Dev 12.26
Turn on : 23.7908
Width : 5.440
Height : 10.060
Entry
ampl
0
2
4
6
8
10
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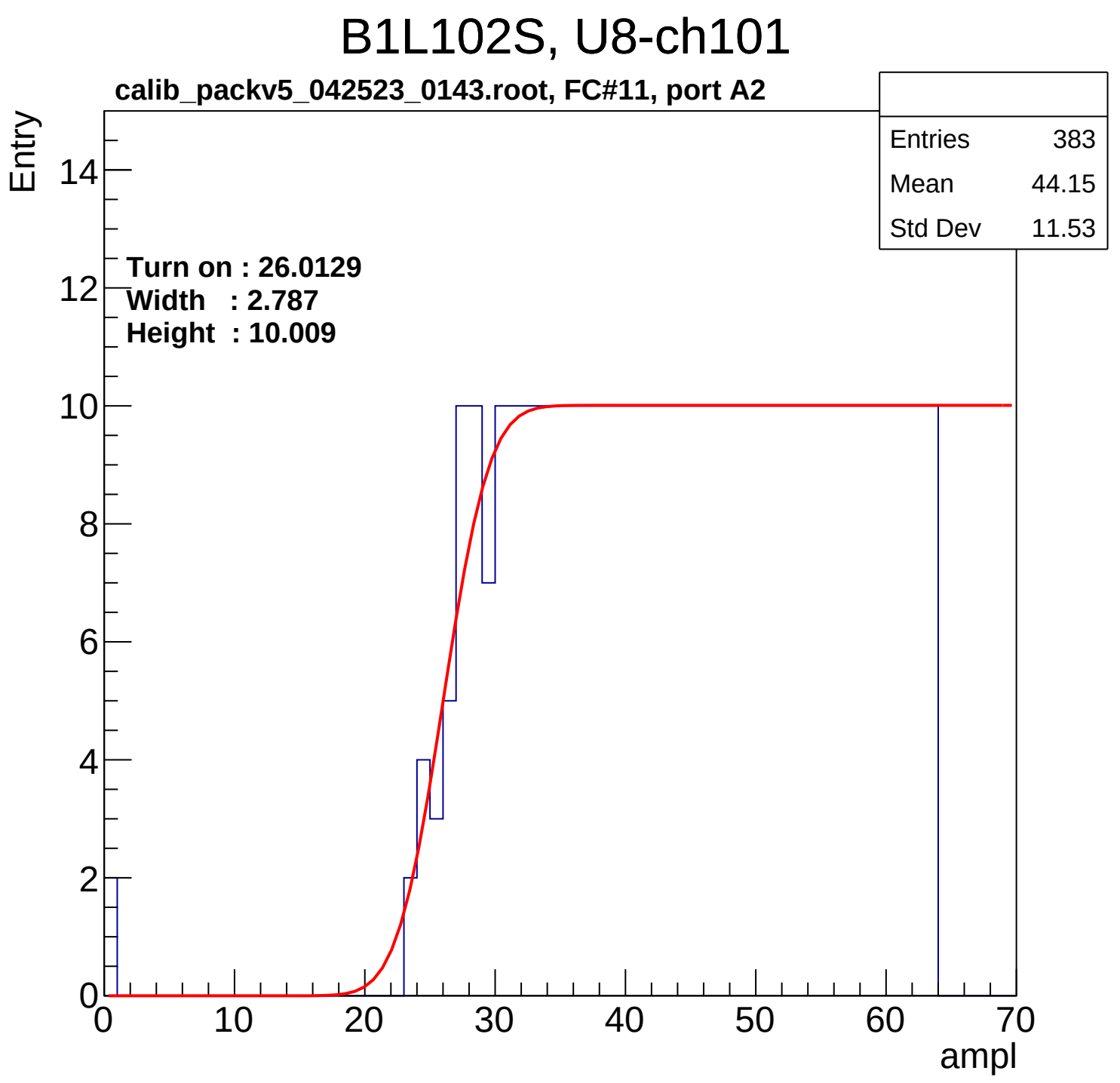
B1L102S, U8-ch101
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.15
Std Dev 11.53
Turn on : 26.0129
Width : 2.787
Height : 10.009
Entry
ampl
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4
6
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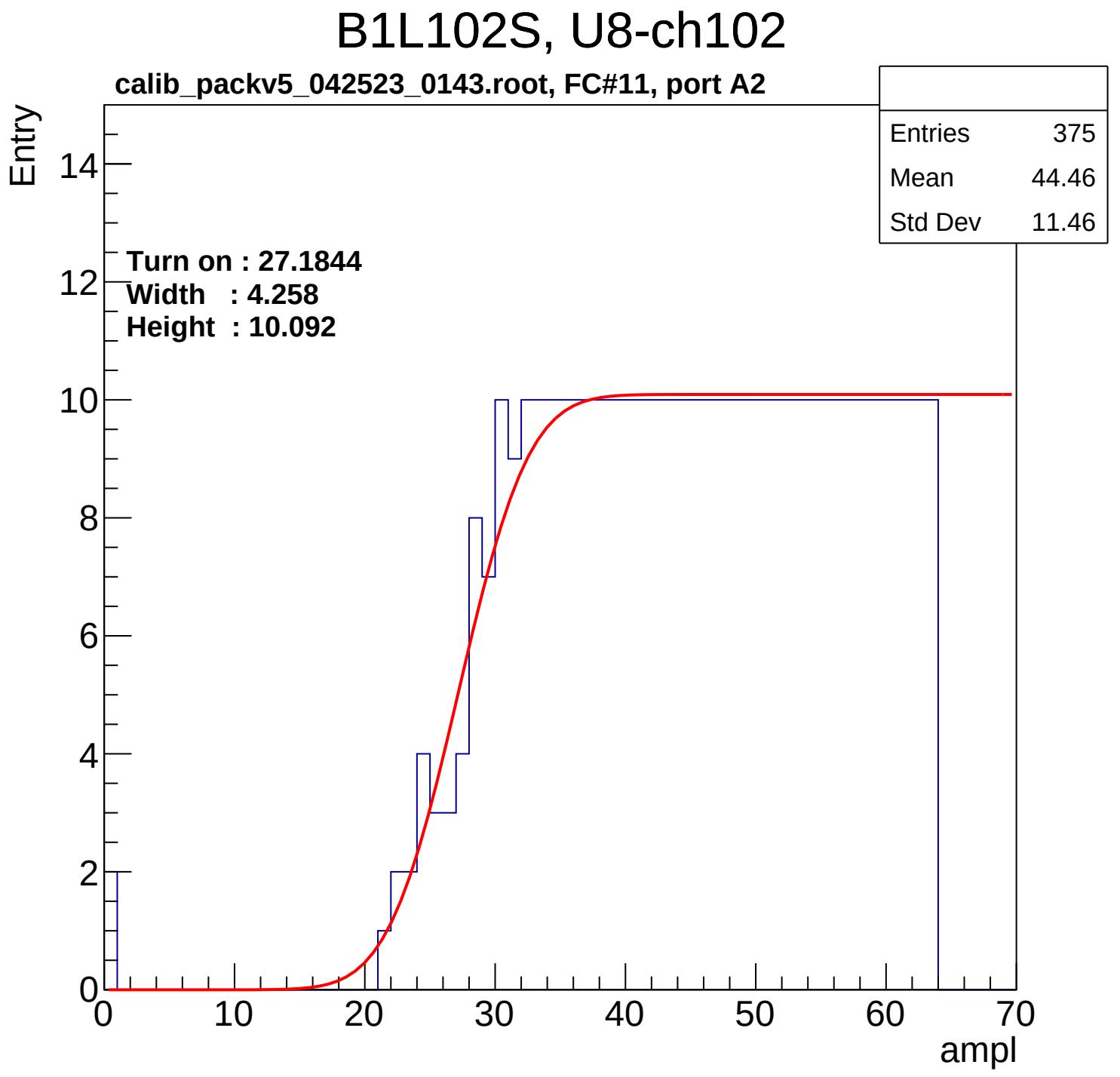
B1L102S, U8-ch102
calib_packv5_042523_0143.root, FC#11, port A2
Entries 375
Mean 44.46
Std Dev 11.46
Turn on : 27.1844
Width : 4.258
Height : 10.092
Entry
ampl
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6
8
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12
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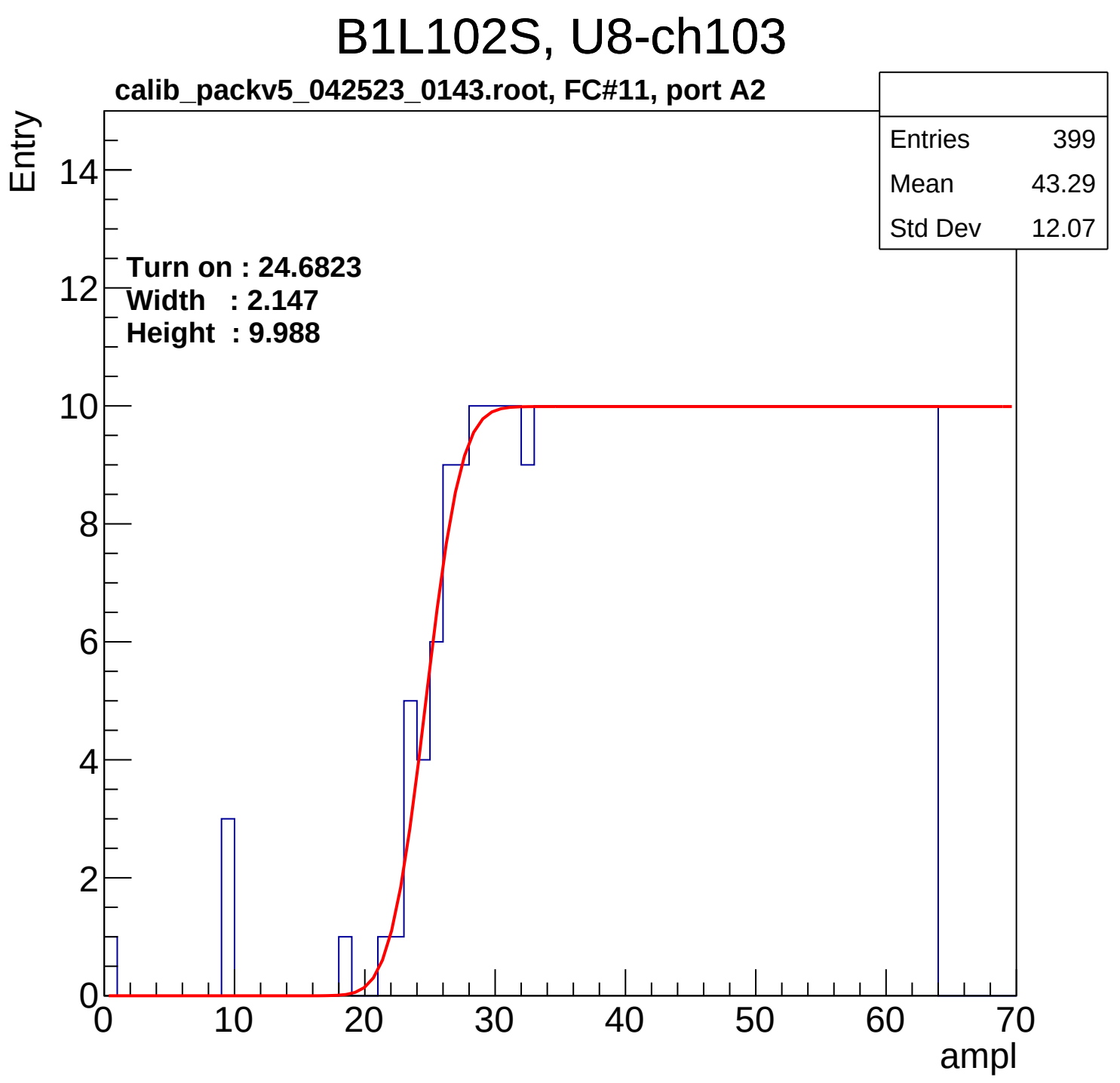
B1L102S, U8-ch103
calib_packv5_042523_0143.root, FC#11, port A2
Entries 399
Mean 43.29
Std Dev 12.07
Turn on : 24.6823
Width : 2.147
Height : 9.988
Entry
ampl
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6
8
10
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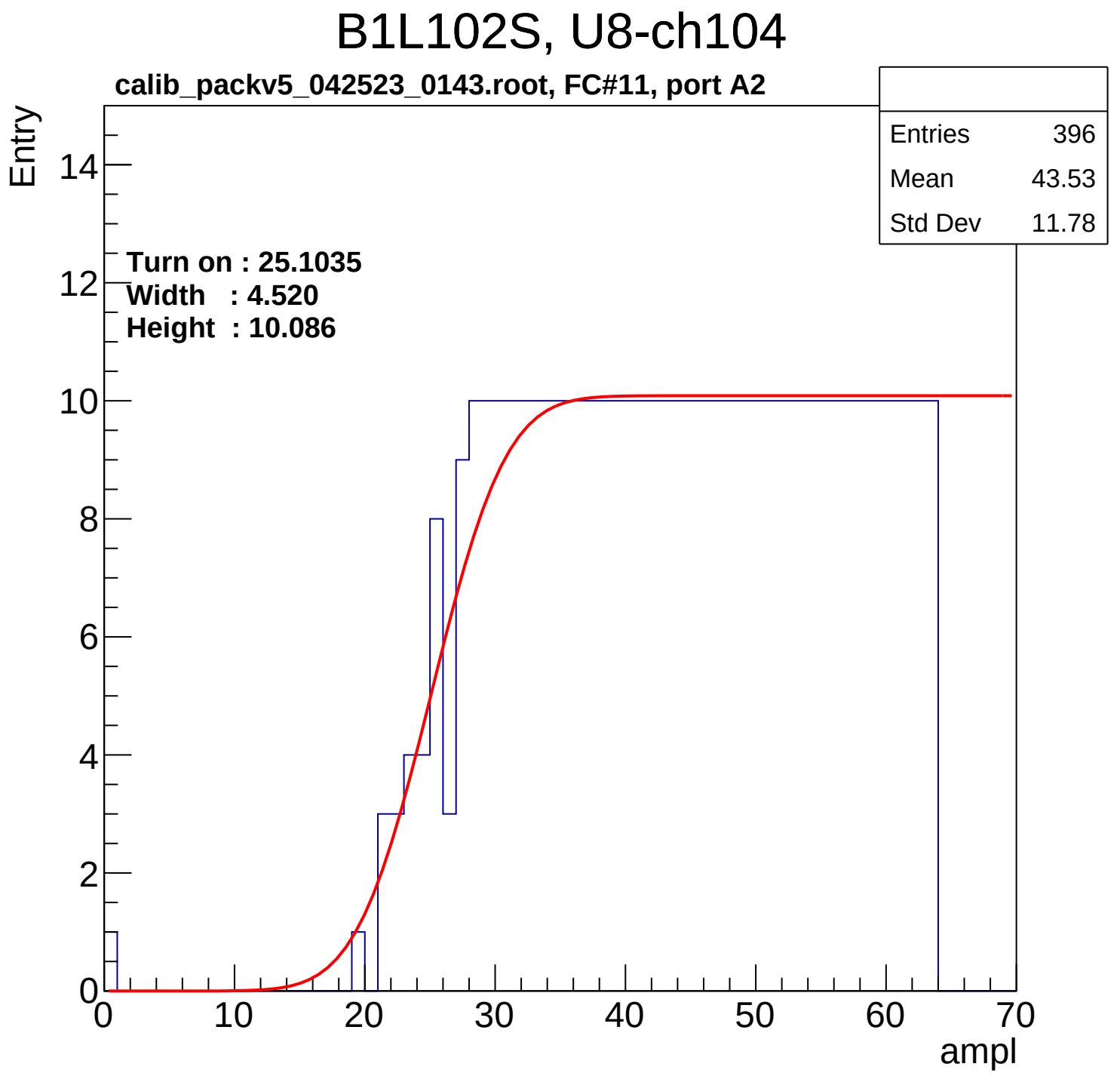
B1L102S, U8-ch104
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.53
Std Dev 11.78
Turn on : 25.1035
Width : 4.520
Height : 10.086
Entry
ampl
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8
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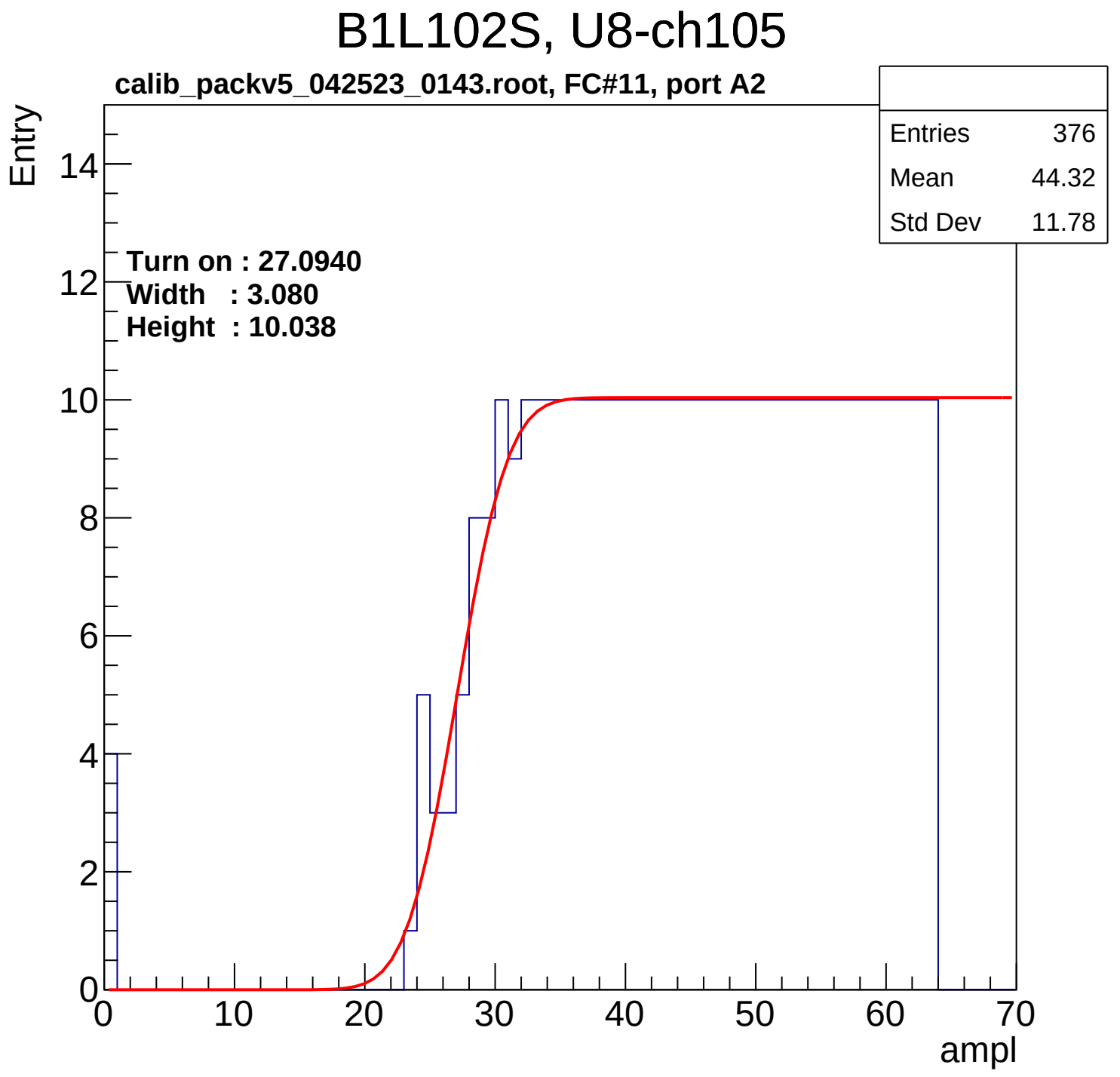
B1L102S, U8-ch105
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.32
Std Dev 11.78
Turn on : 27.0940
Width : 3.080
Height : 10.038
Entry
ampl
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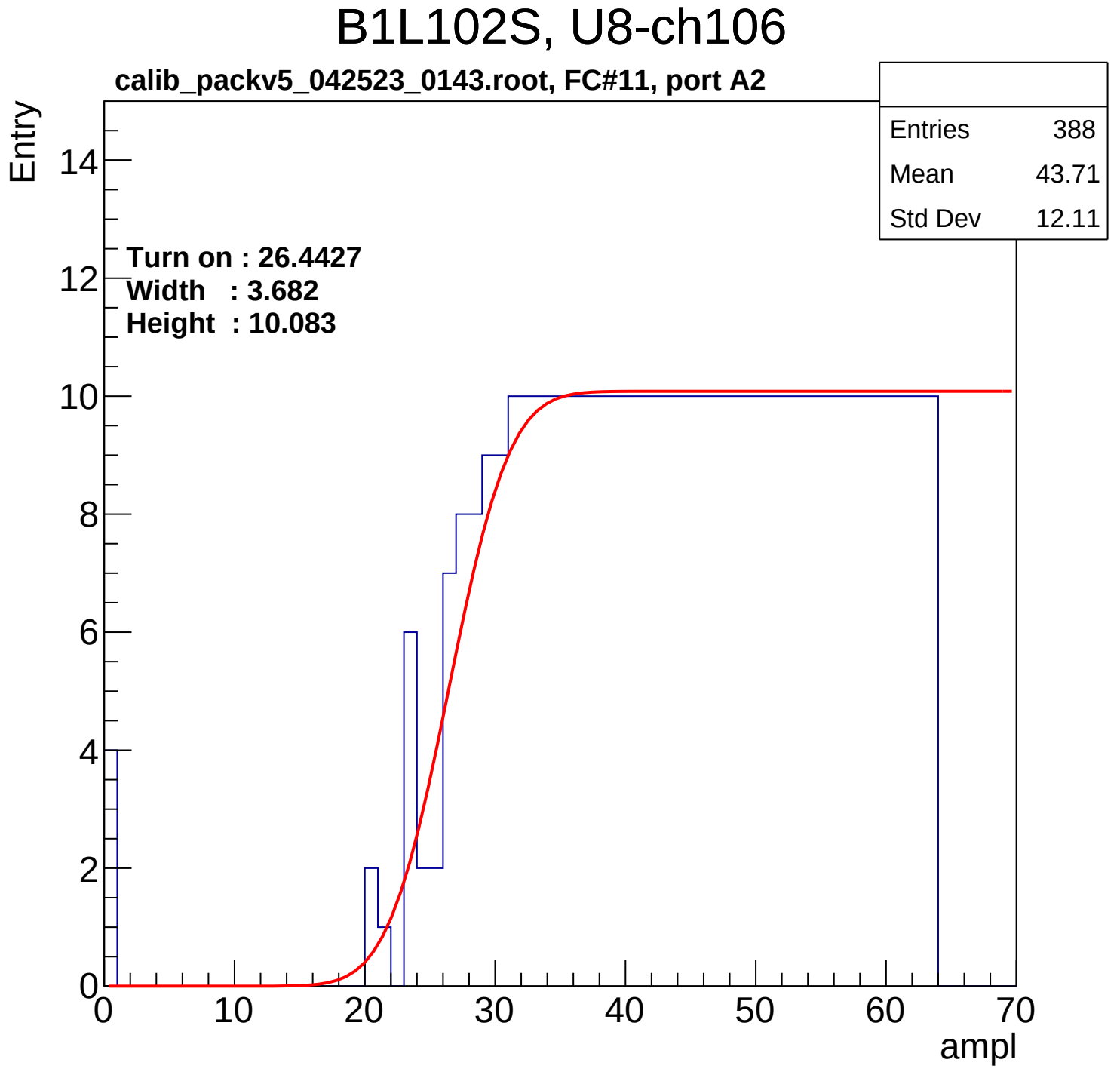
B1L102S, U8-ch106
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.71
Std Dev 12.11
Turn on : 26.4427
Width : 3.682
Height : 10.083
Entry
ampl
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6
8
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0
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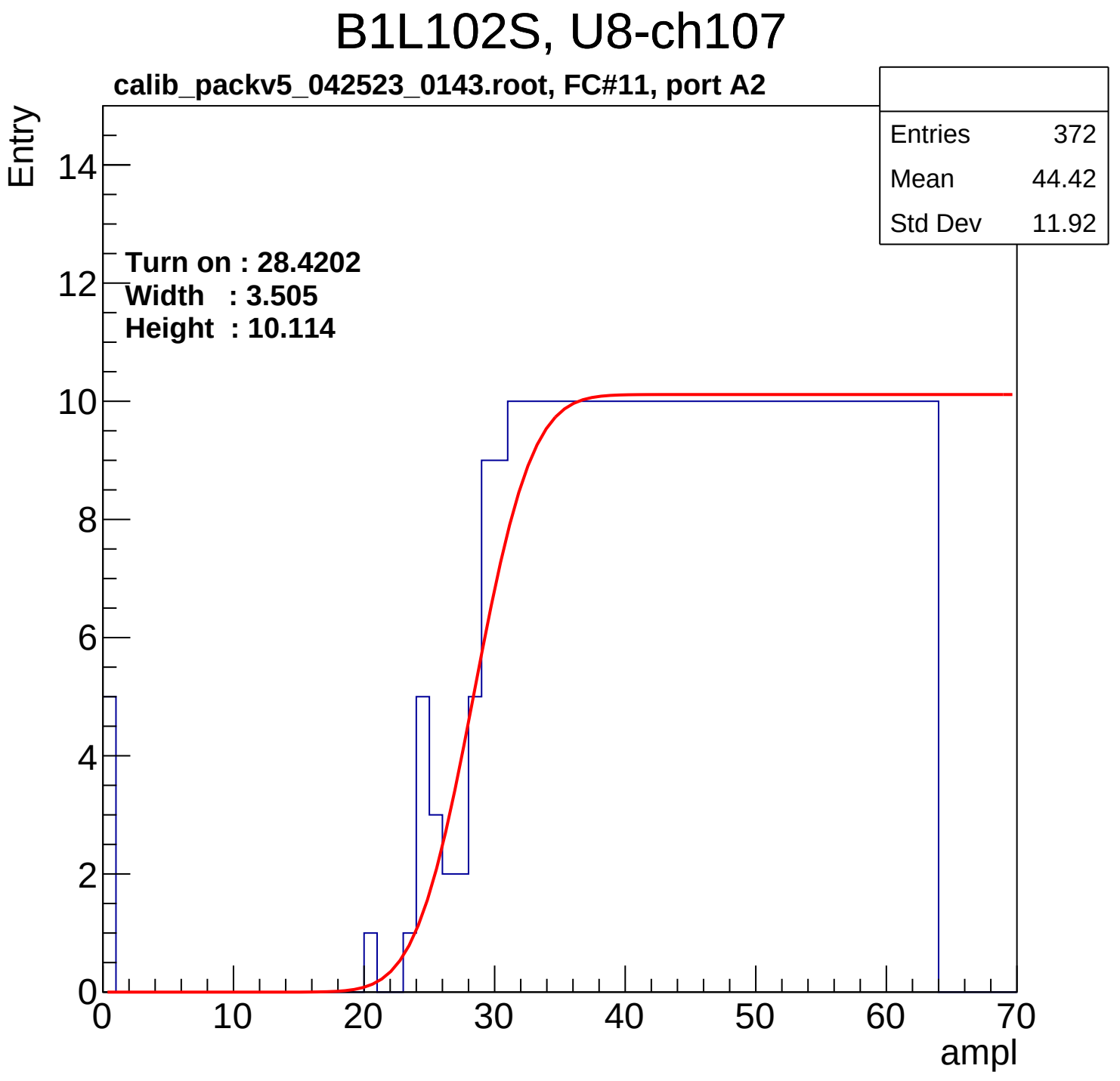
B1L102S, U8-ch107
calib_packv5_042523_0143.root, FC#11, port A2
Entries 372
Mean 44.42
Std Dev 11.92
Turn on : 28.4202
Width : 3.505
Height : 10.114
Entry
ampl
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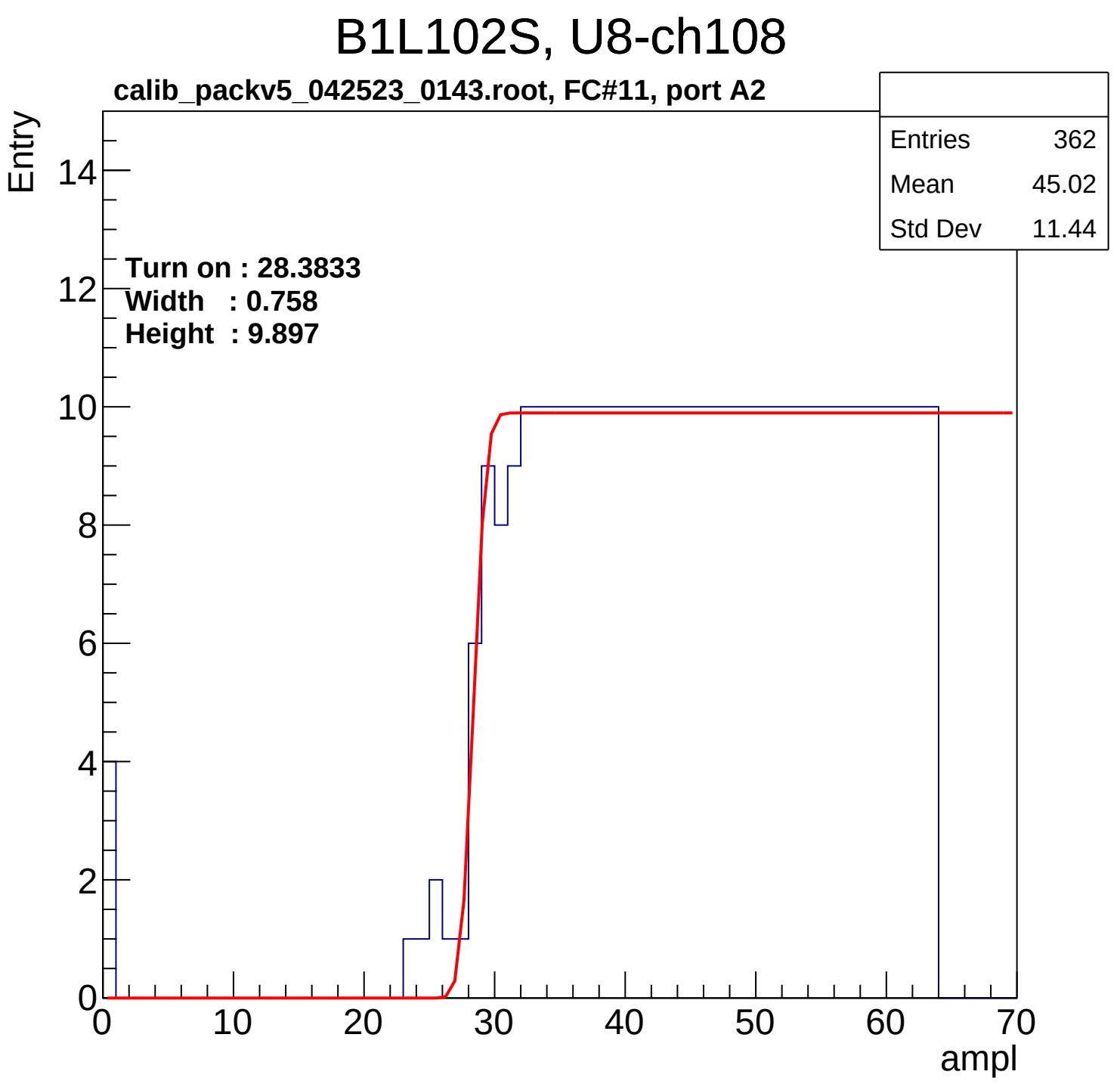
B1L102S, U8-ch108
calib_packv5_042523_0143.root, FC#11, port A2
Entries 362
Mean 45.02
Std Dev 11.44
Turn on : 28.3833
Width : 0.758
Height : 9.897
Entry
ampl
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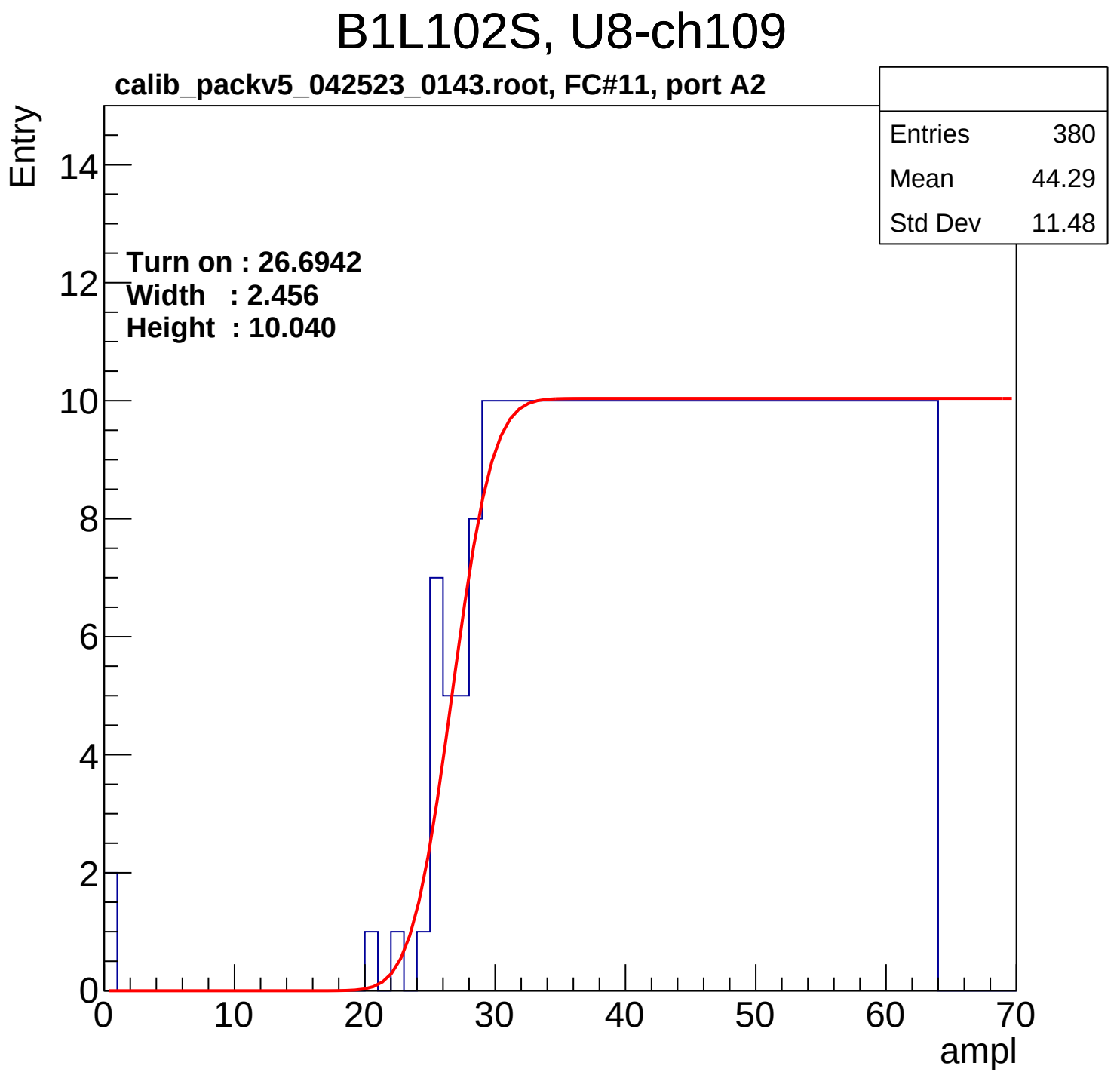
B1L102S, U8-ch109
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.29
Std Dev 11.48
Turn on : 26.6942
Width : 2.456
Height : 10.040
Entry
ampl
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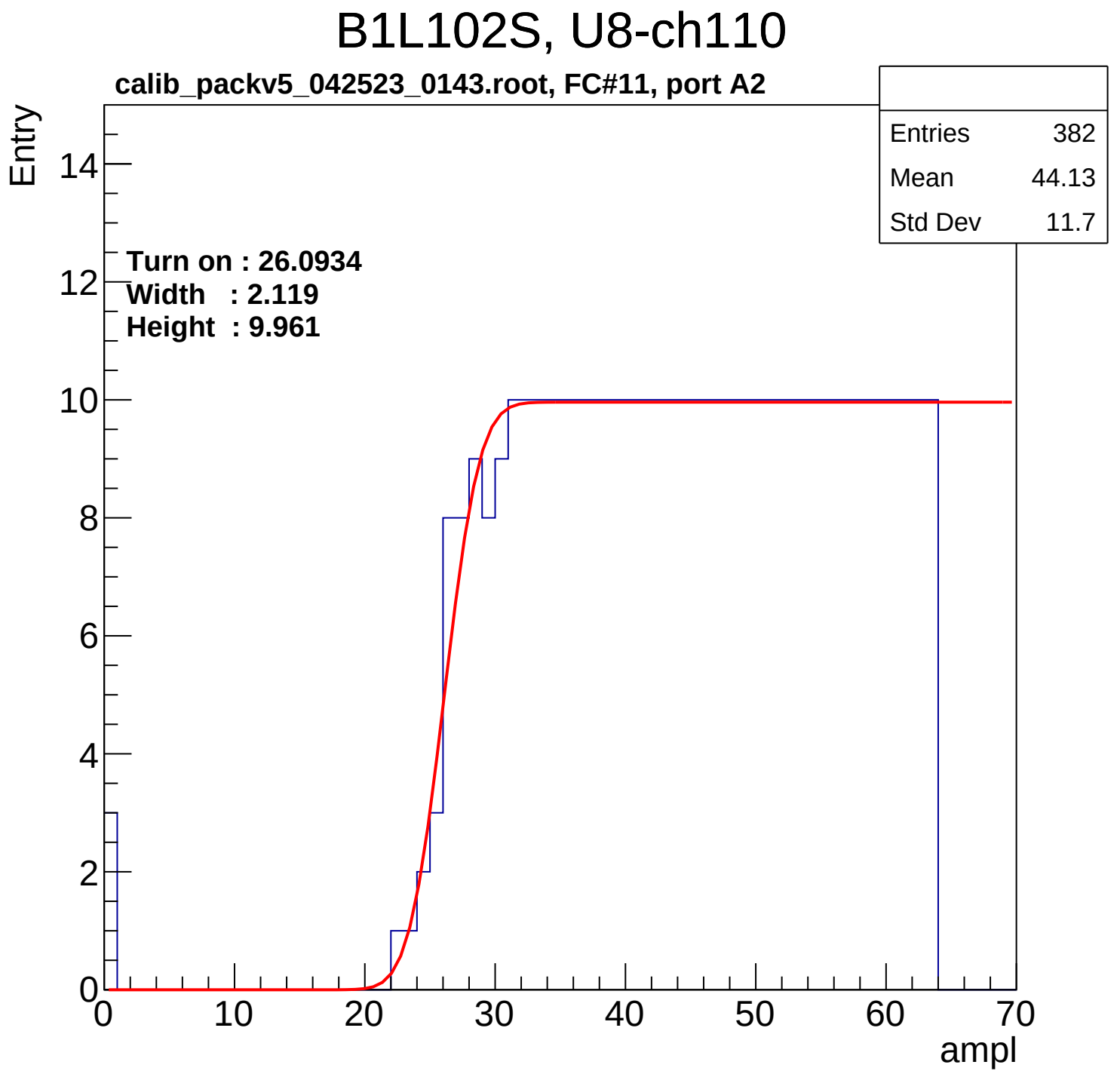
B1L102S, U8-ch110
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.13
Std Dev 11.7
Turn on : 26.0934
Width : 2.119
Height : 9.961
Entry
ampl
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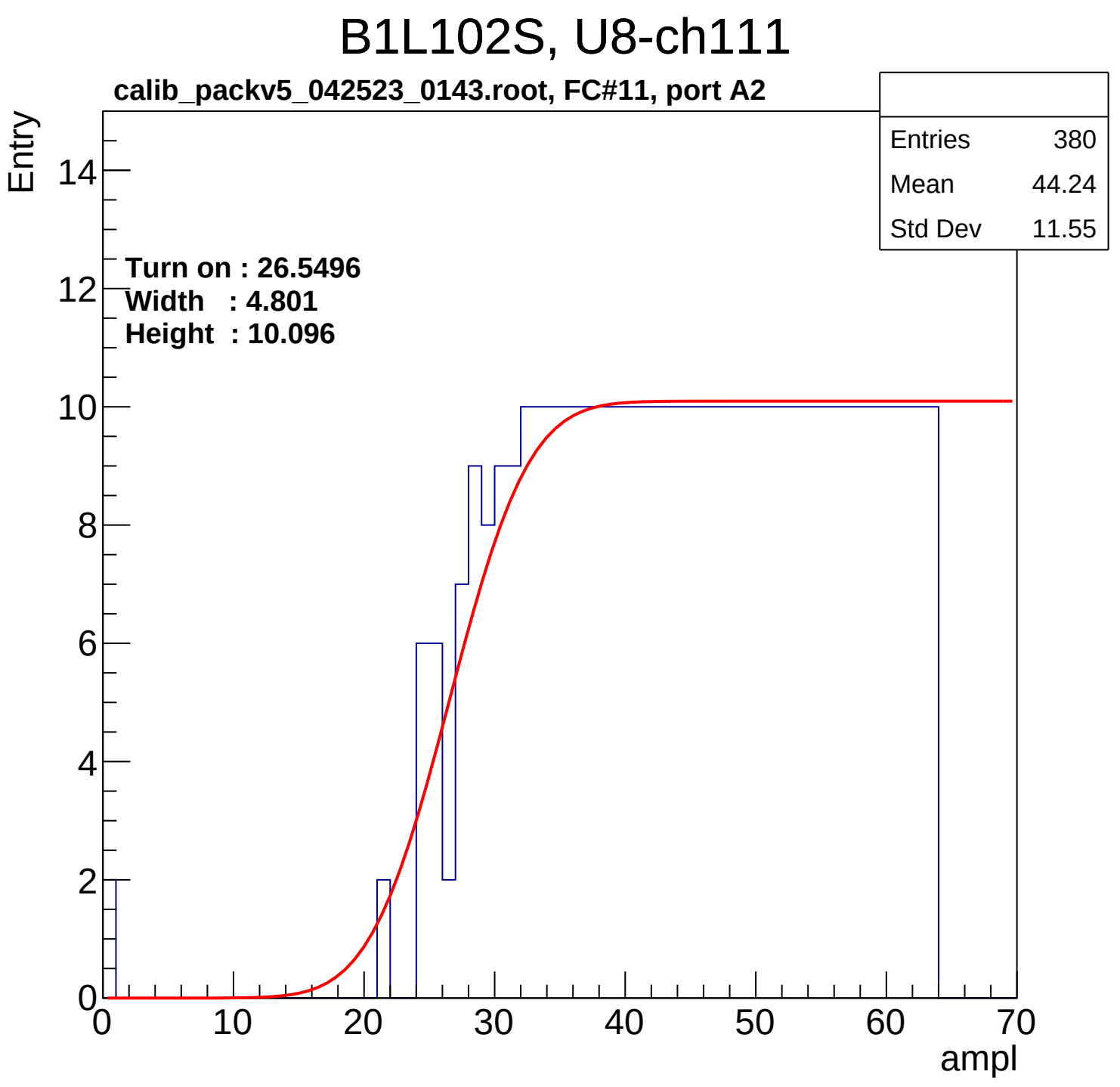
B1L102S, U8-ch111
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.24
Std Dev 11.55
Turn on : 26.5496
Width : 4.801
Height : 10.096
Entry
ampl
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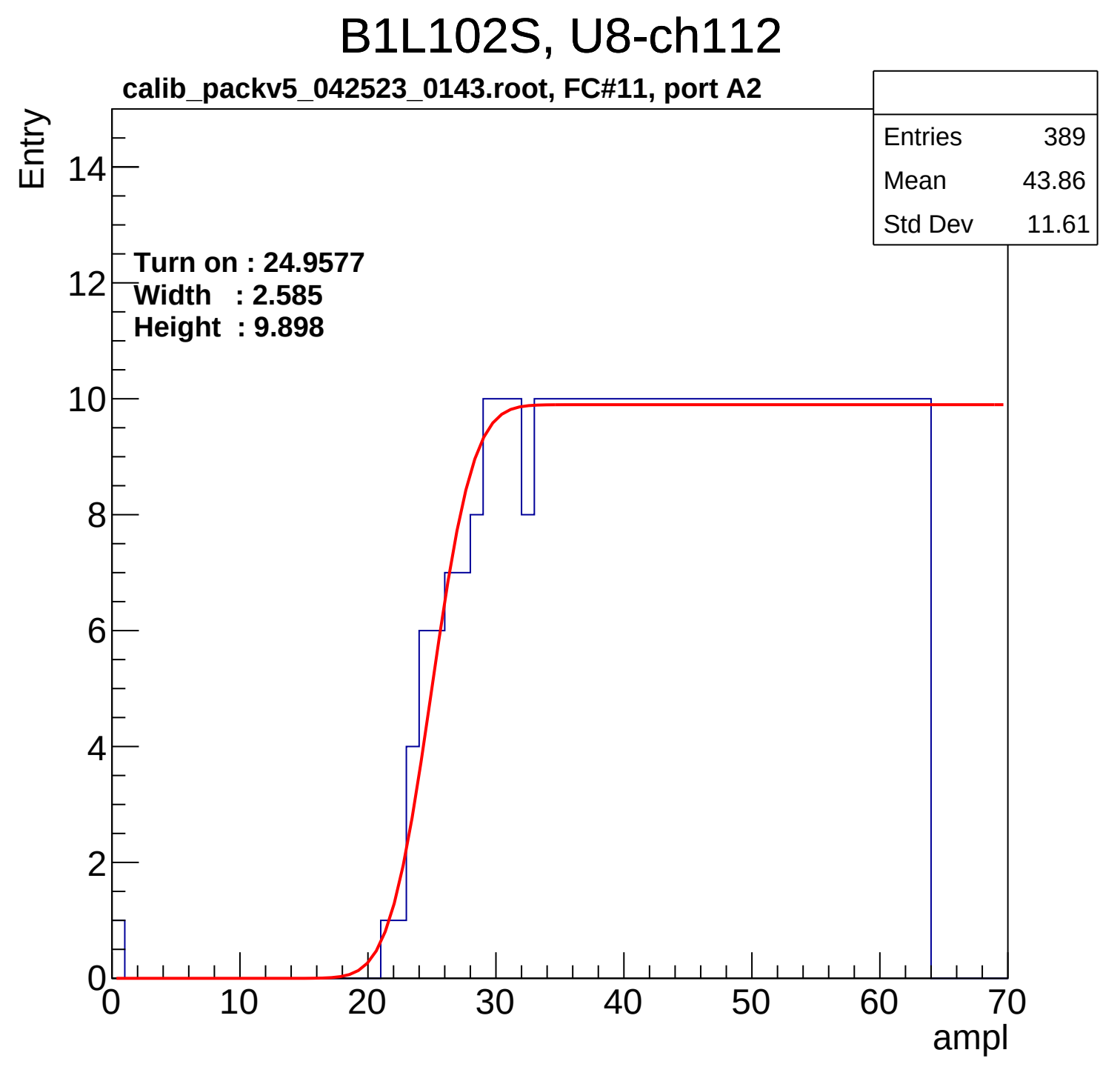
B1L102S, U8-ch112
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.86
Std Dev 11.61
Turn on : 24.9577
Width : 2.585
Height : 9.898
Entry
ampl
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6
8
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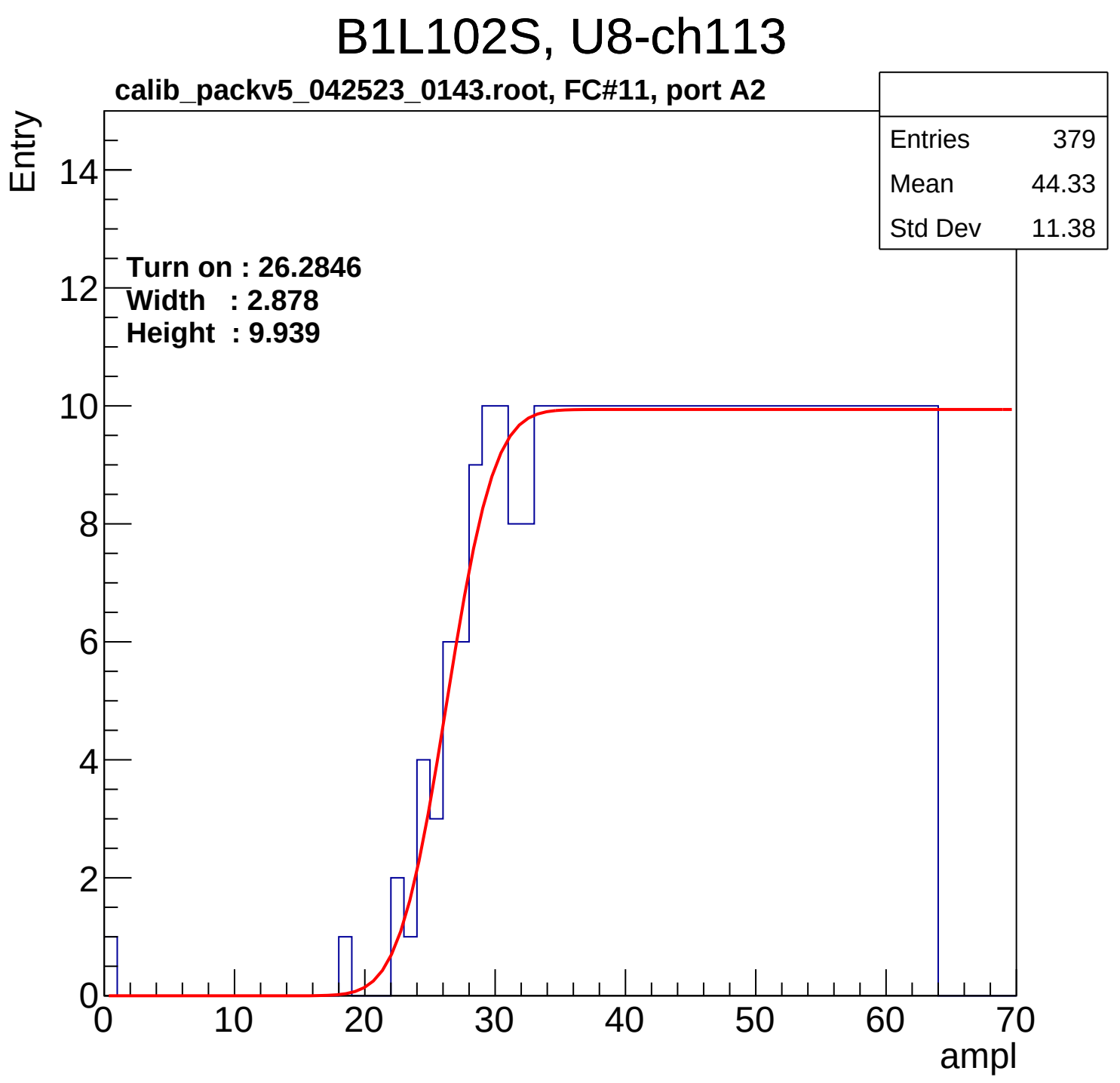
B1L102S, U8-ch113
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.33
Std Dev 11.38
Turn on : 26.2846
Width : 2.878
Height : 9.939
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ampl
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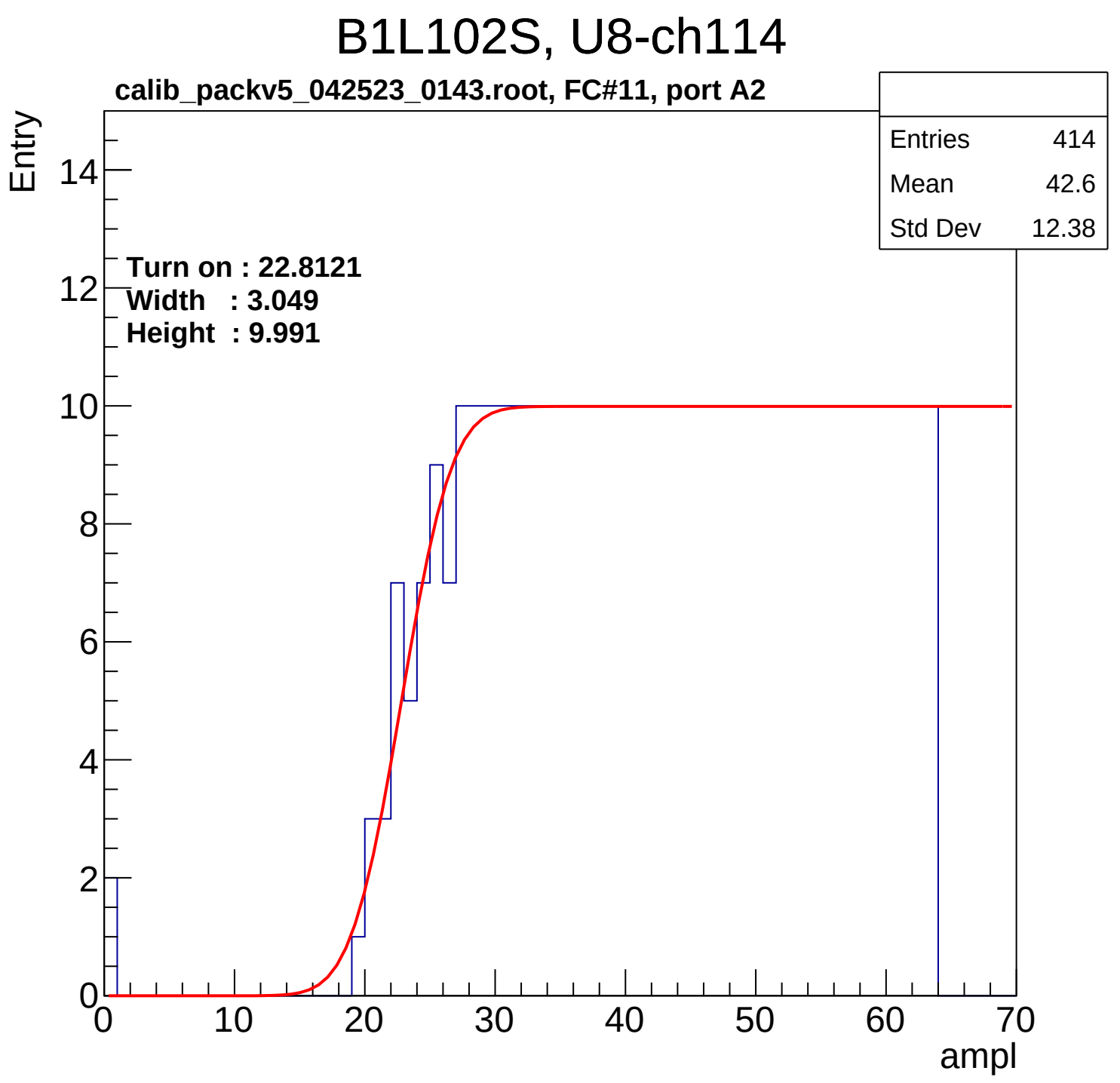
B1L102S, U8-ch114
calib_packv5_042523_0143.root, FC#11, port A2
Entries 414
Mean 42.6
Std Dev 12.38
Turn on : 22.8121
Width : 3.049
Height : 9.991
Entry
ampl
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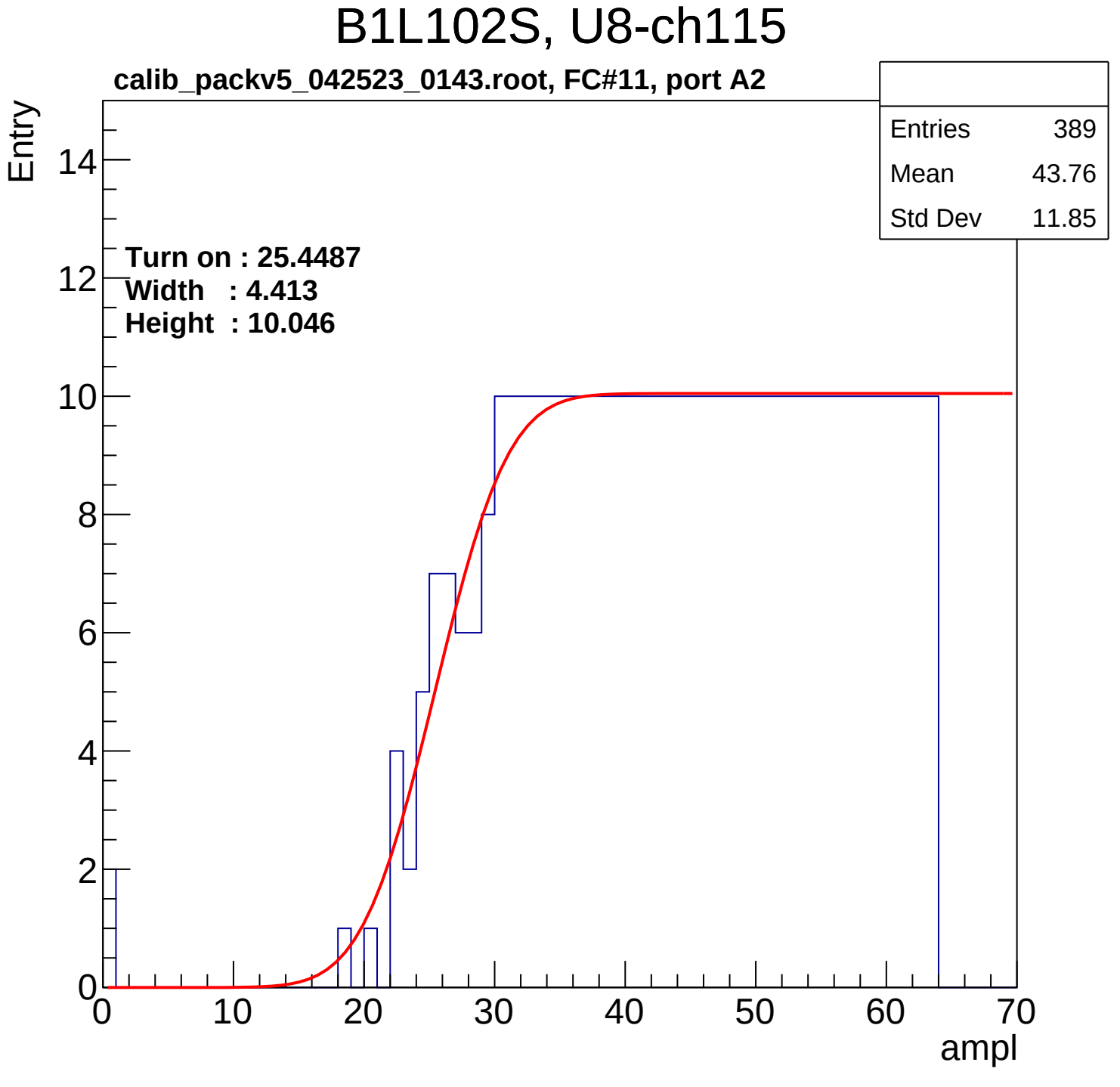
B1L102S, U8-ch115
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.76
Std Dev 11.85
Turn on : 25.4487
Width : 4.413
Height : 10.046
Entry
ampl
0
2
4
6
8
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12
14
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10
20
30
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50
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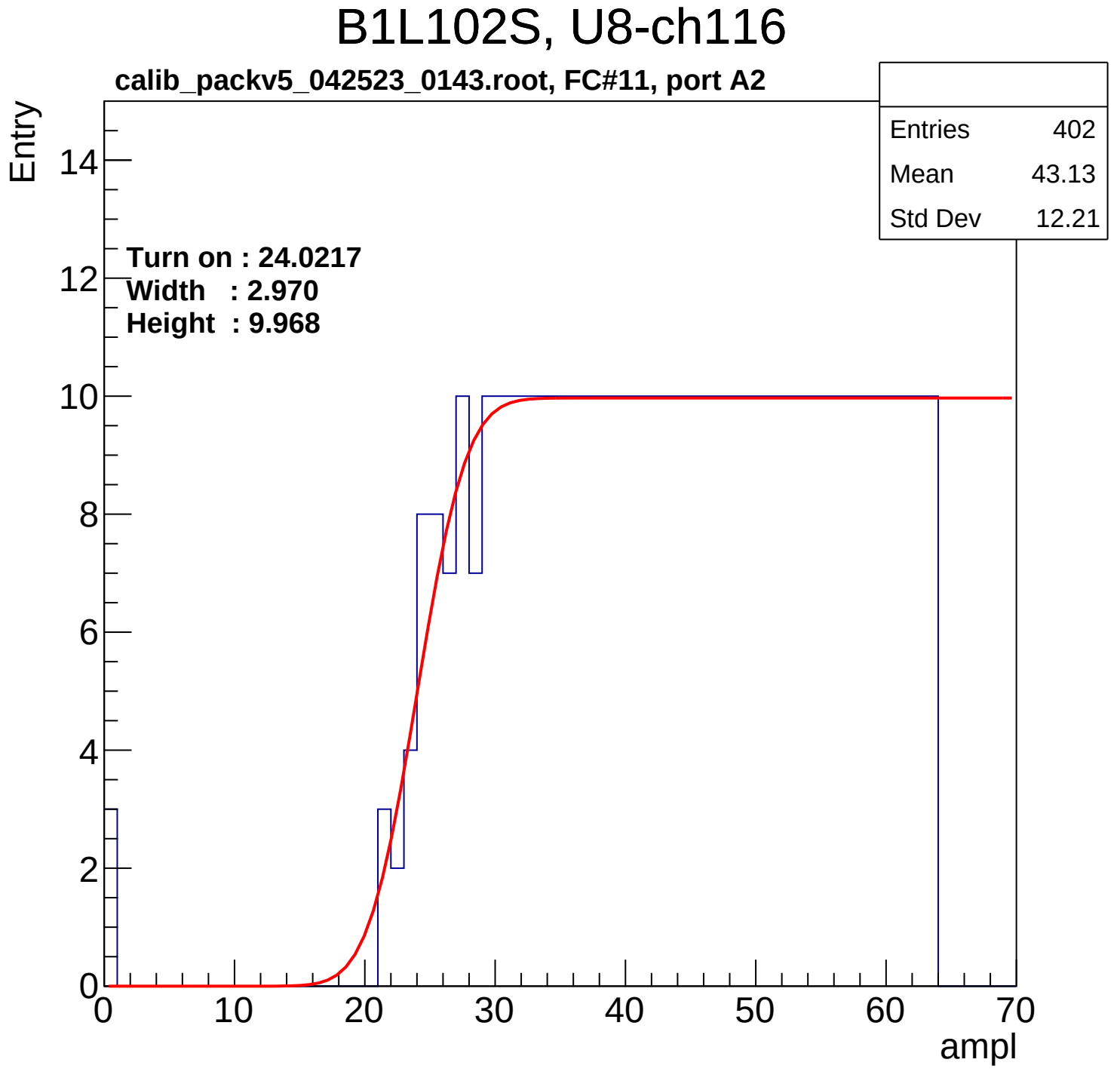
B1L102S, U8-ch116
calib_packv5_042523_0143.root, FC#11, port A2
Entries 402
Mean 43.13
Std Dev 12.21
Turn on : 24.0217
Width : 2.970
Height : 9.968
Entry
ampl
0
2
4
6
8
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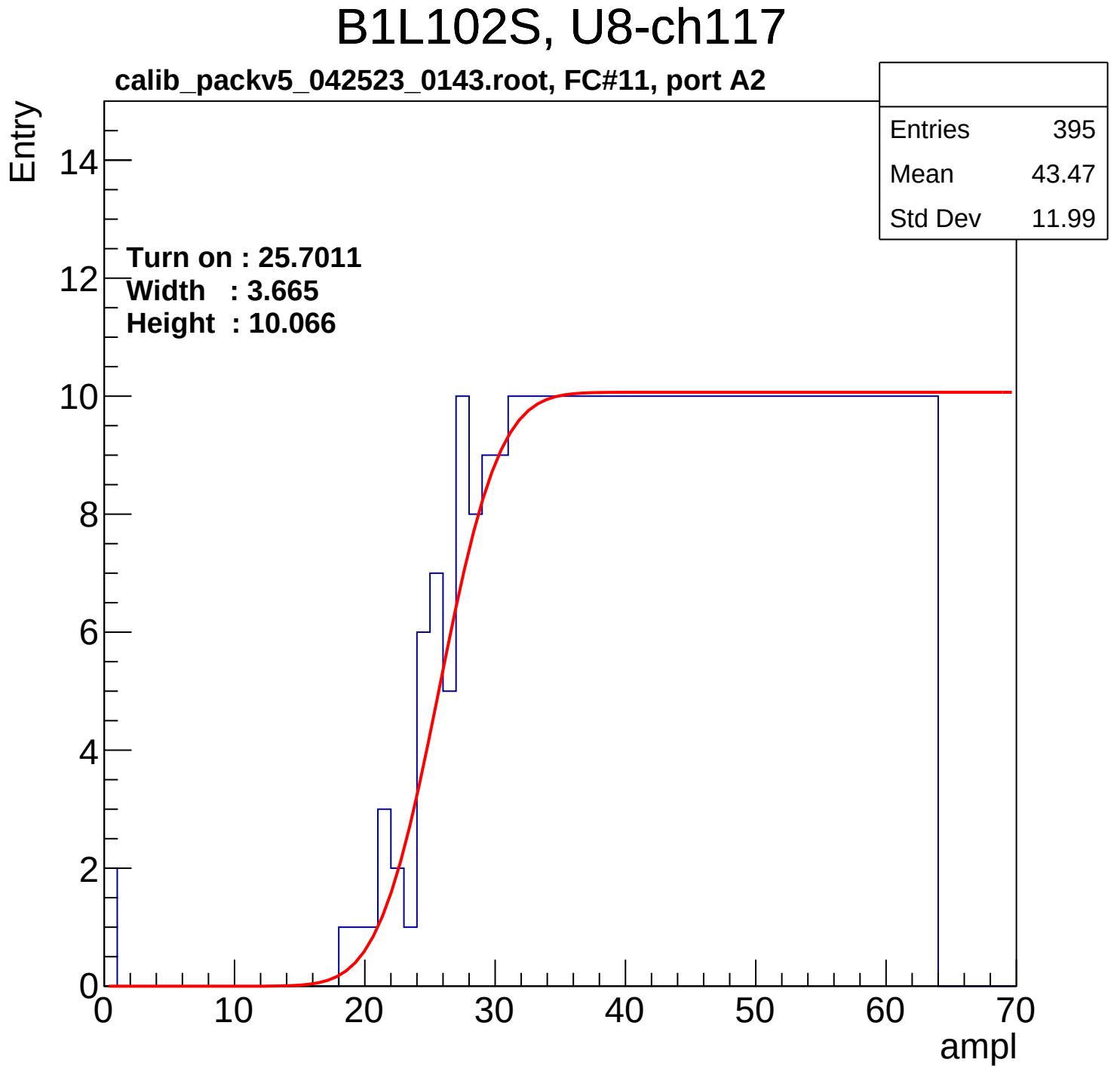
B1L102S, U8-ch117
calib_packv5_042523_0143.root, FC#11, port A2
Entries 395
Mean 43.47
Std Dev 11.99
Turn on : 25.7011
Width : 3.665
Height : 10.066
Entry
ampl
0
2
4
6
8
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12
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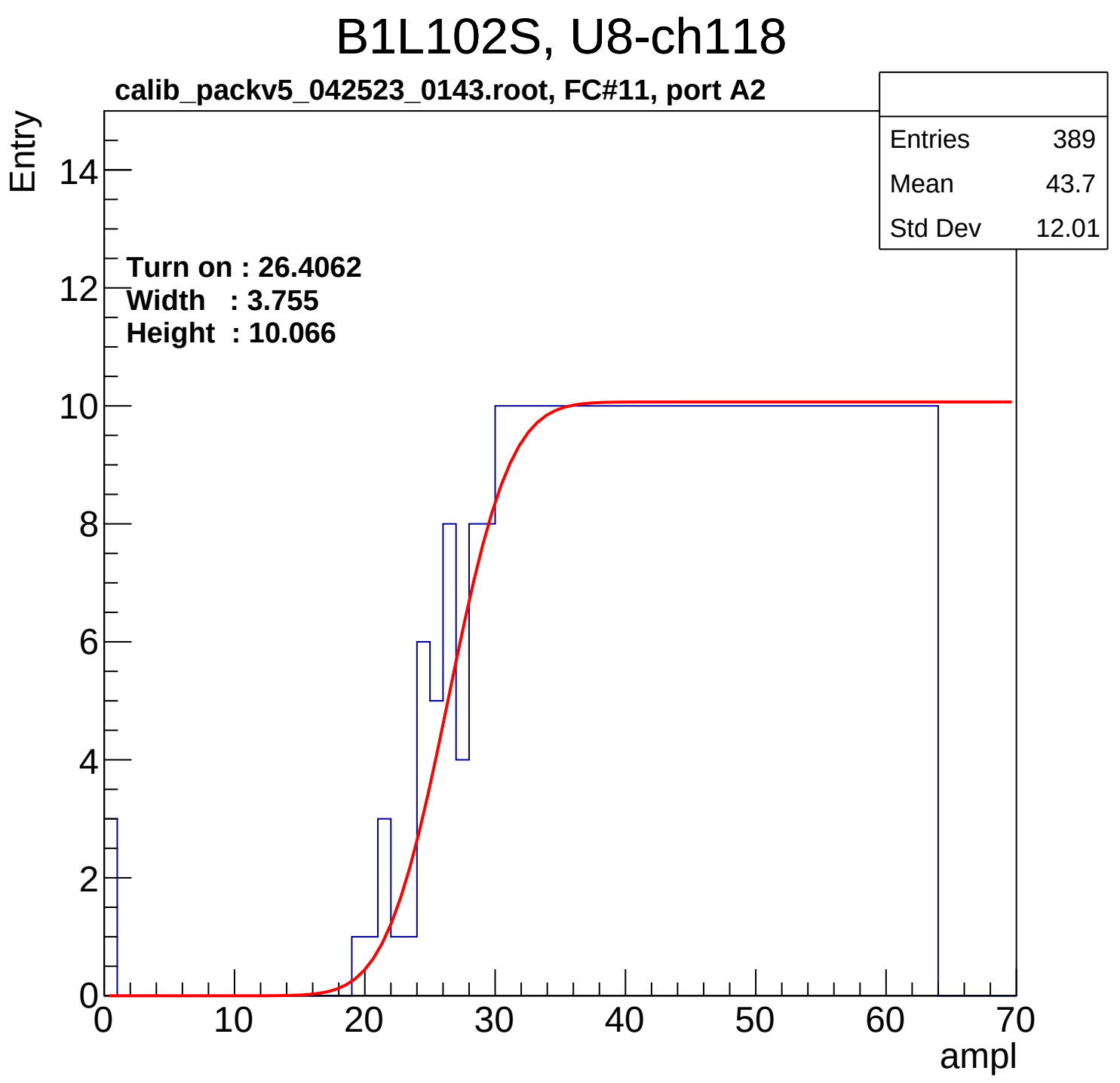
B1L102S, U8-ch118
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.7
Std Dev 12.01
Turn on : 26.4062
Width : 3.755
Height : 10.066
Entry
ampl
0
2
4
6
8
10
12
14
0
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40
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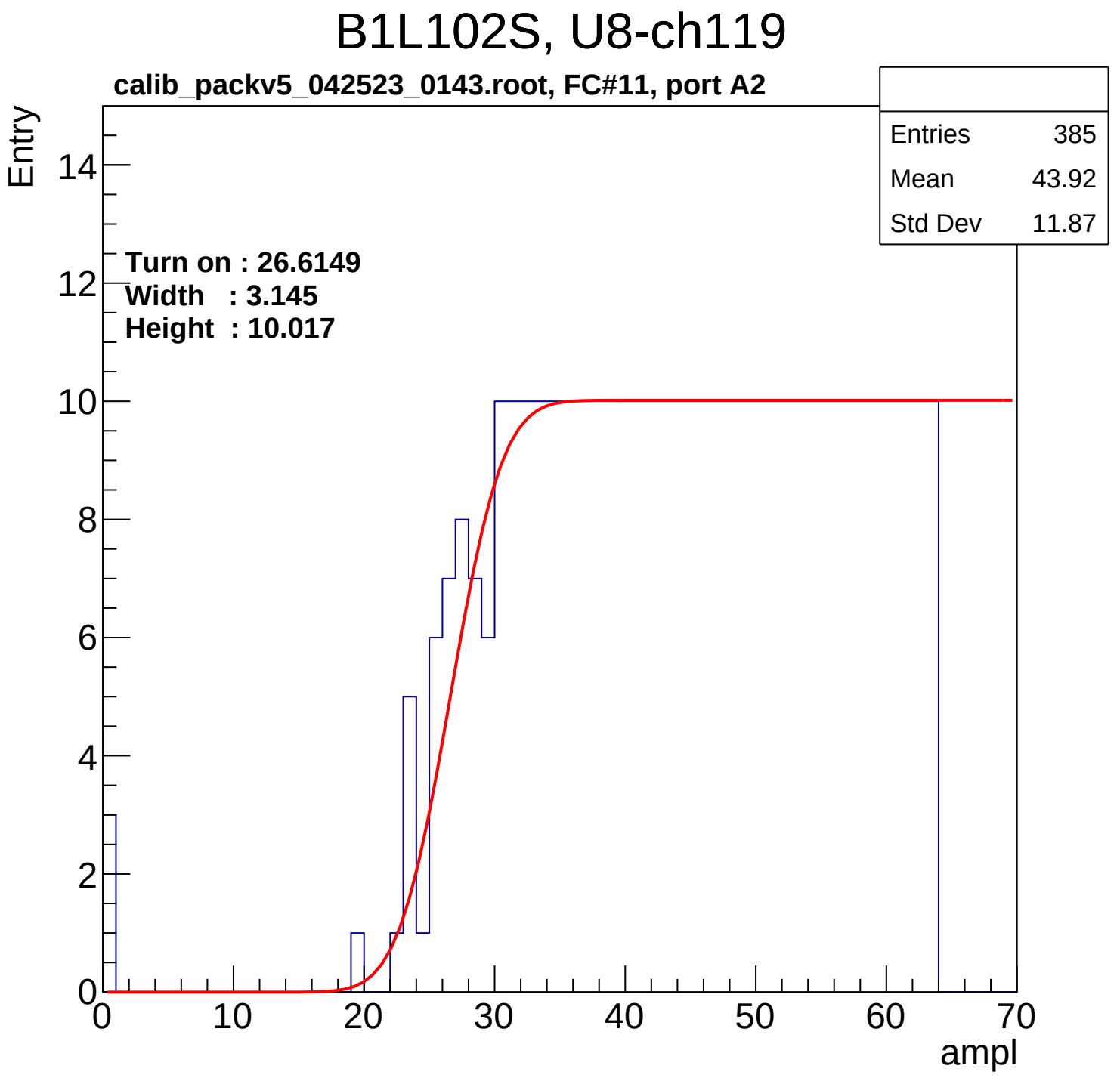
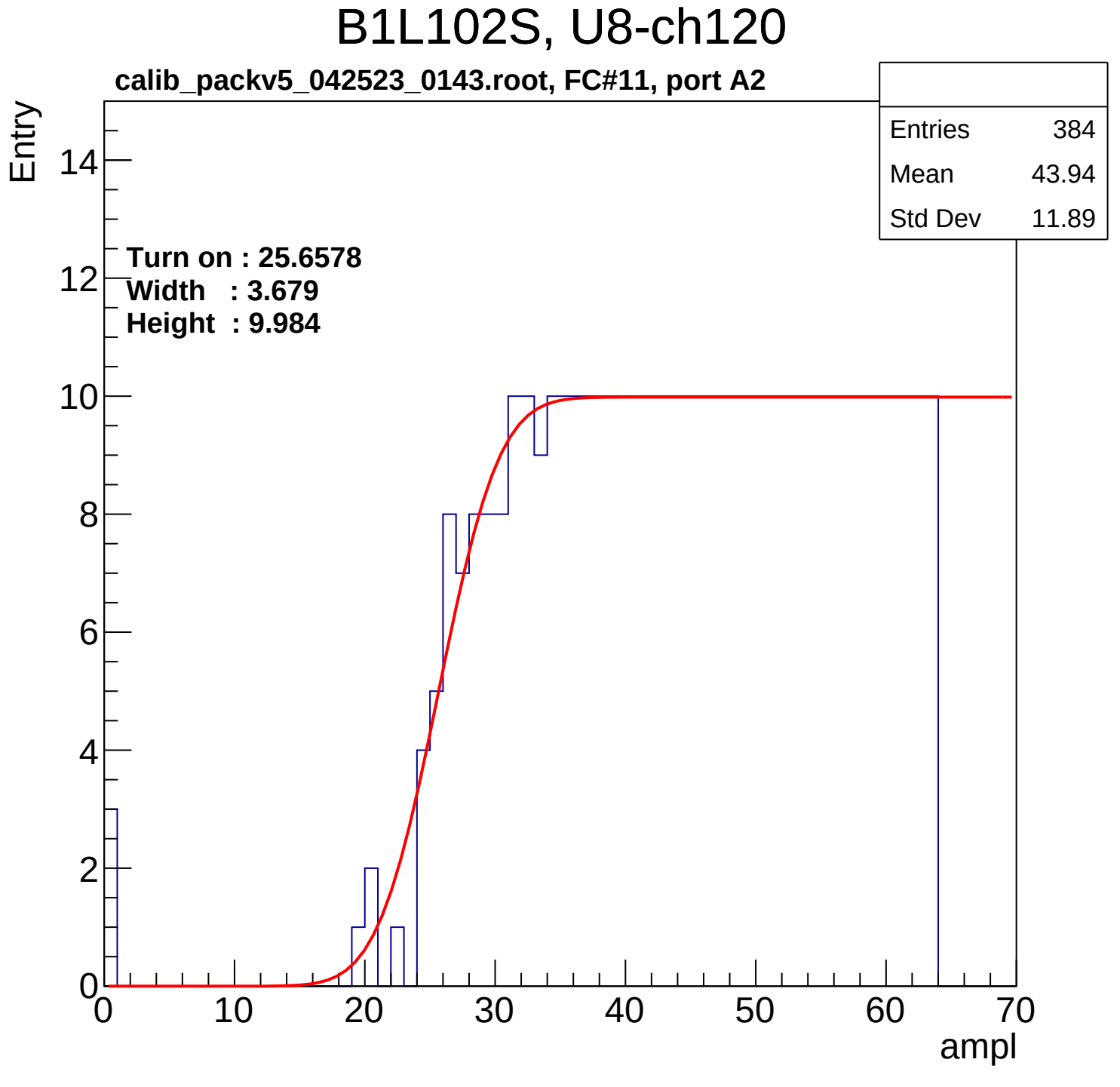

B1L102S, U8-ch119
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.92
Std Dev 11.87
Turn on : 26.6149
Width : 3.145
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U8-ch120
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 43.94
Std Dev 11.89
Turn on : 25.6578
Width : 3.679
Height : 9.984
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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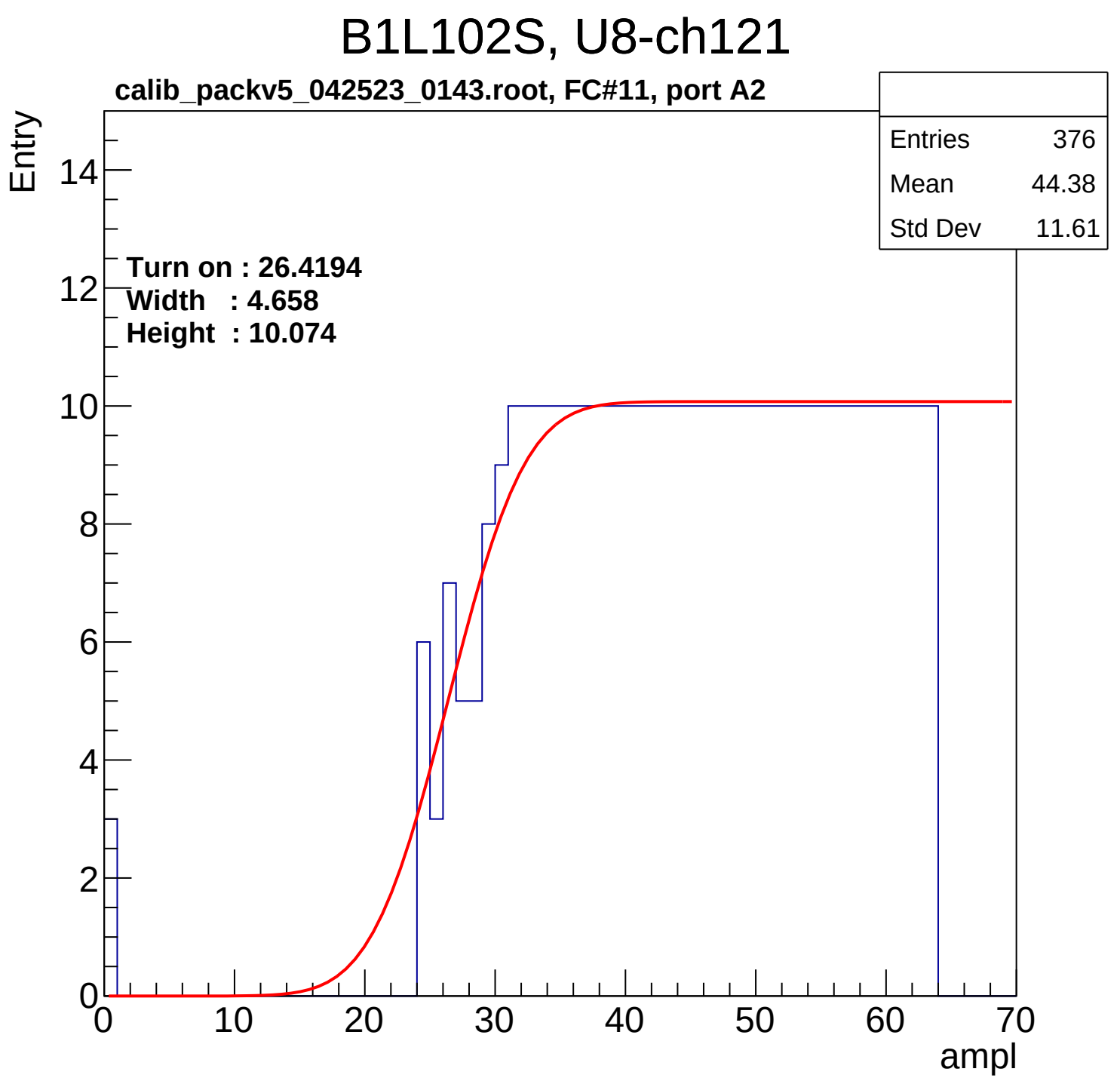
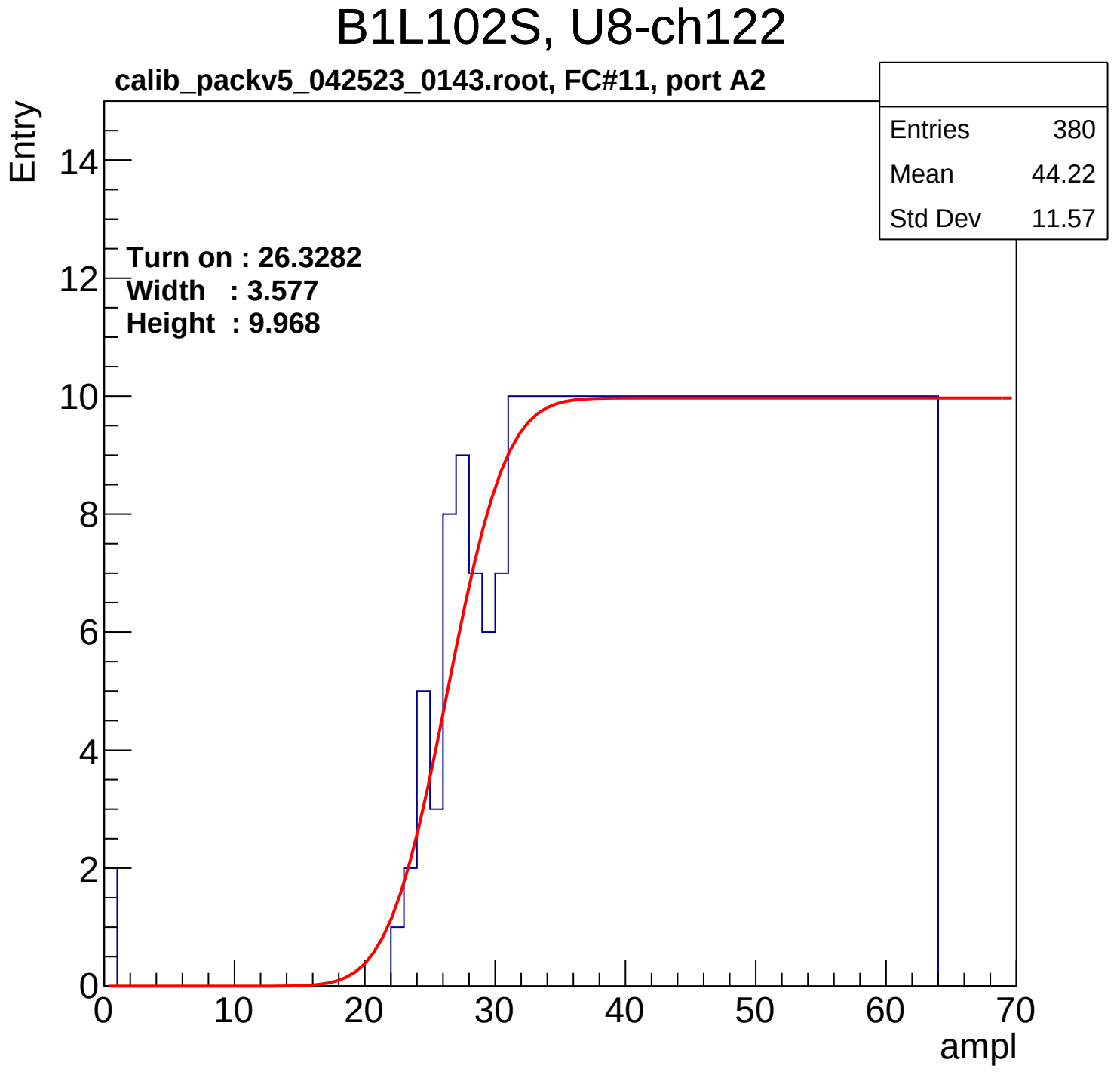

B1L102S, U8-ch121
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.38
Std Dev 11.61
Turn on : 26.4194
Width : 4.658
Height : 10.074
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U8-ch122
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.22
Std Dev 11.57
Turn on : 26.3282
Width : 3.577
Height : 9.968
Entry
ampl
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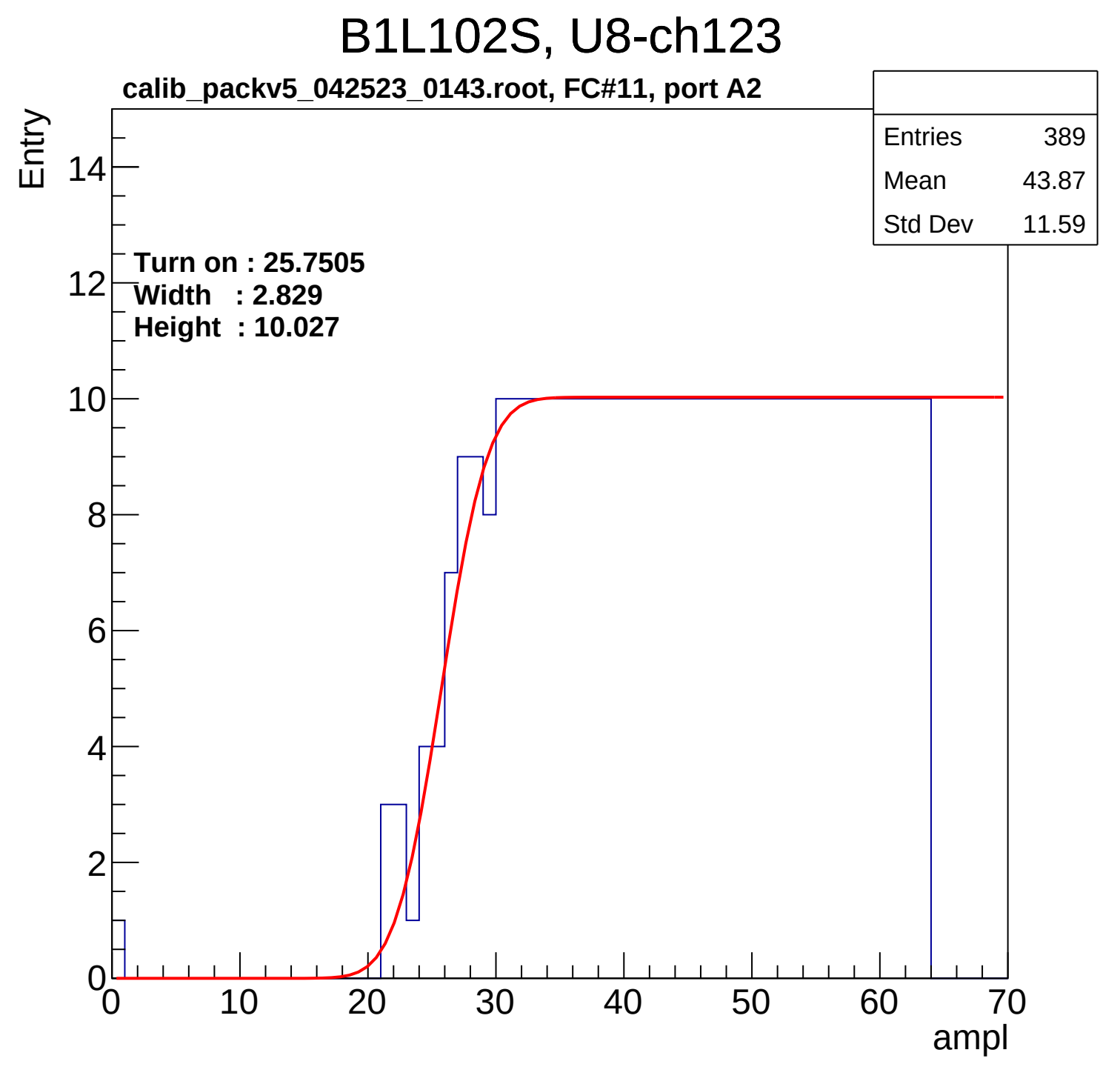
B1L102S, U8-ch123
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.87
Std Dev 11.59
Turn on : 25.7505
Width : 2.829
Height : 10.027
Entry
ampl
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2
4
6
8
10
12
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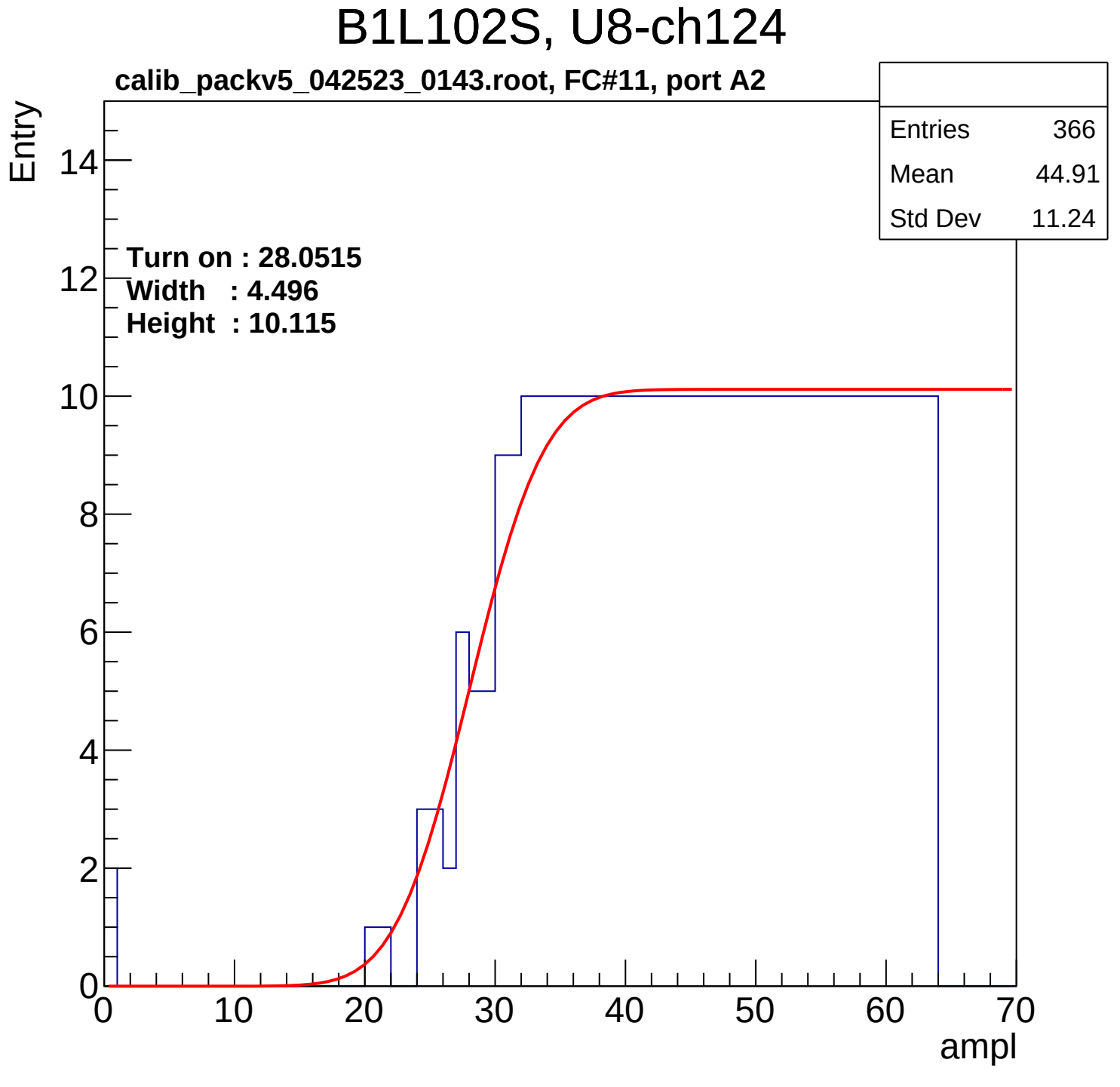
0
10
20
30
40
50
60
70


B1L102S, U8-ch124
calib_packv5_042523_0143.root, FC#11, port A2
Entries 366
Mean 44.91
Std Dev 11.24
Turn on : 28.0515
Width : 4.496
Height : 10.115
Entry
ampl
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6
8
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20
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40
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60
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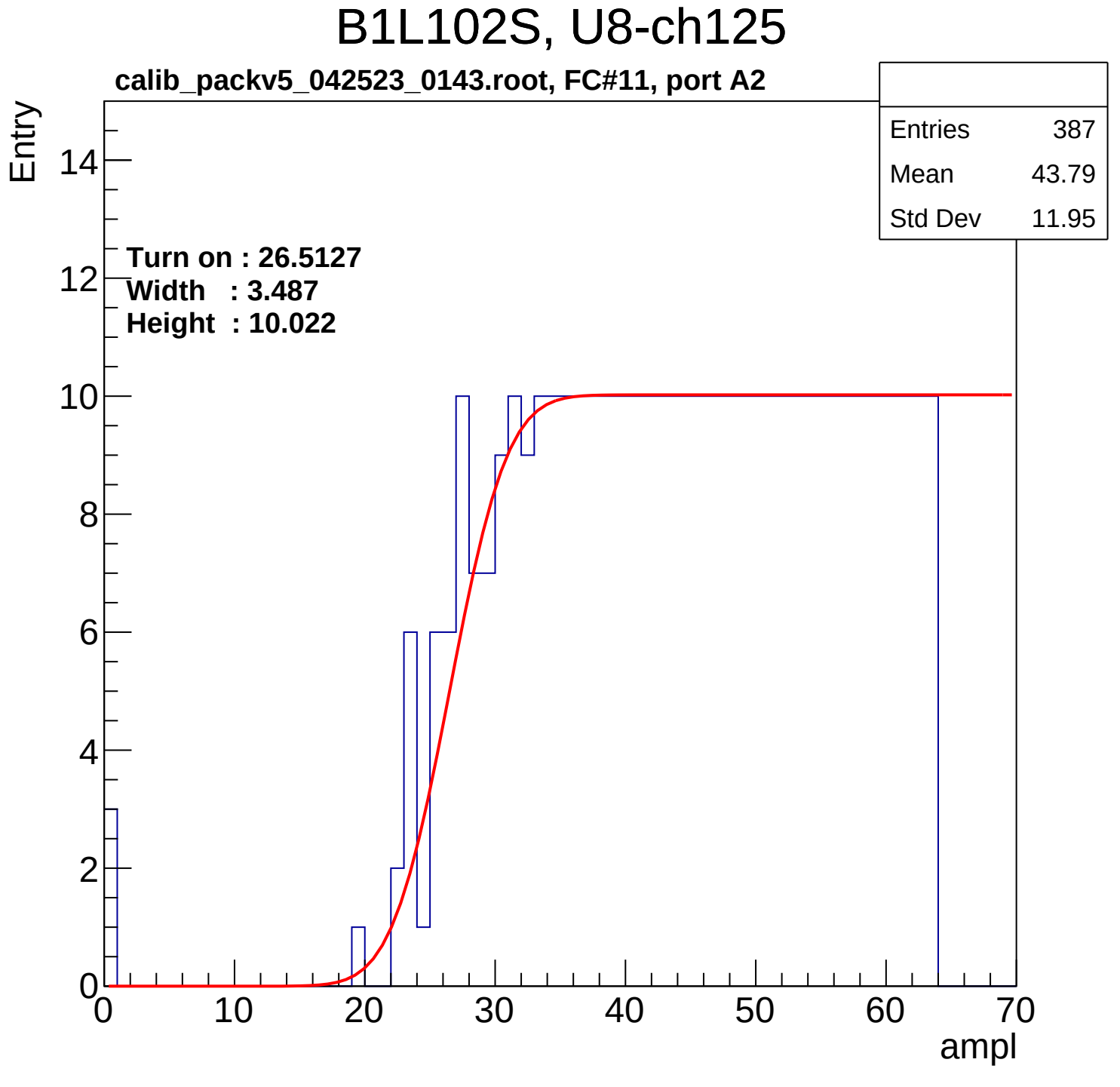
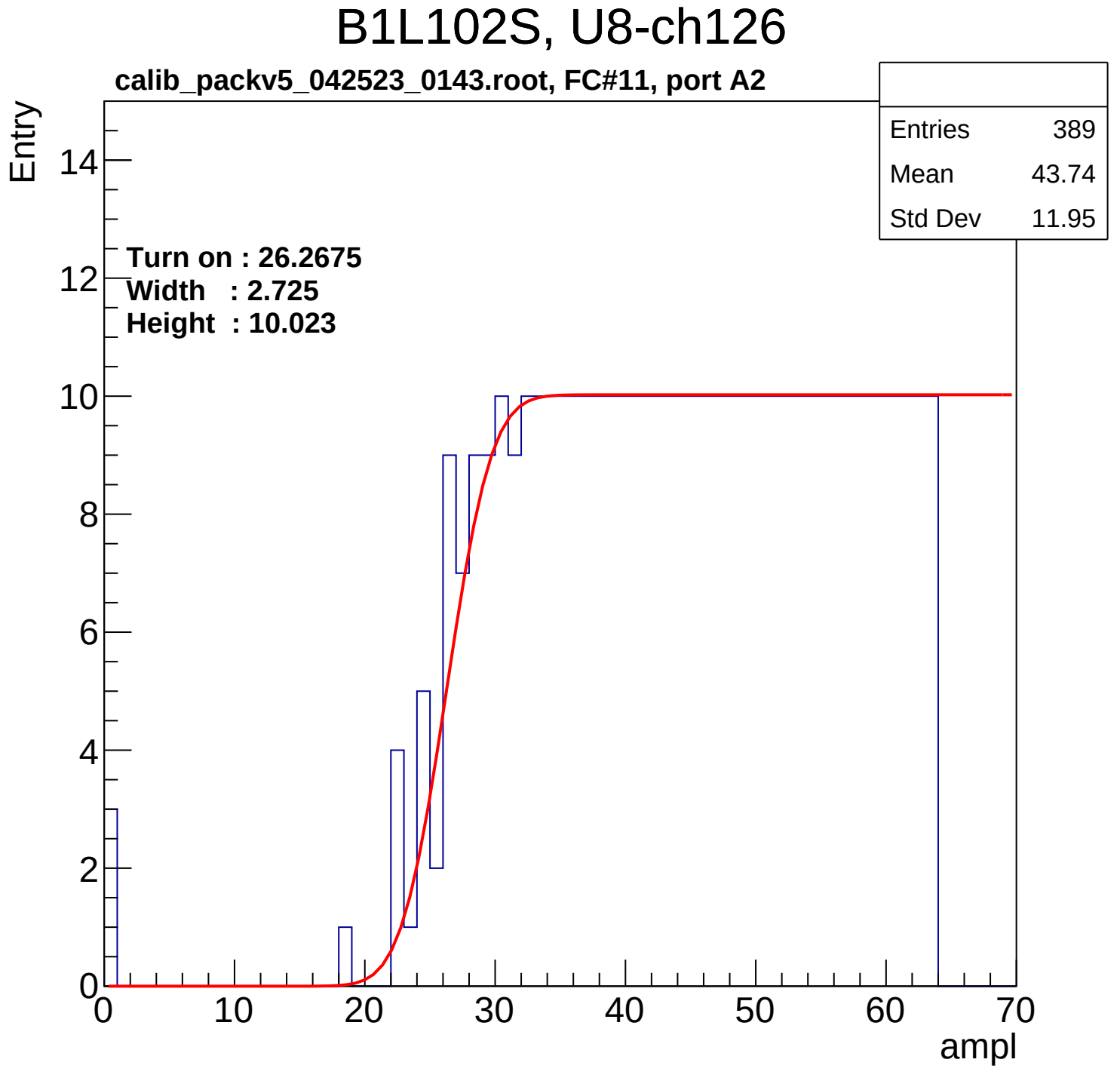

B1L102S, U8-ch125
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.79
Std Dev 11.95
Turn on : 26.5127
Width : 3.487
Height : 10.022
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U8-ch126
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.74
Std Dev 11.95
Turn on : 26.2675
Width : 2.725
Height : 10.023
Entry
ampl
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6
8
10
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0
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60
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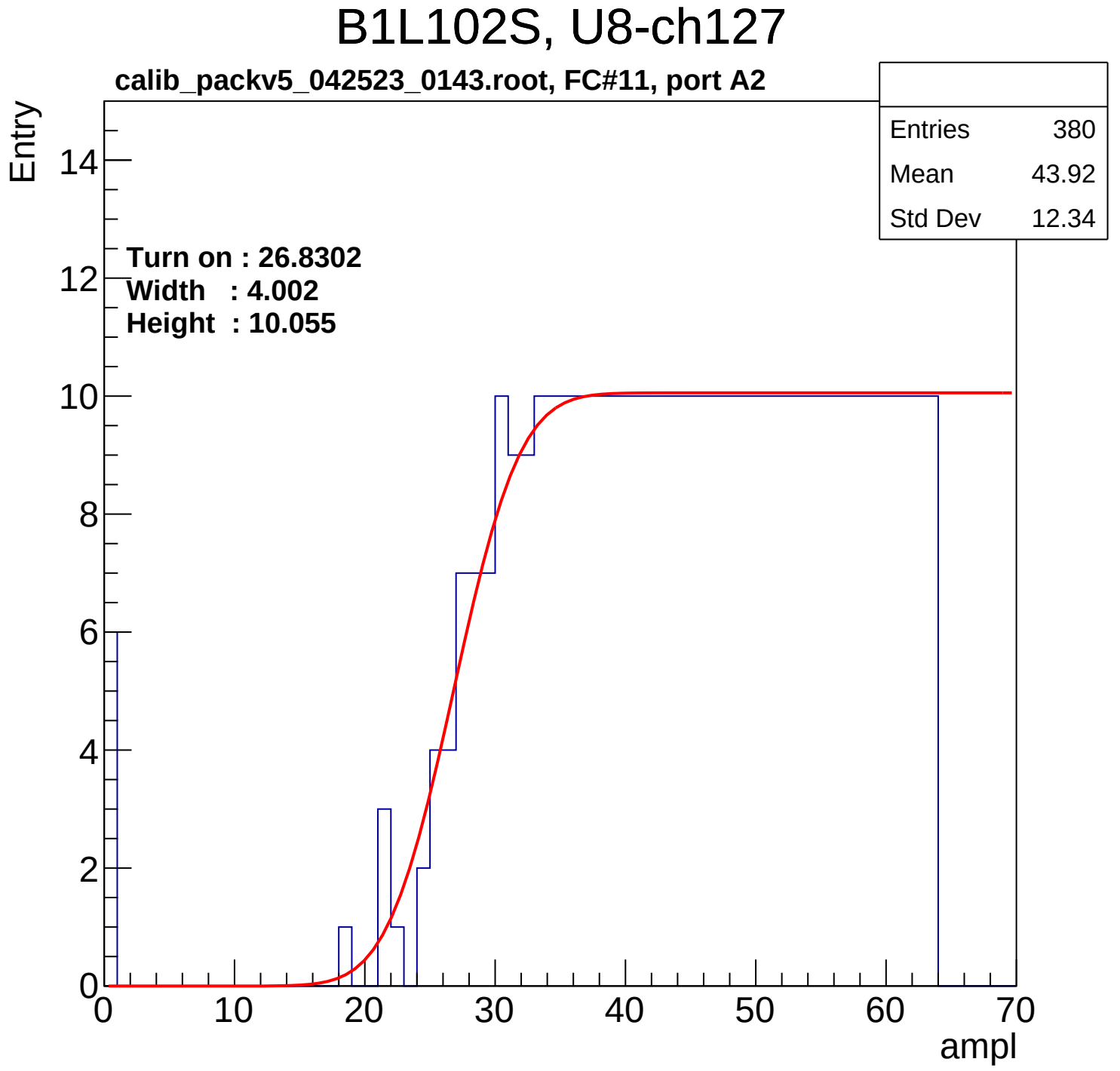
B1L102S, U8-ch127
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 43.92
Std Dev 12.34
Turn on : 26.8302
Width : 4.002
Height : 10.055
Entry
ampl
0
2
4
6
8
10
12
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0
10
20
30
40
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60
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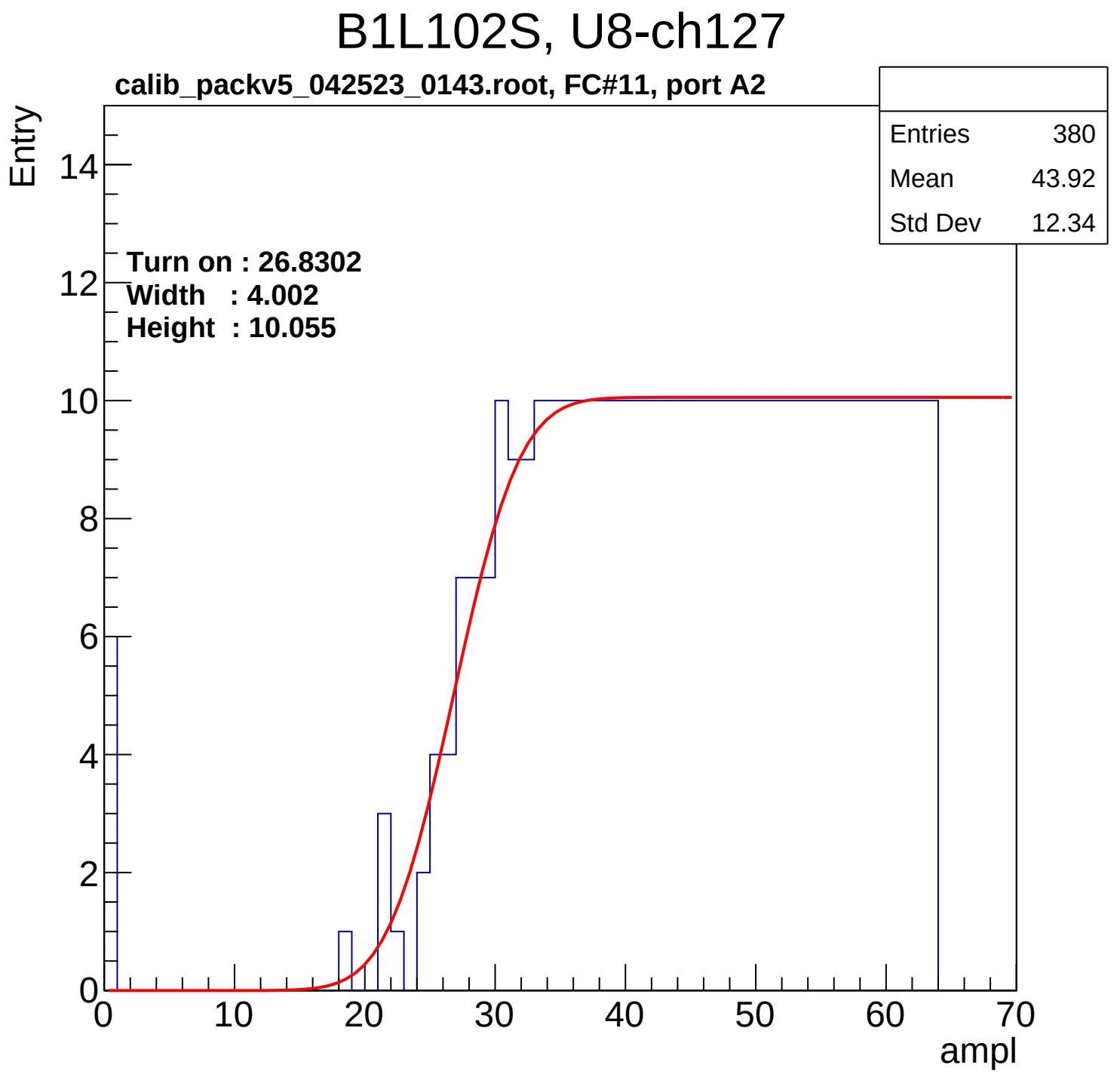
B1L102S, U8-ch127
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 43.92
Std Dev 12.34
Turn on : 26.8302
Width : 4.002
Height : 10.055
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
30
40
50
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70