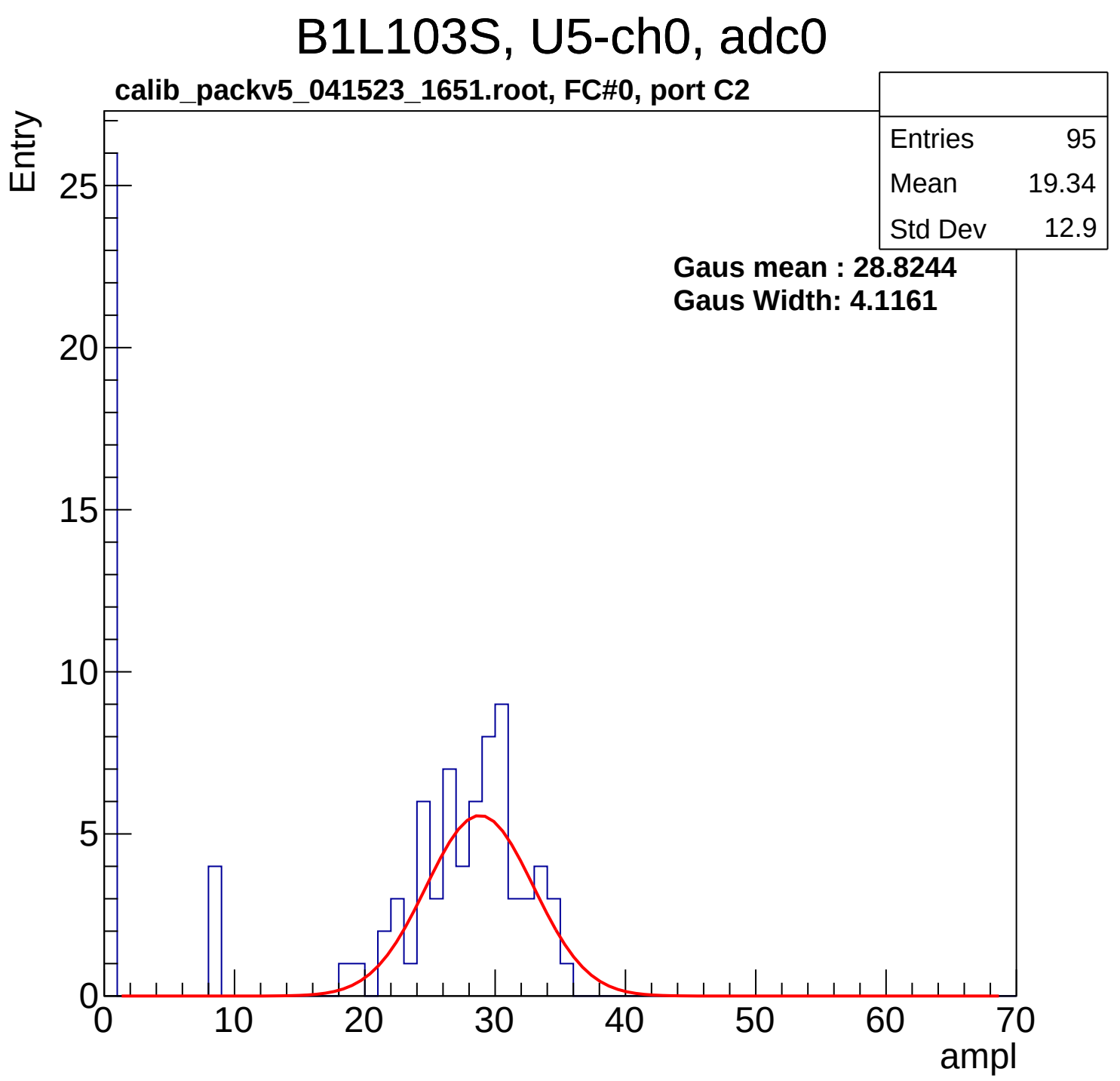
B1L103S, U5-ch0, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 19.34
Std Dev 12.9
Gaus mean : 28.8244
Gaus Width: 4.1161
Entry
ampl
0
5
10
15
20
25
0
10
20
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40
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60
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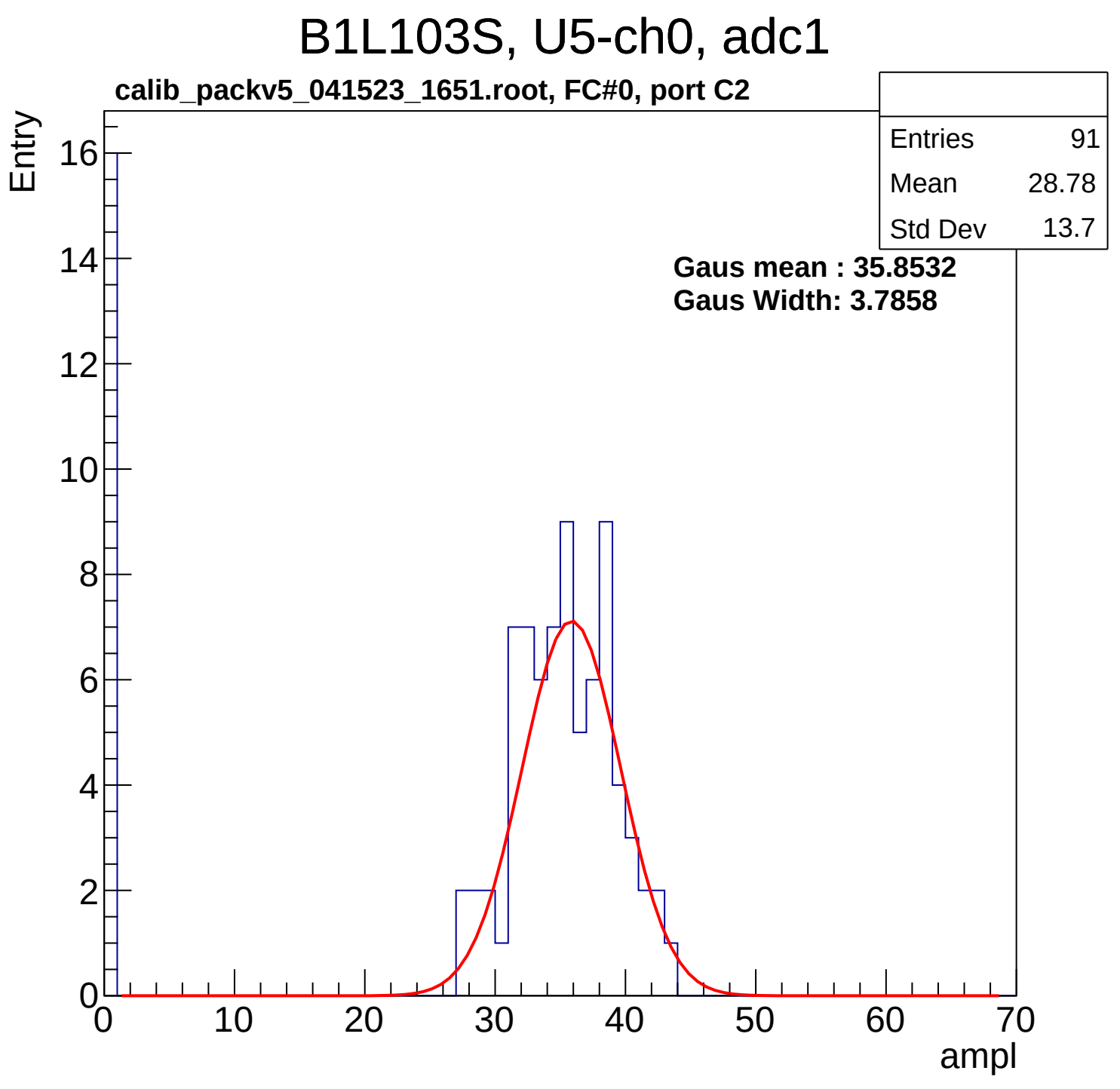
B1L103S, U5-ch0, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 28.78
Std Dev 13.7
Gaus mean : 35.8532
Gaus Width: 3.7858
Entry
ampl
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4
6
8
10
12
14
16
0
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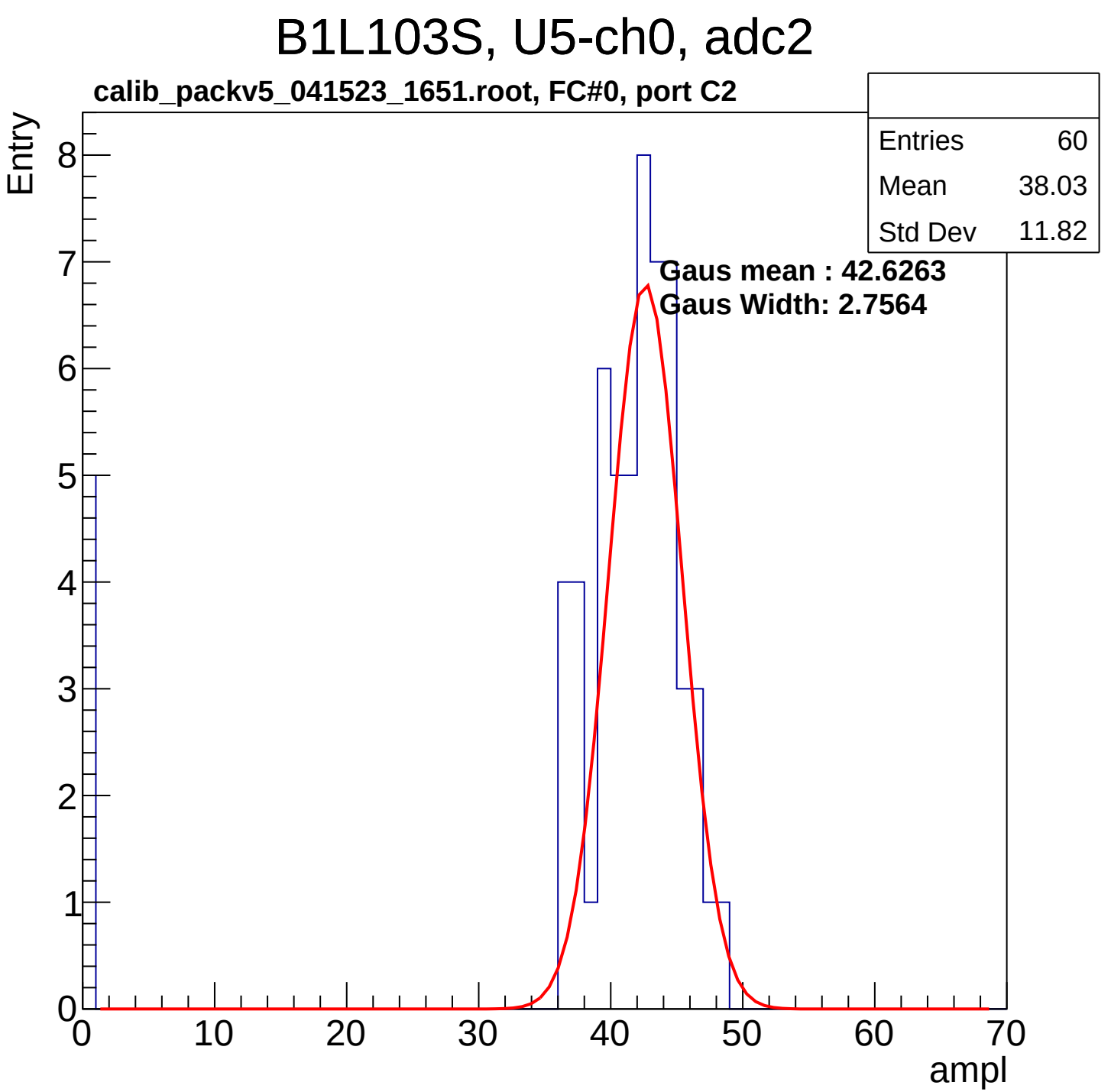
B1L103S, U5-ch0, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 38.03
Std Dev 11.82
Gaus mean : 42.6263
Gaus Width: 2.7564
Entry
ampl
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1
2
3
4
5
6
7
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0
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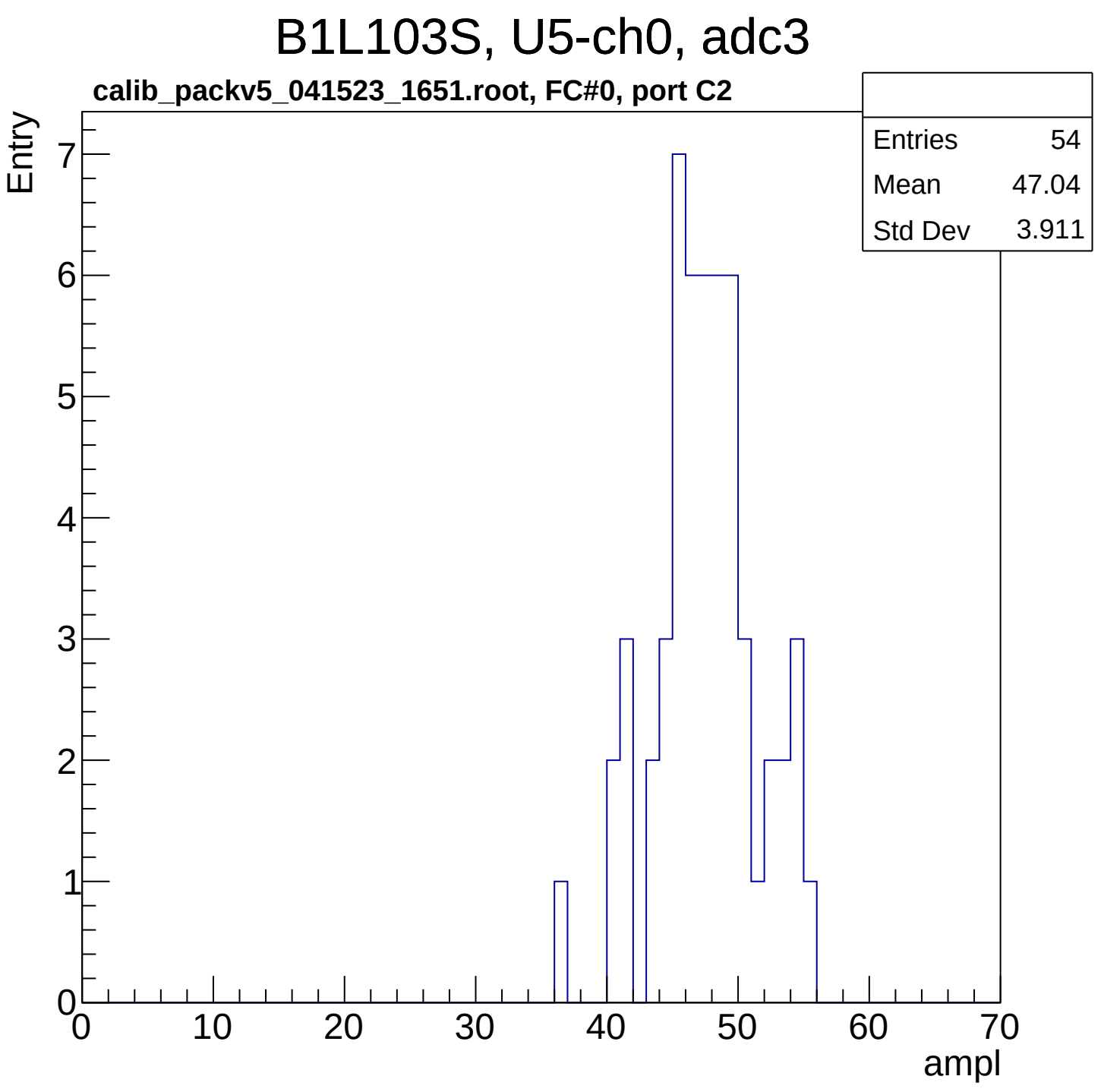
B1L103S, U5-ch0, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 47.04
Std Dev 3.911
Entry
ampl
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1
2
3
4
5
6
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0
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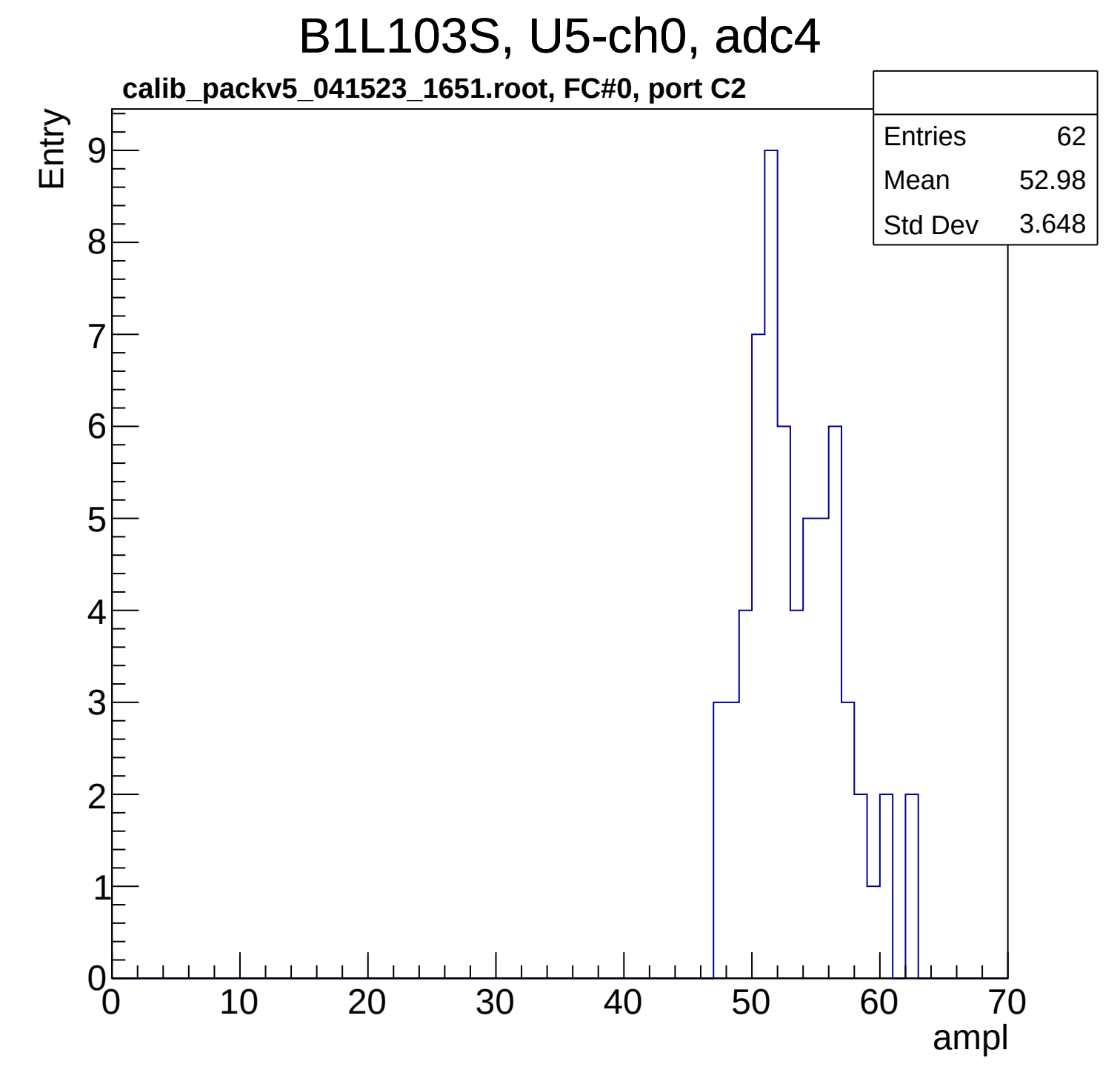
B1L103S, U5-ch0, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 52.98
Std Dev 3.648
Entry
ampl
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3
4
5
6
7
8
9
0
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20
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60
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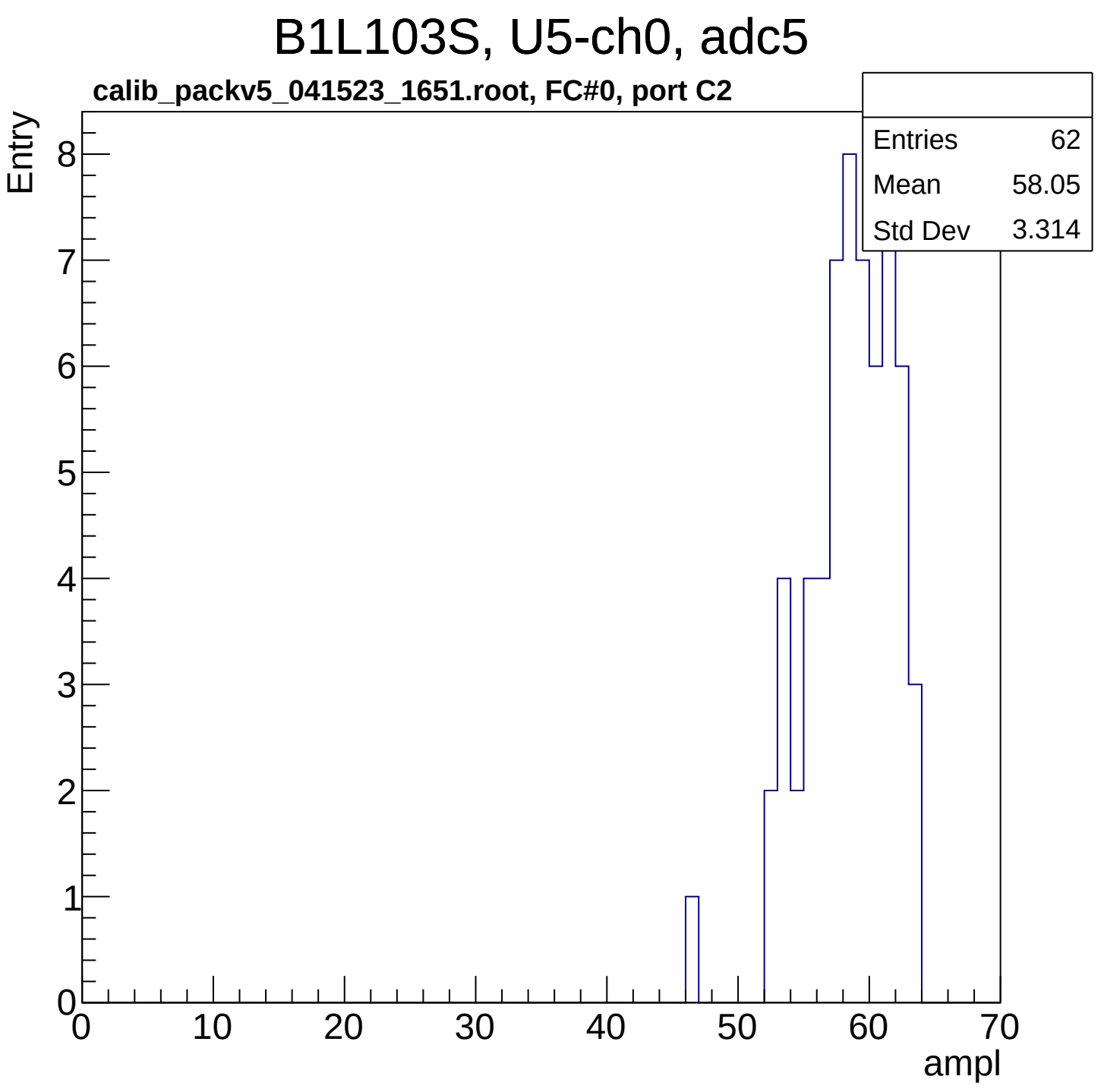
B1L103S, U5-ch0, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 58.05
Std Dev 3.314
Entry
ampl
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2
3
4
5
6
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8
0
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20
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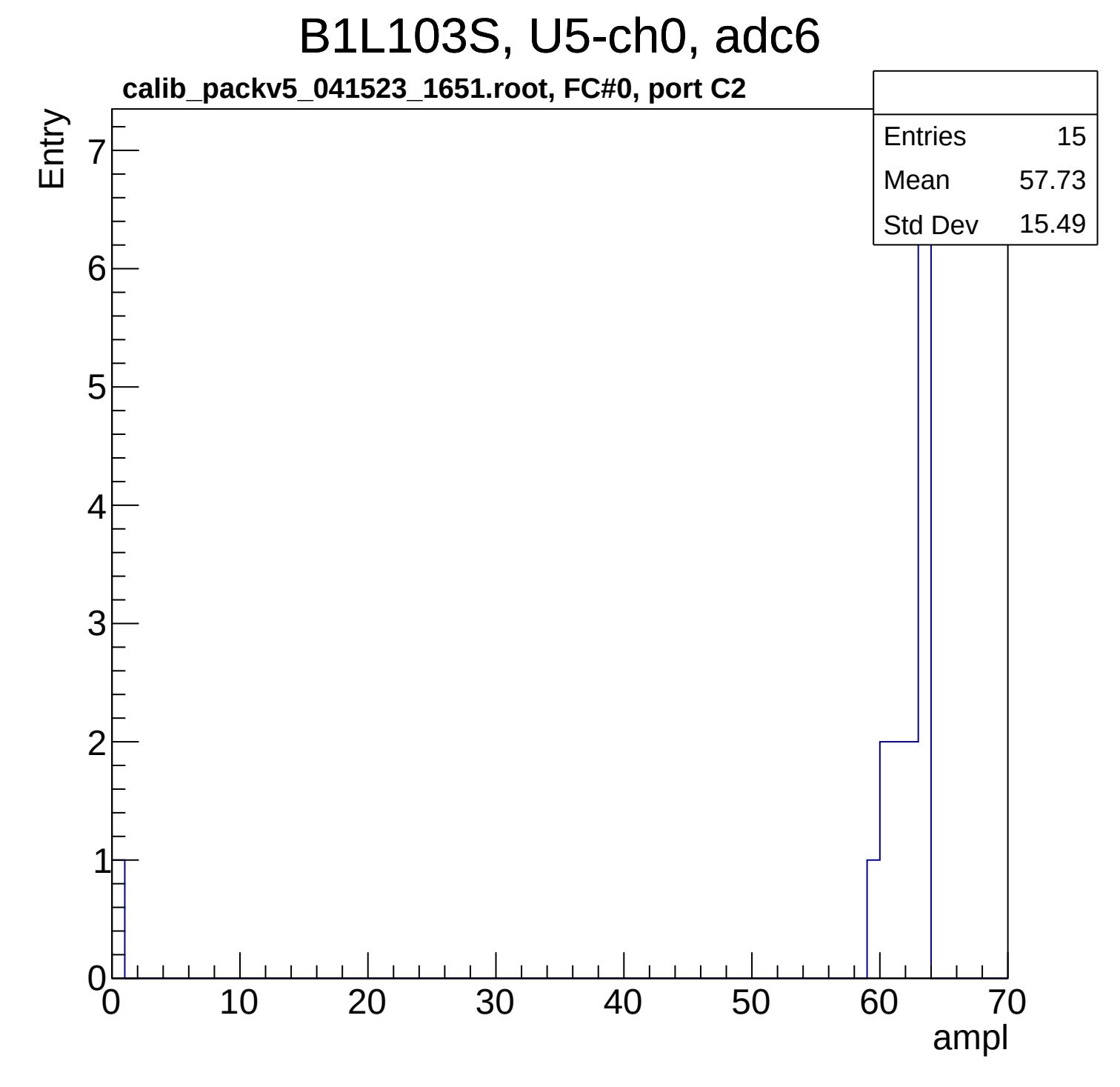
B1L103S, U5-ch0, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.73
Std Dev 15.49
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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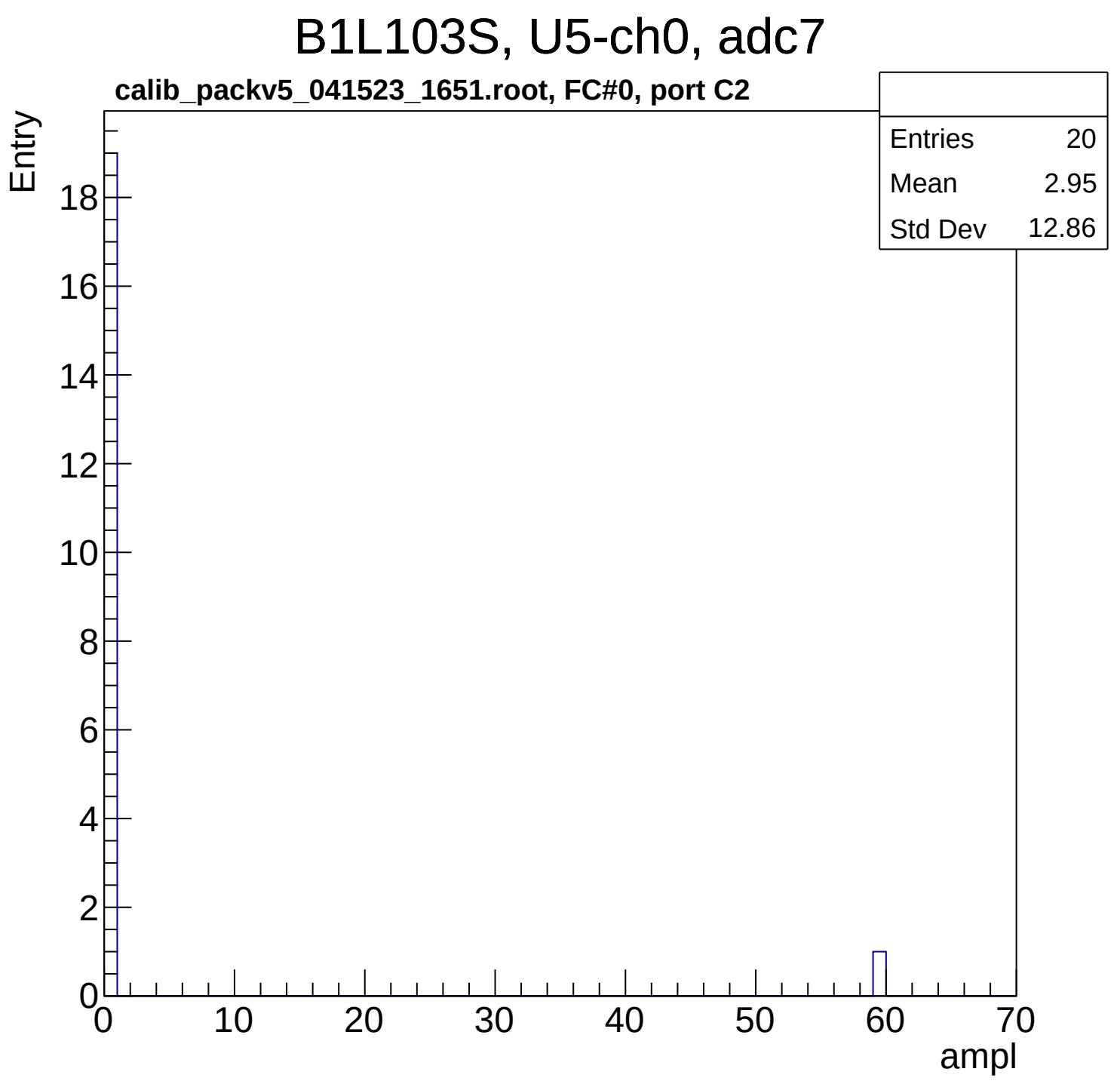
B1L103S, U5-ch0, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 2.95
Std Dev 12.86
Entry
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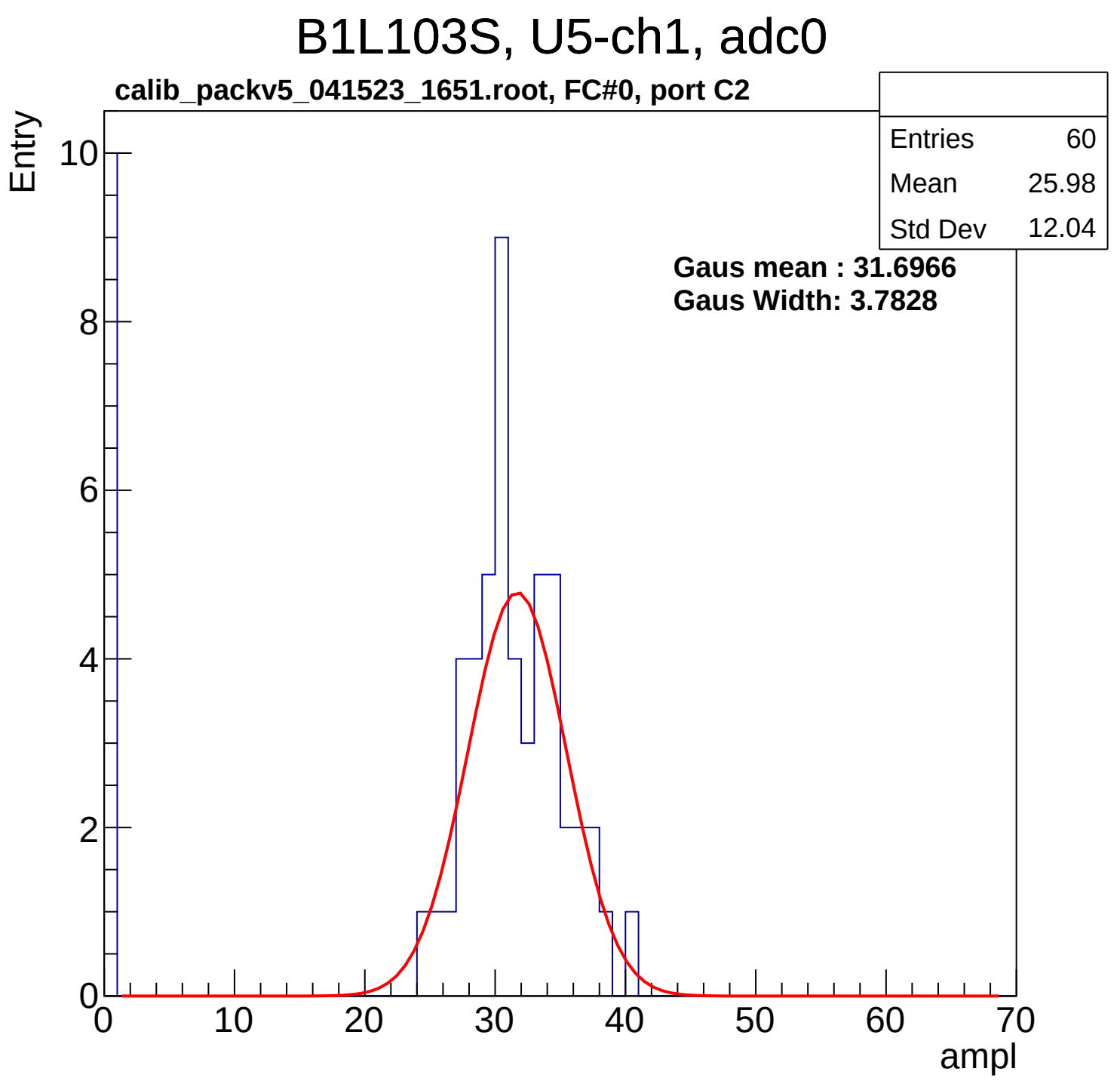
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch1, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 25.98
Std Dev 12.04
Gaus mean : 31.6966
Gaus Width: 3.7828
Entry
ampl
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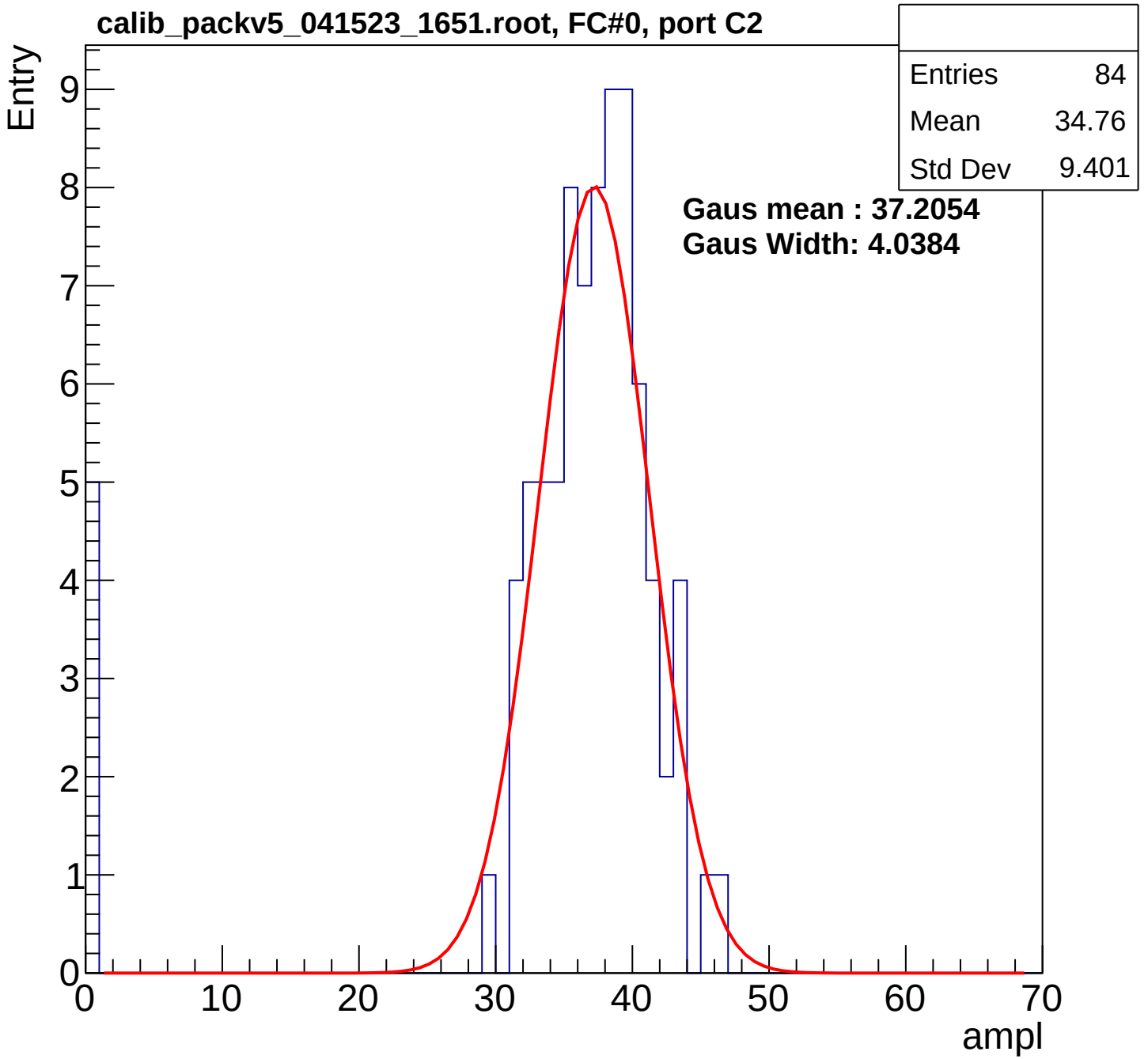
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U5-ch1, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 34.76
Std Dev 9.401
Gaus mean : 37.2054
Gaus Width: 4.0384
Entry
ampl
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10
20
30
40
50
60
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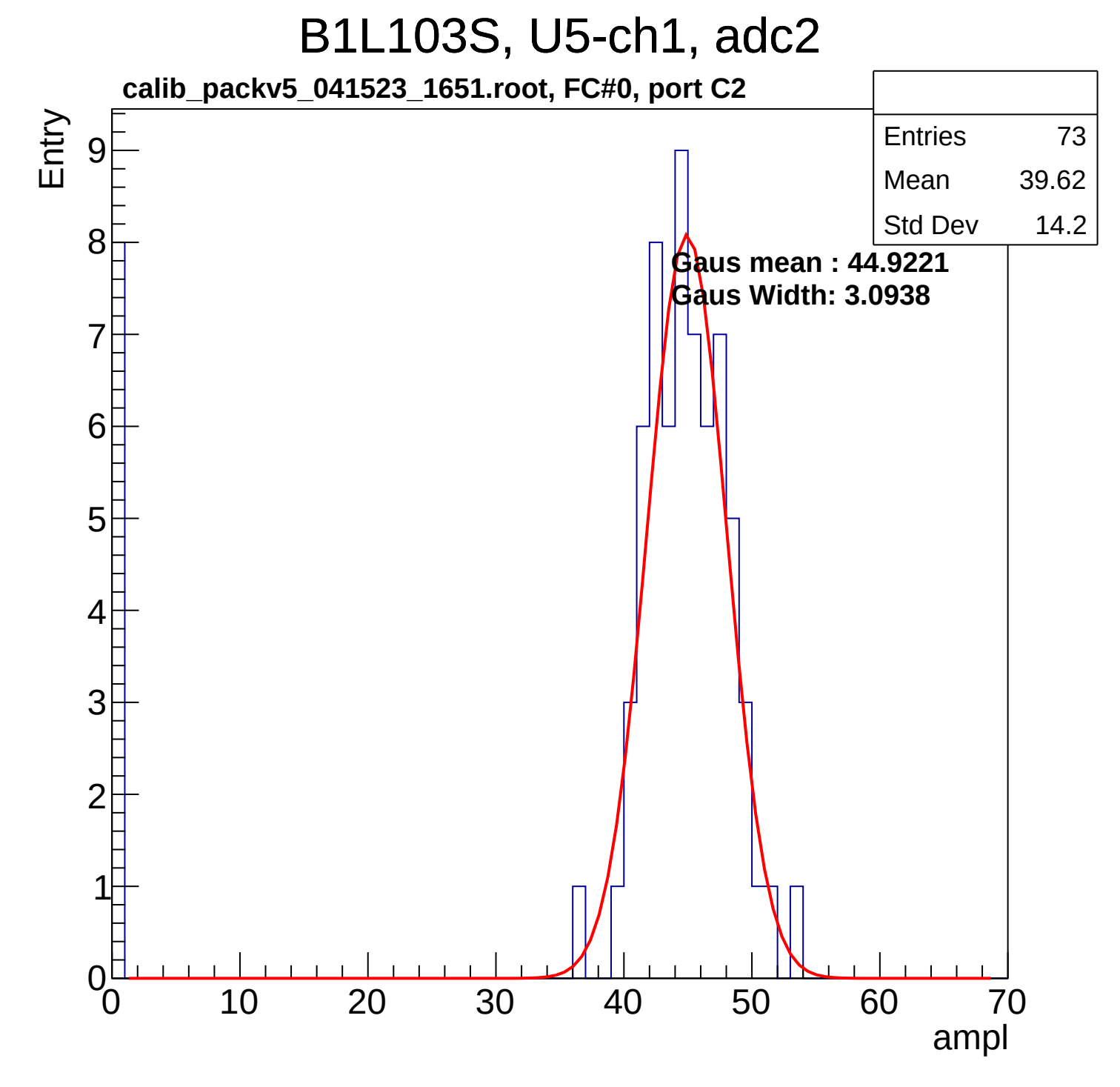
1
2
3
4
5
6
7
8
9


B1L103S, U5-ch1, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 39.62
Std Dev 14.2
Gaus mean : 44.9221
Gaus Width: 3.0938
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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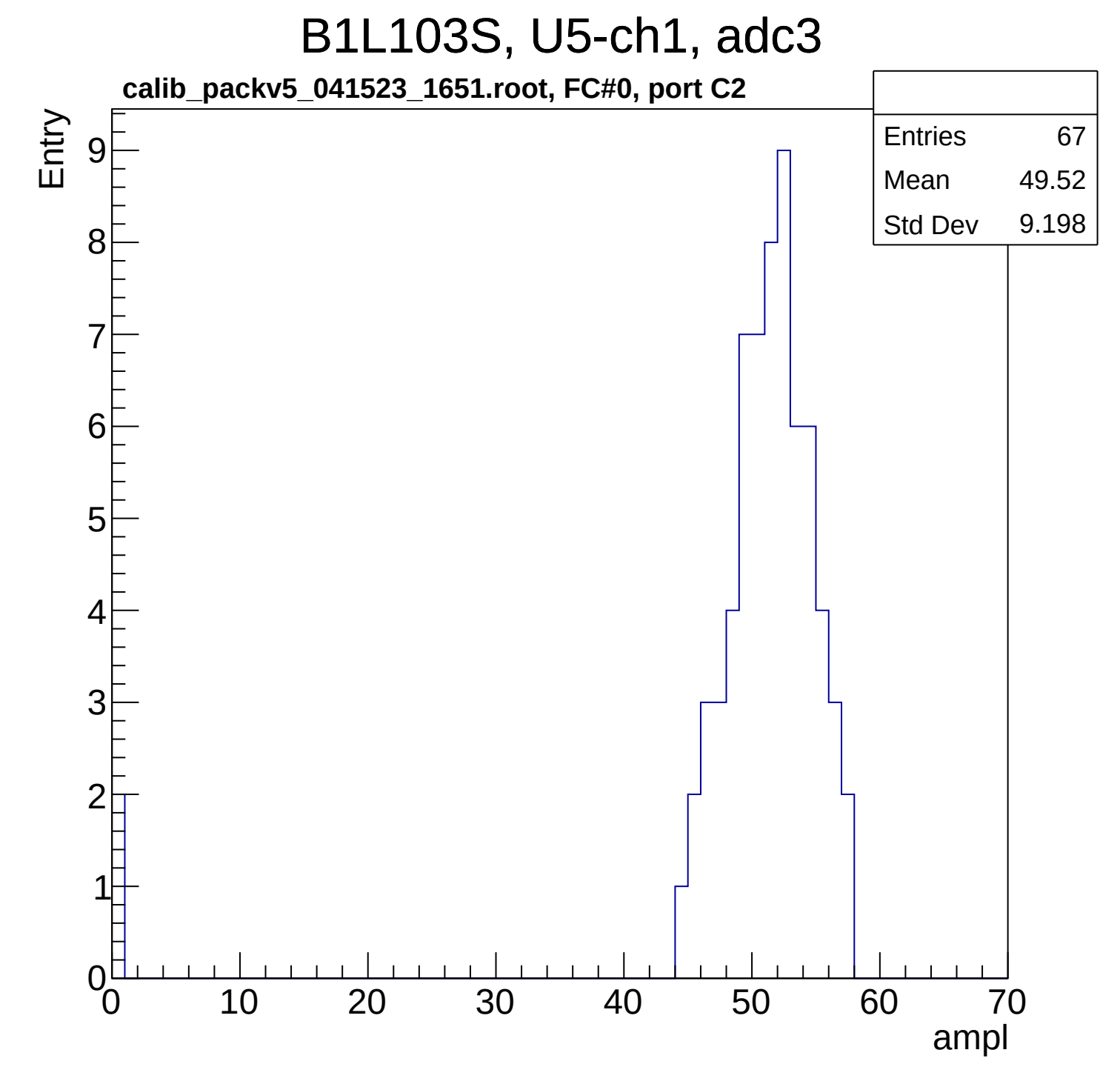
B1L103S, U5-ch1, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 49.52
Std Dev 9.198
Entry
ampl
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3
4
5
6
7
8
9
0
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20
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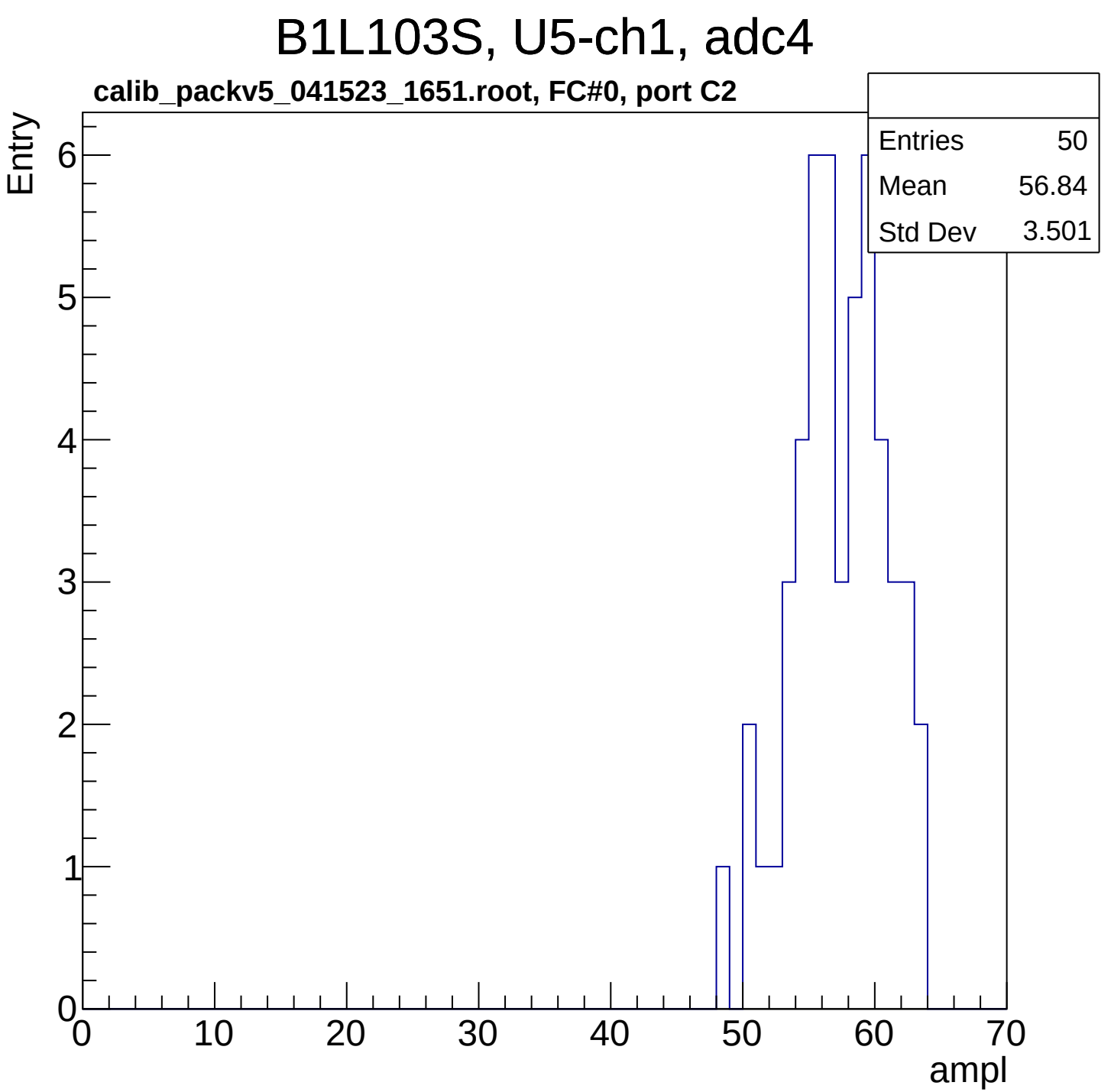
B1L103S, U5-ch1, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 56.84
Std Dev 3.501
Entry
ampl
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2
3
4
5
6
0
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40
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60
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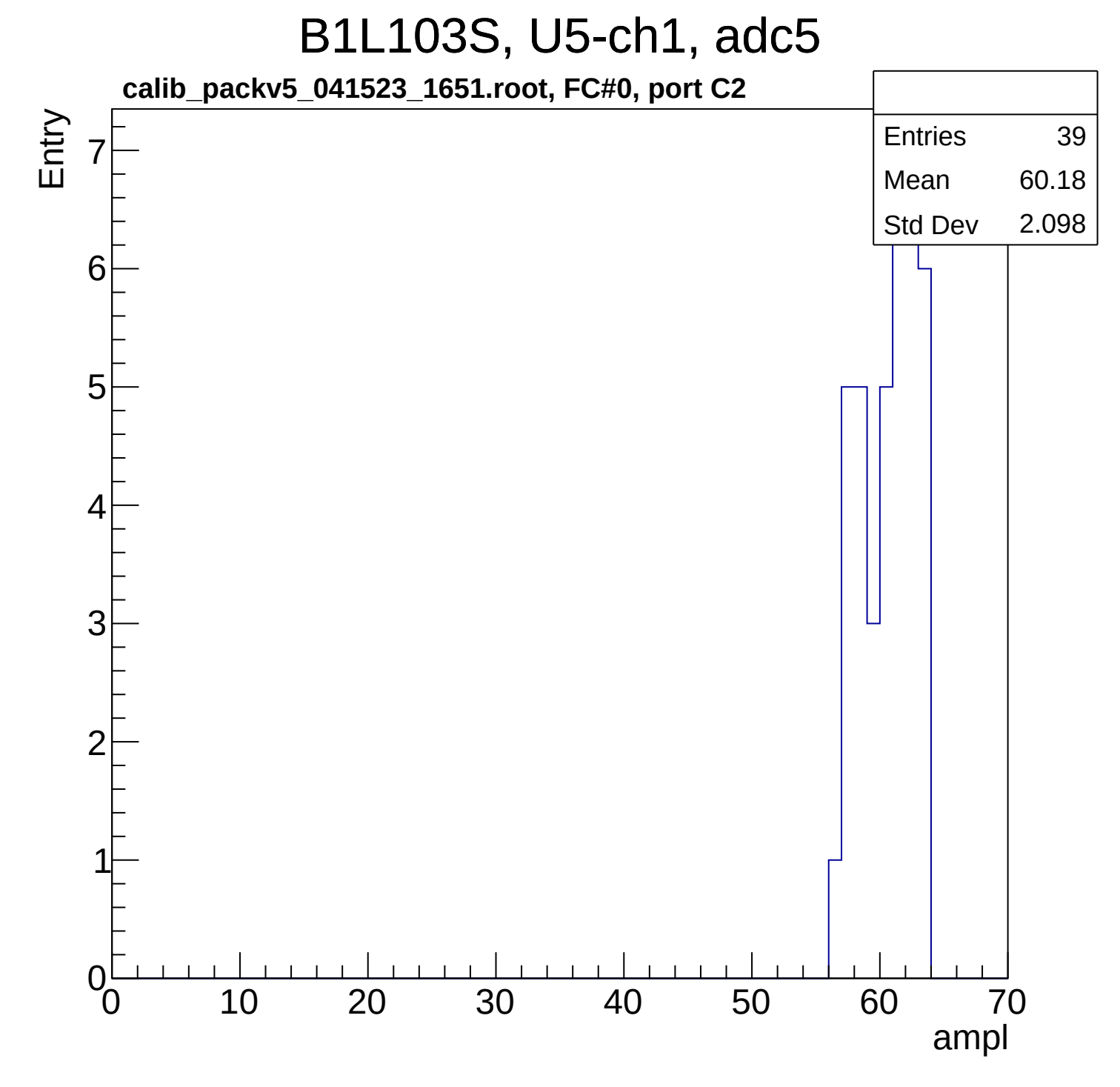
B1L103S, U5-ch1, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 60.18
Std Dev 2.098
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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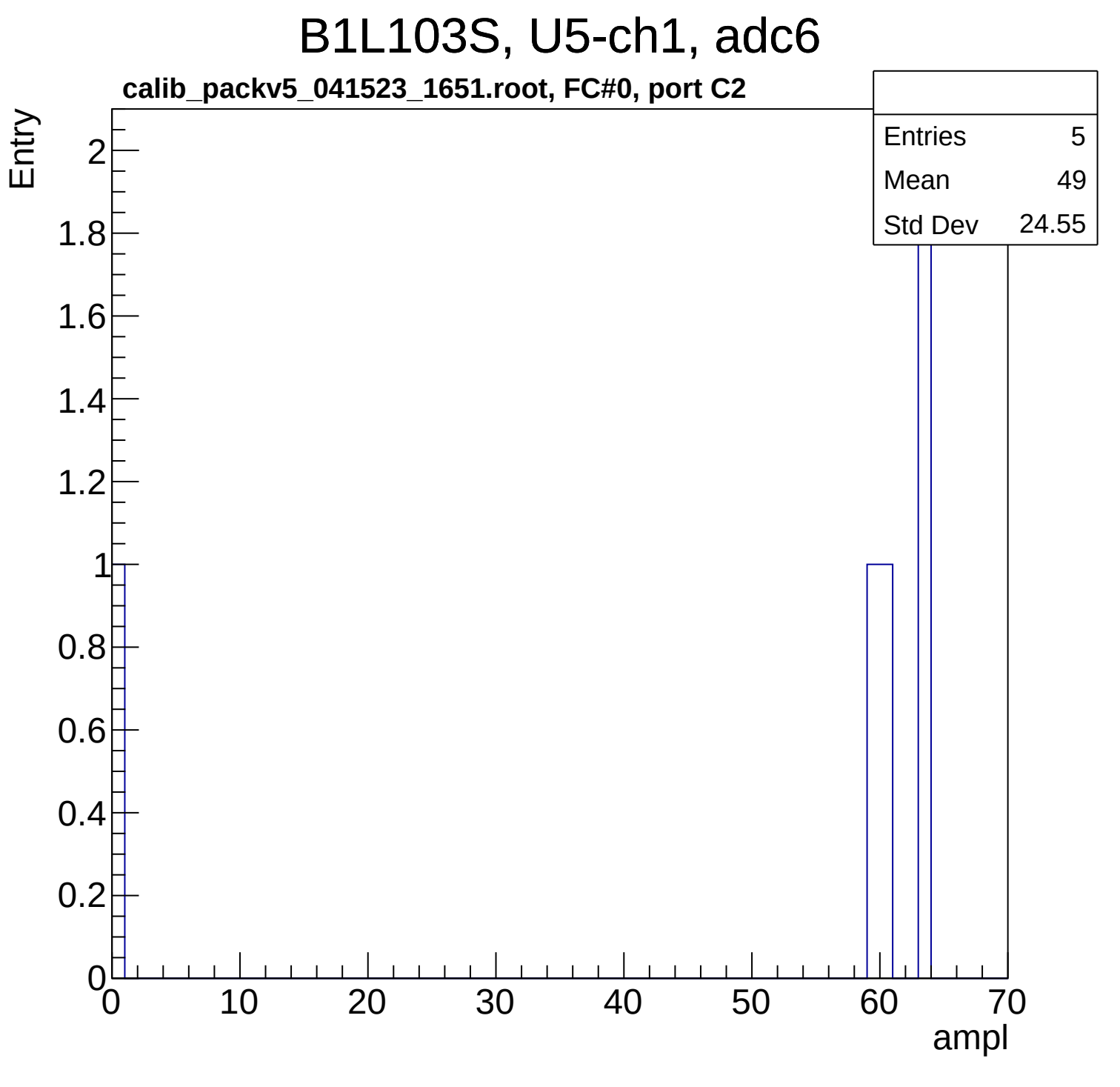
B1L103S, U5-ch1, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 49
Std Dev 24.55
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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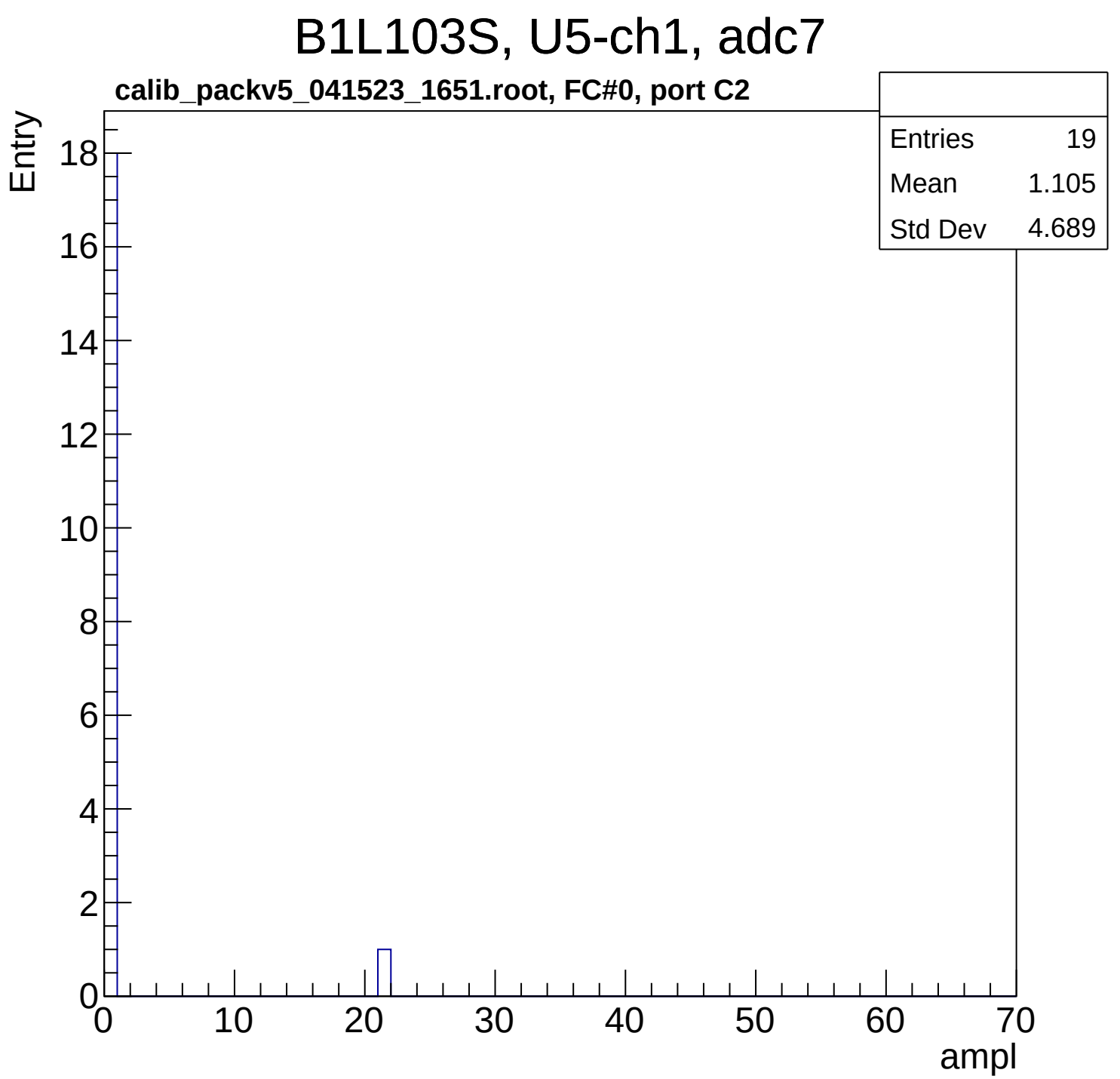
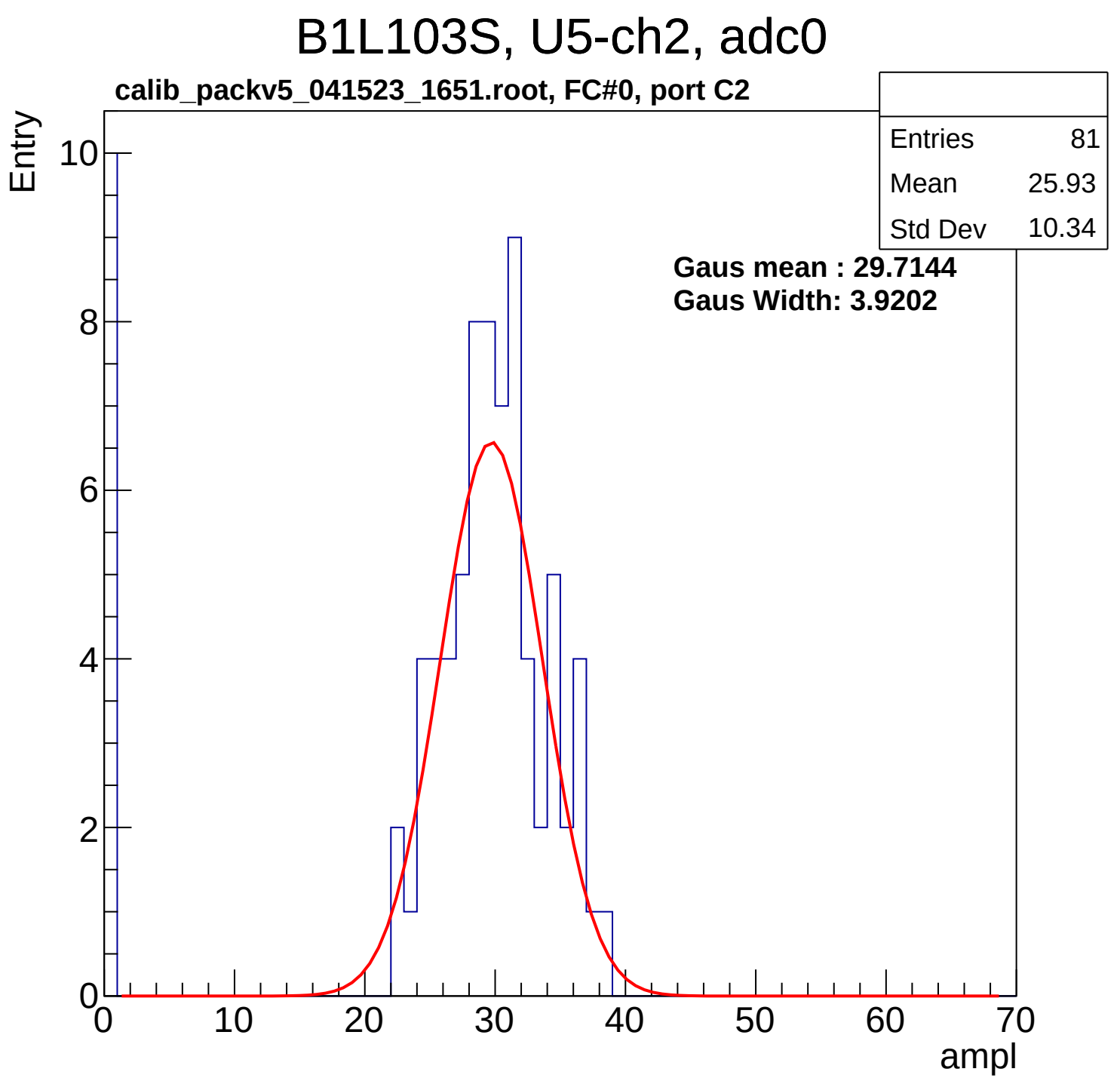

B1L103S, U5-ch1, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch2, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 25.93
Std Dev 10.34
Gaus mean : 29.7144
Gaus Width: 3.9202
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
50
60
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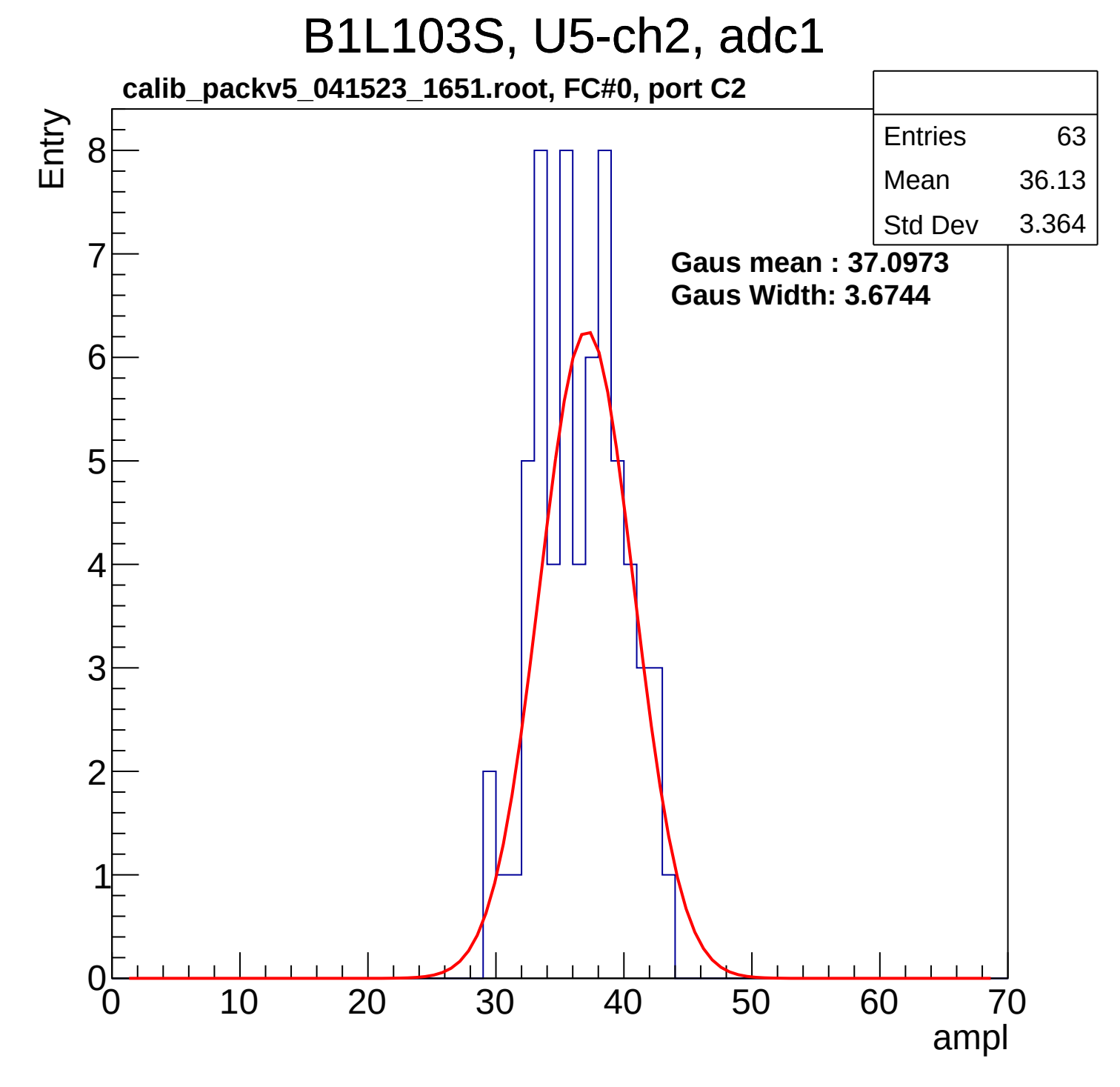
B1L103S, U5-ch2, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 36.13
Std Dev 3.364
Gaus mean : 37.0973
Gaus Width: 3.6744
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
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60
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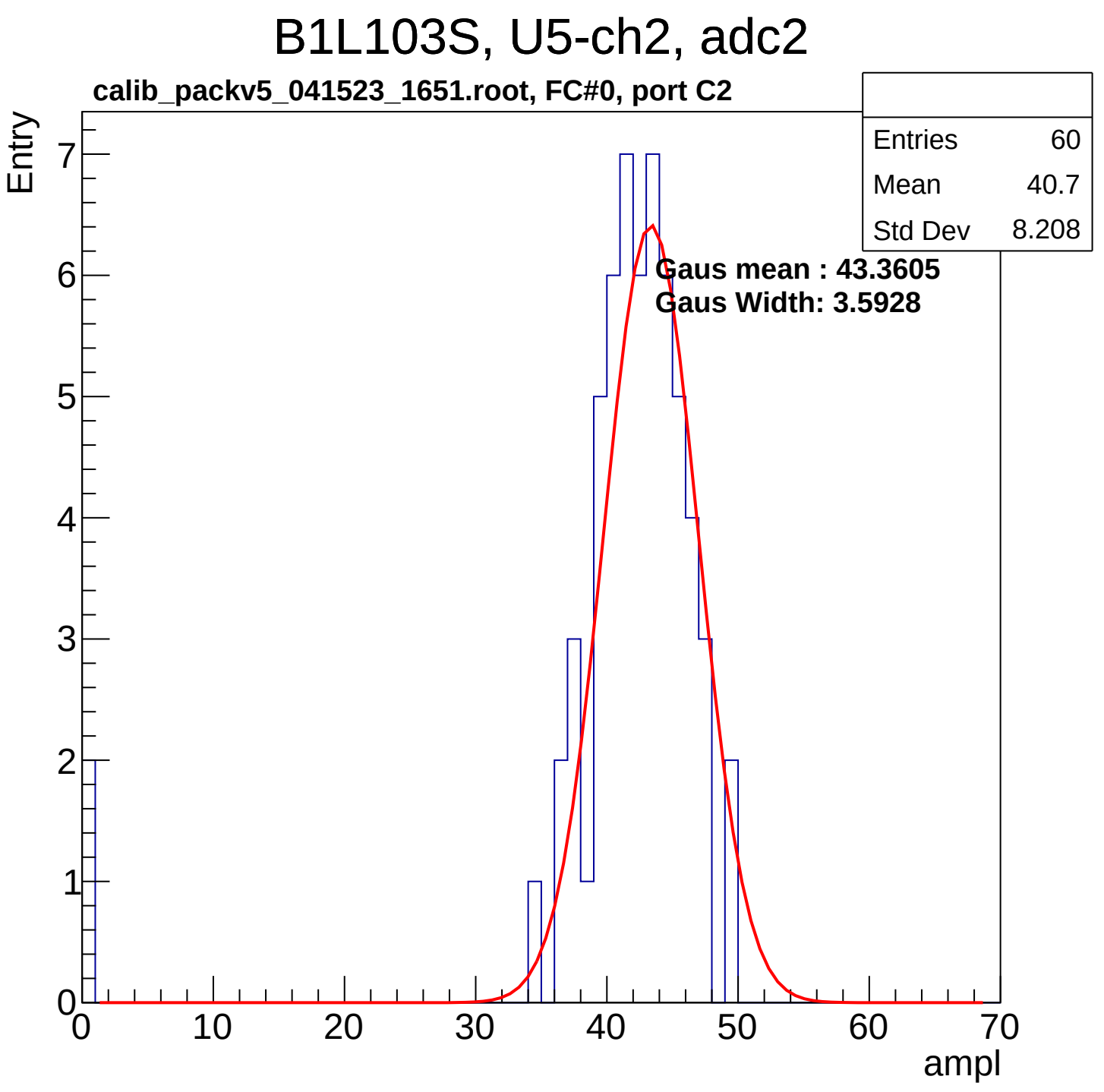
B1L103S, U5-ch2, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 40.7
Std Dev 8.208
Gaus mean : 43.3605
Gaus Width: 3.5928
Entry
ampl
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2
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4
5
6
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0
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60
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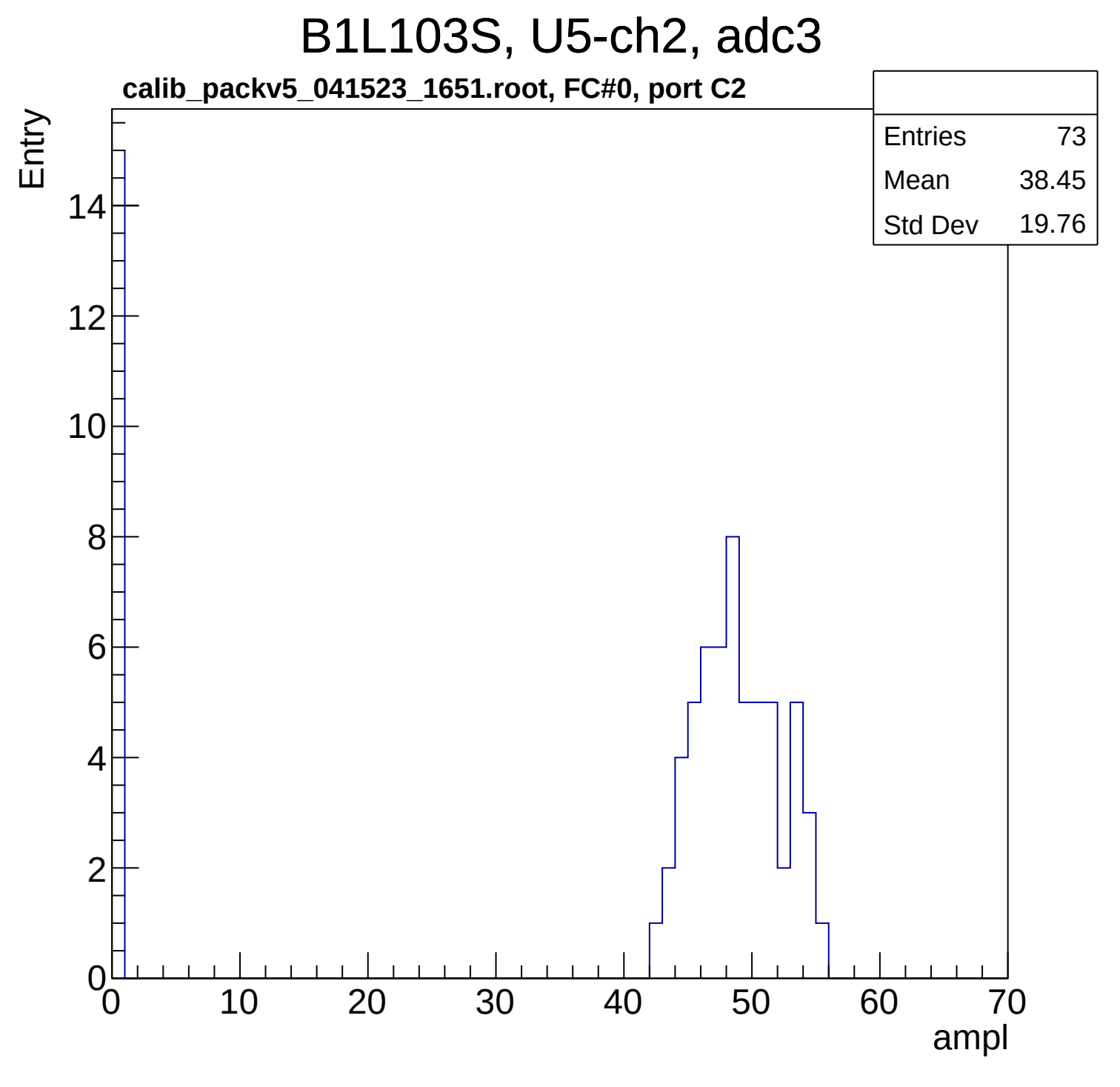
B1L103S, U5-ch2, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 38.45
Std Dev 19.76
Entry
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10
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50
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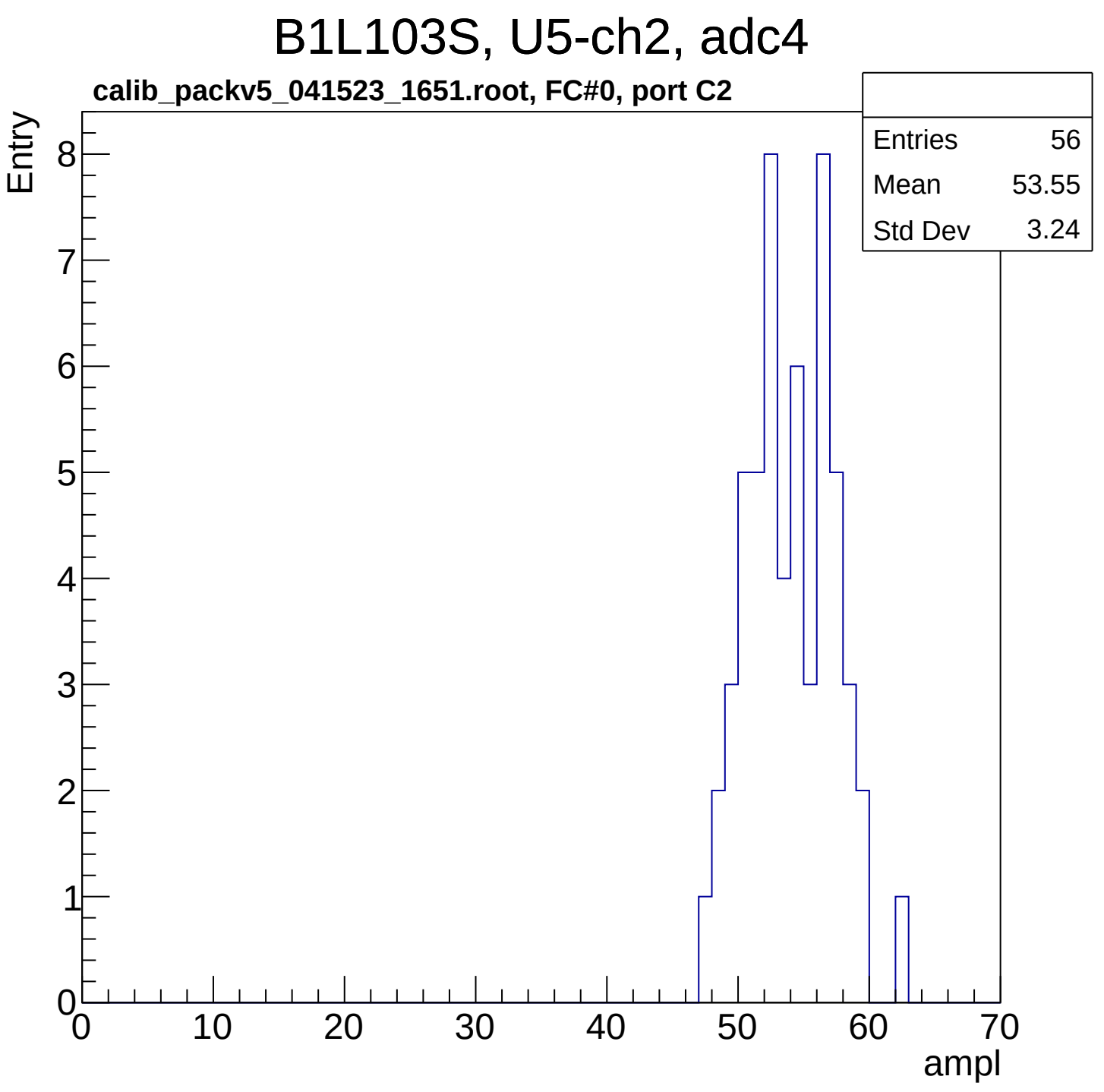
70
ampl


B1L103S, U5-ch2, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 53.55
Std Dev 3.24
Entry
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4
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0
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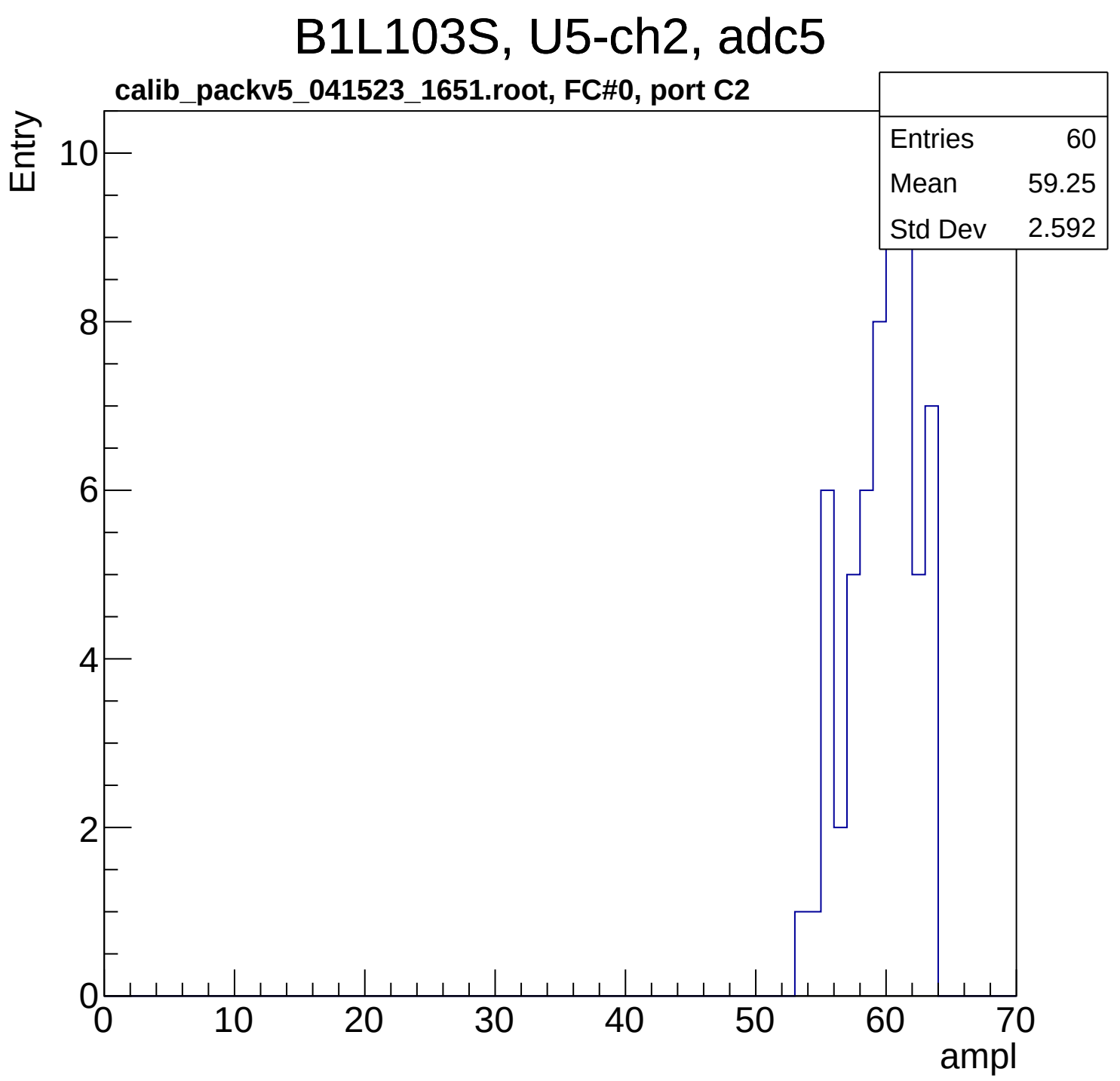
50
60
70
ampl


B1L103S, U5-ch2, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 59.25
Std Dev 2.592
Entry
ampl
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0
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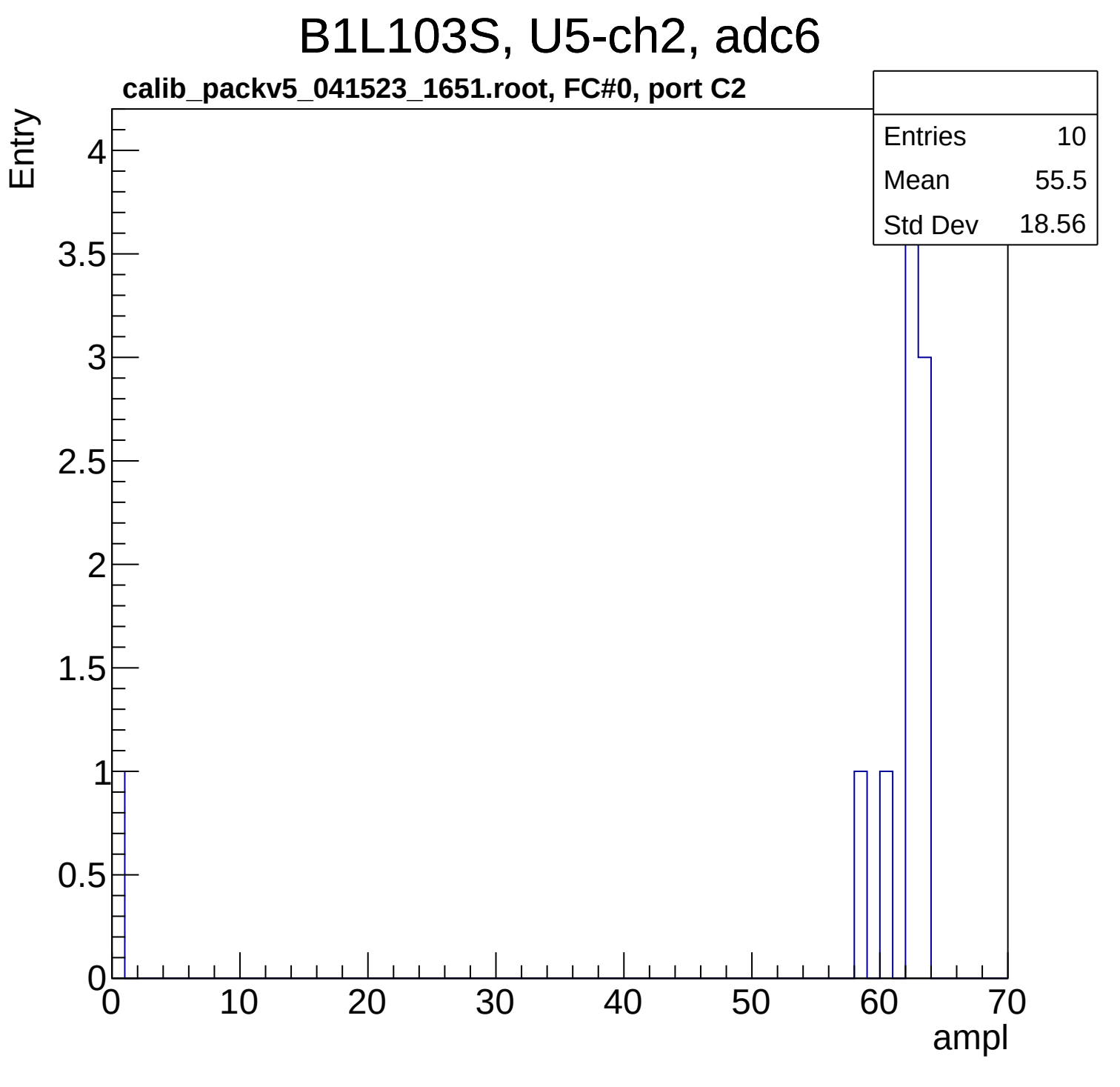
B1L103S, U5-ch2, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.5
Std Dev 18.56
Entry
ampl
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1.5
2
2.5
3
3.5
4
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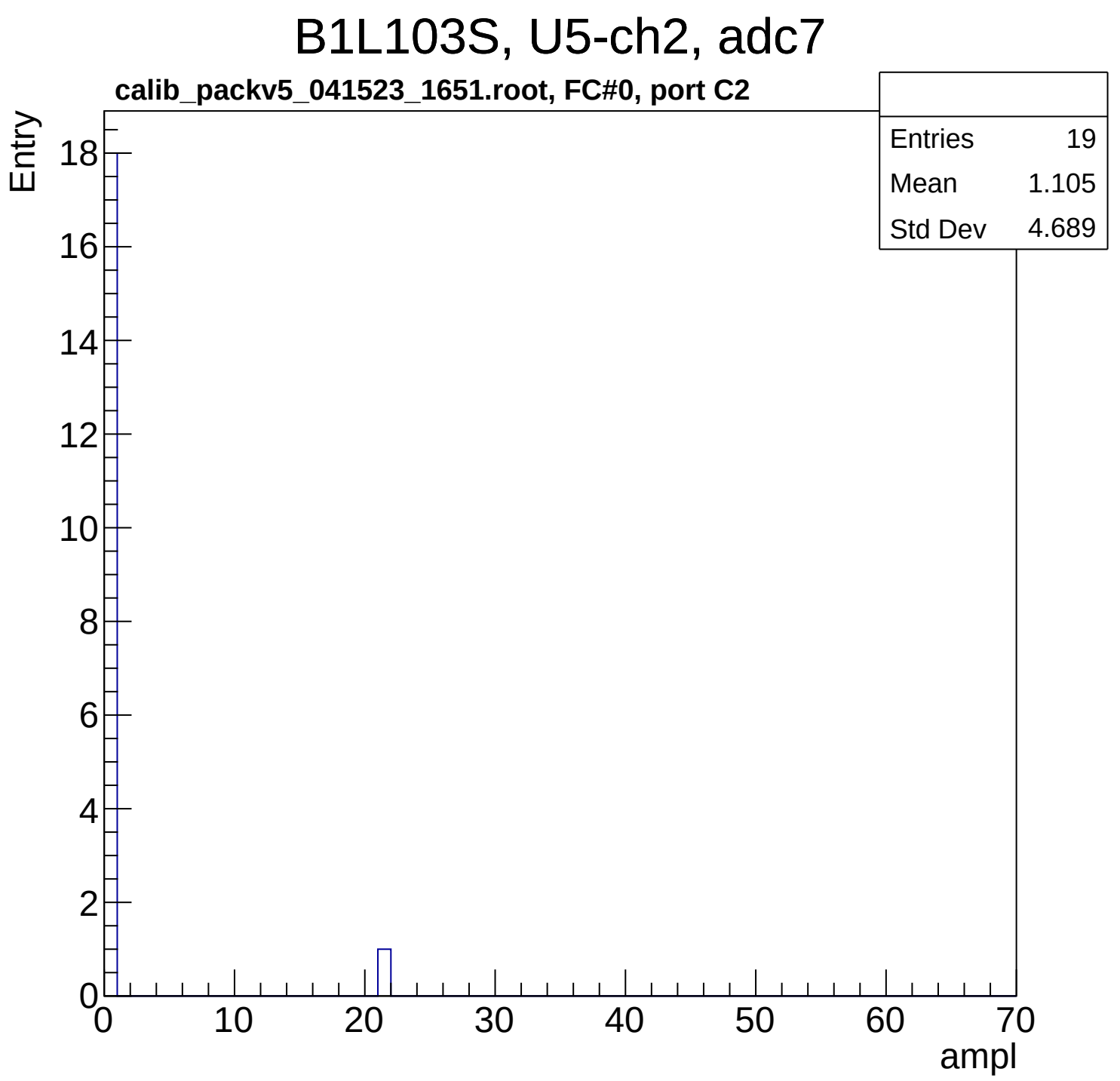
B1L103S, U5-ch2, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
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6
8
10
12
14
16
18
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10
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30
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50
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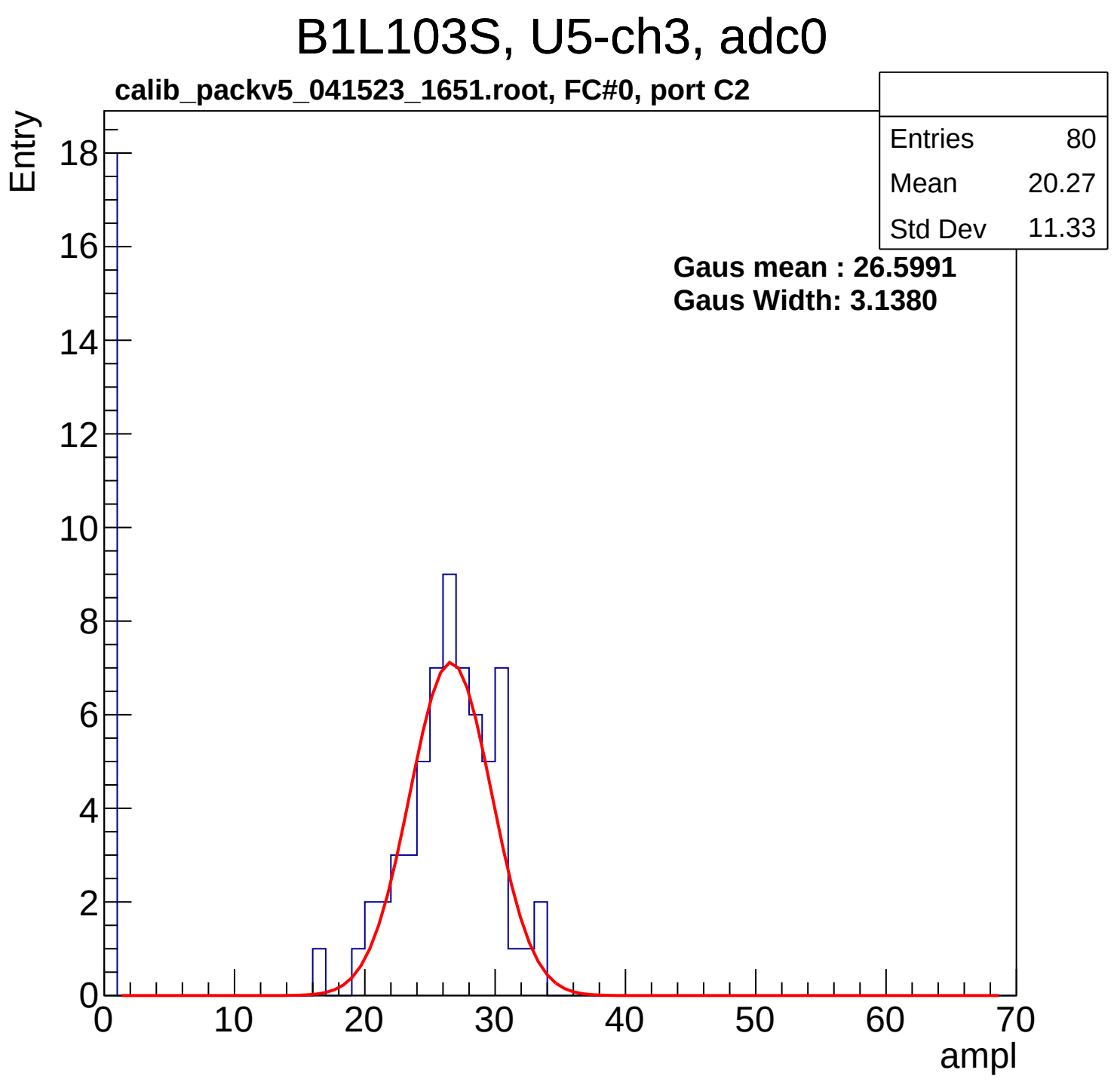
70
ampl


B1L103S, U5-ch3, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 20.27
Std Dev 11.33
Gaus mean : 26.5991
Gaus Width: 3.1380
Entry
ampl
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4
6
8
10
12
14
16
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0
10
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60
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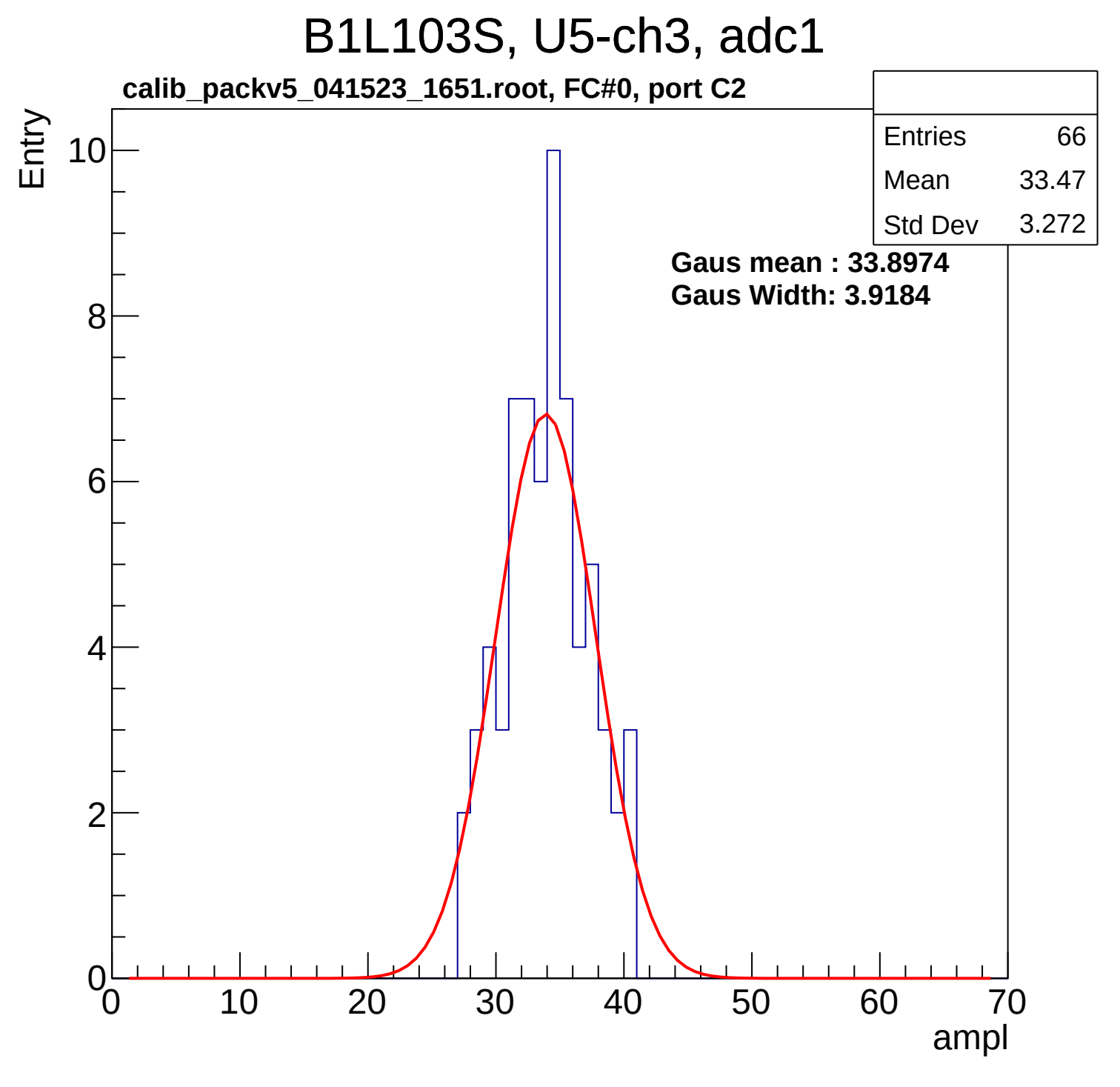
B1L103S, U5-ch3, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 33.47
Std Dev 3.272
Gaus mean : 33.8974
Gaus Width: 3.9184
Entry
ampl
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2
4
6
8
10
0
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20
30
40
50
60
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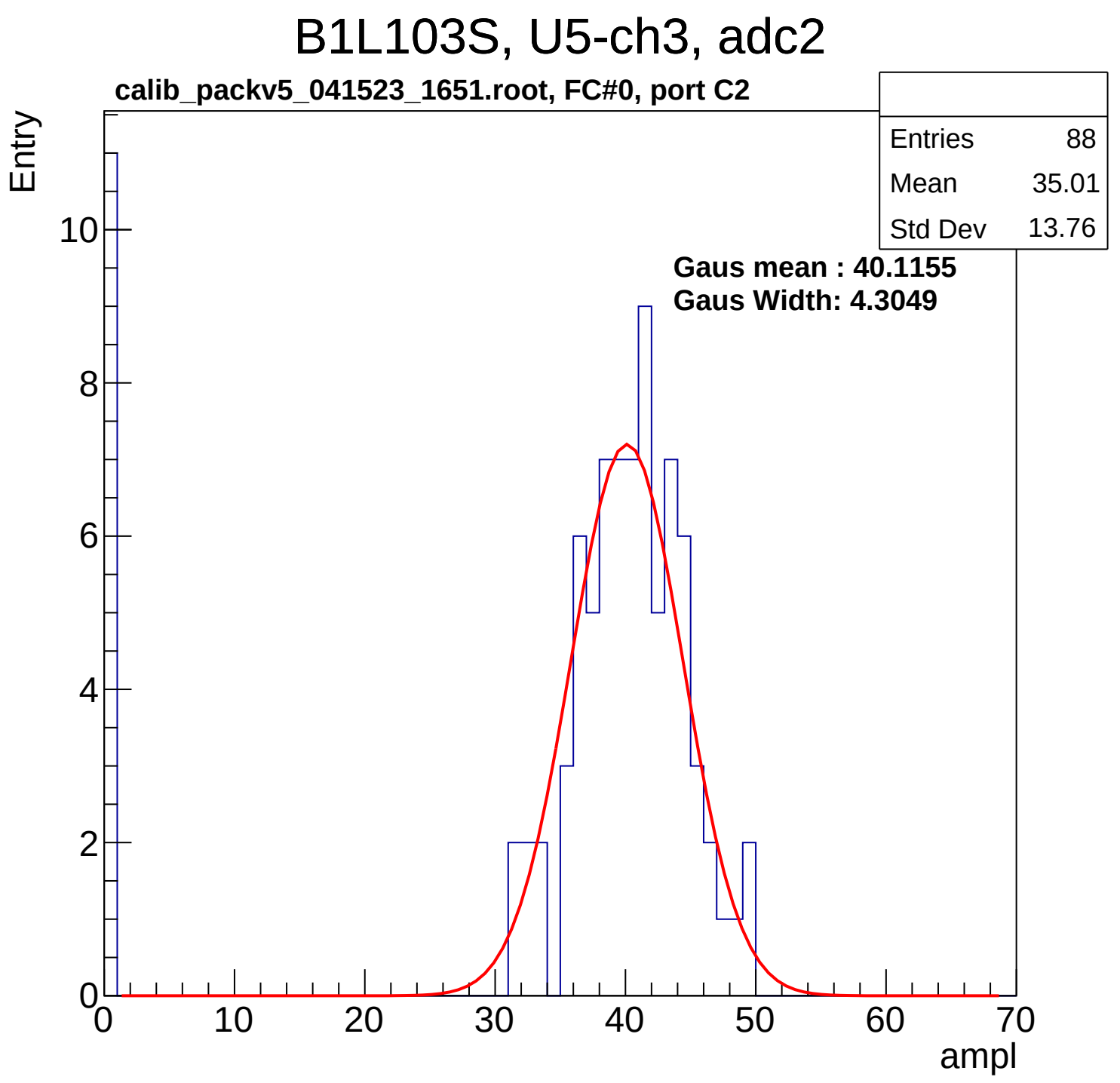
B1L103S, U5-ch3, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 35.01
Std Dev 13.76
Gaus mean : 40.1155
Gaus Width: 4.3049
Entry
ampl
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6
8
10
0
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40
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60
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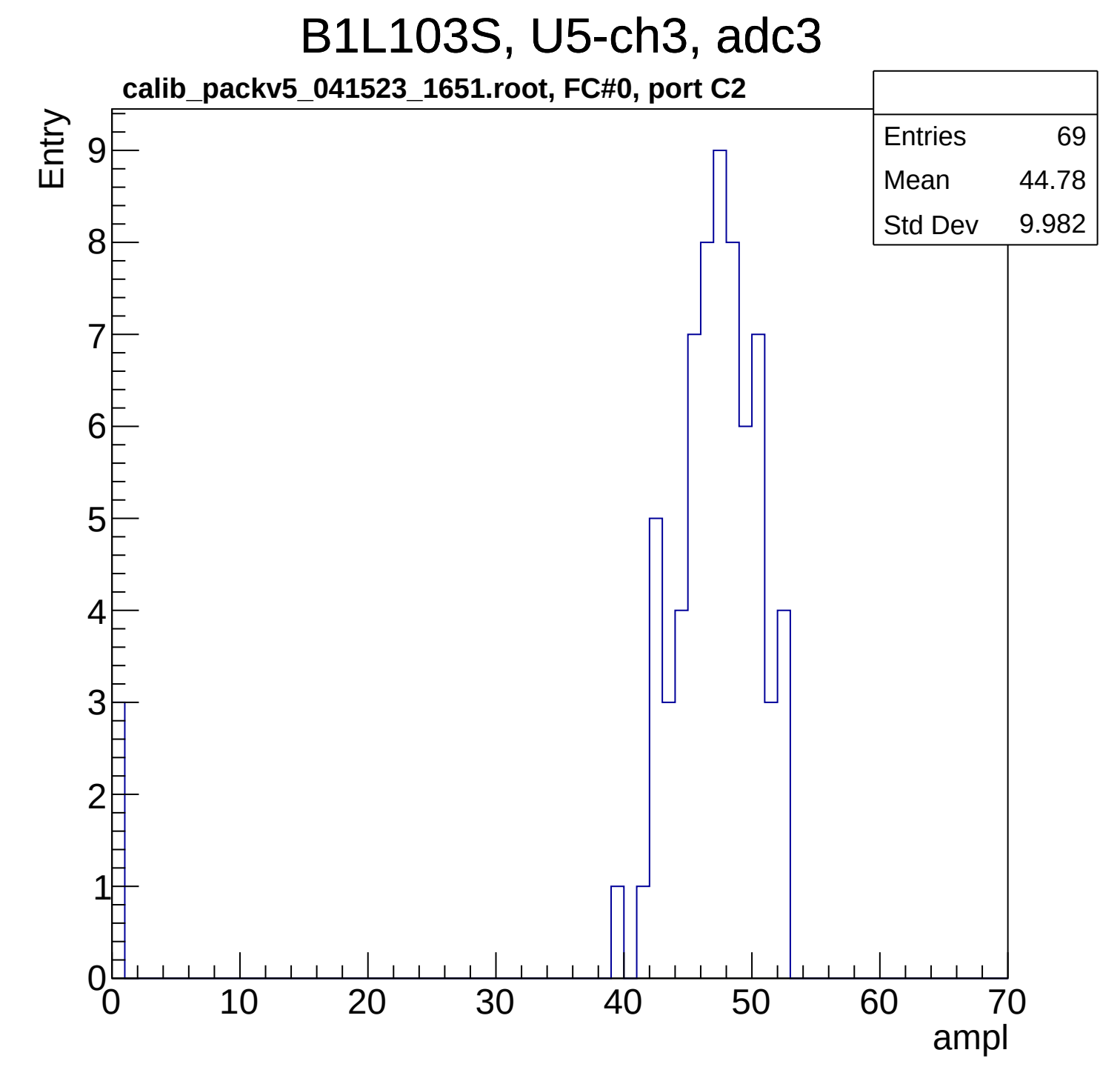
B1L103S, U5-ch3, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 44.78
Std Dev 9.982
Entry
ampl
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5
6
7
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9
0
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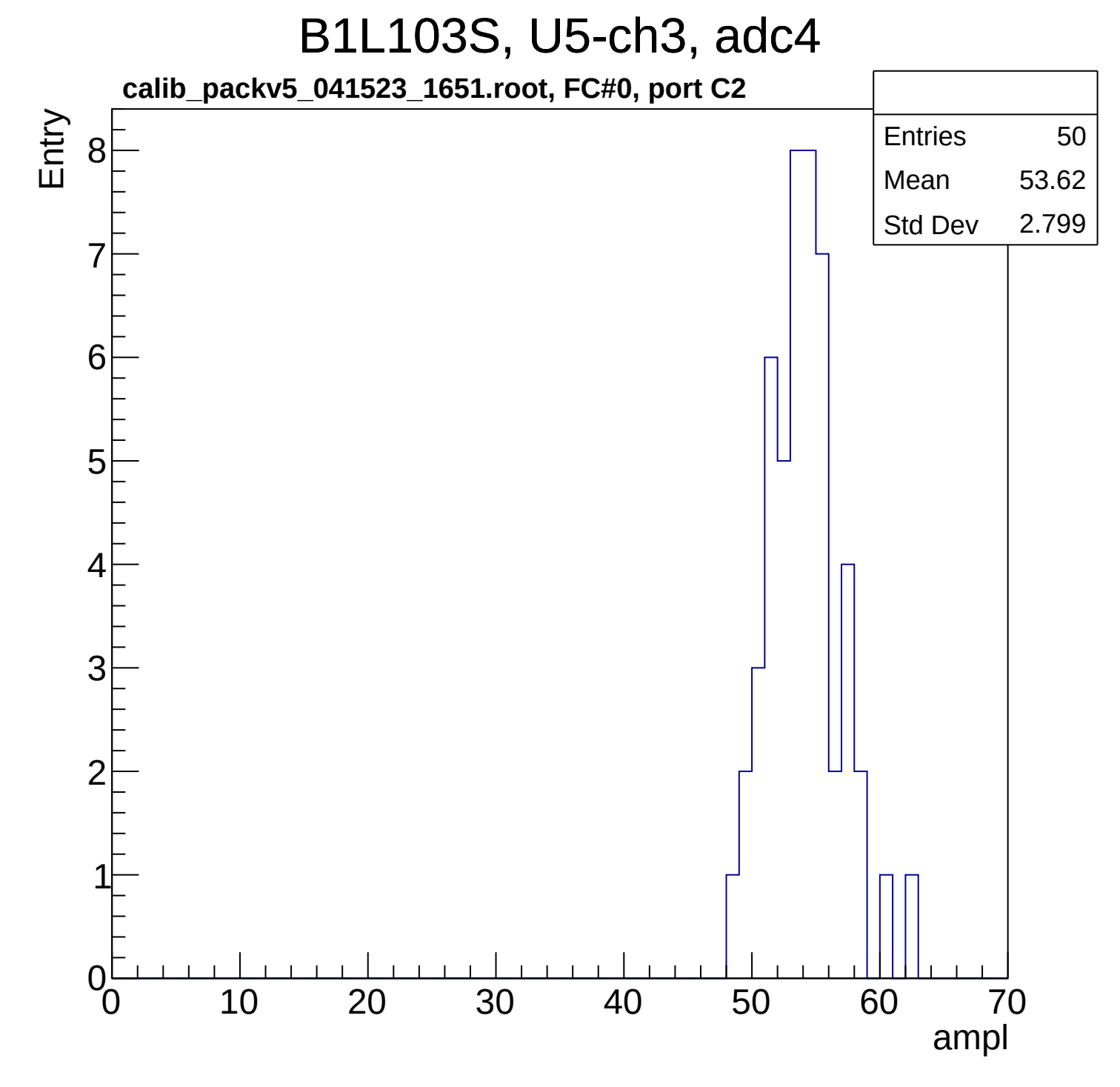
B1L103S, U5-ch3, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 53.62
Std Dev 2.799
Entry
ampl
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3
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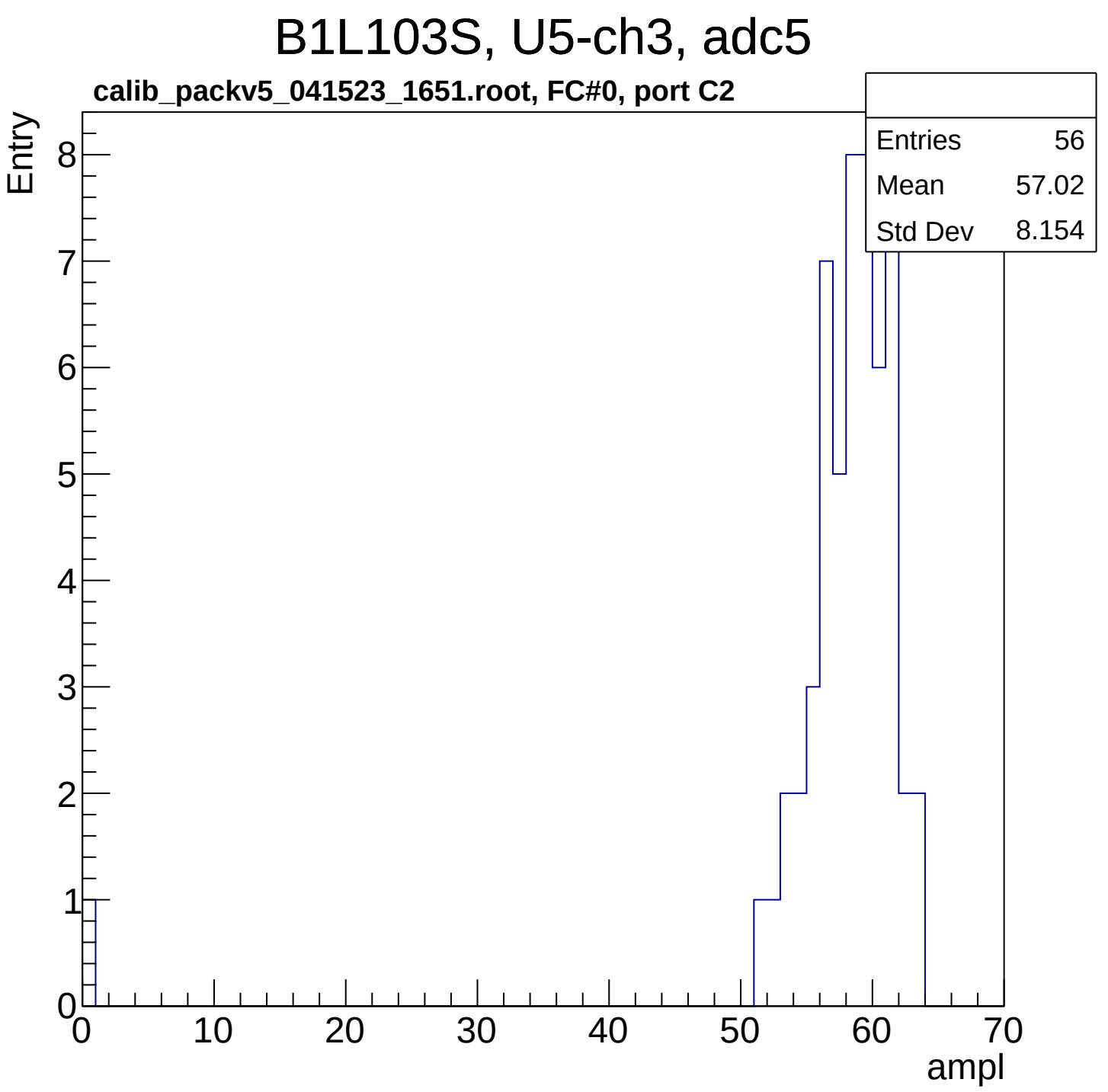
B1L103S, U5-ch3, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 57.02
Std Dev 8.154
Entry
ampl
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2
3
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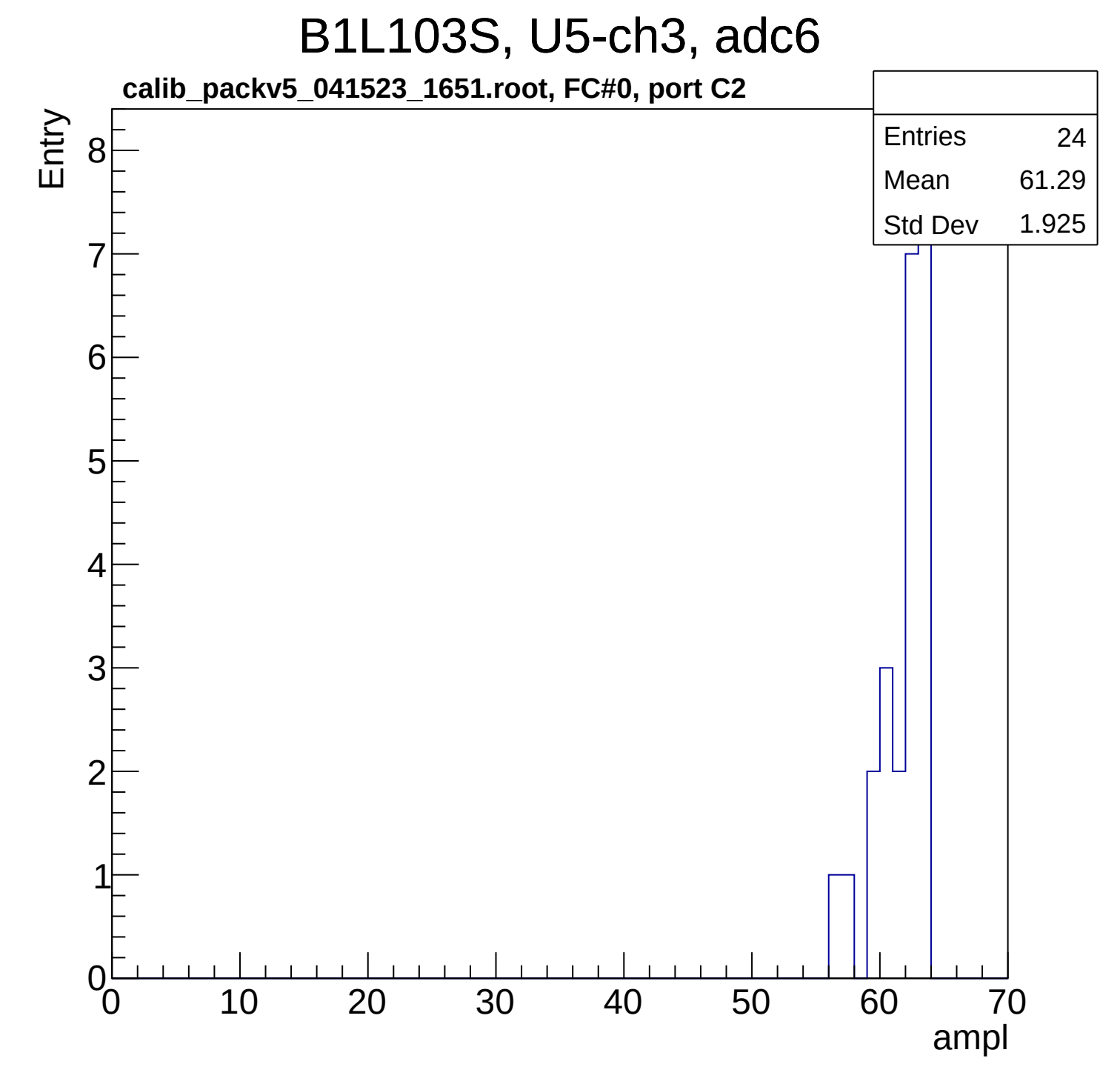
B1L103S, U5-ch3, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 61.29
Std Dev 1.925
Entry
ampl
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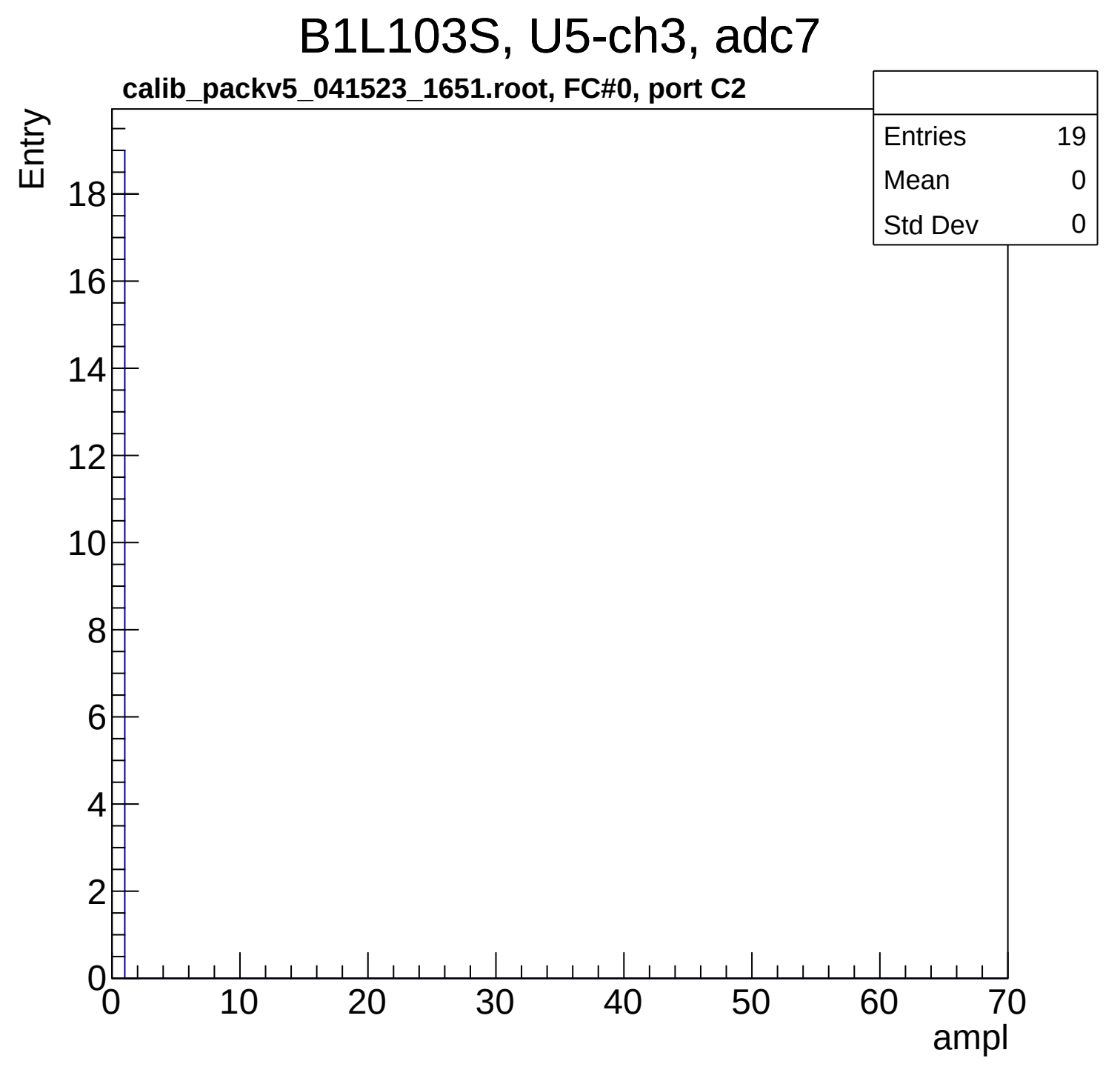
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U5-ch3, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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10
20
30
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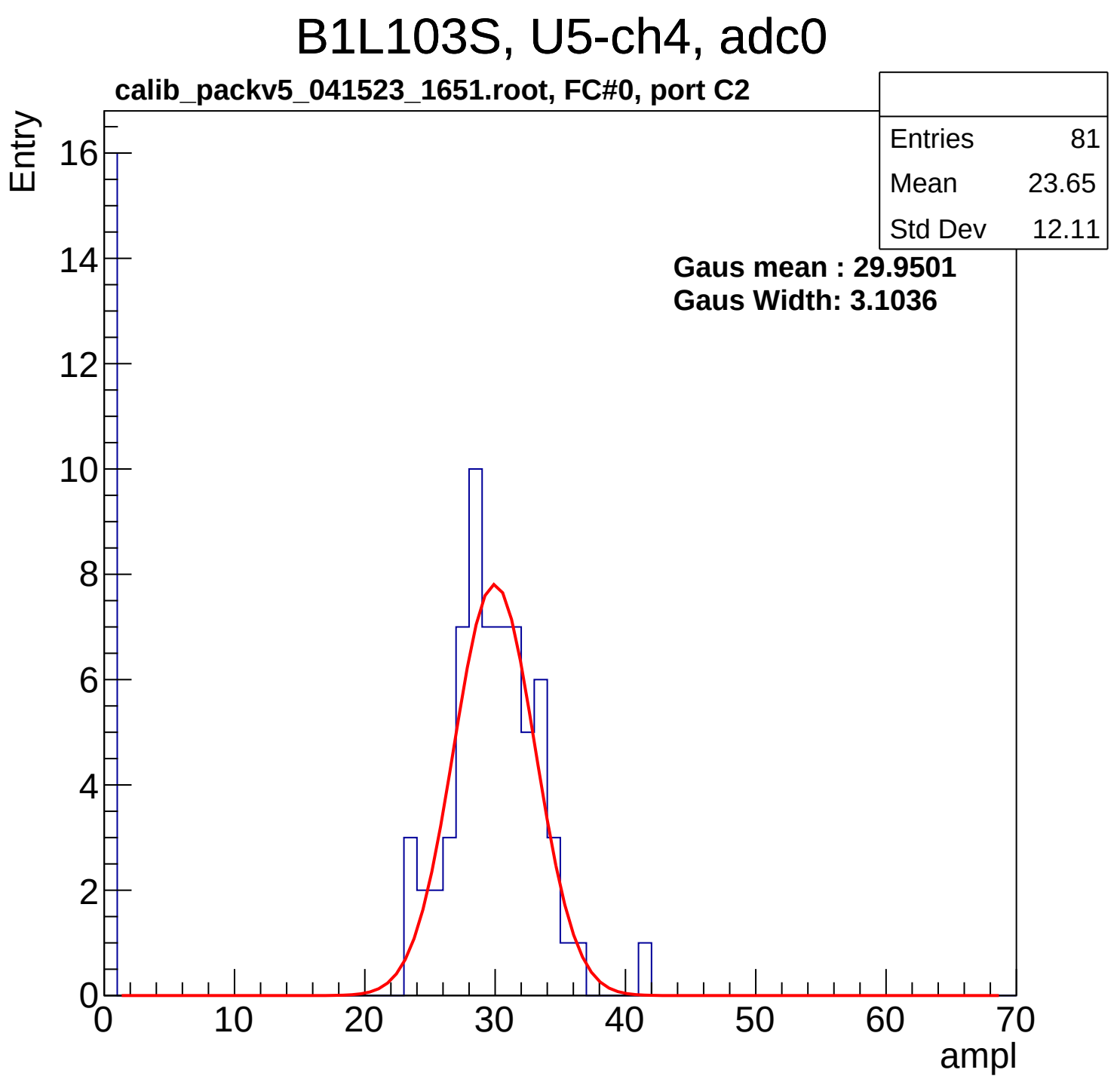
70
ampl


B1L103S, U5-ch4, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 23.65
Std Dev 12.11
Gaus mean : 29.9501
Gaus Width: 3.1036
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
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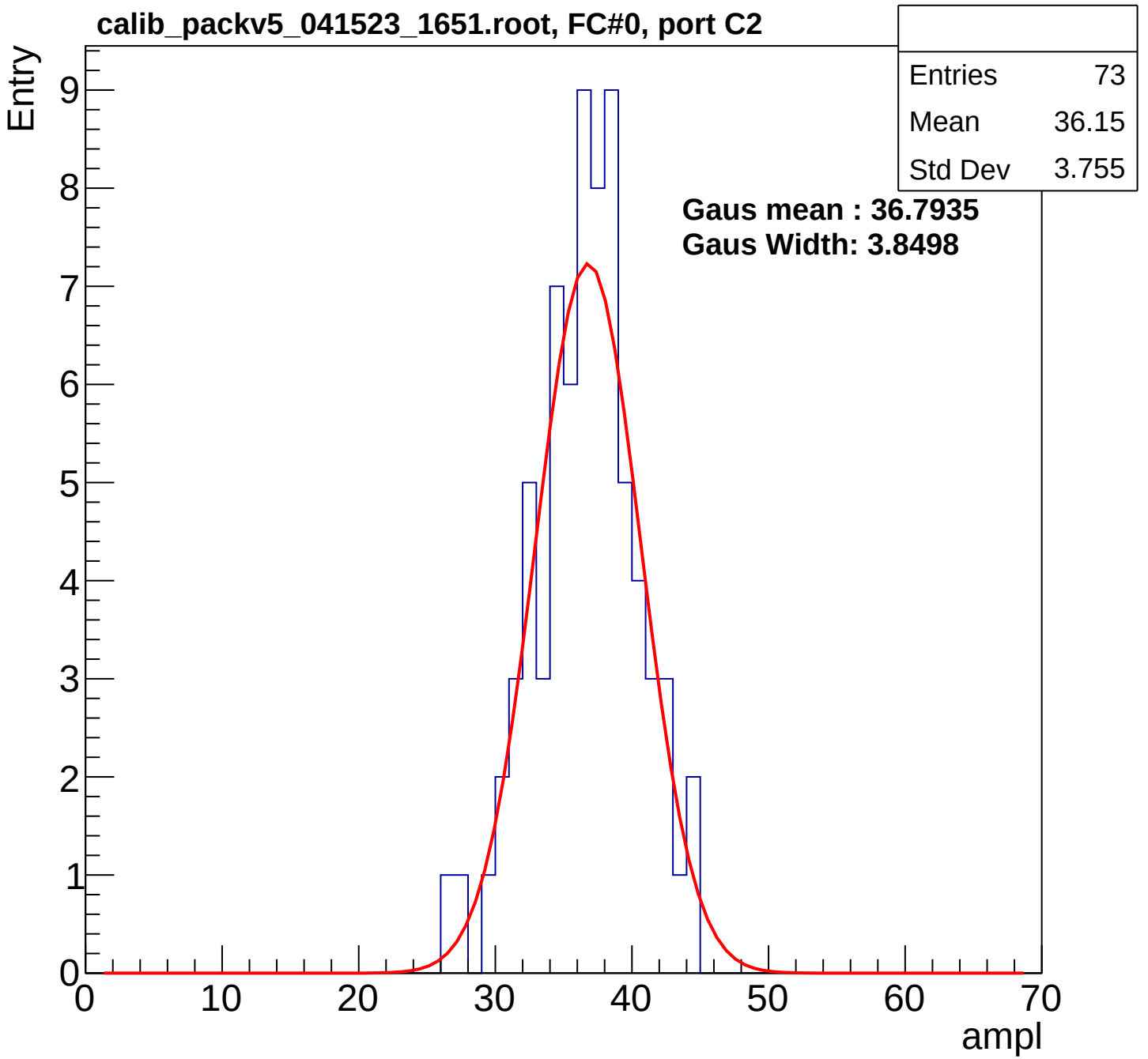
B1L103S, U5-ch4, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 36.15
Std Dev 3.755
Gaus mean : 36.7935
Gaus Width: 3.8498
Entry
ampl
0
10
20
30
40
50
60
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1
2
3
4
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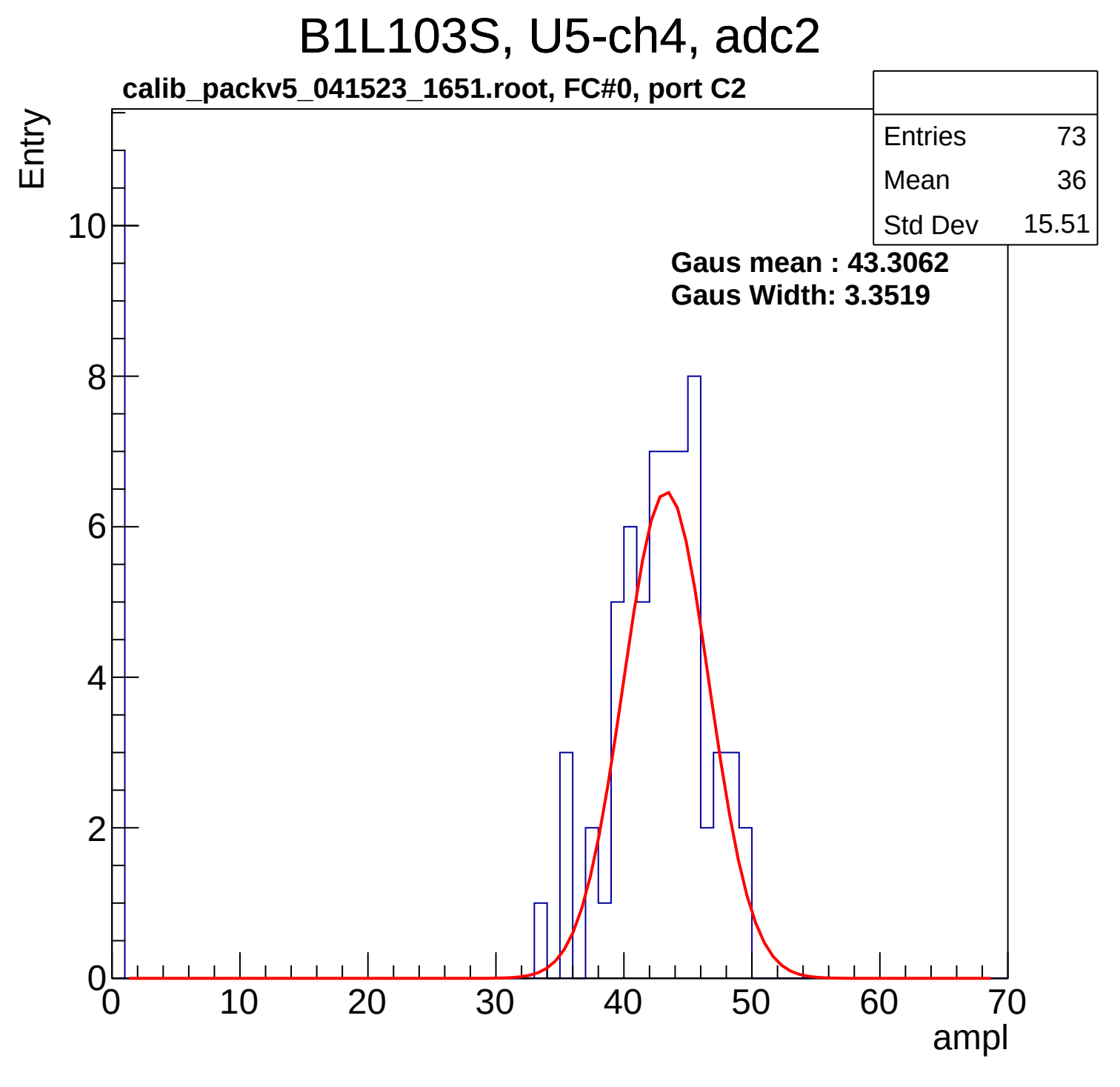
6
7
8
9


B1L103S, U5-ch4, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 36
Std Dev 15.51
Gaus mean : 43.3062
Gaus Width: 3.3519
Entry
ampl
0
2
4
6
8
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0
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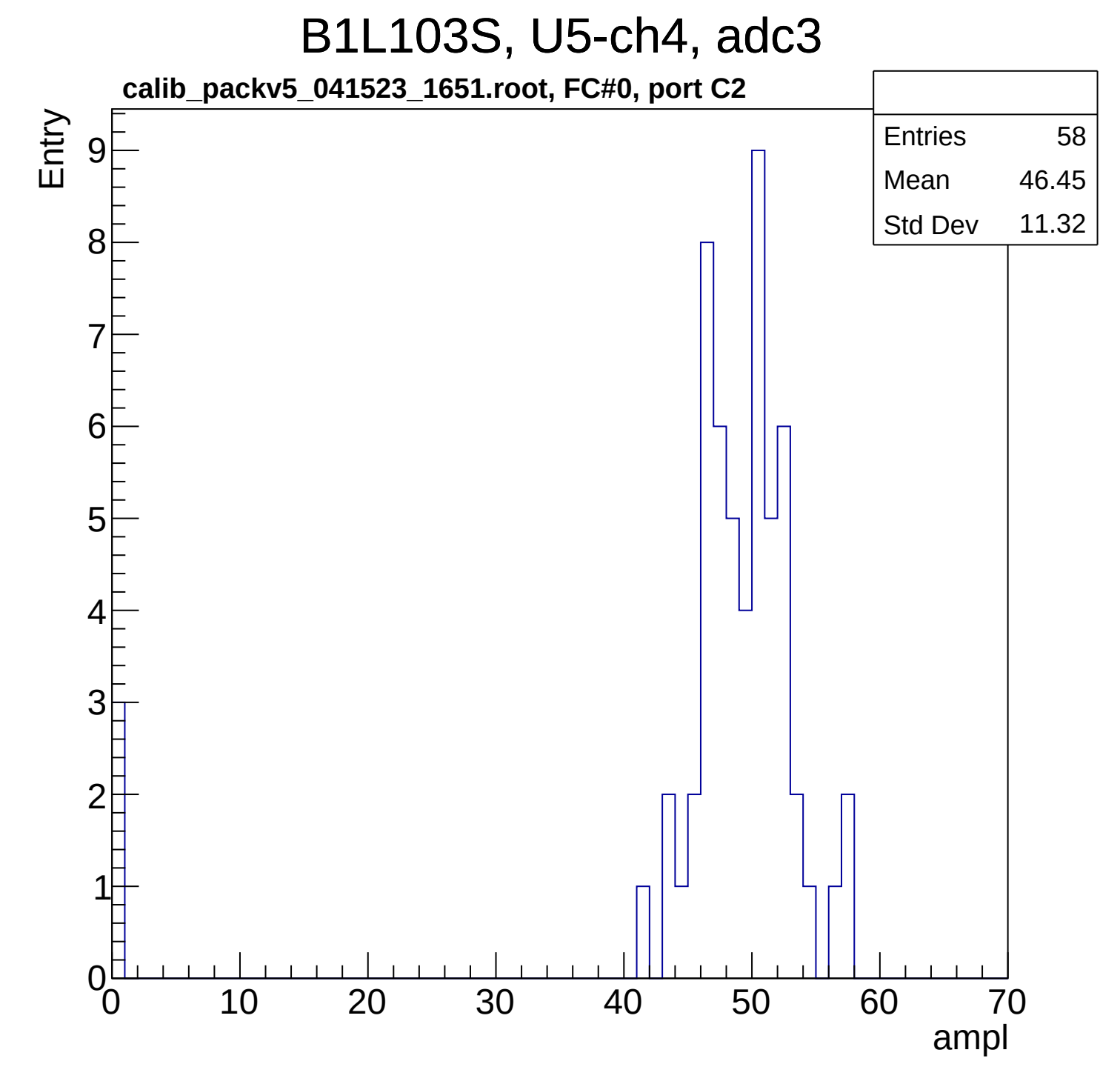
B1L103S, U5-ch4, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 46.45
Std Dev 11.32
Entry
ampl
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1
2
3
4
5
6
7
8
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0
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60
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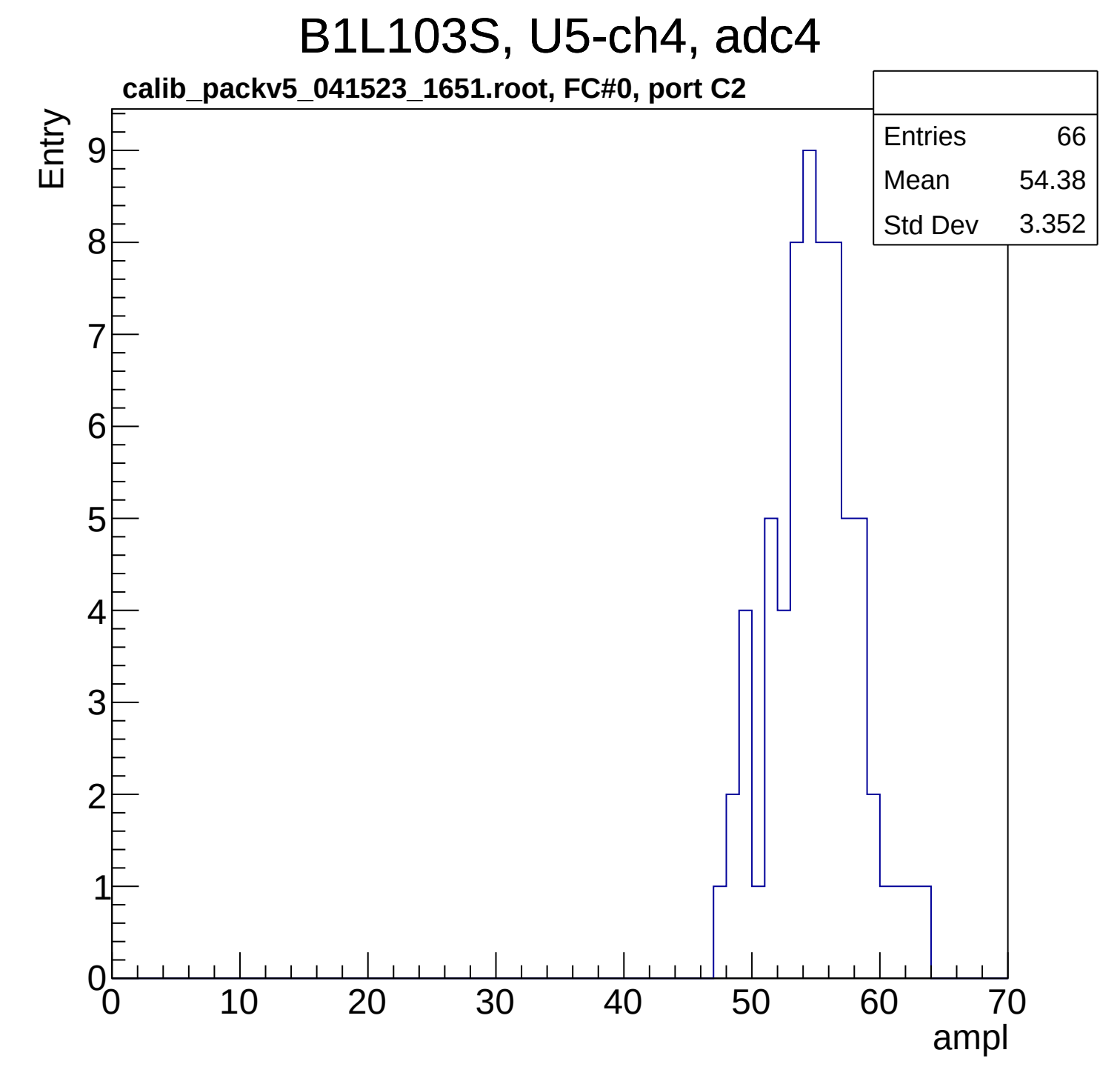
B1L103S, U5-ch4, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 54.38
Std Dev 3.352
Entry
ampl
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2
3
4
5
6
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0
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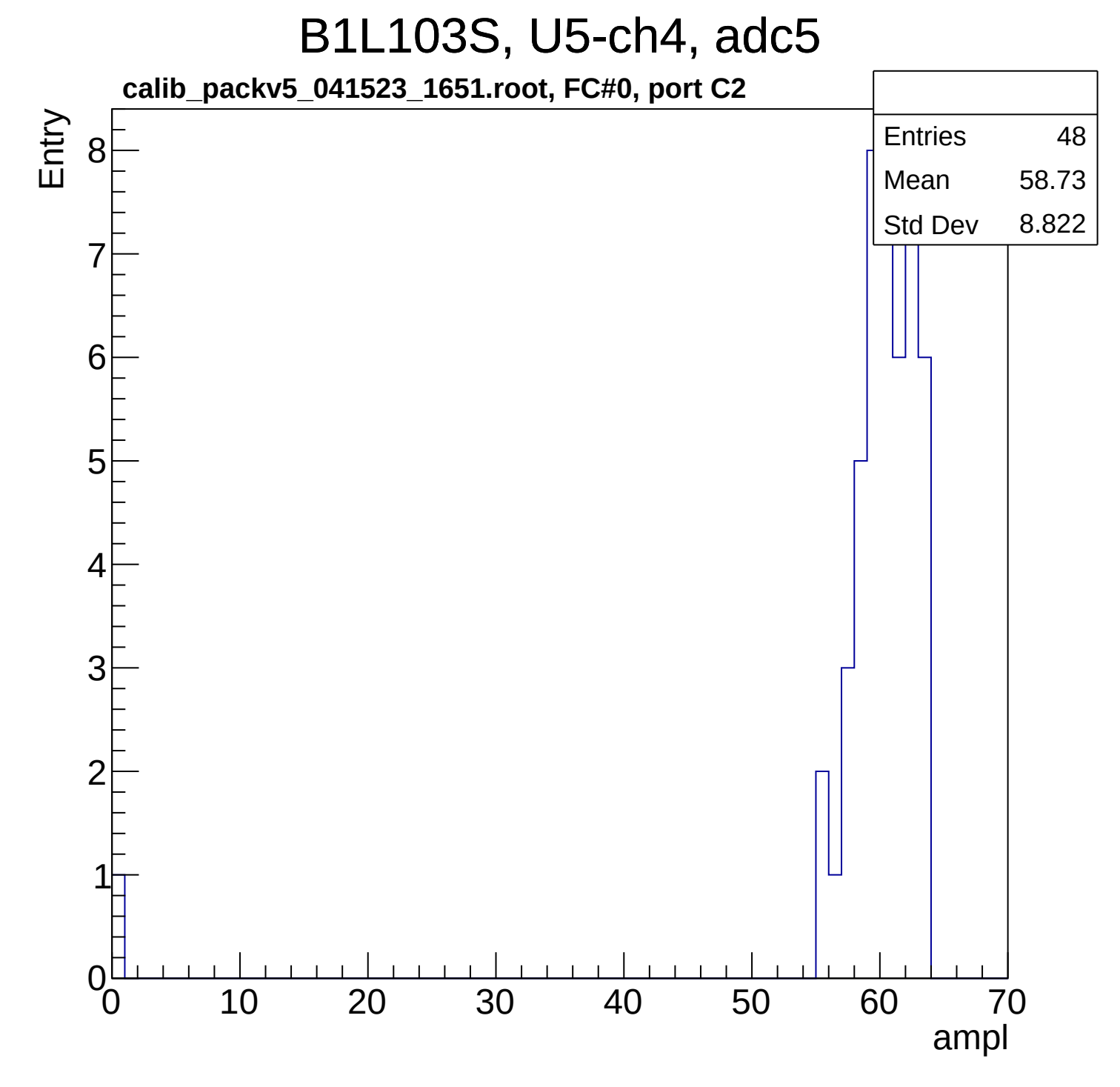
B1L103S, U5-ch4, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.73
Std Dev 8.822
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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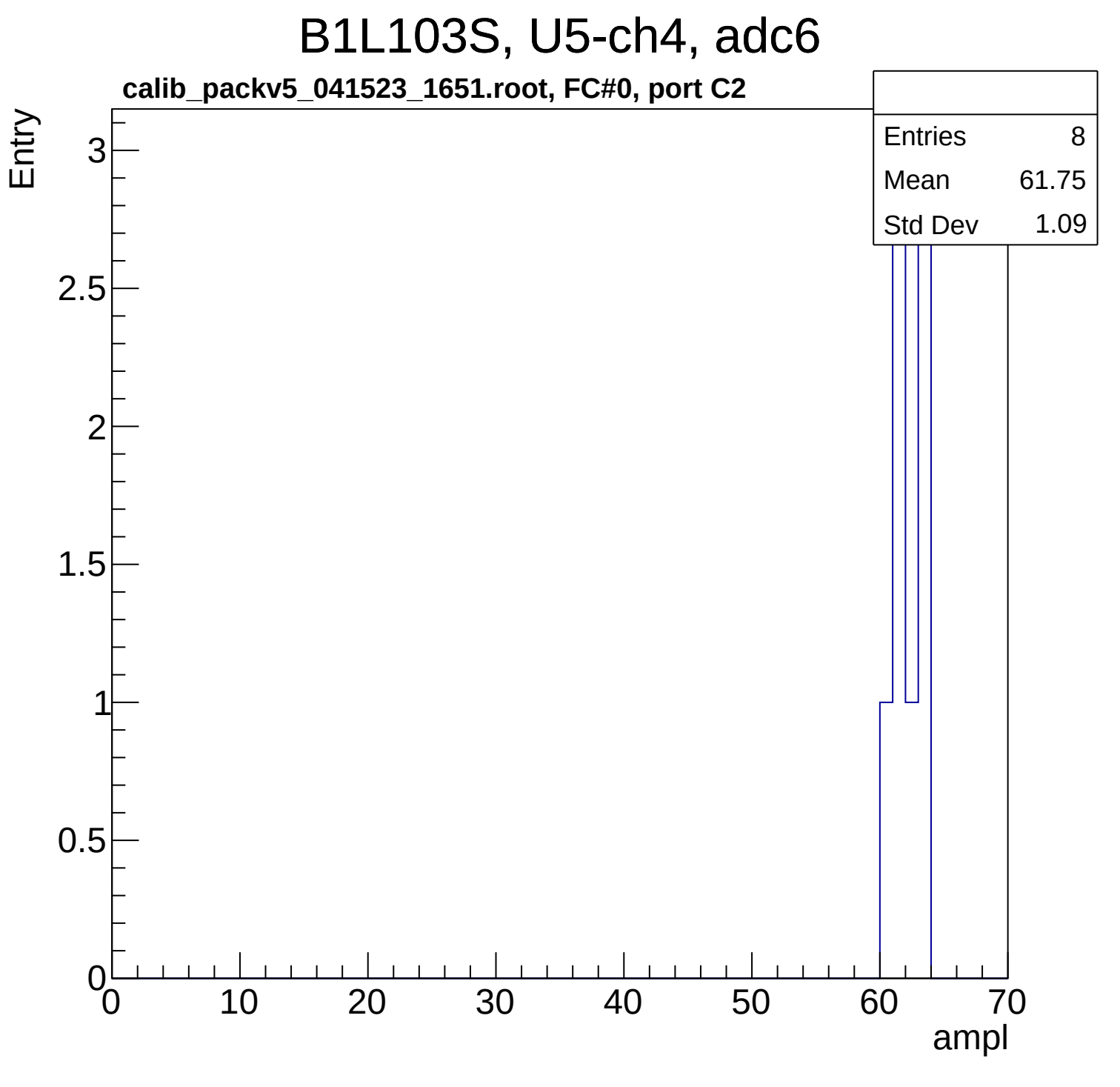
B1L103S, U5-ch4, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.75
Std Dev 1.09
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
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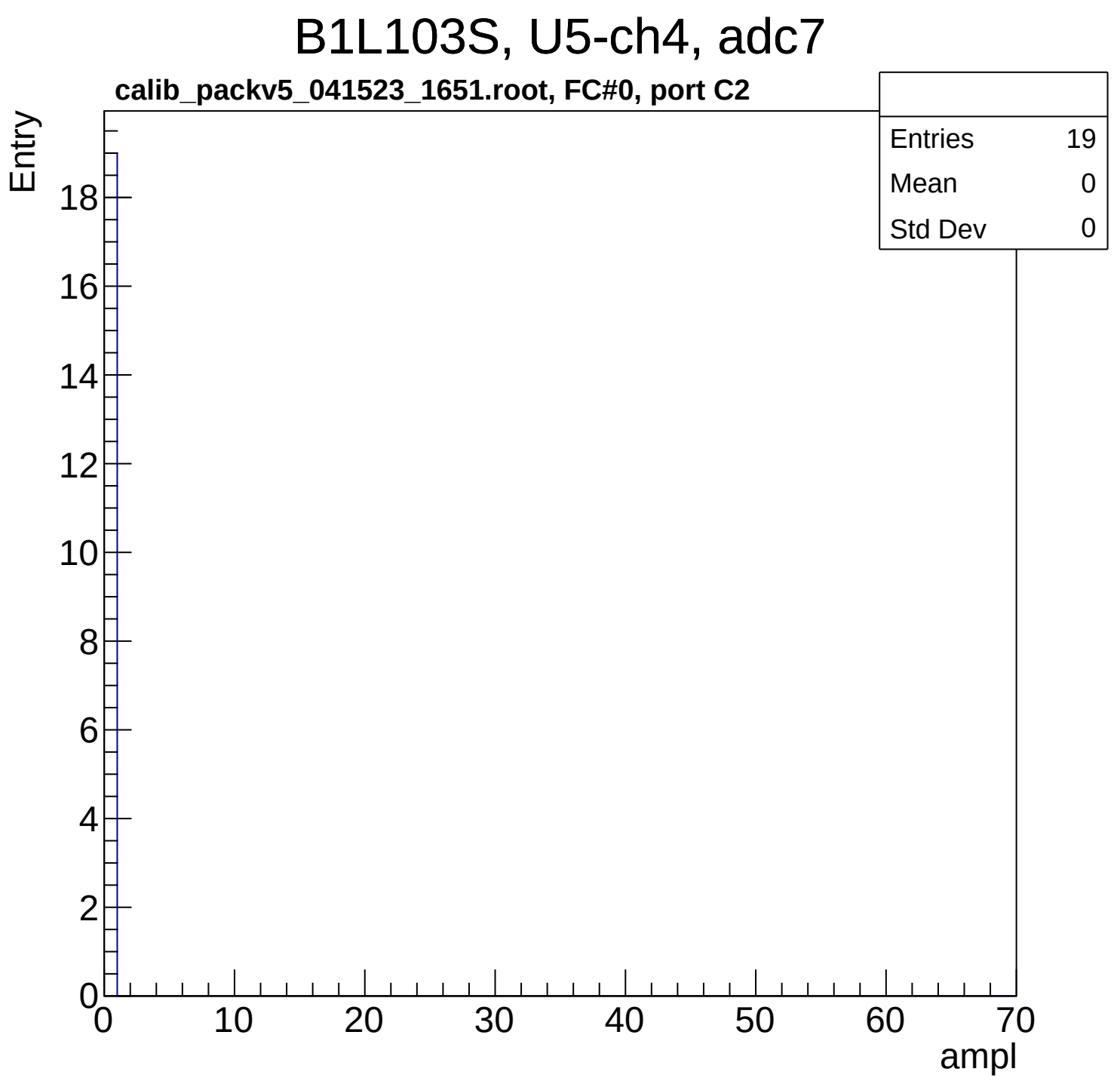
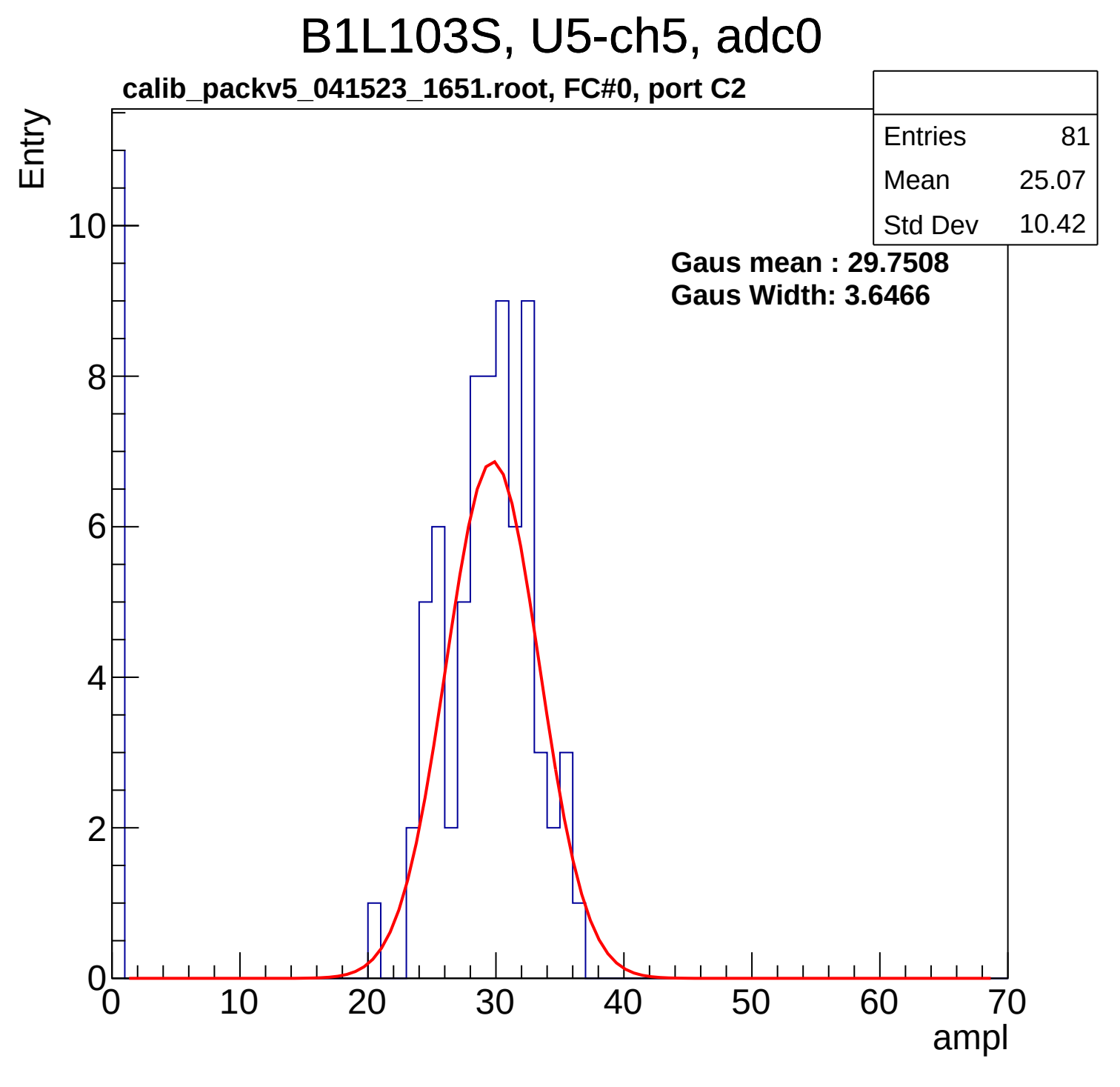
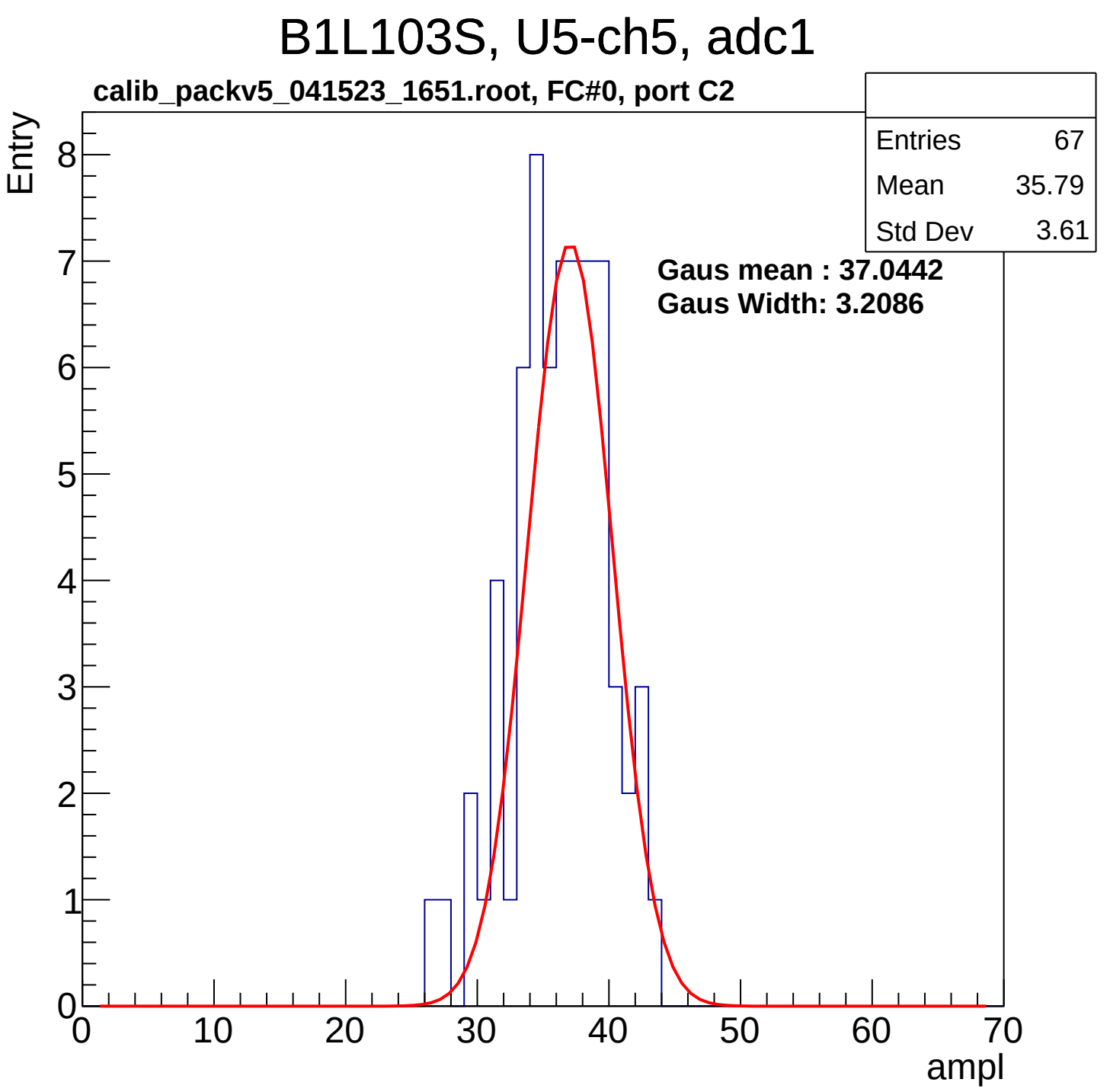

B1L103S, U5-ch4, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch5, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 25.07
Std Dev 10.42
Gaus mean : 29.7508
Gaus Width: 3.6466
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U5-ch5, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 35.79
Std Dev 3.61
Gaus mean : 37.0442
Gaus Width: 3.2086
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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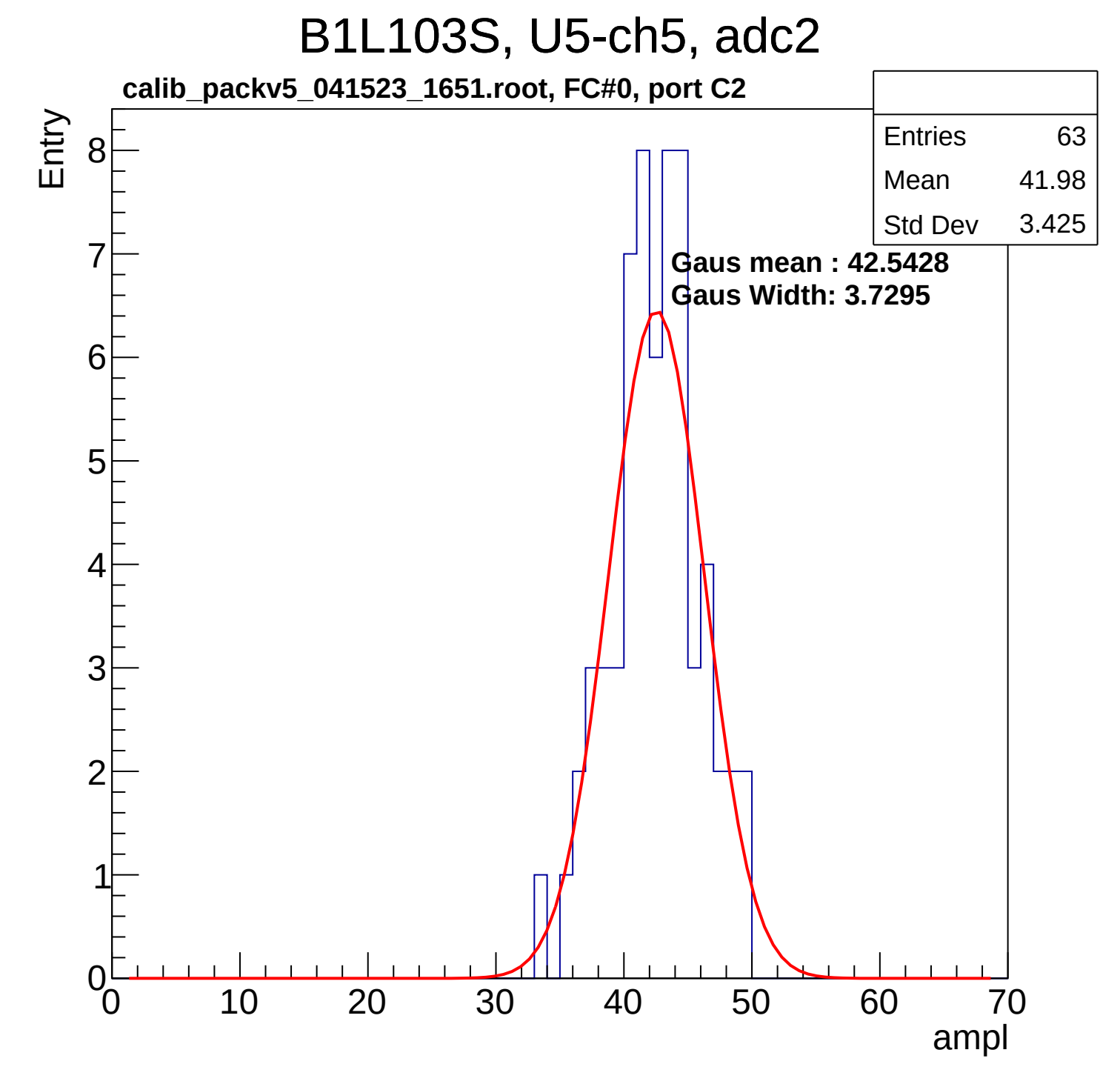
B1L103S, U5-ch5, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 41.98
Std Dev 3.425
Gaus mean : 42.5428
Gaus Width: 3.7295
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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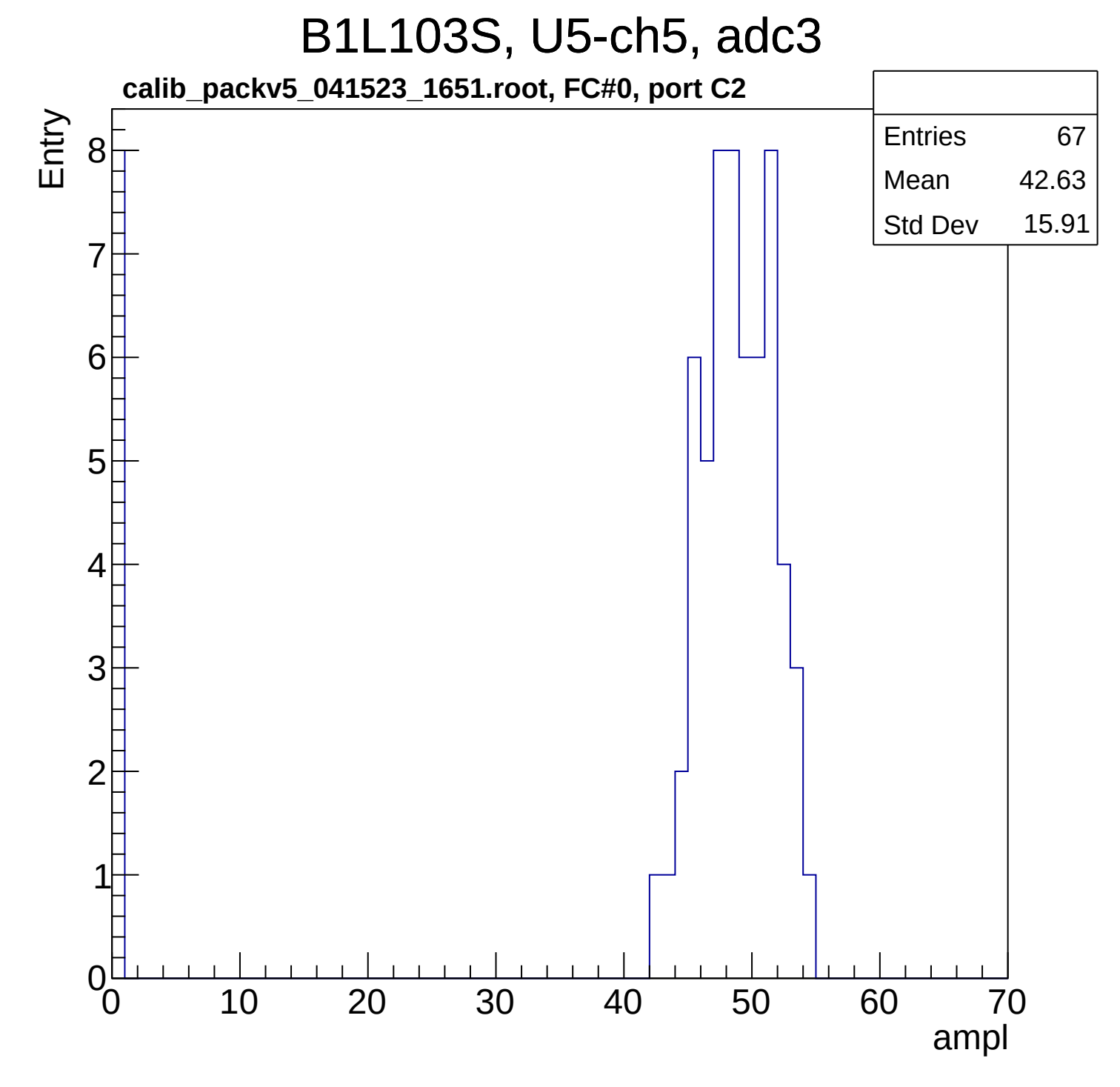
B1L103S, U5-ch5, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 42.63
Std Dev 15.91
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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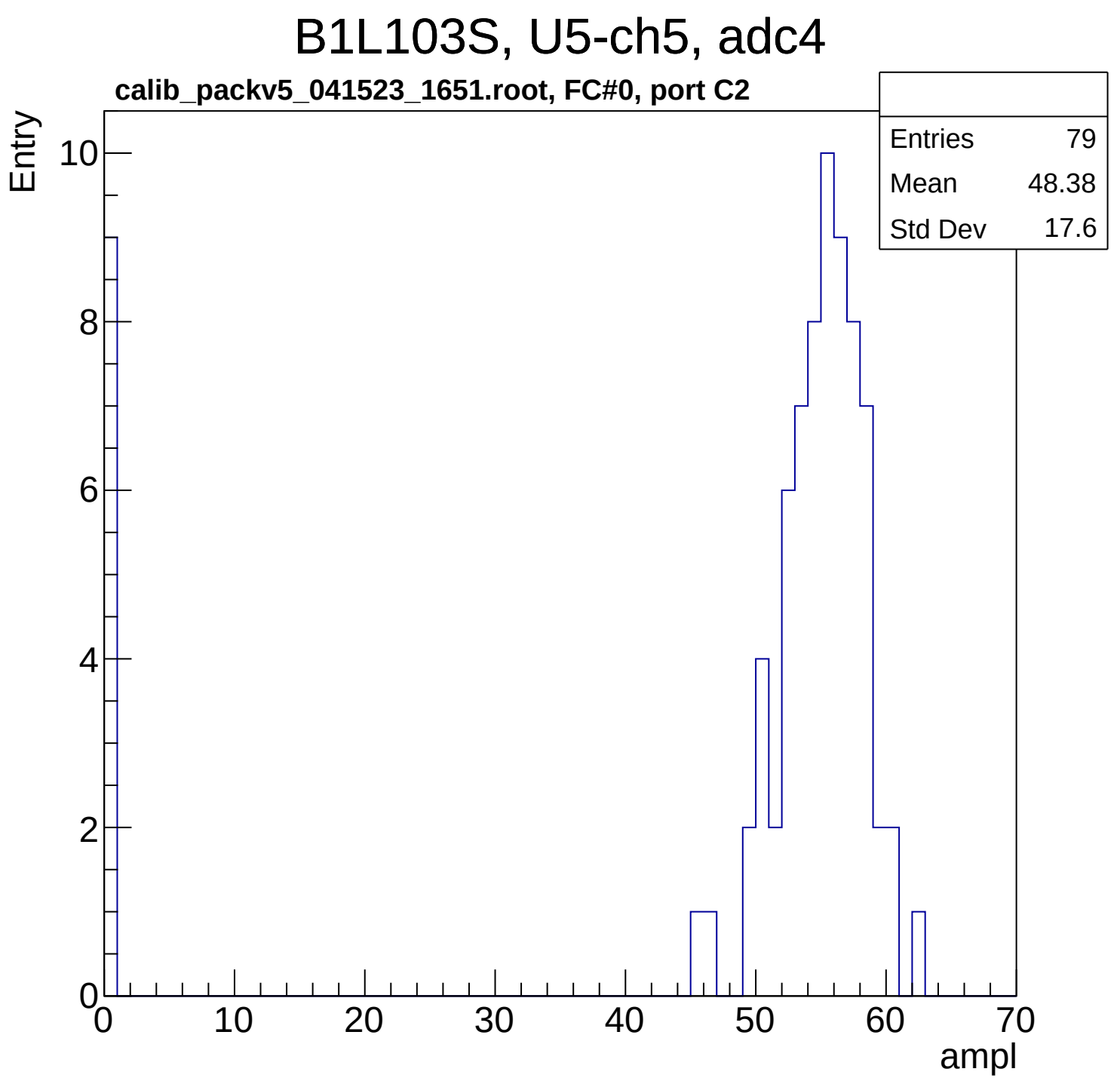
B1L103S, U5-ch5, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 48.38
Std Dev 17.6
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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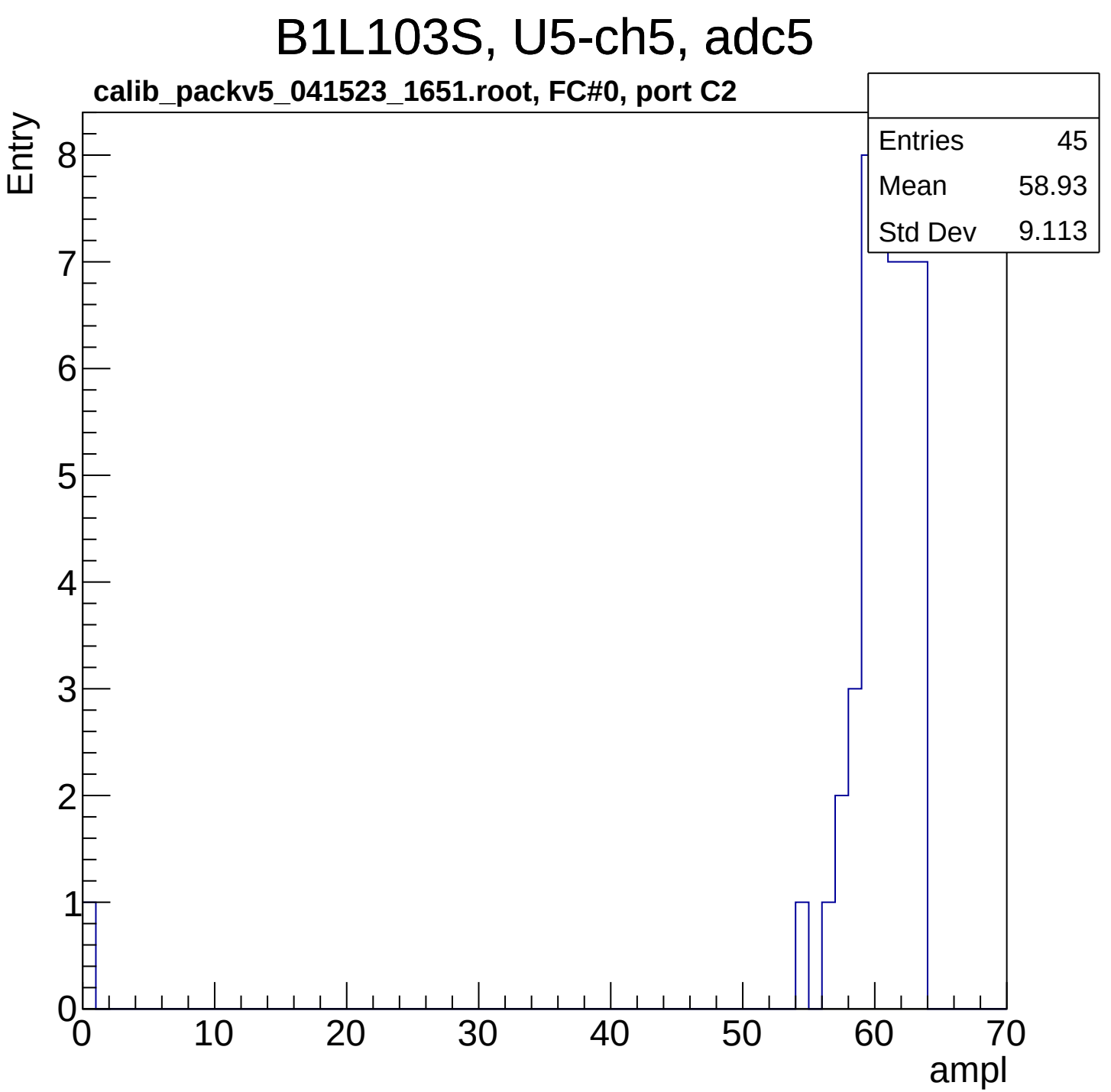
B1L103S, U5-ch5, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.93
Std Dev 9.113
Entry
ampl
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2
3
4
5
6
7
8
0
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20
30
40
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60
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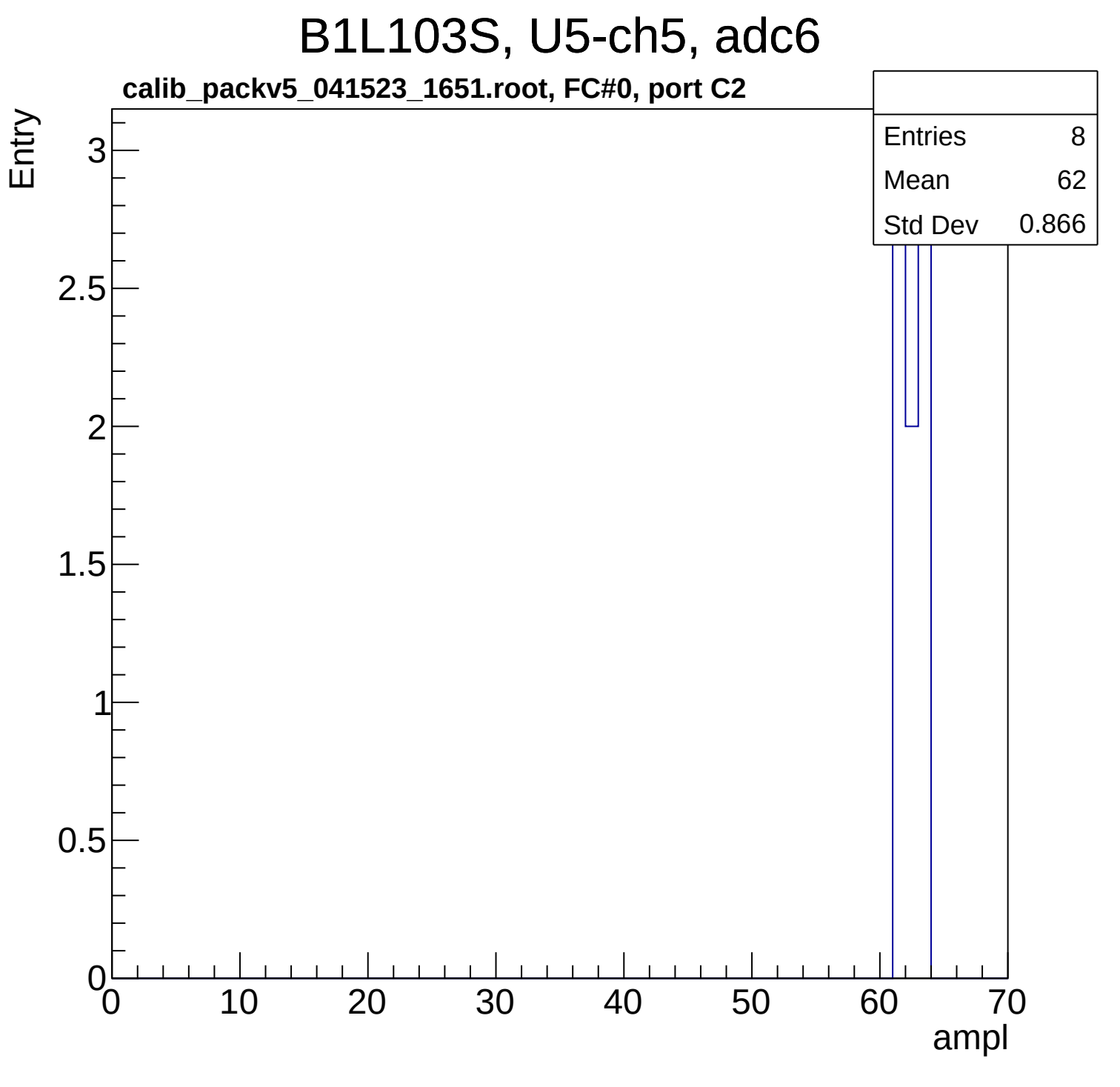
B1L103S, U5-ch5, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62
Std Dev 0.866
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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60
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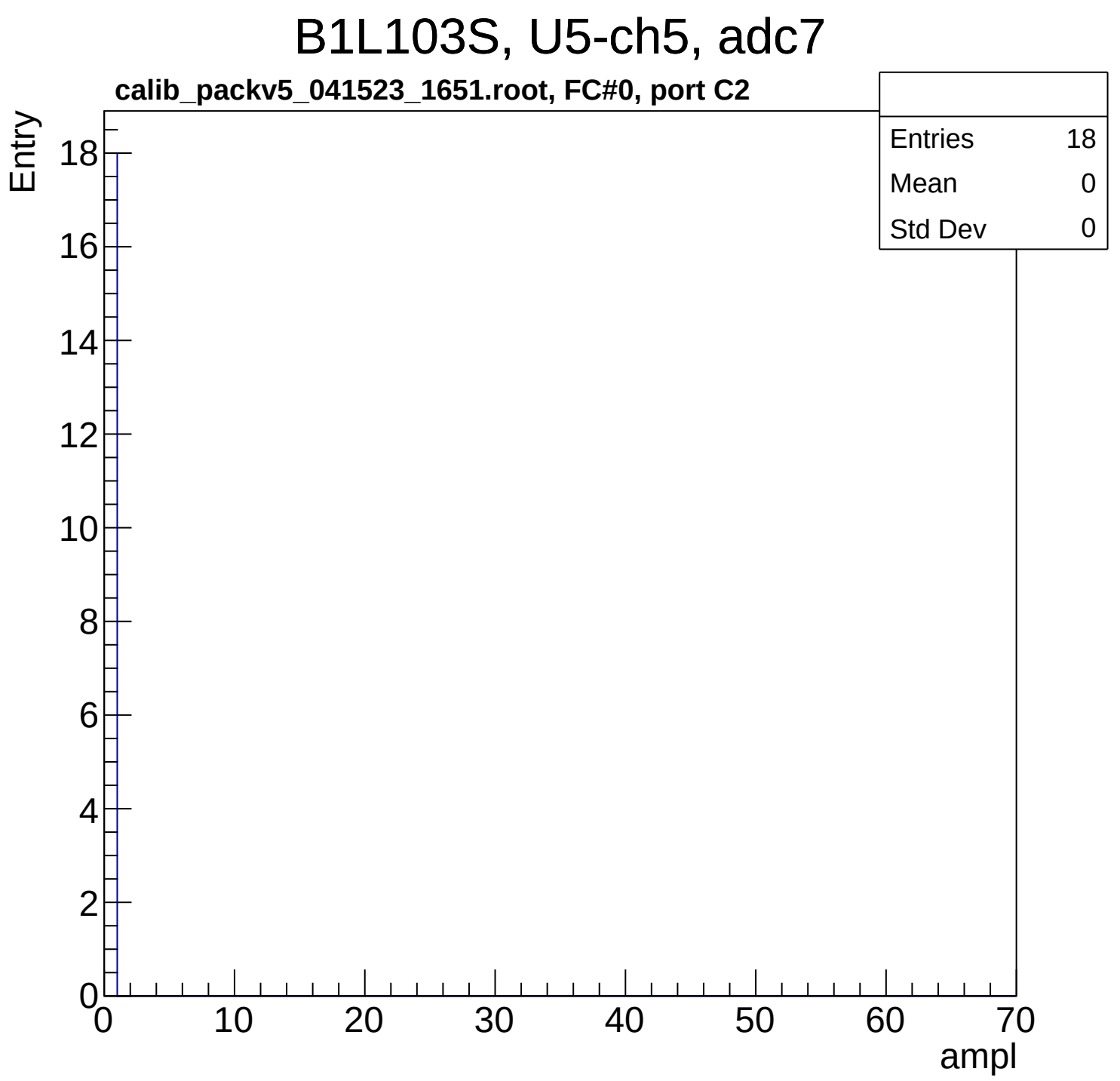
B1L103S, U5-ch5, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
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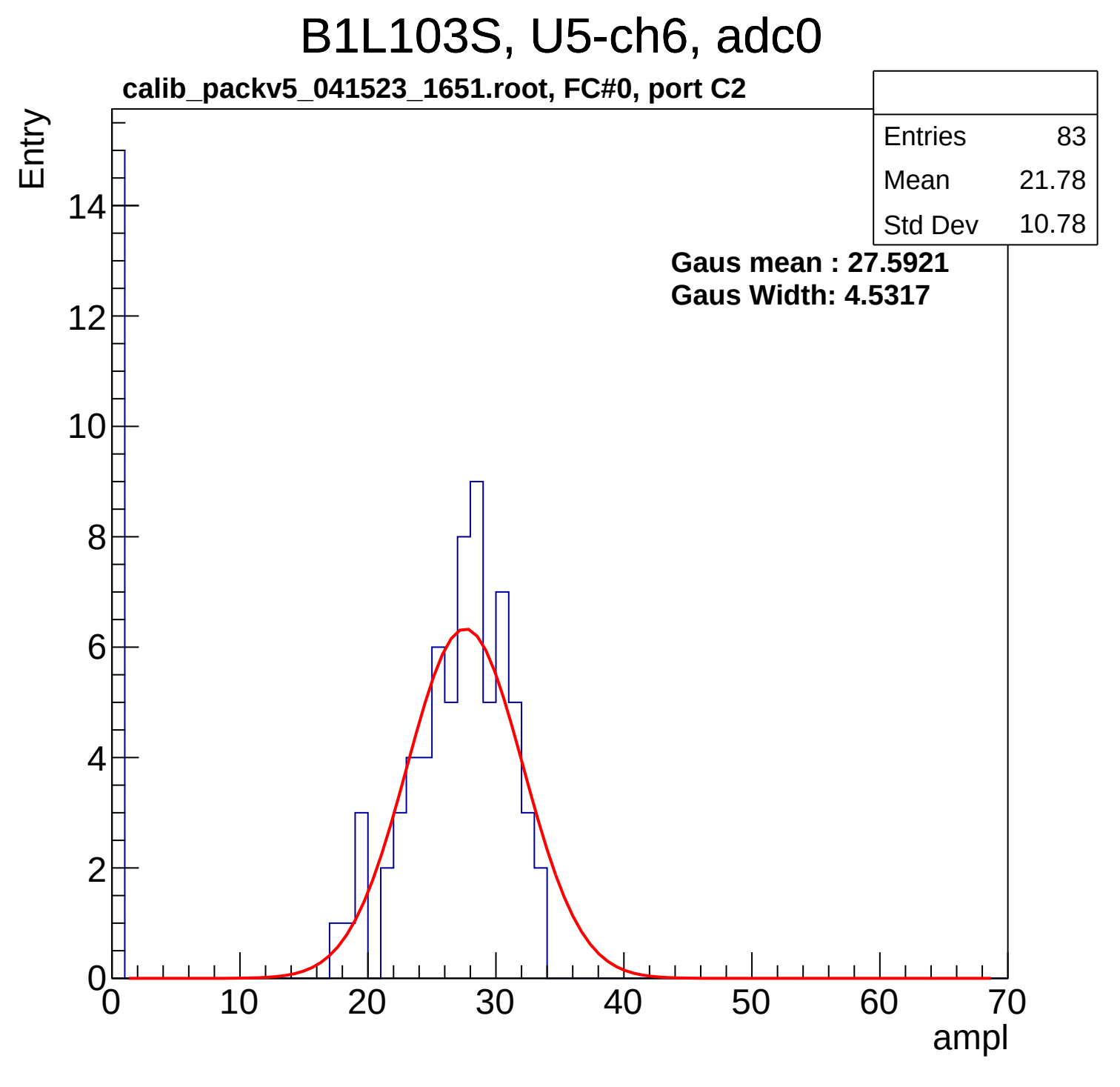
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch6, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 21.78
Std Dev 10.78
Gaus mean : 27.5921
Gaus Width: 4.5317
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
50
60
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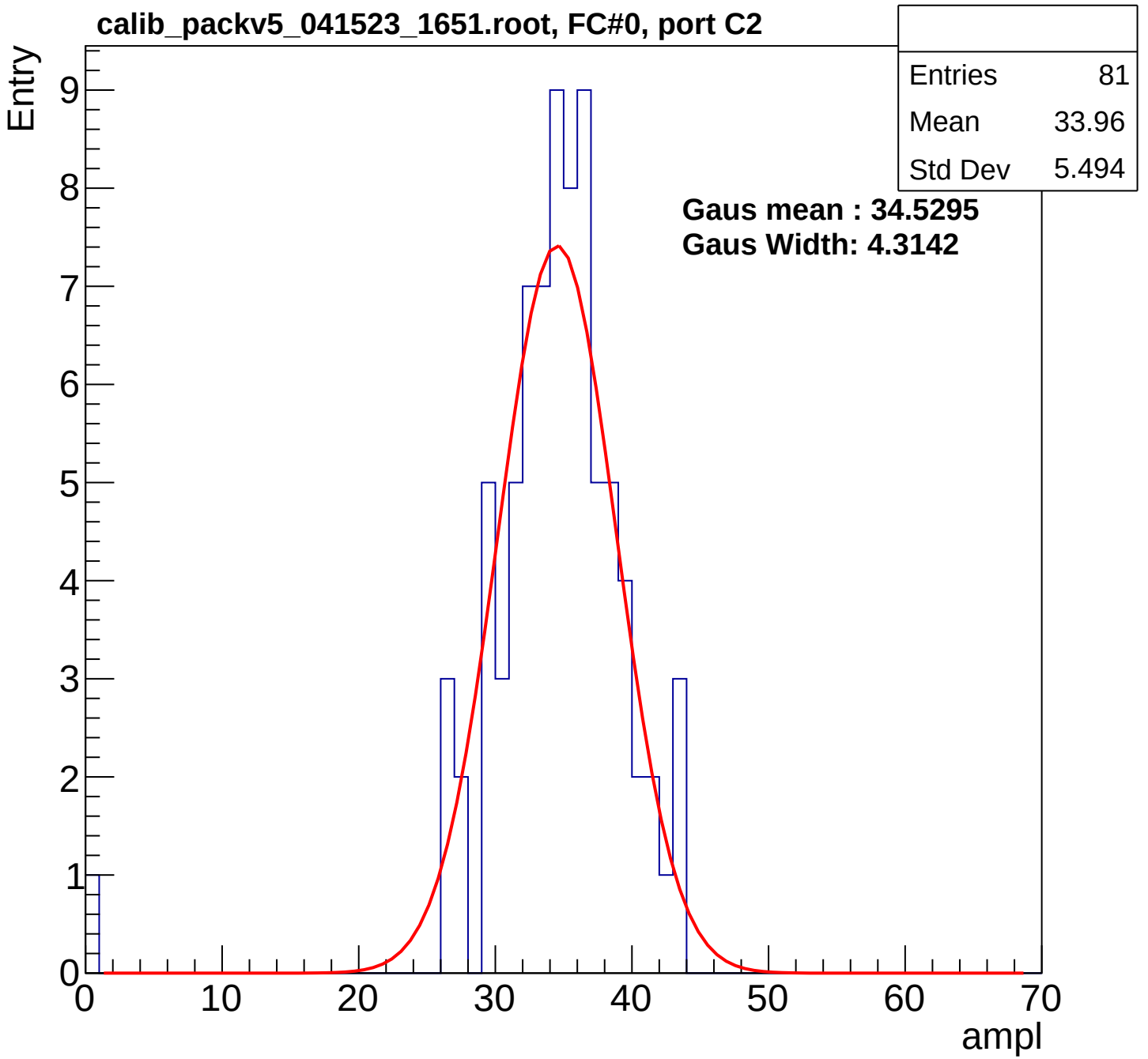
B1L103S, U5-ch6, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 33.96
Std Dev 5.494
Gaus mean : 34.5295
Gaus Width: 4.3142
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
30
40
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60
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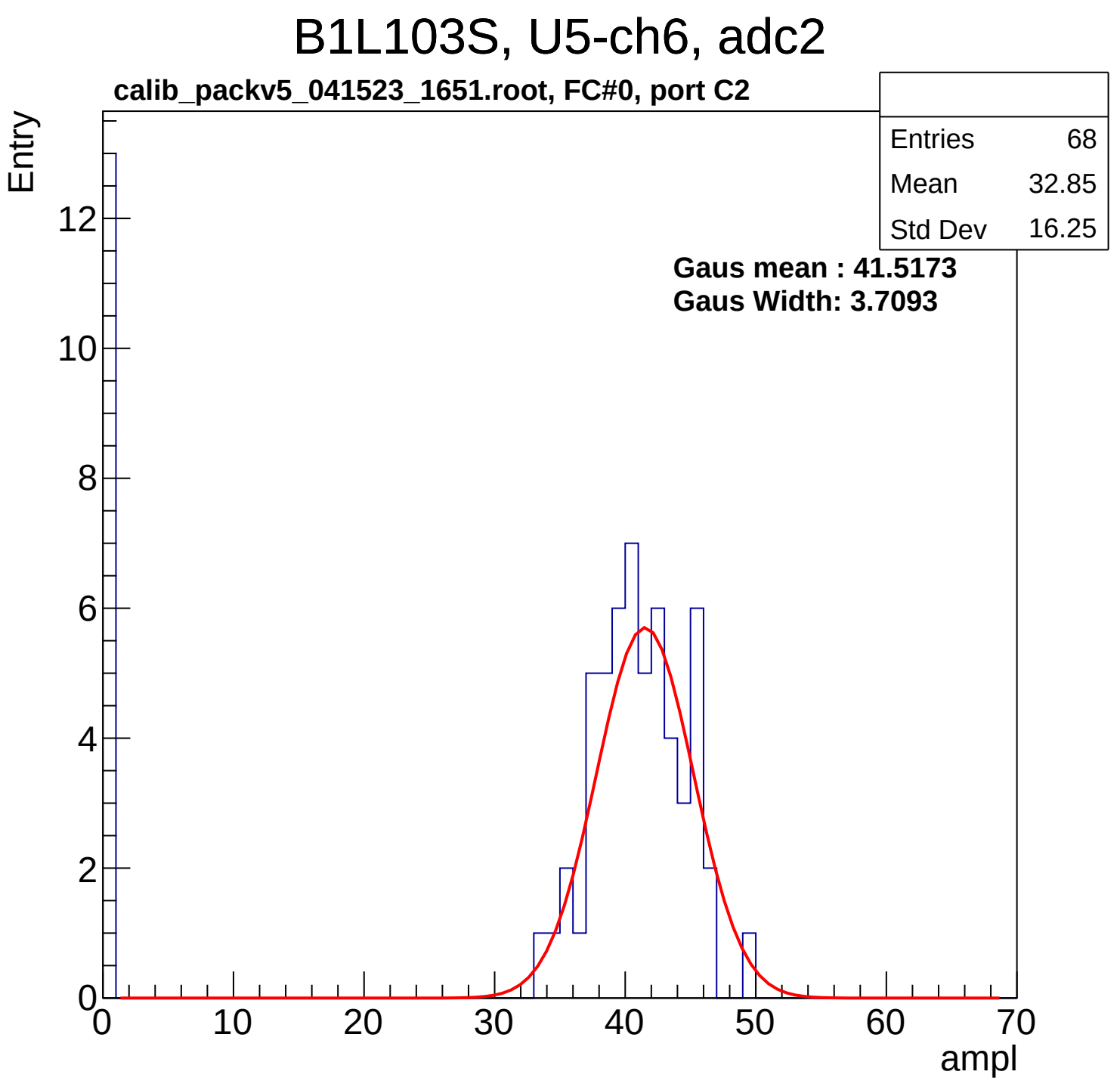
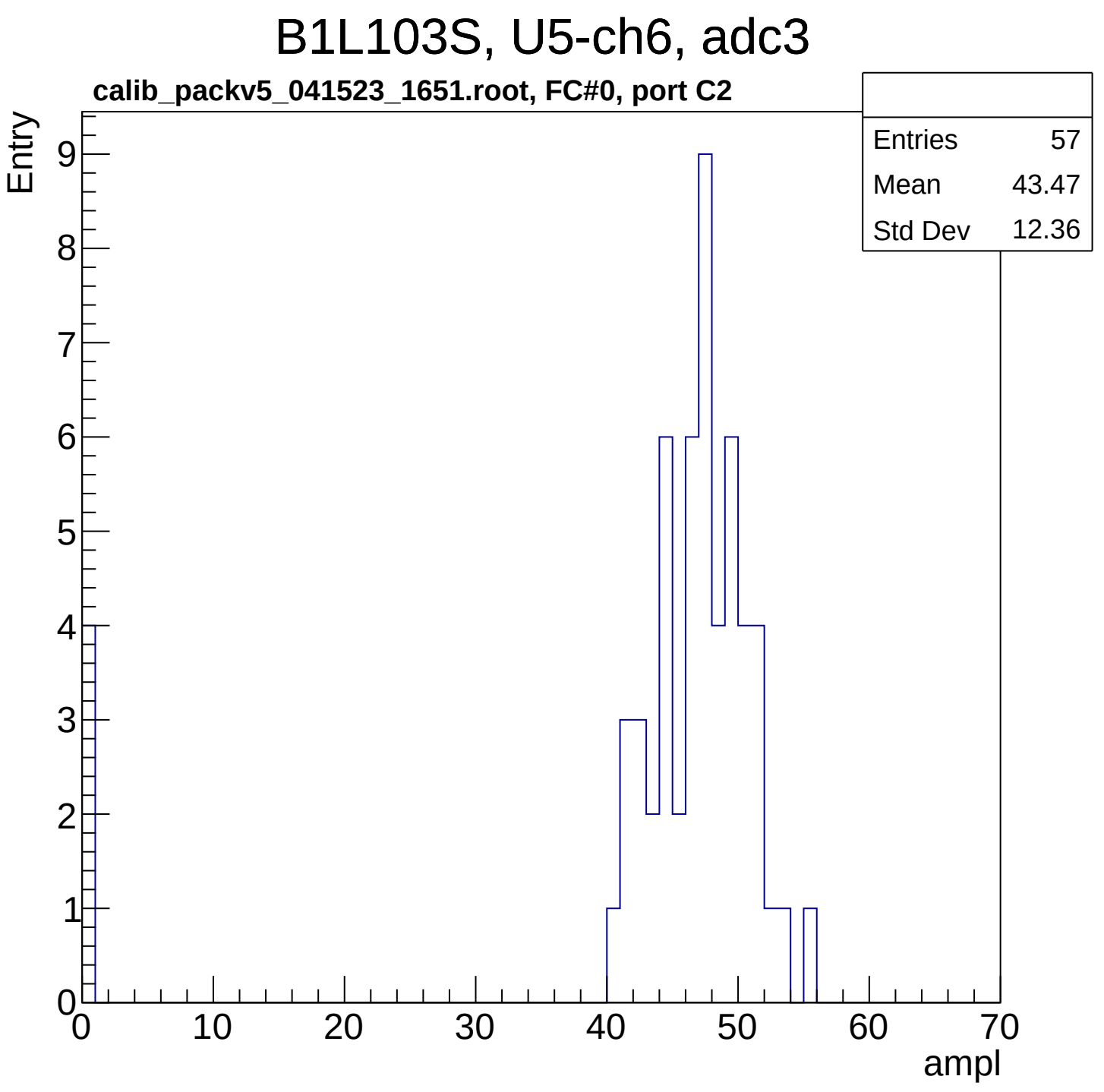

B1L103S, U5-ch6, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 32.85
Std Dev 16.25
Gaus mean : 41.5173
Gaus Width: 3.7093
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U5-ch6, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 43.47
Std Dev 12.36
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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60
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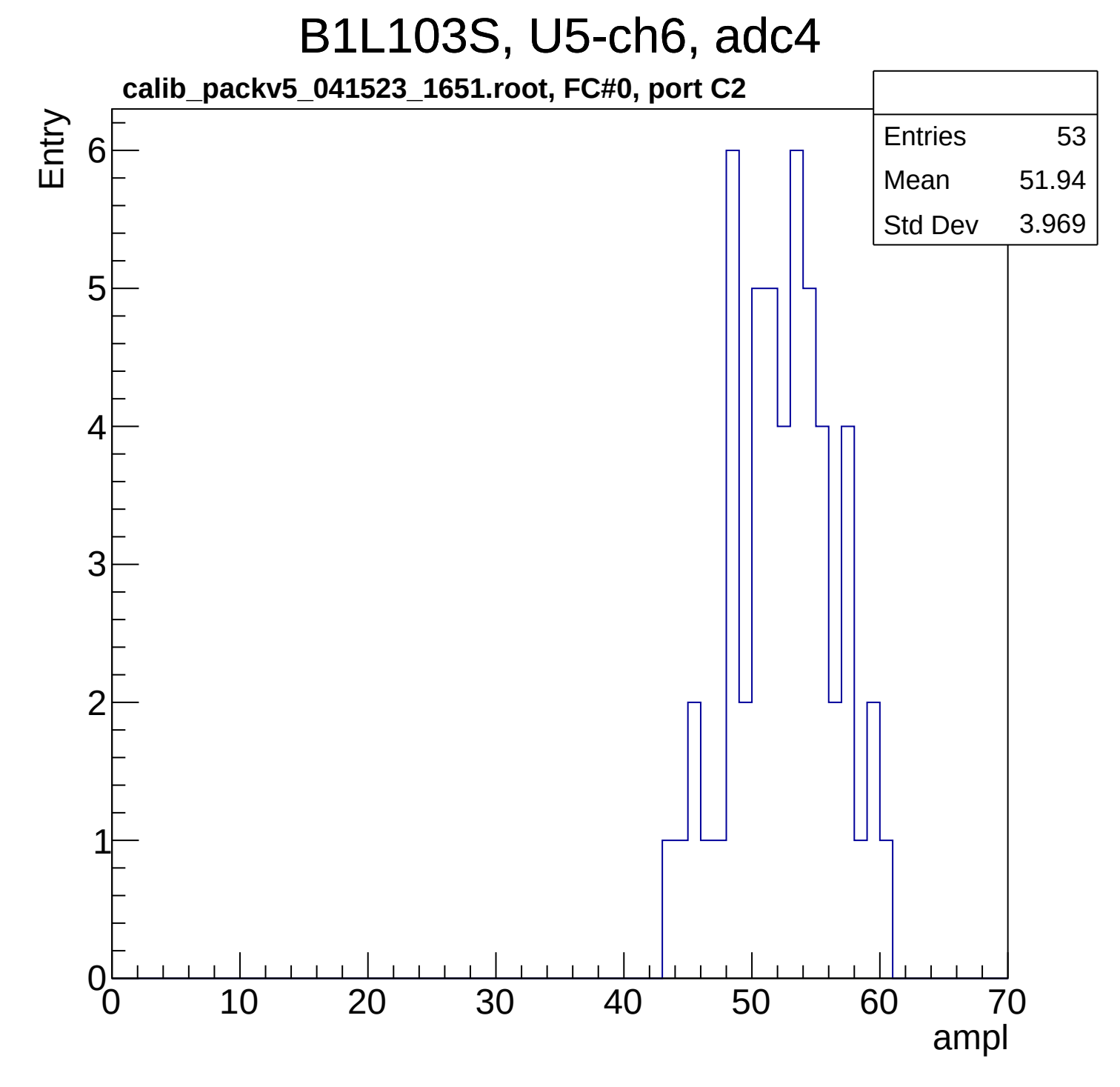
B1L103S, U5-ch6, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 51.94
Std Dev 3.969
Entry
ampl
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3
4
5
6
0
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60
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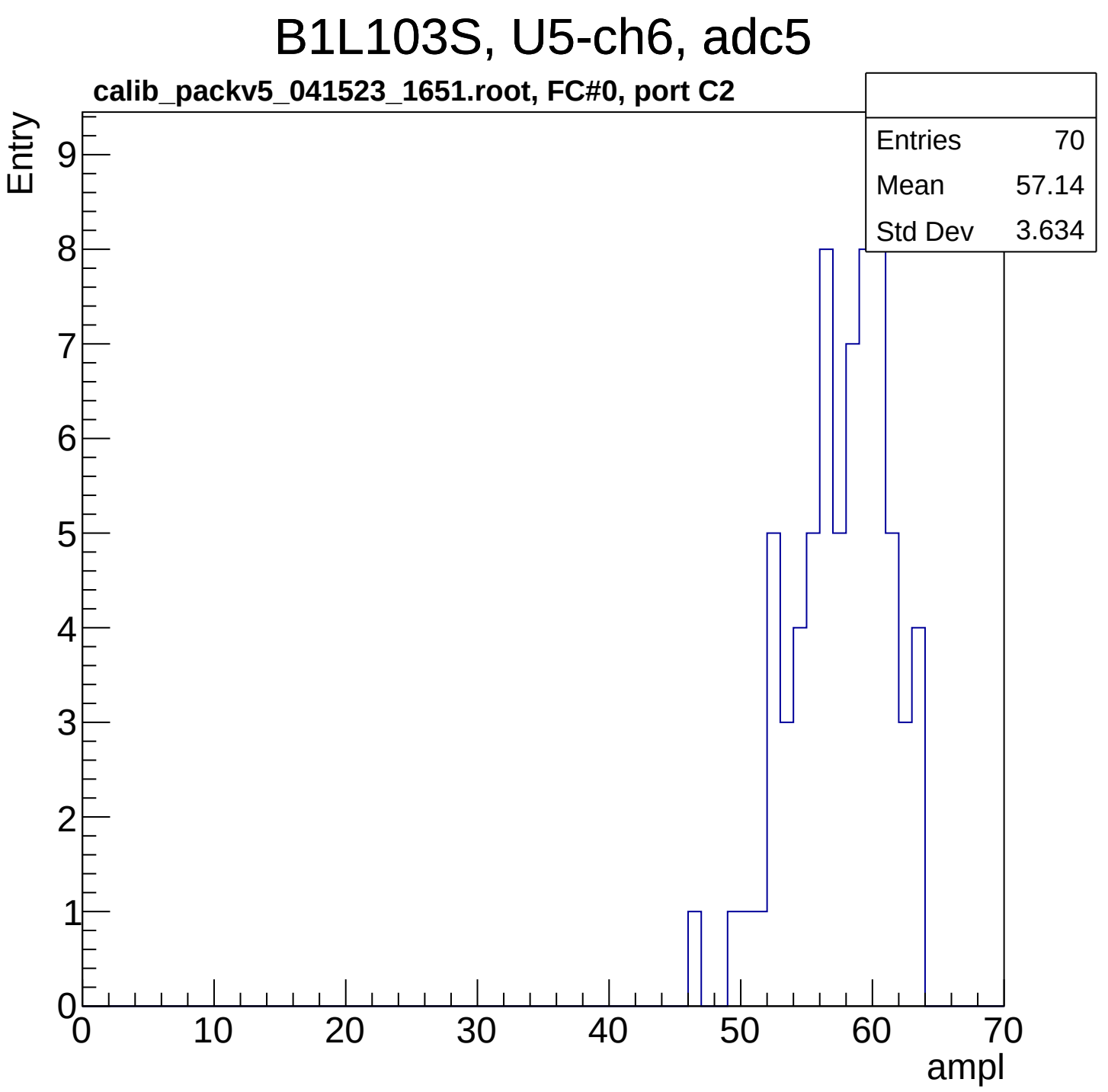
B1L103S, U5-ch6, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 57.14
Std Dev 3.634
Entry
ampl
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3
4
5
6
7
8
9
0
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20
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40
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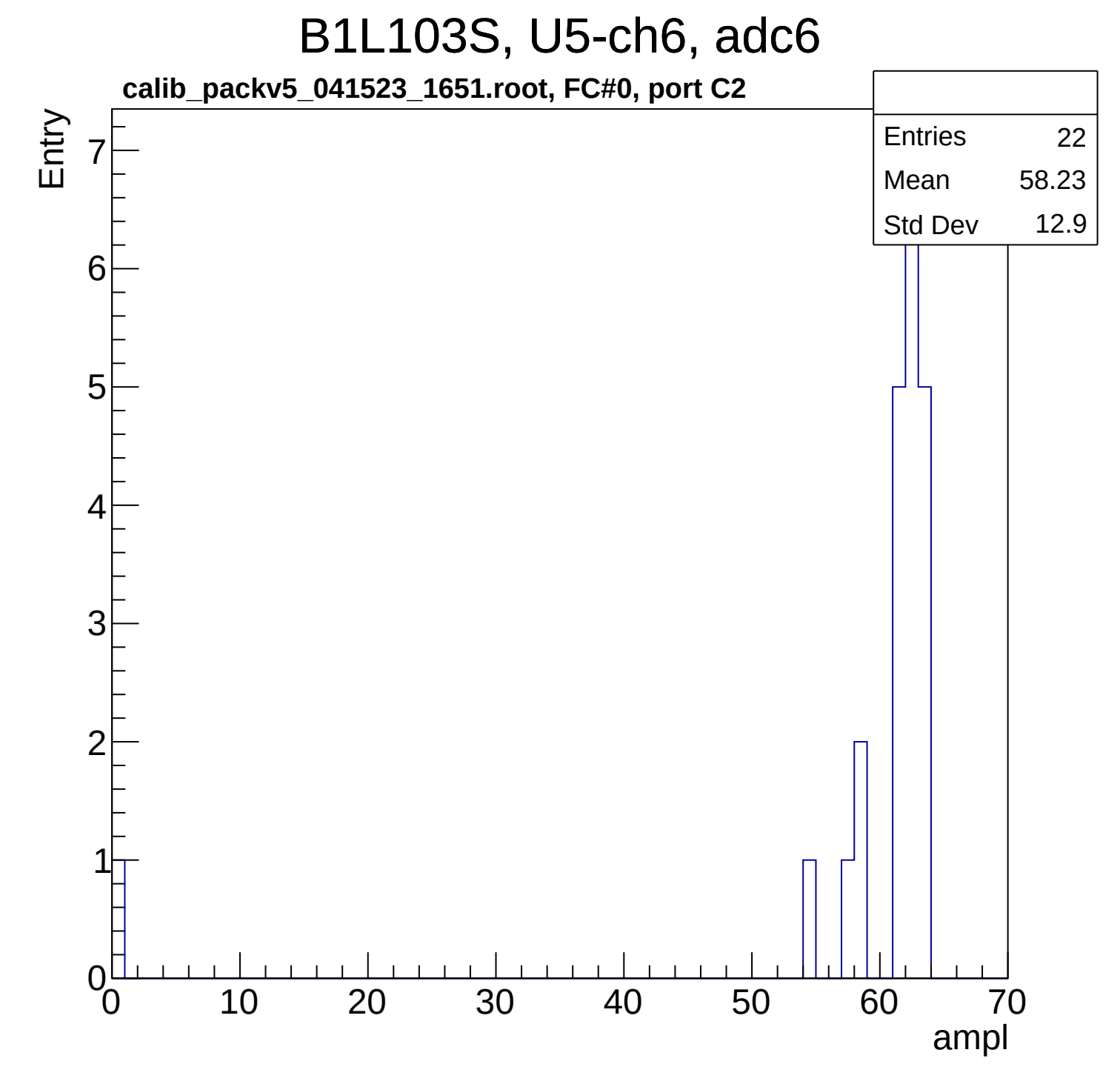
60
70


B1L103S, U5-ch6, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.23
Std Dev 12.9
Entry
ampl
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4
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0
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20
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40
50
60
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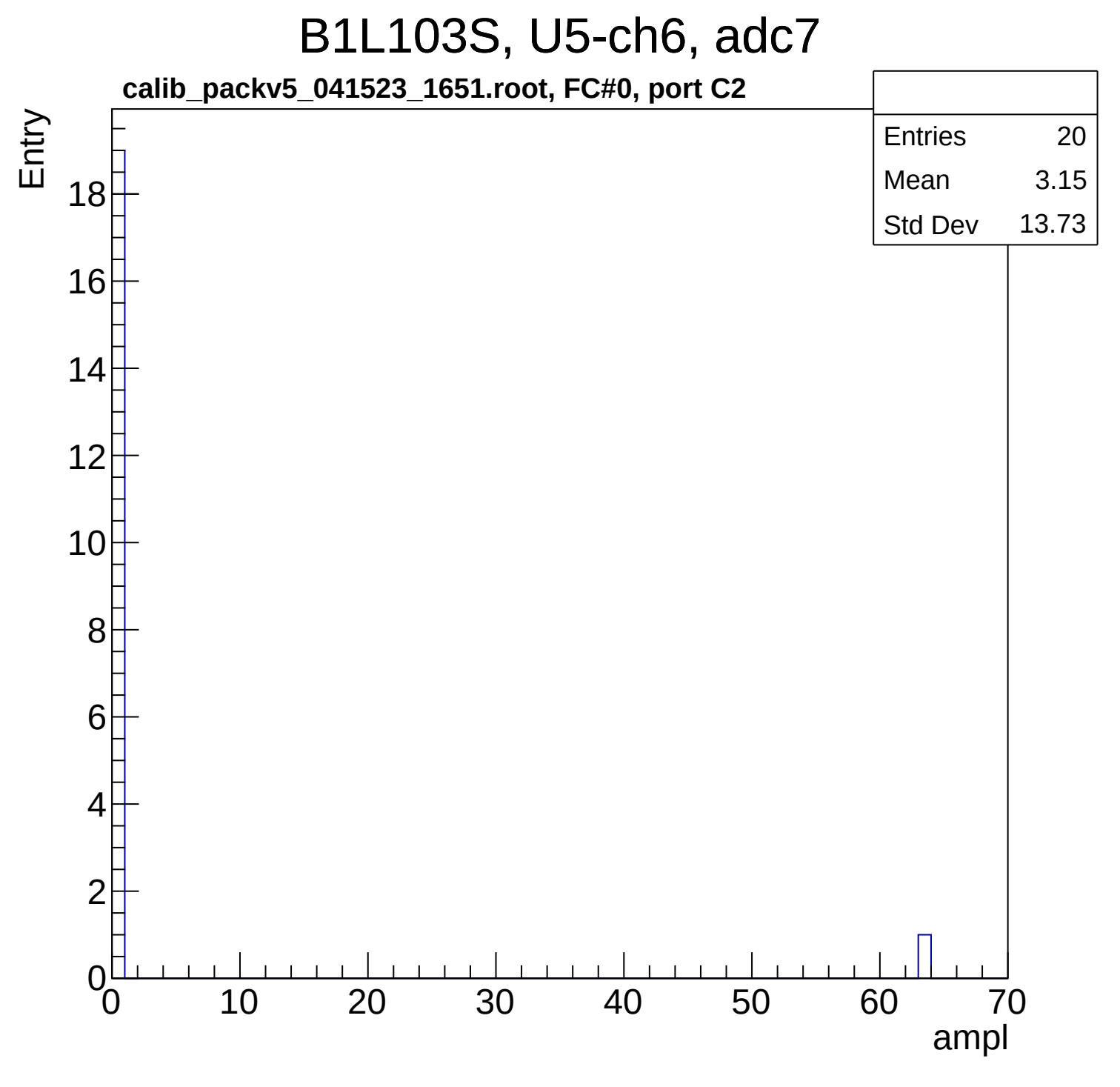
B1L103S, U5-ch6, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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6
8
10
12
14
16
18
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10
20
30
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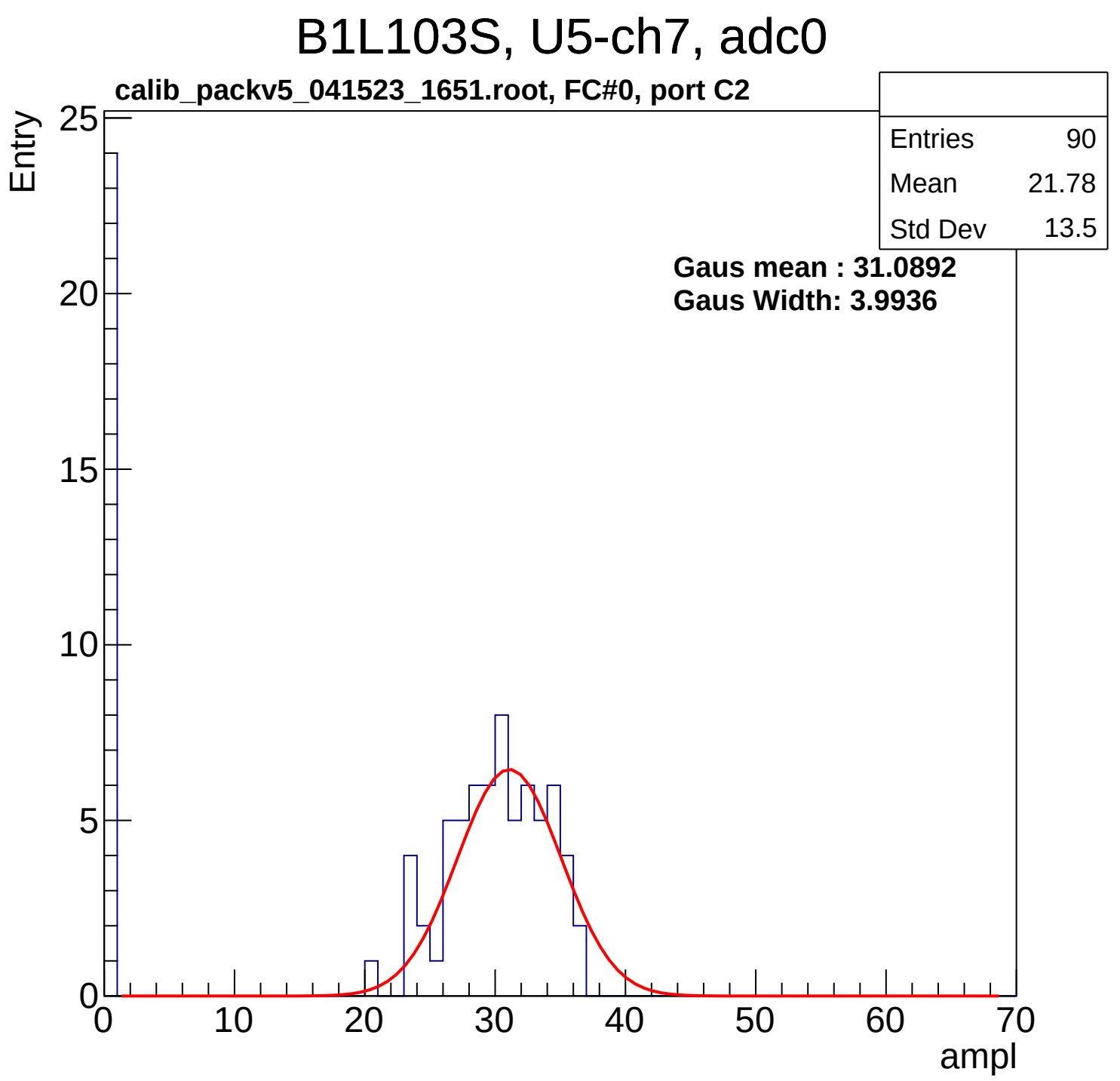
50
60
70
ampl


B1L103S, U5-ch7, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 21.78
Std Dev 13.5
Gaus mean : 31.0892
Gaus Width: 3.9936
Entry
ampl
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5
10
15
20
25
0
10
20
30
40
50
60
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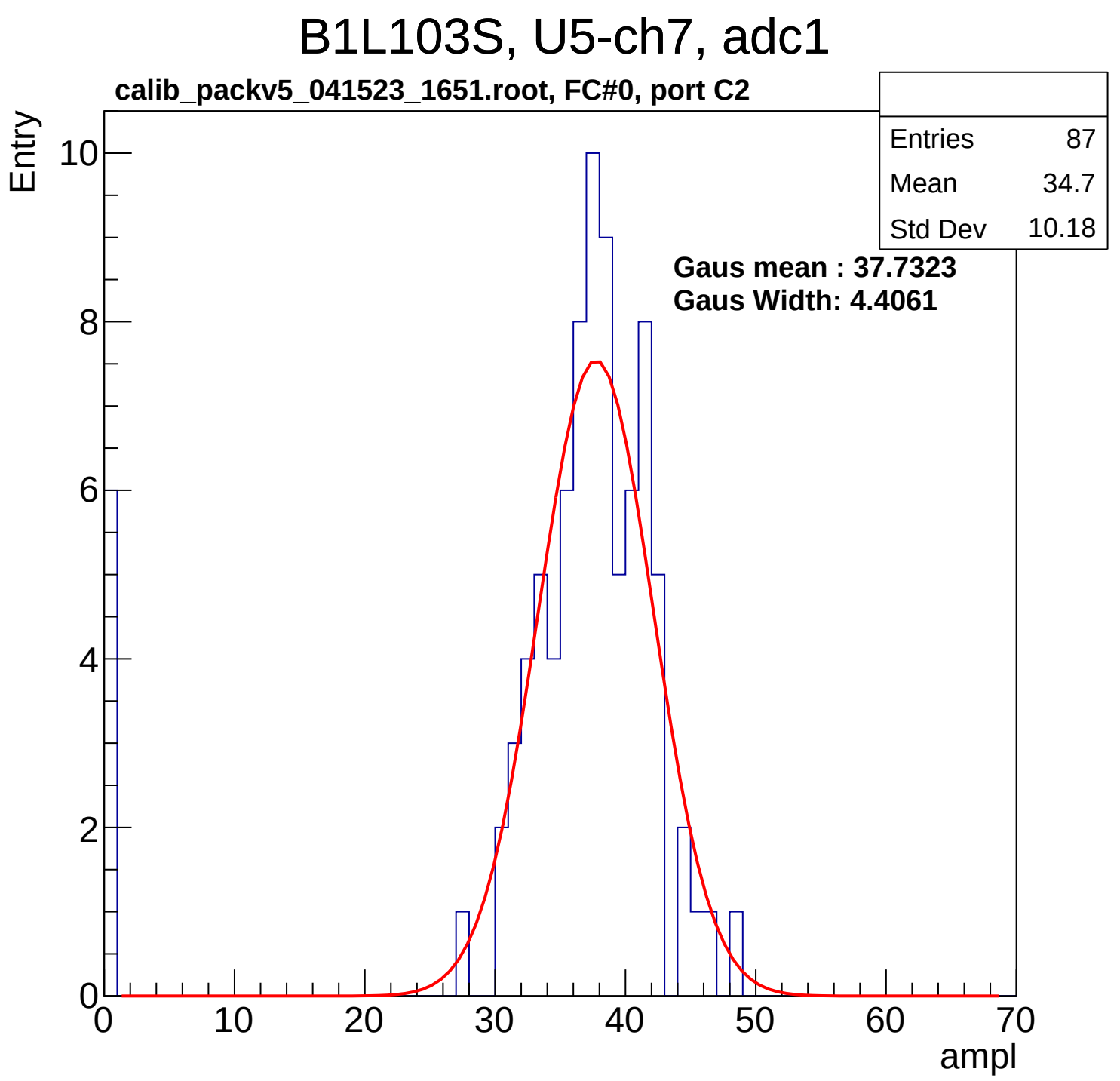
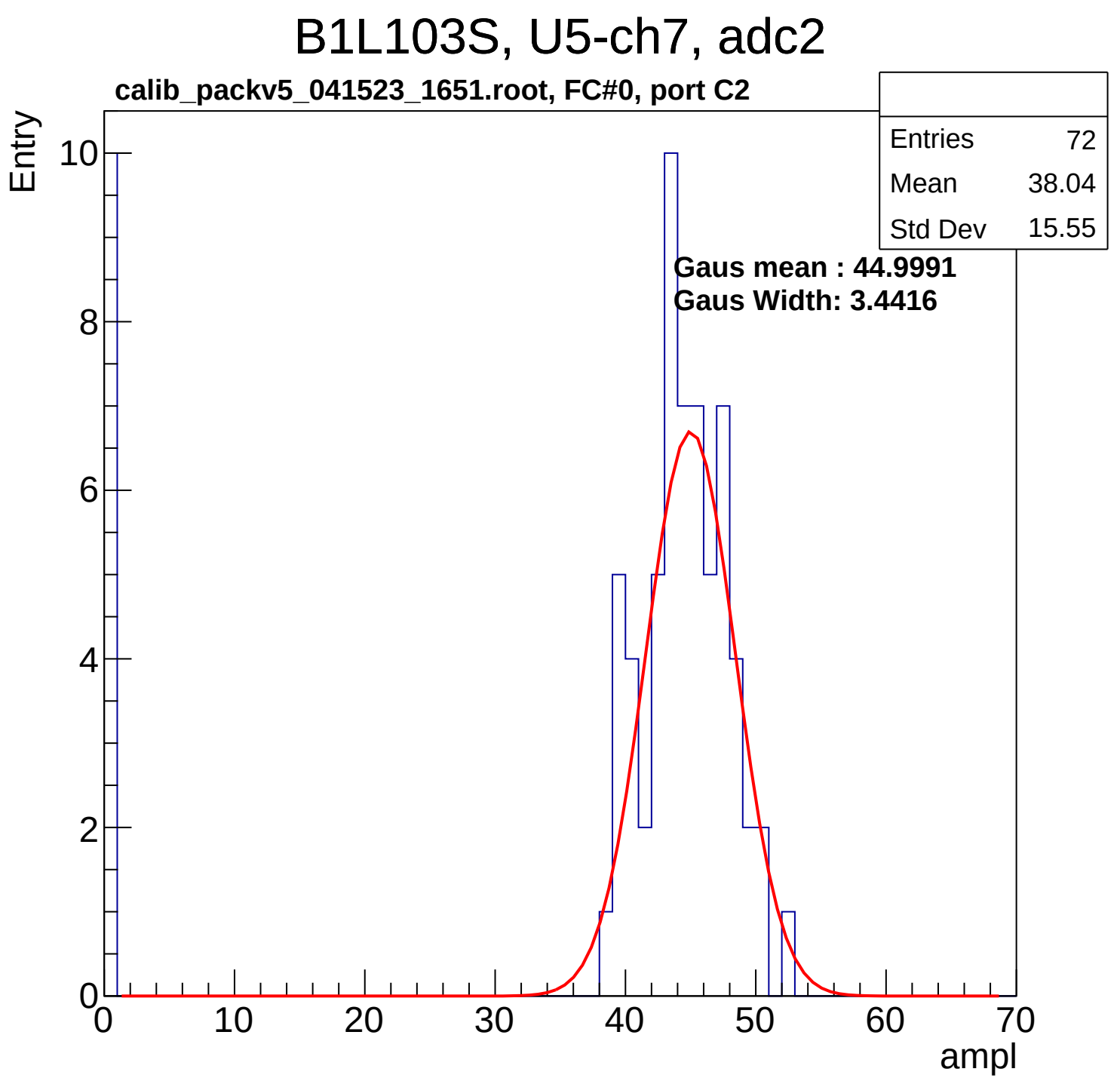
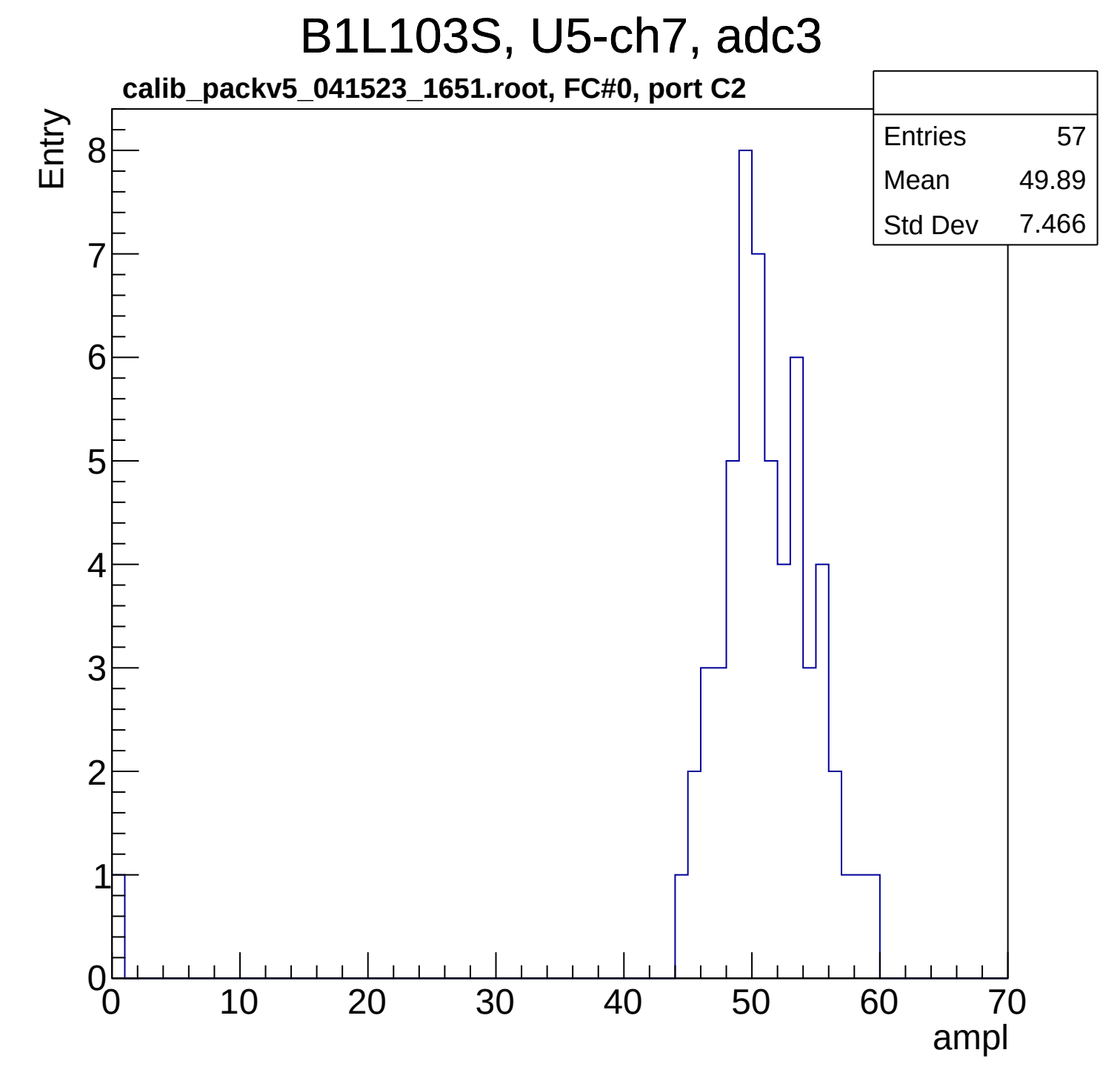

B1L103S, U5-ch7, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 34.7
Std Dev 10.18
Gaus mean : 37.7323
Gaus Width: 4.4061
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U5-ch7, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 38.04
Std Dev 15.55
Gaus mean : 44.9991
Gaus Width: 3.4416
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U5-ch7, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 49.89
Std Dev 7.466
Entry
ampl
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5
6
7
8
0
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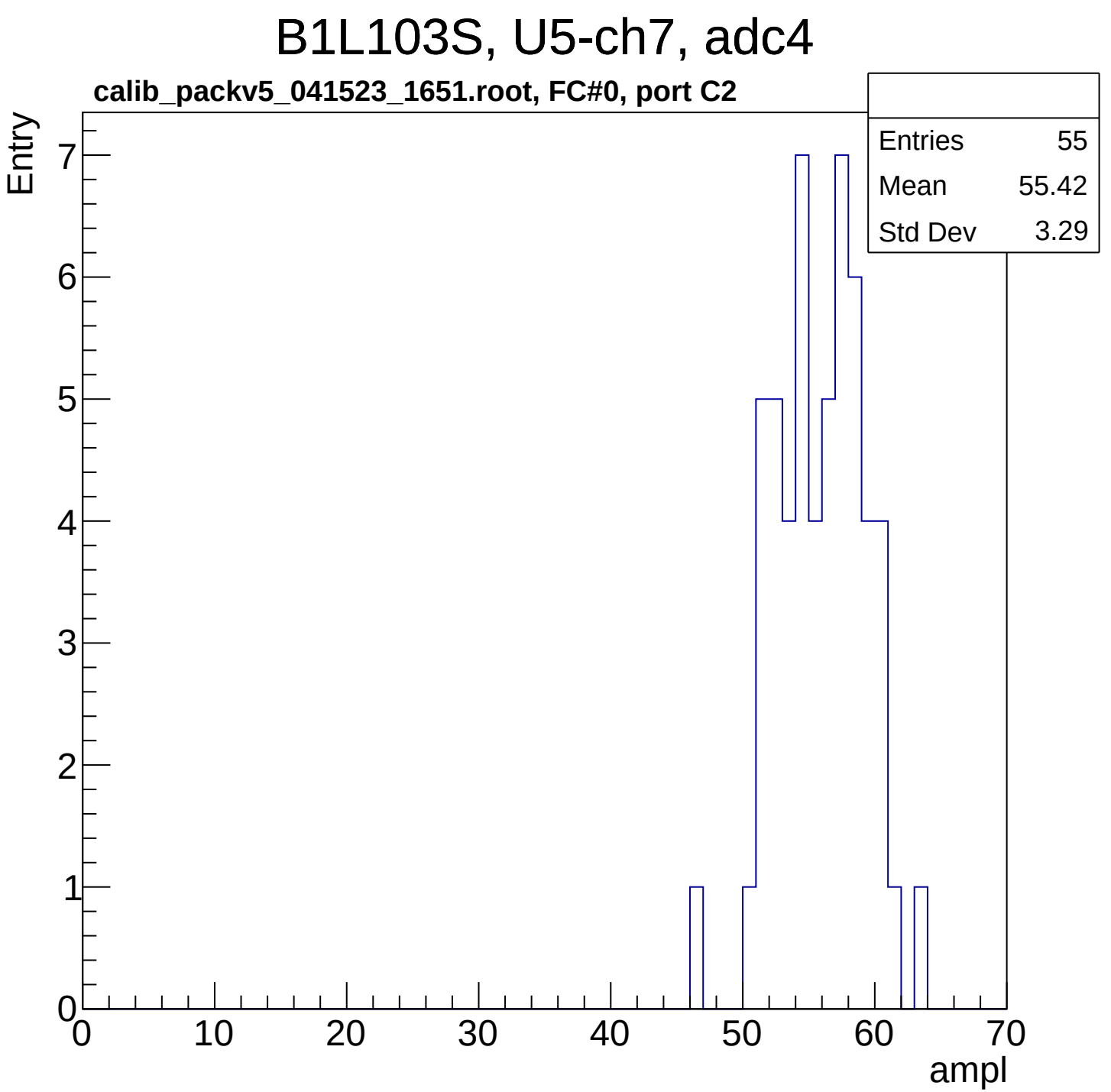
B1L103S, U5-ch7, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 55.42
Std Dev 3.29
Entry
ampl
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3
4
5
6
7
0
10
20
30
40
50
60
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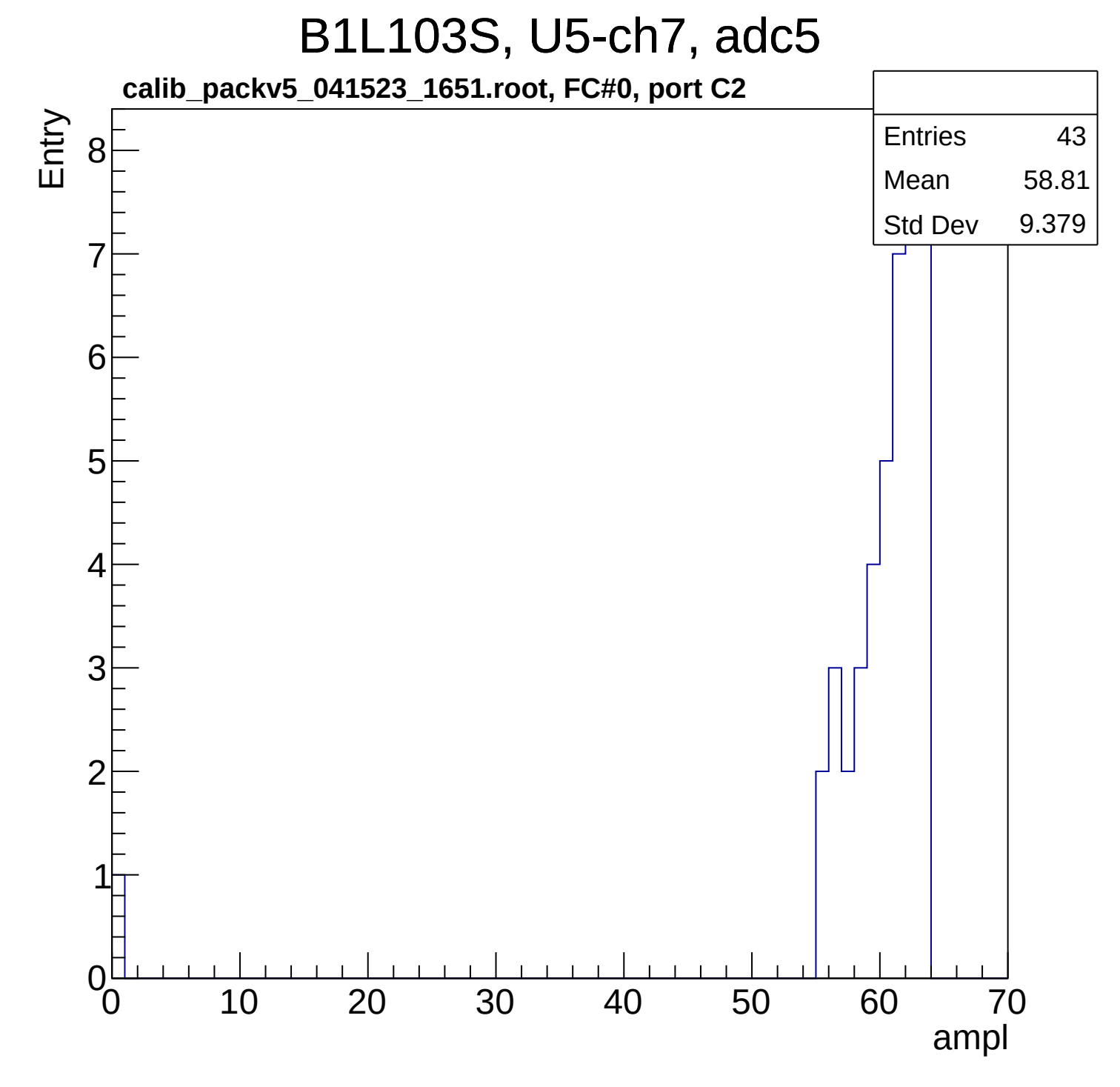
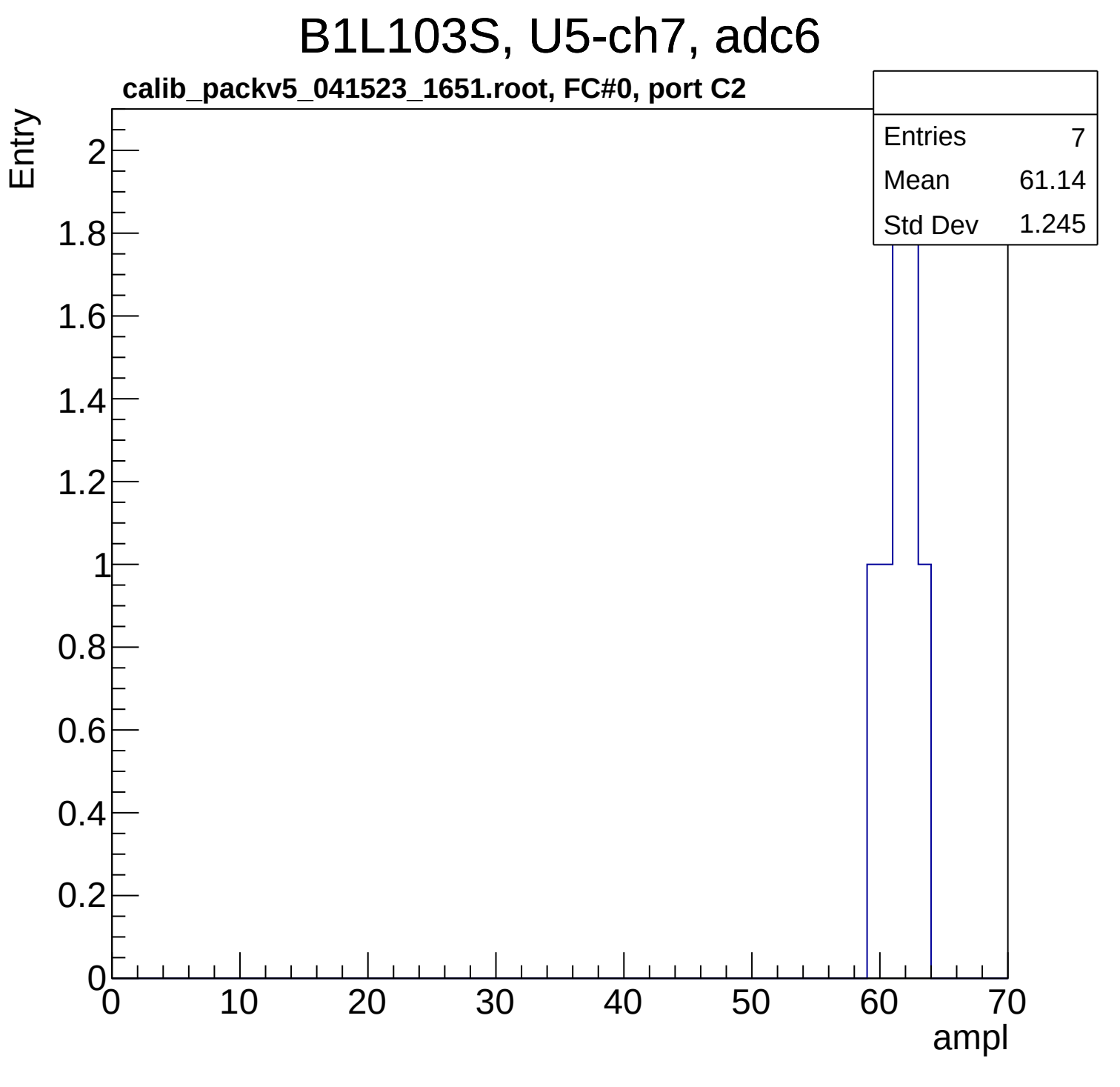

B1L103S, U5-ch7, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 58.81
Std Dev 9.379
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U5-ch7, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.14
Std Dev 1.245
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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40
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60
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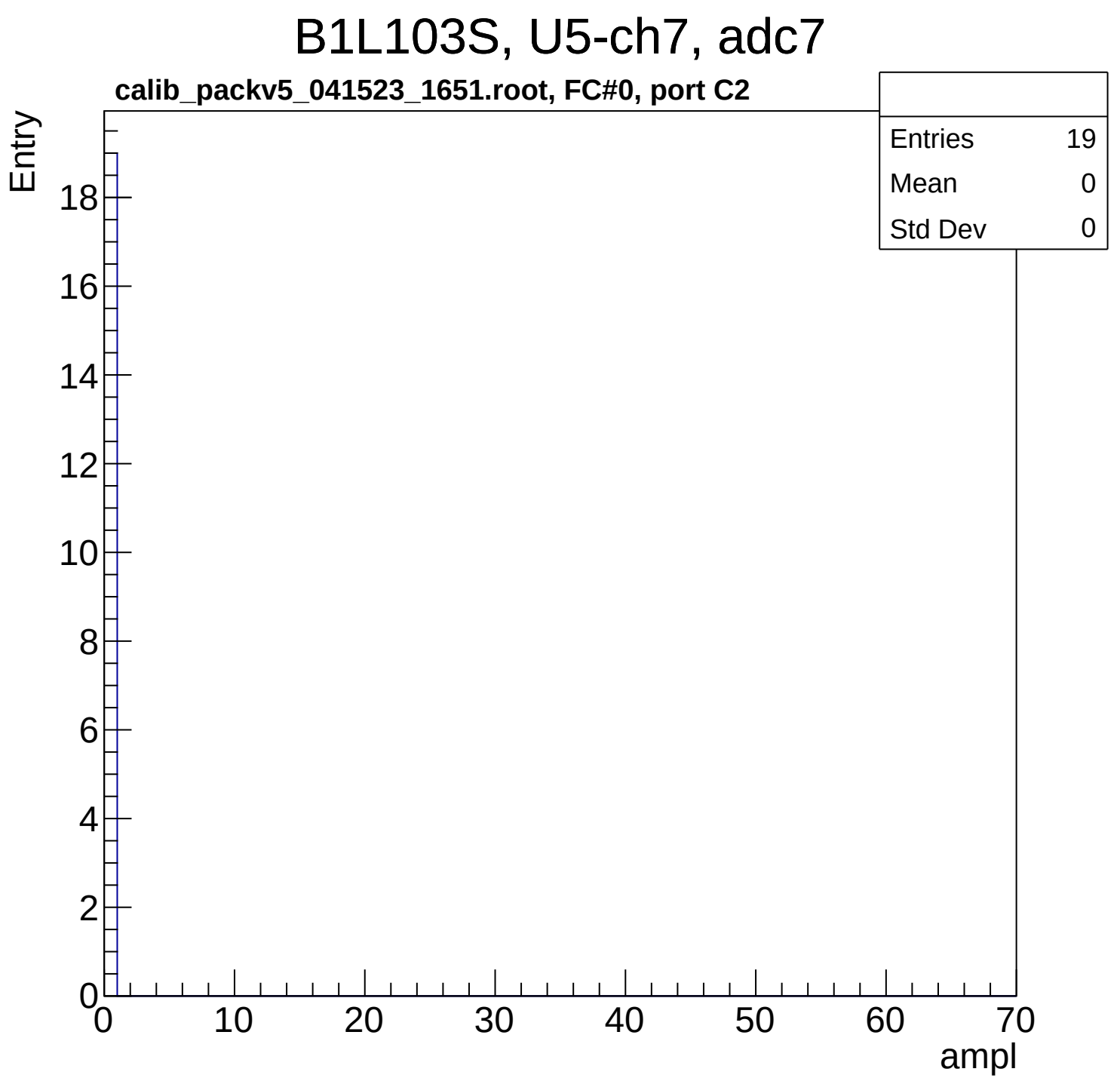
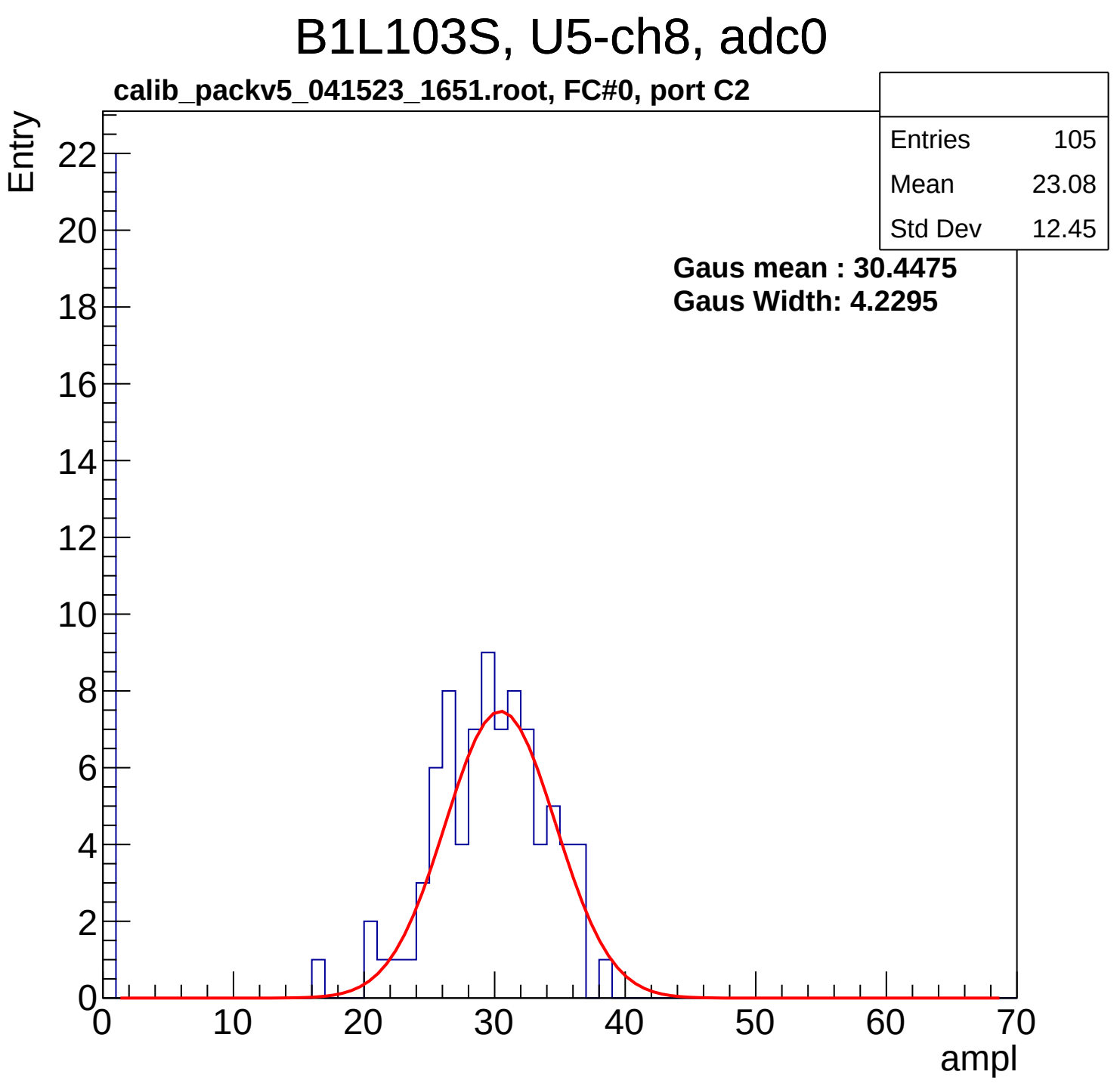
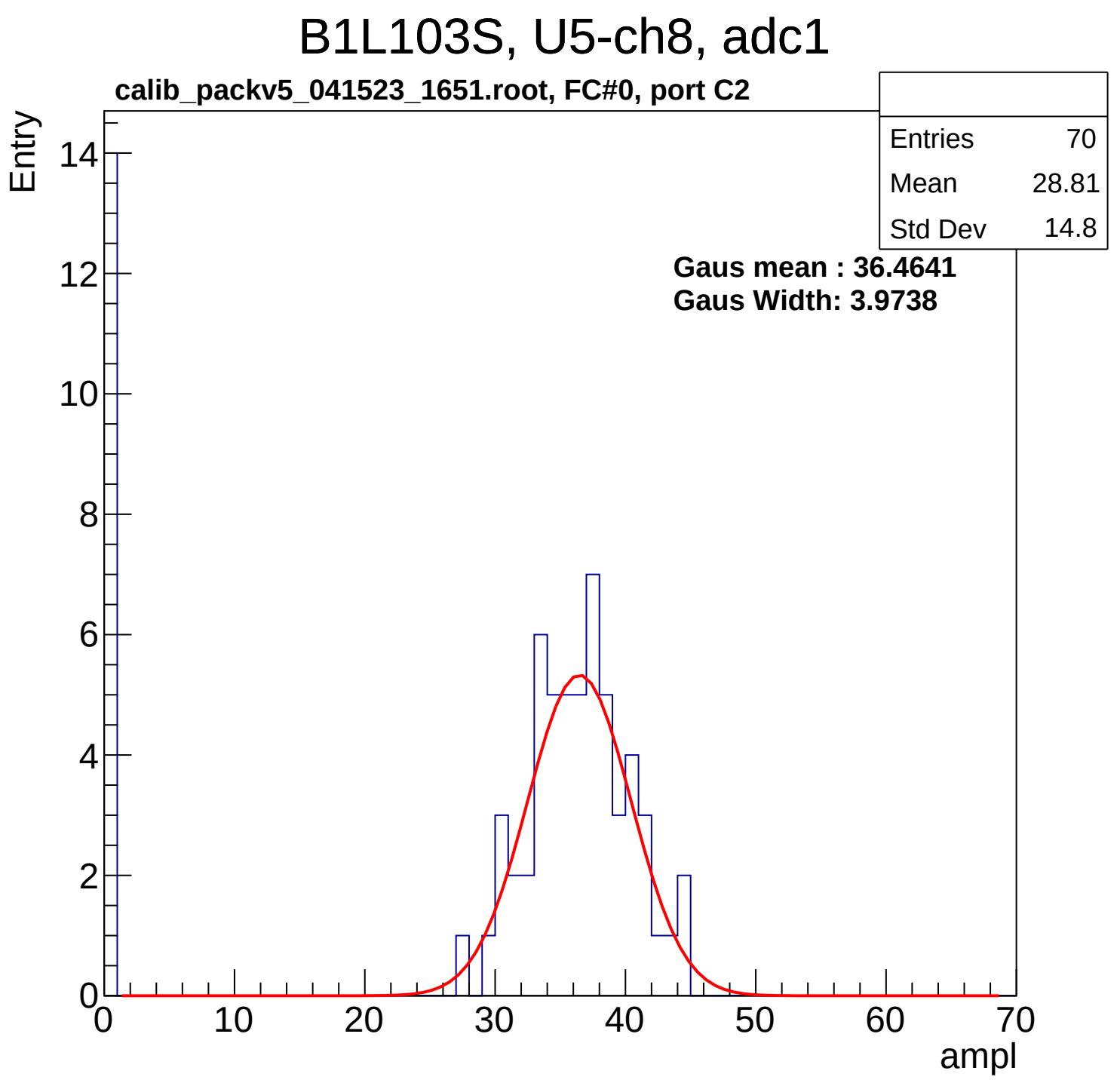

B1L103S, U5-ch7, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch8, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 105
Mean 23.08
Std Dev 12.45
Gaus mean : 30.4475
Gaus Width: 4.2295
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U5-ch8, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 28.81
Std Dev 14.8
Gaus mean : 36.4641
Gaus Width: 3.9738
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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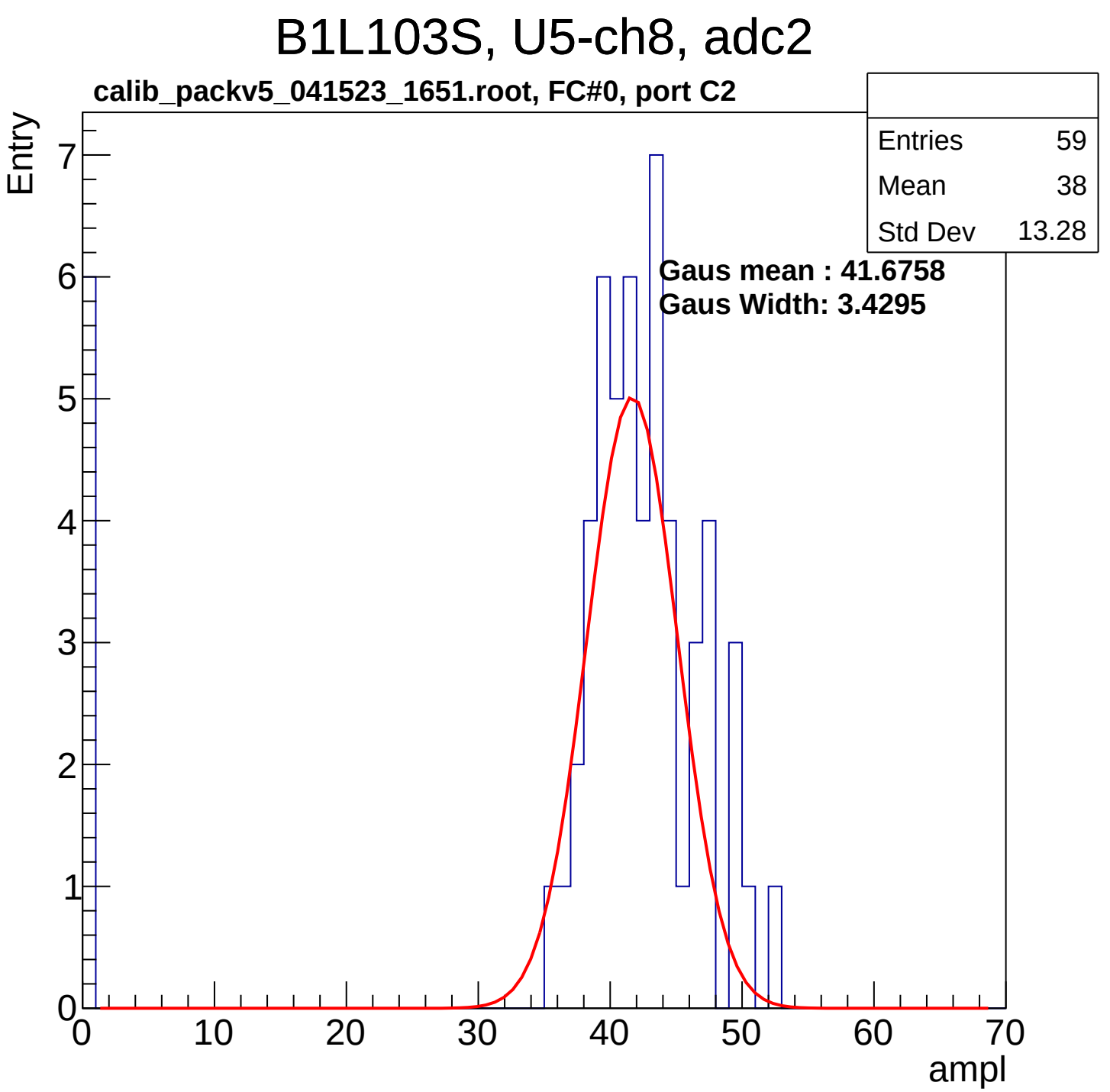
B1L103S, U5-ch8, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 38
Std Dev 13.28
Gaus mean : 41.6758
Gaus Width: 3.4295
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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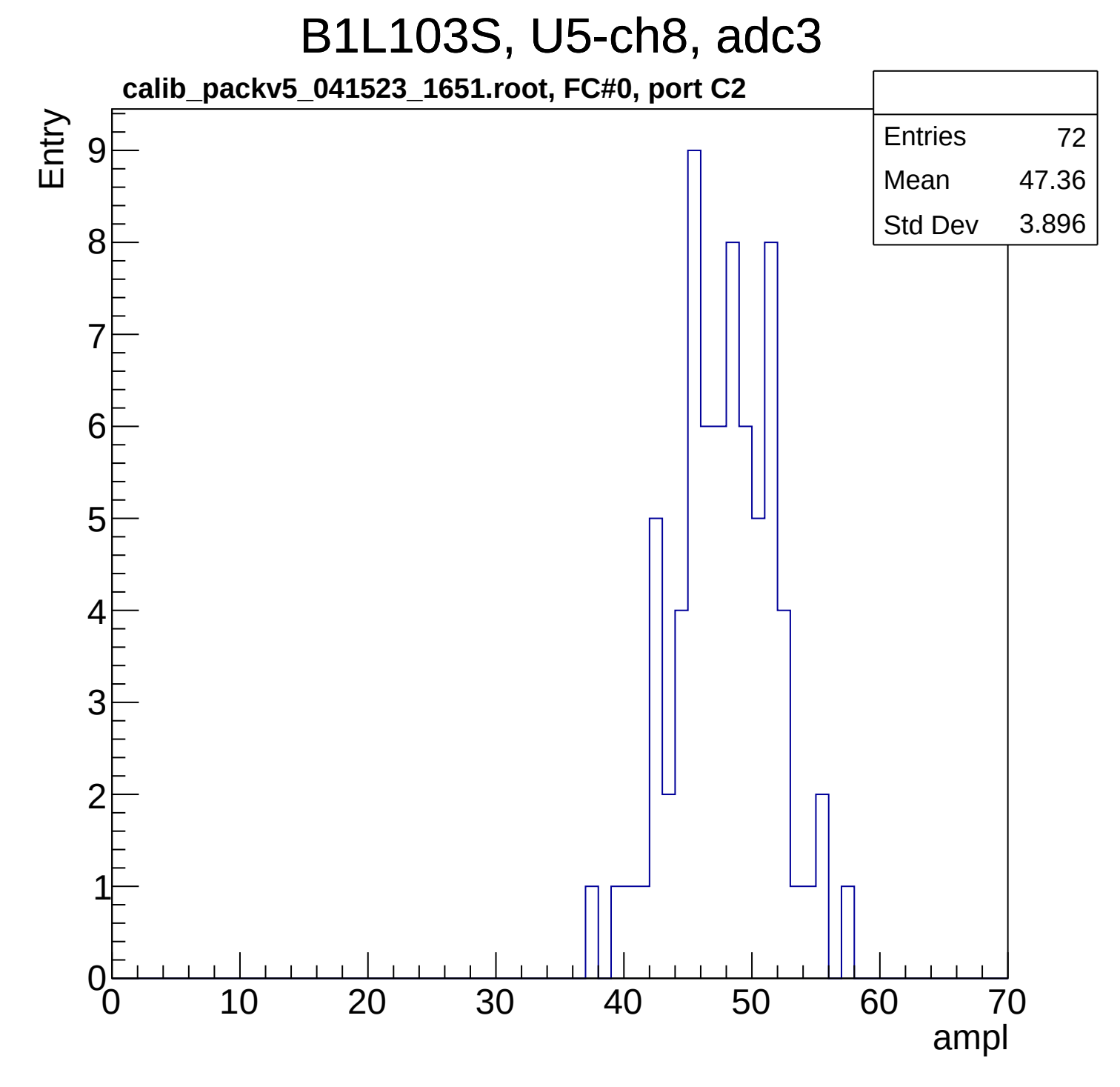
B1L103S, U5-ch8, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 47.36
Std Dev 3.896
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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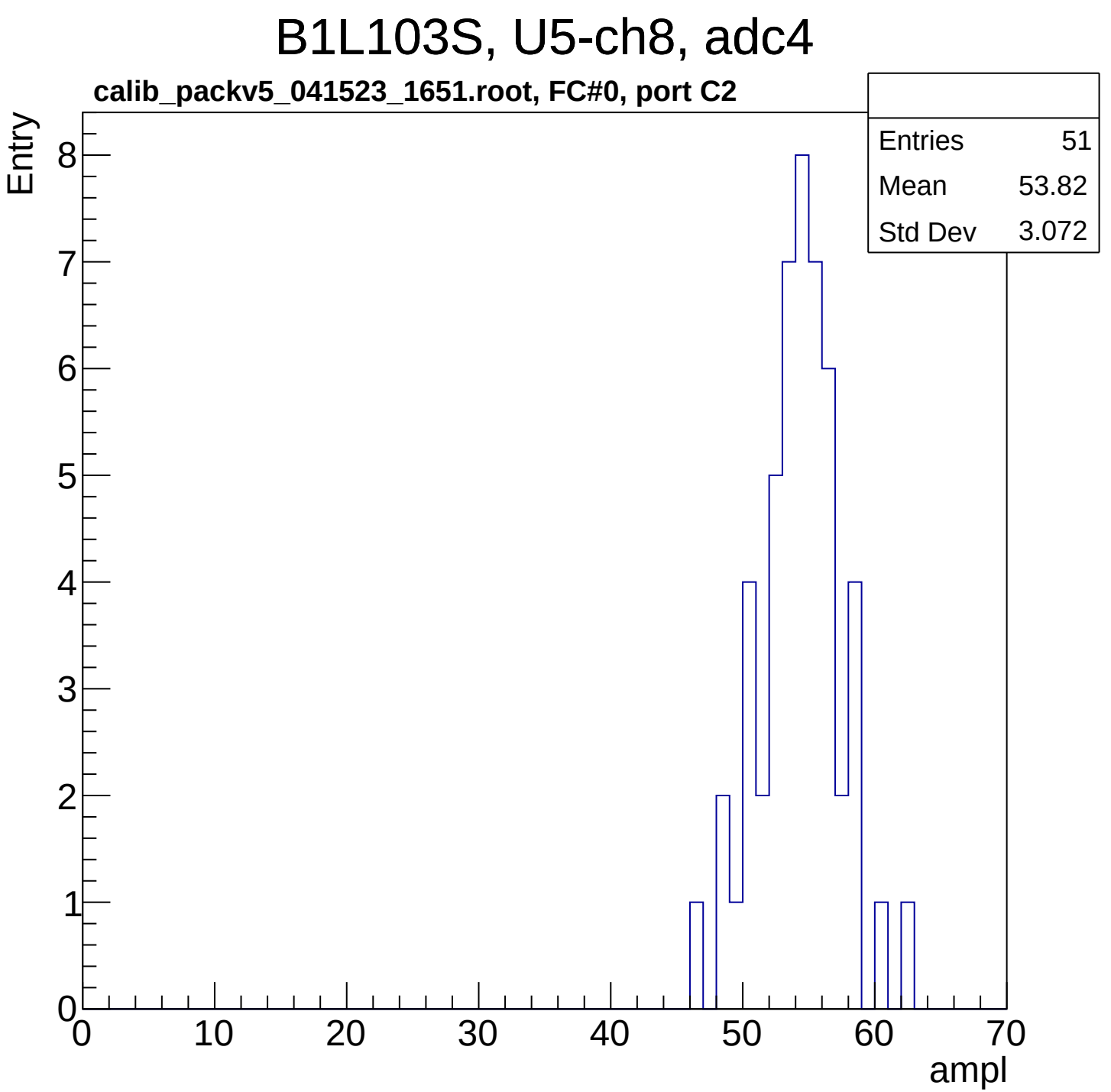
B1L103S, U5-ch8, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 53.82
Std Dev 3.072
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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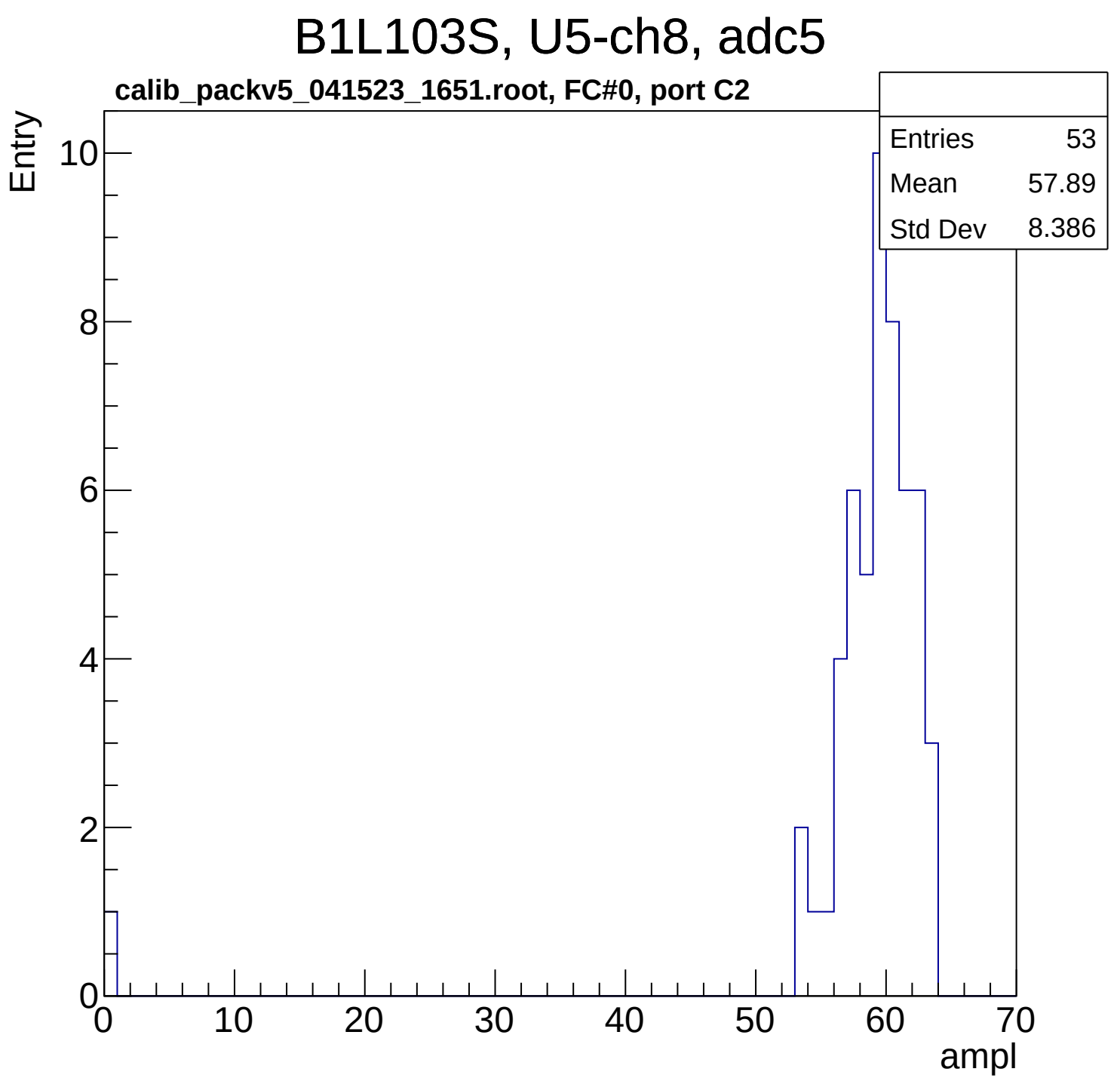
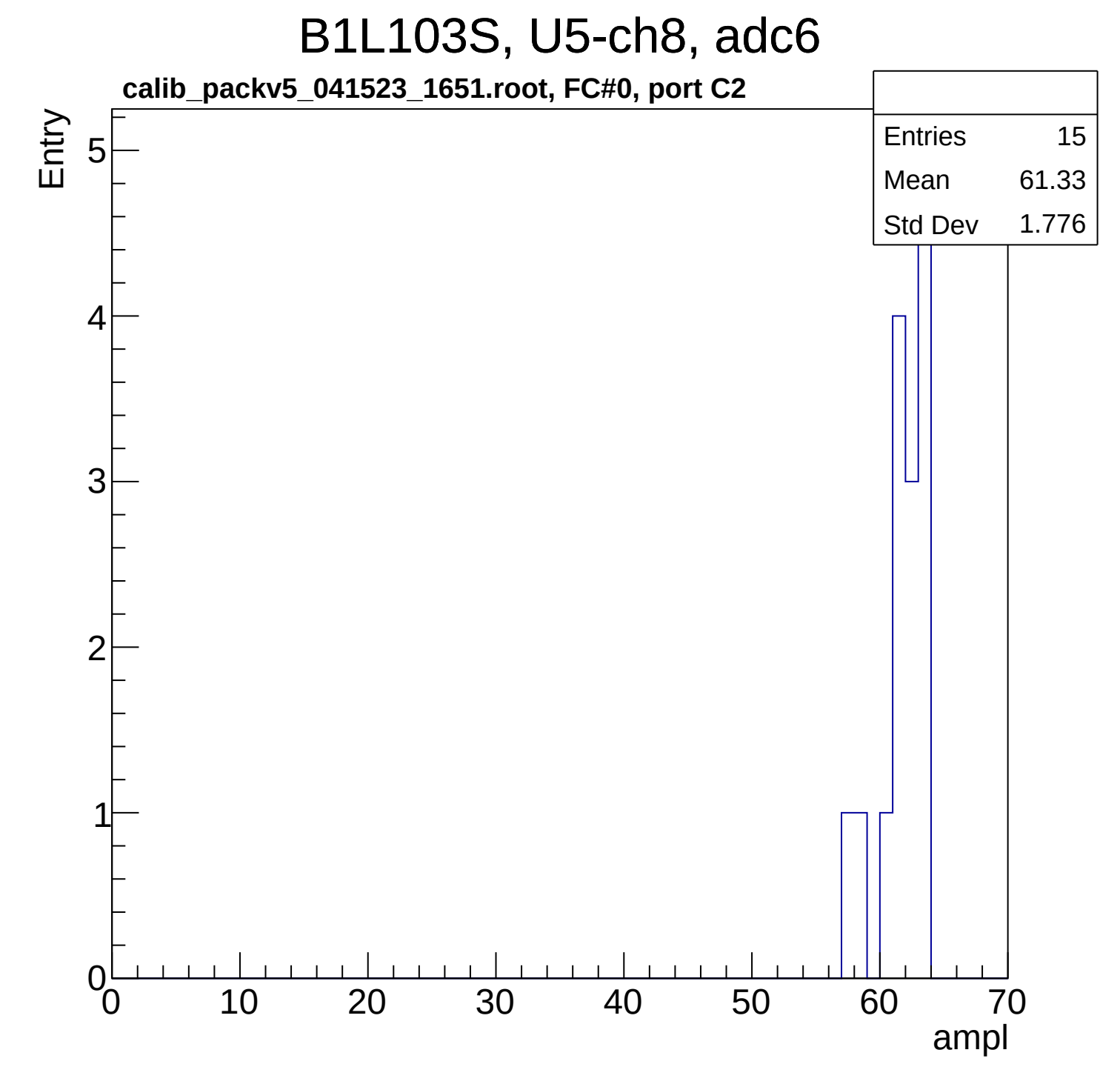
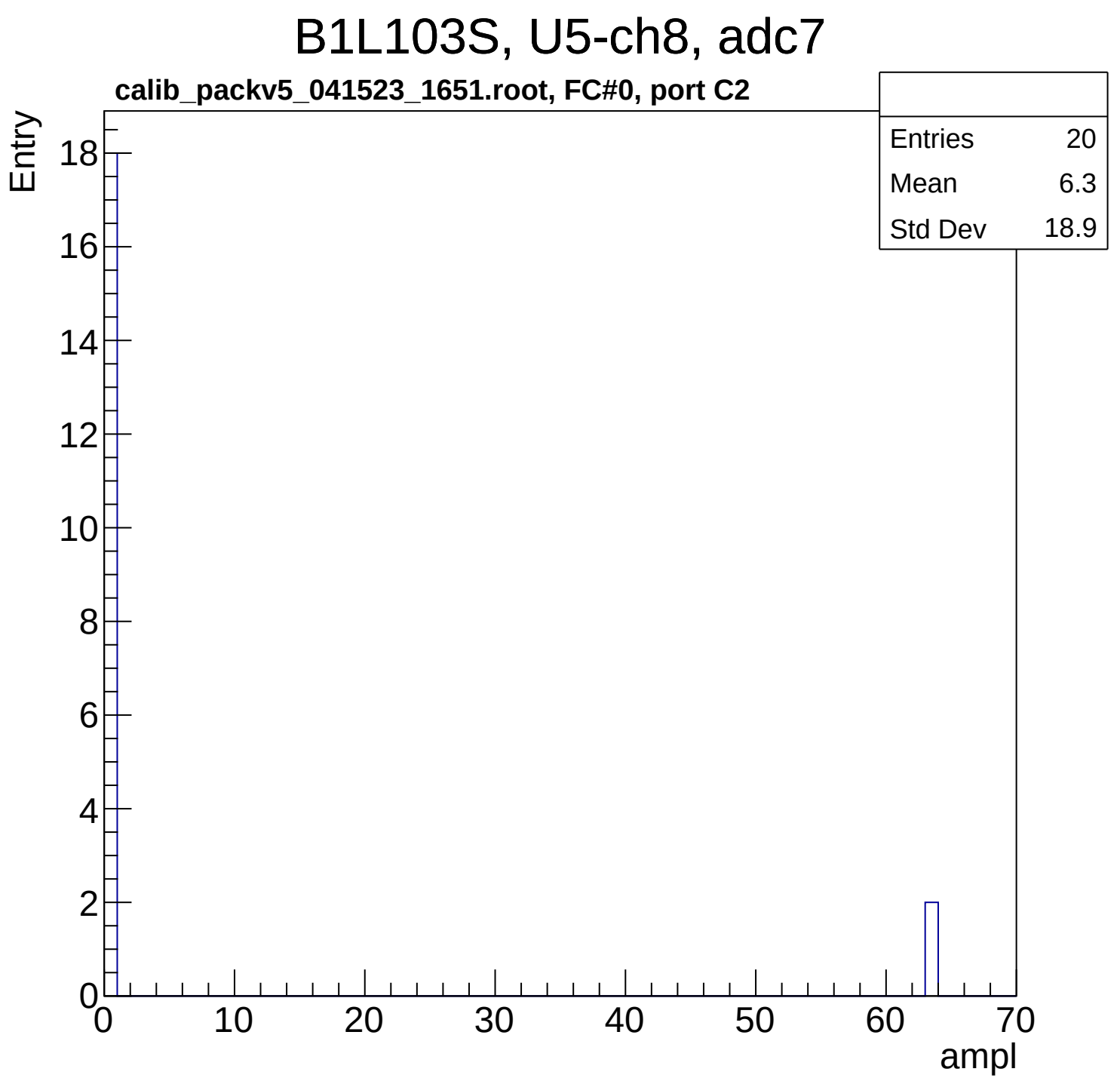
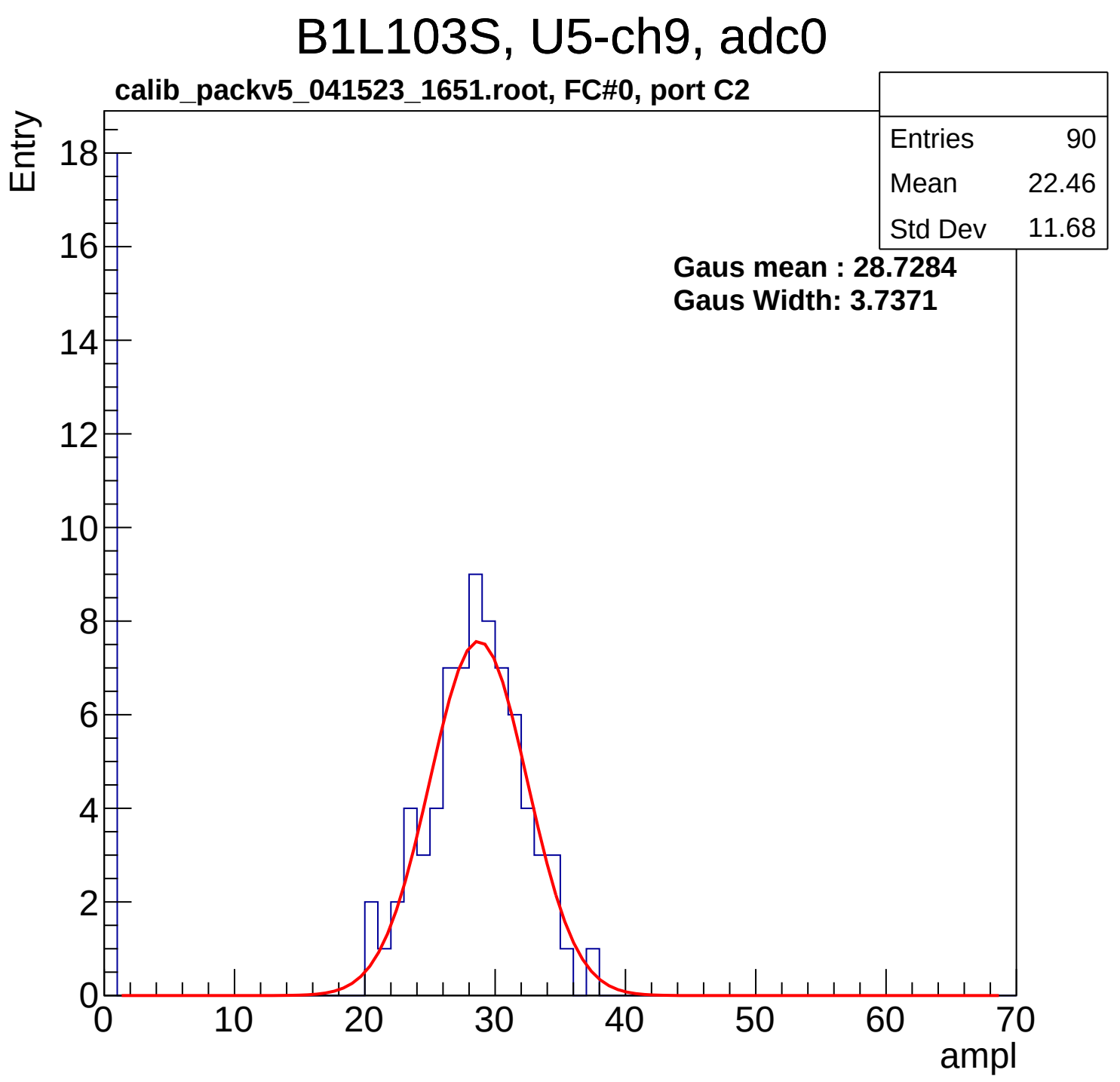

B1L103S, U5-ch8, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 57.89
Std Dev 8.386
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch8, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.33
Std Dev 1.776
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U5-ch8, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.3
Std Dev 18.9
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch9, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 22.46
Std Dev 11.68
Gaus mean : 28.7284
Gaus Width: 3.7371
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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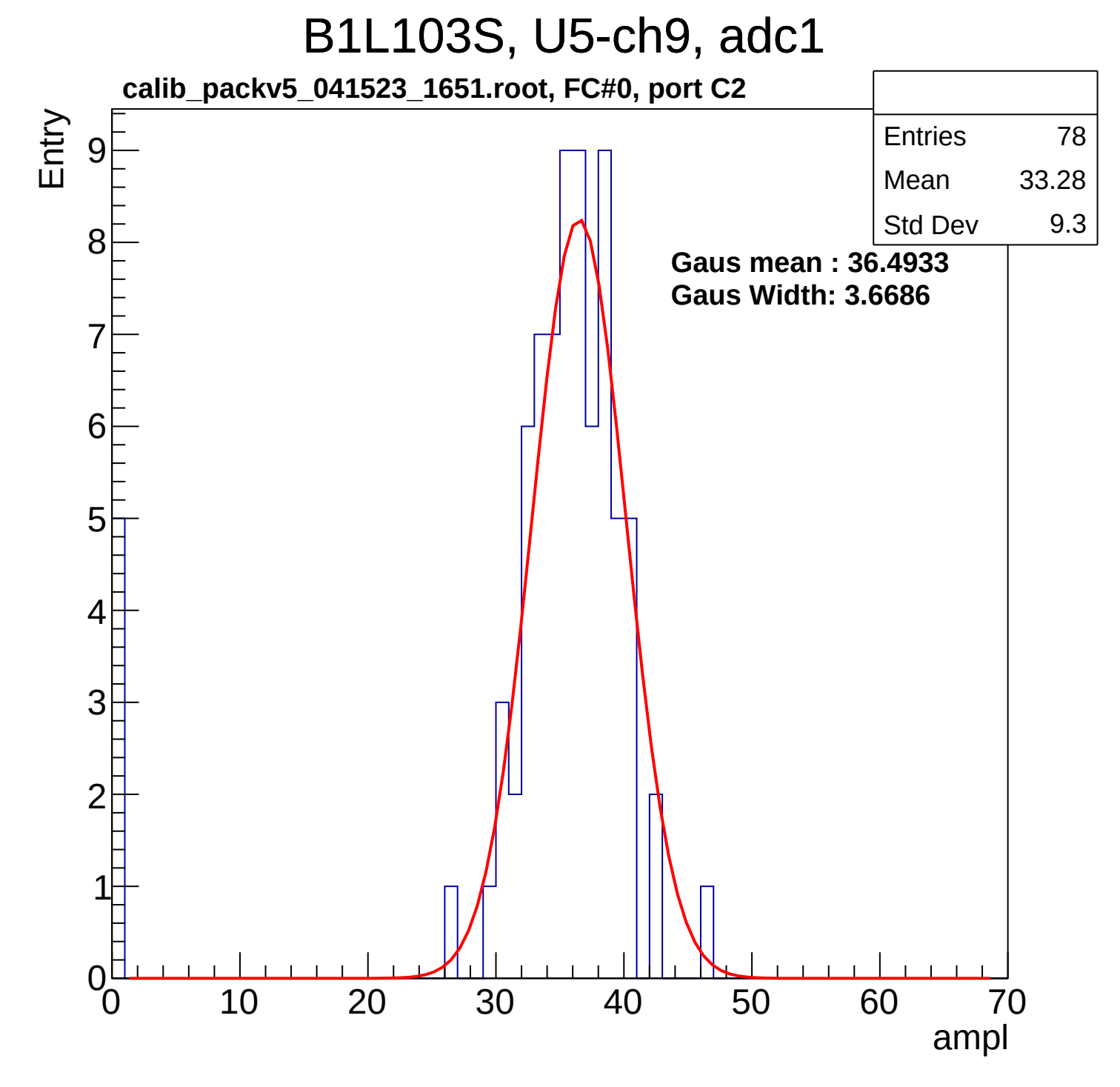
B1L103S, U5-ch9, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 33.28
Std Dev 9.3
Gaus mean : 36.4933
Gaus Width: 3.6686
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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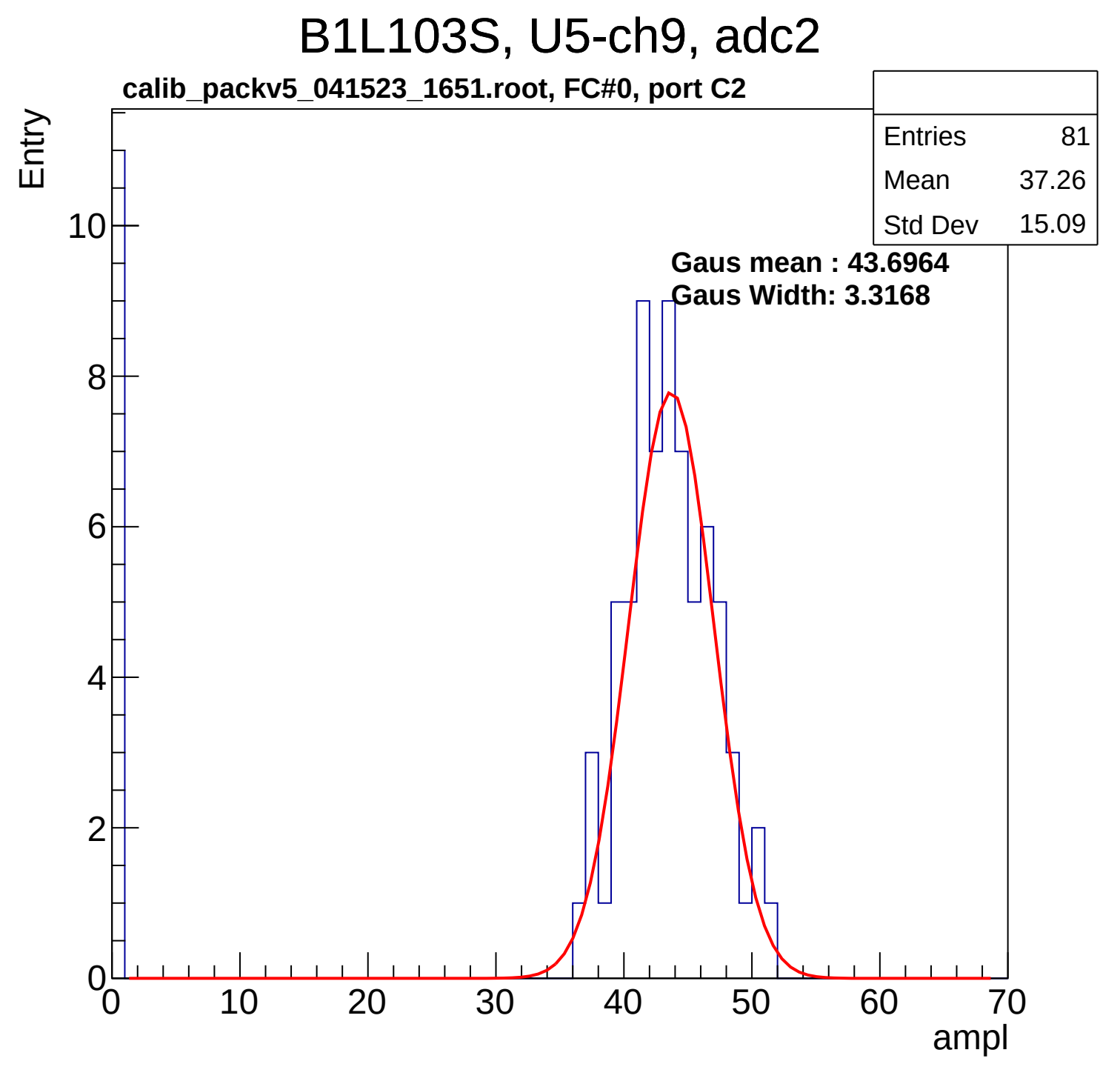
B1L103S, U5-ch9, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 37.26
Std Dev 15.09
Gaus mean : 43.6964
Gaus Width: 3.3168
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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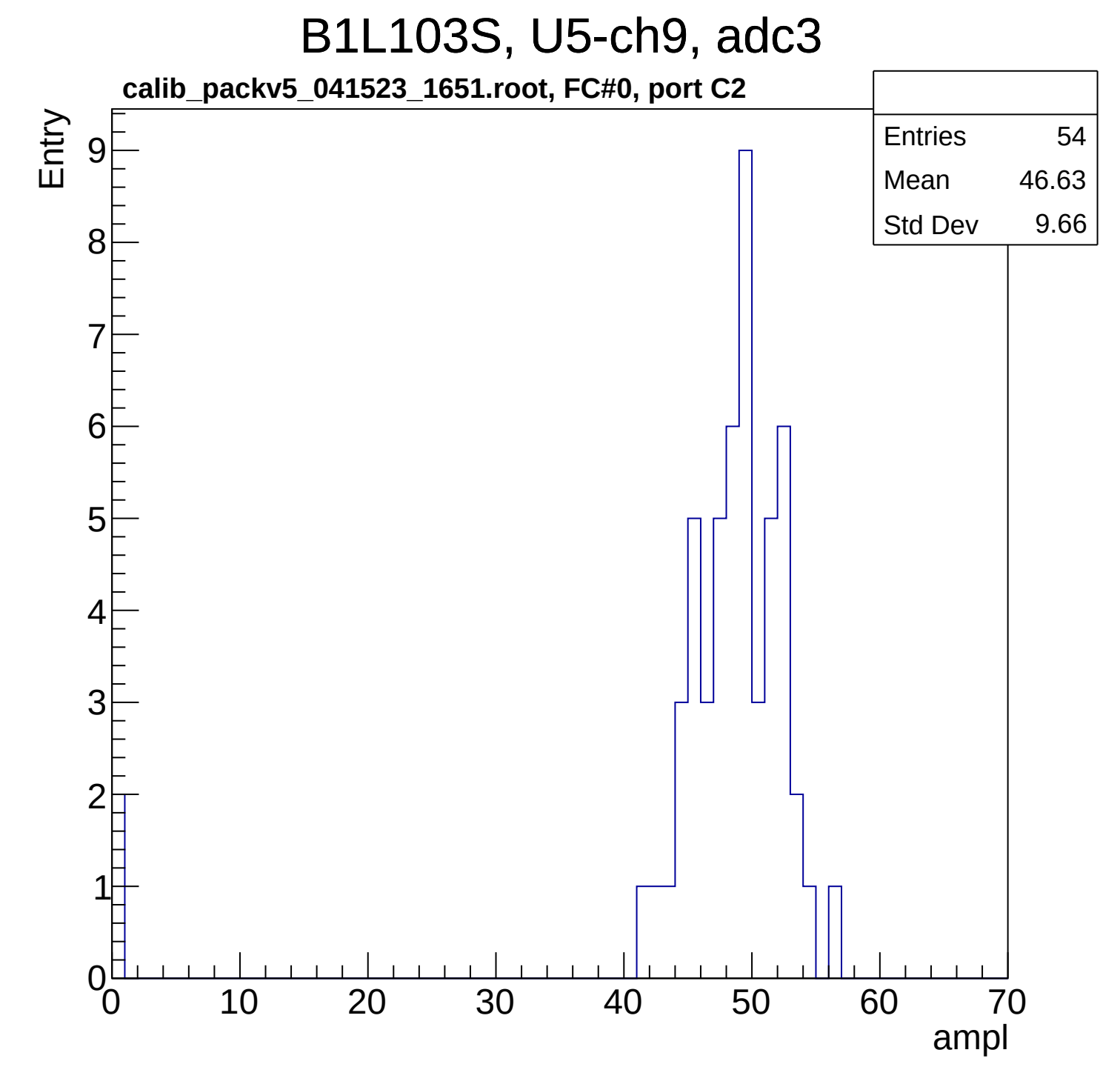
B1L103S, U5-ch9, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 46.63
Std Dev 9.66
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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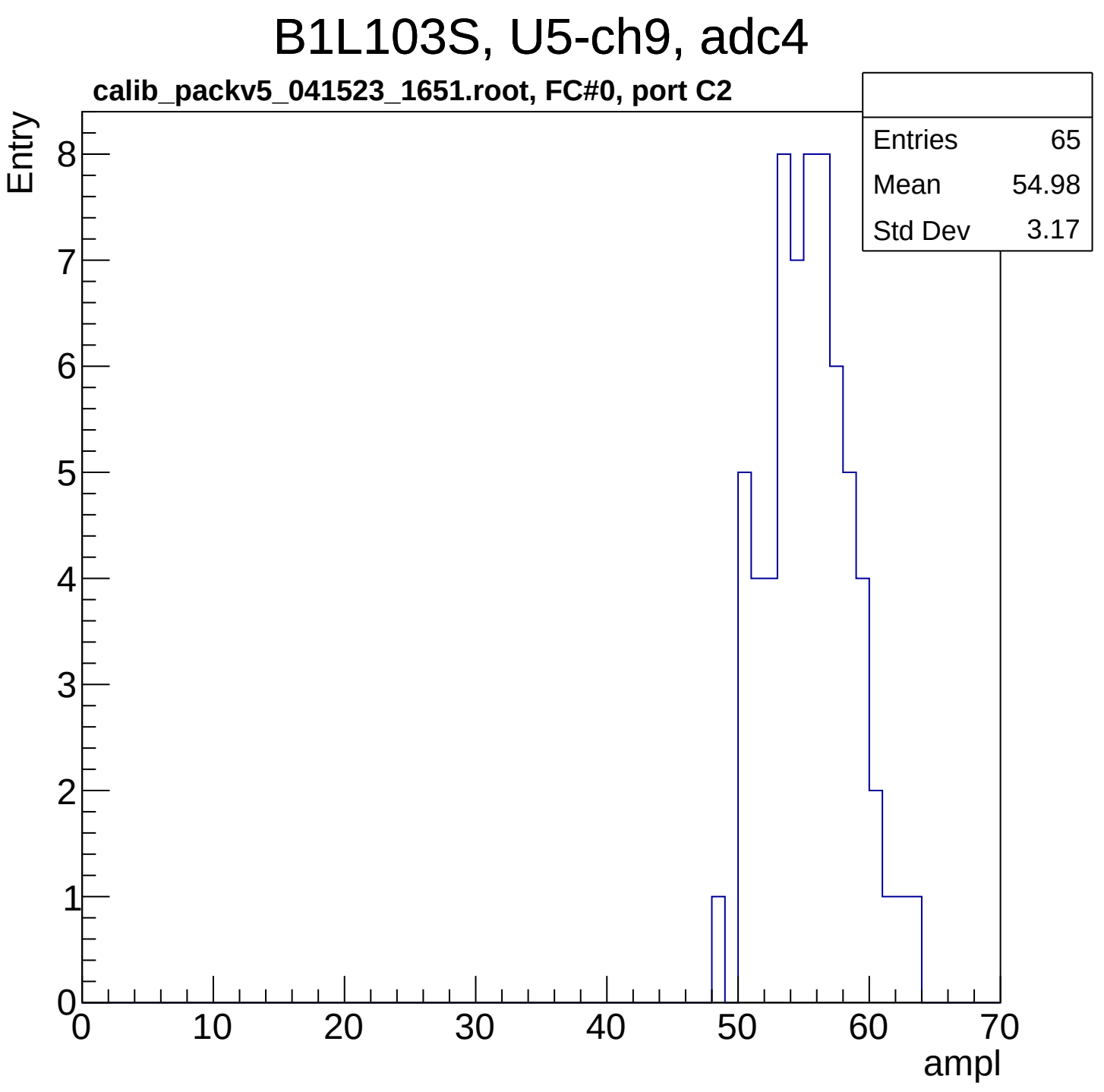
B1L103S, U5-ch9, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 54.98
Std Dev 3.17
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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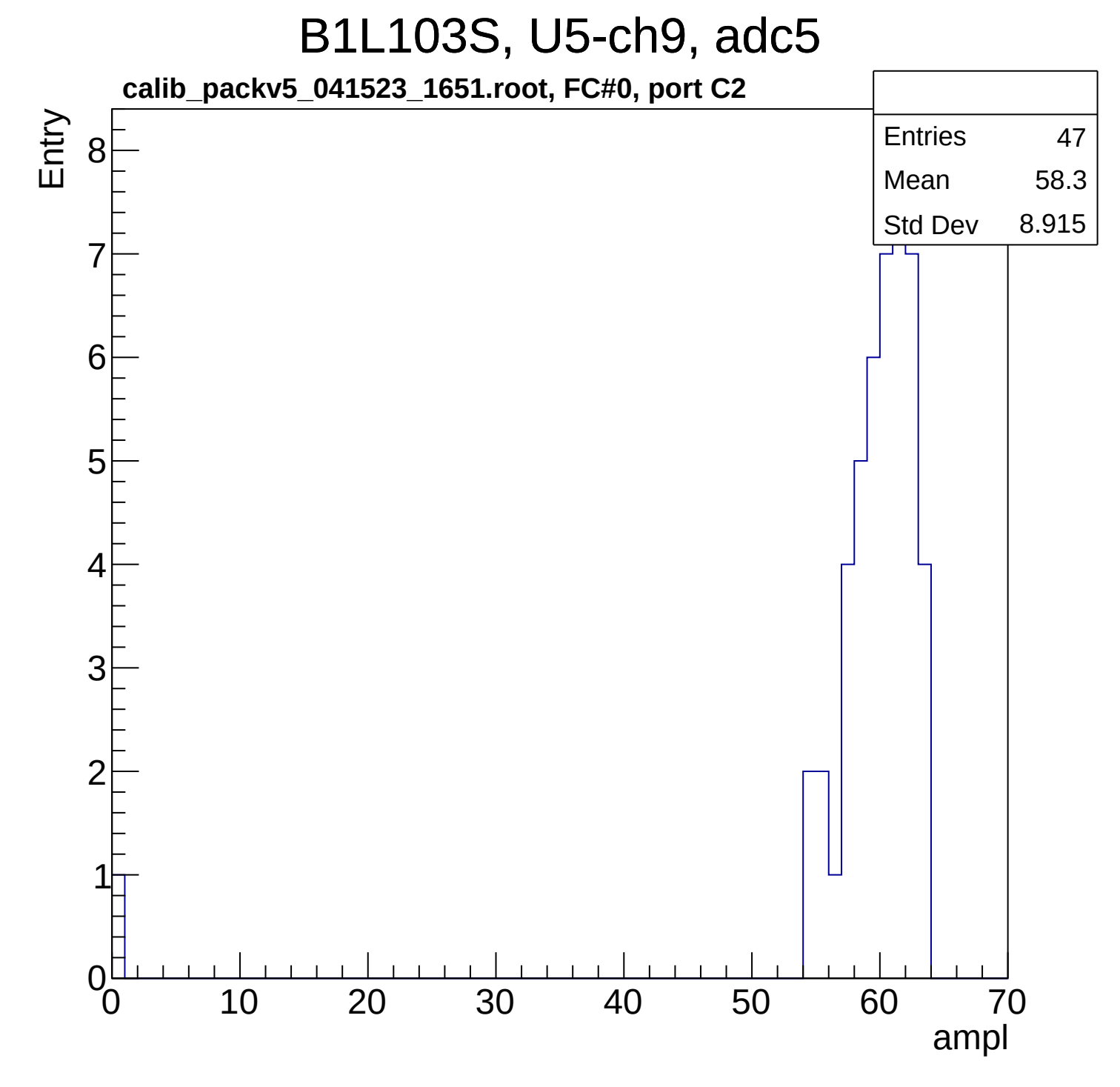
B1L103S, U5-ch9, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.3
Std Dev 8.915
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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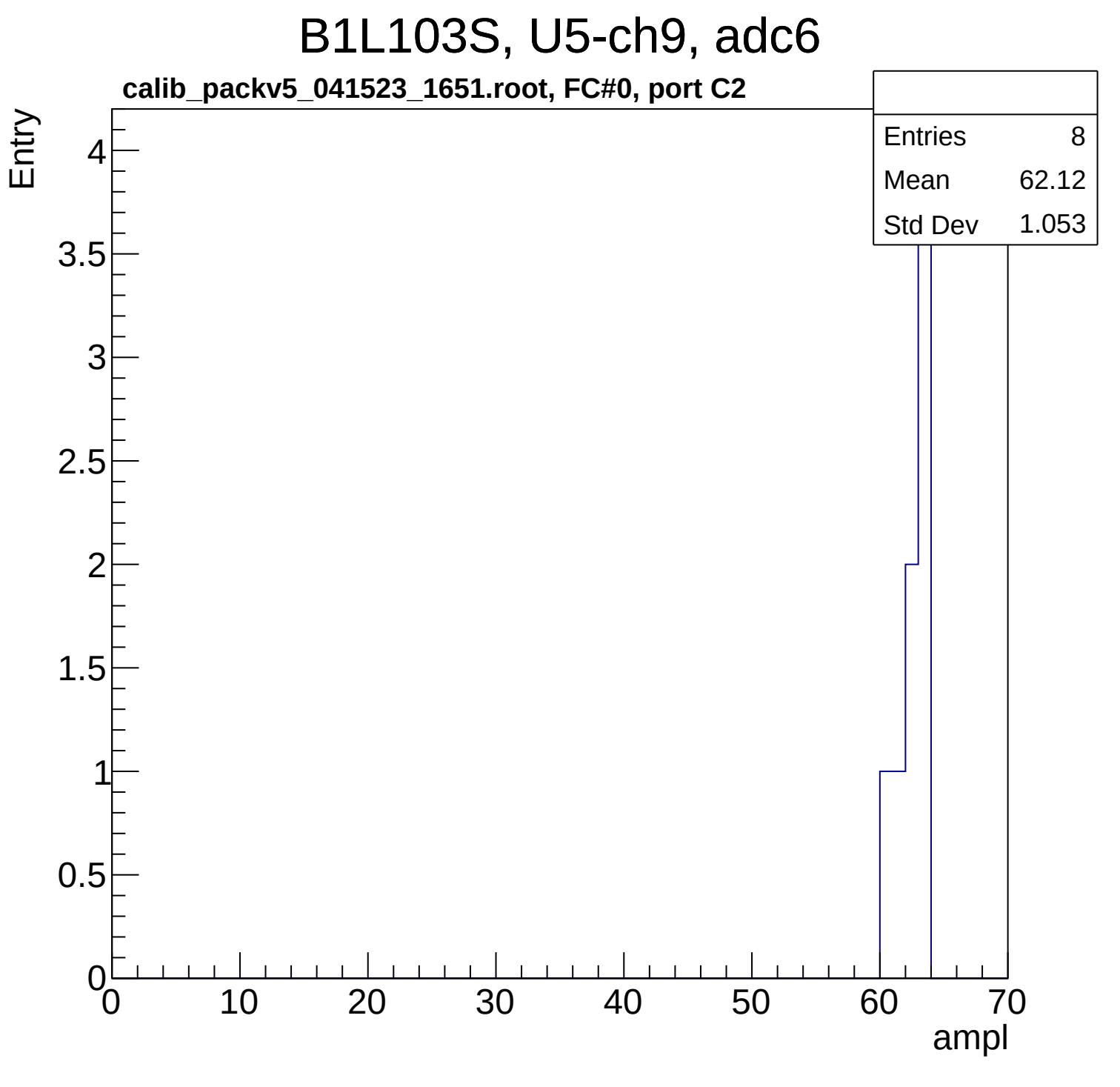
B1L103S, U5-ch9, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62.12
Std Dev 1.053
Entry
ampl
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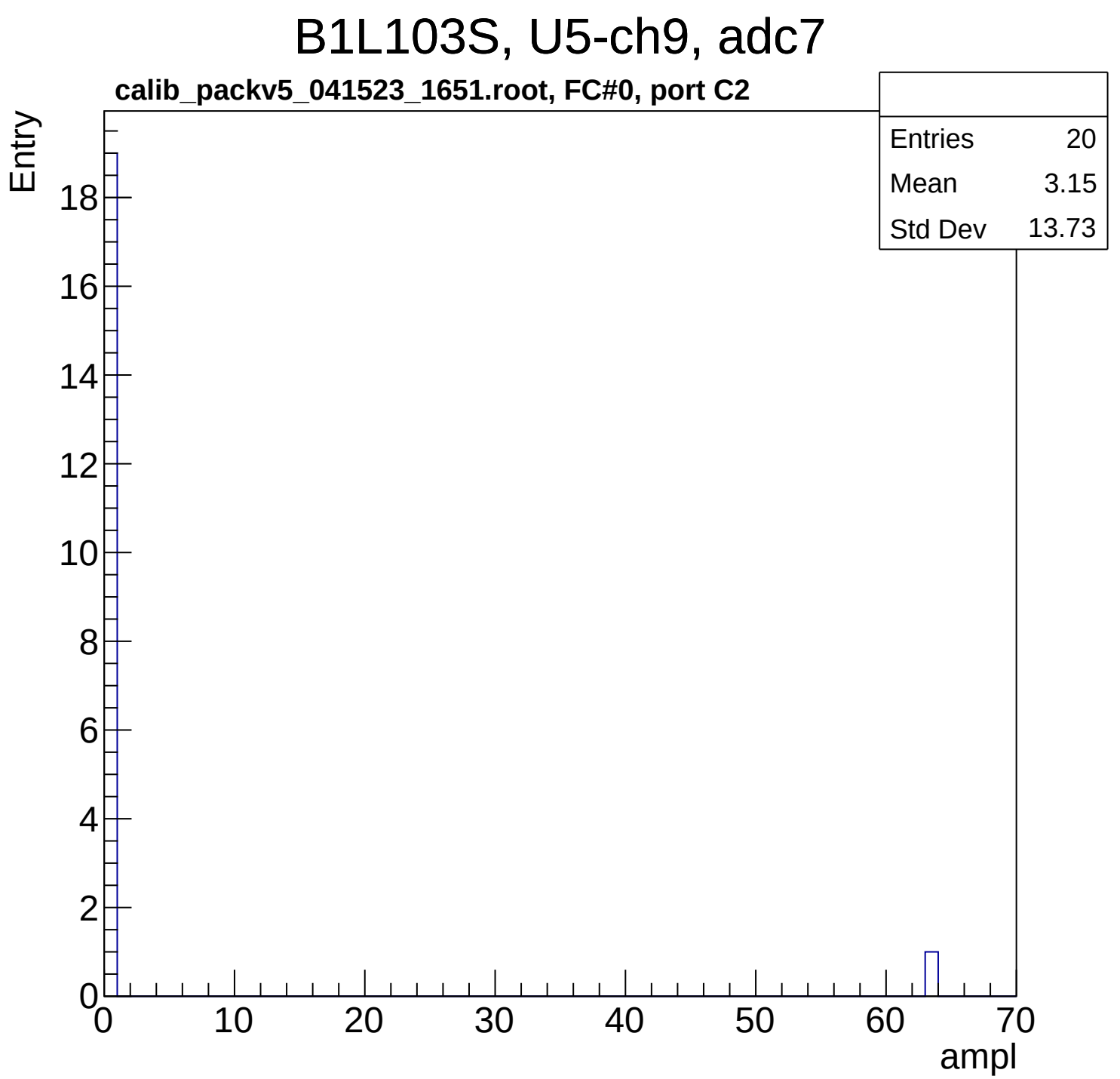
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U5-ch9, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
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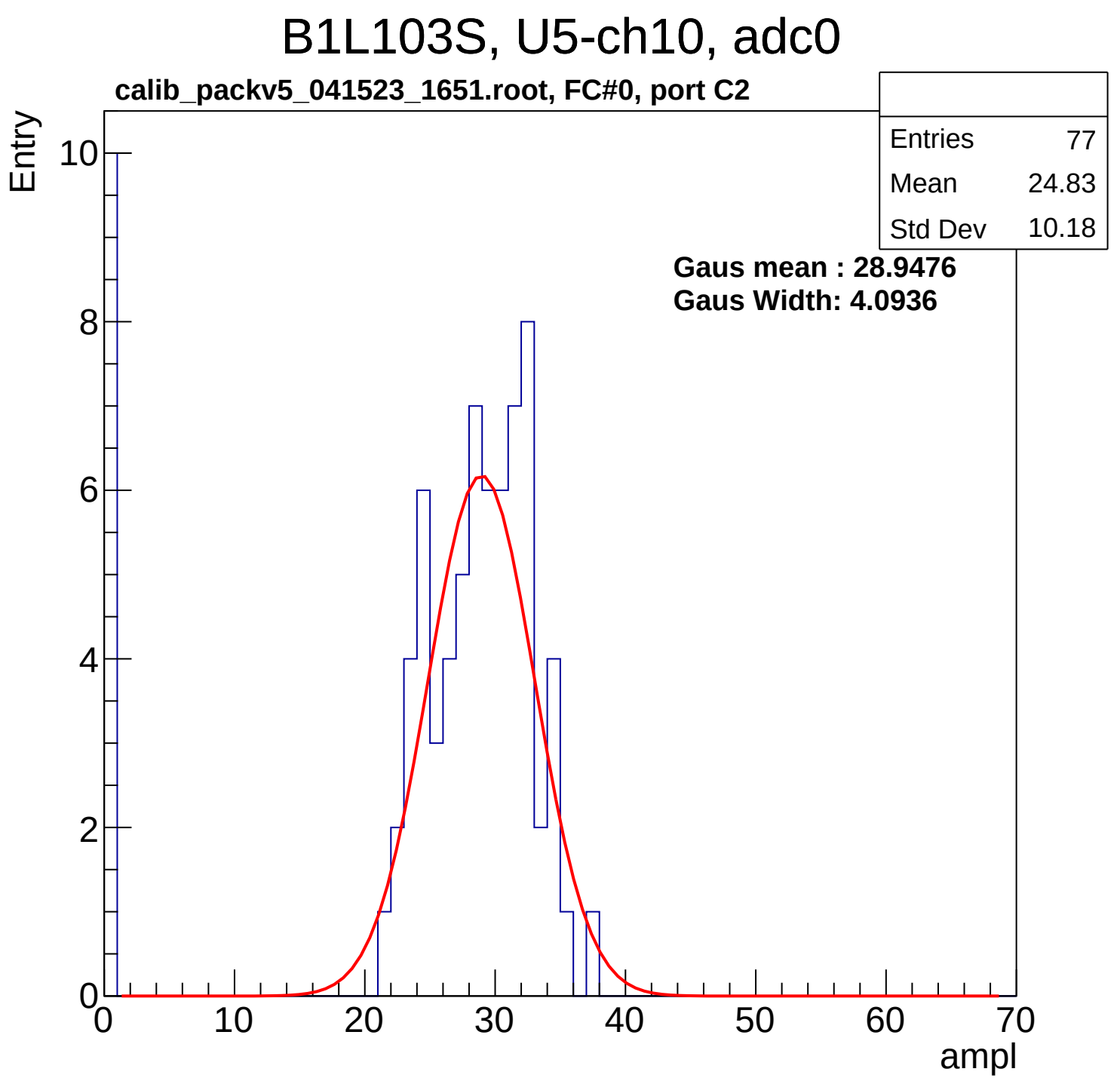
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch10, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 24.83
Std Dev 10.18
Gaus mean : 28.9476
Gaus Width: 4.0936
Entry
ampl
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2
4
6
8
10
0
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20
30
40
50
60
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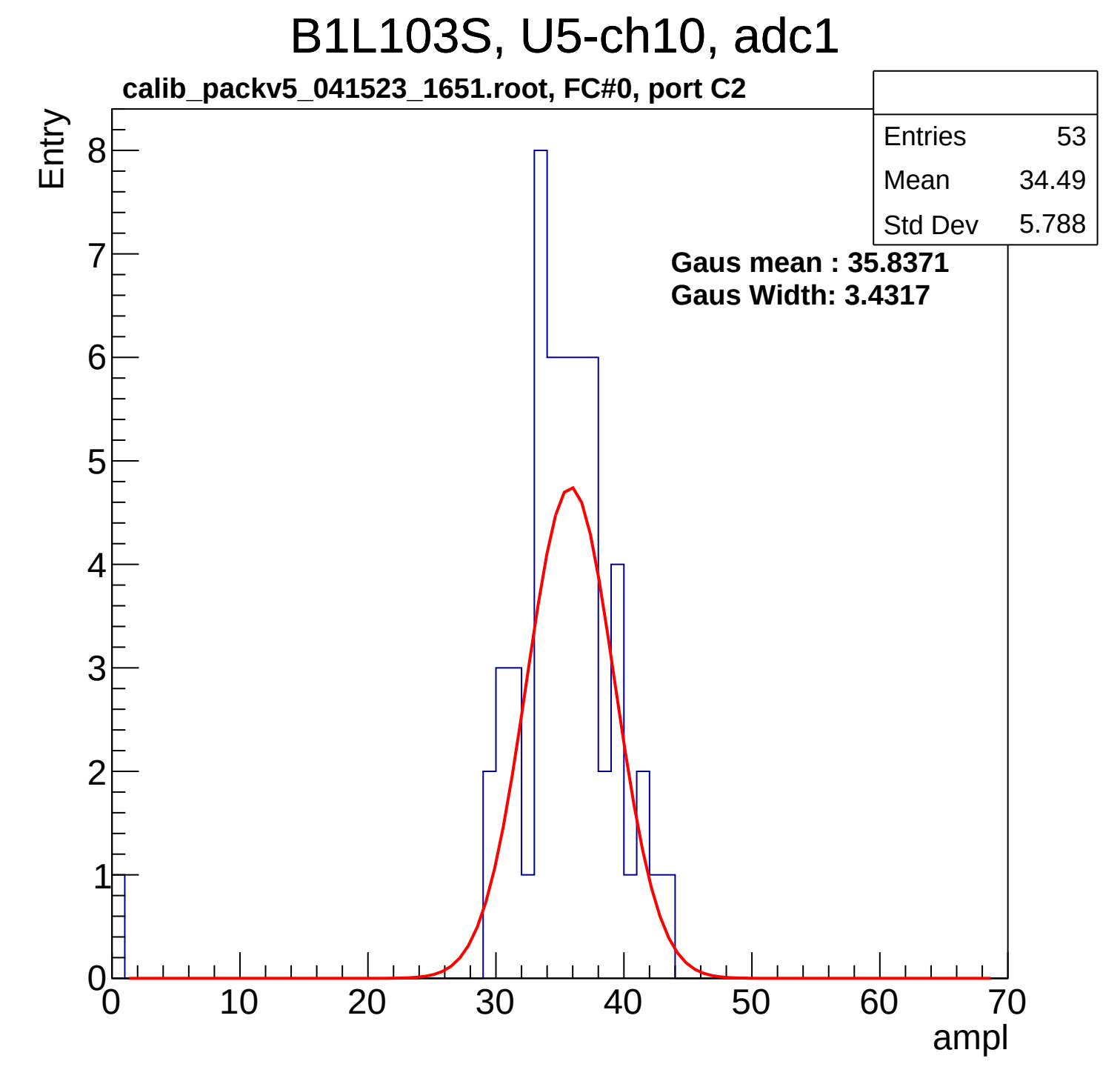
B1L103S, U5-ch10, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 34.49
Std Dev 5.788
Gaus mean : 35.8371
Gaus Width: 3.4317
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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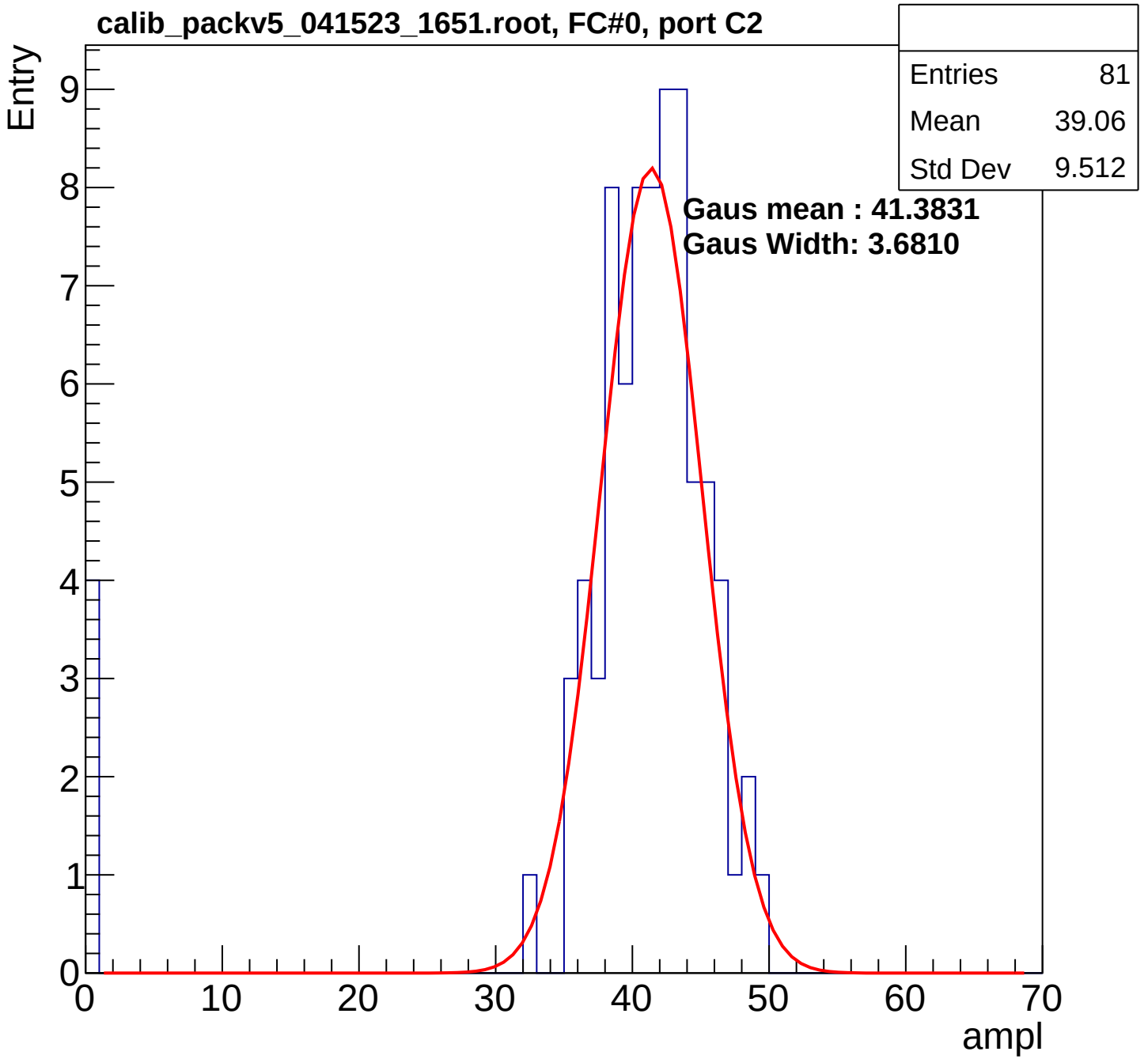
B1L103S, U5-ch10, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 39.06
Std Dev 9.512
Gaus mean : 41.3831
Gaus Width: 3.6810
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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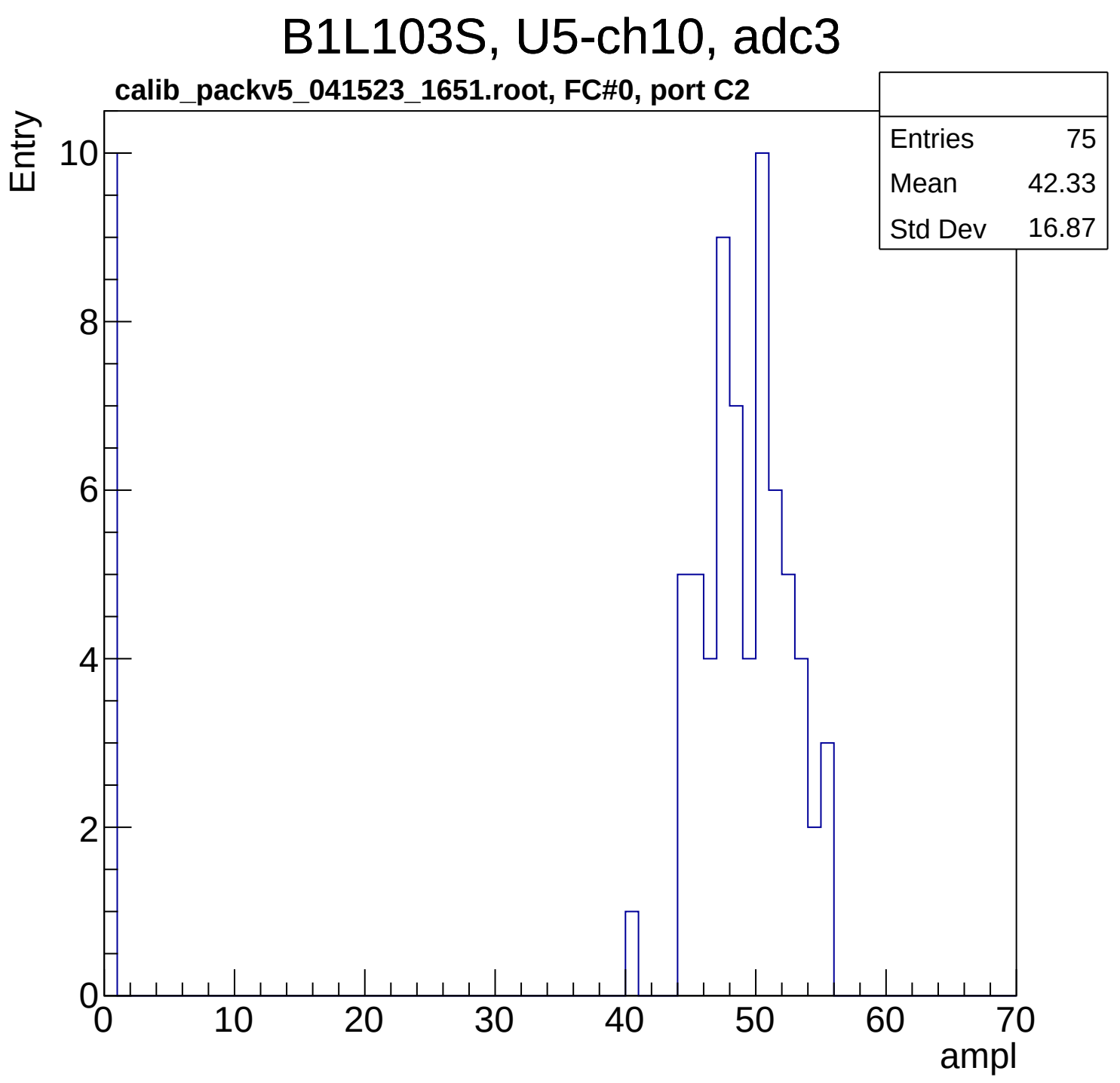
B1L103S, U5-ch10, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 42.33
Std Dev 16.87
Entry
ampl
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2
4
6
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0
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60
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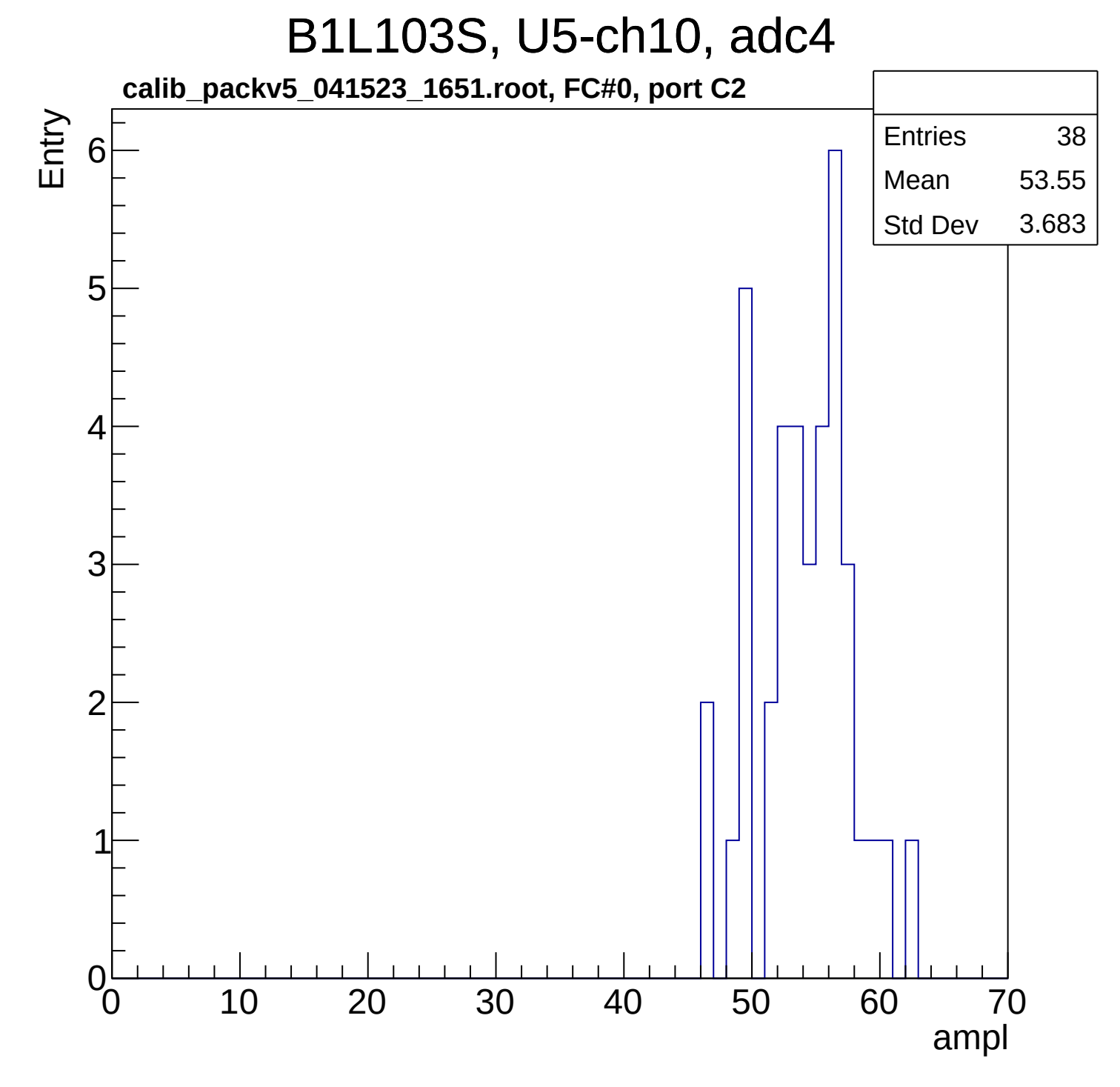
B1L103S, U5-ch10, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 53.55
Std Dev 3.683
Entry
ampl
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3
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0
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60
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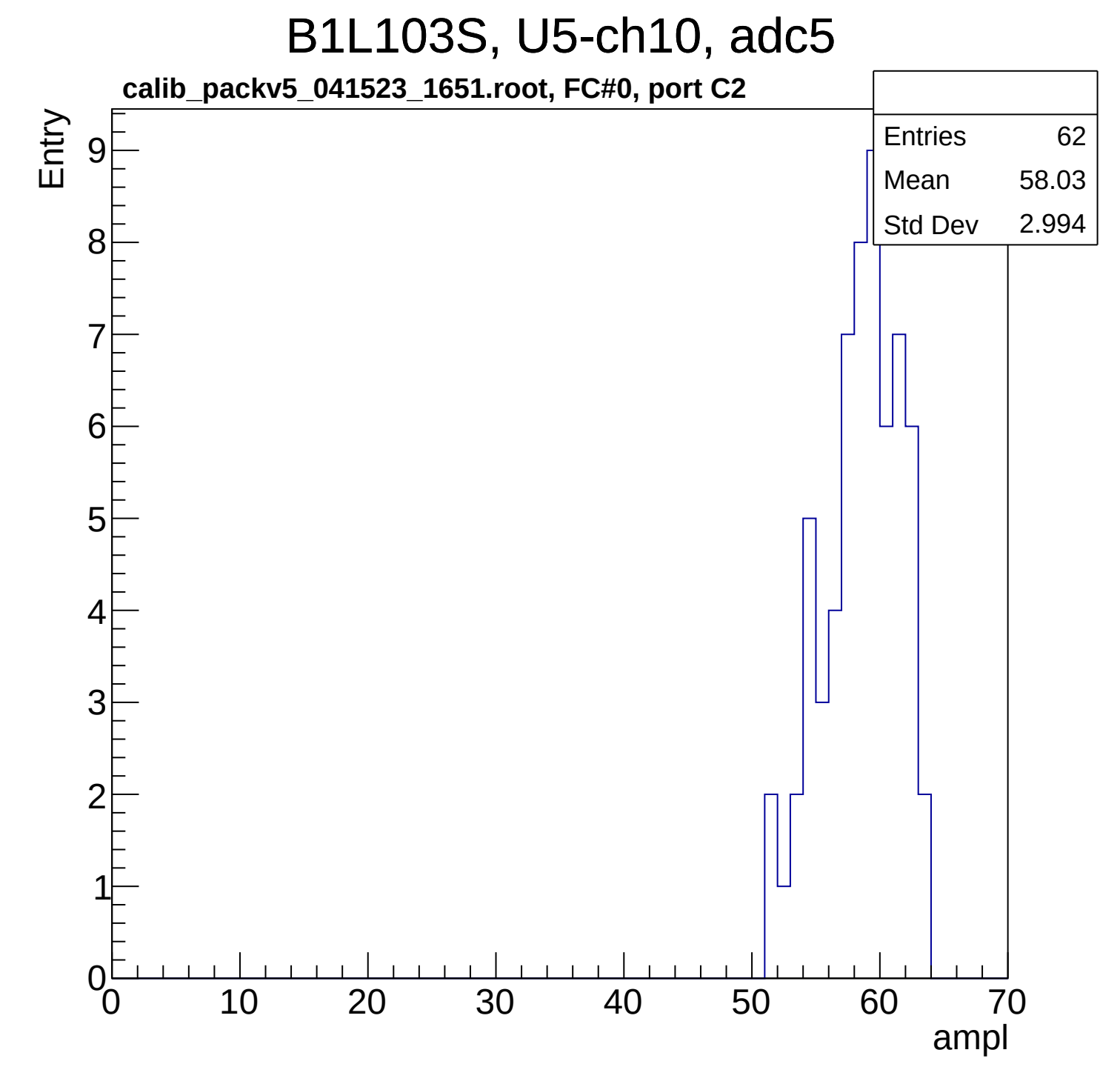
B1L103S, U5-ch10, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 58.03
Std Dev 2.994
Entry
ampl
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2
3
4
5
6
7
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0
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40
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60
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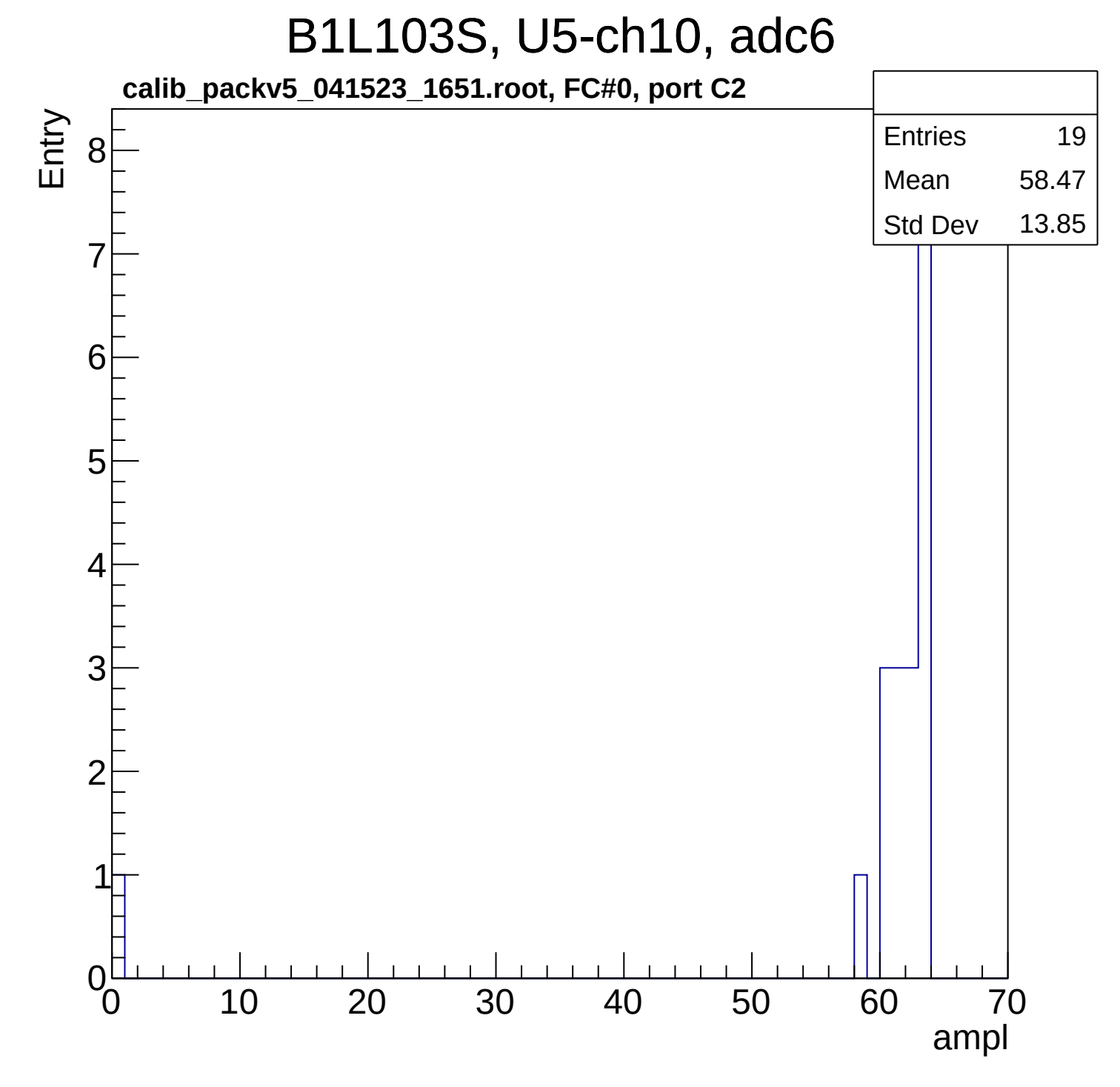
B1L103S, U5-ch10, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 58.47
Std Dev 13.85
Entry
ampl
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1
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3
4
5
6
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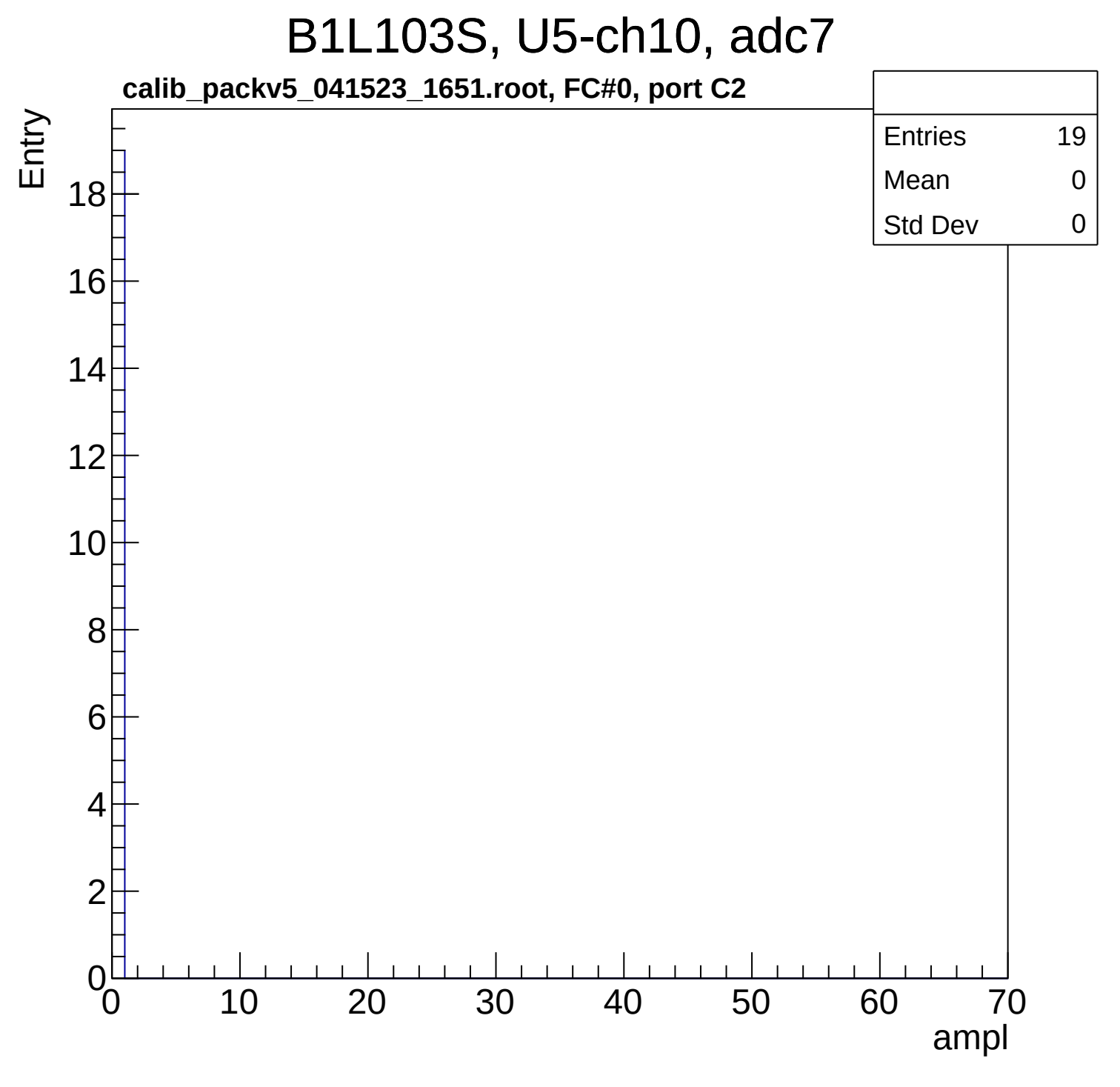
B1L103S, U5-ch10, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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4
6
8
10
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18
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10
20
30
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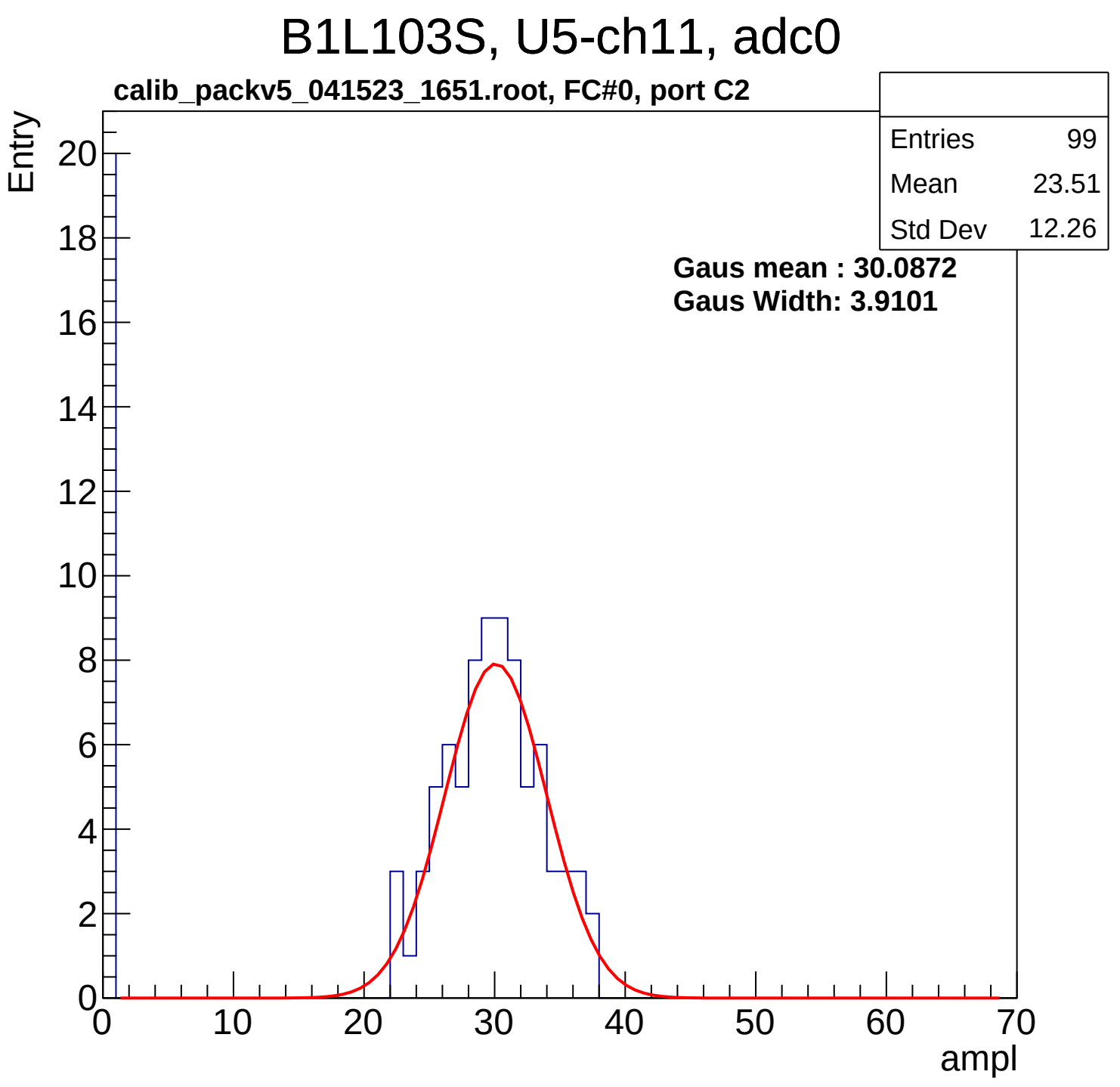
70
ampl


B1L103S, U5-ch11, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 23.51
Std Dev 12.26
Gaus mean : 30.0872
Gaus Width: 3.9101
Entry
ampl
0
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4
6
8
10
12
14
16
18
20
0
10
20
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60
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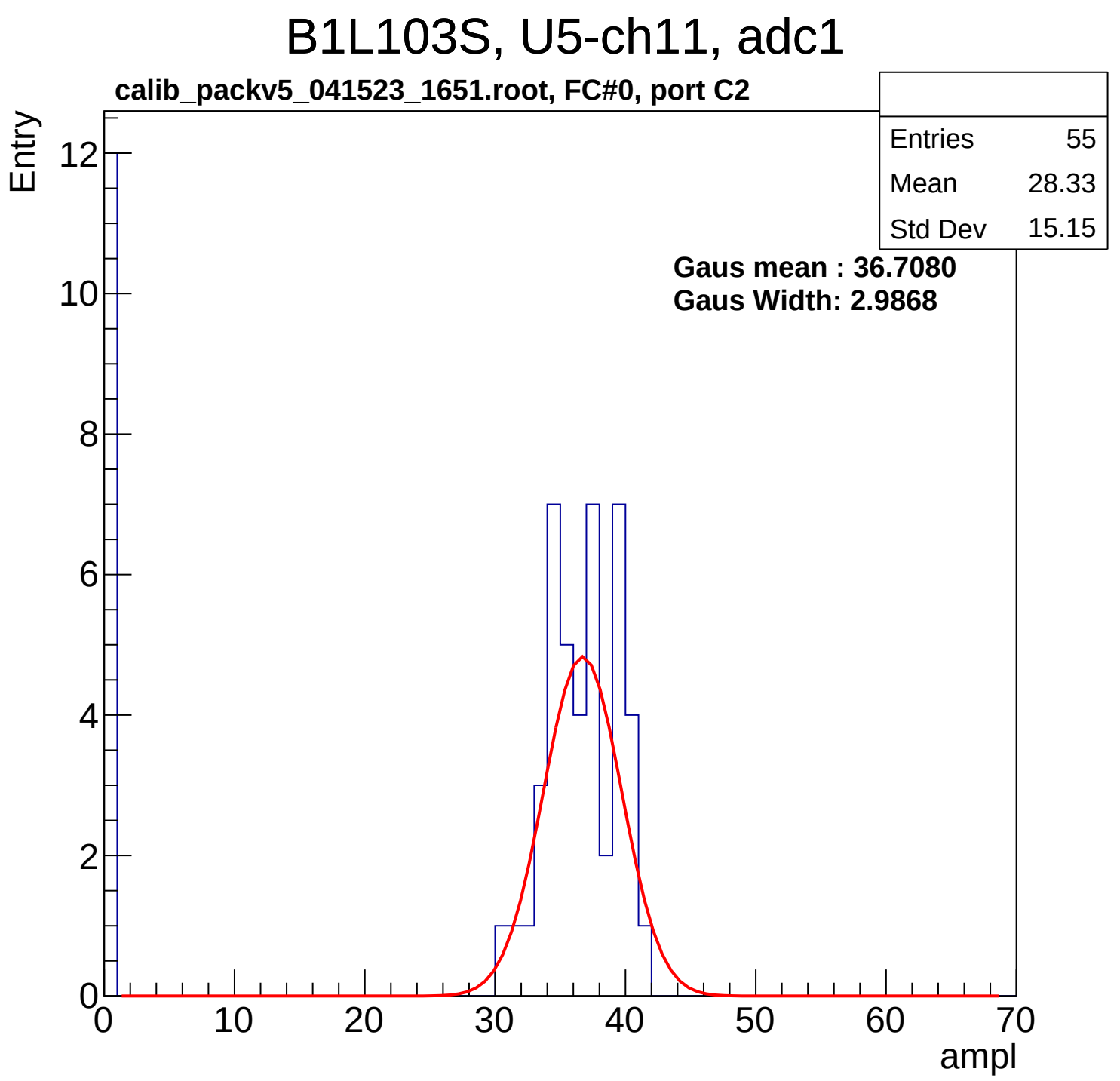
B1L103S, U5-ch11, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 28.33
Std Dev 15.15
Gaus mean : 36.7080
Gaus Width: 2.9868
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
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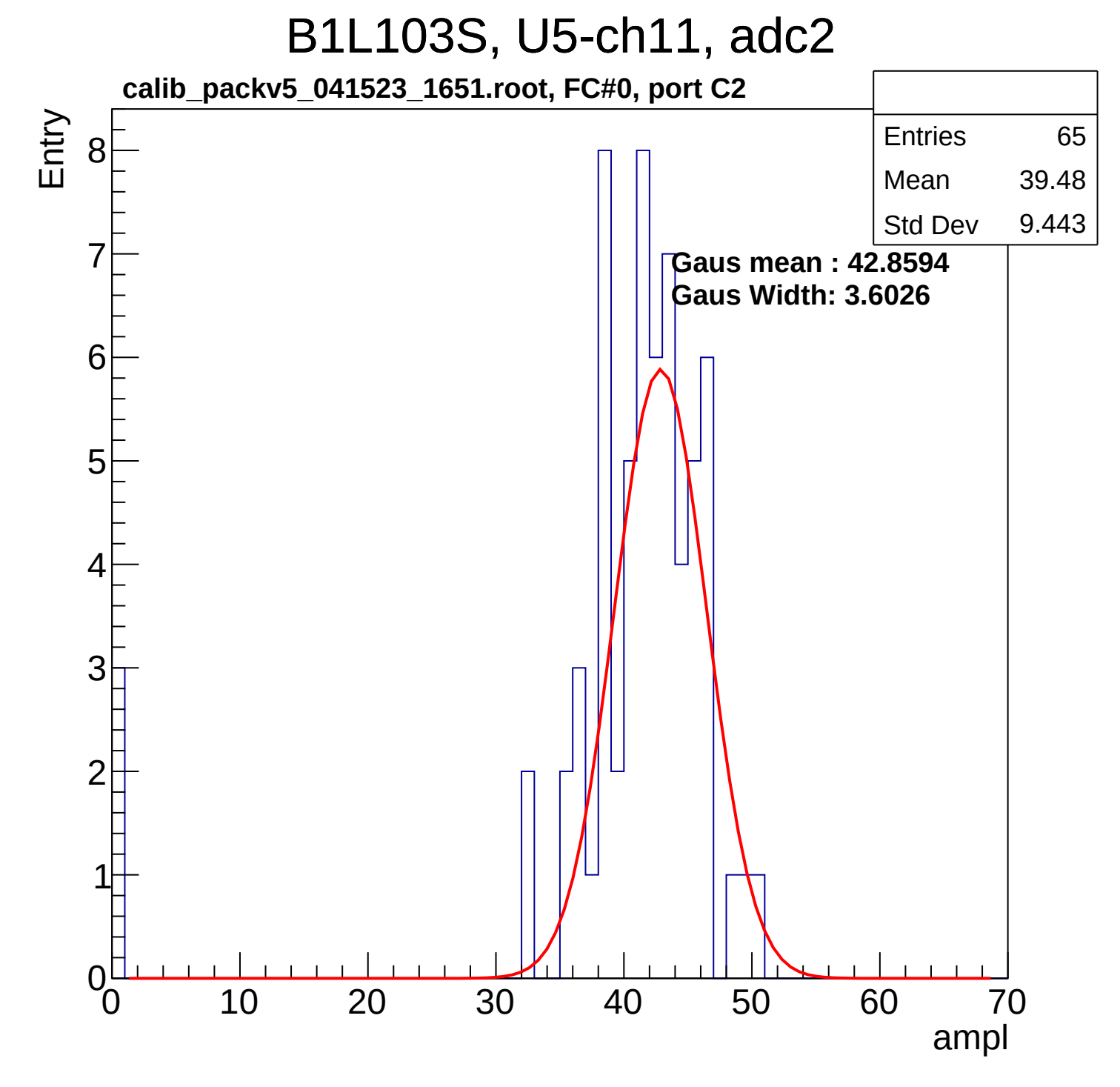
B1L103S, U5-ch11, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 39.48
Std Dev 9.443
Gaus mean : 42.8594
Gaus Width: 3.6026
Entry
ampl
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1
2
3
4
5
6
7
8
0
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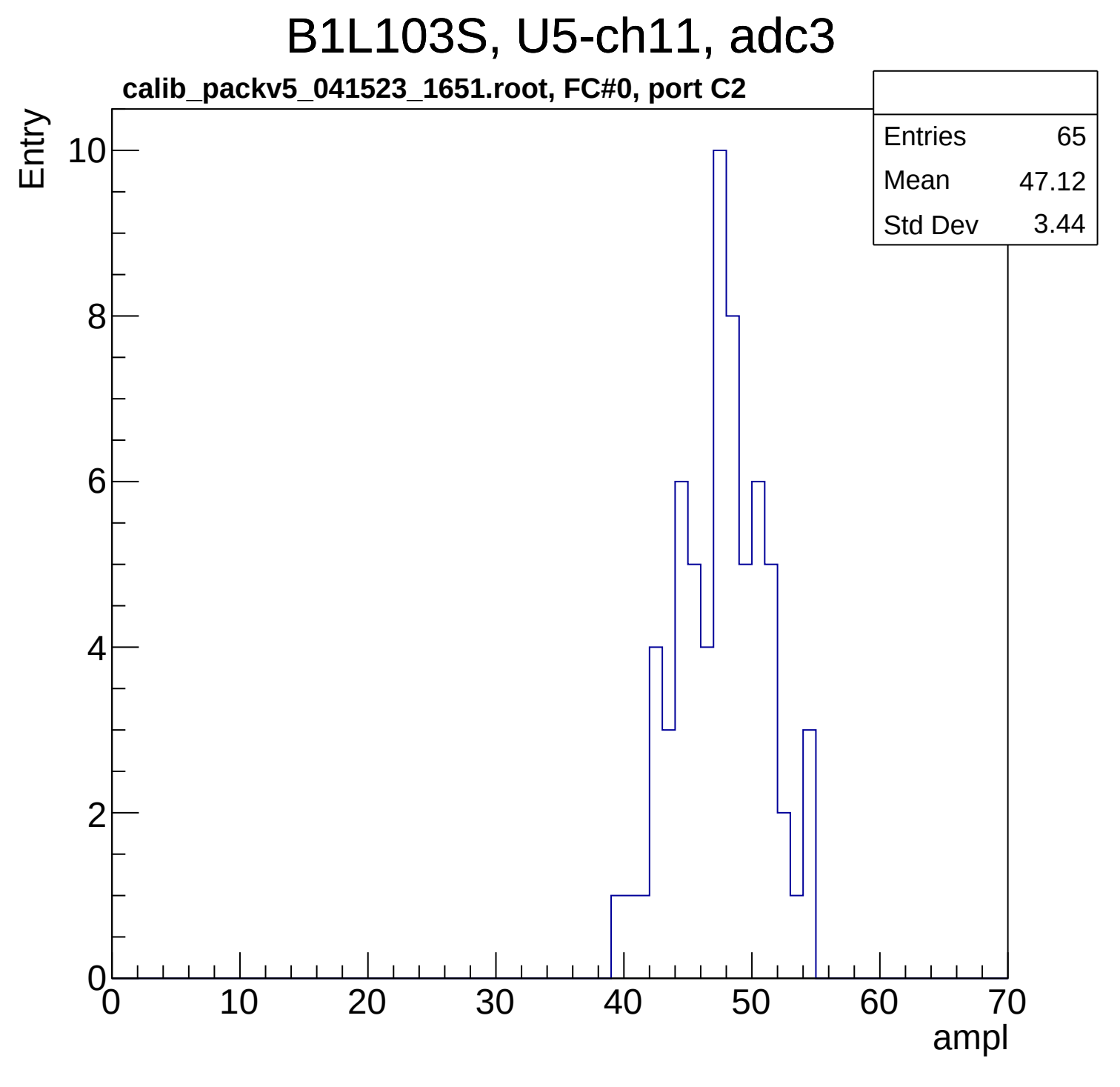
B1L103S, U5-ch11, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 47.12
Std Dev 3.44
Entry
ampl
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4
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40
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60
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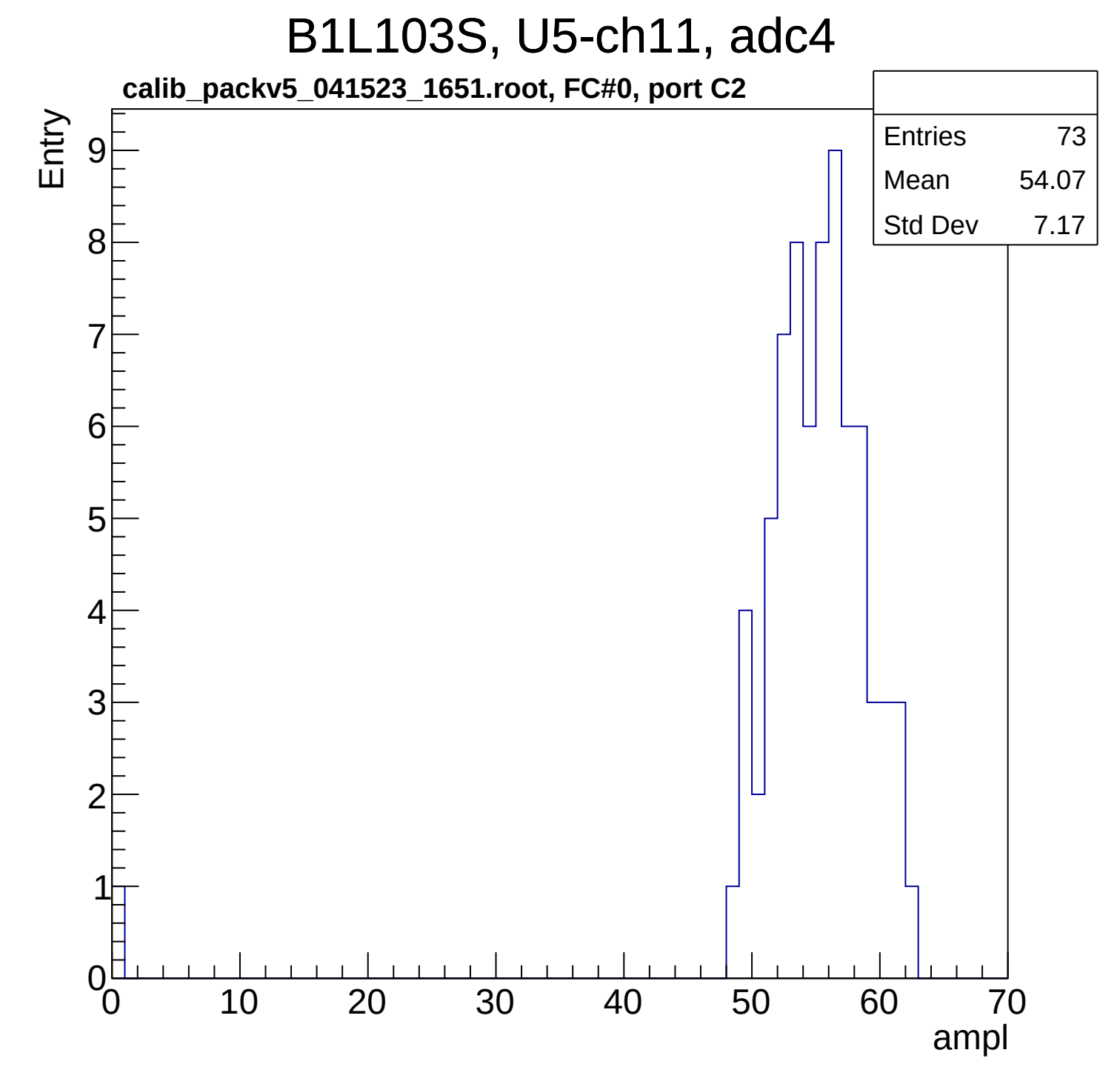
B1L103S, U5-ch11, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 54.07
Std Dev 7.17
Entry
ampl
0
1
2
3
4
5
6
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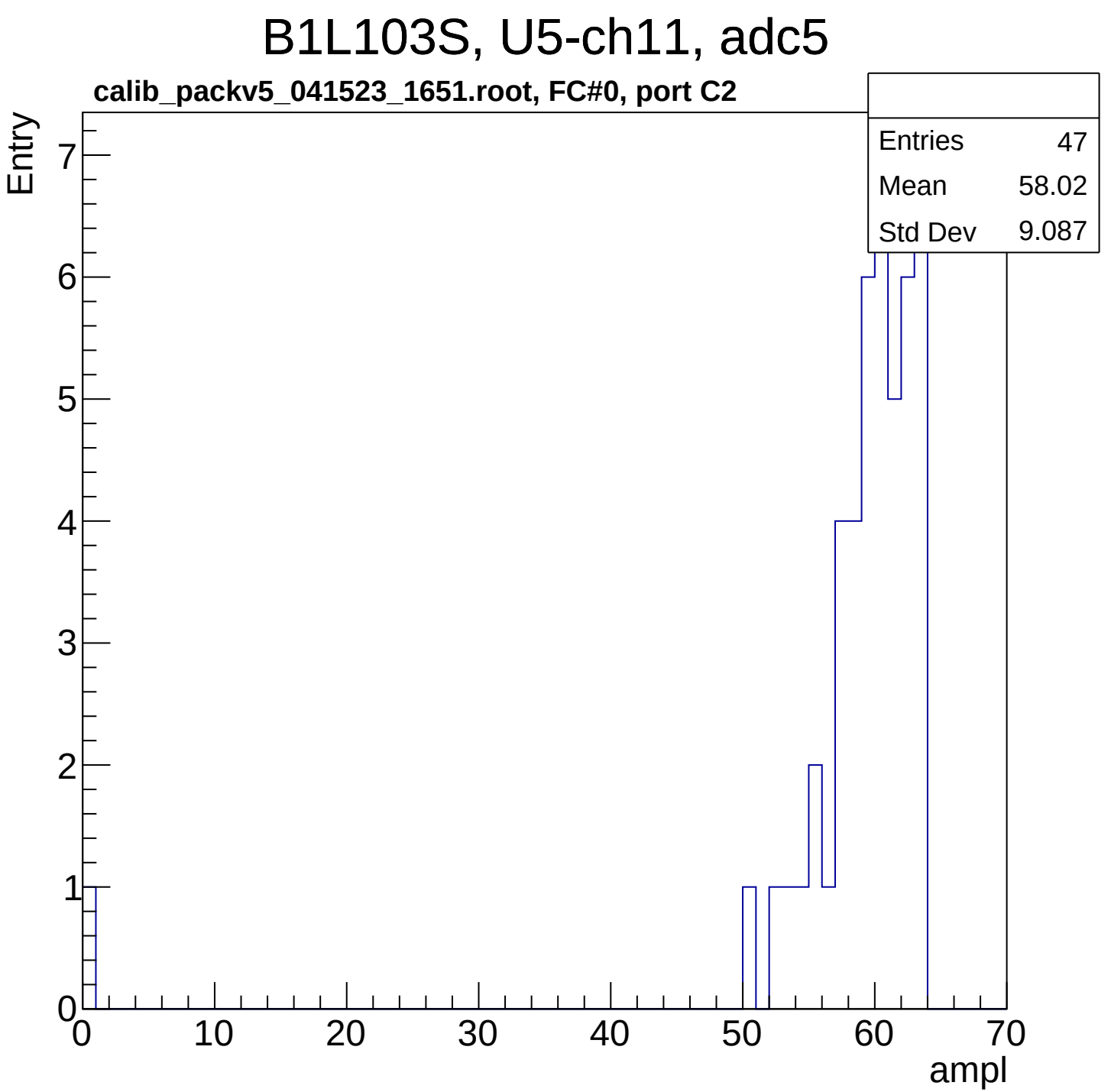
B1L103S, U5-ch11, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.02
Std Dev 9.087
Entry
ampl
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4
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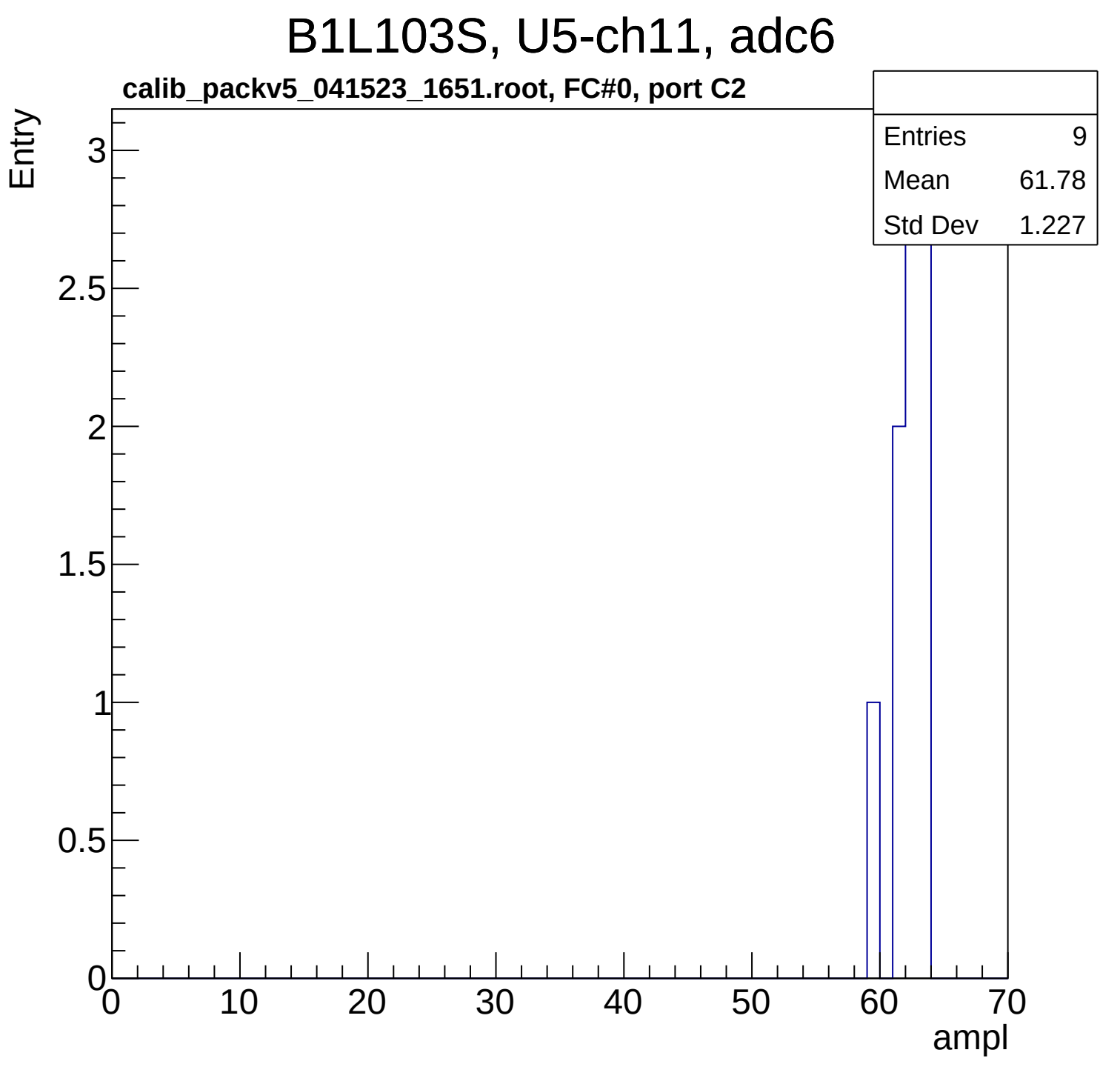
B1L103S, U5-ch11, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.78
Std Dev 1.227
Entry
ampl
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0.5
1
1.5
2
2.5
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0
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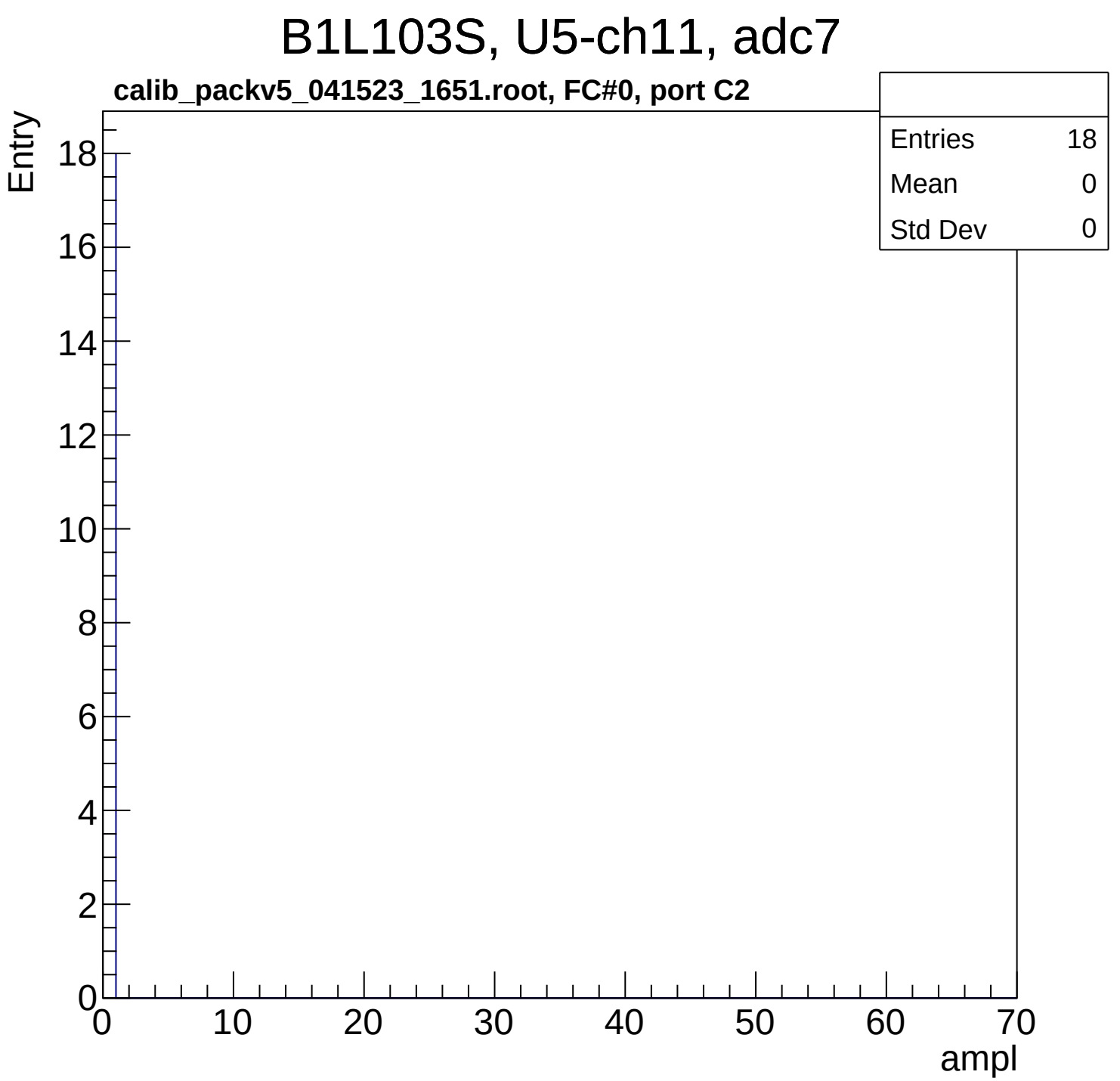
B1L103S, U5-ch11, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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2
4
6
8
10
12
14
16
18
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10
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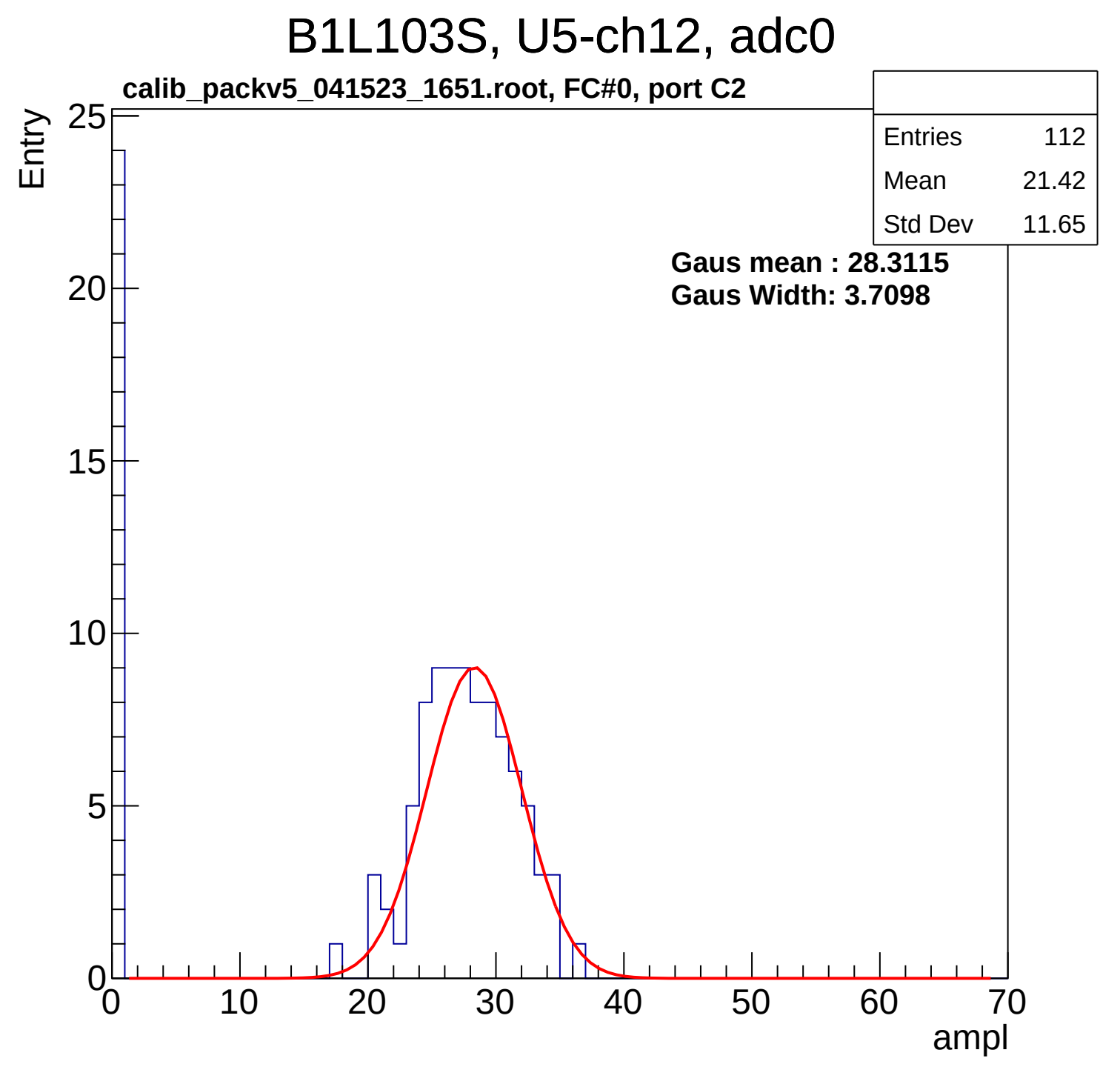
30
40
50
60
70
ampl


B1L103S, U5-ch12, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 112
Mean 21.42
Std Dev 11.65
Gaus mean : 28.3115
Gaus Width: 3.7098
Entry
ampl
0
5
10
15
20
25
0
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40
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60
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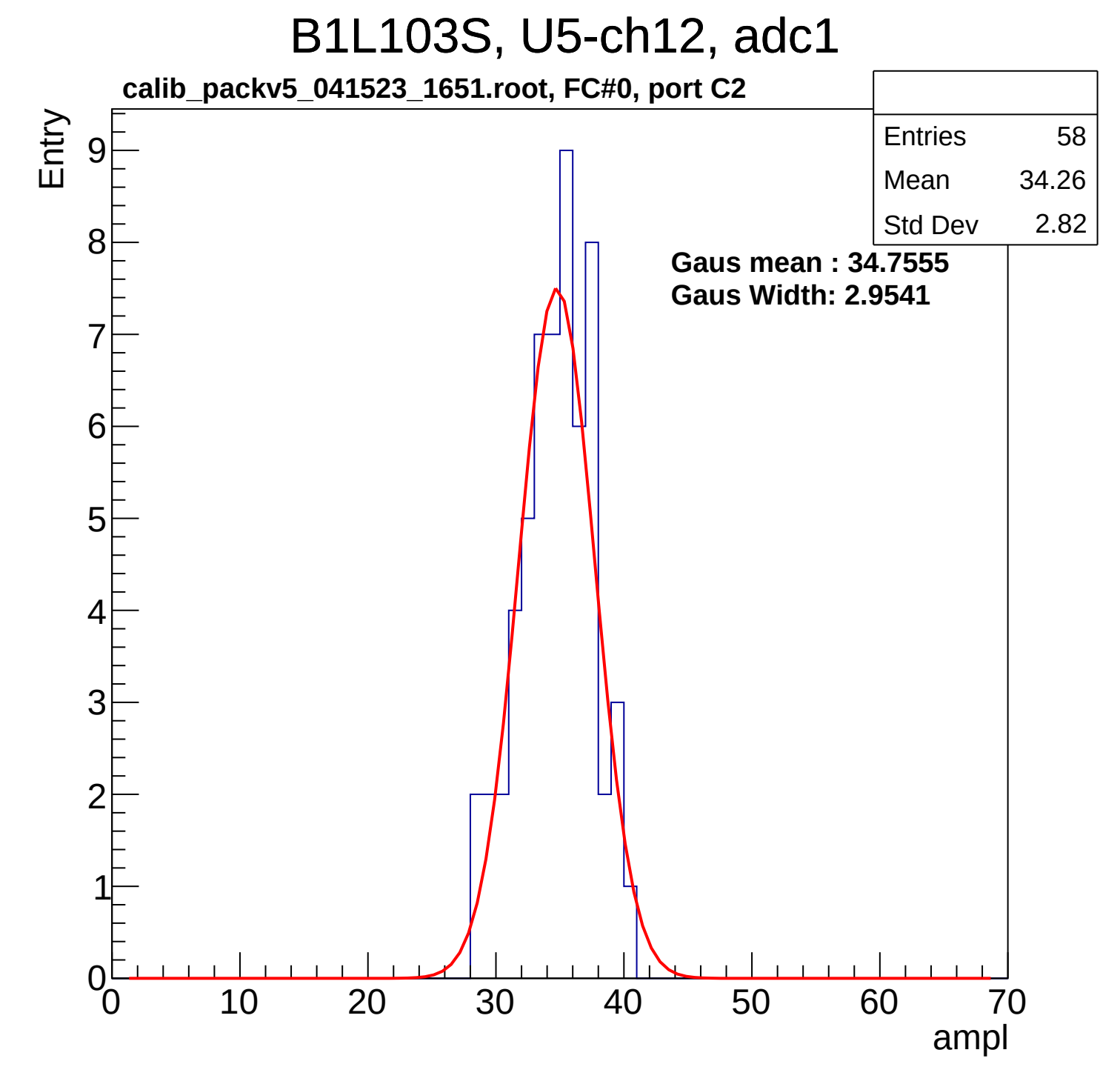
B1L103S, U5-ch12, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 34.26
Std Dev 2.82
Gaus mean : 34.7555
Gaus Width: 2.9541
Entry
ampl
0
10
20
30
40
50
60
70
1
2
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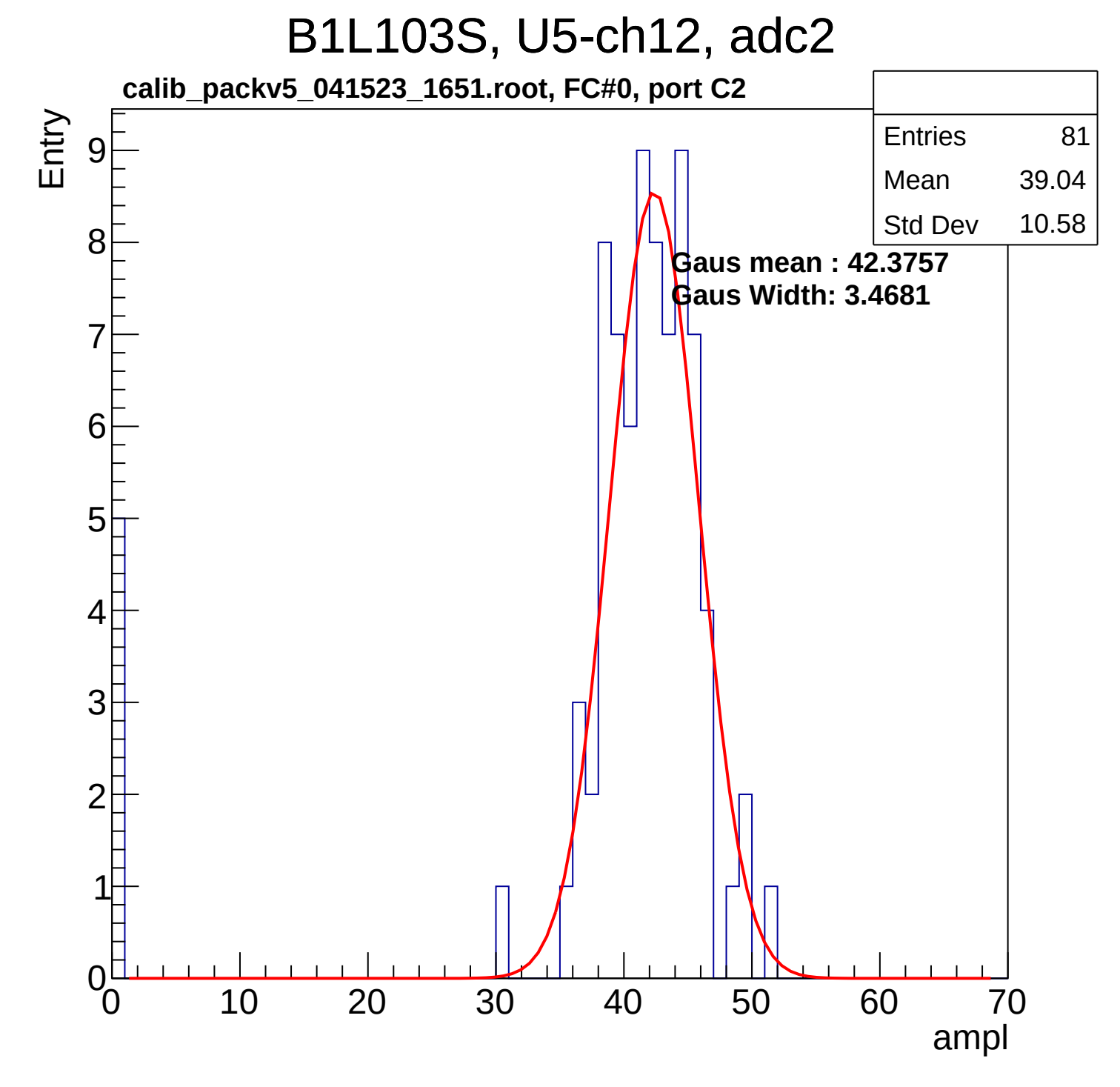
4
5
6
7
8
9


B1L103S, U5-ch12, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 39.04
Std Dev 10.58
Gaus mean : 42.3757
Gaus Width: 3.4681
Entry
ampl
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2
3
4
5
6
7
8
9
0
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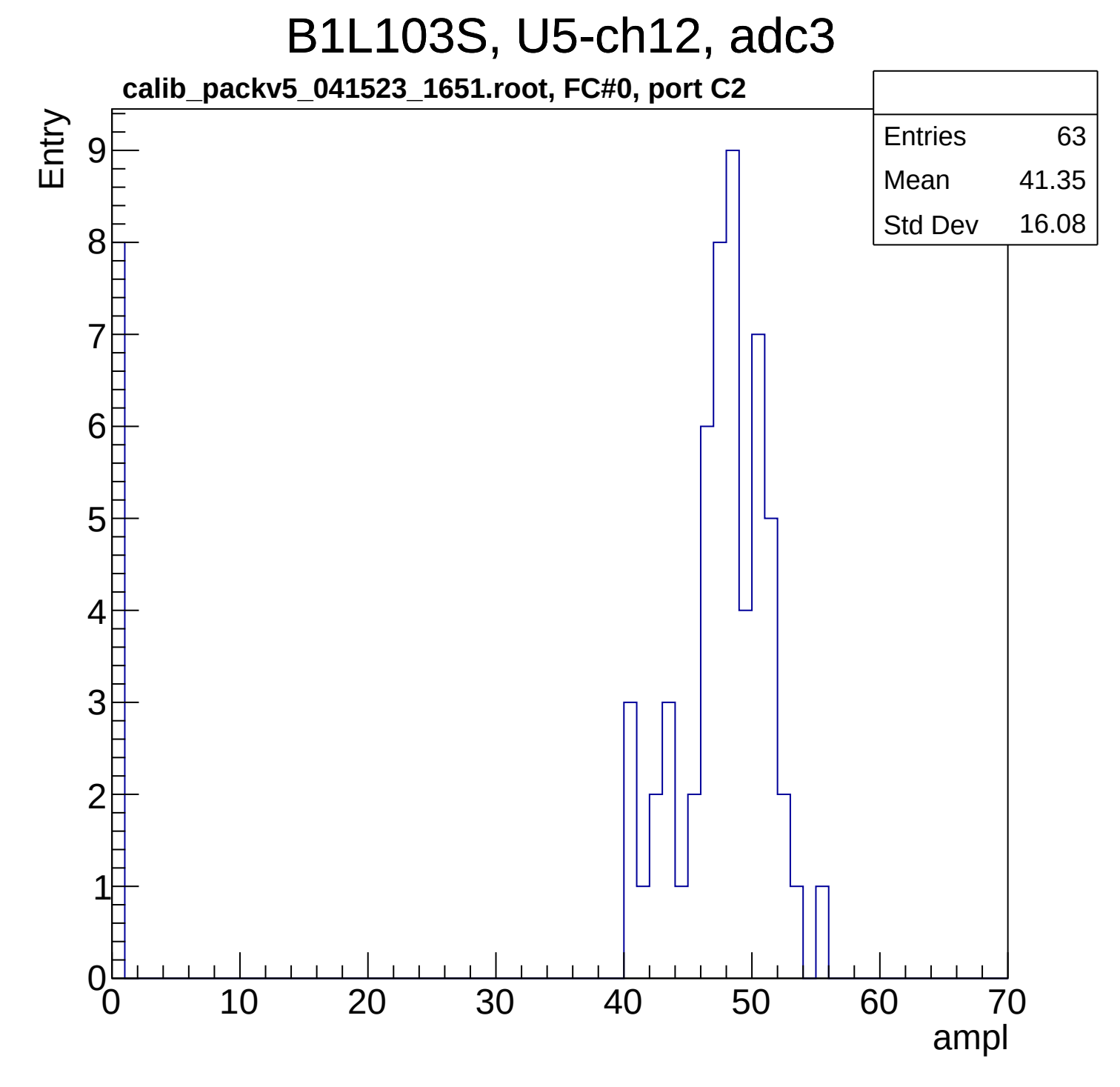
B1L103S, U5-ch12, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 41.35
Std Dev 16.08
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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60
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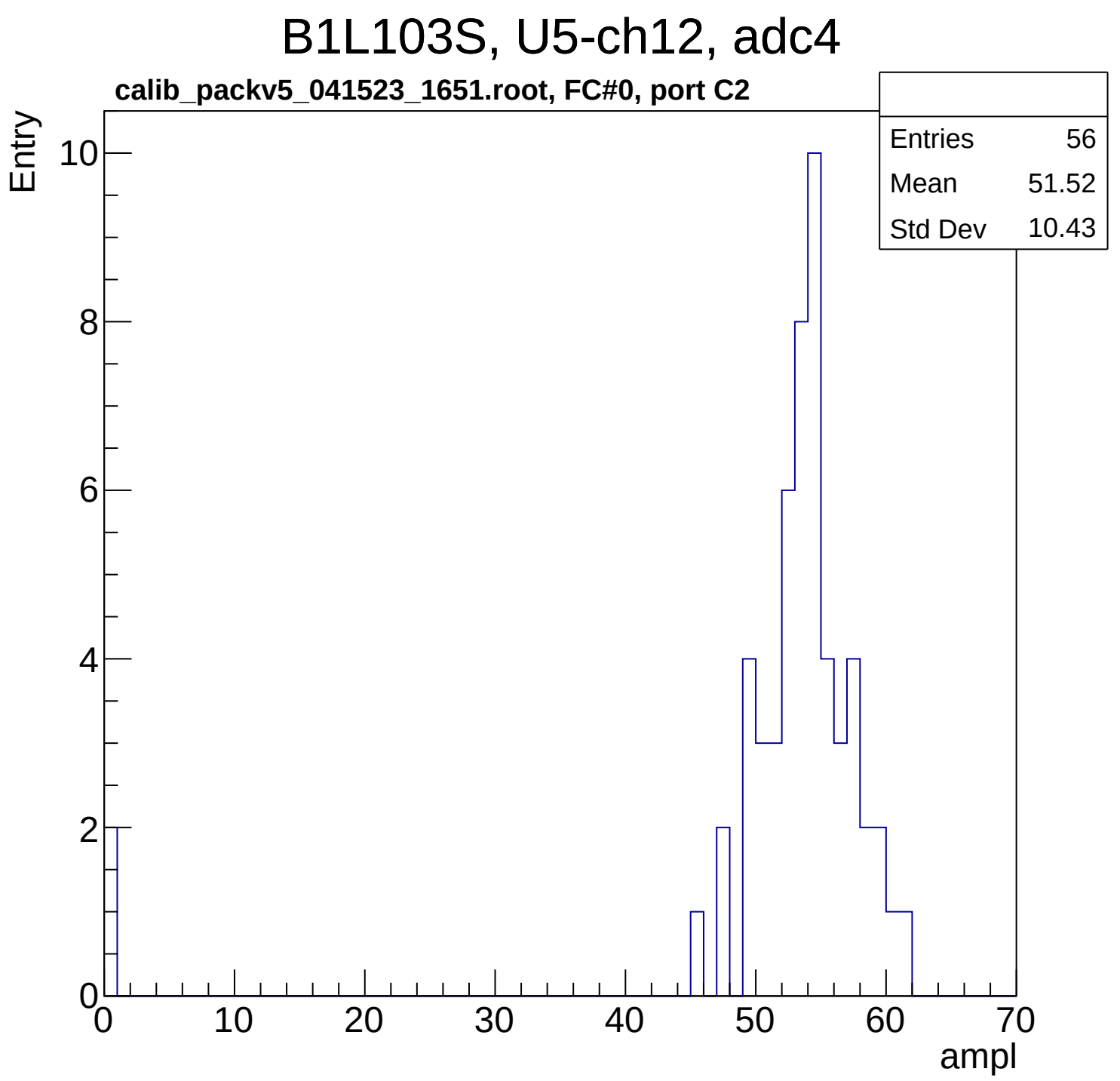
B1L103S, U5-ch12, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 51.52
Std Dev 10.43
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
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60
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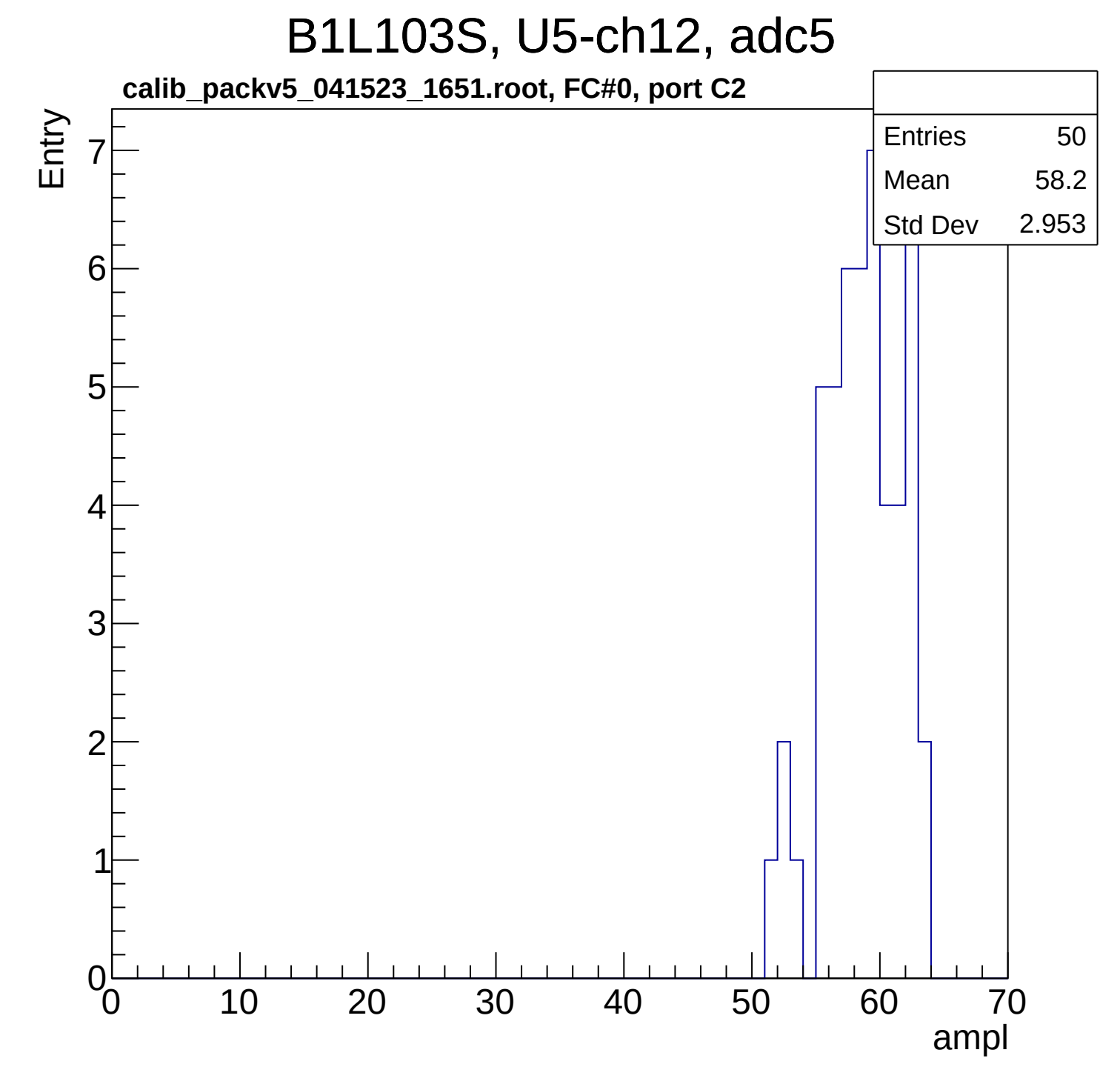
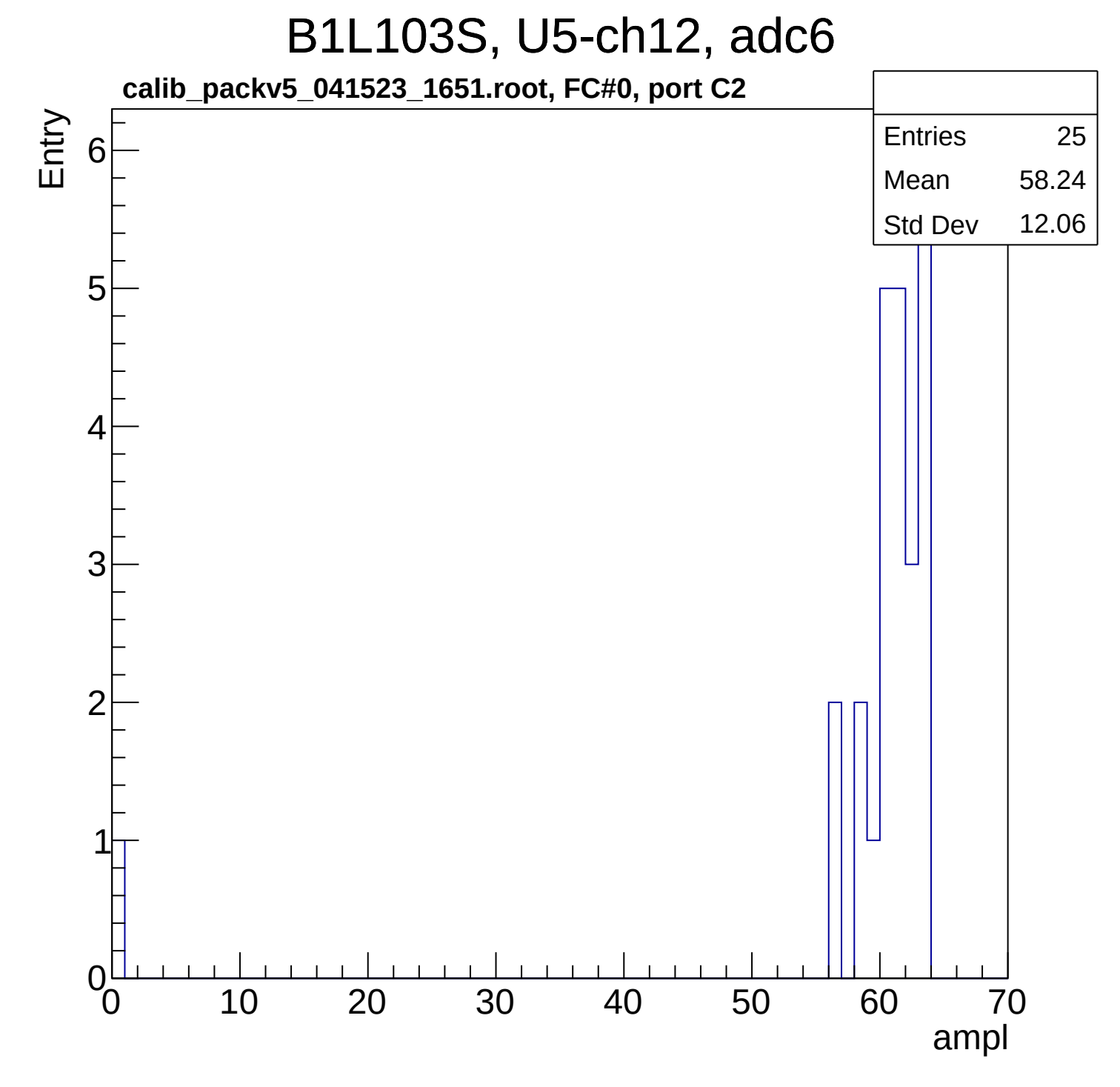
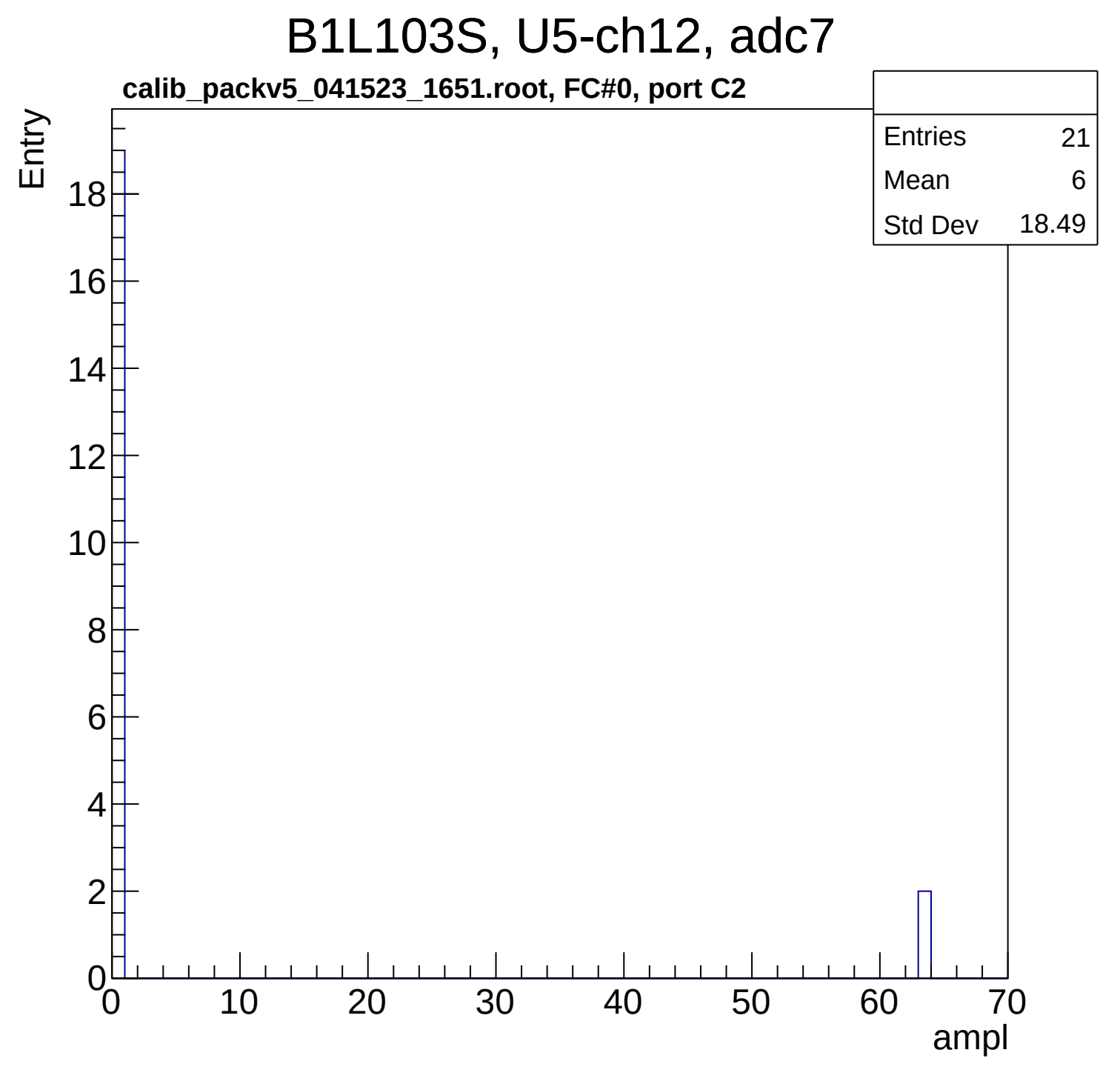

B1L103S, U5-ch12, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.2
Std Dev 2.953
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U5-ch12, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 58.24
Std Dev 12.06
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U5-ch12, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
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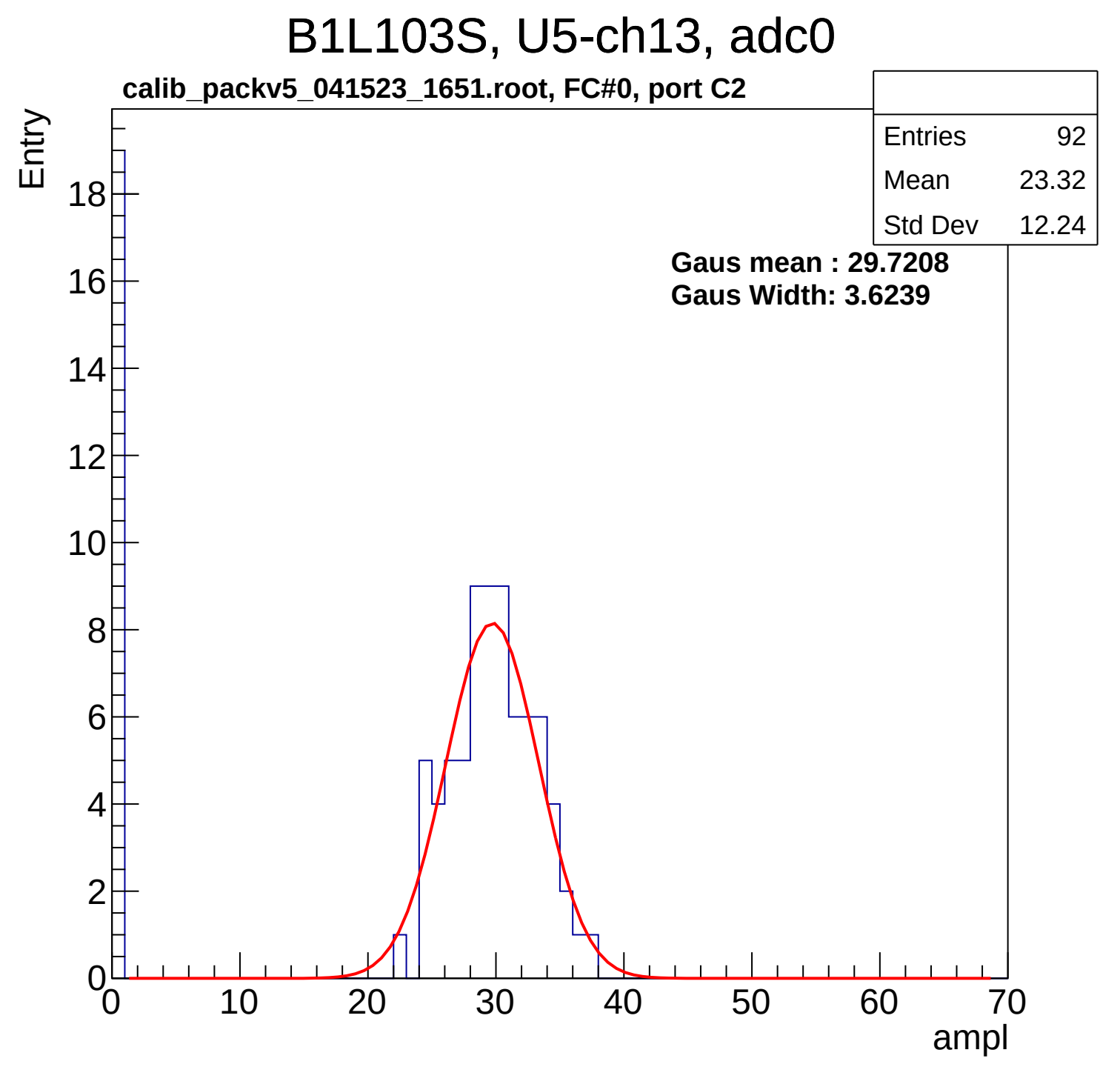
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch13, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 23.32
Std Dev 12.24
Gaus mean : 29.7208
Gaus Width: 3.6239
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
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40
50
60
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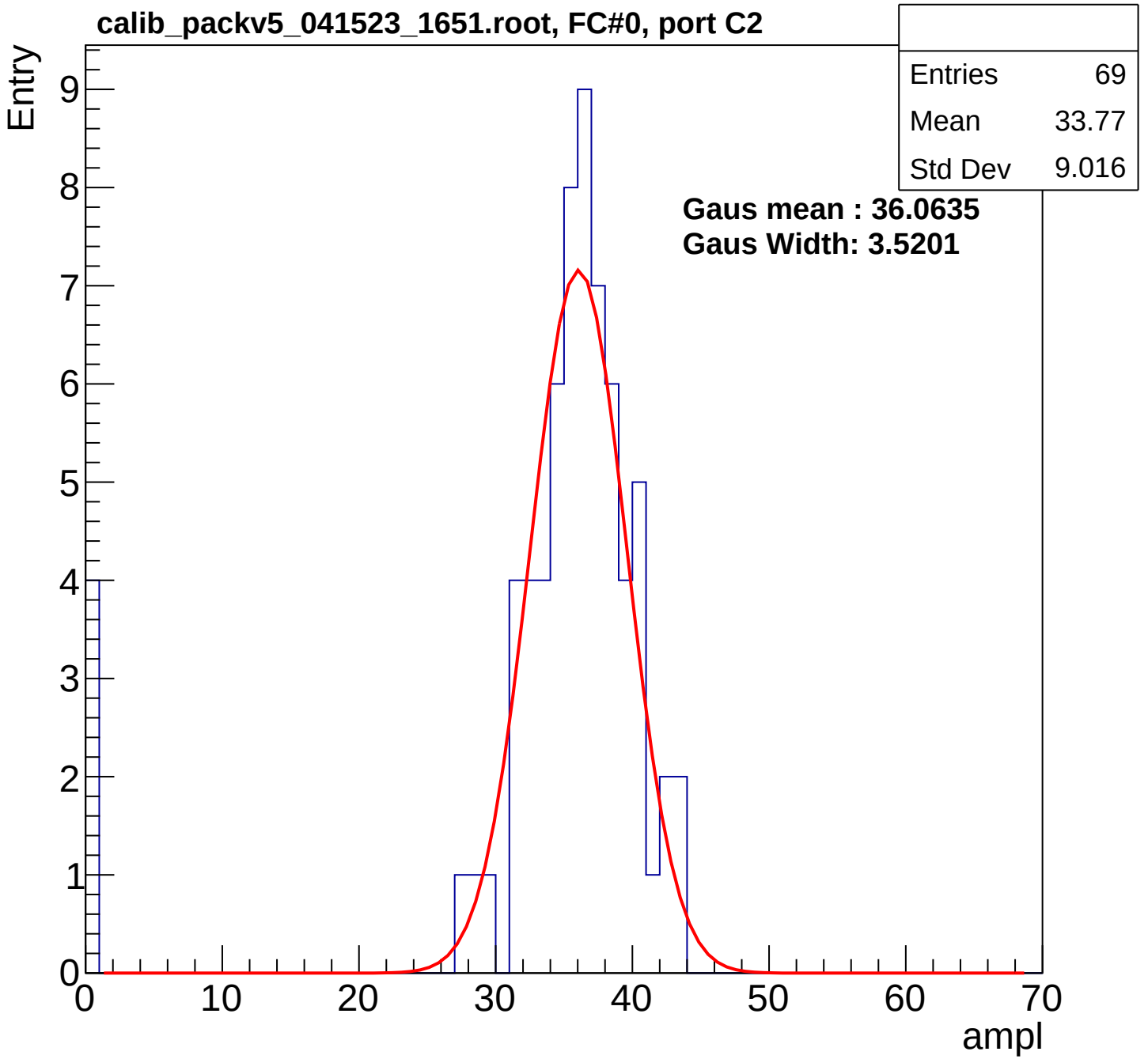
B1L103S, U5-ch13, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 33.77
Std Dev 9.016
Gaus mean : 36.0635
Gaus Width: 3.5201
Entry
ampl
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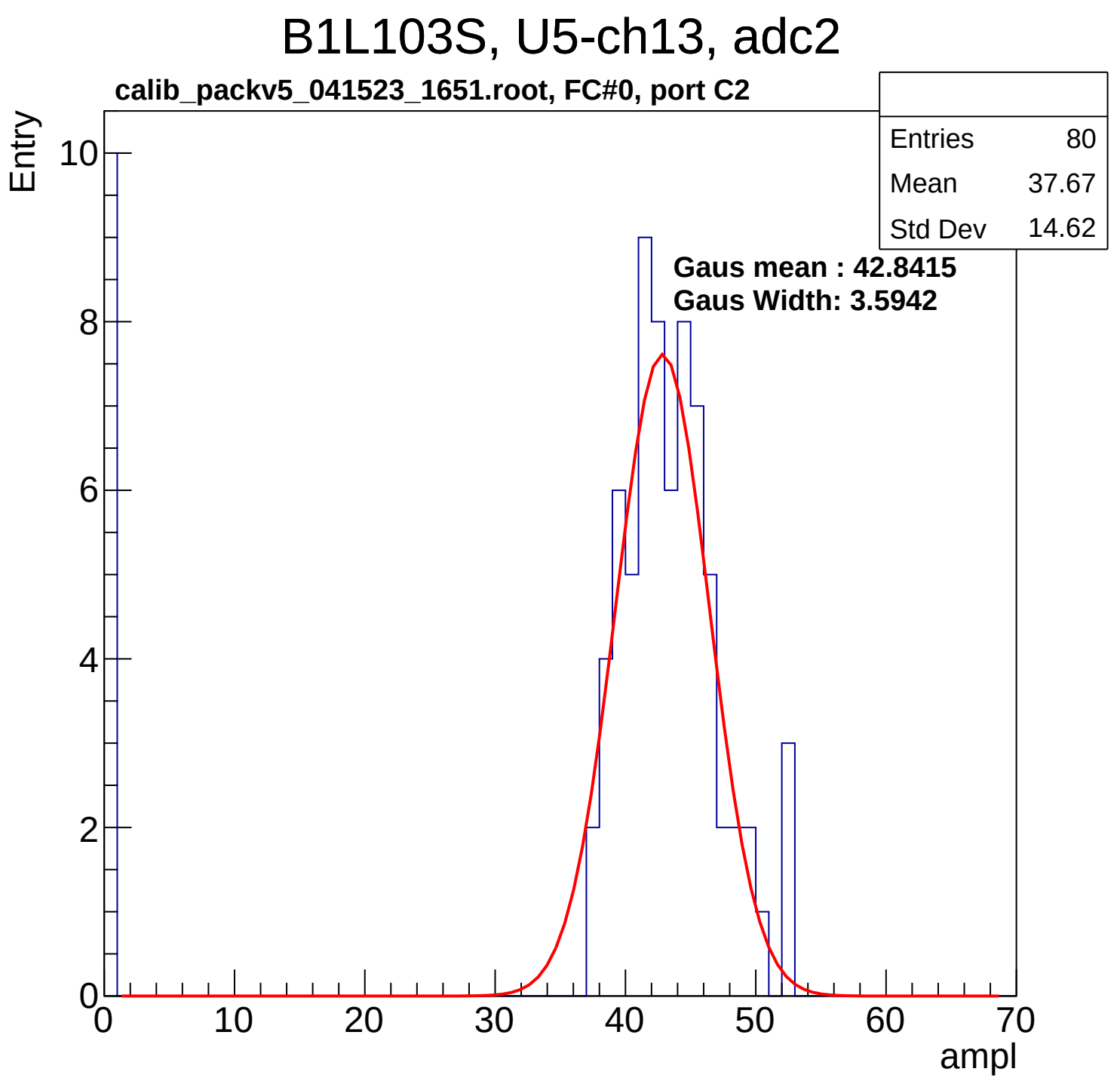
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U5-ch13, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 37.67
Std Dev 14.62
Gaus mean : 42.8415
Gaus Width: 3.5942
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
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60
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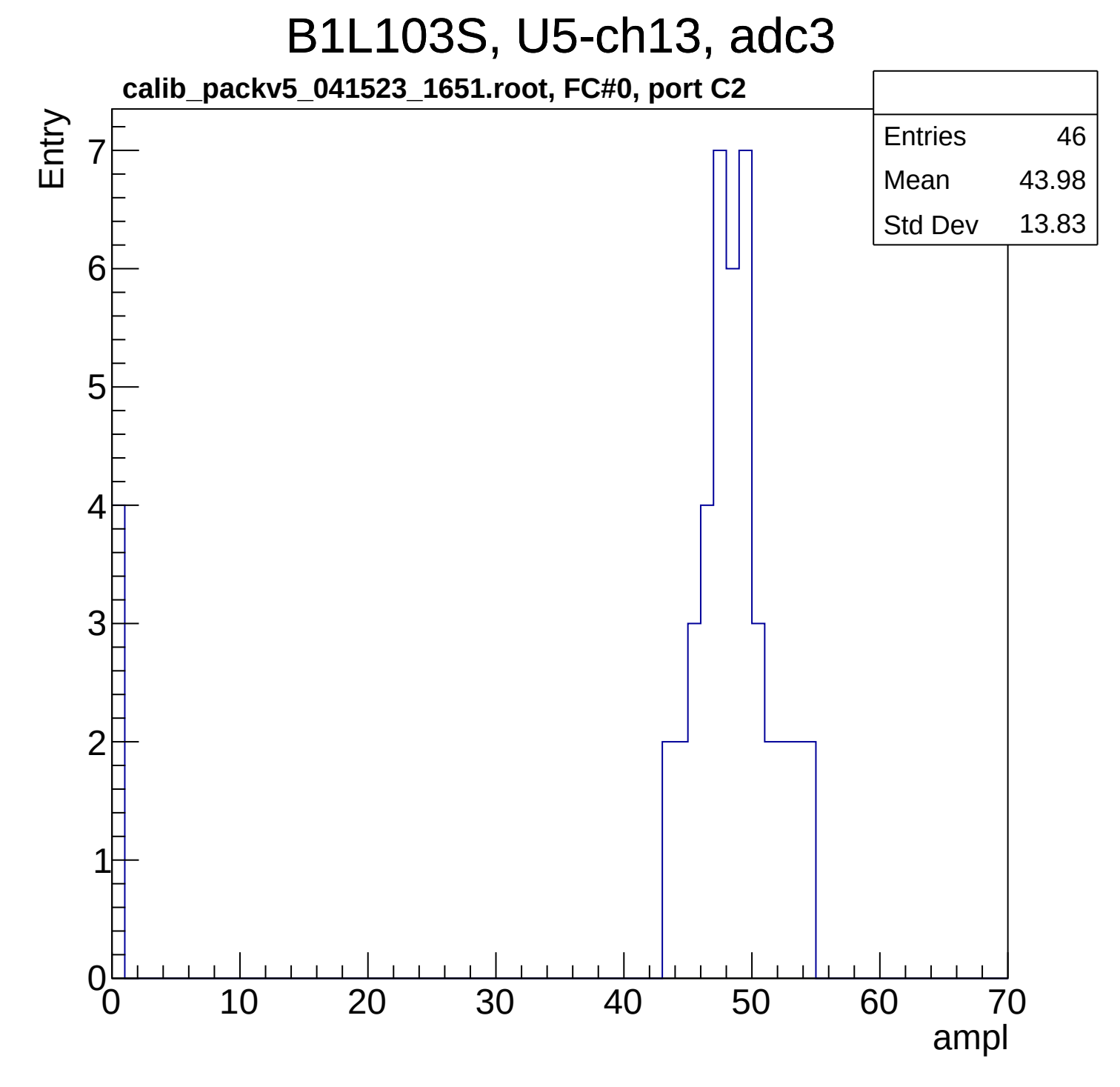
B1L103S, U5-ch13, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 43.98
Std Dev 13.83
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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40
50
60
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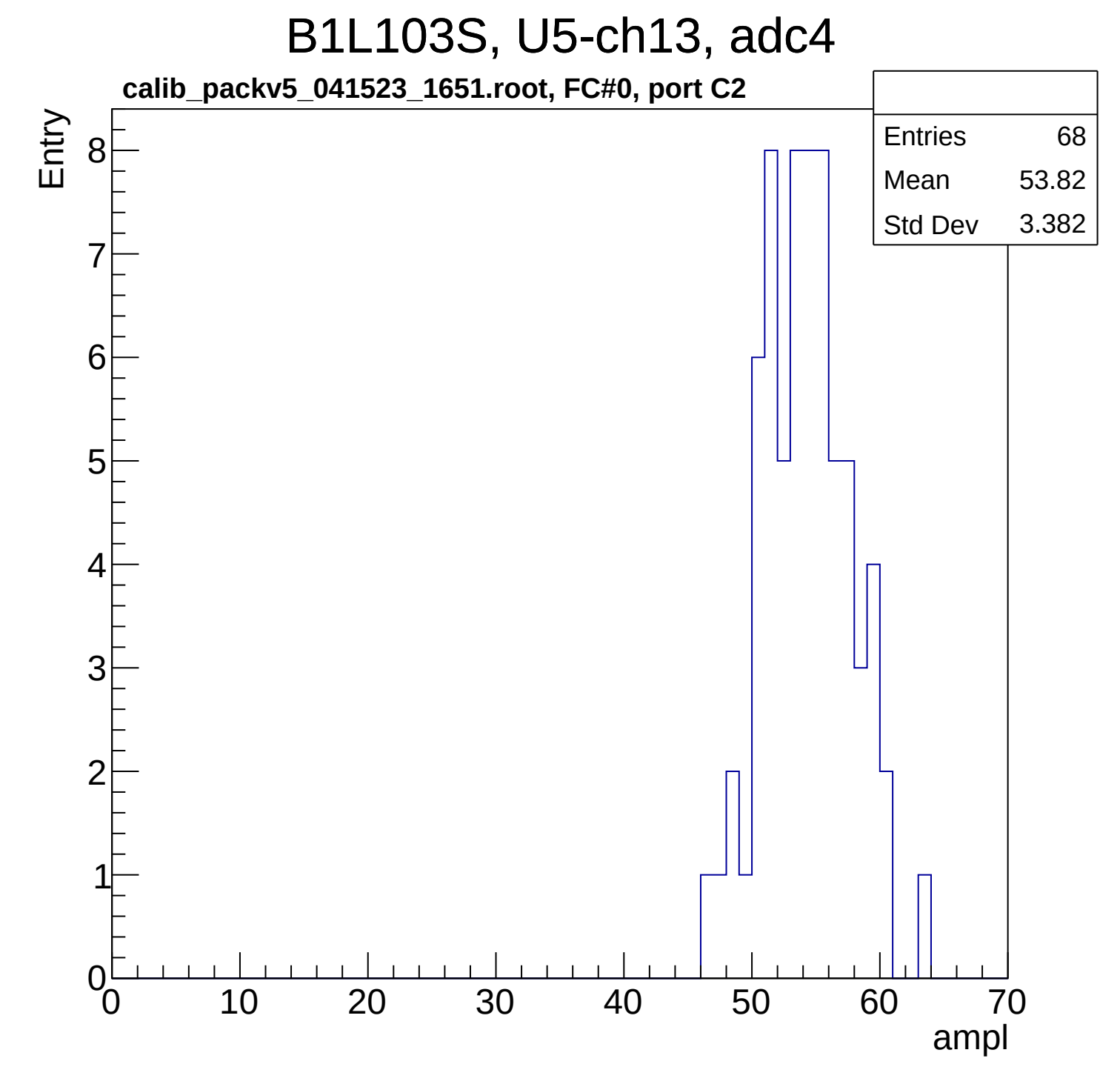
B1L103S, U5-ch13, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 53.82
Std Dev 3.382
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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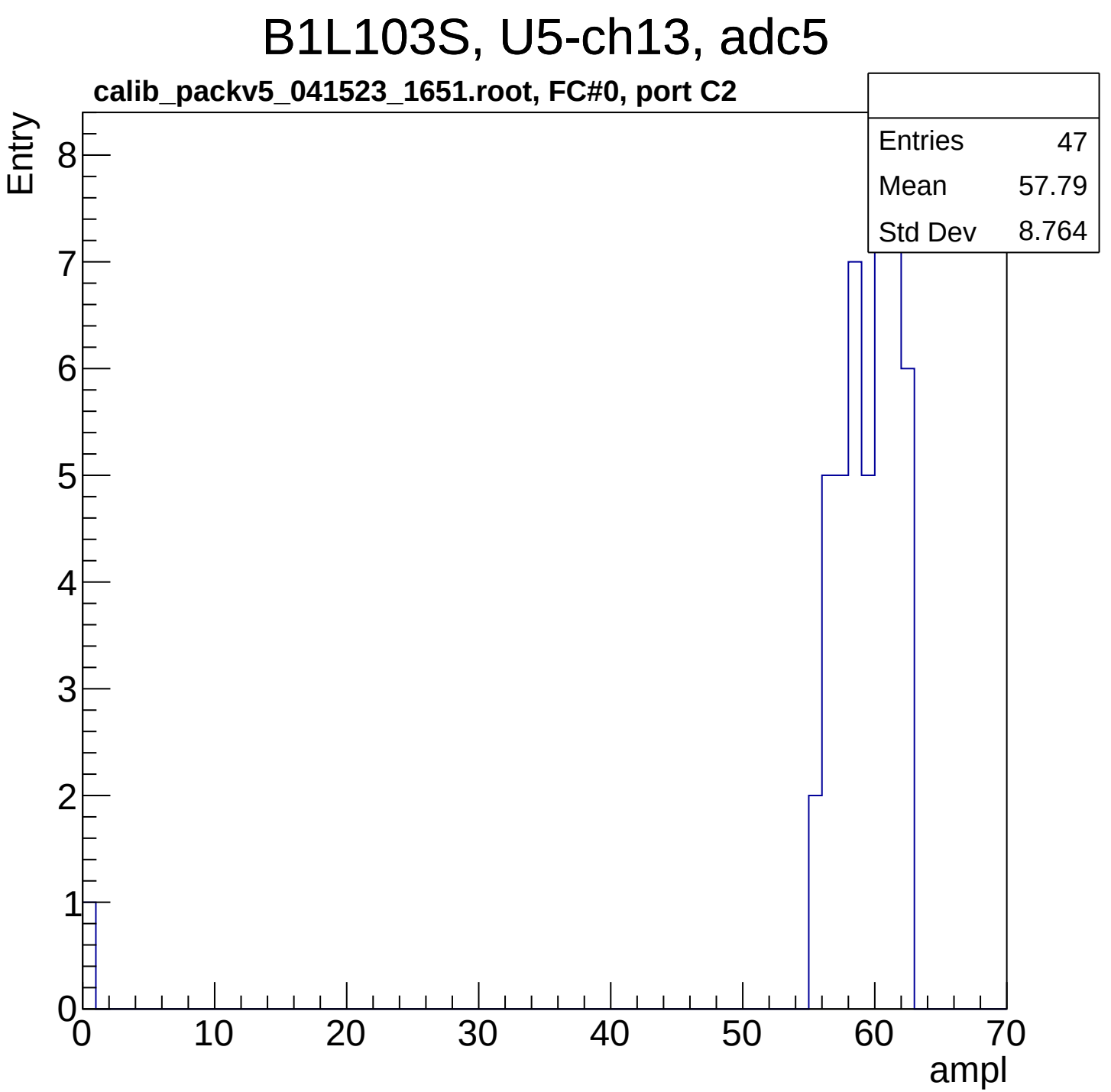
B1L103S, U5-ch13, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 57.79
Std Dev 8.764
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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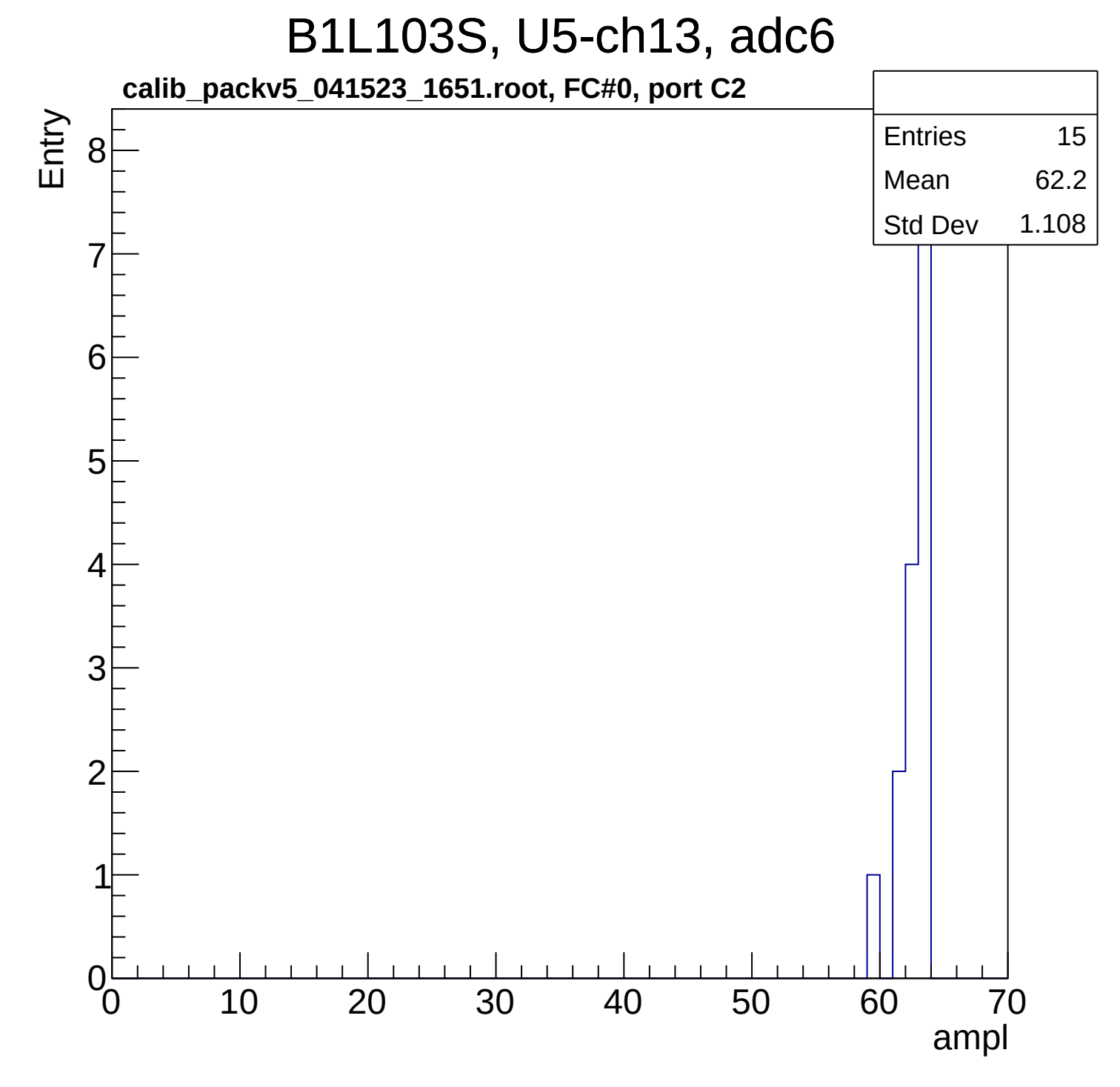
B1L103S, U5-ch13, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 62.2
Std Dev 1.108
Entry
ampl
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2
3
4
5
6
7
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0
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20
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60
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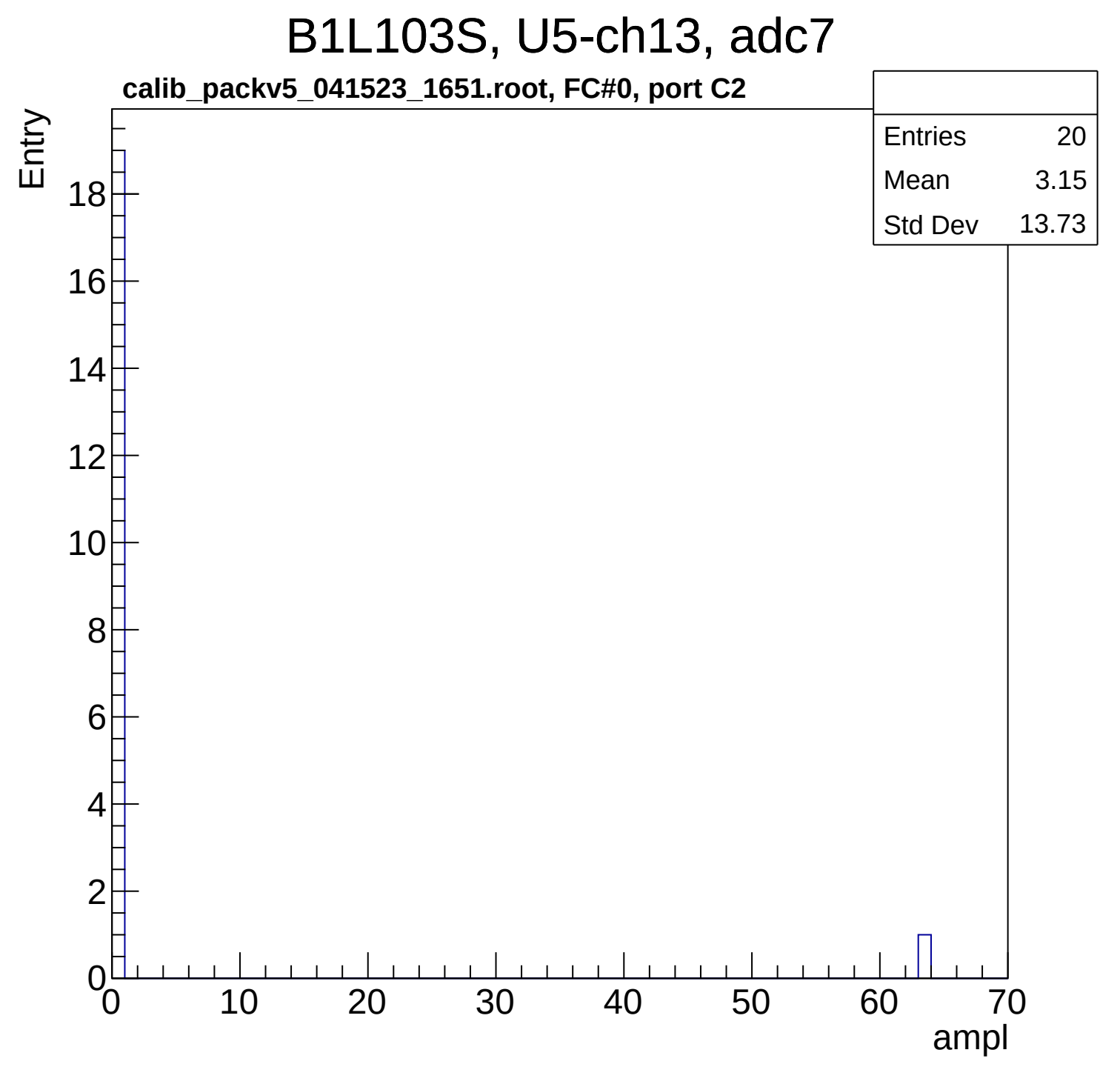
B1L103S, U5-ch13, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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6
8
10
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14
16
18
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10
20
30
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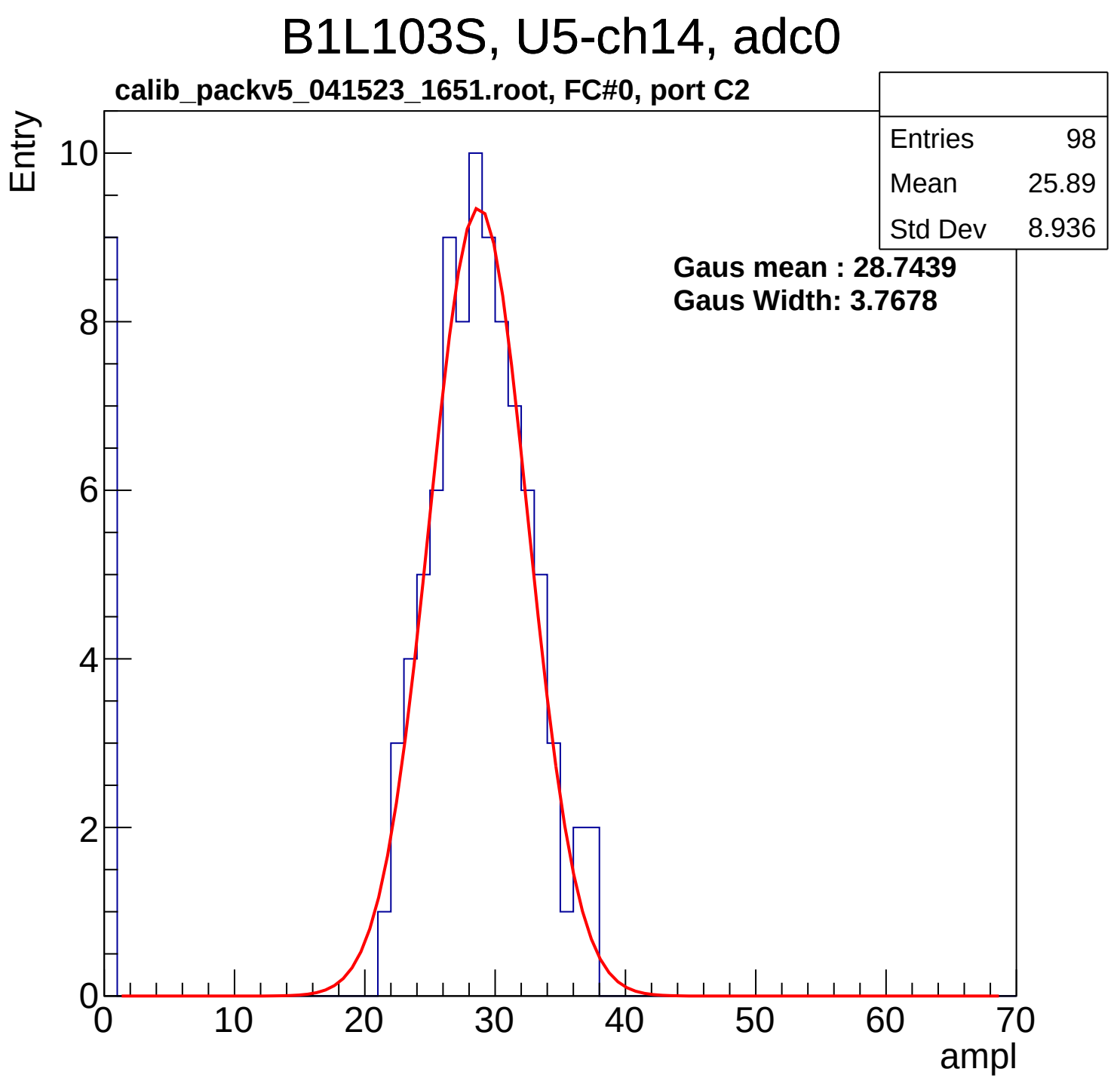
50
60
70
ampl


B1L103S, U5-ch14, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 25.89
Std Dev 8.936
Gaus mean : 28.7439
Gaus Width: 3.7678
Entry
ampl
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6
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0
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60
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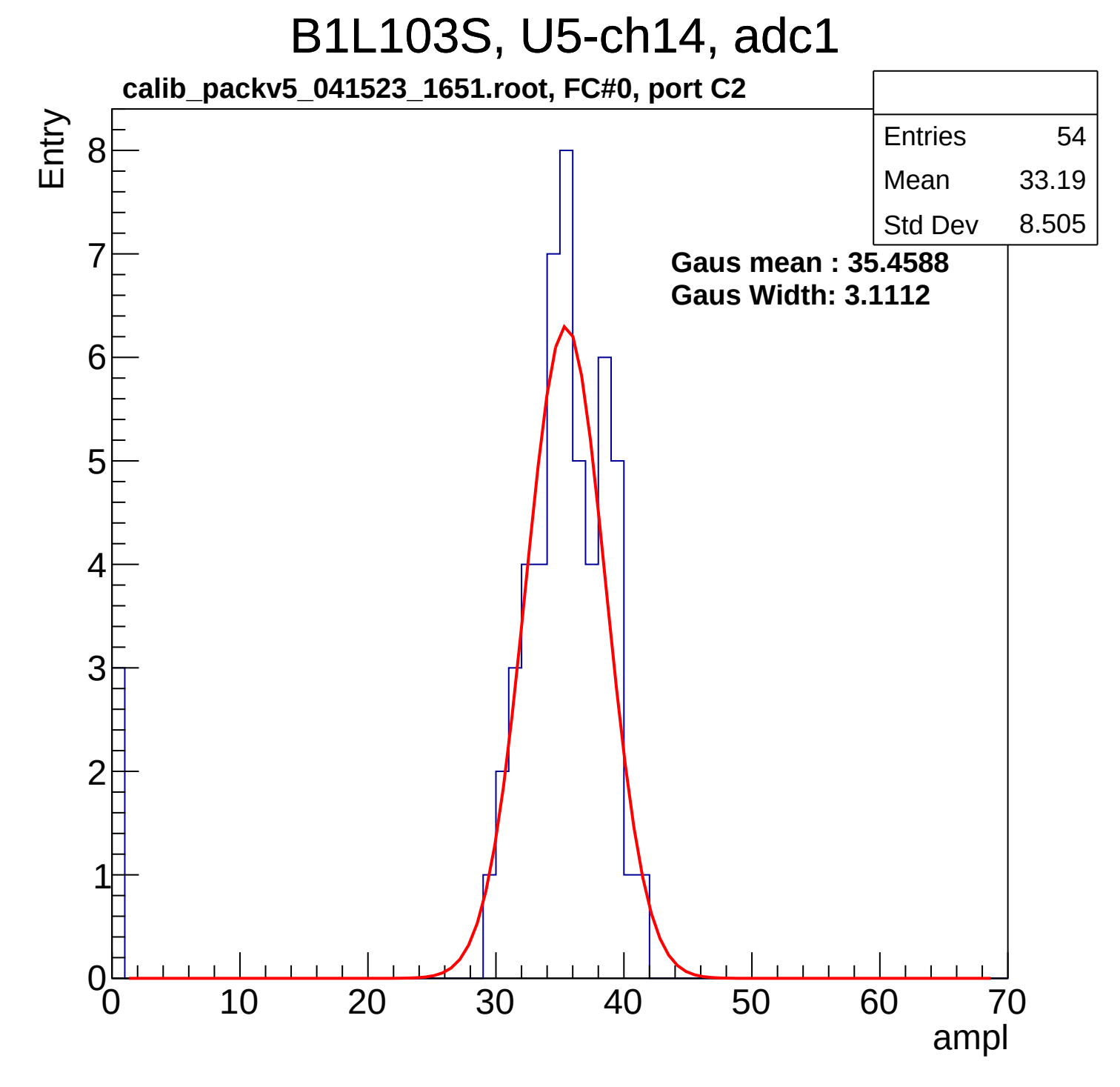
B1L103S, U5-ch14, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 33.19
Std Dev 8.505
Gaus mean : 35.4588
Gaus Width: 3.1112
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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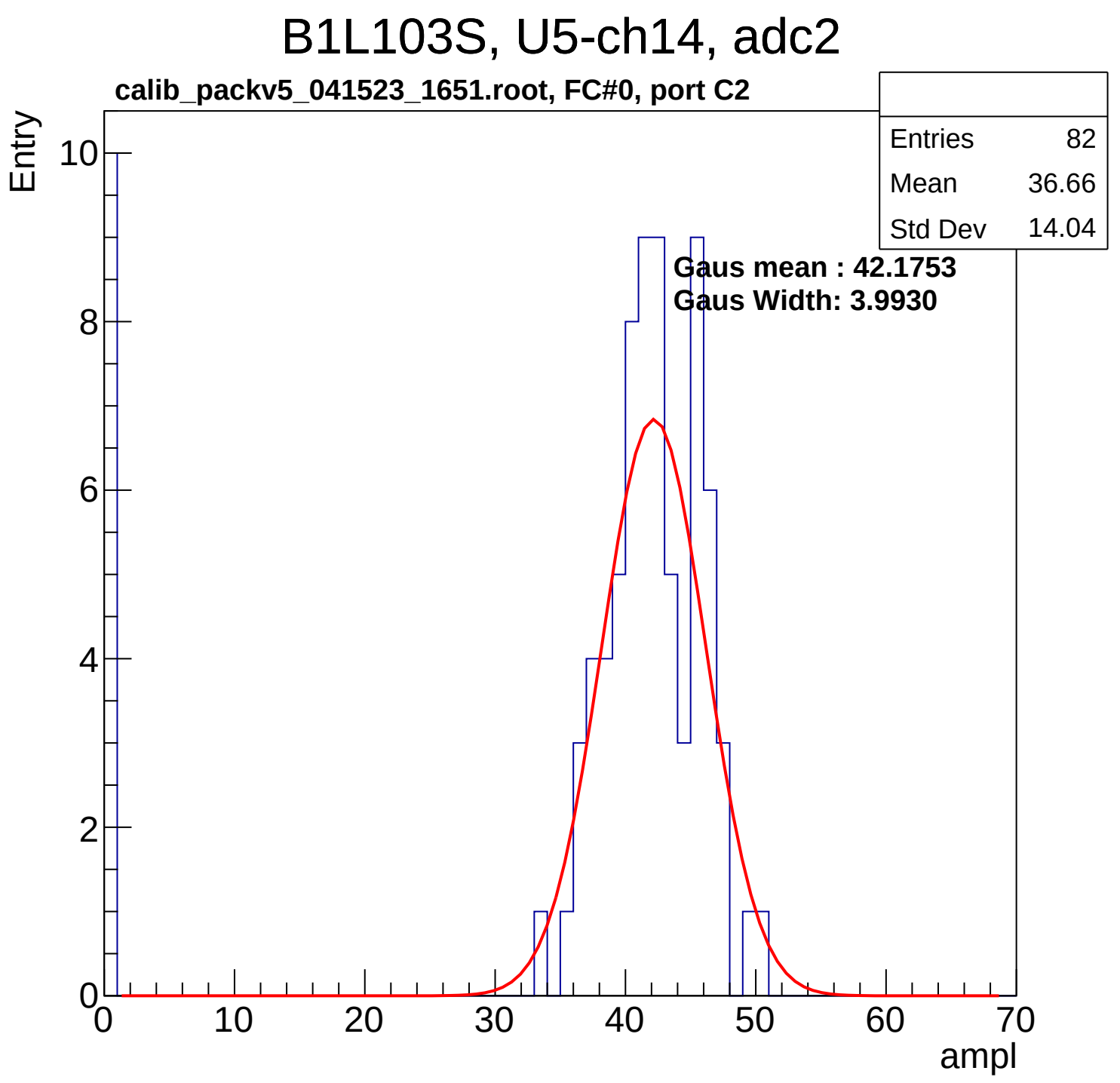
B1L103S, U5-ch14, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 36.66
Std Dev 14.04
Gaus mean : 42.1753
Gaus Width: 3.9930
Entry
ampl
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2
4
6
8
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0
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60
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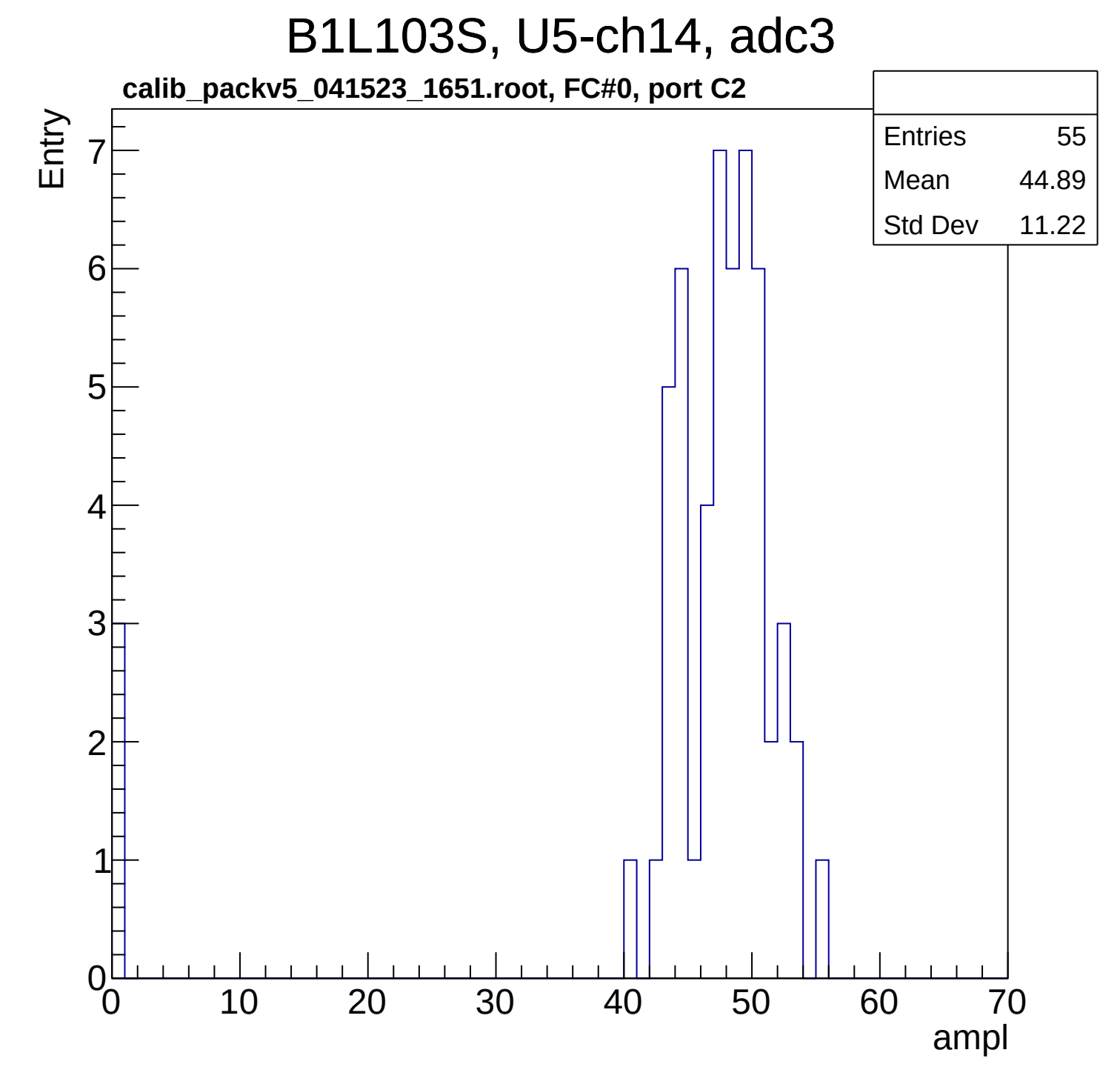
B1L103S, U5-ch14, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 44.89
Std Dev 11.22
Entry
ampl
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3
4
5
6
7
0
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60
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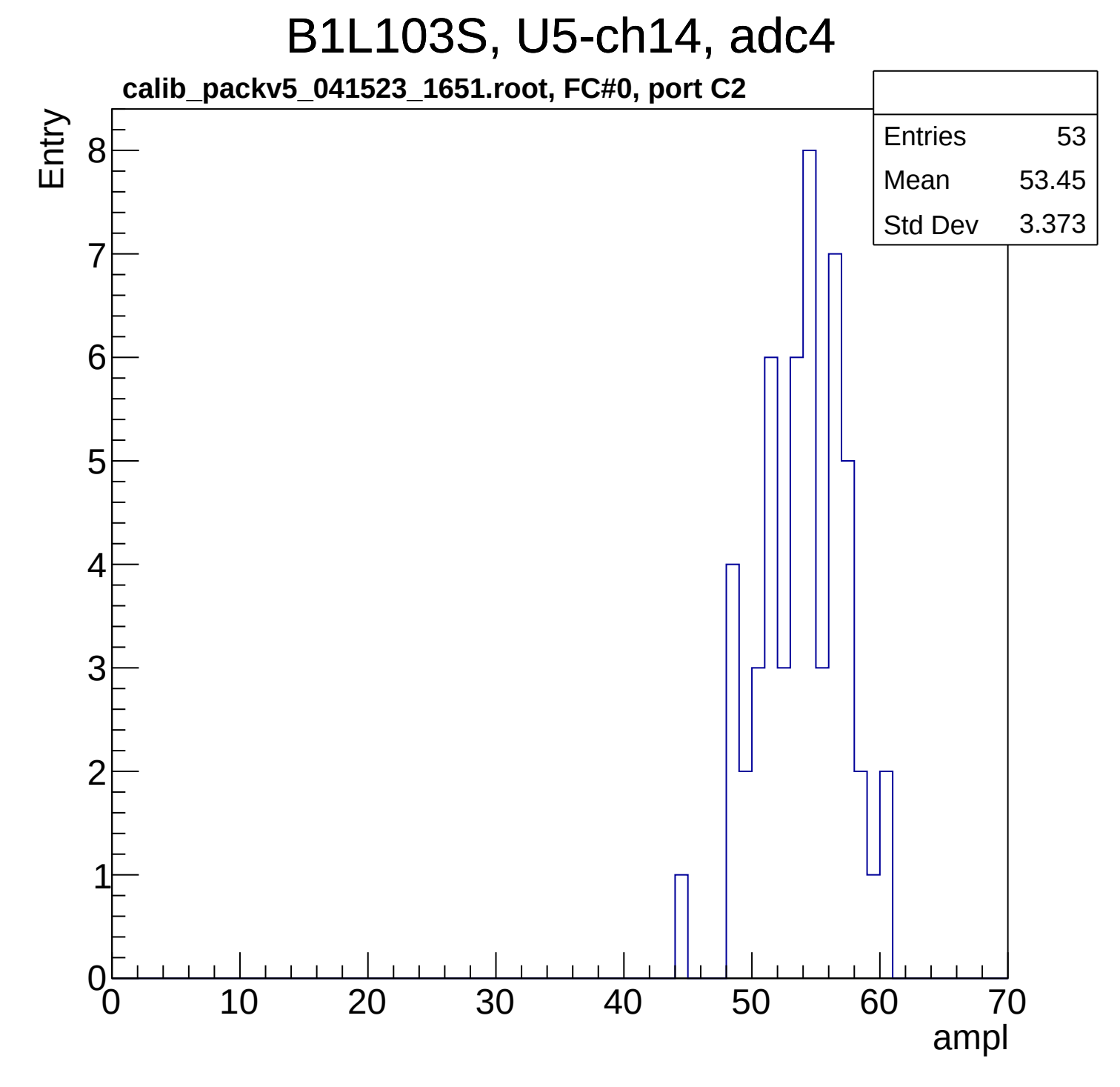
B1L103S, U5-ch14, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 53.45
Std Dev 3.373
Entry
ampl
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0
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60
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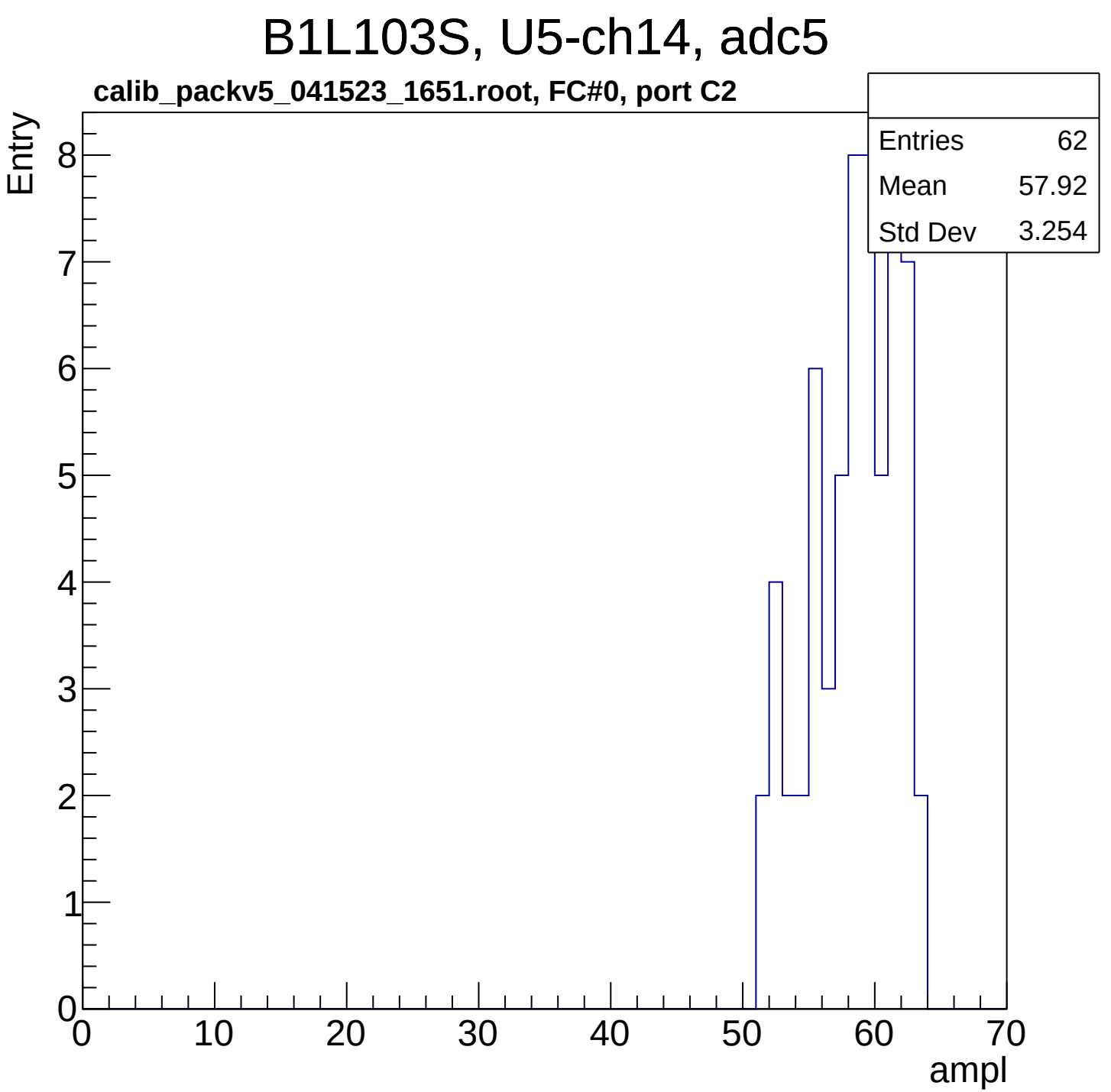
B1L103S, U5-ch14, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 57.92
Std Dev 3.254
Entry
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2
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4
5
6
7
8
0
10
20
30
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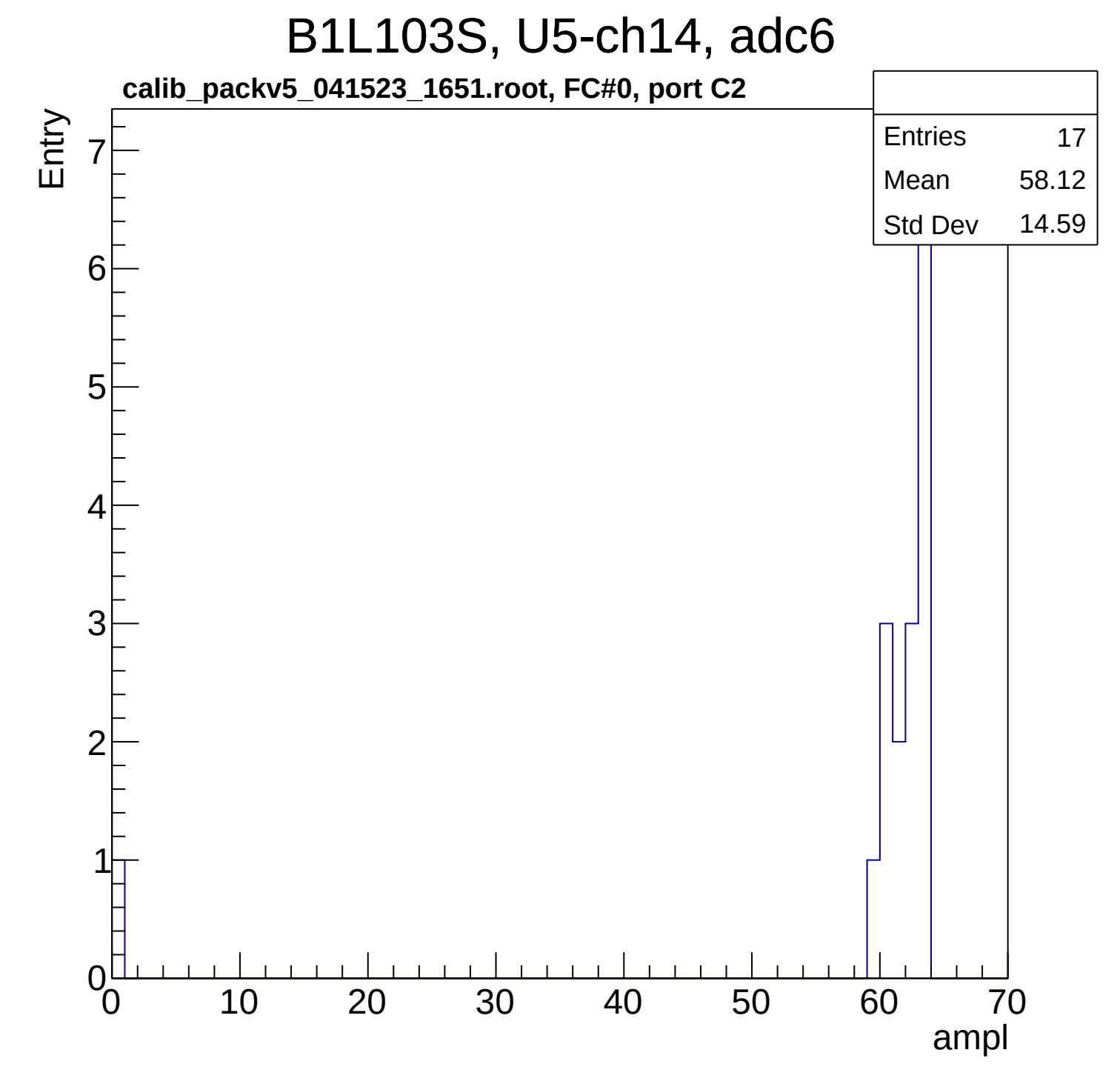
50
60
70
ampl


B1L103S, U5-ch14, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 58.12
Std Dev 14.59
Entry
ampl
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4
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0
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60
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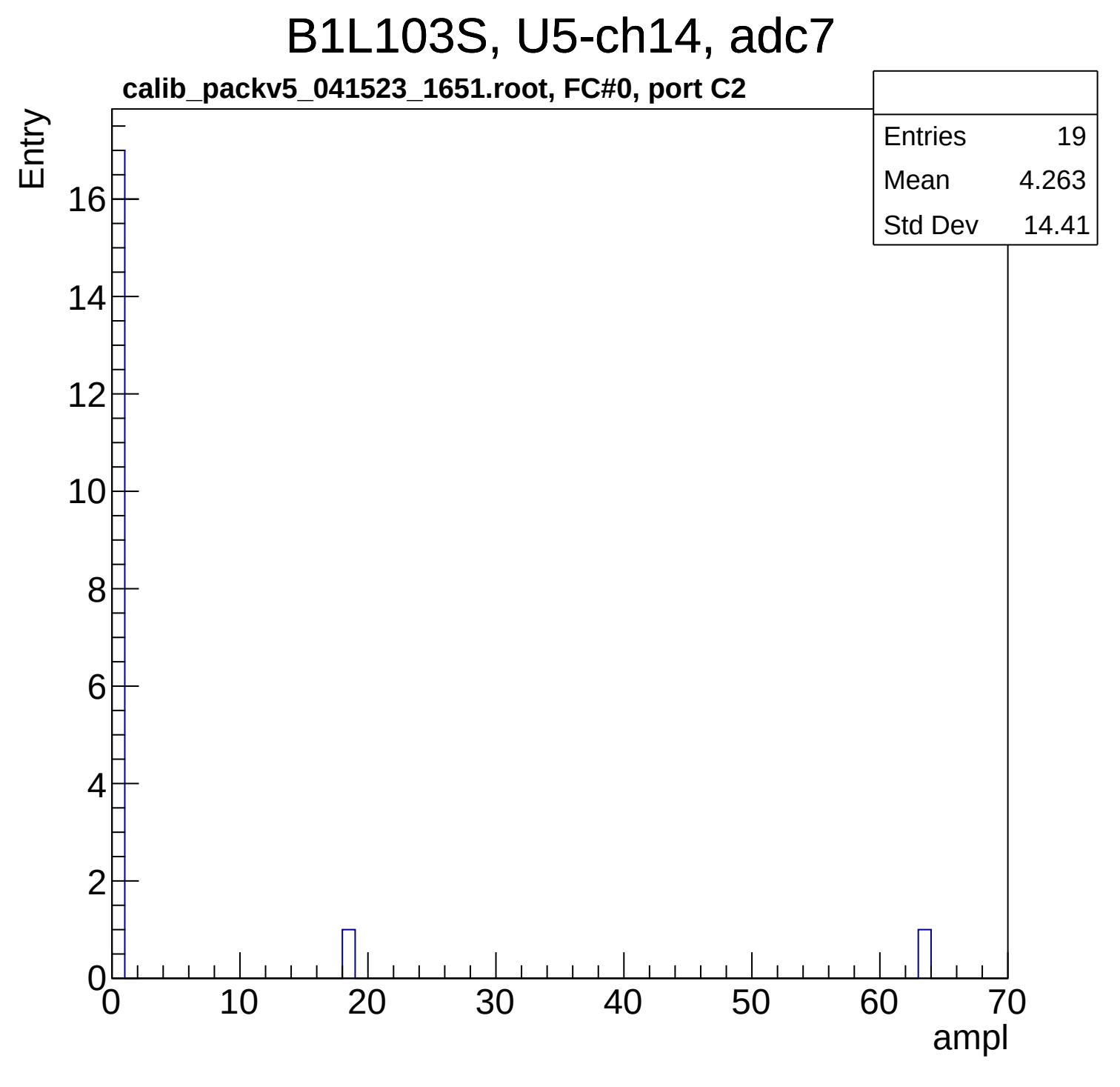
B1L103S, U5-ch14, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 4.263
Std Dev 14.41
Entry
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8
10
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14
16
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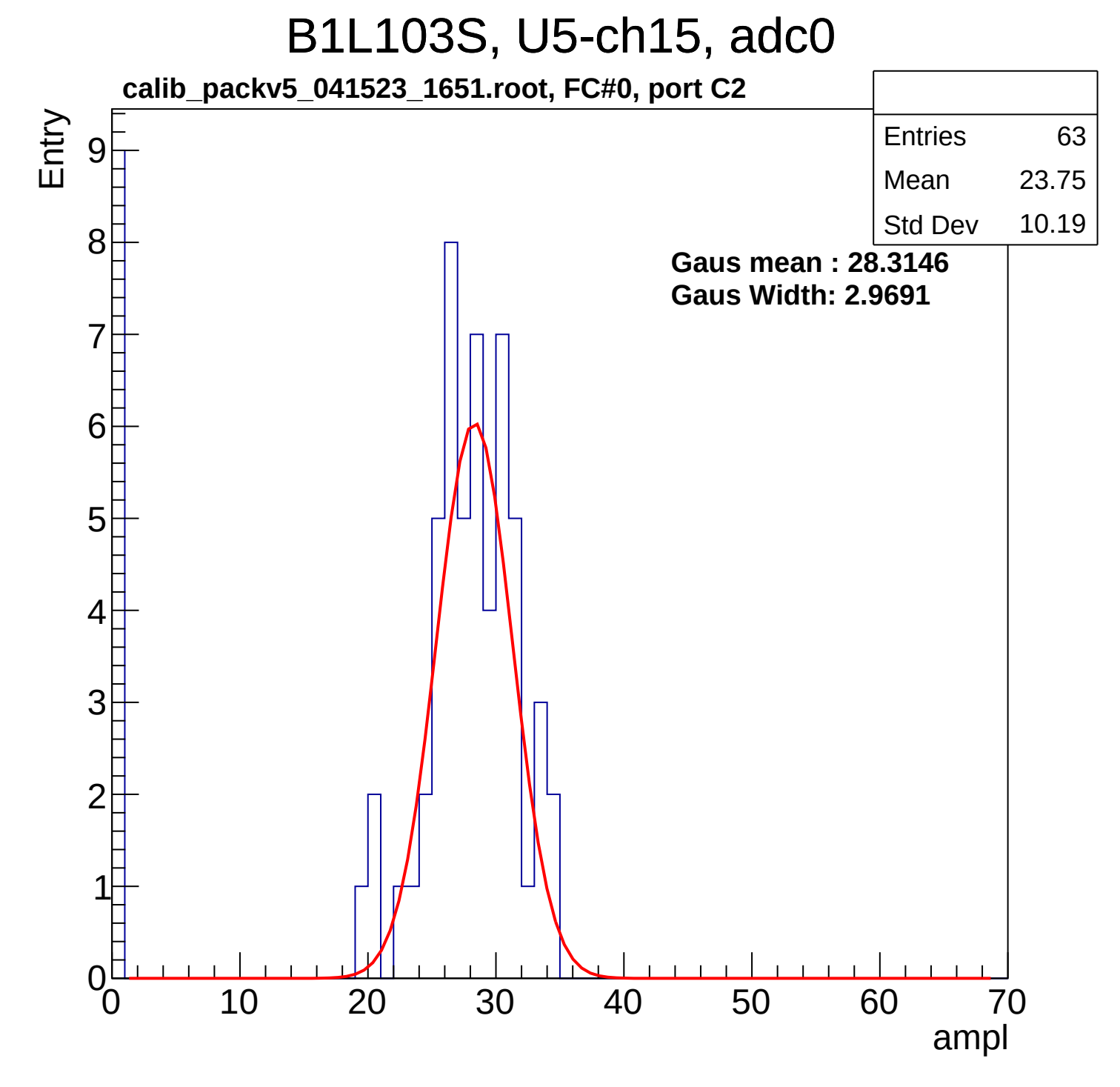
50
60
70
ampl


B1L103S, U5-ch15, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 23.75
Std Dev 10.19
Gaus mean : 28.3146
Gaus Width: 2.9691
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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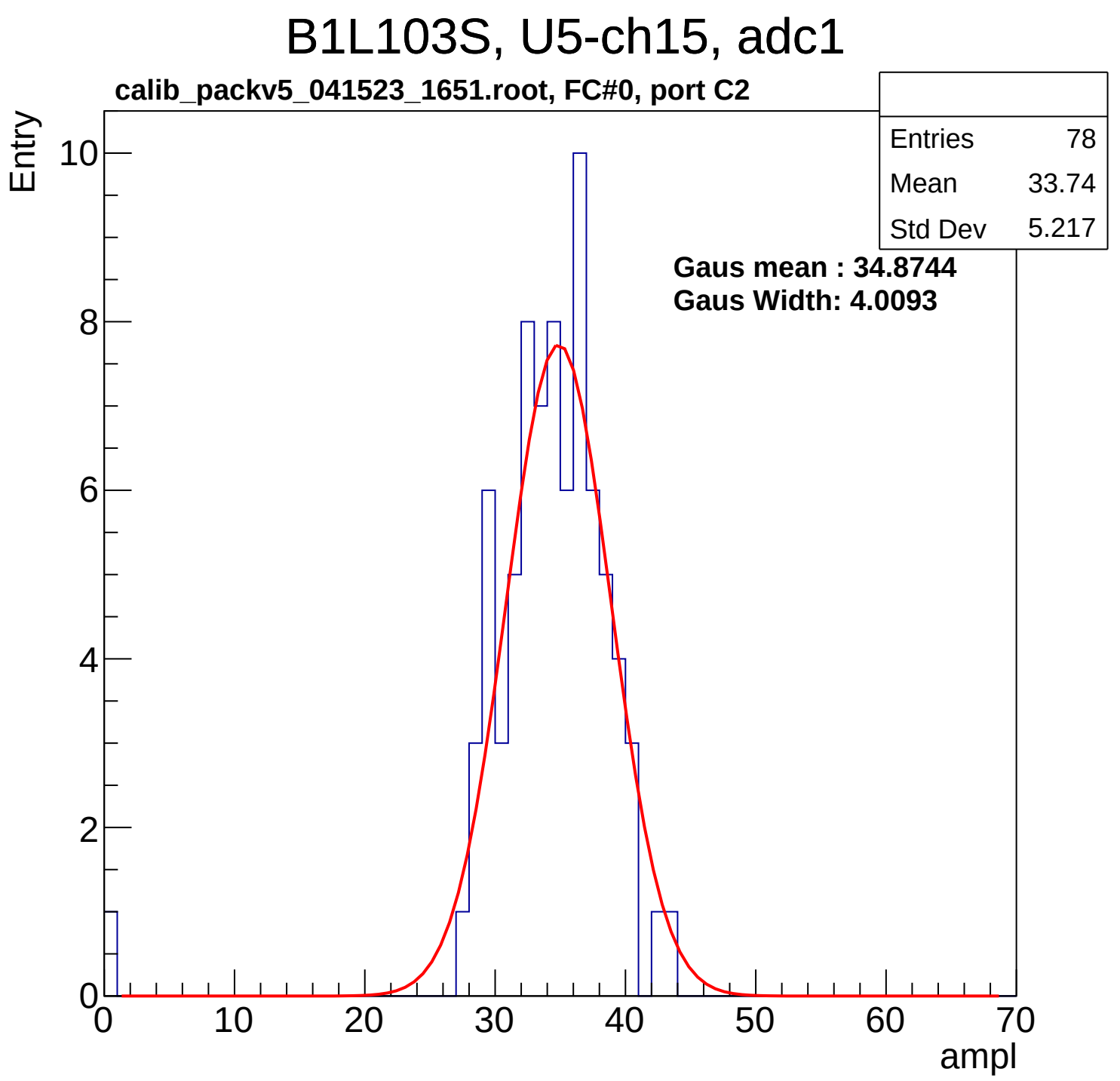
B1L103S, U5-ch15, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 33.74
Std Dev 5.217
Gaus mean : 34.8744
Gaus Width: 4.0093
Entry
ampl
0
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4
6
8
10
0
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20
30
40
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60
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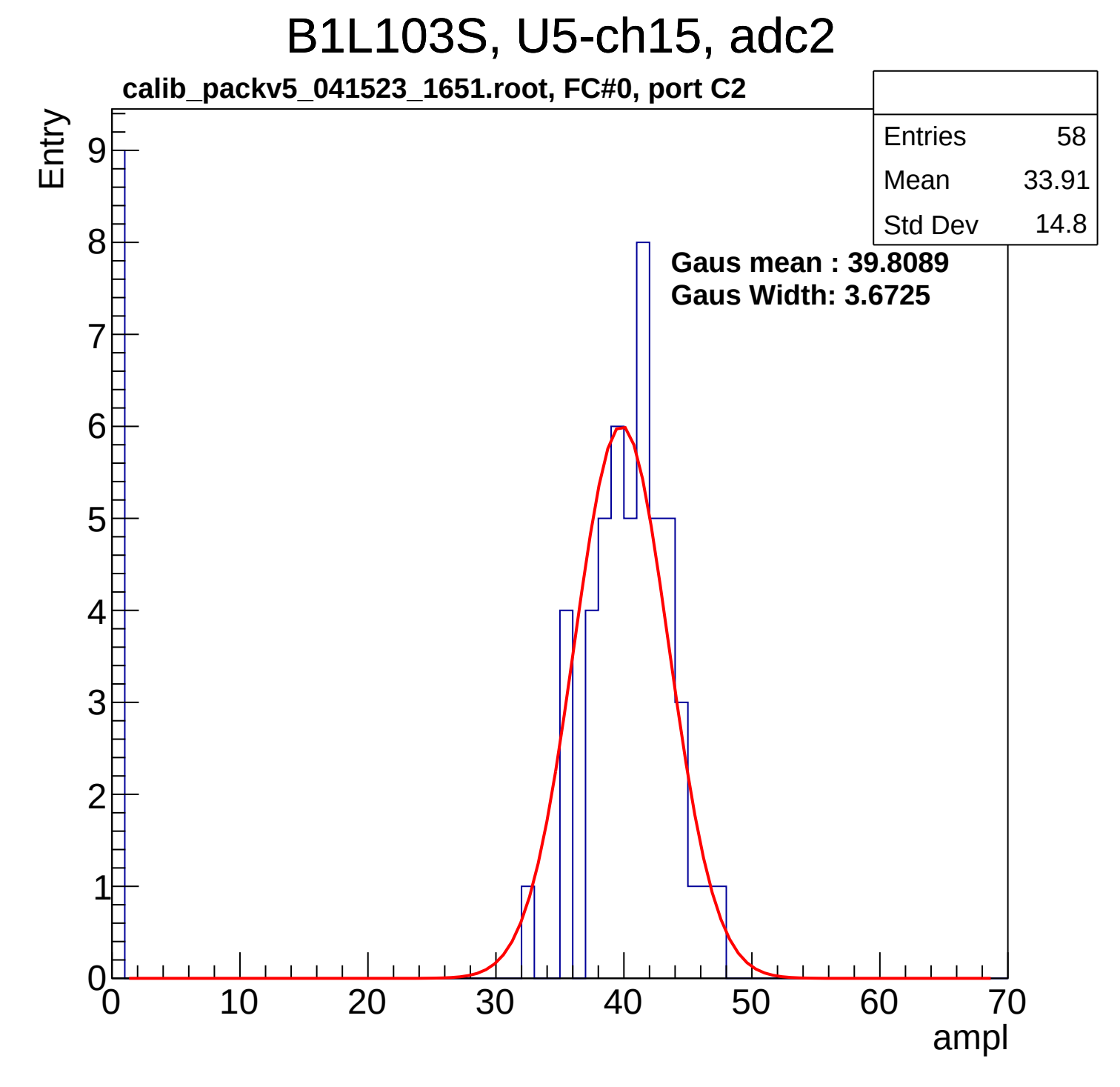
B1L103S, U5-ch15, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 33.91
Std Dev 14.8
Gaus mean : 39.8089
Gaus Width: 3.6725
Entry
ampl
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2
3
4
5
6
7
8
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0
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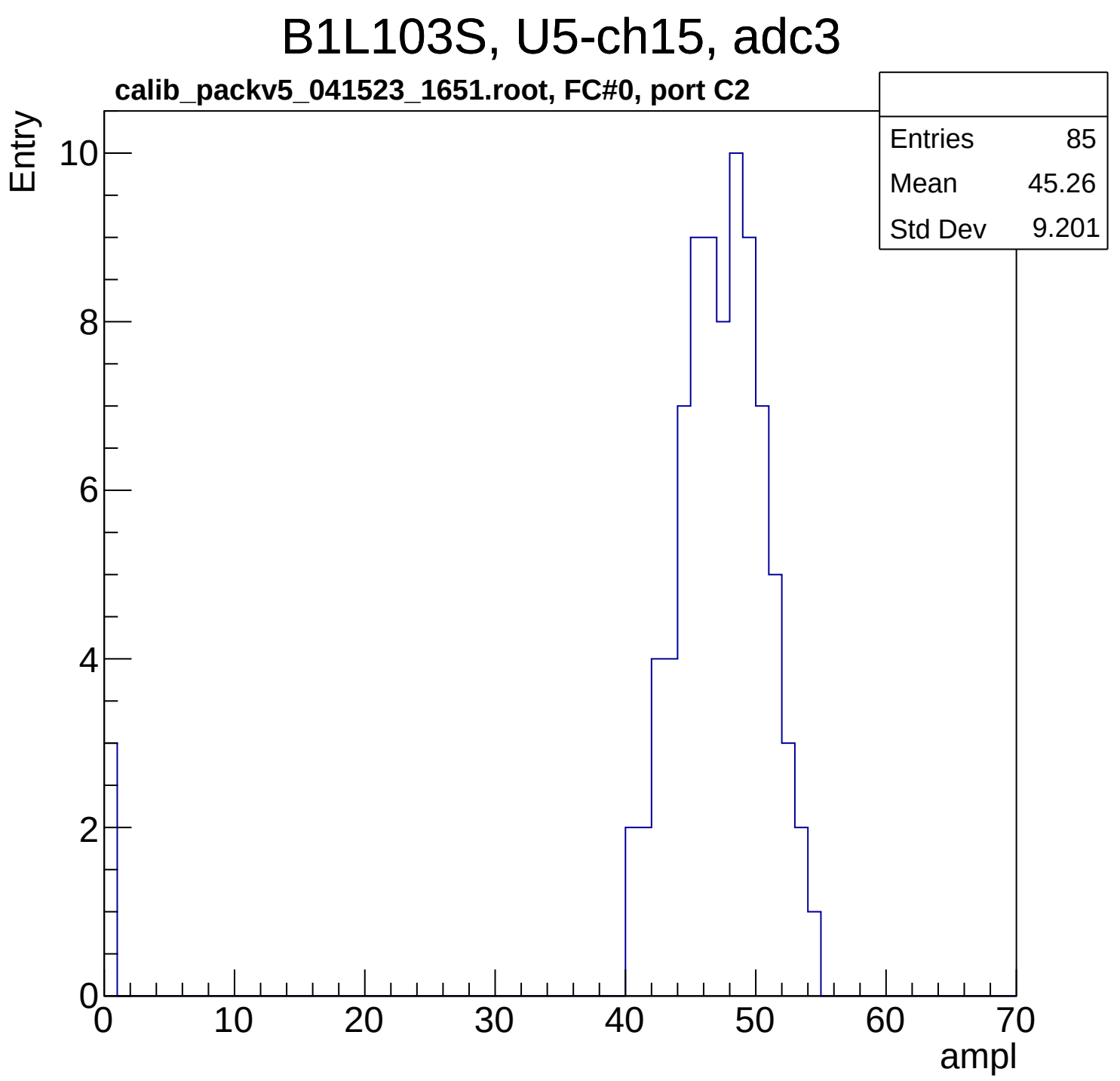
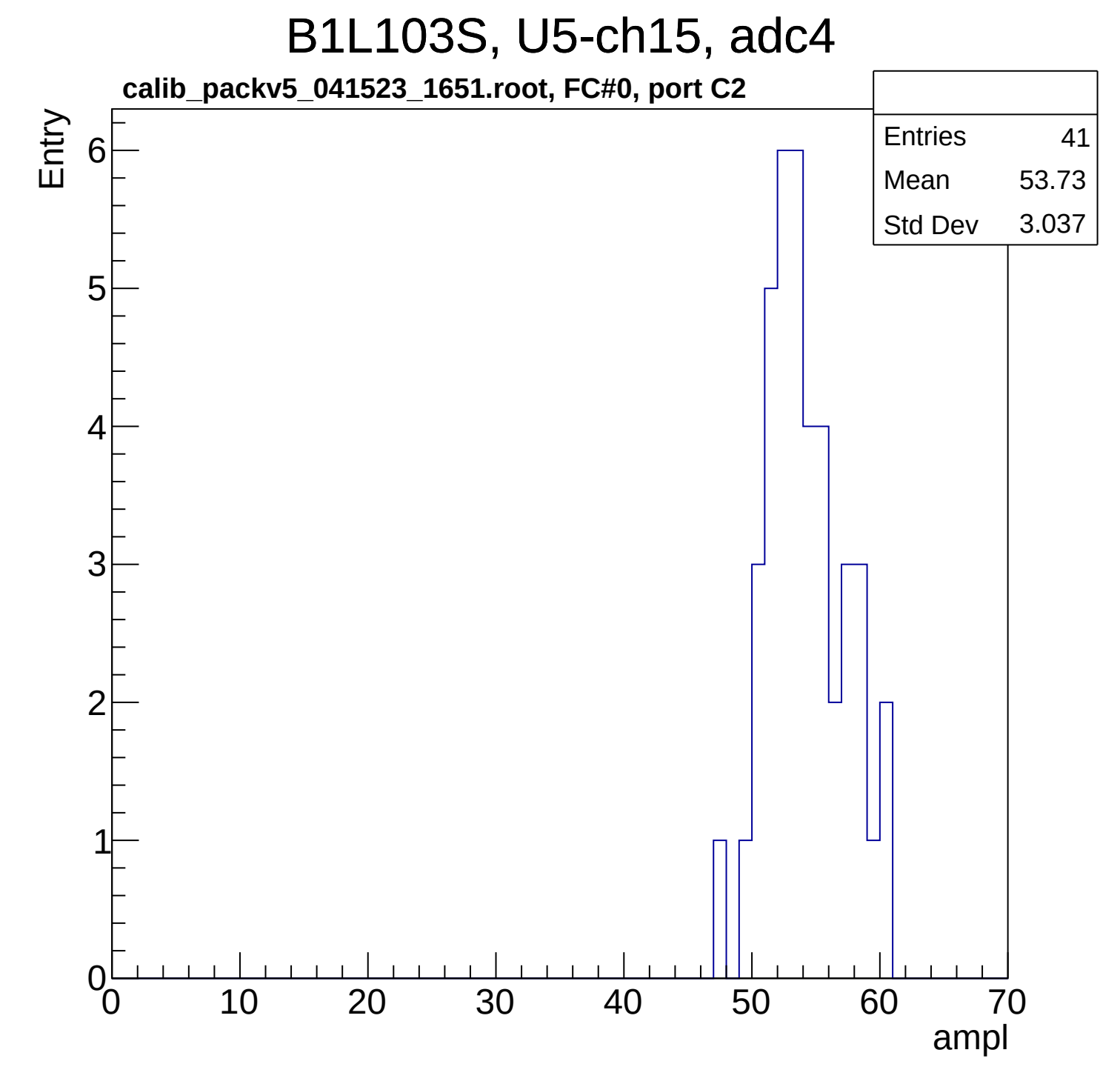

B1L103S, U5-ch15, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 45.26
Std Dev 9.201
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U5-ch15, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 53.73
Std Dev 3.037
Entry
ampl
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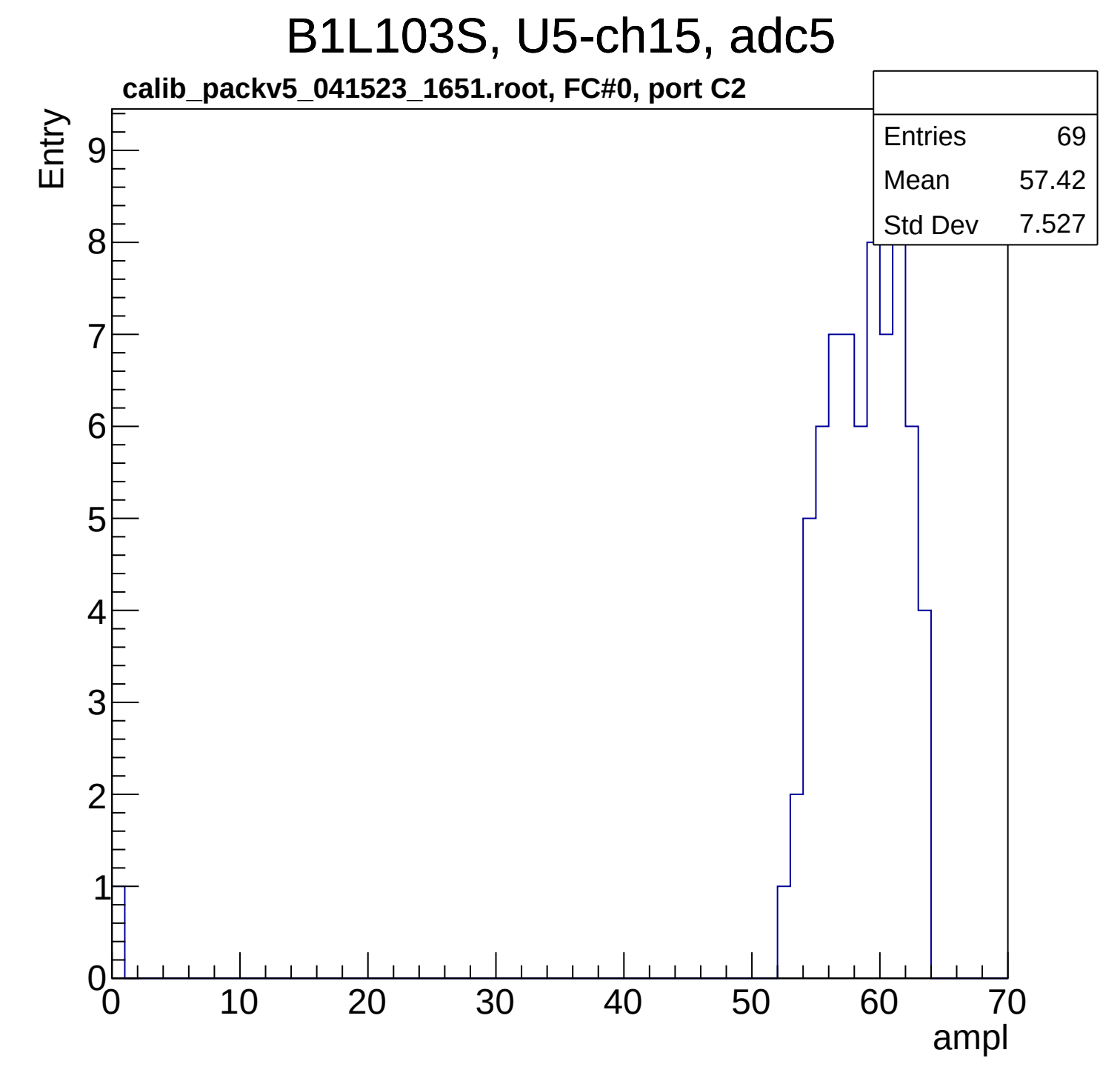
B1L103S, U5-ch15, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 57.42
Std Dev 7.527
Entry
ampl
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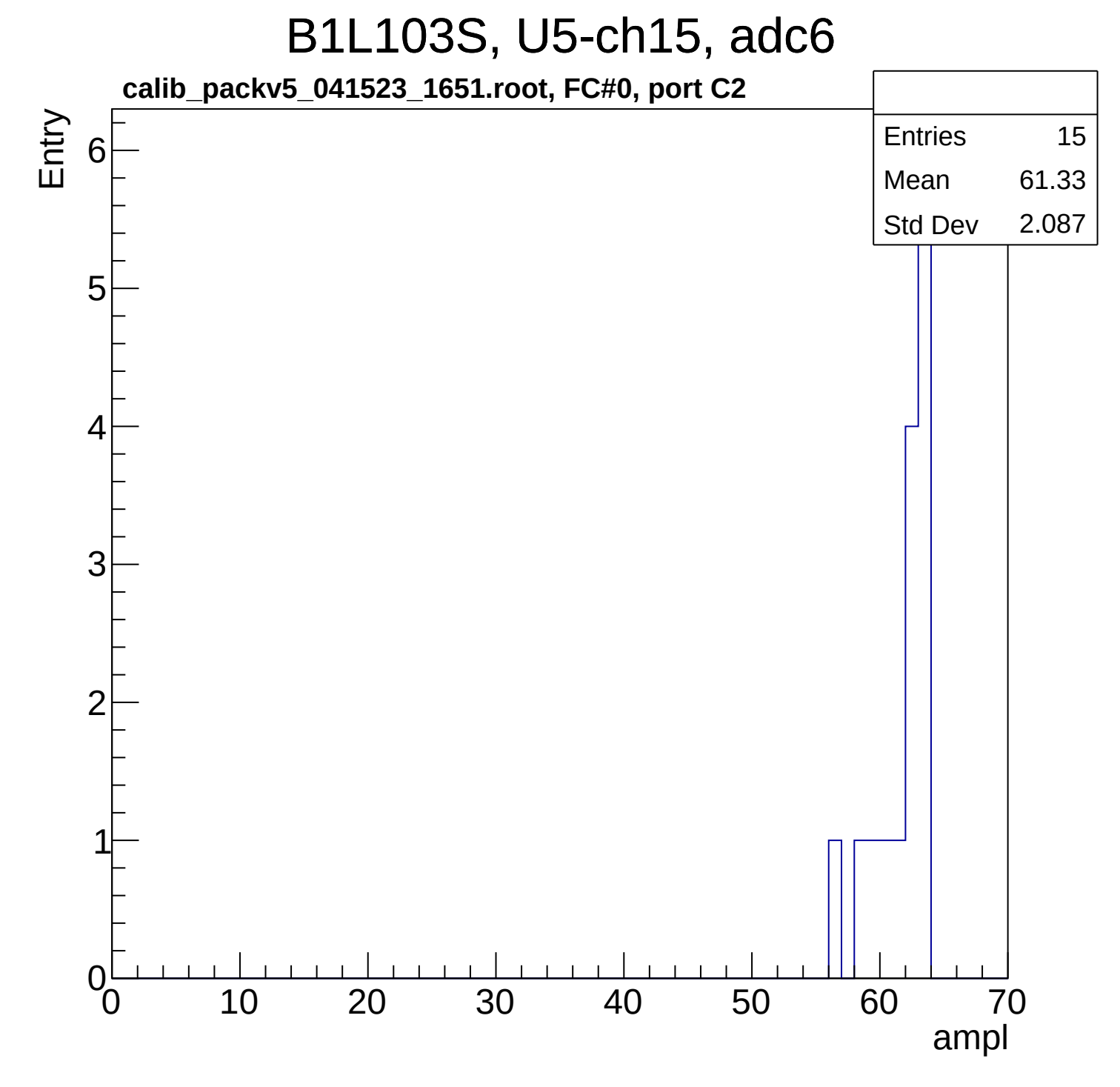
B1L103S, U5-ch15, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.33
Std Dev 2.087
Entry
ampl
0
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2
3
4
5
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0
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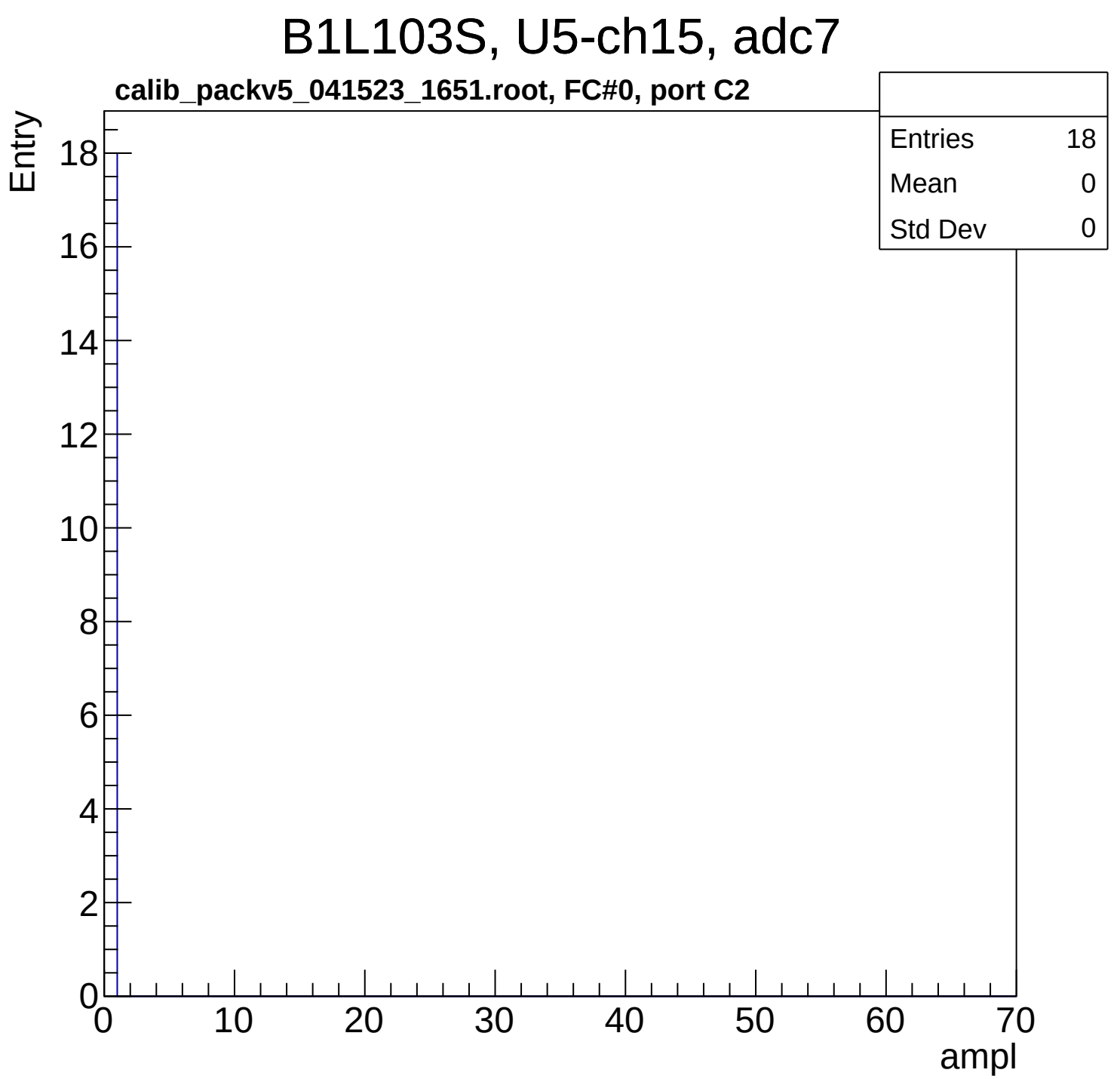
B1L103S, U5-ch15, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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6
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10
12
14
16
18
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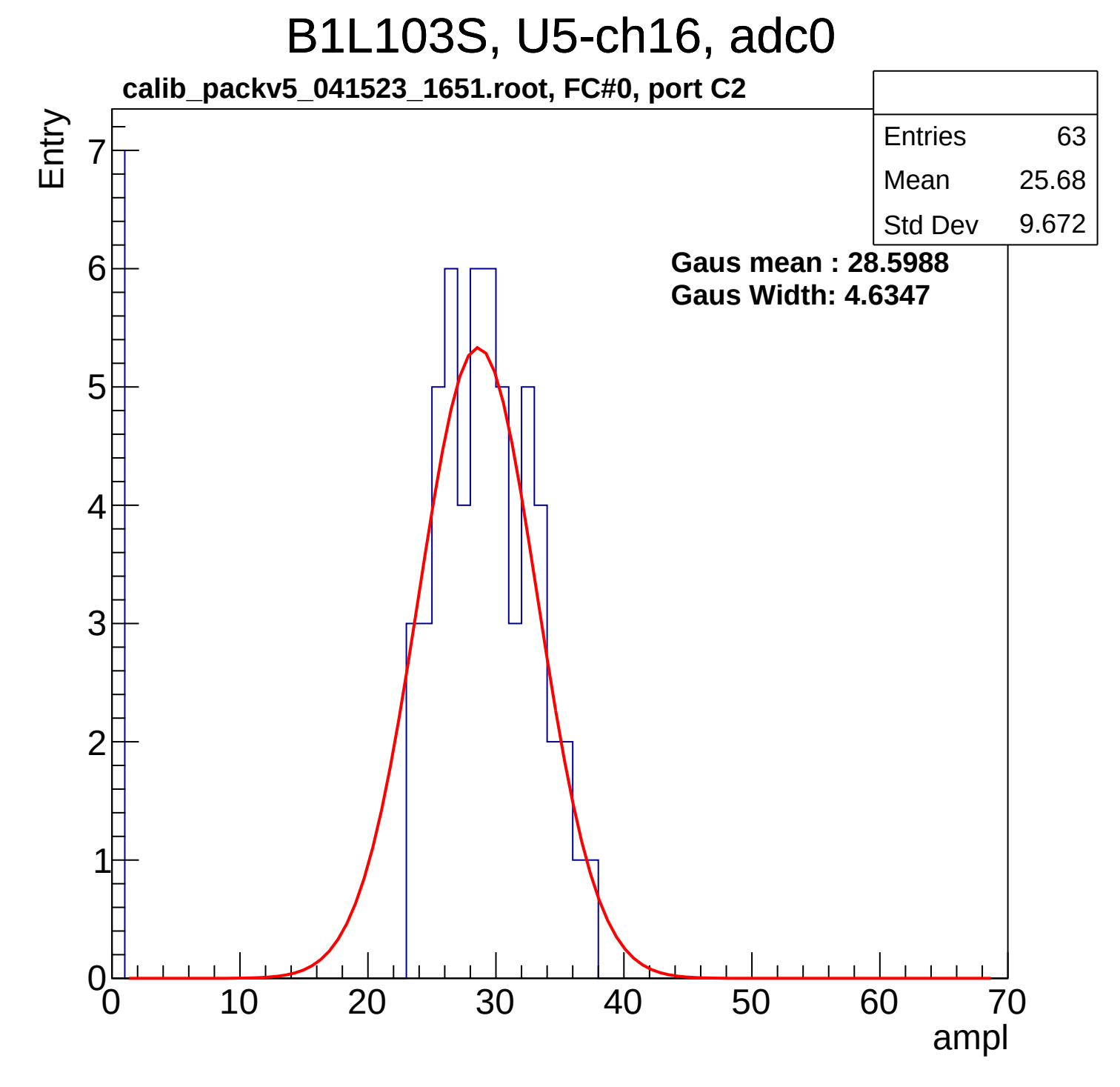
70
ampl


B1L103S, U5-ch16, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 25.68
Std Dev 9.672
Gaus mean : 28.5988
Gaus Width: 4.6347
Entry
ampl
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1
2
3
4
5
6
7
0
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40
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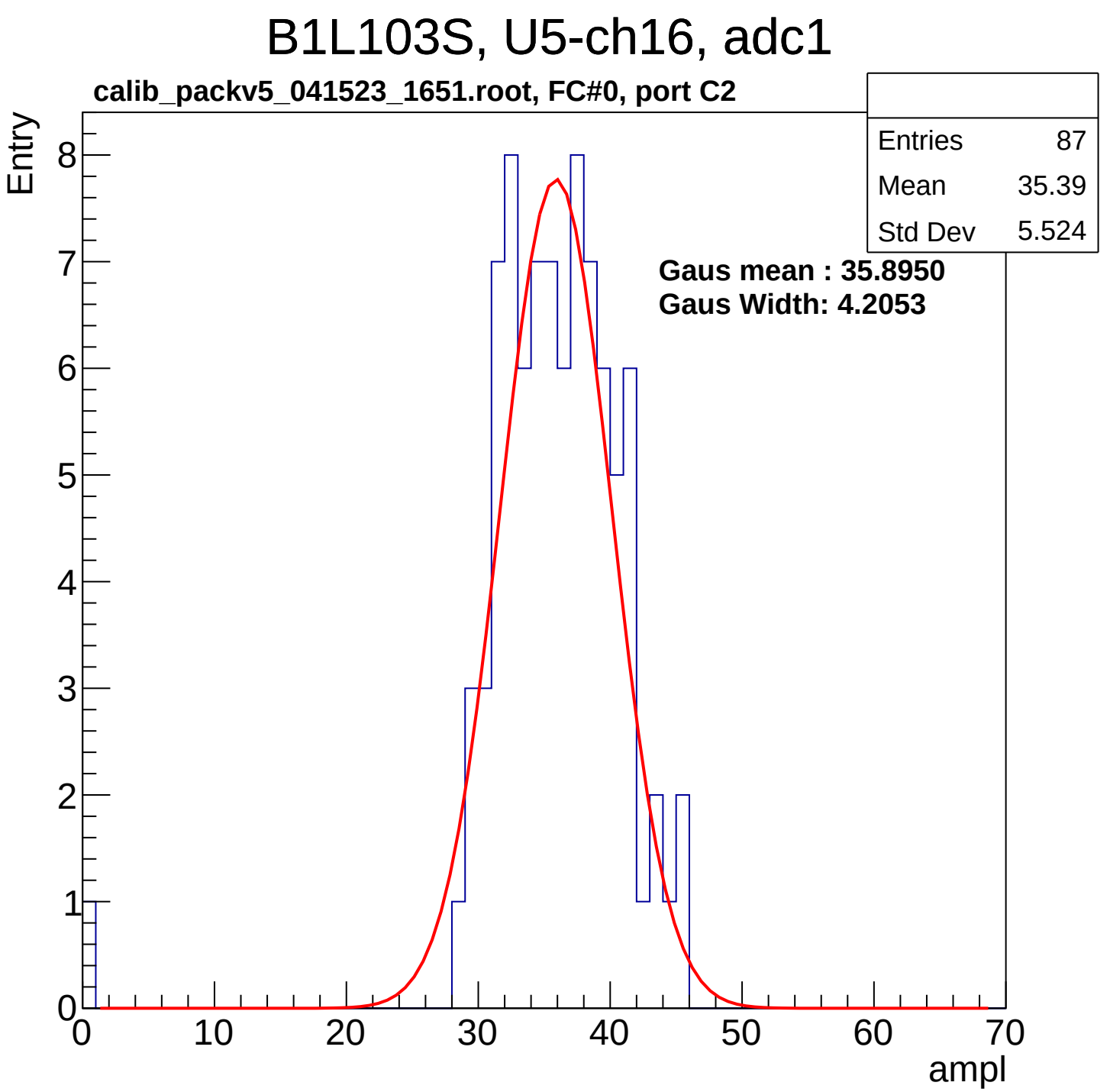
B1L103S, U5-ch16, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 35.39
Std Dev 5.524
Gaus mean : 35.8950
Gaus Width: 4.2053
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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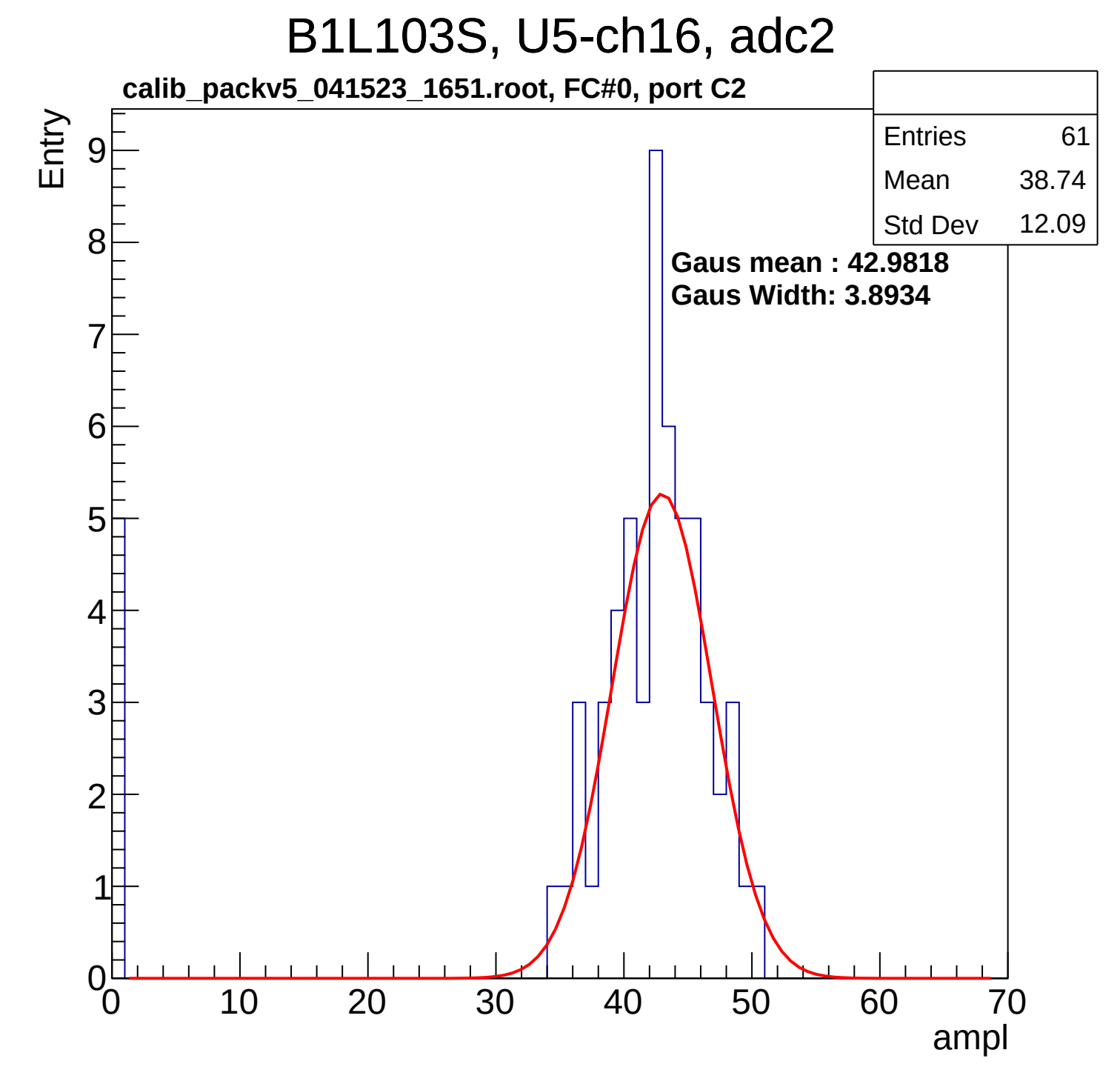
B1L103S, U5-ch16, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 38.74
Std Dev 12.09
Gaus mean : 42.9818
Gaus Width: 3.8934
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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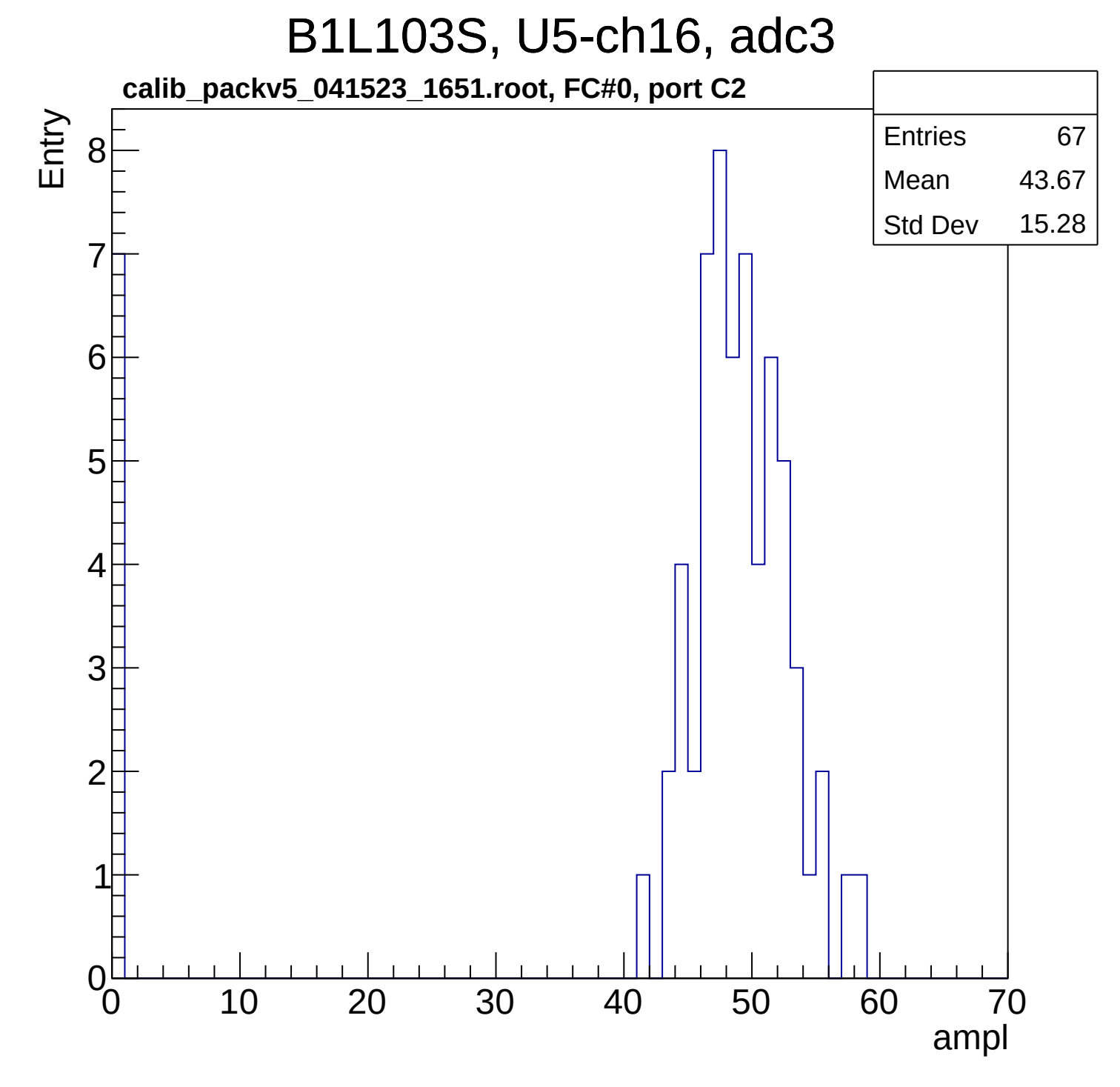
B1L103S, U5-ch16, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 43.67
Std Dev 15.28
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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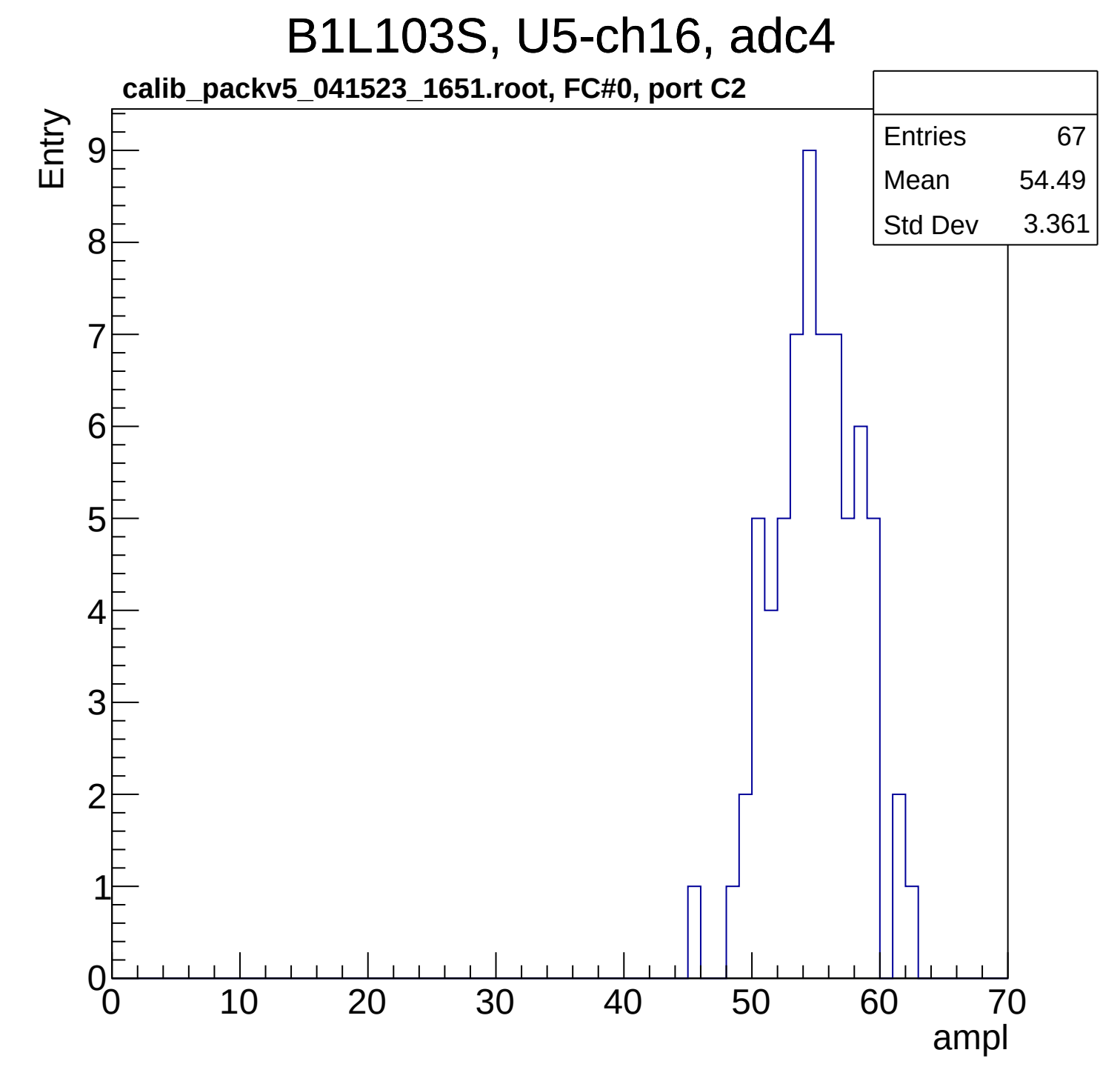
B1L103S, U5-ch16, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 54.49
Std Dev 3.361
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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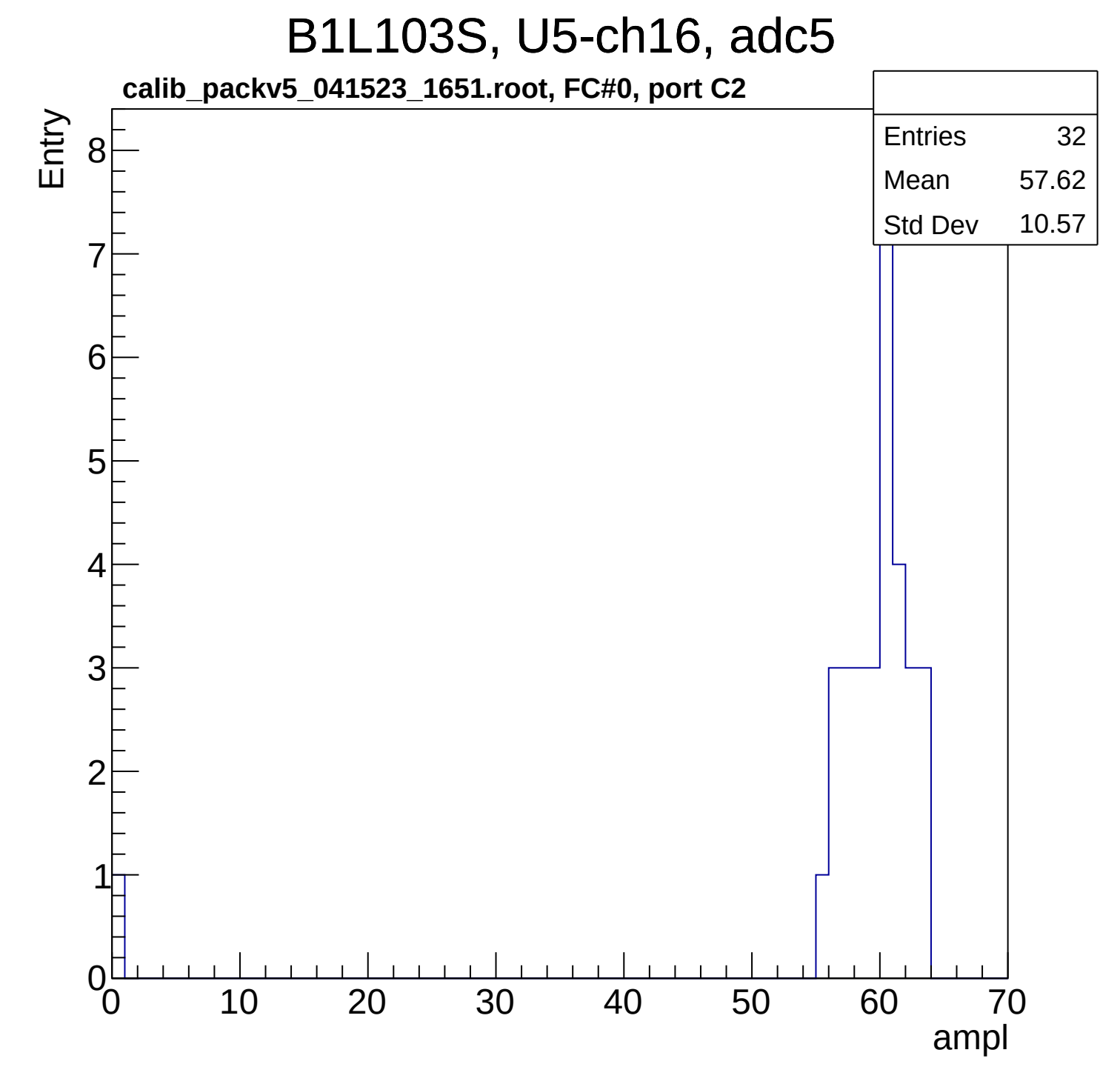
B1L103S, U5-ch16, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 57.62
Std Dev 10.57
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
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60
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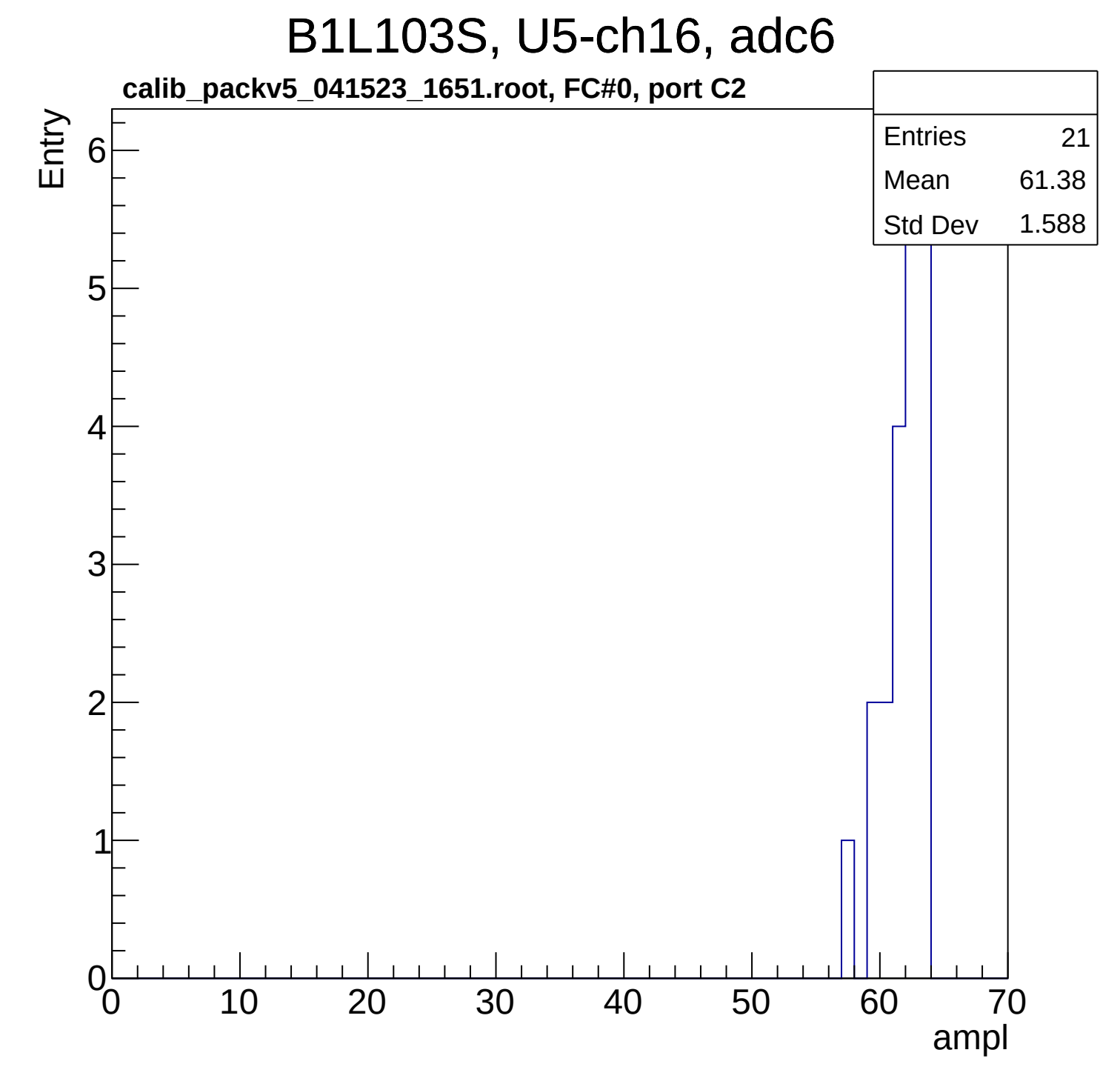
B1L103S, U5-ch16, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 61.38
Std Dev 1.588
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
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60
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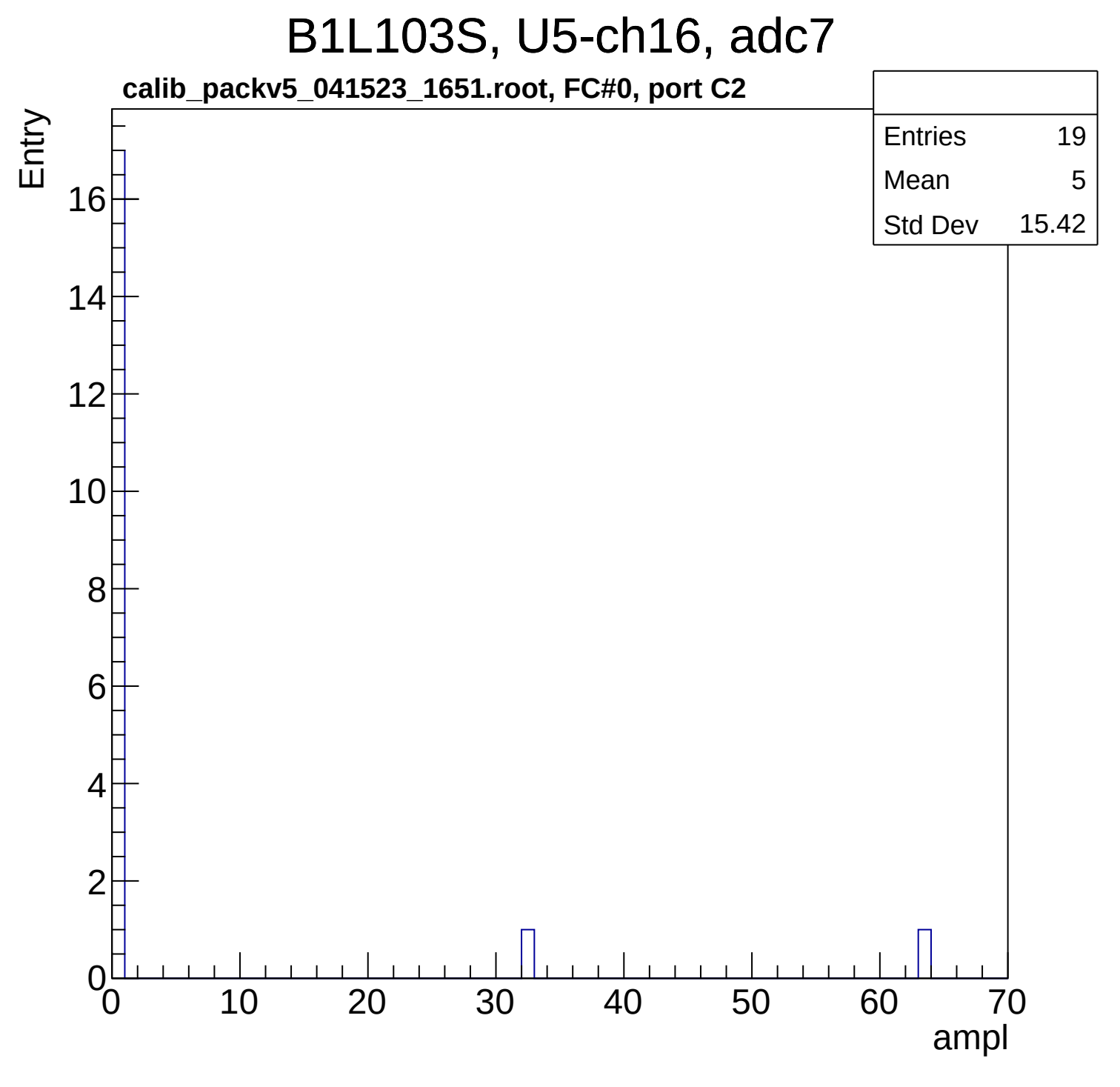
B1L103S, U5-ch16, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 5
Std Dev 15.42
Entry
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4
6
8
10
12
14
16
0
10
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30
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50
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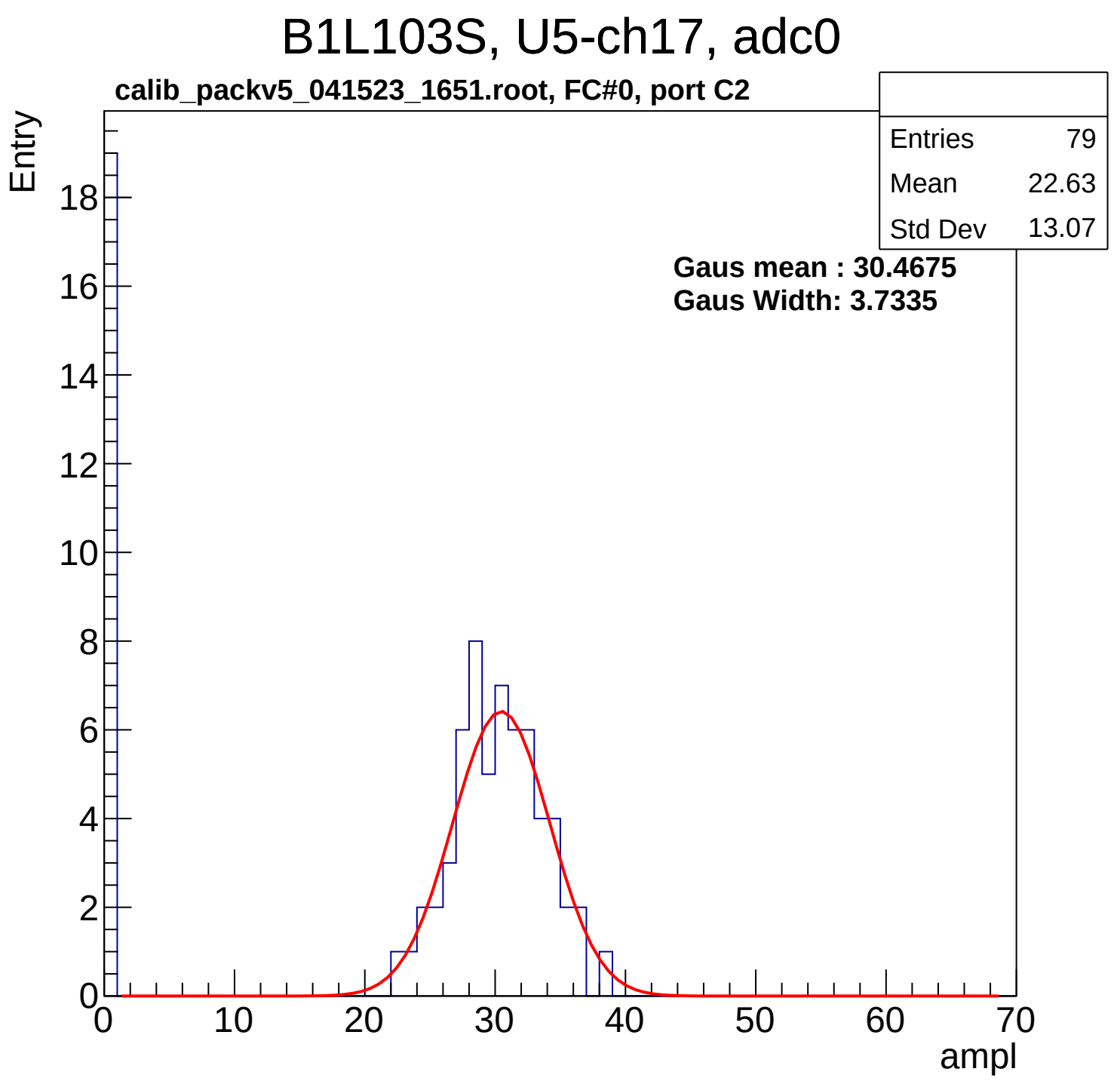
70
ampl


B1L103S, U5-ch17, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 22.63
Std Dev 13.07
Gaus mean : 30.4675
Gaus Width: 3.7335
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
30
40
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60
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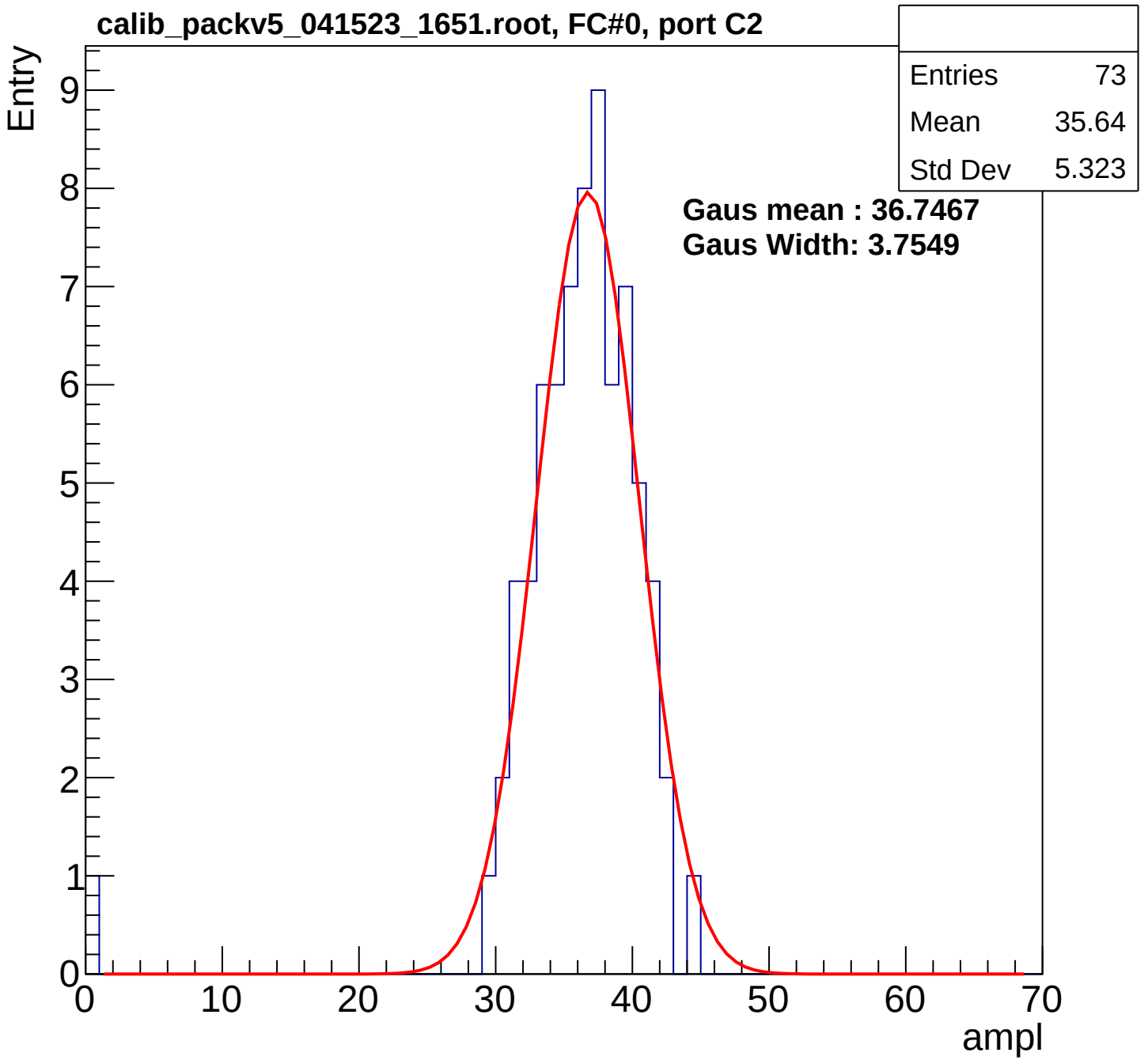
B1L103S, U5-ch17, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 35.64
Std Dev 5.323
Gaus mean : 36.7467
Gaus Width: 3.7549
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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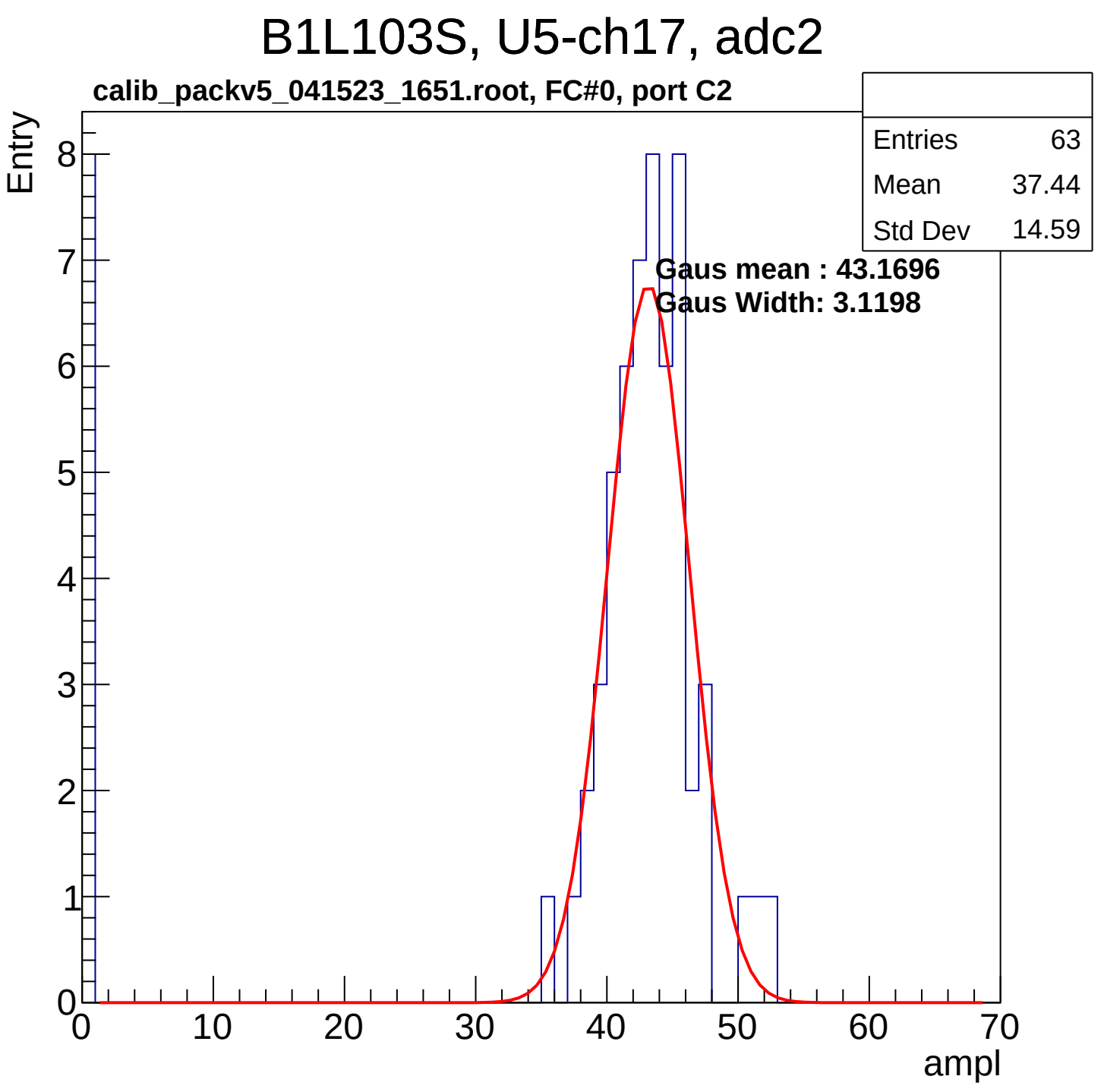
B1L103S, U5-ch17, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 37.44
Std Dev 14.59
Gaus mean : 43.1696
Gaus Width: 3.1198
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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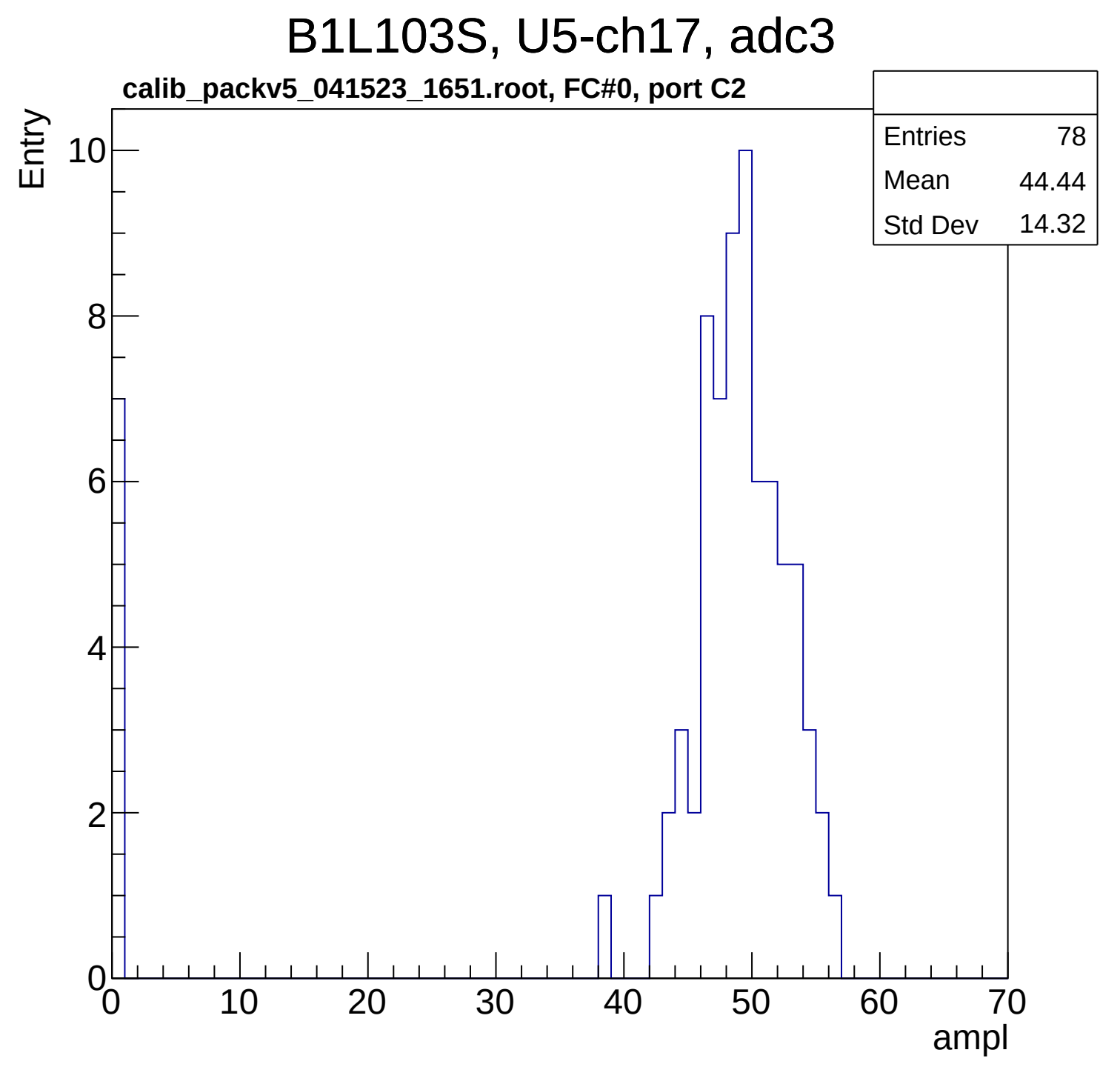
B1L103S, U5-ch17, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 44.44
Std Dev 14.32
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
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60
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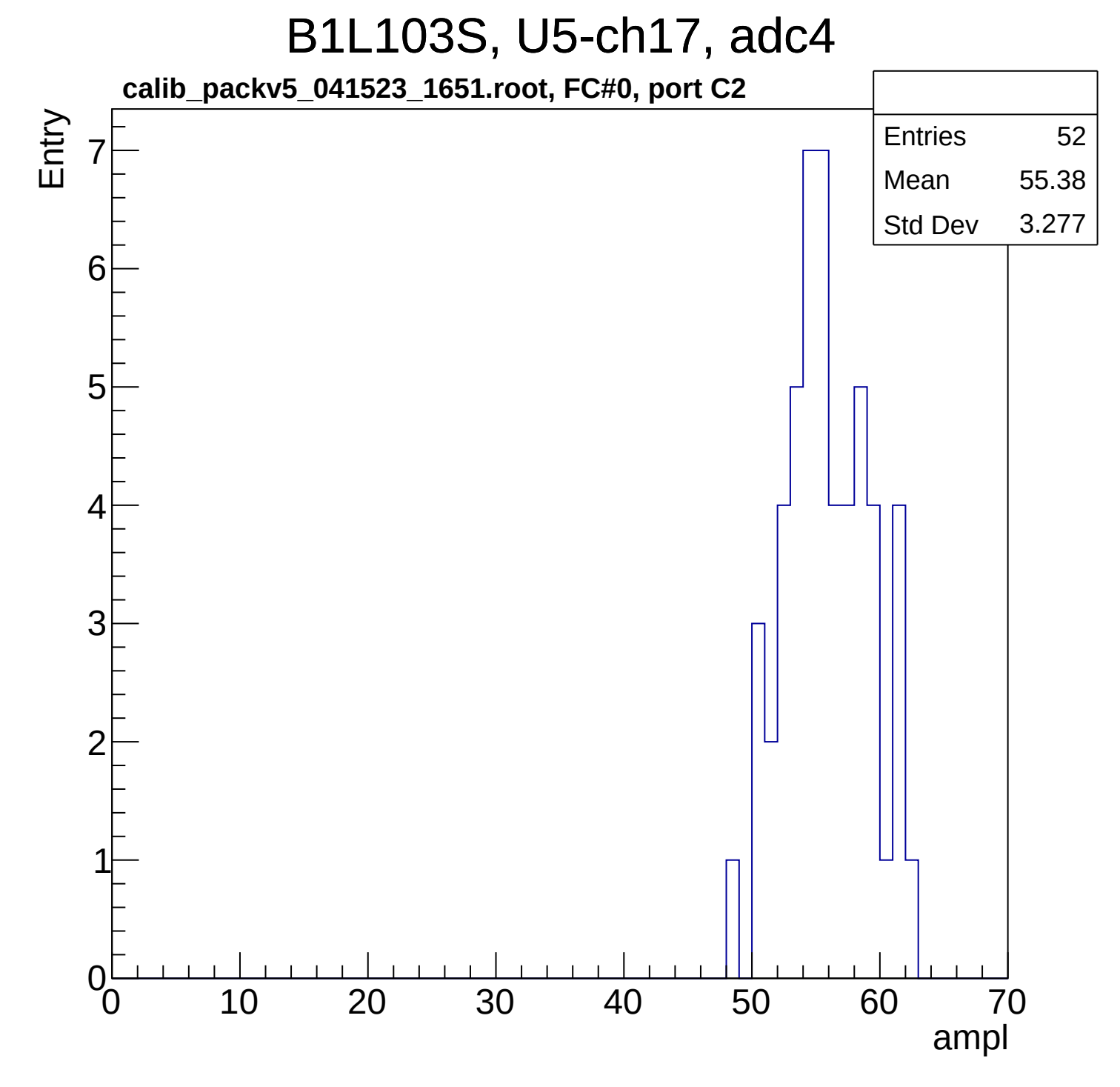
B1L103S, U5-ch17, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 55.38
Std Dev 3.277
Entry
ampl
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1
2
3
4
5
6
7
0
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40
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60
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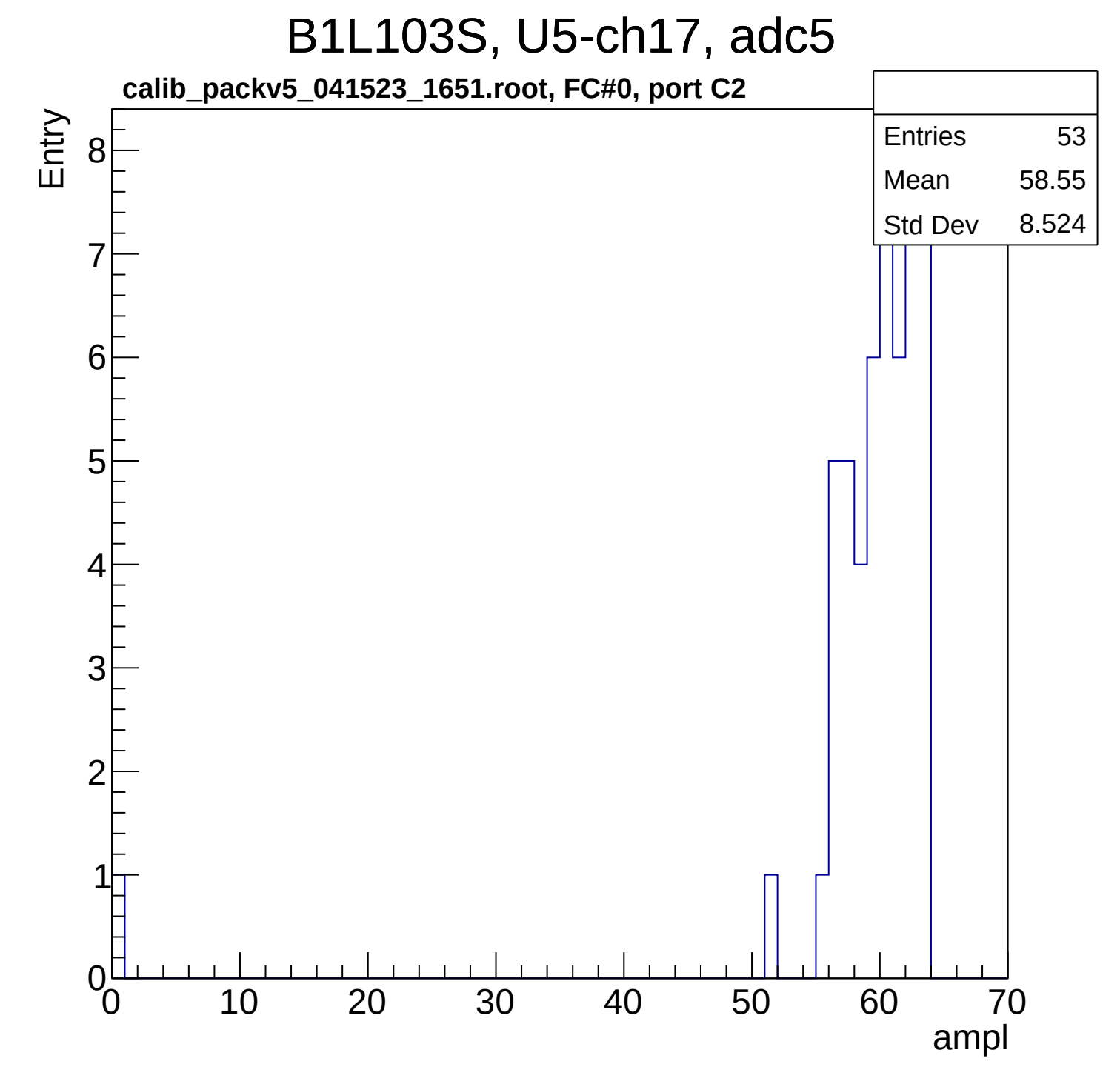
B1L103S, U5-ch17, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.55
Std Dev 8.524
Entry
ampl
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3
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5
6
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40
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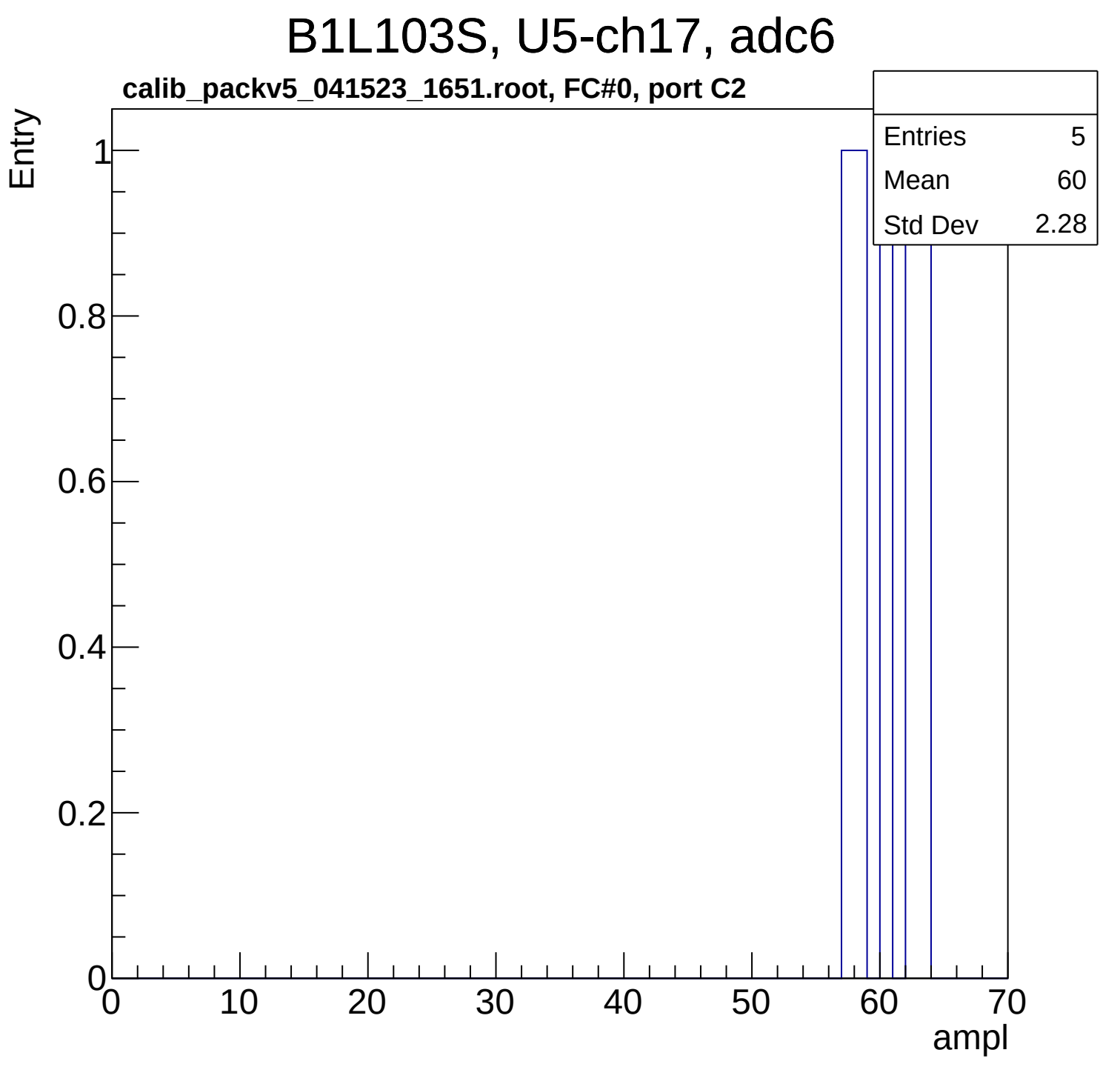
B1L103S, U5-ch17, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 60
Std Dev 2.28
Entry
ampl
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0.4
0.6
0.8
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40
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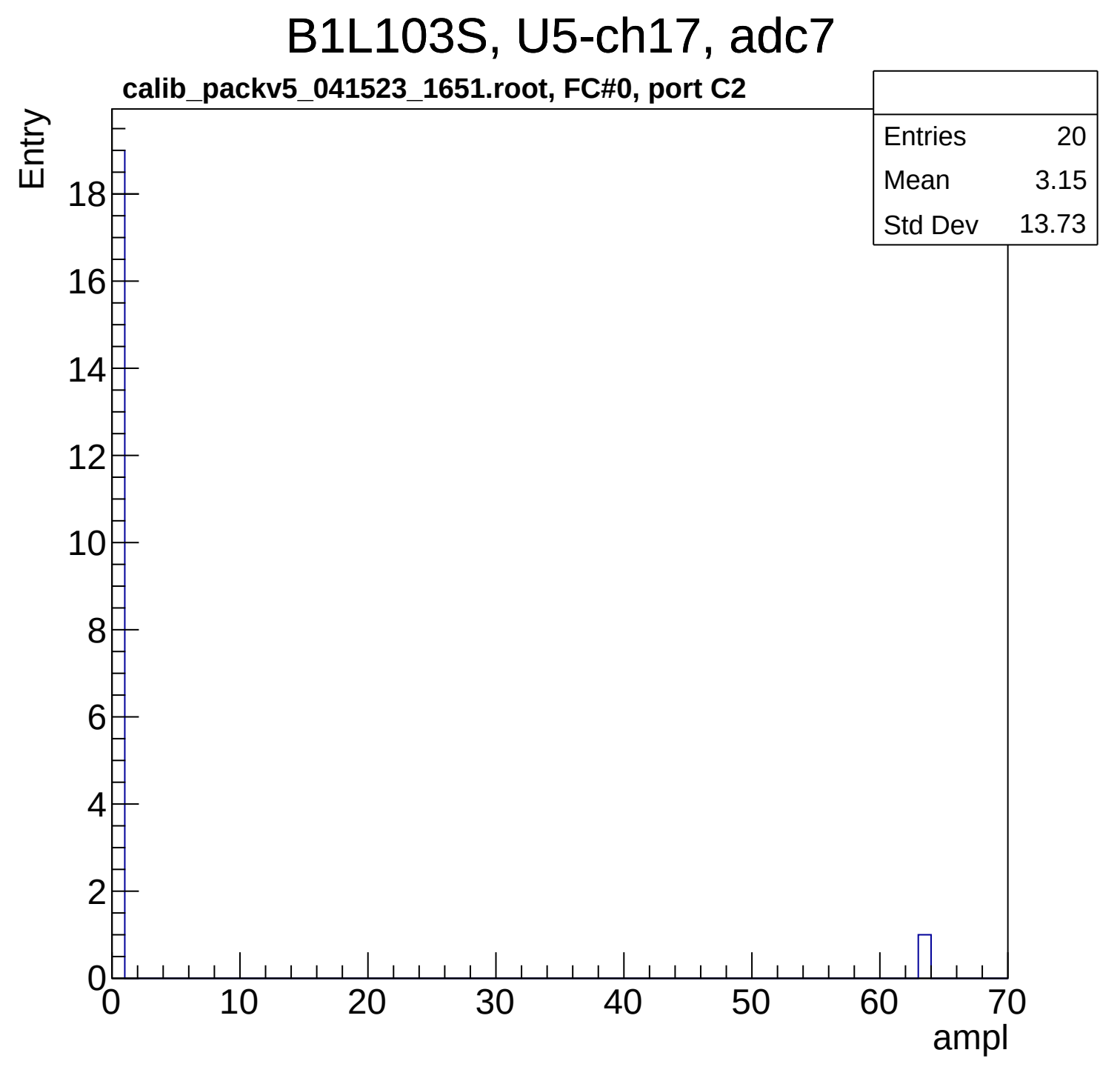
B1L103S, U5-ch17, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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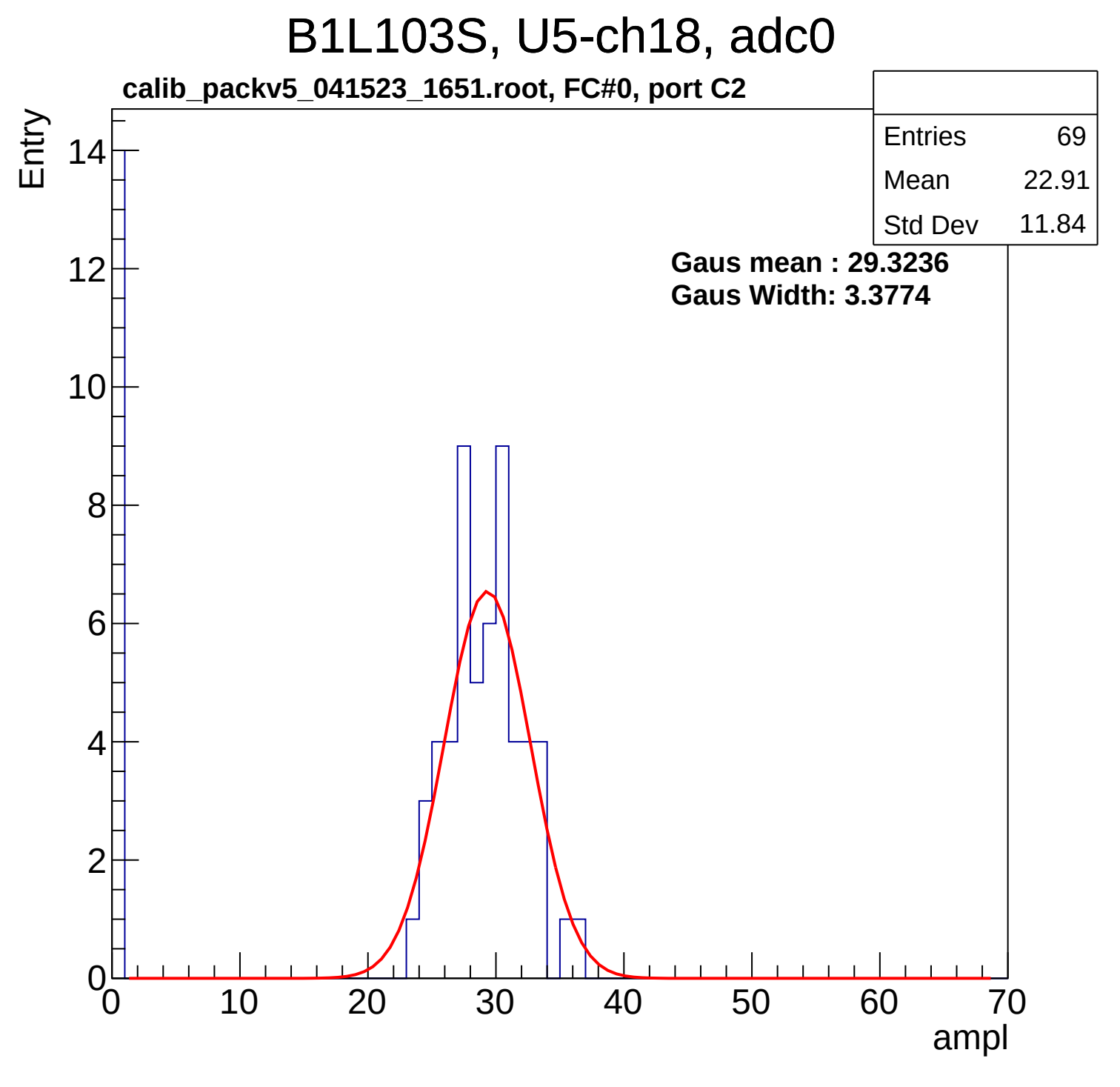
70
ampl


B1L103S, U5-ch18, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 22.91
Std Dev 11.84
Gaus mean : 29.3236
Gaus Width: 3.3774
Entry
ampl
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2
4
6
8
10
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0
10
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60
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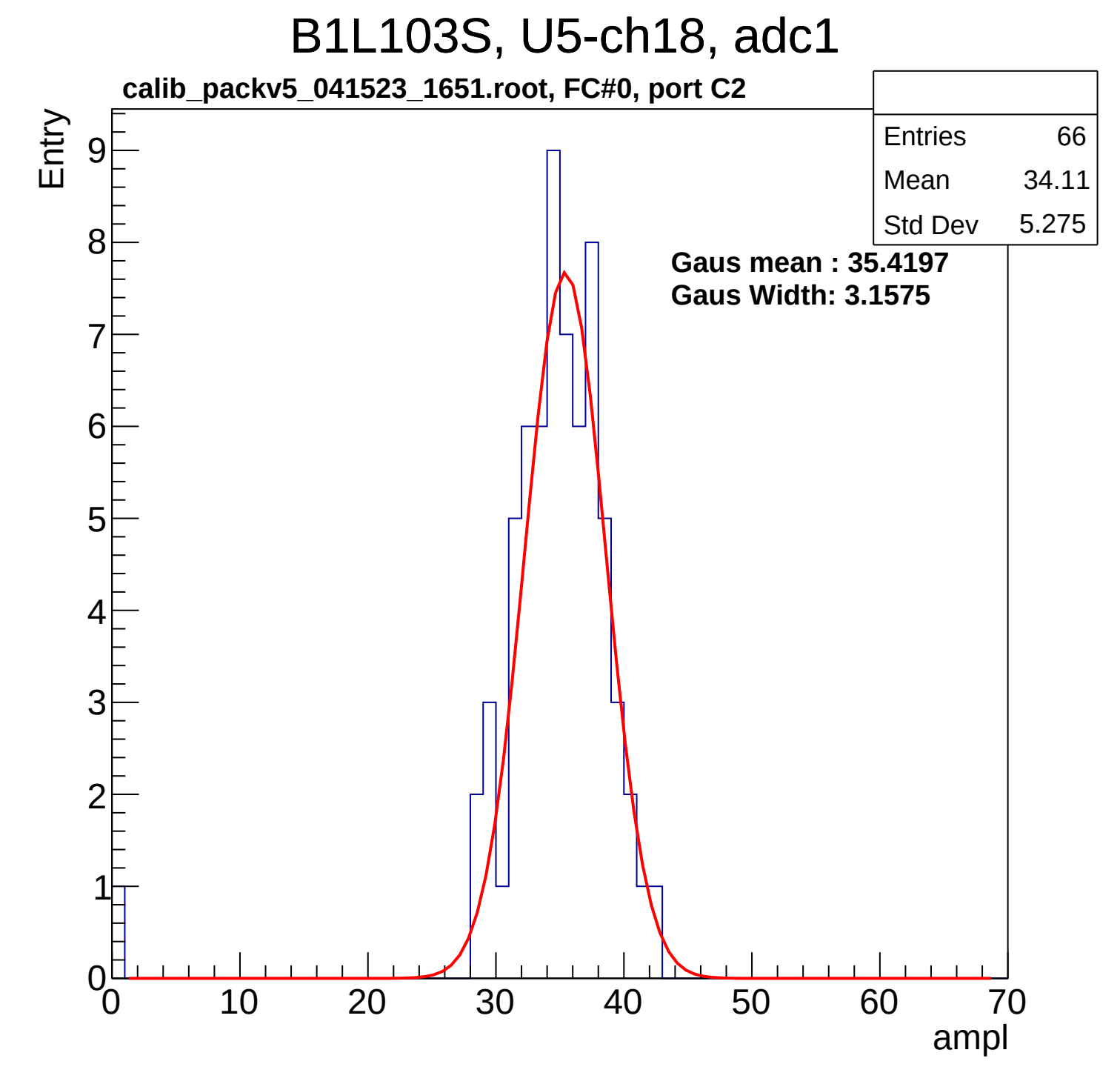
B1L103S, U5-ch18, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 34.11
Std Dev 5.275
Gaus mean : 35.4197
Gaus Width: 3.1575
Entry
ampl
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3
4
5
6
7
8
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0
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20
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40
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60
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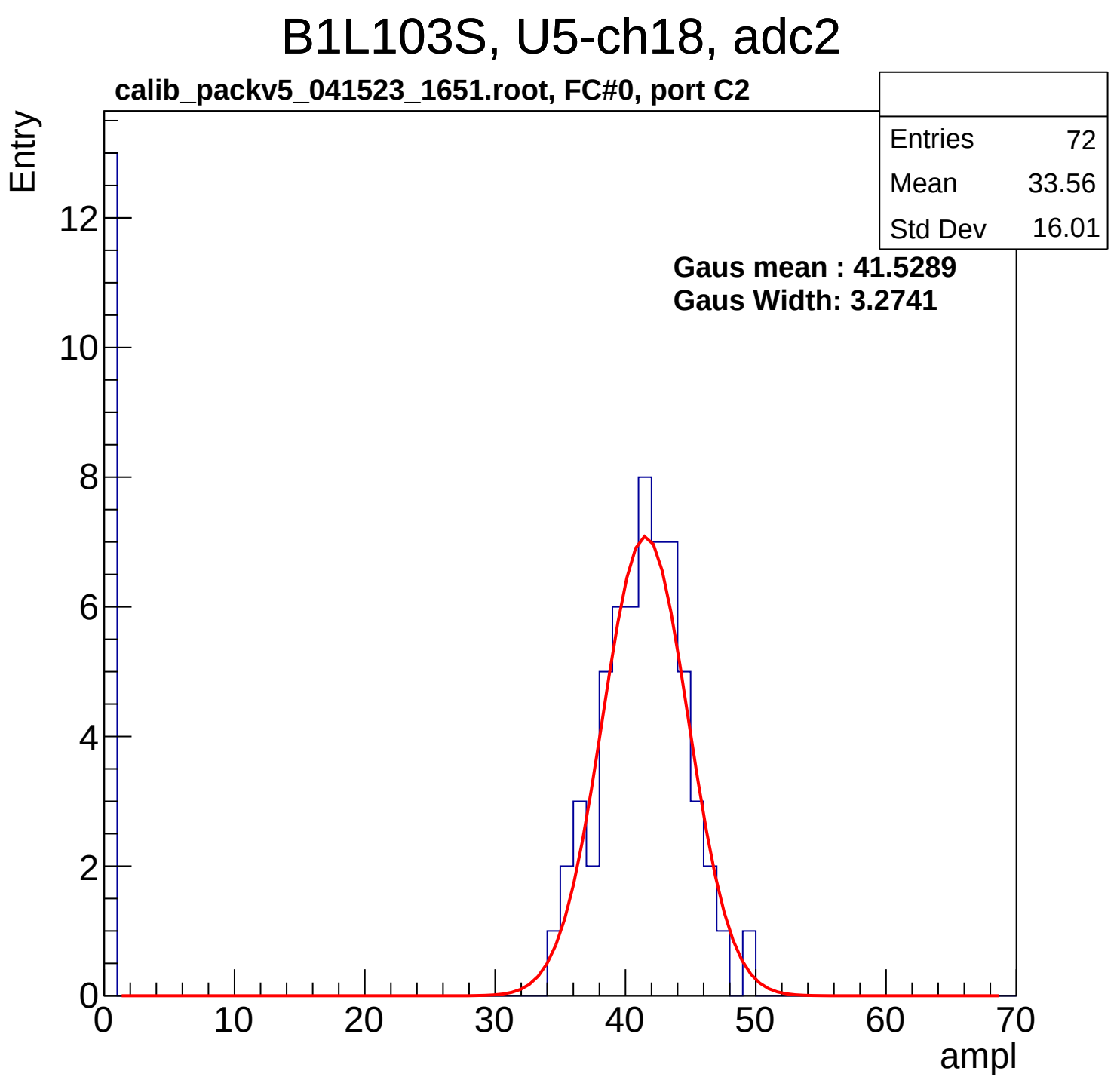
B1L103S, U5-ch18, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 33.56
Std Dev 16.01
Gaus mean : 41.5289
Gaus Width: 3.2741
Entry
ampl
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6
8
10
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0
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20
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40
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60
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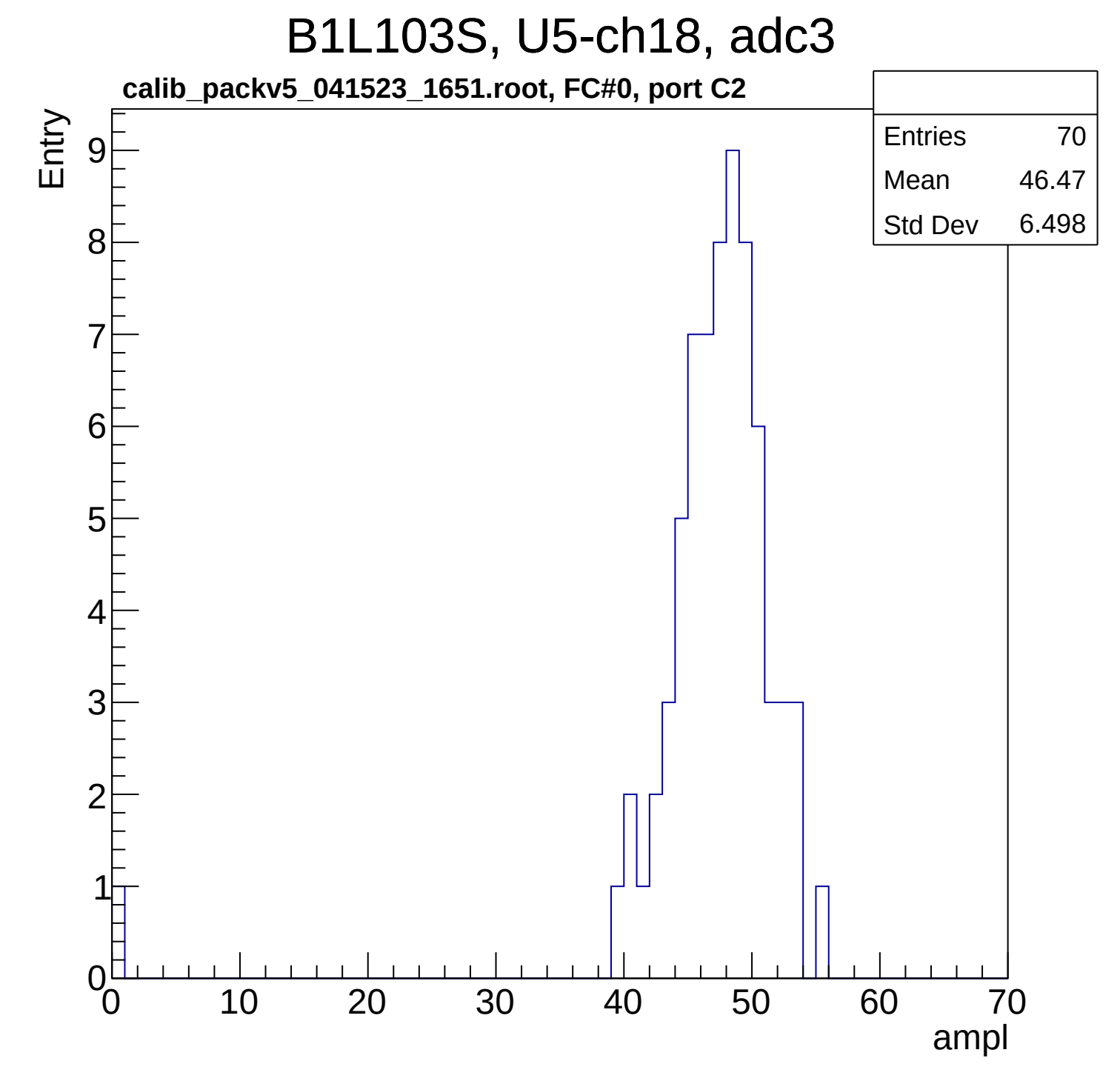
B1L103S, U5-ch18, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 46.47
Std Dev 6.498
Entry
ampl
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4
5
6
7
8
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0
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40
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60
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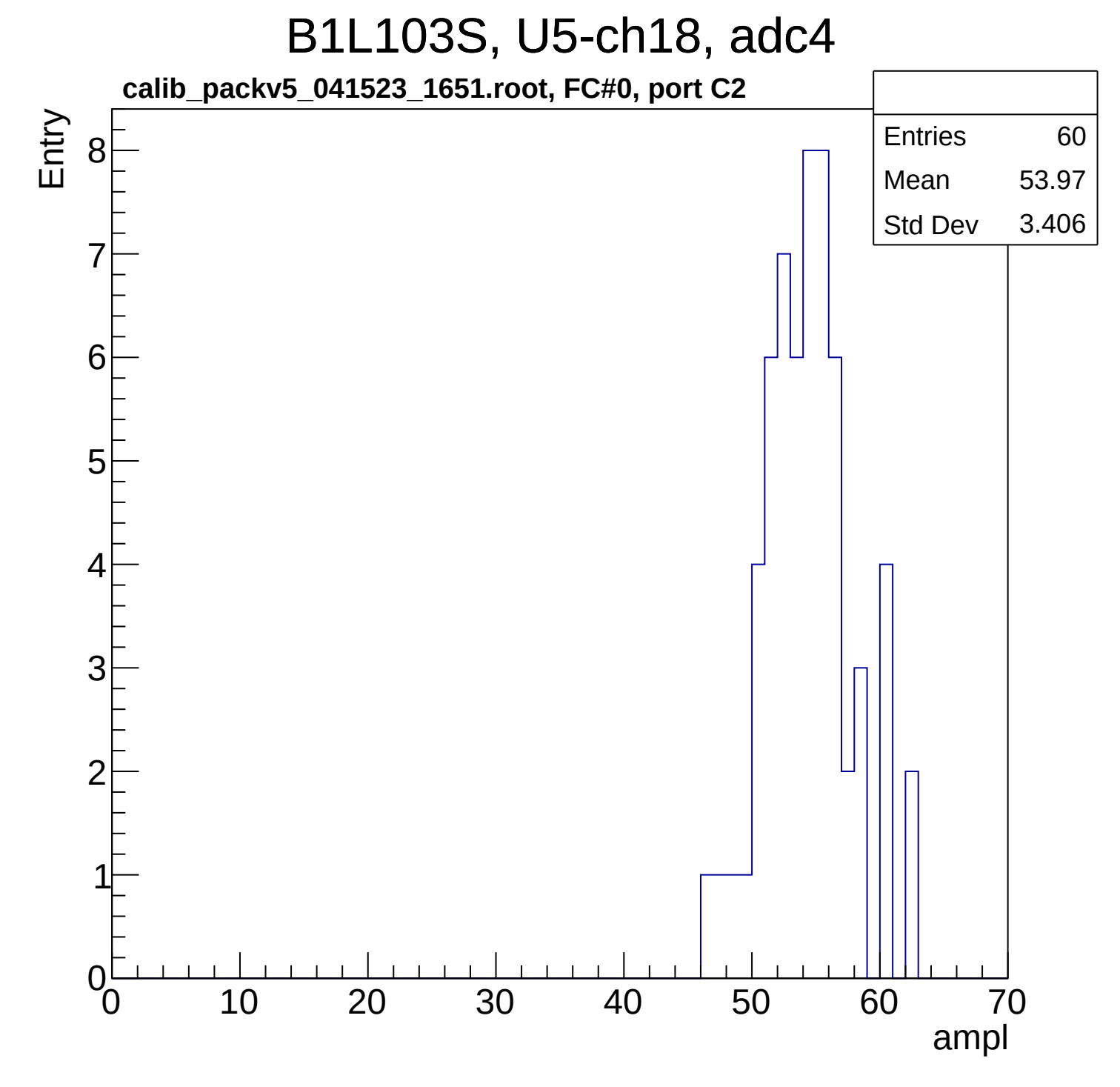
B1L103S, U5-ch18, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 53.97
Std Dev 3.406
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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60
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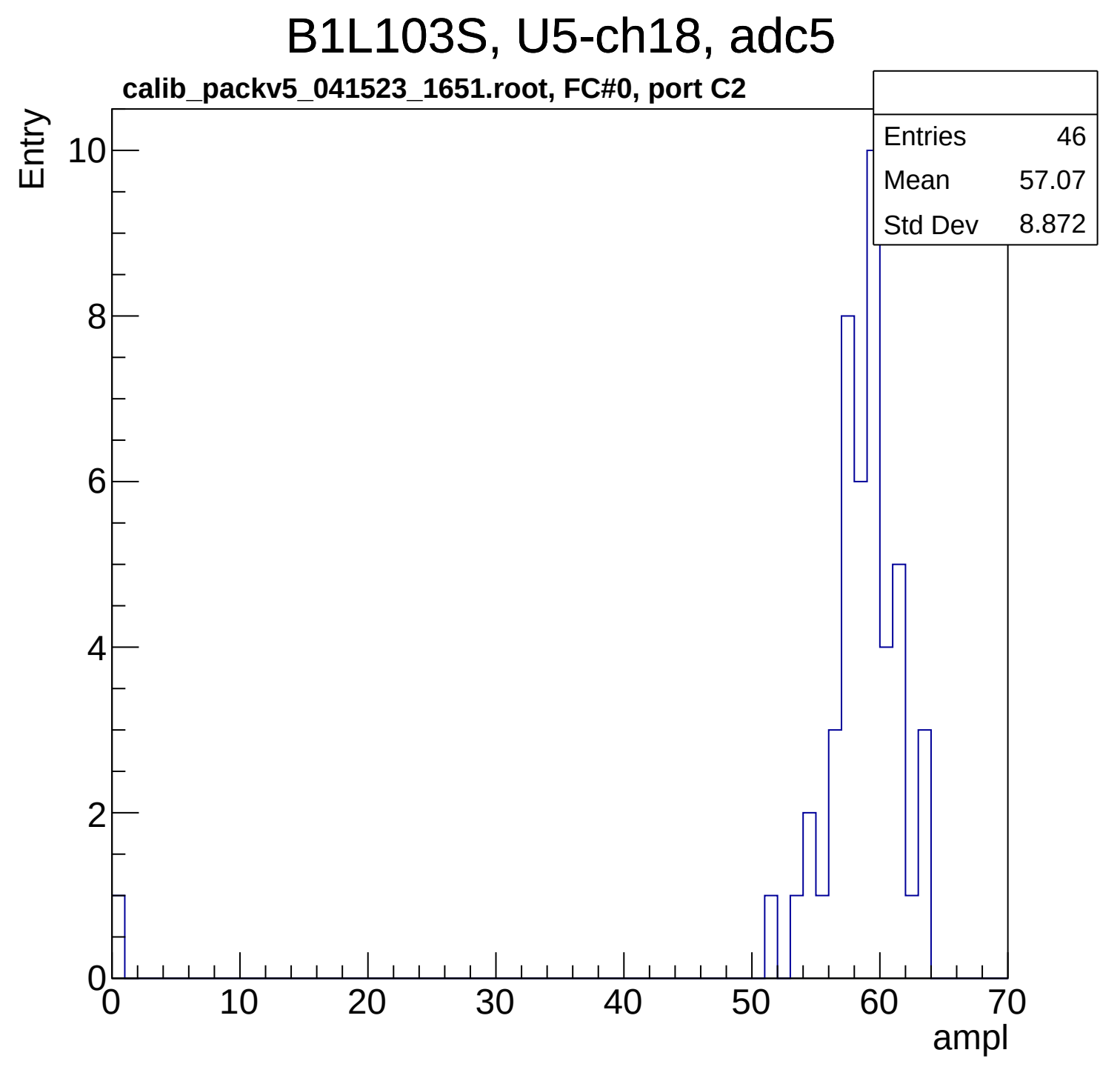
B1L103S, U5-ch18, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 57.07
Std Dev 8.872
Entry
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4
6
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10
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10
20
30
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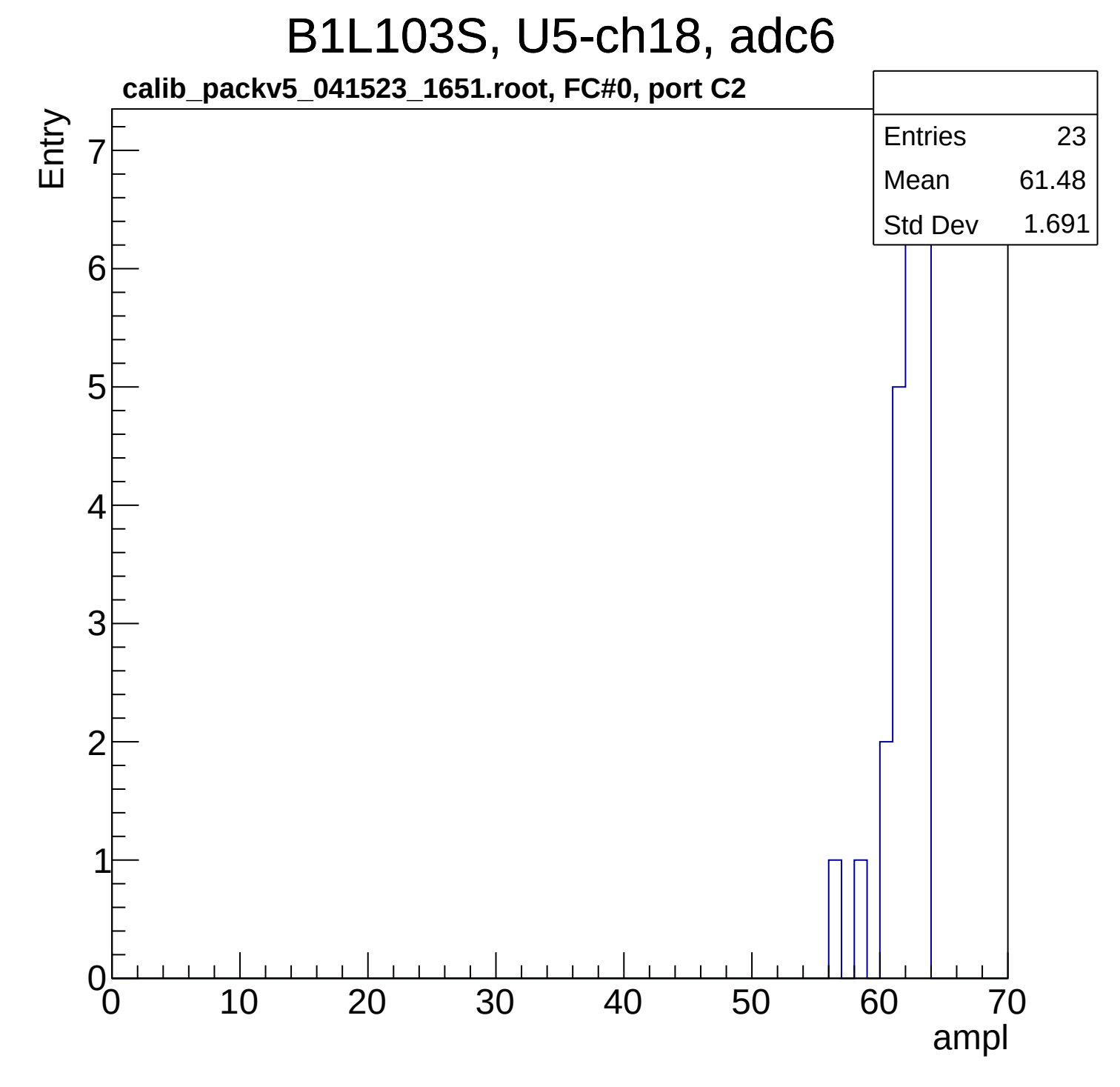
50
60
70
ampl


B1L103S, U5-ch18, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 61.48
Std Dev 1.691
Entry
ampl
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1
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3
4
5
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7
0
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20
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40
50
60
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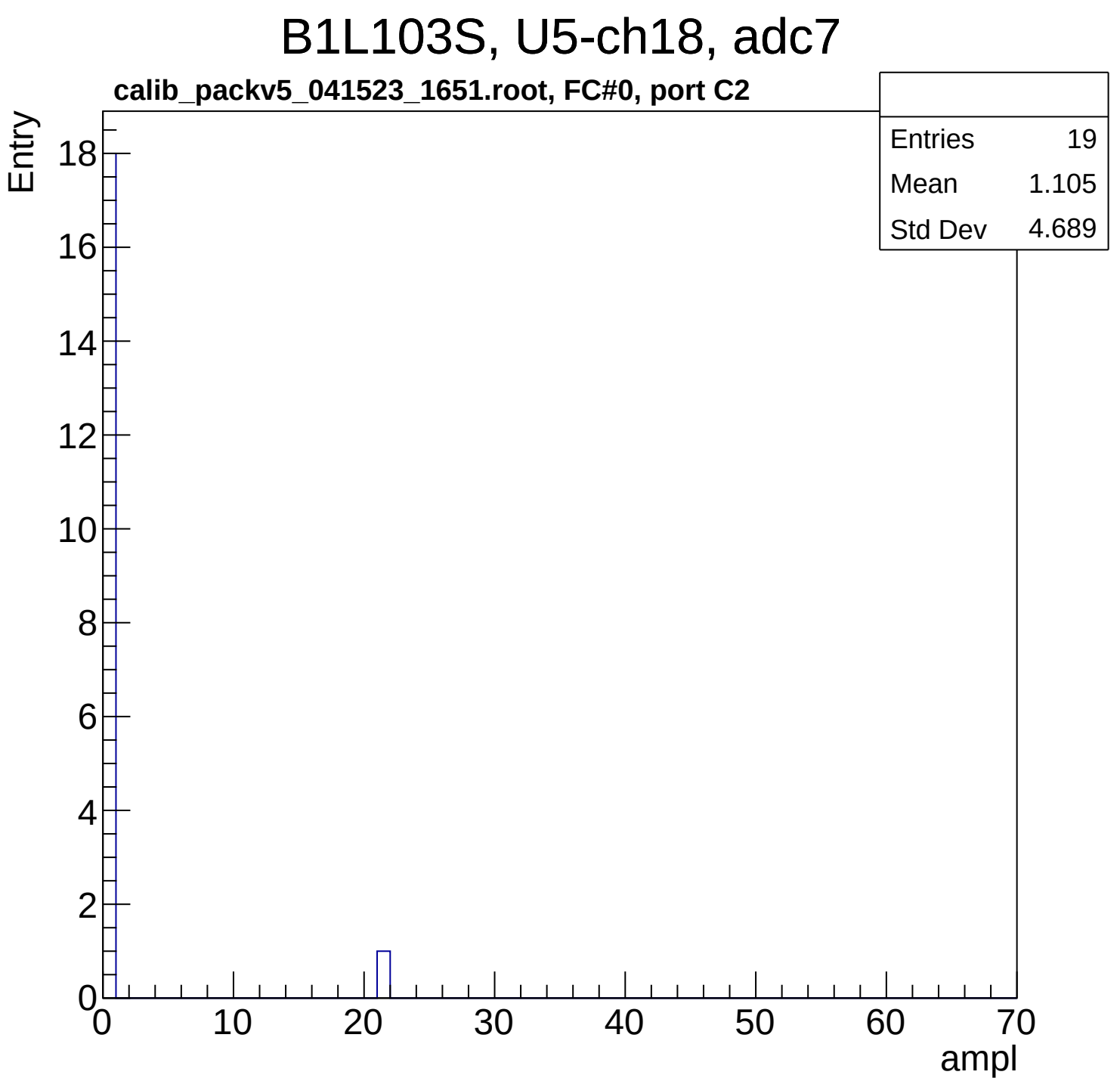
B1L103S, U5-ch18, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
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6
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10
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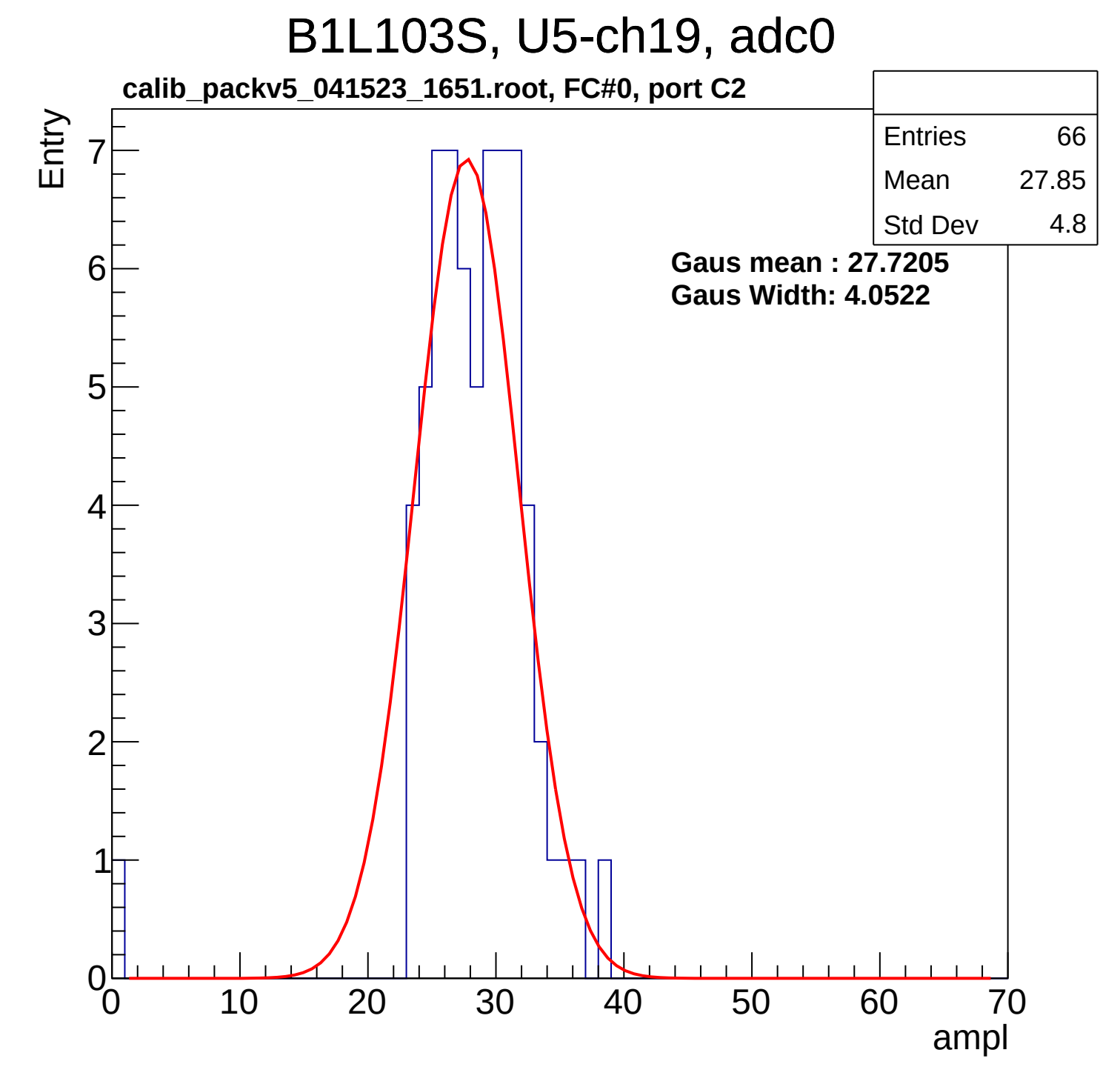
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch19, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 27.85
Std Dev 4.8
Gaus mean : 27.7205
Gaus Width: 4.0522
Entry
ampl
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1
2
3
4
5
6
7
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40
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60
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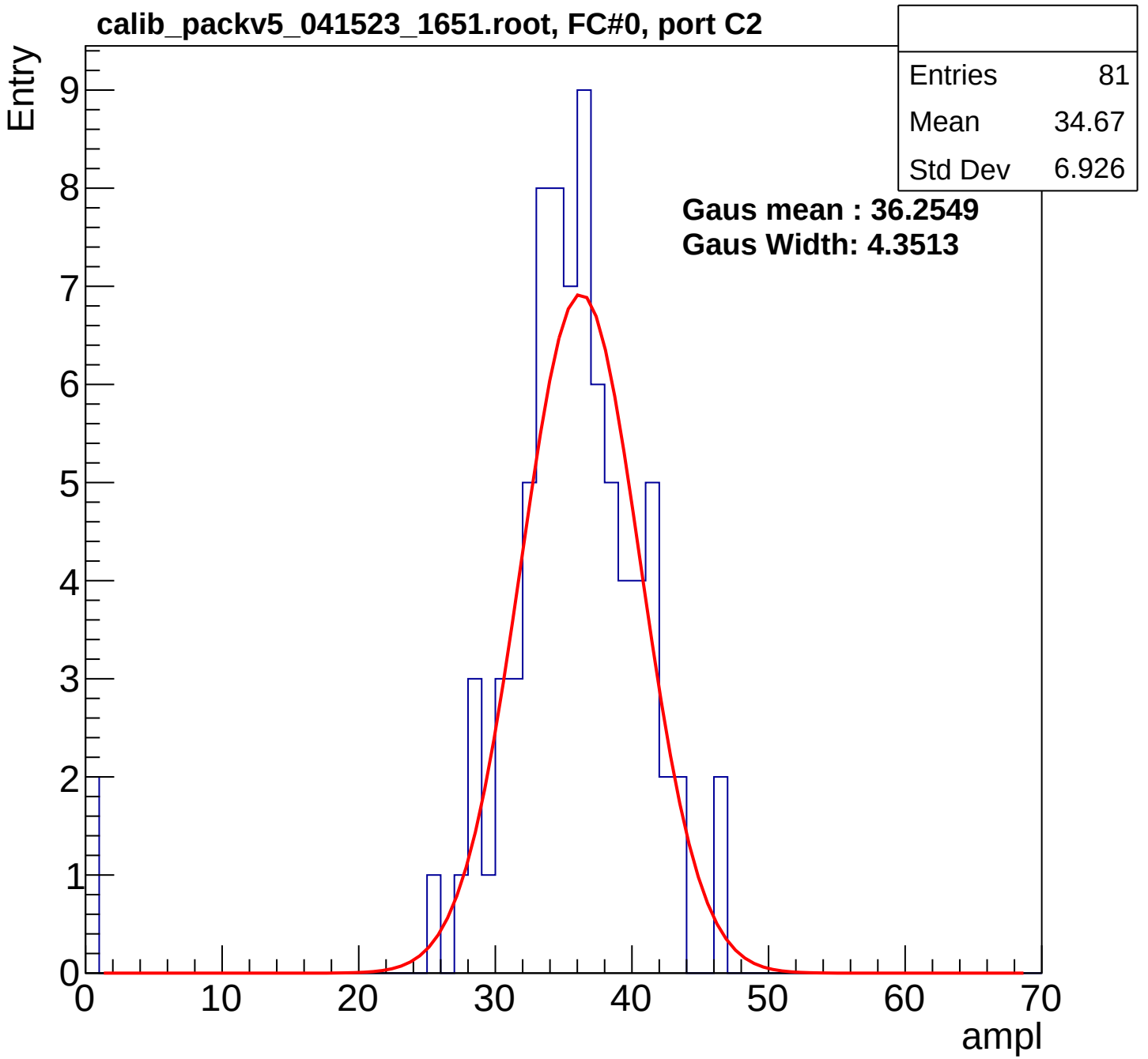
B1L103S, U5-ch19, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 34.67
Std Dev 6.926
Gaus mean : 36.2549
Gaus Width: 4.3513
Entry
ampl
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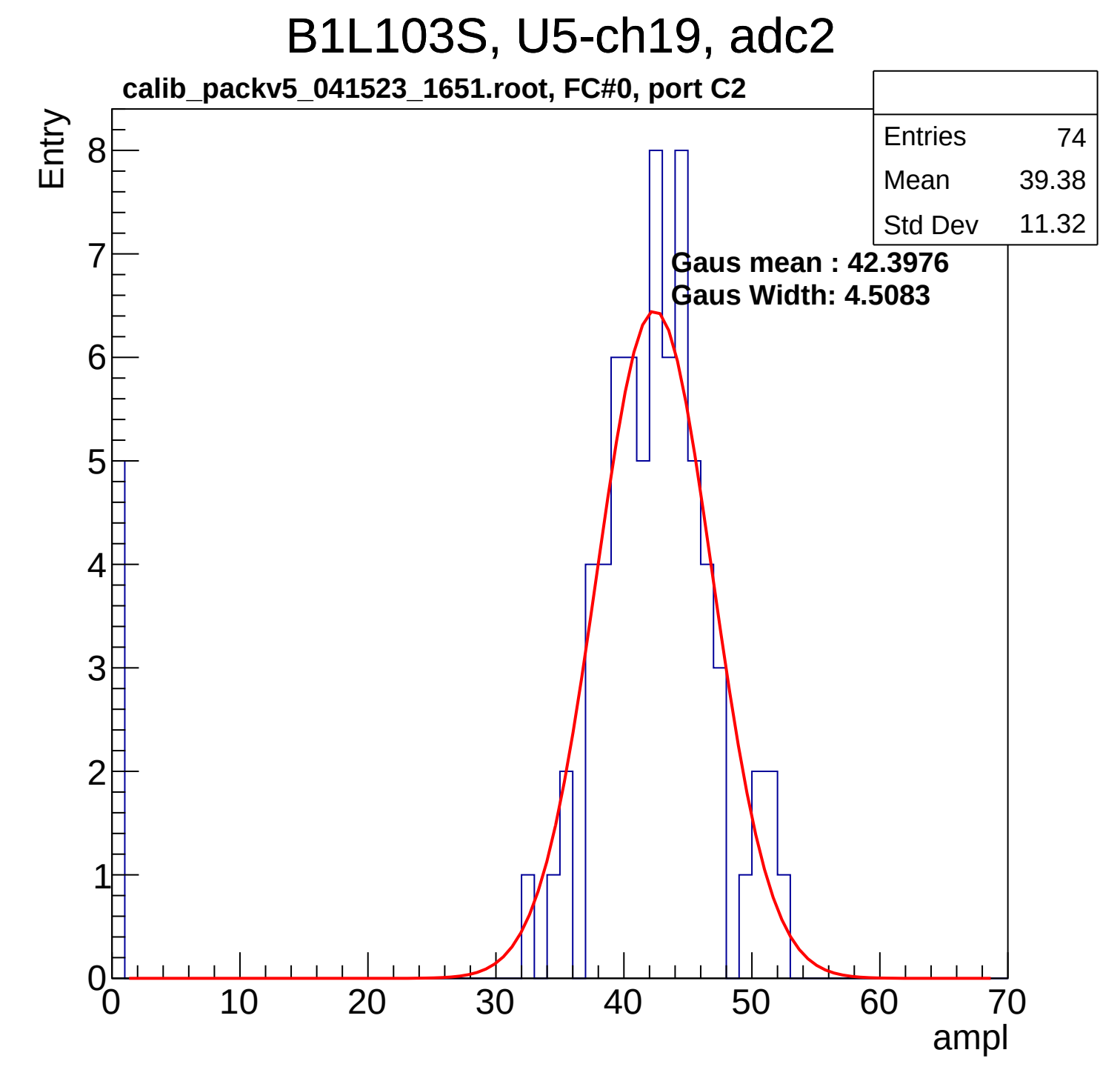
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U5-ch19, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 39.38
Std Dev 11.32
Gaus mean : 42.3976
Gaus Width: 4.5083
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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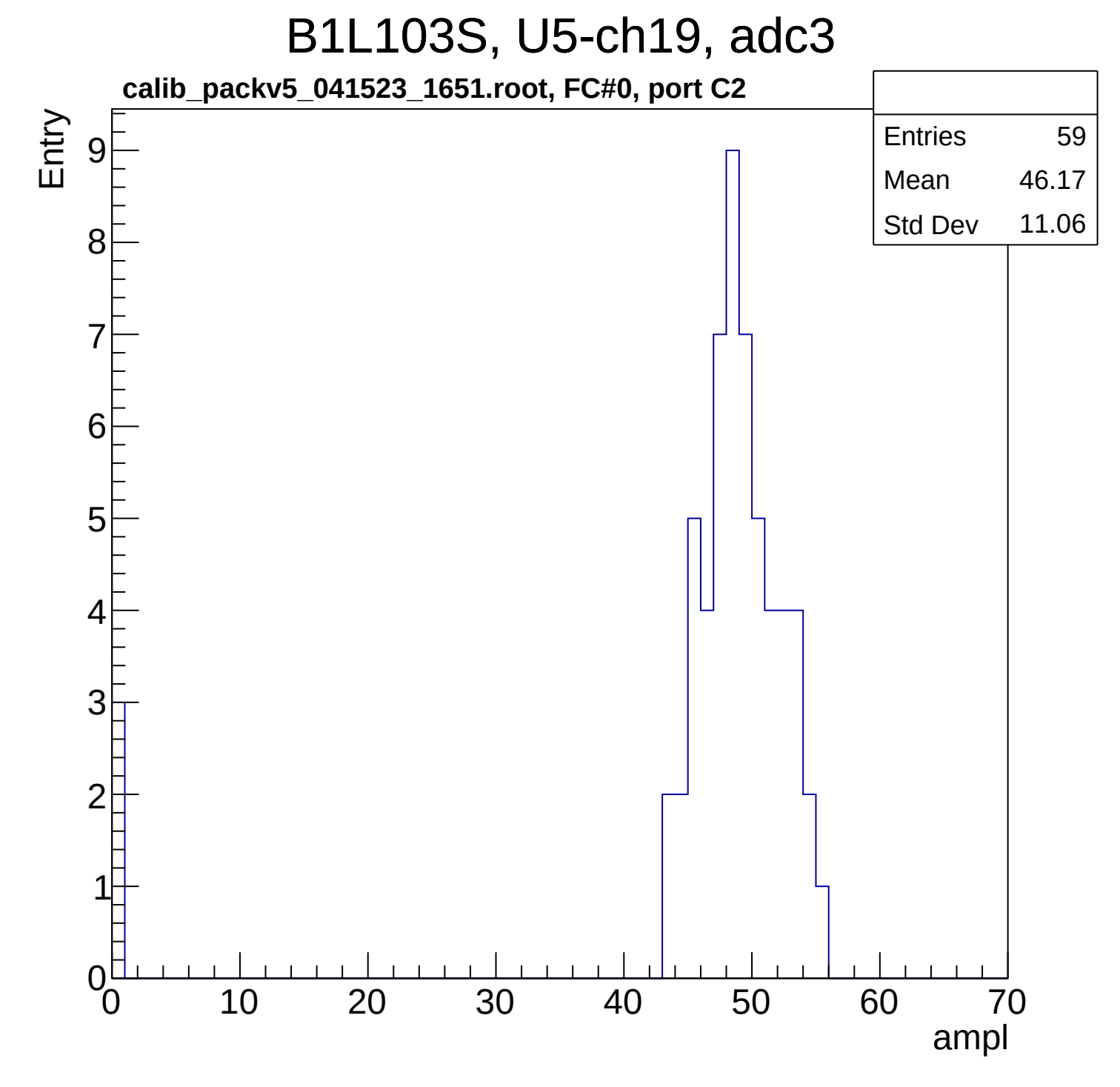
B1L103S, U5-ch19, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 46.17
Std Dev 11.06
Entry
ampl
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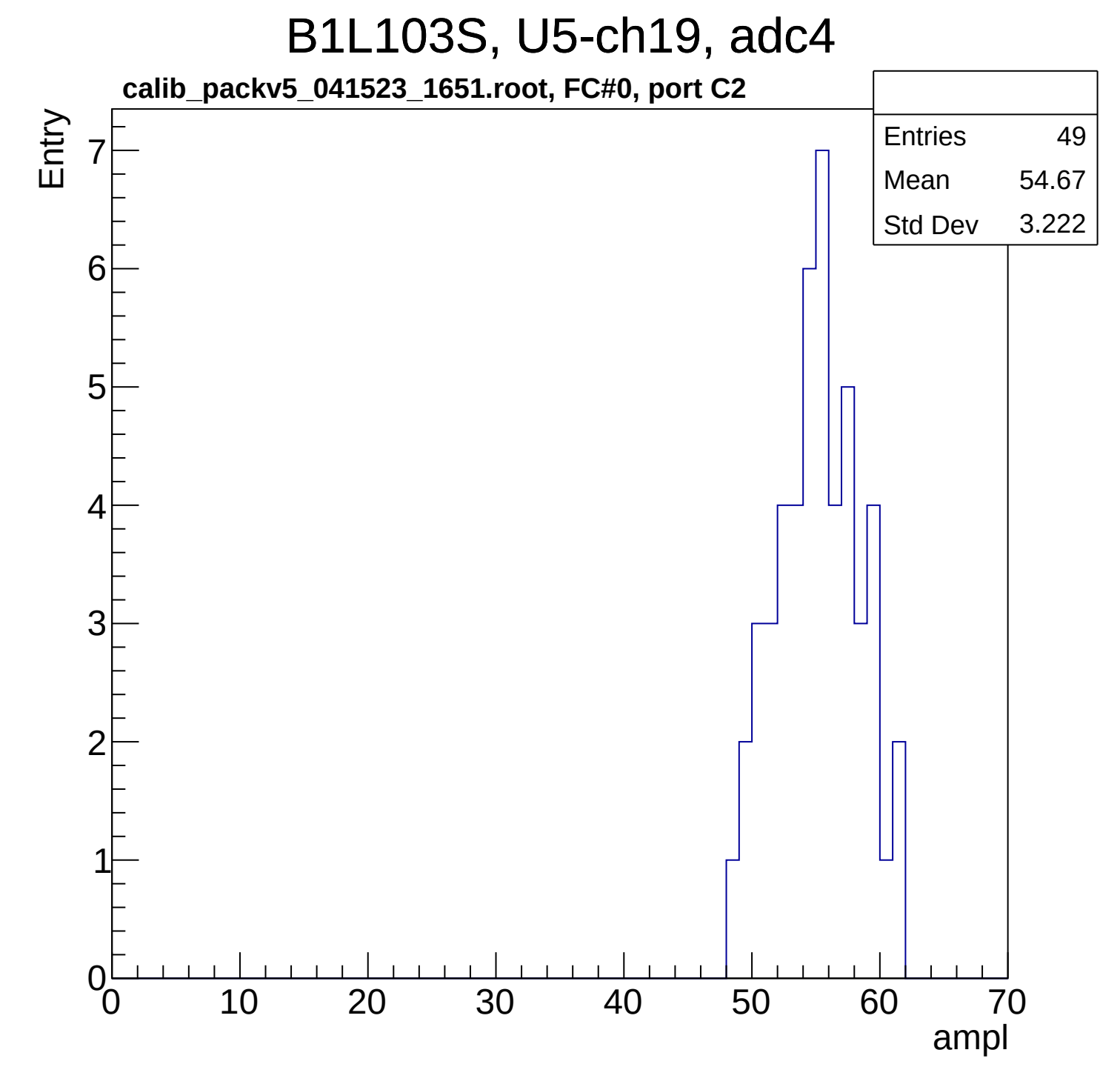
B1L103S, U5-ch19, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 54.67
Std Dev 3.222
Entry
ampl
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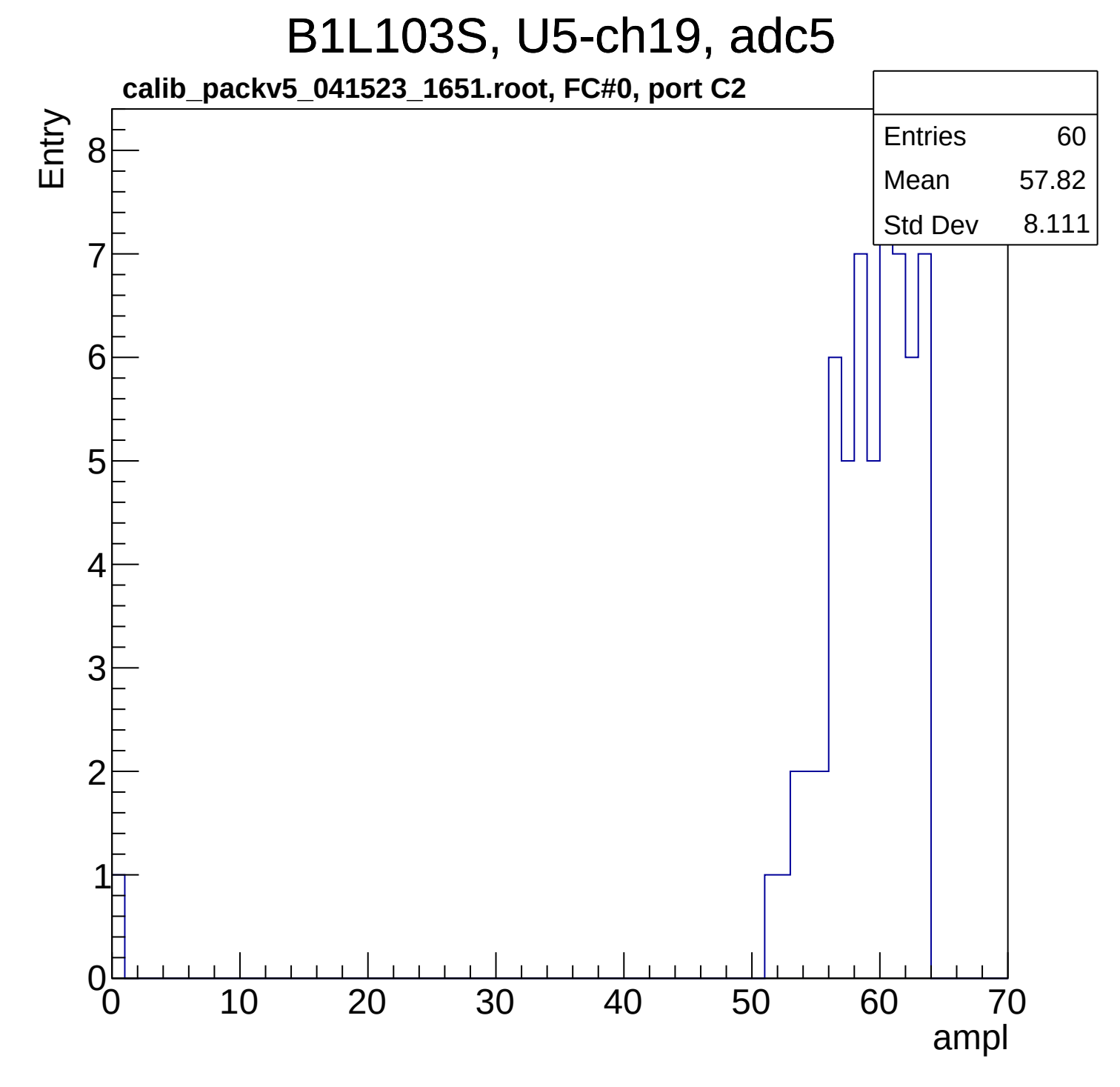
B1L103S, U5-ch19, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 57.82
Std Dev 8.111
Entry
ampl
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1
2
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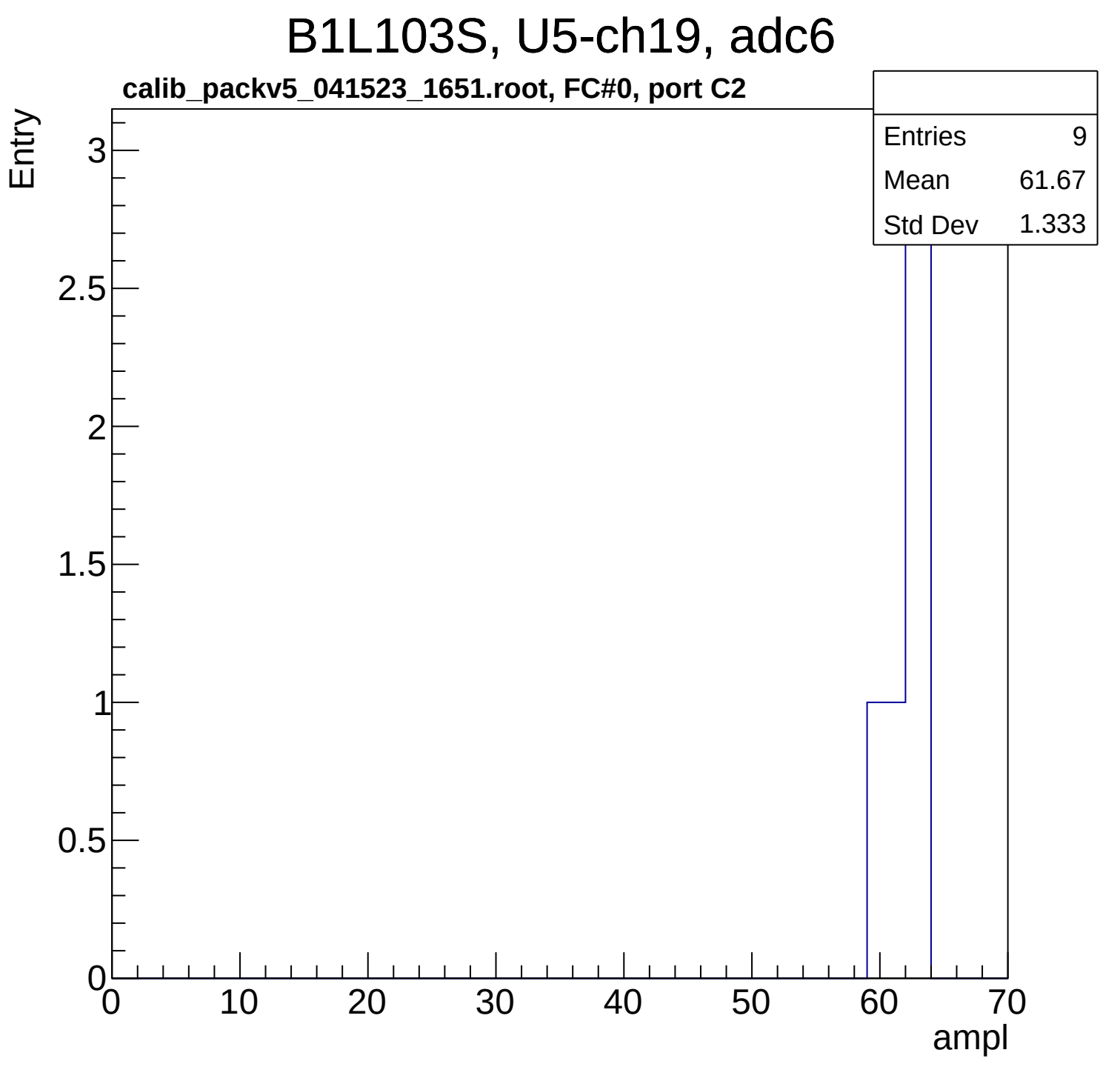
B1L103S, U5-ch19, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.67
Std Dev 1.333
Entry
ampl
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0.5
1
1.5
2
2.5
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0
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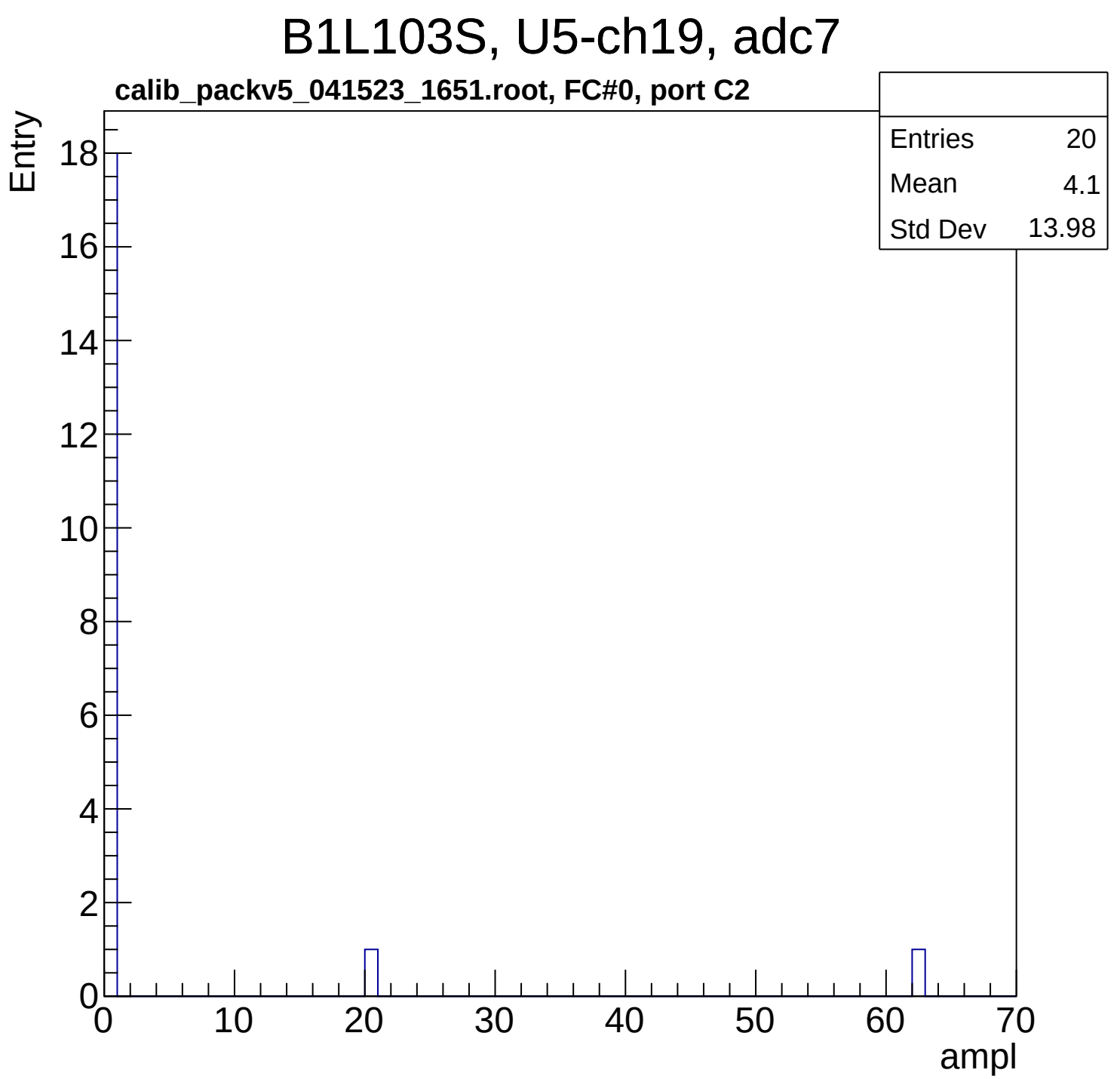
B1L103S, U5-ch19, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.1
Std Dev 13.98
Entry
0
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6
8
10
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14
16
18
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10
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60
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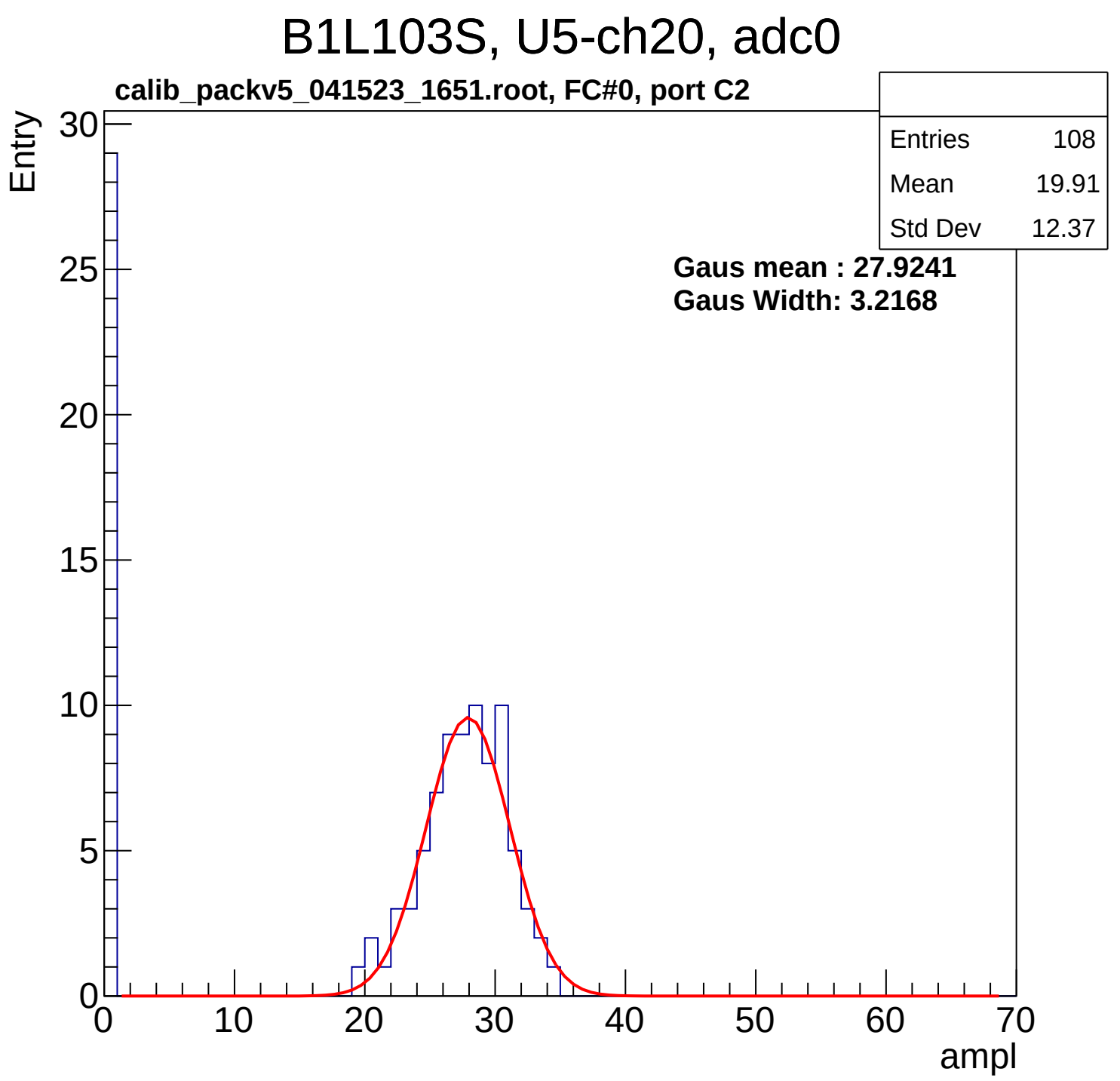
ampl


B1L103S, U5-ch20, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 108
Mean 19.91
Std Dev 12.37
Gaus mean : 27.9241
Gaus Width: 3.2168
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
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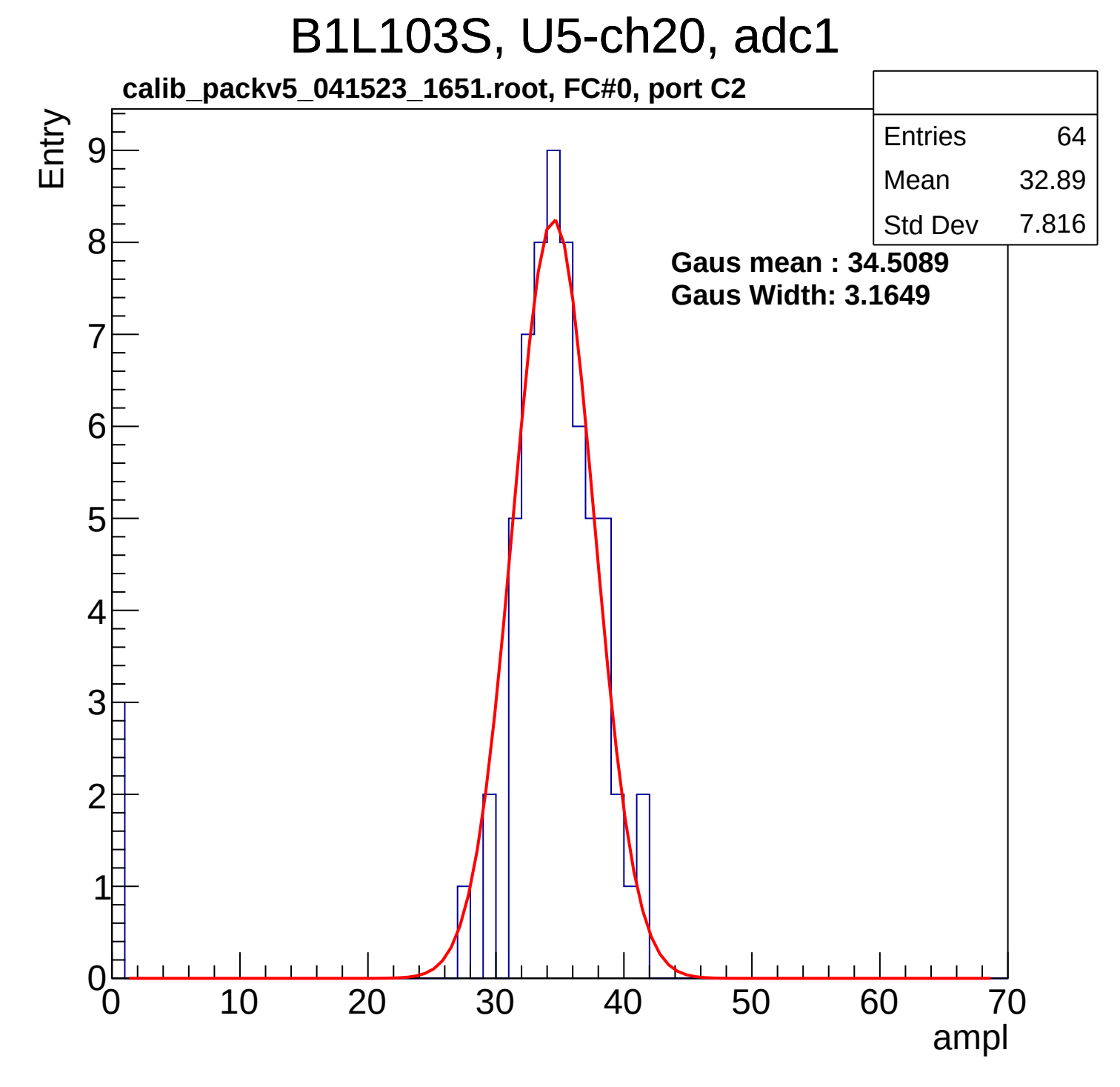
B1L103S, U5-ch20, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 32.89
Std Dev 7.816
Gaus mean : 34.5089
Gaus Width: 3.1649
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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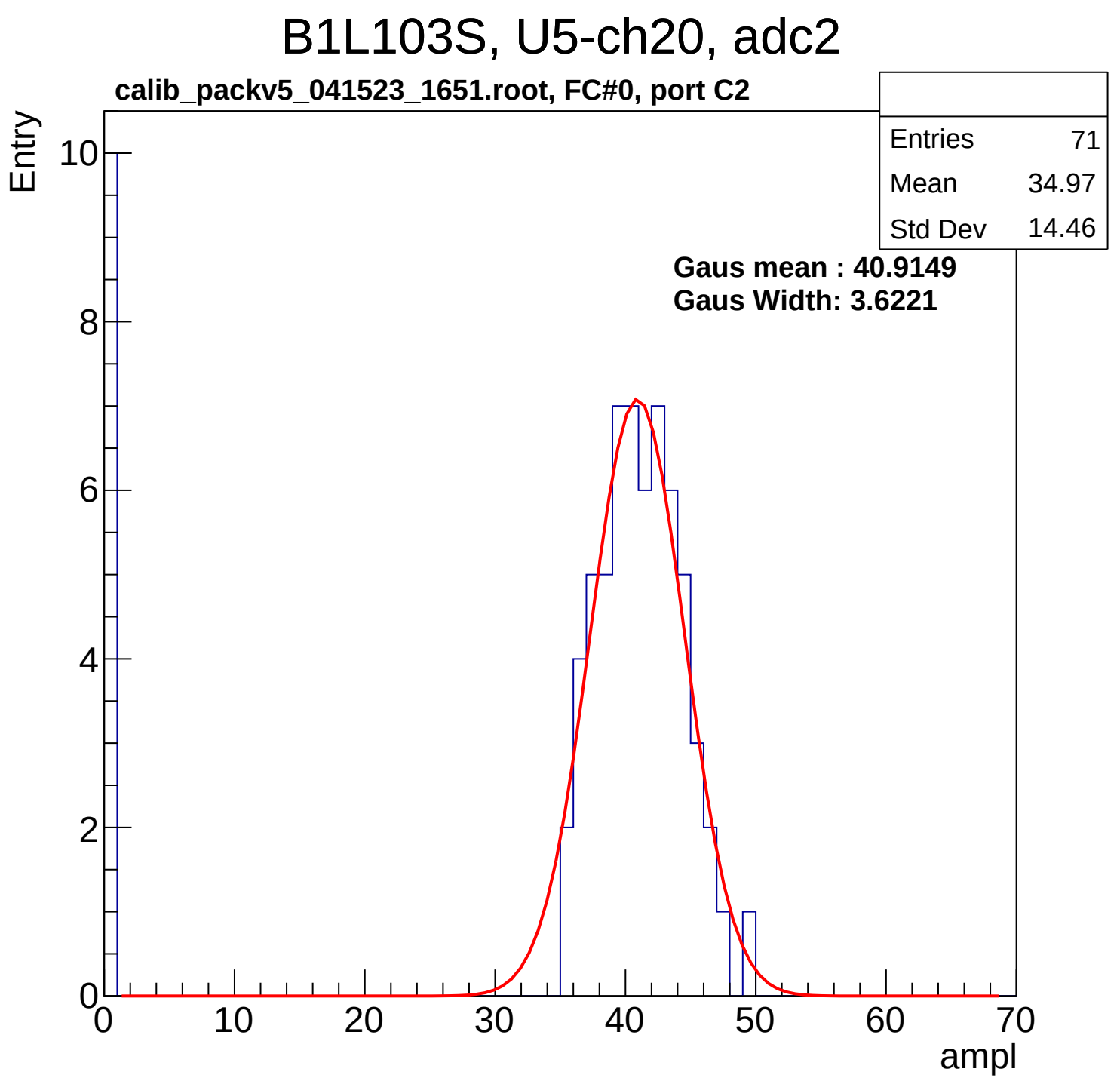
B1L103S, U5-ch20, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 34.97
Std Dev 14.46
Gaus mean : 40.9149
Gaus Width: 3.6221
Entry
ampl
0
2
4
6
8
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0
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40
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60
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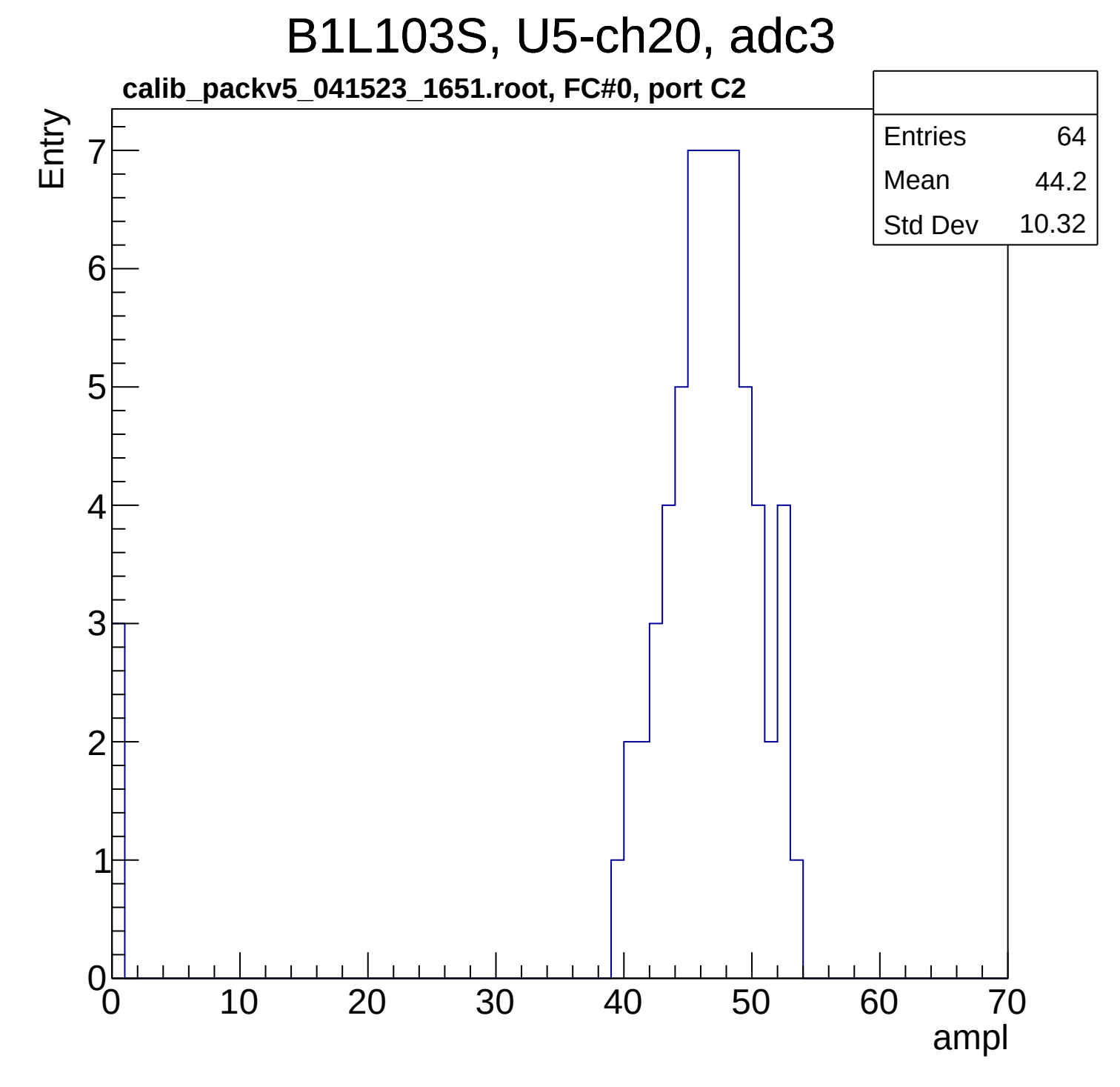
B1L103S, U5-ch20, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 44.2
Std Dev 10.32
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
50
60
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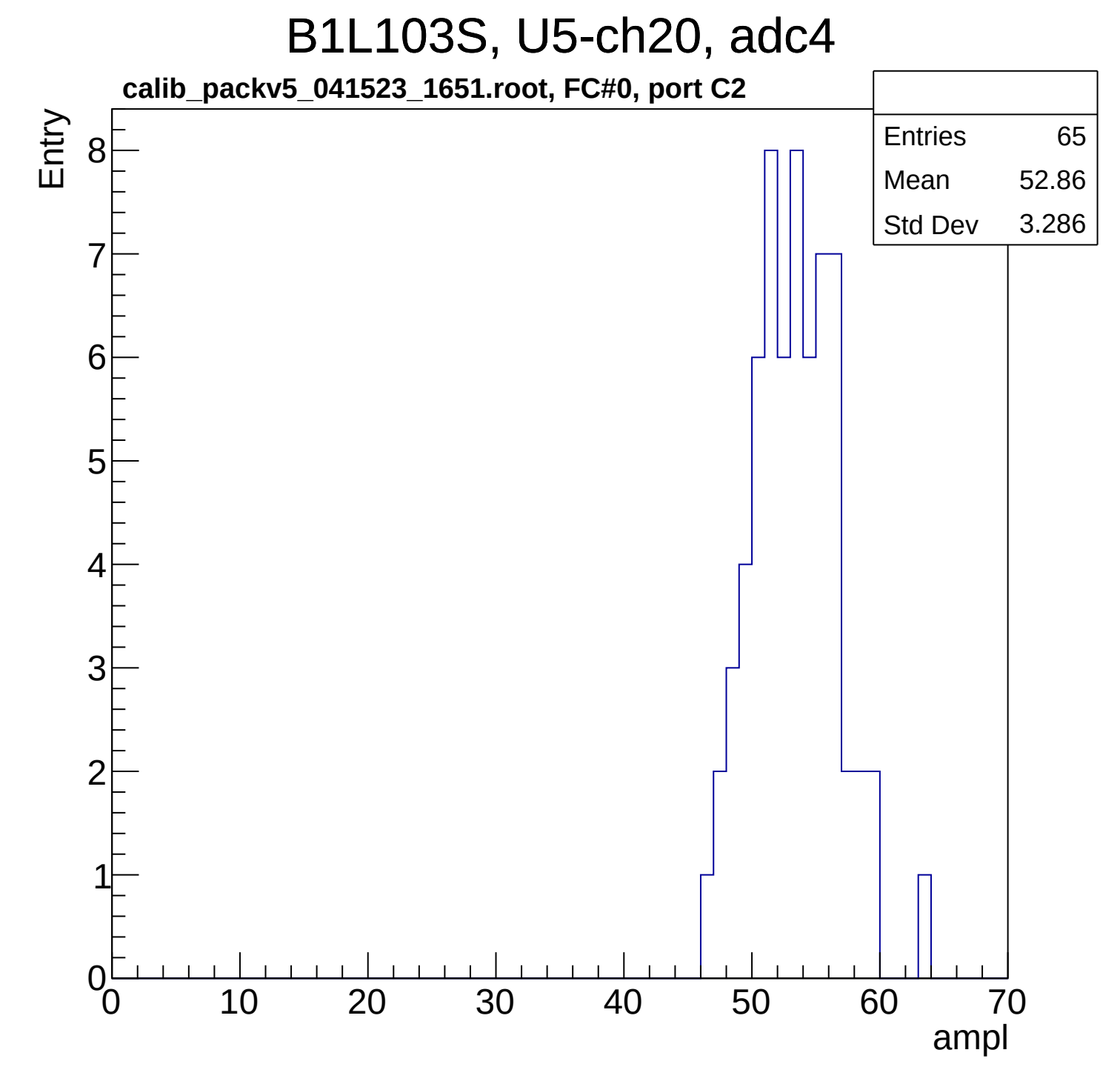
B1L103S, U5-ch20, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 52.86
Std Dev 3.286
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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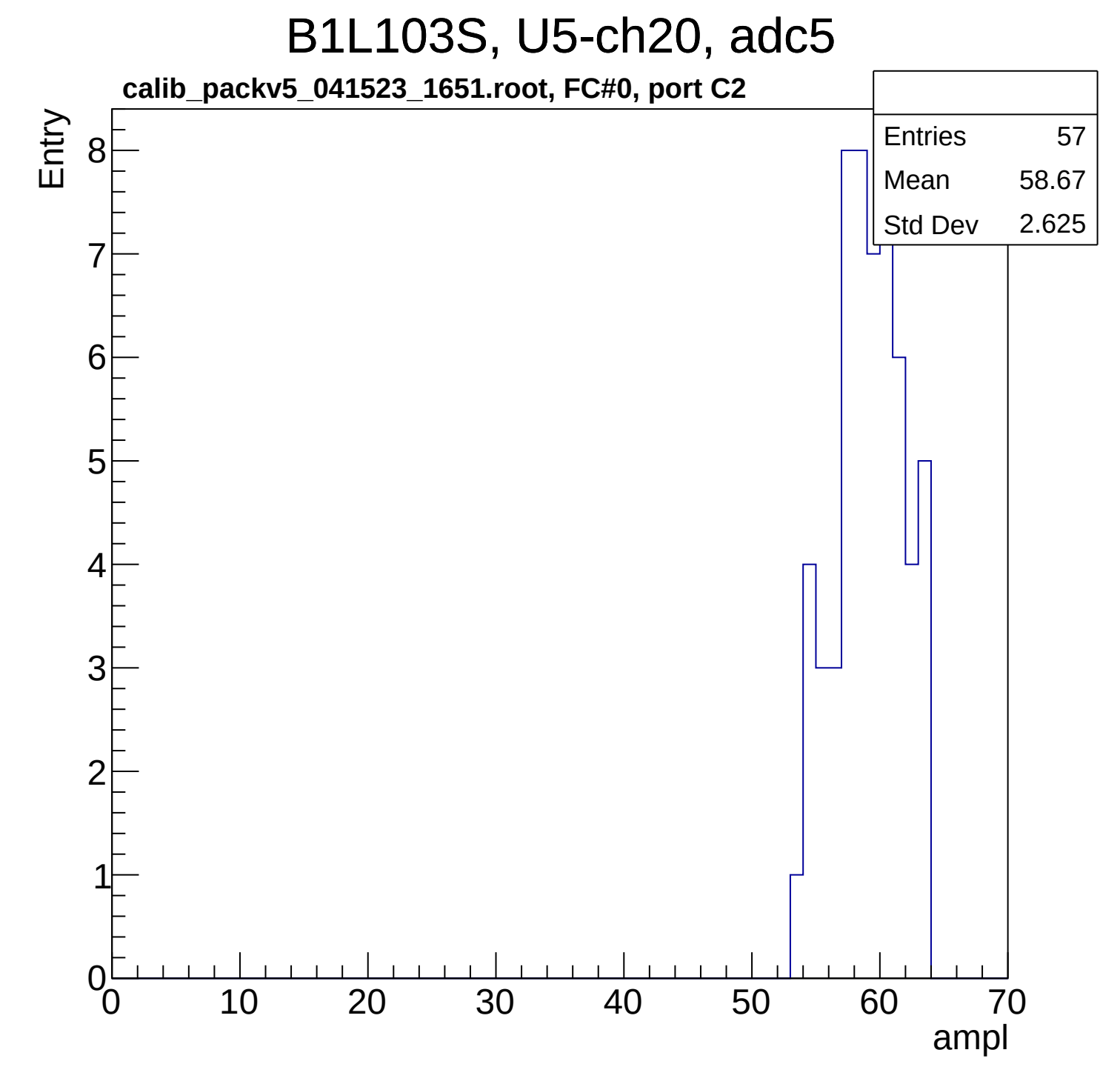
B1L103S, U5-ch20, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.67
Std Dev 2.625
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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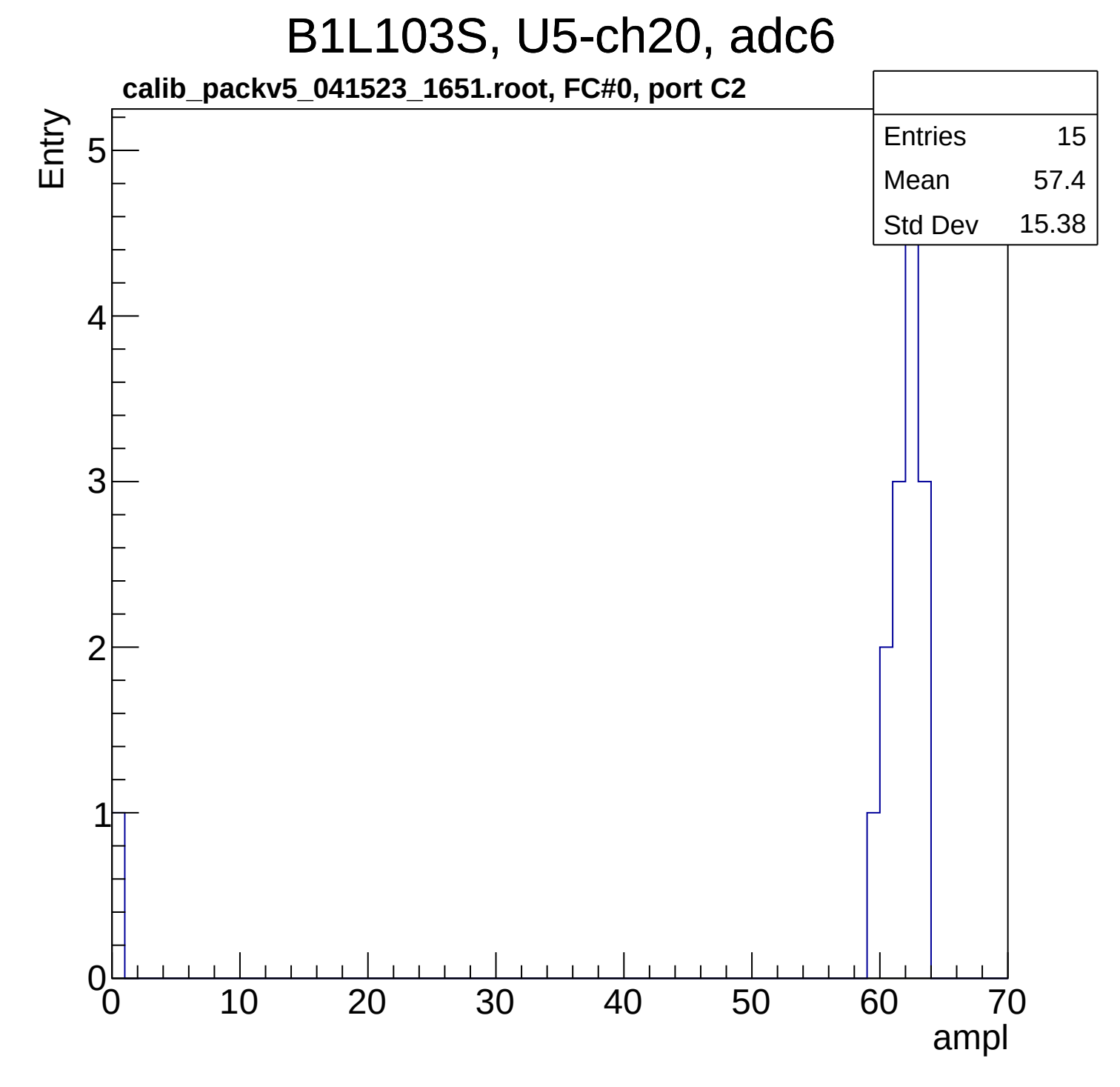
B1L103S, U5-ch20, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.4
Std Dev 15.38
Entry
ampl
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3
4
5
0
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20
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40
50
60
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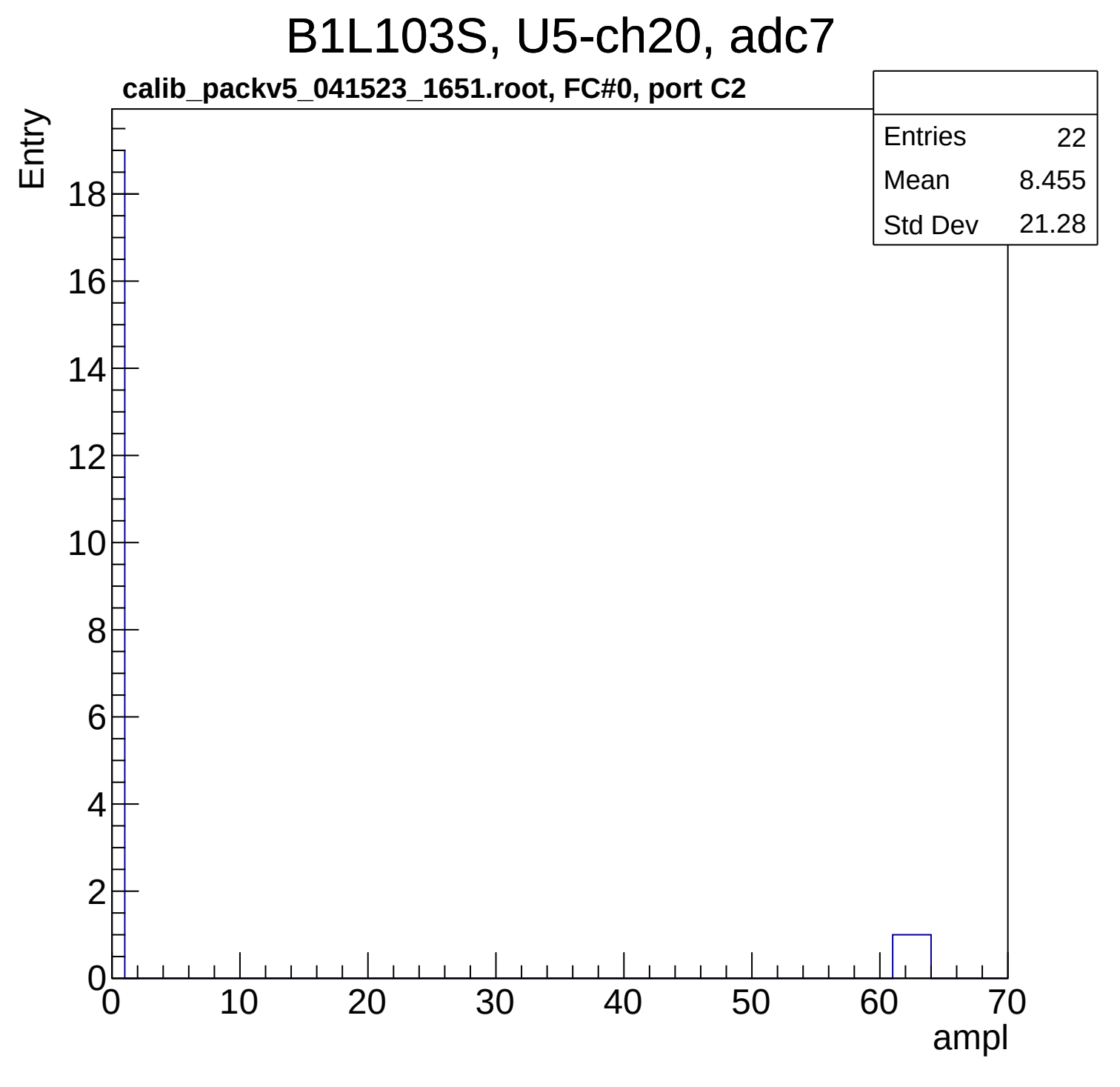
B1L103S, U5-ch20, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.455
Std Dev 21.28
Entry
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6
8
10
12
14
16
18
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10
20
30
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50
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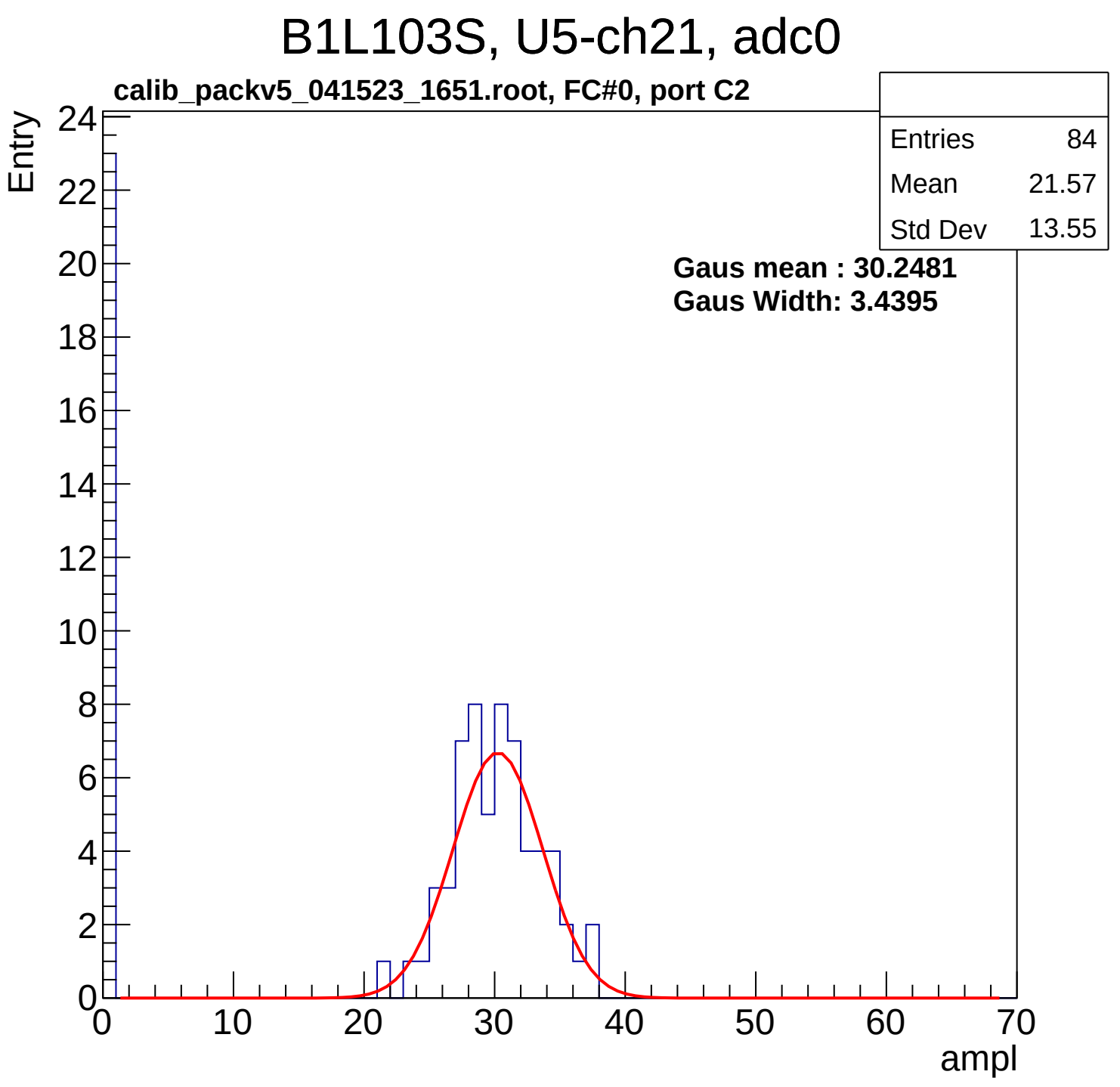
70
ampl


B1L103S, U5-ch21, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 21.57
Std Dev 13.55
Gaus mean : 30.2481
Gaus Width: 3.4395
Entry
ampl
0
2
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6
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10
12
14
16
18
20
22
24
0
10
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30
40
50
60
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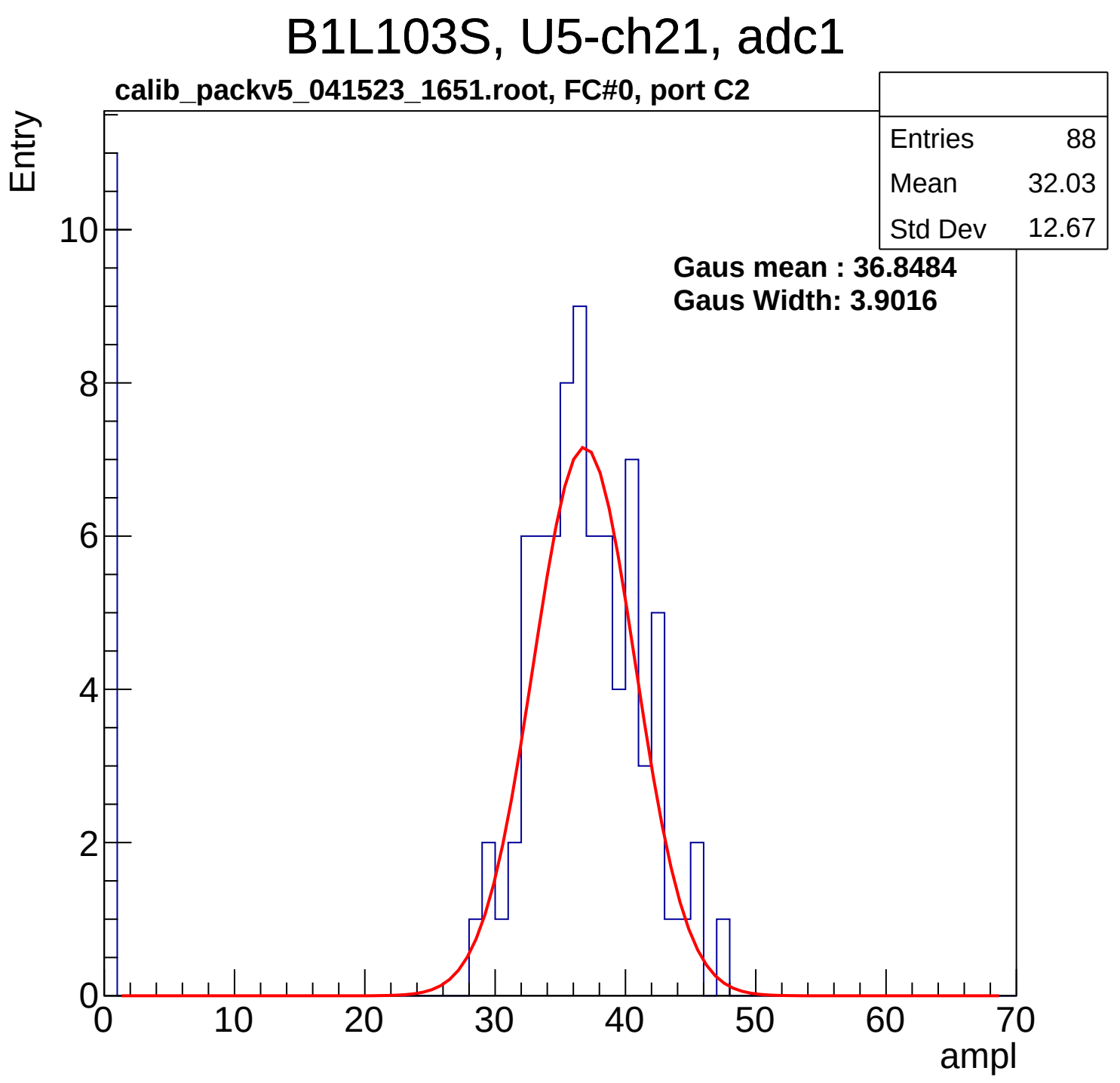
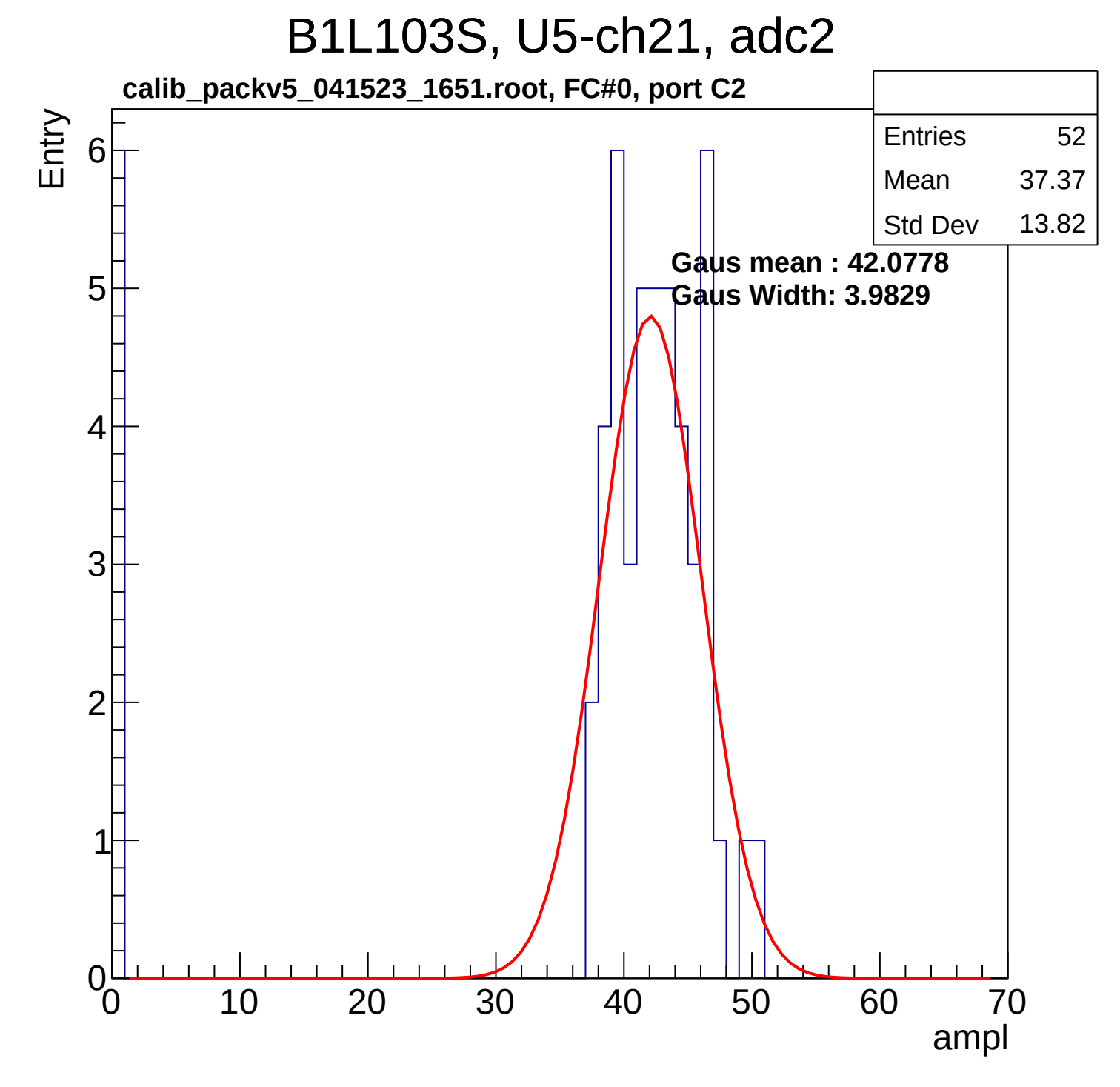

B1L103S, U5-ch21, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 32.03
Std Dev 12.67
Gaus mean : 36.8484
Gaus Width: 3.9016
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U5-ch21, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 37.37
Std Dev 13.82
Gaus mean : 42.0778
Gaus Width: 3.9829
Entry
ampl
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1
2
3
4
5
6
0
10
20
30
40
50
60
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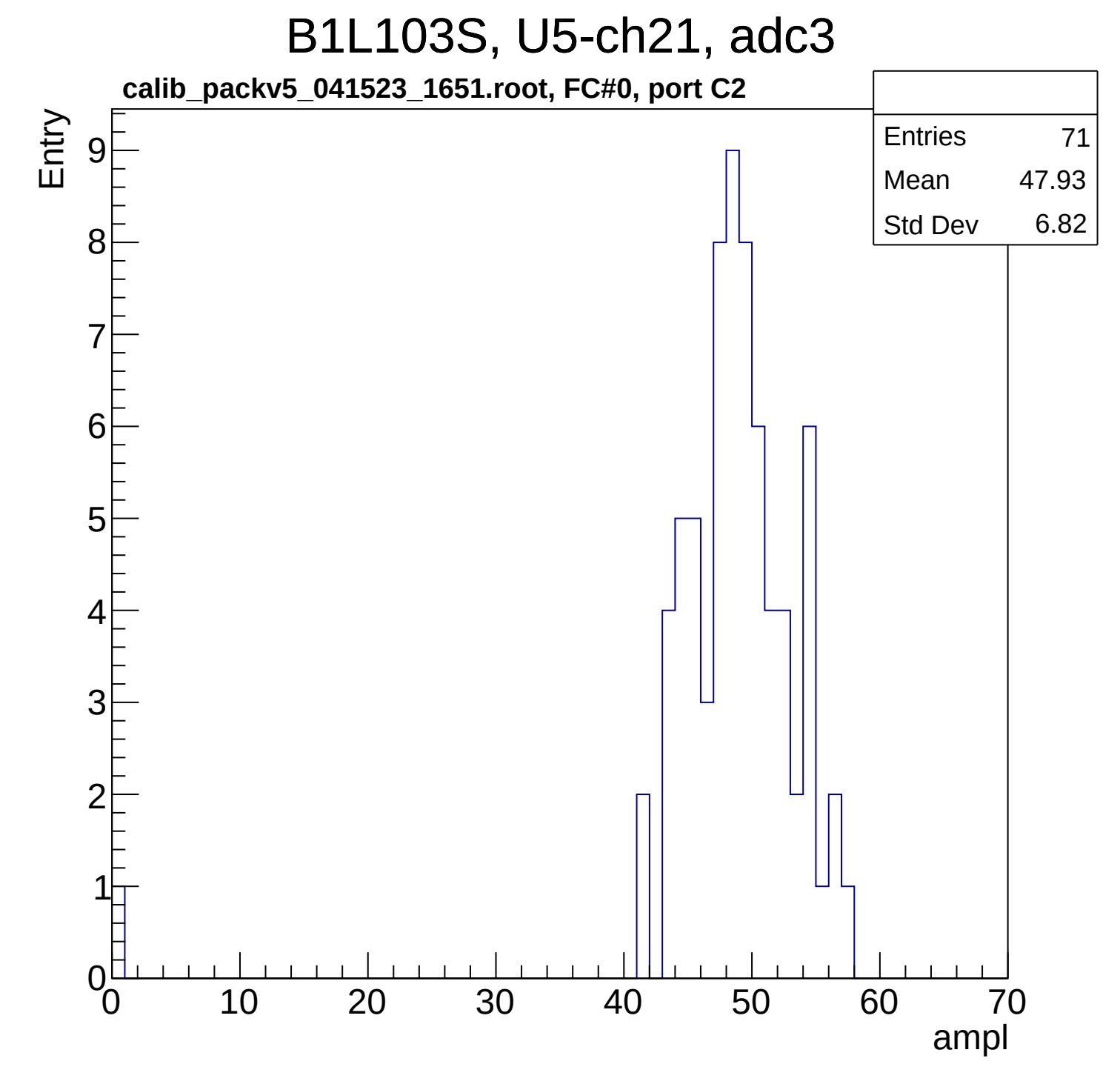
B1L103S, U5-ch21, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 47.93
Std Dev 6.82
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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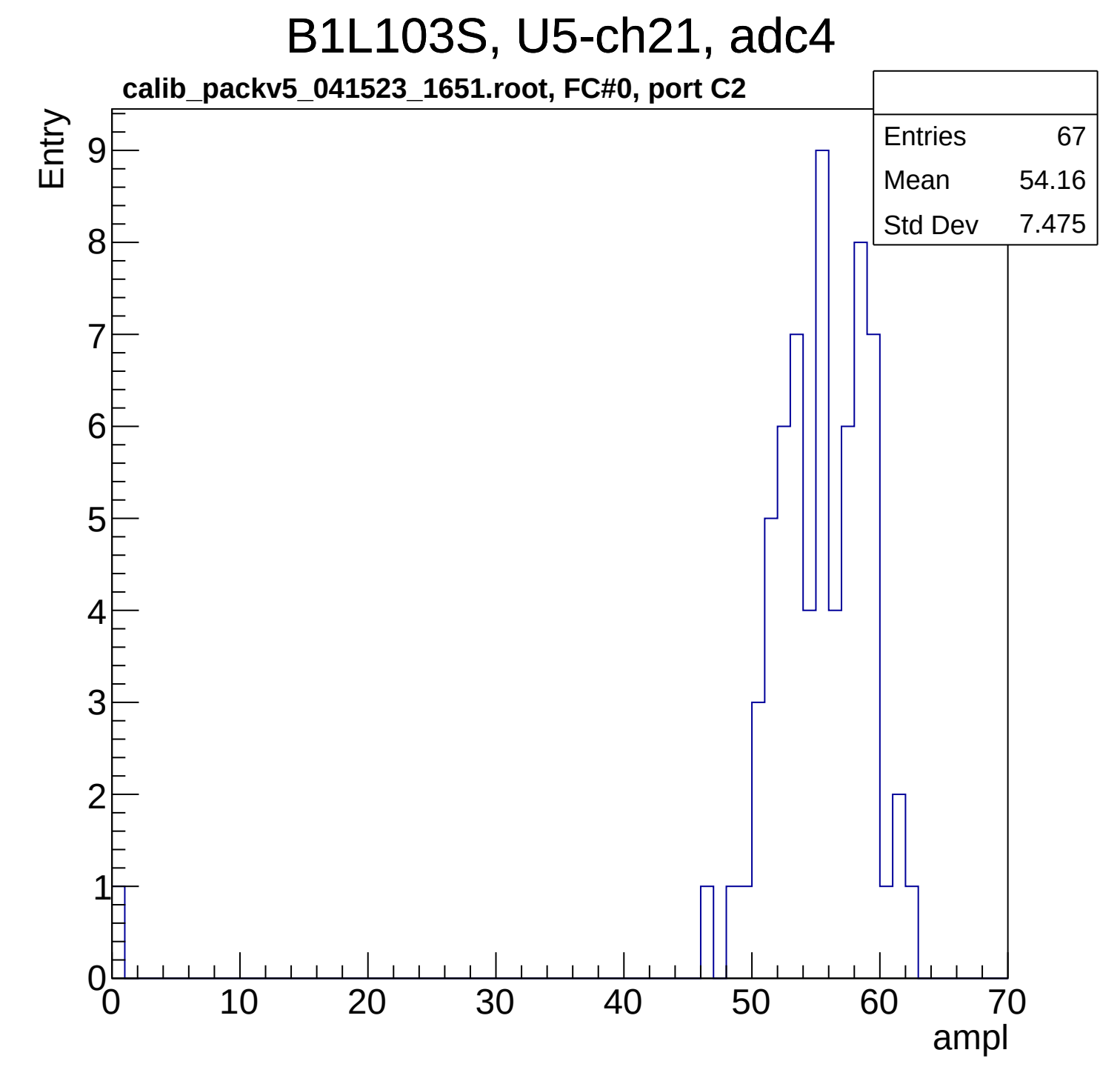
B1L103S, U5-ch21, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 54.16
Std Dev 7.475
Entry
ampl
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6
7
8
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0
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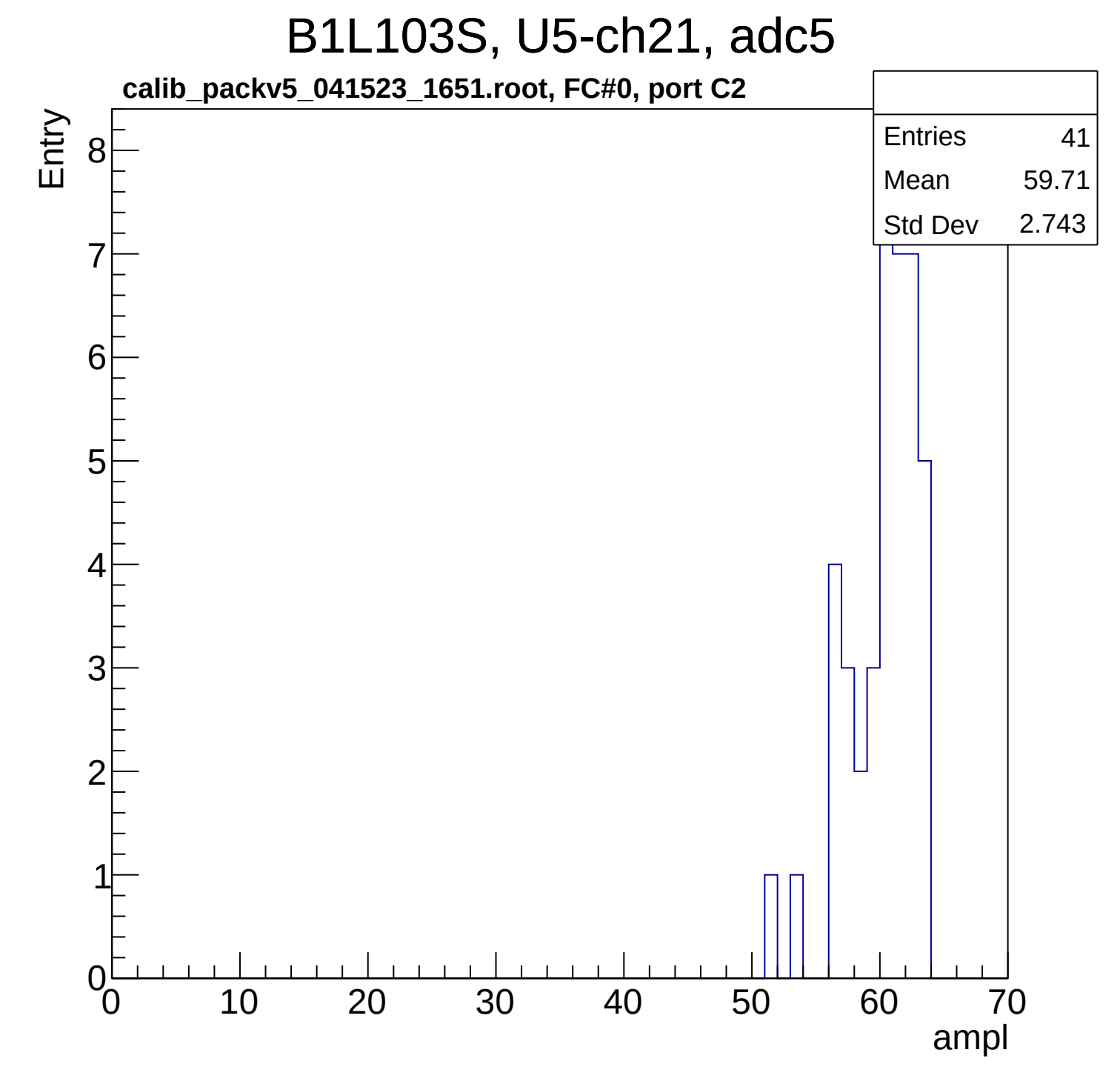
B1L103S, U5-ch21, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 59.71
Std Dev 2.743
Entry
ampl
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5
6
7
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0
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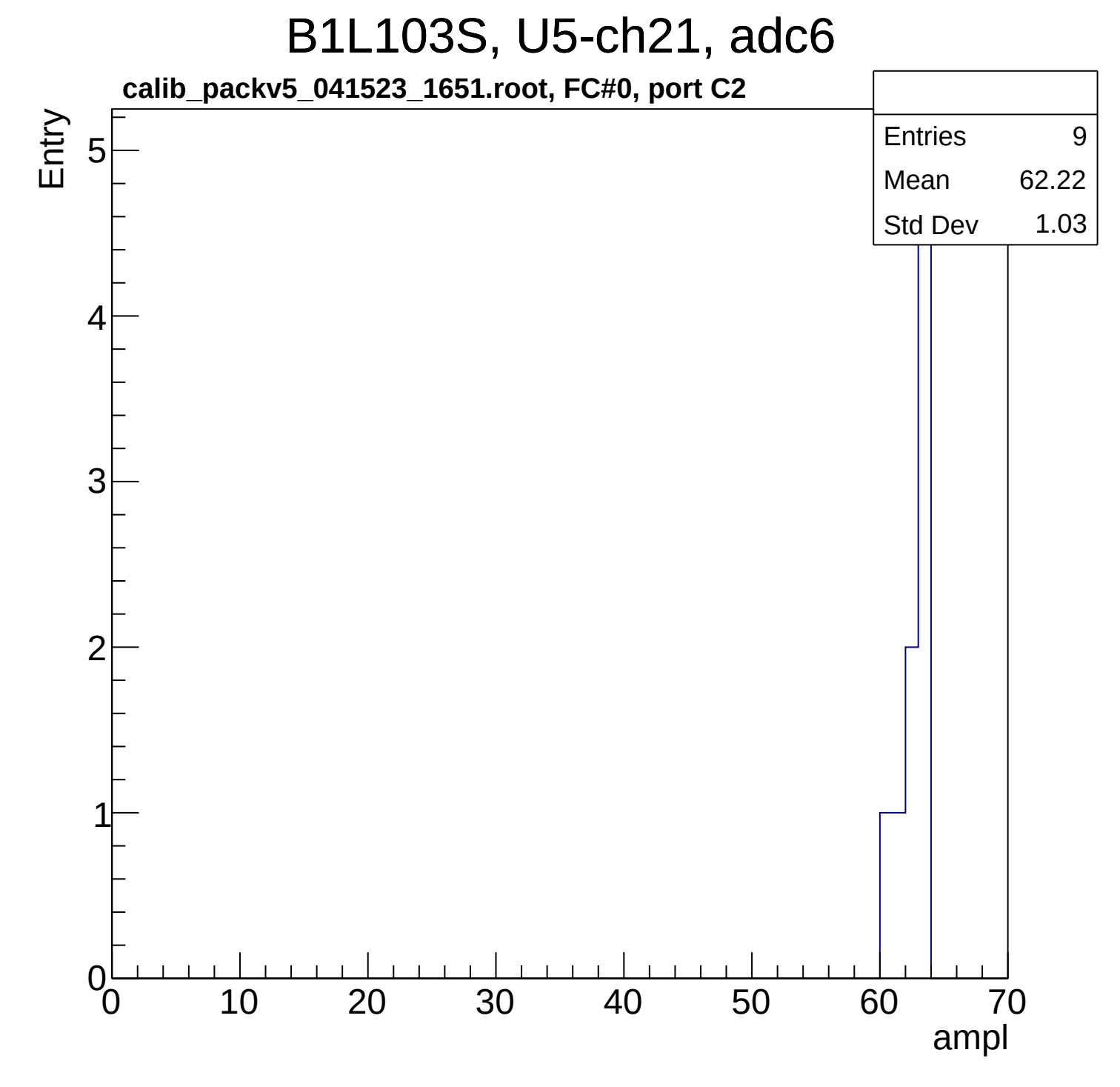
B1L103S, U5-ch21, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 62.22
Std Dev 1.03
Entry
ampl
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0
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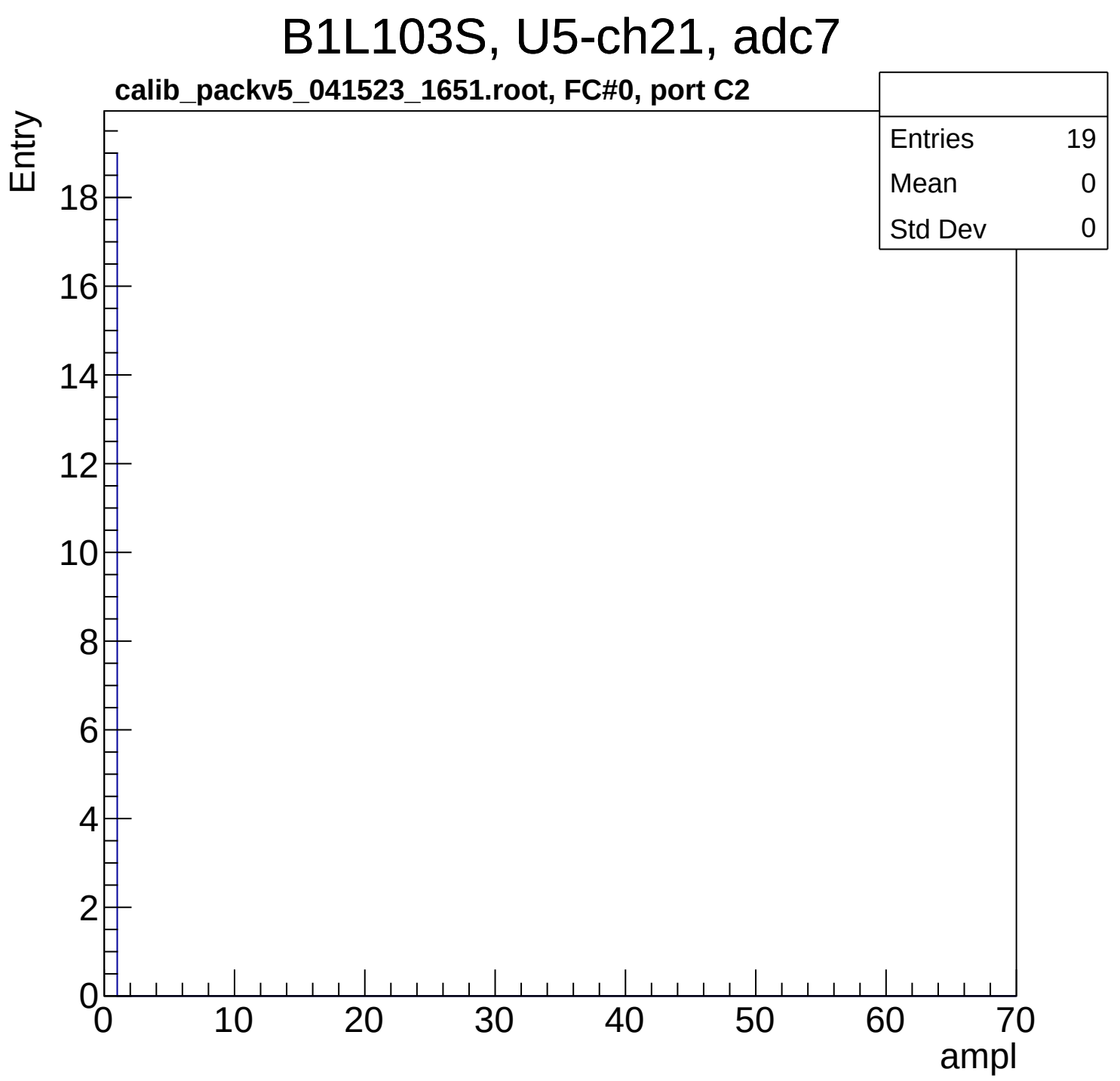
B1L103S, U5-ch21, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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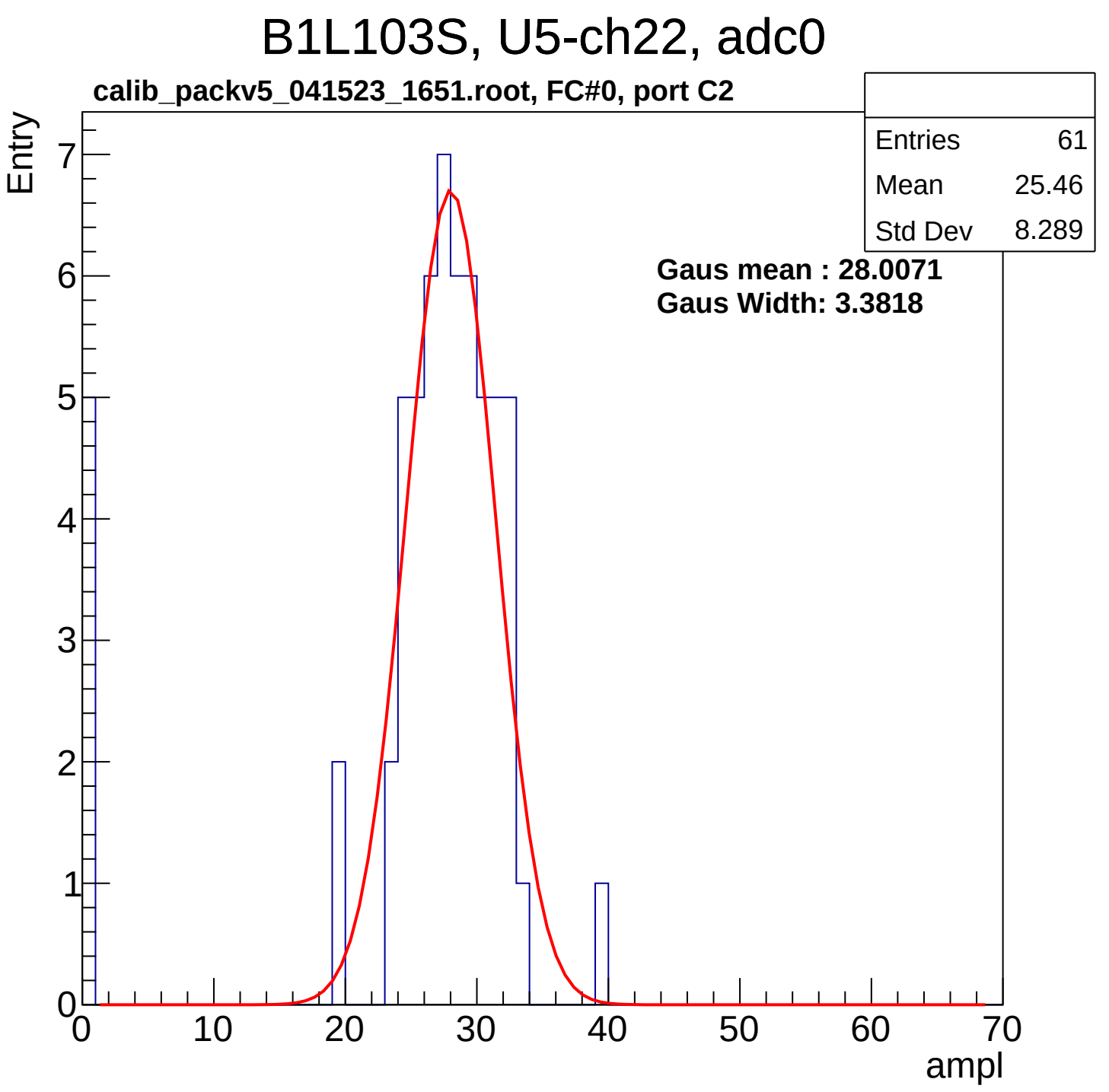
60
70
ampl


B1L103S, U5-ch22, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 25.46
Std Dev 8.289
Gaus mean : 28.0071
Gaus Width: 3.3818
Entry
ampl
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3
4
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0
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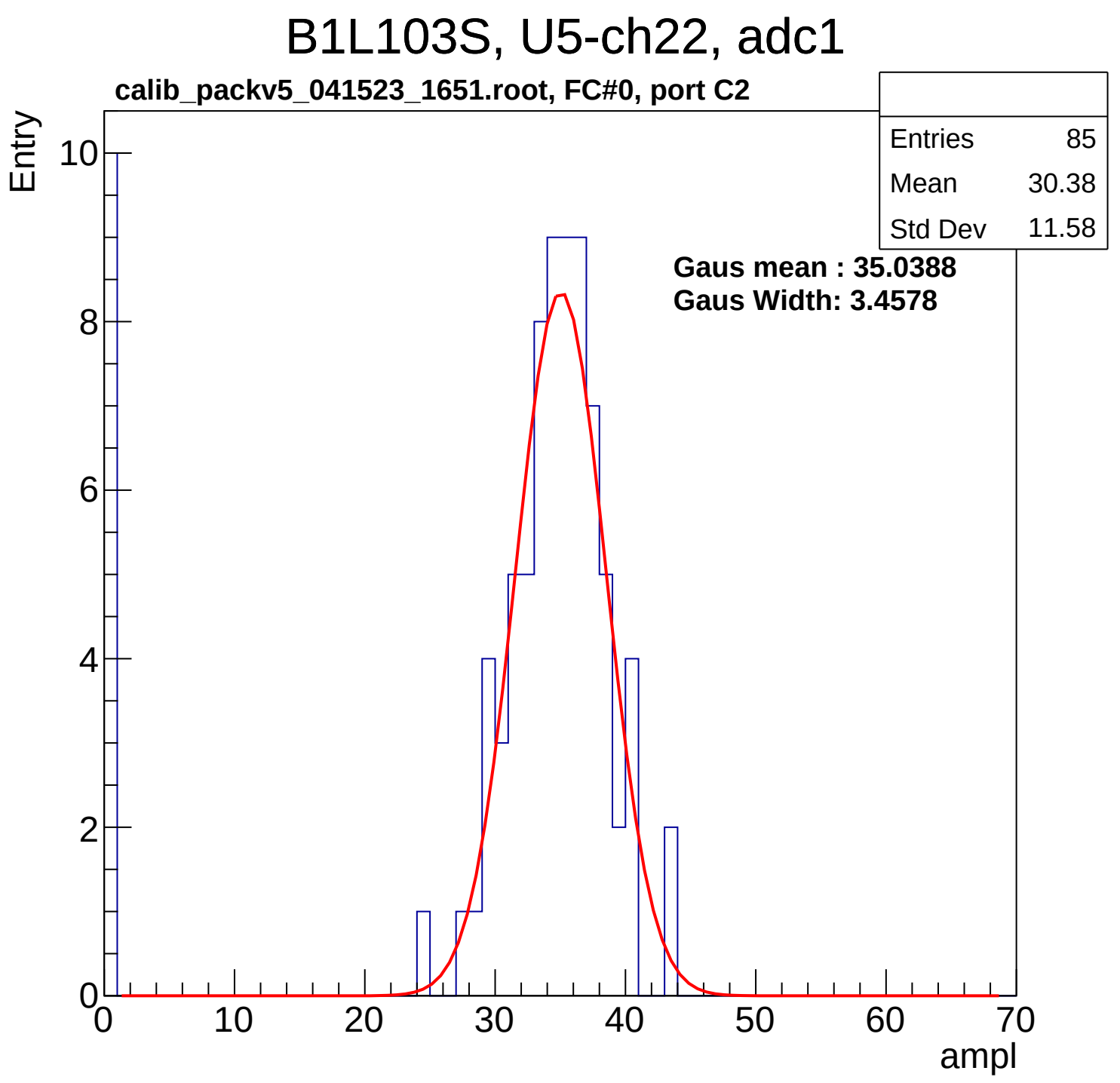
B1L103S, U5-ch22, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 30.38
Std Dev 11.58
Gaus mean : 35.0388
Gaus Width: 3.4578
Entry
ampl
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6
8
10
0
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20
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40
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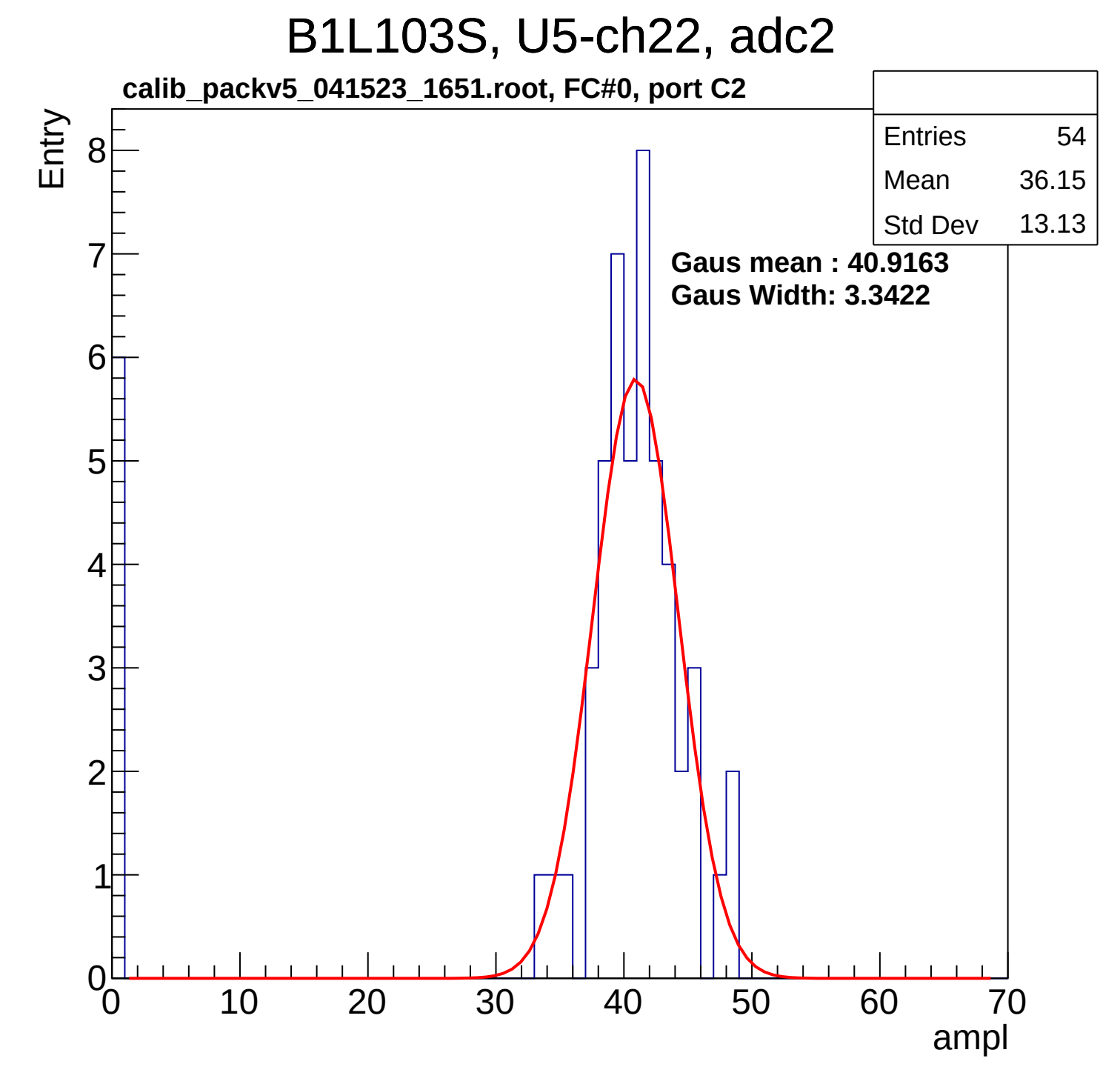
B1L103S, U5-ch22, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 36.15
Std Dev 13.13
Gaus mean : 40.9163
Gaus Width: 3.3422
Entry
ampl
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2
3
4
5
6
7
8
0
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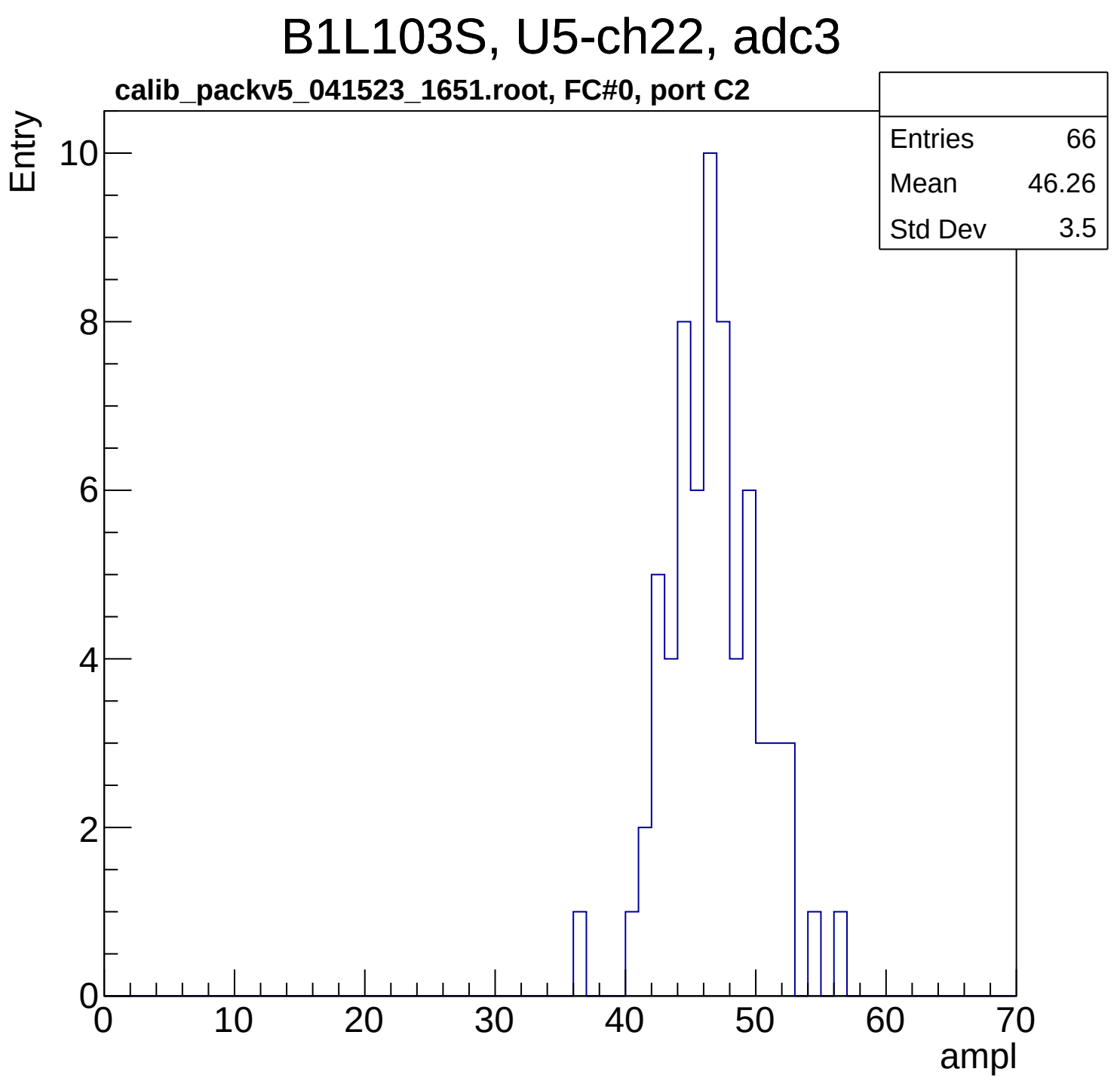
B1L103S, U5-ch22, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 46.26
Std Dev 3.5
Entry
ampl
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0
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40
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60
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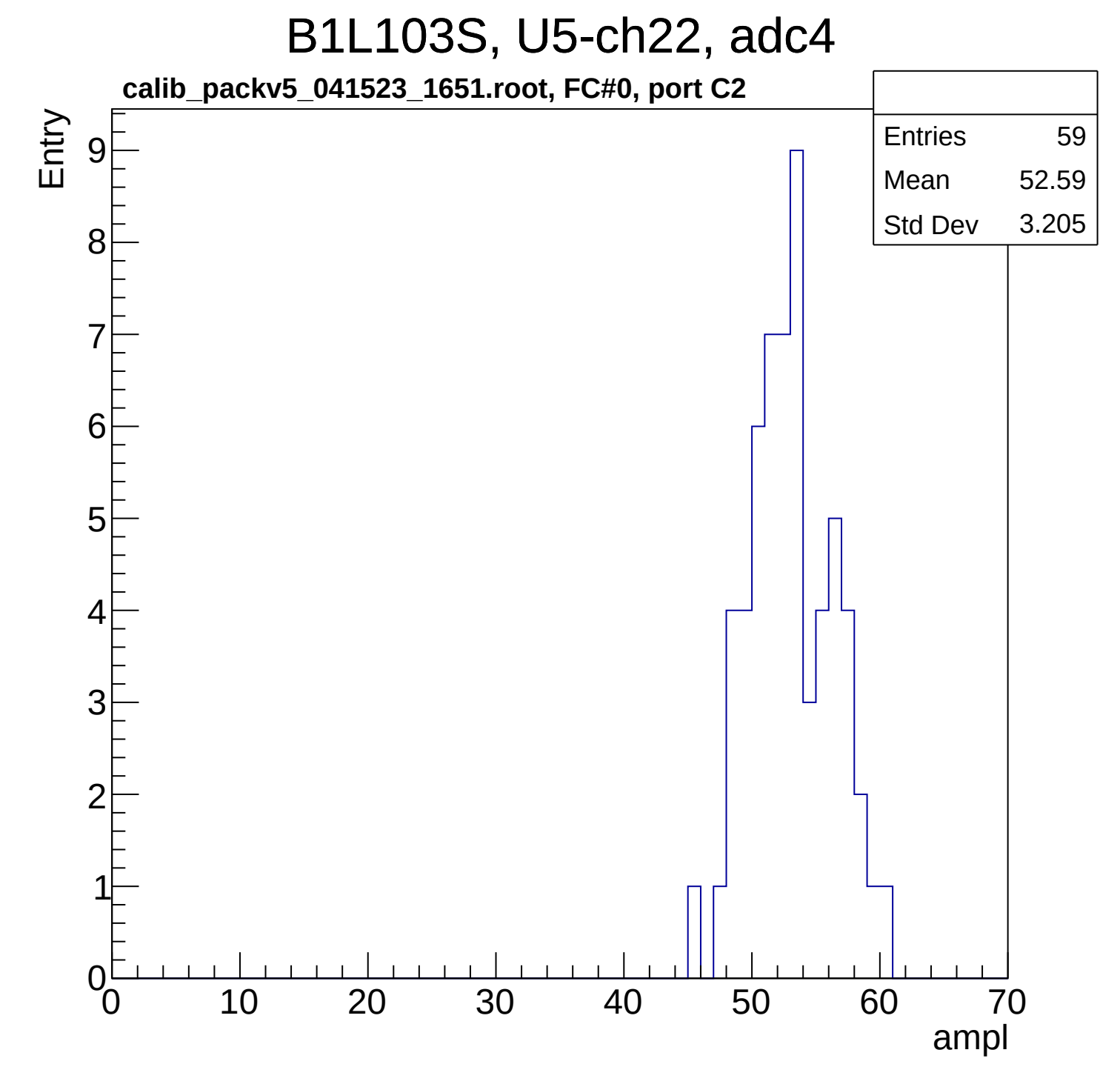
B1L103S, U5-ch22, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 52.59
Std Dev 3.205
Entry
ampl
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2
3
4
5
6
7
8
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0
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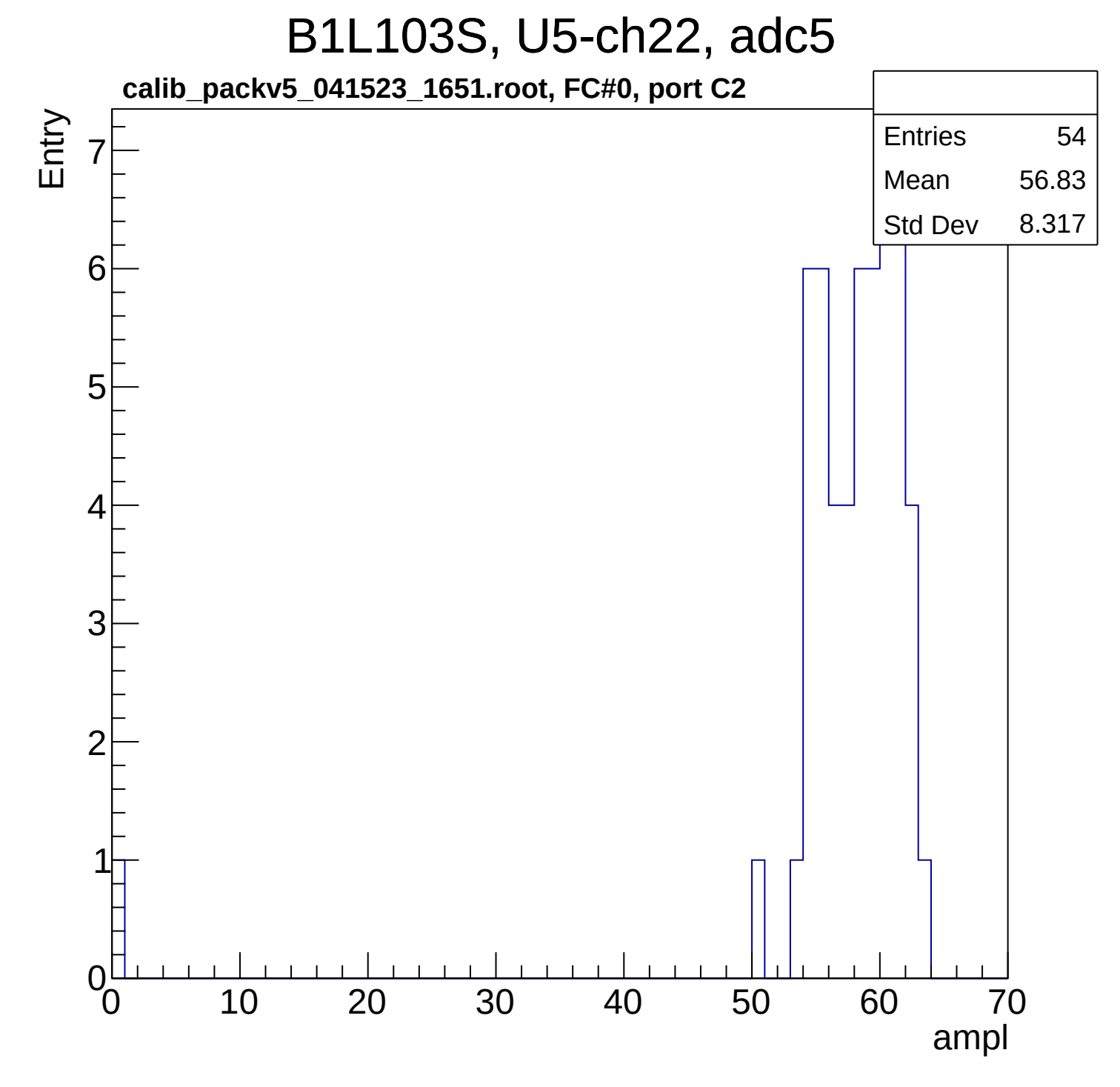
B1L103S, U5-ch22, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 56.83
Std Dev 8.317
Entry
ampl
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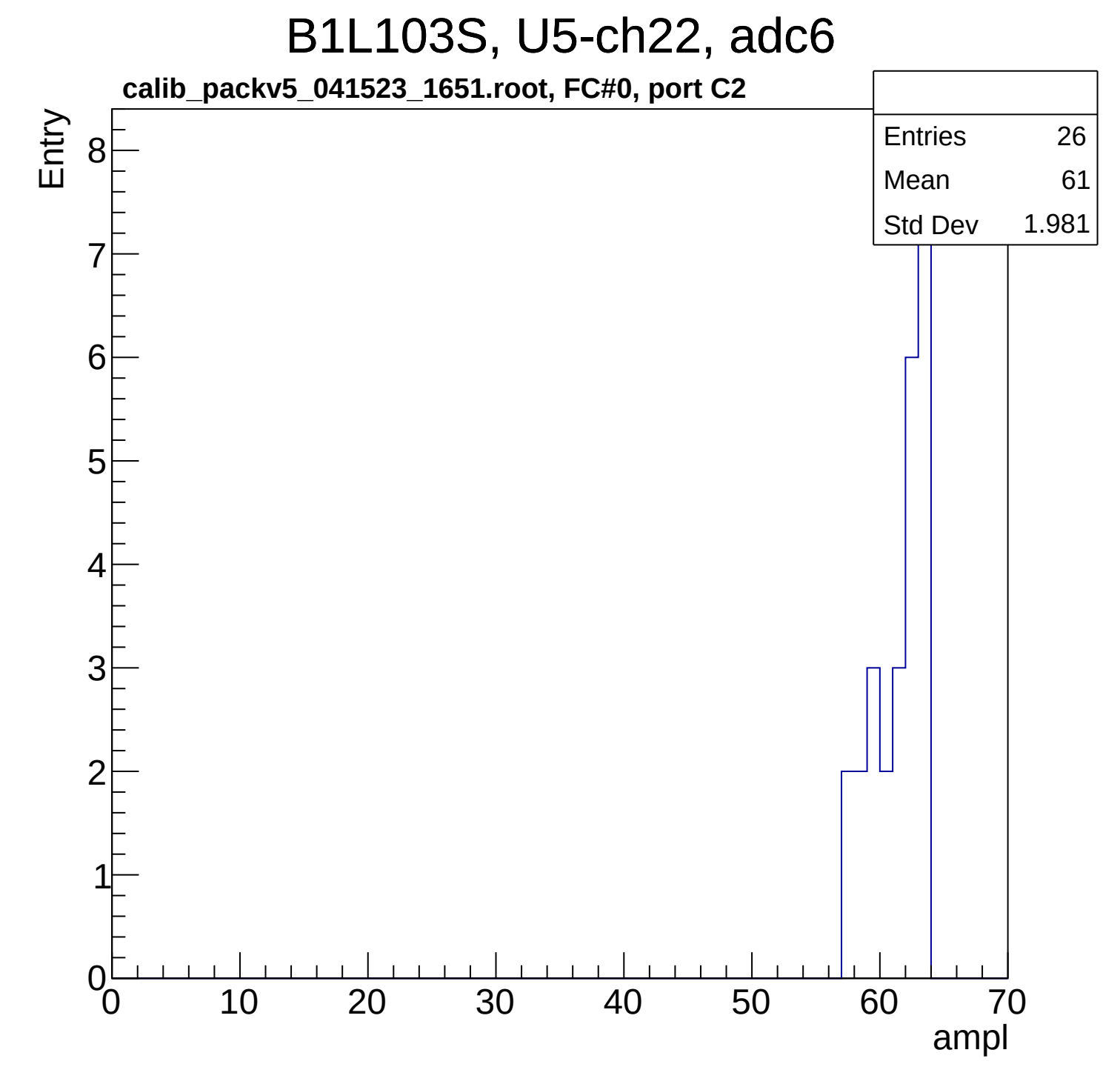
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U5-ch22, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 61
Std Dev 1.981
Entry
ampl
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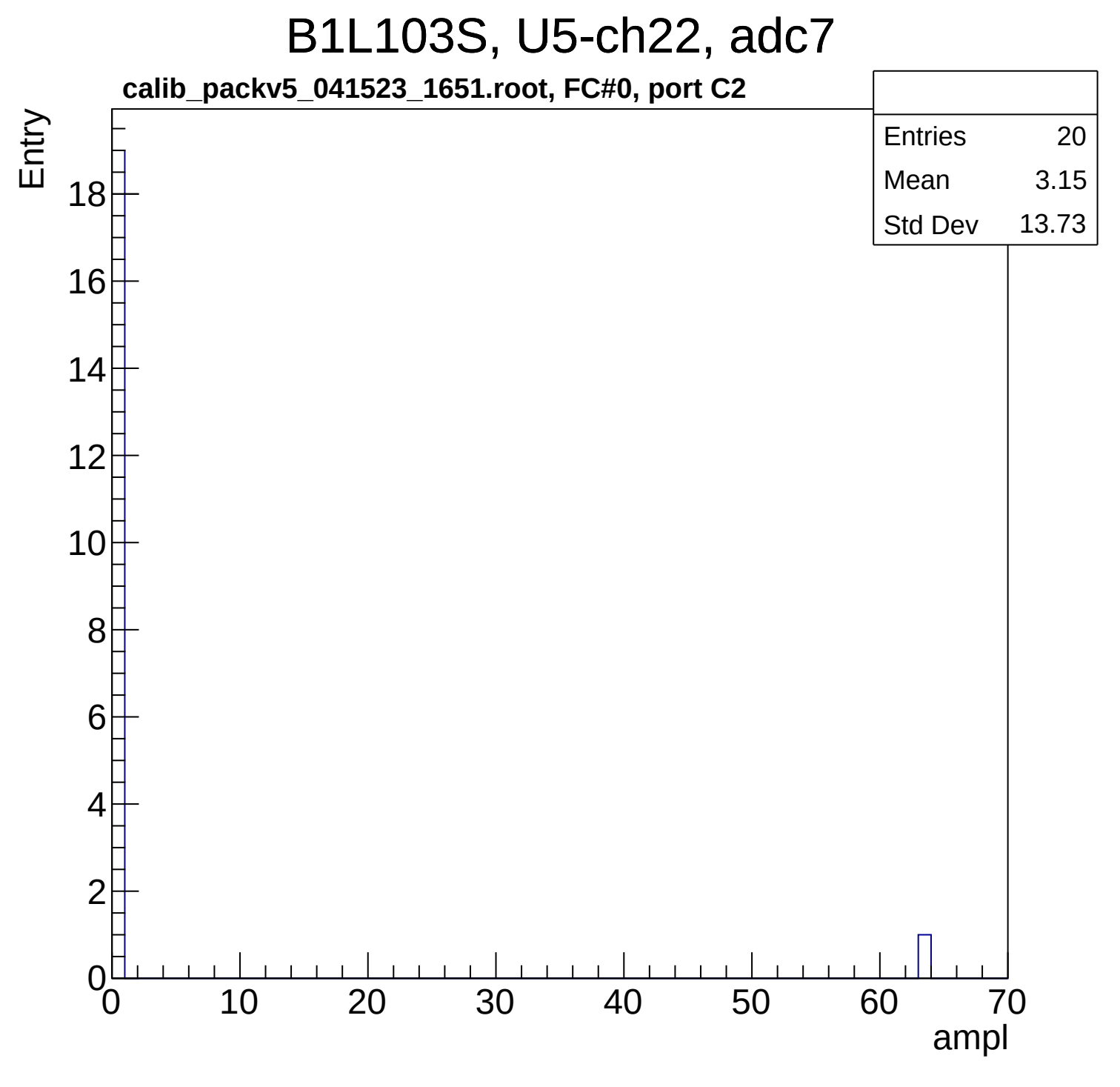
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U5-ch22, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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8
10
12
14
16
18
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10
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30
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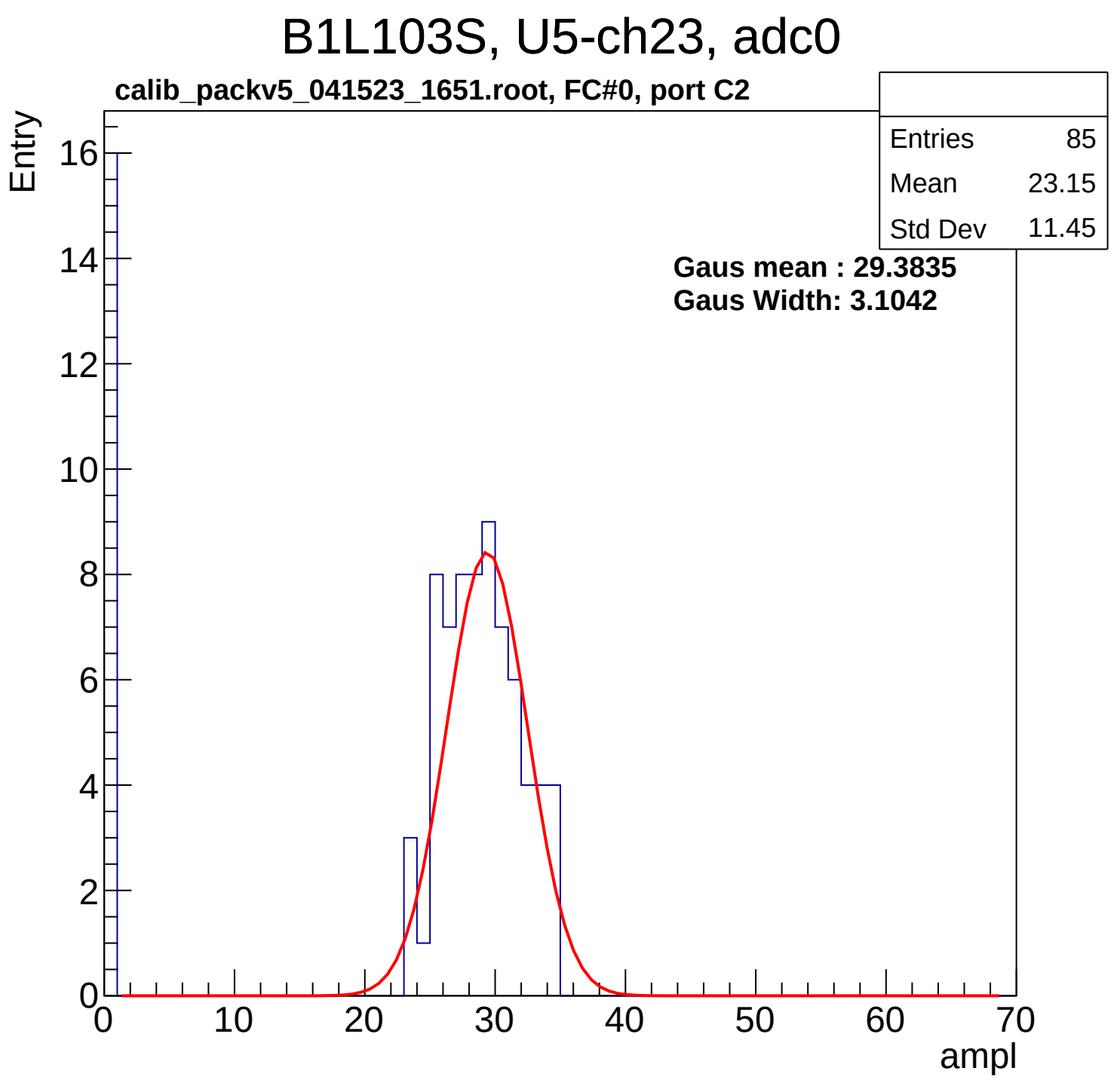
50
60
70
ampl


B1L103S, U5-ch23, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 23.15
Std Dev 11.45
Gaus mean : 29.3835
Gaus Width: 3.1042
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
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40
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60
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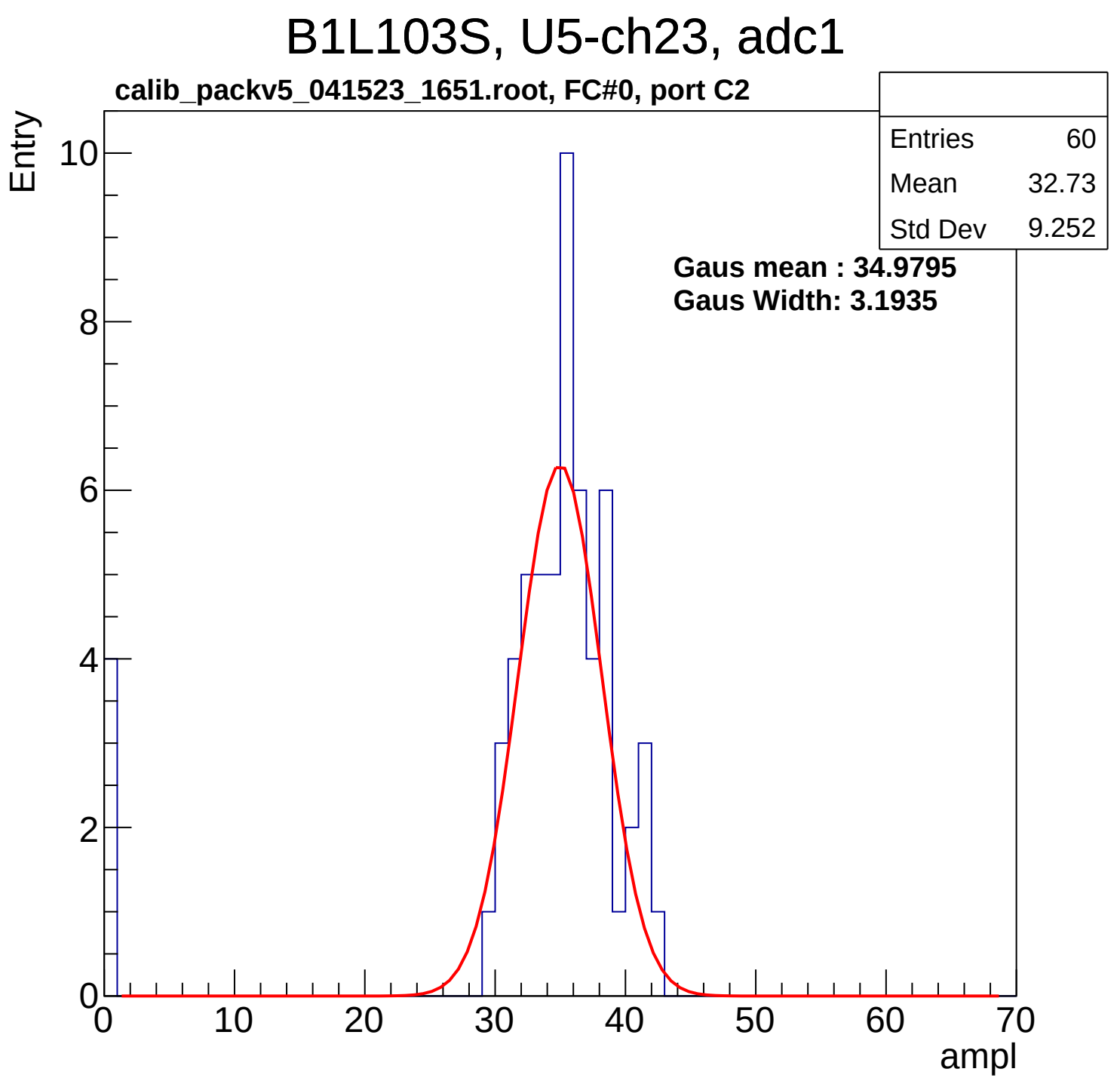
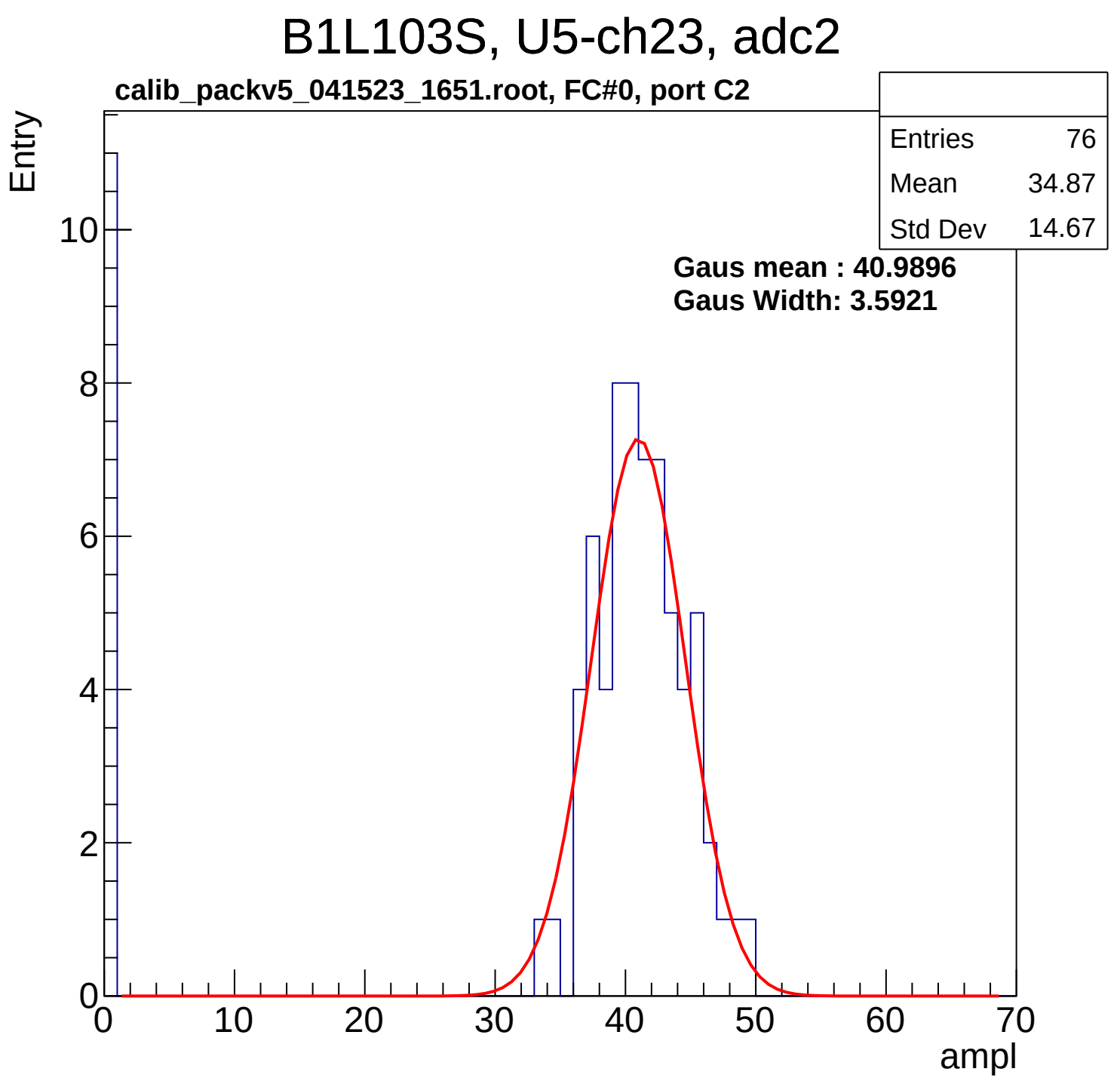

B1L103S, U5-ch23, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 32.73
Std Dev 9.252
Gaus mean : 34.9795
Gaus Width: 3.1935
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U5-ch23, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 34.87
Std Dev 14.67
Gaus mean : 40.9896
Gaus Width: 3.5921
Entry
ampl
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2
4
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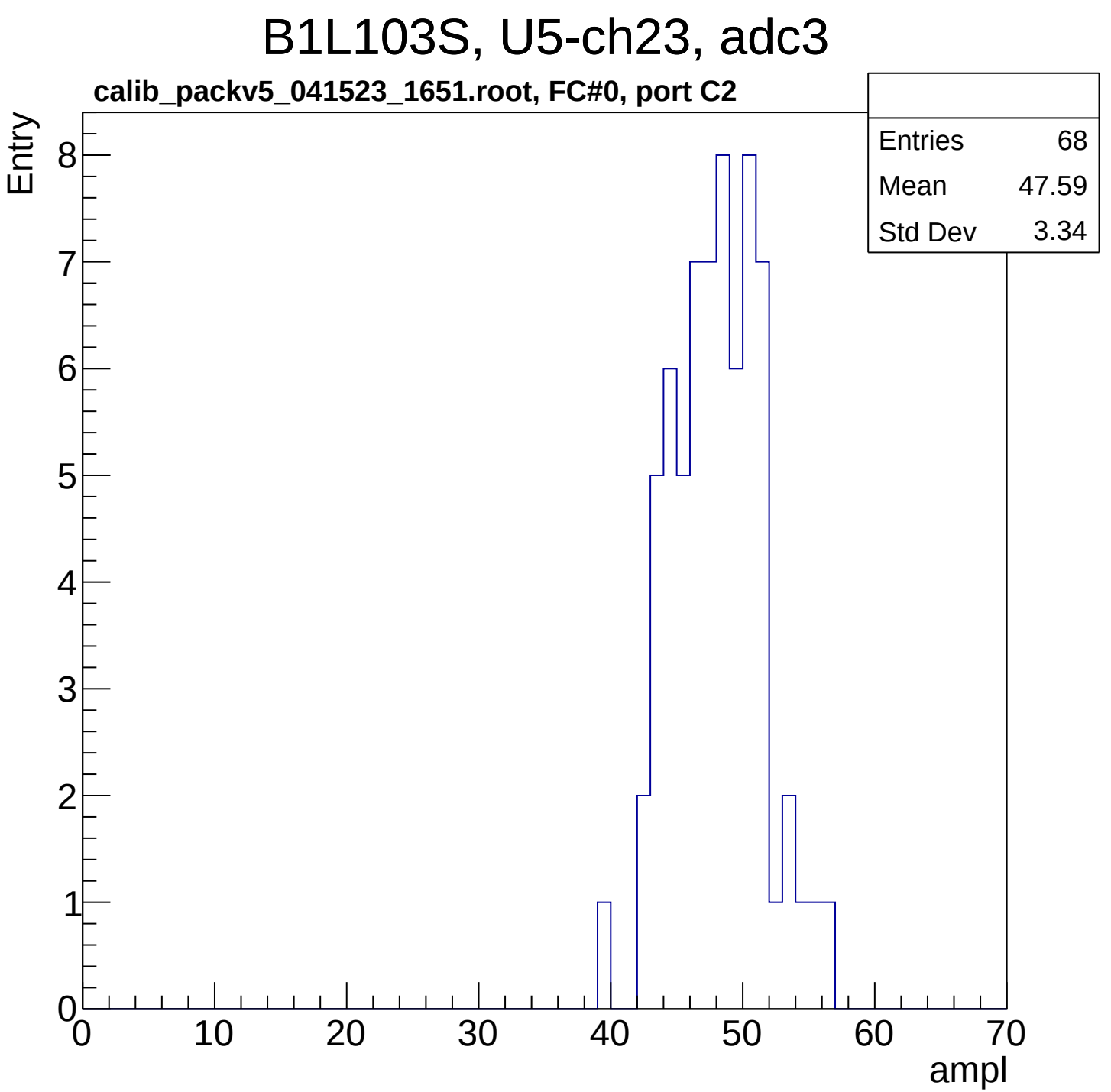
B1L103S, U5-ch23, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 47.59
Std Dev 3.34
Entry
ampl
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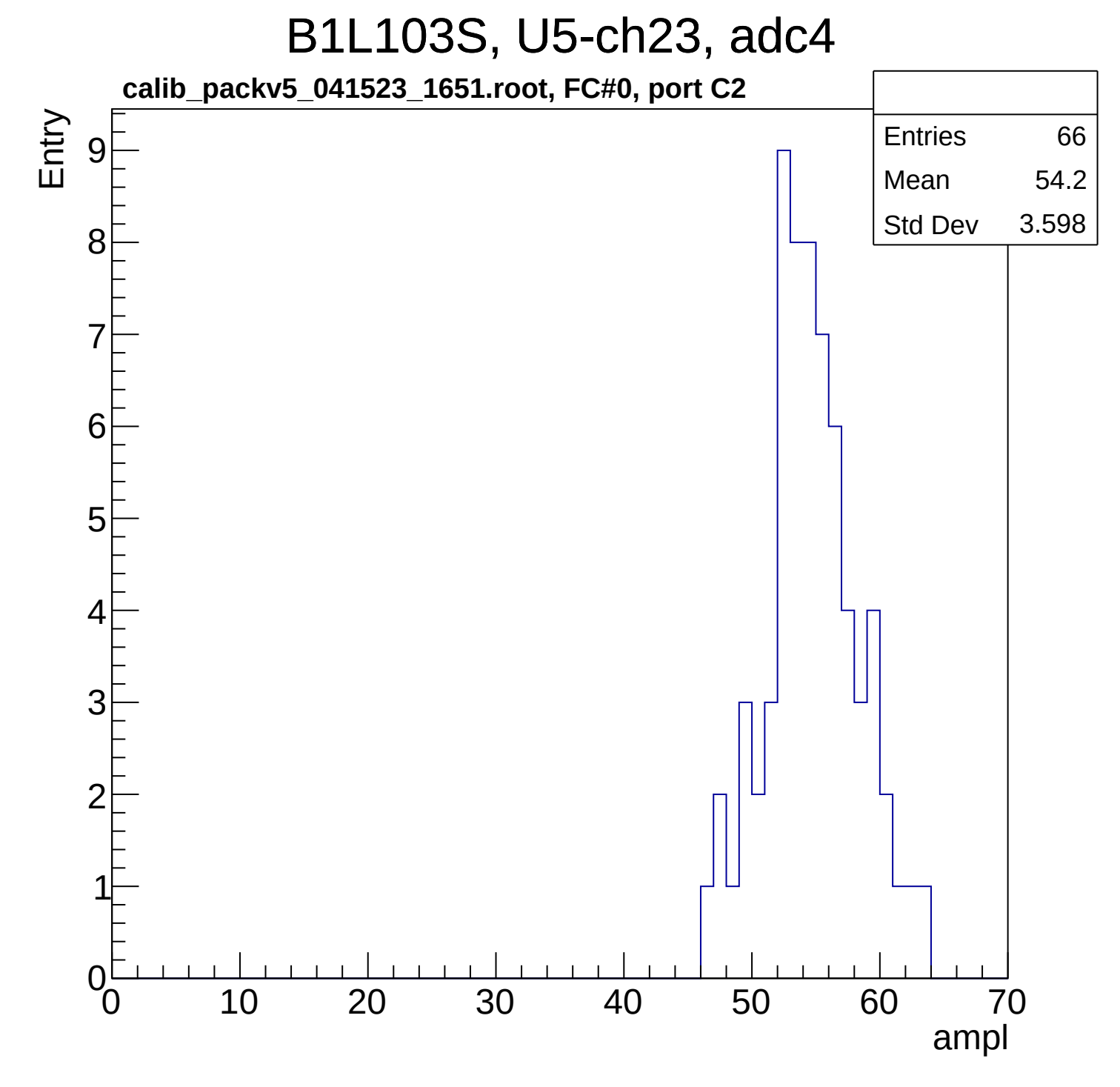
B1L103S, U5-ch23, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 54.2
Std Dev 3.598
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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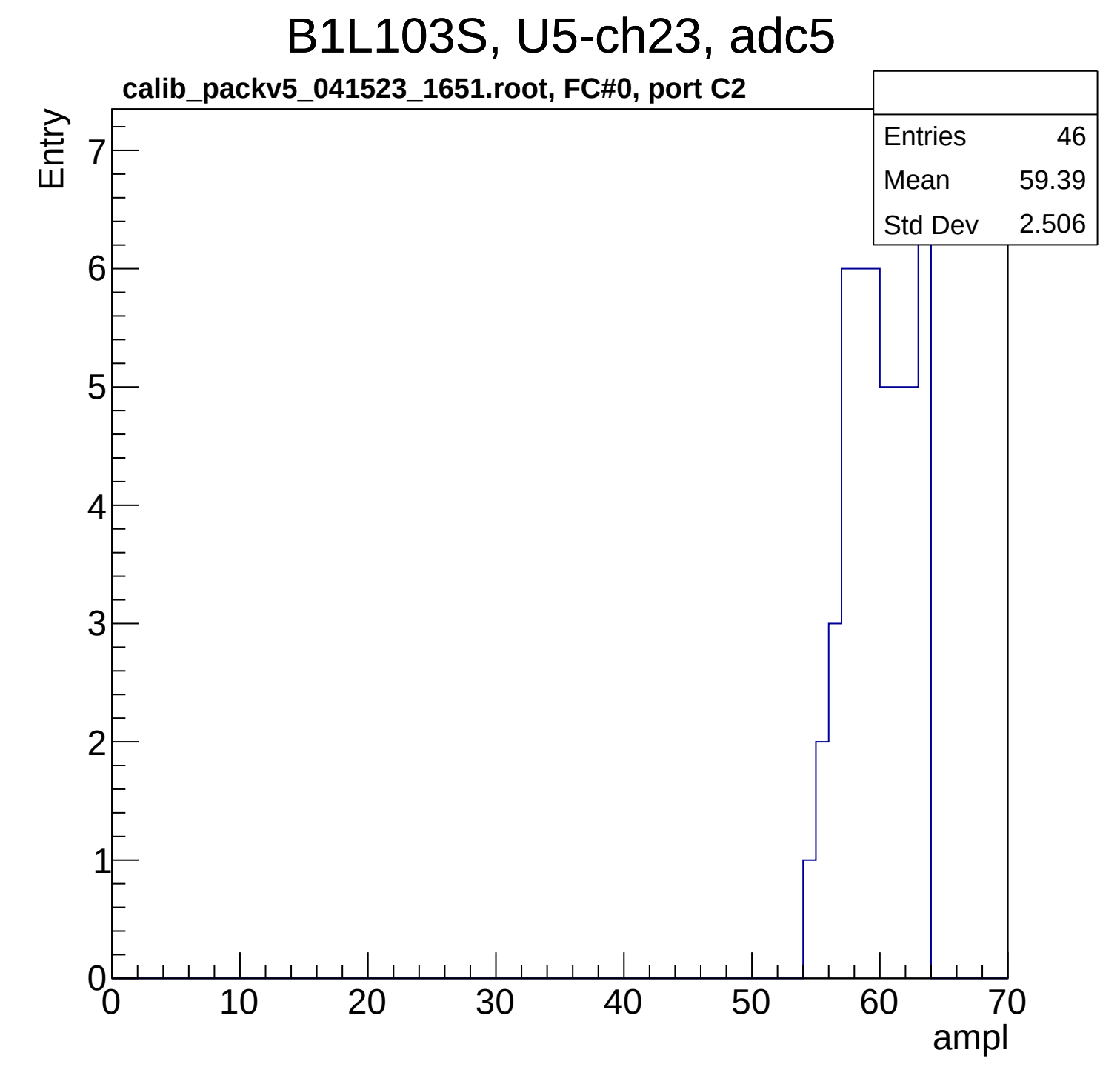
B1L103S, U5-ch23, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 59.39
Std Dev 2.506
Entry
ampl
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2
3
4
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0
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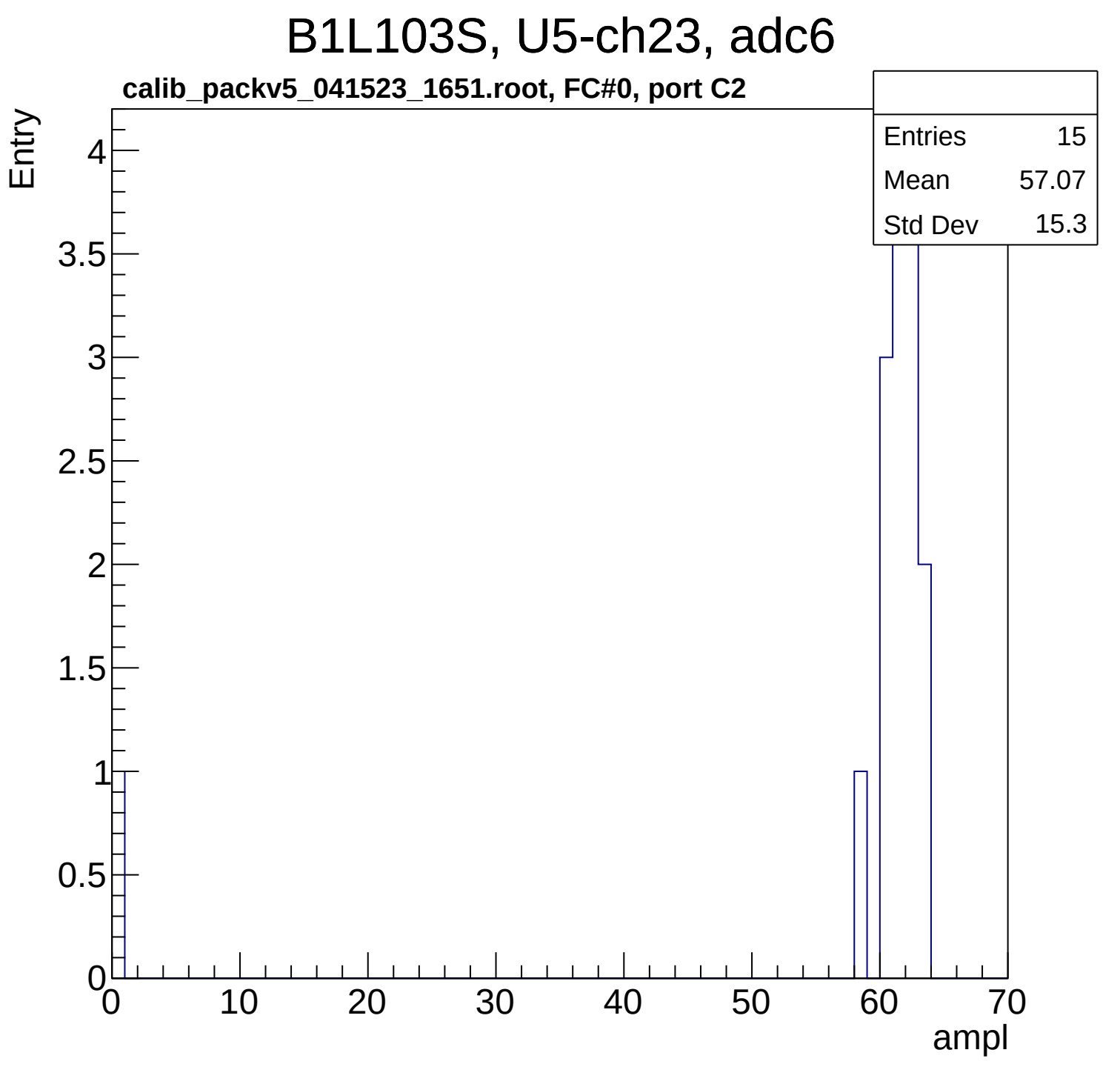
B1L103S, U5-ch23, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.07
Std Dev 15.3
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
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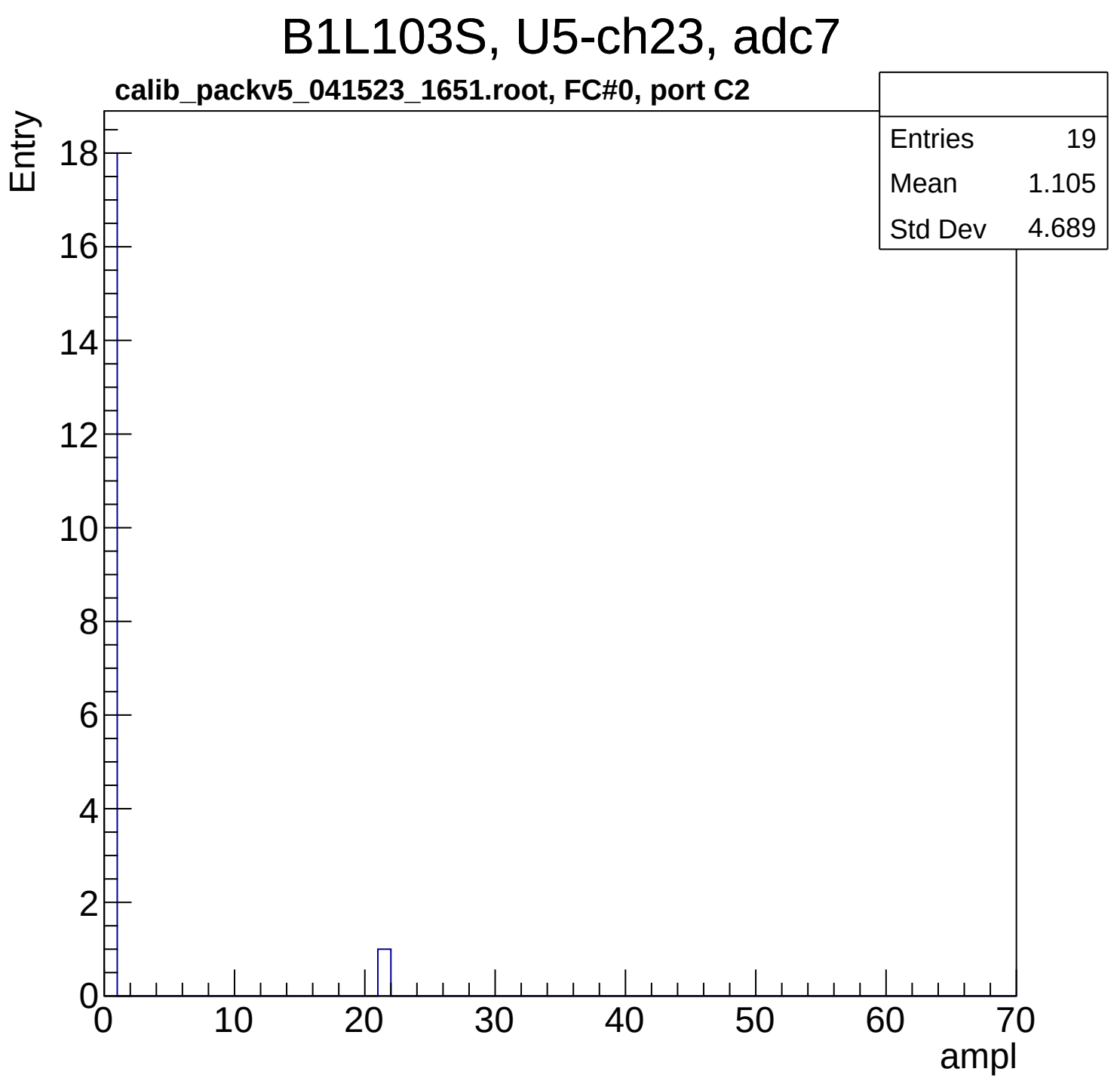
B1L103S, U5-ch23, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
0
2
4
6
8
10
12
14
16
18
0
10
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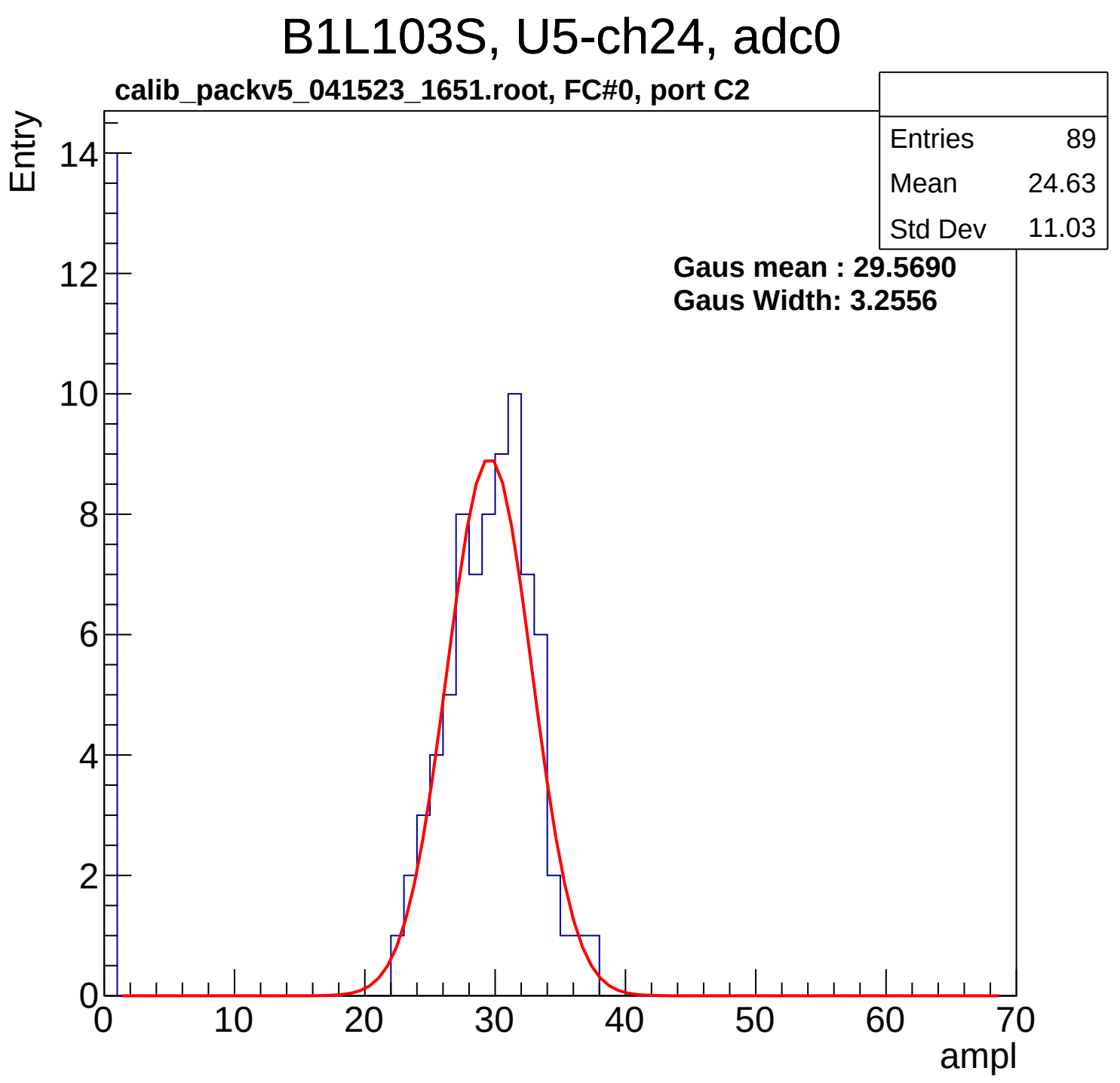
60
70
ampl


B1L103S, U5-ch24, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 24.63
Std Dev 11.03
Gaus mean : 29.5690
Gaus Width: 3.2556
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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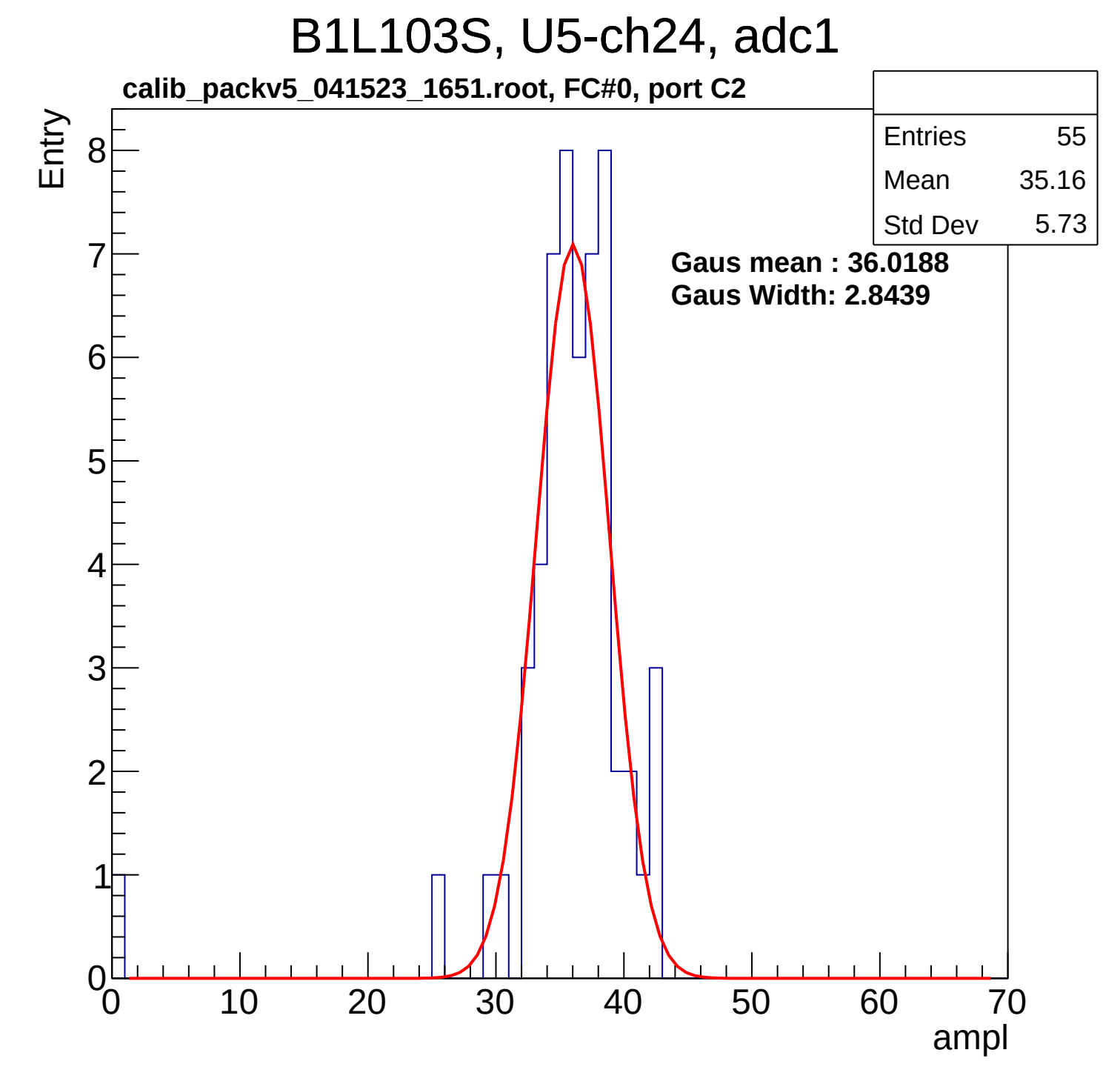
B1L103S, U5-ch24, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 35.16
Std Dev 5.73
Gaus mean : 36.0188
Gaus Width: 2.8439
Entry
ampl
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1
2
3
4
5
6
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8
0
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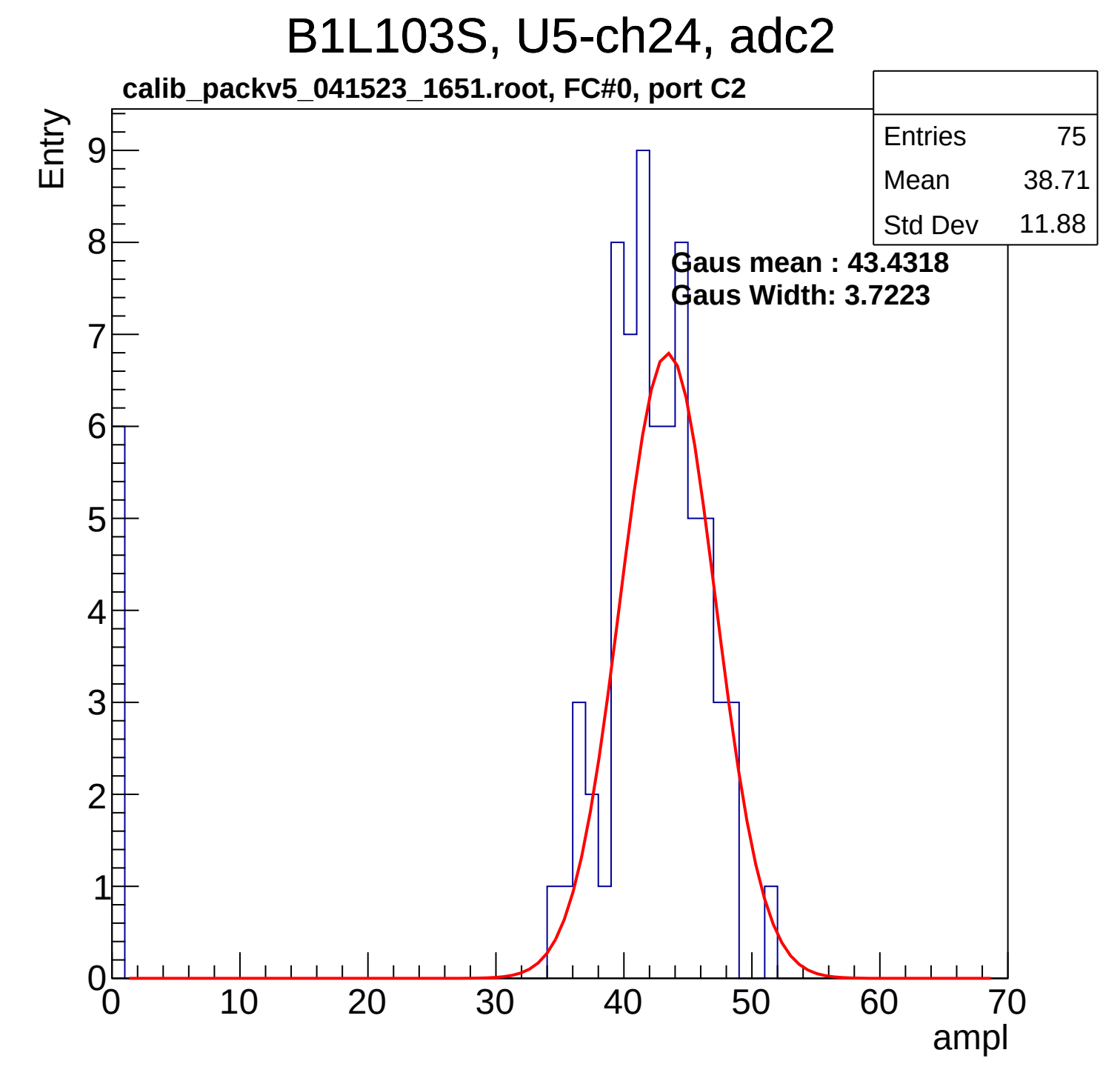
B1L103S, U5-ch24, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 38.71
Std Dev 11.88
Gaus mean : 43.4318
Gaus Width: 3.7223
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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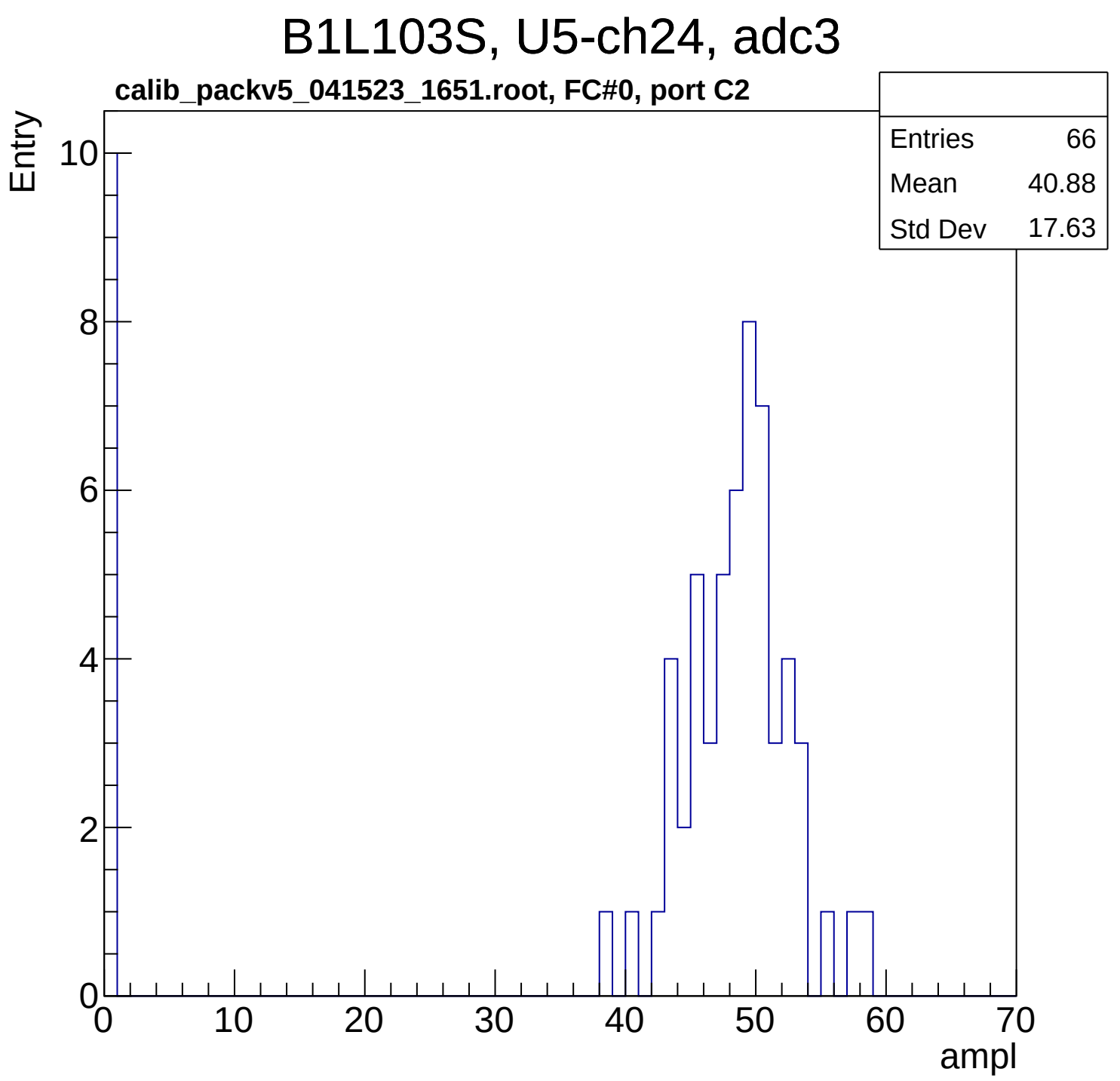
B1L103S, U5-ch24, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 40.88
Std Dev 17.63
Entry
ampl
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4
6
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0
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20
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40
50
60
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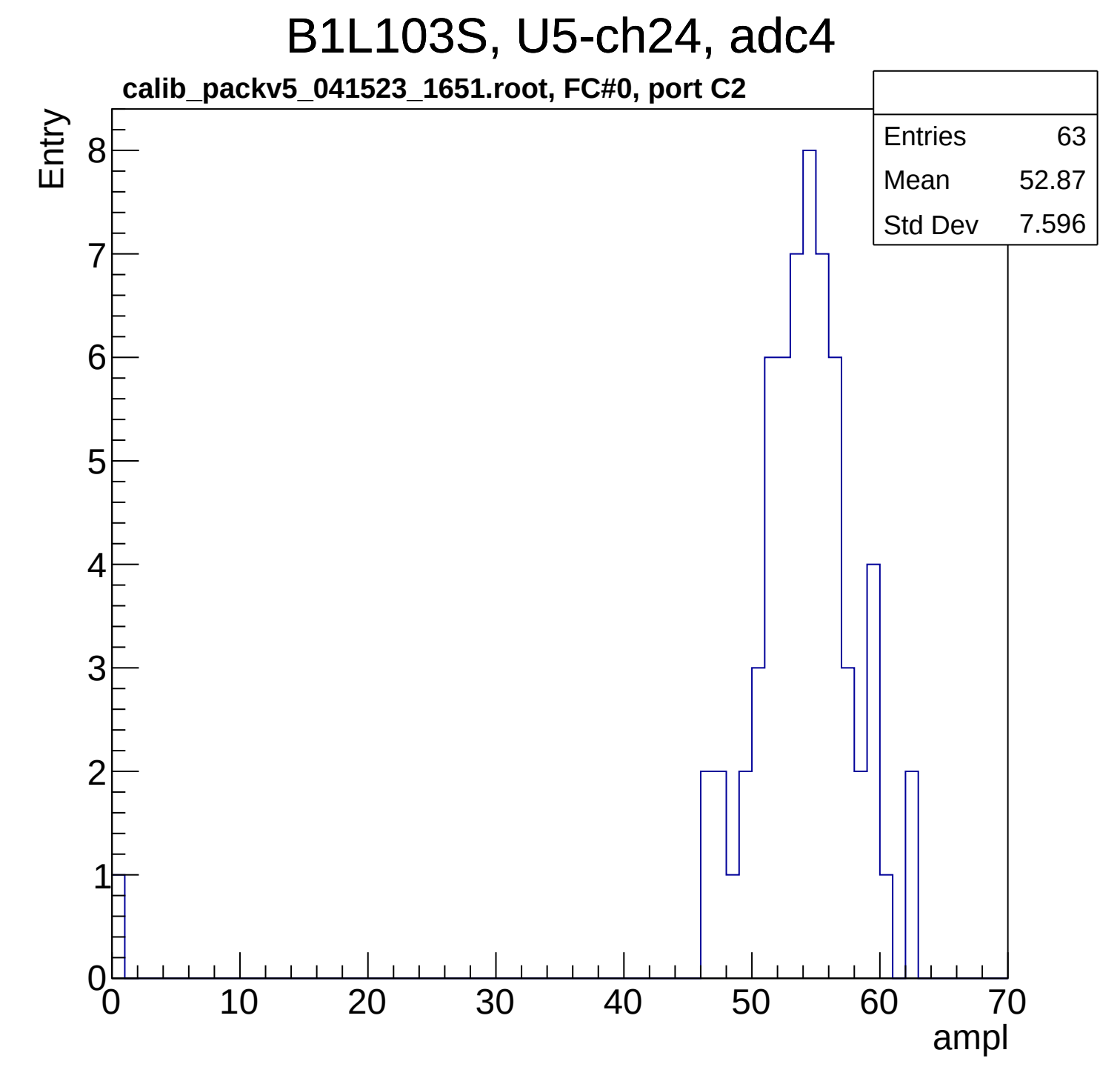
B1L103S, U5-ch24, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 52.87
Std Dev 7.596
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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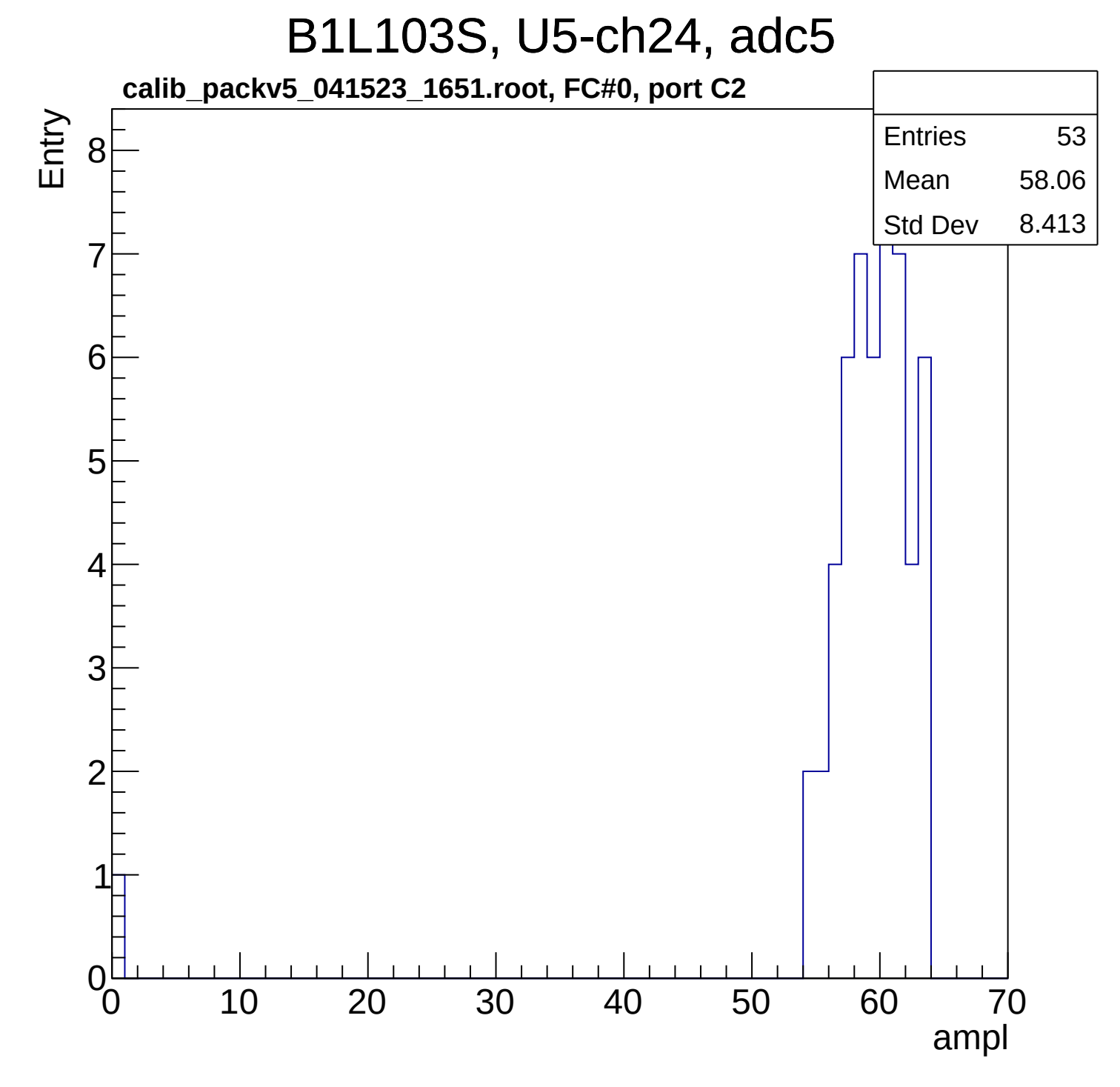
B1L103S, U5-ch24, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.06
Std Dev 8.413
Entry
ampl
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2
3
4
5
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0
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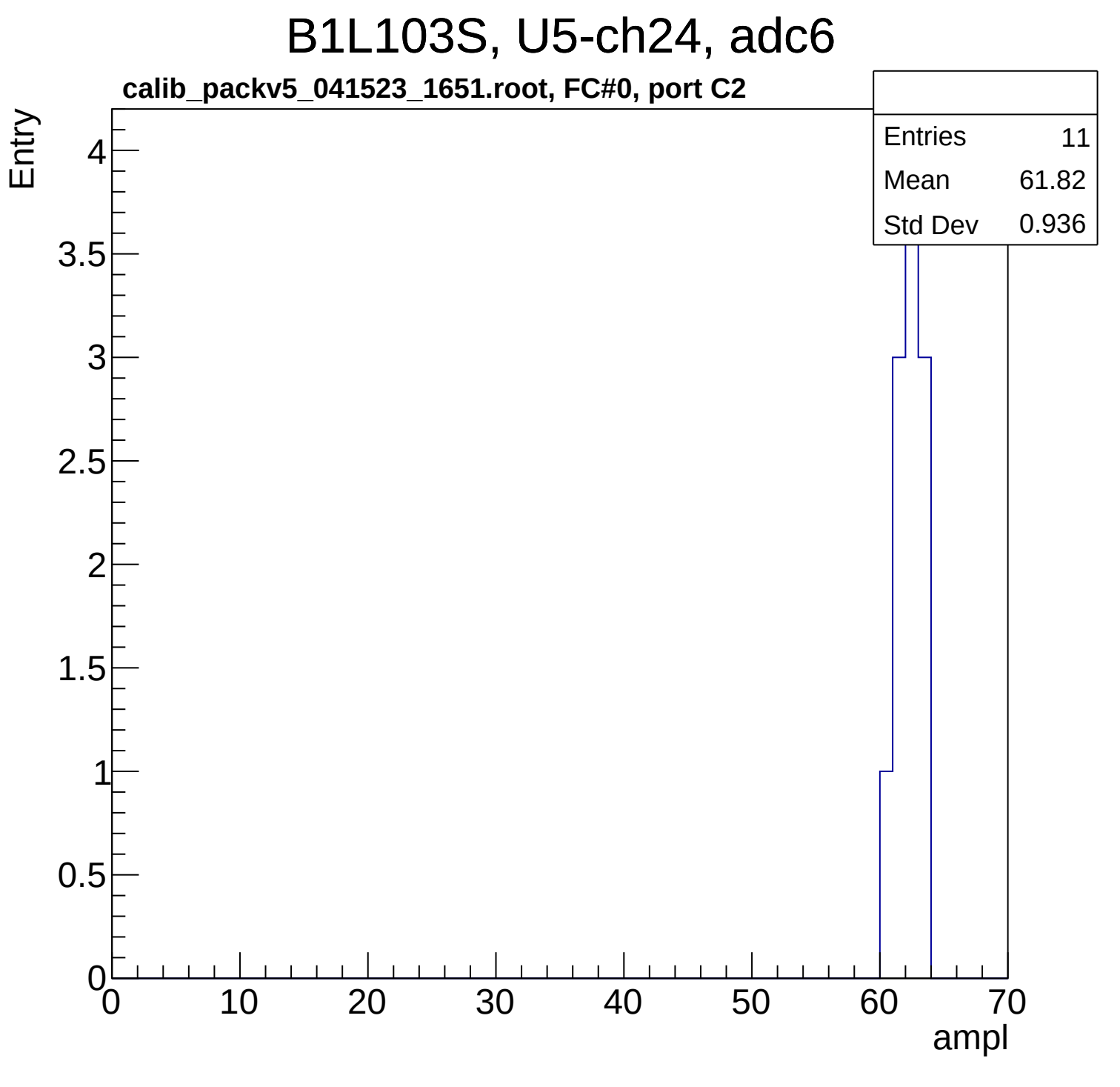
B1L103S, U5-ch24, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.82
Std Dev 0.936
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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20
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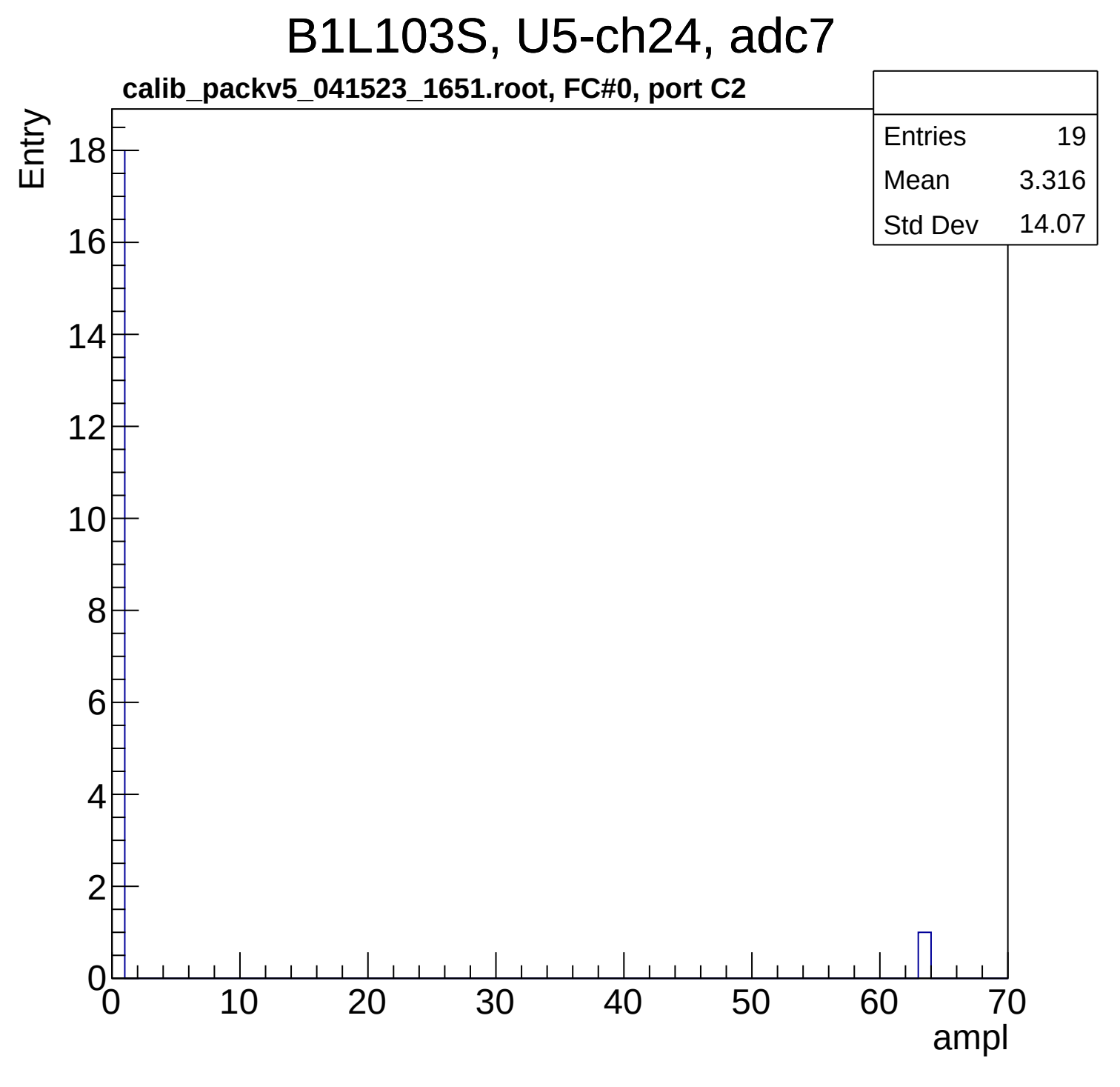
40
50
60
70


B1L103S, U5-ch24, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
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6
8
10
12
14
16
18
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50
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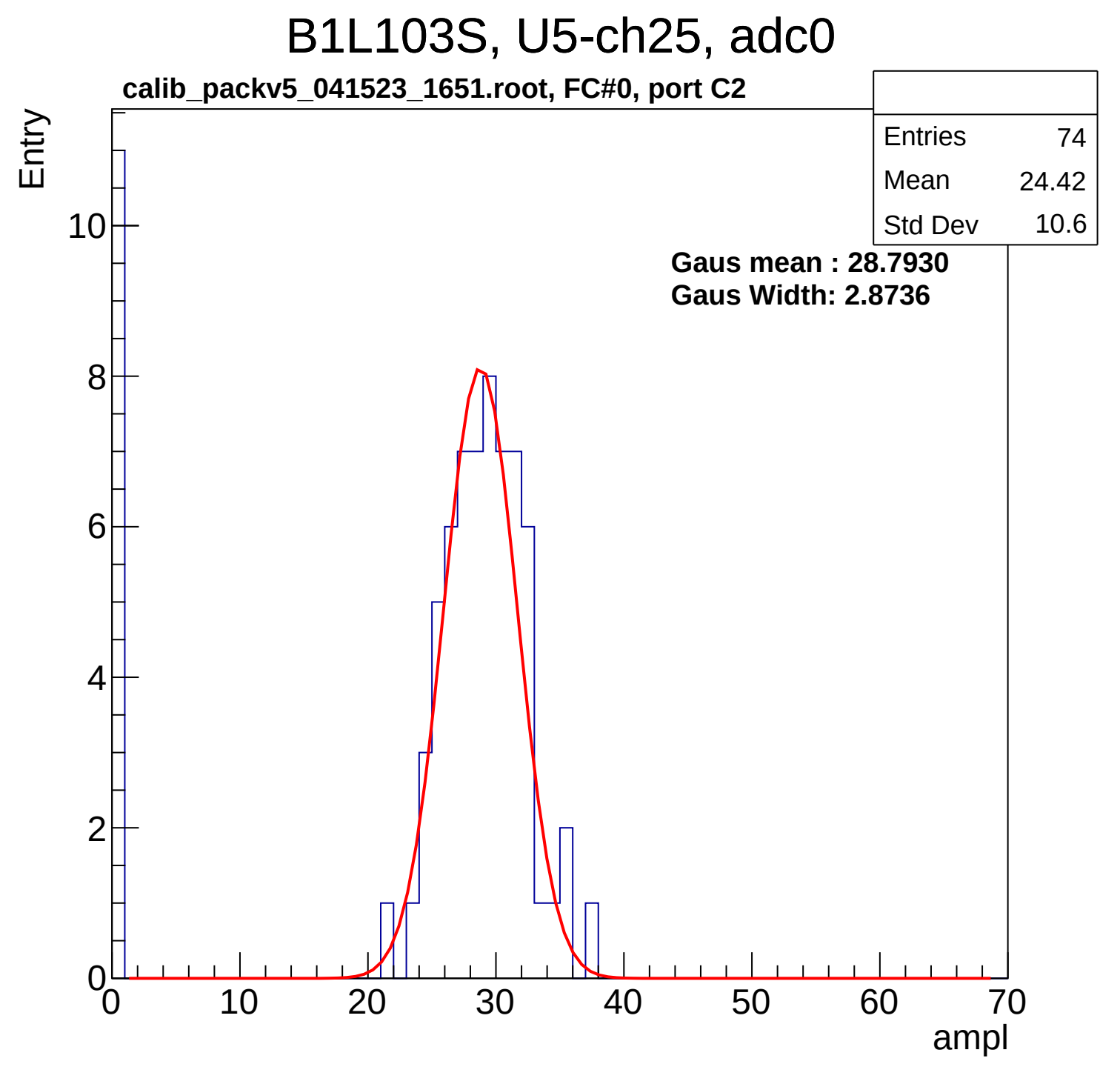
70
ampl


B1L103S, U5-ch25, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 24.42
Std Dev 10.6
Gaus mean : 28.7930
Gaus Width: 2.8736
Entry
ampl
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4
6
8
10
0
10
20
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40
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60
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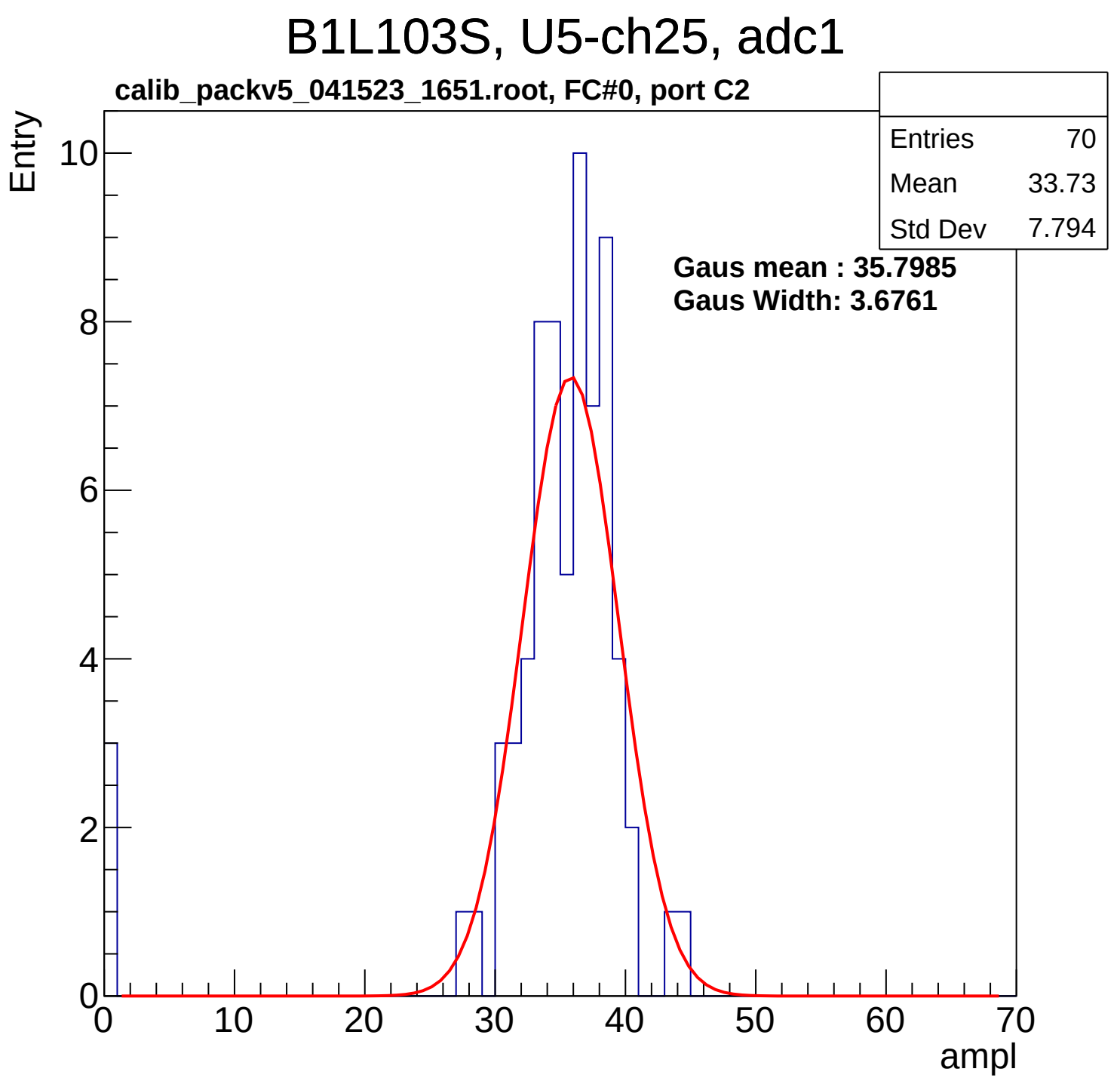
B1L103S, U5-ch25, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 33.73
Std Dev 7.794
Gaus mean : 35.7985
Gaus Width: 3.6761
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
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60
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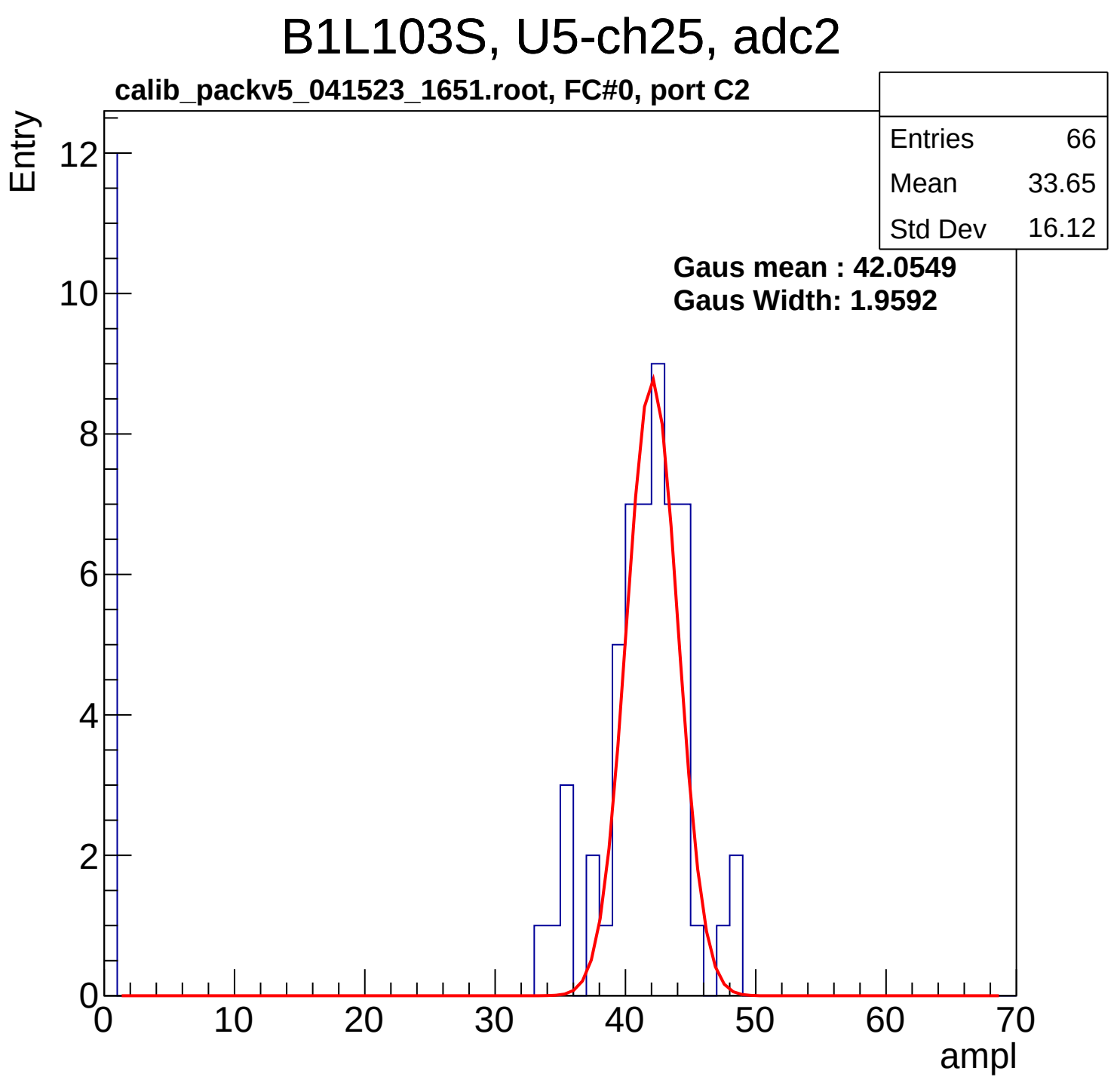
B1L103S, U5-ch25, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 33.65
Std Dev 16.12
Gaus mean : 42.0549
Gaus Width: 1.9592
Entry
ampl
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6
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10
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0
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60
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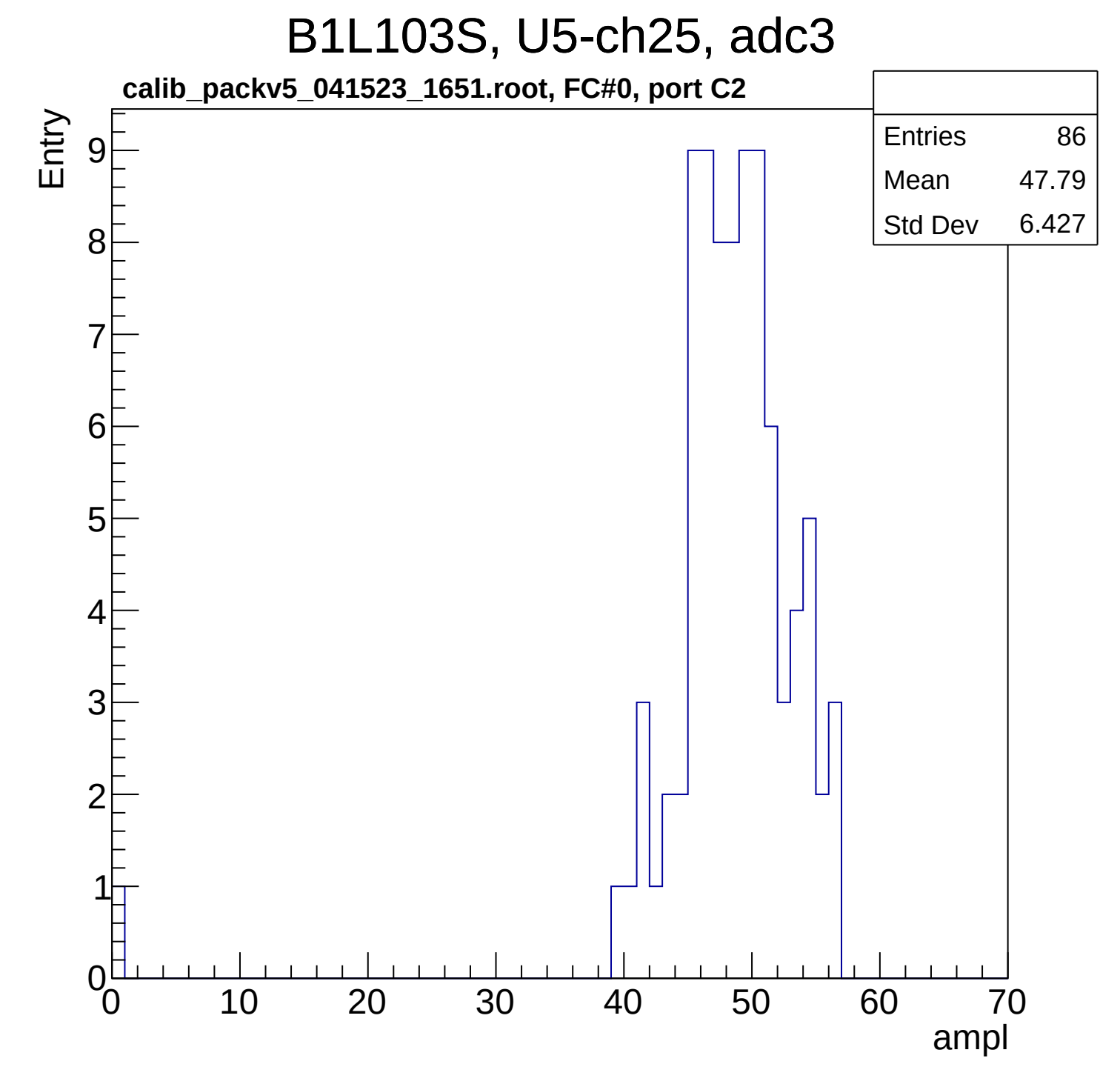
B1L103S, U5-ch25, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 47.79
Std Dev 6.427
Entry
ampl
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6
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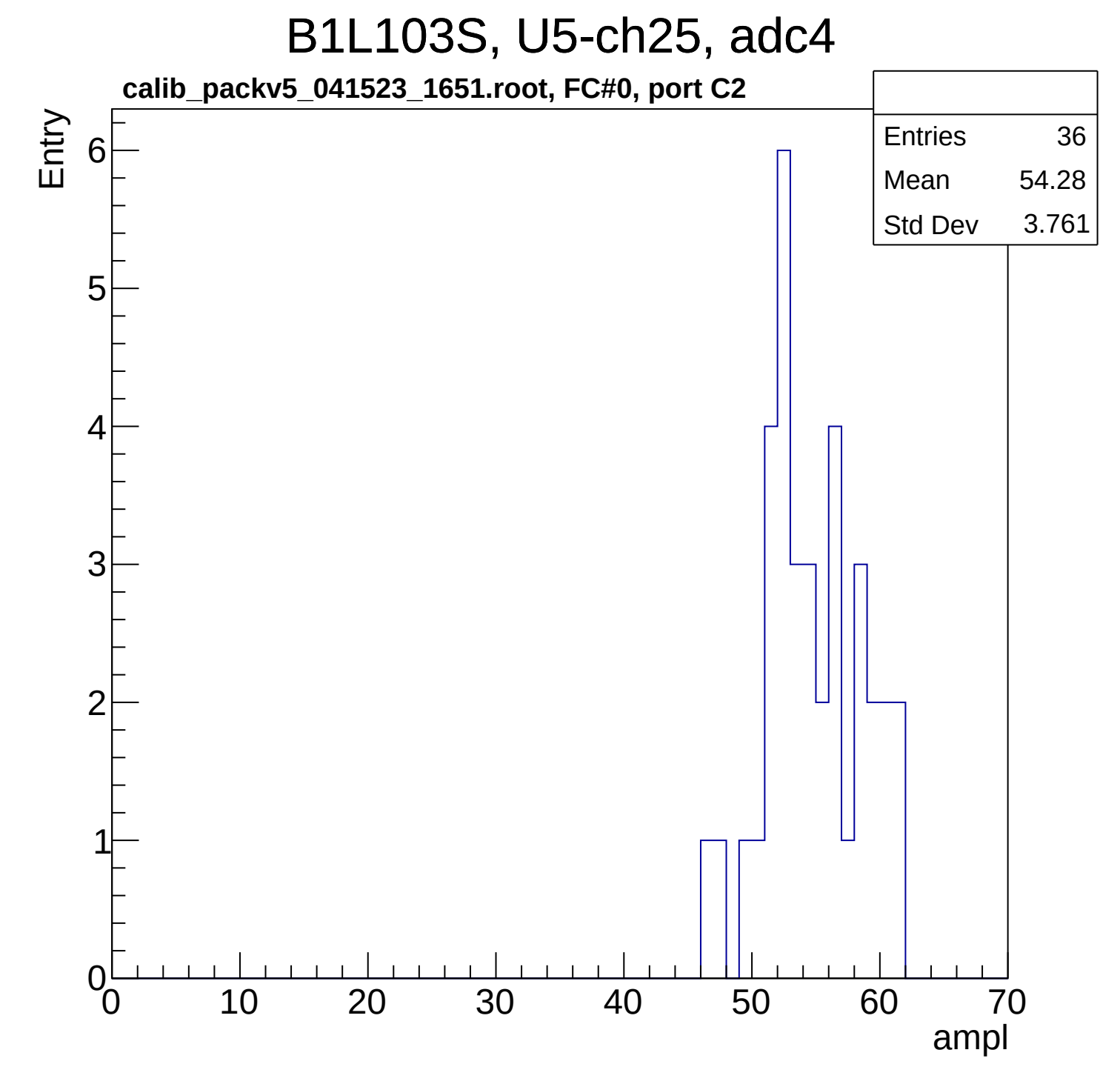
B1L103S, U5-ch25, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 54.28
Std Dev 3.761
Entry
ampl
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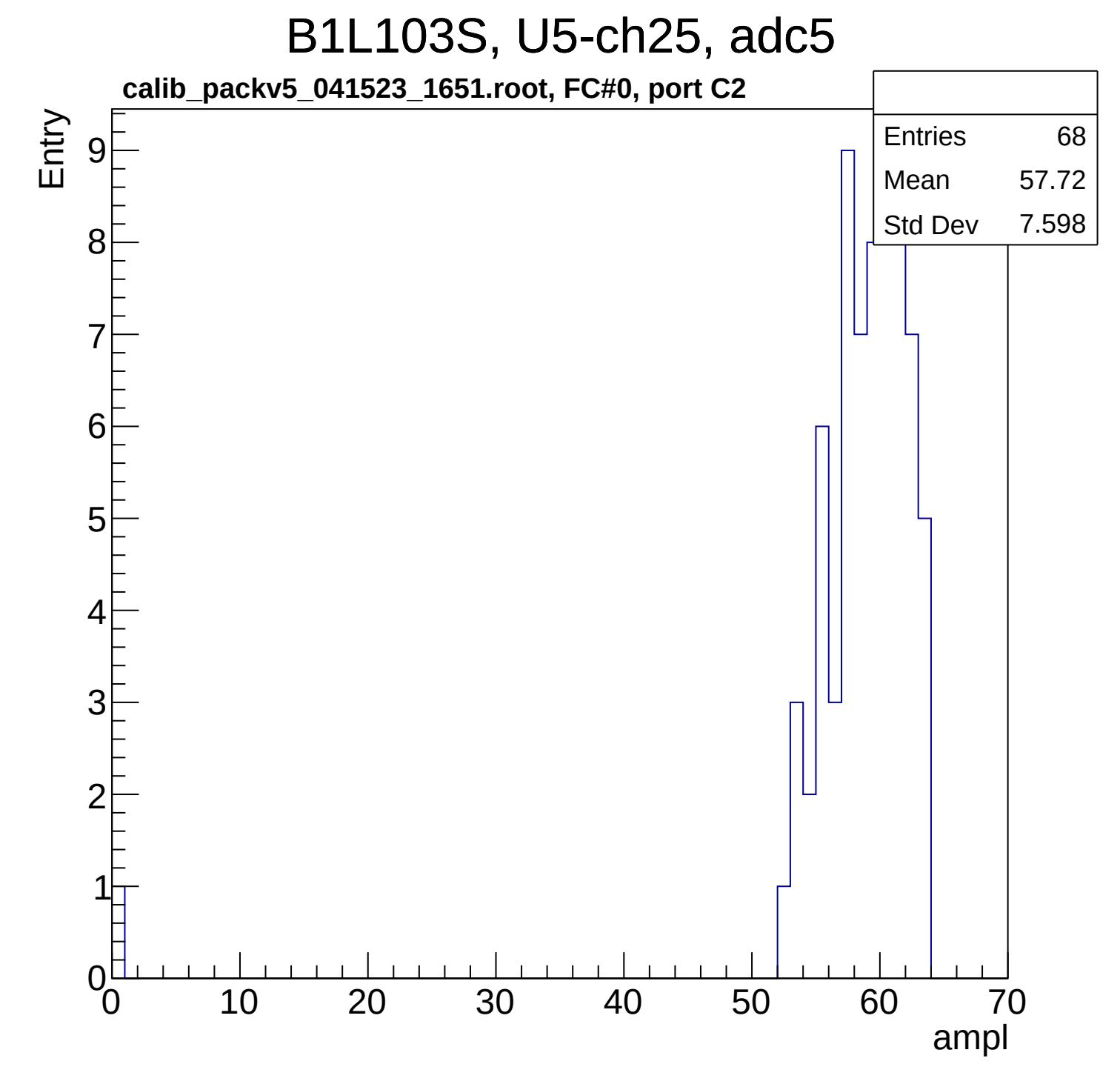
B1L103S, U5-ch25, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 57.72
Std Dev 7.598
Entry
ampl
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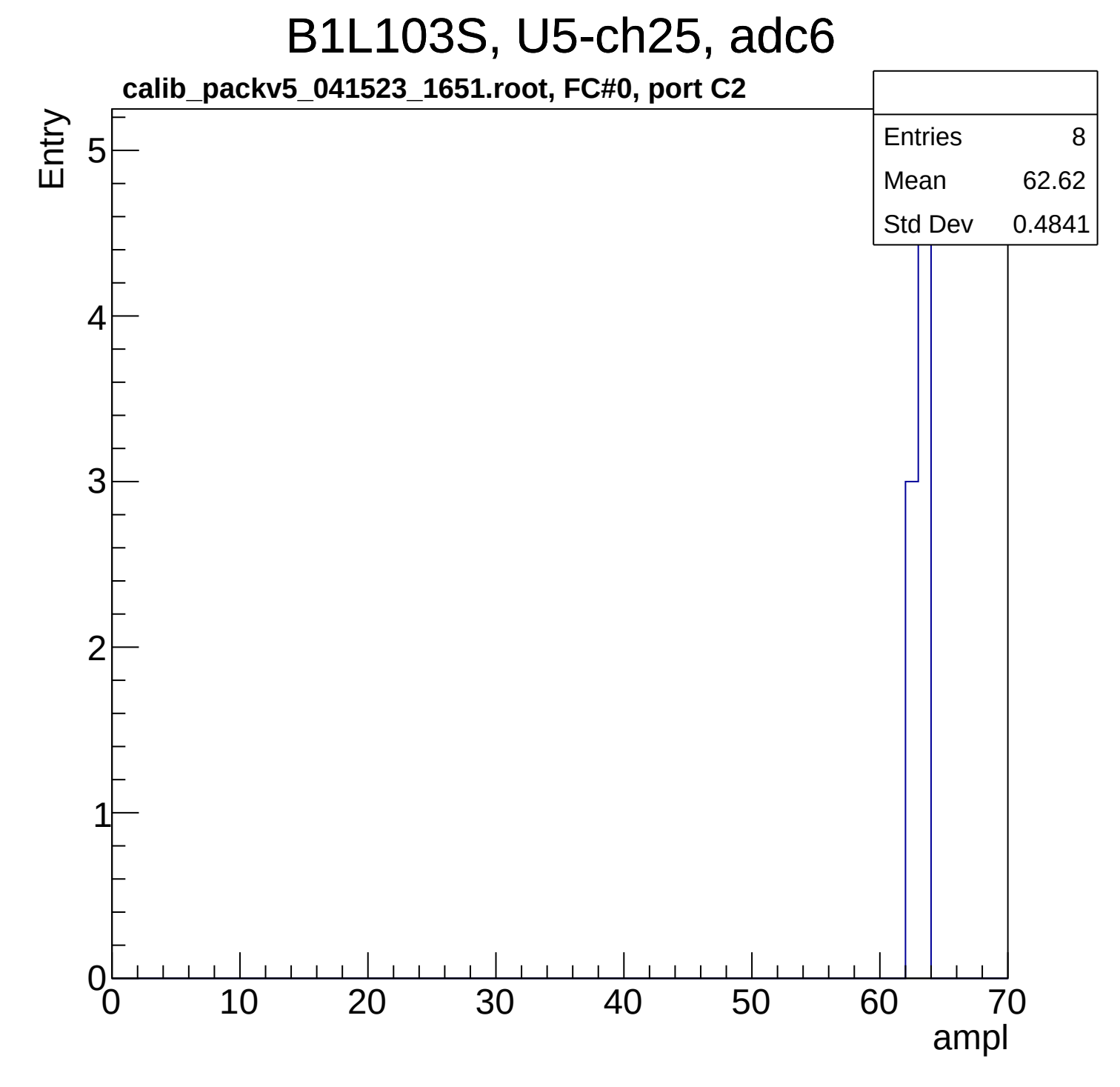
B1L103S, U5-ch25, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62.62
Std Dev 0.4841
Entry
ampl
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60
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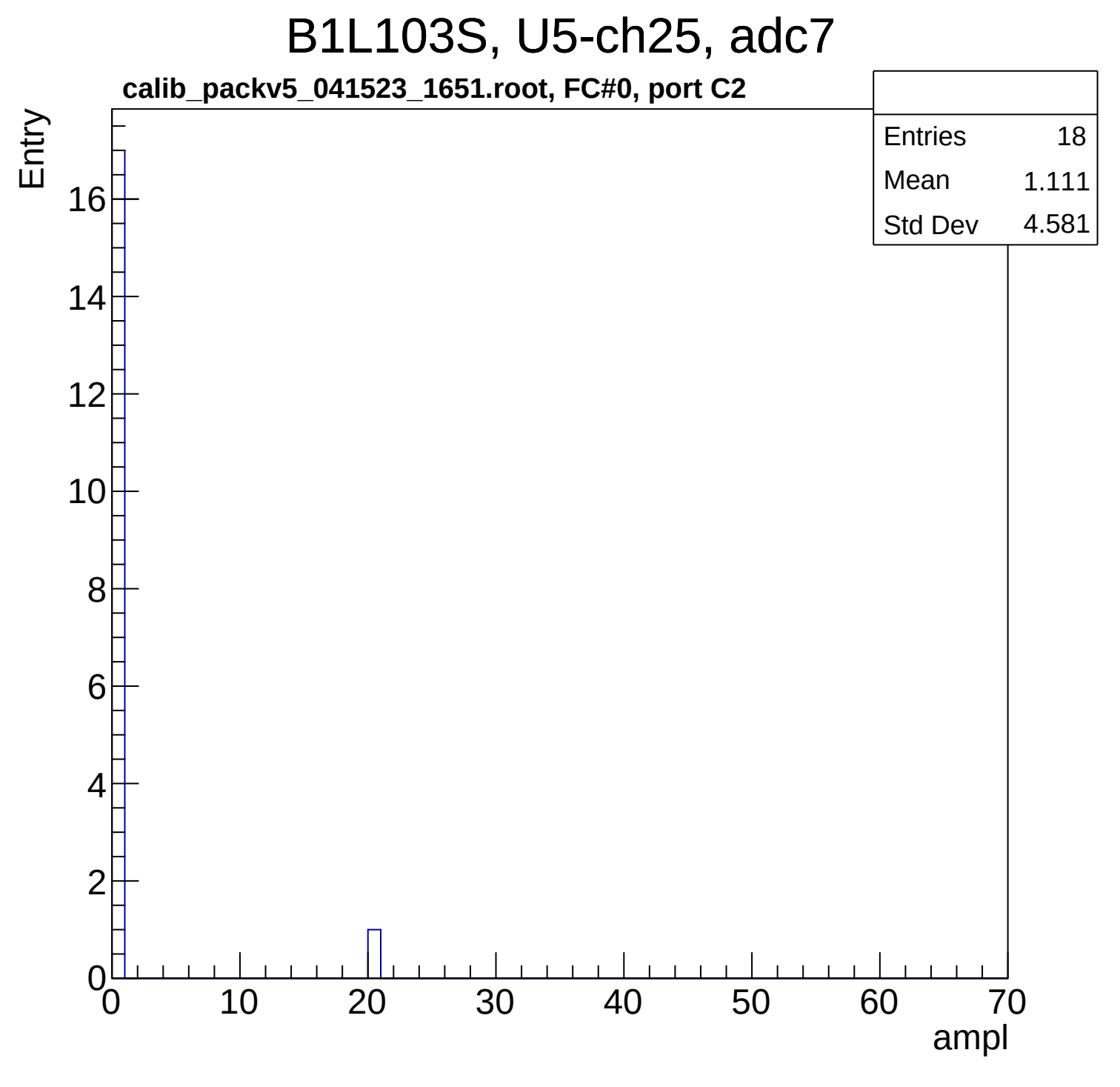
B1L103S, U5-ch25, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.111
Std Dev 4.581
Entry
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10
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50
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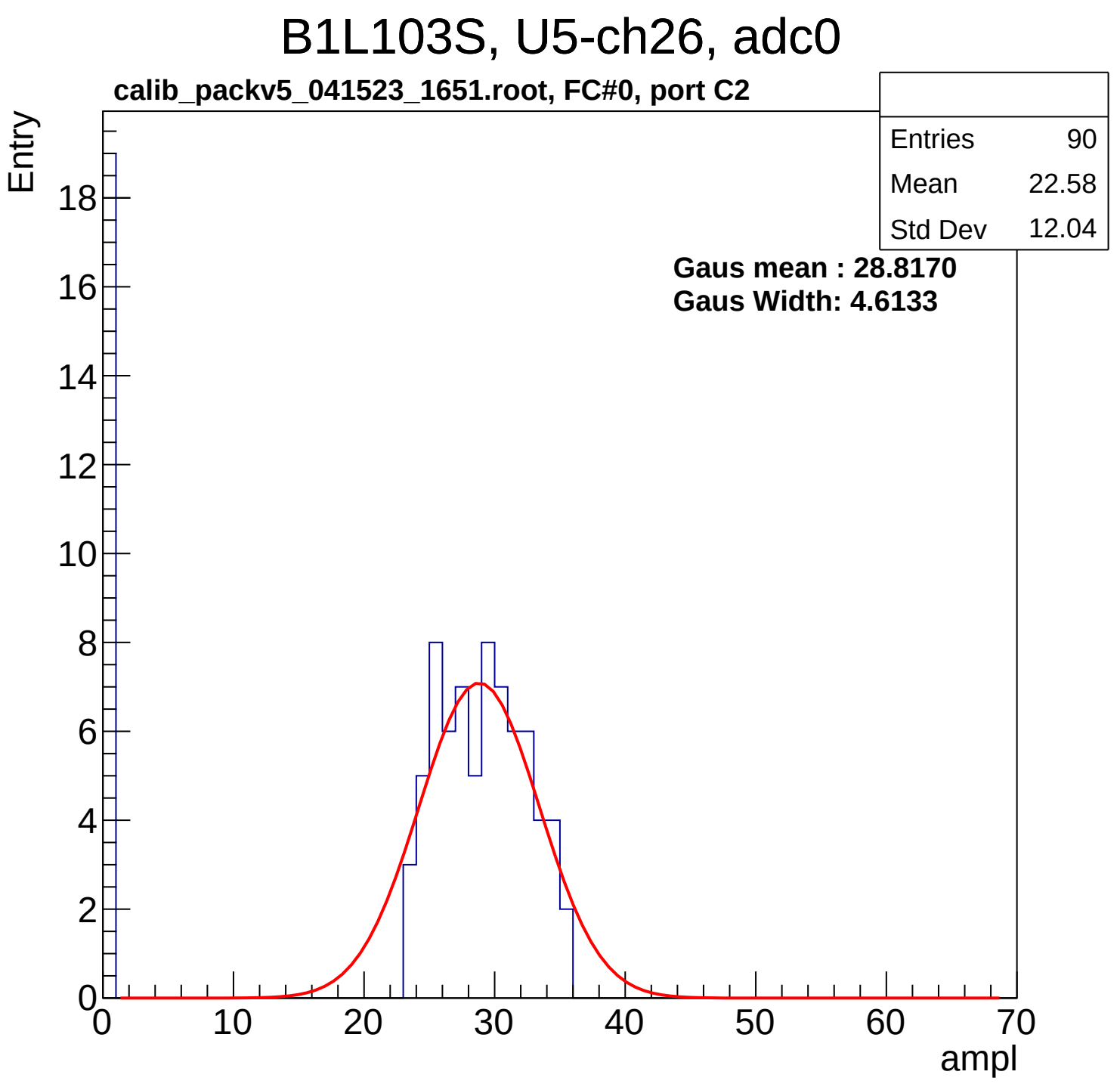
70
ampl


B1L103S, U5-ch26, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 22.58
Std Dev 12.04
Gaus mean : 28.8170
Gaus Width: 4.6133
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
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40
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60
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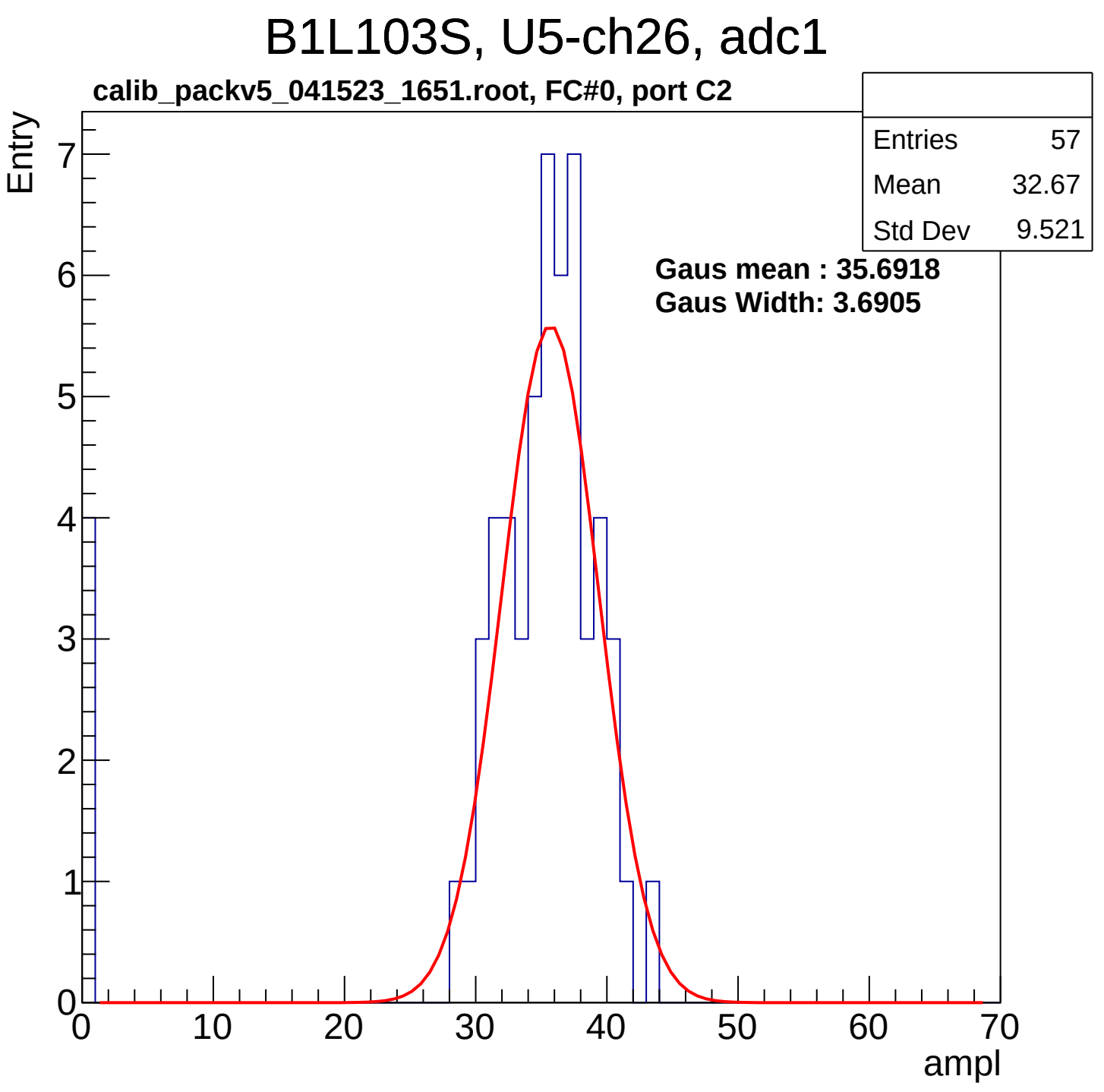
B1L103S, U5-ch26, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 32.67
Std Dev 9.521
Gaus mean : 35.6918
Gaus Width: 3.6905
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
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60
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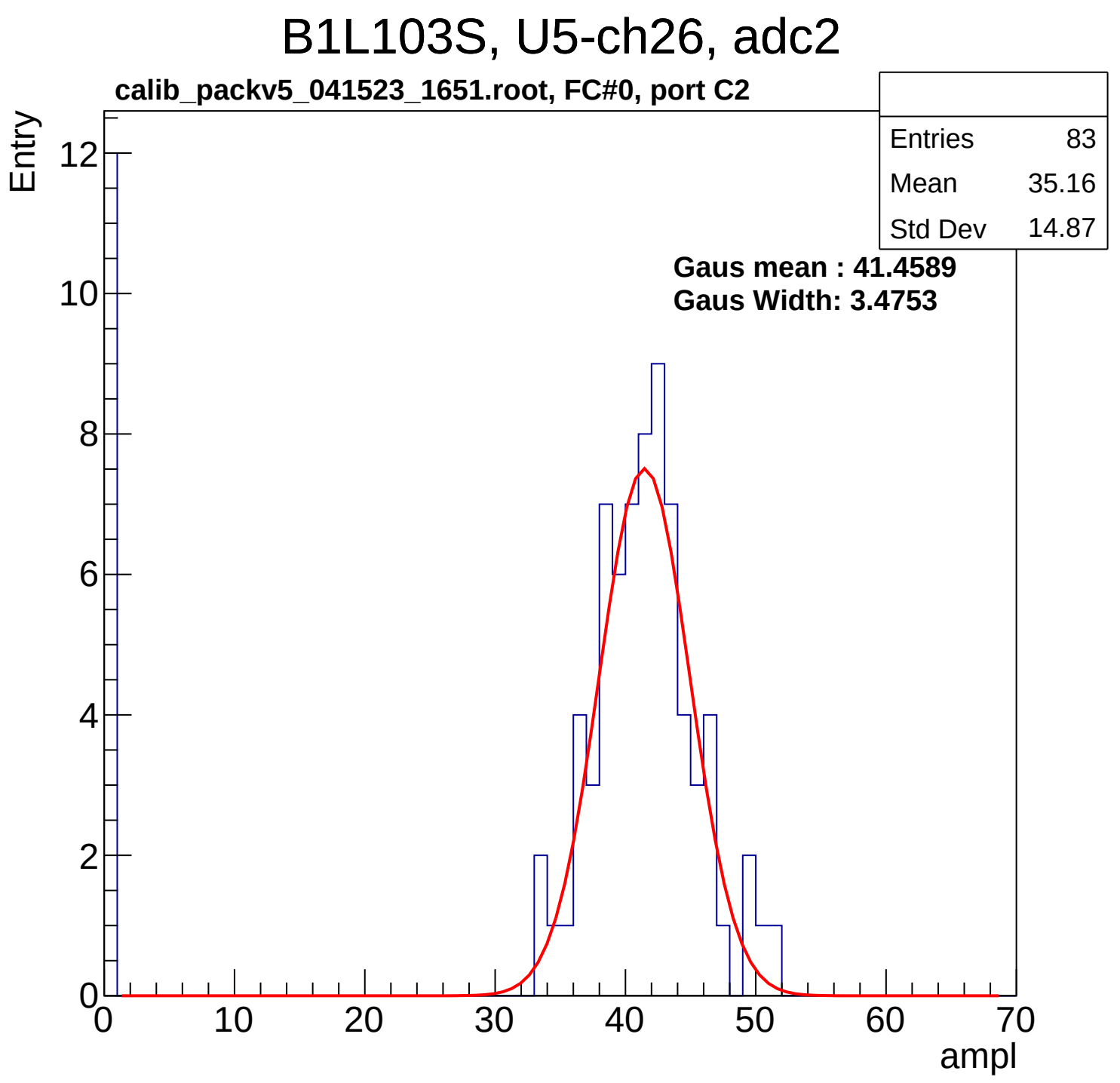
B1L103S, U5-ch26, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 35.16
Std Dev 14.87
Gaus mean : 41.4589
Gaus Width: 3.4753
Entry
ampl
0
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4
6
8
10
12
0
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60
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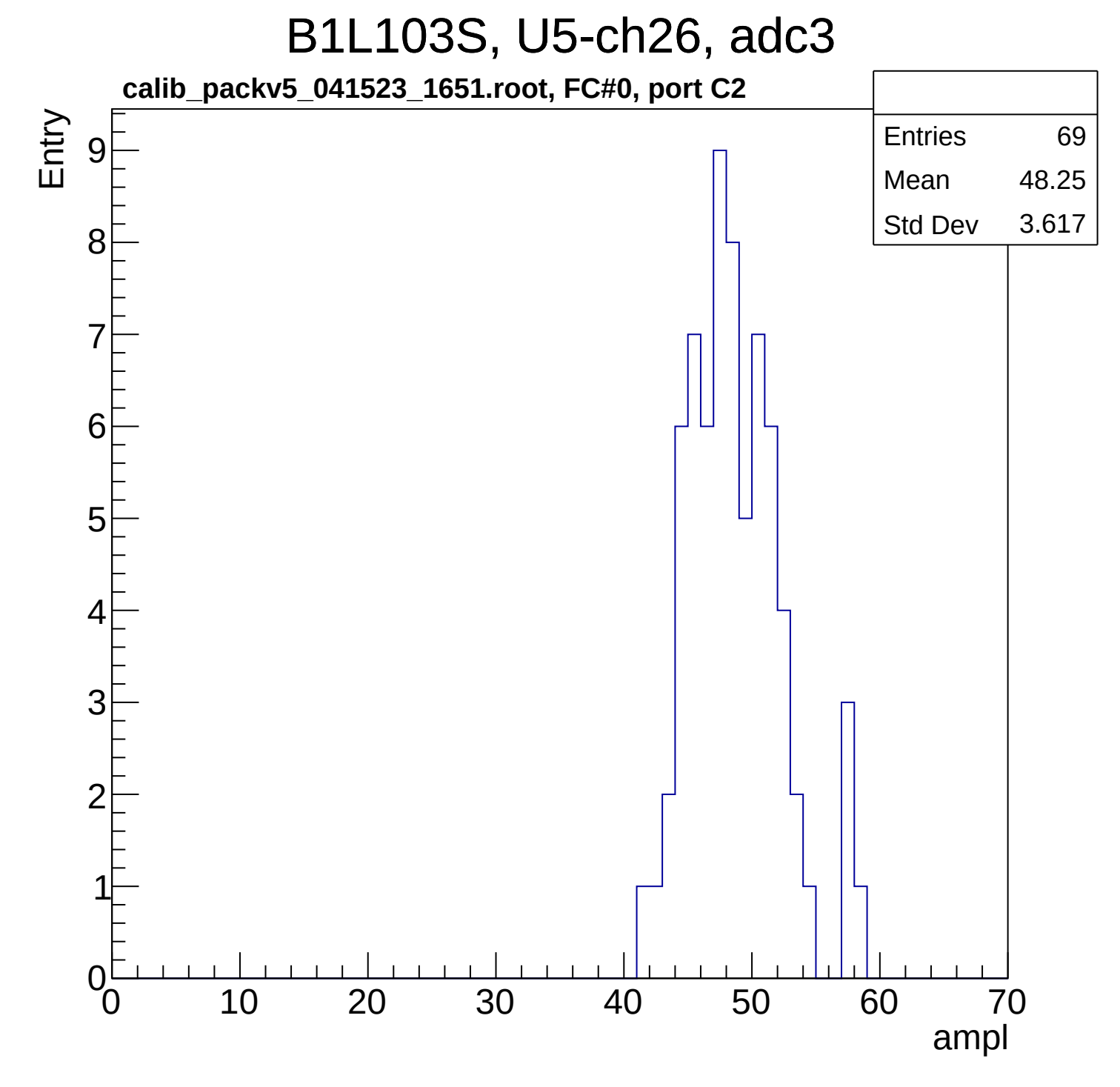
B1L103S, U5-ch26, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 48.25
Std Dev 3.617
Entry
ampl
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4
5
6
7
8
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0
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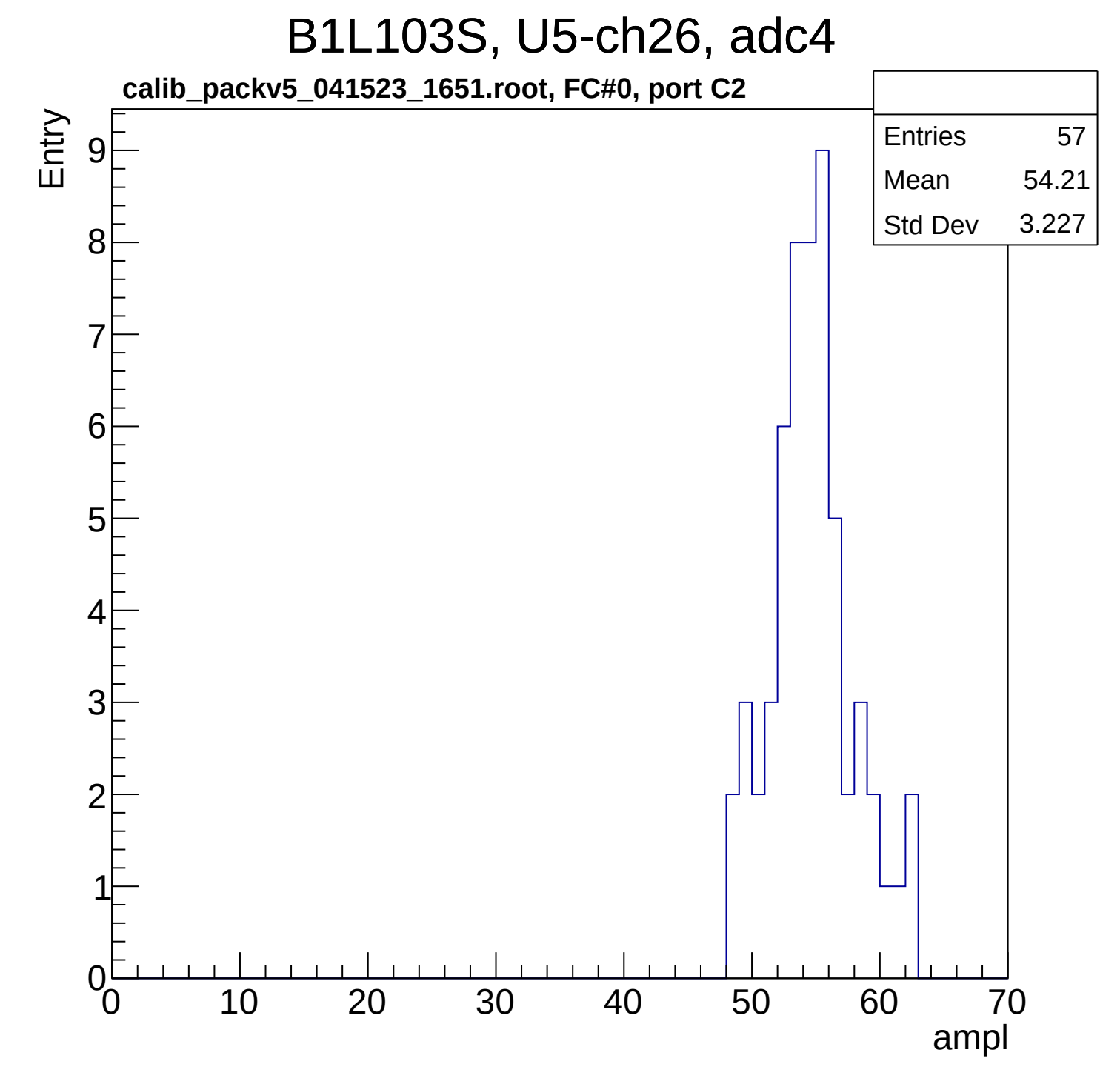
B1L103S, U5-ch26, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 54.21
Std Dev 3.227
Entry
ampl
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4
5
6
7
8
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0
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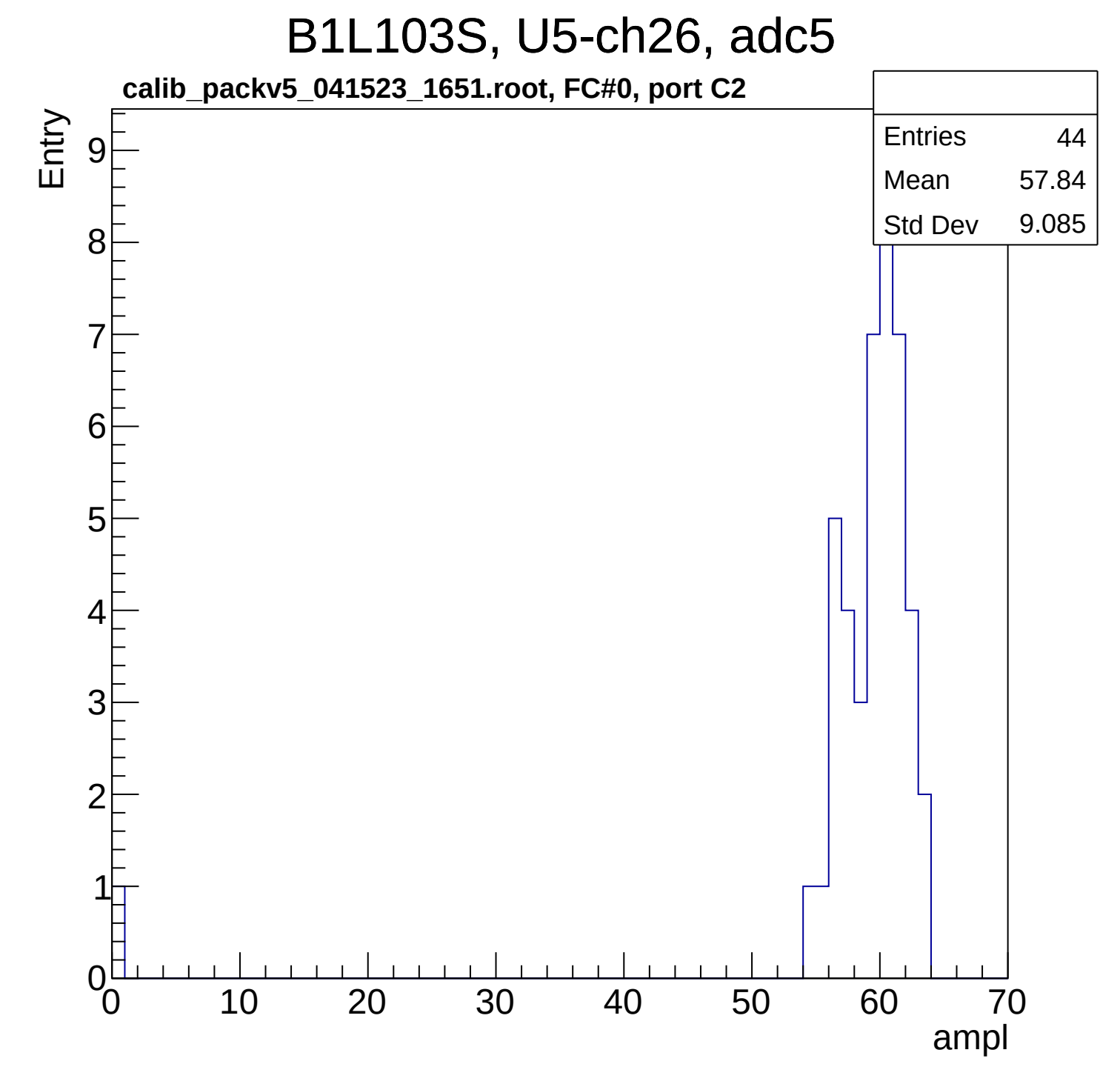
B1L103S, U5-ch26, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 57.84
Std Dev 9.085
Entry
ampl
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3
4
5
6
7
8
9
0
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20
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40
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60
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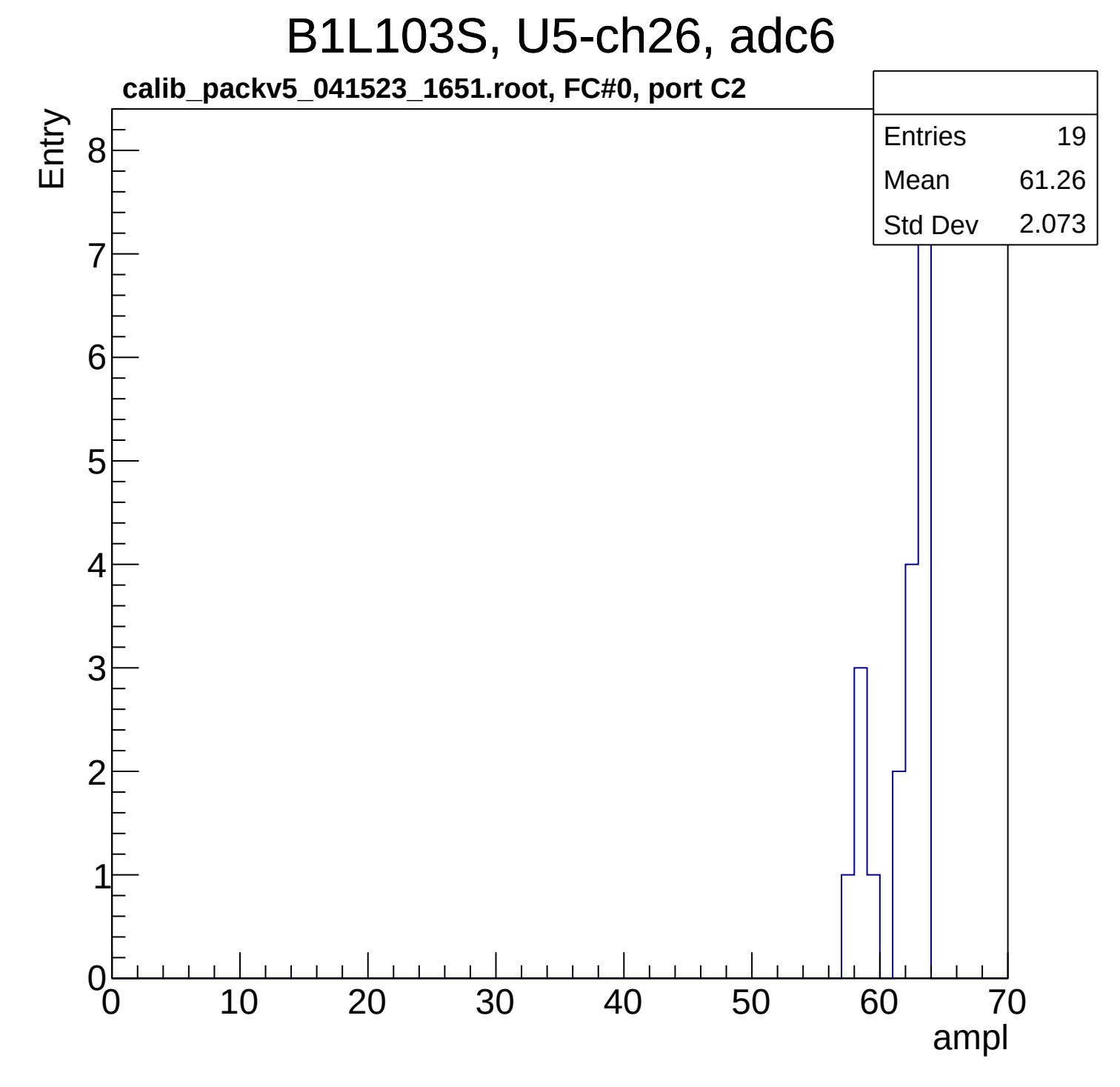
B1L103S, U5-ch26, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 61.26
Std Dev 2.073
Entry
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2
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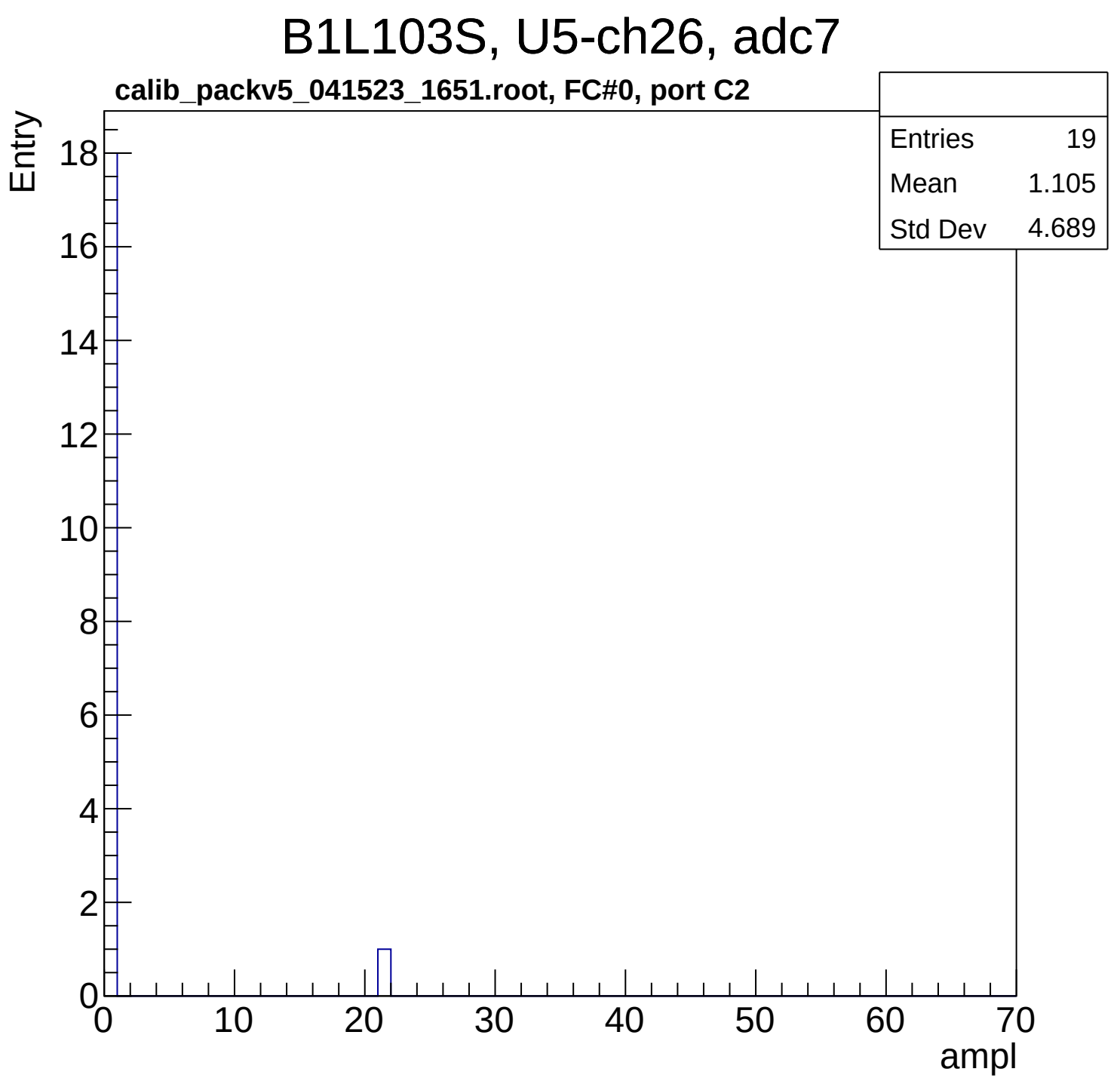
B1L103S, U5-ch26, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
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6
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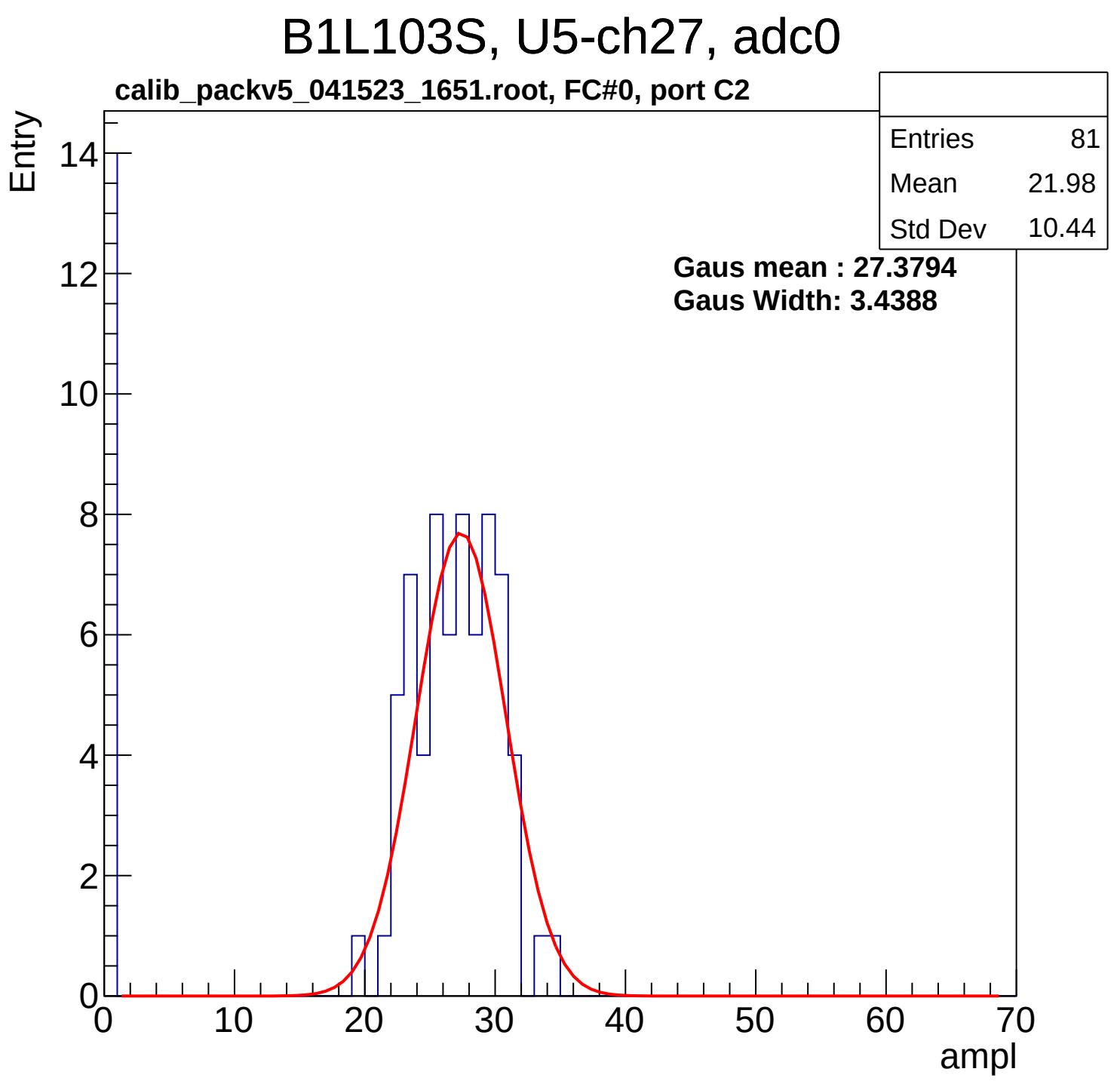
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch27, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 21.98
Std Dev 10.44
Gaus mean : 27.3794
Gaus Width: 3.4388
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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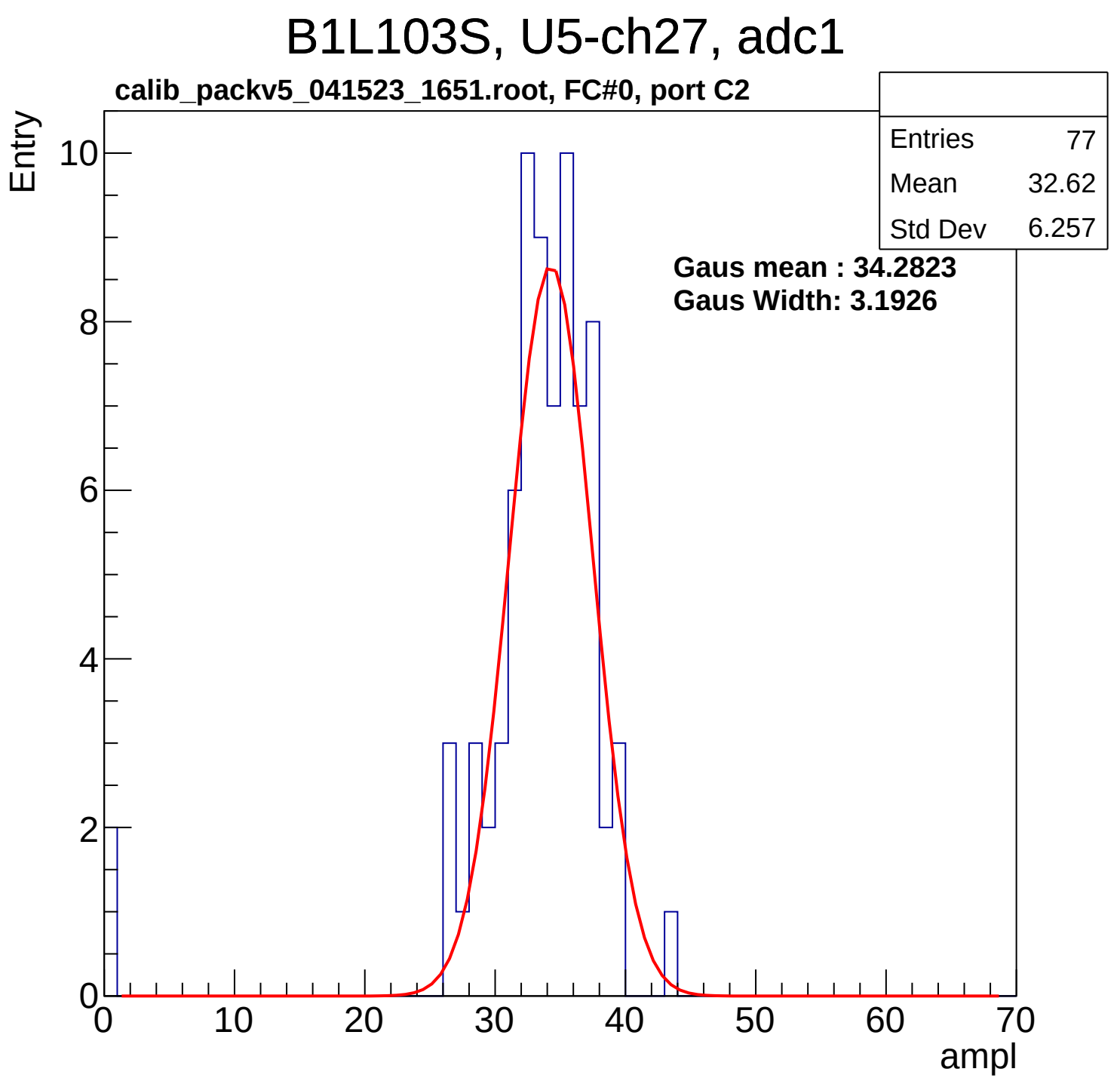
B1L103S, U5-ch27, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 32.62
Std Dev 6.257
Gaus mean : 34.2823
Gaus Width: 3.1926
Entry
ampl
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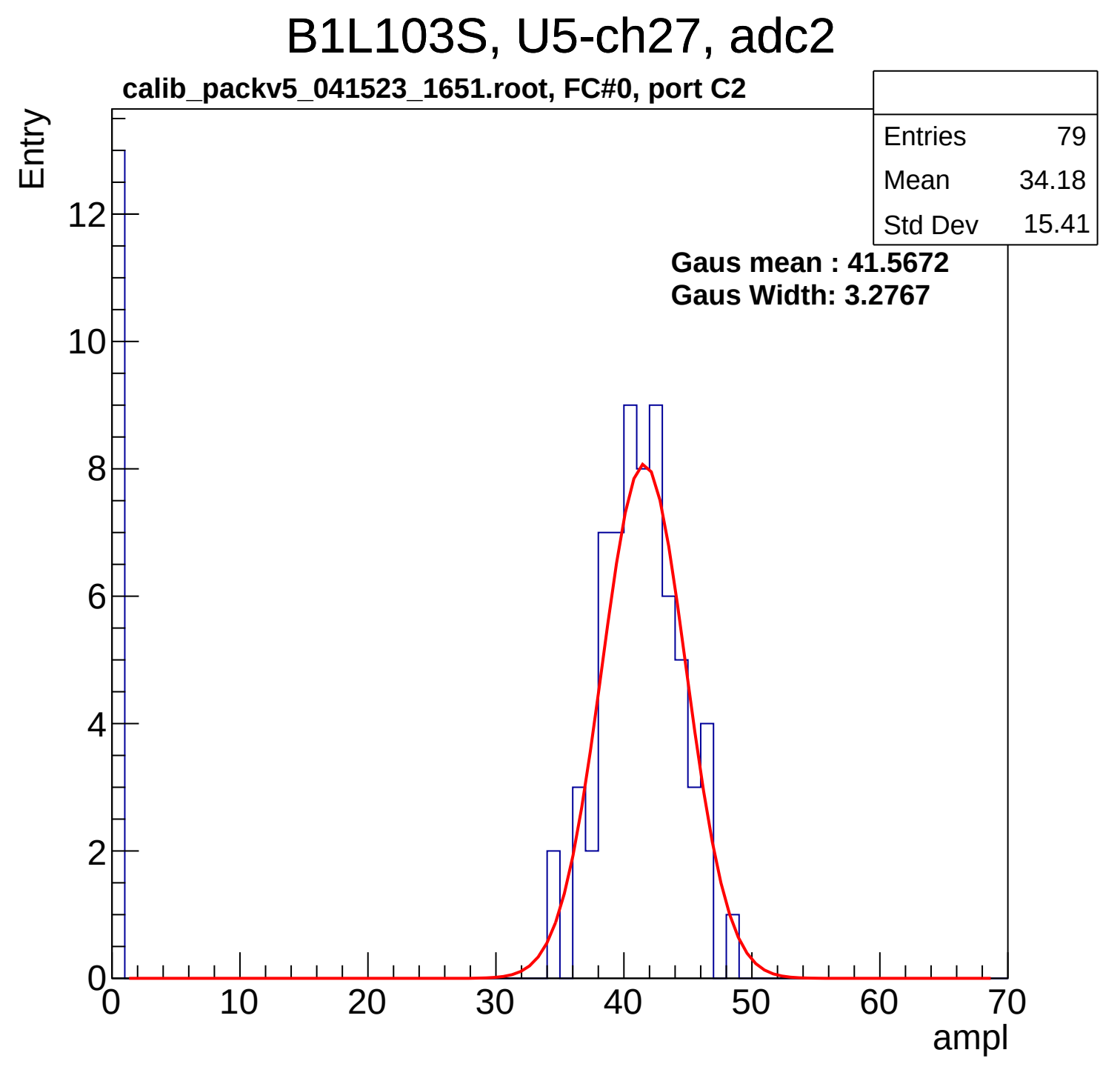
B1L103S, U5-ch27, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 34.18
Std Dev 15.41
Gaus mean : 41.5672
Gaus Width: 3.2767
Entry
ampl
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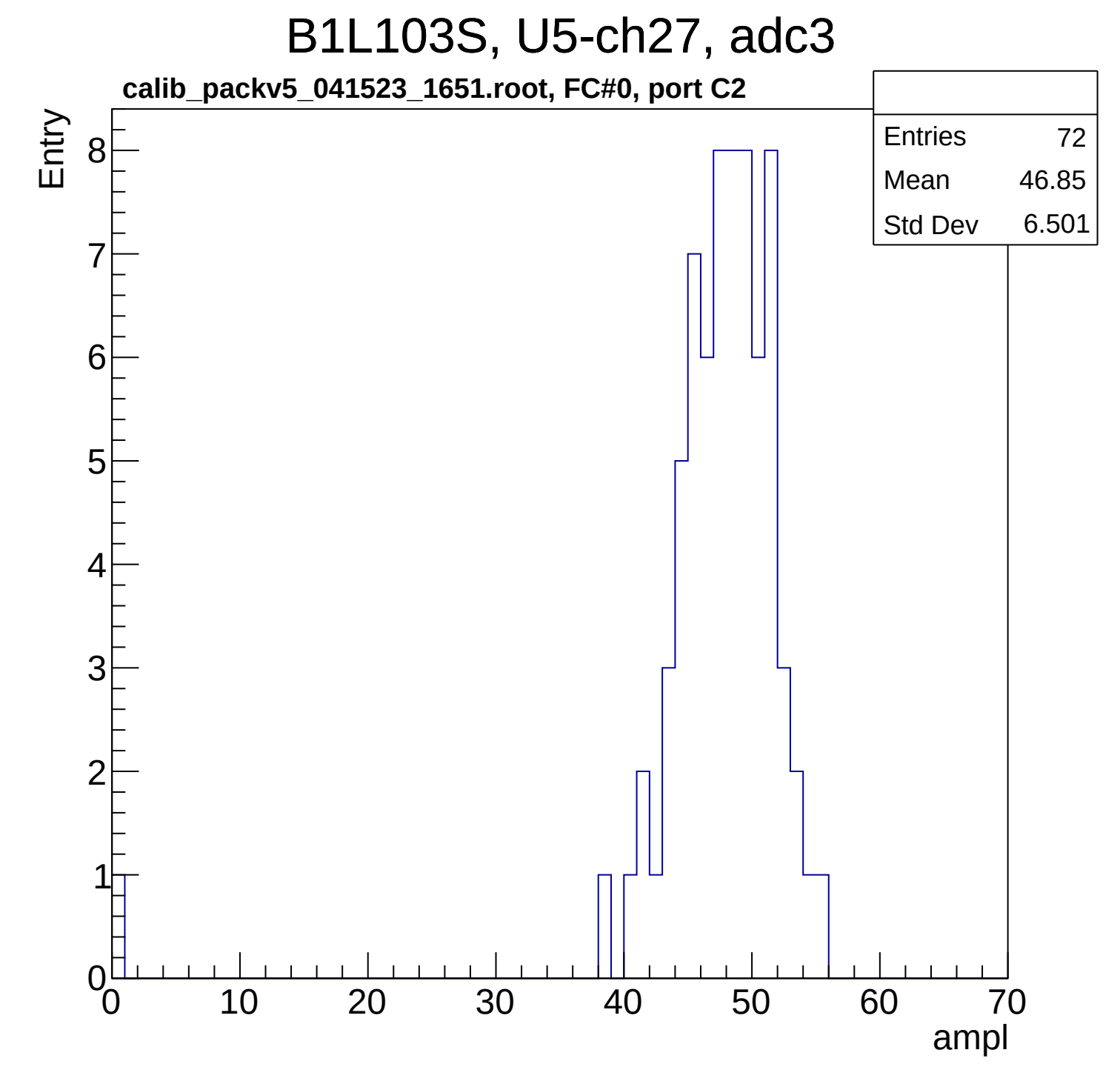
B1L103S, U5-ch27, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 46.85
Std Dev 6.501
Entry
ampl
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1
2
3
4
5
6
7
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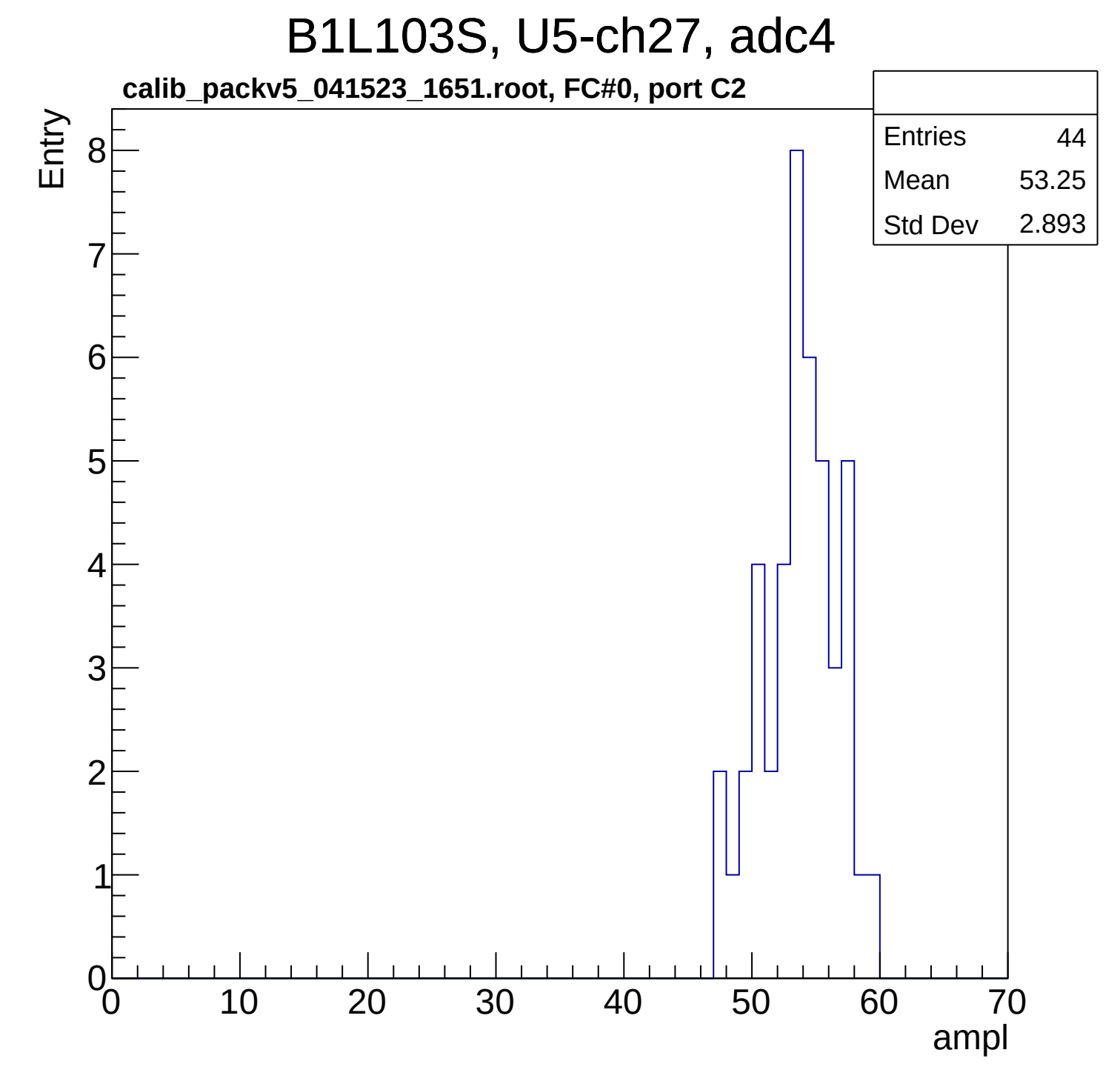
B1L103S, U5-ch27, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 53.25
Std Dev 2.893
Entry
ampl
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1
2
3
4
5
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7
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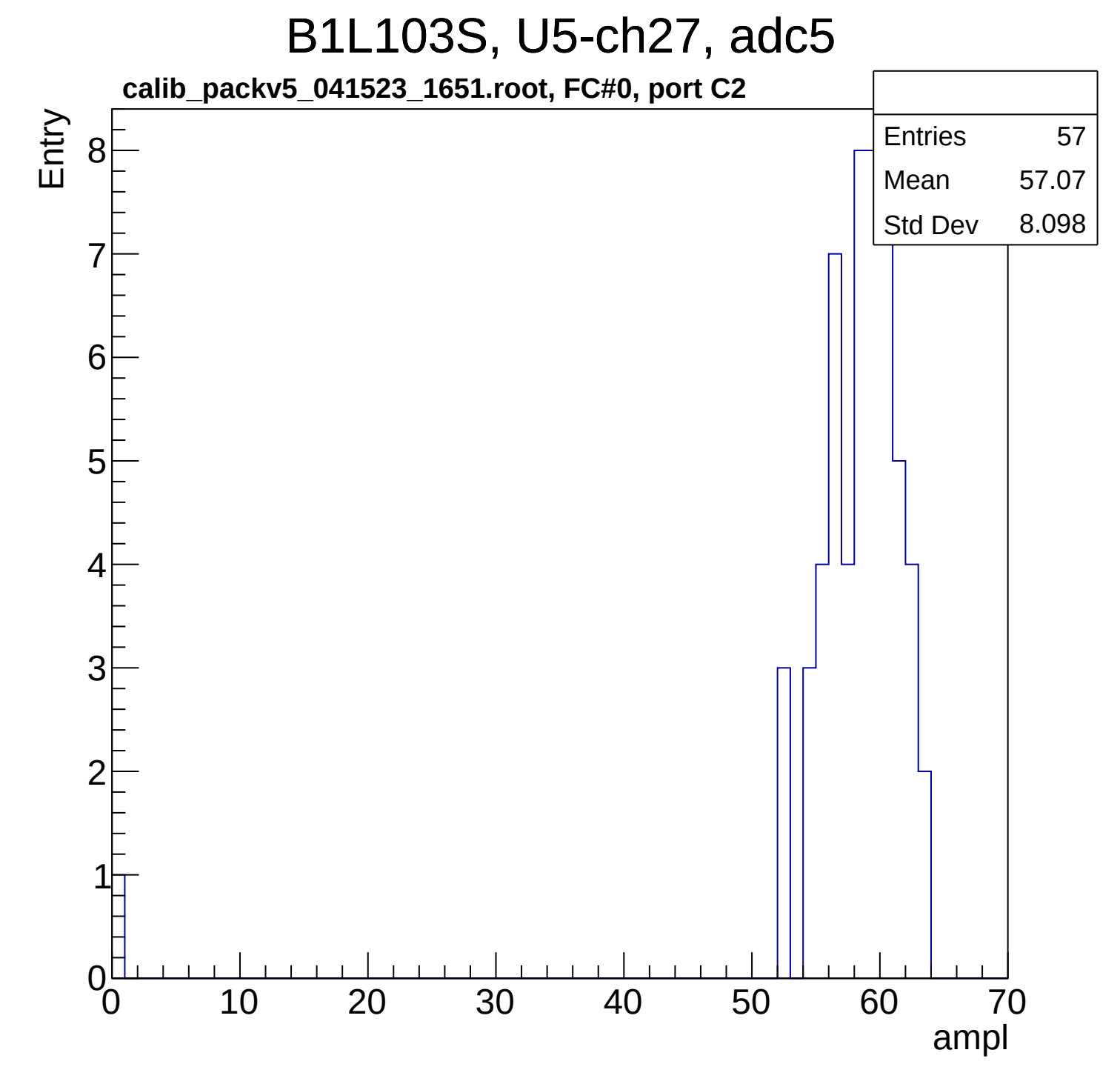
B1L103S, U5-ch27, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 57.07
Std Dev 8.098
Entry
ampl
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2
3
4
5
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0
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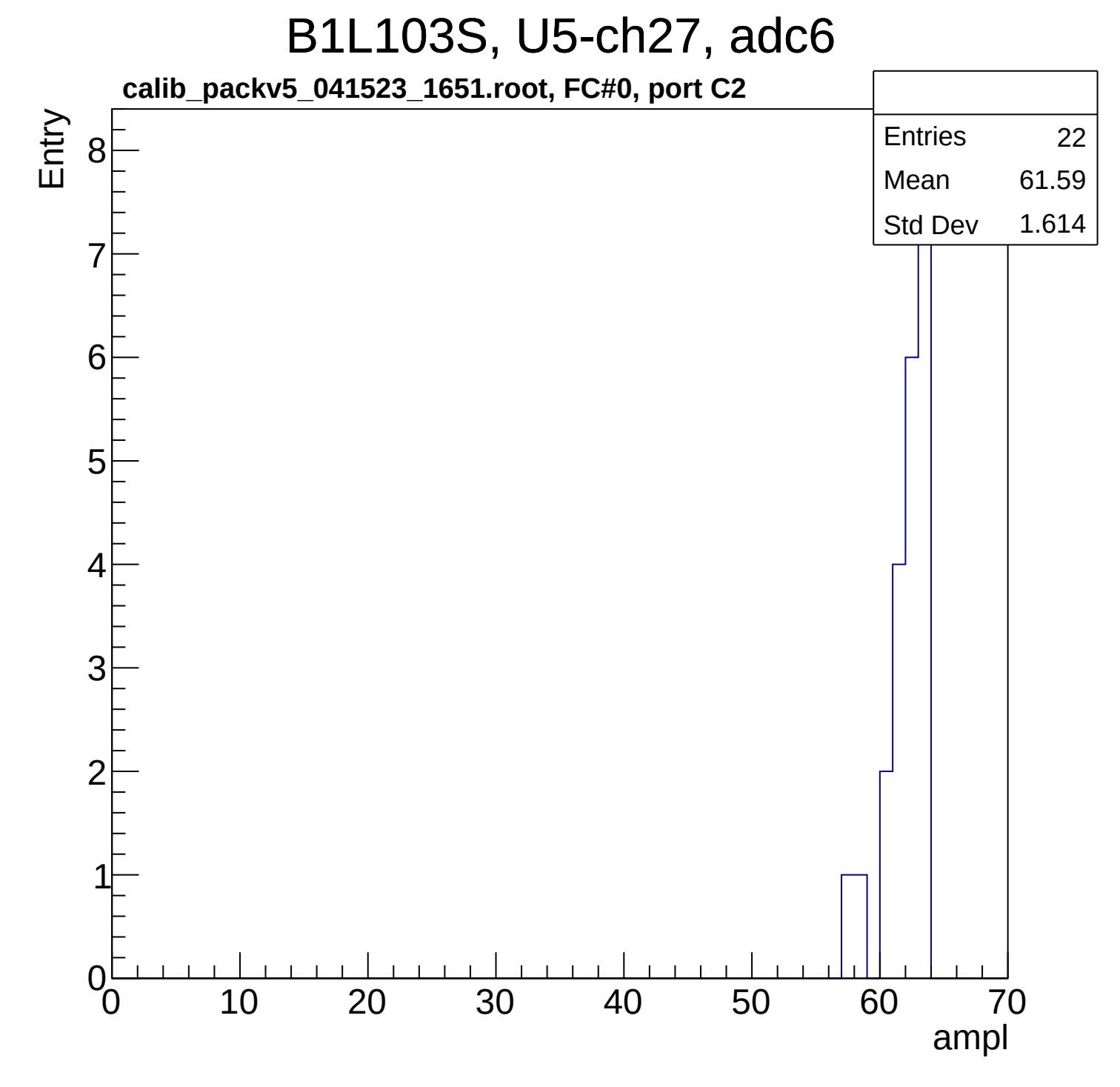
B1L103S, U5-ch27, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 61.59
Std Dev 1.614
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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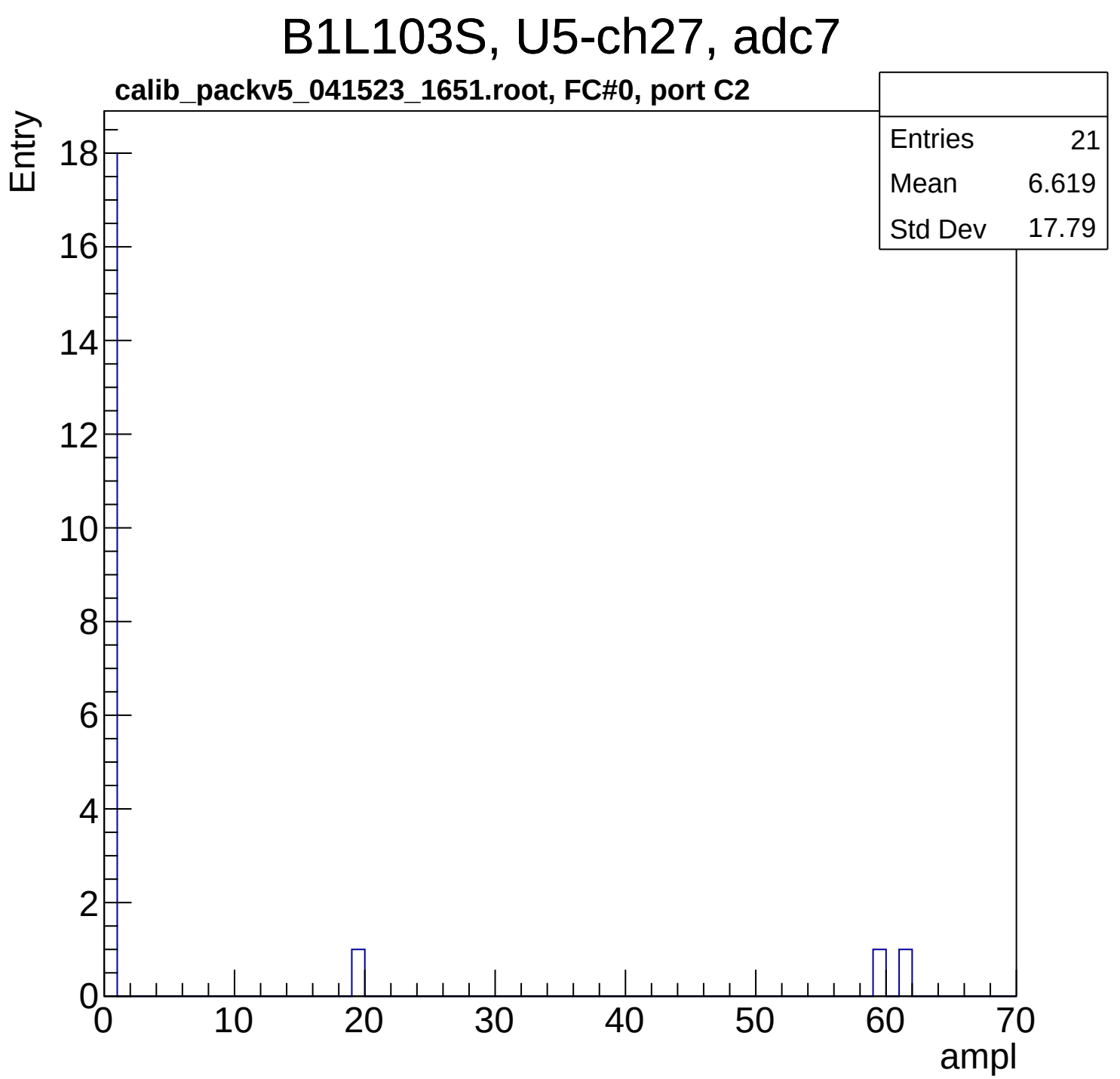
B1L103S, U5-ch27, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6.619
Std Dev 17.79
Entry
0
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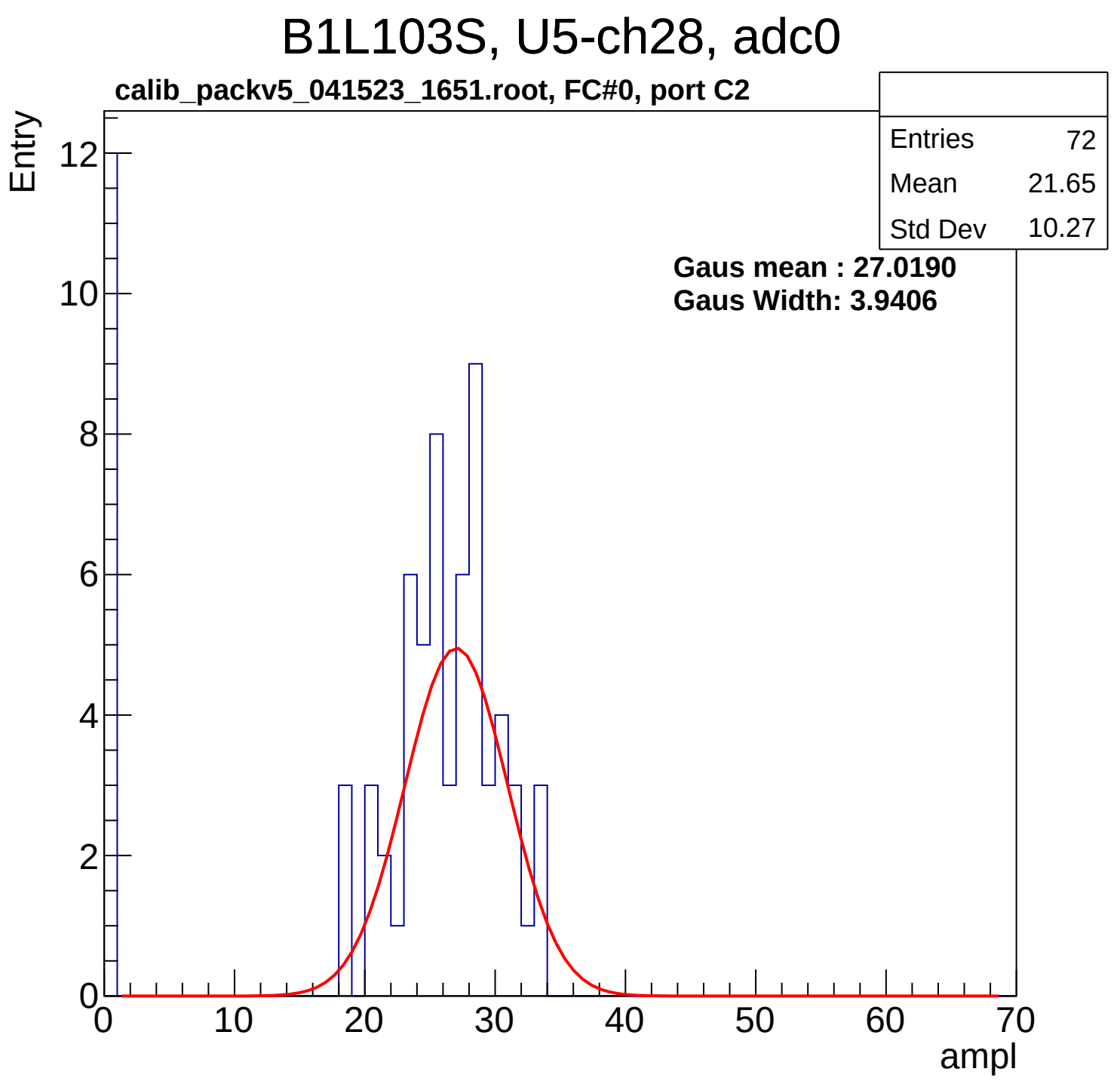
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch28, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 21.65
Std Dev 10.27
Gaus mean : 27.0190
Gaus Width: 3.9406
Entry
ampl
0
2
4
6
8
10
12
0
10
20
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40
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60
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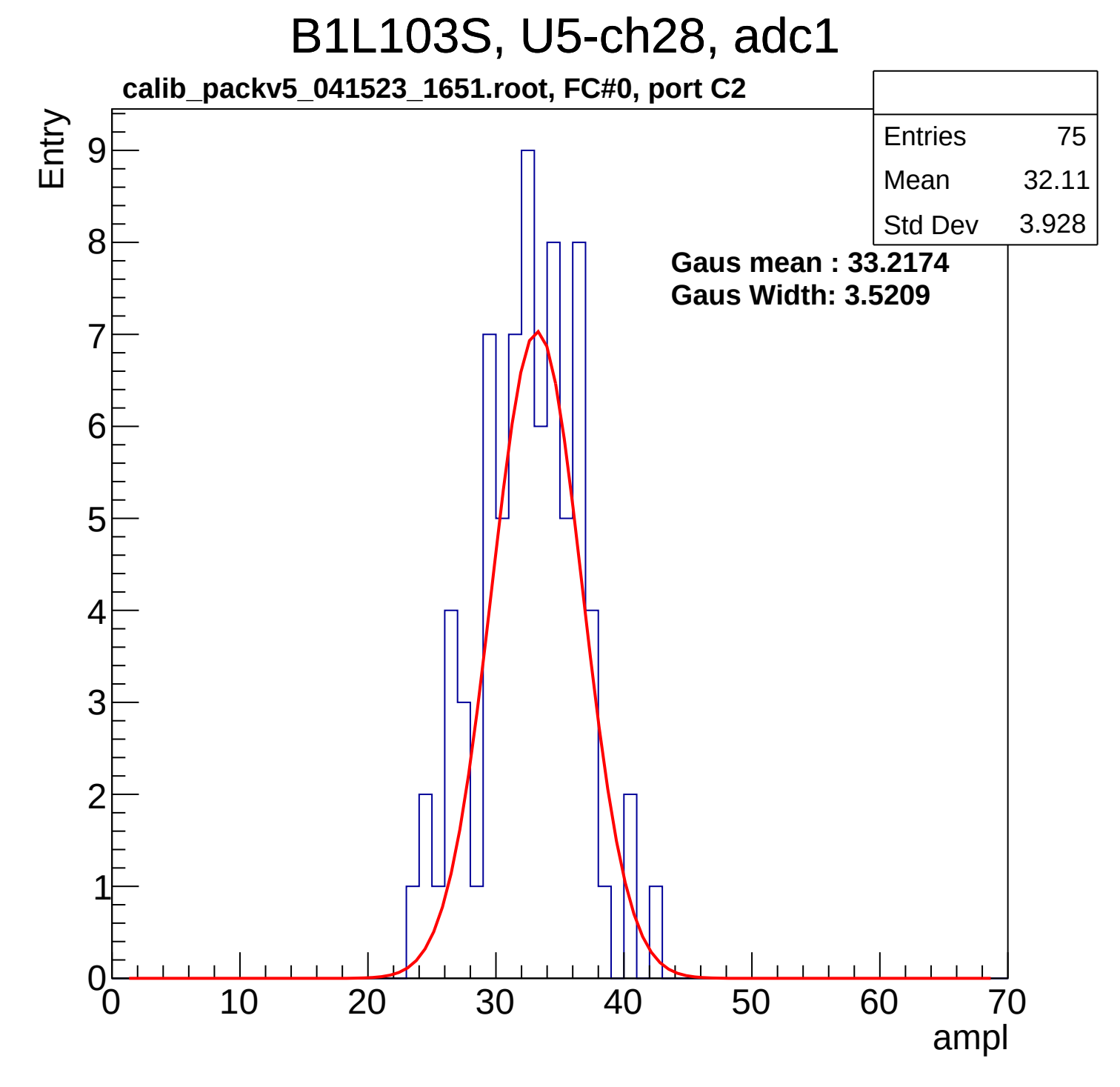
B1L103S, U5-ch28, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 32.11
Std Dev 3.928
Gaus mean : 33.2174
Gaus Width: 3.5209
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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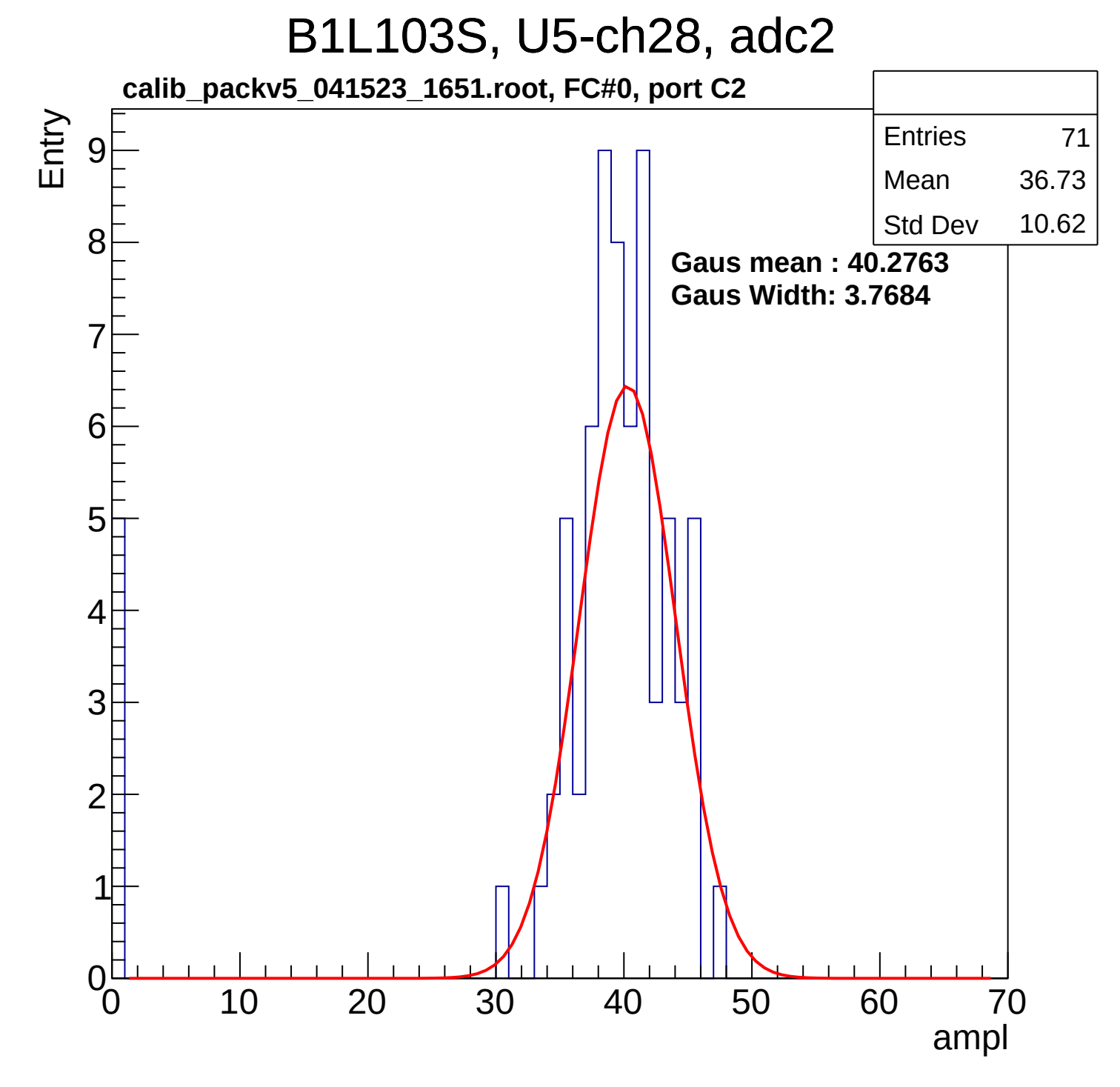
B1L103S, U5-ch28, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 36.73
Std Dev 10.62
Gaus mean : 40.2763
Gaus Width: 3.7684
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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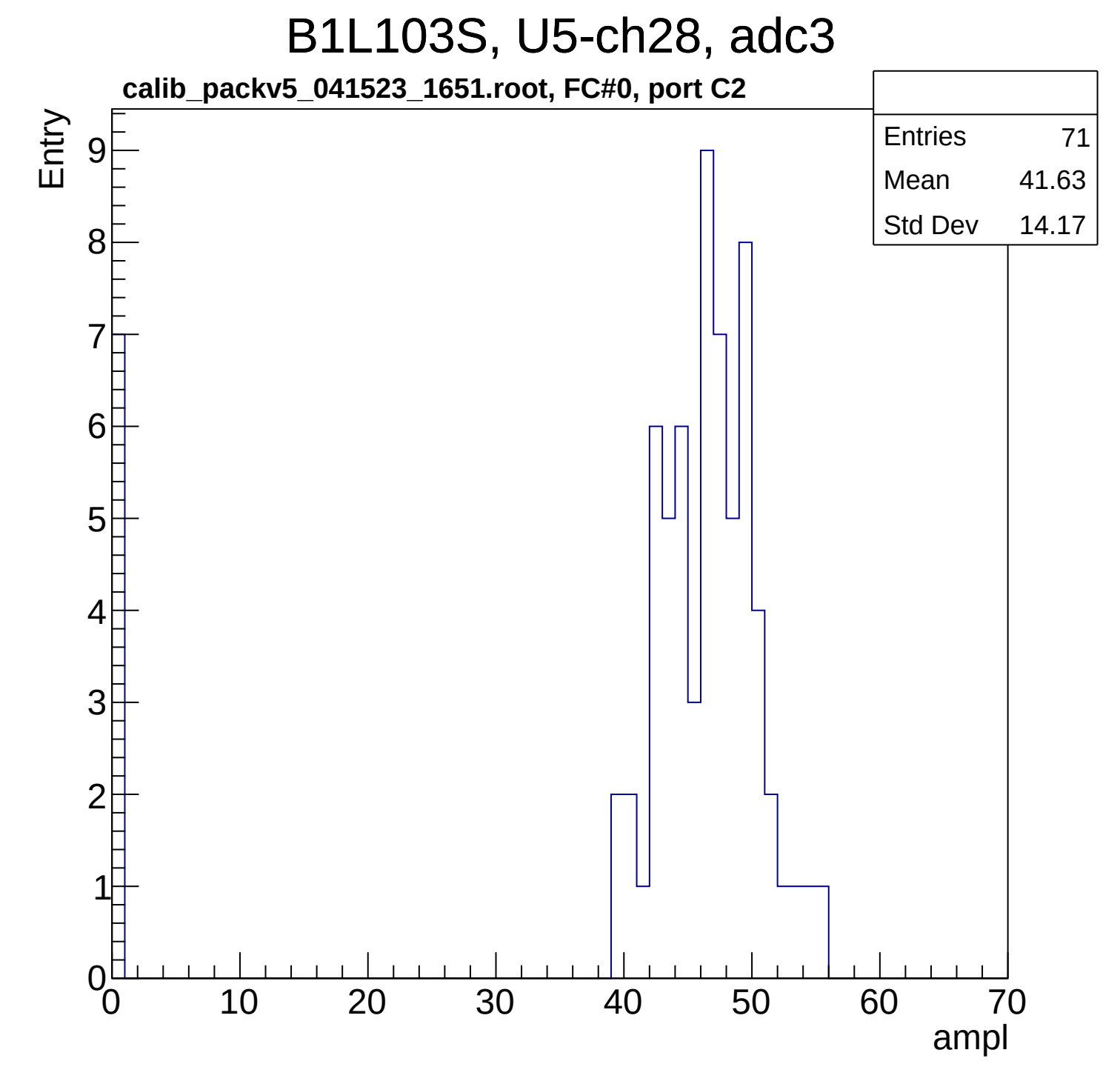
B1L103S, U5-ch28, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 41.63
Std Dev 14.17
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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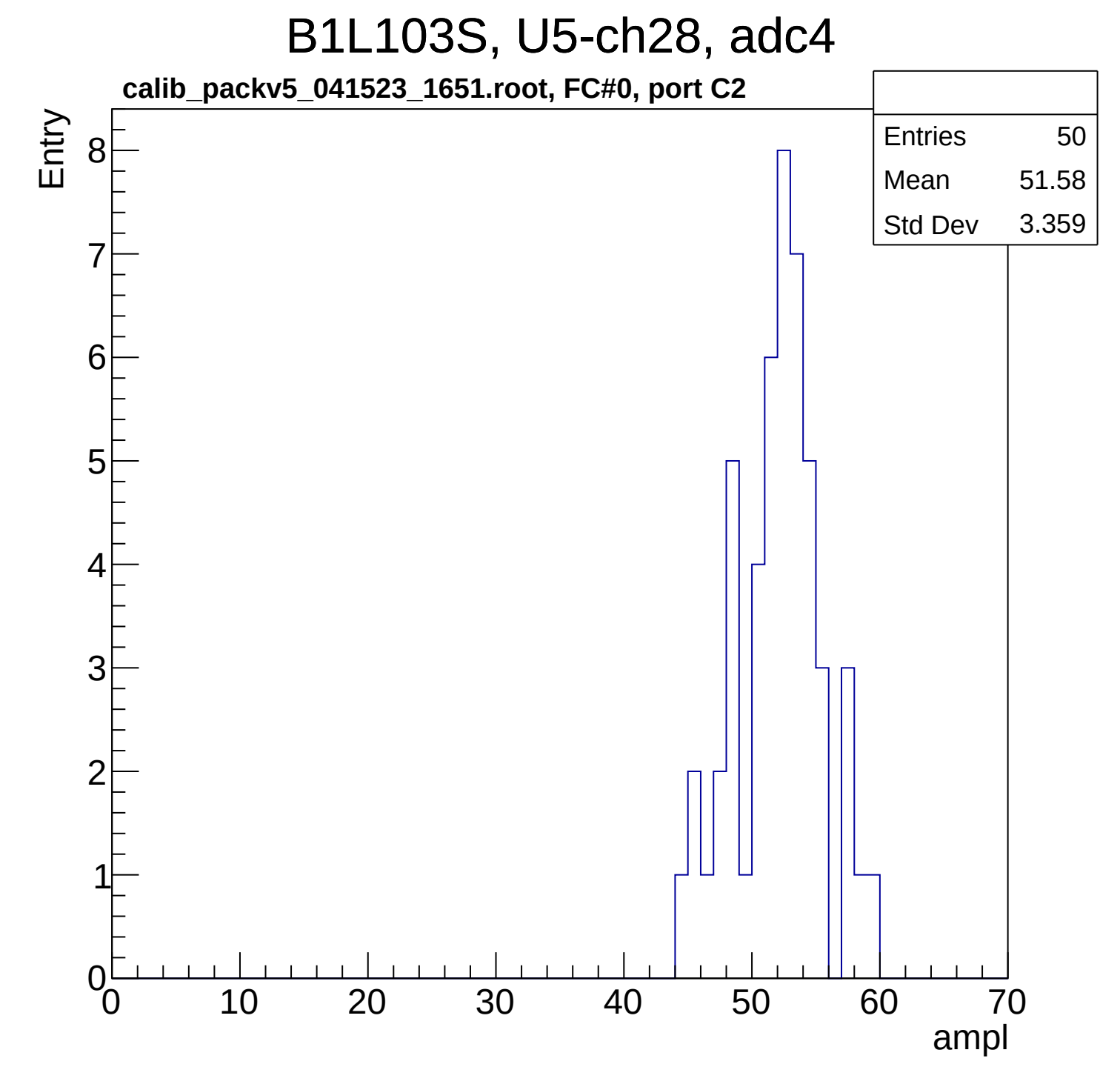
B1L103S, U5-ch28, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 51.58
Std Dev 3.359
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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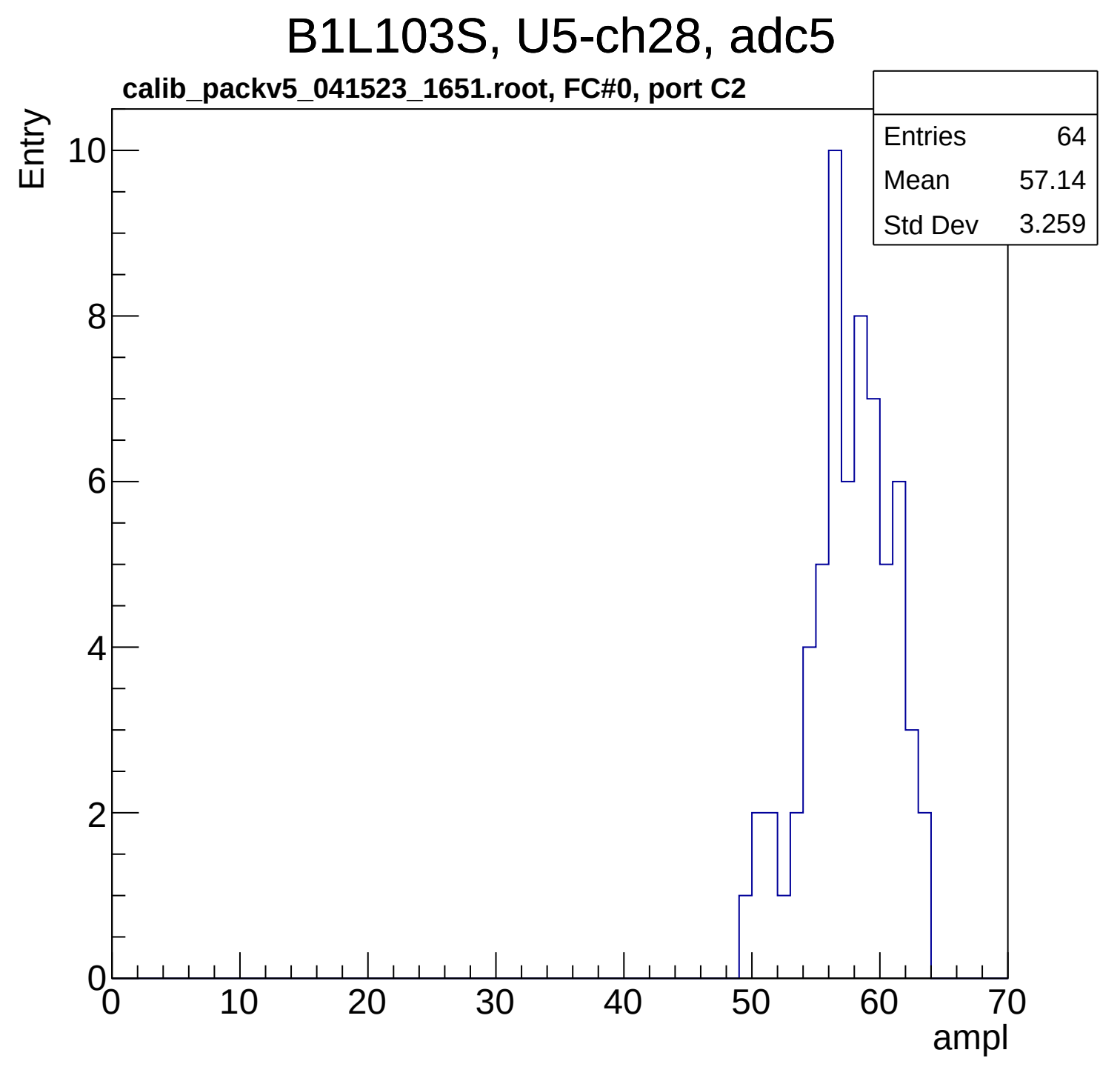
B1L103S, U5-ch28, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 57.14
Std Dev 3.259
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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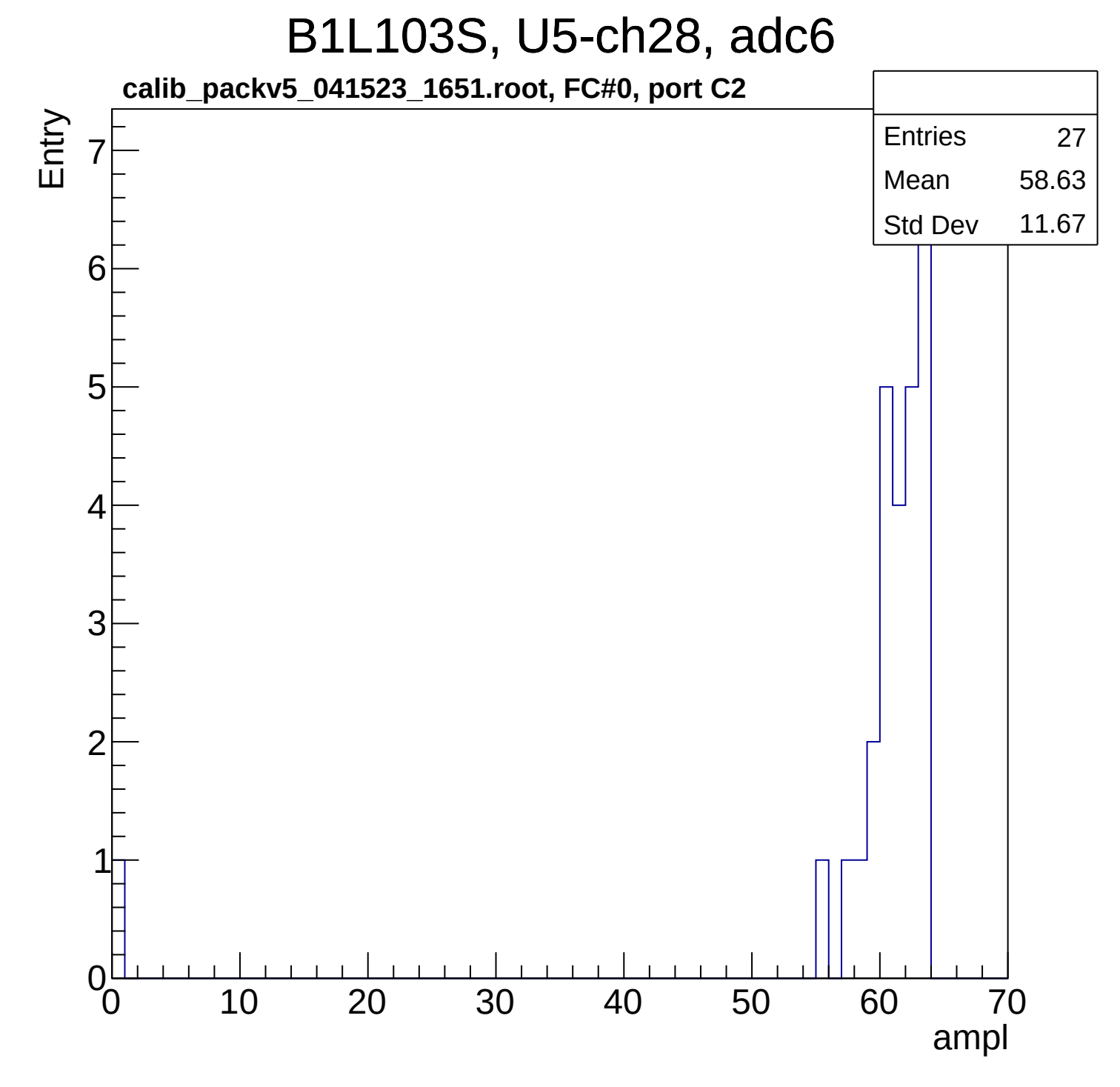
B1L103S, U5-ch28, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 58.63
Std Dev 11.67
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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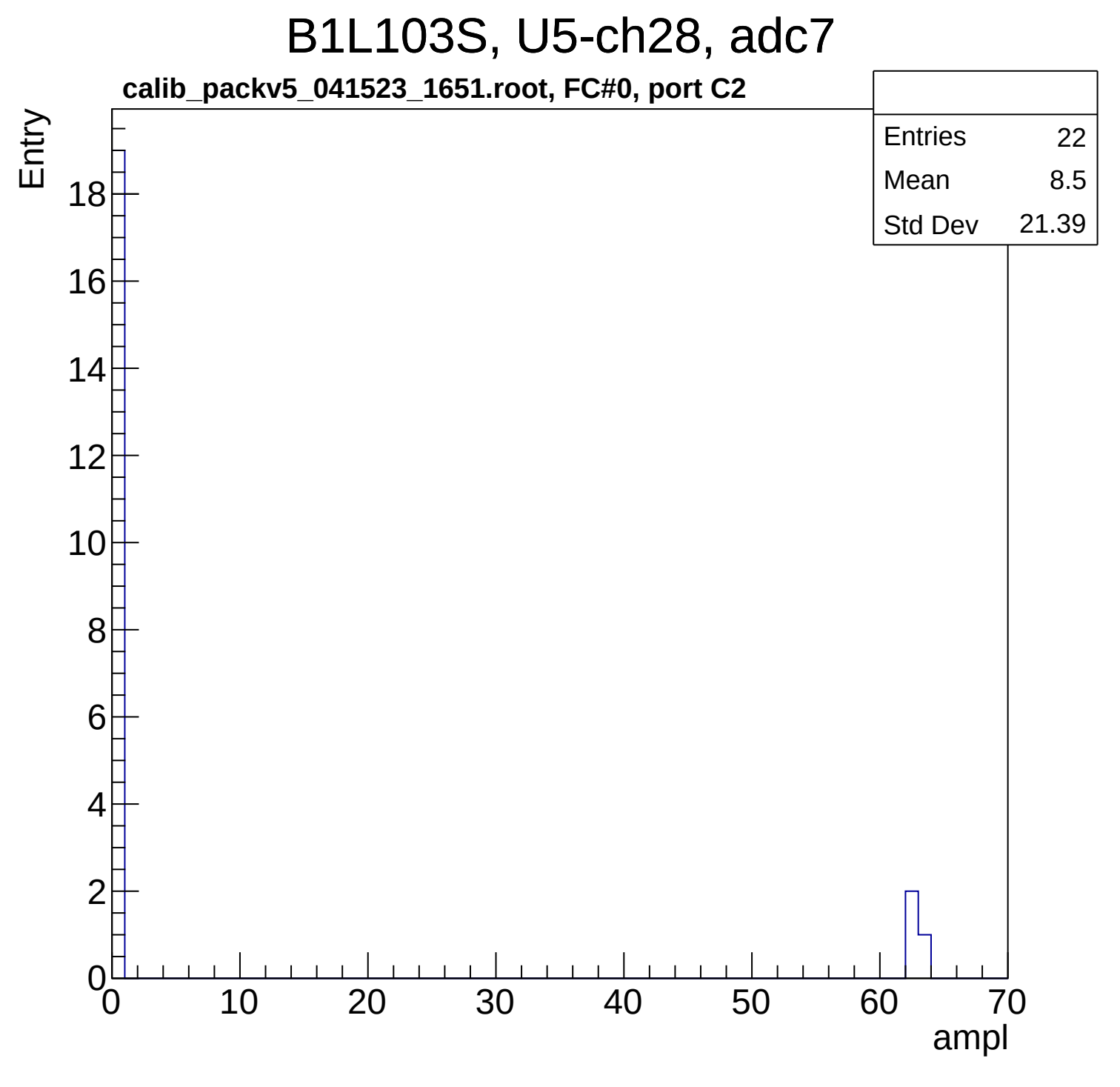
B1L103S, U5-ch28, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.5
Std Dev 21.39
Entry
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6
8
10
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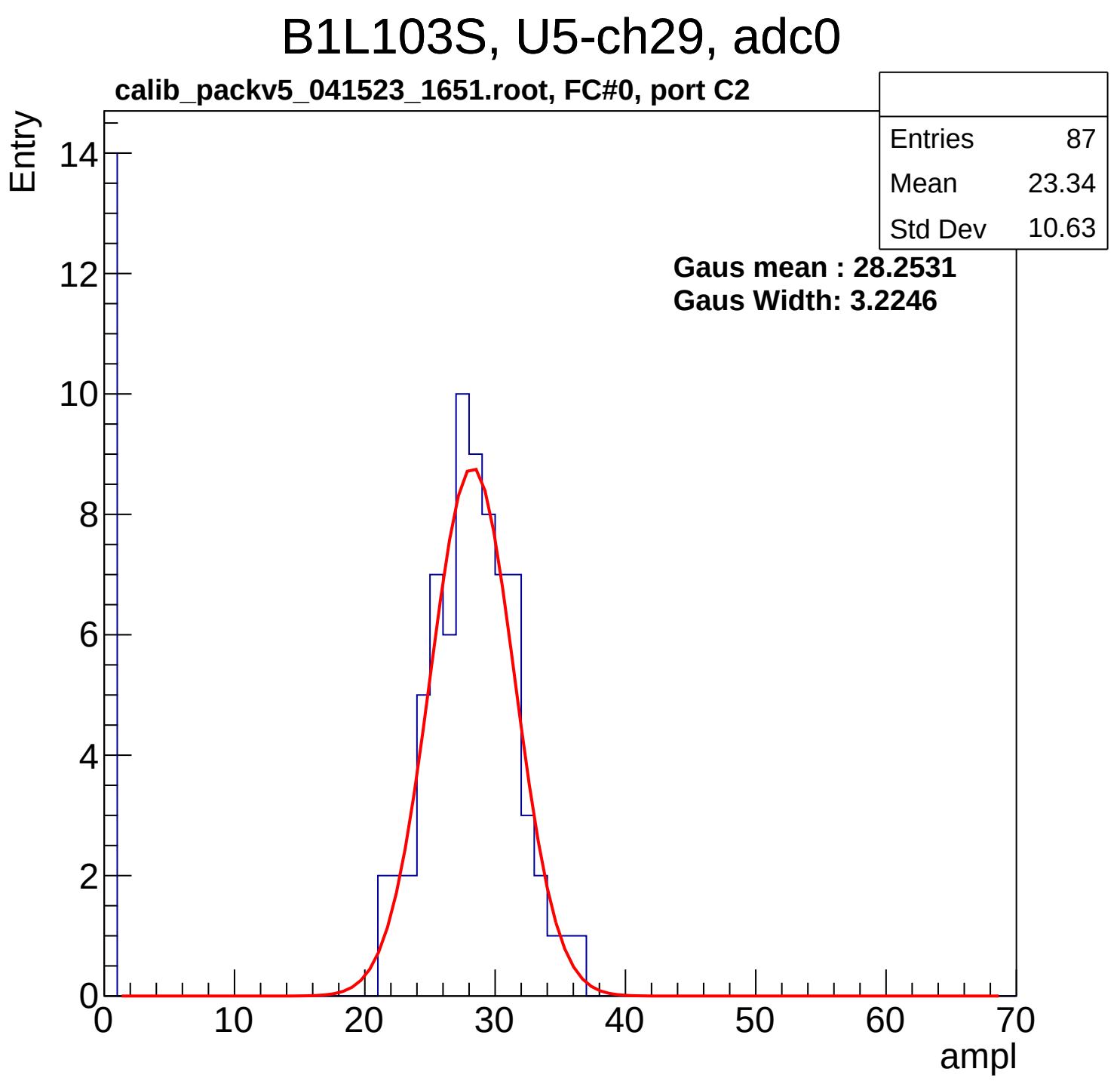
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch29, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 23.34
Std Dev 10.63
Gaus mean : 28.2531
Gaus Width: 3.2246
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
50
60
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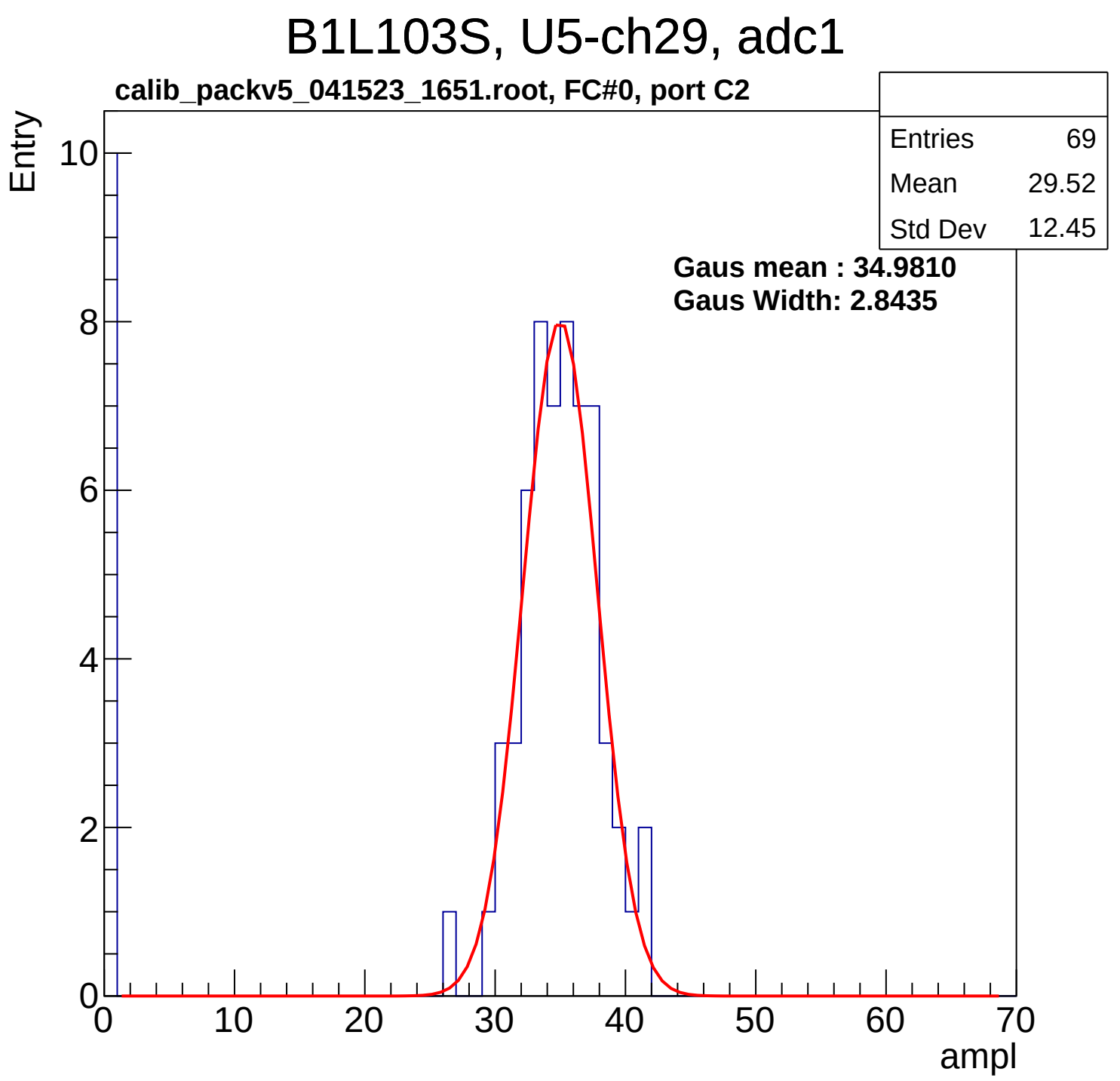
B1L103S, U5-ch29, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 29.52
Std Dev 12.45
Gaus mean : 34.9810
Gaus Width: 2.8435
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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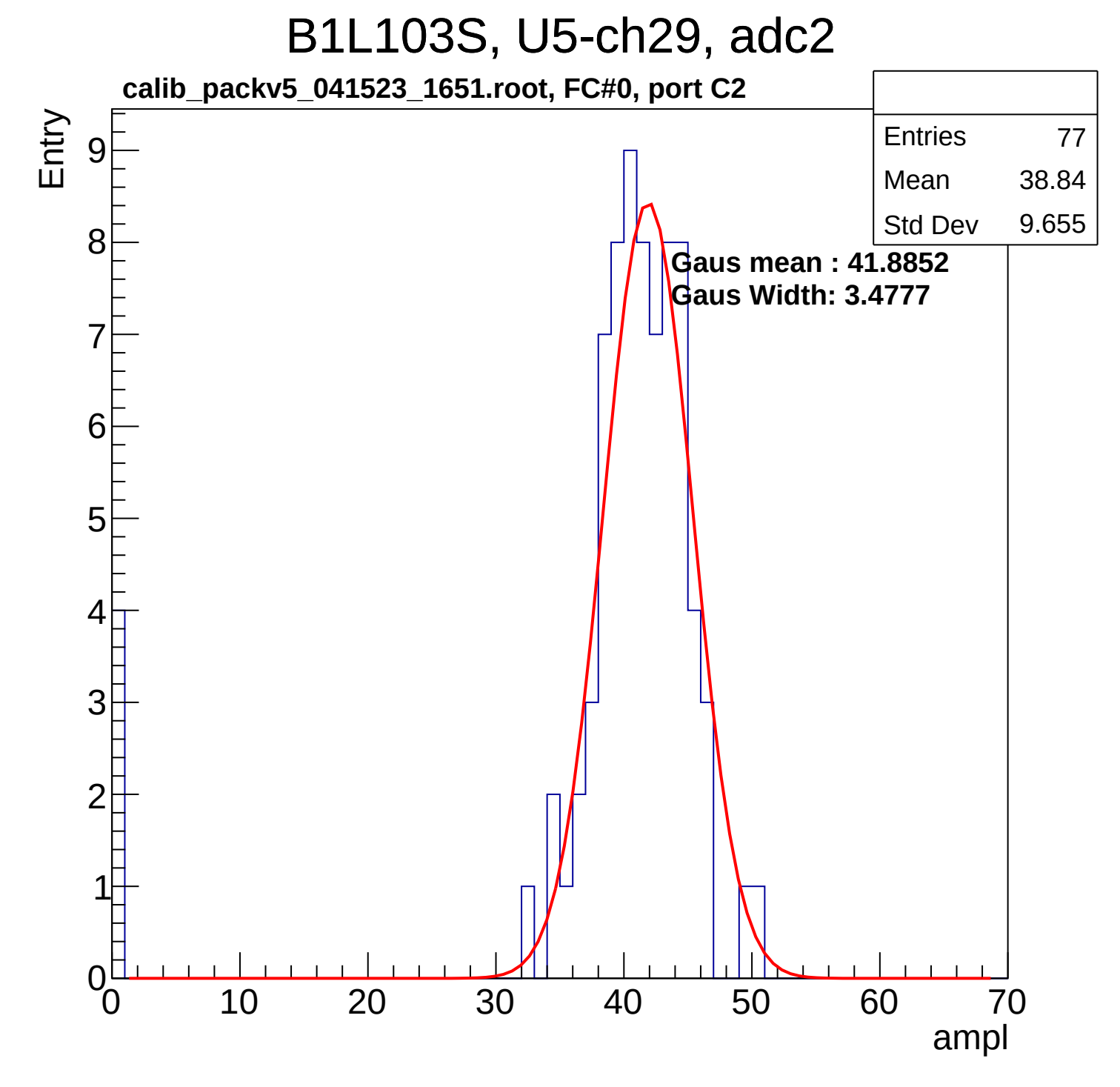
B1L103S, U5-ch29, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 38.84
Std Dev 9.655
Gaus mean : 41.8852
Gaus Width: 3.4777
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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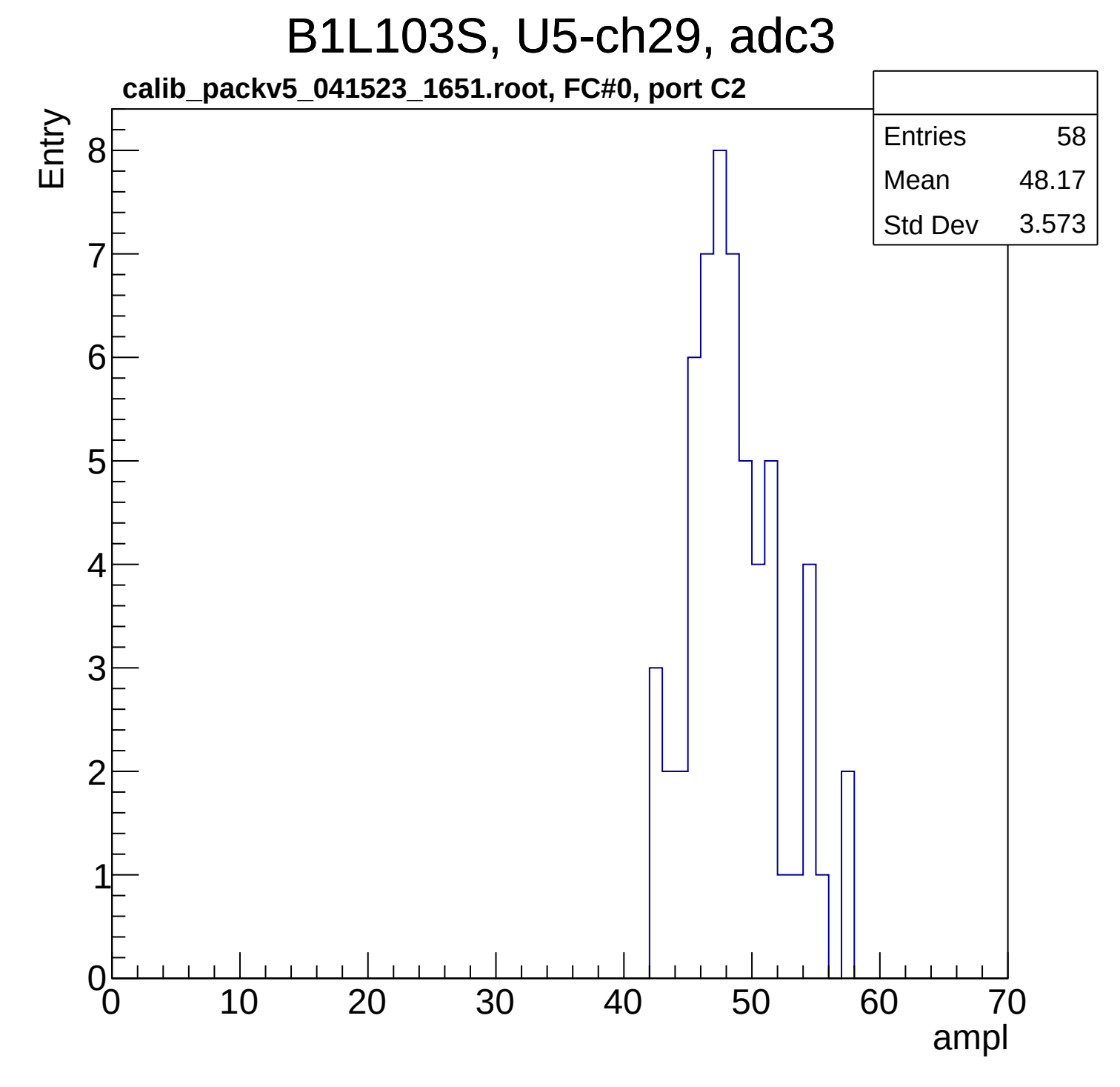
B1L103S, U5-ch29, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 48.17
Std Dev 3.573
Entry
ampl
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6
7
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0
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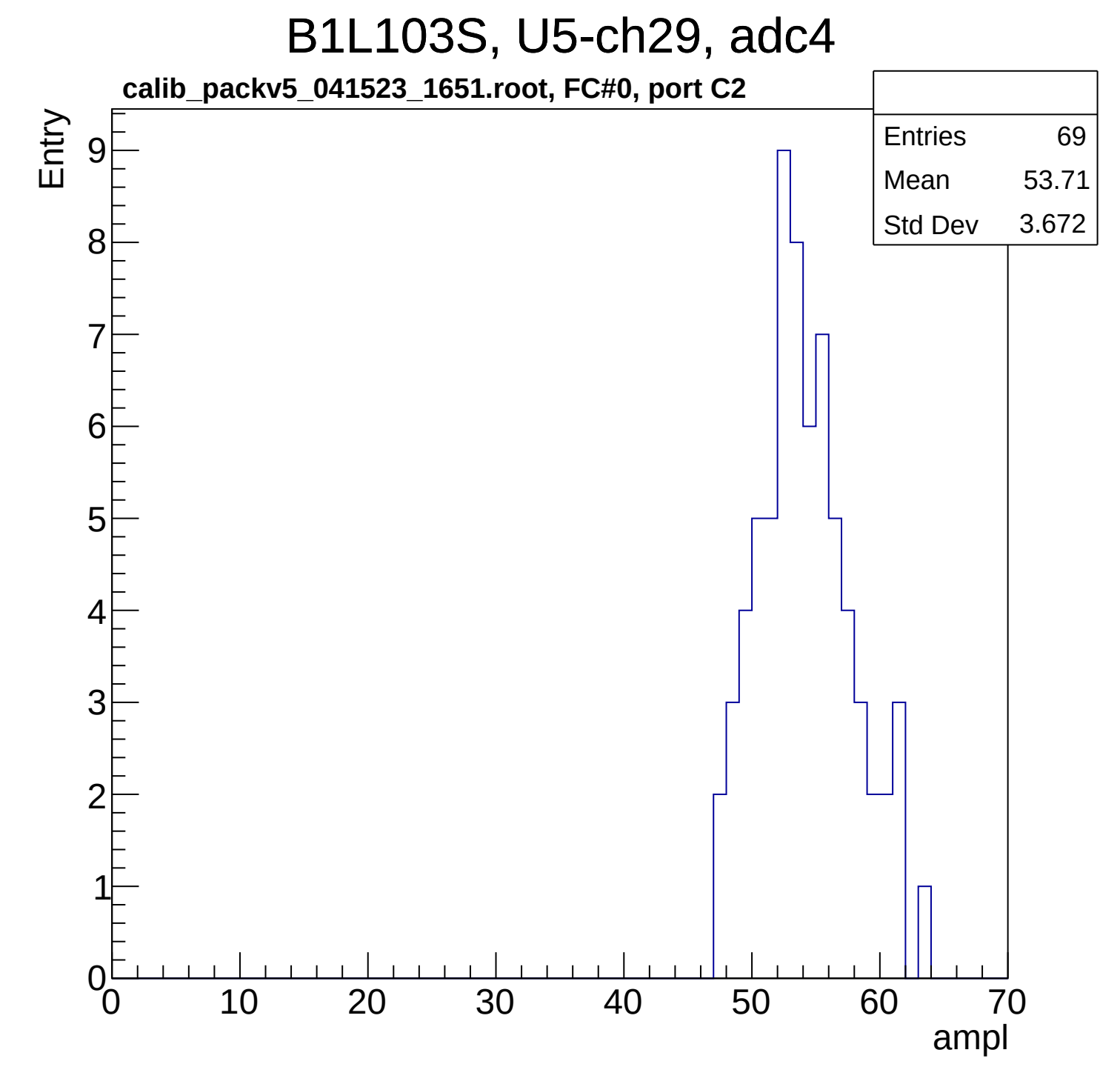
B1L103S, U5-ch29, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 53.71
Std Dev 3.672
Entry
ampl
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0
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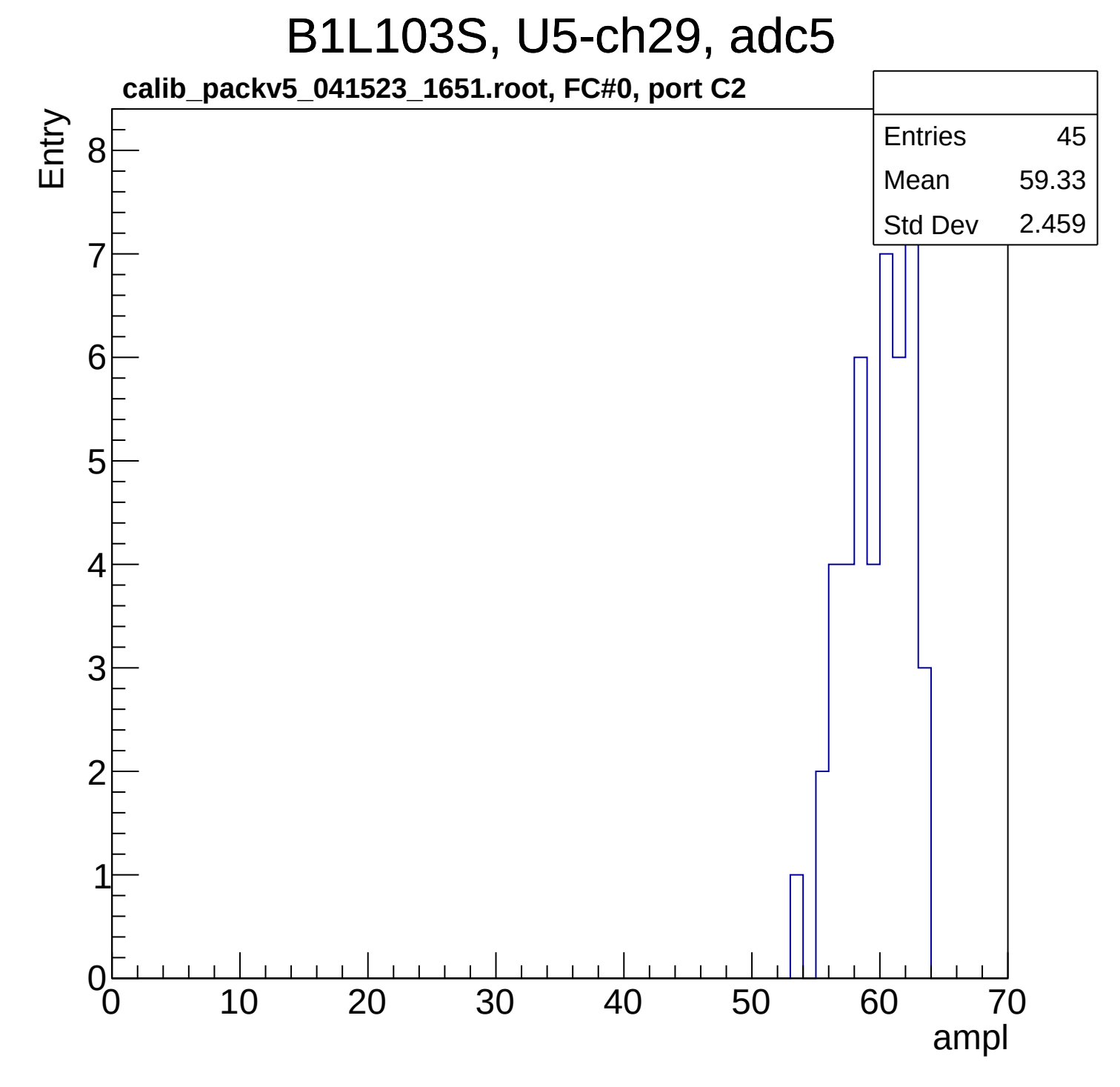
B1L103S, U5-ch29, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 59.33
Std Dev 2.459
Entry
ampl
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0
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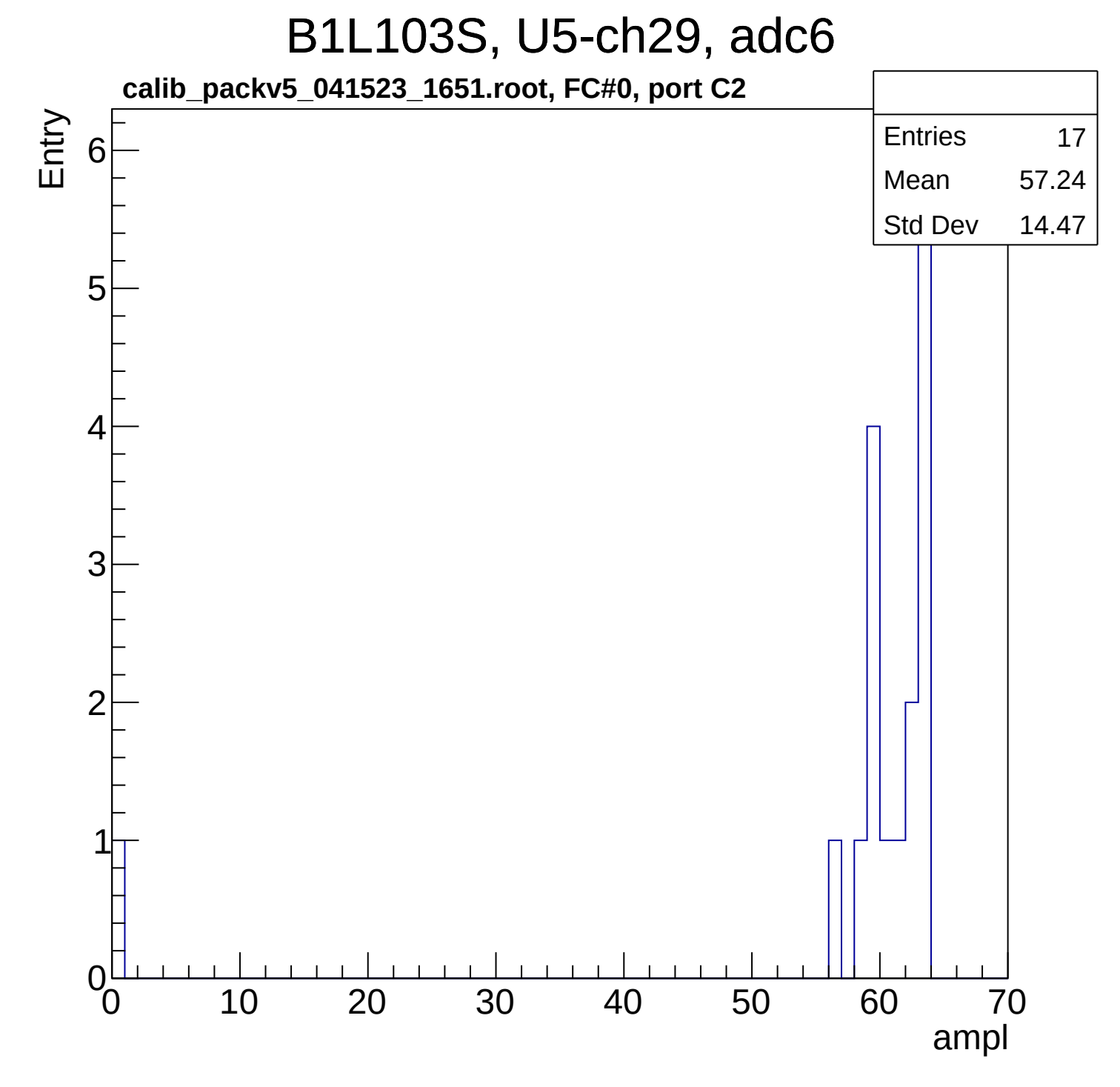
B1L103S, U5-ch29, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 57.24
Std Dev 14.47
Entry
ampl
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0
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40
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60
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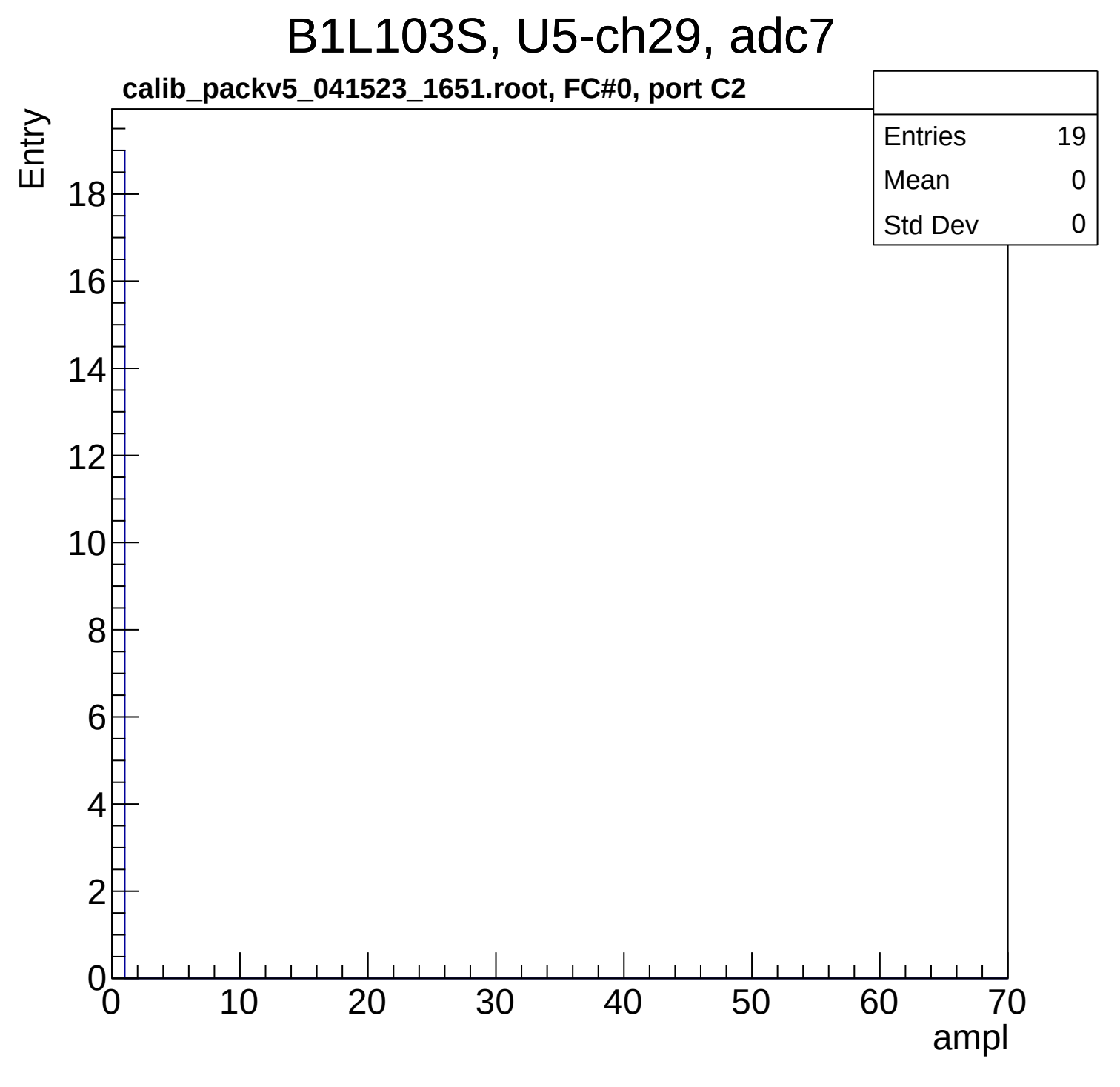
B1L103S, U5-ch29, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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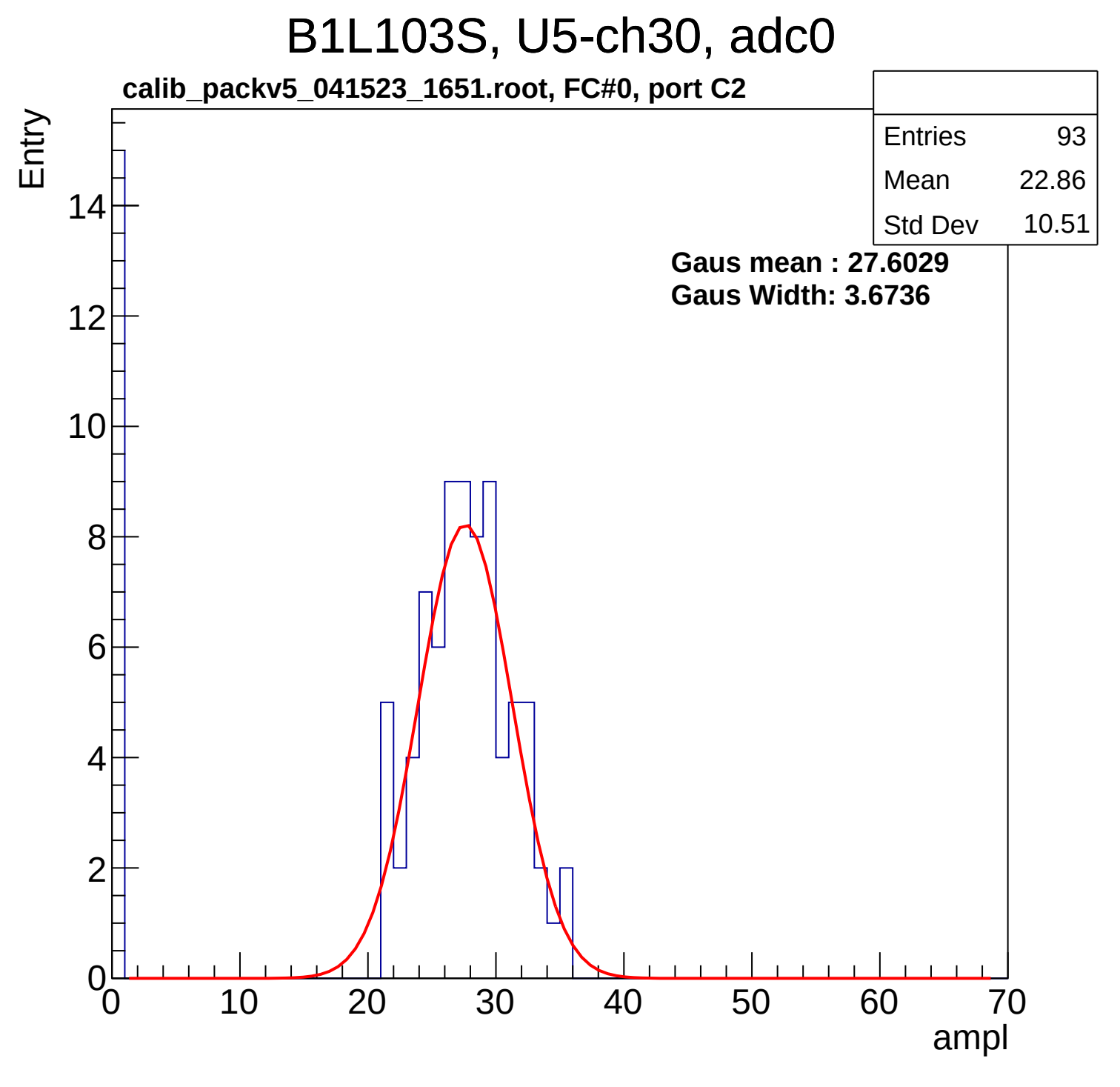
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch30, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 22.86
Std Dev 10.51
Gaus mean : 27.6029
Gaus Width: 3.6736
Entry
ampl
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6
8
10
12
14
0
10
20
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40
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60
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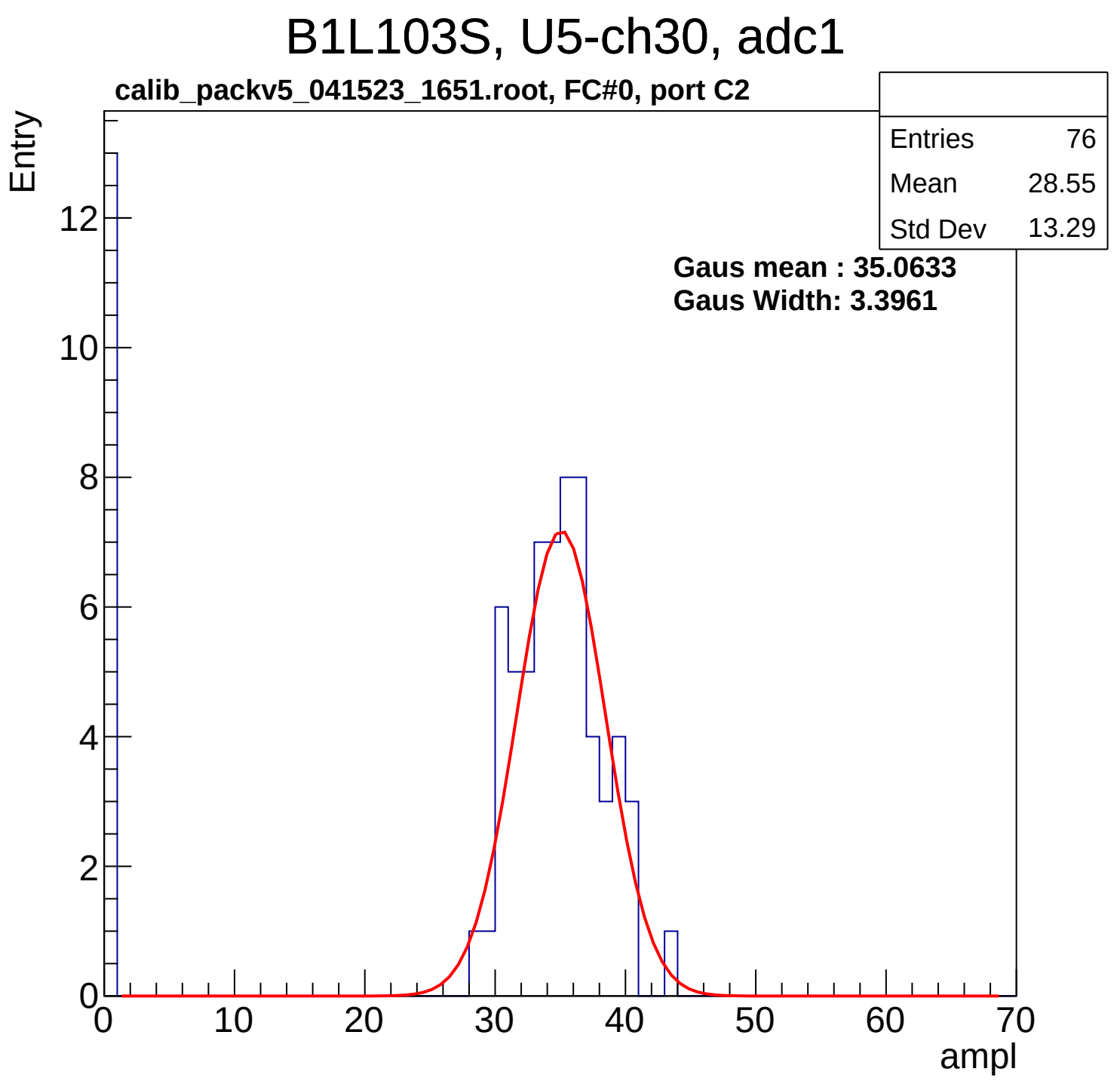
B1L103S, U5-ch30, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 28.55
Std Dev 13.29
Gaus mean : 35.0633
Gaus Width: 3.3961
Entry
ampl
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2
4
6
8
10
12
0
10
20
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40
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60
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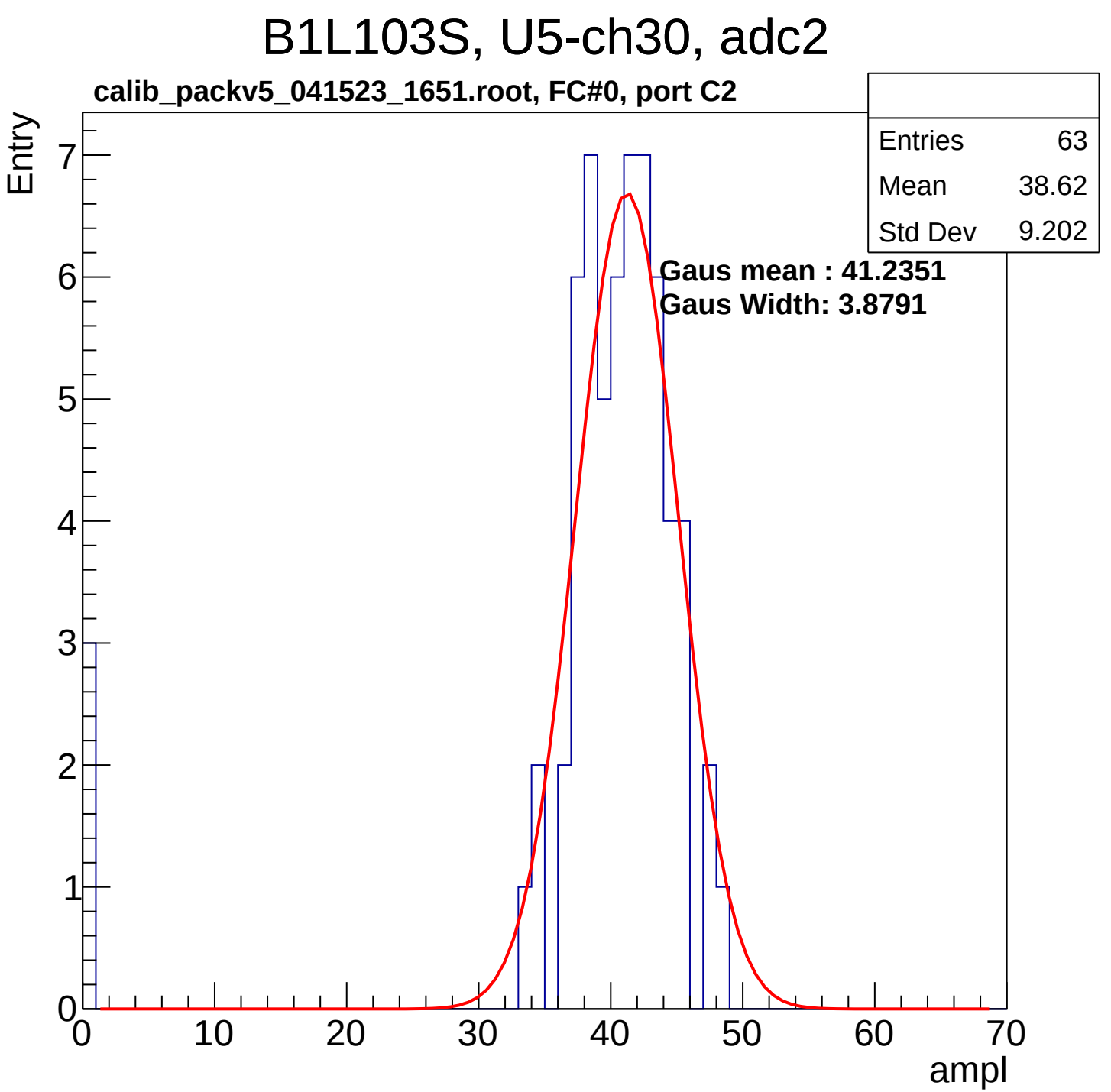
B1L103S, U5-ch30, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 38.62
Std Dev 9.202
Gaus mean : 41.2351
Gaus Width: 3.8791
Entry
ampl
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1
2
3
4
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0
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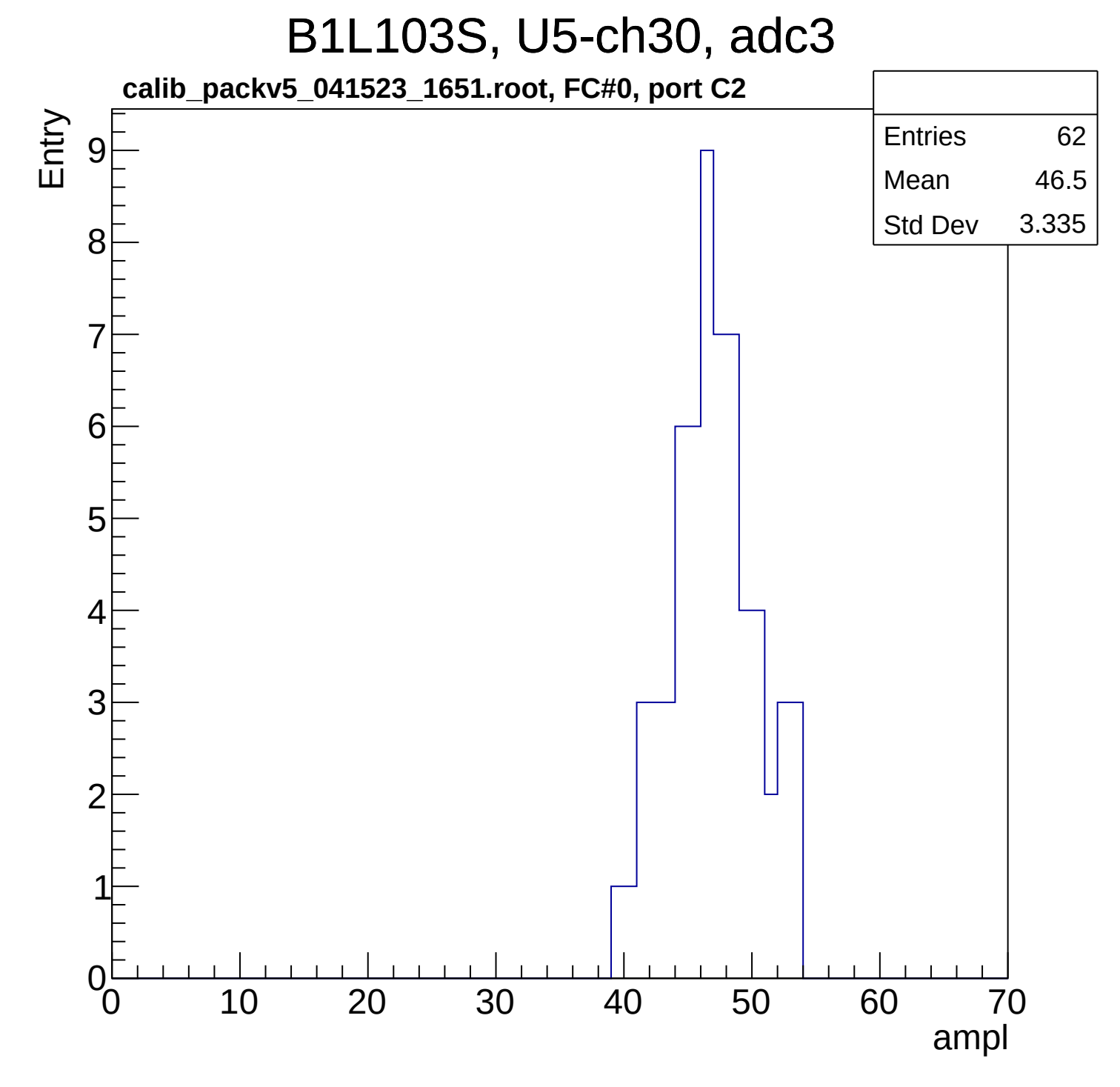
B1L103S, U5-ch30, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 46.5
Std Dev 3.335
Entry
ampl
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4
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0
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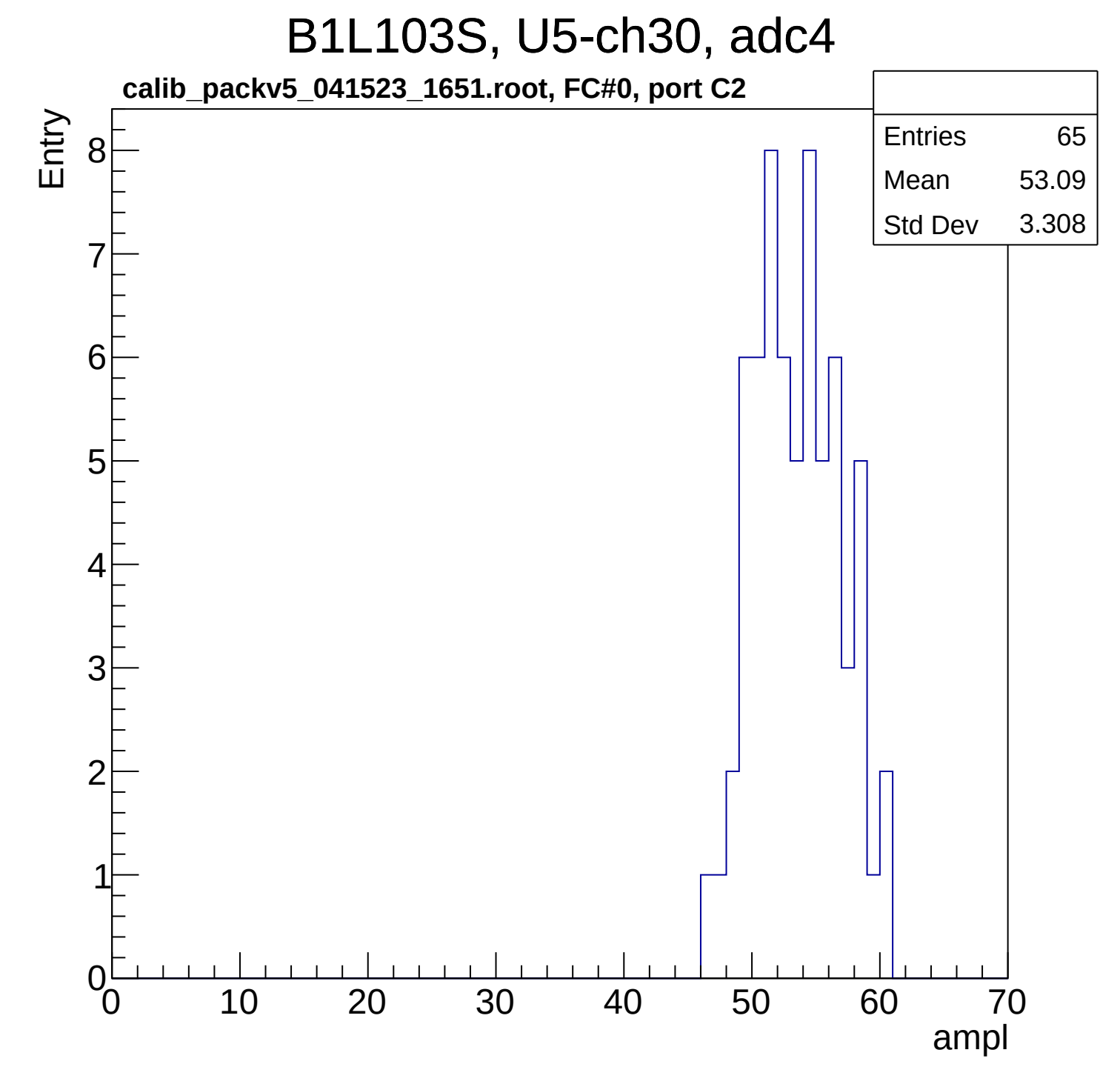
B1L103S, U5-ch30, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 53.09
Std Dev 3.308
Entry
ampl
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3
4
5
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0
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20
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60
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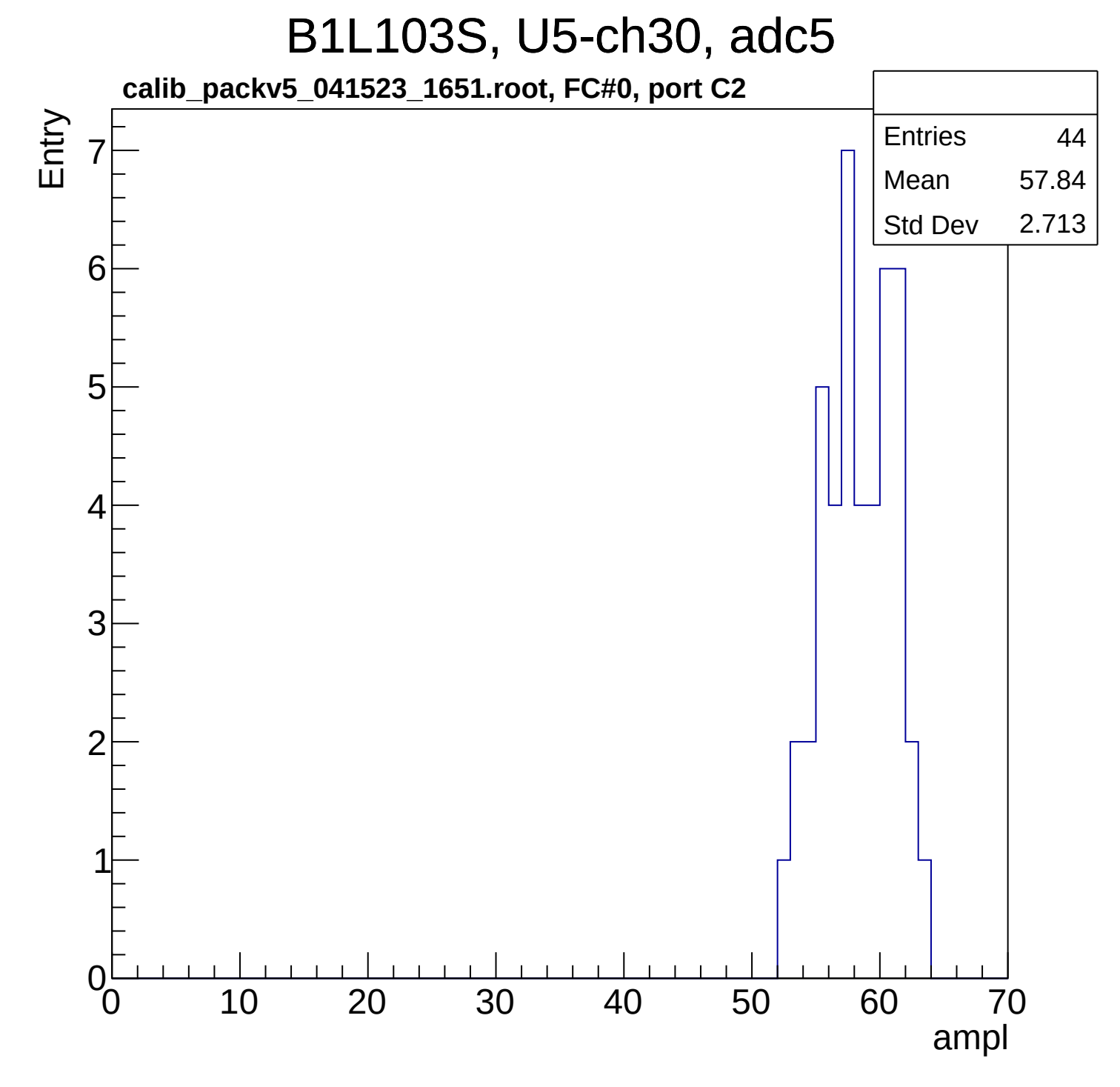
B1L103S, U5-ch30, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 57.84
Std Dev 2.713
Entry
ampl
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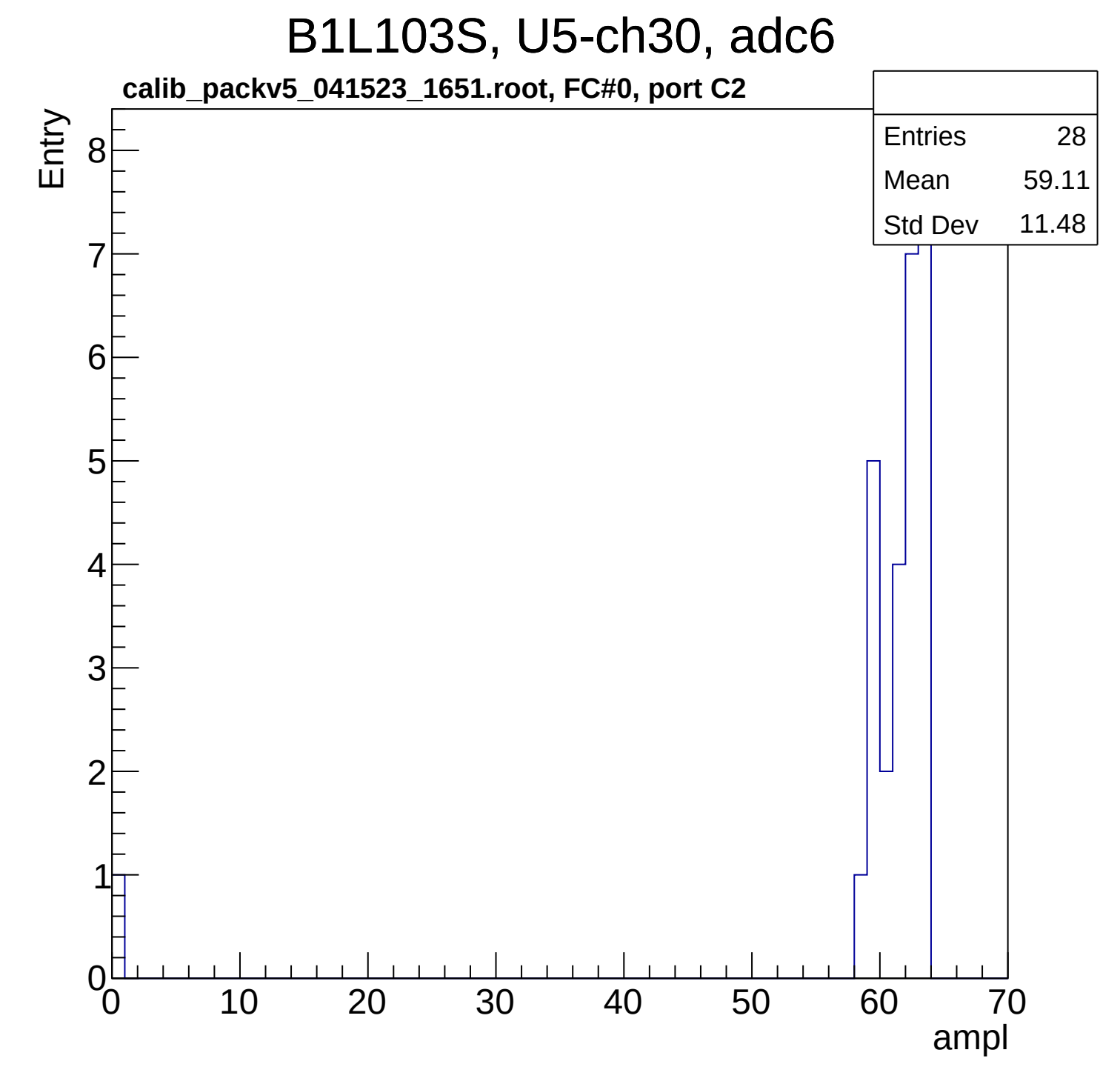
B1L103S, U5-ch30, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 59.11
Std Dev 11.48
Entry
ampl
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0
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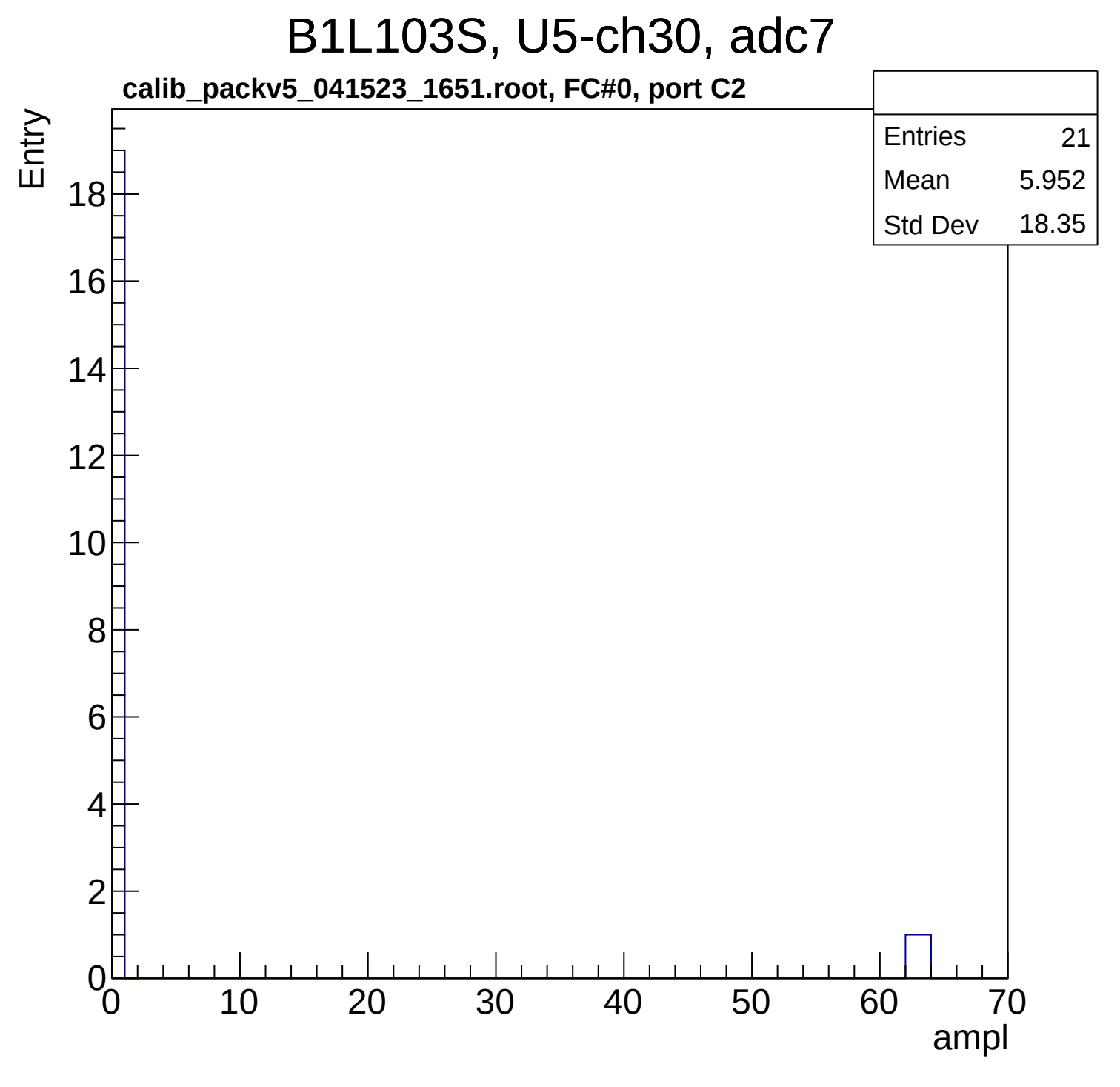
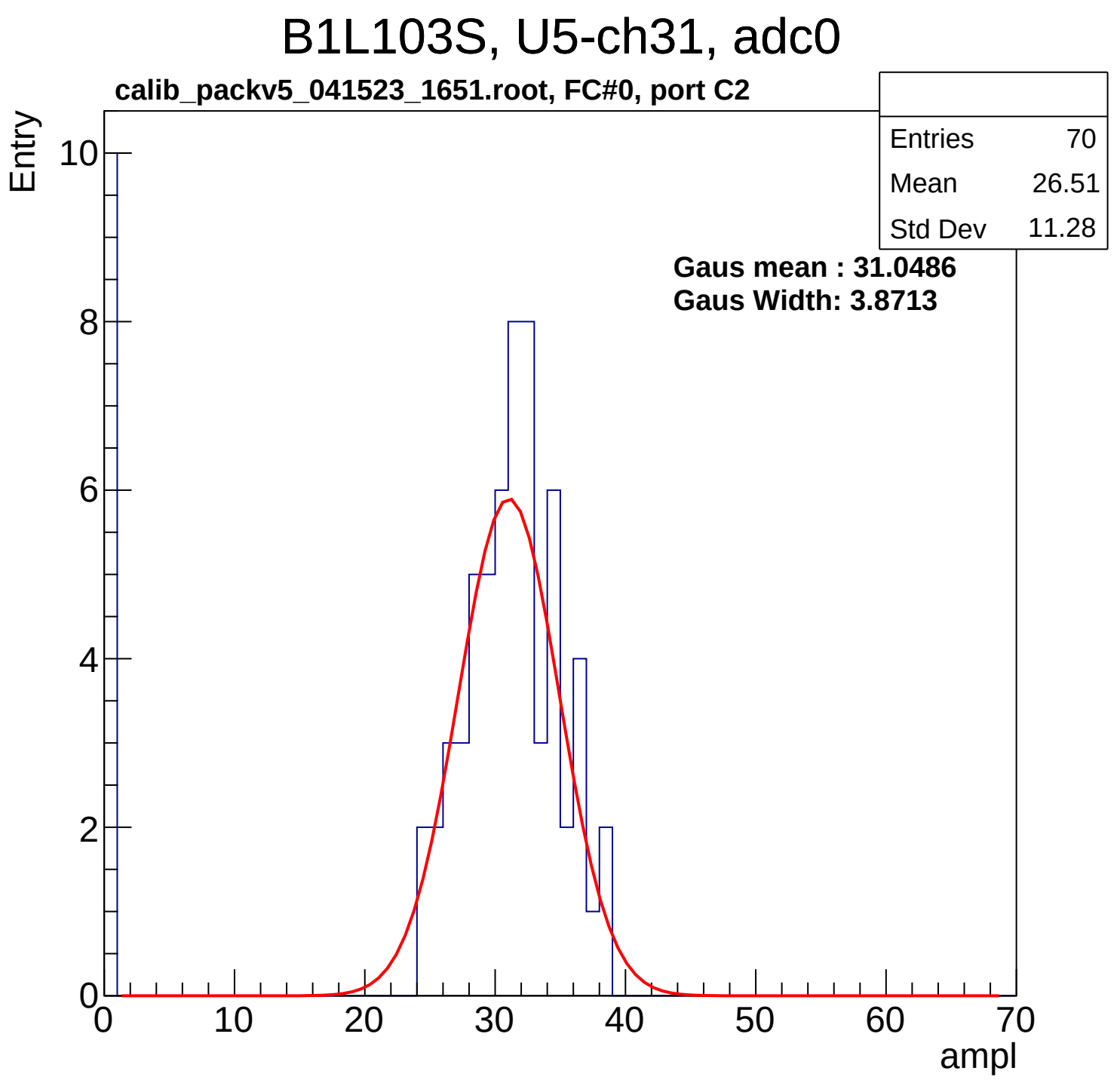

B1L103S, U5-ch30, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch31, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 26.51
Std Dev 11.28
Gaus mean : 31.0486
Gaus Width: 3.8713
Entry
ampl
0
2
4
6
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0
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60
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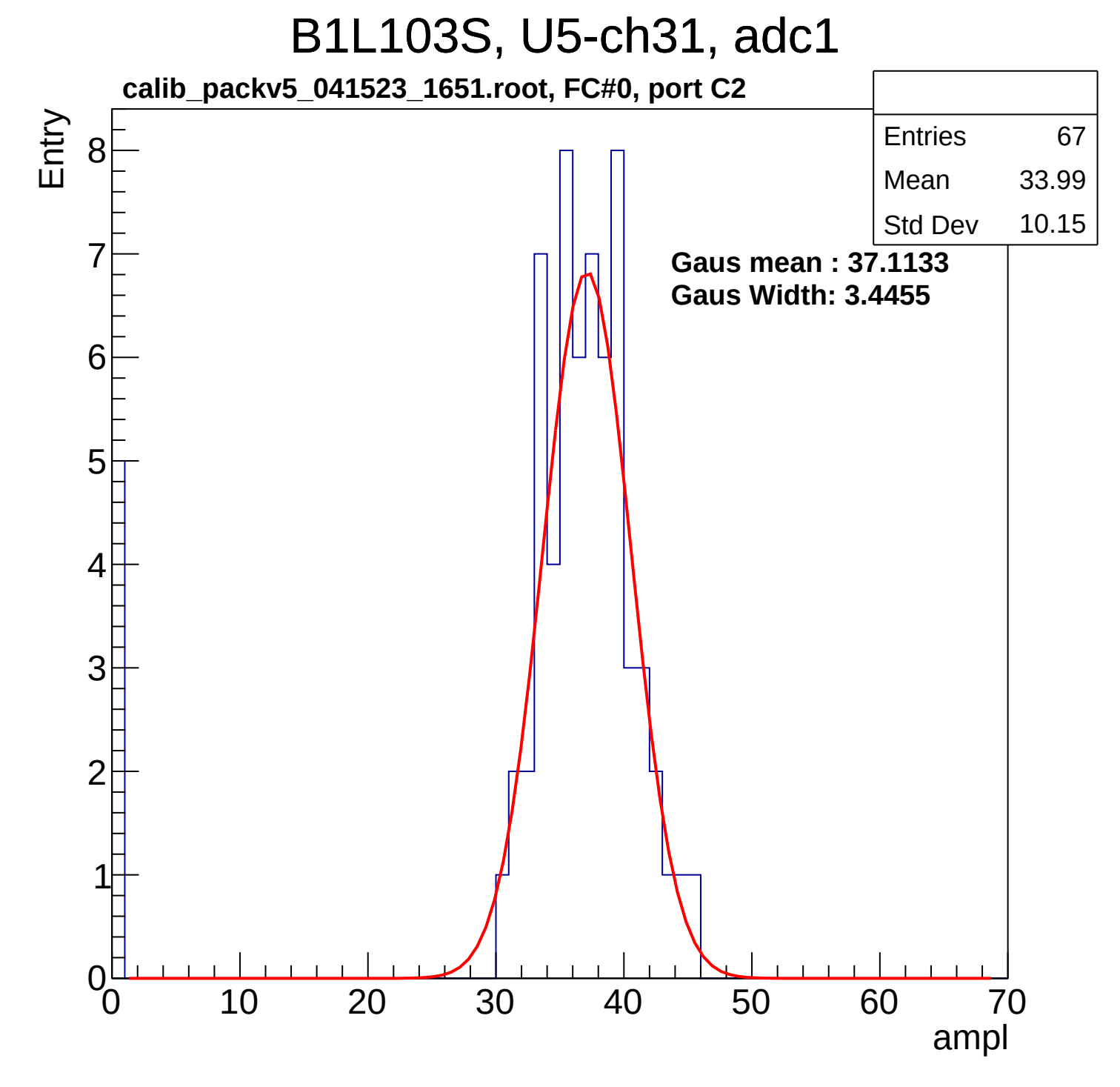
B1L103S, U5-ch31, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 33.99
Std Dev 10.15
Gaus mean : 37.1133
Gaus Width: 3.4455
Entry
ampl
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1
2
3
4
5
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7
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60
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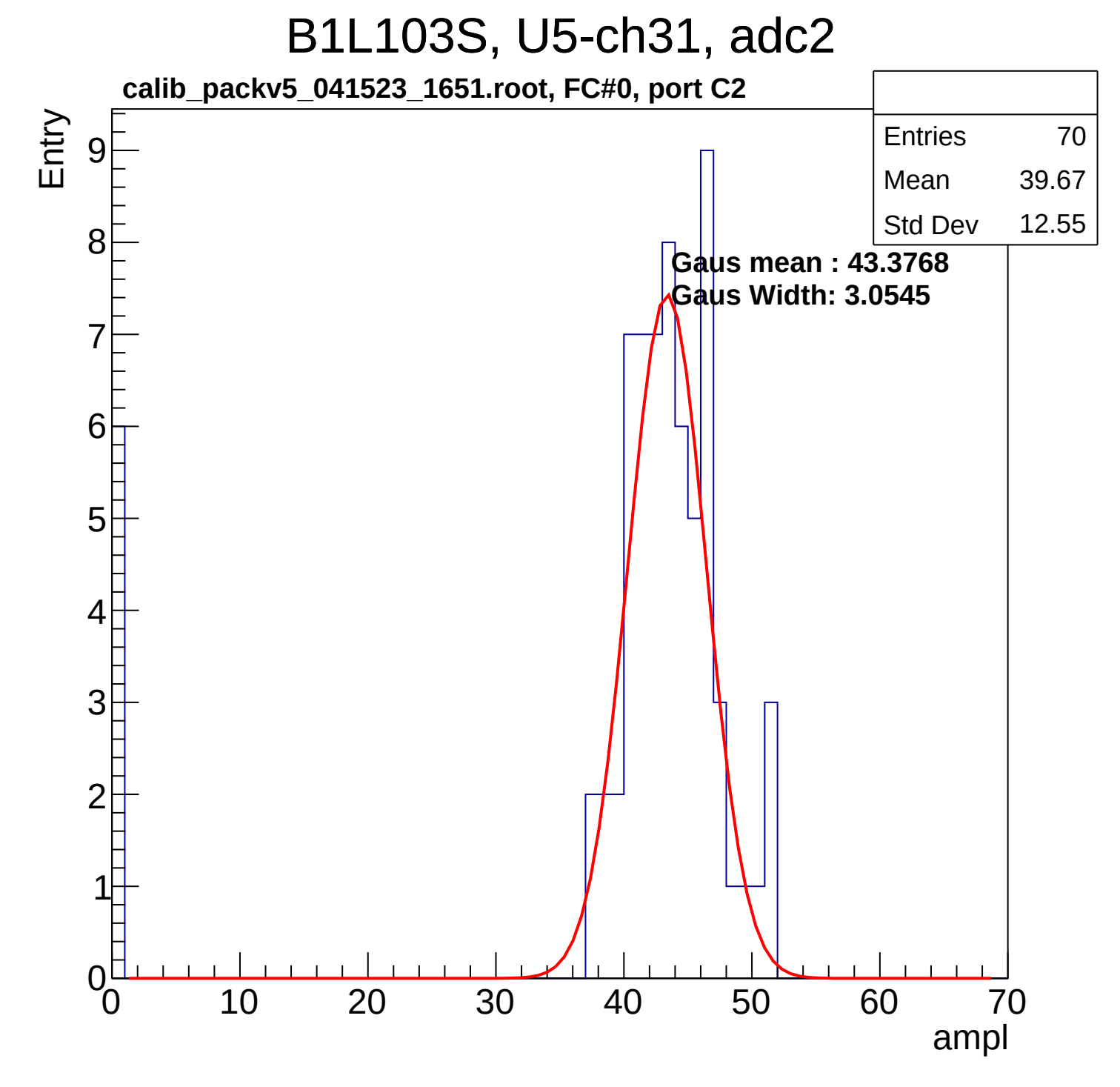
B1L103S, U5-ch31, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 39.67
Std Dev 12.55
Gaus mean : 43.3768
Gaus Width: 3.0545
Entry
ampl
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3
4
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6
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0
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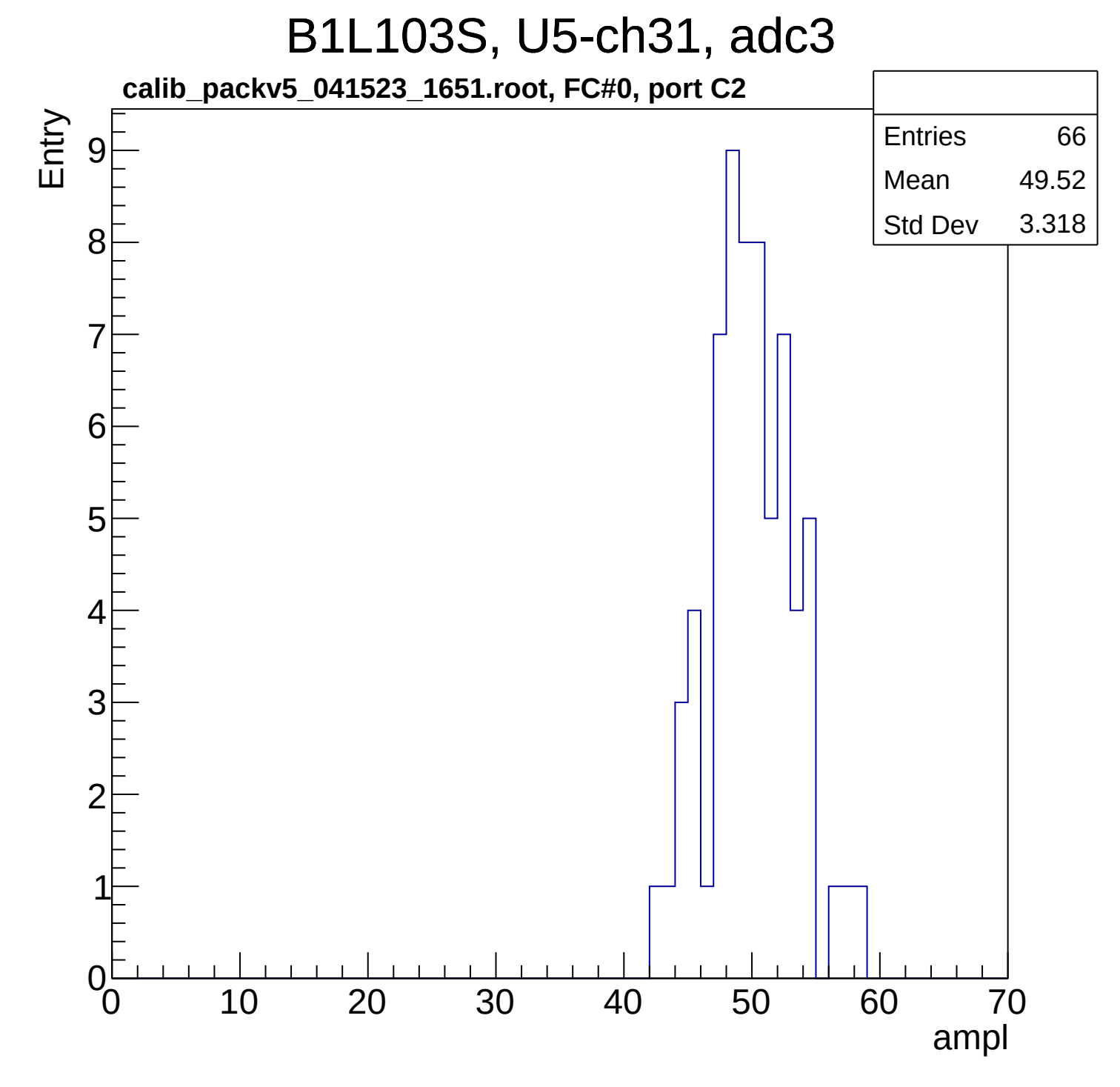
B1L103S, U5-ch31, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 49.52
Std Dev 3.318
Entry
ampl
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3
4
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6
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8
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0
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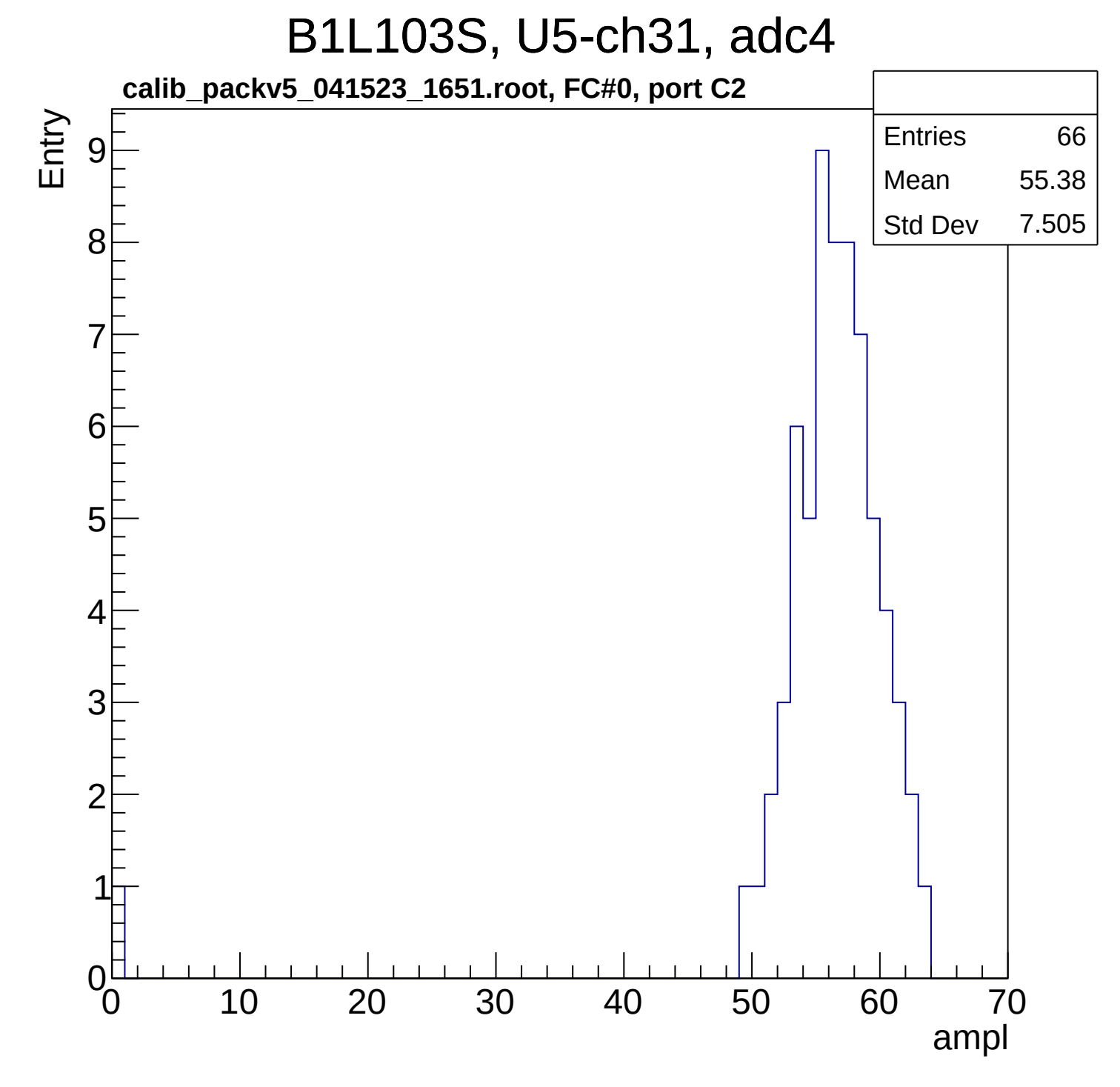
B1L103S, U5-ch31, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 55.38
Std Dev 7.505
Entry
ampl
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0
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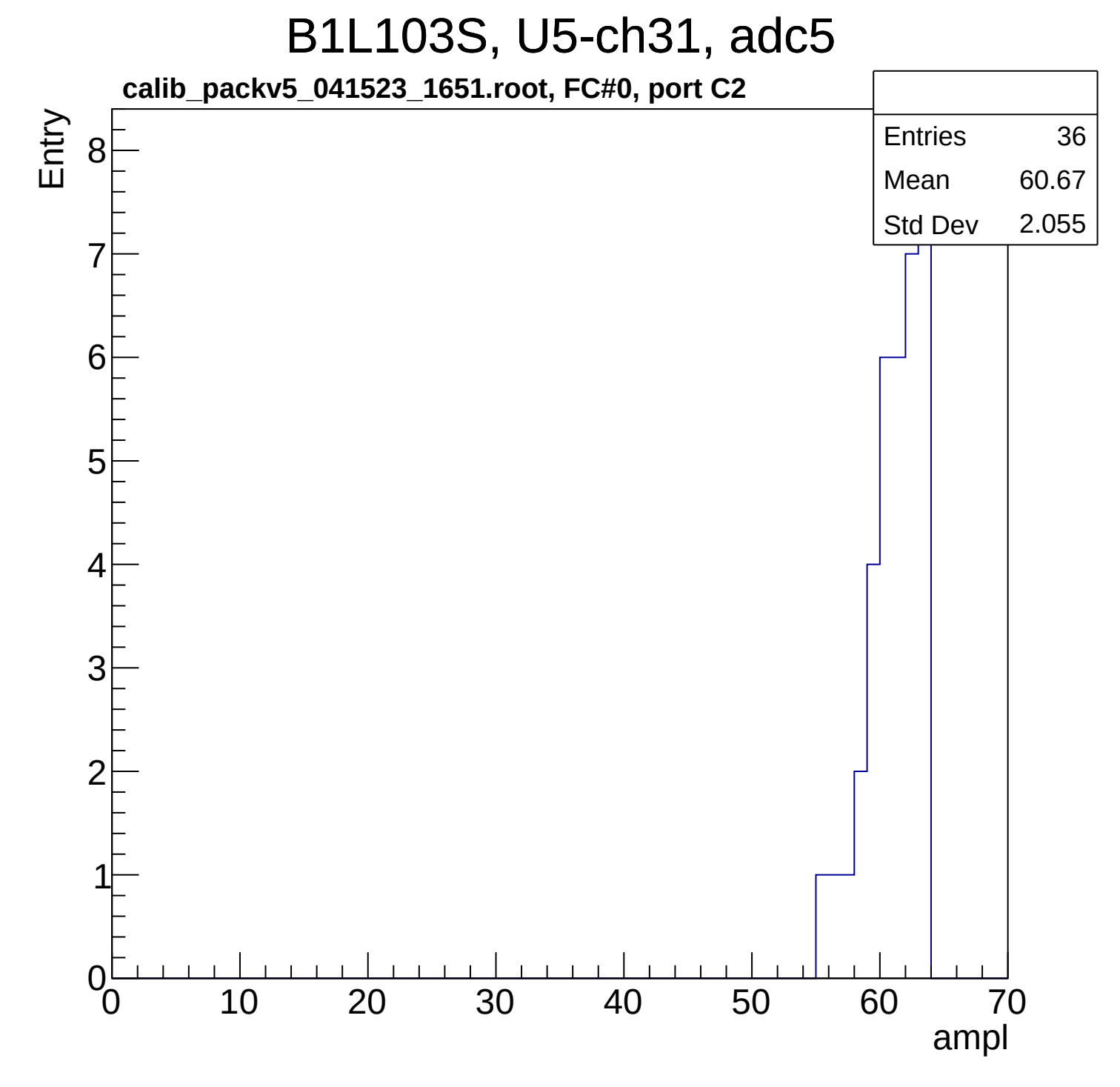
B1L103S, U5-ch31, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 60.67
Std Dev 2.055
Entry
ampl
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1
2
3
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7
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0
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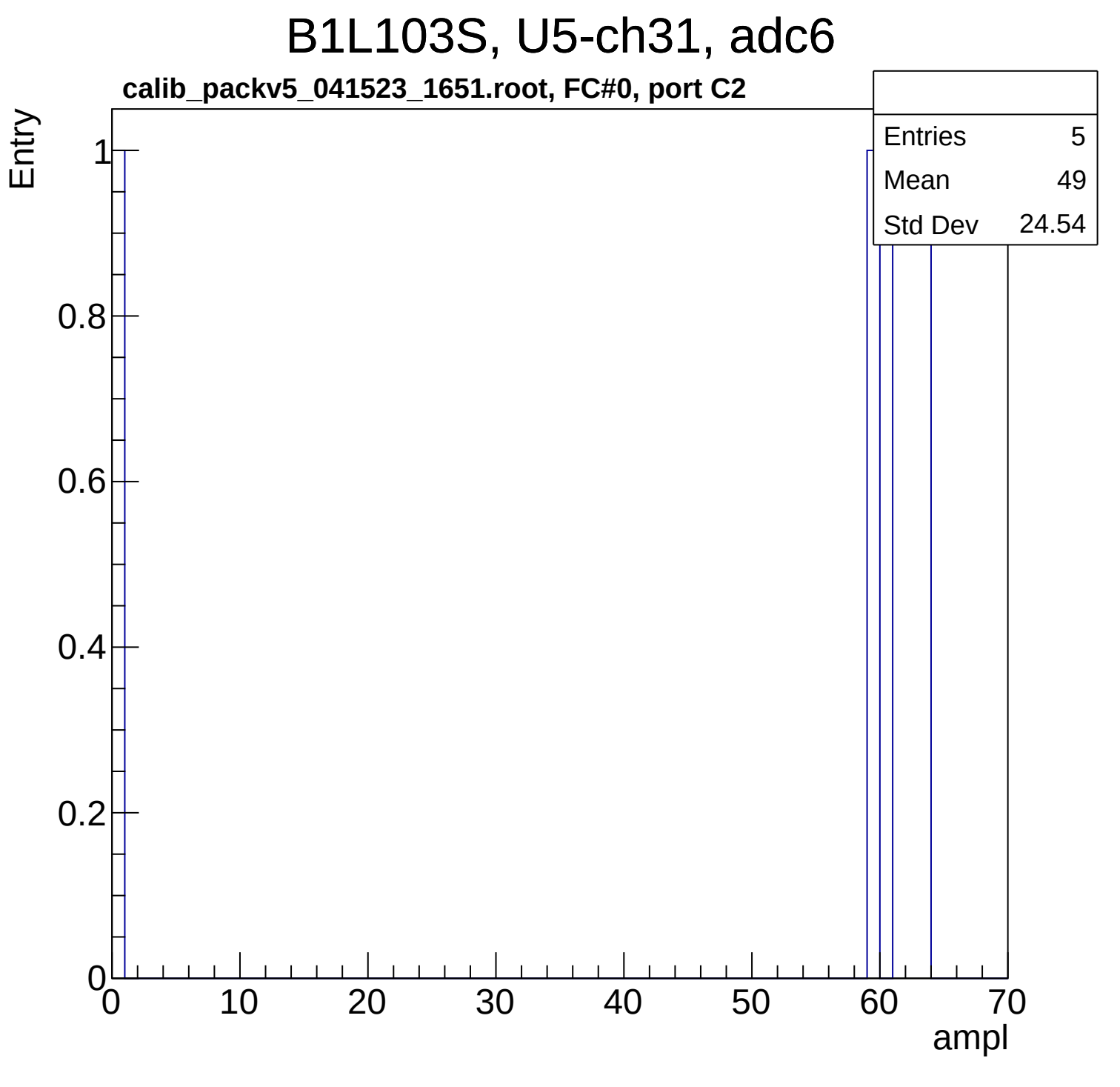
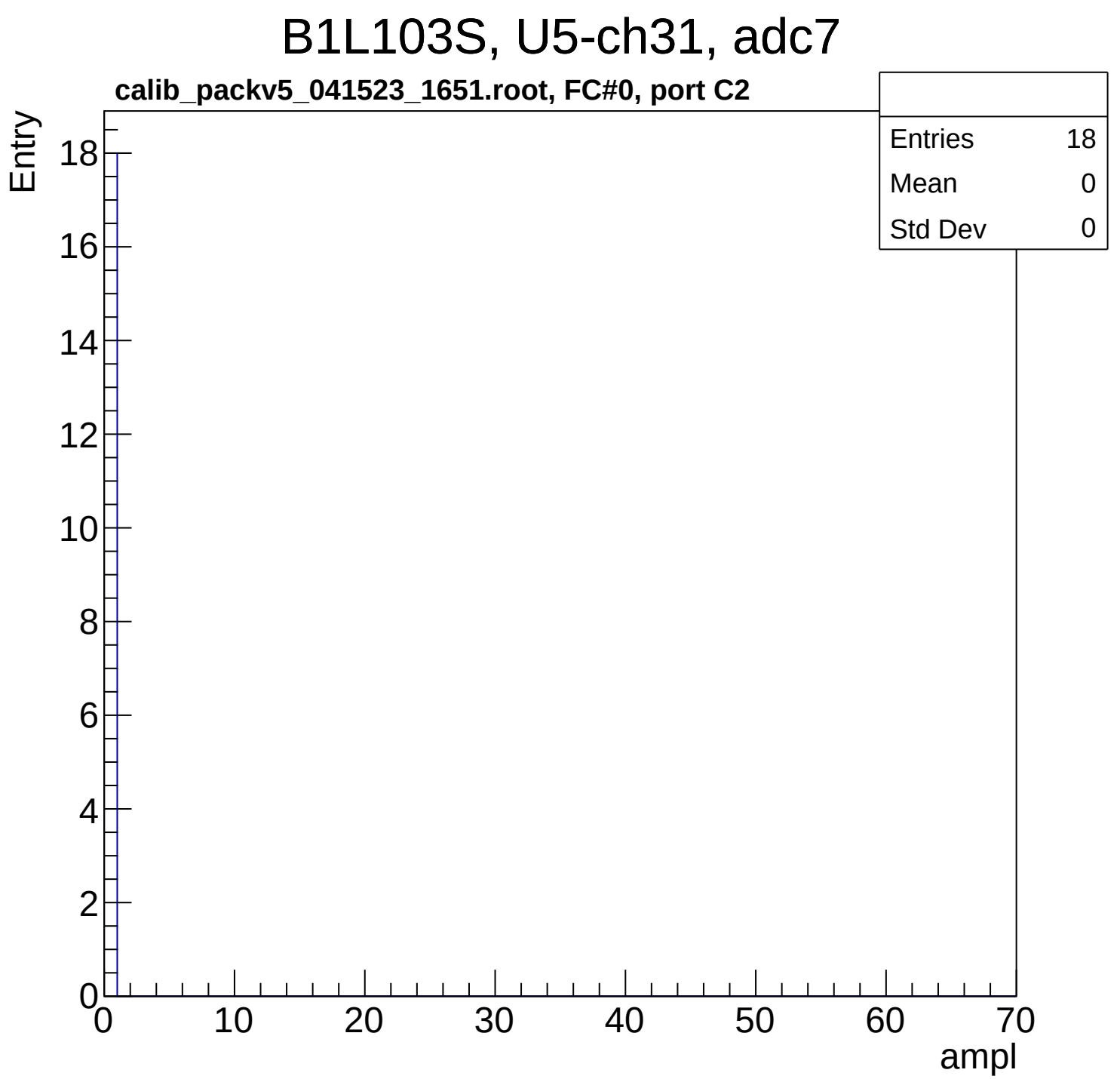
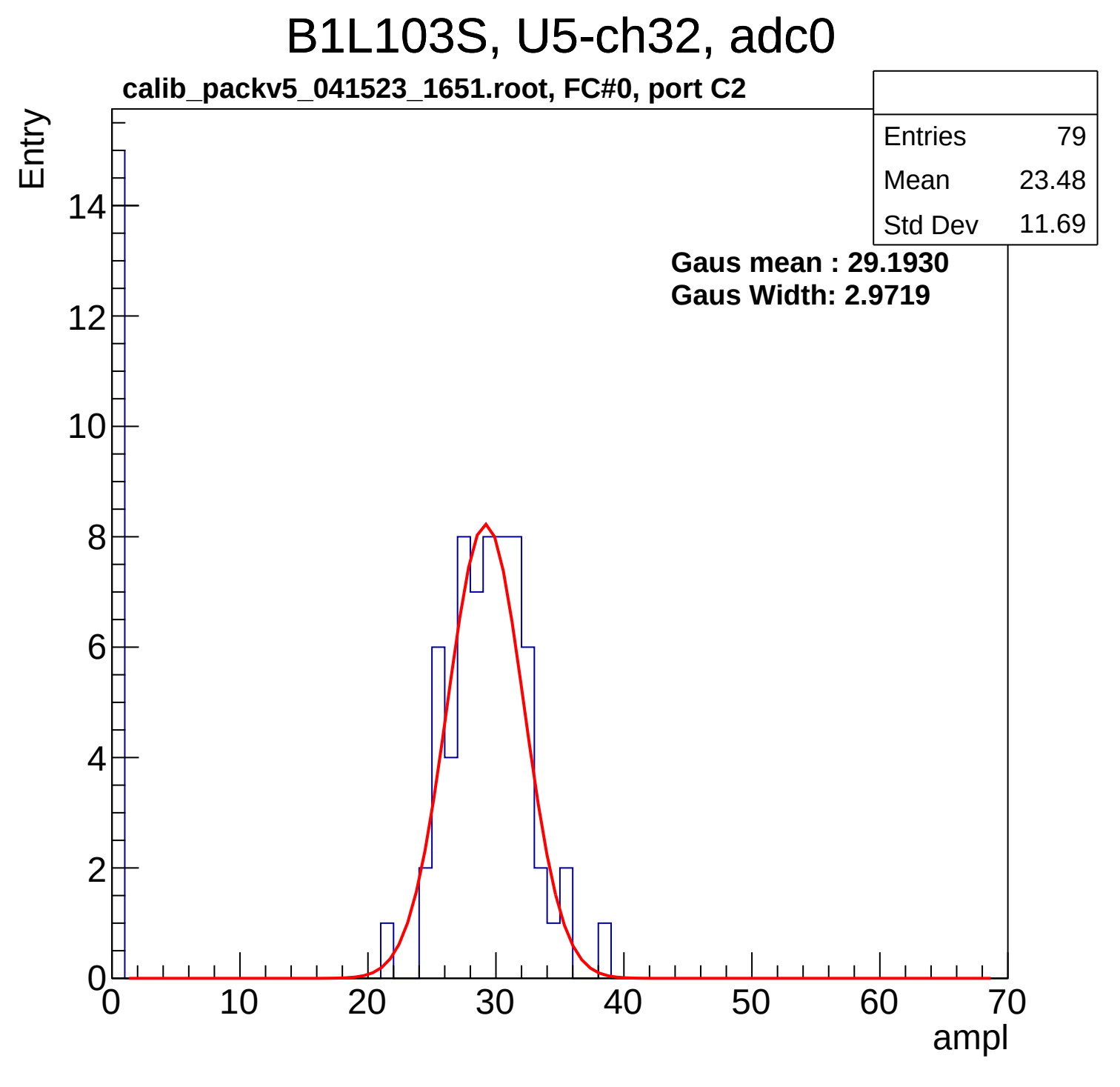
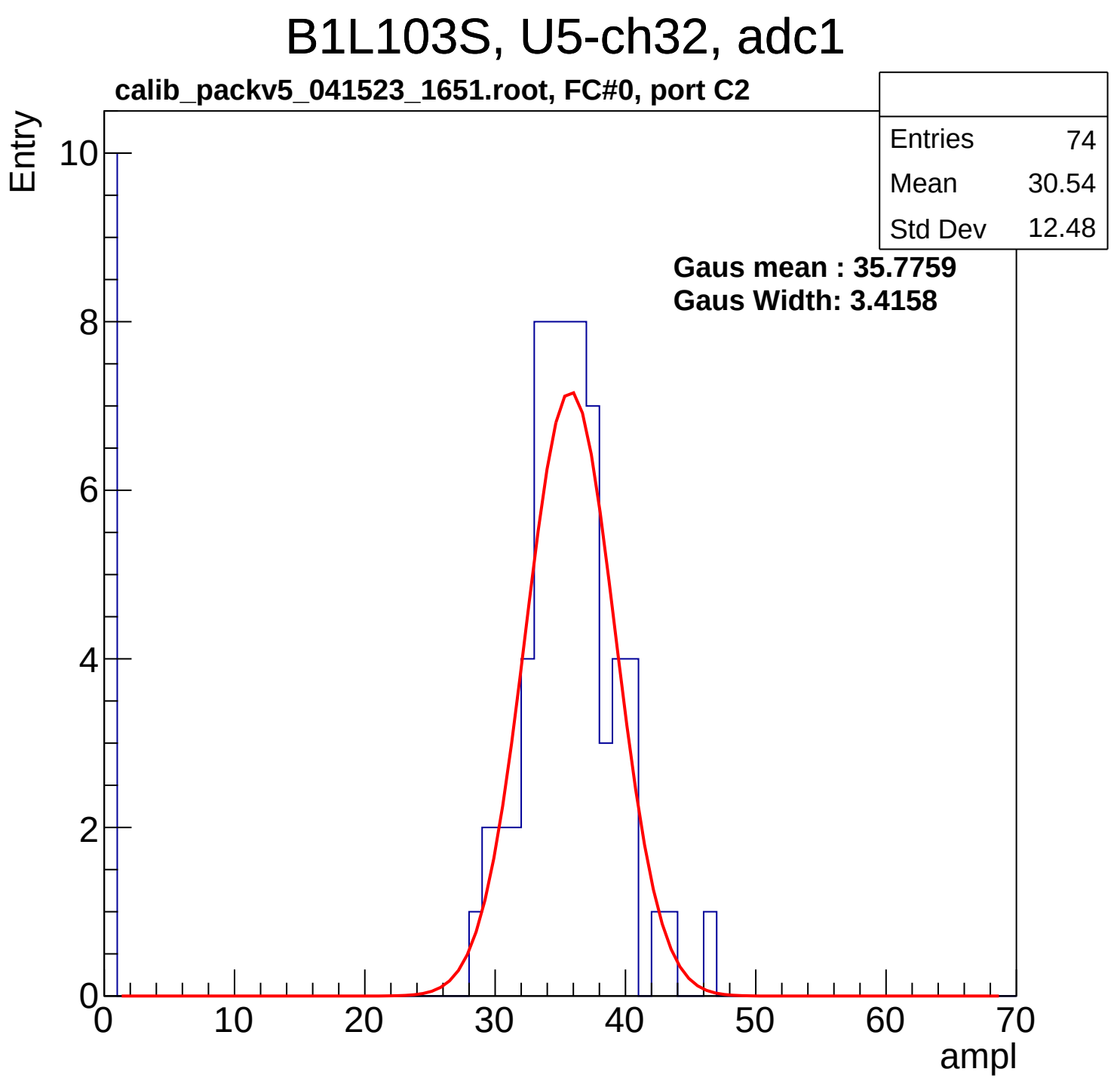

B1L103S, U5-ch31, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 49
Std Dev 24.54
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L103S, U5-ch31, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch32, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 23.48
Std Dev 11.69
Gaus mean : 29.1930
Gaus Width: 2.9719
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U5-ch32, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 30.54
Std Dev 12.48
Gaus mean : 35.7759
Gaus Width: 3.4158
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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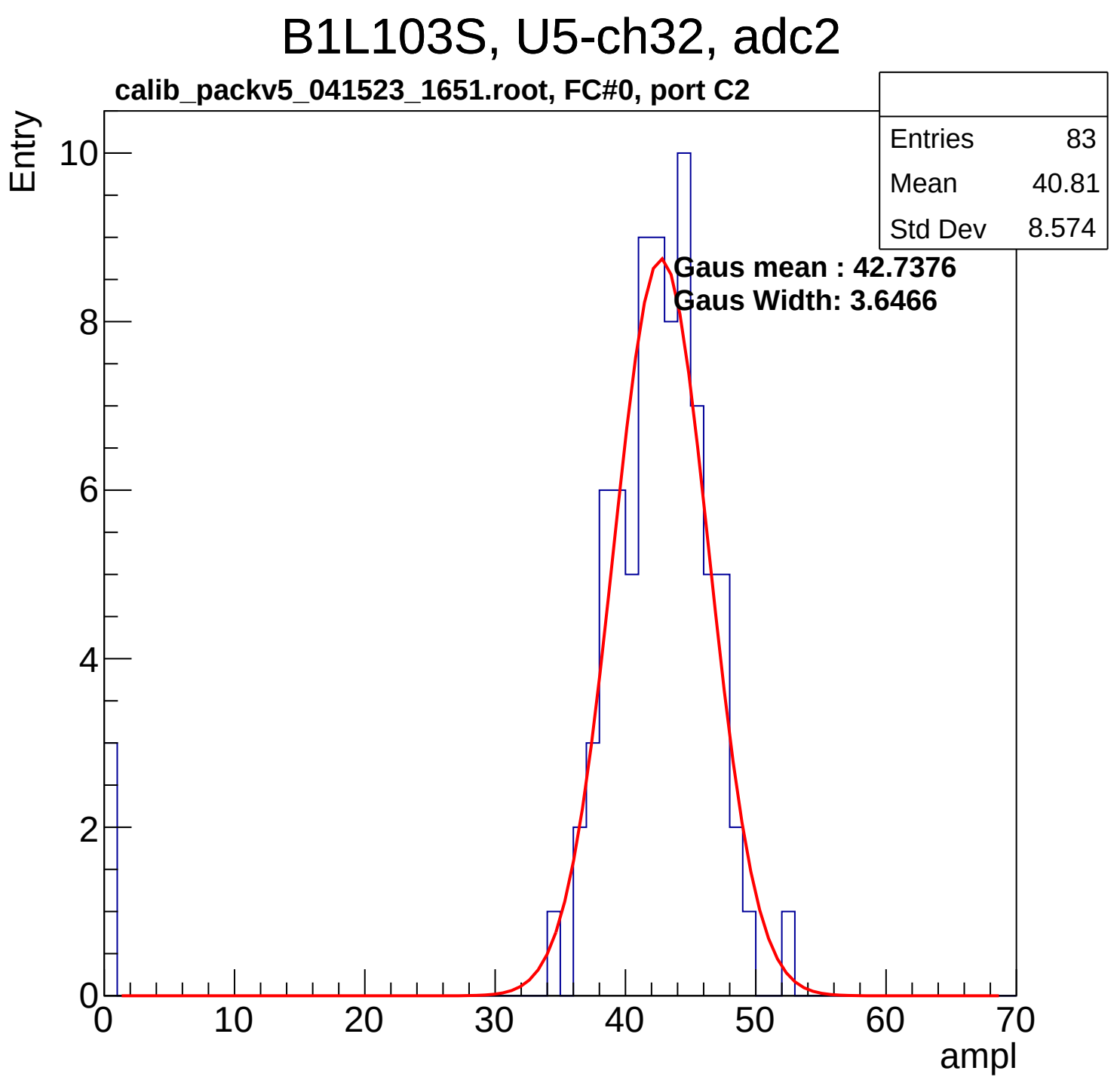
B1L103S, U5-ch32, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 40.81
Std Dev 8.574
Gaus mean : 42.7376
Gaus Width: 3.6466
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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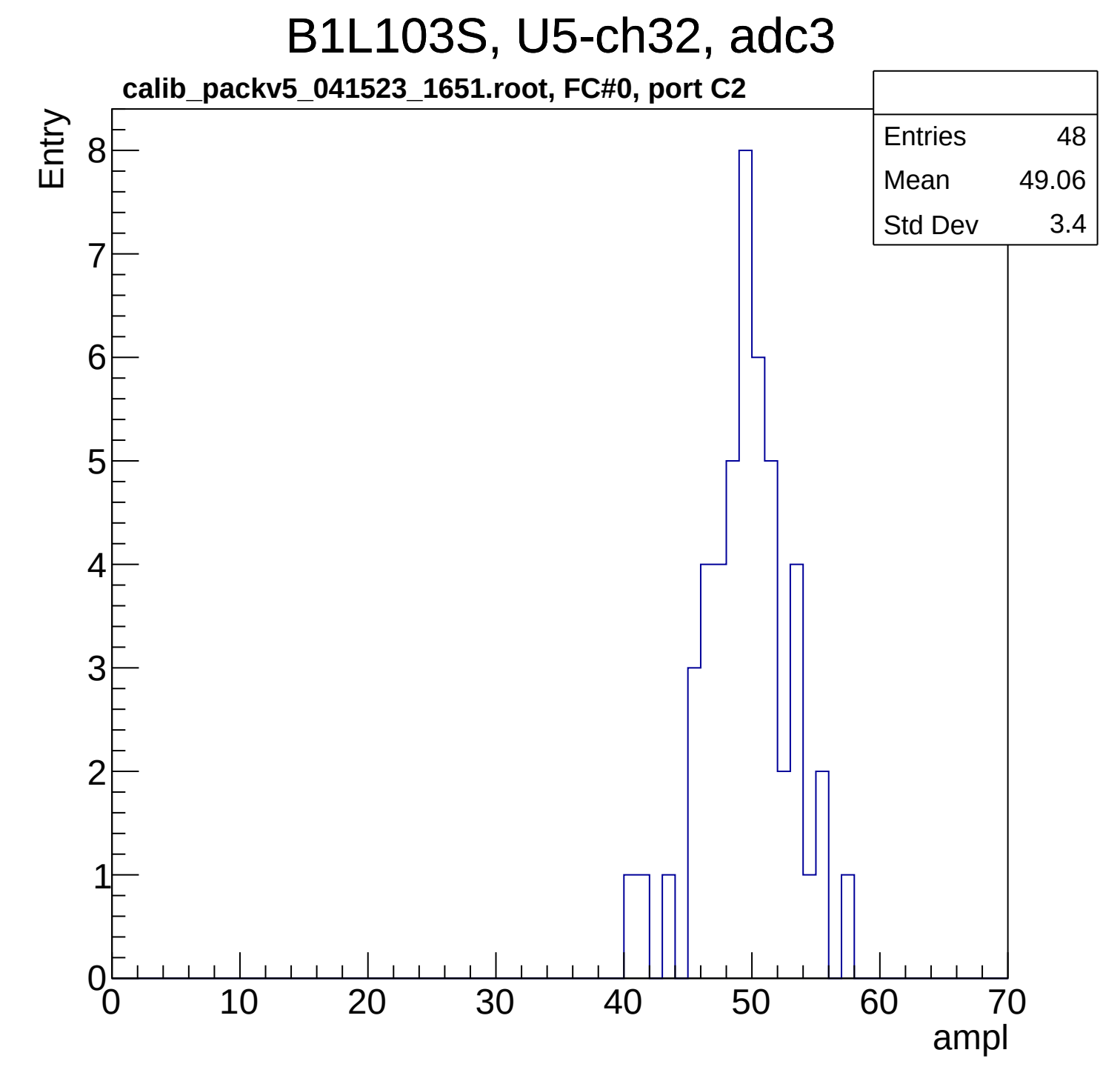
B1L103S, U5-ch32, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 49.06
Std Dev 3.4
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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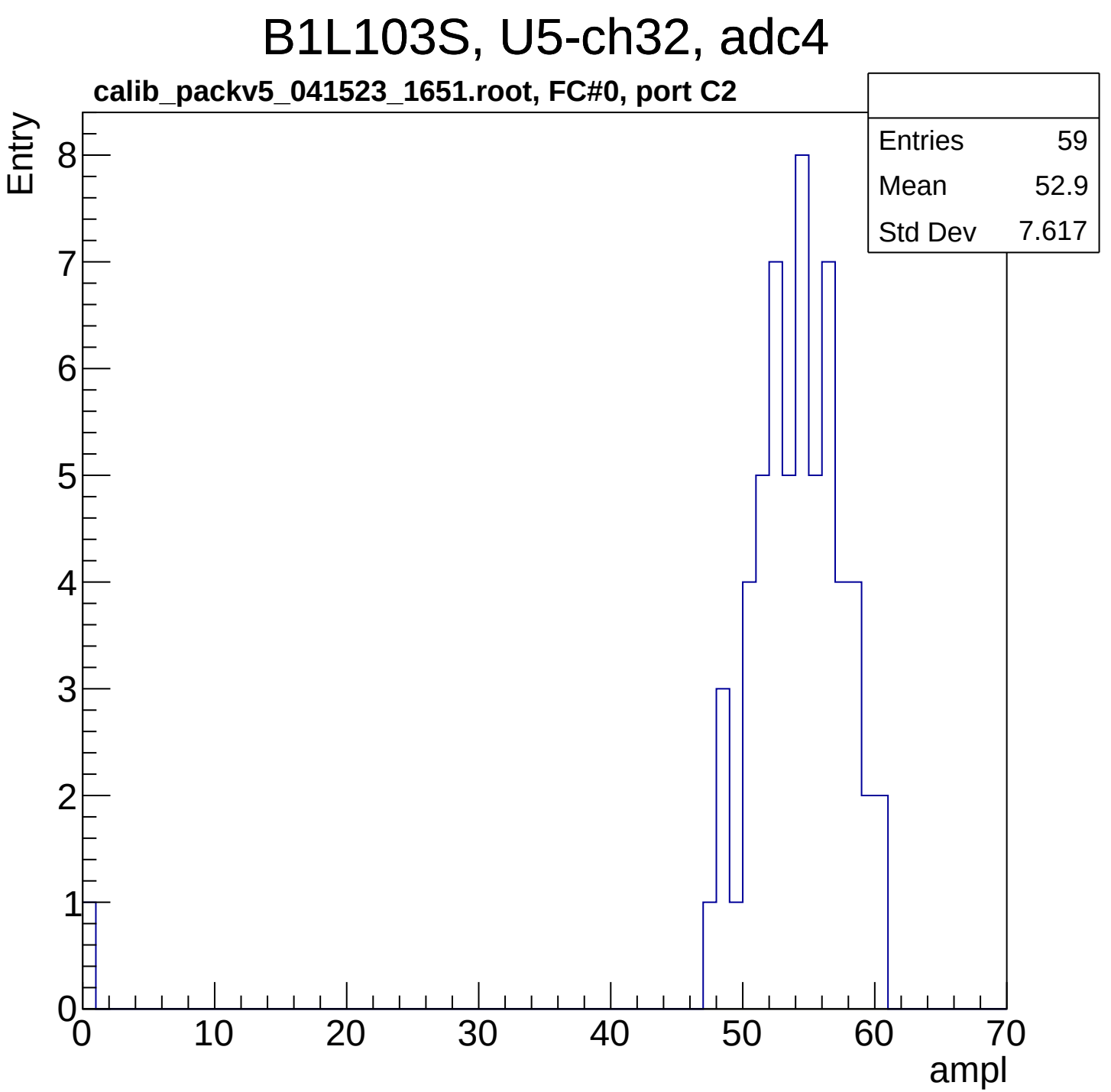
B1L103S, U5-ch32, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 52.9
Std Dev 7.617
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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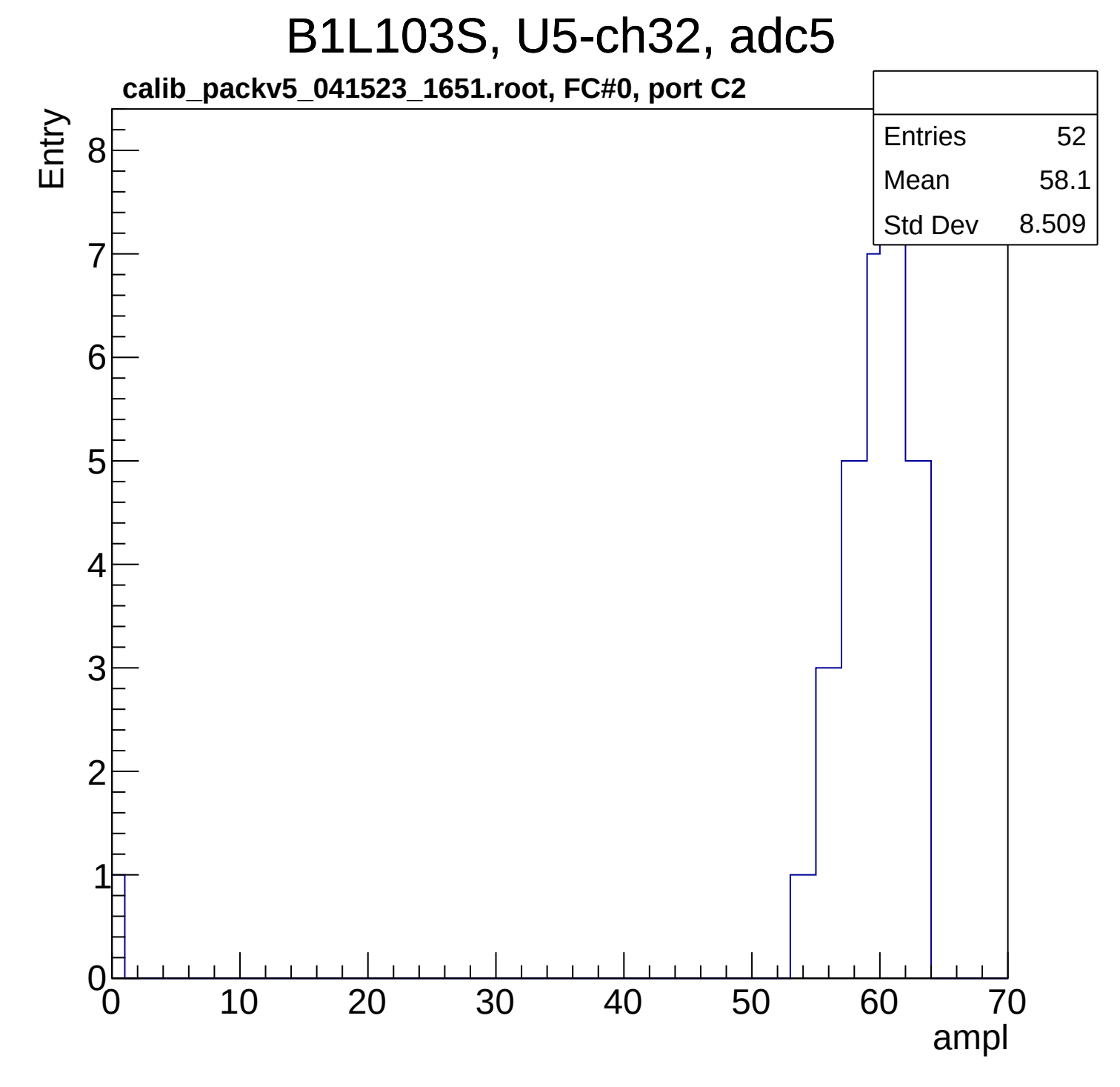
B1L103S, U5-ch32, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.1
Std Dev 8.509
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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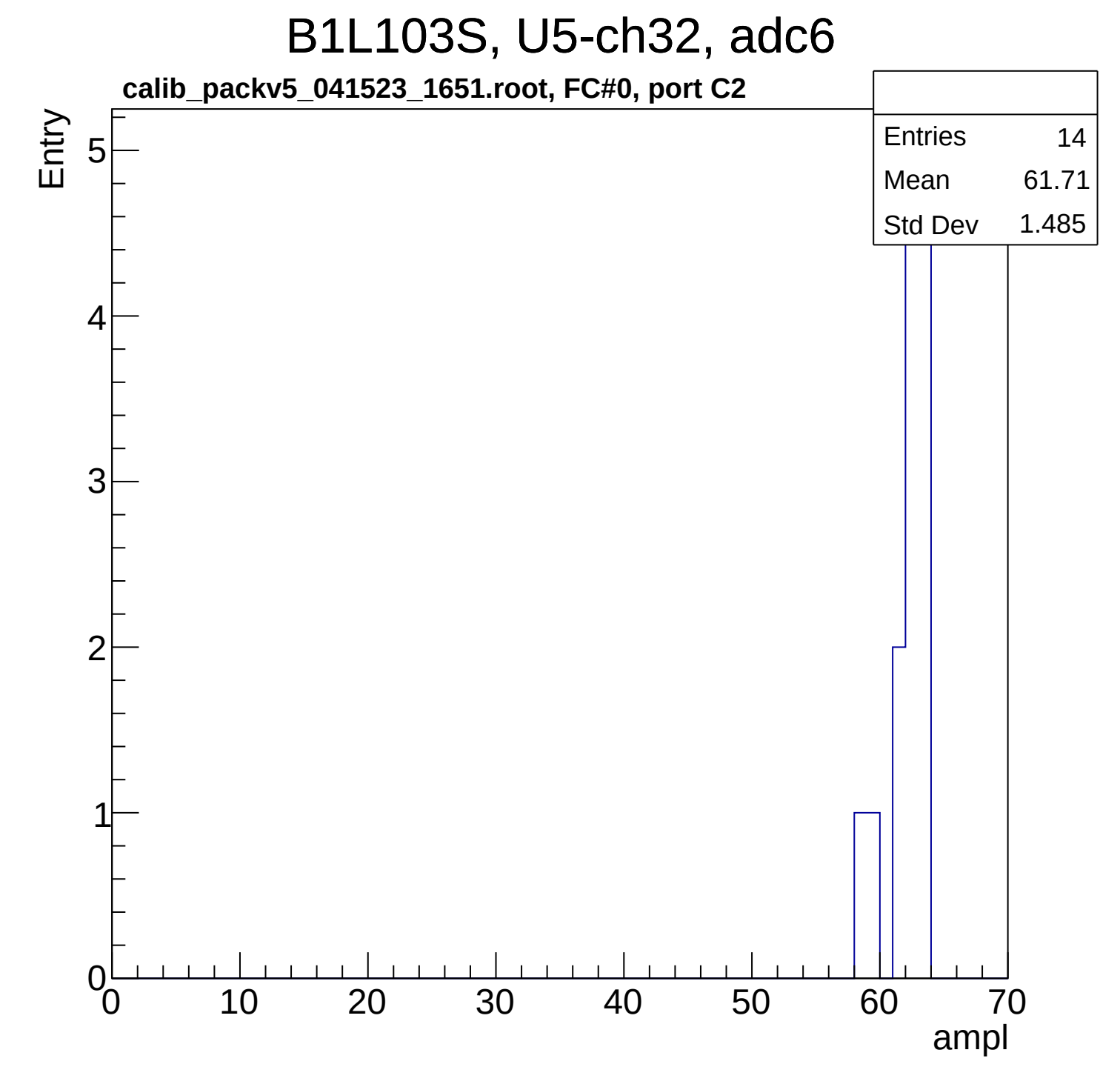
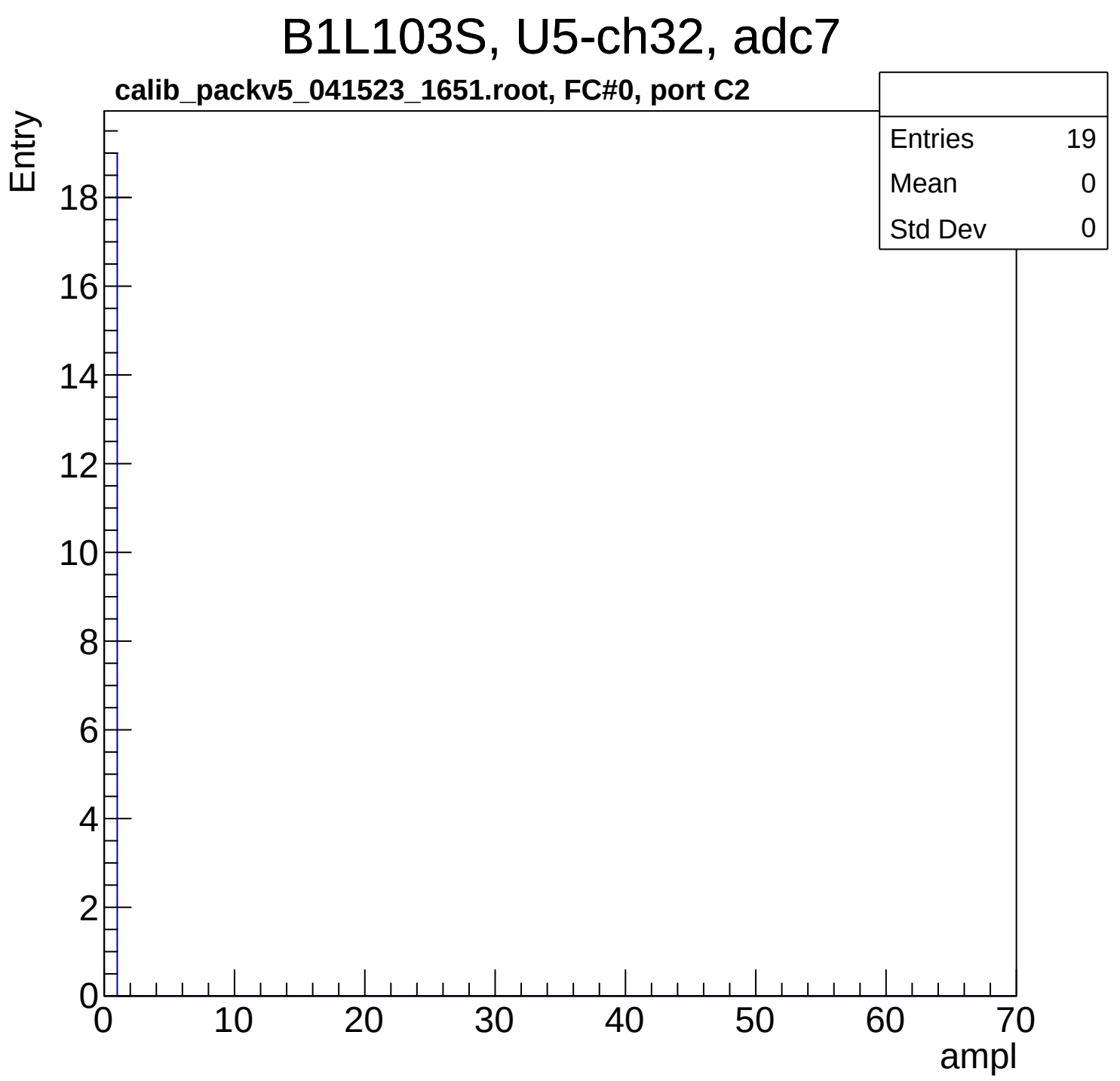
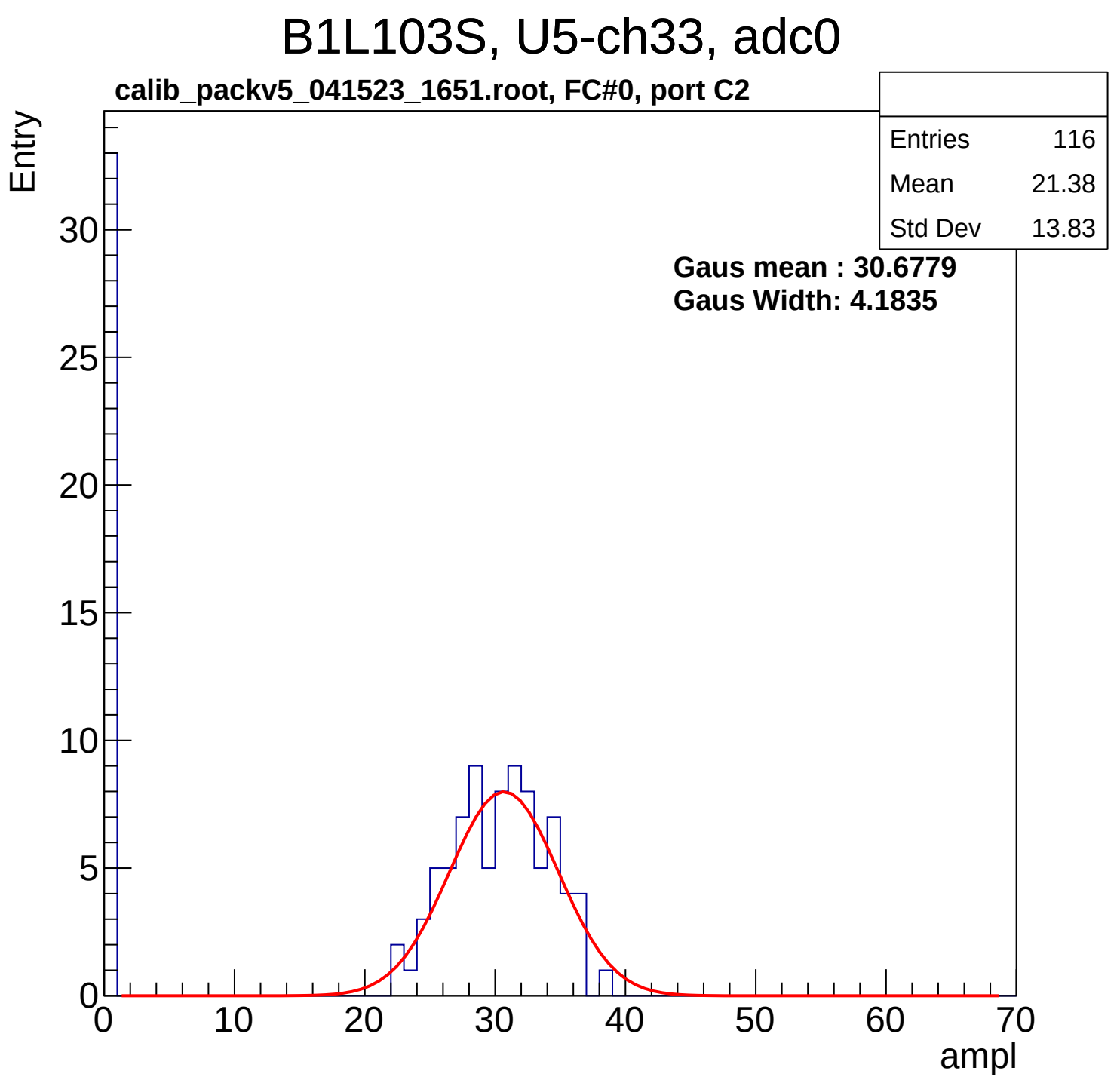

B1L103S, U5-ch32, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.71
Std Dev 1.485
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U5-ch32, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch33, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 116
Mean 21.38
Std Dev 13.83
Gaus mean : 30.6779
Gaus Width: 4.1835
Entry
ampl
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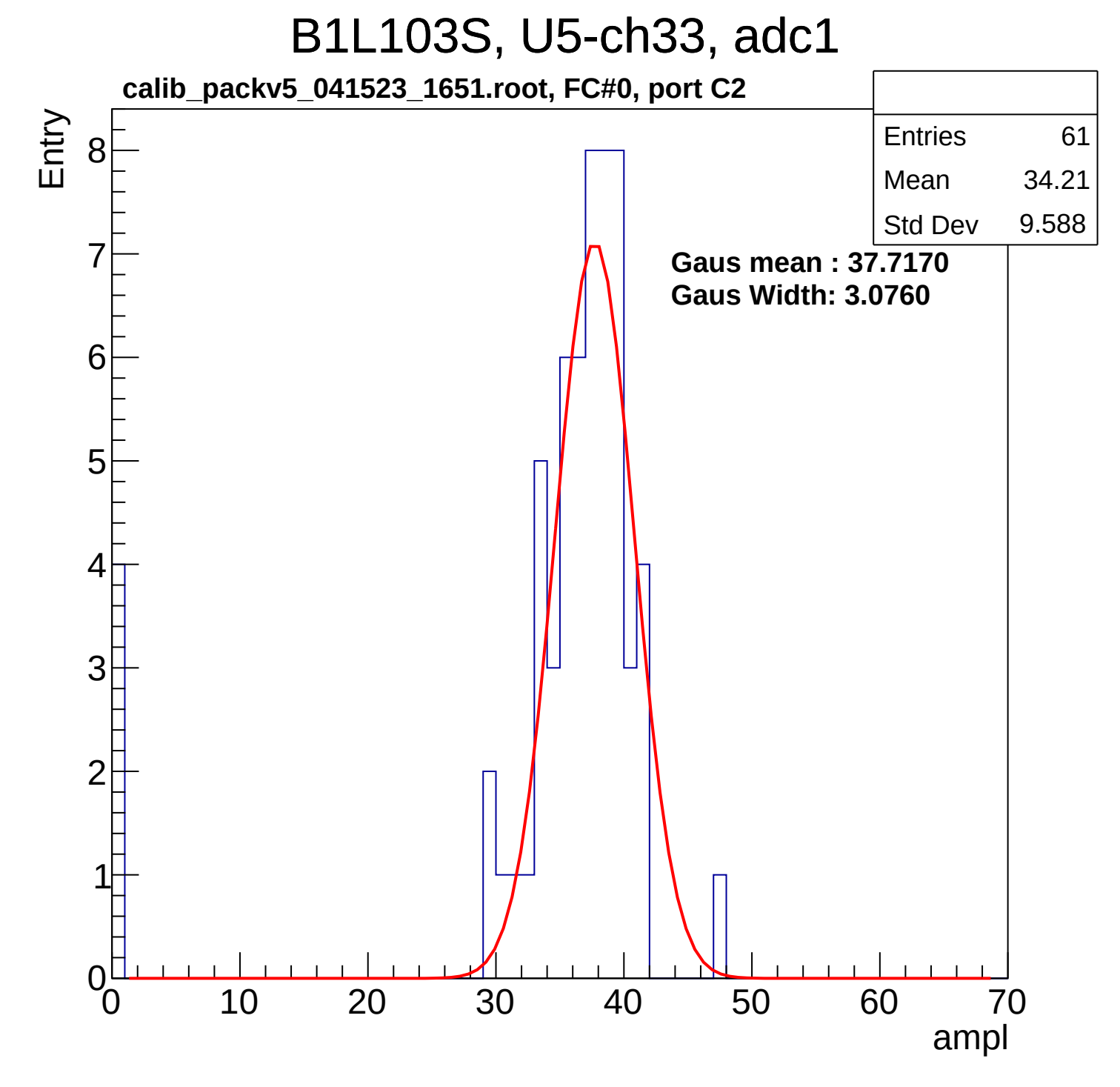
5
10
15
20
25
30
0
10
20
30
40
50
60
70


B1L103S, U5-ch33, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 34.21
Std Dev 9.588
Gaus mean : 37.7170
Gaus Width: 3.0760
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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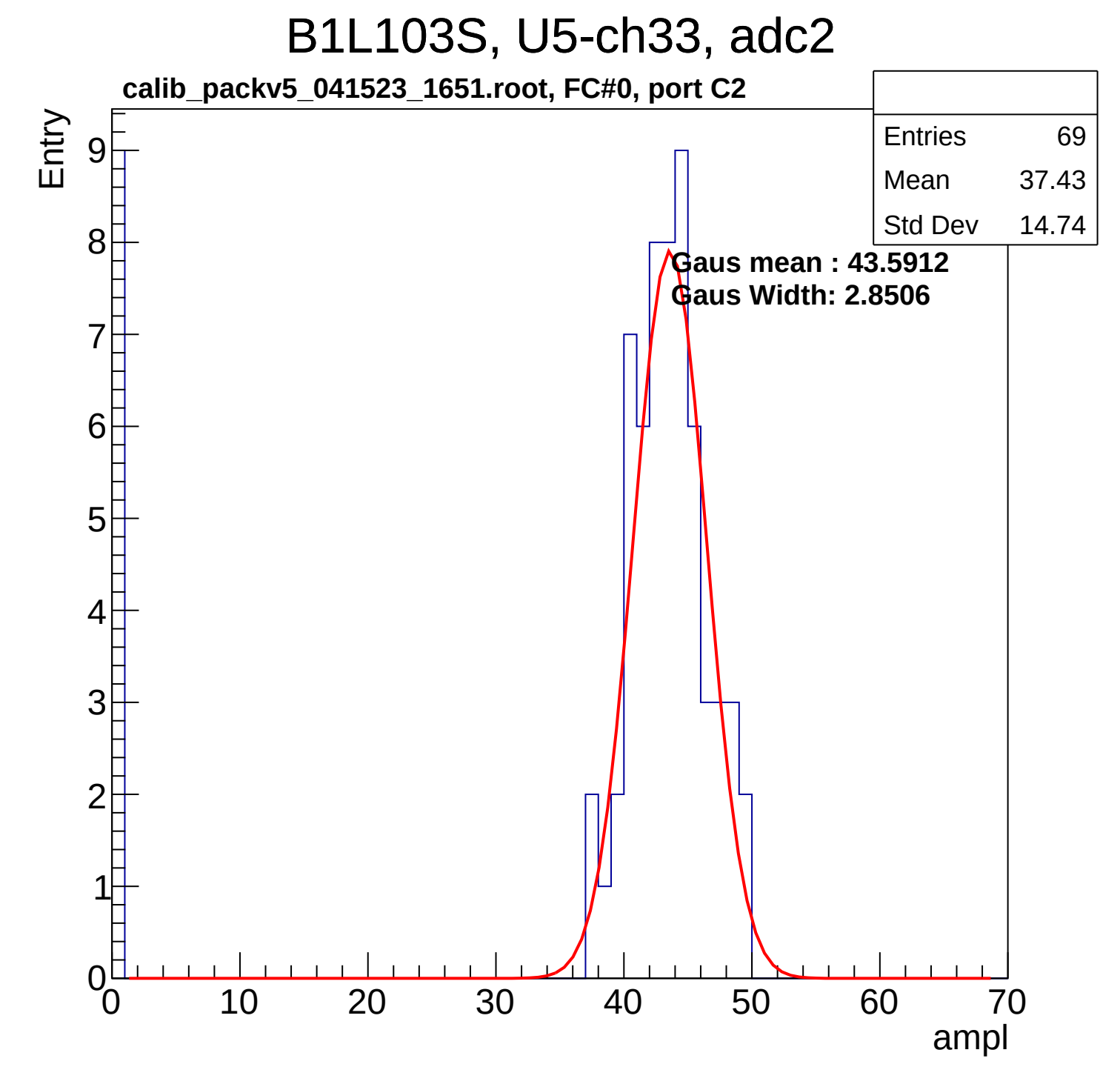
B1L103S, U5-ch33, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 37.43
Std Dev 14.74
Gaus mean : 43.5912
Gaus Width: 2.8506
Entry
ampl
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10
20
30
40
50
60
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1
2
3
4
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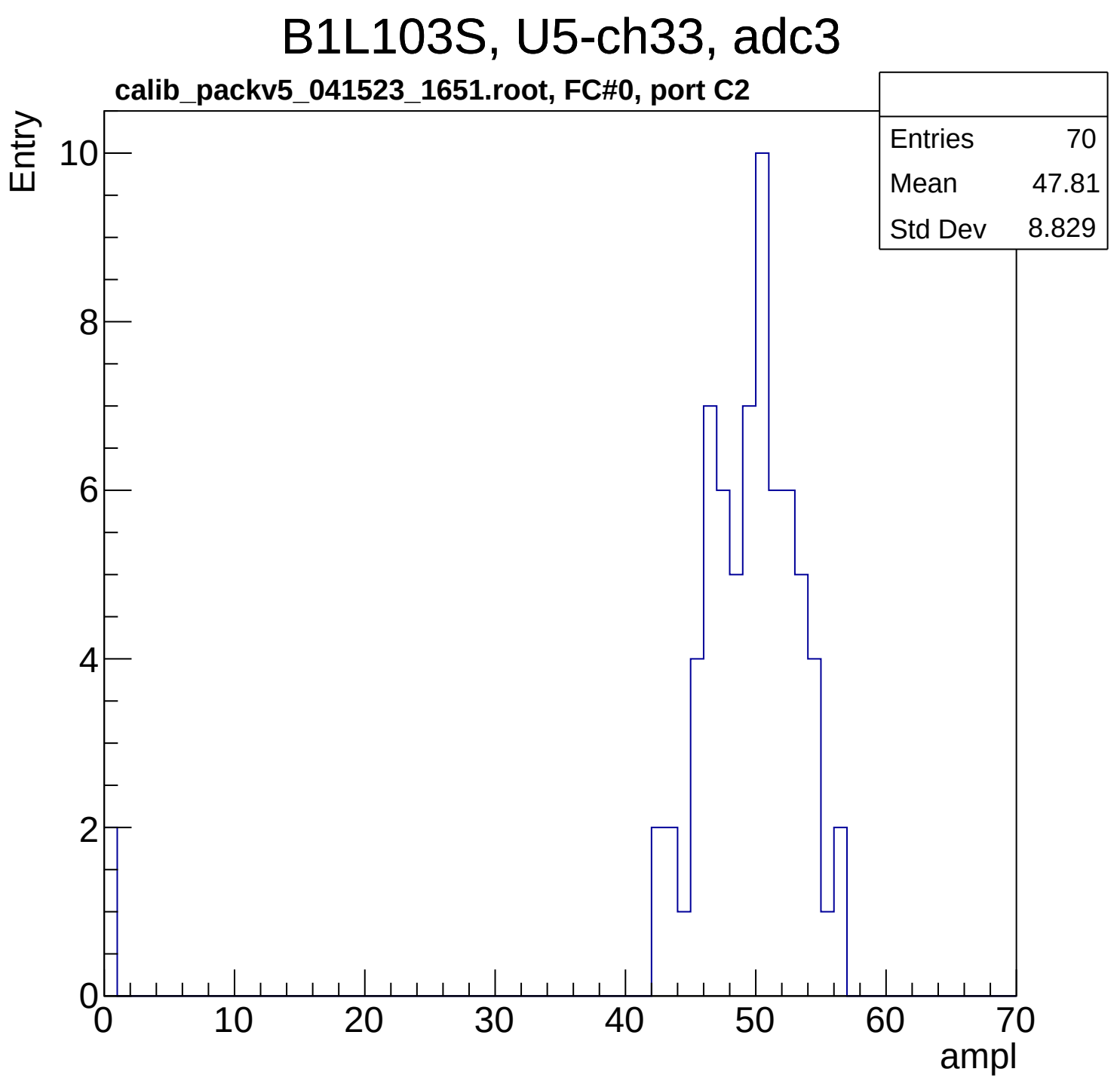
6
7
8
9


B1L103S, U5-ch33, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 47.81
Std Dev 8.829
Entry
ampl
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0
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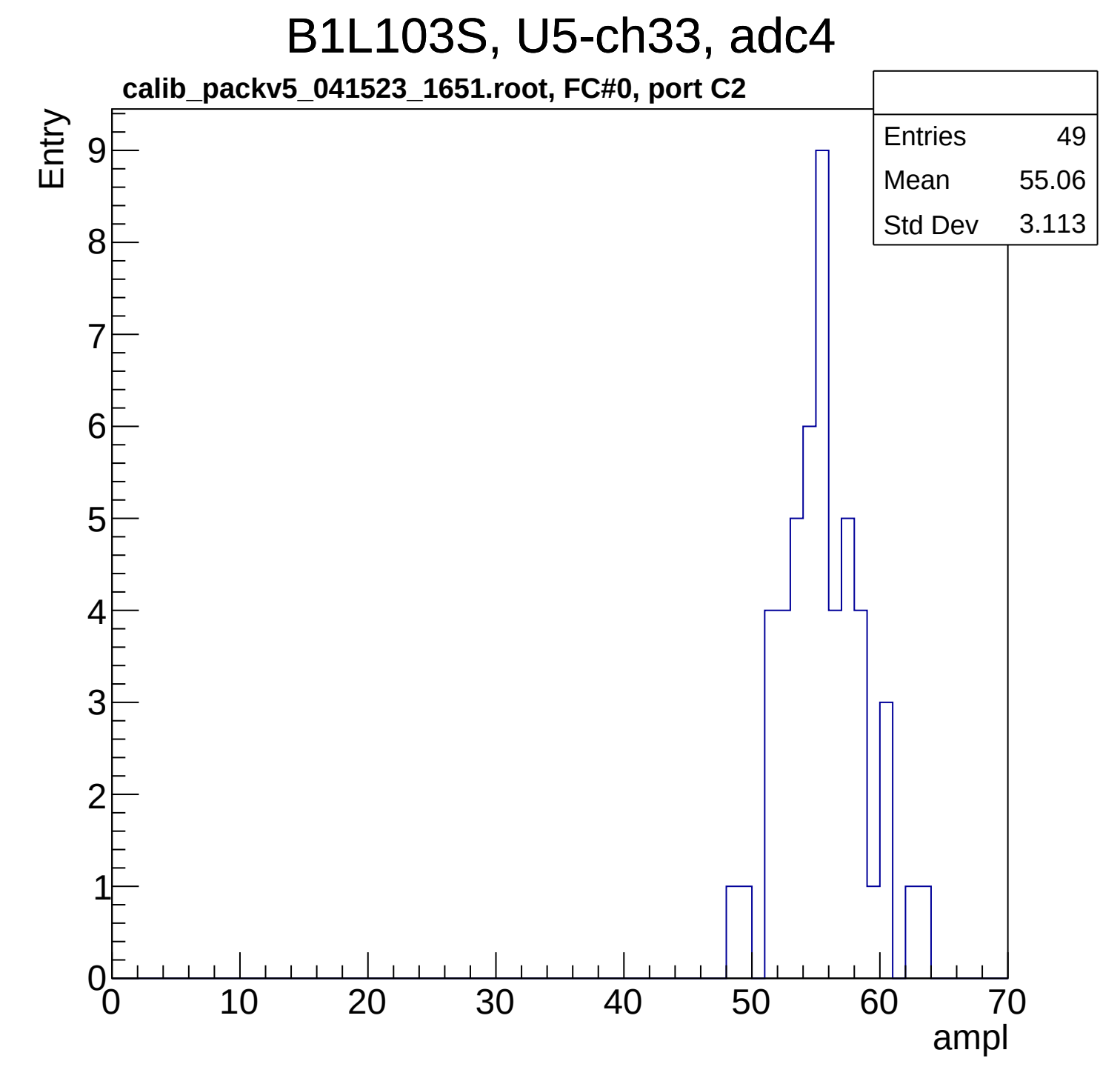
B1L103S, U5-ch33, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 55.06
Std Dev 3.113
Entry
ampl
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3
4
5
6
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0
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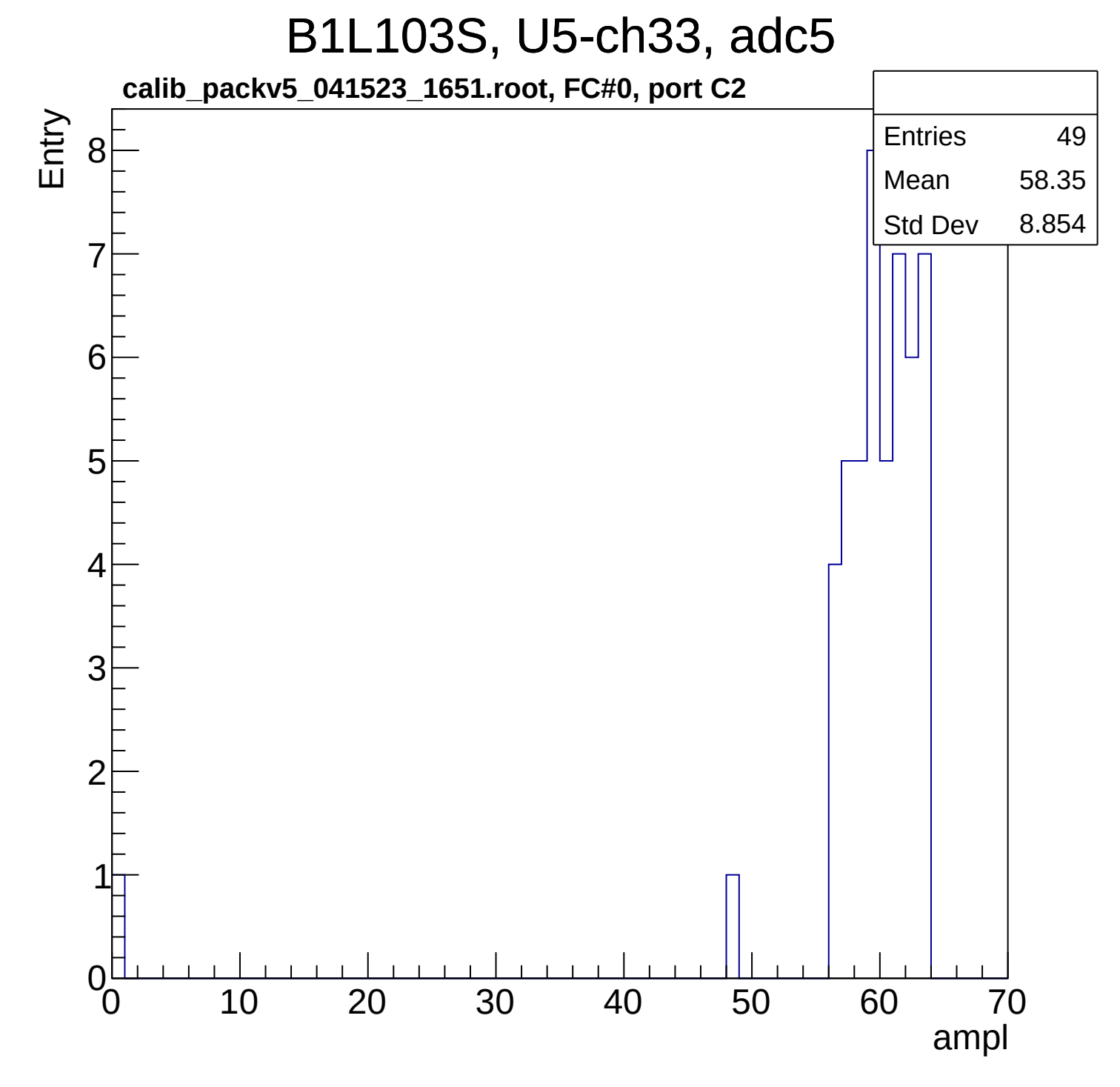
B1L103S, U5-ch33, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.35
Std Dev 8.854
Entry
ampl
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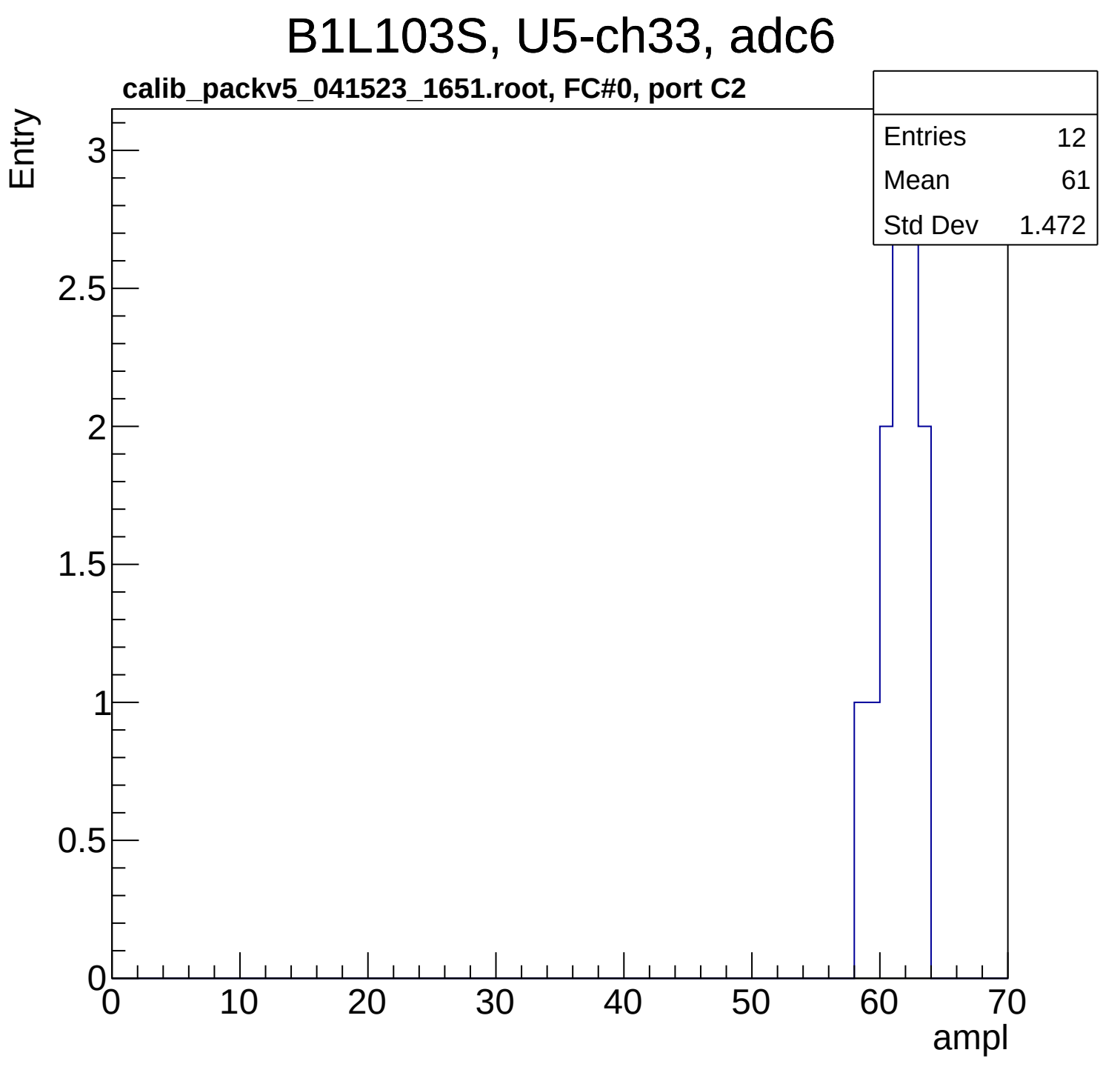
B1L103S, U5-ch33, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61
Std Dev 1.472
Entry
ampl
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1
1.5
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2.5
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0
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60
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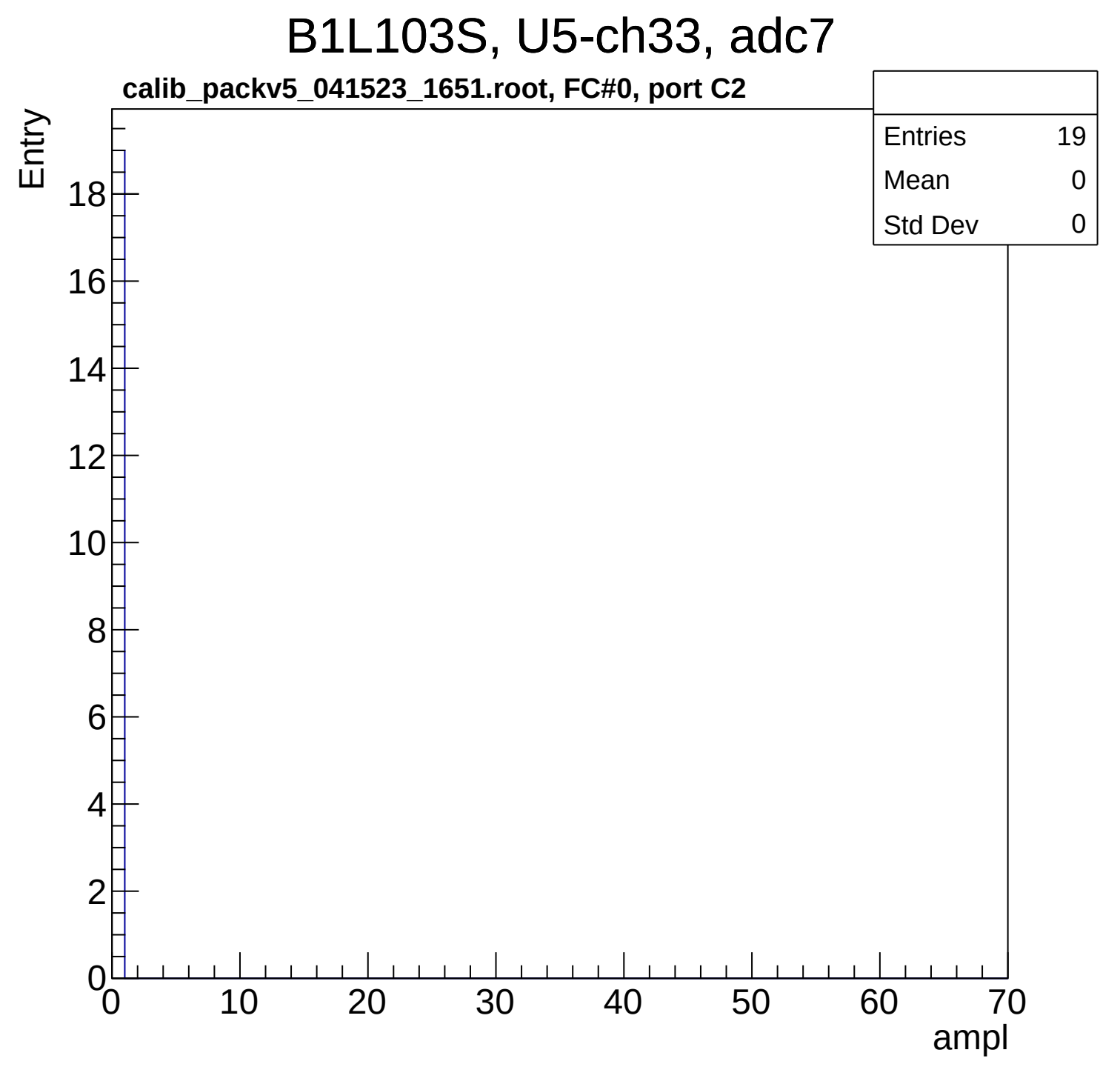
B1L103S, U5-ch33, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
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18
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10
20
30
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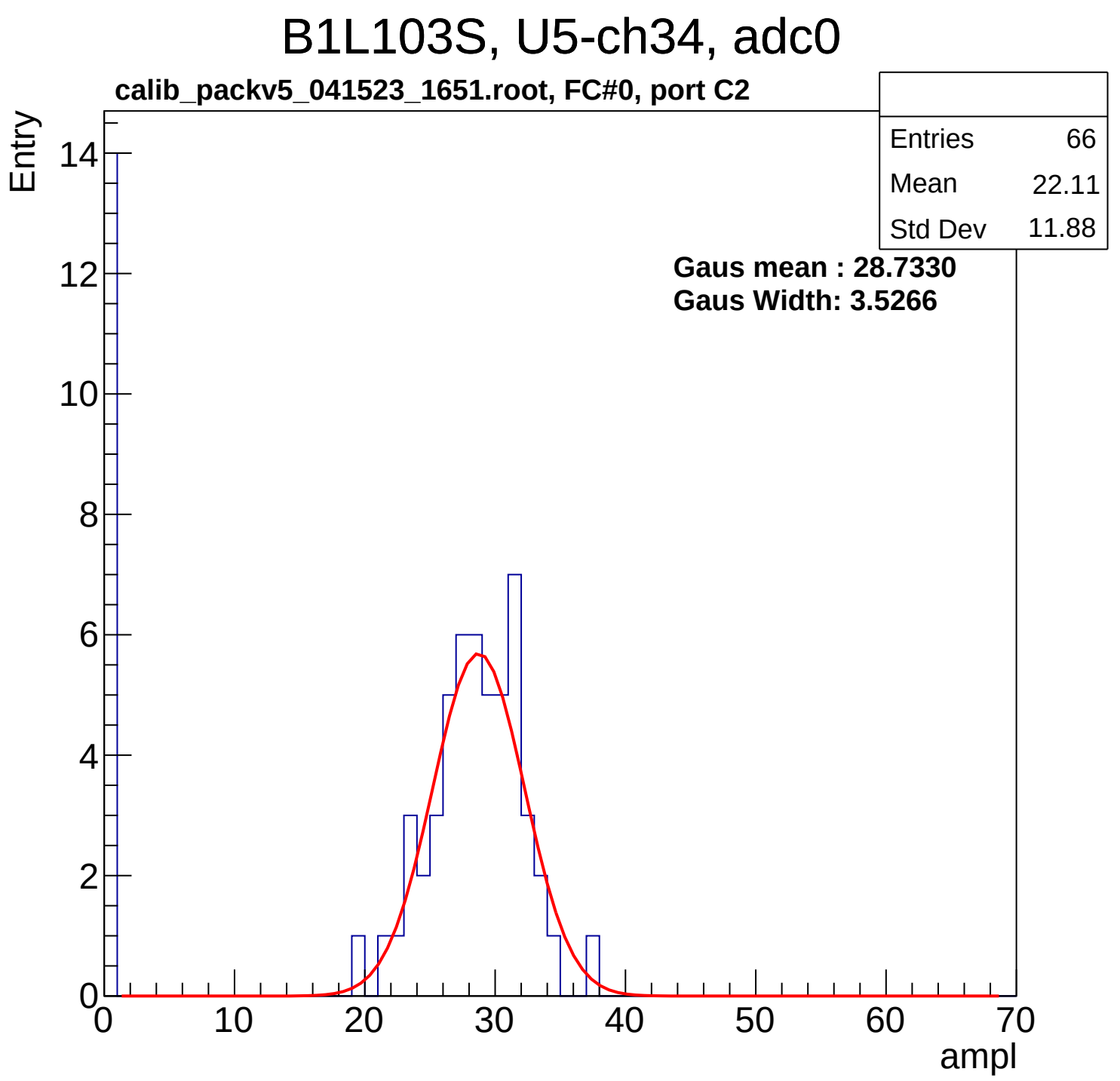
50
60
70
ampl


B1L103S, U5-ch34, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 22.11
Std Dev 11.88
Gaus mean : 28.7330
Gaus Width: 3.5266
Entry
ampl
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6
8
10
12
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0
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40
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60
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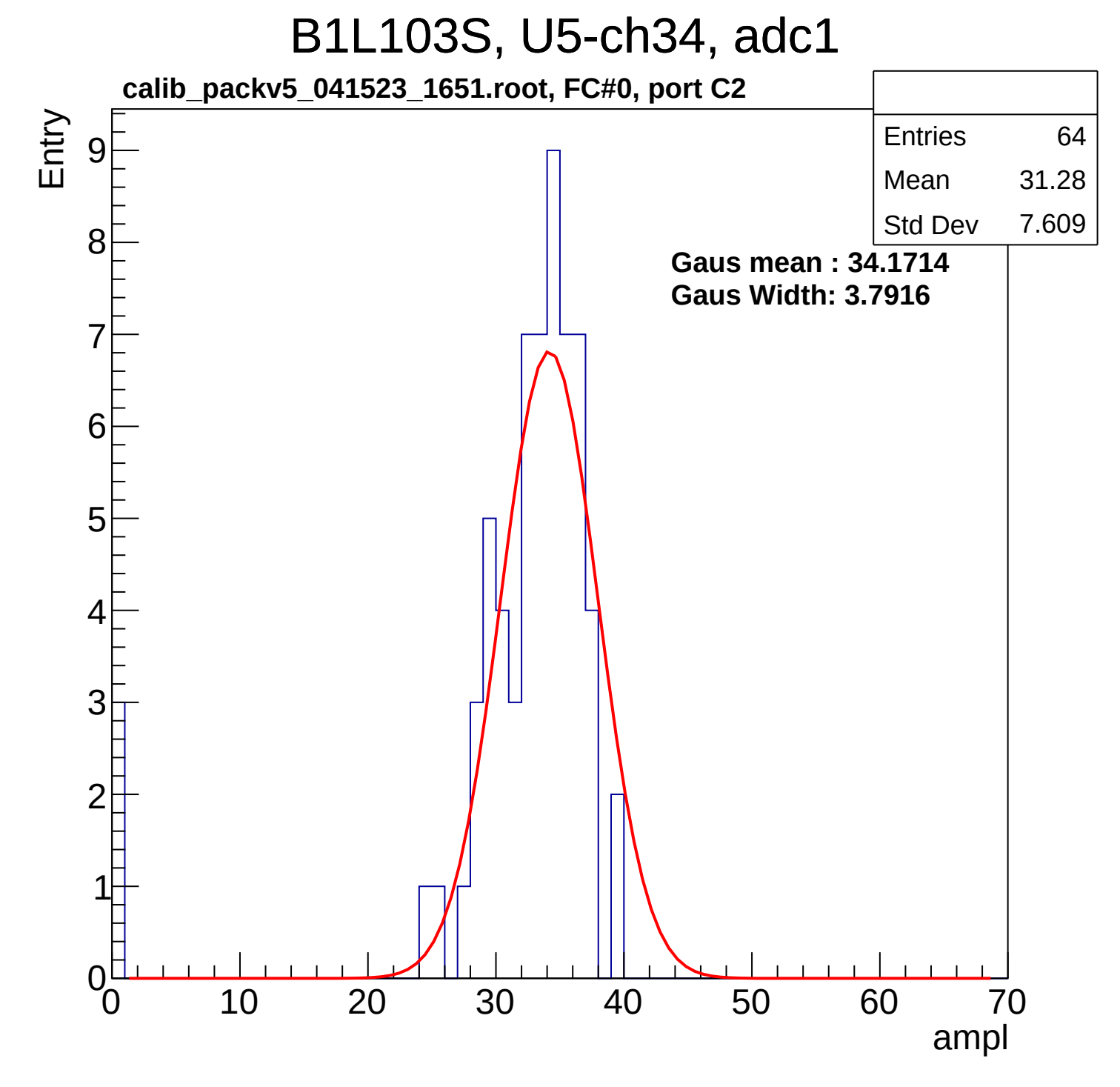
B1L103S, U5-ch34, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 31.28
Std Dev 7.609
Gaus mean : 34.1714
Gaus Width: 3.7916
Entry
ampl
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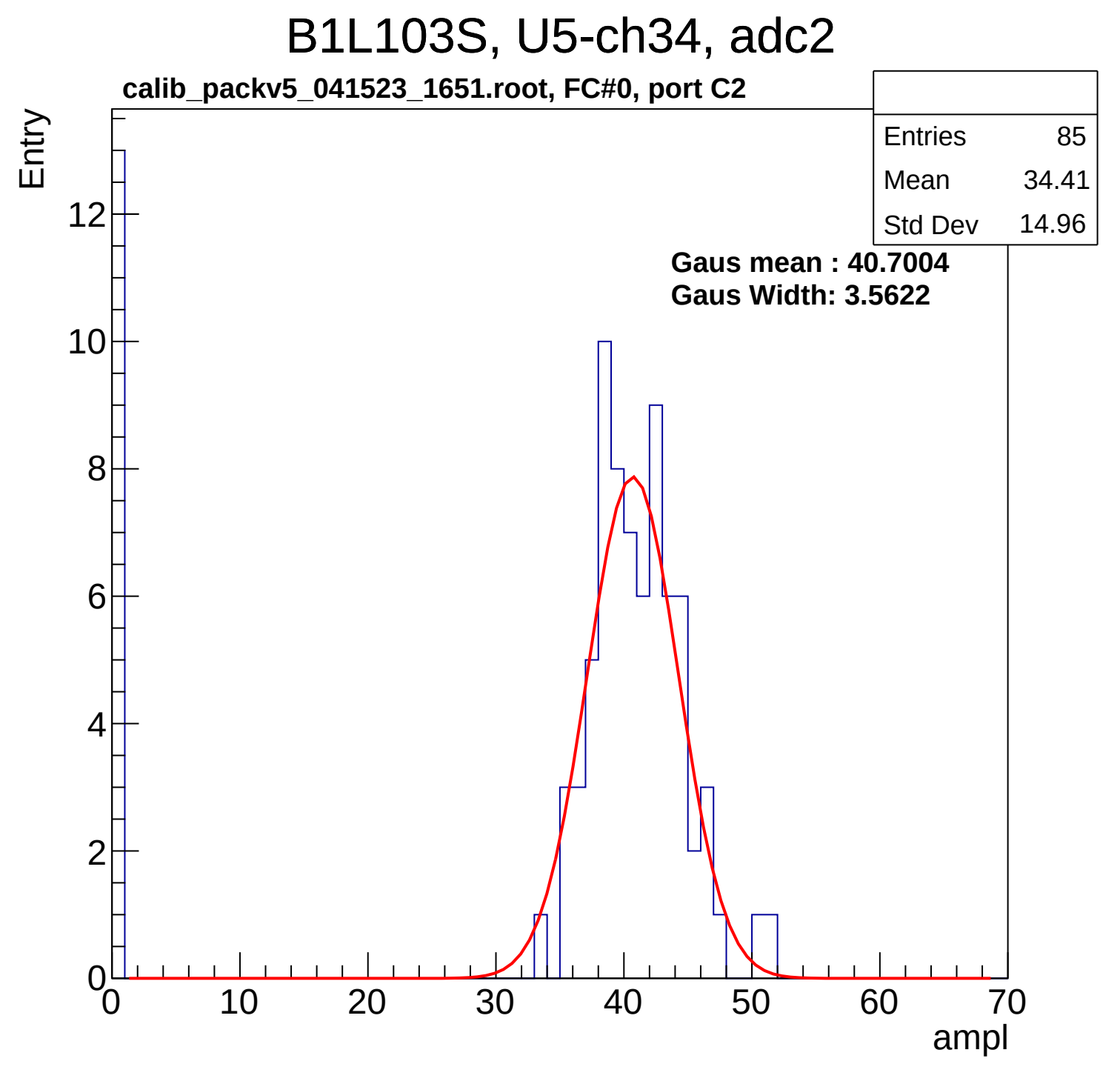
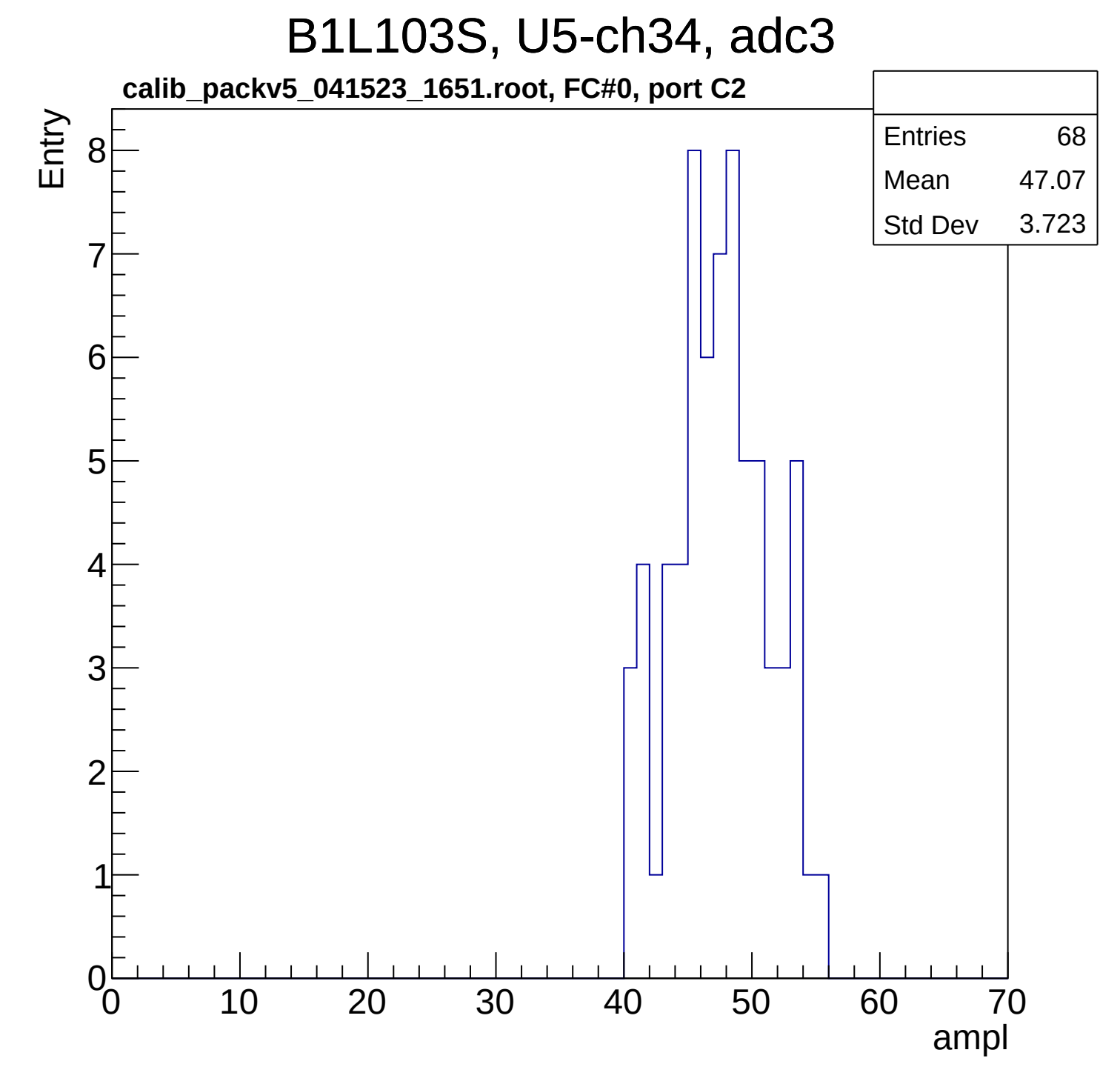
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U5-ch34, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 34.41
Std Dev 14.96
Gaus mean : 40.7004
Gaus Width: 3.5622
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U5-ch34, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 47.07
Std Dev 3.723
Entry
ampl
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2
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4
5
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7
8
0
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60
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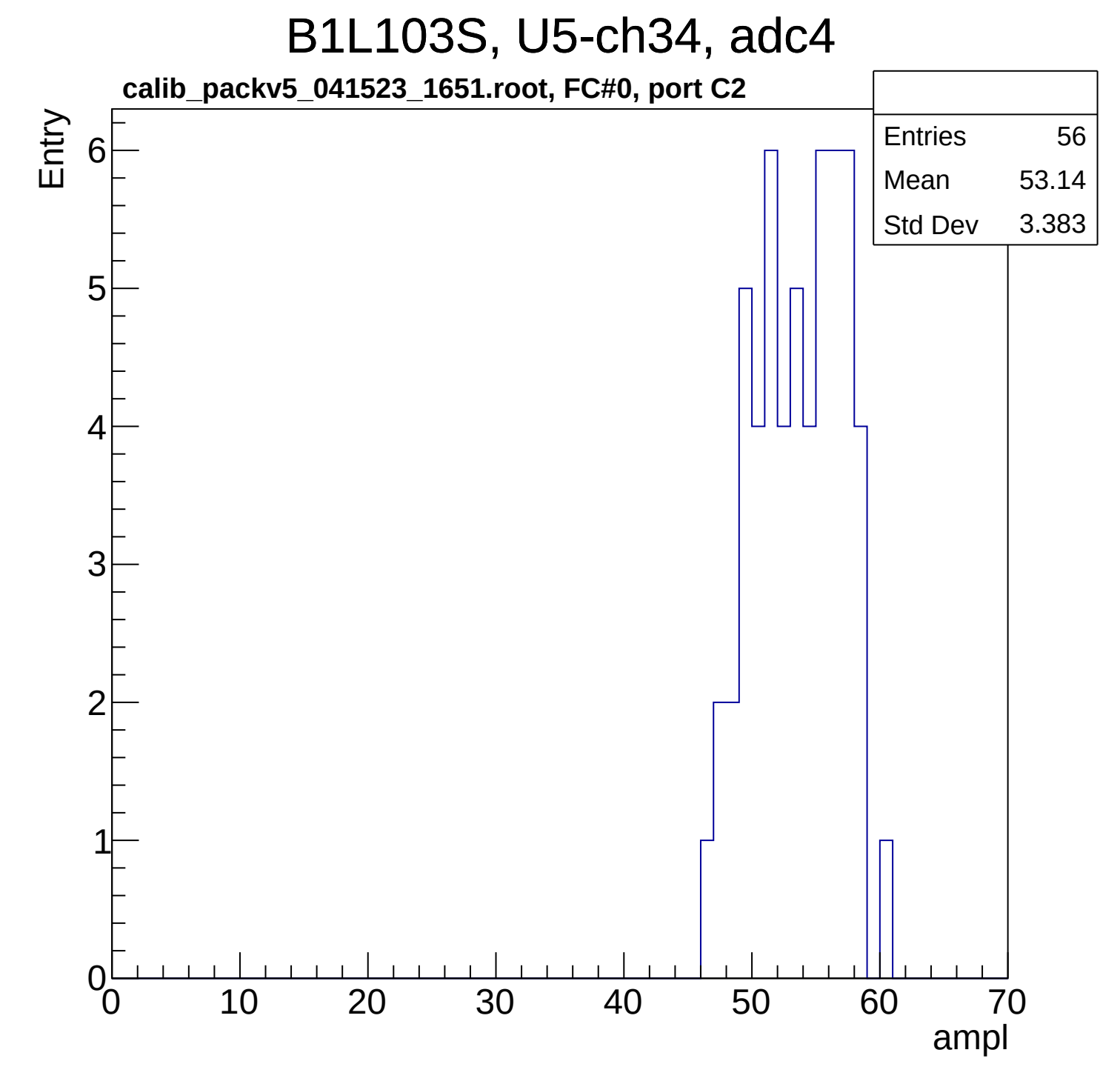
B1L103S, U5-ch34, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 53.14
Std Dev 3.383
Entry
ampl
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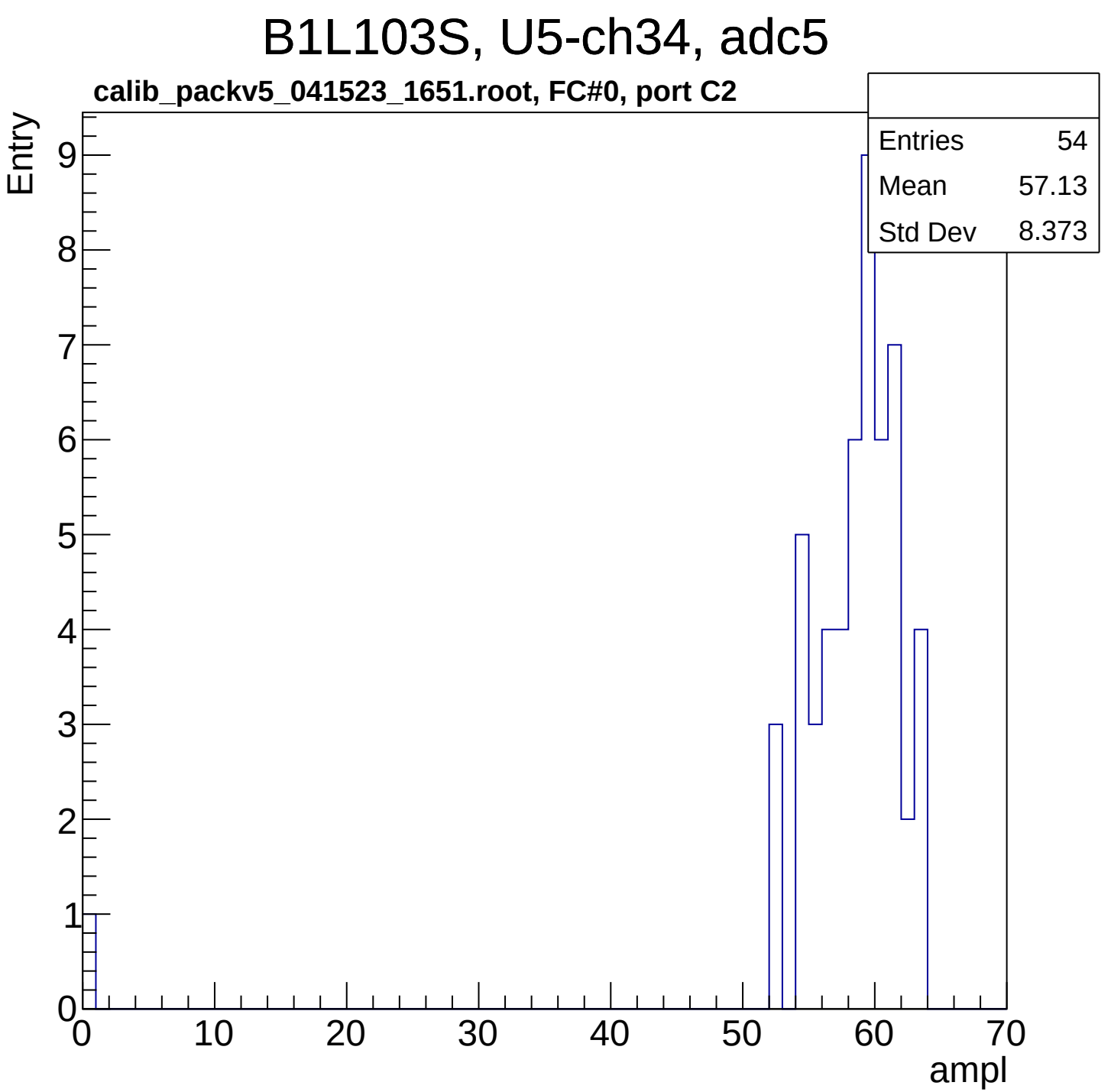
B1L103S, U5-ch34, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.13
Std Dev 8.373
Entry
ampl
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3
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7
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0
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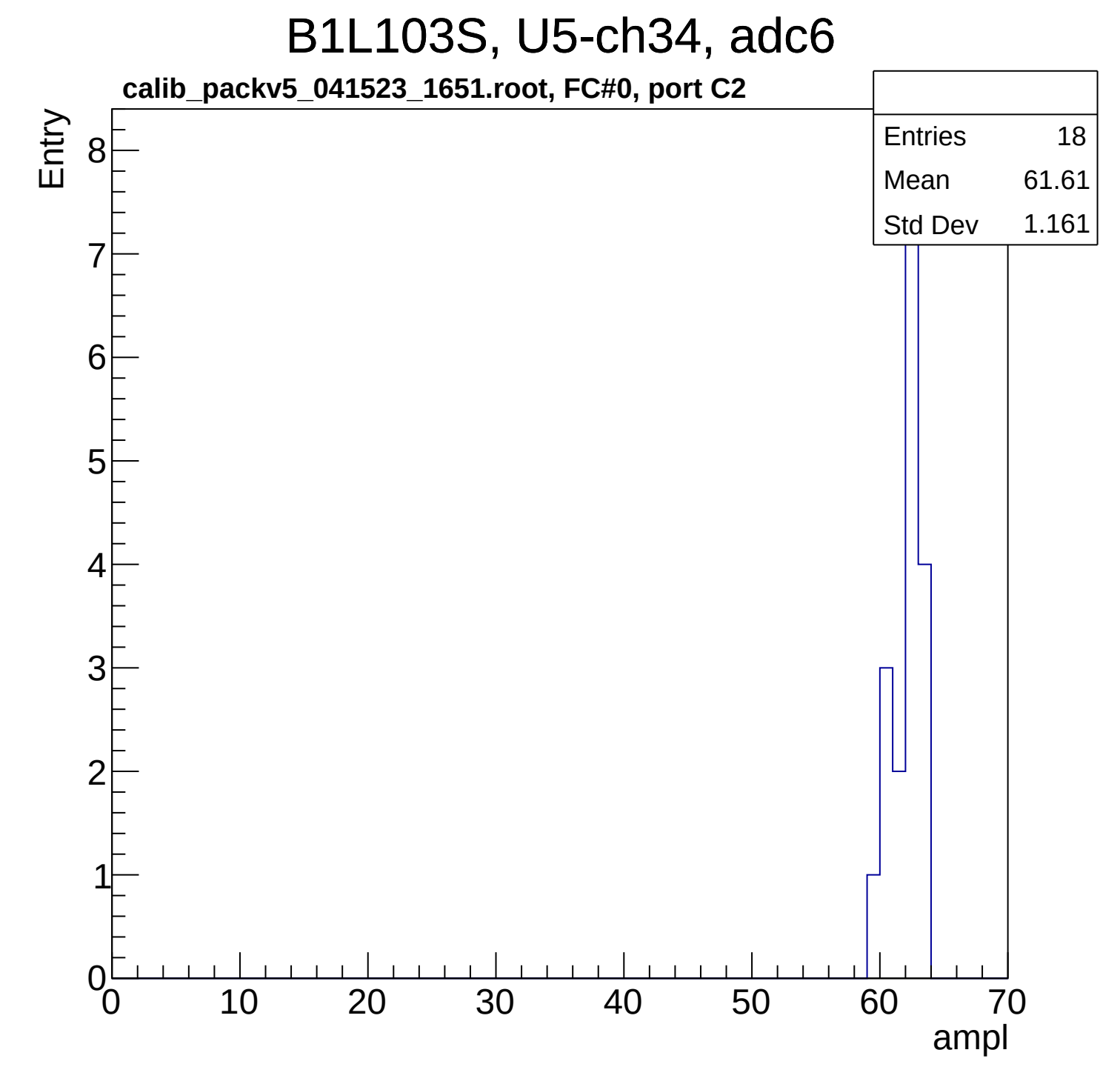
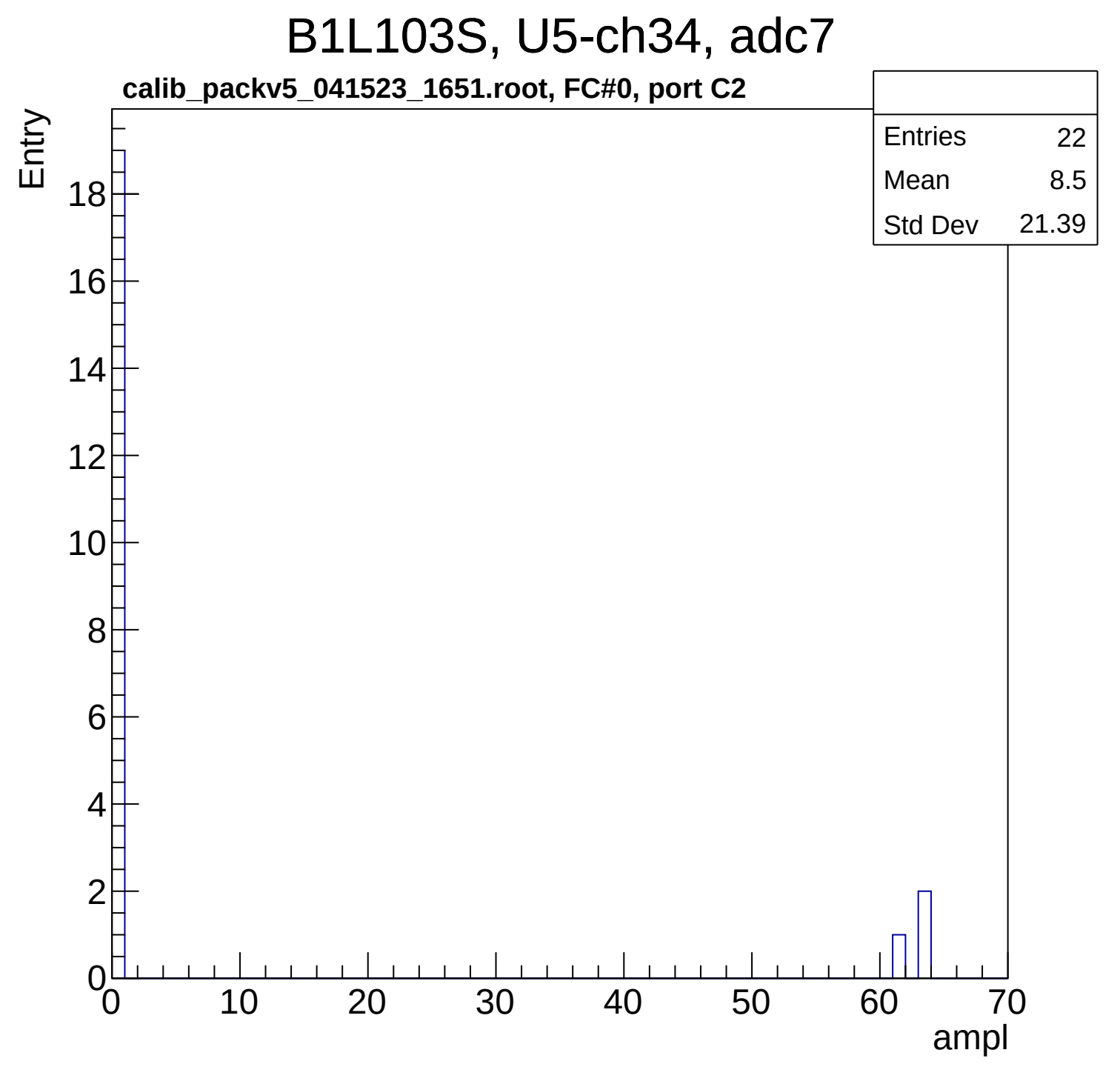

B1L103S, U5-ch34, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 61.61
Std Dev 1.161
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U5-ch34, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.5
Std Dev 21.39
Entry
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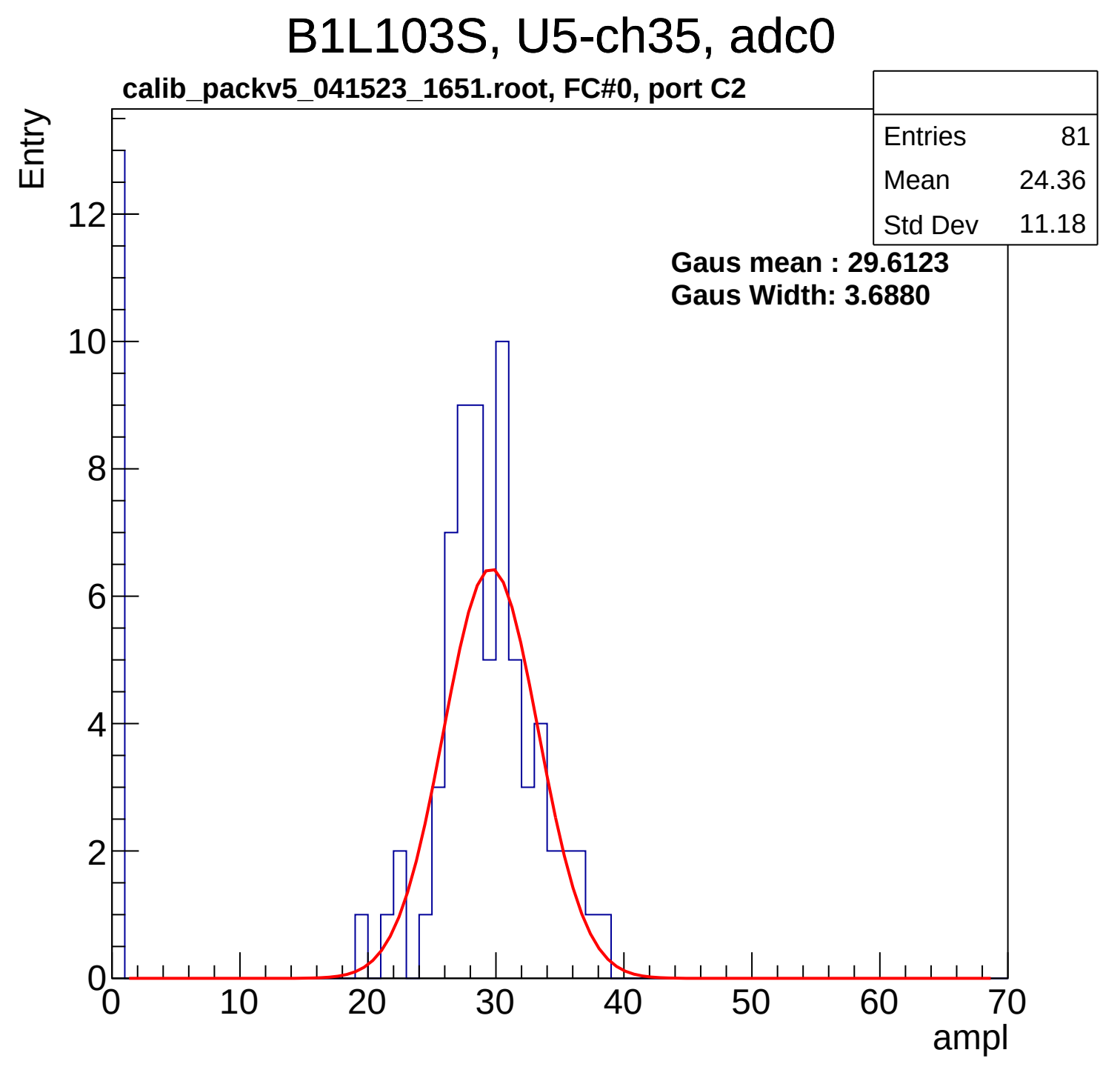
ampl


B1L103S, U5-ch35, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 24.36
Std Dev 11.18
Gaus mean : 29.6123
Gaus Width: 3.6880
Entry
ampl
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2
4
6
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10
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0
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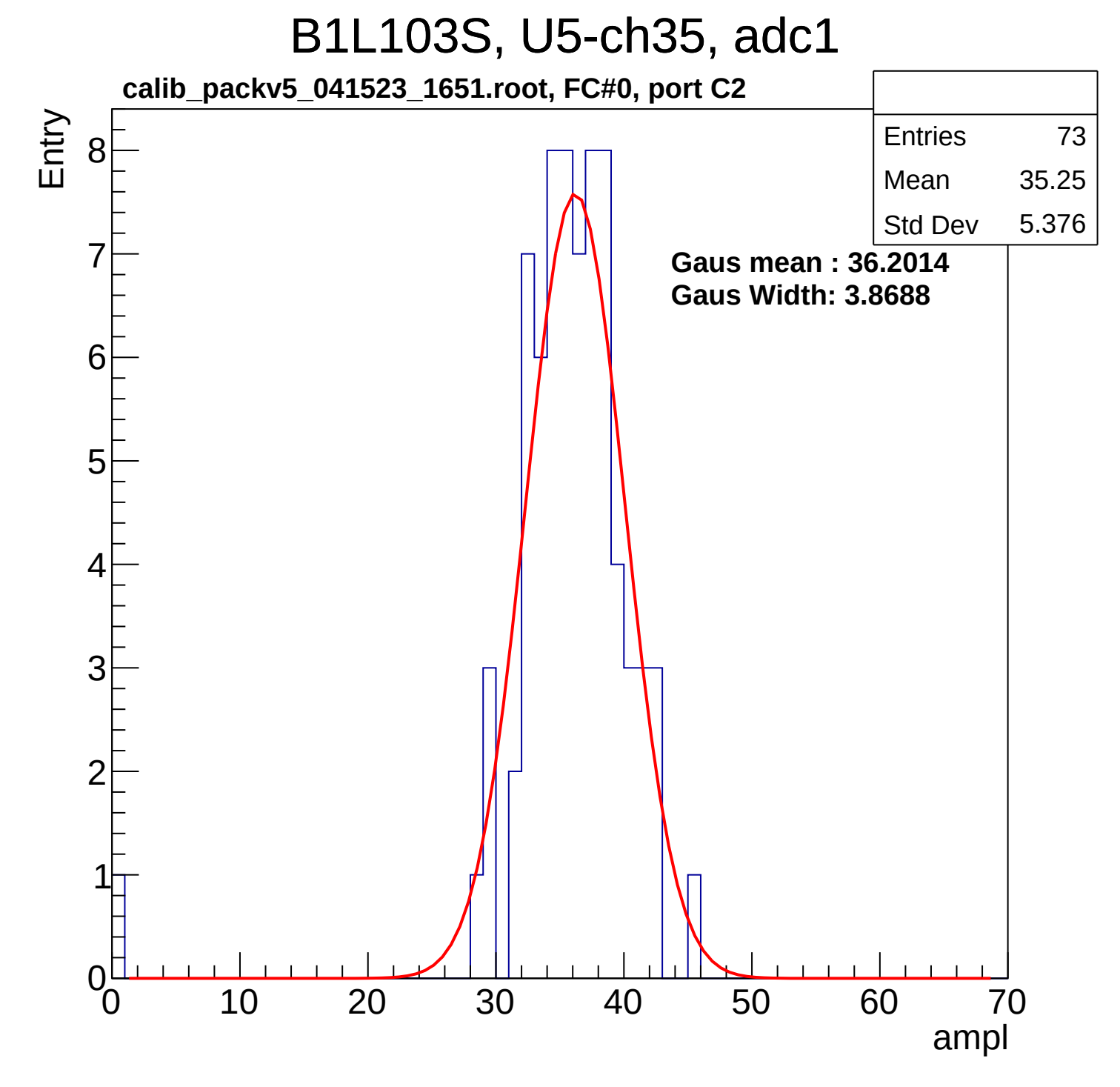
B1L103S, U5-ch35, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 35.25
Std Dev 5.376
Gaus mean : 36.2014
Gaus Width: 3.8688
Entry
ampl
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2
3
4
5
6
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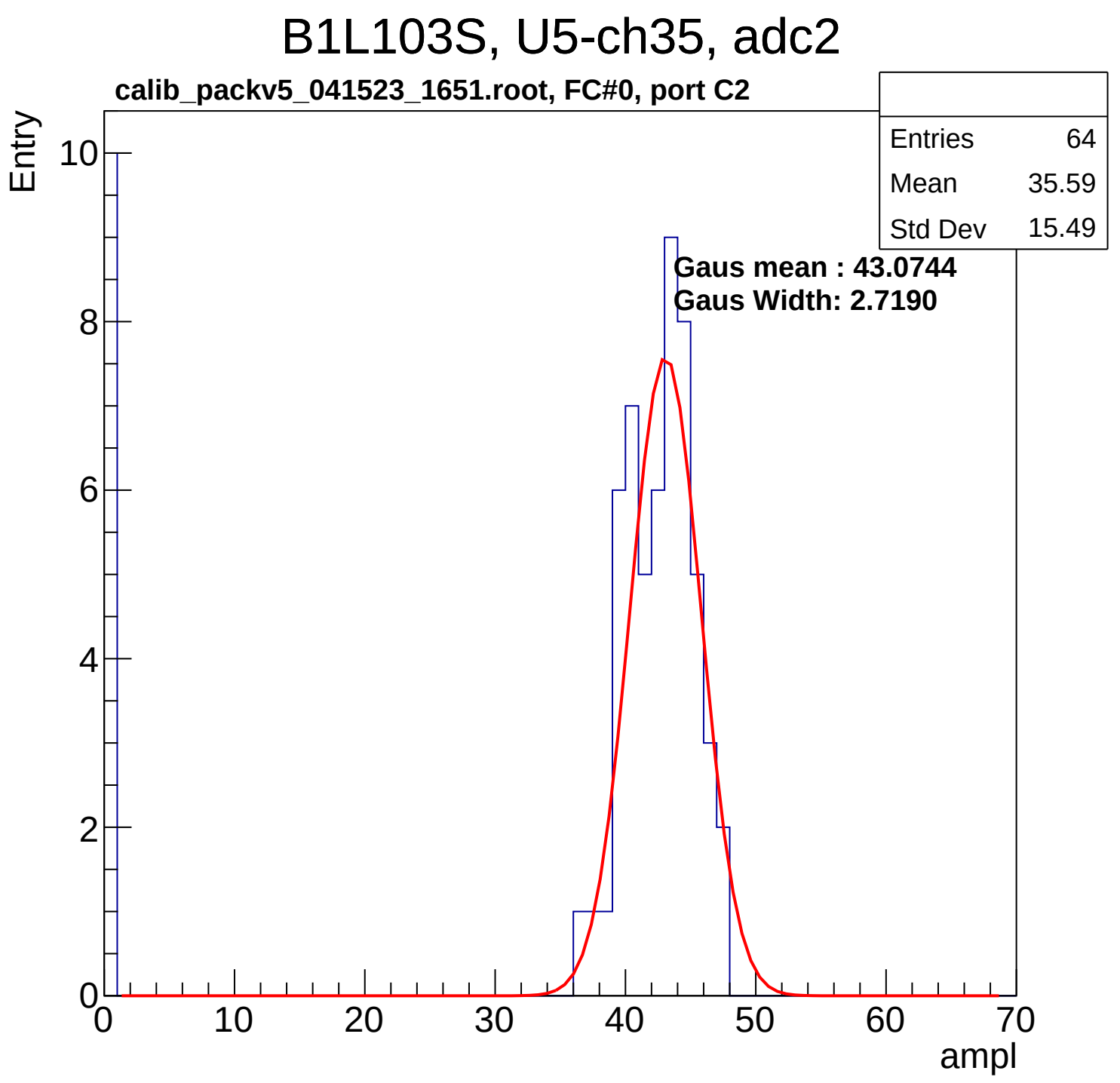
B1L103S, U5-ch35, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 35.59
Std Dev 15.49
Gaus mean : 43.0744
Gaus Width: 2.7190
Entry
ampl
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0
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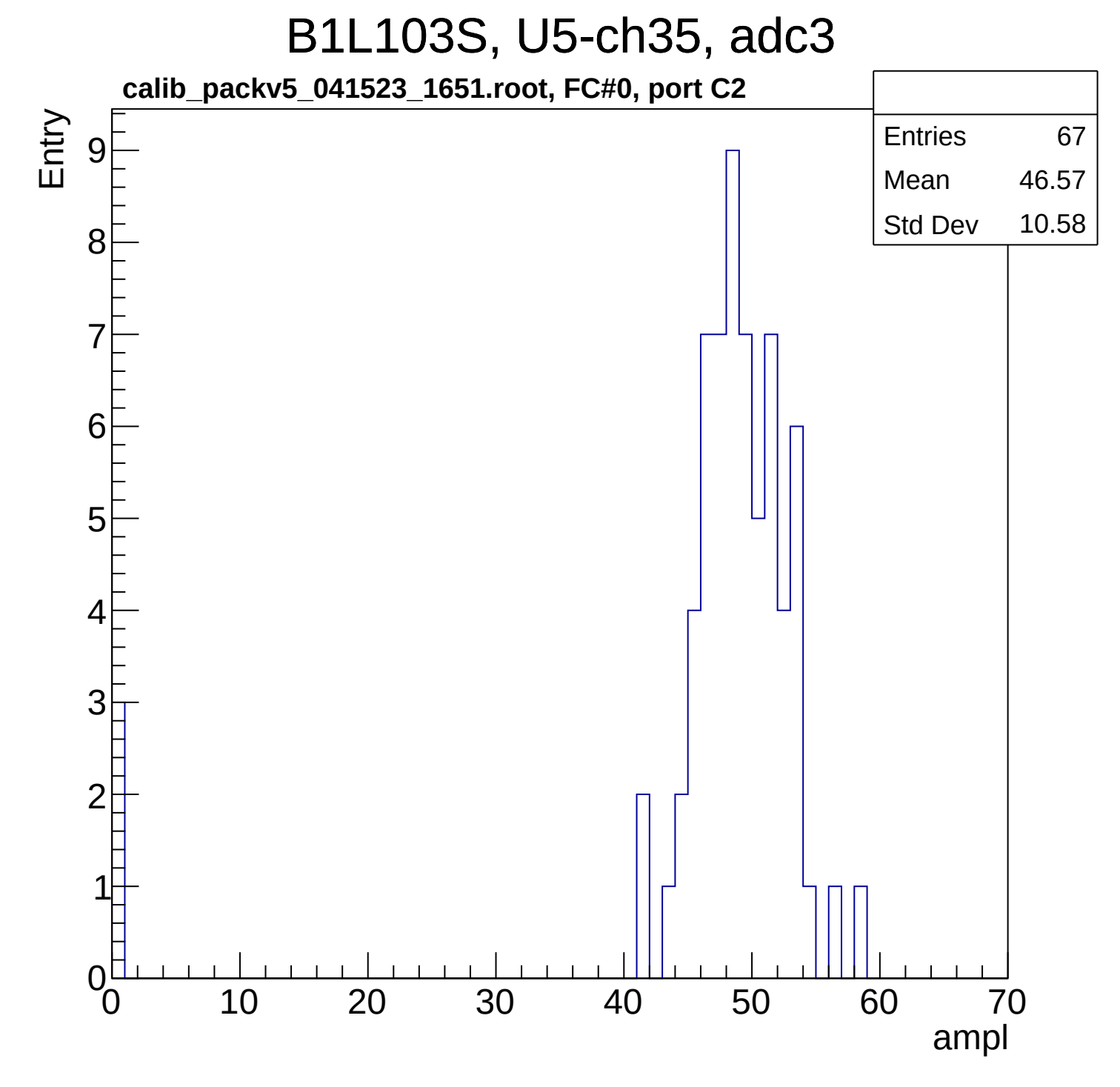
B1L103S, U5-ch35, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 46.57
Std Dev 10.58
Entry
ampl
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0
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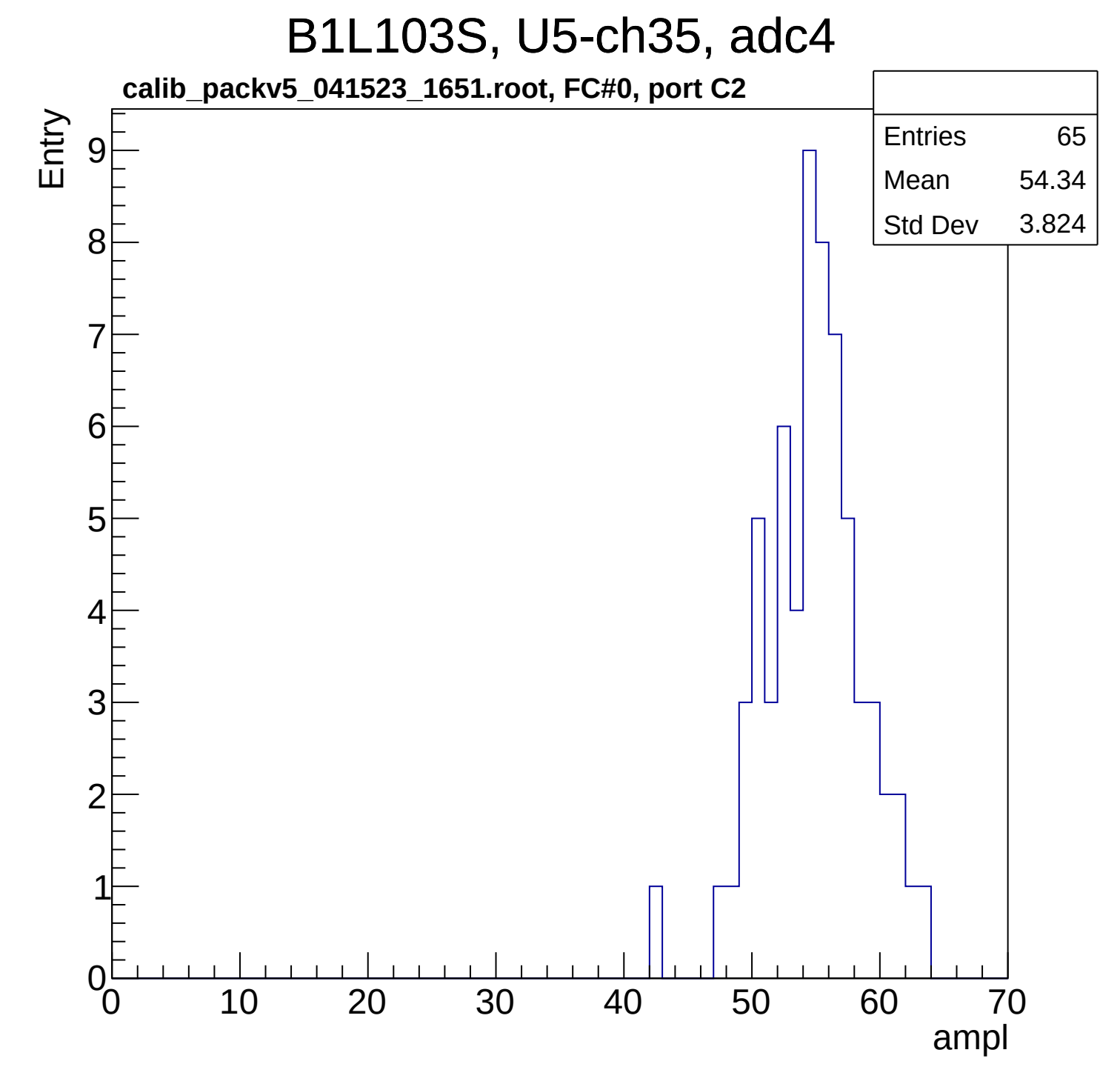
B1L103S, U5-ch35, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 54.34
Std Dev 3.824
Entry
ampl
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3
4
5
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0
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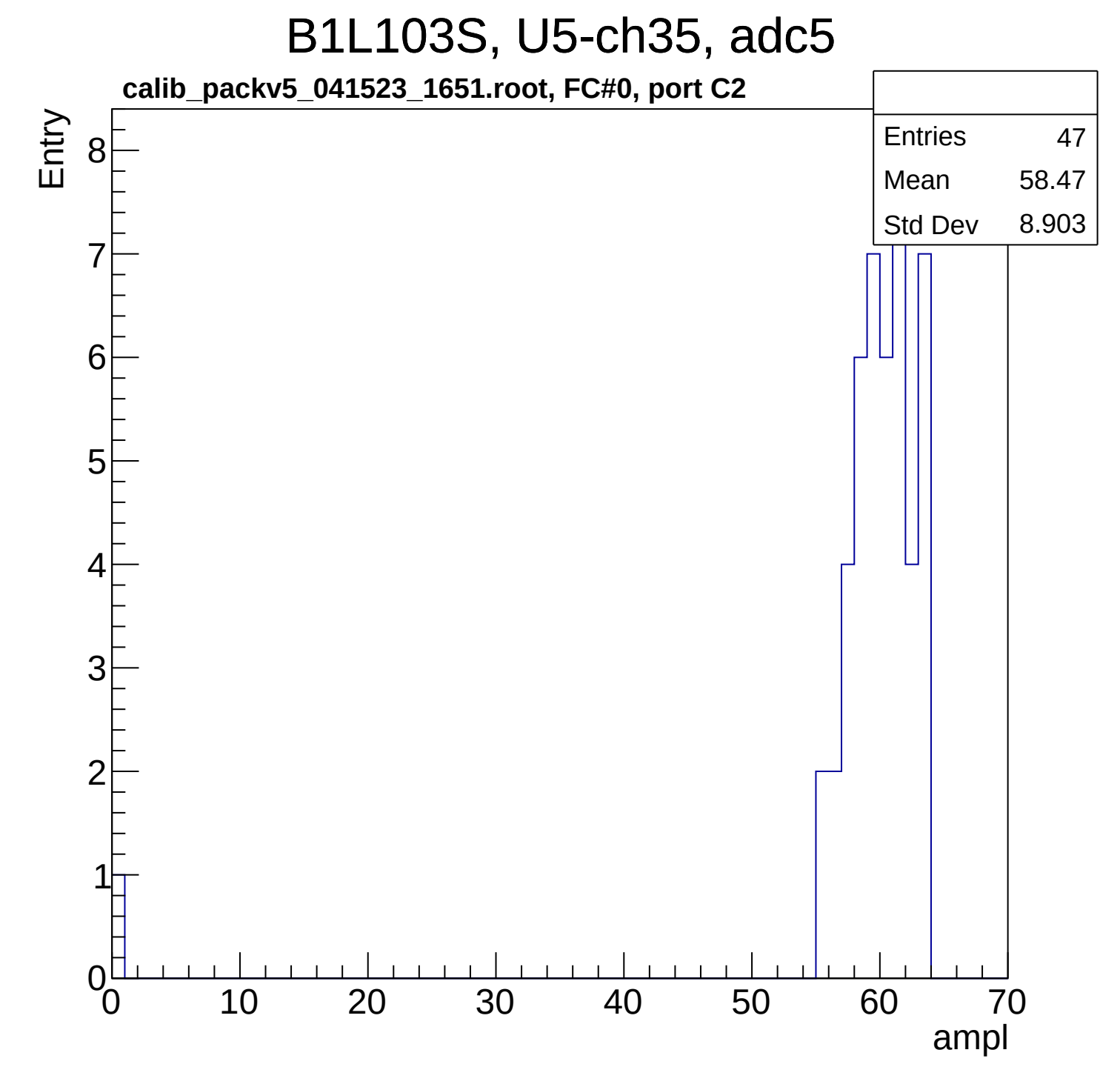
B1L103S, U5-ch35, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.47
Std Dev 8.903
Entry
ampl
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1
2
3
4
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7
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0
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60
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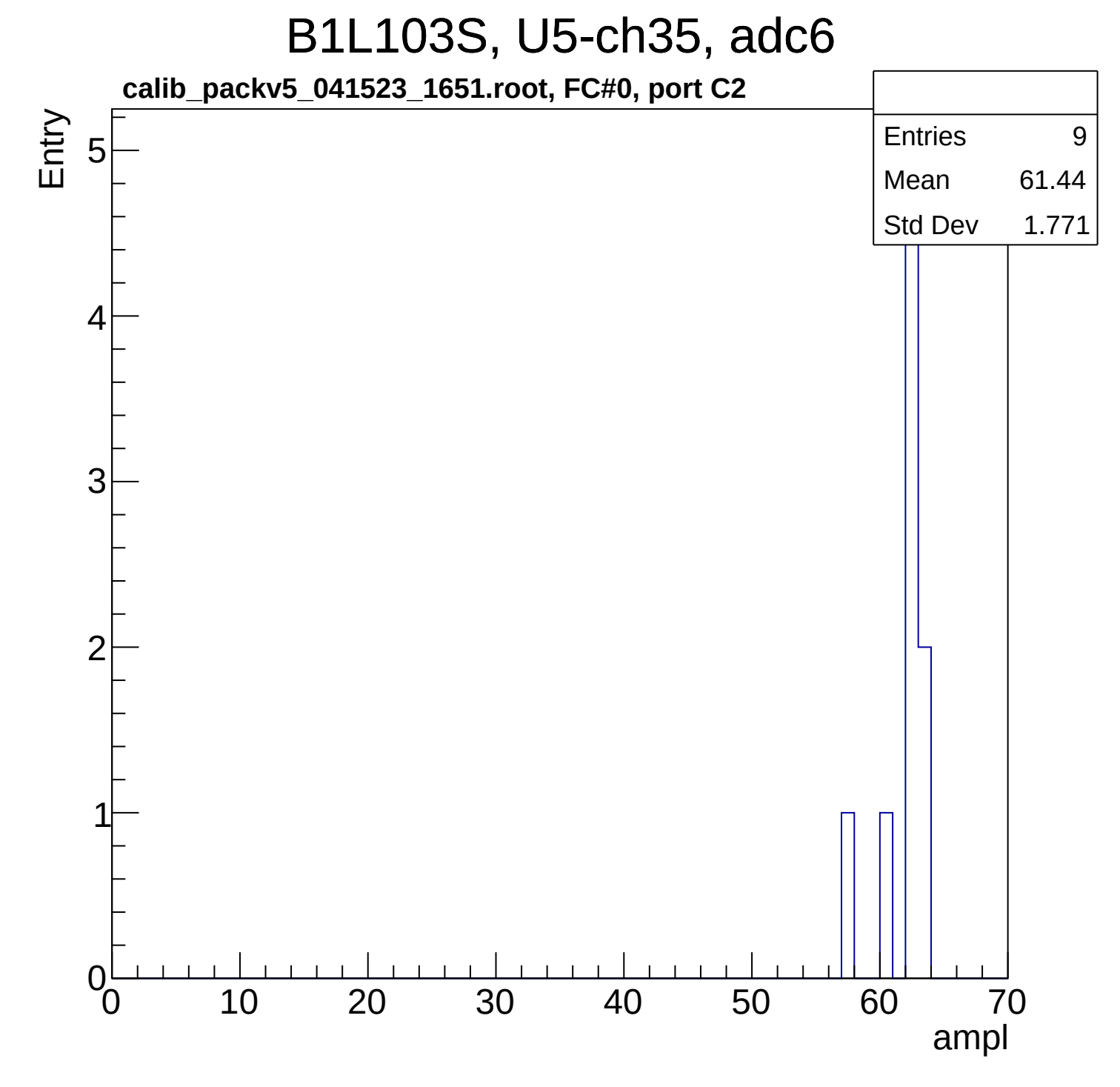
B1L103S, U5-ch35, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.44
Std Dev 1.771
Entry
ampl
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3
4
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0
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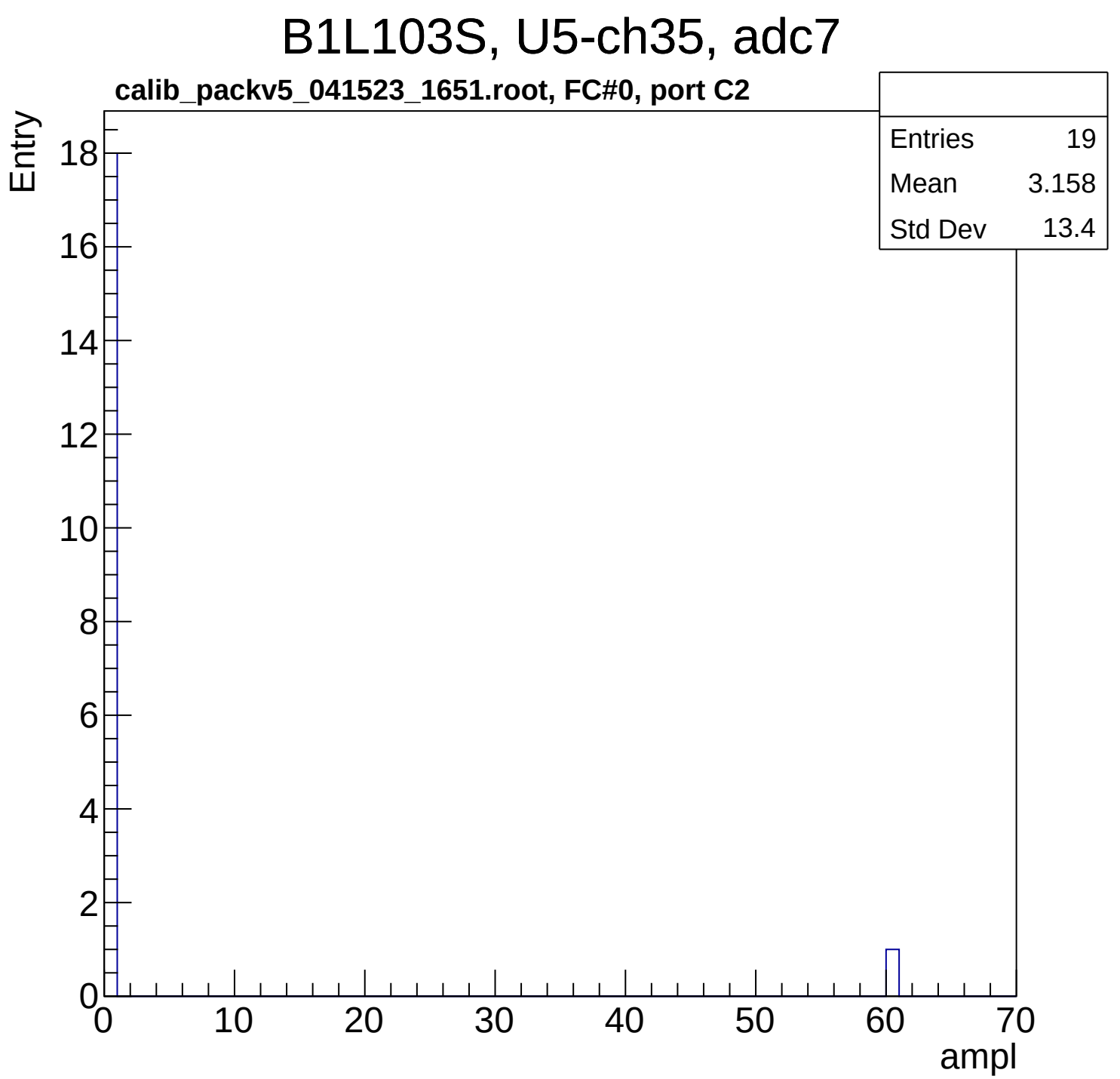
B1L103S, U5-ch35, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.158
Std Dev 13.4
Entry
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6
8
10
12
14
16
18
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10
20
30
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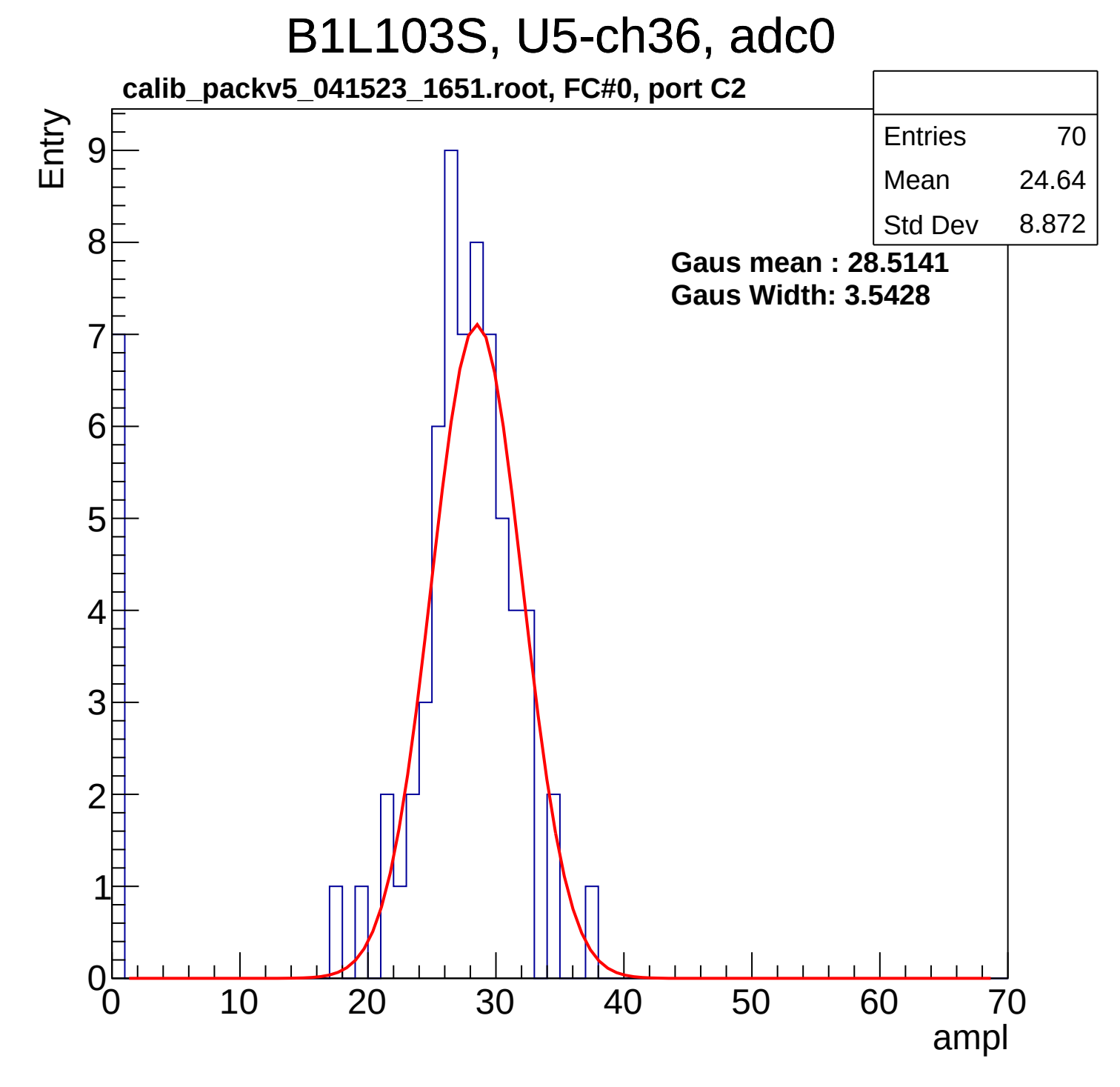
50
60
70
ampl


B1L103S, U5-ch36, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 24.64
Std Dev 8.872
Gaus mean : 28.5141
Gaus Width: 3.5428
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
50
60
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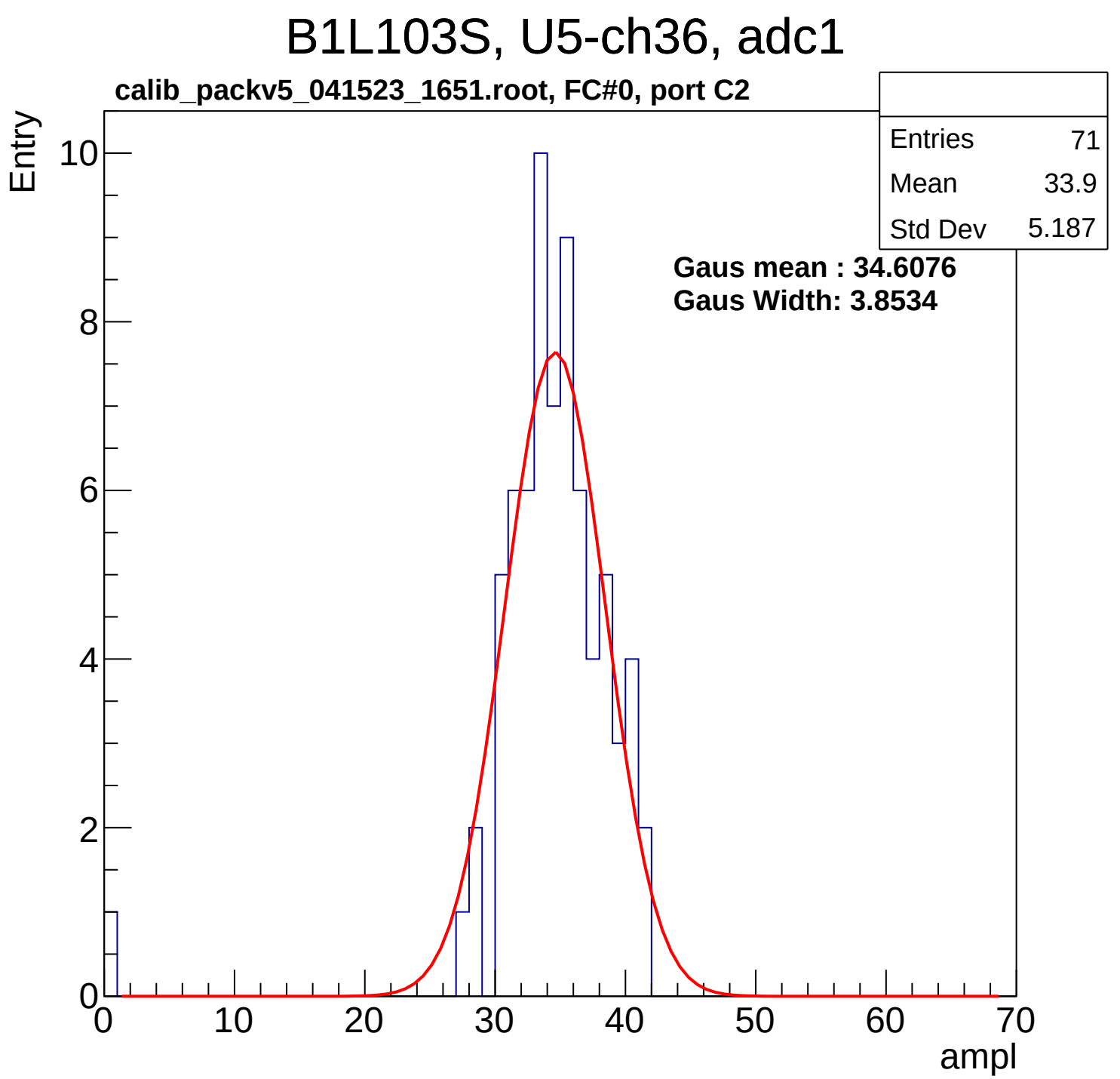
B1L103S, U5-ch36, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 33.9
Std Dev 5.187
Gaus mean : 34.6076
Gaus Width: 3.8534
Entry
ampl
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4
6
8
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0
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20
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40
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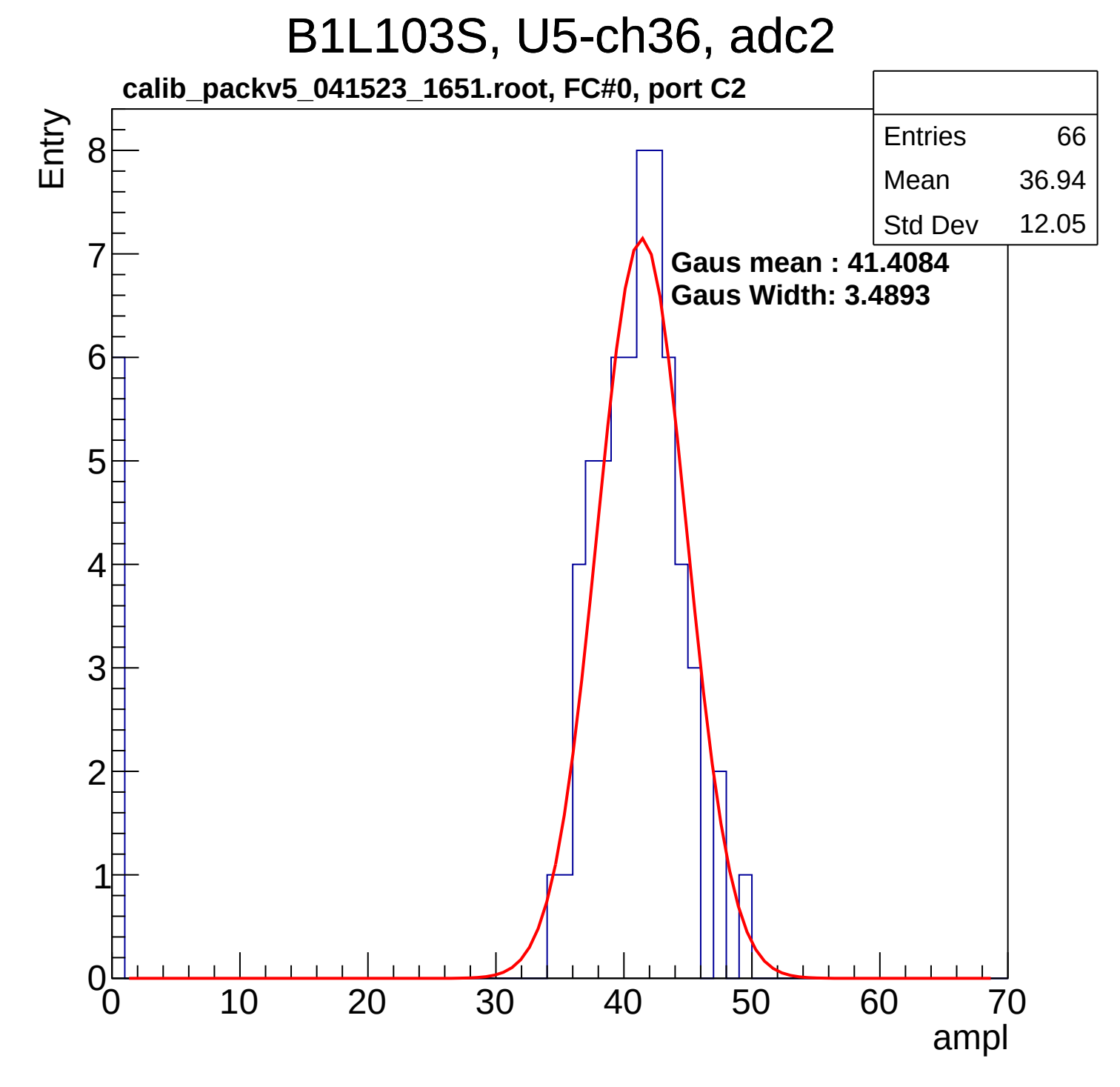
B1L103S, U5-ch36, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 36.94
Std Dev 12.05
Gaus mean : 41.4084
Gaus Width: 3.4893
Entry
ampl
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1
2
3
4
5
6
7
8
0
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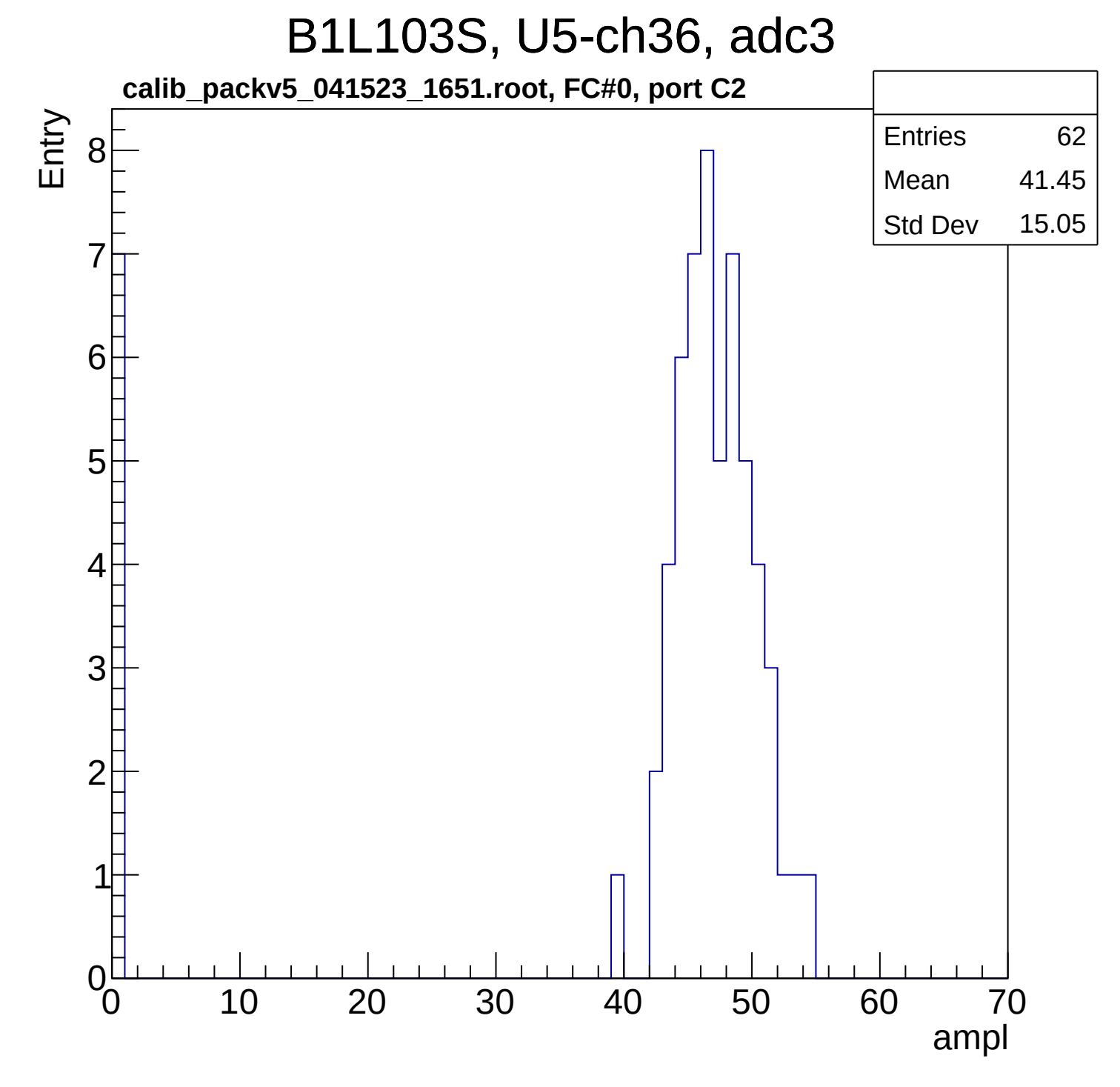
B1L103S, U5-ch36, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 41.45
Std Dev 15.05
Entry
ampl
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4
5
6
7
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0
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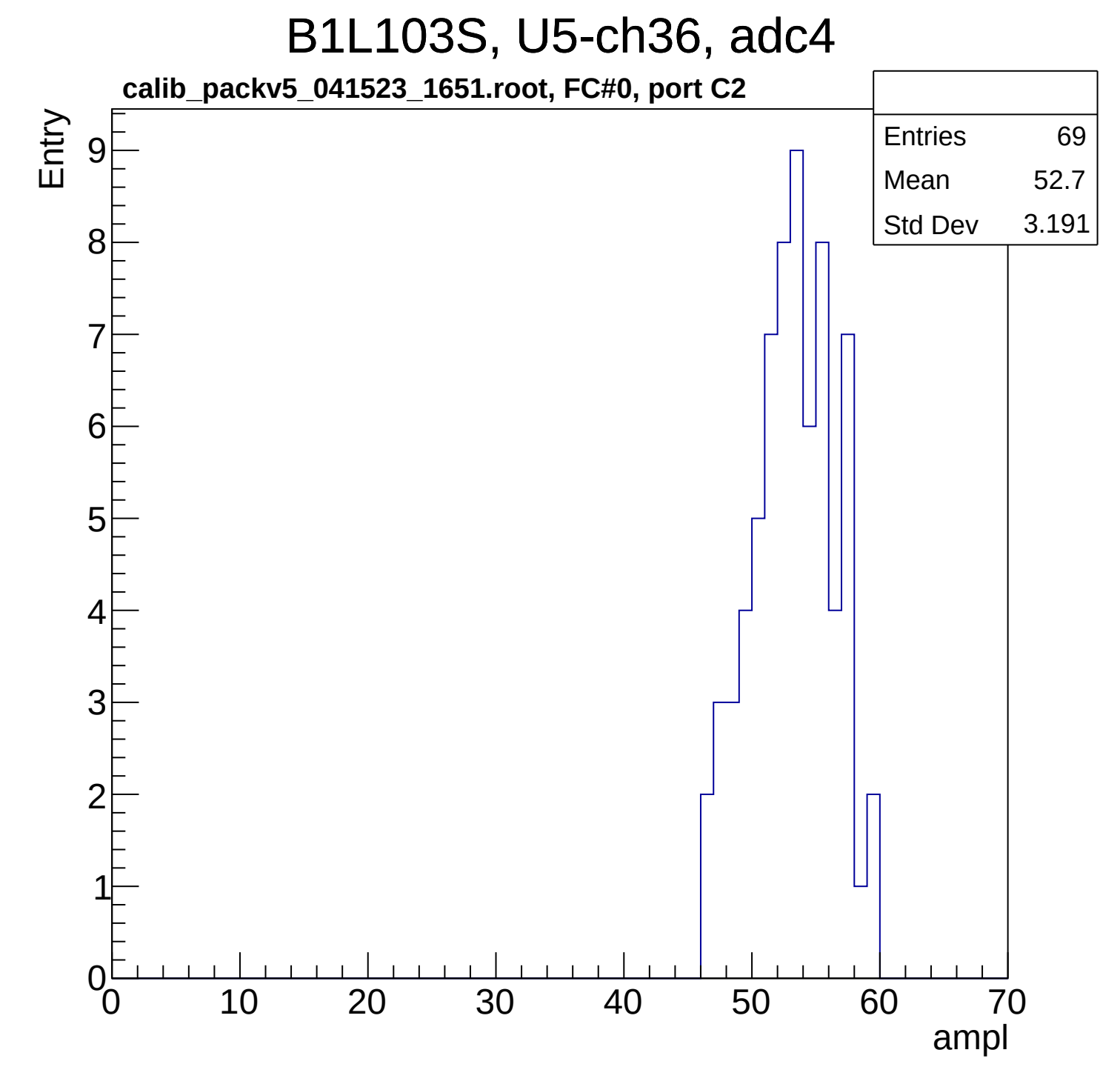
B1L103S, U5-ch36, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 52.7
Std Dev 3.191
Entry
ampl
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5
6
7
8
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0
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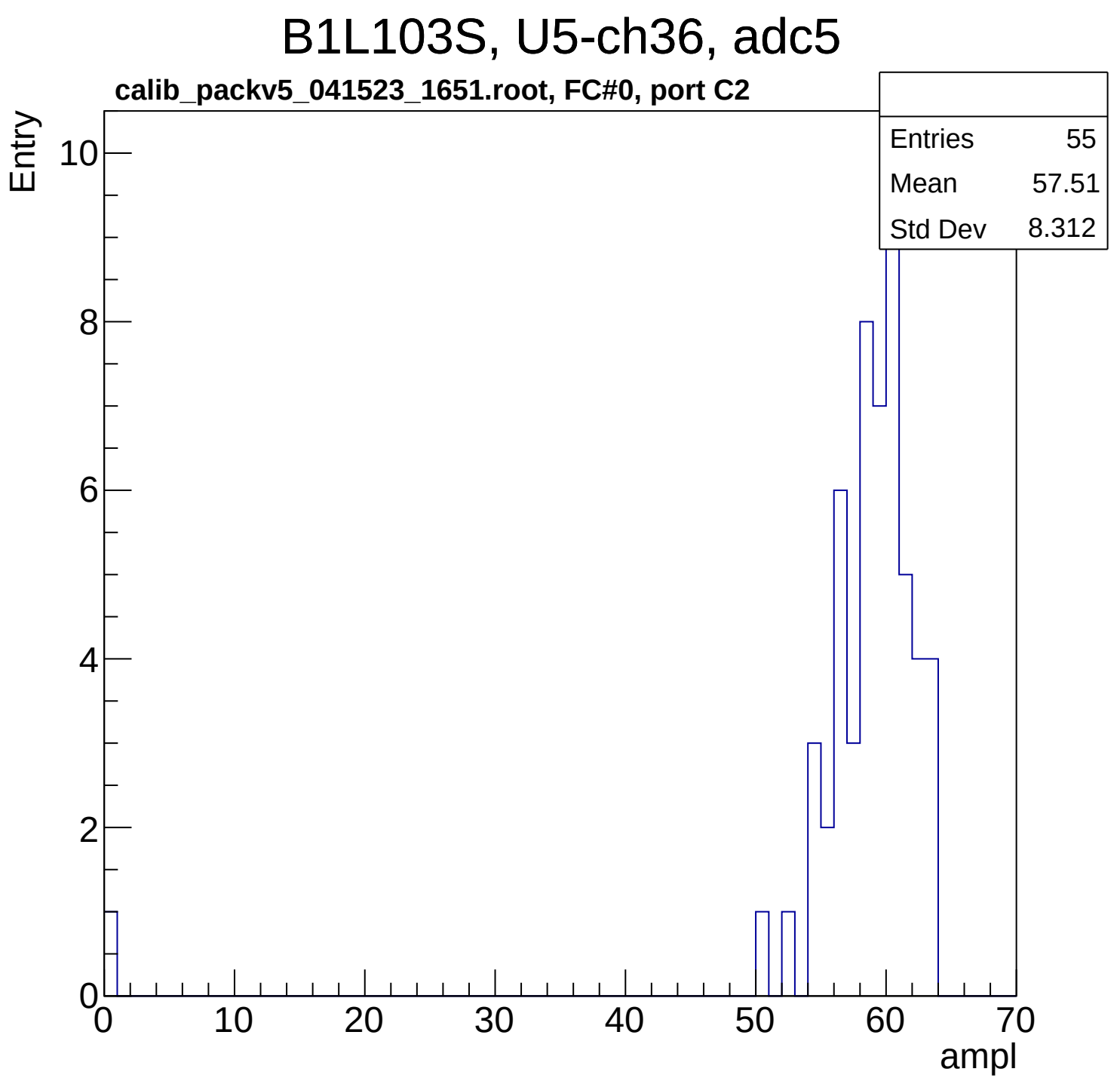
B1L103S, U5-ch36, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.51
Std Dev 8.312
Entry
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6
8
10
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10
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30
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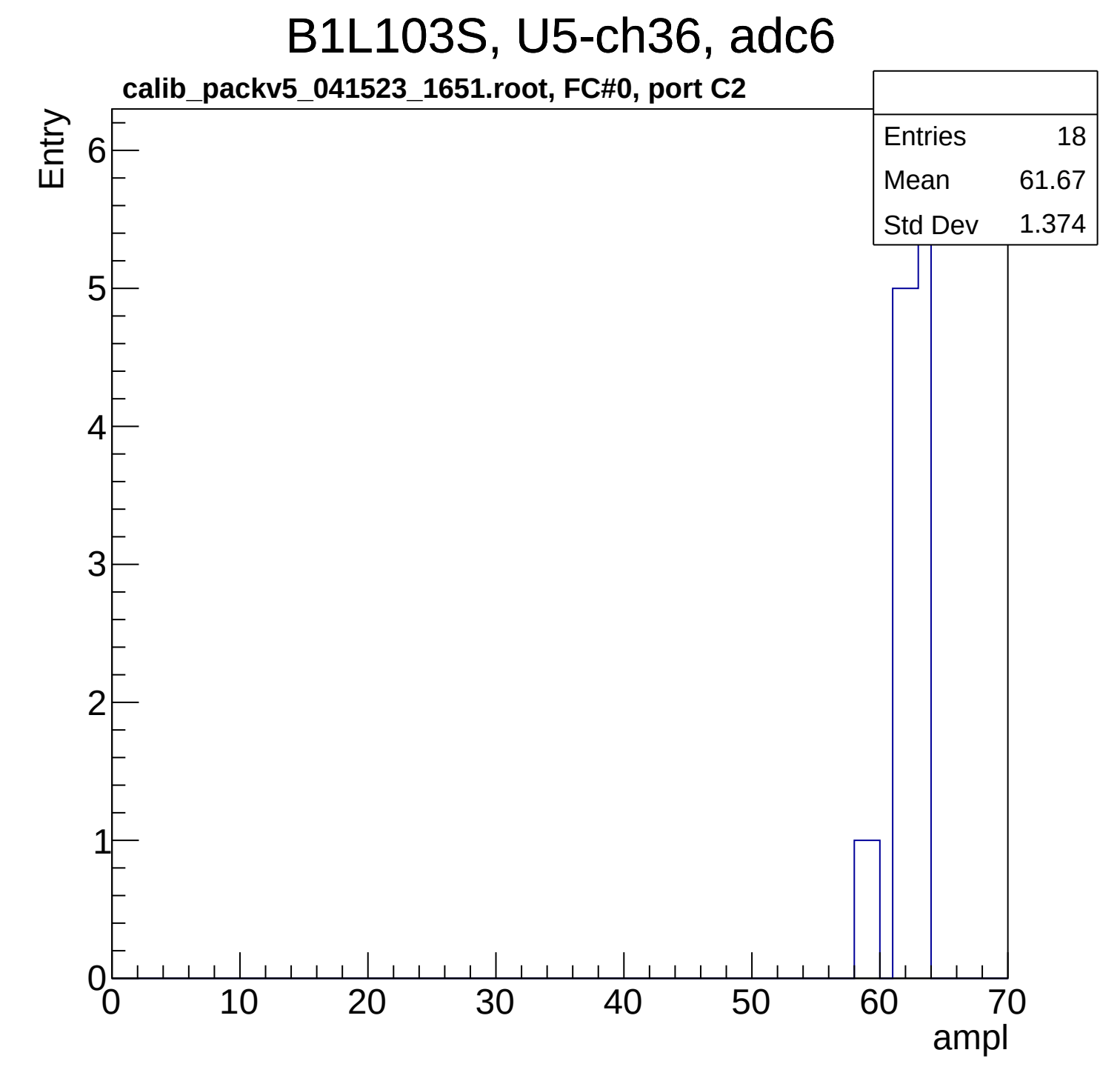
50
60
70
ampl


B1L103S, U5-ch36, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 61.67
Std Dev 1.374
Entry
ampl
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0
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20
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40
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60
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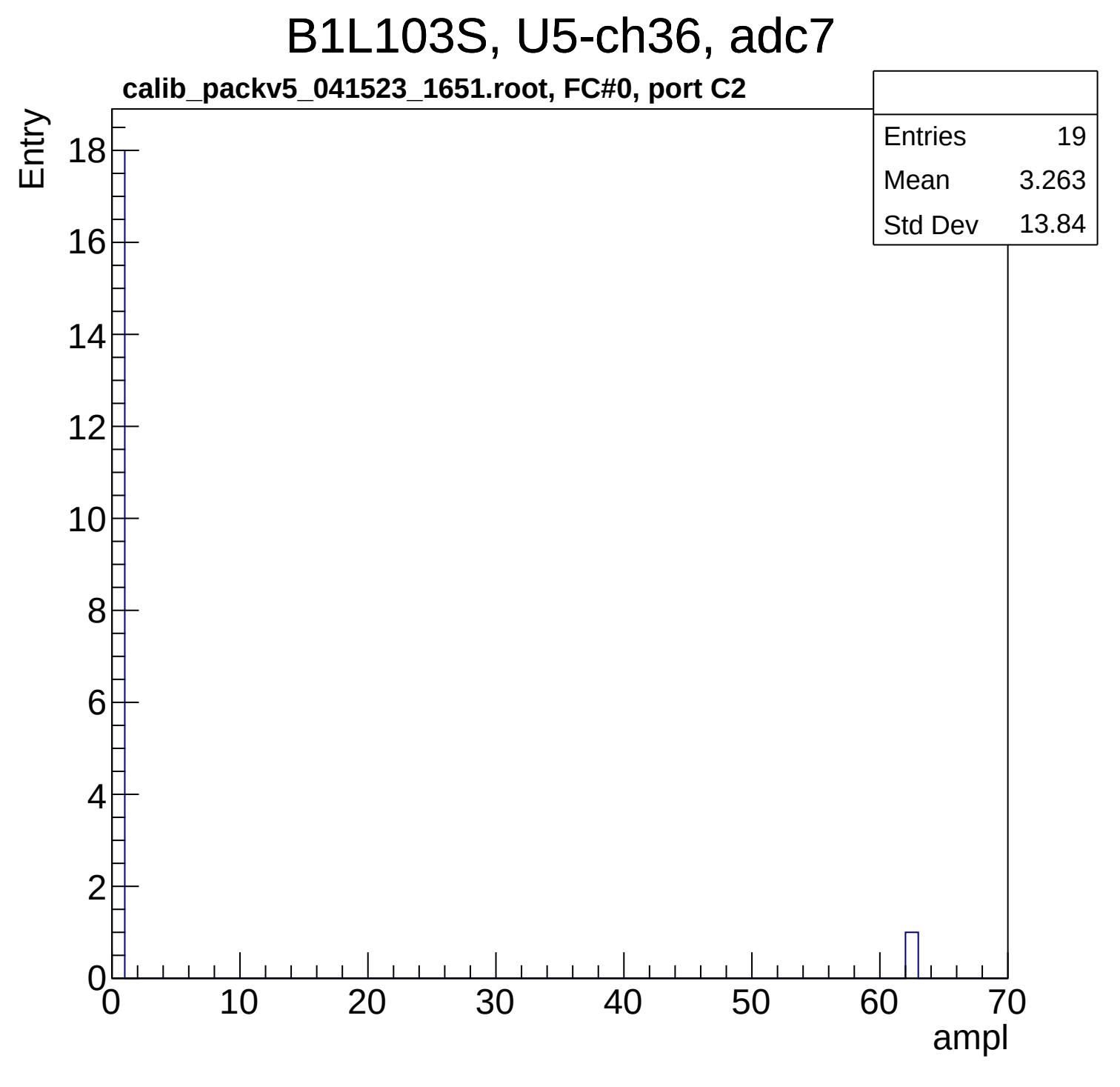
B1L103S, U5-ch36, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.263
Std Dev 13.84
Entry
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14
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18
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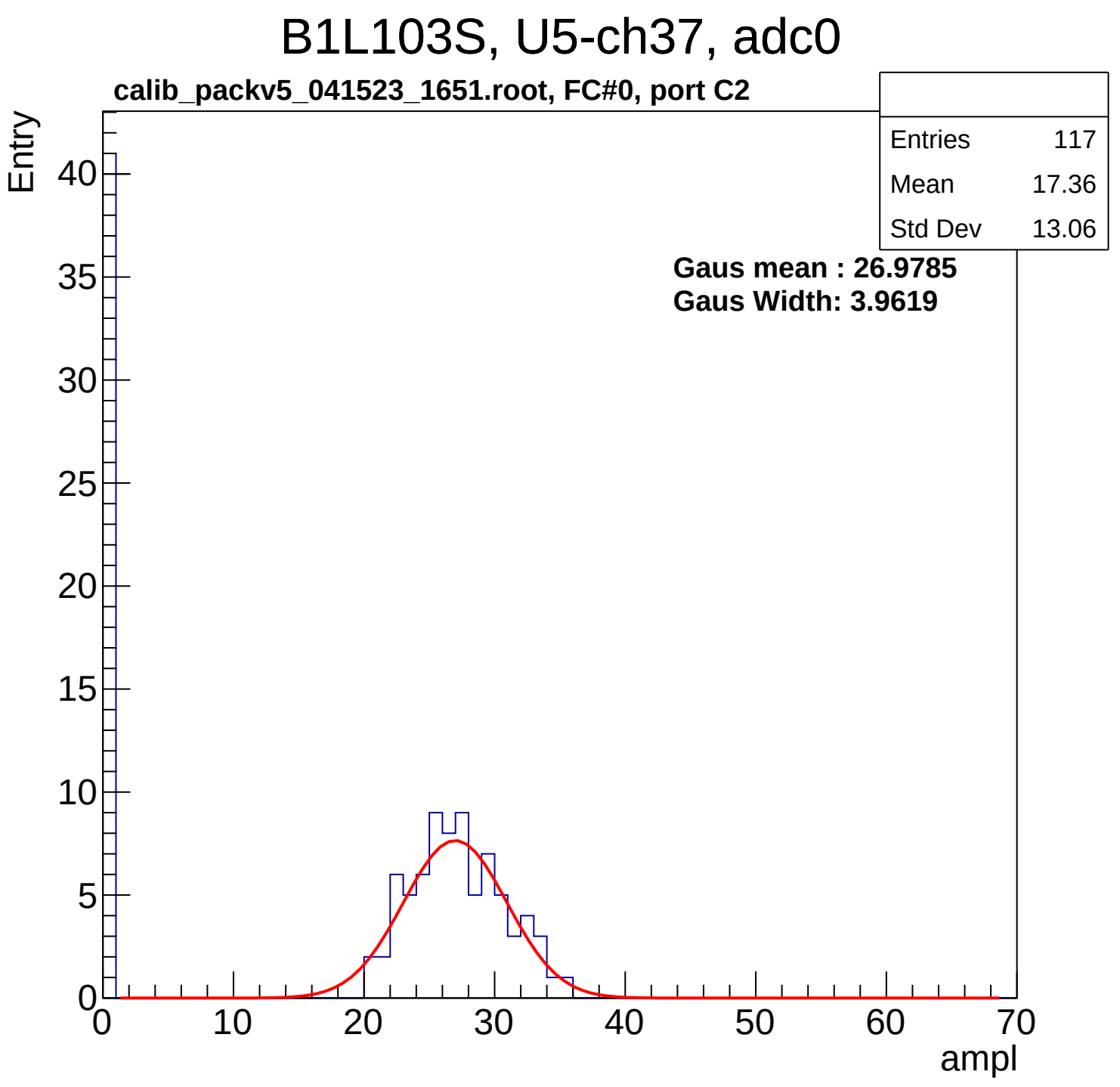
50
60
70
ampl


B1L103S, U5-ch37, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 117
Mean 17.36
Std Dev 13.06
Gaus mean : 26.9785
Gaus Width: 3.9619
Entry
ampl
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15
20
25
30
35
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0
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20
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40
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60
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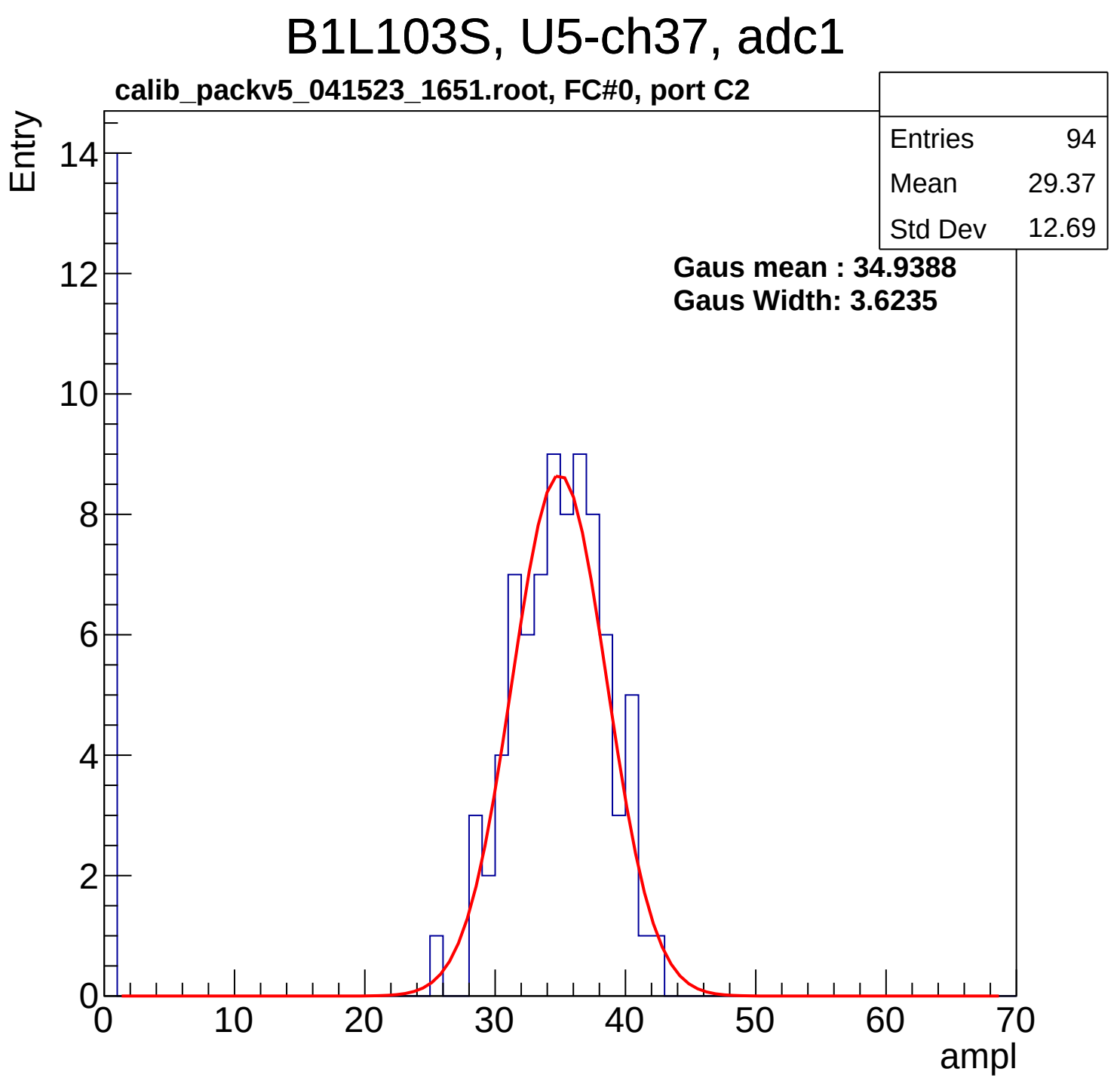
B1L103S, U5-ch37, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 29.37
Std Dev 12.69
Gaus mean : 34.9388
Gaus Width: 3.6235
Entry
ampl
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6
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12
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0
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20
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40
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60
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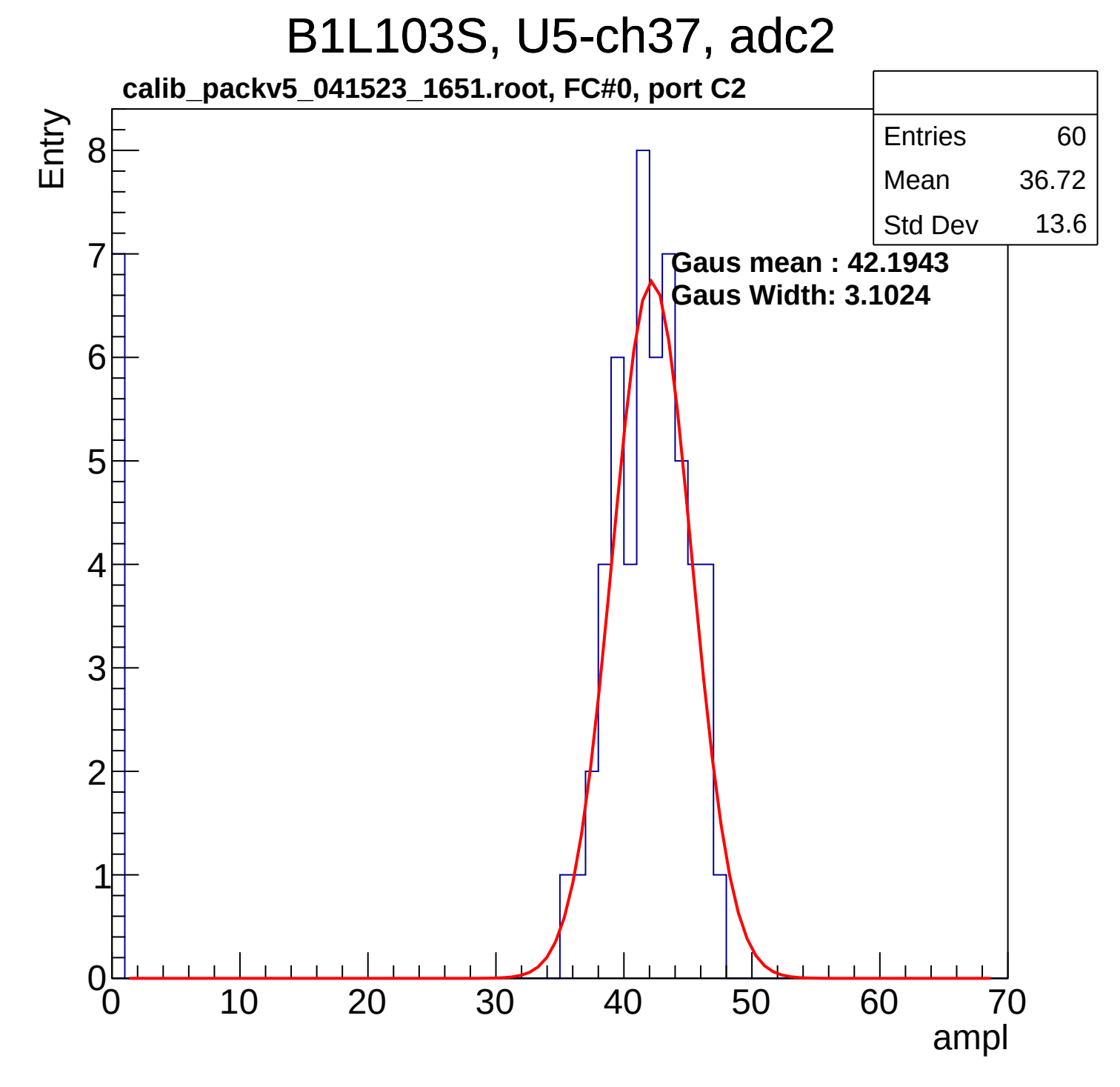
B1L103S, U5-ch37, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 36.72
Std Dev 13.6
Gaus mean : 42.1943
Gaus Width: 3.1024
Entry
ampl
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5
6
7
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0
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20
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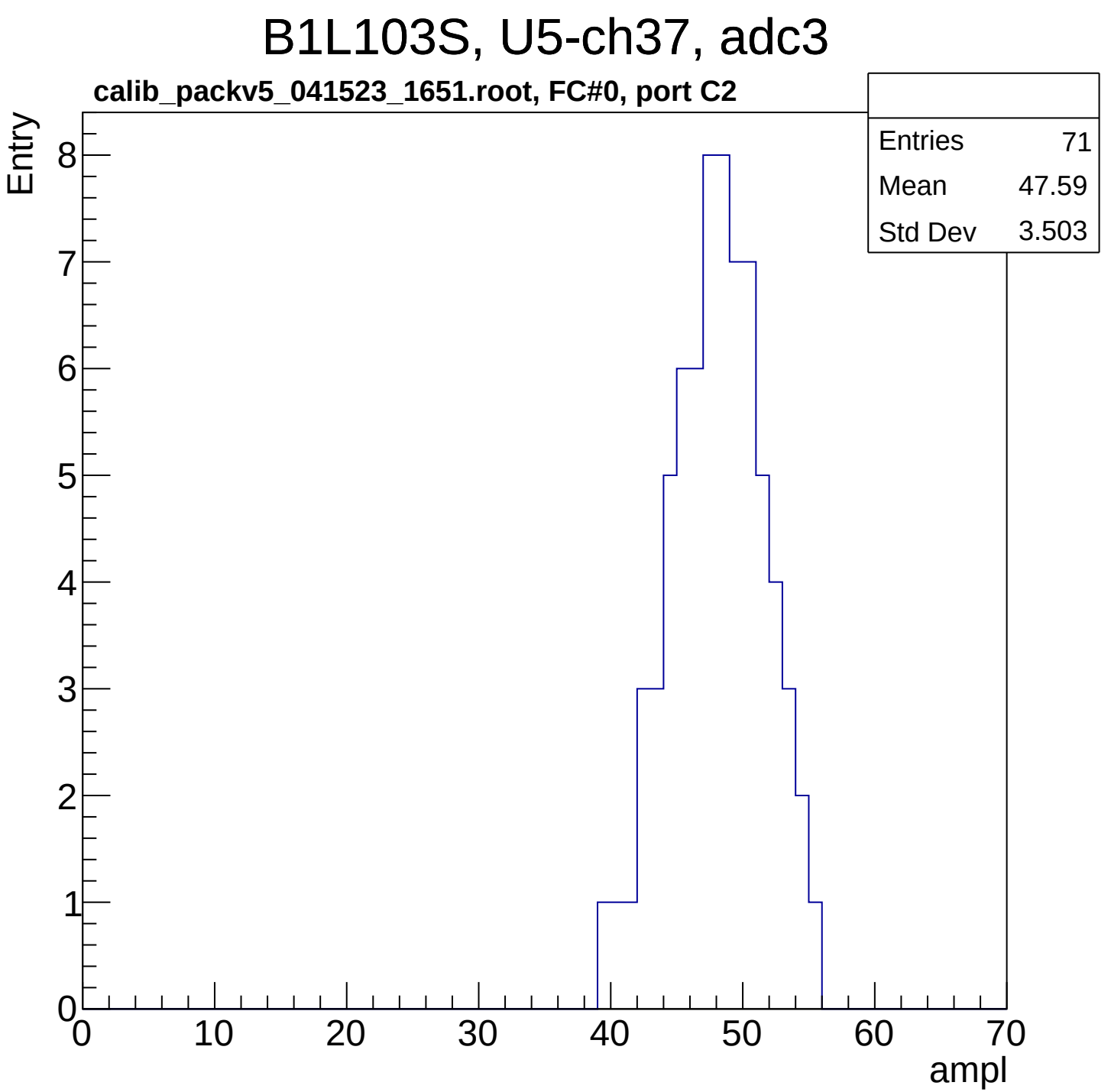
B1L103S, U5-ch37, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 47.59
Std Dev 3.503
Entry
ampl
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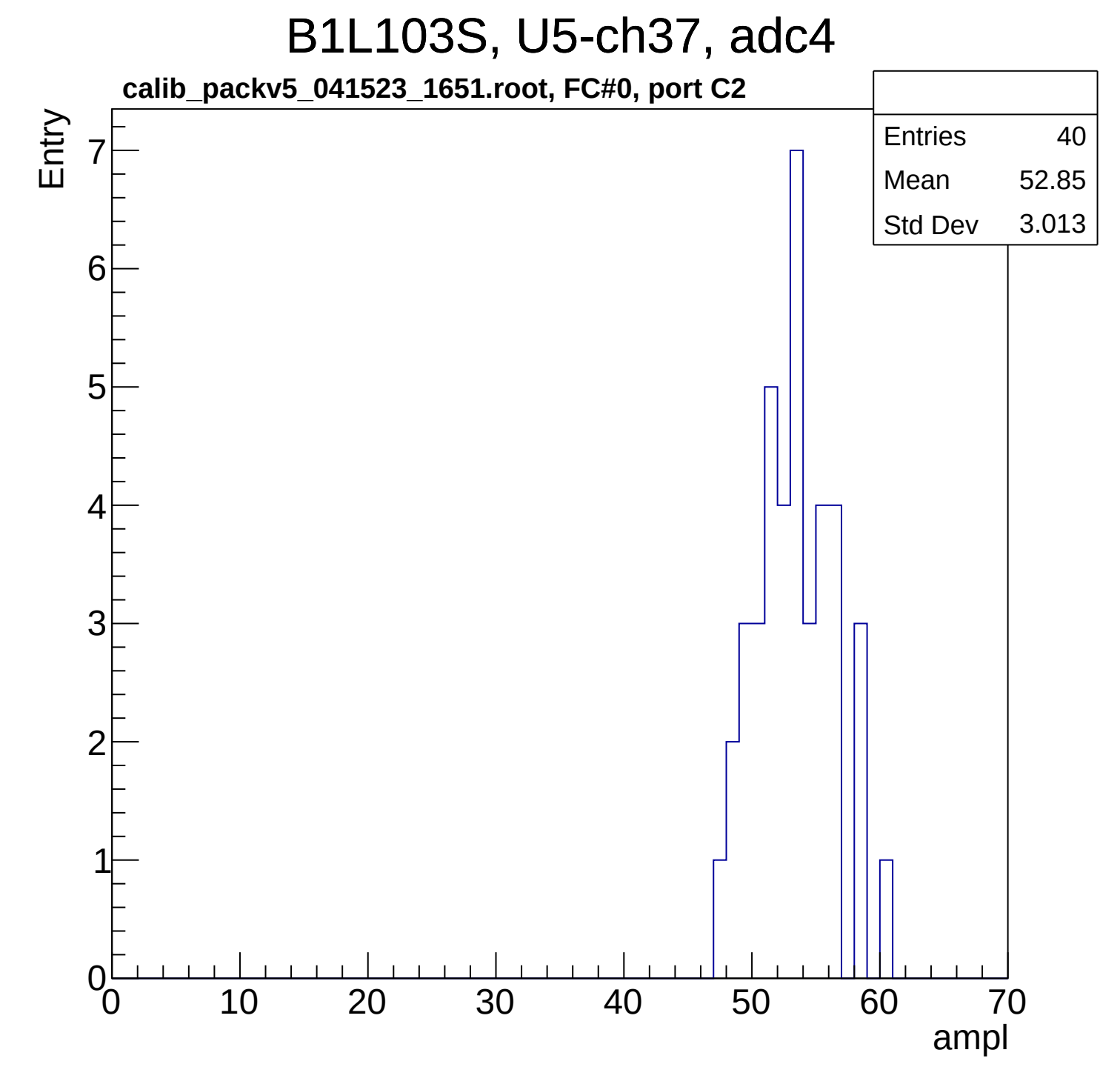
B1L103S, U5-ch37, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 52.85
Std Dev 3.013
Entry
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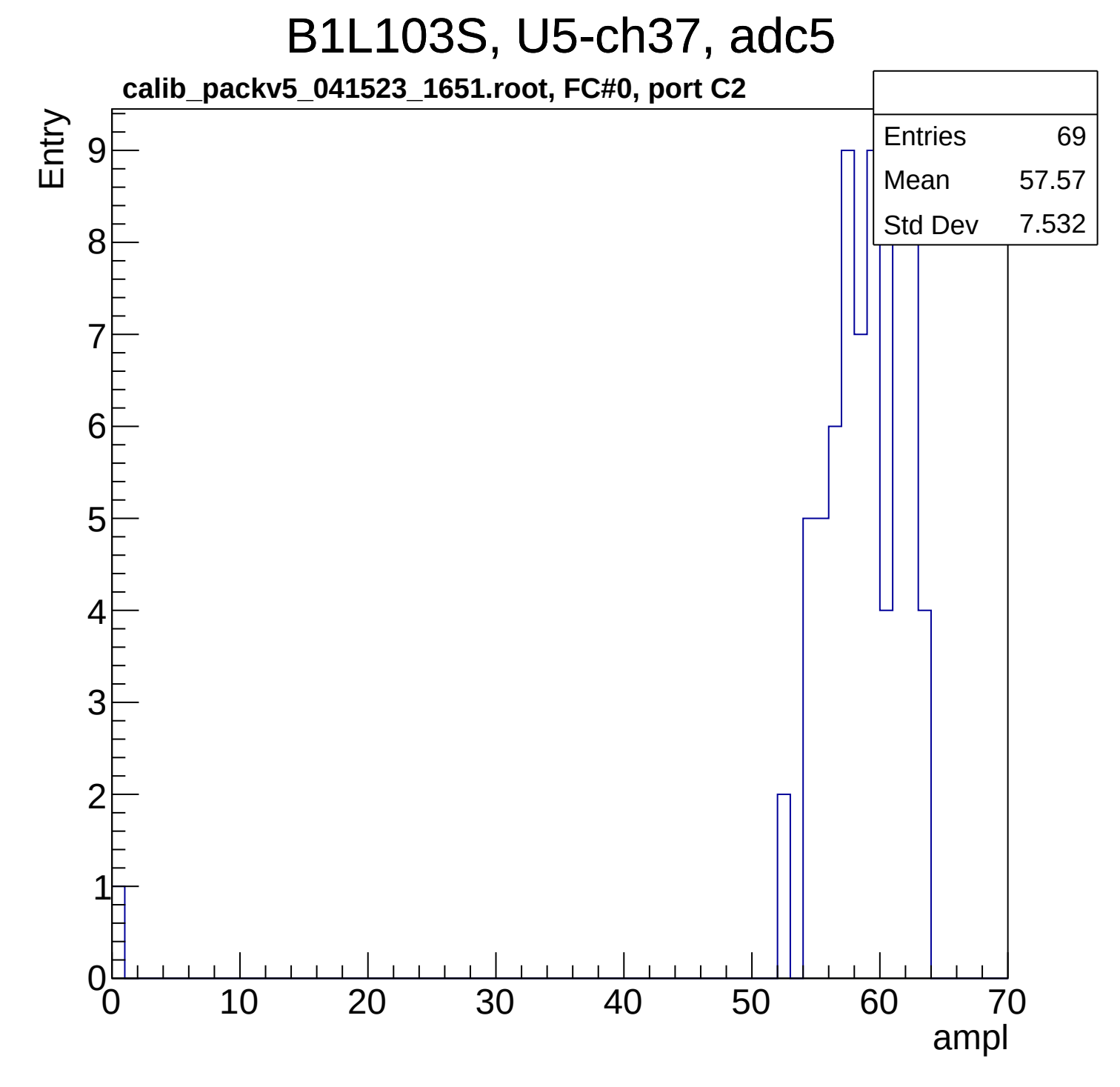
B1L103S, U5-ch37, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 57.57
Std Dev 7.532
Entry
ampl
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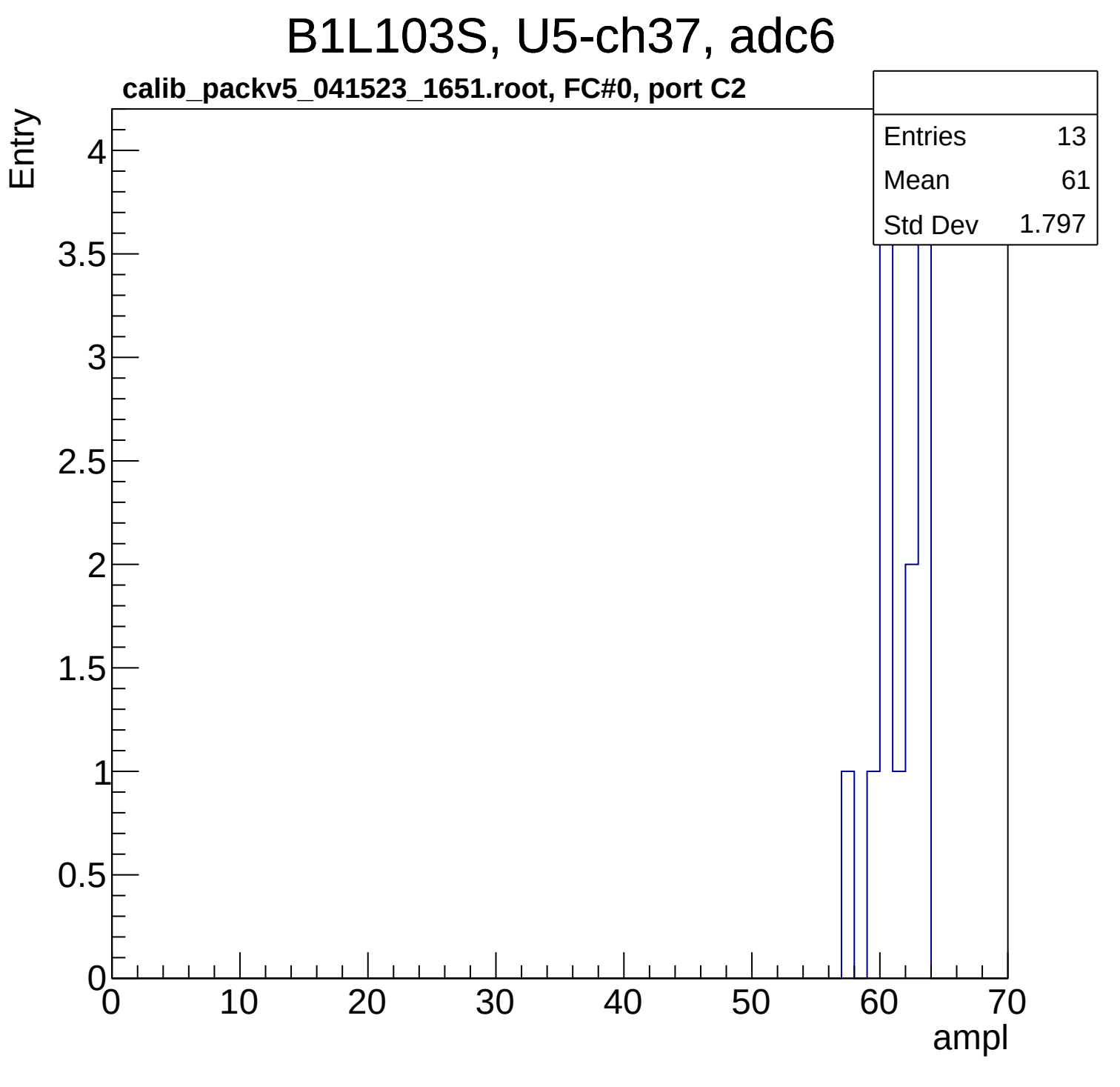
B1L103S, U5-ch37, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61
Std Dev 1.797
Entry
ampl
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1.5
2
2.5
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3.5
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0
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20
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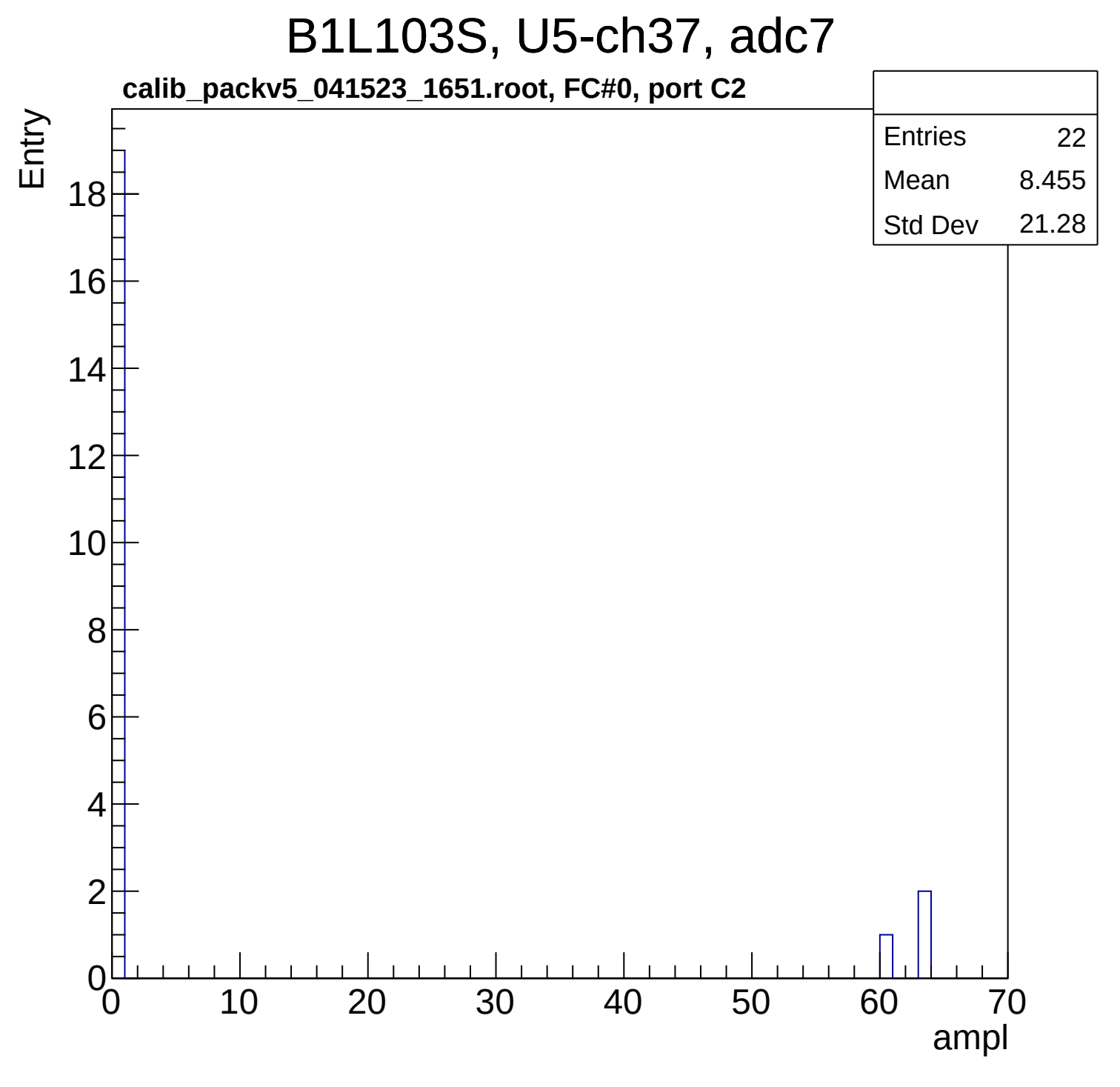
B1L103S, U5-ch37, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.455
Std Dev 21.28
Entry
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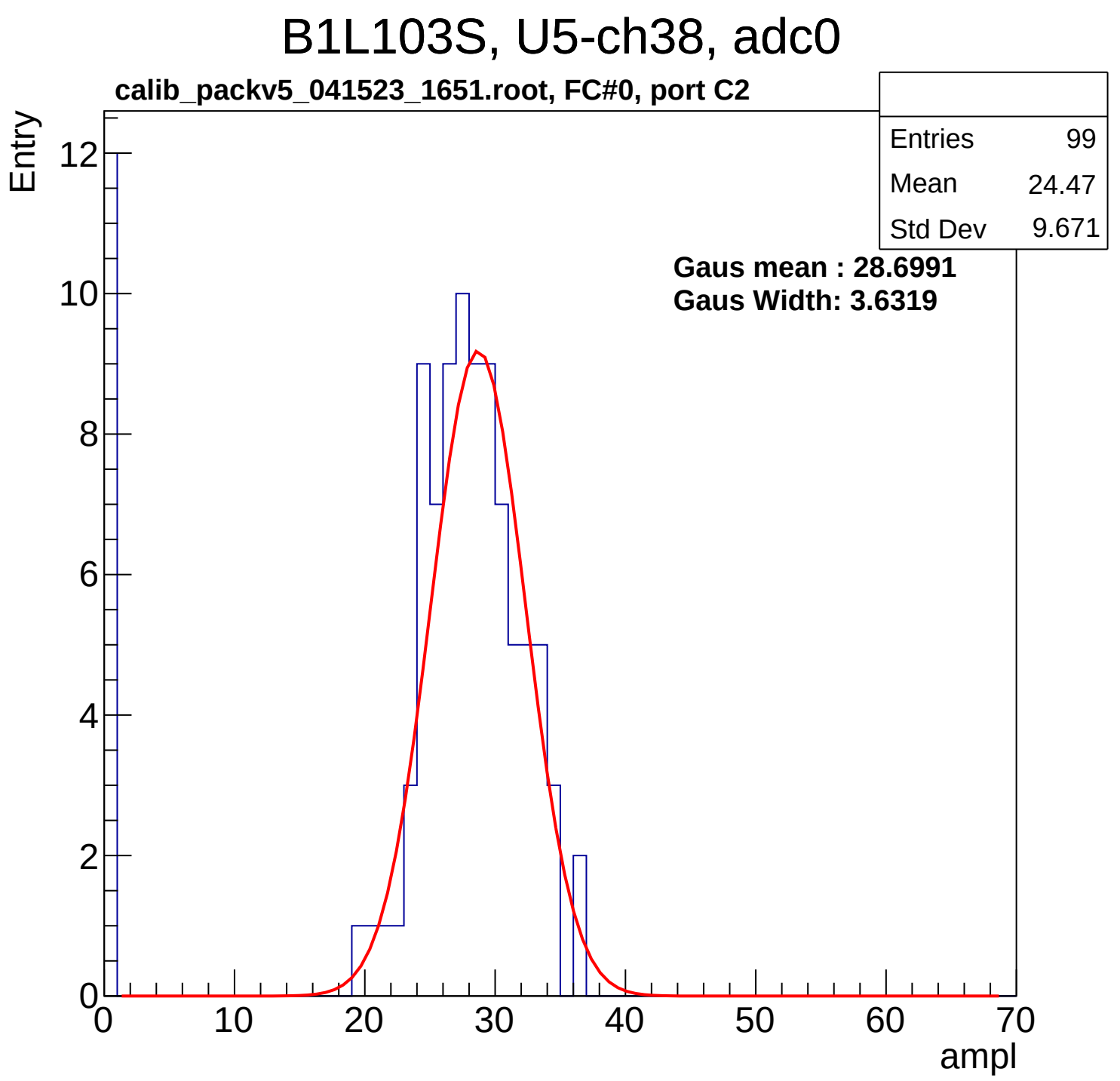
ampl


B1L103S, U5-ch38, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 24.47
Std Dev 9.671
Gaus mean : 28.6991
Gaus Width: 3.6319
Entry
ampl
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6
8
10
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0
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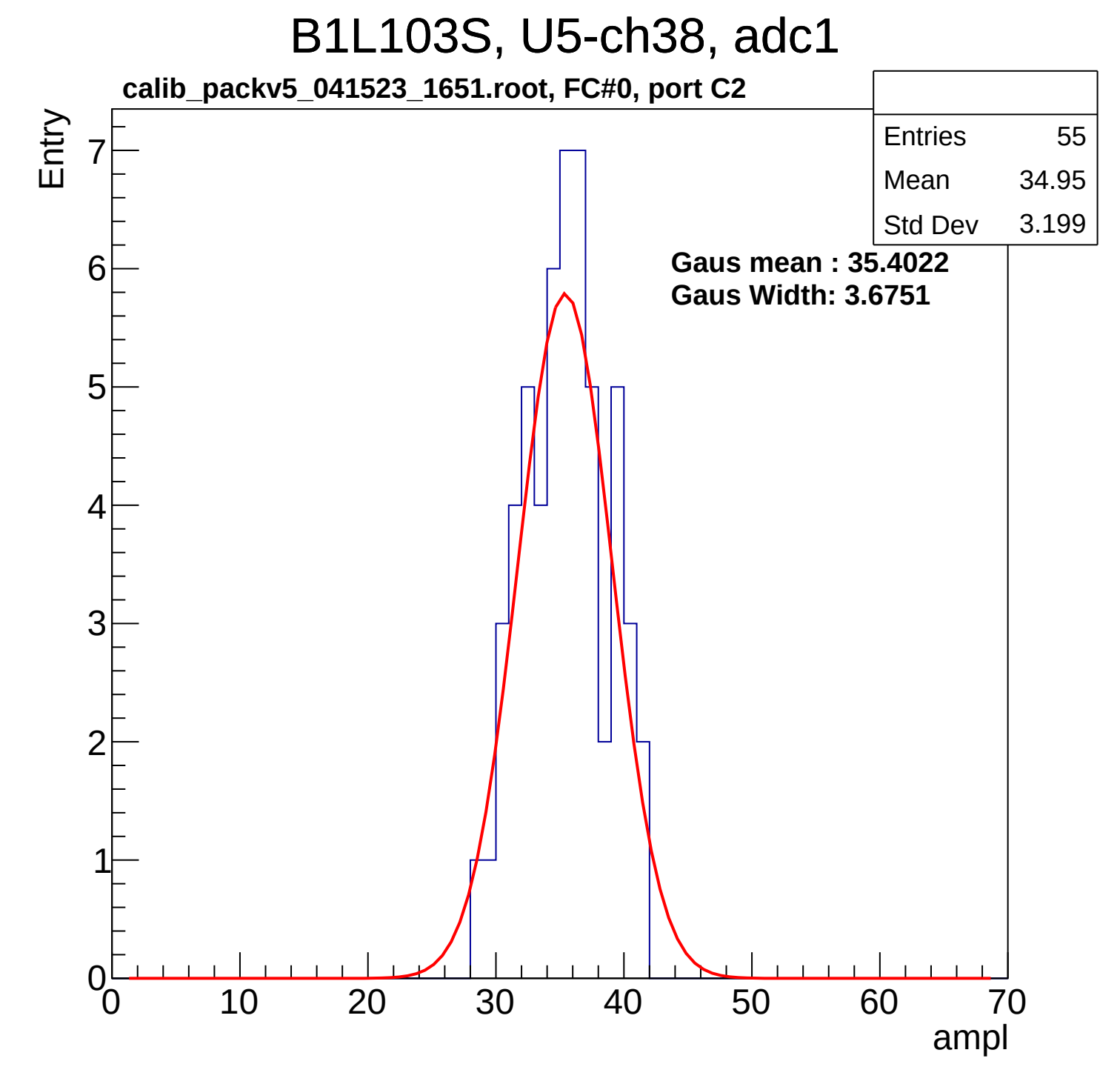
B1L103S, U5-ch38, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 34.95
Std Dev 3.199
Gaus mean : 35.4022
Gaus Width: 3.6751
Entry
ampl
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4
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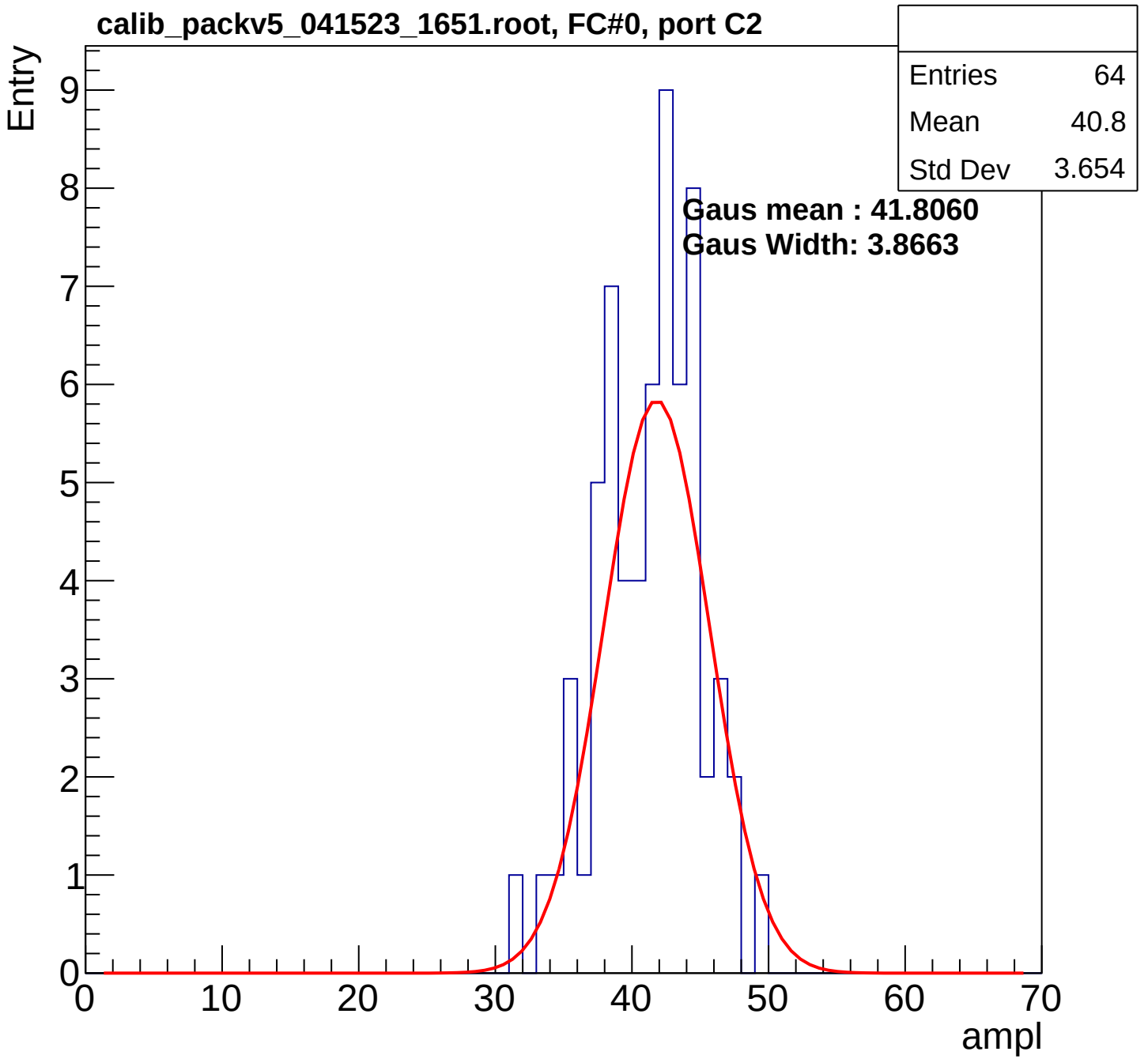
B1L103S, U5-ch38, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 40.8
Std Dev 3.654
Gaus mean : 41.8060
Gaus Width: 3.8663
Entry
ampl
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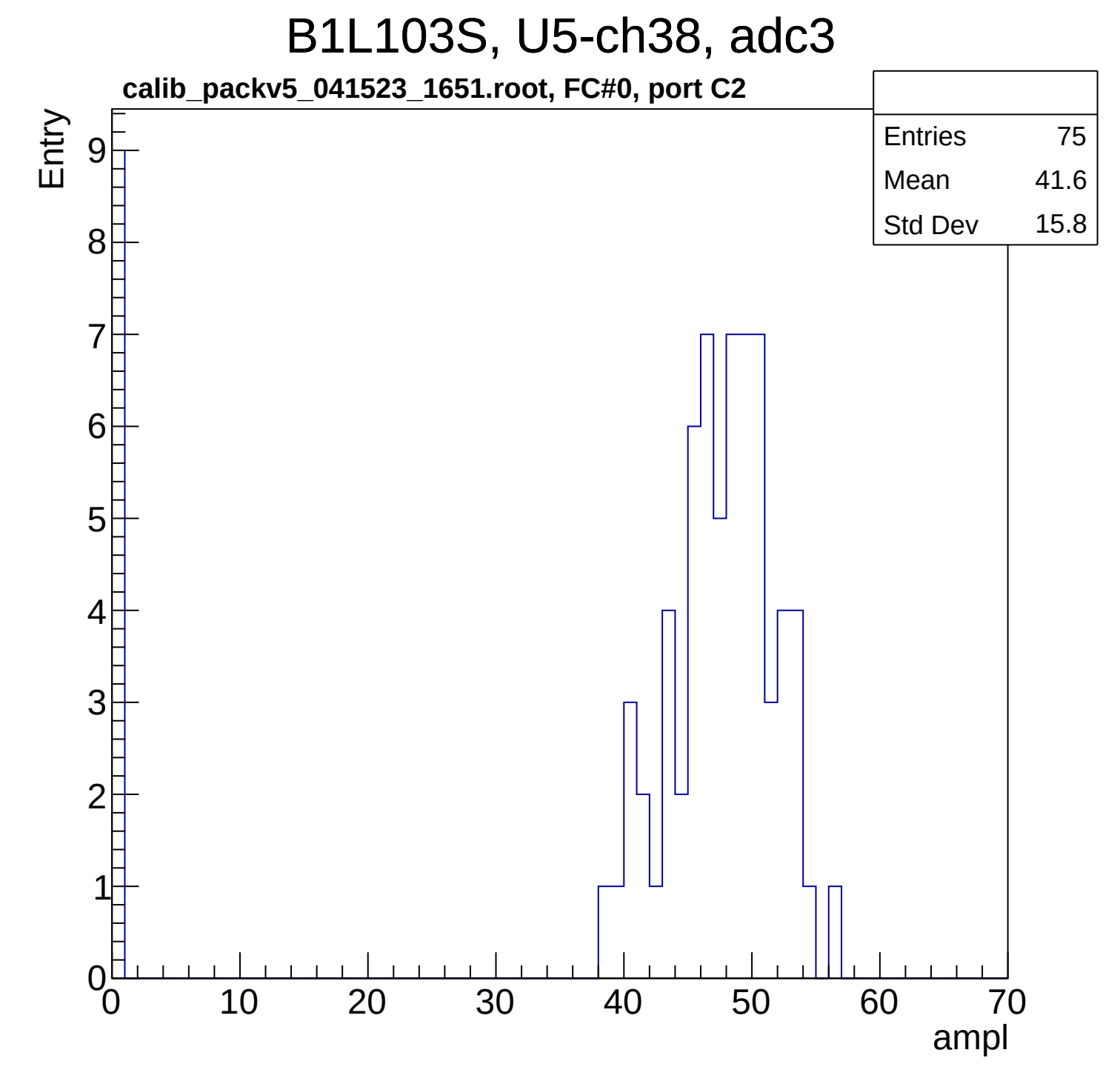
B1L103S, U5-ch38, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 41.6
Std Dev 15.8
Entry
ampl
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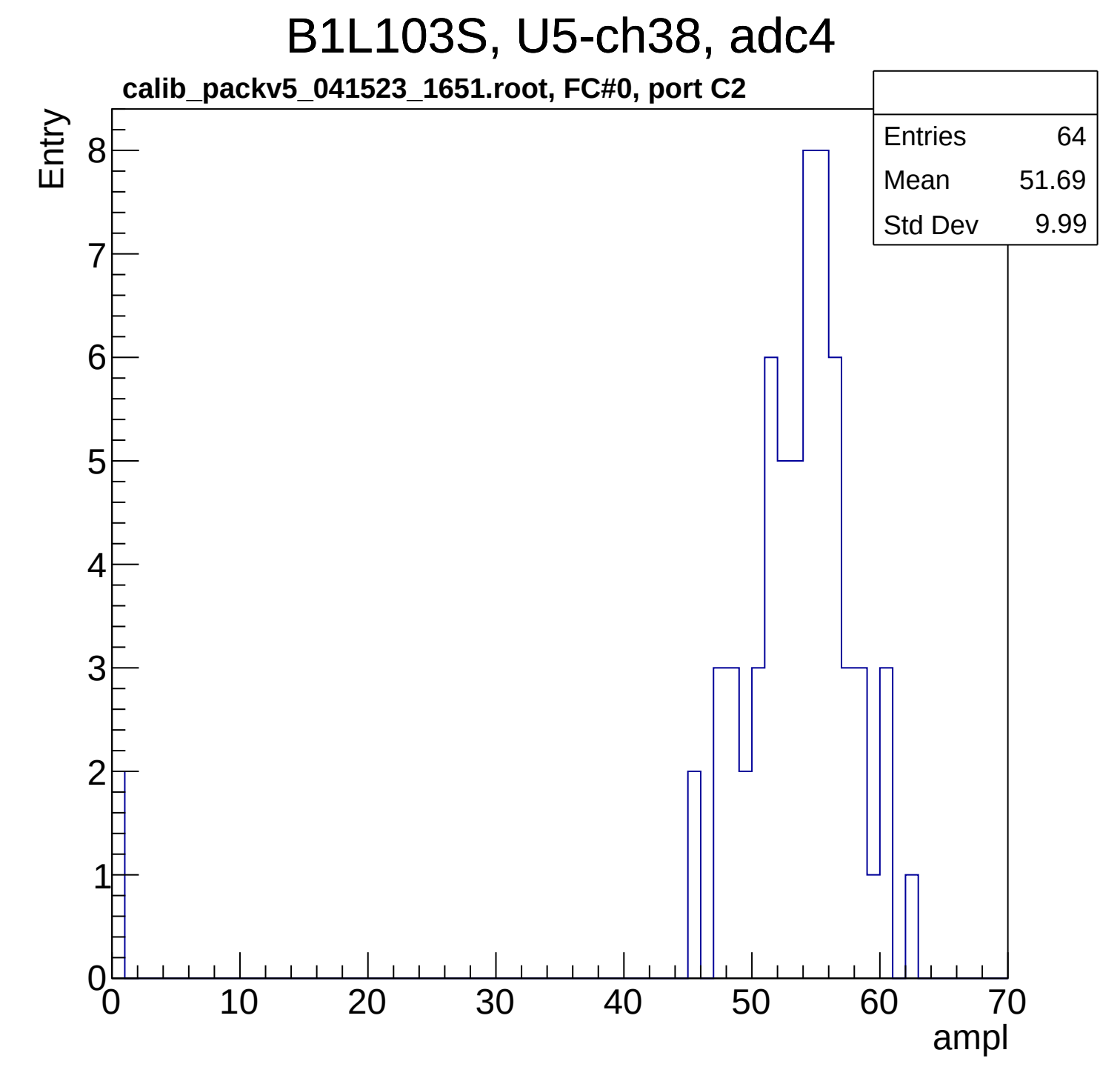
B1L103S, U5-ch38, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 51.69
Std Dev 9.99
Entry
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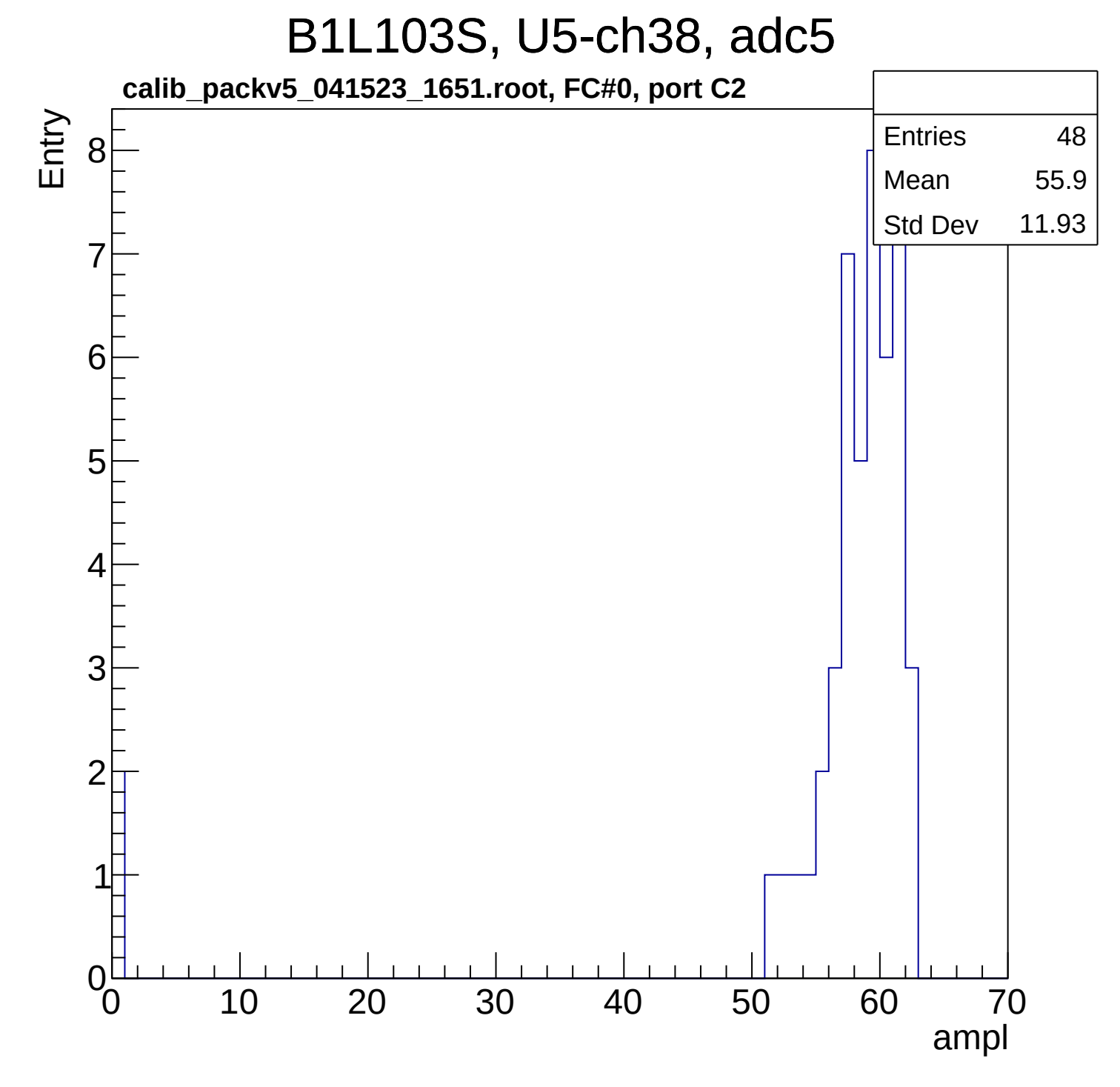
B1L103S, U5-ch38, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 55.9
Std Dev 11.93
Entry
ampl
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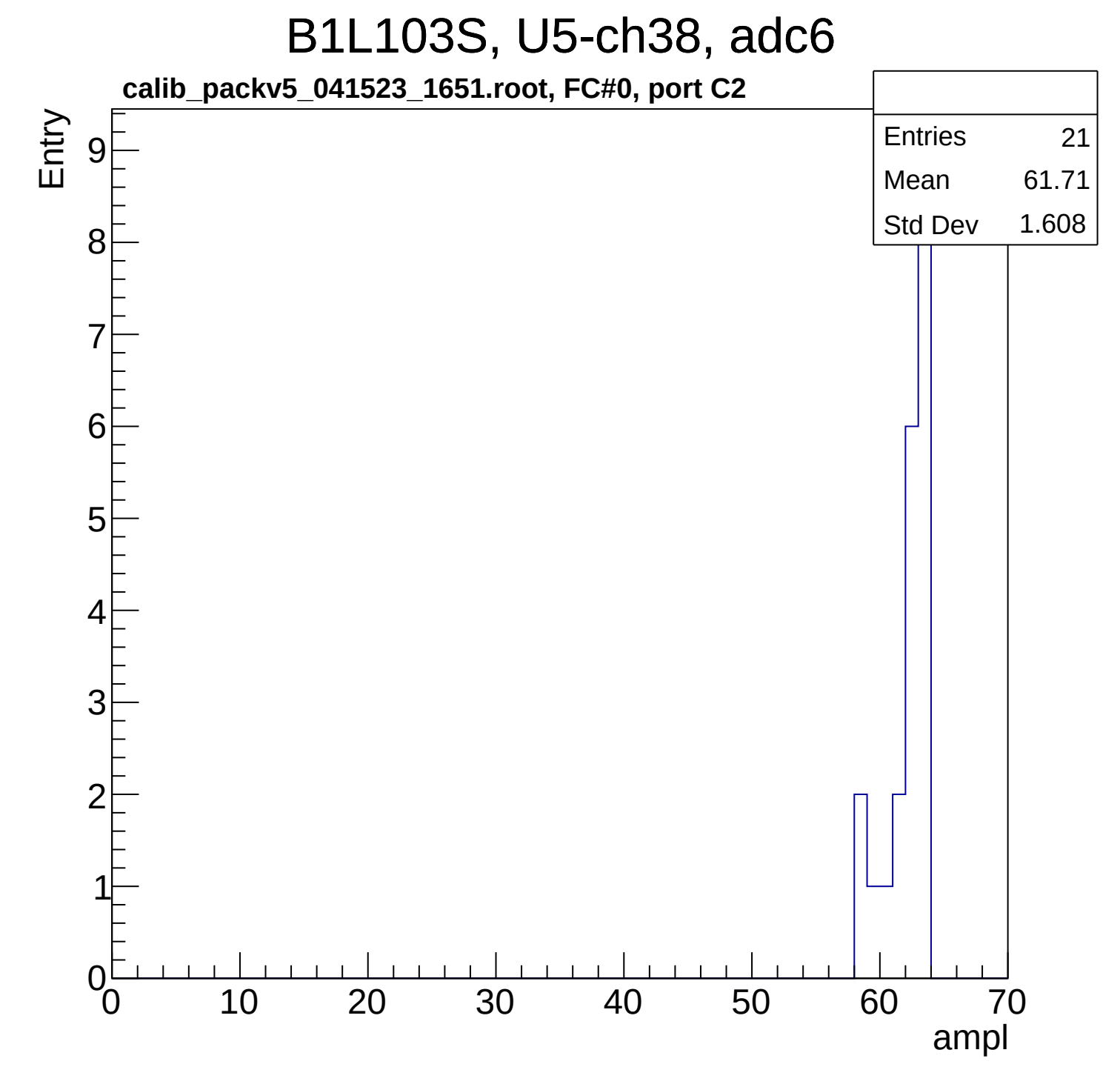
B1L103S, U5-ch38, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 61.71
Std Dev 1.608
Entry
ampl
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3
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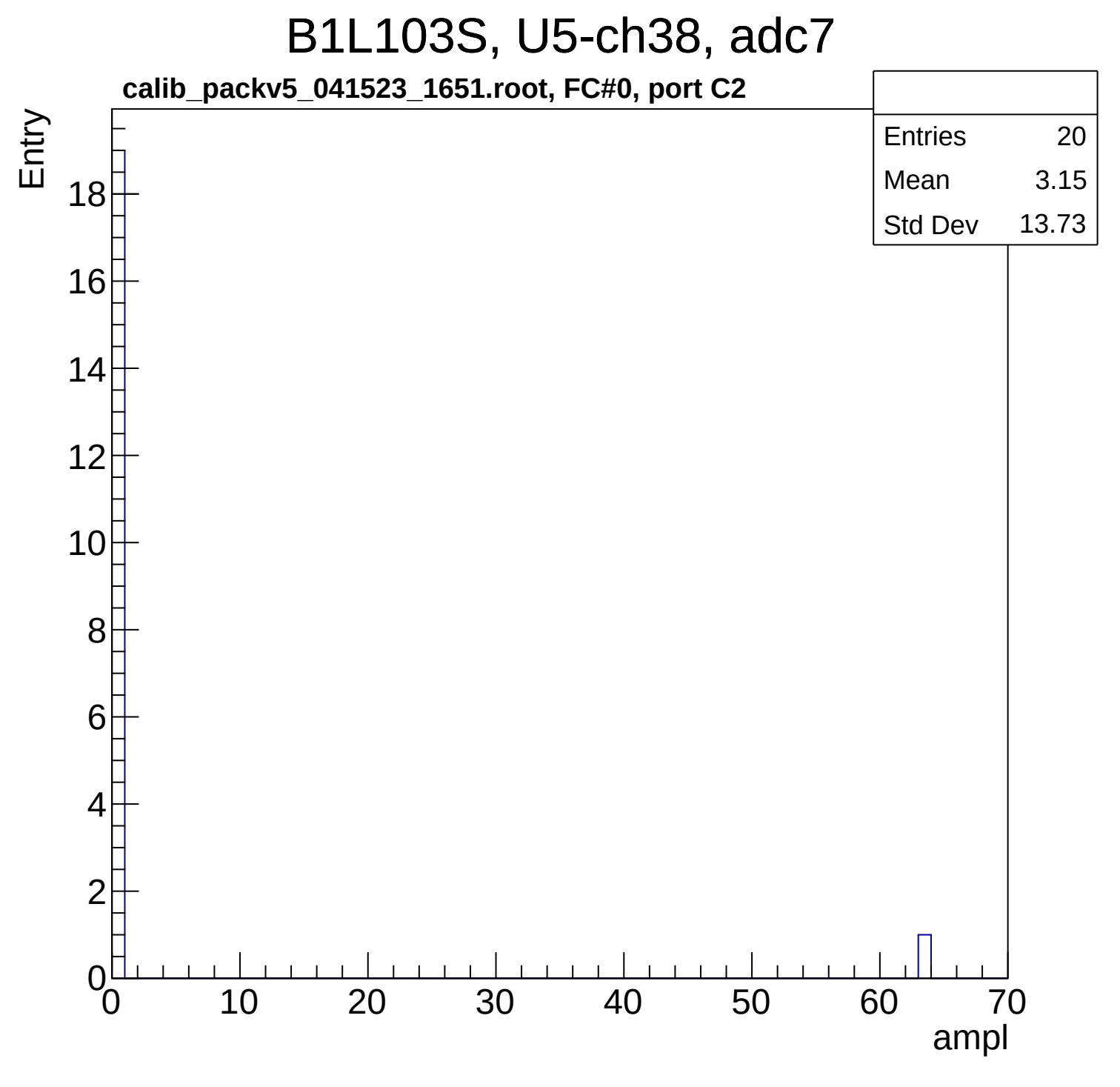
B1L103S, U5-ch38, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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6
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14
16
18
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10
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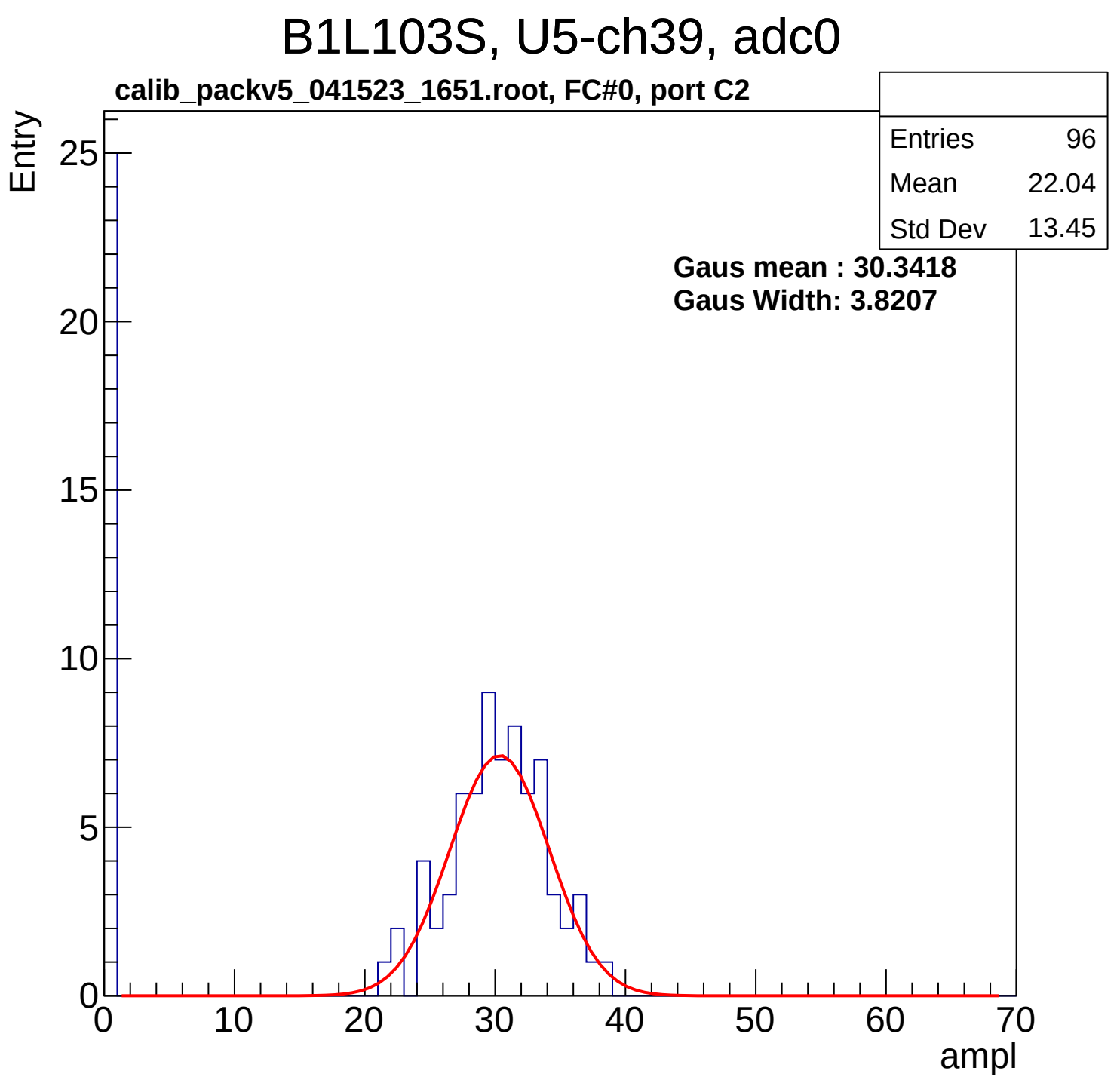
70
ampl


B1L103S, U5-ch39, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 22.04
Std Dev 13.45
Gaus mean : 30.3418
Gaus Width: 3.8207
Entry
ampl
0
5
10
15
20
25
0
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40
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60
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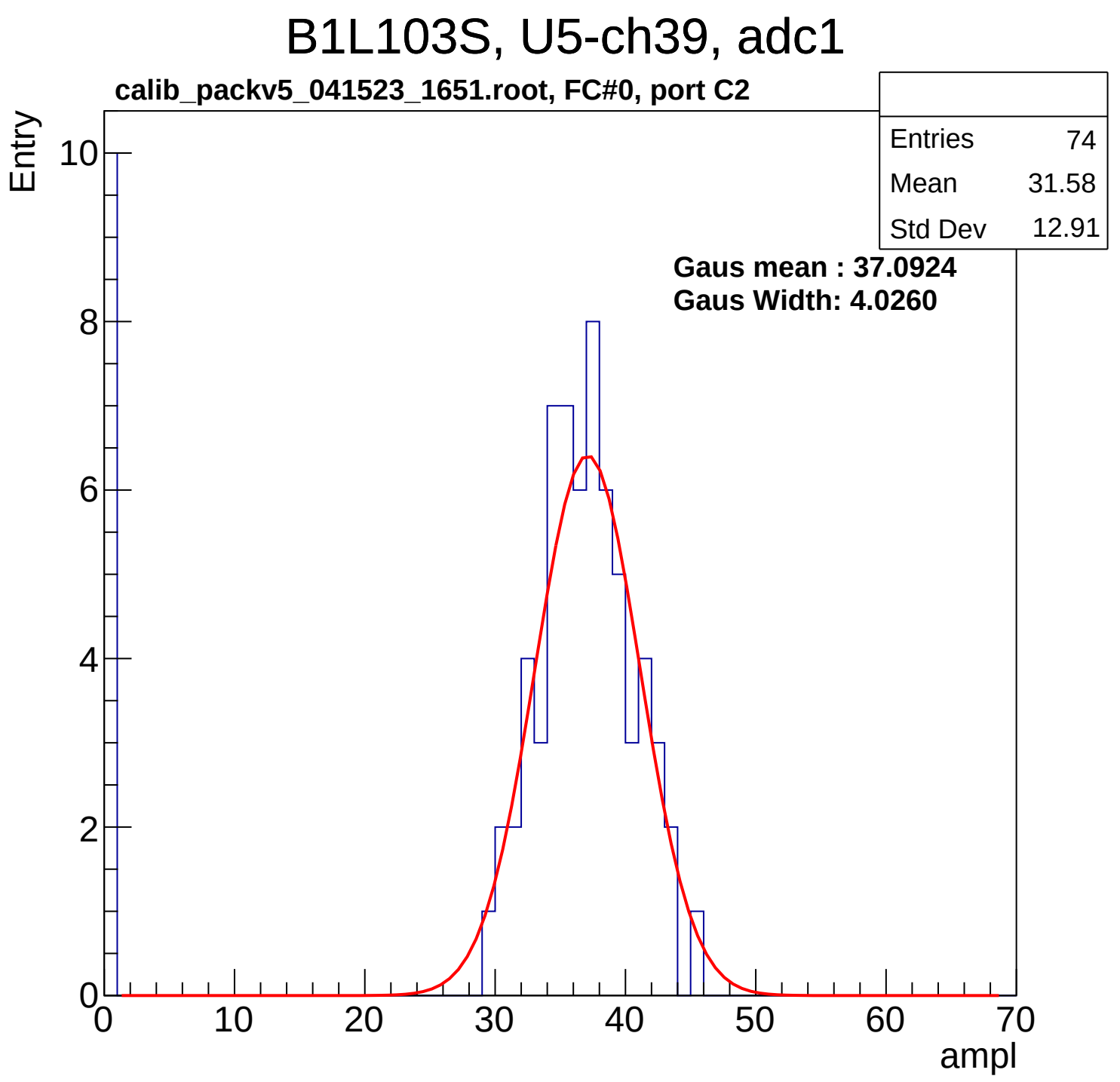
B1L103S, U5-ch39, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 31.58
Std Dev 12.91
Gaus mean : 37.0924
Gaus Width: 4.0260
Entry
ampl
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0
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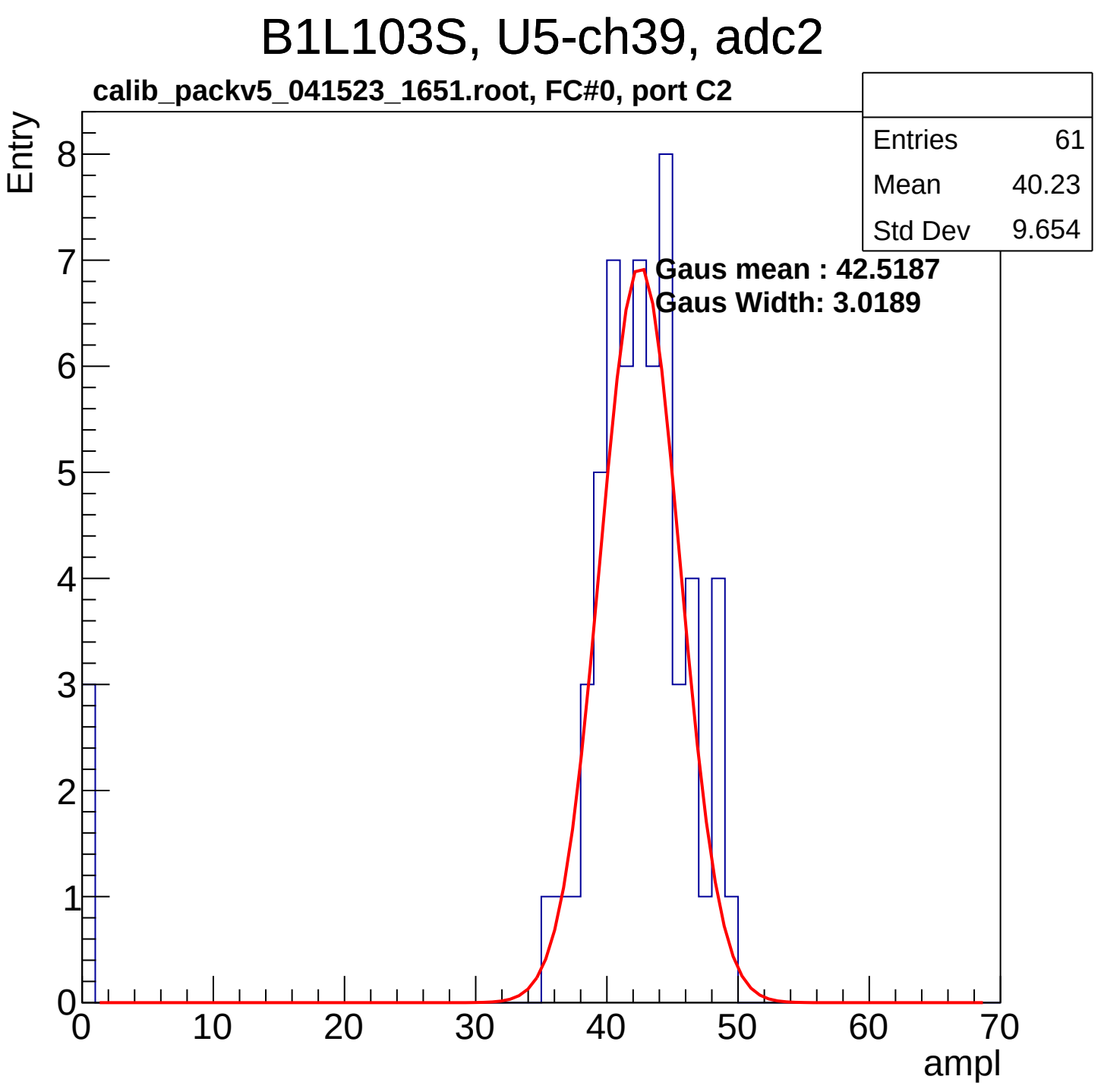
B1L103S, U5-ch39, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 40.23
Std Dev 9.654
Gaus mean : 42.5187
Gaus Width: 3.0189
Entry
ampl
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1
2
3
4
5
6
7
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0
10
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40
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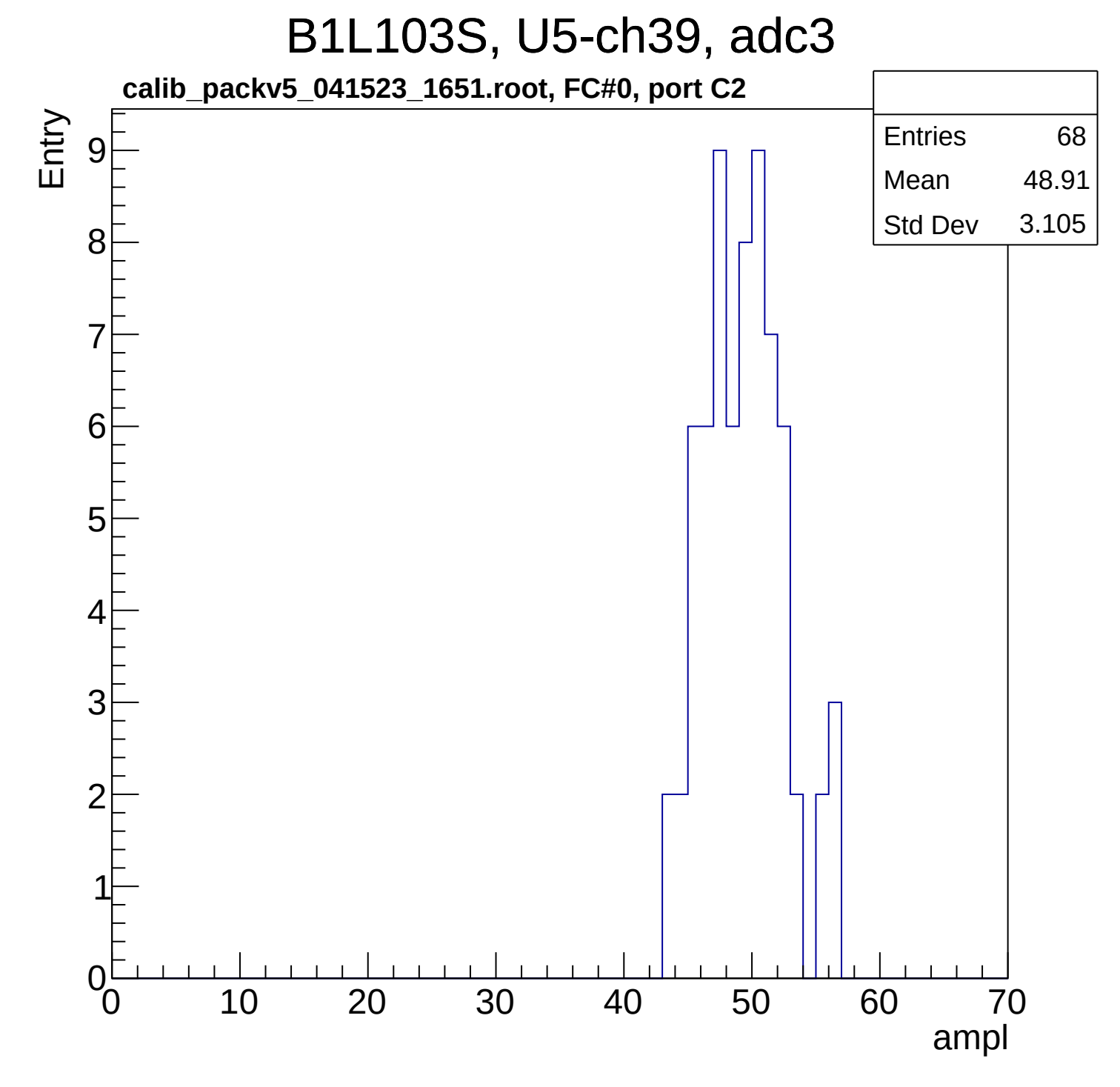
B1L103S, U5-ch39, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 48.91
Std Dev 3.105
Entry
ampl
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2
3
4
5
6
7
8
9
0
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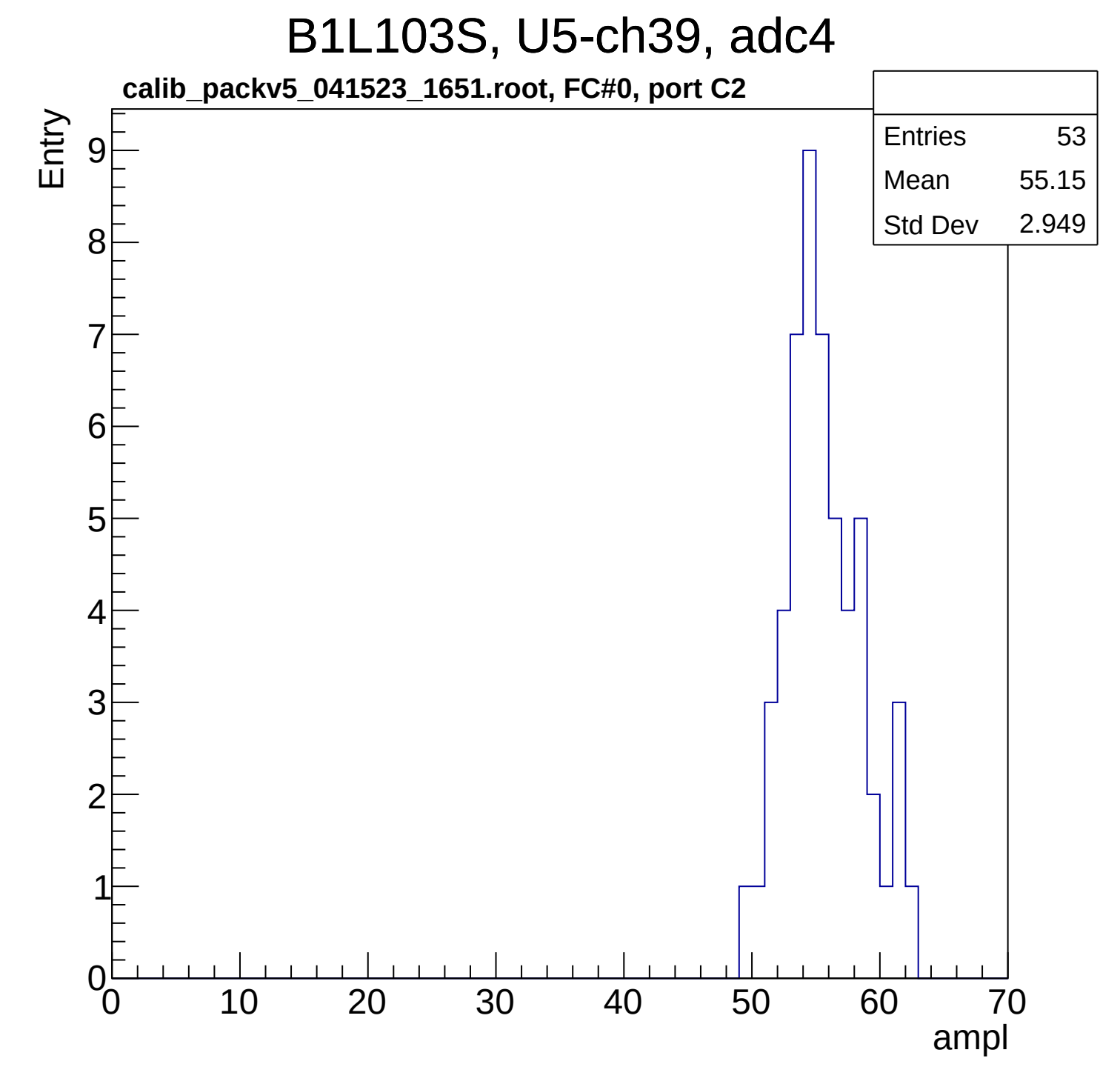
B1L103S, U5-ch39, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 55.15
Std Dev 2.949
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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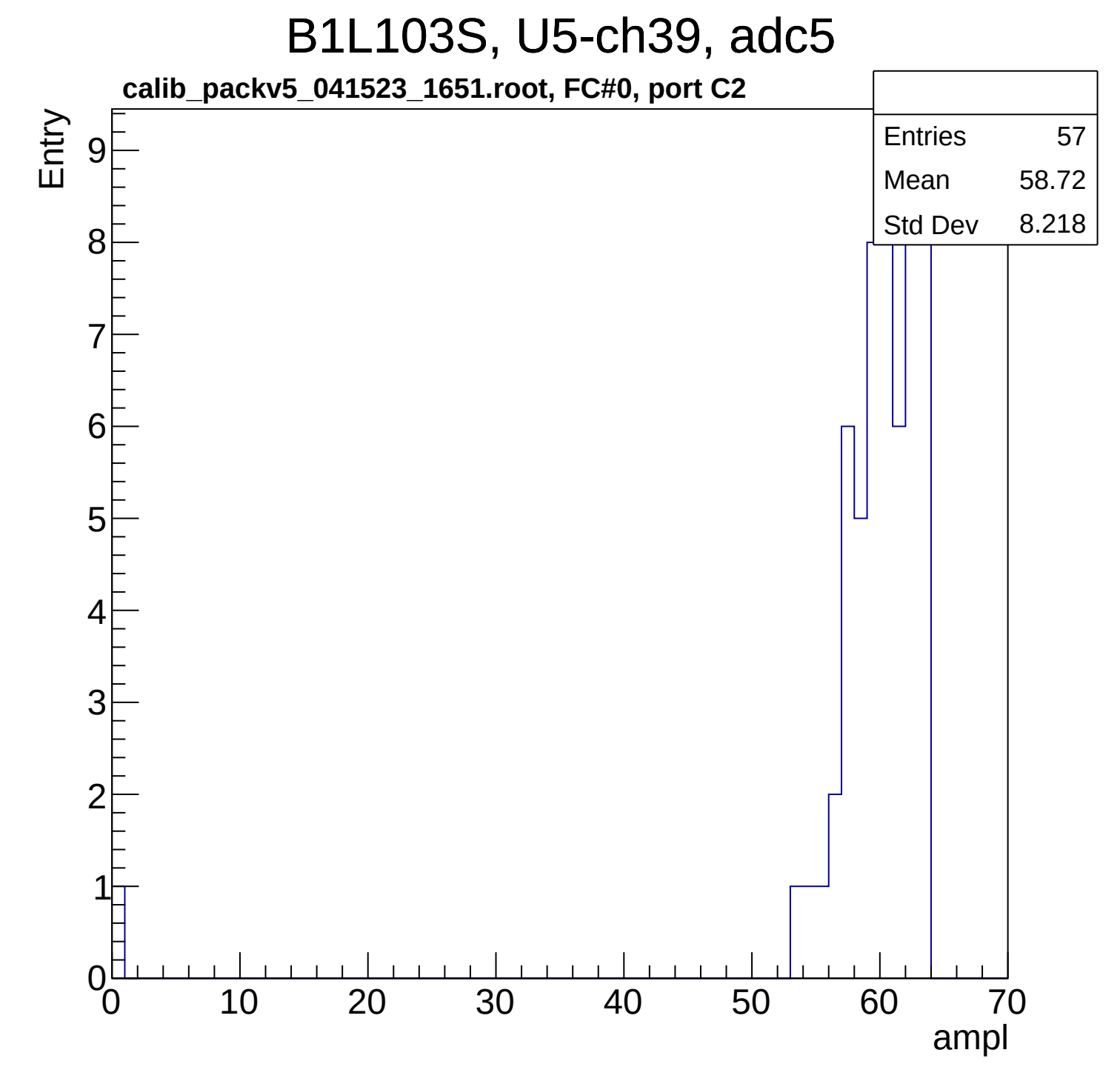
B1L103S, U5-ch39, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.72
Std Dev 8.218
Entry
ampl
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0
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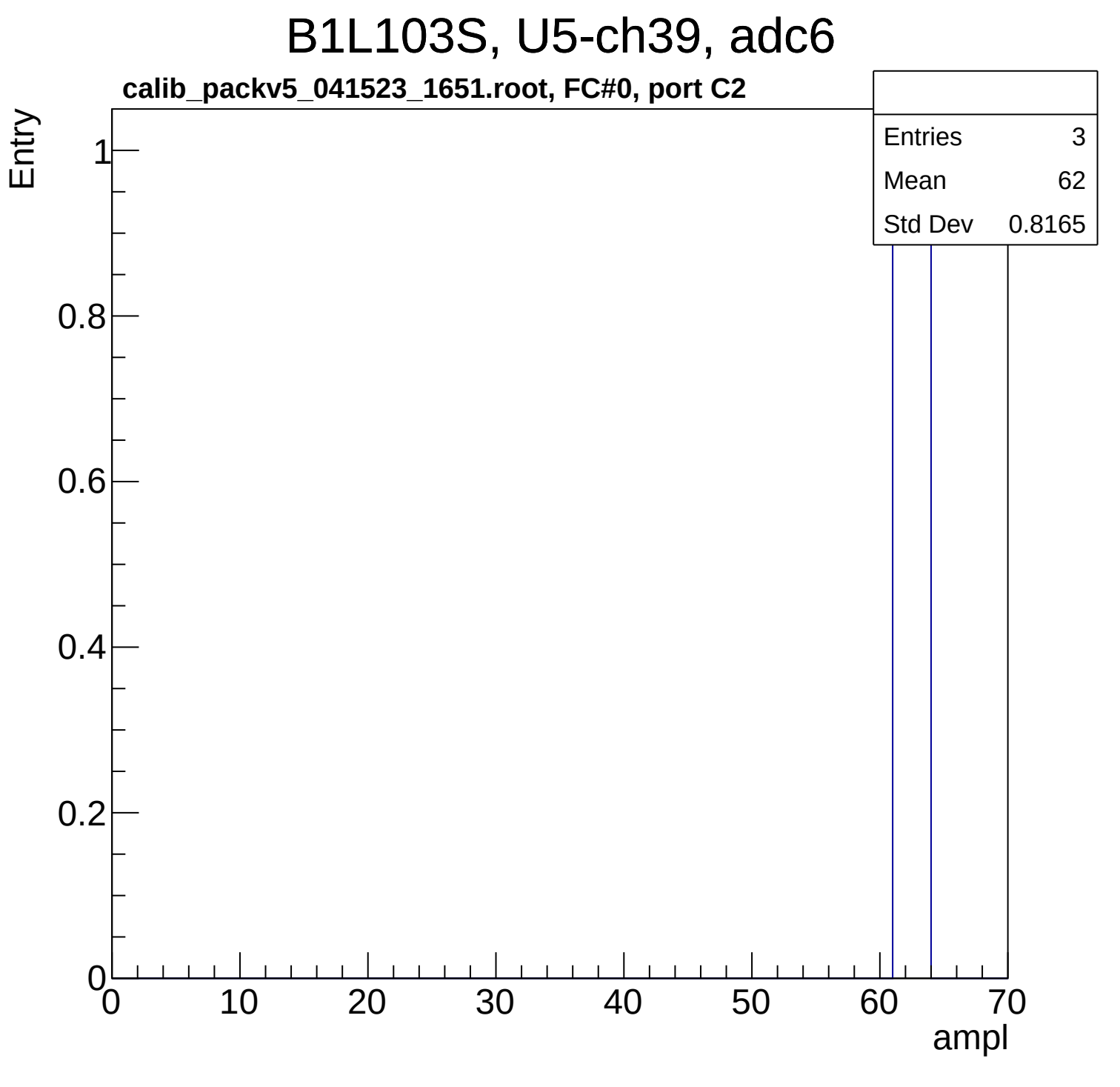
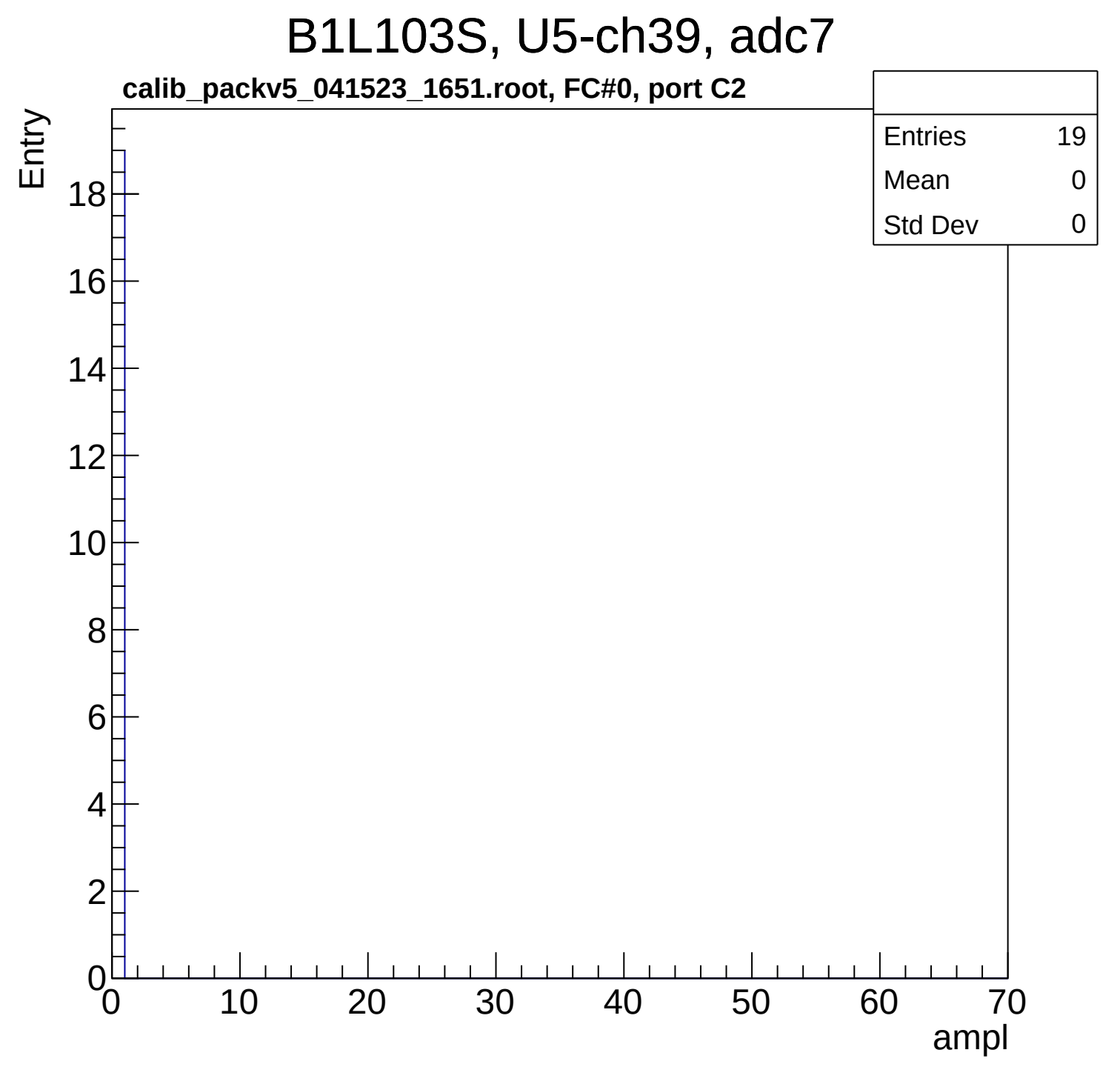
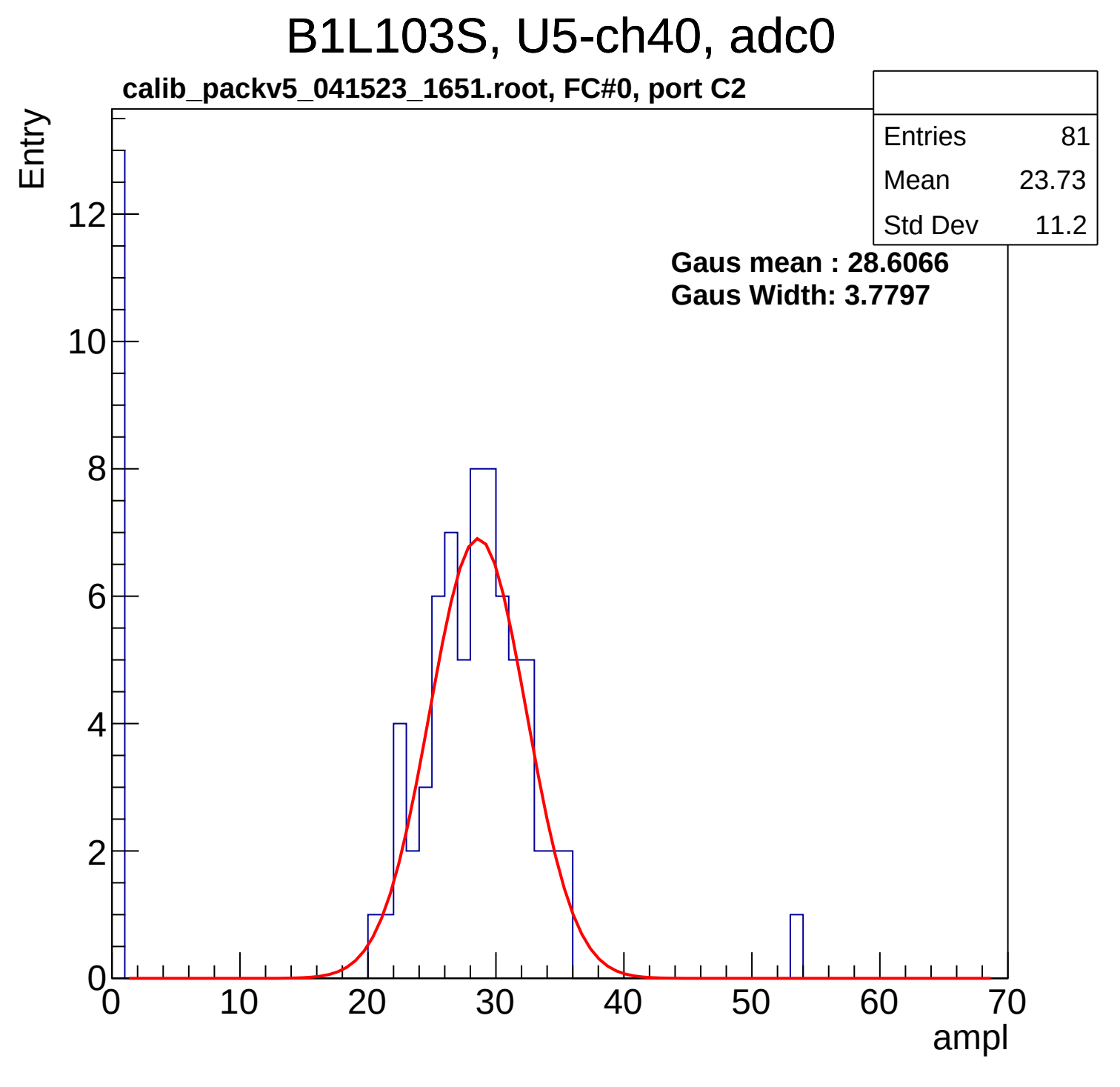

B1L103S, U5-ch39, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62
Std Dev 0.8165
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch39, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch40, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 23.73
Std Dev 11.2
Gaus mean : 28.6066
Gaus Width: 3.7797
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
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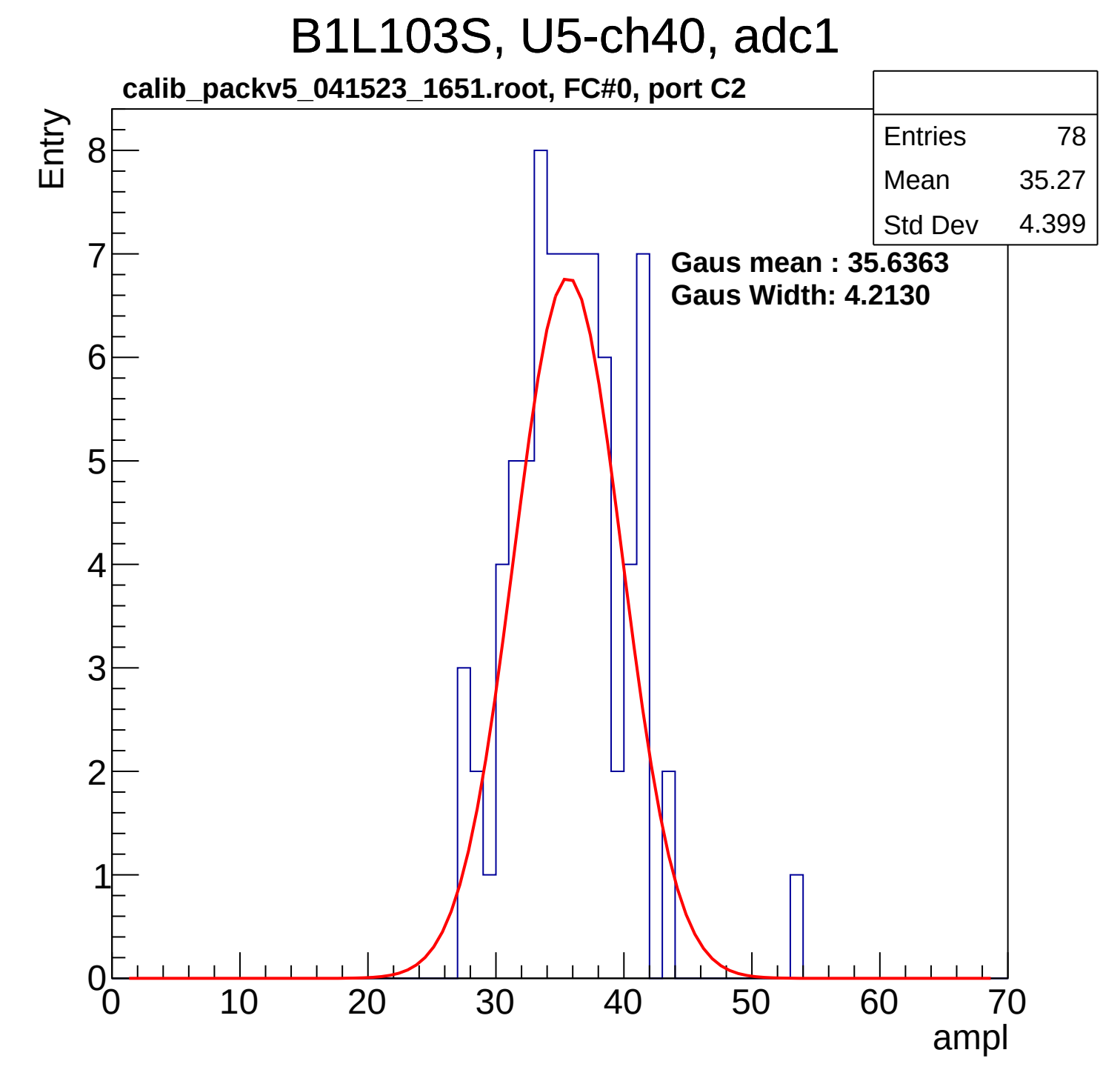
B1L103S, U5-ch40, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 35.27
Std Dev 4.399
Gaus mean : 35.6363
Gaus Width: 4.2130
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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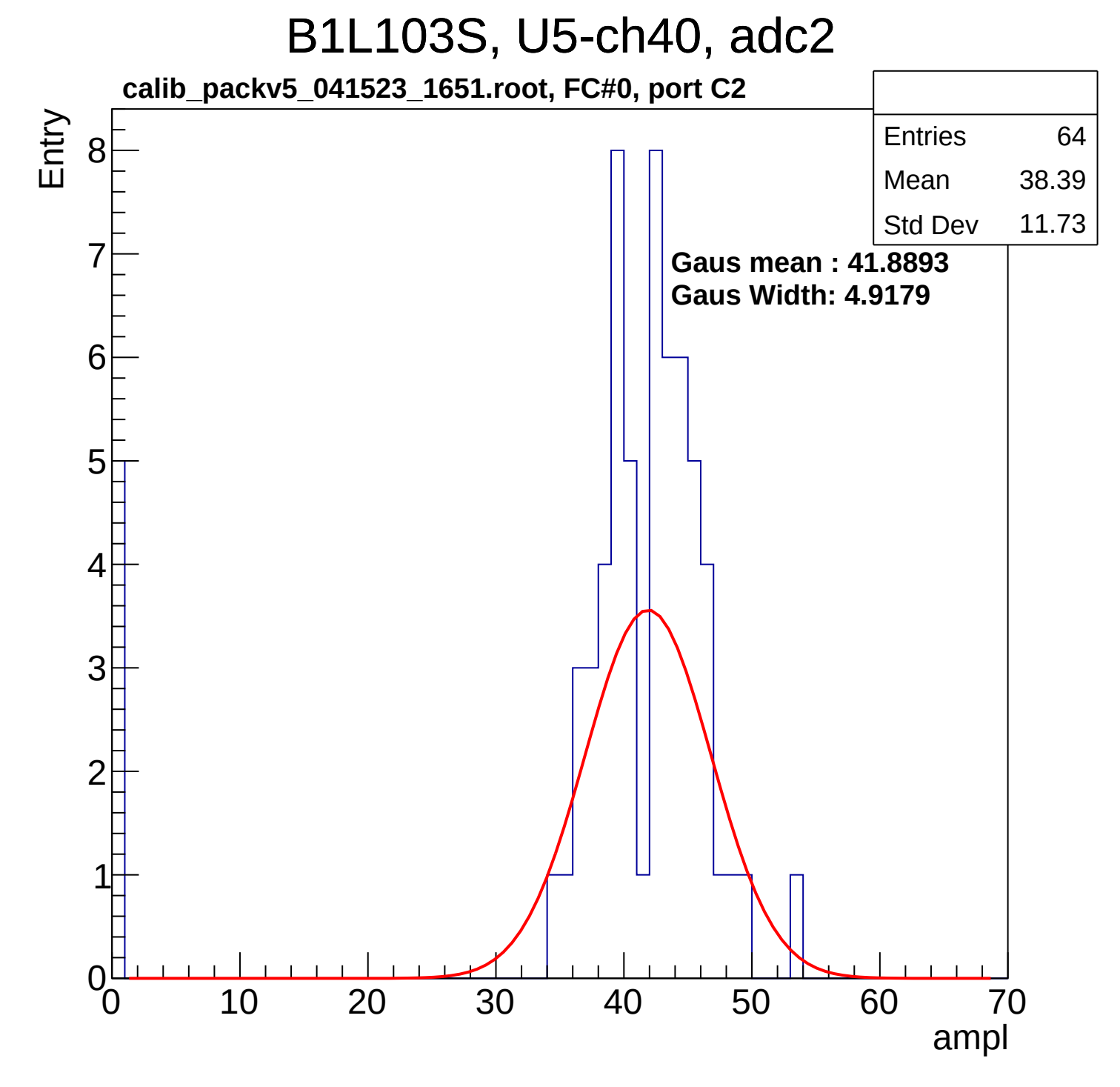
B1L103S, U5-ch40, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 38.39
Std Dev 11.73
Gaus mean : 41.8893
Gaus Width: 4.9179
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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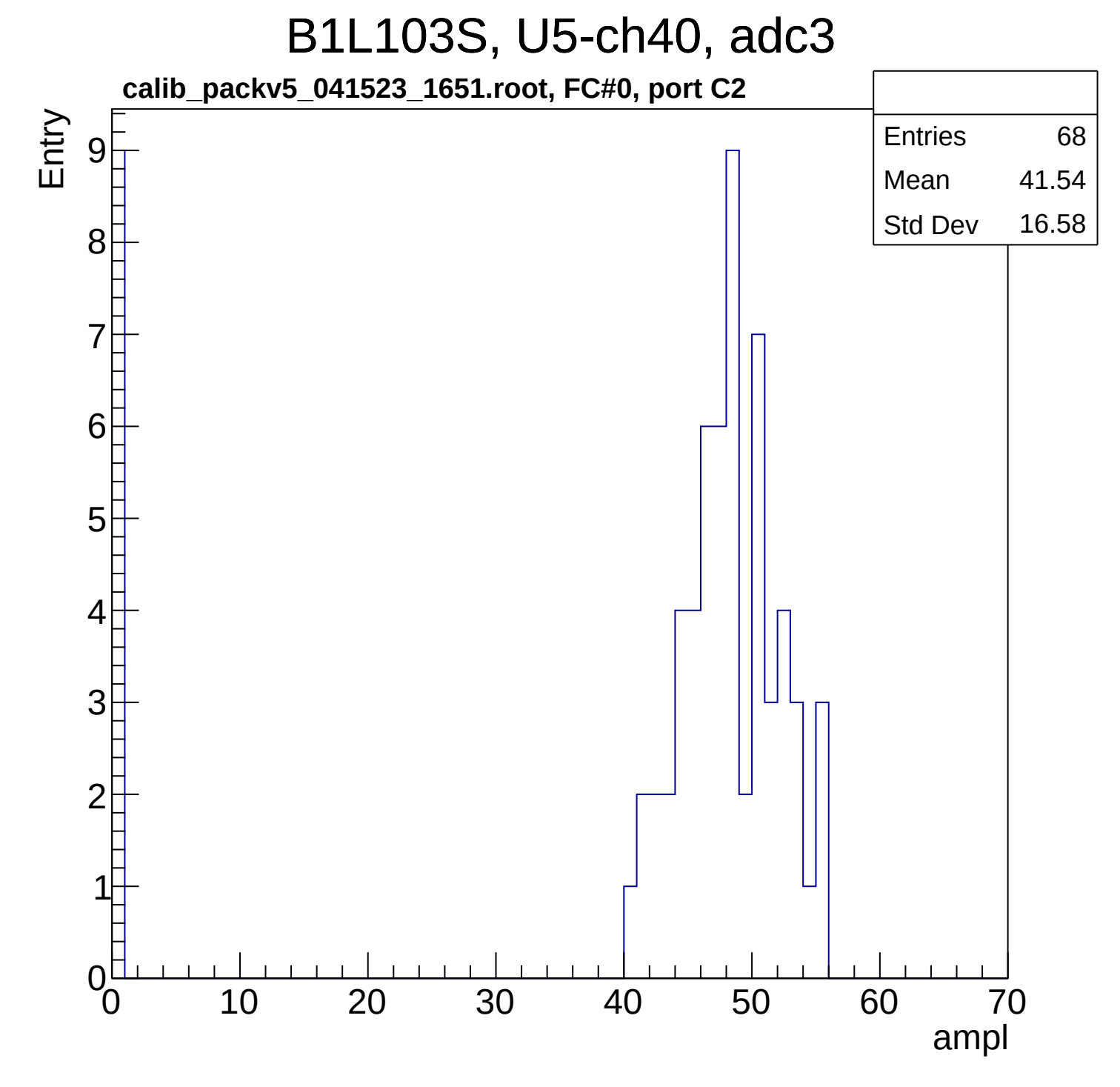
B1L103S, U5-ch40, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 41.54
Std Dev 16.58
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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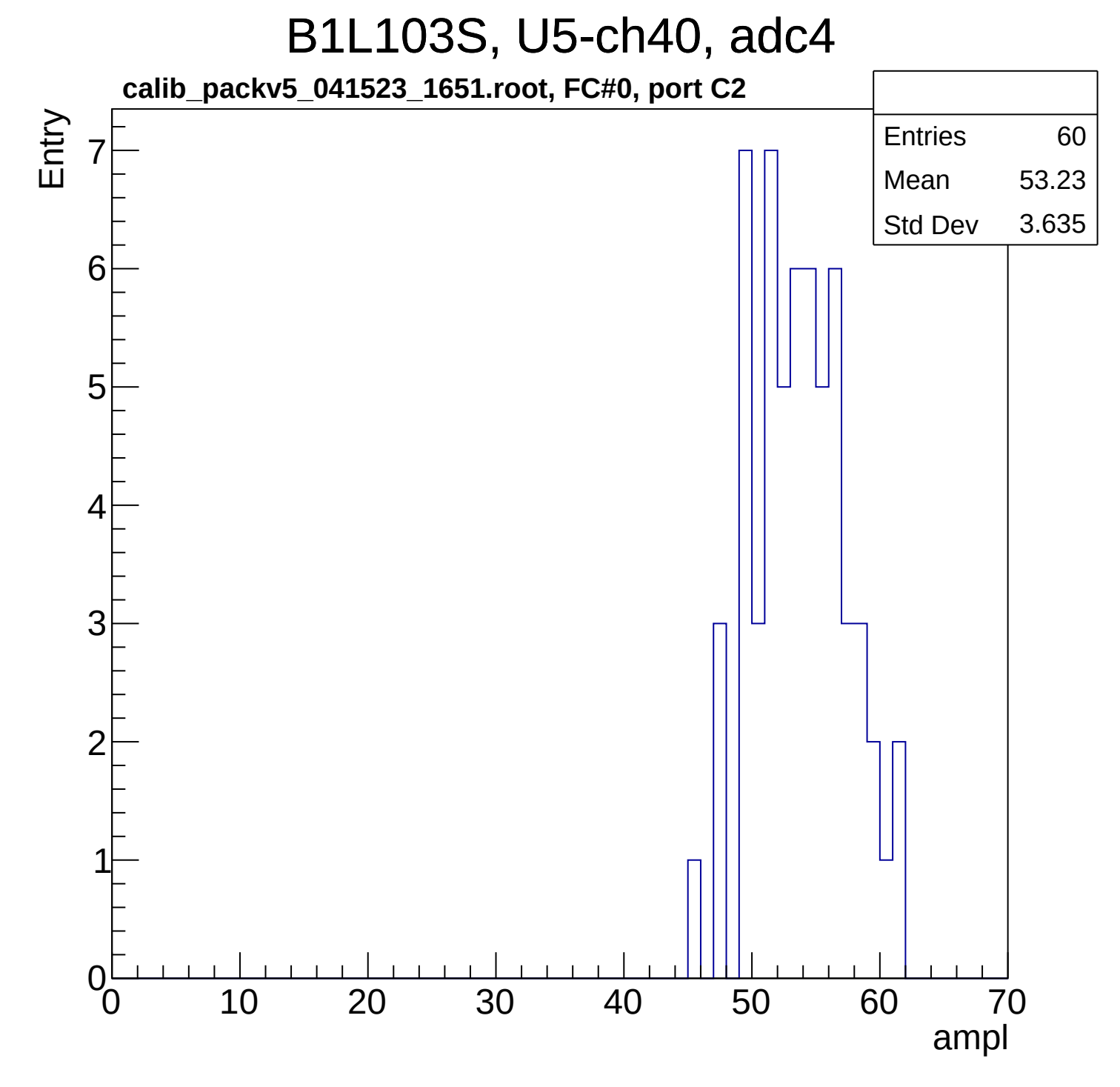
B1L103S, U5-ch40, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 53.23
Std Dev 3.635
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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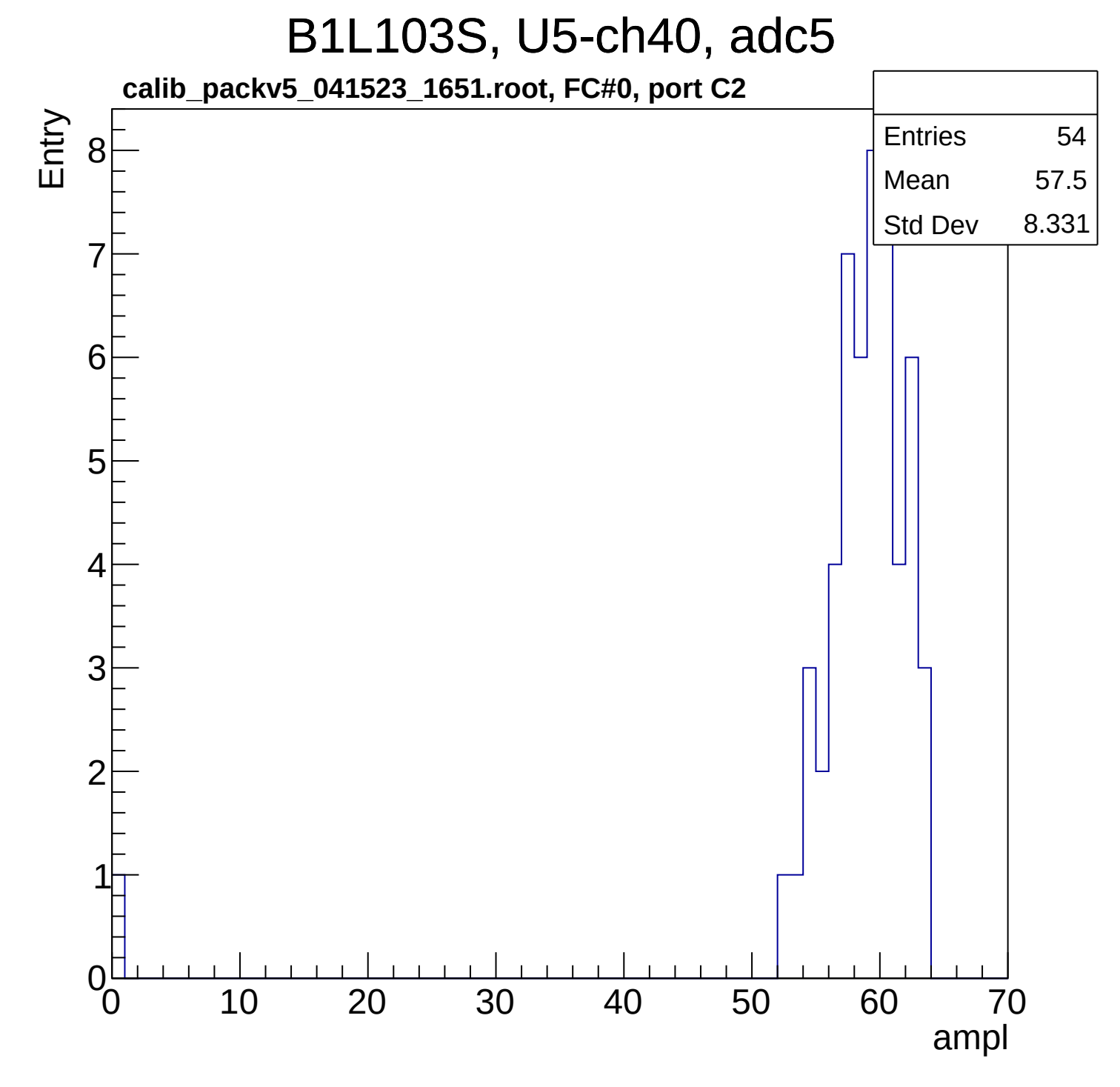
B1L103S, U5-ch40, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.5
Std Dev 8.331
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
50
60
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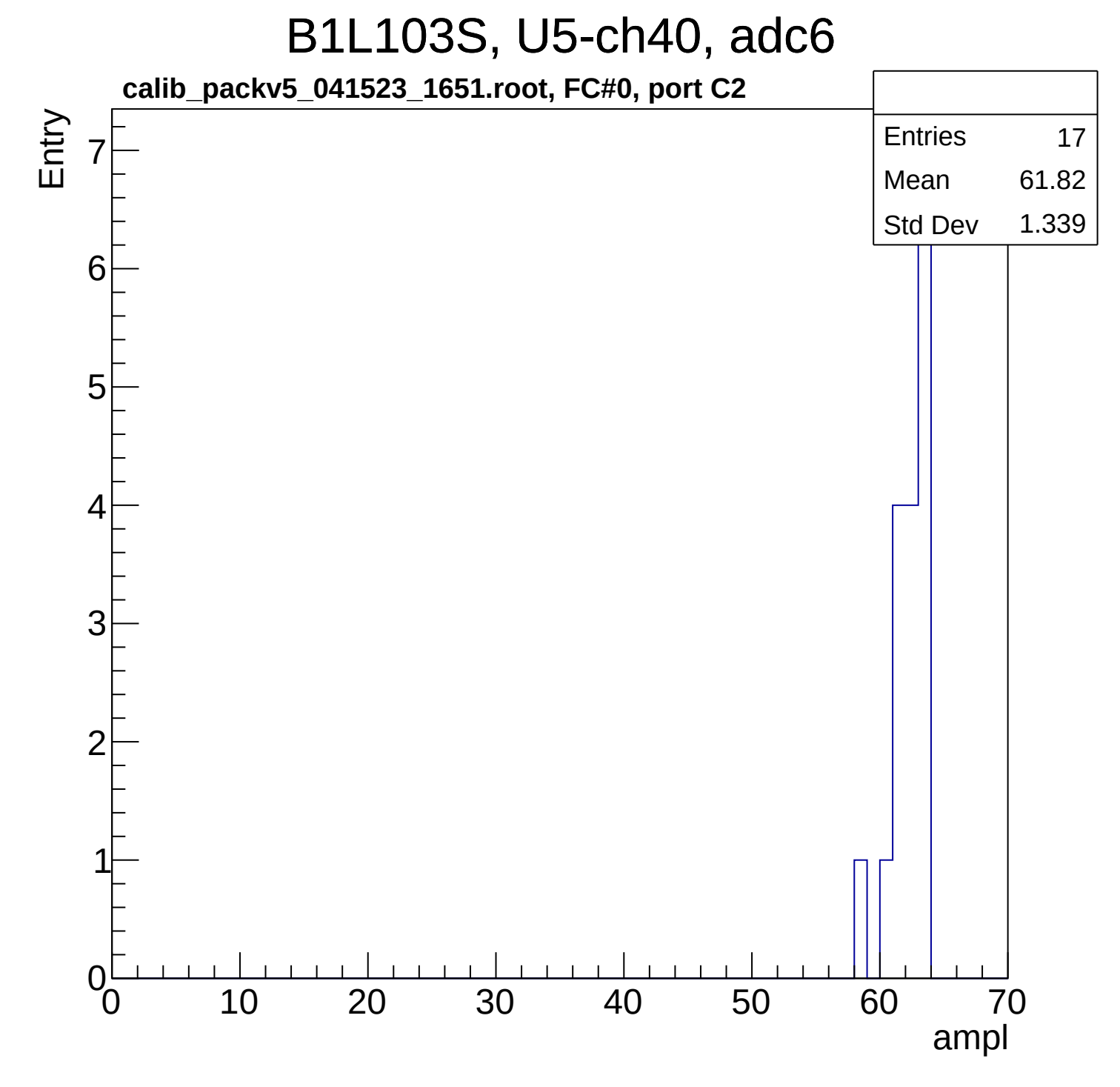
B1L103S, U5-ch40, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.82
Std Dev 1.339
Entry
ampl
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2
3
4
5
6
7
0
10
20
30
40
50
60
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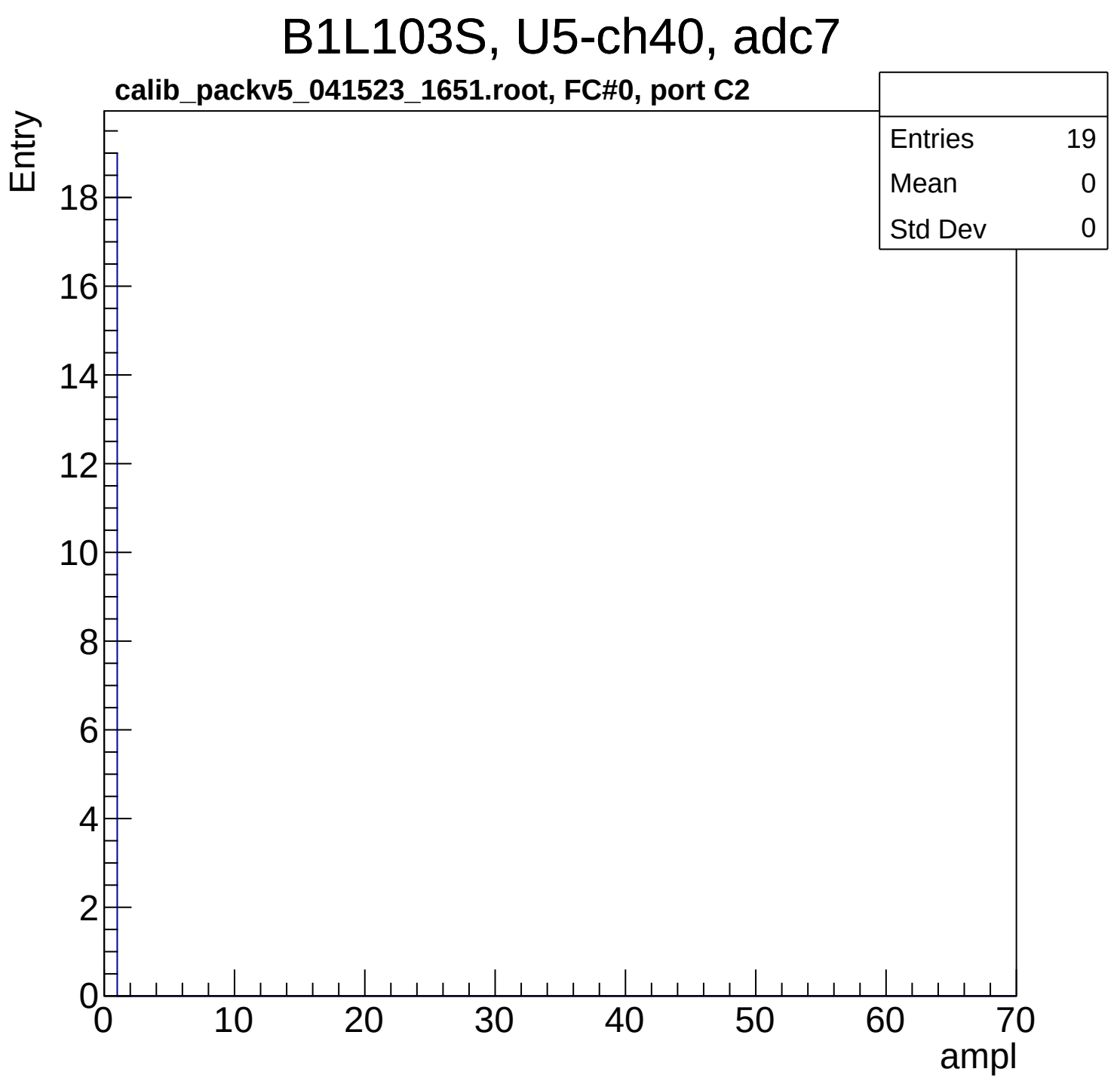
B1L103S, U5-ch40, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
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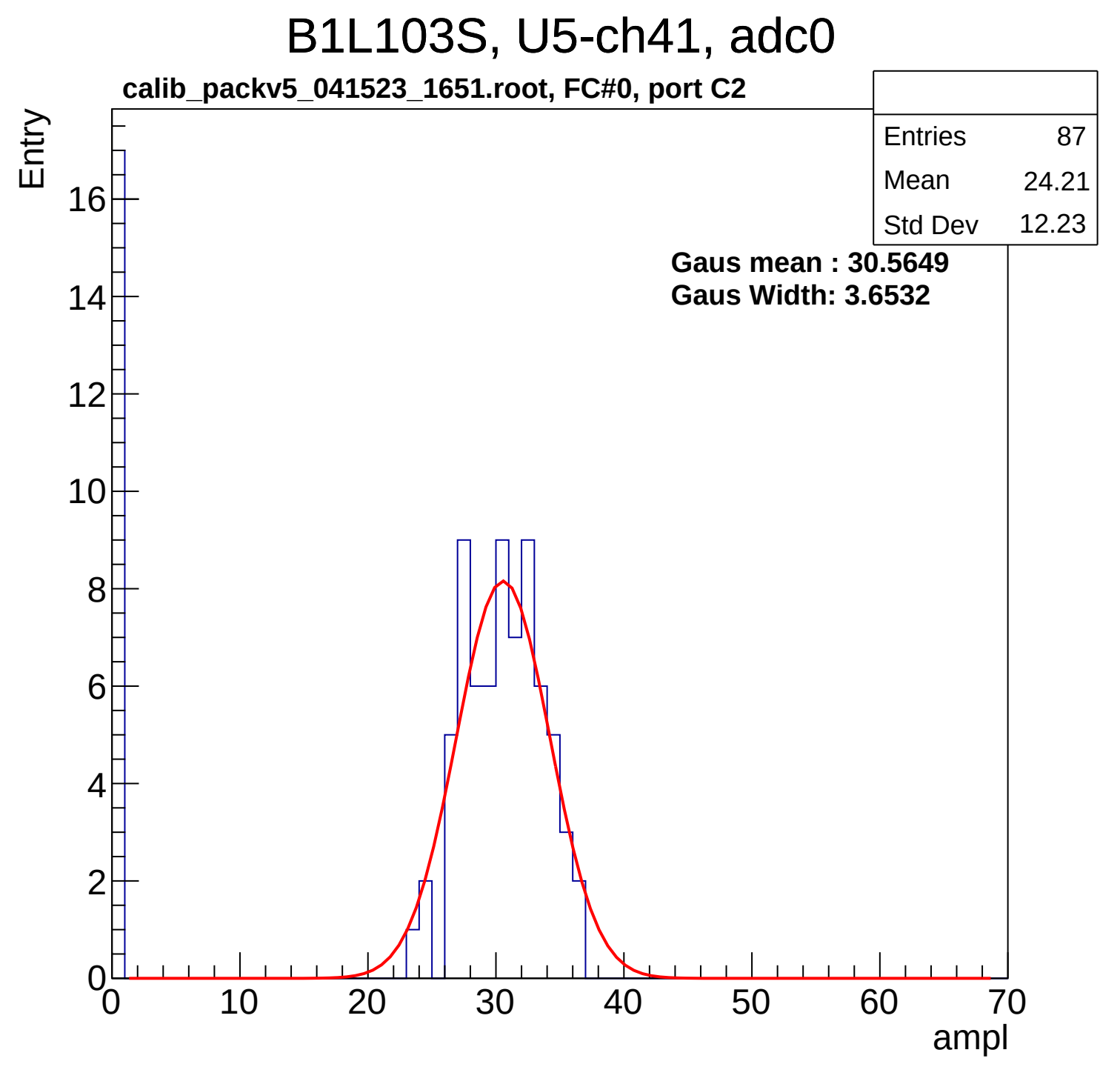
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch41, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 24.21
Std Dev 12.23
Gaus mean : 30.5649
Gaus Width: 3.6532
Entry
ampl
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4
6
8
10
12
14
16
0
10
20
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40
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60
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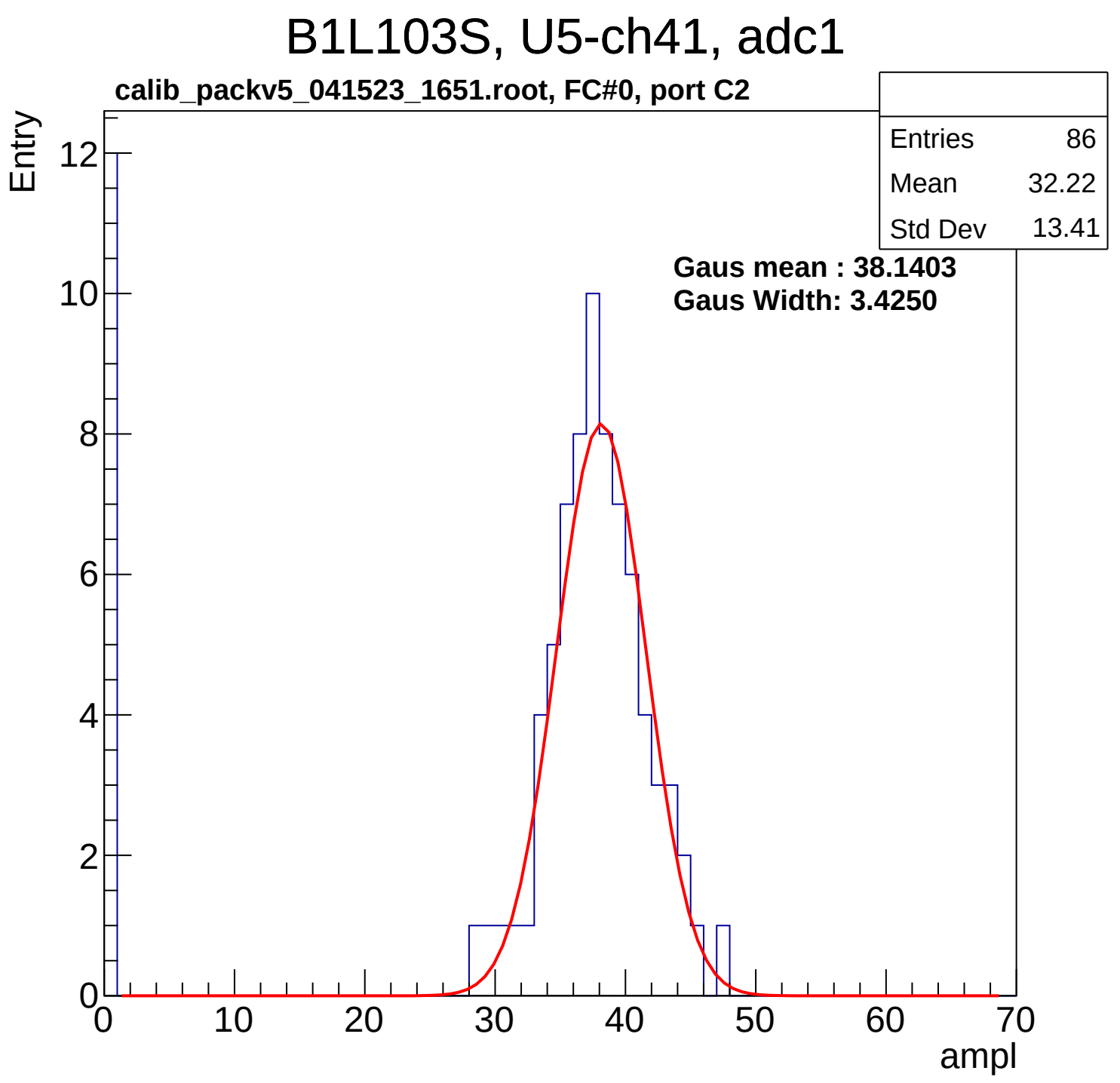
B1L103S, U5-ch41, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 32.22
Std Dev 13.41
Gaus mean : 38.1403
Gaus Width: 3.4250
Entry
ampl
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6
8
10
12
0
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20
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40
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60
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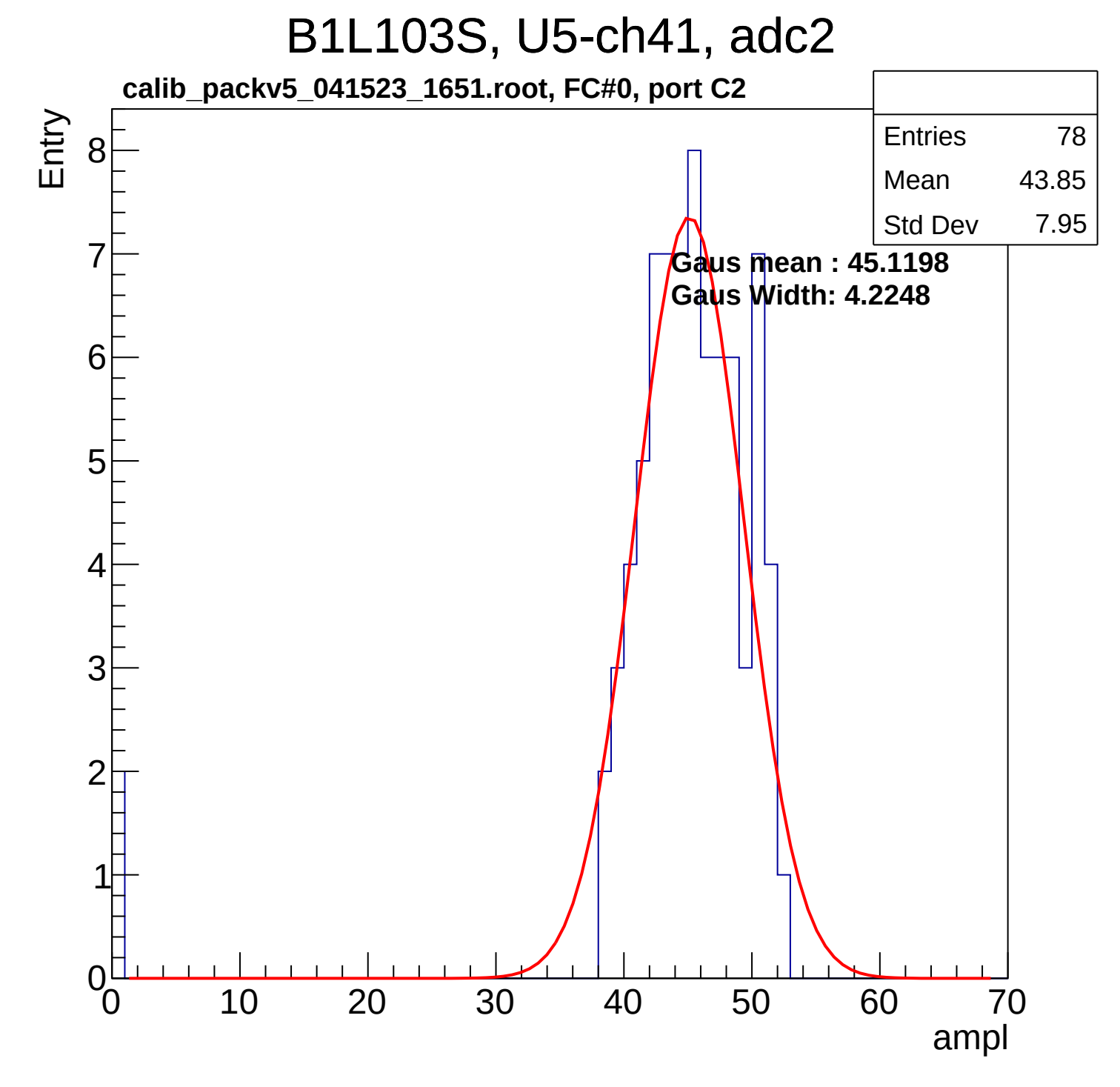
B1L103S, U5-ch41, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 43.85
Std Dev 7.95
Gaus mean : 45.1198
Gaus Width: 4.2248
Entry
ampl
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1
2
3
4
5
6
7
8
0
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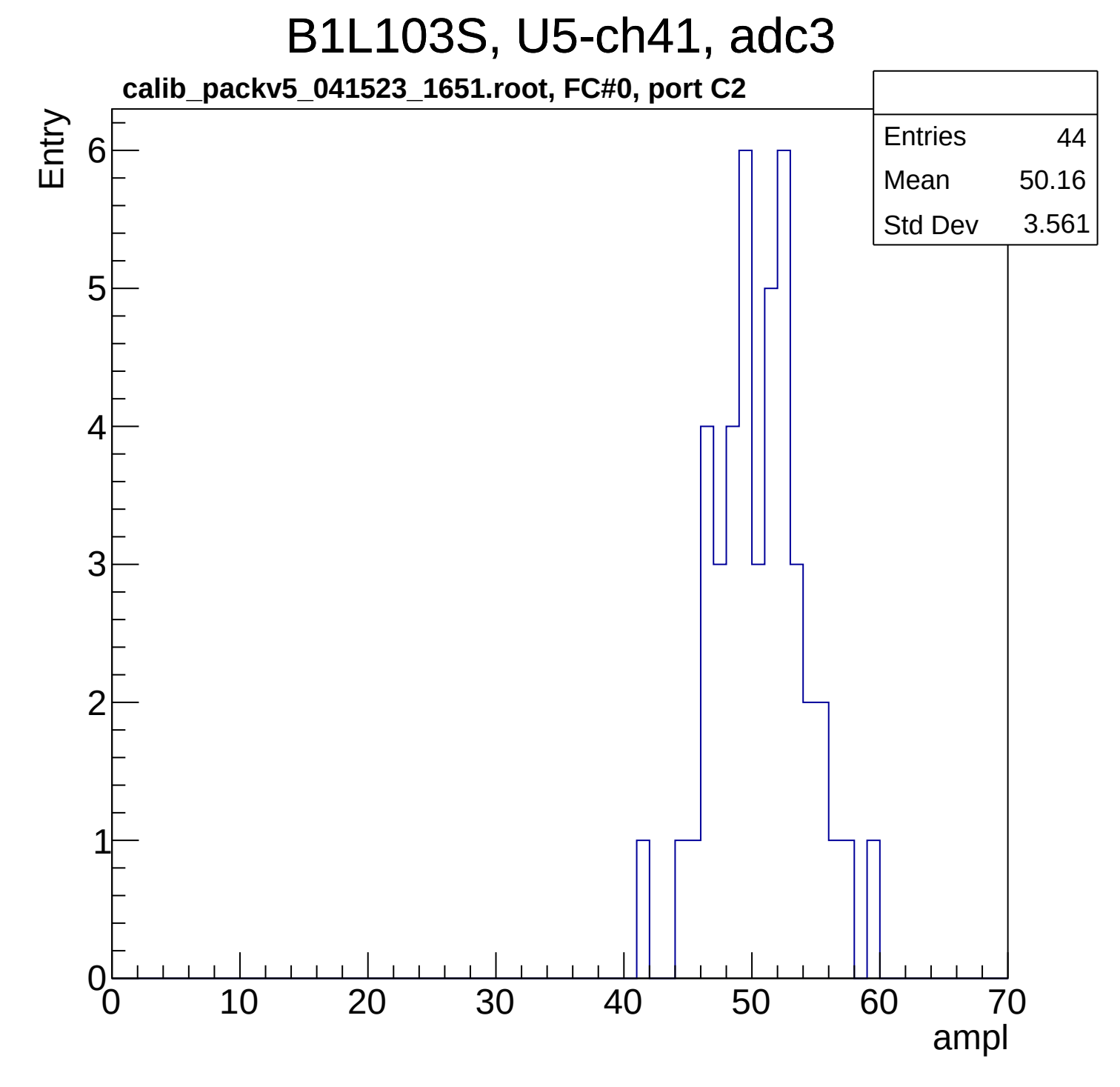
B1L103S, U5-ch41, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 50.16
Std Dev 3.561
Entry
ampl
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3
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5
6
0
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20
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40
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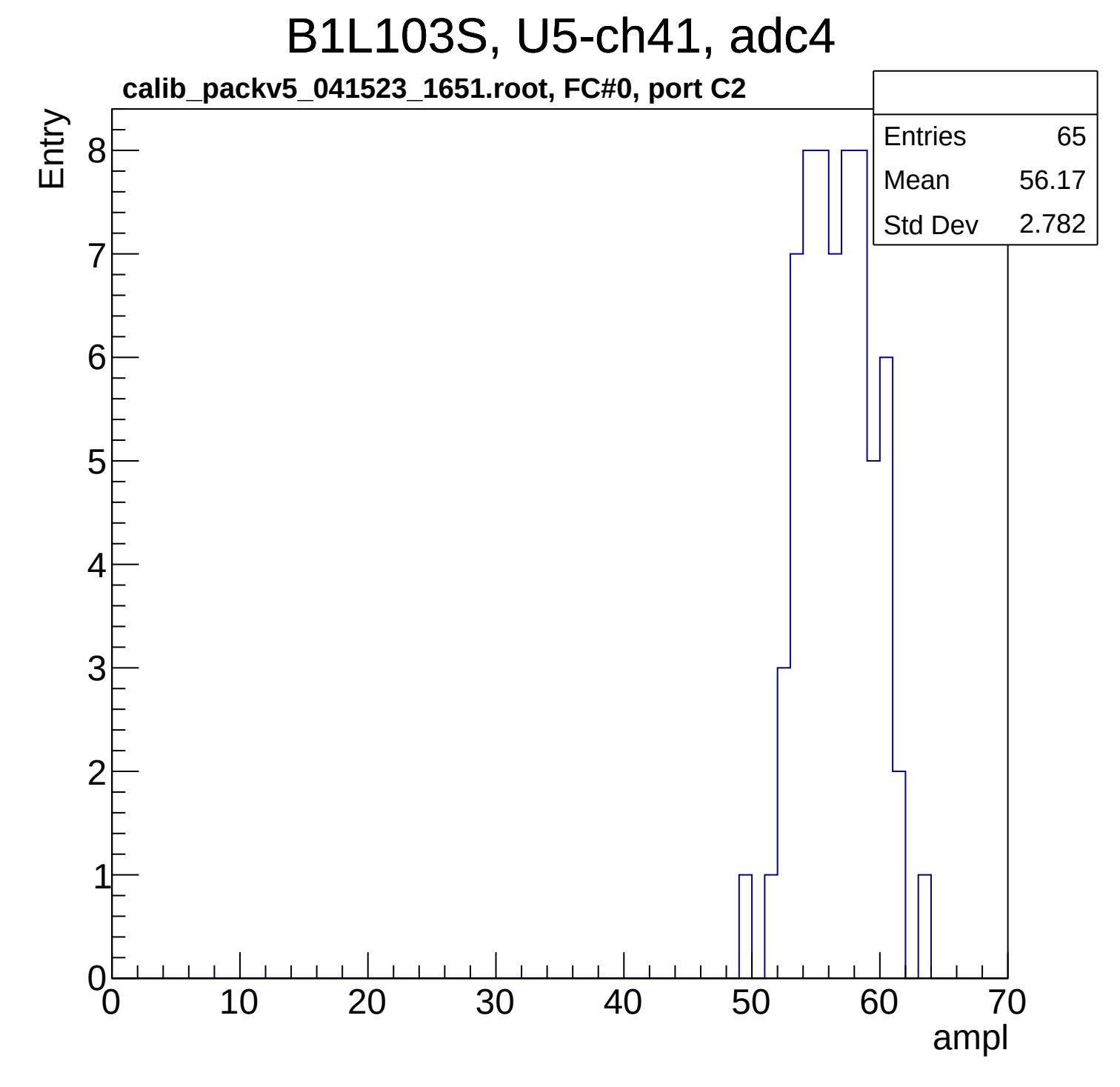
60
70


B1L103S, U5-ch41, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 56.17
Std Dev 2.782
Entry
ampl
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4
5
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7
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0
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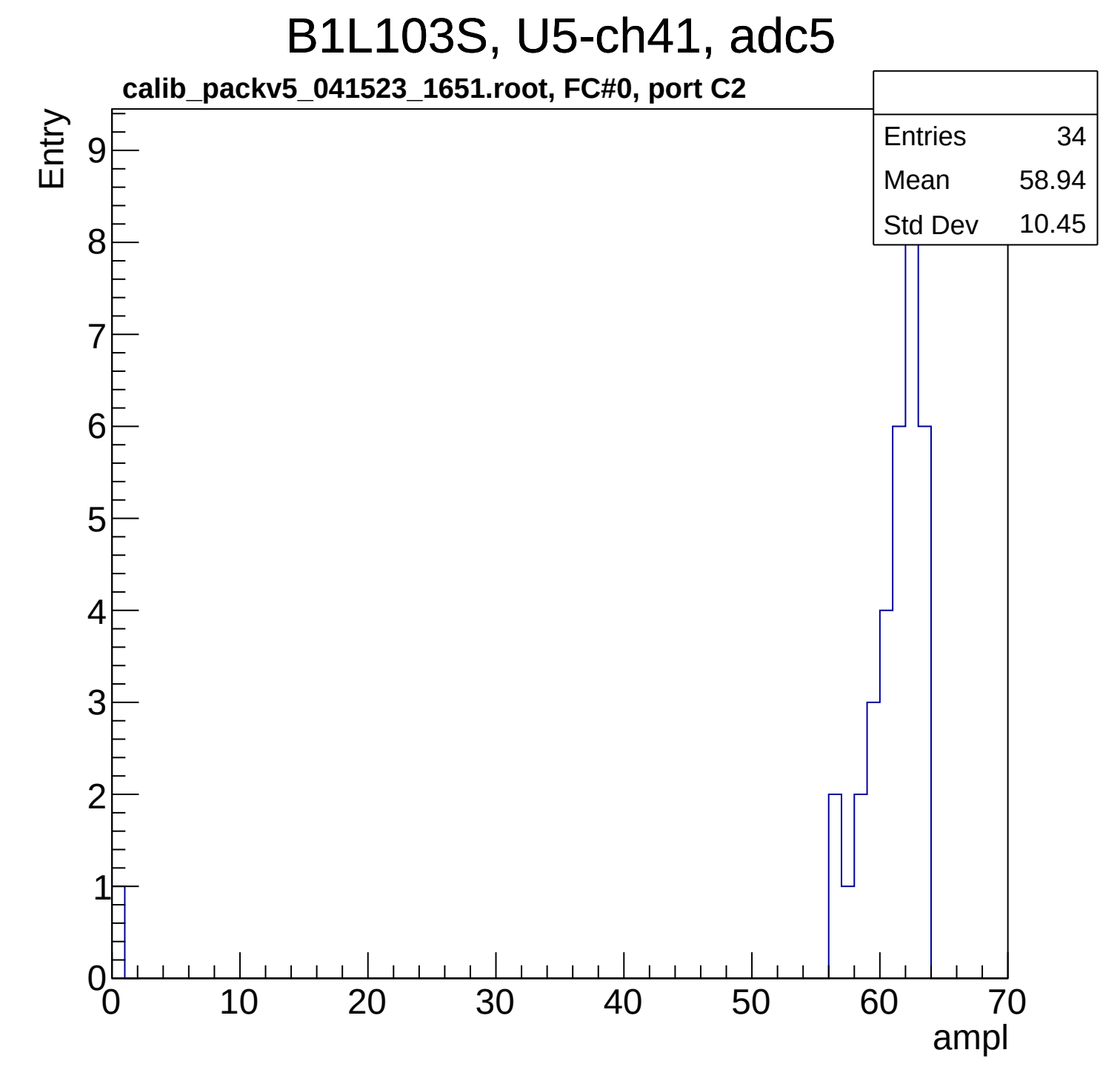
B1L103S, U5-ch41, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 58.94
Std Dev 10.45
Entry
ampl
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3
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5
6
7
8
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0
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40
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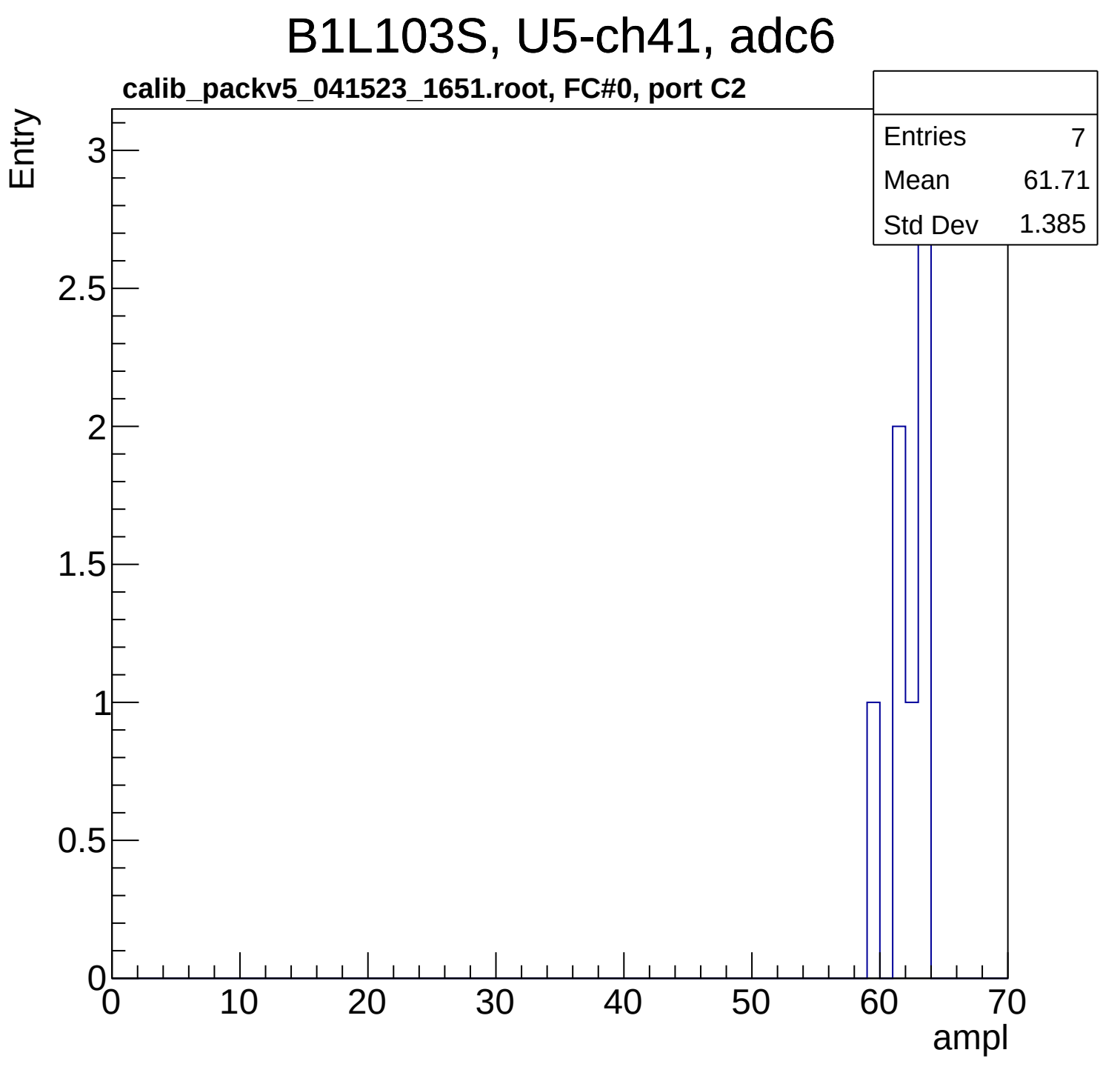
B1L103S, U5-ch41, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.71
Std Dev 1.385
Entry
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1
1.5
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2.5
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0
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20
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40
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60
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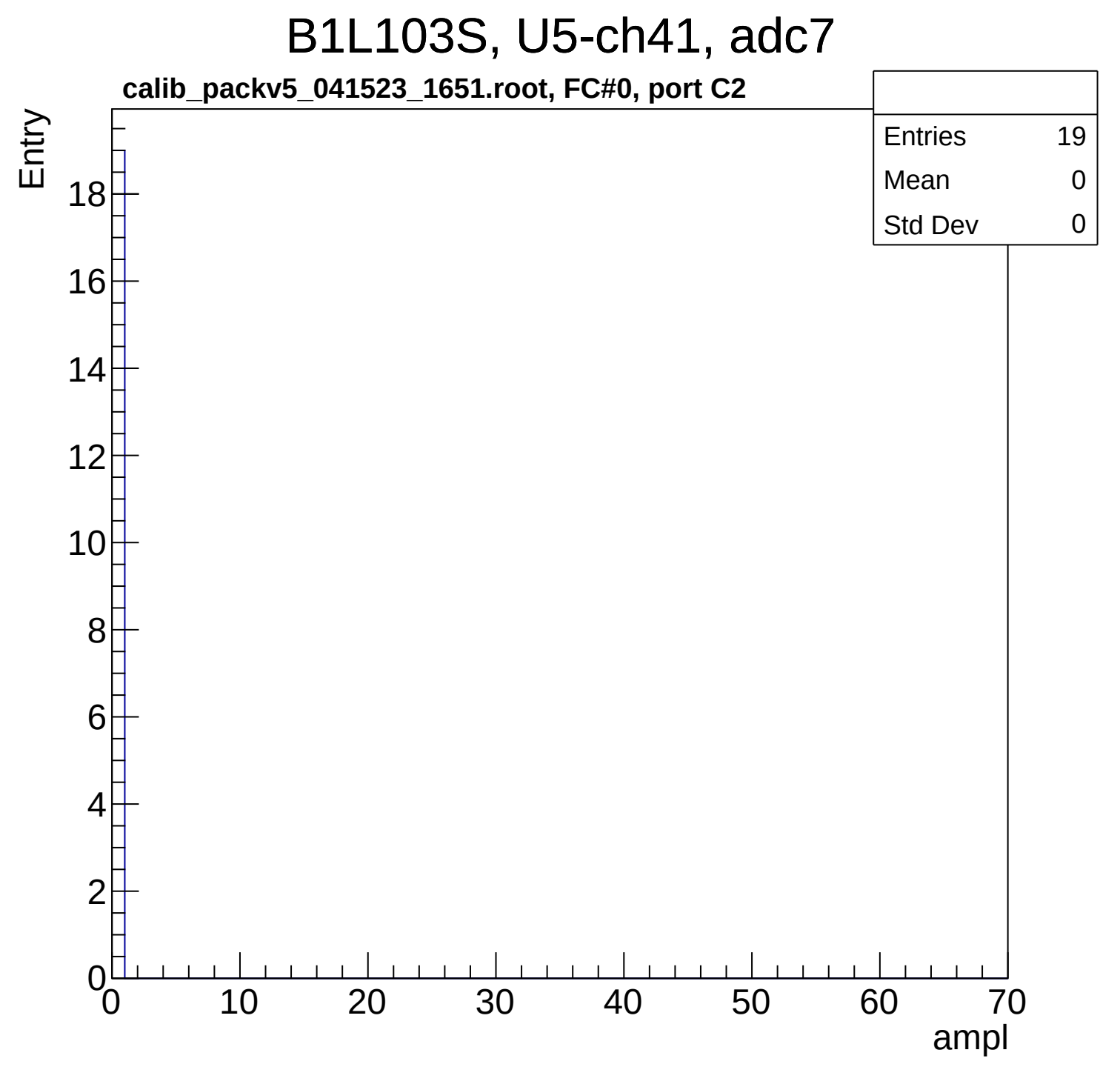
B1L103S, U5-ch41, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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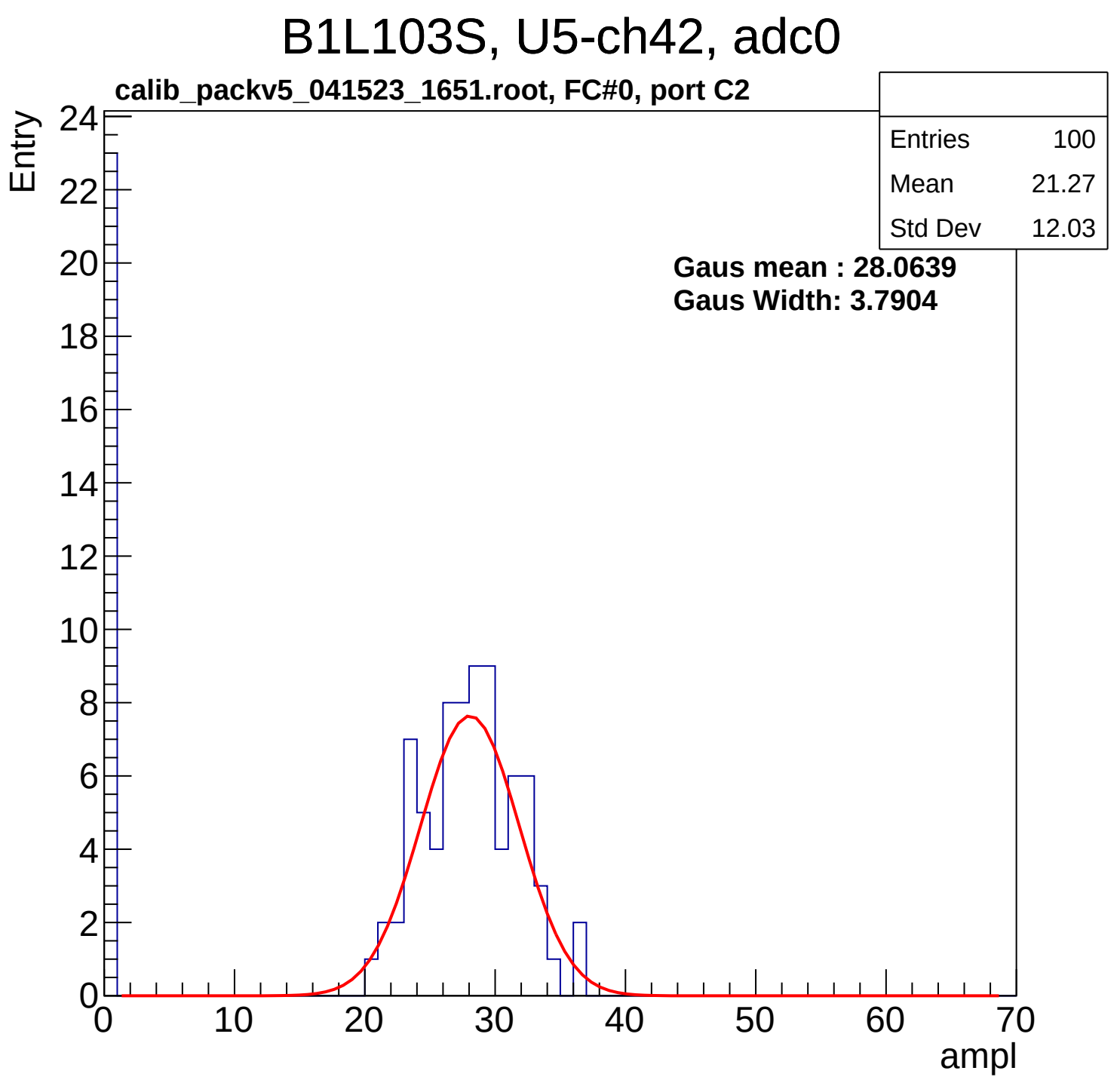
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch42, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 21.27
Std Dev 12.03
Gaus mean : 28.0639
Gaus Width: 3.7904
Entry
ampl
0
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10
12
14
16
18
20
22
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0
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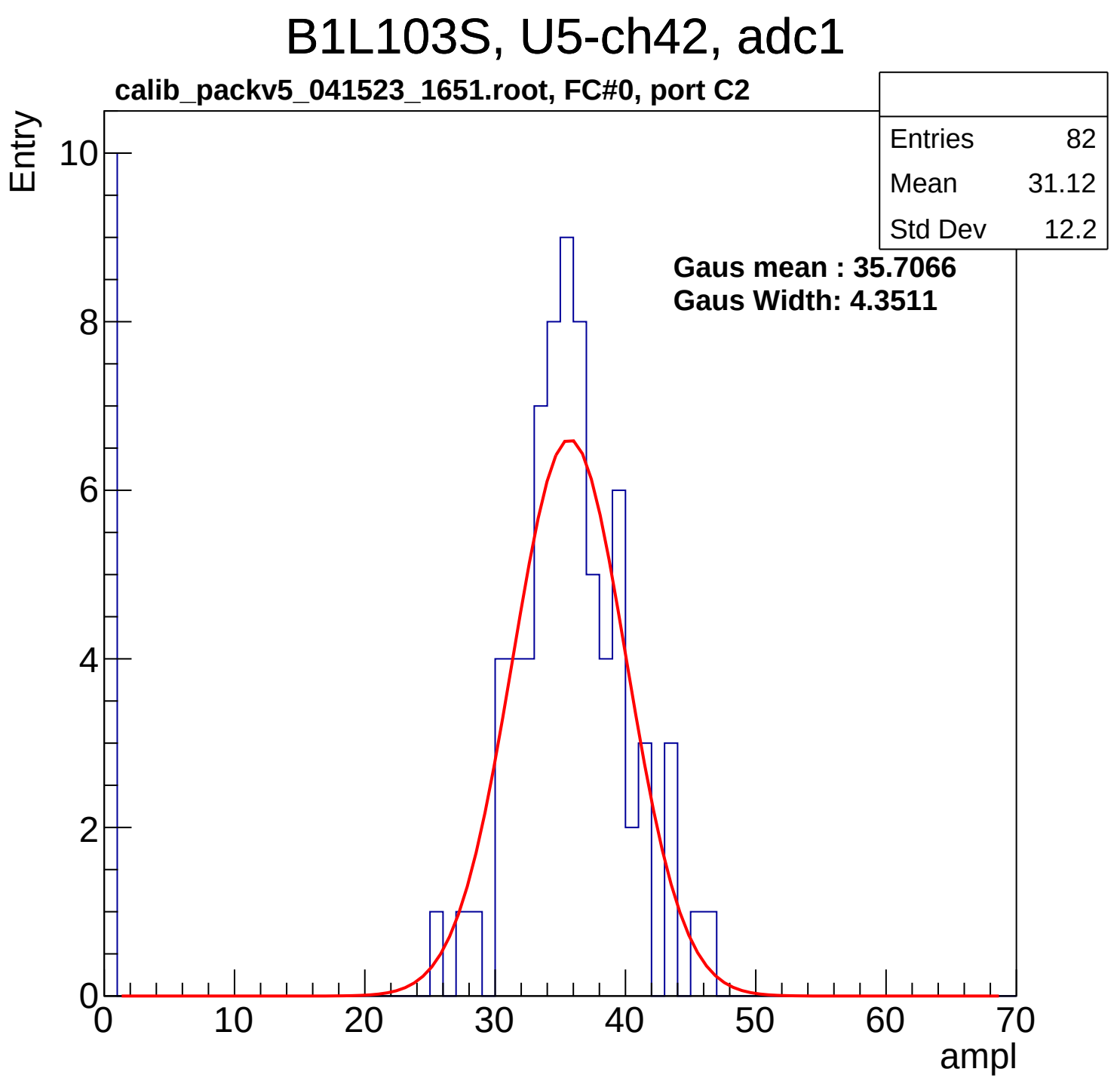
B1L103S, U5-ch42, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 31.12
Std Dev 12.2
Gaus mean : 35.7066
Gaus Width: 4.3511
Entry
ampl
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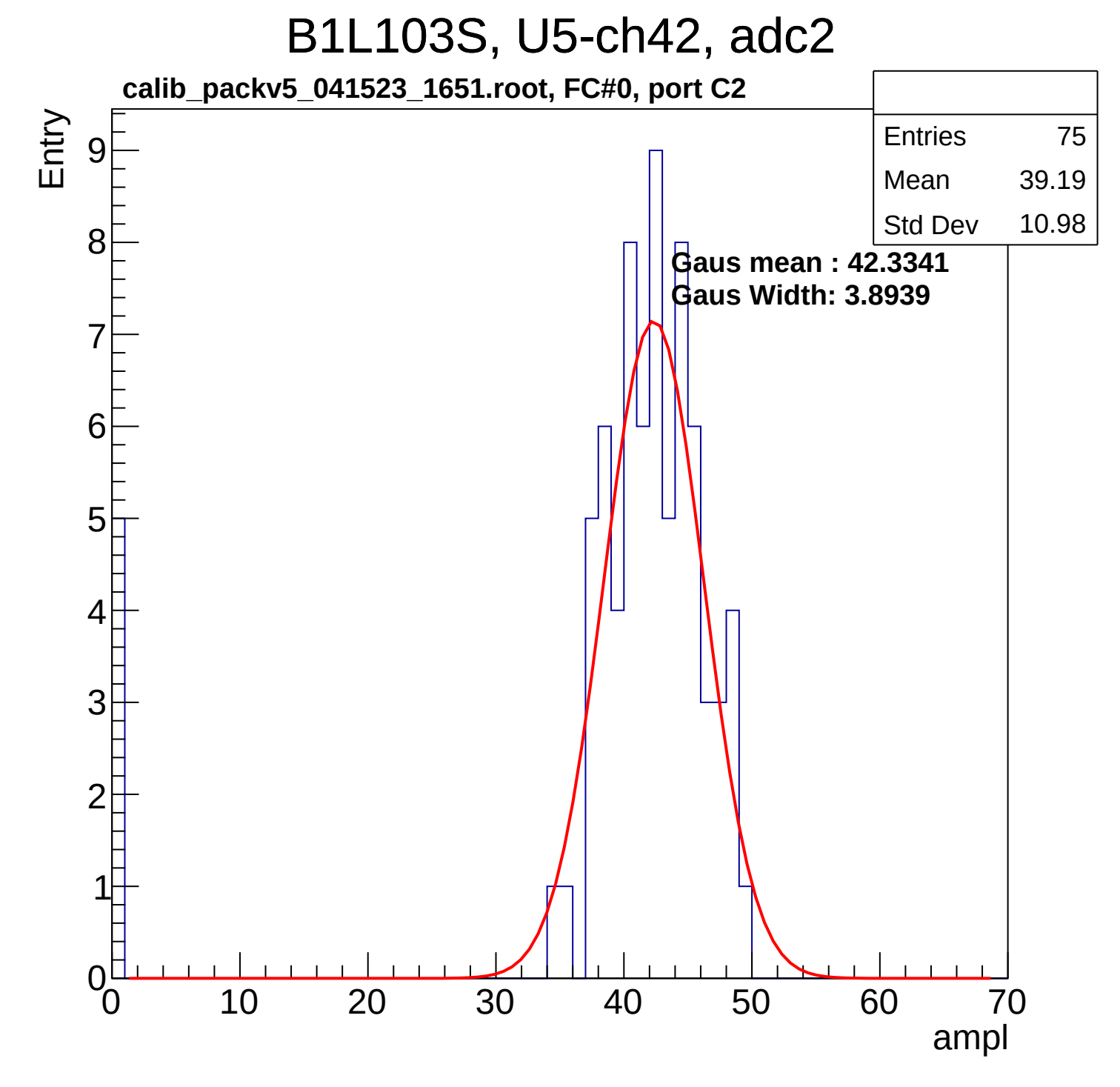
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U5-ch42, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 39.19
Std Dev 10.98
Gaus mean : 42.3341
Gaus Width: 3.8939
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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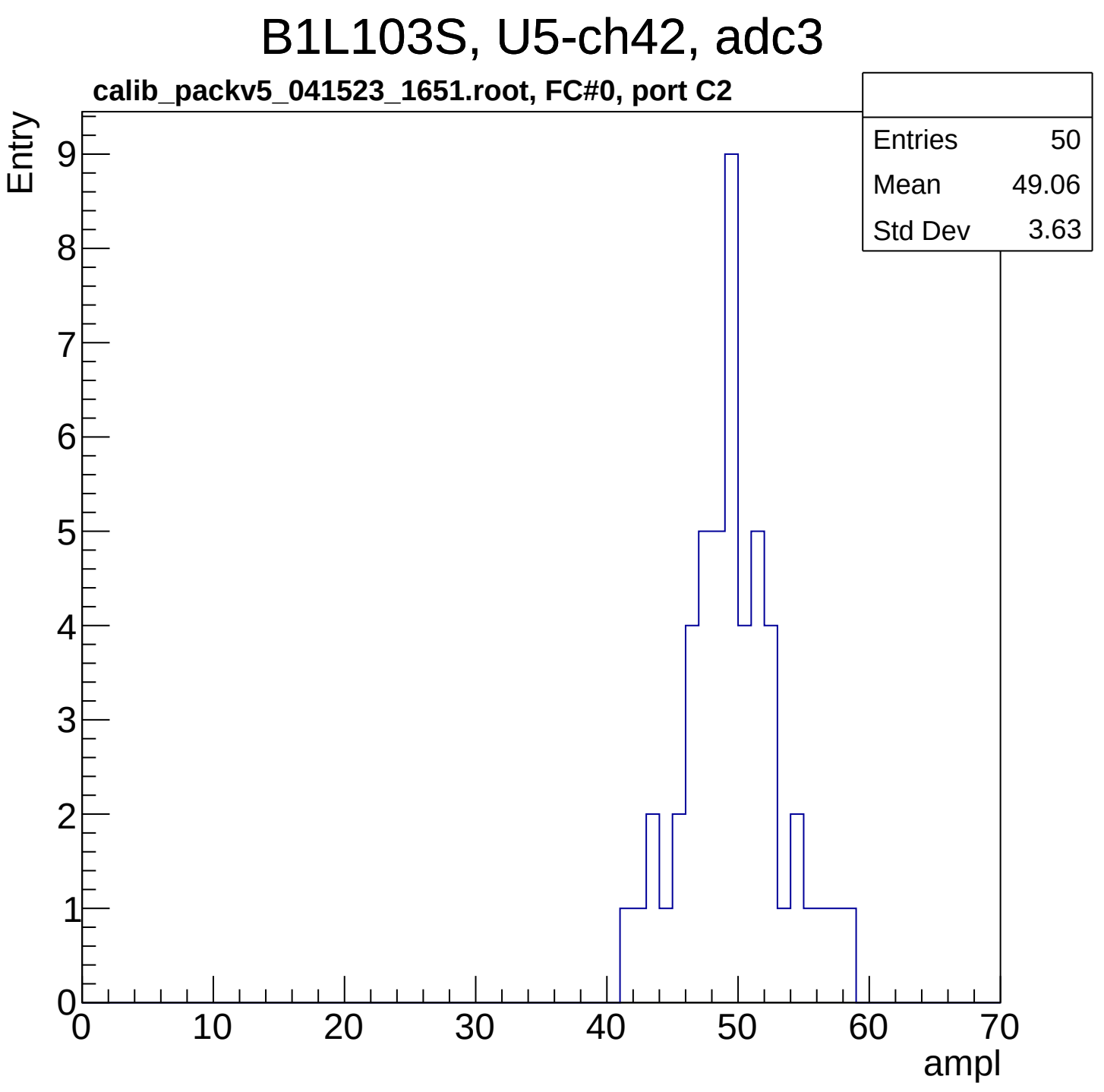
B1L103S, U5-ch42, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 49.06
Std Dev 3.63
Entry
ampl
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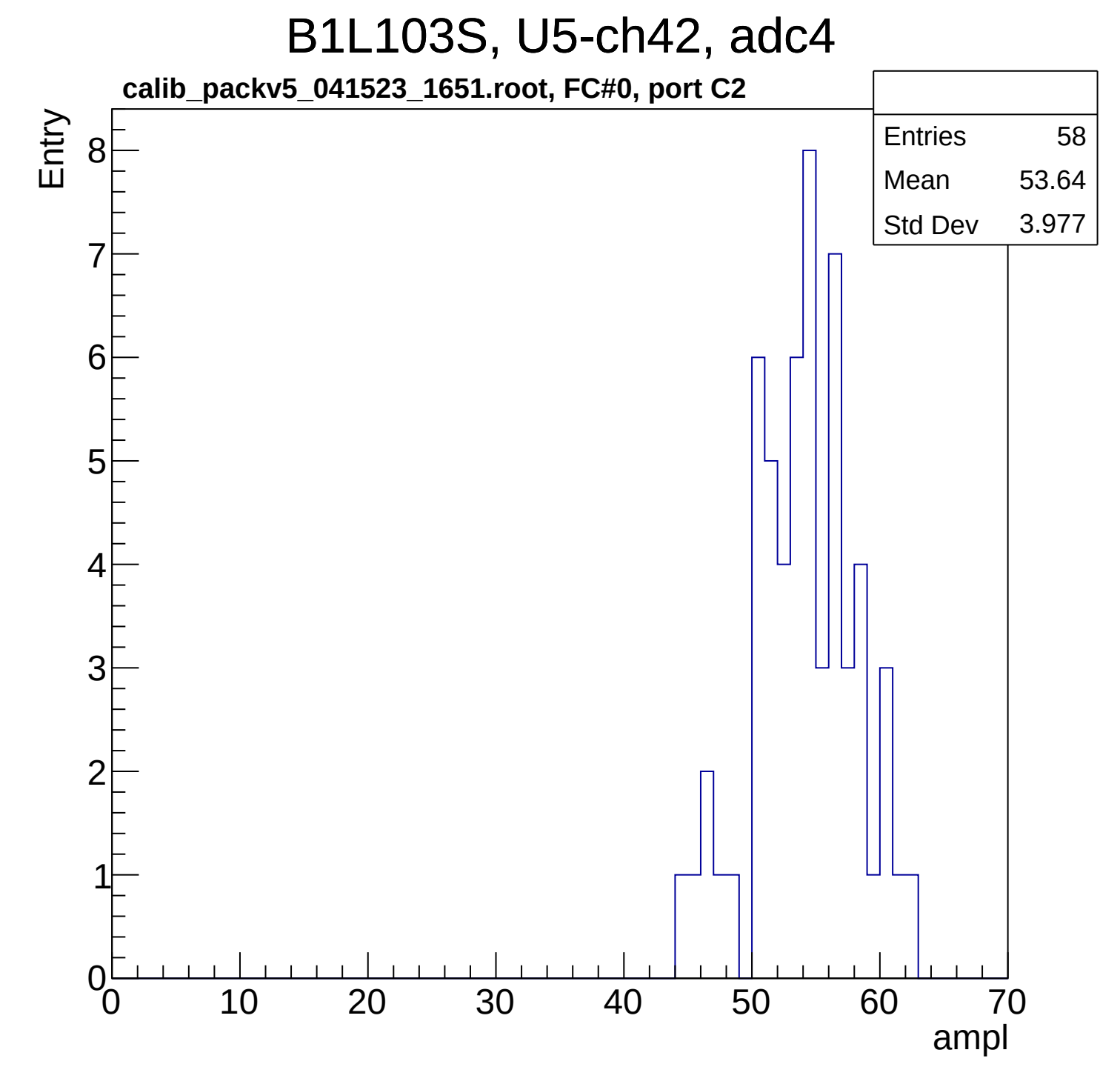
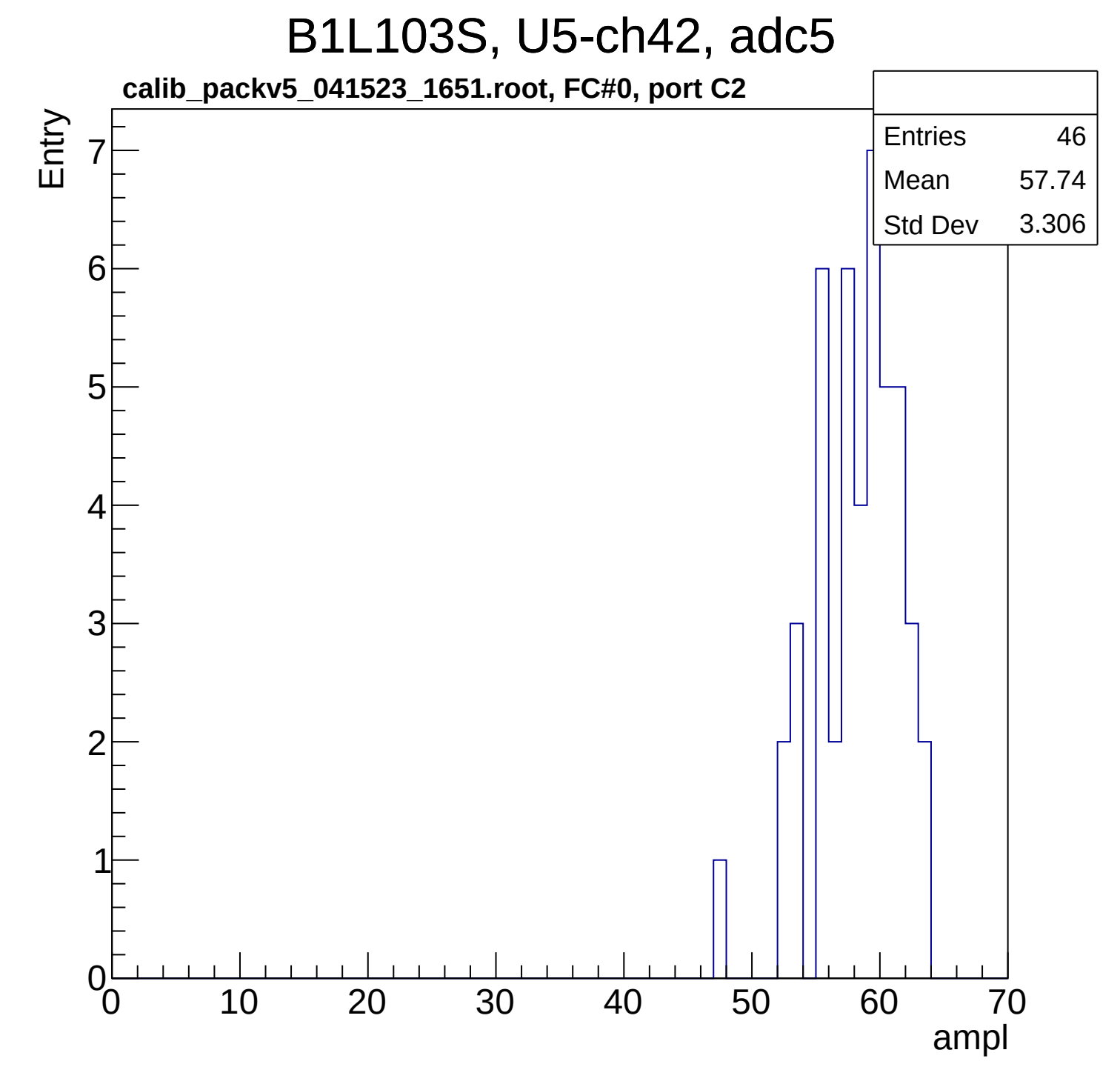

B1L103S, U5-ch42, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 53.64
Std Dev 3.977
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U5-ch42, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 57.74
Std Dev 3.306
Entry
ampl
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1
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4
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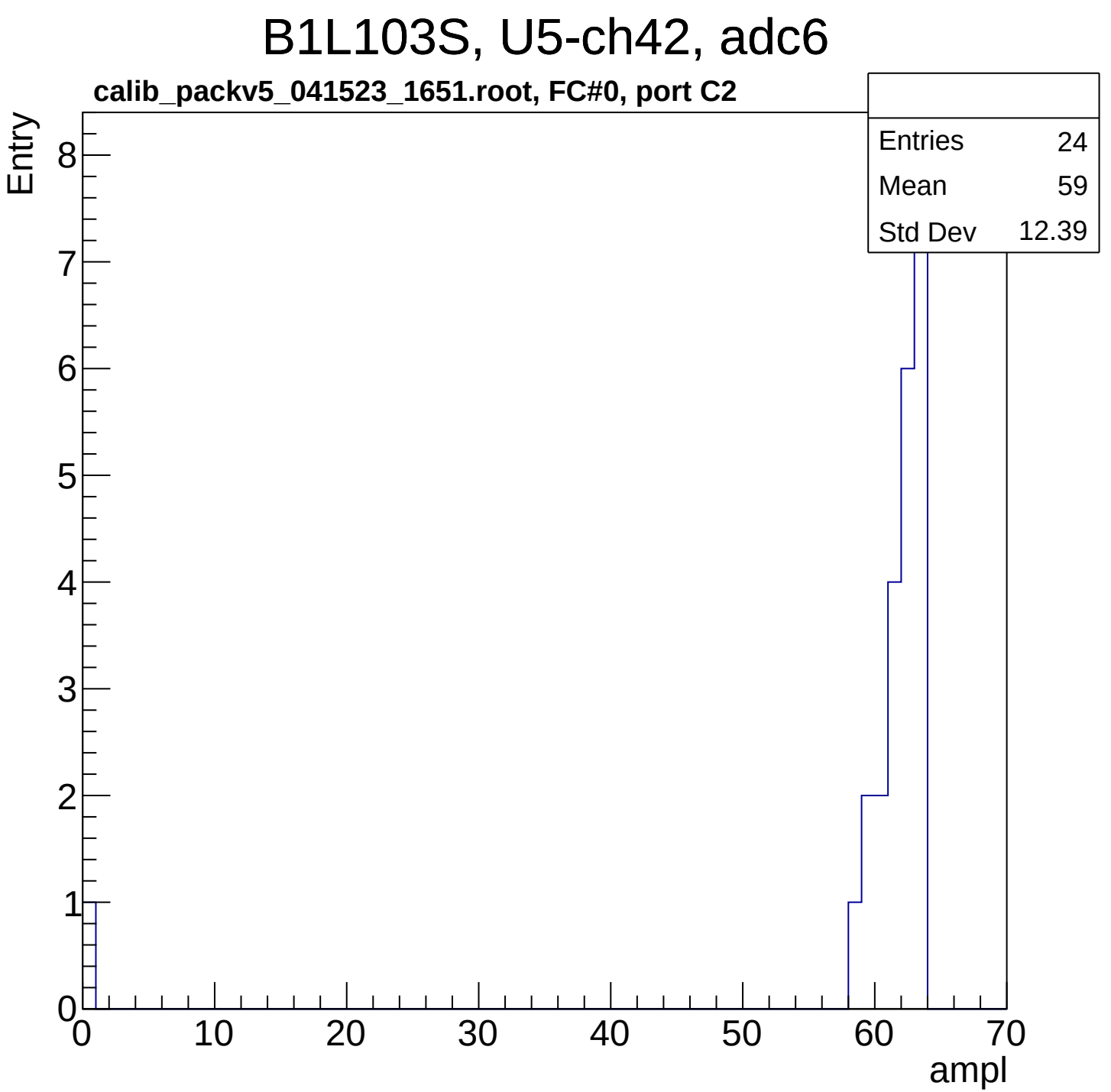
B1L103S, U5-ch42, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 59
Std Dev 12.39
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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40
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60
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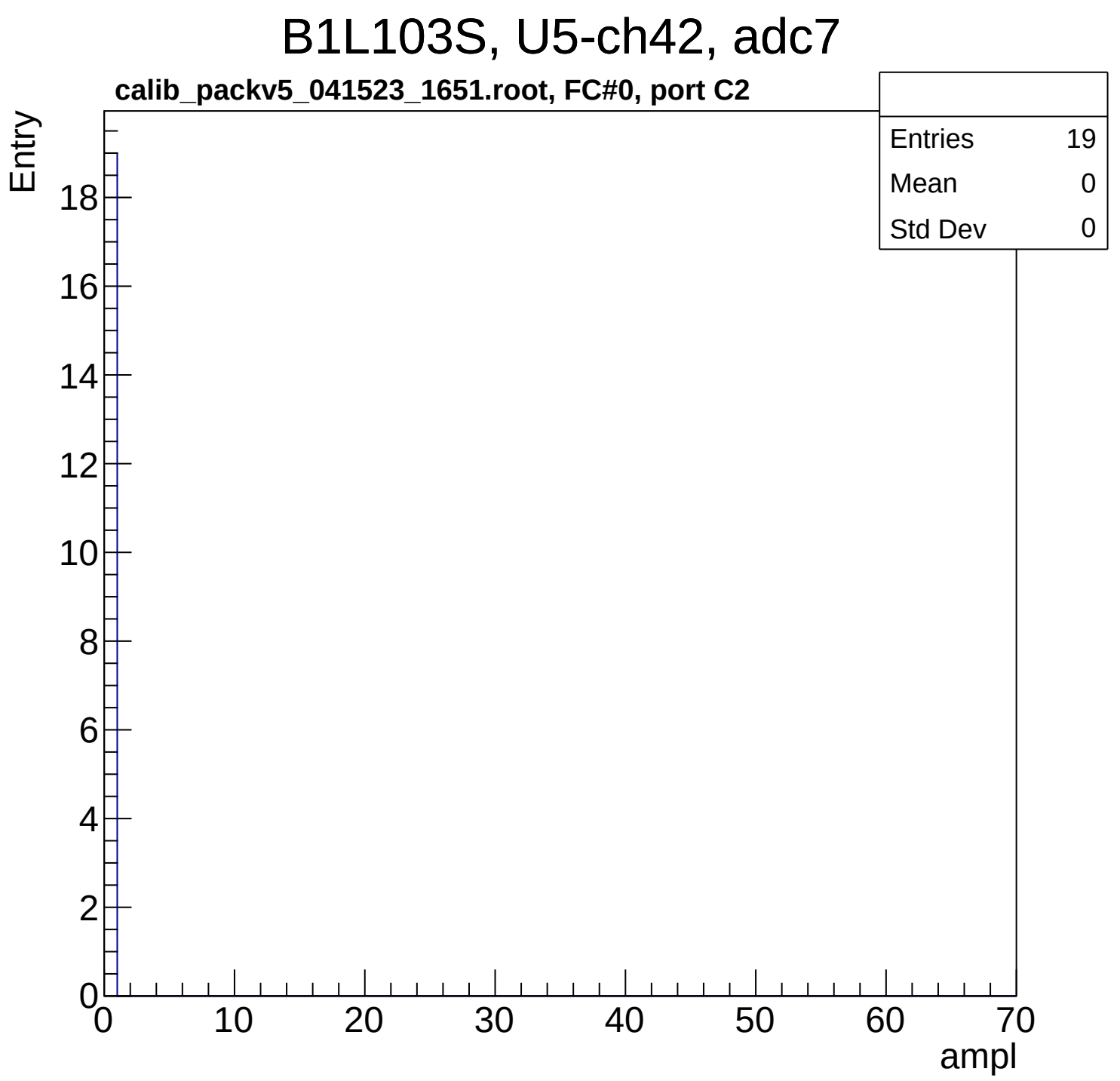
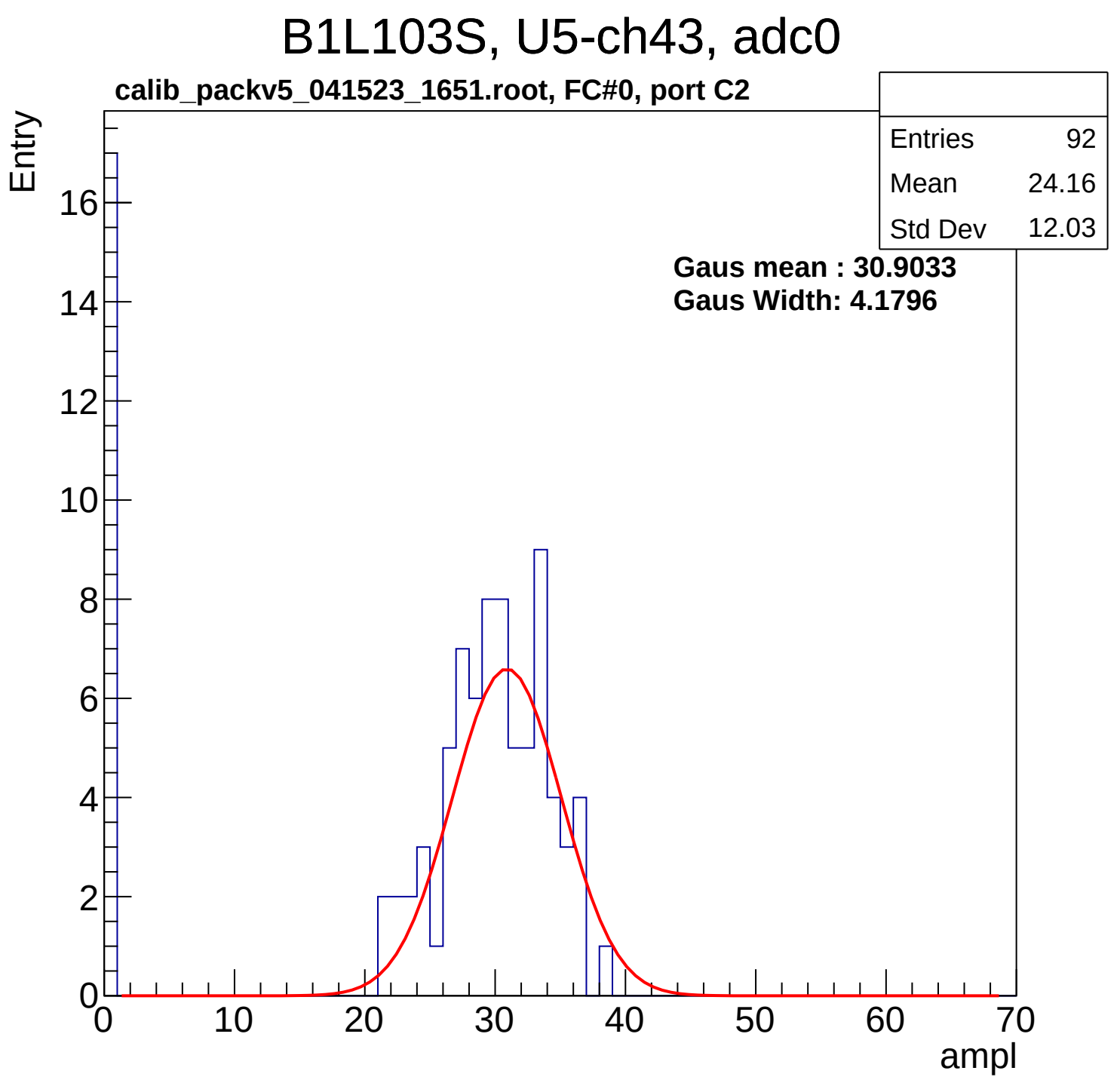
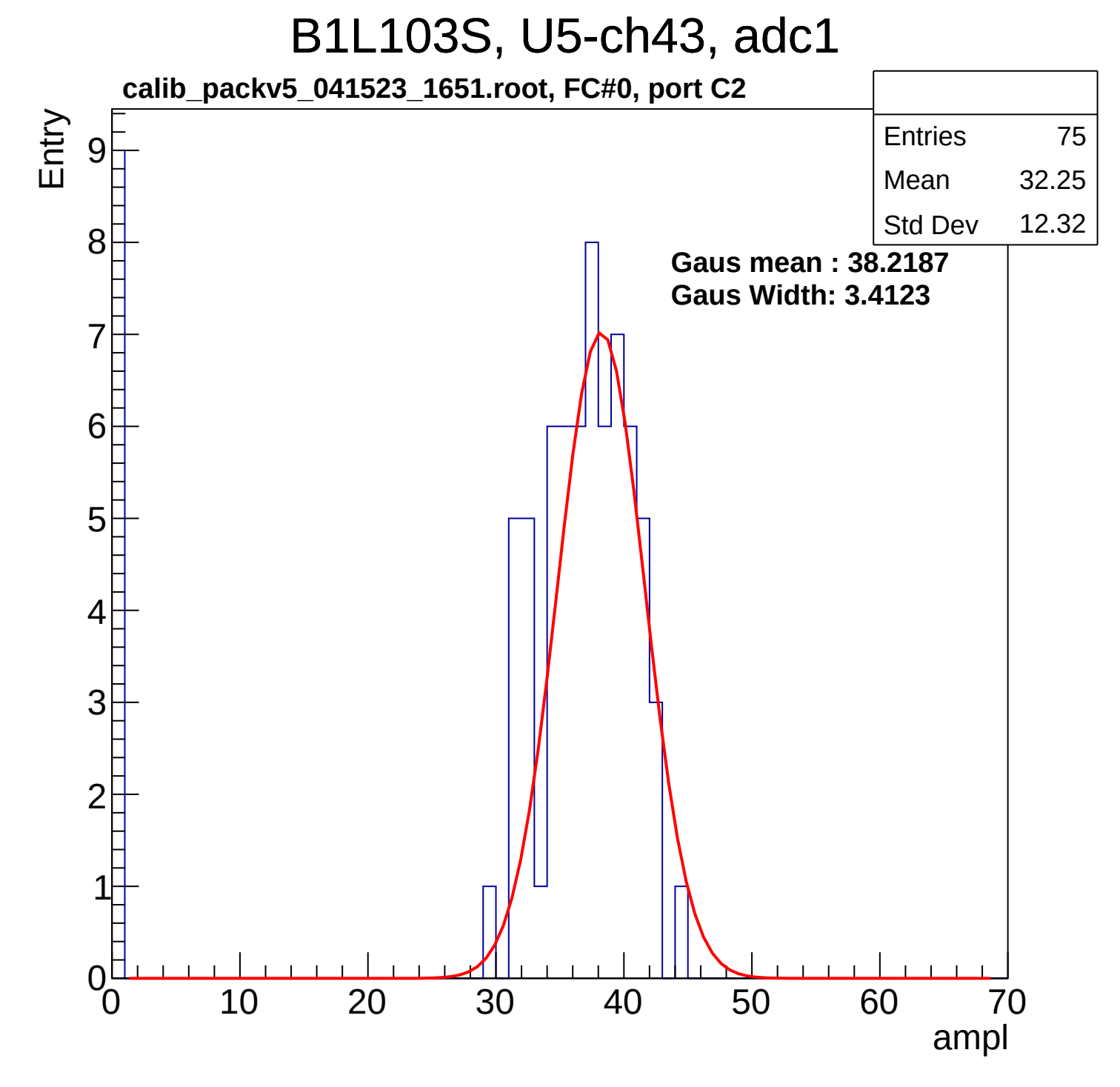

B1L103S, U5-ch42, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch43, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 24.16
Std Dev 12.03
Gaus mean : 30.9033
Gaus Width: 4.1796
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U5-ch43, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 32.25
Std Dev 12.32
Gaus mean : 38.2187
Gaus Width: 3.4123
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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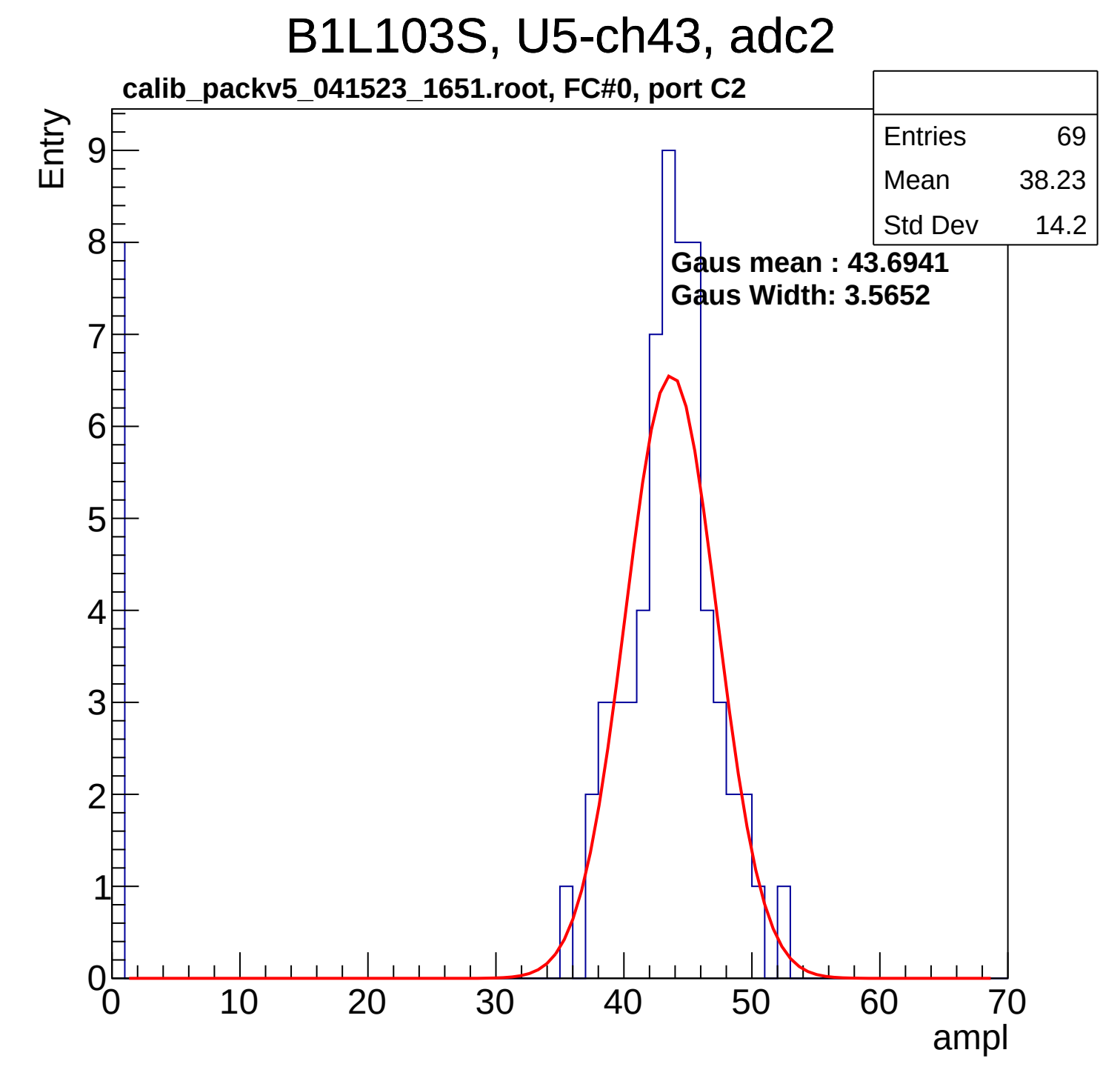
B1L103S, U5-ch43, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 38.23
Std Dev 14.2
Gaus mean : 43.6941
Gaus Width: 3.5652
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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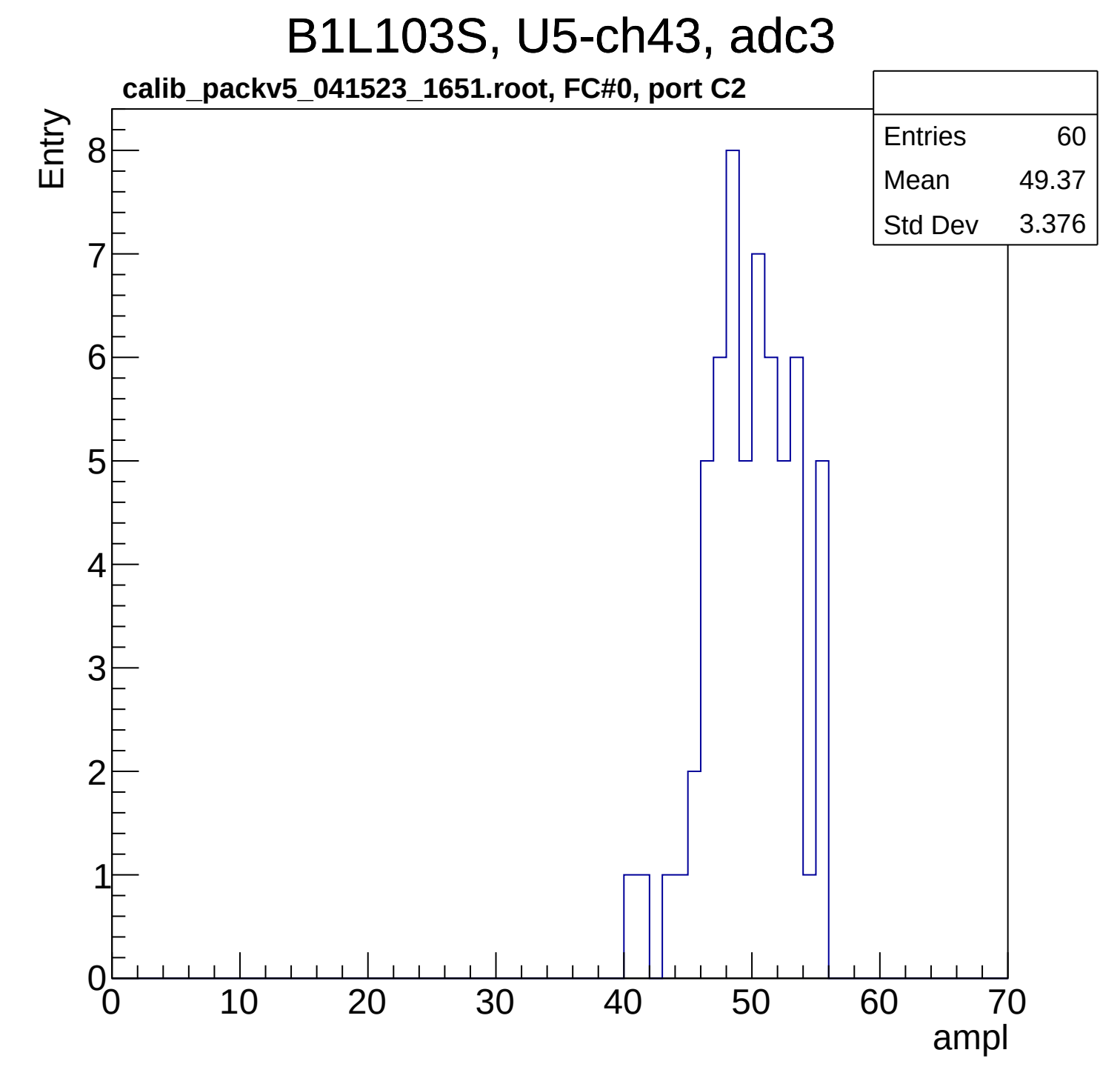
B1L103S, U5-ch43, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 49.37
Std Dev 3.376
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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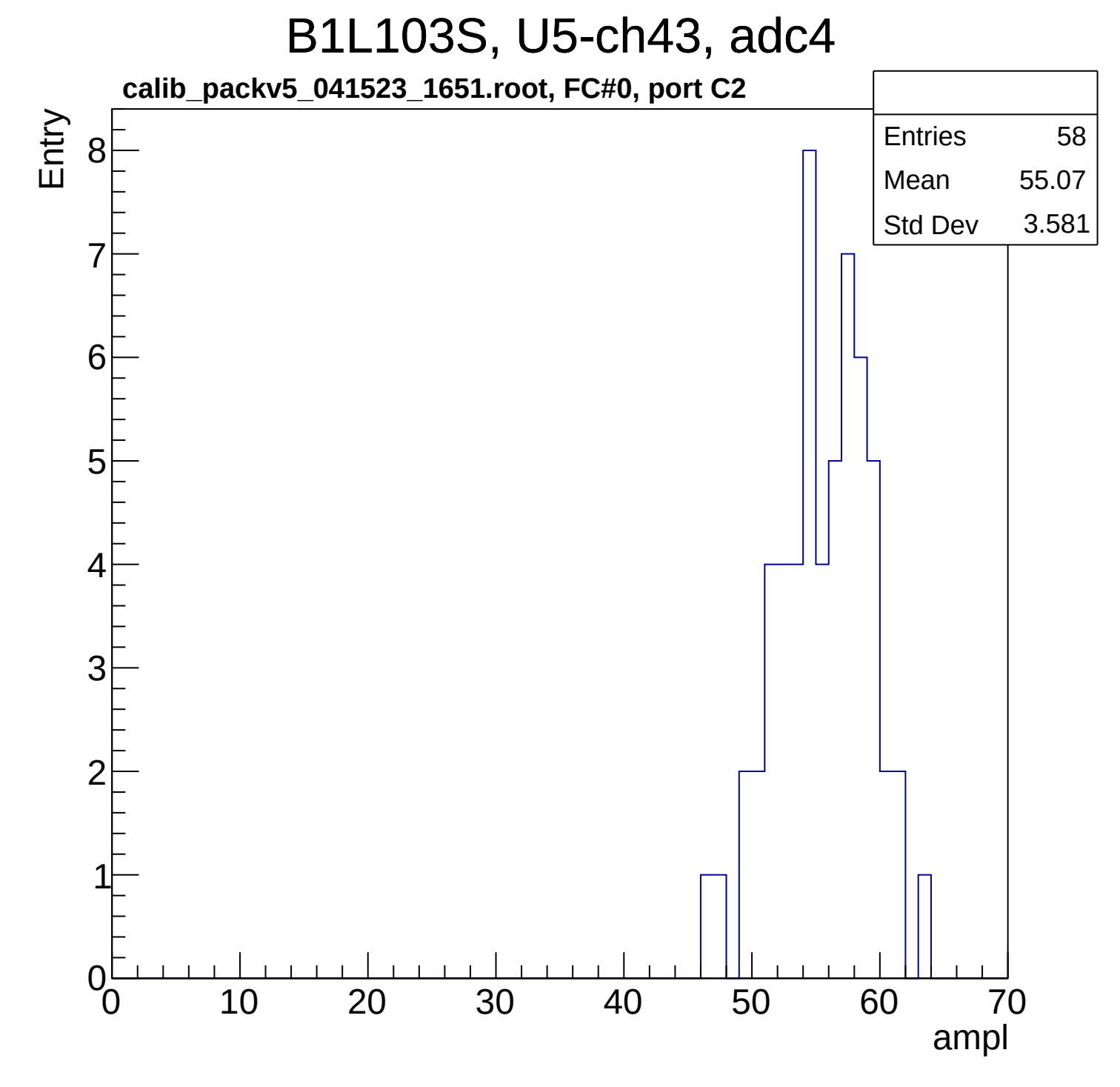
B1L103S, U5-ch43, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 55.07
Std Dev 3.581
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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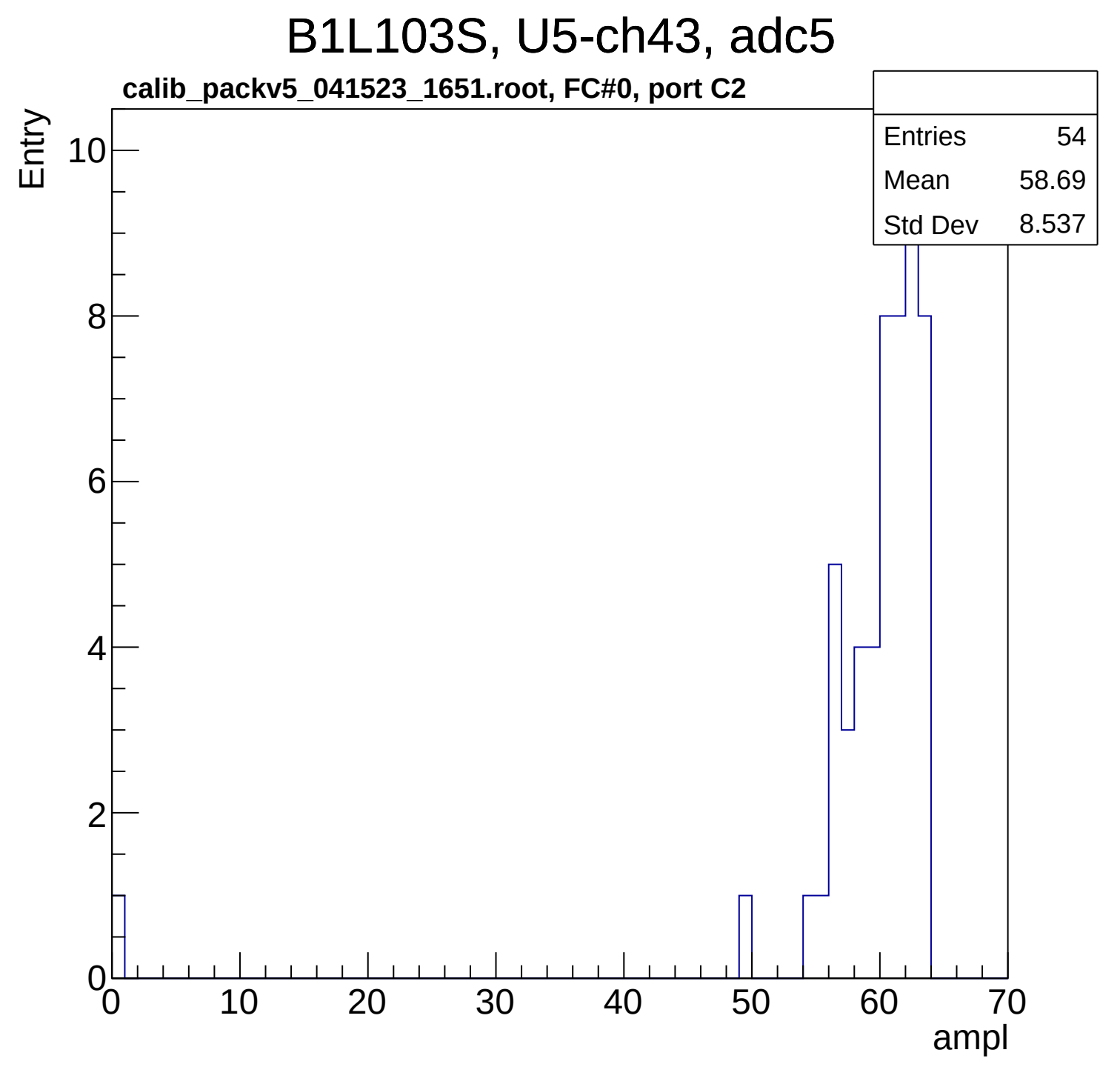
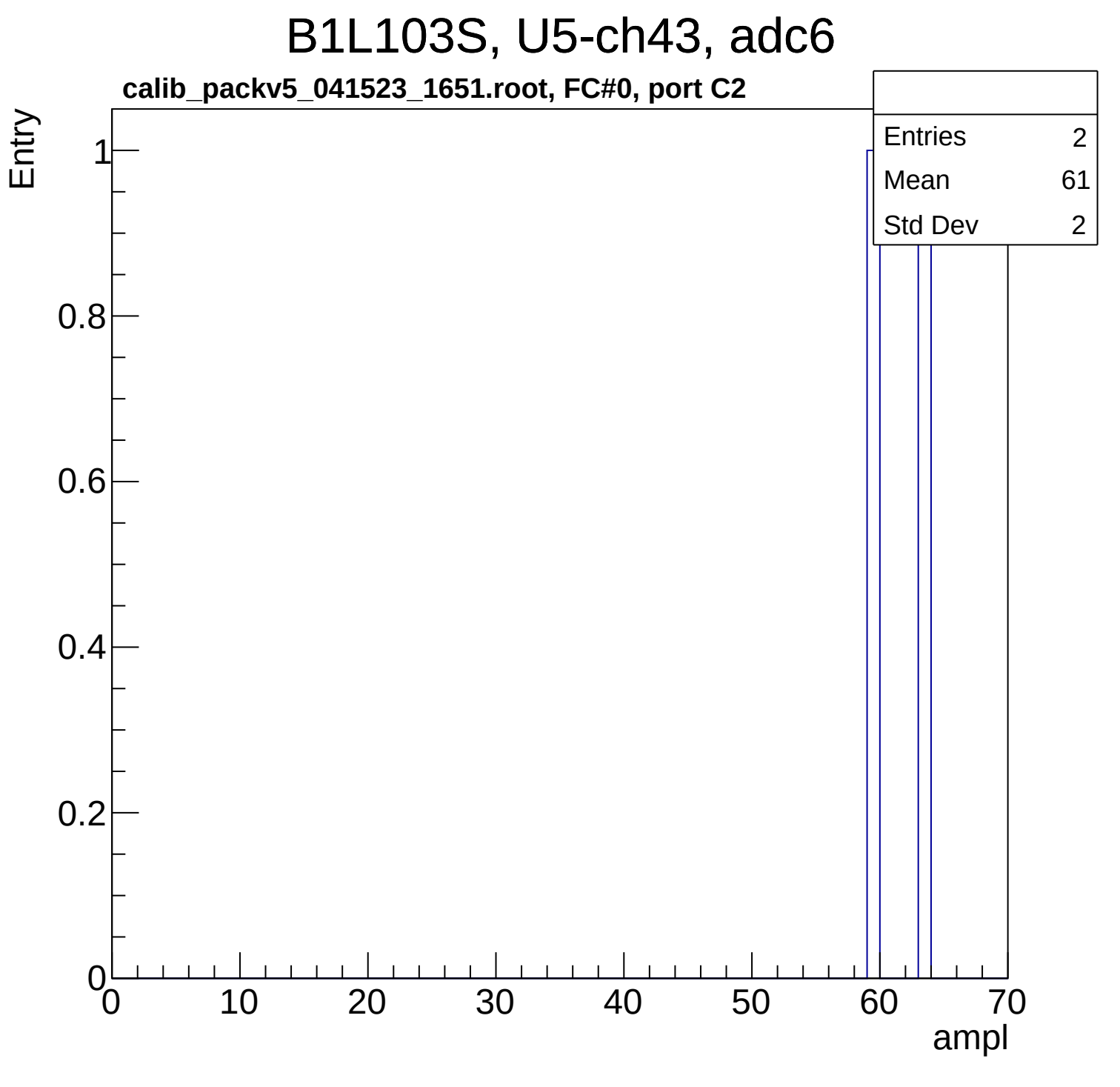
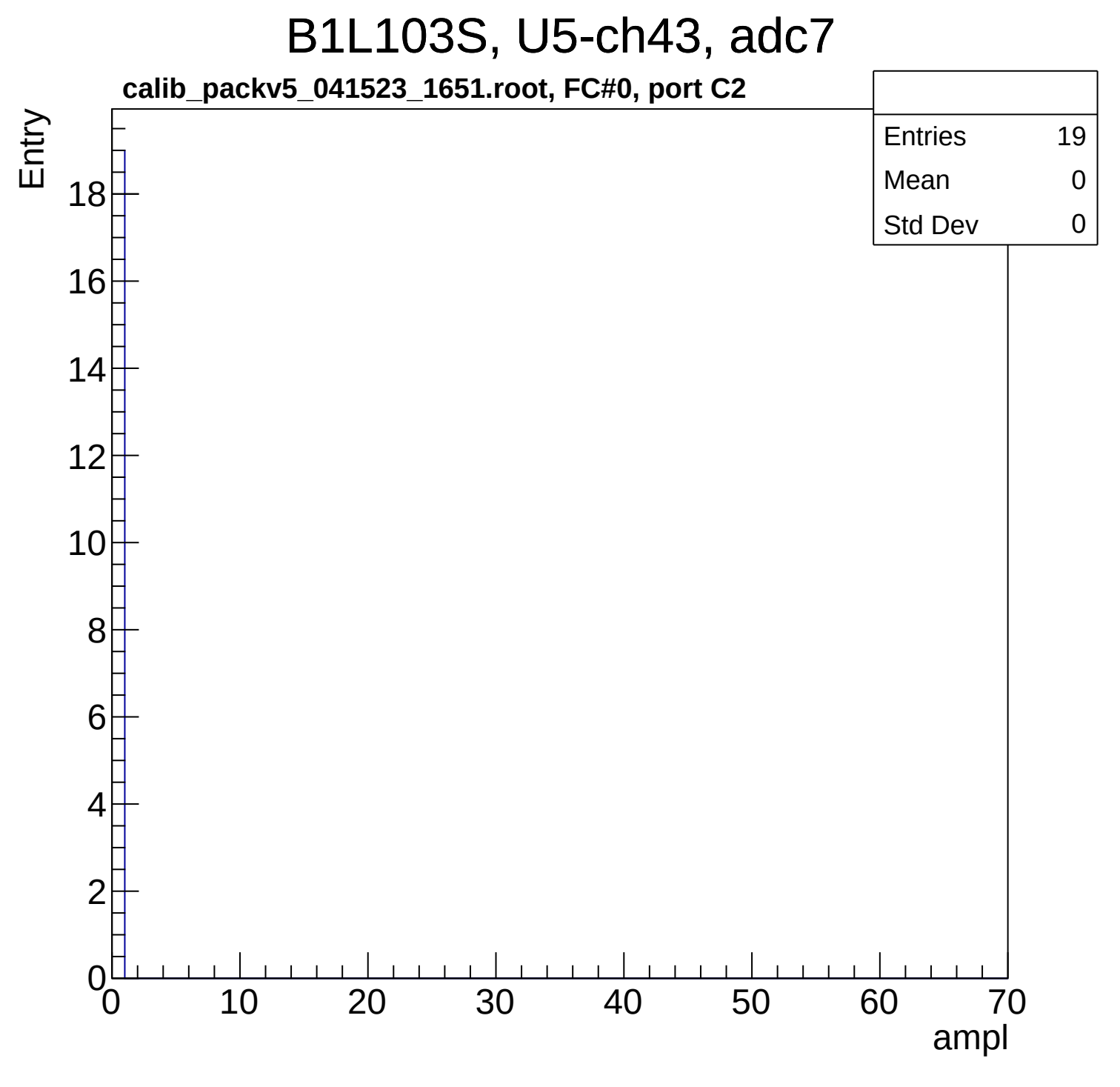
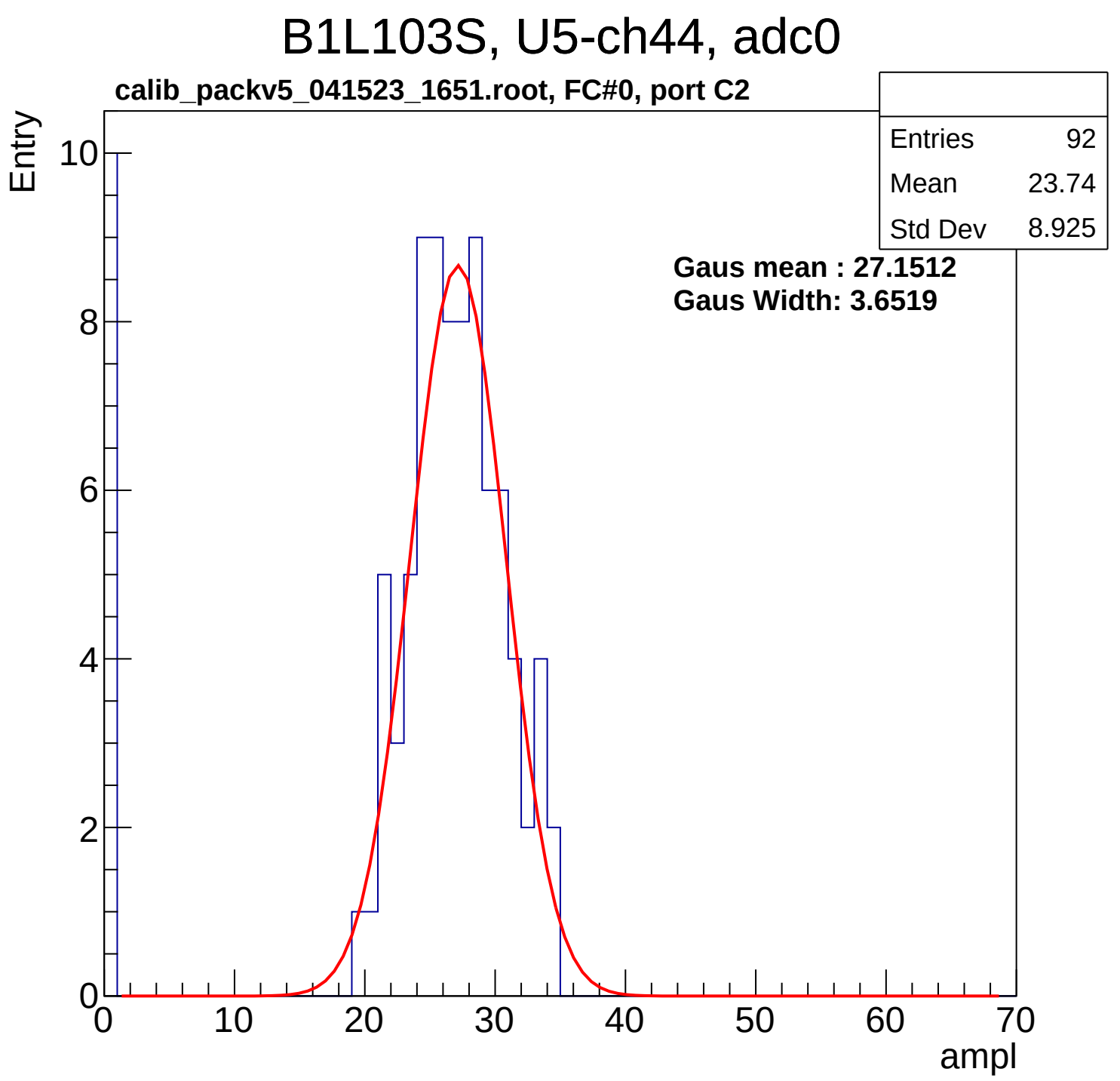
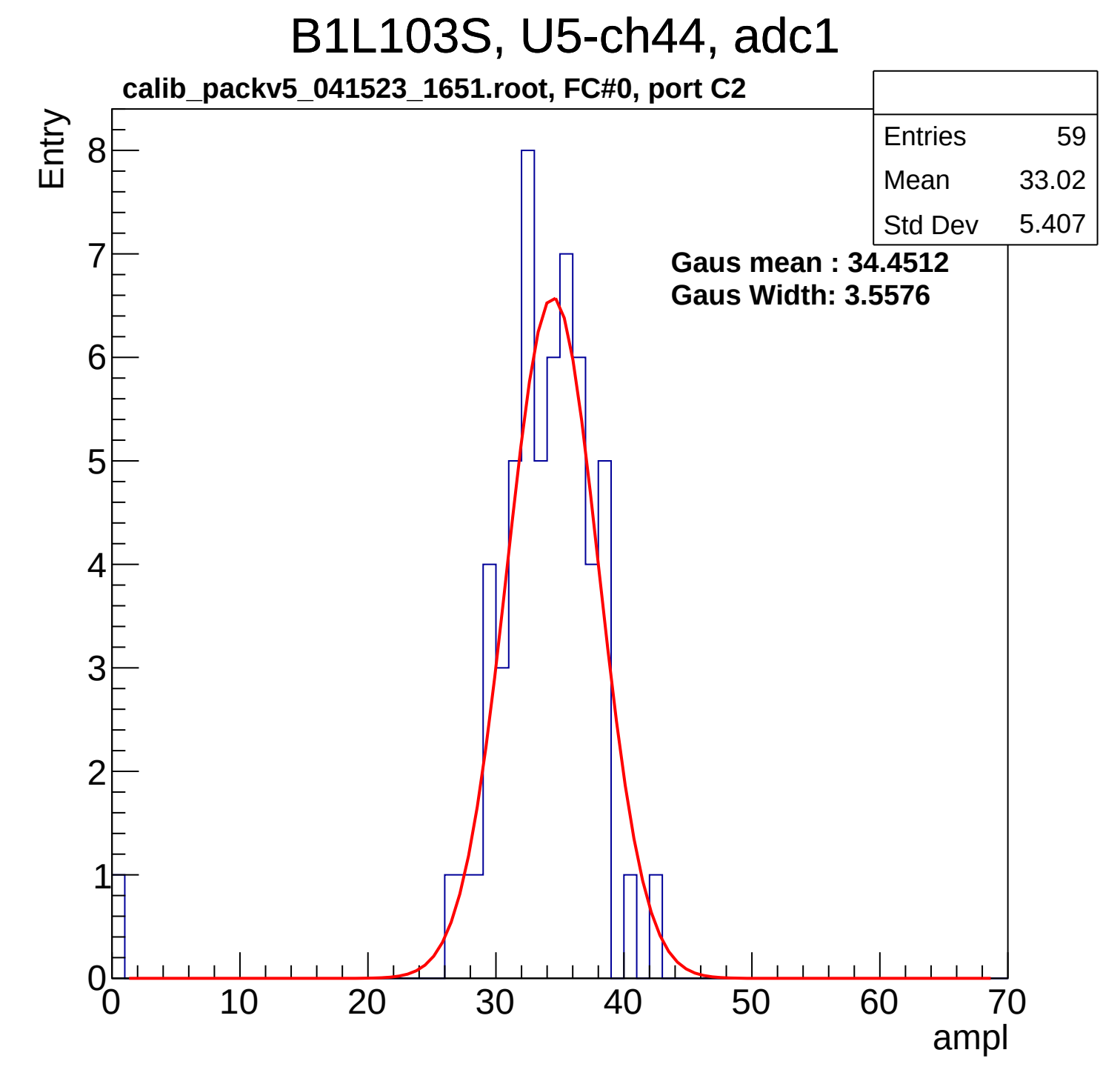

B1L103S, U5-ch43, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.69
Std Dev 8.537
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U5-ch43, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 61
Std Dev 2
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch43, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch44, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 23.74
Std Dev 8.925
Gaus mean : 27.1512
Gaus Width: 3.6519
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U5-ch44, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 33.02
Std Dev 5.407
Gaus mean : 34.4512
Gaus Width: 3.5576
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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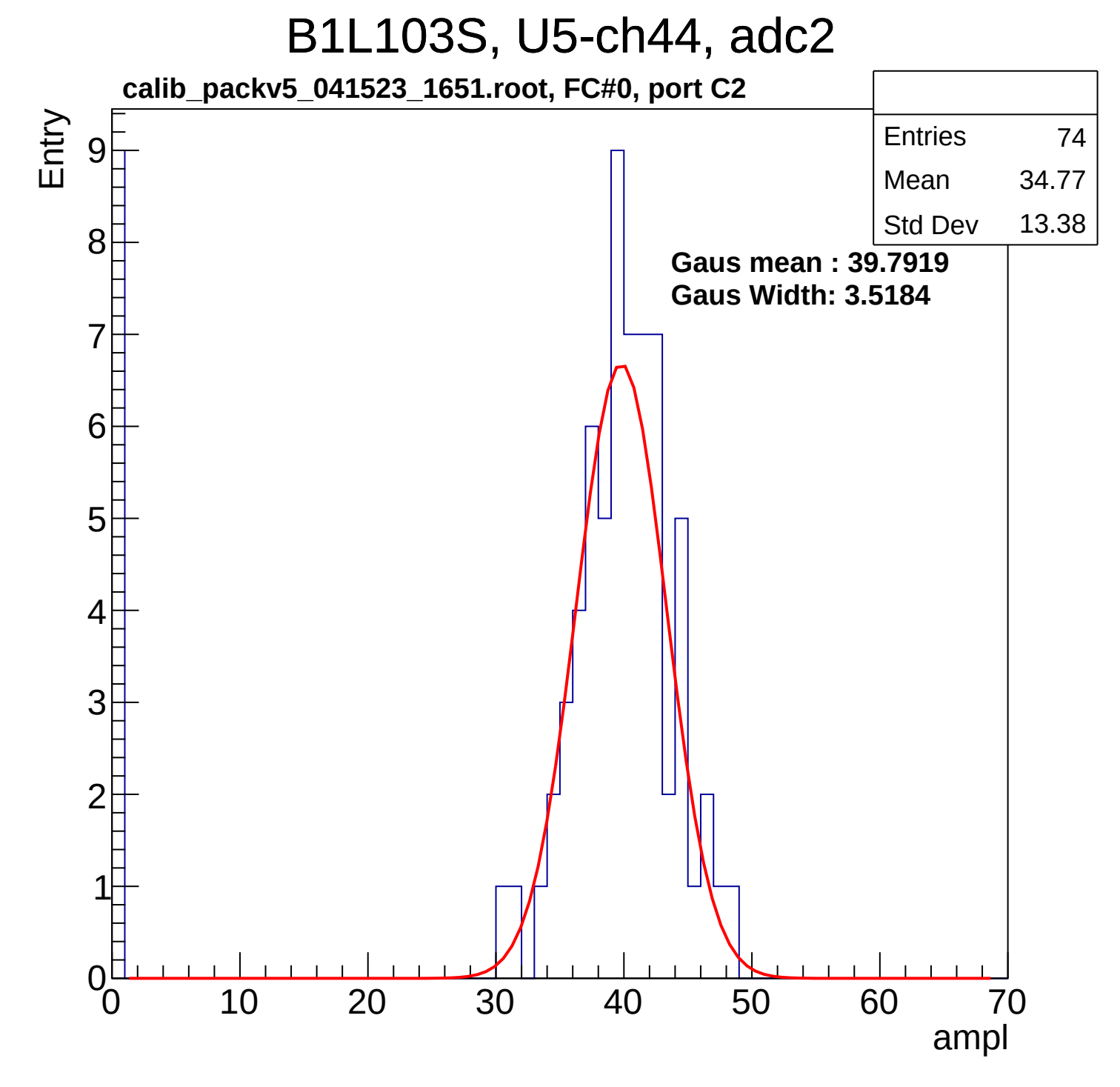
B1L103S, U5-ch44, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 34.77
Std Dev 13.38
Gaus mean : 39.7919
Gaus Width: 3.5184
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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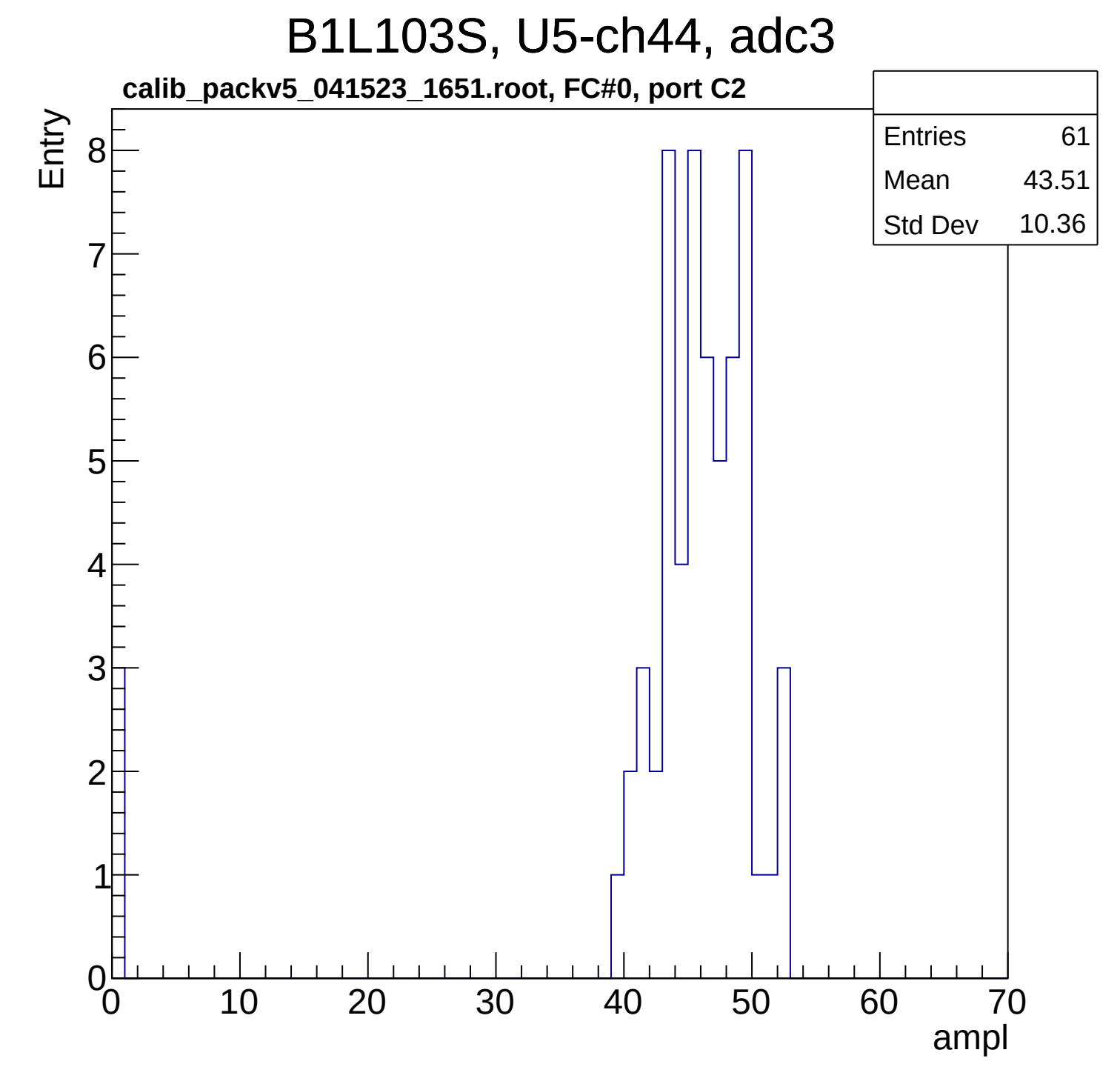
B1L103S, U5-ch44, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 43.51
Std Dev 10.36
Entry
ampl
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1
2
3
4
5
6
7
8
0
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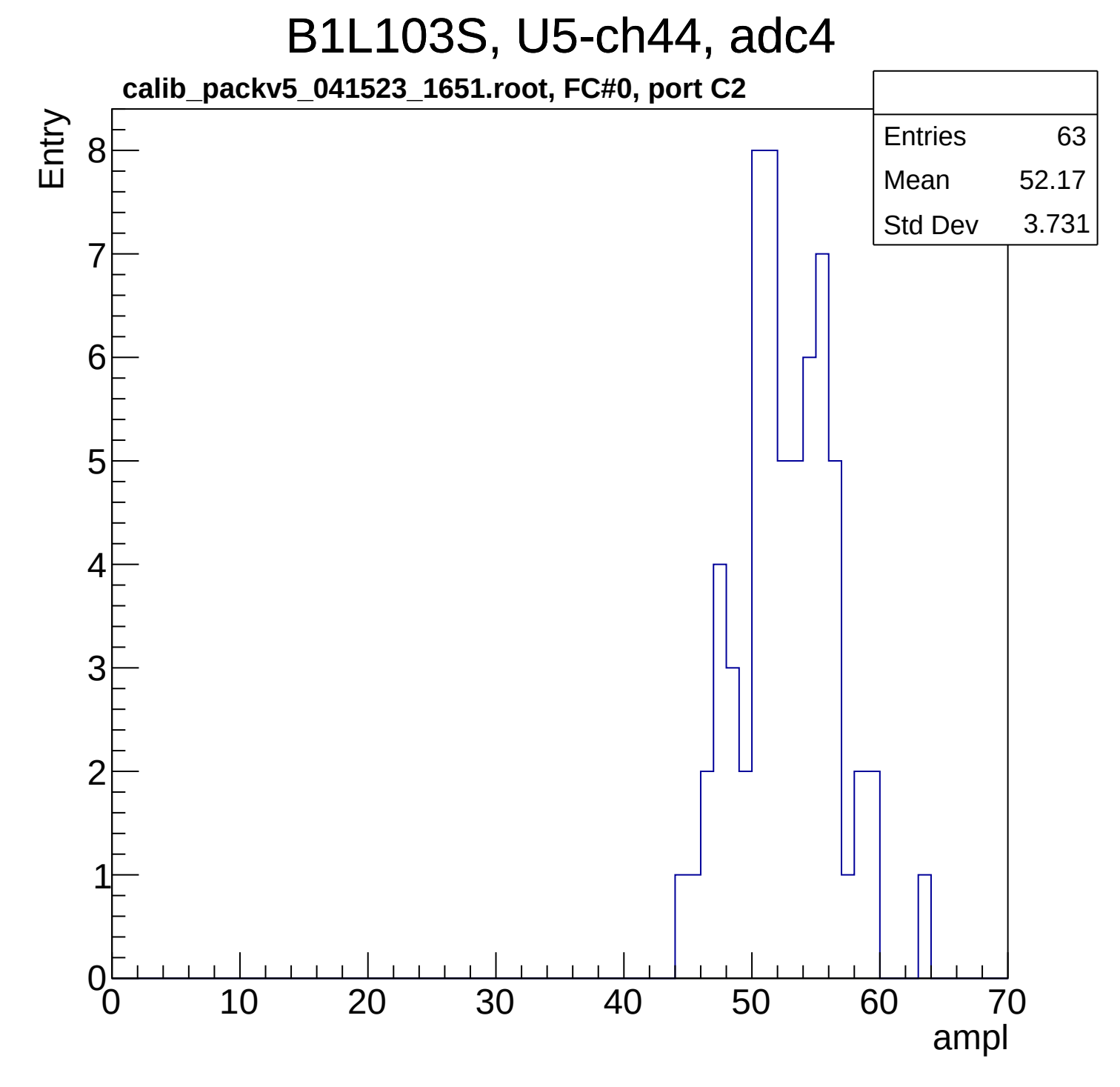
B1L103S, U5-ch44, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 52.17
Std Dev 3.731
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
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60
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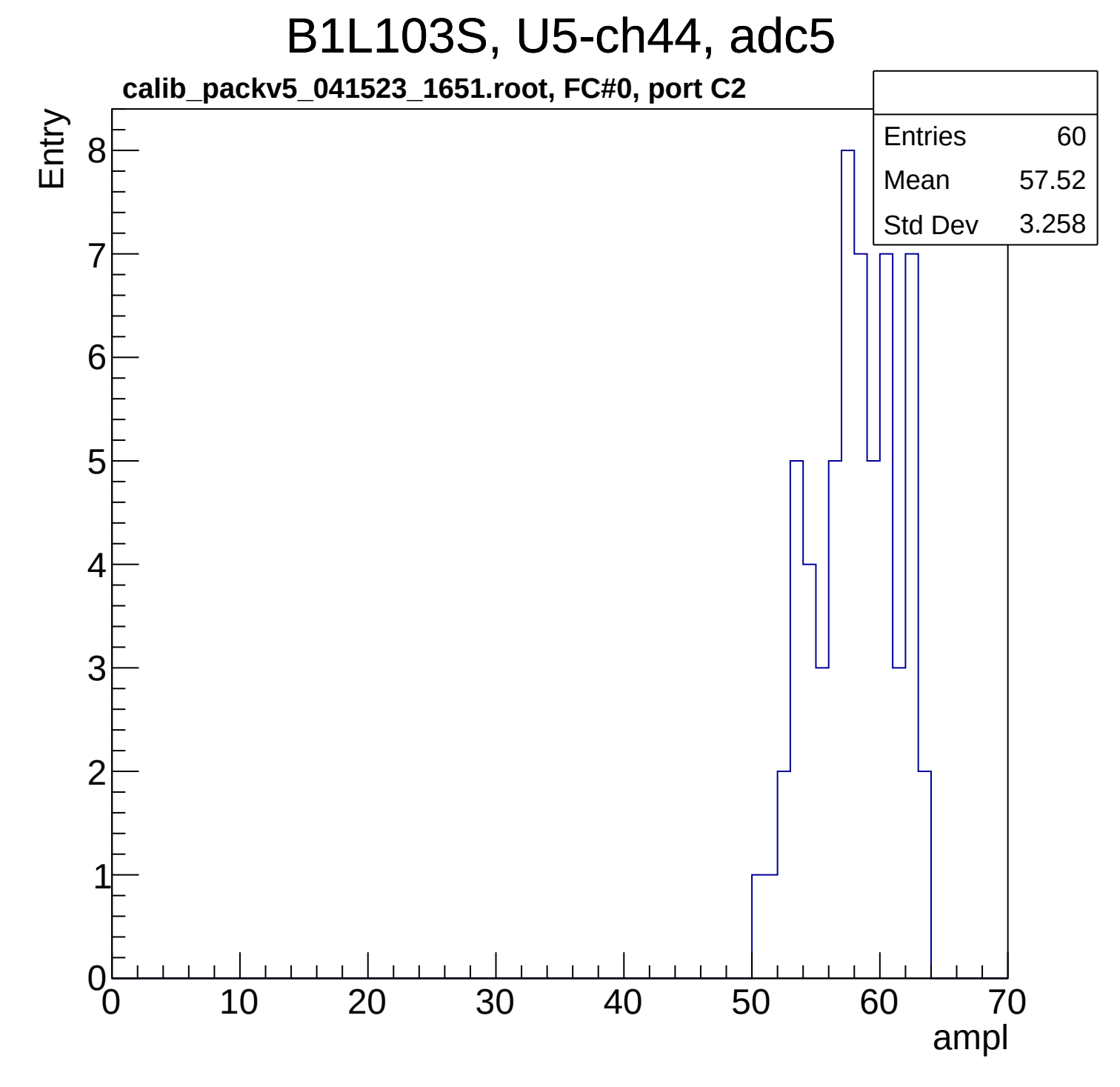
B1L103S, U5-ch44, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 57.52
Std Dev 3.258
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
50
60
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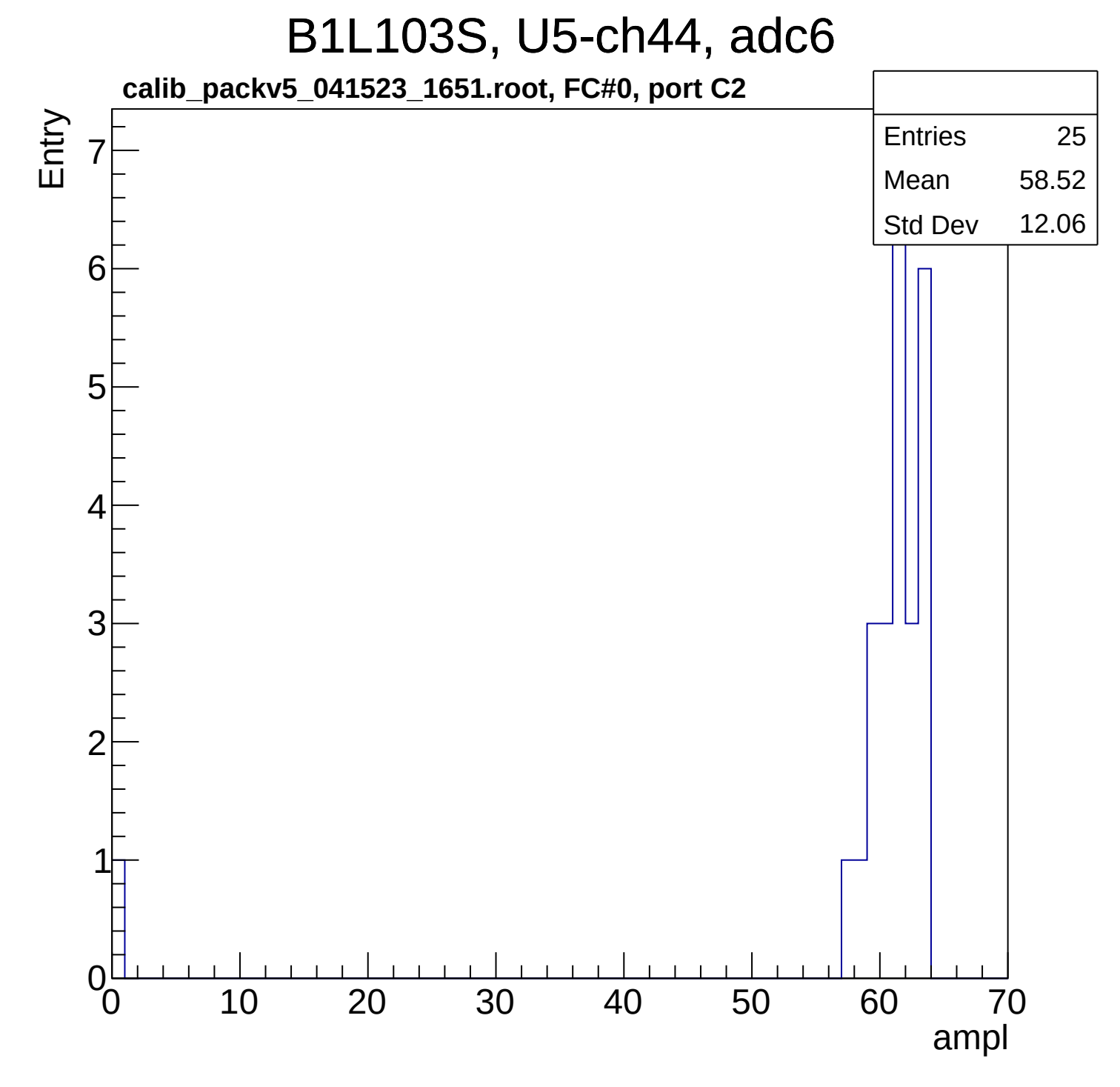
B1L103S, U5-ch44, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 58.52
Std Dev 12.06
Entry
ampl
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1
2
3
4
5
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0
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40
50
60
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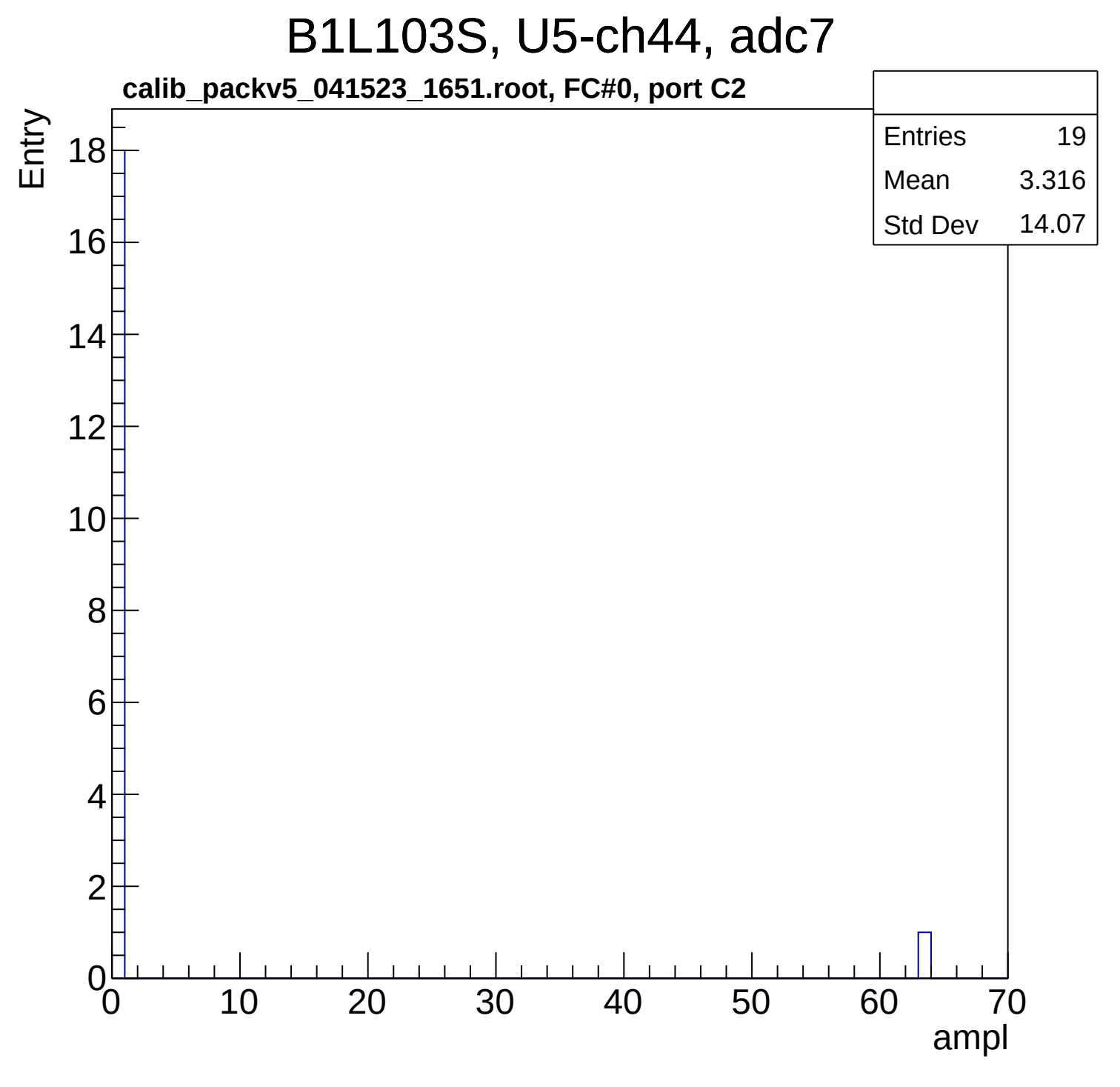
B1L103S, U5-ch44, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
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6
8
10
12
14
16
18
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10
20
30
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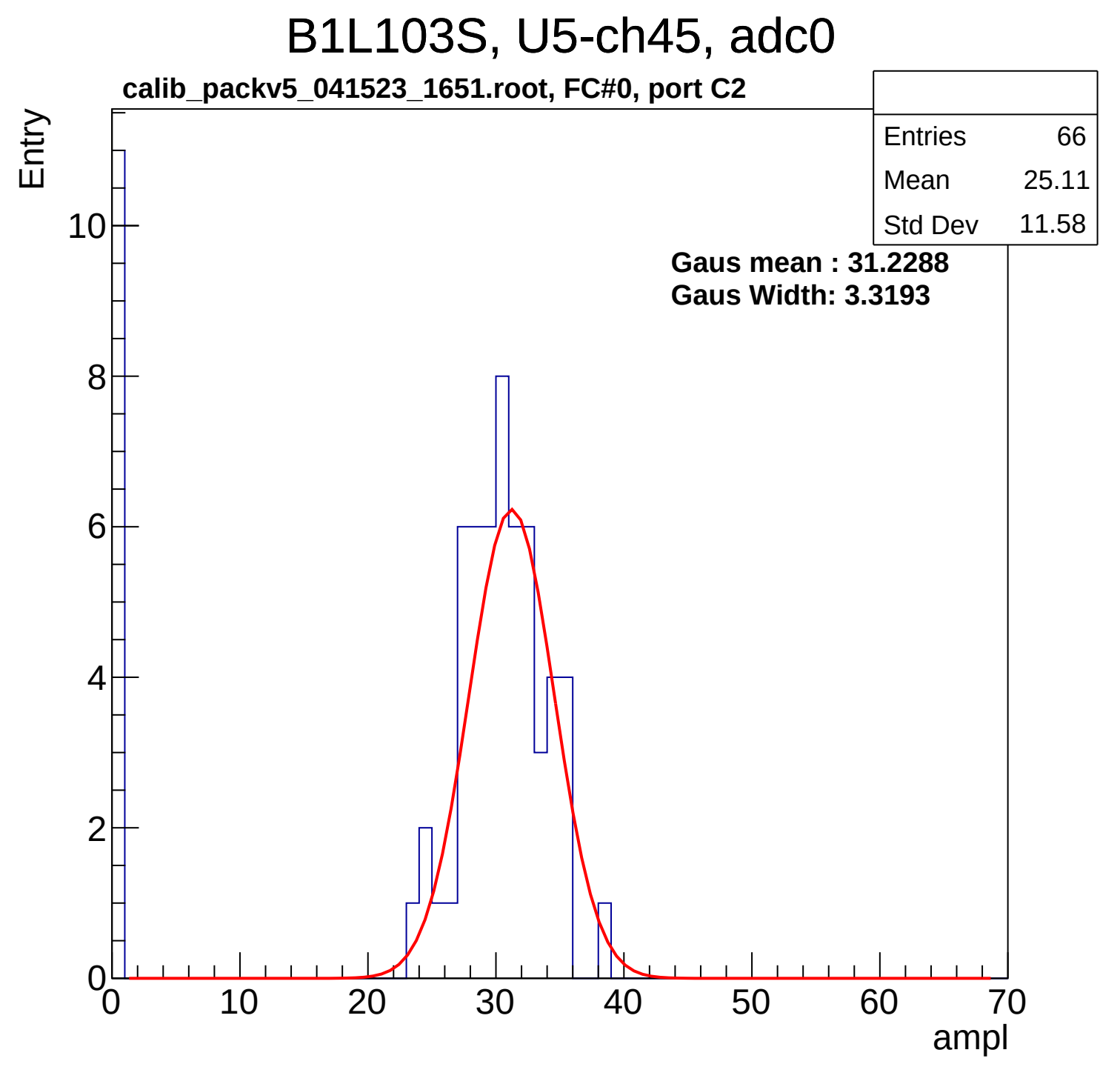
50
60
70
ampl


B1L103S, U5-ch45, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 25.11
Std Dev 11.58
Gaus mean : 31.2288
Gaus Width: 3.3193
Entry
ampl
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2
4
6
8
10
0
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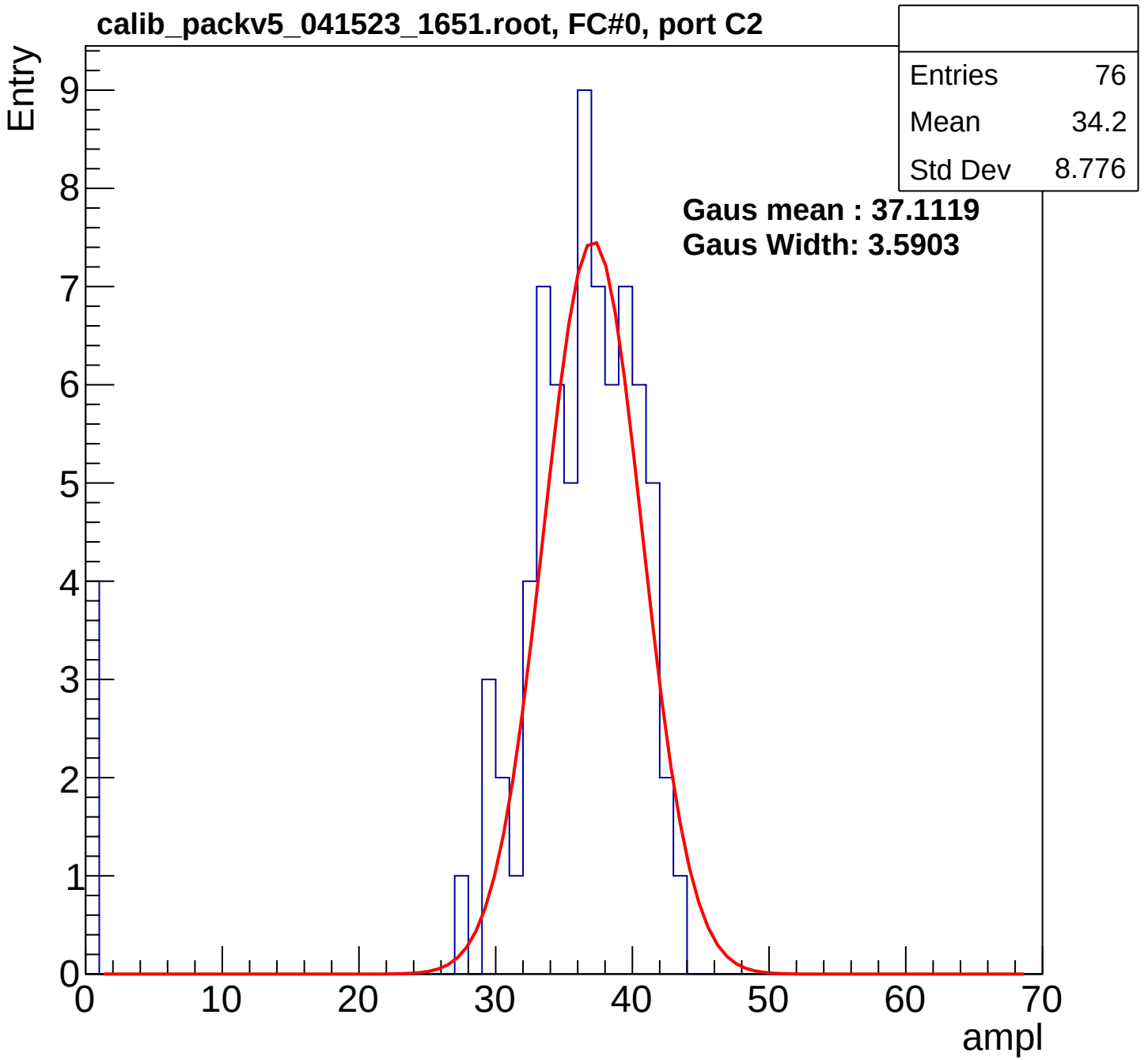
20
30
40
50
60
70


B1L103S, U5-ch45, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 34.2
Std Dev 8.776
Gaus mean : 37.1119
Gaus Width: 3.5903
Entry
ampl
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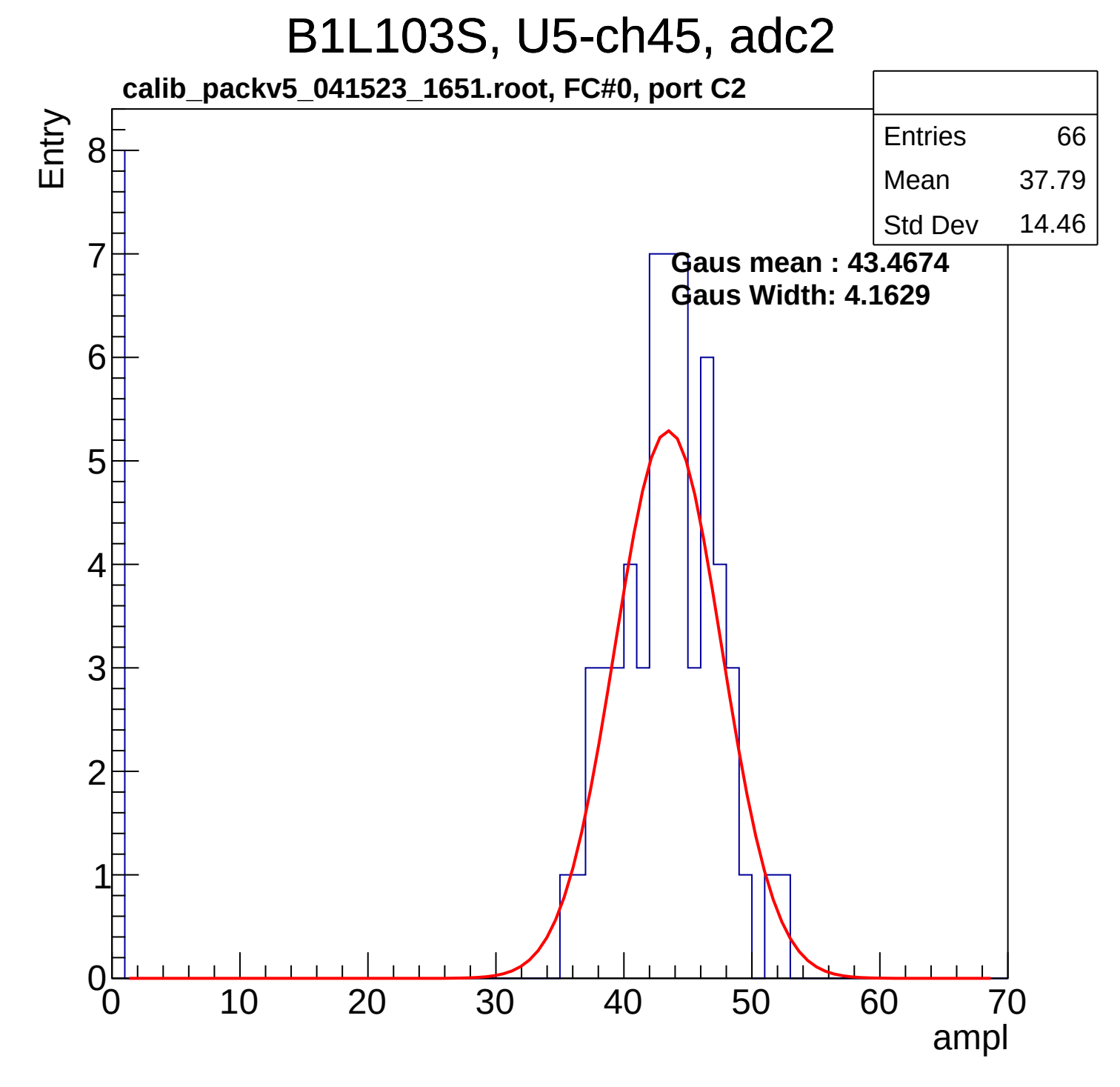
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U5-ch45, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 37.79
Std Dev 14.46
Gaus mean : 43.4674
Gaus Width: 4.1629
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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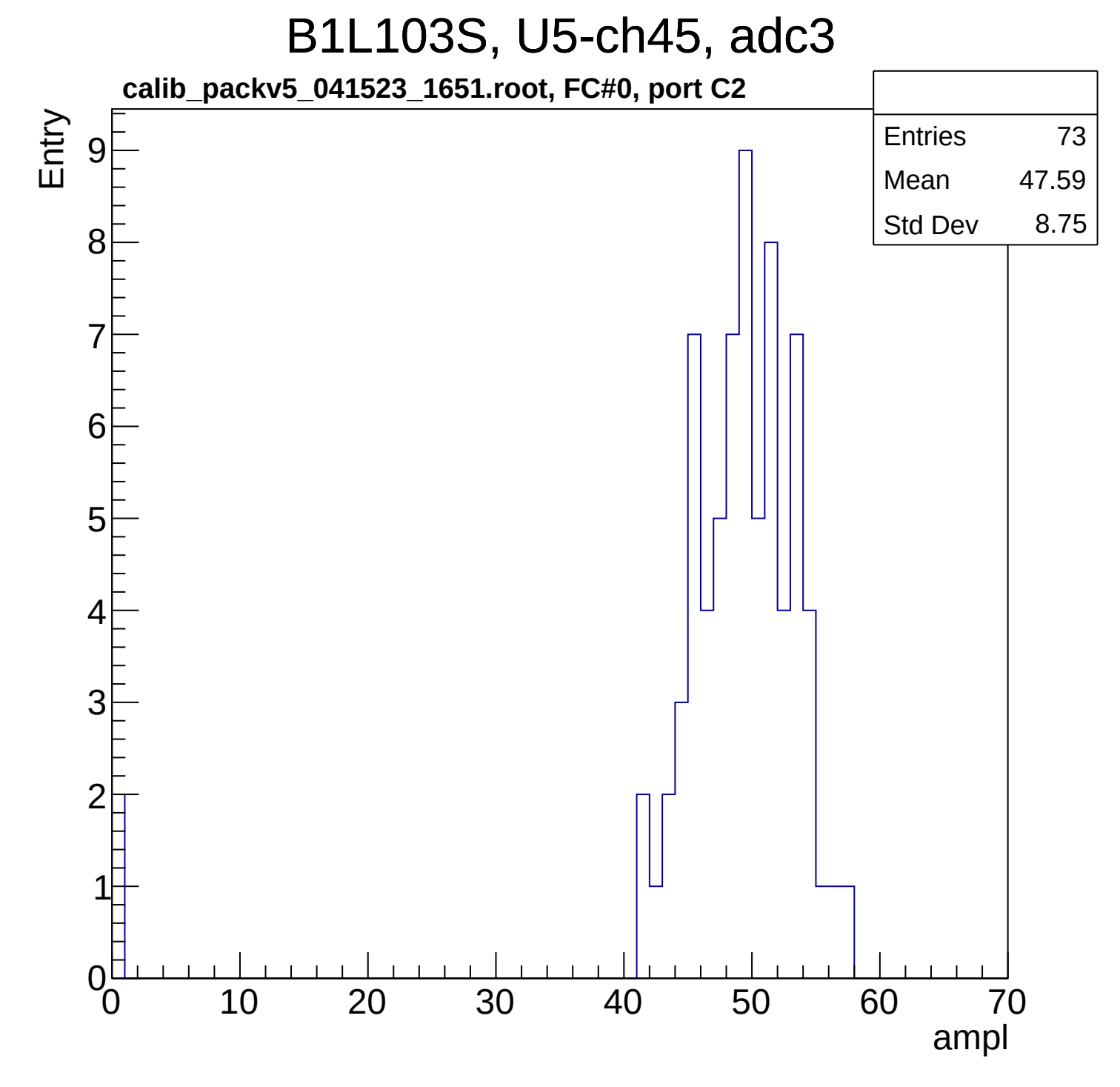
B1L103S, U5-ch45, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 47.59
Std Dev 8.75
Entry
ampl
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2
3
4
5
6
7
8
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0
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20
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60
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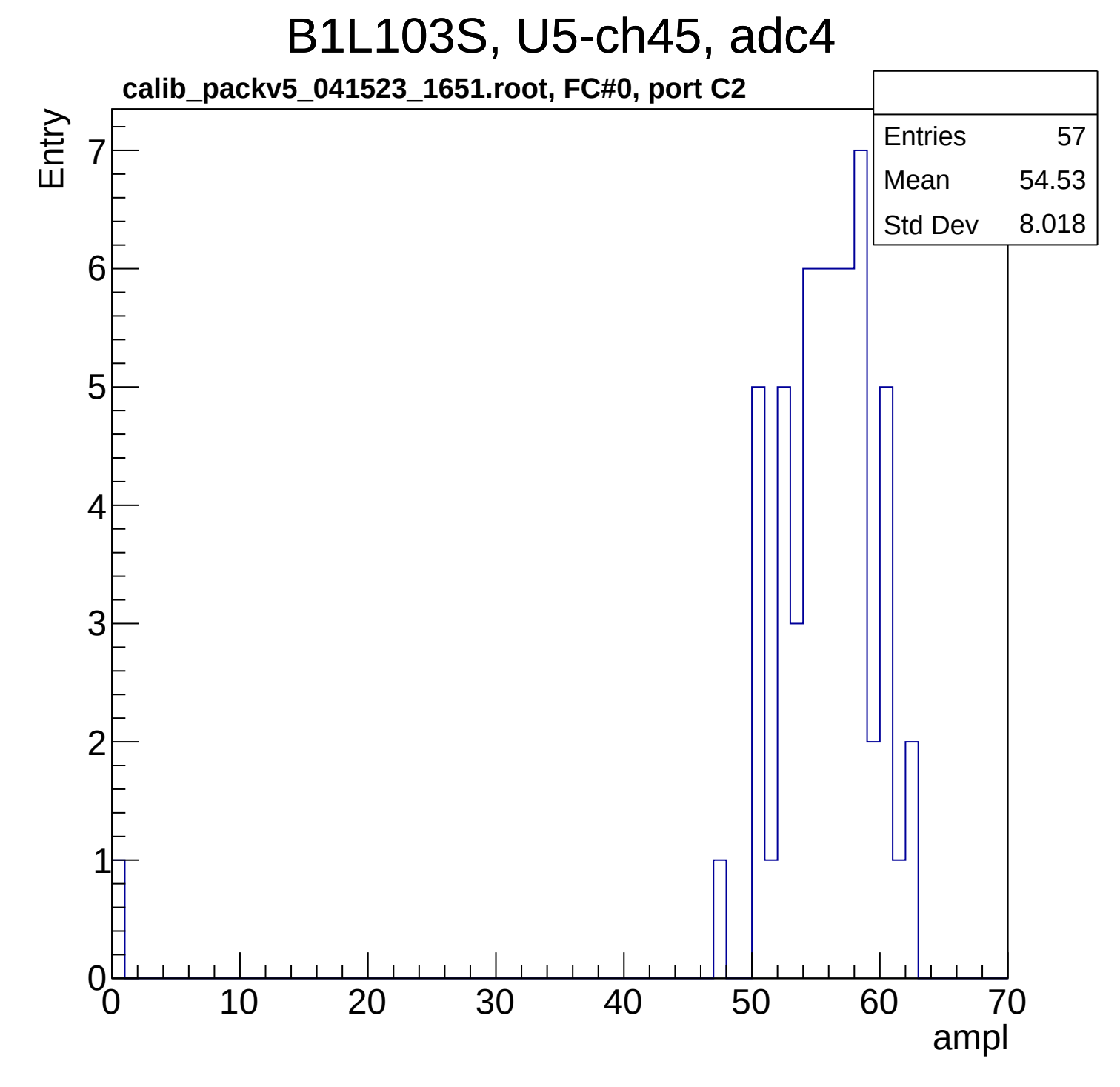
B1L103S, U5-ch45, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 54.53
Std Dev 8.018
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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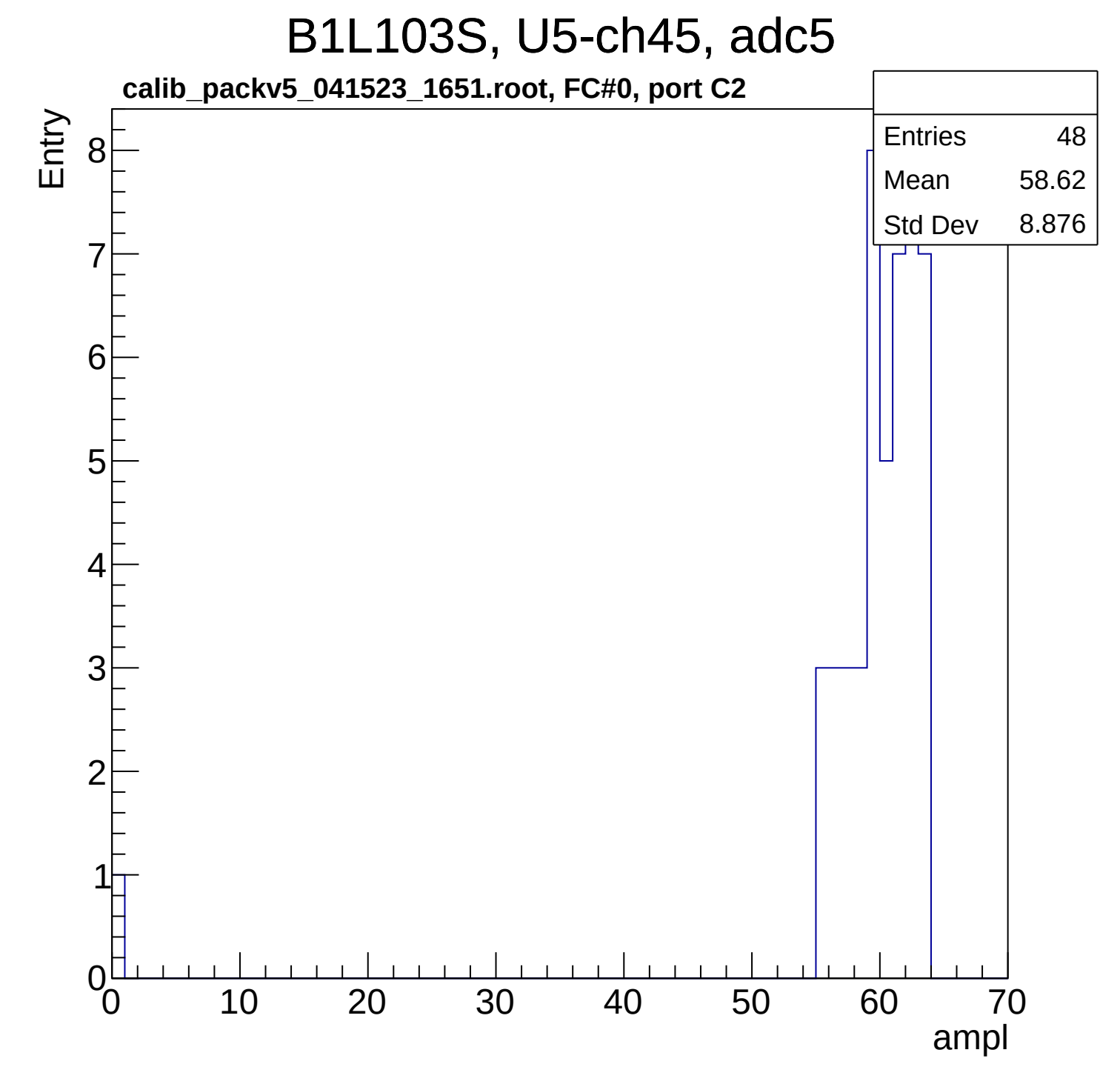
B1L103S, U5-ch45, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.62
Std Dev 8.876
Entry
ampl
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3
4
5
6
7
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0
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60
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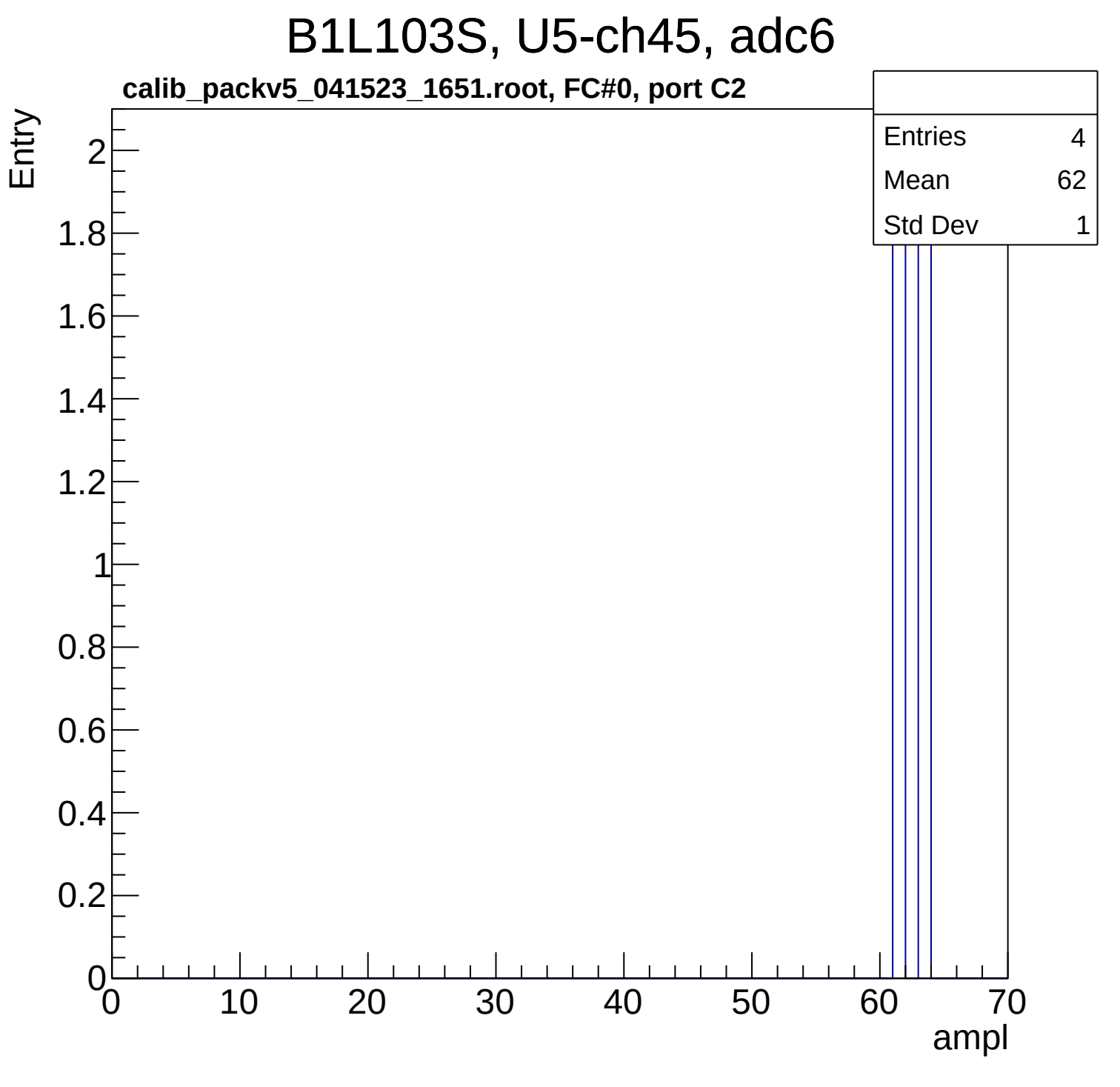
B1L103S, U5-ch45, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62
Std Dev 1
Entry
ampl
0
0.2
0.4
0.6
0.8
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1.2
1.4
1.6
1.8
2
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10
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40
50
60
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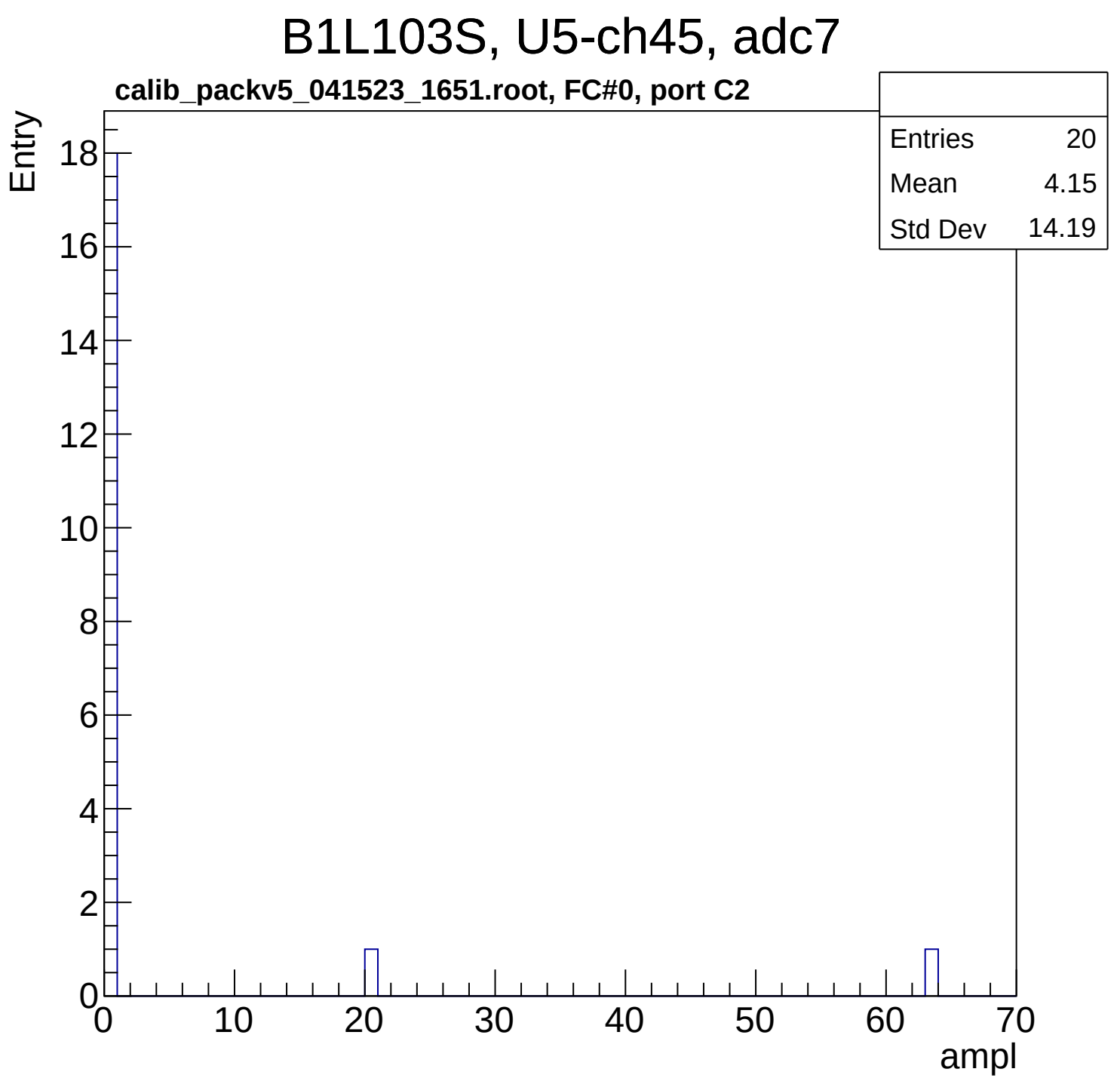
B1L103S, U5-ch45, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.15
Std Dev 14.19
Entry
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2
4
6
8
10
12
14
16
18
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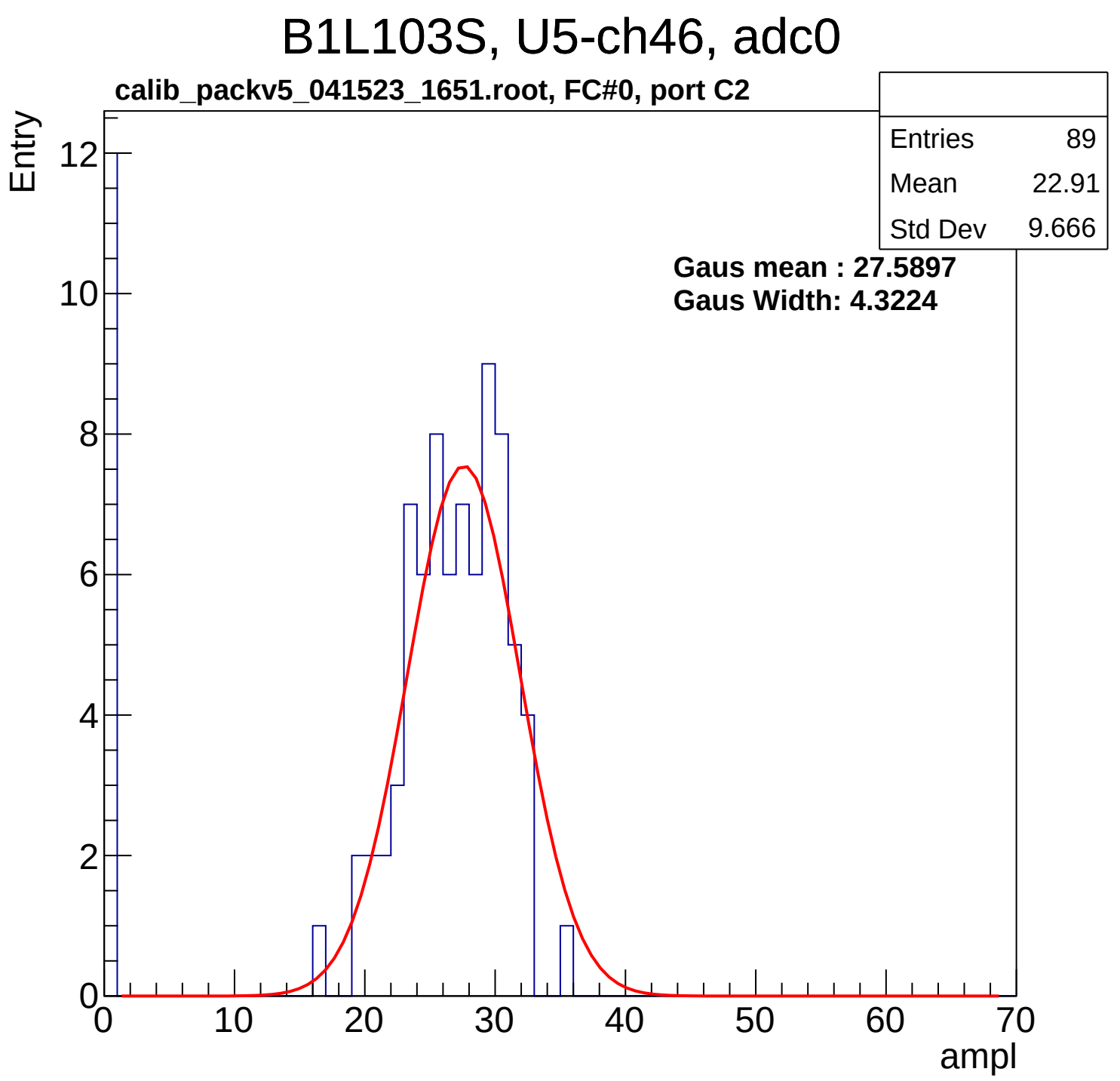
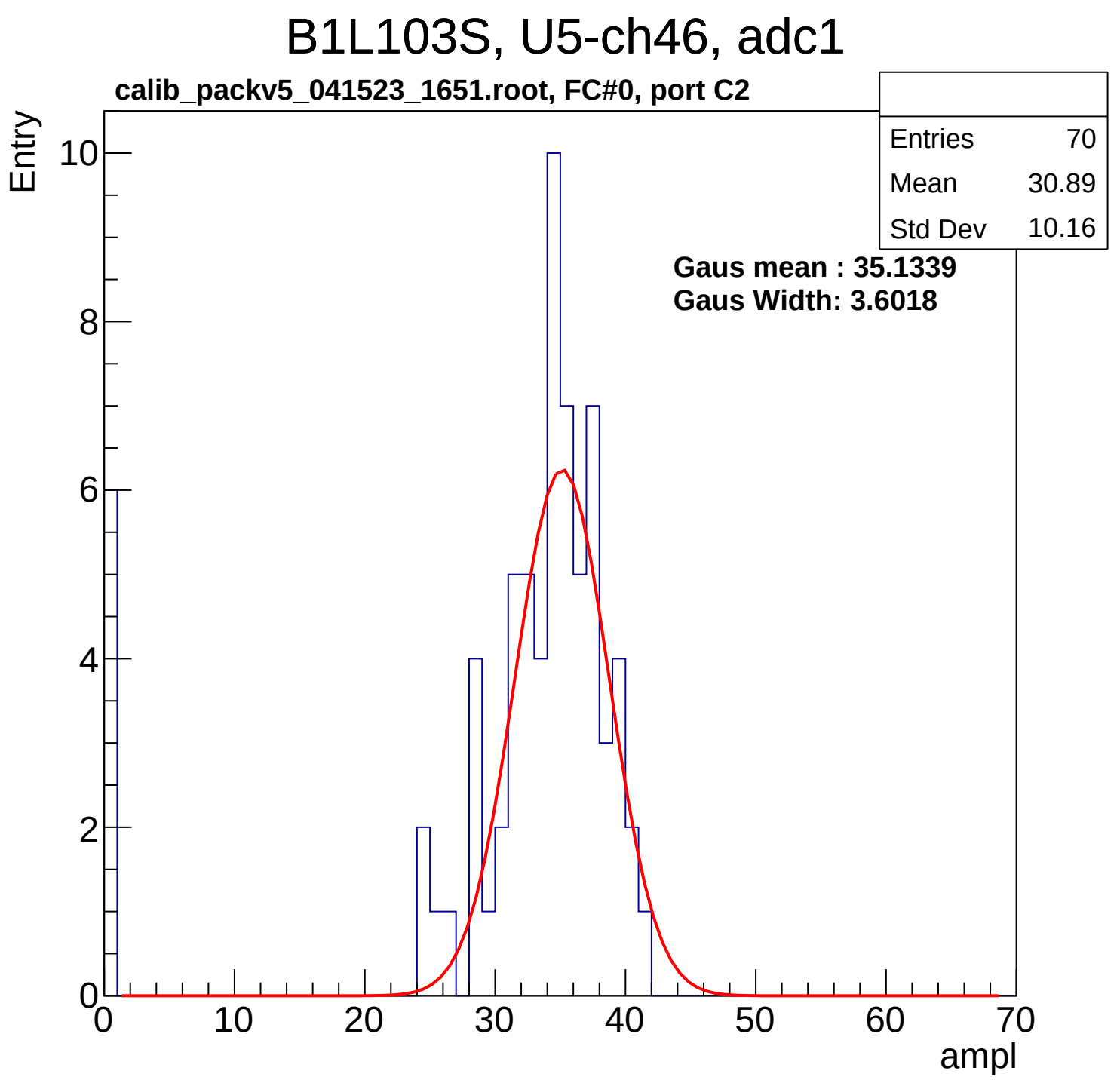
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch46, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 22.91
Std Dev 9.666
Gaus mean : 27.5897
Gaus Width: 4.3224
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U5-ch46, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 30.89
Std Dev 10.16
Gaus mean : 35.1339
Gaus Width: 3.6018
Entry
ampl
0
2
4
6
8
10
0
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20
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40
50
60
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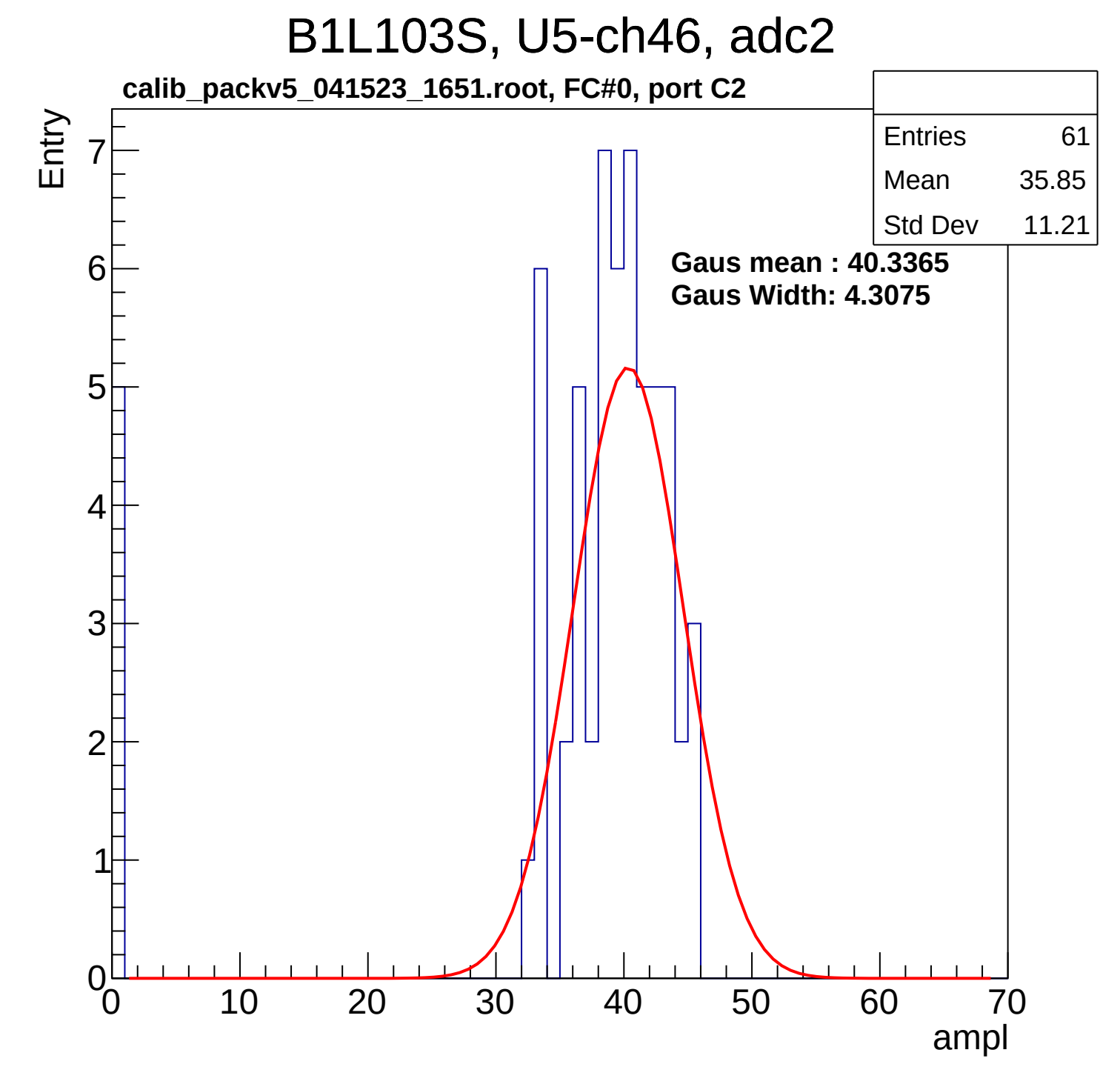
B1L103S, U5-ch46, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 35.85
Std Dev 11.21
Gaus mean : 40.3365
Gaus Width: 4.3075
Entry
ampl
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1
2
3
4
5
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0
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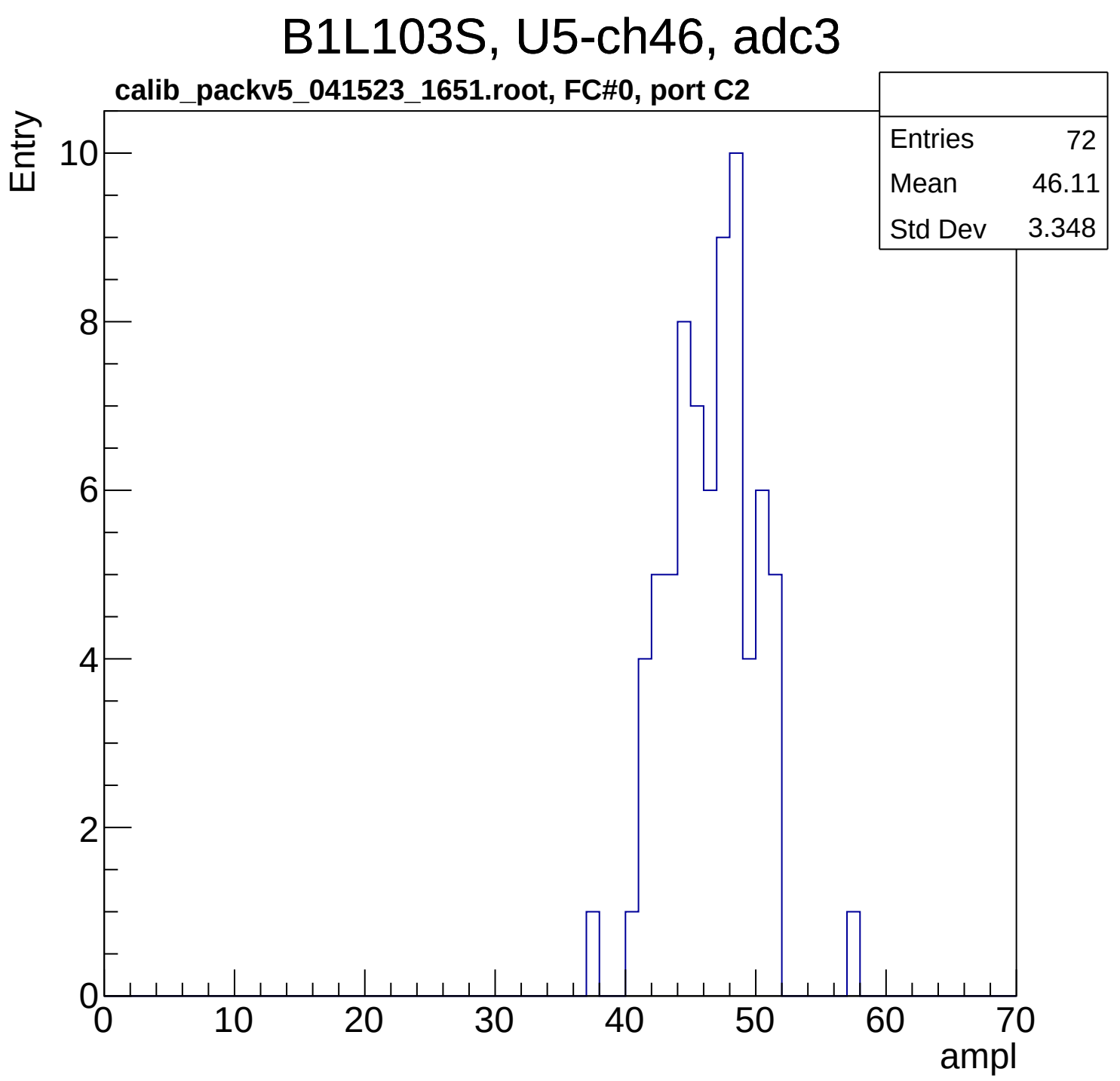
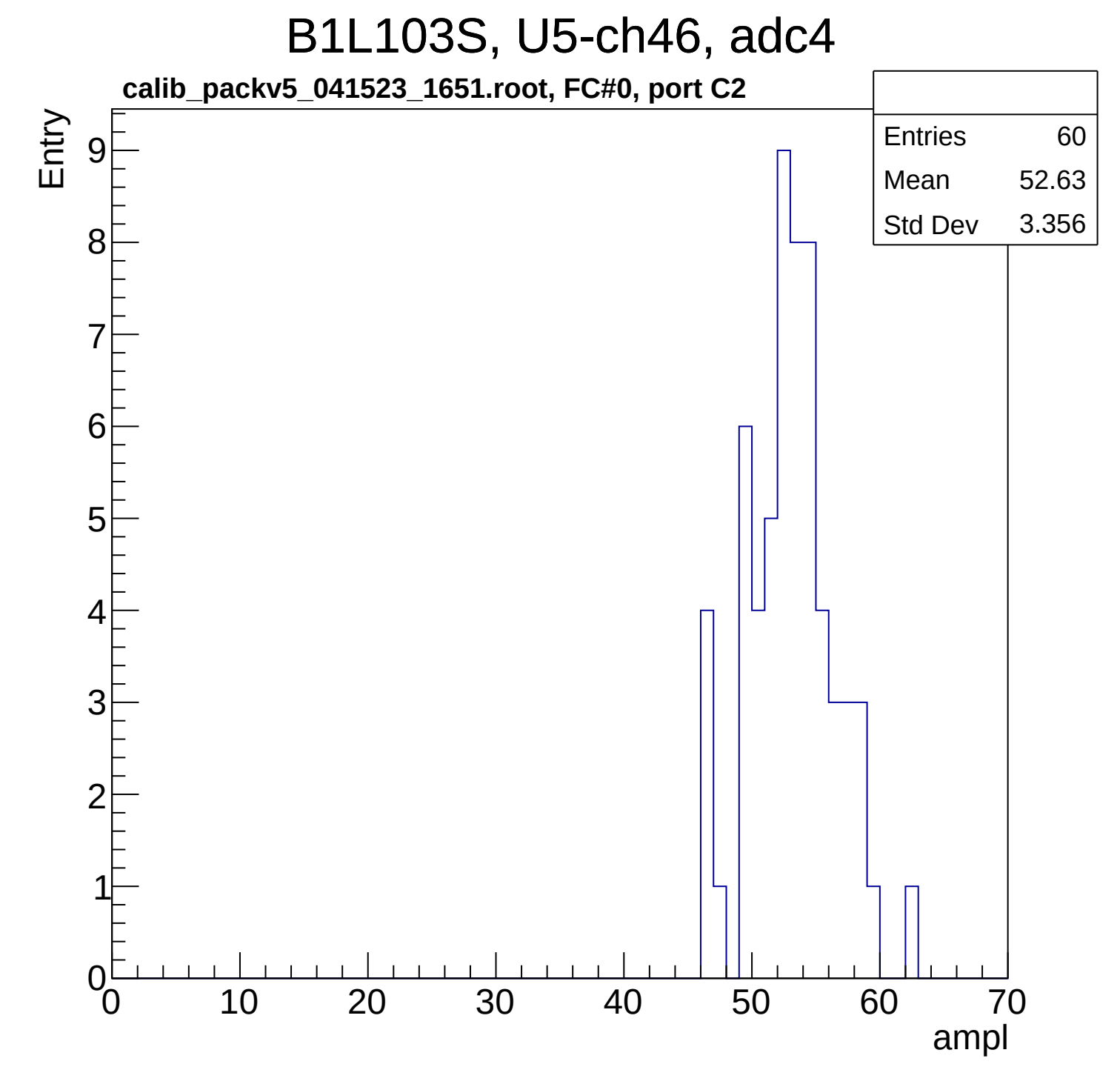

B1L103S, U5-ch46, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 46.11
Std Dev 3.348
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U5-ch46, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 52.63
Std Dev 3.356
Entry
ampl
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2
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6
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0
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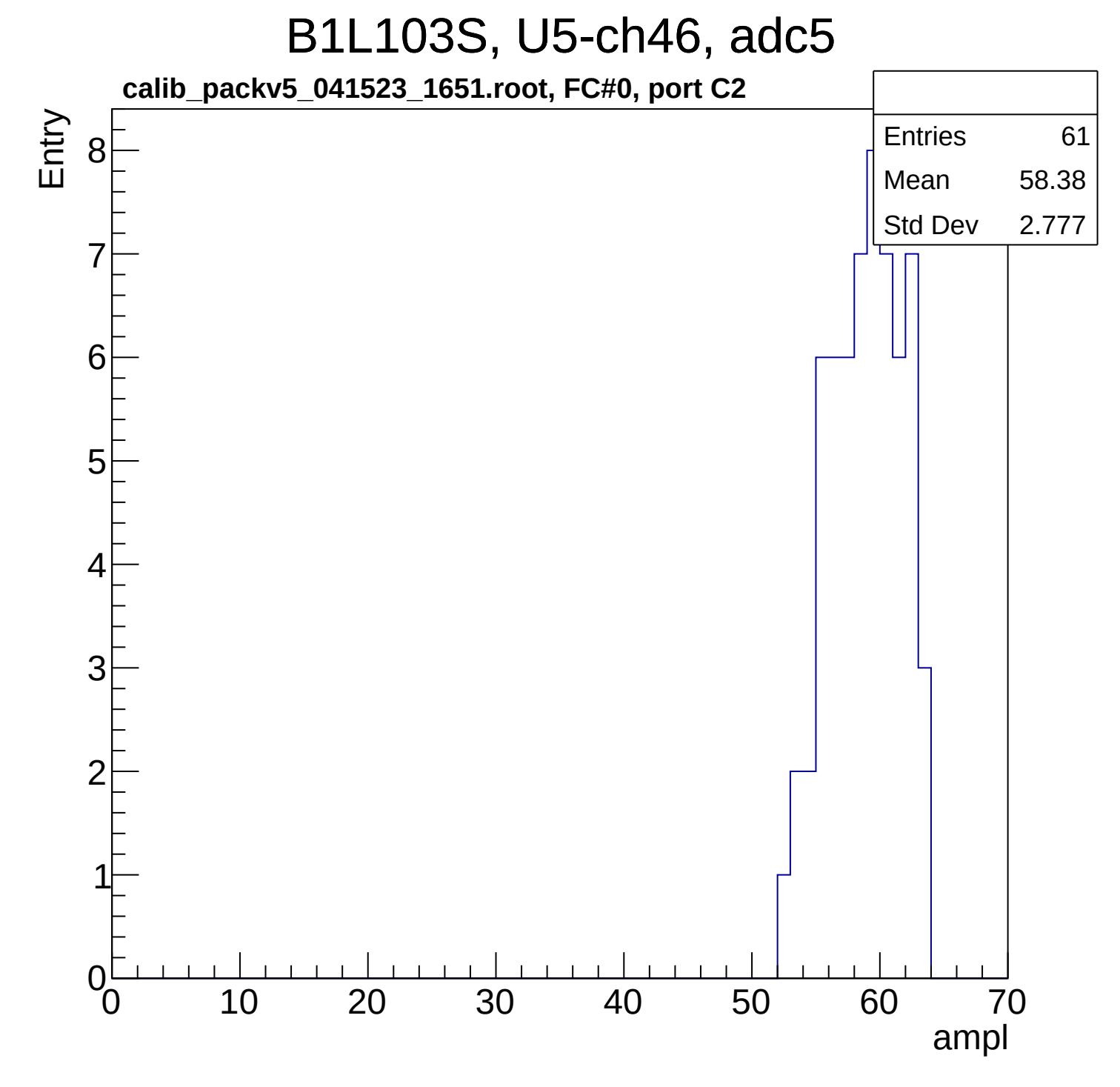
B1L103S, U5-ch46, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 58.38
Std Dev 2.777
Entry
ampl
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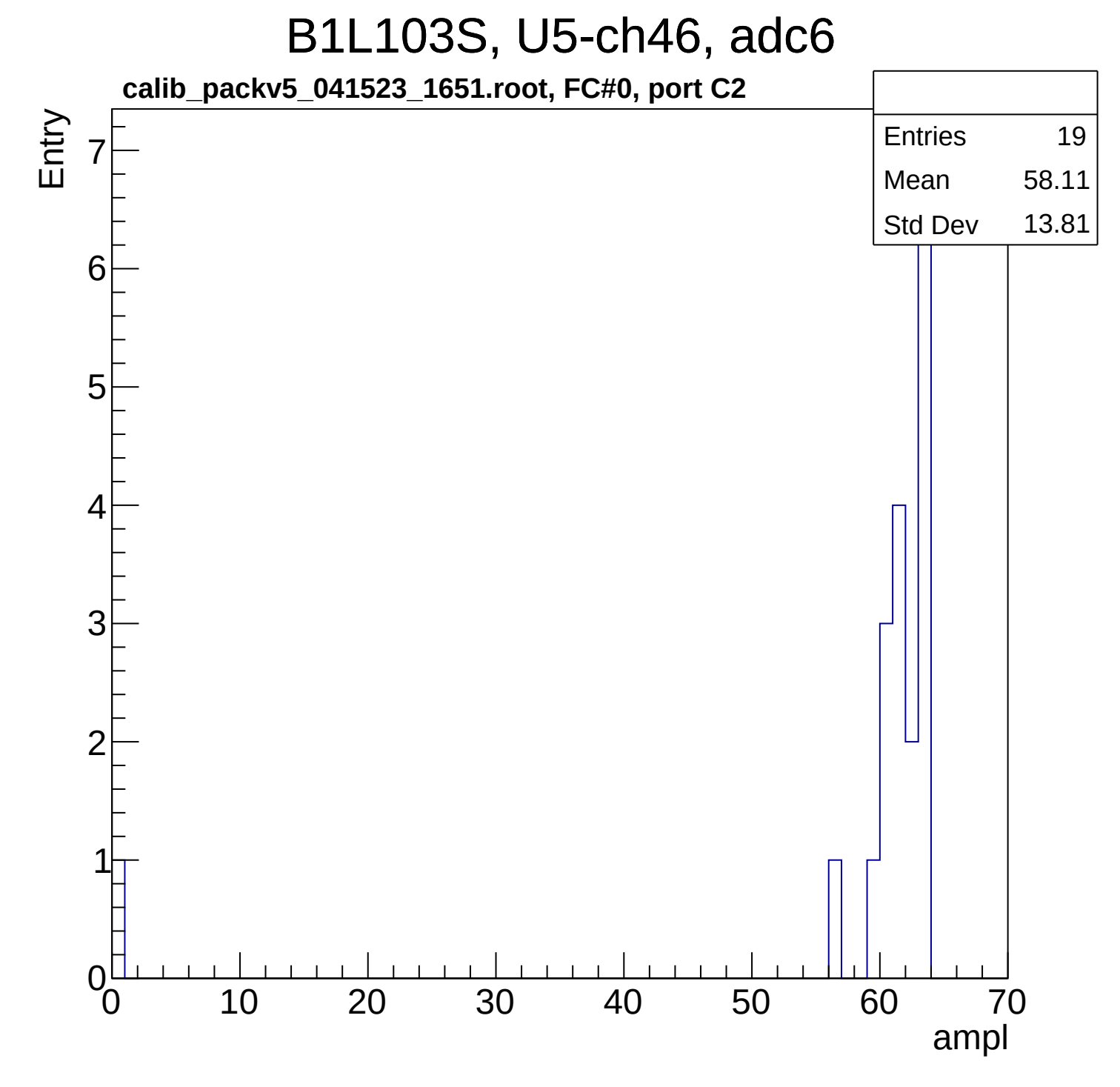
B1L103S, U5-ch46, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 58.11
Std Dev 13.81
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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40
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60
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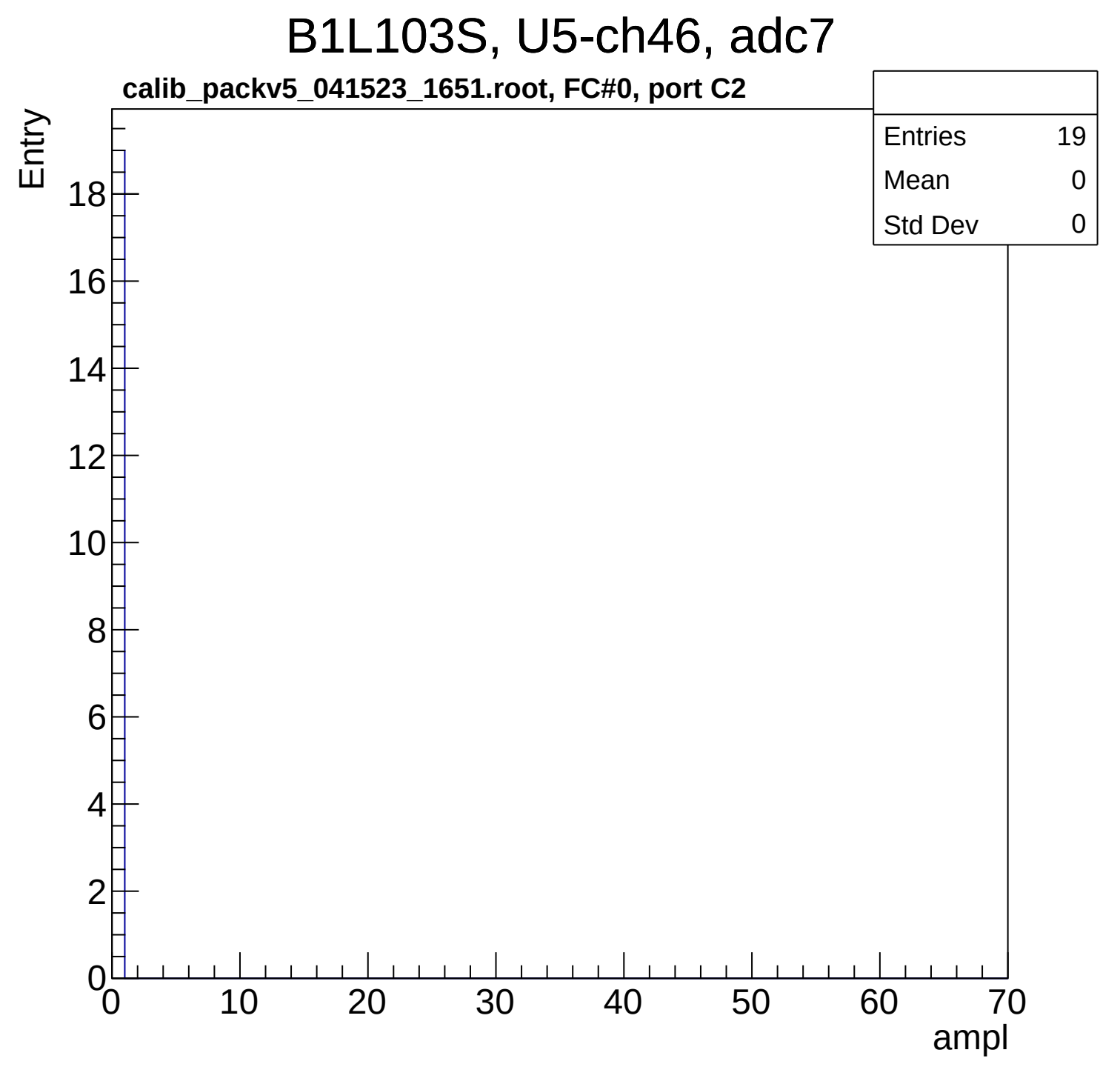
B1L103S, U5-ch46, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
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10
20
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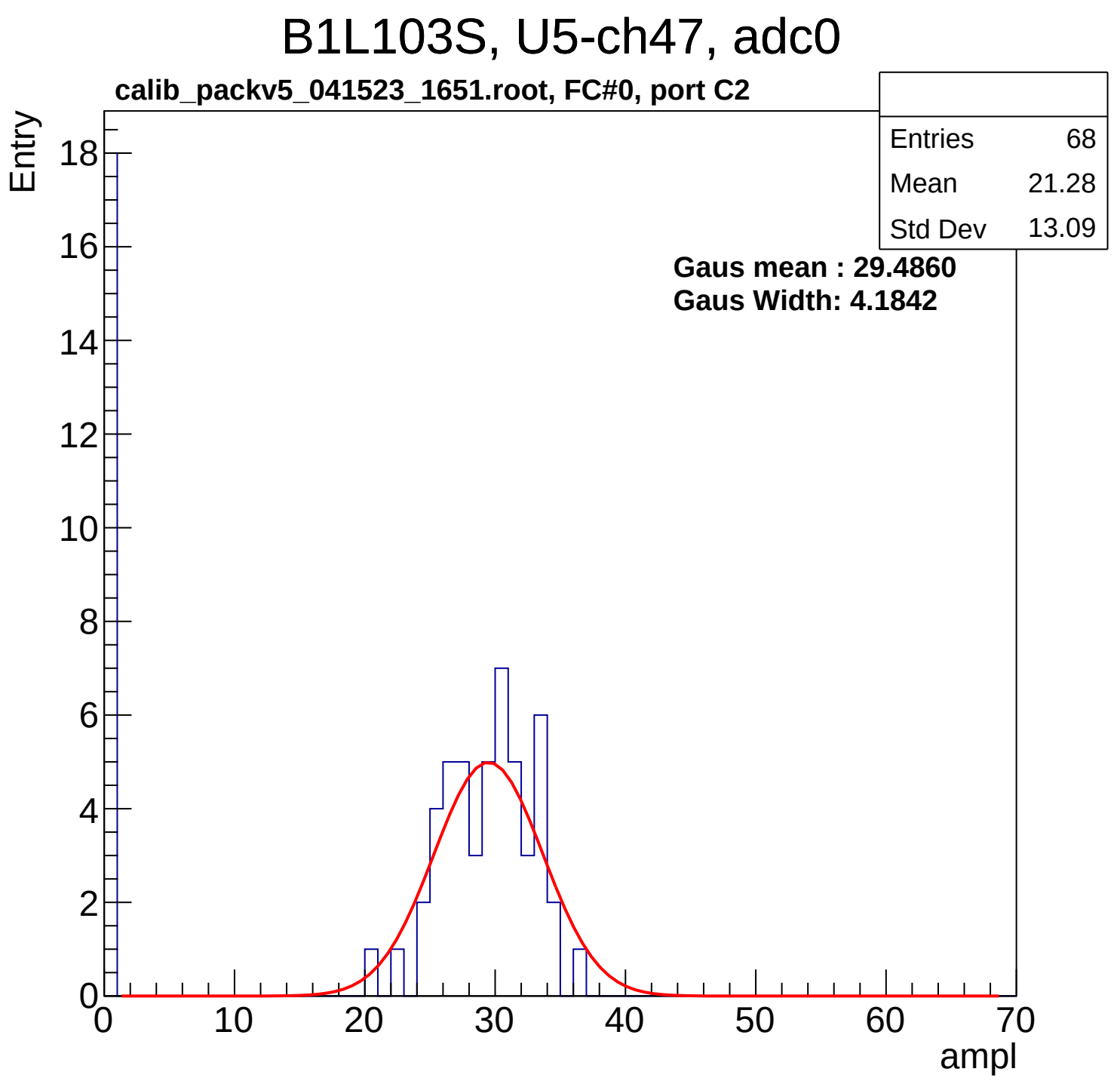
50
60
70
ampl


B1L103S, U5-ch47, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 21.28
Std Dev 13.09
Gaus mean : 29.4860
Gaus Width: 4.1842
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
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60
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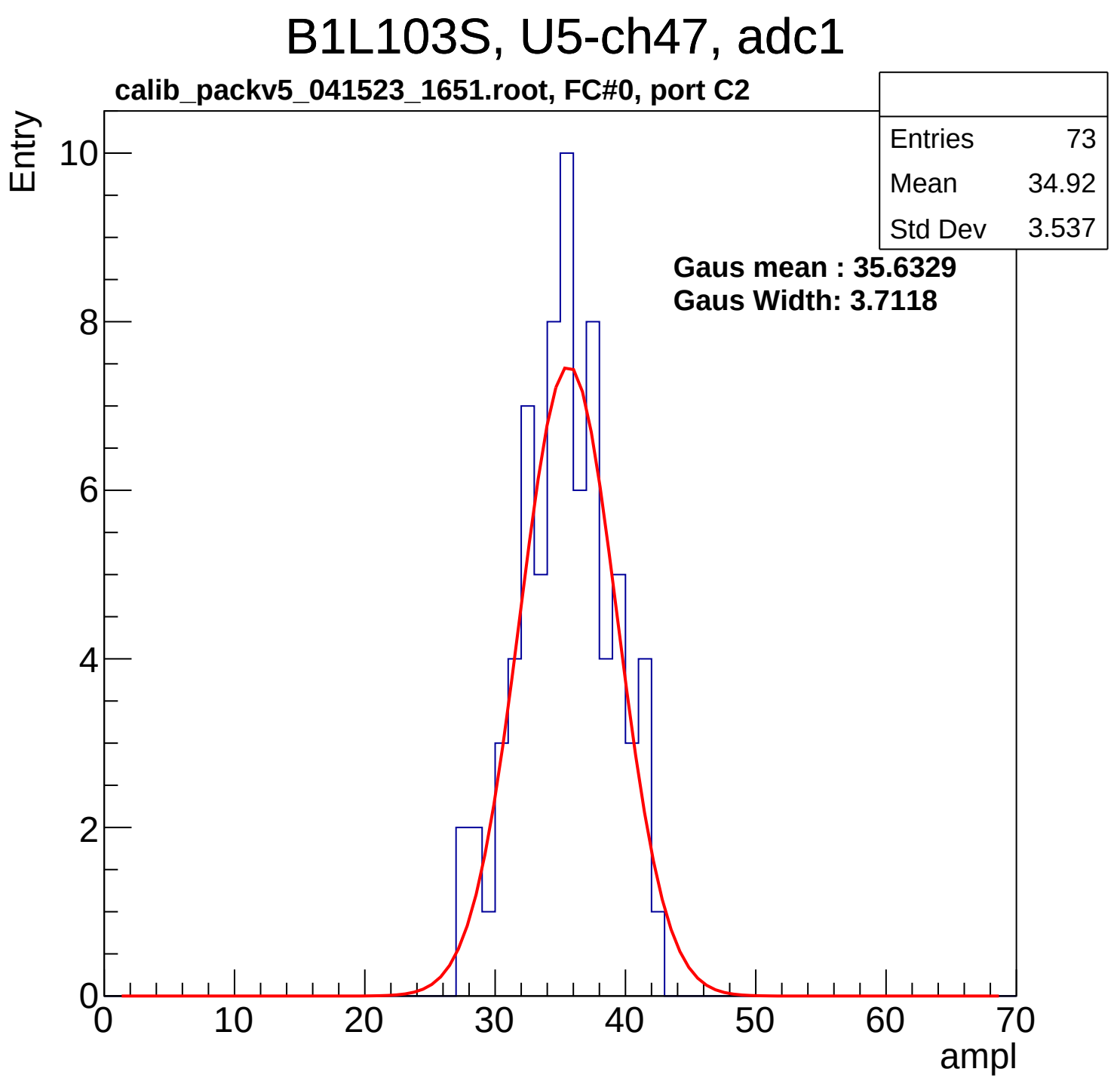
B1L103S, U5-ch47, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 34.92
Std Dev 3.537
Gaus mean : 35.6329
Gaus Width: 3.7118
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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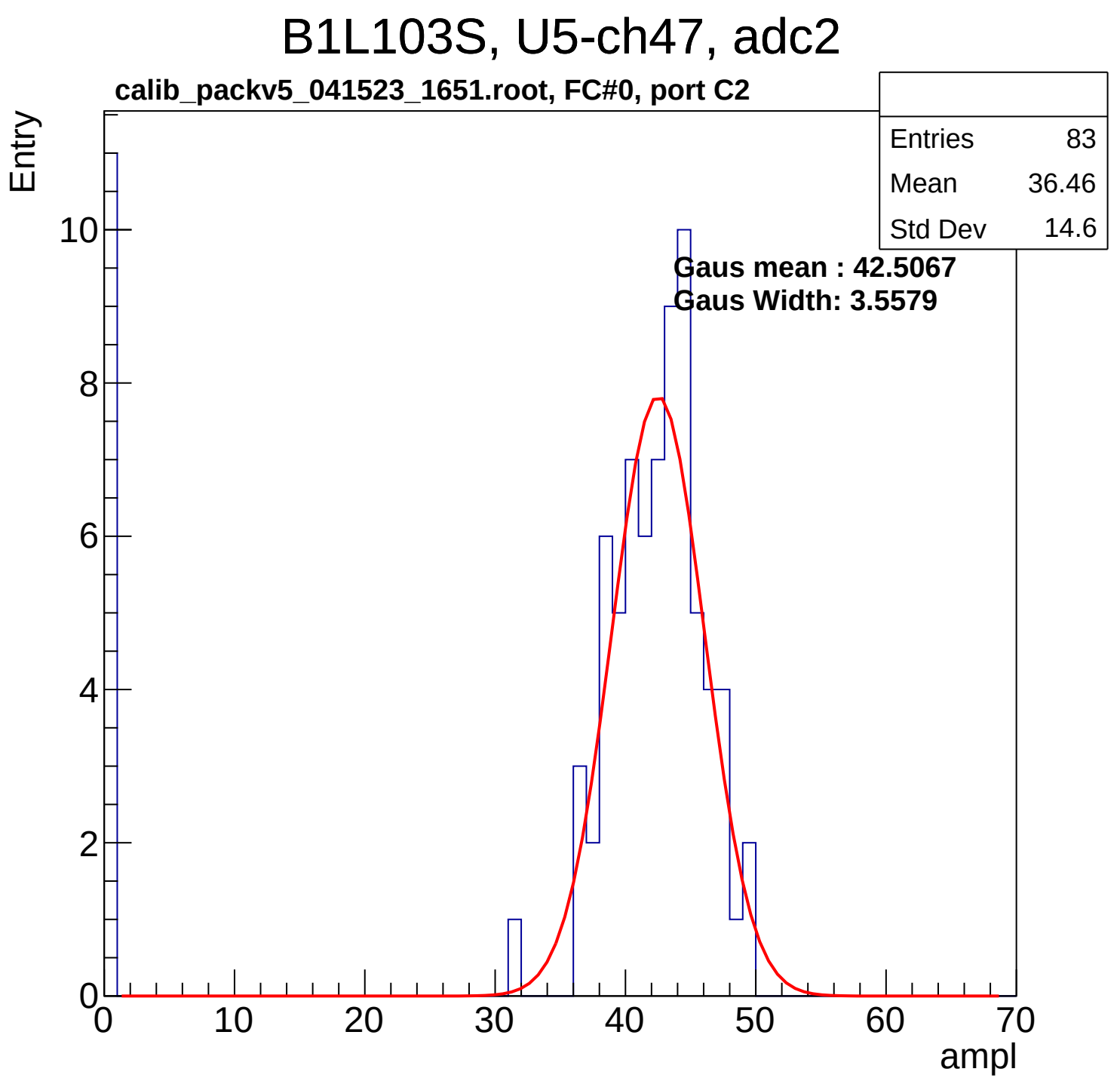
B1L103S, U5-ch47, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 36.46
Std Dev 14.6
Gaus mean : 42.5067
Gaus Width: 3.5579
Entry
ampl
0
2
4
6
8
10
0
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20
30
40
50
60
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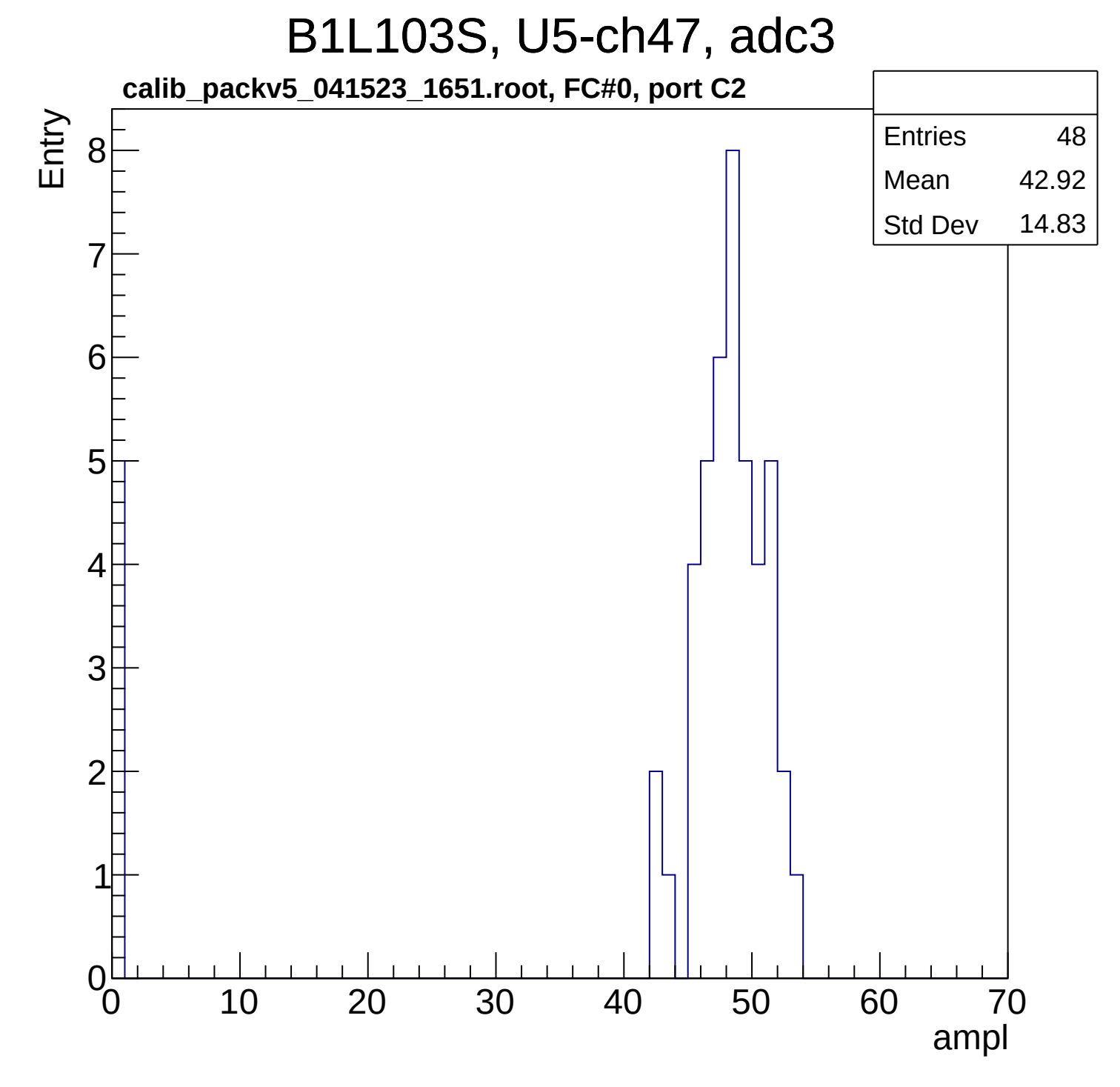
B1L103S, U5-ch47, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 42.92
Std Dev 14.83
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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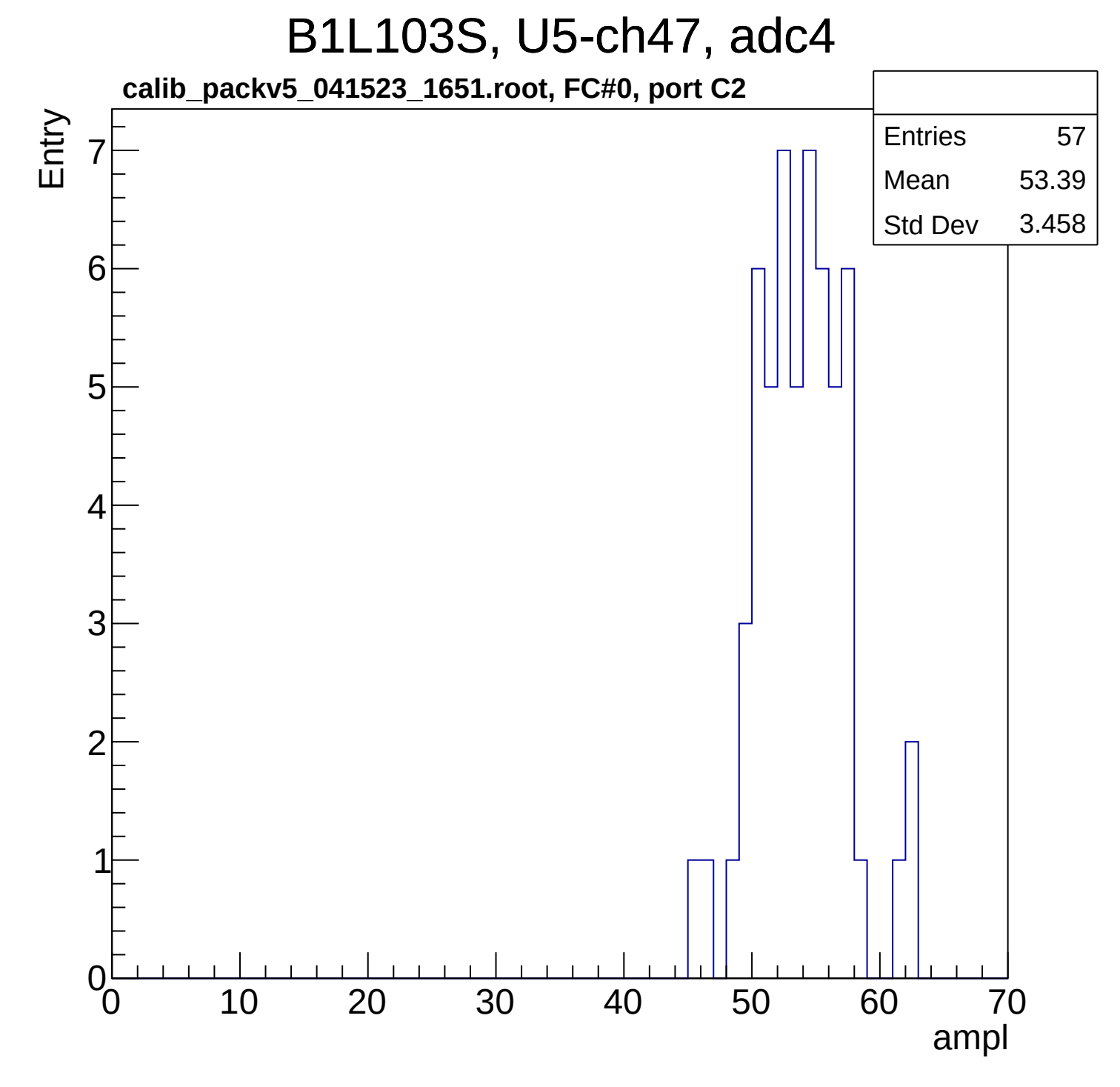
B1L103S, U5-ch47, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 53.39
Std Dev 3.458
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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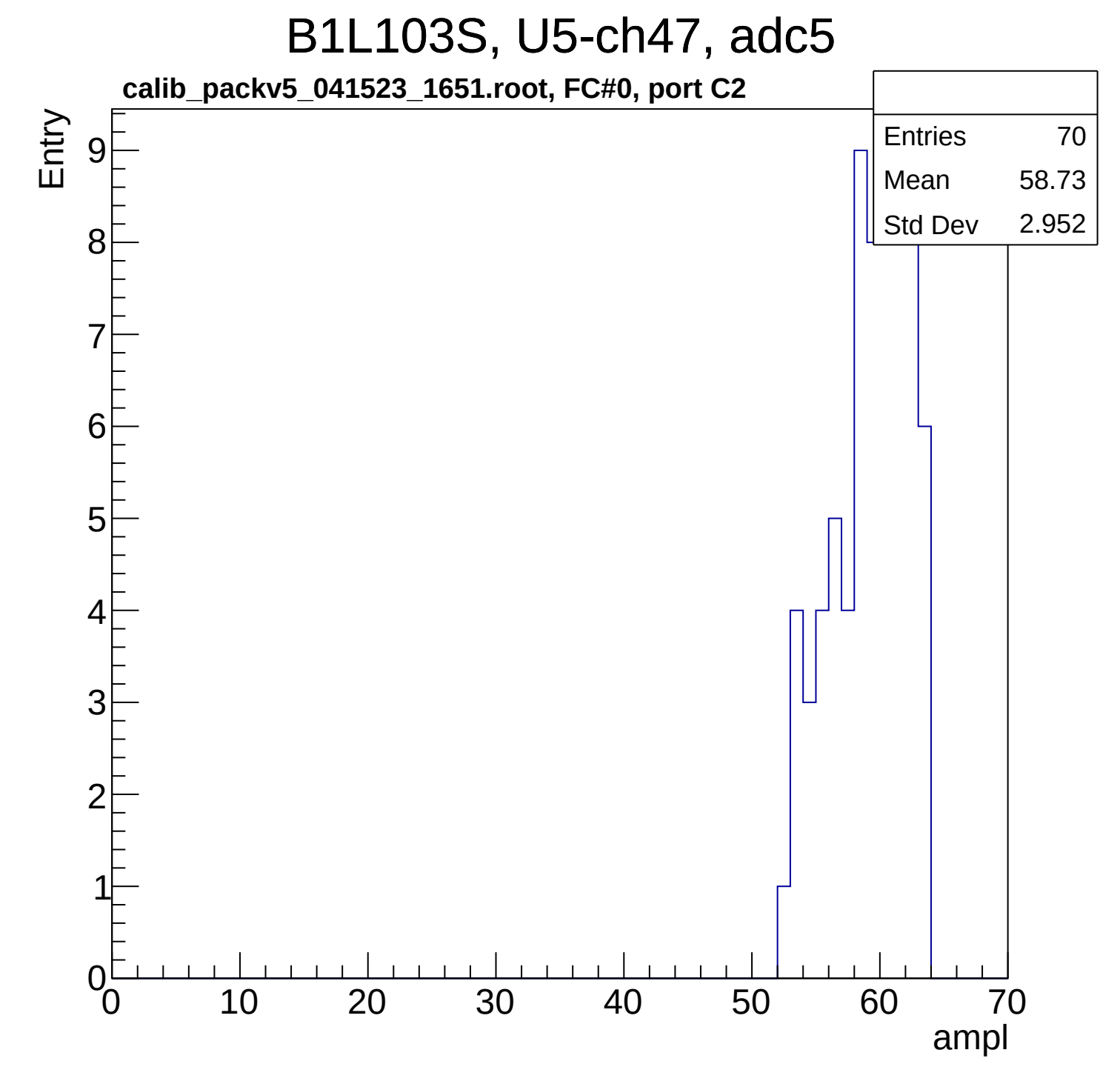
B1L103S, U5-ch47, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 58.73
Std Dev 2.952
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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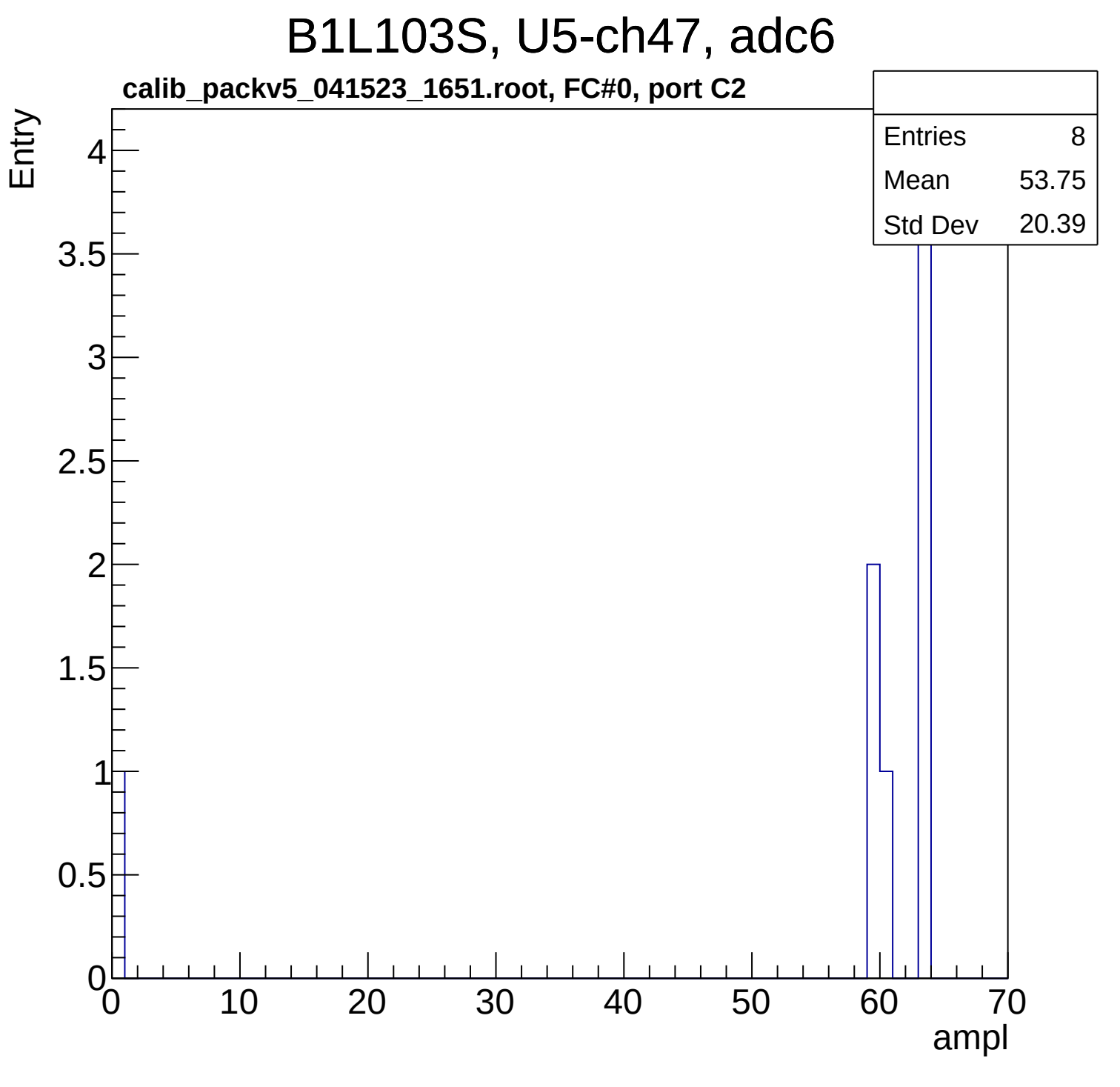
B1L103S, U5-ch47, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 53.75
Std Dev 20.39
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
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20
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40
50
60
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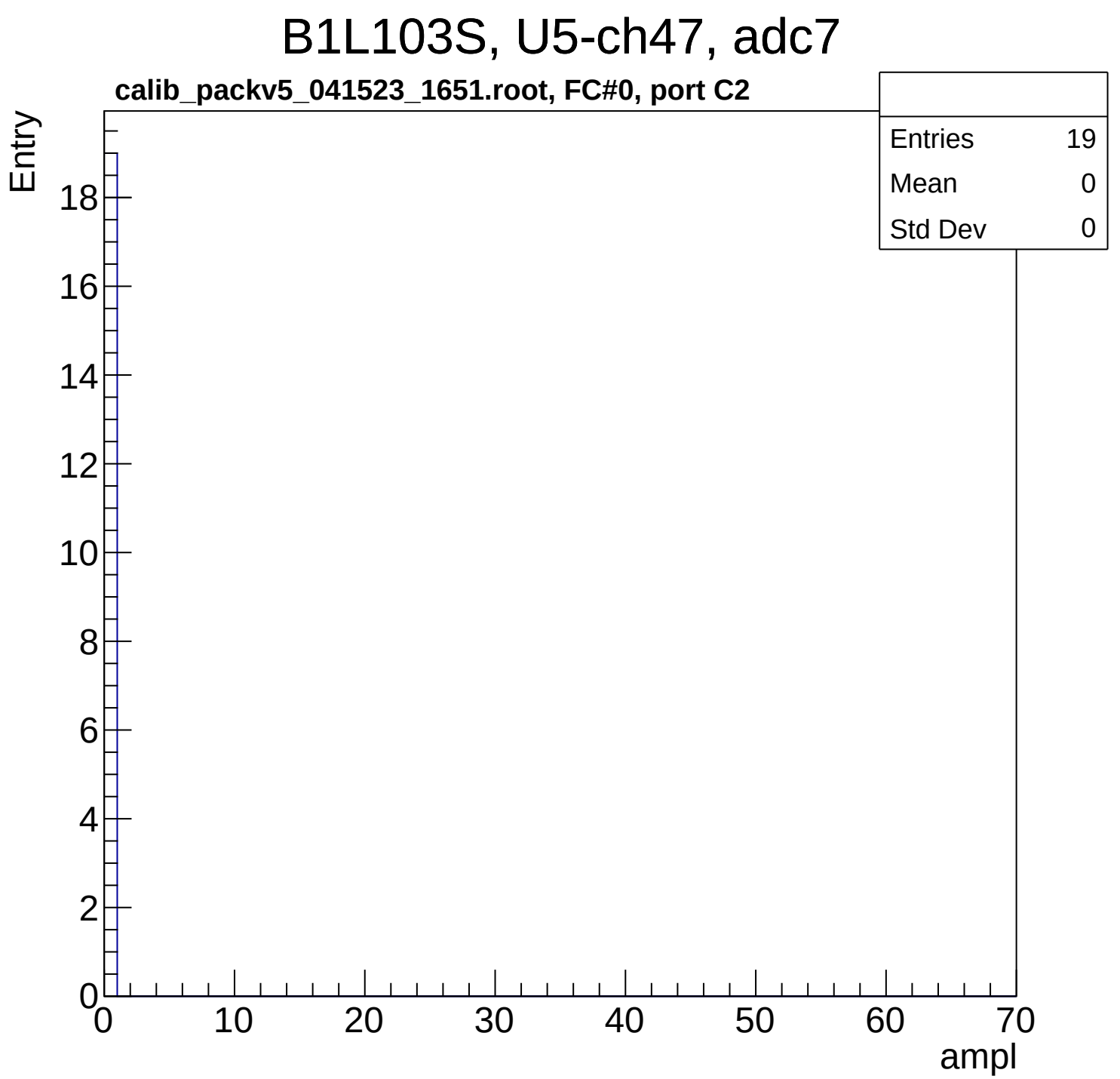
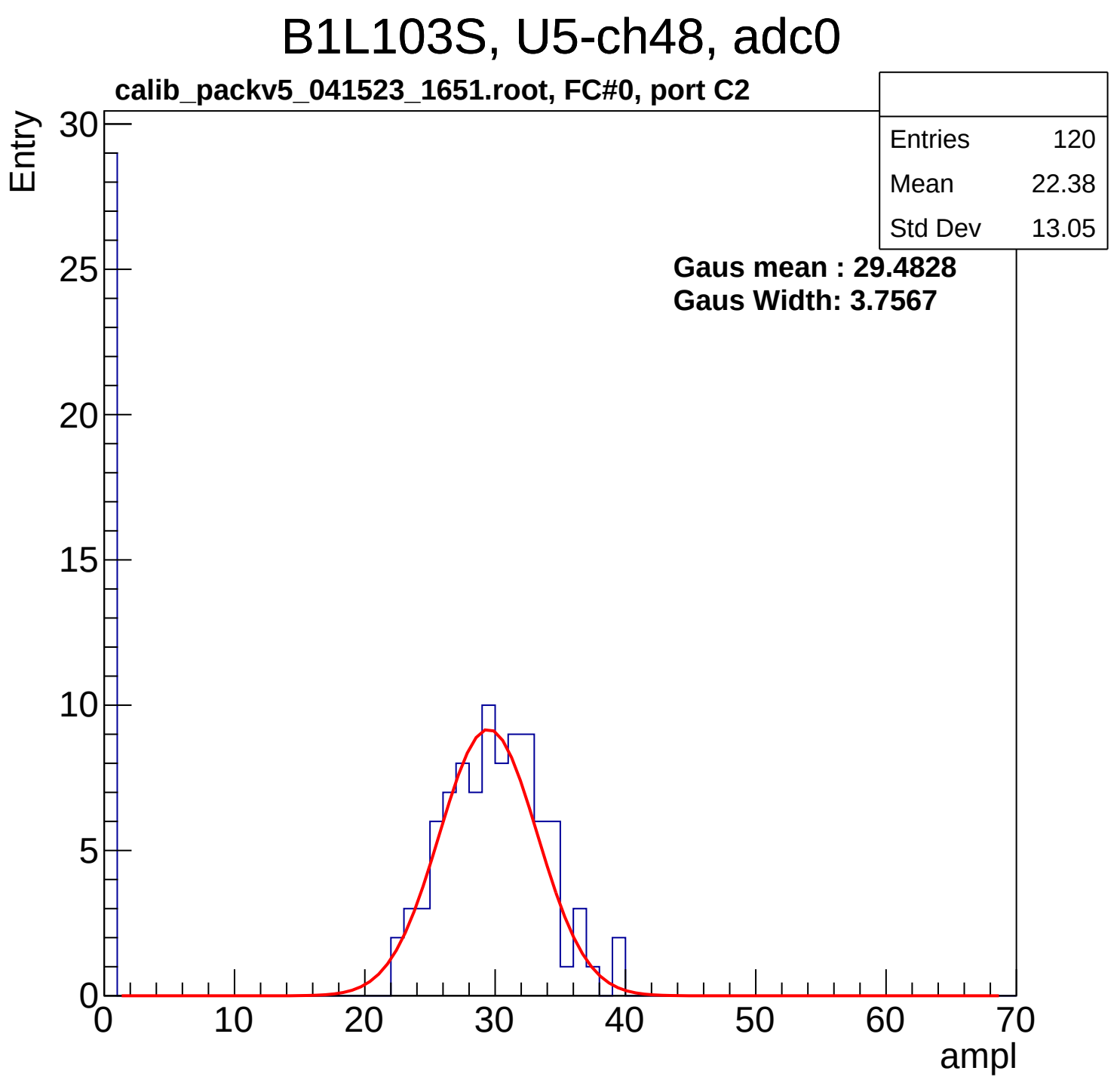
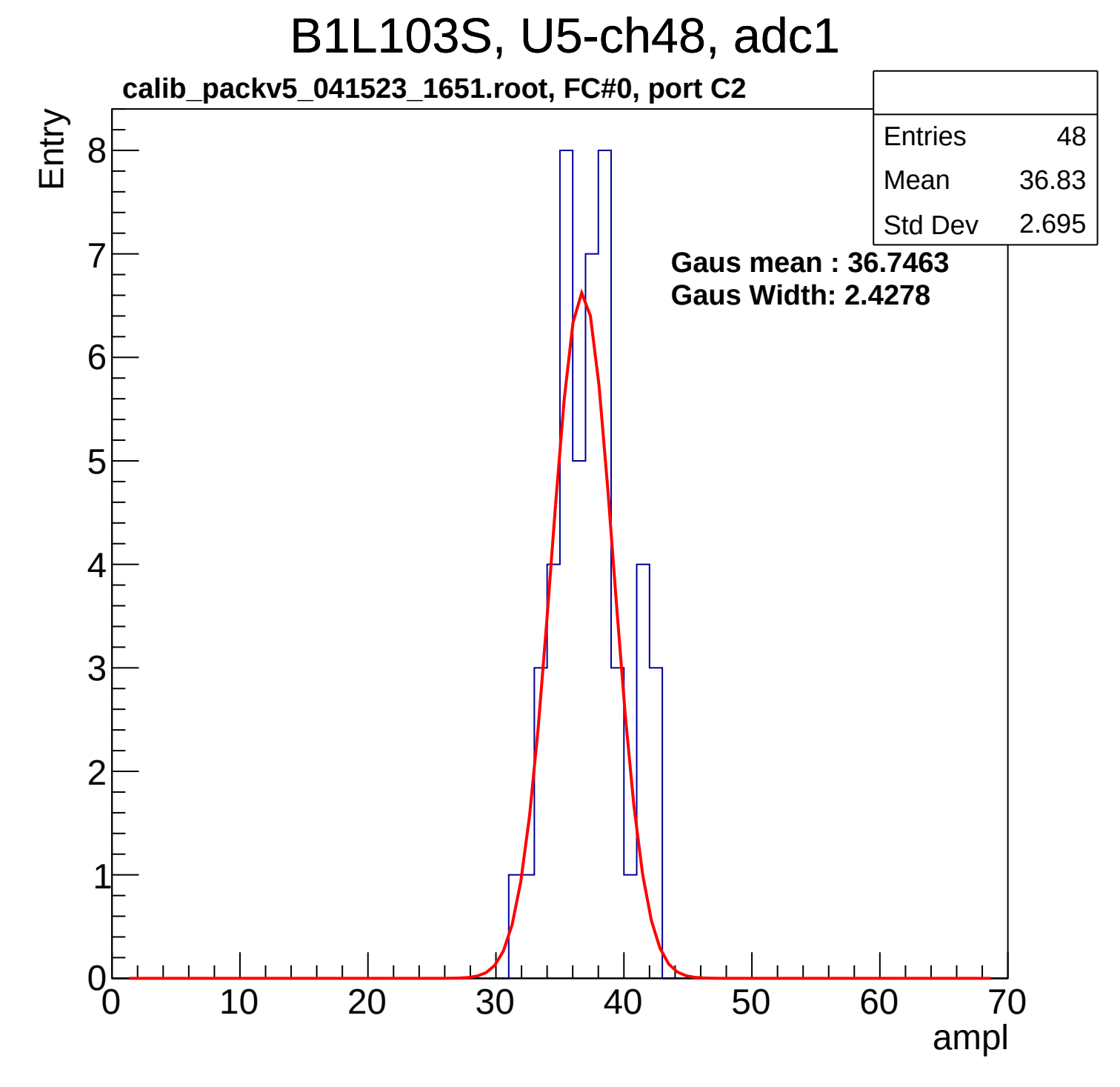

B1L103S, U5-ch47, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch48, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 120
Mean 22.38
Std Dev 13.05
Gaus mean : 29.4828
Gaus Width: 3.7567
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70


B1L103S, U5-ch48, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 36.83
Std Dev 2.695
Gaus mean : 36.7463
Gaus Width: 2.4278
Entry
ampl
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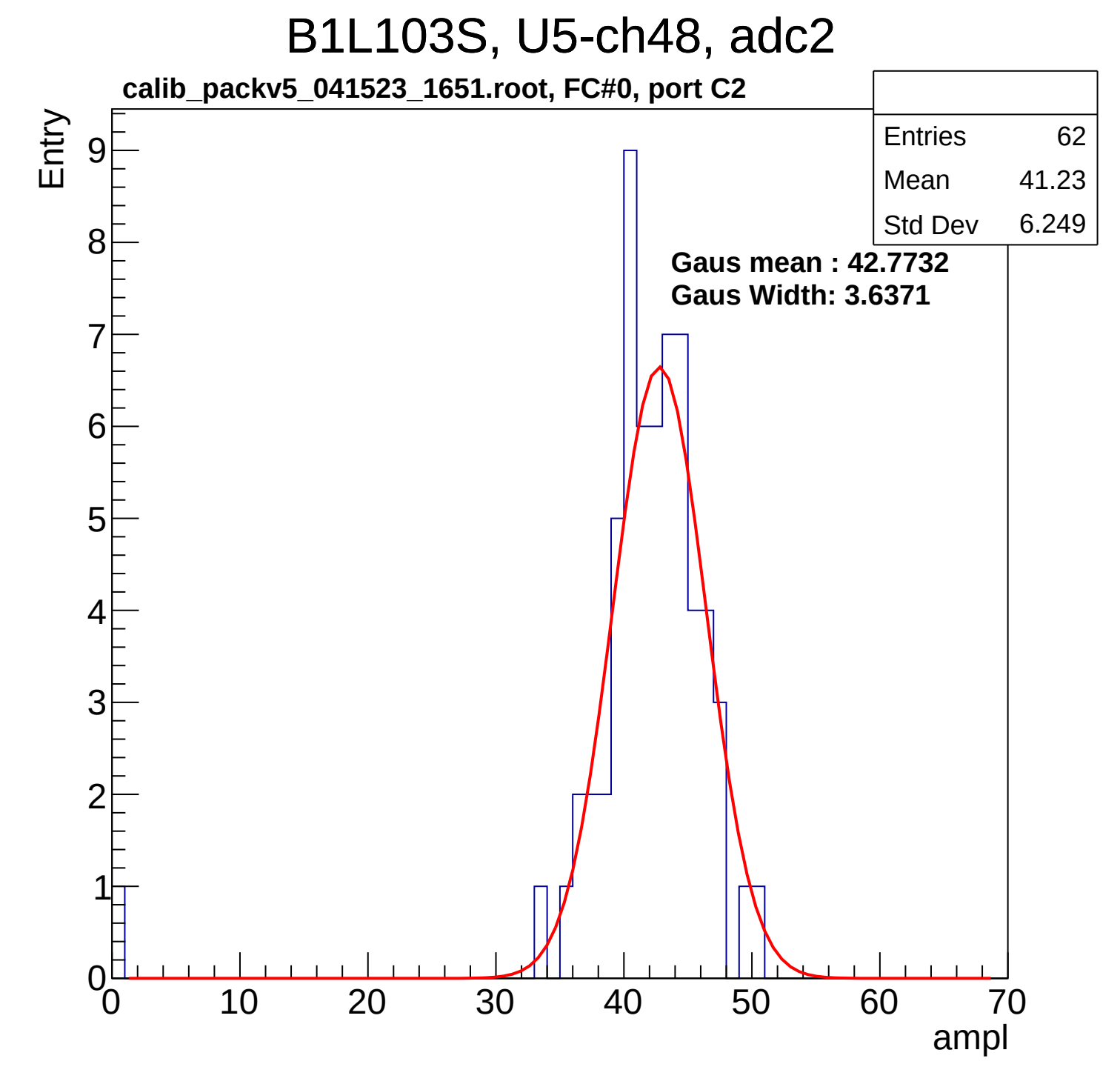
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U5-ch48, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 41.23
Std Dev 6.249
Gaus mean : 42.7732
Gaus Width: 3.6371
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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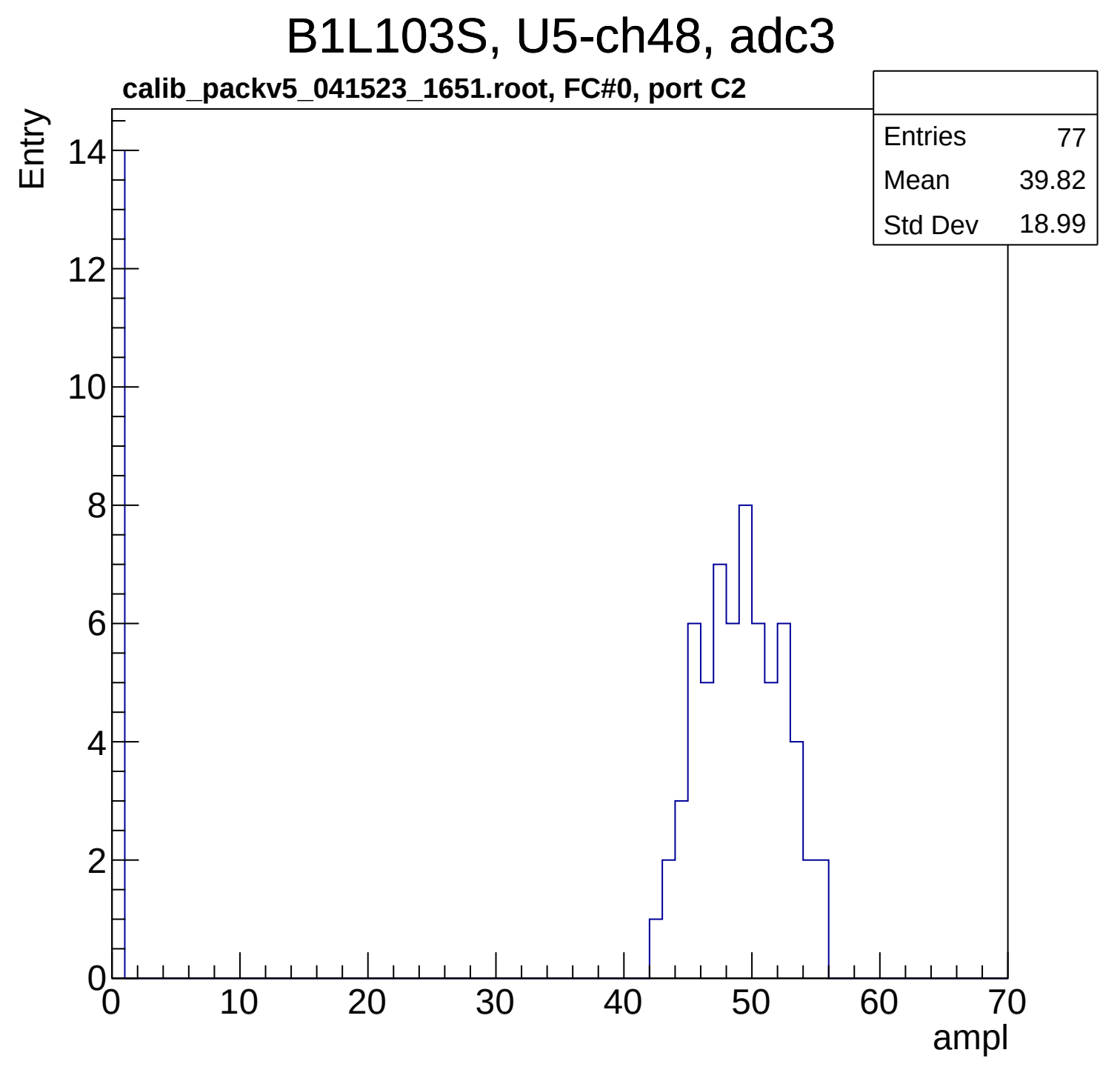
B1L103S, U5-ch48, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 39.82
Std Dev 18.99
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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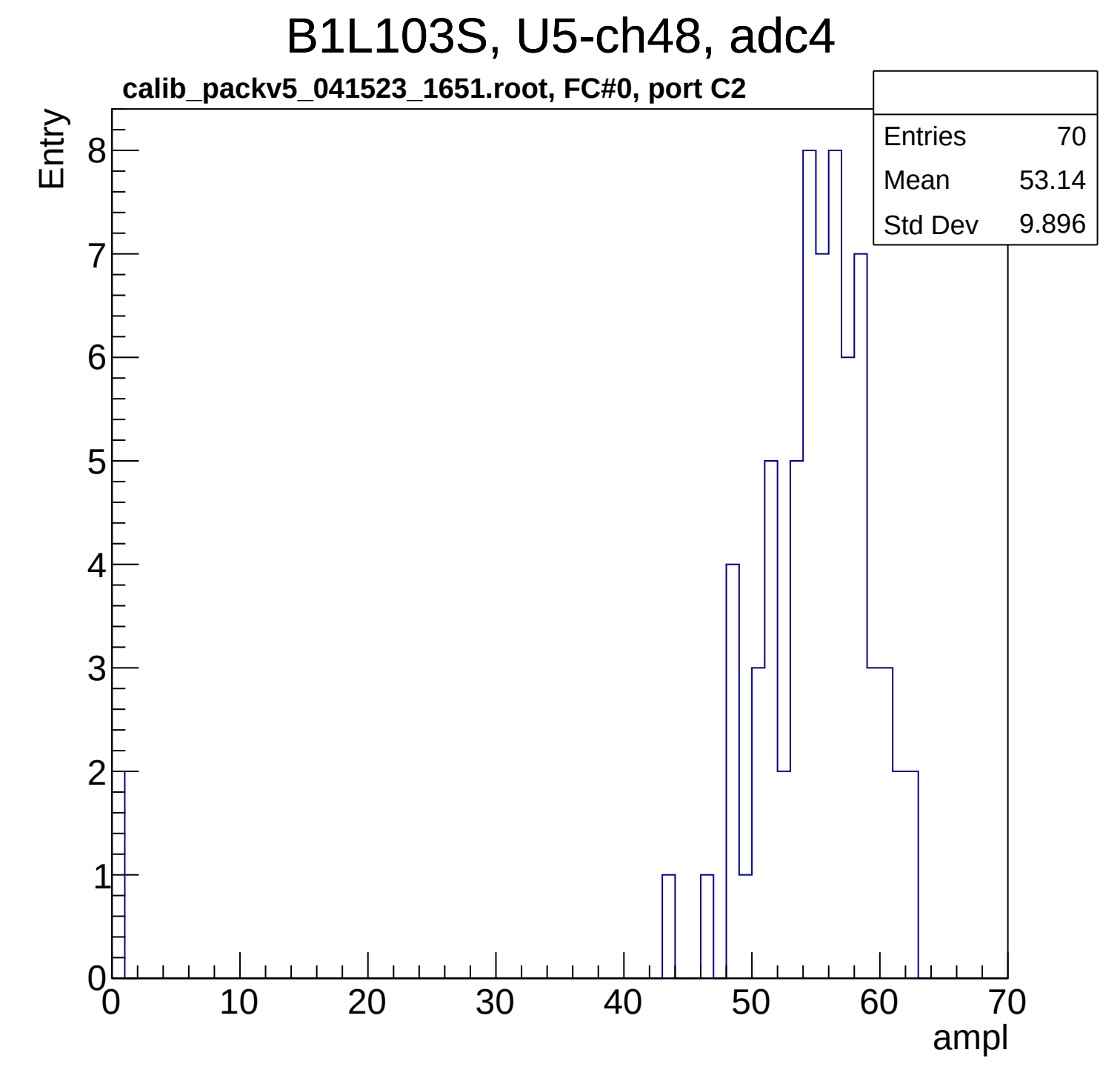
B1L103S, U5-ch48, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 53.14
Std Dev 9.896
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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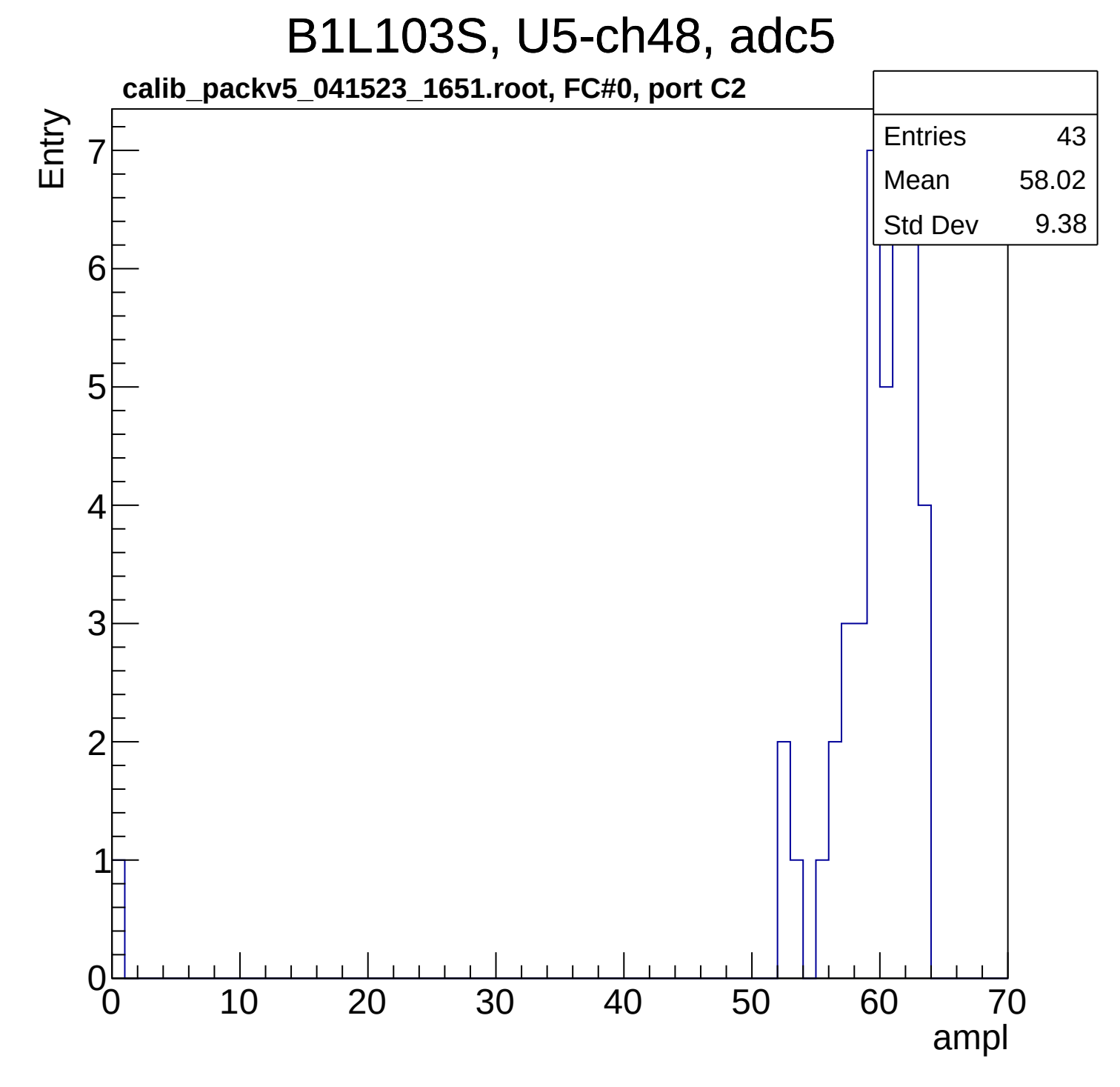
B1L103S, U5-ch48, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 58.02
Std Dev 9.38
Entry
ampl
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3
4
5
6
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0
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20
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40
50
60
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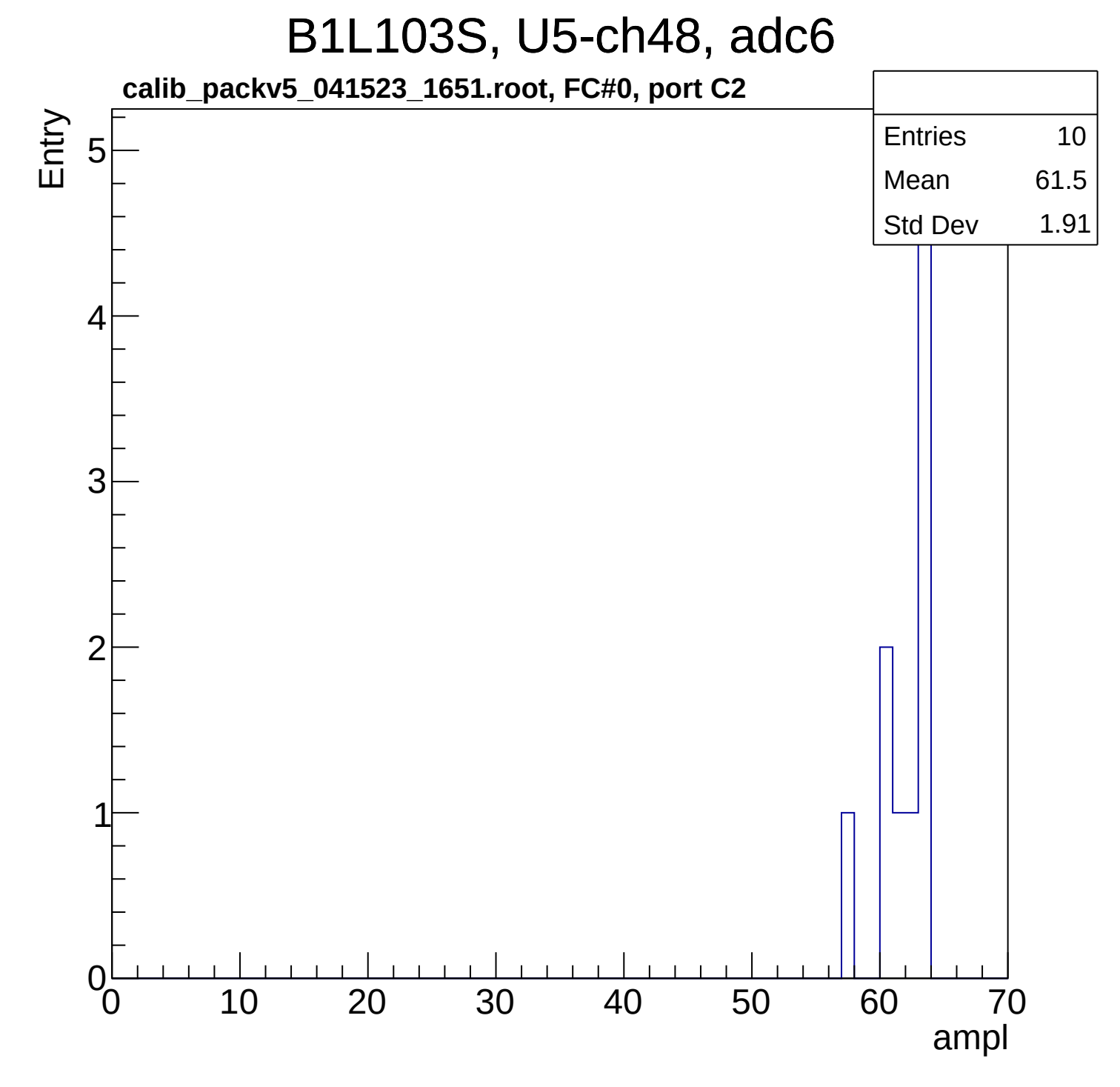
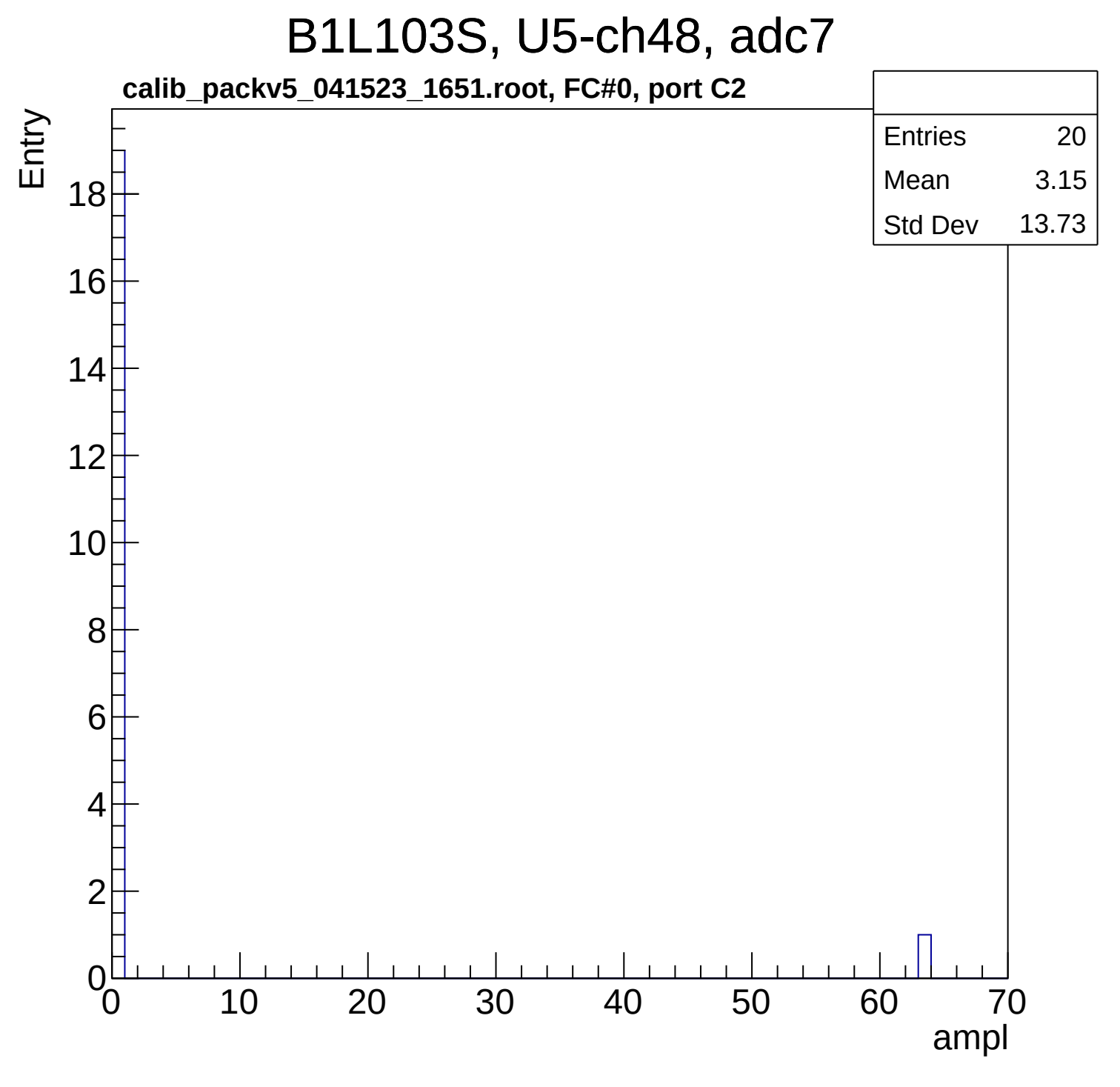

B1L103S, U5-ch48, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.5
Std Dev 1.91
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U5-ch48, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
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10
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10
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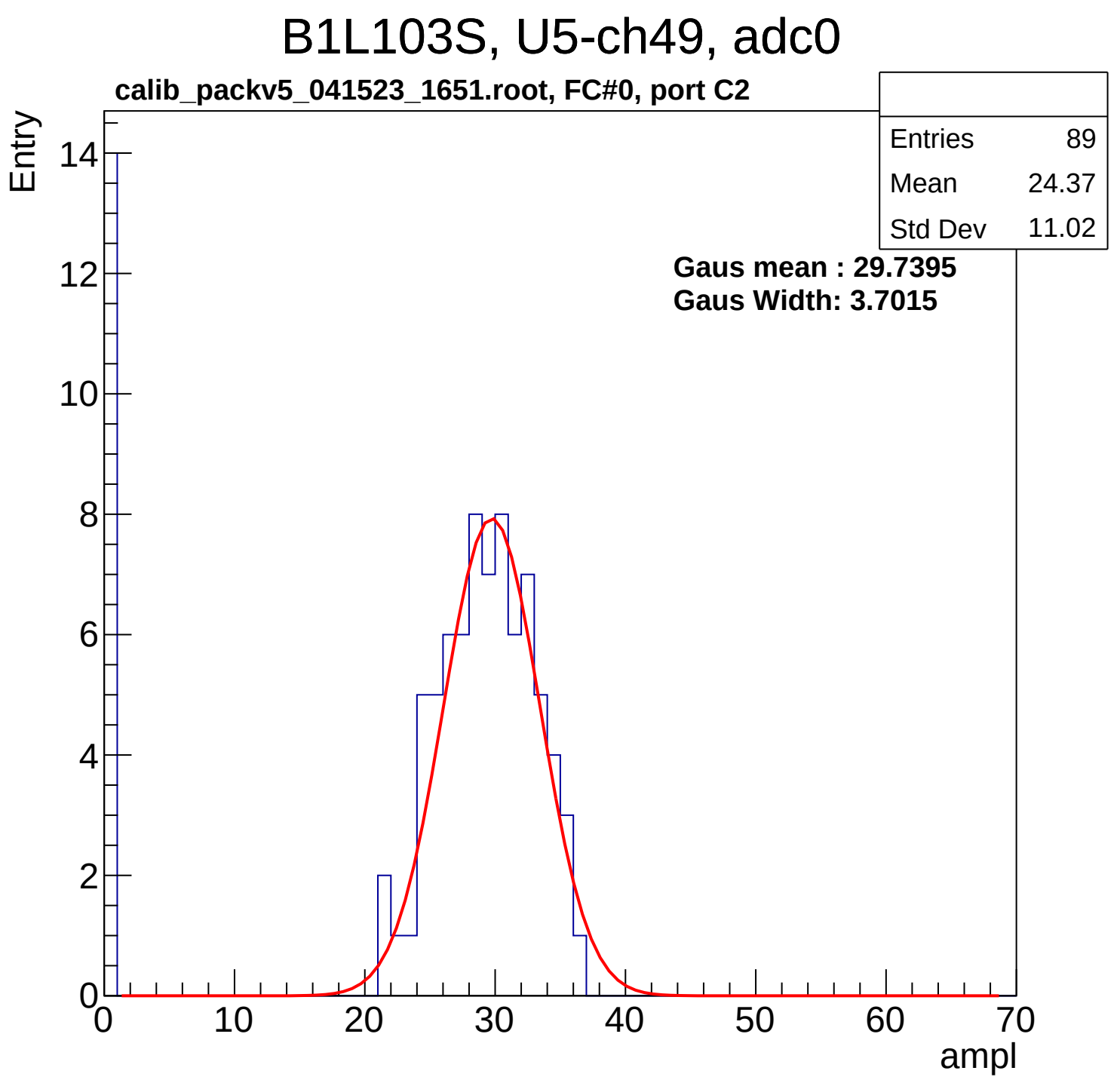
50
60
70
ampl


B1L103S, U5-ch49, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 24.37
Std Dev 11.02
Gaus mean : 29.7395
Gaus Width: 3.7015
Entry
ampl
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2
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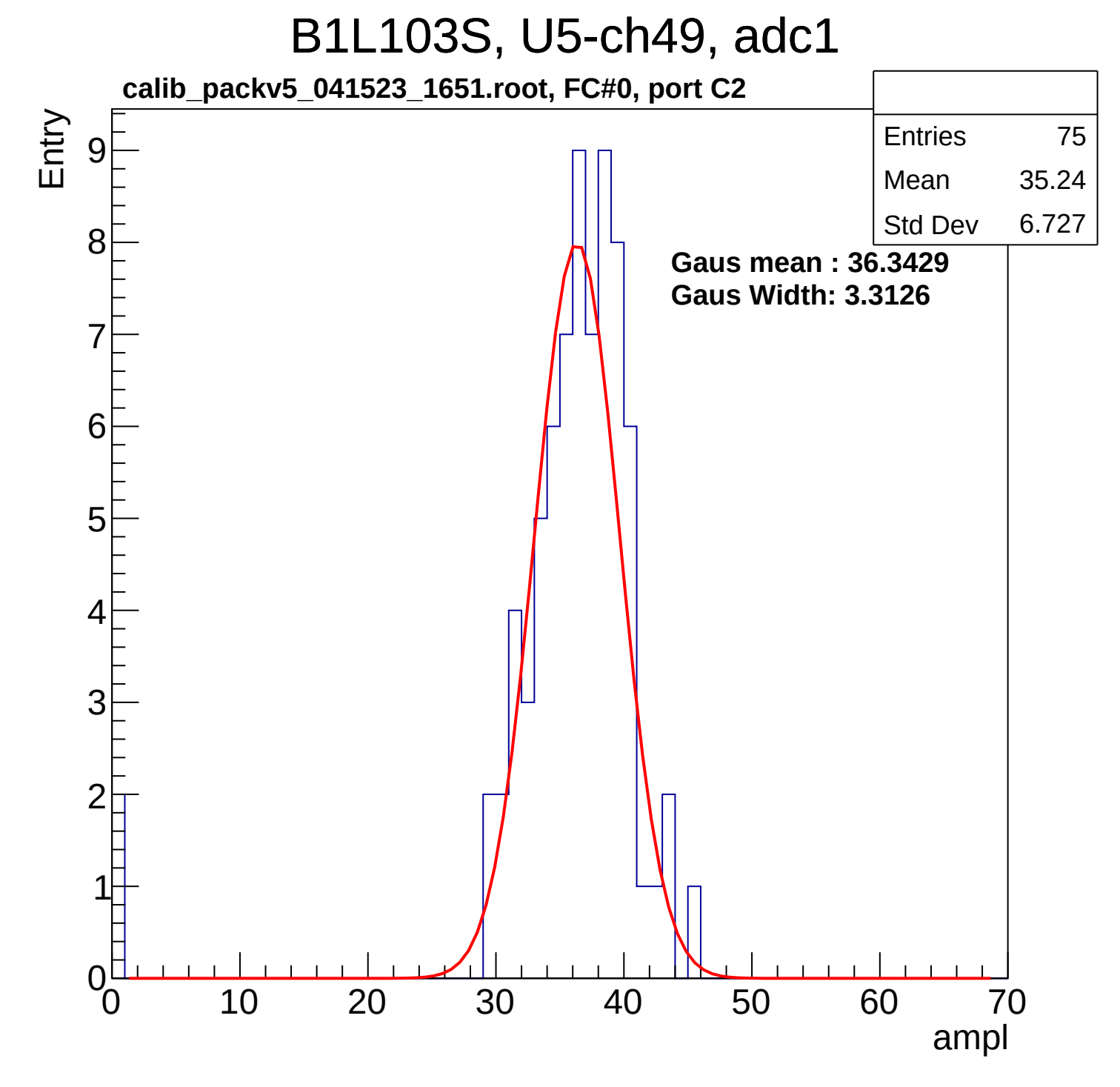
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U5-ch49, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 35.24
Std Dev 6.727
Gaus mean : 36.3429
Gaus Width: 3.3126
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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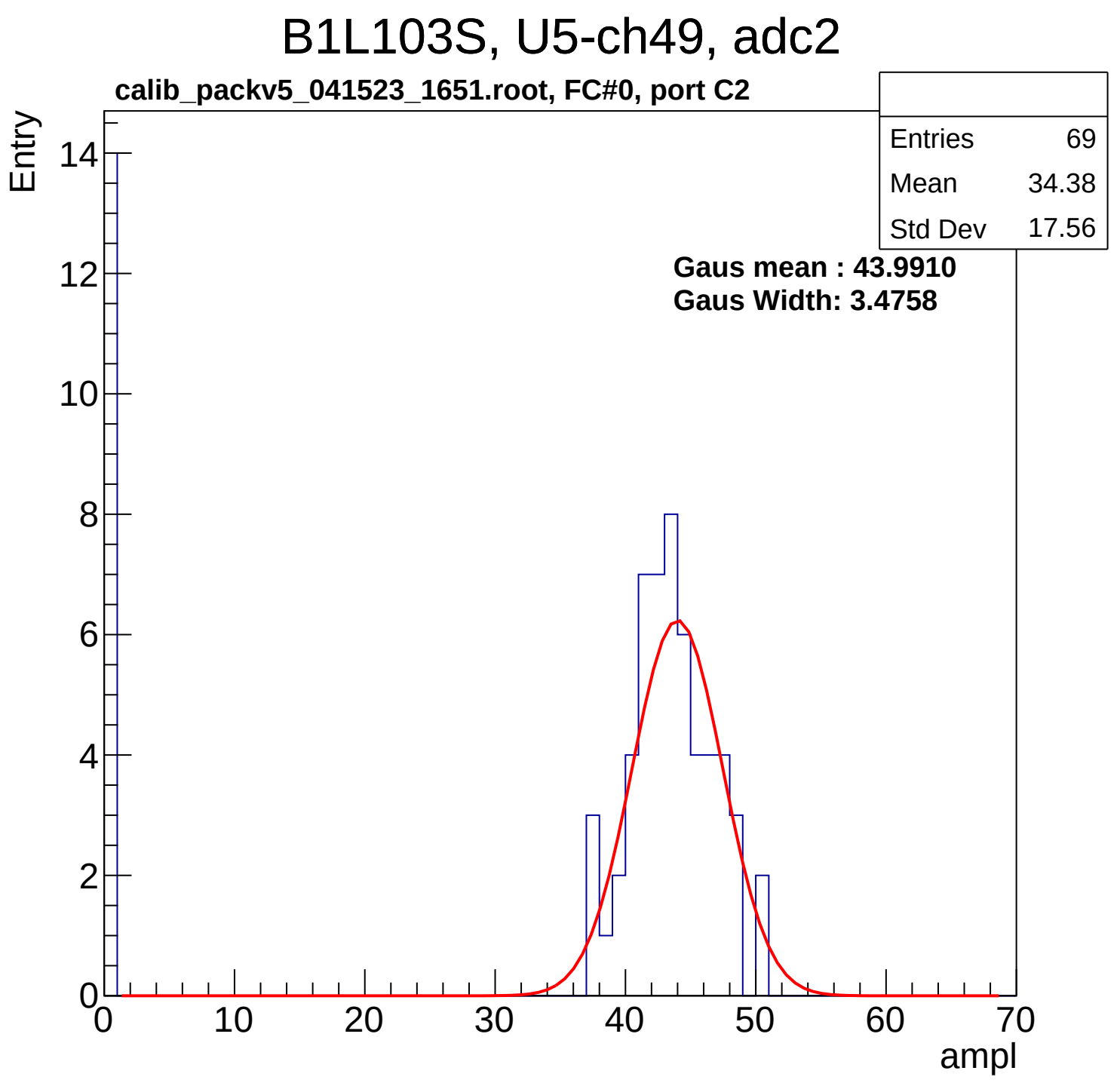
B1L103S, U5-ch49, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 34.38
Std Dev 17.56
Gaus mean : 43.9910
Gaus Width: 3.4758
Entry
ampl
0
2
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6
8
10
12
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0
10
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60
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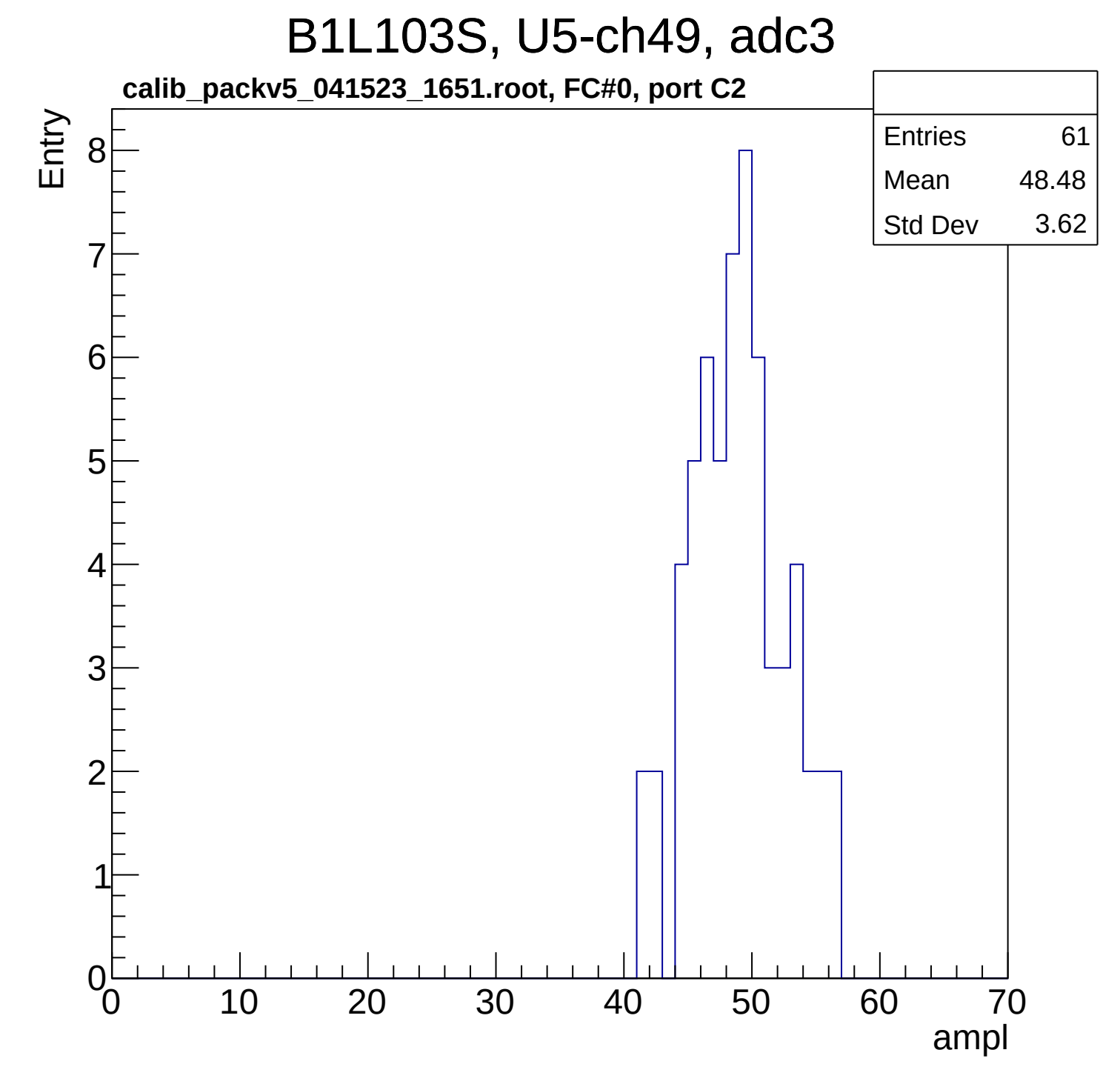
B1L103S, U5-ch49, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 48.48
Std Dev 3.62
Entry
ampl
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2
3
4
5
6
7
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0
10
20
30
40
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60
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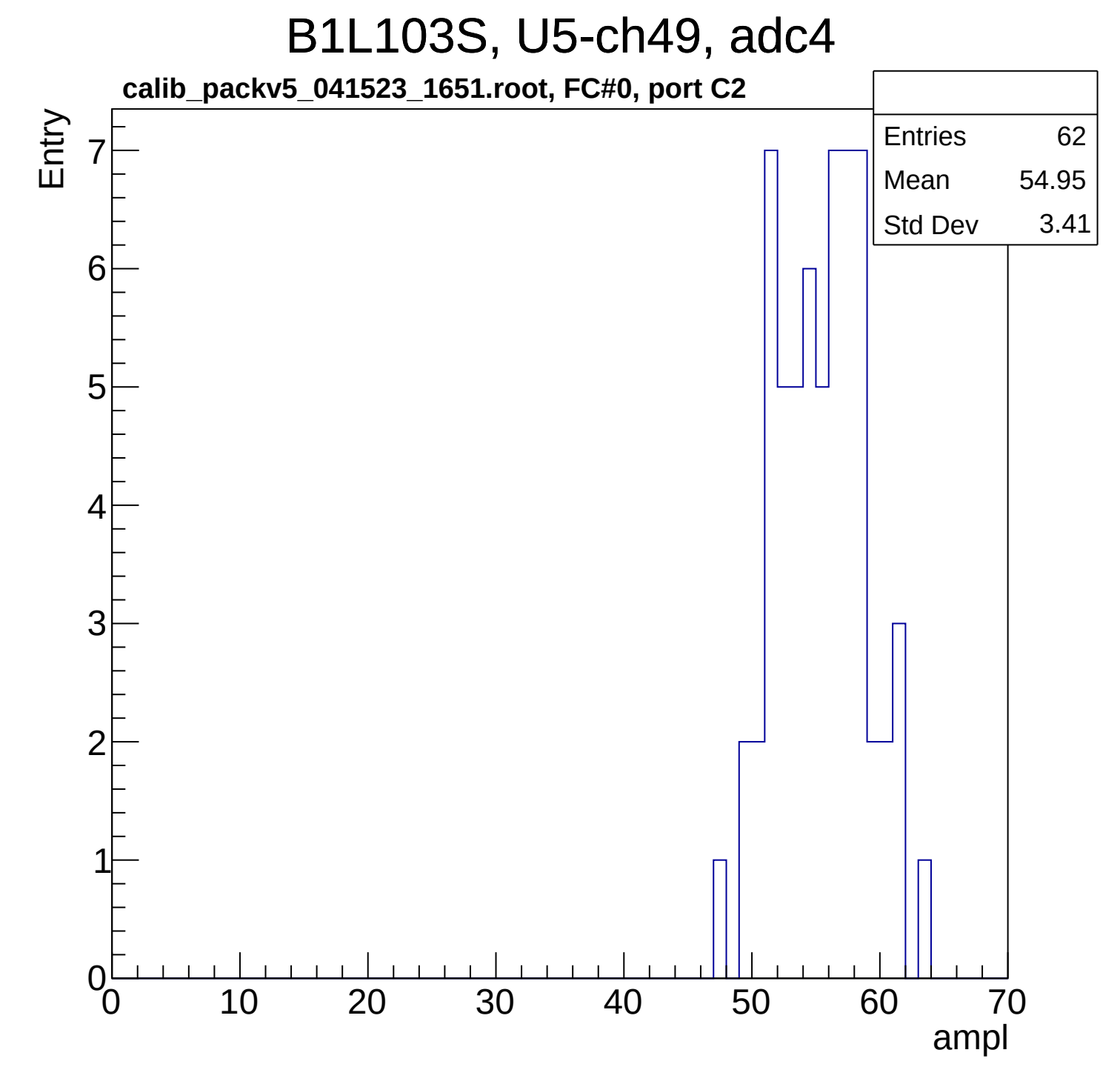
B1L103S, U5-ch49, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 54.95
Std Dev 3.41
Entry
ampl
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2
3
4
5
6
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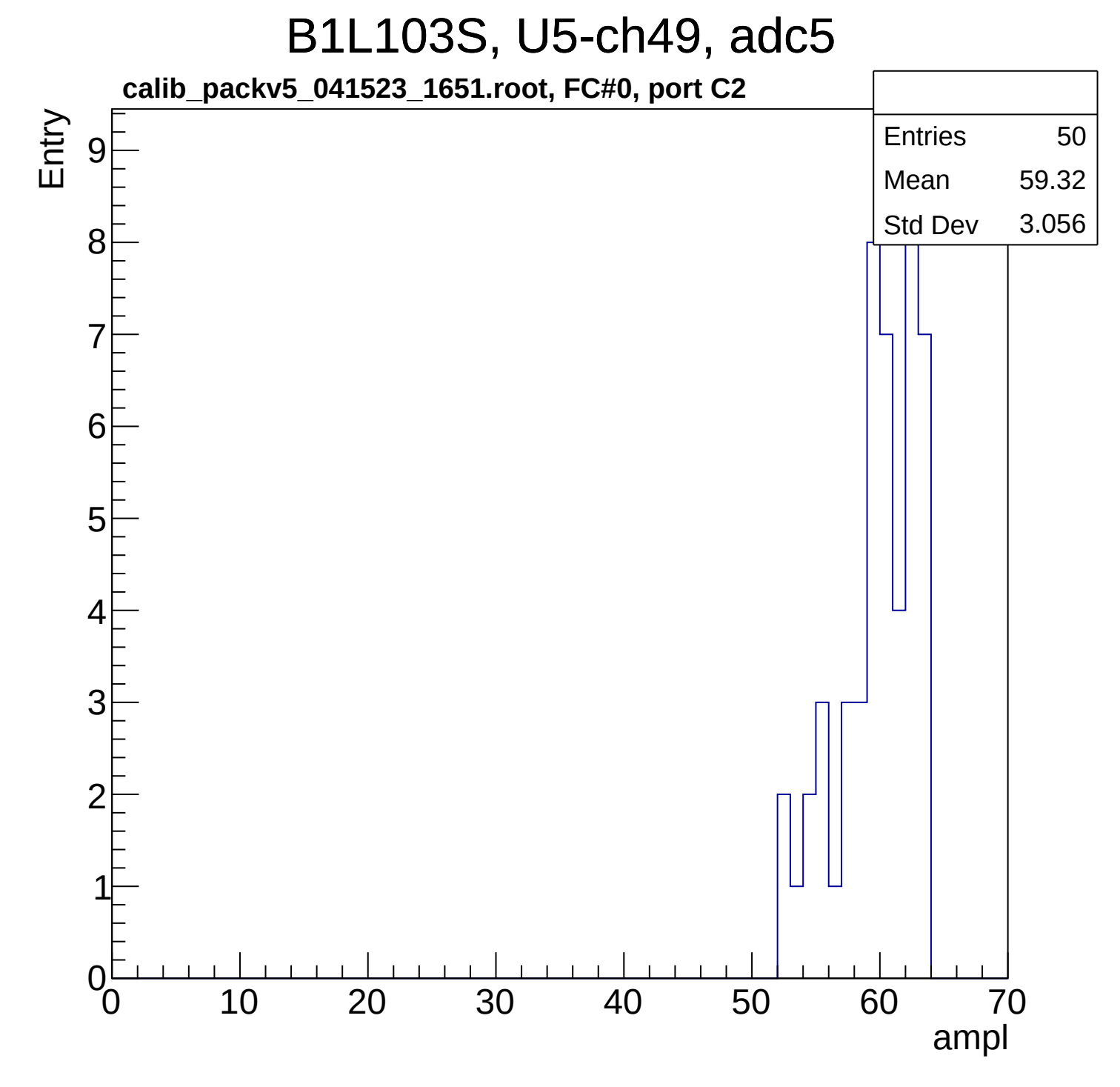
B1L103S, U5-ch49, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 59.32
Std Dev 3.056
Entry
ampl
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2
3
4
5
6
7
8
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0
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20
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60
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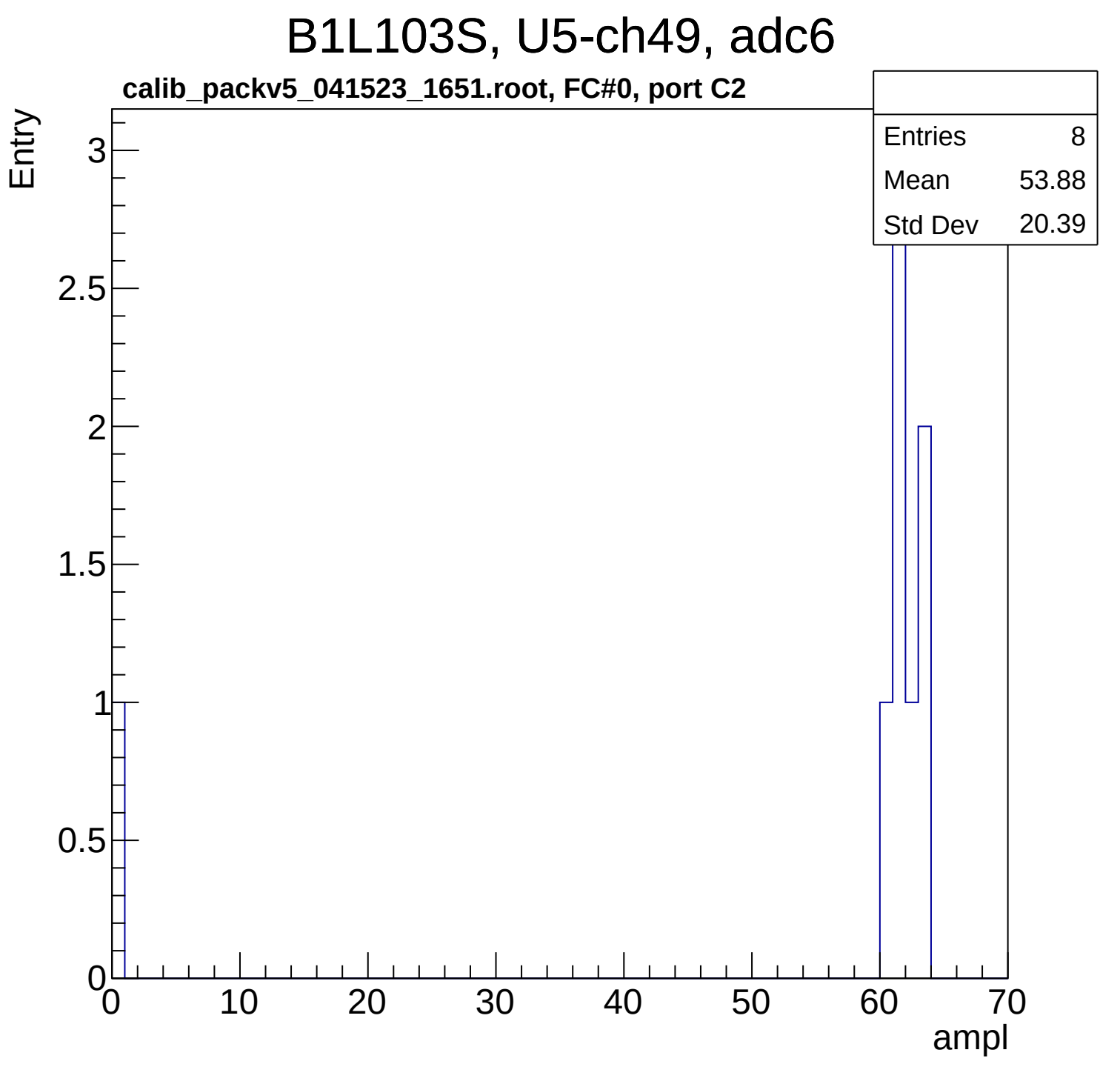
B1L103S, U5-ch49, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 53.88
Std Dev 20.39
Entry
ampl
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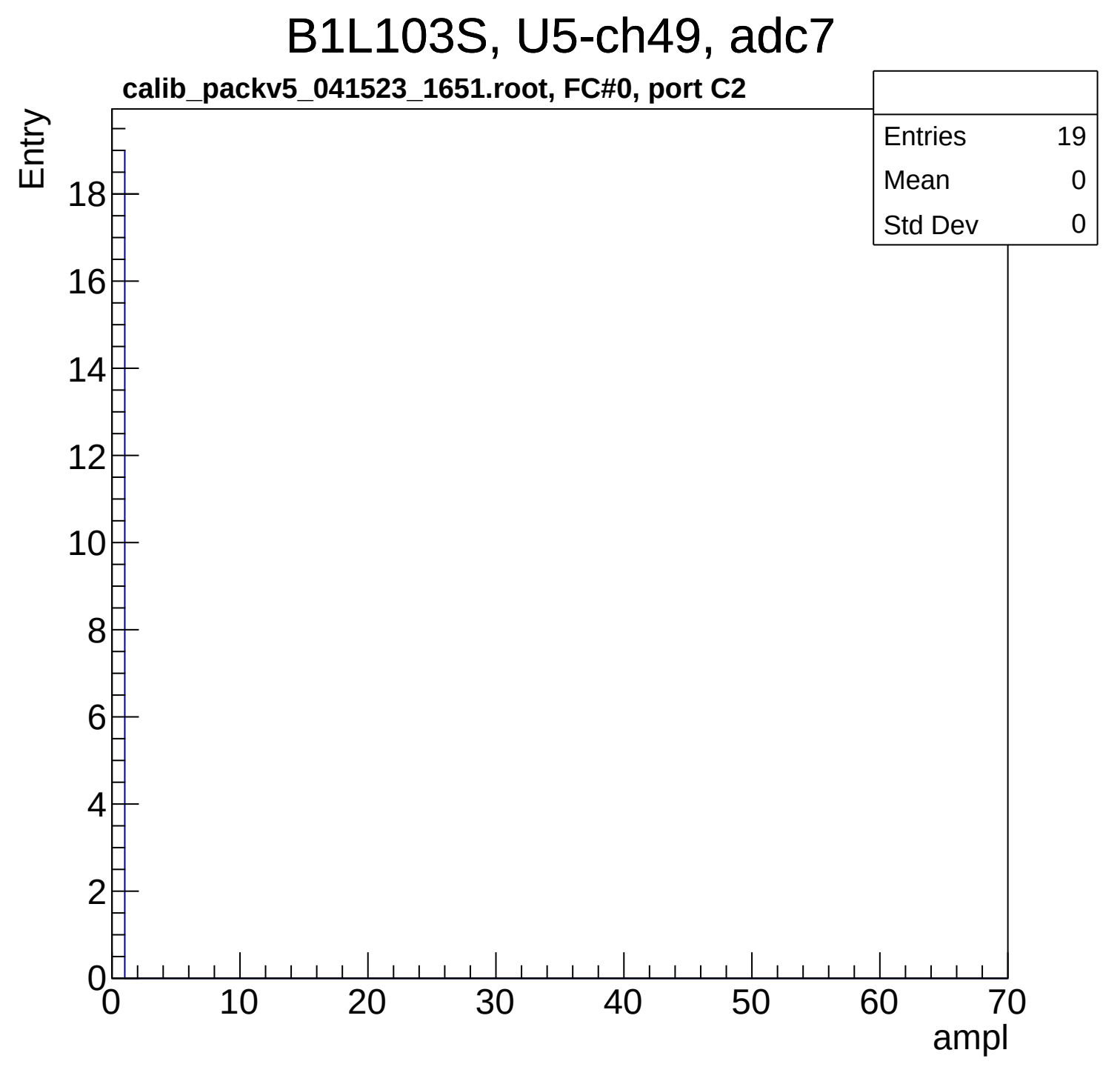
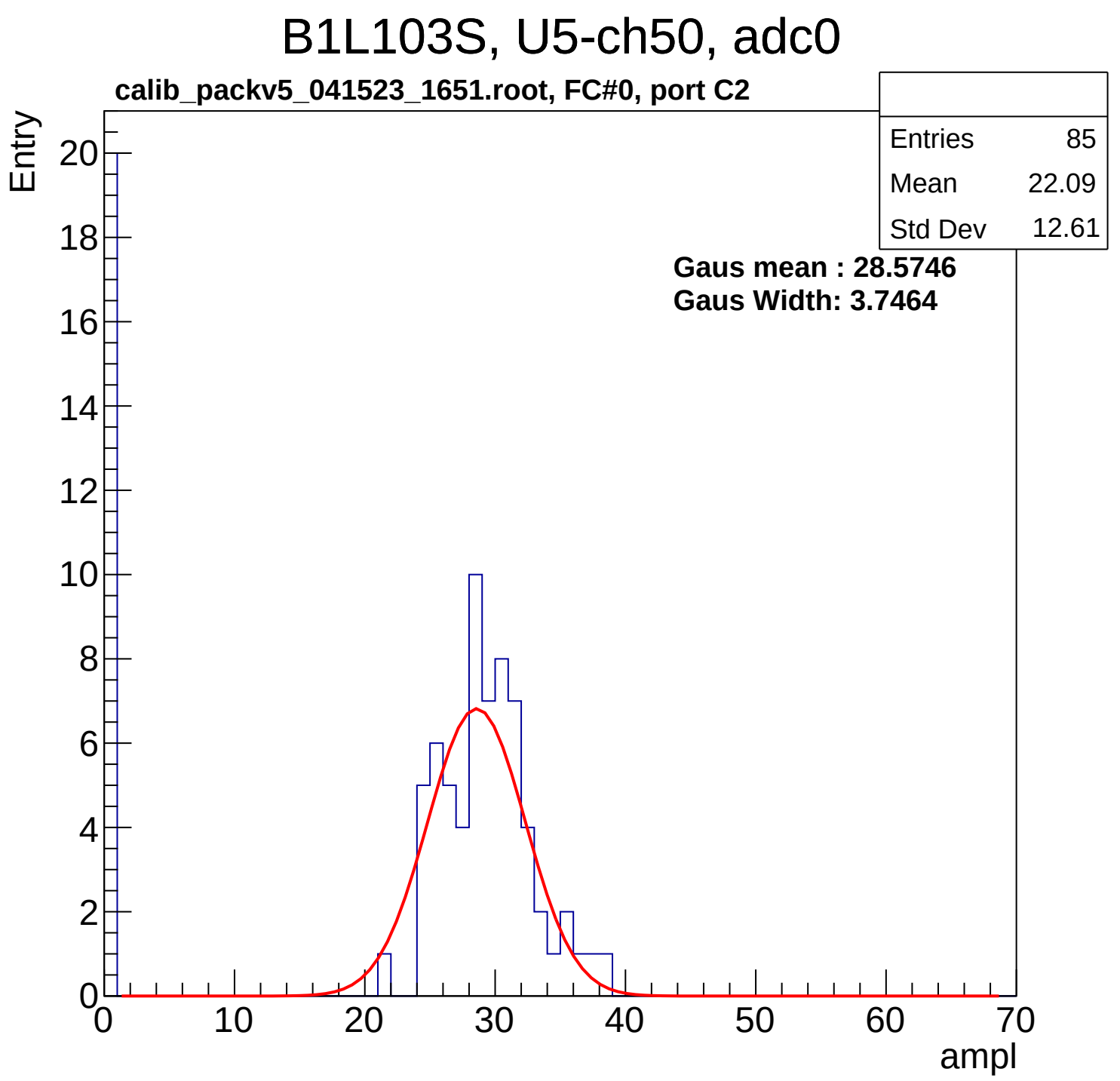
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U5-ch49, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch50, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 22.09
Std Dev 12.61
Gaus mean : 28.5746
Gaus Width: 3.7464
Entry
ampl
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6
8
10
12
14
16
18
20
0
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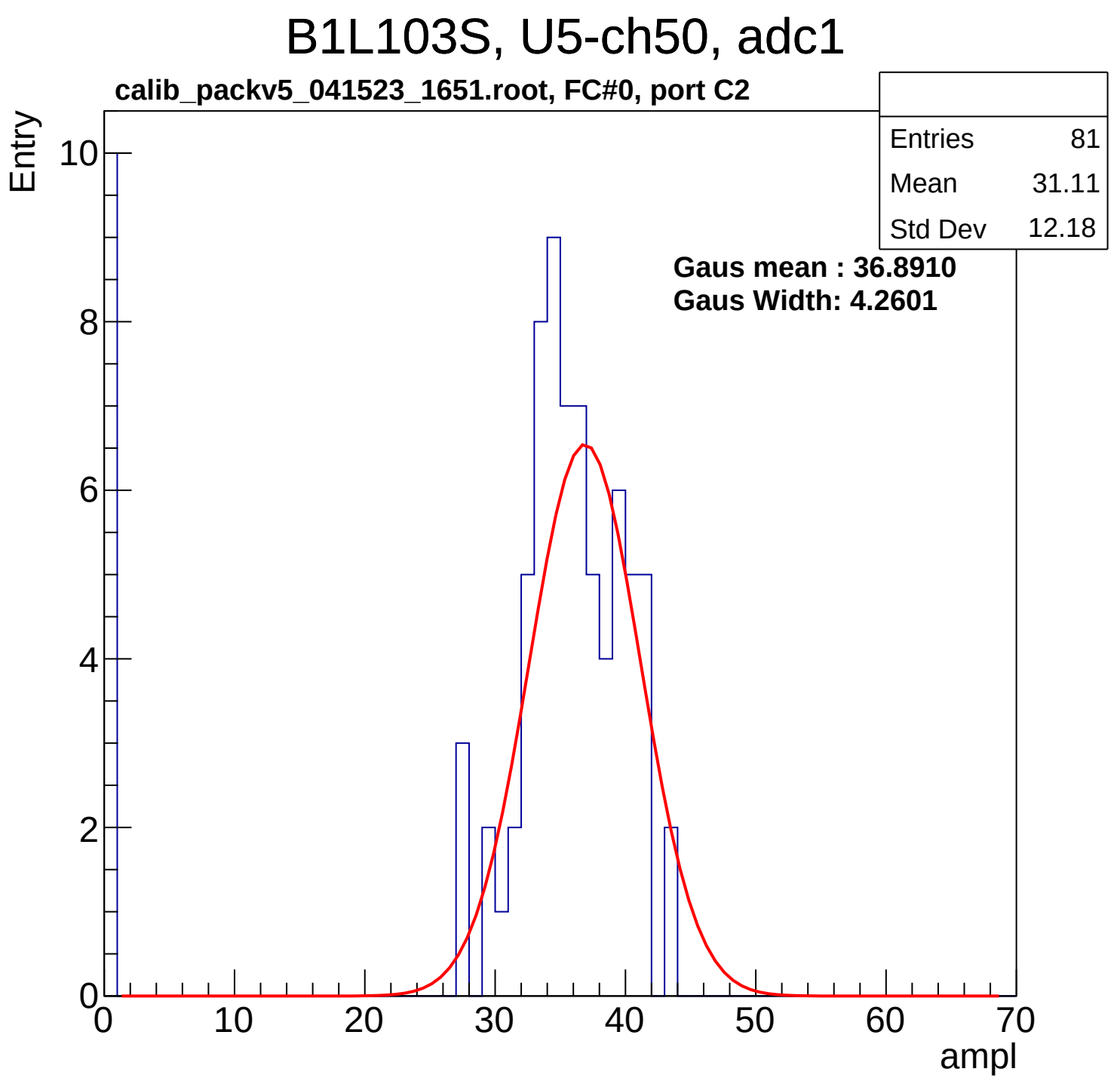
B1L103S, U5-ch50, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 31.11
Std Dev 12.18
Gaus mean : 36.8910
Gaus Width: 4.2601
Entry
ampl
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4
6
8
10
0
10
20
30
40
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60
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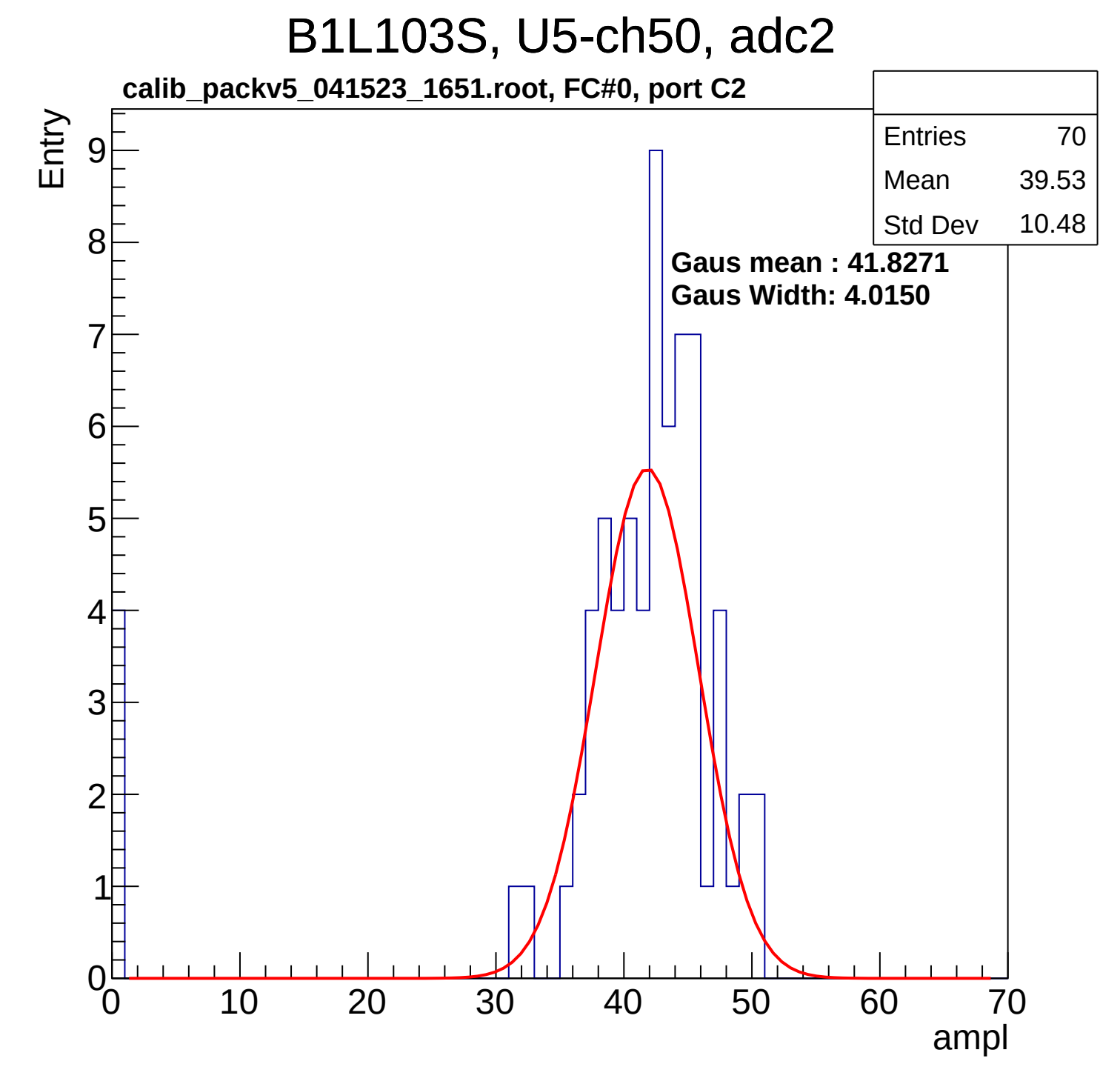
B1L103S, U5-ch50, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 39.53
Std Dev 10.48
Gaus mean : 41.8271
Gaus Width: 4.0150
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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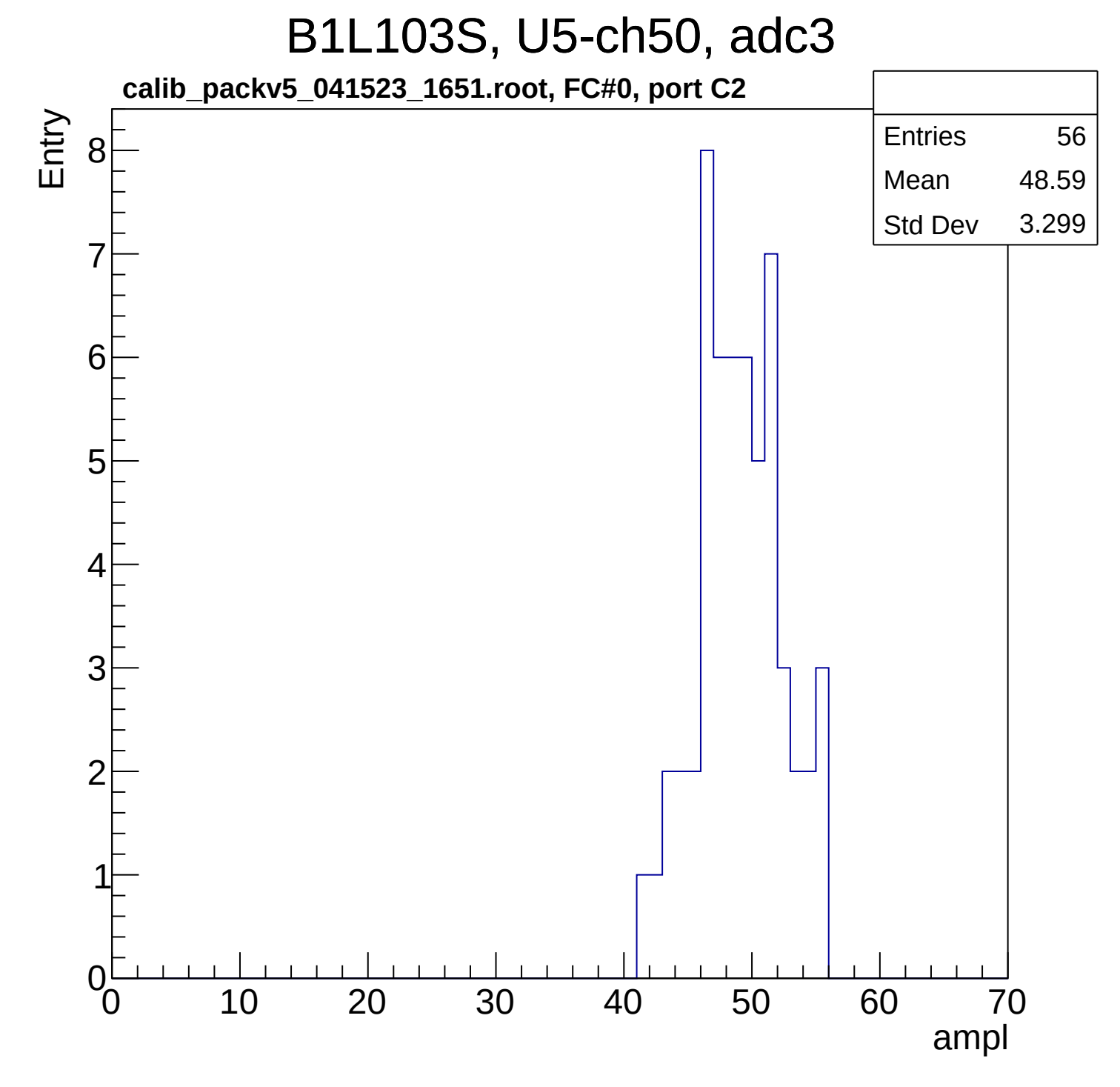
B1L103S, U5-ch50, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 48.59
Std Dev 3.299
Entry
ampl
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2
3
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5
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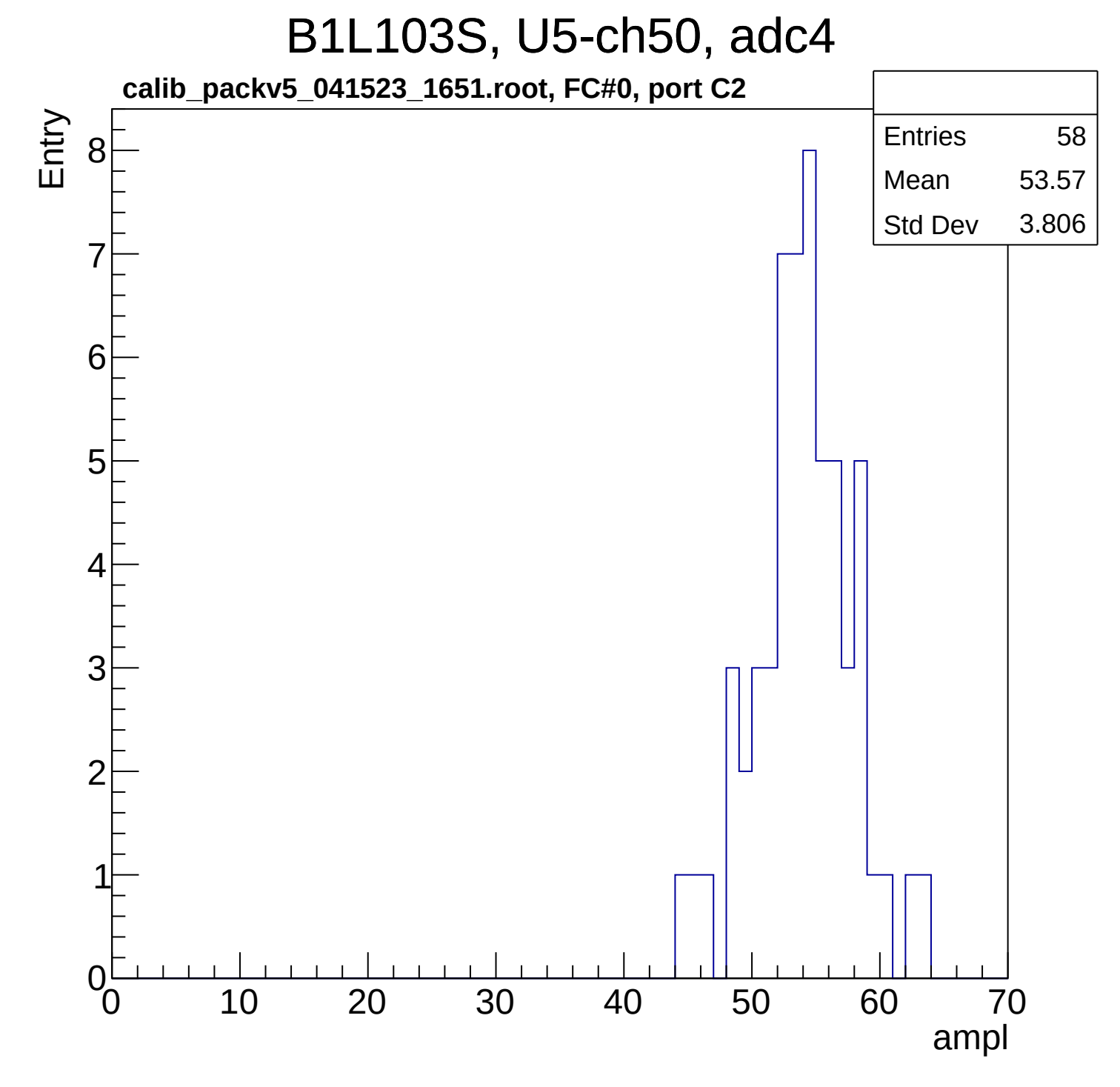
B1L103S, U5-ch50, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 53.57
Std Dev 3.806
Entry
ampl
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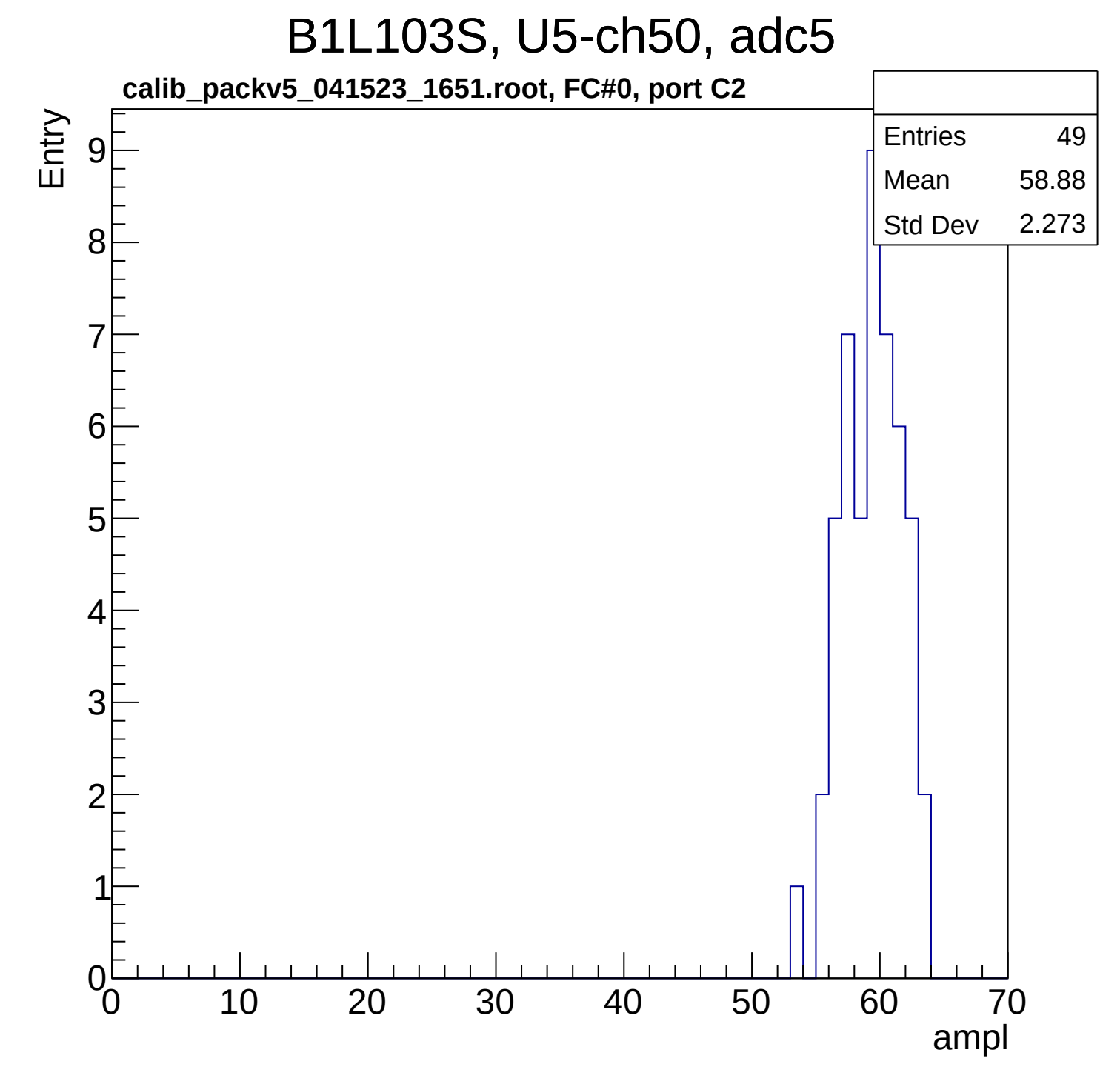
B1L103S, U5-ch50, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.88
Std Dev 2.273
Entry
ampl
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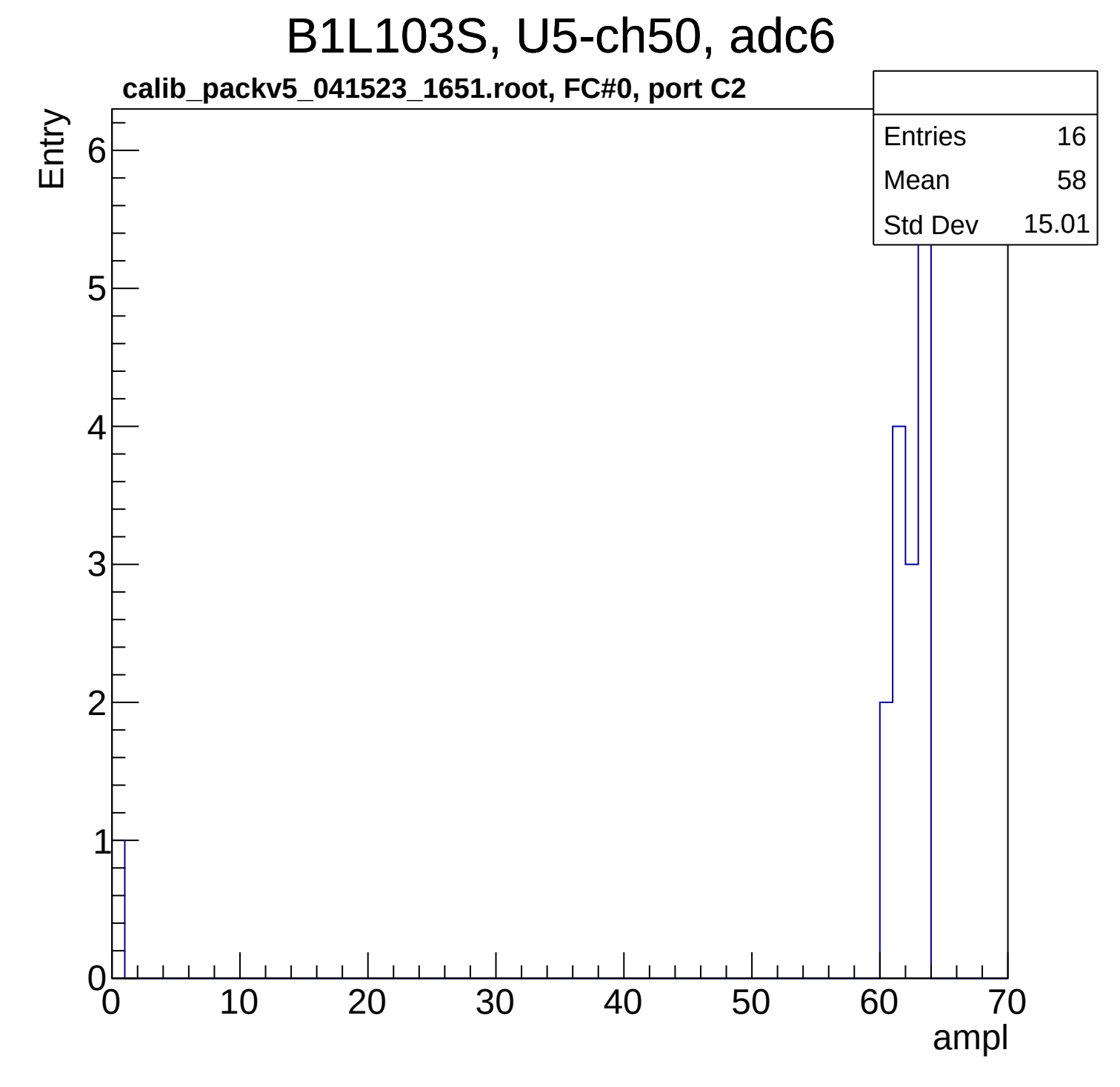
B1L103S, U5-ch50, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 58
Std Dev 15.01
Entry
ampl
0
1
2
3
4
5
6
0
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40
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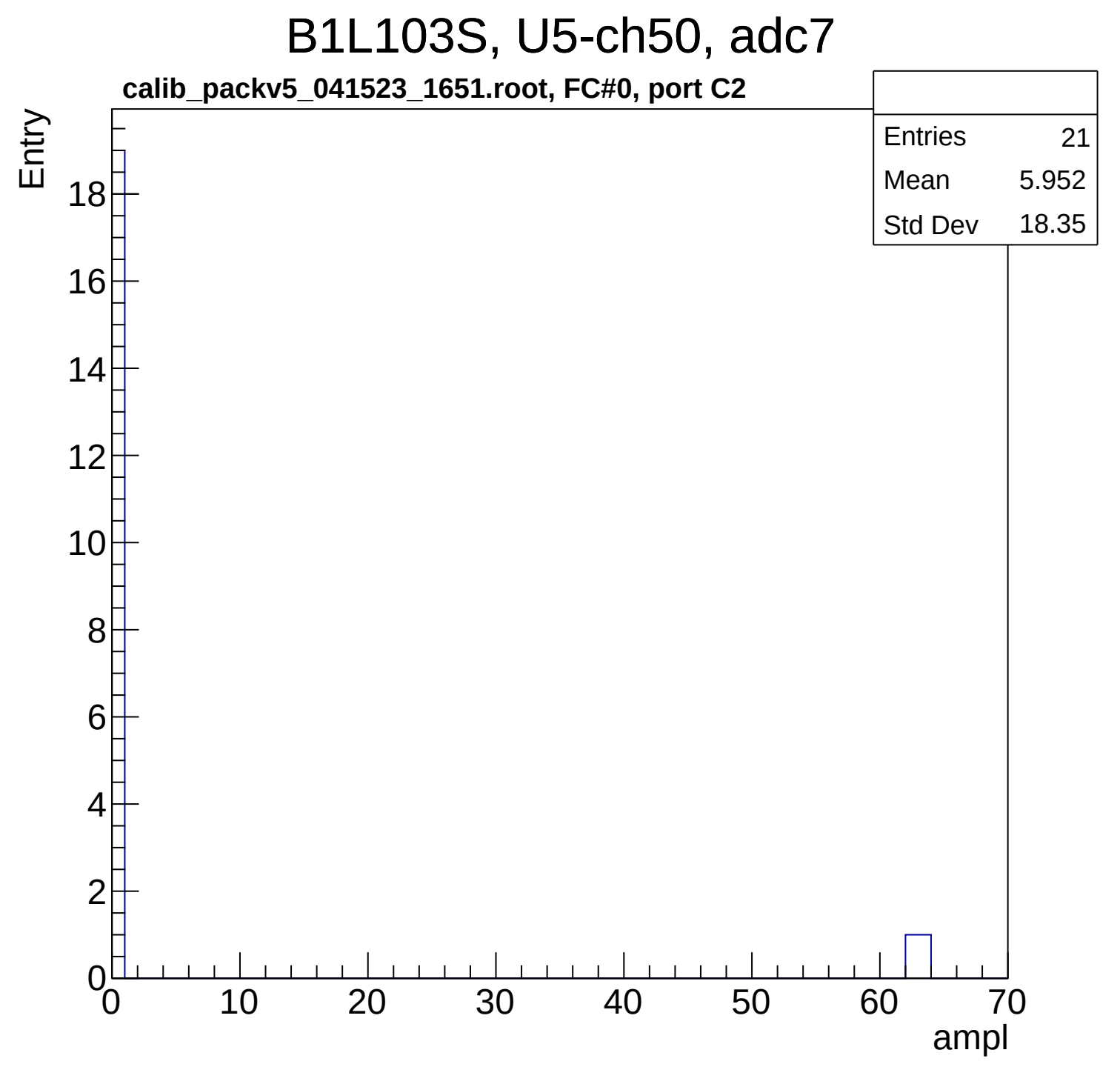
B1L103S, U5-ch50, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
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8
10
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14
16
18
0
10
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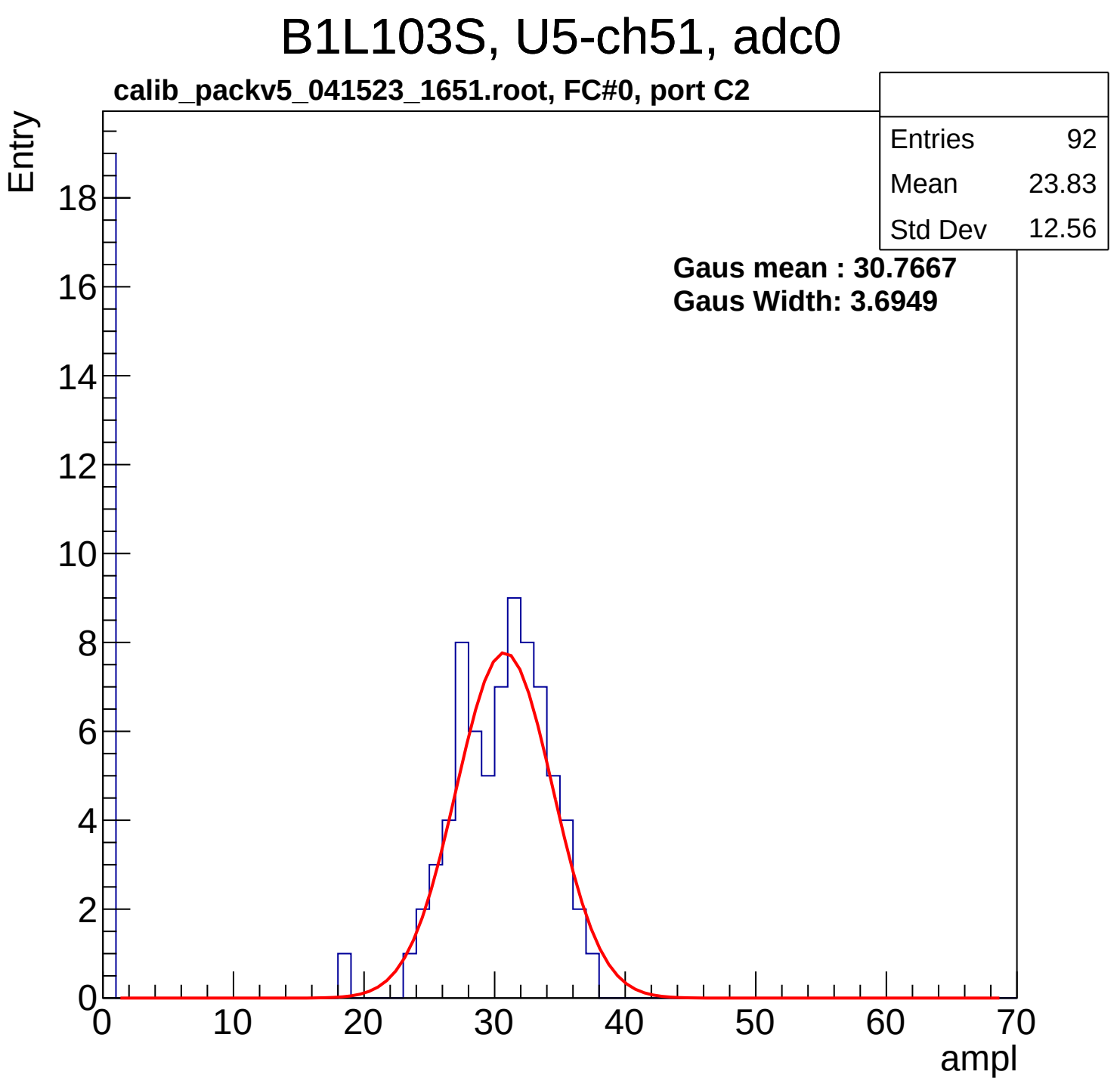
50
60
70
ampl


B1L103S, U5-ch51, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 23.83
Std Dev 12.56
Gaus mean : 30.7667
Gaus Width: 3.6949
Entry
ampl
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2
4
6
8
10
12
14
16
18
0
10
20
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40
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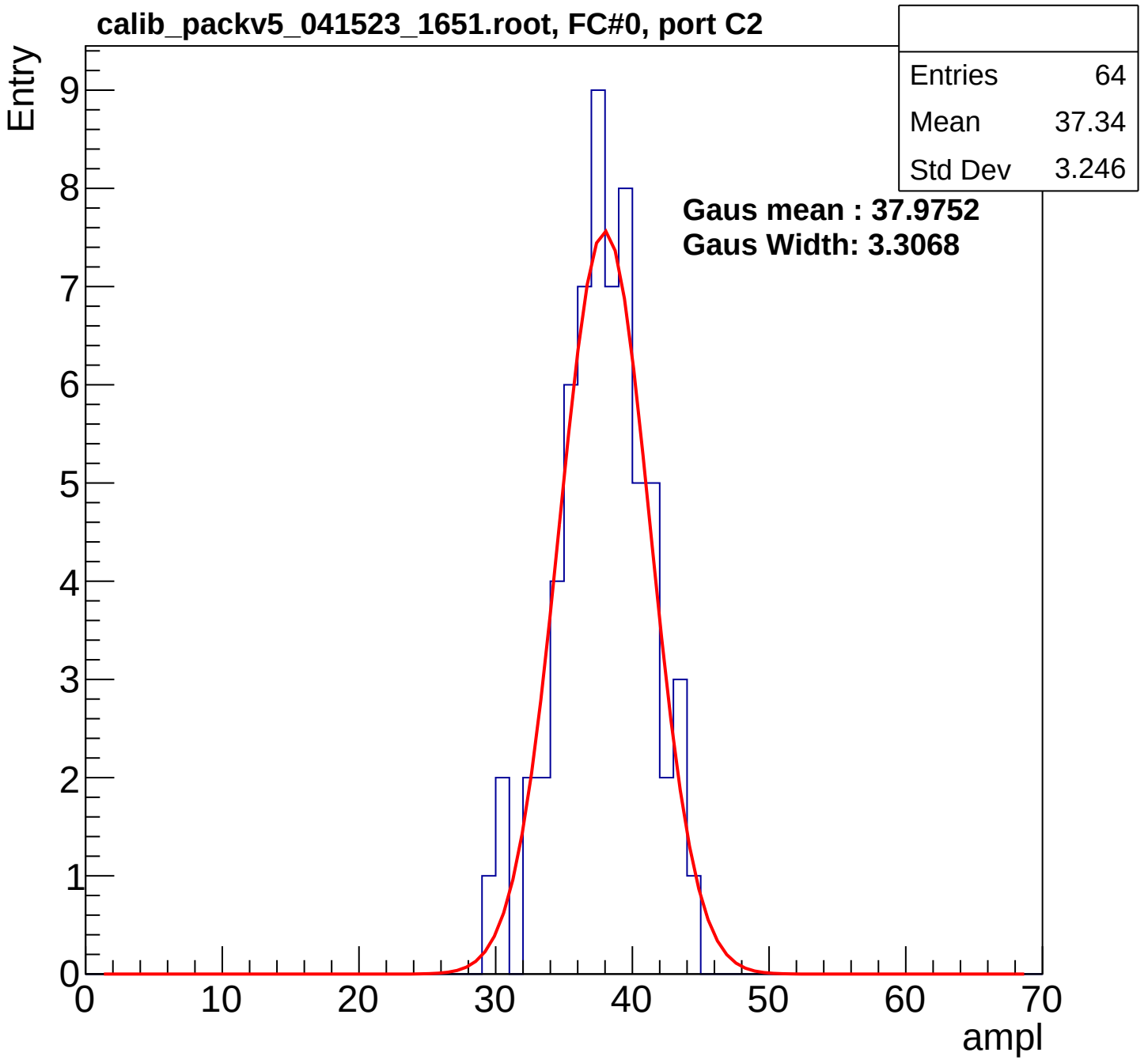
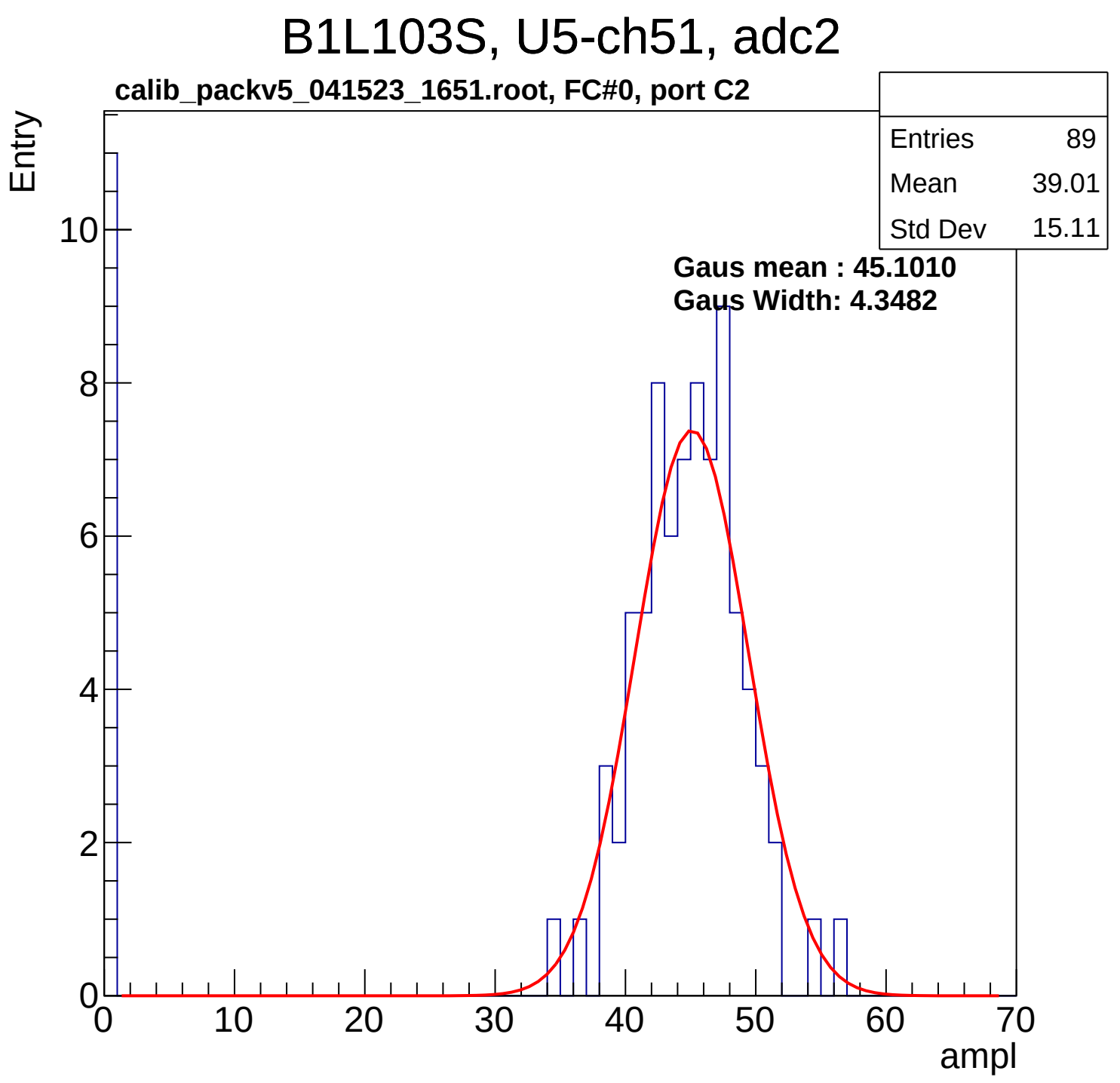

B1L103S, U5-ch51, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 37.34
Std Dev 3.246
Gaus mean : 37.9752
Gaus Width: 3.3068
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U5-ch51, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 39.01
Std Dev 15.11
Gaus mean : 45.1010
Gaus Width: 4.3482
Entry
ampl
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2
4
6
8
10
0
10
20
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50
60
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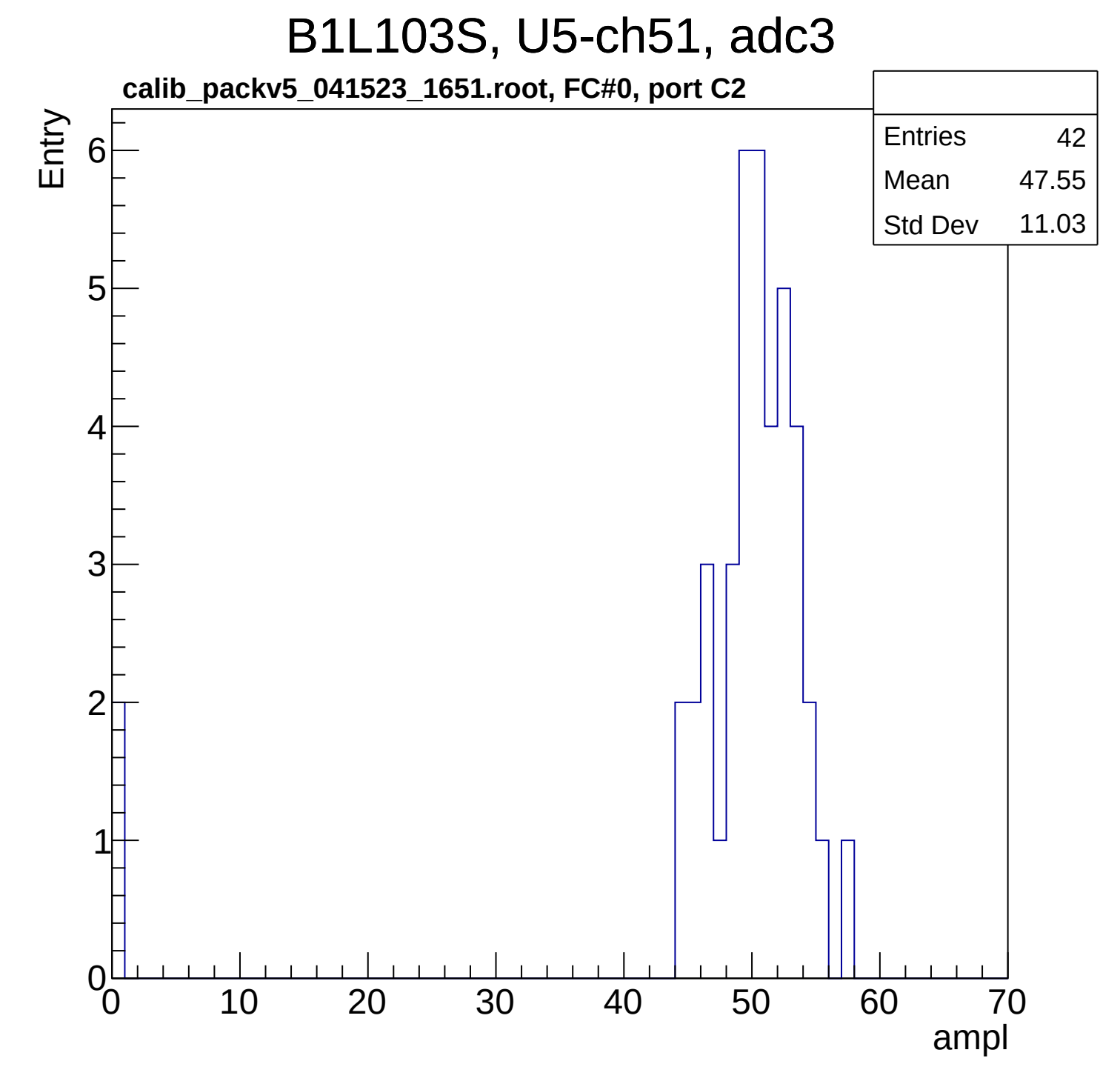
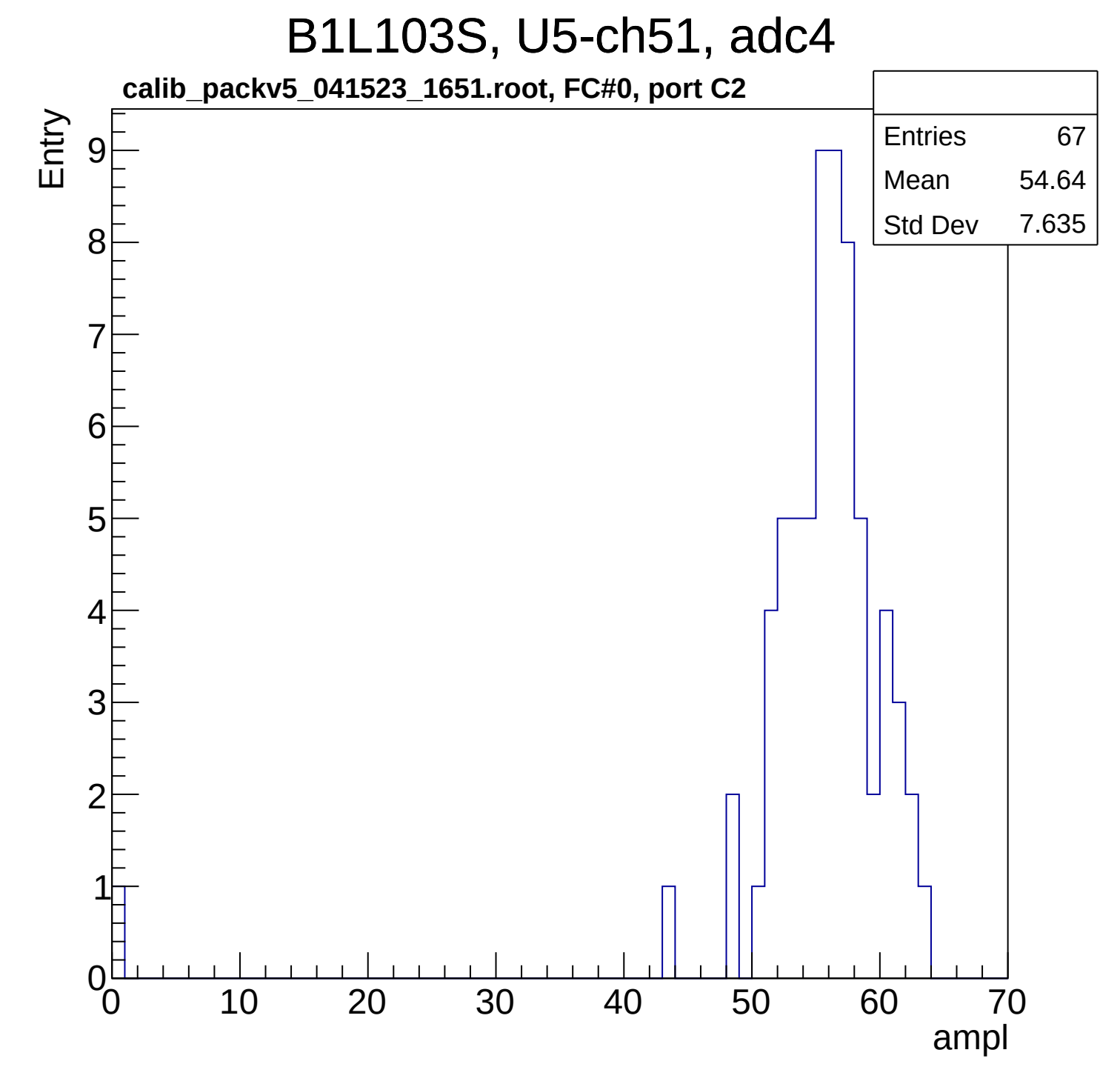

B1L103S, U5-ch51, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 47.55
Std Dev 11.03
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch51, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 54.64
Std Dev 7.635
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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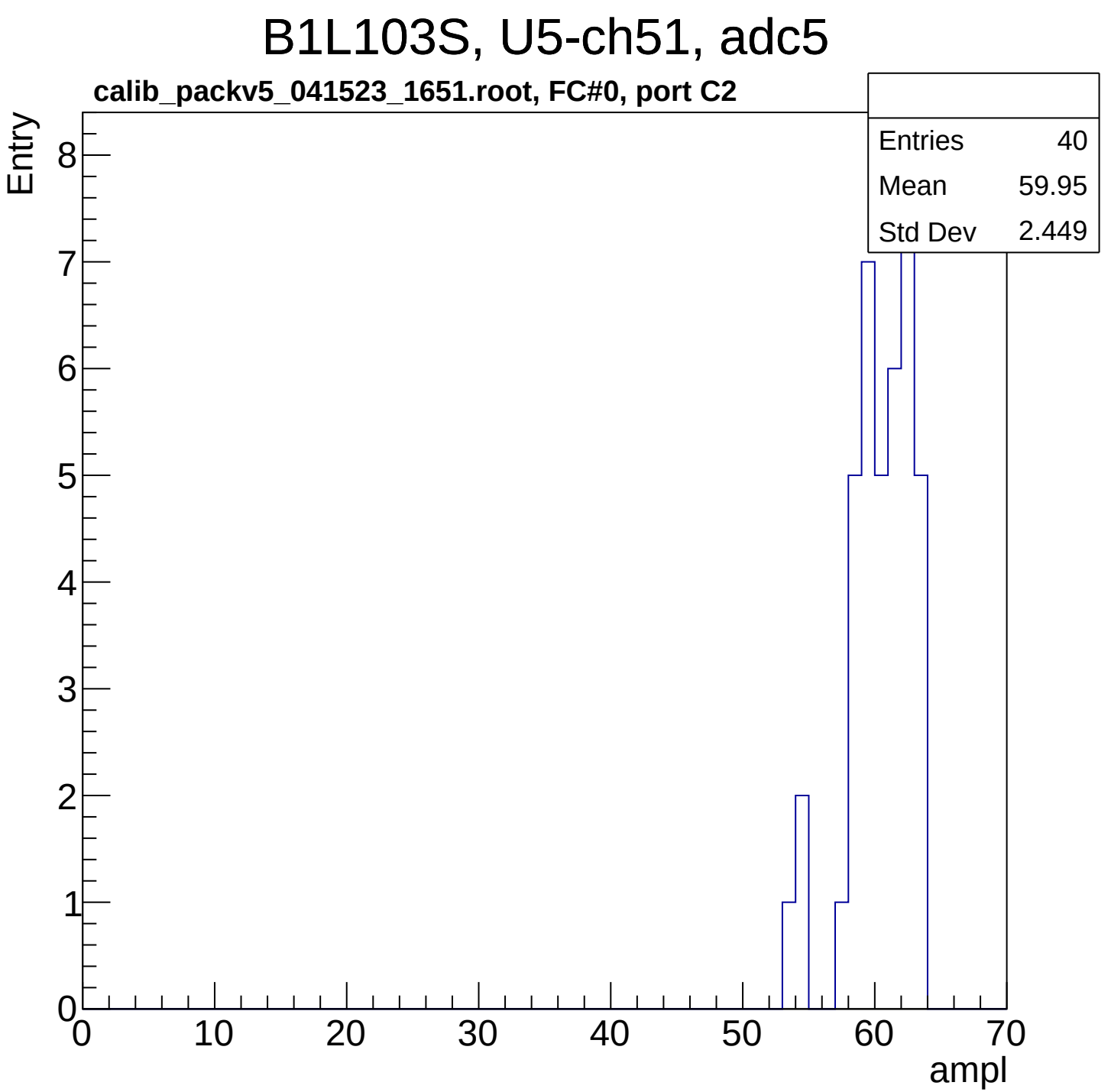
B1L103S, U5-ch51, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 59.95
Std Dev 2.449
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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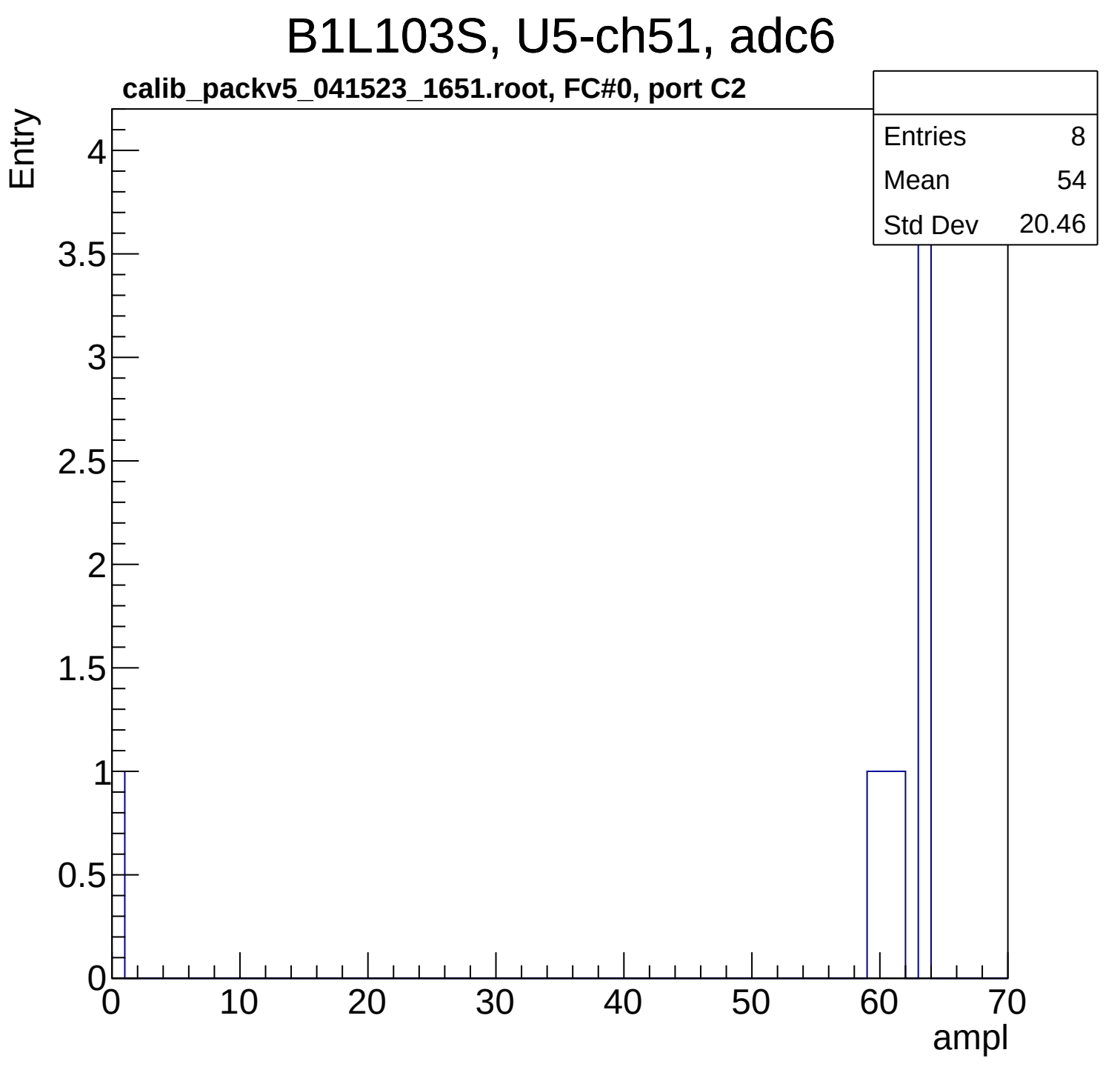
B1L103S, U5-ch51, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 54
Std Dev 20.46
Entry
ampl
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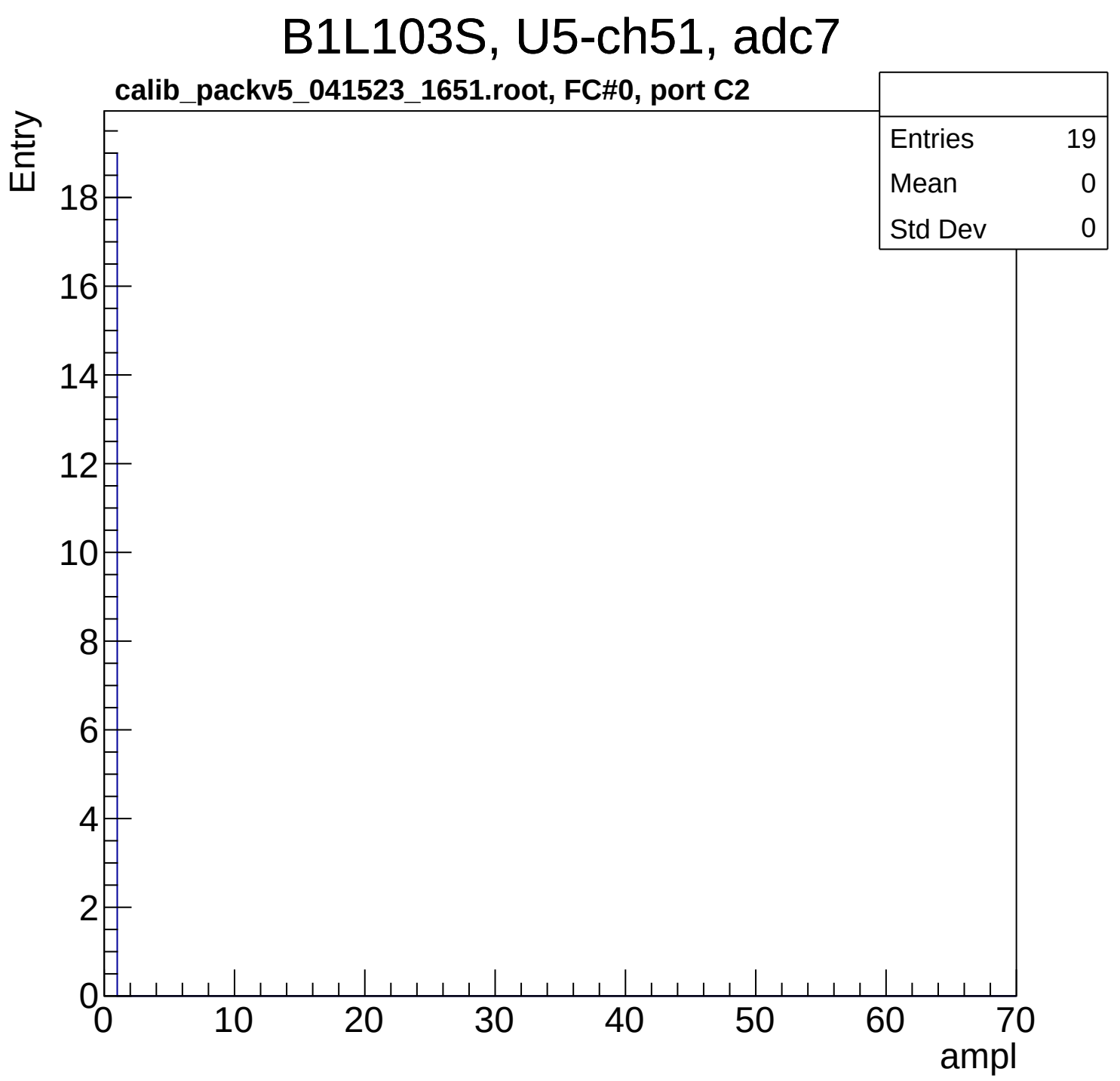
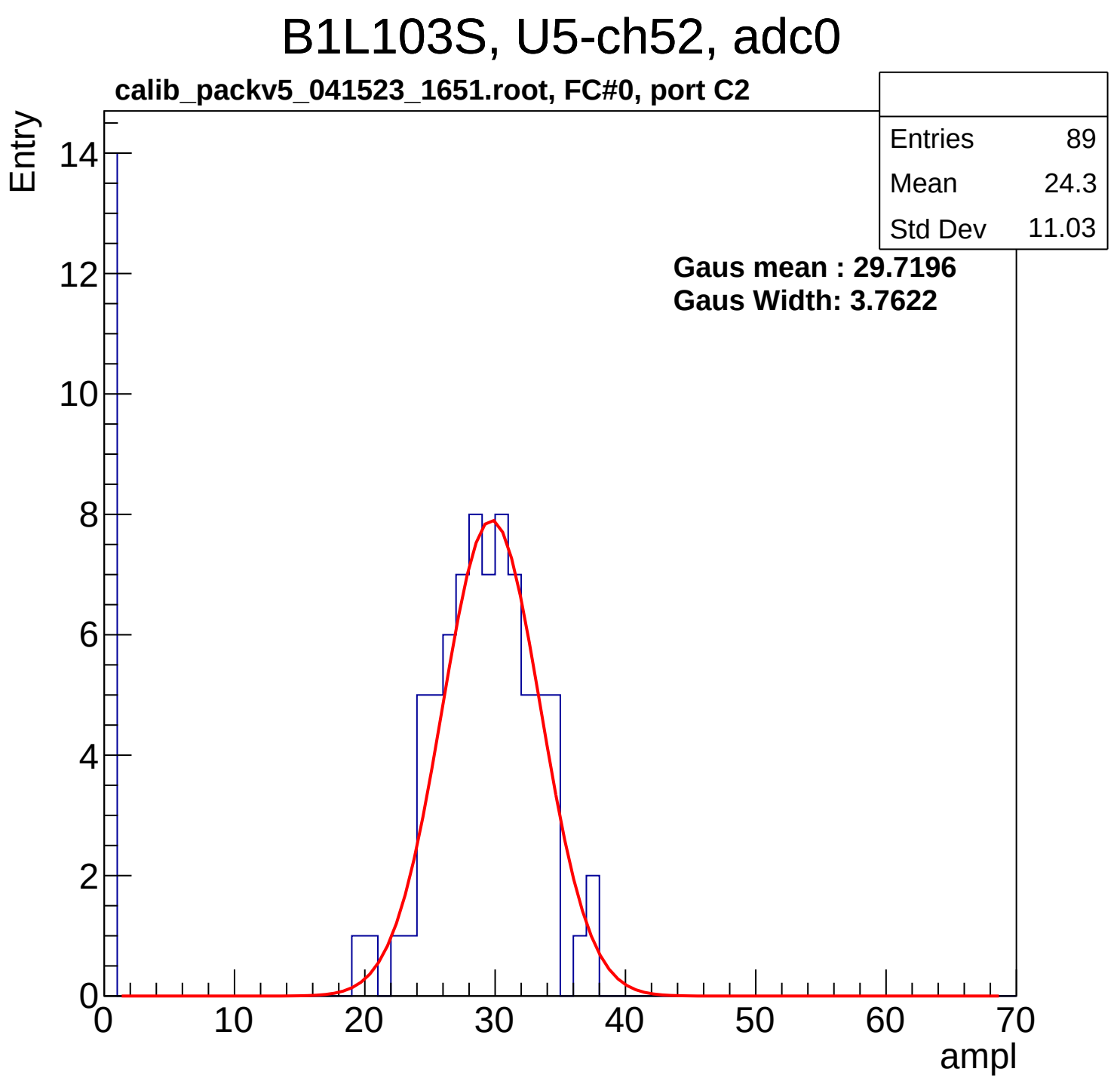
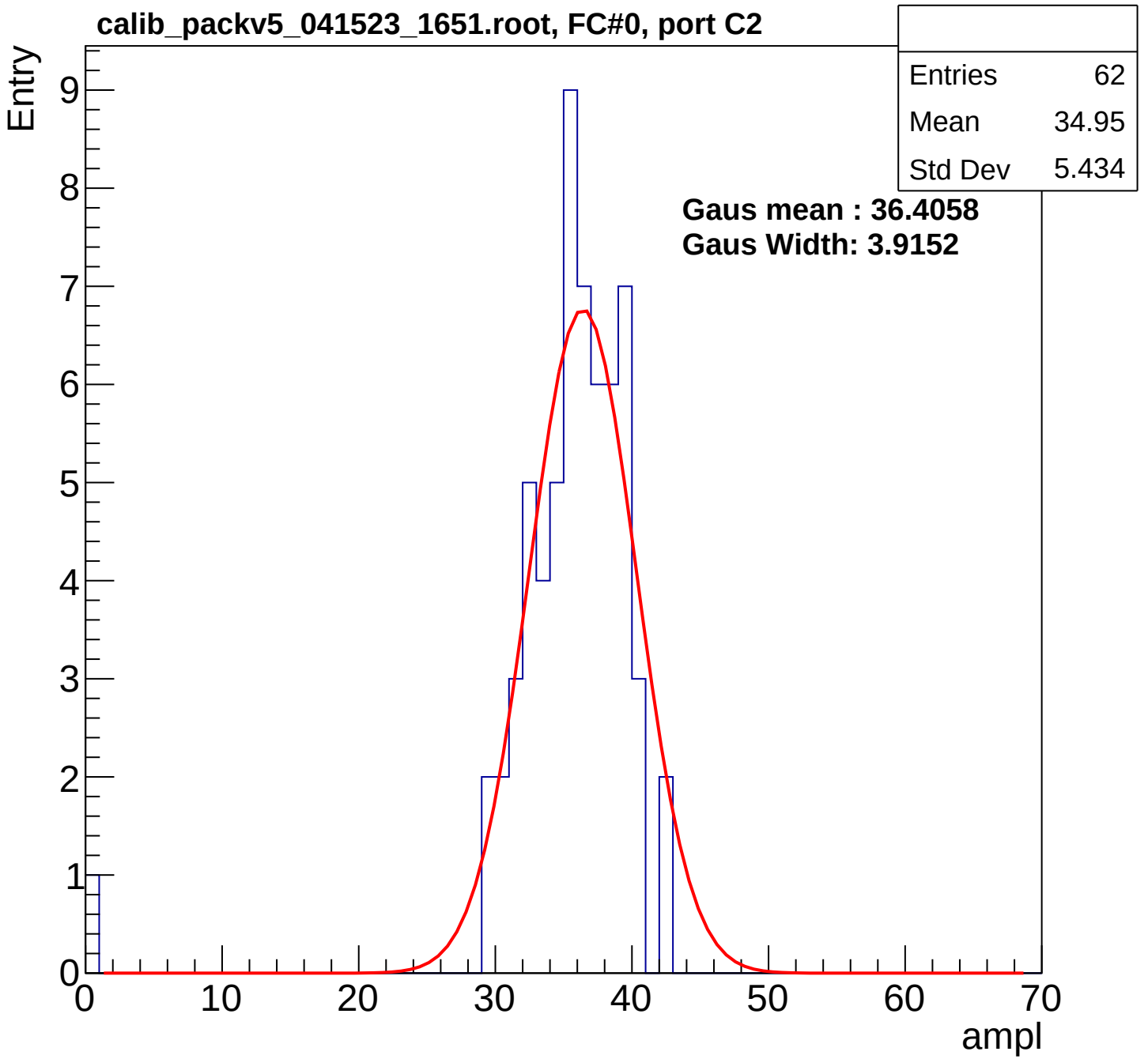
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U5-ch51, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch52, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 24.3
Std Dev 11.03
Gaus mean : 29.7196
Gaus Width: 3.7622
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U5-ch52, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 34.95
Std Dev 5.434
Gaus mean : 36.4058
Gaus Width: 3.9152
Entry
ampl
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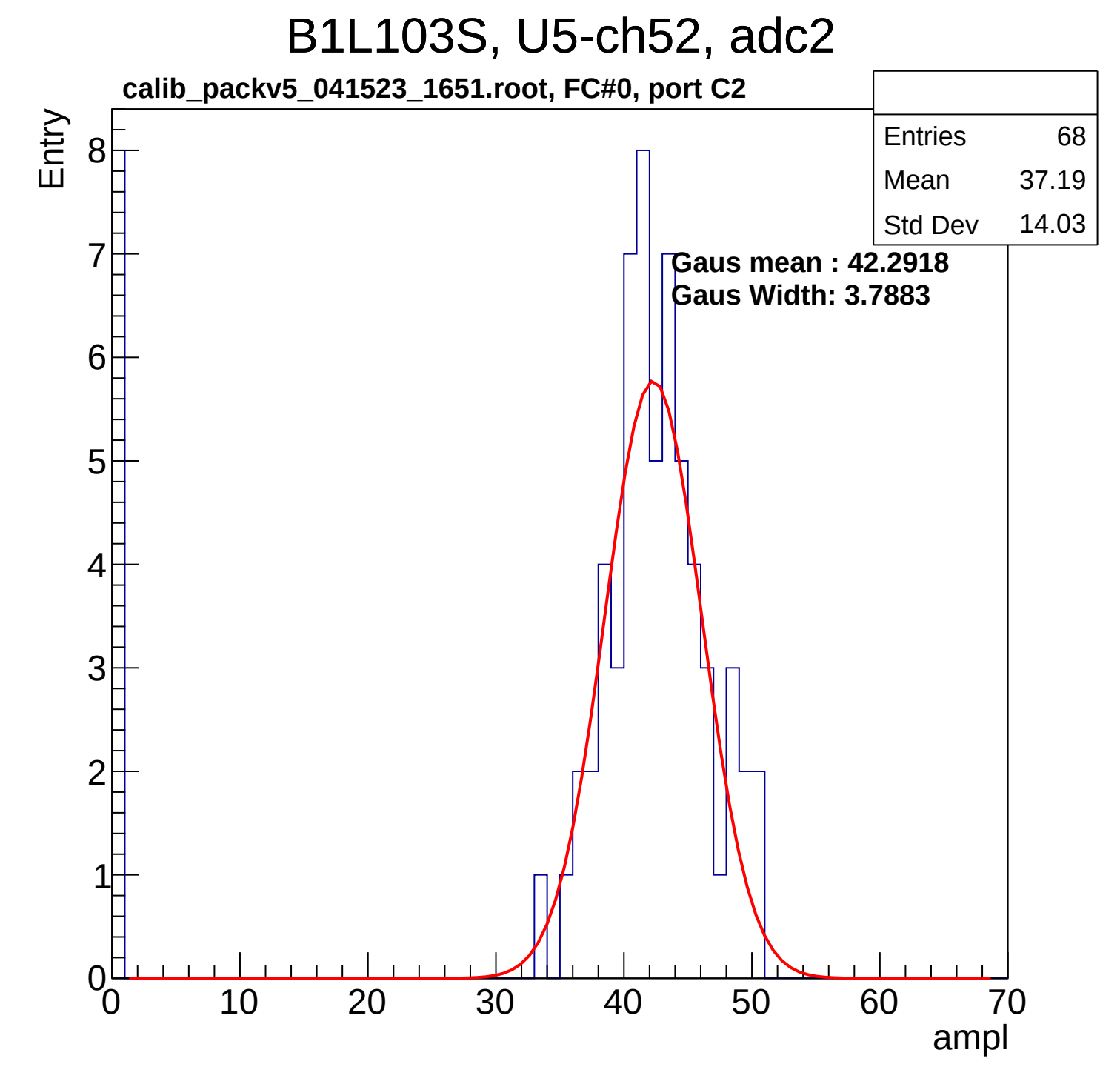
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U5-ch52, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 37.19
Std Dev 14.03
Gaus mean : 42.2918
Gaus Width: 3.7883
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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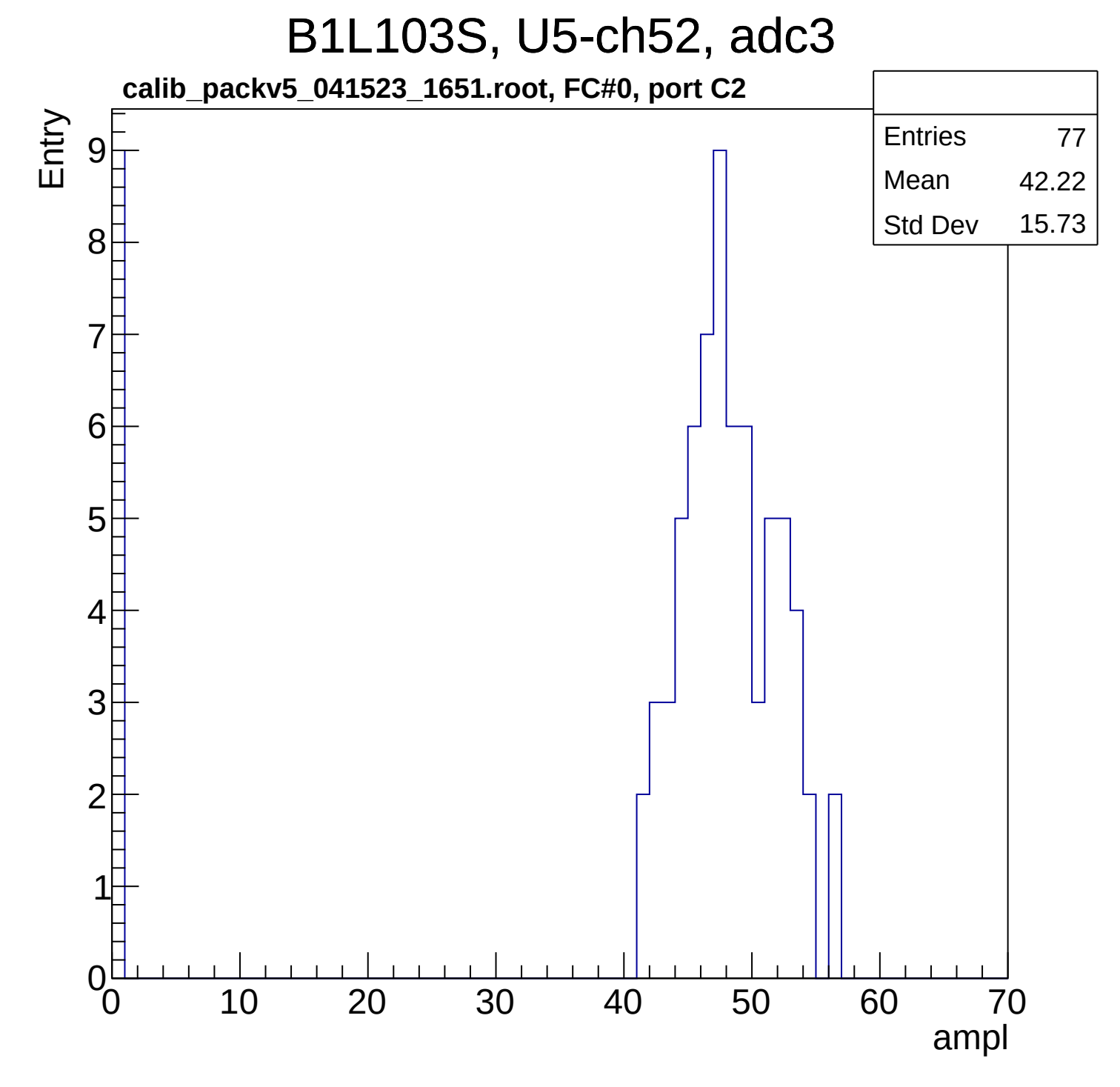
B1L103S, U5-ch52, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 42.22
Std Dev 15.73
Entry
ampl
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3
4
5
6
7
8
9
0
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40
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60
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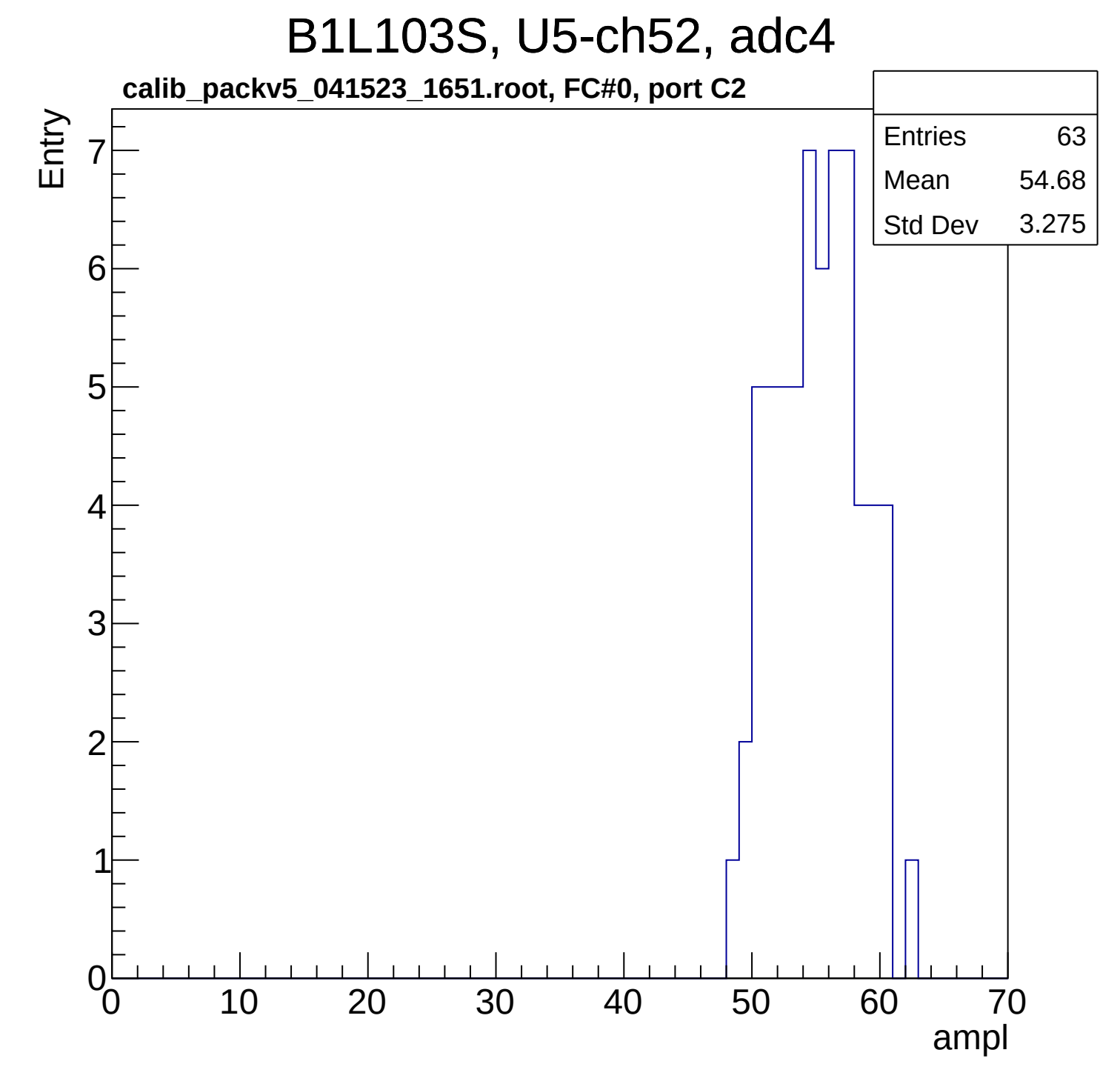
B1L103S, U5-ch52, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 54.68
Std Dev 3.275
Entry
ampl
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3
4
5
6
7
0
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20
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40
50
60
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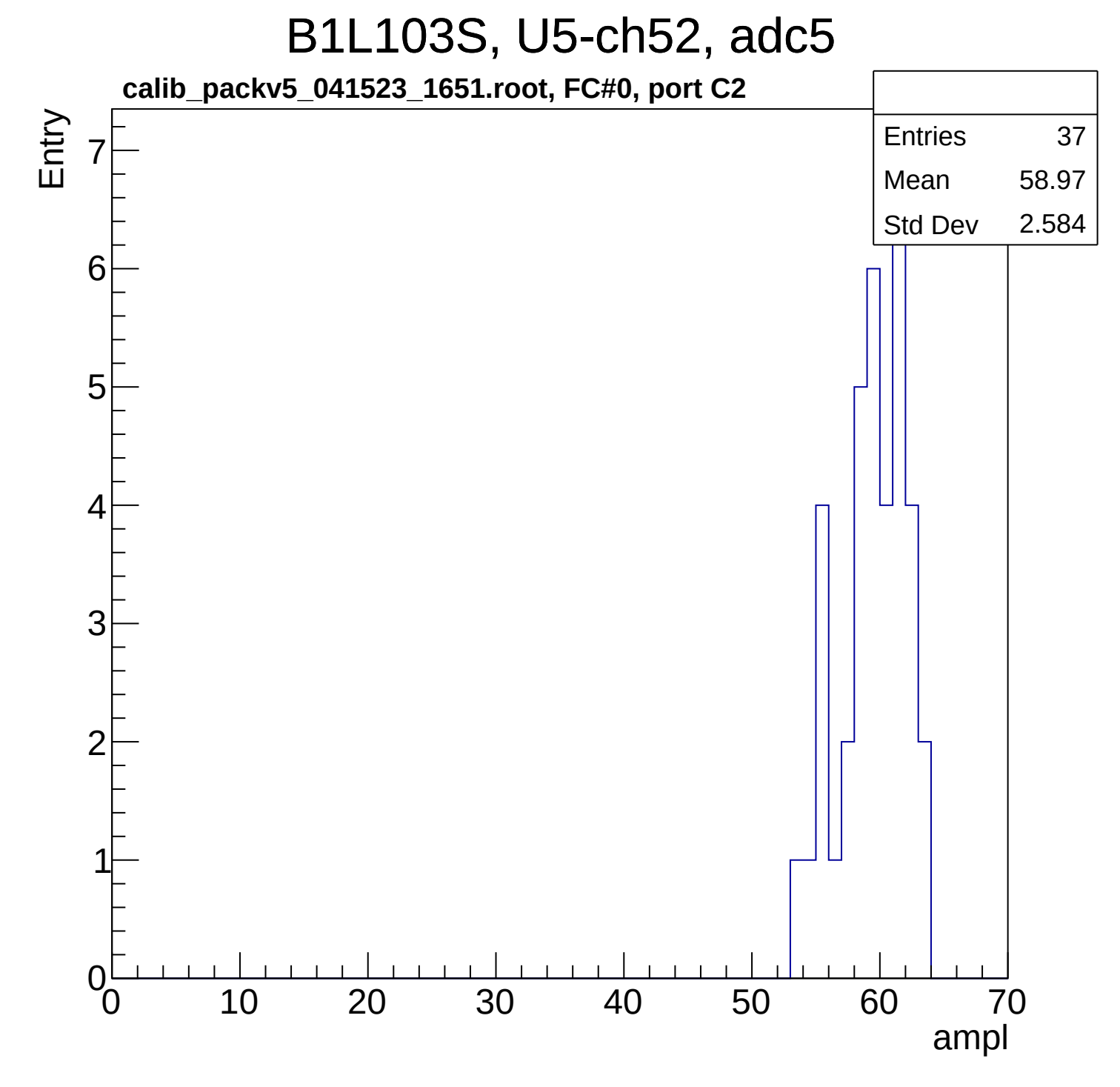
B1L103S, U5-ch52, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 58.97
Std Dev 2.584
Entry
ampl
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3
4
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0
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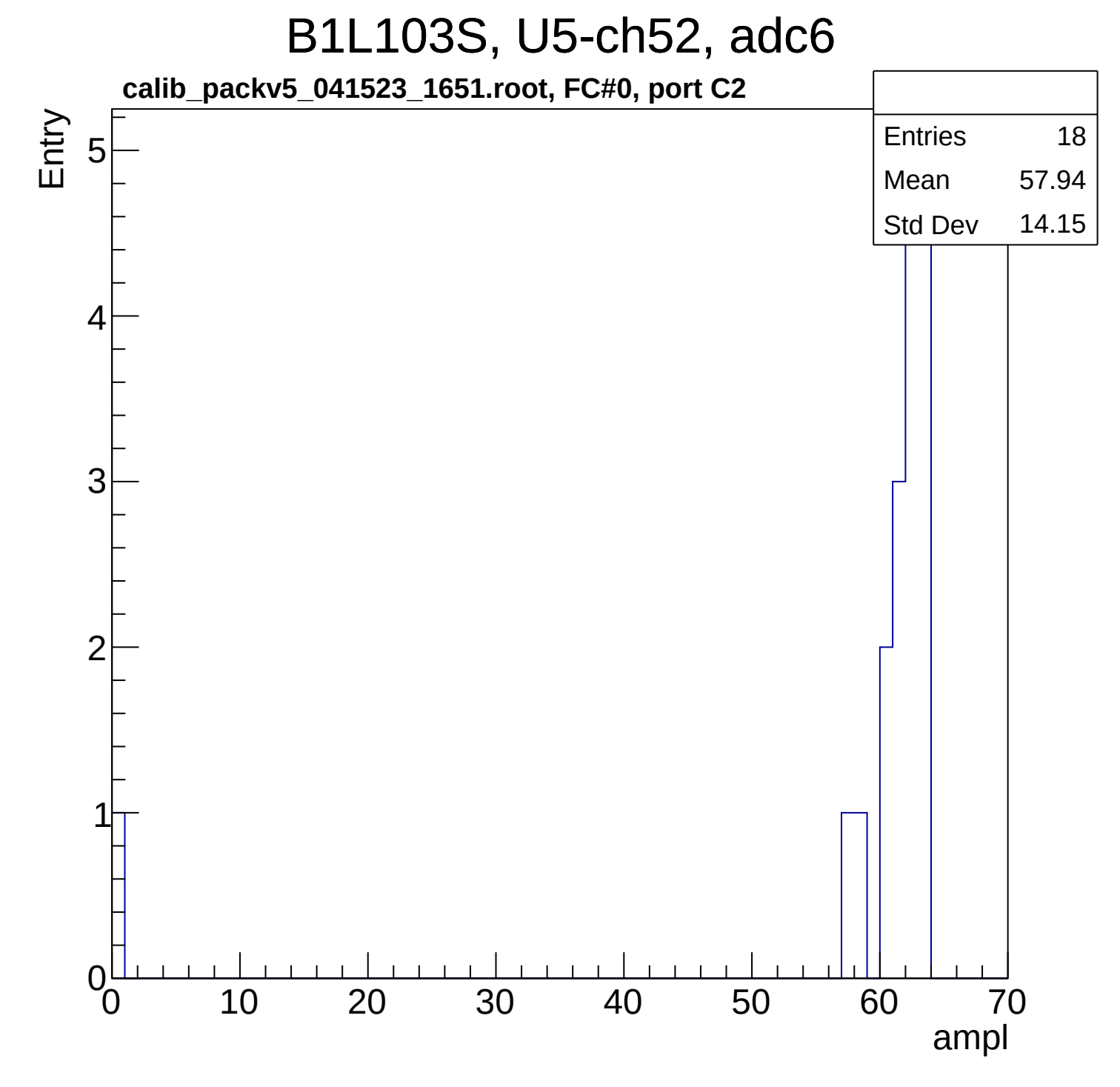
B1L103S, U5-ch52, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 57.94
Std Dev 14.15
Entry
ampl
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2
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0
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40
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60
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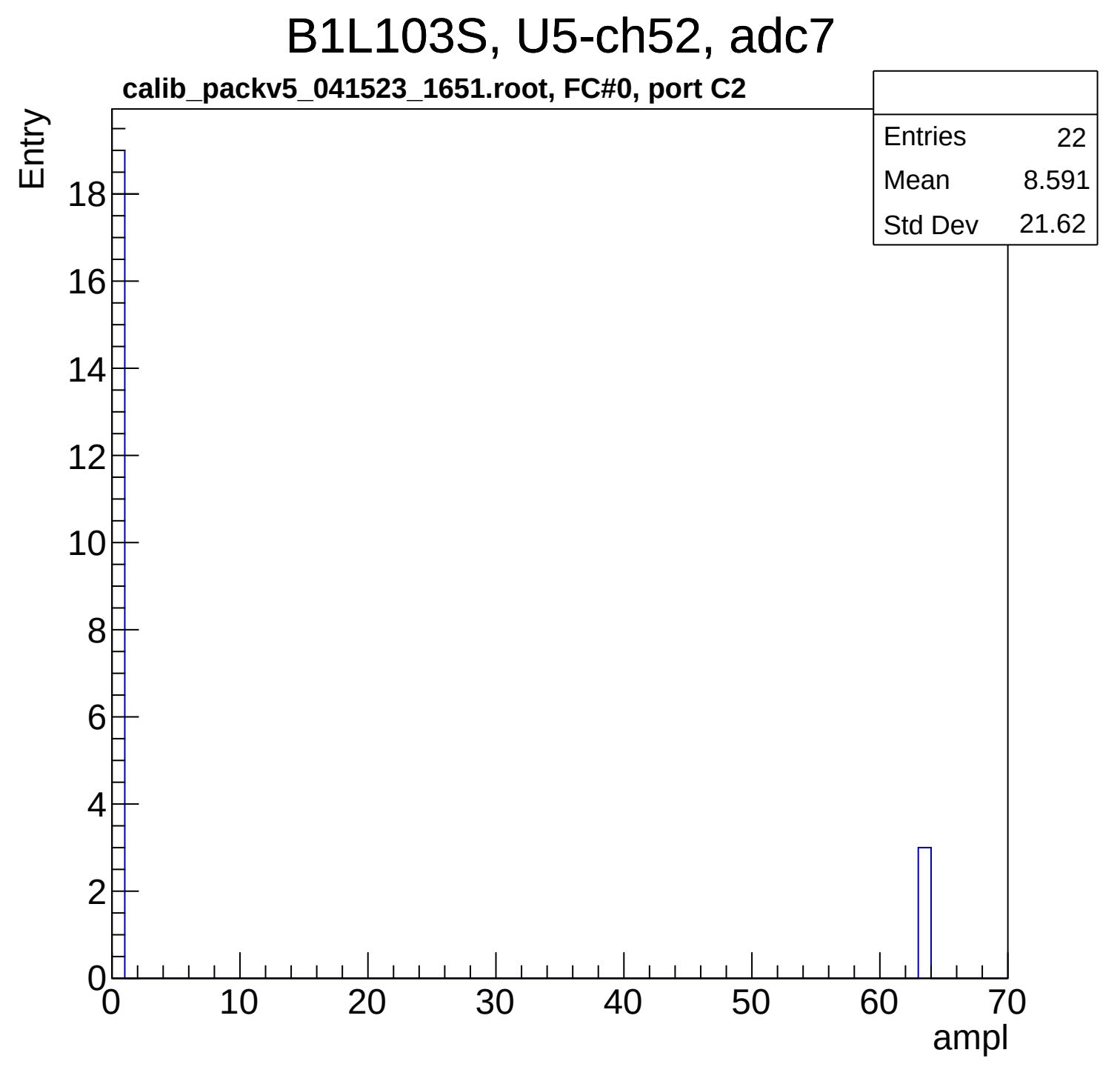
B1L103S, U5-ch52, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.591
Std Dev 21.62
Entry
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8
10
12
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18
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10
20
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50
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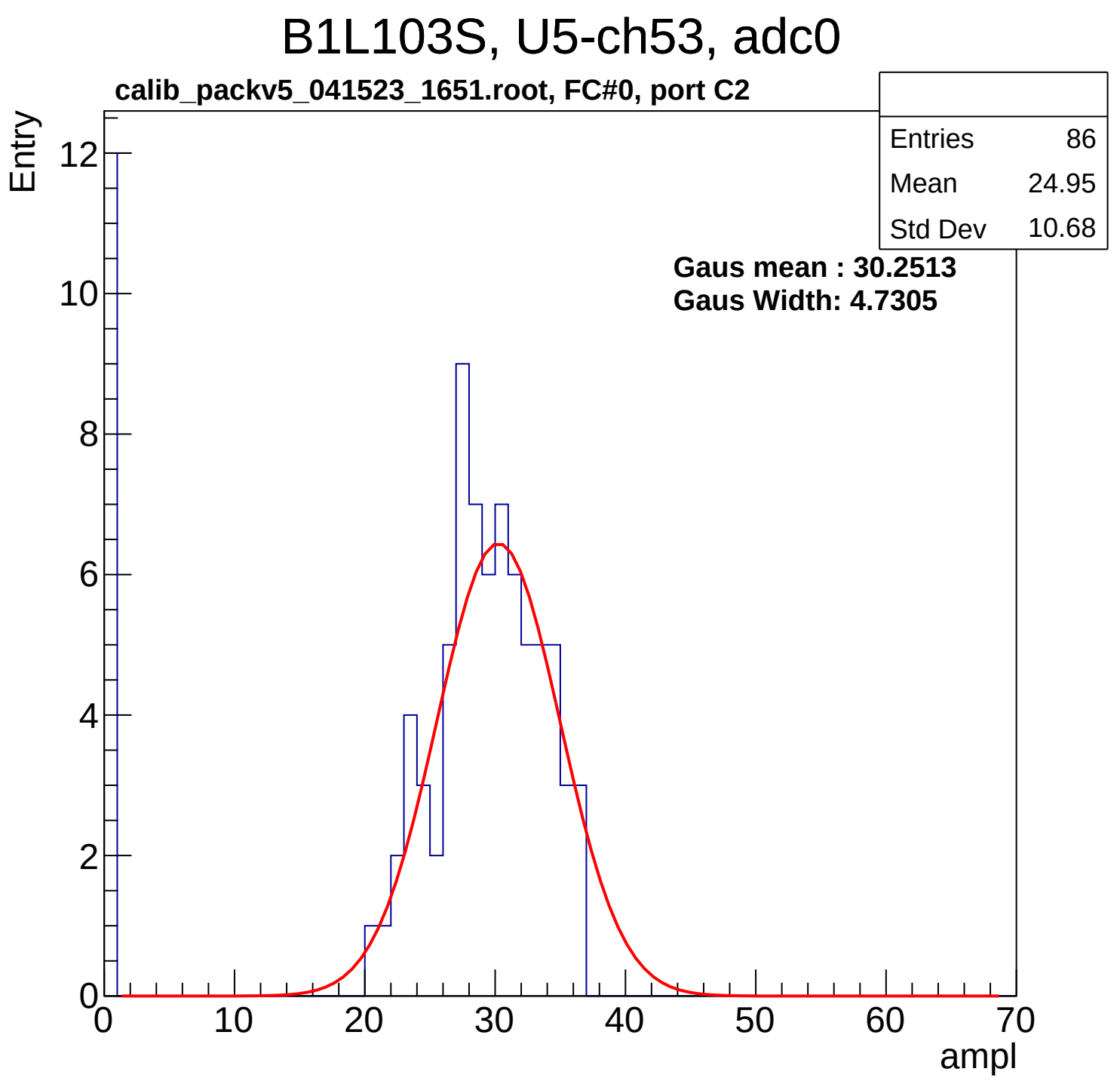
70
ampl


B1L103S, U5-ch53, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 24.95
Std Dev 10.68
Gaus mean : 30.2513
Gaus Width: 4.7305
Entry
ampl
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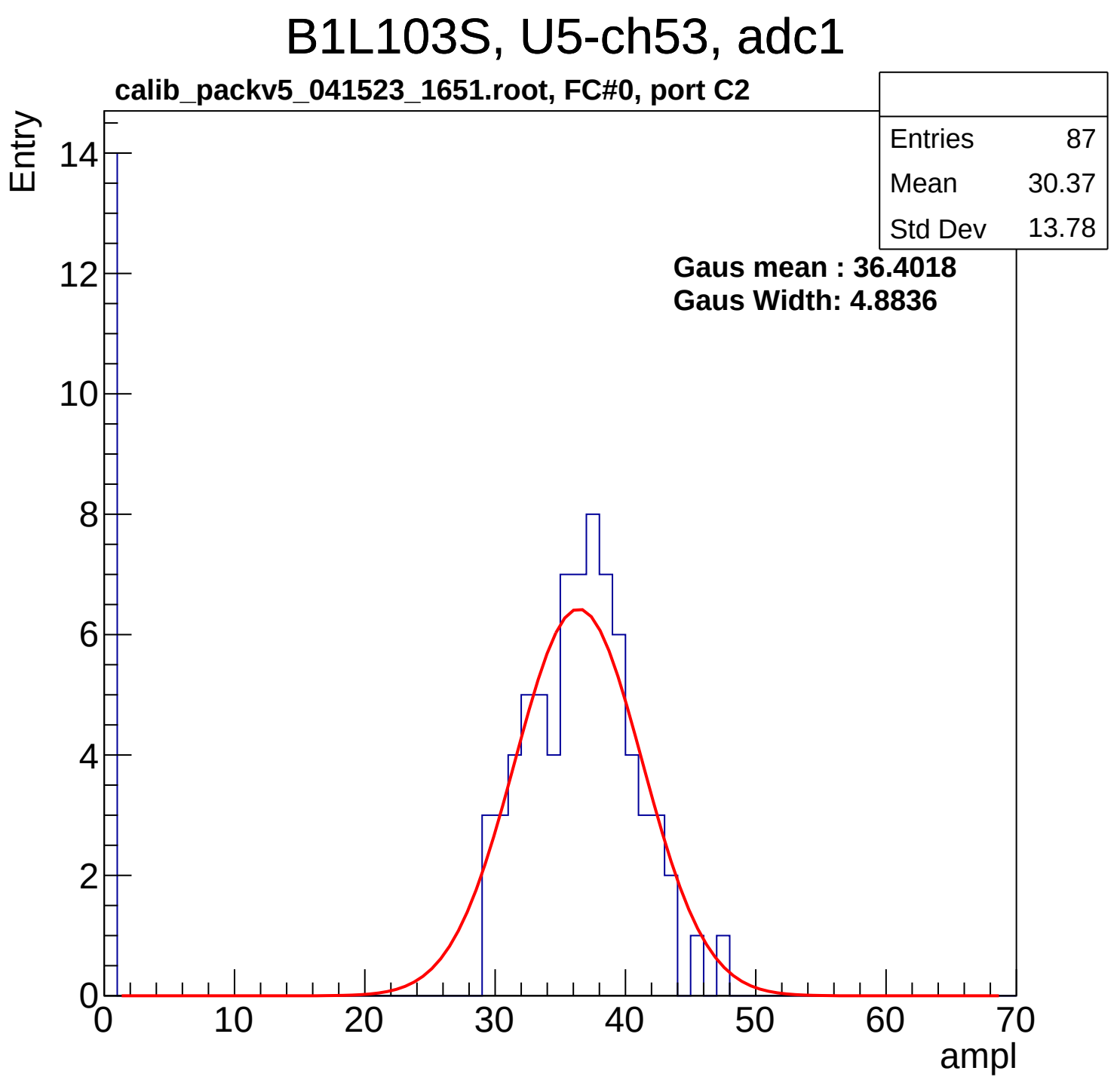
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U5-ch53, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 30.37
Std Dev 13.78
Gaus mean : 36.4018
Gaus Width: 4.8836
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
50
60
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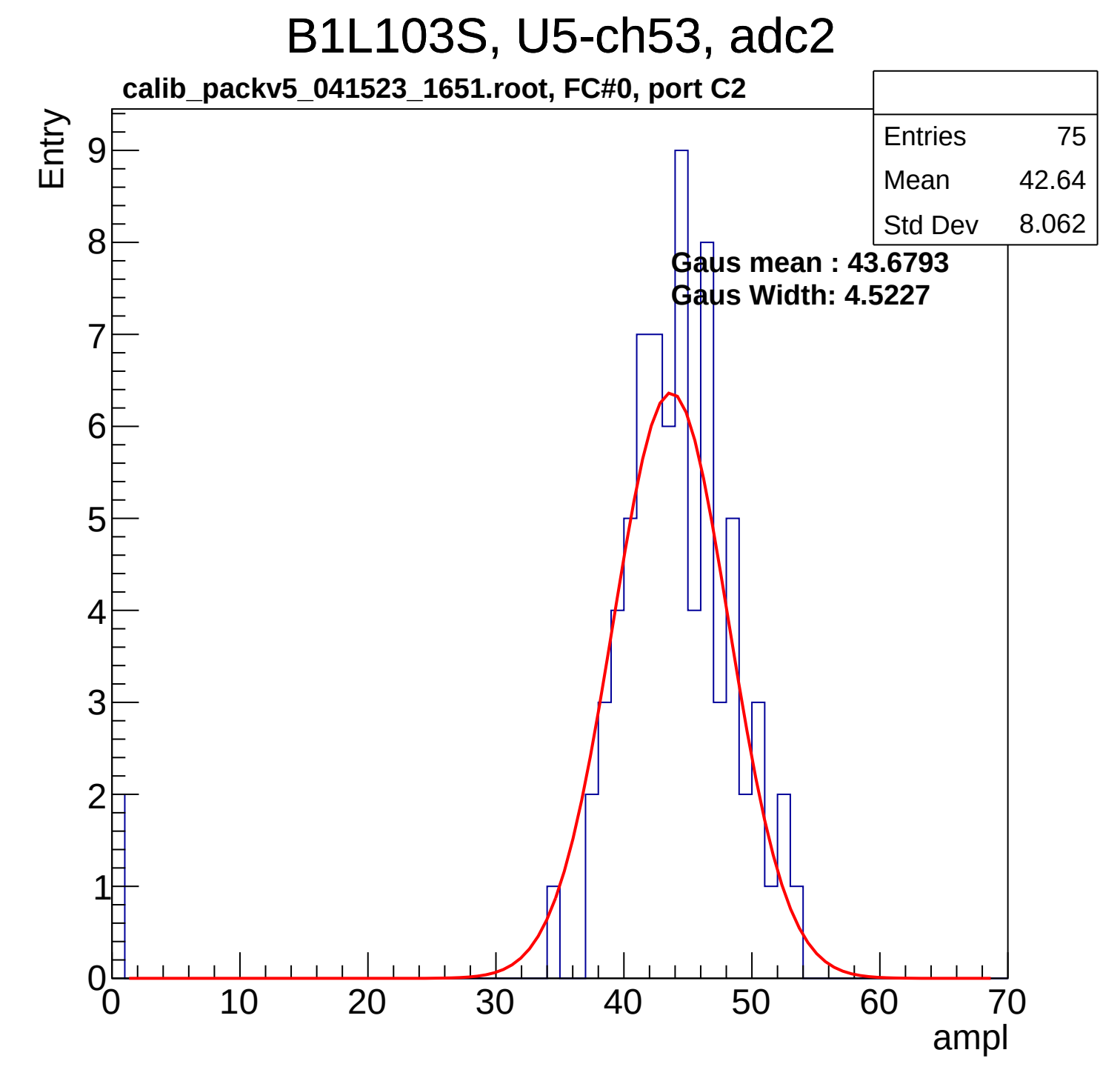
B1L103S, U5-ch53, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 42.64
Std Dev 8.062
Gaus mean : 43.6793
Gaus Width: 4.5227
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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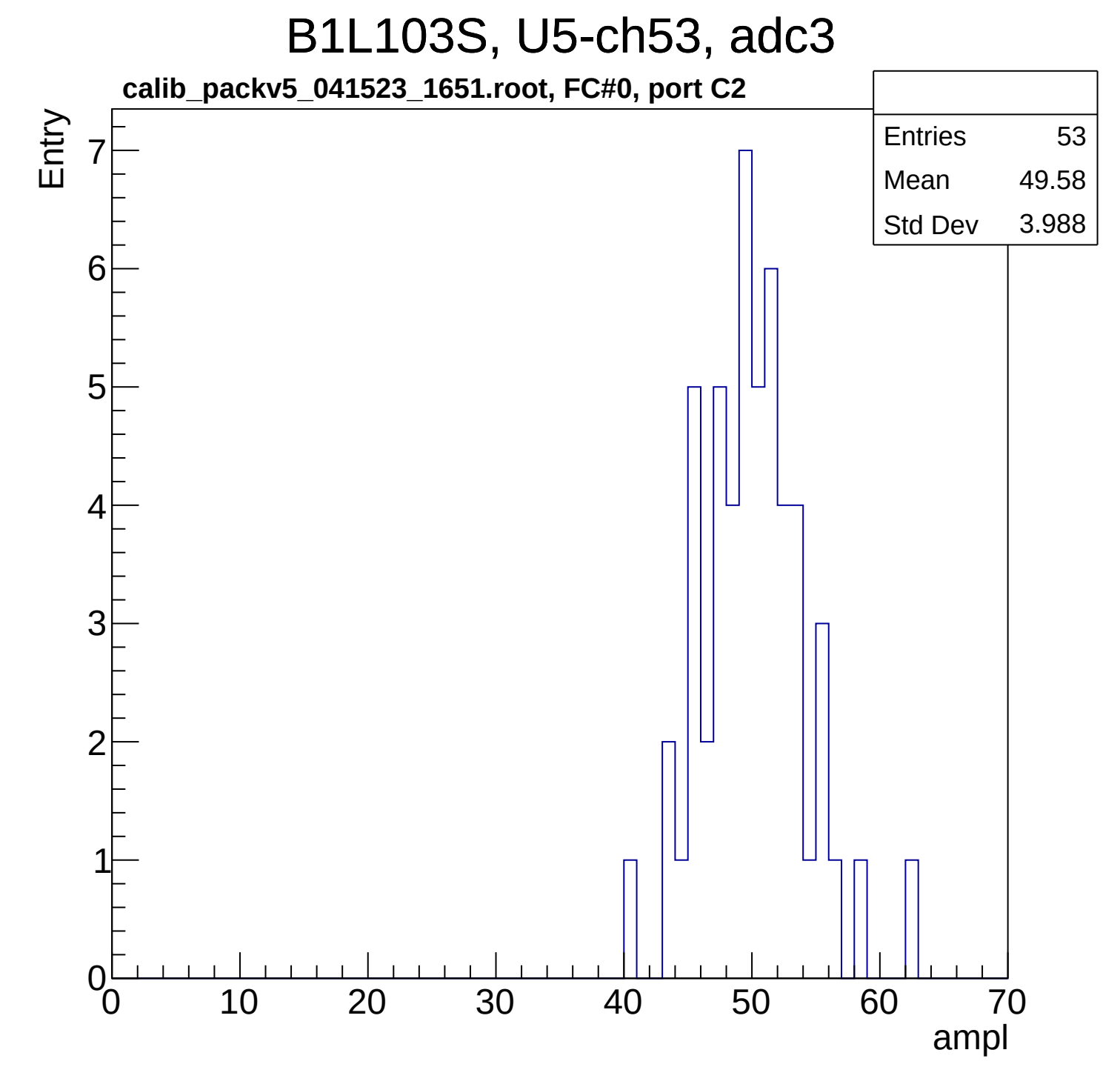
B1L103S, U5-ch53, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 49.58
Std Dev 3.988
Entry
ampl
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4
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6
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0
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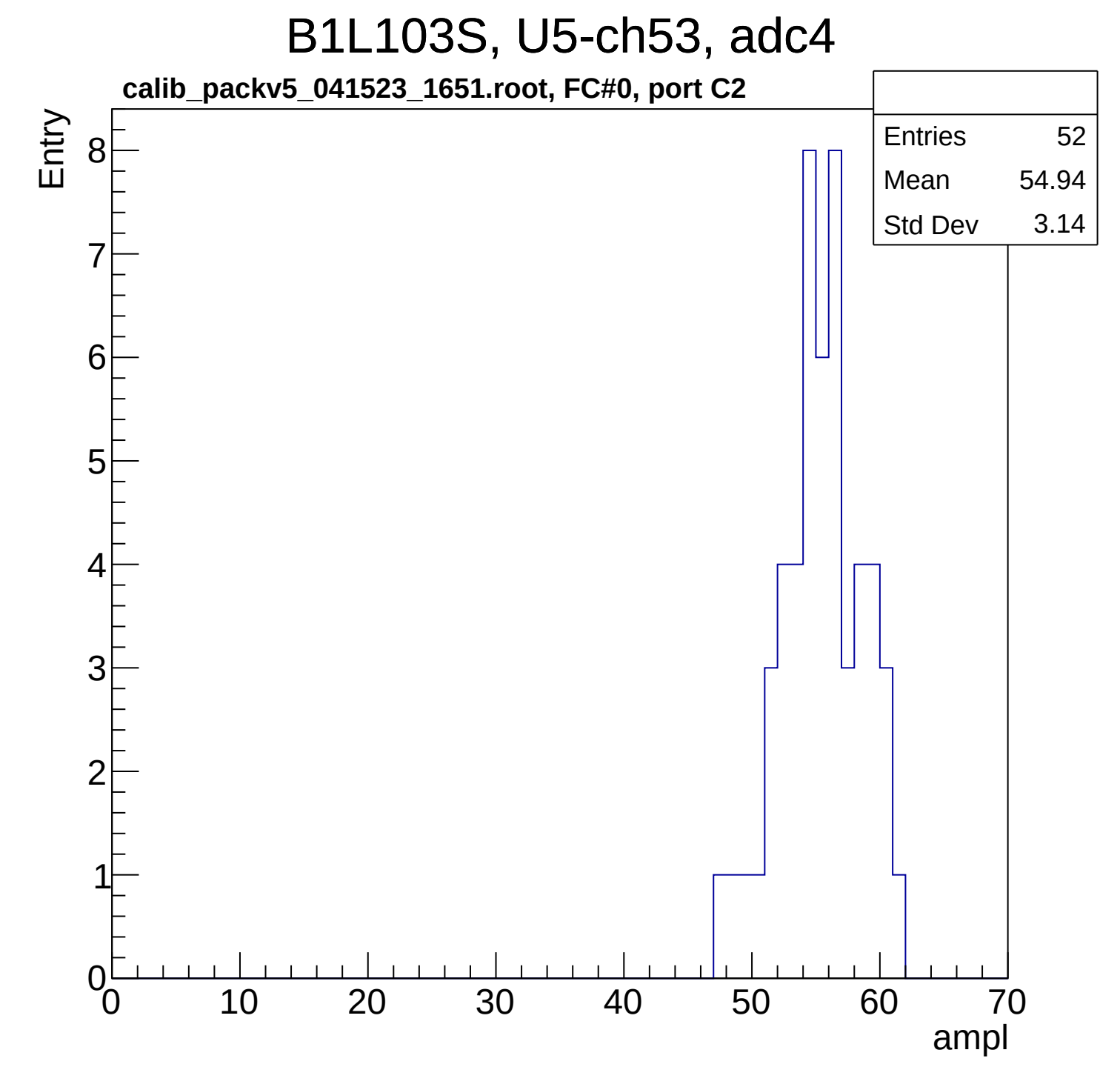
B1L103S, U5-ch53, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 54.94
Std Dev 3.14
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
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60
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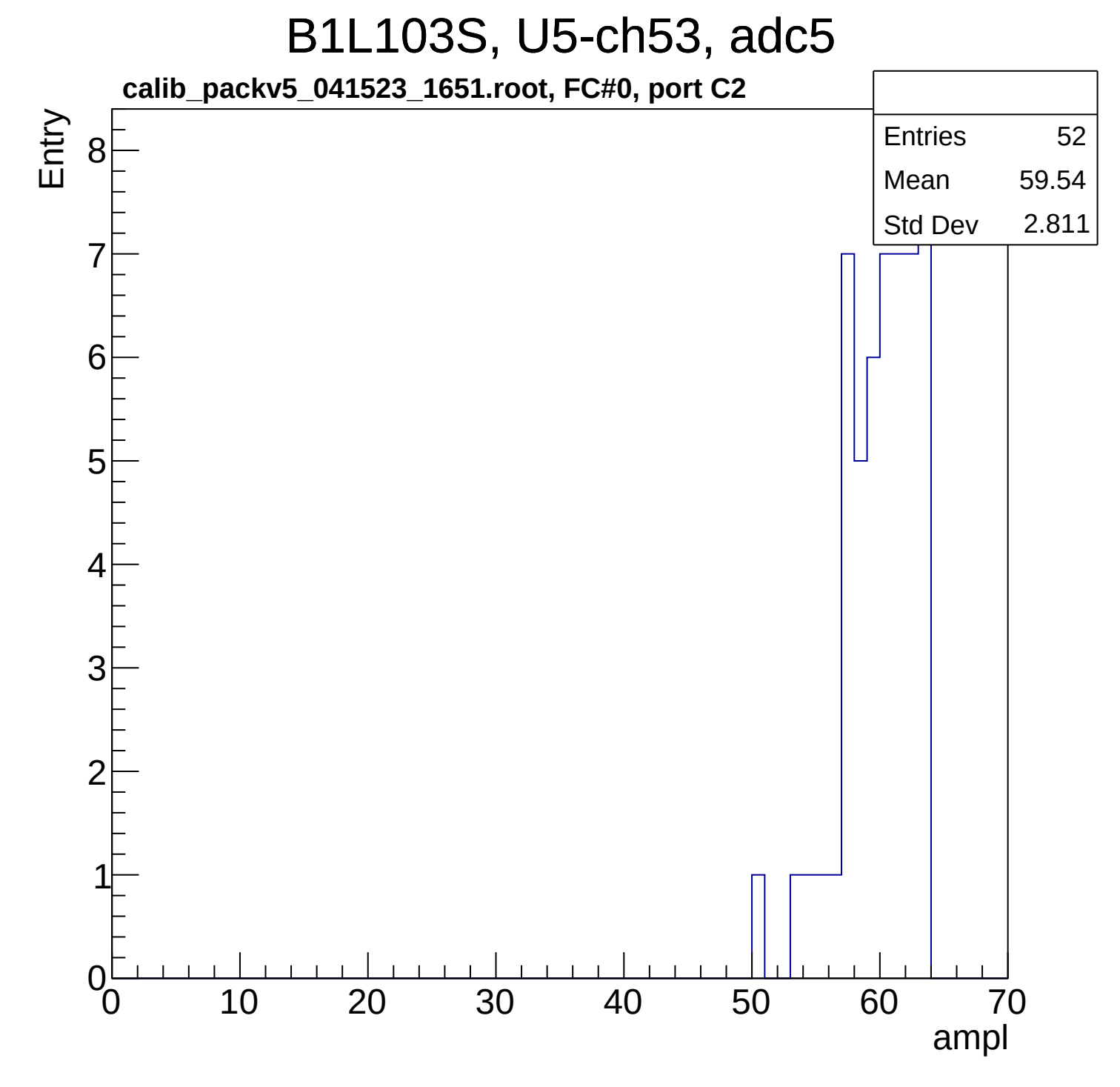
B1L103S, U5-ch53, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 59.54
Std Dev 2.811
Entry
ampl
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3
4
5
6
7
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0
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60
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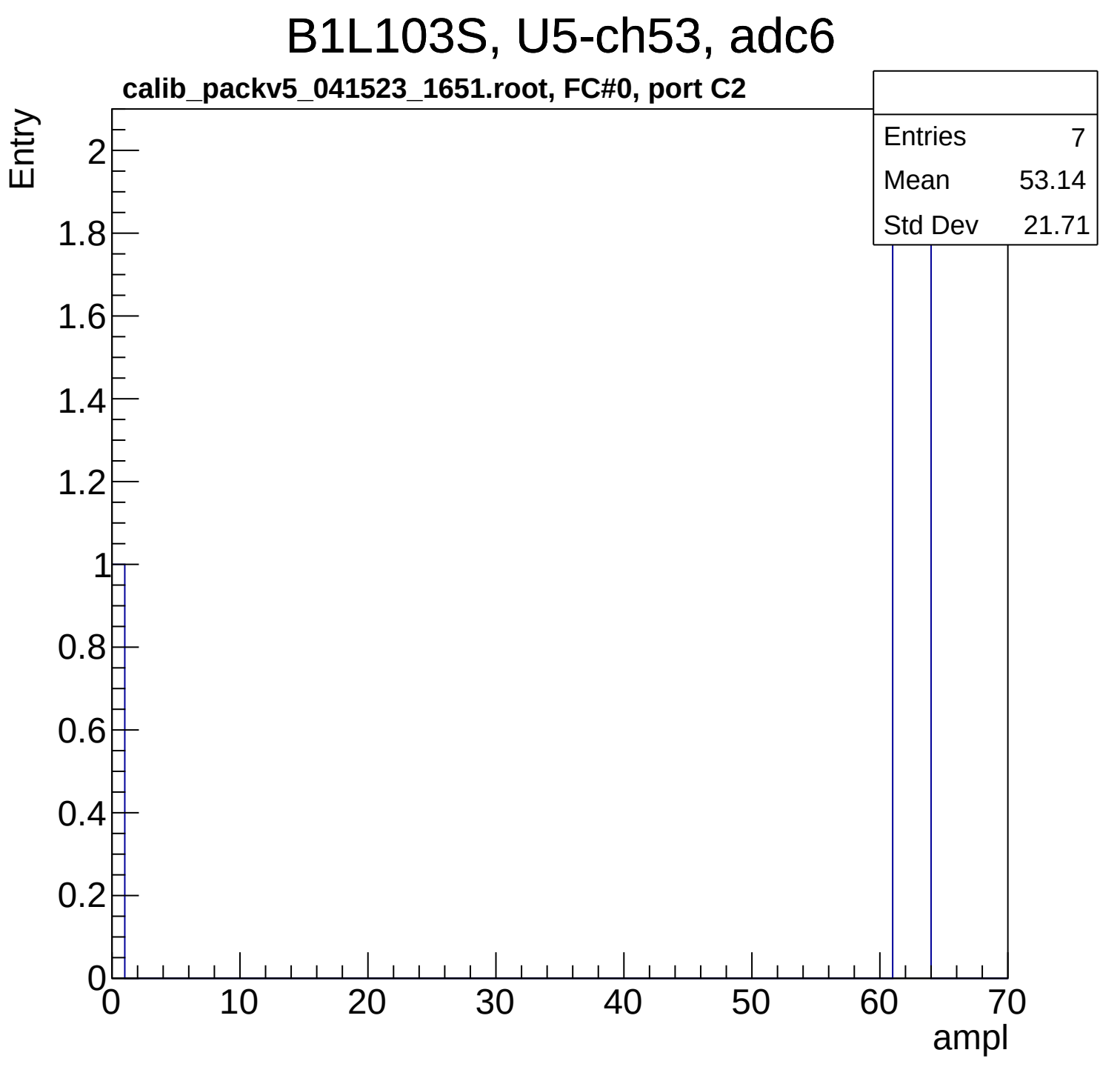
B1L103S, U5-ch53, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 53.14
Std Dev 21.71
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
50
60
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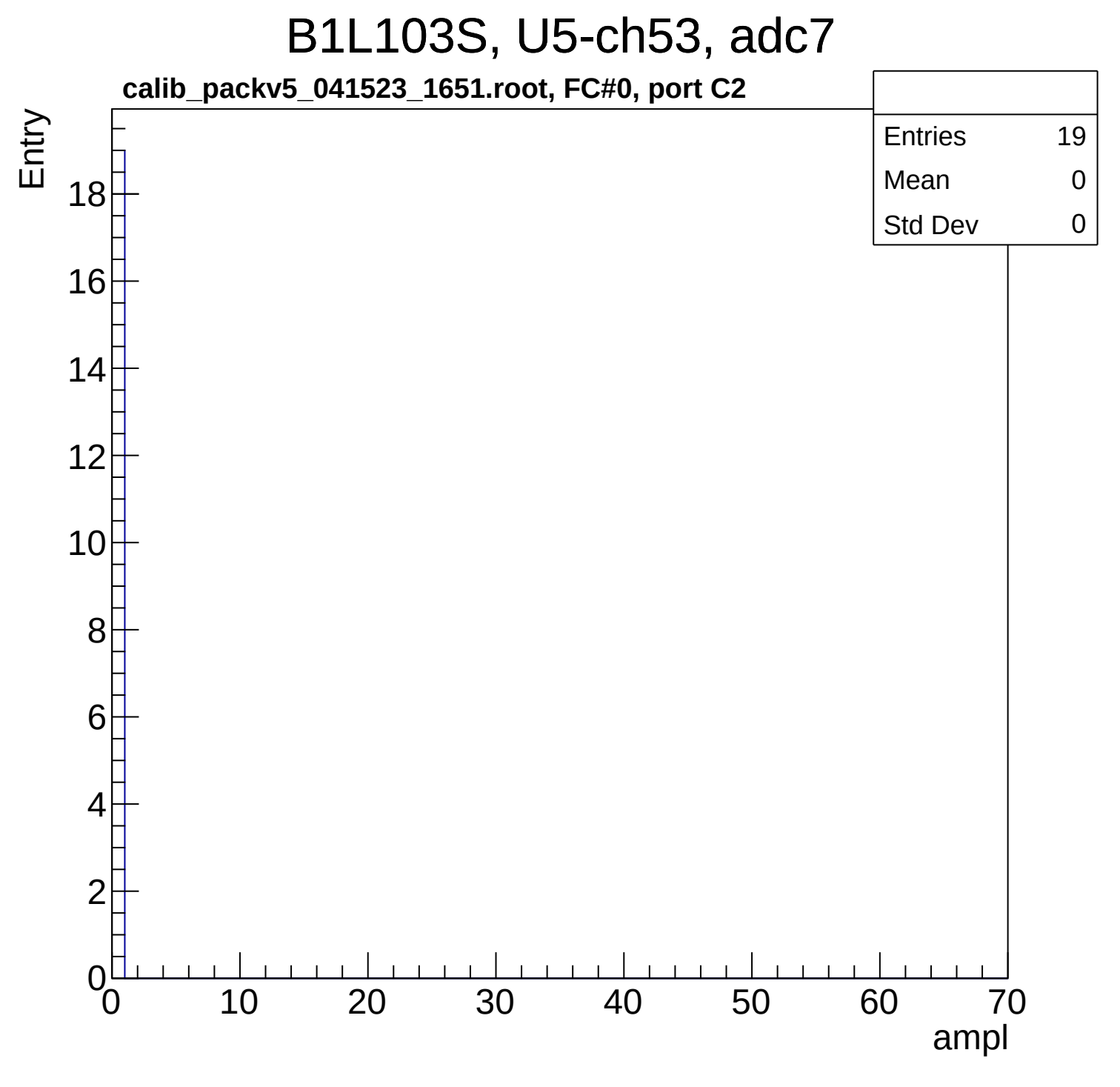
B1L103S, U5-ch53, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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18
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30
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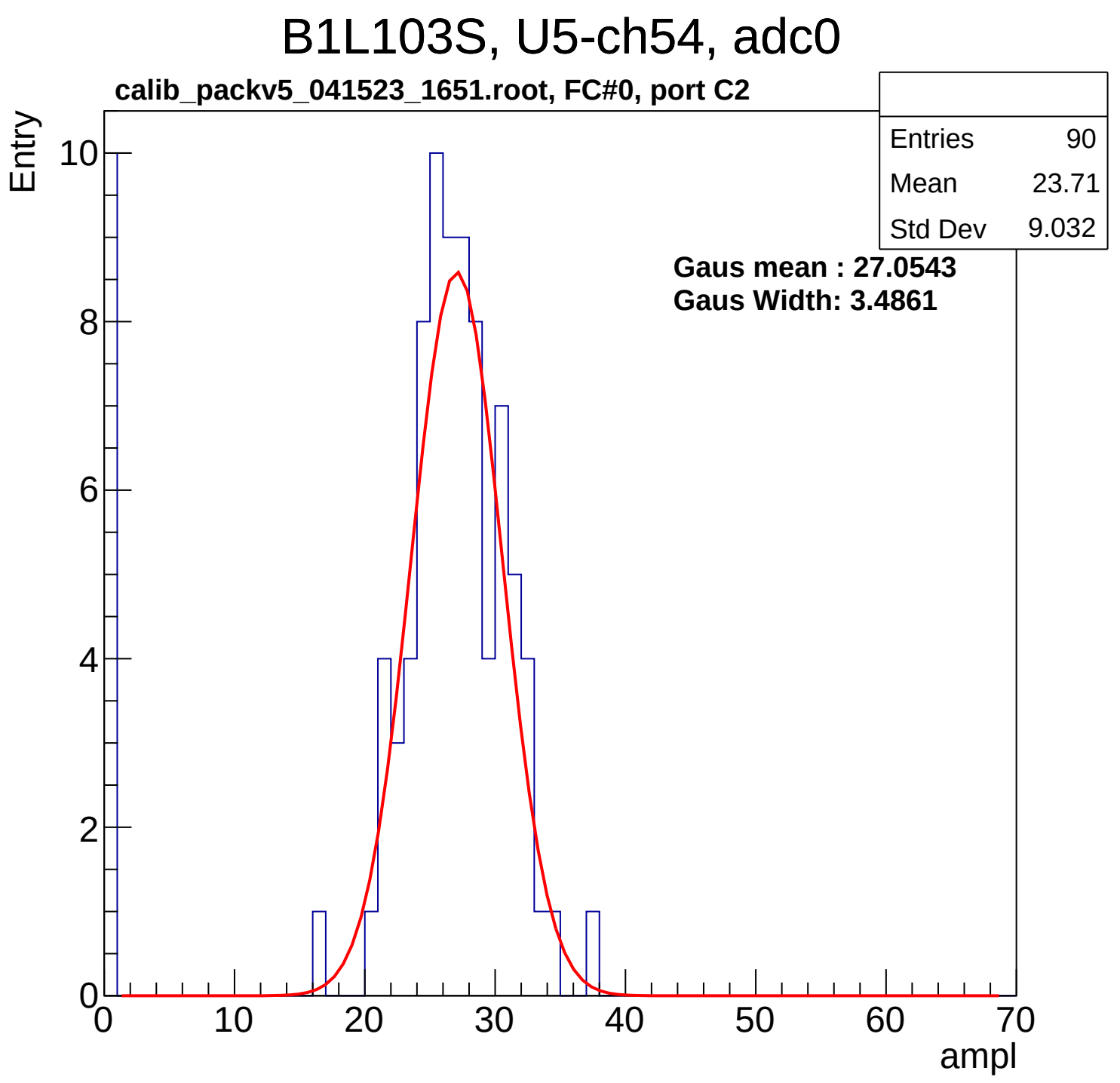
50
60
70
ampl


B1L103S, U5-ch54, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 23.71
Std Dev 9.032
Gaus mean : 27.0543
Gaus Width: 3.4861
Entry
ampl
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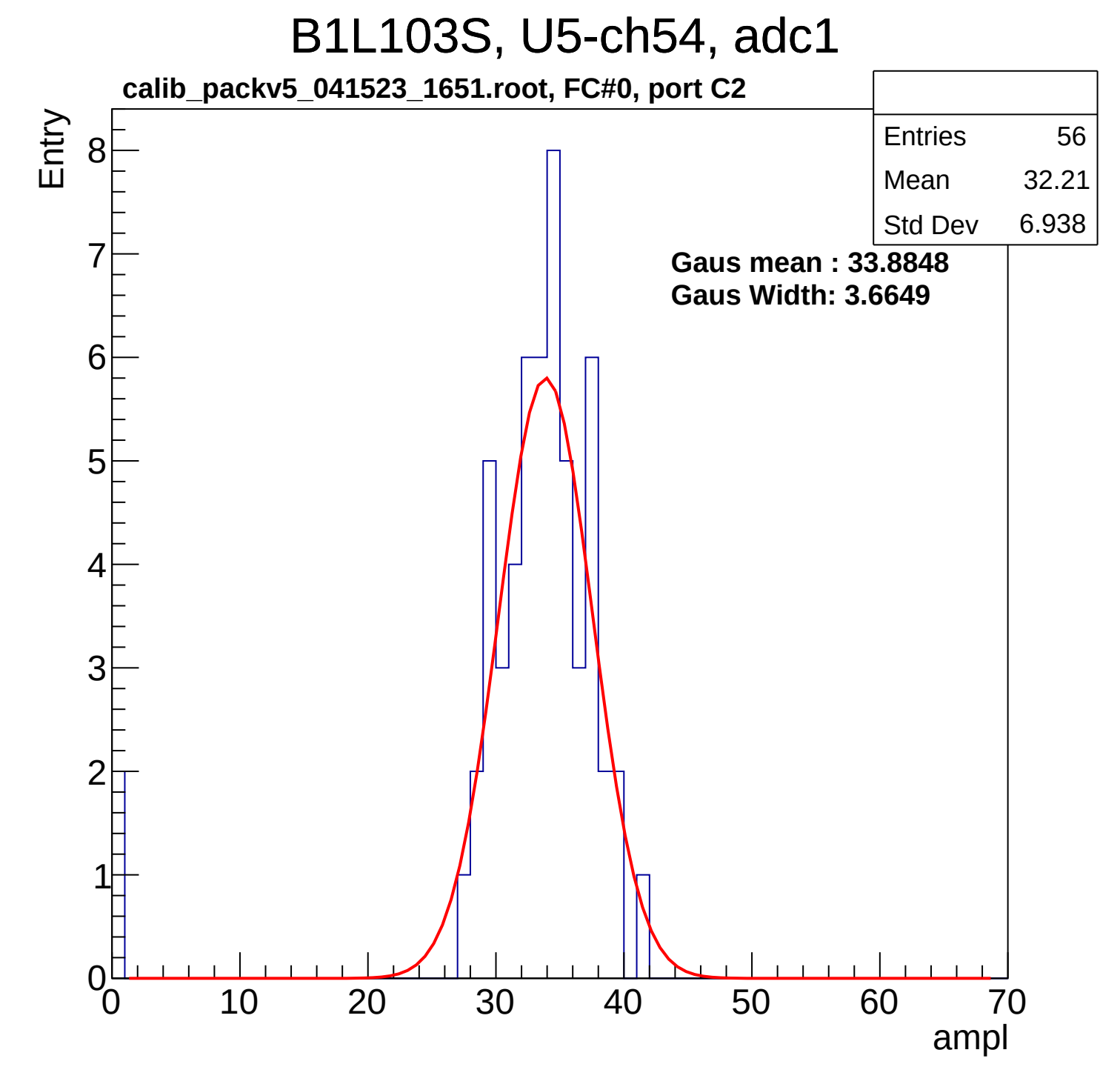
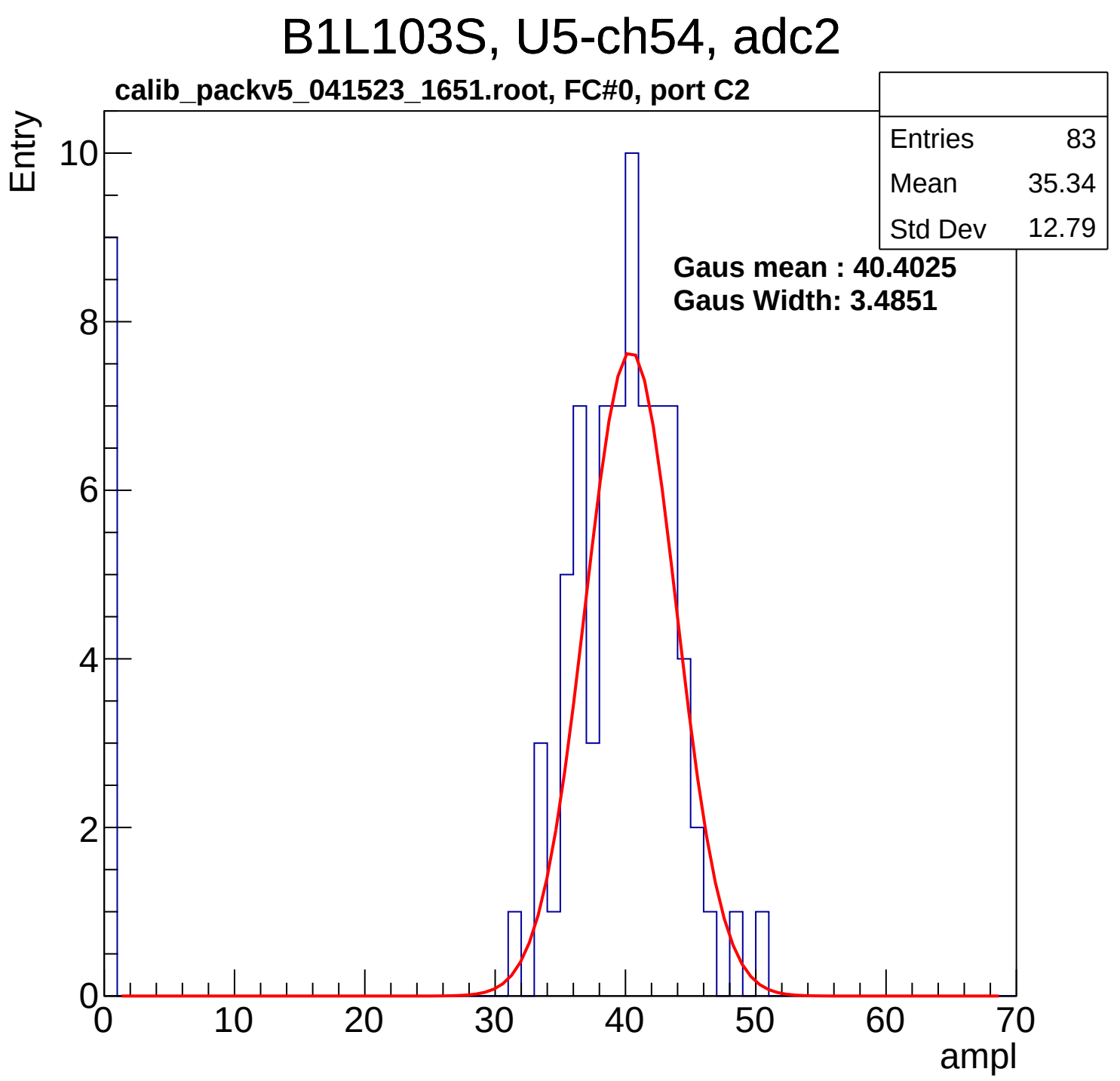
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U5-ch54, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 32.21
Std Dev 6.938
Gaus mean : 33.8848
Gaus Width: 3.6649
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U5-ch54, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 35.34
Std Dev 12.79
Gaus mean : 40.4025
Gaus Width: 3.4851
Entry
ampl
0
2
4
6
8
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0
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20
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40
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60
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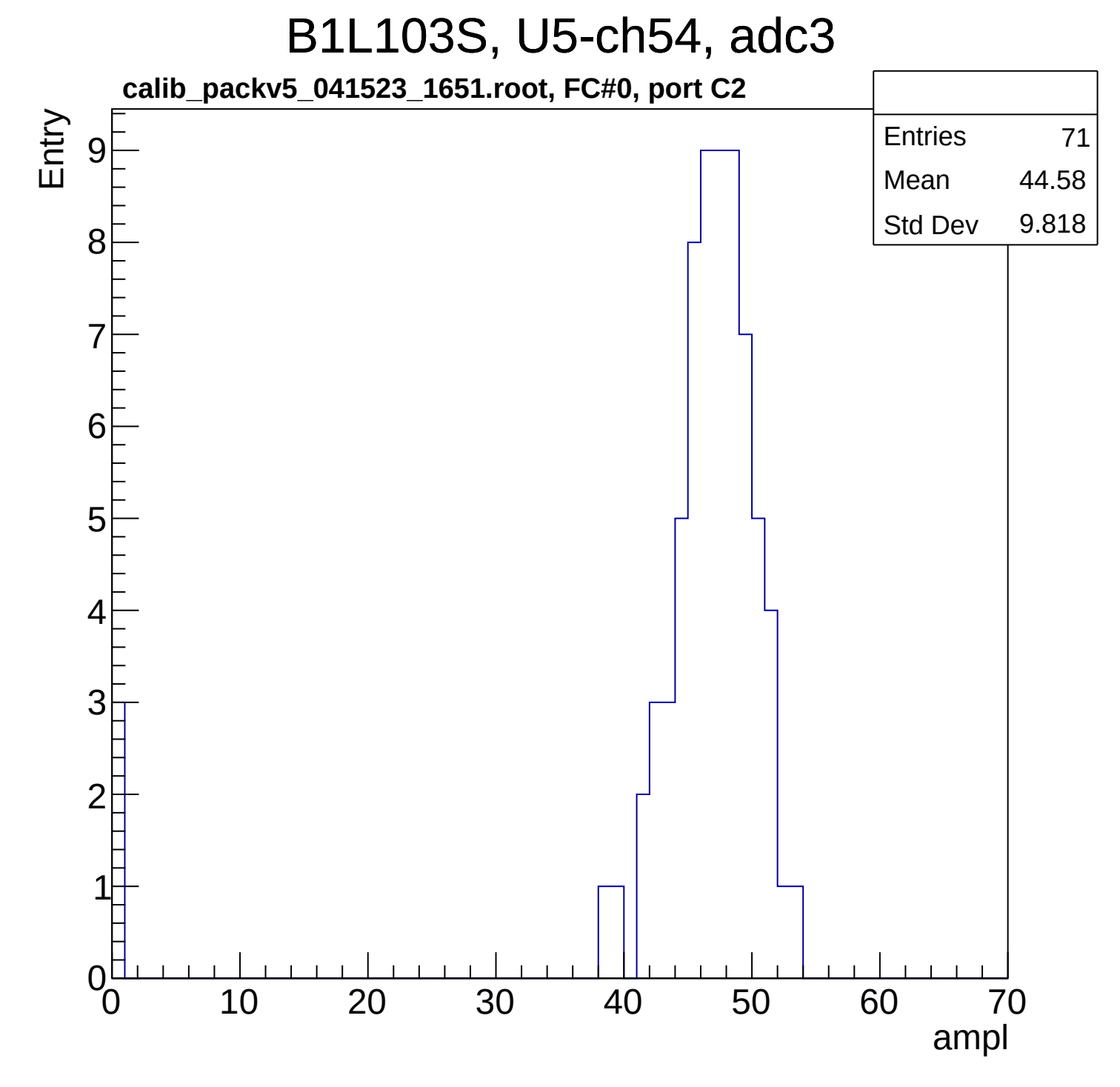
B1L103S, U5-ch54, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 44.58
Std Dev 9.818
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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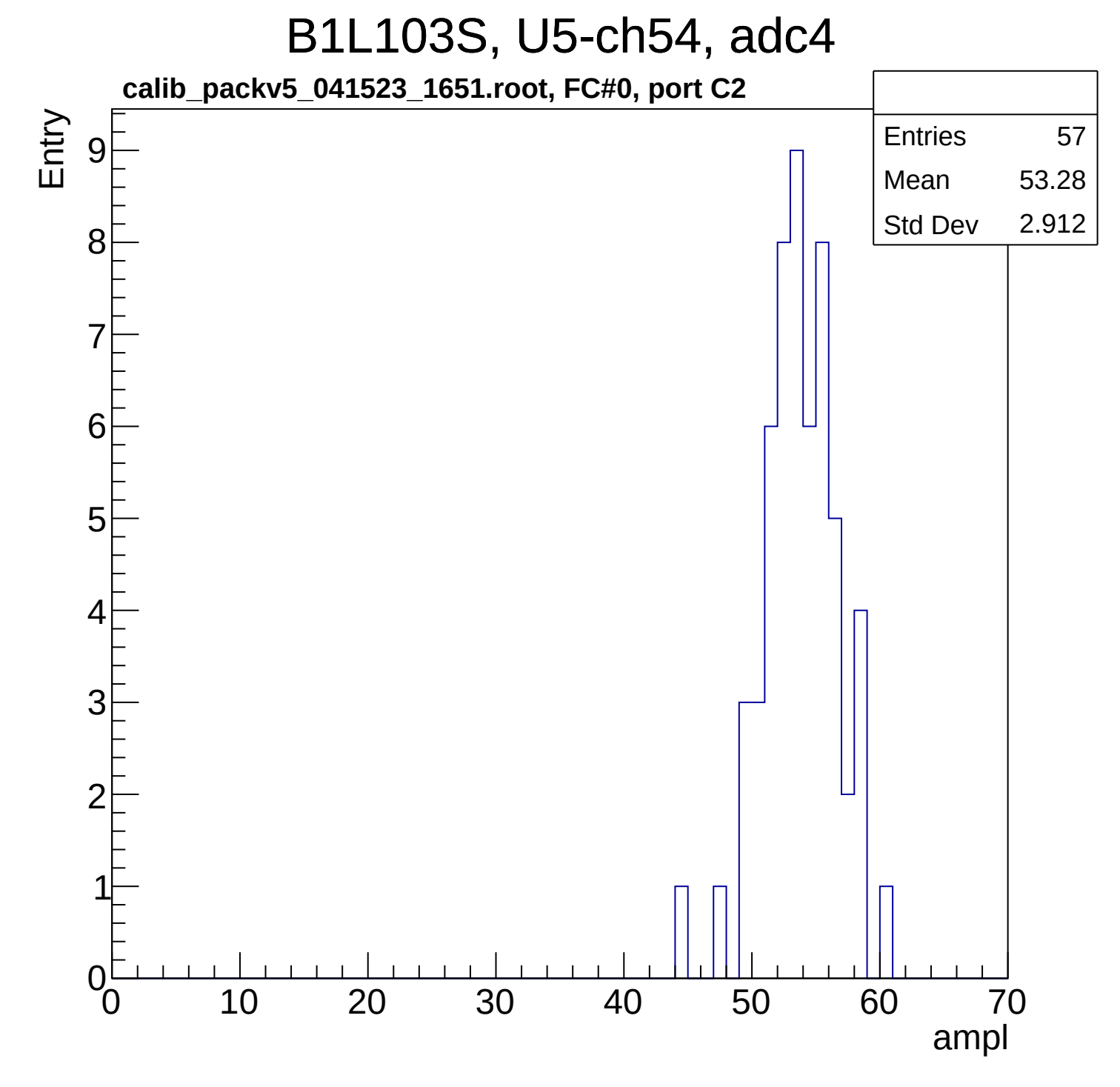
B1L103S, U5-ch54, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 53.28
Std Dev 2.912
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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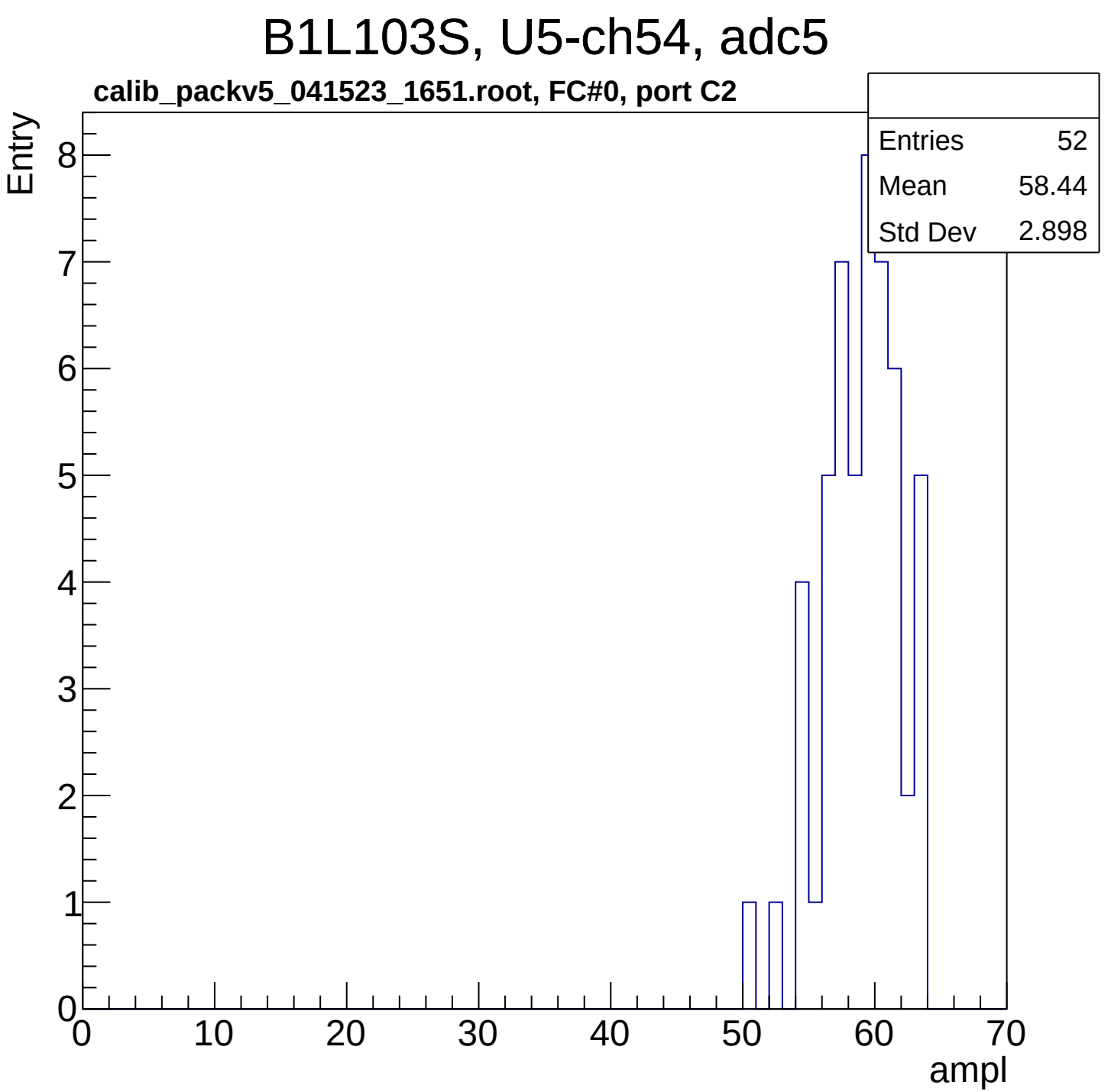
B1L103S, U5-ch54, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.44
Std Dev 2.898
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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30
40
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60
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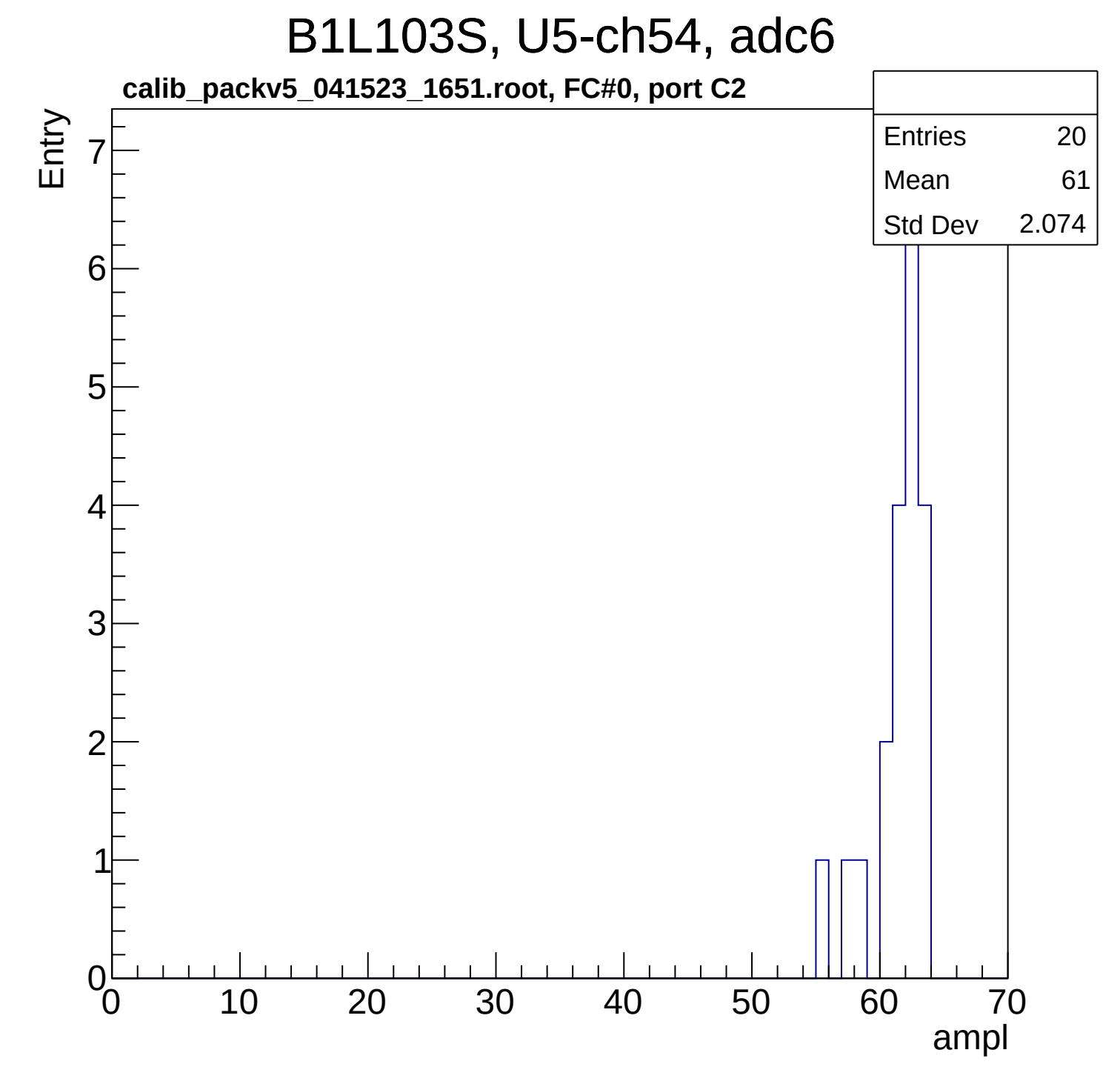
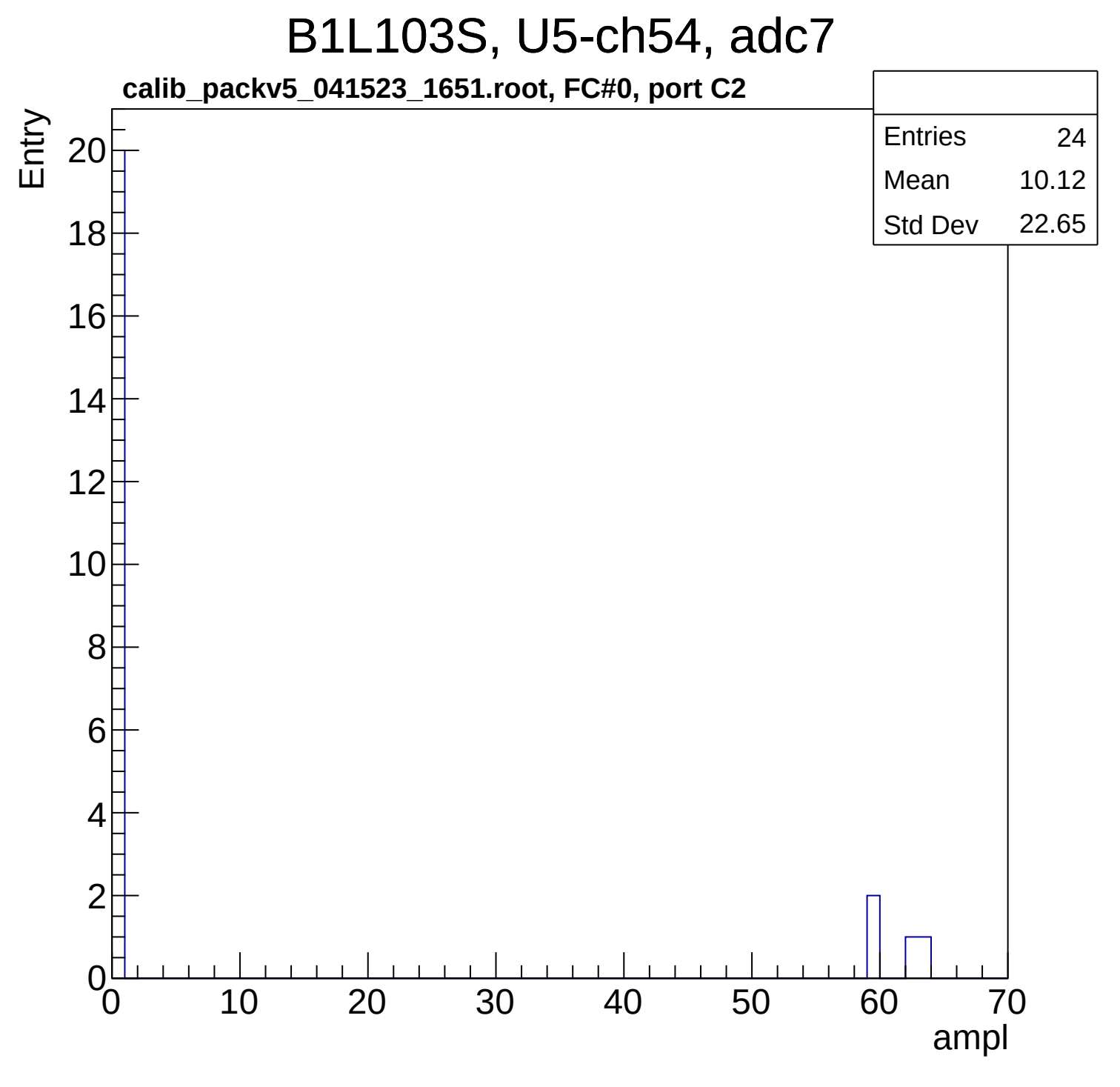

B1L103S, U5-ch54, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 61
Std Dev 2.074
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U5-ch54, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 10.12
Std Dev 22.65
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
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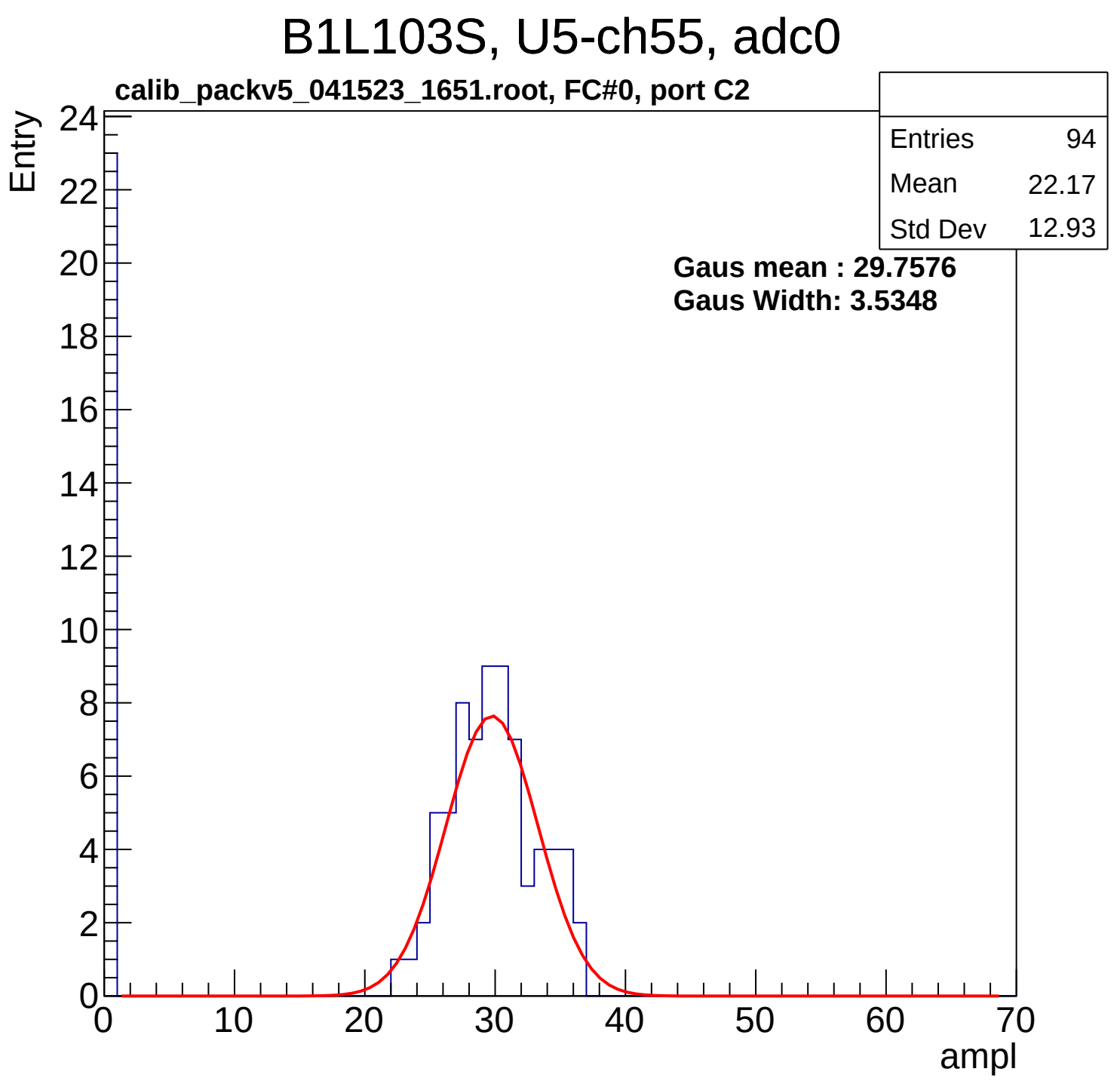
B1L103S, U5-ch55, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 22.17
Std Dev 12.93
Gaus mean : 29.7576
Gaus Width: 3.5348
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
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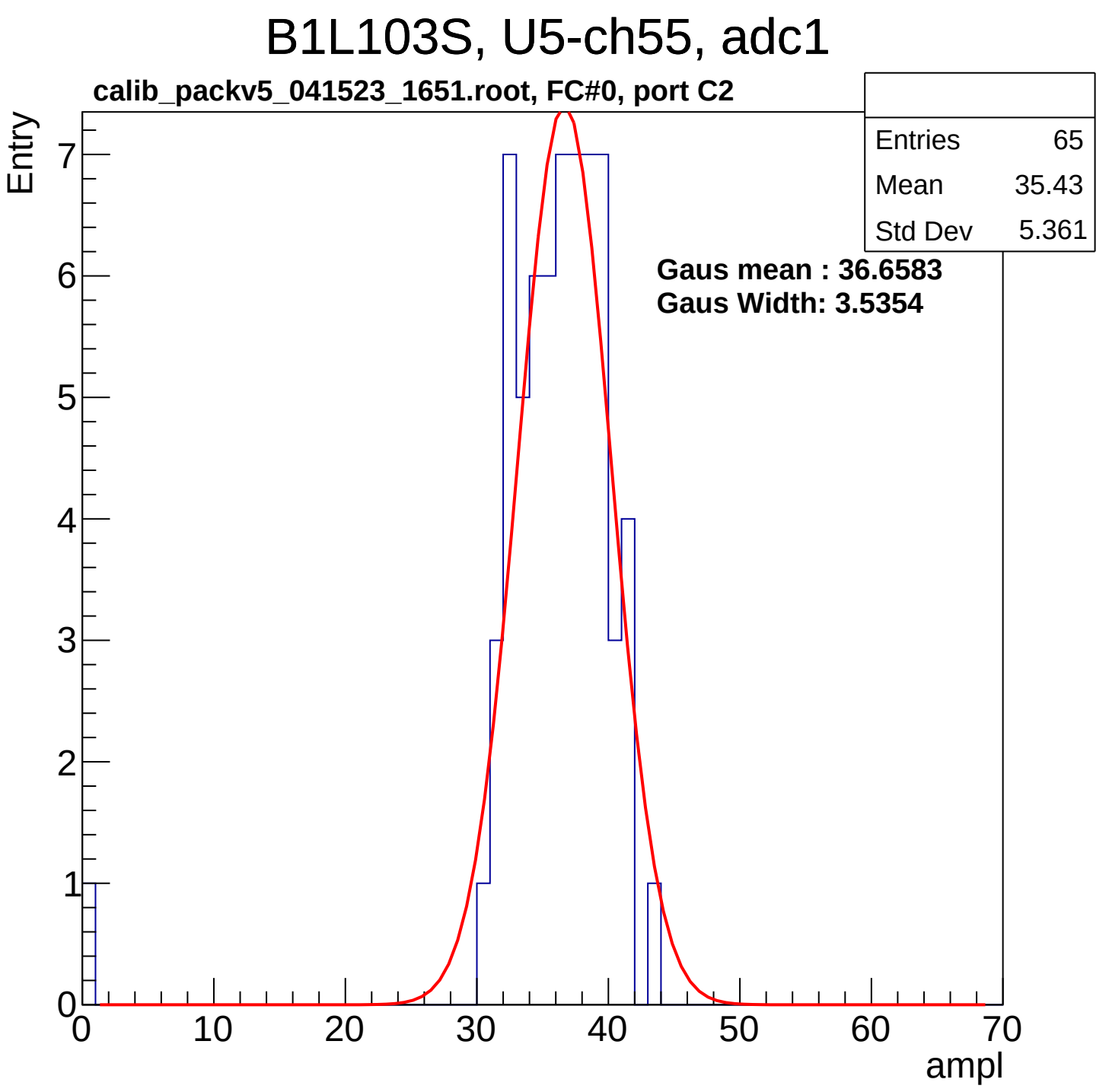
B1L103S, U5-ch55, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 35.43
Std Dev 5.361
Gaus mean : 36.6583
Gaus Width: 3.5354
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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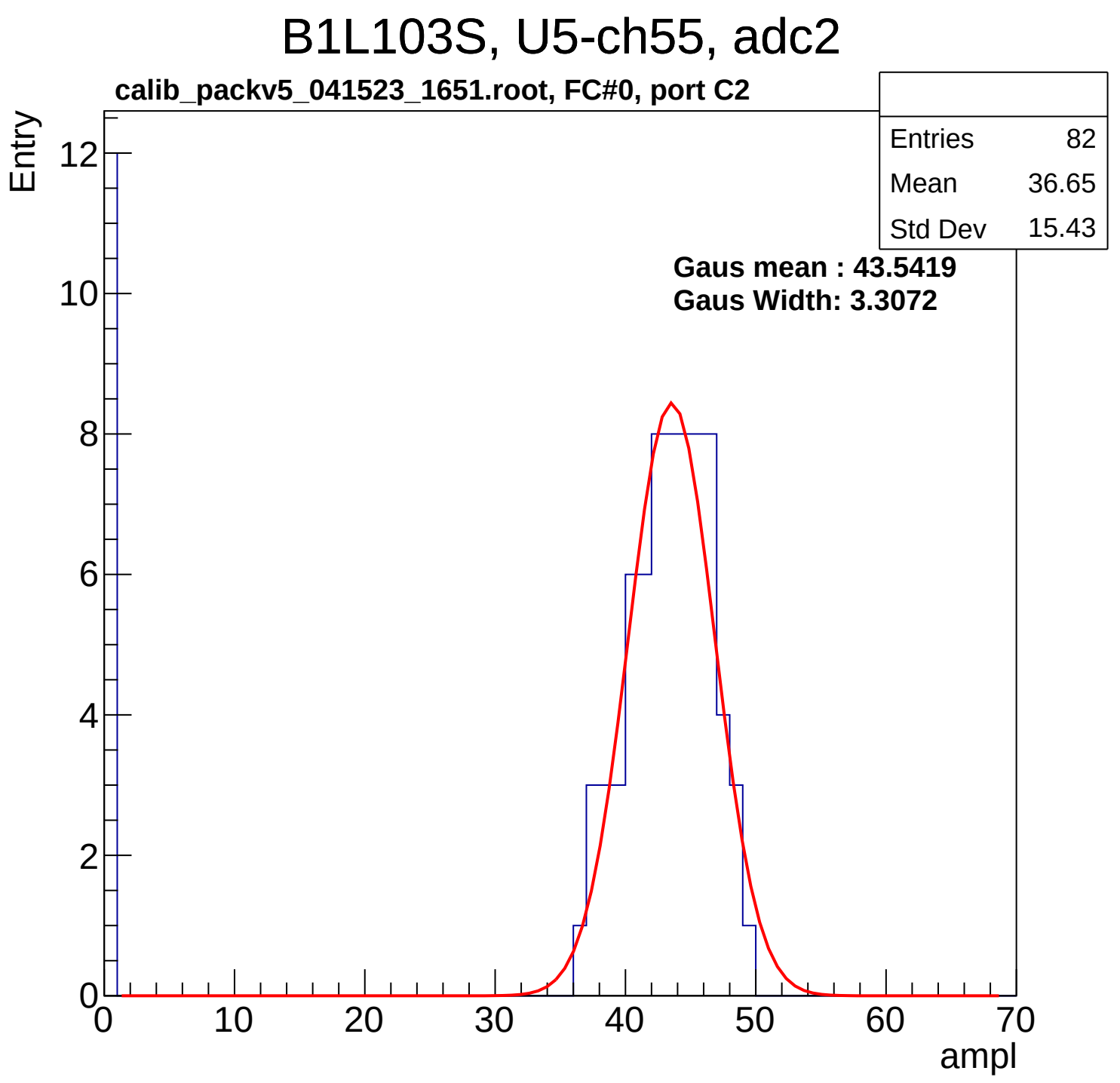
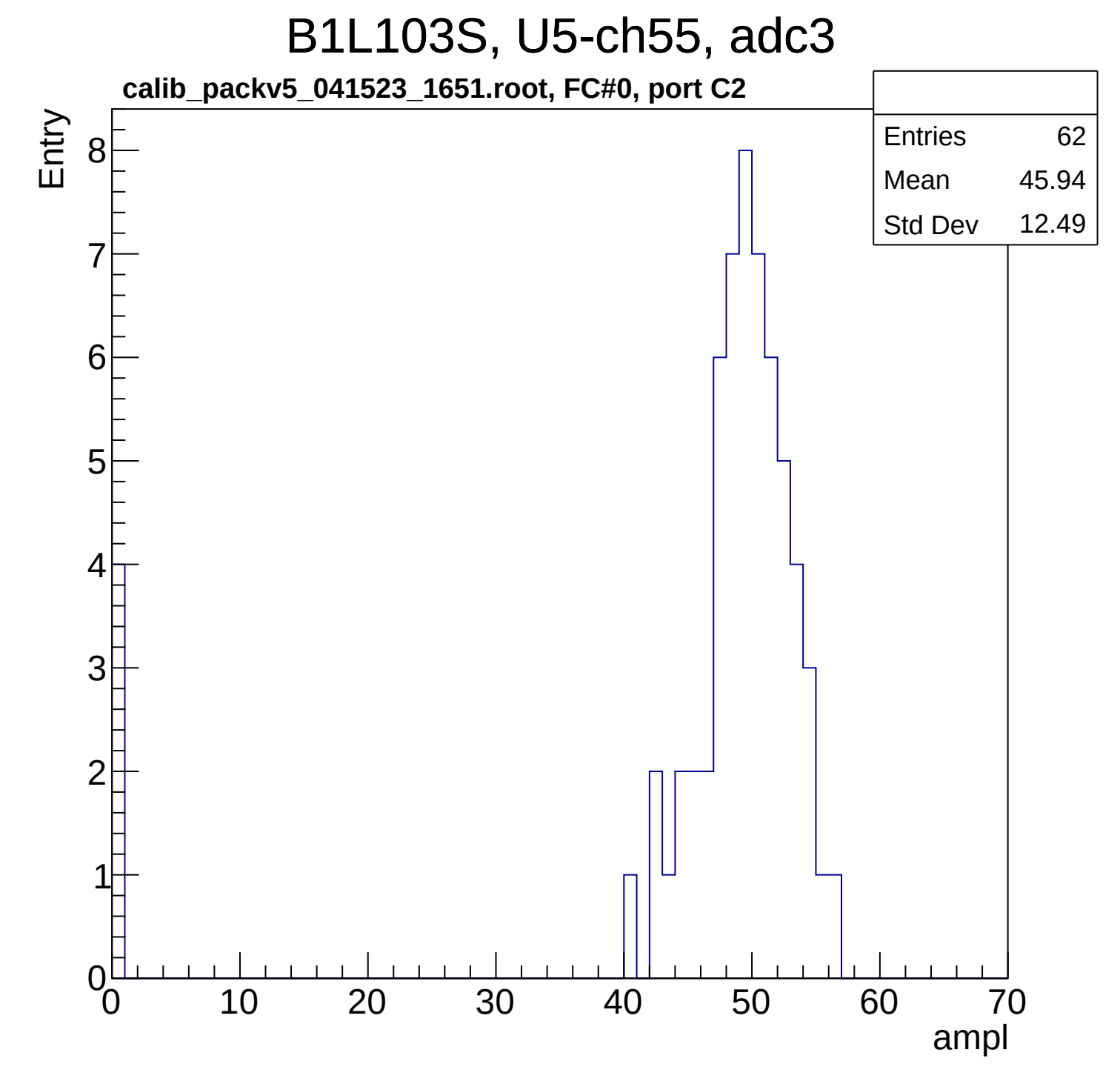
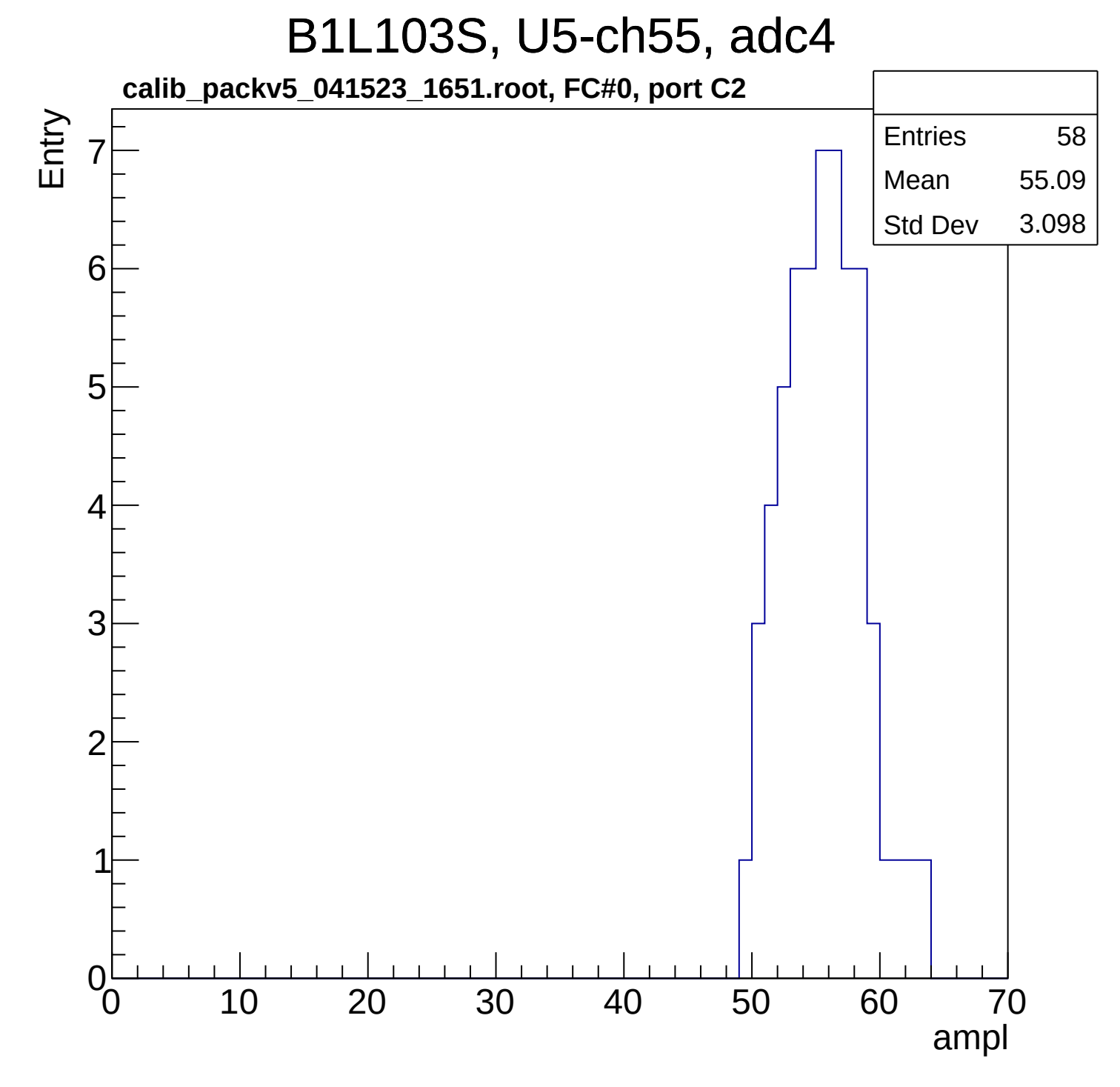
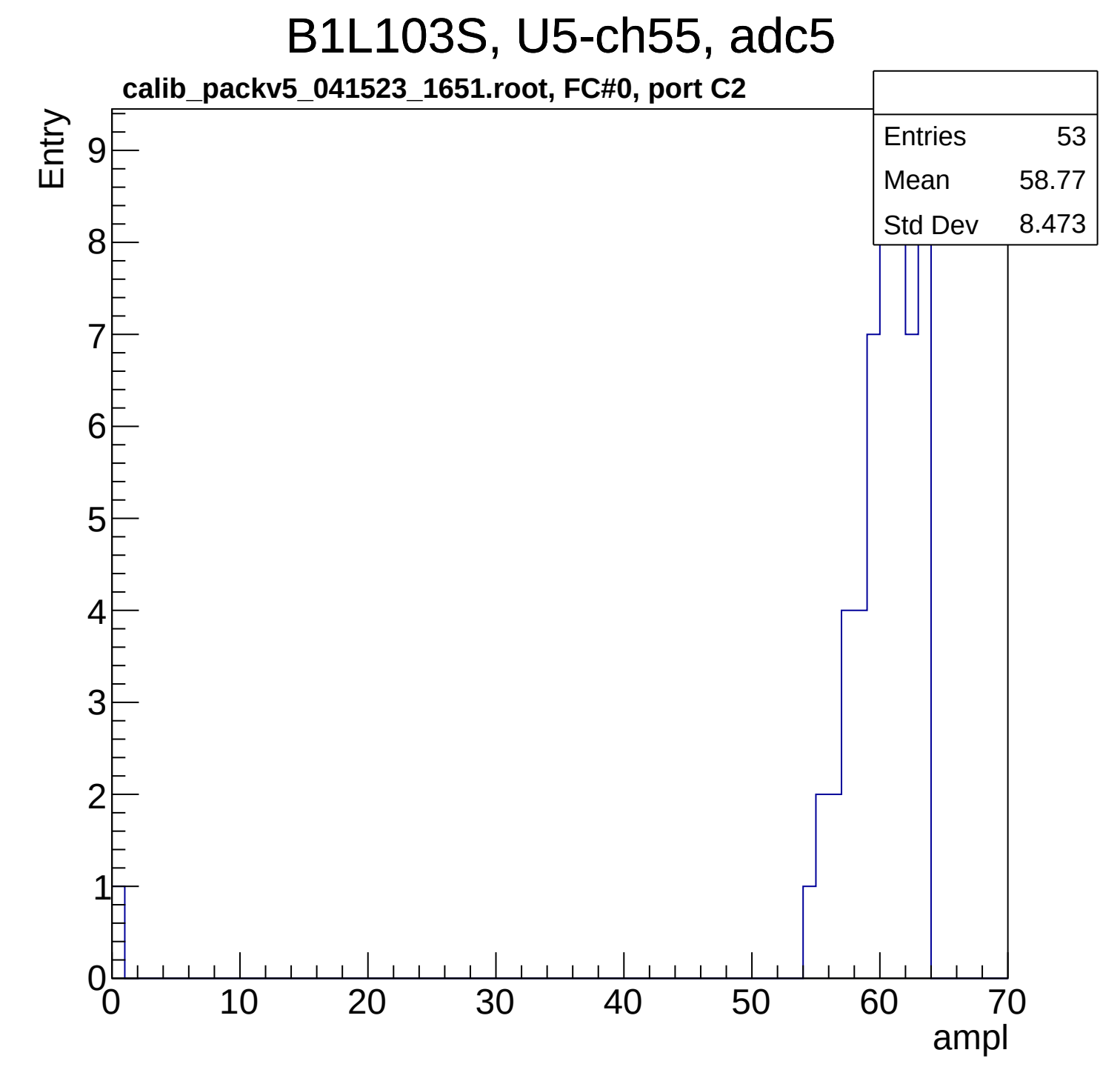

B1L103S, U5-ch55, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 36.65
Std Dev 15.43
Gaus mean : 43.5419
Gaus Width: 3.3072
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U5-ch55, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 45.94
Std Dev 12.49
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U5-ch55, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 55.09
Std Dev 3.098
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U5-ch55, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.77
Std Dev 8.473
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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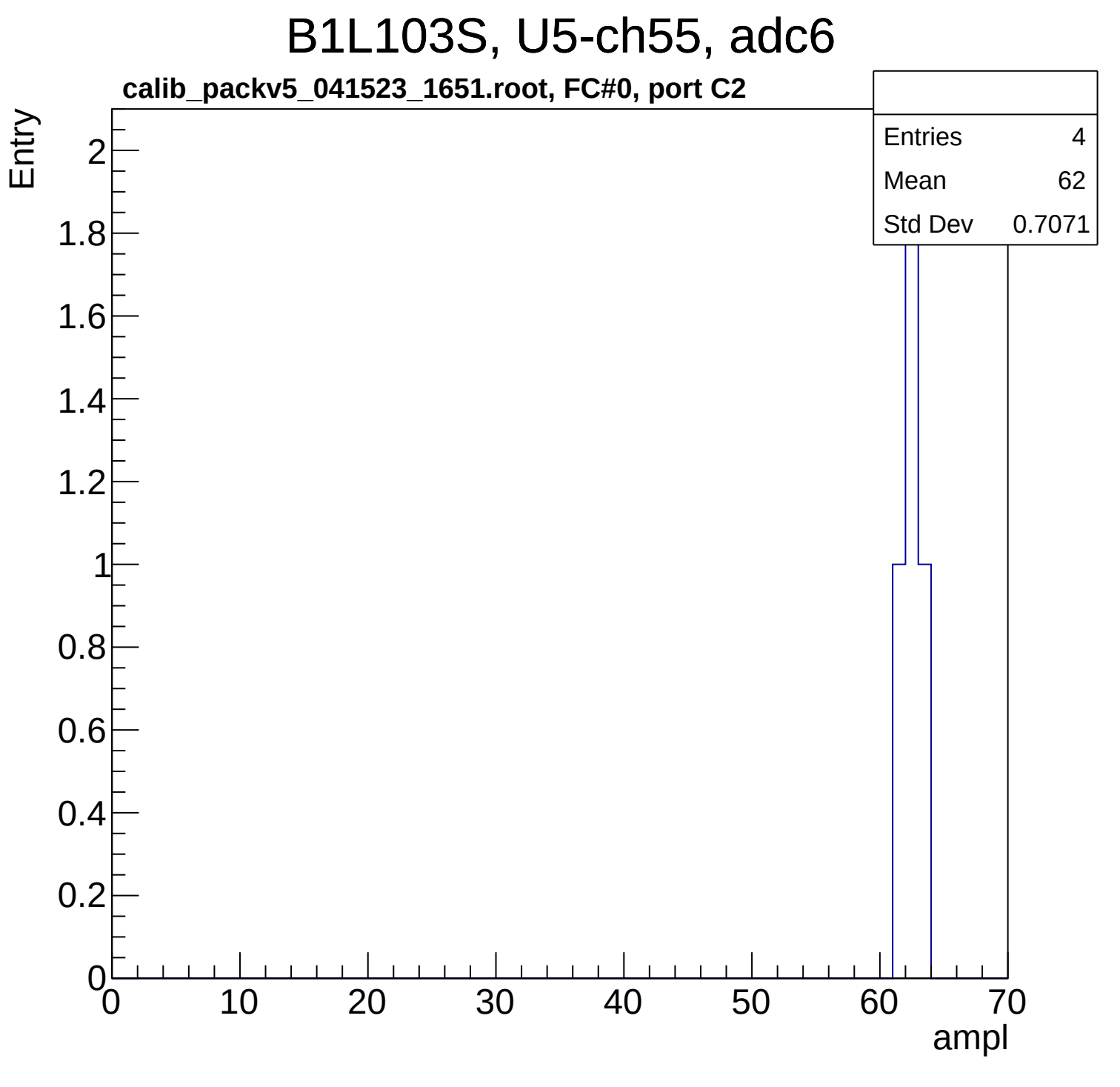
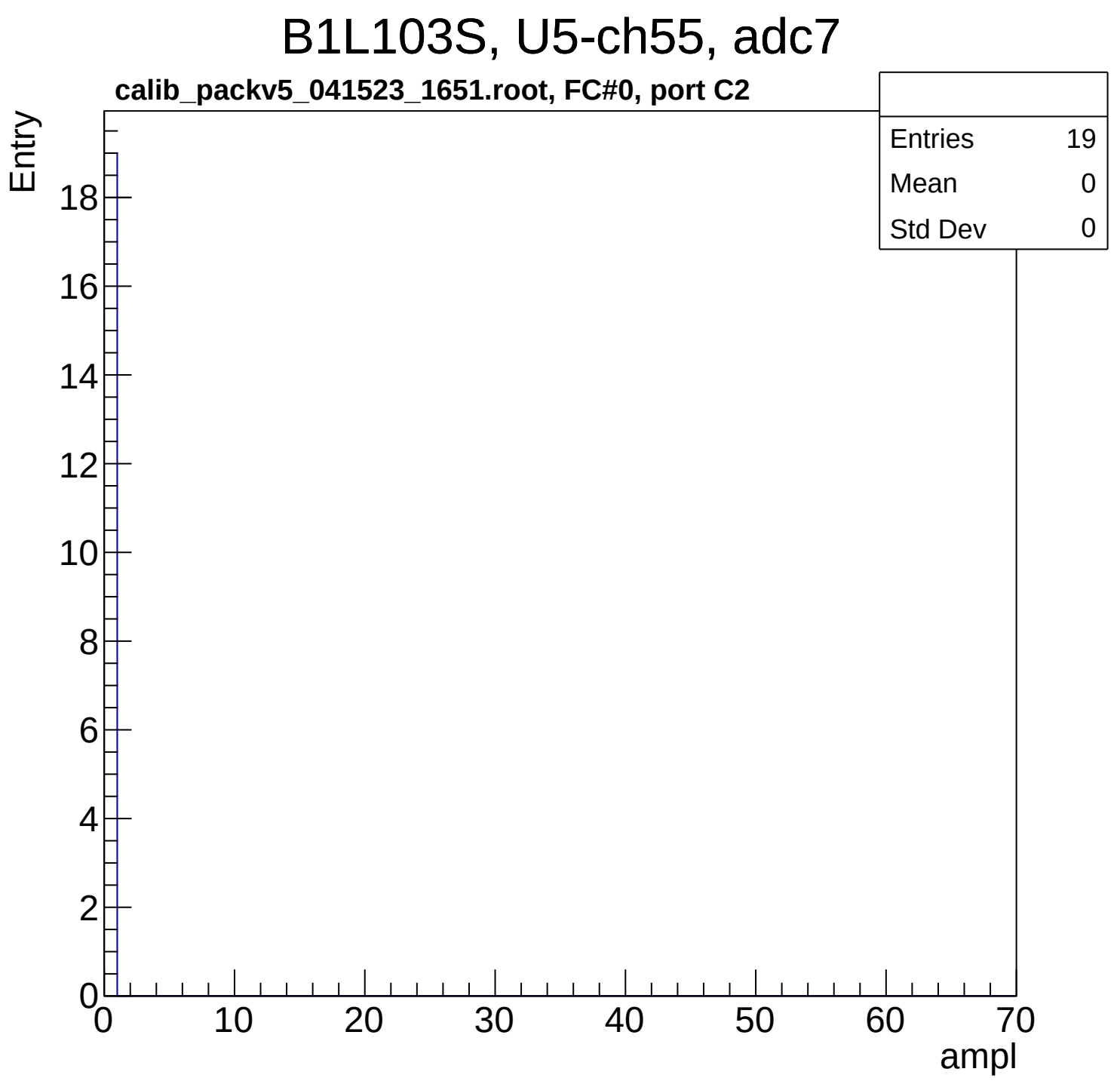
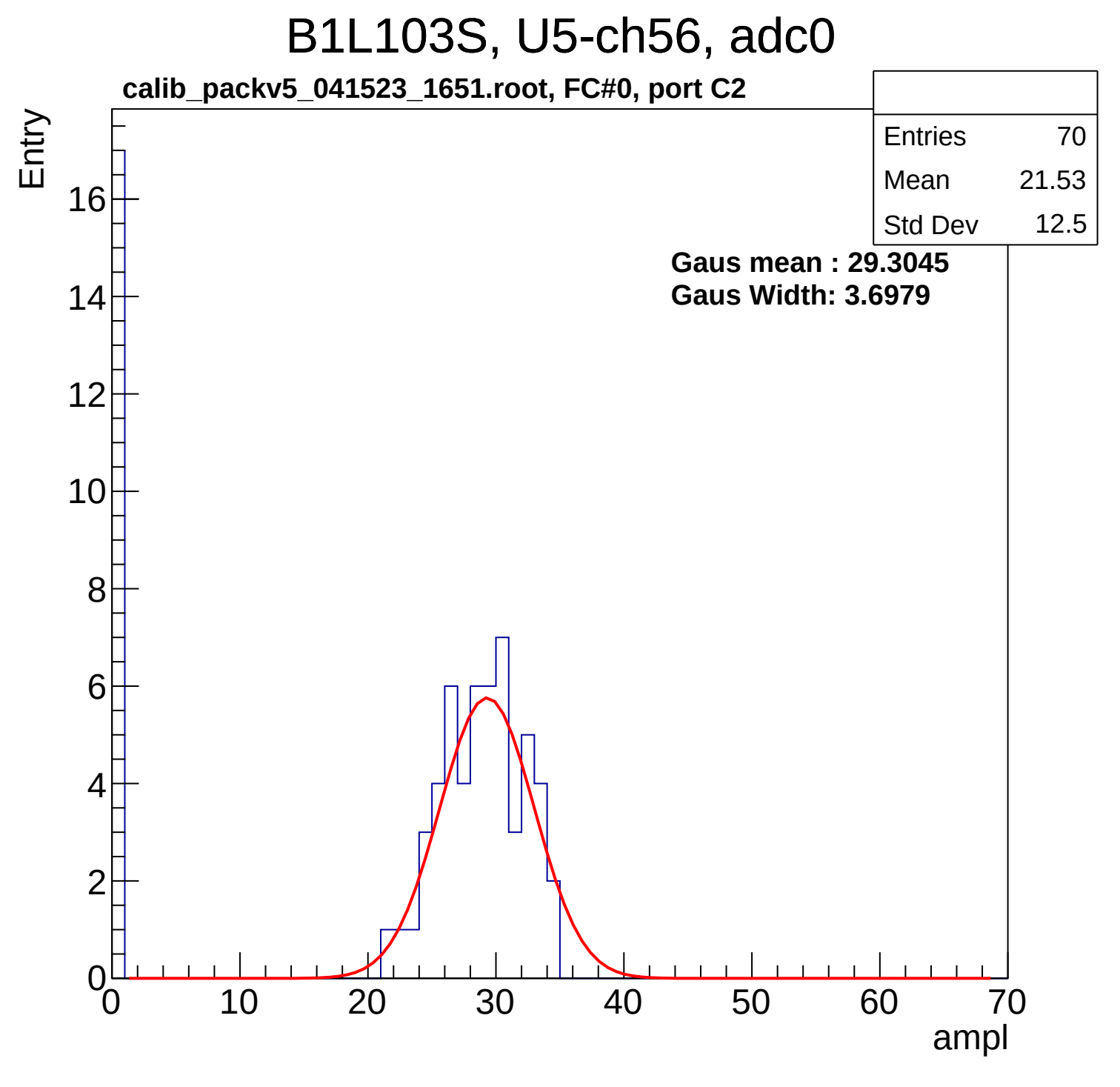
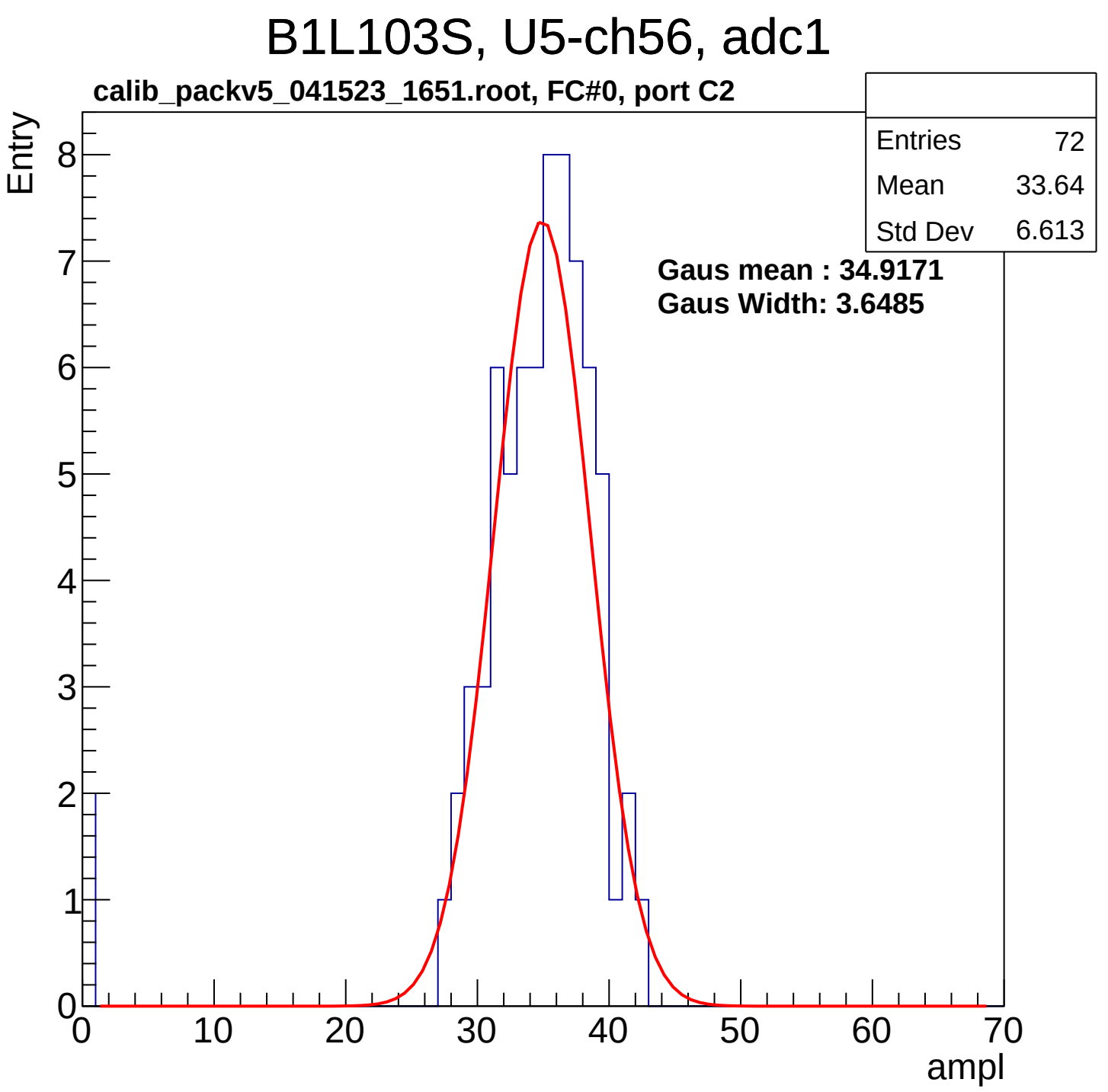
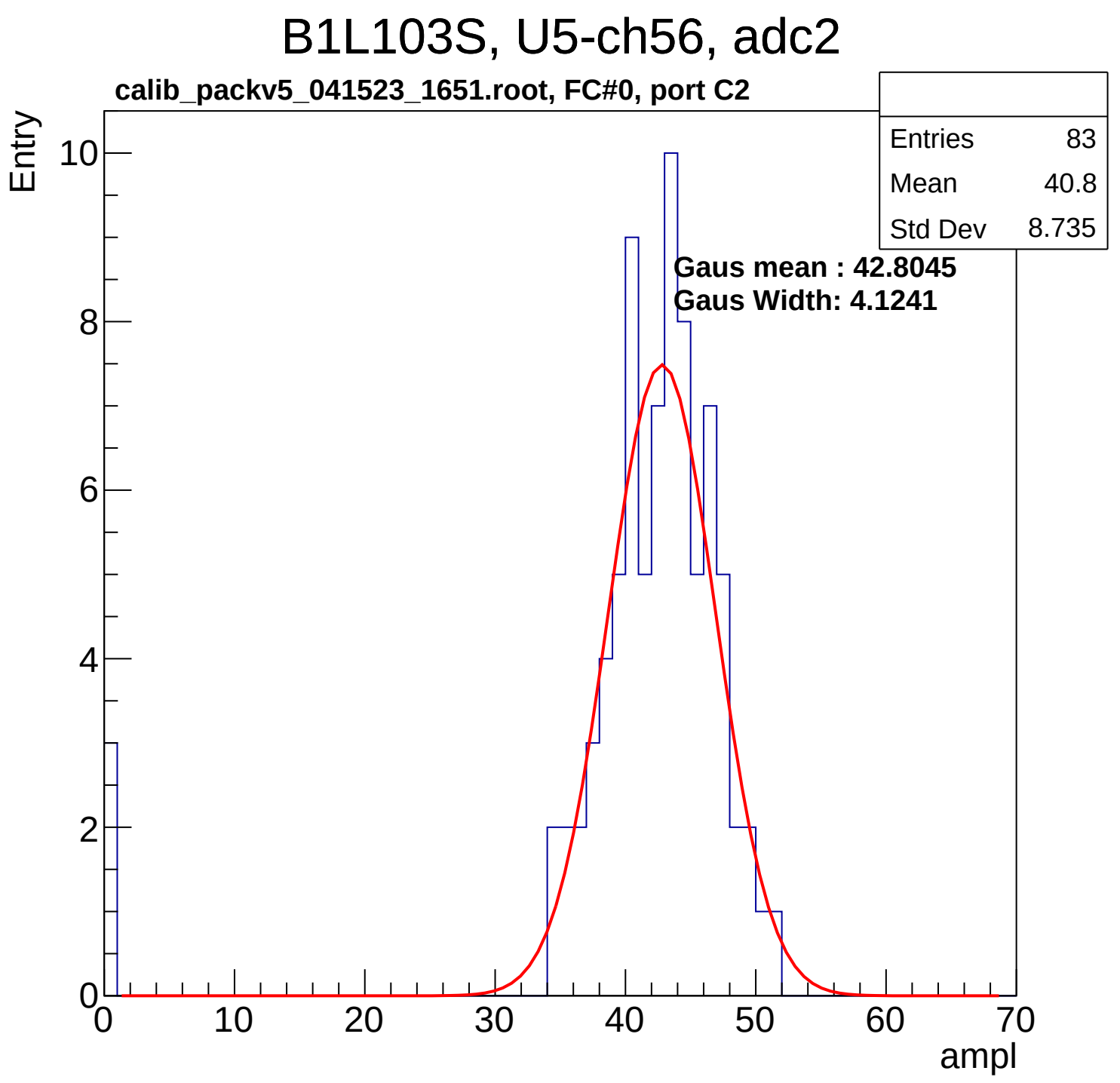
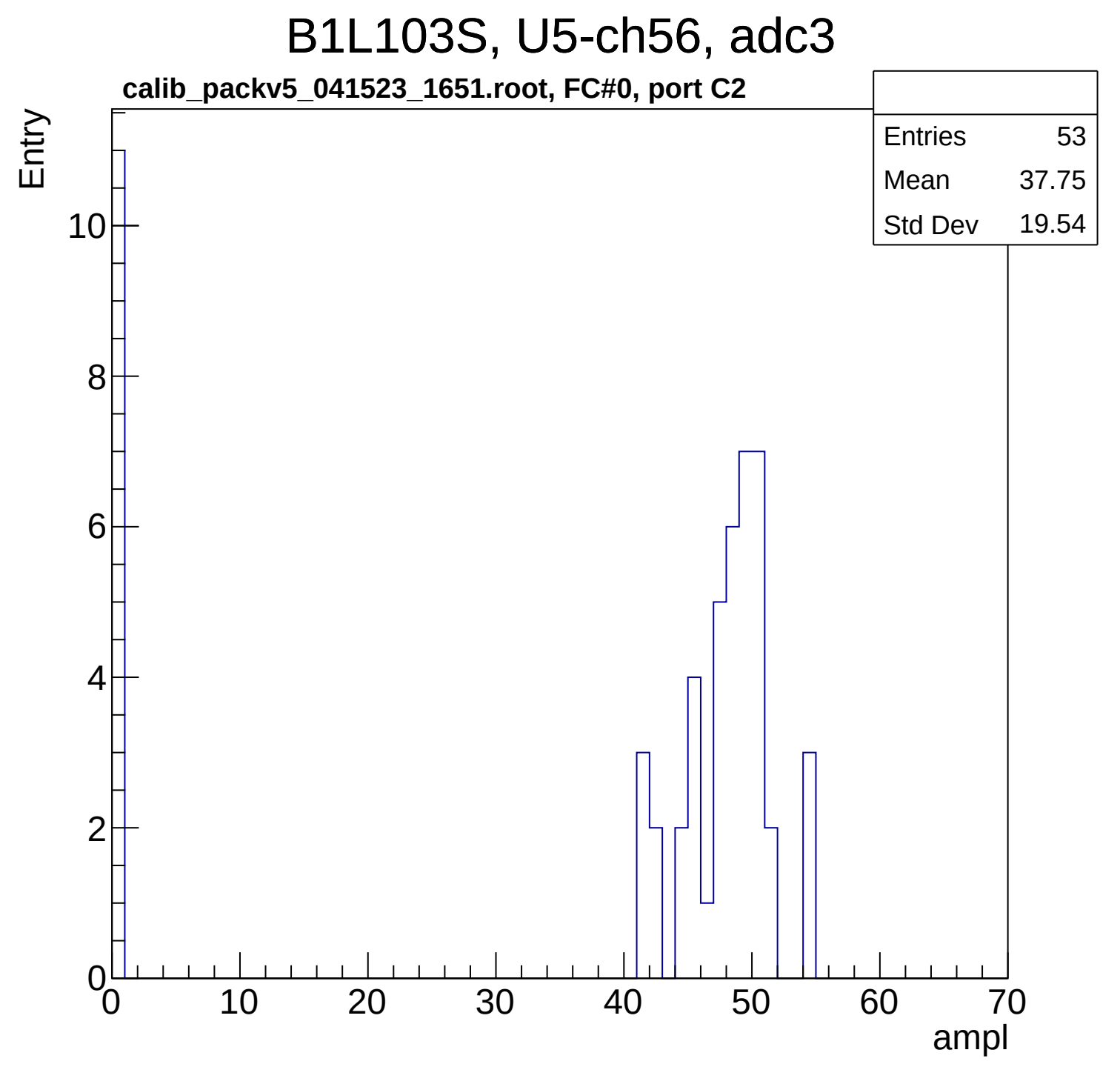

B1L103S, U5-ch55, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62
Std Dev 0.7071
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

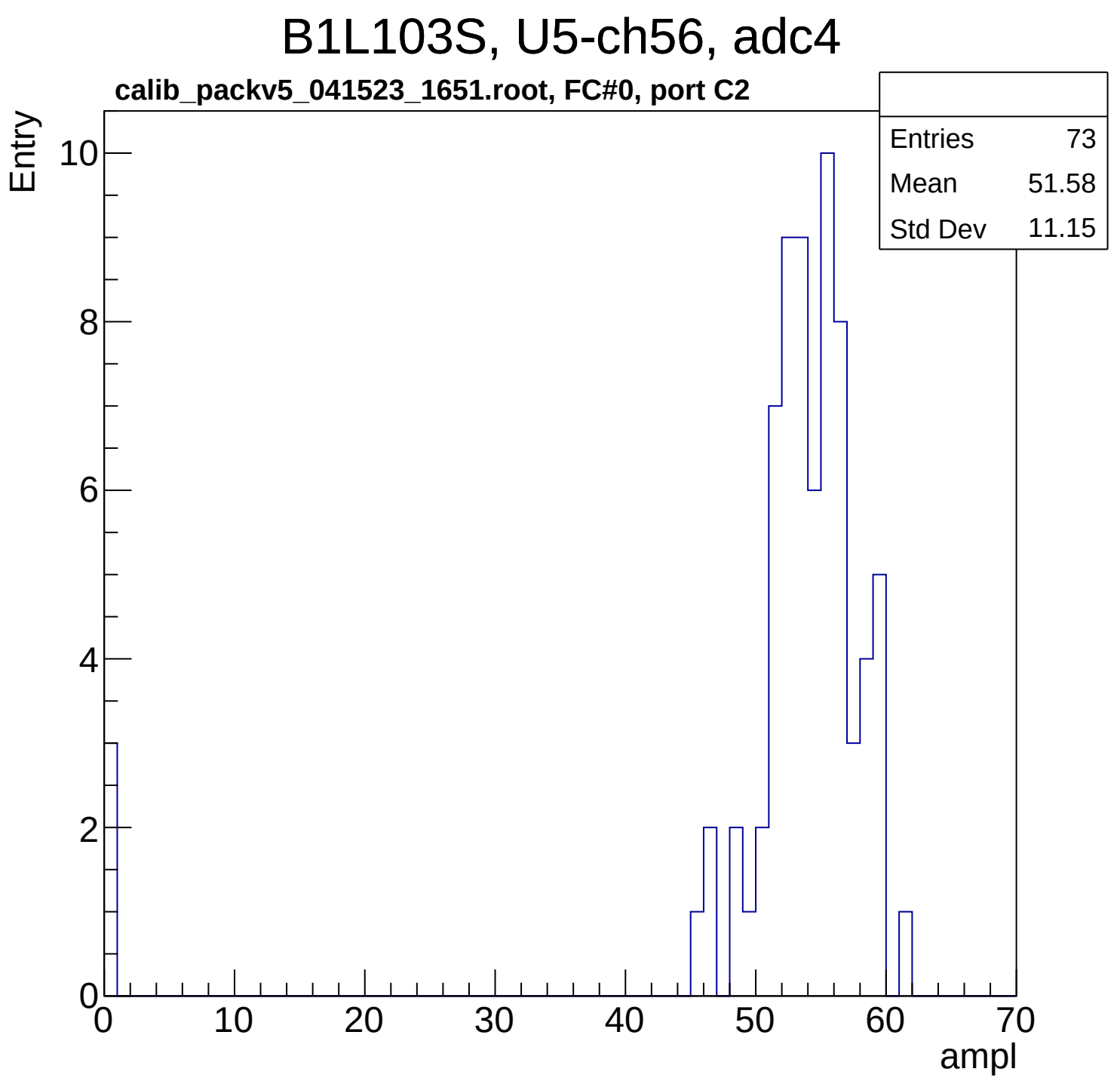

B1L103S, U5-ch55, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch56, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 21.53
Std Dev 12.5
Gaus mean : 29.3045
Gaus Width: 3.6979
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U5-ch56, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 33.64
Std Dev 6.613
Gaus mean : 34.9171
Gaus Width: 3.6485
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U5-ch56, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 40.8
Std Dev 8.735
Gaus mean : 42.8045
Gaus Width: 4.1241
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U5-ch56, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 37.75
Std Dev 19.54
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch56, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 51.58
Std Dev 11.15
Entry
ampl
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2
4
6
8
10
0
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20
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40
50
60
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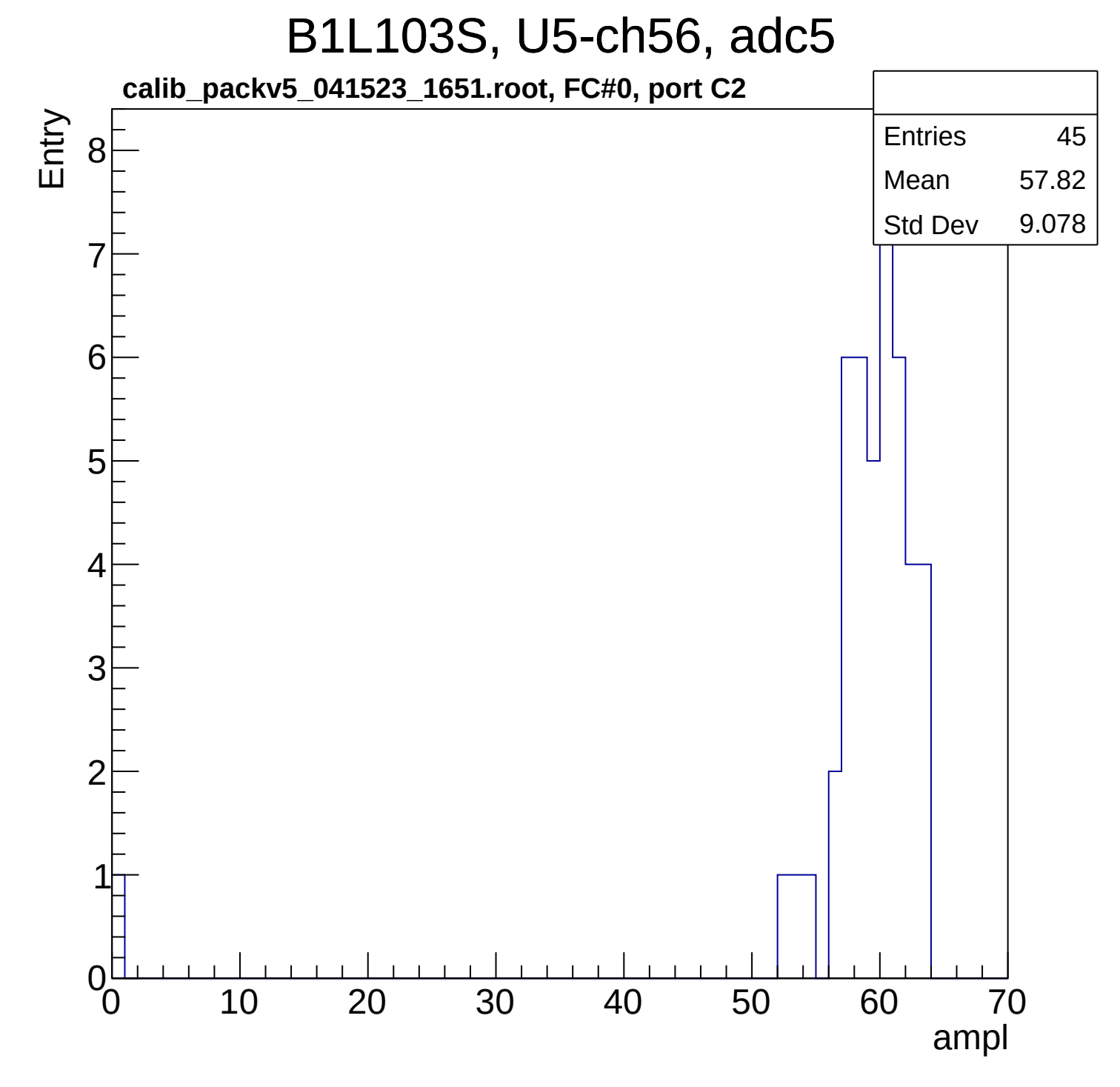
B1L103S, U5-ch56, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 57.82
Std Dev 9.078
Entry
ampl
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1
2
3
4
5
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7
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0
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60
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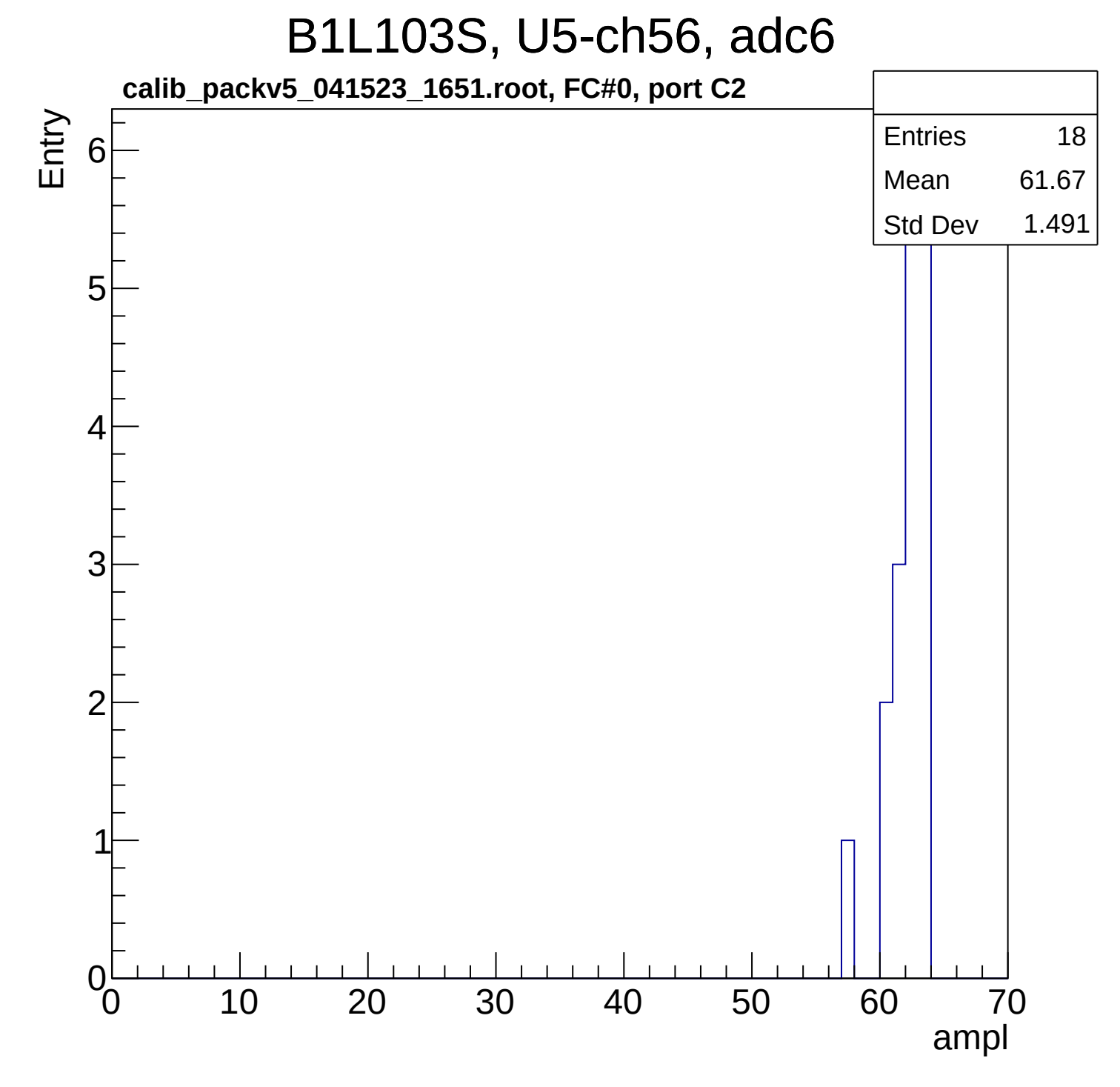
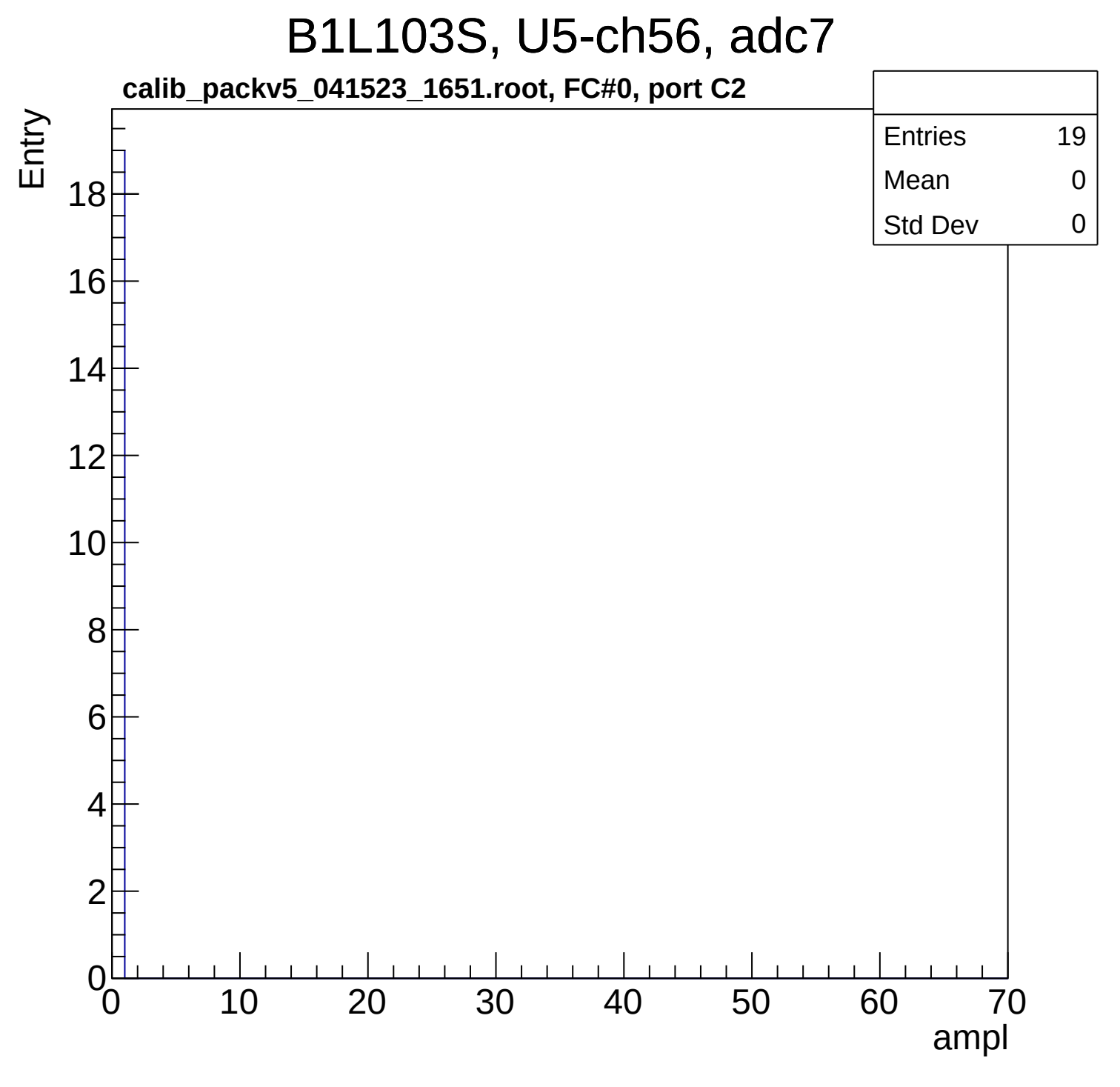
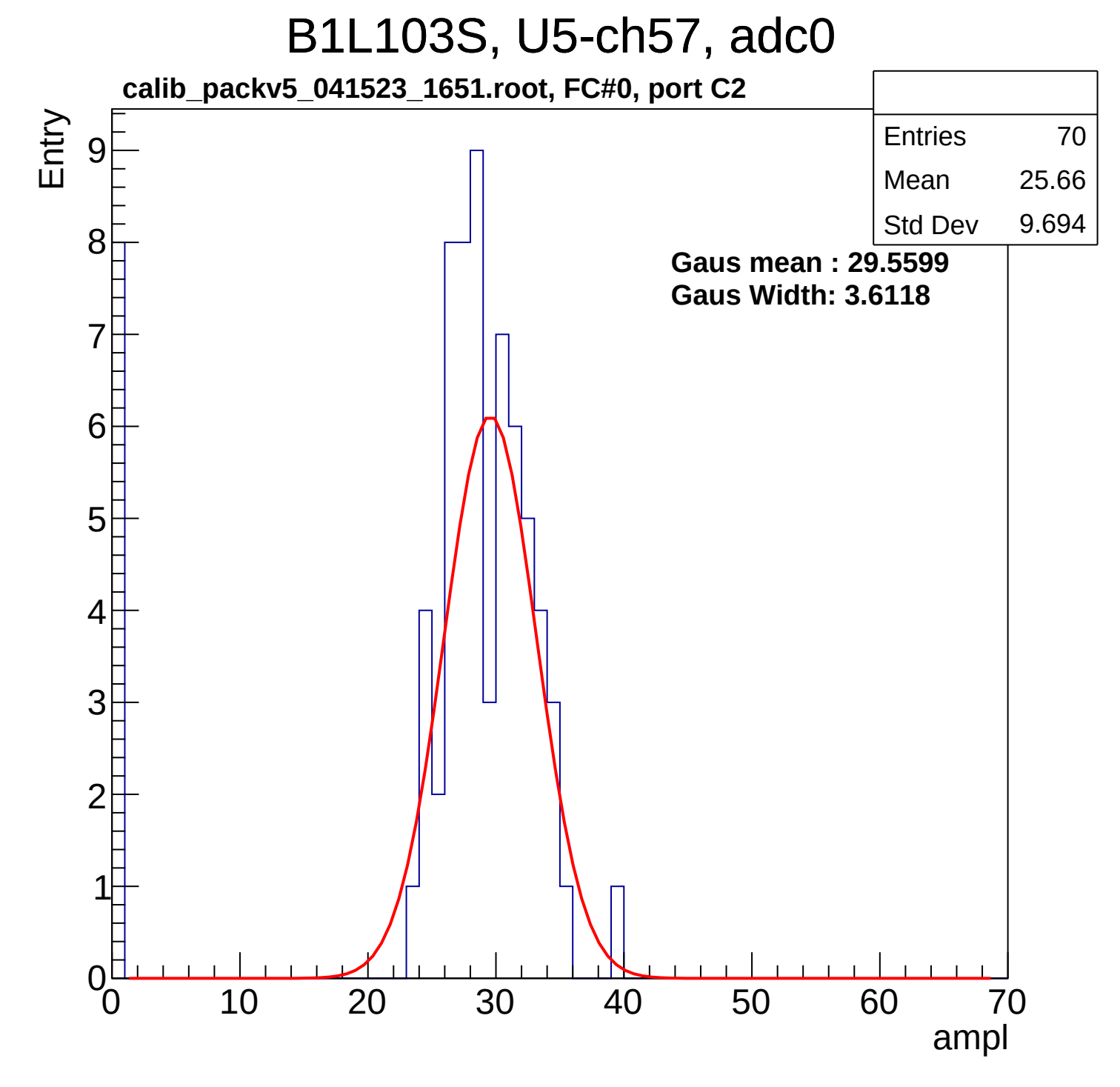

B1L103S, U5-ch56, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 61.67
Std Dev 1.491
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U5-ch56, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch57, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 25.66
Std Dev 9.694
Gaus mean : 29.5599
Gaus Width: 3.6118
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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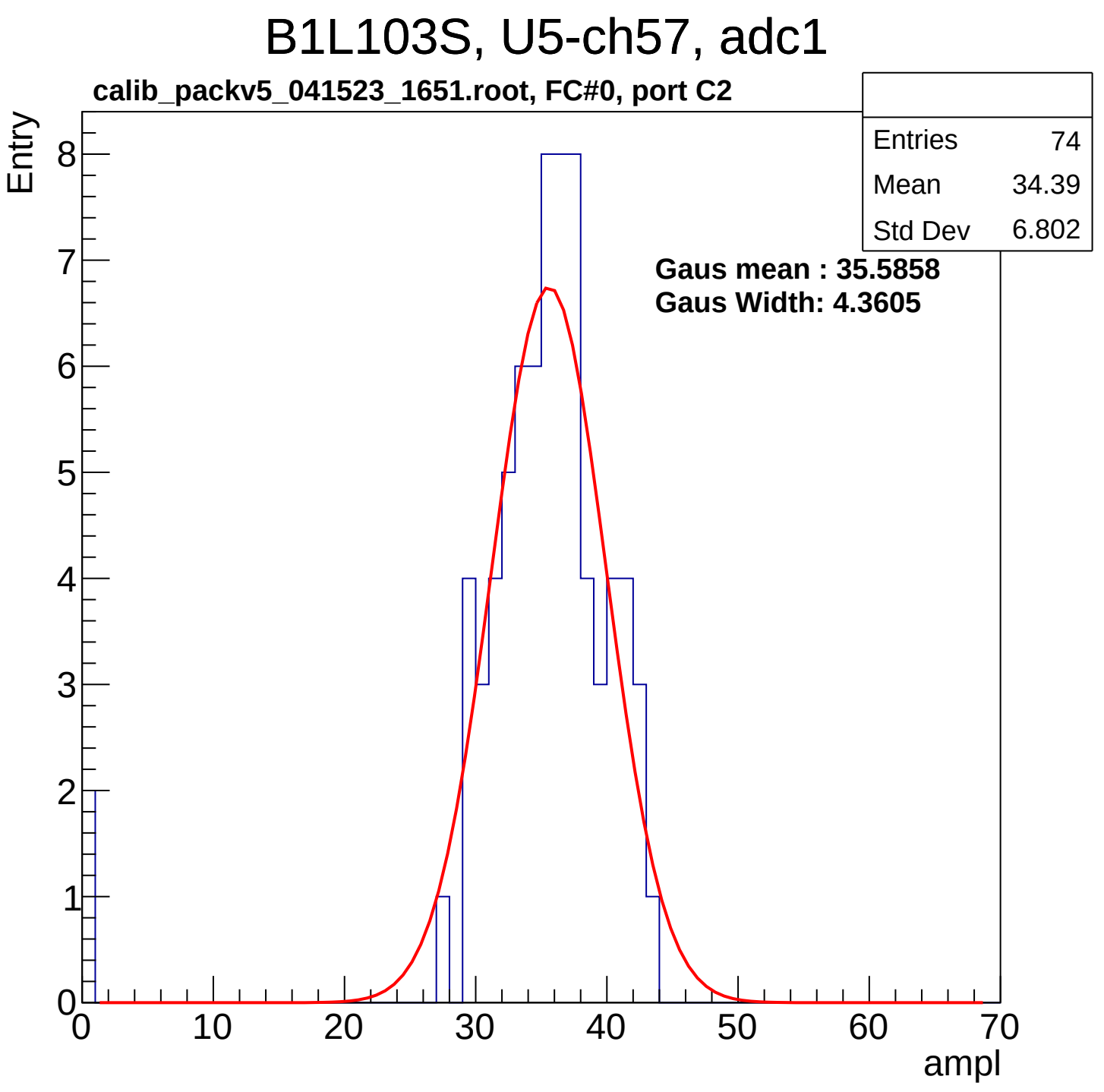
B1L103S, U5-ch57, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 34.39
Std Dev 6.802
Gaus mean : 35.5858
Gaus Width: 4.3605
Entry
ampl
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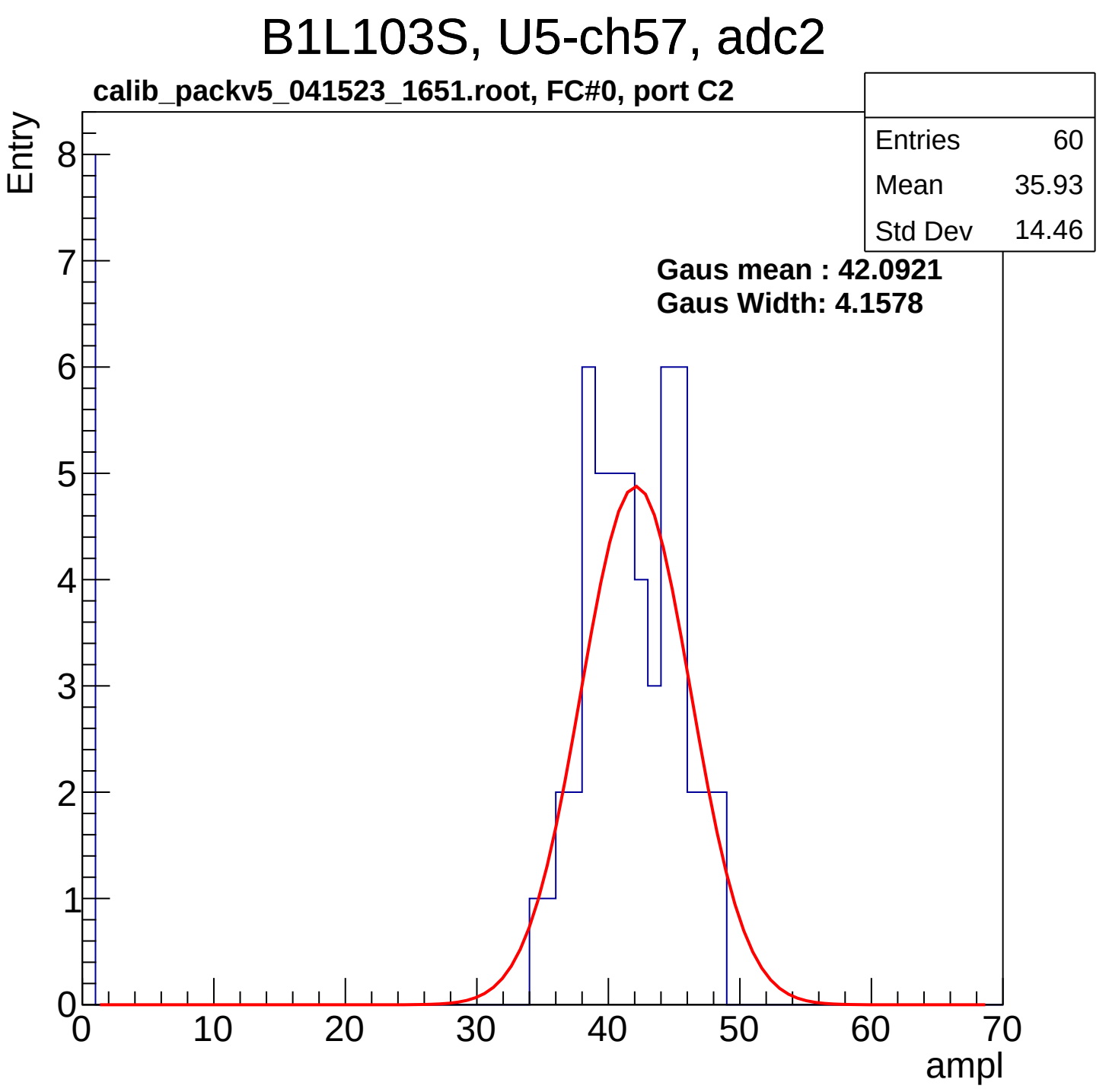
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U5-ch57, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 35.93
Std Dev 14.46
Gaus mean : 42.0921
Gaus Width: 4.1578
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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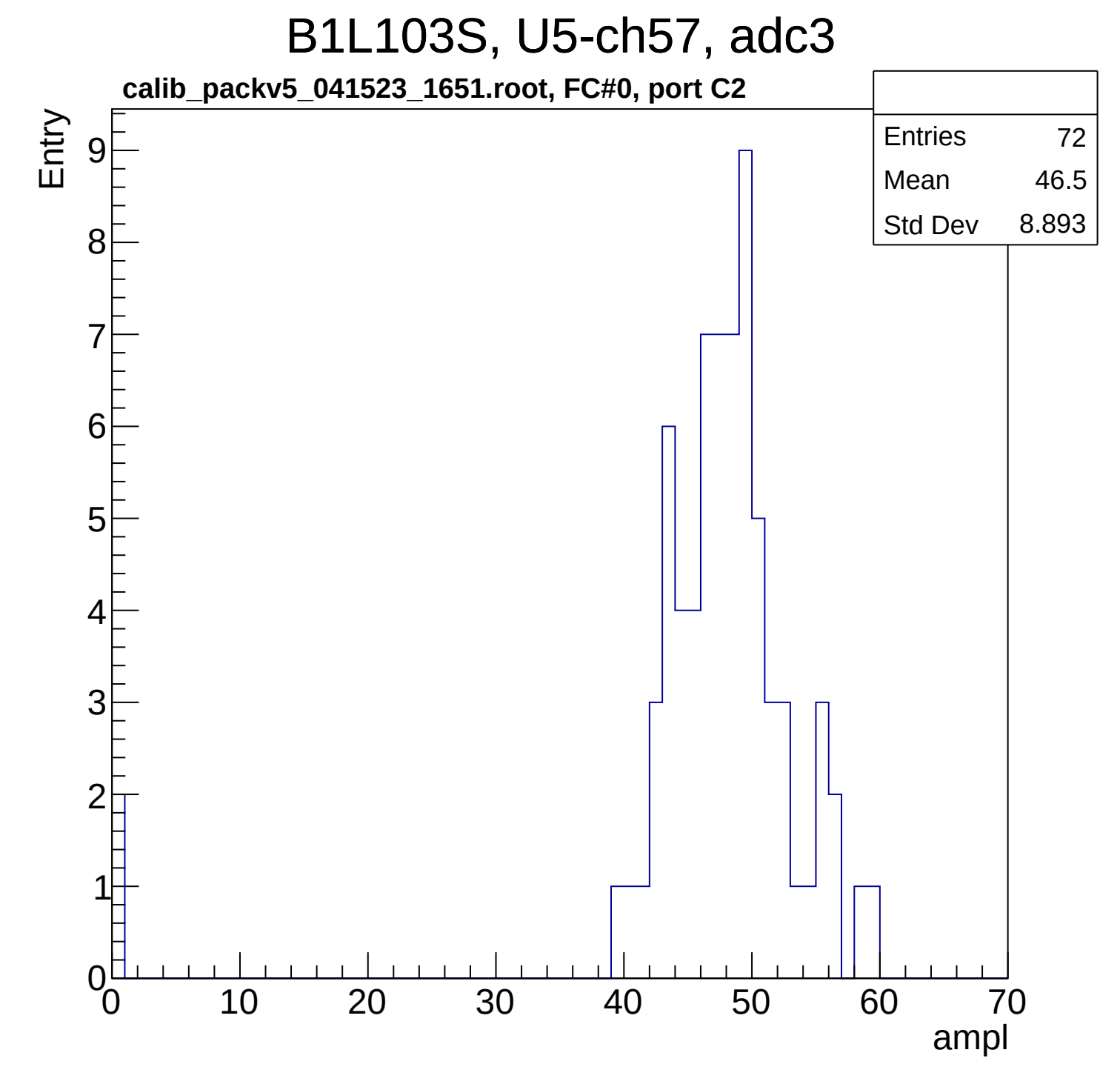
B1L103S, U5-ch57, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 46.5
Std Dev 8.893
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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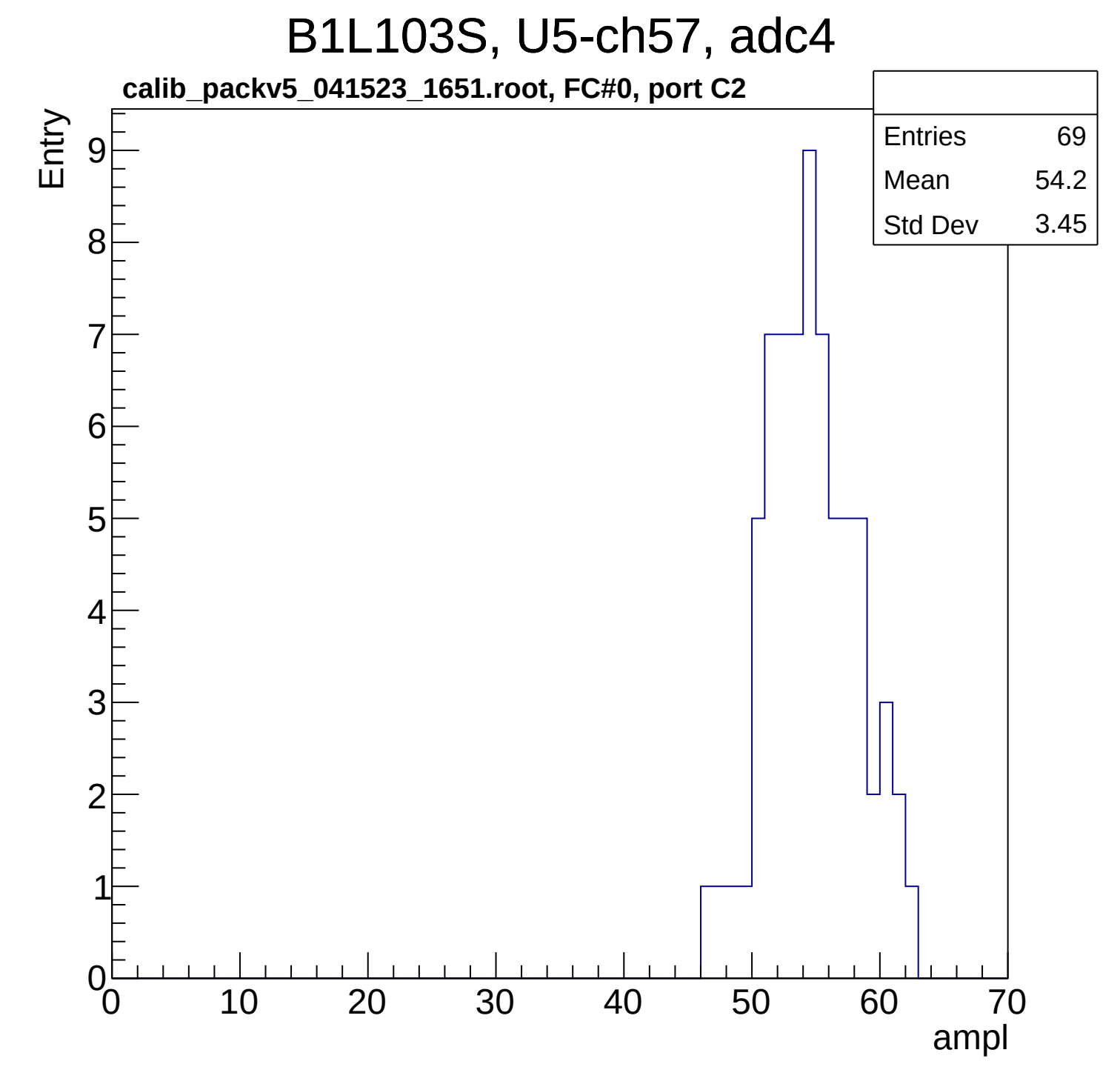
B1L103S, U5-ch57, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 54.2
Std Dev 3.45
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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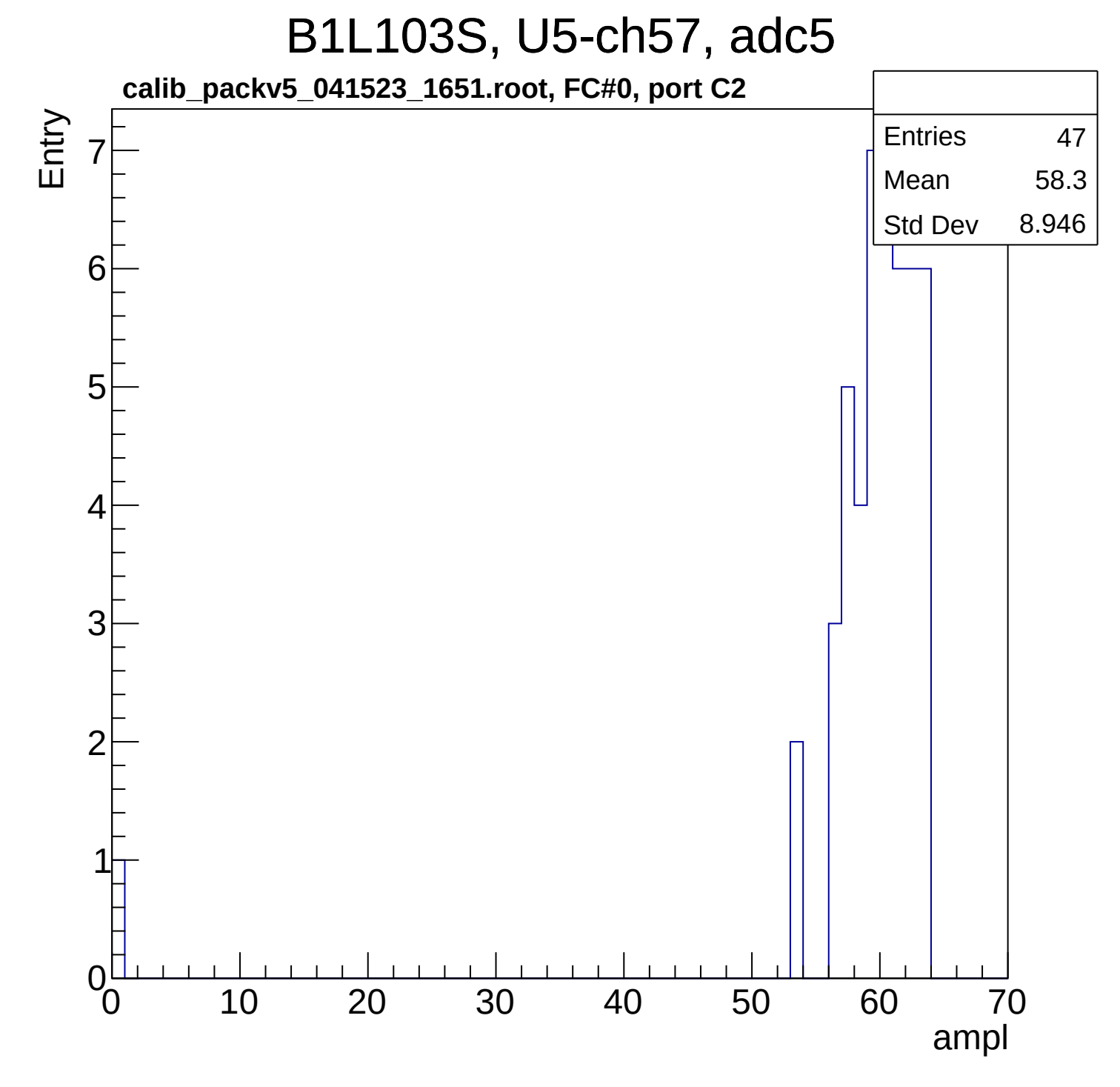
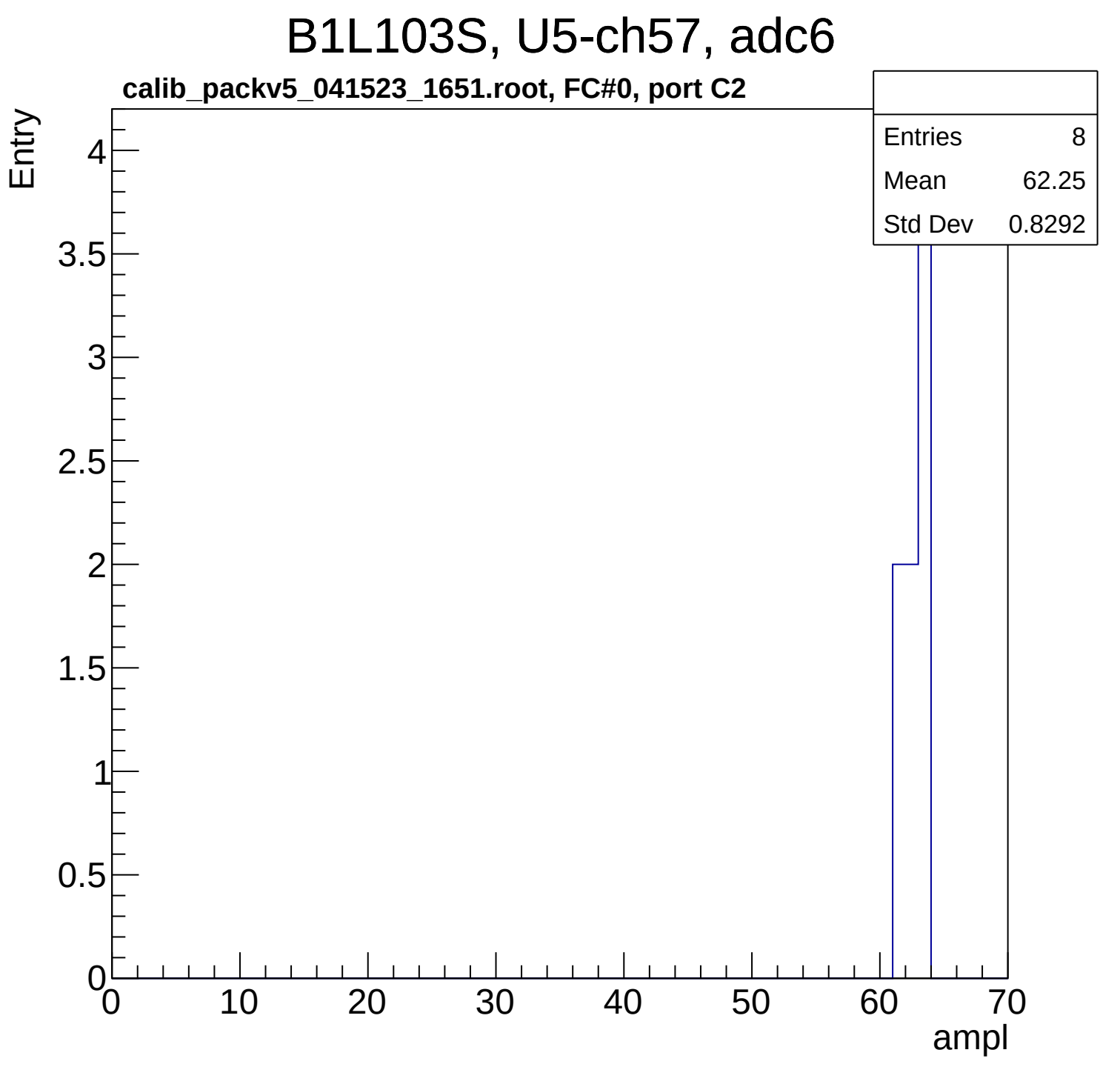

B1L103S, U5-ch57, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.3
Std Dev 8.946
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U5-ch57, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62.25
Std Dev 0.8292
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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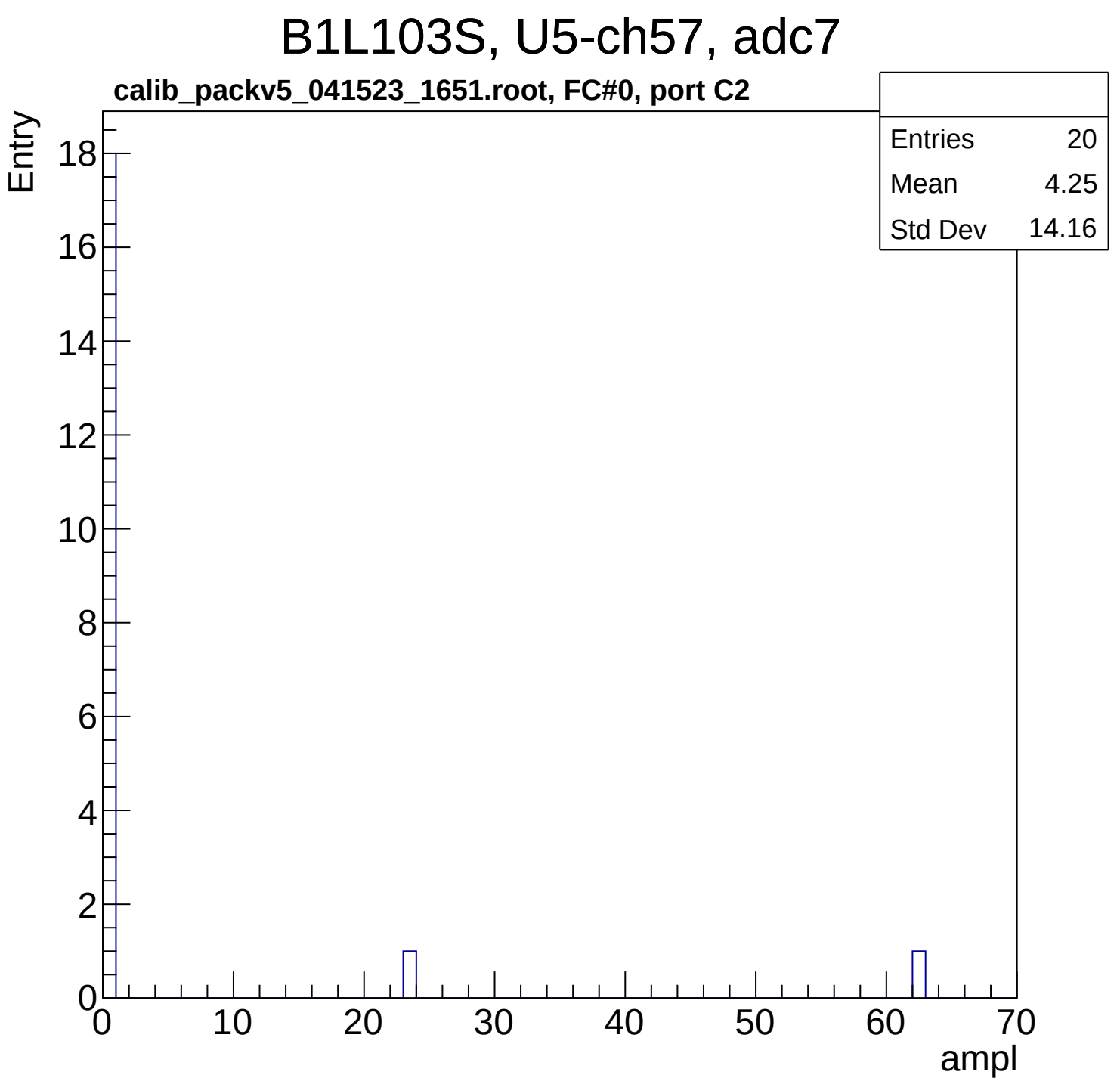
B1L103S, U5-ch57, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.25
Std Dev 14.16
Entry
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6
8
10
12
14
16
18
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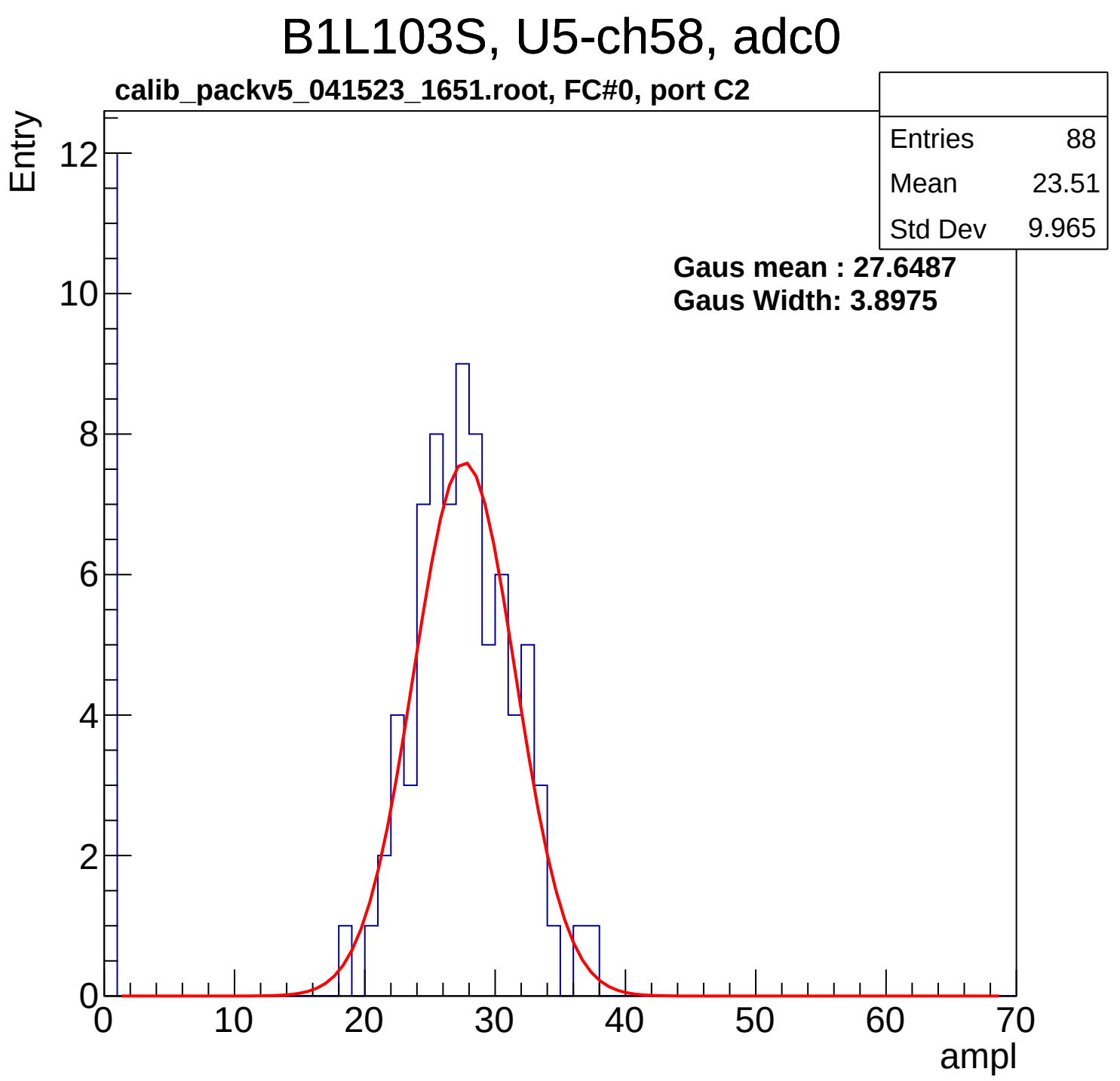
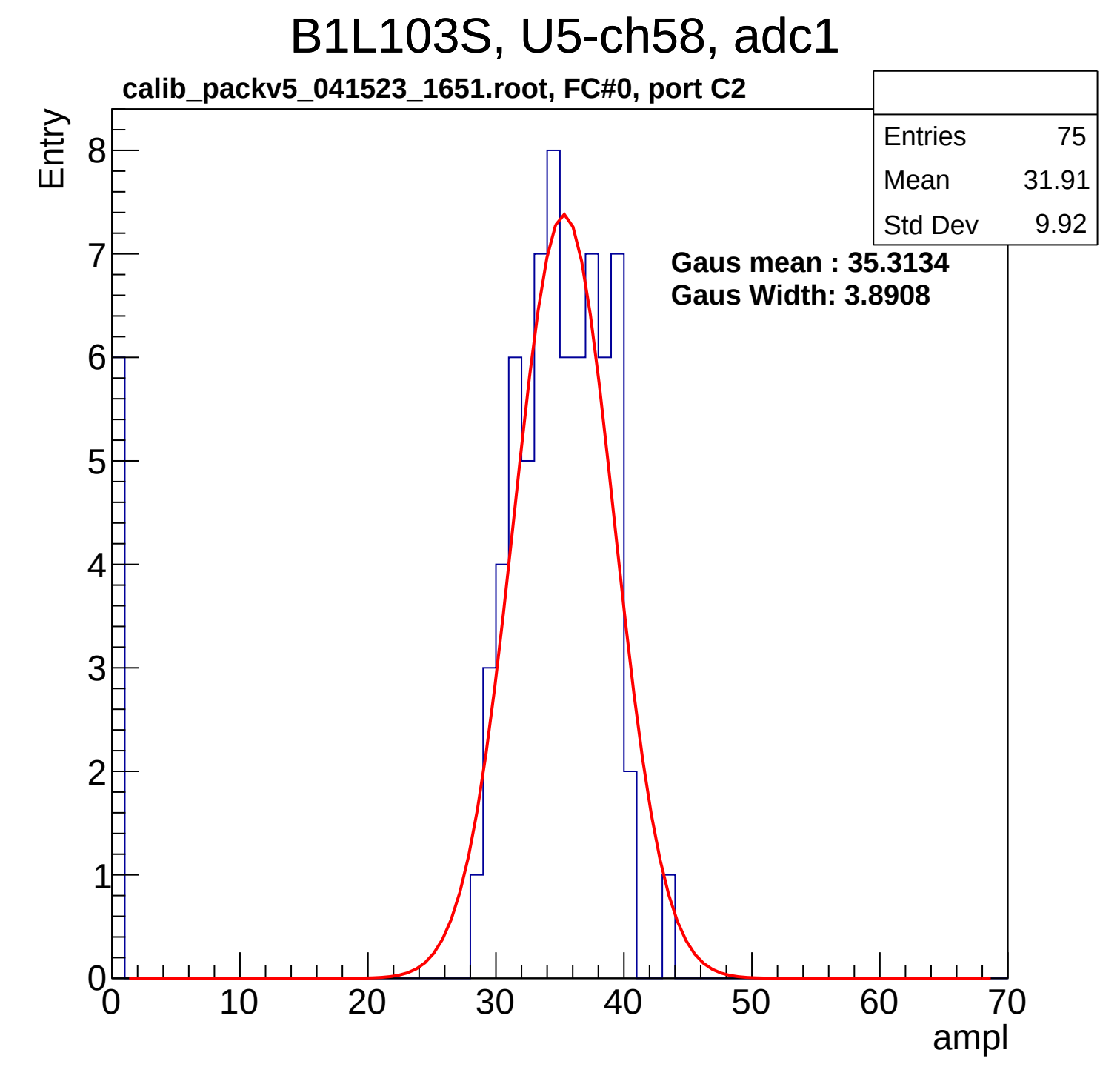
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch58, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 23.51
Std Dev 9.965
Gaus mean : 27.6487
Gaus Width: 3.8975
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U5-ch58, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 31.91
Std Dev 9.92
Gaus mean : 35.3134
Gaus Width: 3.8908
Entry
ampl
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2
3
4
5
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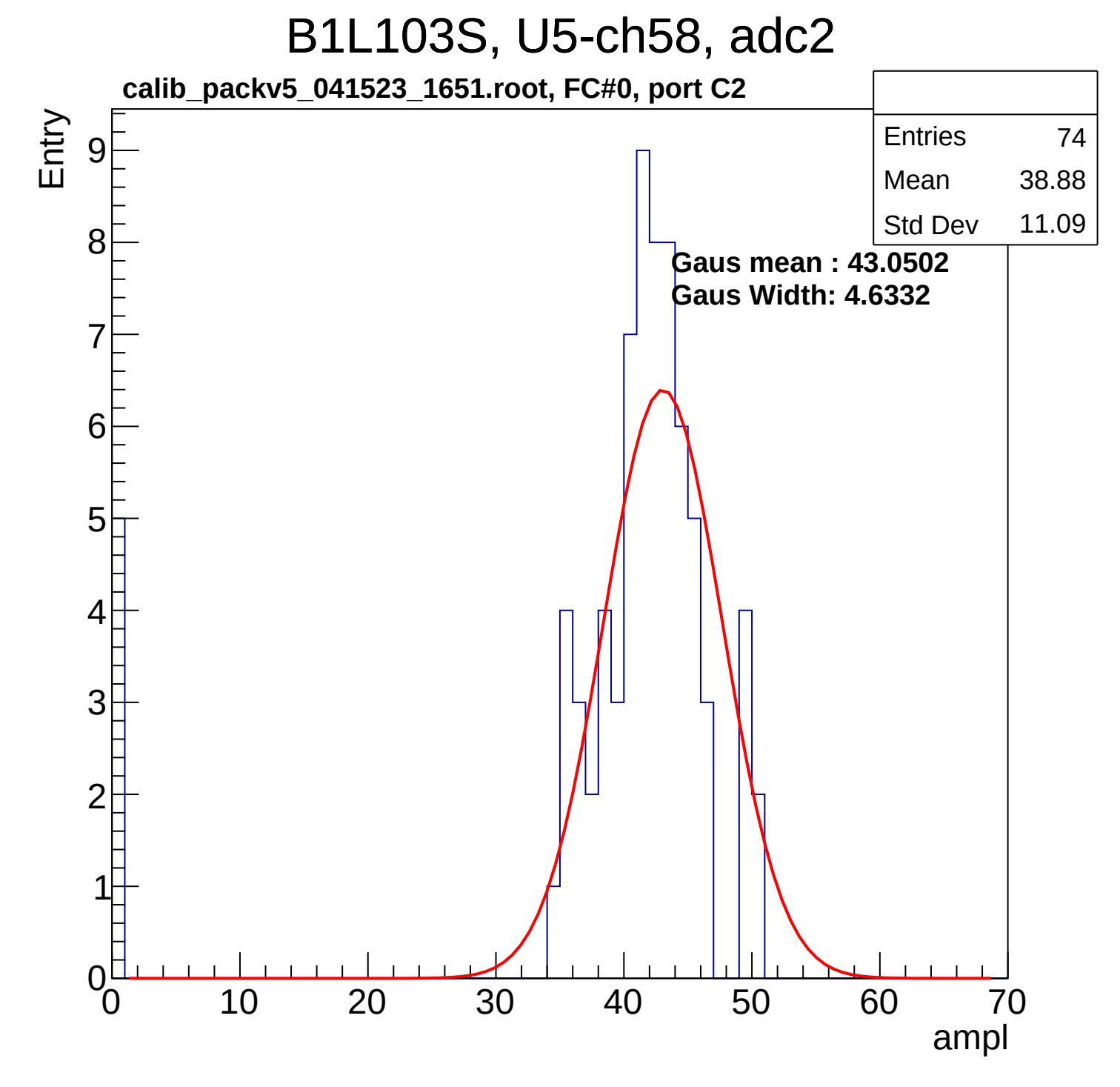
B1L103S, U5-ch58, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 38.88
Std Dev 11.09
Gaus mean : 43.0502
Gaus Width: 4.6332
Entry
ampl
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3
4
5
6
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0
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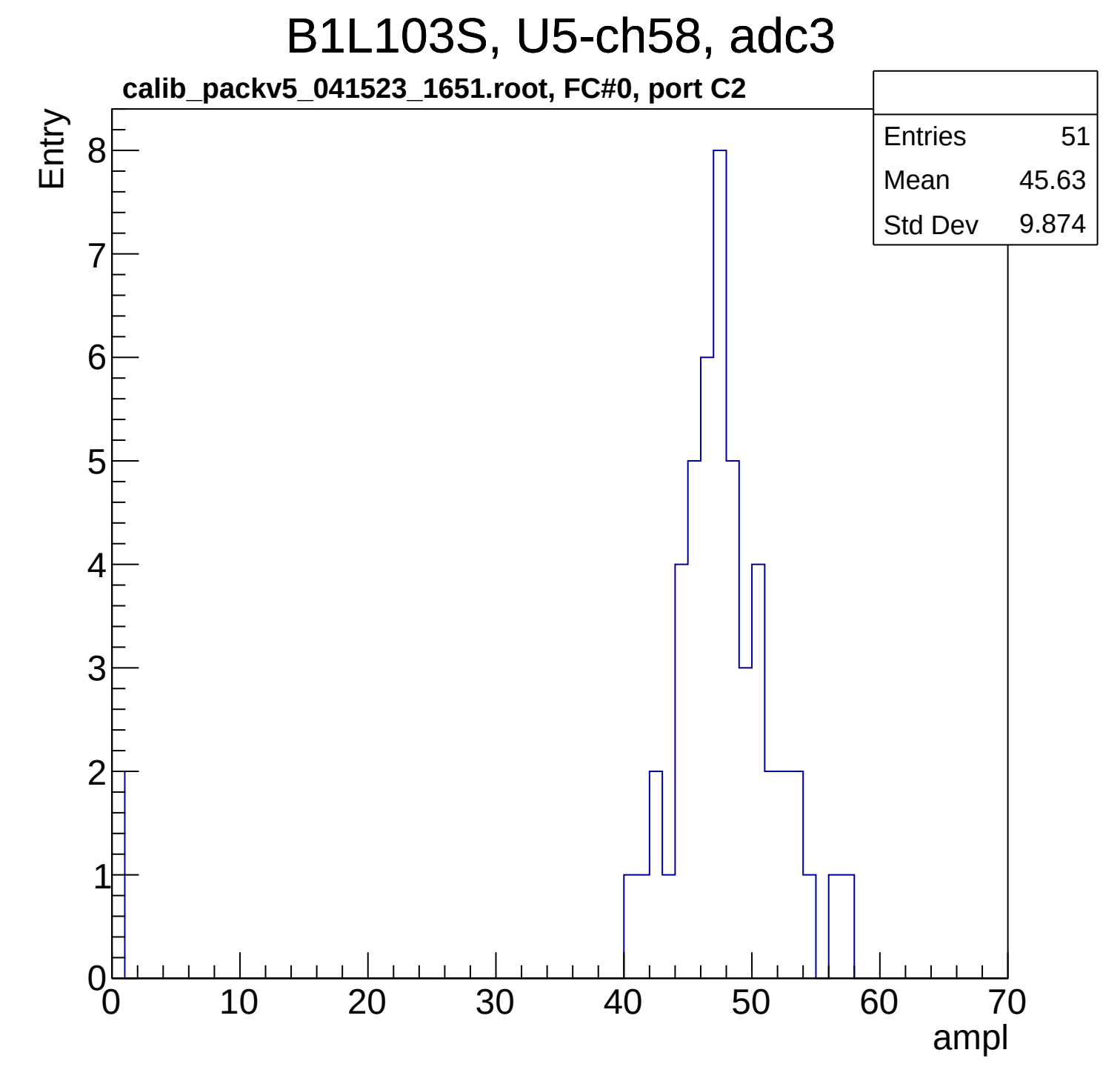
B1L103S, U5-ch58, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 45.63
Std Dev 9.874
Entry
ampl
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3
4
5
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0
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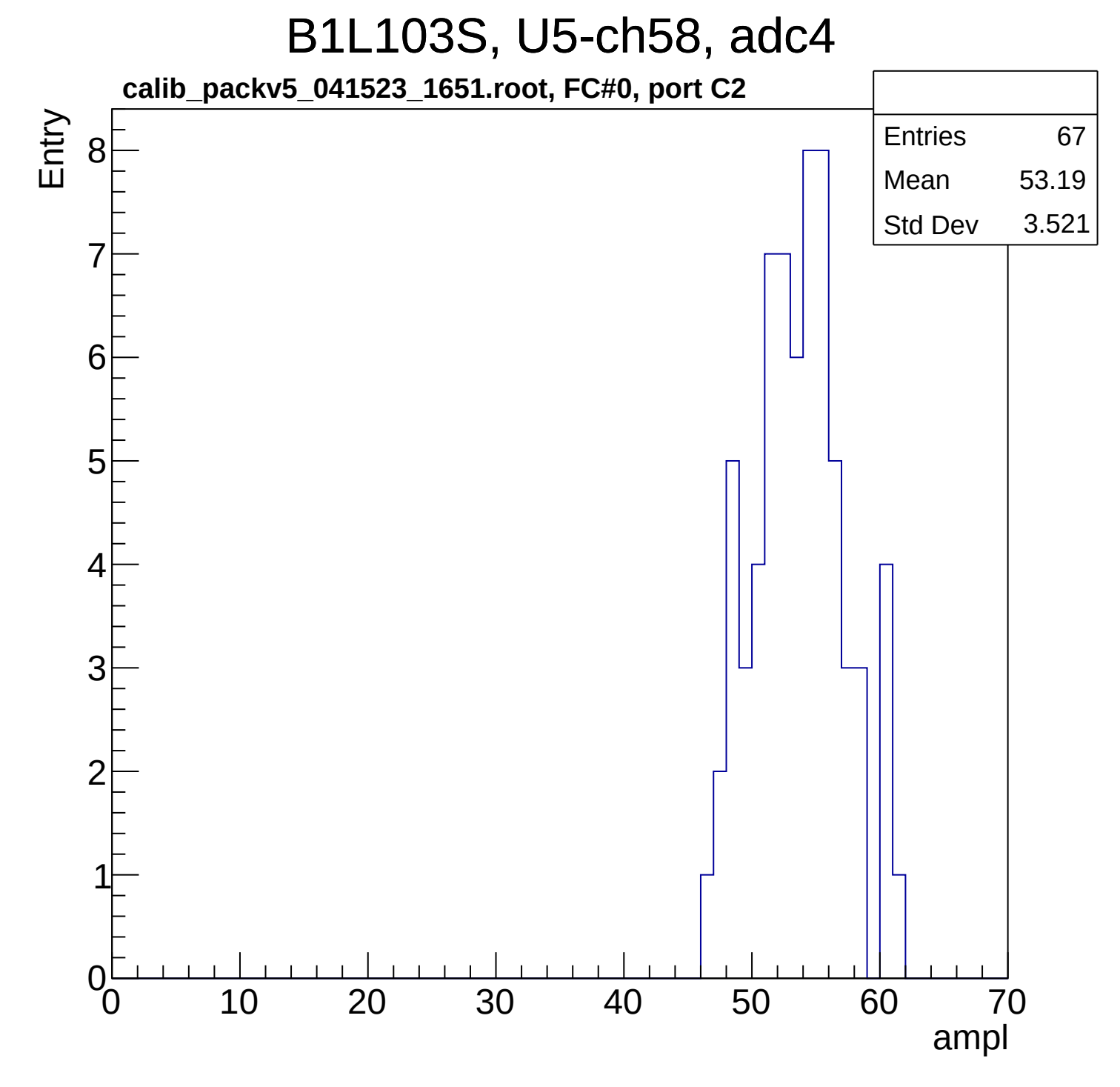
B1L103S, U5-ch58, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 53.19
Std Dev 3.521
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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60
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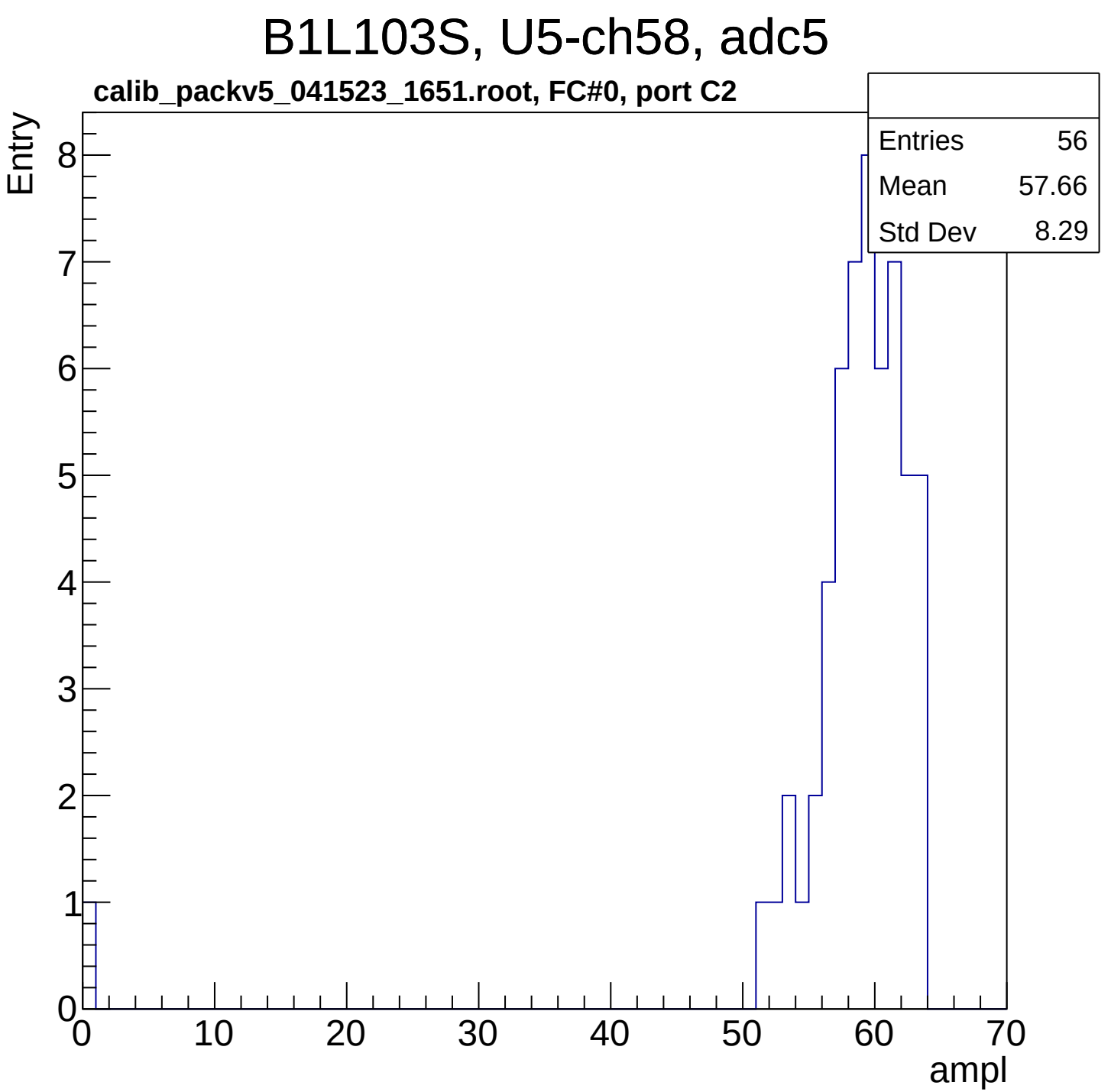
B1L103S, U5-ch58, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 57.66
Std Dev 8.29
Entry
ampl
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3
4
5
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7
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0
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40
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60
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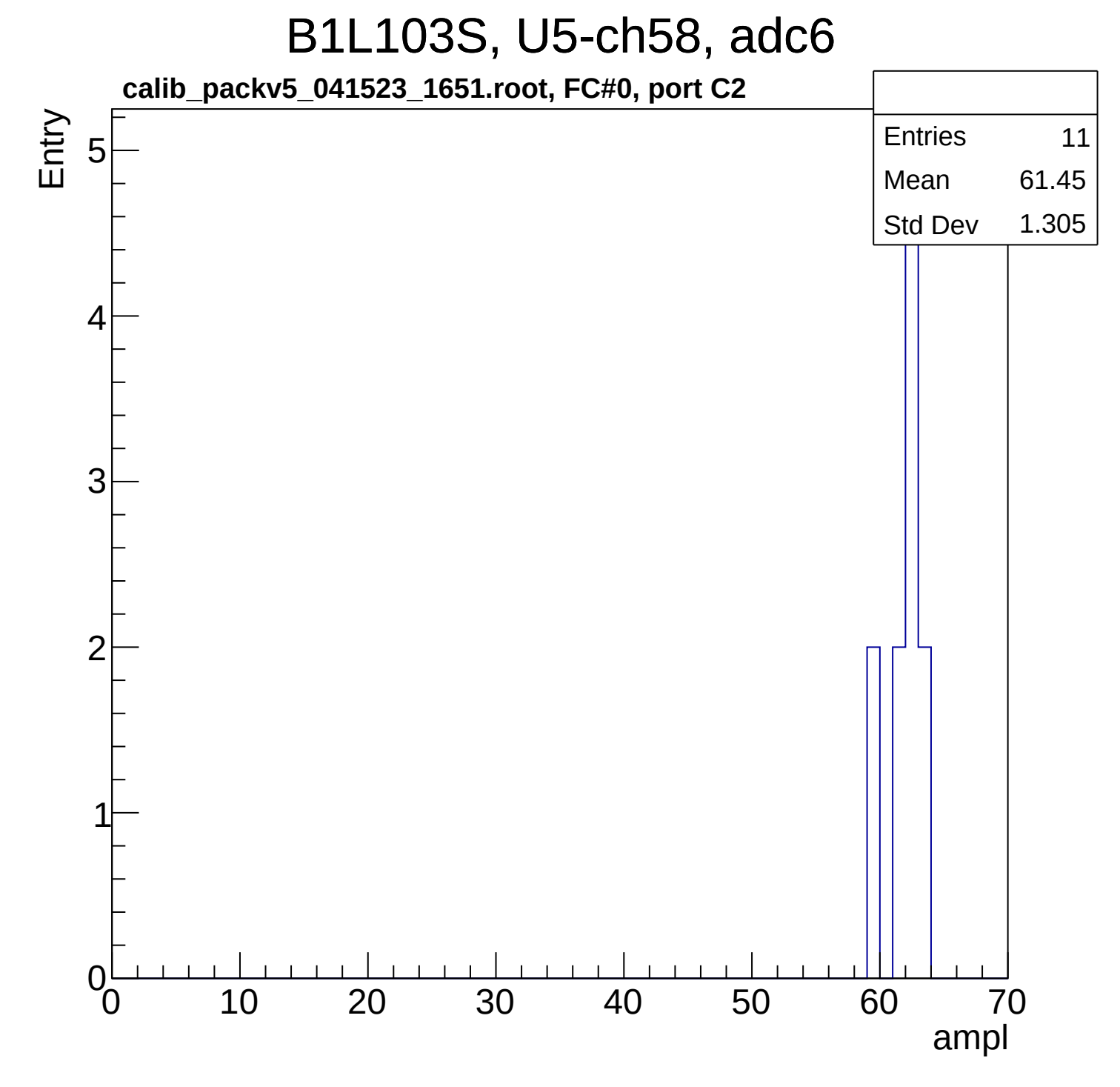
B1L103S, U5-ch58, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.45
Std Dev 1.305
Entry
ampl
0
1
2
3
4
5
0
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20
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40
50
60
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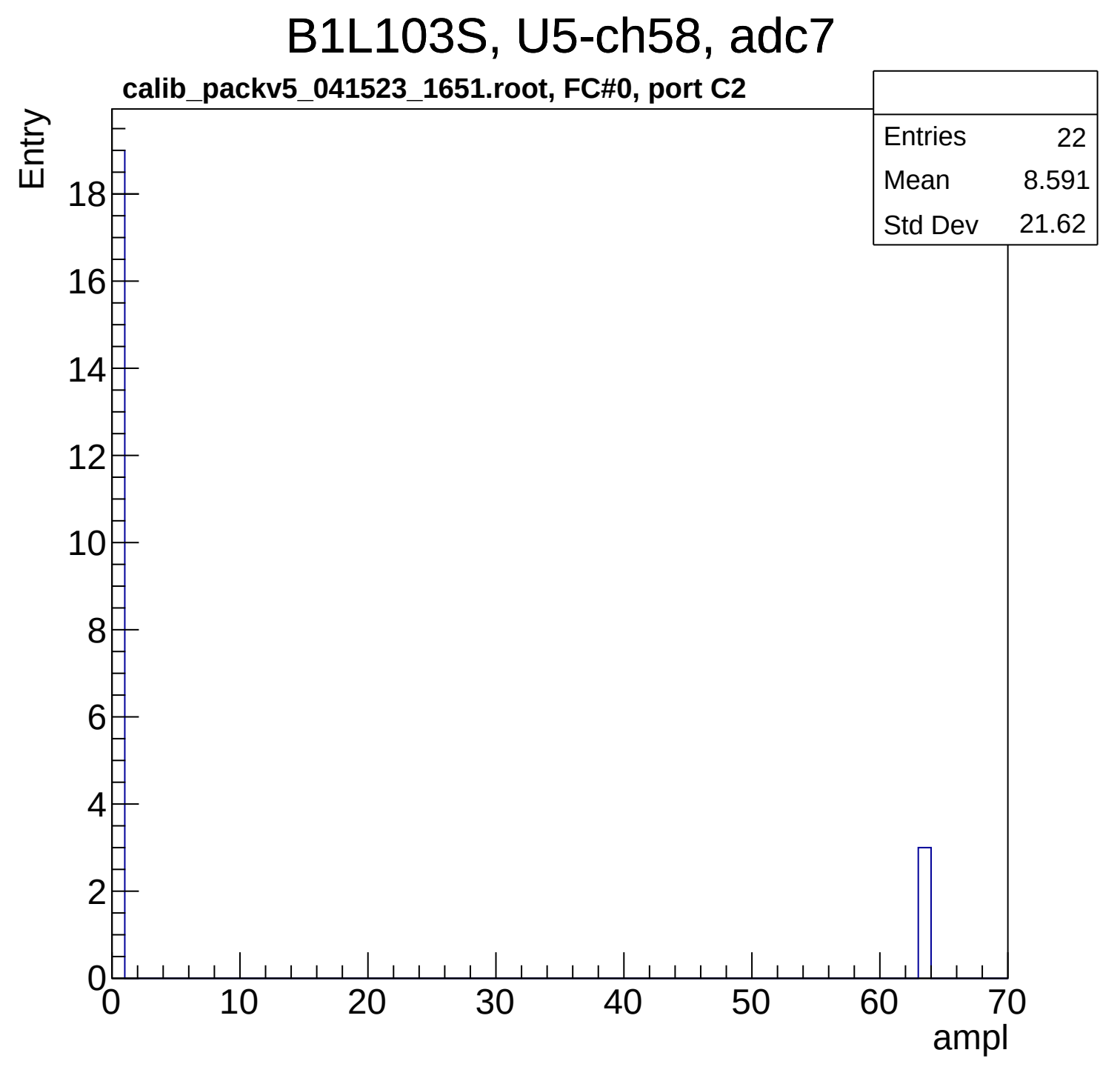
B1L103S, U5-ch58, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.591
Std Dev 21.62
Entry
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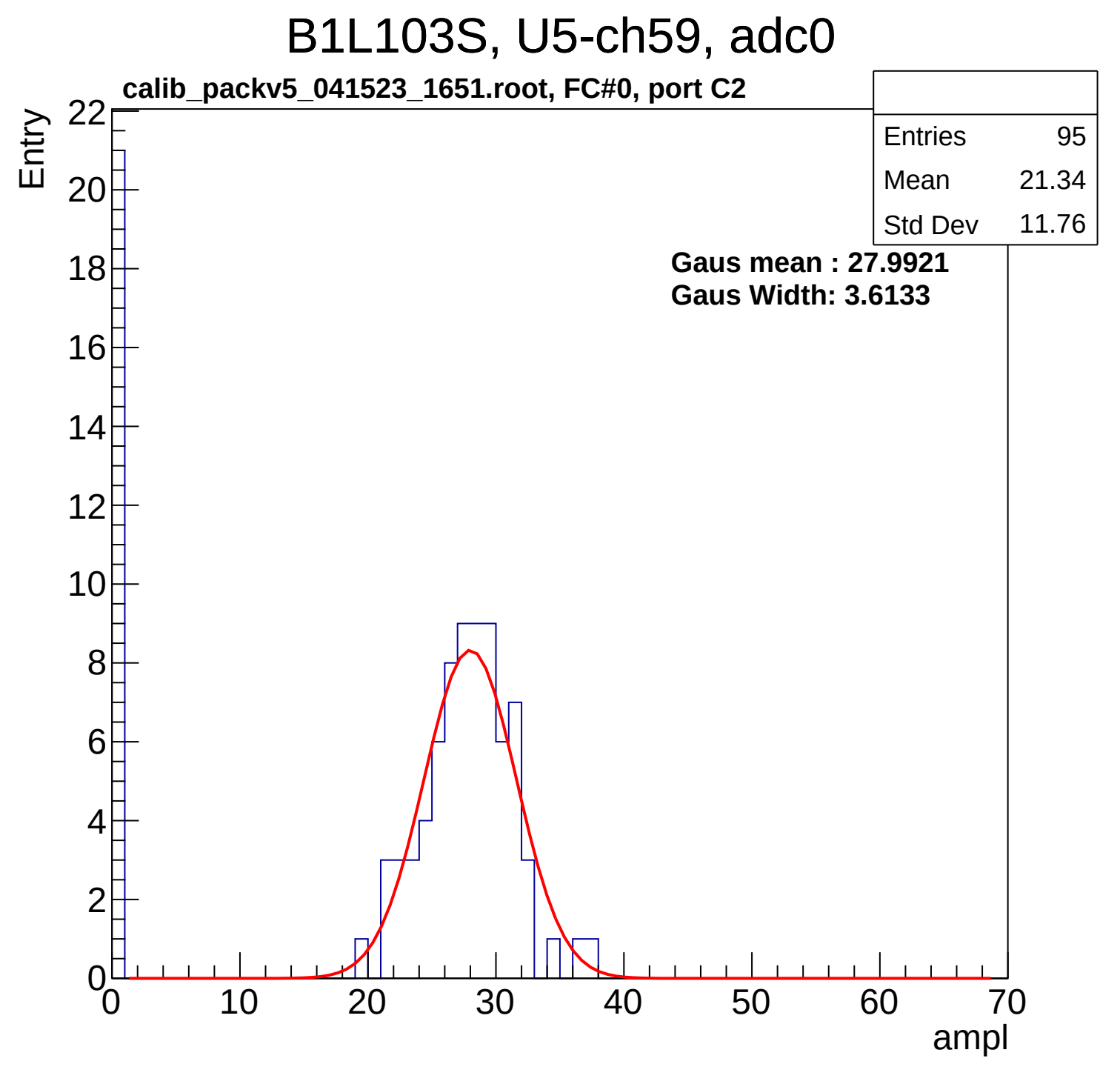
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch59, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 21.34
Std Dev 11.76
Gaus mean : 27.9921
Gaus Width: 3.6133
Entry
ampl
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2
4
6
8
10
12
14
16
18
20
22
0
10
20
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40
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60
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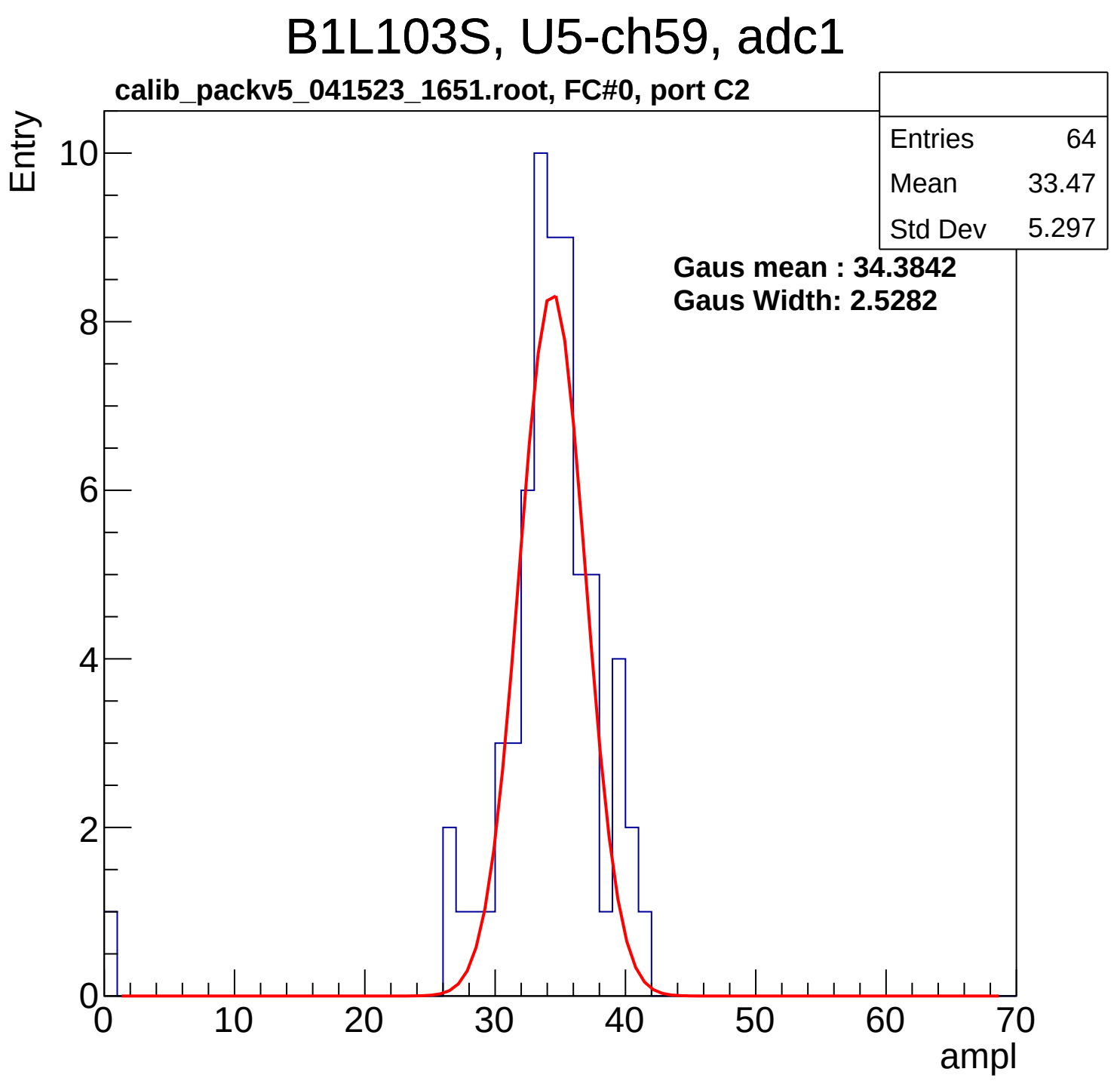
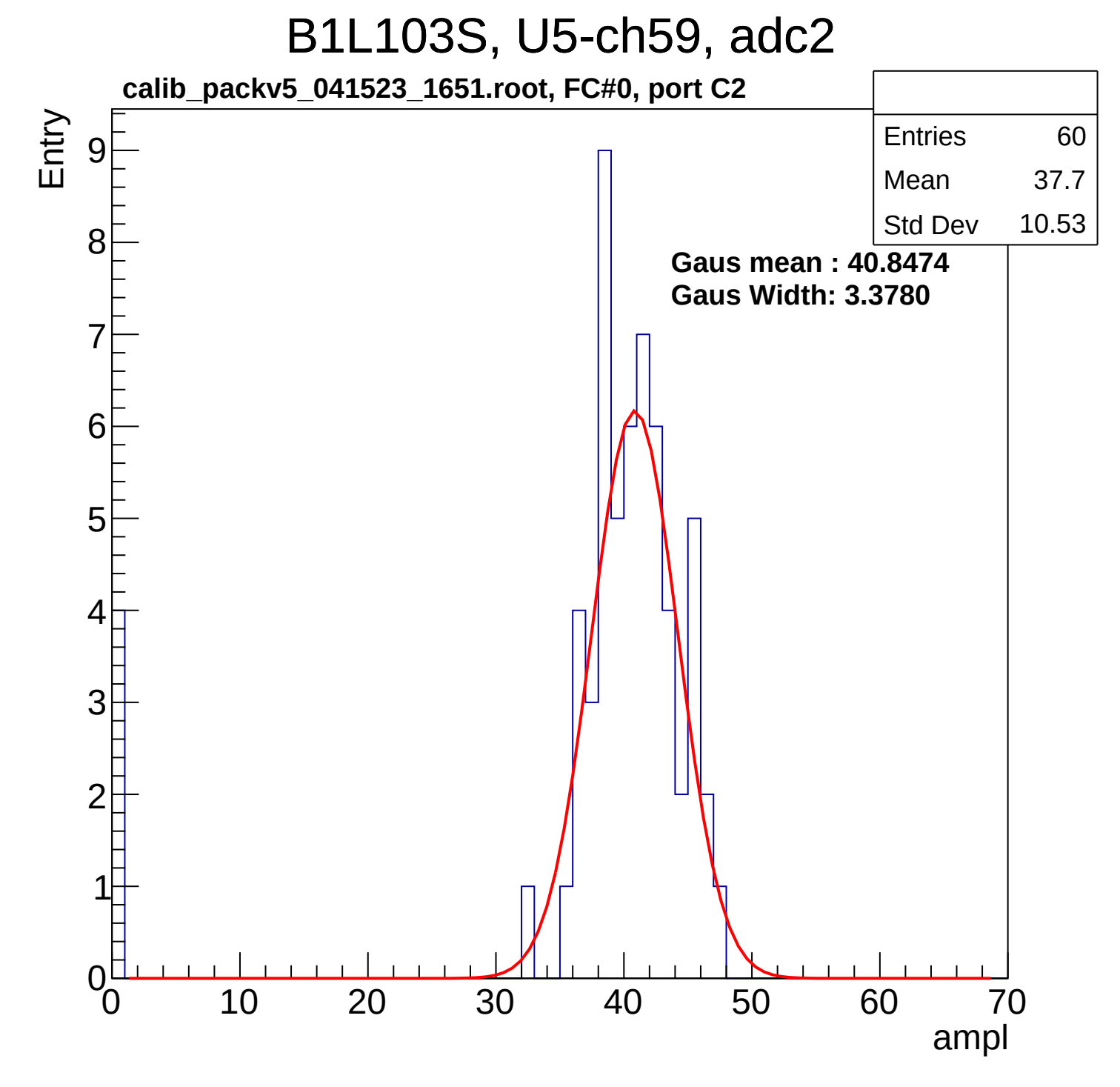

B1L103S, U5-ch59, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 33.47
Std Dev 5.297
Gaus mean : 34.3842
Gaus Width: 2.5282
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U5-ch59, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 37.7
Std Dev 10.53
Gaus mean : 40.8474
Gaus Width: 3.3780
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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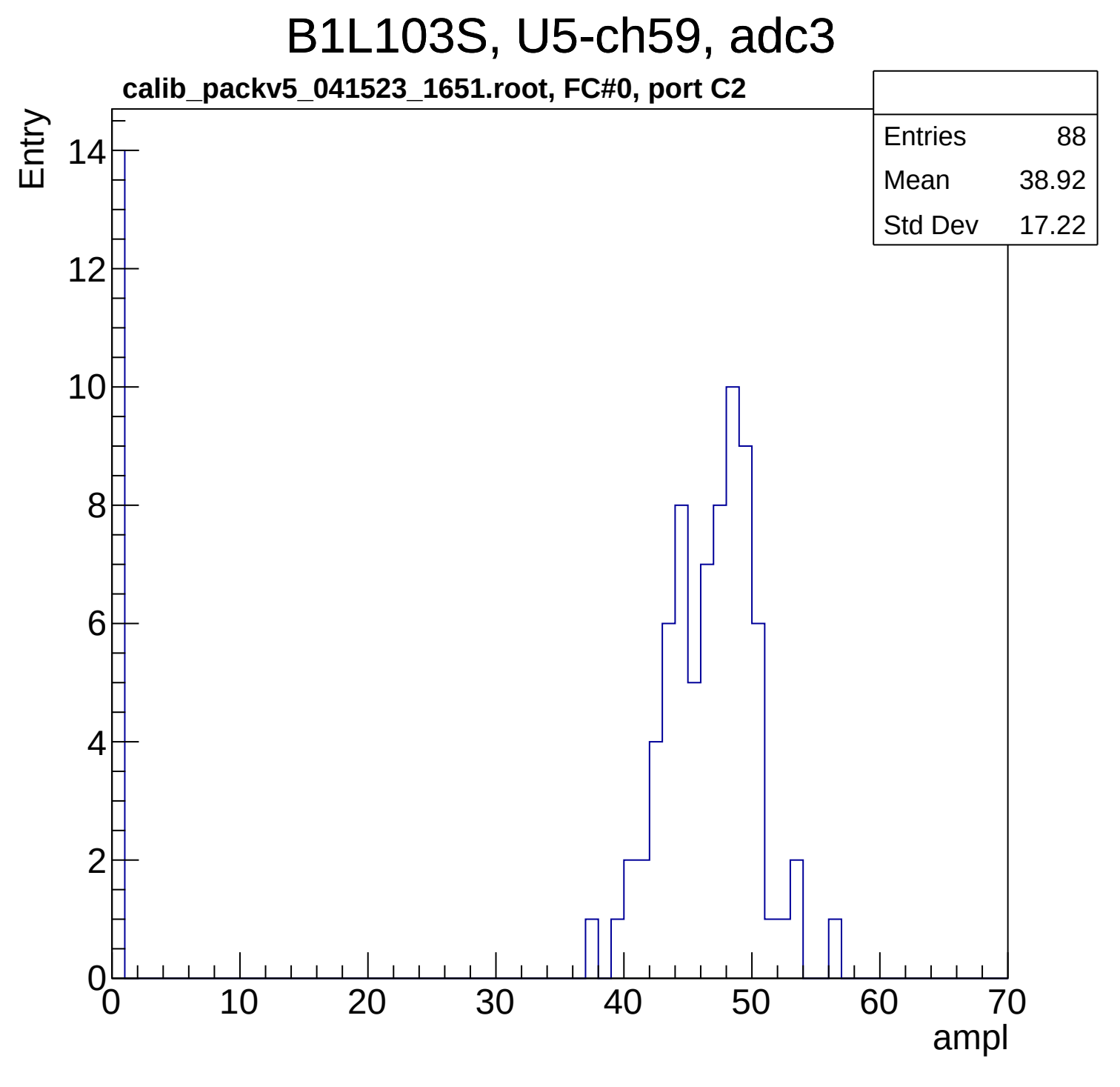
B1L103S, U5-ch59, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 38.92
Std Dev 17.22
Entry
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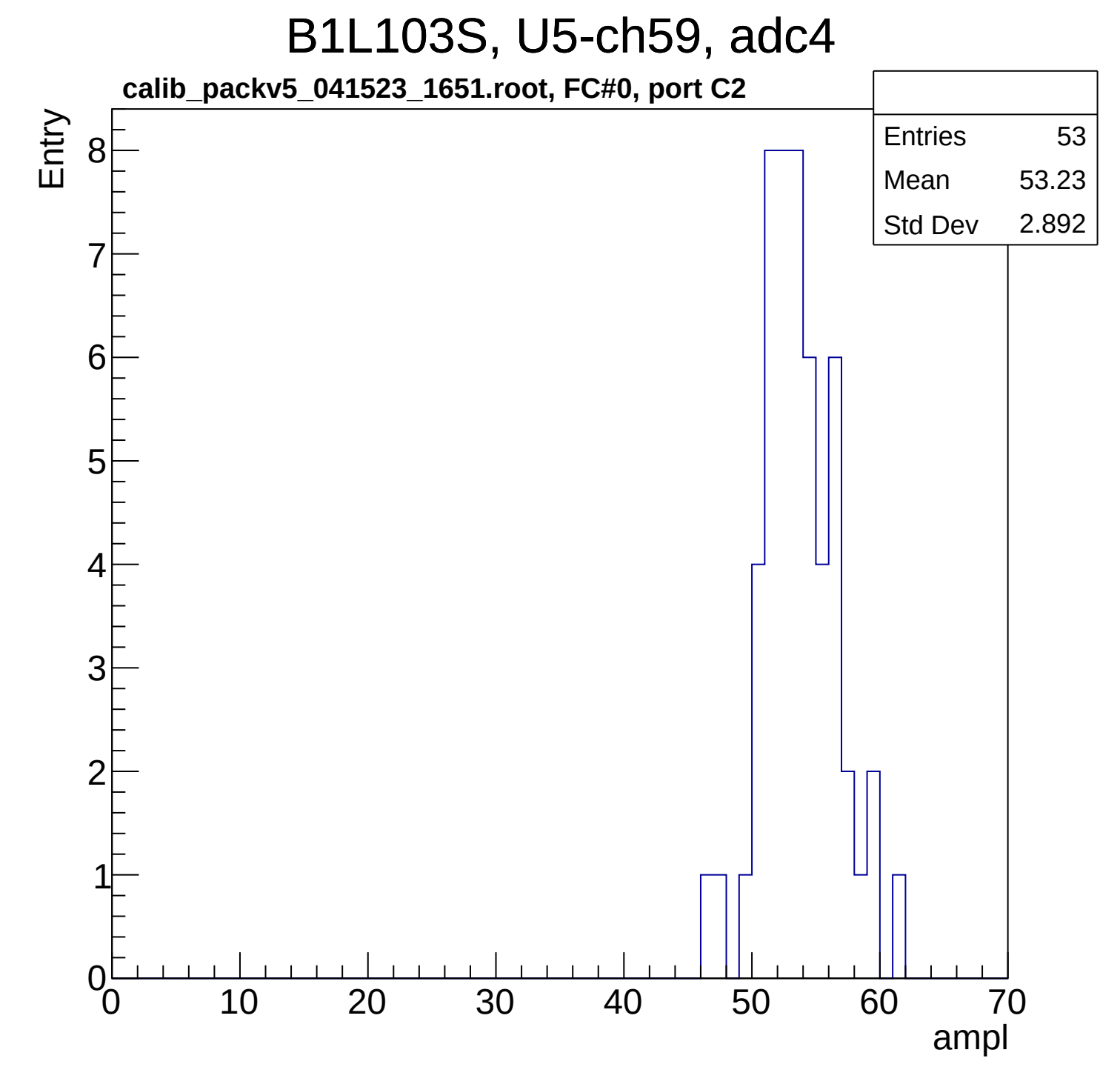
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch59, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 53.23
Std Dev 2.892
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
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60
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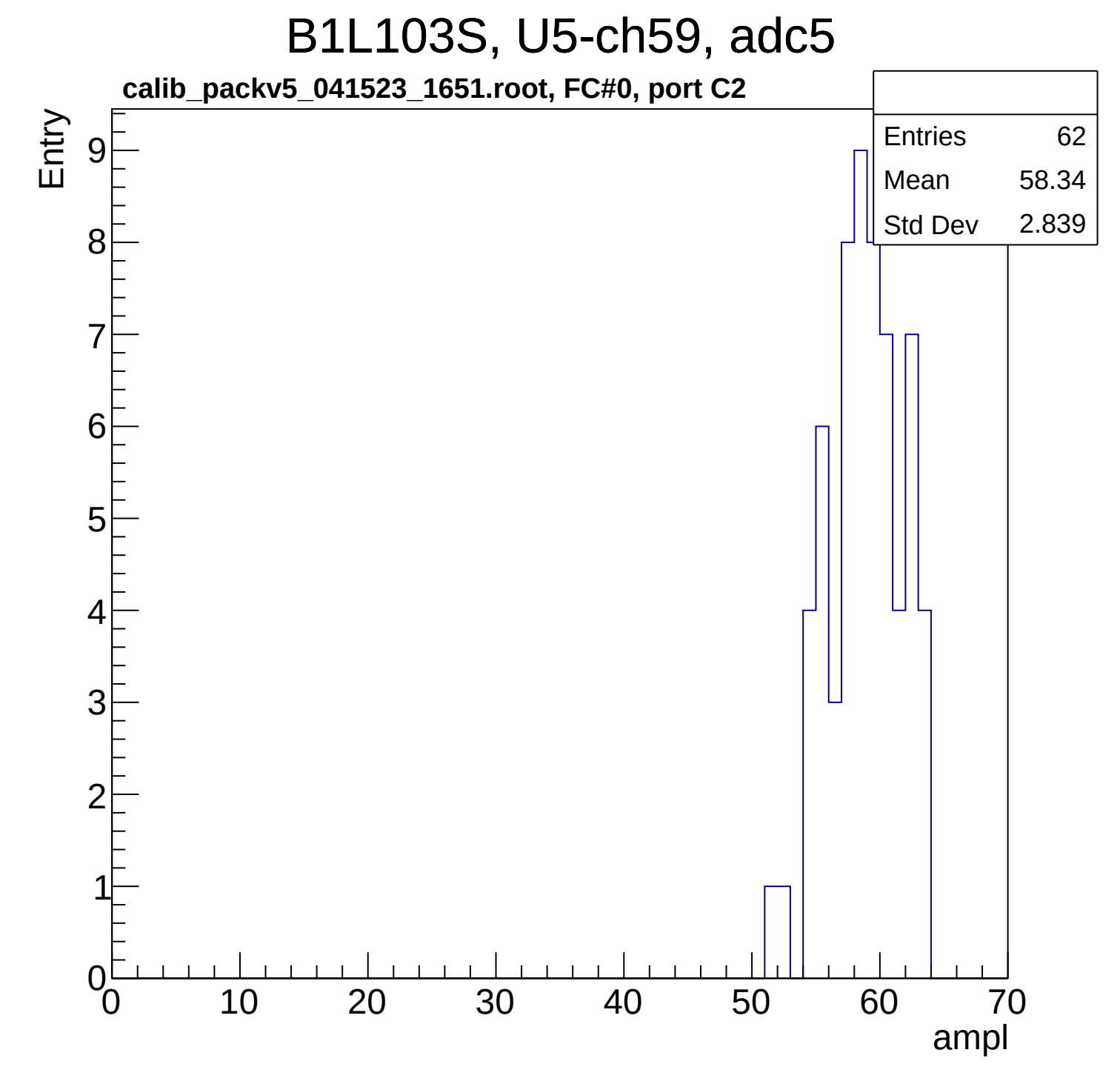
B1L103S, U5-ch59, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 58.34
Std Dev 2.839
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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60
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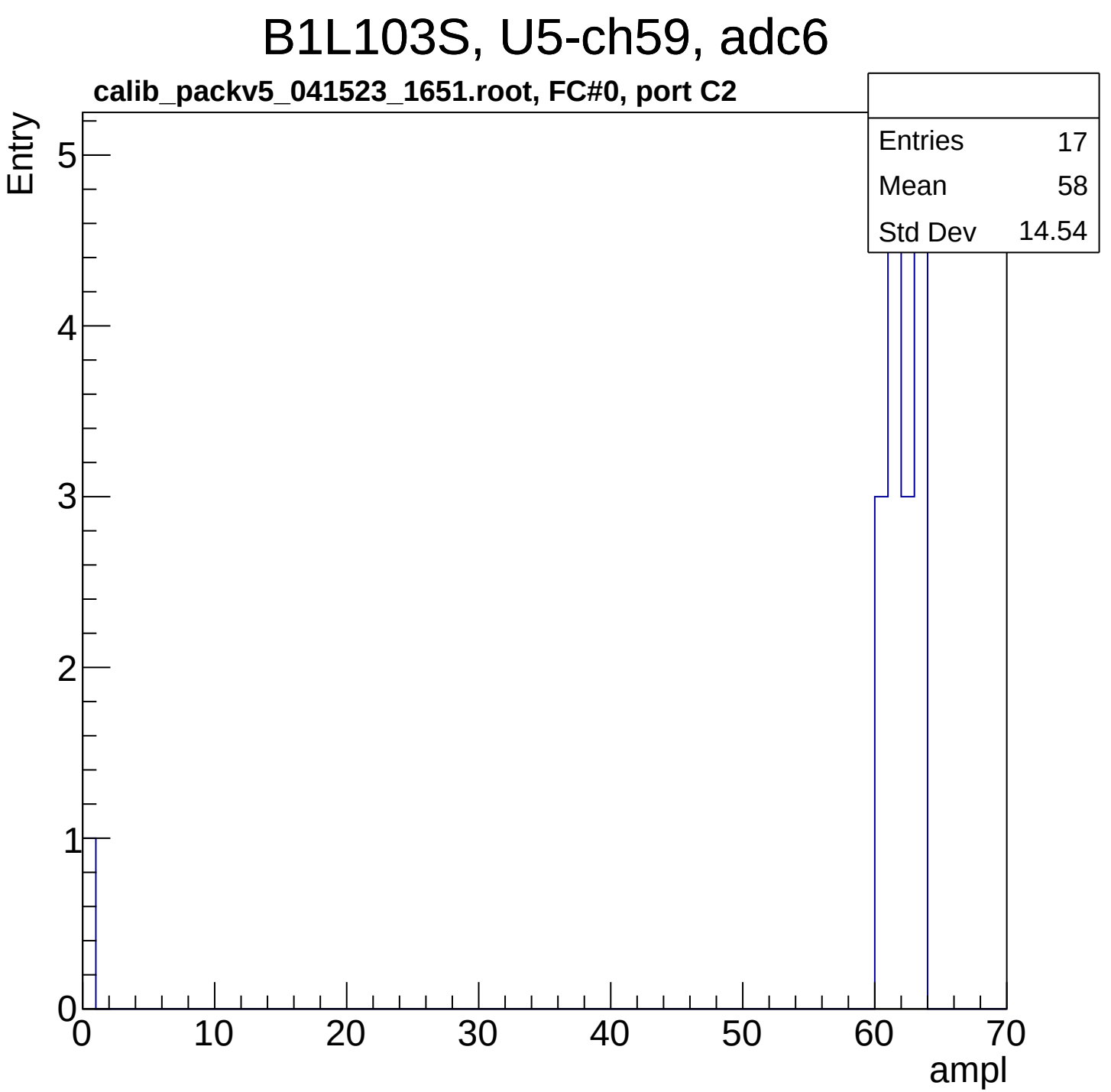
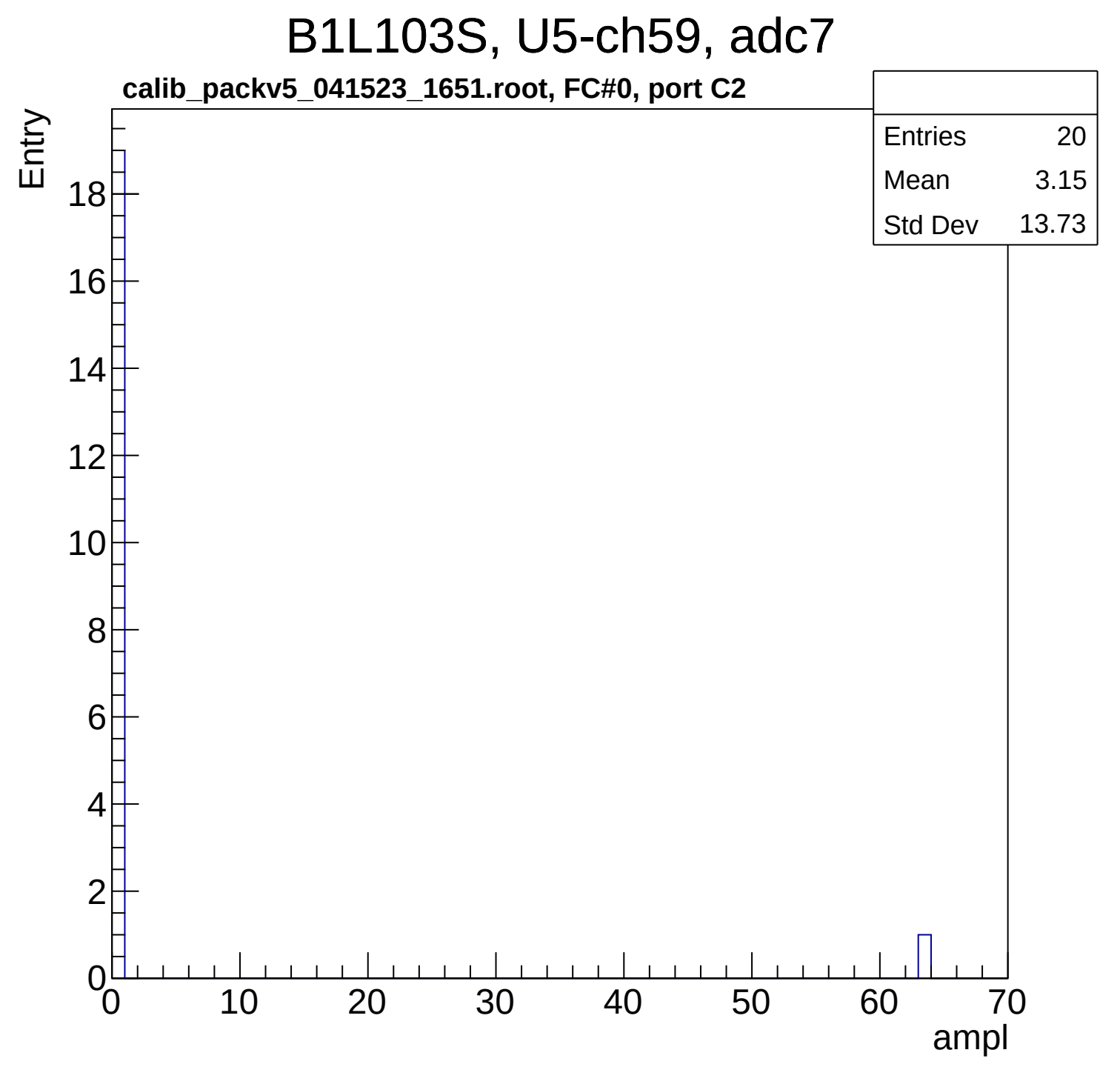
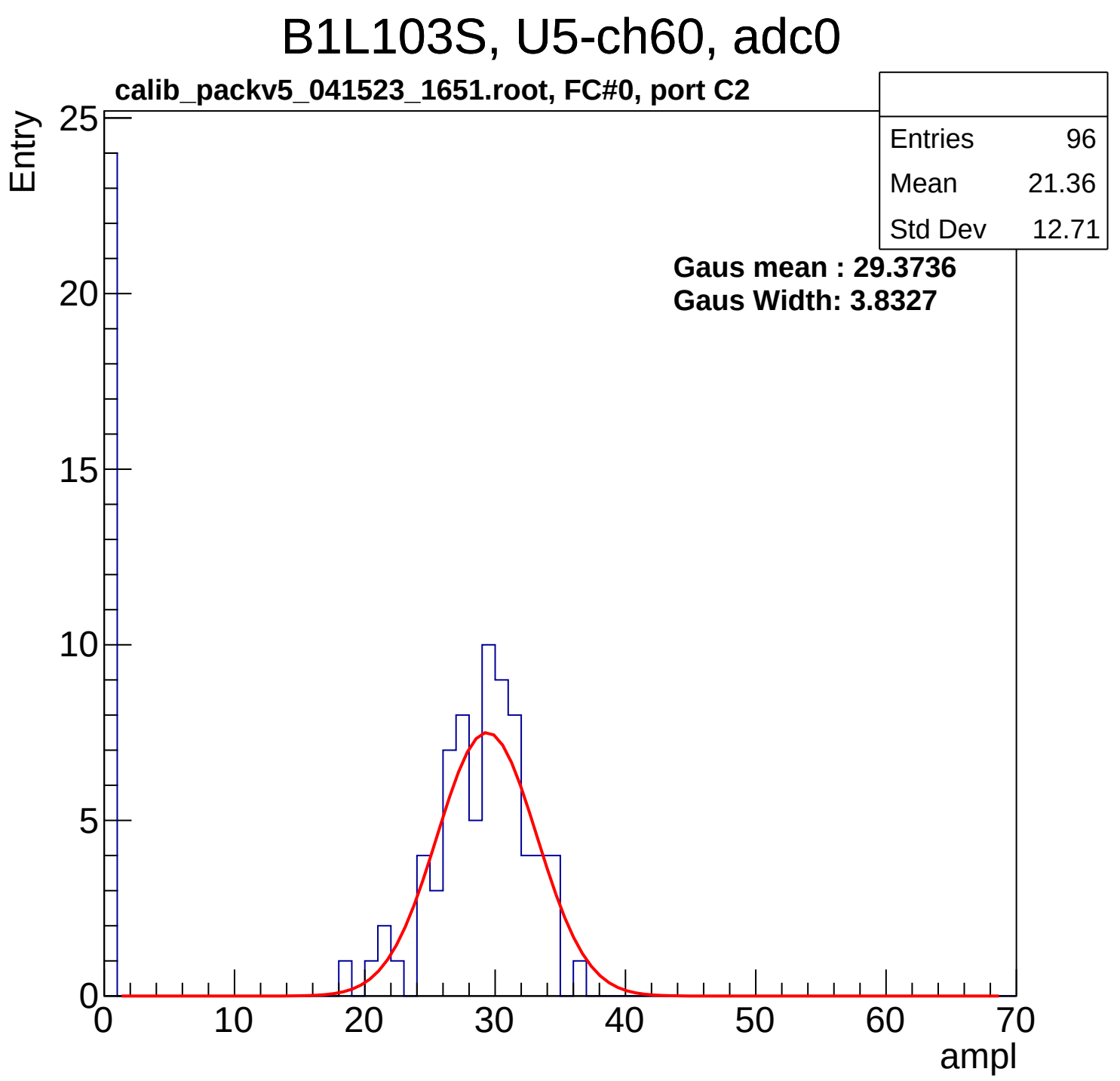
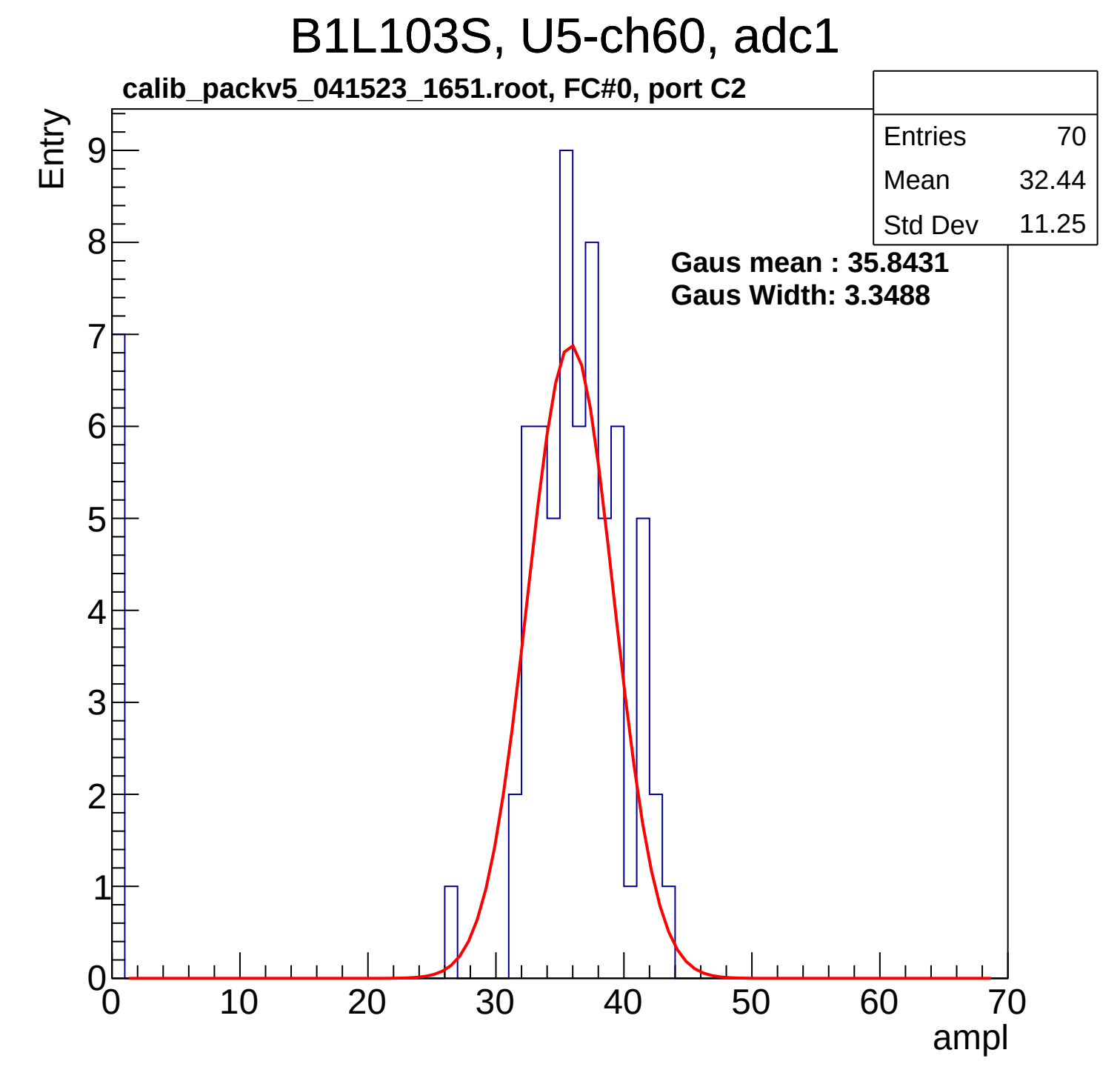

B1L103S, U5-ch59, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 58
Std Dev 14.54
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U5-ch59, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch60, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 21.36
Std Dev 12.71
Gaus mean : 29.3736
Gaus Width: 3.8327
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U5-ch60, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 32.44
Std Dev 11.25
Gaus mean : 35.8431
Gaus Width: 3.3488
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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60
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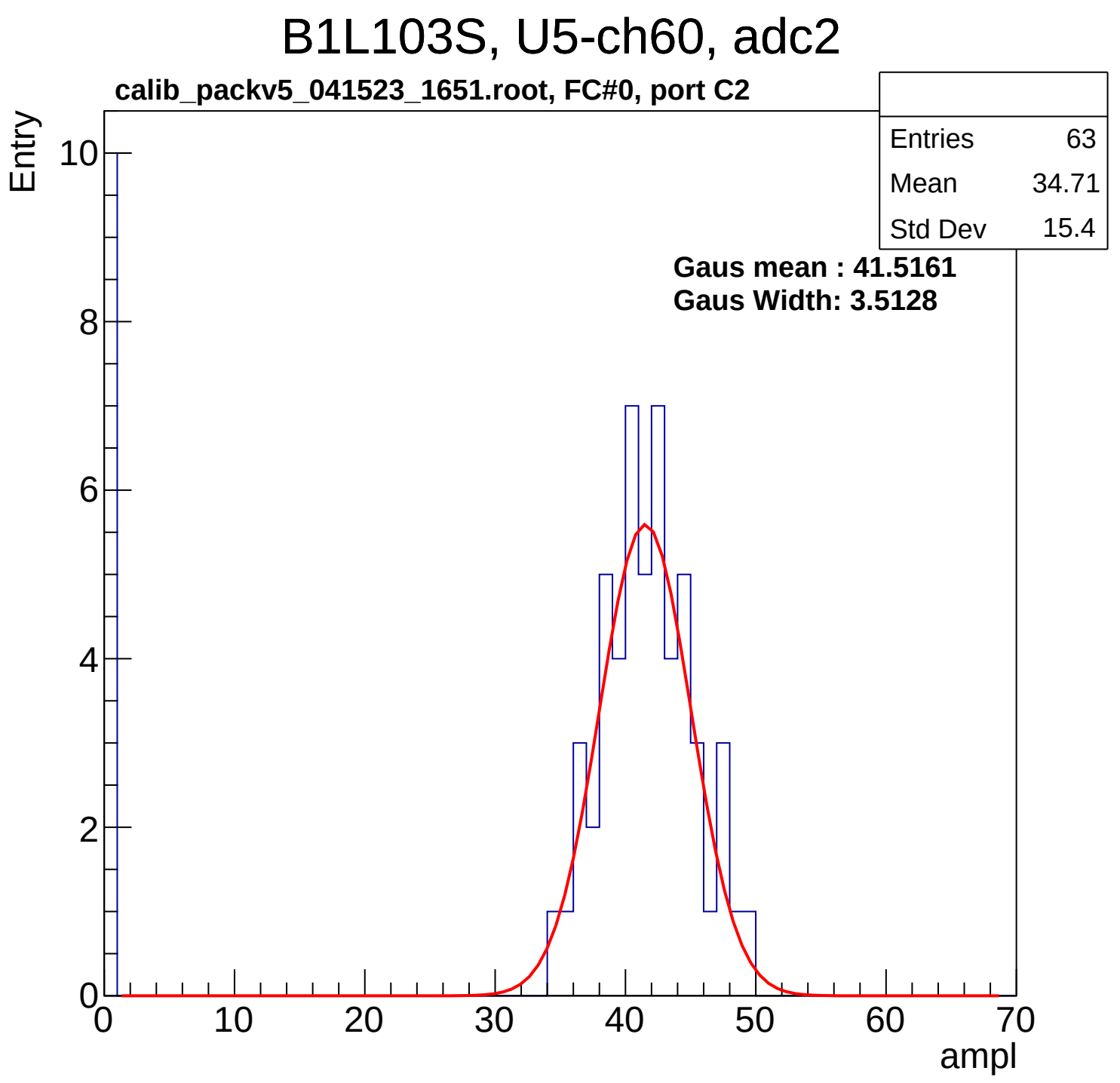
B1L103S, U5-ch60, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 34.71
Std Dev 15.4
Gaus mean : 41.5161
Gaus Width: 3.5128
Entry
ampl
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4
6
8
10
0
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20
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40
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60
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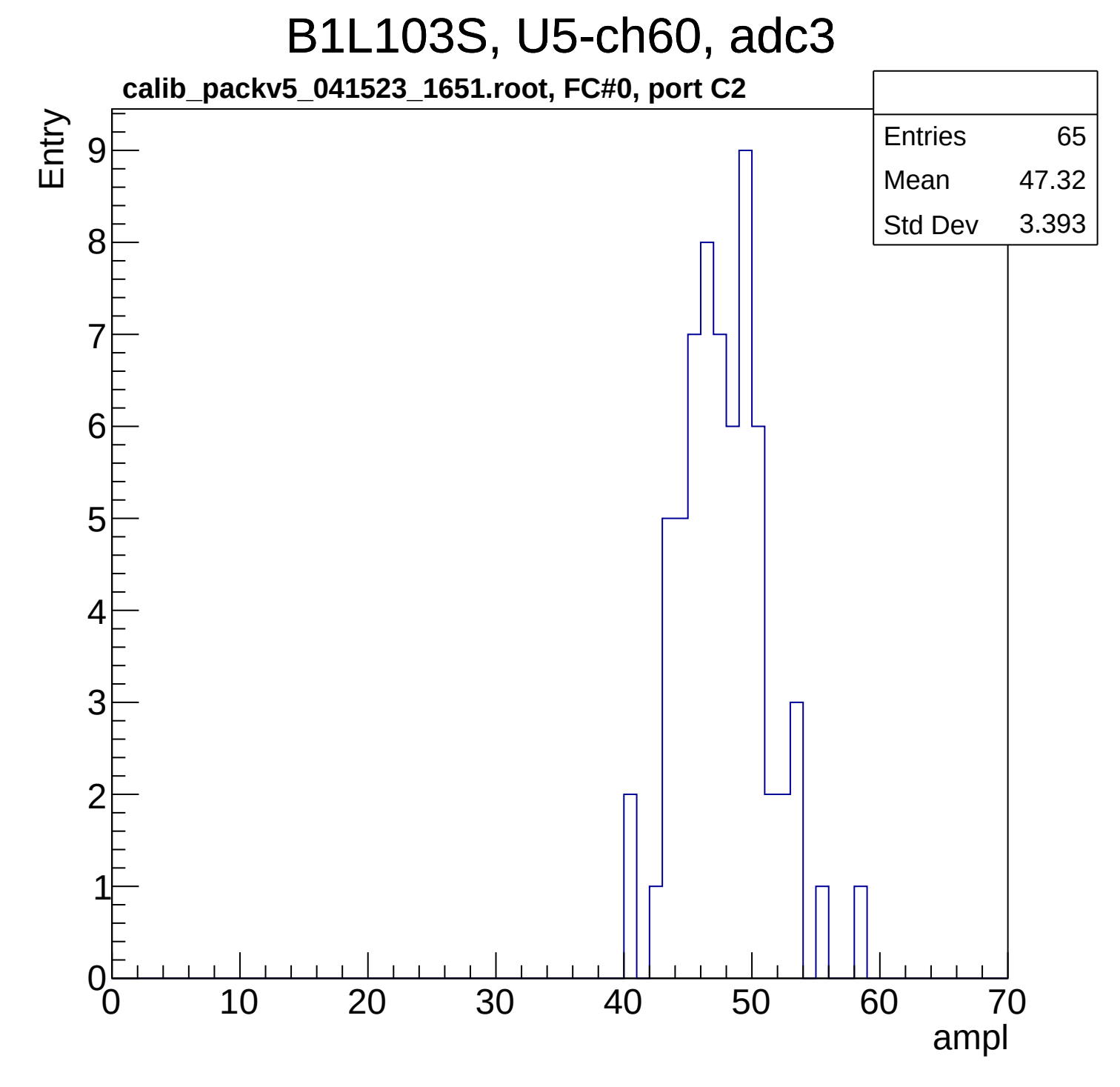
B1L103S, U5-ch60, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 47.32
Std Dev 3.393
Entry
ampl
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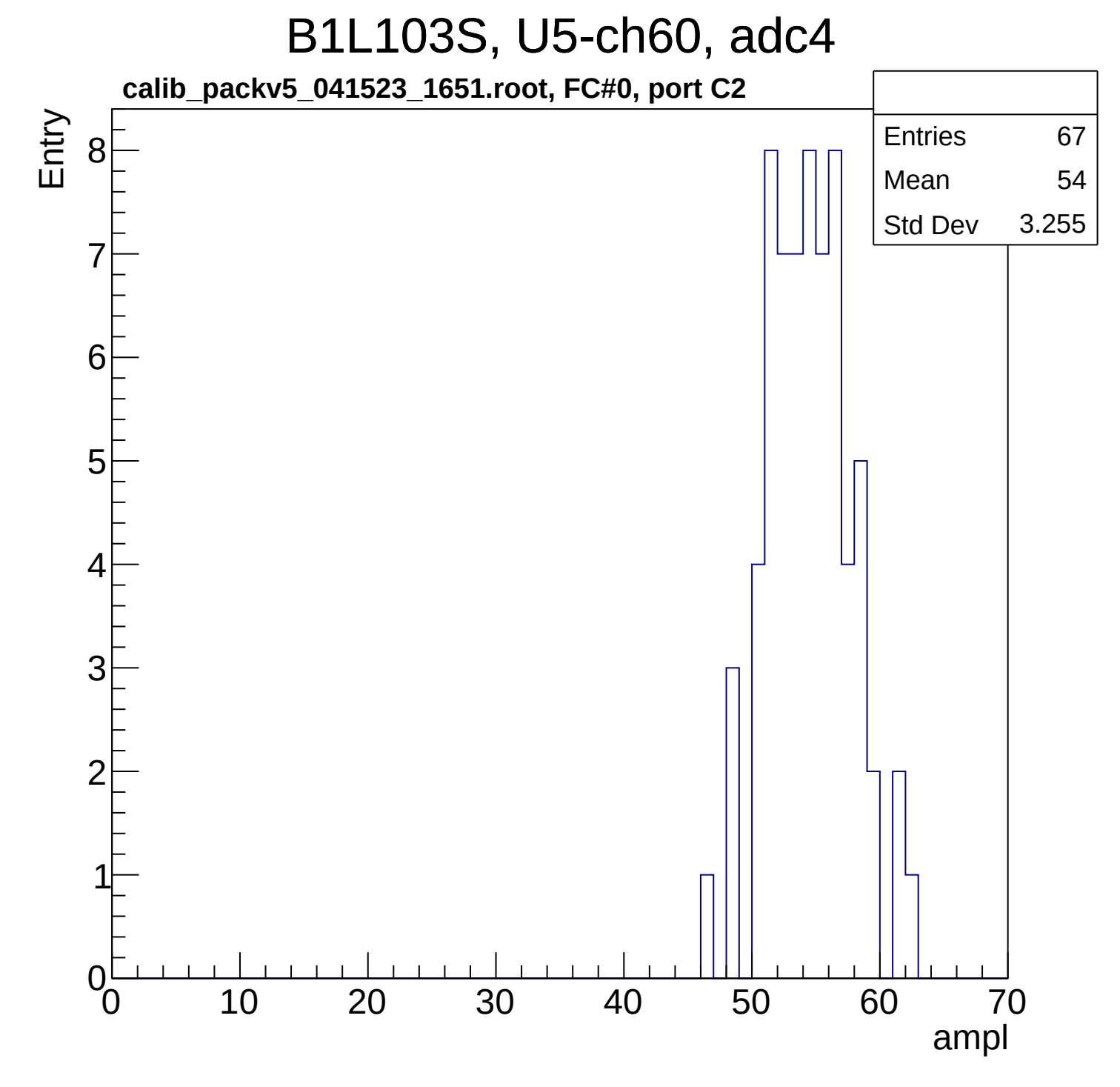
B1L103S, U5-ch60, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 54
Std Dev 3.255
Entry
ampl
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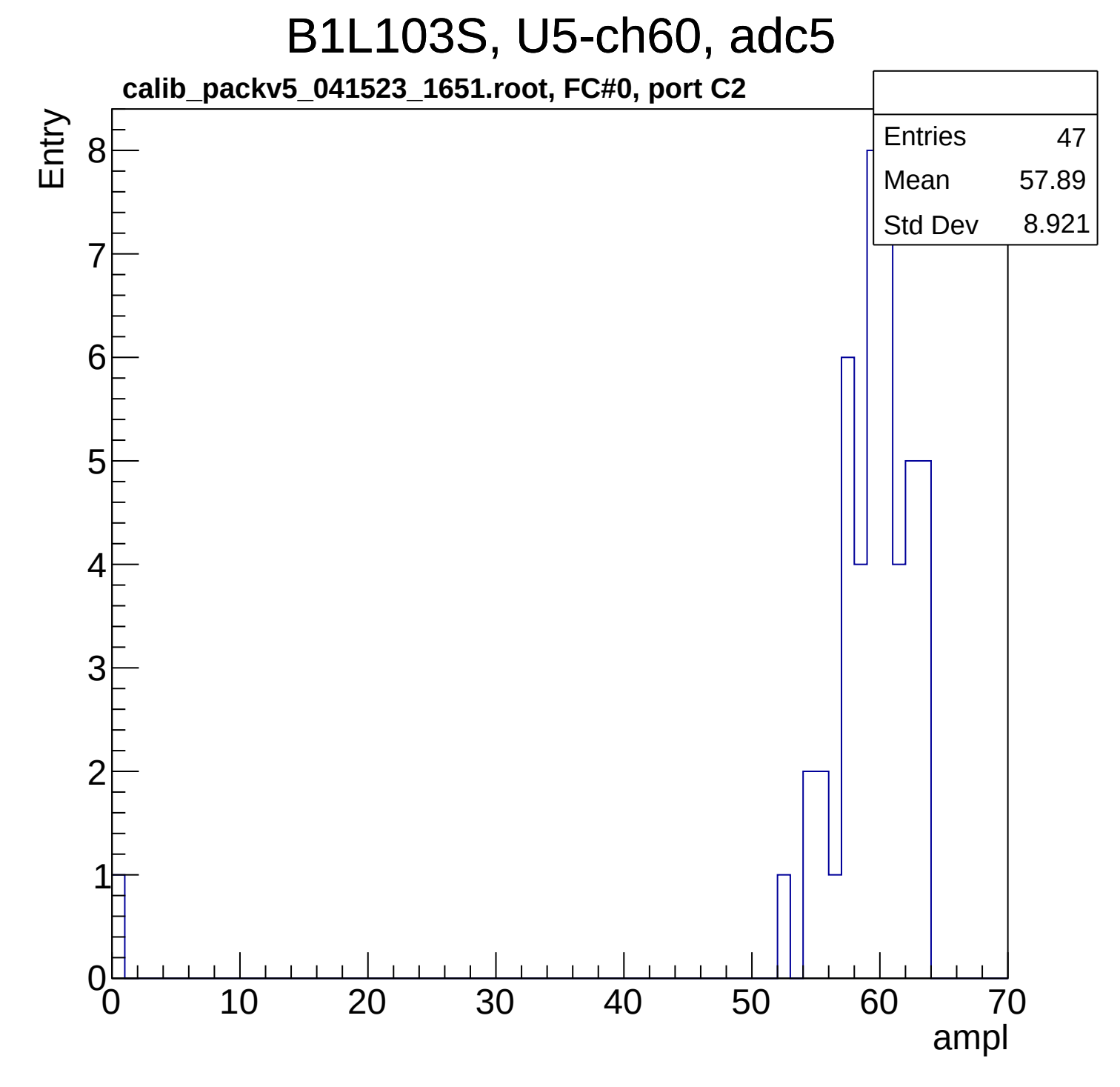
B1L103S, U5-ch60, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 57.89
Std Dev 8.921
Entry
ampl
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0
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60
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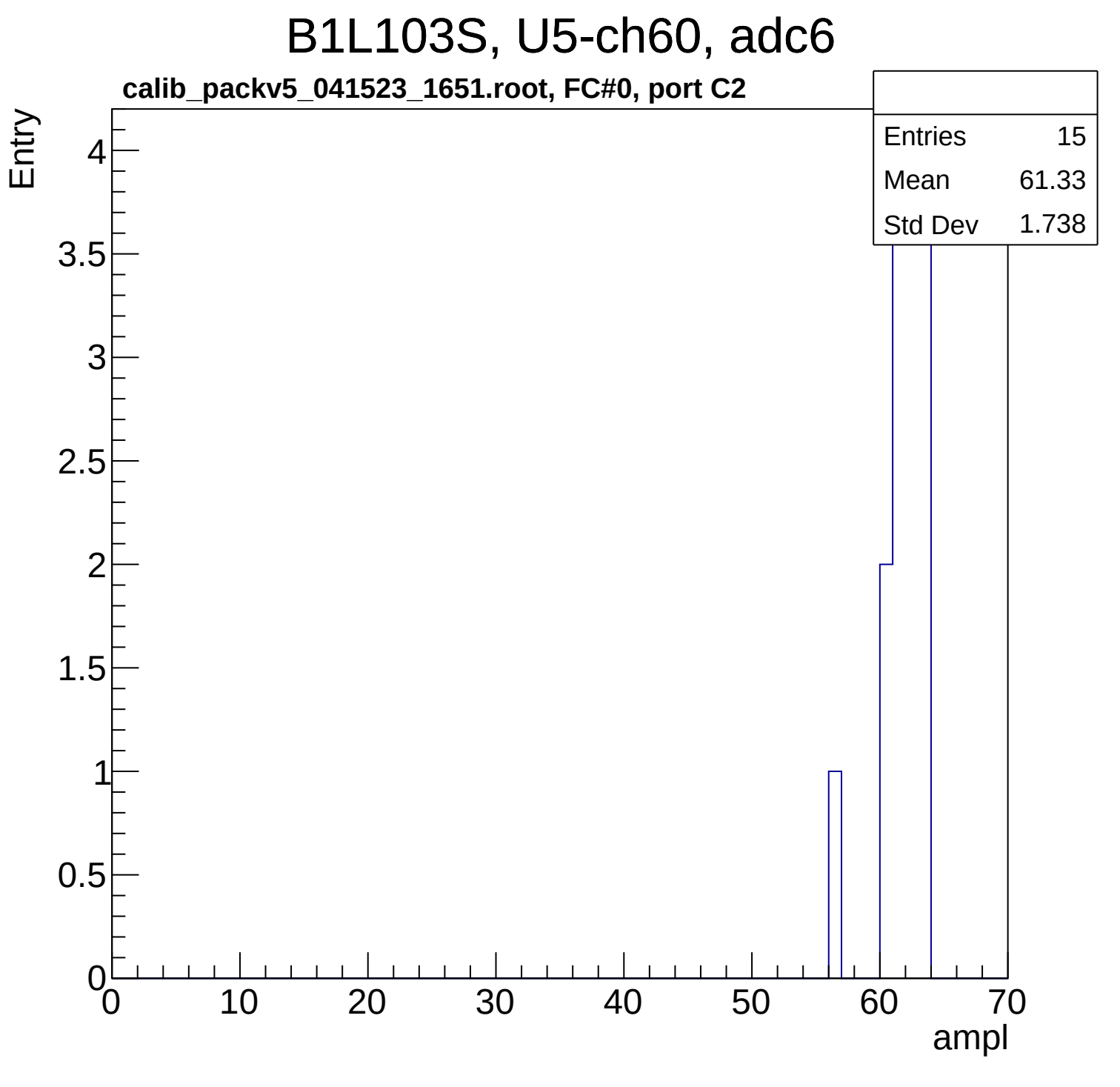
B1L103S, U5-ch60, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.33
Std Dev 1.738
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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60
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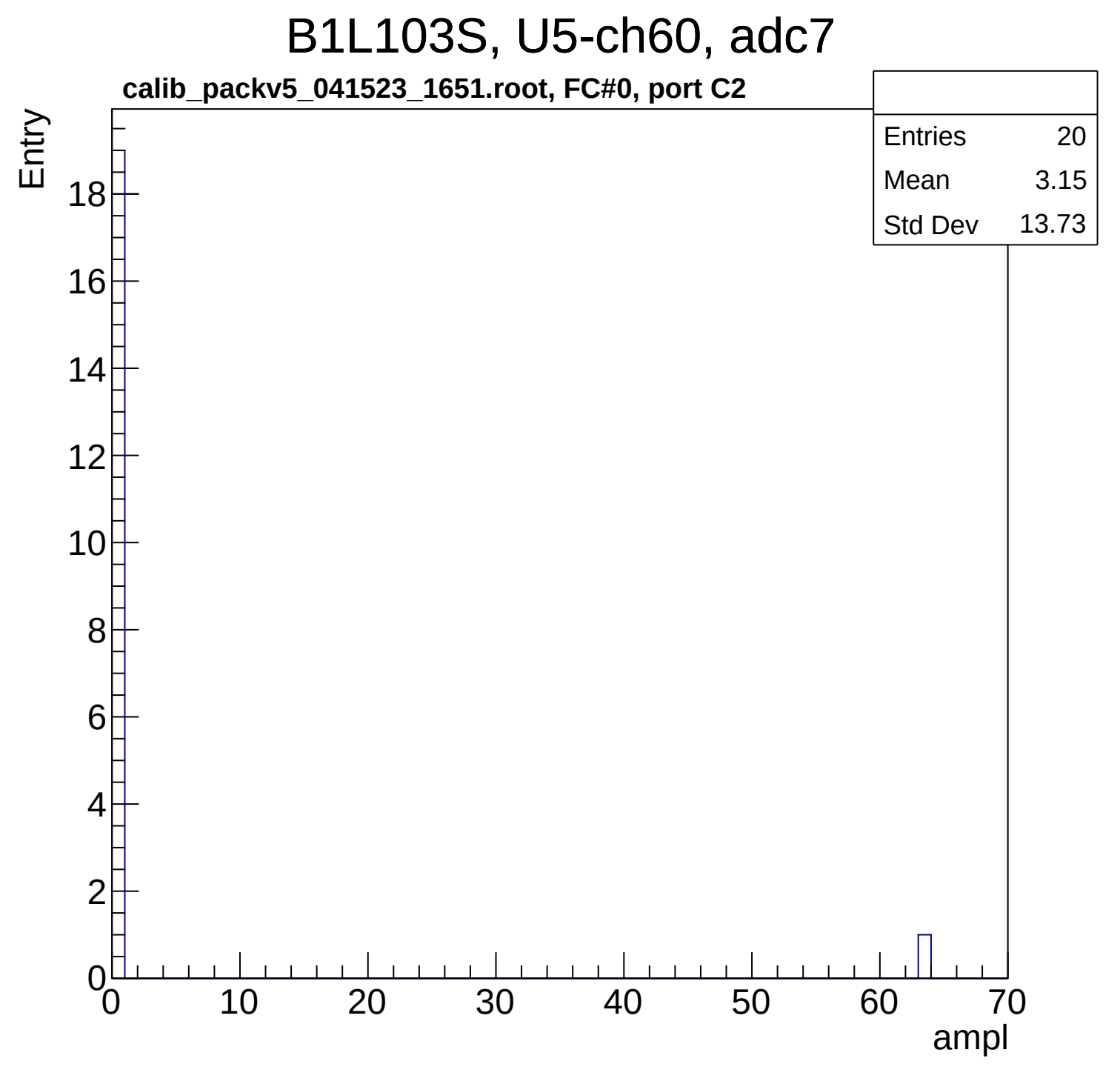
B1L103S, U5-ch60, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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6
8
10
12
14
16
18
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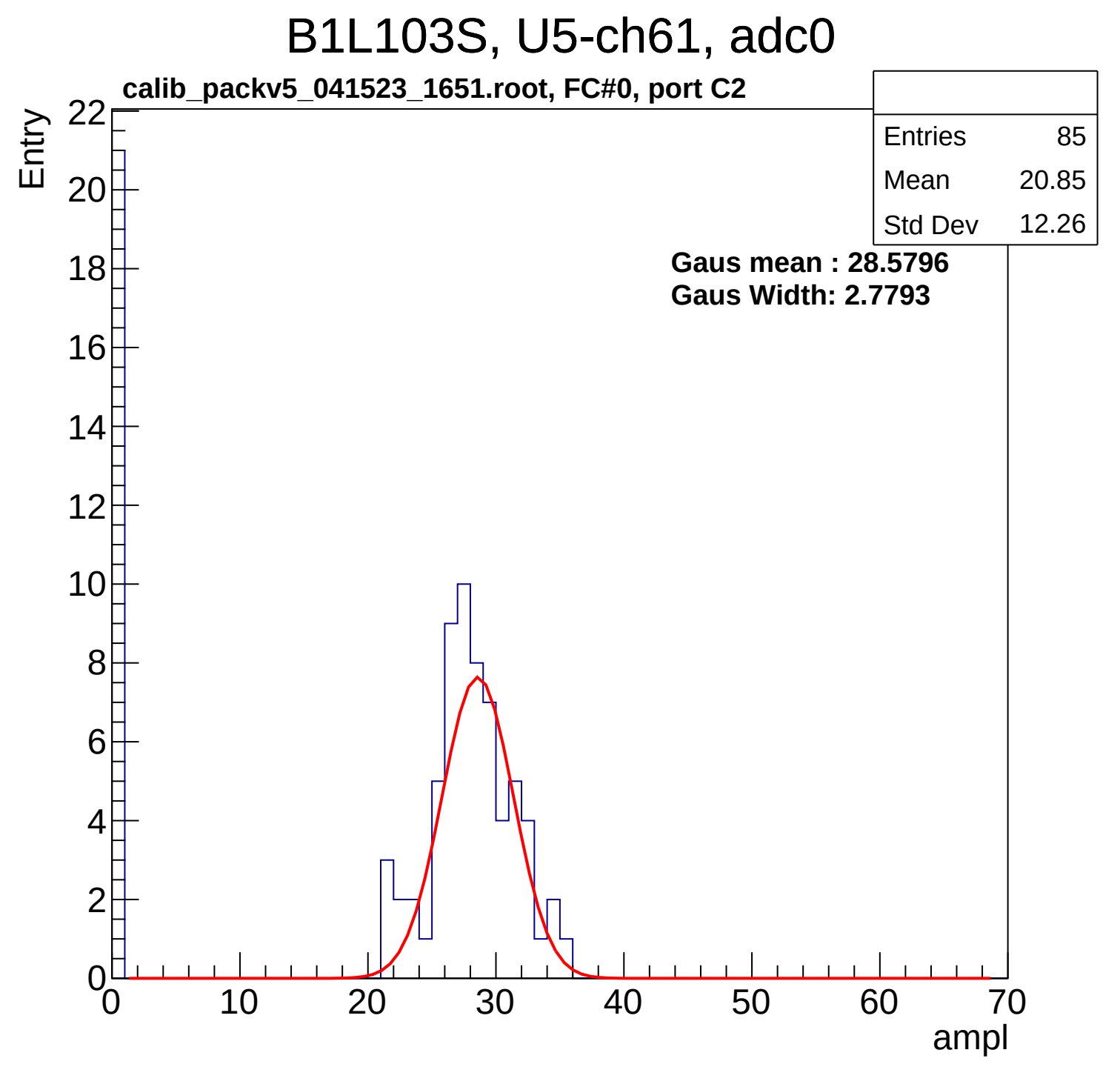
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch61, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 20.85
Std Dev 12.26
Gaus mean : 28.5796
Gaus Width: 2.7793
Entry
ampl
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8
10
12
14
16
18
20
22
0
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60
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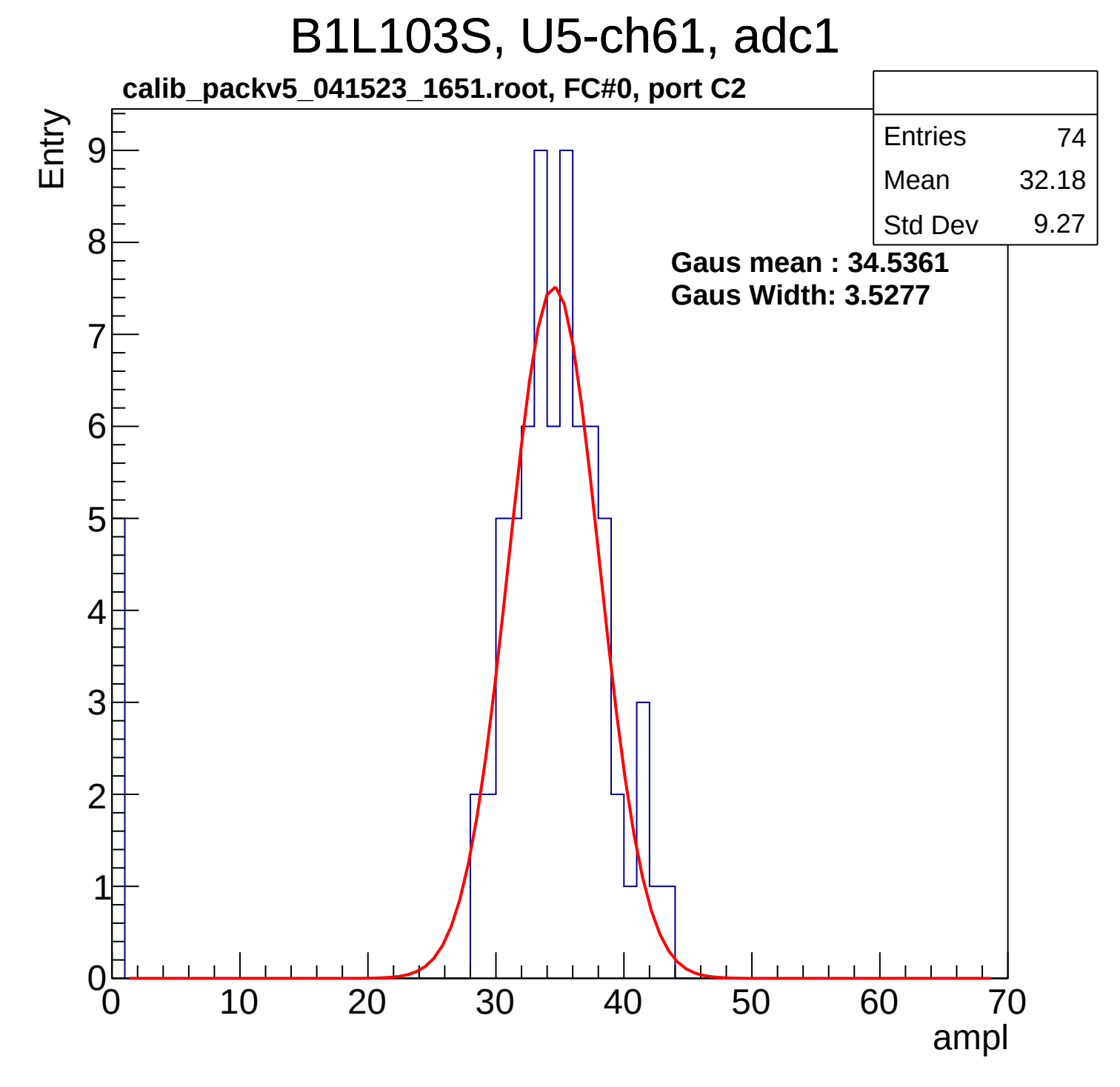
B1L103S, U5-ch61, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 32.18
Std Dev 9.27
Gaus mean : 34.5361
Gaus Width: 3.5277
Entry
ampl
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2
3
4
5
6
7
8
9
0
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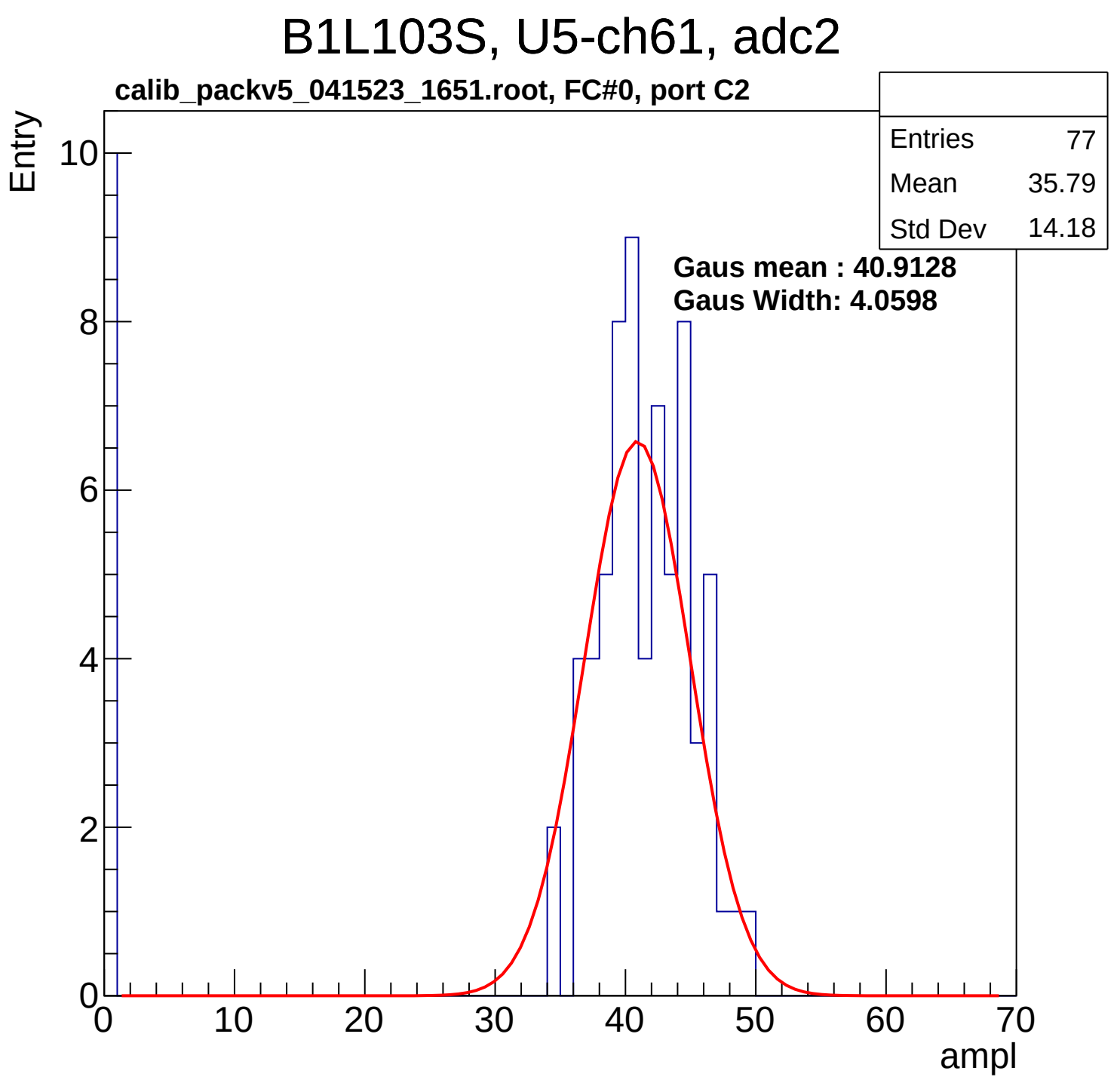
B1L103S, U5-ch61, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 35.79
Std Dev 14.18
Gaus mean : 40.9128
Gaus Width: 4.0598
Entry
ampl
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4
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8
10
0
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20
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40
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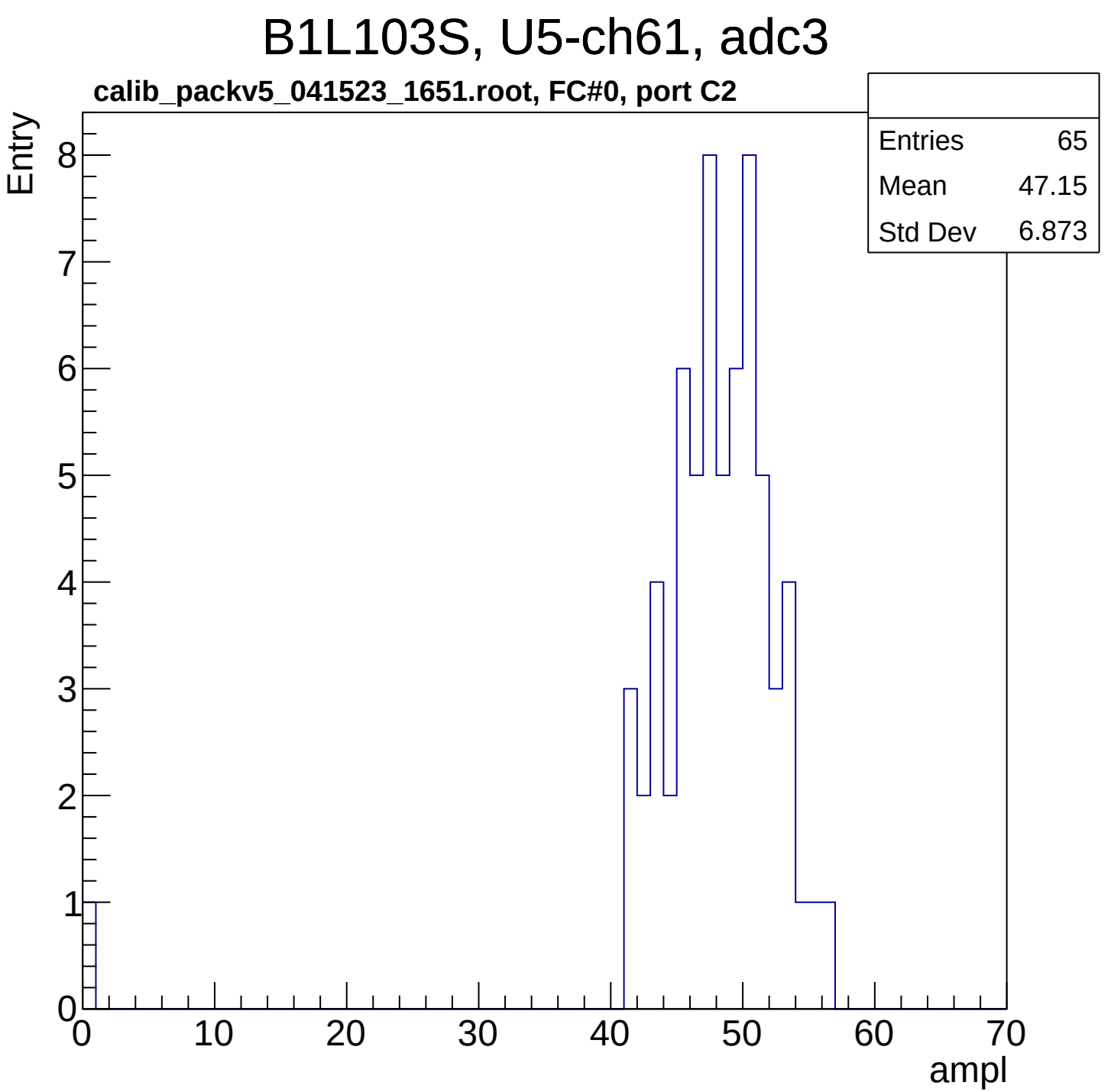
B1L103S, U5-ch61, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 47.15
Std Dev 6.873
Entry
ampl
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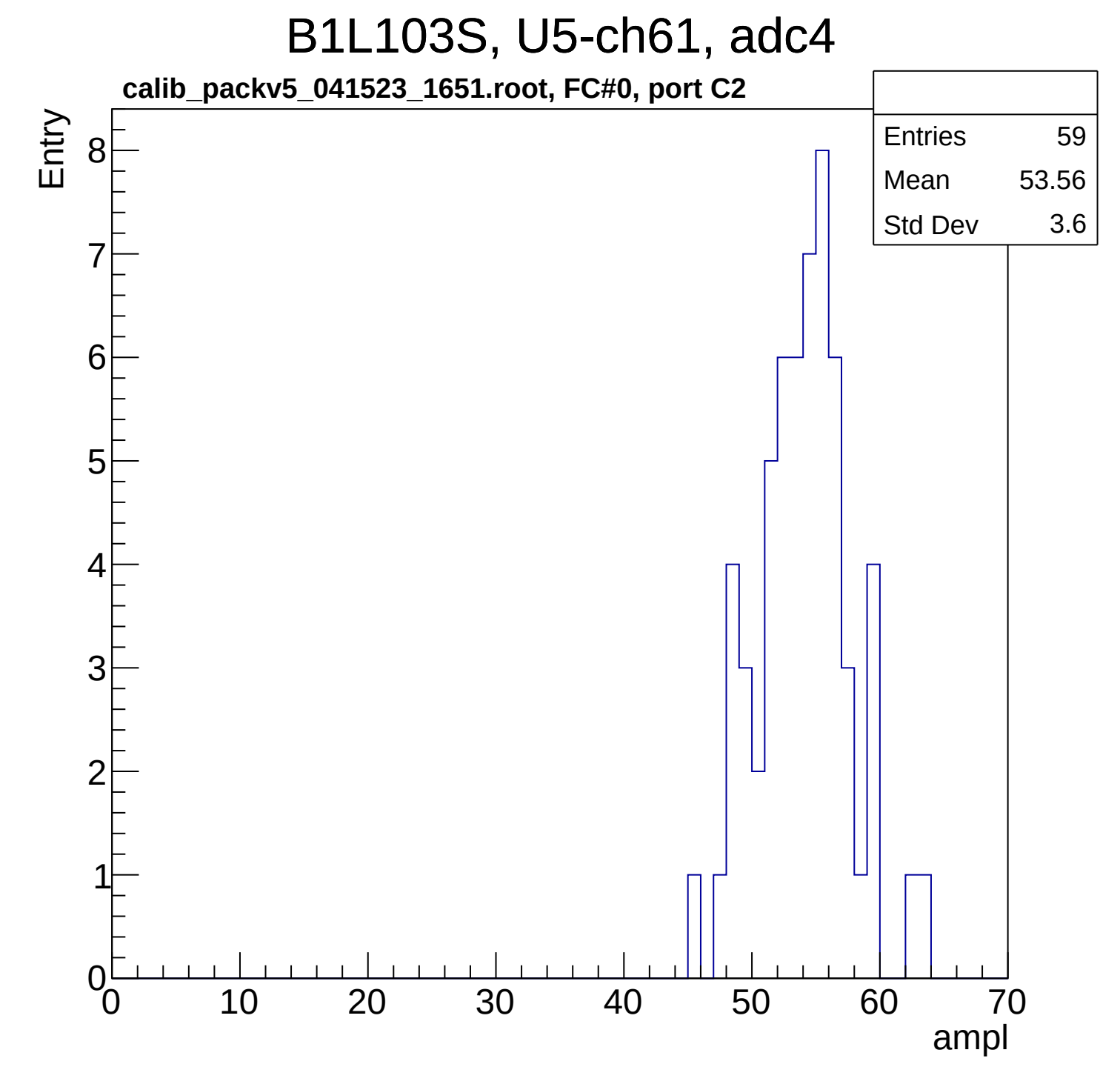
B1L103S, U5-ch61, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 53.56
Std Dev 3.6
Entry
ampl
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6
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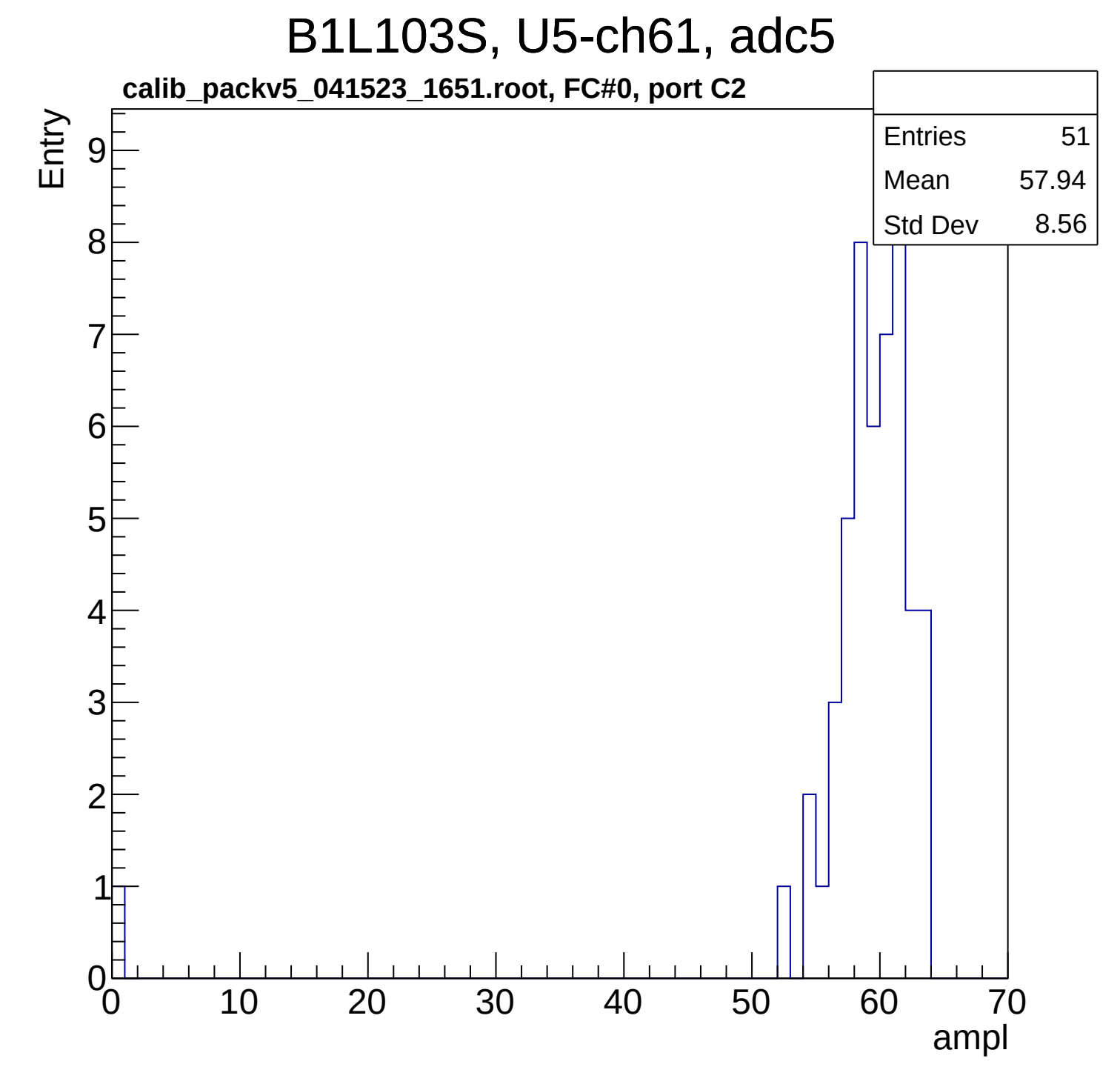
B1L103S, U5-ch61, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 57.94
Std Dev 8.56
Entry
ampl
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3
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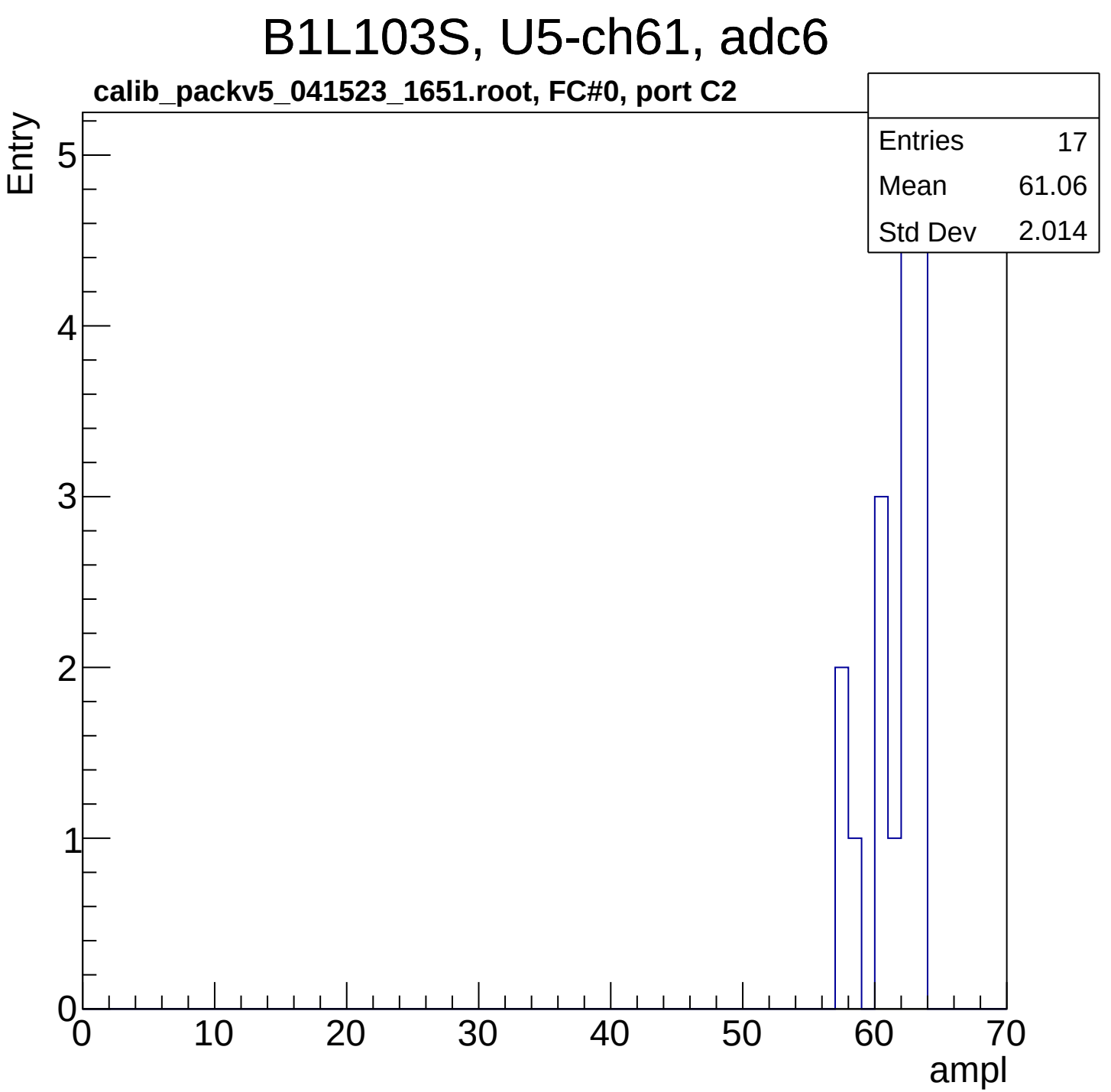
B1L103S, U5-ch61, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.06
Std Dev 2.014
Entry
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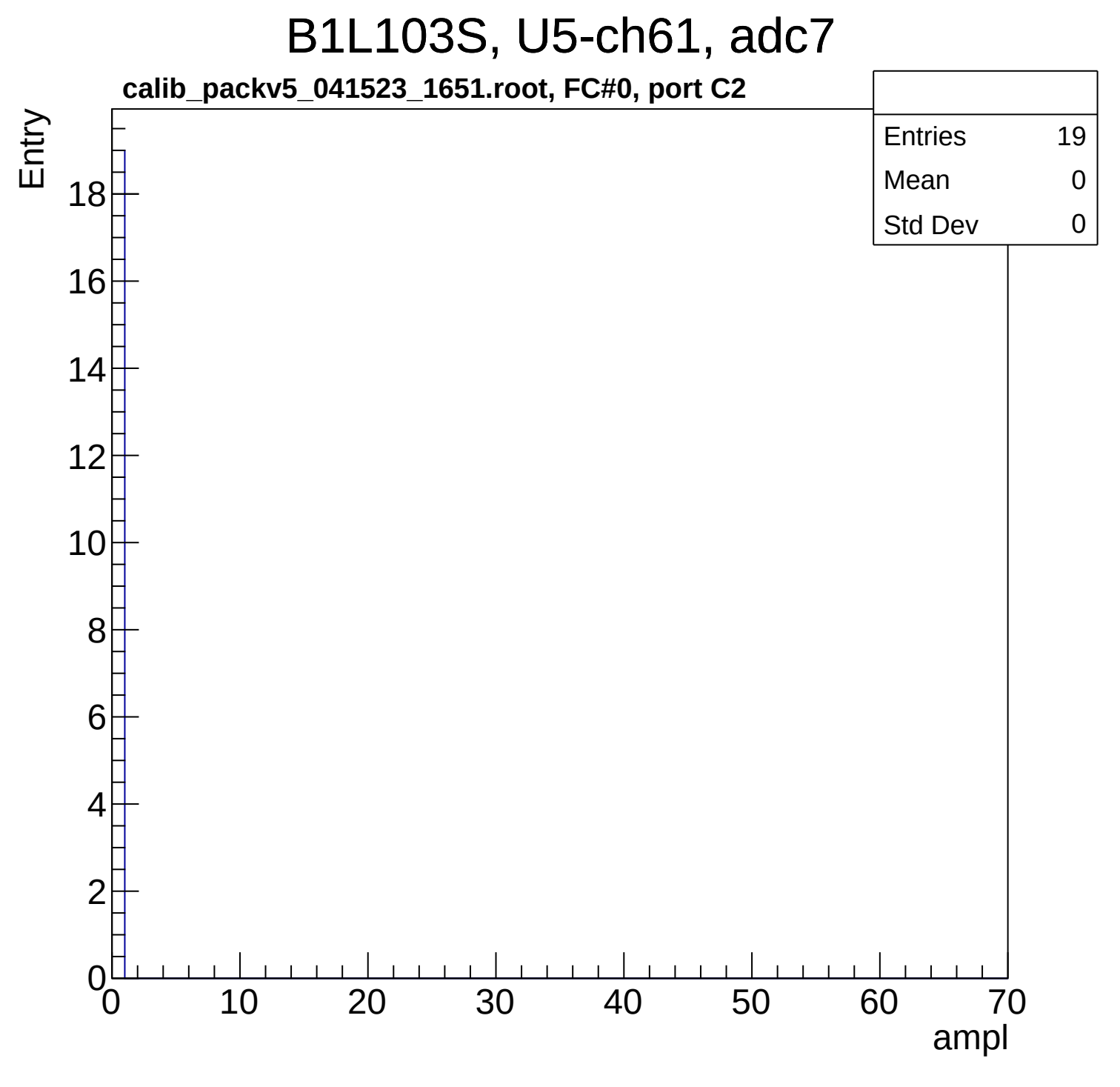
50
60
70
ampl


B1L103S, U5-ch61, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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30
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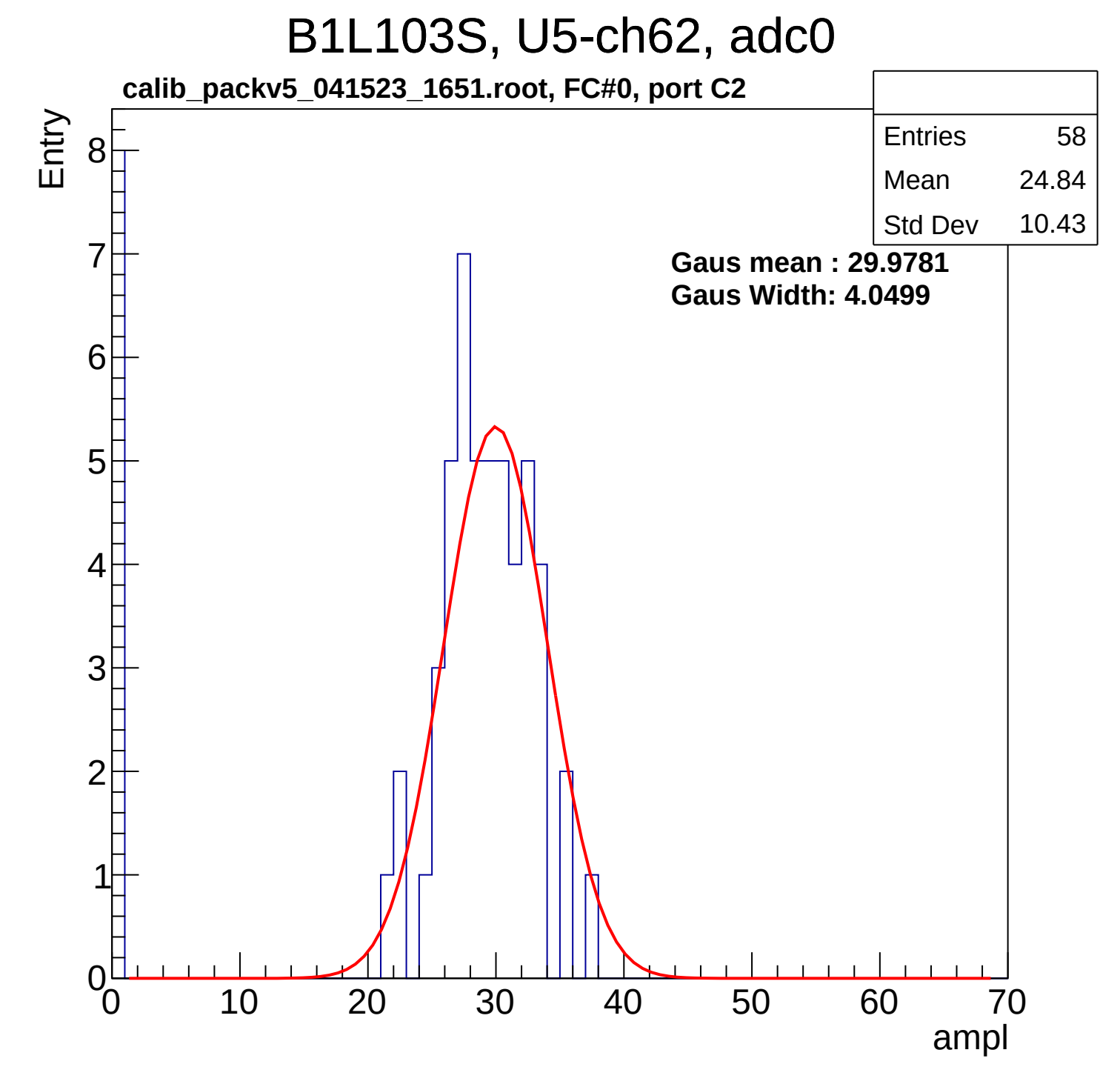
70
ampl


B1L103S, U5-ch62, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 24.84
Std Dev 10.43
Gaus mean : 29.9781
Gaus Width: 4.0499
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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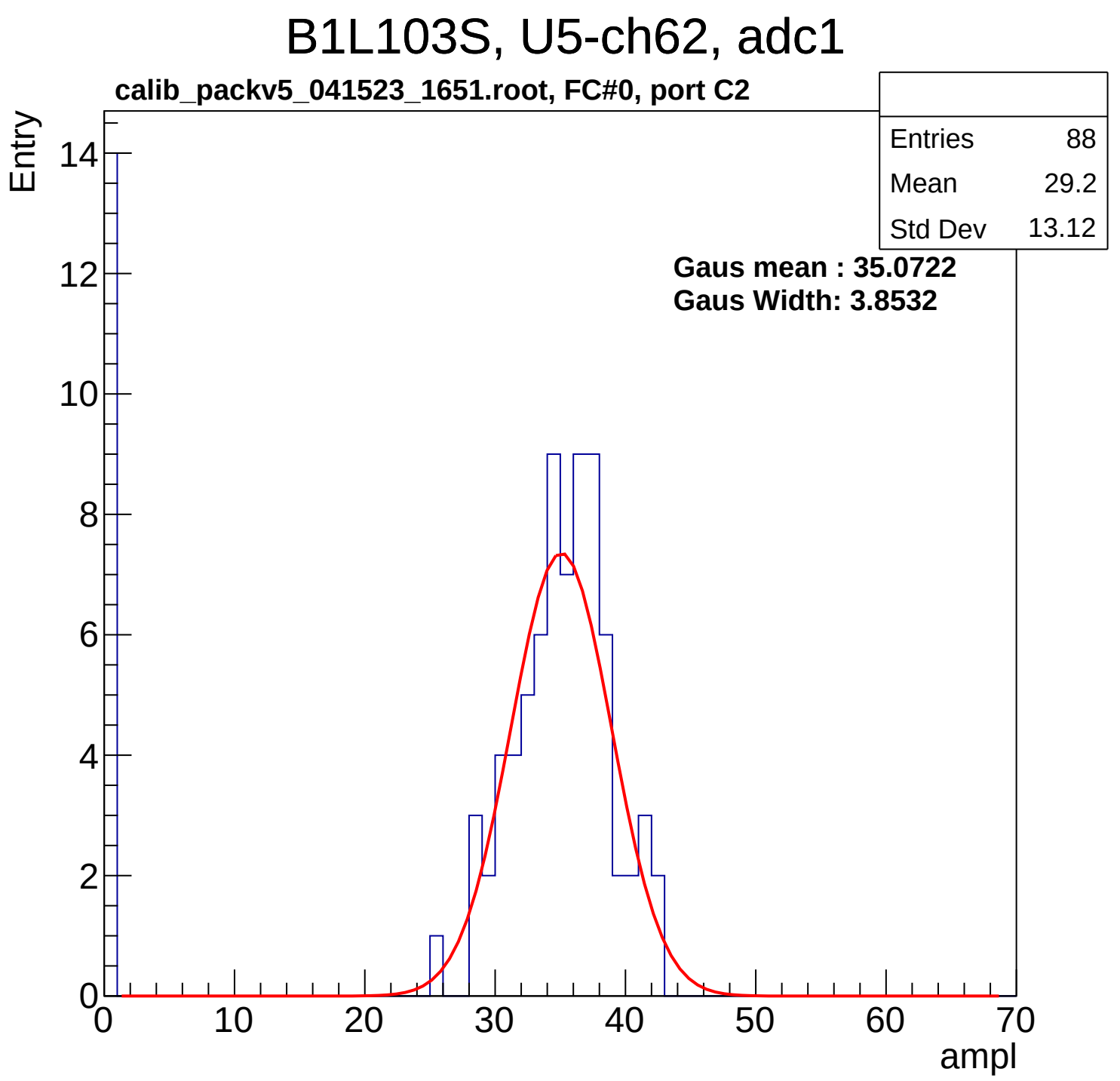
B1L103S, U5-ch62, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 29.2
Std Dev 13.12
Gaus mean : 35.0722
Gaus Width: 3.8532
Entry
ampl
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2
4
6
8
10
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14
0
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20
30
40
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60
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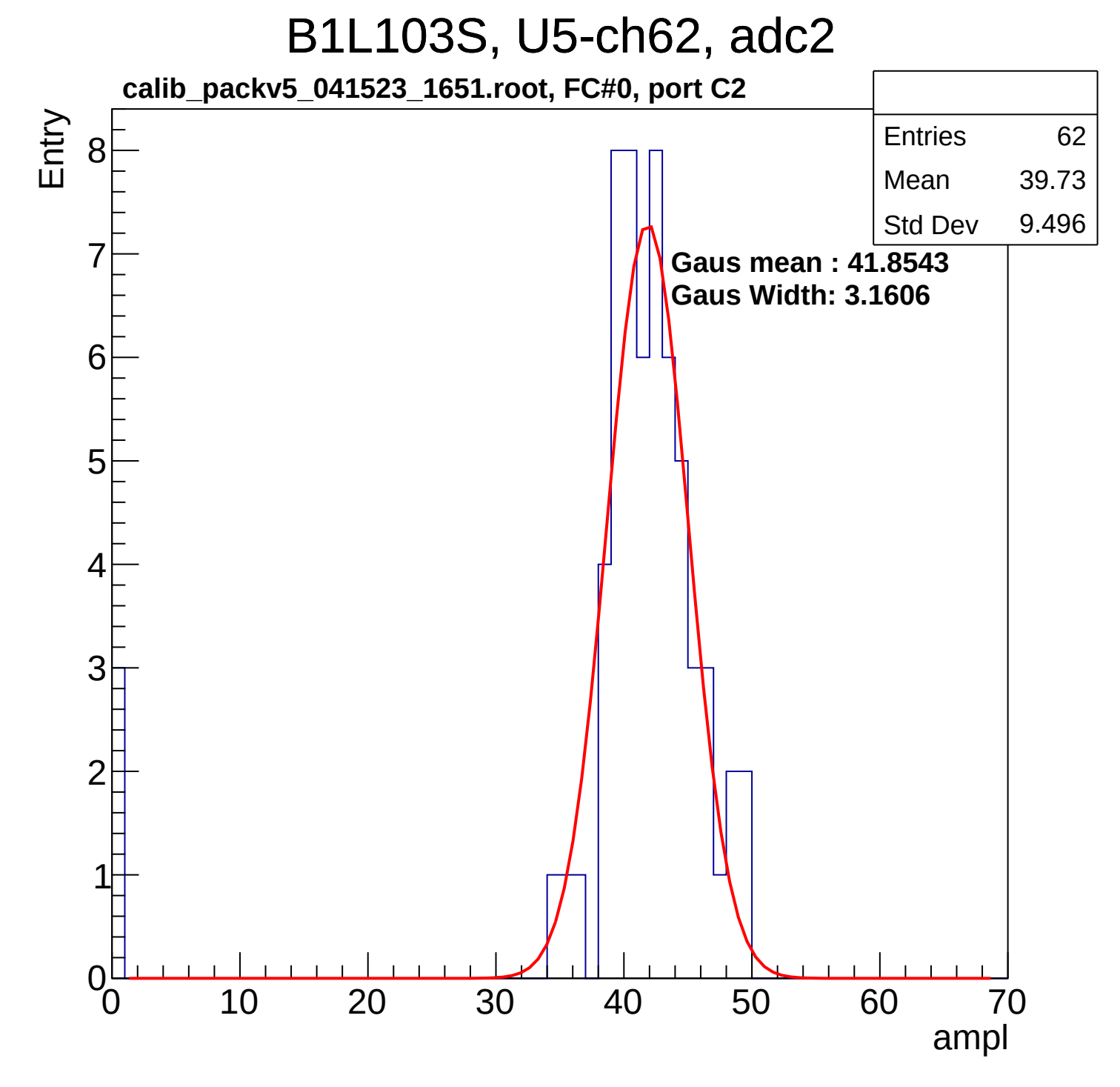
B1L103S, U5-ch62, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 39.73
Std Dev 9.496
Gaus mean : 41.8543
Gaus Width: 3.1606
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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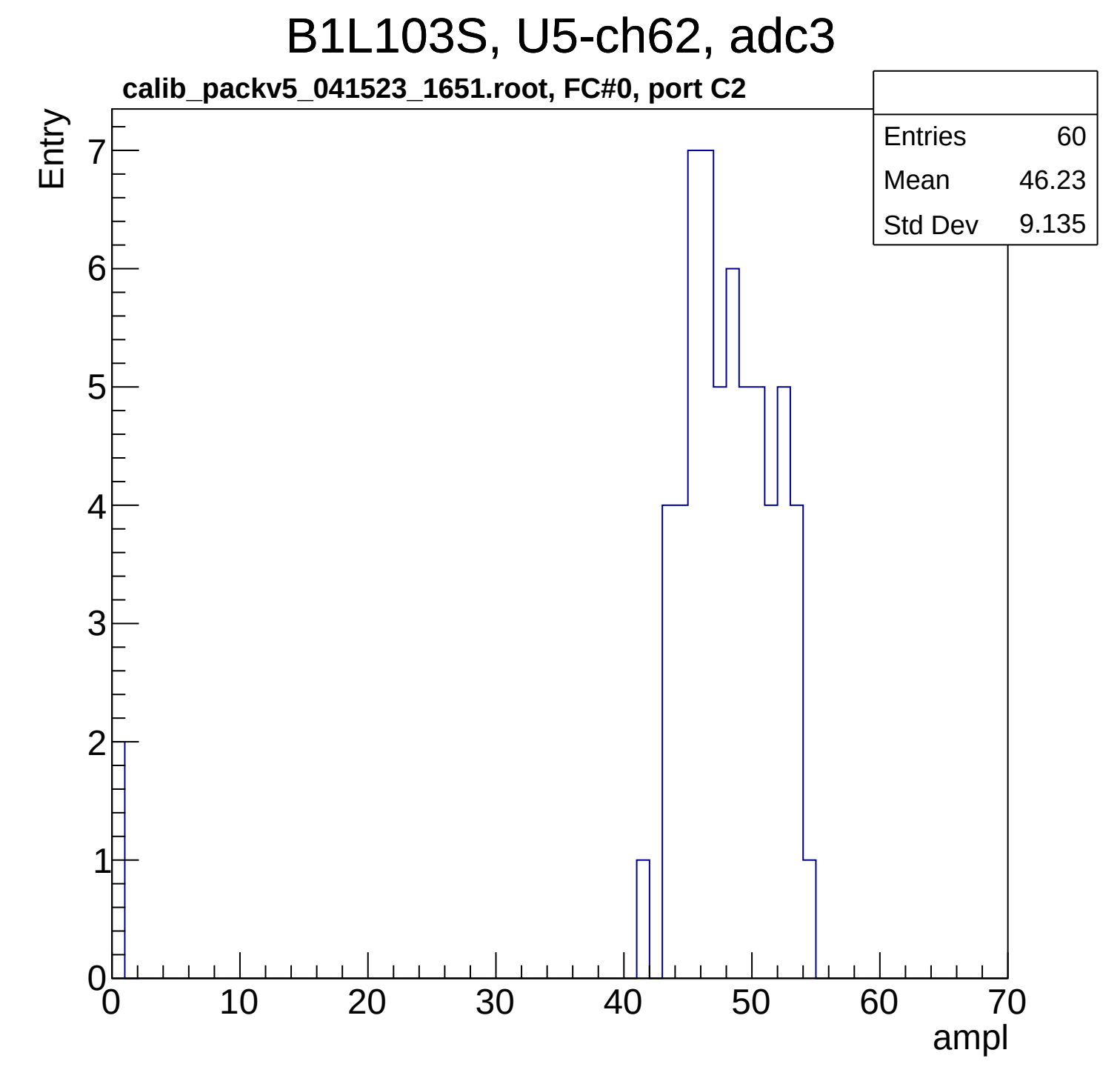
B1L103S, U5-ch62, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 46.23
Std Dev 9.135
Entry
ampl
0
1
2
3
4
5
6
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0
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60
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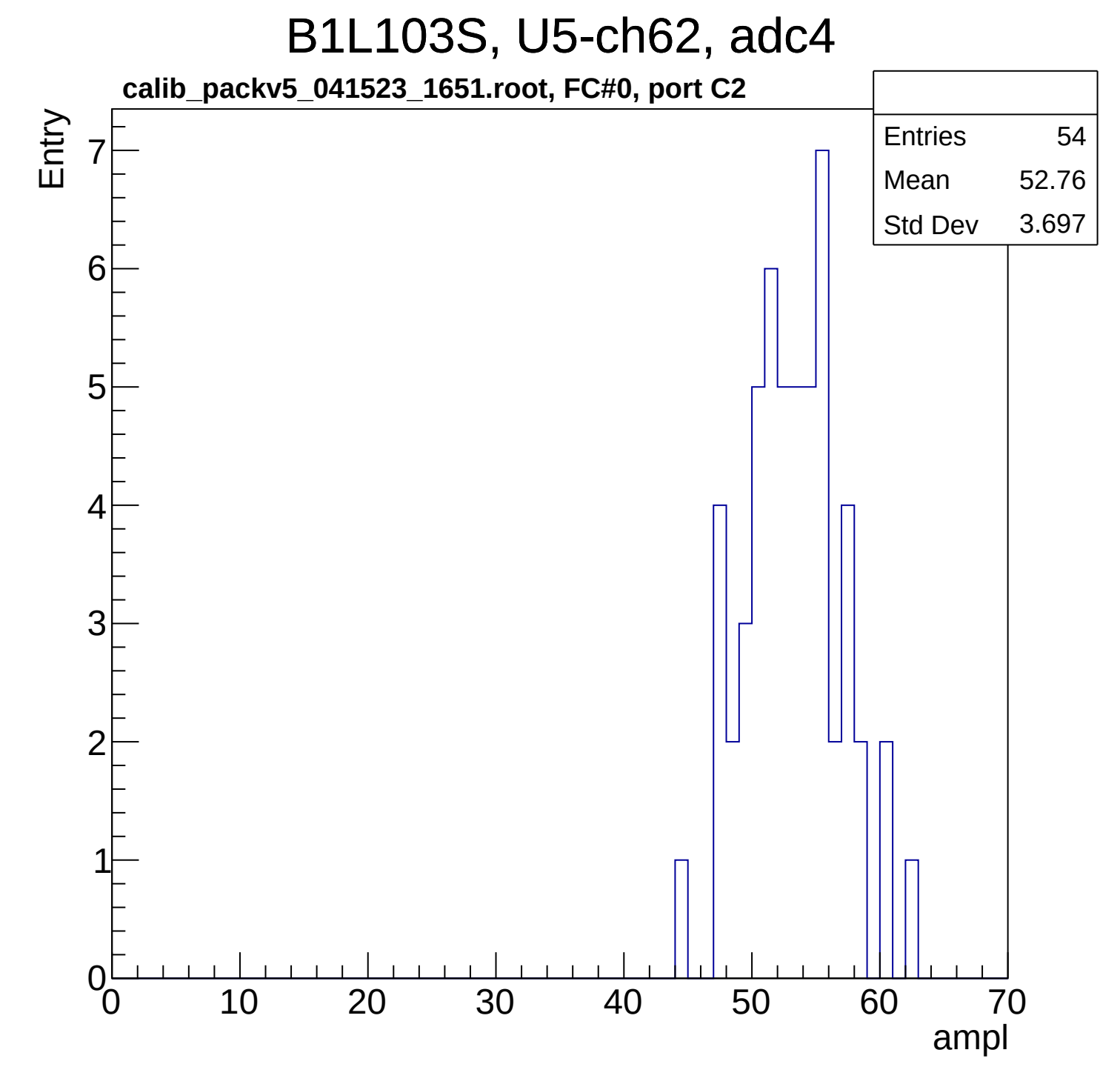
B1L103S, U5-ch62, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 52.76
Std Dev 3.697
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
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60
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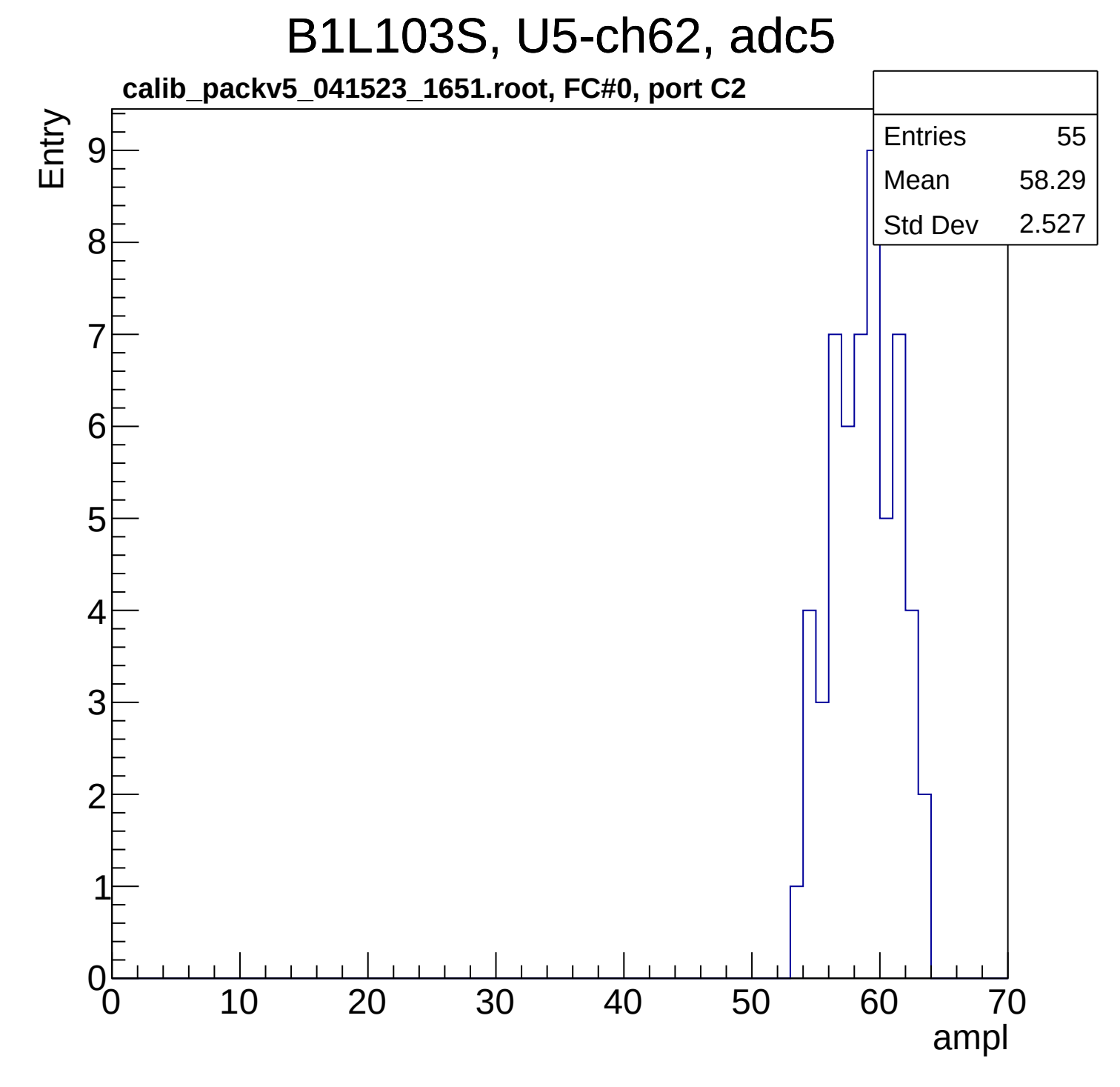
B1L103S, U5-ch62, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.29
Std Dev 2.527
Entry
ampl
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6
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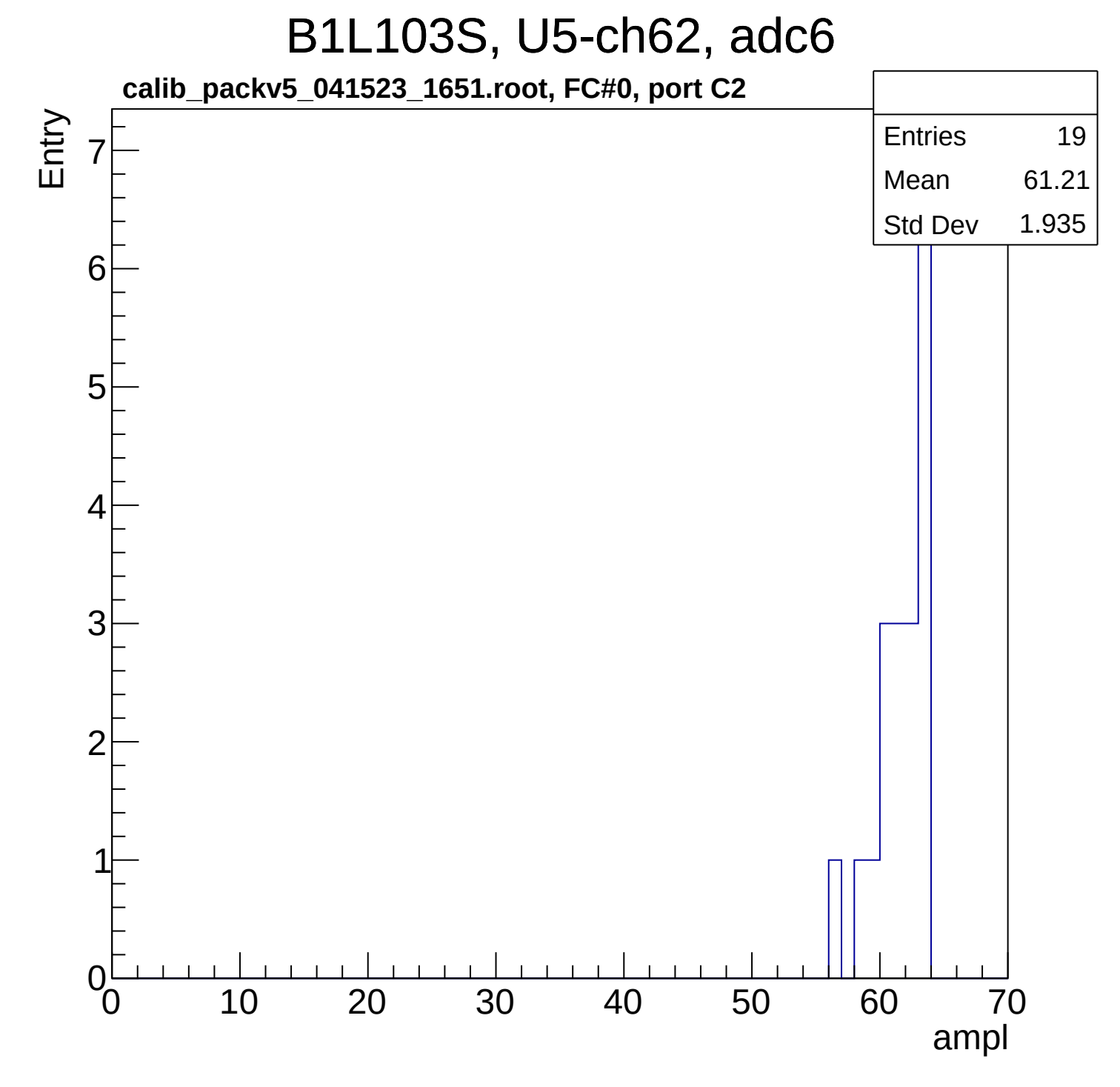
B1L103S, U5-ch62, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 61.21
Std Dev 1.935
Entry
ampl
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2
3
4
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6
7
0
10
20
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40
50
60
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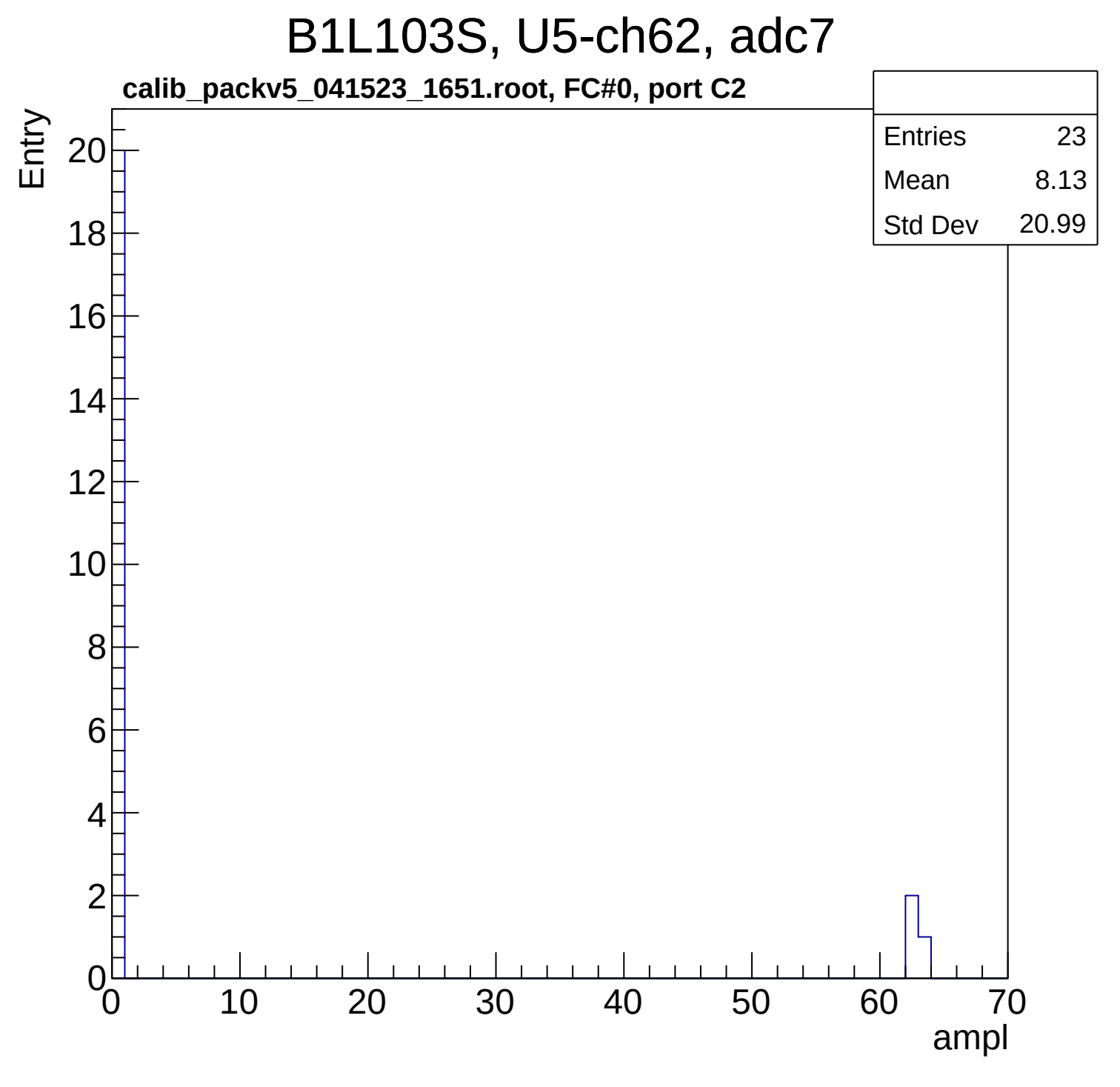
B1L103S, U5-ch62, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 8.13
Std Dev 20.99
Entry
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8
10
12
14
16
18
20
0
10
20
30
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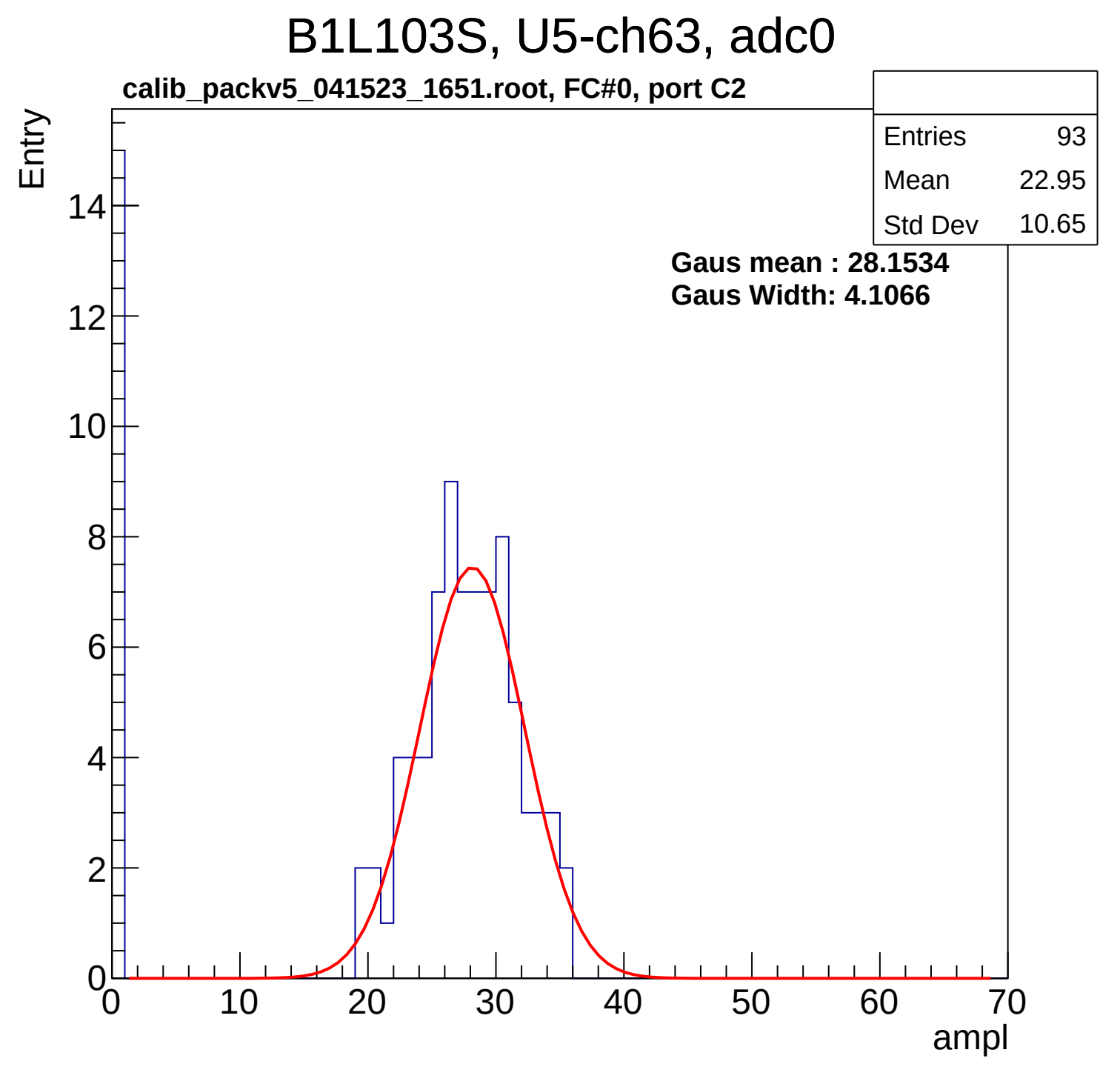
50
60
70
ampl


B1L103S, U5-ch63, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 22.95
Std Dev 10.65
Gaus mean : 28.1534
Gaus Width: 4.1066
Entry
ampl
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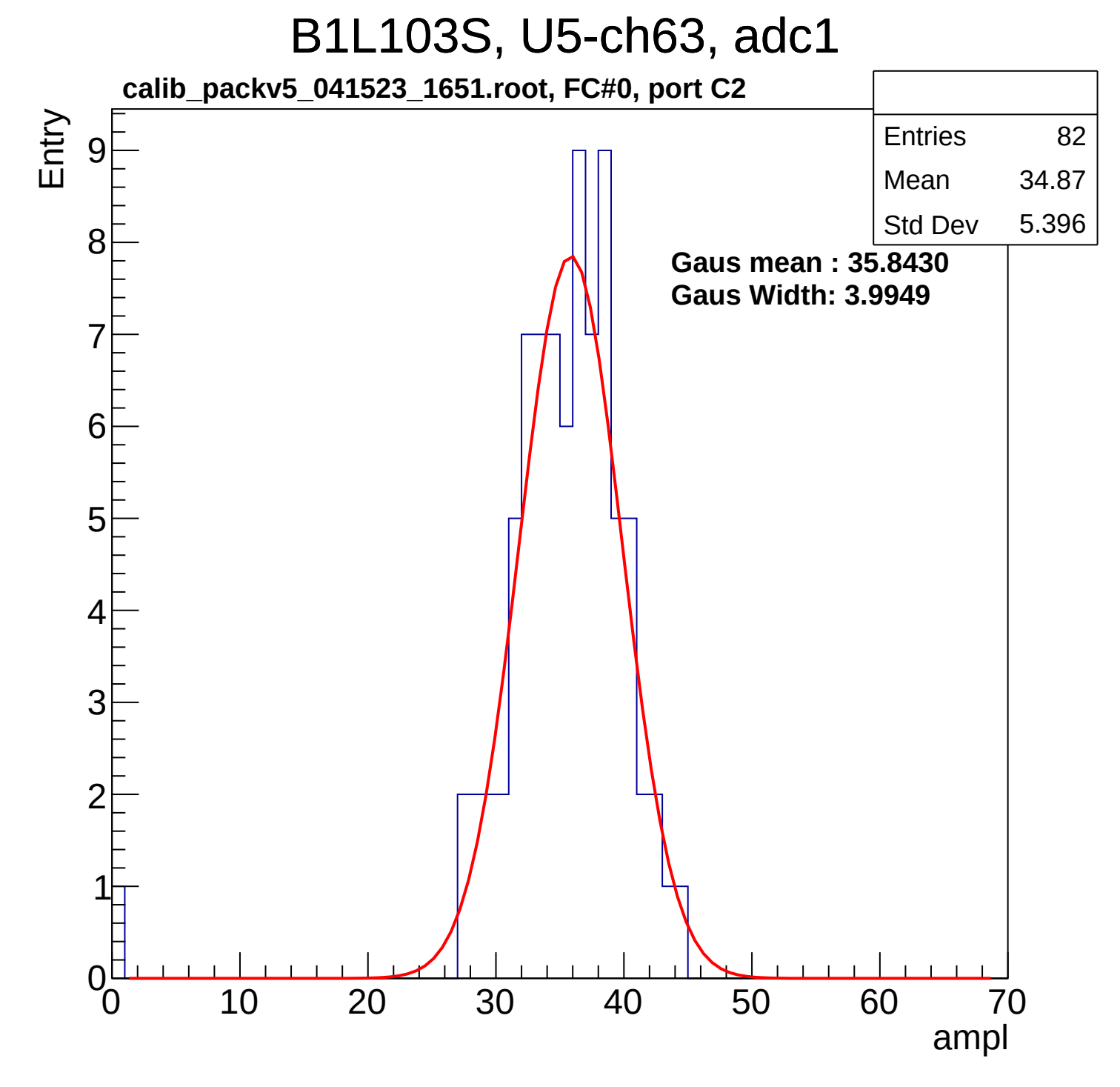
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U5-ch63, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 34.87
Std Dev 5.396
Gaus mean : 35.8430
Gaus Width: 3.9949
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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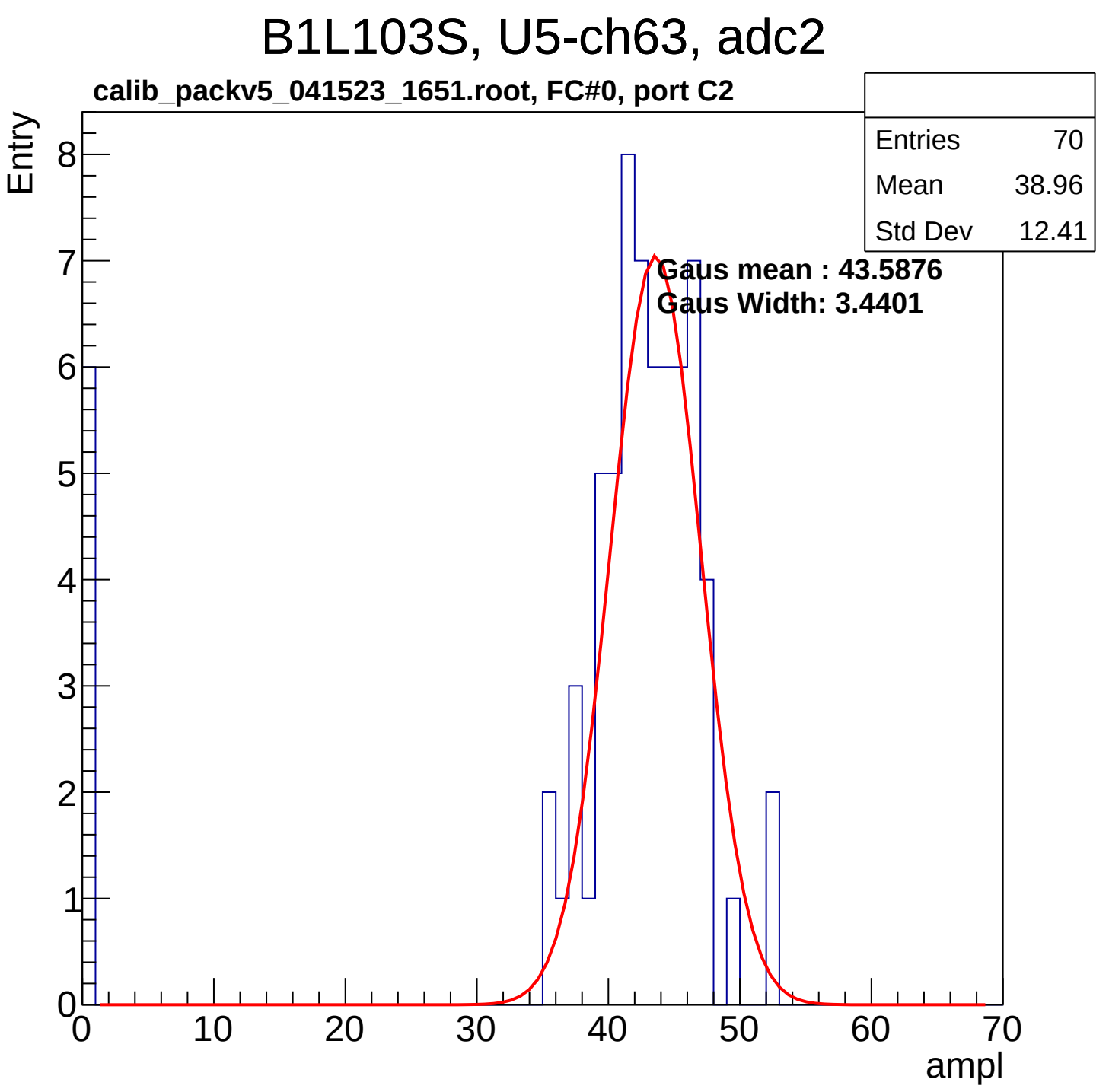
B1L103S, U5-ch63, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 38.96
Std Dev 12.41
Gaus mean : 43.5876
Gaus Width: 3.4401
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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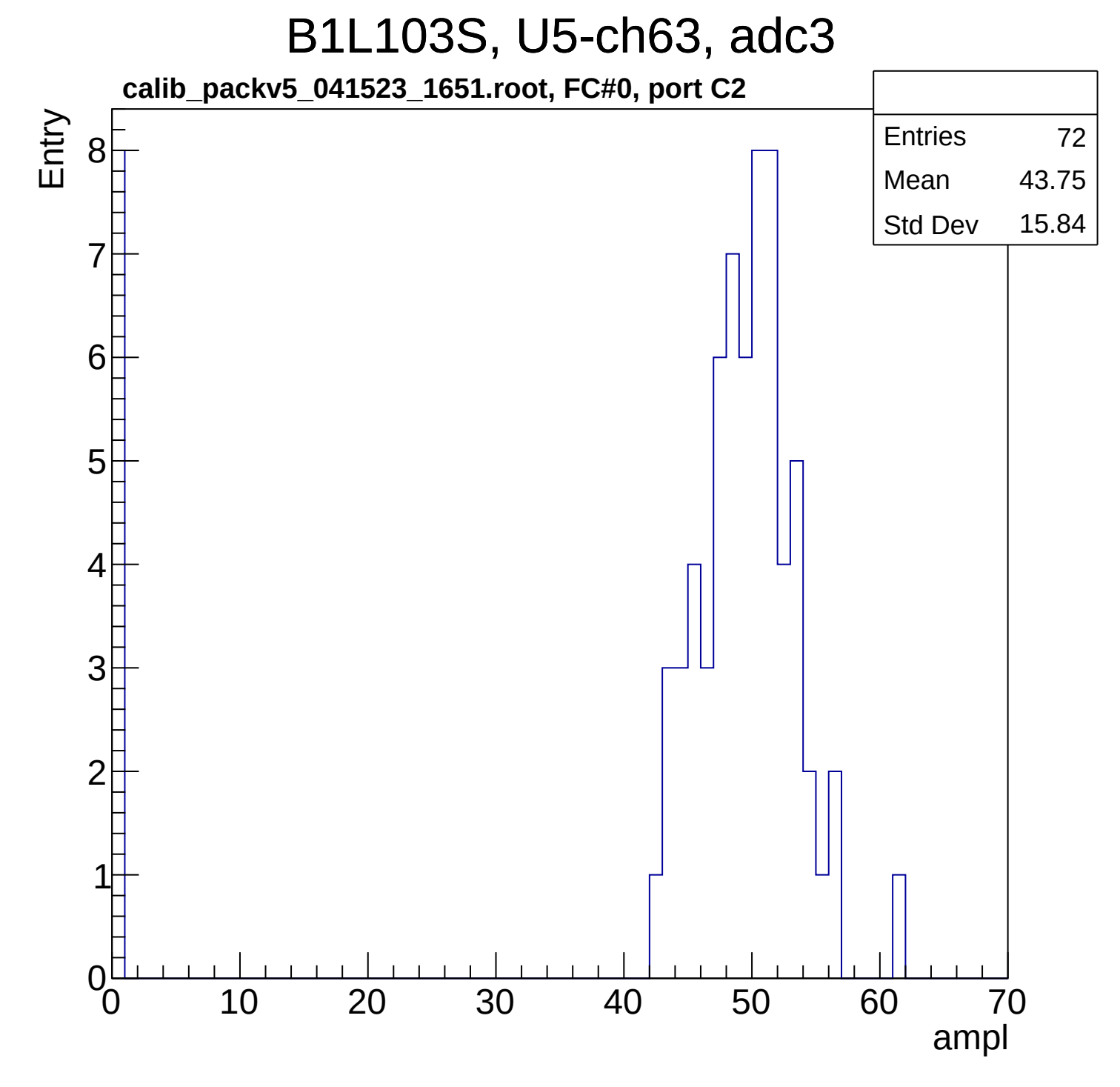
B1L103S, U5-ch63, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 43.75
Std Dev 15.84
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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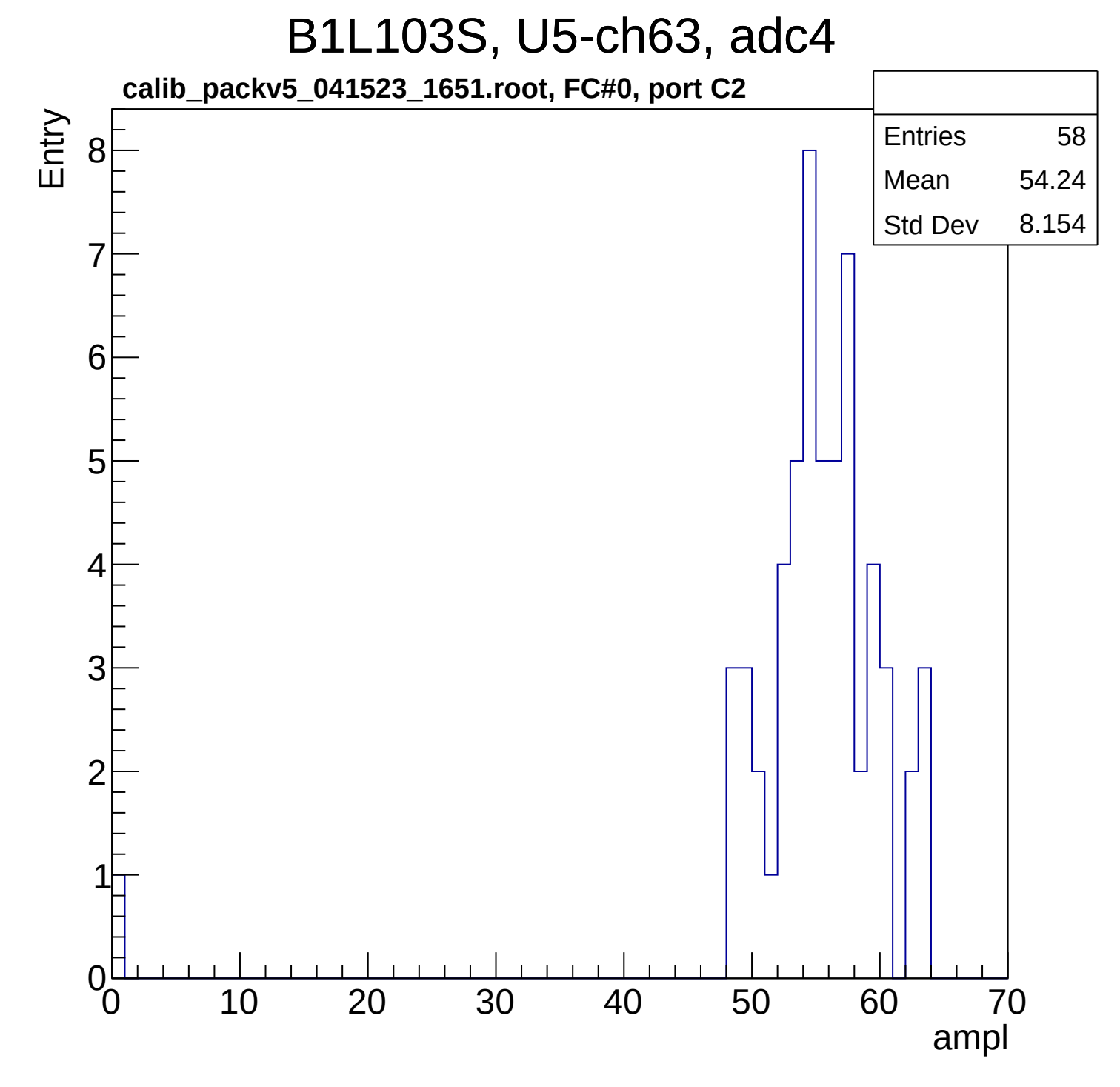
B1L103S, U5-ch63, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 54.24
Std Dev 8.154
Entry
ampl
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2
3
4
5
6
7
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0
10
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60
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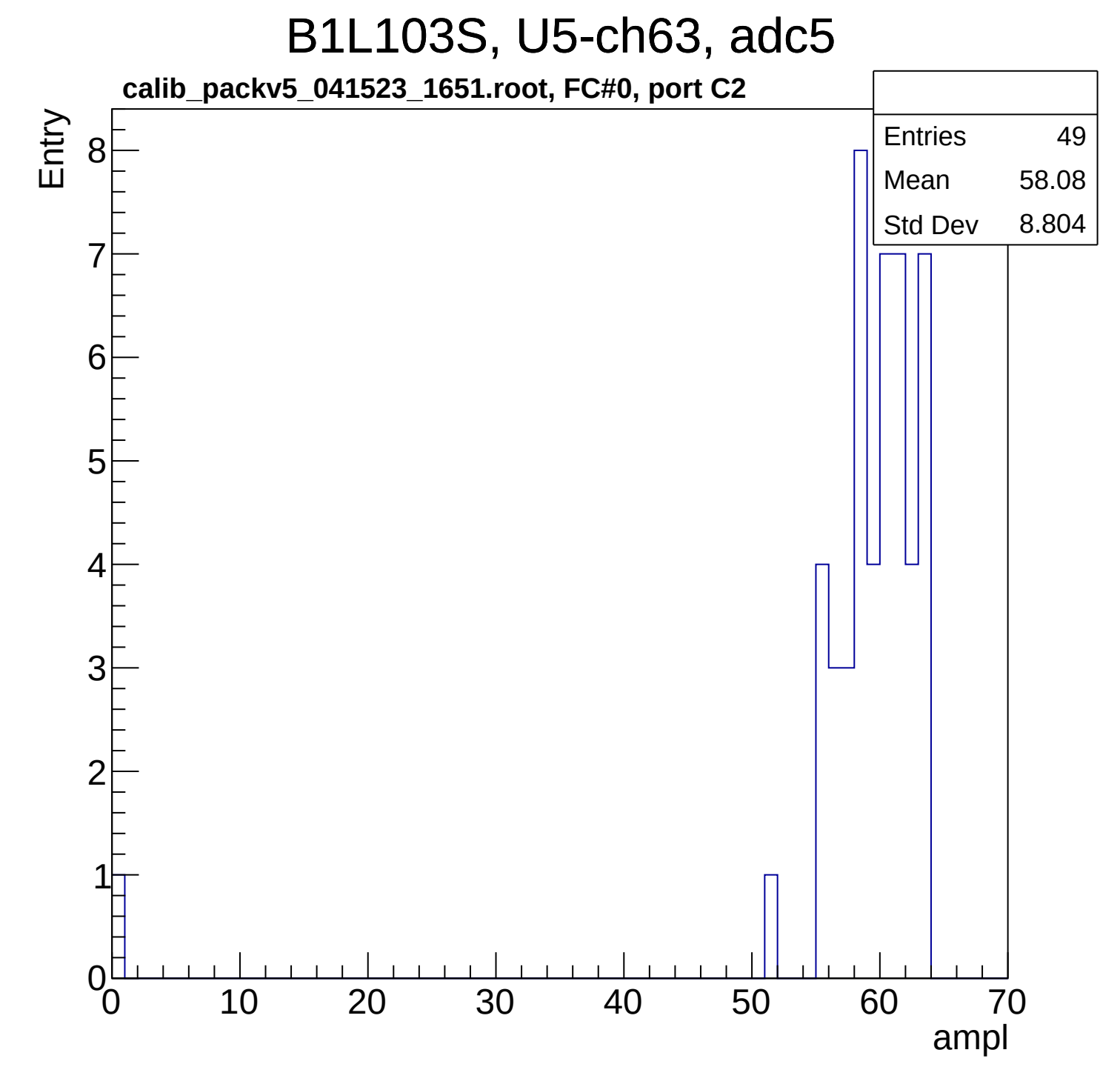
B1L103S, U5-ch63, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.08
Std Dev 8.804
Entry
ampl
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1
2
3
4
5
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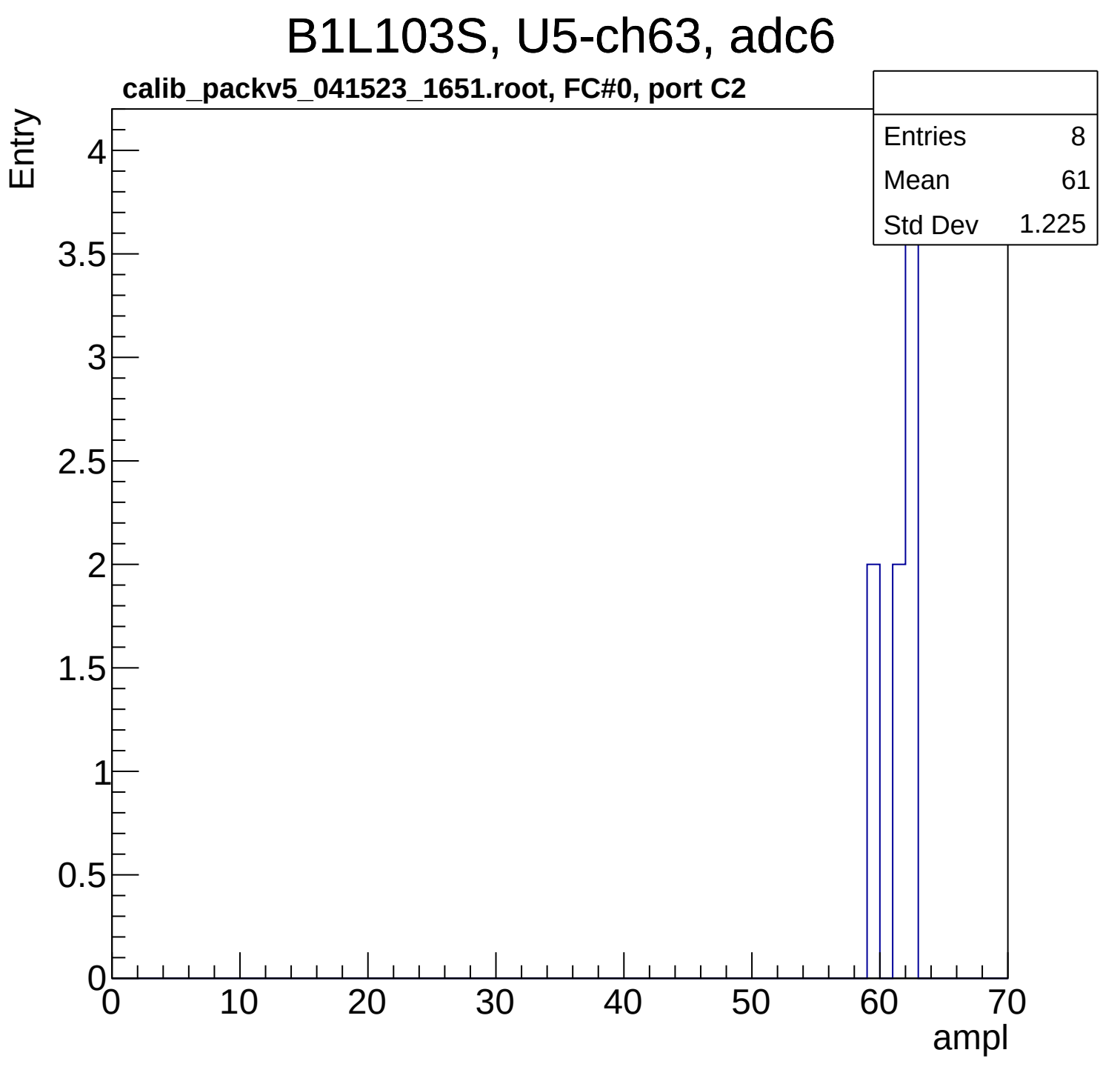
B1L103S, U5-ch63, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61
Std Dev 1.225
Entry
ampl
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1
1.5
2
2.5
3
3.5
4
0
10
20
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40
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60
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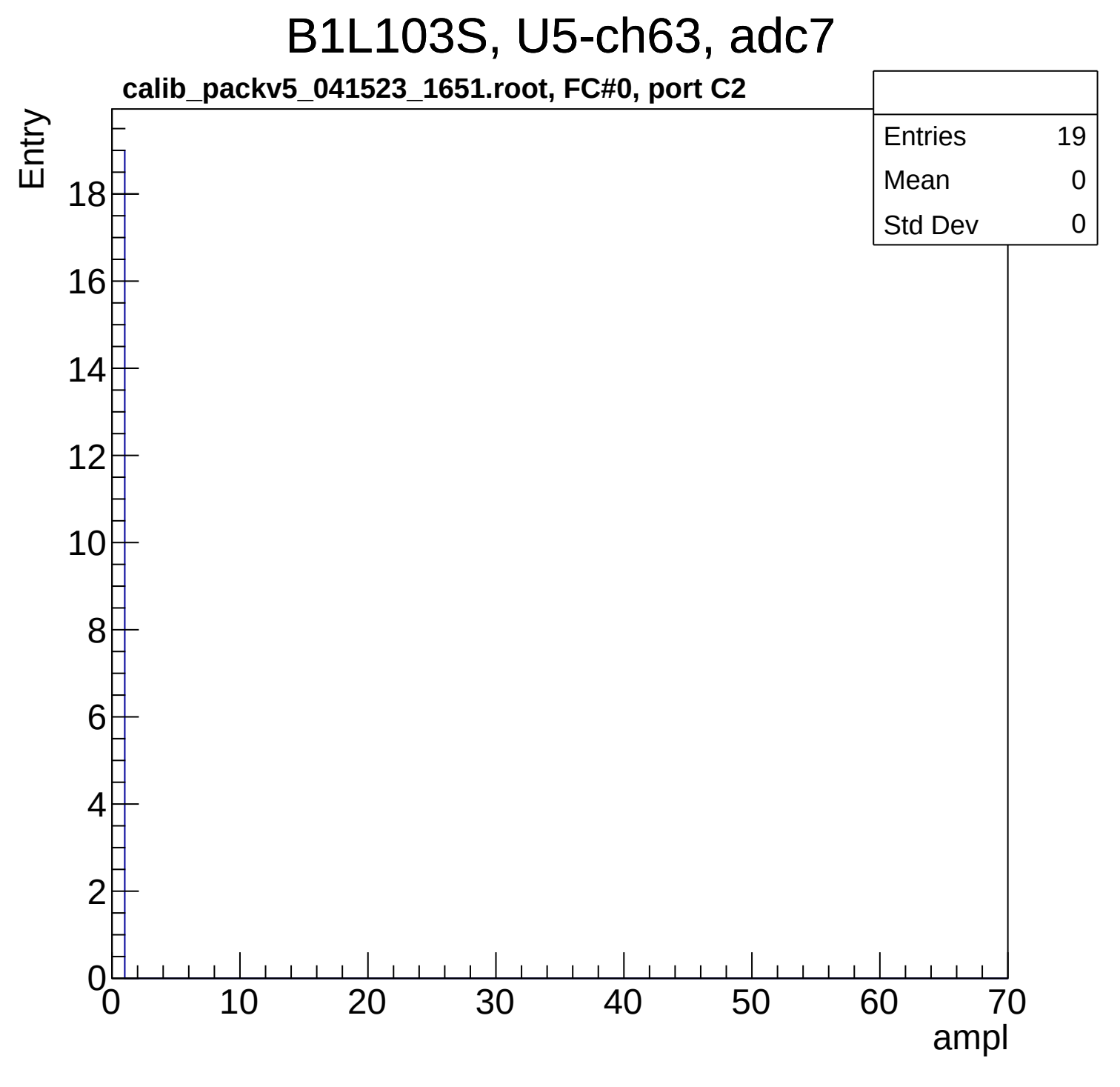
B1L103S, U5-ch63, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
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10
20
30
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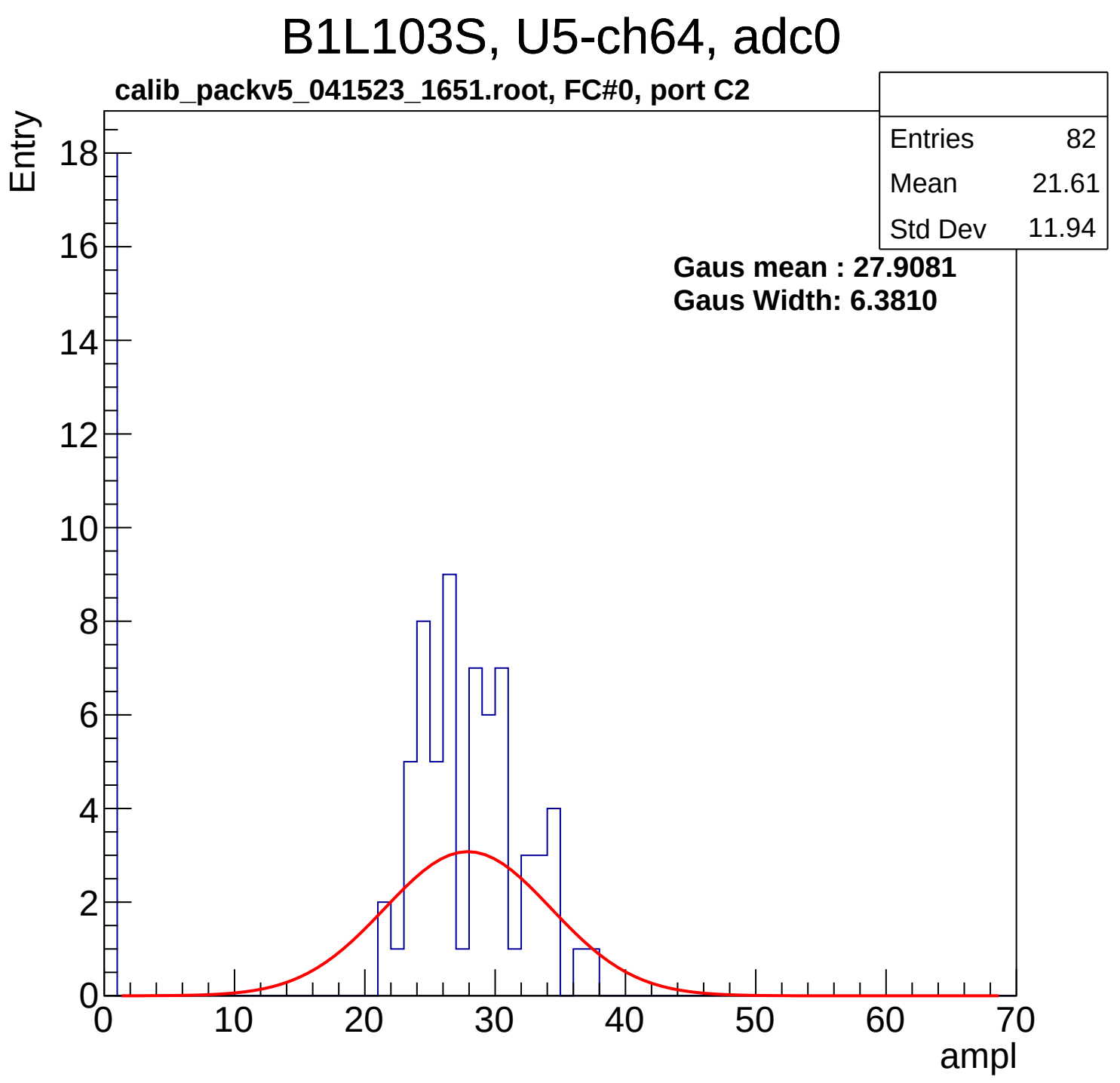
50
60
70
ampl


B1L103S, U5-ch64, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 21.61
Std Dev 11.94
Gaus mean : 27.9081
Gaus Width: 6.3810
Entry
ampl
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4
6
8
10
12
14
16
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0
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20
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40
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60
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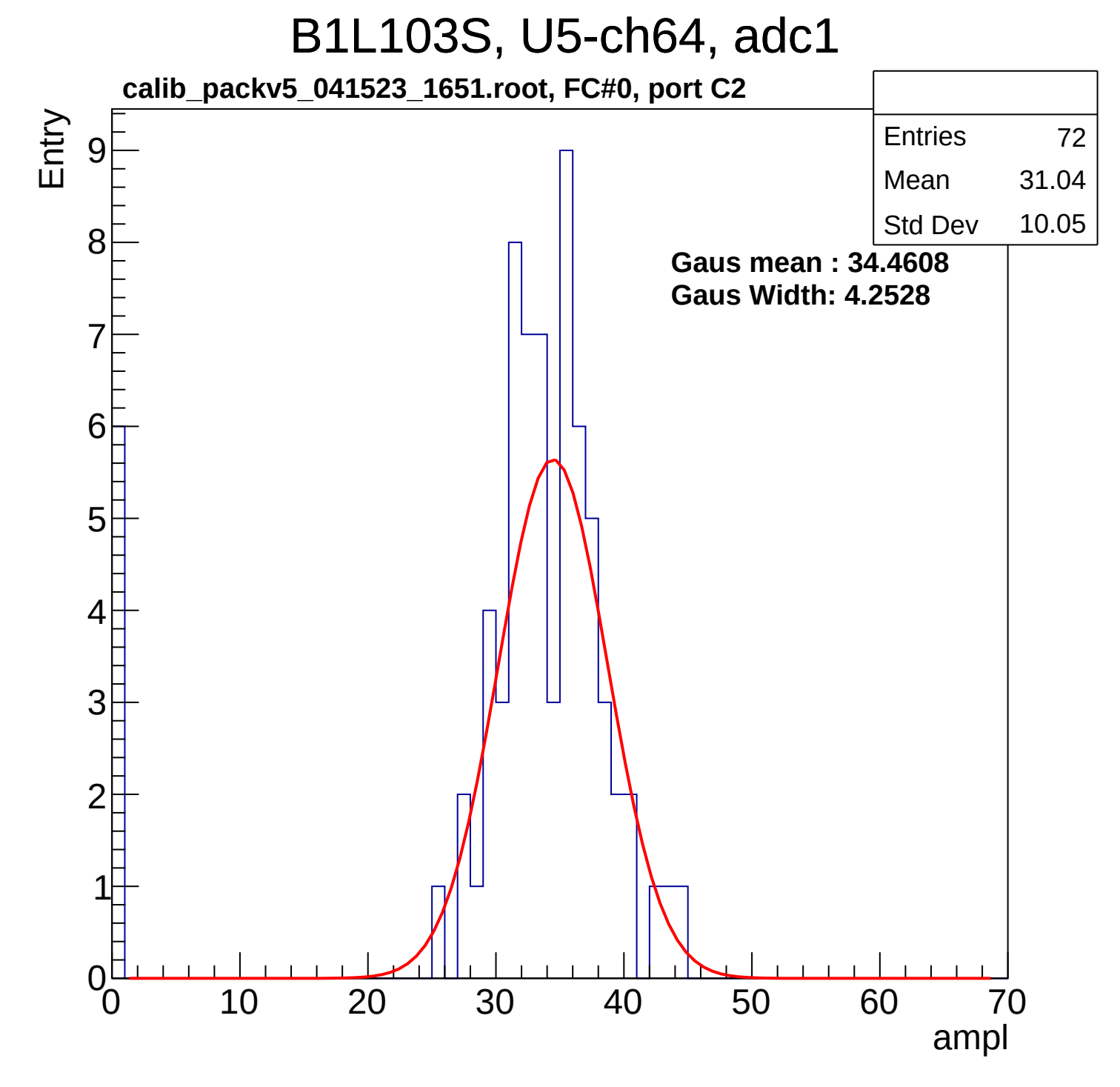
B1L103S, U5-ch64, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 31.04
Std Dev 10.05
Gaus mean : 34.4608
Gaus Width: 4.2528
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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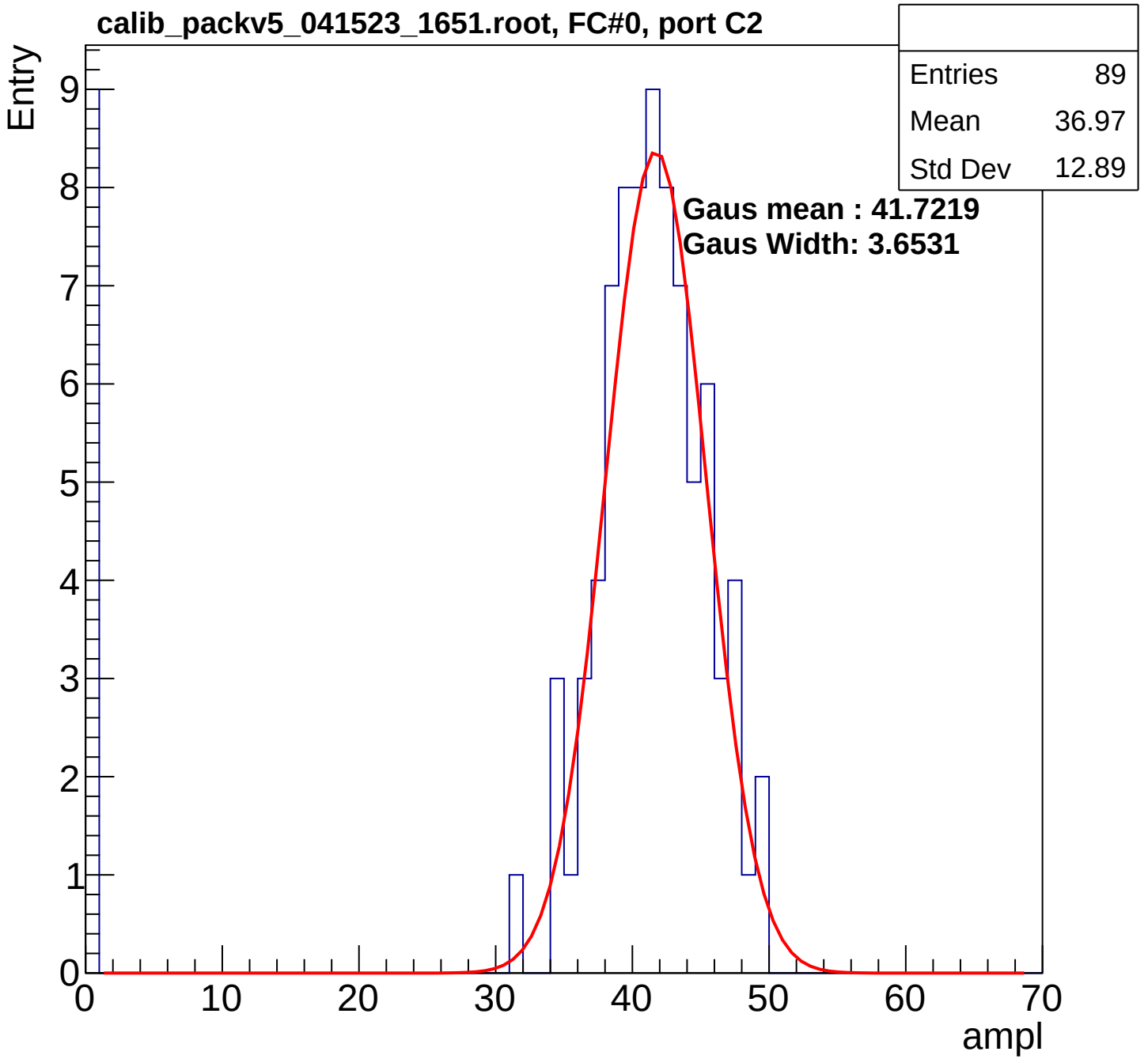
B1L103S, U5-ch64, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 36.97
Std Dev 12.89
Gaus mean : 41.7219
Gaus Width: 3.6531
Entry
ampl
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2
3
4
5
6
7
8
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0
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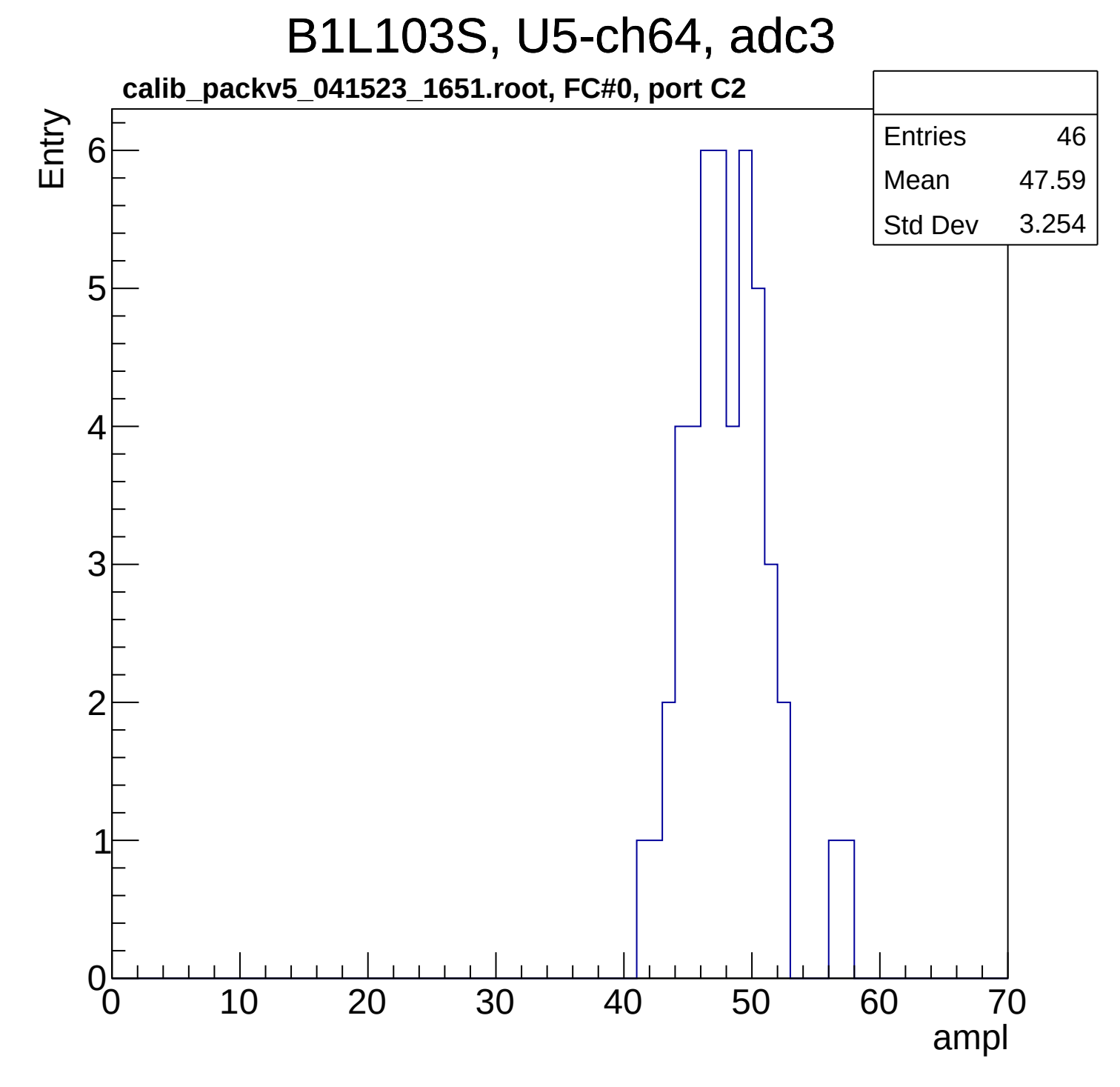
B1L103S, U5-ch64, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 47.59
Std Dev 3.254
Entry
ampl
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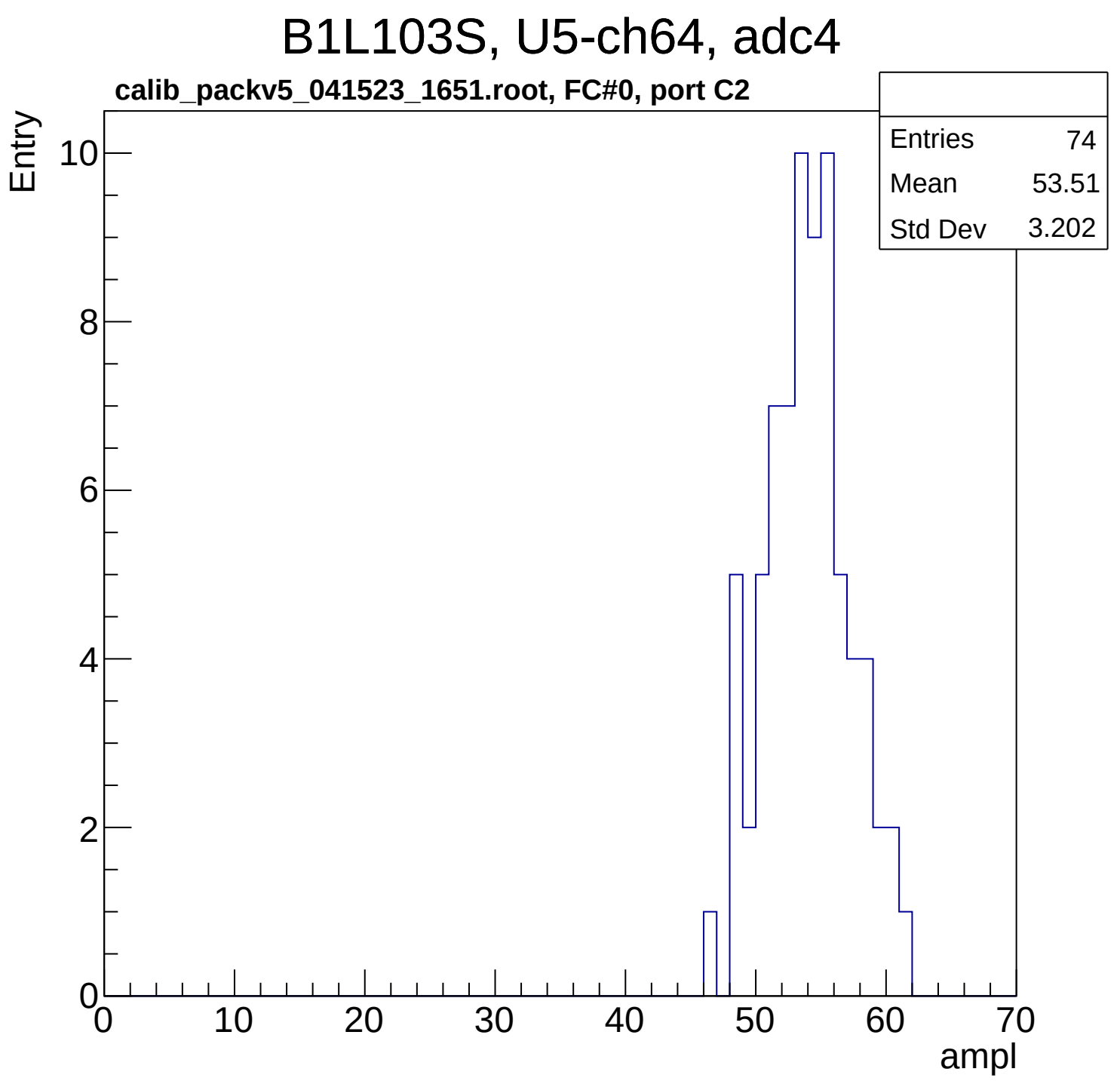
B1L103S, U5-ch64, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 53.51
Std Dev 3.202
Entry
ampl
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60
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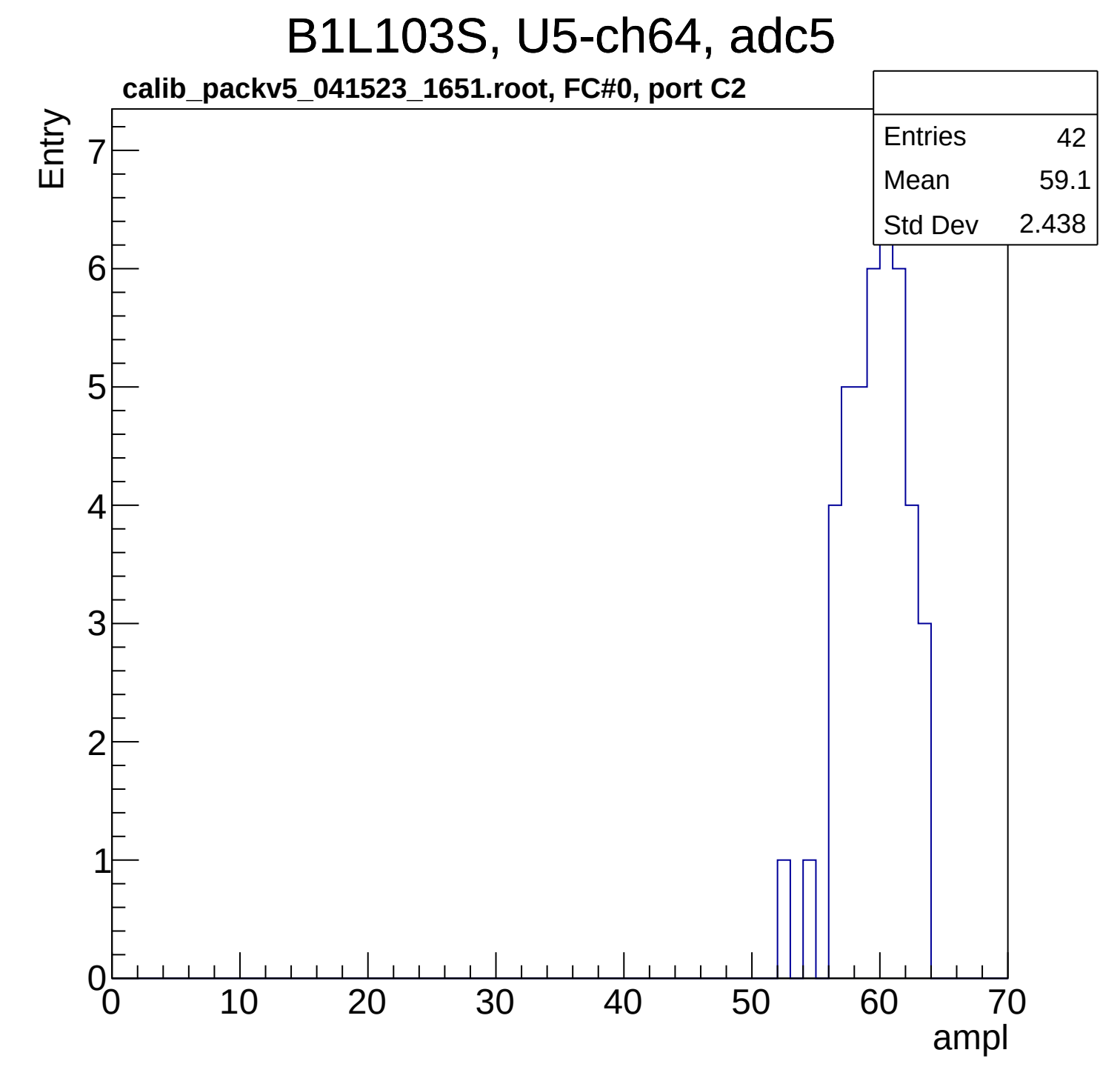
B1L103S, U5-ch64, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 59.1
Std Dev 2.438
Entry
ampl
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3
4
5
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20
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60
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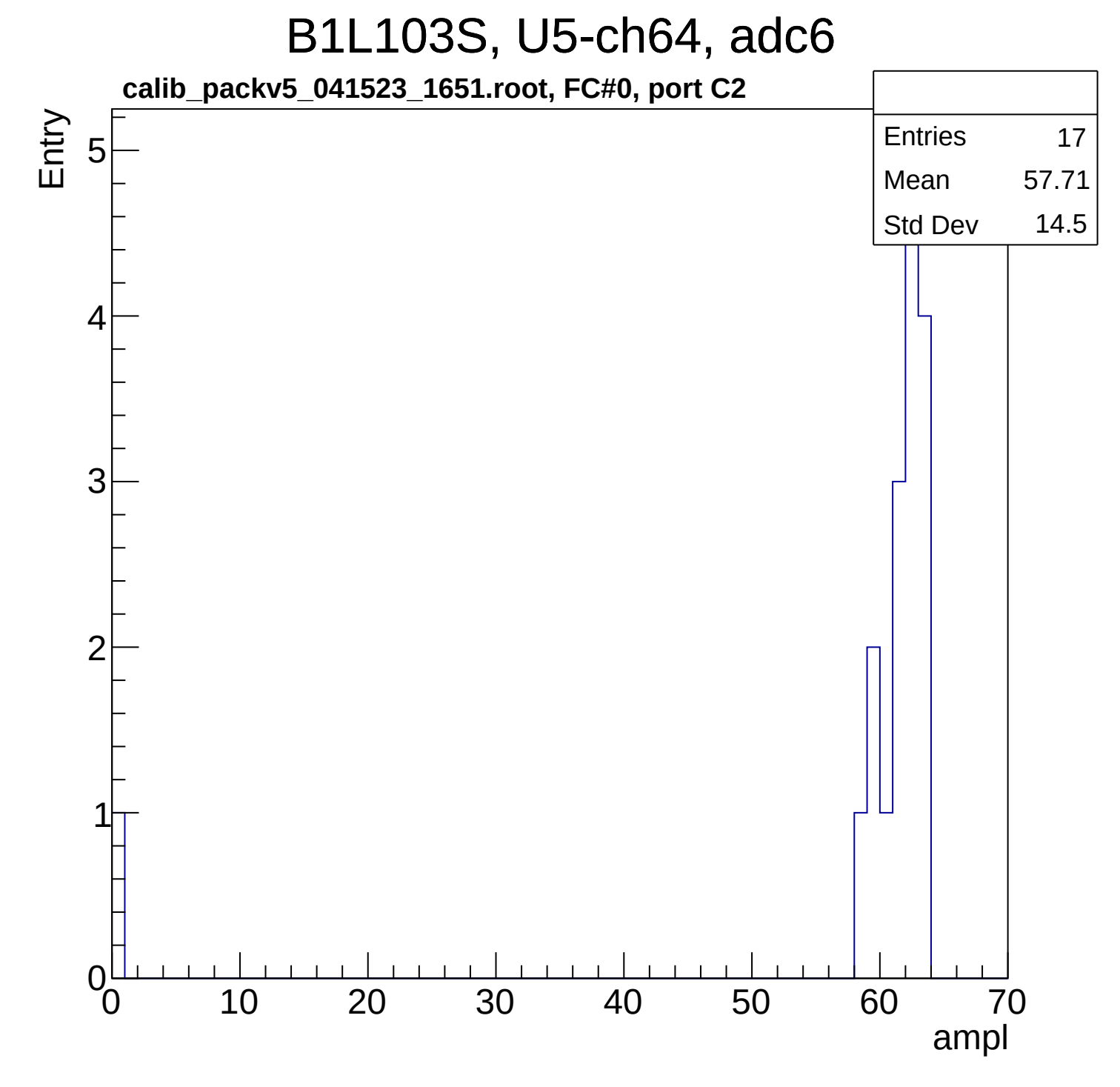
B1L103S, U5-ch64, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 57.71
Std Dev 14.5
Entry
ampl
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3
4
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40
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60
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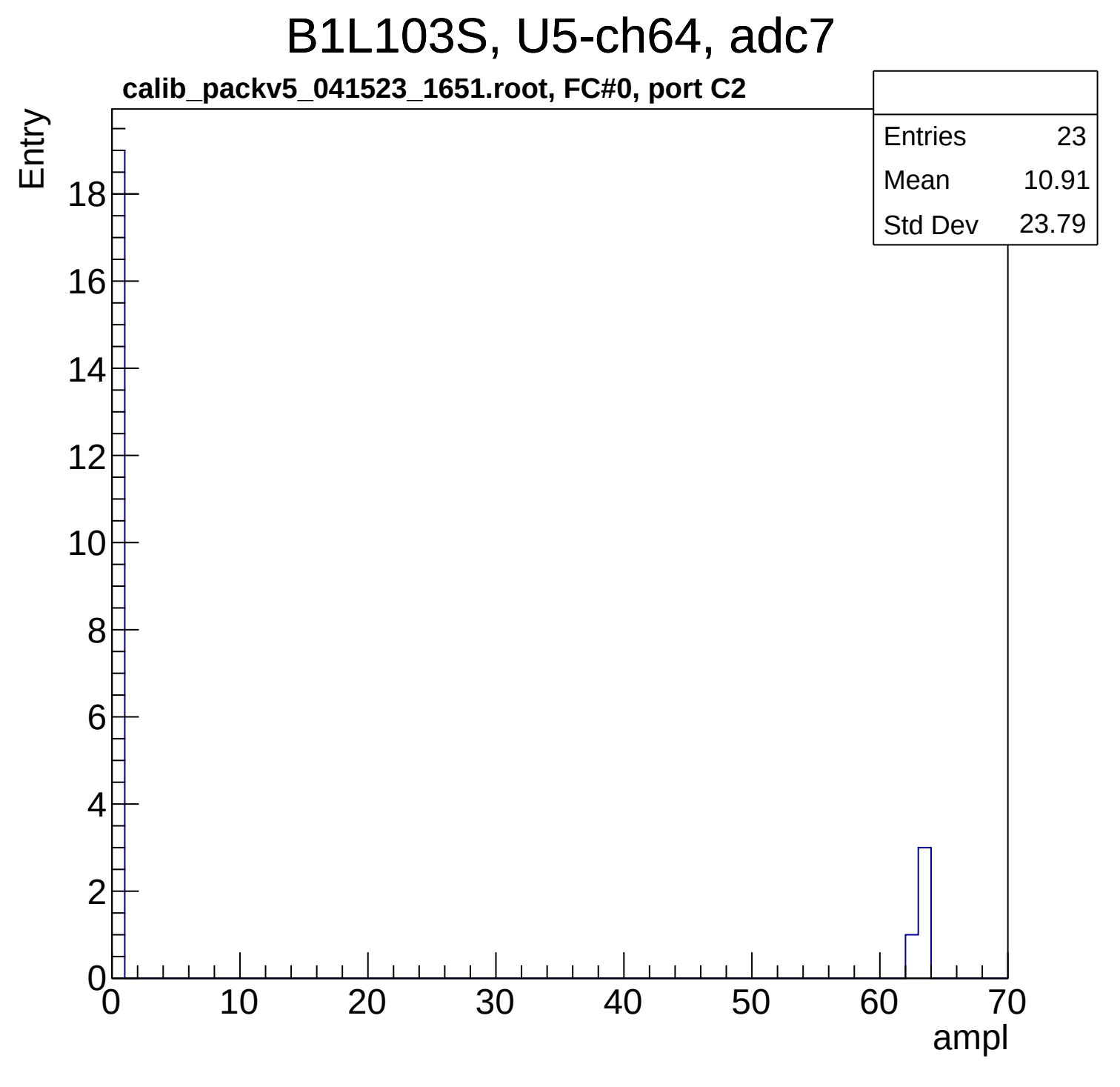
B1L103S, U5-ch64, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.91
Std Dev 23.79
Entry
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6
8
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14
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10
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50
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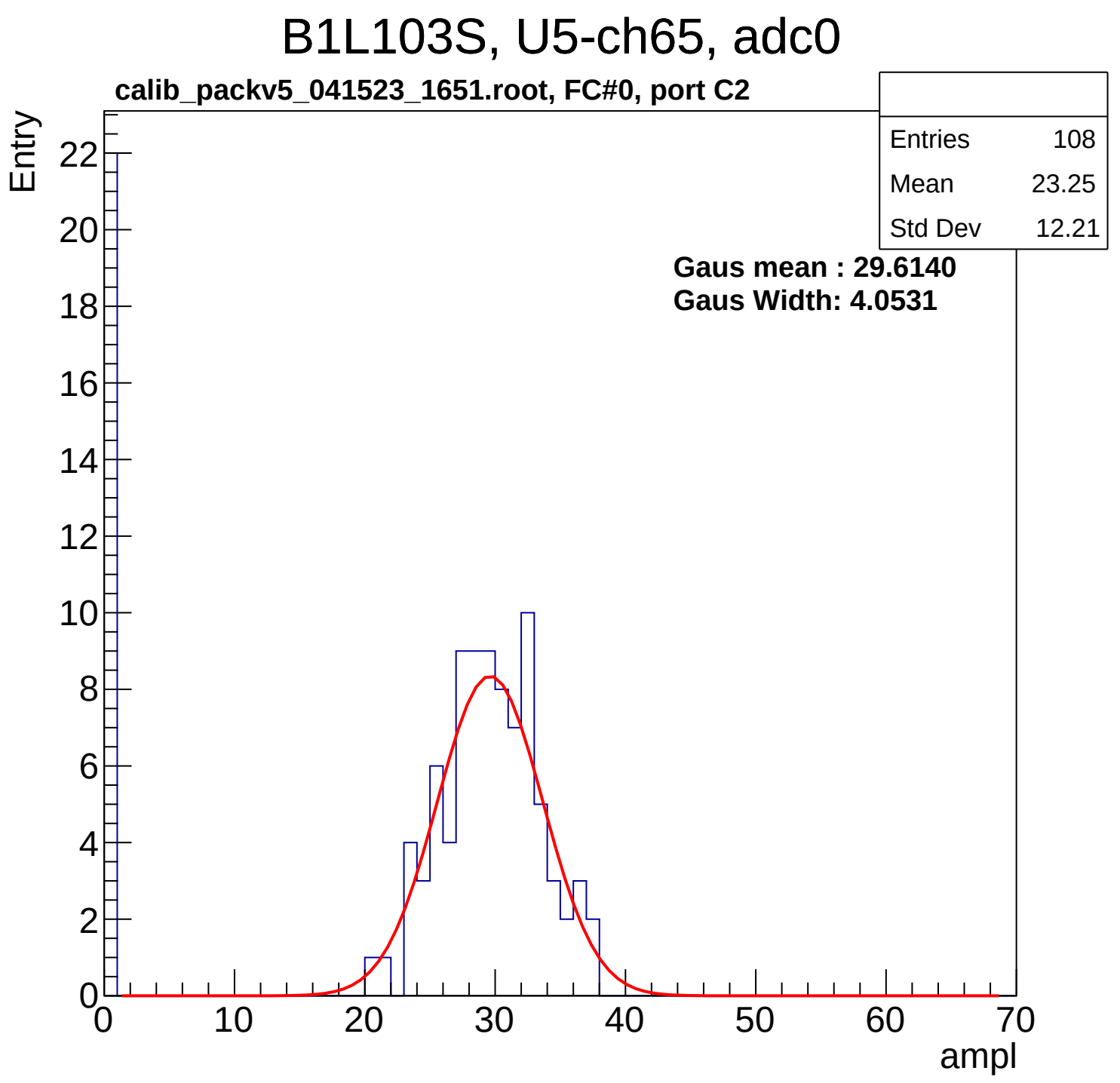
70
ampl


B1L103S, U5-ch65, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 108
Mean 23.25
Std Dev 12.21
Gaus mean : 29.6140
Gaus Width: 4.0531
Entry
ampl
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8
10
12
14
16
18
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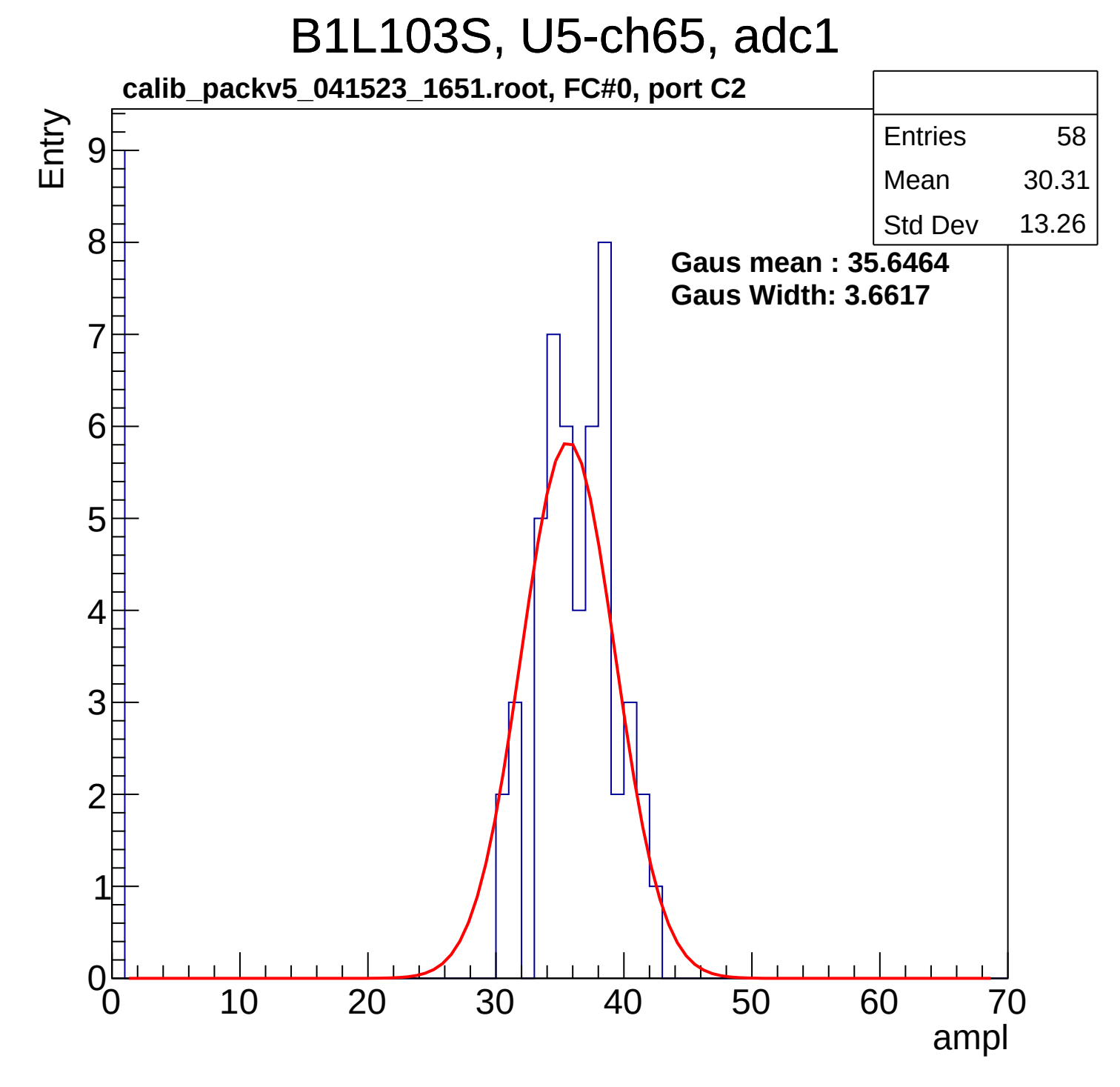
B1L103S, U5-ch65, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 30.31
Std Dev 13.26
Gaus mean : 35.6464
Gaus Width: 3.6617
Entry
ampl
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3
4
5
6
7
8
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0
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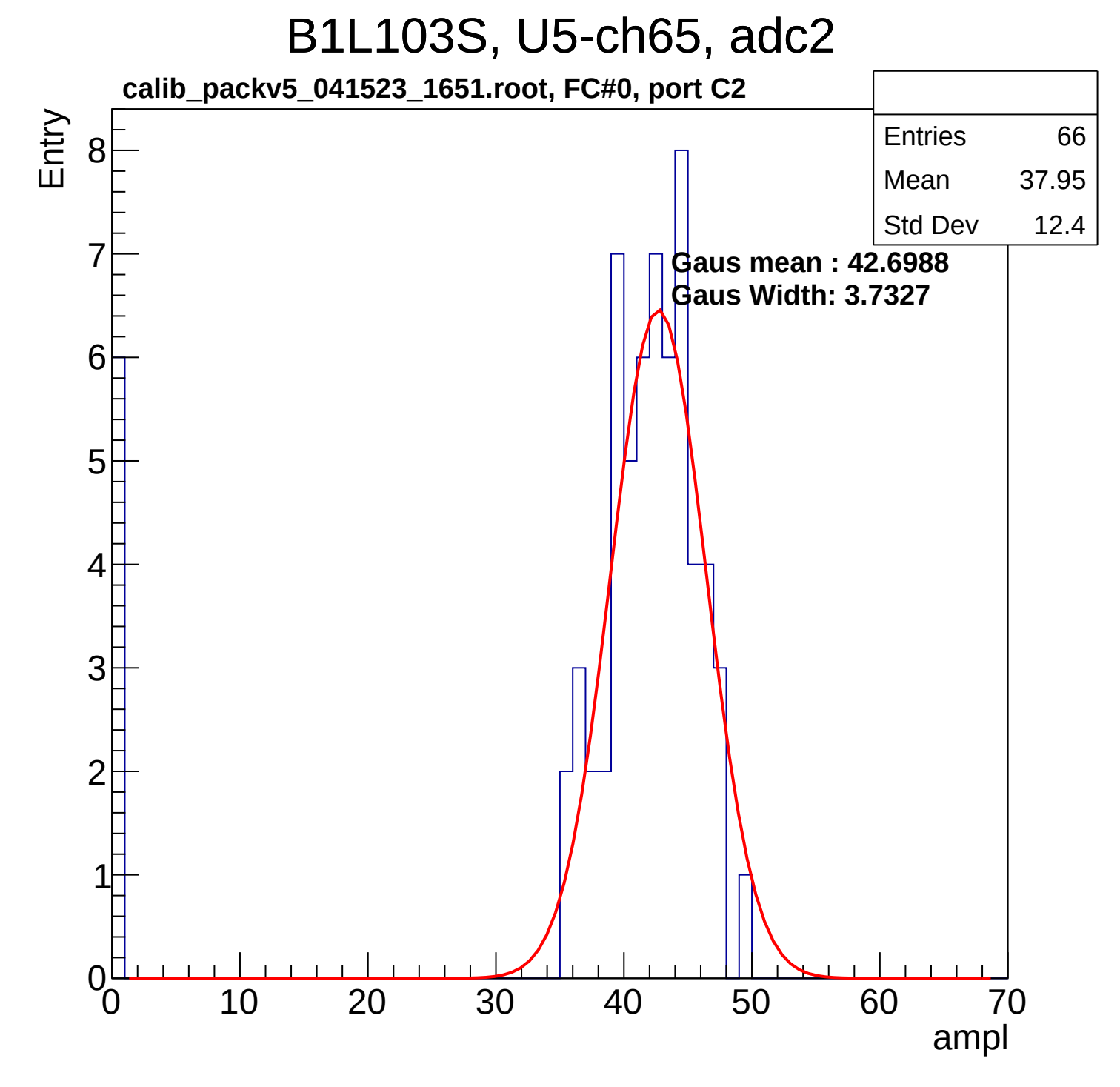
B1L103S, U5-ch65, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 37.95
Std Dev 12.4
Gaus mean : 42.6988
Gaus Width: 3.7327
Entry
ampl
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4
5
6
7
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0
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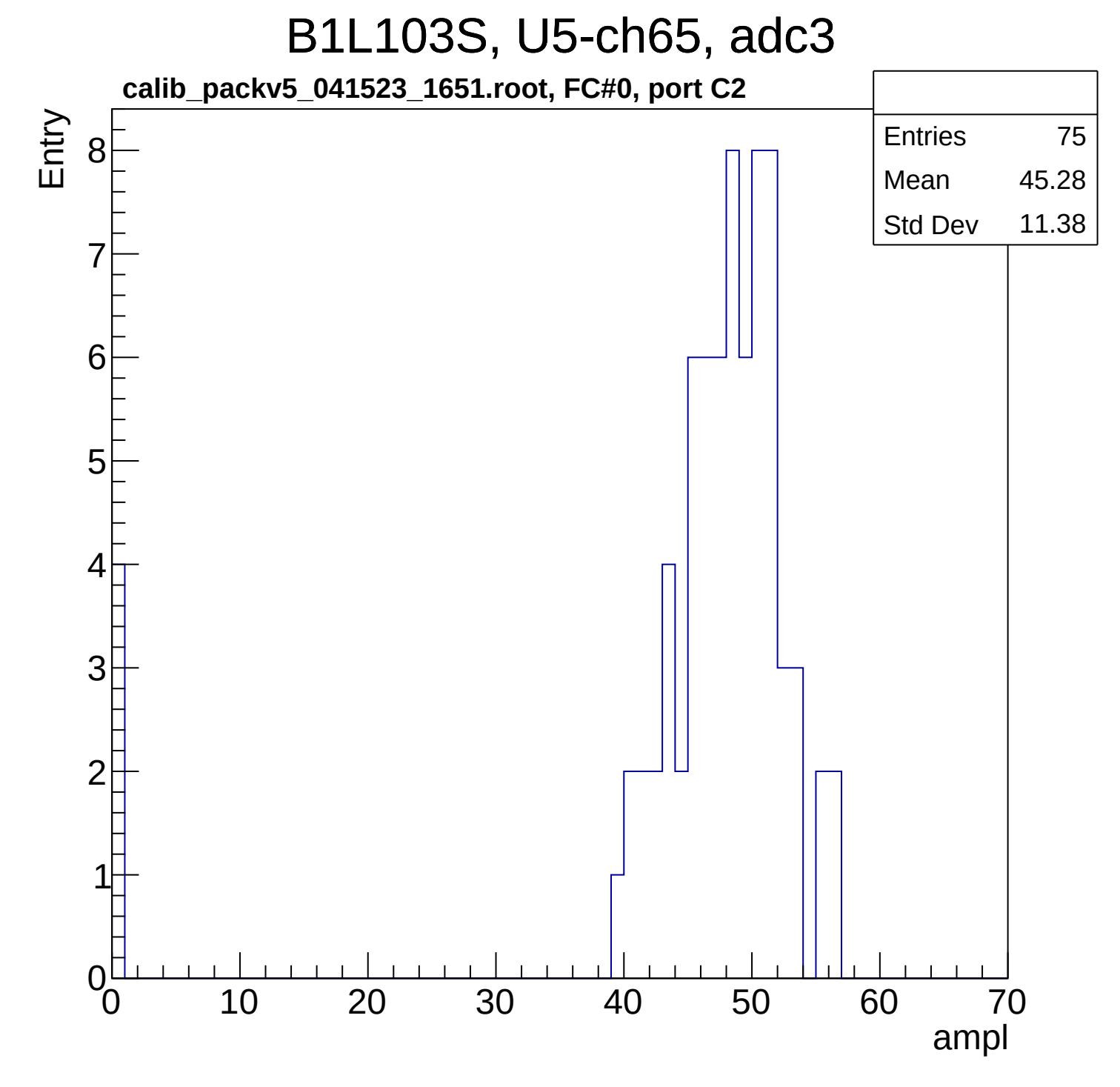
B1L103S, U5-ch65, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 45.28
Std Dev 11.38
Entry
ampl
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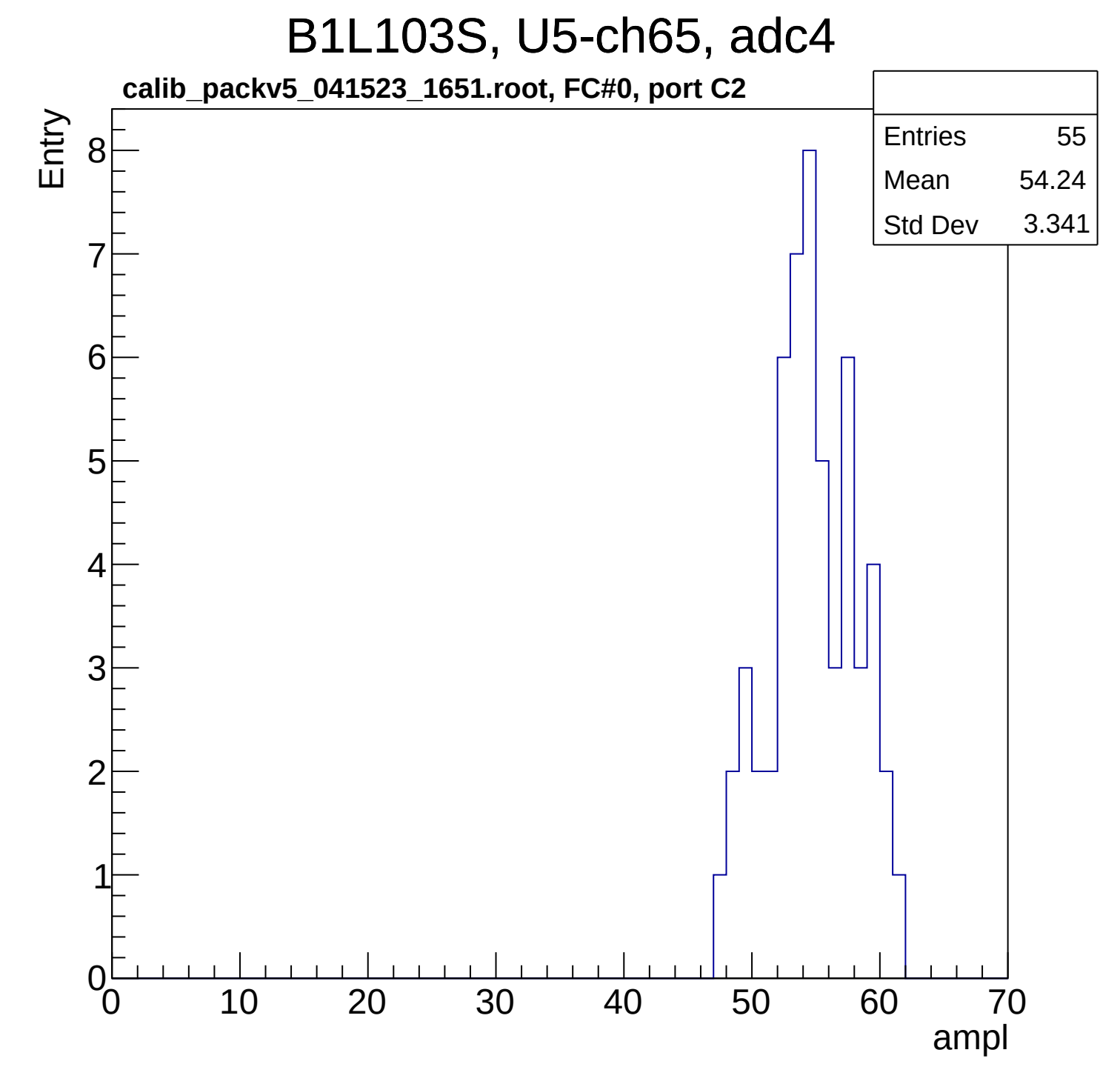
B1L103S, U5-ch65, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 54.24
Std Dev 3.341
Entry
ampl
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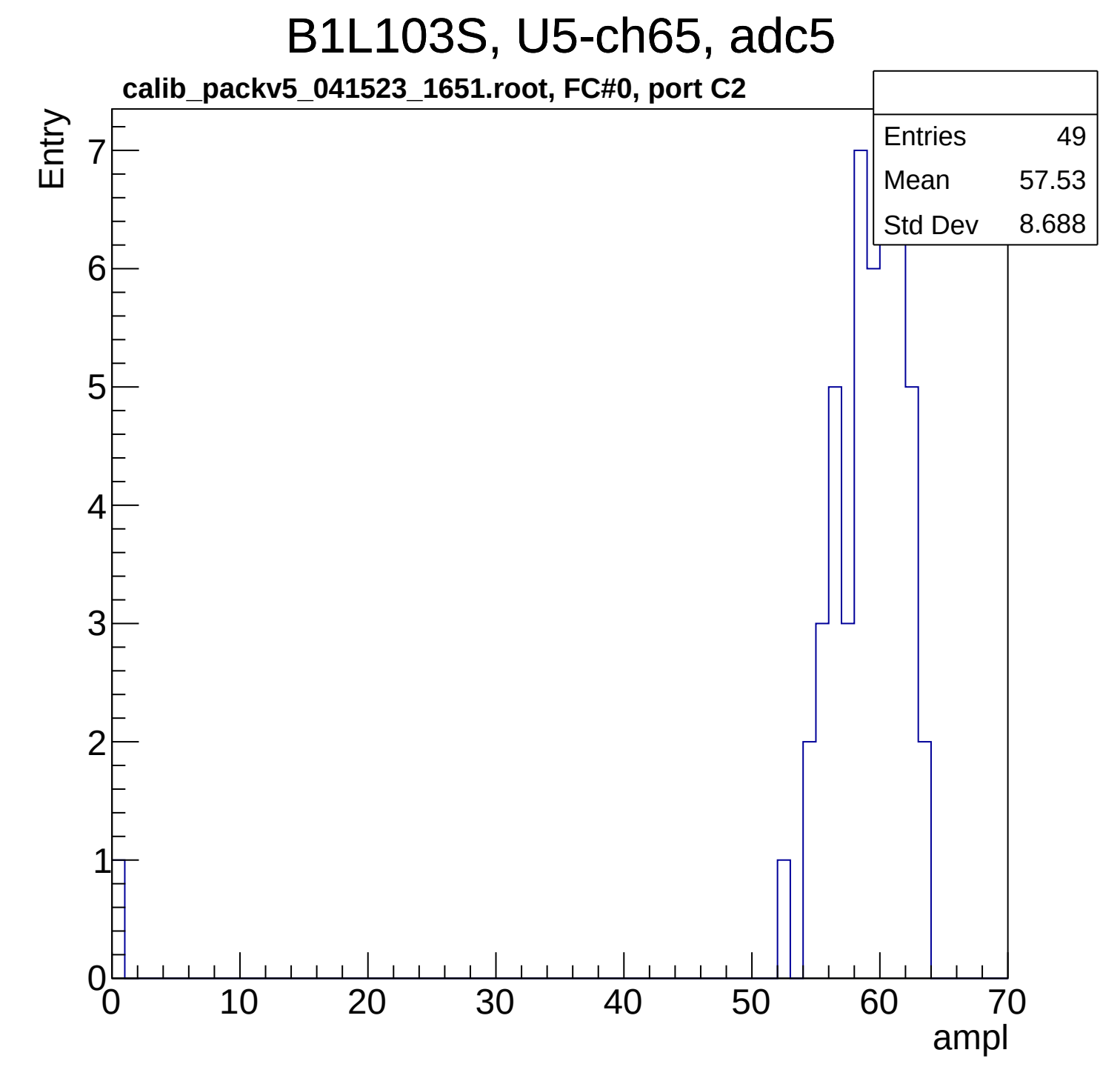
B1L103S, U5-ch65, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 57.53
Std Dev 8.688
Entry
ampl
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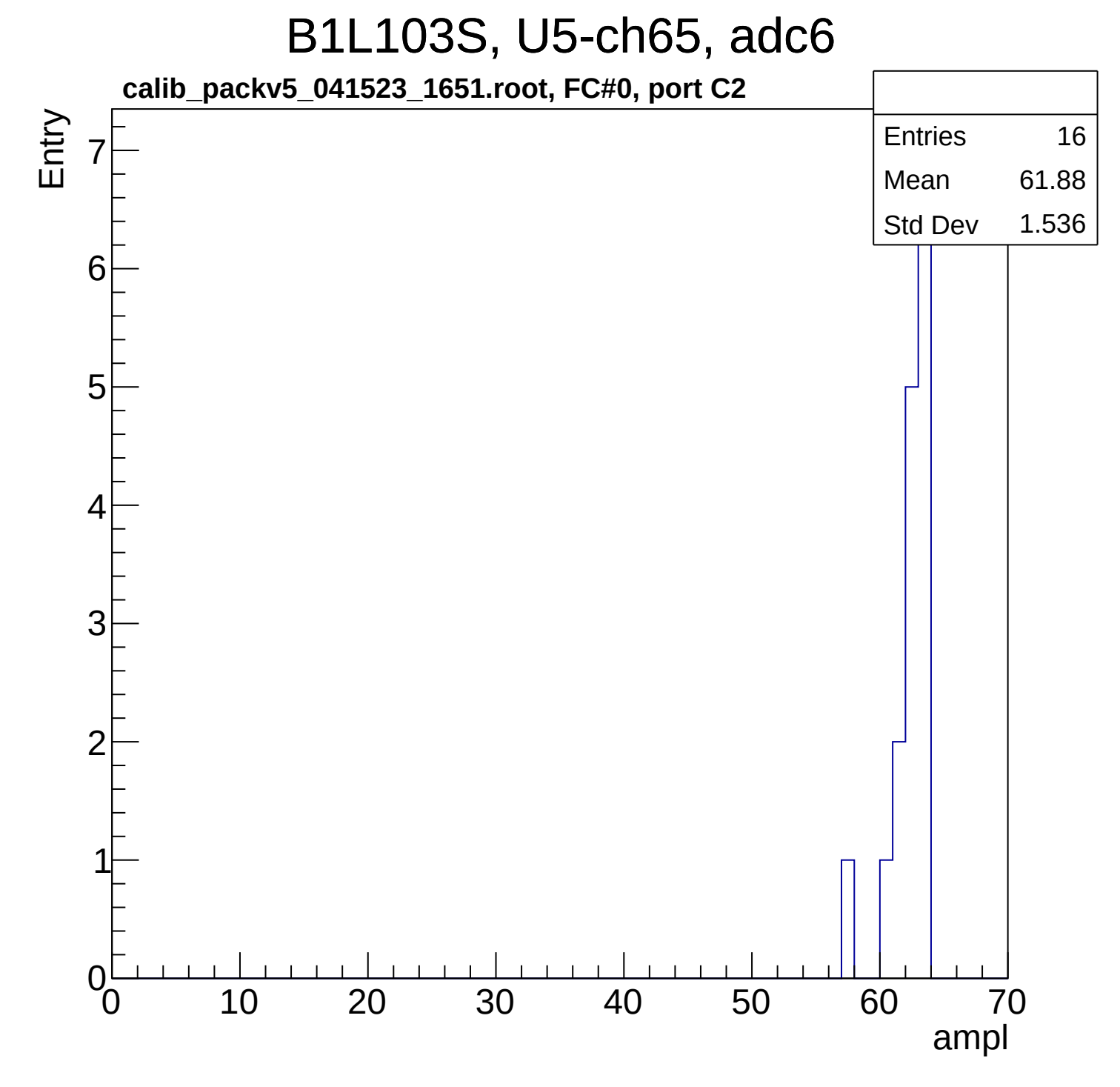
B1L103S, U5-ch65, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 61.88
Std Dev 1.536
Entry
ampl
0
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4
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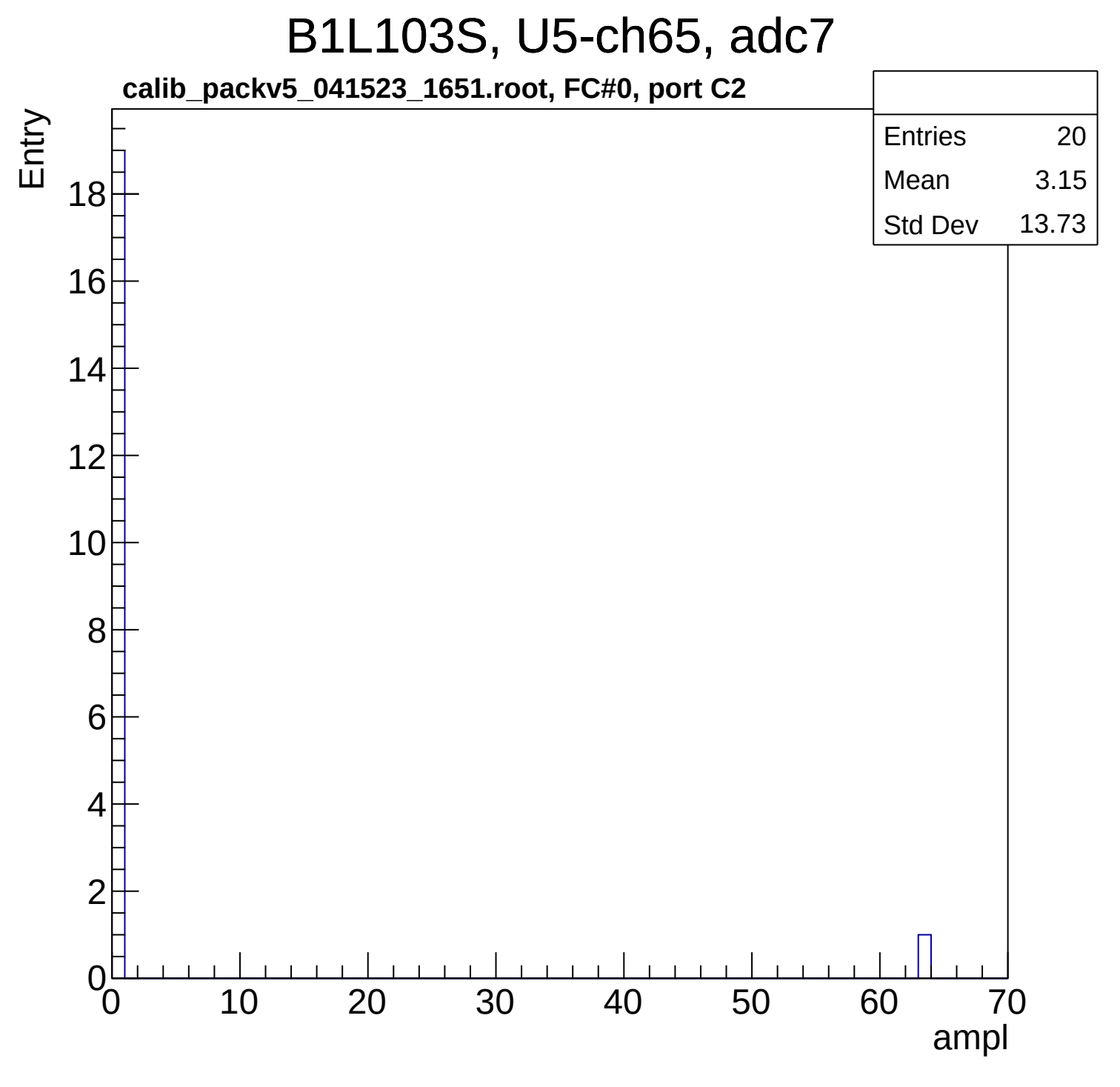
B1L103S, U5-ch65, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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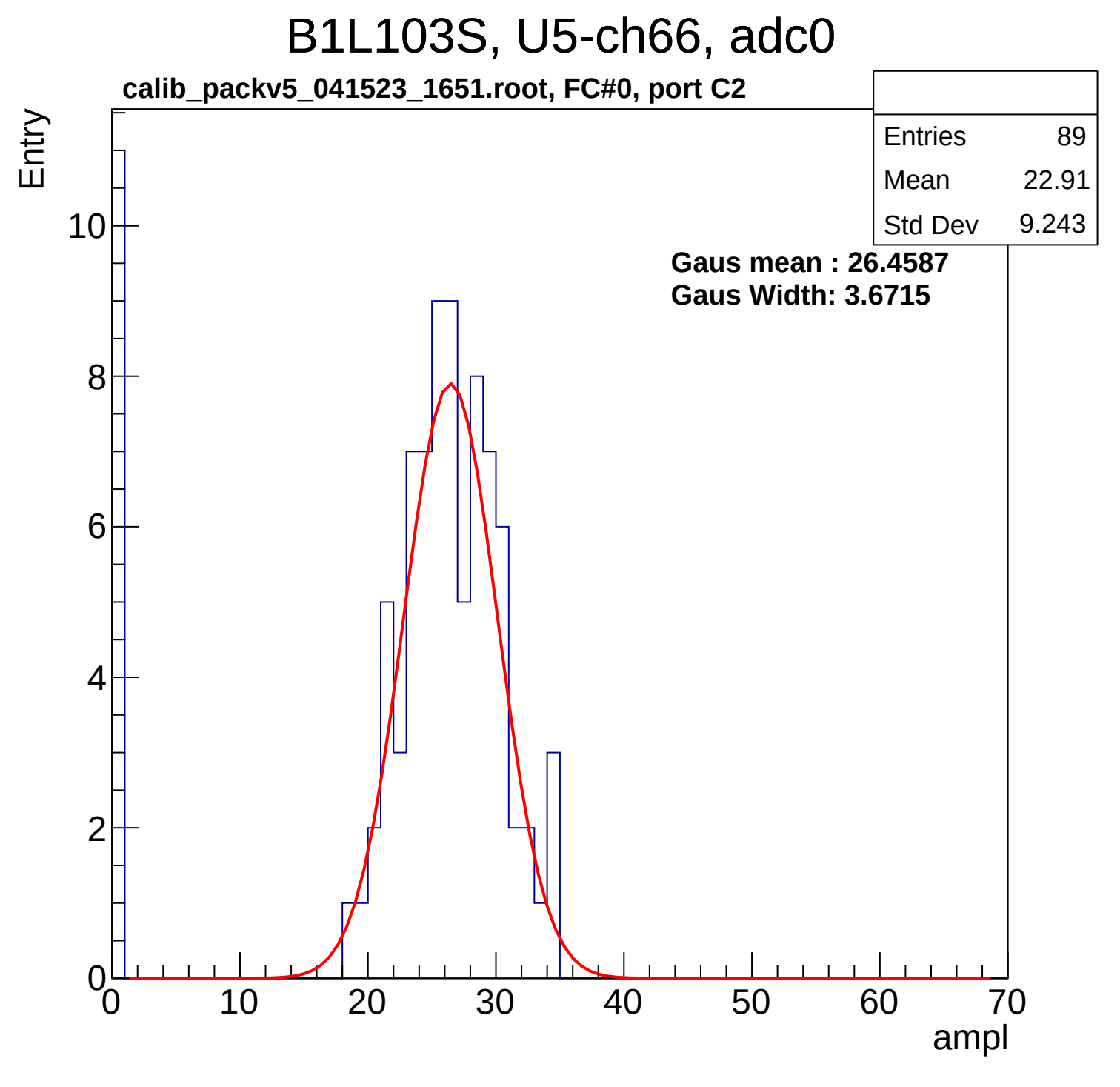
ampl


B1L103S, U5-ch66, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 22.91
Std Dev 9.243
Gaus mean : 26.4587
Gaus Width: 3.6715
Entry
ampl
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0
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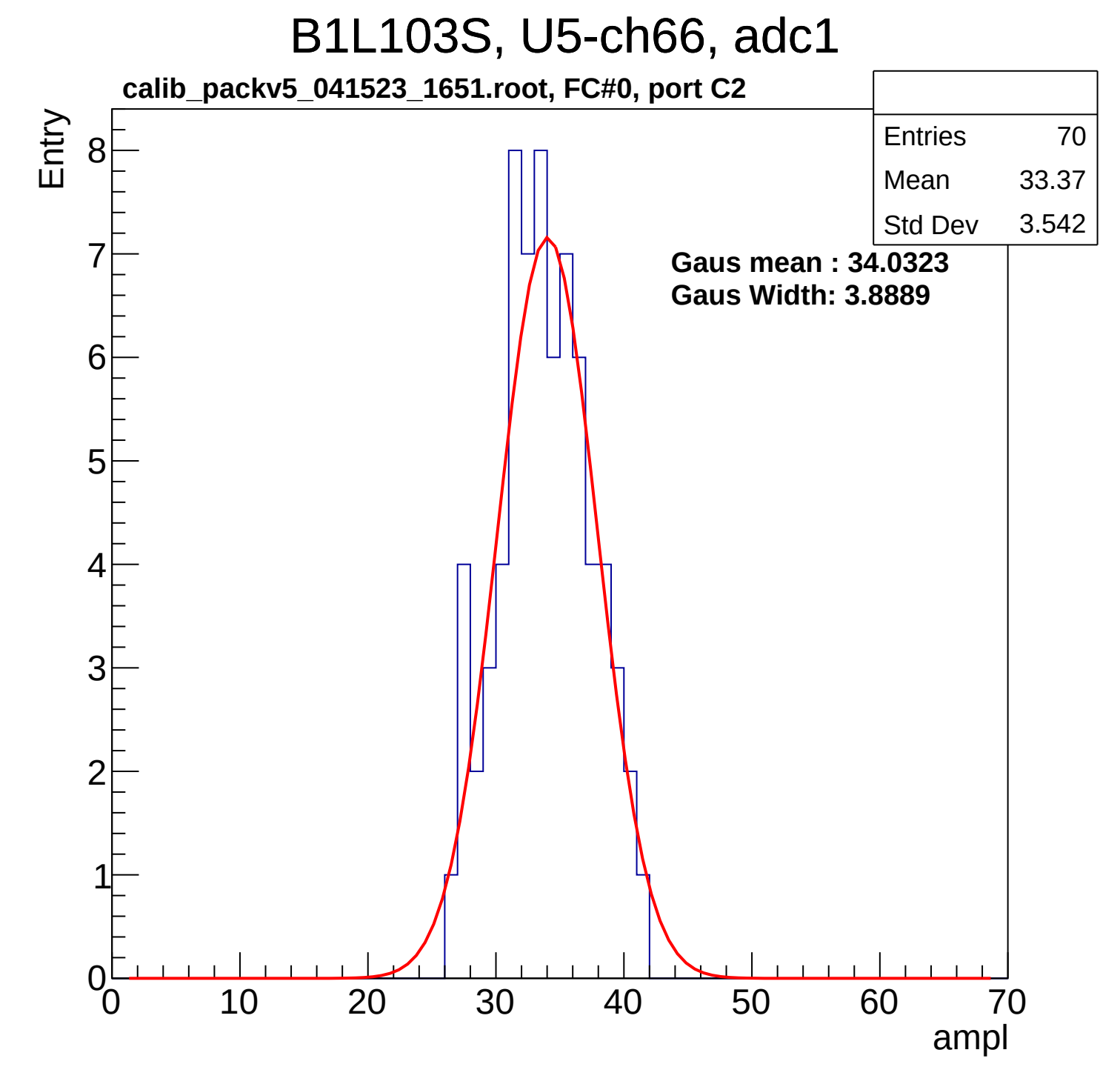
B1L103S, U5-ch66, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 33.37
Std Dev 3.542
Gaus mean : 34.0323
Gaus Width: 3.8889
Entry
ampl
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4
5
6
7
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0
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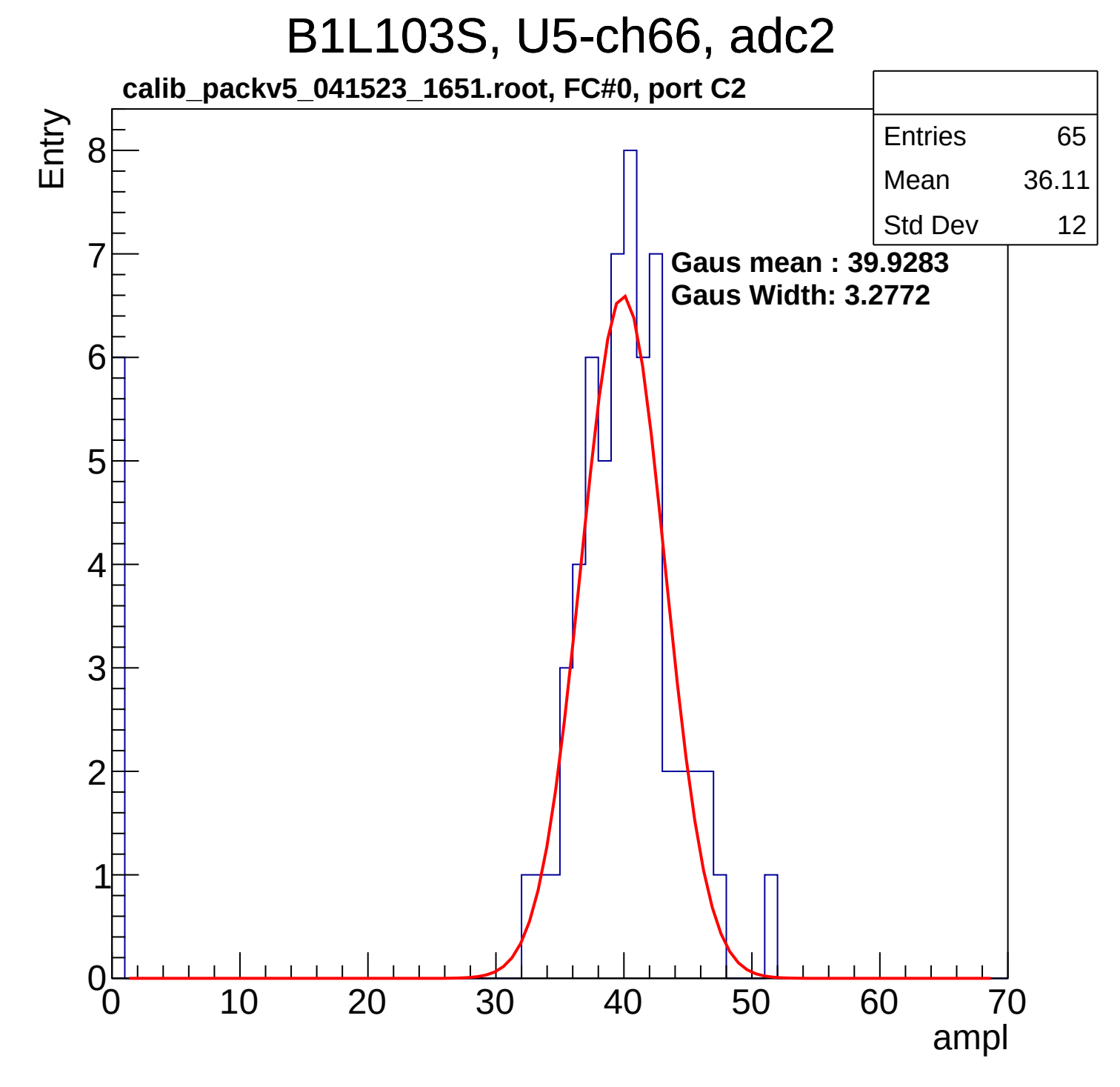
B1L103S, U5-ch66, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 36.11
Std Dev 12
Gaus mean : 39.9283
Gaus Width: 3.2772
Entry
ampl
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4
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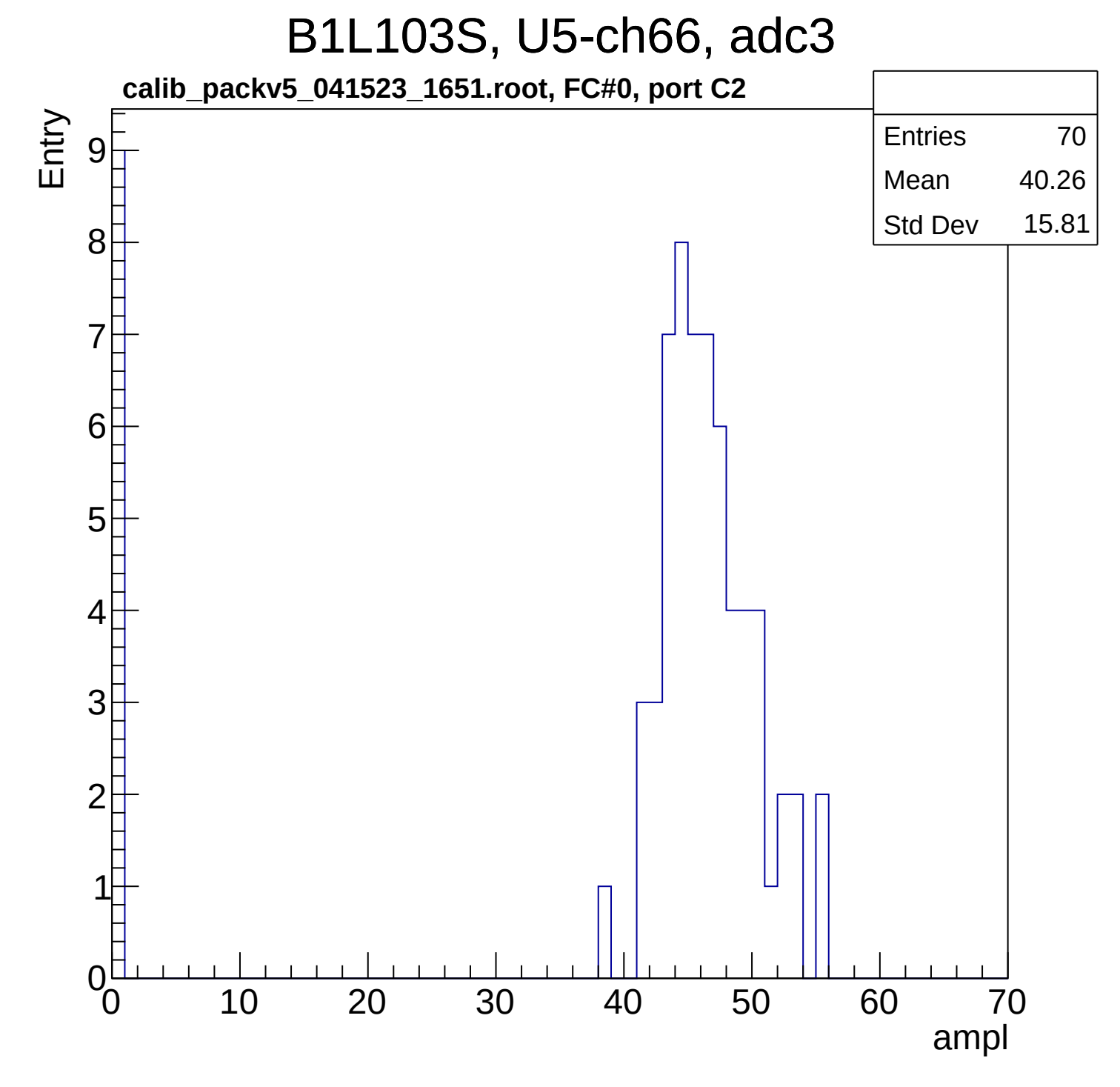
B1L103S, U5-ch66, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 40.26
Std Dev 15.81
Entry
ampl
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2
3
4
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6
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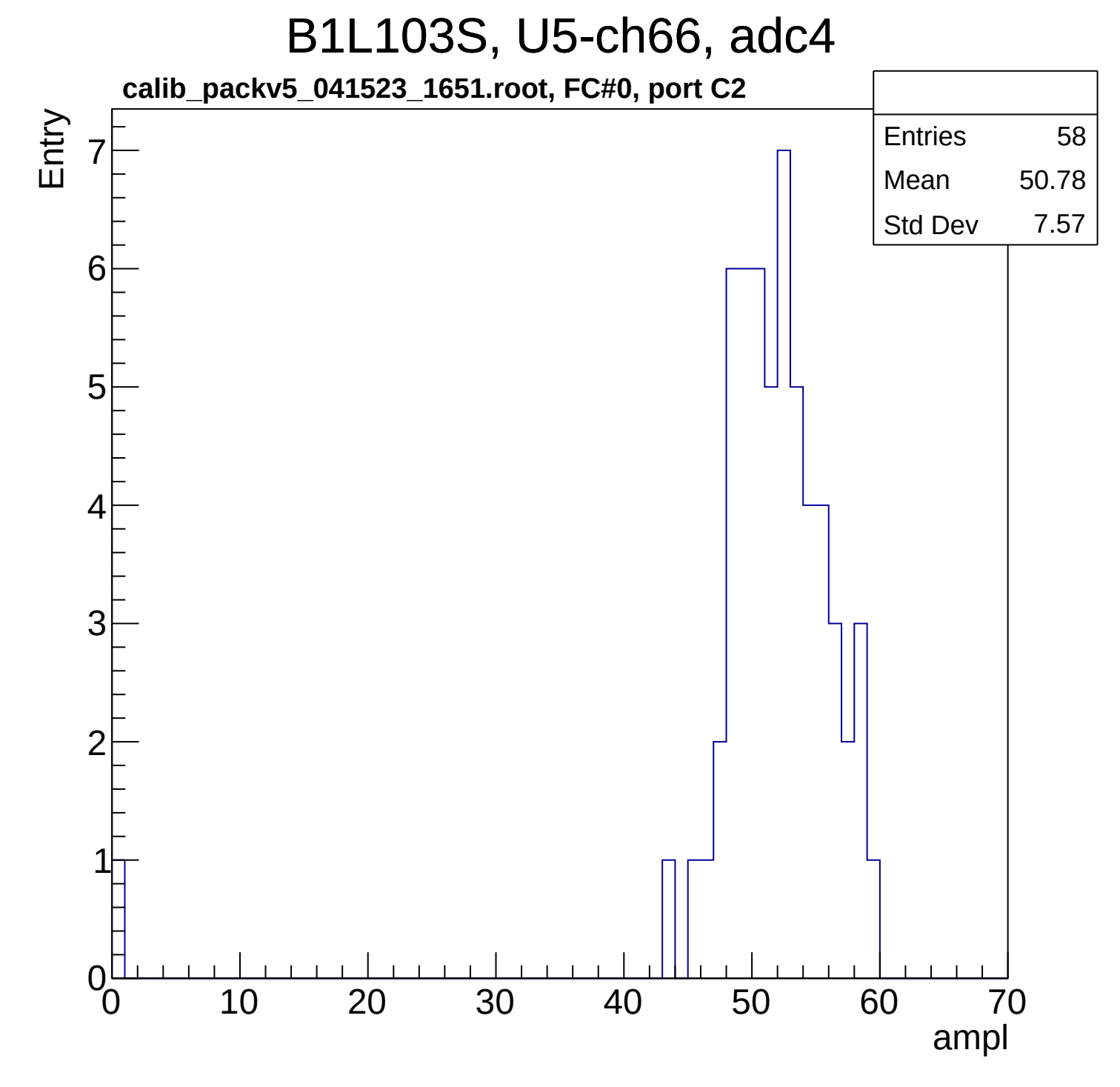
B1L103S, U5-ch66, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 50.78
Std Dev 7.57
Entry
ampl
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1
2
3
4
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6
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0
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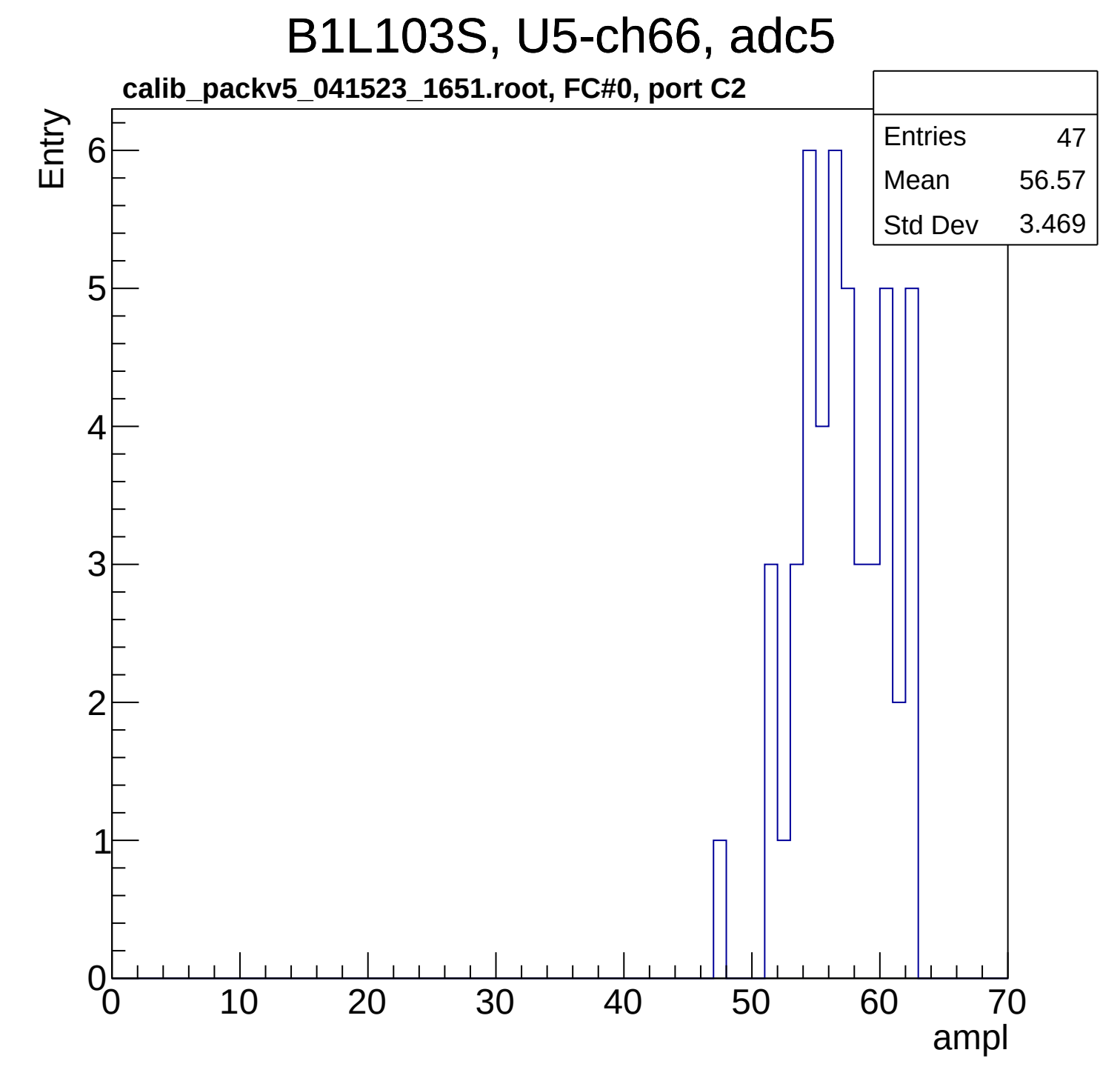
B1L103S, U5-ch66, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 56.57
Std Dev 3.469
Entry
ampl
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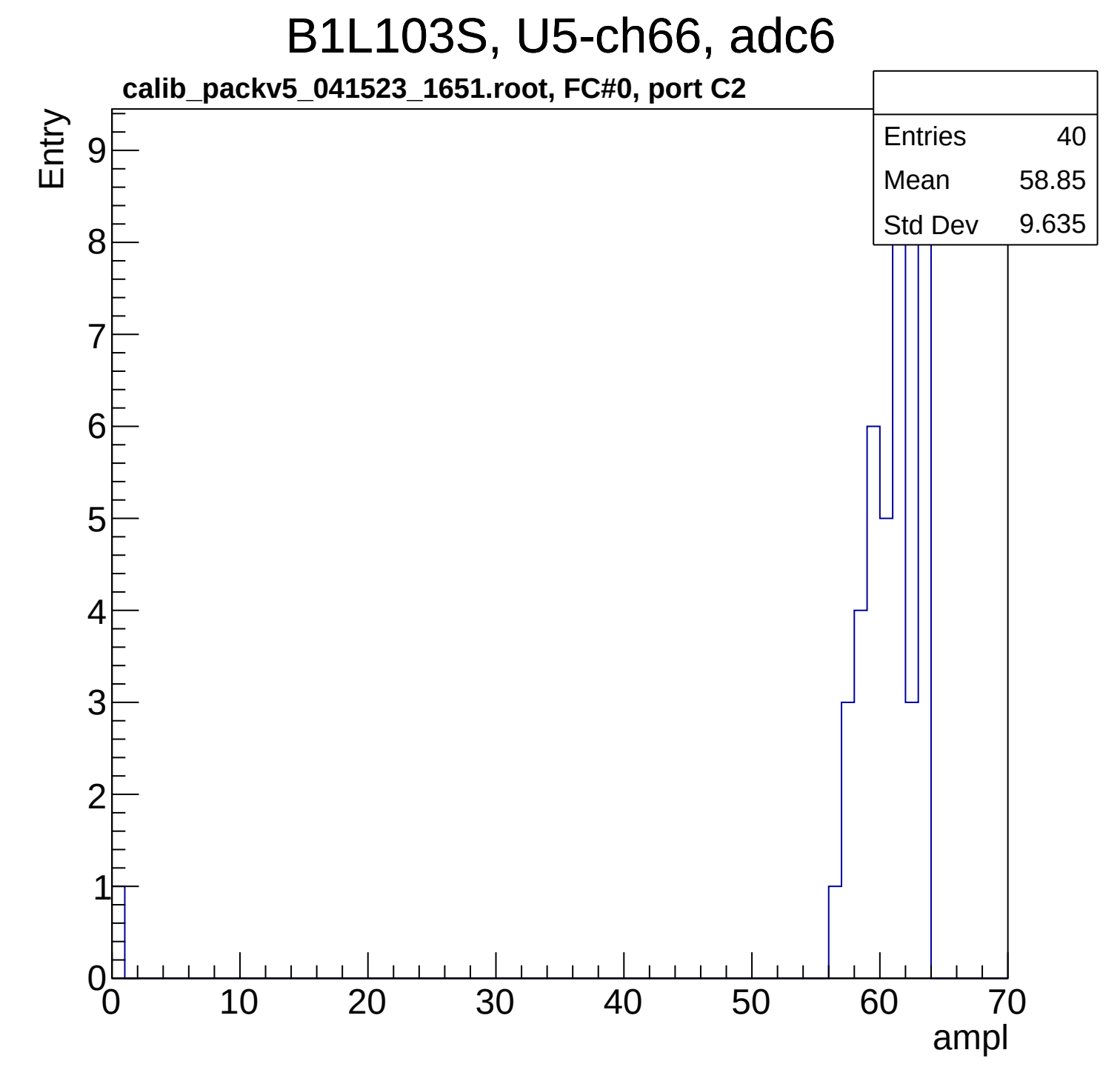
B1L103S, U5-ch66, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 58.85
Std Dev 9.635
Entry
ampl
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0
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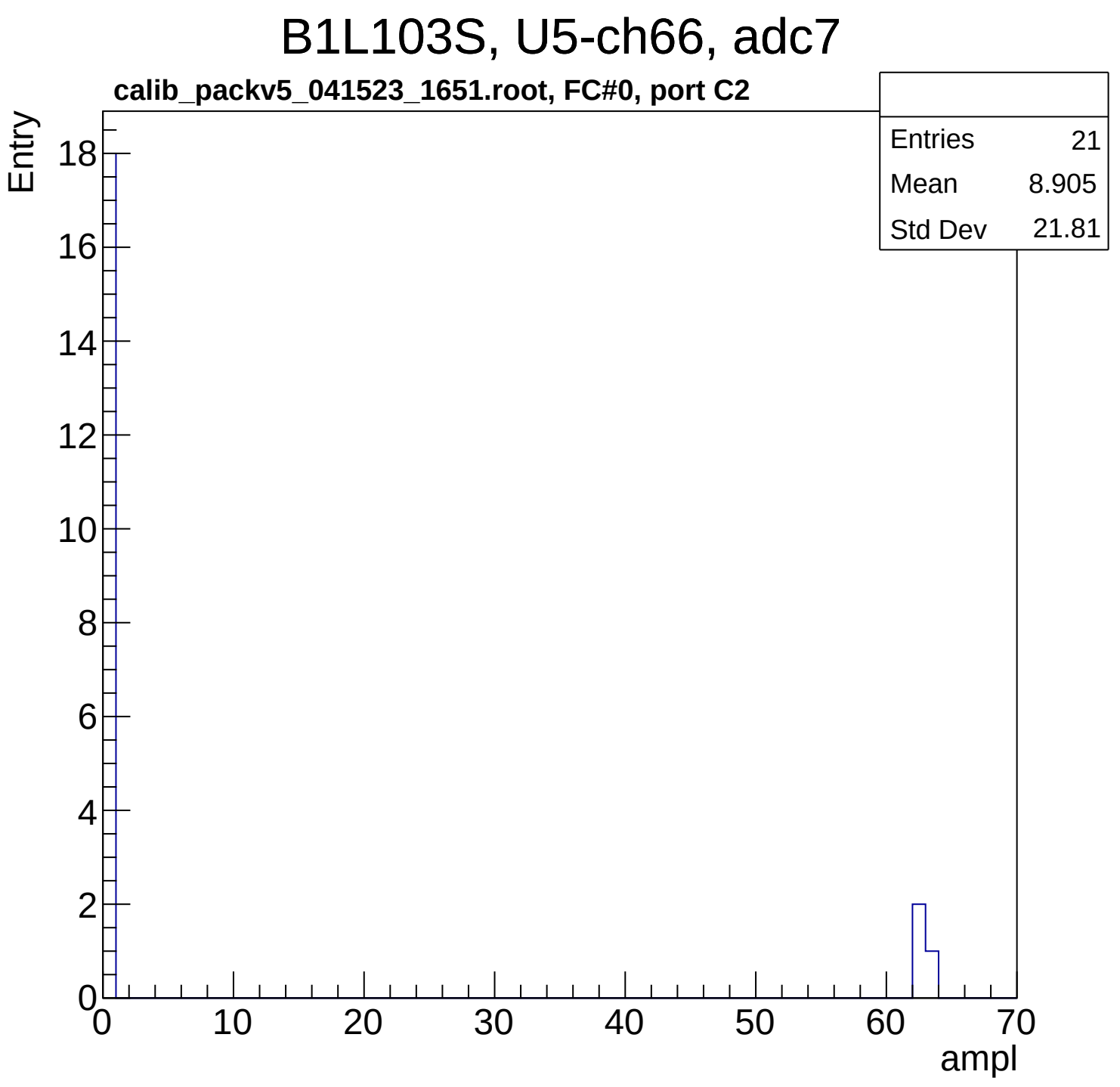
B1L103S, U5-ch66, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 8.905
Std Dev 21.81
Entry
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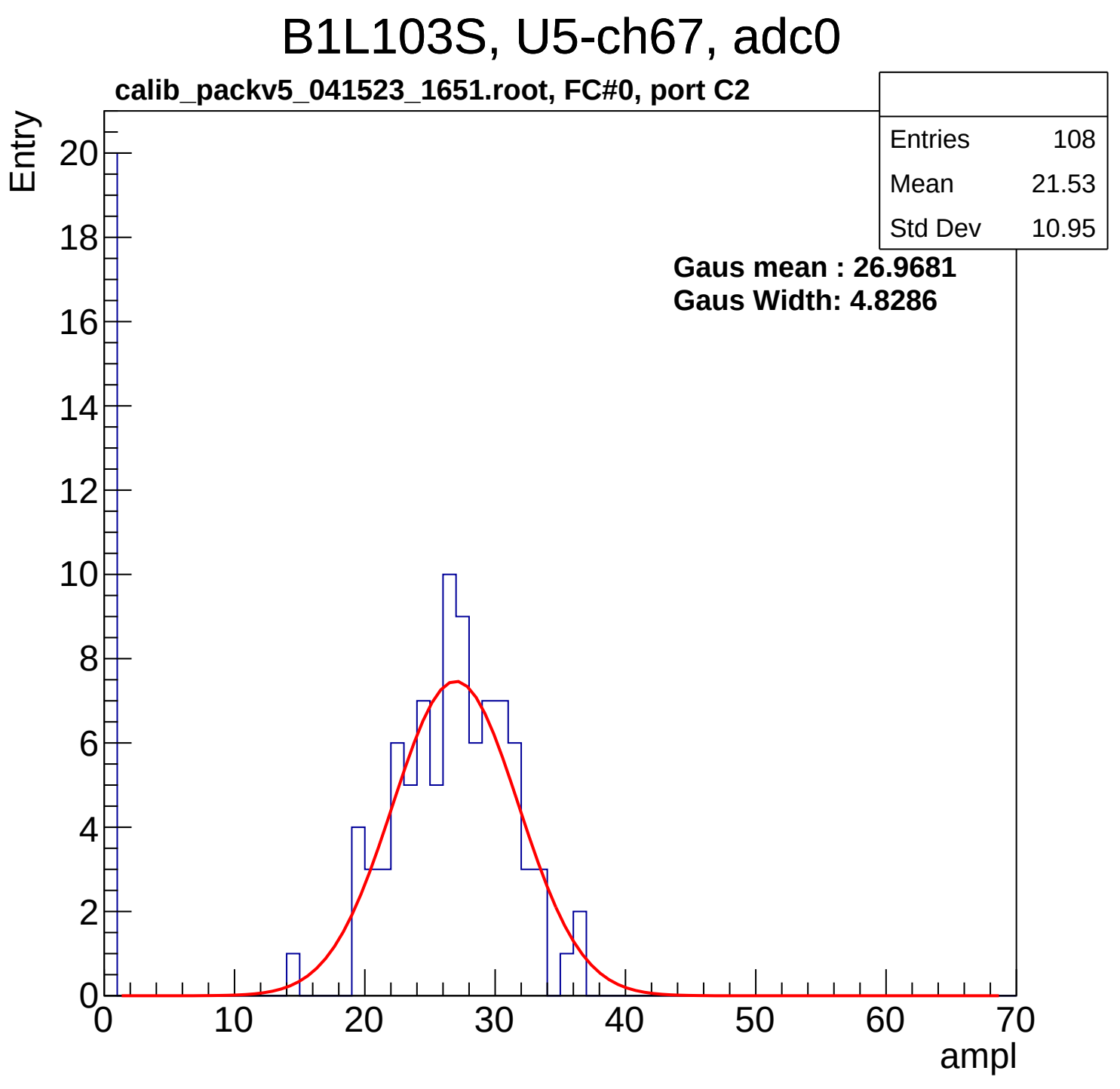
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch67, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 108
Mean 21.53
Std Dev 10.95
Gaus mean : 26.9681
Gaus Width: 4.8286
Entry
ampl
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6
8
10
12
14
16
18
20
0
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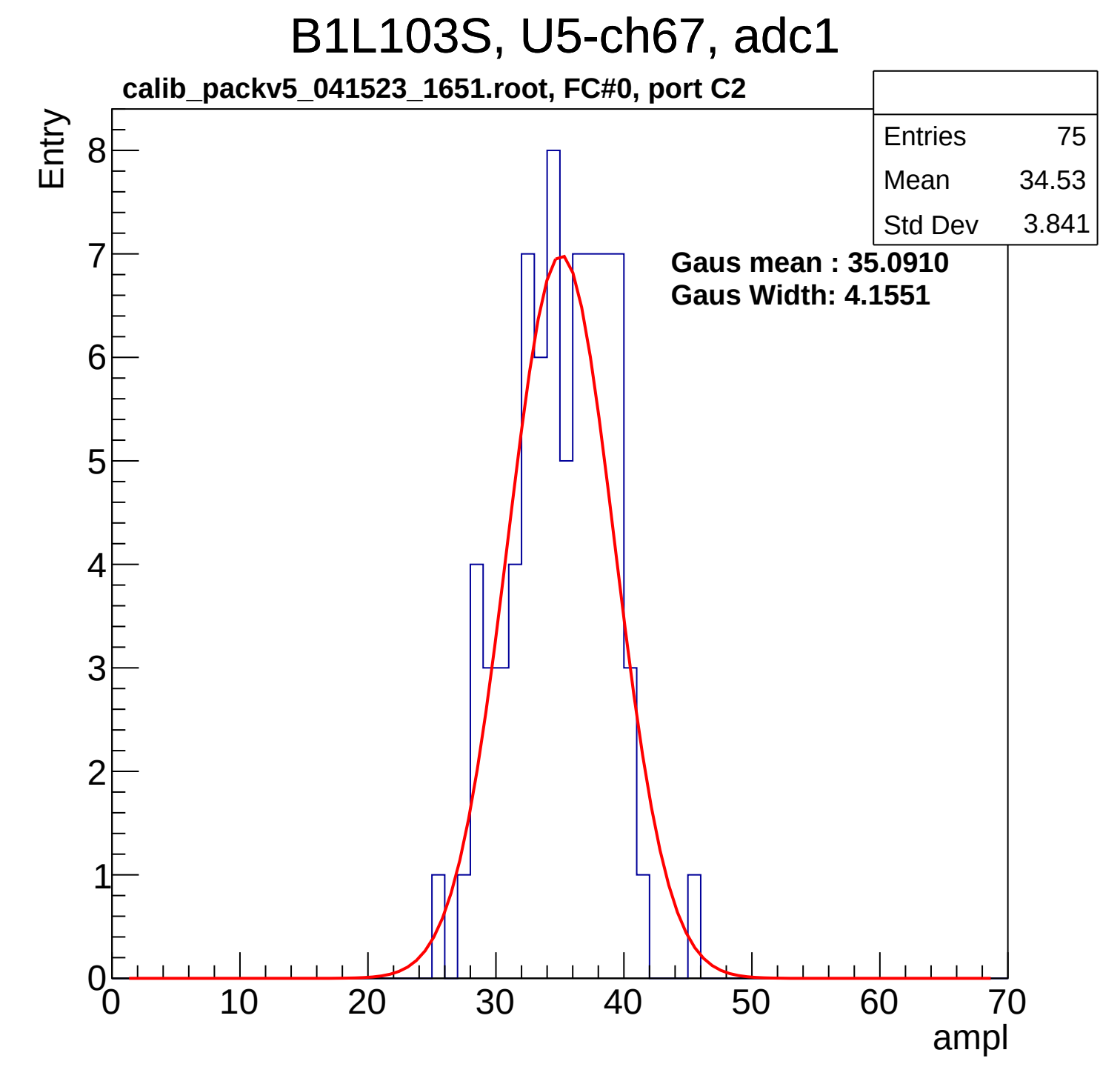
B1L103S, U5-ch67, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 34.53
Std Dev 3.841
Gaus mean : 35.0910
Gaus Width: 4.1551
Entry
ampl
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3
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5
6
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0
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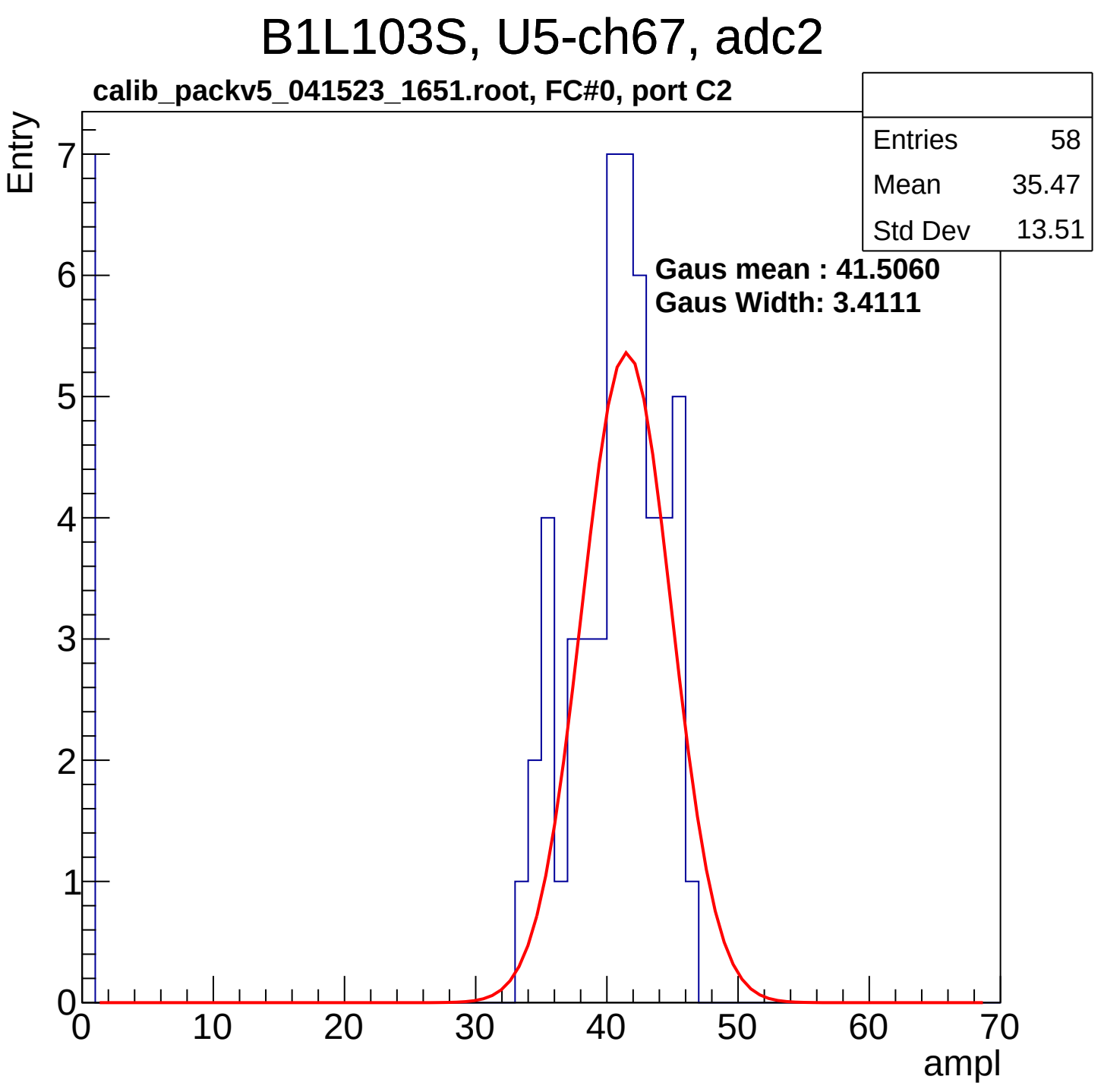
B1L103S, U5-ch67, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 35.47
Std Dev 13.51
Gaus mean : 41.5060
Gaus Width: 3.4111
Entry
ampl
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4
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6
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0
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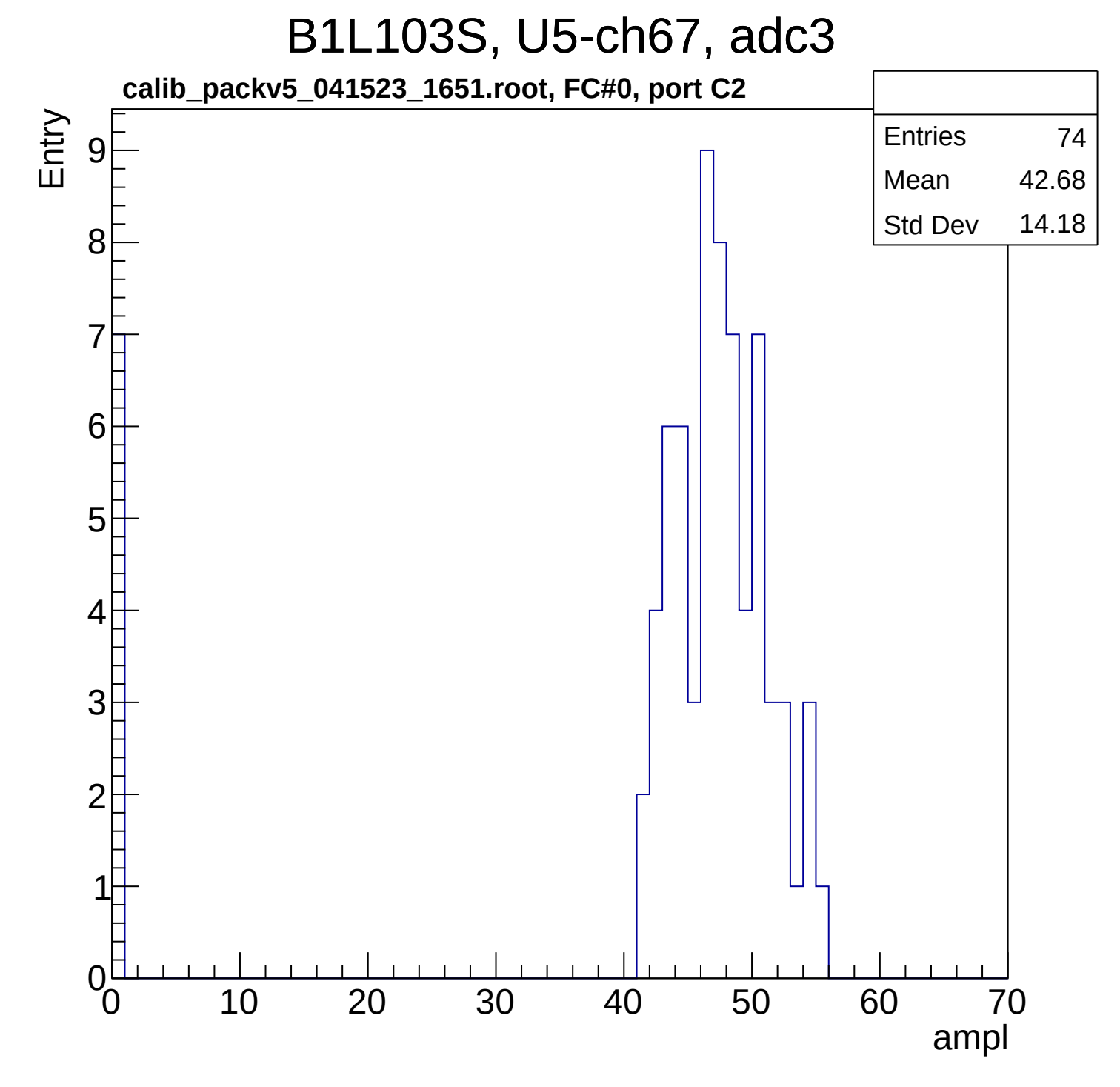
B1L103S, U5-ch67, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 42.68
Std Dev 14.18
Entry
ampl
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3
4
5
6
7
8
9
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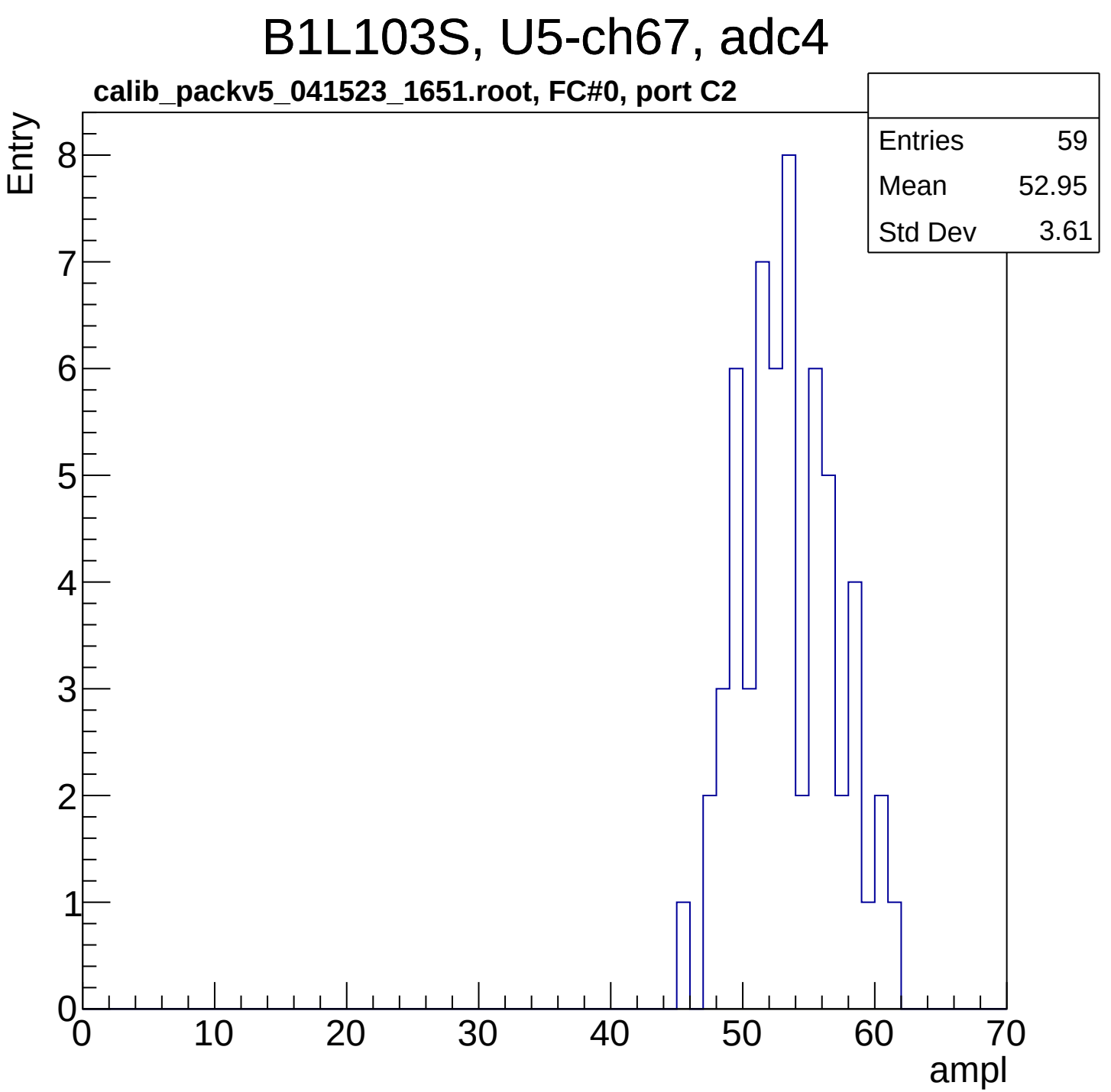
B1L103S, U5-ch67, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 52.95
Std Dev 3.61
Entry
ampl
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5
6
7
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0
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20
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60
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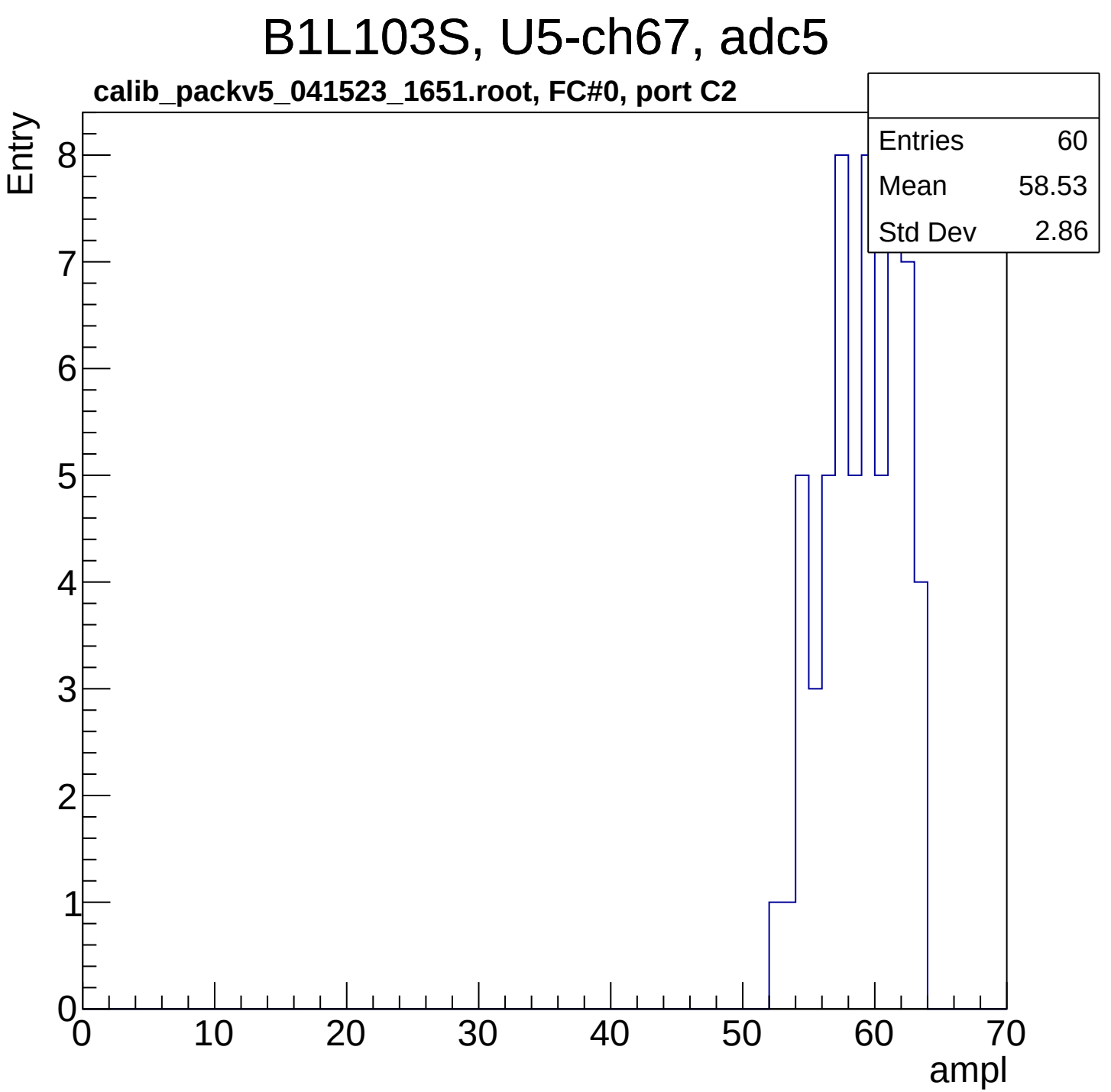
B1L103S, U5-ch67, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 58.53
Std Dev 2.86
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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60
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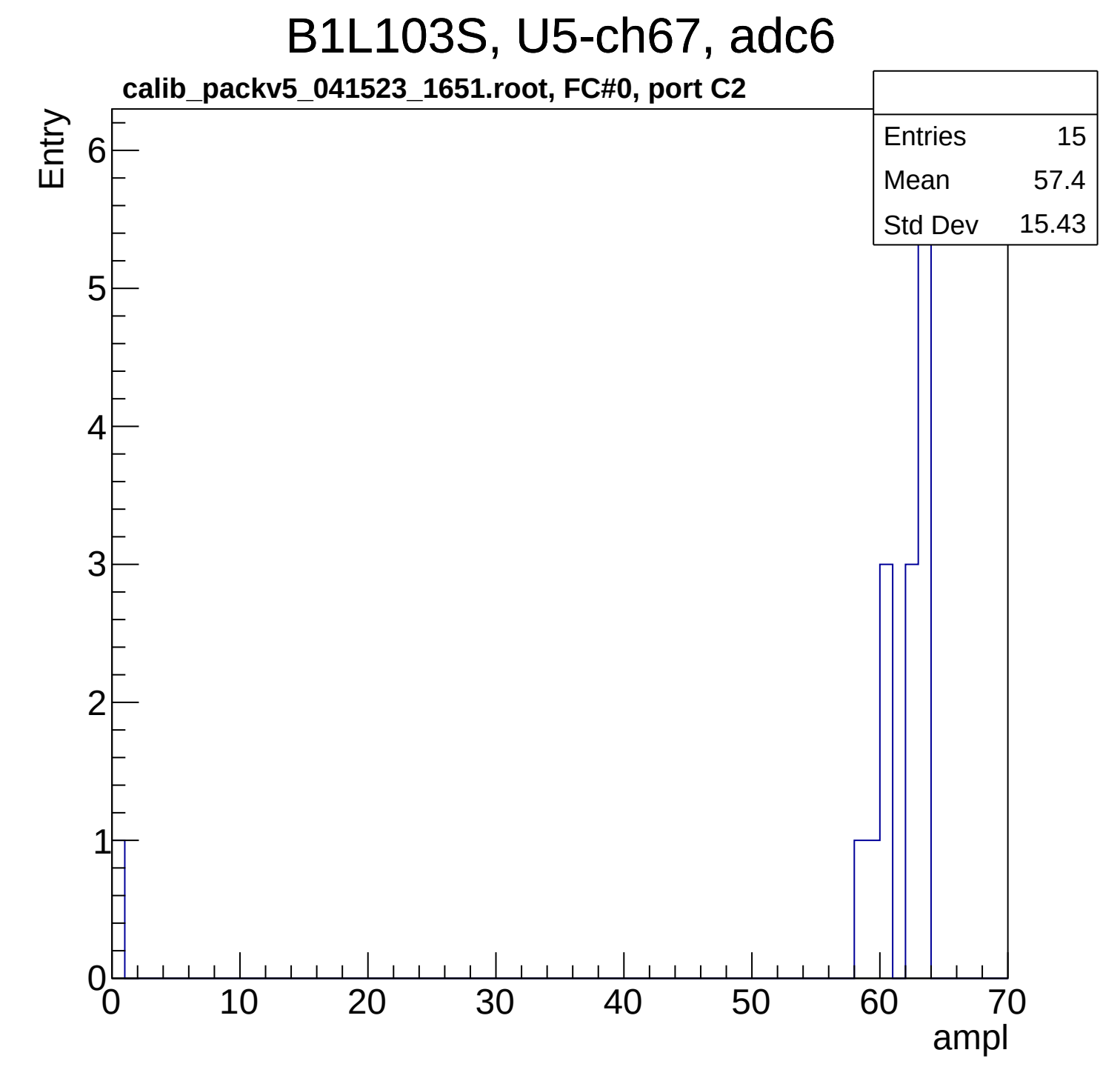
B1L103S, U5-ch67, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.4
Std Dev 15.43
Entry
ampl
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1
2
3
4
5
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20
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40
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60
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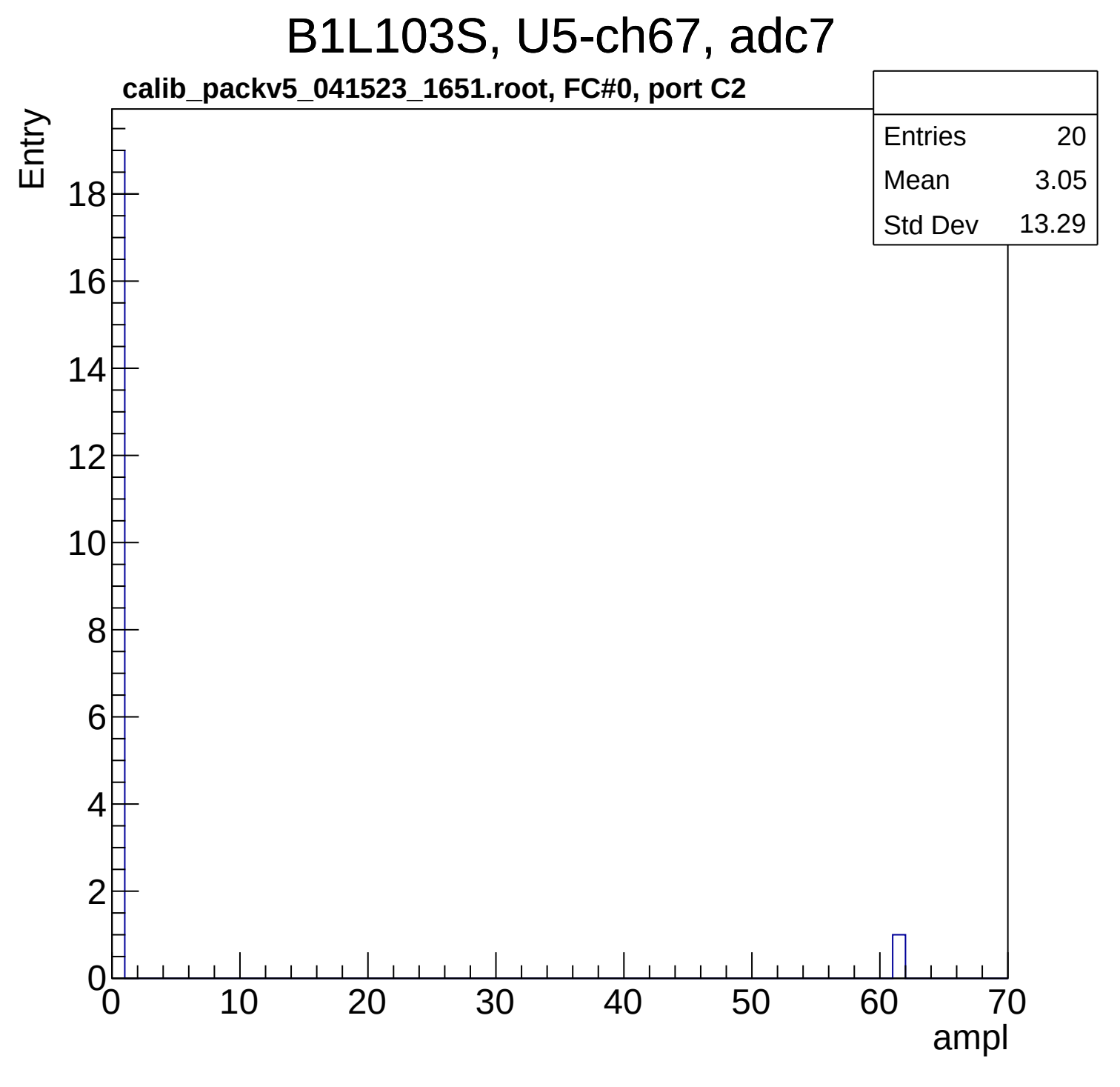
B1L103S, U5-ch67, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
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8
10
12
14
16
18
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10
20
30
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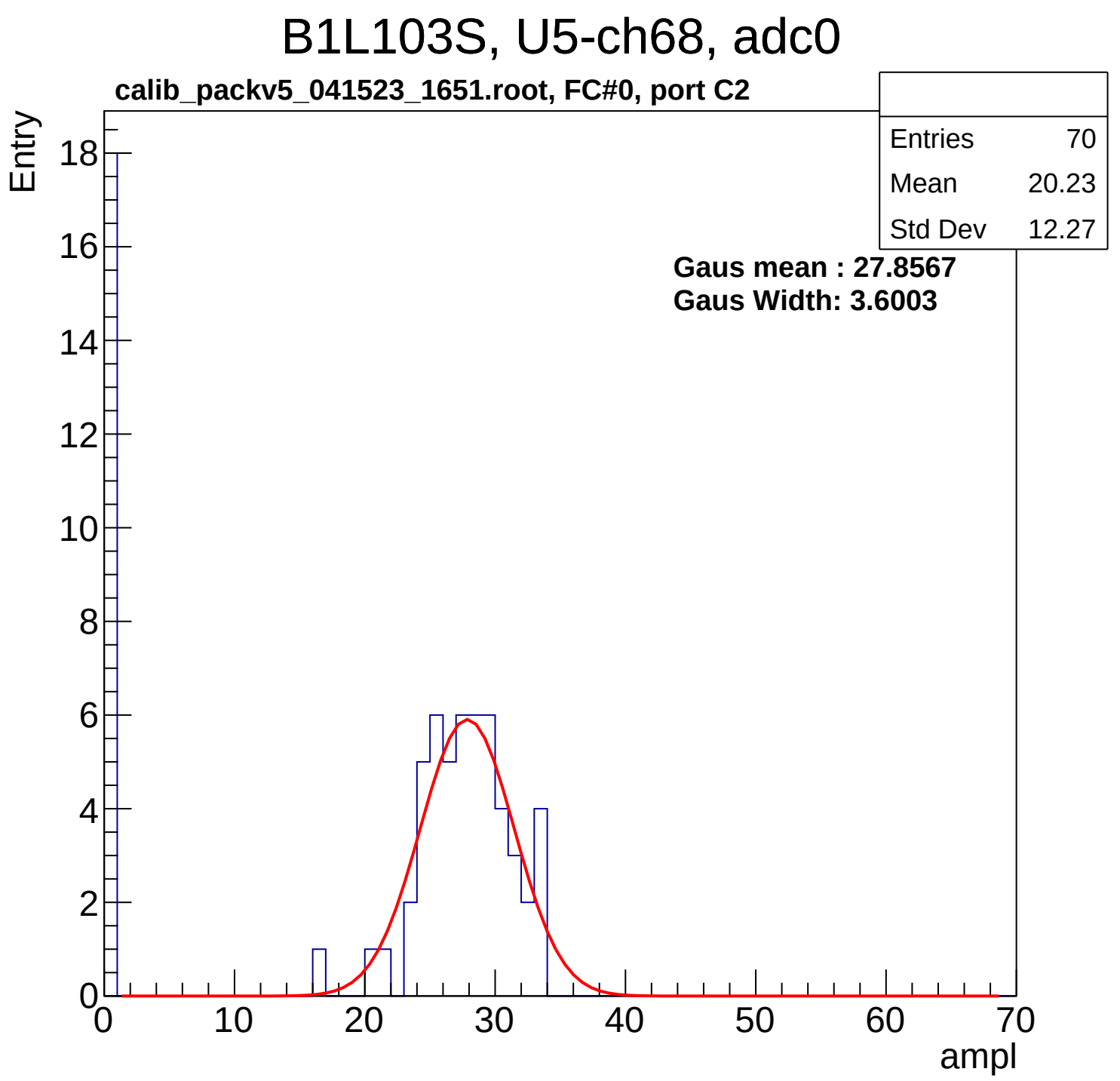
50
60
70
ampl


B1L103S, U5-ch68, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 20.23
Std Dev 12.27
Gaus mean : 27.8567
Gaus Width: 3.6003
Entry
ampl
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4
6
8
10
12
14
16
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0
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20
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40
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60
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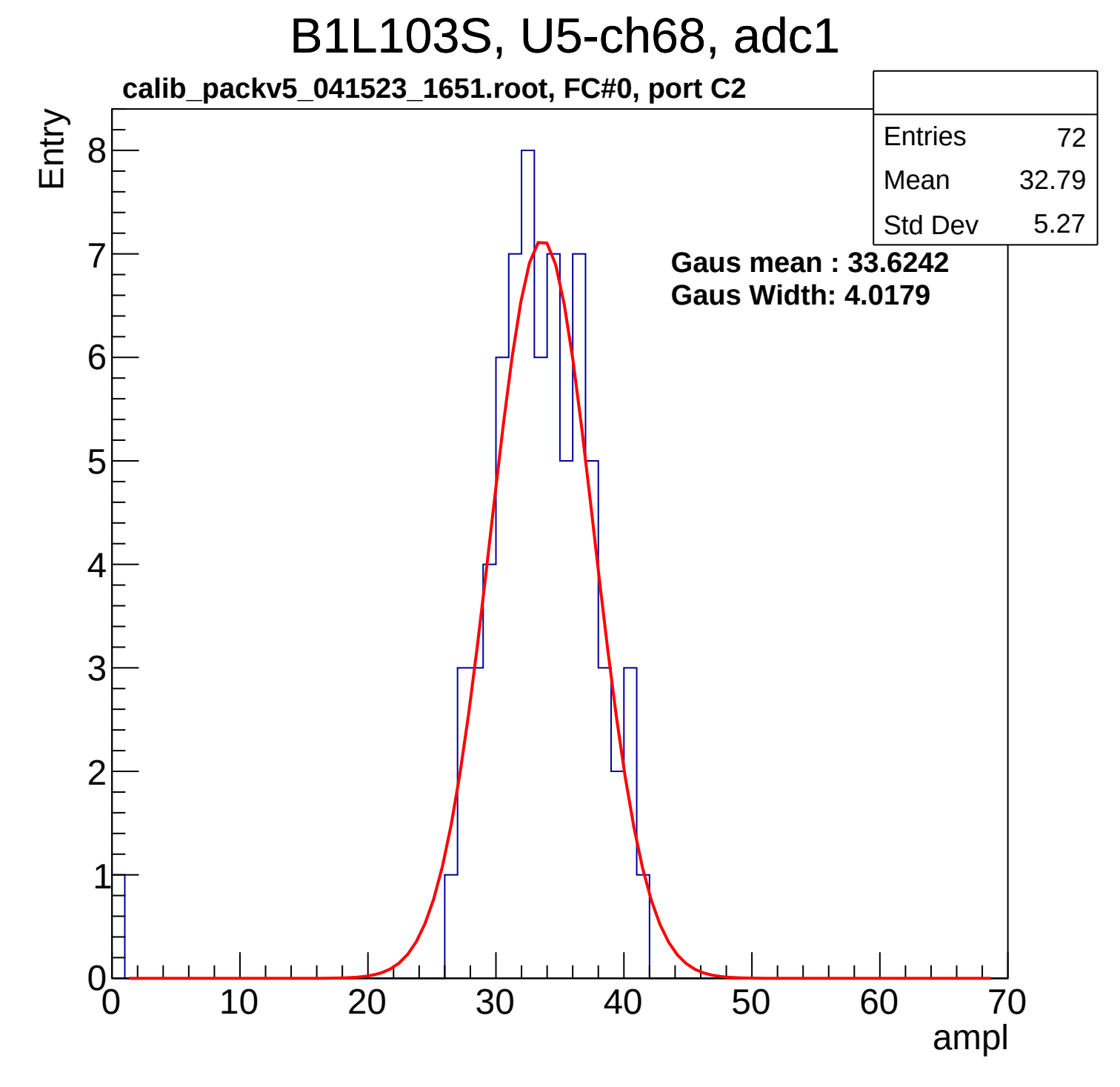
B1L103S, U5-ch68, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 32.79
Std Dev 5.27
Gaus mean : 33.6242
Gaus Width: 4.0179
Entry
ampl
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2
3
4
5
6
7
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0
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20
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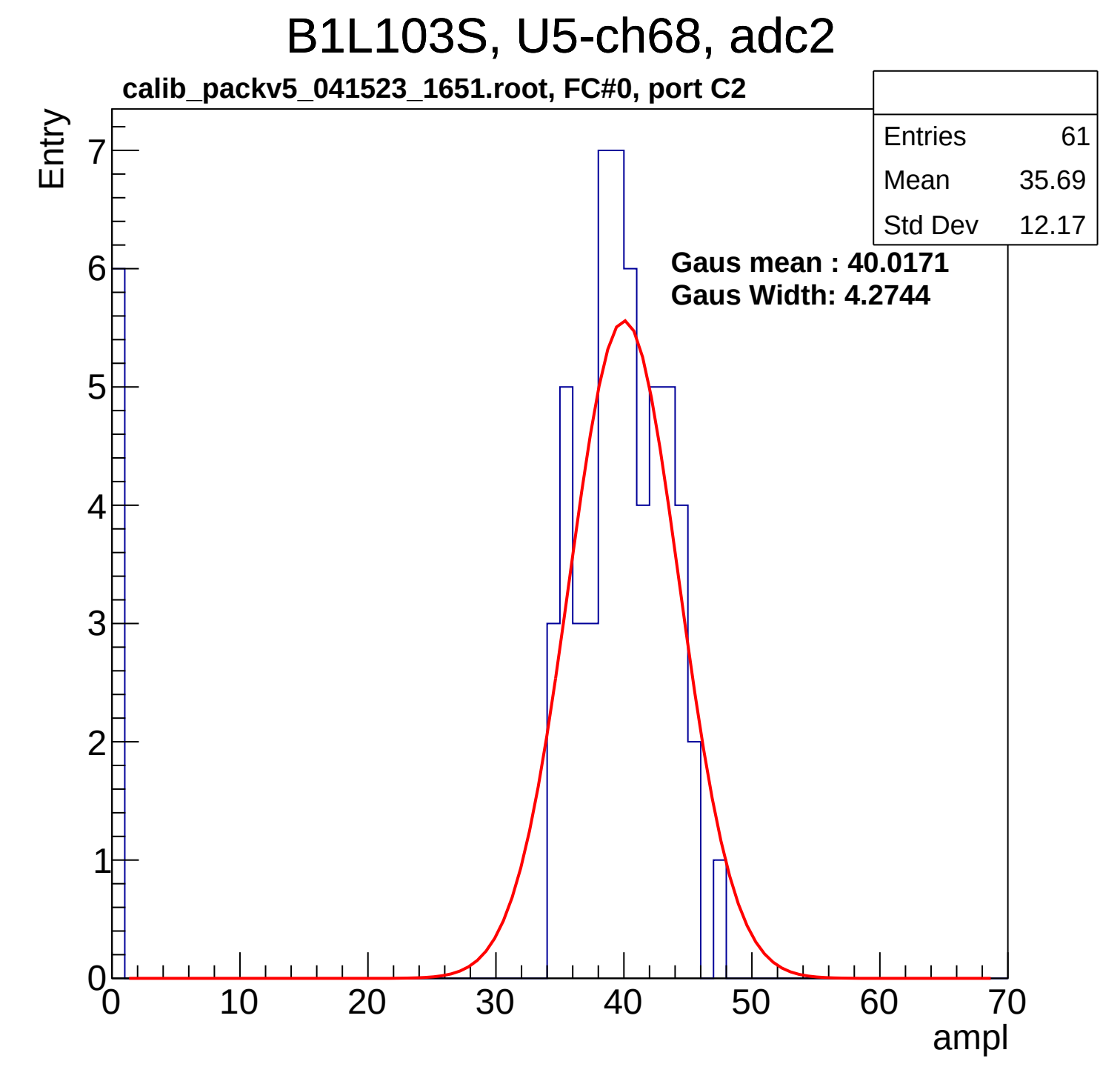
B1L103S, U5-ch68, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 35.69
Std Dev 12.17
Gaus mean : 40.0171
Gaus Width: 4.2744
Entry
ampl
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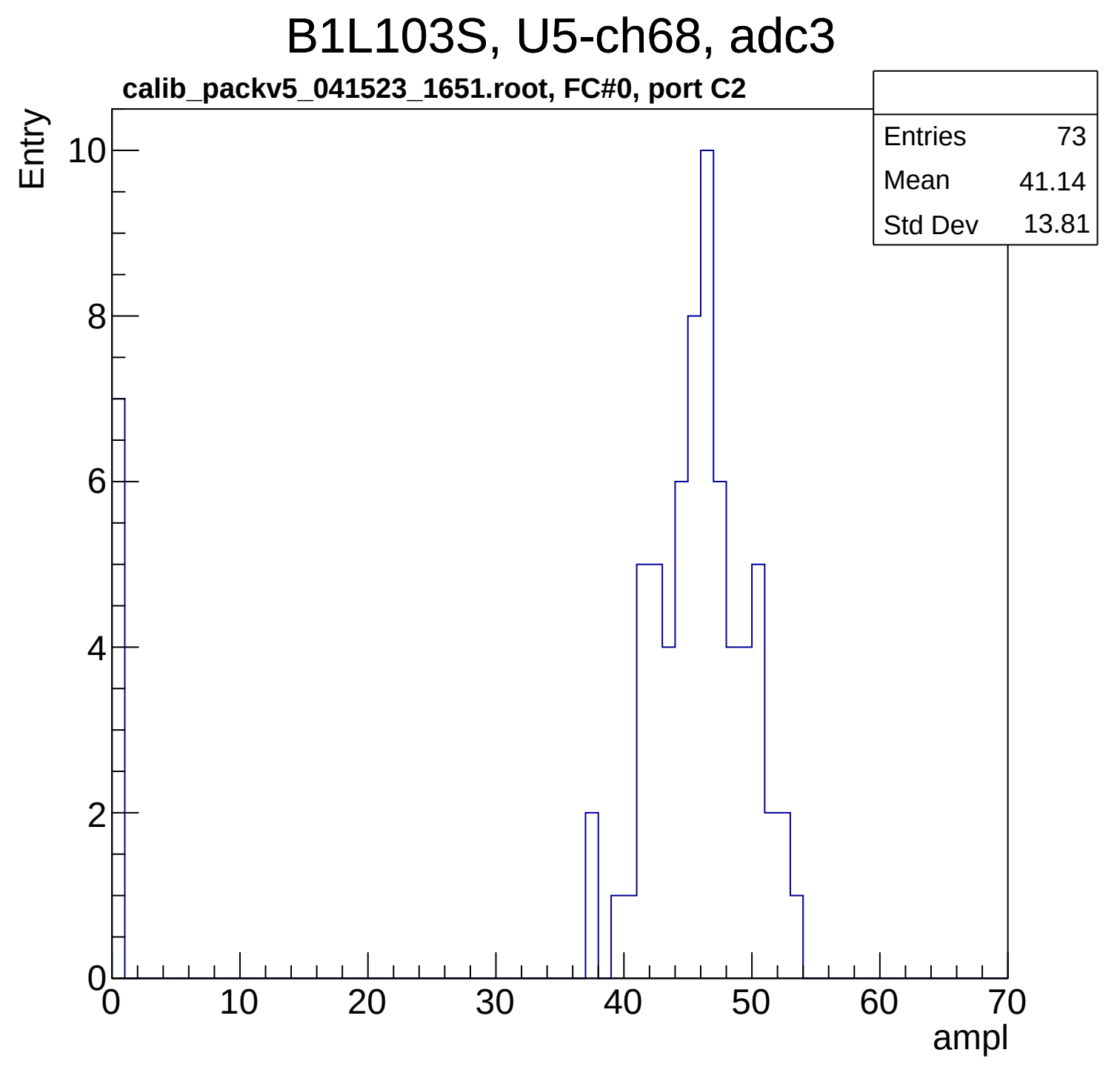
B1L103S, U5-ch68, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 41.14
Std Dev 13.81
Entry
ampl
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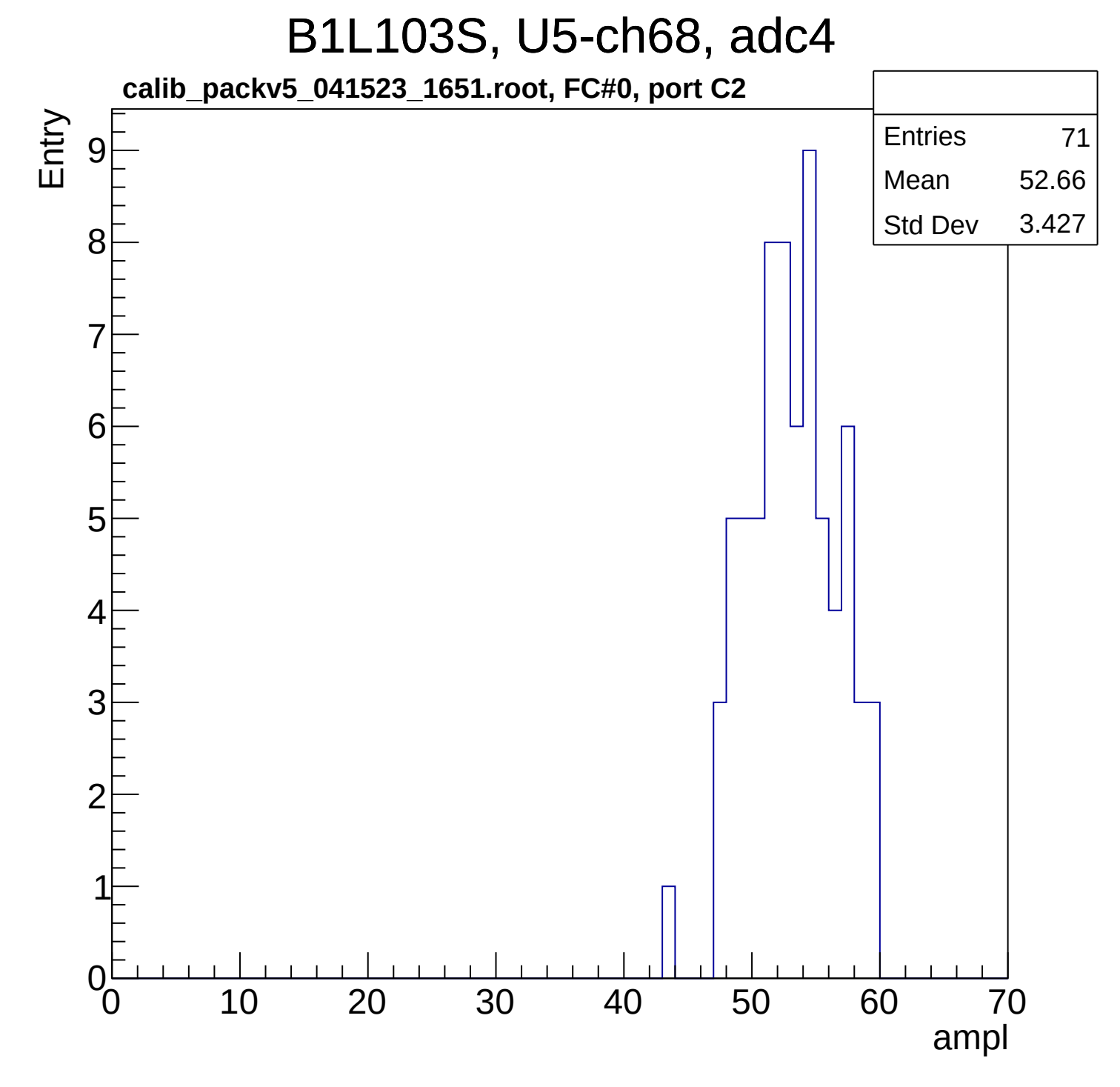
B1L103S, U5-ch68, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 52.66
Std Dev 3.427
Entry
ampl
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6
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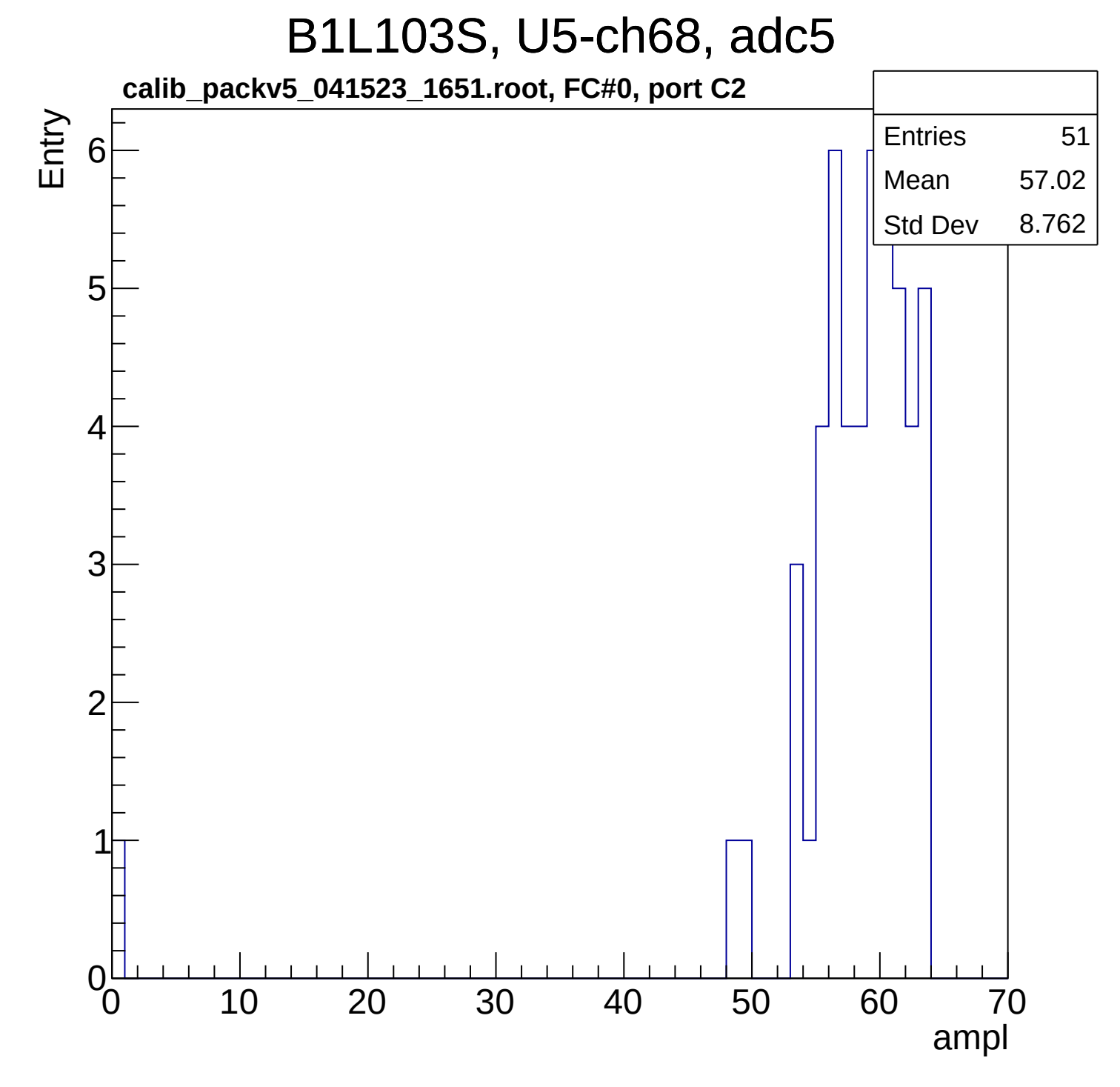
B1L103S, U5-ch68, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 57.02
Std Dev 8.762
Entry
ampl
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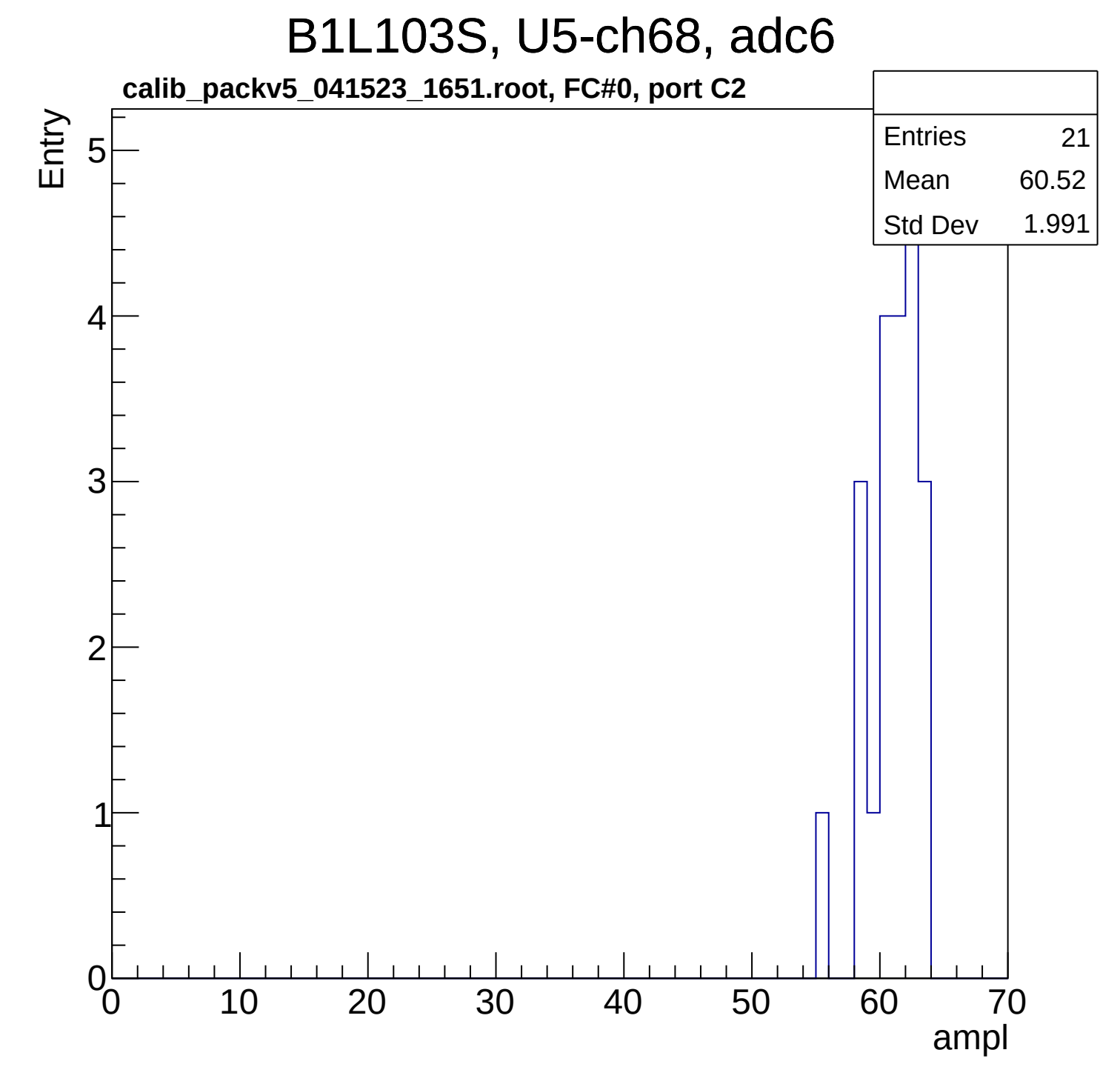
B1L103S, U5-ch68, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 60.52
Std Dev 1.991
Entry
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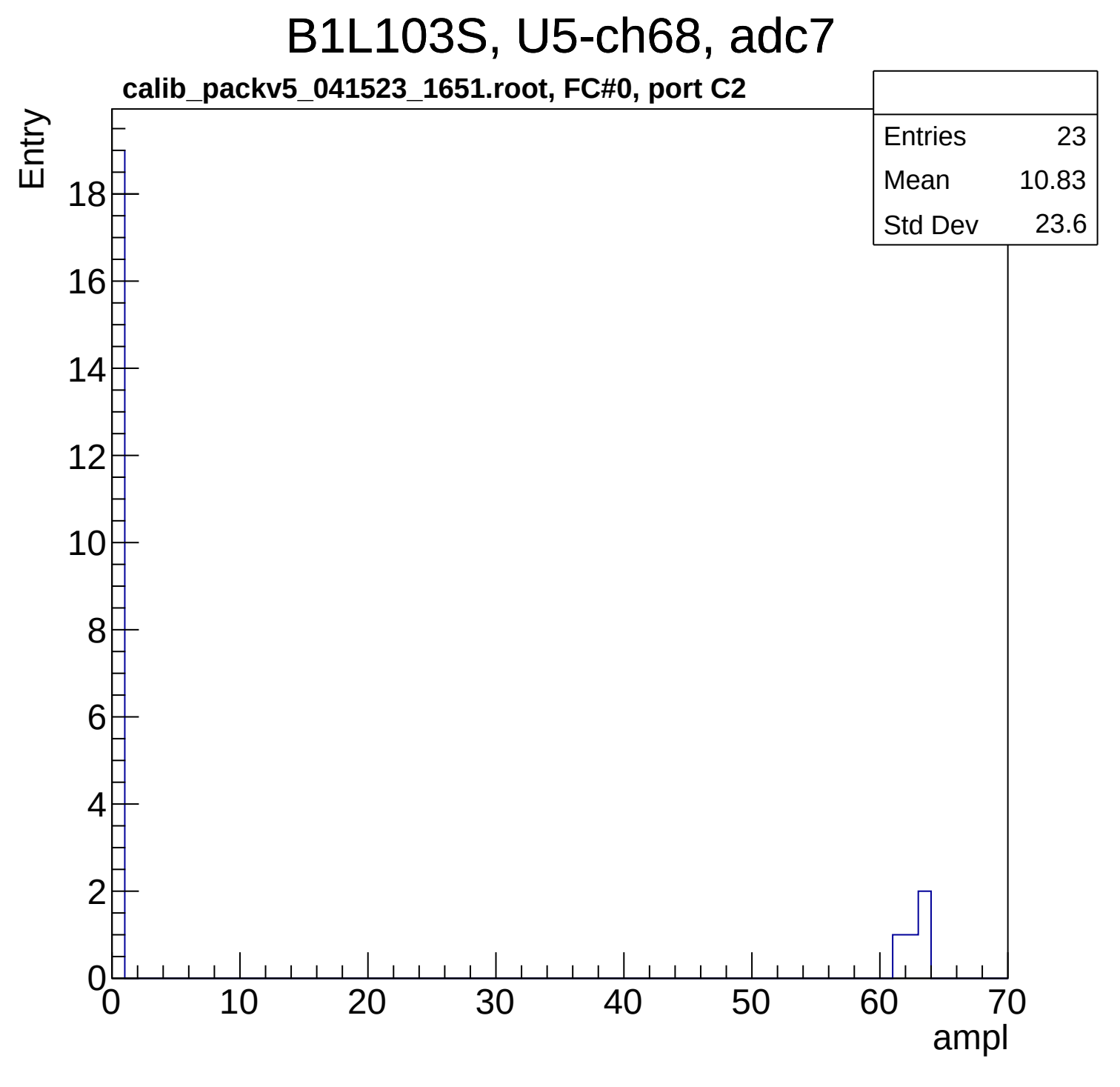
50
60
70
ampl


B1L103S, U5-ch68, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.83
Std Dev 23.6
Entry
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8
10
12
14
16
18
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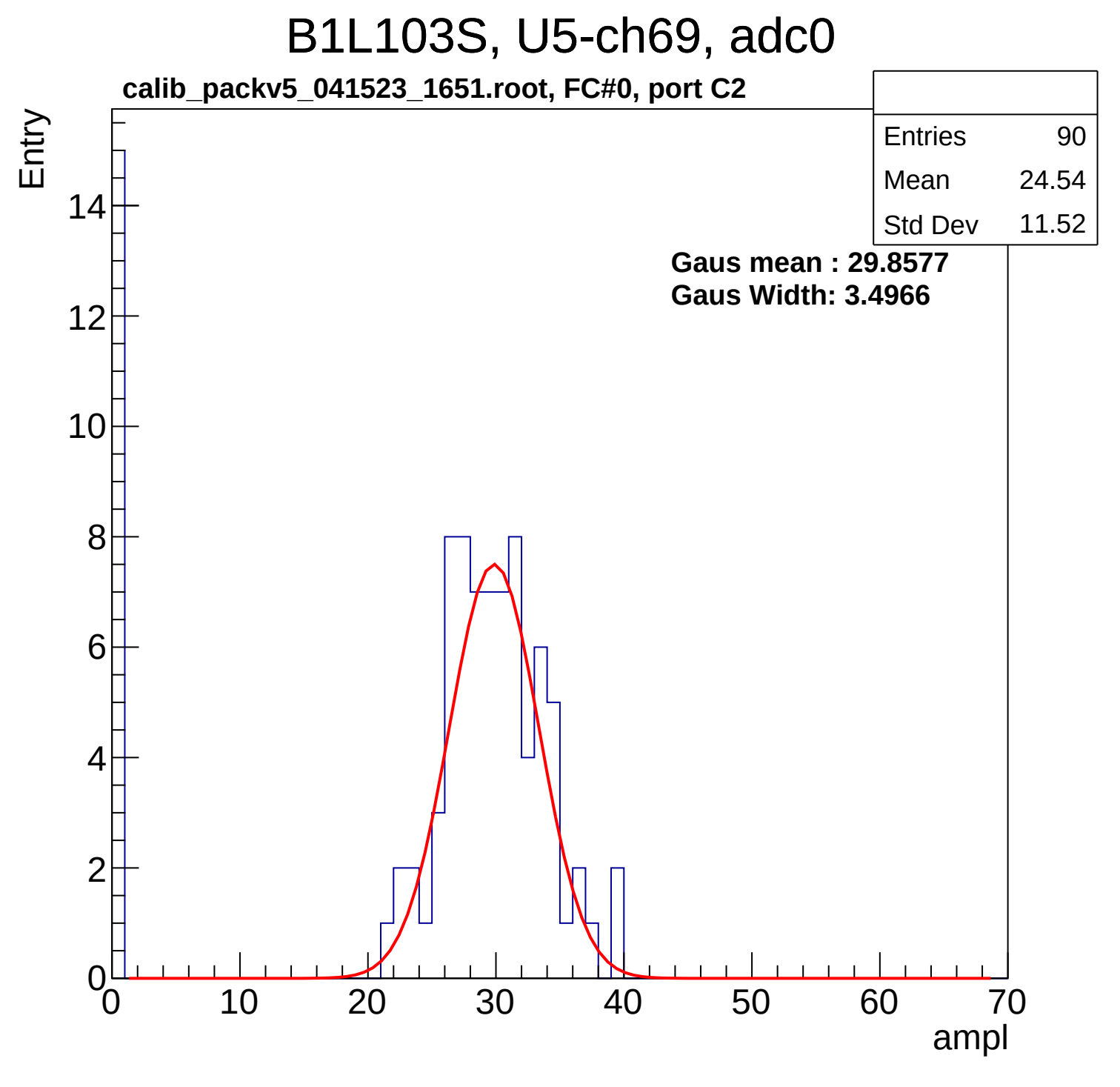
70
ampl


B1L103S, U5-ch69, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 24.54
Std Dev 11.52
Gaus mean : 29.8577
Gaus Width: 3.4966
Entry
ampl
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8
10
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0
10
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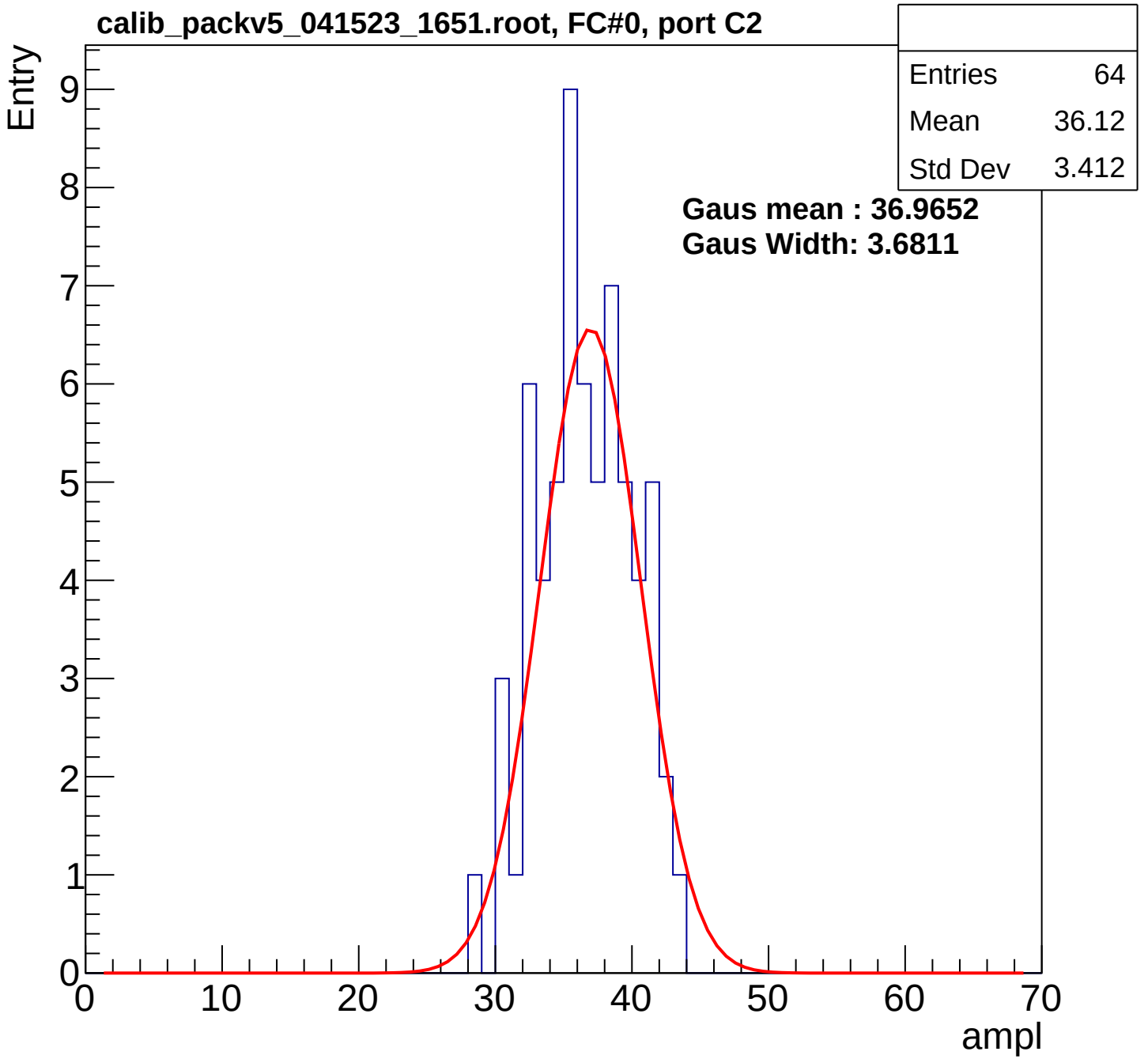
B1L103S, U5-ch69, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 36.12
Std Dev 3.412
Gaus mean : 36.9652
Gaus Width: 3.6811
Entry
ampl
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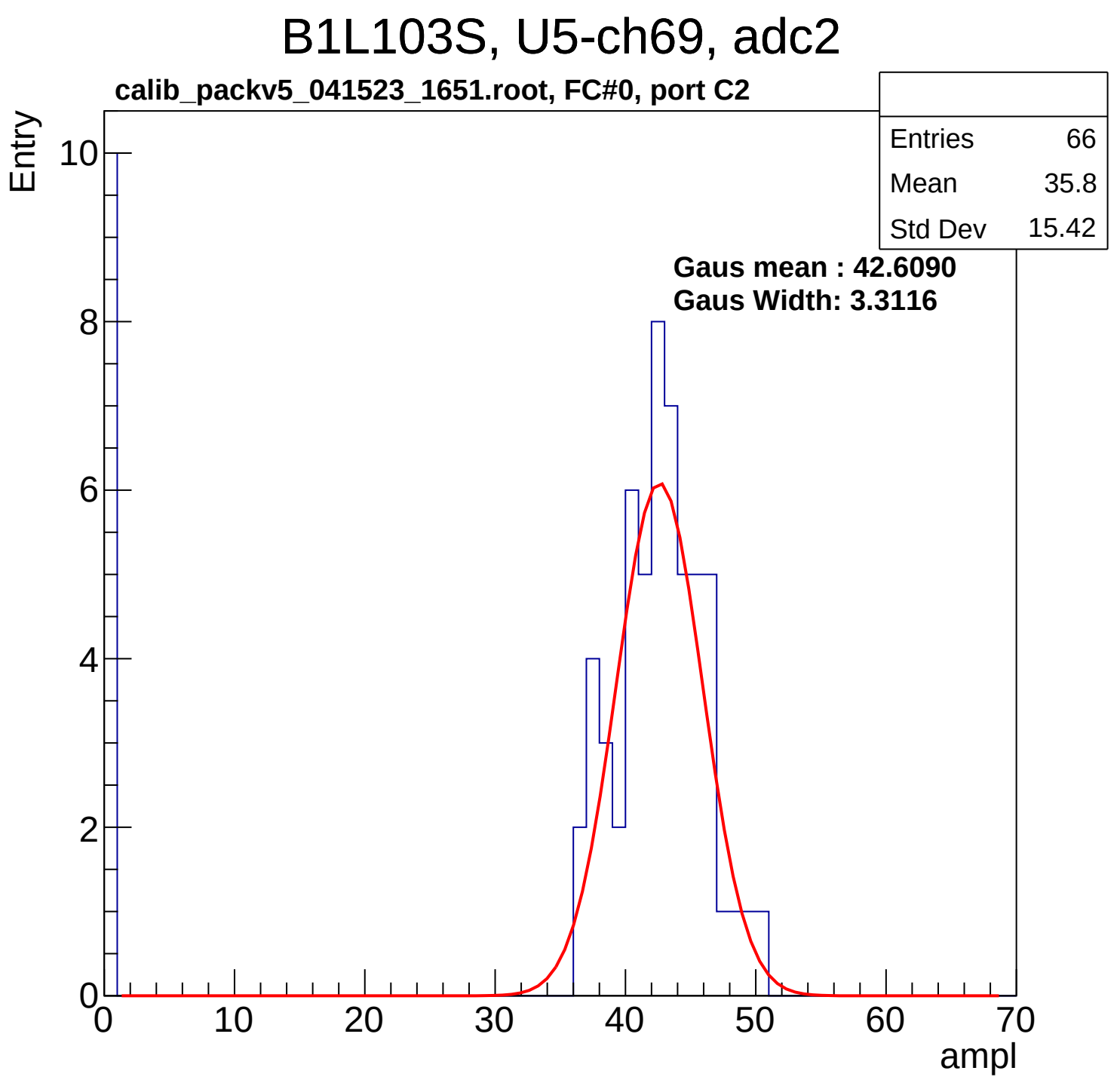
B1L103S, U5-ch69, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 35.8
Std Dev 15.42
Gaus mean : 42.6090
Gaus Width: 3.3116
Entry
ampl
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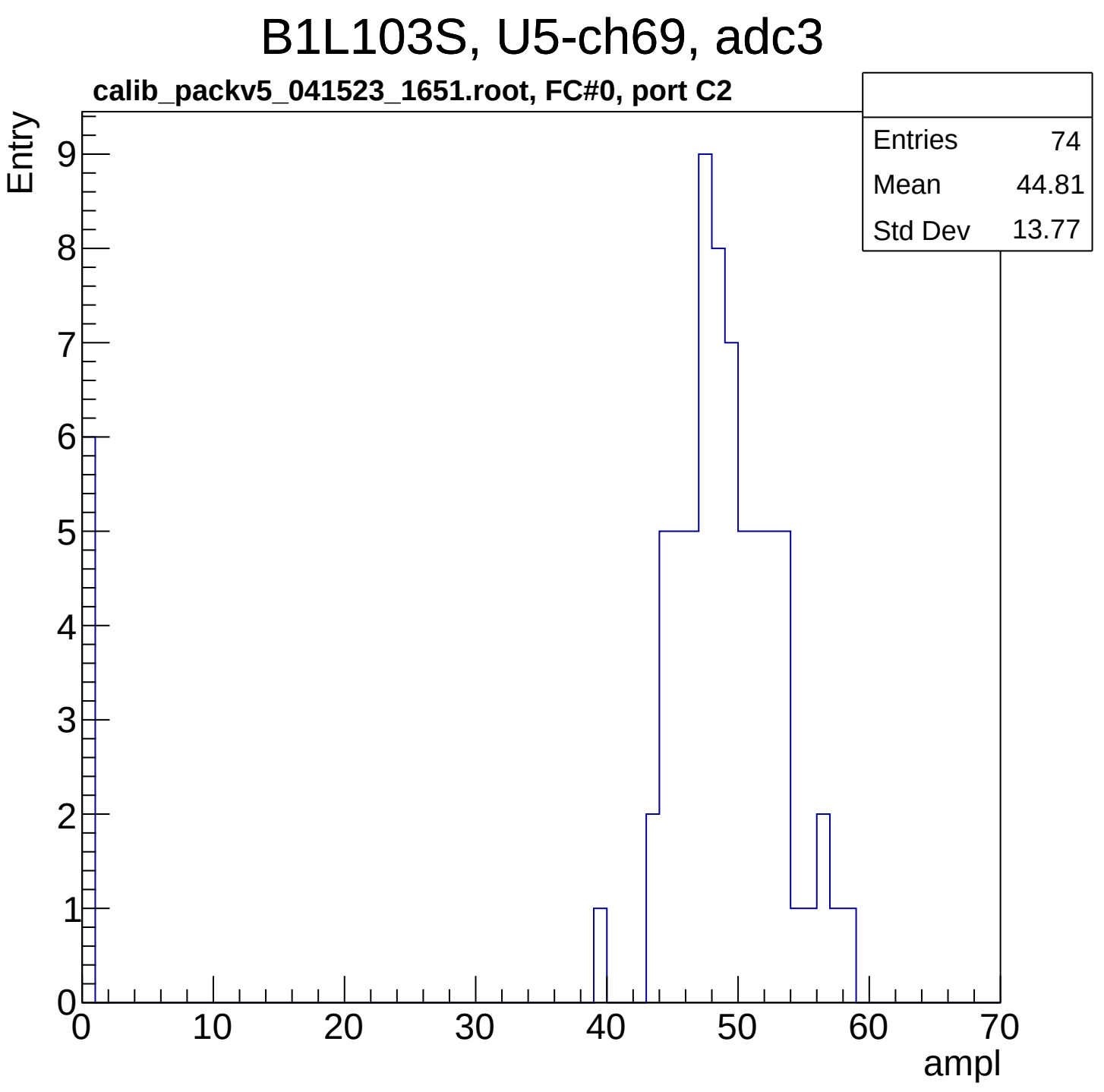
B1L103S, U5-ch69, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 44.81
Std Dev 13.77
Entry
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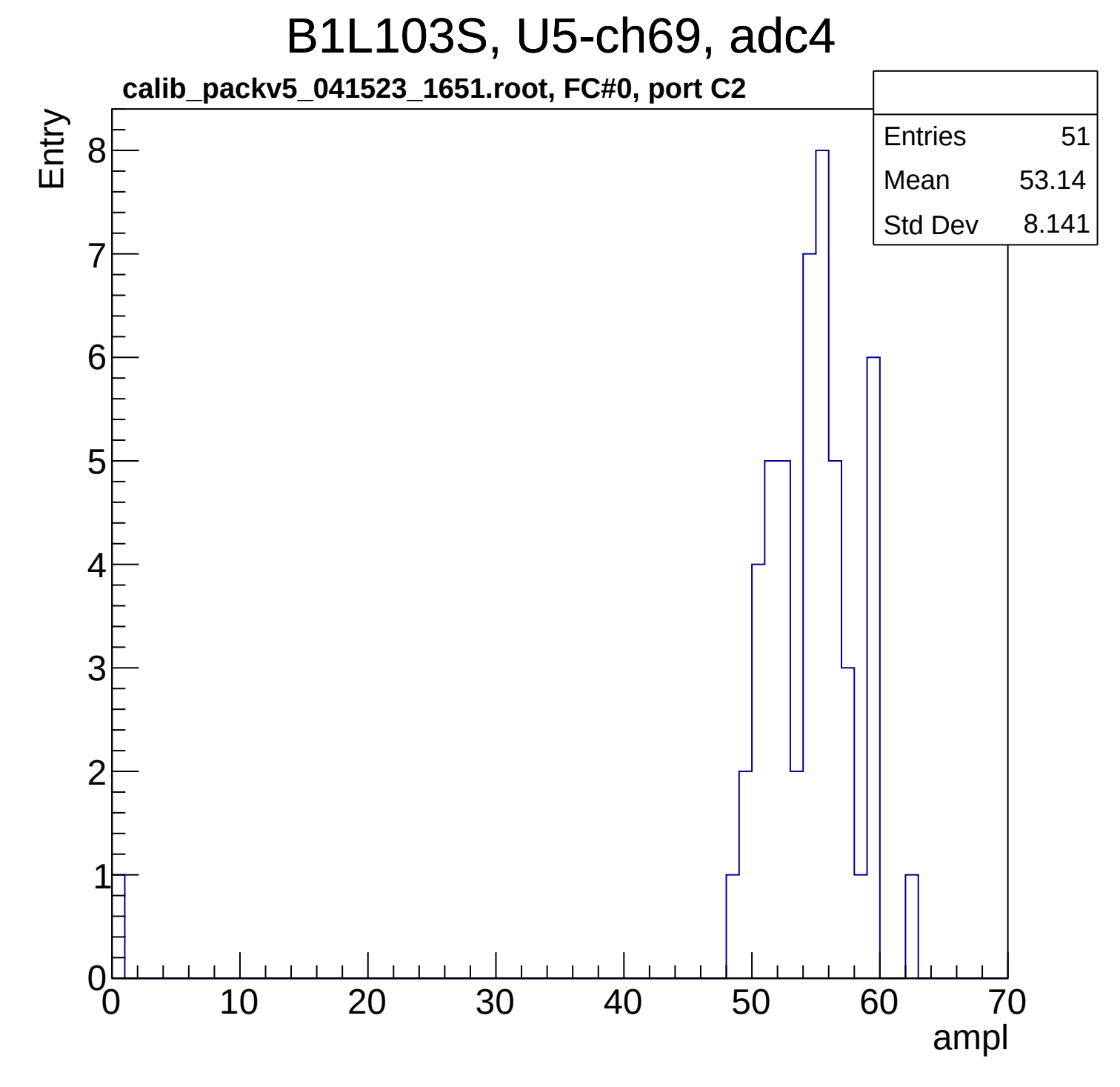
B1L103S, U5-ch69, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 53.14
Std Dev 8.141
Entry
ampl
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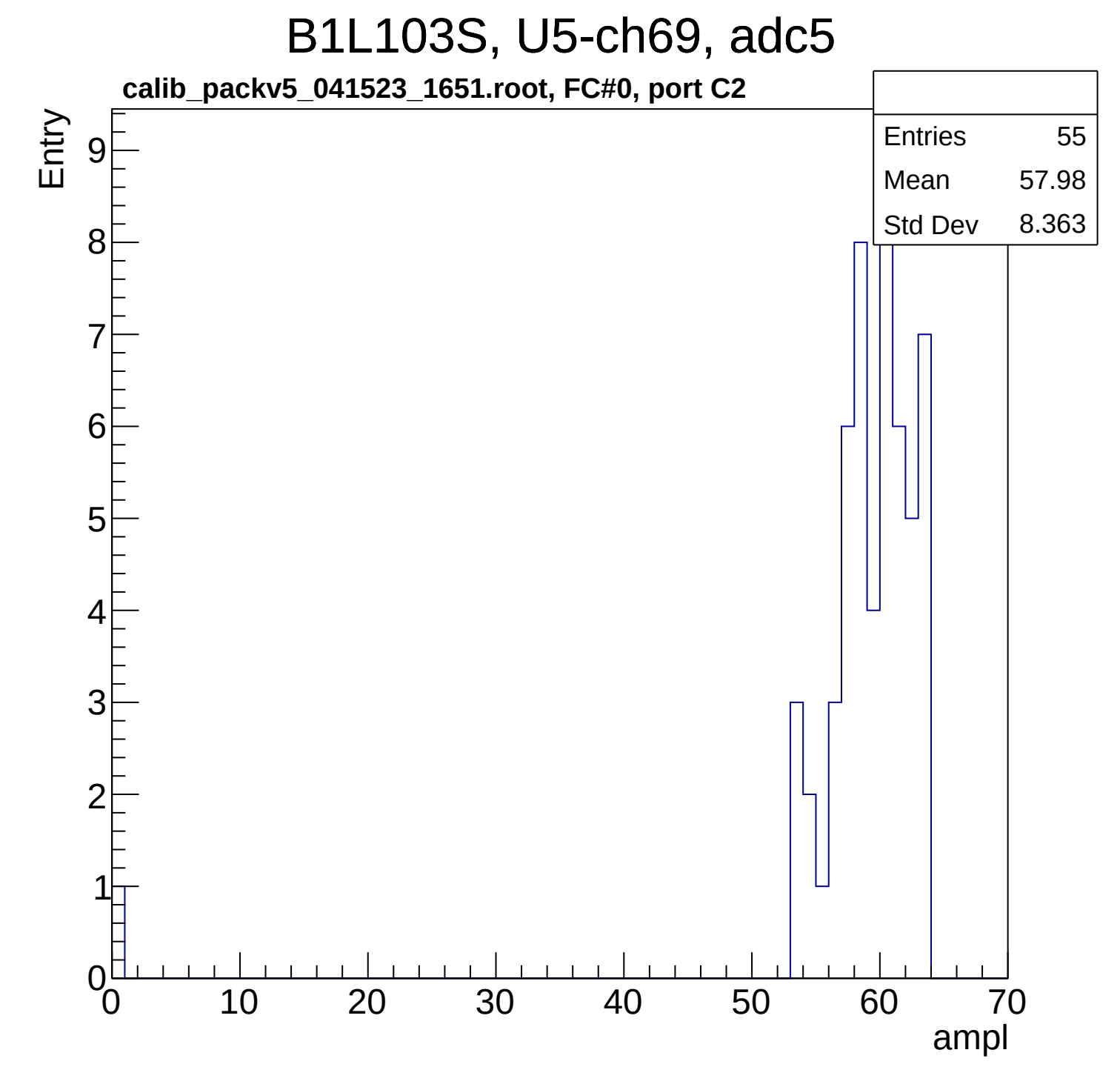
B1L103S, U5-ch69, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.98
Std Dev 8.363
Entry
ampl
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3
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60
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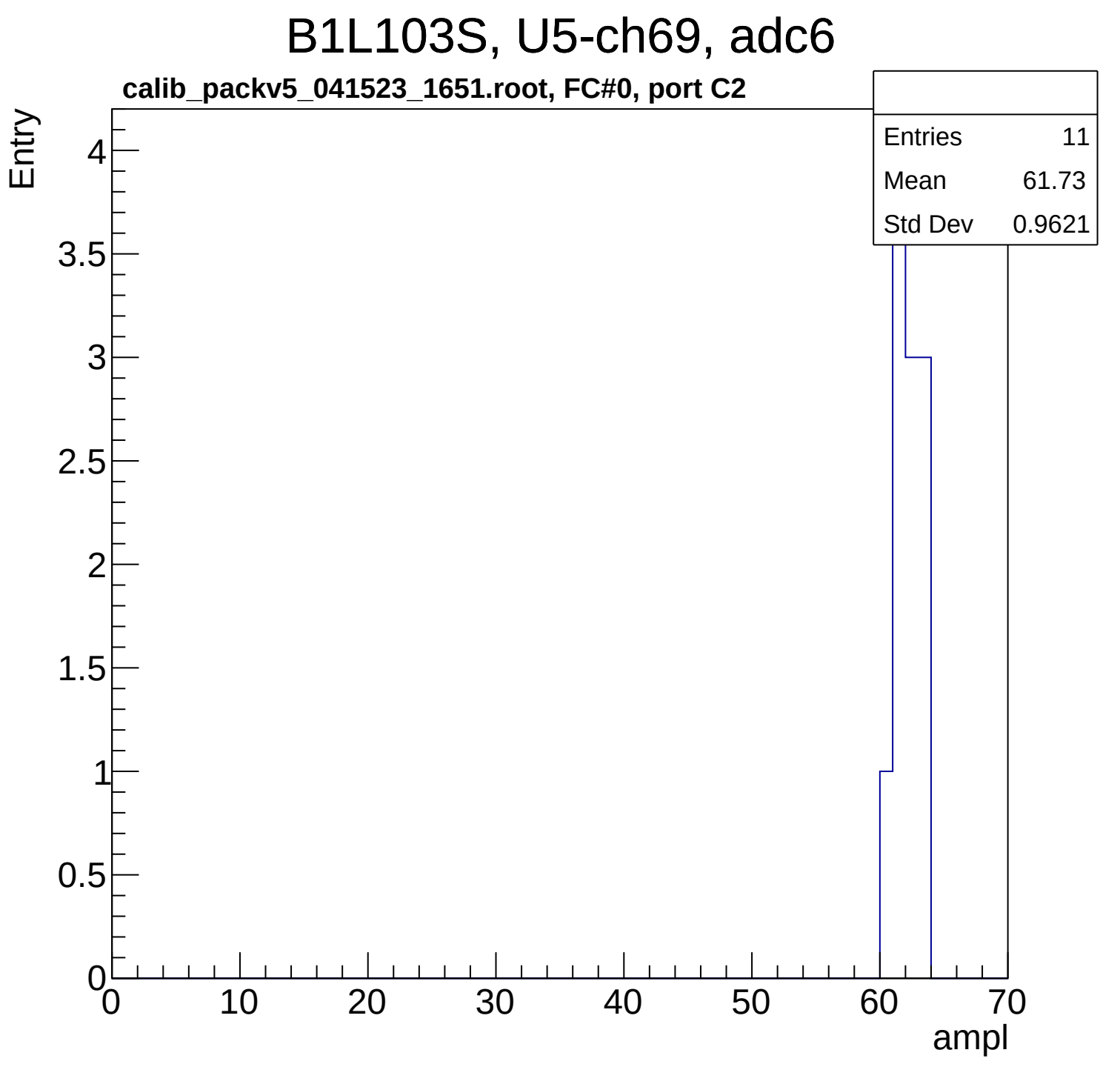
B1L103S, U5-ch69, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.73
Std Dev 0.9621
Entry
ampl
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0.5
1
1.5
2
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3
3.5
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0
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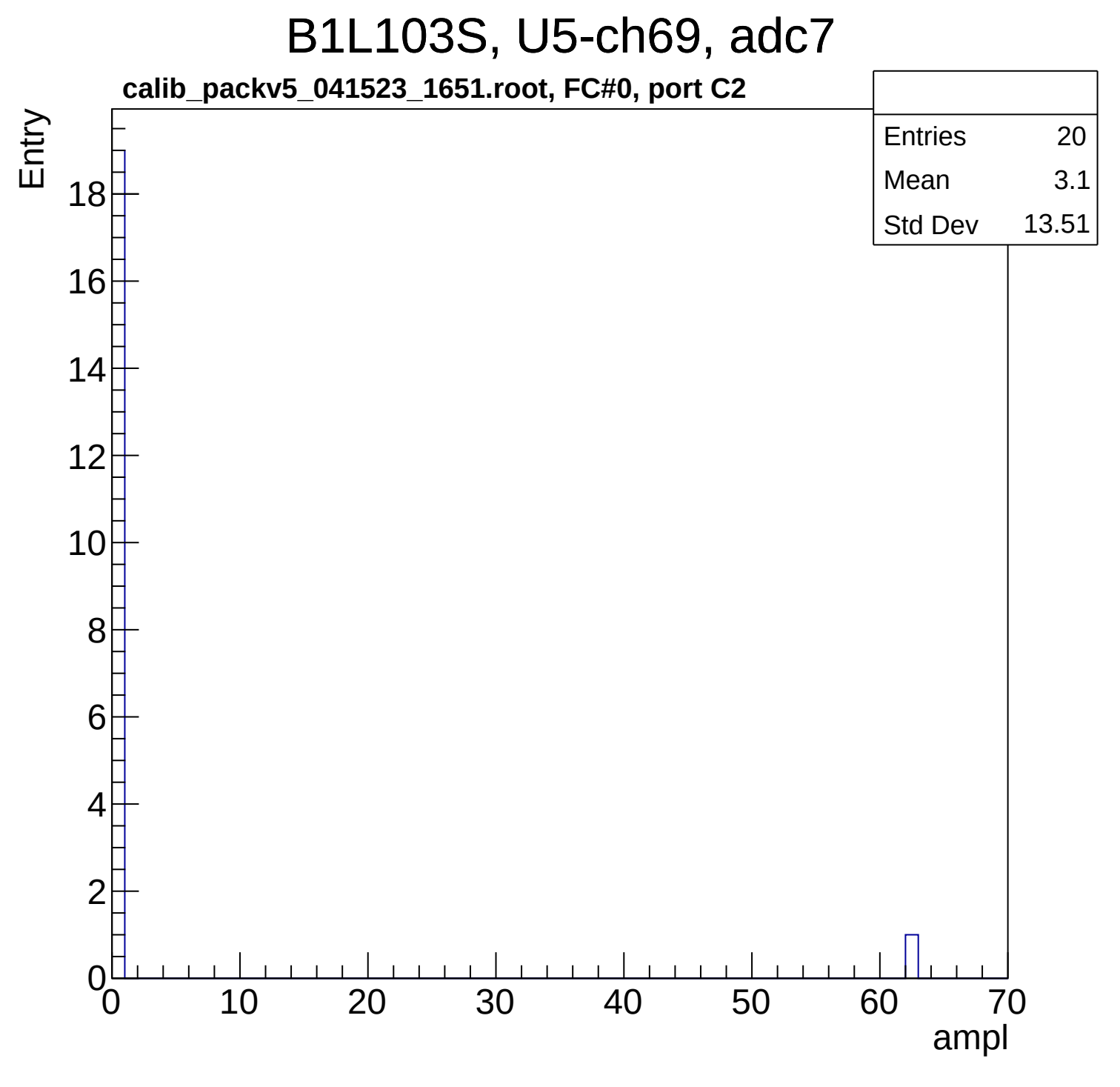
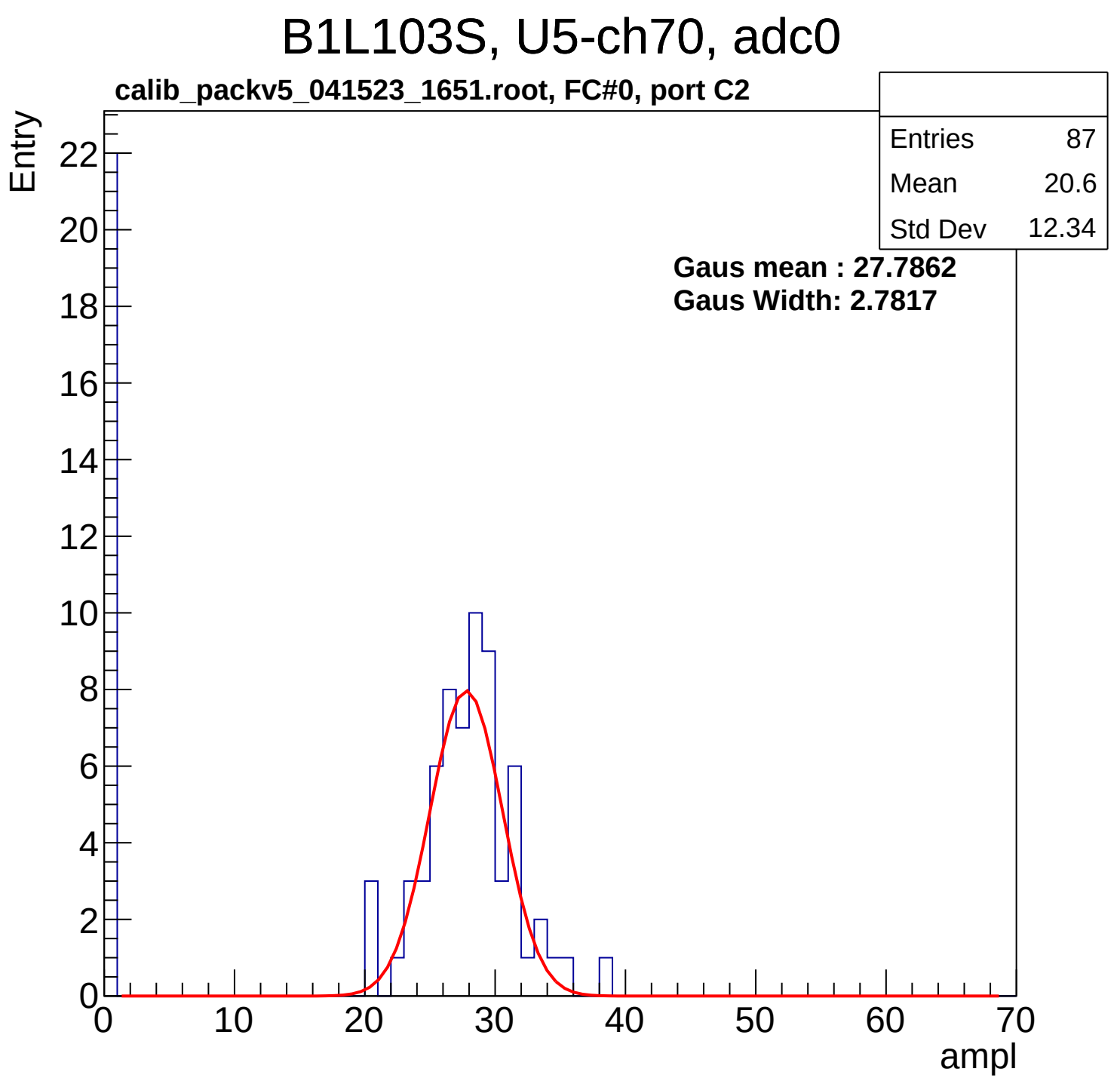

B1L103S, U5-ch69, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch70, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 20.6
Std Dev 12.34
Gaus mean : 27.7862
Gaus Width: 2.7817
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
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20
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40
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60
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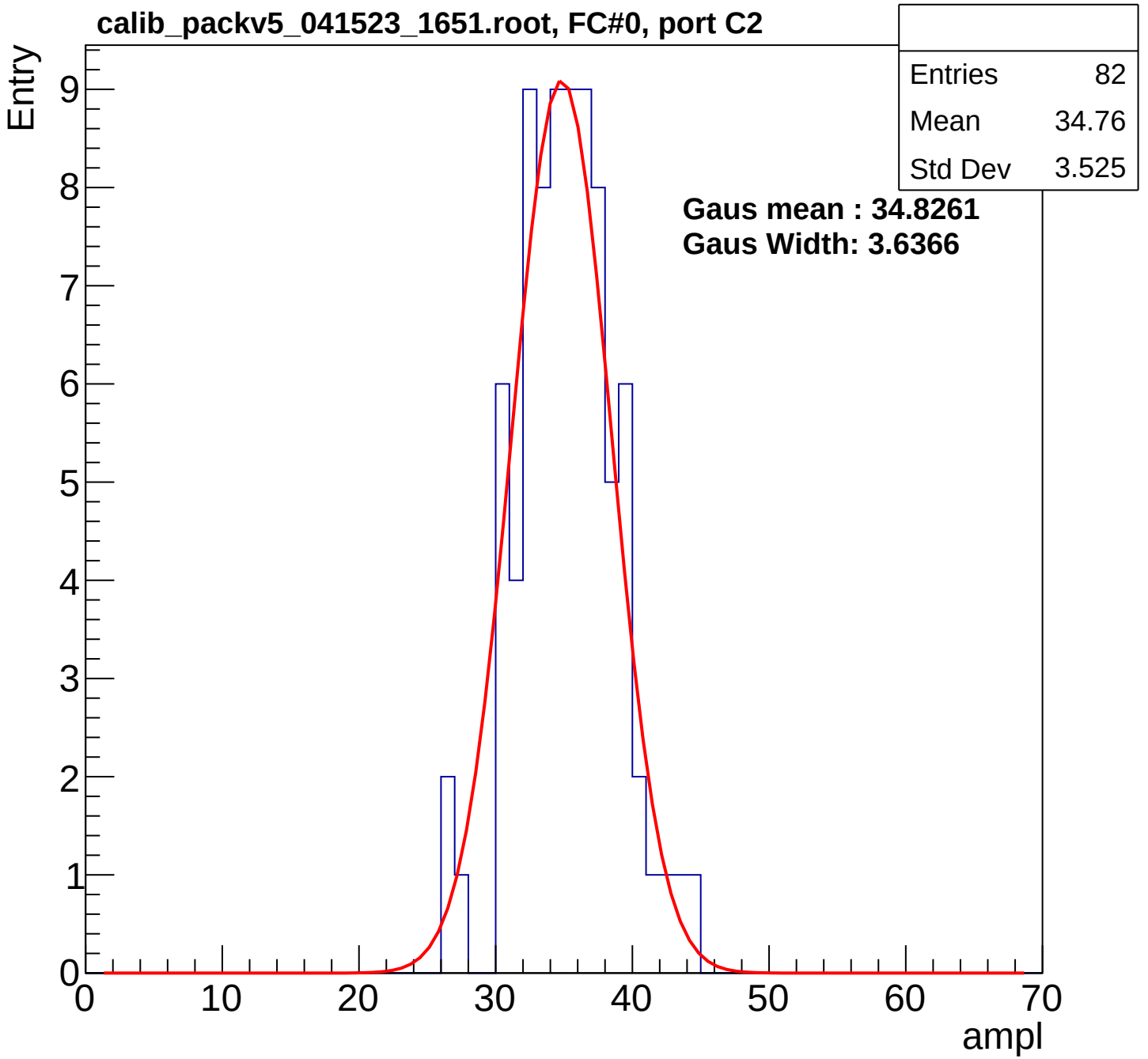
B1L103S, U5-ch70, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 34.76
Std Dev 3.525
Gaus mean : 34.8261
Gaus Width: 3.6366
Entry
ampl
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2
3
4
5
6
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0
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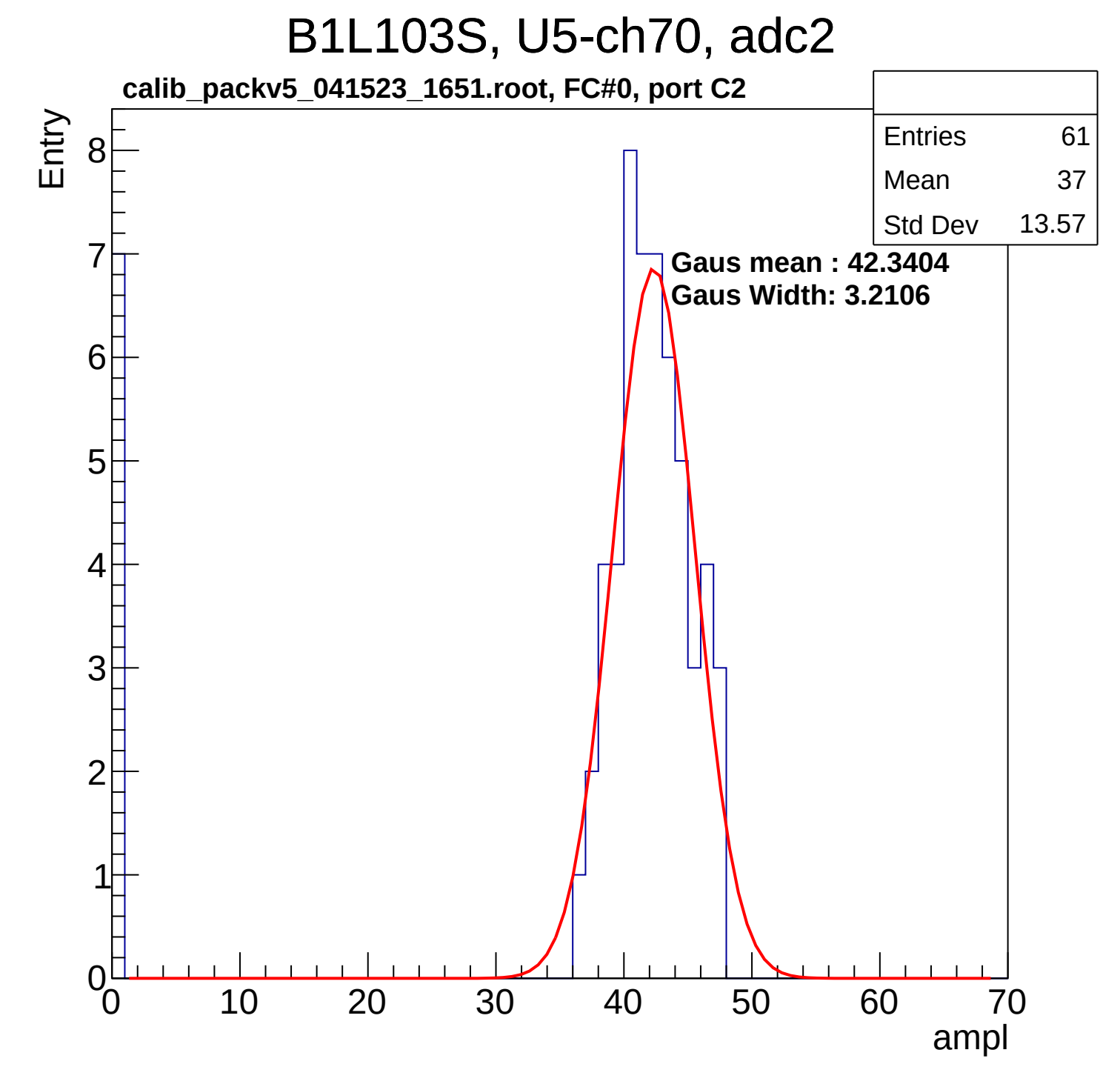
B1L103S, U5-ch70, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 37
Std Dev 13.57
Gaus mean : 42.3404
Gaus Width: 3.2106
Entry
ampl
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1
2
3
4
5
6
7
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0
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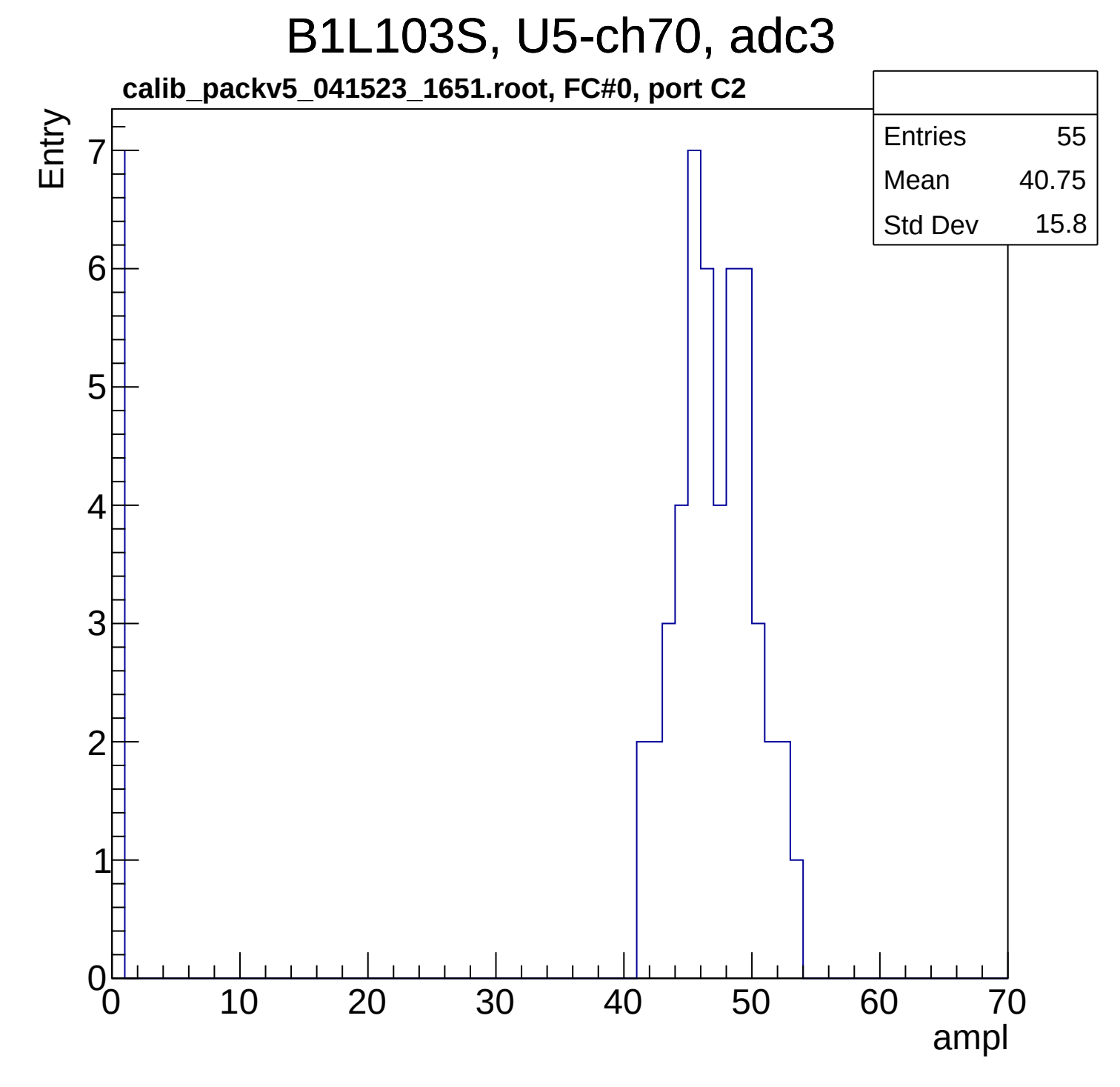
B1L103S, U5-ch70, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 40.75
Std Dev 15.8
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
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60
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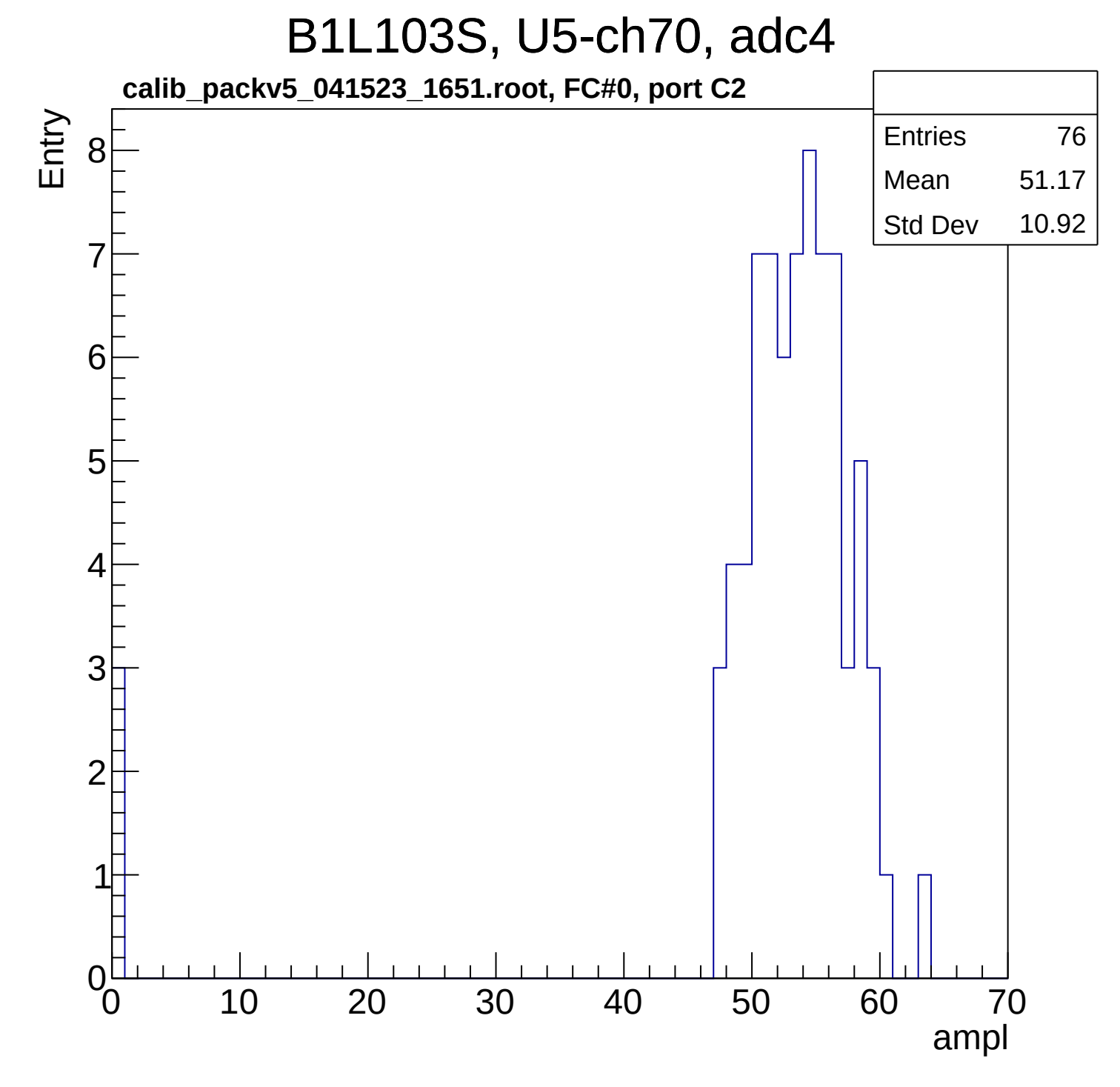
B1L103S, U5-ch70, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 51.17
Std Dev 10.92
Entry
ampl
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1
2
3
4
5
6
7
8
0
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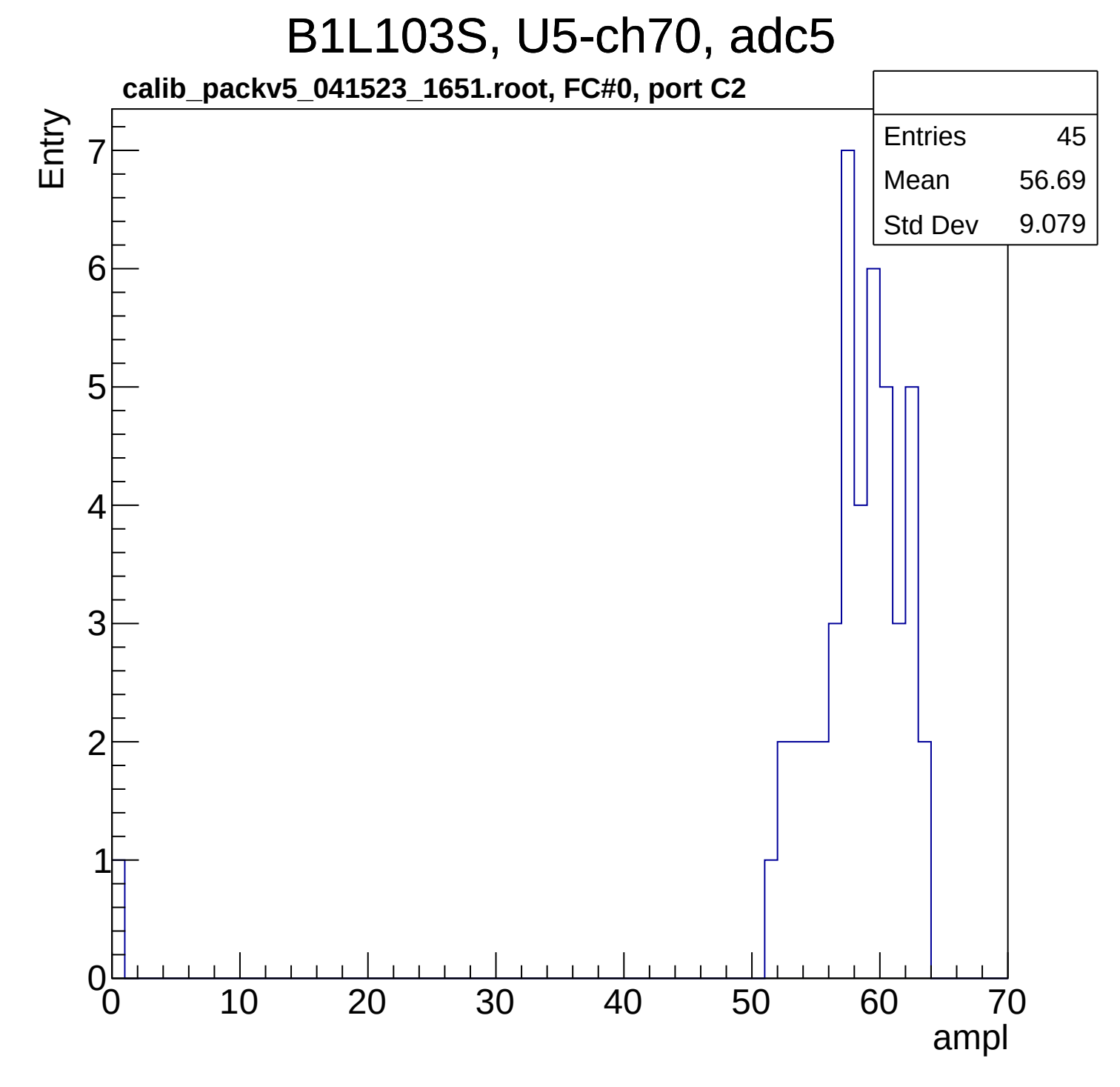
B1L103S, U5-ch70, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 56.69
Std Dev 9.079
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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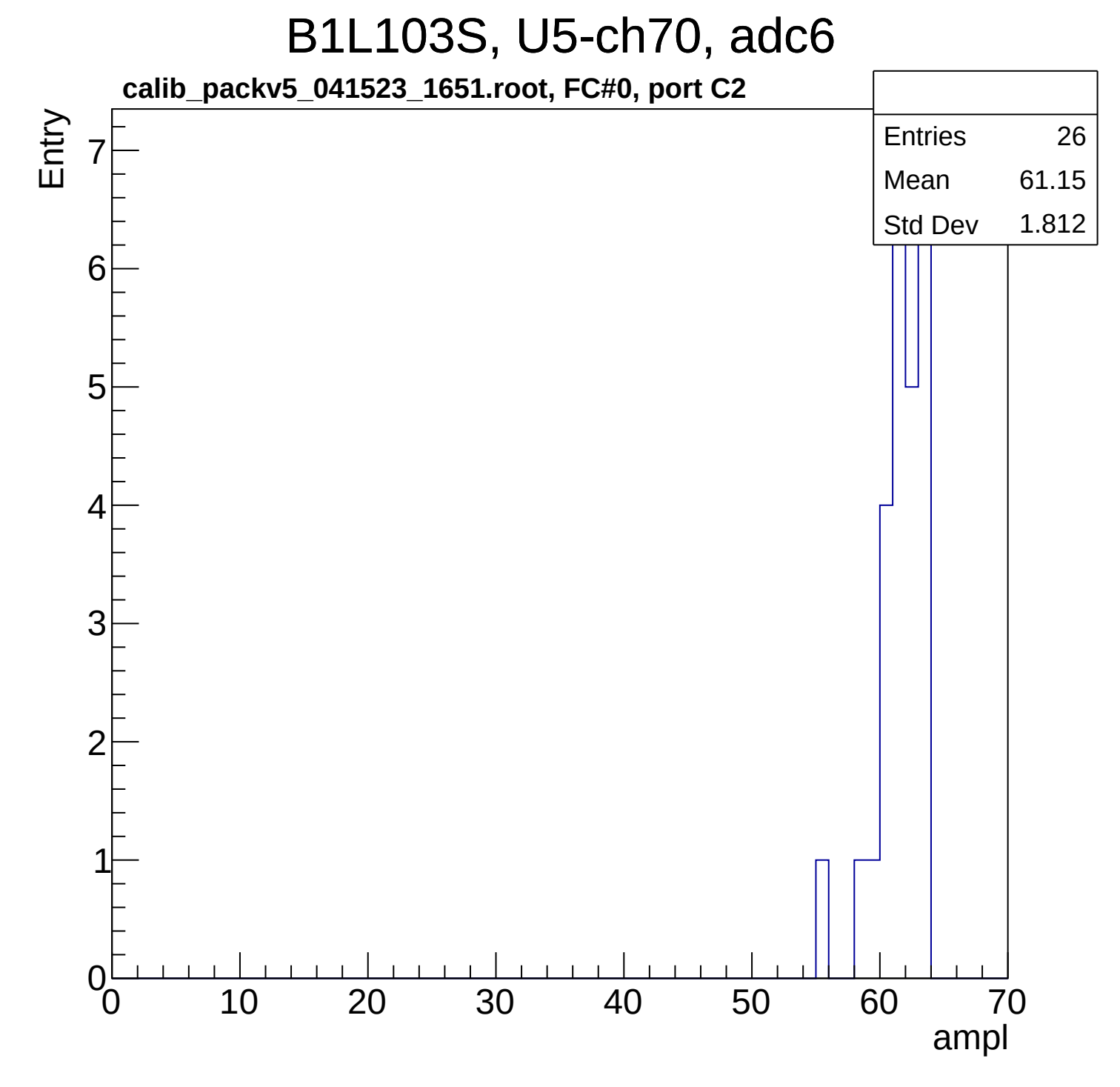
B1L103S, U5-ch70, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 61.15
Std Dev 1.812
Entry
ampl
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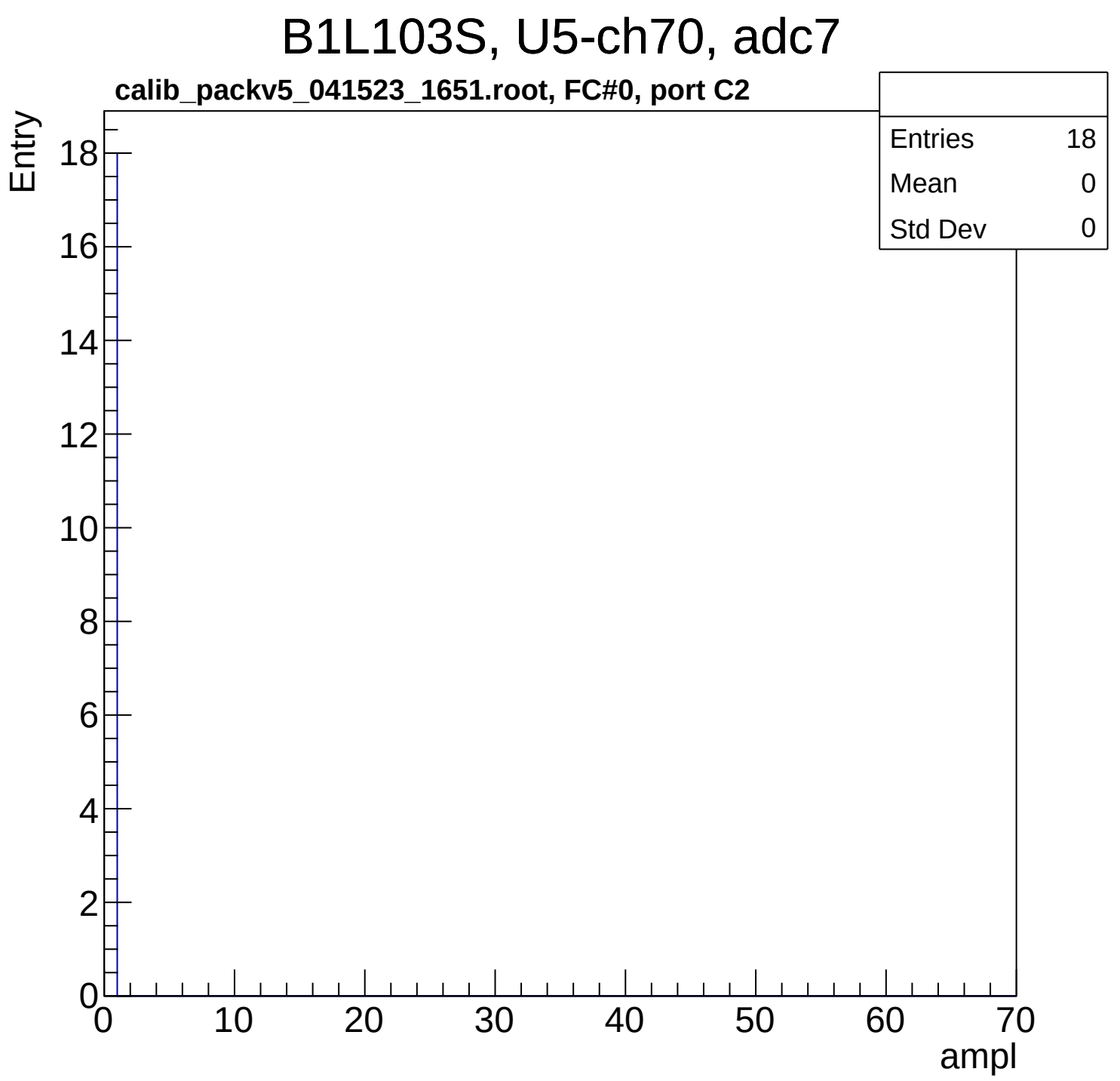
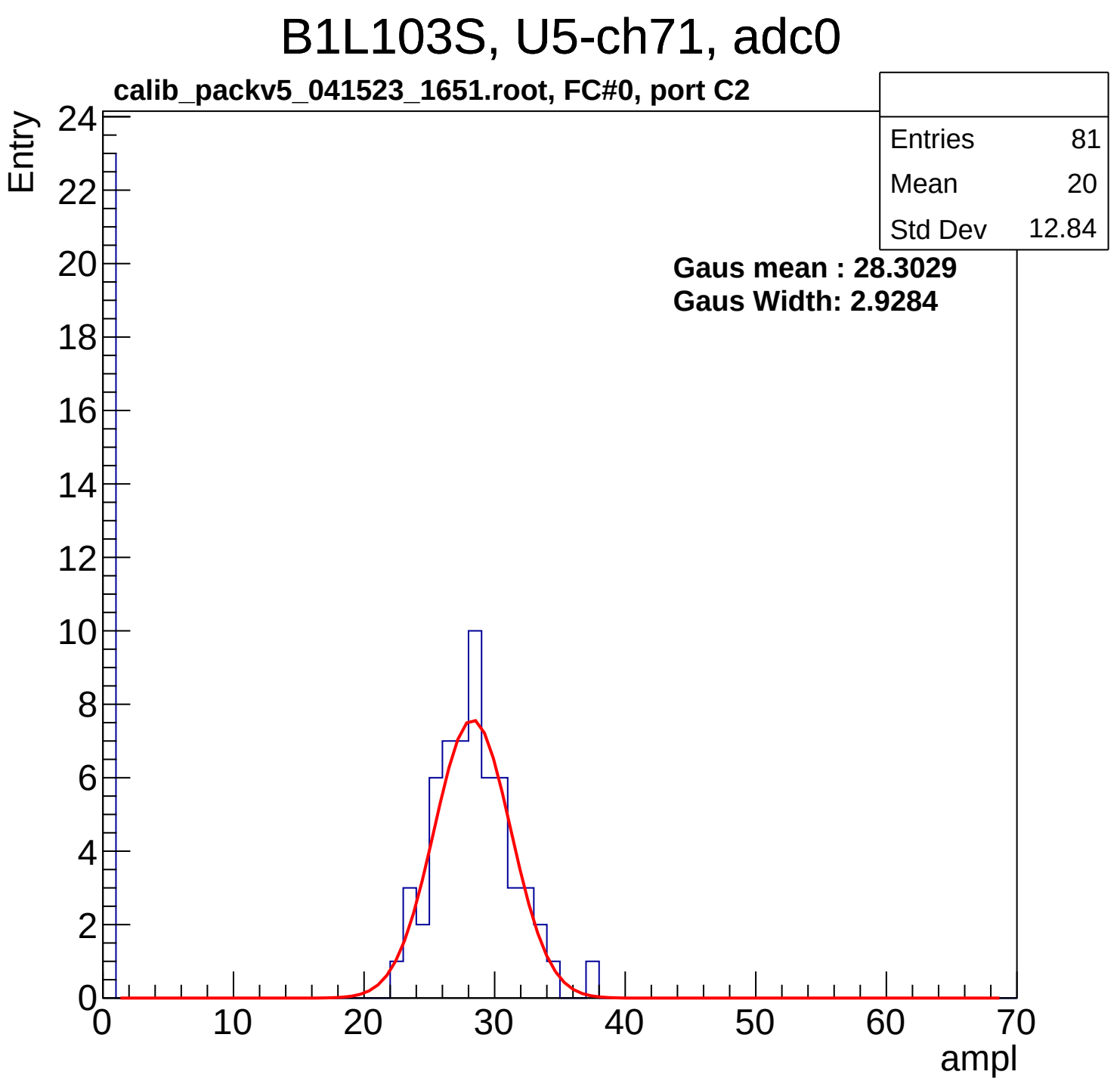
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U5-ch70, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch71, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 20
Std Dev 12.84
Gaus mean : 28.3029
Gaus Width: 2.9284
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
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20
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40
50
60
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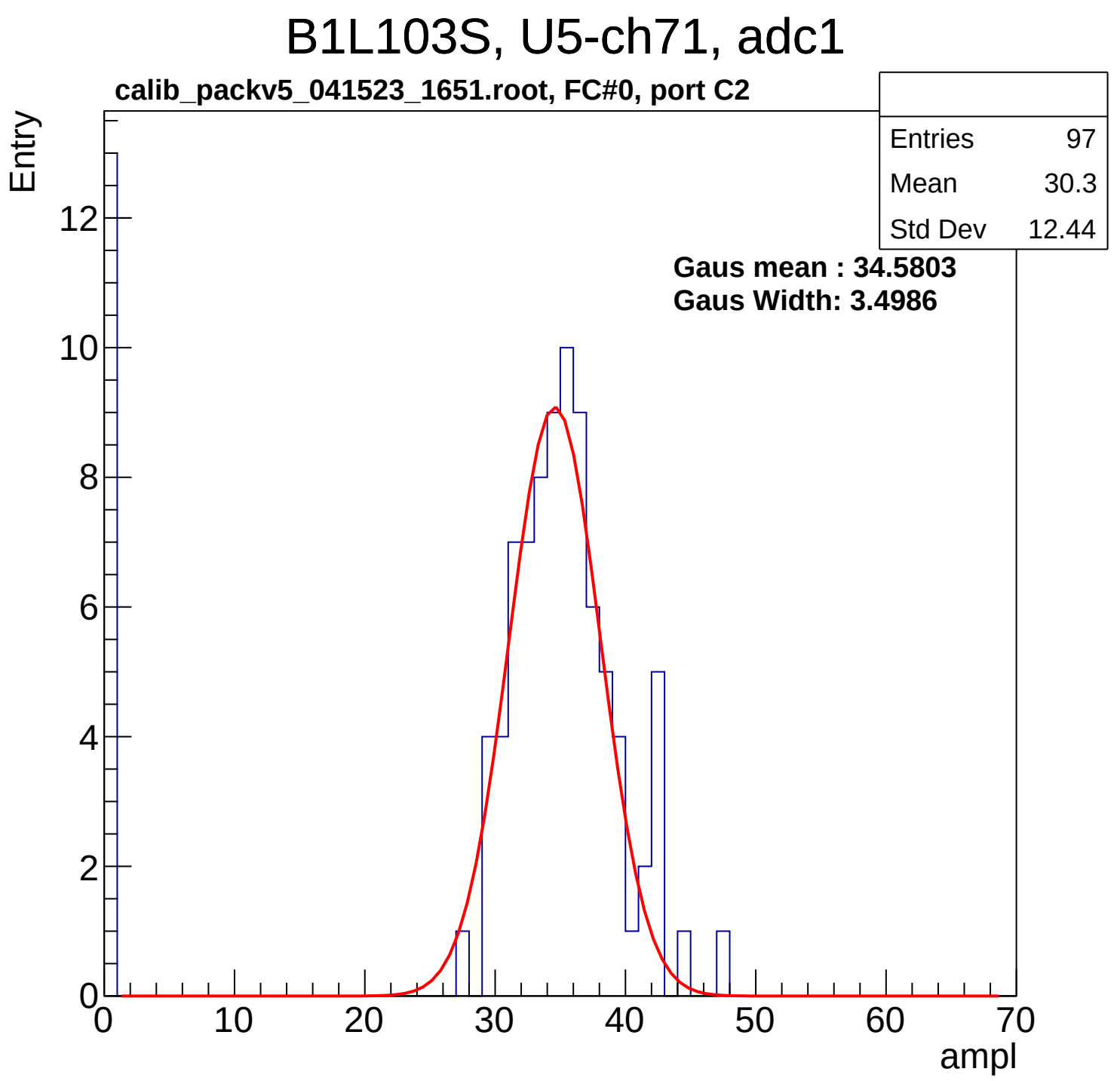
B1L103S, U5-ch71, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 30.3
Std Dev 12.44
Gaus mean : 34.5803
Gaus Width: 3.4986
Entry
ampl
0
2
4
6
8
10
12
0
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20
30
40
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60
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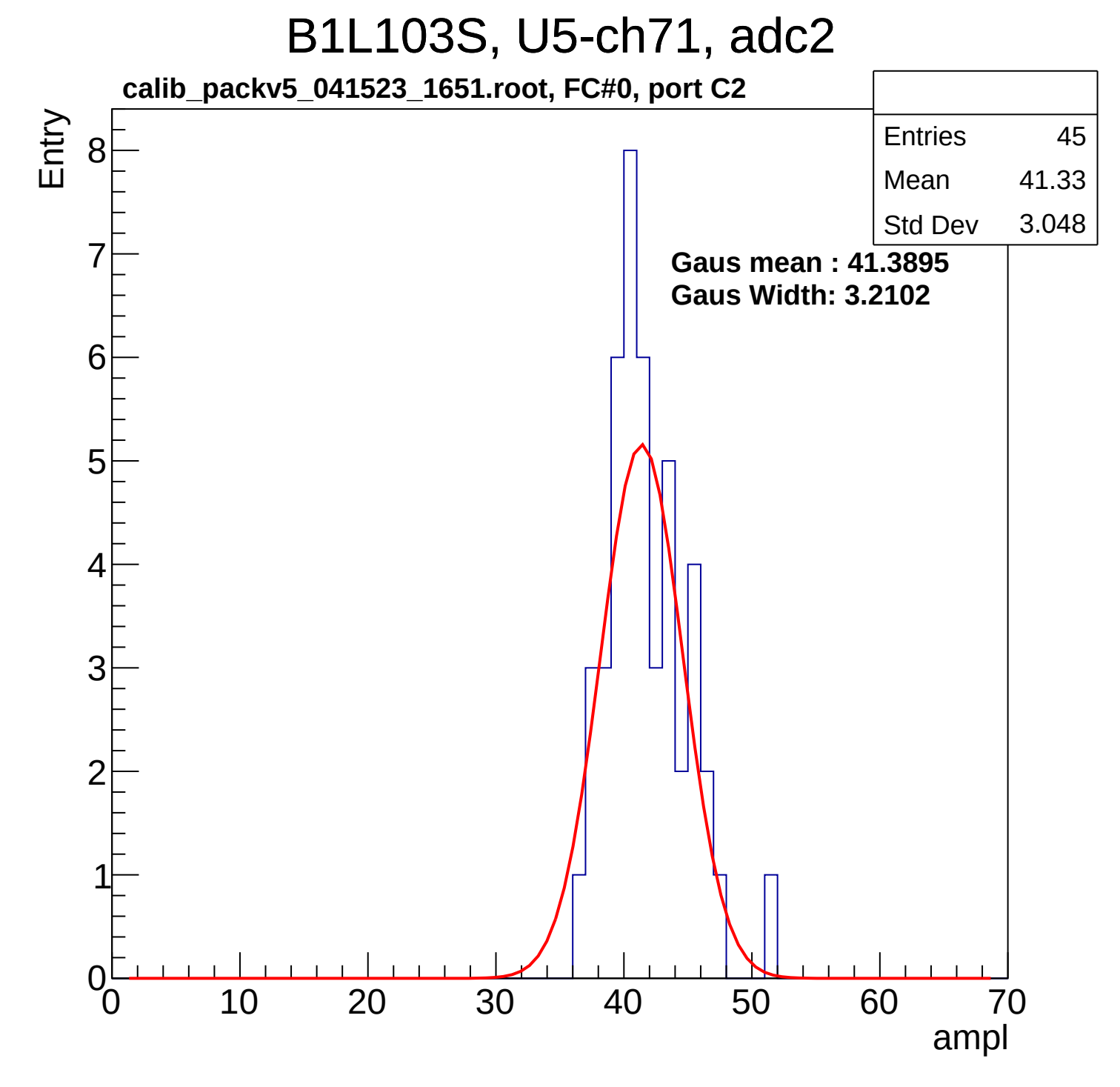
B1L103S, U5-ch71, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 41.33
Std Dev 3.048
Gaus mean : 41.3895
Gaus Width: 3.2102
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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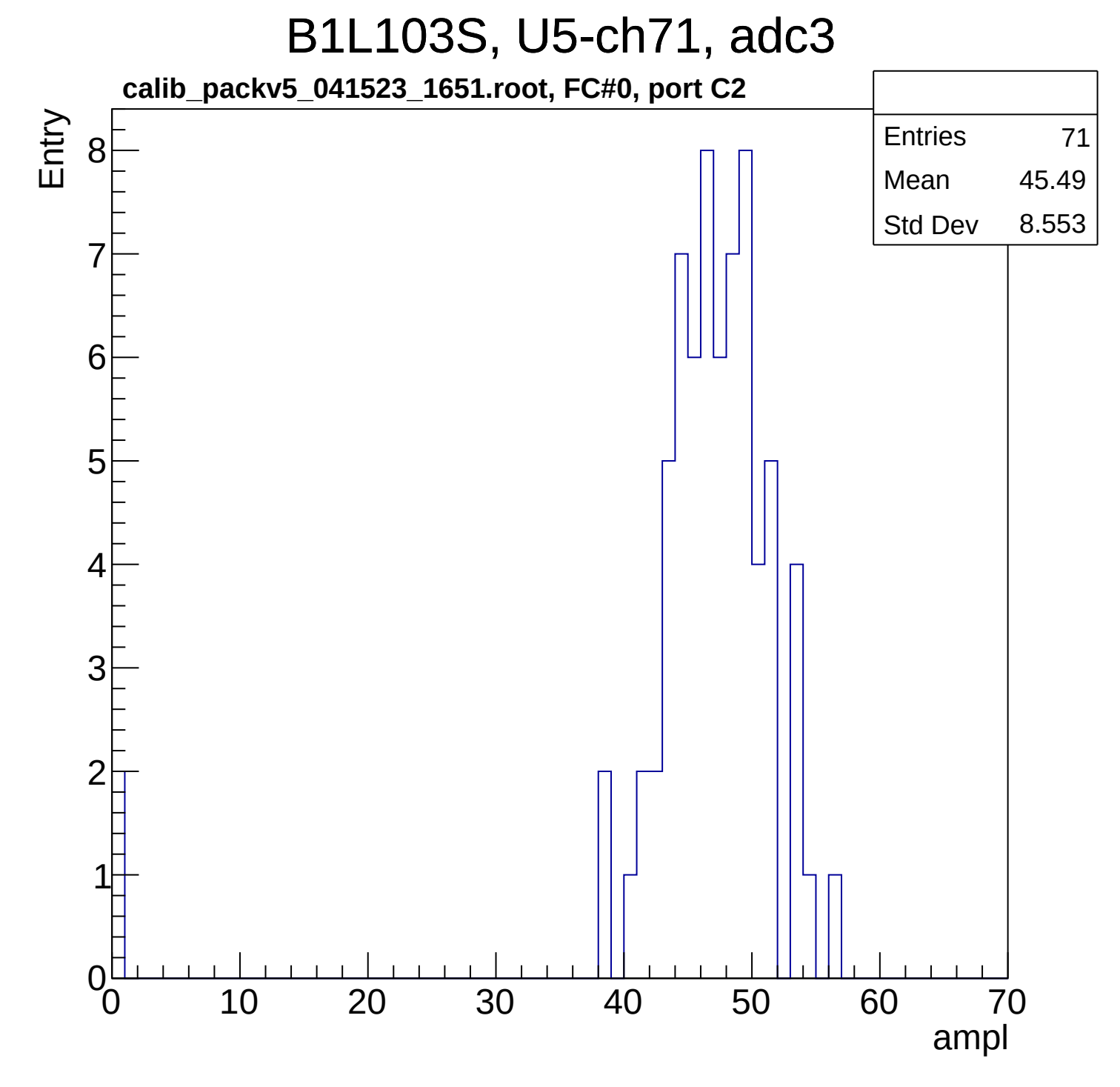
B1L103S, U5-ch71, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 45.49
Std Dev 8.553
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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60
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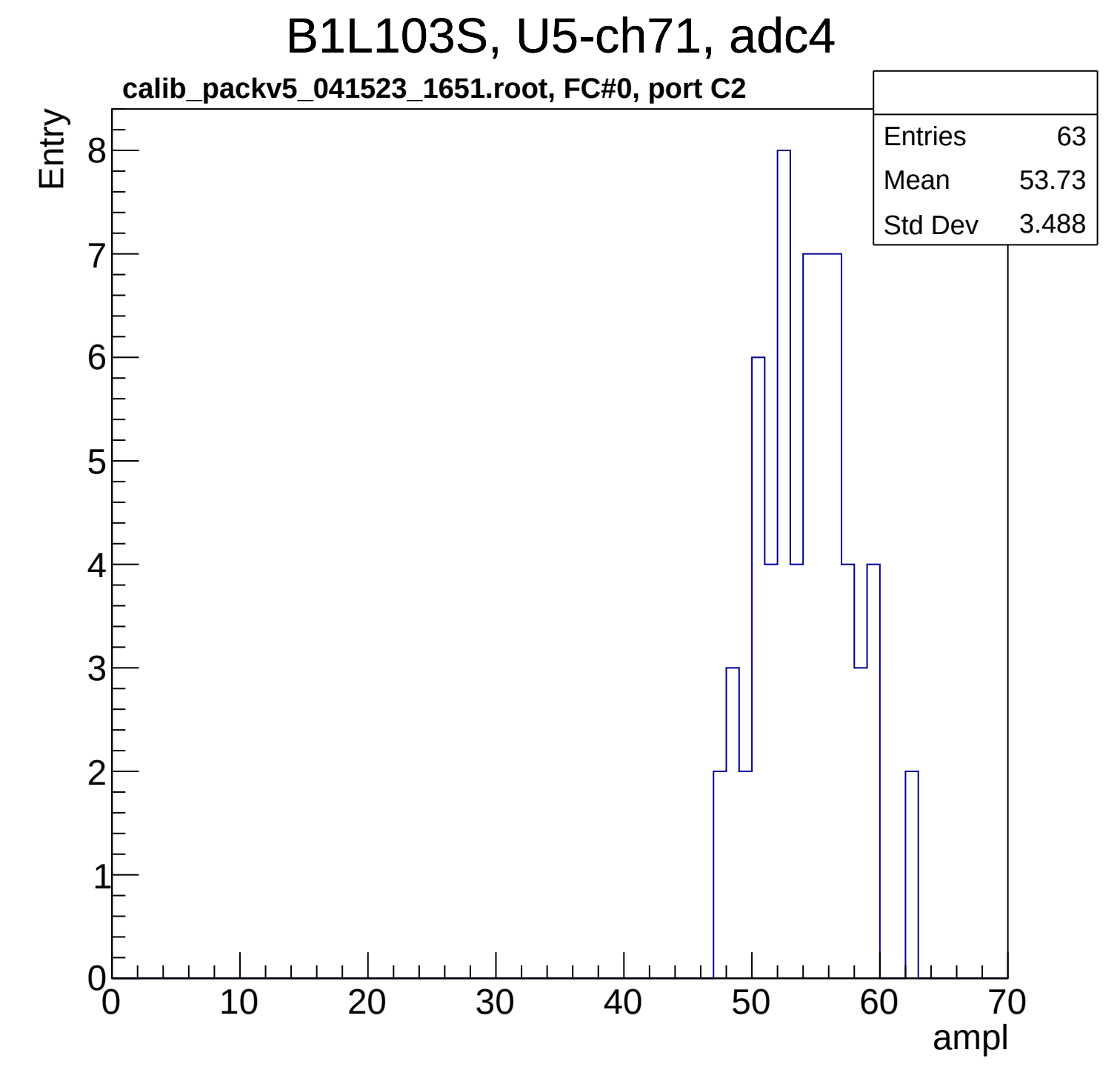
B1L103S, U5-ch71, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 53.73
Std Dev 3.488
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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60
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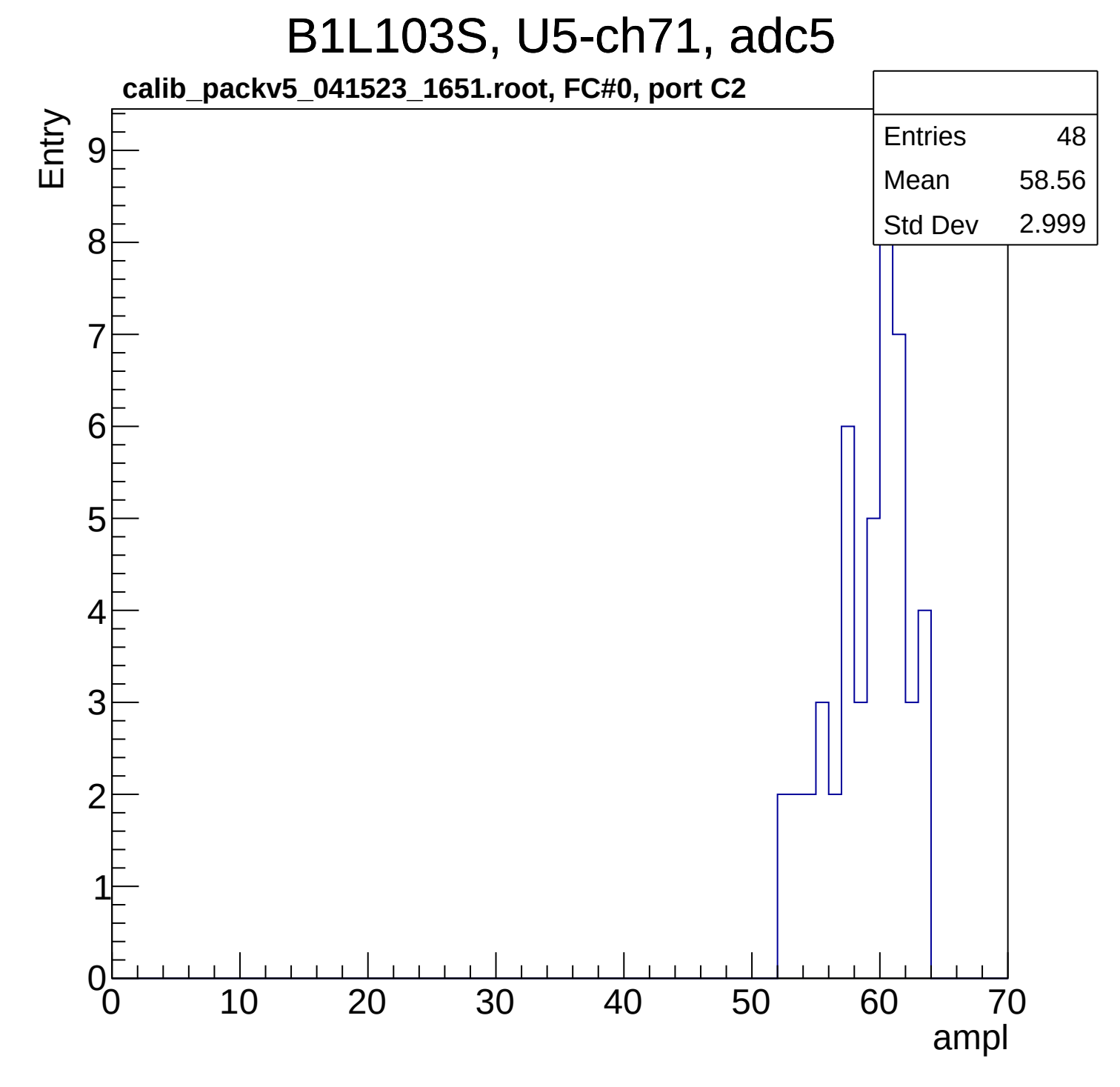
B1L103S, U5-ch71, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.56
Std Dev 2.999
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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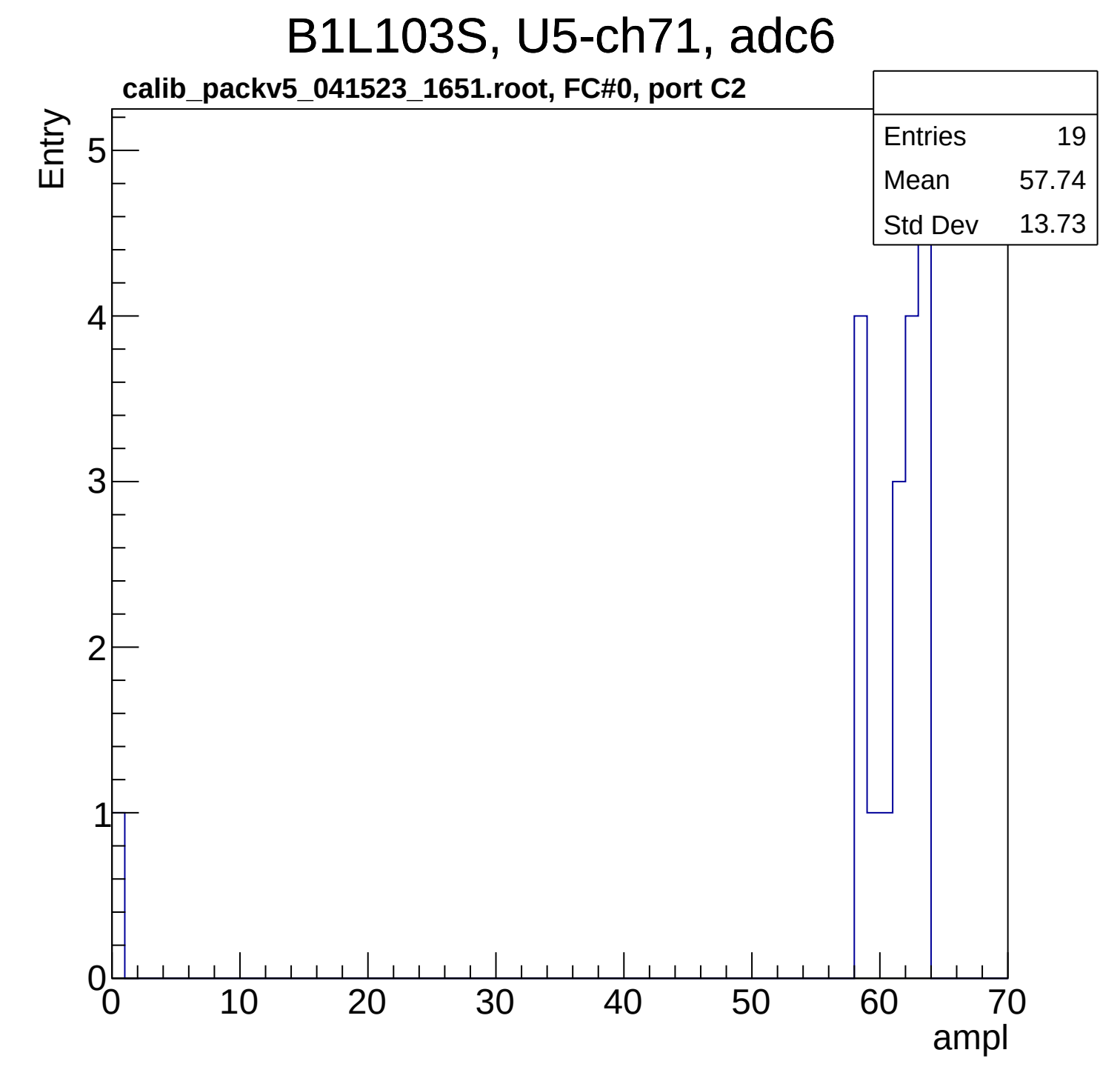
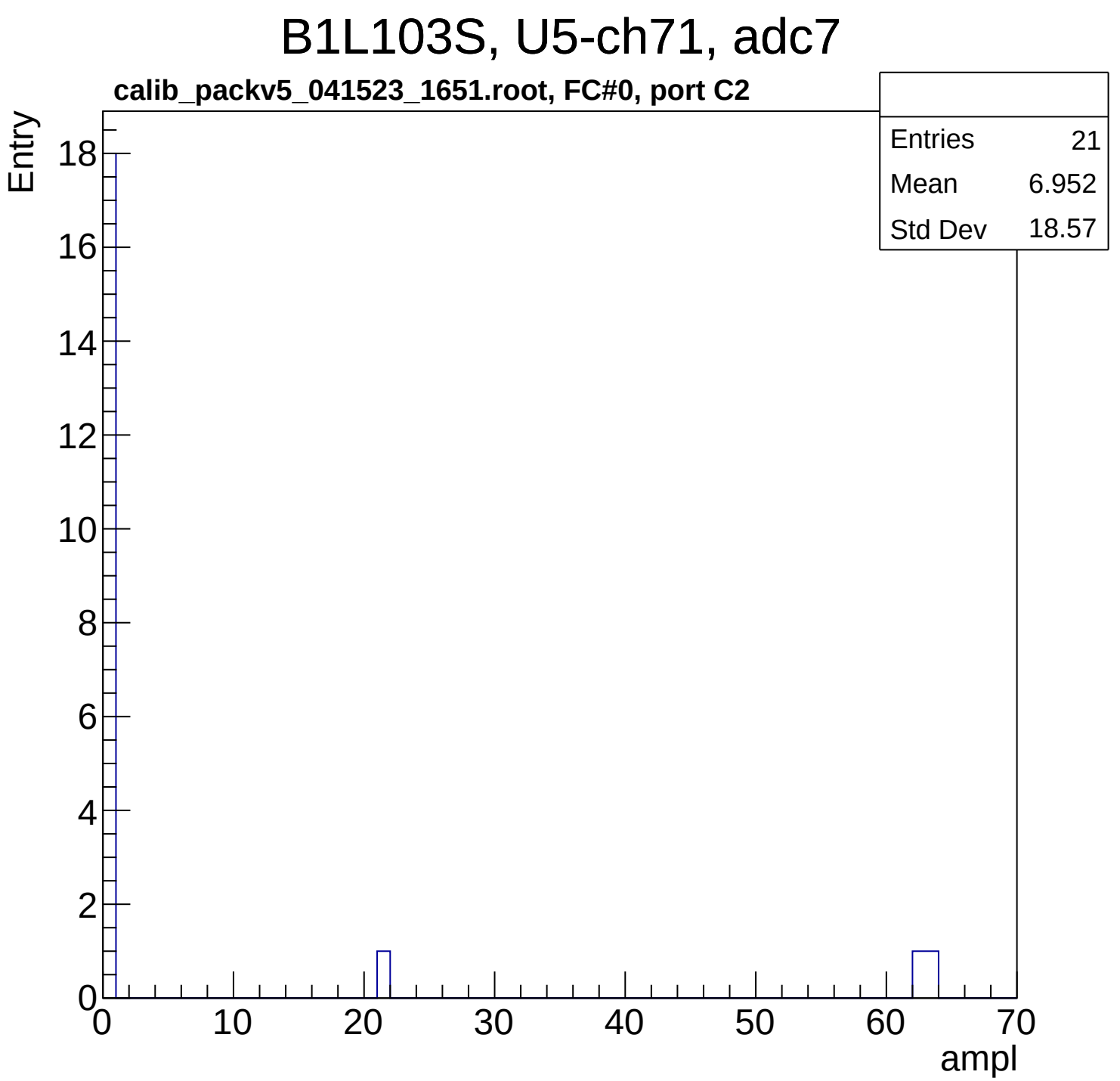

B1L103S, U5-ch71, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 57.74
Std Dev 13.73
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U5-ch71, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6.952
Std Dev 18.57
Entry
0
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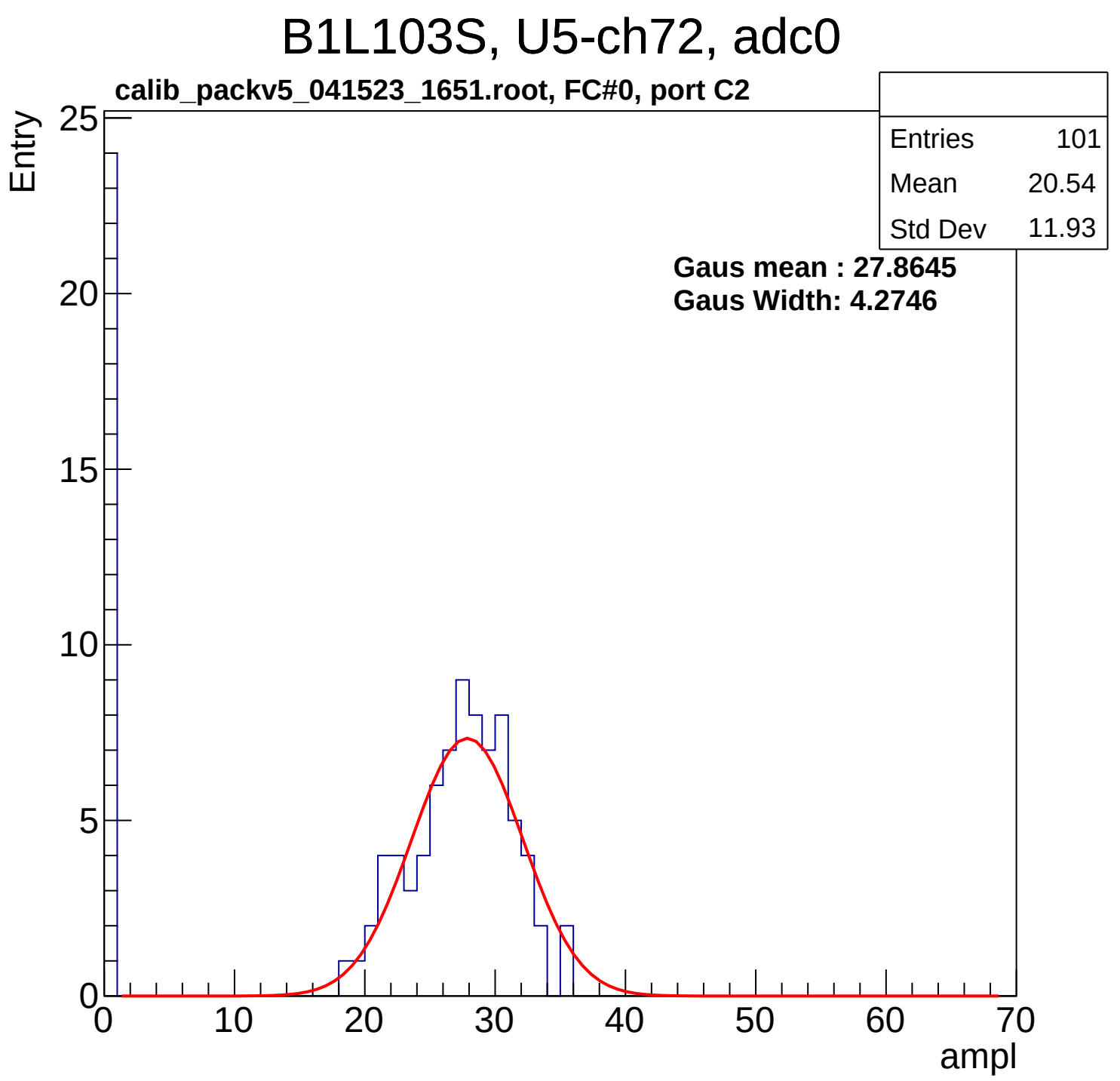
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch72, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 20.54
Std Dev 11.93
Gaus mean : 27.8645
Gaus Width: 4.2746
Entry
ampl
0
5
10
15
20
25
0
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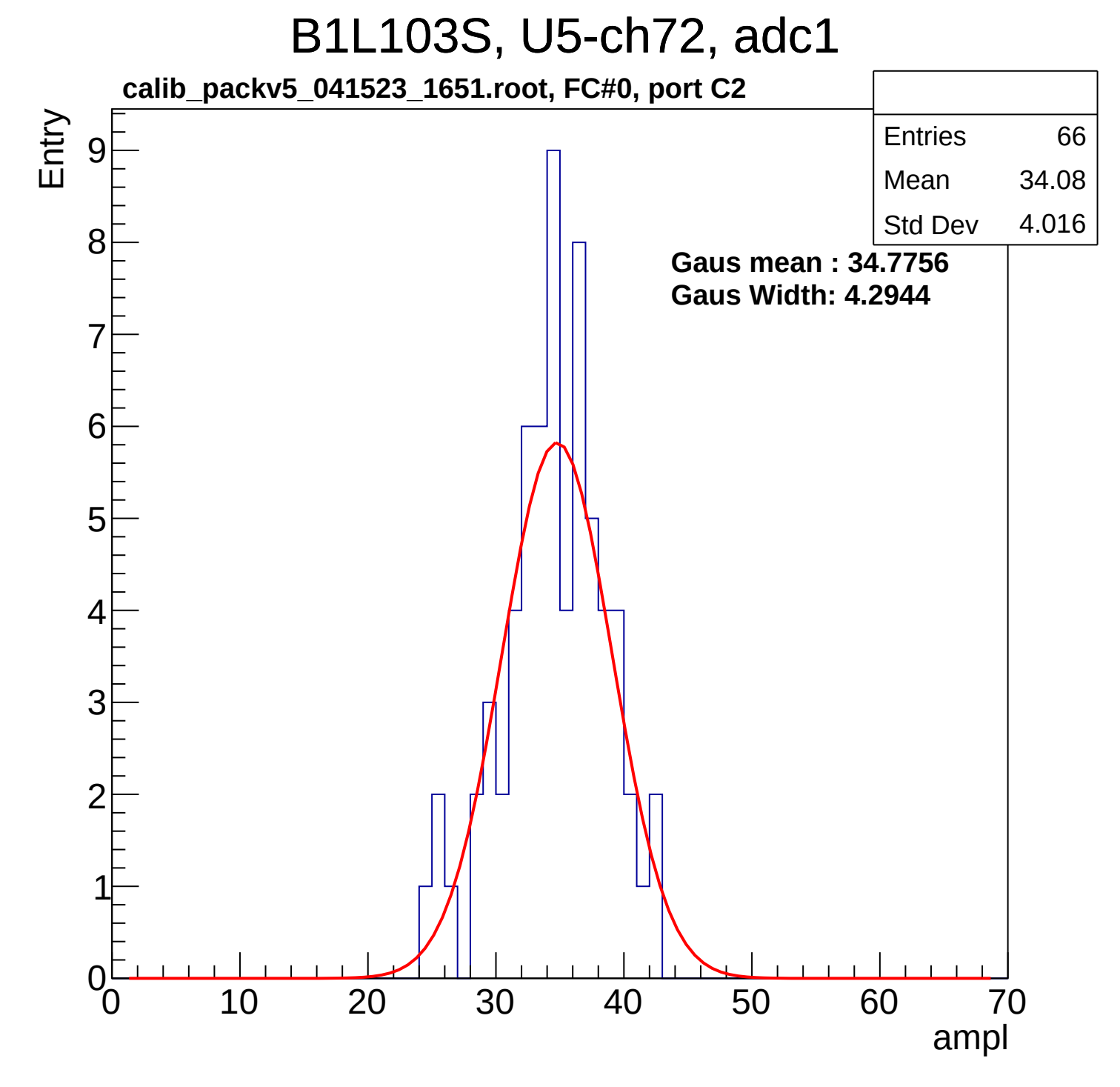
20
30
40
50
60
70


B1L103S, U5-ch72, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 34.08
Std Dev 4.016
Gaus mean : 34.7756
Gaus Width: 4.2944
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
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60
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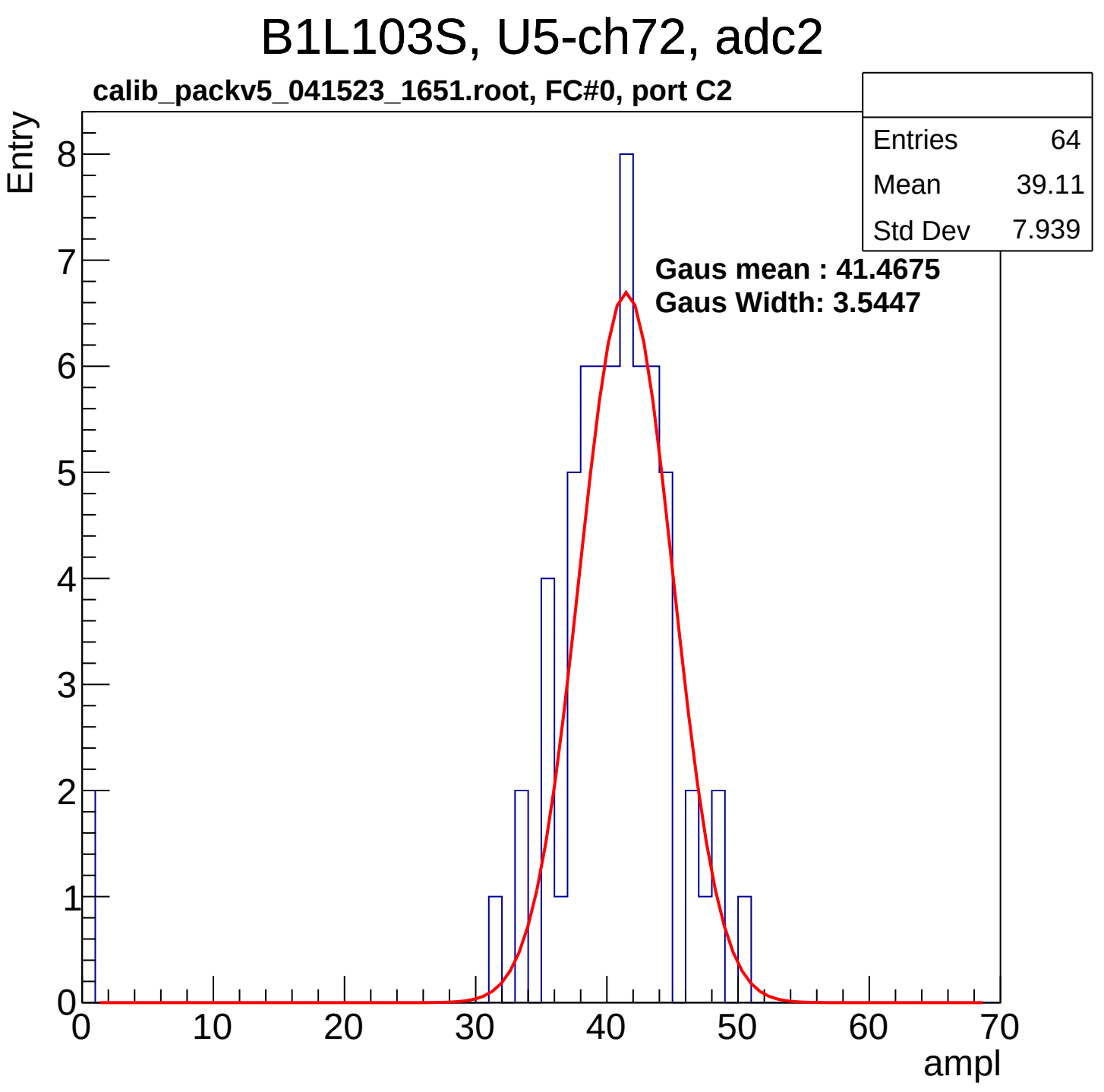
B1L103S, U5-ch72, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 39.11
Std Dev 7.939
Gaus mean : 41.4675
Gaus Width: 3.5447
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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60
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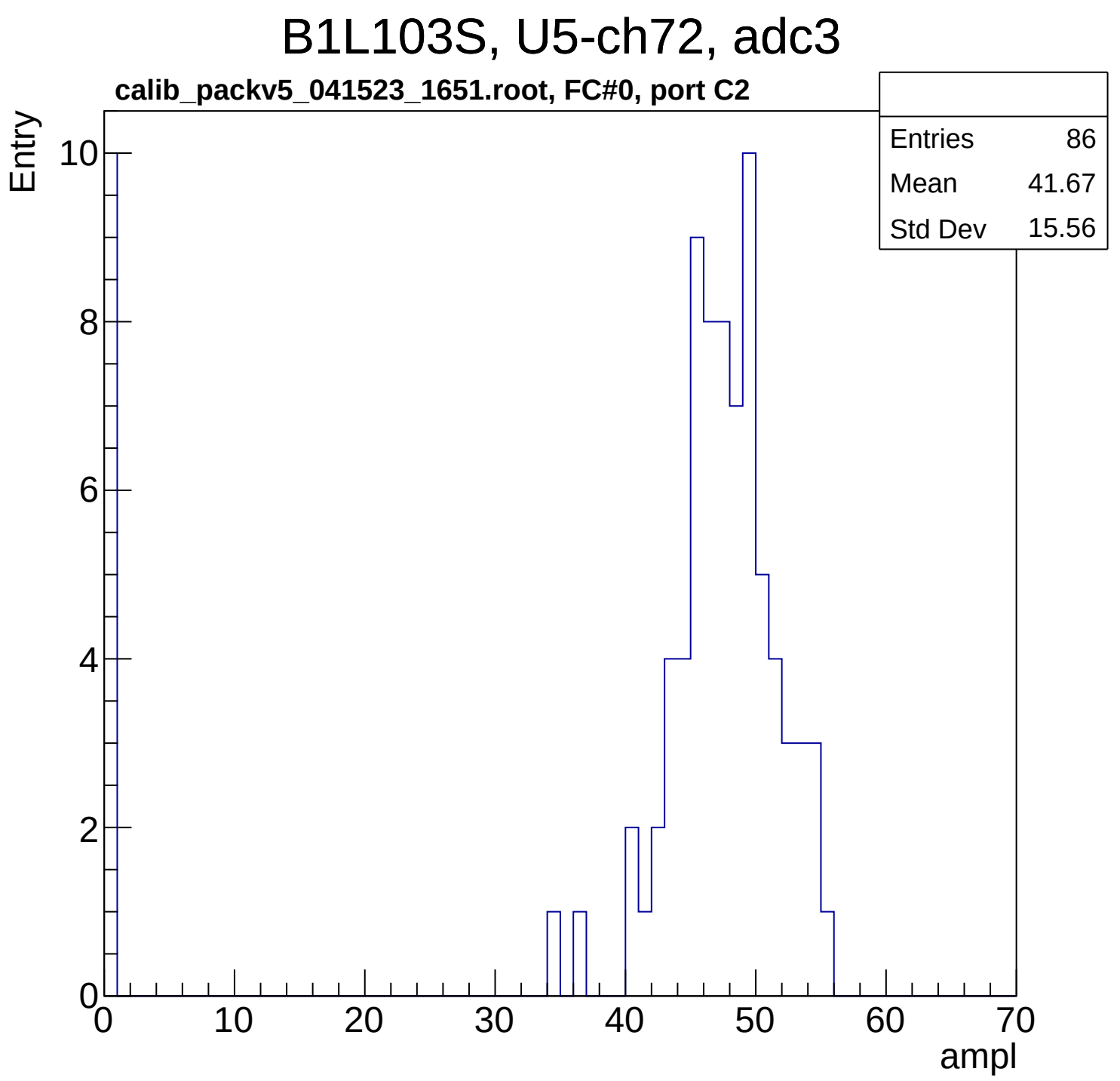
B1L103S, U5-ch72, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 41.67
Std Dev 15.56
Entry
ampl
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2
4
6
8
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0
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20
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60
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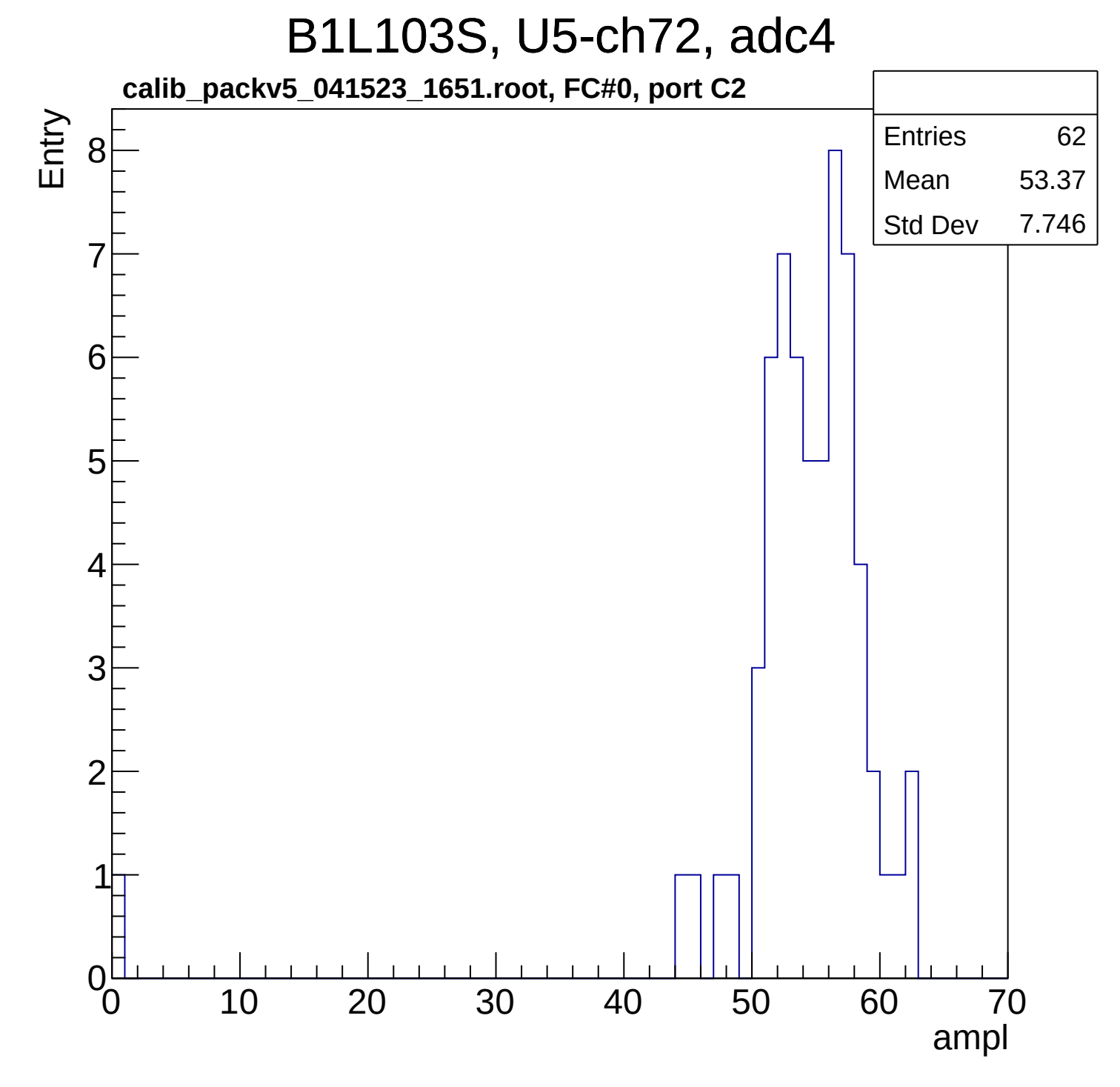
B1L103S, U5-ch72, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 53.37
Std Dev 7.746
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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50
60
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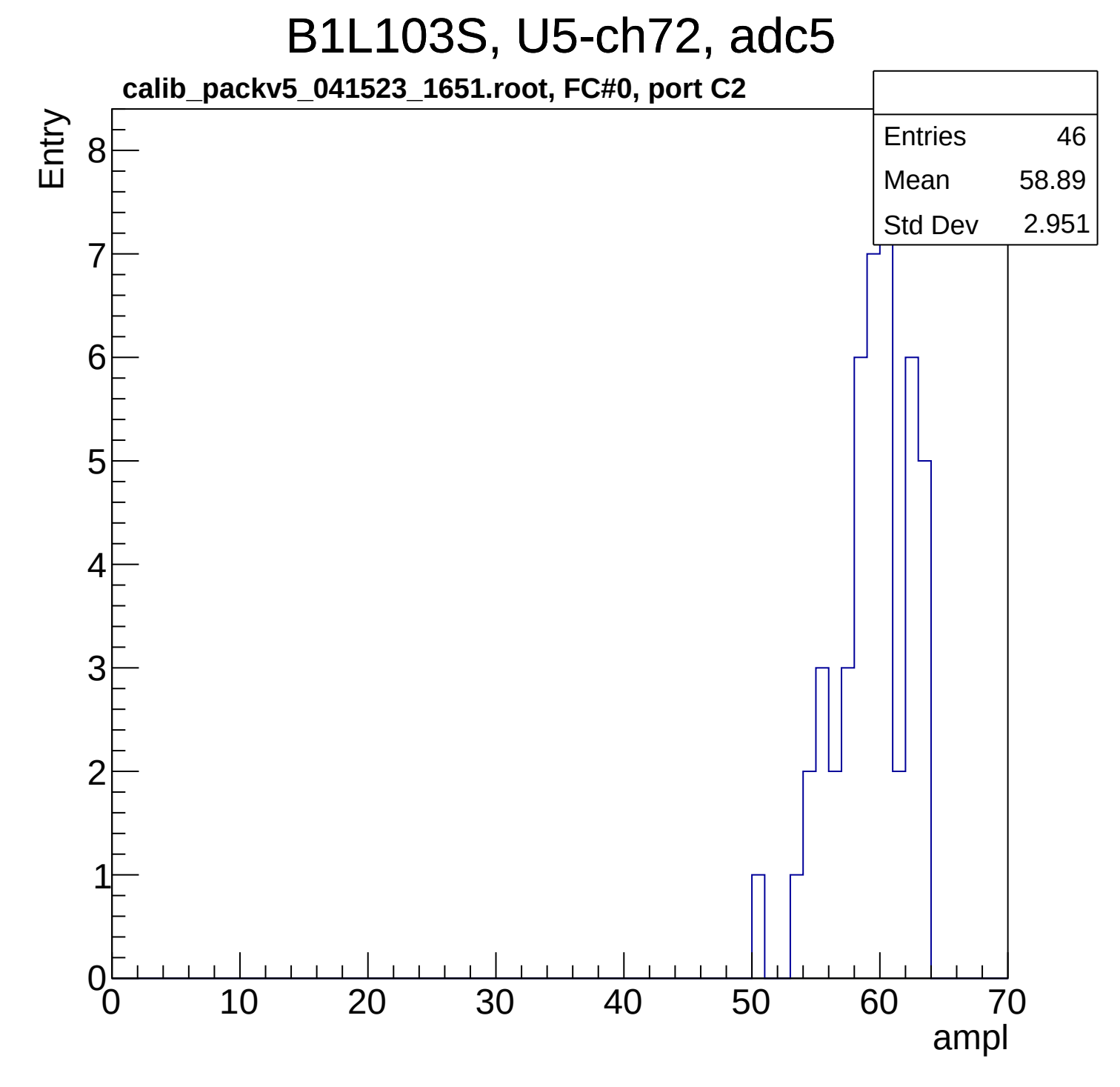
B1L103S, U5-ch72, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.89
Std Dev 2.951
Entry
ampl
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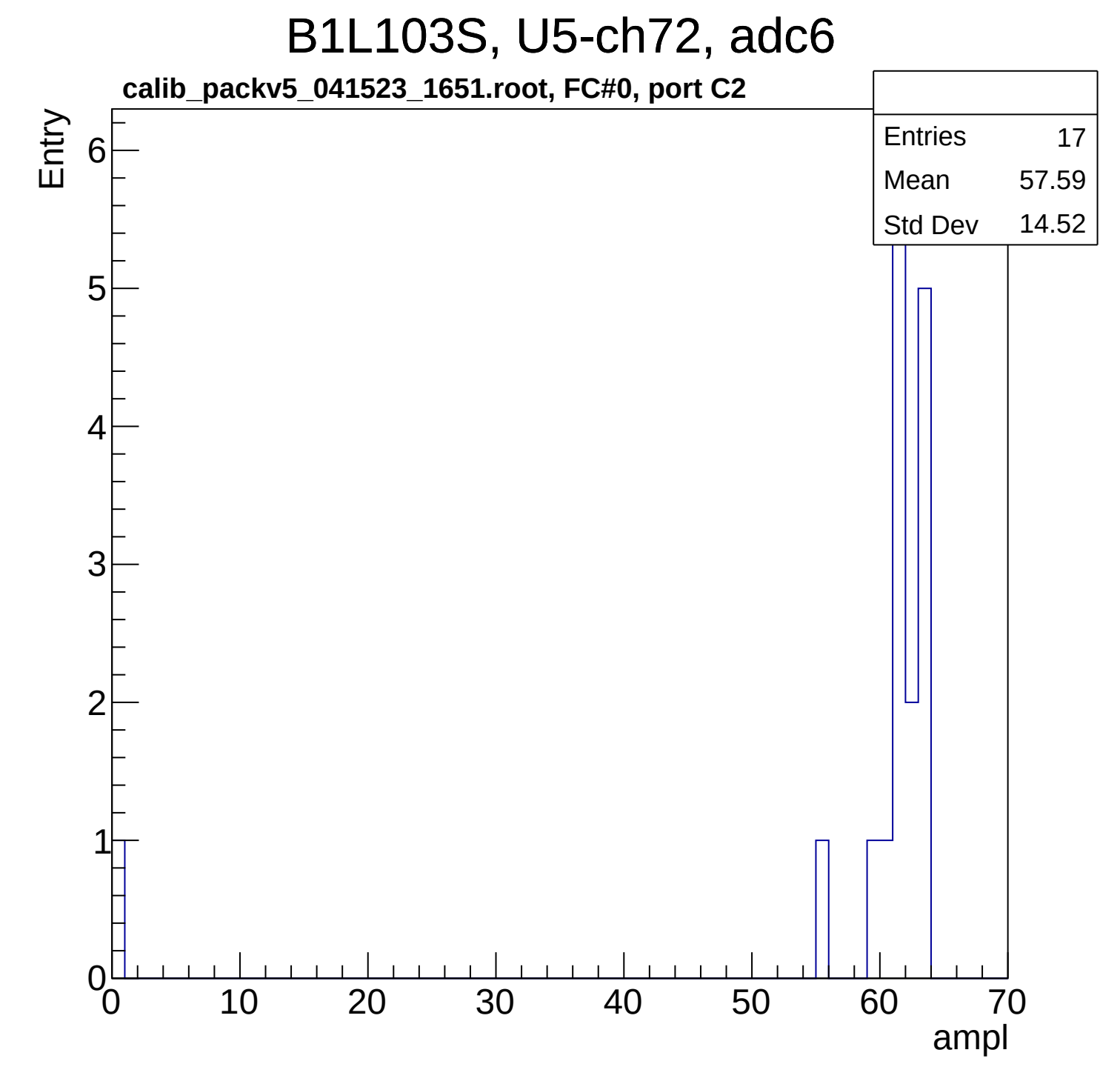
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U5-ch72, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 57.59
Std Dev 14.52
Entry
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2
3
4
5
6
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10
20
30
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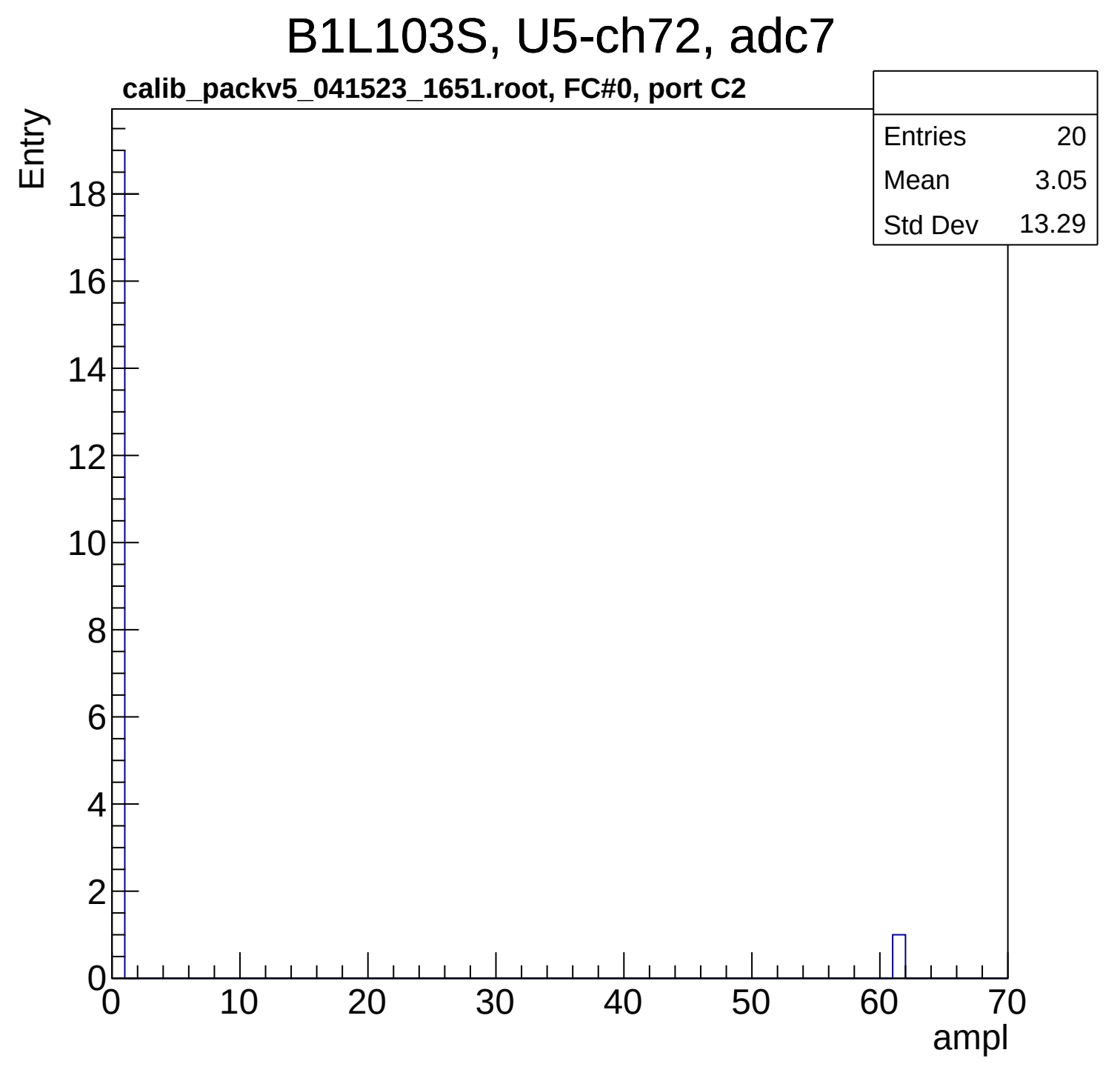
50
60
70
ampl


B1L103S, U5-ch72, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
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6
8
10
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14
16
18
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10
20
30
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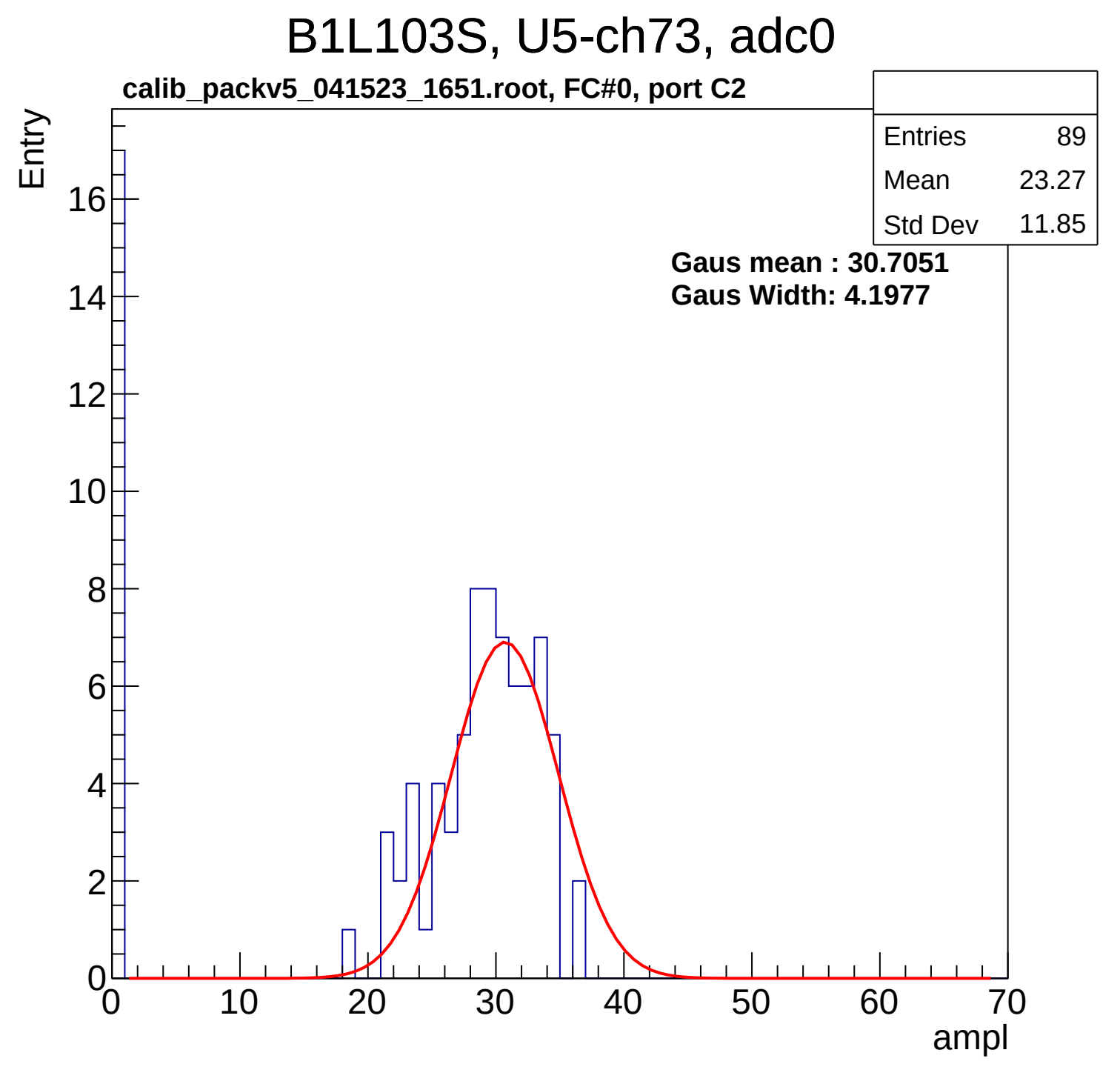
50
60
70
ampl


B1L103S, U5-ch73, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 23.27
Std Dev 11.85
Gaus mean : 30.7051
Gaus Width: 4.1977
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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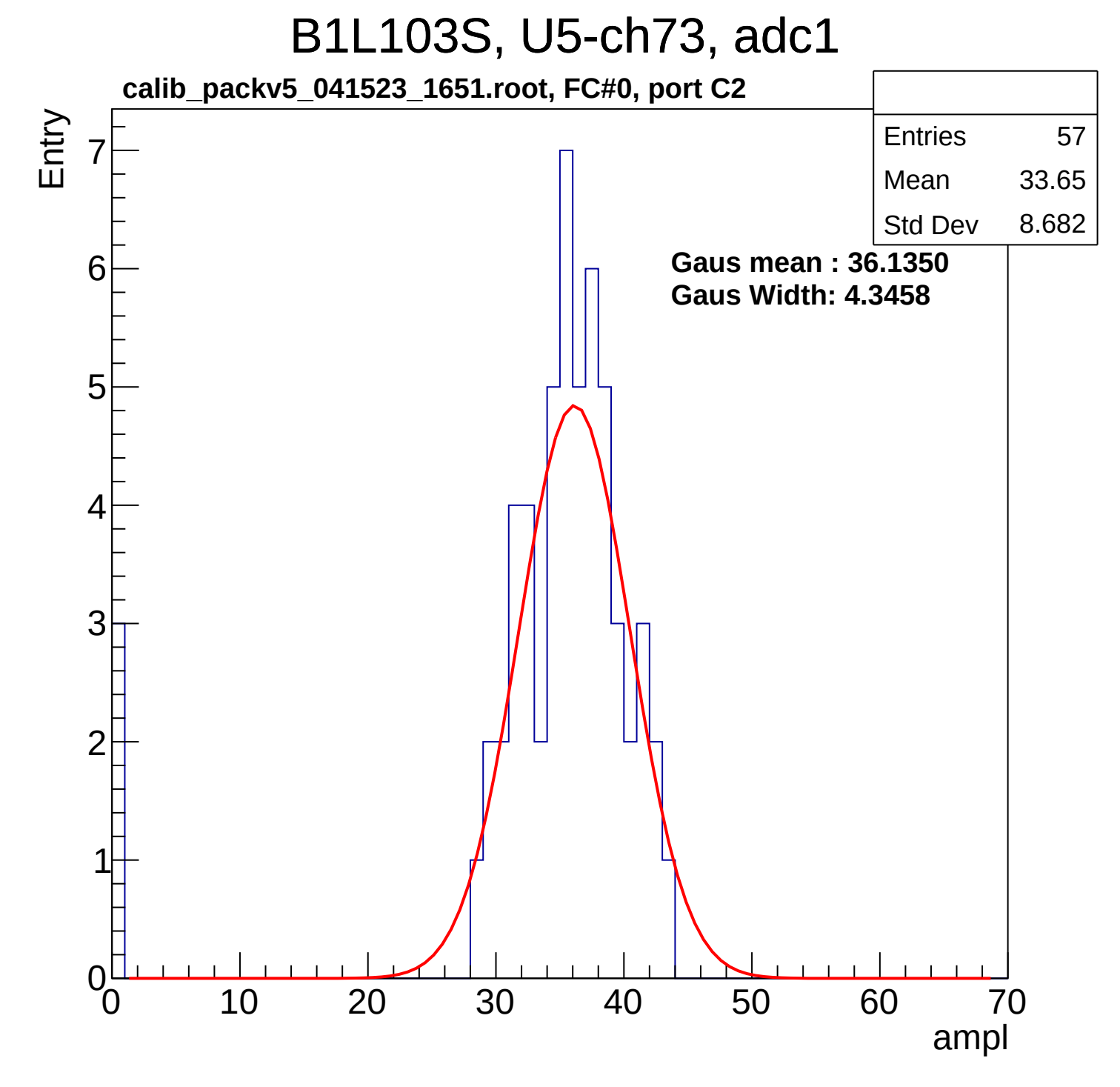
B1L103S, U5-ch73, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 33.65
Std Dev 8.682
Gaus mean : 36.1350
Gaus Width: 4.3458
Entry
ampl
0
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2
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0
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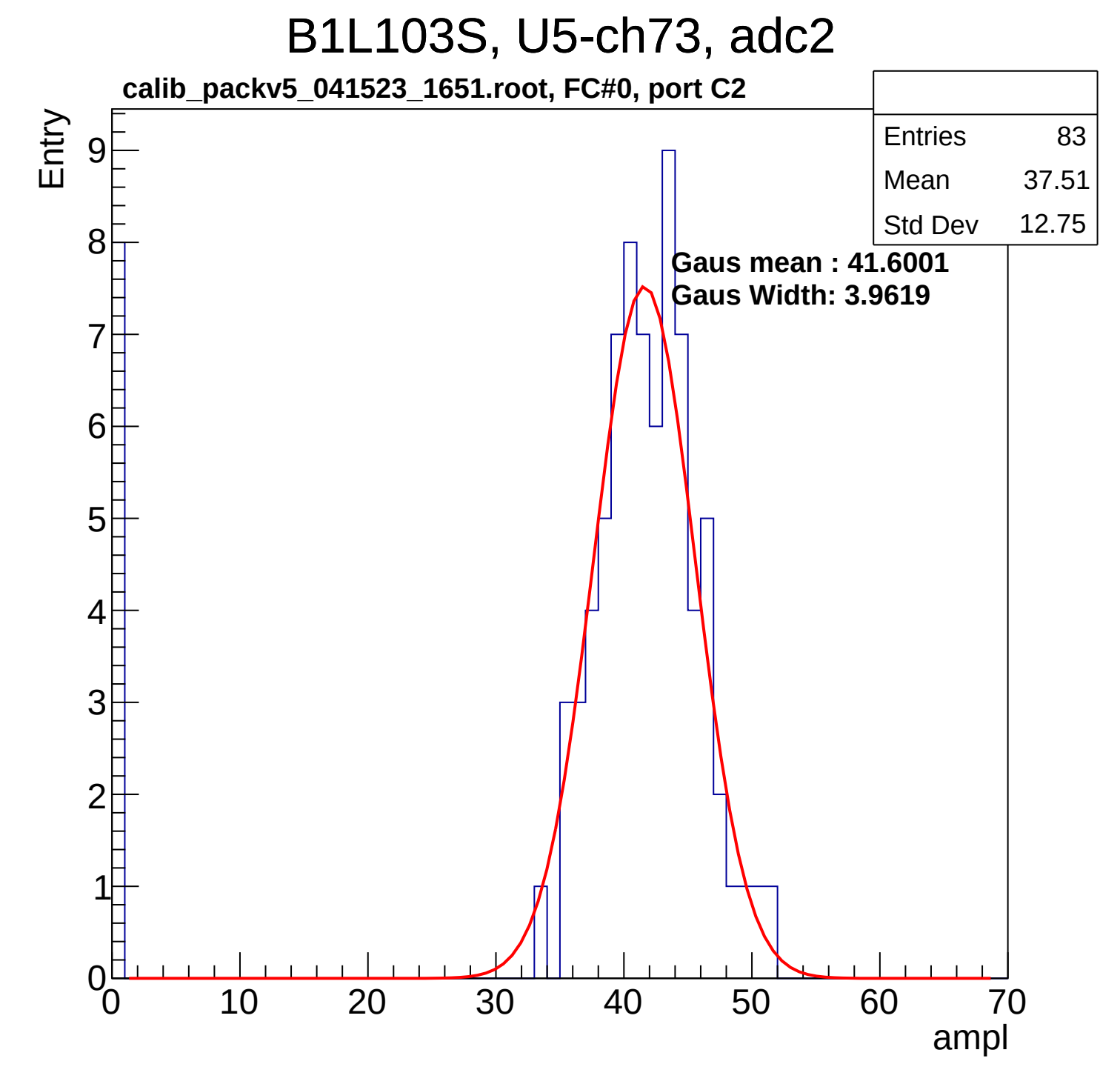
B1L103S, U5-ch73, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 37.51
Std Dev 12.75
Gaus mean : 41.6001
Gaus Width: 3.9619
Entry
ampl
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2
3
4
5
6
7
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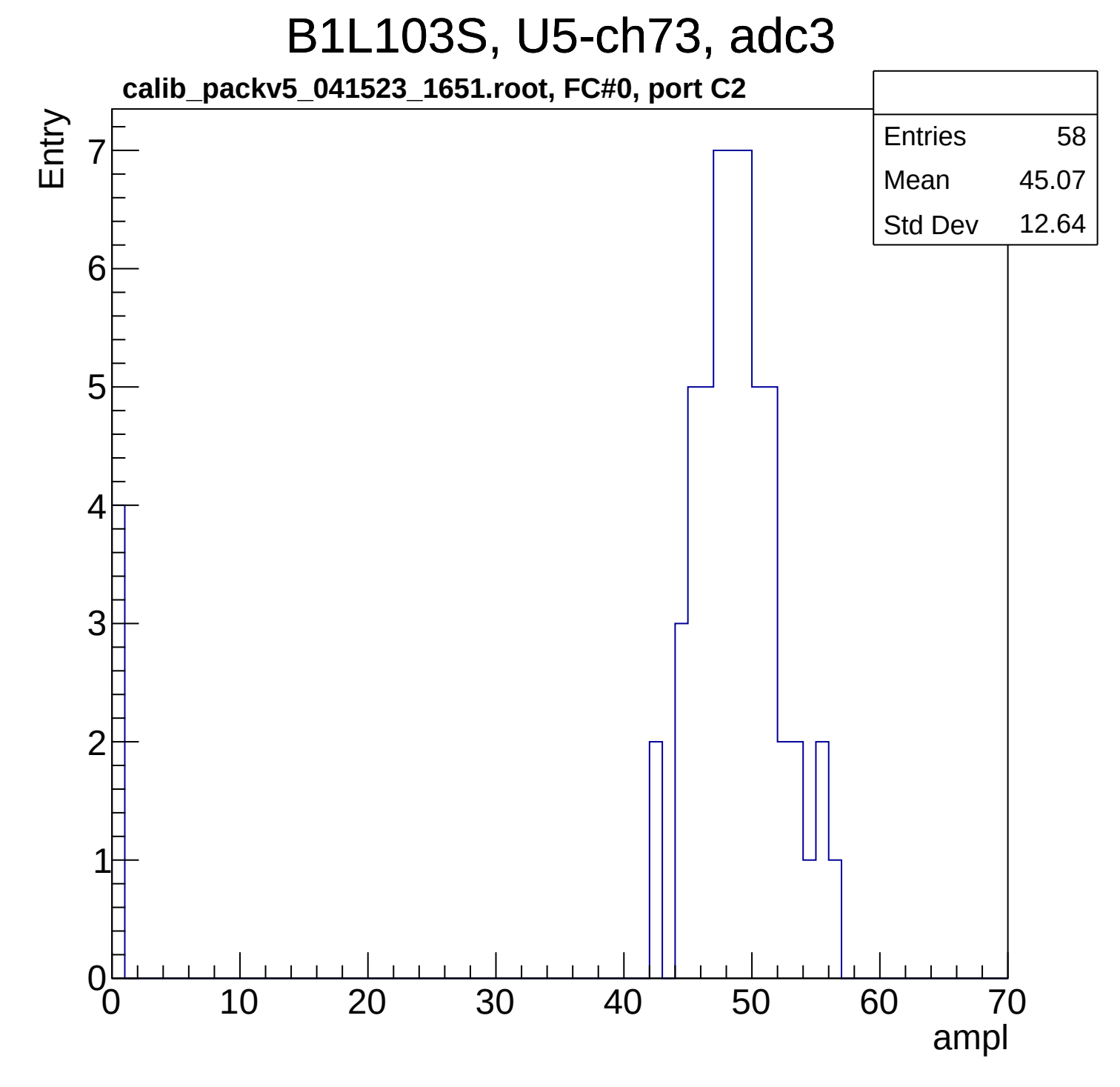
B1L103S, U5-ch73, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 45.07
Std Dev 12.64
Entry
ampl
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2
3
4
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6
7
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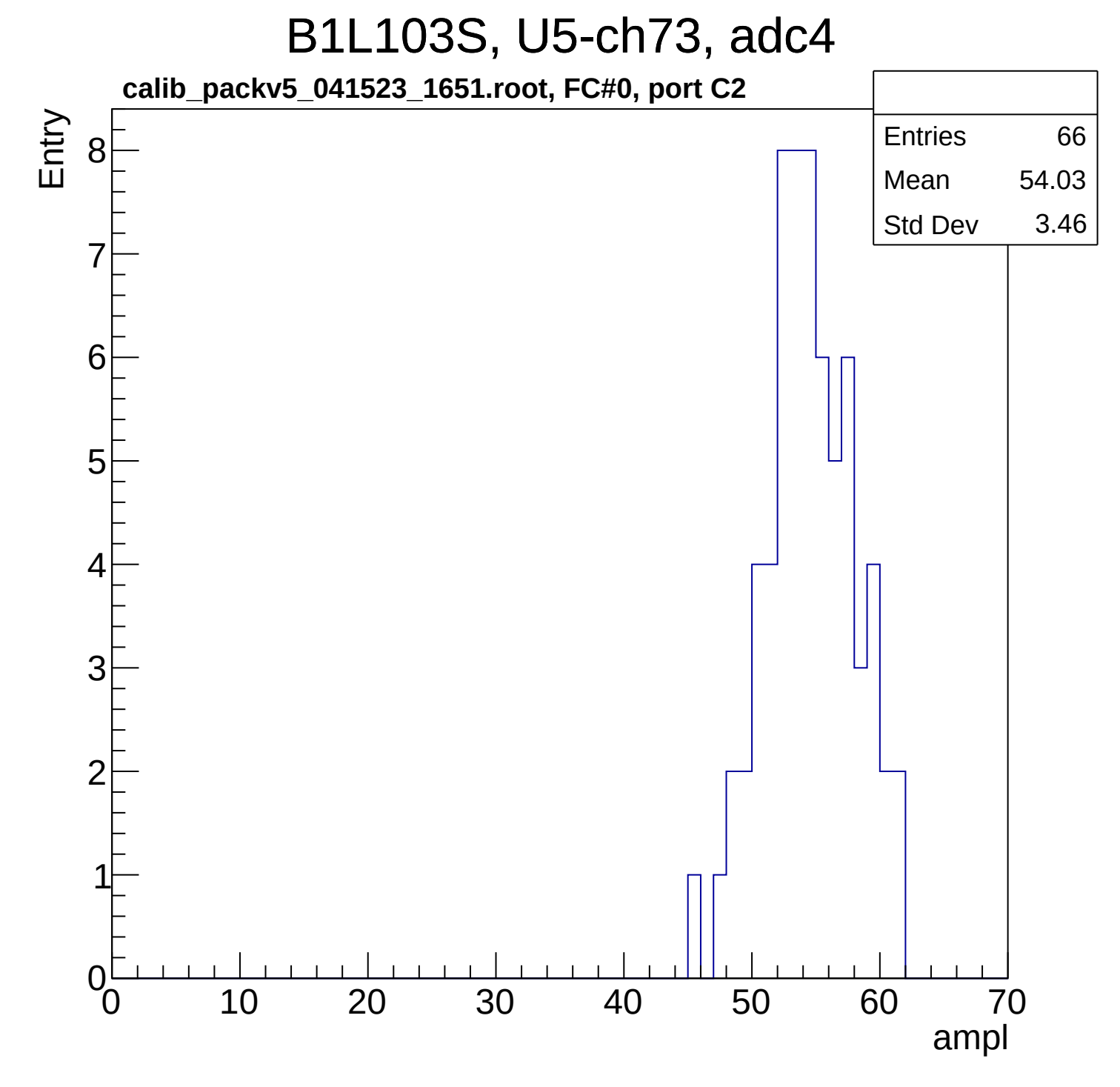
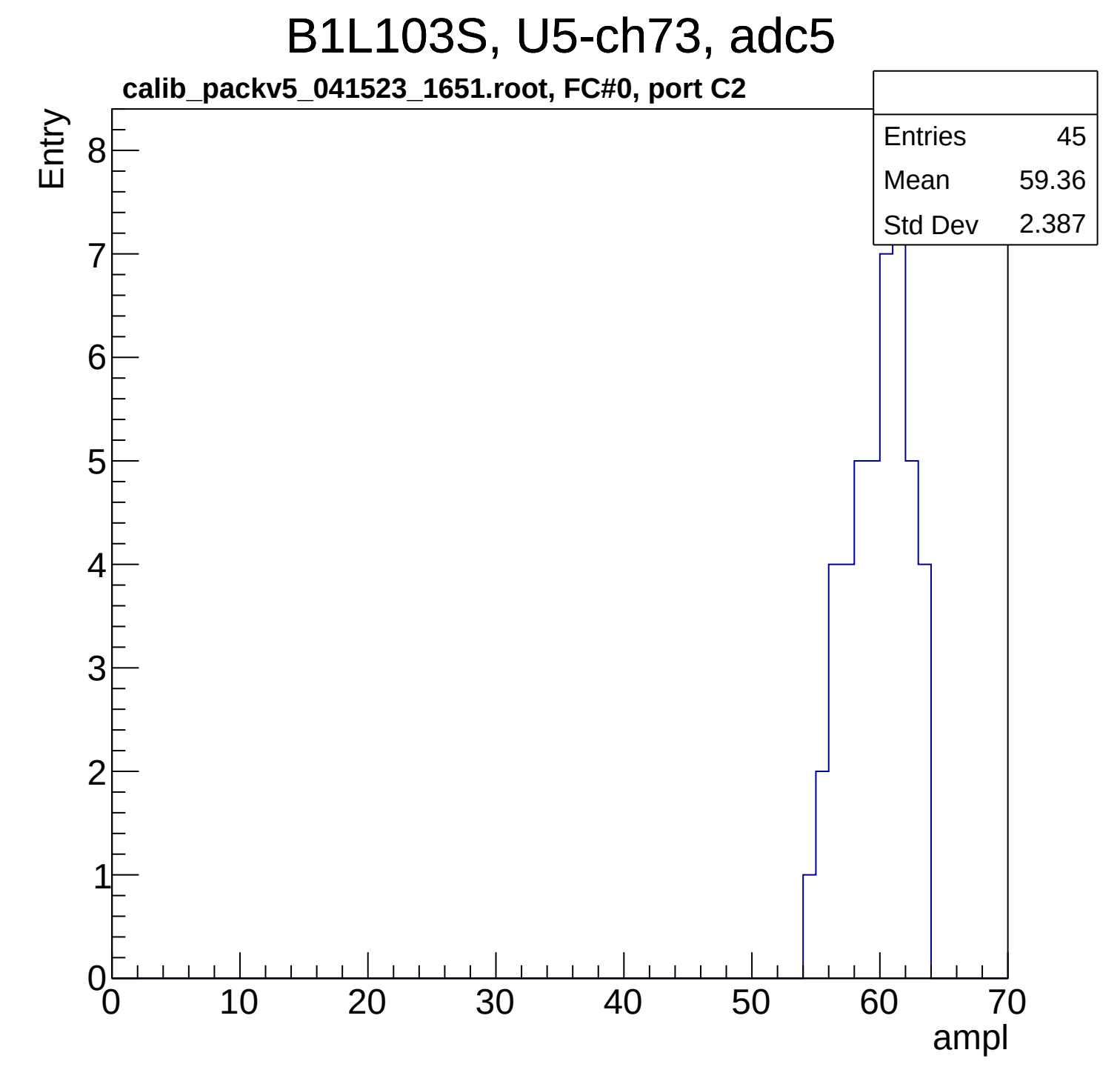

B1L103S, U5-ch73, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 54.03
Std Dev 3.46
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U5-ch73, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 59.36
Std Dev 2.387
Entry
ampl
0
1
2
3
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5
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0
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60
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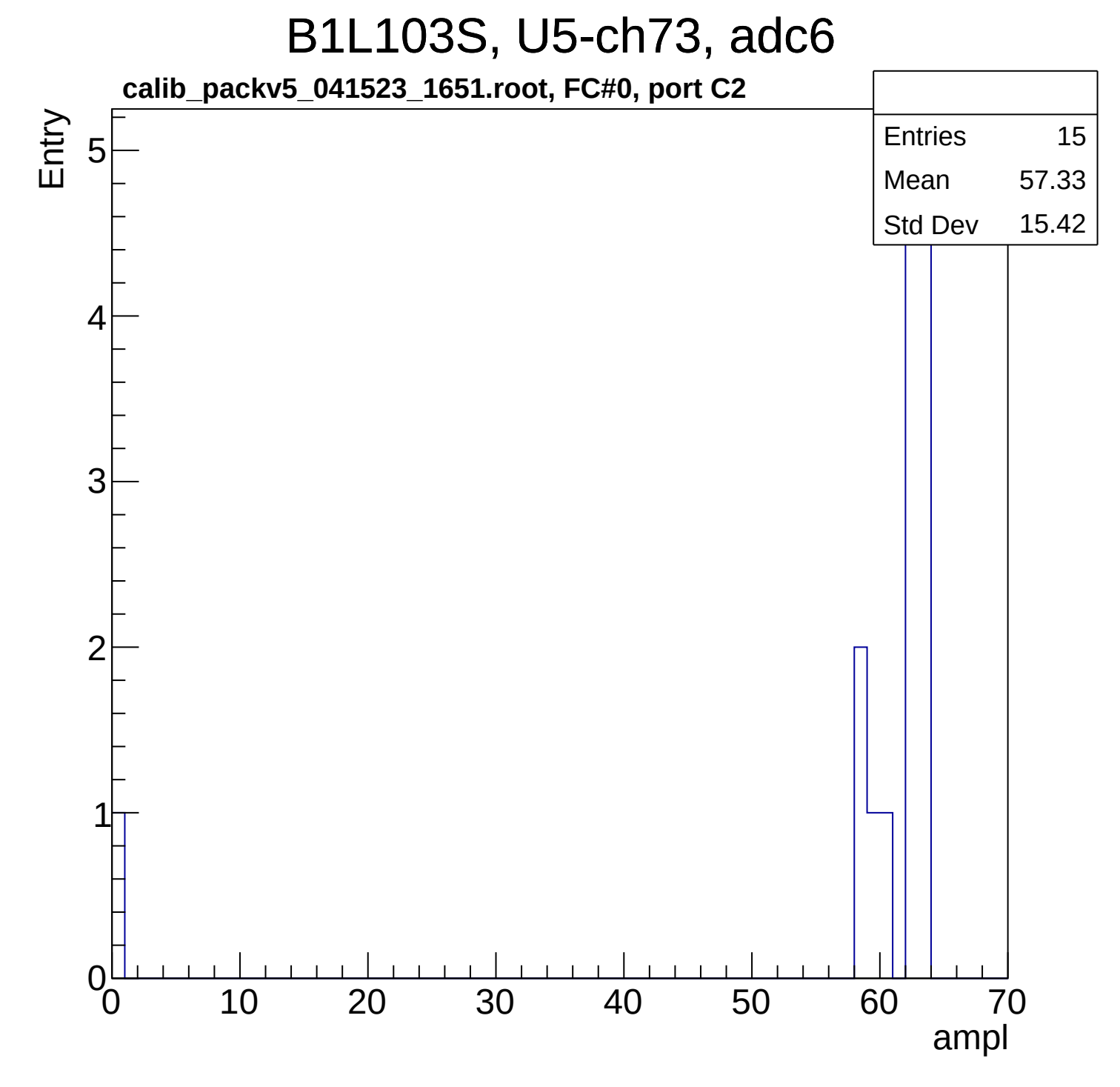
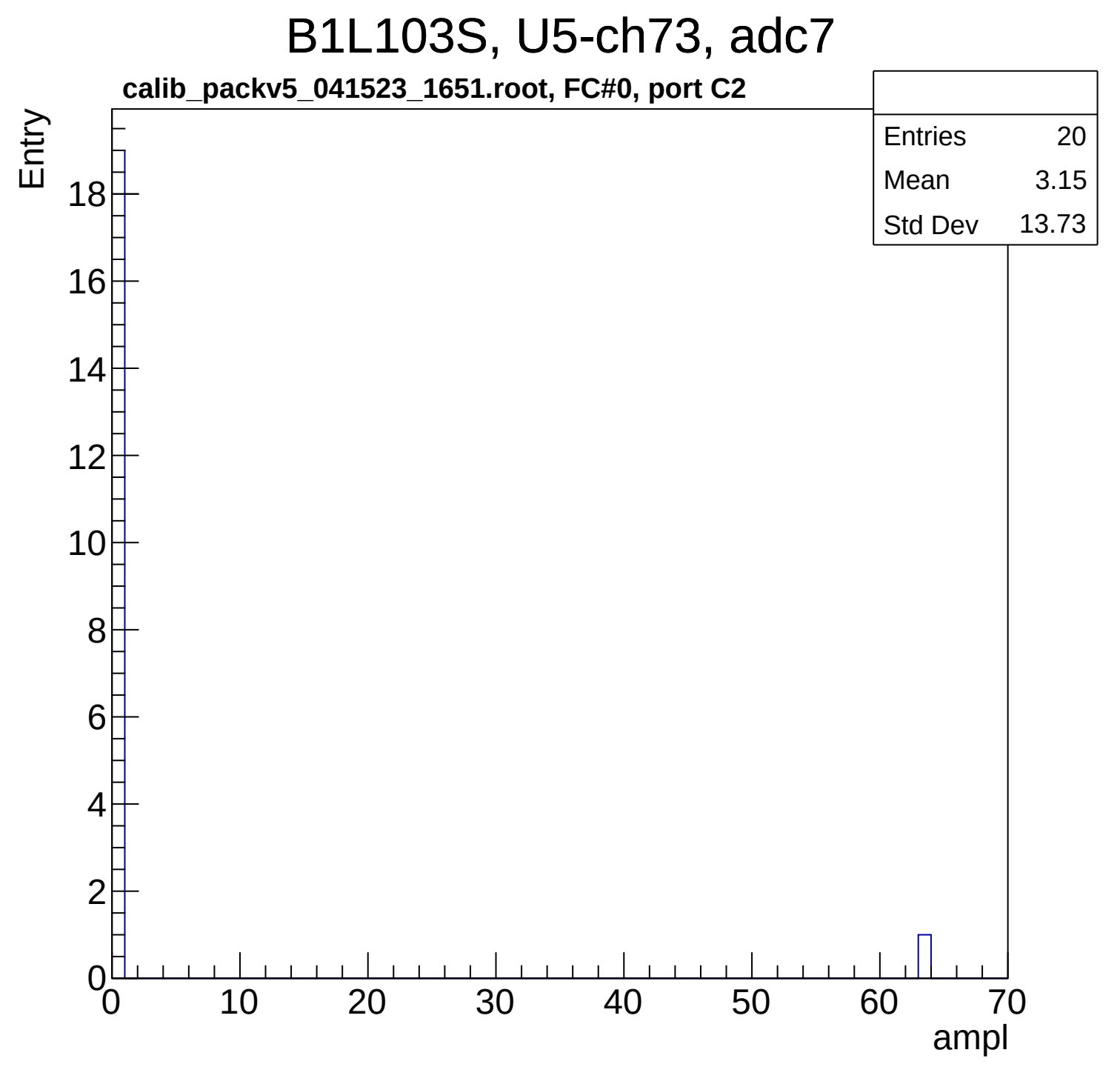
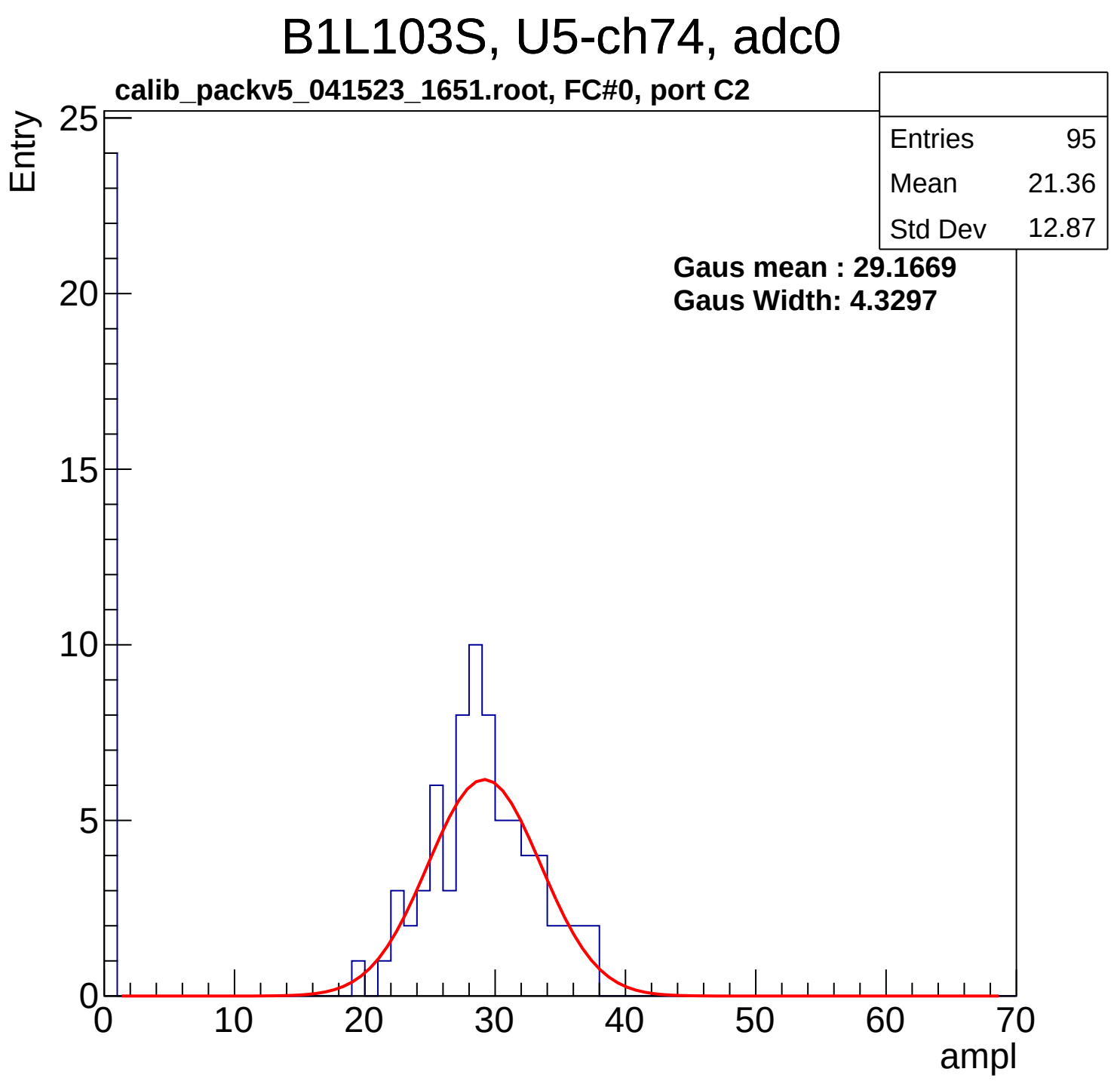

B1L103S, U5-ch73, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.33
Std Dev 15.42
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch73, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch74, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 21.36
Std Dev 12.87
Gaus mean : 29.1669
Gaus Width: 4.3297
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
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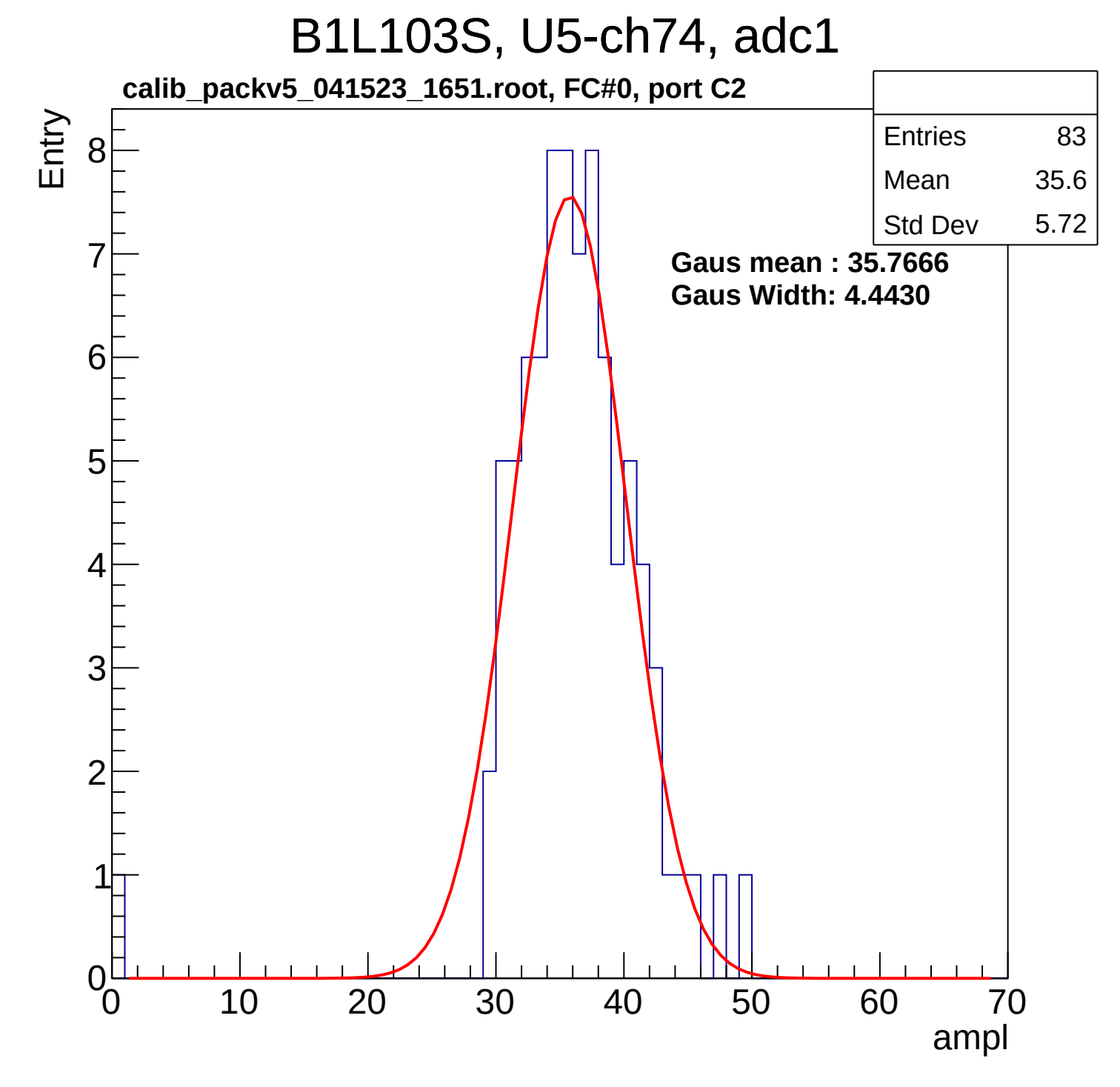
B1L103S, U5-ch74, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 35.6
Std Dev 5.72
Gaus mean : 35.7666
Gaus Width: 4.4430
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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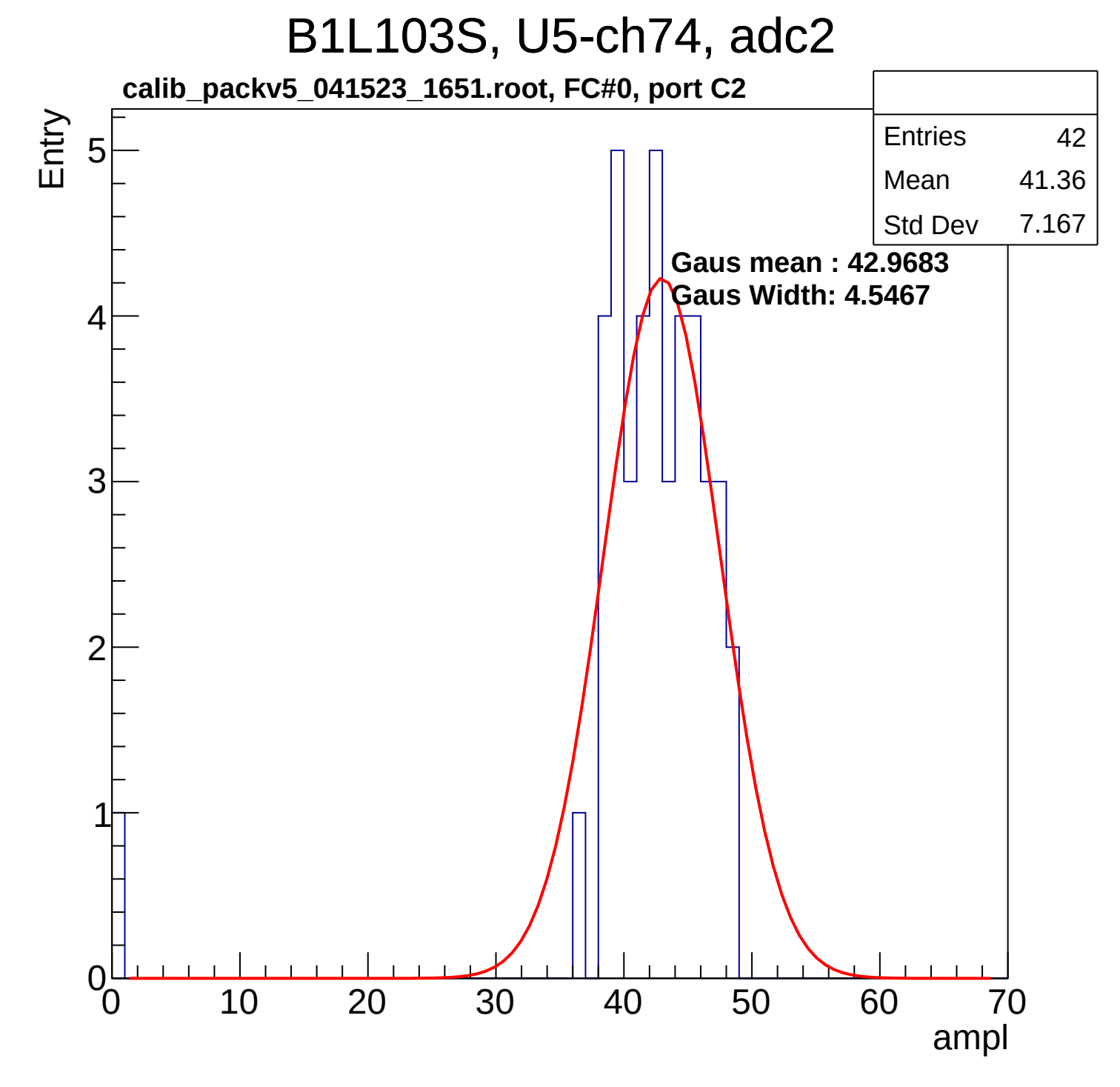
B1L103S, U5-ch74, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 41.36
Std Dev 7.167
Gaus mean : 42.9683
Gaus Width: 4.5467
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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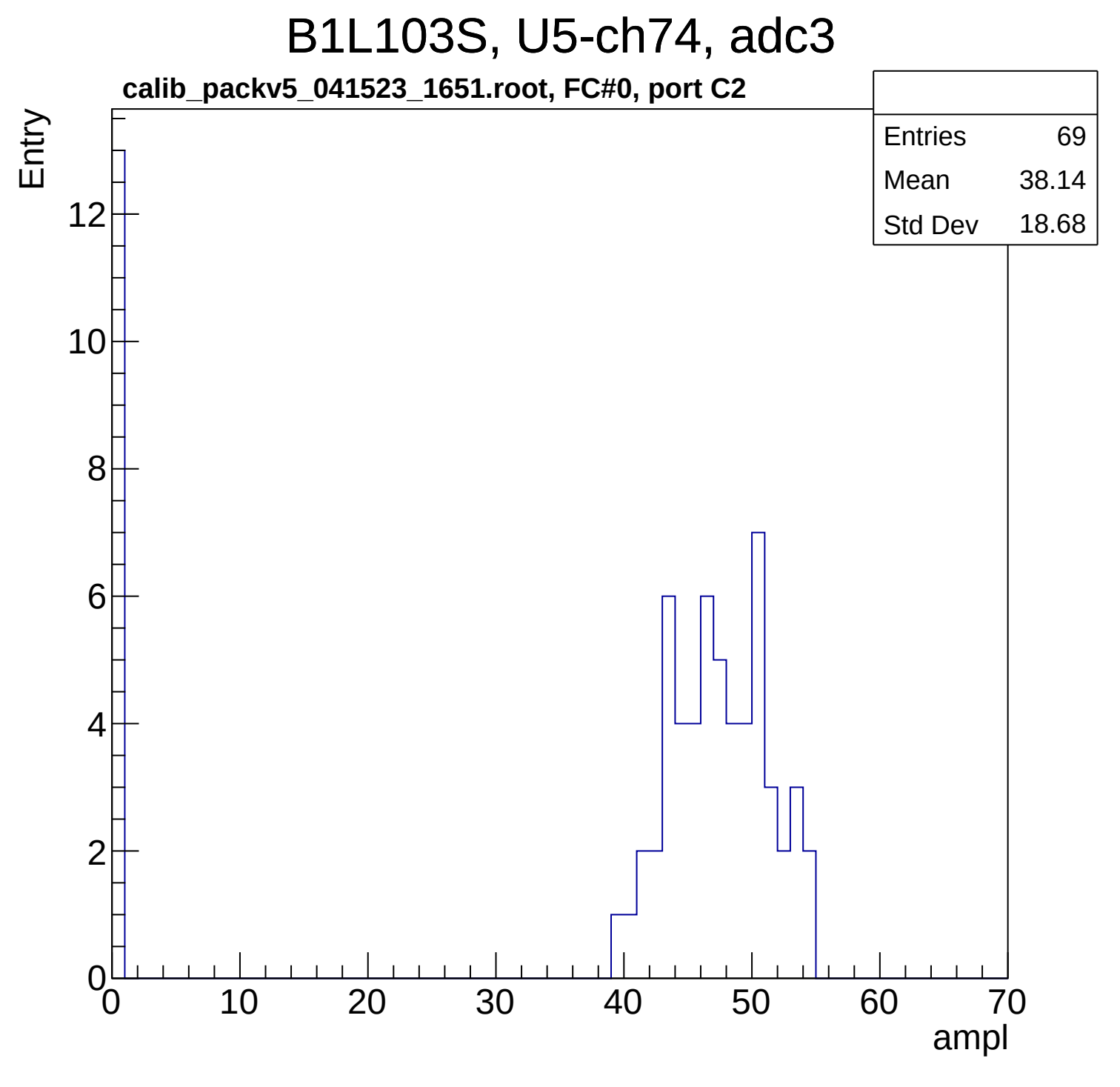
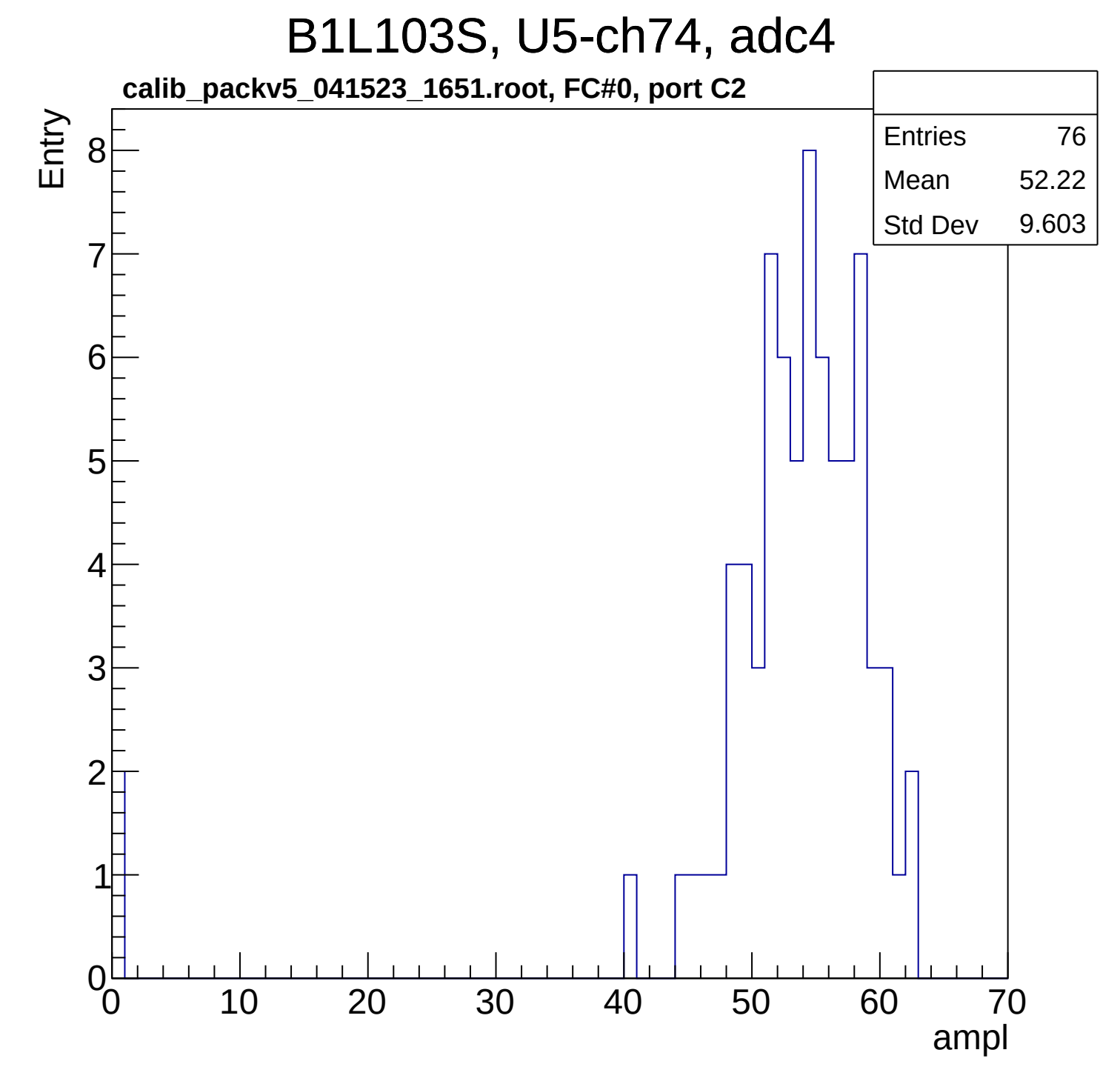

B1L103S, U5-ch74, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 38.14
Std Dev 18.68
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch74, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 52.22
Std Dev 9.603
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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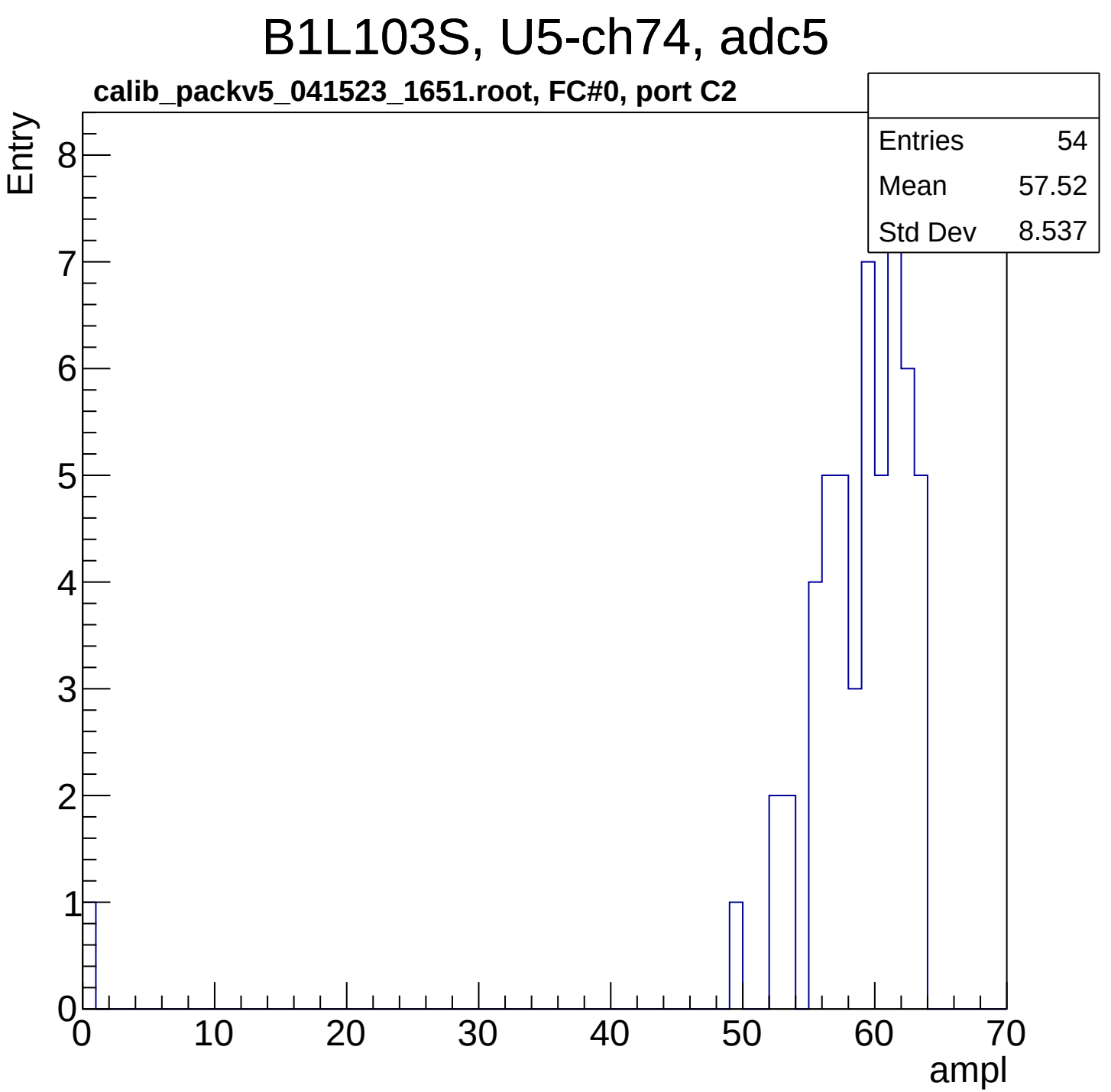
B1L103S, U5-ch74, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.52
Std Dev 8.537
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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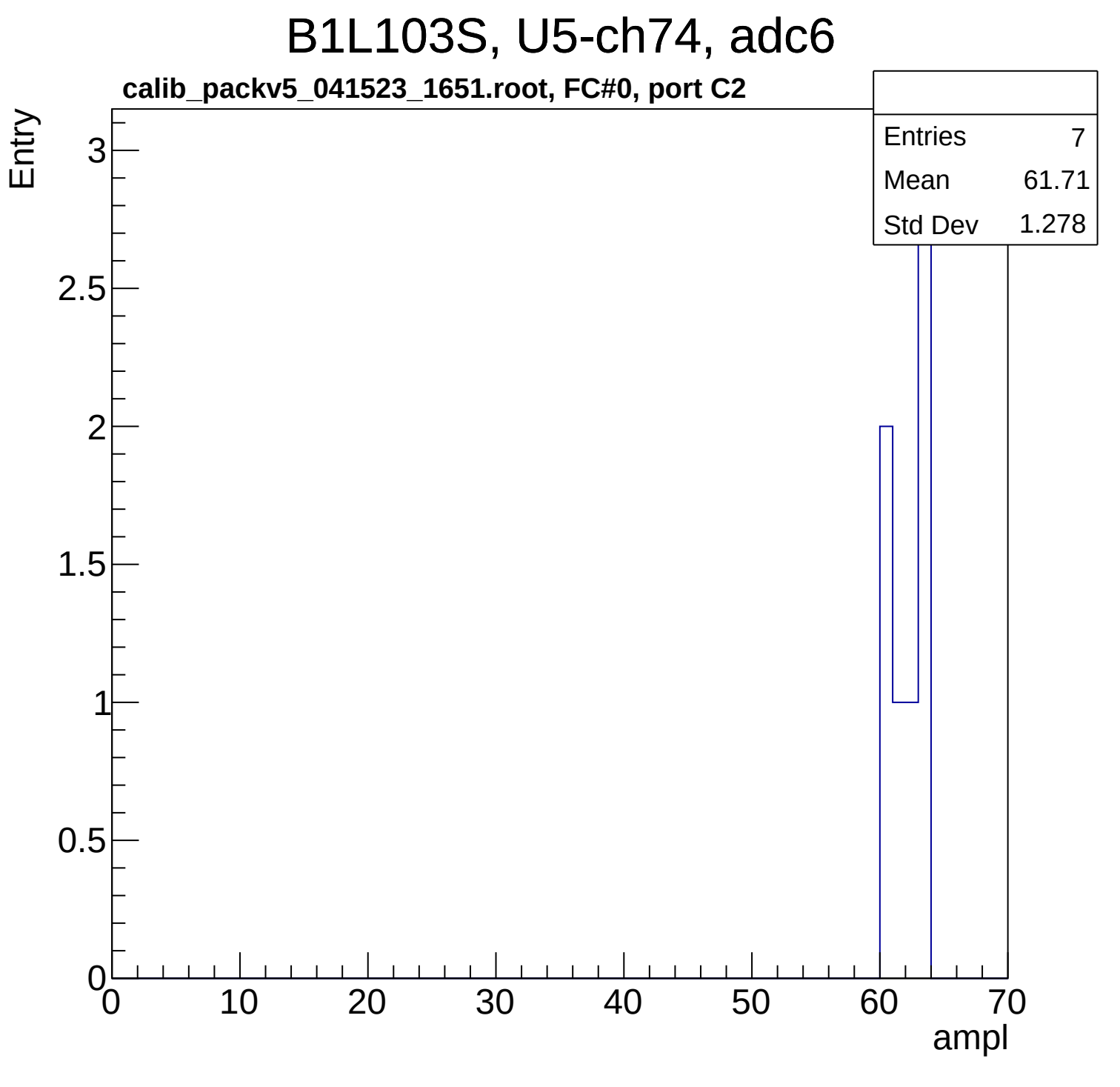
B1L103S, U5-ch74, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.71
Std Dev 1.278
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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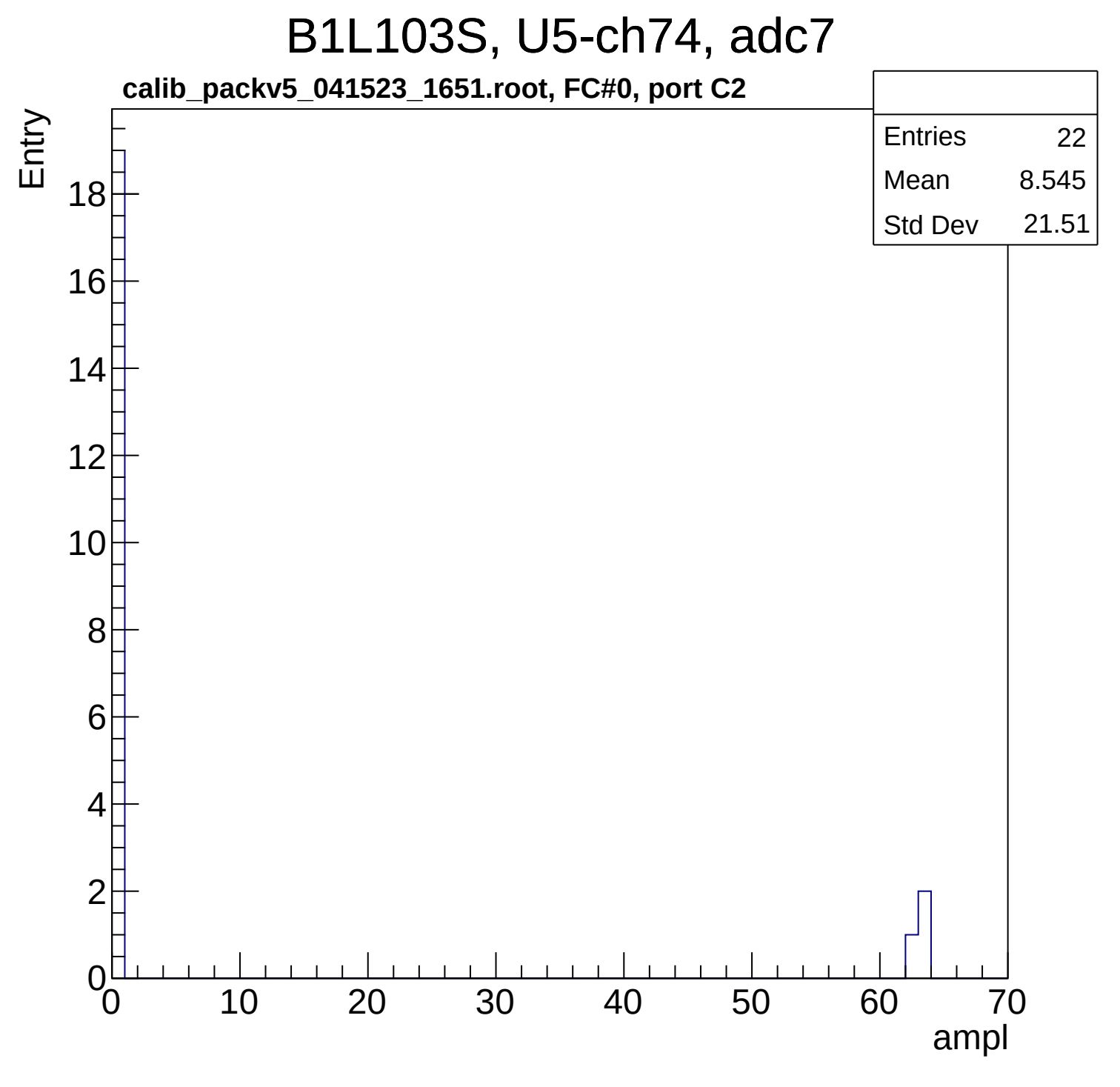
B1L103S, U5-ch74, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.545
Std Dev 21.51
Entry
0
2
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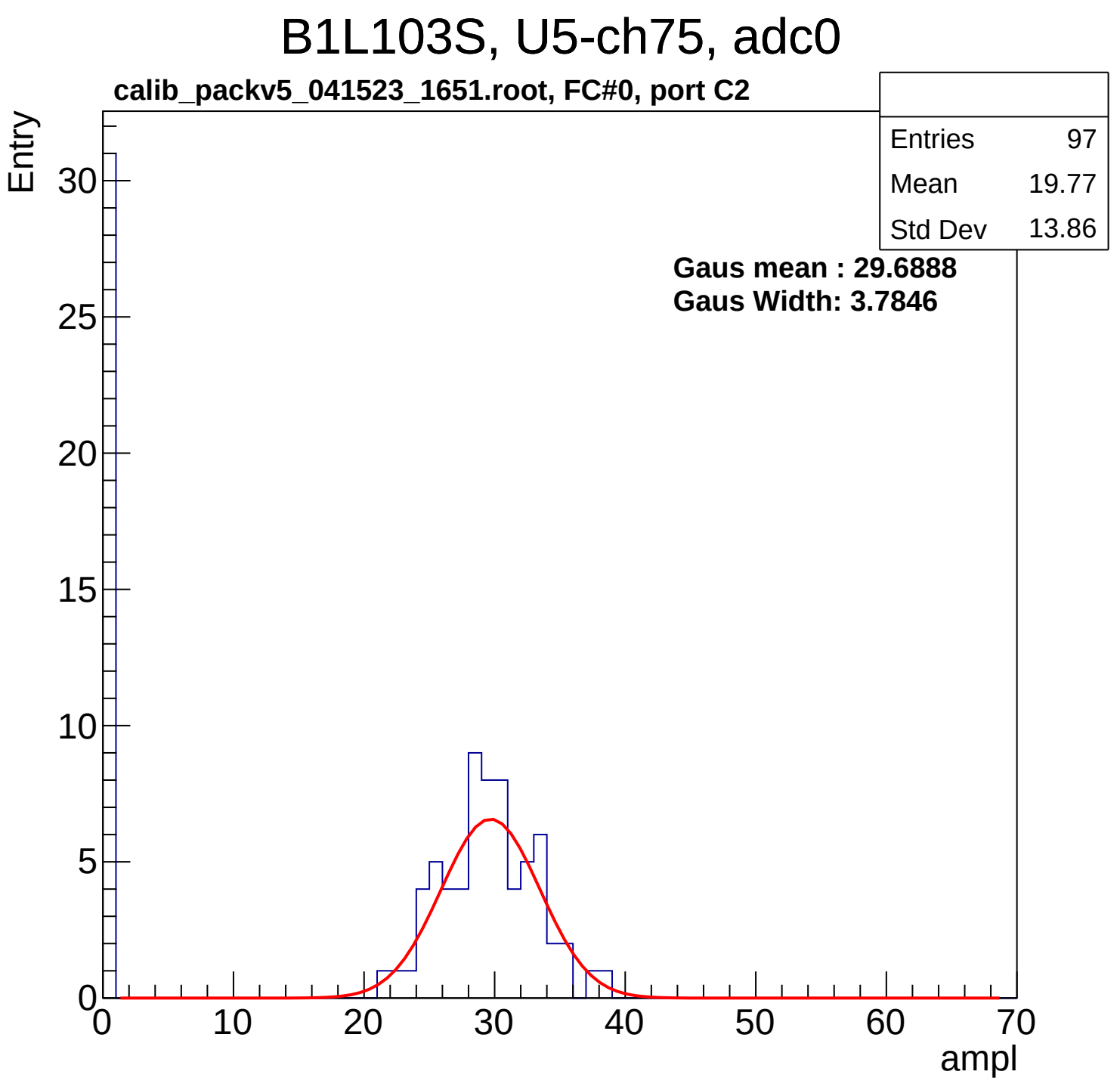
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch75, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 19.77
Std Dev 13.86
Gaus mean : 29.6888
Gaus Width: 3.7846
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
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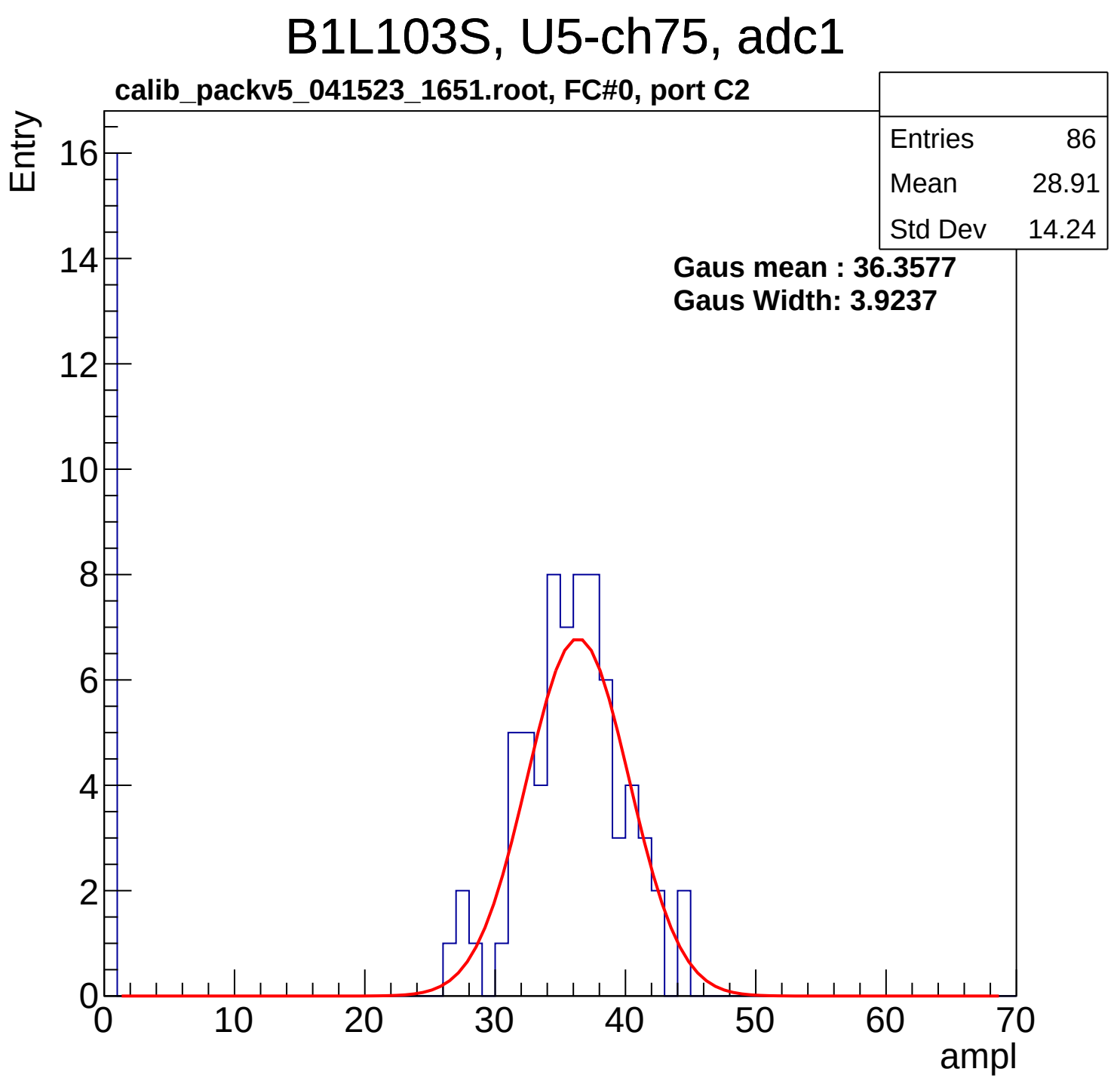
B1L103S, U5-ch75, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 28.91
Std Dev 14.24
Gaus mean : 36.3577
Gaus Width: 3.9237
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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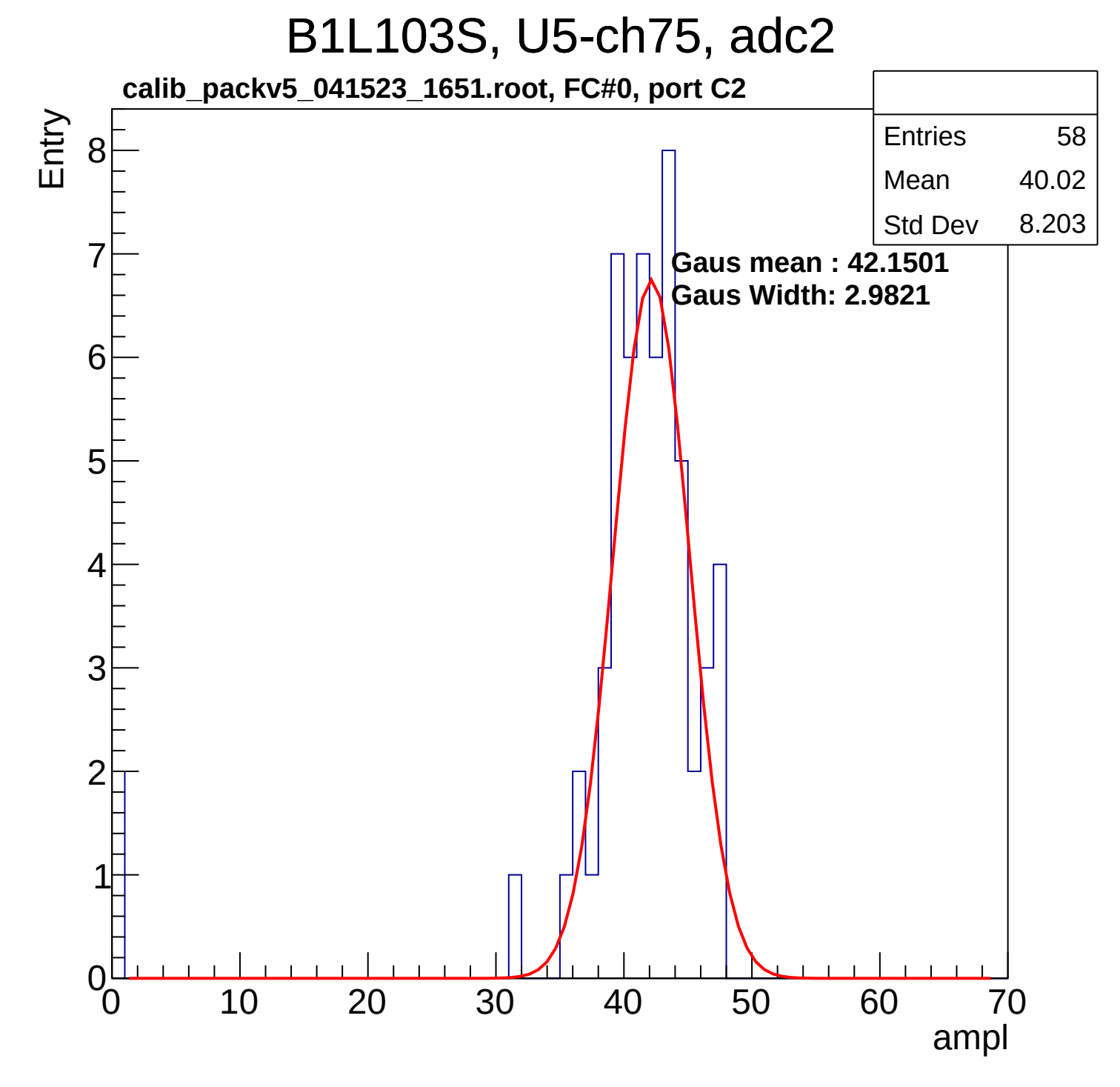
B1L103S, U5-ch75, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 40.02
Std Dev 8.203
Gaus mean : 42.1501
Gaus Width: 2.9821
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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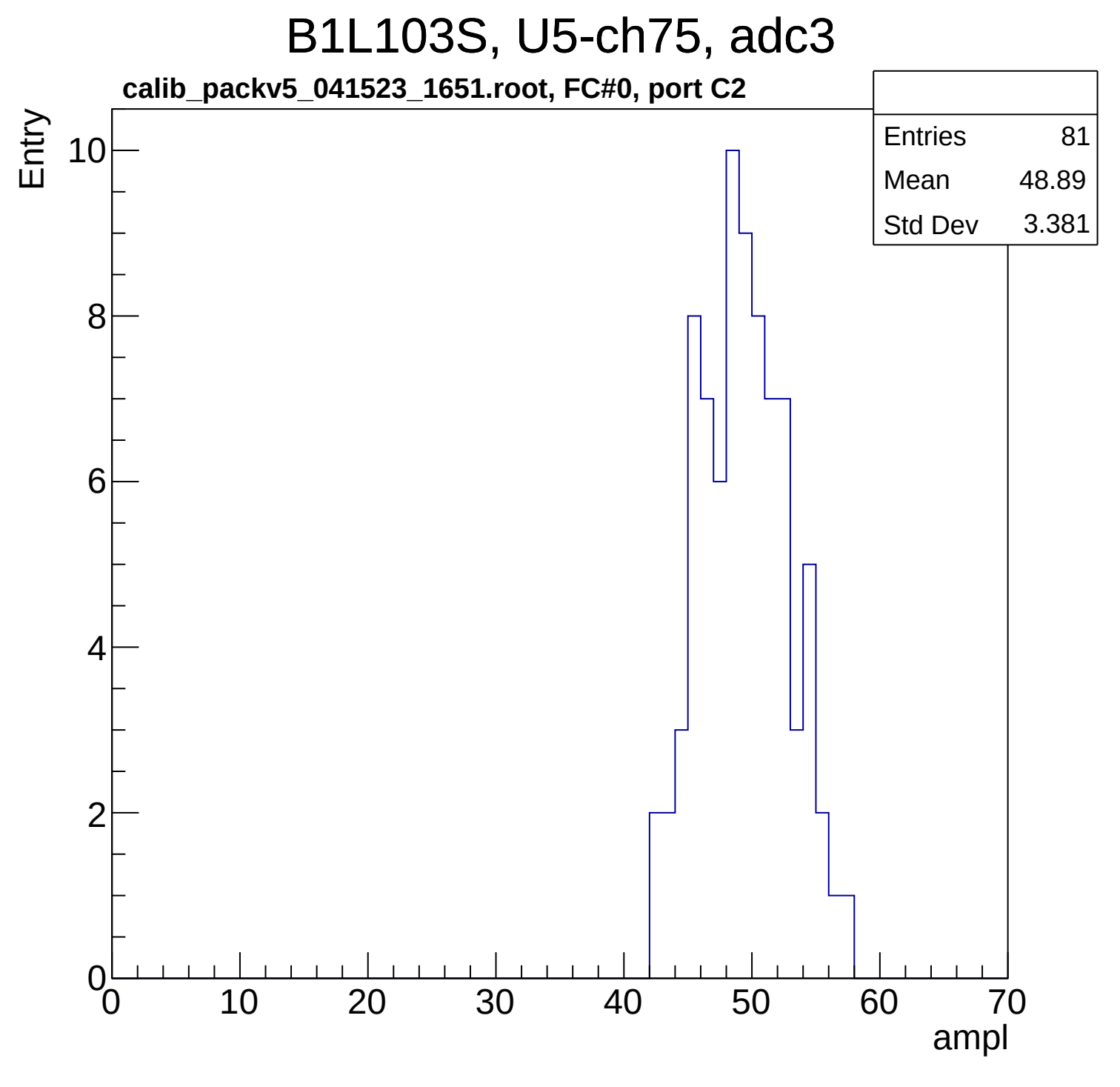
B1L103S, U5-ch75, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 48.89
Std Dev 3.381
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
50
60
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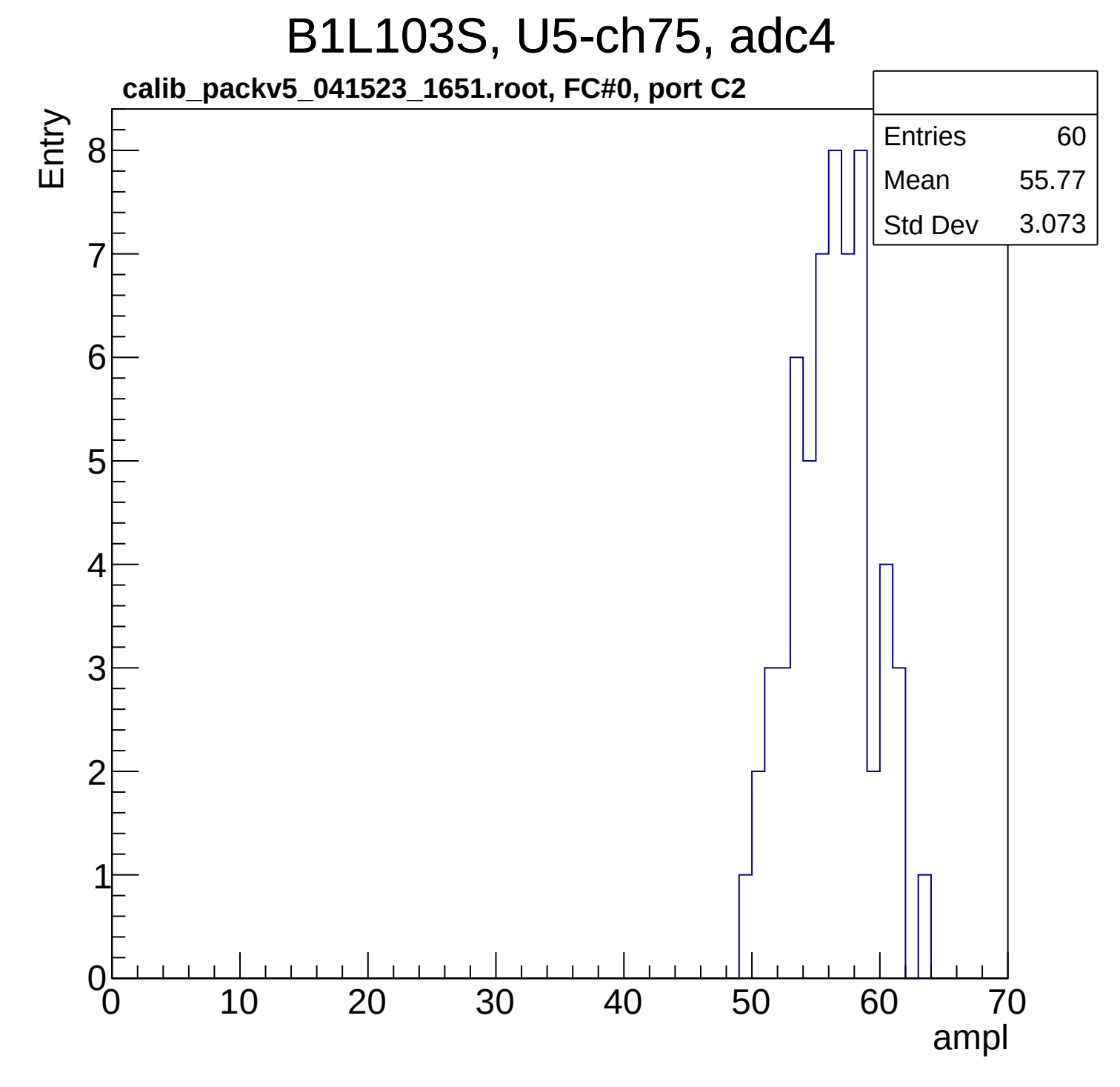
B1L103S, U5-ch75, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 55.77
Std Dev 3.073
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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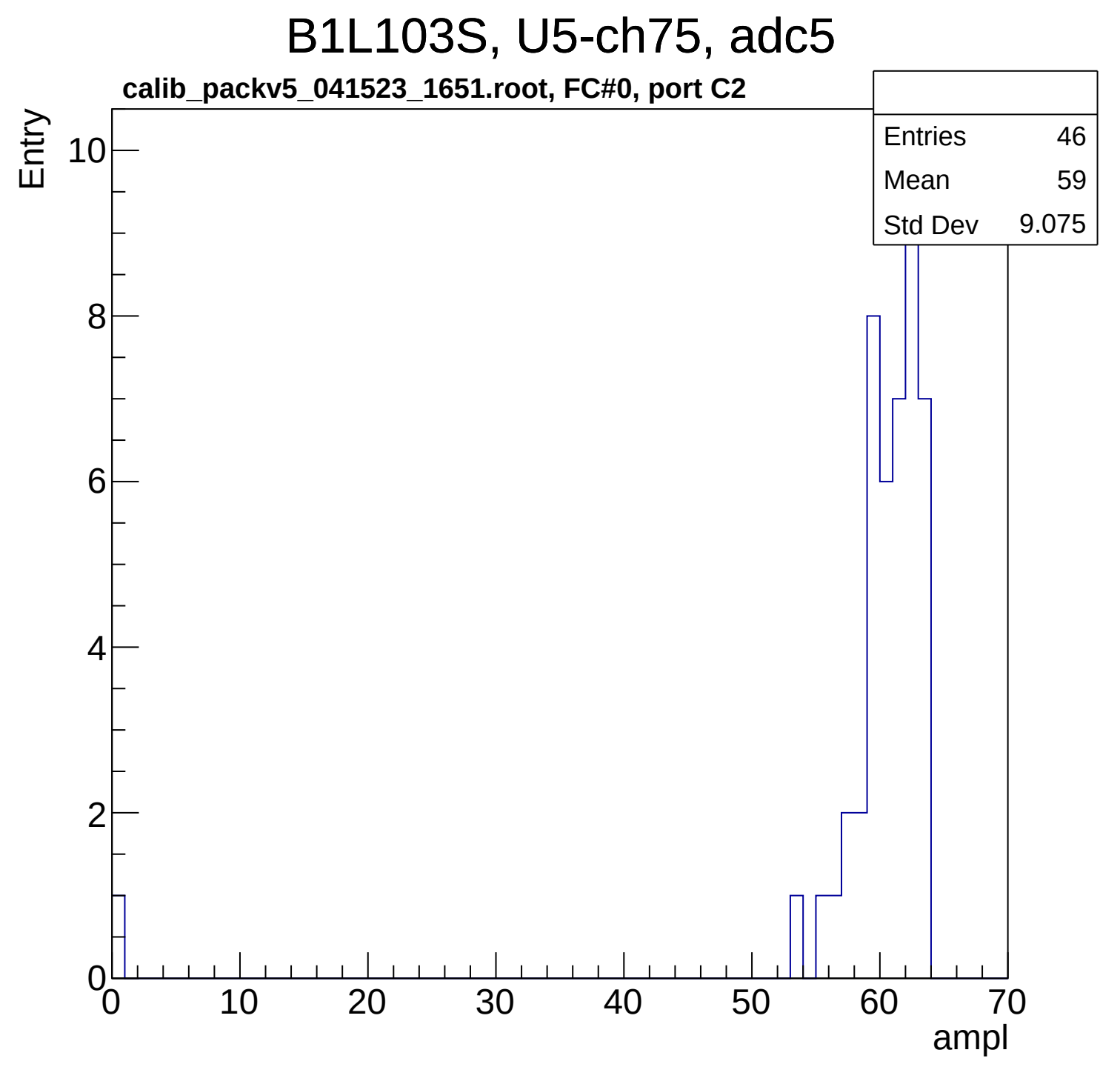
B1L103S, U5-ch75, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 59
Std Dev 9.075
Entry
ampl
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2
4
6
8
10
0
10
20
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40
50
60
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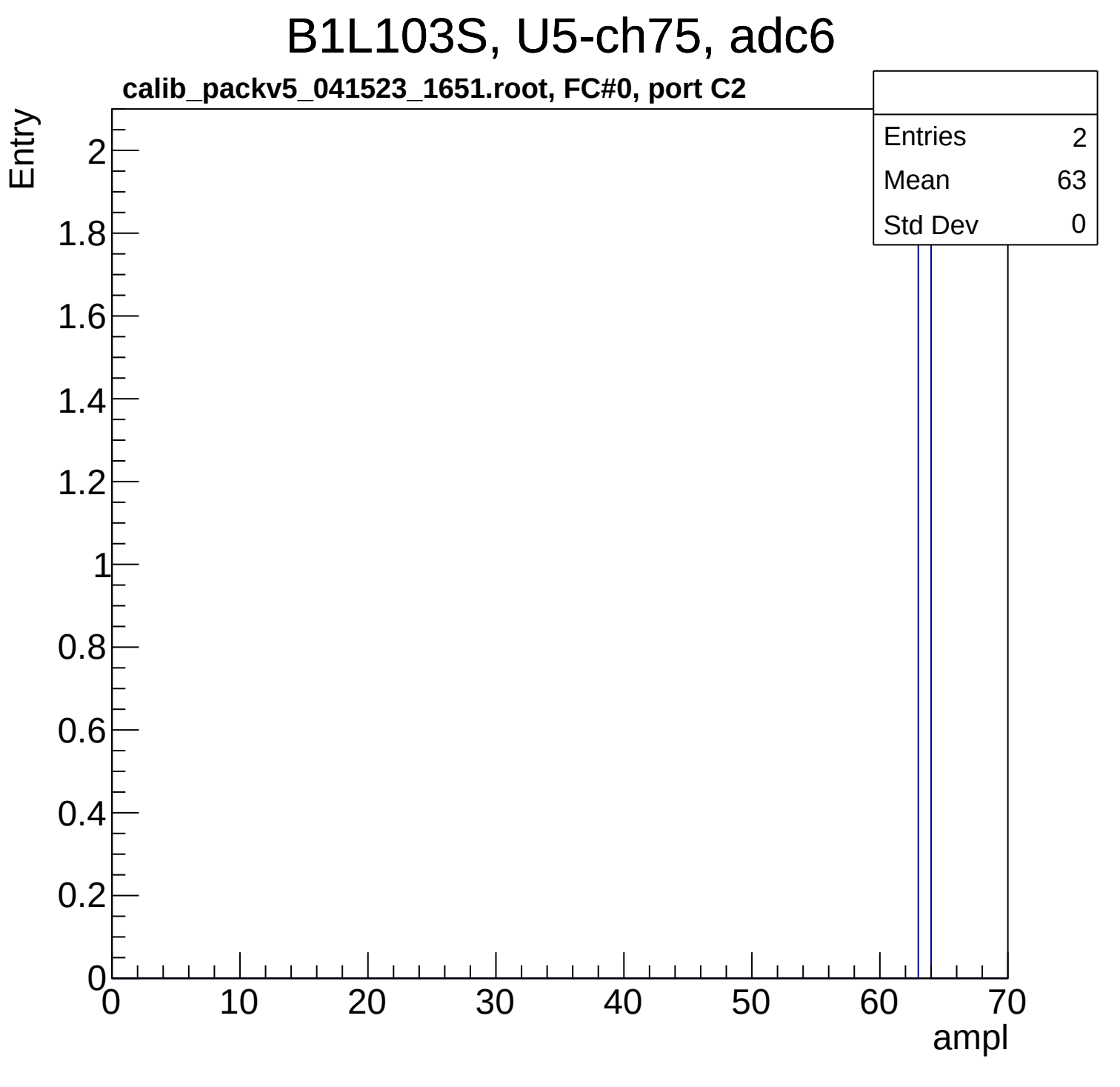
B1L103S, U5-ch75, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
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1.2
1.4
1.6
1.8
2
0
10
20
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40
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60
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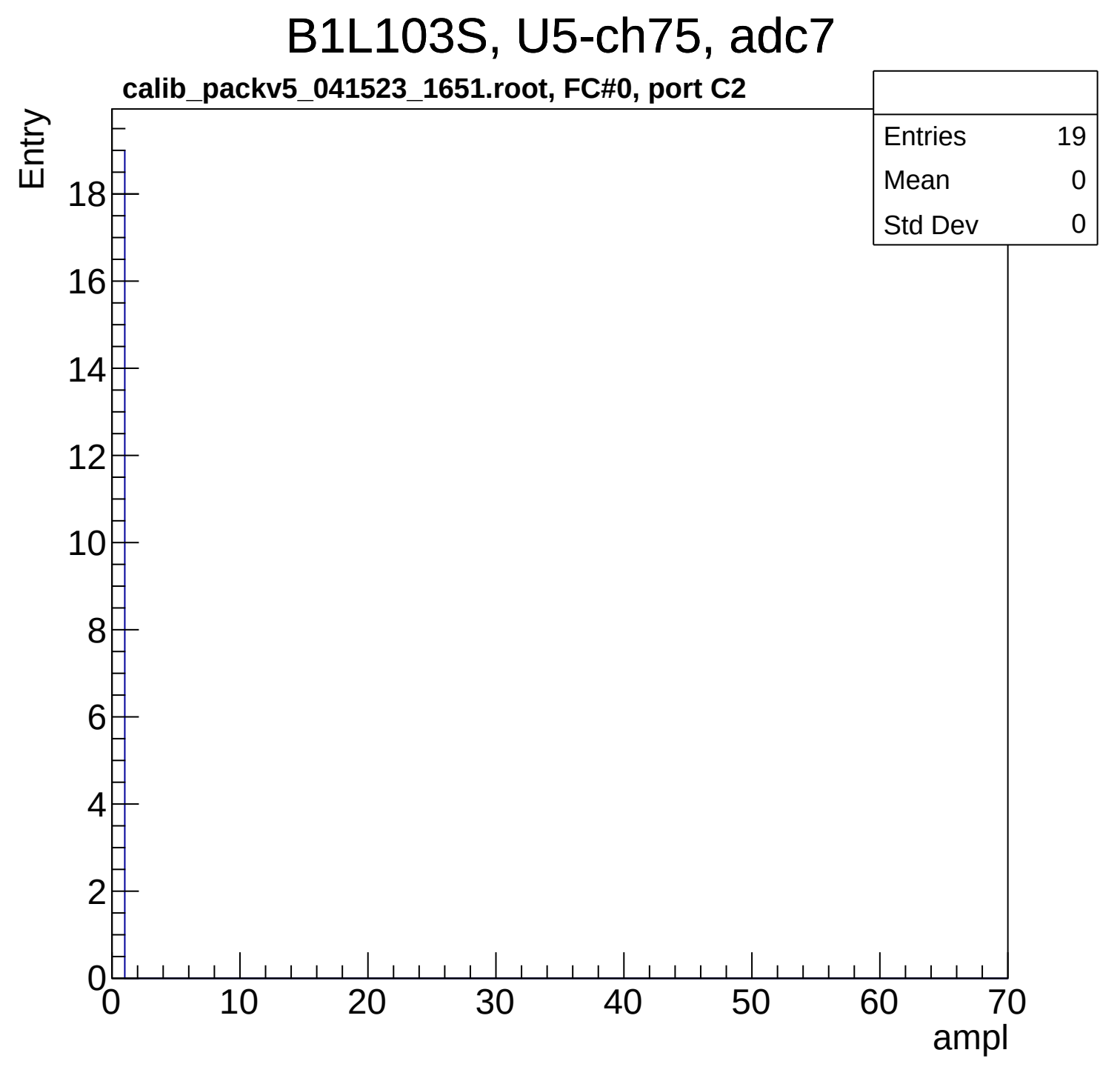
B1L103S, U5-ch75, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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8
10
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14
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18
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10
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30
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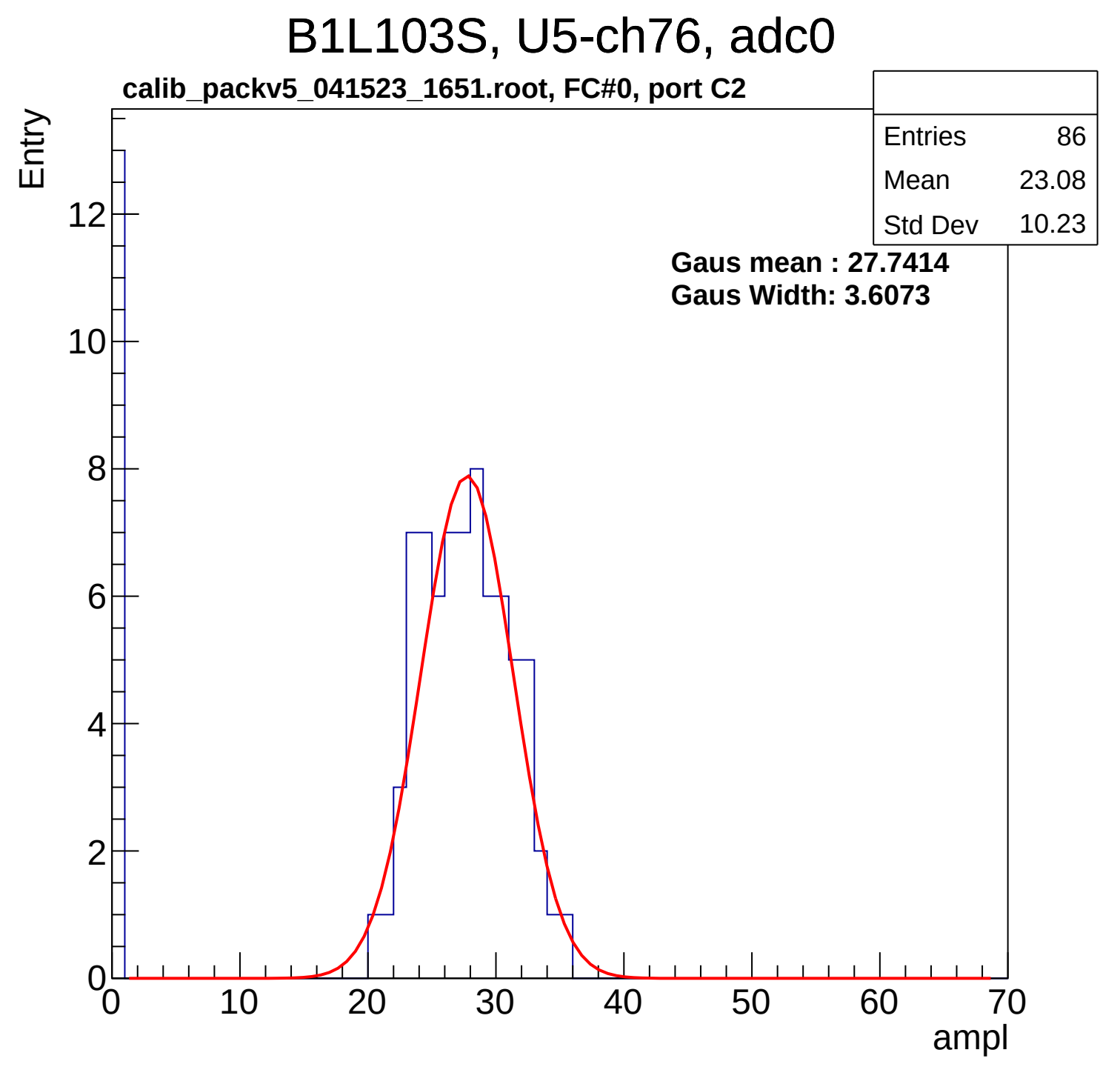
50
60
70
ampl


B1L103S, U5-ch76, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 23.08
Std Dev 10.23
Gaus mean : 27.7414
Gaus Width: 3.6073
Entry
ampl
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6
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0
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20
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40
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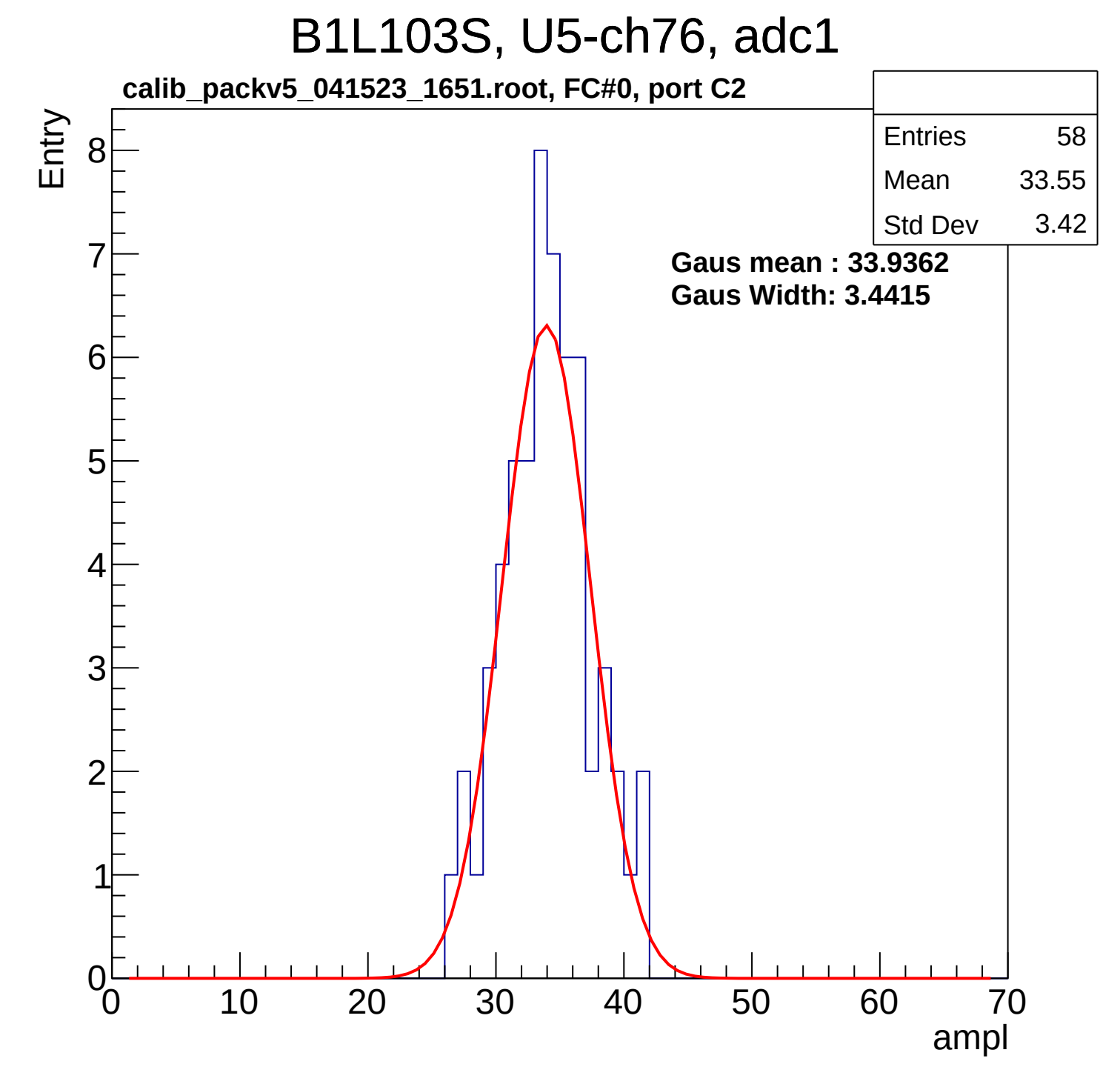
B1L103S, U5-ch76, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 33.55
Std Dev 3.42
Gaus mean : 33.9362
Gaus Width: 3.4415
Entry
ampl
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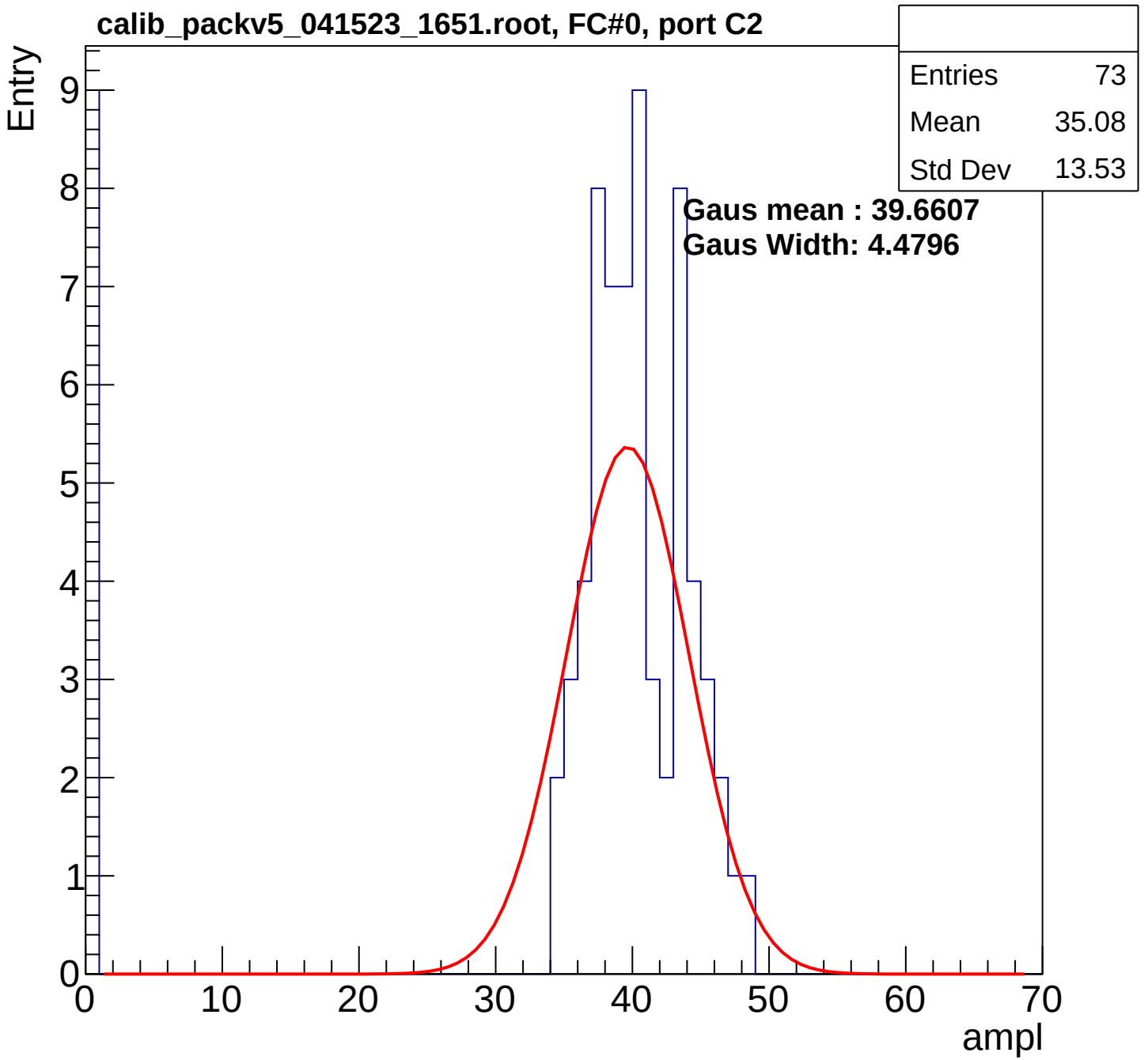
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U5-ch76, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 35.08
Std Dev 13.53
Gaus mean : 39.6607
Gaus Width: 4.4796
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
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60
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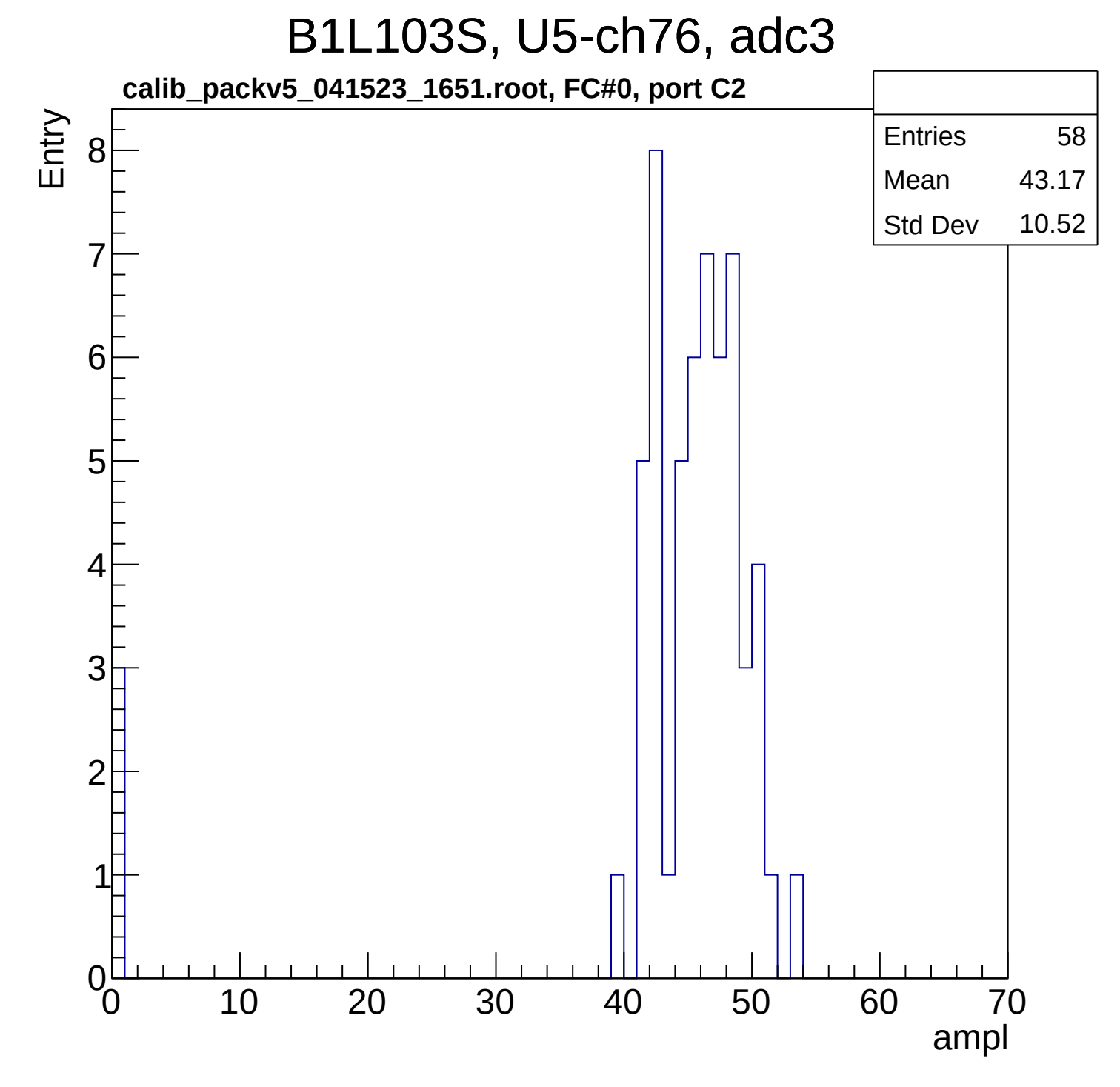
B1L103S, U5-ch76, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 43.17
Std Dev 10.52
Entry
ampl
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1
2
3
4
5
6
7
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10
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40
50
60
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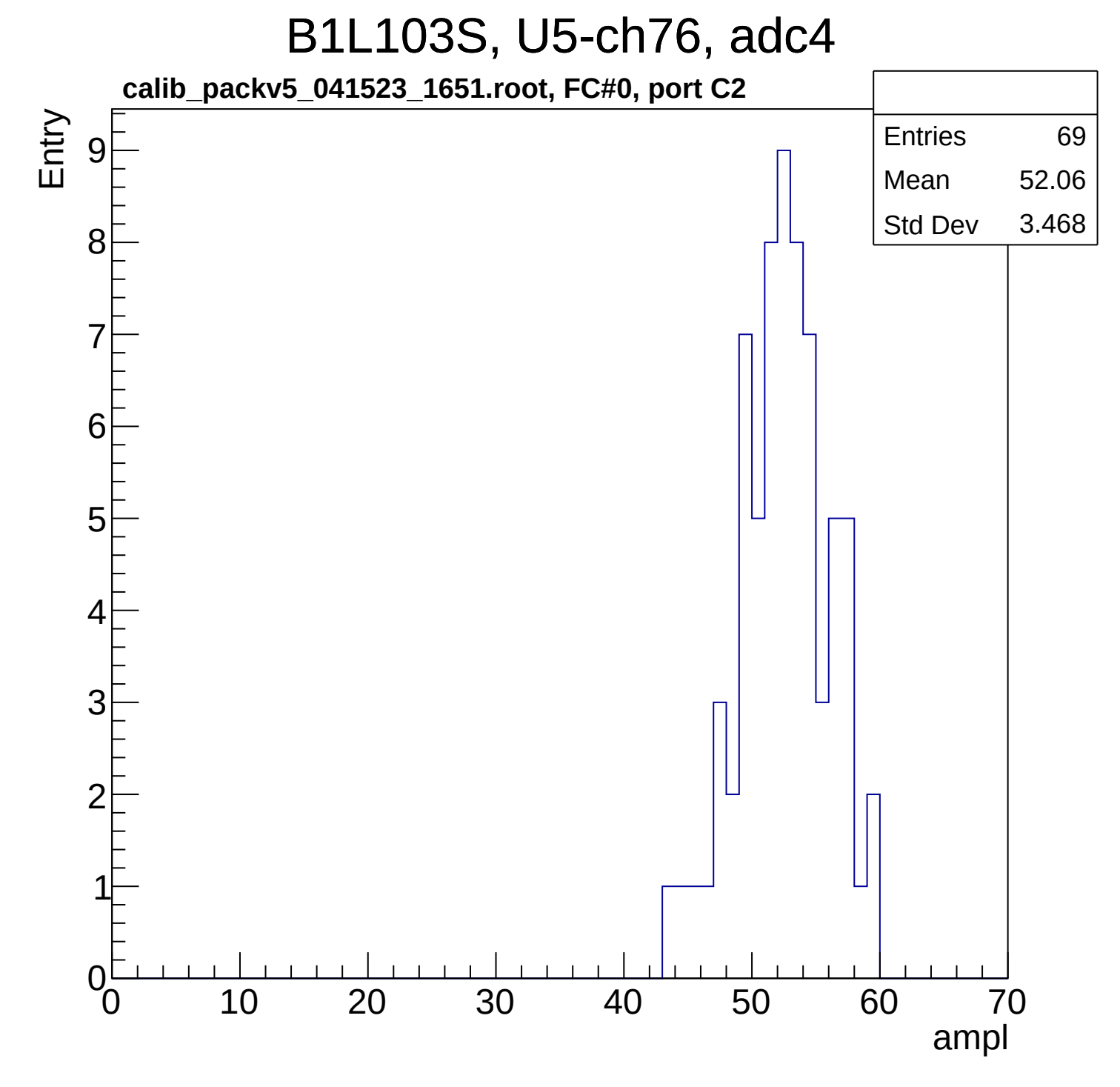
B1L103S, U5-ch76, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 52.06
Std Dev 3.468
Entry
ampl
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3
4
5
6
7
8
9
0
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40
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60
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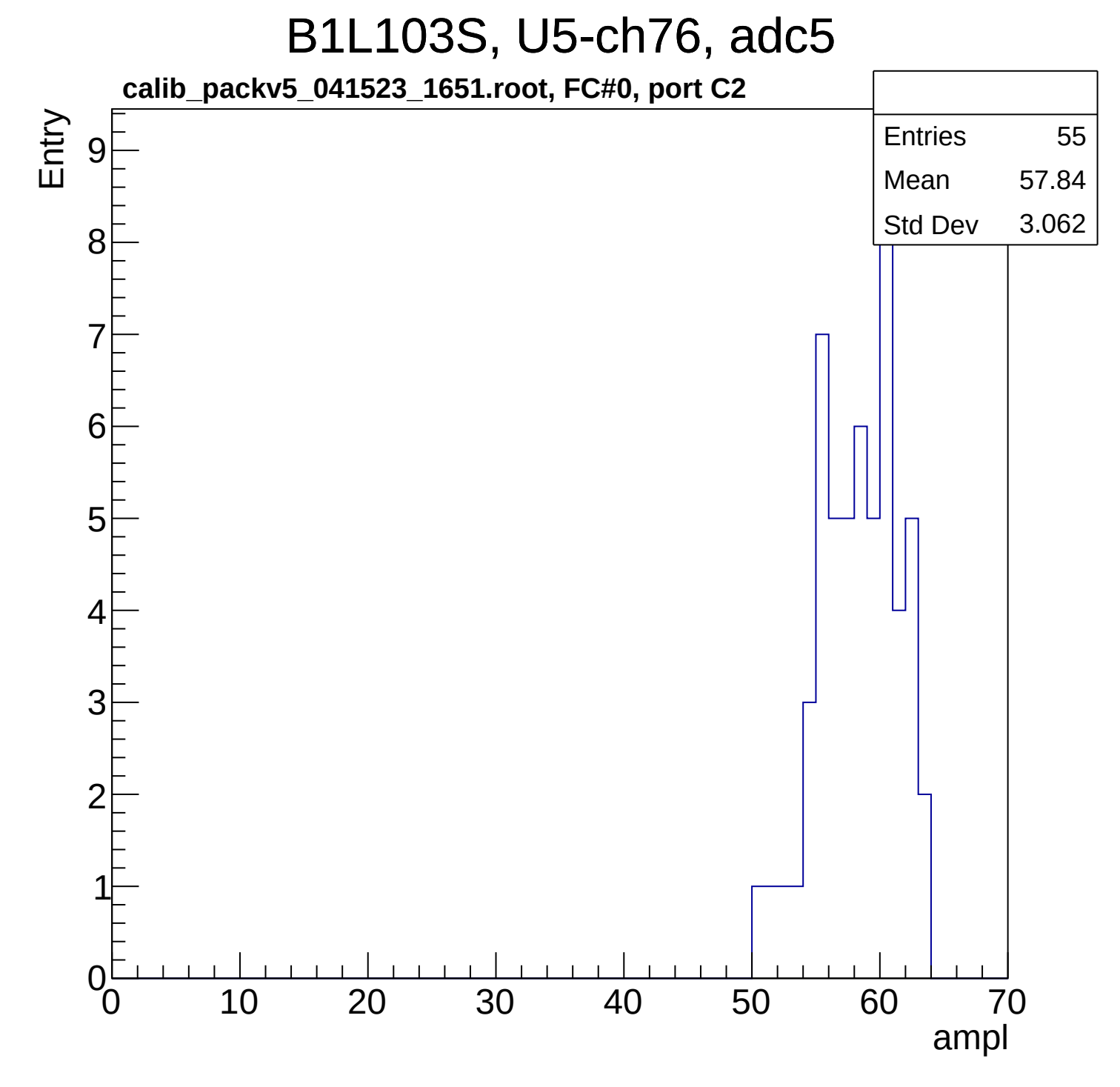
B1L103S, U5-ch76, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.84
Std Dev 3.062
Entry
ampl
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3
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0
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60
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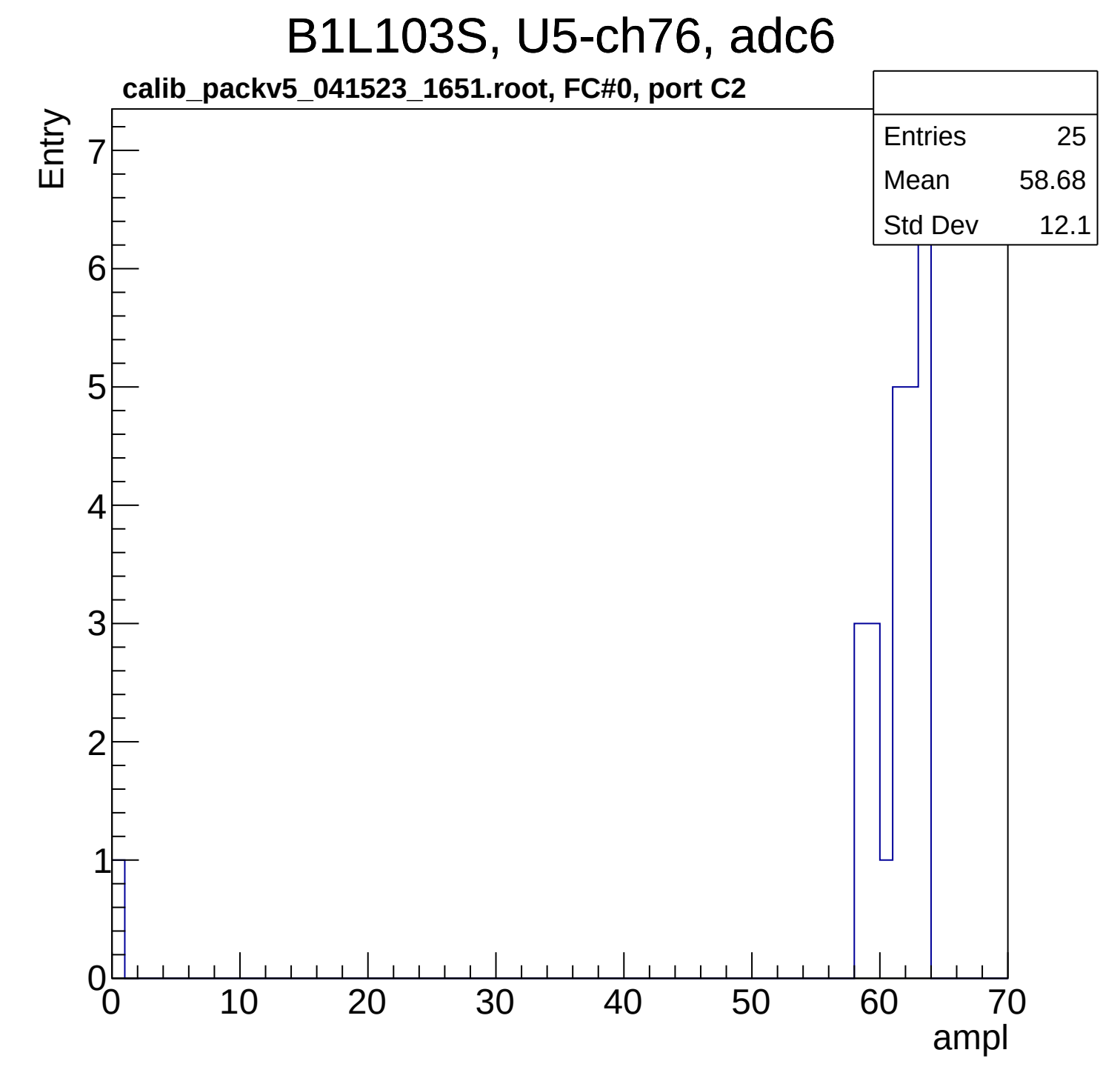
B1L103S, U5-ch76, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 58.68
Std Dev 12.1
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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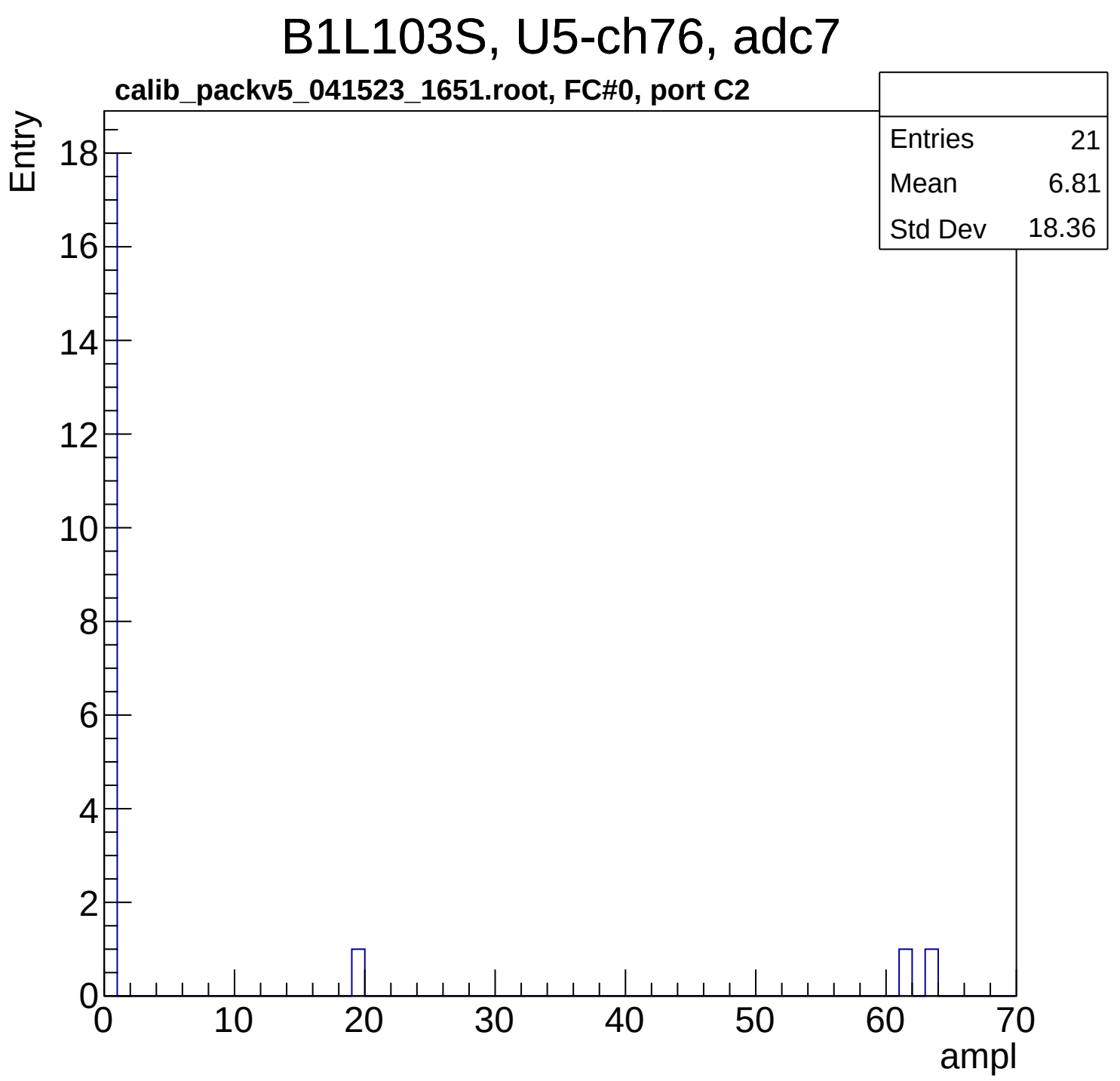
B1L103S, U5-ch76, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6.81
Std Dev 18.36
Entry
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6
8
10
12
14
16
18
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10
20
30
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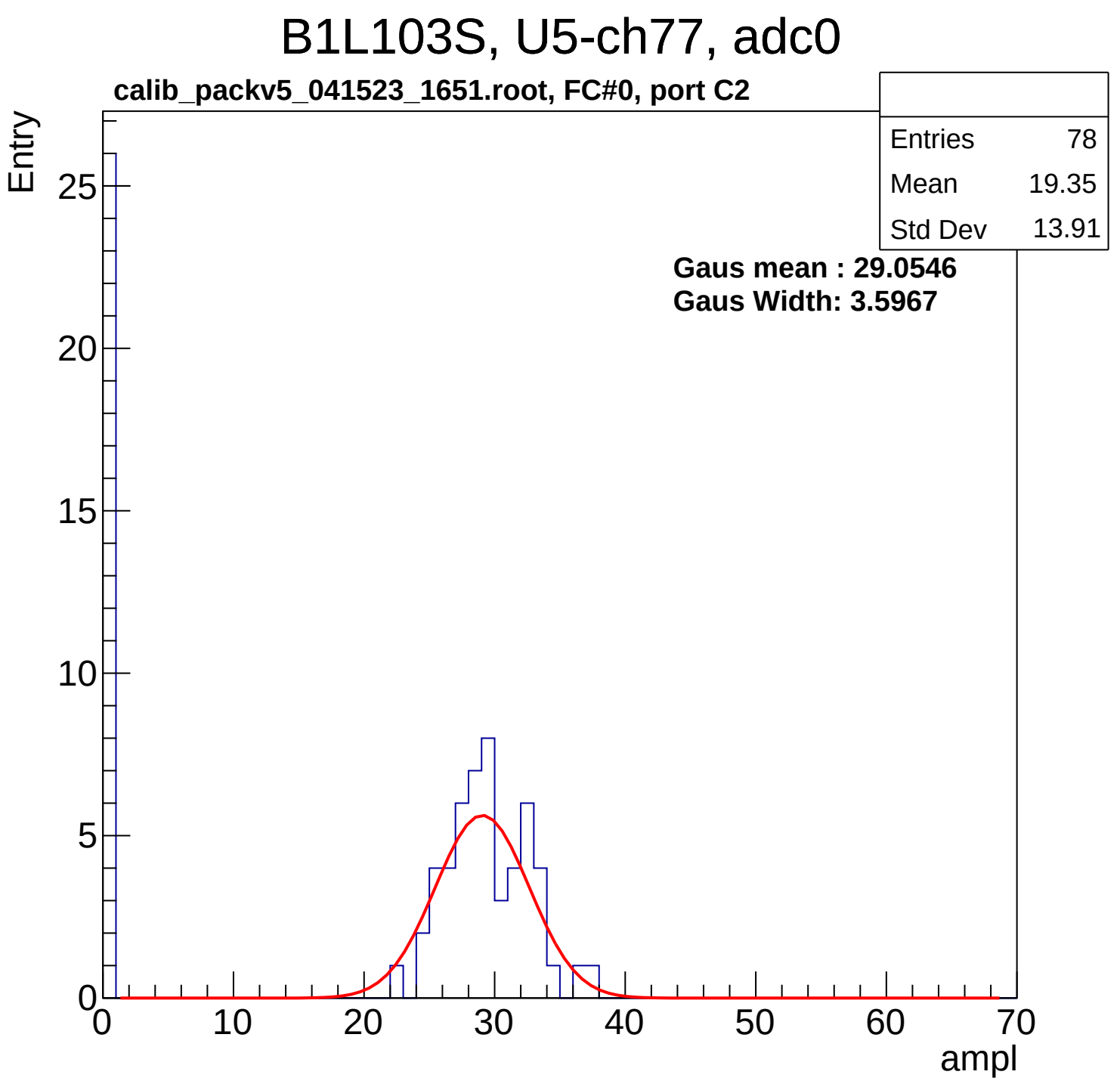
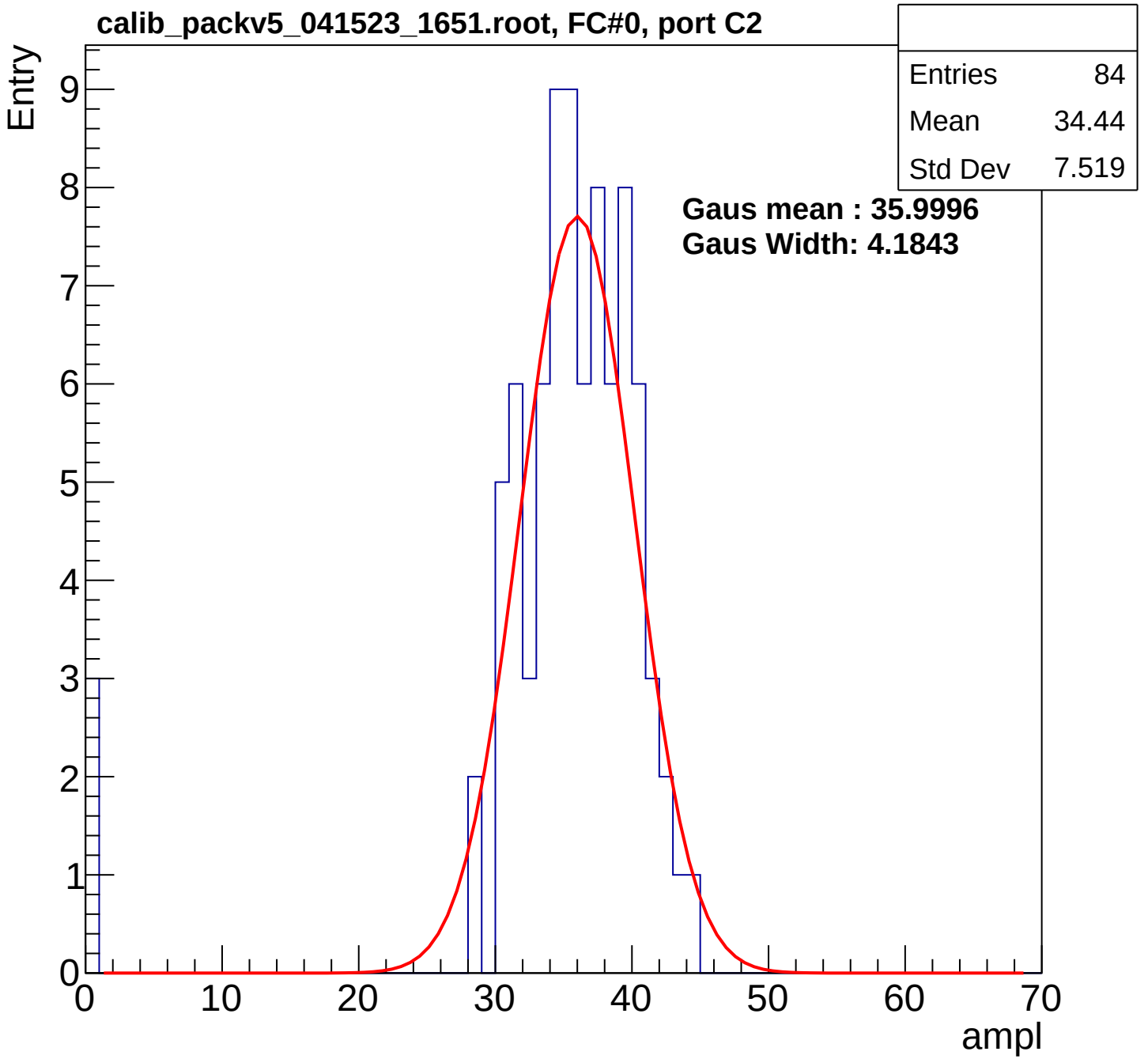
50
60
70
ampl


B1L103S, U5-ch77, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 19.35
Std Dev 13.91
Gaus mean : 29.0546
Gaus Width: 3.5967
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U5-ch77, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 34.44
Std Dev 7.519
Gaus mean : 35.9996
Gaus Width: 4.1843
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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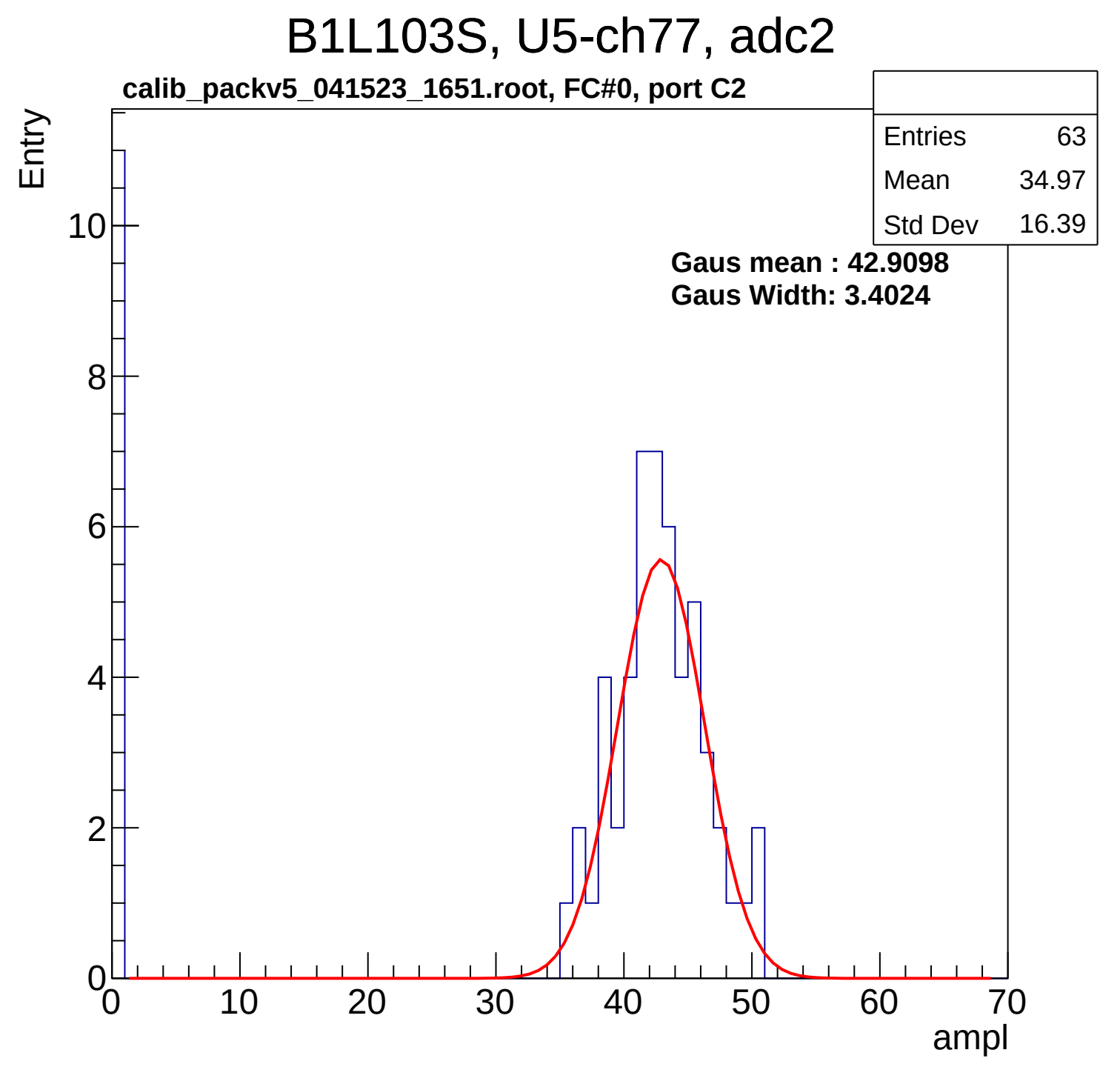
B1L103S, U5-ch77, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 34.97
Std Dev 16.39
Gaus mean : 42.9098
Gaus Width: 3.4024
Entry
ampl
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30
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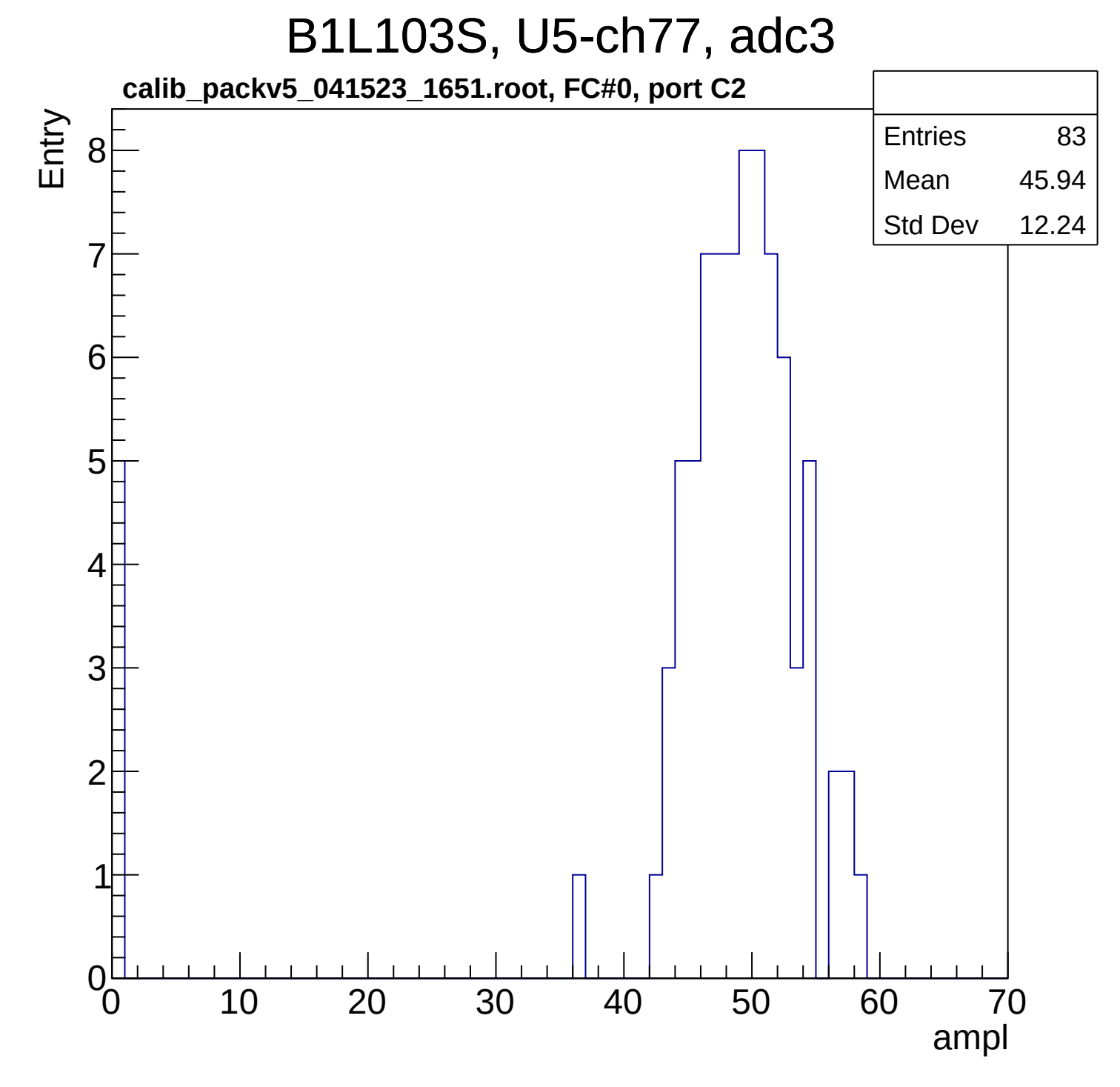
B1L103S, U5-ch77, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 45.94
Std Dev 12.24
Entry
ampl
0
1
2
3
4
5
6
7
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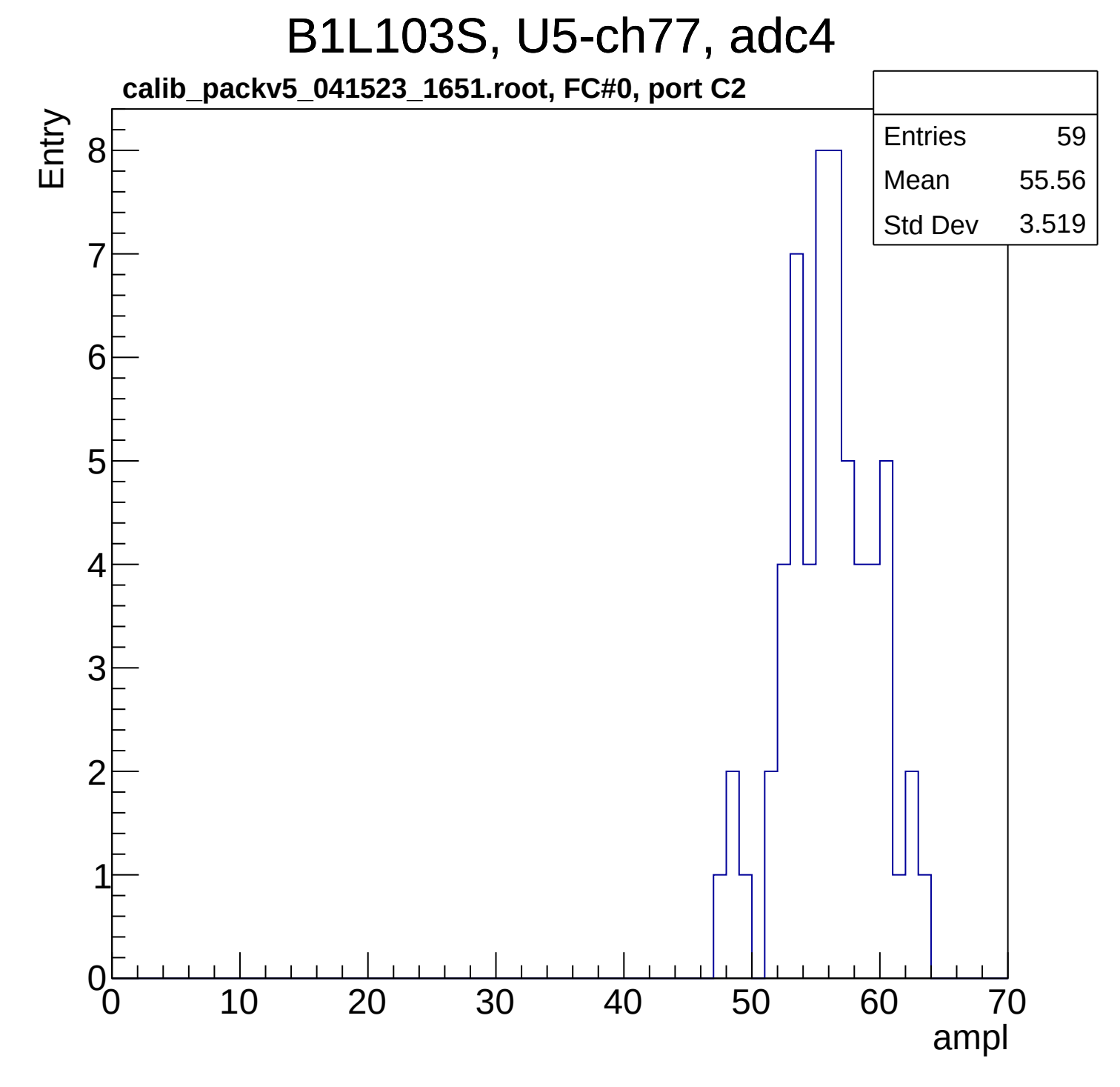
B1L103S, U5-ch77, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 55.56
Std Dev 3.519
Entry
ampl
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1
2
3
4
5
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60
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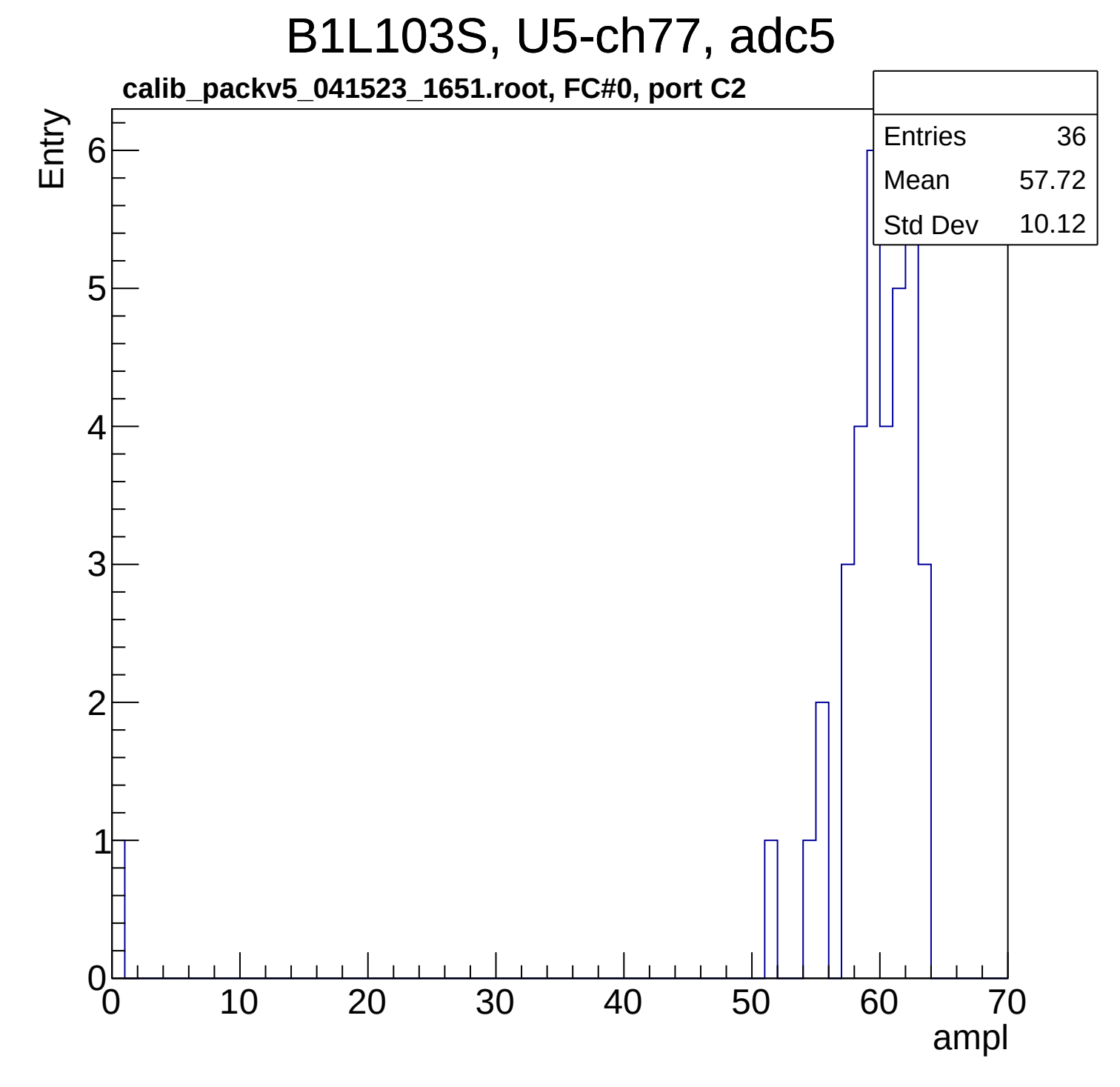
B1L103S, U5-ch77, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 57.72
Std Dev 10.12
Entry
ampl
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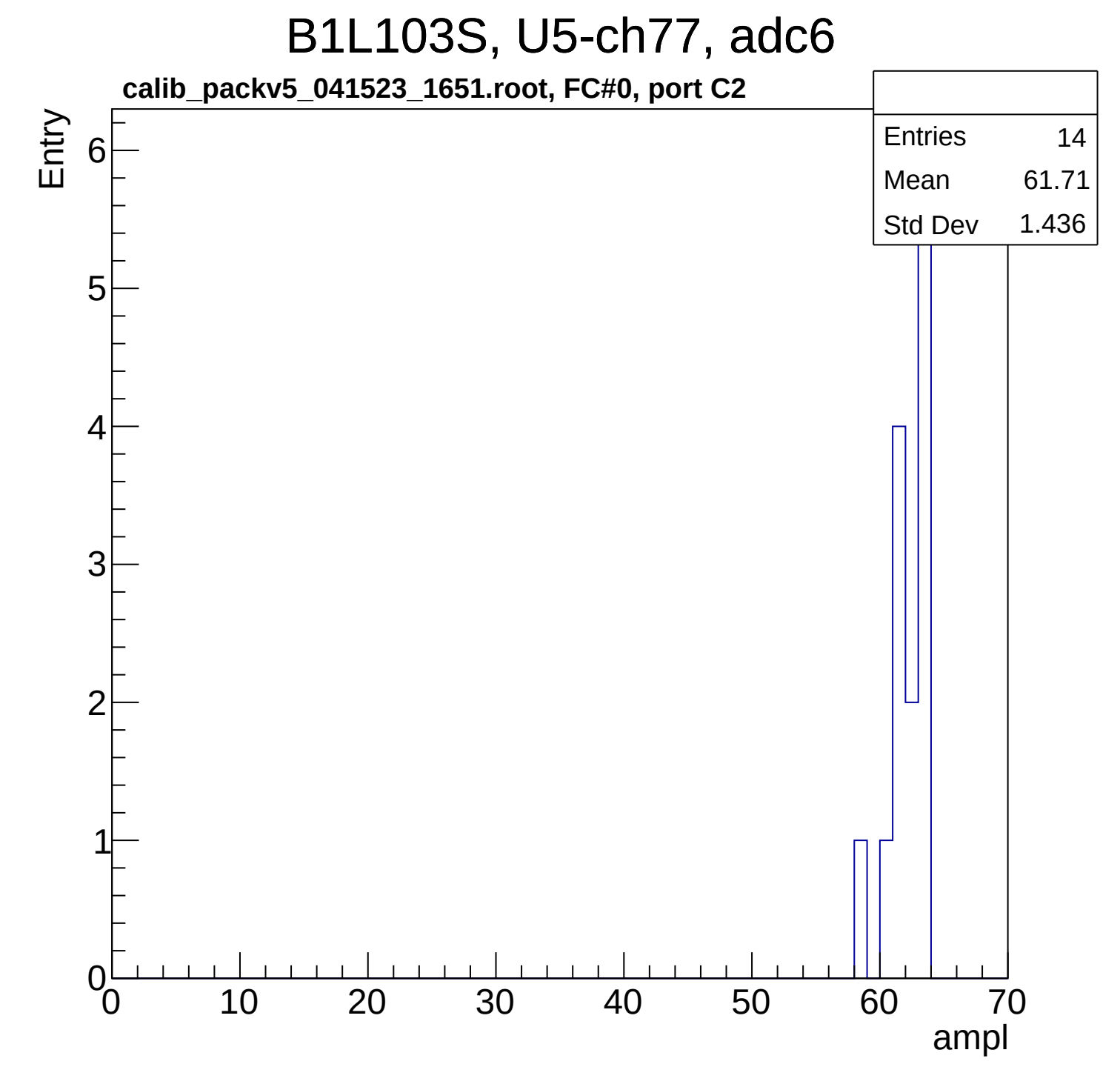
B1L103S, U5-ch77, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.71
Std Dev 1.436
Entry
ampl
0
1
2
3
4
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0
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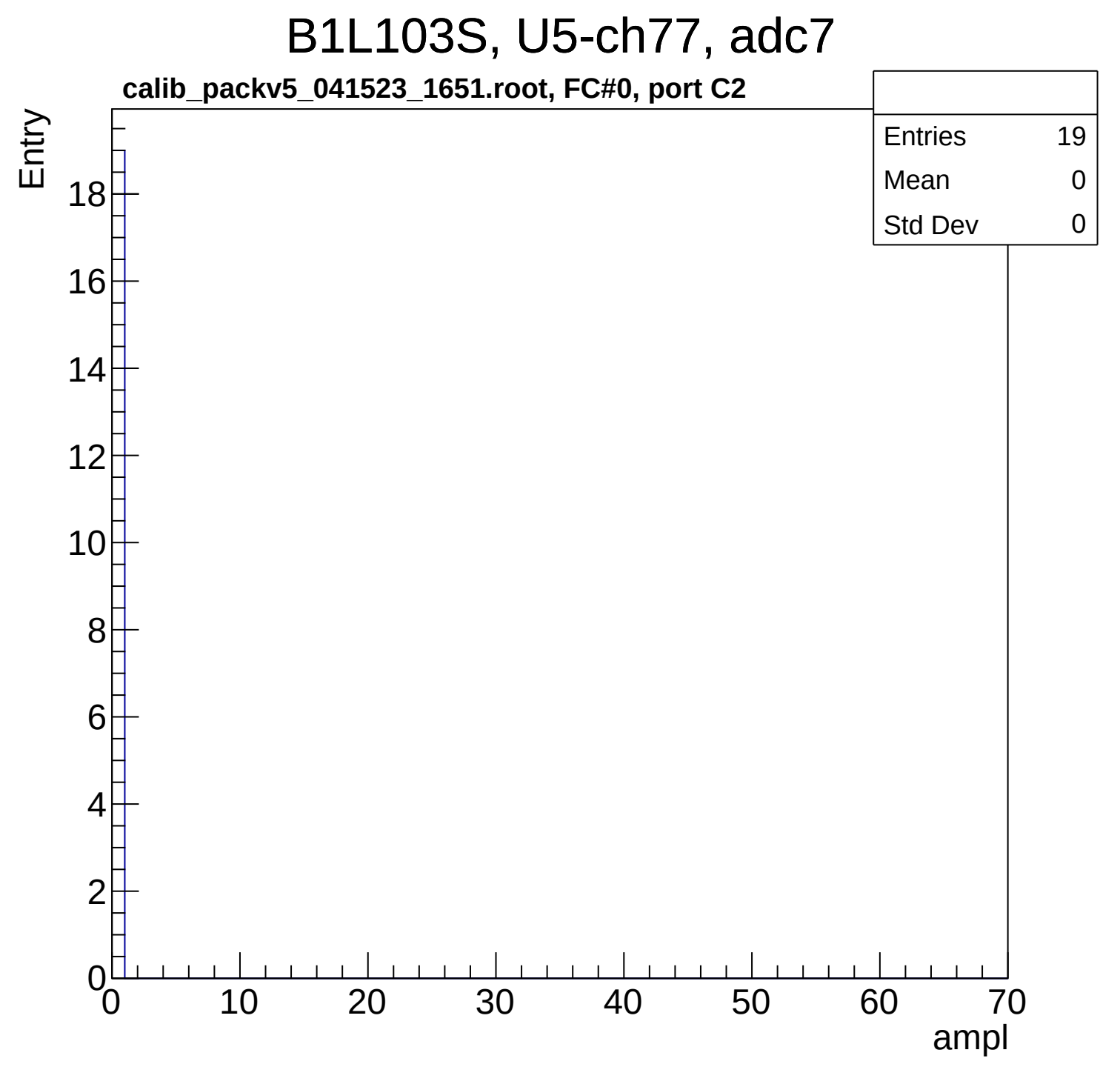
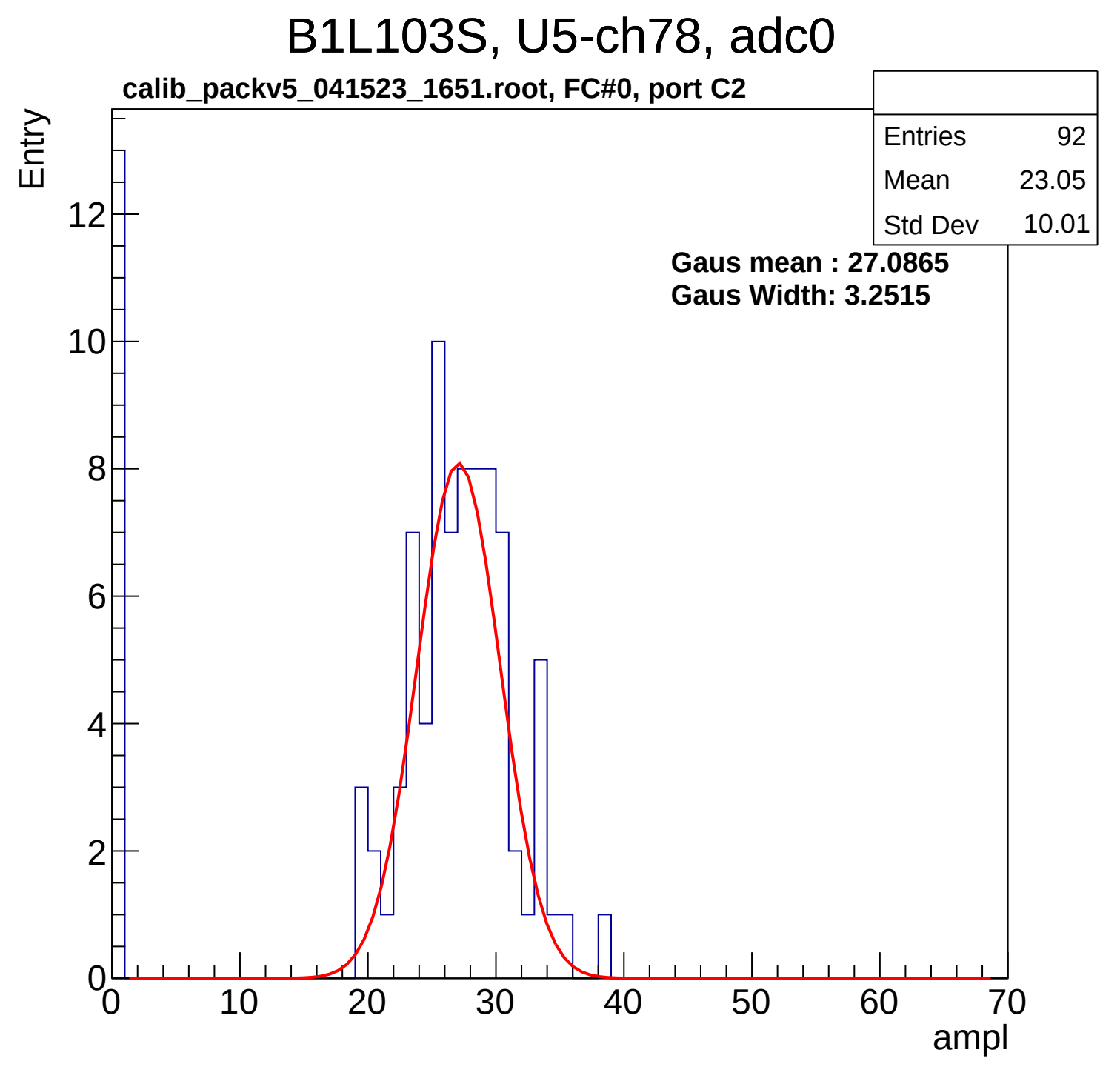

B1L103S, U5-ch77, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch78, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 23.05
Std Dev 10.01
Gaus mean : 27.0865
Gaus Width: 3.2515
Entry
ampl
0
2
4
6
8
10
12
0
10
20
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40
50
60
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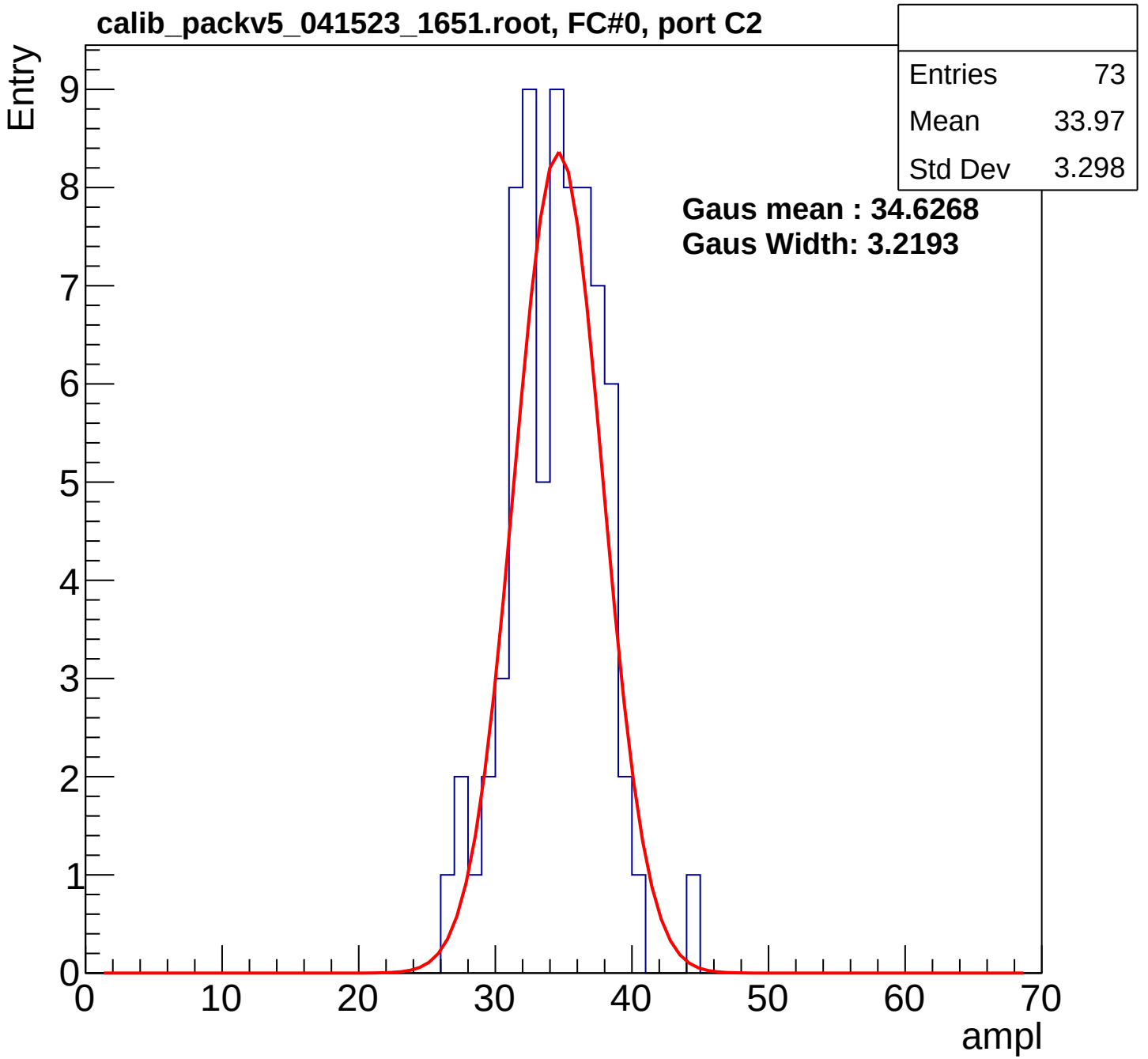
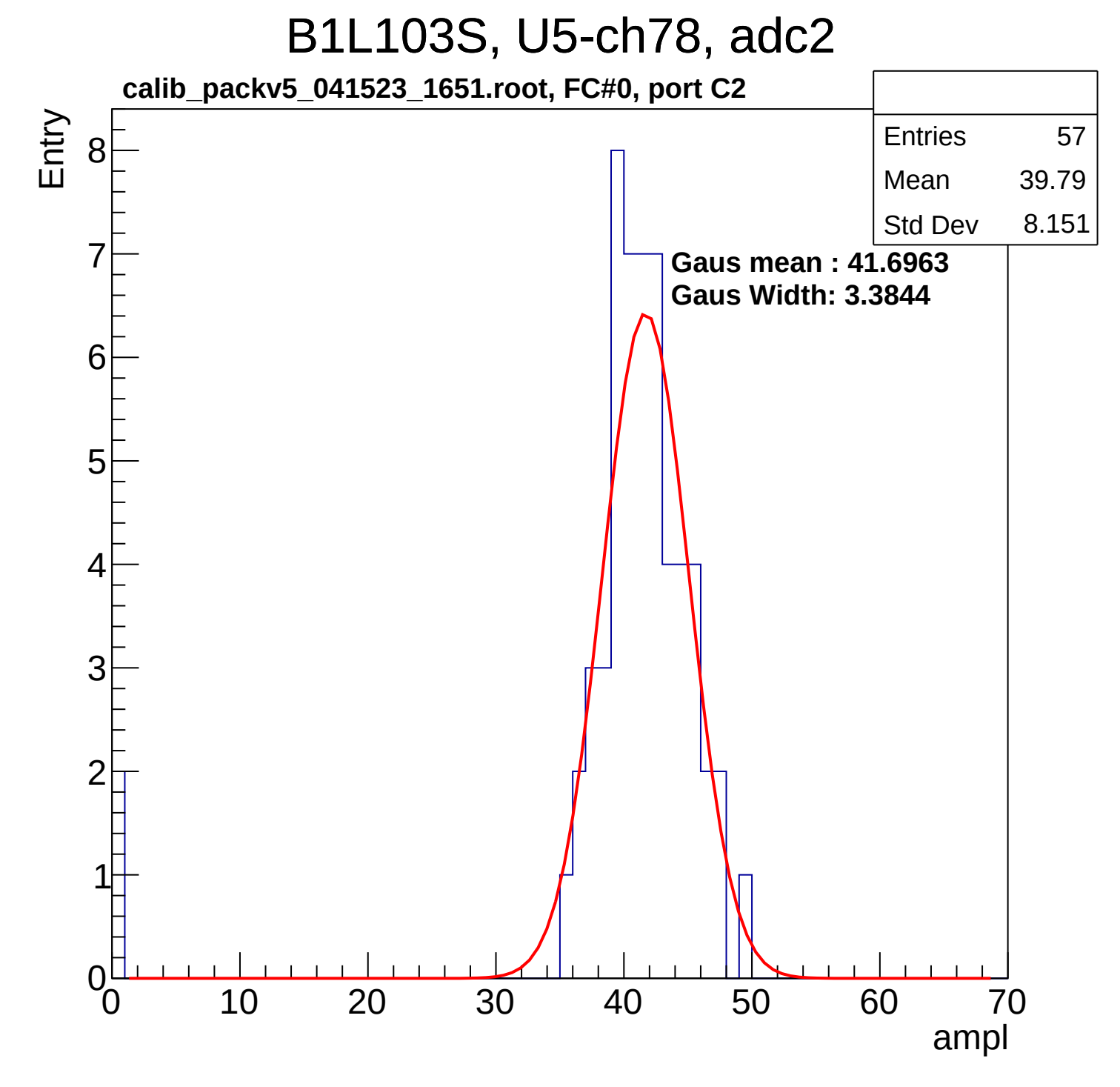

B1L103S, U5-ch78, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 33.97
Std Dev 3.298
Gaus mean : 34.6268
Gaus Width: 3.2193
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U5-ch78, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 39.79
Std Dev 8.151
Gaus mean : 41.6963
Gaus Width: 3.3844
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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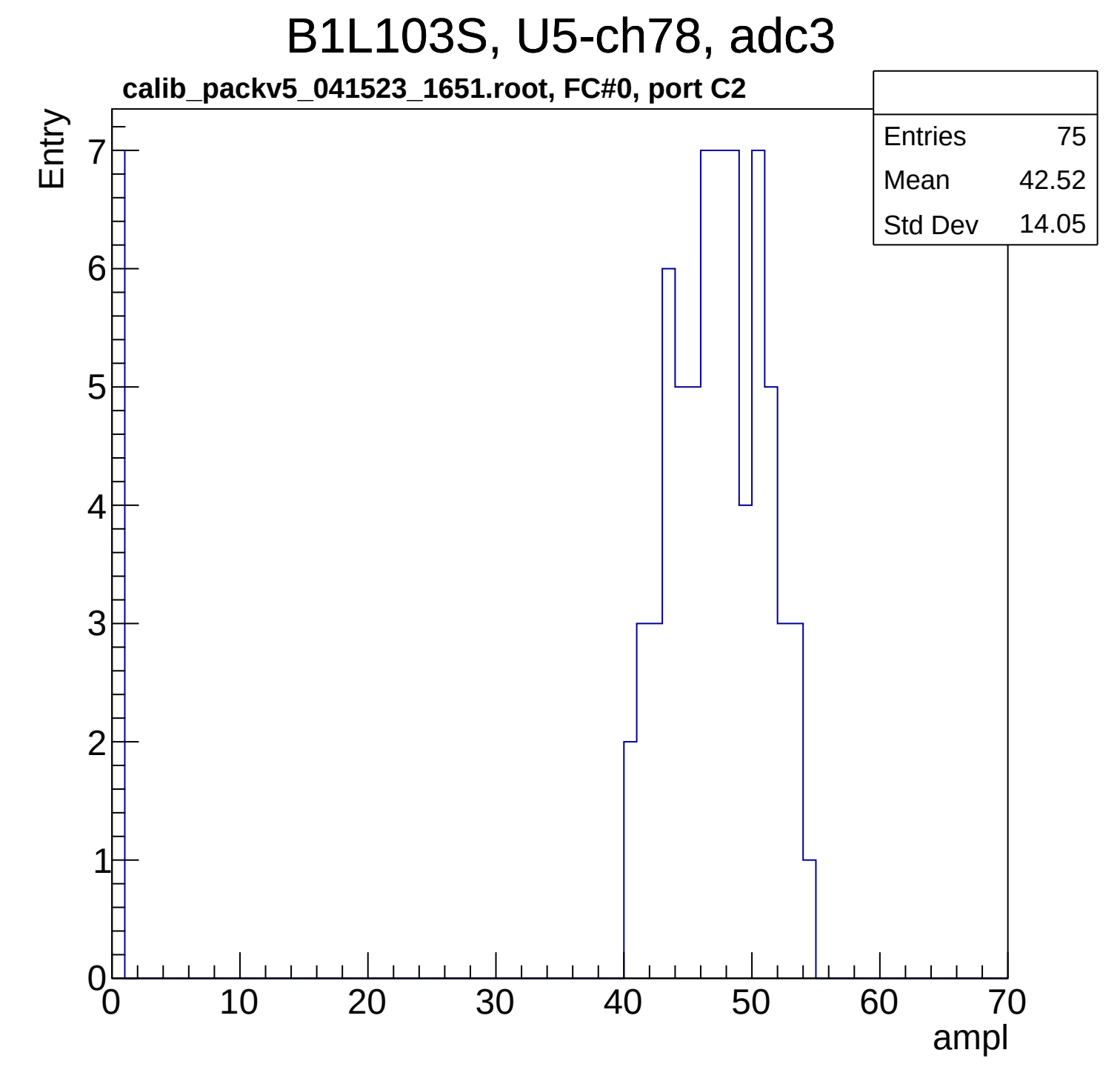
B1L103S, U5-ch78, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 42.52
Std Dev 14.05
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
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60
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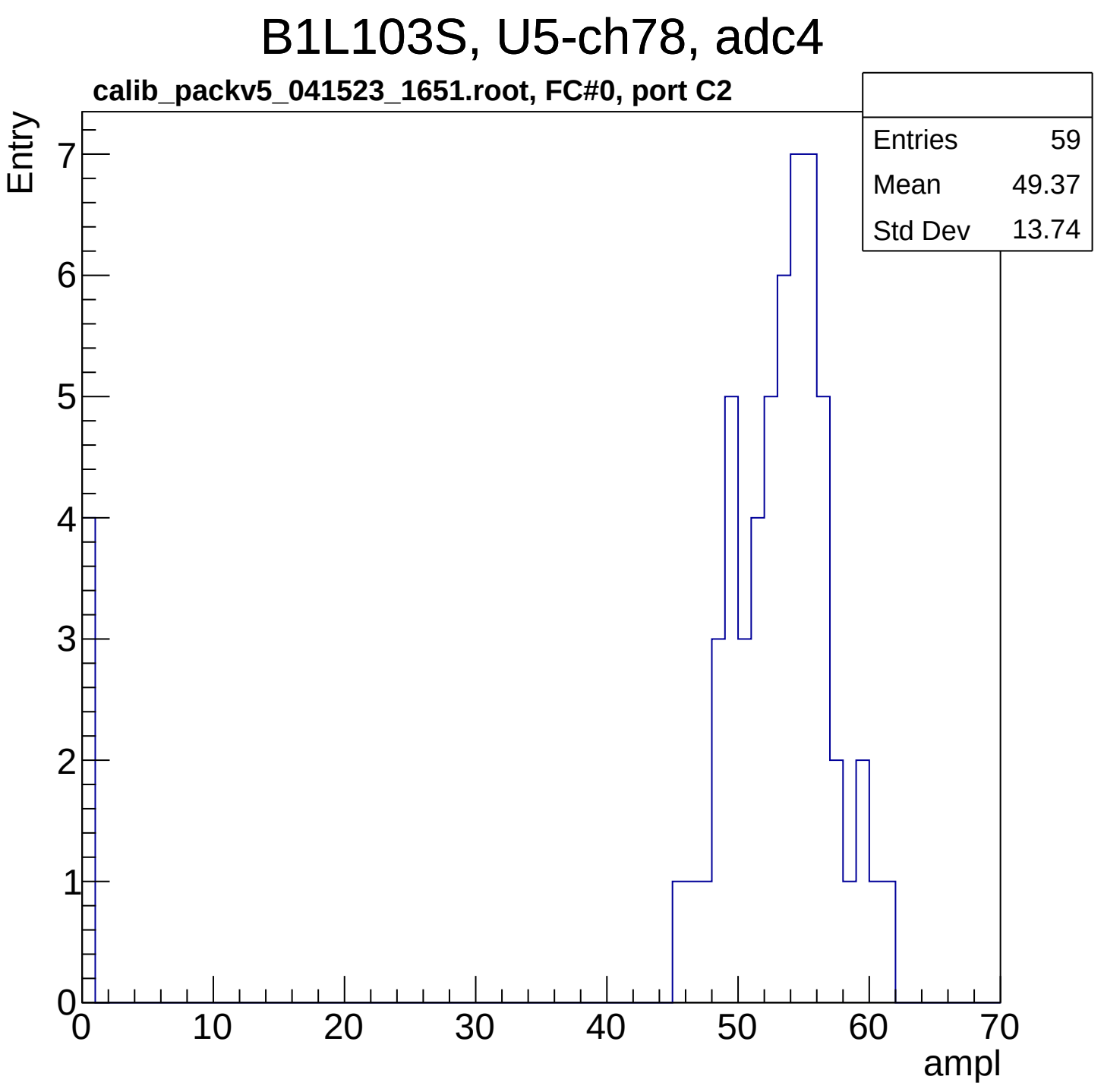
B1L103S, U5-ch78, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 49.37
Std Dev 13.74
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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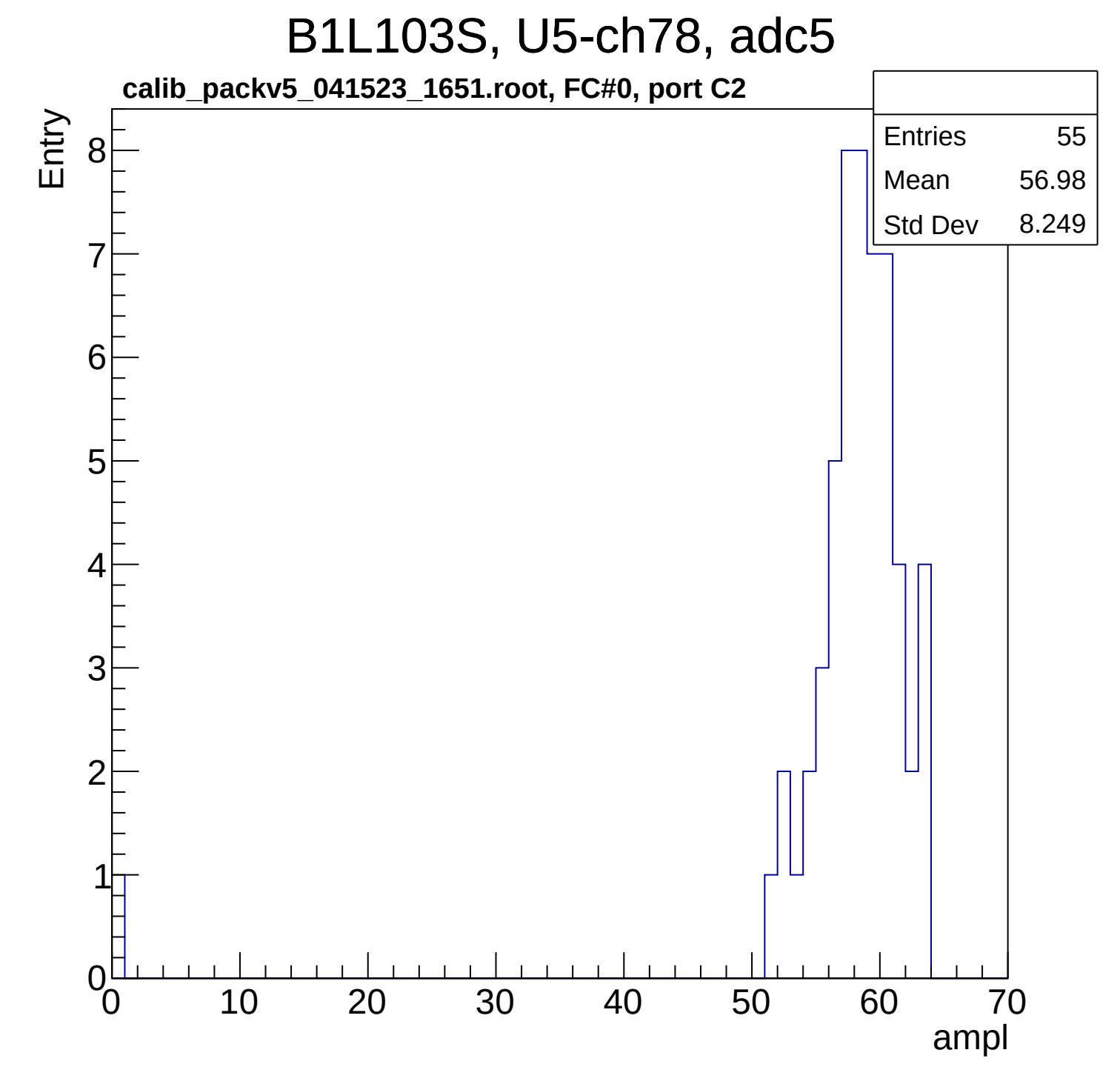
B1L103S, U5-ch78, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 56.98
Std Dev 8.249
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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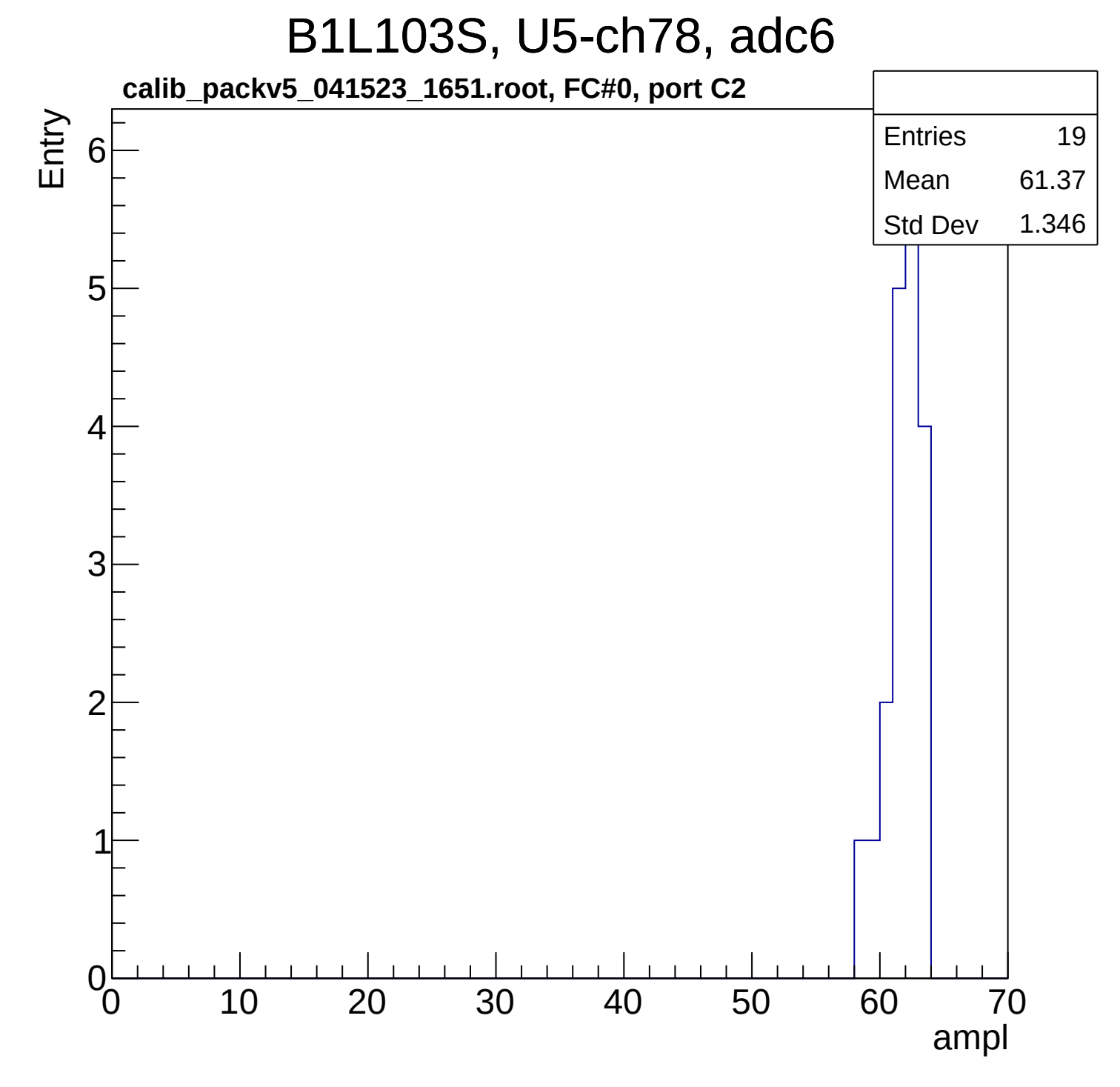
B1L103S, U5-ch78, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 61.37
Std Dev 1.346
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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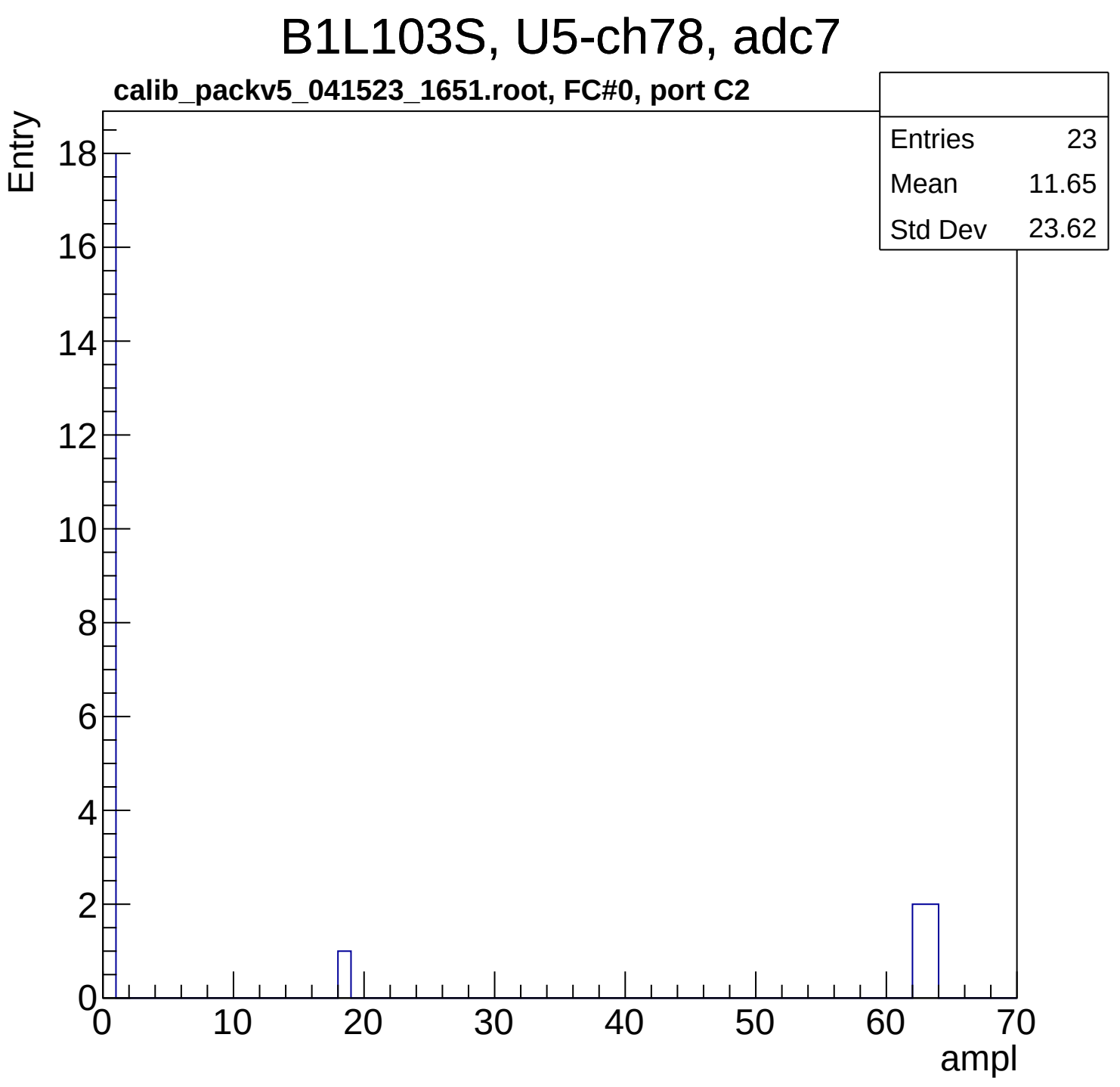
B1L103S, U5-ch78, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 11.65
Std Dev 23.62
Entry
0
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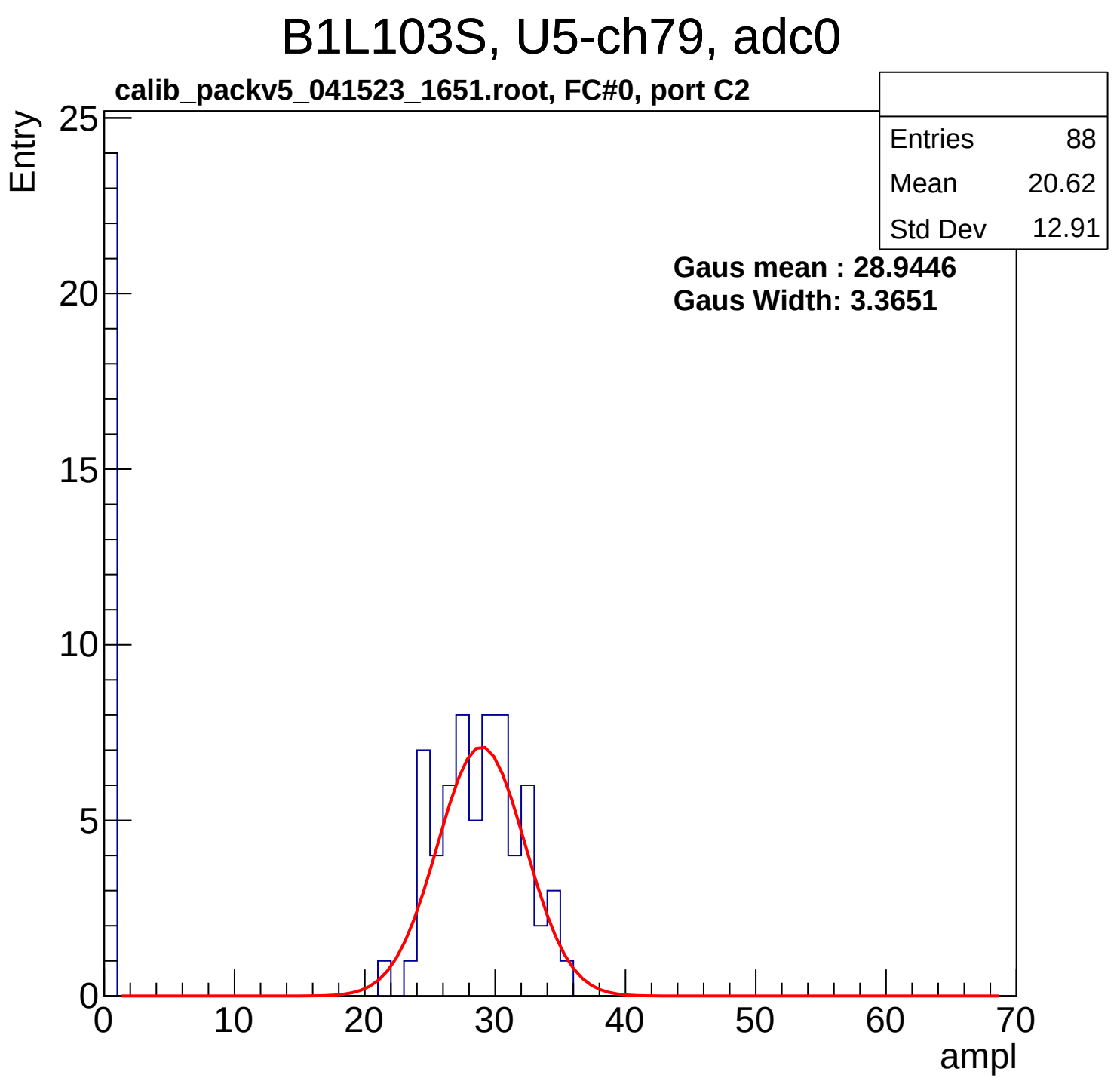
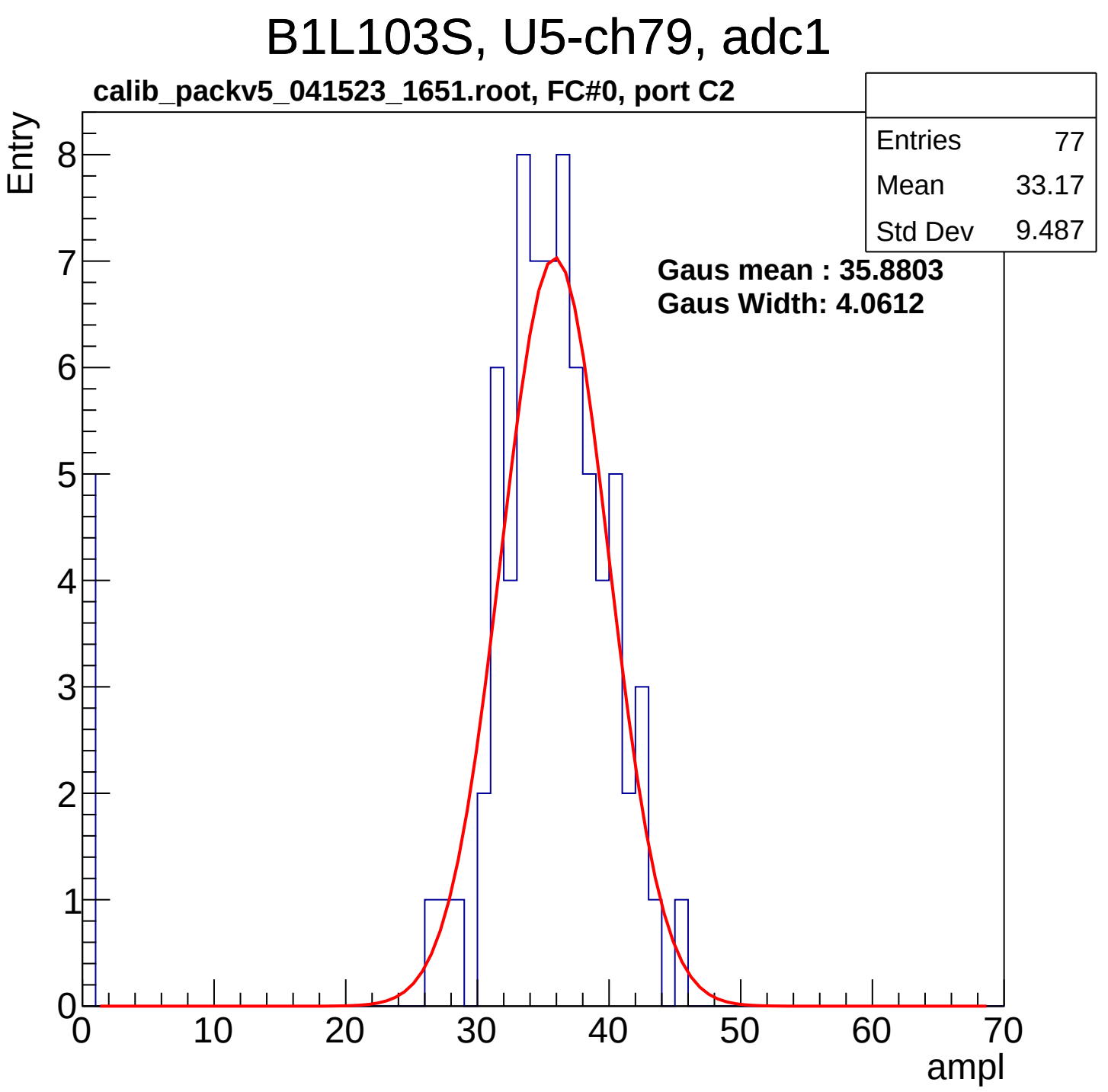
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch79, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 20.62
Std Dev 12.91
Gaus mean : 28.9446
Gaus Width: 3.3651
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U5-ch79, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 33.17
Std Dev 9.487
Gaus mean : 35.8803
Gaus Width: 4.0612
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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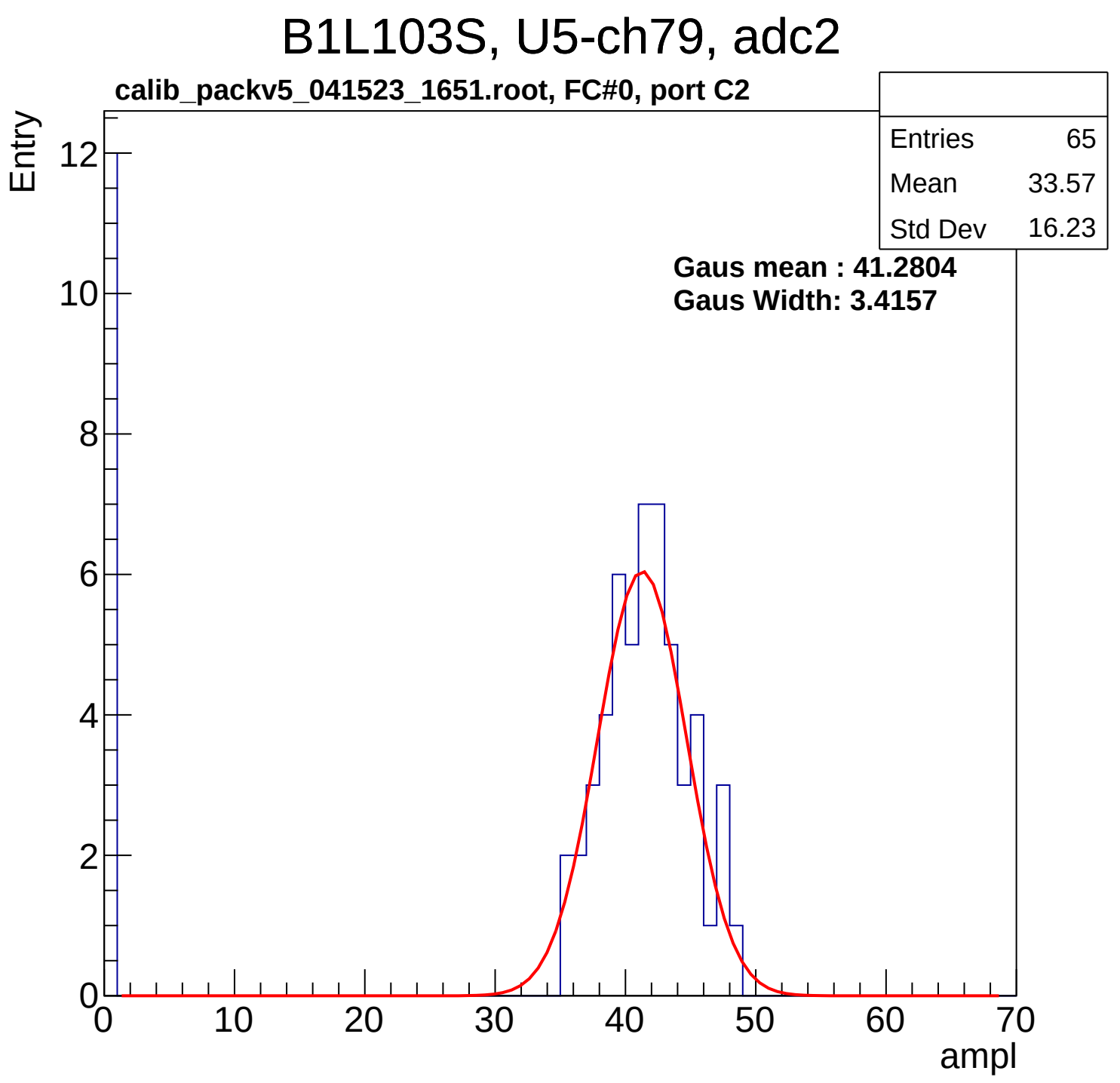
B1L103S, U5-ch79, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 33.57
Std Dev 16.23
Gaus mean : 41.2804
Gaus Width: 3.4157
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
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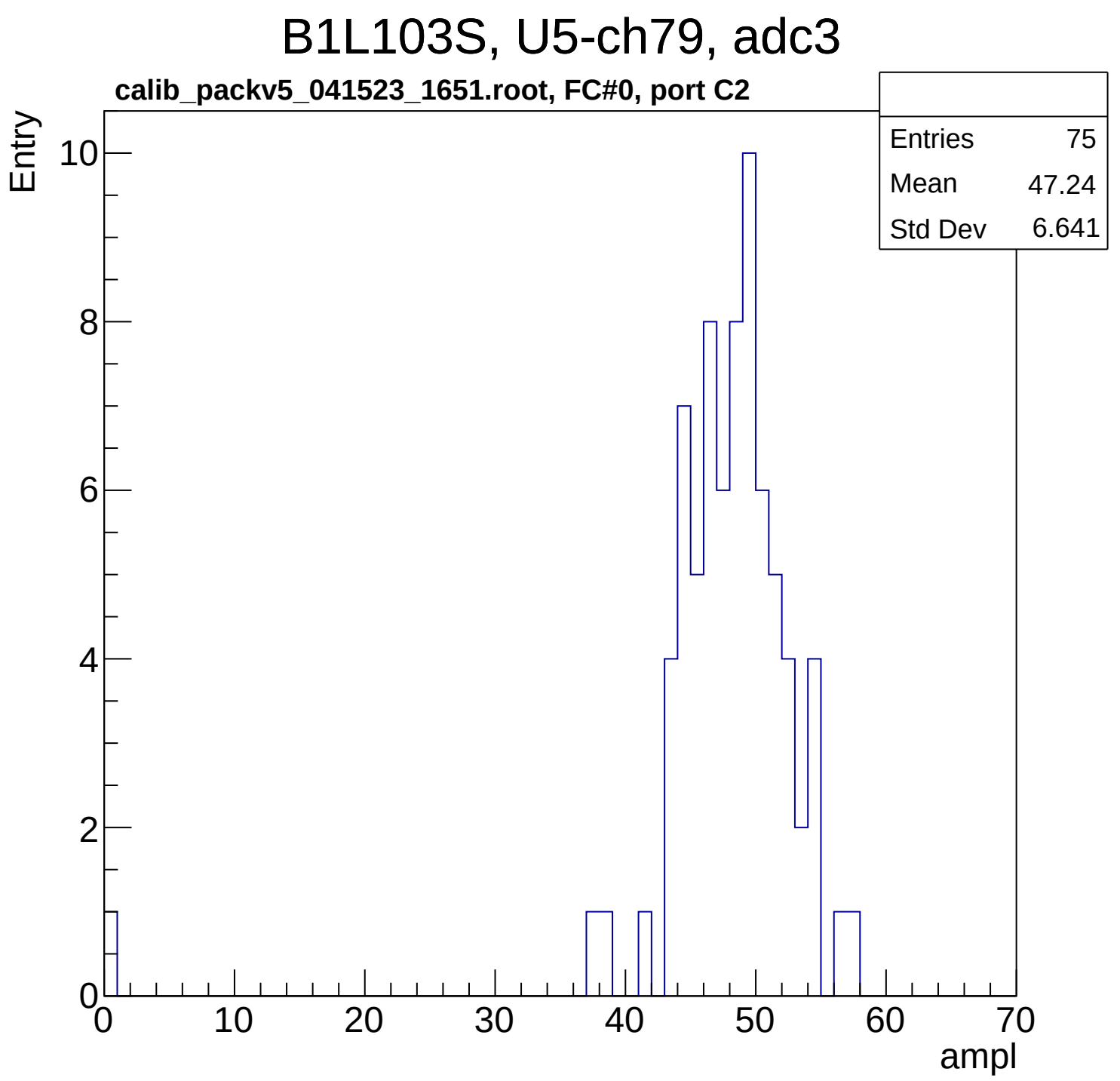
B1L103S, U5-ch79, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 47.24
Std Dev 6.641
Entry
ampl
0
2
4
6
8
10
0
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20
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40
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60
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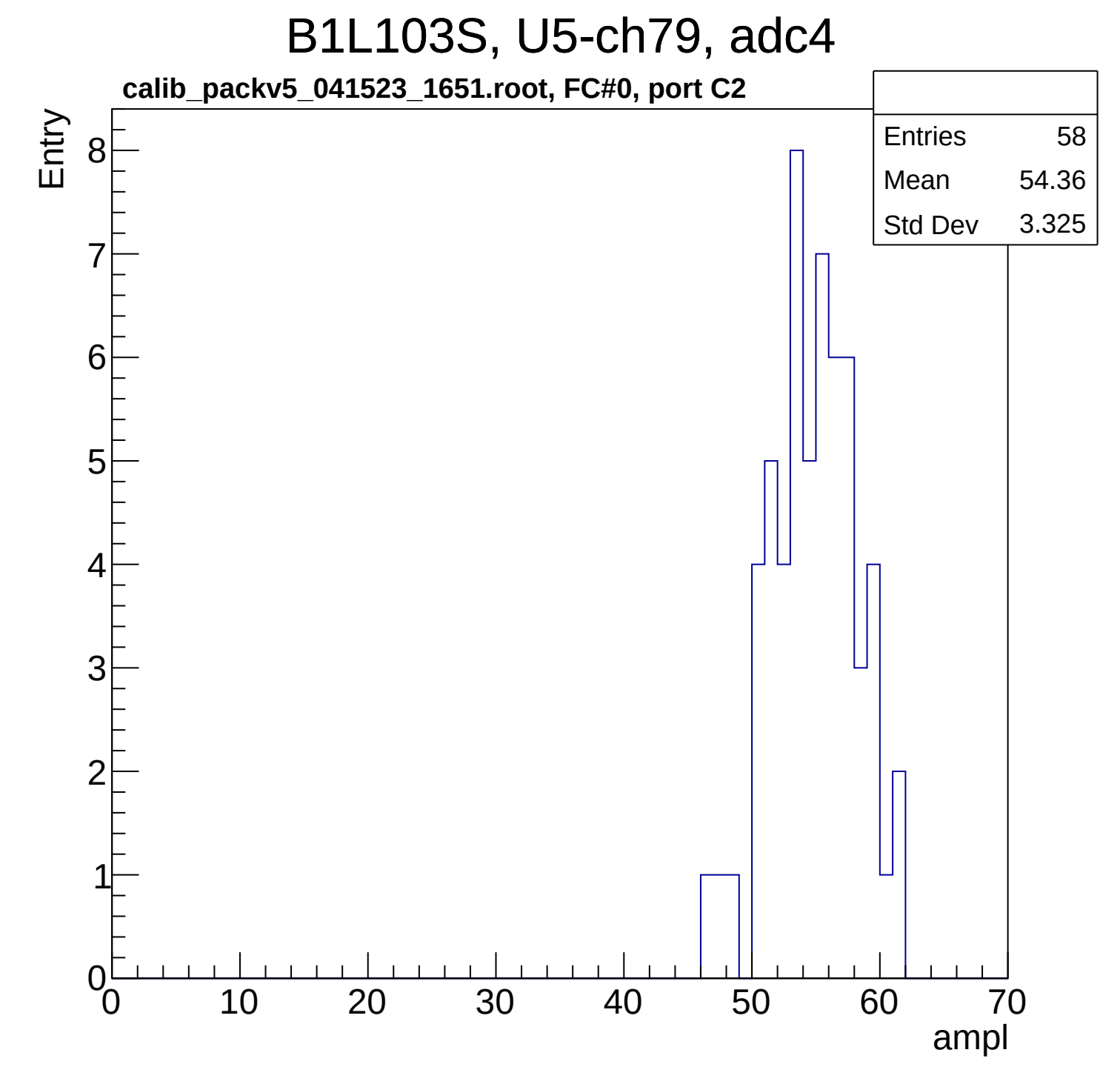
B1L103S, U5-ch79, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 54.36
Std Dev 3.325
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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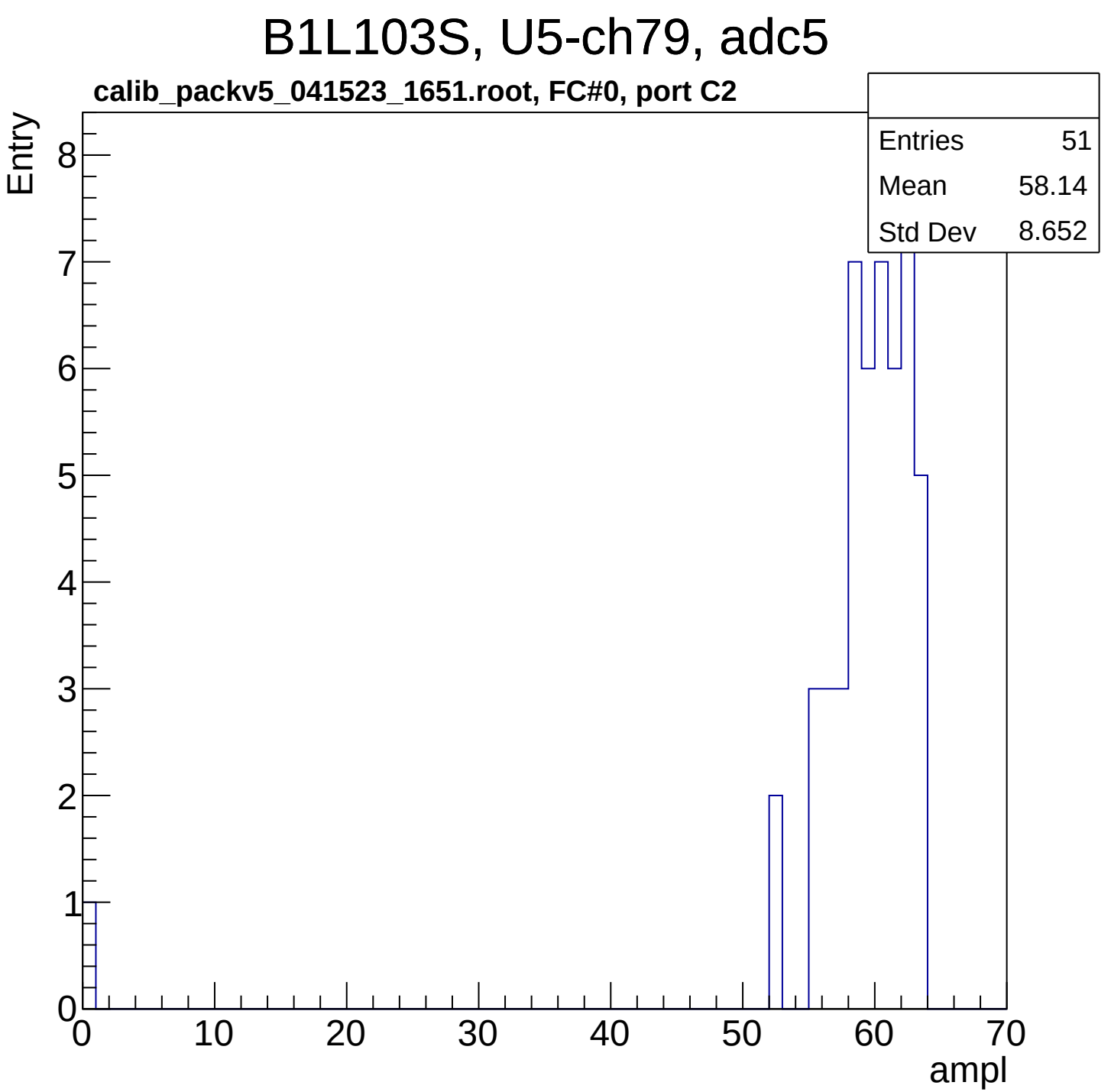
B1L103S, U5-ch79, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.14
Std Dev 8.652
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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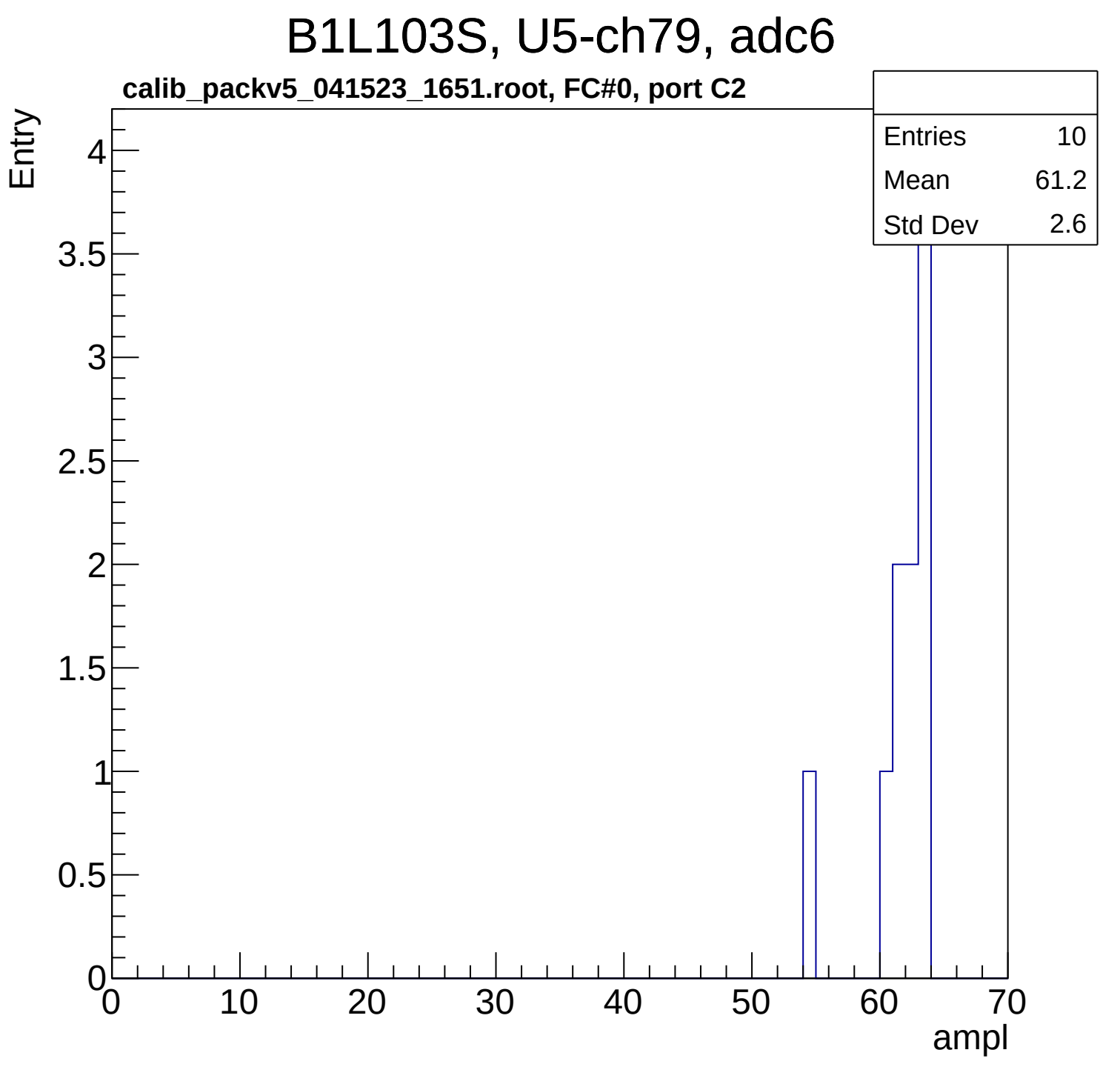
B1L103S, U5-ch79, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.2
Std Dev 2.6
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
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60
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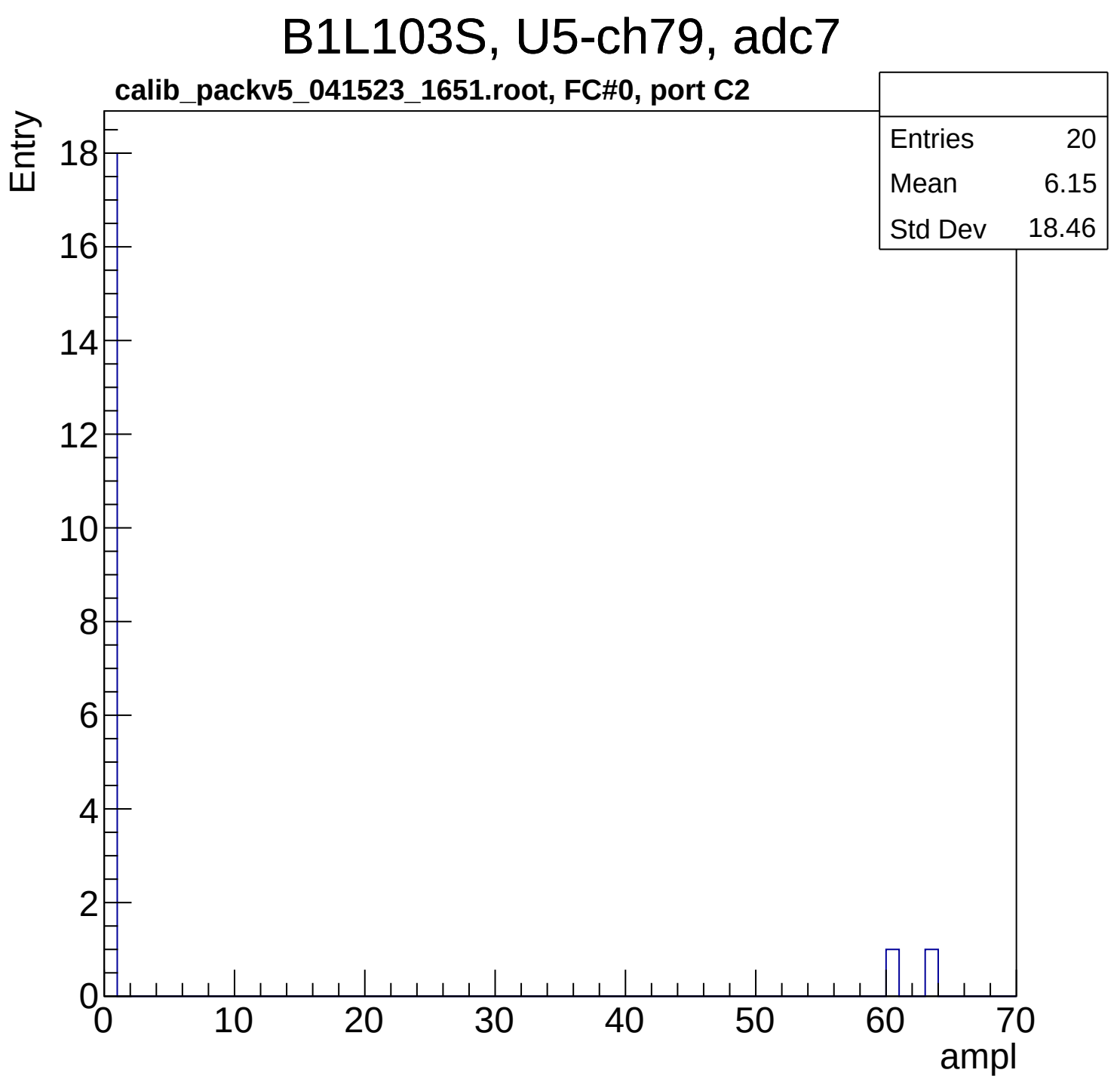
B1L103S, U5-ch79, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.15
Std Dev 18.46
Entry
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6
8
10
12
14
16
18
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10
20
30
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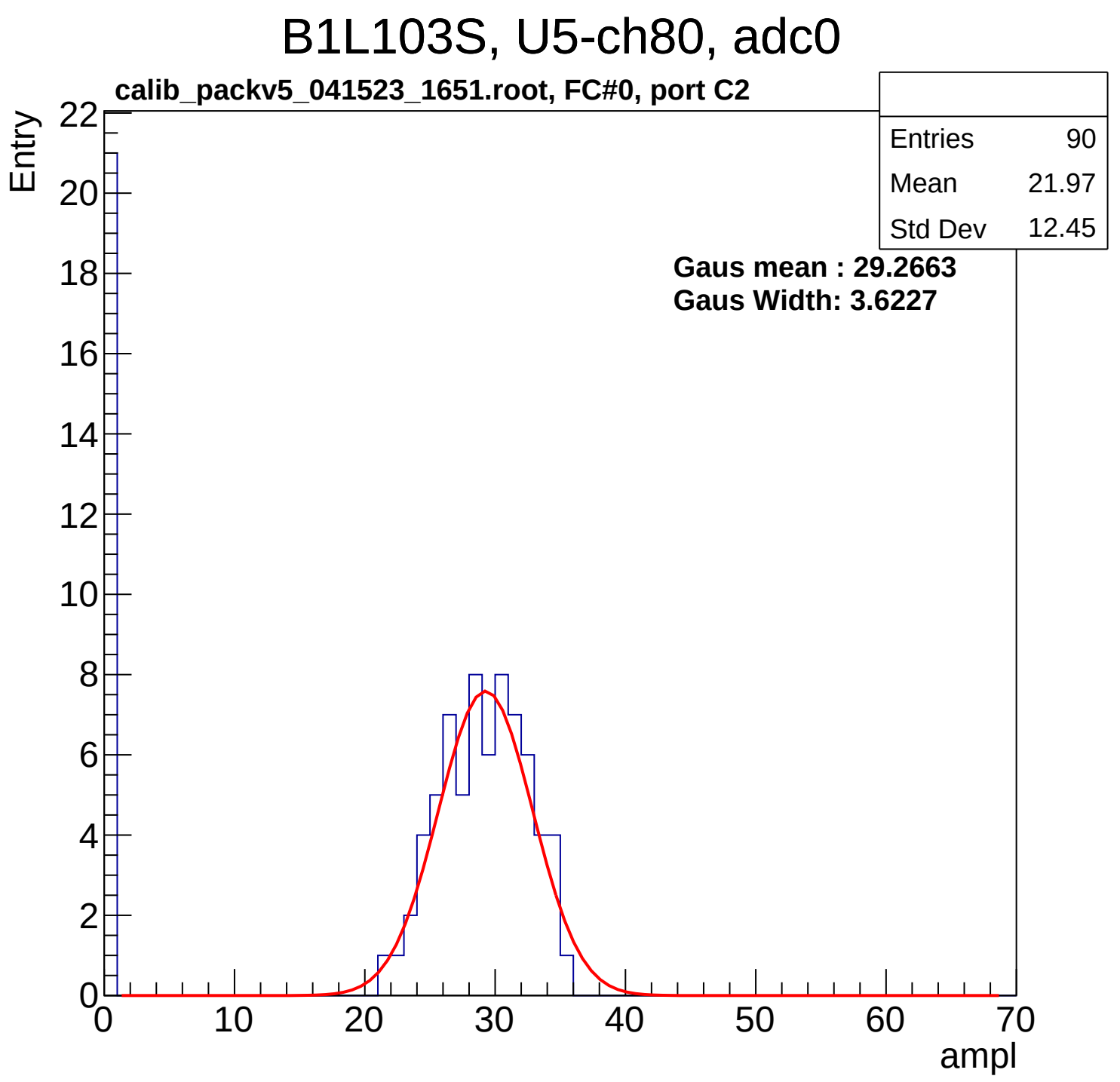
50
60
70
ampl


B1L103S, U5-ch80, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 21.97
Std Dev 12.45
Gaus mean : 29.2663
Gaus Width: 3.6227
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
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60
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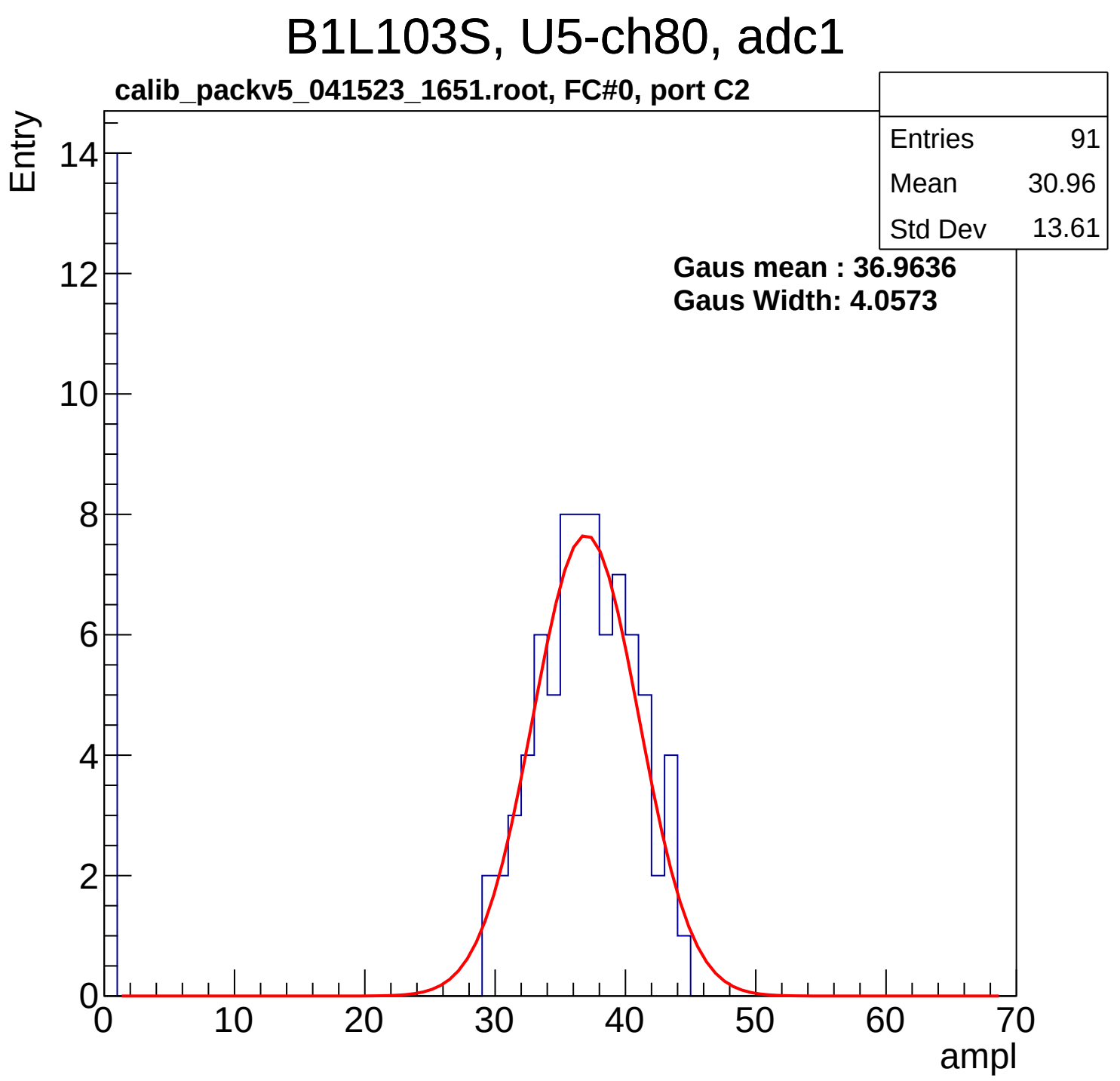
B1L103S, U5-ch80, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 30.96
Std Dev 13.61
Gaus mean : 36.9636
Gaus Width: 4.0573
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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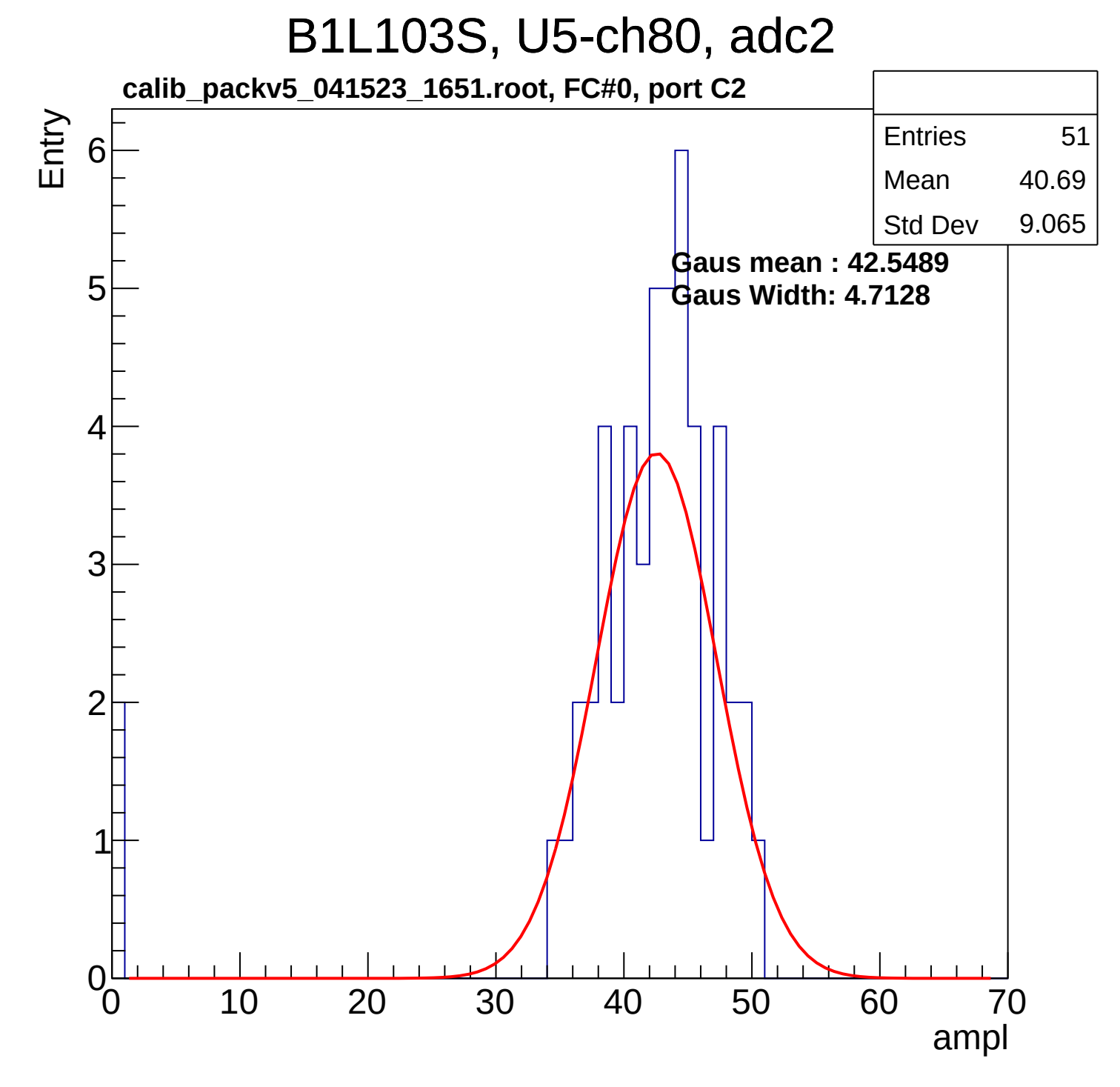
B1L103S, U5-ch80, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 40.69
Std Dev 9.065
Gaus mean : 42.5489
Gaus Width: 4.7128
Entry
ampl
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1
2
3
4
5
6
0
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20
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40
50
60
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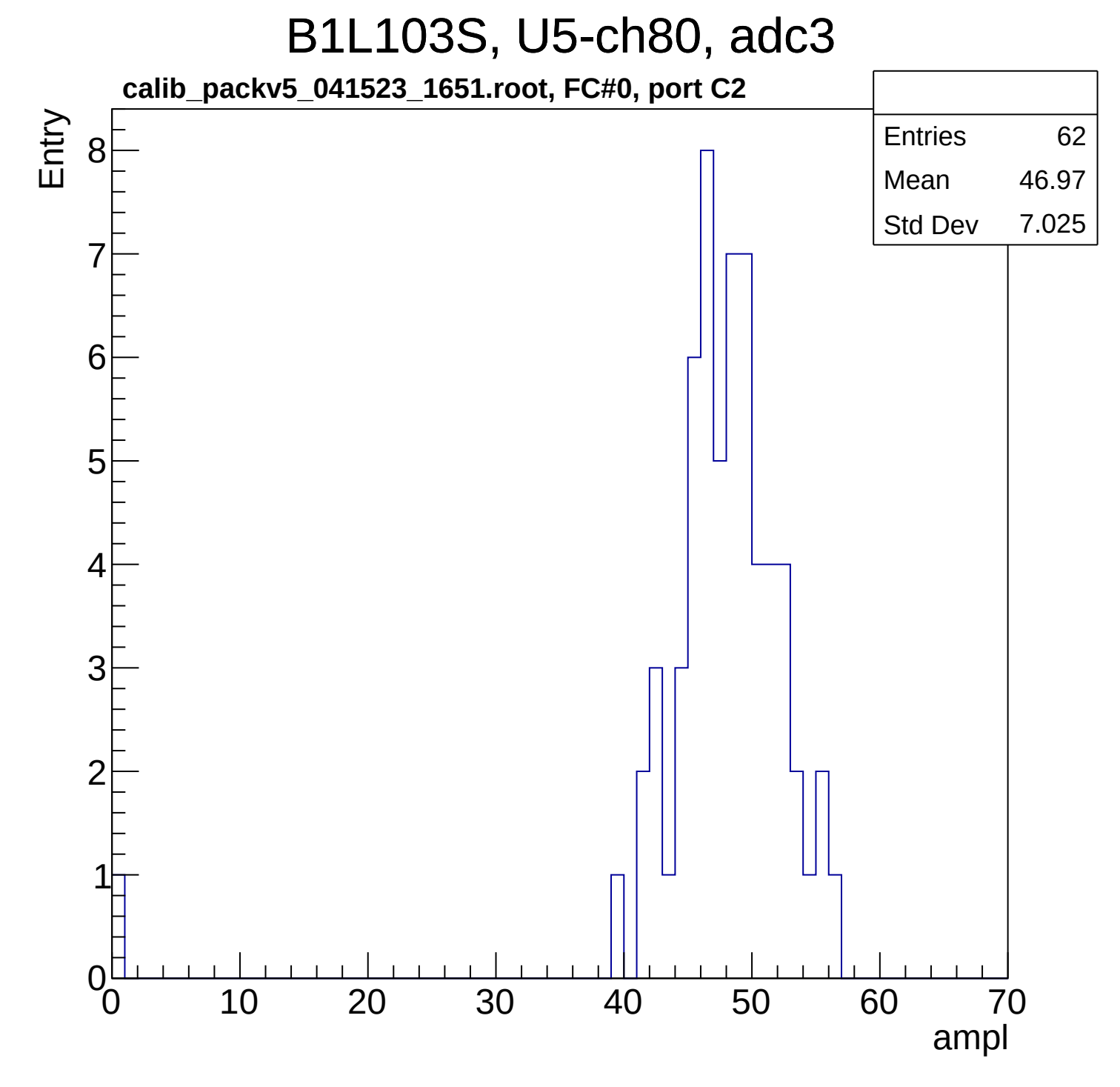
B1L103S, U5-ch80, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 46.97
Std Dev 7.025
Entry
ampl
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3
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5
6
7
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0
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20
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60
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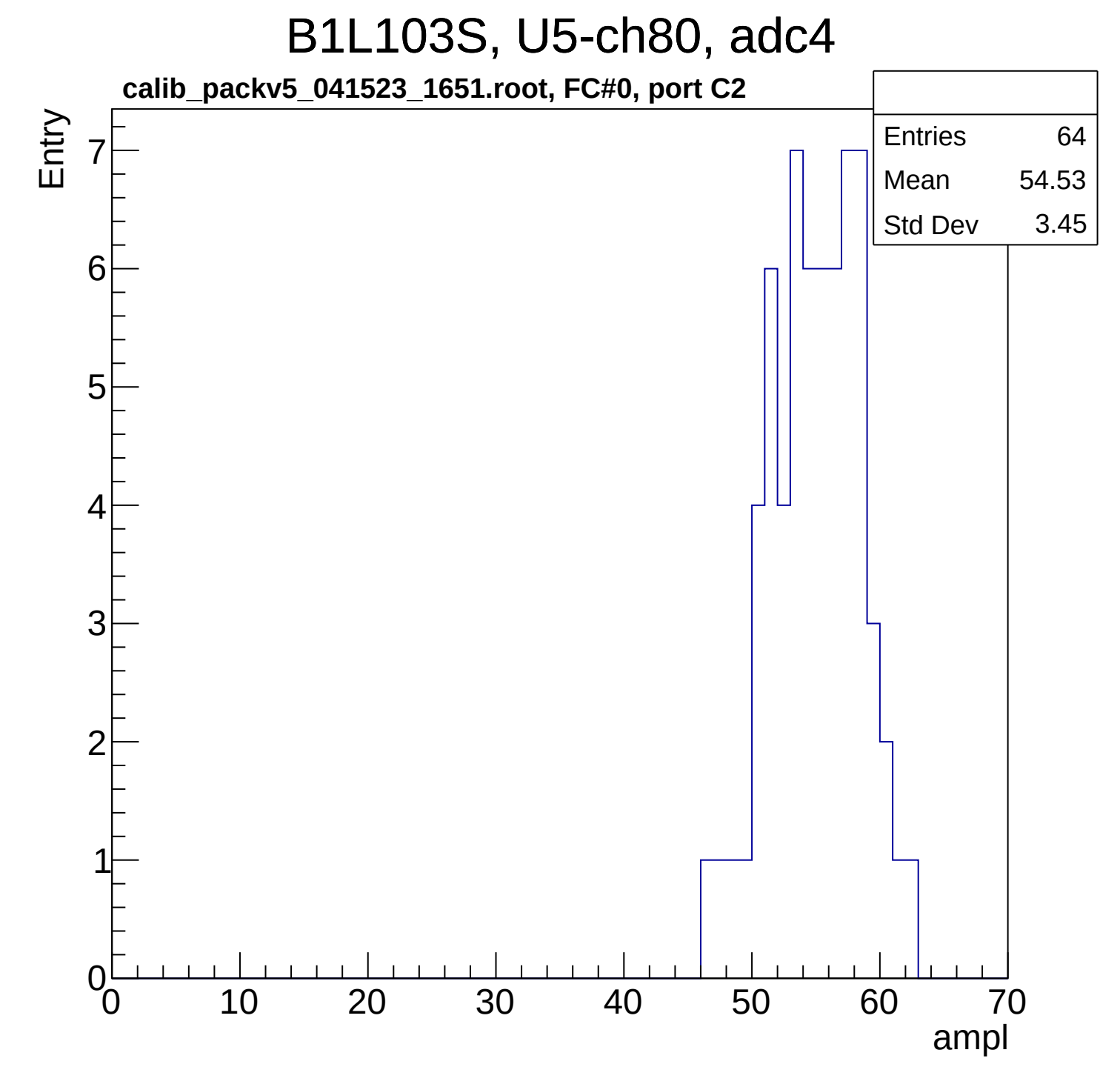
B1L103S, U5-ch80, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 54.53
Std Dev 3.45
Entry
ampl
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3
4
5
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7
0
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60
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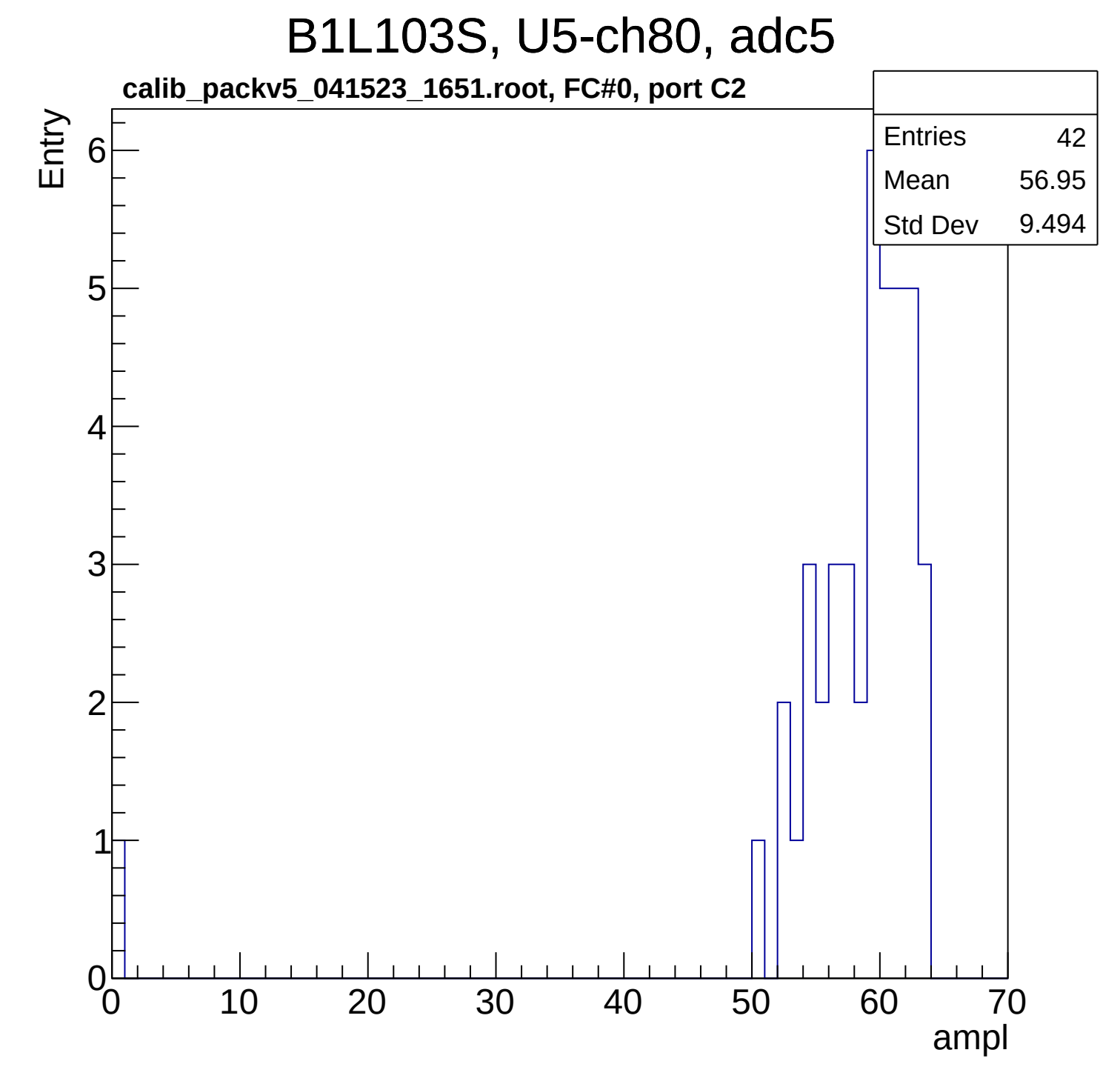
B1L103S, U5-ch80, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 56.95
Std Dev 9.494
Entry
ampl
0
1
2
3
4
5
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0
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20
30
40
50
60
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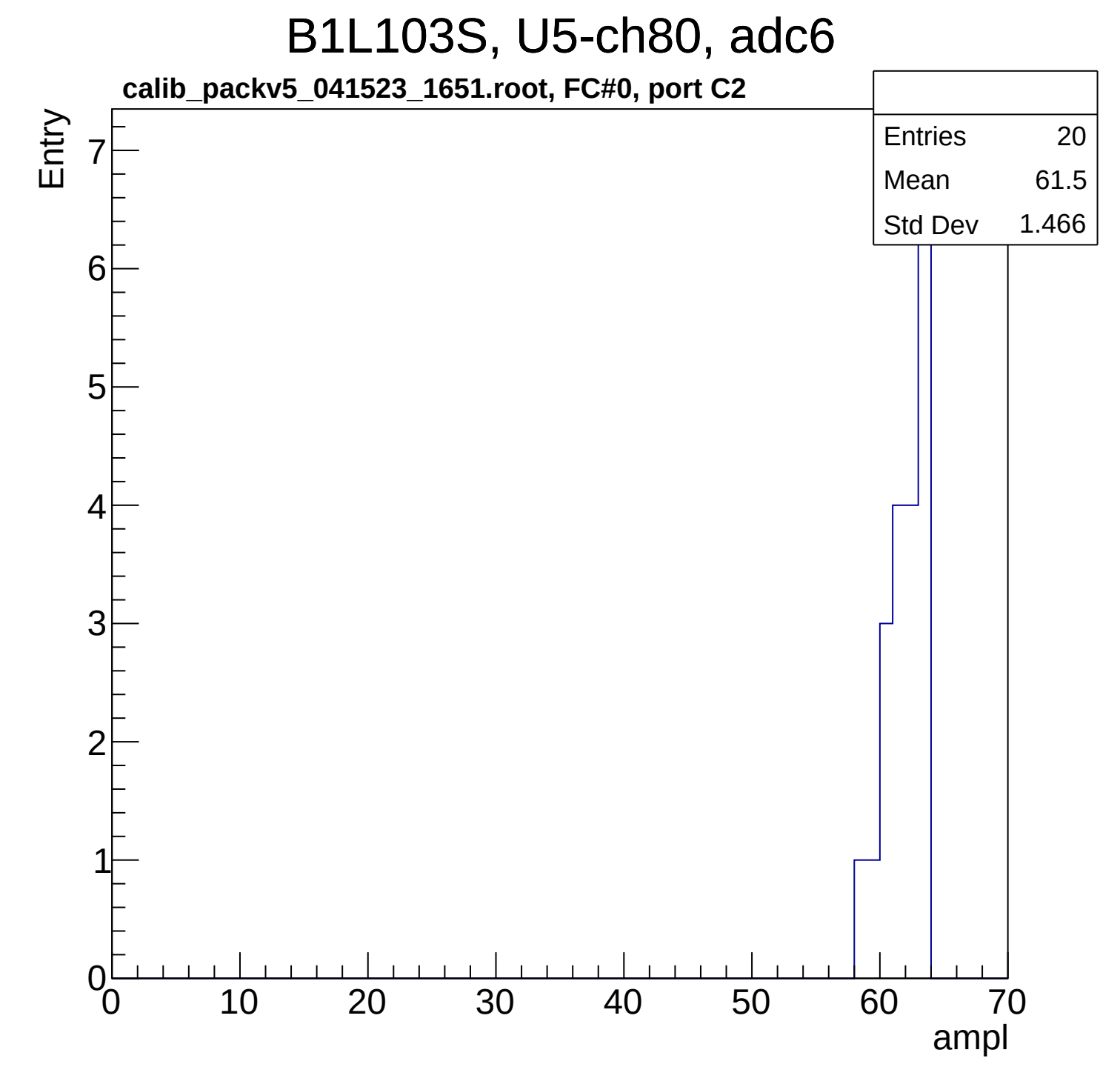
B1L103S, U5-ch80, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 61.5
Std Dev 1.466
Entry
ampl
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2
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4
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0
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20
30
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60
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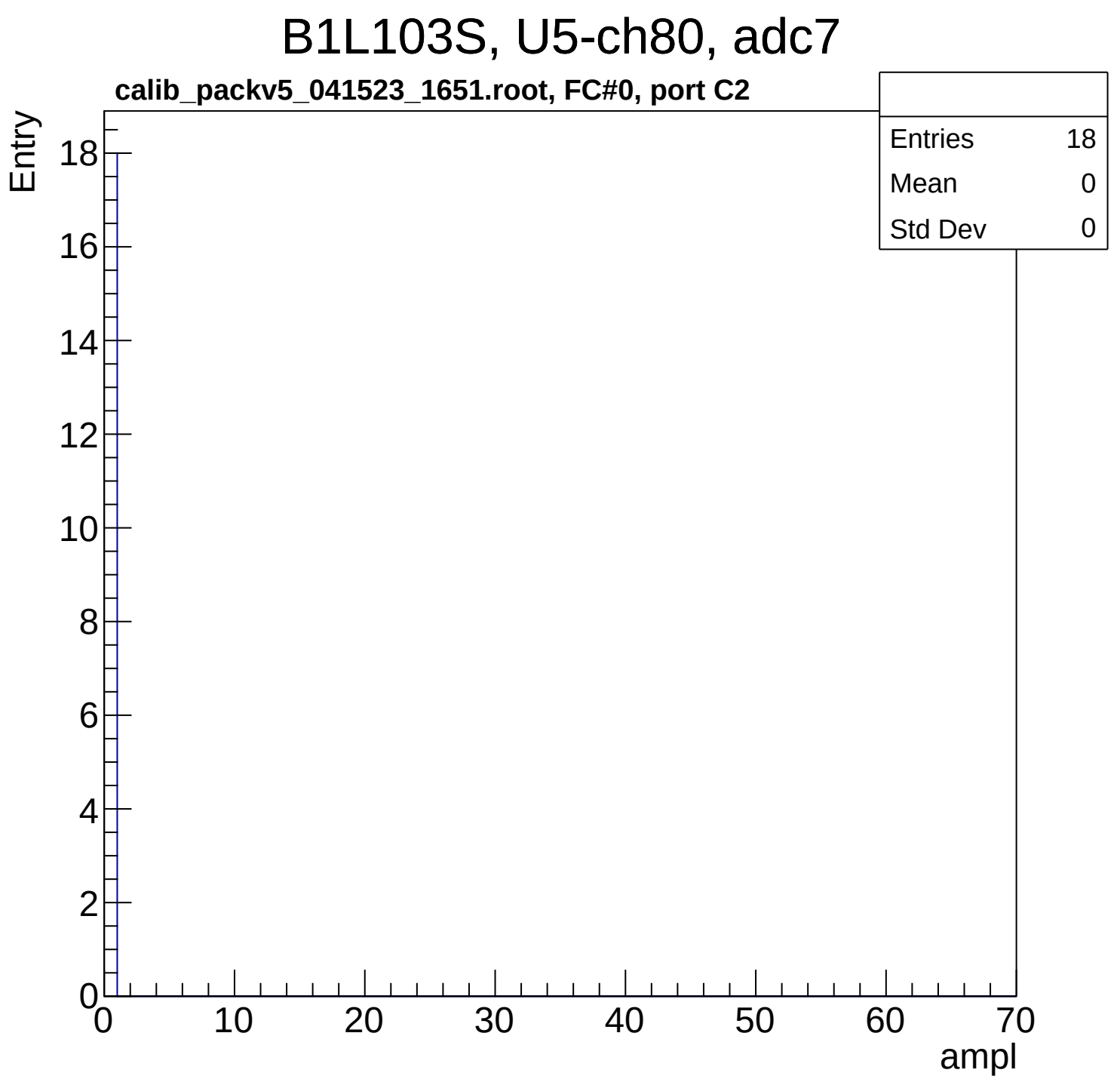
B1L103S, U5-ch80, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
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18
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10
20
30
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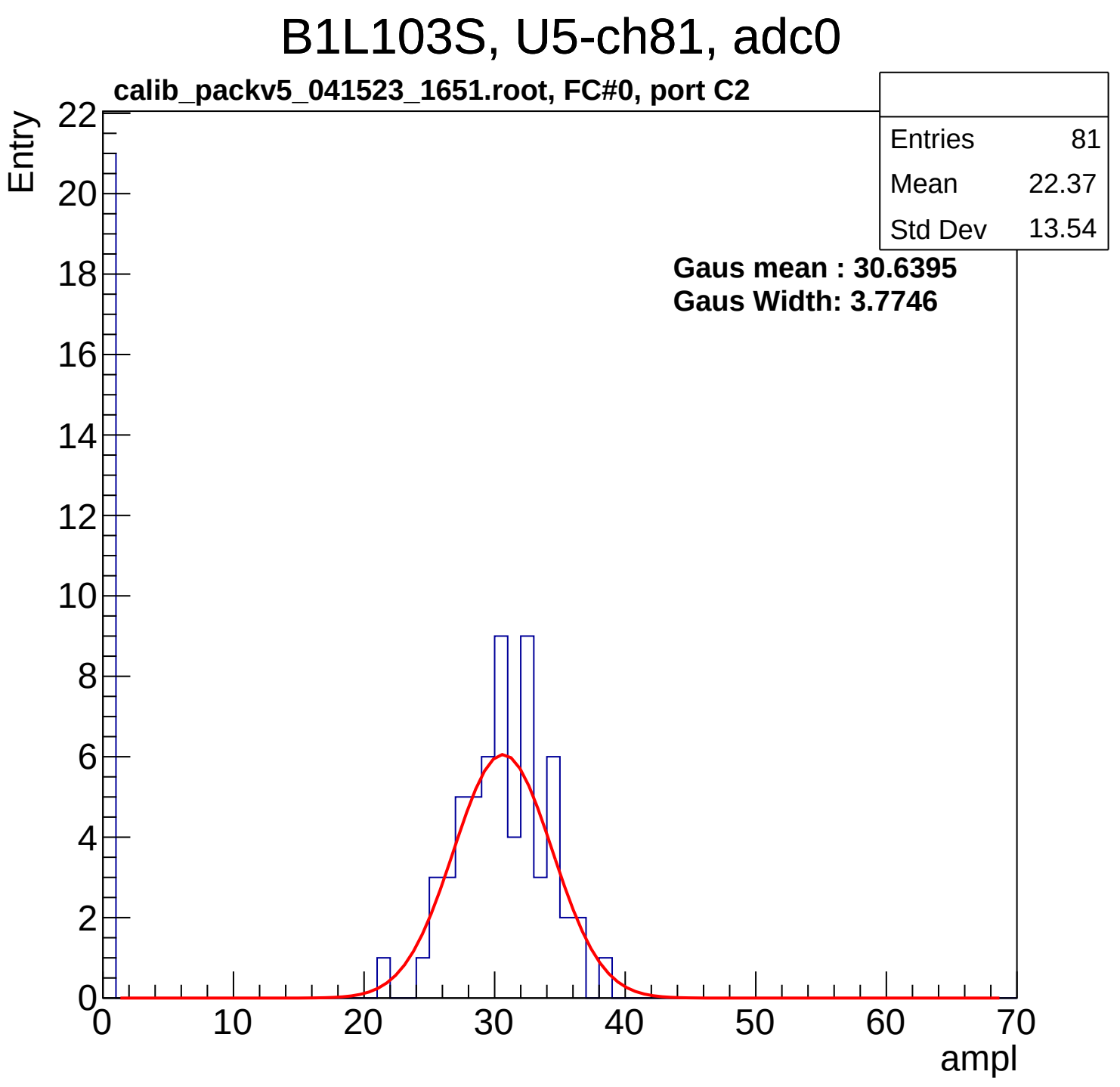
50
60
70
ampl


B1L103S, U5-ch81, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 22.37
Std Dev 13.54
Gaus mean : 30.6395
Gaus Width: 3.7746
Entry
ampl
0
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8
10
12
14
16
18
20
22
0
10
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60
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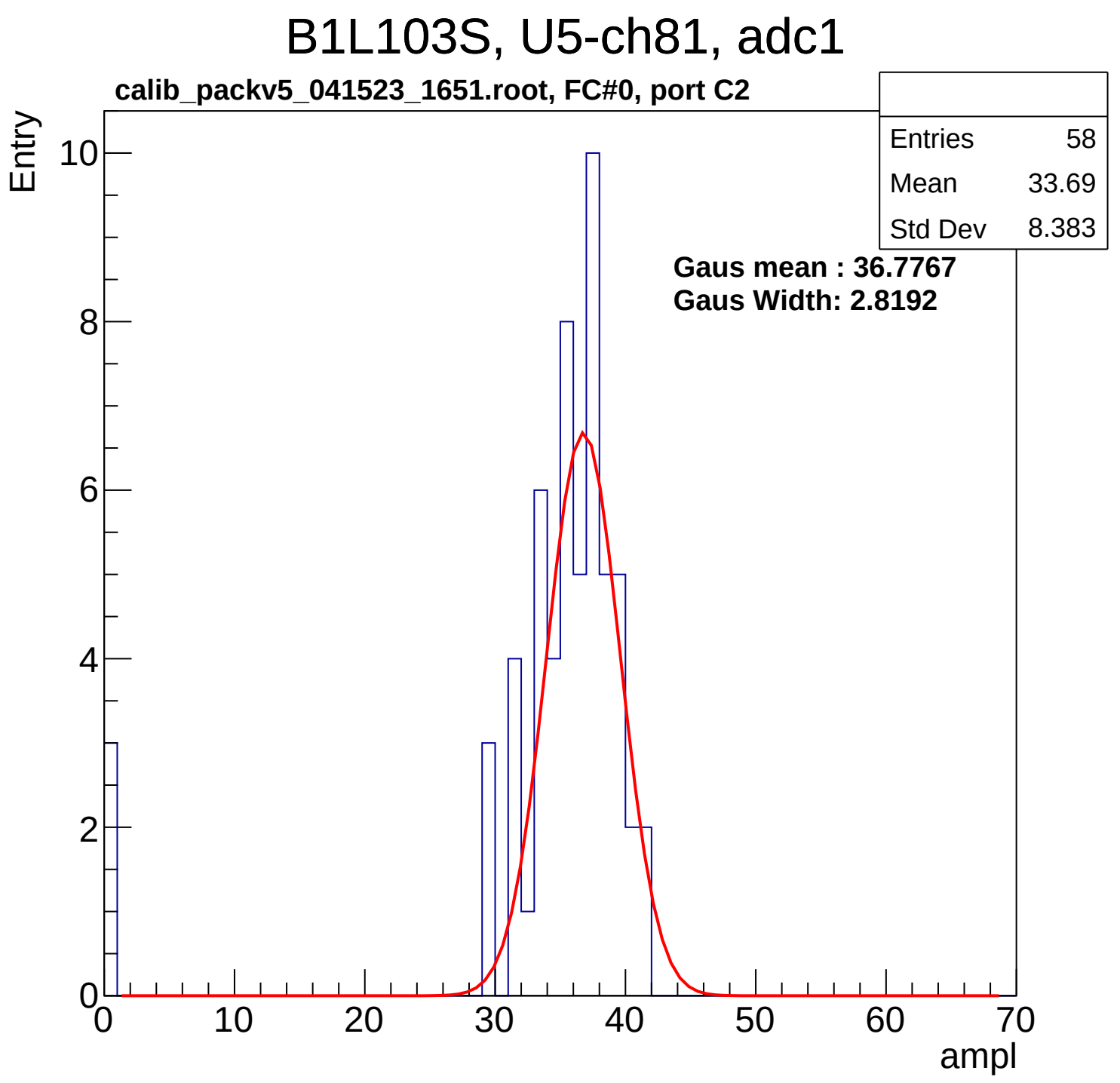
B1L103S, U5-ch81, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 33.69
Std Dev 8.383
Gaus mean : 36.7767
Gaus Width: 2.8192
Entry
ampl
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6
8
10
0
10
20
30
40
50
60
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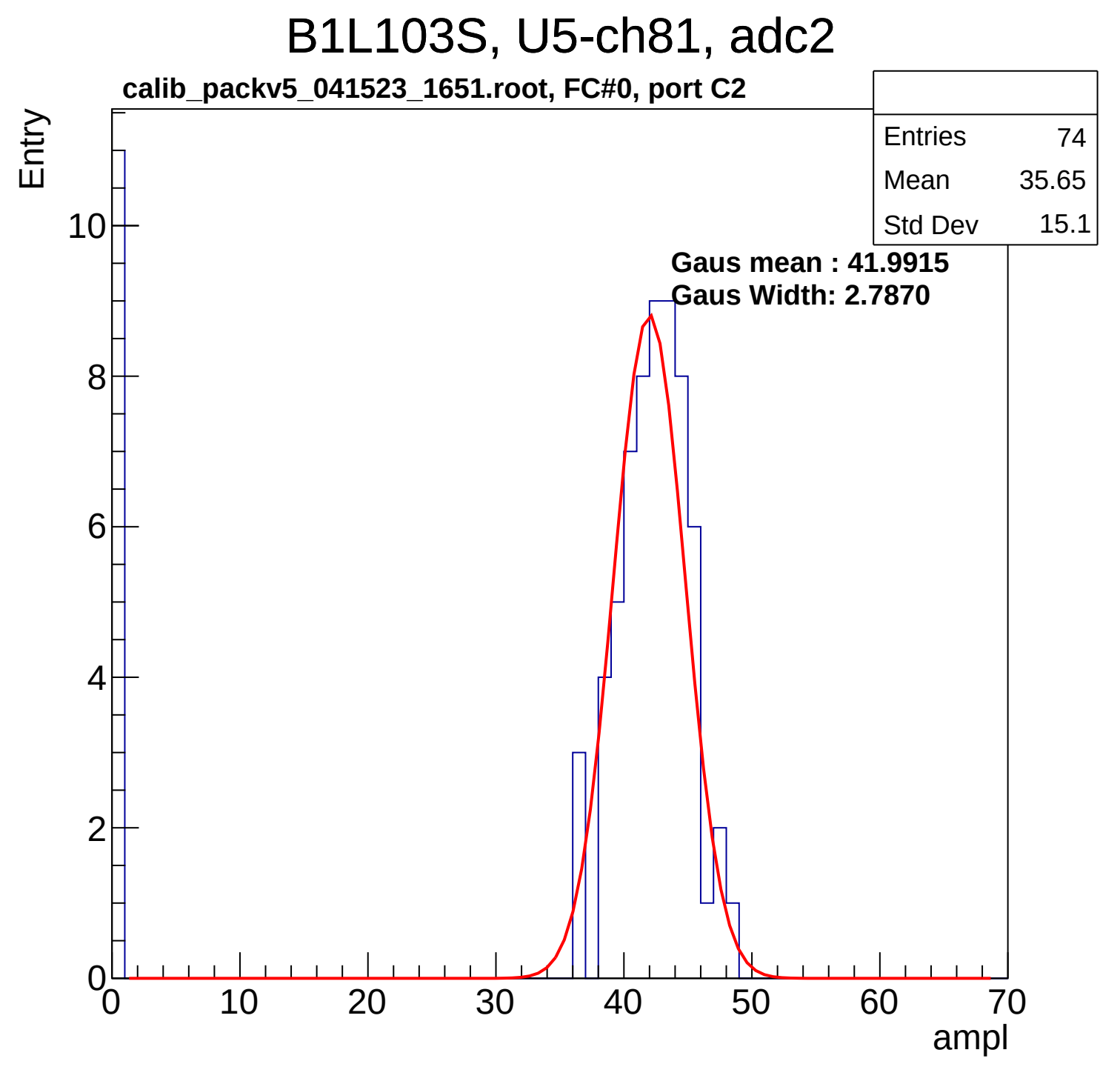
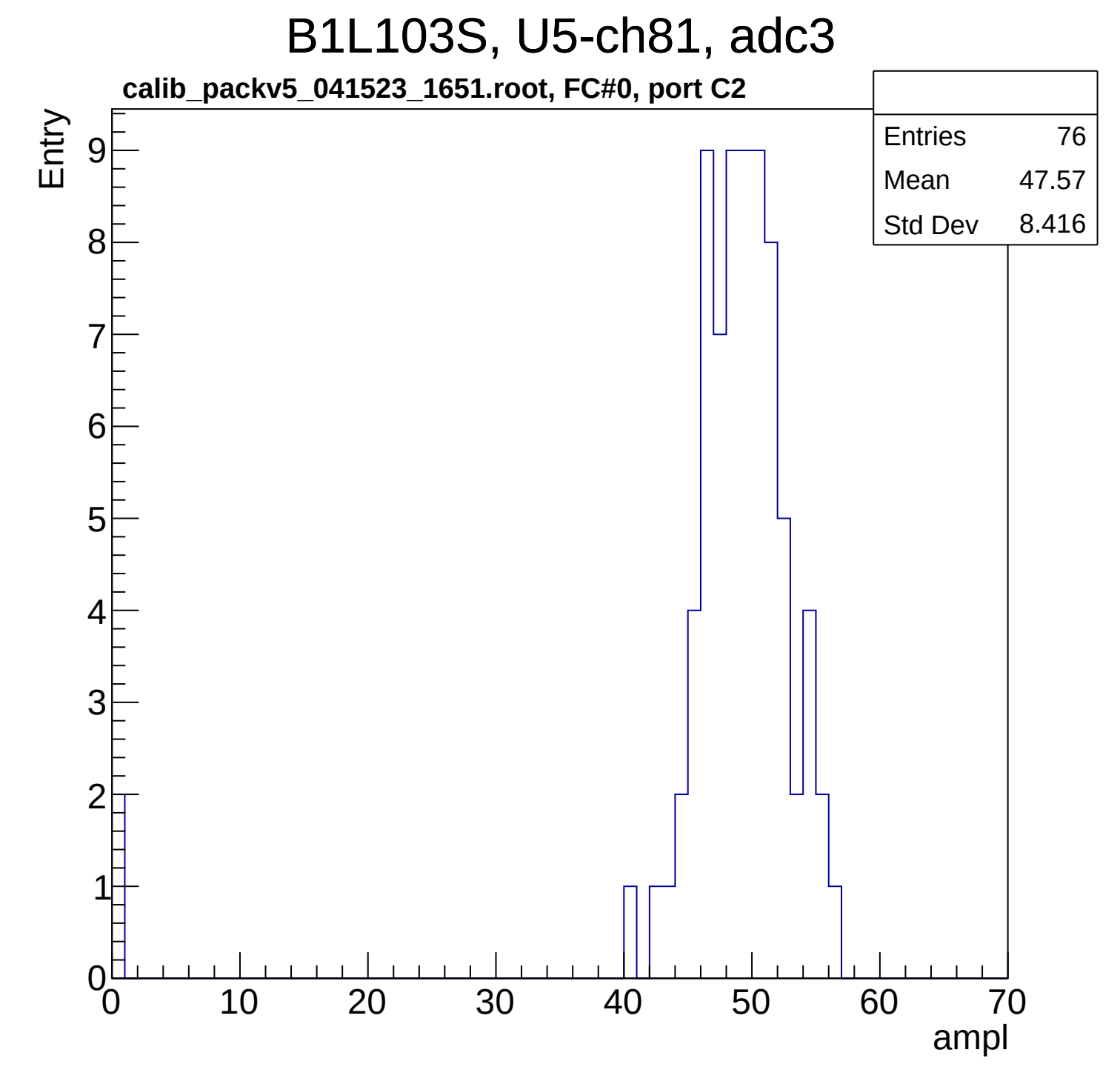

B1L103S, U5-ch81, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 35.65
Std Dev 15.1
Gaus mean : 41.9915
Gaus Width: 2.7870
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U5-ch81, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 47.57
Std Dev 8.416
Entry
ampl
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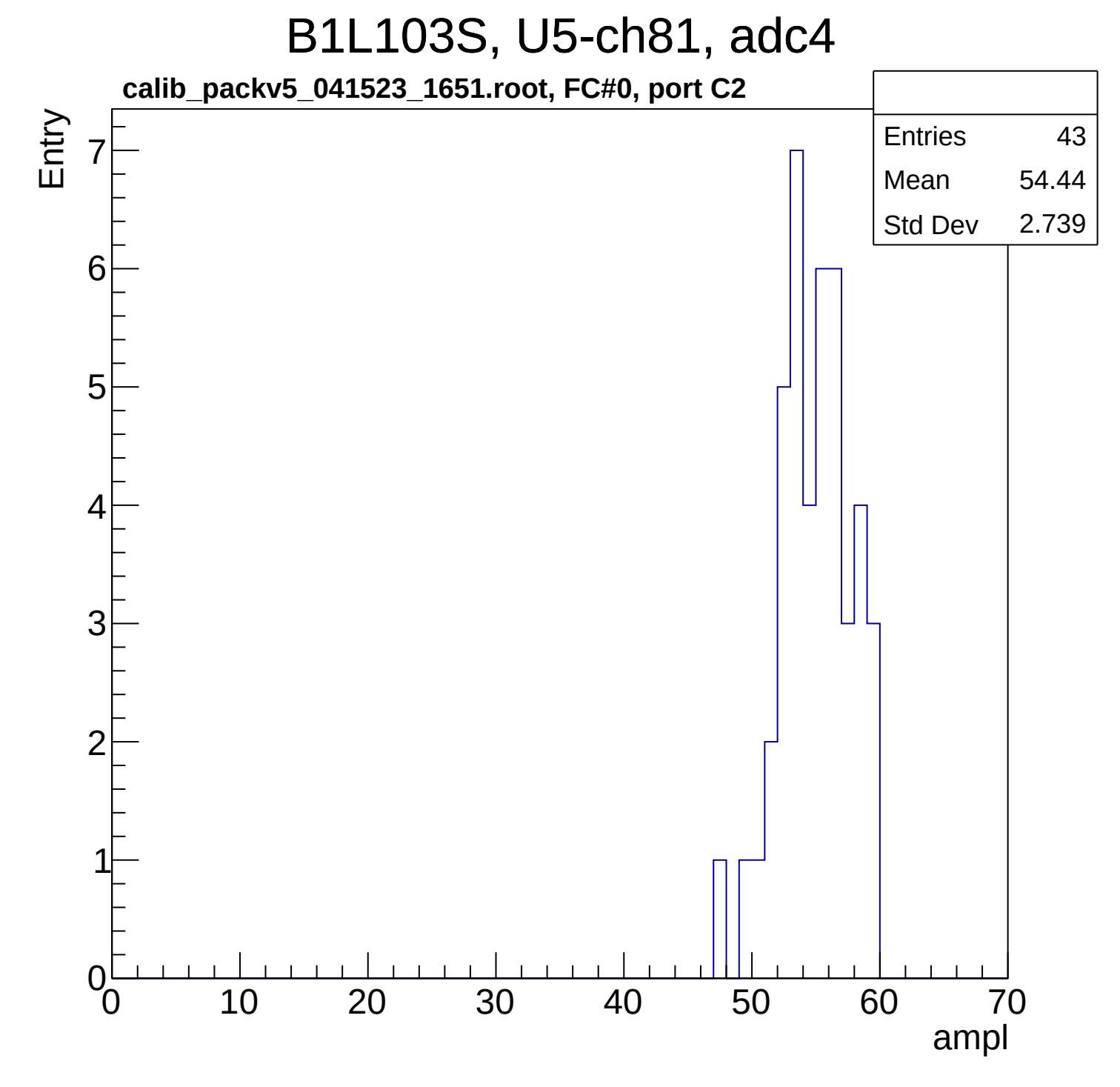
B1L103S, U5-ch81, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 54.44
Std Dev 2.739
Entry
ampl
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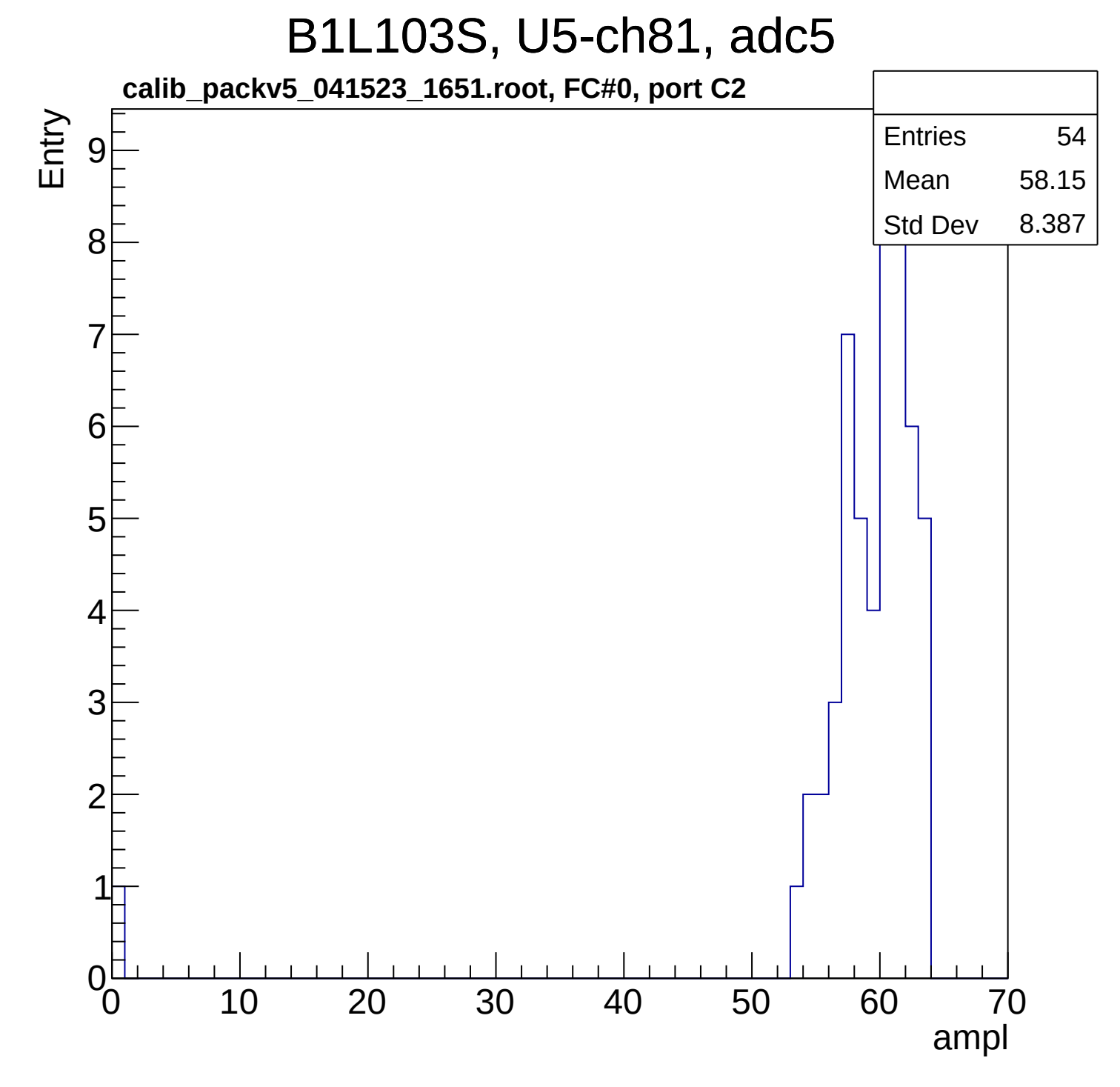
B1L103S, U5-ch81, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.15
Std Dev 8.387
Entry
ampl
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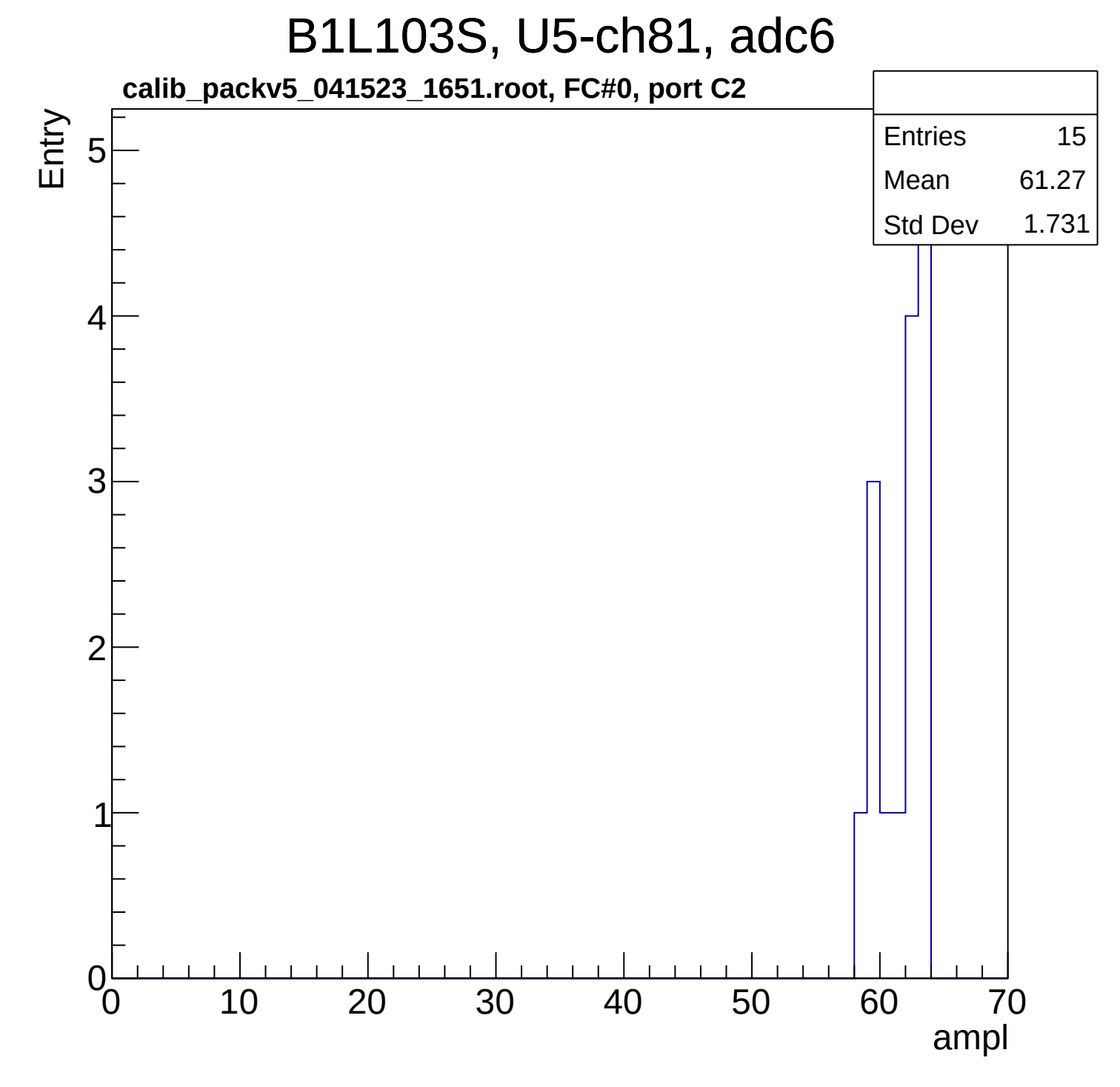
B1L103S, U5-ch81, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.27
Std Dev 1.731
Entry
ampl
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0
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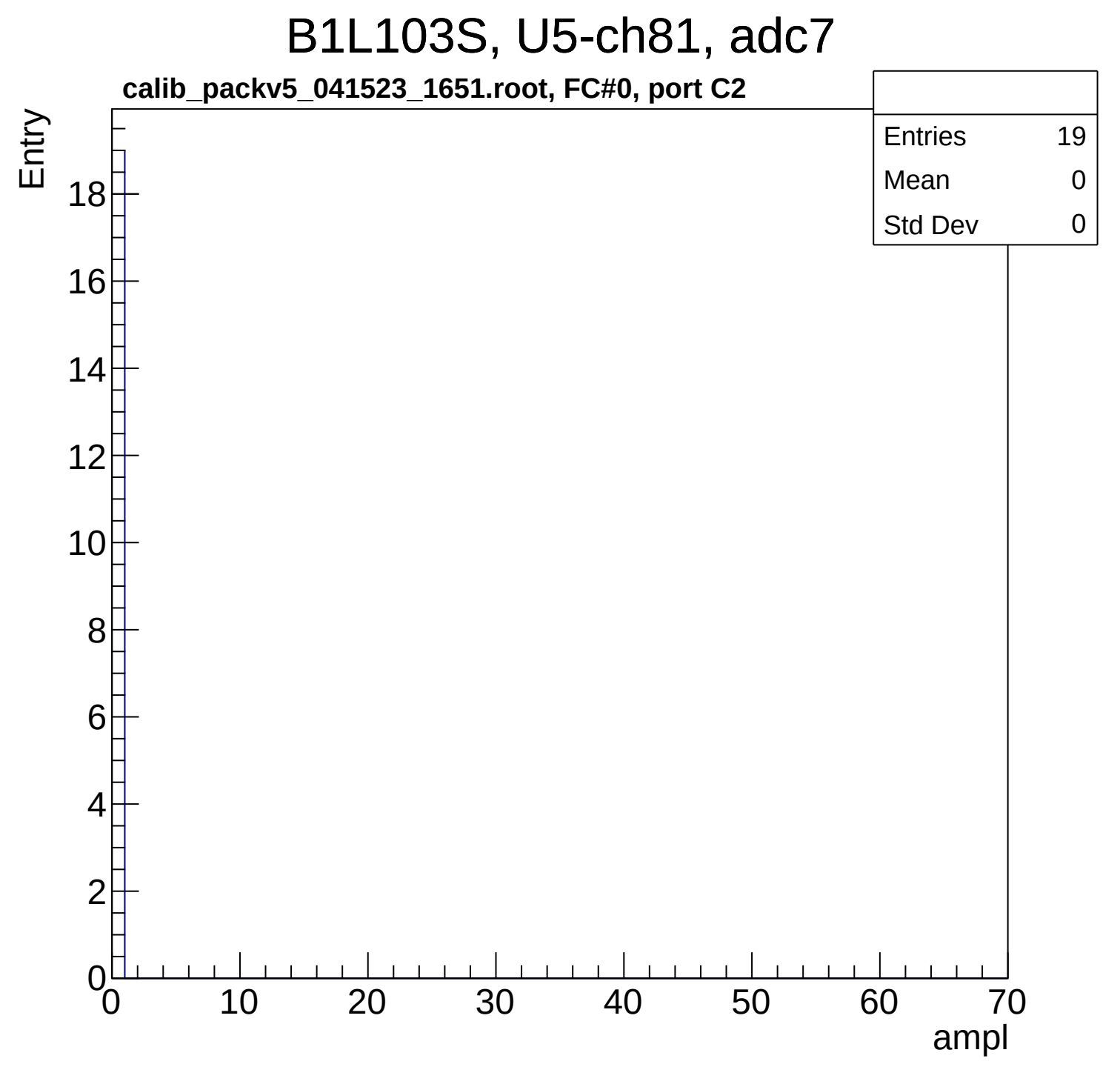
B1L103S, U5-ch81, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
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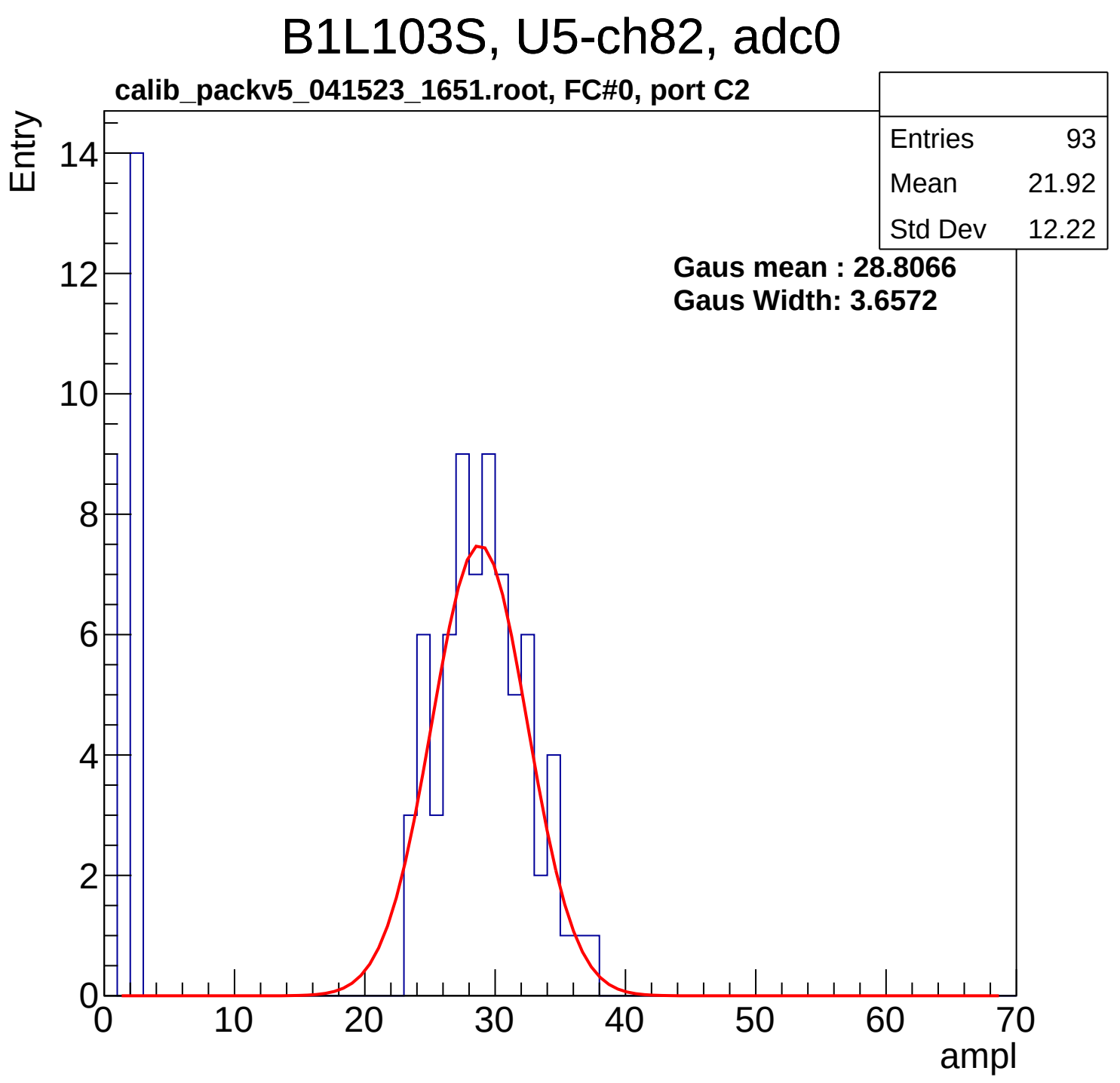
70
ampl


B1L103S, U5-ch82, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 21.92
Std Dev 12.22
Gaus mean : 28.8066
Gaus Width: 3.6572
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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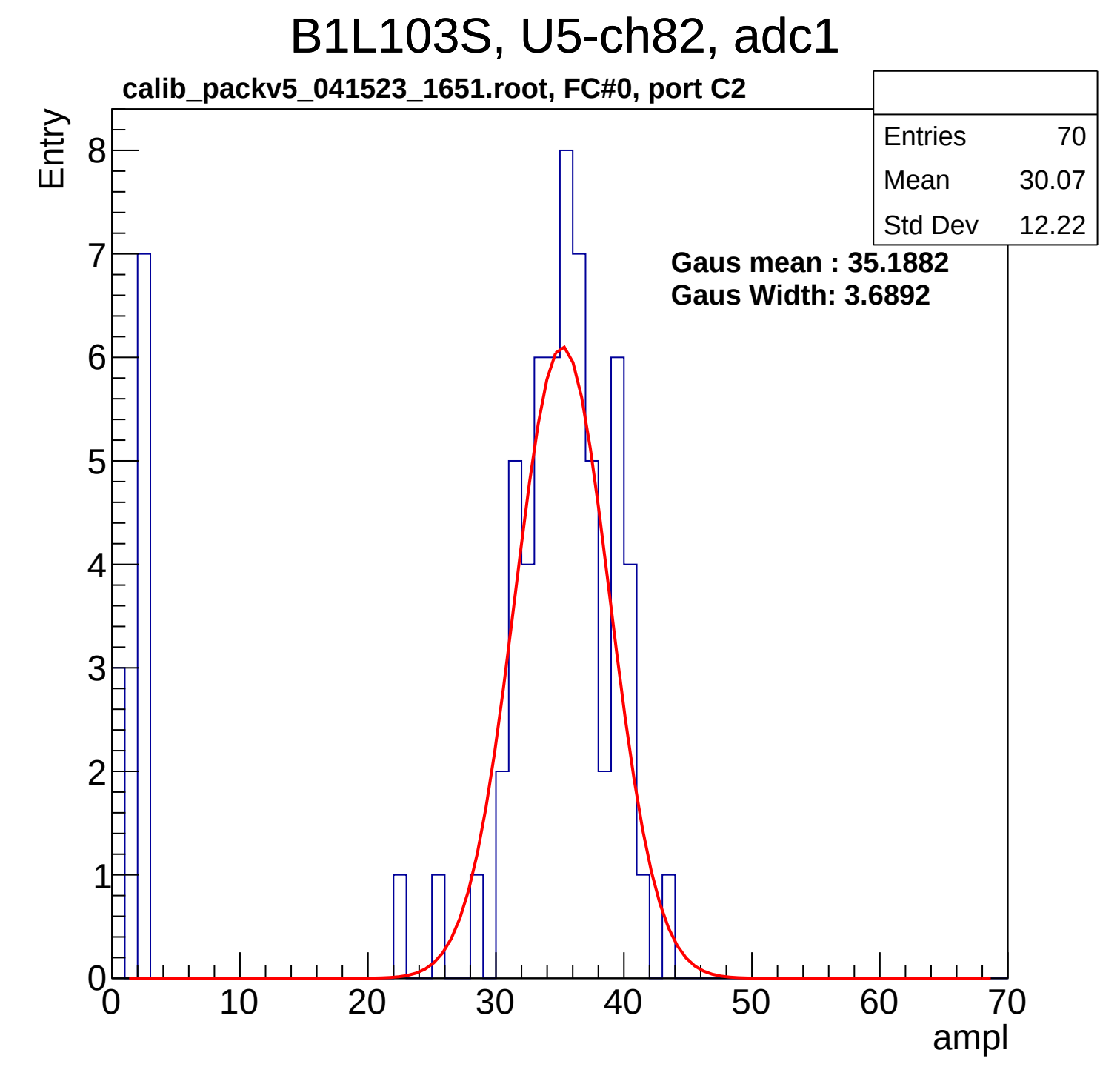
B1L103S, U5-ch82, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 30.07
Std Dev 12.22
Gaus mean : 35.1882
Gaus Width: 3.6892
Entry
ampl
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2
3
4
5
6
7
8
0
10
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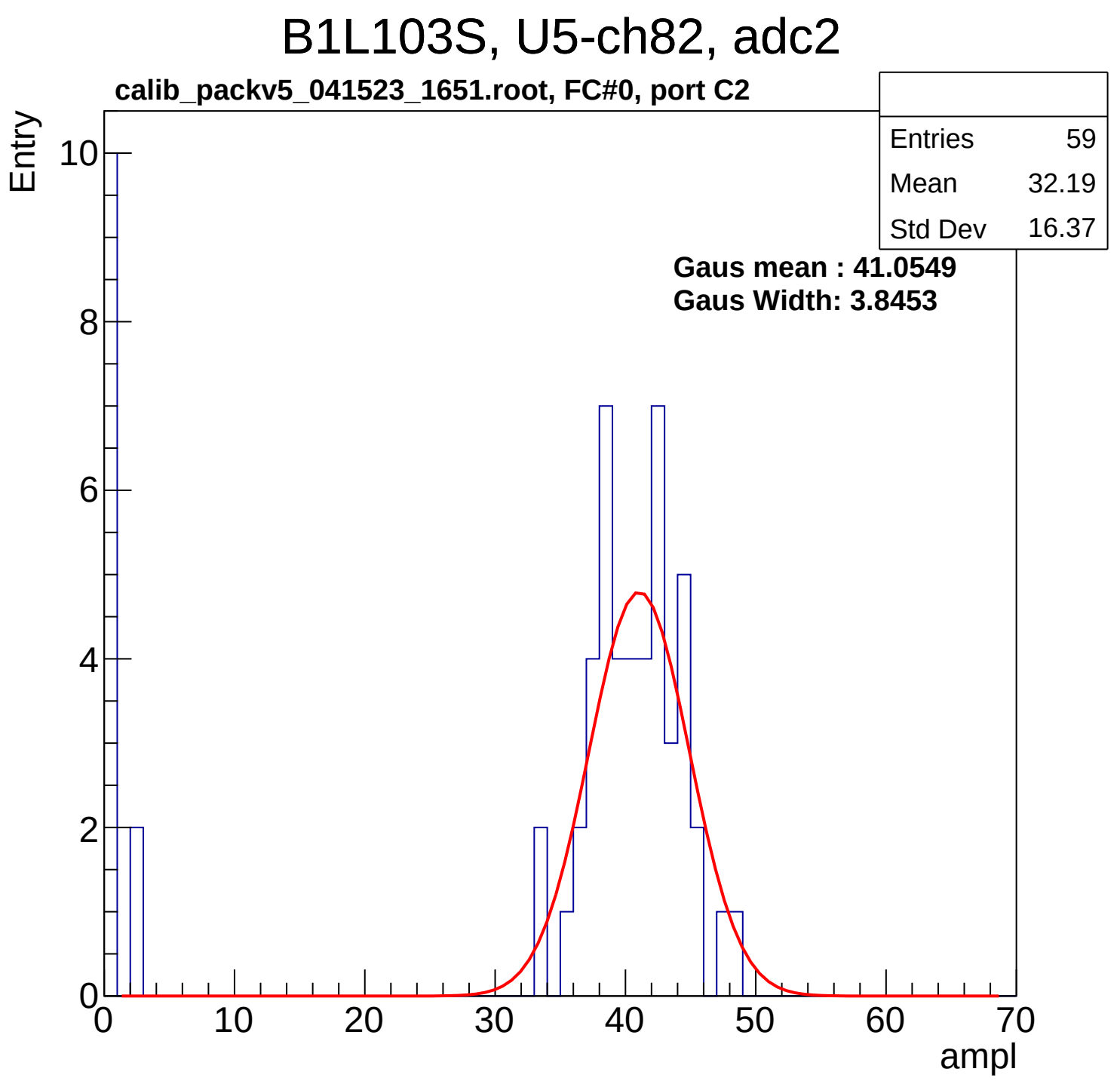
B1L103S, U5-ch82, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 32.19
Std Dev 16.37
Gaus mean : 41.0549
Gaus Width: 3.8453
Entry
ampl
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0
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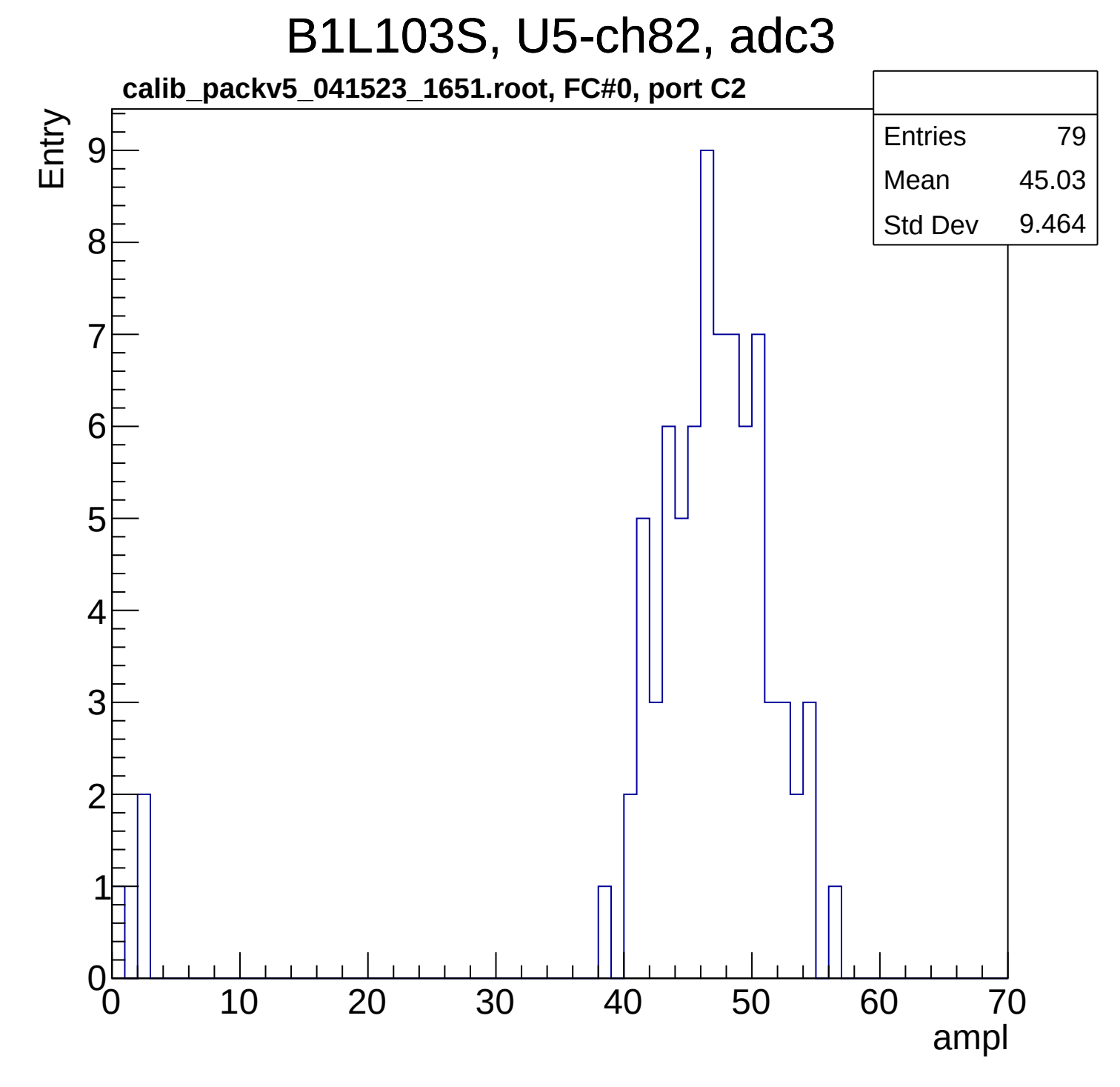
B1L103S, U5-ch82, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 45.03
Std Dev 9.464
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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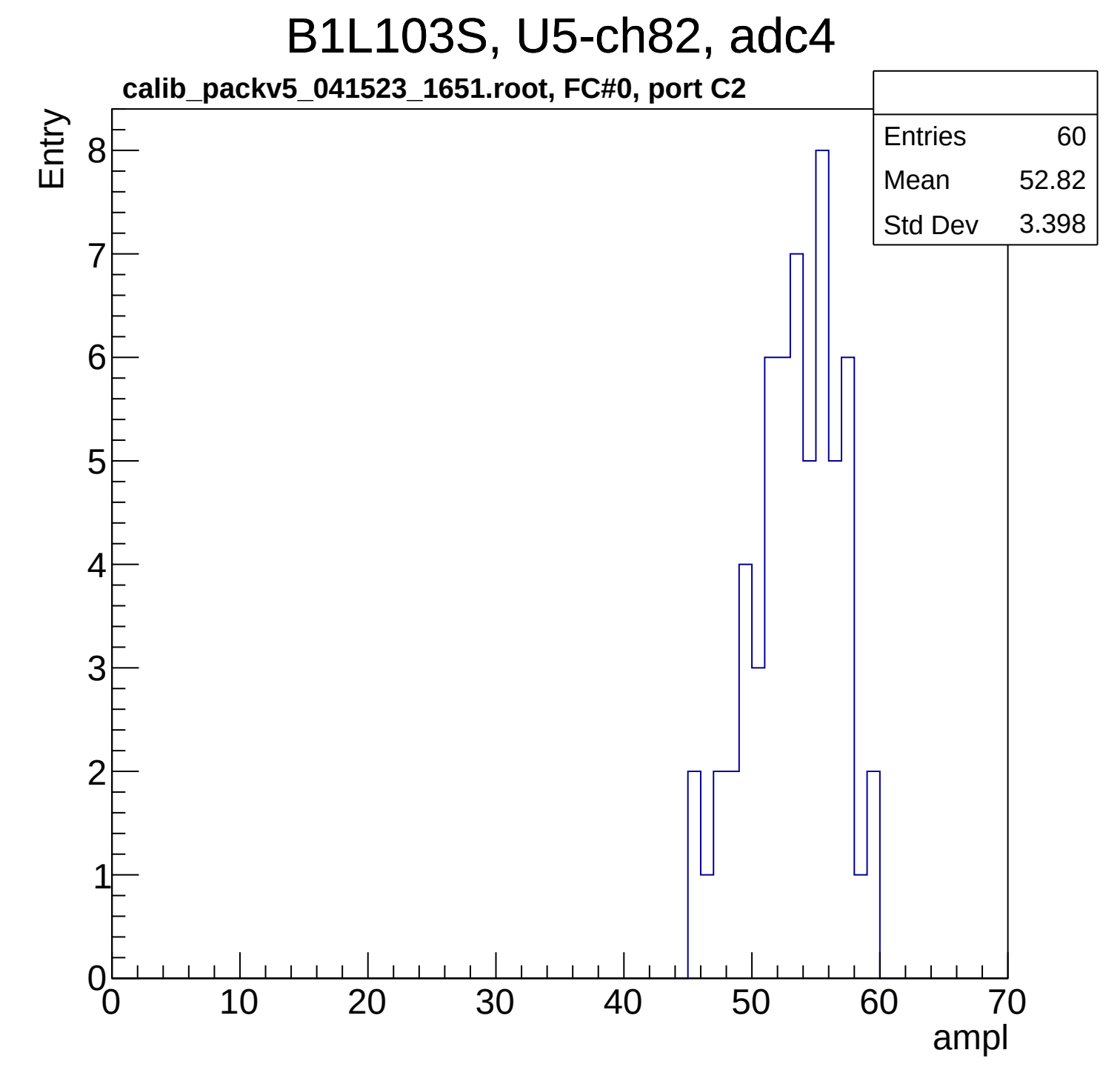
B1L103S, U5-ch82, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 52.82
Std Dev 3.398
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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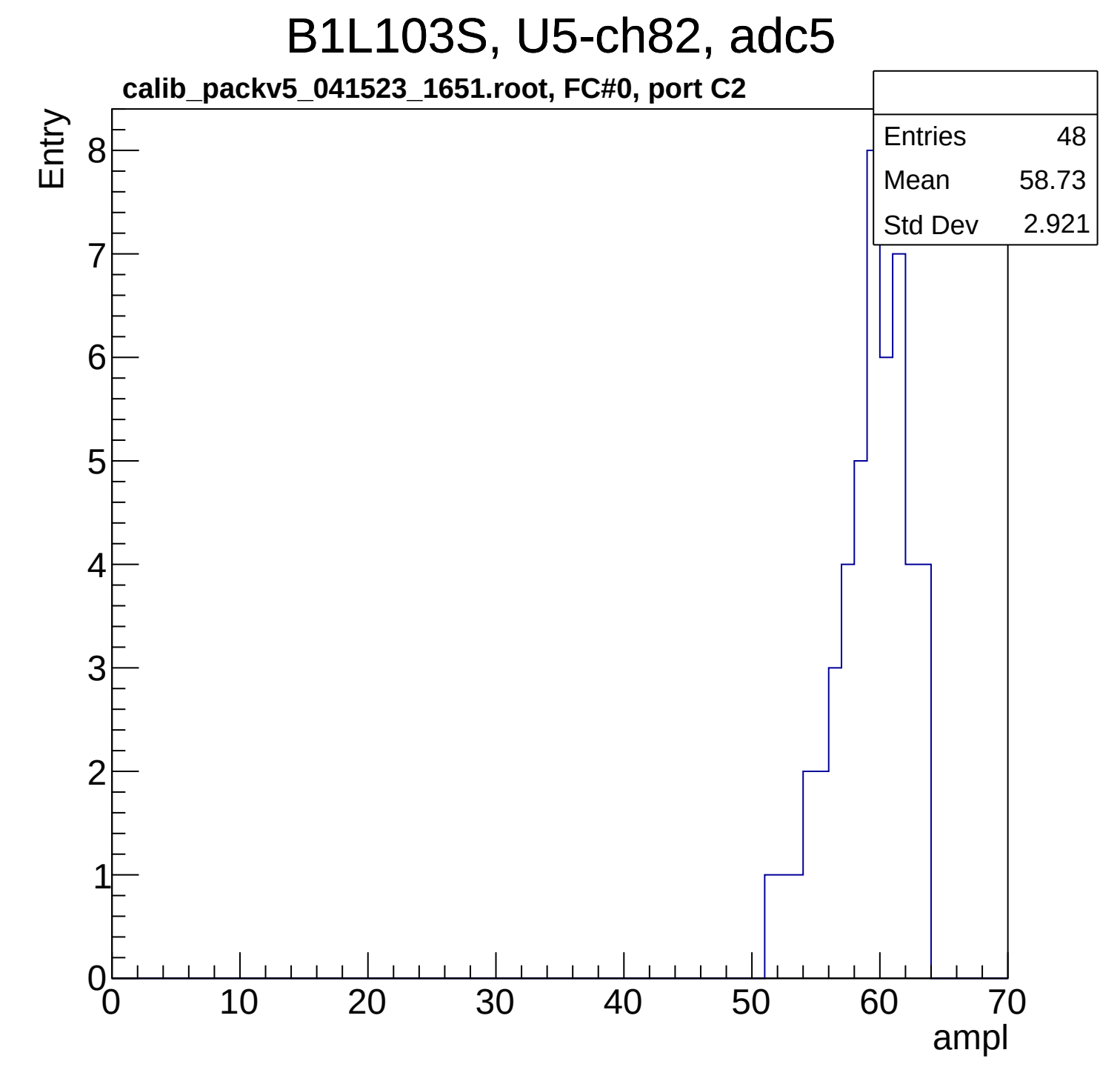
B1L103S, U5-ch82, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.73
Std Dev 2.921
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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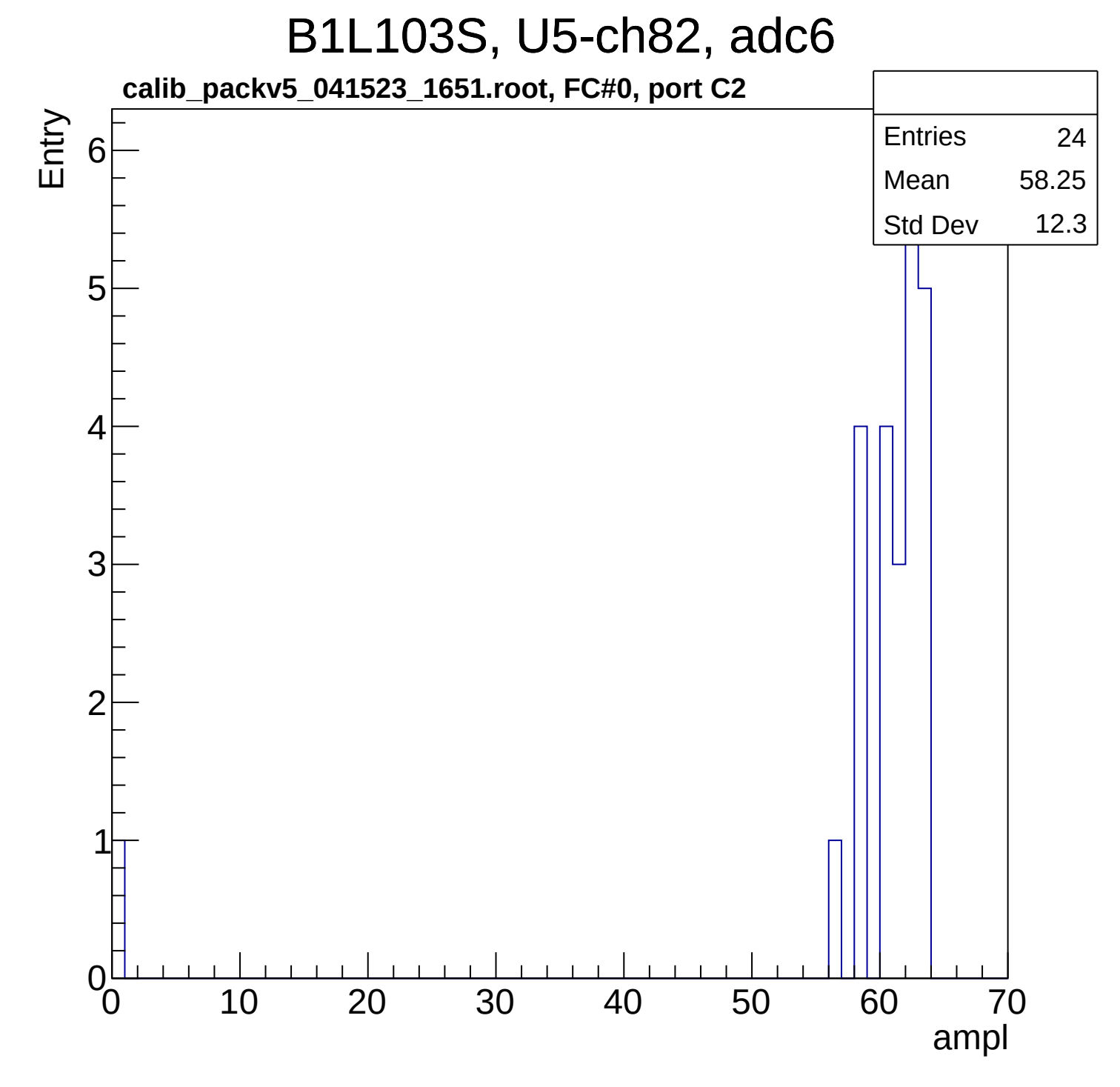
B1L103S, U5-ch82, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 58.25
Std Dev 12.3
Entry
ampl
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2
3
4
5
6
0
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20
30
40
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60
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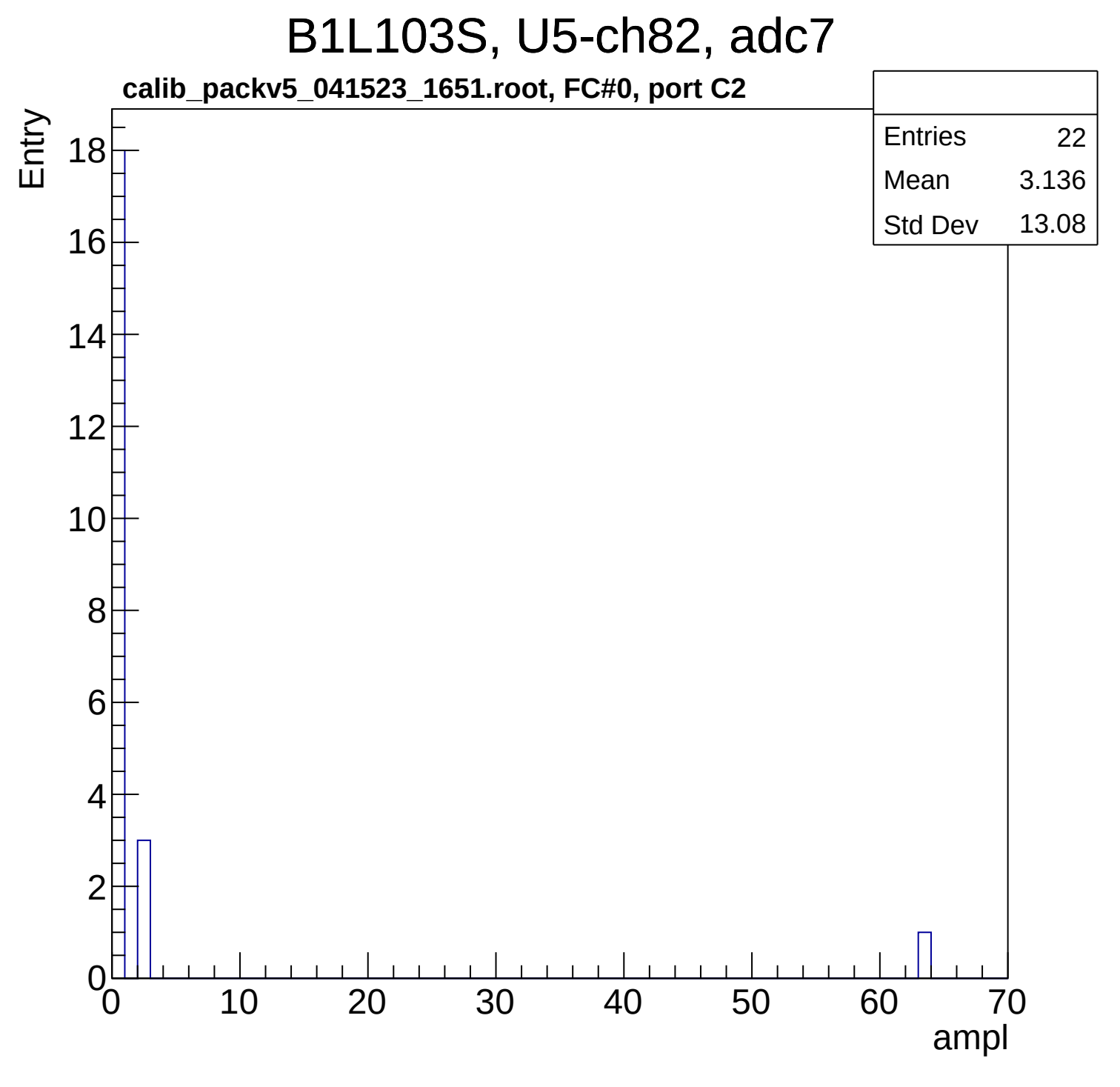
B1L103S, U5-ch82, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 3.136
Std Dev 13.08
Entry
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6
8
10
12
14
16
18
0
10
20
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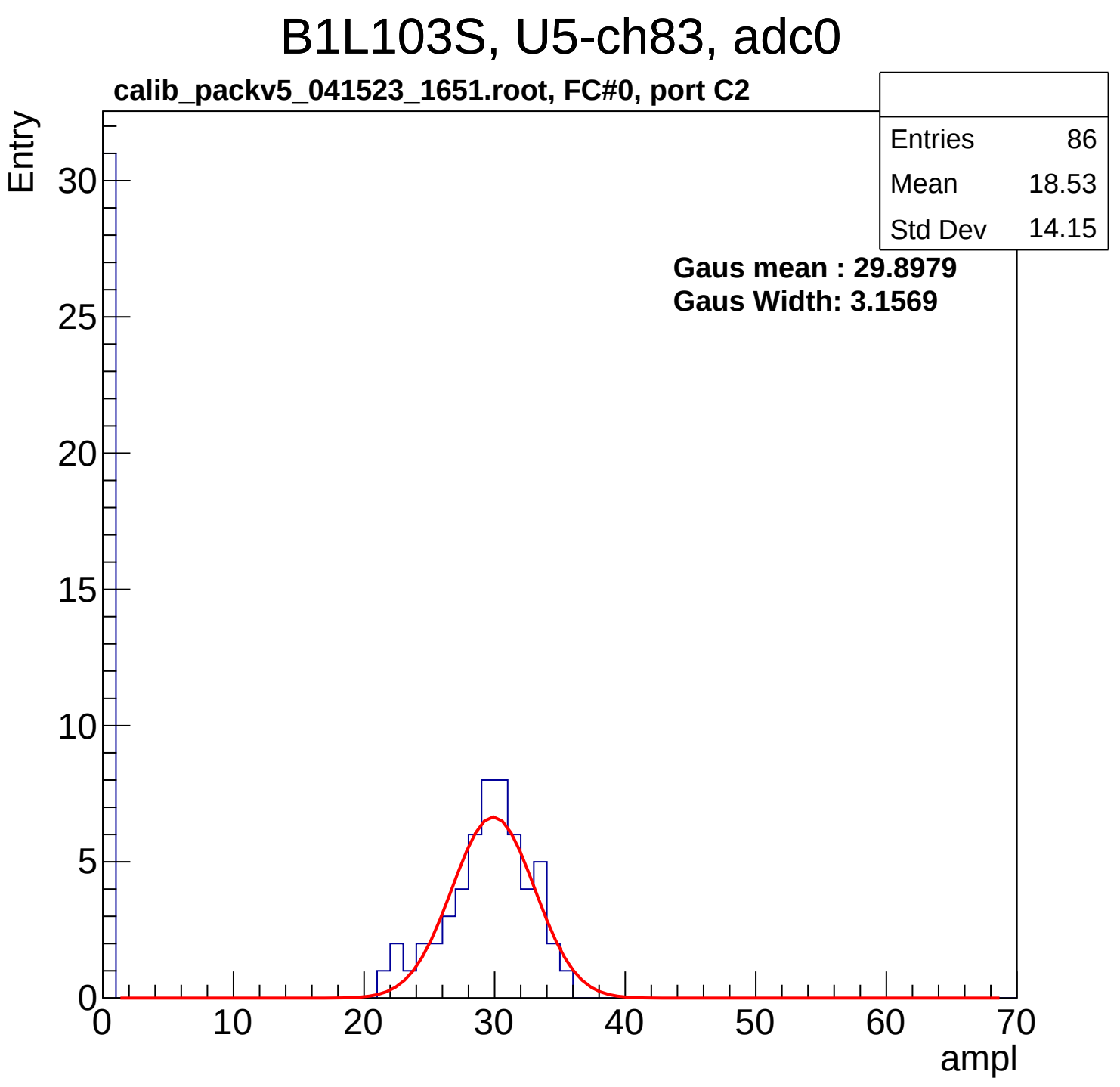
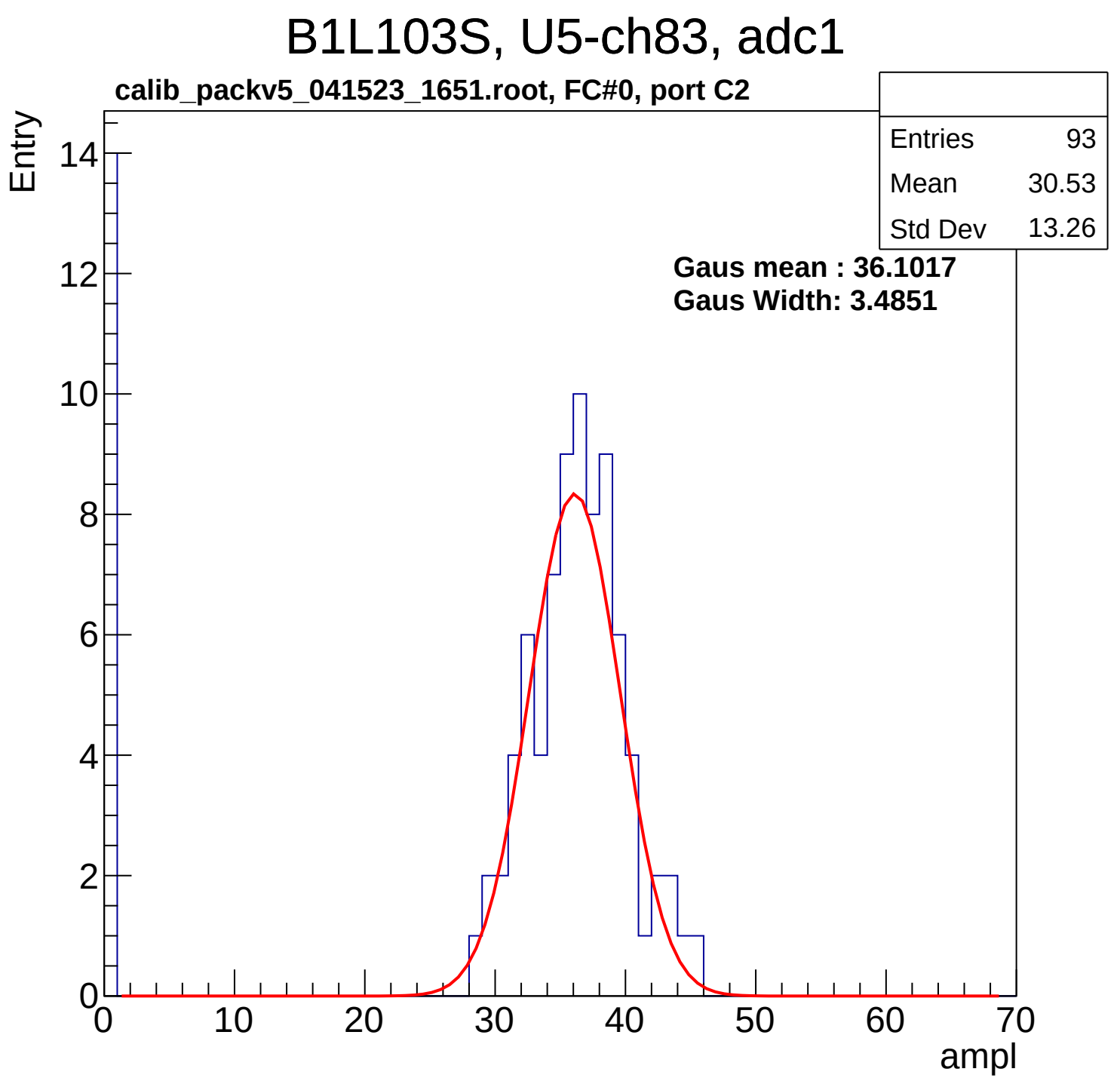
50
60
70
ampl


B1L103S, U5-ch83, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 18.53
Std Dev 14.15
Gaus mean : 29.8979
Gaus Width: 3.1569
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70


B1L103S, U5-ch83, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 30.53
Std Dev 13.26
Gaus mean : 36.1017
Gaus Width: 3.4851
Entry
ampl
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2
4
6
8
10
12
14
0
10
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40
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60
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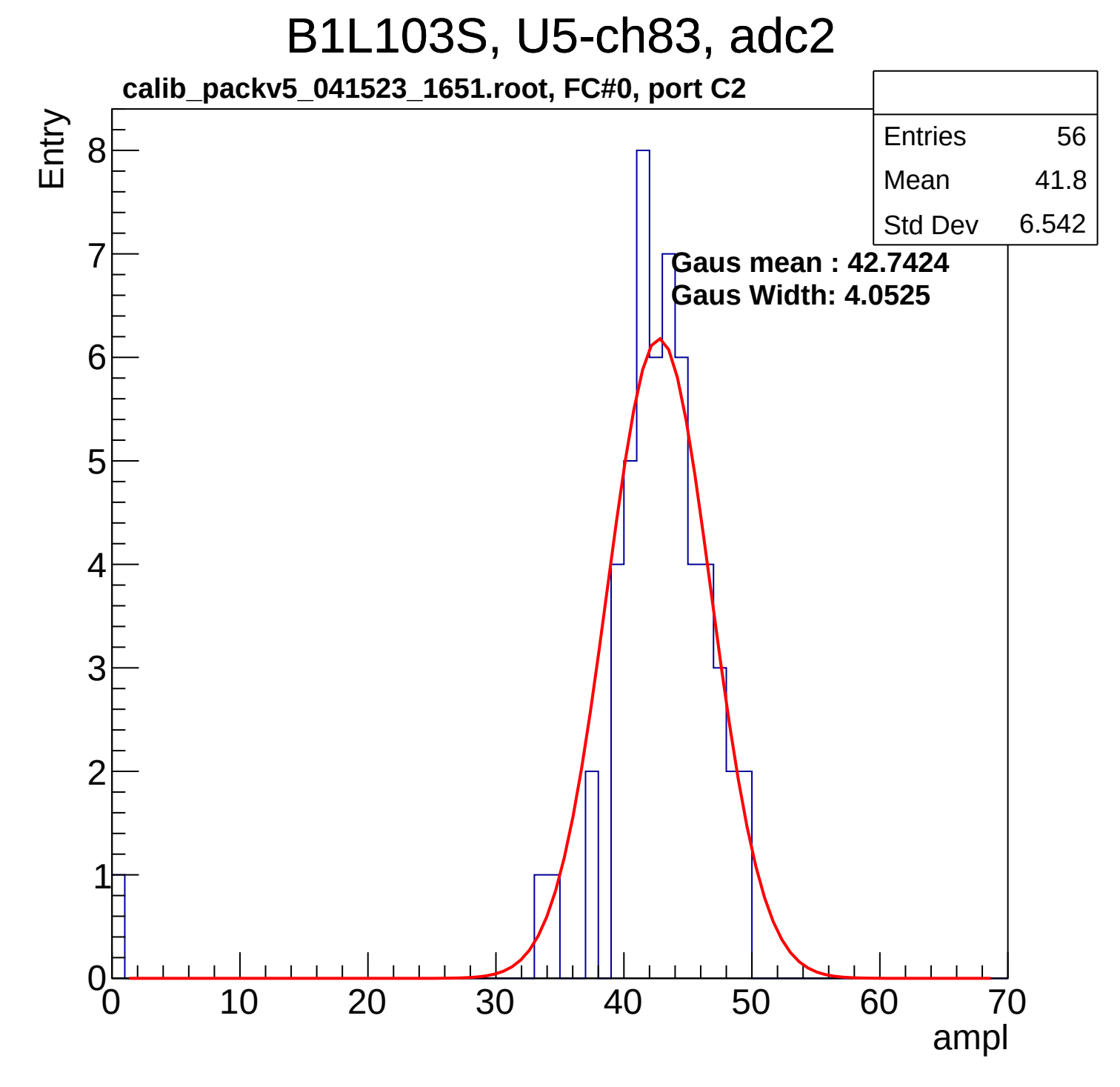
B1L103S, U5-ch83, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 41.8
Std Dev 6.542
Gaus mean : 42.7424
Gaus Width: 4.0525
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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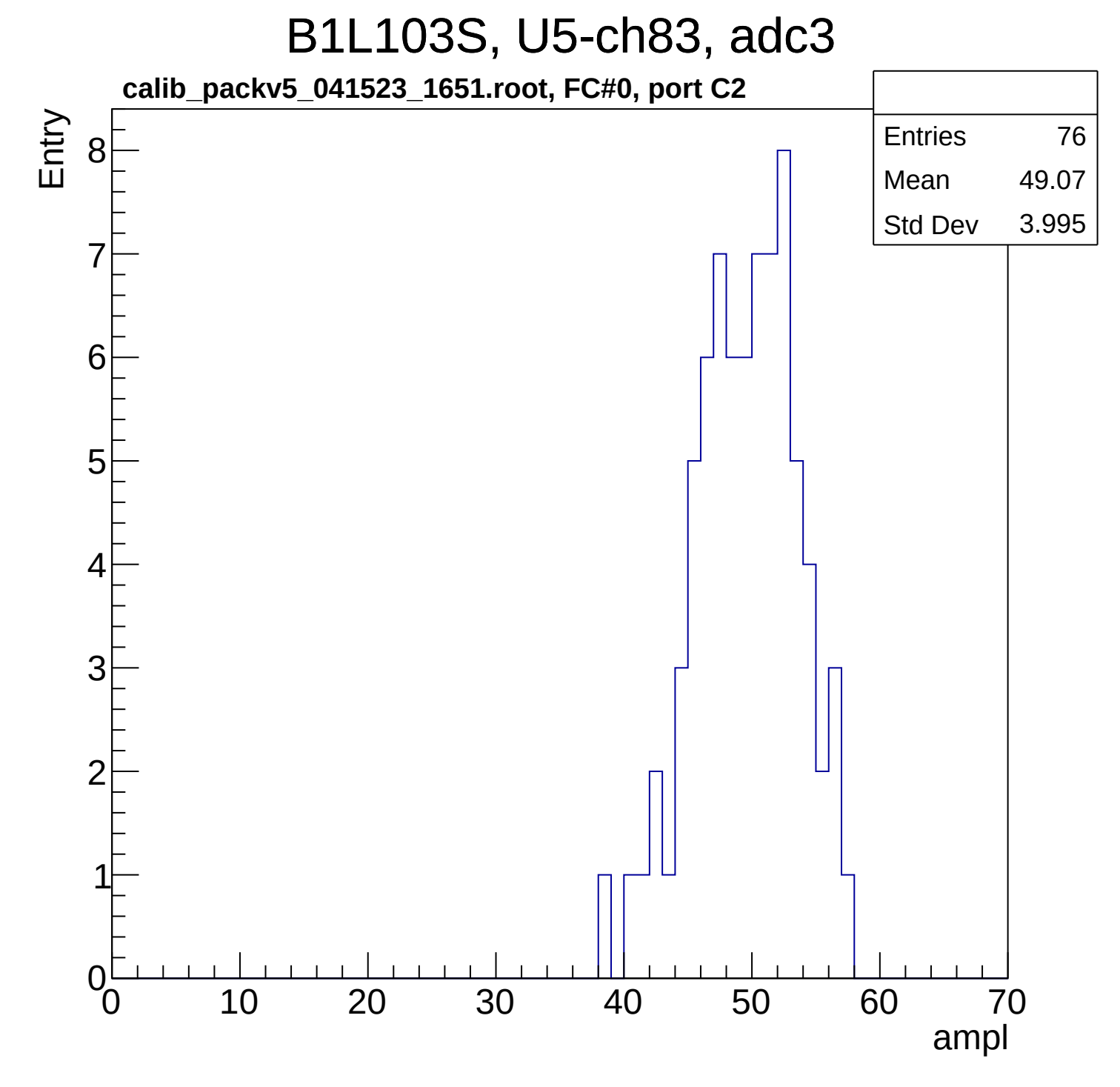
B1L103S, U5-ch83, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 49.07
Std Dev 3.995
Entry
ampl
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3
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0
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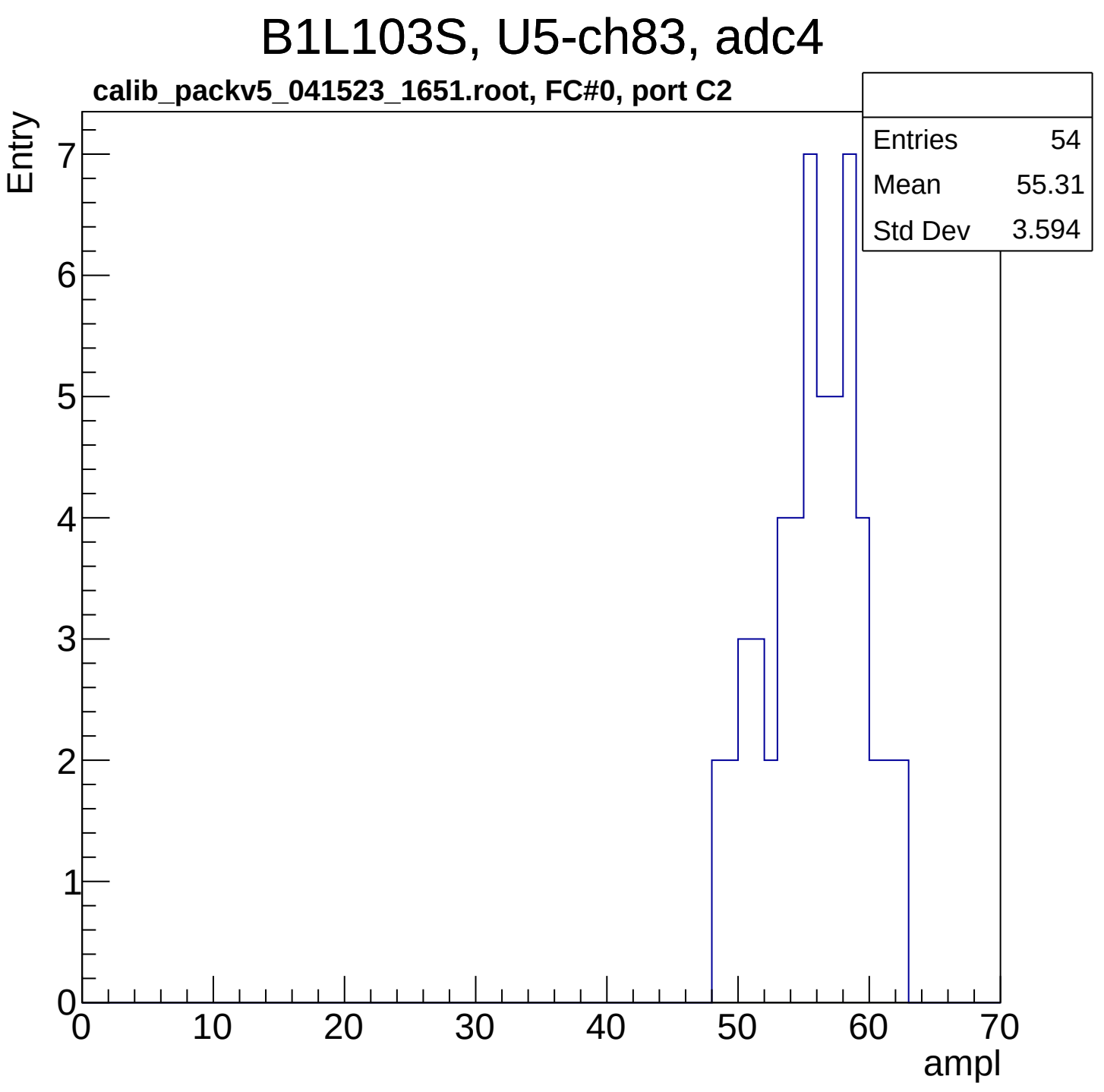
B1L103S, U5-ch83, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 55.31
Std Dev 3.594
Entry
ampl
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0
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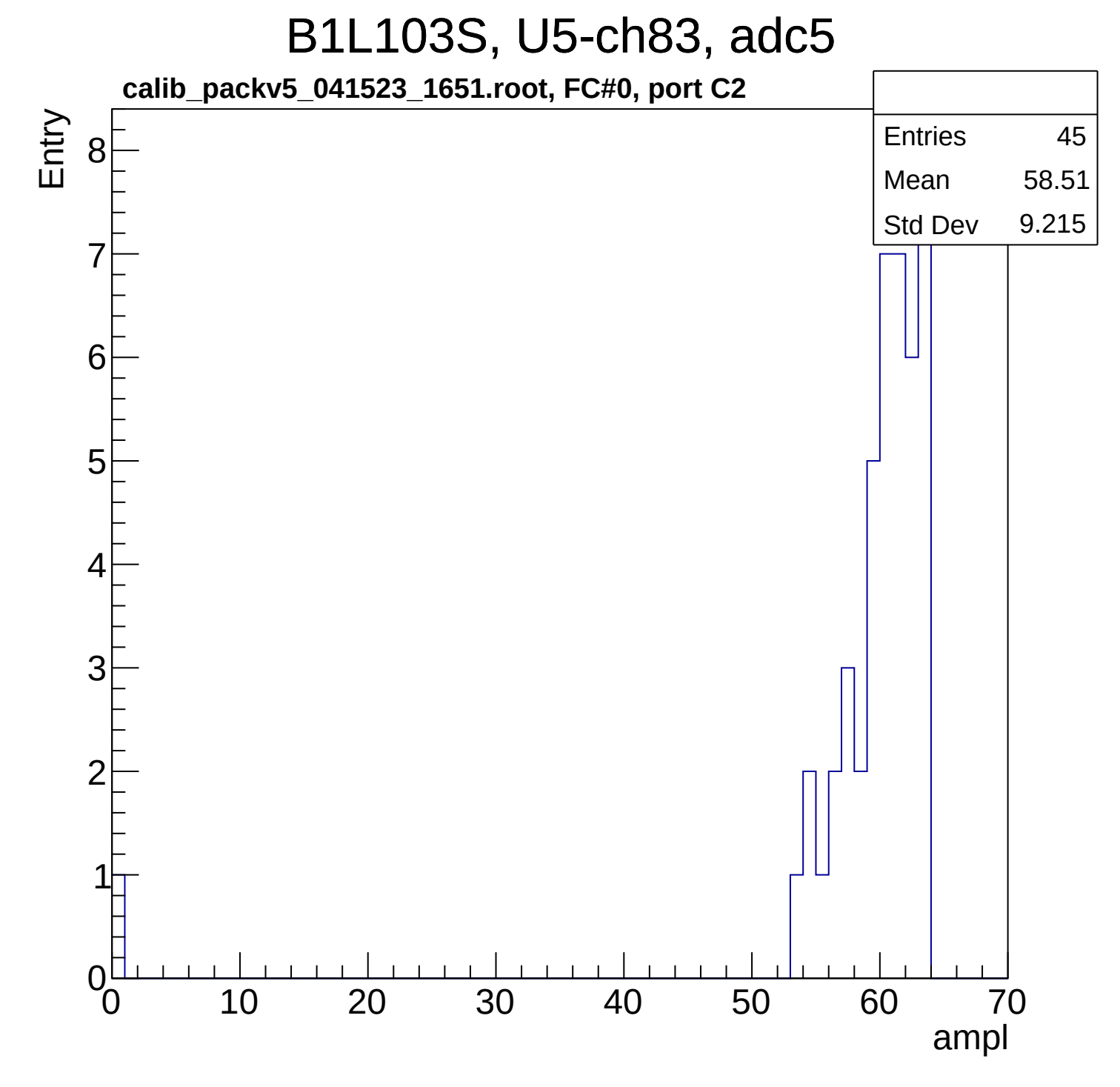
B1L103S, U5-ch83, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.51
Std Dev 9.215
Entry
ampl
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3
4
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0
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60
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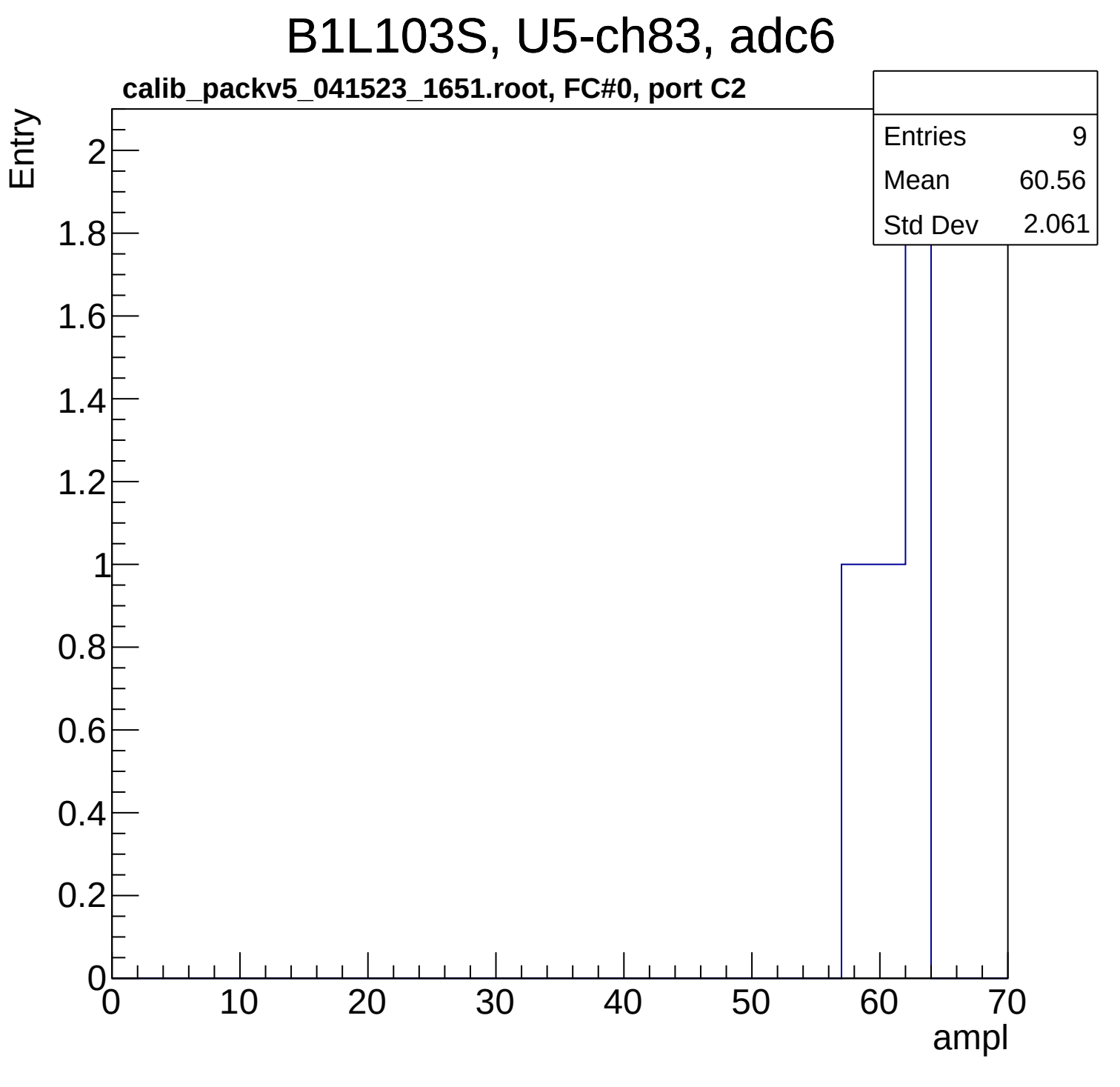
B1L103S, U5-ch83, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 60.56
Std Dev 2.061
Entry
ampl
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0.2
0.4
0.6
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1.2
1.4
1.6
1.8
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0
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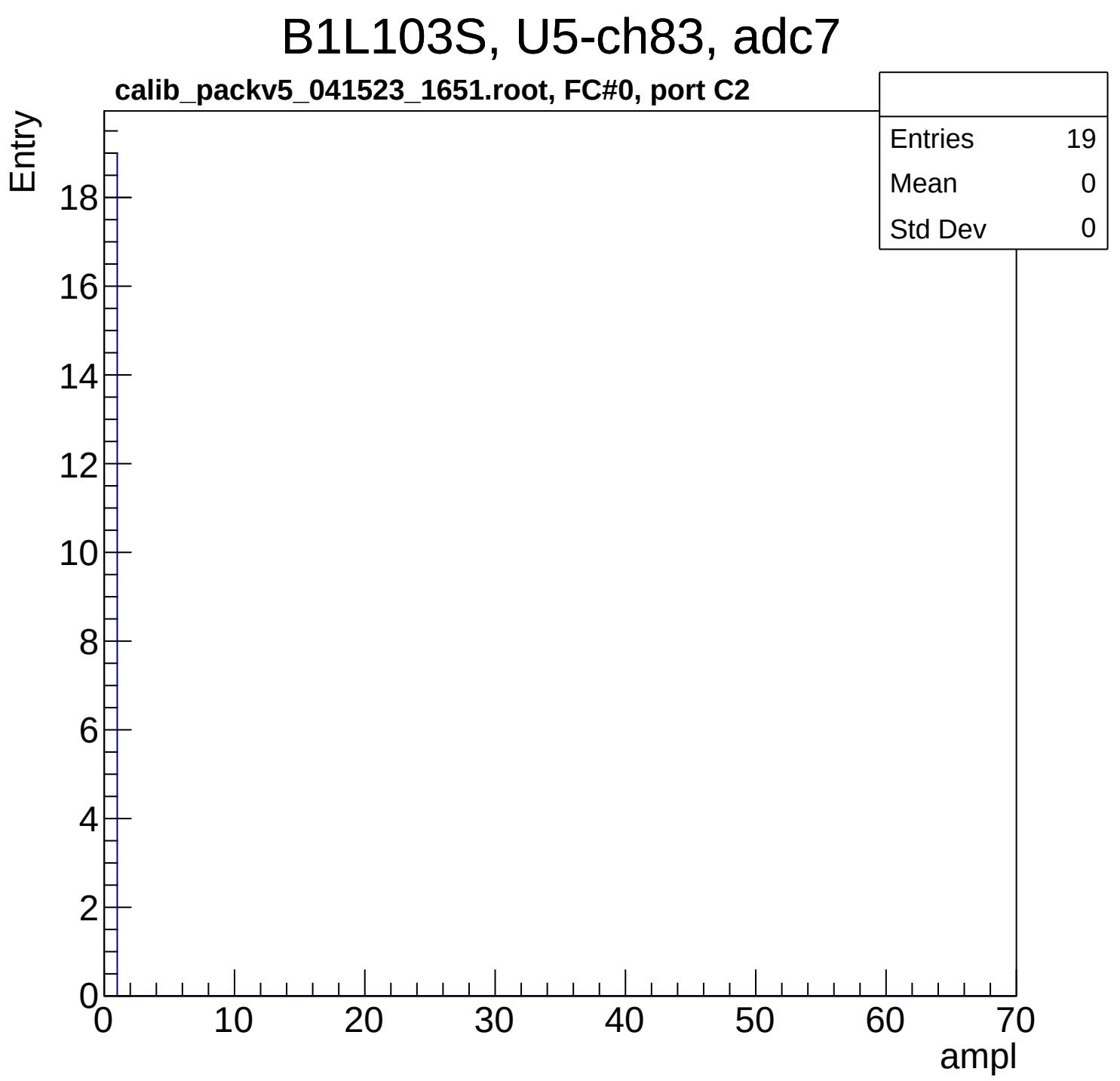
B1L103S, U5-ch83, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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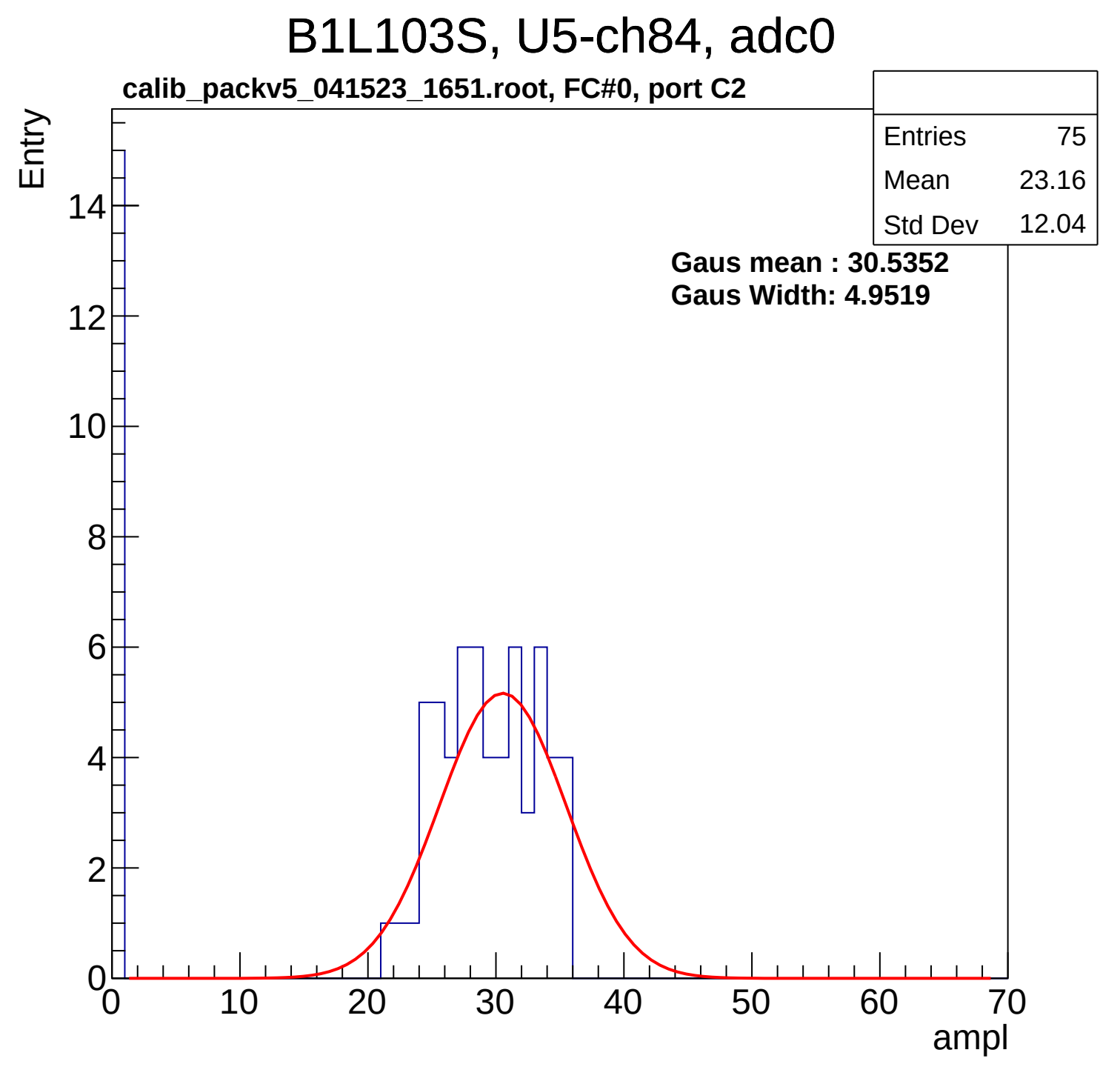
70
ampl


B1L103S, U5-ch84, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 23.16
Std Dev 12.04
Gaus mean : 30.5352
Gaus Width: 4.9519
Entry
ampl
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2
4
6
8
10
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14
0
10
20
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40
50
60
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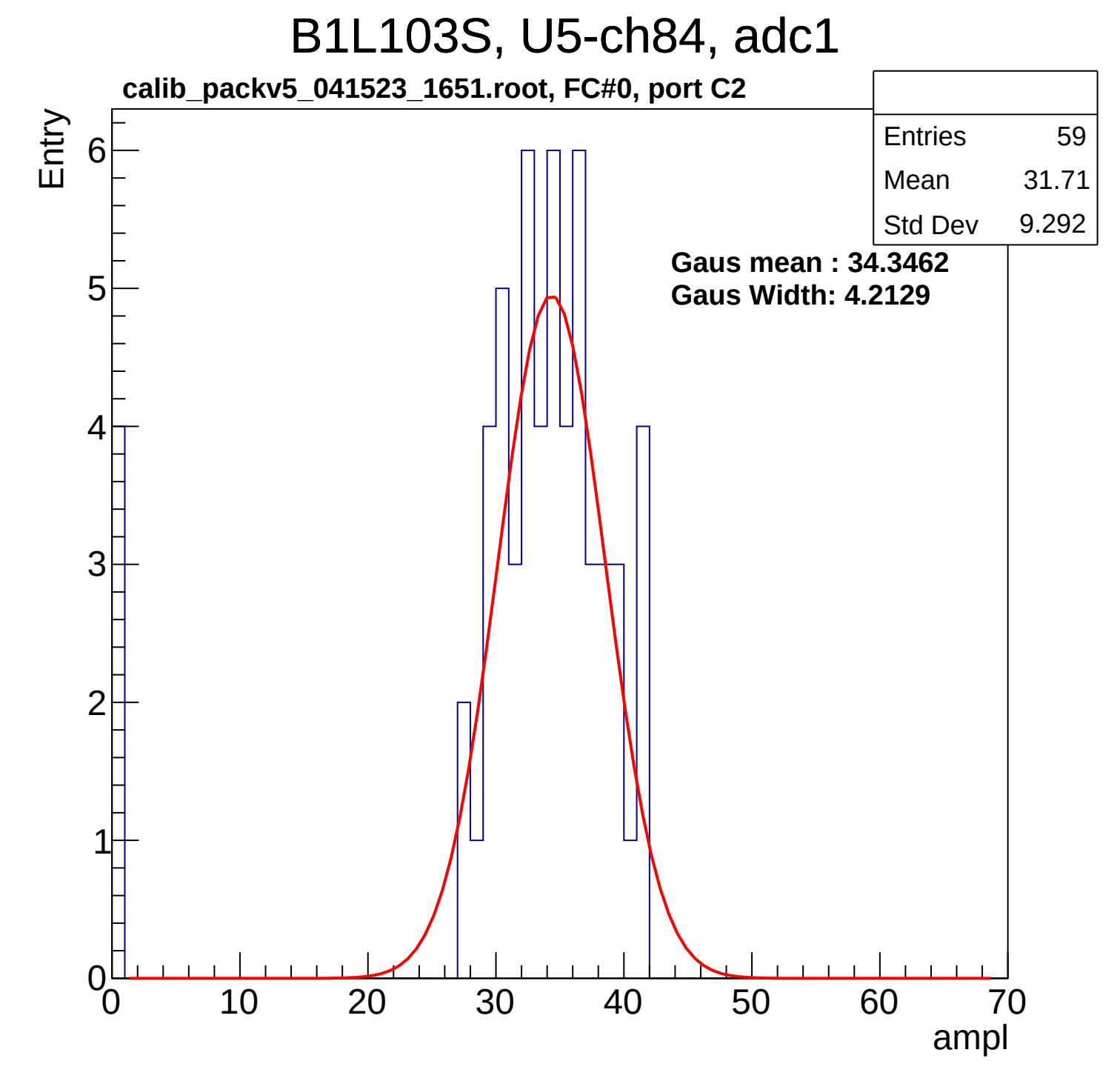
B1L103S, U5-ch84, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 31.71
Std Dev 9.292
Gaus mean : 34.3462
Gaus Width: 4.2129
Entry
ampl
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3
4
5
6
0
10
20
30
40
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60
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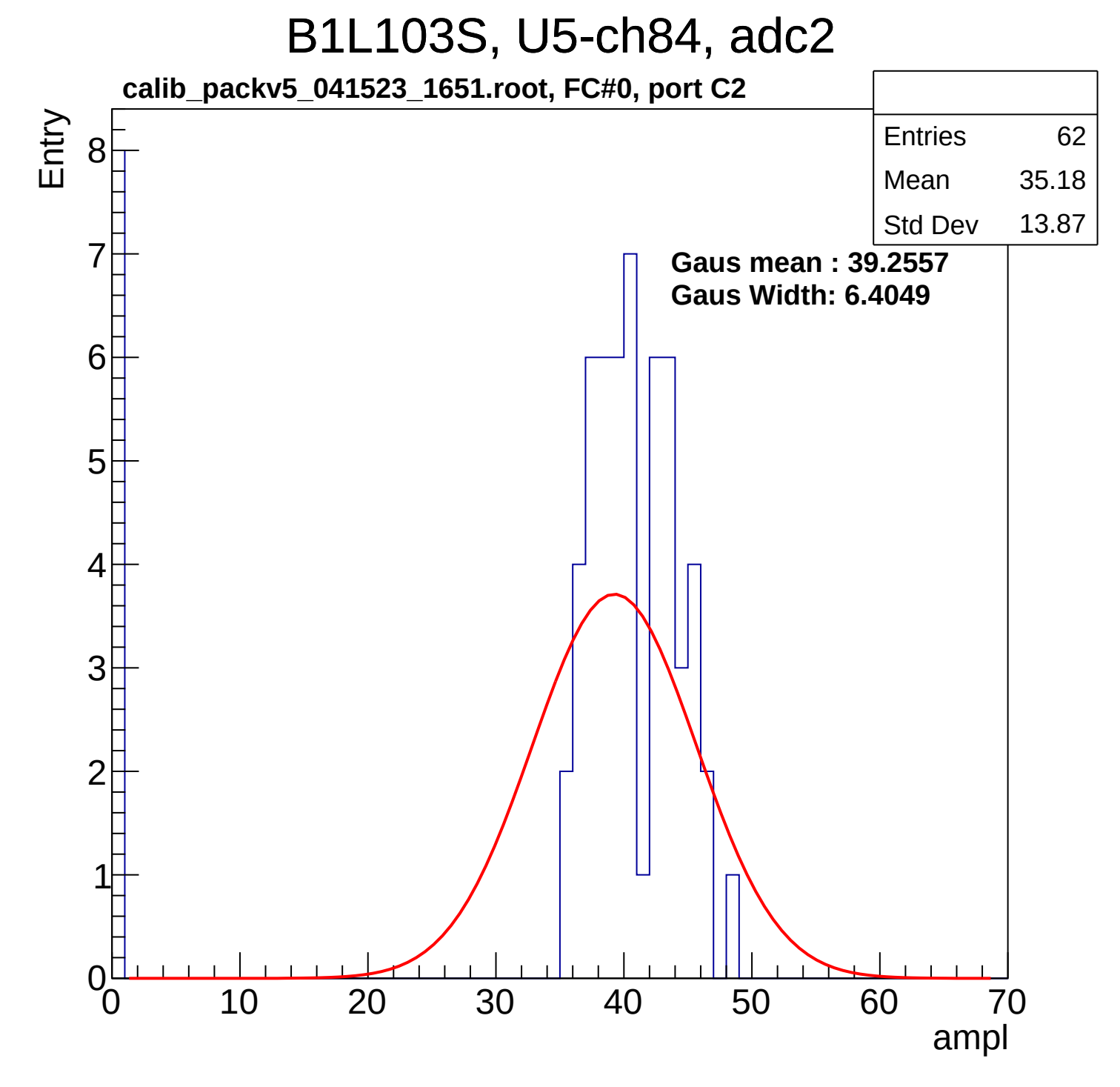
B1L103S, U5-ch84, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 35.18
Std Dev 13.87
Gaus mean : 39.2557
Gaus Width: 6.4049
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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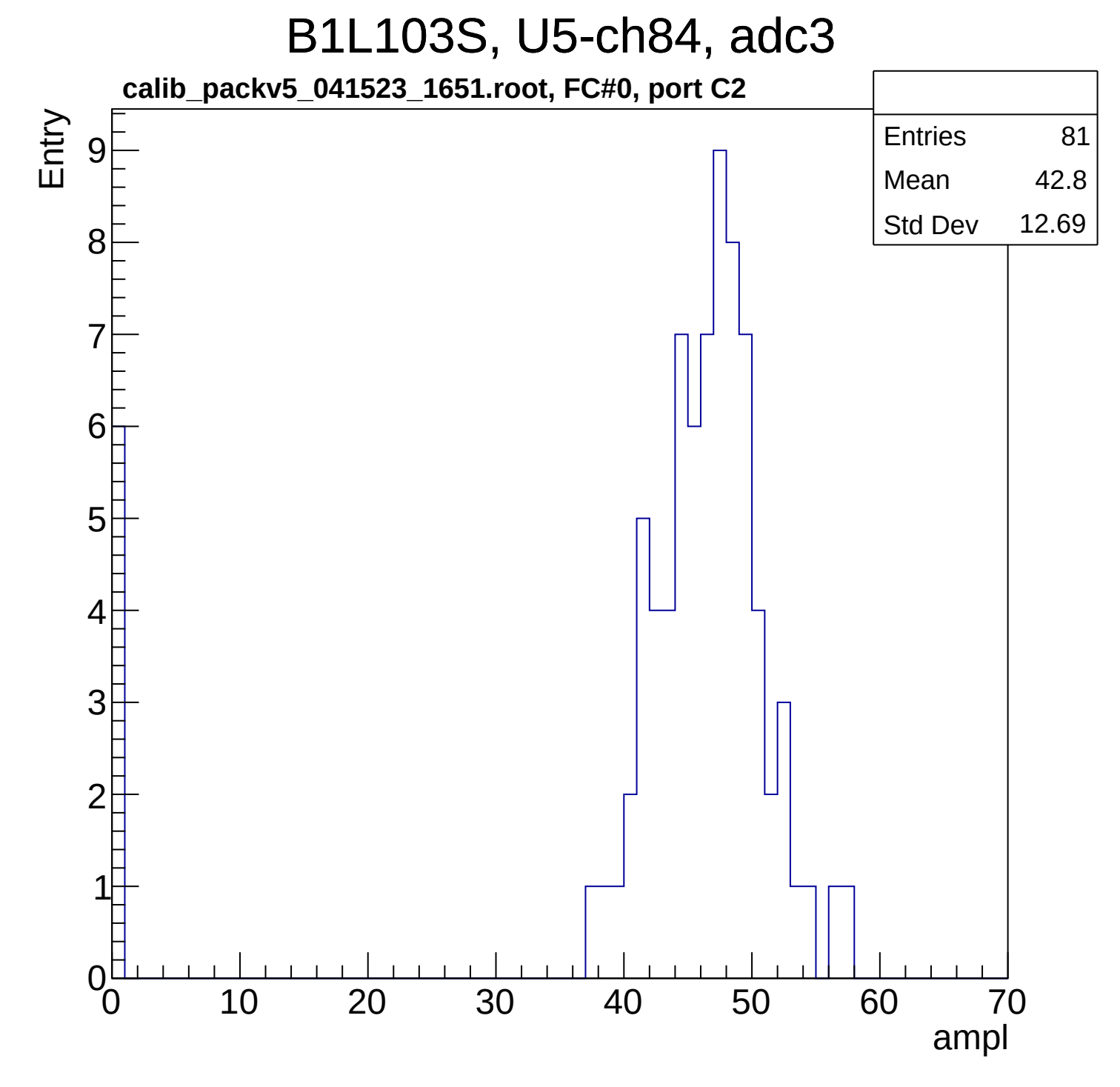
B1L103S, U5-ch84, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 42.8
Std Dev 12.69
Entry
ampl
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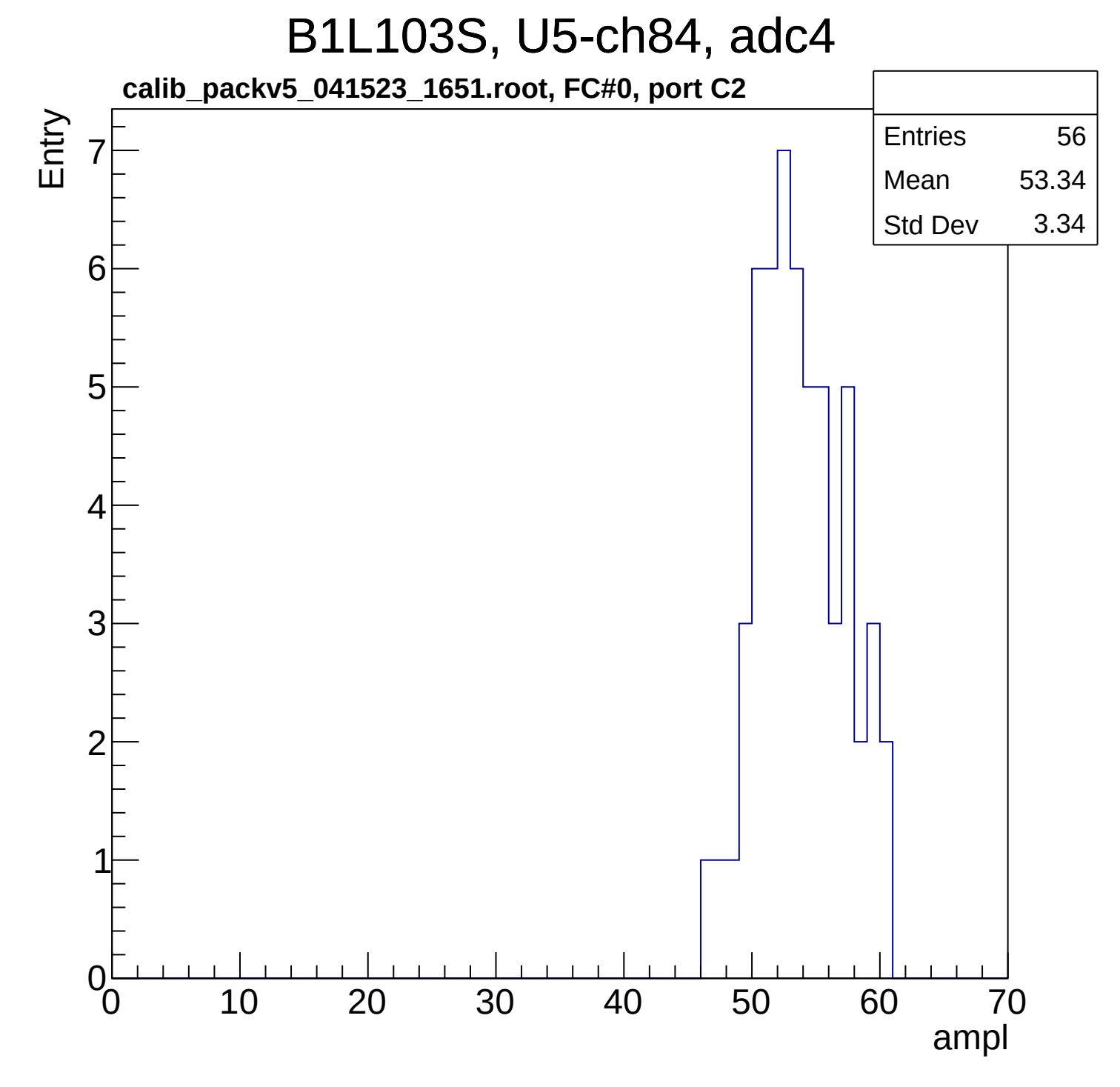
B1L103S, U5-ch84, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 53.34
Std Dev 3.34
Entry
ampl
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4
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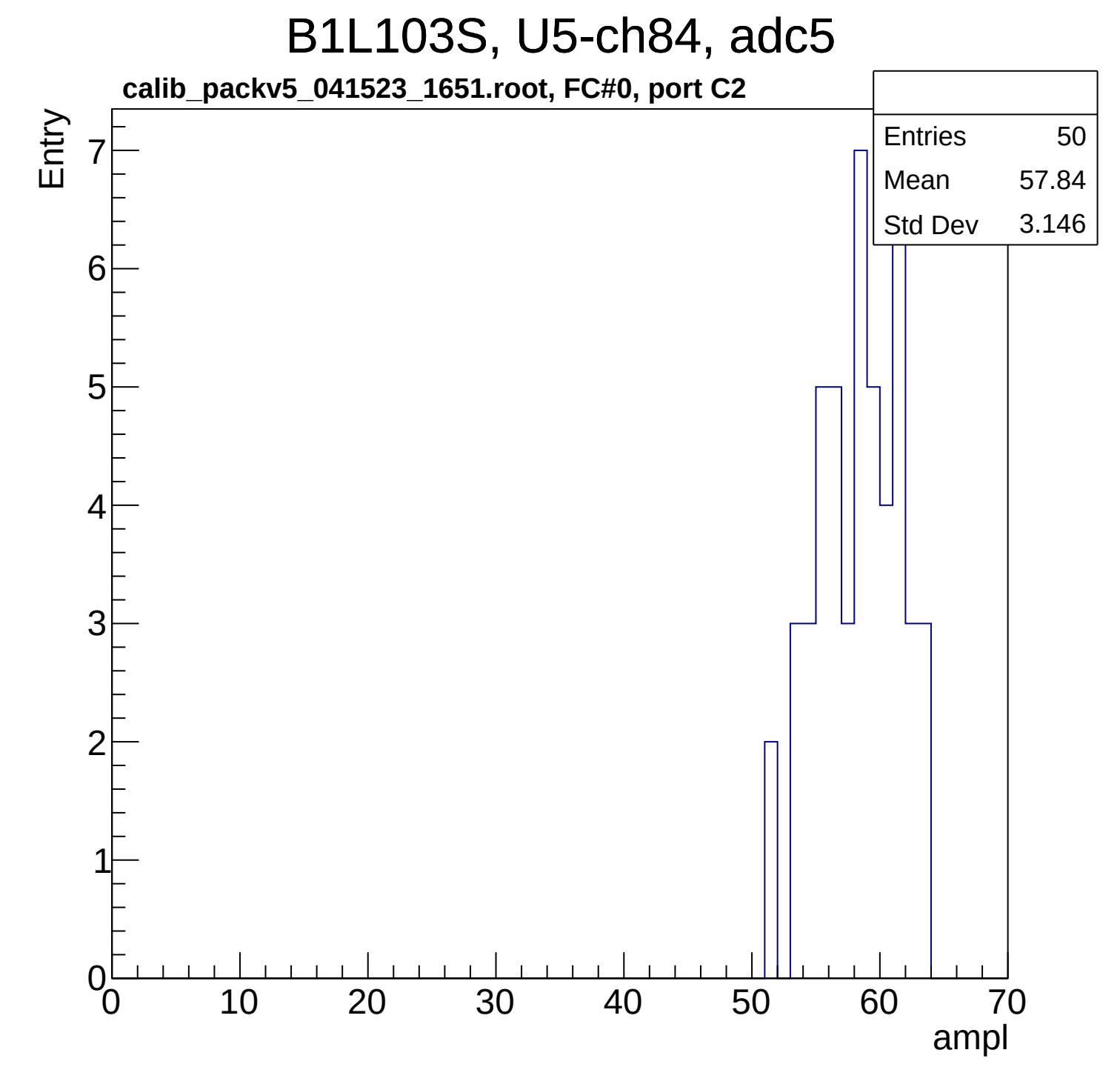
B1L103S, U5-ch84, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 57.84
Std Dev 3.146
Entry
ampl
0
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3
4
5
6
7
0
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20
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60
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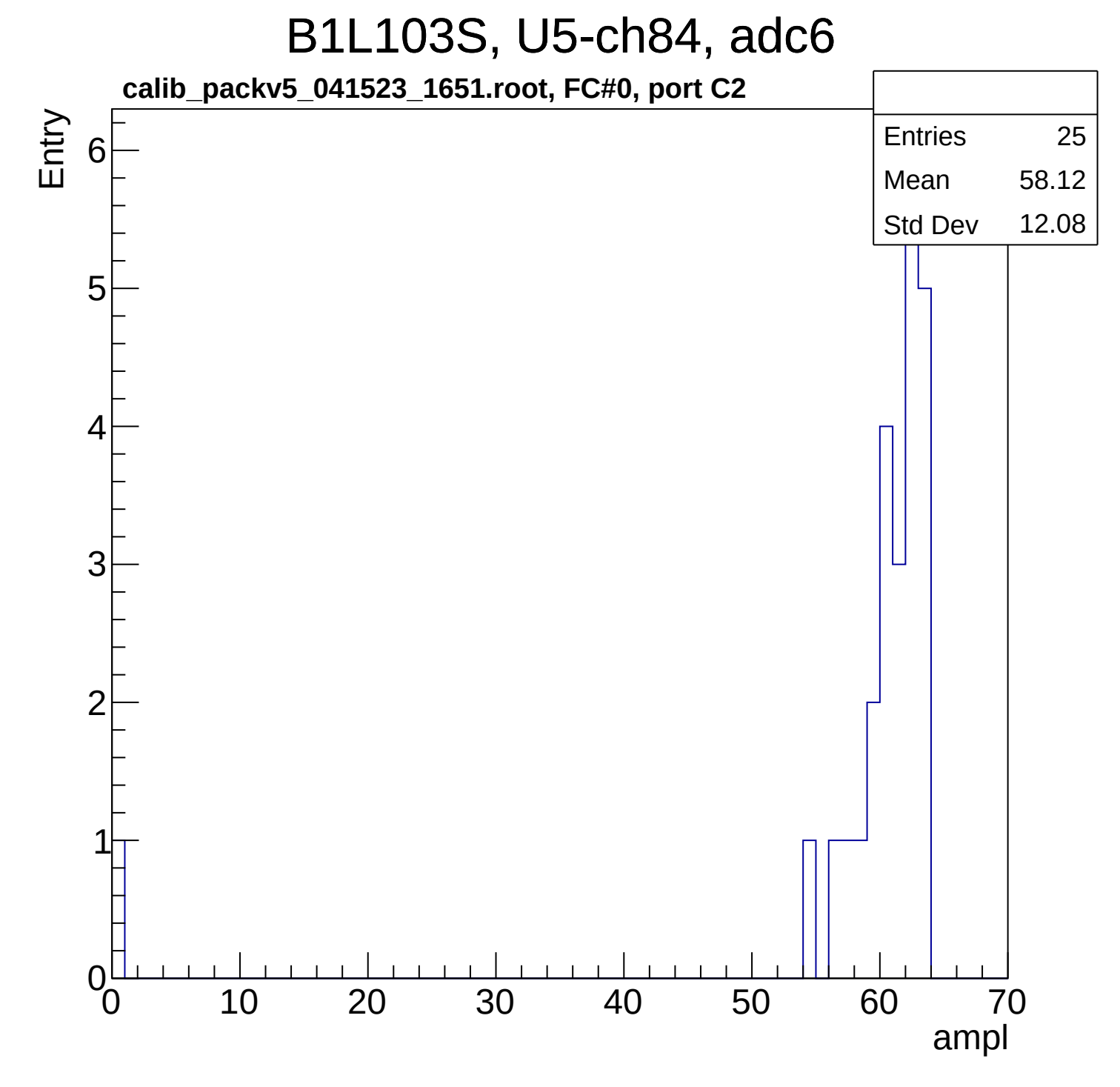
B1L103S, U5-ch84, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 58.12
Std Dev 12.08
Entry
ampl
0
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2
3
4
5
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0
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40
50
60
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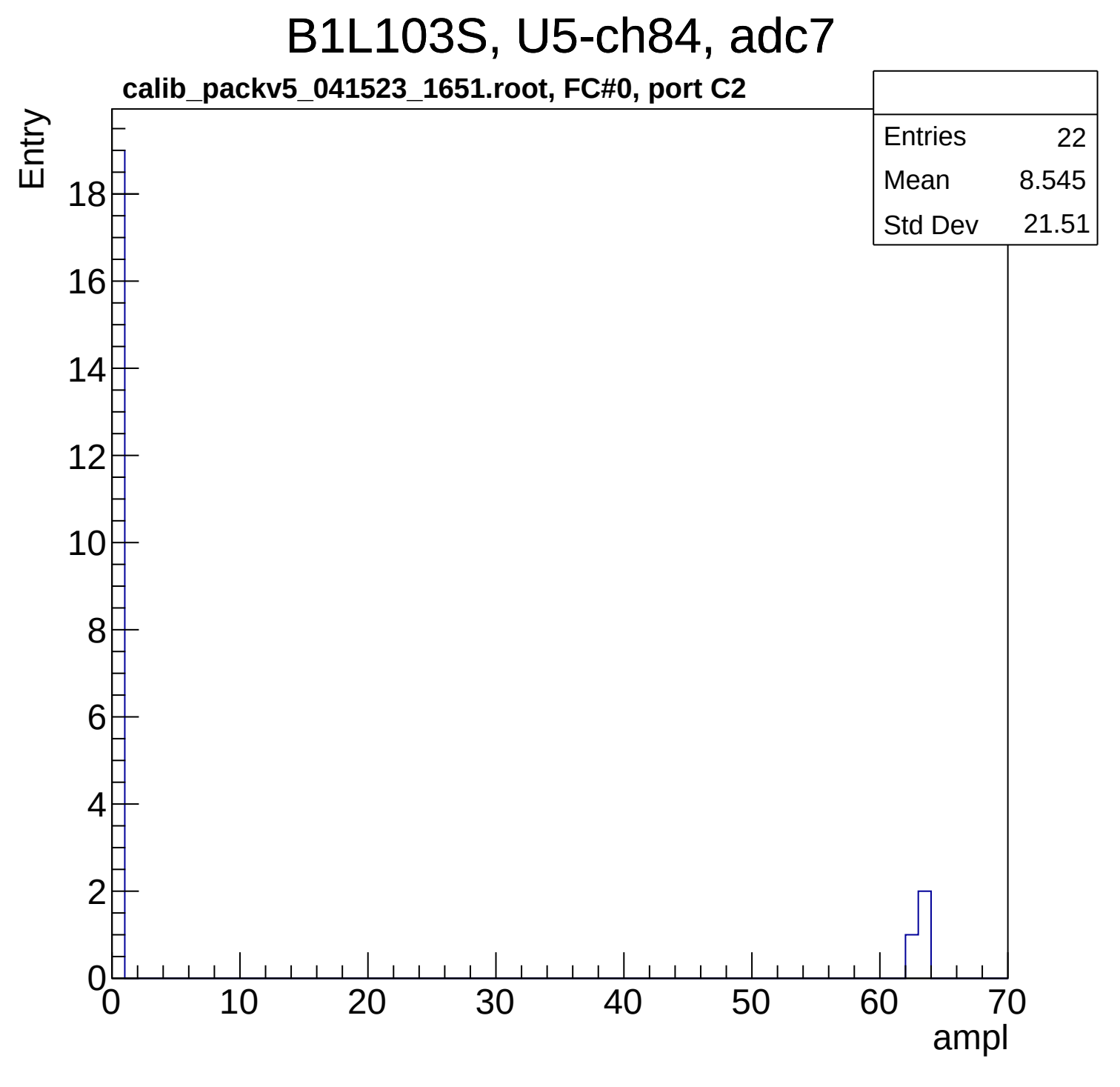
B1L103S, U5-ch84, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.545
Std Dev 21.51
Entry
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14
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30
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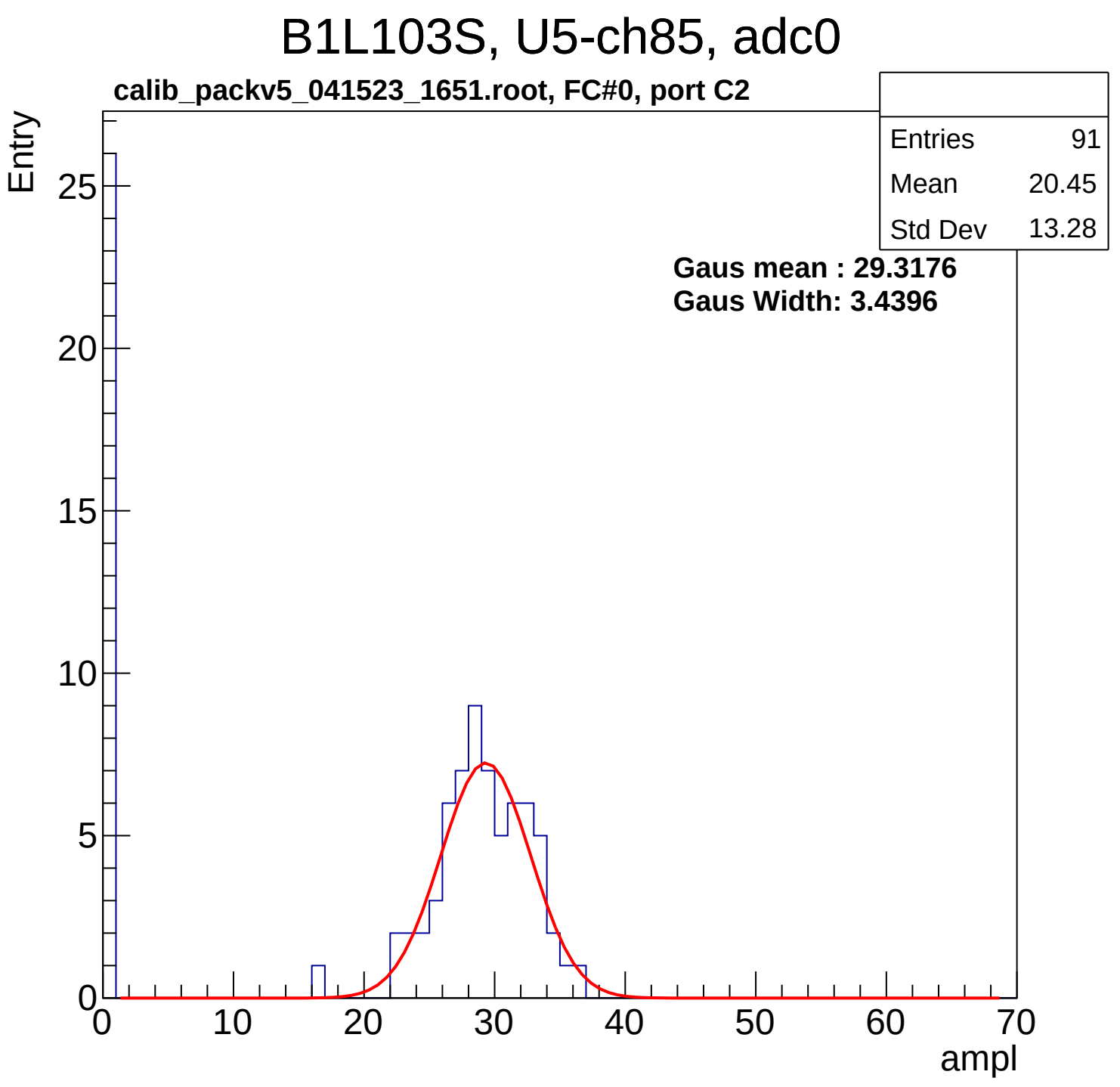
50
60
70
ampl


B1L103S, U5-ch85, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 20.45
Std Dev 13.28
Gaus mean : 29.3176
Gaus Width: 3.4396
Entry
ampl
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10
15
20
25
0
10
20
30
40
50
60
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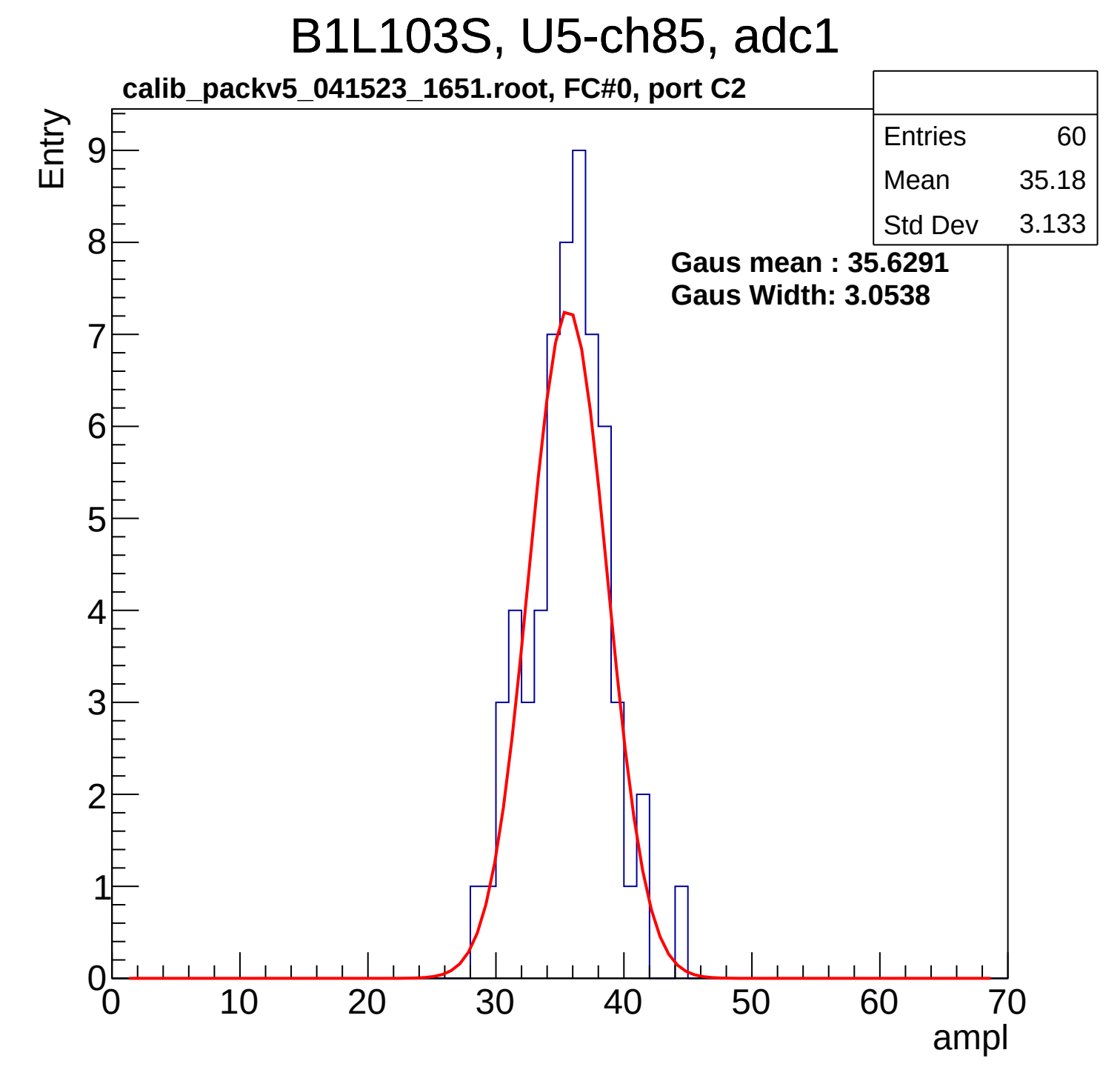
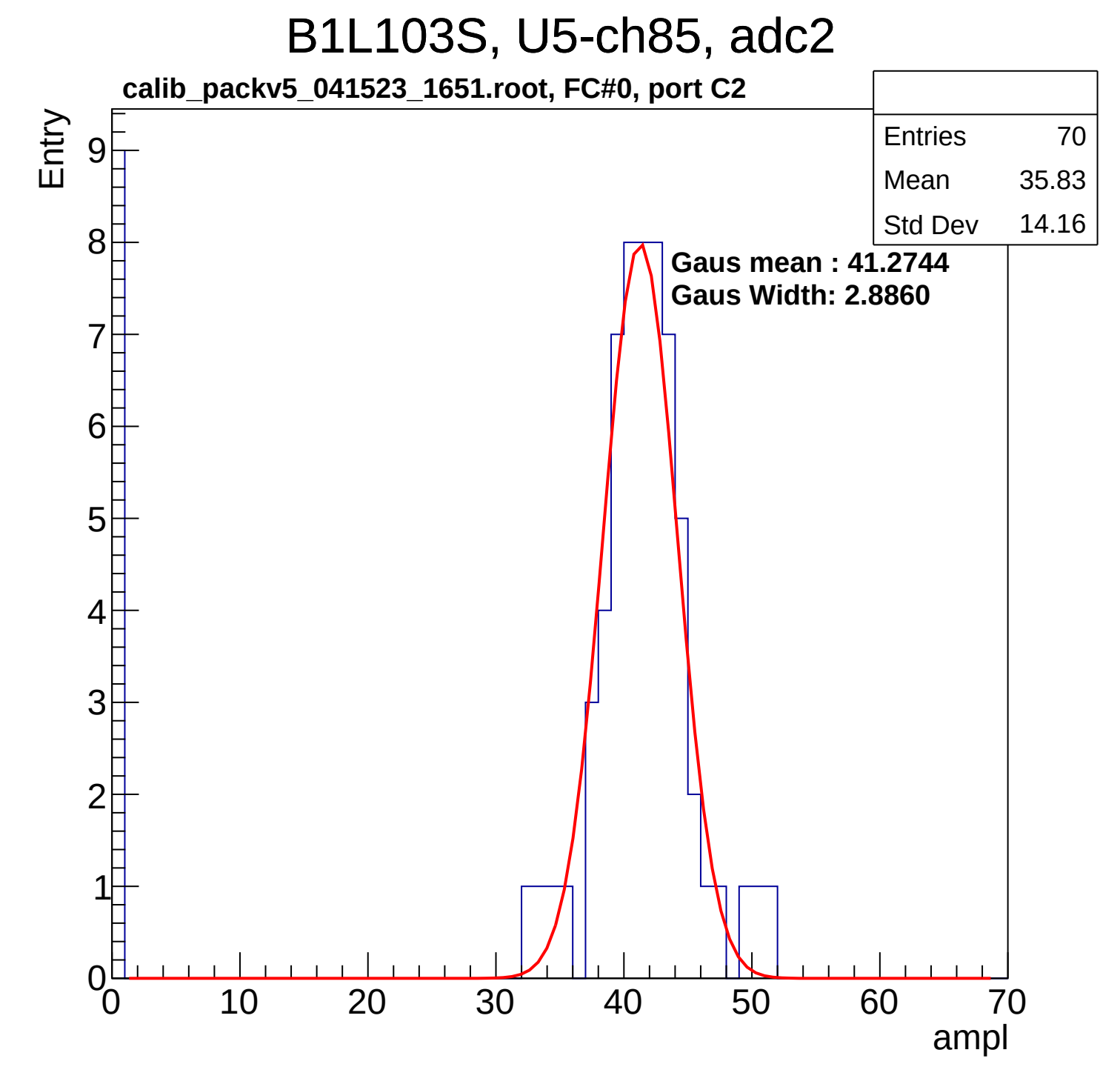

B1L103S, U5-ch85, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 35.18
Std Dev 3.133
Gaus mean : 35.6291
Gaus Width: 3.0538
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U5-ch85, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 35.83
Std Dev 14.16
Gaus mean : 41.2744
Gaus Width: 2.8860
Entry
ampl
0
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2
3
4
5
6
7
8
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0
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40
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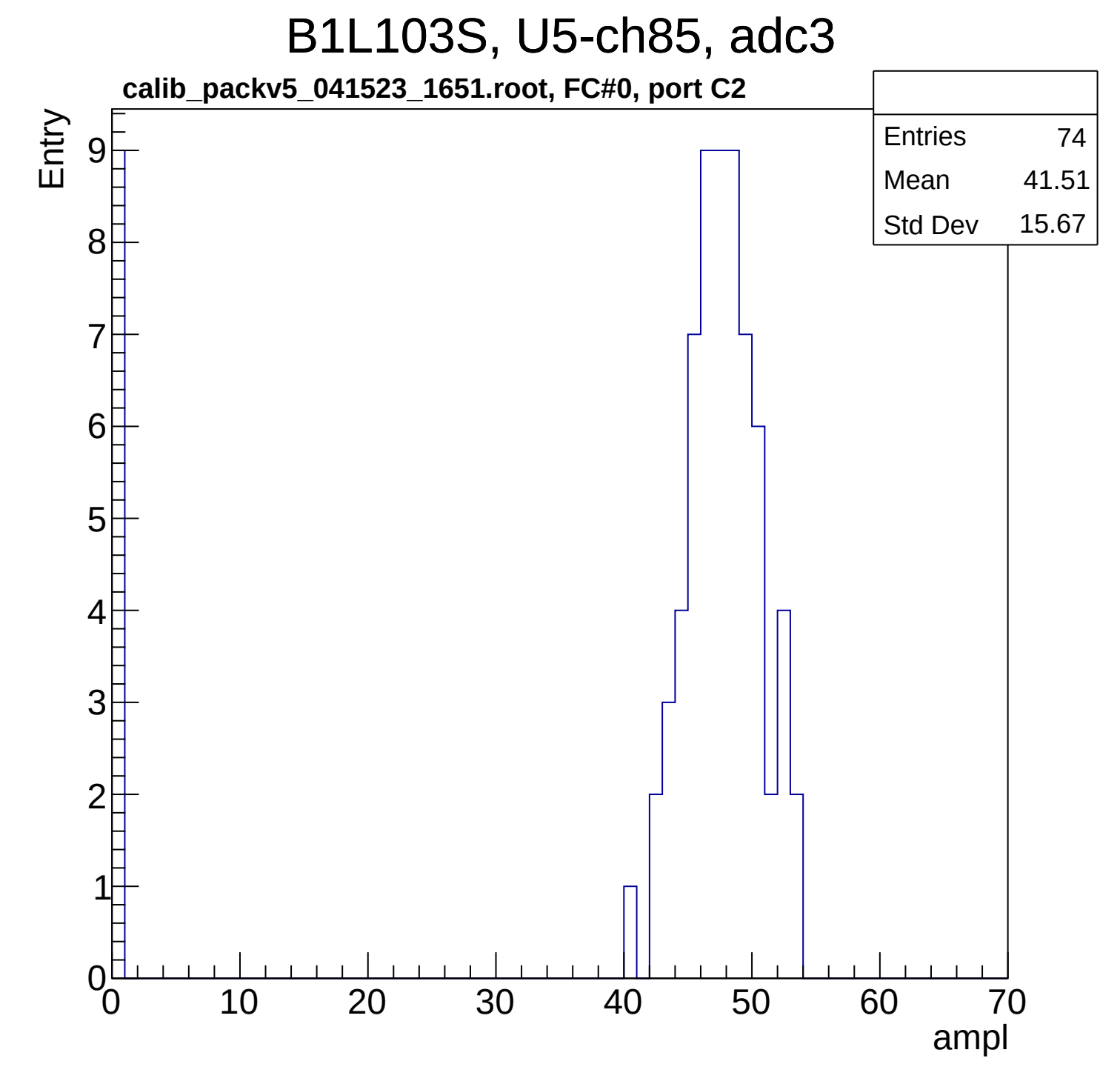
B1L103S, U5-ch85, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 41.51
Std Dev 15.67
Entry
ampl
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1
2
3
4
5
6
7
8
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0
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40
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60
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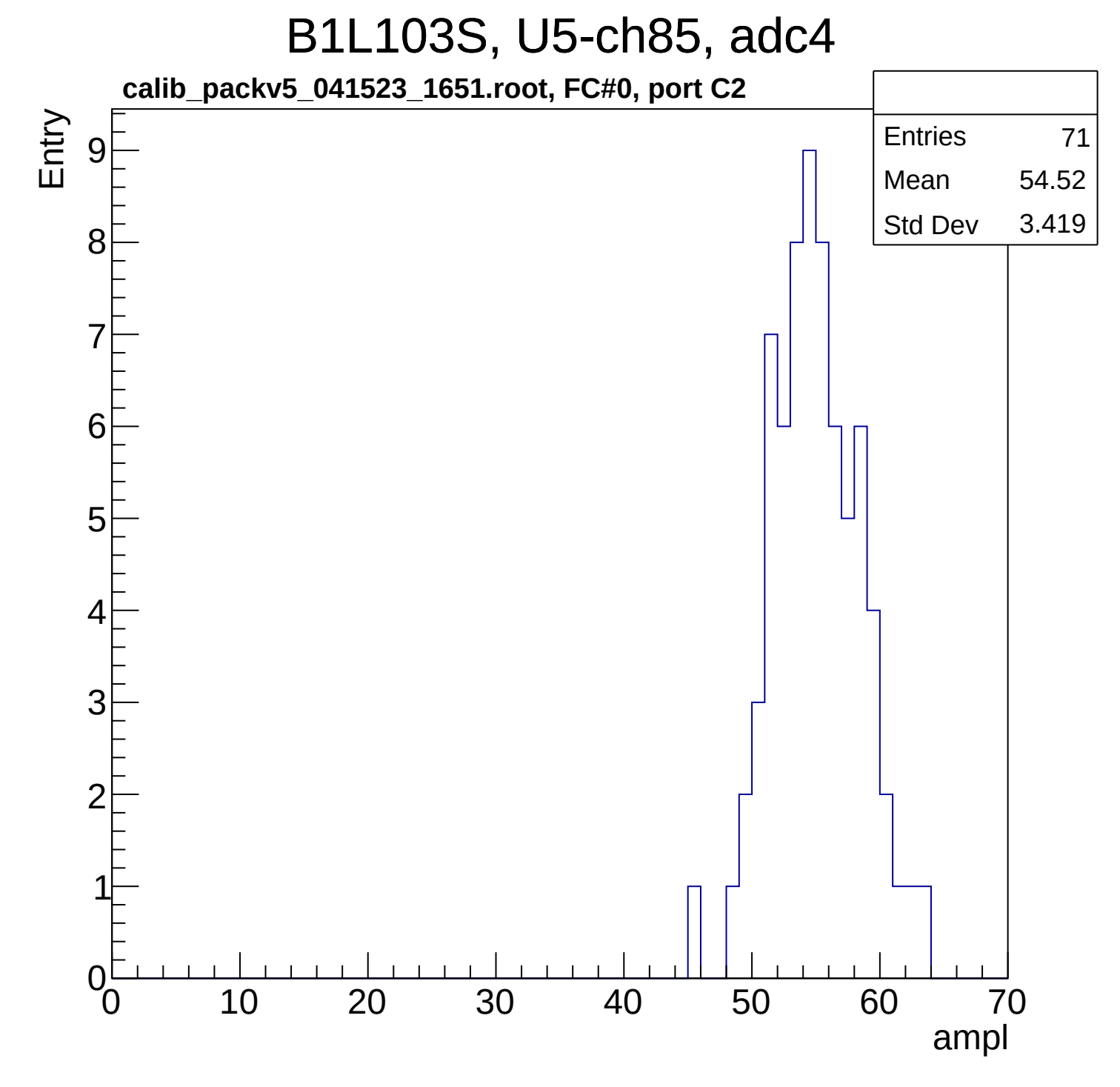
B1L103S, U5-ch85, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 54.52
Std Dev 3.419
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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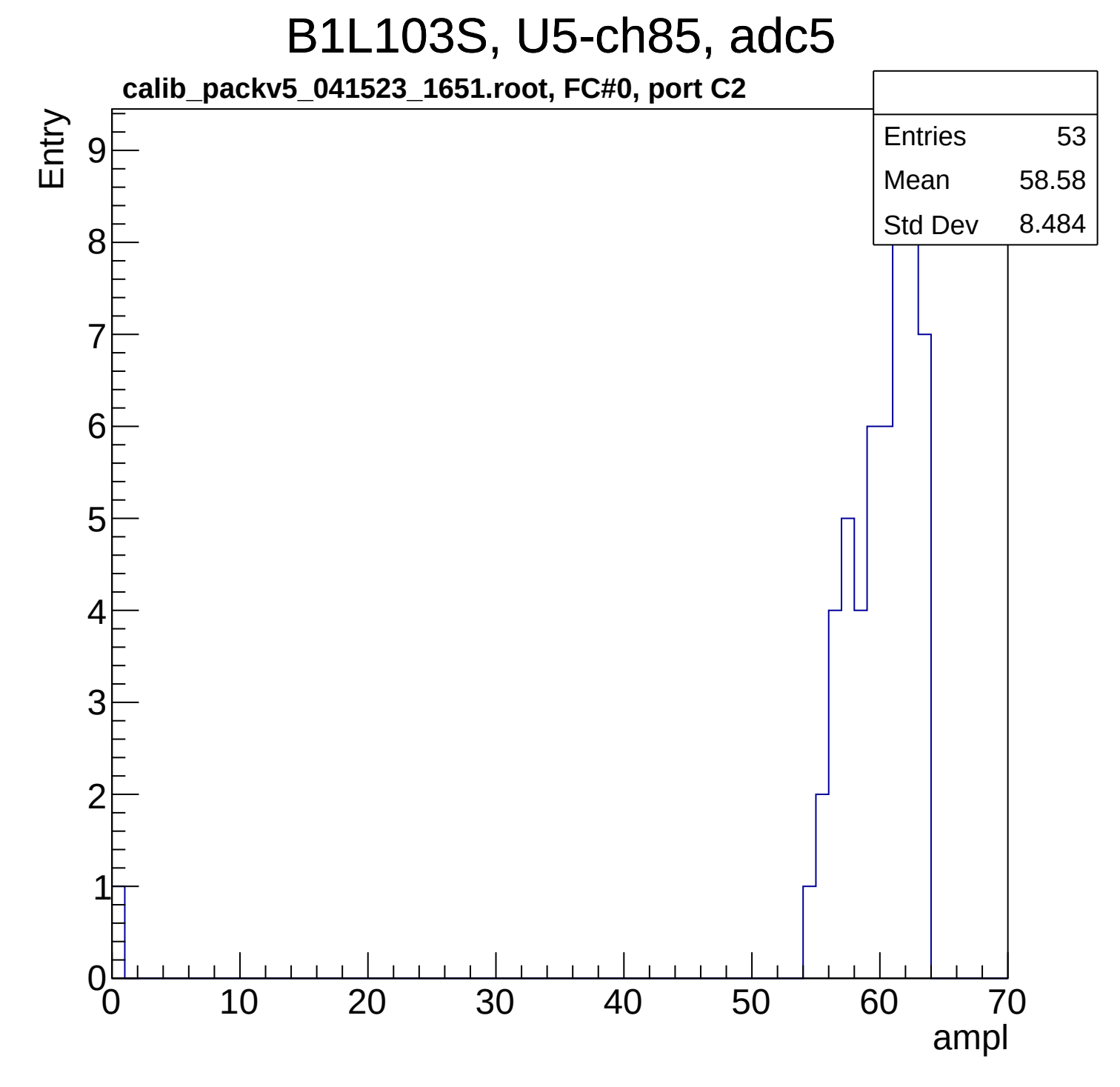
B1L103S, U5-ch85, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.58
Std Dev 8.484
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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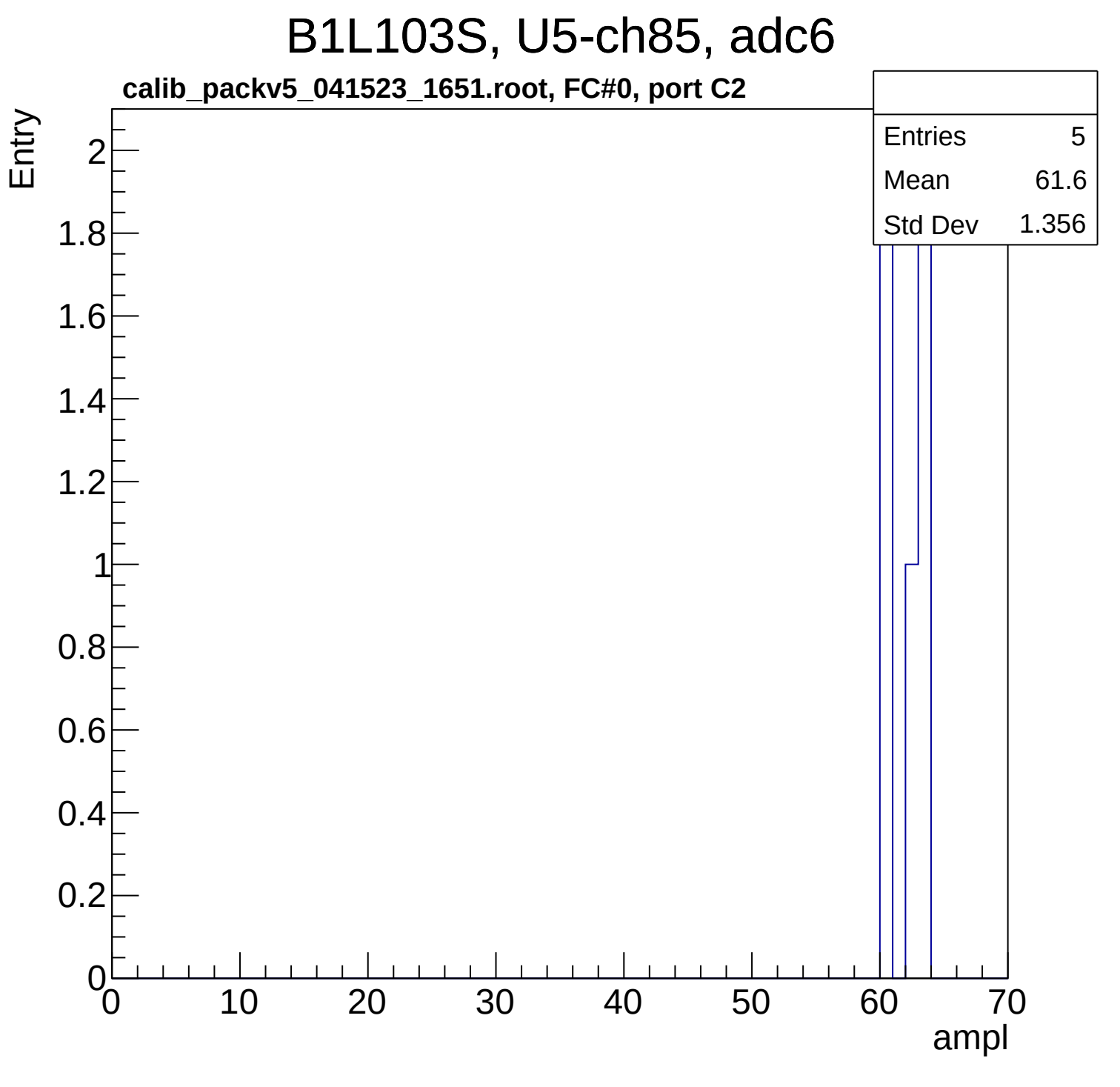
B1L103S, U5-ch85, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.6
Std Dev 1.356
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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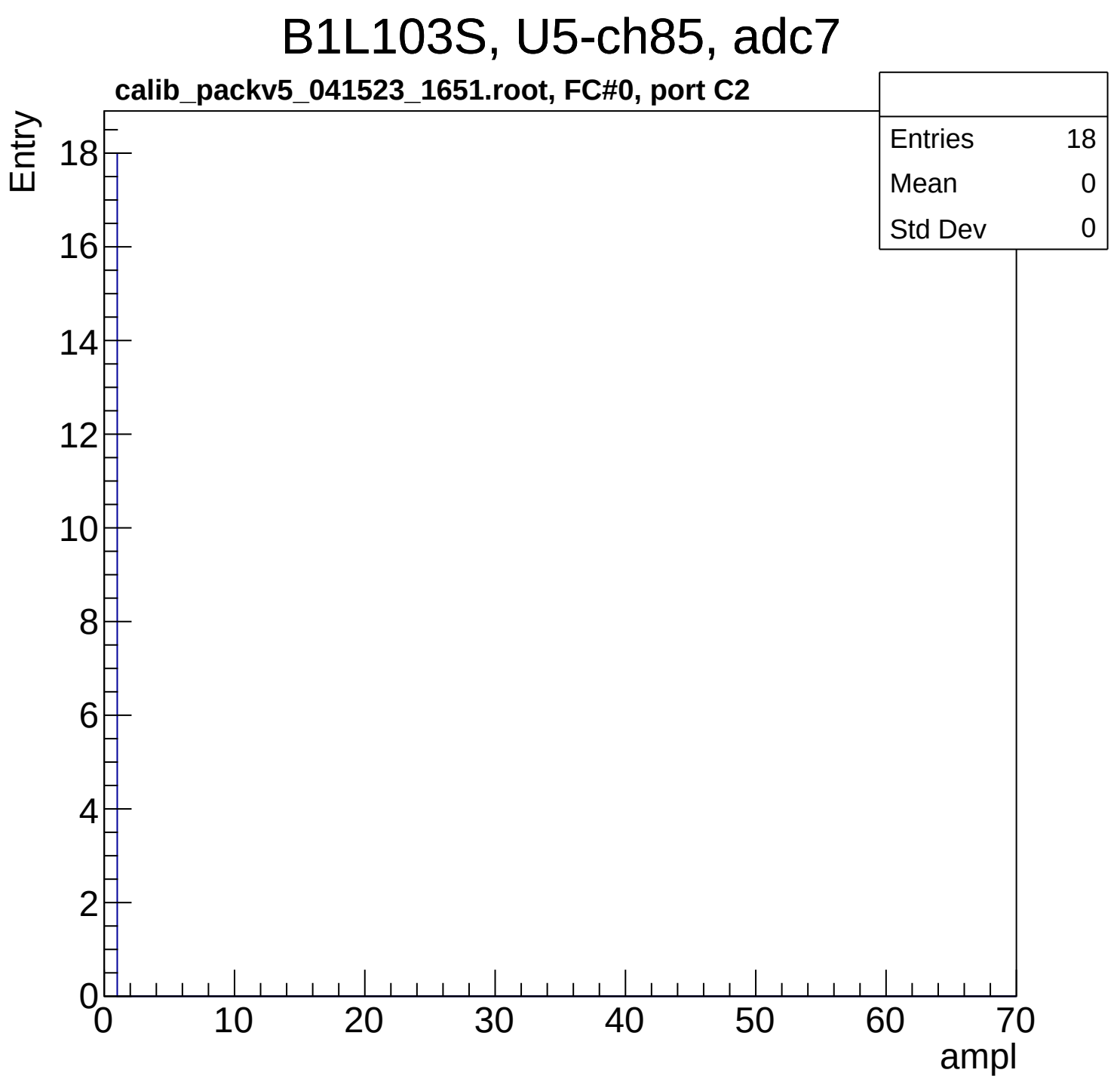
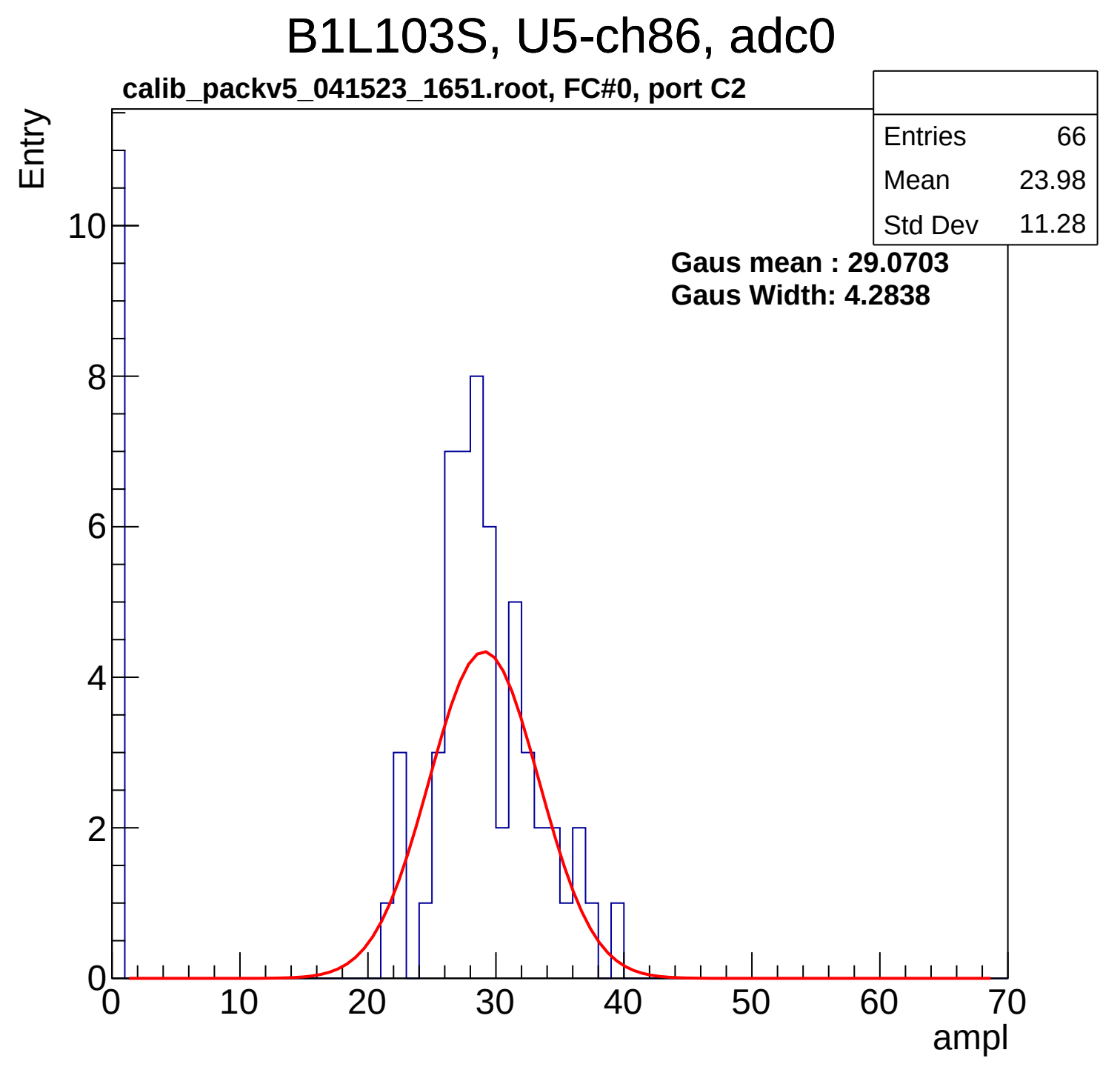
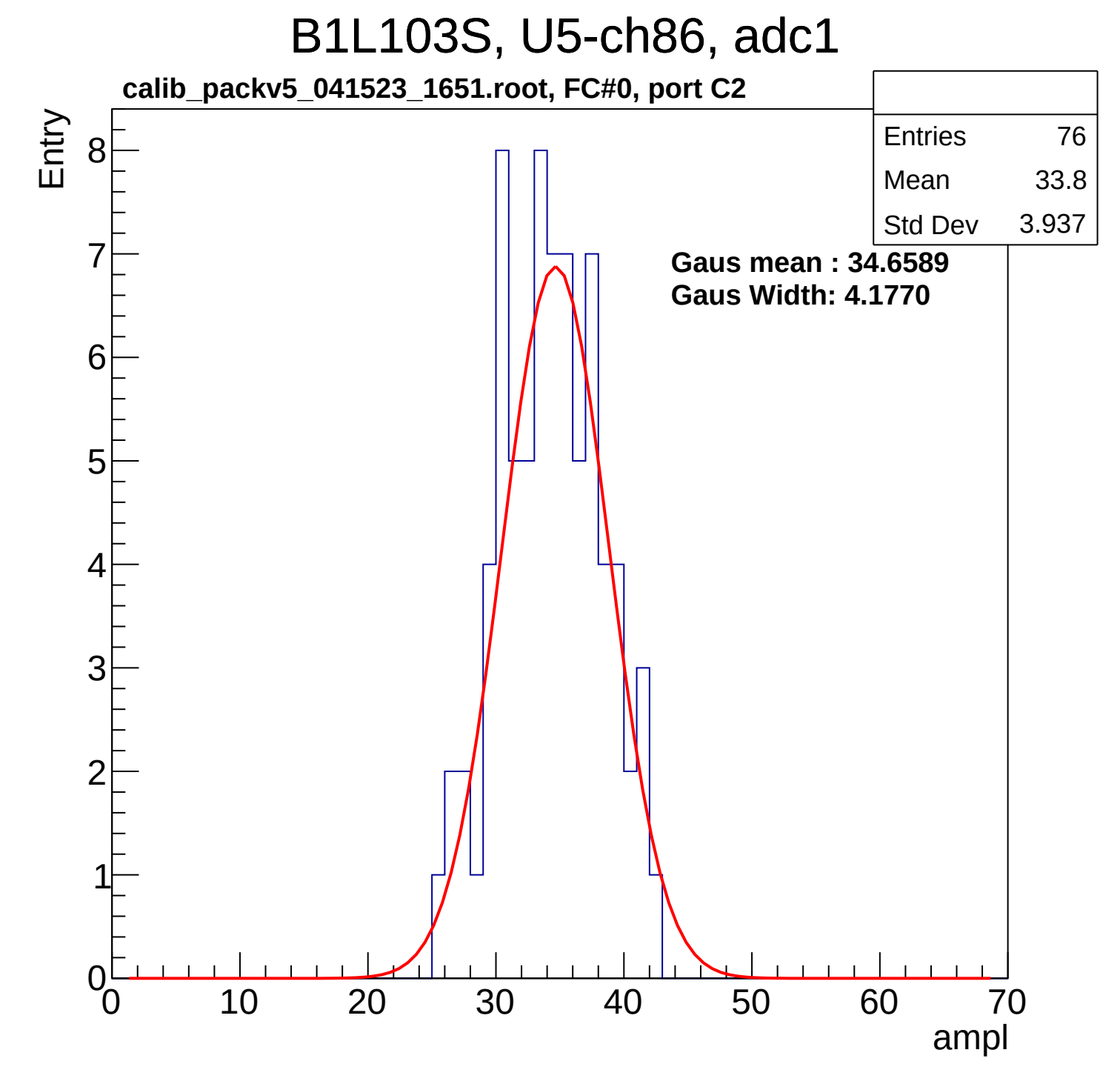

B1L103S, U5-ch85, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch86, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 23.98
Std Dev 11.28
Gaus mean : 29.0703
Gaus Width: 4.2838
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U5-ch86, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 33.8
Std Dev 3.937
Gaus mean : 34.6589
Gaus Width: 4.1770
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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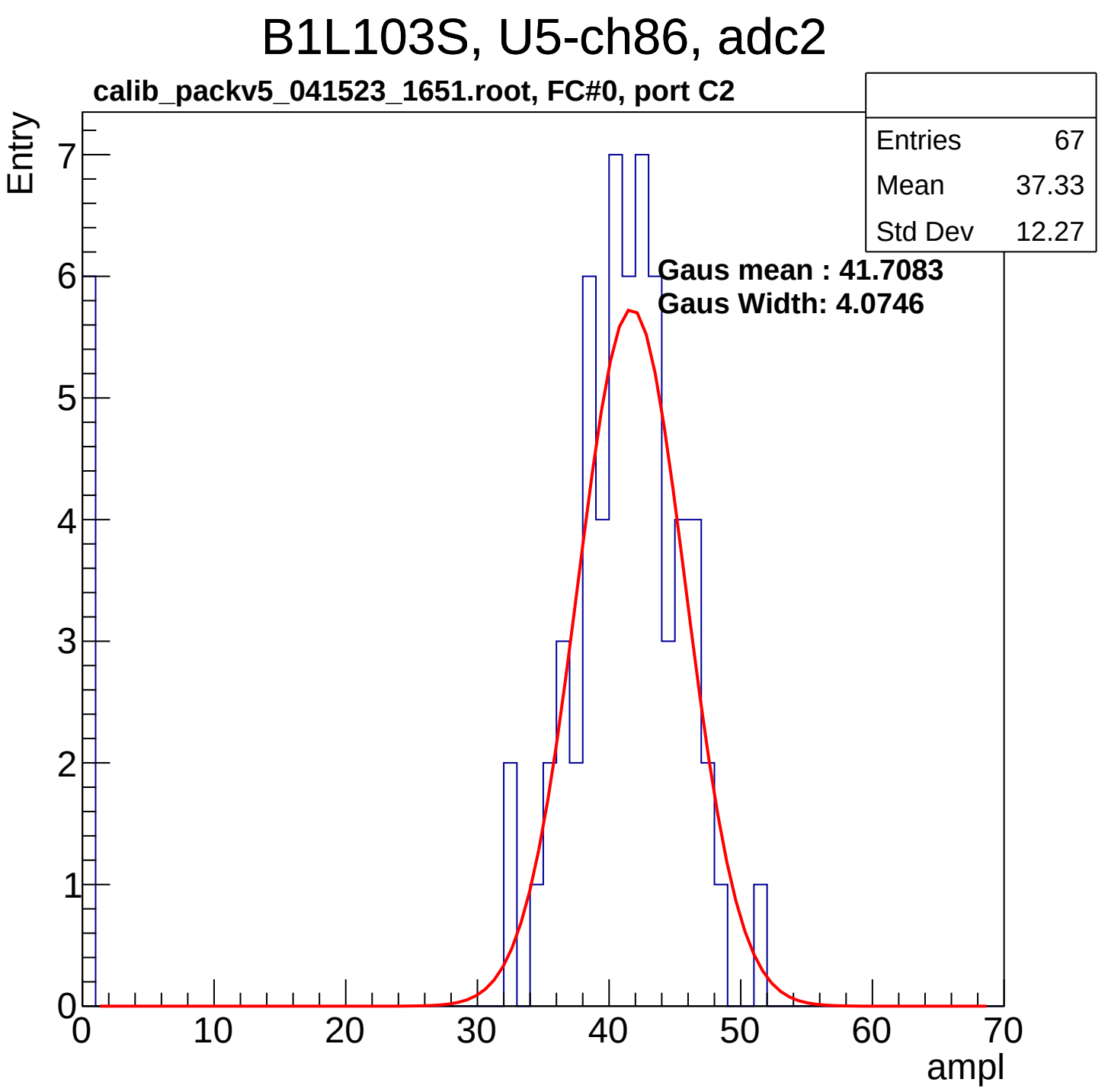
B1L103S, U5-ch86, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 37.33
Std Dev 12.27
Gaus mean : 41.7083
Gaus Width: 4.0746
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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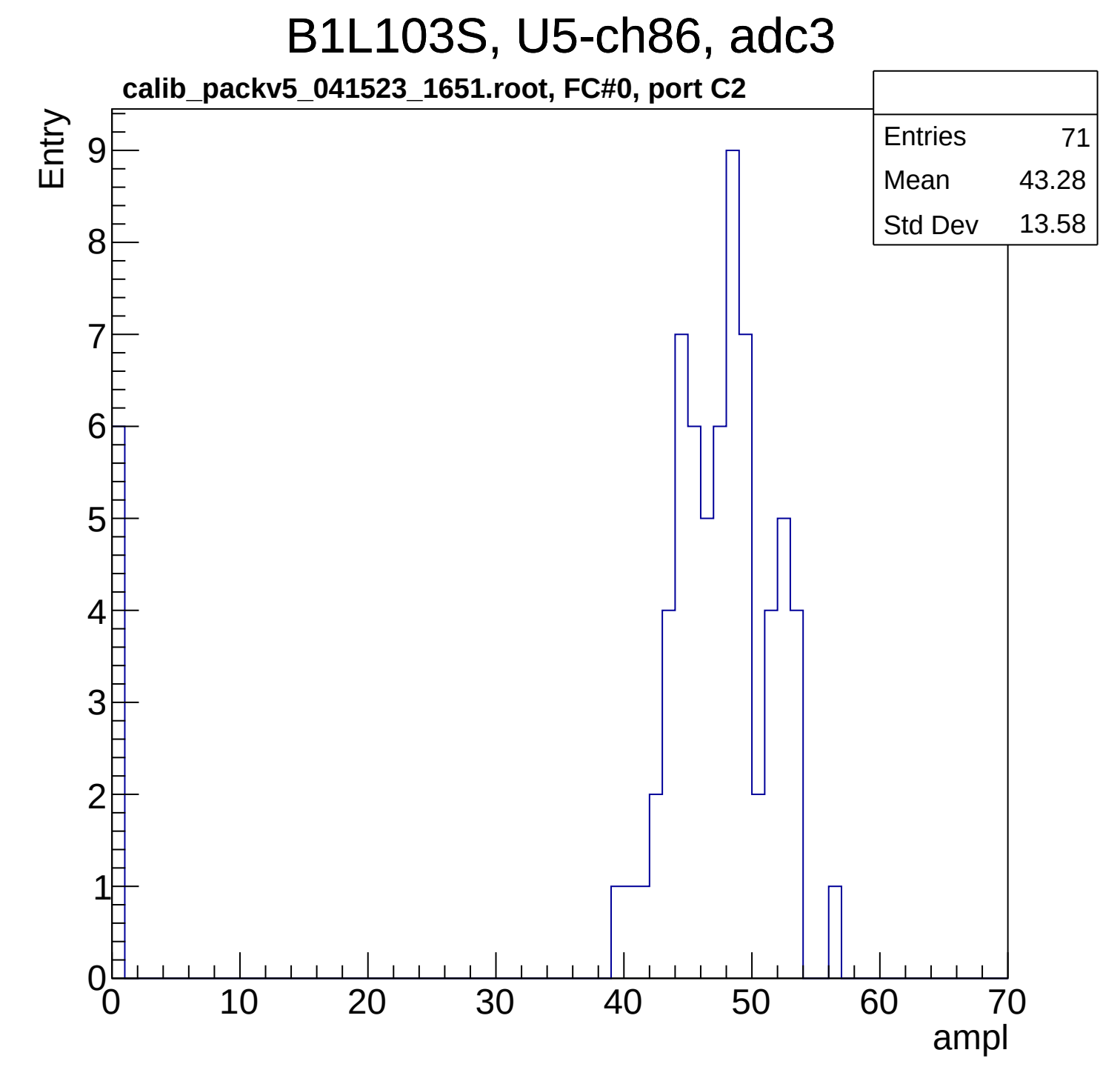
B1L103S, U5-ch86, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 43.28
Std Dev 13.58
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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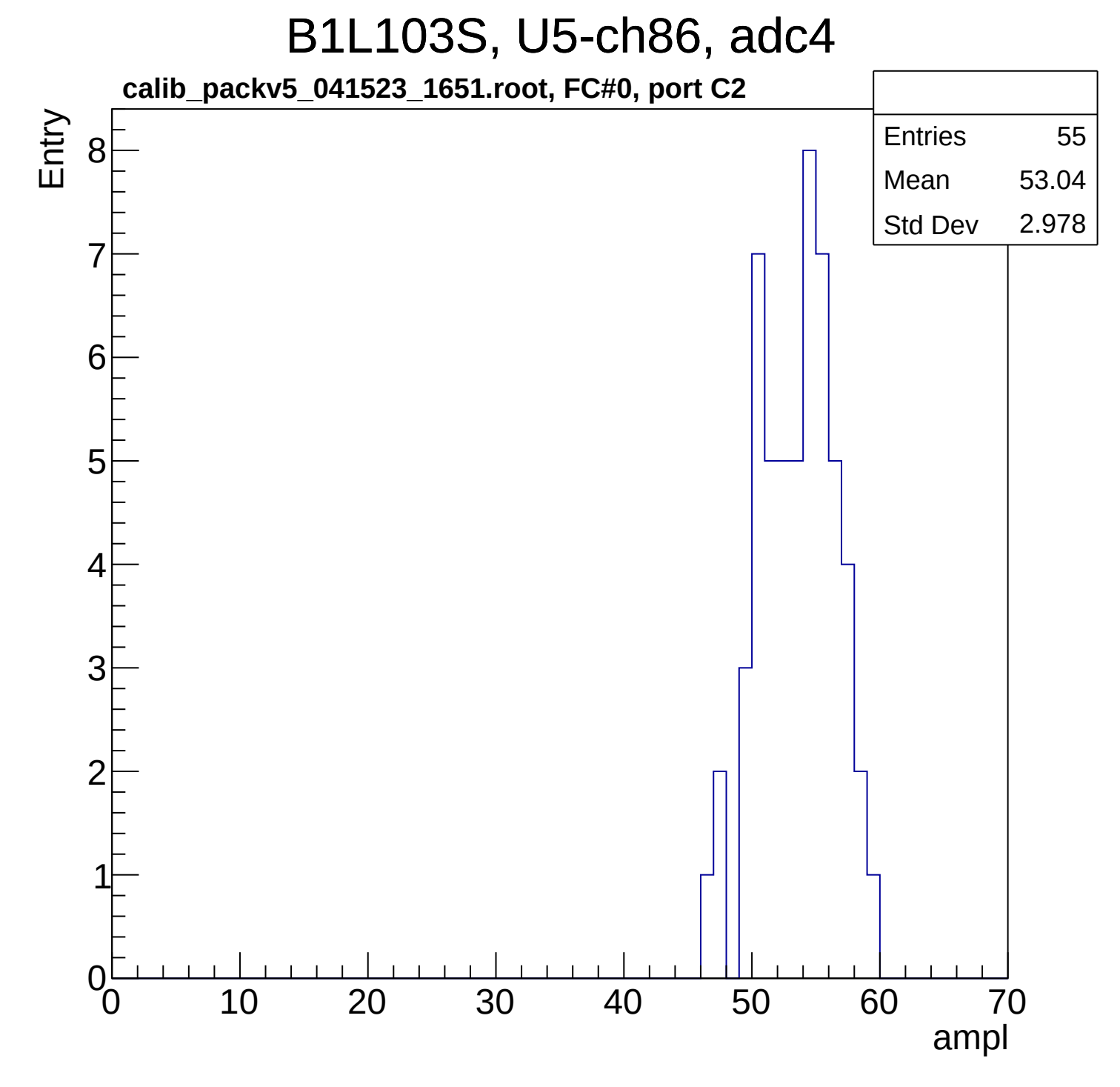
B1L103S, U5-ch86, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 53.04
Std Dev 2.978
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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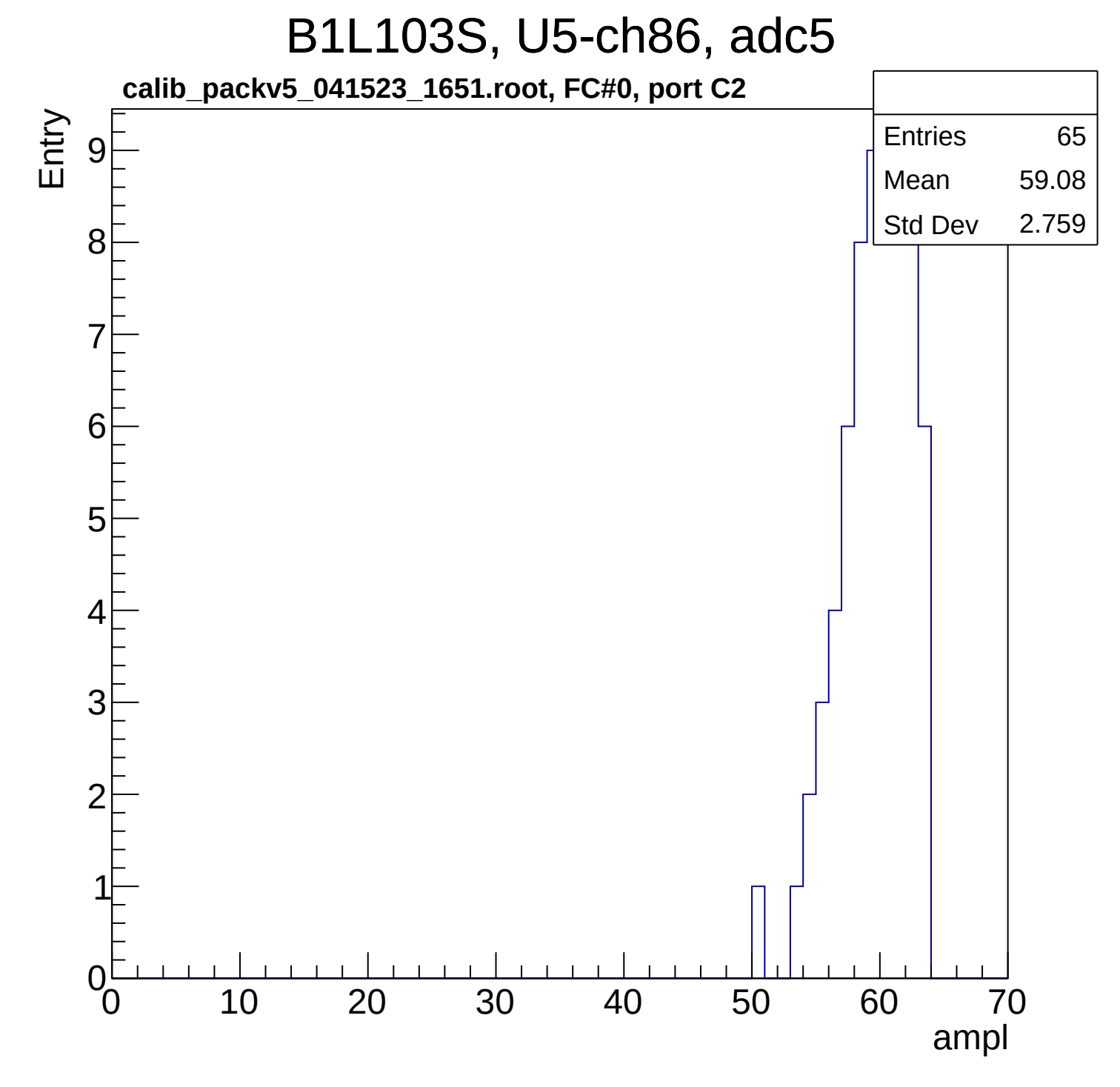
B1L103S, U5-ch86, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 59.08
Std Dev 2.759
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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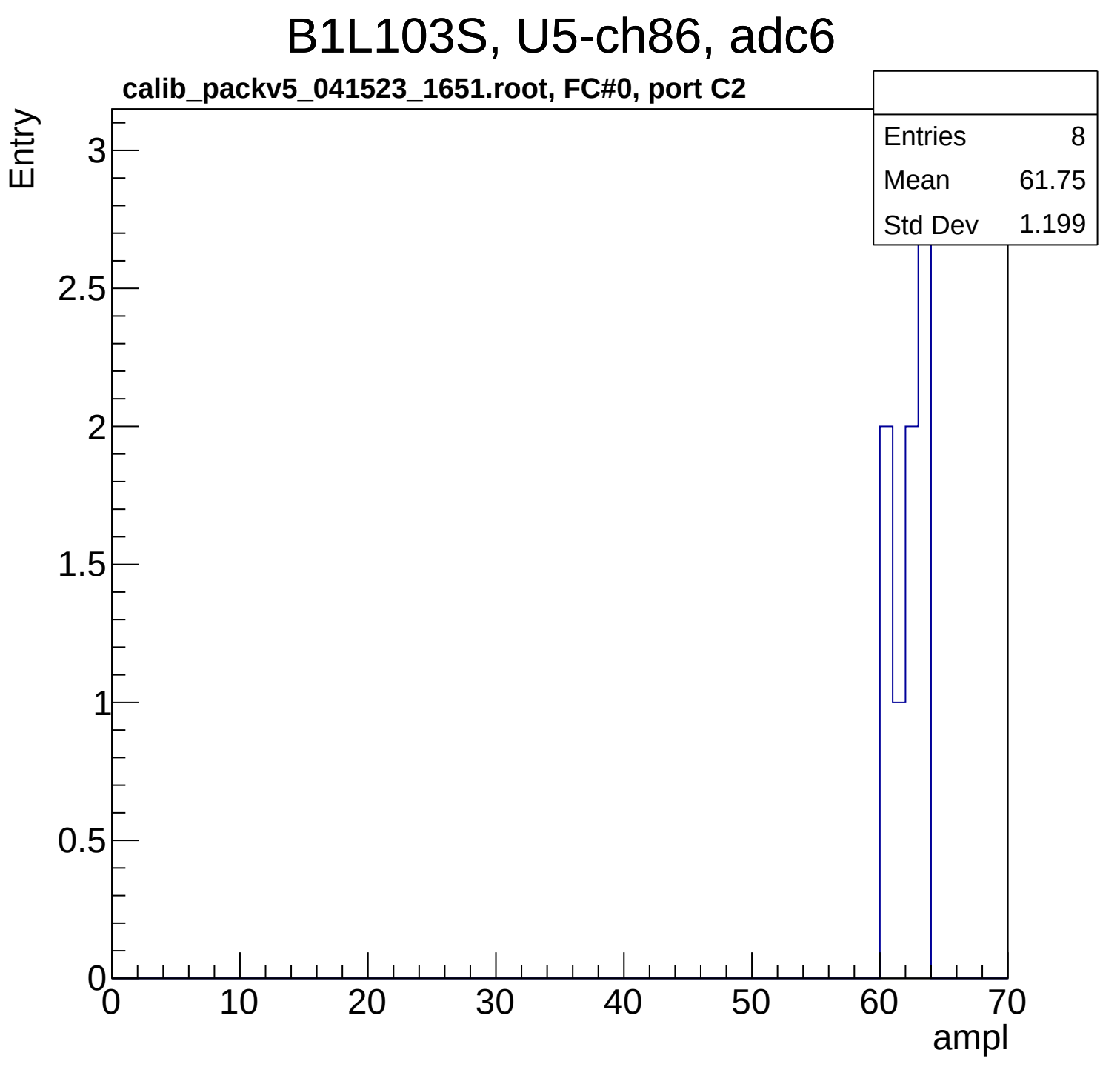
B1L103S, U5-ch86, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.75
Std Dev 1.199
Entry
ampl
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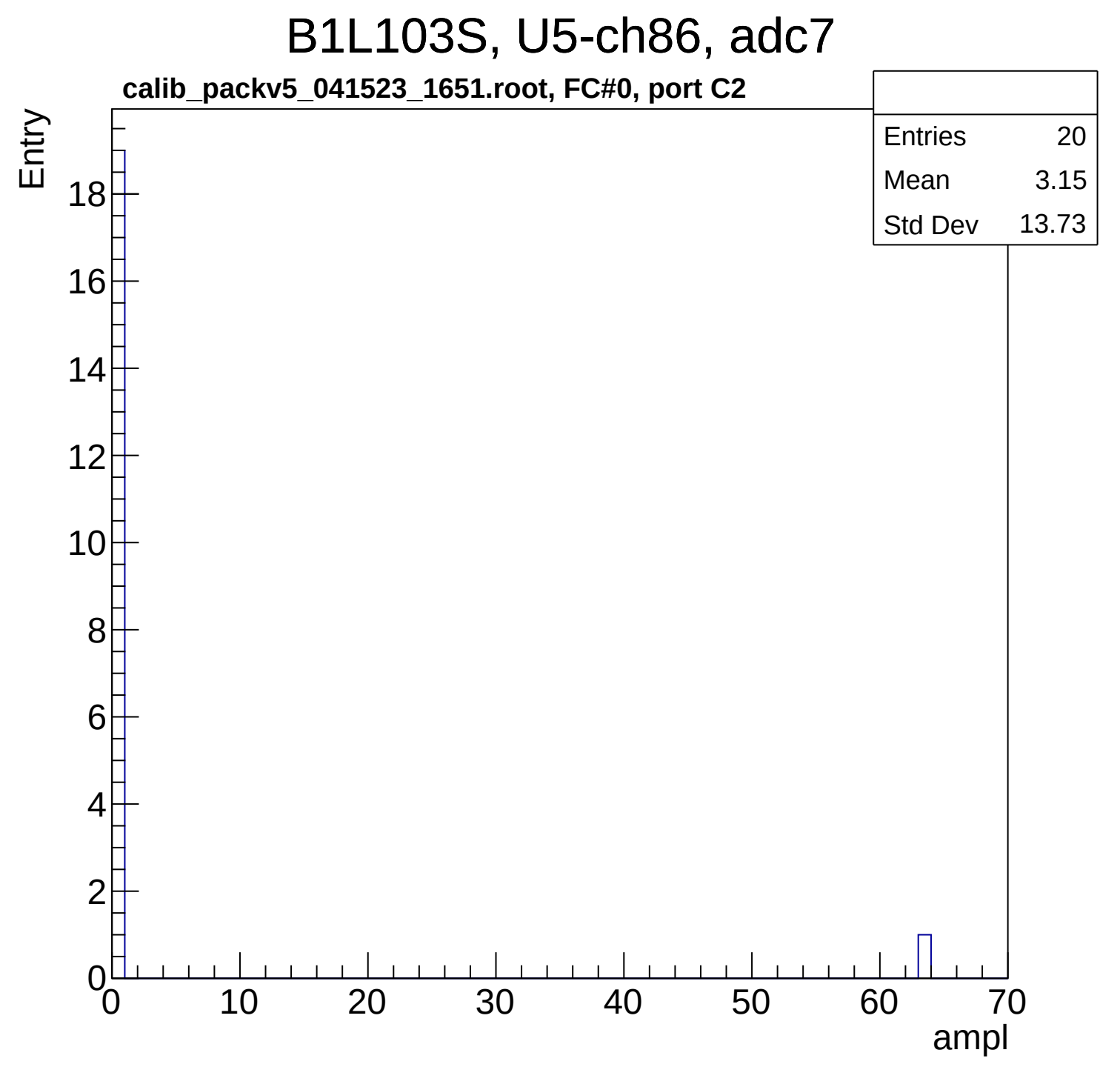
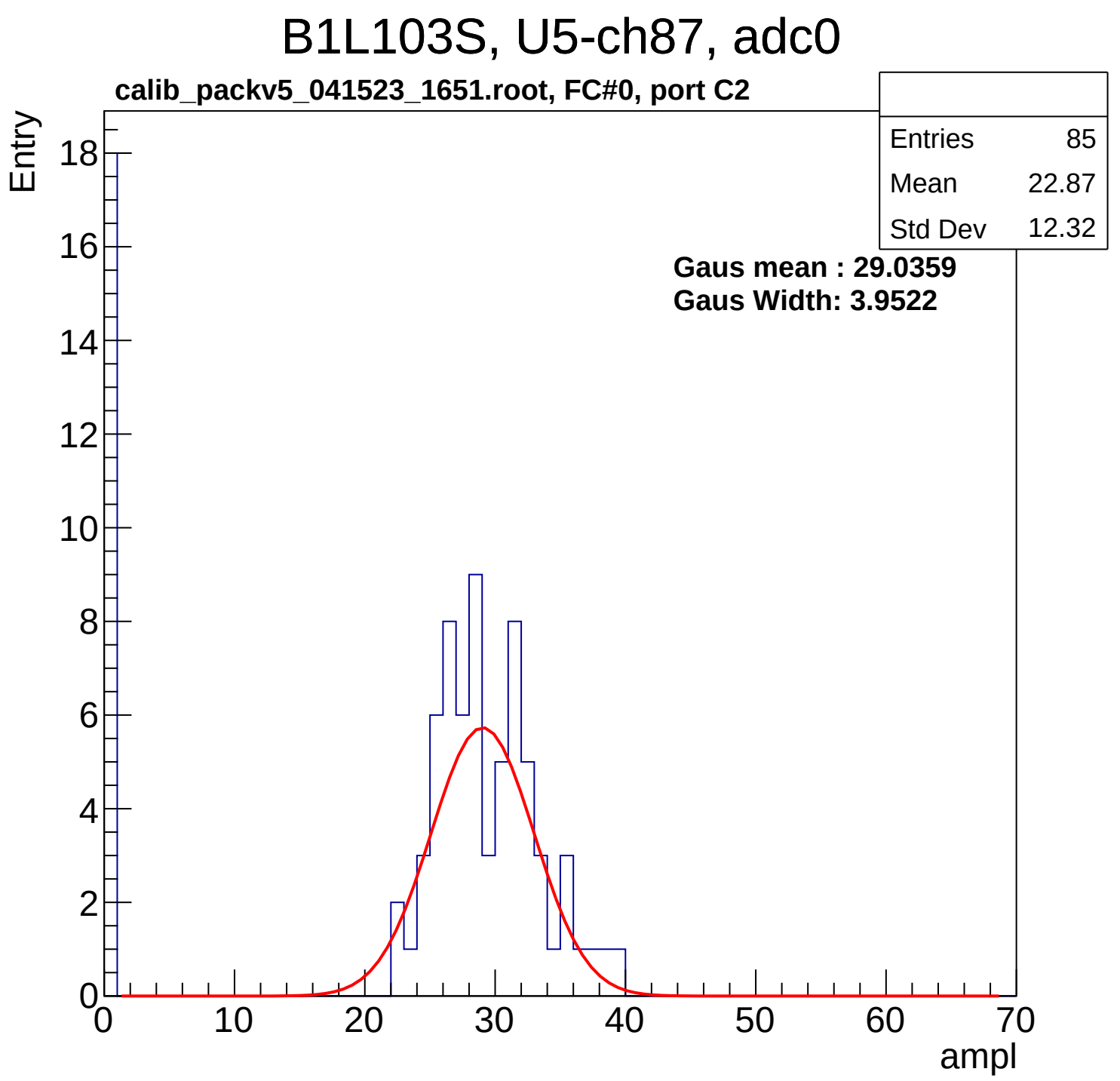
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U5-ch86, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch87, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 22.87
Std Dev 12.32
Gaus mean : 29.0359
Gaus Width: 3.9522
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
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60
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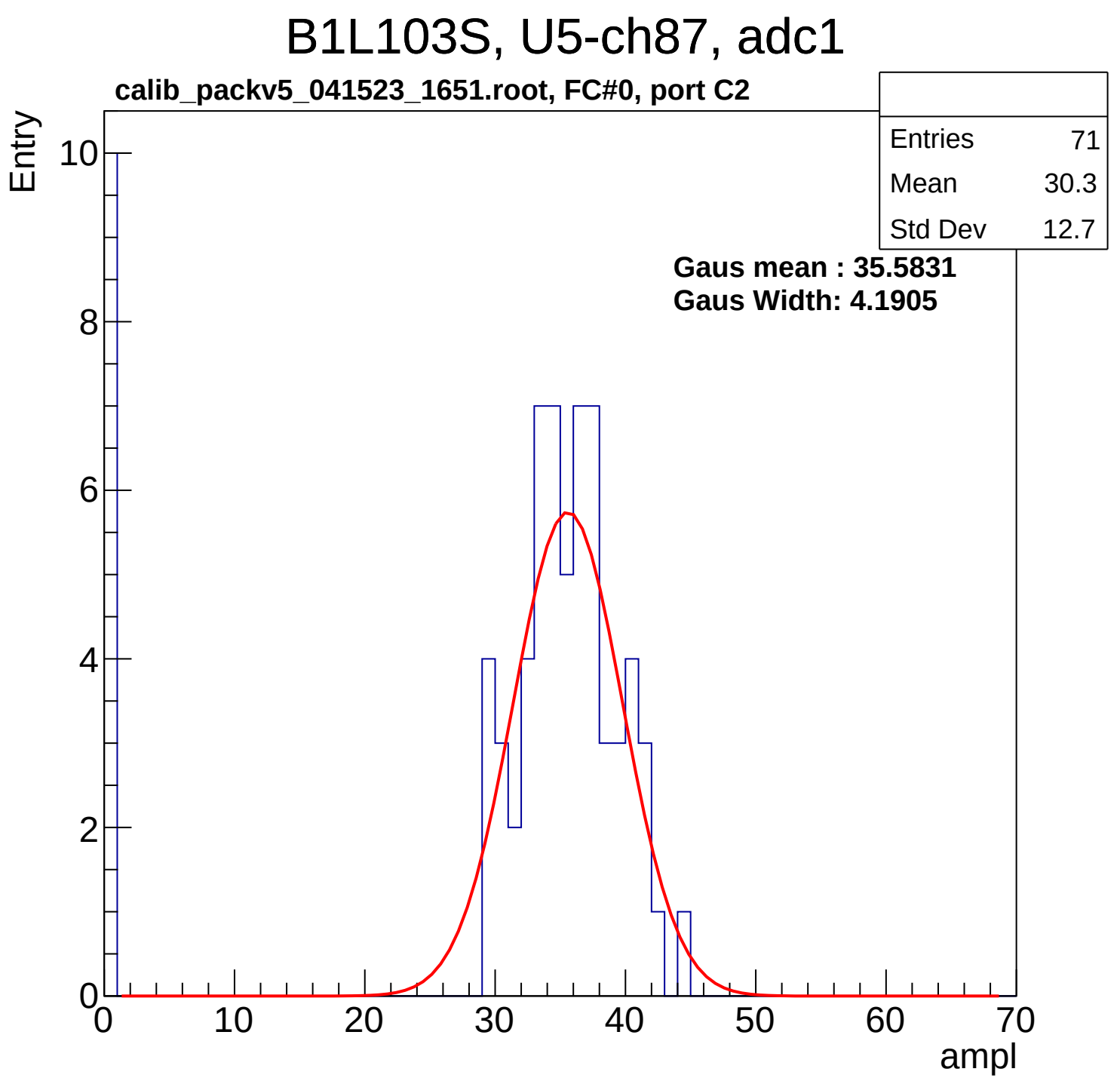
B1L103S, U5-ch87, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 30.3
Std Dev 12.7
Gaus mean : 35.5831
Gaus Width: 4.1905
Entry
ampl
0
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4
6
8
10
0
10
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40
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60
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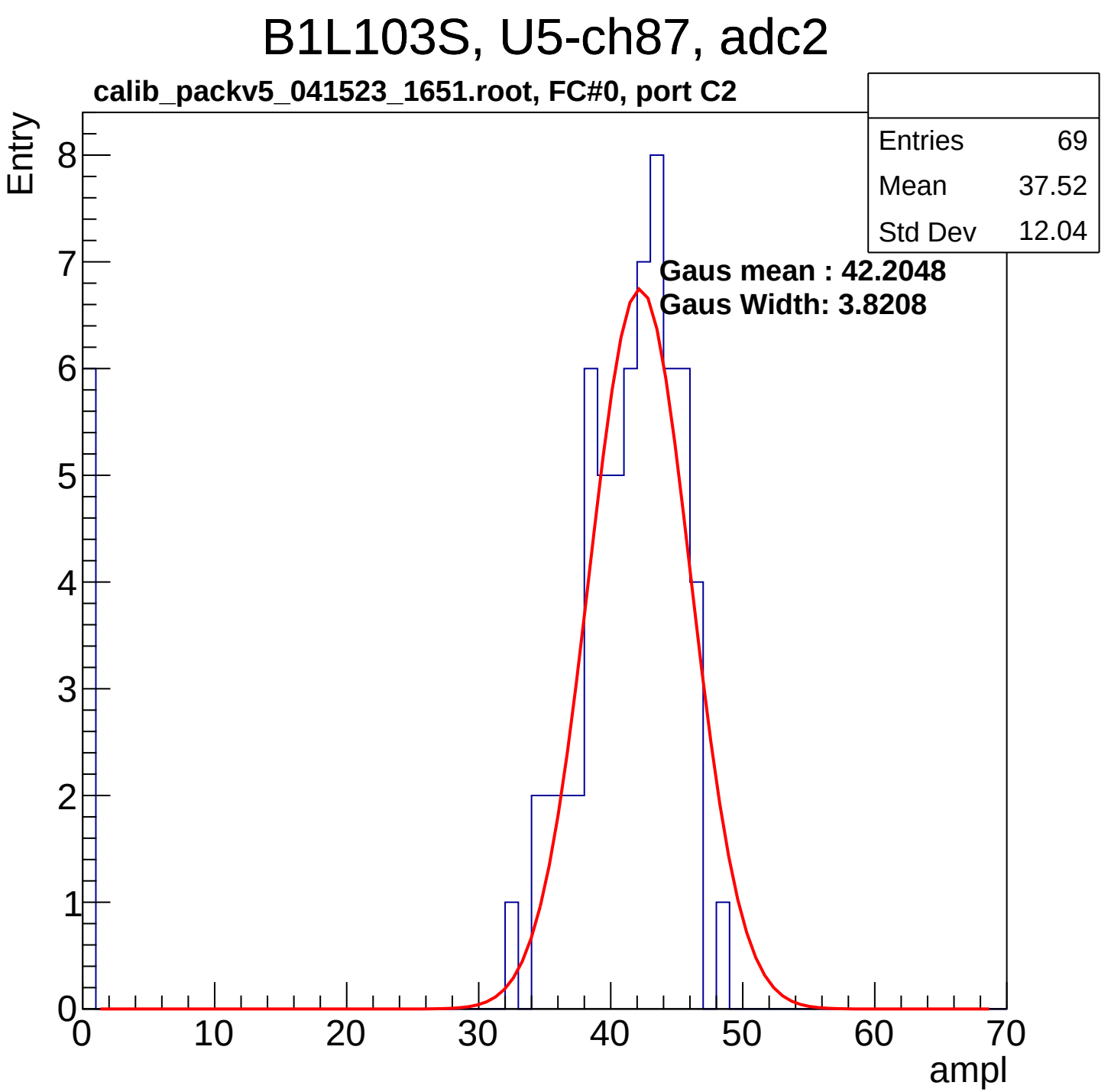
B1L103S, U5-ch87, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 37.52
Std Dev 12.04
Gaus mean : 42.2048
Gaus Width: 3.8208
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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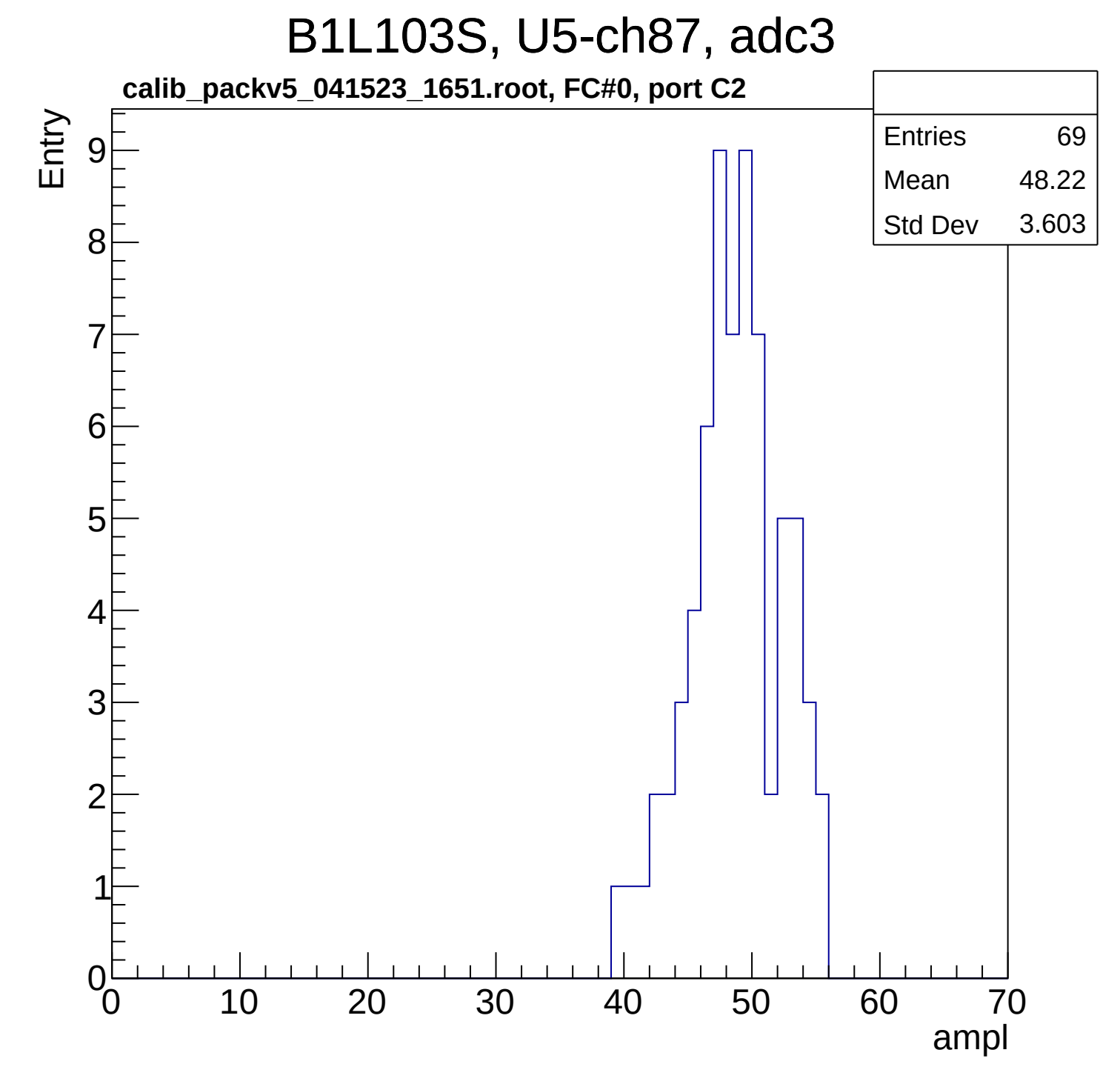
40
50
60
70


B1L103S, U5-ch87, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 48.22
Std Dev 3.603
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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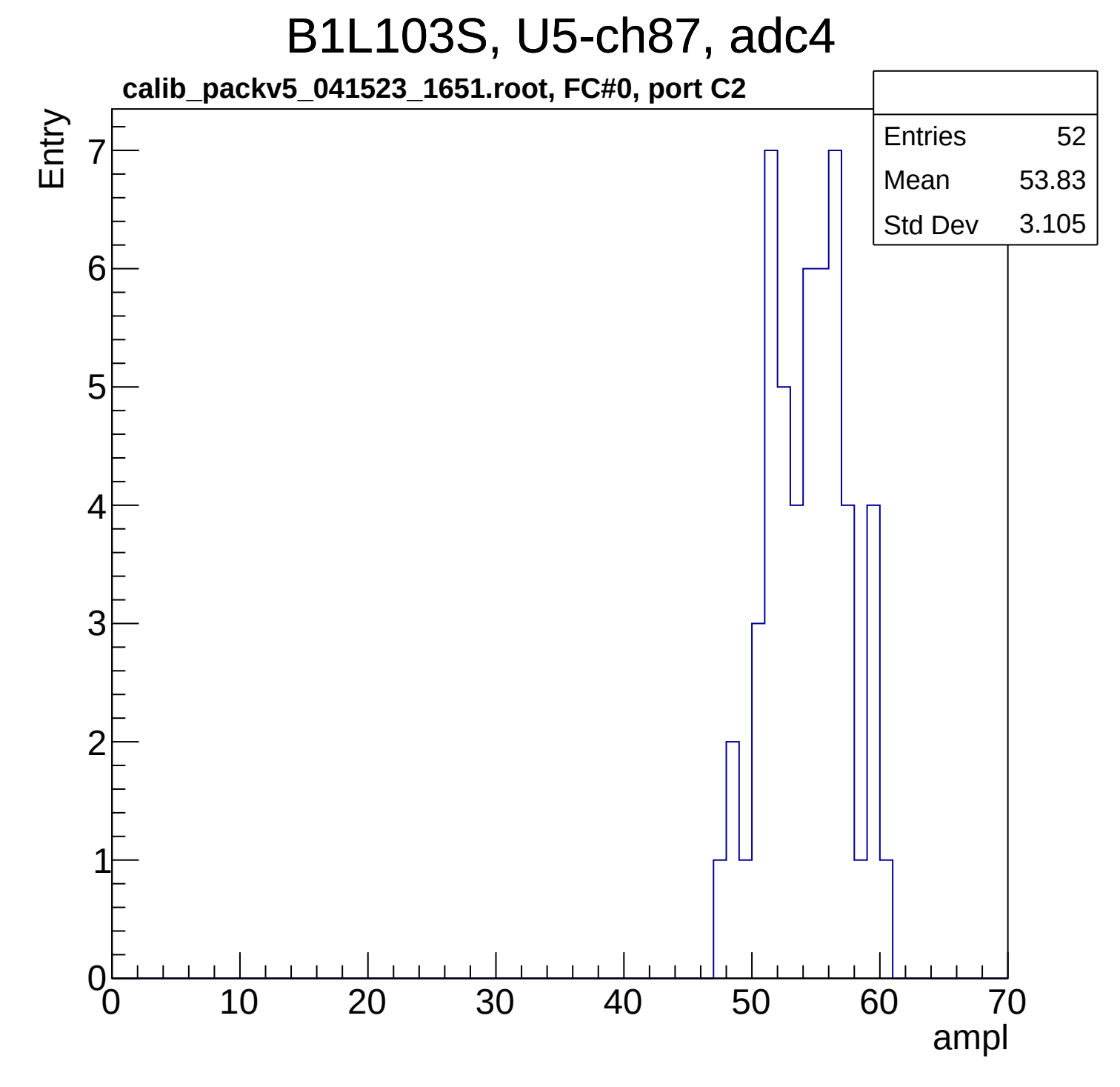
B1L103S, U5-ch87, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 53.83
Std Dev 3.105
Entry
ampl
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1
2
3
4
5
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0
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20
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60
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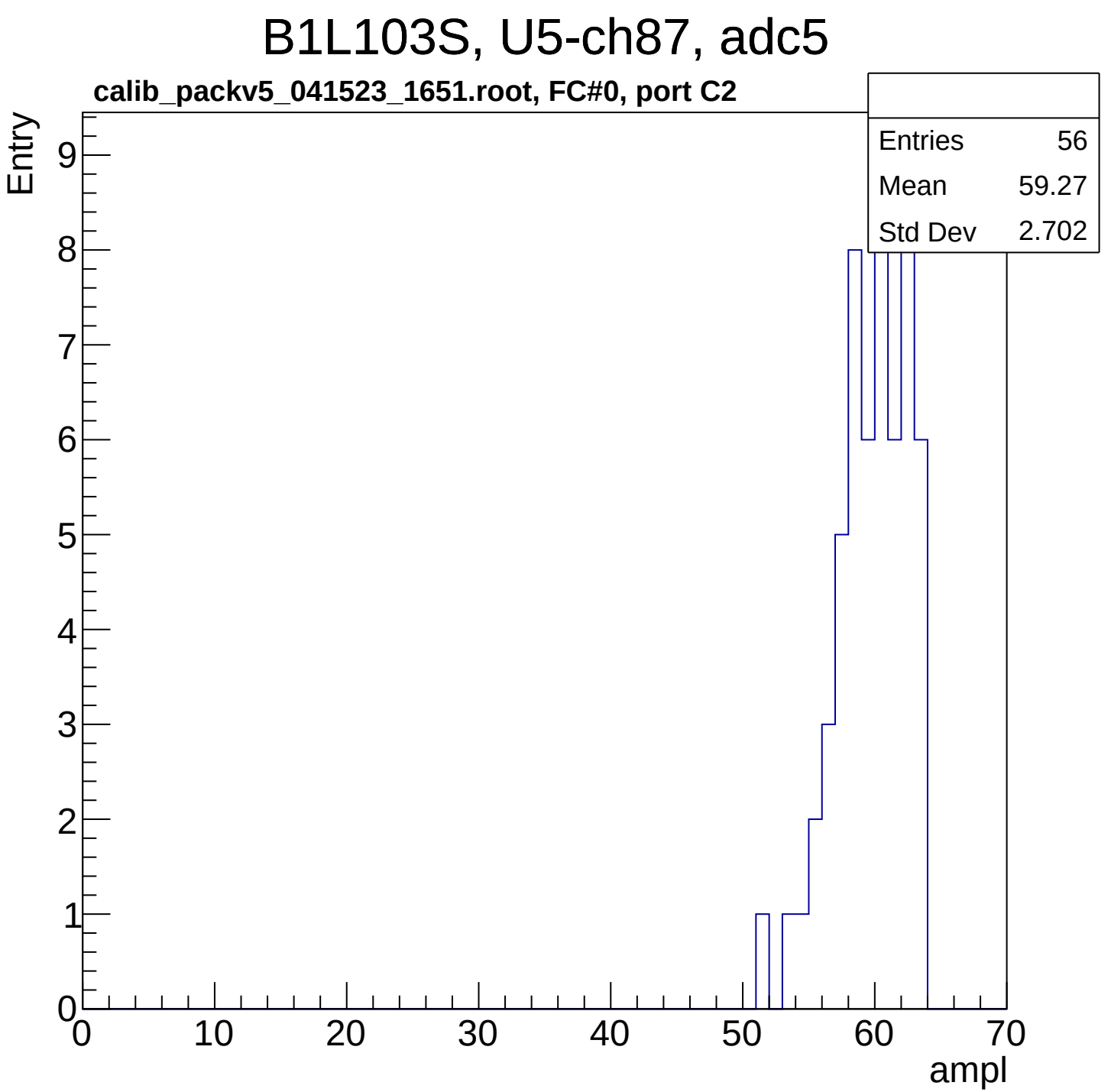
B1L103S, U5-ch87, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 59.27
Std Dev 2.702
Entry
ampl
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0
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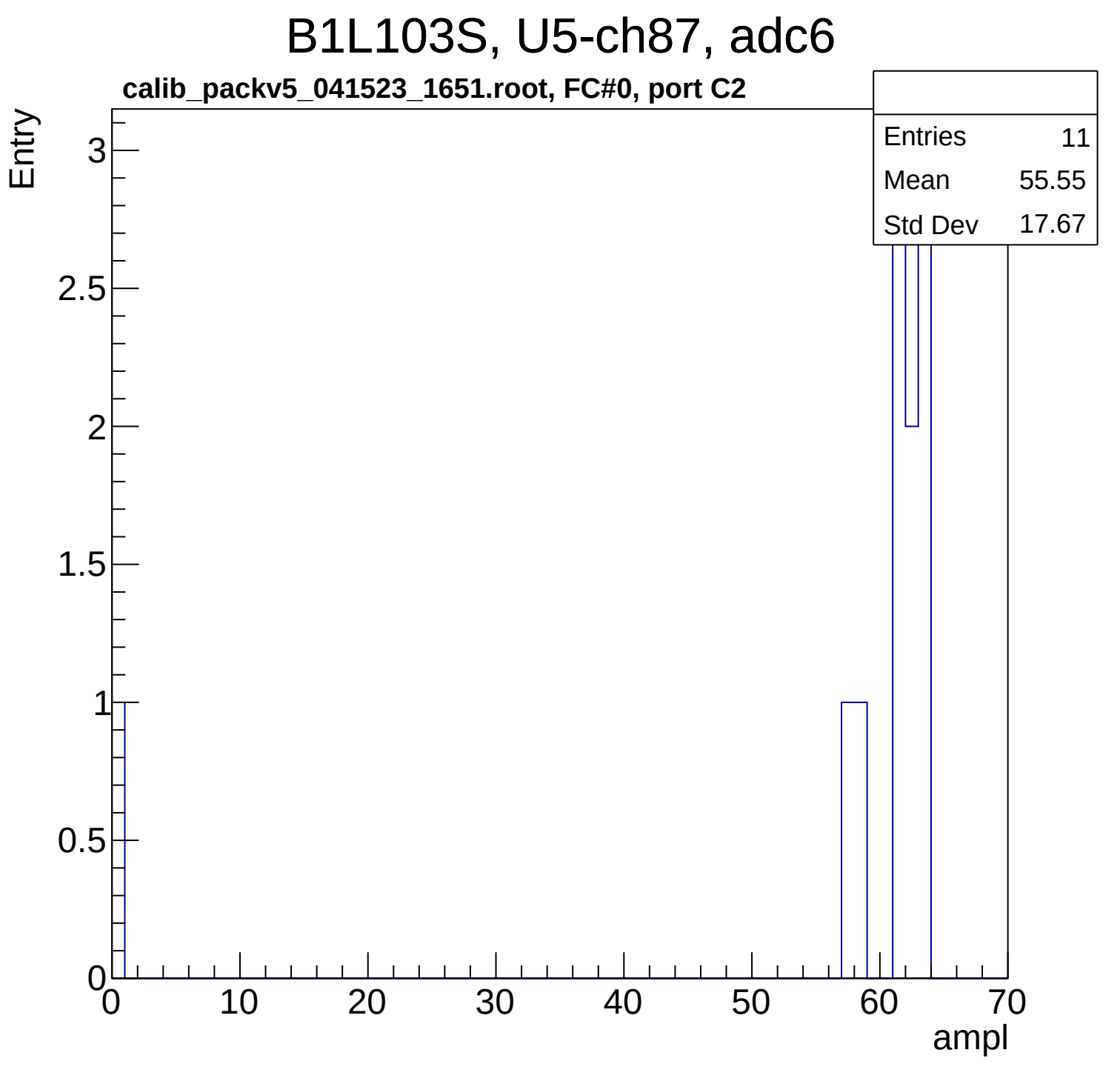
B1L103S, U5-ch87, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 55.55
Std Dev 17.67
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
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60
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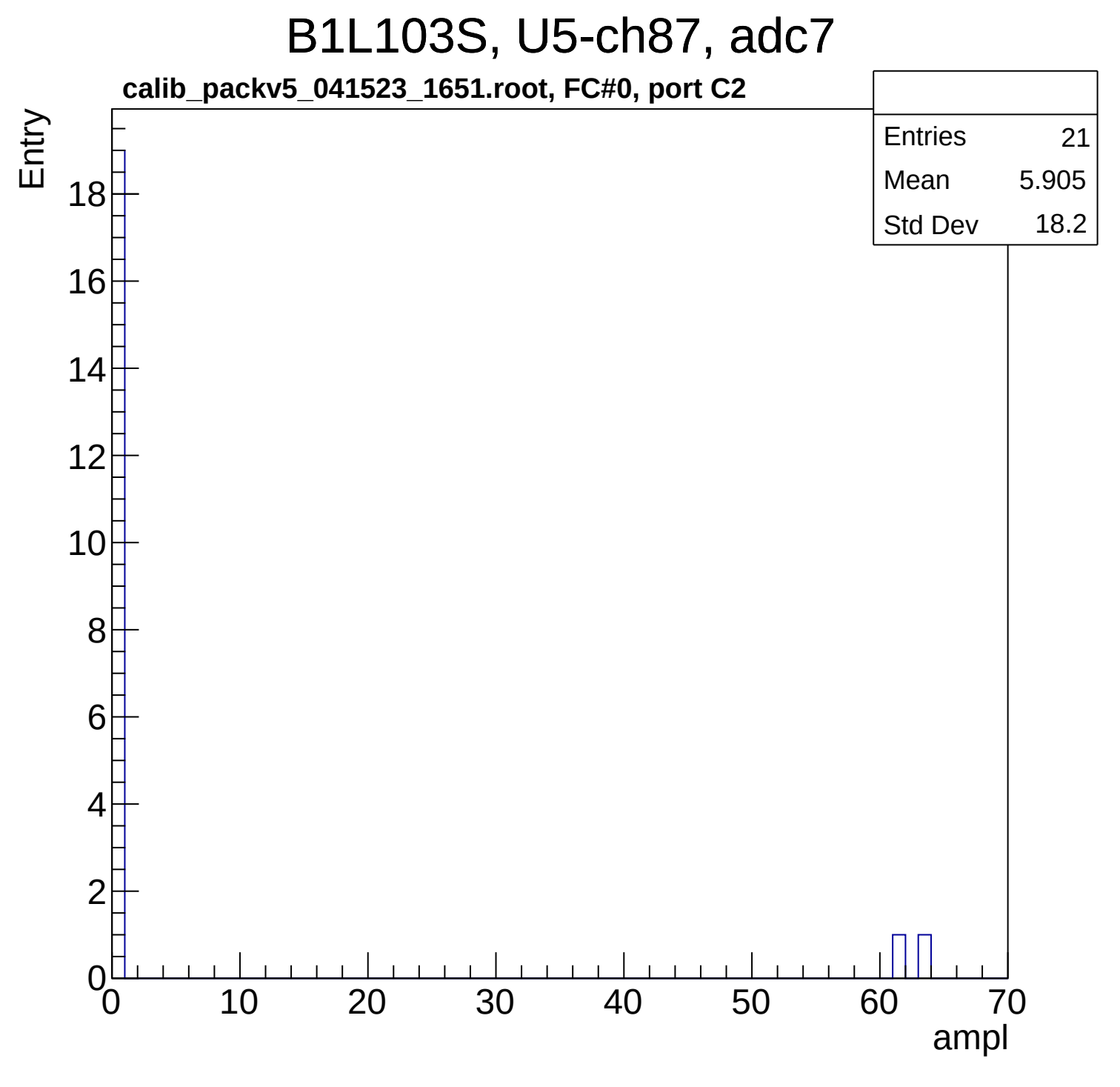
B1L103S, U5-ch87, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
0
2
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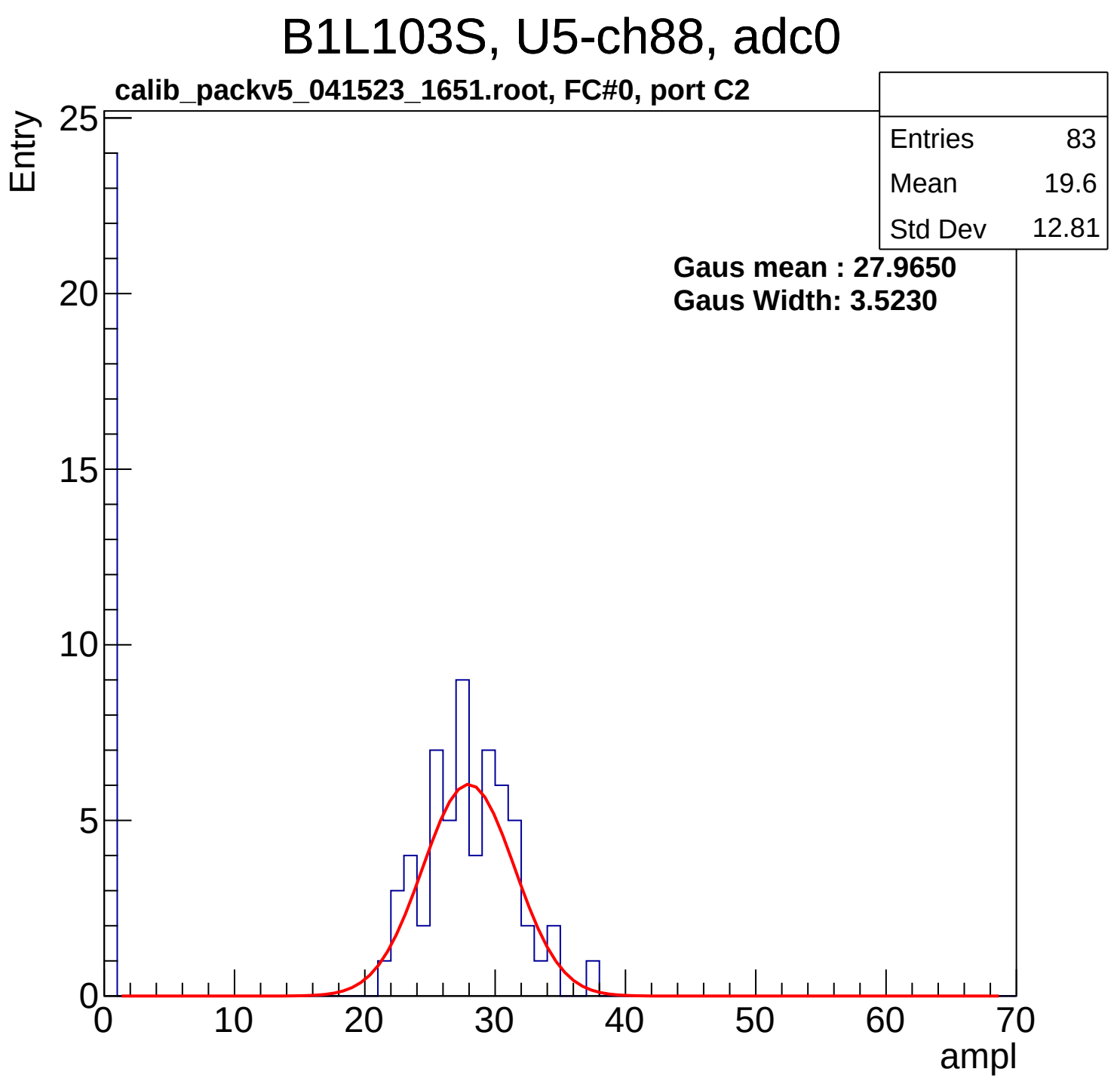
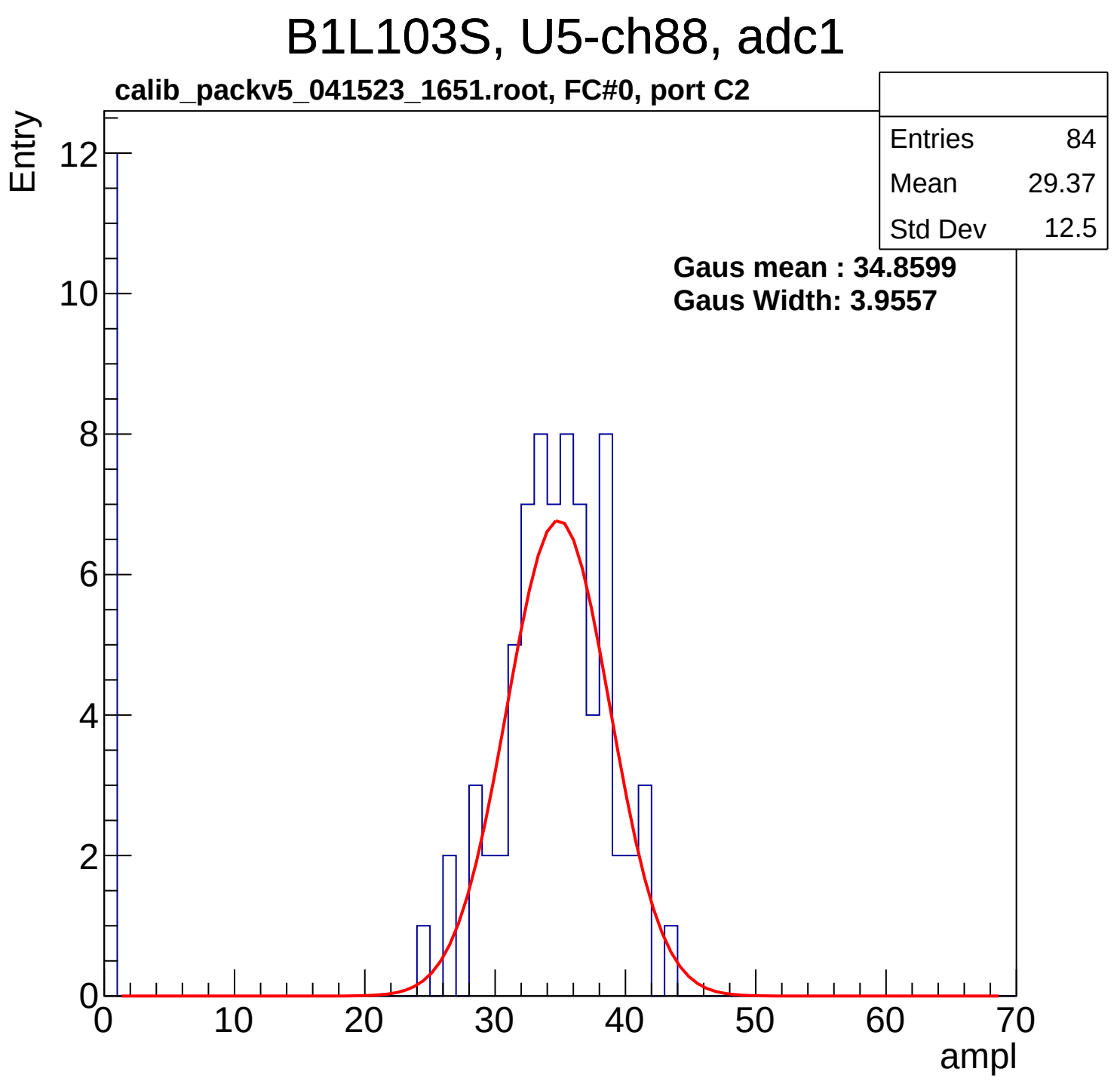
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch88, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 19.6
Std Dev 12.81
Gaus mean : 27.9650
Gaus Width: 3.5230
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U5-ch88, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 29.37
Std Dev 12.5
Gaus mean : 34.8599
Gaus Width: 3.9557
Entry
ampl
0
2
4
6
8
10
12
0
10
20
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40
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60
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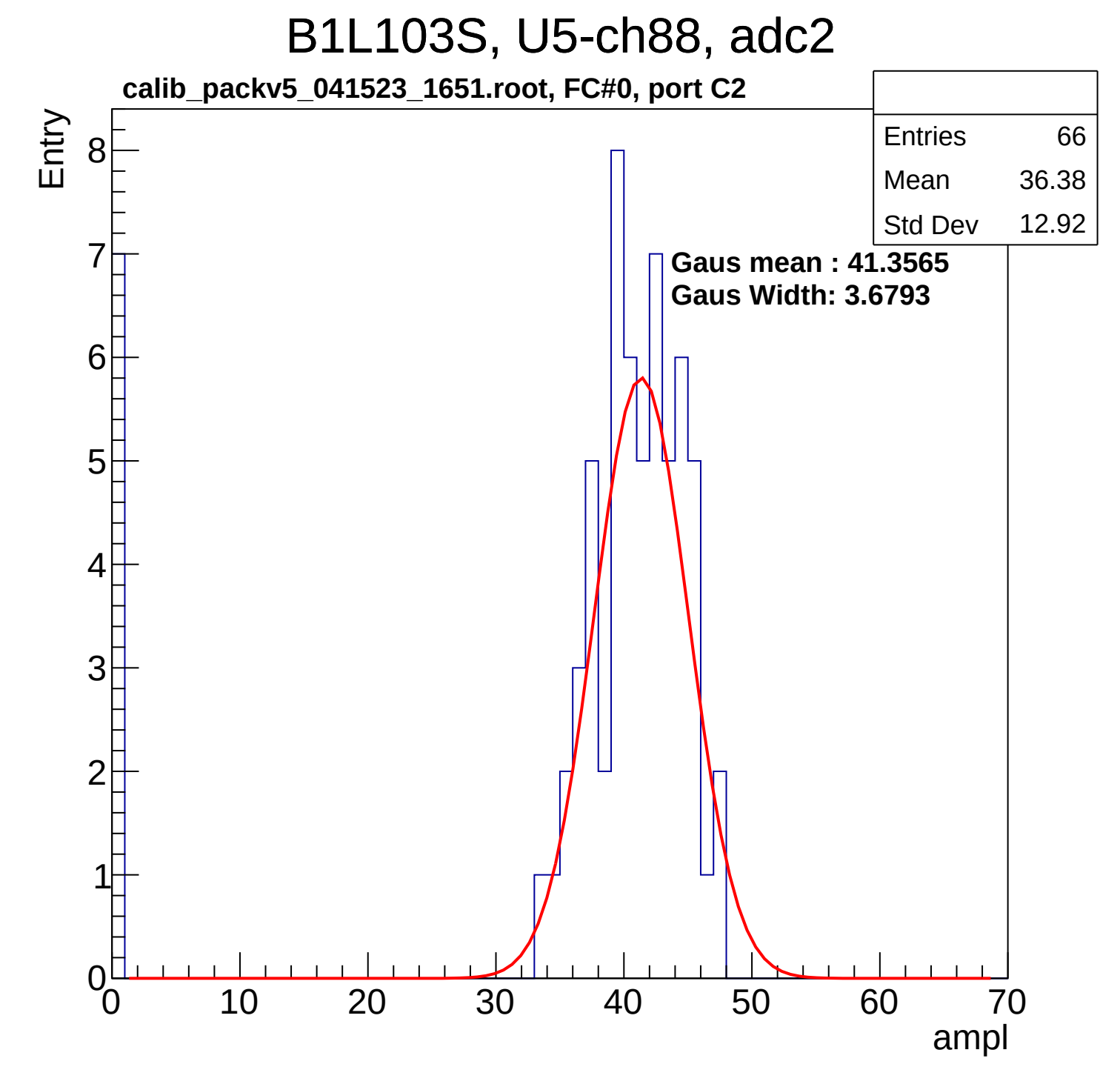
B1L103S, U5-ch88, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 36.38
Std Dev 12.92
Gaus mean : 41.3565
Gaus Width: 3.6793
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
50
60
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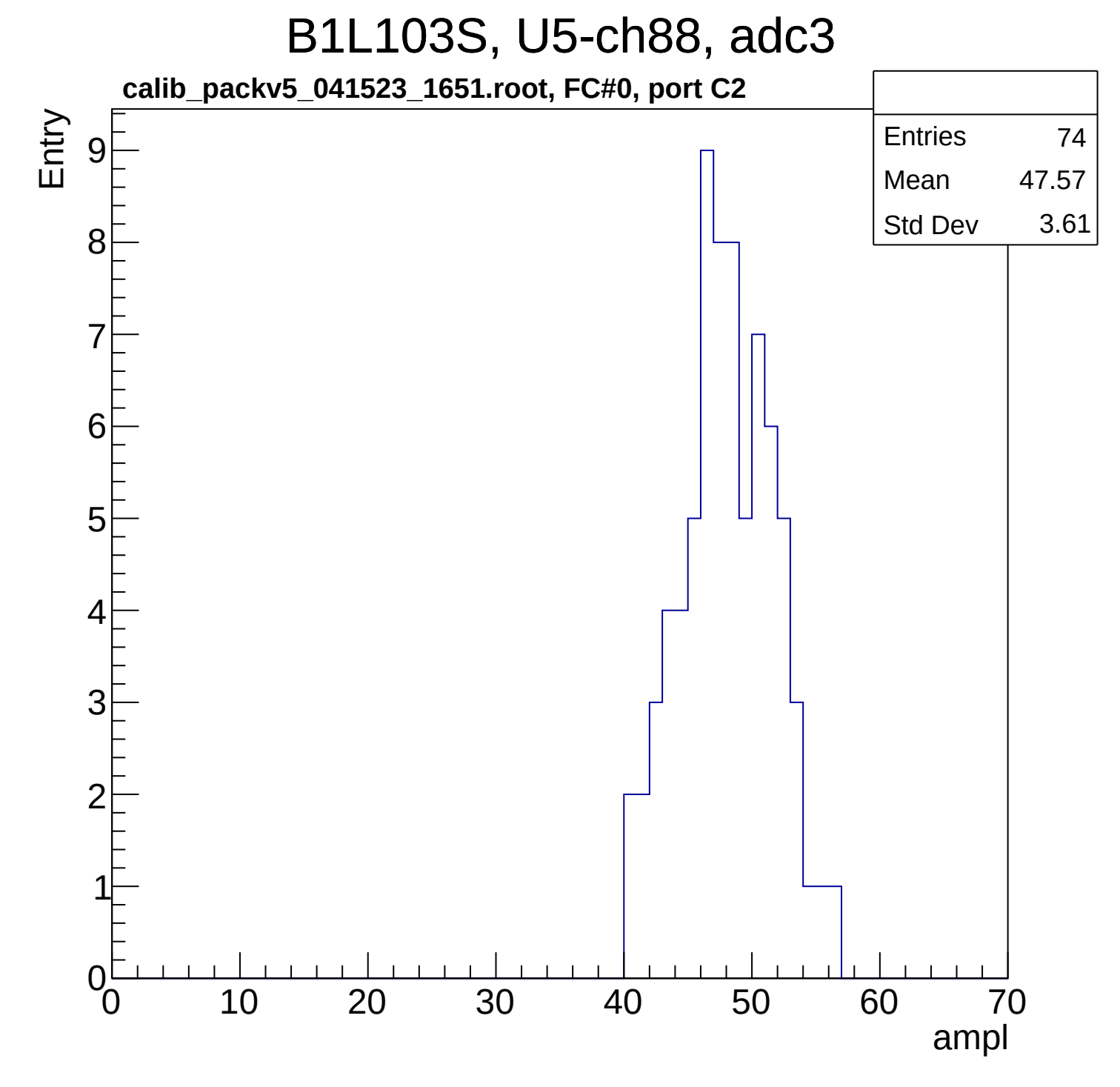
B1L103S, U5-ch88, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 47.57
Std Dev 3.61
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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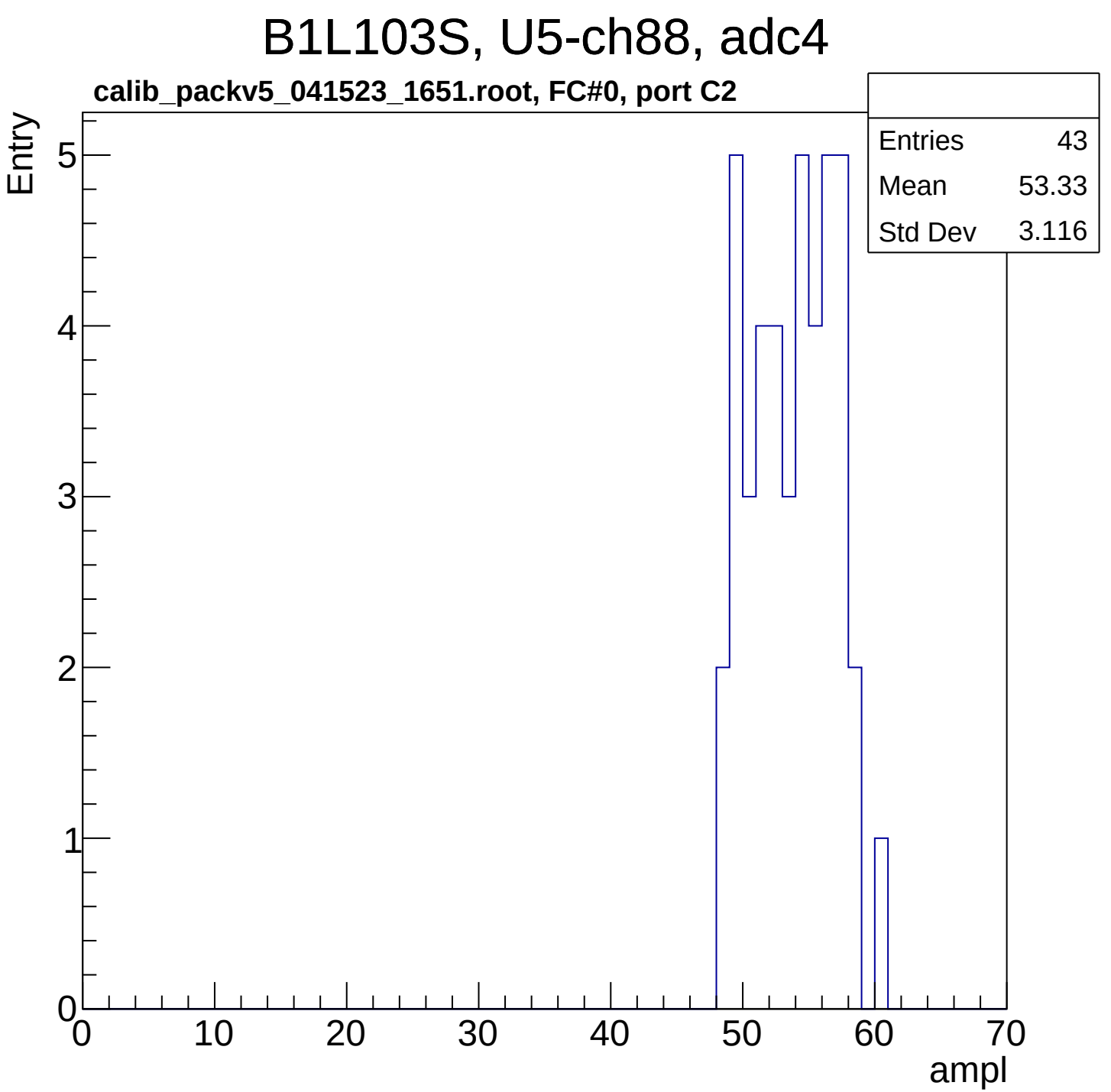
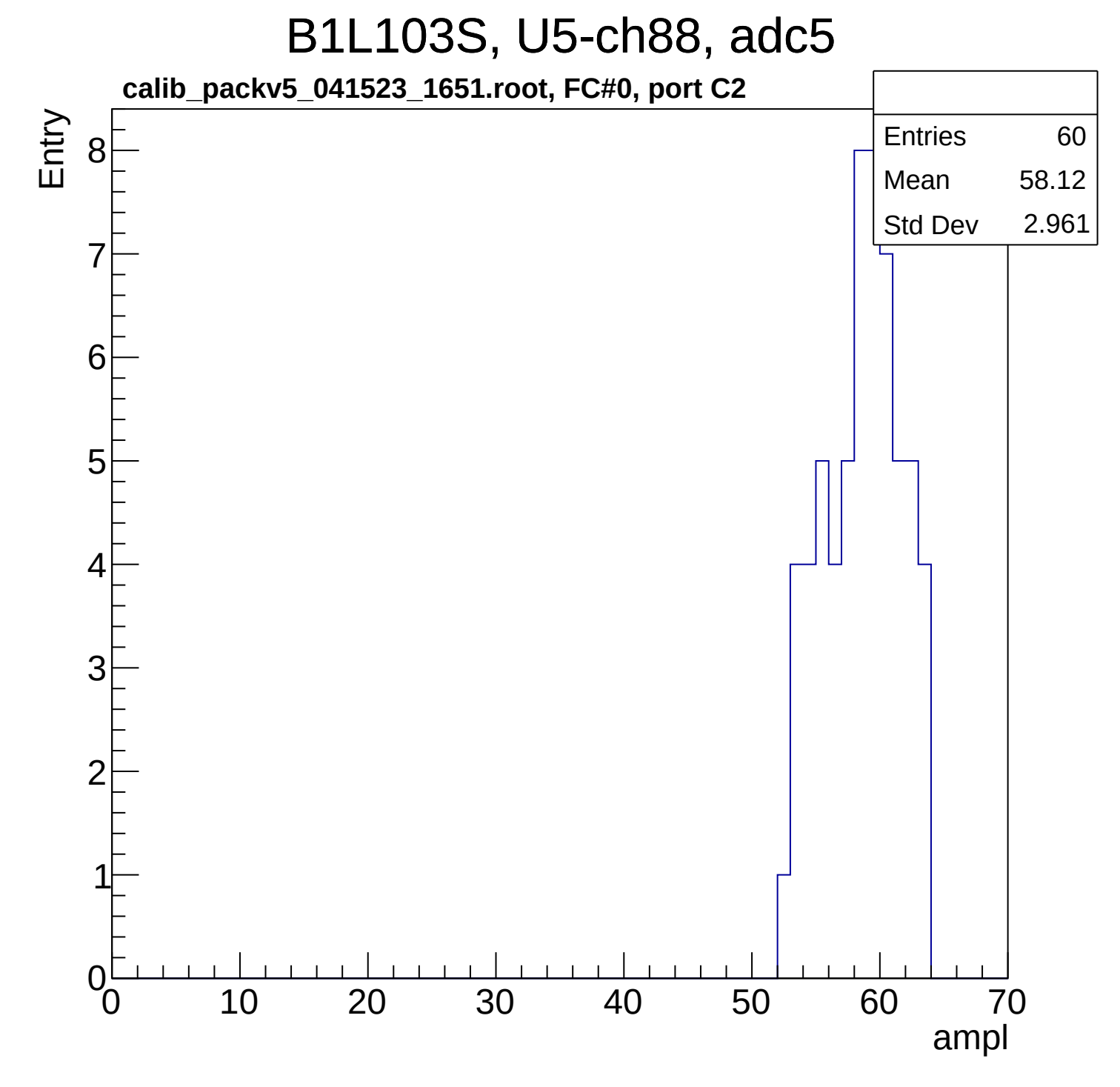

B1L103S, U5-ch88, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 53.33
Std Dev 3.116
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch88, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 58.12
Std Dev 2.961
Entry
ampl
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1
2
3
4
5
6
7
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20
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60
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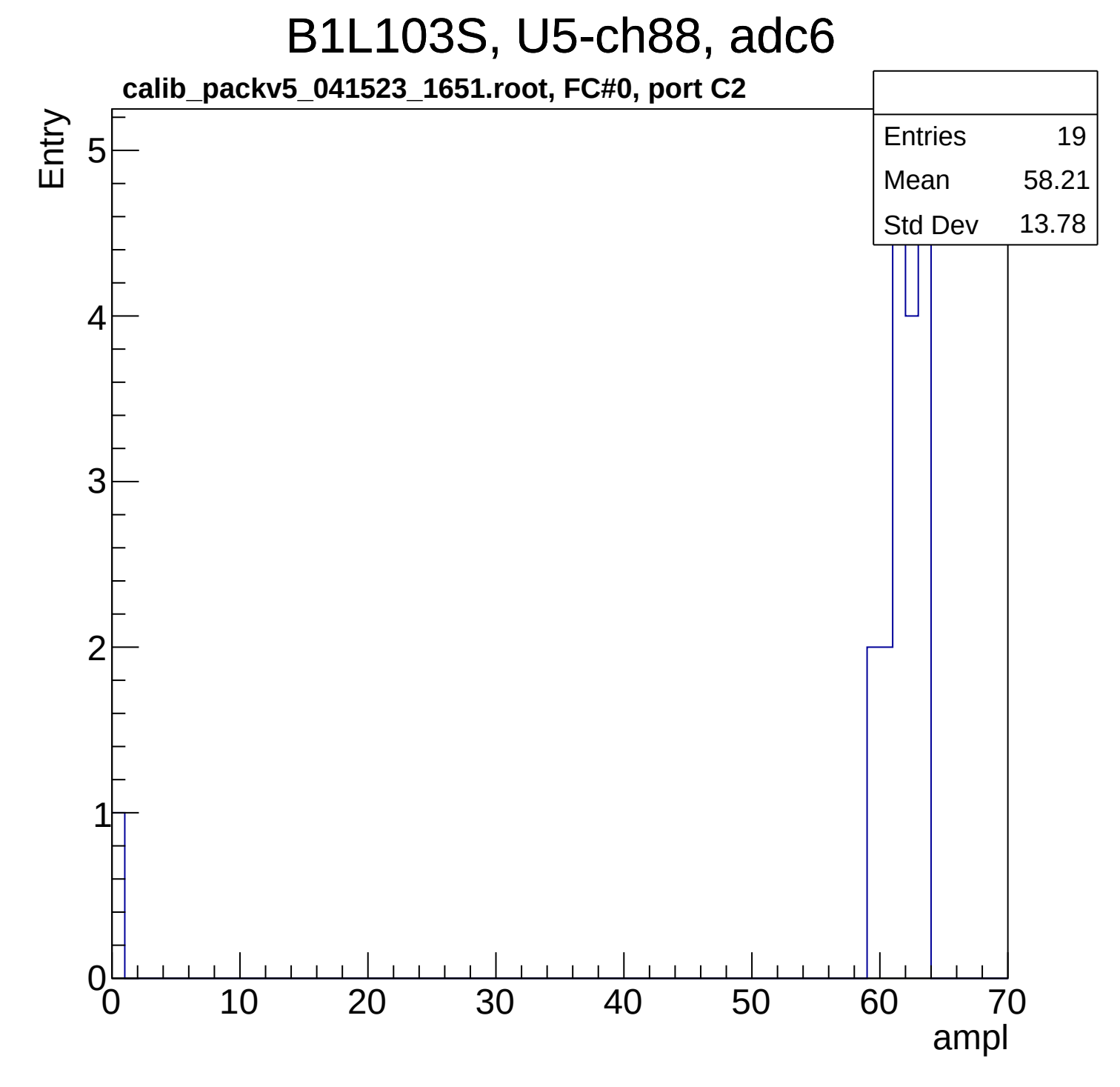
B1L103S, U5-ch88, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 58.21
Std Dev 13.78
Entry
ampl
0
1
2
3
4
5
0
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40
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60
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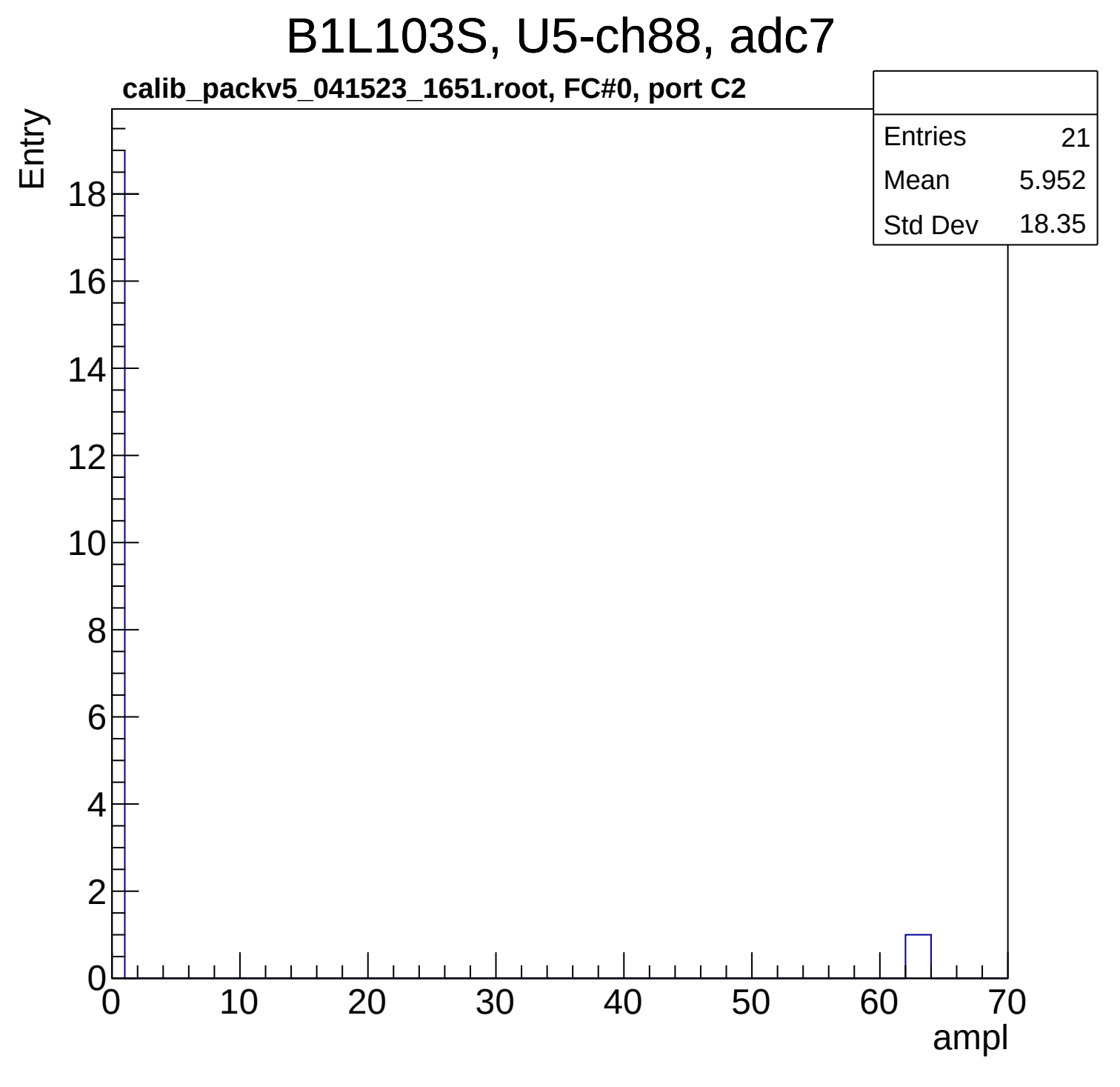
B1L103S, U5-ch88, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
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8
10
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10
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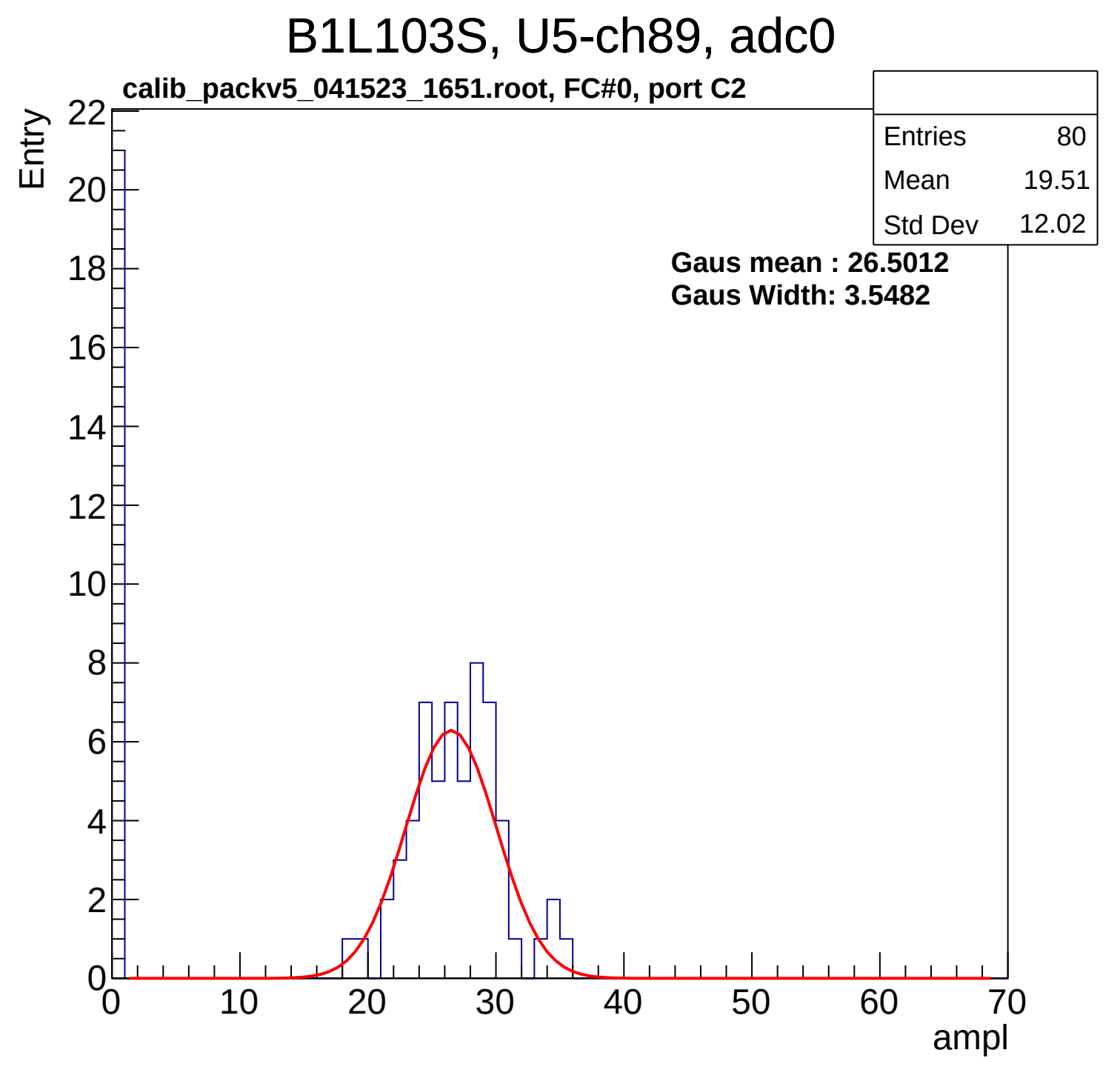
60
70
ampl


B1L103S, U5-ch89, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 19.51
Std Dev 12.02
Gaus mean : 26.5012
Gaus Width: 3.5482
Entry
ampl
0
2
4
6
8
10
12
14
16
18
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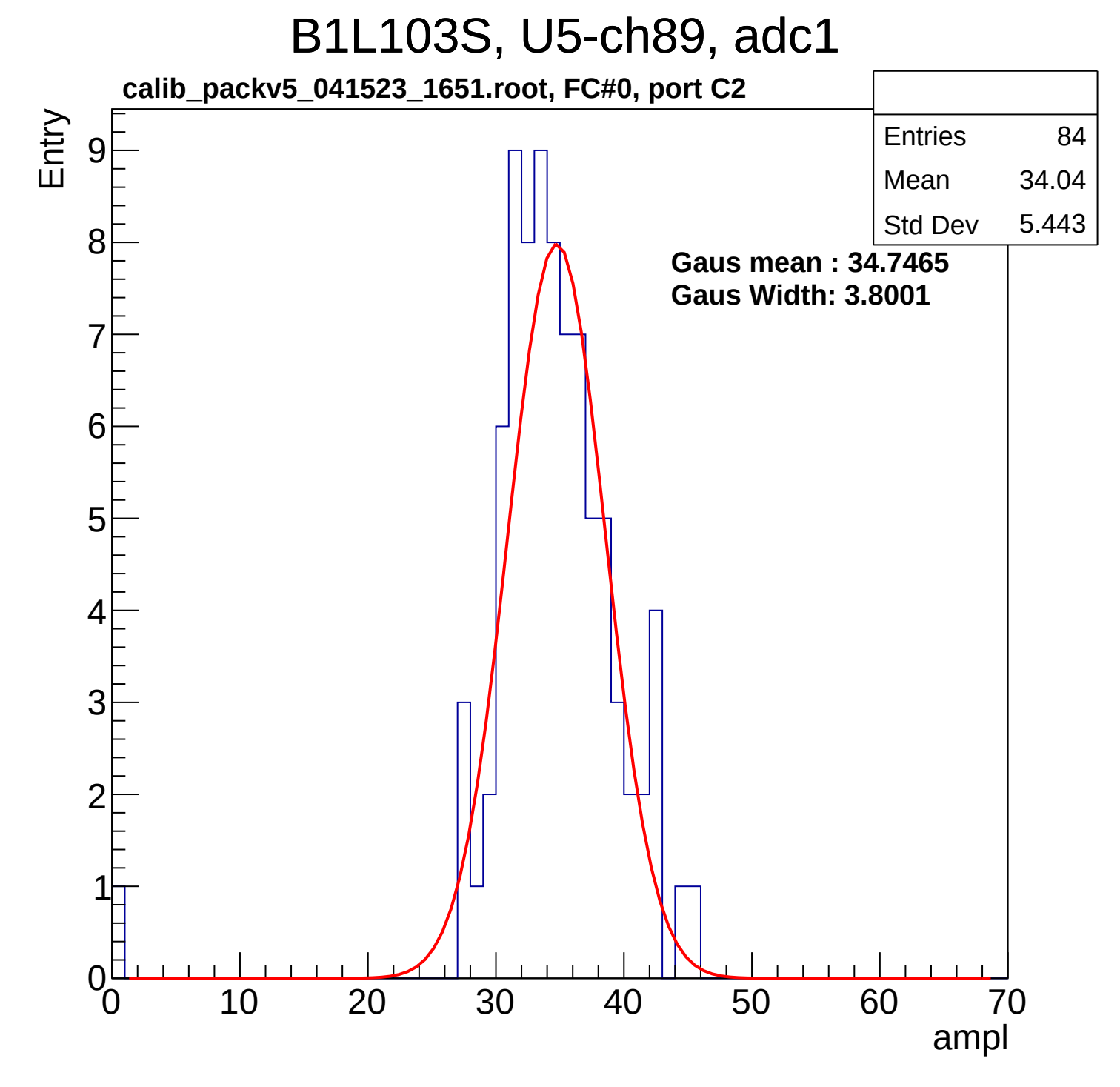
B1L103S, U5-ch89, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 34.04
Std Dev 5.443
Gaus mean : 34.7465
Gaus Width: 3.8001
Entry
ampl
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3
4
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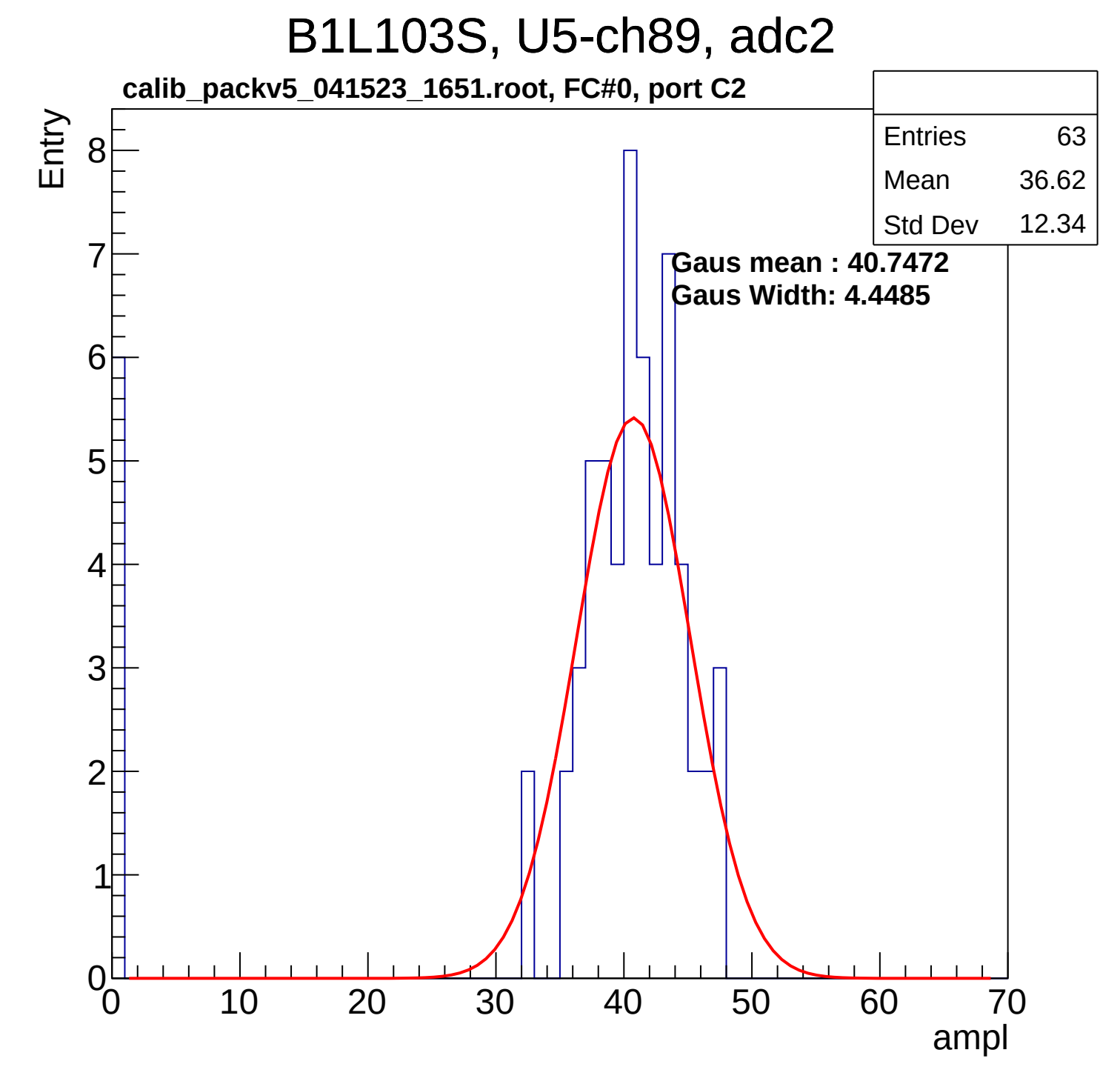
B1L103S, U5-ch89, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 36.62
Std Dev 12.34
Gaus mean : 40.7472
Gaus Width: 4.4485
Entry
ampl
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2
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5
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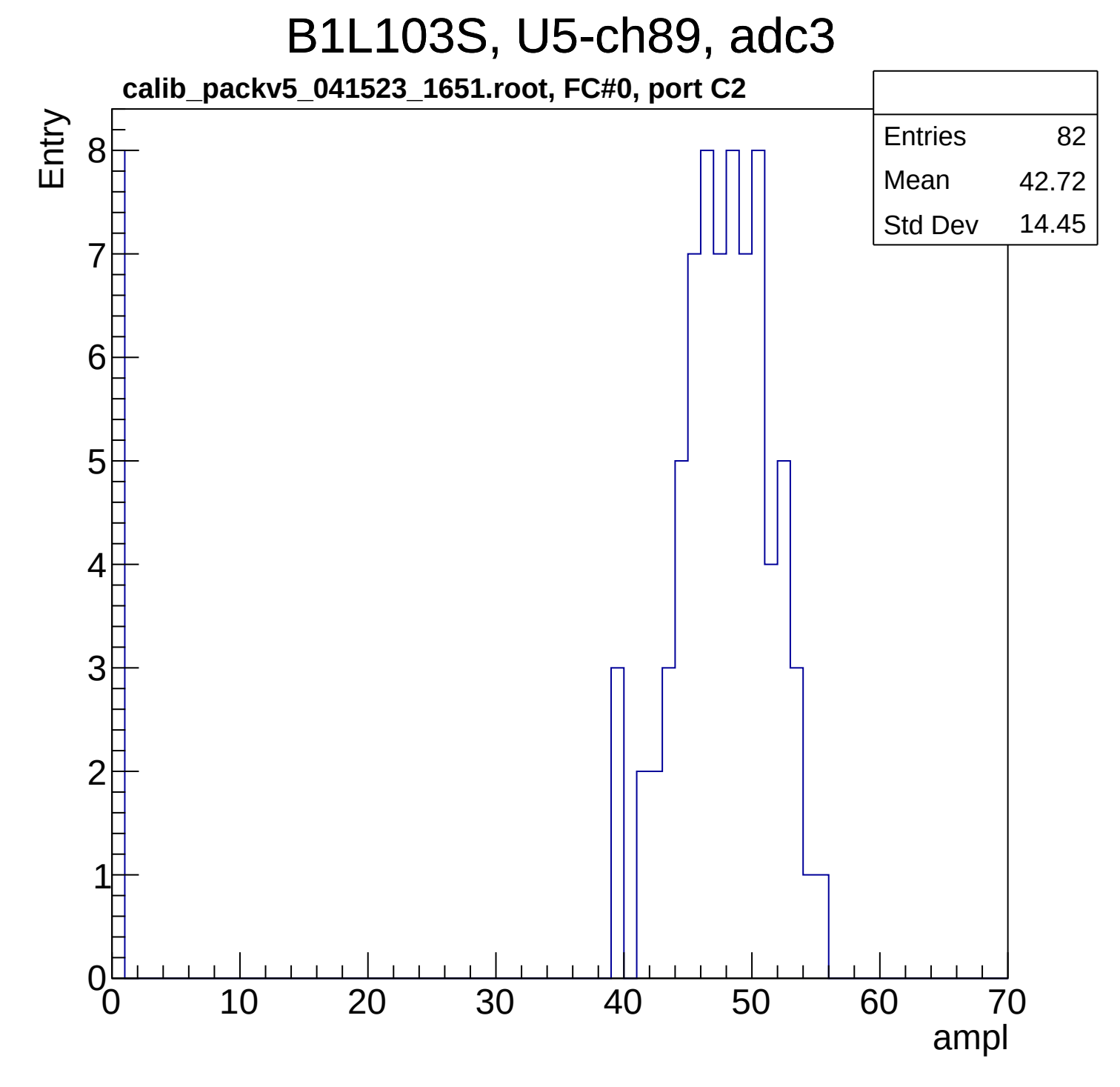
B1L103S, U5-ch89, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 42.72
Std Dev 14.45
Entry
ampl
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4
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0
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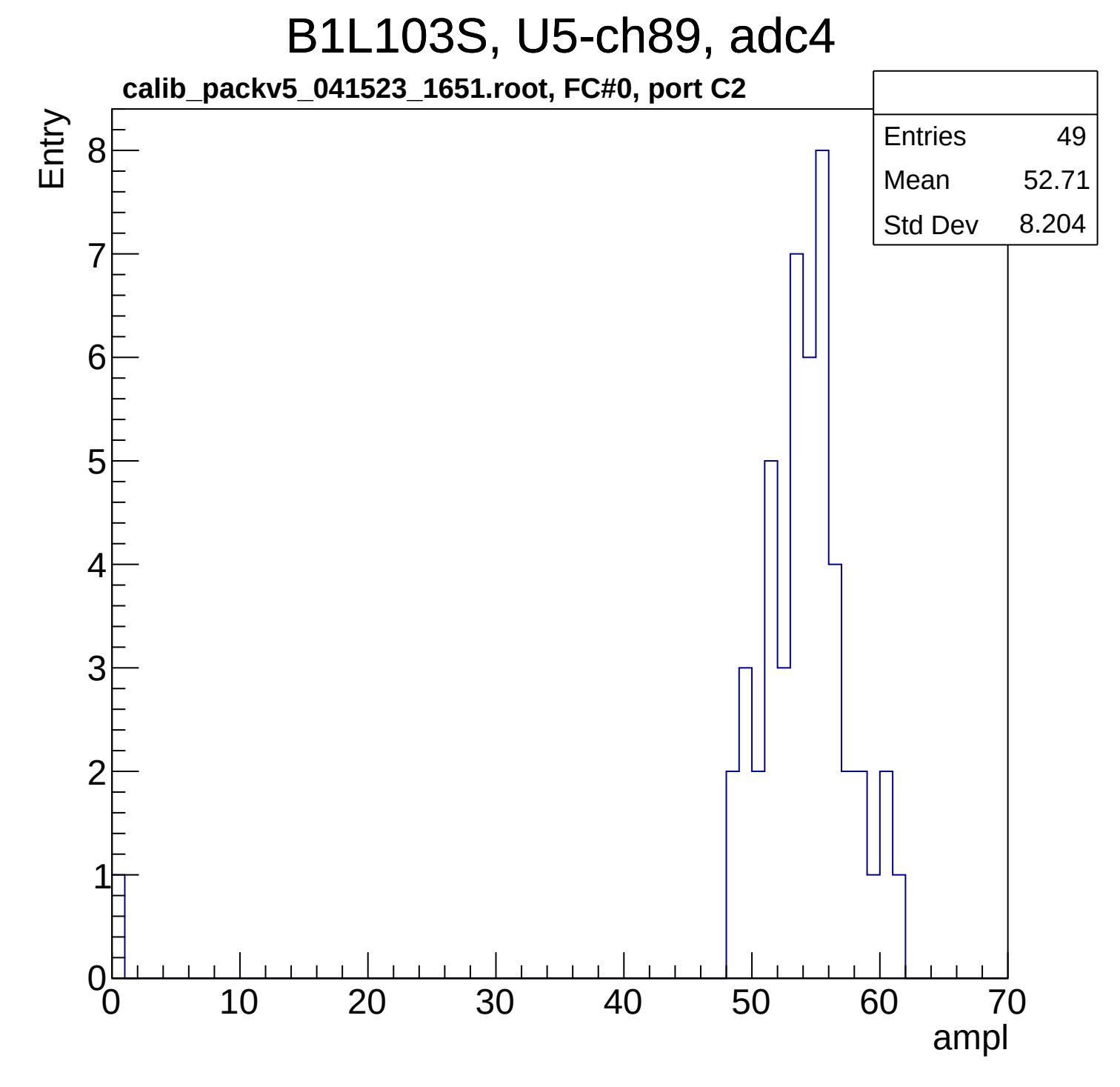
B1L103S, U5-ch89, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 52.71
Std Dev 8.204
Entry
ampl
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3
4
5
6
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0
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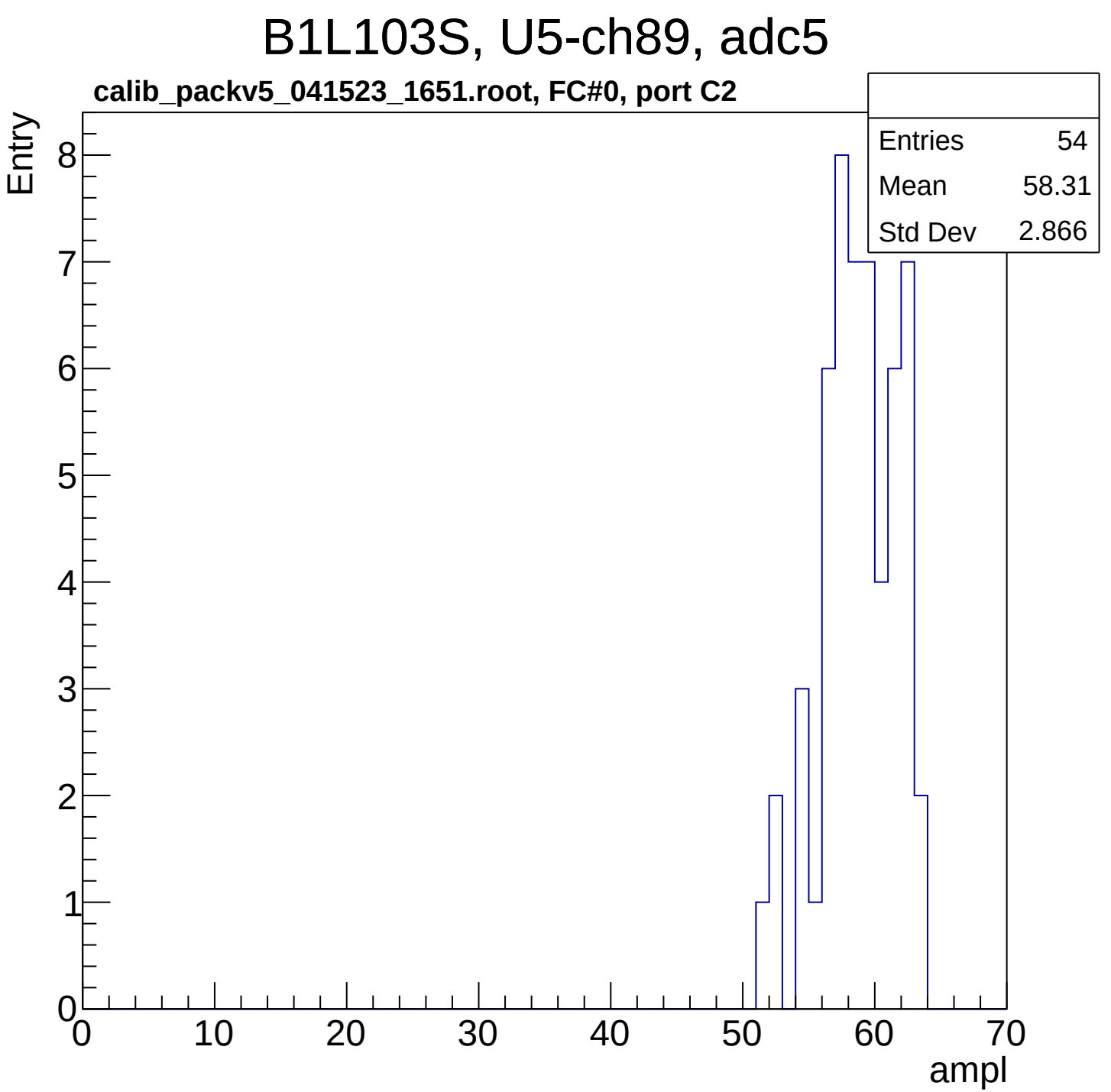
B1L103S, U5-ch89, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.31
Std Dev 2.866
Entry
ampl
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5
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0
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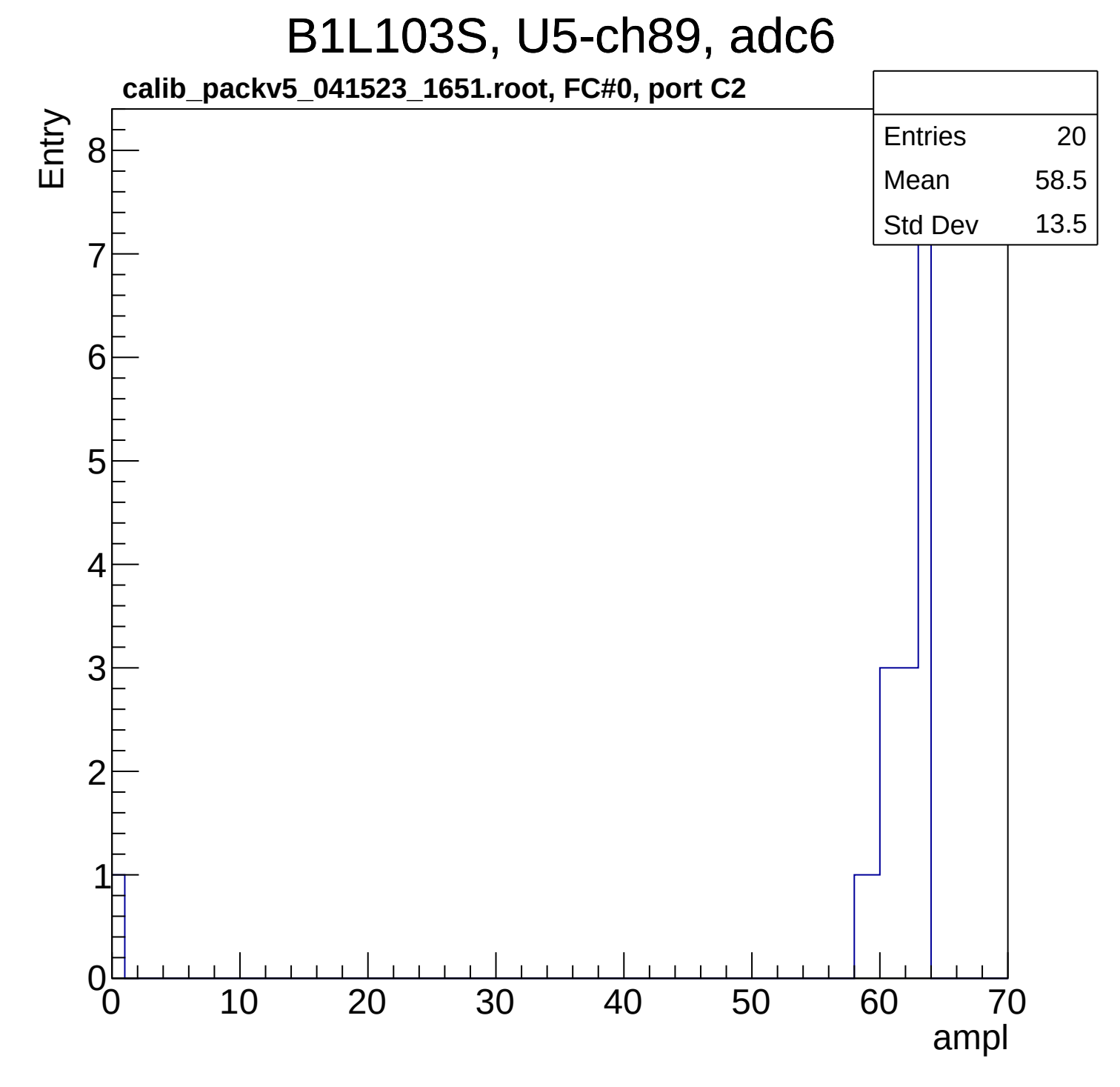
B1L103S, U5-ch89, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 58.5
Std Dev 13.5
Entry
ampl
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2
3
4
5
6
7
8
0
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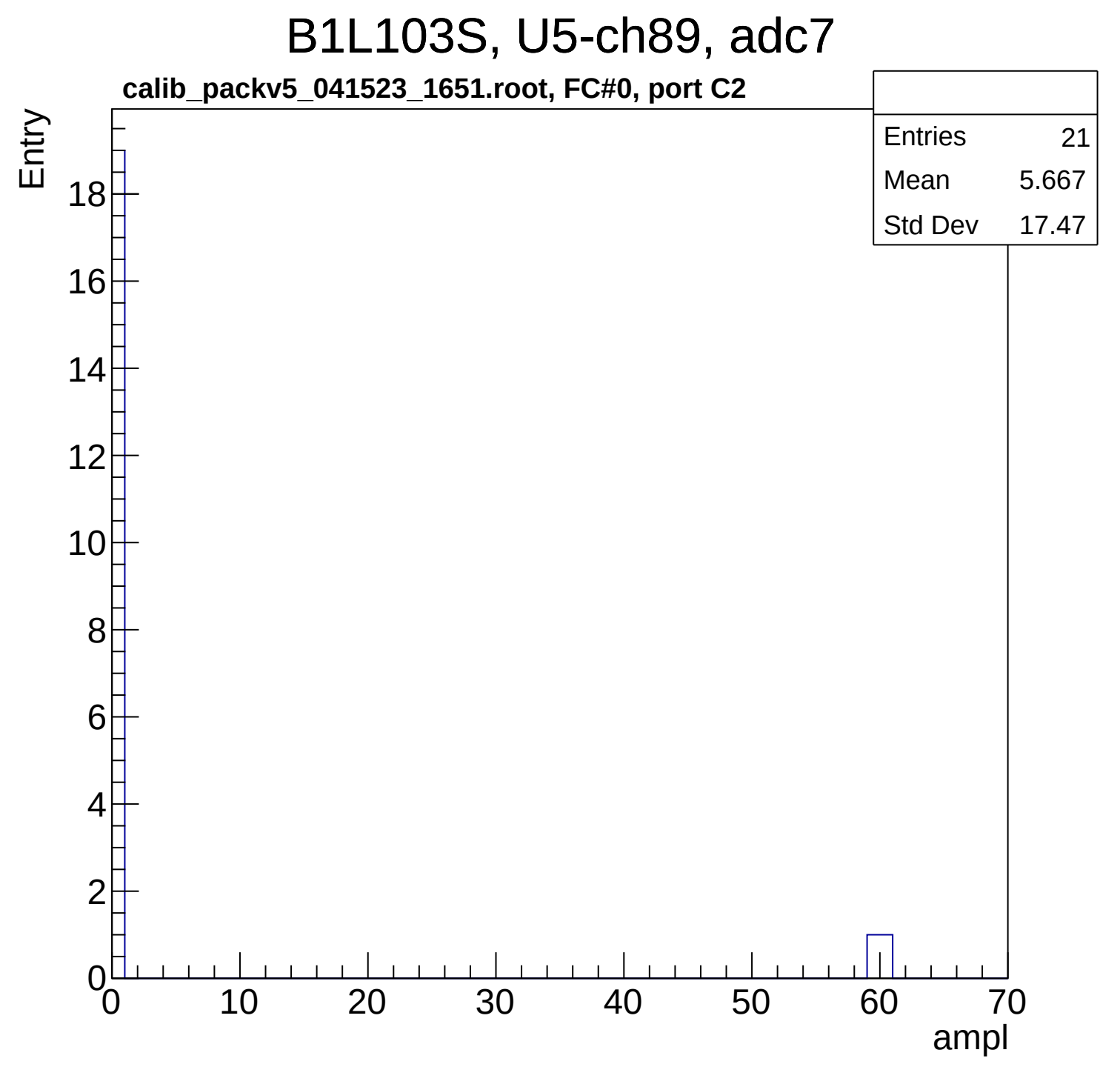
B1L103S, U5-ch89, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.667
Std Dev 17.47
Entry
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6
8
10
12
14
16
18
0
10
20
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50
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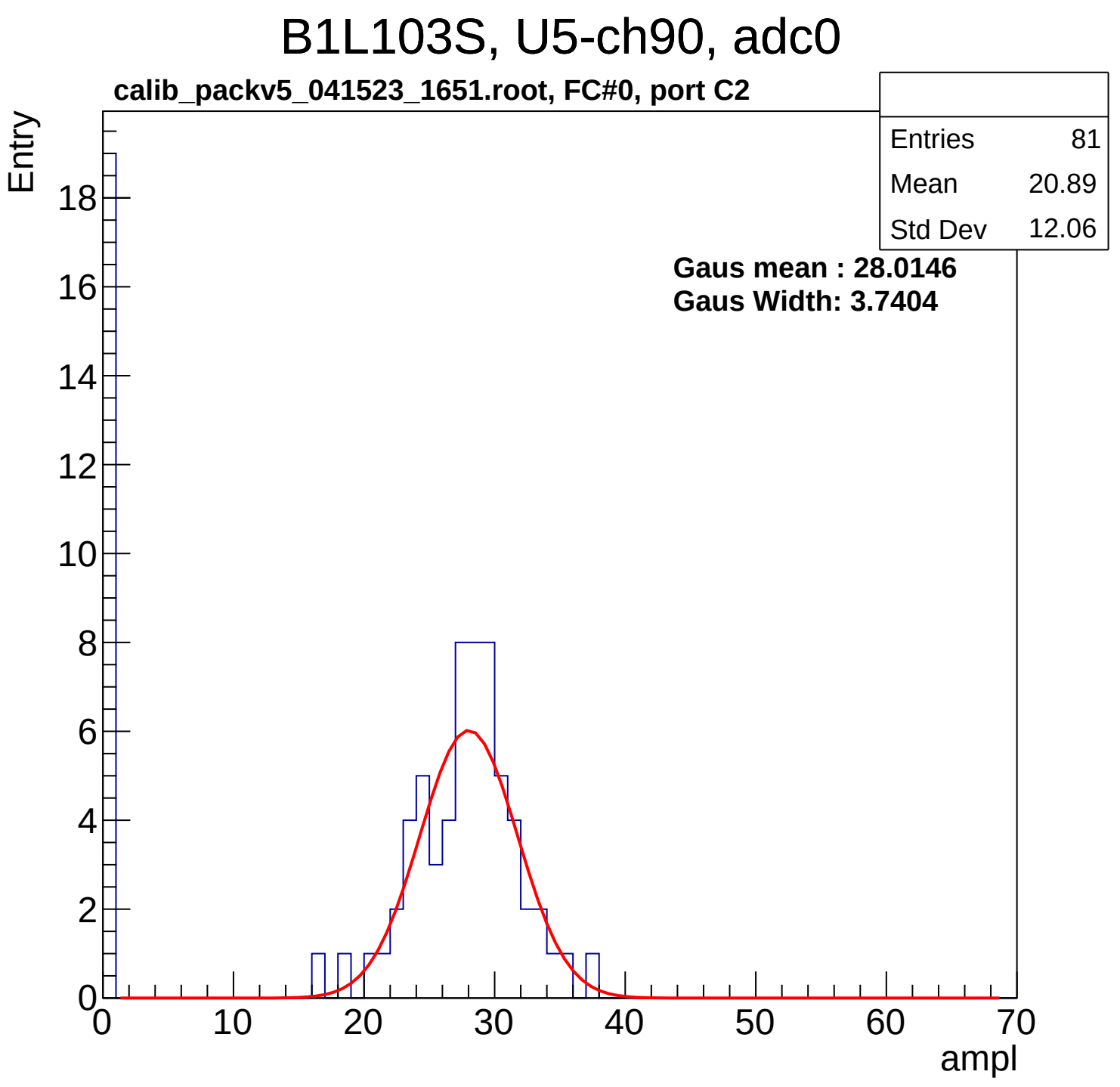
70
ampl


B1L103S, U5-ch90, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 20.89
Std Dev 12.06
Gaus mean : 28.0146
Gaus Width: 3.7404
Entry
ampl
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6
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10
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14
16
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0
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40
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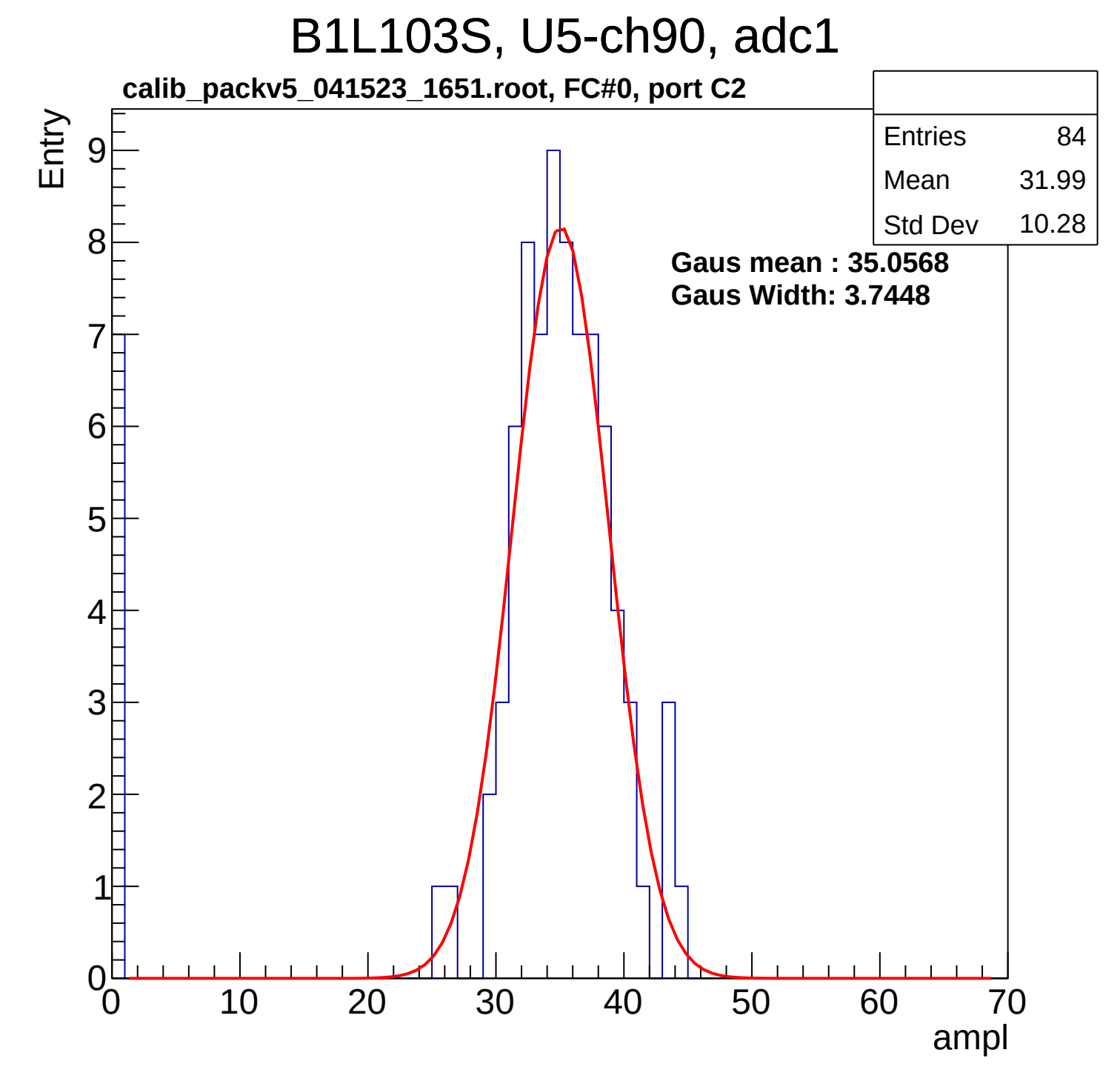
B1L103S, U5-ch90, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 31.99
Std Dev 10.28
Gaus mean : 35.0568
Gaus Width: 3.7448
Entry
ampl
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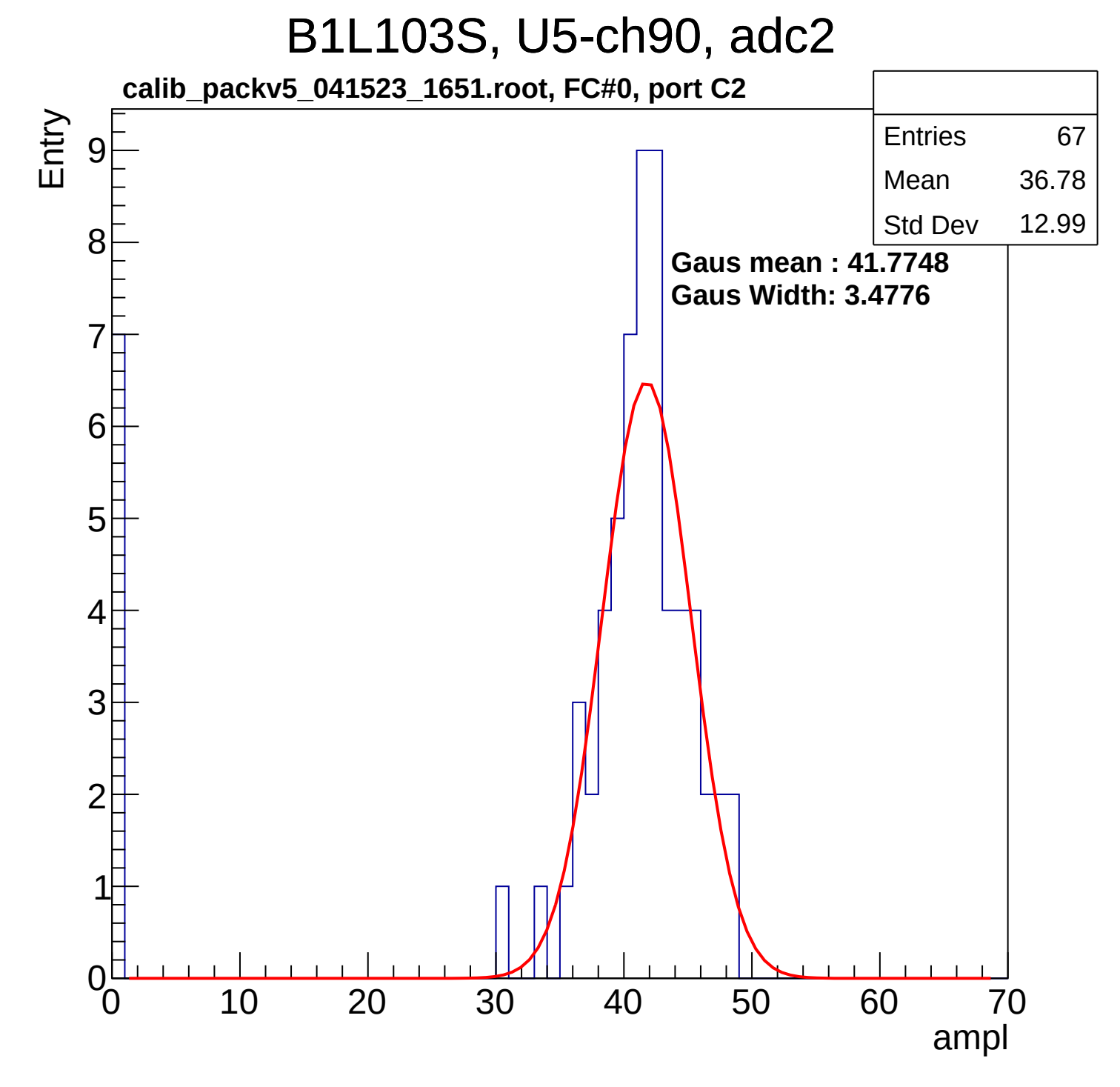
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U5-ch90, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 36.78
Std Dev 12.99
Gaus mean : 41.7748
Gaus Width: 3.4776
Entry
ampl
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20
30
40
50
60
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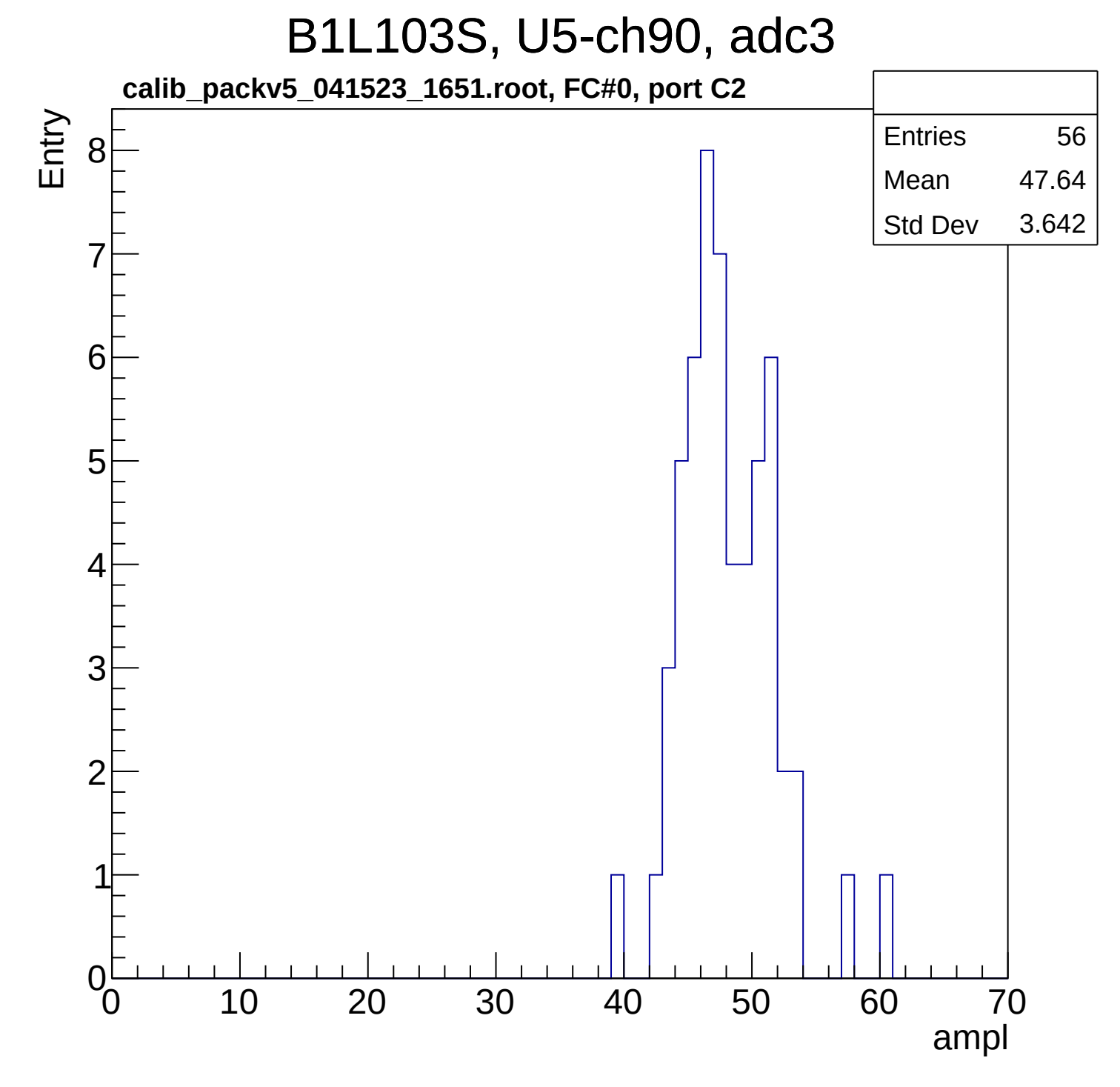
1
2
3
4
5
6
7
8
9


B1L103S, U5-ch90, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 47.64
Std Dev 3.642
Entry
ampl
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3
4
5
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0
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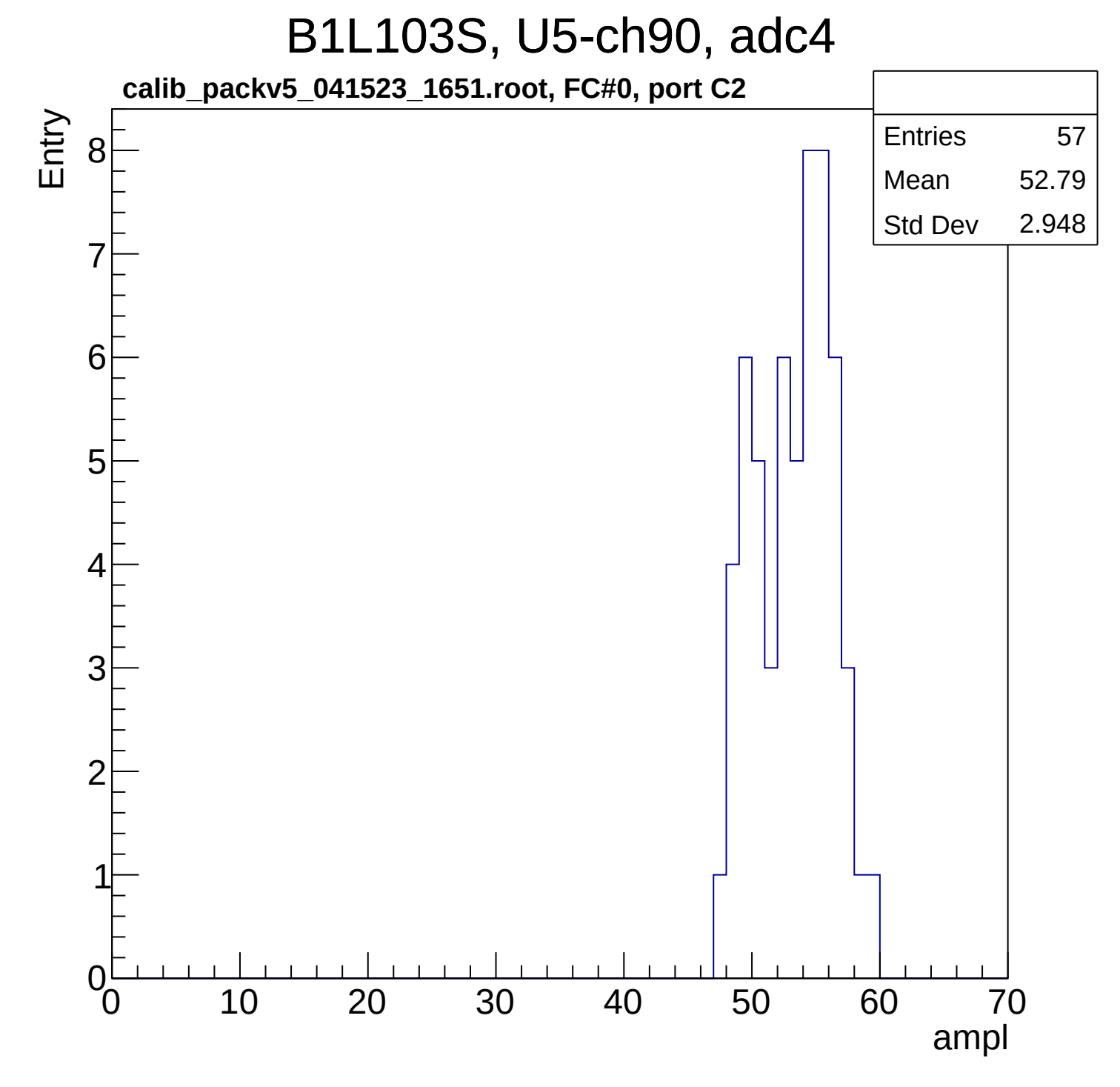
B1L103S, U5-ch90, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 52.79
Std Dev 2.948
Entry
ampl
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0
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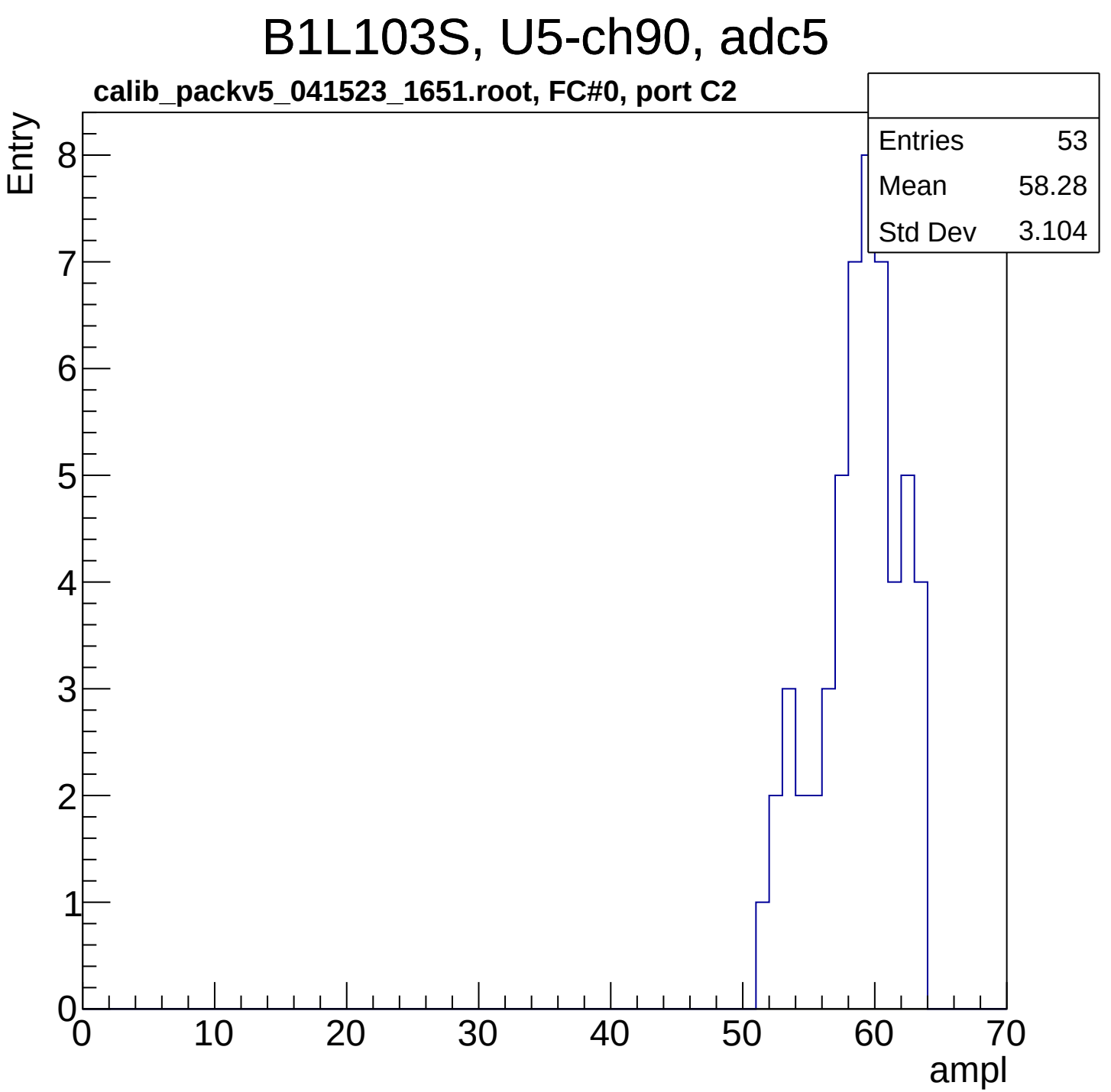
B1L103S, U5-ch90, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.28
Std Dev 3.104
Entry
ampl
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2
3
4
5
6
7
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0
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40
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60
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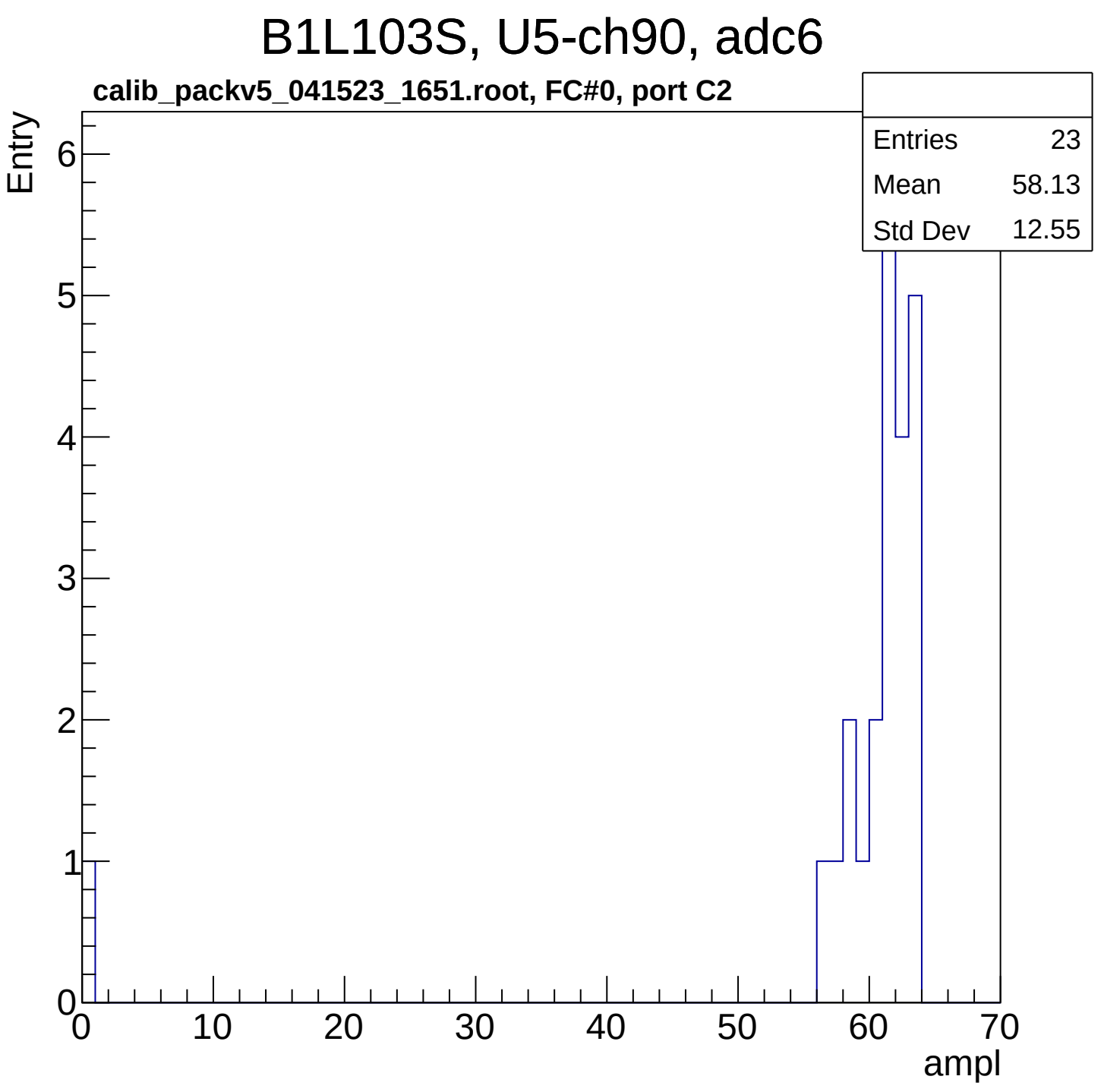
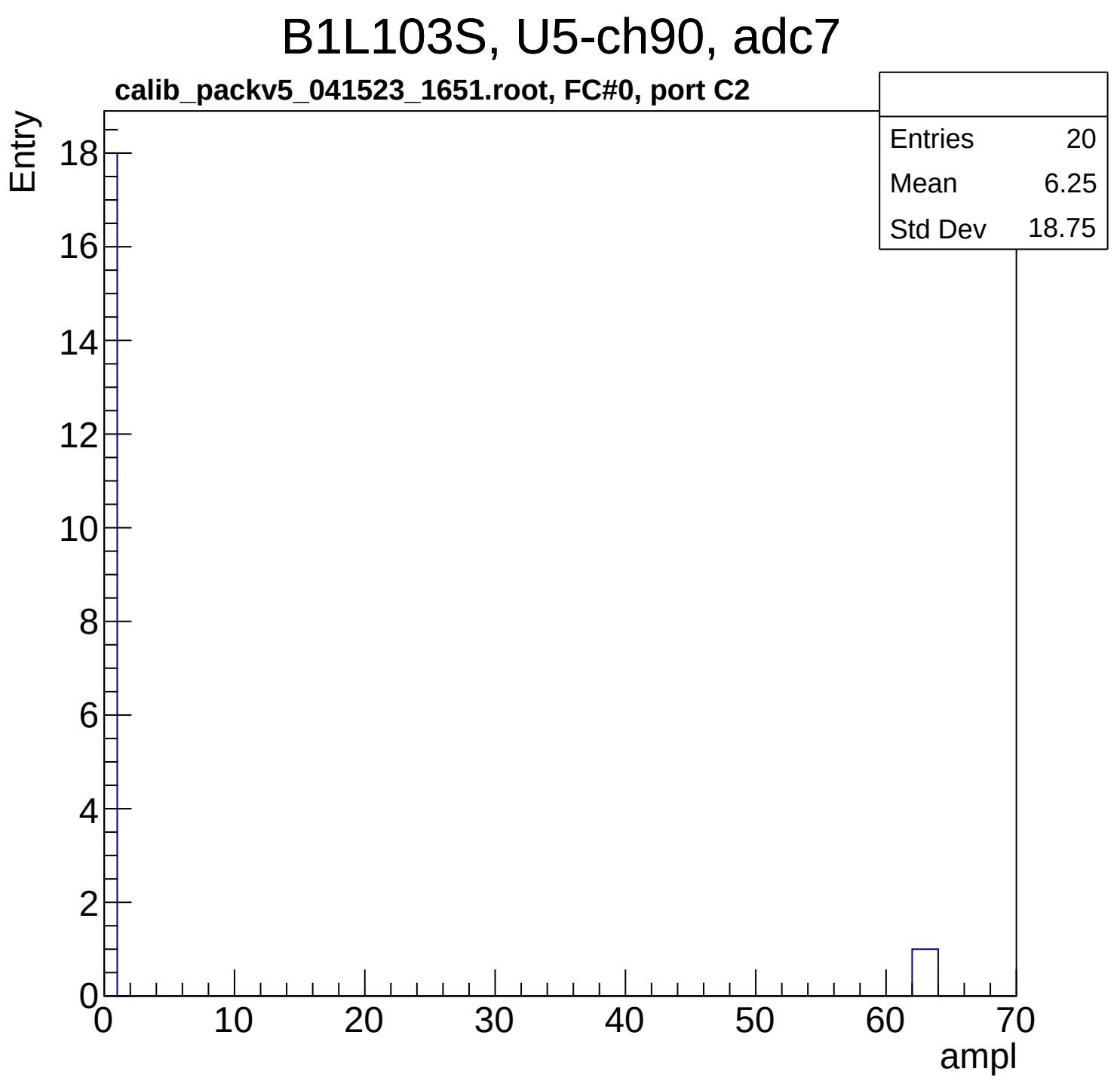

B1L103S, U5-ch90, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 58.13
Std Dev 12.55
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch90, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.25
Std Dev 18.75
Entry
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6
8
10
12
14
16
18
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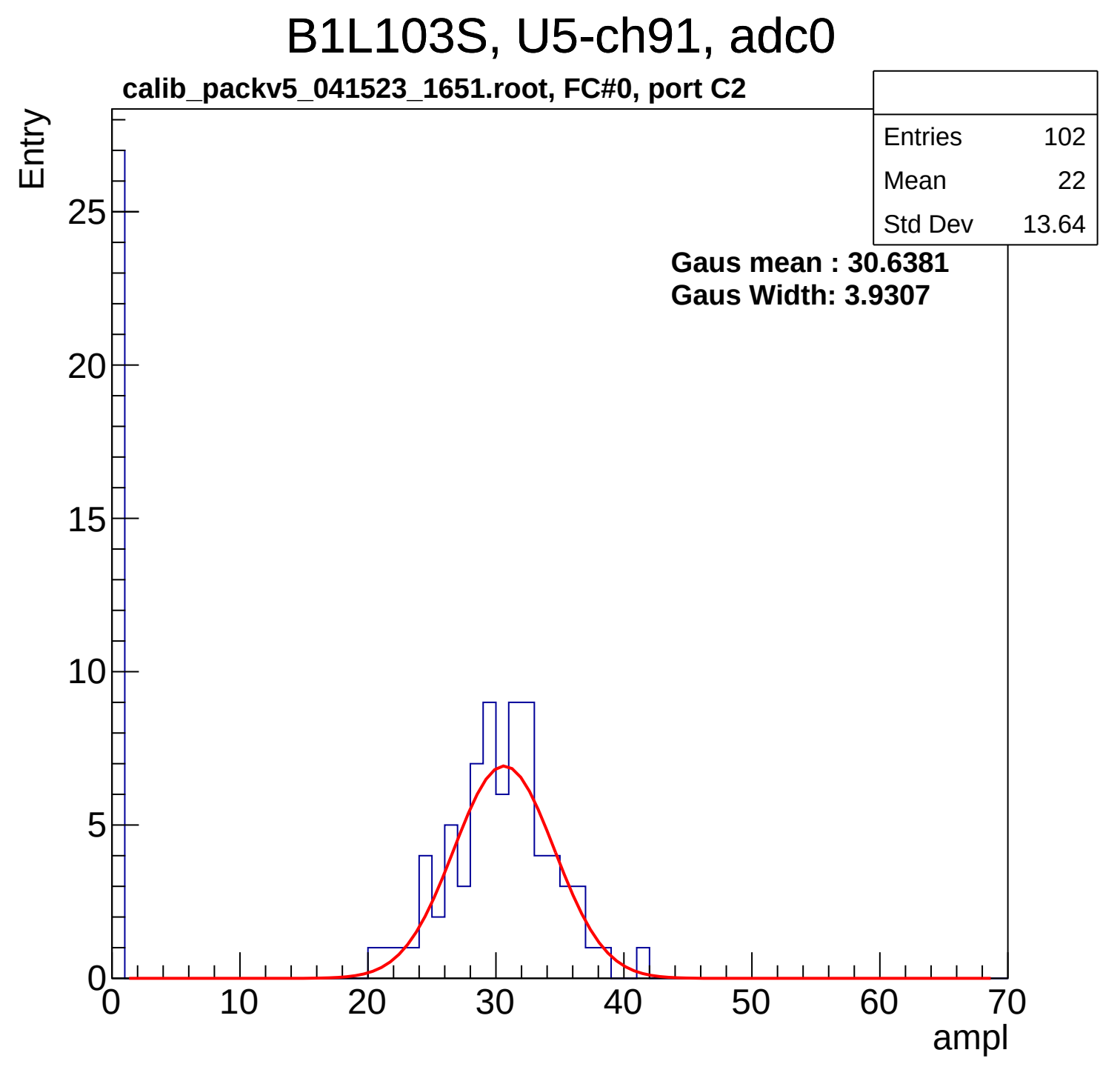
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch91, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 22
Std Dev 13.64
Gaus mean : 30.6381
Gaus Width: 3.9307
Entry
ampl
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5
10
15
20
25
0
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40
50
60
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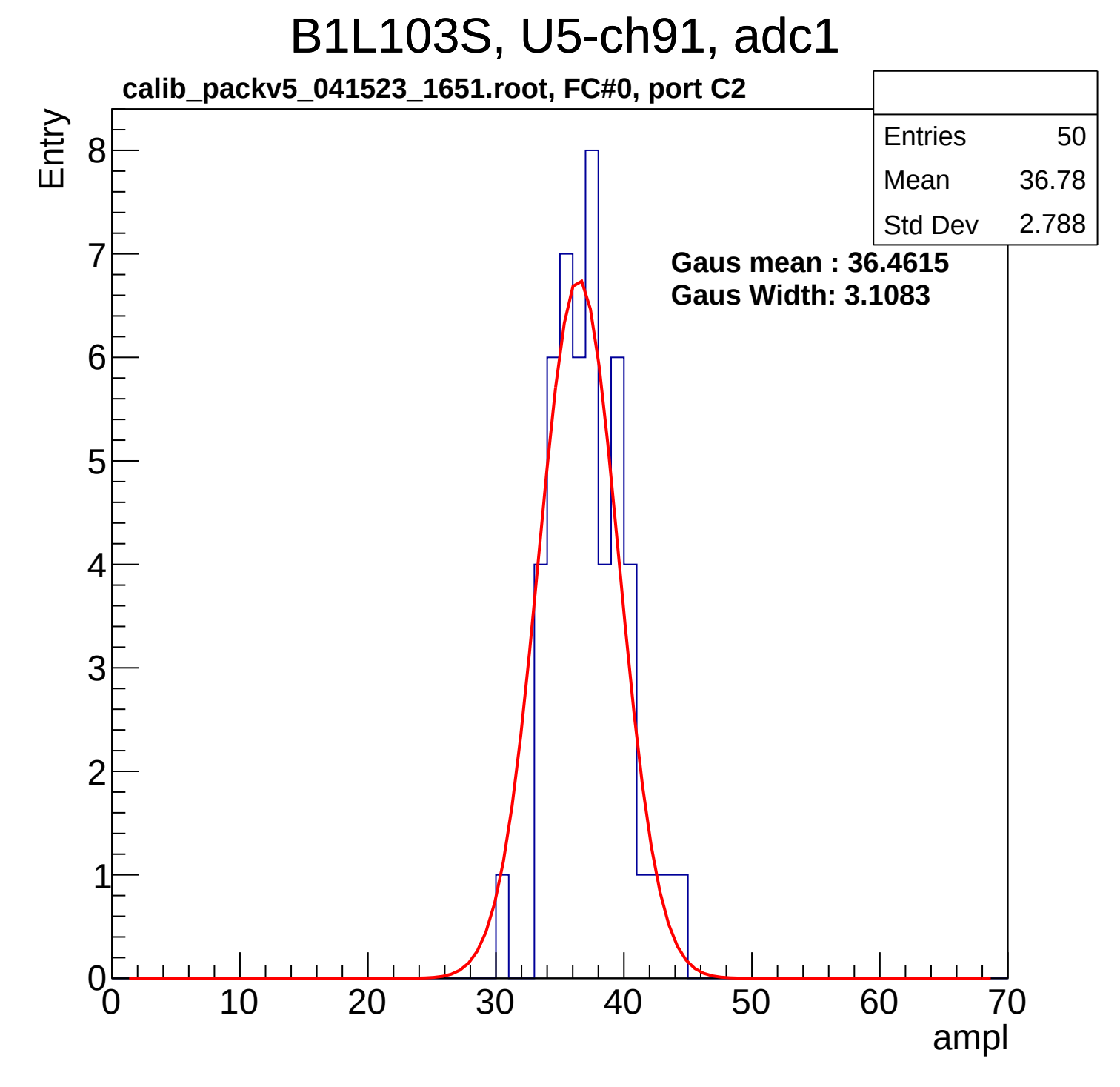
B1L103S, U5-ch91, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 36.78
Std Dev 2.788
Gaus mean : 36.4615
Gaus Width: 3.1083
Entry
ampl
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2
3
4
5
6
7
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0
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60
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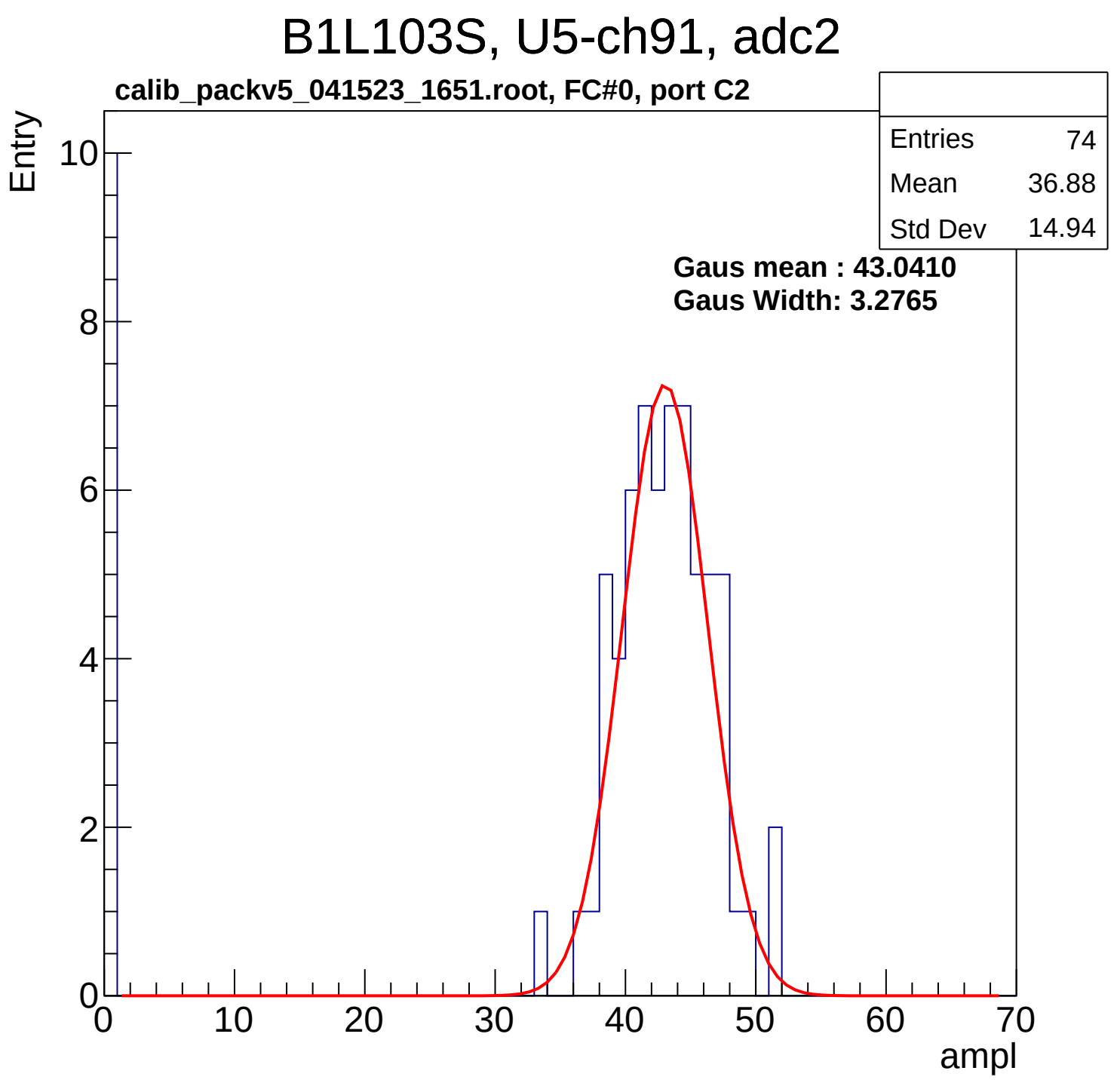
B1L103S, U5-ch91, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 36.88
Std Dev 14.94
Gaus mean : 43.0410
Gaus Width: 3.2765
Entry
ampl
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0
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40
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60
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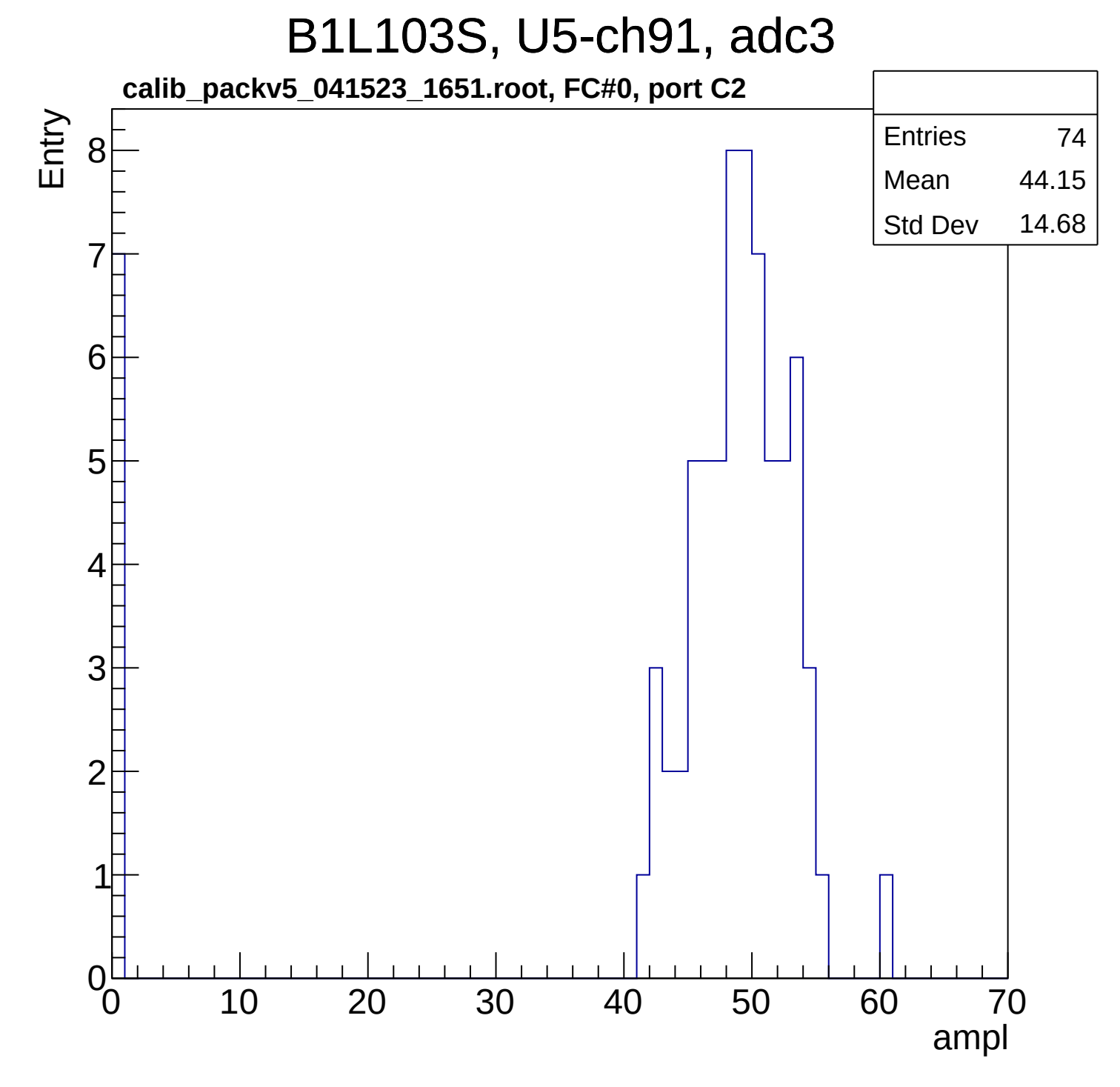
B1L103S, U5-ch91, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 44.15
Std Dev 14.68
Entry
ampl
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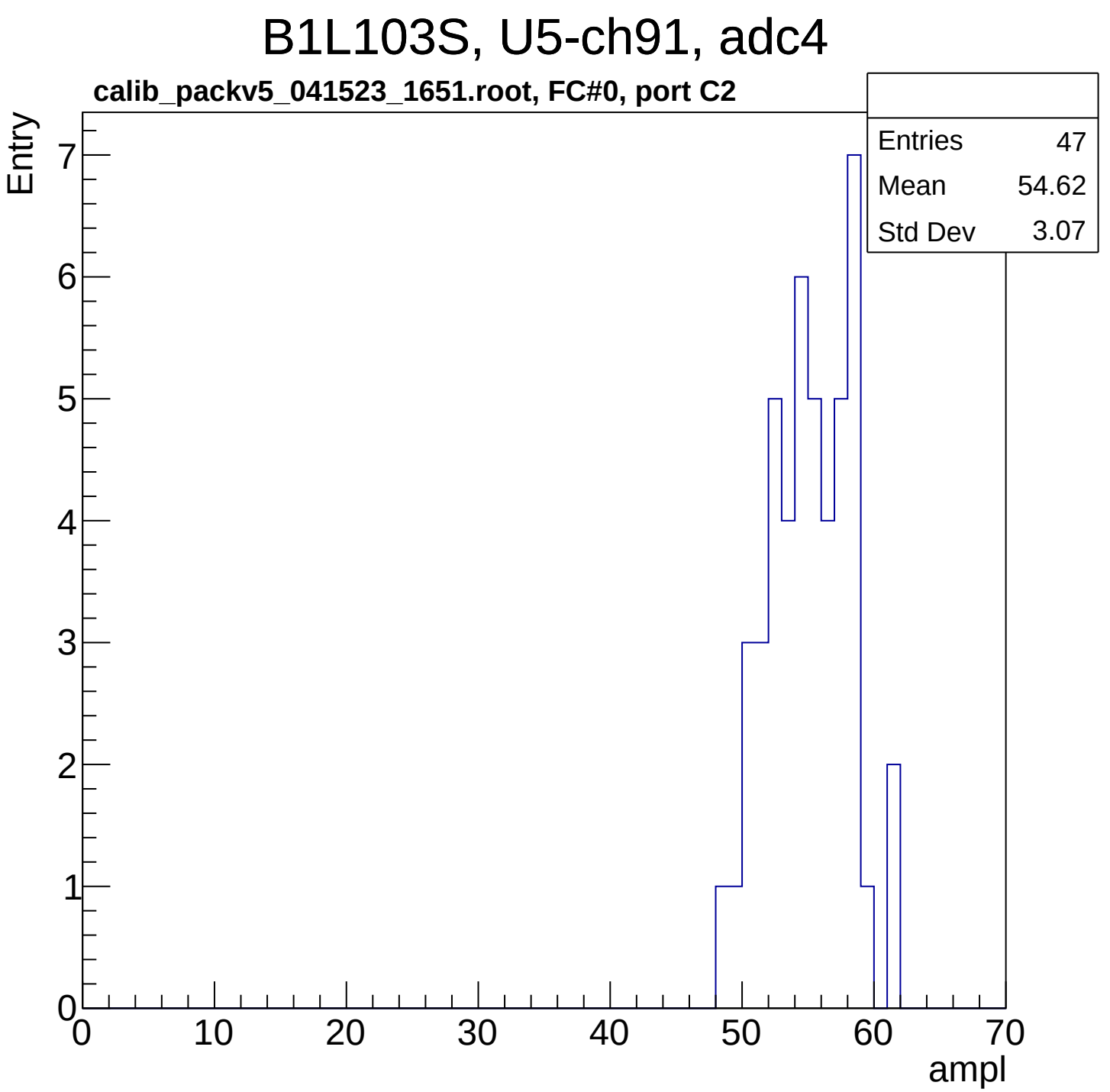
B1L103S, U5-ch91, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 54.62
Std Dev 3.07
Entry
ampl
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0
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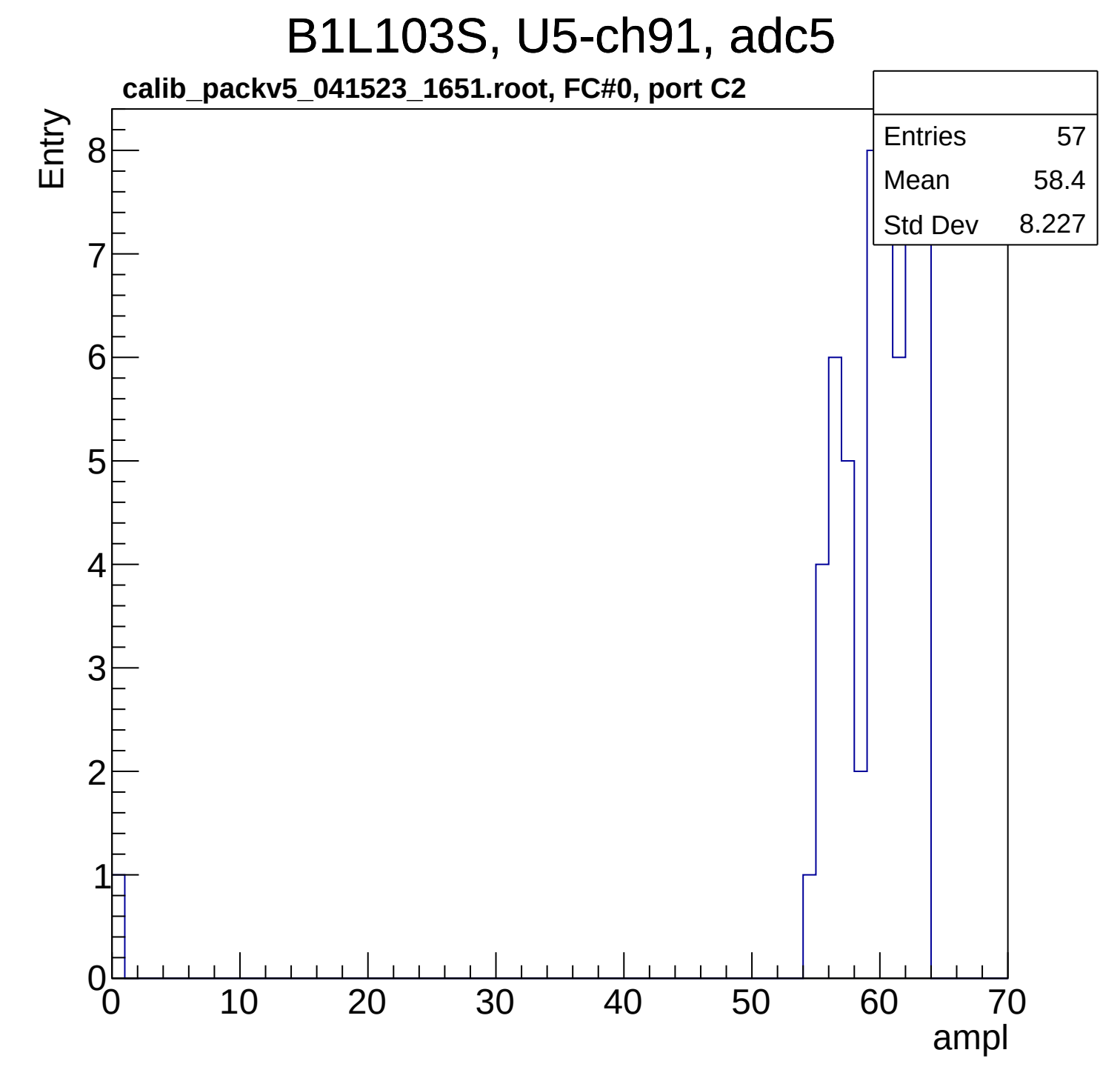
B1L103S, U5-ch91, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.4
Std Dev 8.227
Entry
ampl
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0
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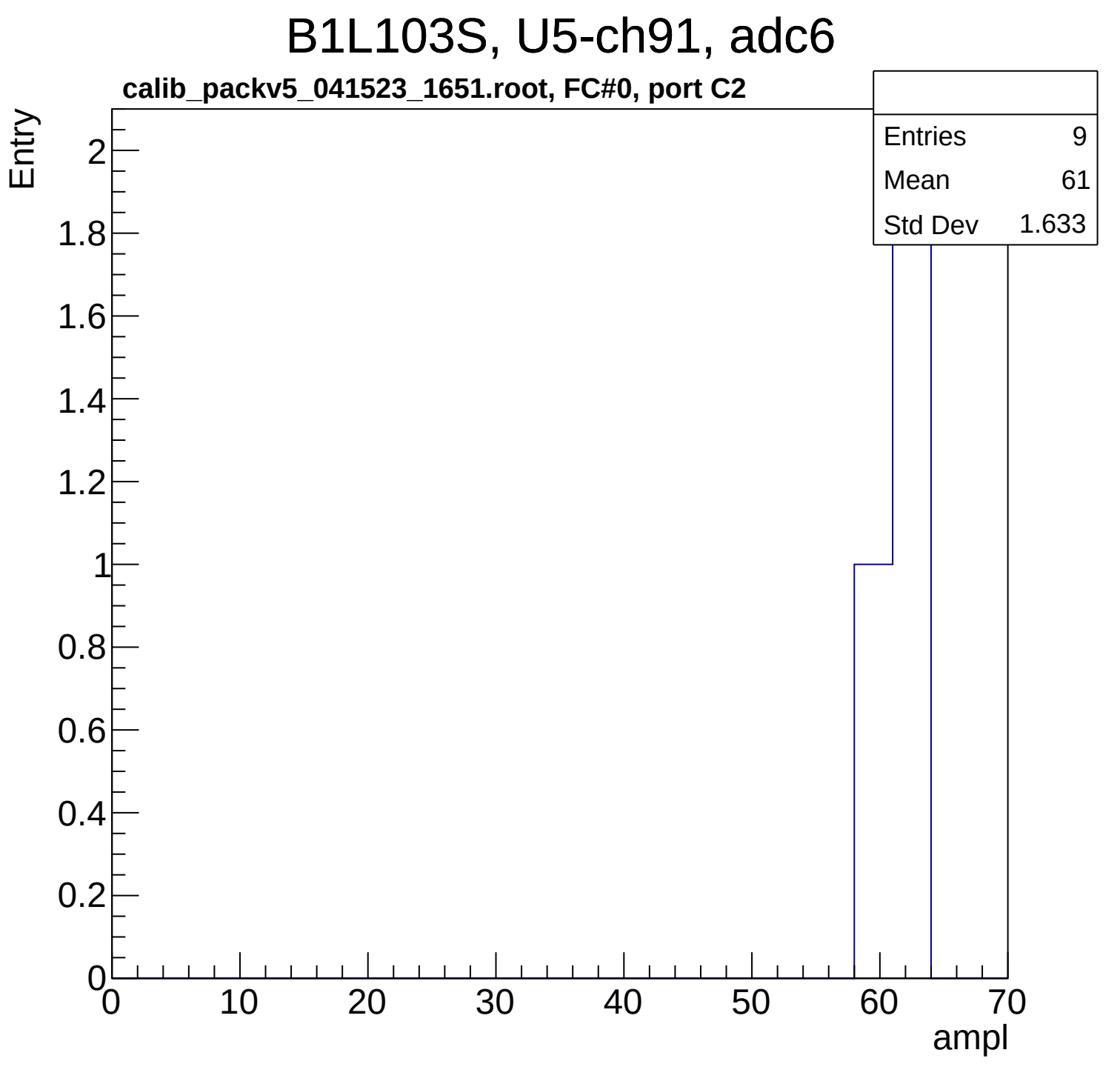
B1L103S, U5-ch91, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61
Std Dev 1.633
Entry
ampl
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0.2
0.4
0.6
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1
1.2
1.4
1.6
1.8
2
0
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60
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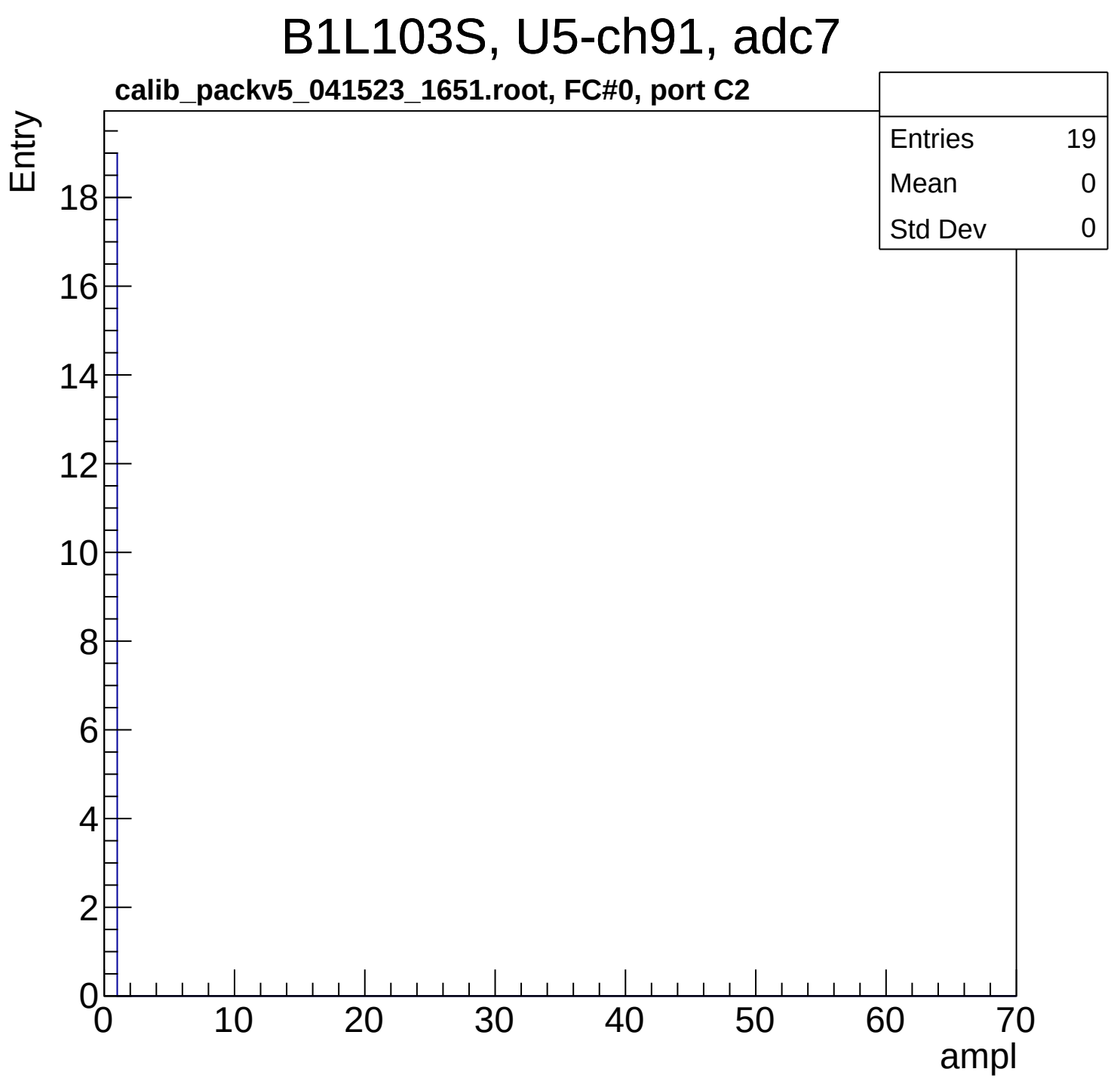
B1L103S, U5-ch91, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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10
12
14
16
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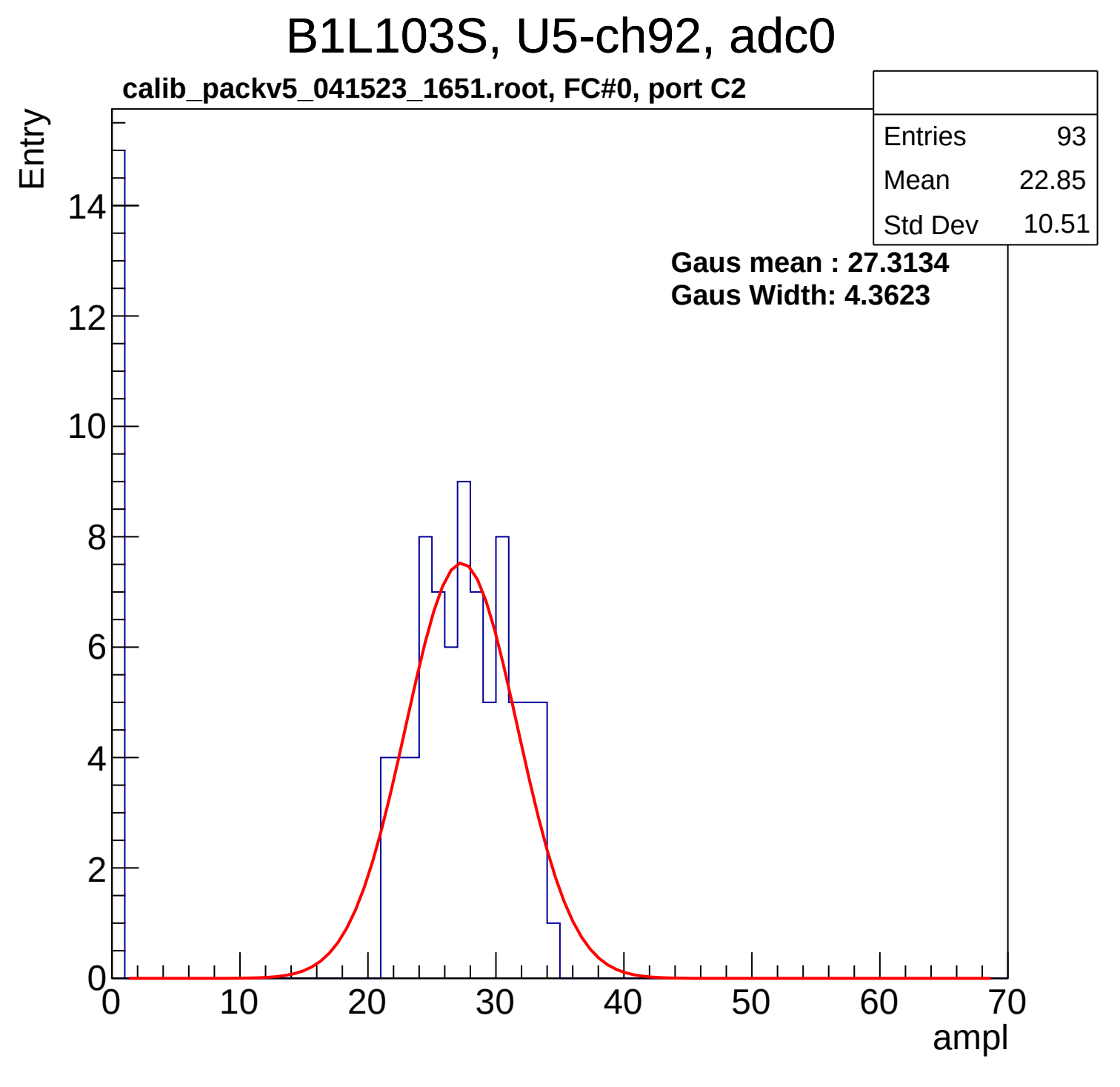
50
60
70
ampl


B1L103S, U5-ch92, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 22.85
Std Dev 10.51
Gaus mean : 27.3134
Gaus Width: 4.3623
Entry
ampl
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8
10
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0
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60
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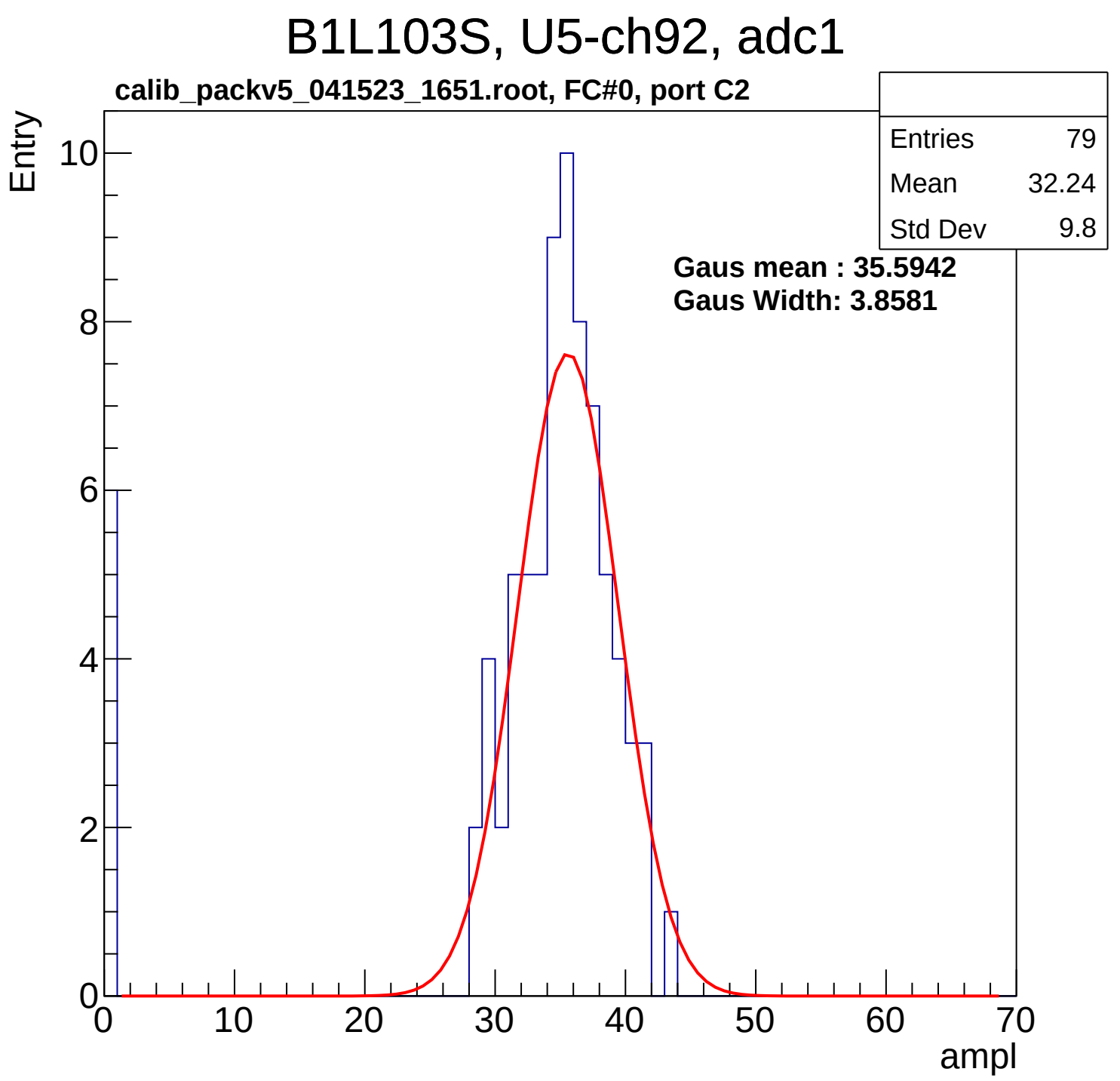
B1L103S, U5-ch92, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 32.24
Std Dev 9.8
Gaus mean : 35.5942
Gaus Width: 3.8581
Entry
ampl
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4
6
8
10
0
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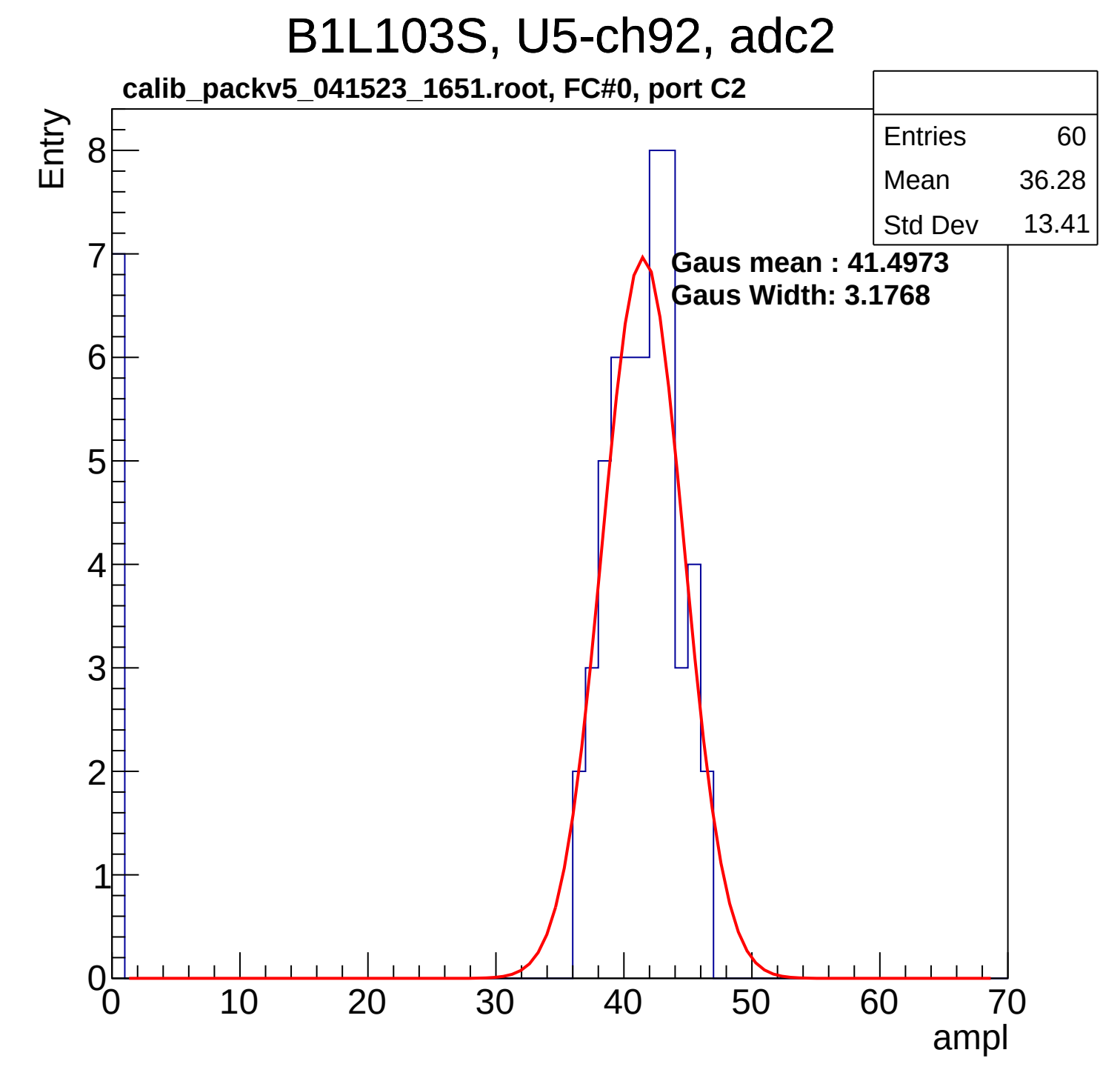
B1L103S, U5-ch92, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 36.28
Std Dev 13.41
Gaus mean : 41.4973
Gaus Width: 3.1768
Entry
ampl
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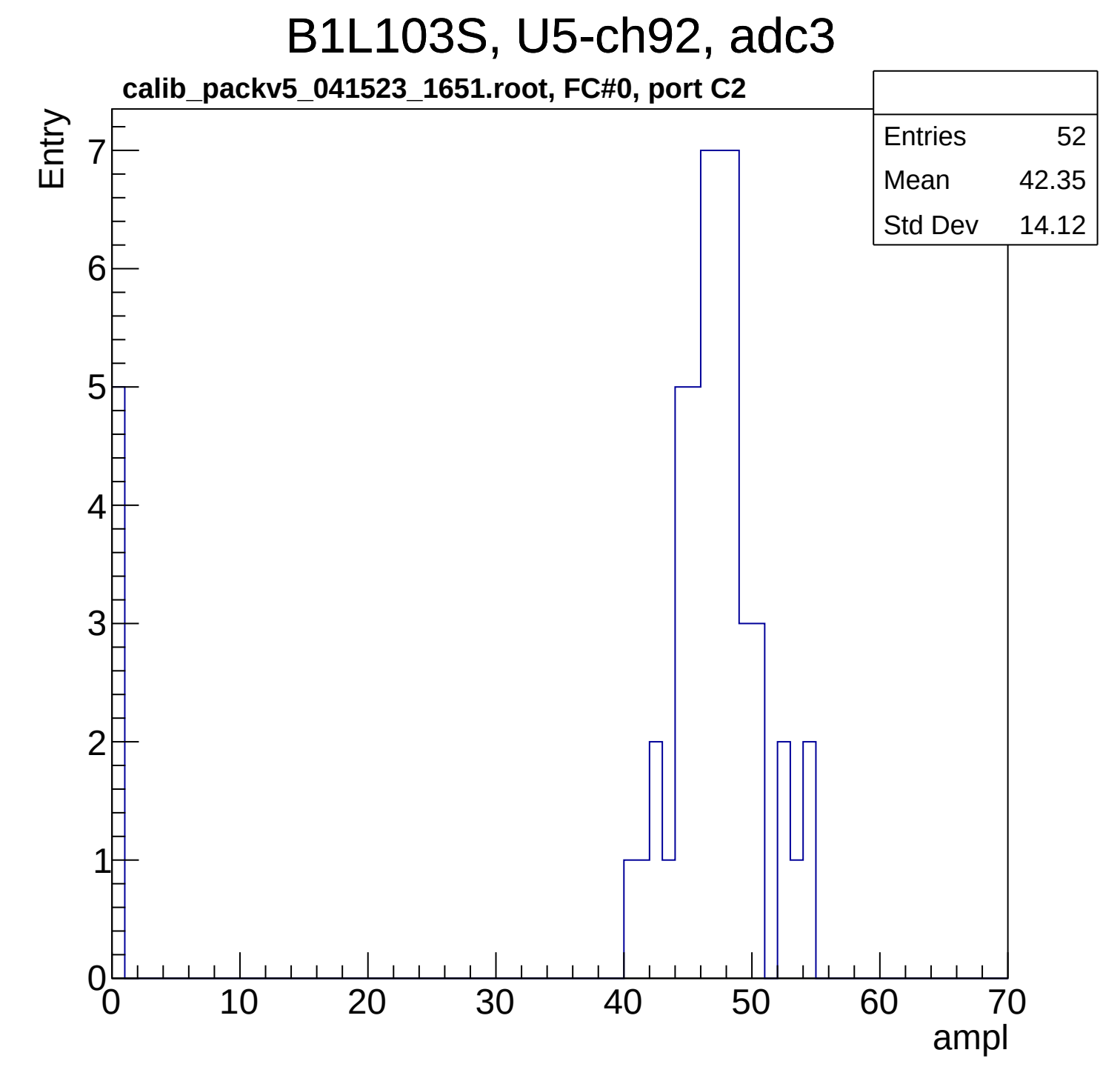
B1L103S, U5-ch92, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 42.35
Std Dev 14.12
Entry
ampl
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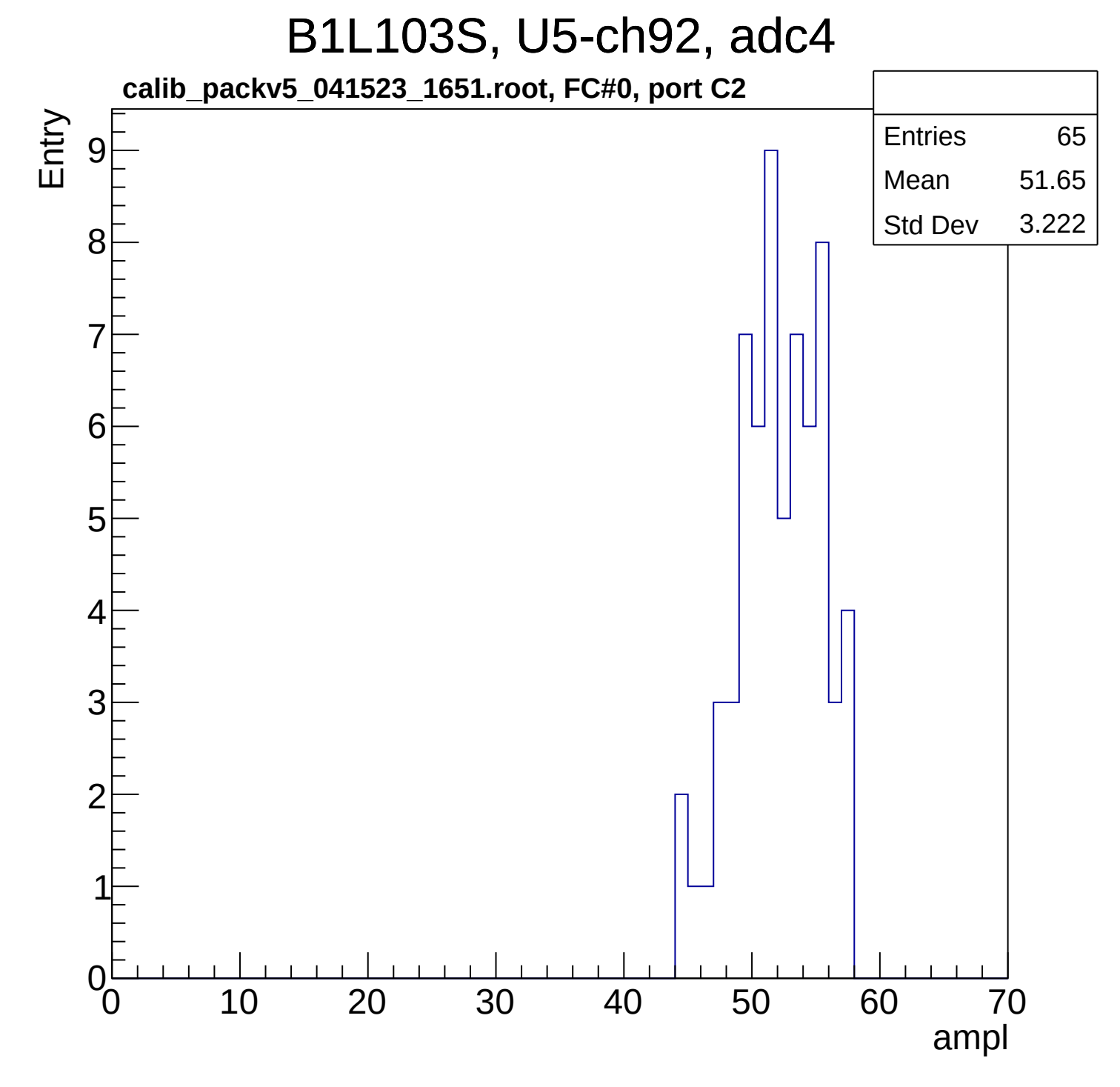
B1L103S, U5-ch92, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 51.65
Std Dev 3.222
Entry
ampl
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30
40
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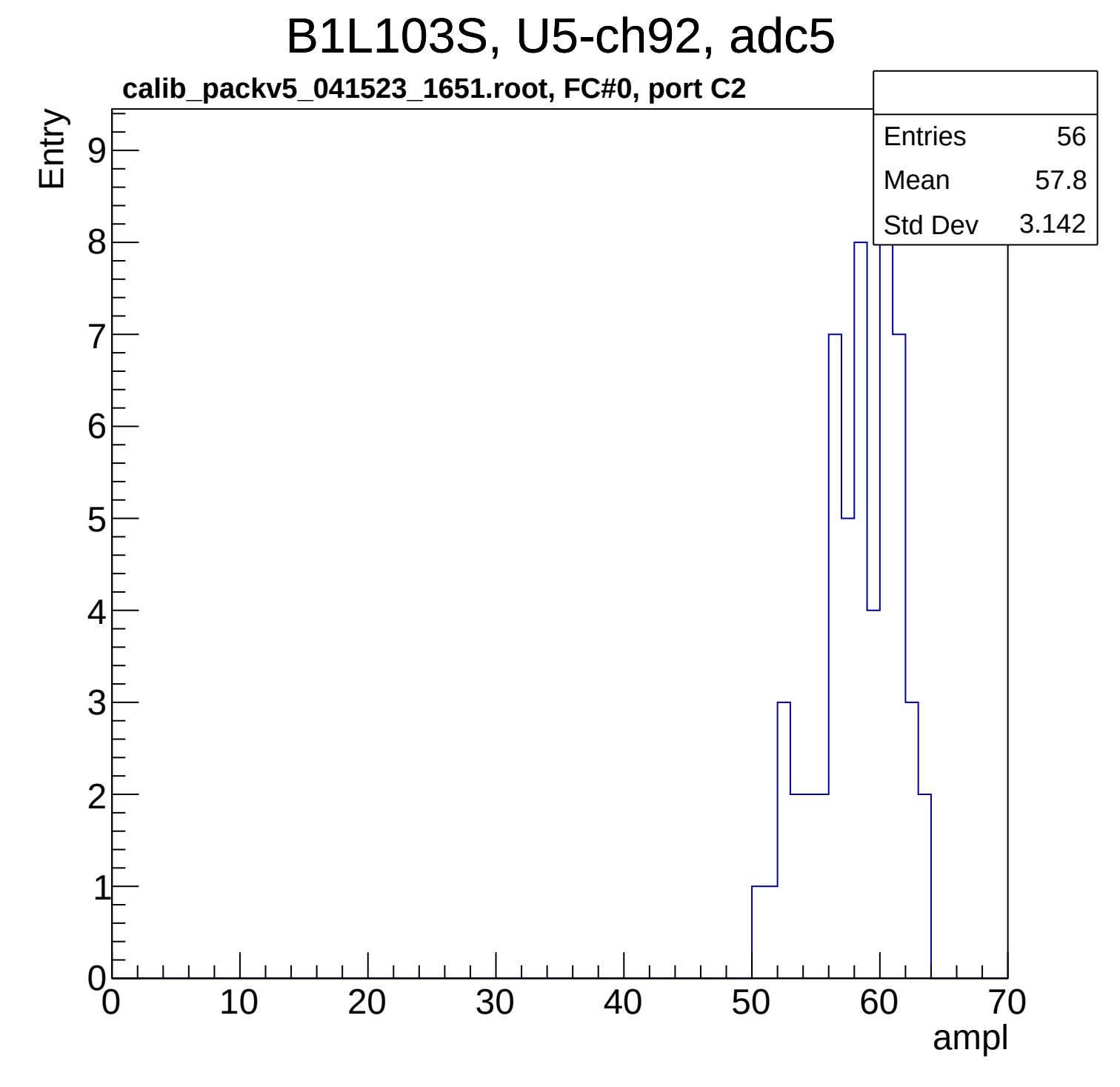
6
7
8
9


B1L103S, U5-ch92, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 57.8
Std Dev 3.142
Entry
ampl
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0
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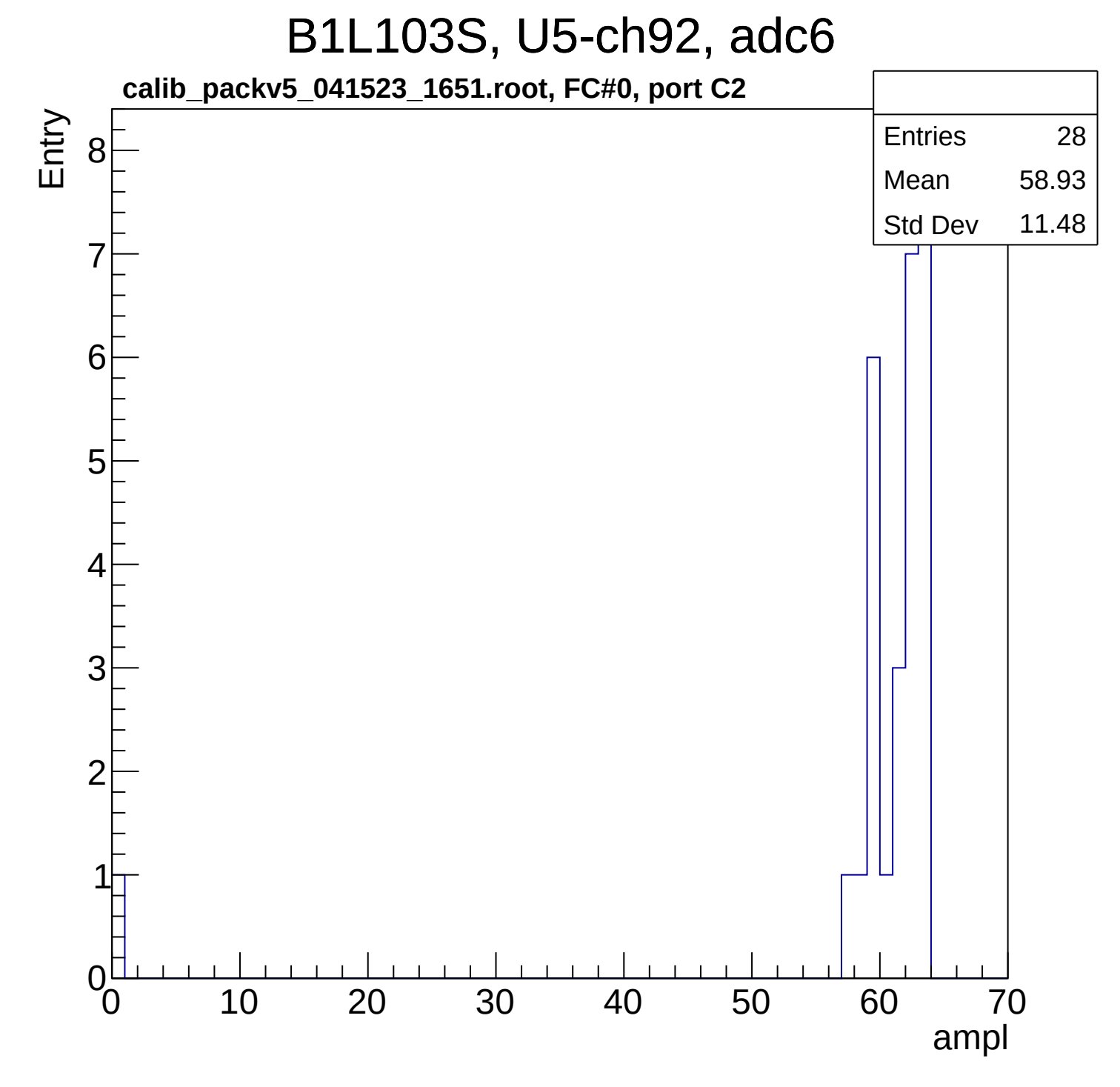
B1L103S, U5-ch92, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 58.93
Std Dev 11.48
Entry
ampl
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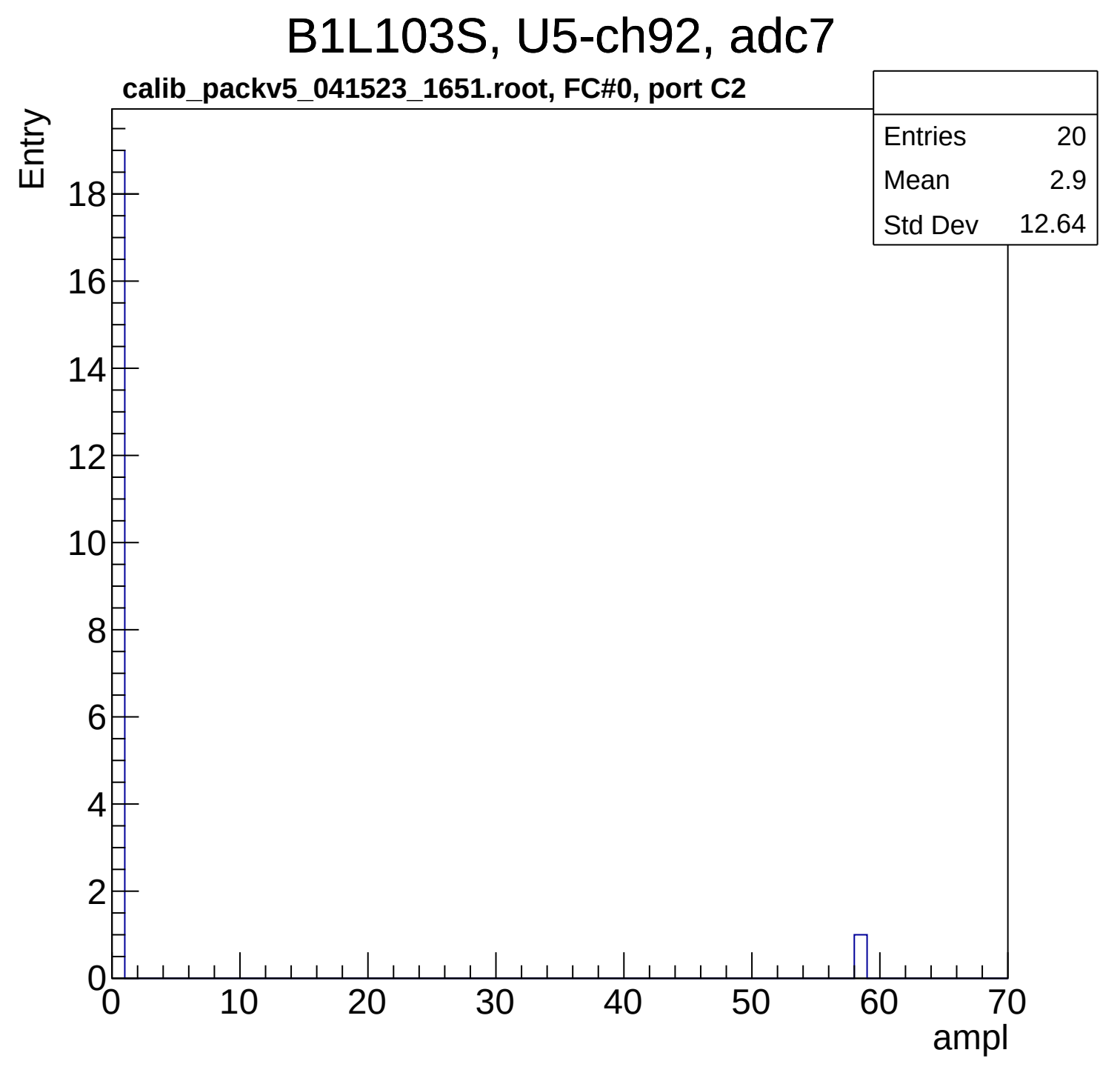
B1L103S, U5-ch92, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 2.9
Std Dev 12.64
Entry
0
2
4
6
8
10
12
14
16
18
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50
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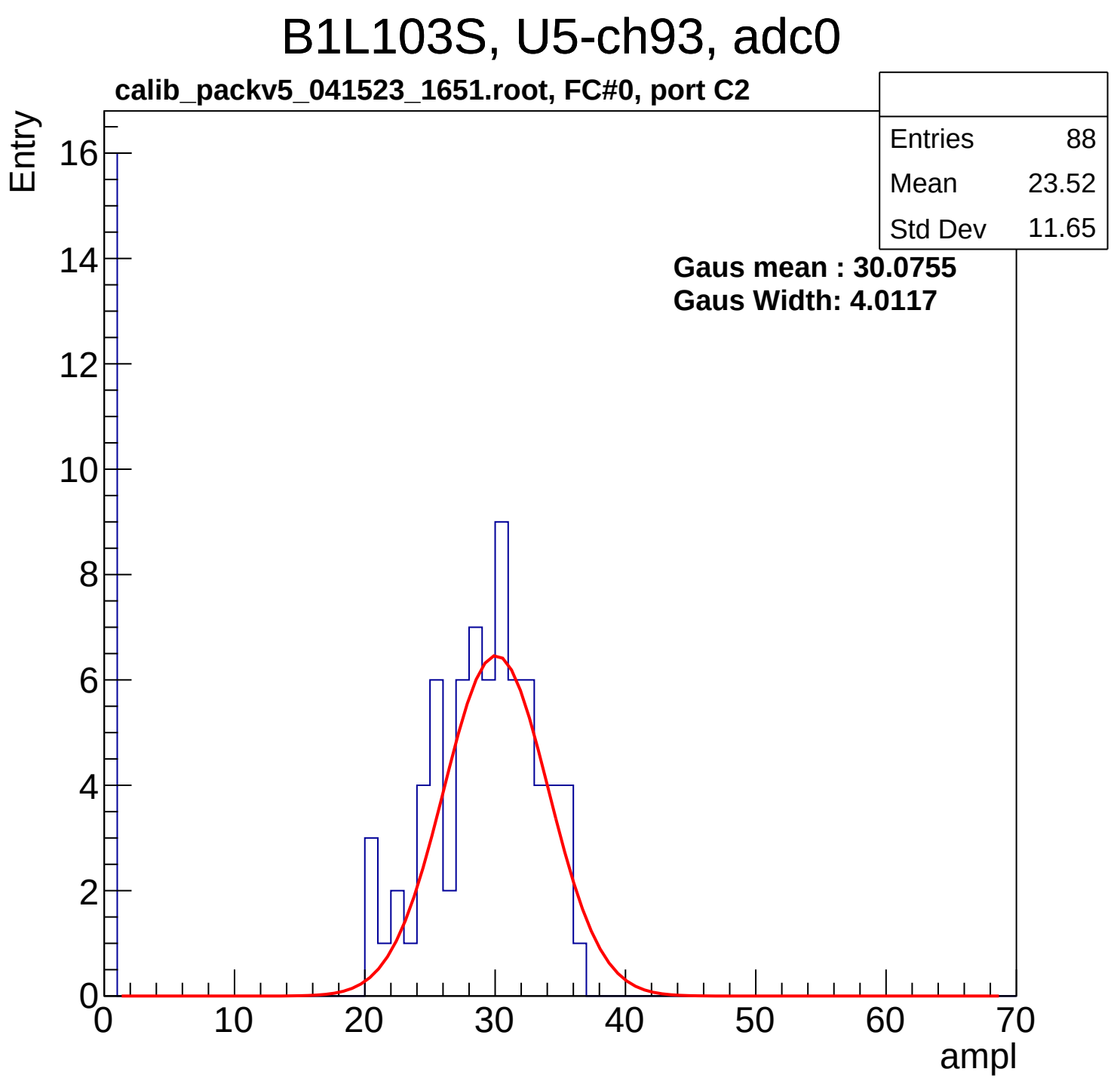
70
ampl


B1L103S, U5-ch93, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 23.52
Std Dev 11.65
Gaus mean : 30.0755
Gaus Width: 4.0117
Entry
ampl
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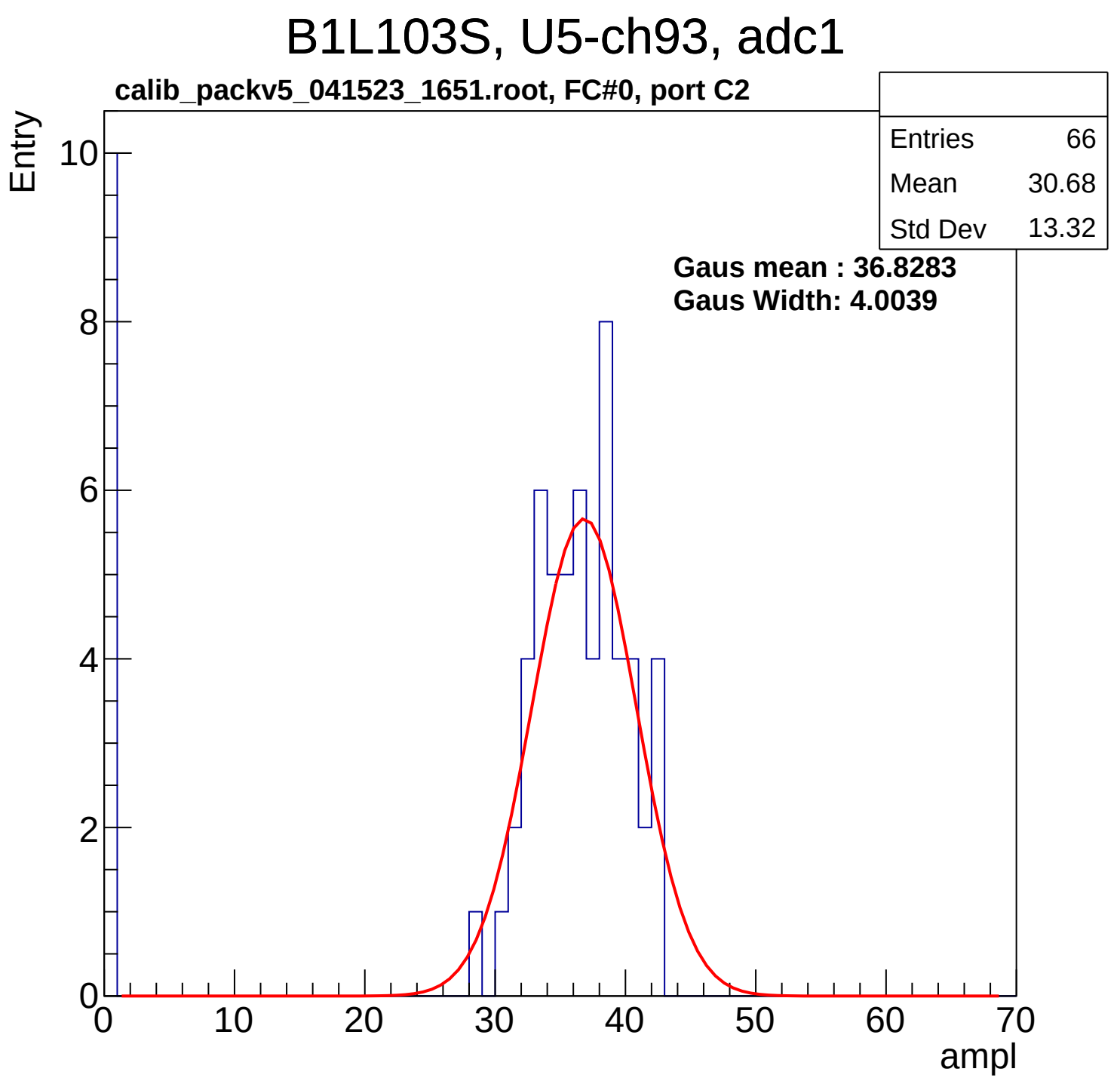
B1L103S, U5-ch93, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 30.68
Std Dev 13.32
Gaus mean : 36.8283
Gaus Width: 4.0039
Entry
ampl
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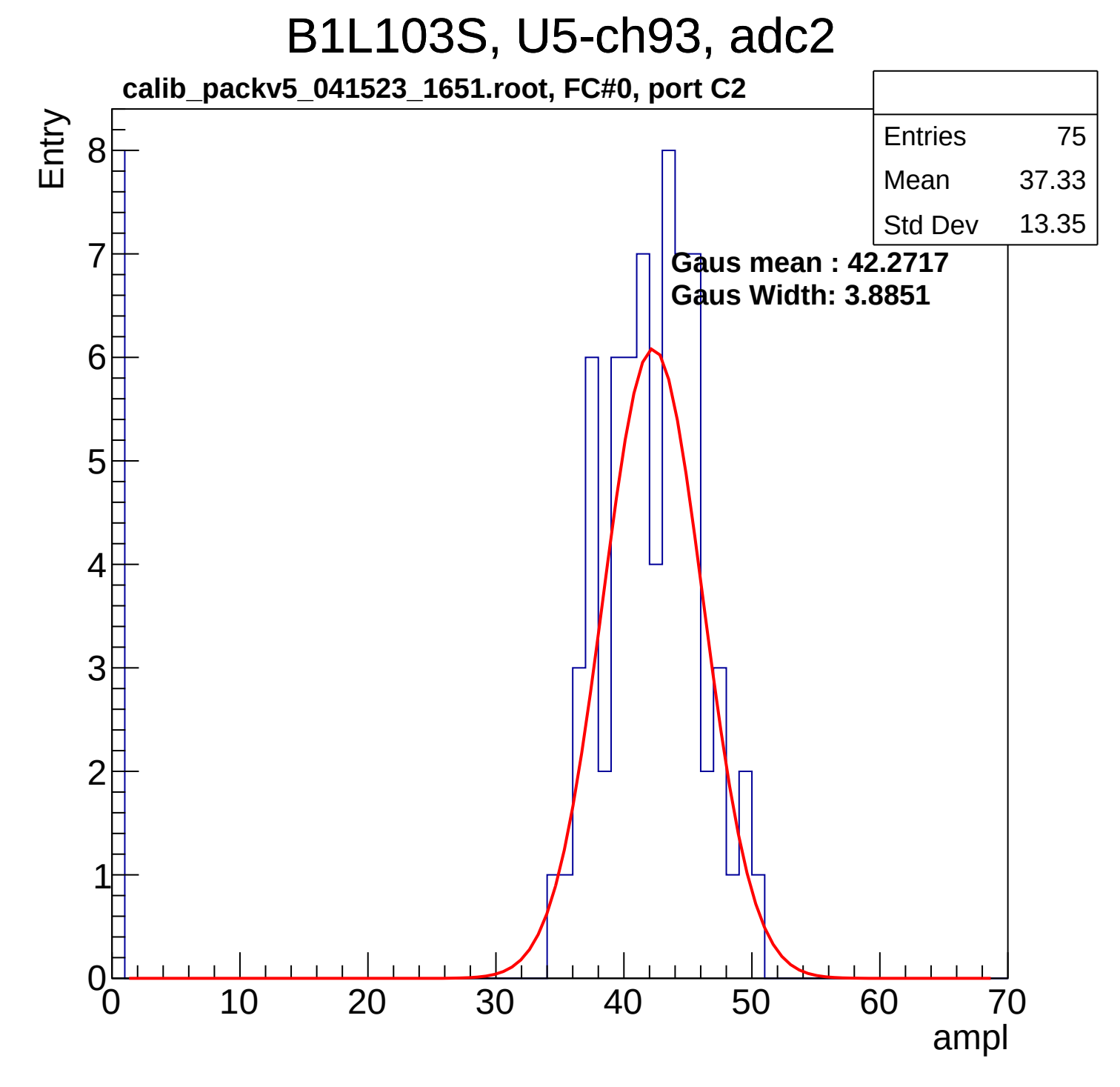
B1L103S, U5-ch93, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 37.33
Std Dev 13.35
Gaus mean : 42.2717
Gaus Width: 3.8851
Entry
ampl
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3
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0
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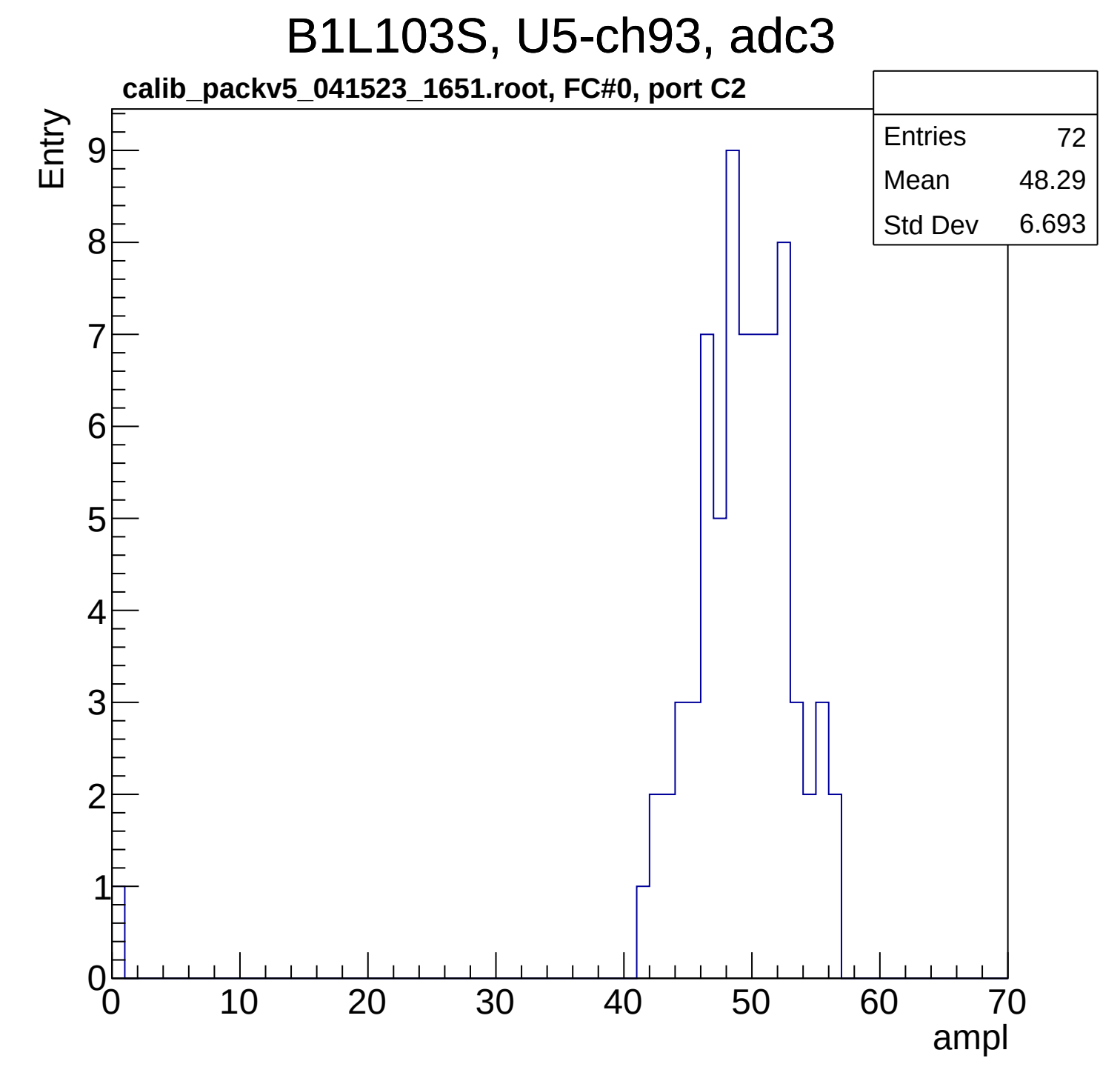
B1L103S, U5-ch93, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 48.29
Std Dev 6.693
Entry
ampl
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3
4
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6
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8
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0
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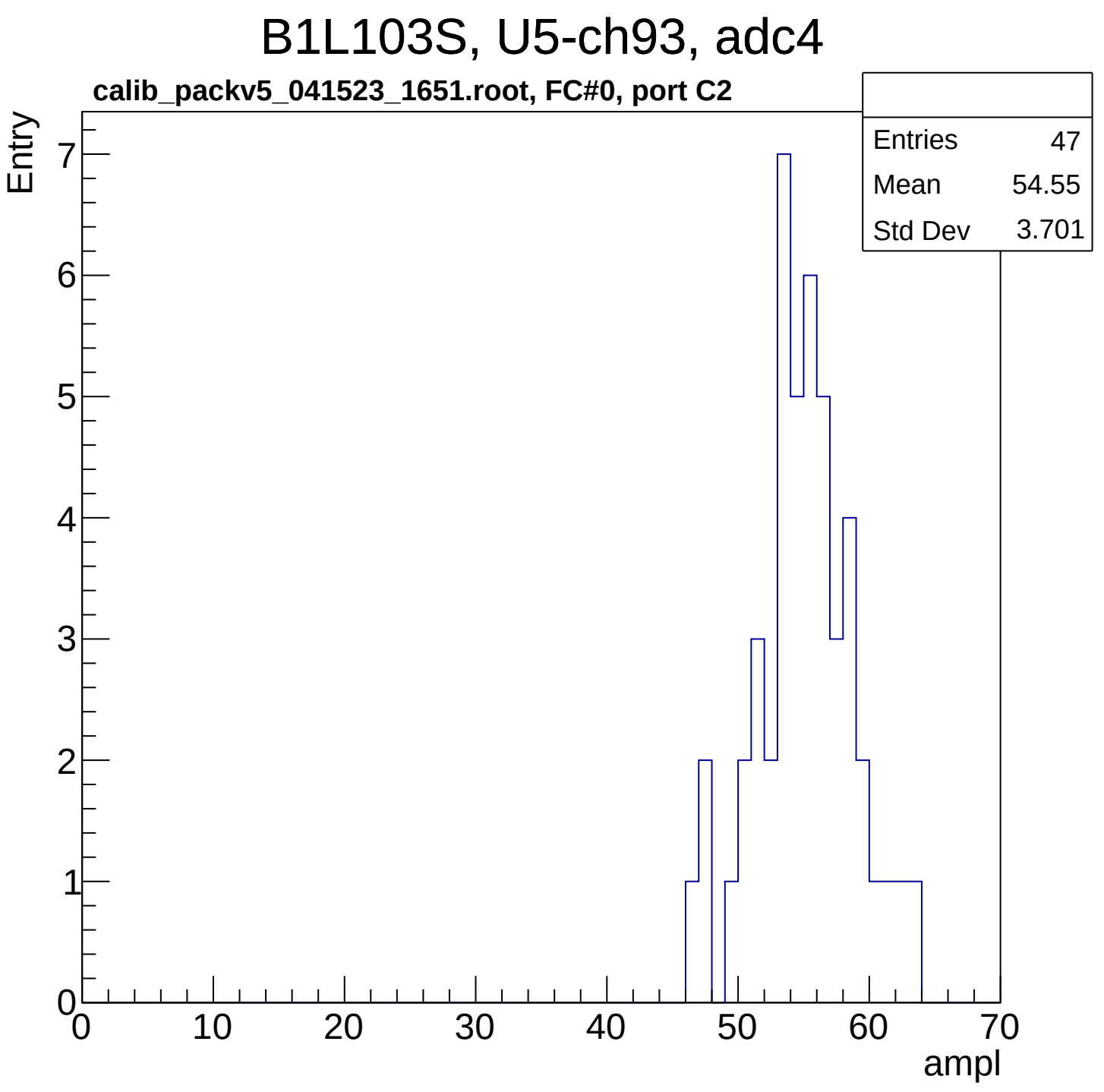
B1L103S, U5-ch93, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 54.55
Std Dev 3.701
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
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60
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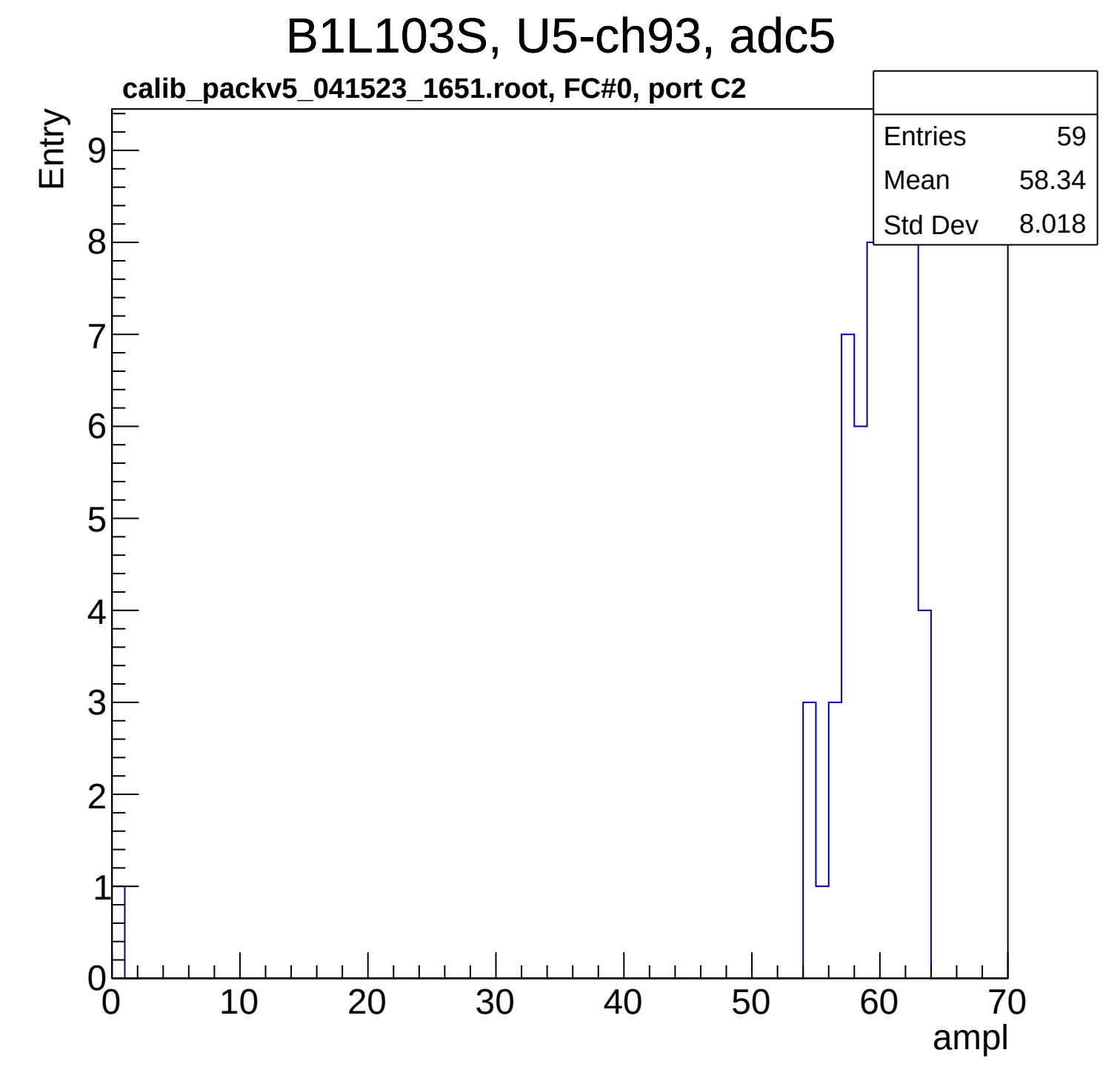
B1L103S, U5-ch93, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 58.34
Std Dev 8.018
Entry
ampl
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3
4
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0
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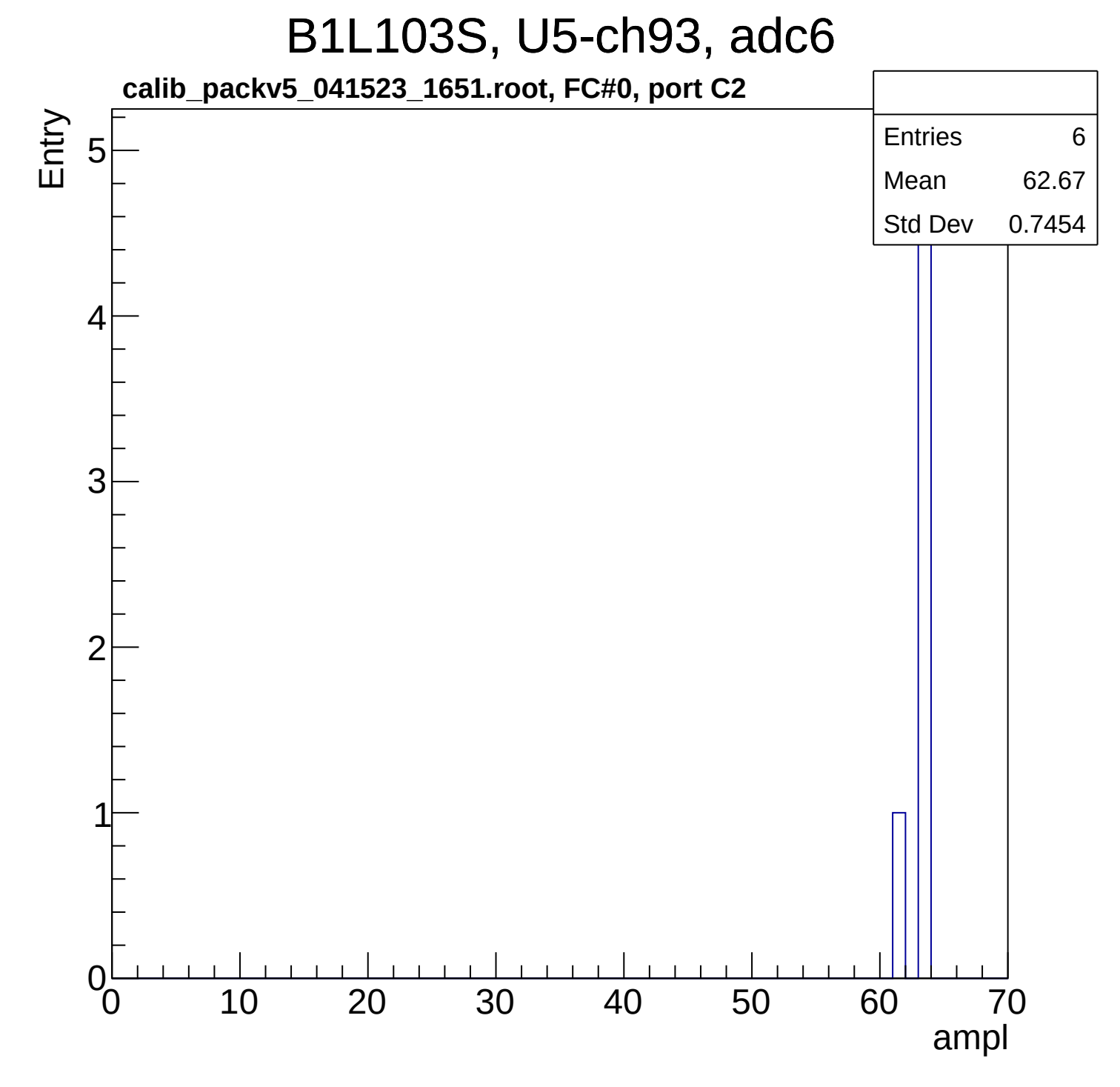
B1L103S, U5-ch93, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.67
Std Dev 0.7454
Entry
ampl
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1
2
3
4
5
0
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40
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60
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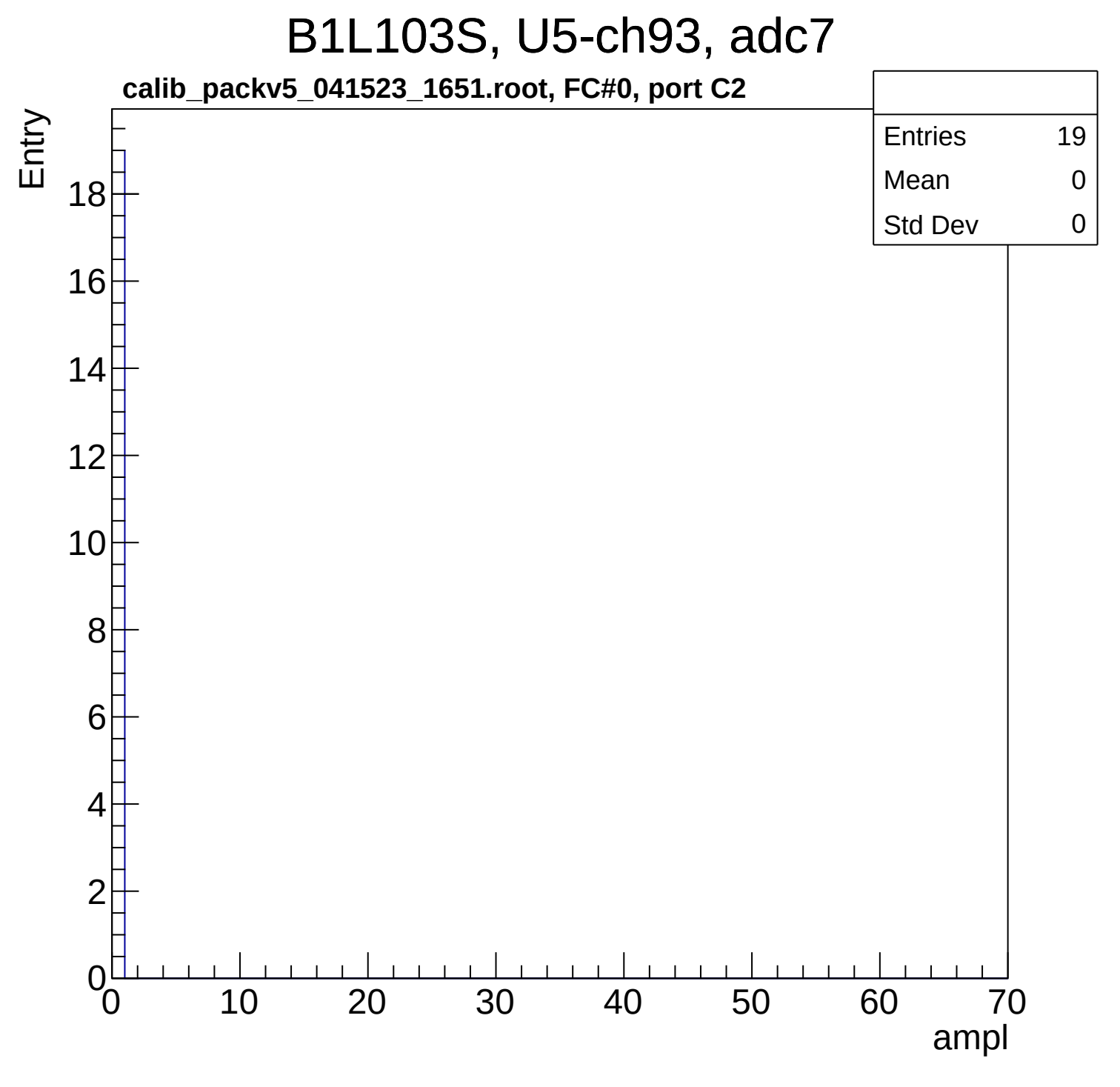
B1L103S, U5-ch93, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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10
12
14
16
18
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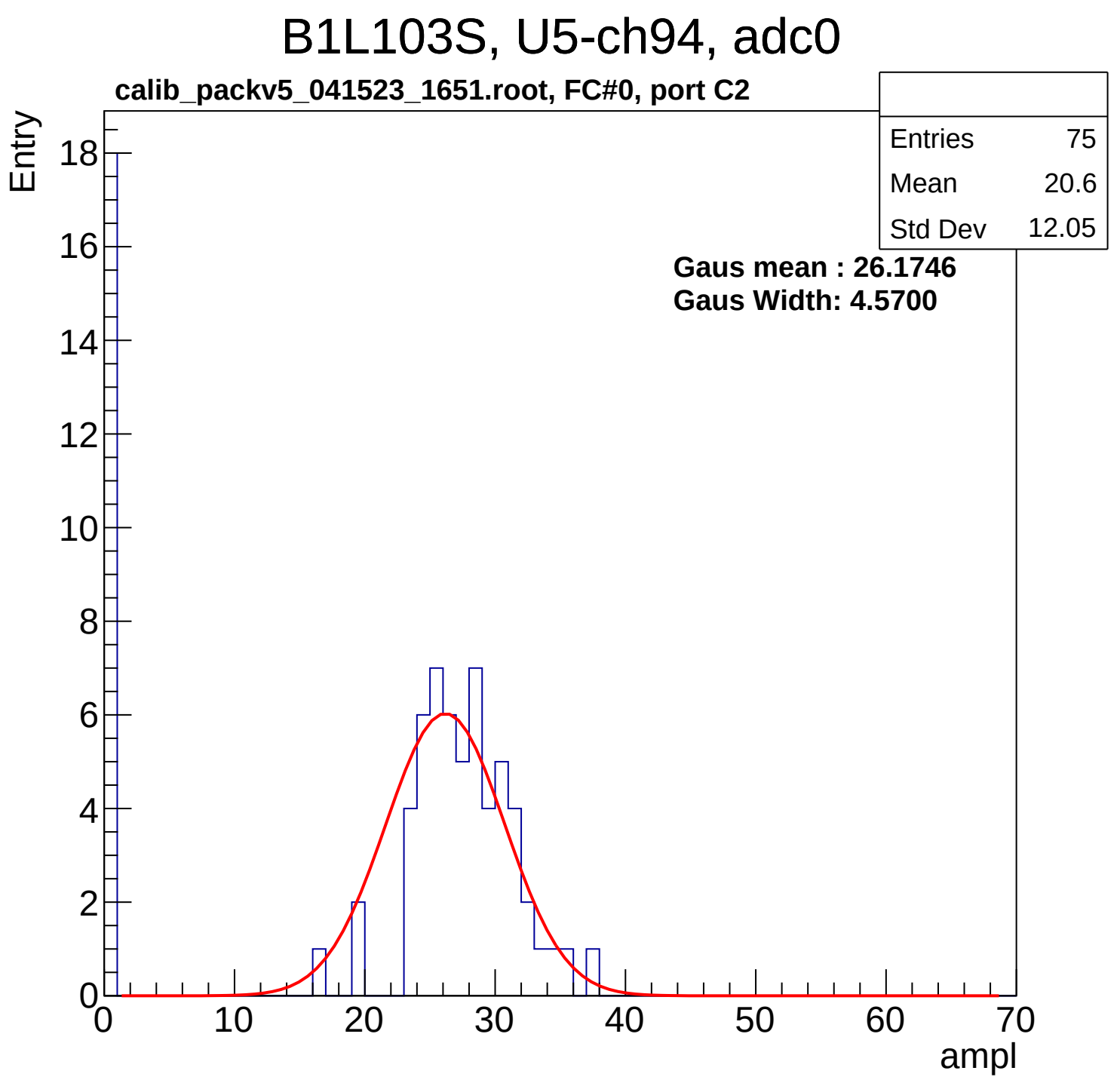
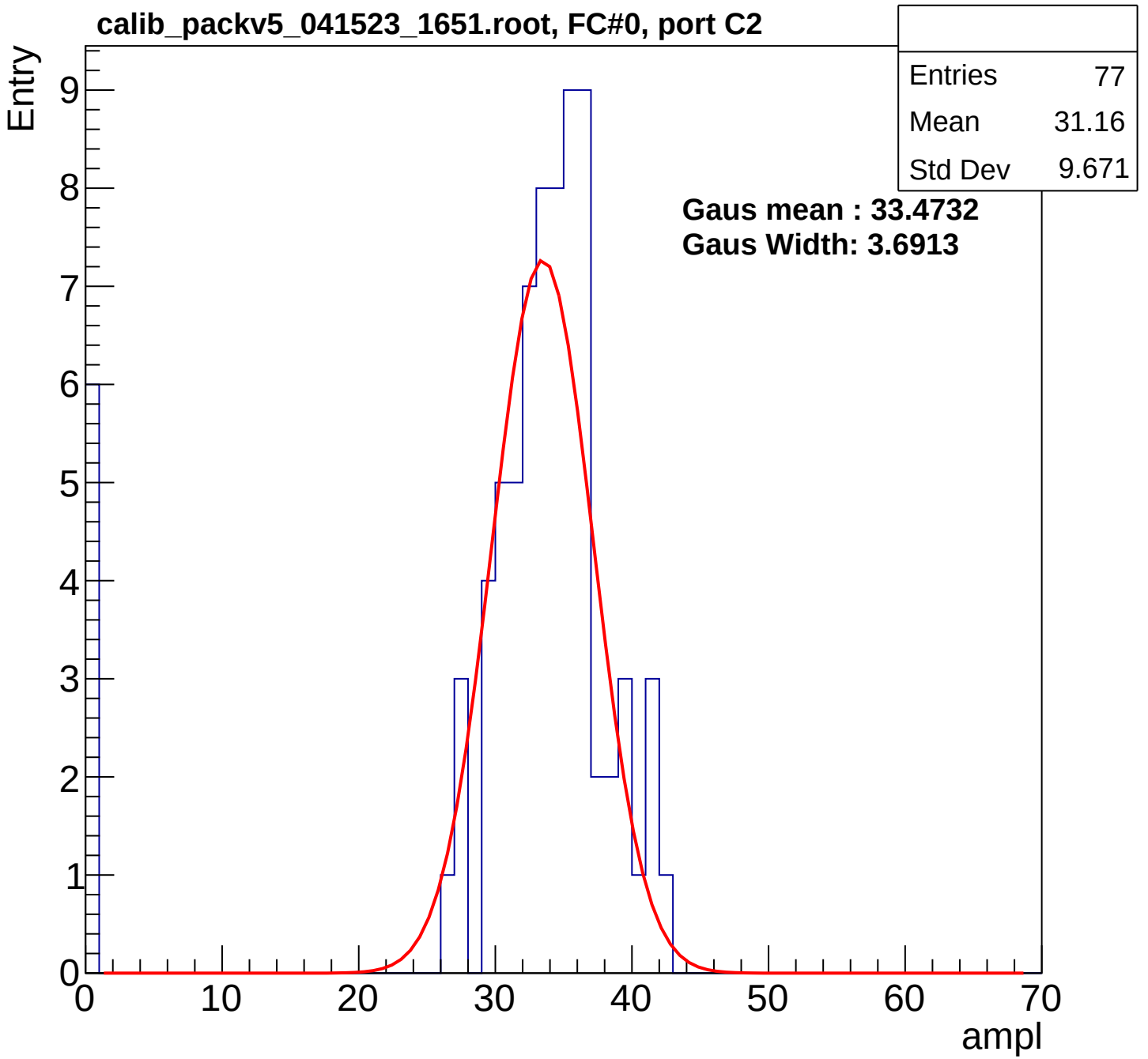
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch94, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 20.6
Std Dev 12.05
Gaus mean : 26.1746
Gaus Width: 4.5700
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L103S, U5-ch94, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 31.16
Std Dev 9.671
Gaus mean : 33.4732
Gaus Width: 3.6913
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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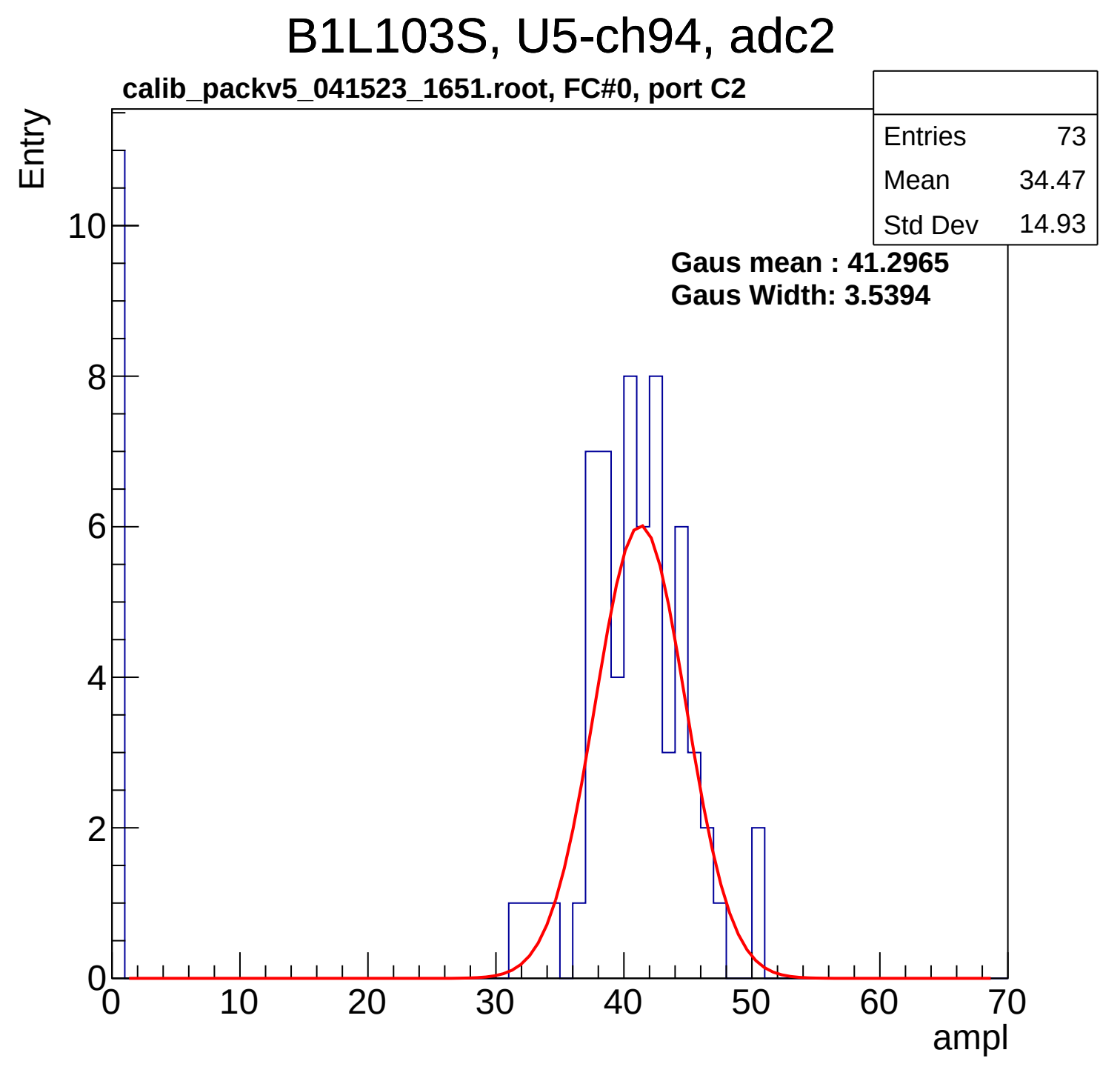
B1L103S, U5-ch94, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 34.47
Std Dev 14.93
Gaus mean : 41.2965
Gaus Width: 3.5394
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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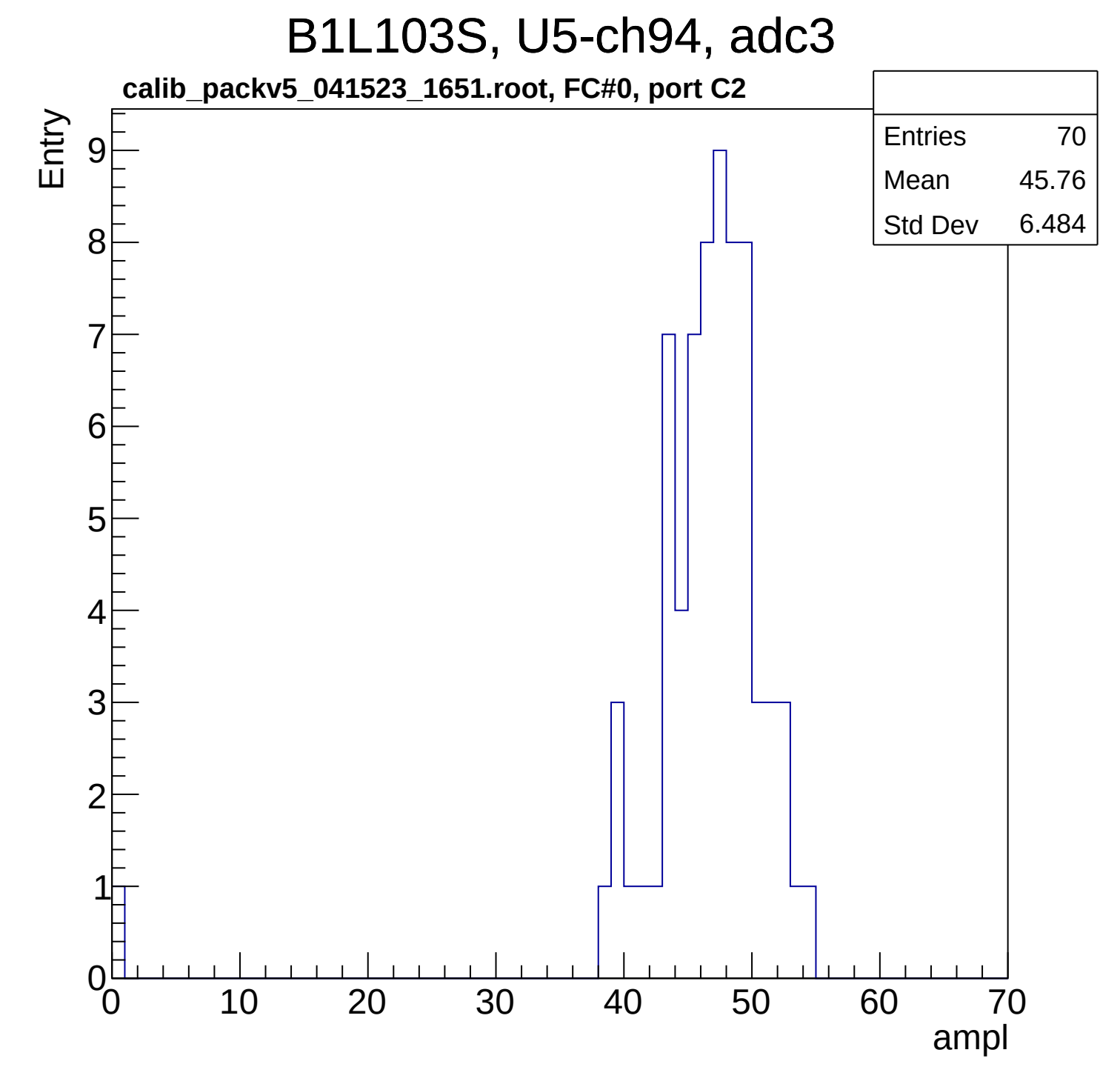
B1L103S, U5-ch94, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 45.76
Std Dev 6.484
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
50
60
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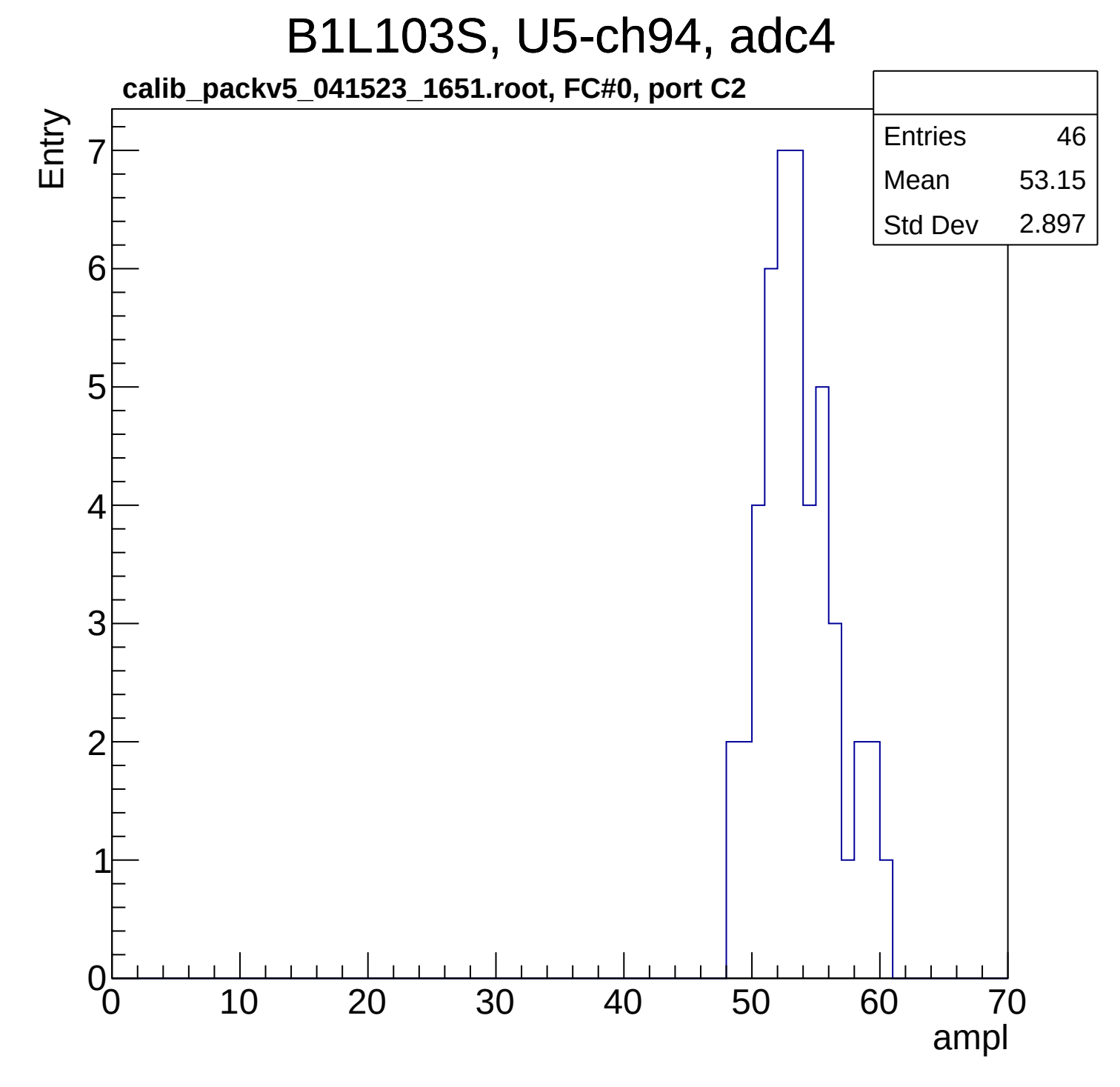
B1L103S, U5-ch94, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 53.15
Std Dev 2.897
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
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60
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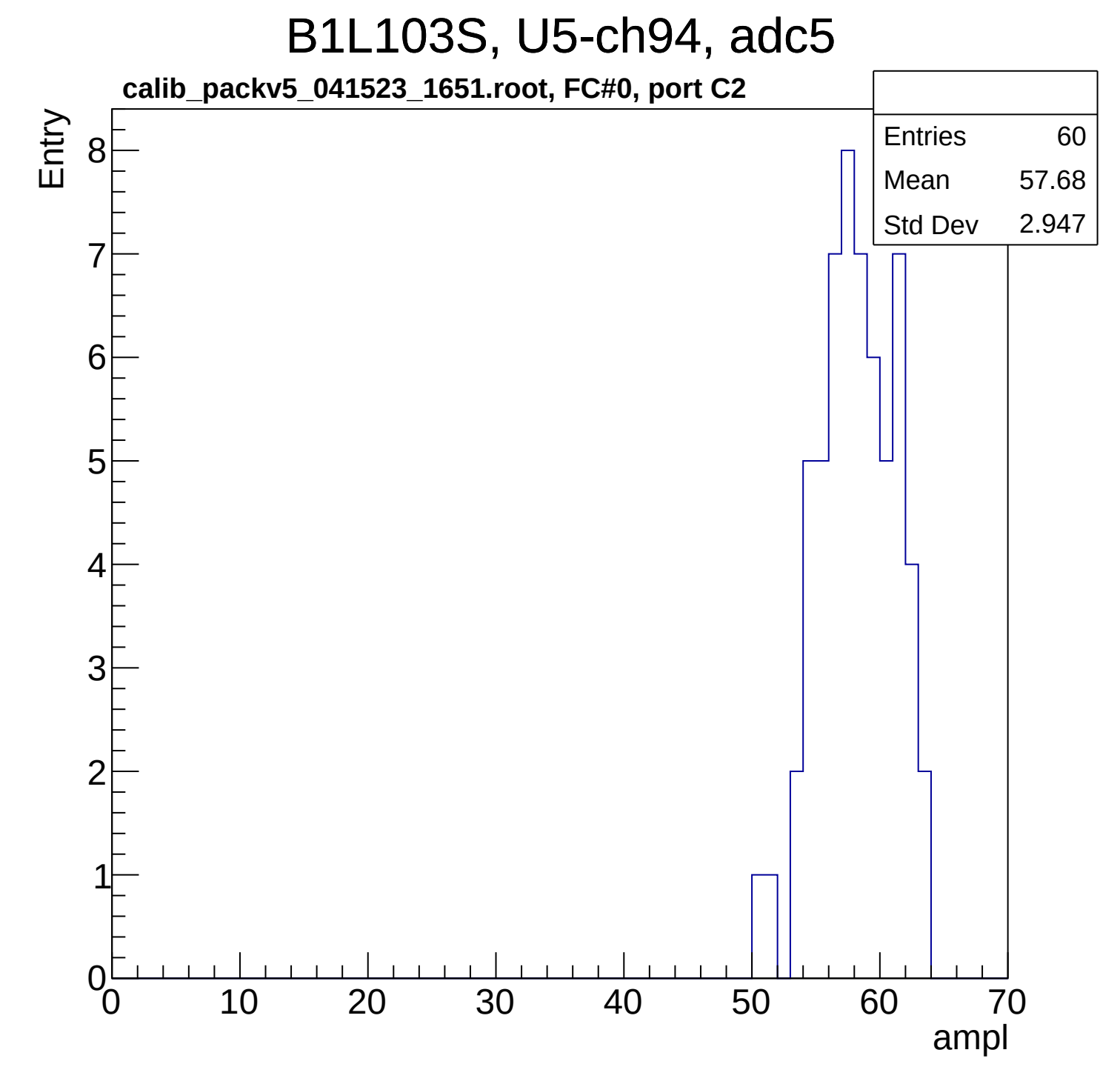
B1L103S, U5-ch94, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 57.68
Std Dev 2.947
Entry
ampl
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1
2
3
4
5
6
7
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0
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40
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60
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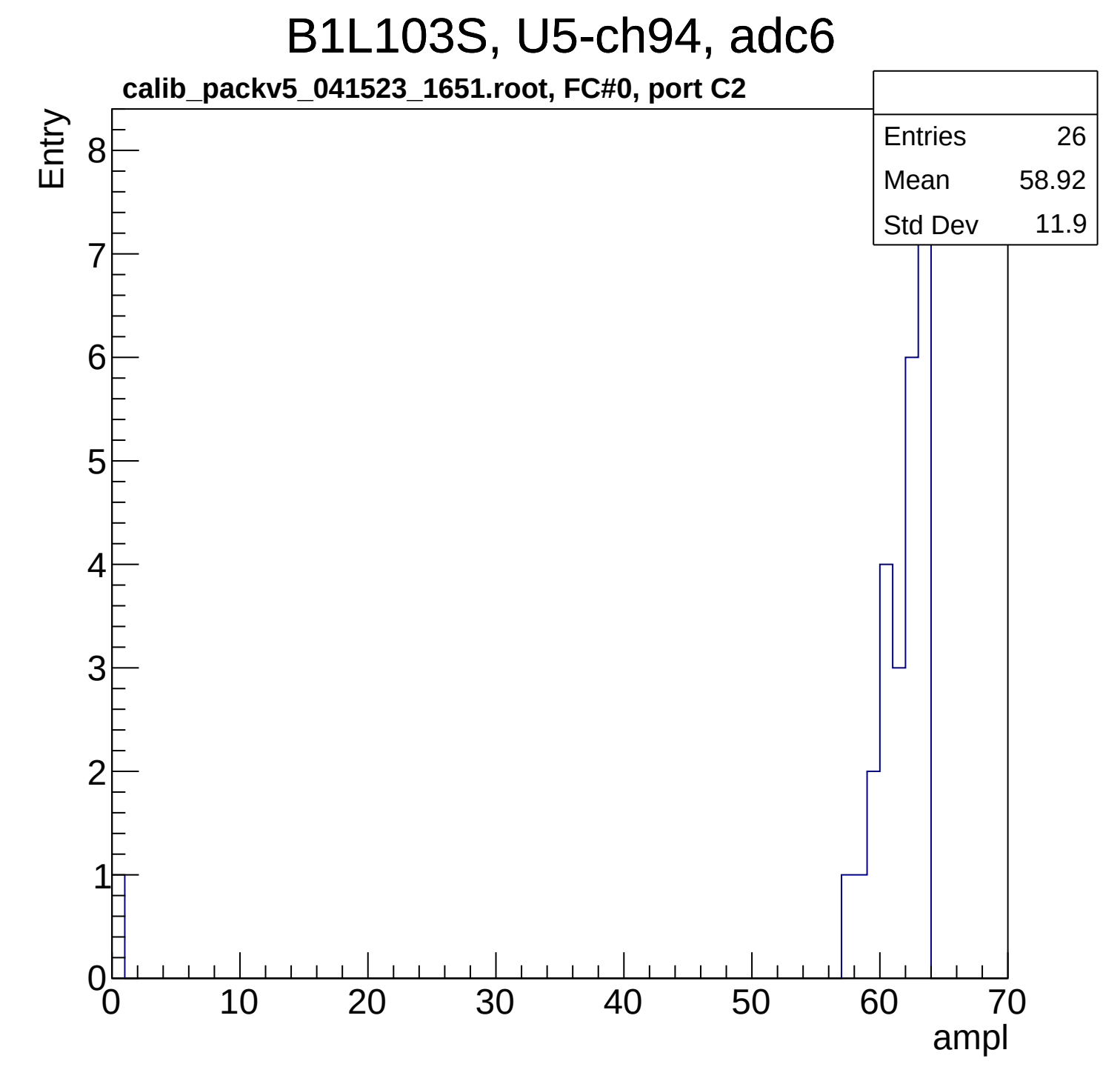
B1L103S, U5-ch94, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 58.92
Std Dev 11.9
Entry
ampl
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3
4
5
6
7
8
0
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20
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40
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60
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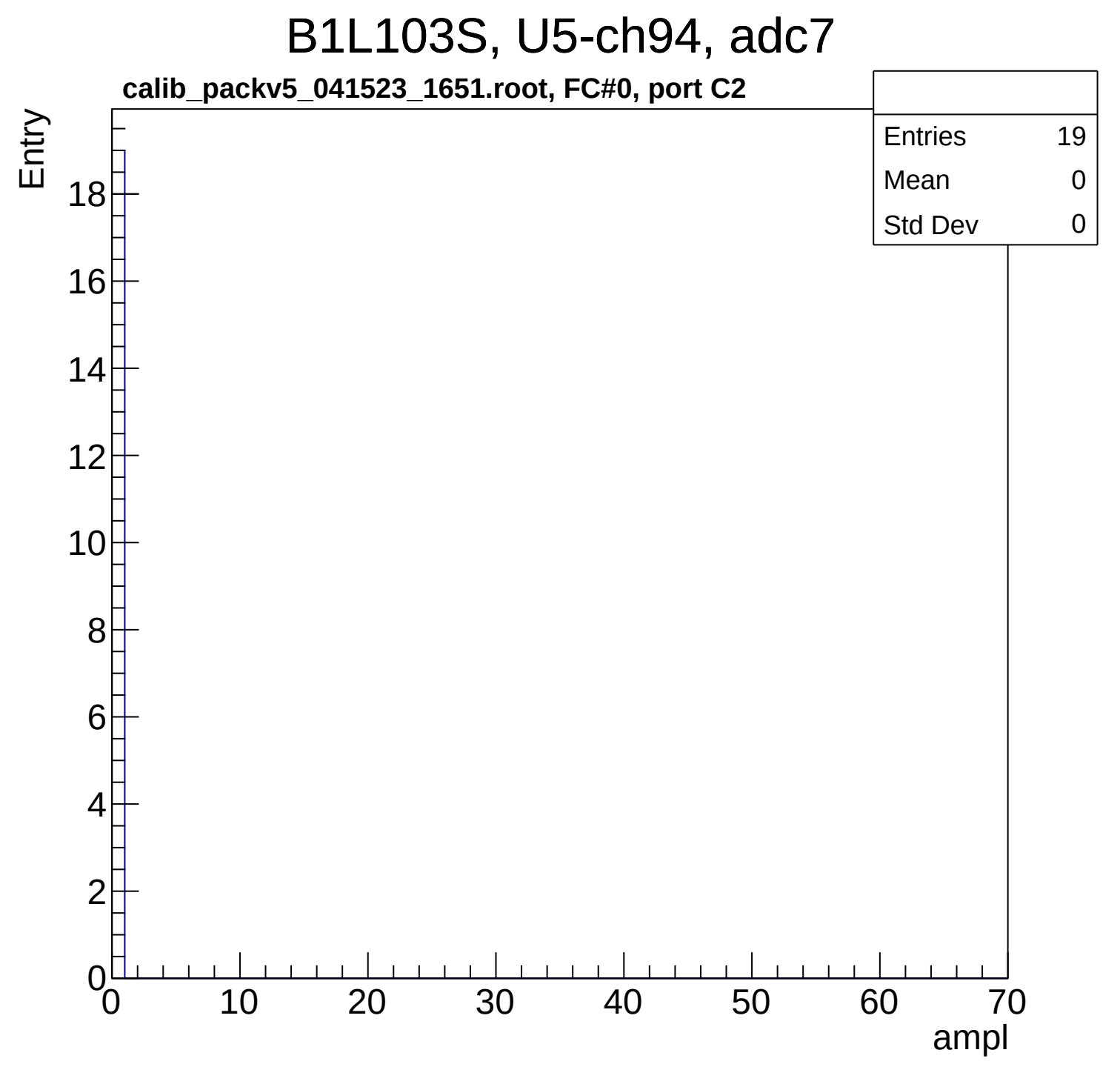
B1L103S, U5-ch94, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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10
20
30
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50
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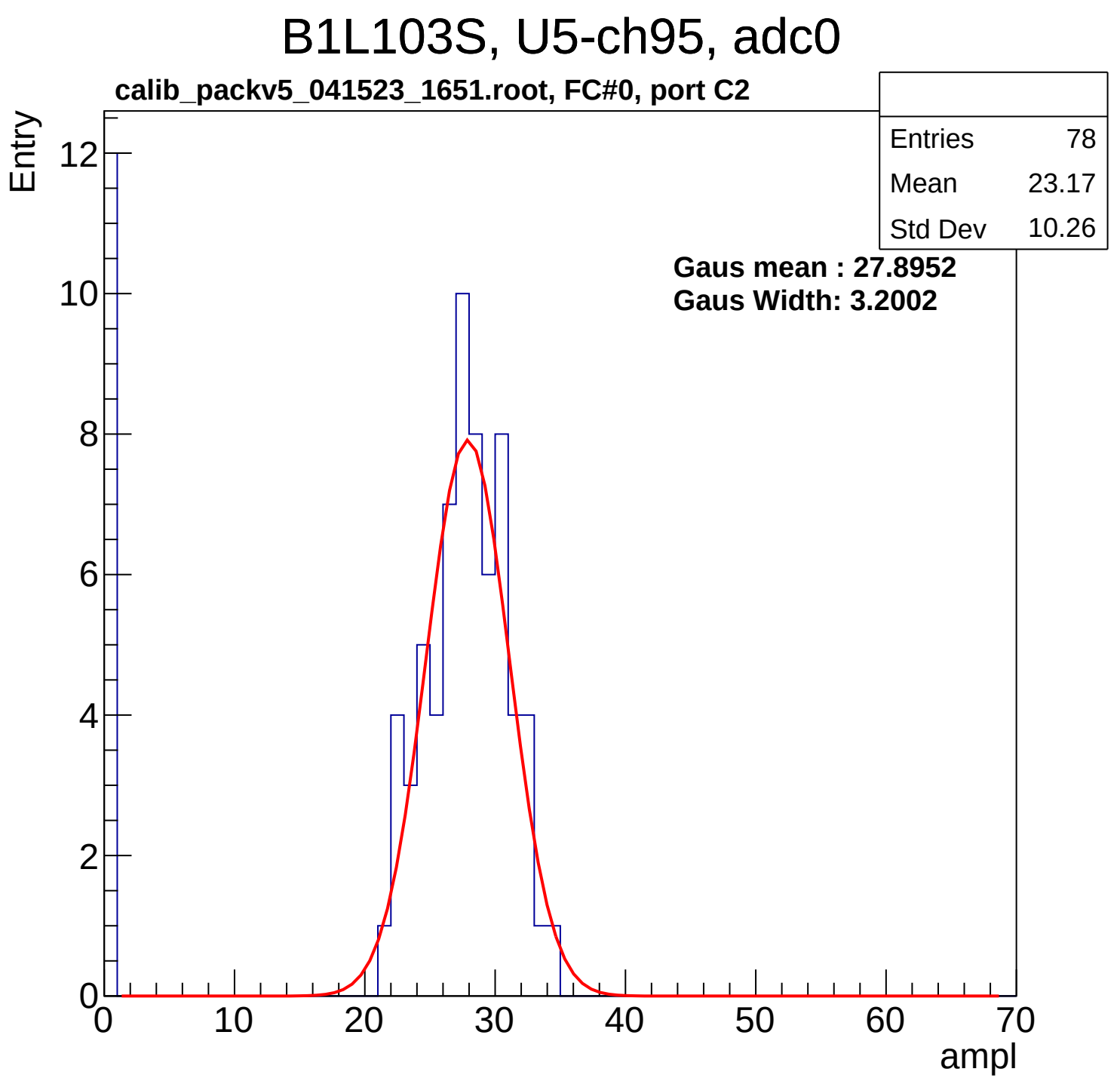
70
ampl


B1L103S, U5-ch95, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 23.17
Std Dev 10.26
Gaus mean : 27.8952
Gaus Width: 3.2002
Entry
ampl
0
2
4
6
8
10
12
0
10
20
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40
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60
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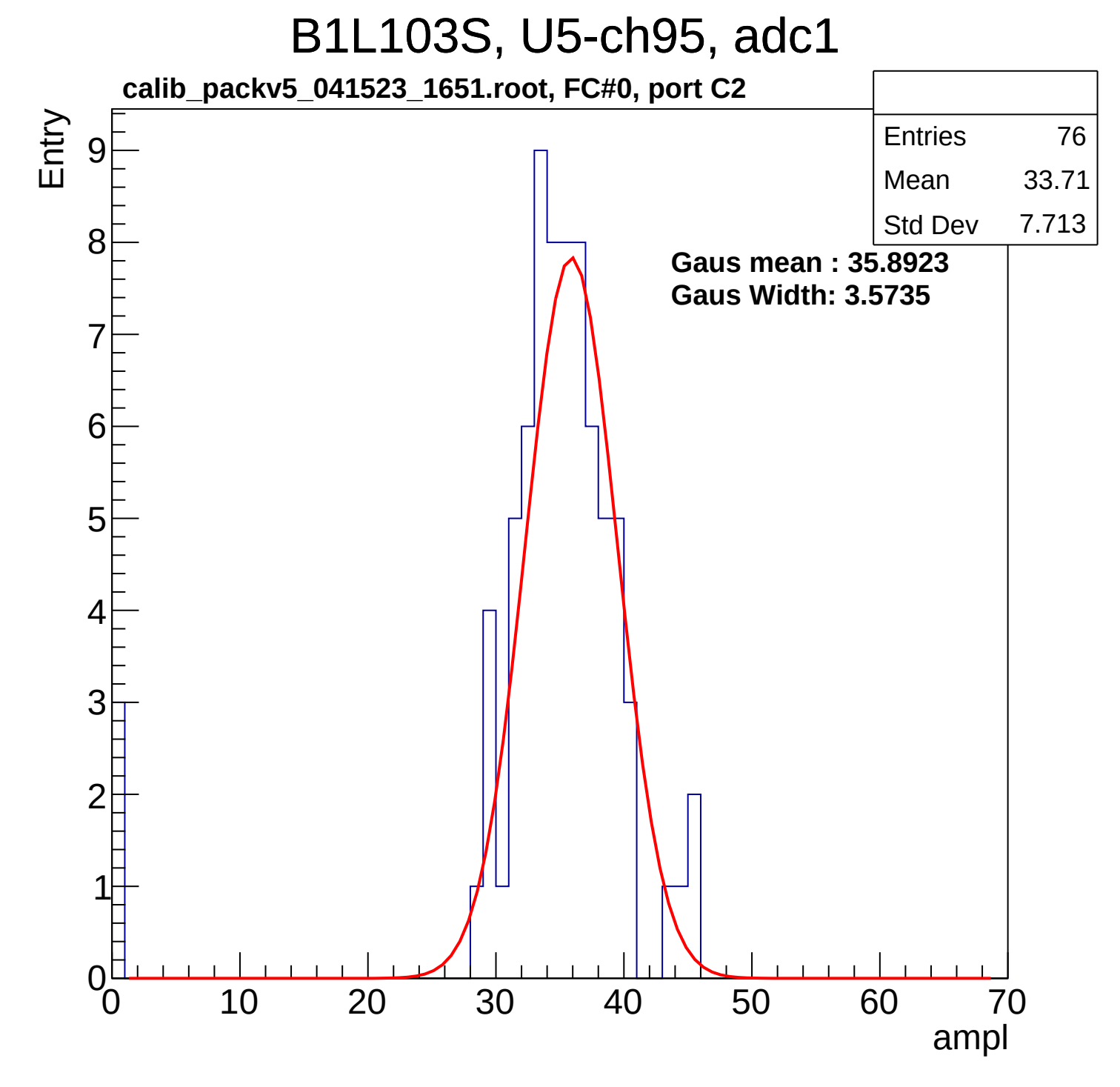
B1L103S, U5-ch95, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 33.71
Std Dev 7.713
Gaus mean : 35.8923
Gaus Width: 3.5735
Entry
ampl
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20
30
40
50
60
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1
2
3
4
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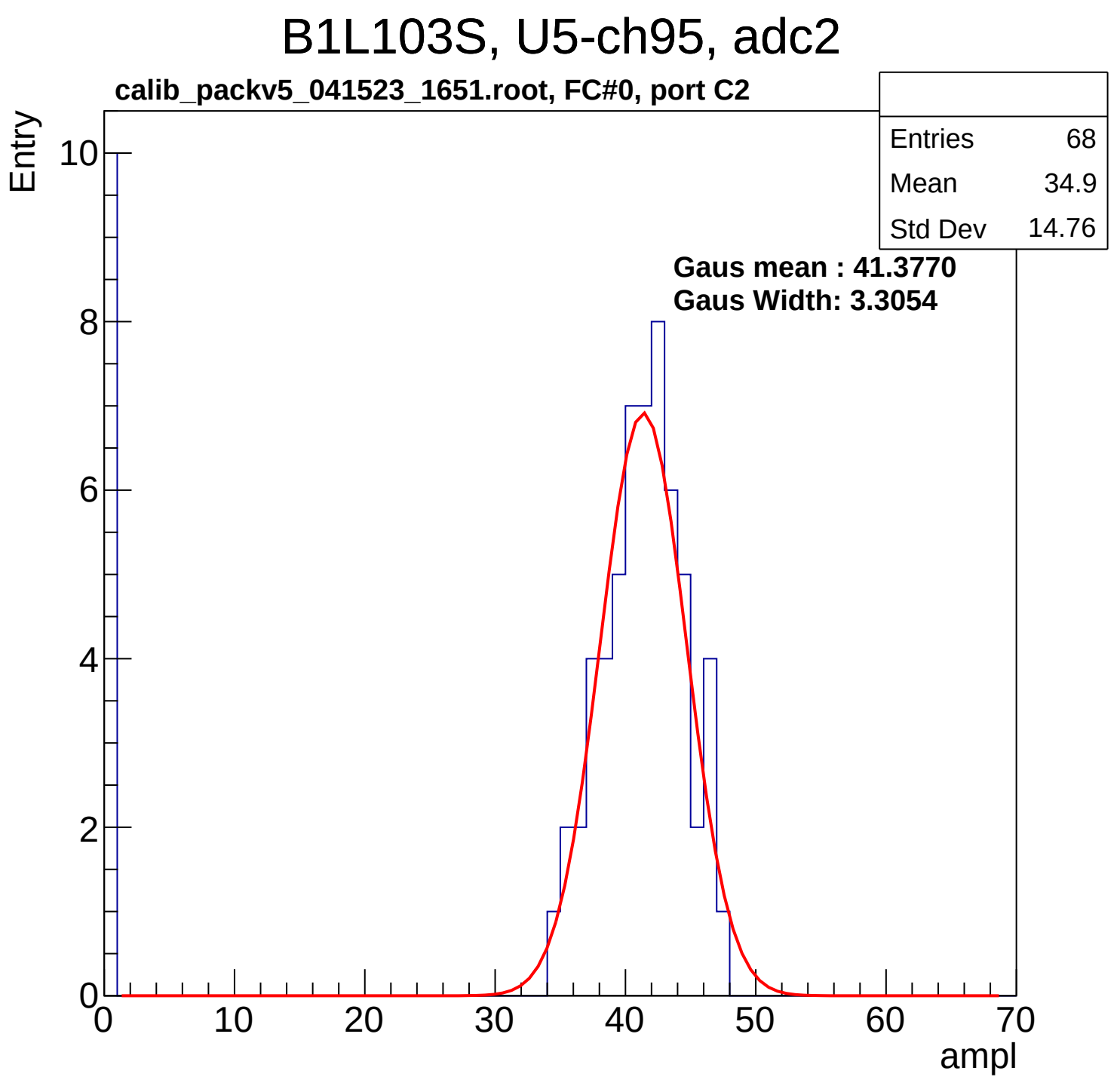
6
7
8
9


B1L103S, U5-ch95, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 34.9
Std Dev 14.76
Gaus mean : 41.3770
Gaus Width: 3.3054
Entry
ampl
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2
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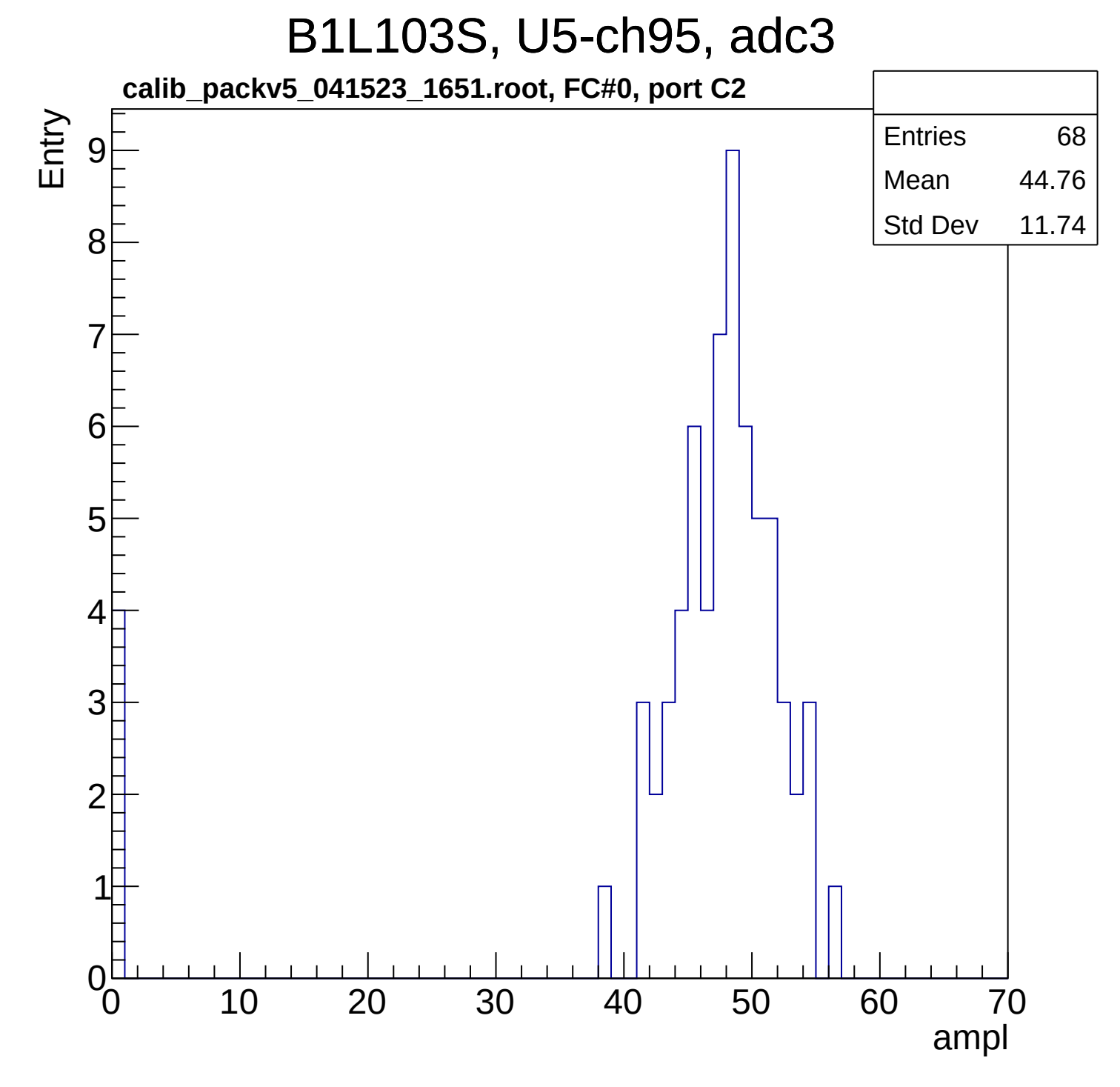
B1L103S, U5-ch95, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 44.76
Std Dev 11.74
Entry
ampl
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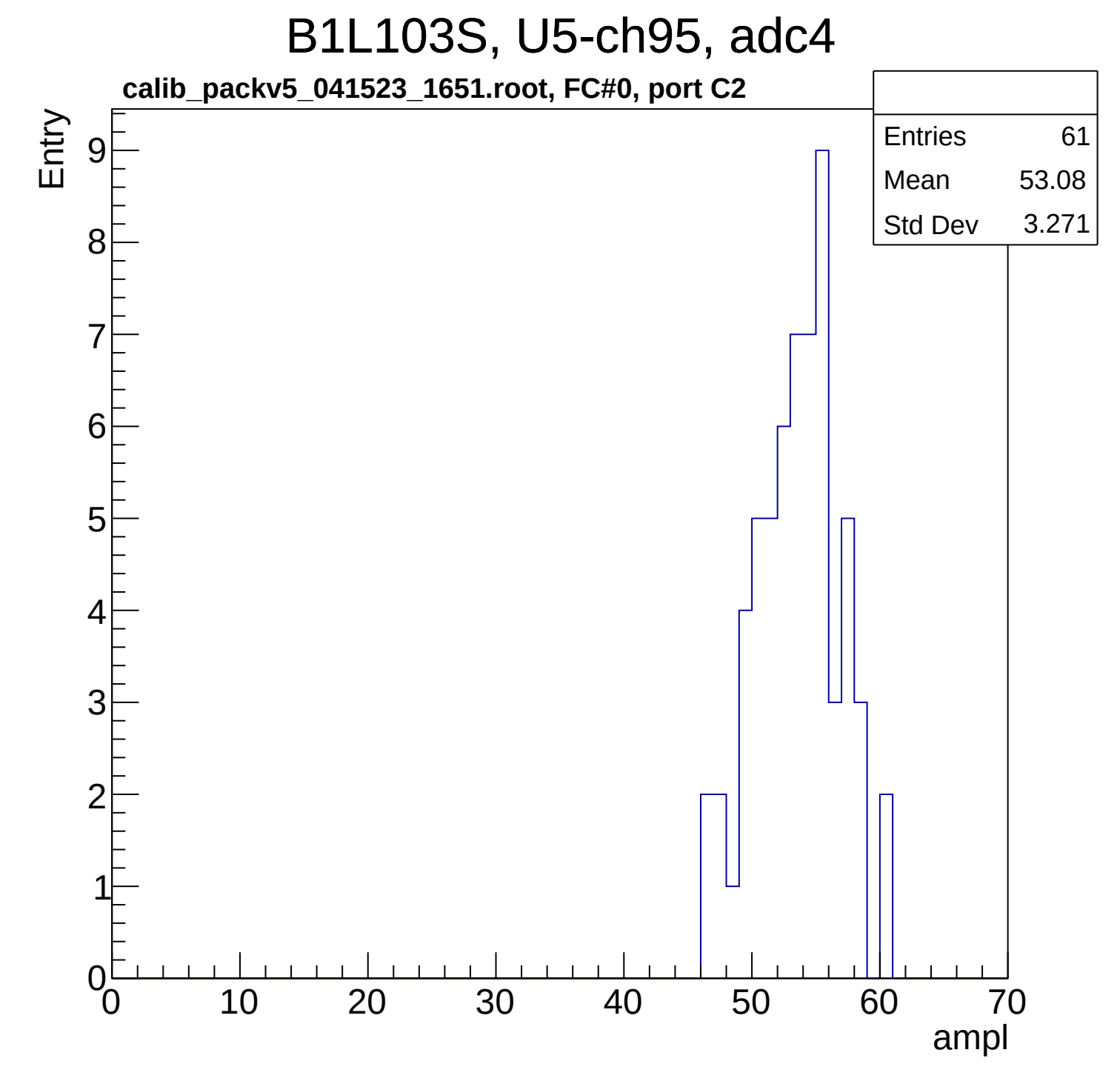
B1L103S, U5-ch95, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 53.08
Std Dev 3.271
Entry
ampl
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0
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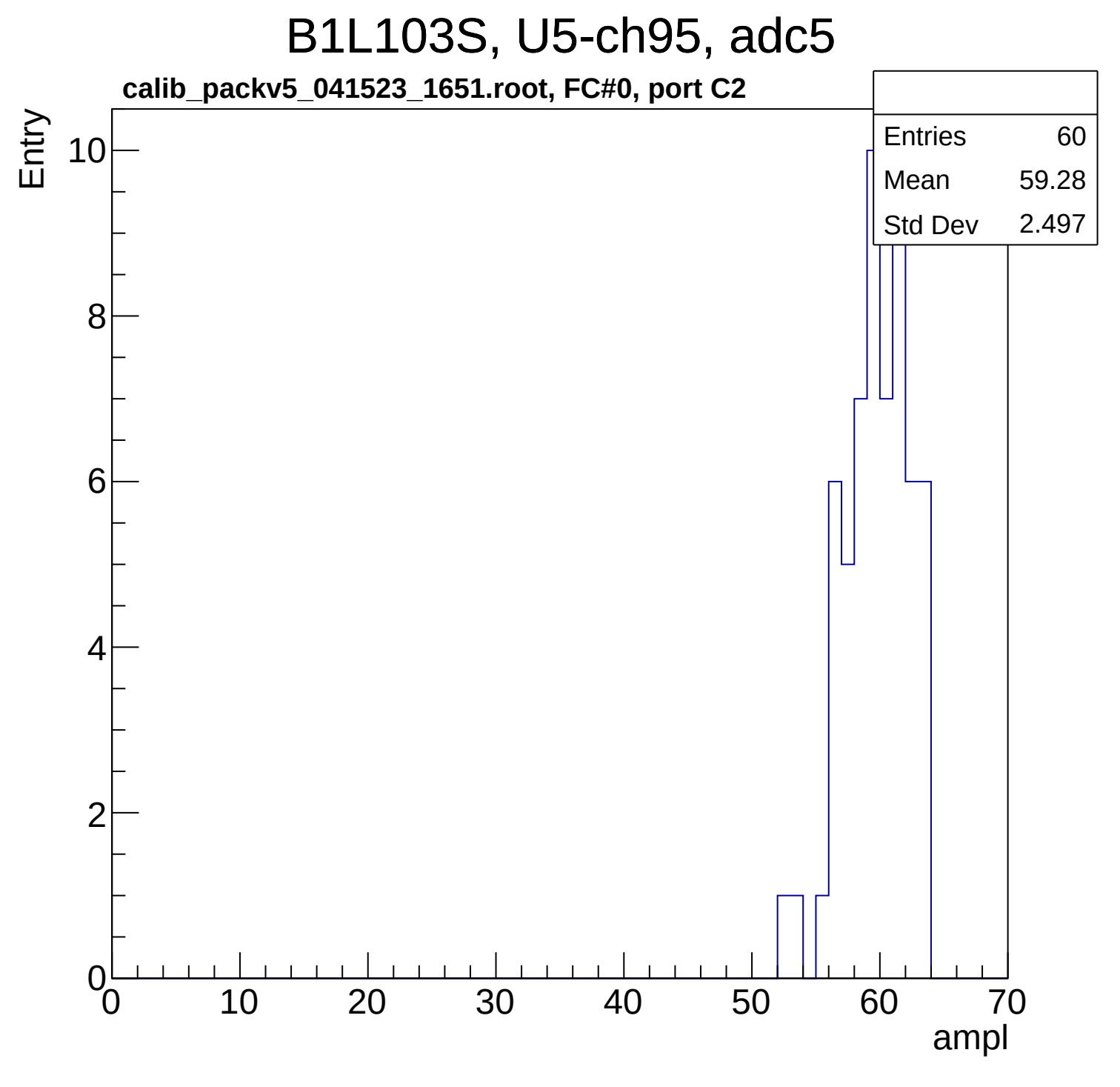
B1L103S, U5-ch95, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 59.28
Std Dev 2.497
Entry
ampl
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0
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60
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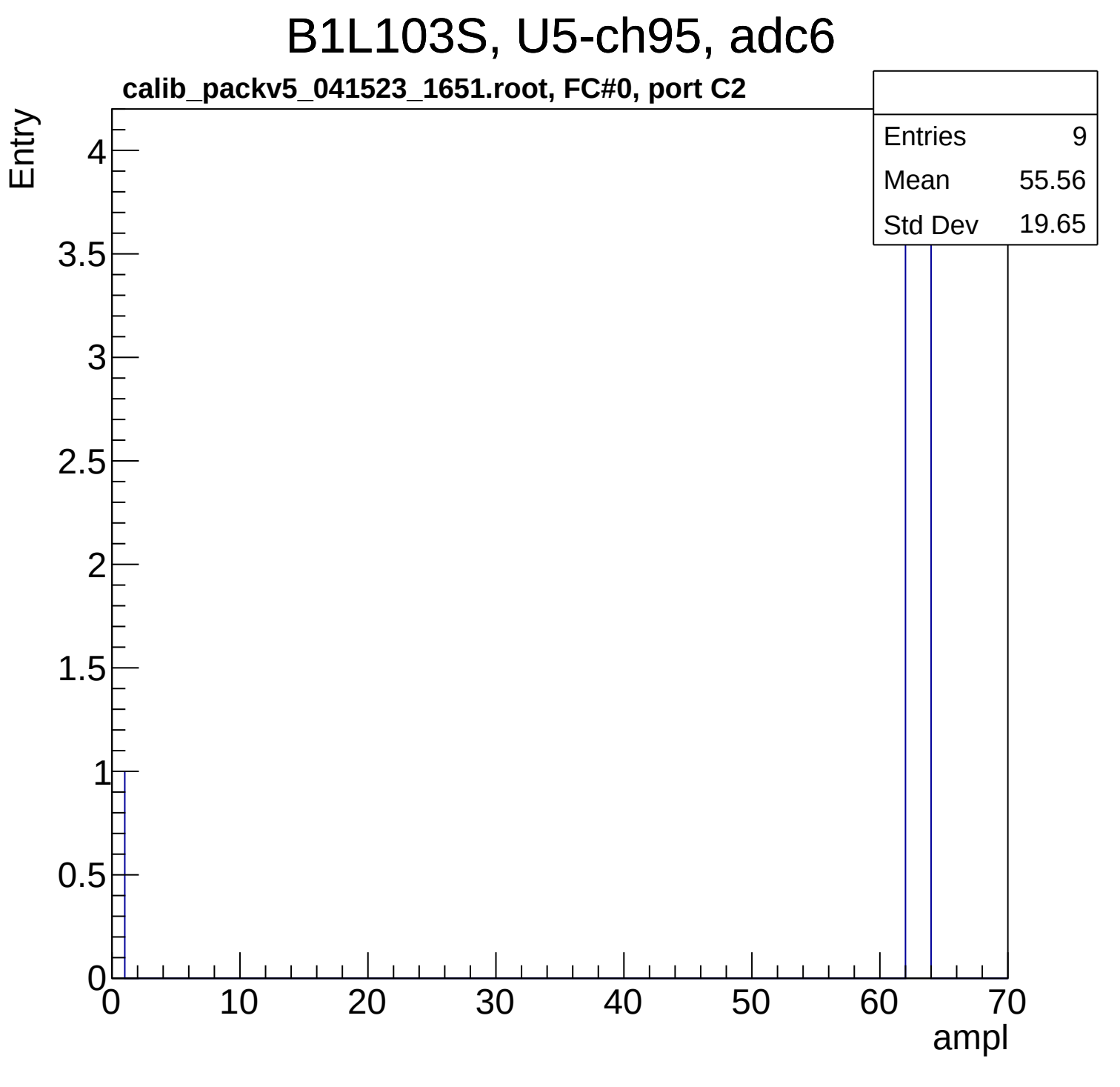
B1L103S, U5-ch95, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 55.56
Std Dev 19.65
Entry
ampl
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1.5
2
2.5
3
3.5
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0
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20
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40
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60
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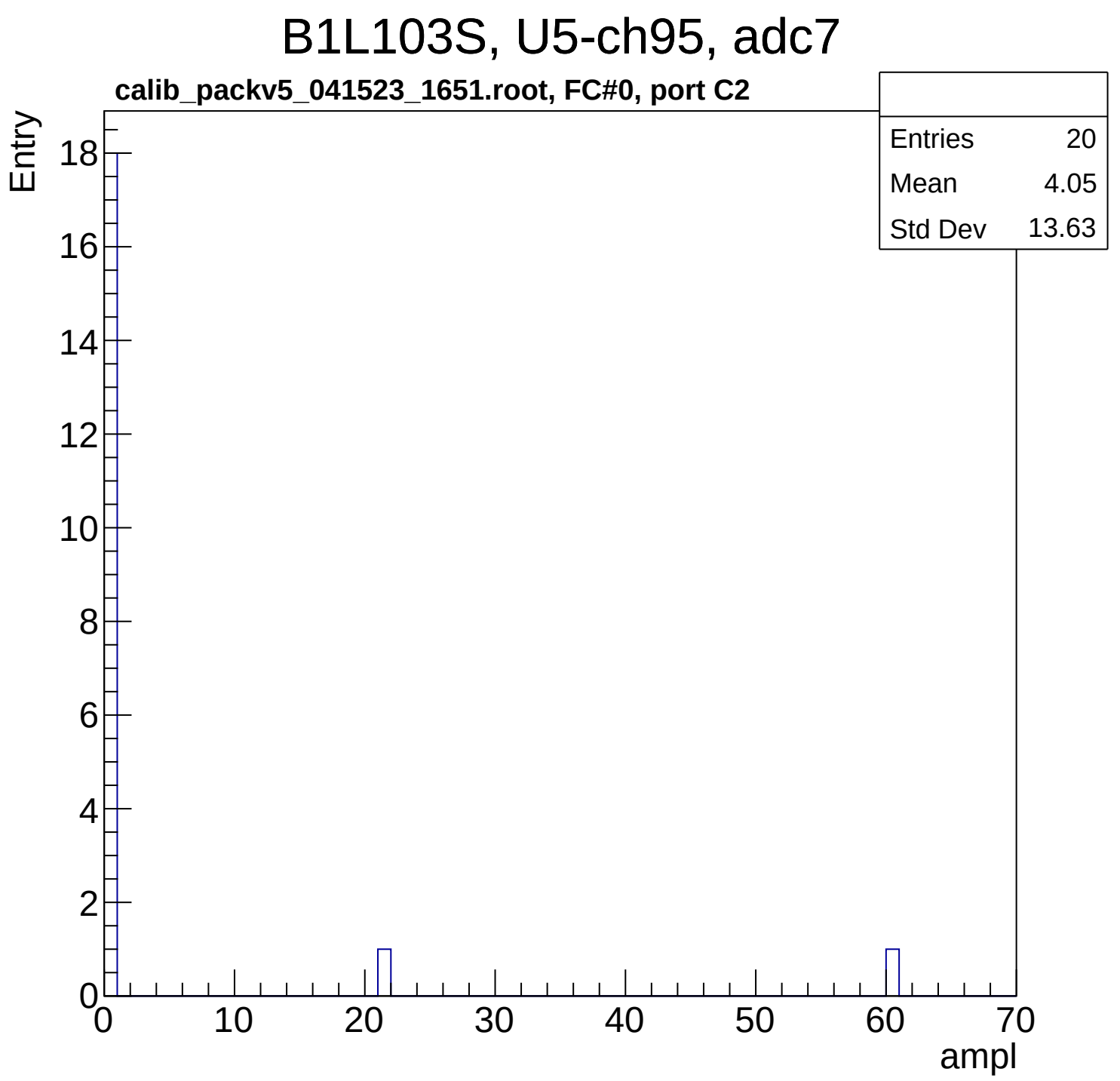
B1L103S, U5-ch95, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.05
Std Dev 13.63
Entry
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6
8
10
12
14
16
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10
20
30
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50
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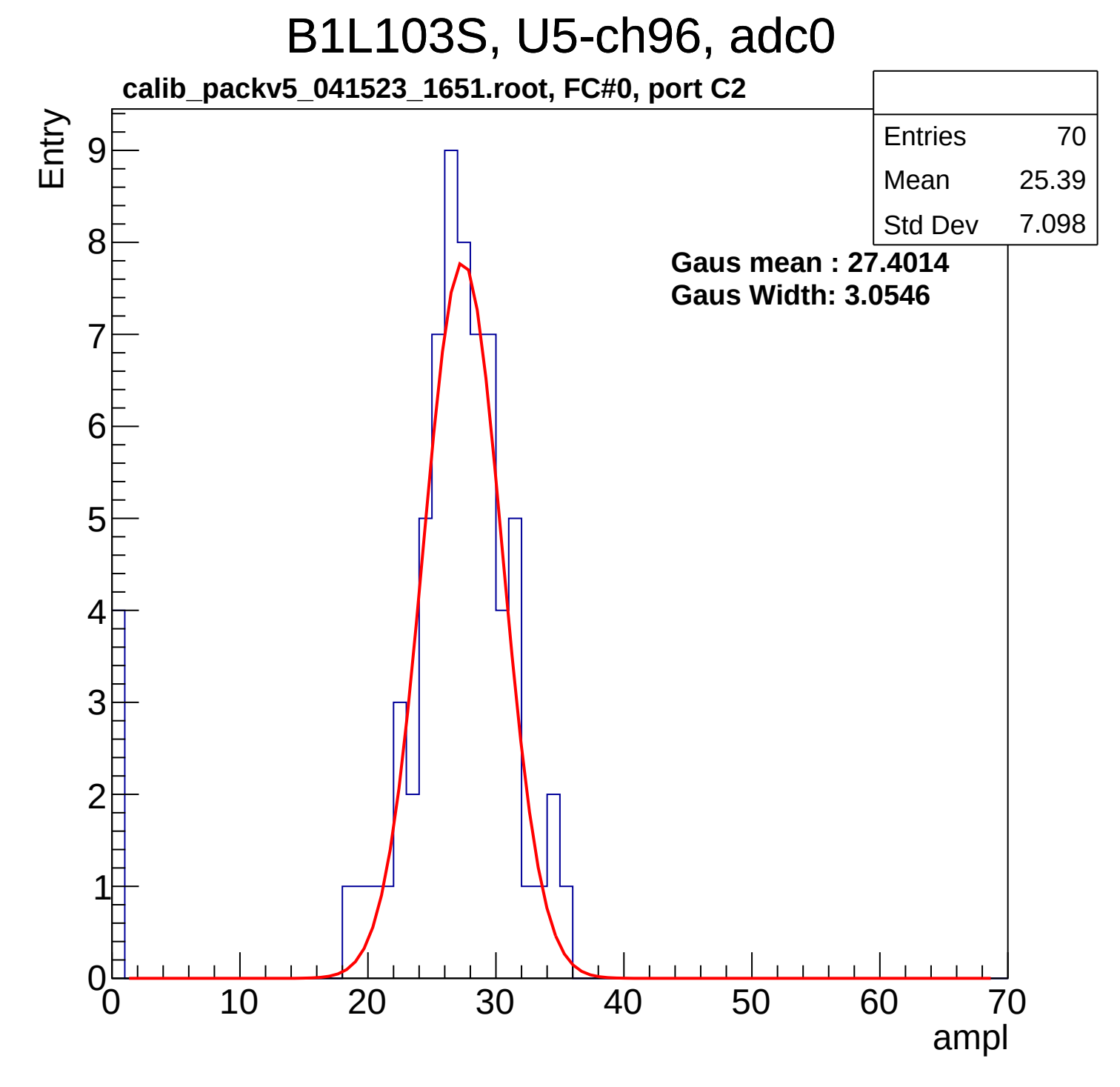
70
ampl


B1L103S, U5-ch96, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 25.39
Std Dev 7.098
Gaus mean : 27.4014
Gaus Width: 3.0546
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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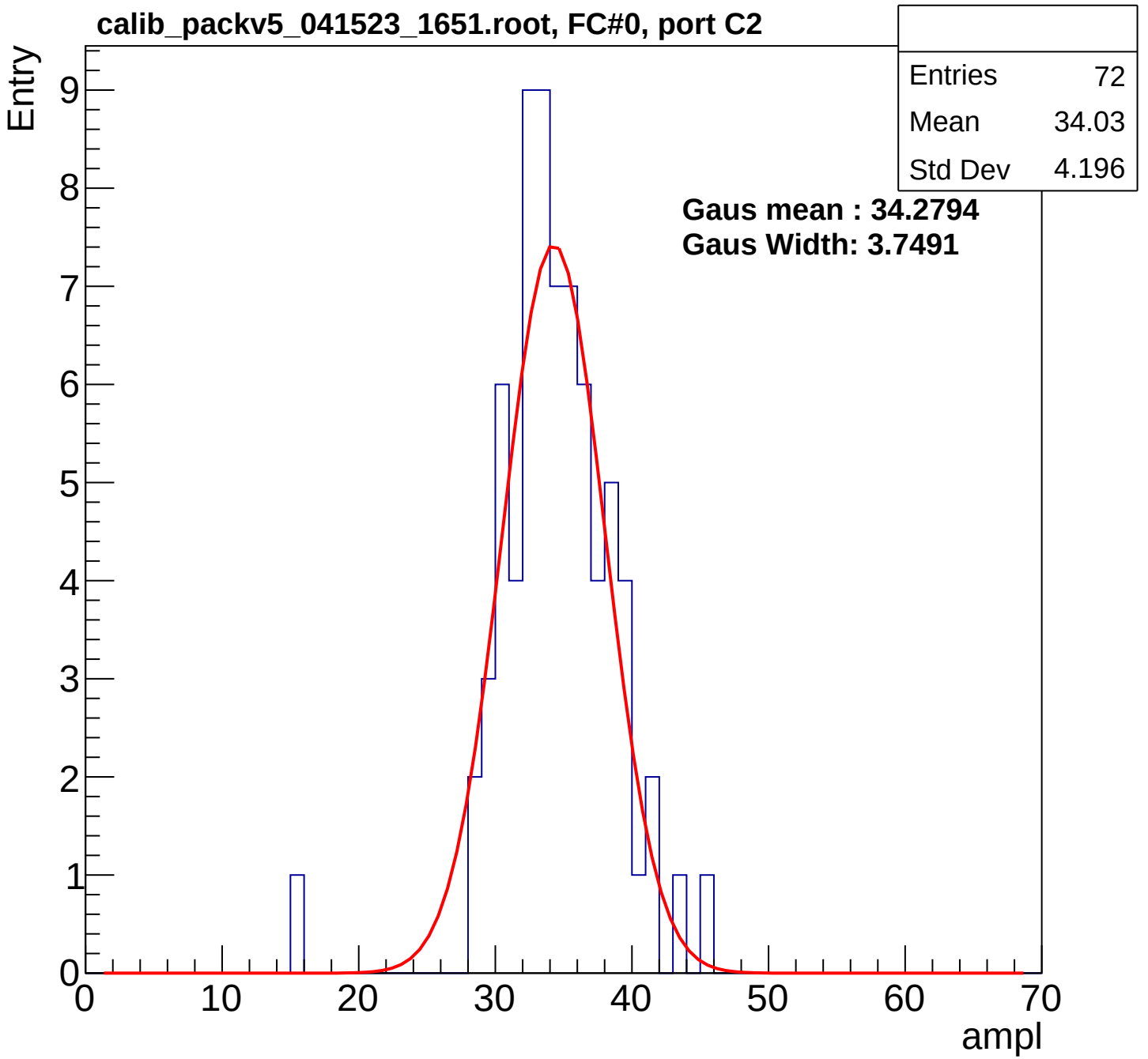
B1L103S, U5-ch96, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 34.03
Std Dev 4.196
Gaus mean : 34.2794
Gaus Width: 3.7491
Entry
ampl
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2
3
4
5
6
7
8
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0
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20
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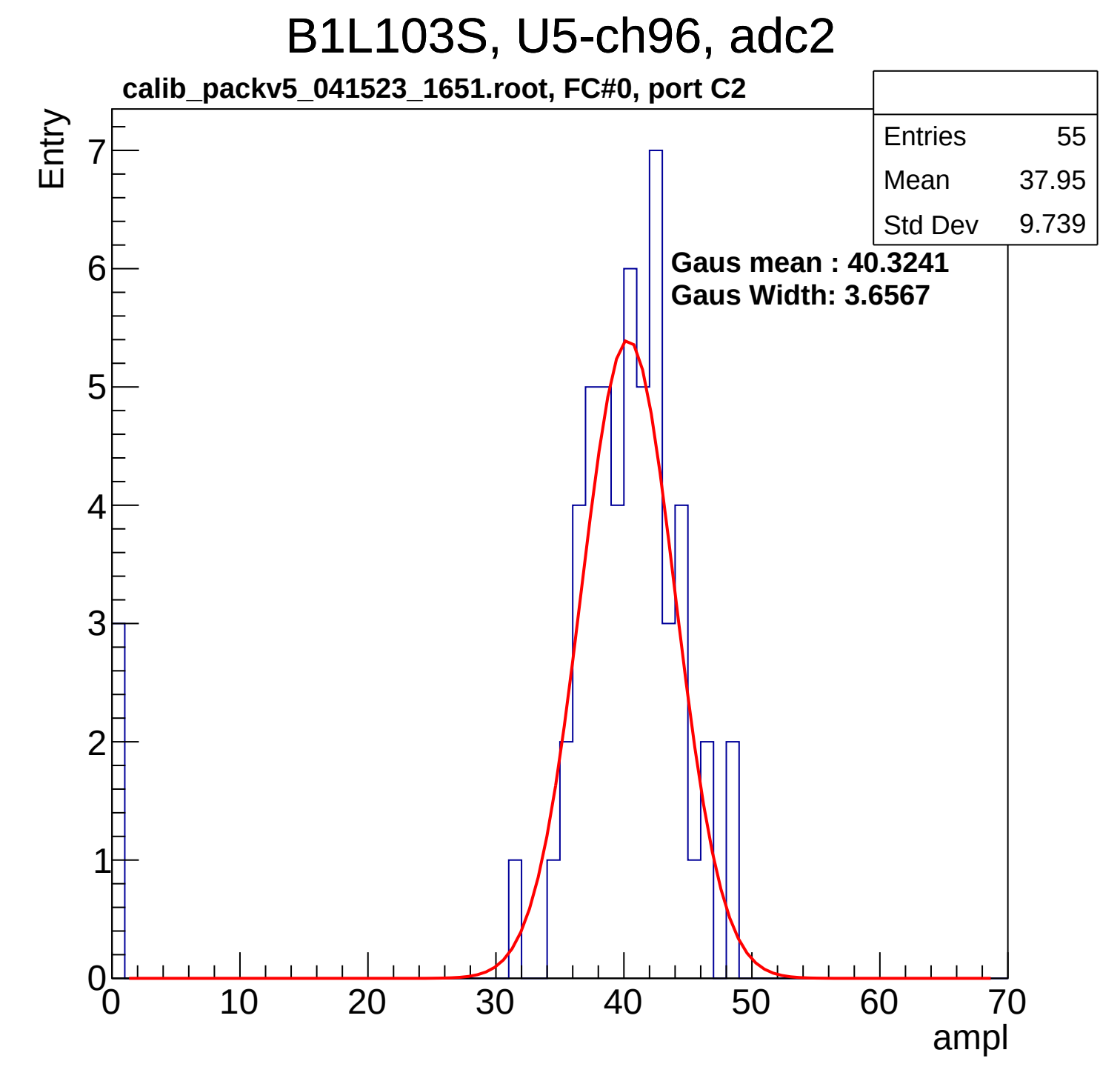
B1L103S, U5-ch96, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 37.95
Std Dev 9.739
Gaus mean : 40.3241
Gaus Width: 3.6567
Entry
ampl
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2
3
4
5
6
7
0
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20
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60
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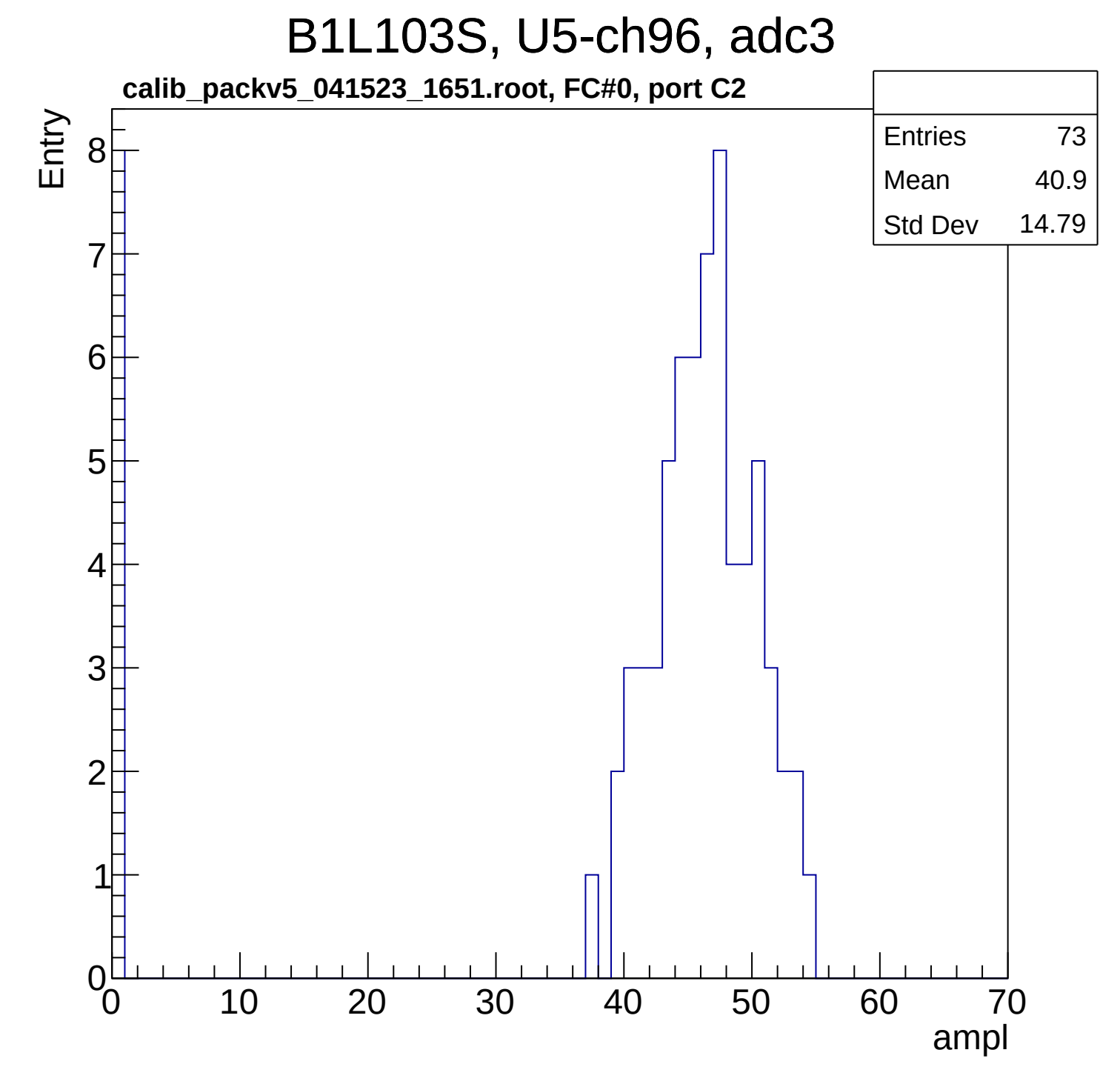
B1L103S, U5-ch96, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 40.9
Std Dev 14.79
Entry
ampl
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2
3
4
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6
7
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40
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60
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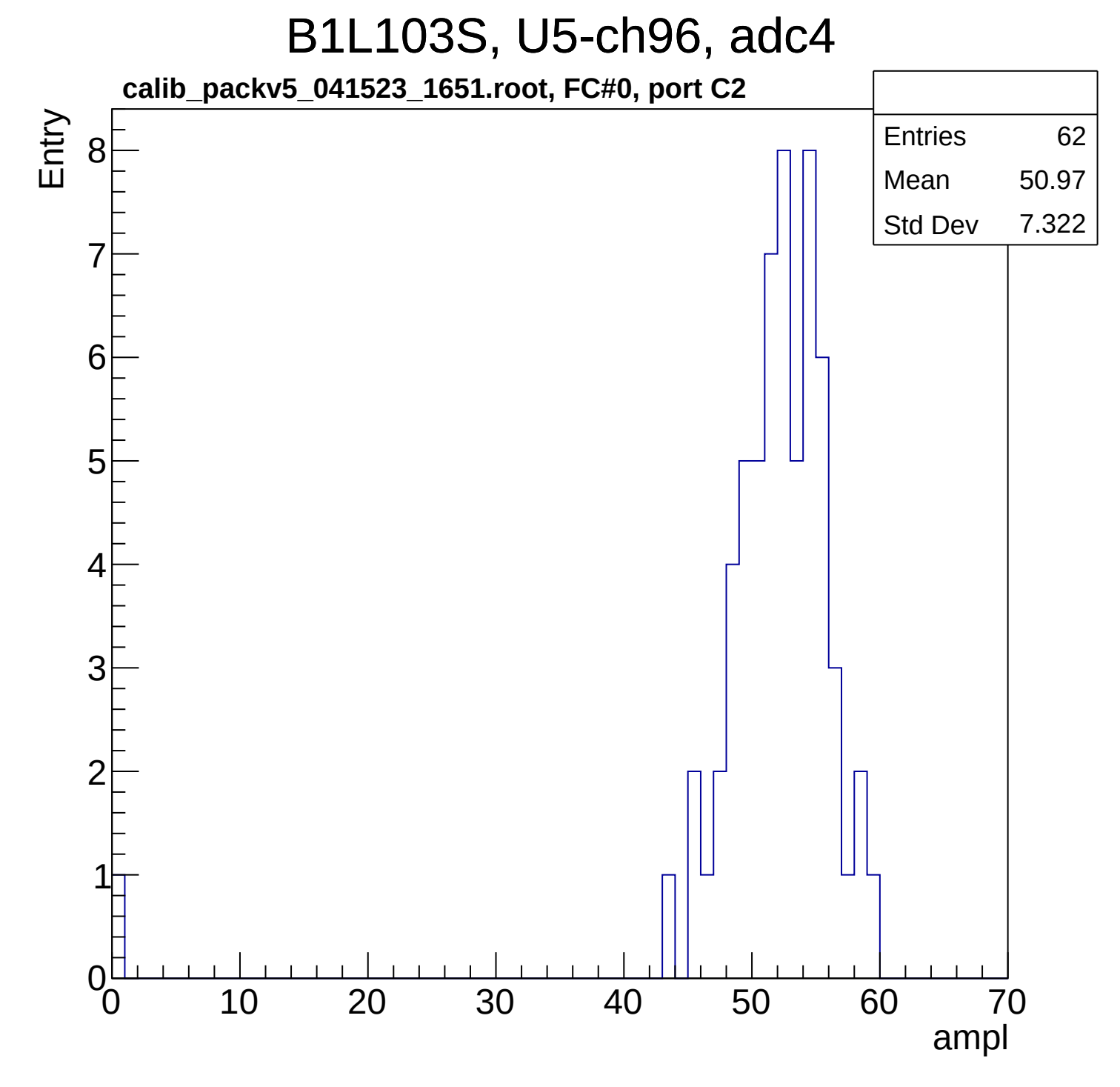
B1L103S, U5-ch96, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 50.97
Std Dev 7.322
Entry
ampl
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2
3
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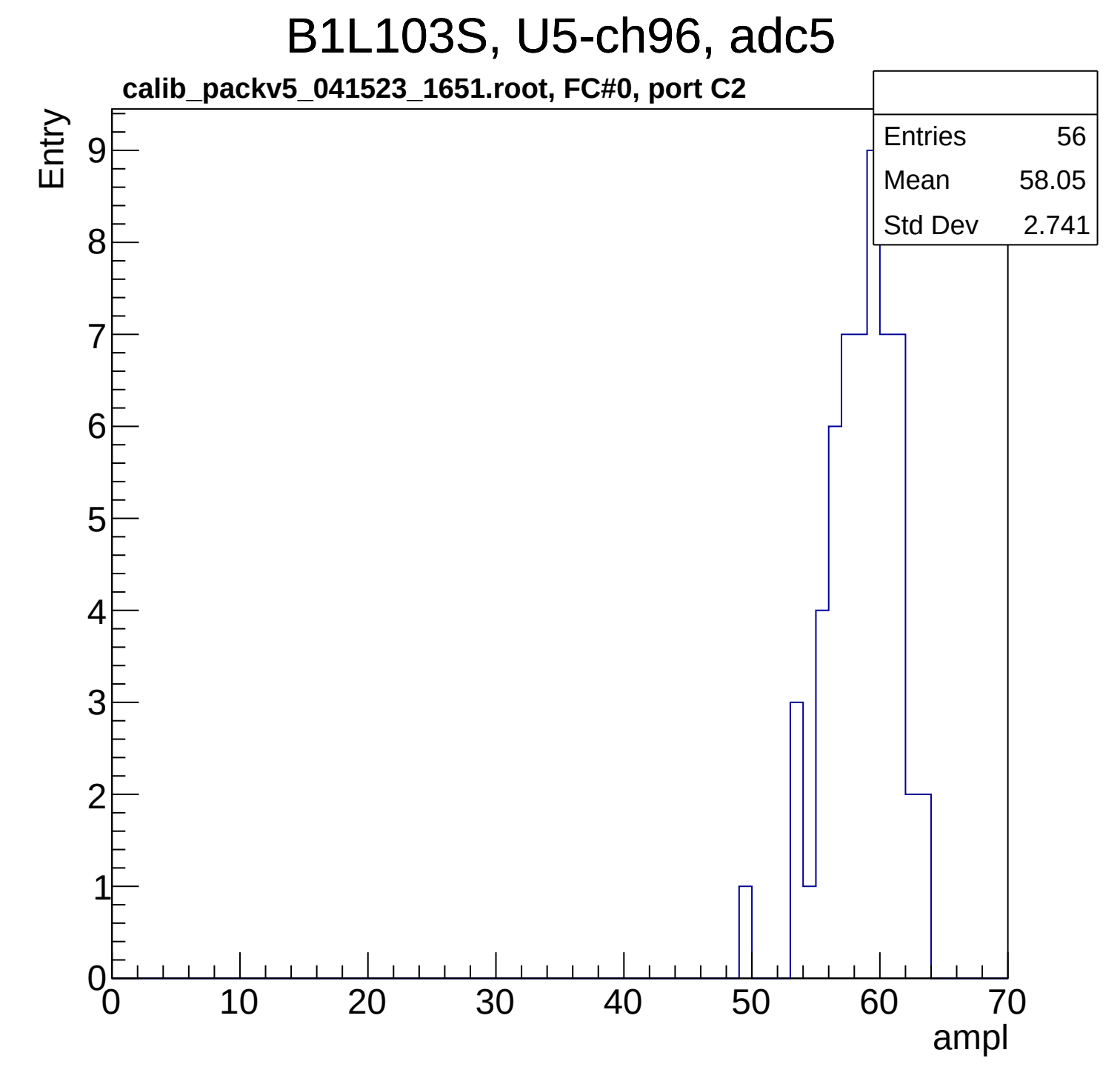
B1L103S, U5-ch96, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.05
Std Dev 2.741
Entry
ampl
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3
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5
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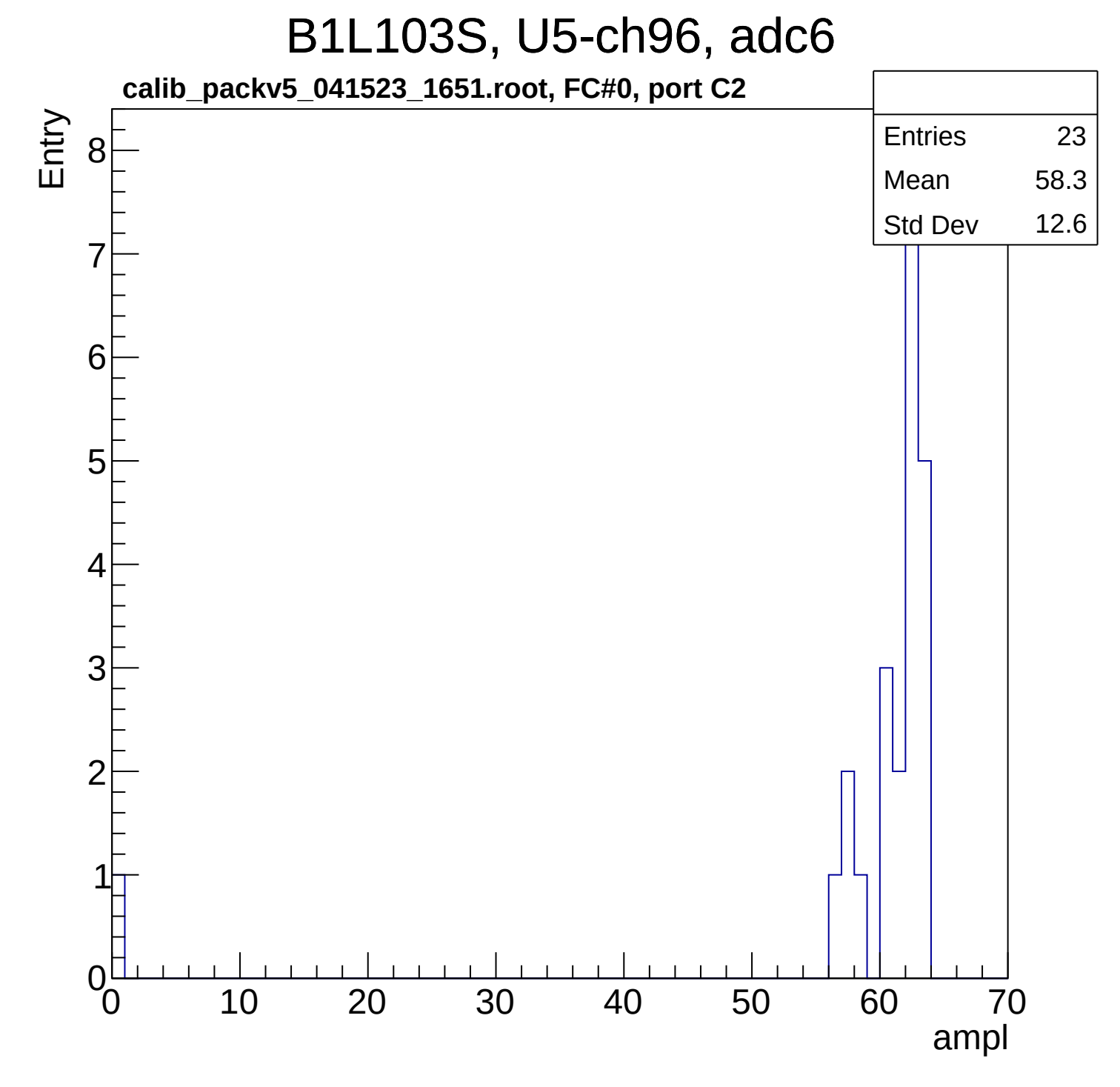
B1L103S, U5-ch96, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 58.3
Std Dev 12.6
Entry
ampl
0
1
2
3
4
5
6
7
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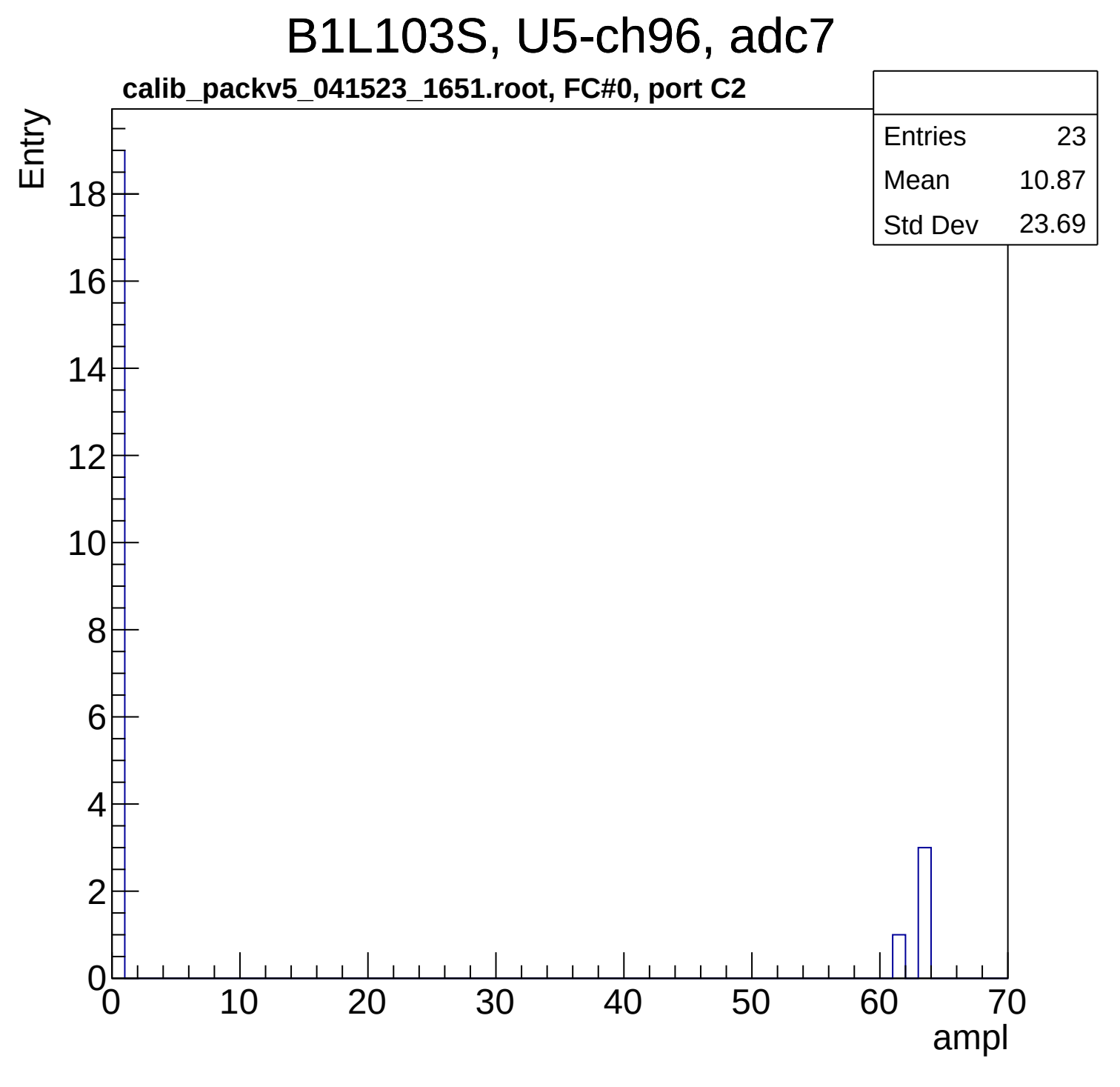
B1L103S, U5-ch96, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.87
Std Dev 23.69
Entry
0
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6
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16
18
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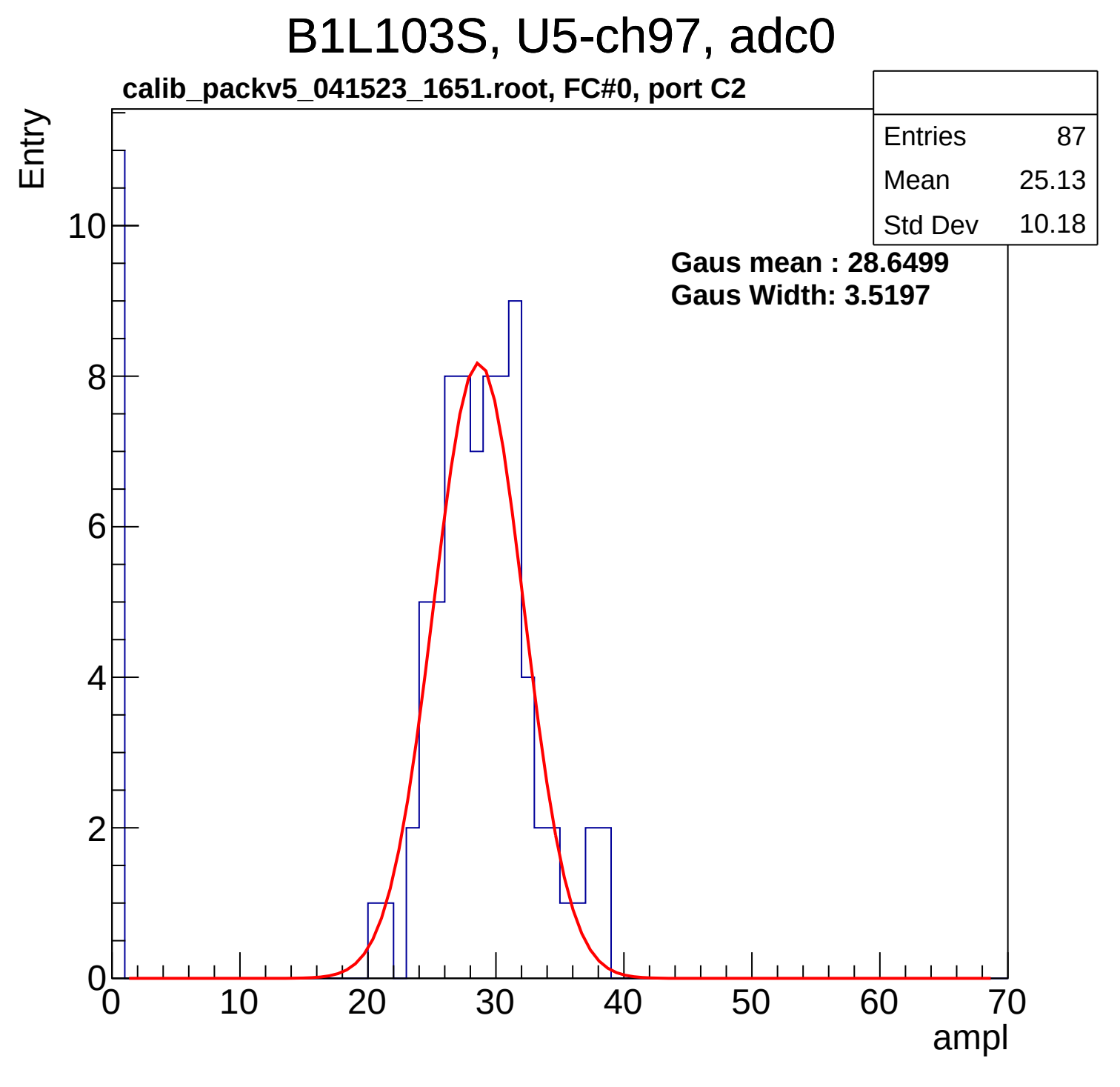
ampl


B1L103S, U5-ch97, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 25.13
Std Dev 10.18
Gaus mean : 28.6499
Gaus Width: 3.5197
Entry
ampl
0
2
4
6
8
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0
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40
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60
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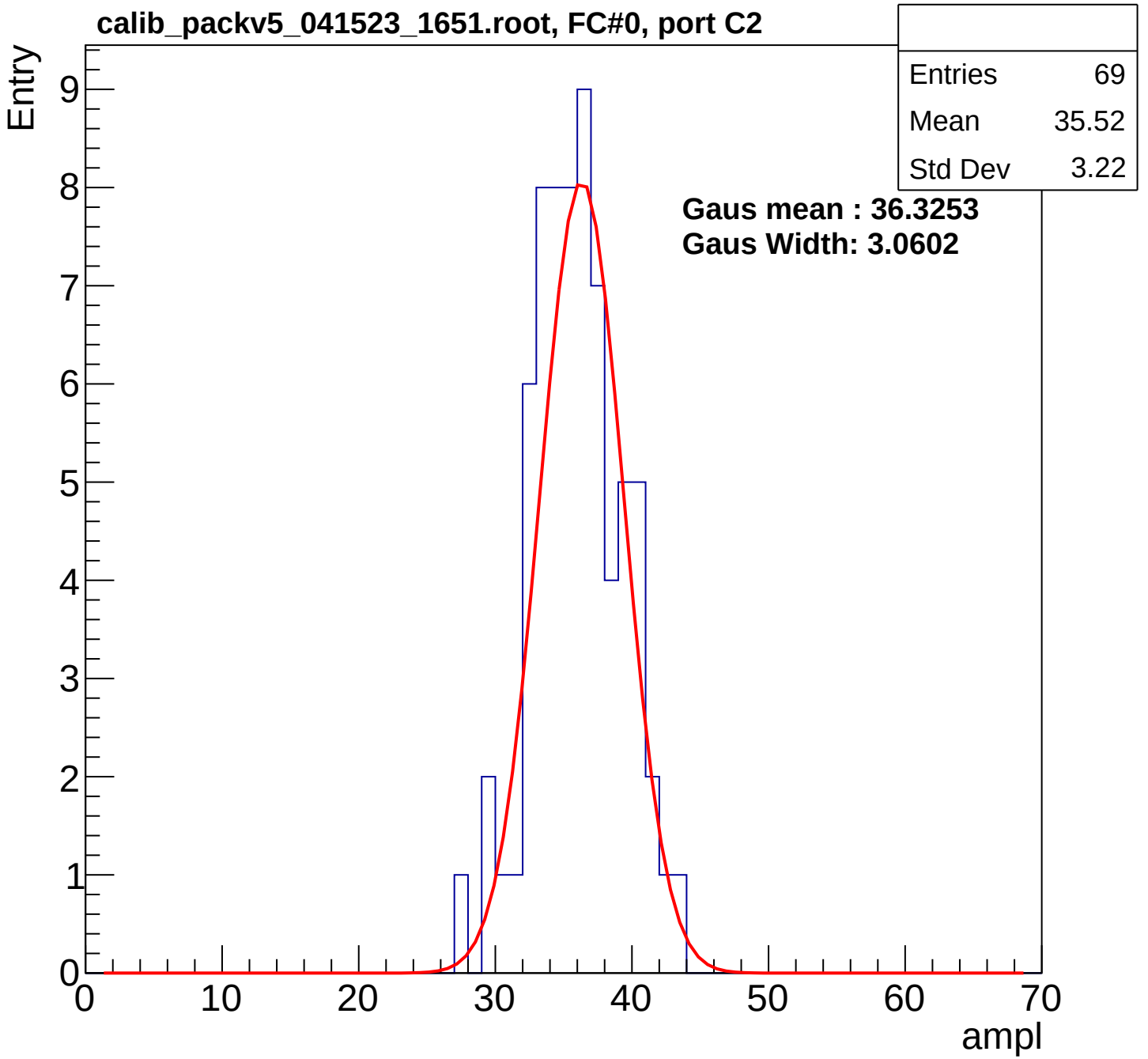
B1L103S, U5-ch97, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 35.52
Std Dev 3.22
Gaus mean : 36.3253
Gaus Width: 3.0602
Entry
ampl
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3
4
5
6
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8
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0
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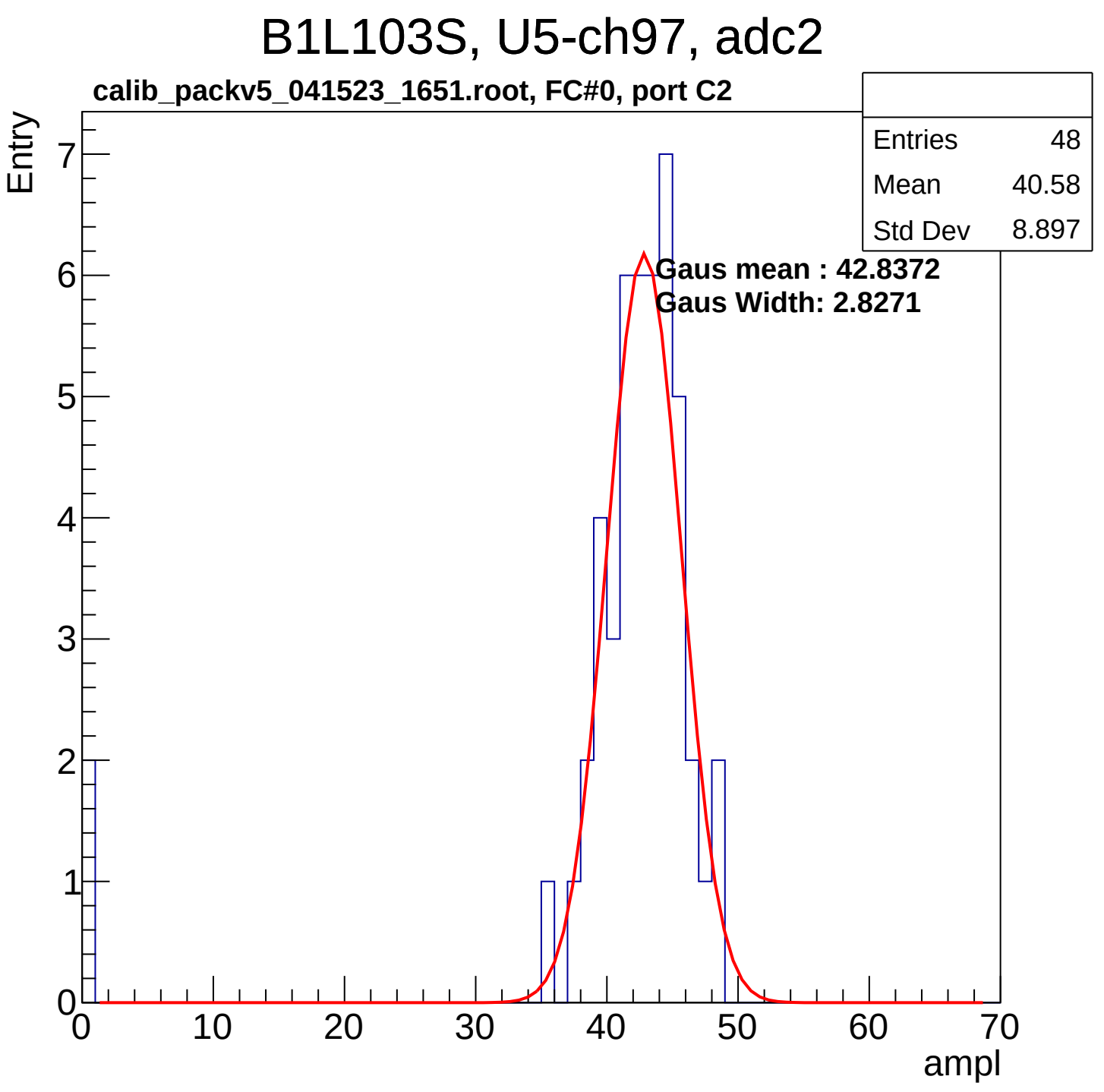
B1L103S, U5-ch97, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 40.58
Std Dev 8.897
Gaus mean : 42.8372
Gaus Width: 2.8271
Entry
ampl
0
1
2
3
4
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0
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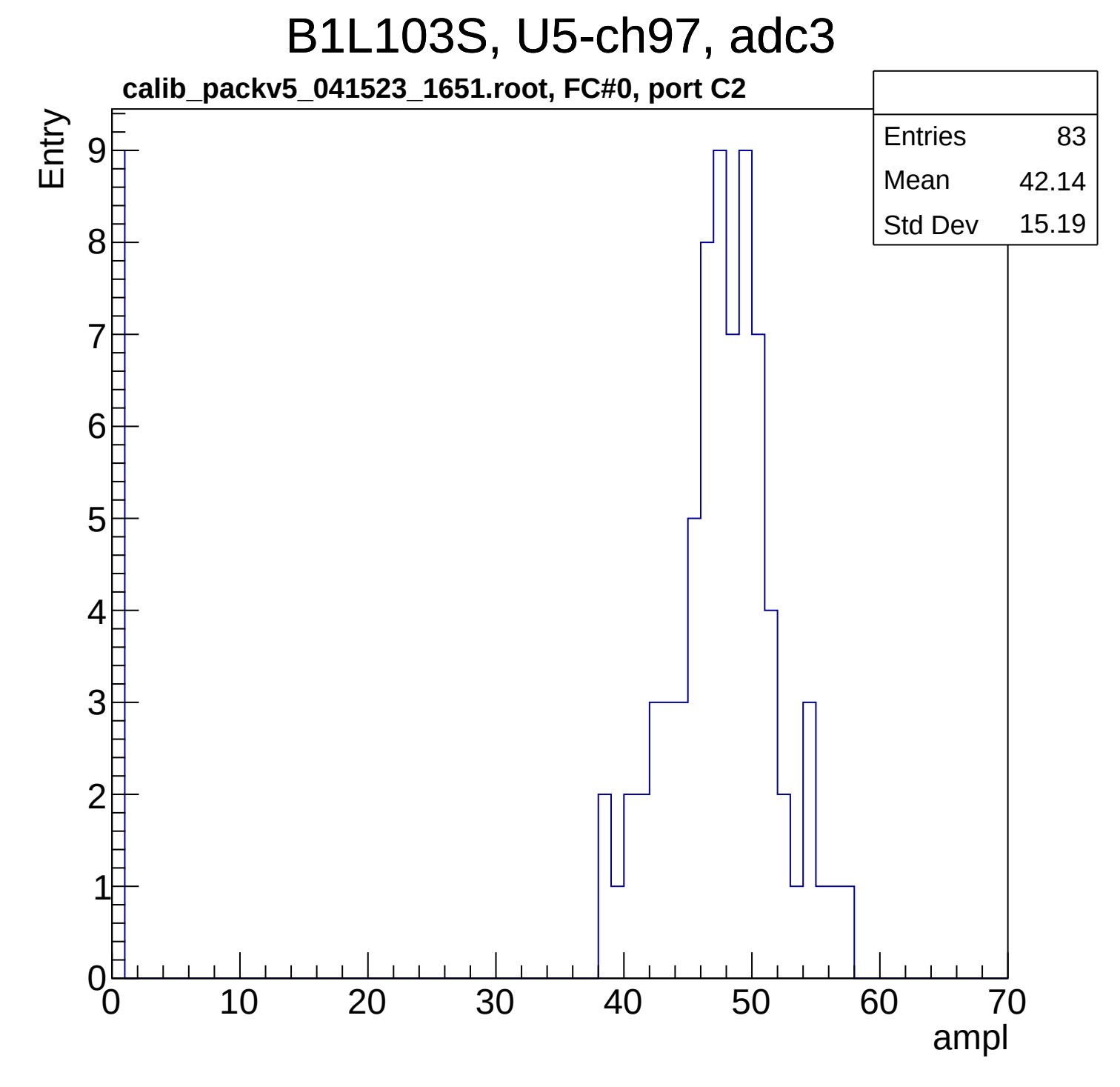
B1L103S, U5-ch97, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 42.14
Std Dev 15.19
Entry
ampl
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1
2
3
4
5
6
7
8
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0
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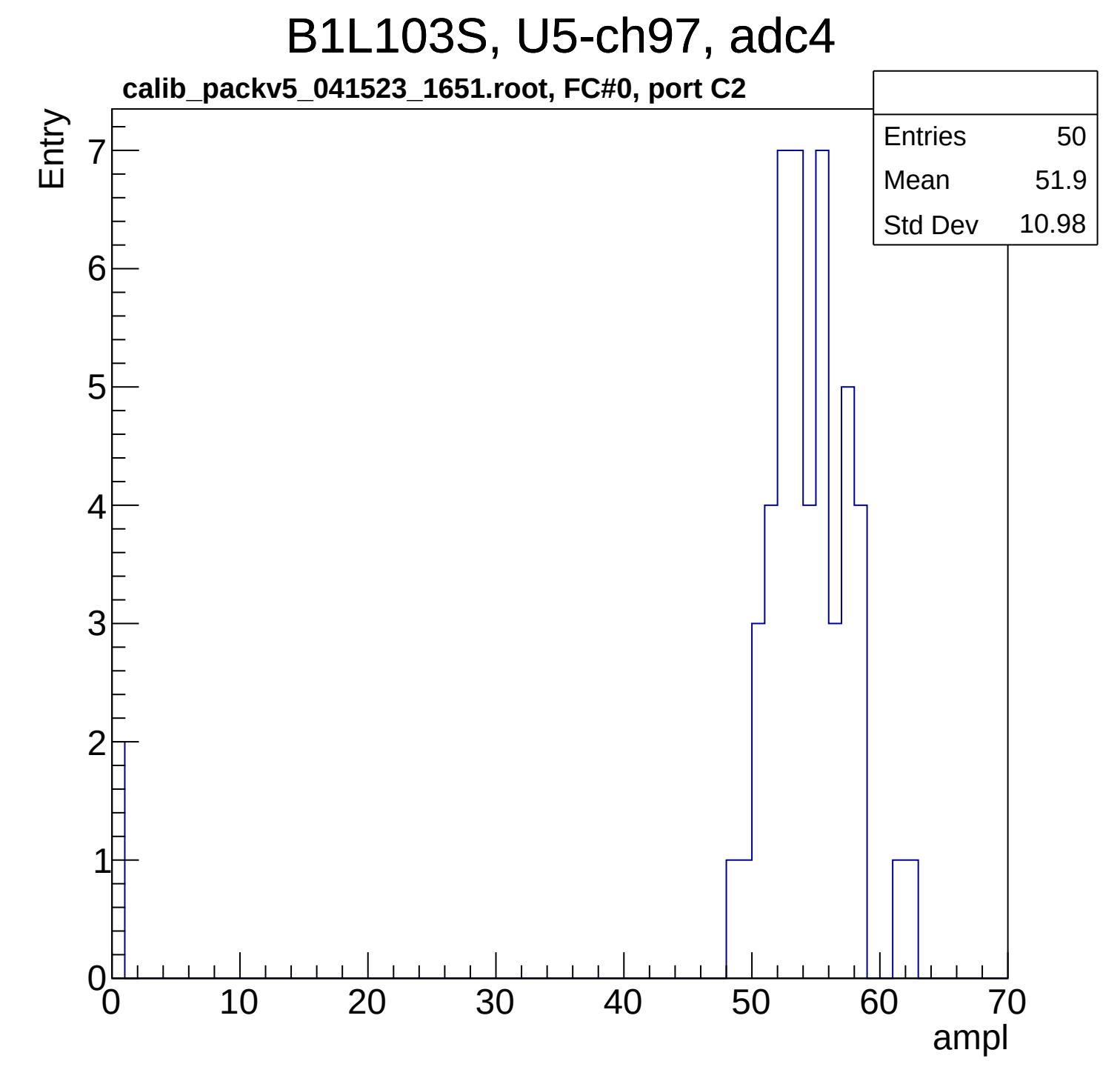
B1L103S, U5-ch97, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 51.9
Std Dev 10.98
Entry
ampl
0
1
2
3
4
5
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0
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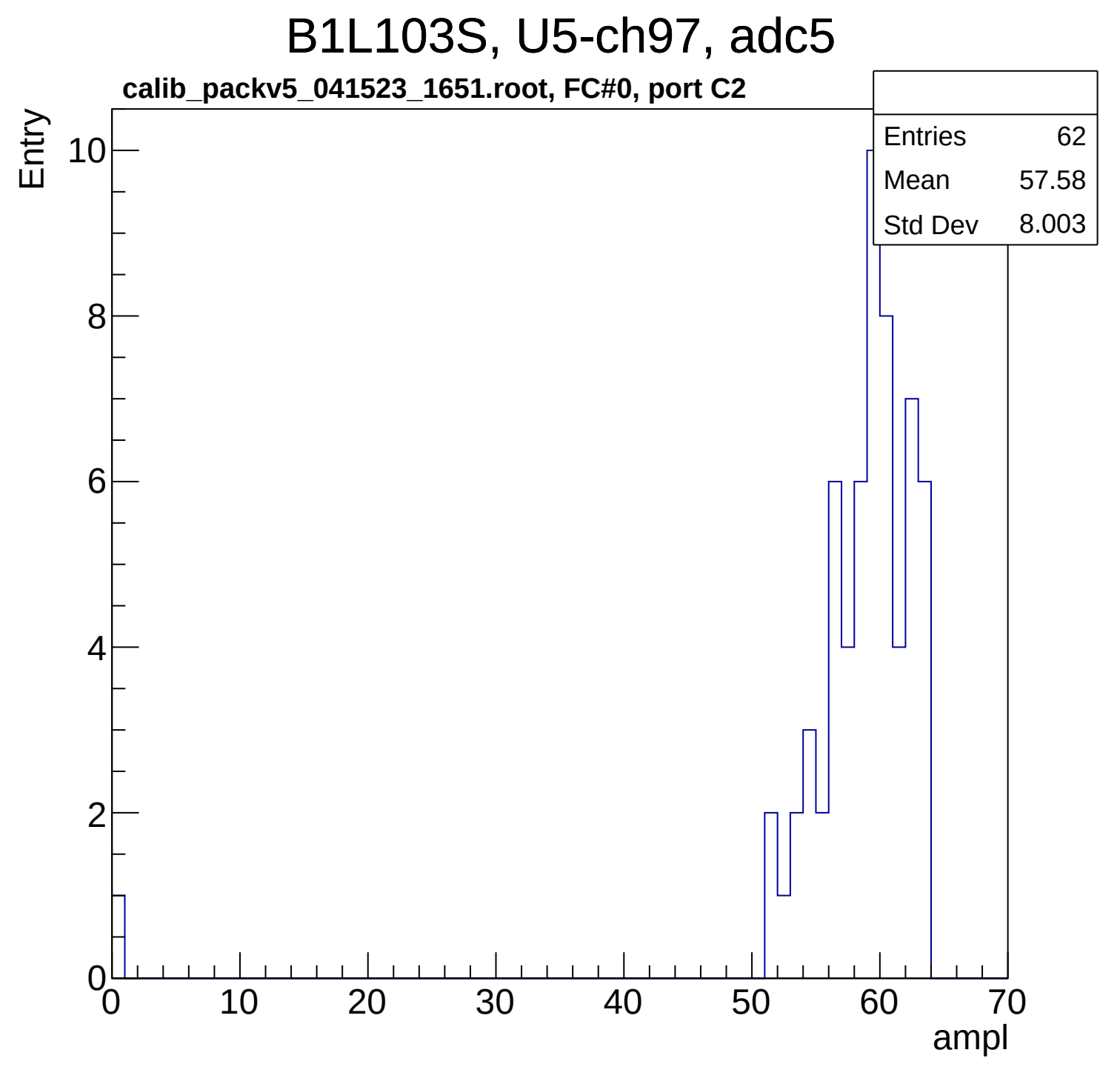
B1L103S, U5-ch97, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 57.58
Std Dev 8.003
Entry
ampl
0
2
4
6
8
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0
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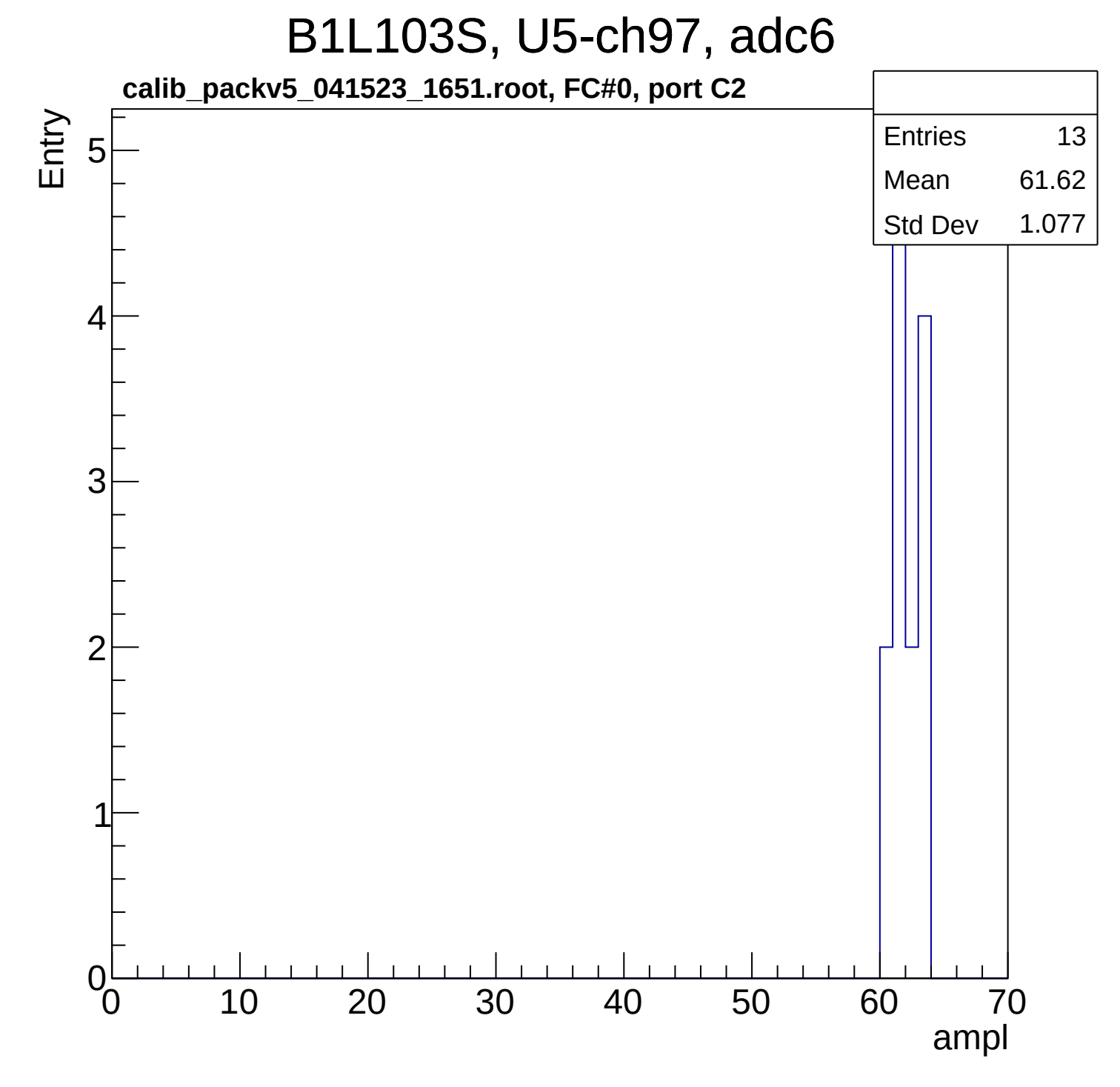
B1L103S, U5-ch97, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.62
Std Dev 1.077
Entry
ampl
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1
2
3
4
5
0
10
20
30
40
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60
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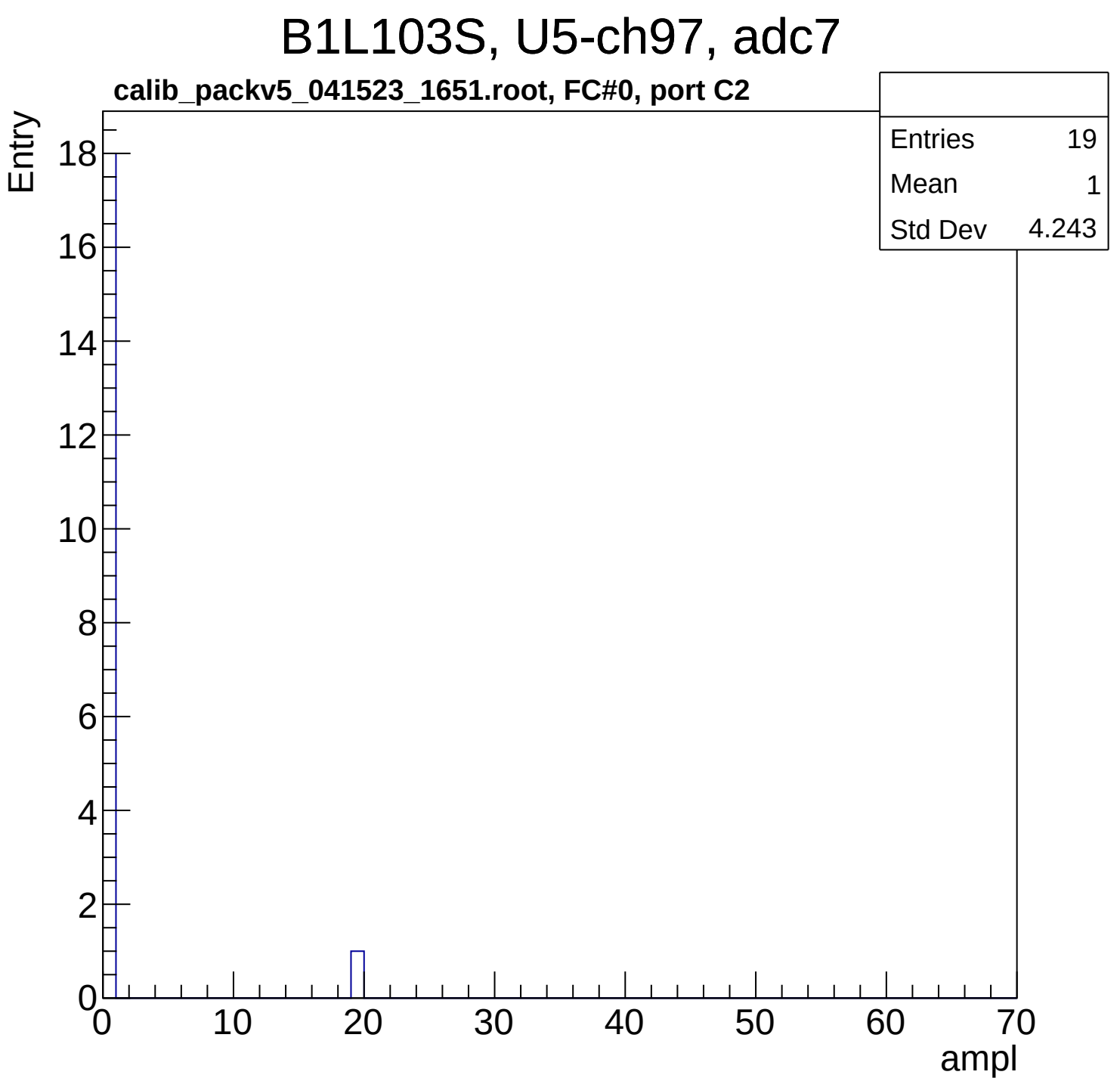
B1L103S, U5-ch97, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1
Std Dev 4.243
Entry
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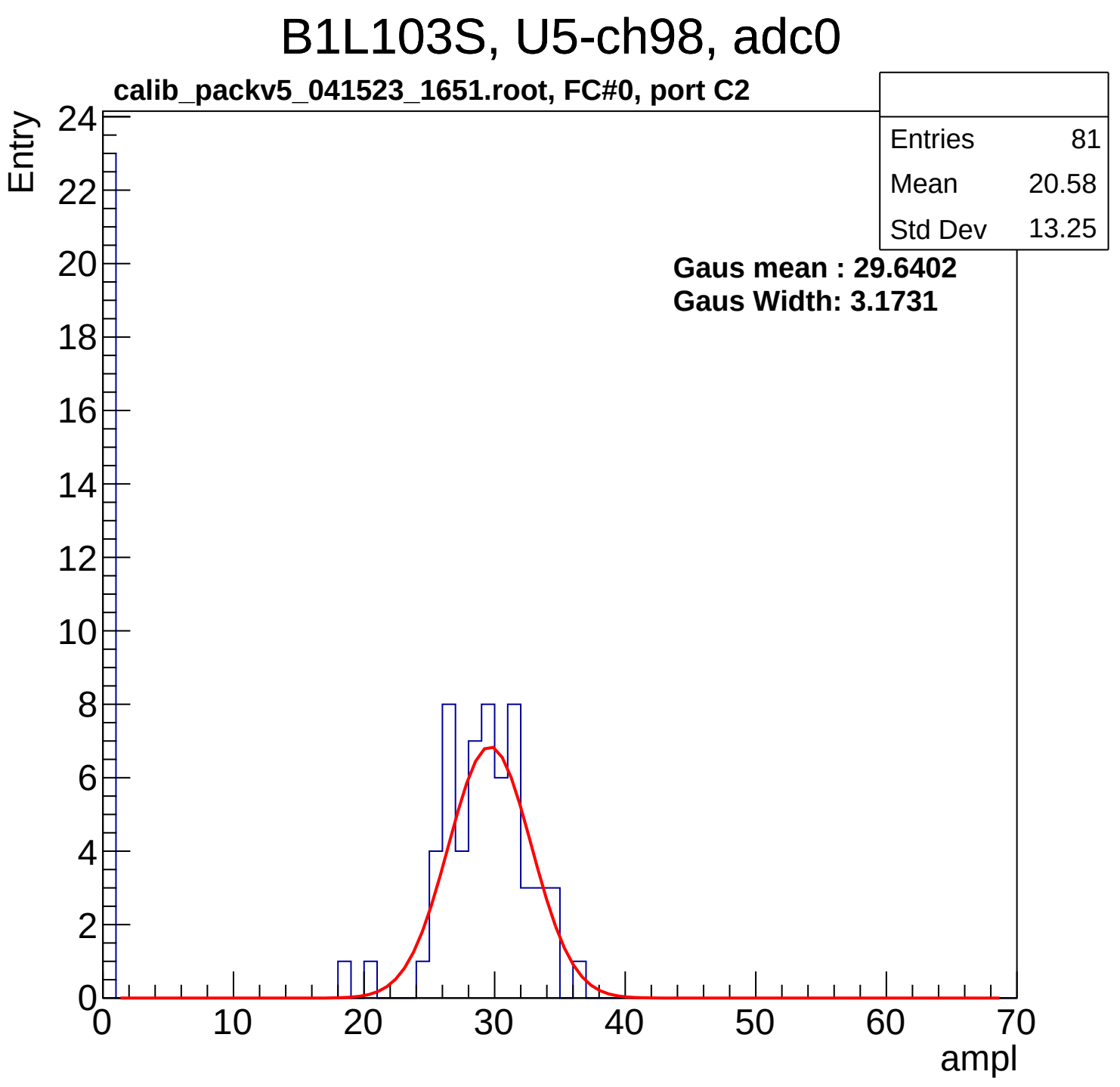
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch98, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 20.58
Std Dev 13.25
Gaus mean : 29.6402
Gaus Width: 3.1731
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
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20
30
40
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60
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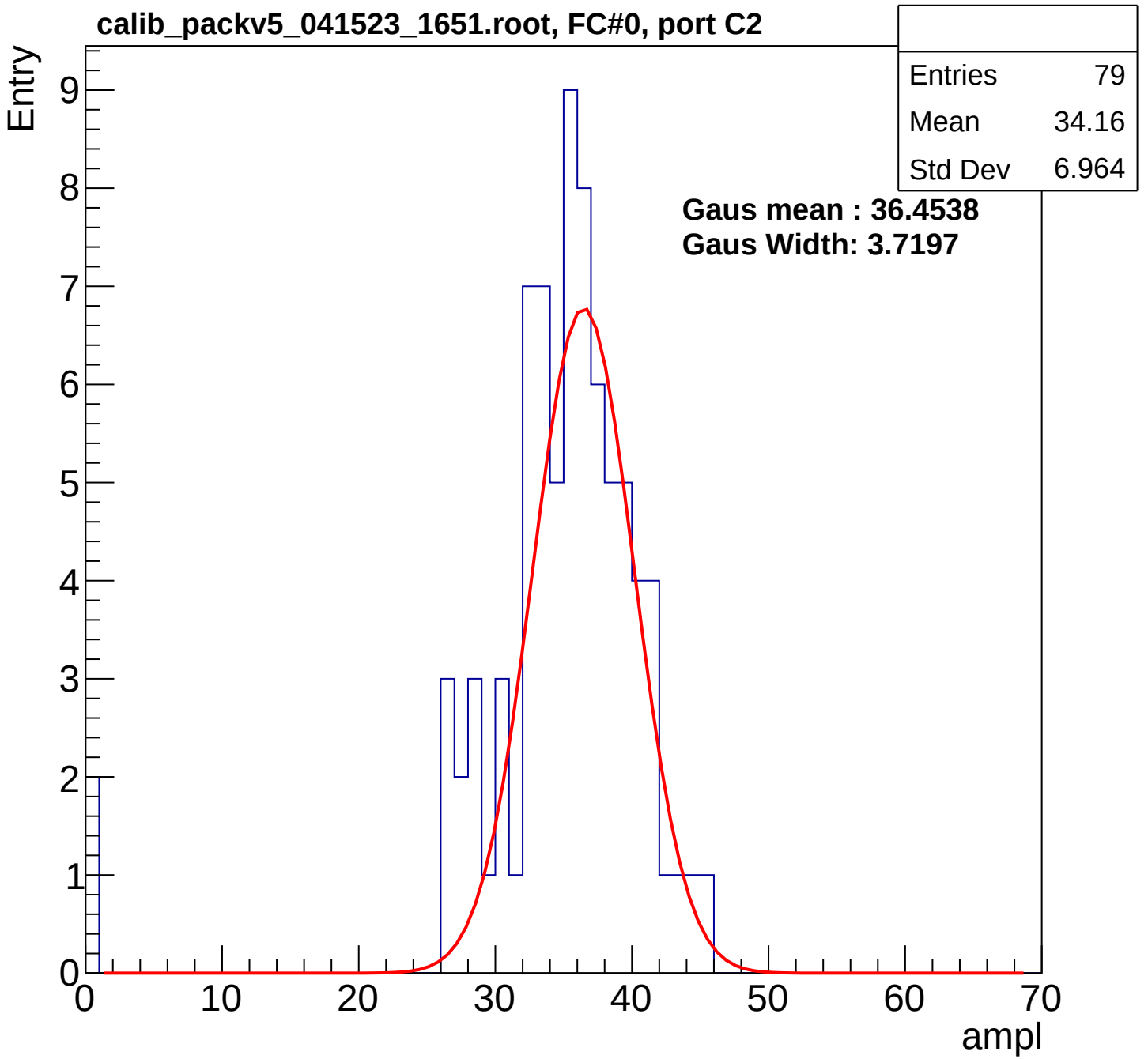
B1L103S, U5-ch98, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 34.16
Std Dev 6.964
Gaus mean : 36.4538
Gaus Width: 3.7197
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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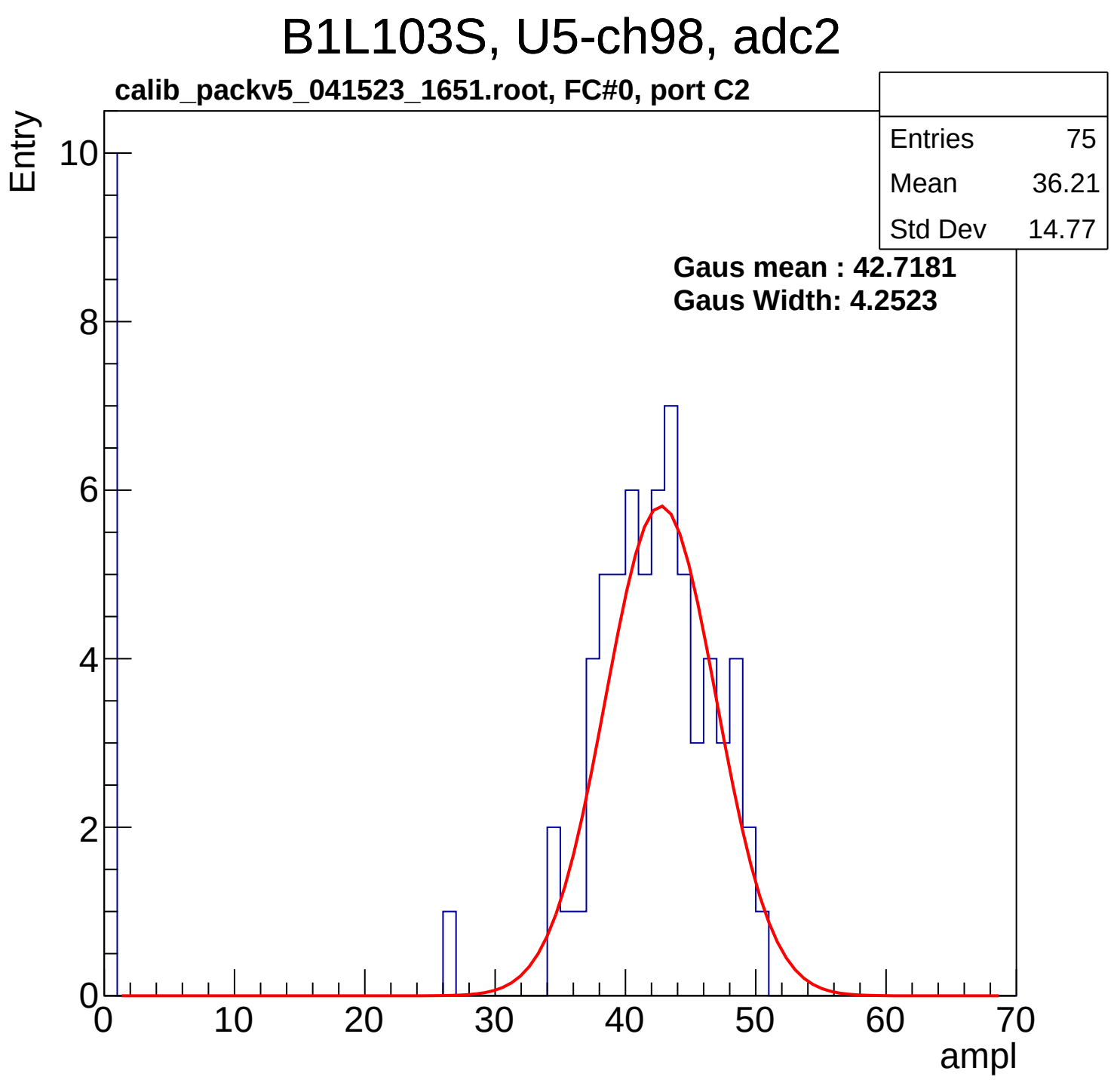
B1L103S, U5-ch98, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 36.21
Std Dev 14.77
Gaus mean : 42.7181
Gaus Width: 4.2523
Entry
ampl
0
2
4
6
8
10
0
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20
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40
50
60
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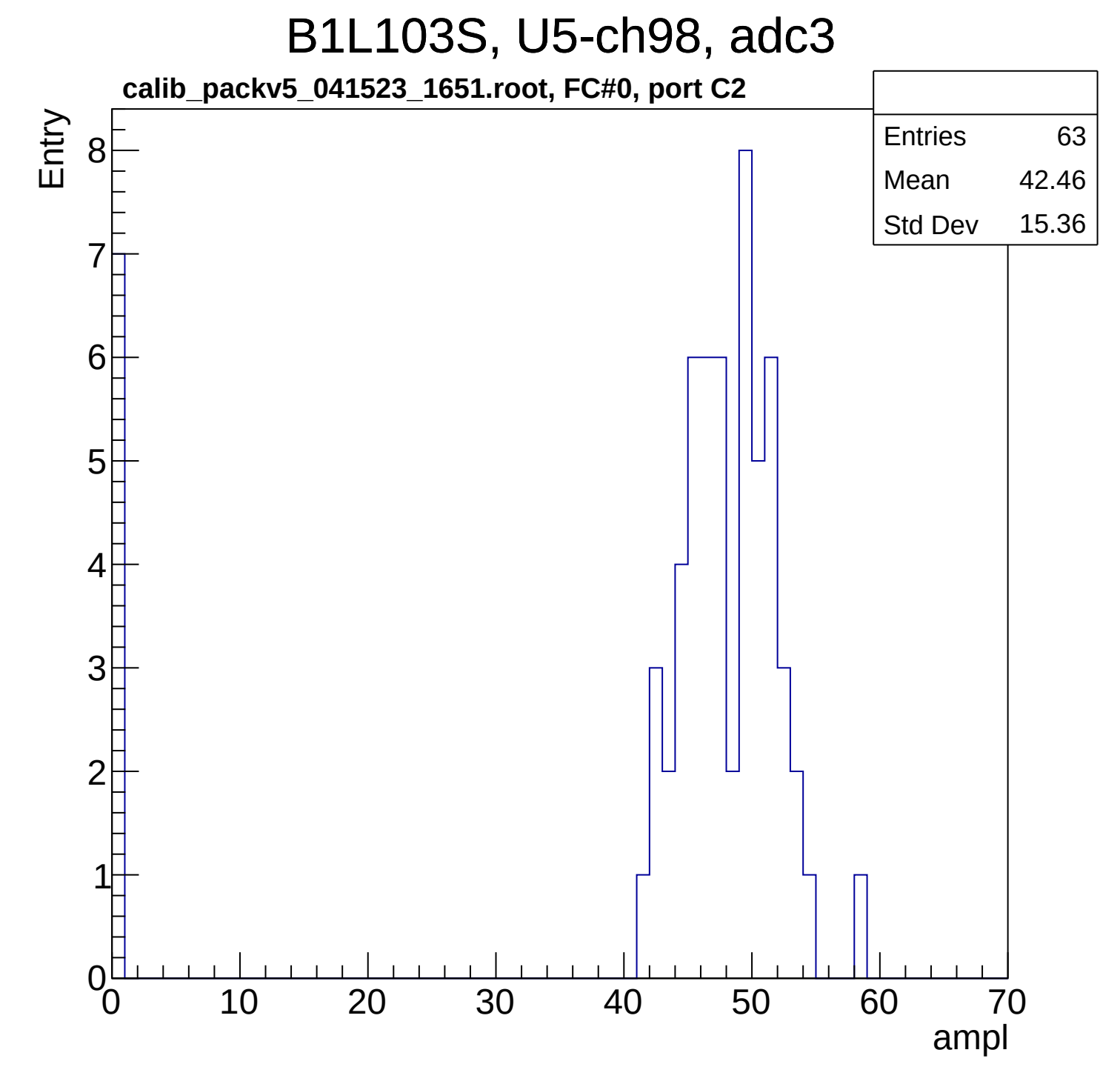
B1L103S, U5-ch98, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 42.46
Std Dev 15.36
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
50
60
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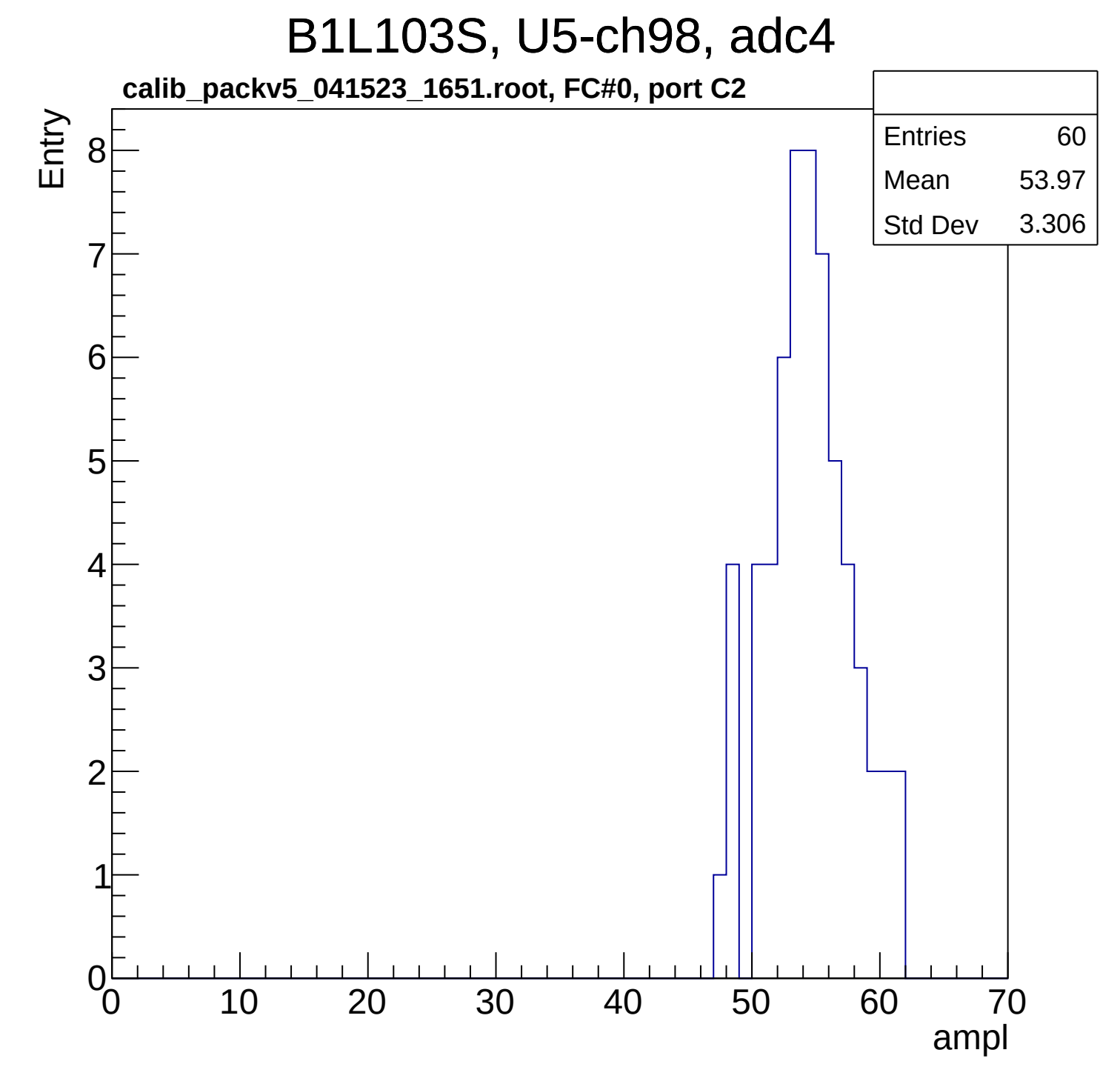
B1L103S, U5-ch98, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 53.97
Std Dev 3.306
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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60
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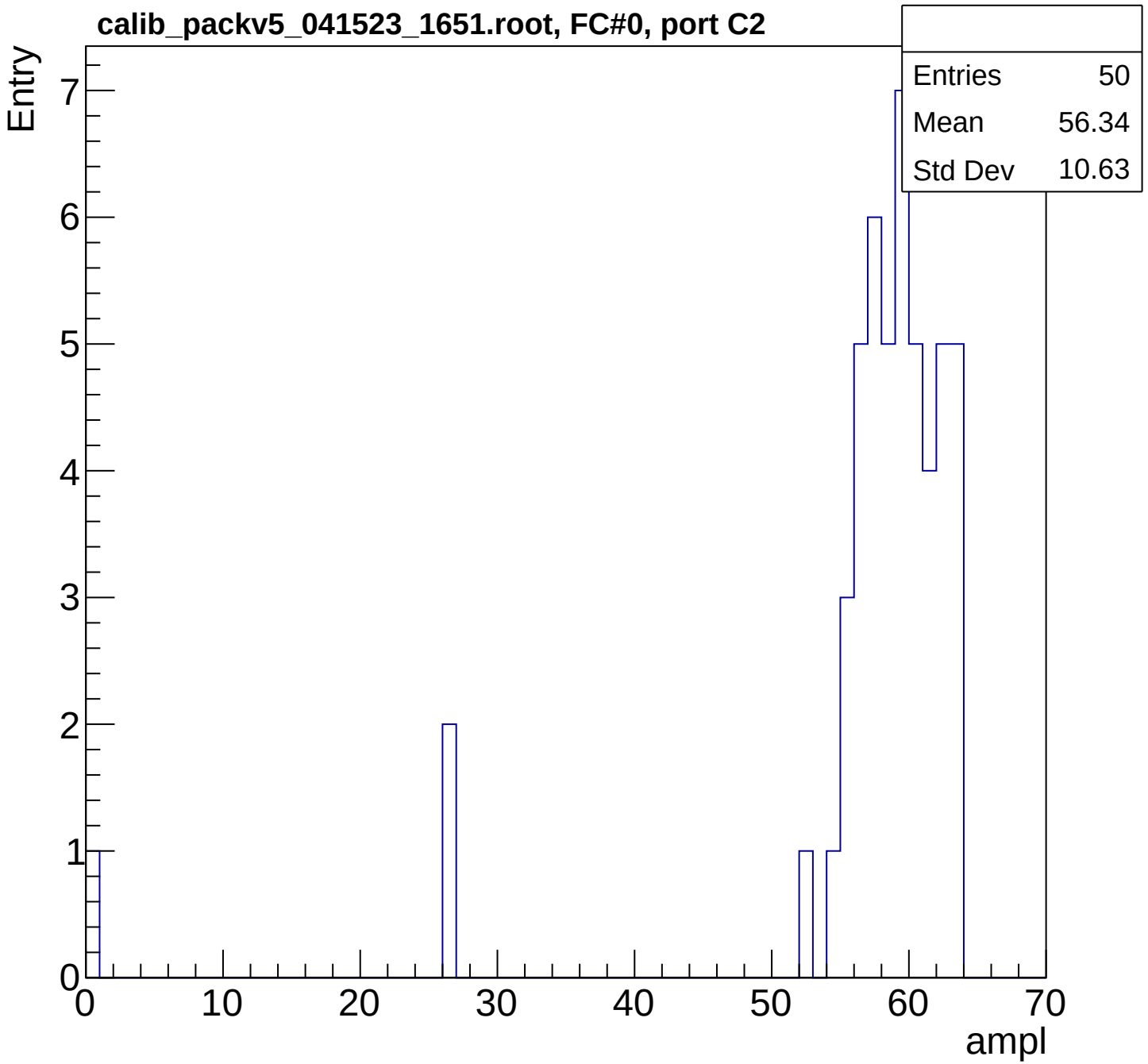
B1L103S, U5-ch98, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 56.34
Std Dev 10.63
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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40
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60
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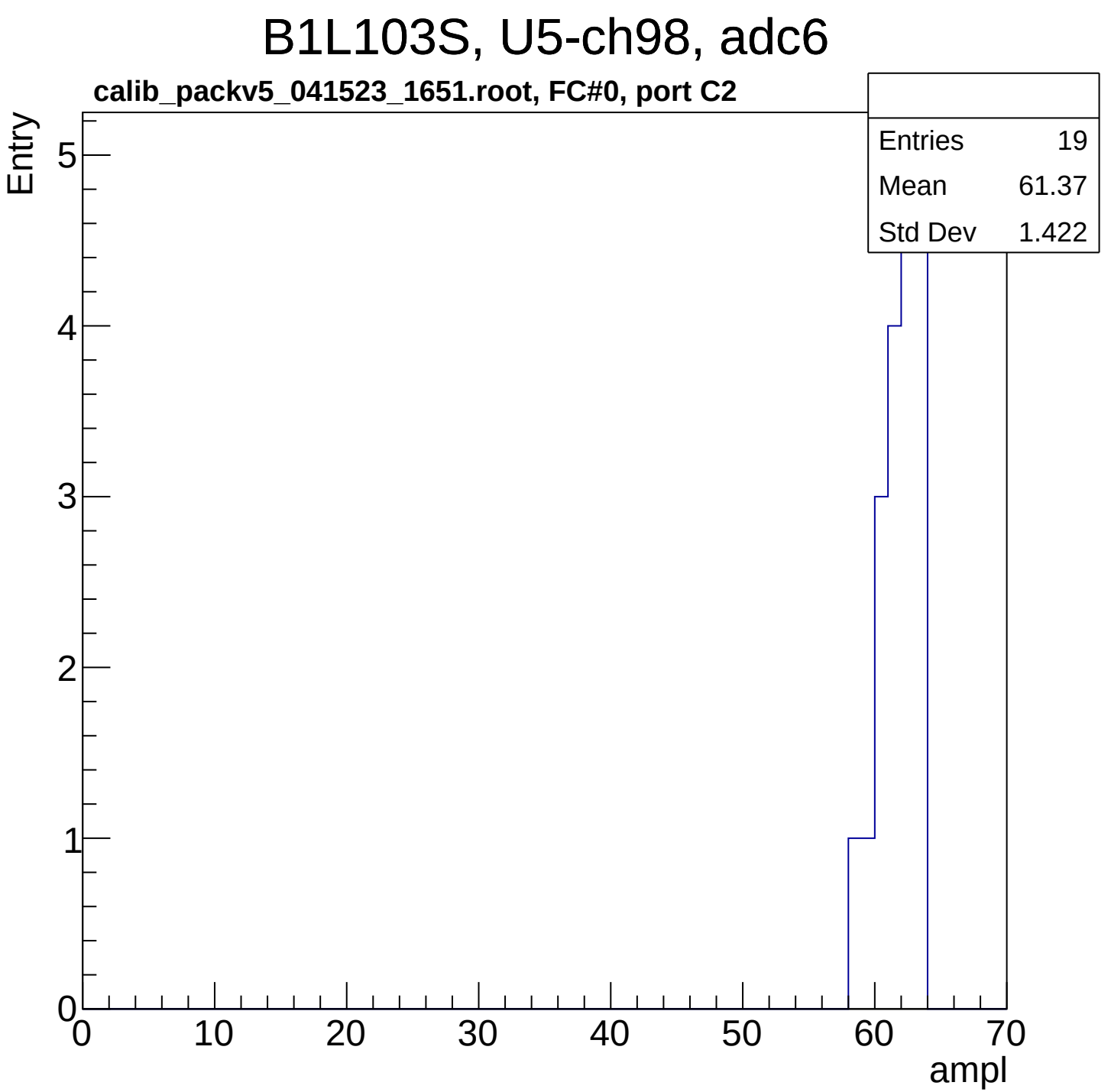
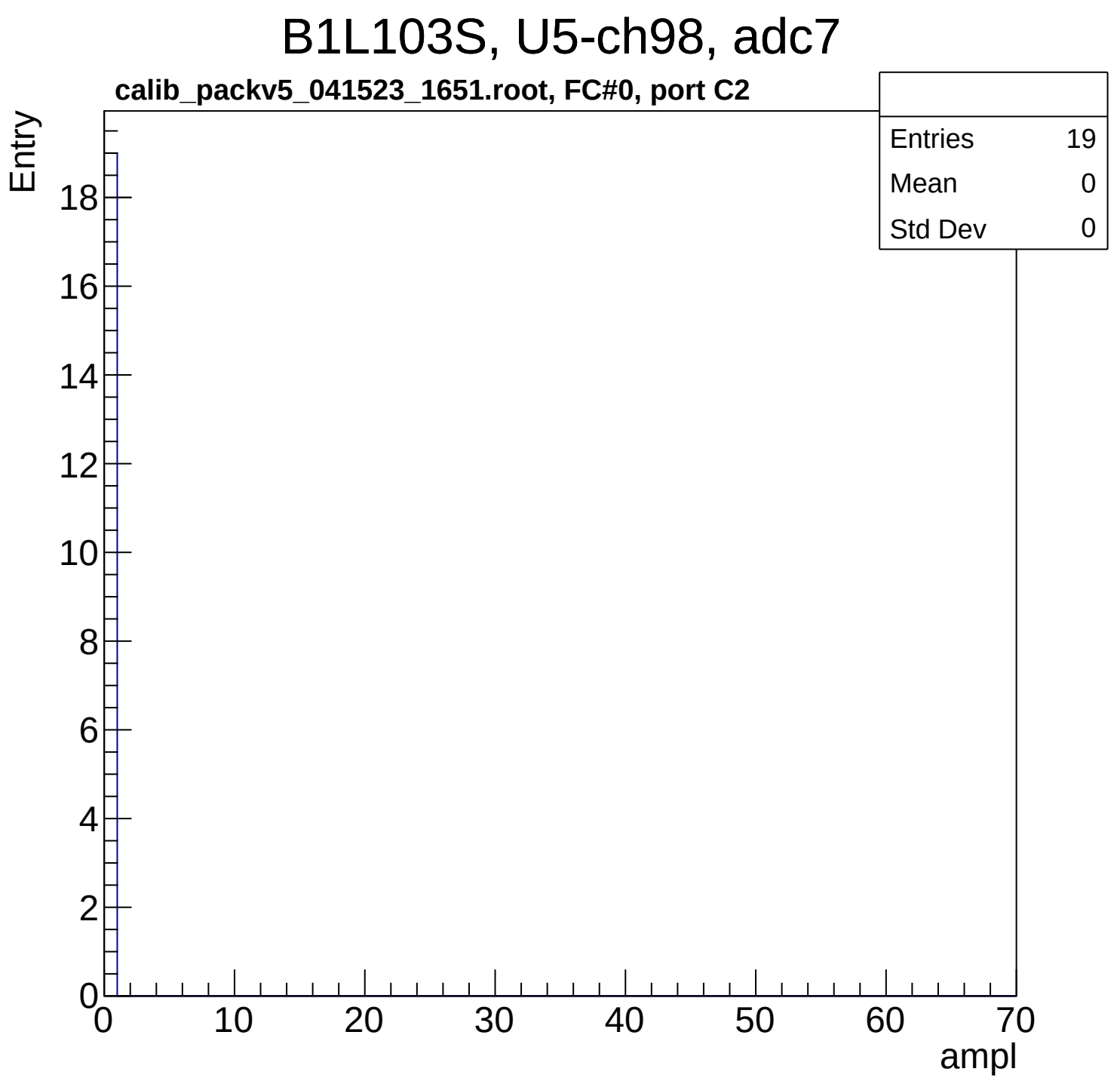

B1L103S, U5-ch98, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 61.37
Std Dev 1.422
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch98, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
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6
8
10
12
14
16
18
0
10
20
30
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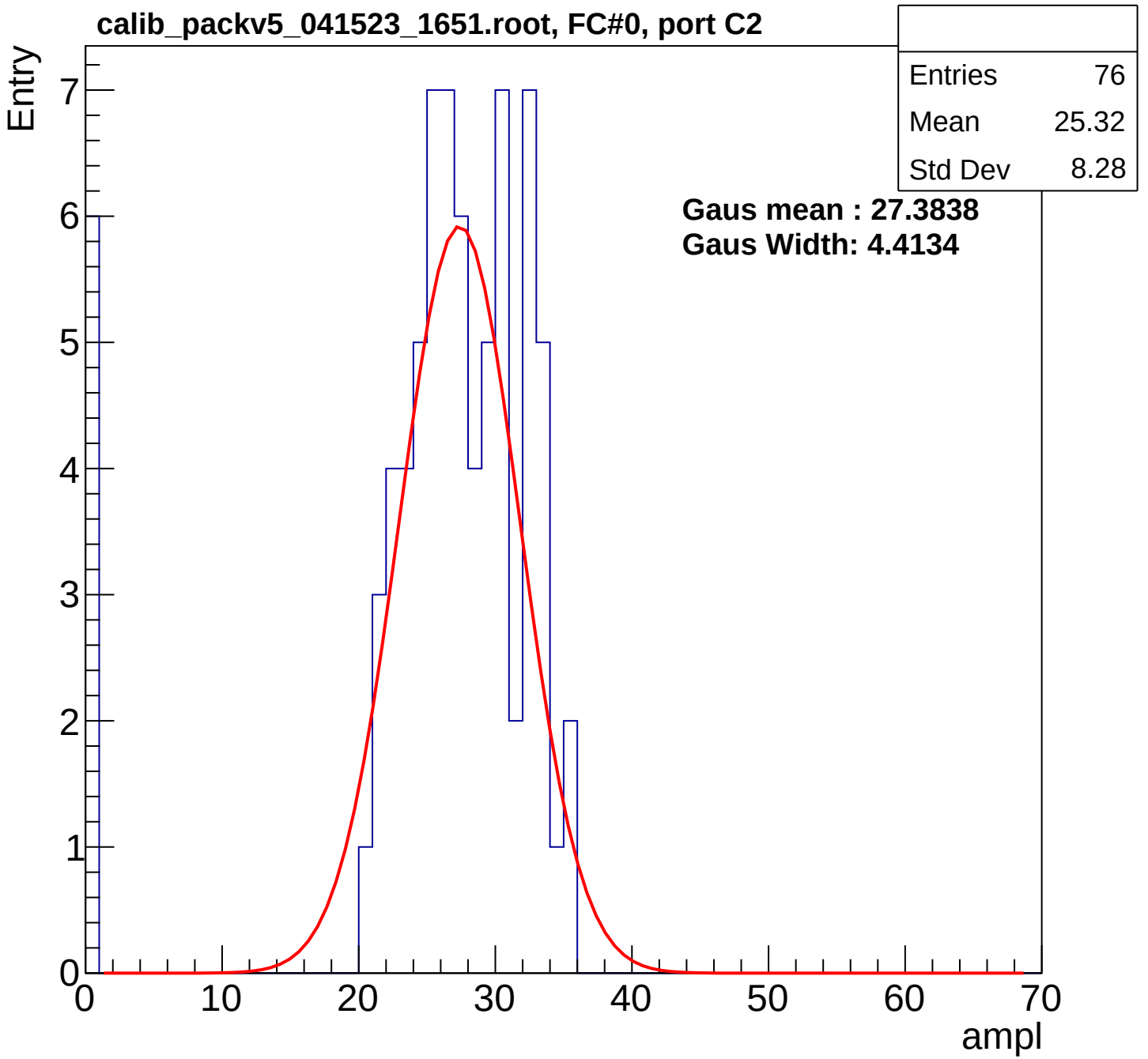
50
60
70
ampl


B1L103S, U5-ch99, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 25.32
Std Dev 8.28
Gaus mean : 27.3838
Gaus Width: 4.4134
Entry
ampl
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4
5
6
7
0
10
20
30
40
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60
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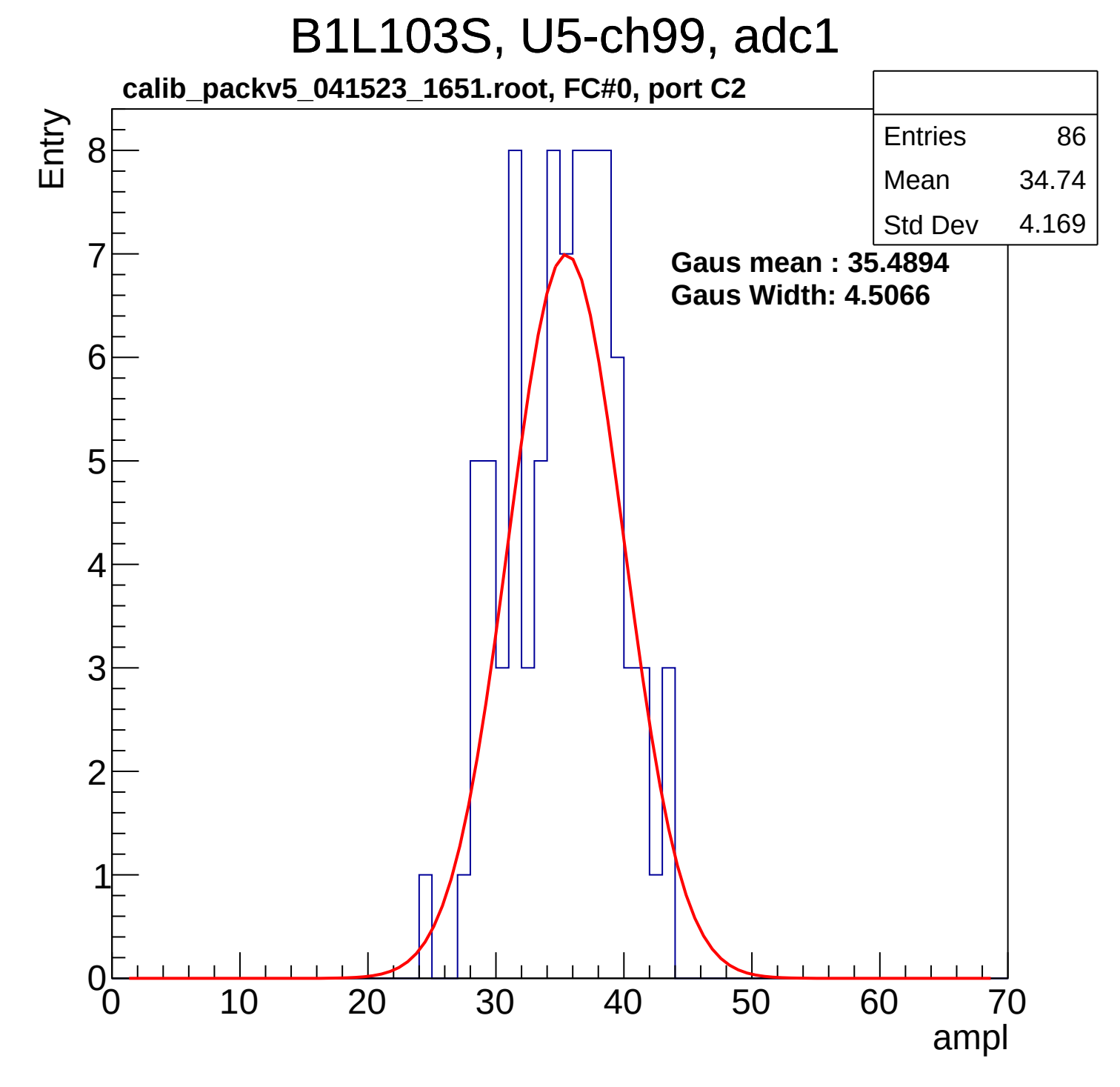
B1L103S, U5-ch99, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 34.74
Std Dev 4.169
Gaus mean : 35.4894
Gaus Width: 4.5066
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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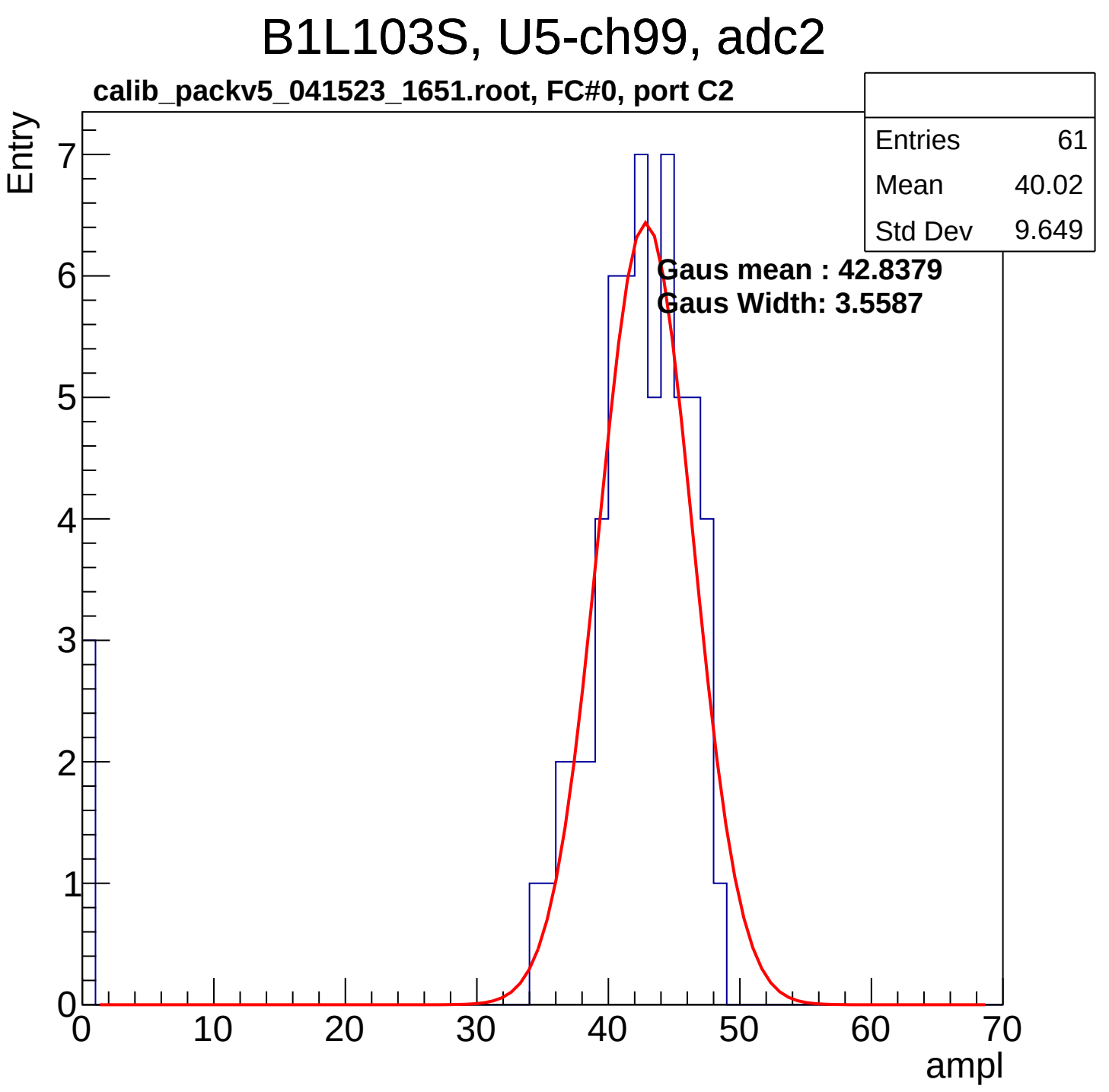
B1L103S, U5-ch99, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 40.02
Std Dev 9.649
Gaus mean : 42.8379
Gaus Width: 3.5587
Entry
ampl
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1
2
3
4
5
6
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0
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20
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60
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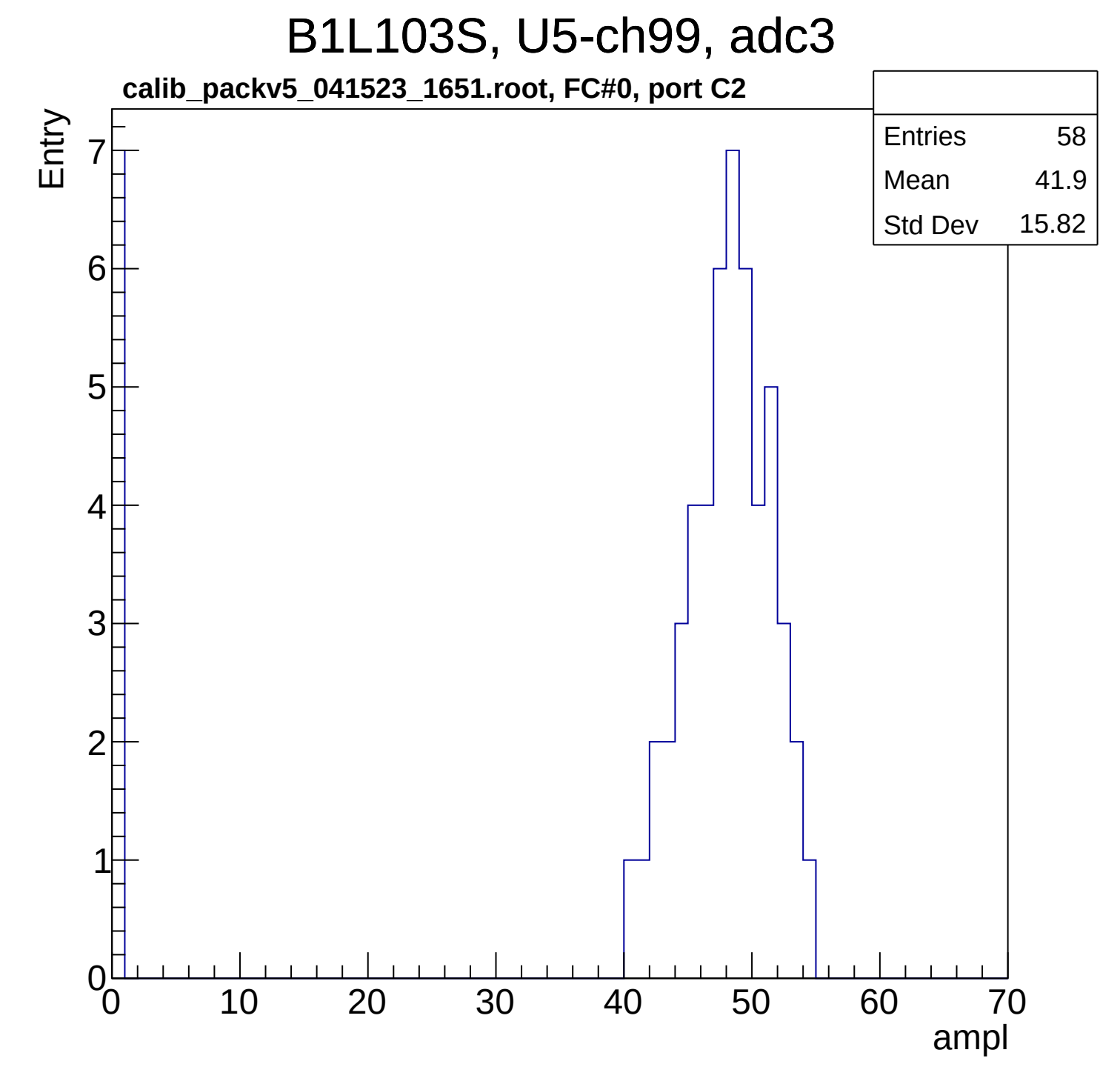
B1L103S, U5-ch99, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 41.9
Std Dev 15.82
Entry
ampl
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1
2
3
4
5
6
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0
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20
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60
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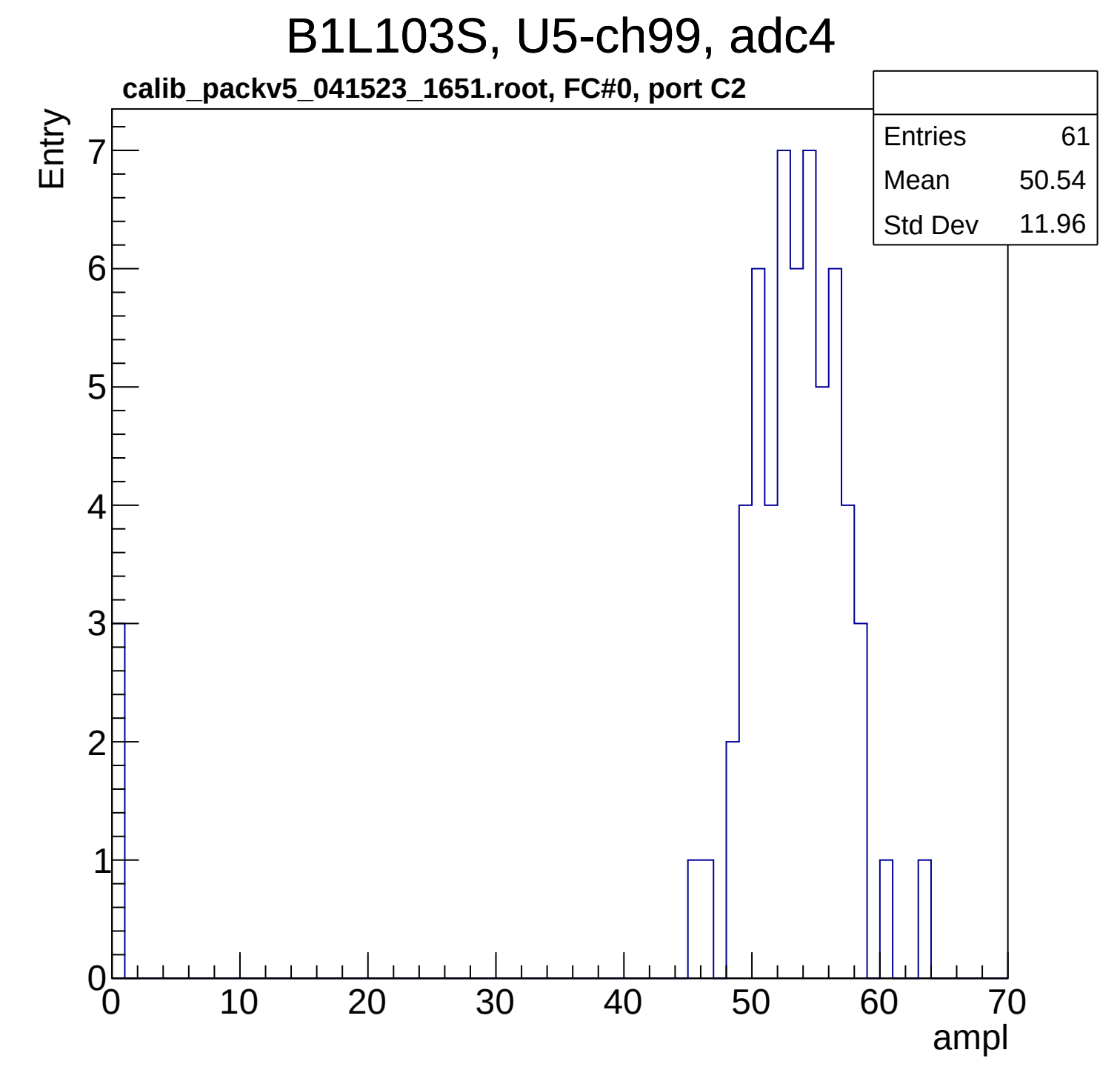
B1L103S, U5-ch99, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 50.54
Std Dev 11.96
Entry
ampl
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4
5
6
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0
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20
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60
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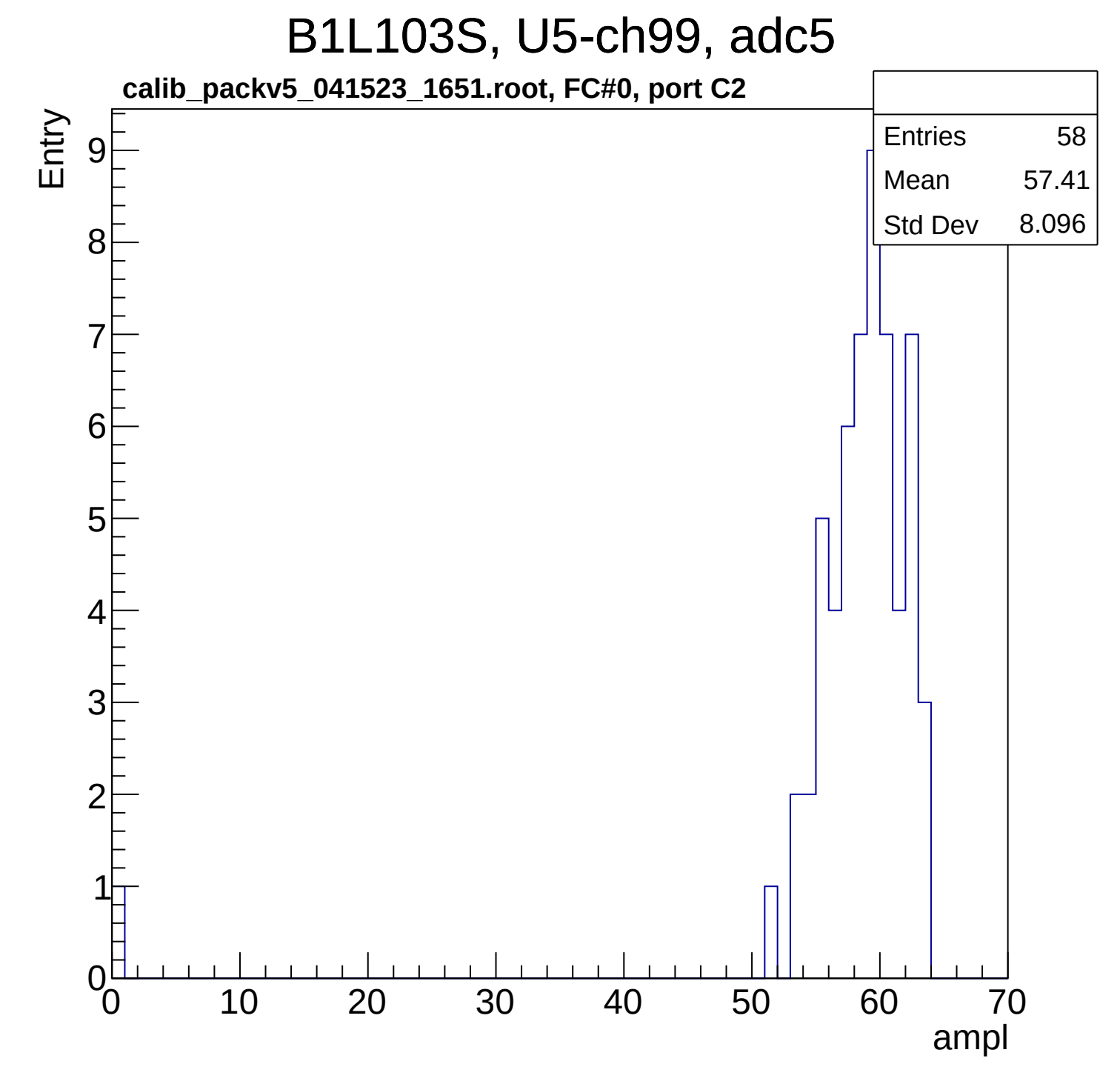
B1L103S, U5-ch99, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 57.41
Std Dev 8.096
Entry
ampl
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6
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0
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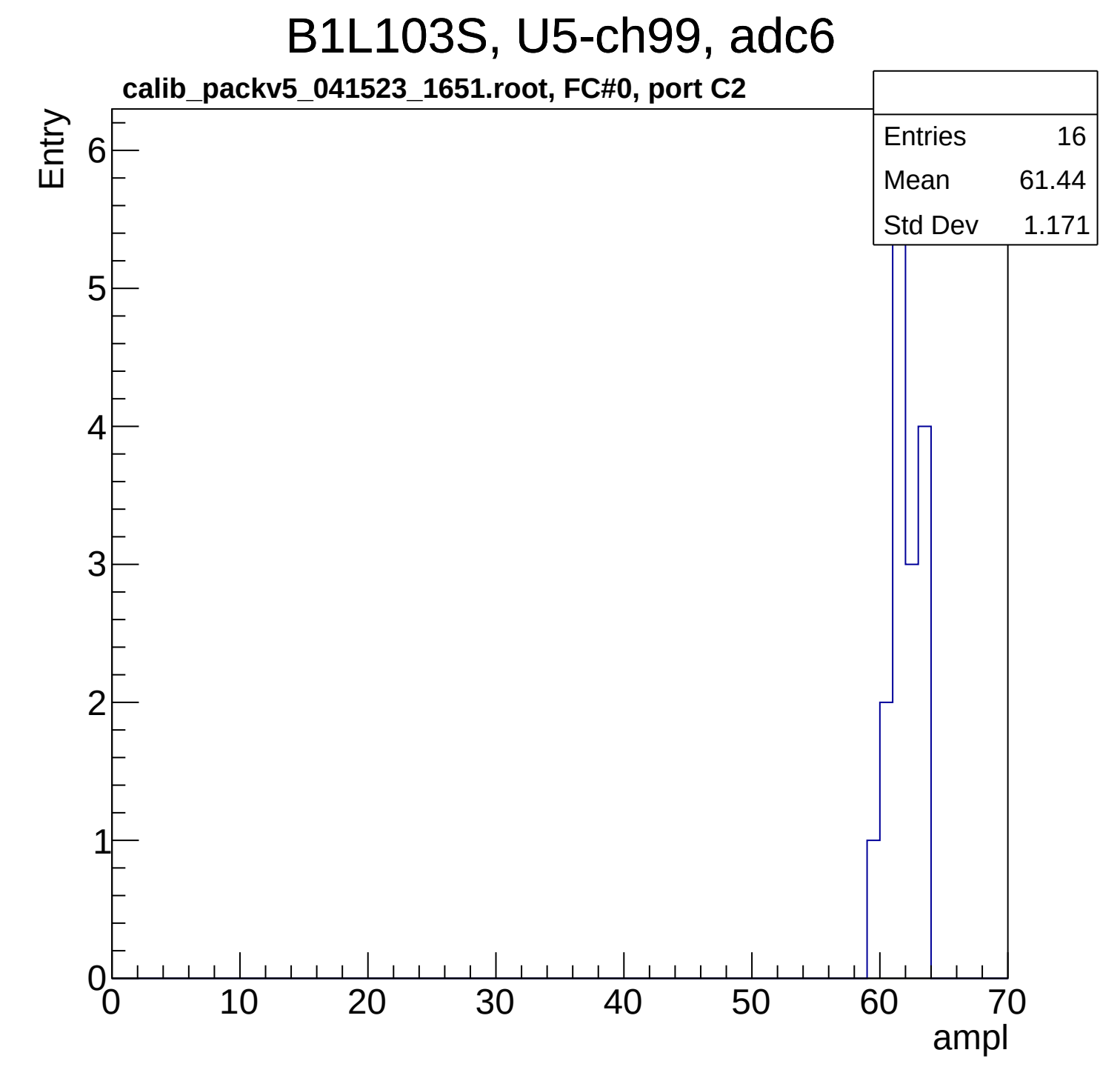
B1L103S, U5-ch99, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 61.44
Std Dev 1.171
Entry
ampl
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0
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40
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60
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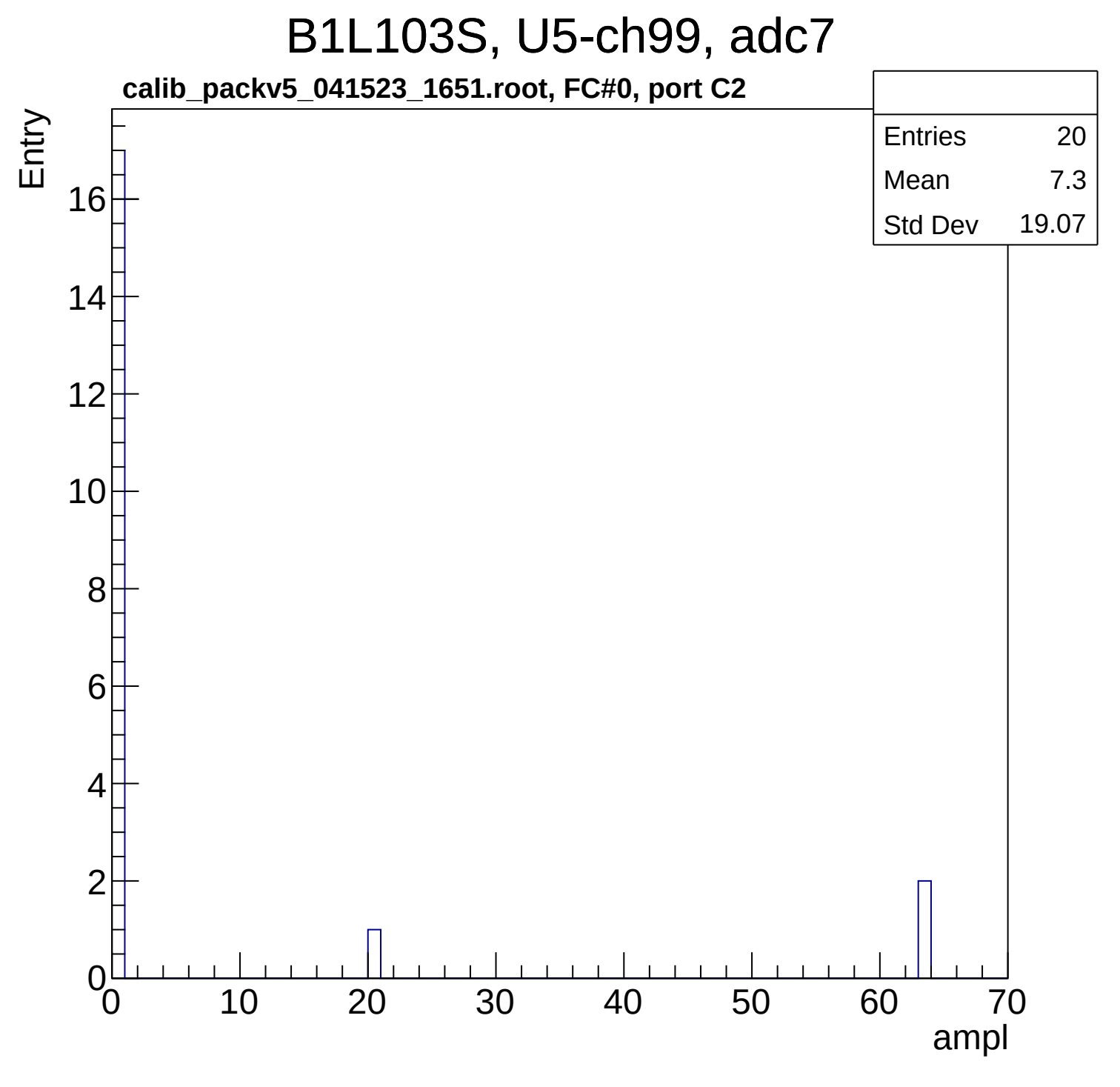
B1L103S, U5-ch99, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 7.3
Std Dev 19.07
Entry
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8
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16
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10
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30
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50
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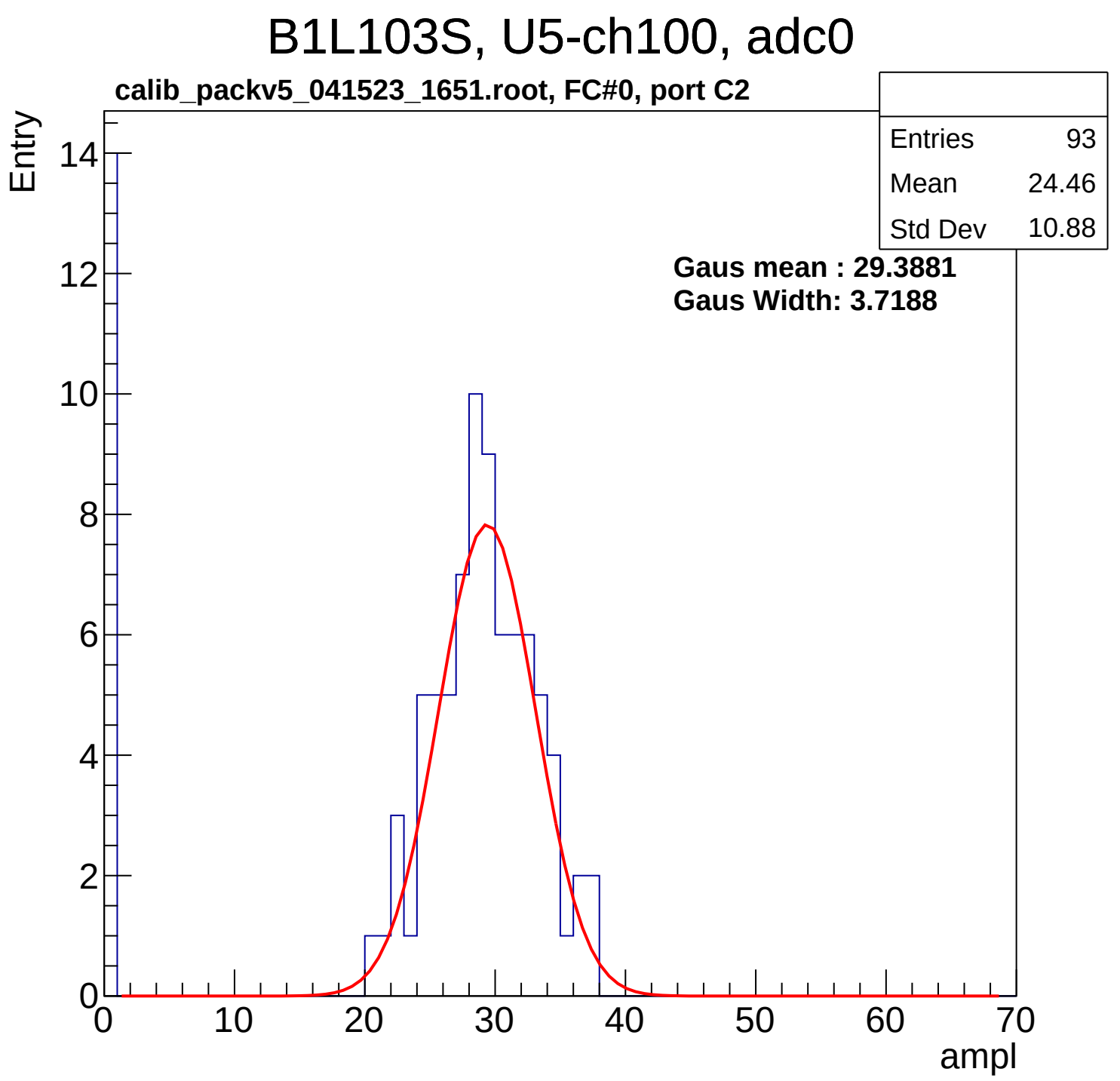
70
ampl


B1L103S, U5-ch100, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 24.46
Std Dev 10.88
Gaus mean : 29.3881
Gaus Width: 3.7188
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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60
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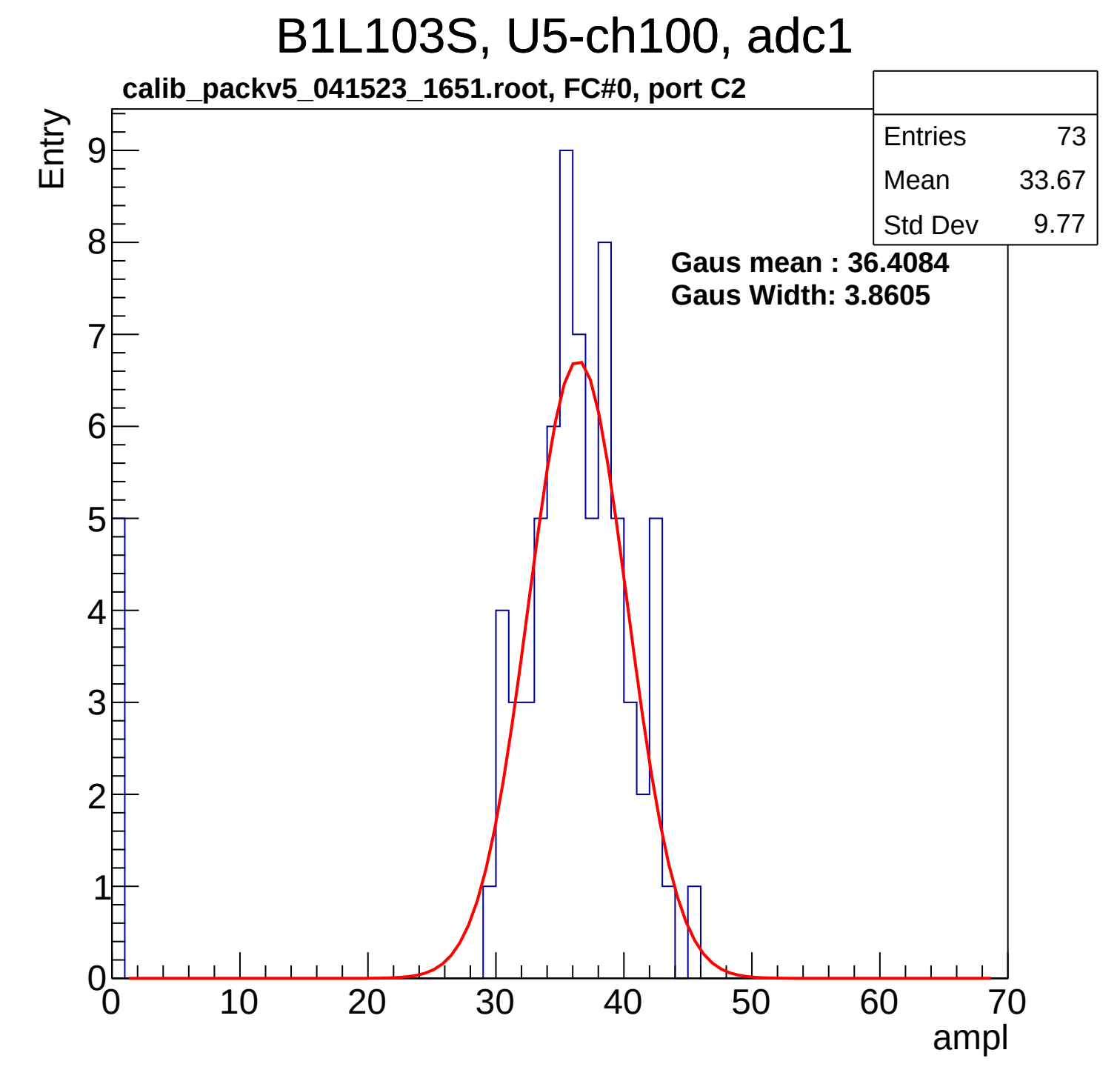
B1L103S, U5-ch100, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 33.67
Std Dev 9.77
Gaus mean : 36.4084
Gaus Width: 3.8605
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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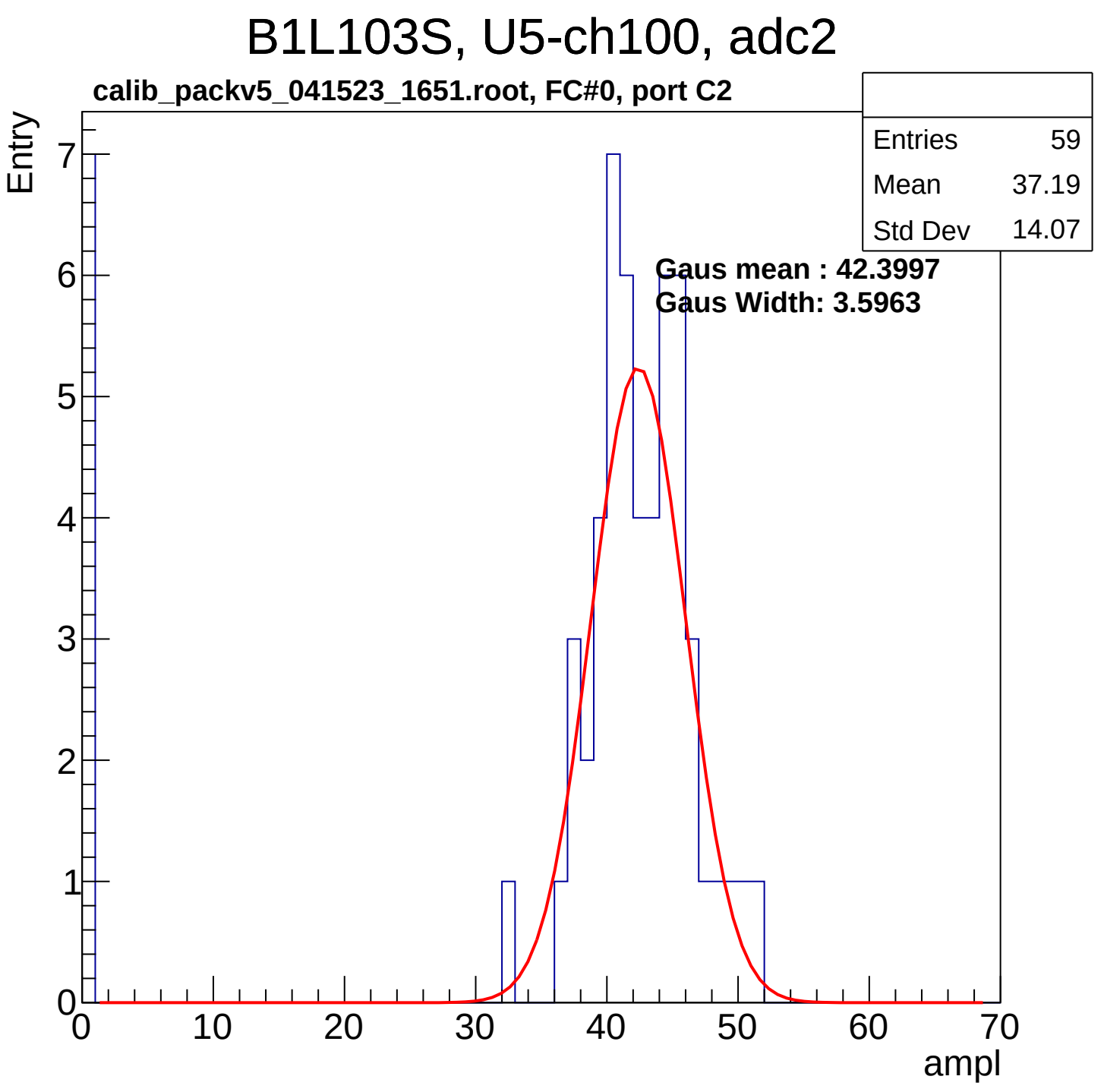
B1L103S, U5-ch100, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 37.19
Std Dev 14.07
Gaus mean : 42.3997
Gaus Width: 3.5963
Entry
ampl
0
1
2
3
4
5
6
7
0
10
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60
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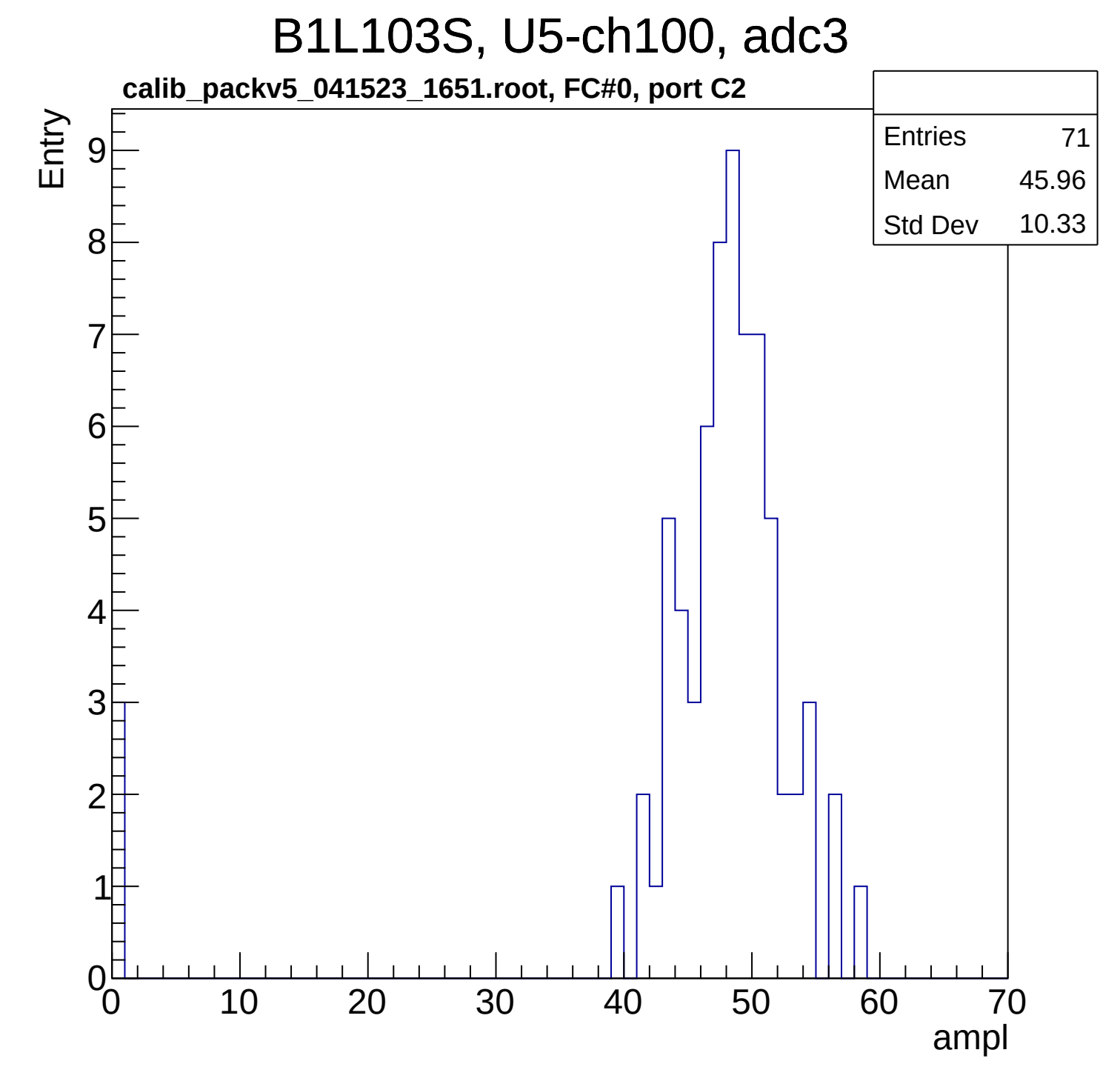
B1L103S, U5-ch100, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 45.96
Std Dev 10.33
Entry
ampl
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3
4
5
6
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8
9
0
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20
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40
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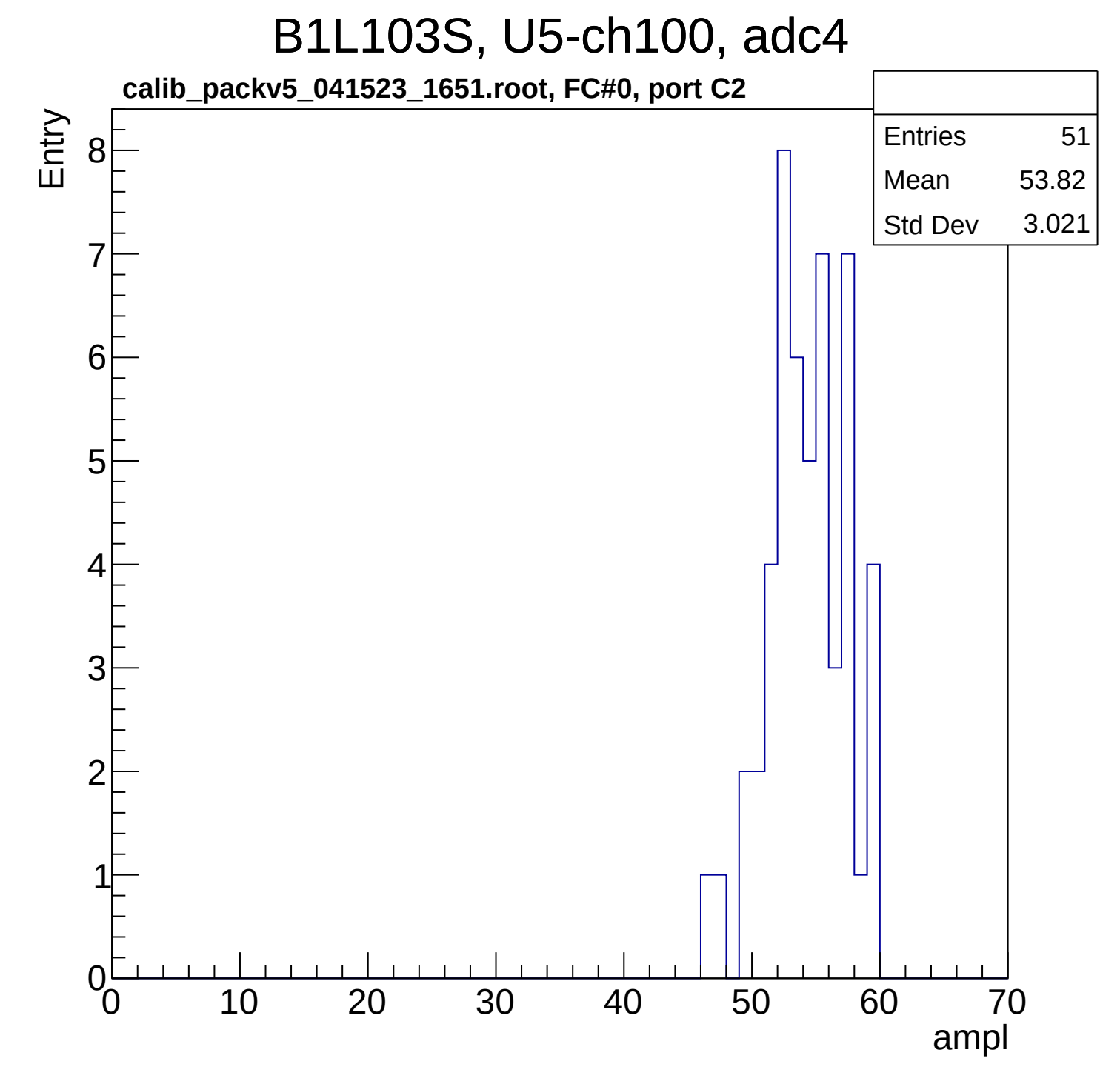
B1L103S, U5-ch100, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 53.82
Std Dev 3.021
Entry
ampl
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2
3
4
5
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7
8
0
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20
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40
50
60
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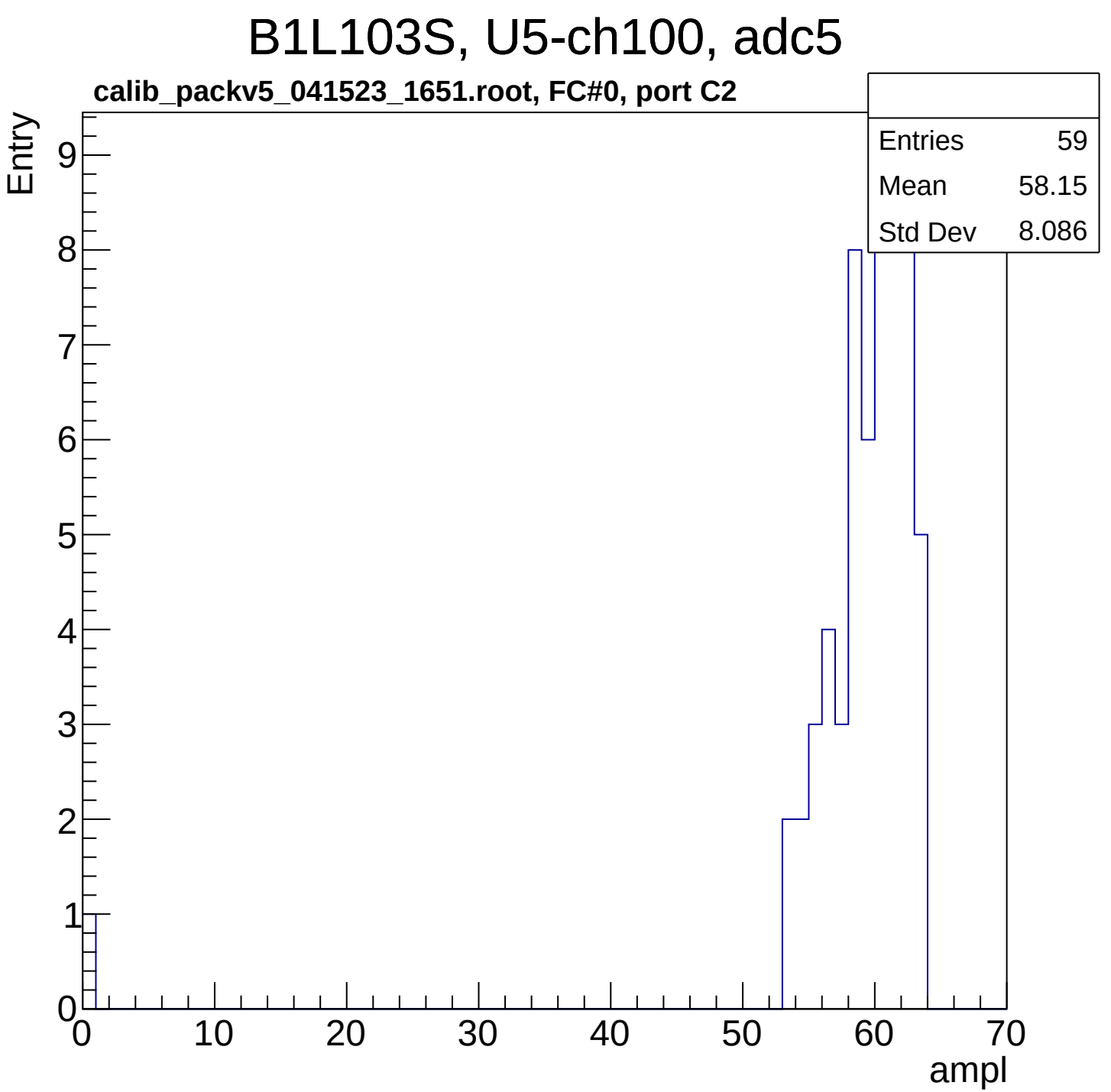
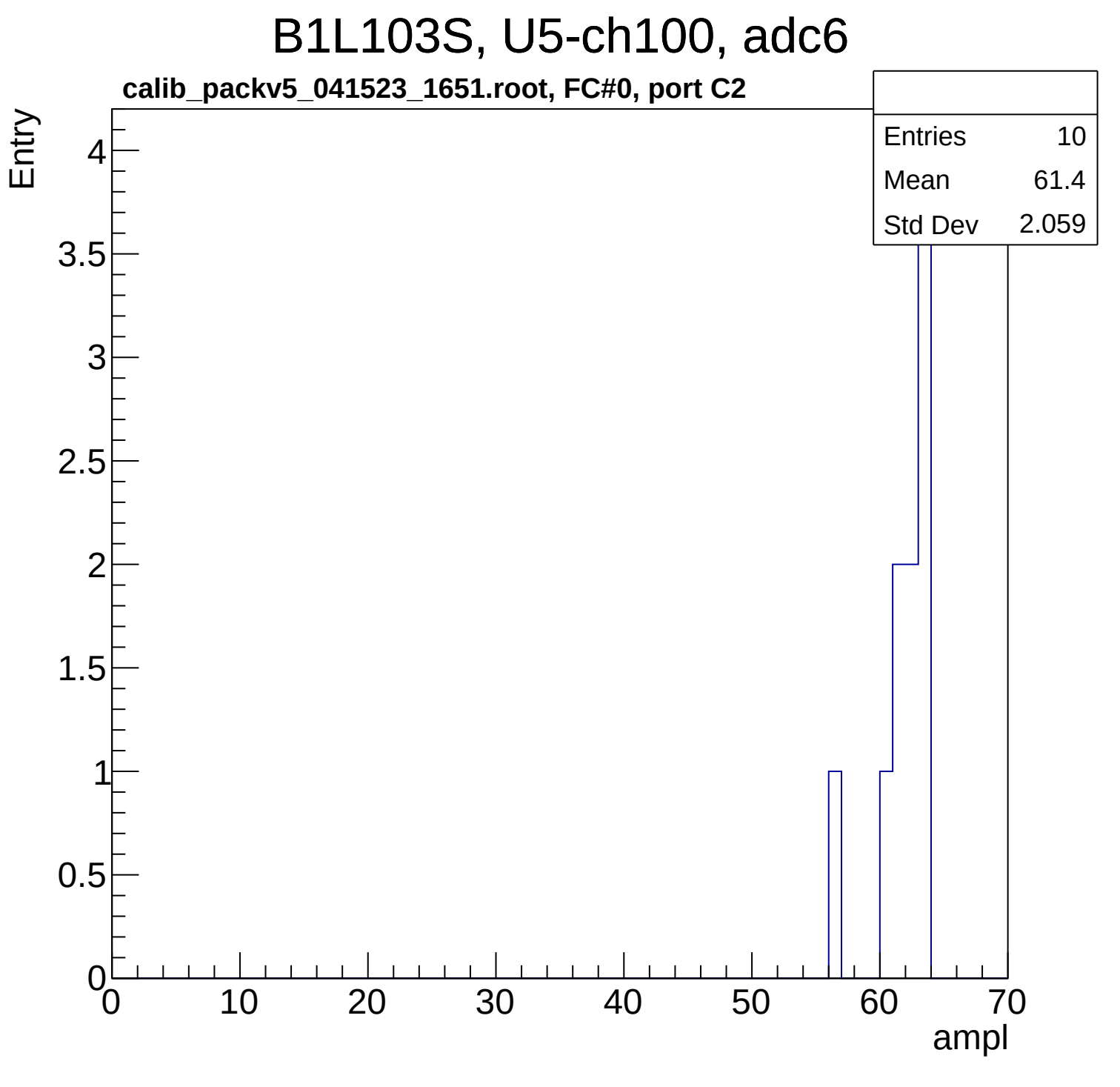

B1L103S, U5-ch100, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 58.15
Std Dev 8.086
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U5-ch100, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.4
Std Dev 2.059
Entry
ampl
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2
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3
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0
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60
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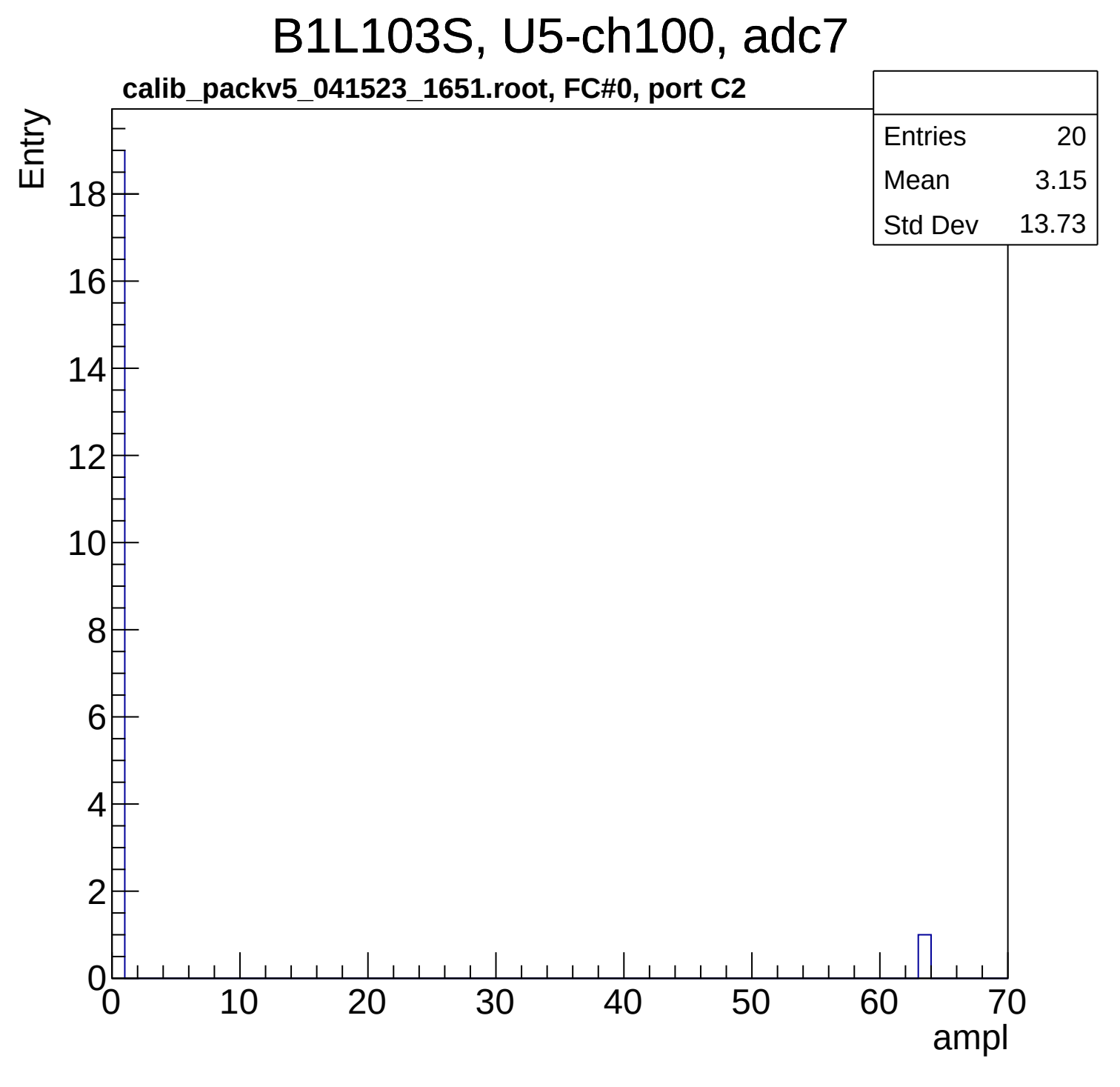
B1L103S, U5-ch100, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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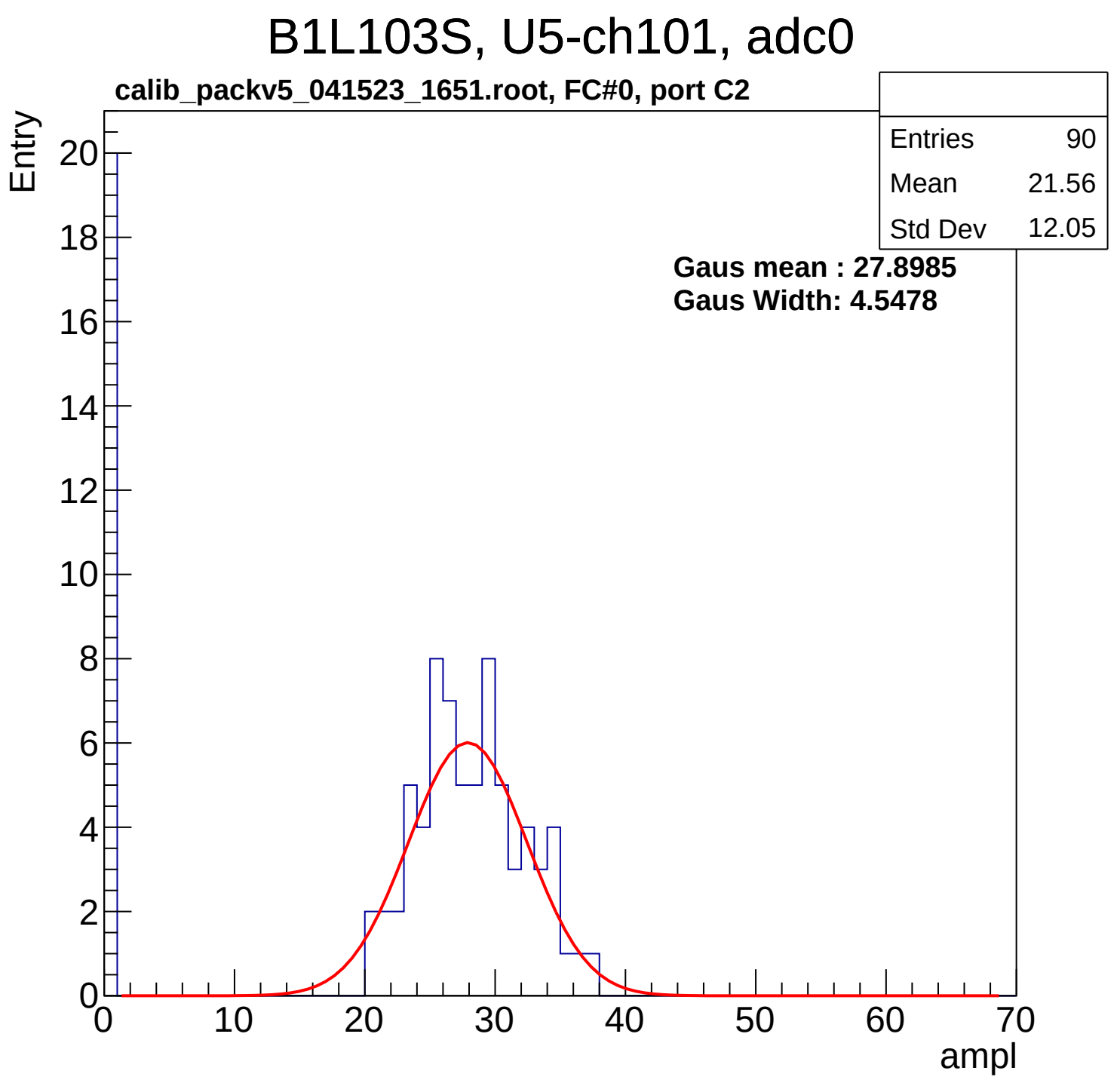
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch101, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 21.56
Std Dev 12.05
Gaus mean : 27.8985
Gaus Width: 4.5478
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
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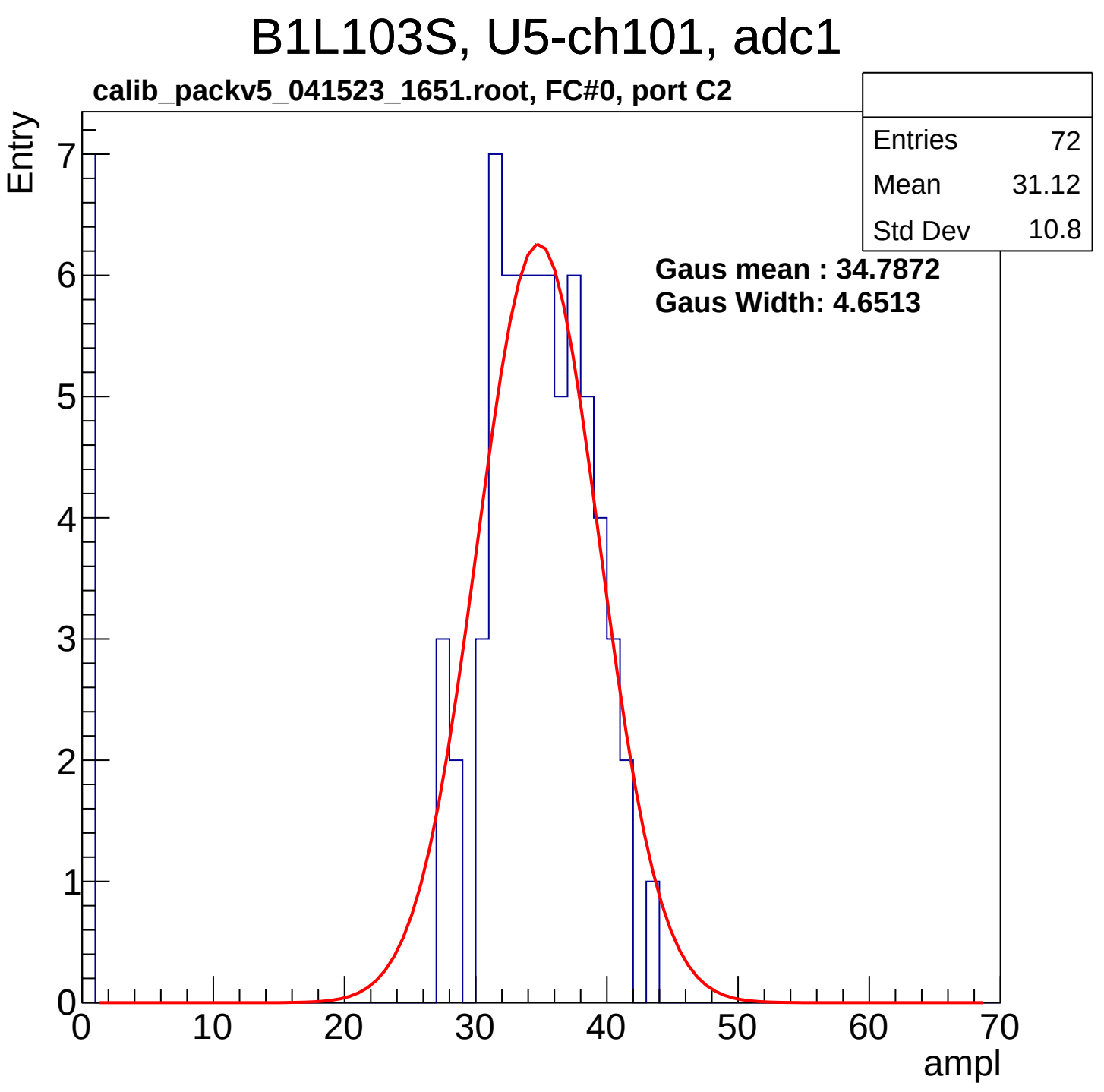
B1L103S, U5-ch101, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 31.12
Std Dev 10.8
Gaus mean : 34.7872
Gaus Width: 4.6513
Entry
ampl
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1
2
3
4
5
6
7
0
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30
40
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60
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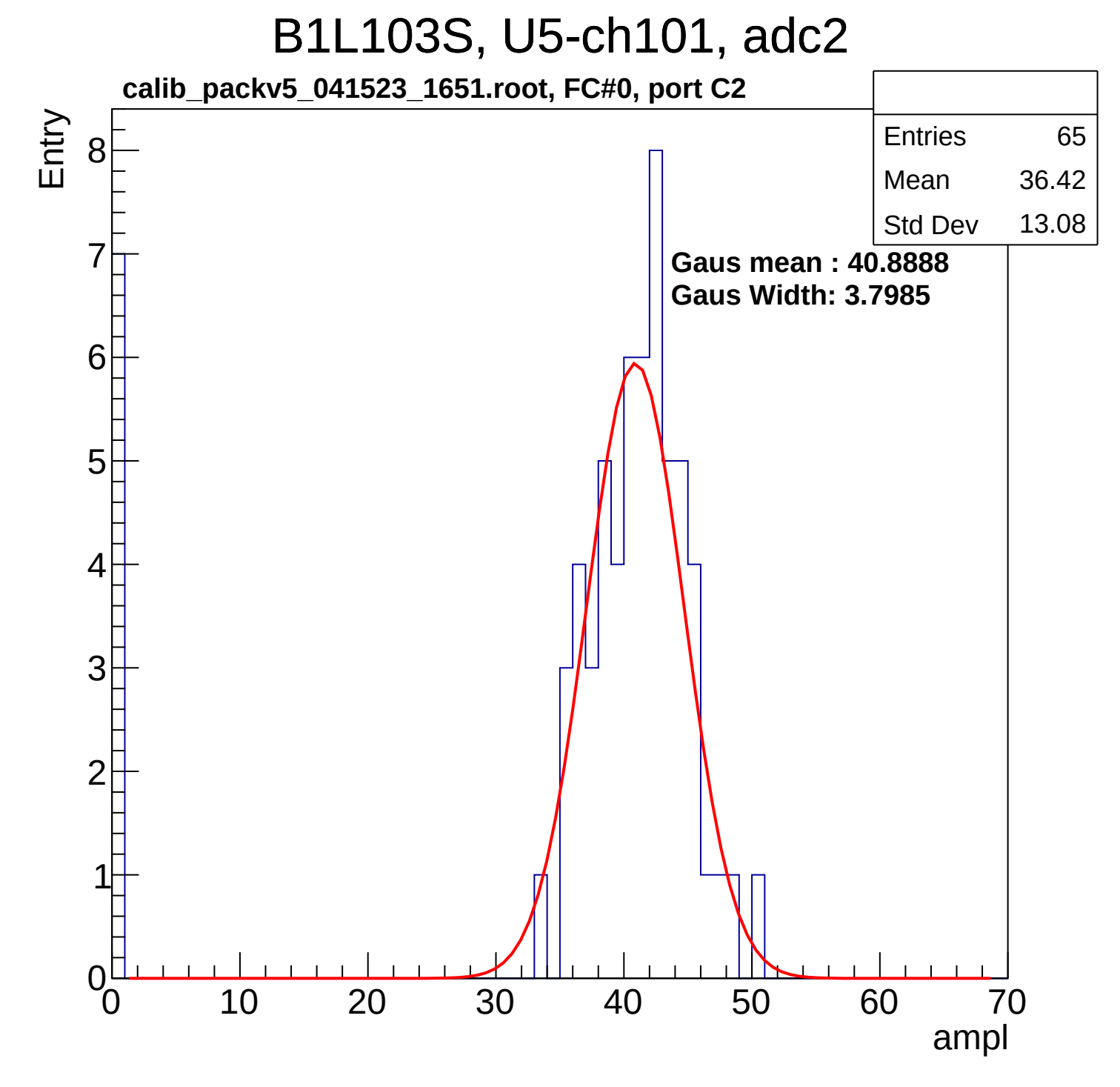
B1L103S, U5-ch101, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 36.42
Std Dev 13.08
Gaus mean : 40.8888
Gaus Width: 3.7985
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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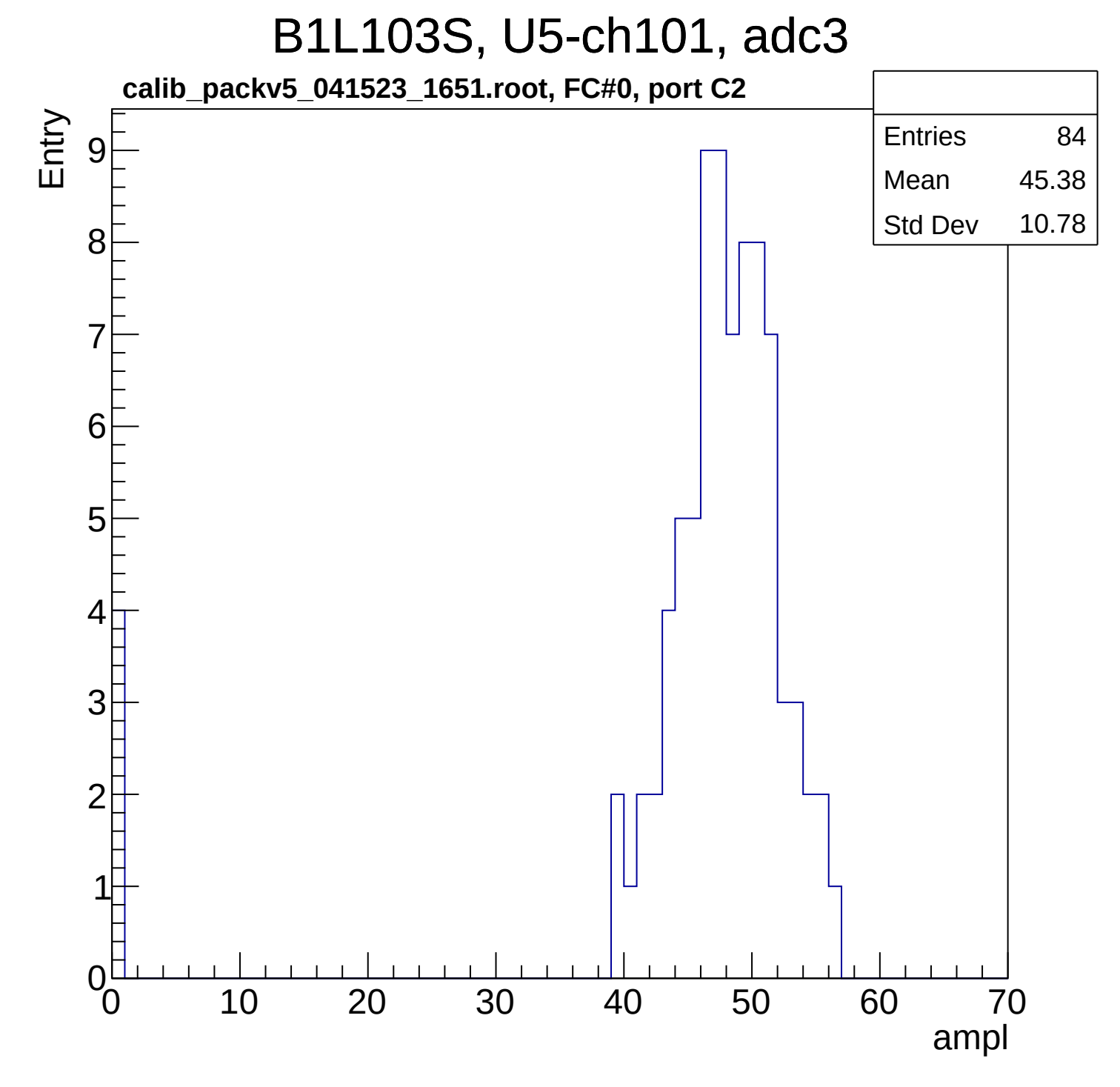
B1L103S, U5-ch101, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 45.38
Std Dev 10.78
Entry
ampl
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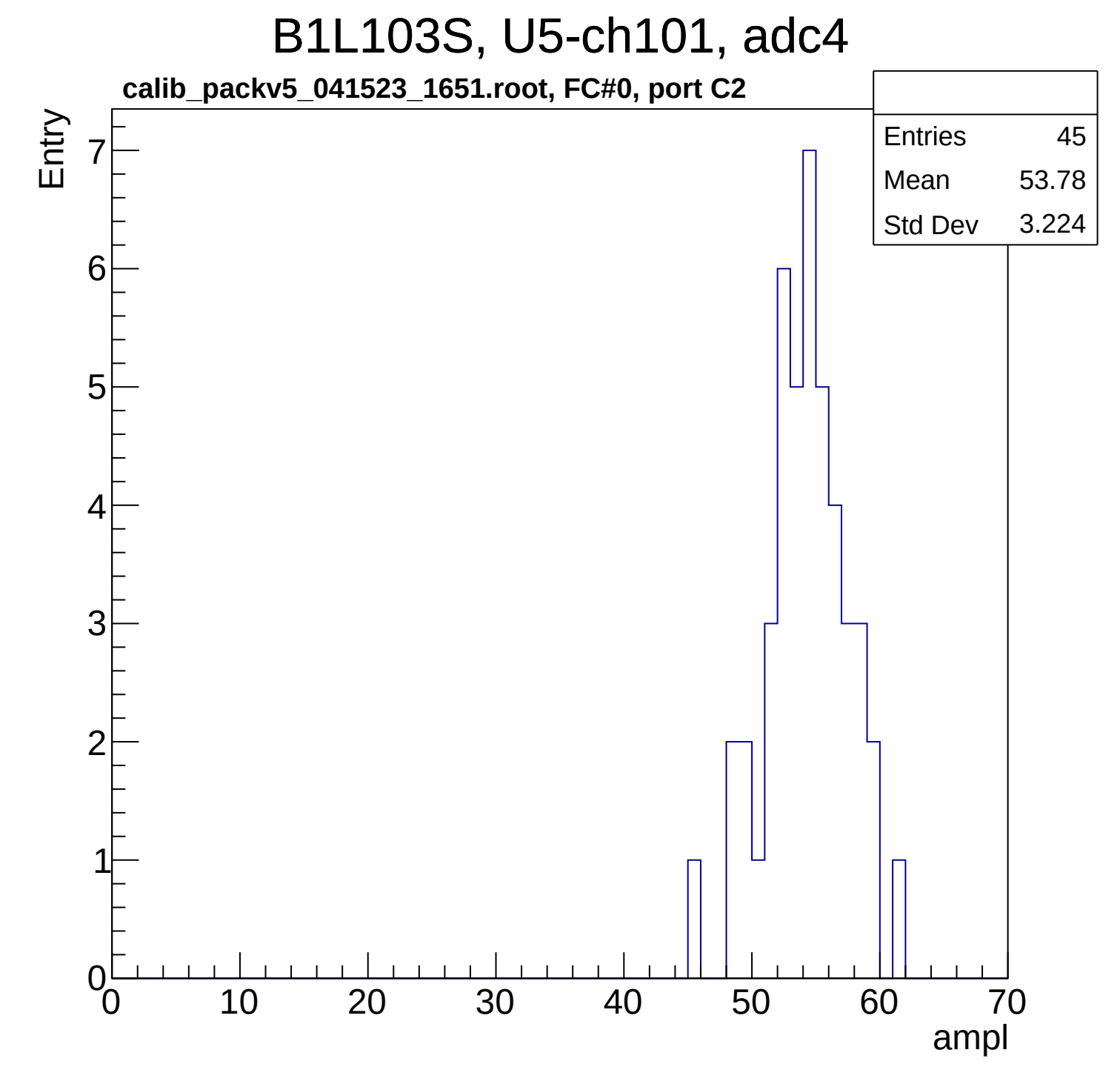
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U5-ch101, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 53.78
Std Dev 3.224
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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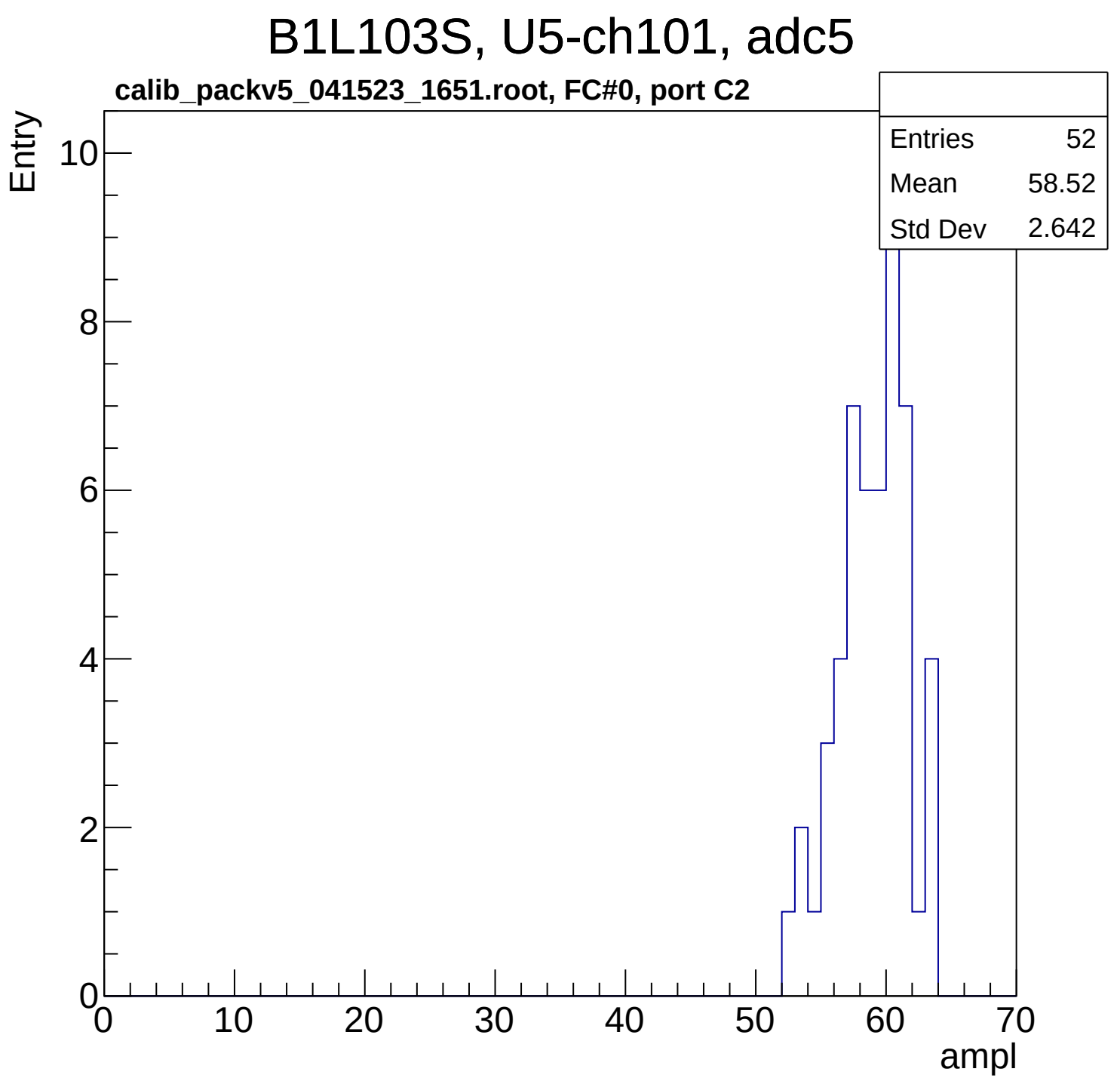
B1L103S, U5-ch101, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.52
Std Dev 2.642
Entry
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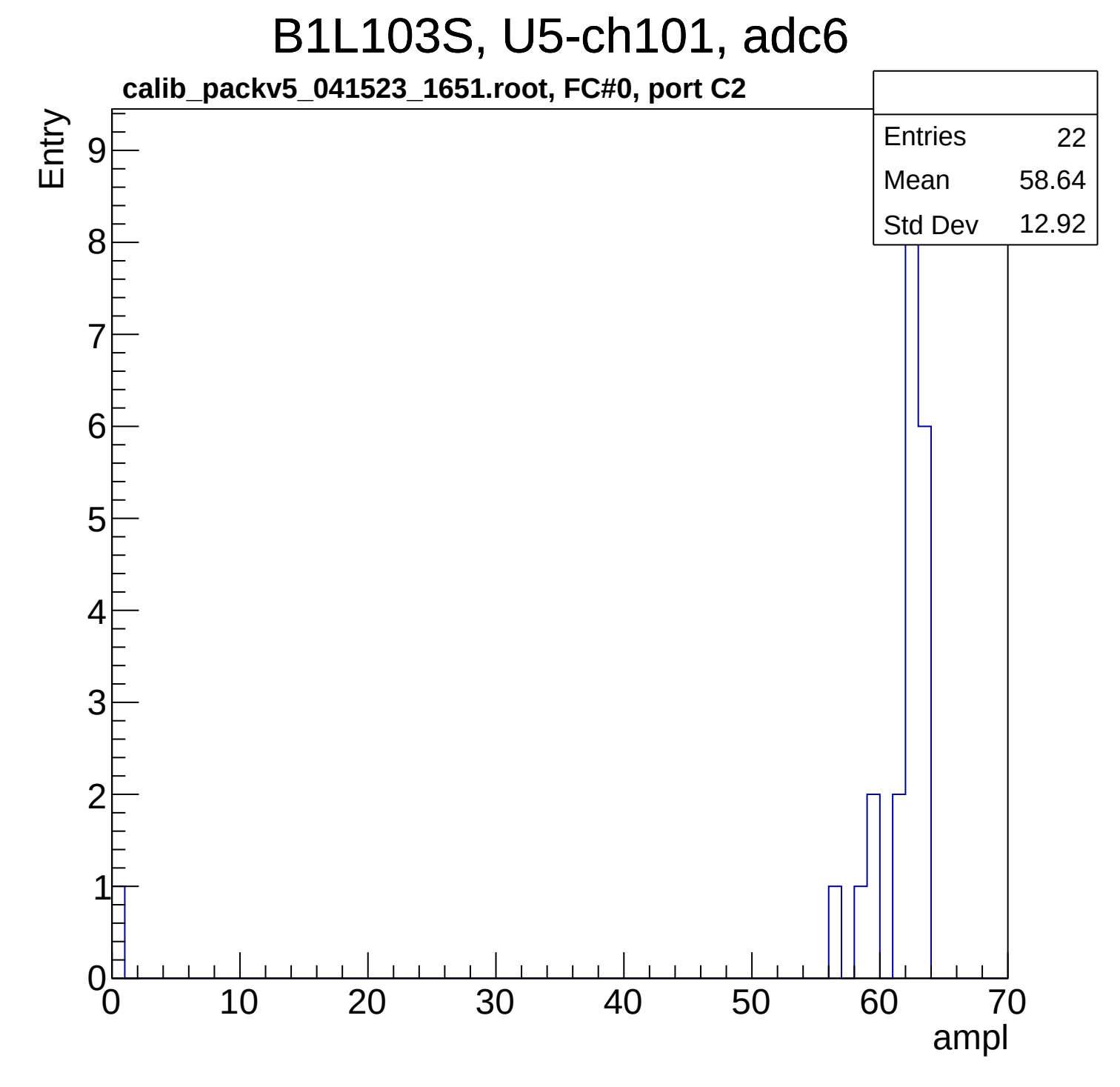
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch101, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.64
Std Dev 12.92
Entry
ampl
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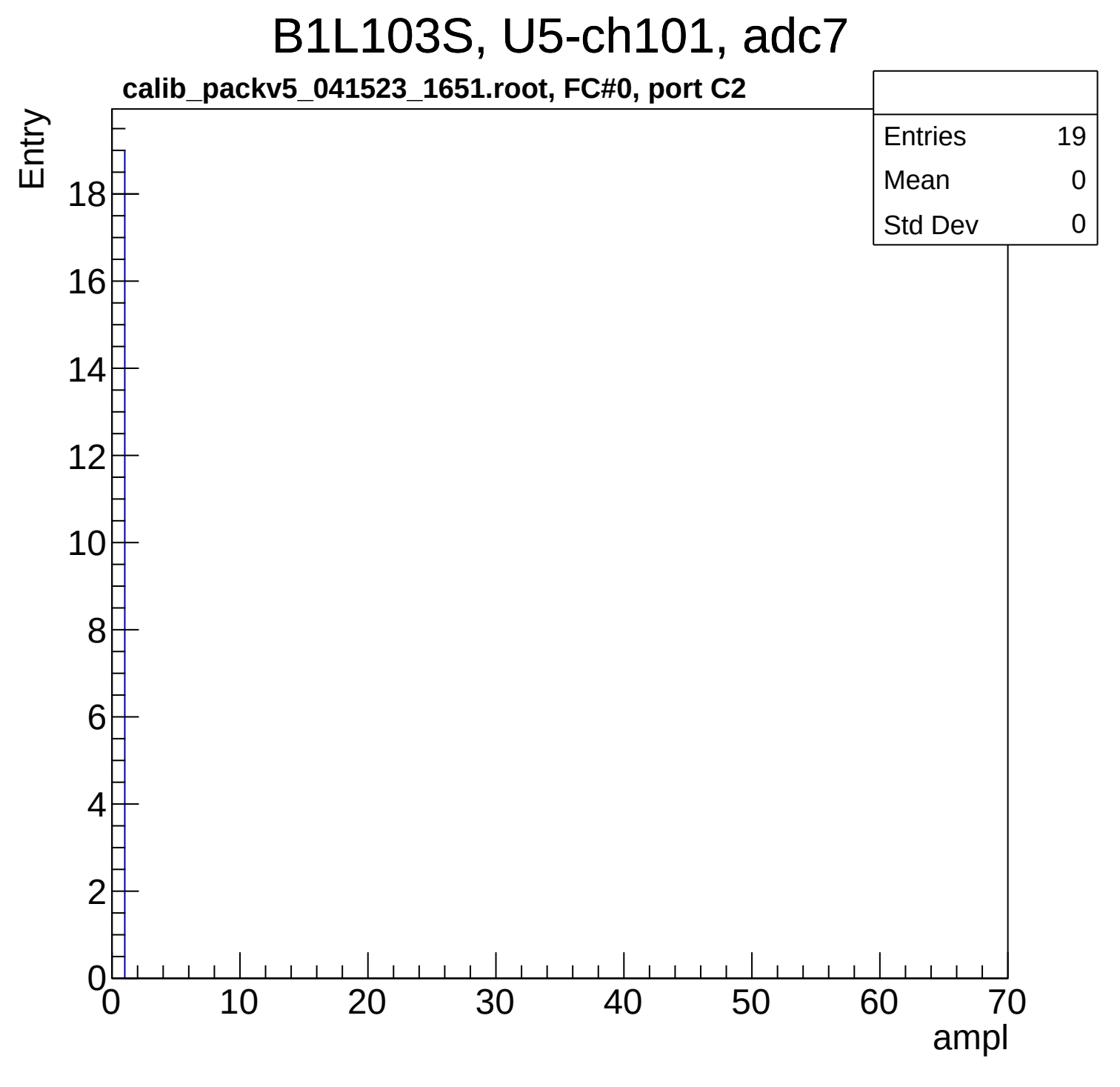
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U5-ch101, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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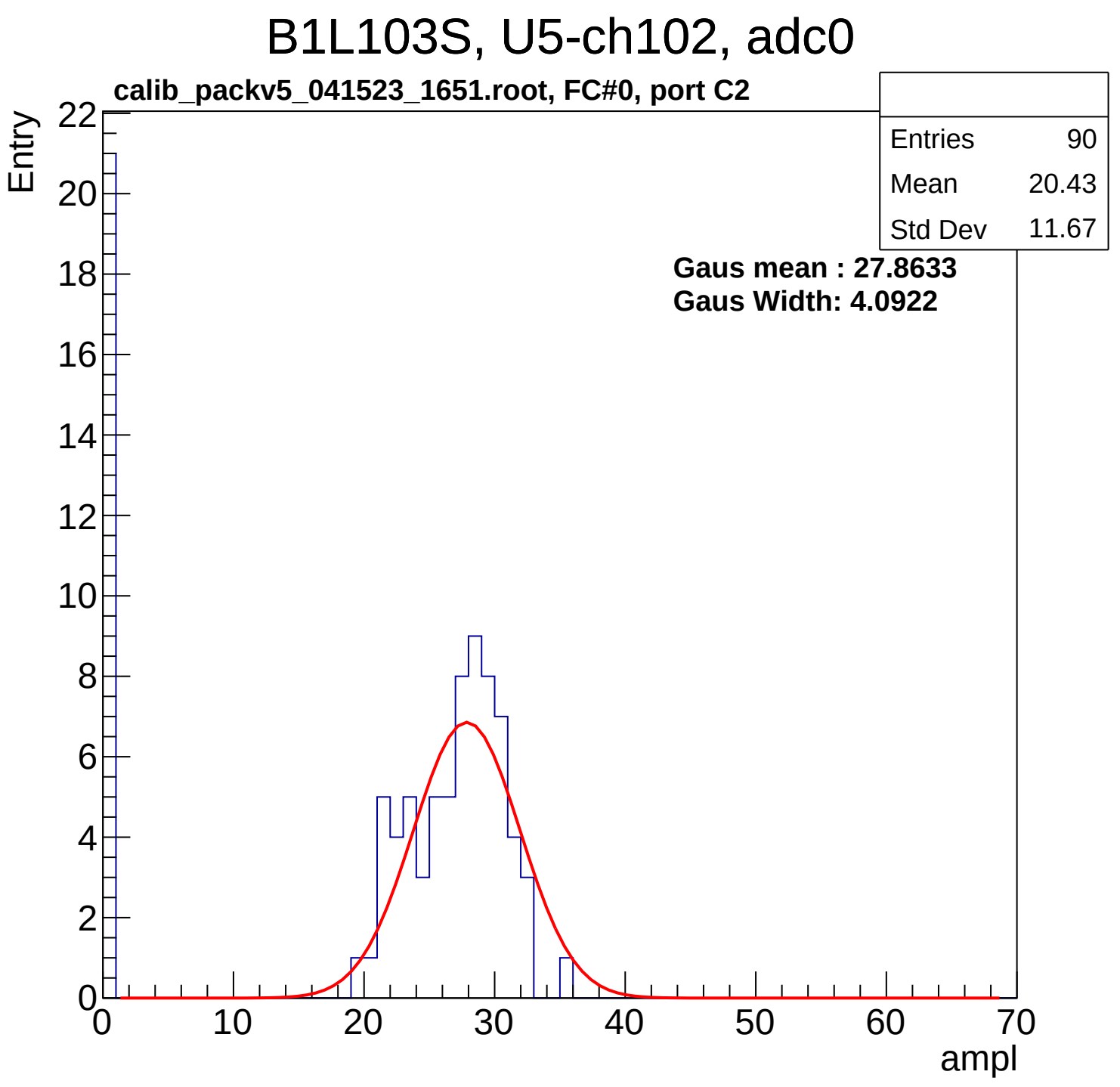
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch102, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 20.43
Std Dev 11.67
Gaus mean : 27.8633
Gaus Width: 4.0922
Entry
ampl
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2
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6
8
10
12
14
16
18
20
22
0
10
20
30
40
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60
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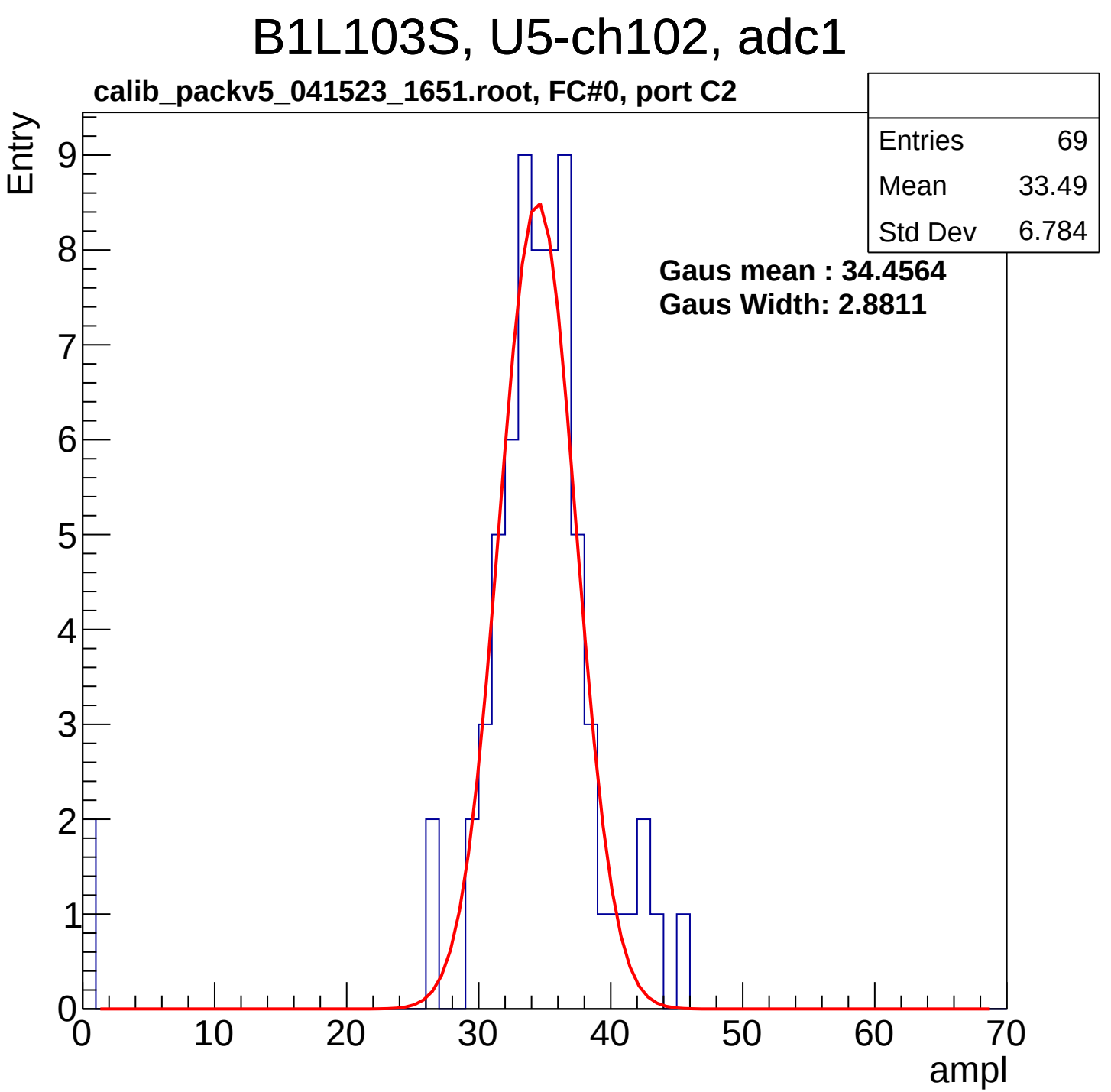
B1L103S, U5-ch102, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 33.49
Std Dev 6.784
Gaus mean : 34.4564
Gaus Width: 2.8811
Entry
ampl
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2
3
4
5
6
7
8
9
0
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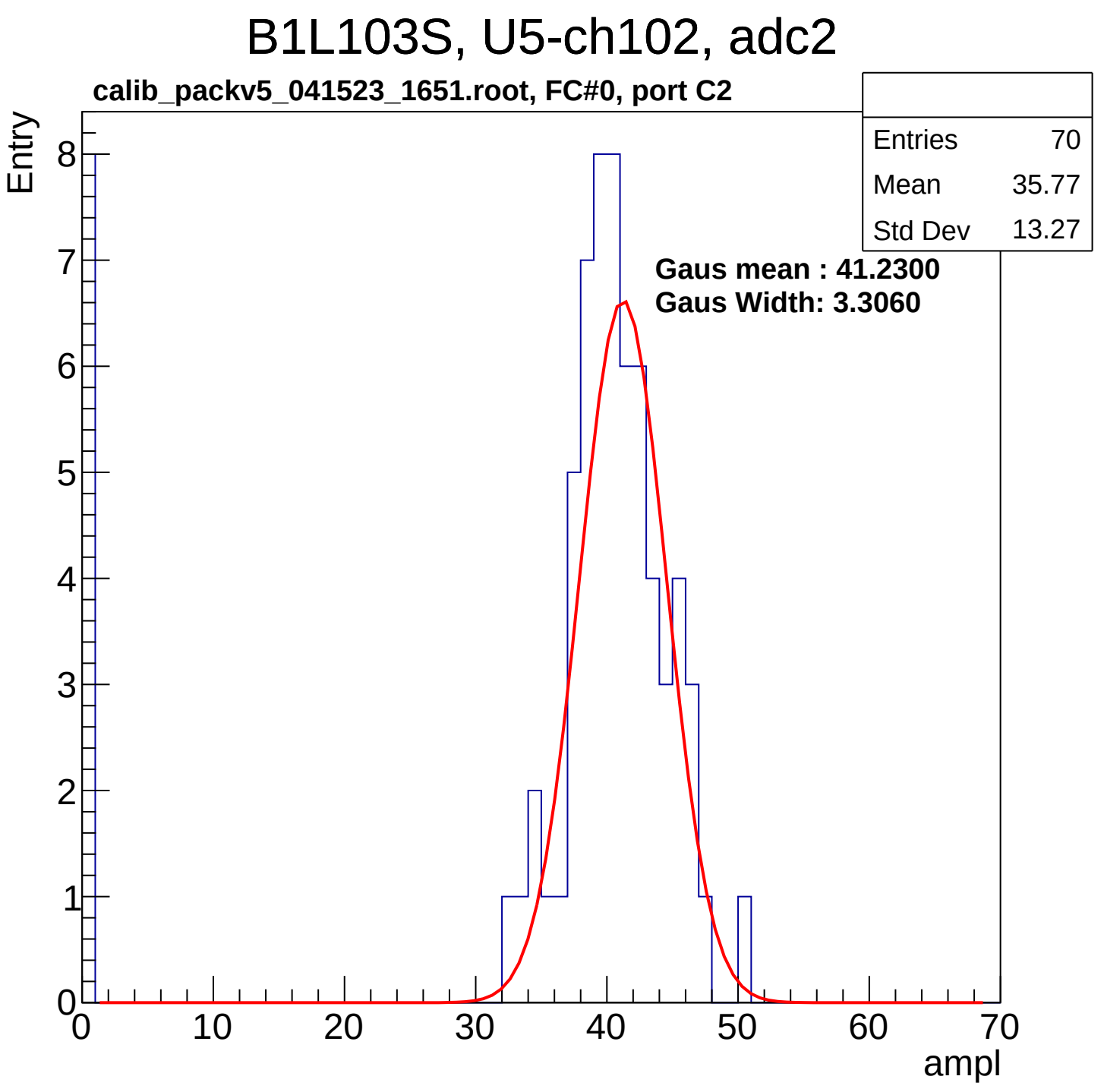
B1L103S, U5-ch102, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 35.77
Std Dev 13.27
Gaus mean : 41.2300
Gaus Width: 3.3060
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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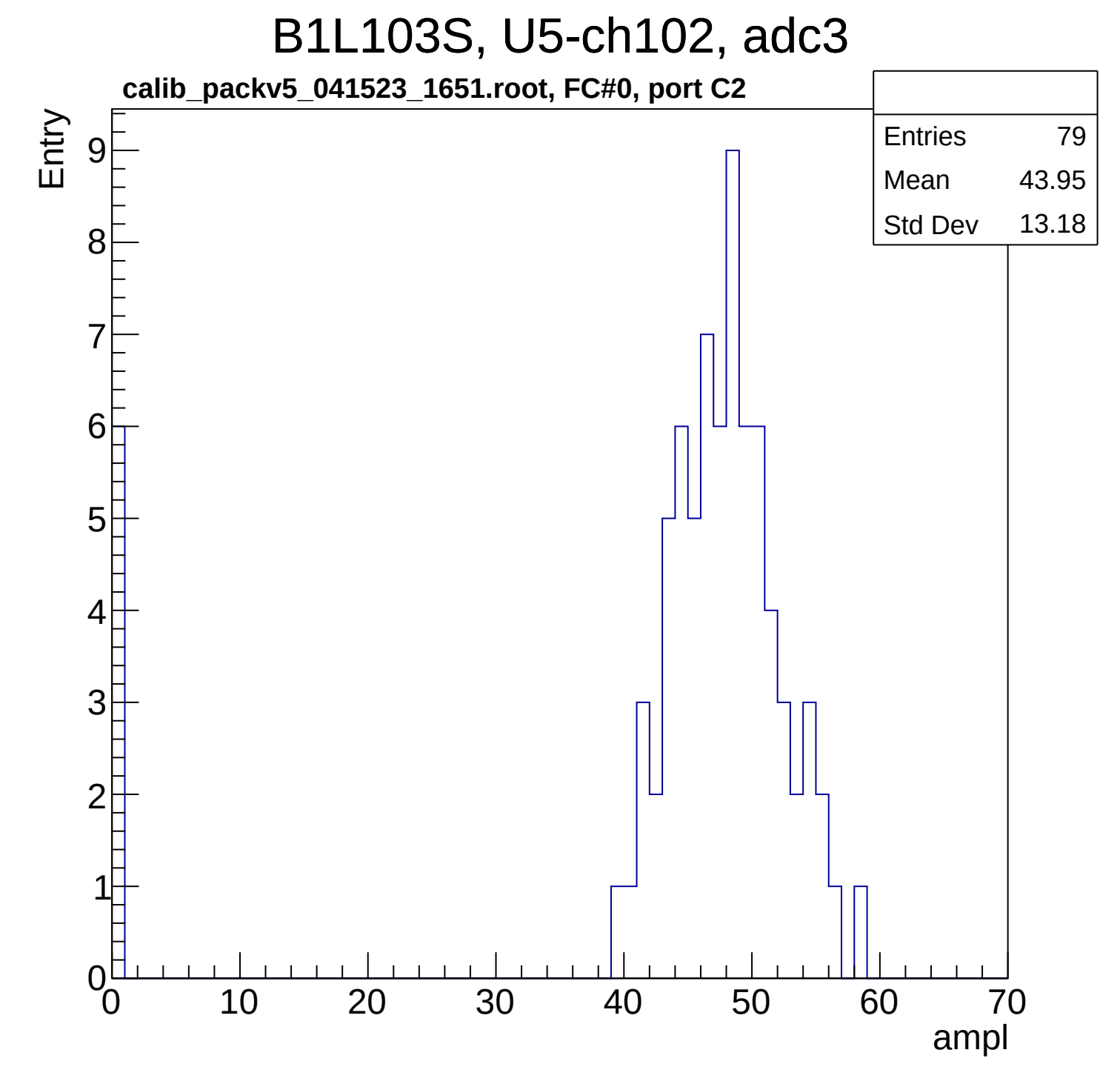
B1L103S, U5-ch102, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 43.95
Std Dev 13.18
Entry
ampl
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2
3
4
5
6
7
8
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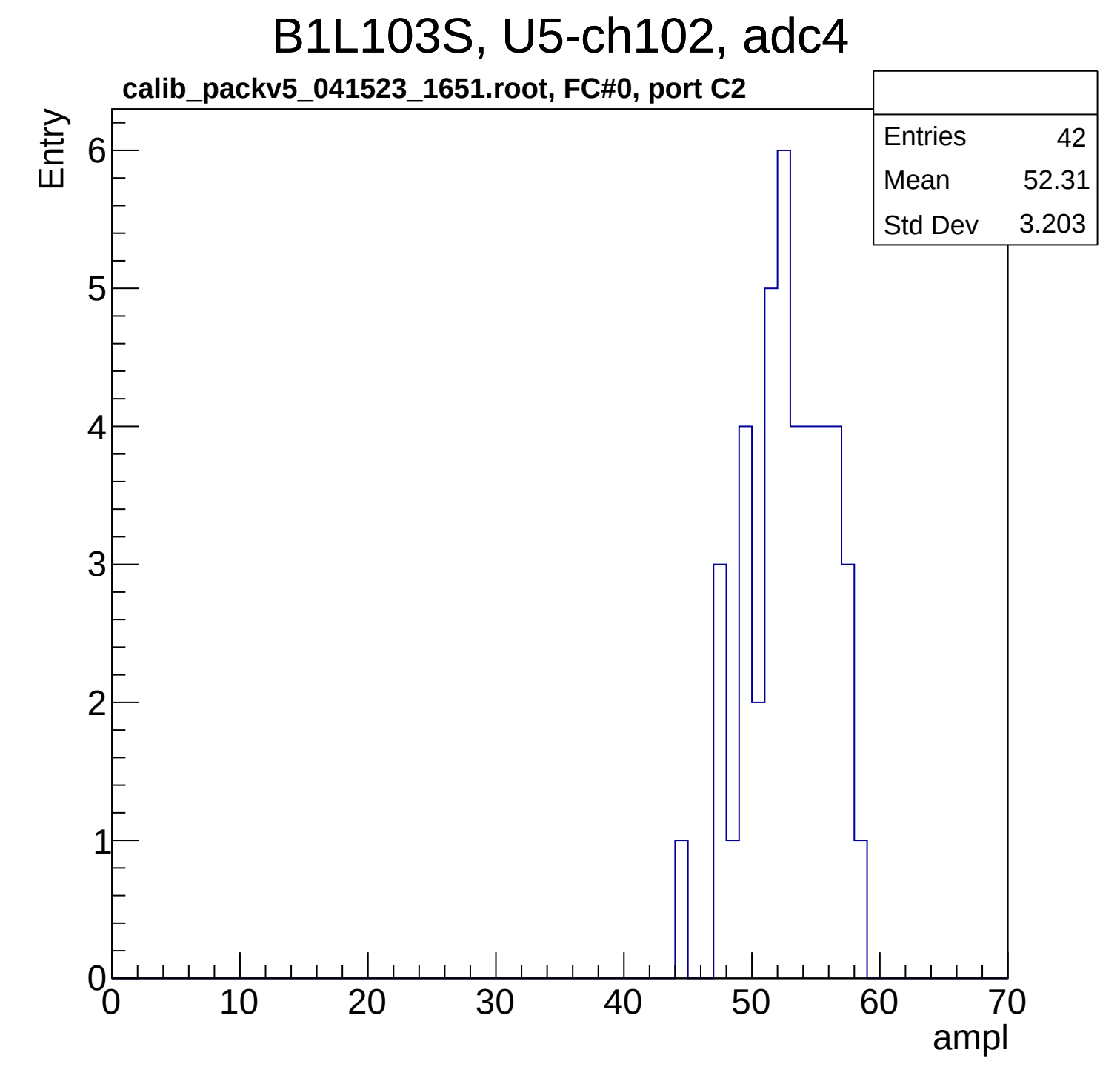
B1L103S, U5-ch102, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 52.31
Std Dev 3.203
Entry
ampl
0
1
2
3
4
5
6
0
10
20
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40
50
60
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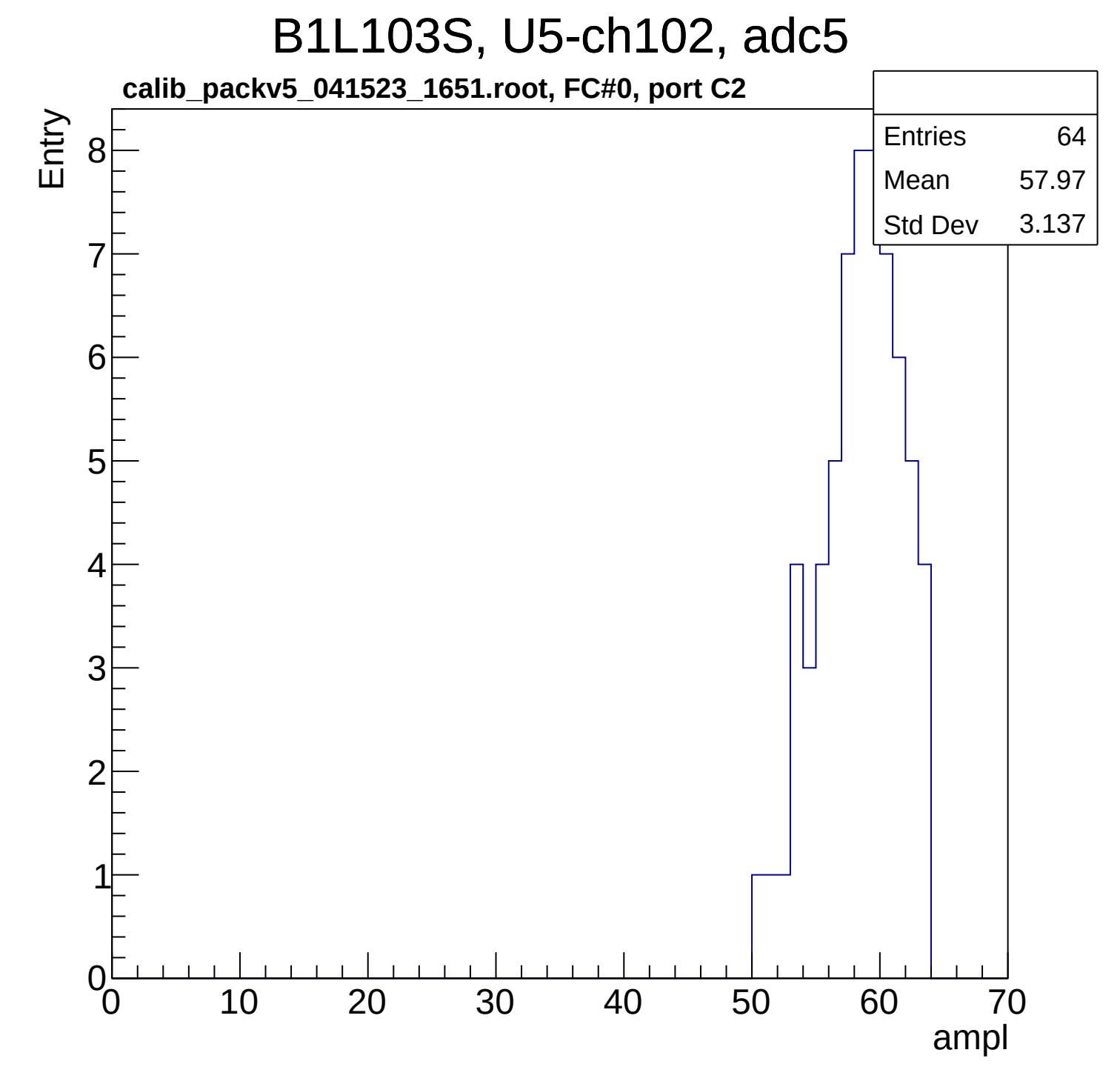
B1L103S, U5-ch102, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 57.97
Std Dev 3.137
Entry
ampl
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1
2
3
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5
6
7
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0
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40
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60
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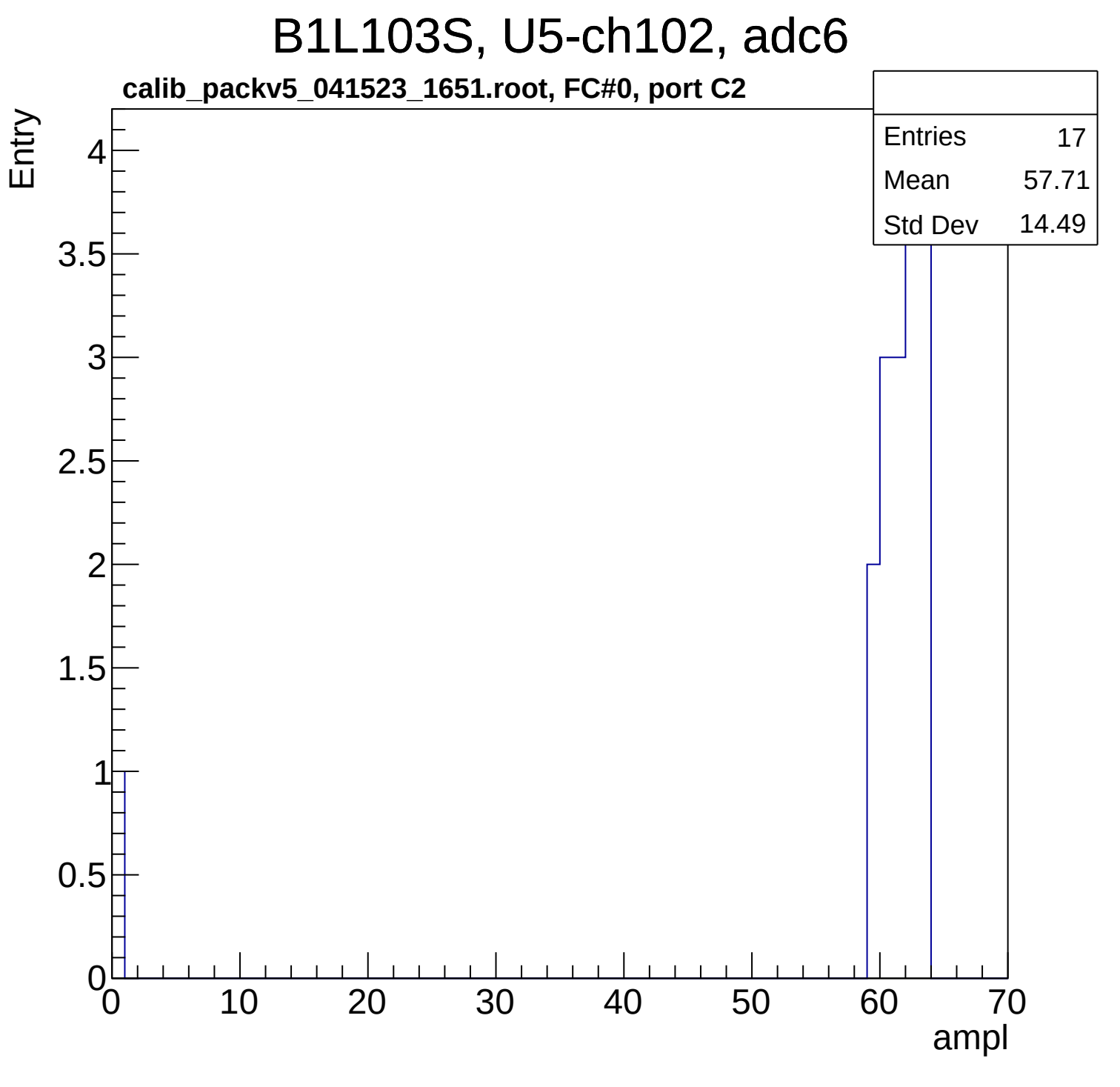
B1L103S, U5-ch102, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 57.71
Std Dev 14.49
Entry
ampl
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1.5
2
2.5
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3.5
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0
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40
50
60
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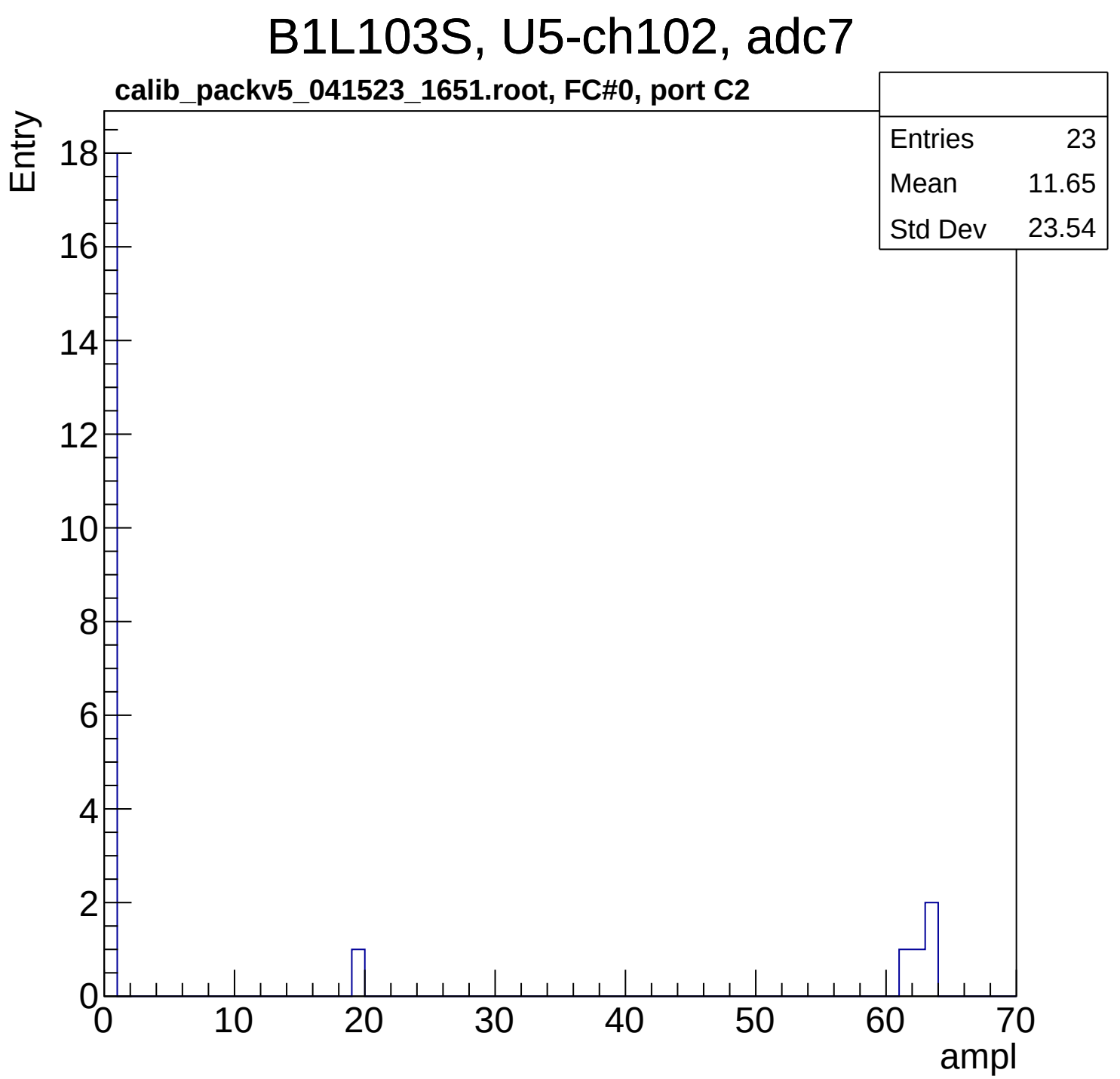
B1L103S, U5-ch102, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 11.65
Std Dev 23.54
Entry
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8
10
12
14
16
18
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10
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30
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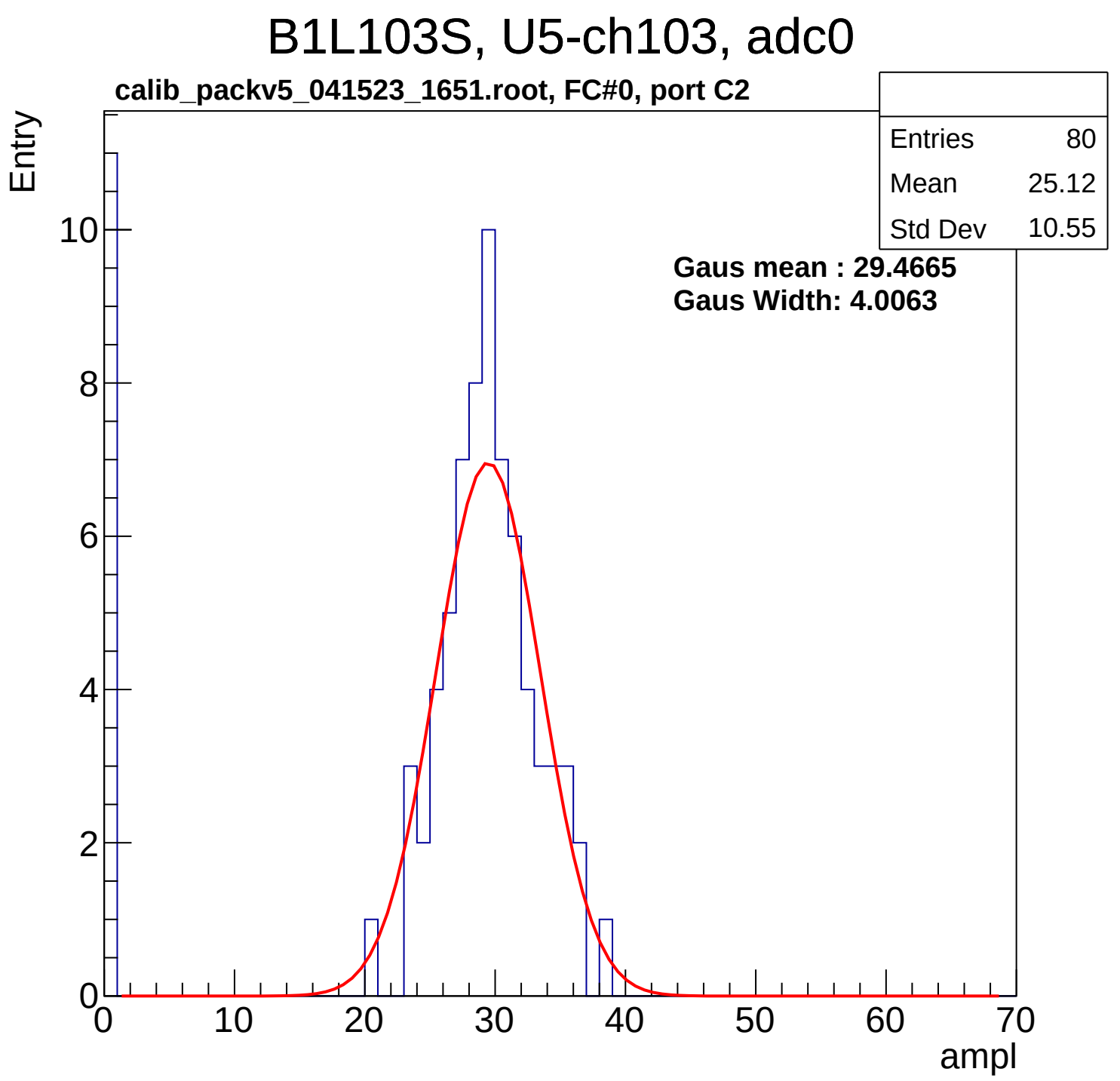
50
60
70
ampl


B1L103S, U5-ch103, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 25.12
Std Dev 10.55
Gaus mean : 29.4665
Gaus Width: 4.0063
Entry
ampl
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2
4
6
8
10
0
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20
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40
50
60
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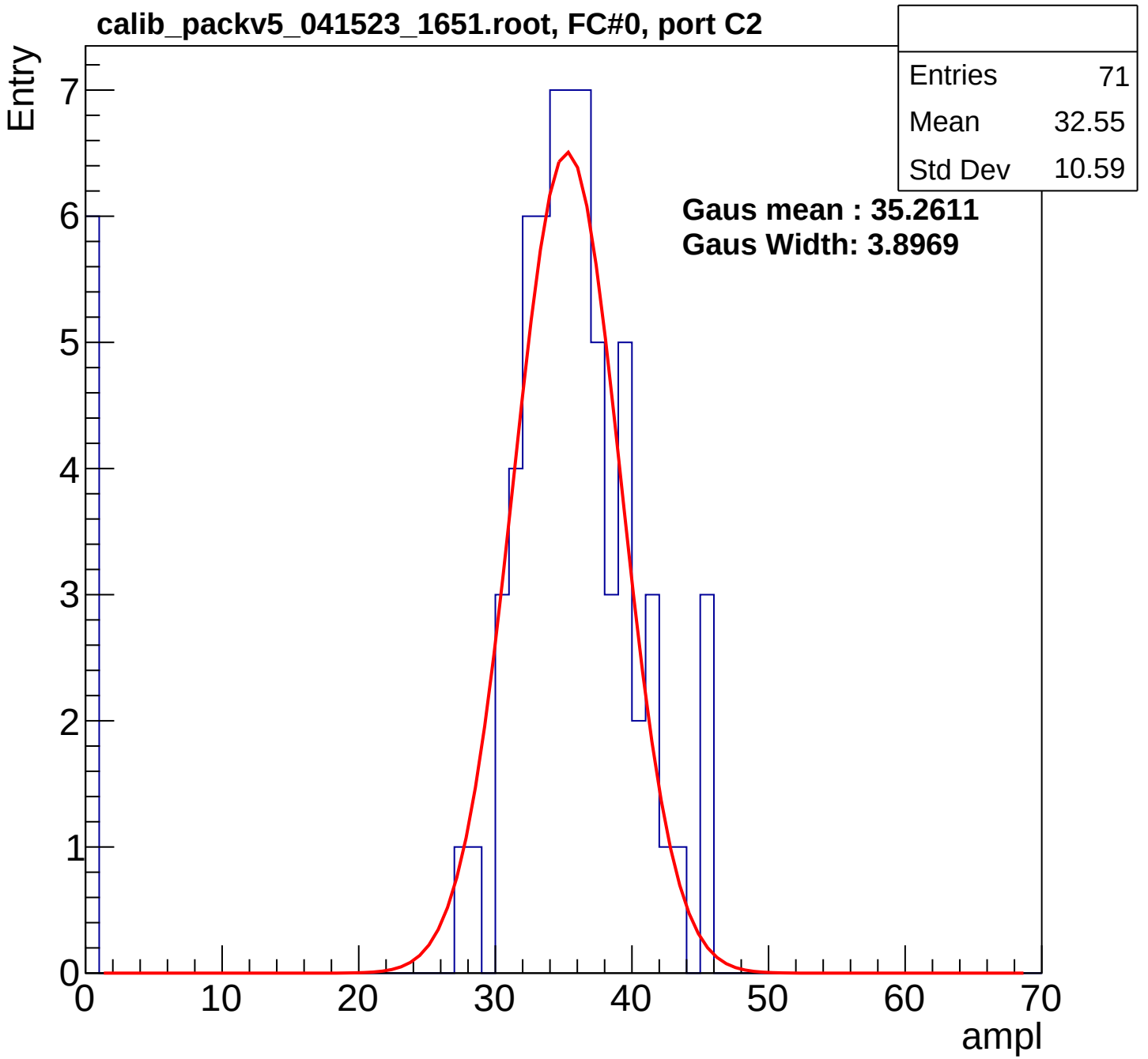
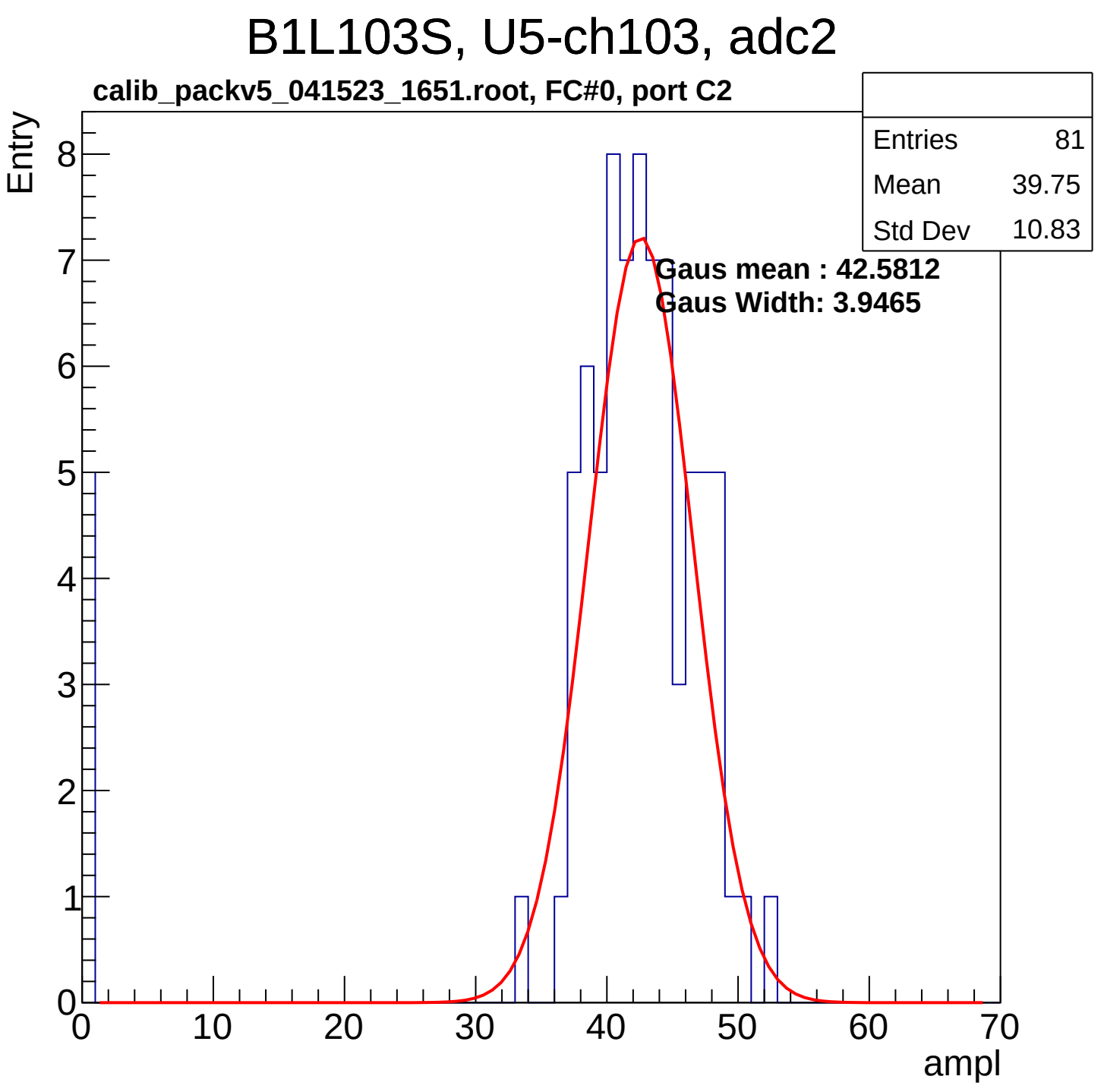

B1L103S, U5-ch103, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 32.55
Std Dev 10.59
Gaus mean : 35.2611
Gaus Width: 3.8969
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U5-ch103, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 39.75
Std Dev 10.83
Gaus mean : 42.5812
Gaus Width: 3.9465
Entry
ampl
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1
2
3
4
5
6
7
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0
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60
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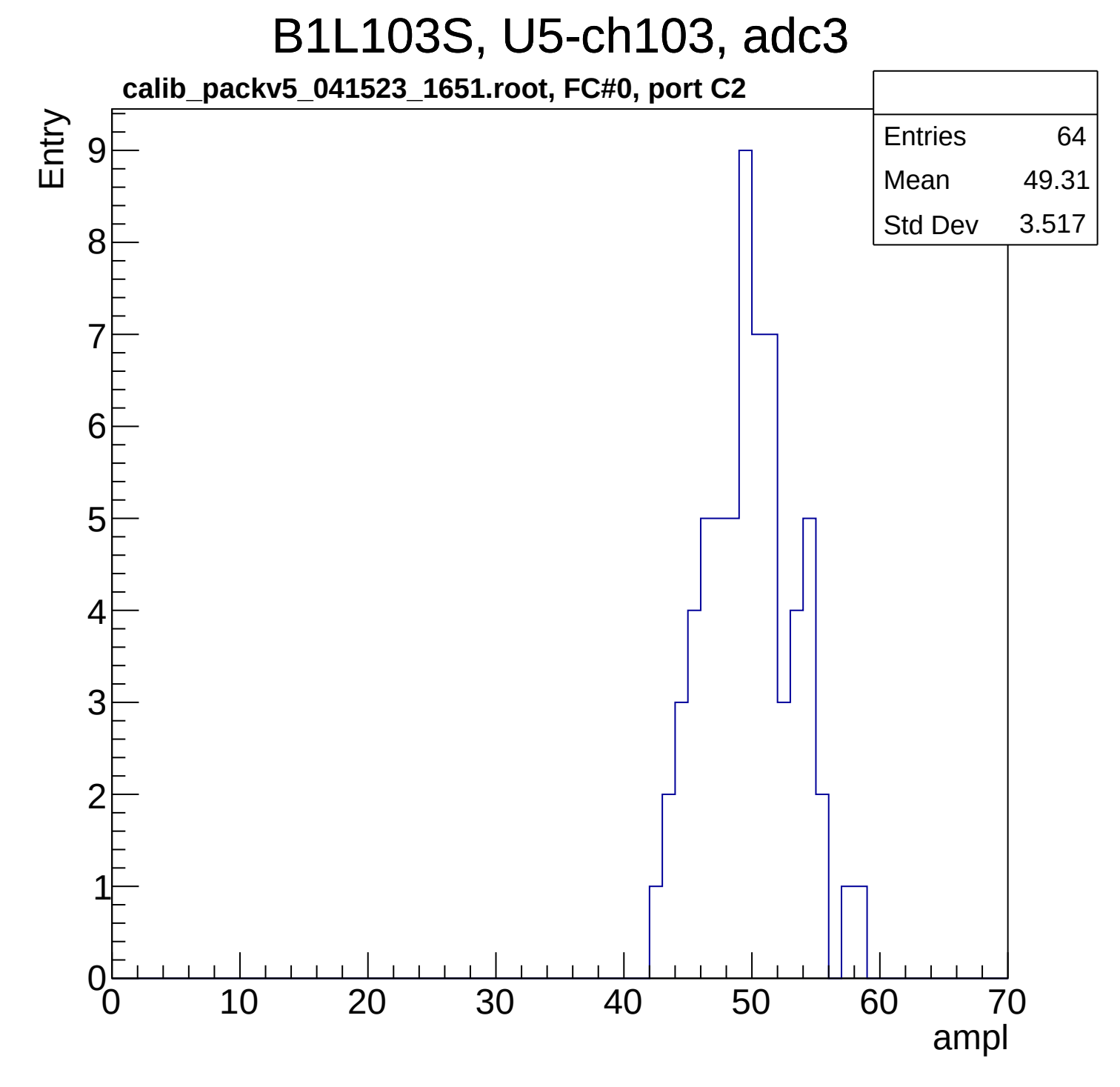
B1L103S, U5-ch103, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 49.31
Std Dev 3.517
Entry
ampl
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20
30
40
50
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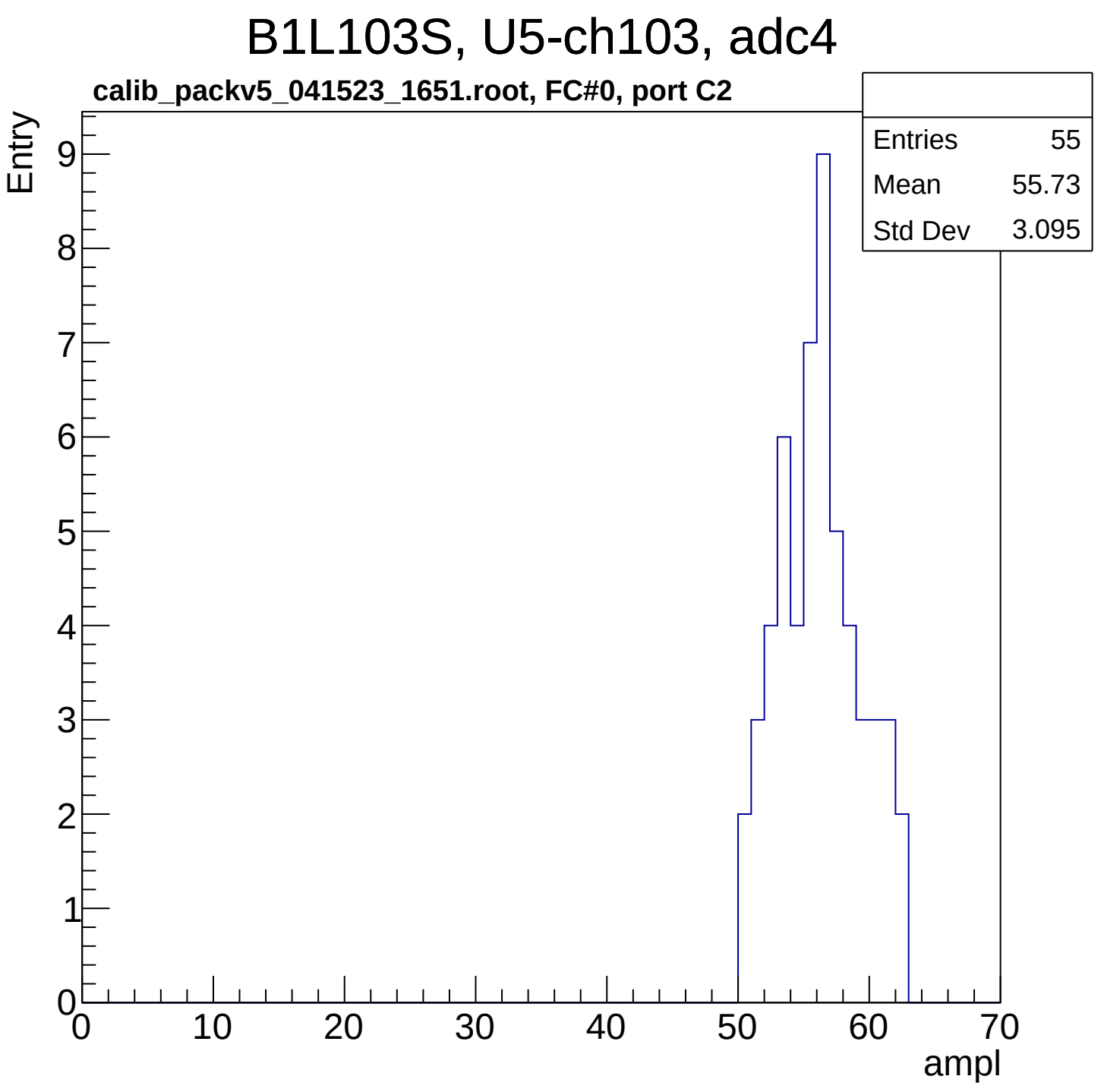
6
7
8
9


B1L103S, U5-ch103, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 55.73
Std Dev 3.095
Entry
ampl
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4
5
6
7
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0
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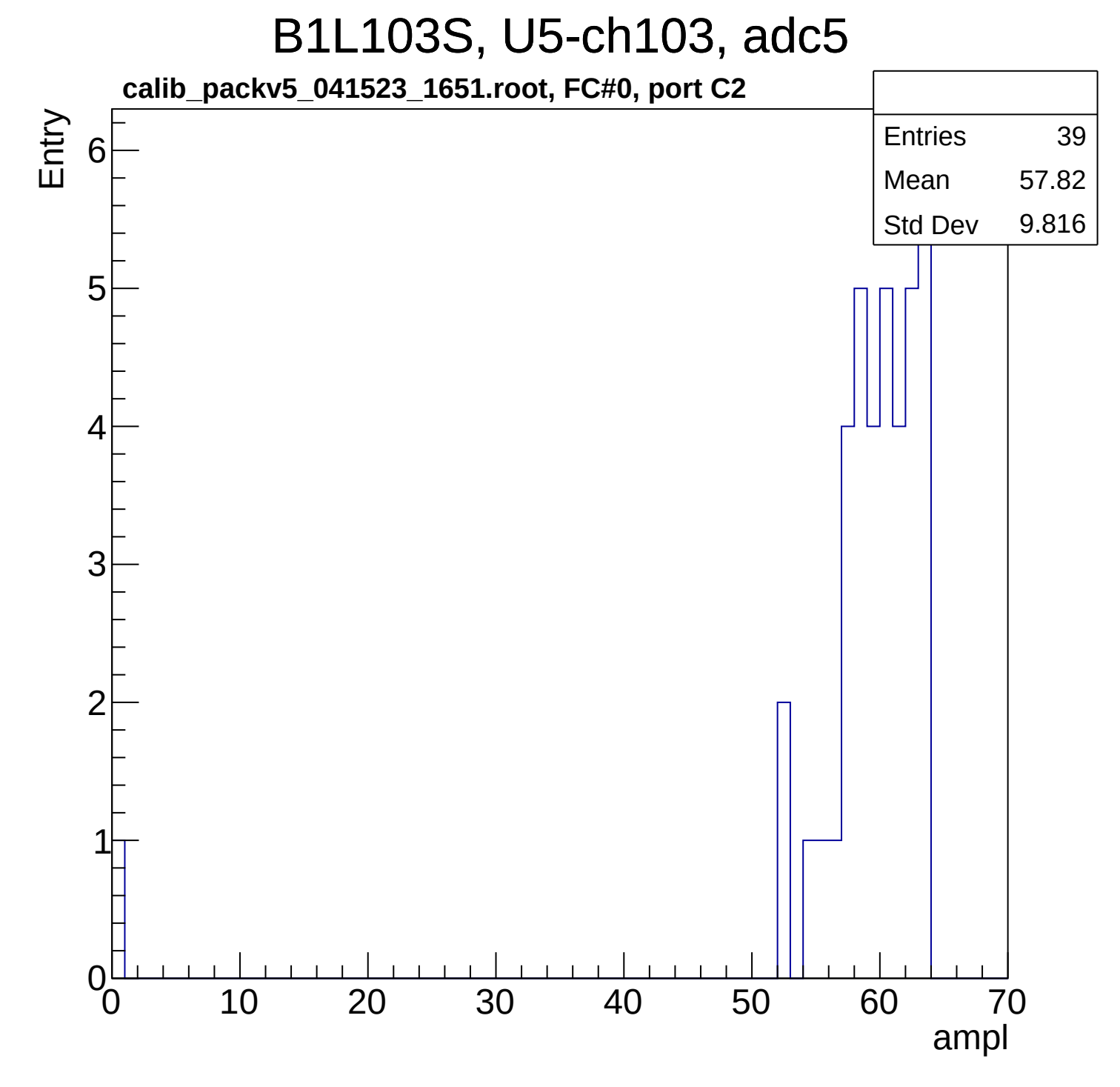
B1L103S, U5-ch103, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 57.82
Std Dev 9.816
Entry
ampl
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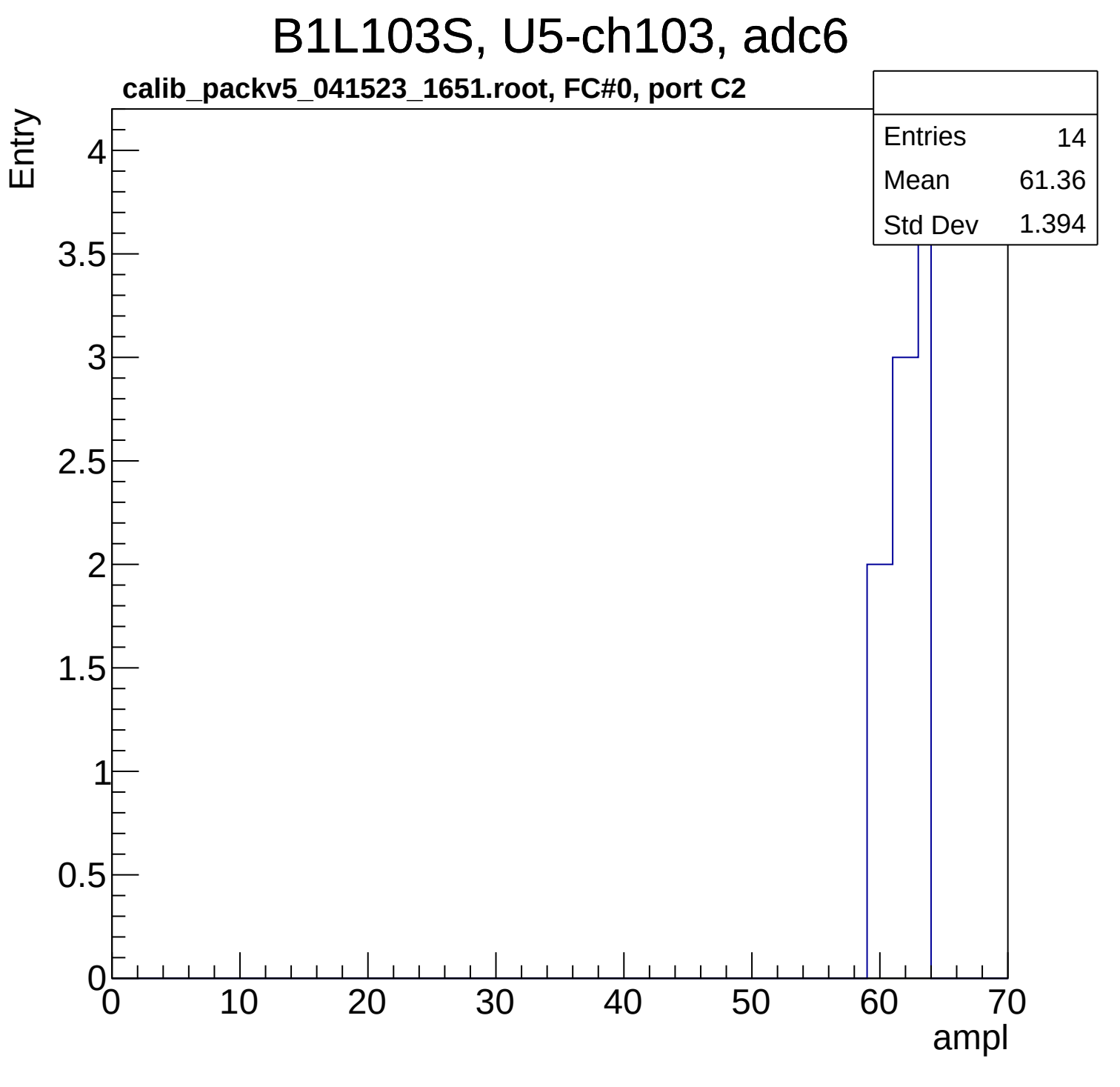
B1L103S, U5-ch103, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.36
Std Dev 1.394
Entry
ampl
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1.5
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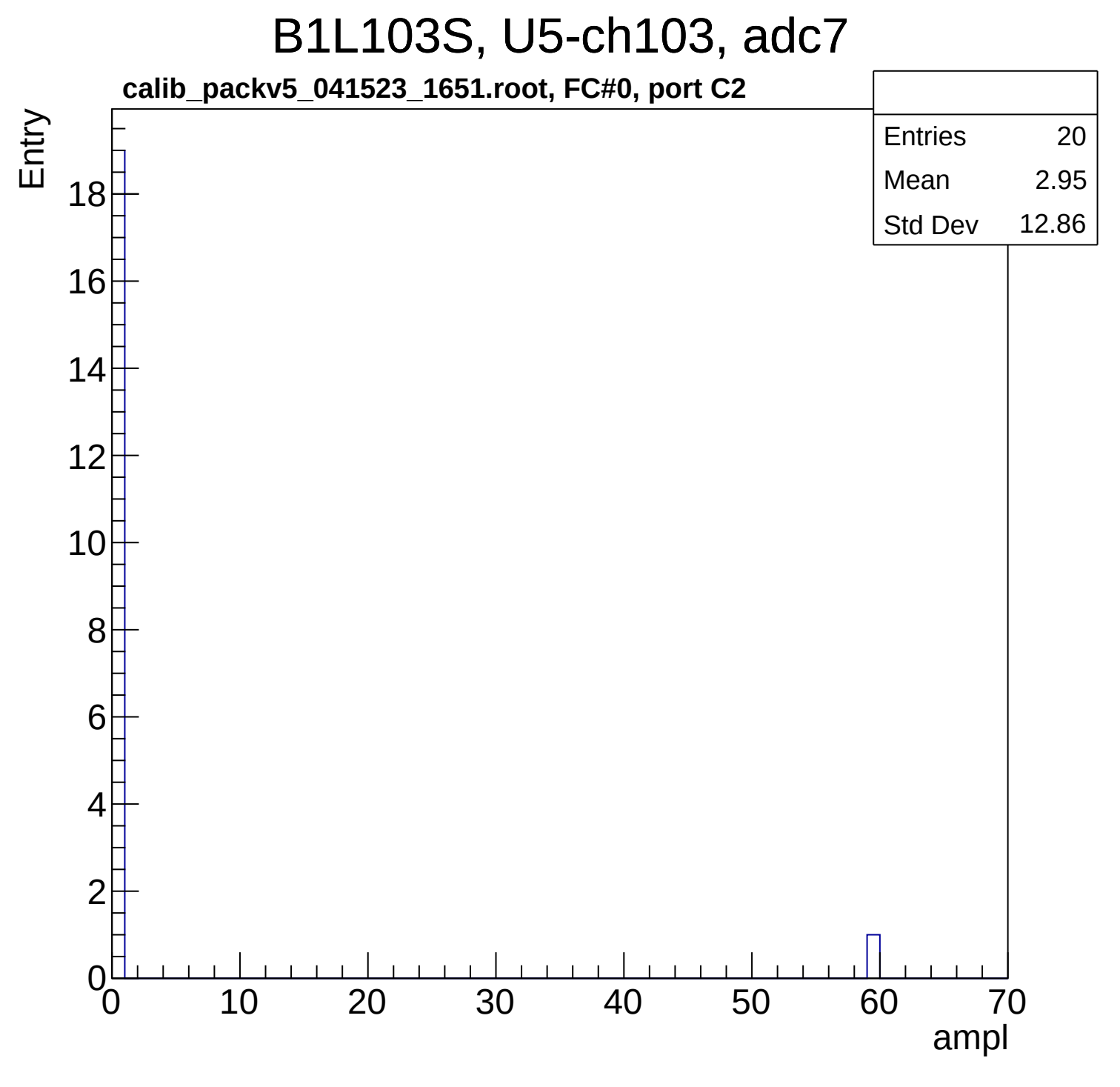
B1L103S, U5-ch103, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 2.95
Std Dev 12.86
Entry
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10
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14
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10
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30
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50
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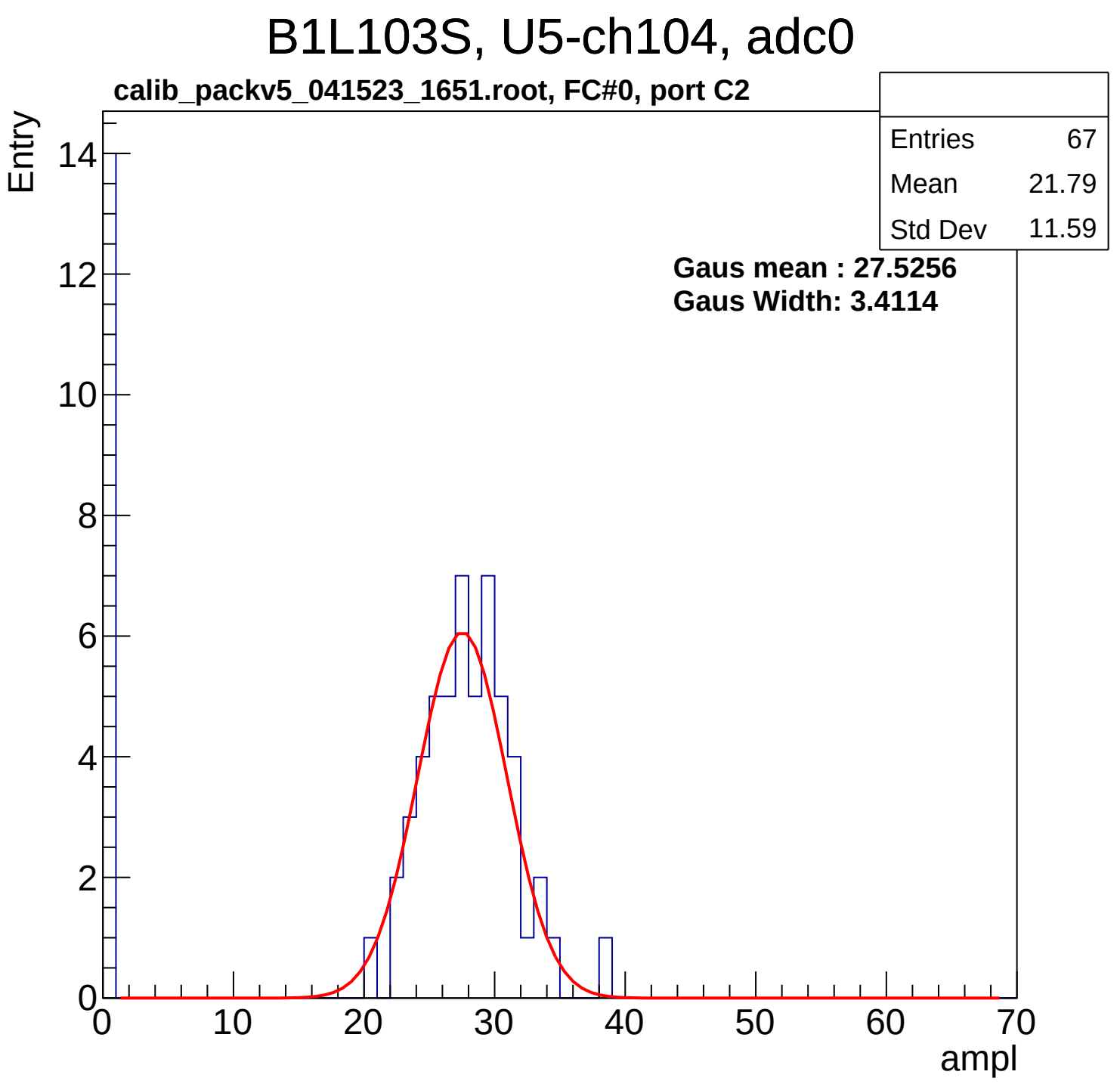
70
ampl


B1L103S, U5-ch104, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 21.79
Std Dev 11.59
Gaus mean : 27.5256
Gaus Width: 3.4114
Entry
ampl
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2
4
6
8
10
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0
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60
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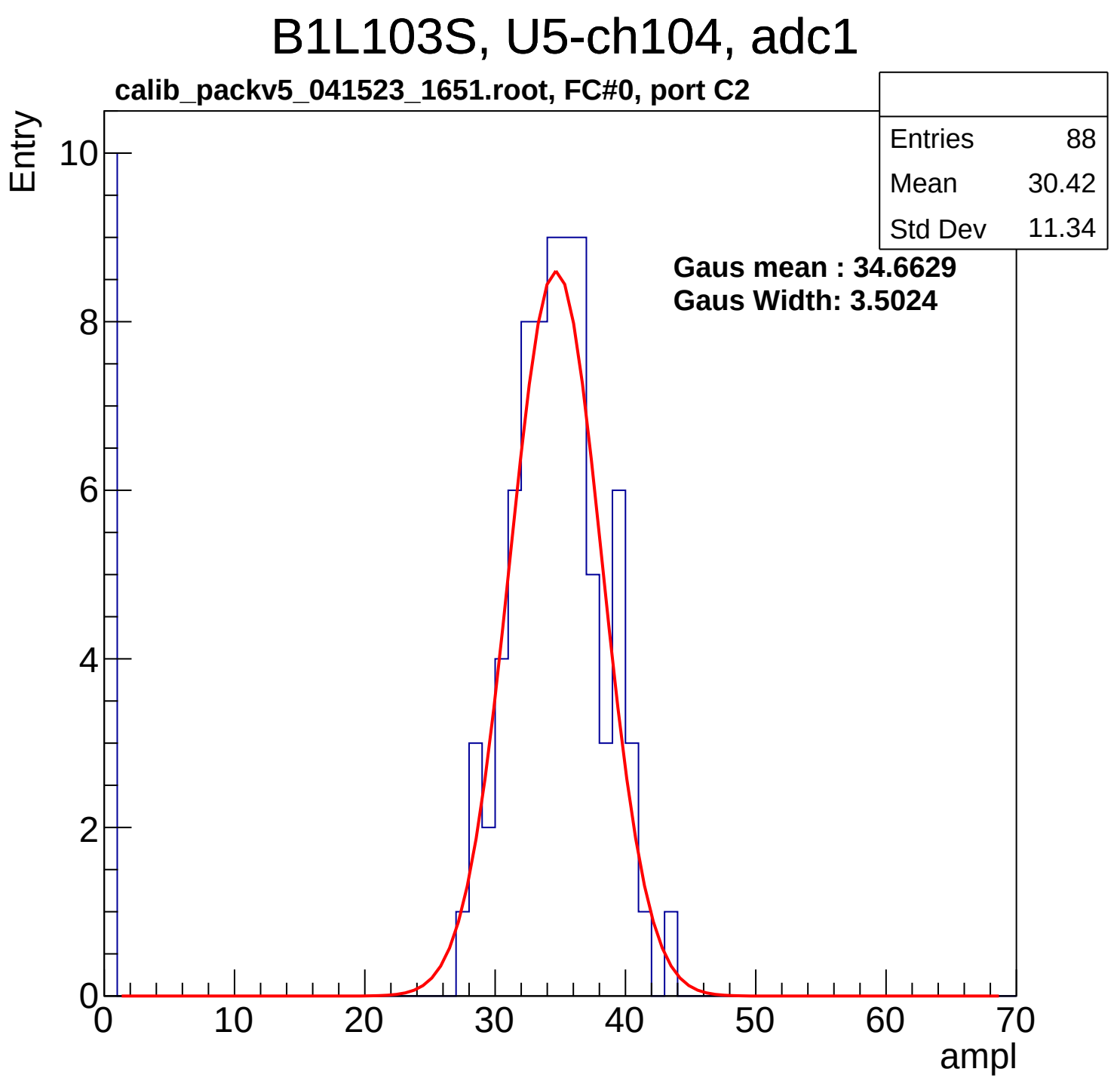
B1L103S, U5-ch104, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 30.42
Std Dev 11.34
Gaus mean : 34.6629
Gaus Width: 3.5024
Entry
ampl
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4
6
8
10
0
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20
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40
50
60
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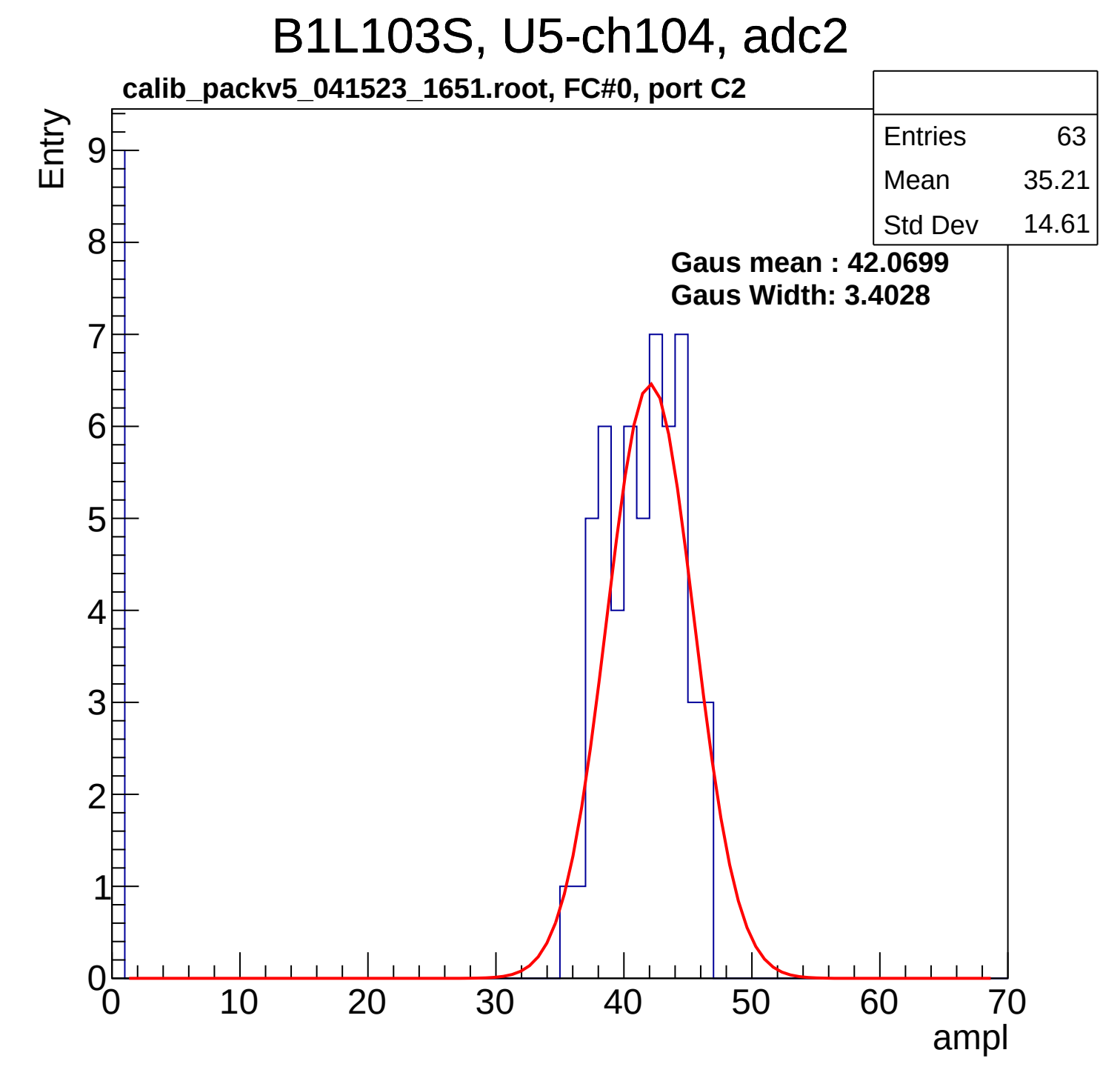
B1L103S, U5-ch104, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 35.21
Std Dev 14.61
Gaus mean : 42.0699
Gaus Width: 3.4028
Entry
ampl
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2
3
4
5
6
7
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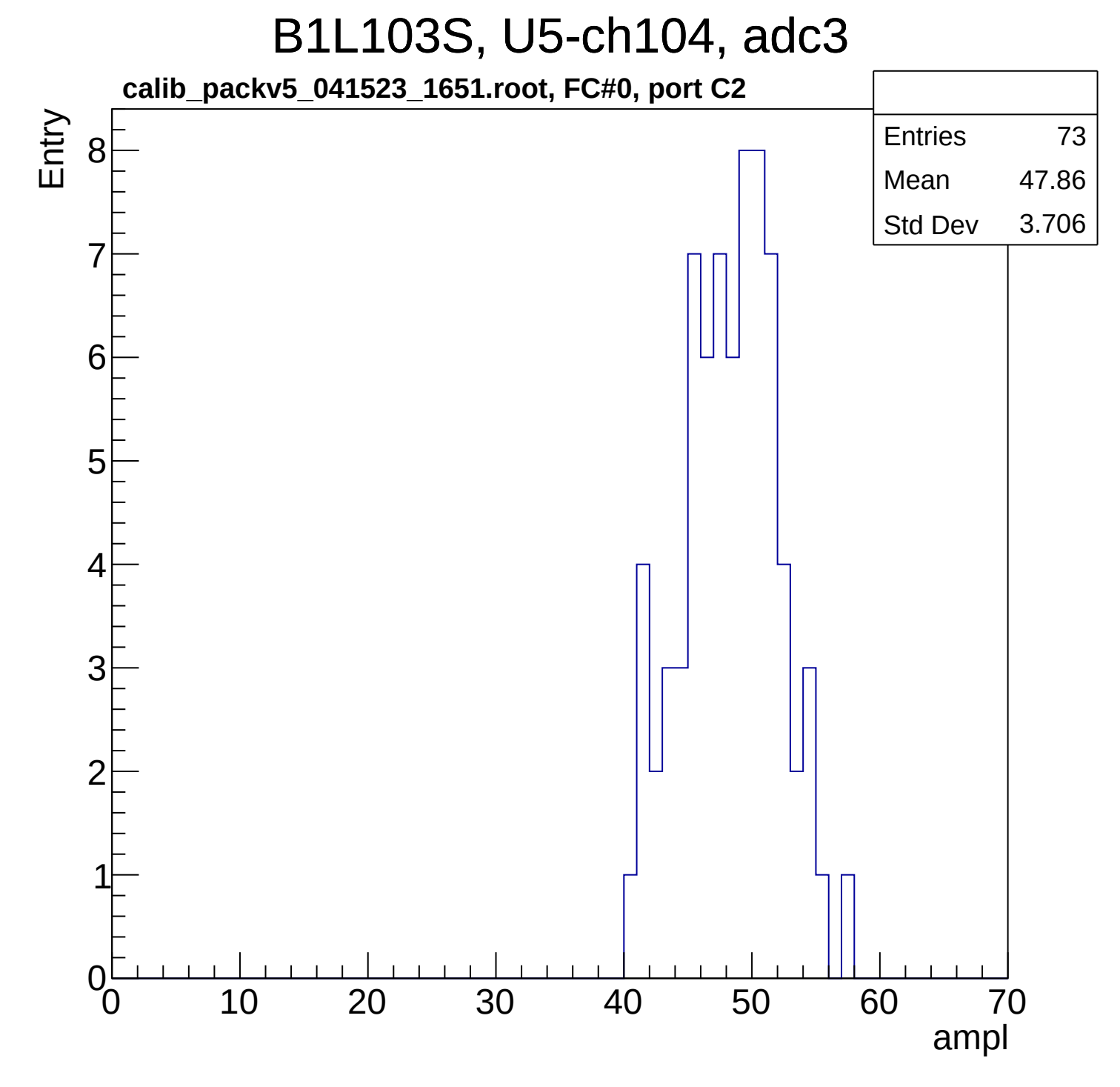
B1L103S, U5-ch104, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 47.86
Std Dev 3.706
Entry
ampl
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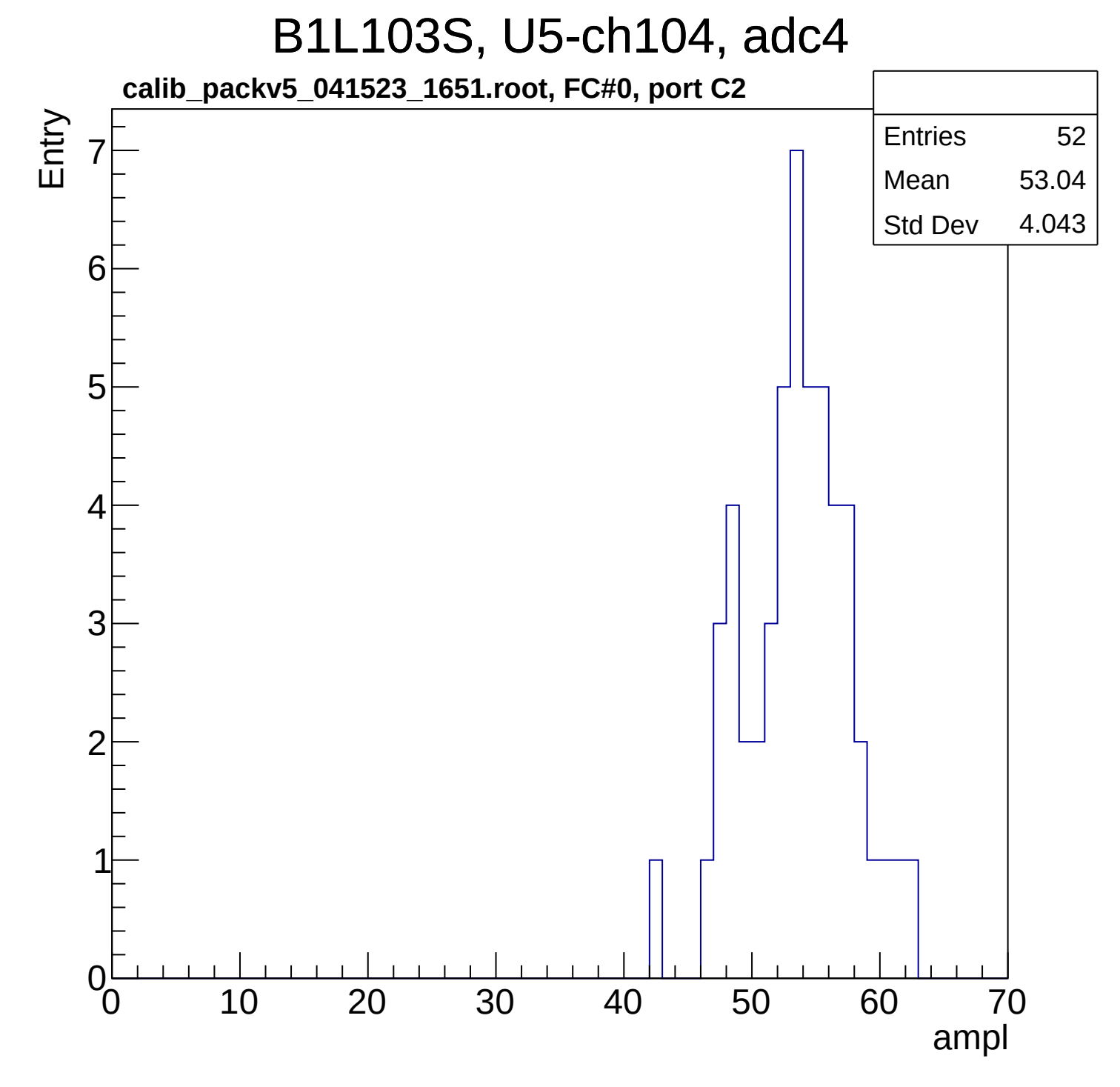
B1L103S, U5-ch104, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 53.04
Std Dev 4.043
Entry
ampl
0
1
2
3
4
5
6
7
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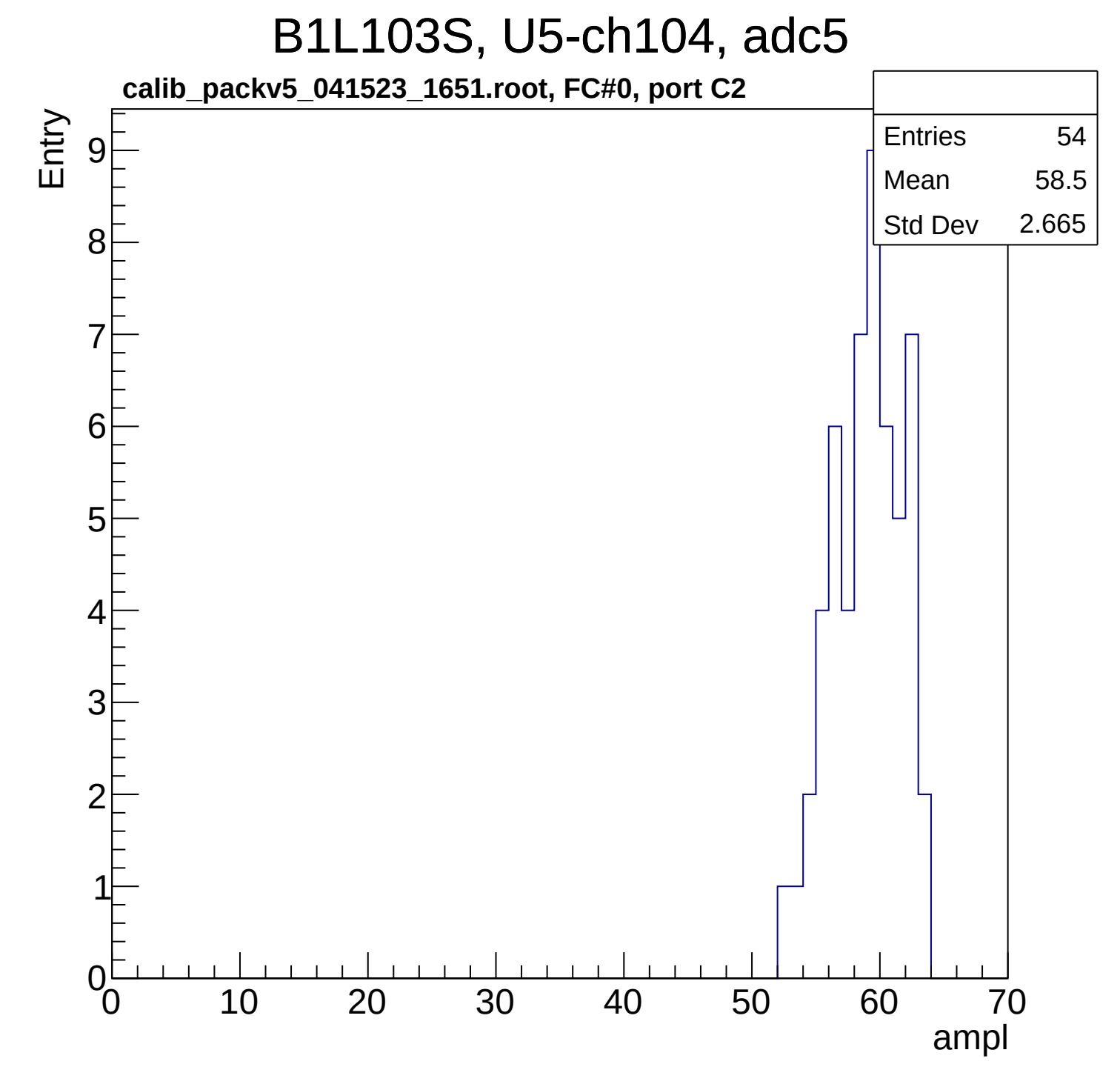
B1L103S, U5-ch104, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.5
Std Dev 2.665
Entry
ampl
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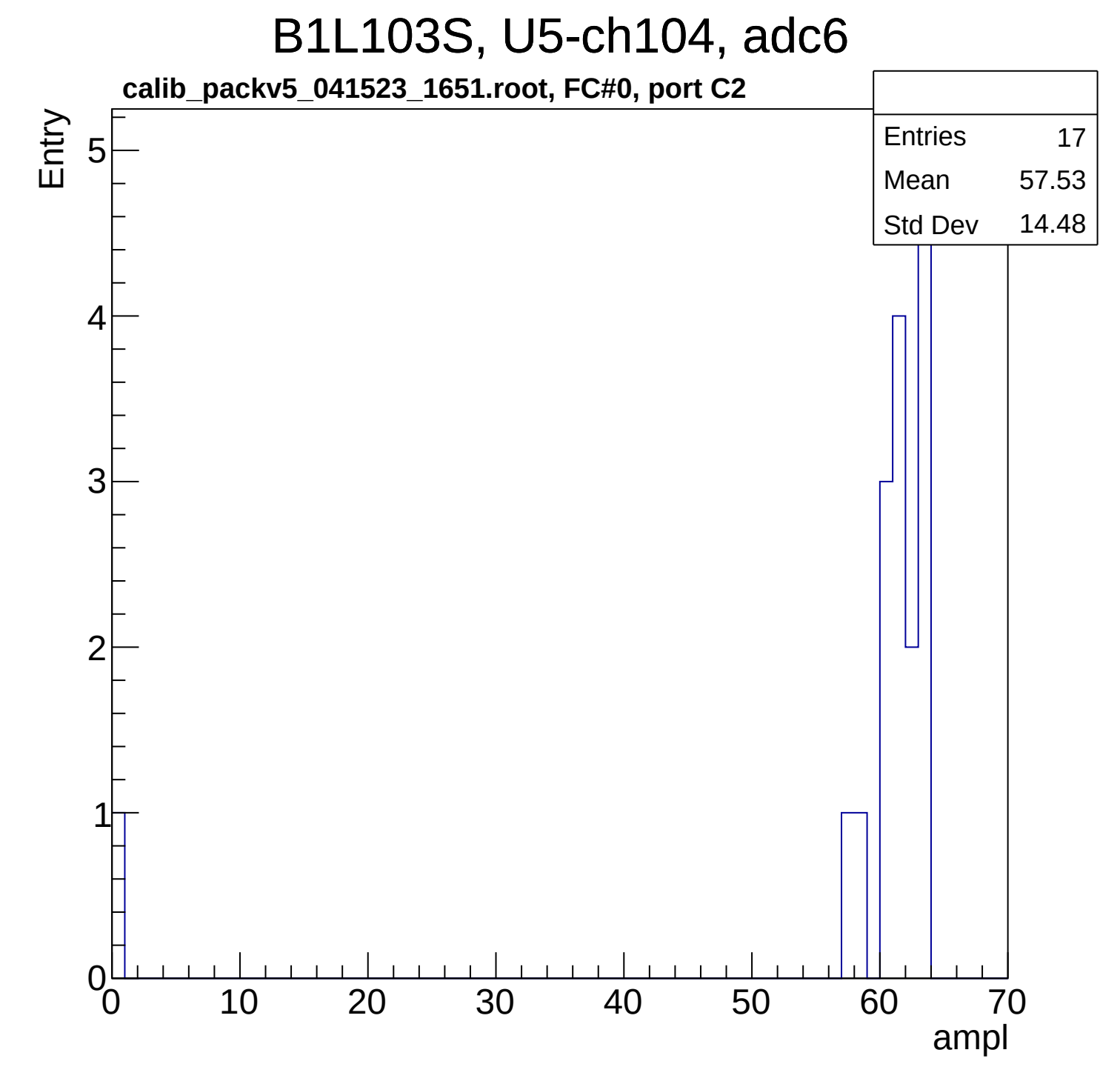
B1L103S, U5-ch104, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 57.53
Std Dev 14.48
Entry
ampl
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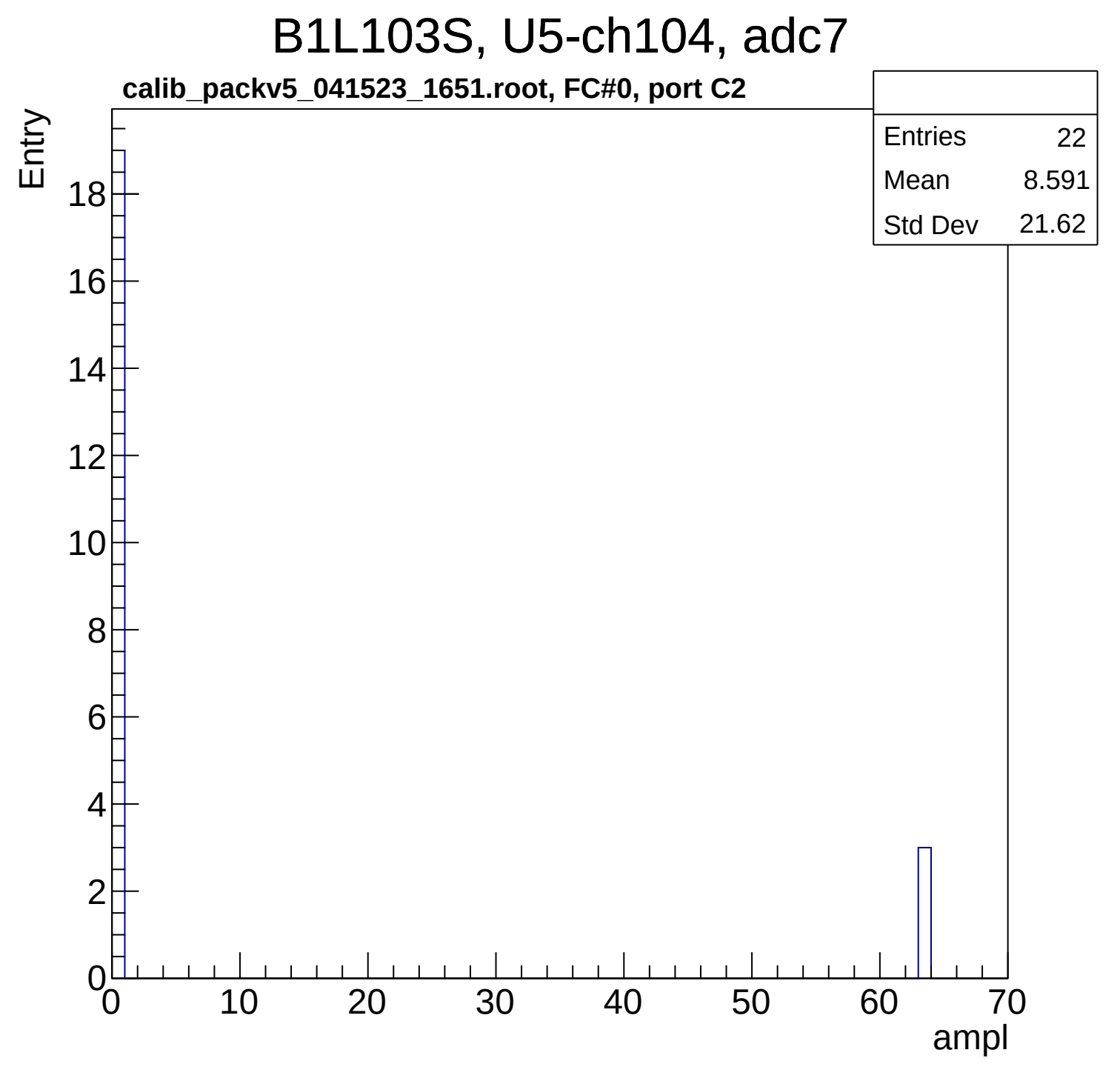
B1L103S, U5-ch104, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.591
Std Dev 21.62
Entry
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6
8
10
12
14
16
18
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20
30
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50
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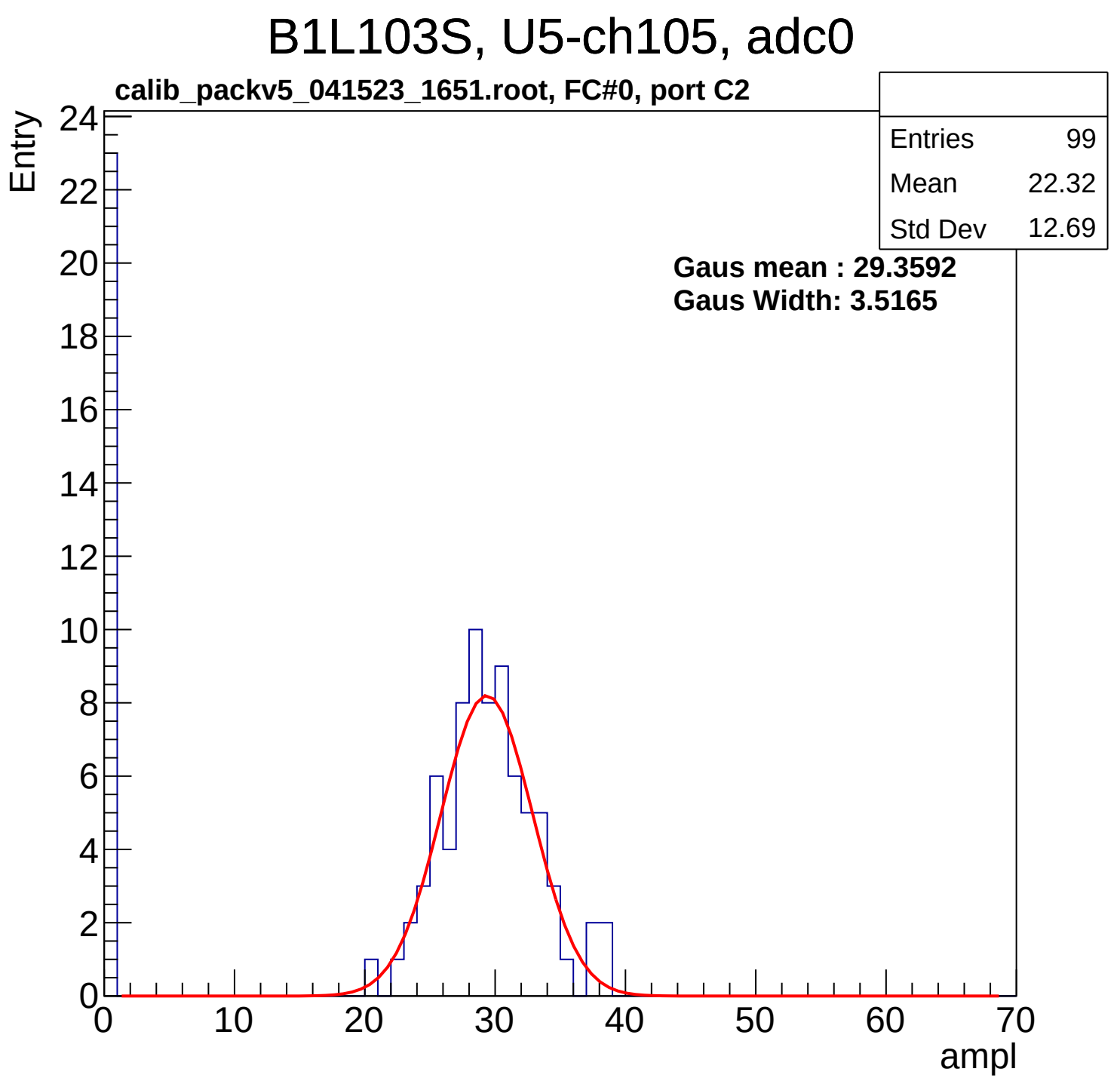
70
ampl


B1L103S, U5-ch105, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 22.32
Std Dev 12.69
Gaus mean : 29.3592
Gaus Width: 3.5165
Entry
ampl
0
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10
12
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16
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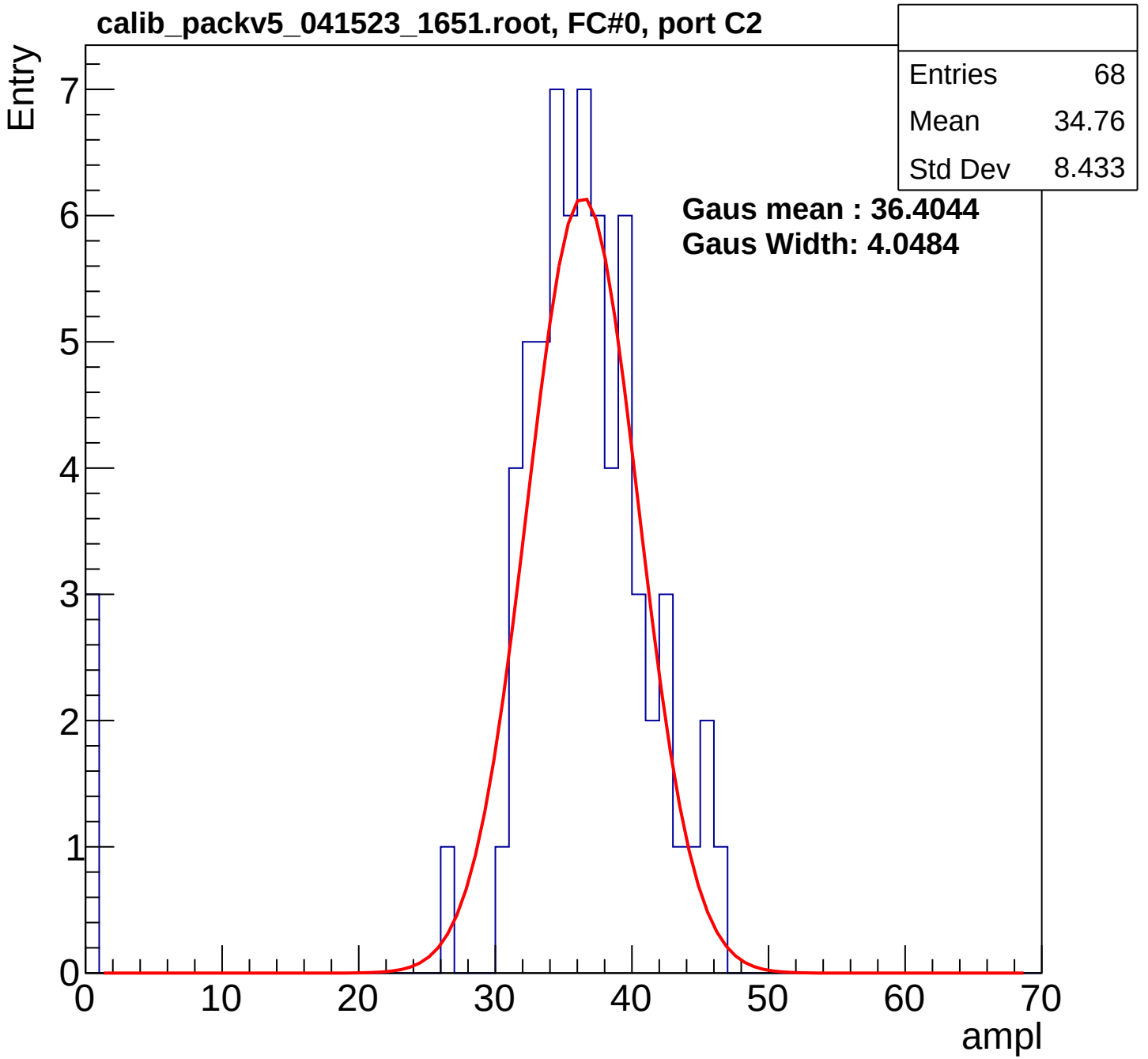
B1L103S, U5-ch105, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 34.76
Std Dev 8.433
Gaus mean : 36.4044
Gaus Width: 4.0484
Entry
ampl
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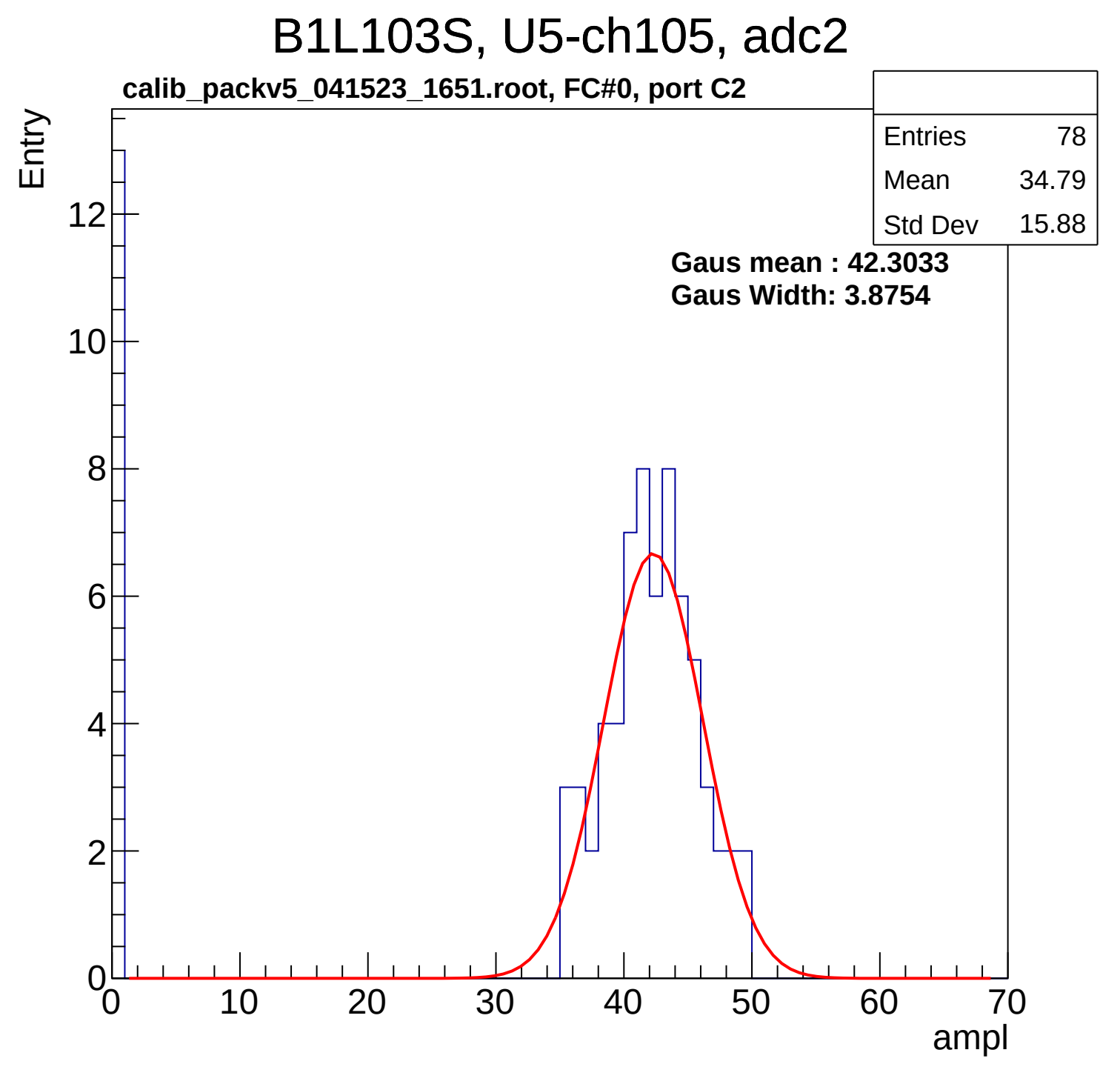
B1L103S, U5-ch105, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 34.79
Std Dev 15.88
Gaus mean : 42.3033
Gaus Width: 3.8754
Entry
ampl
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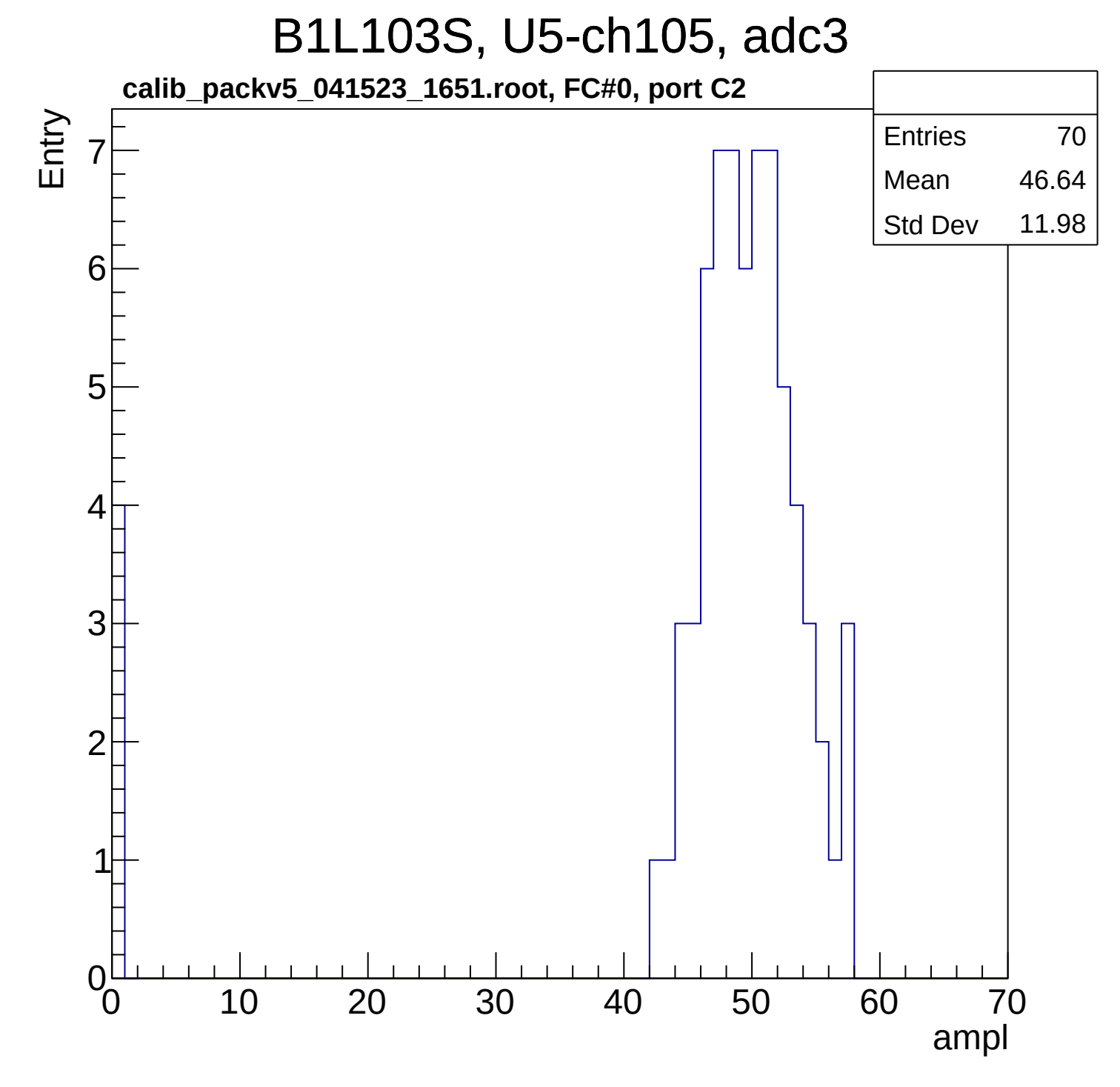
B1L103S, U5-ch105, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 46.64
Std Dev 11.98
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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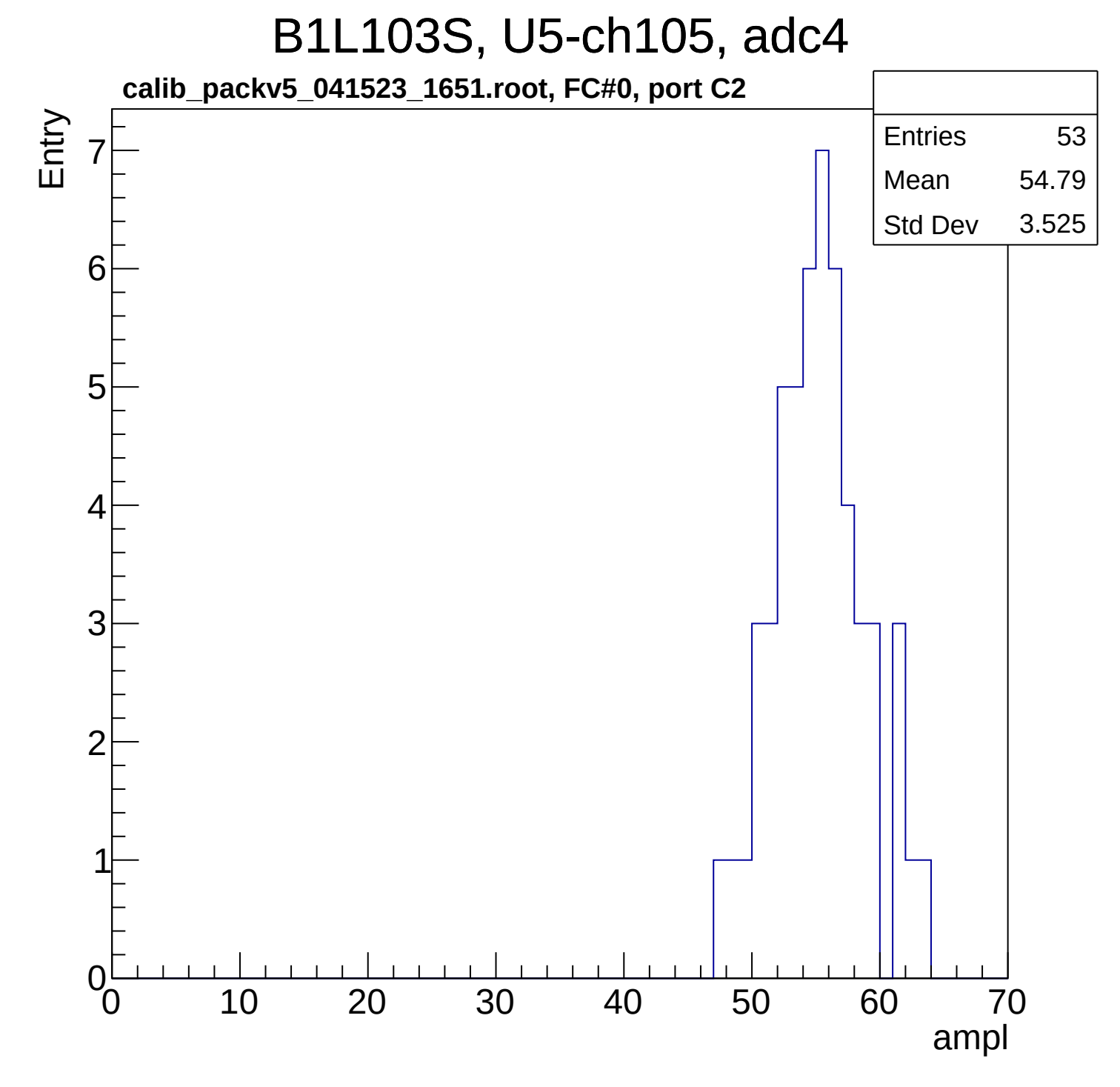
B1L103S, U5-ch105, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 54.79
Std Dev 3.525
Entry
ampl
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0
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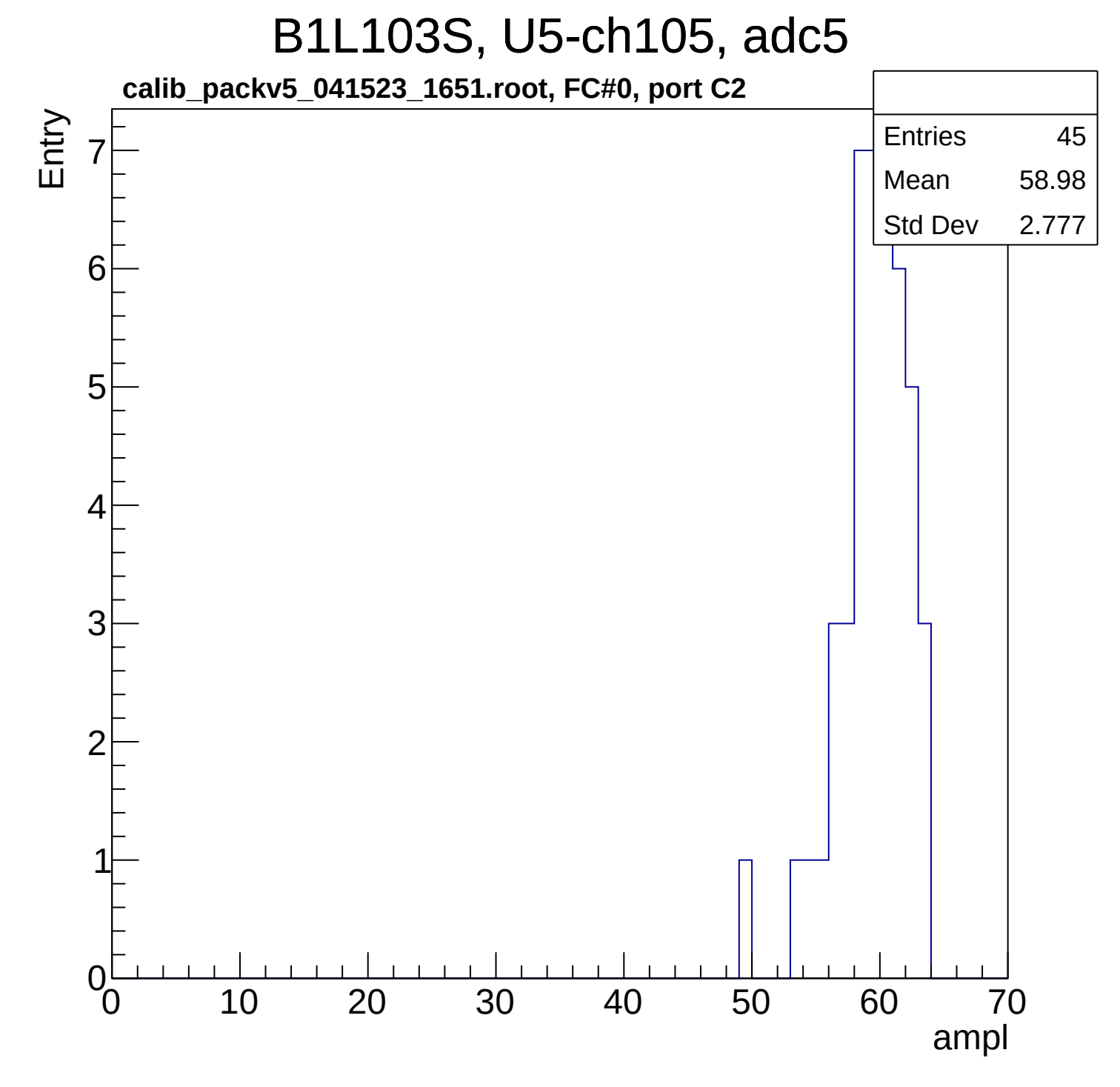
B1L103S, U5-ch105, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.98
Std Dev 2.777
Entry
ampl
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4
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6
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0
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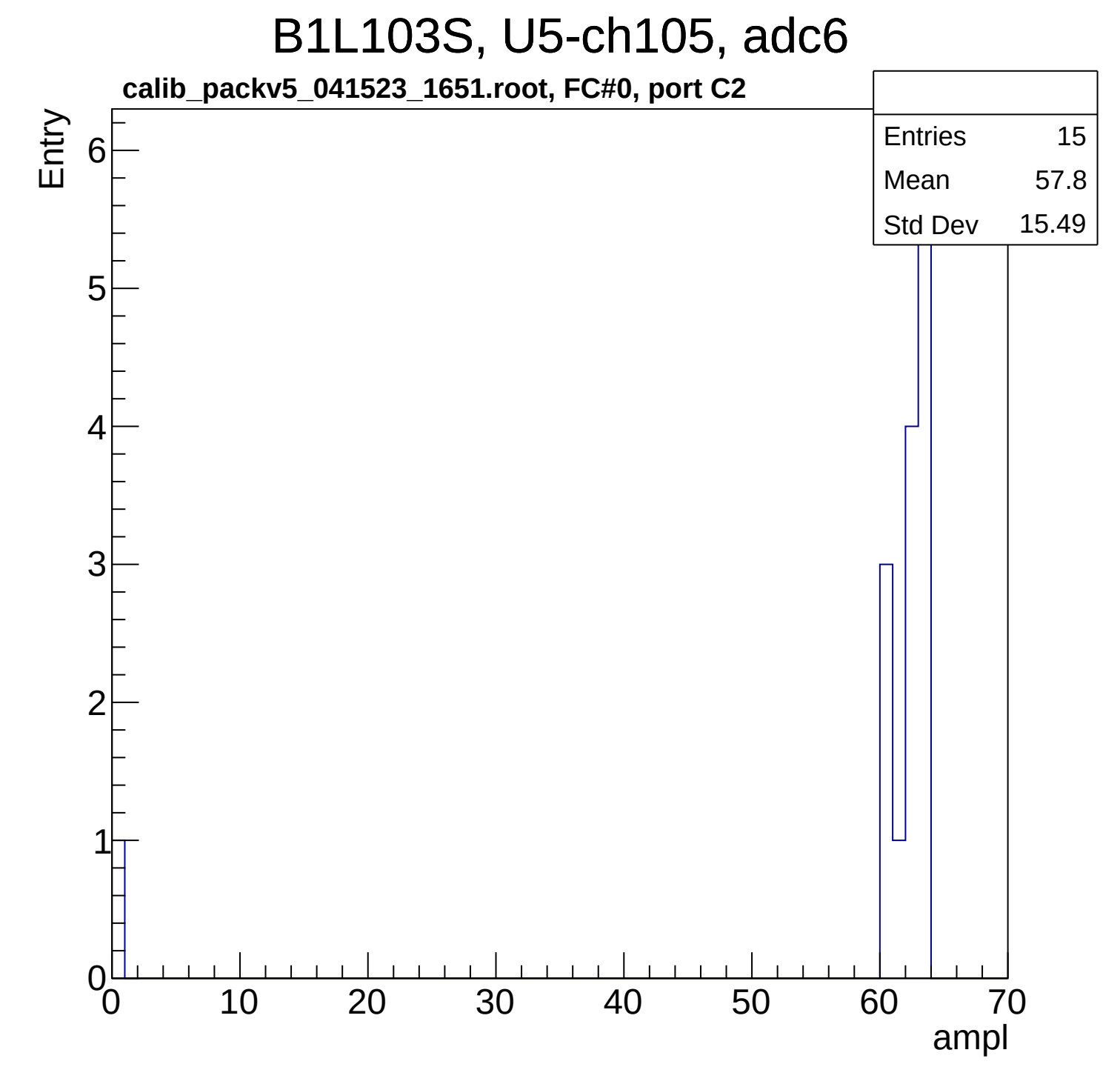
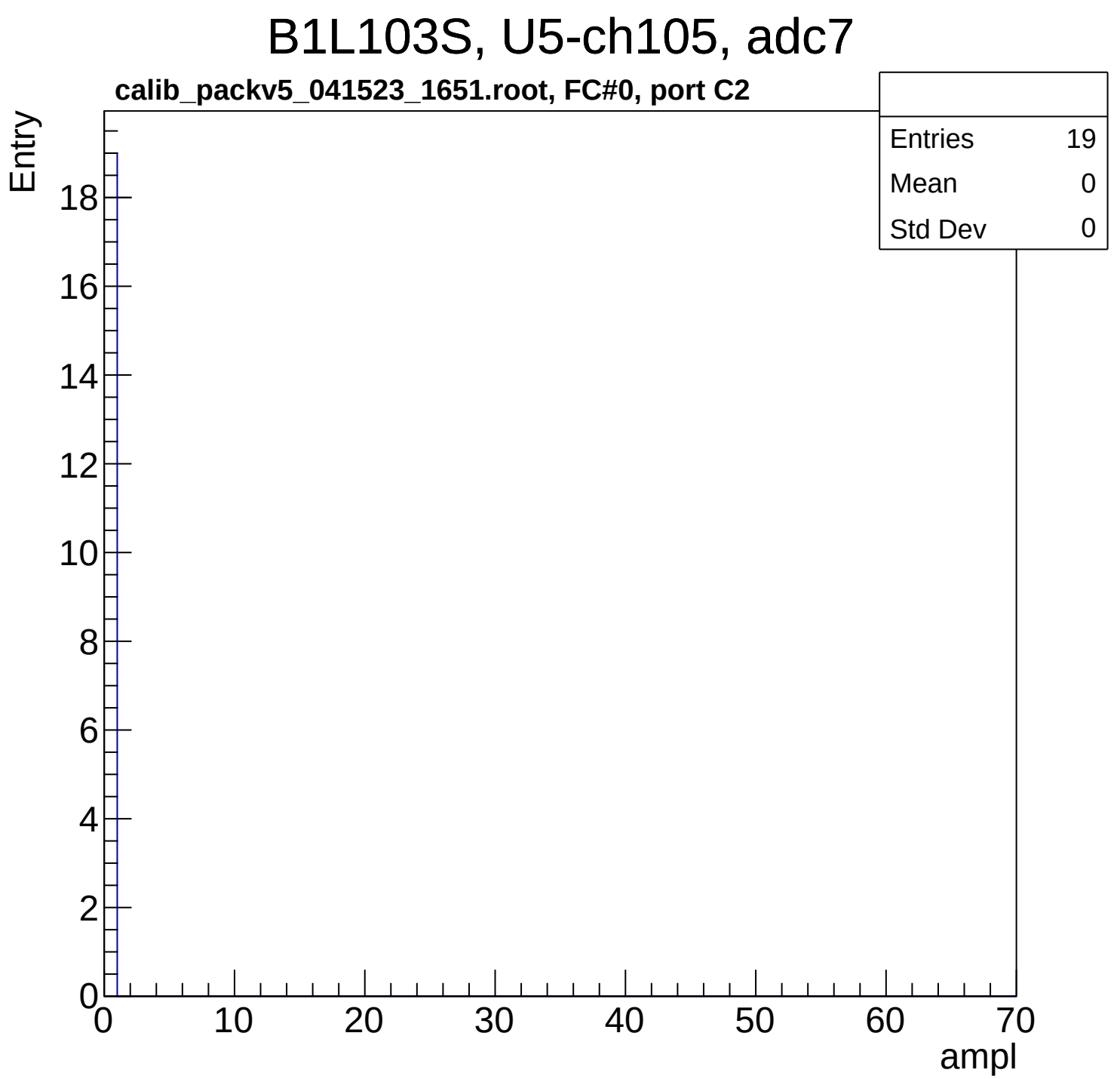

B1L103S, U5-ch105, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.8
Std Dev 15.49
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch105, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
0
10
20
30
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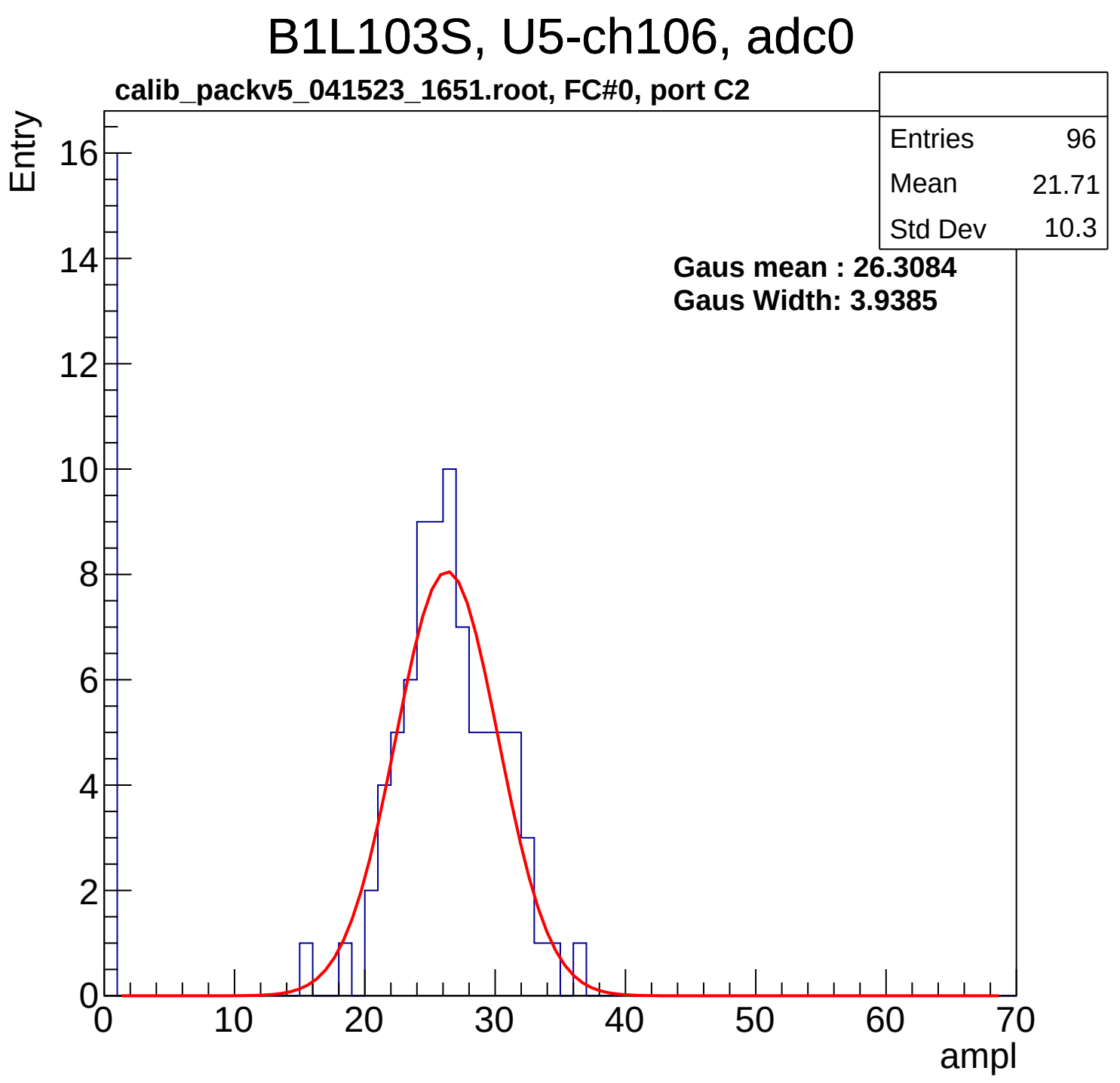
50
60
70
ampl


B1L103S, U5-ch106, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 21.71
Std Dev 10.3
Gaus mean : 26.3084
Gaus Width: 3.9385
Entry
ampl
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4
6
8
10
12
14
16
0
10
20
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40
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60
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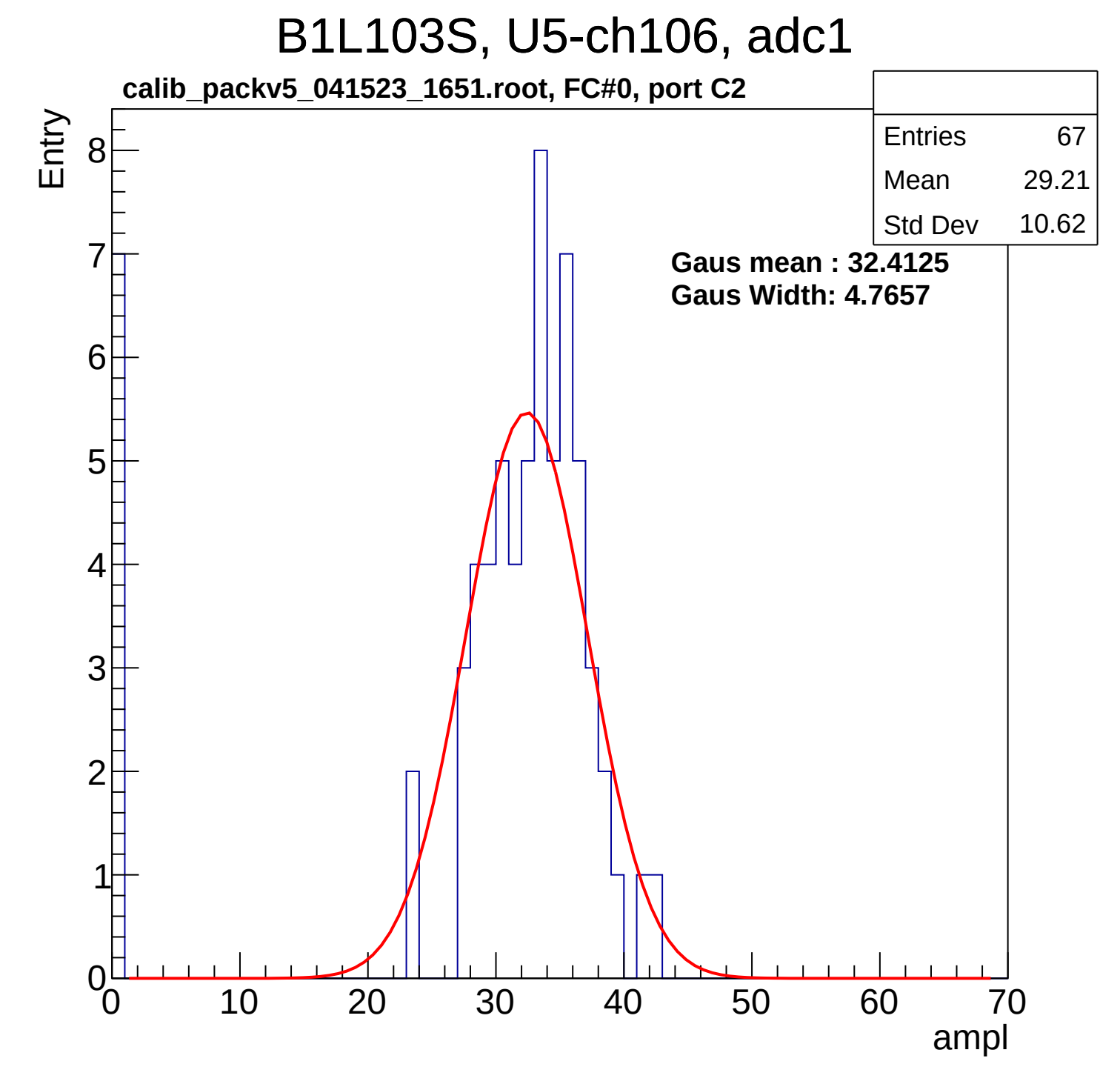
B1L103S, U5-ch106, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 29.21
Std Dev 10.62
Gaus mean : 32.4125
Gaus Width: 4.7657
Entry
ampl
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2
3
4
5
6
7
8
0
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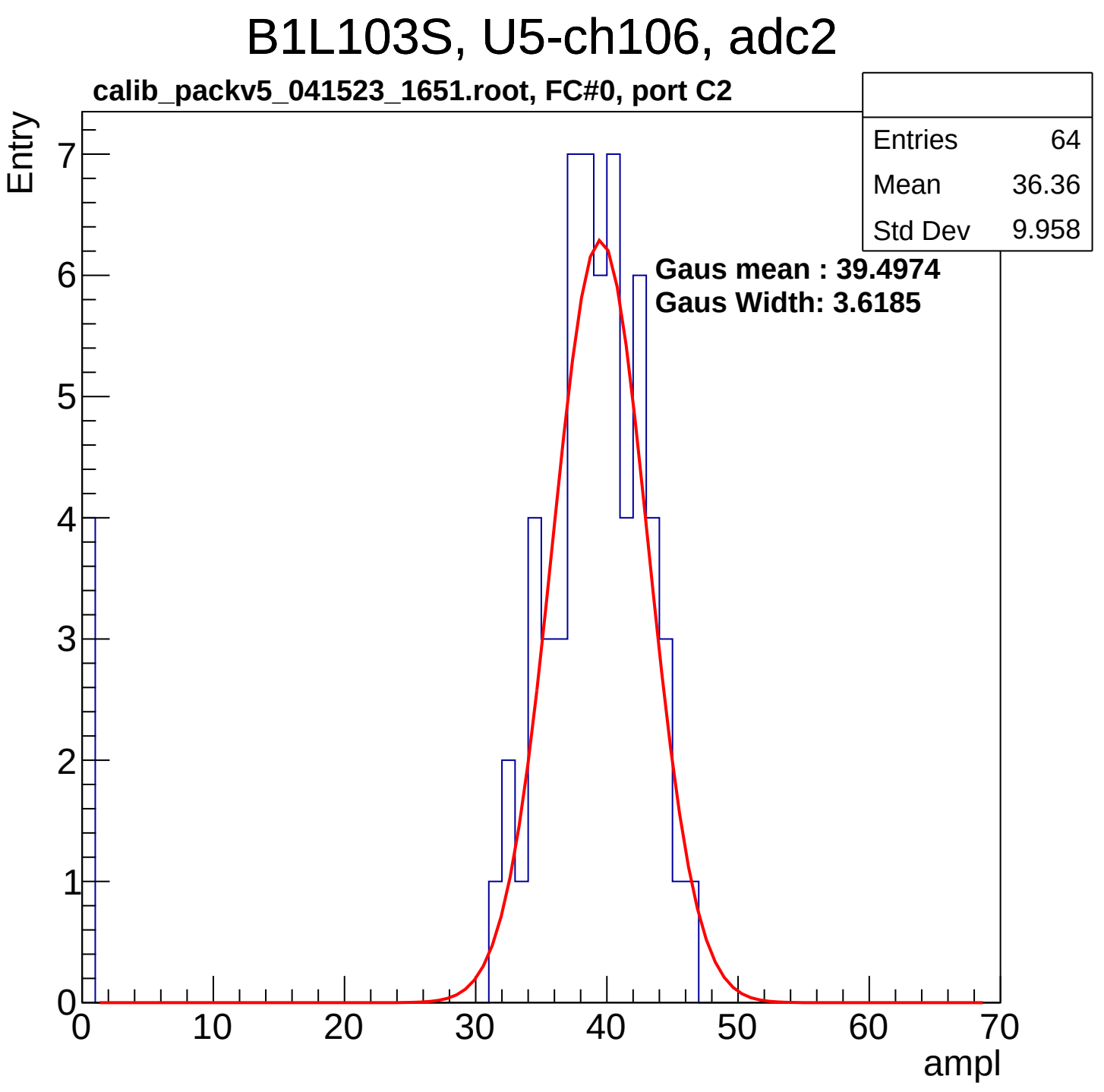
B1L103S, U5-ch106, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 36.36
Std Dev 9.958
Gaus mean : 39.4974
Gaus Width: 3.6185
Entry
ampl
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3
4
5
6
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0
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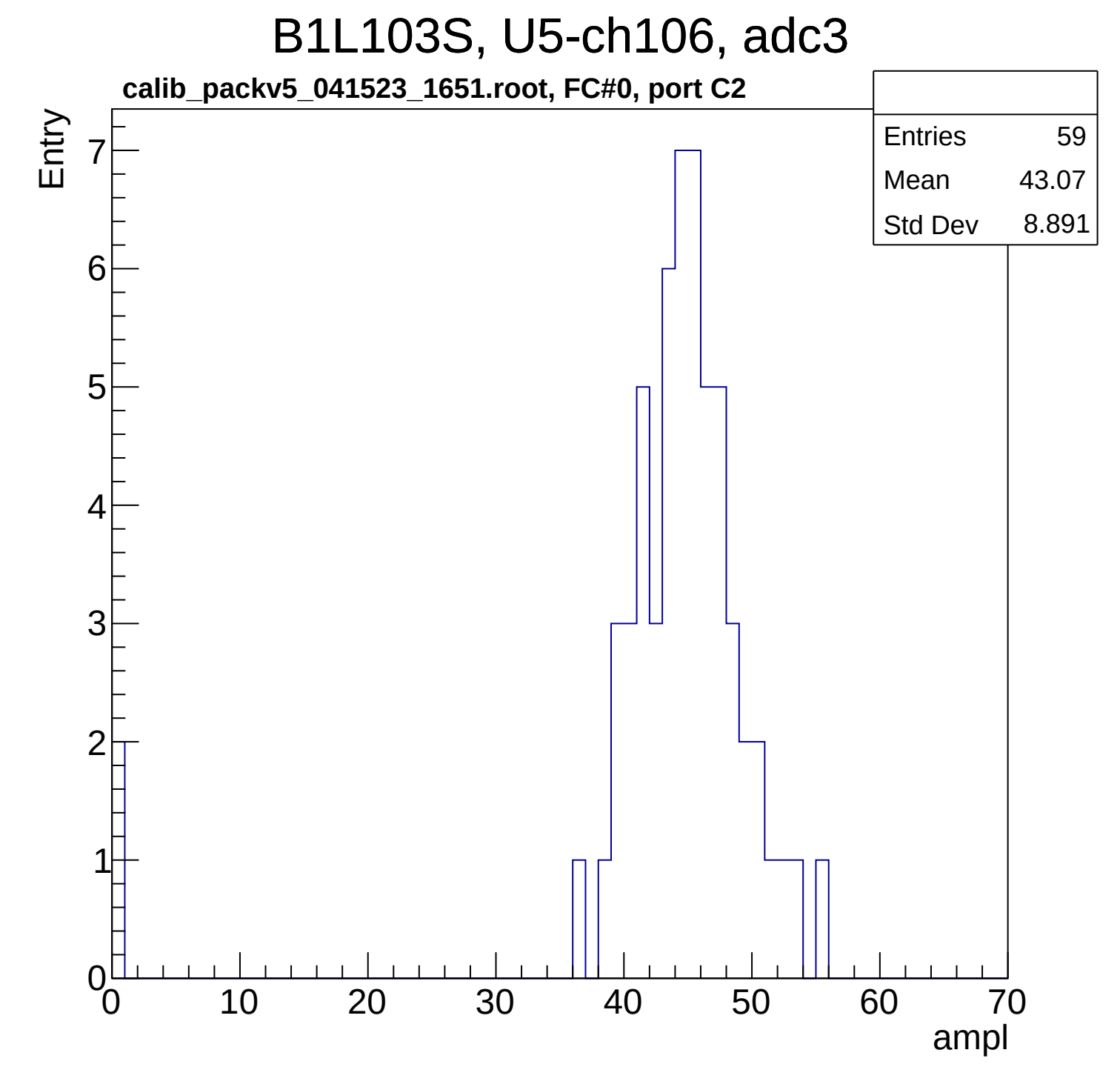
B1L103S, U5-ch106, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 43.07
Std Dev 8.891
Entry
ampl
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2
3
4
5
6
7
0
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20
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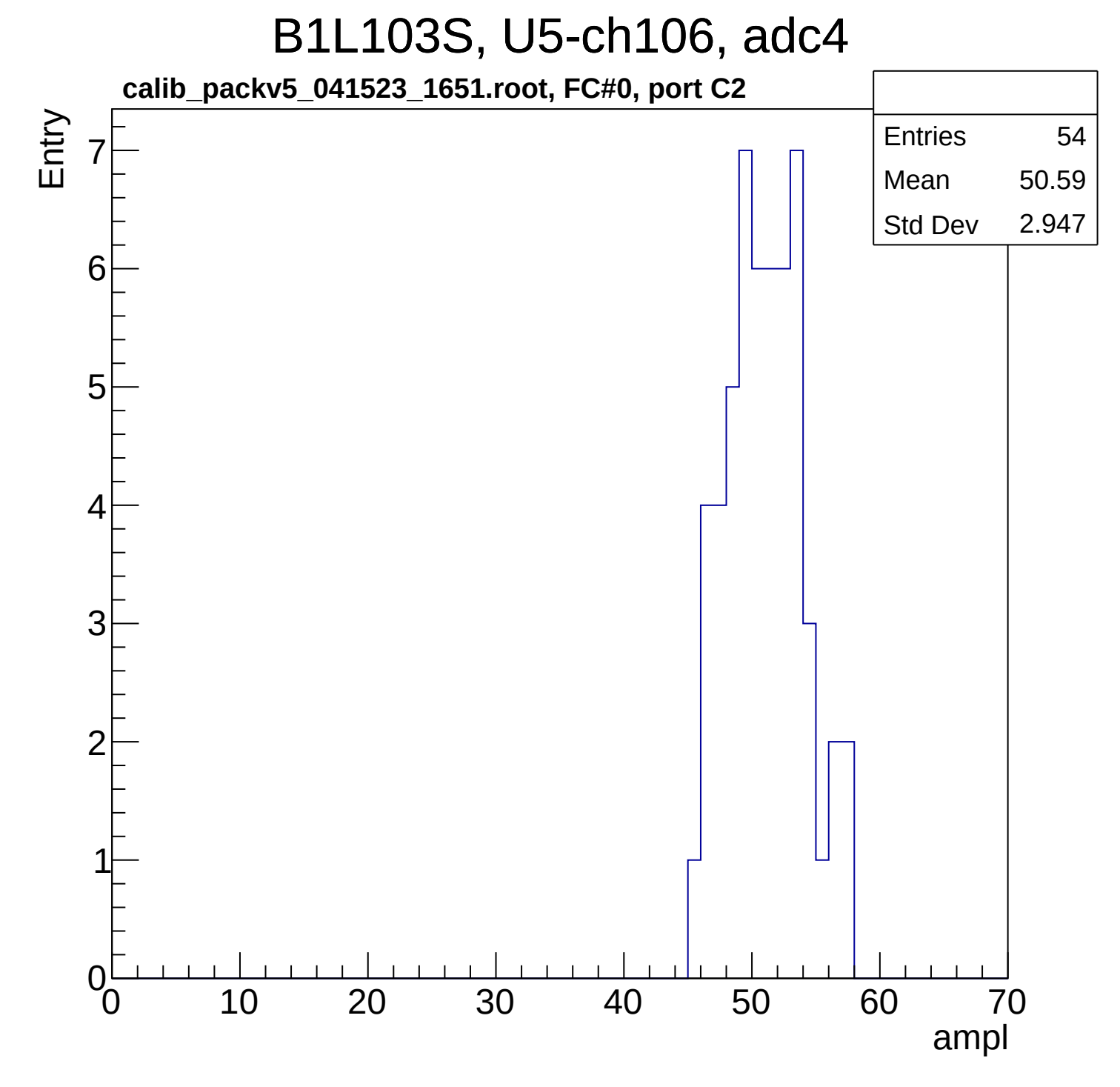
B1L103S, U5-ch106, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 50.59
Std Dev 2.947
Entry
ampl
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1
2
3
4
5
6
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0
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20
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60
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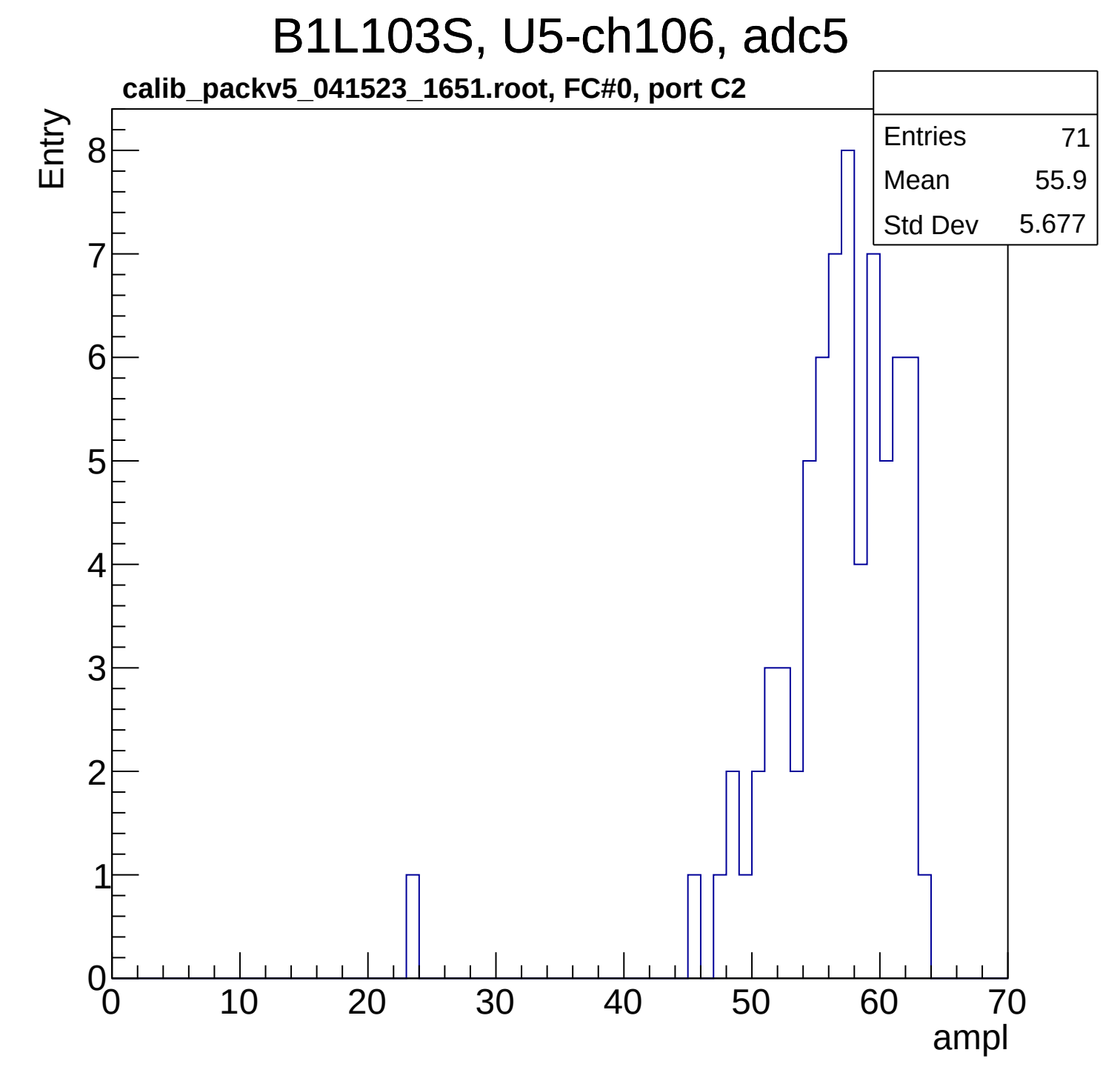
B1L103S, U5-ch106, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 55.9
Std Dev 5.677
Entry
ampl
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0
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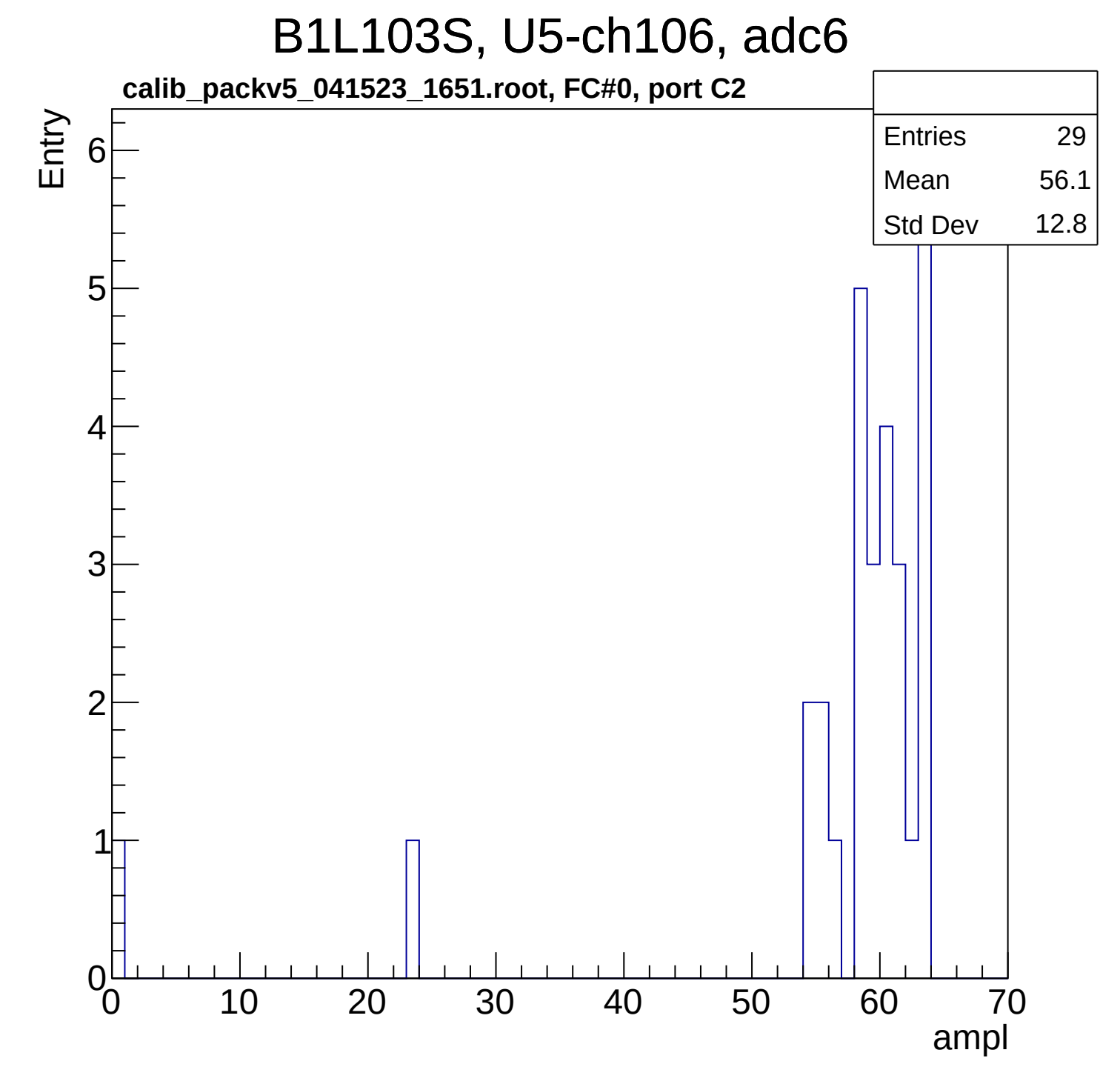
B1L103S, U5-ch106, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 56.1
Std Dev 12.8
Entry
ampl
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3
4
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0
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20
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60
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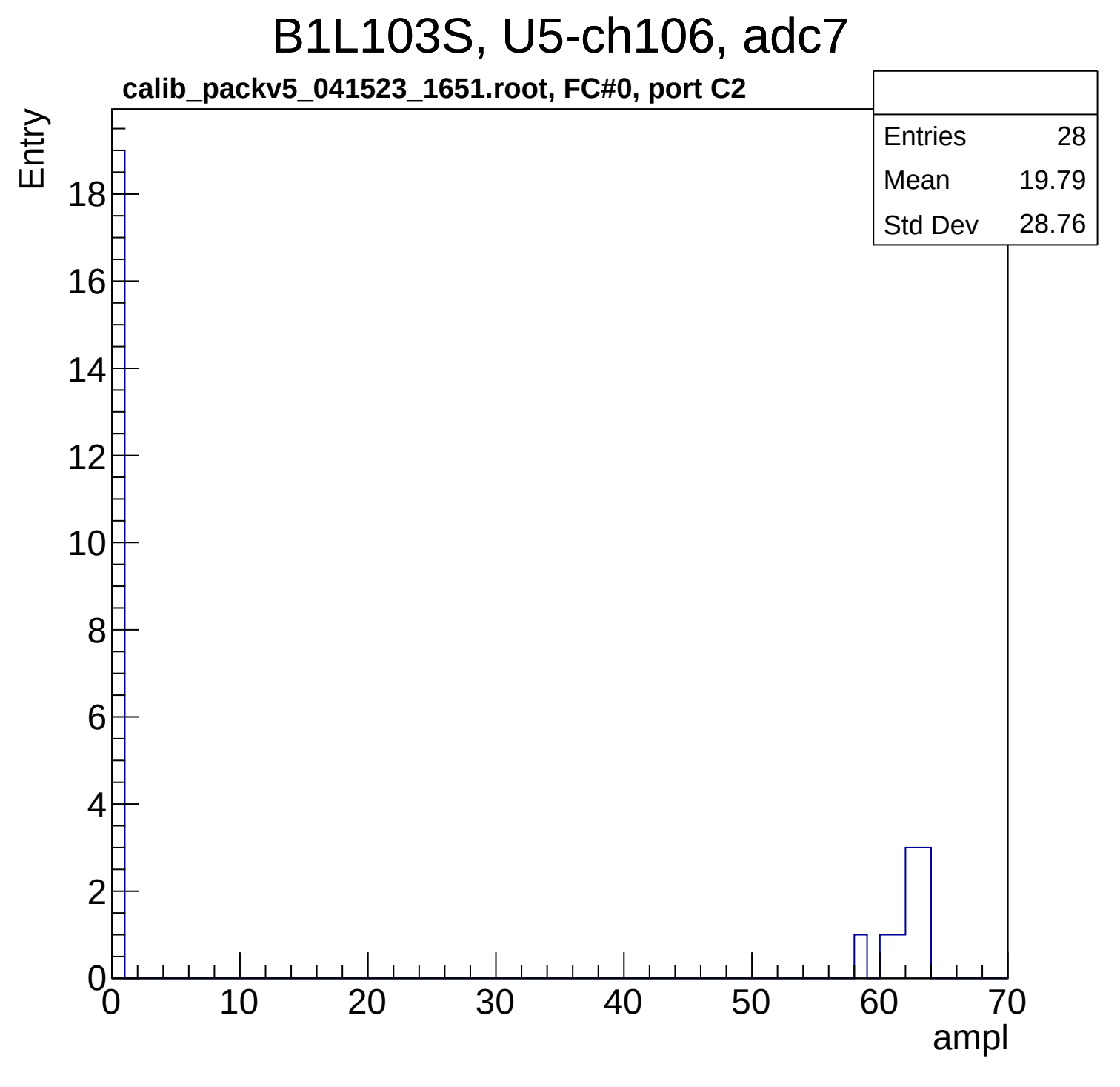
B1L103S, U5-ch106, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 19.79
Std Dev 28.76
Entry
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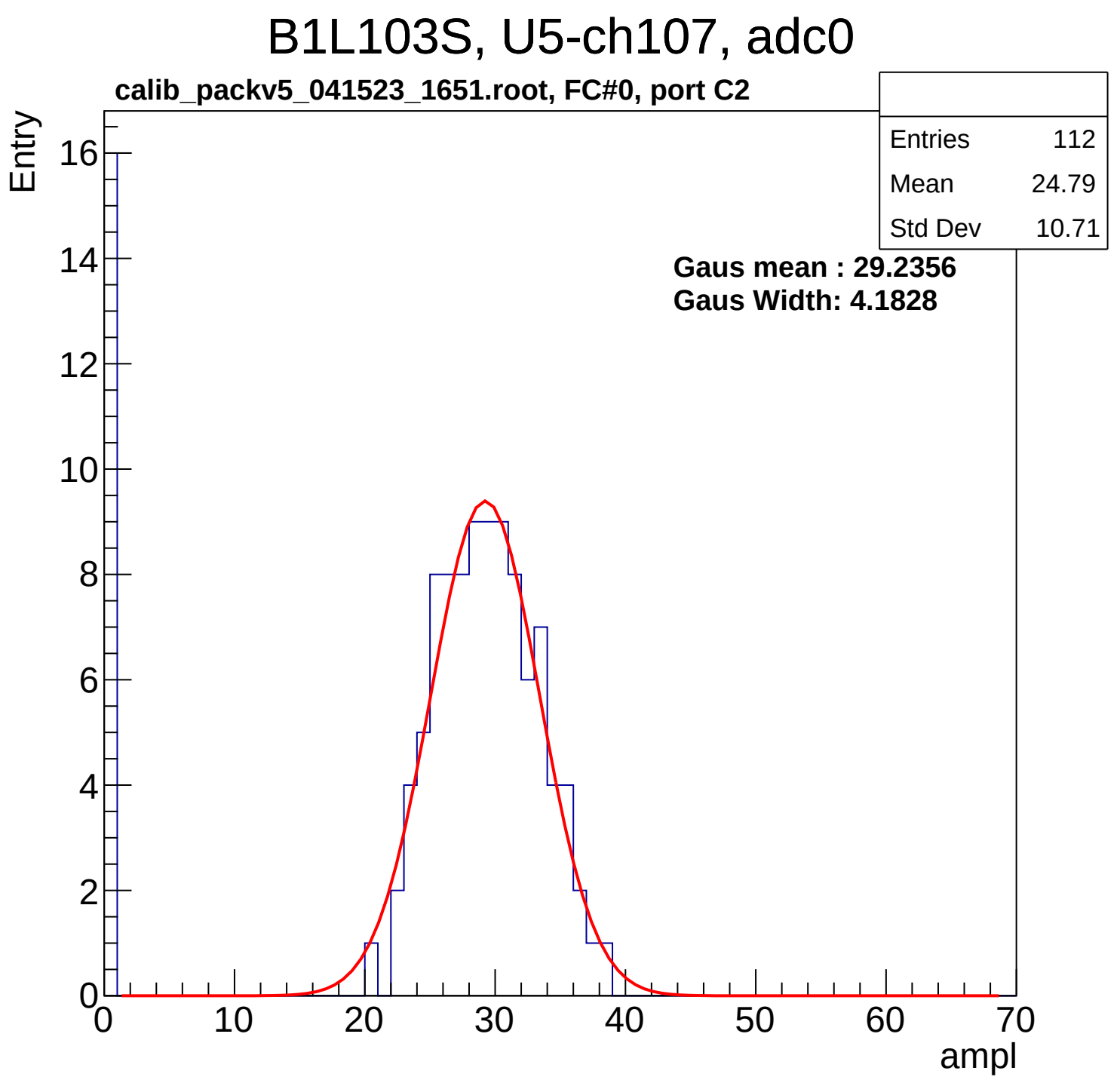
ampl


B1L103S, U5-ch107, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 112
Mean 24.79
Std Dev 10.71
Gaus mean : 29.2356
Gaus Width: 4.1828
Entry
ampl
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4
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8
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0
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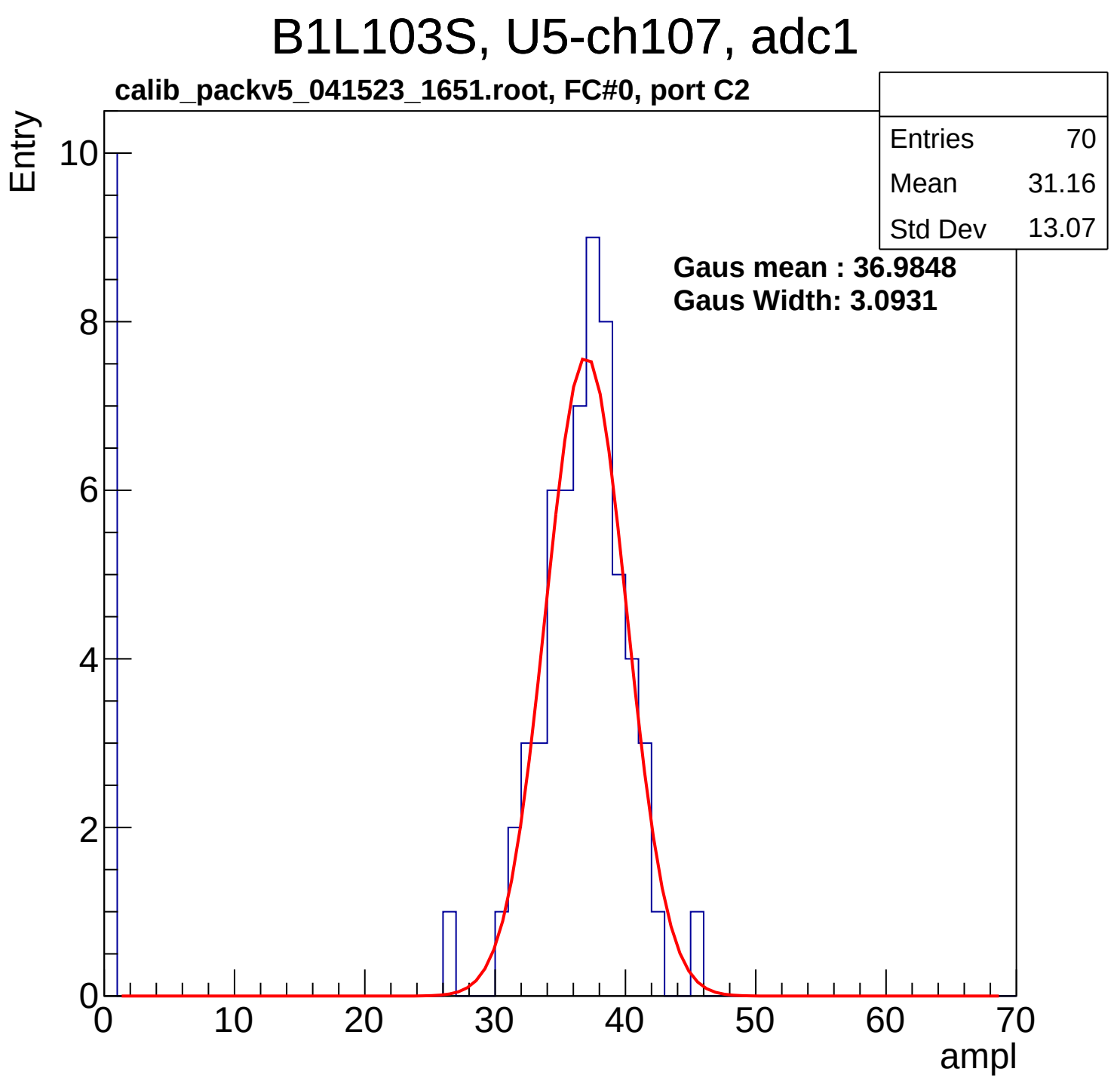
B1L103S, U5-ch107, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 31.16
Std Dev 13.07
Gaus mean : 36.9848
Gaus Width: 3.0931
Entry
ampl
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0
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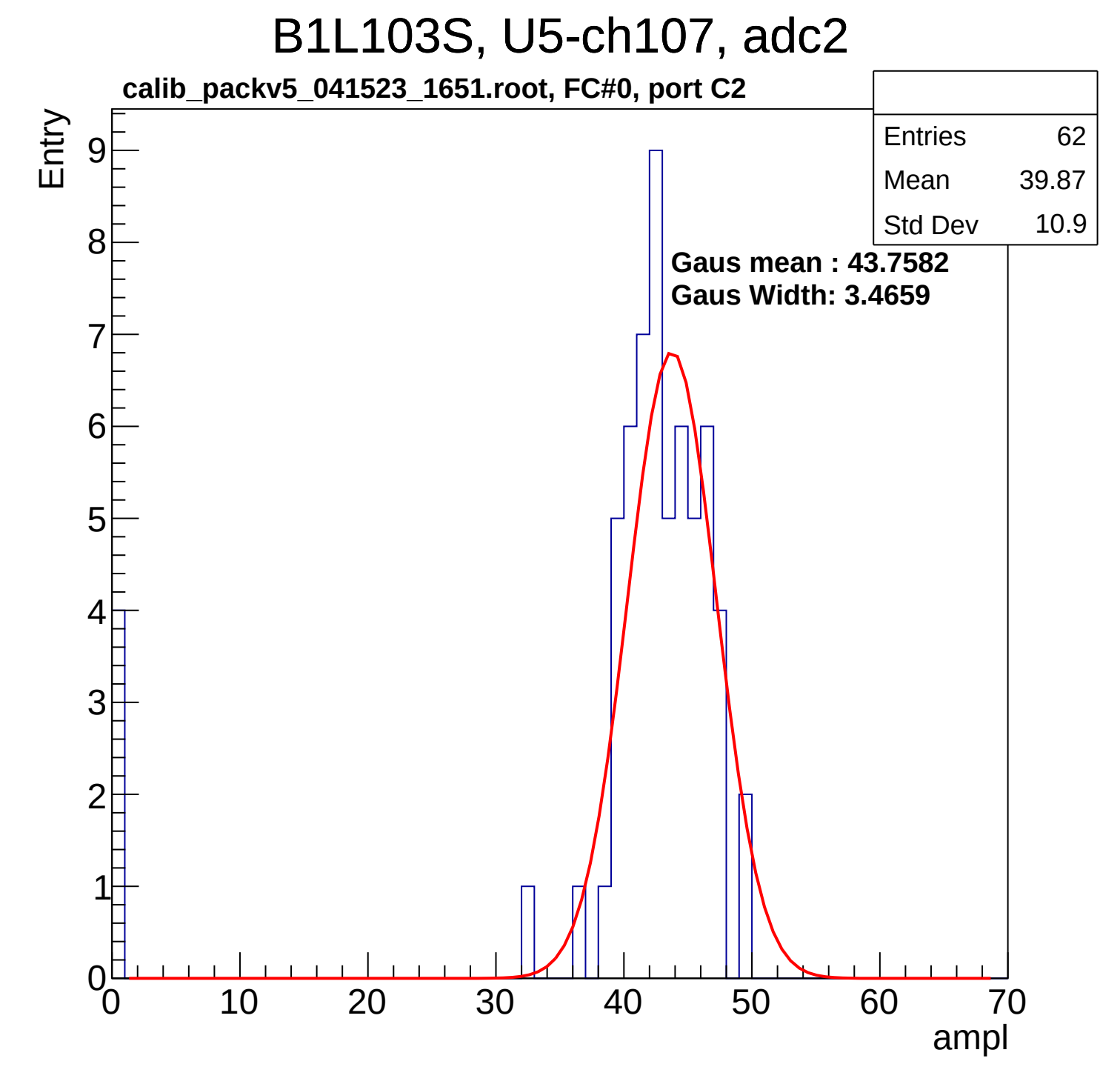
B1L103S, U5-ch107, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 39.87
Std Dev 10.9
Gaus mean : 43.7582
Gaus Width: 3.4659
Entry
ampl
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5
6
7
8
9
0
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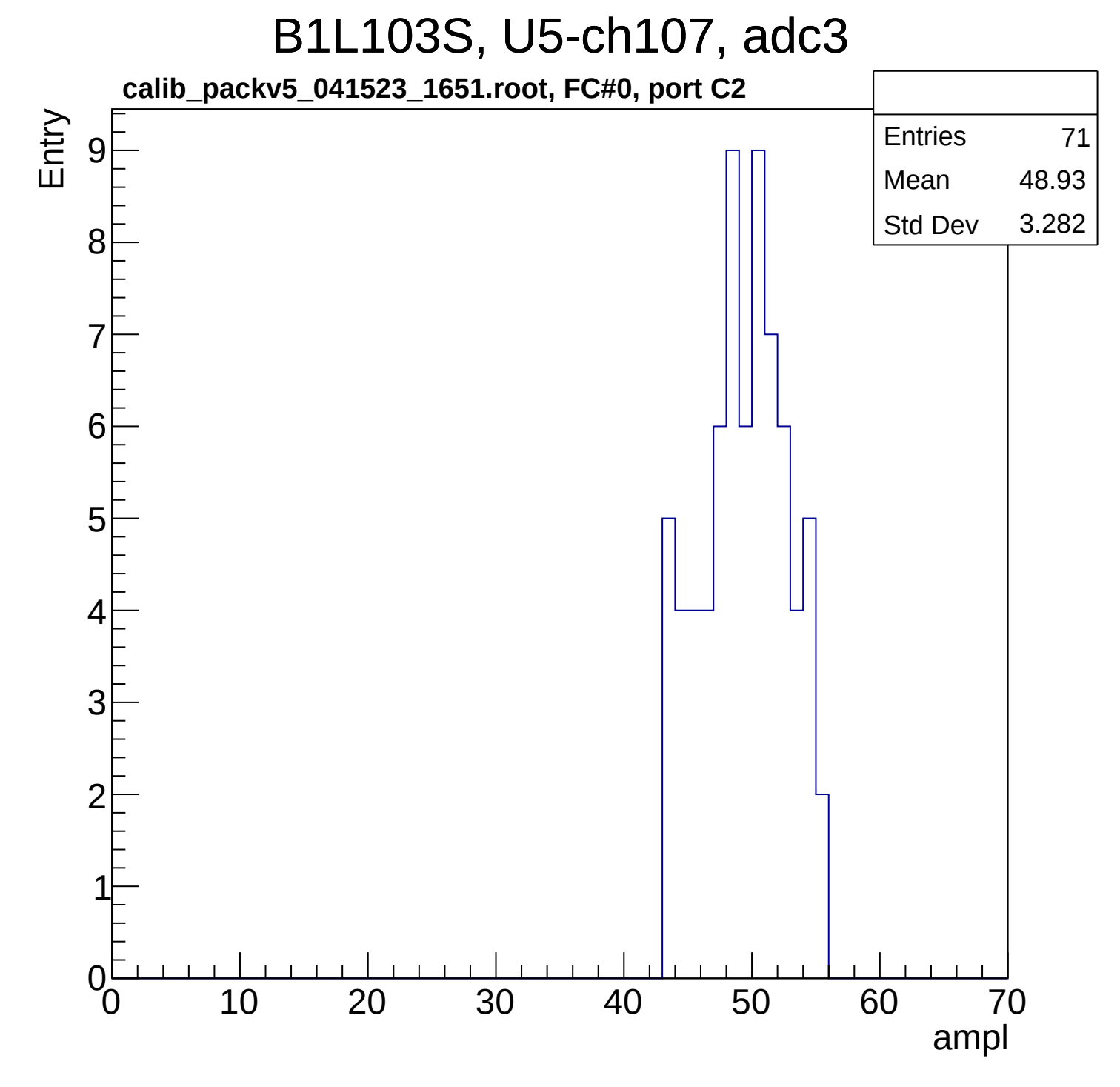
B1L103S, U5-ch107, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 48.93
Std Dev 3.282
Entry
ampl
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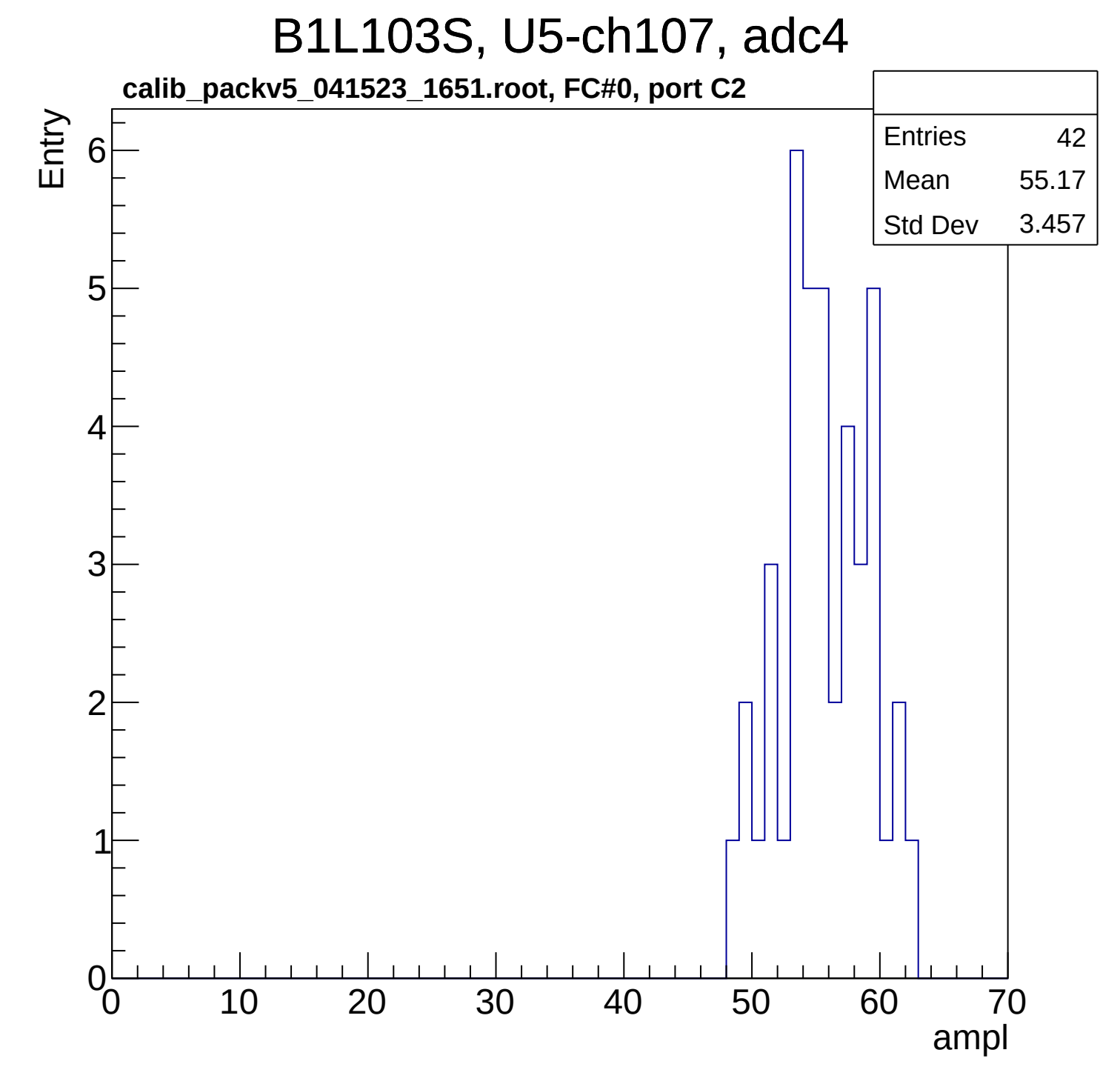
B1L103S, U5-ch107, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 55.17
Std Dev 3.457
Entry
ampl
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0
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60
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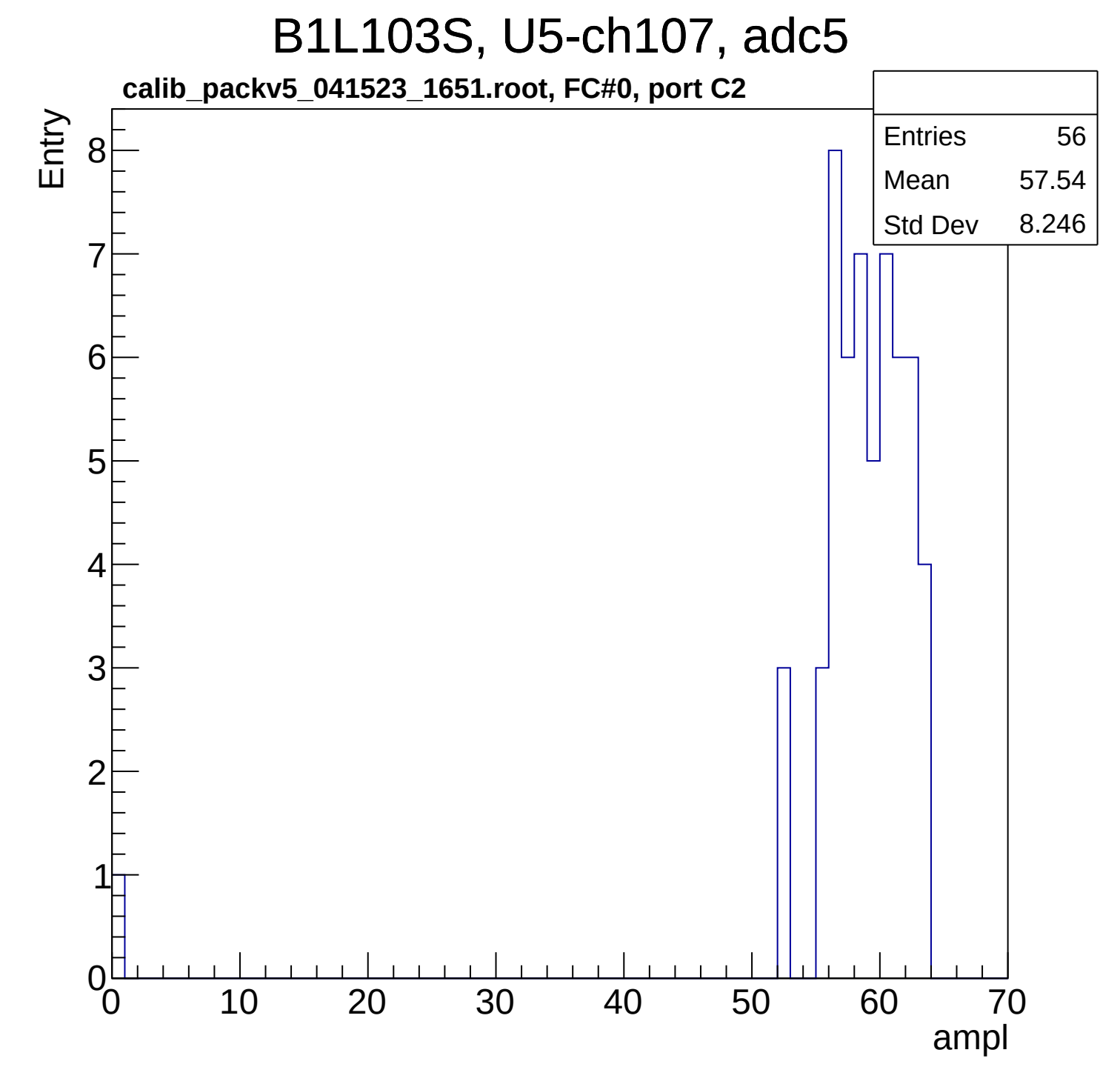
B1L103S, U5-ch107, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 57.54
Std Dev 8.246
Entry
ampl
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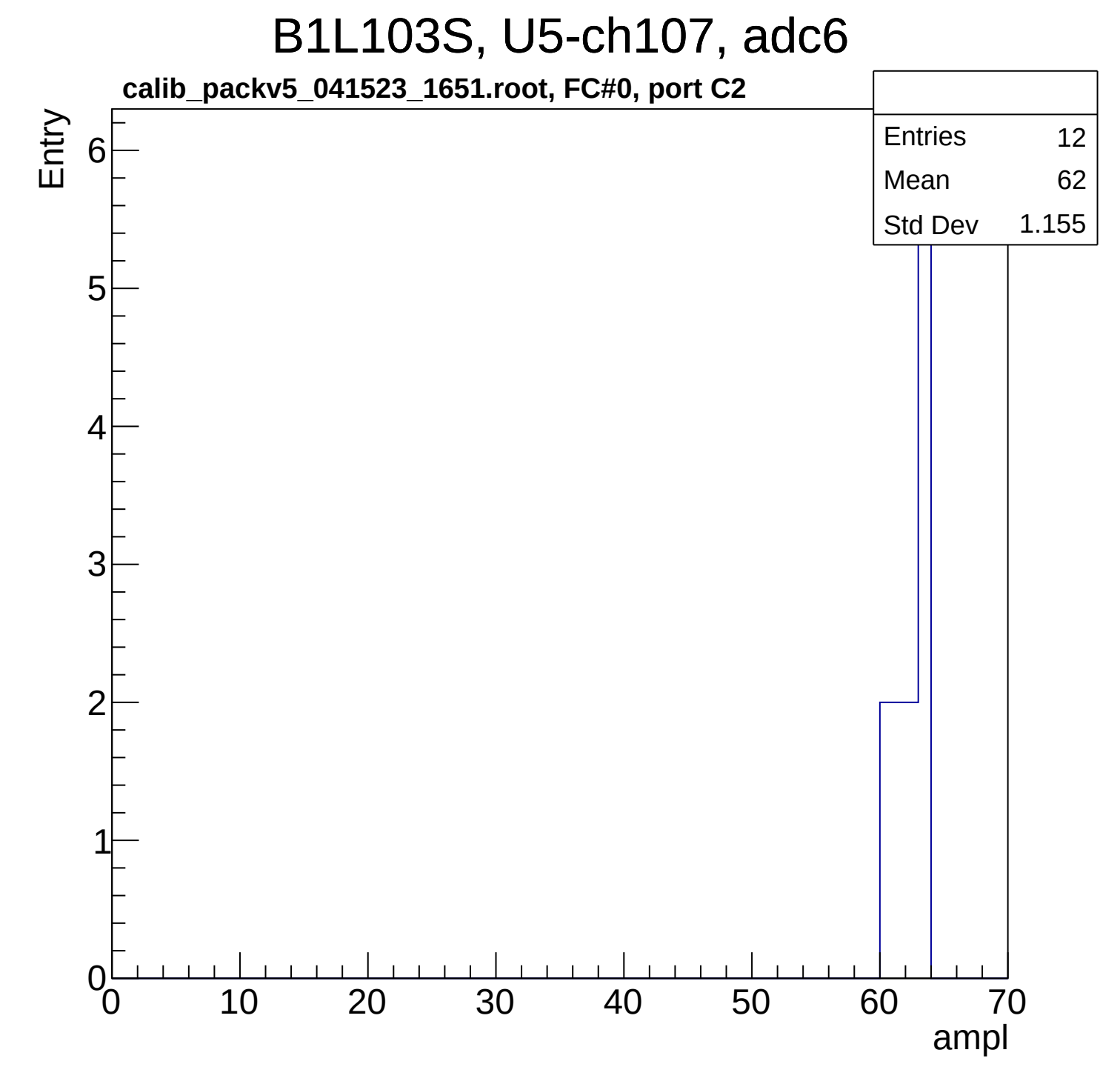
B1L103S, U5-ch107, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 62
Std Dev 1.155
Entry
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4
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10
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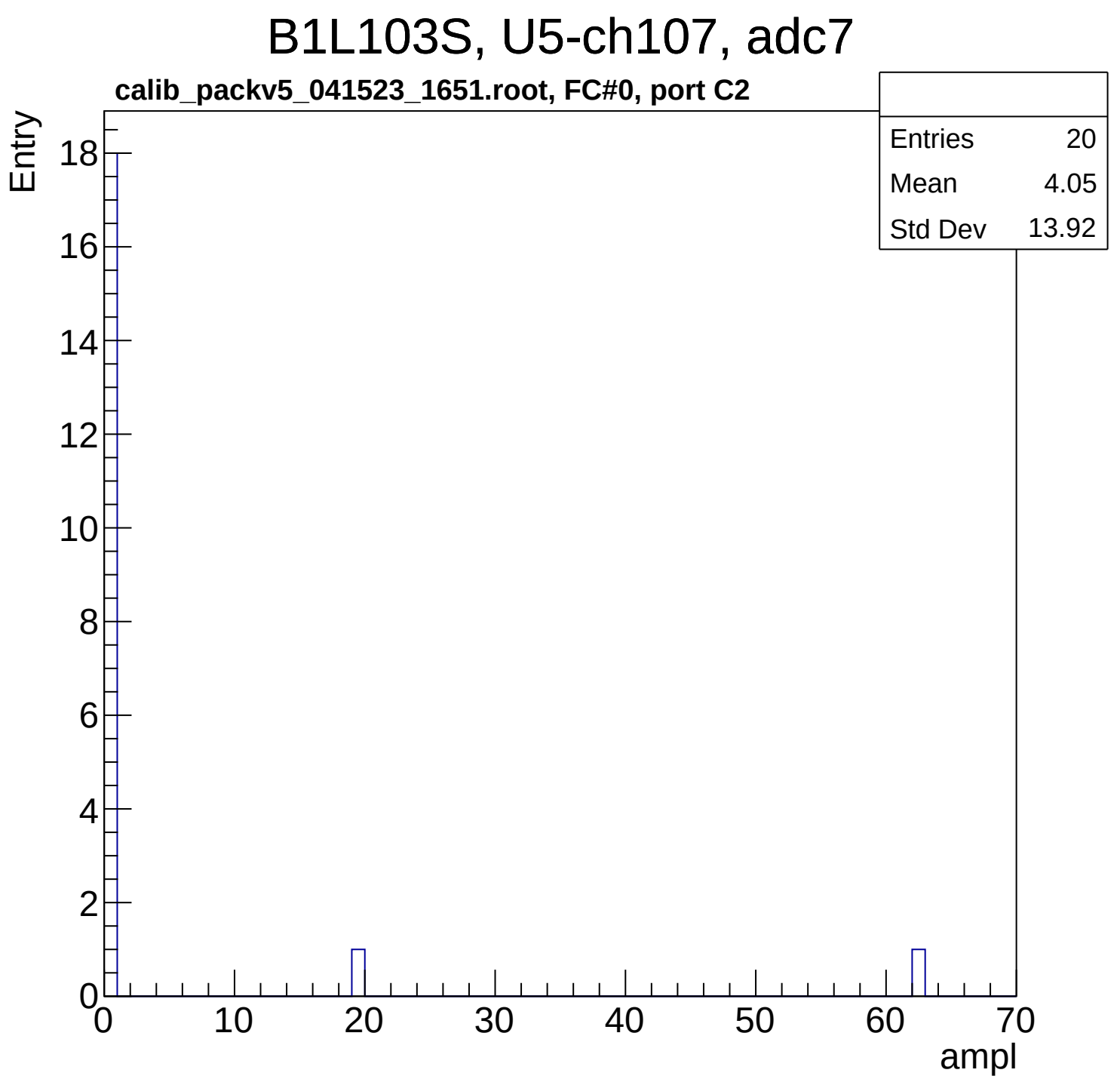
50
60
70
ampl


B1L103S, U5-ch107, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.05
Std Dev 13.92
Entry
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10
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10
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30
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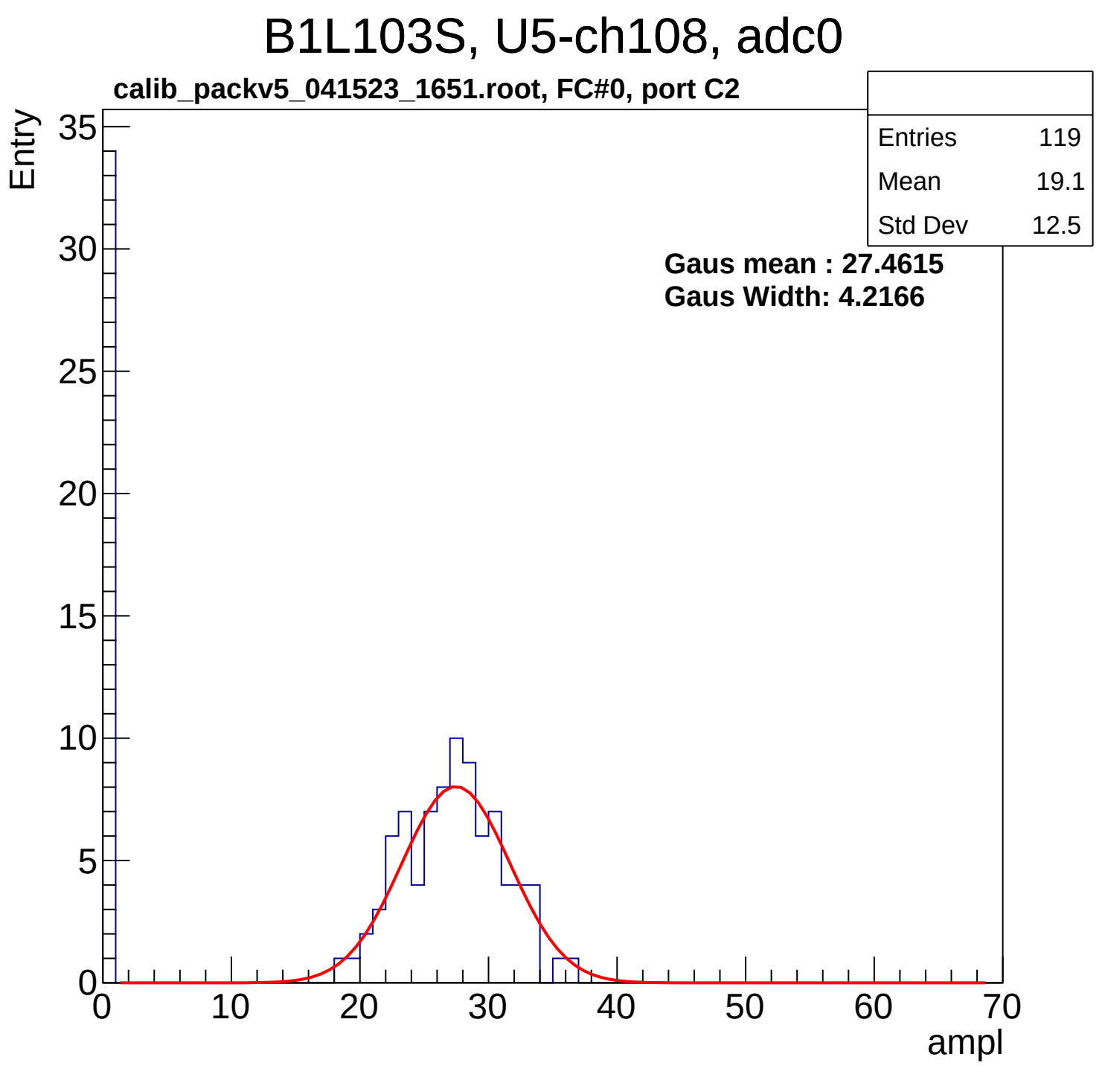
50
60
70
ampl


B1L103S, U5-ch108, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 119
Mean 19.1
Std Dev 12.5
Gaus mean : 27.4615
Gaus Width: 4.2166
Entry
ampl
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5
10
15
20
25
30
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0
10
20
30
40
50
60
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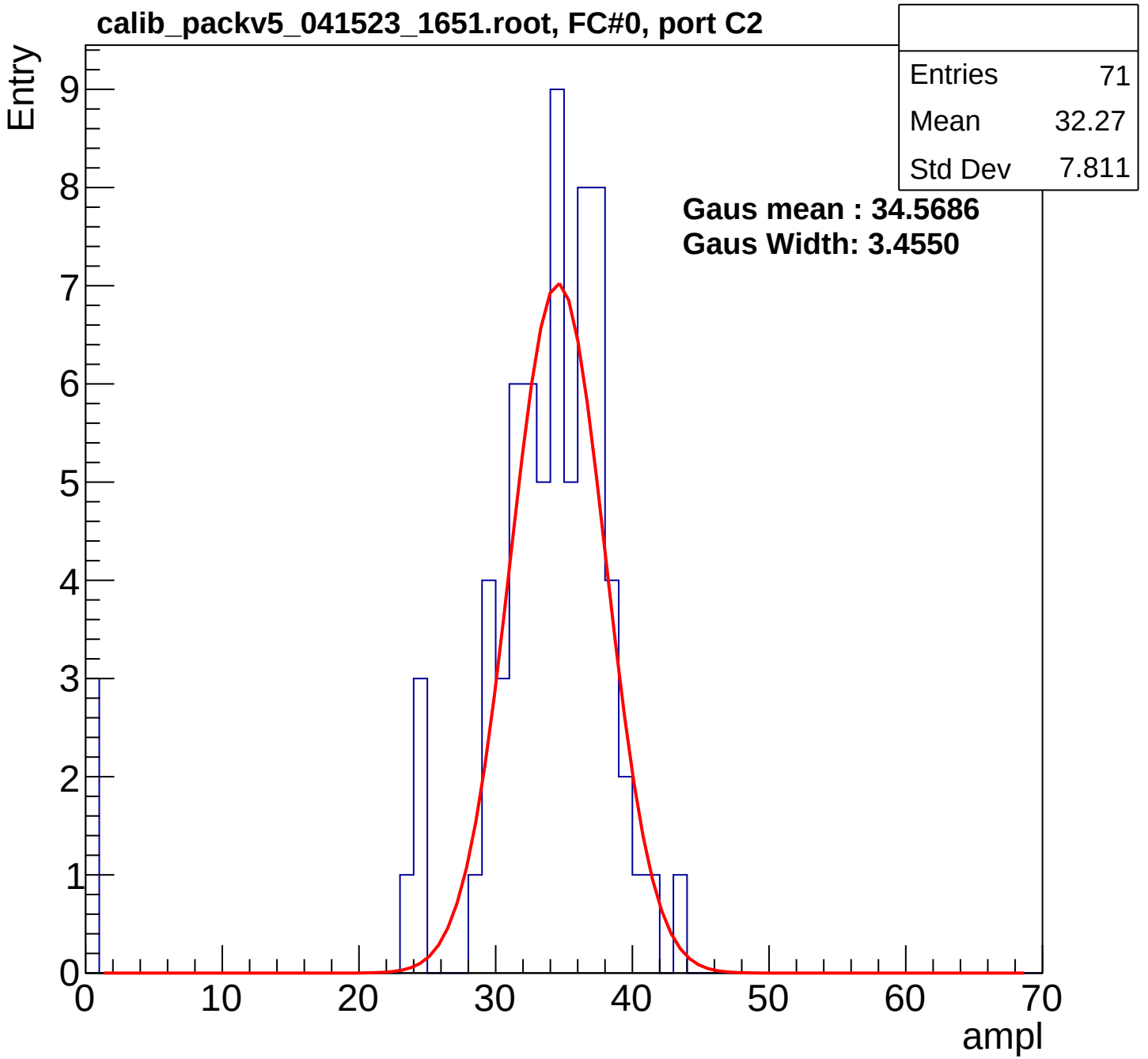
B1L103S, U5-ch108, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 32.27
Std Dev 7.811
Gaus mean : 34.5686
Gaus Width: 3.4550
Entry
ampl
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7
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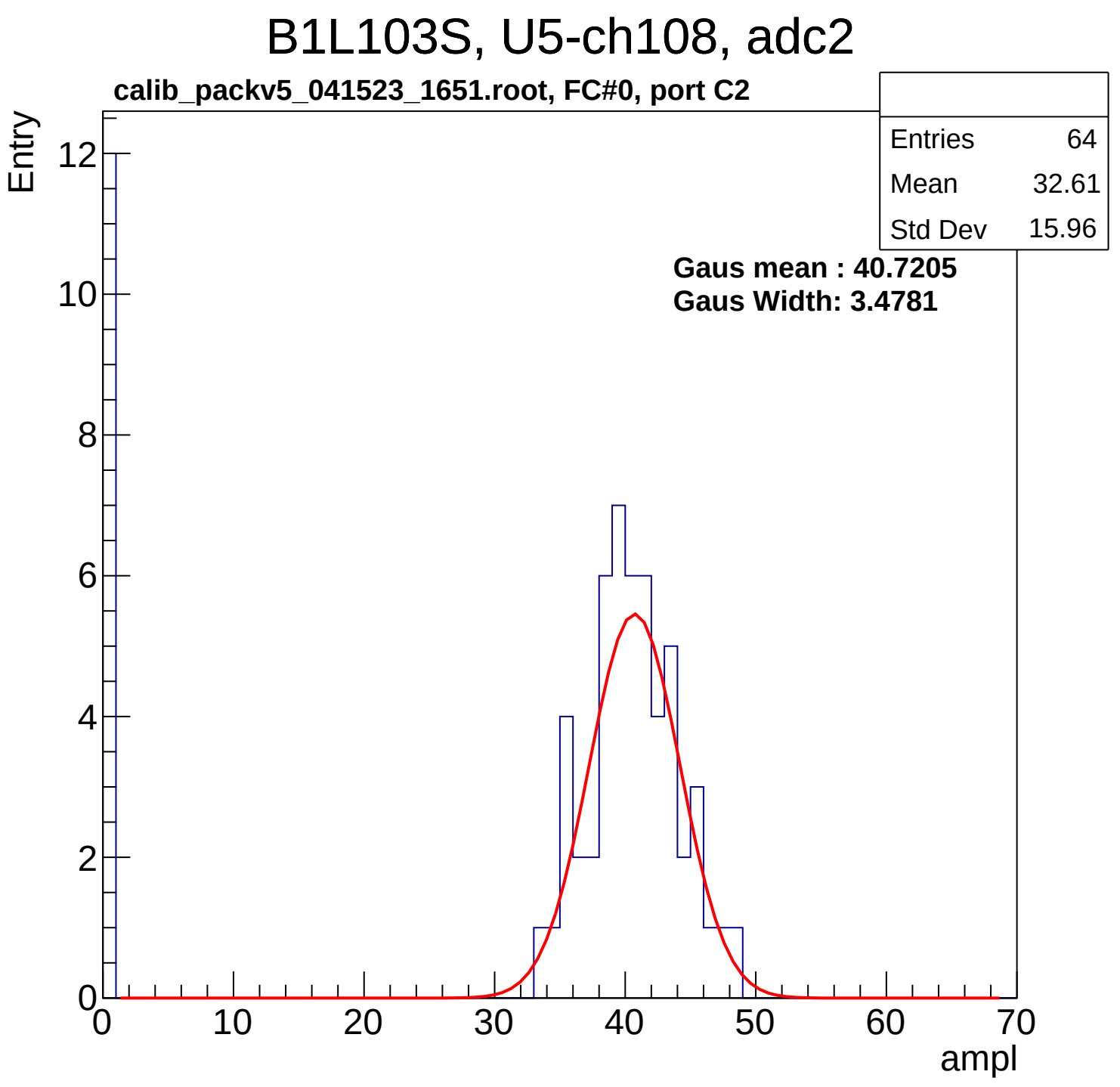
B1L103S, U5-ch108, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 32.61
Std Dev 15.96
Gaus mean : 40.7205
Gaus Width: 3.4781
Entry
ampl
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8
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12
0
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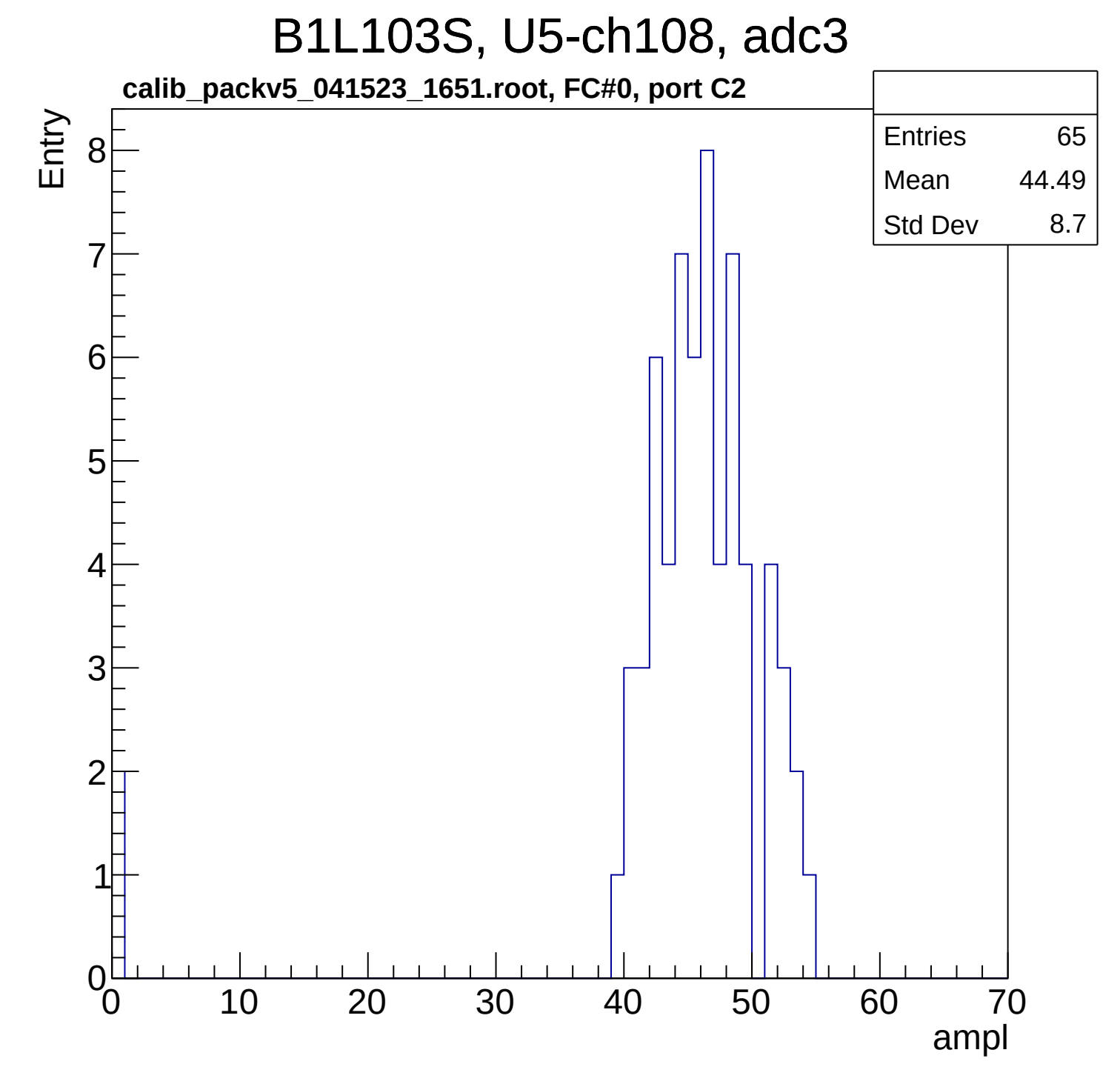
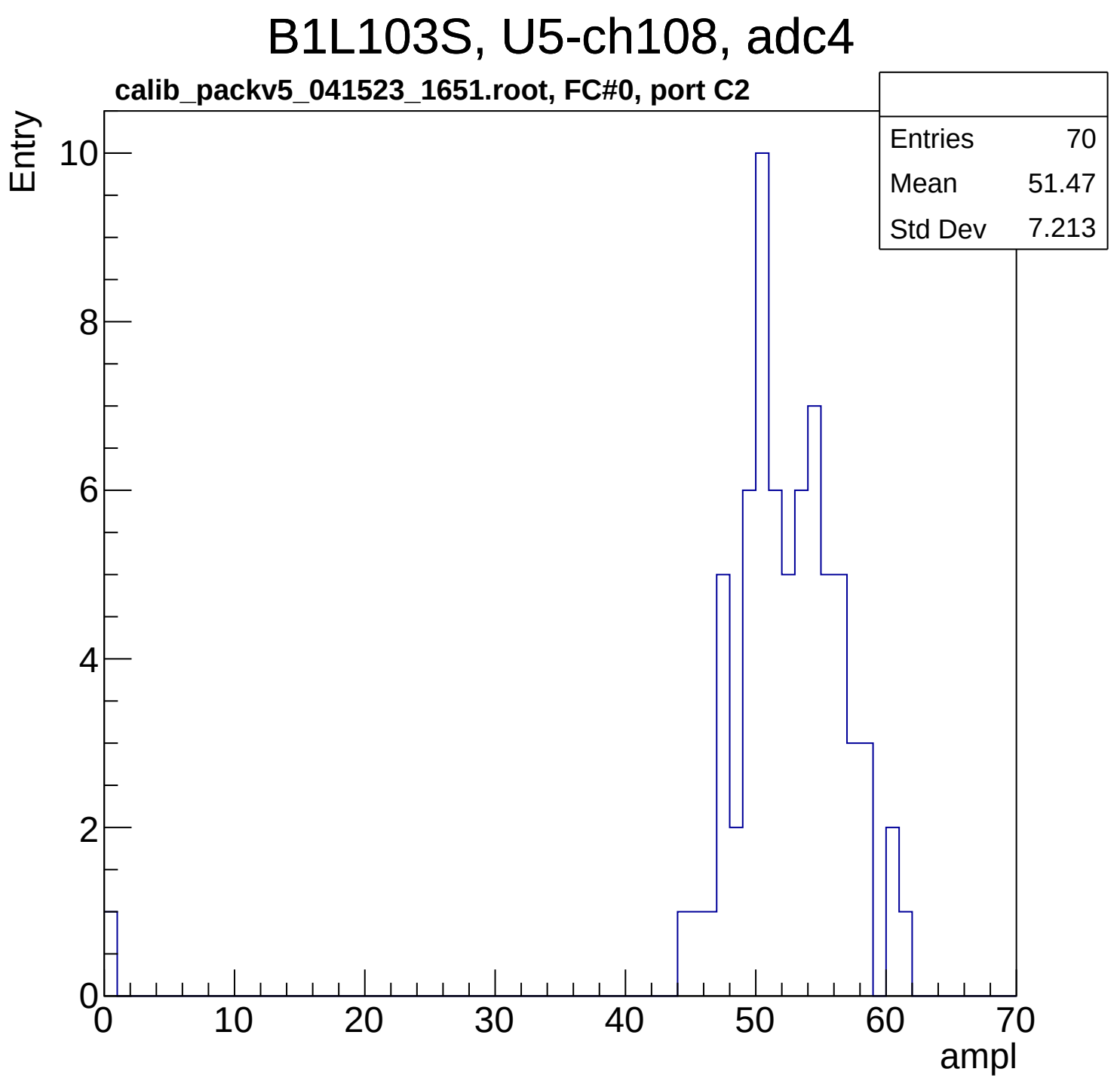

B1L103S, U5-ch108, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 44.49
Std Dev 8.7
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U5-ch108, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 51.47
Std Dev 7.213
Entry
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2
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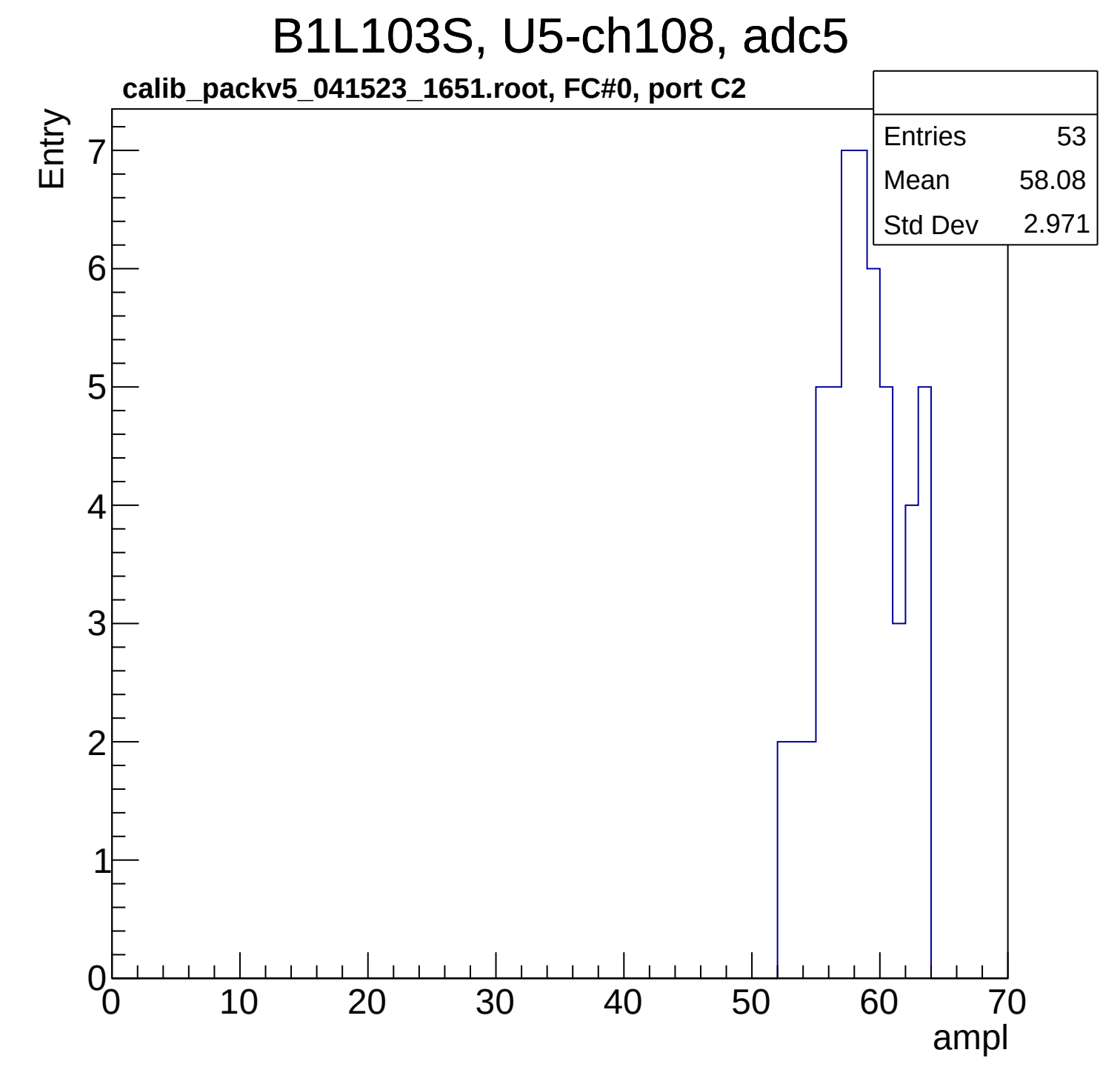
70
ampl


B1L103S, U5-ch108, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.08
Std Dev 2.971
Entry
ampl
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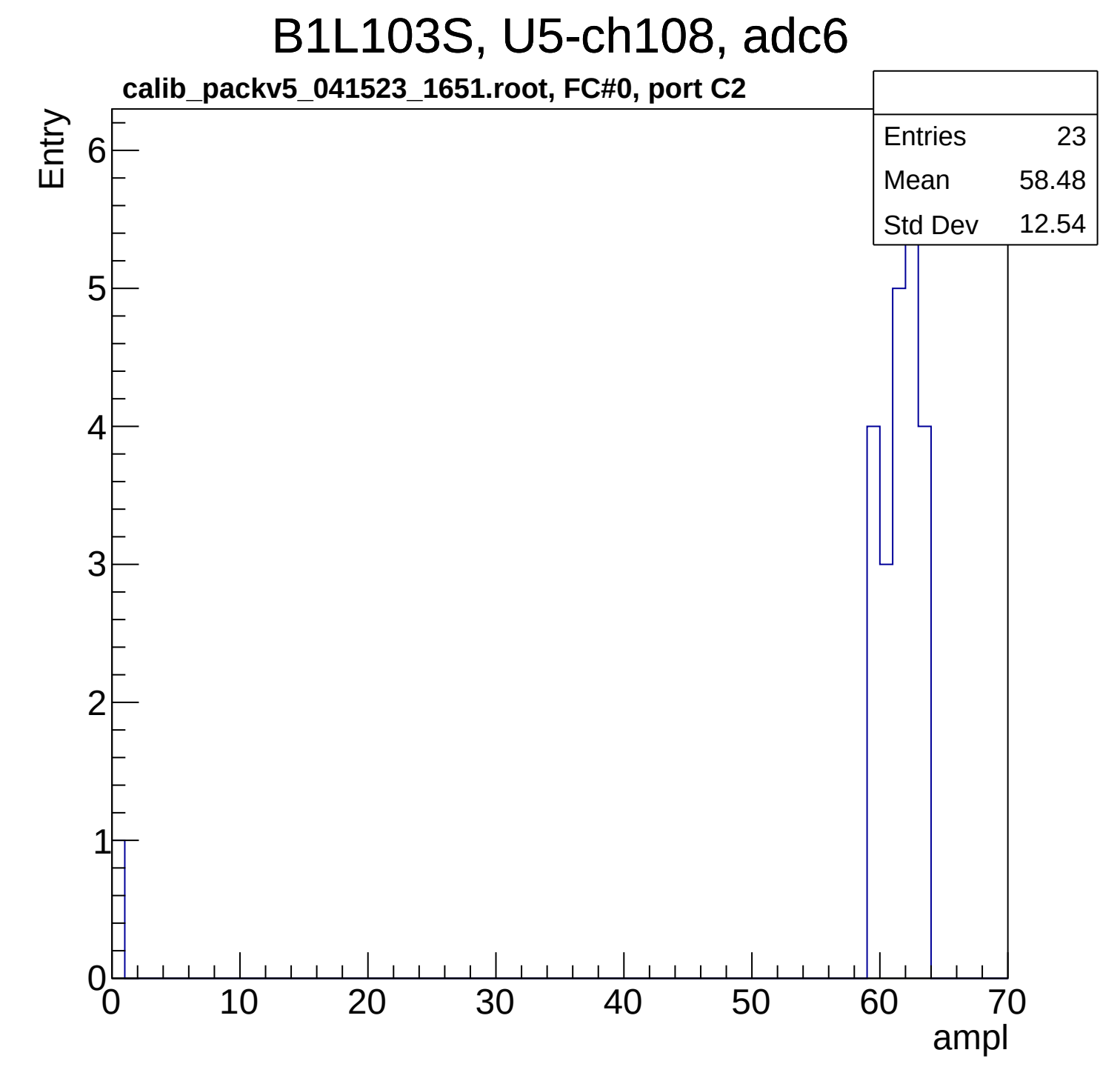
B1L103S, U5-ch108, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 58.48
Std Dev 12.54
Entry
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2
3
4
5
6
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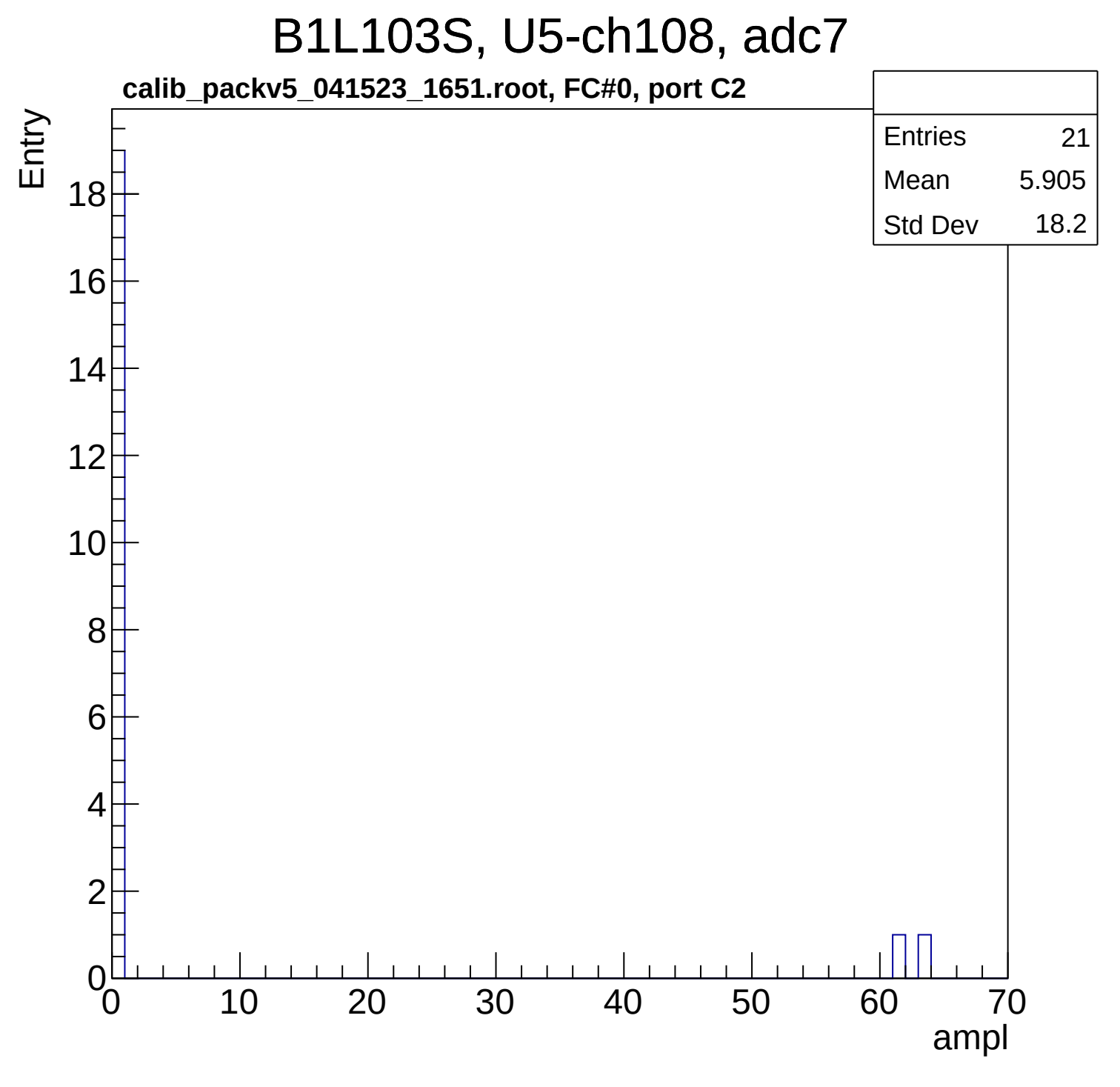
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch108, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
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6
8
10
12
14
16
18
0
10
20
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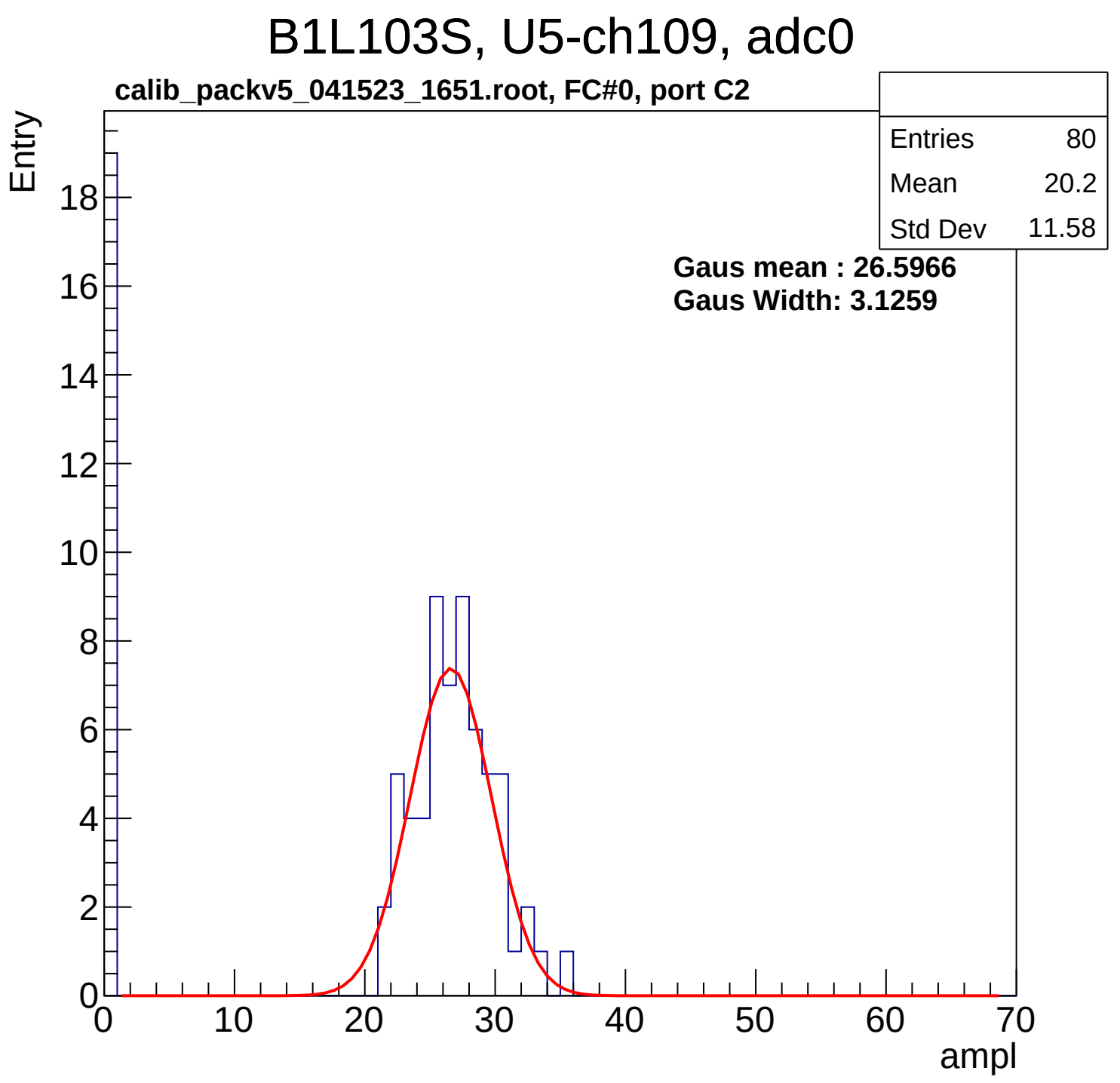
50
60
70
ampl


B1L103S, U5-ch109, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 20.2
Std Dev 11.58
Gaus mean : 26.5966
Gaus Width: 3.1259
Entry
ampl
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2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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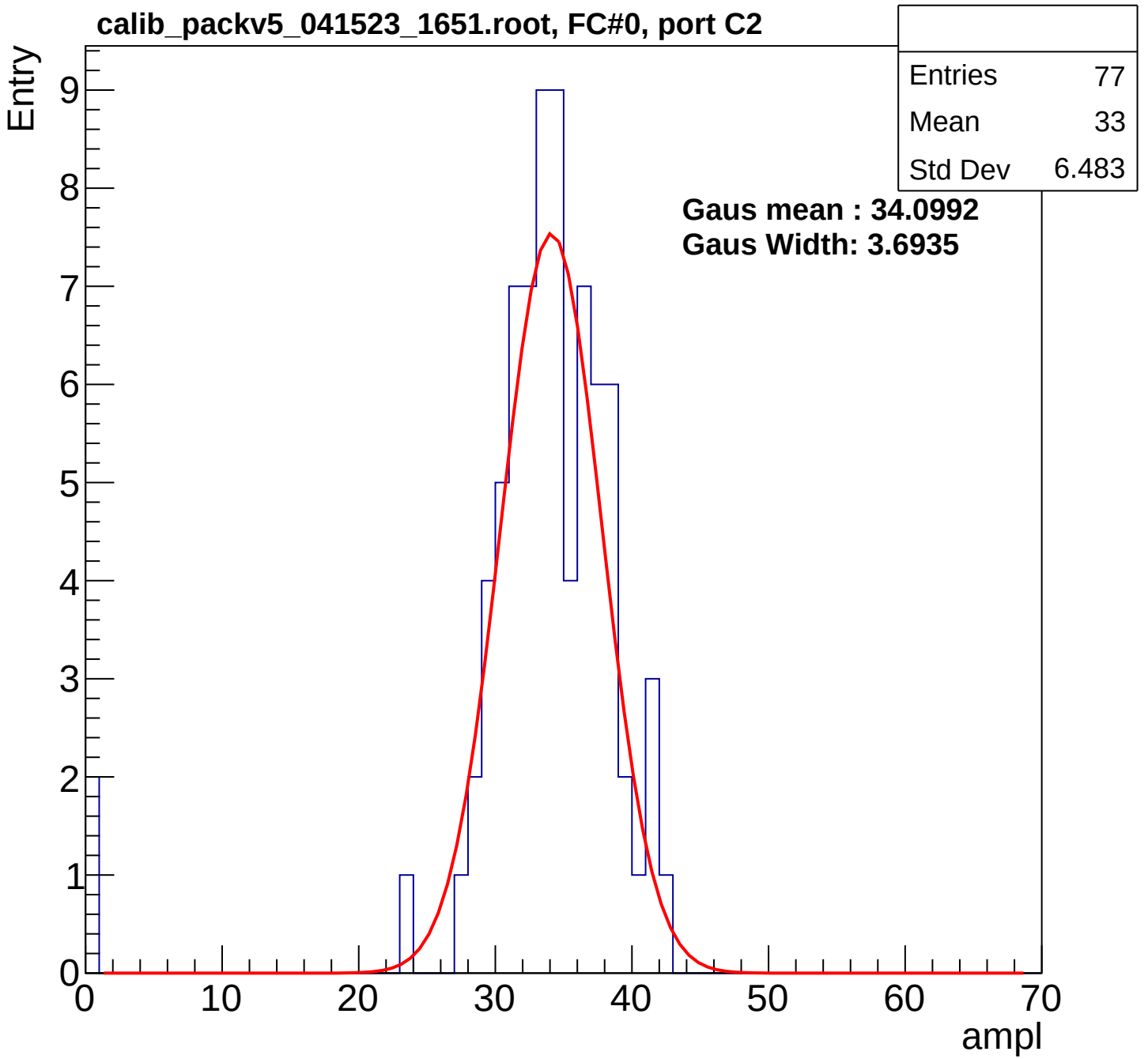
B1L103S, U5-ch109, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 33
Std Dev 6.483
Gaus mean : 34.0992
Gaus Width: 3.6935
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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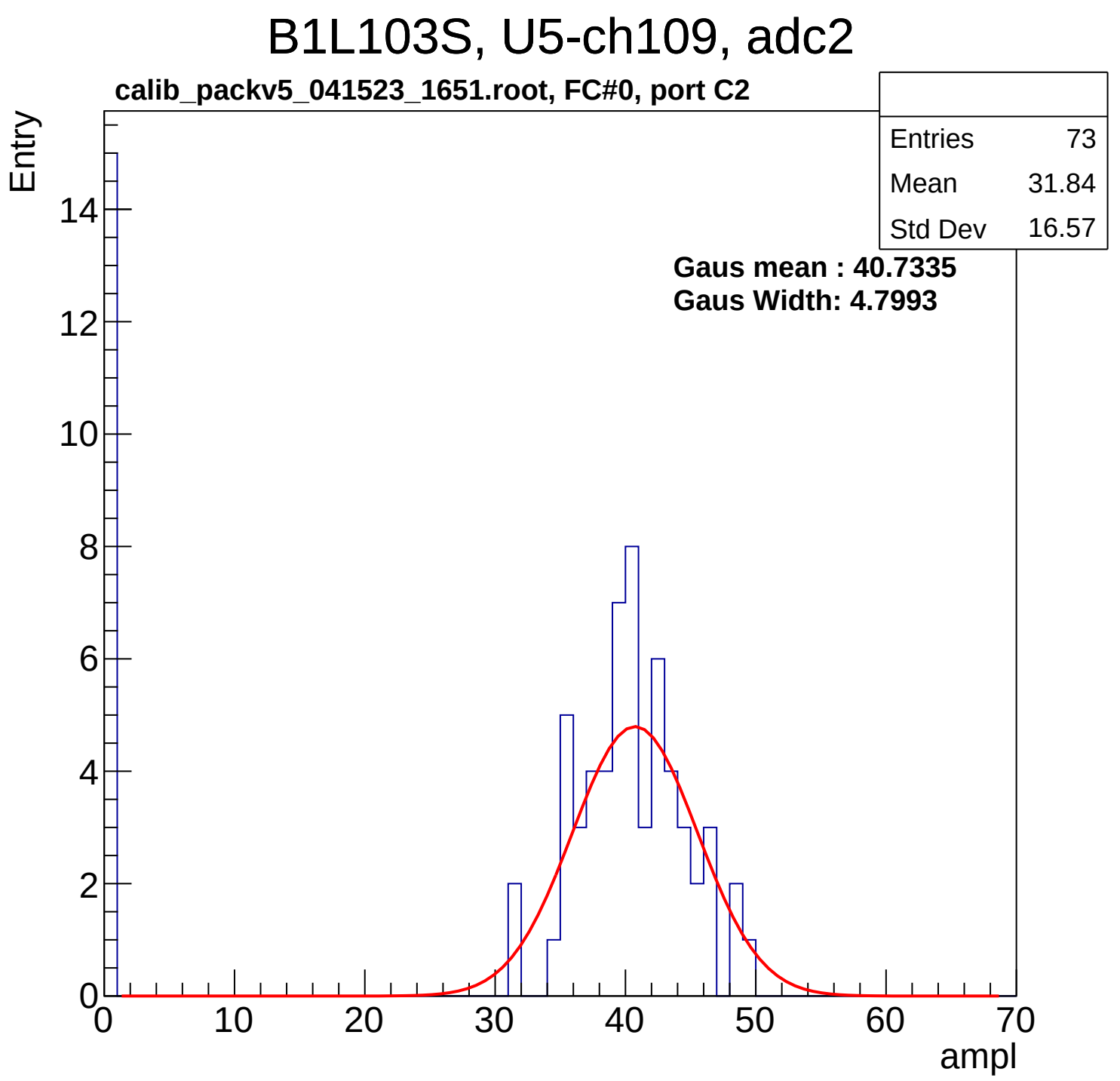
B1L103S, U5-ch109, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 31.84
Std Dev 16.57
Gaus mean : 40.7335
Gaus Width: 4.7993
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
50
60
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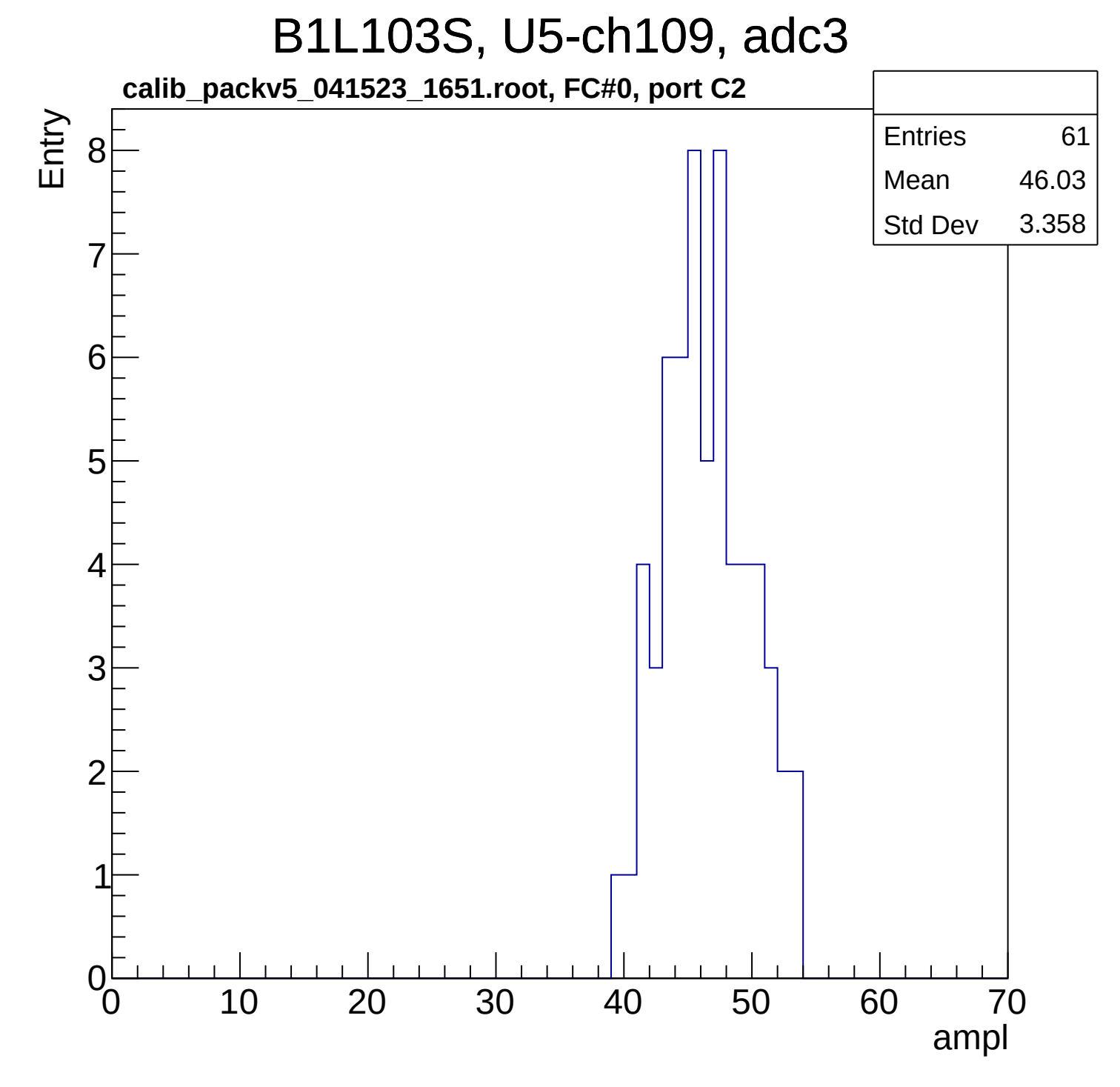
B1L103S, U5-ch109, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 46.03
Std Dev 3.358
Entry
ampl
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2
3
4
5
6
7
8
0
10
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40
50
60
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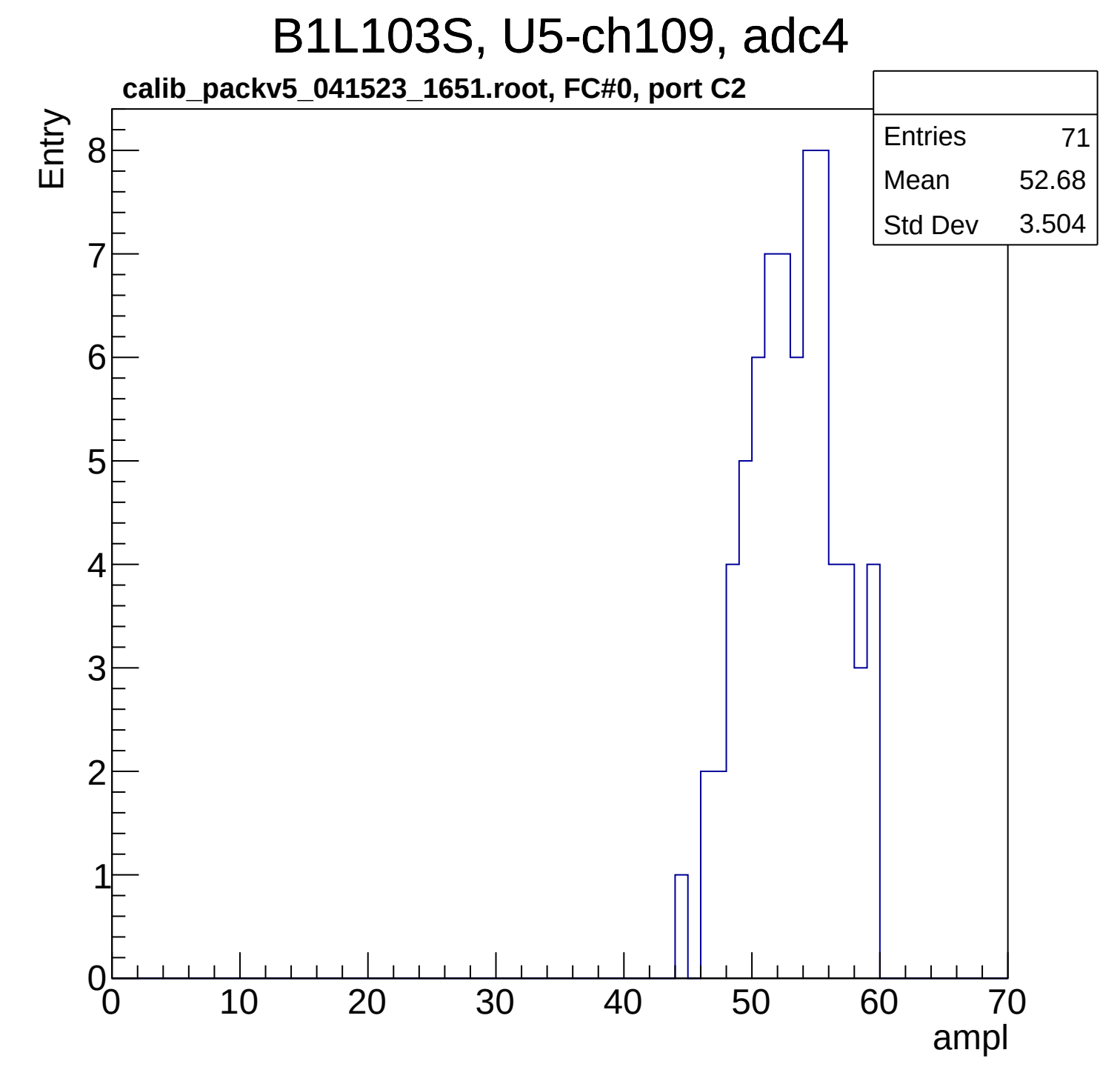
B1L103S, U5-ch109, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 52.68
Std Dev 3.504
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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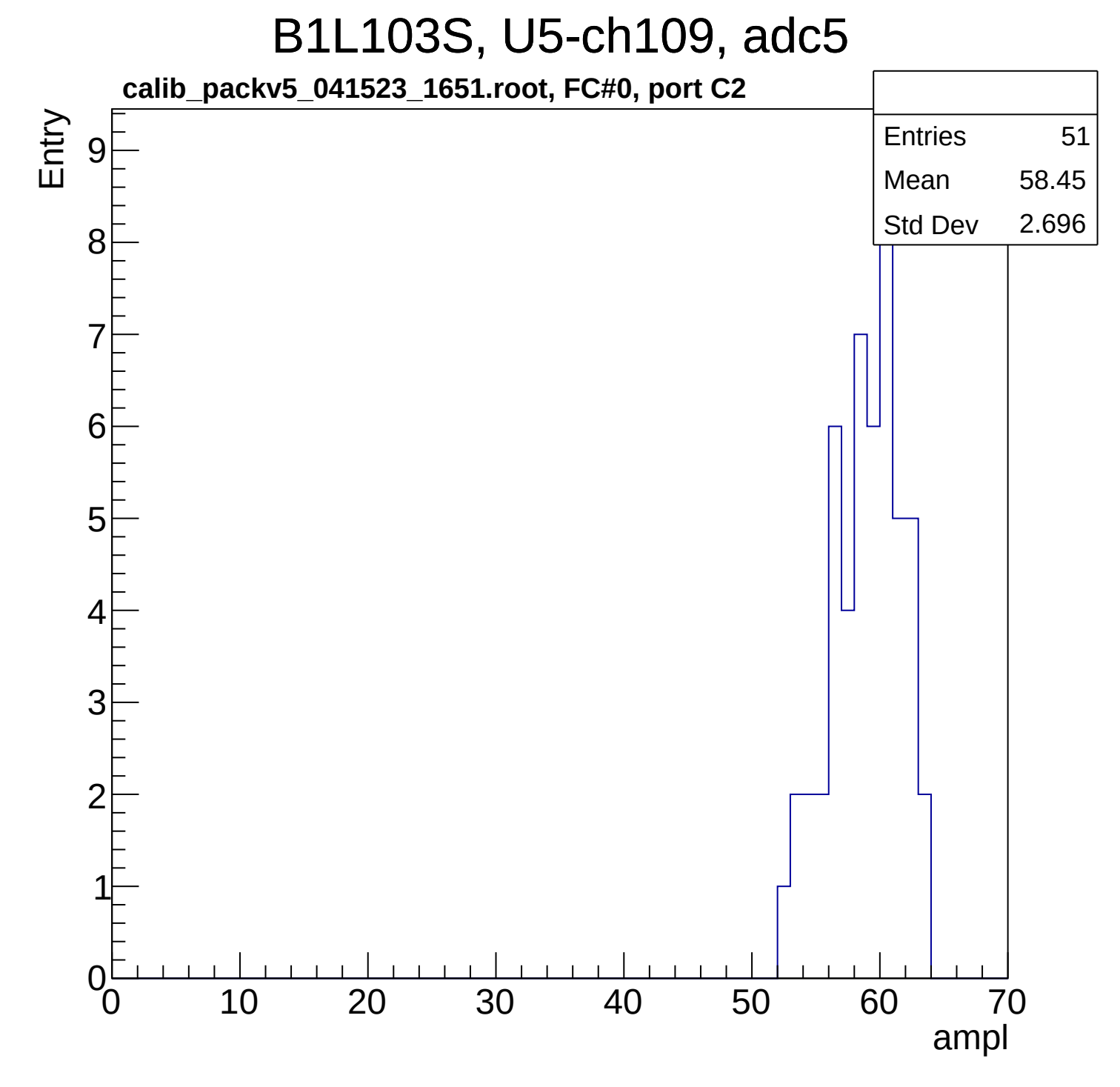
B1L103S, U5-ch109, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.45
Std Dev 2.696
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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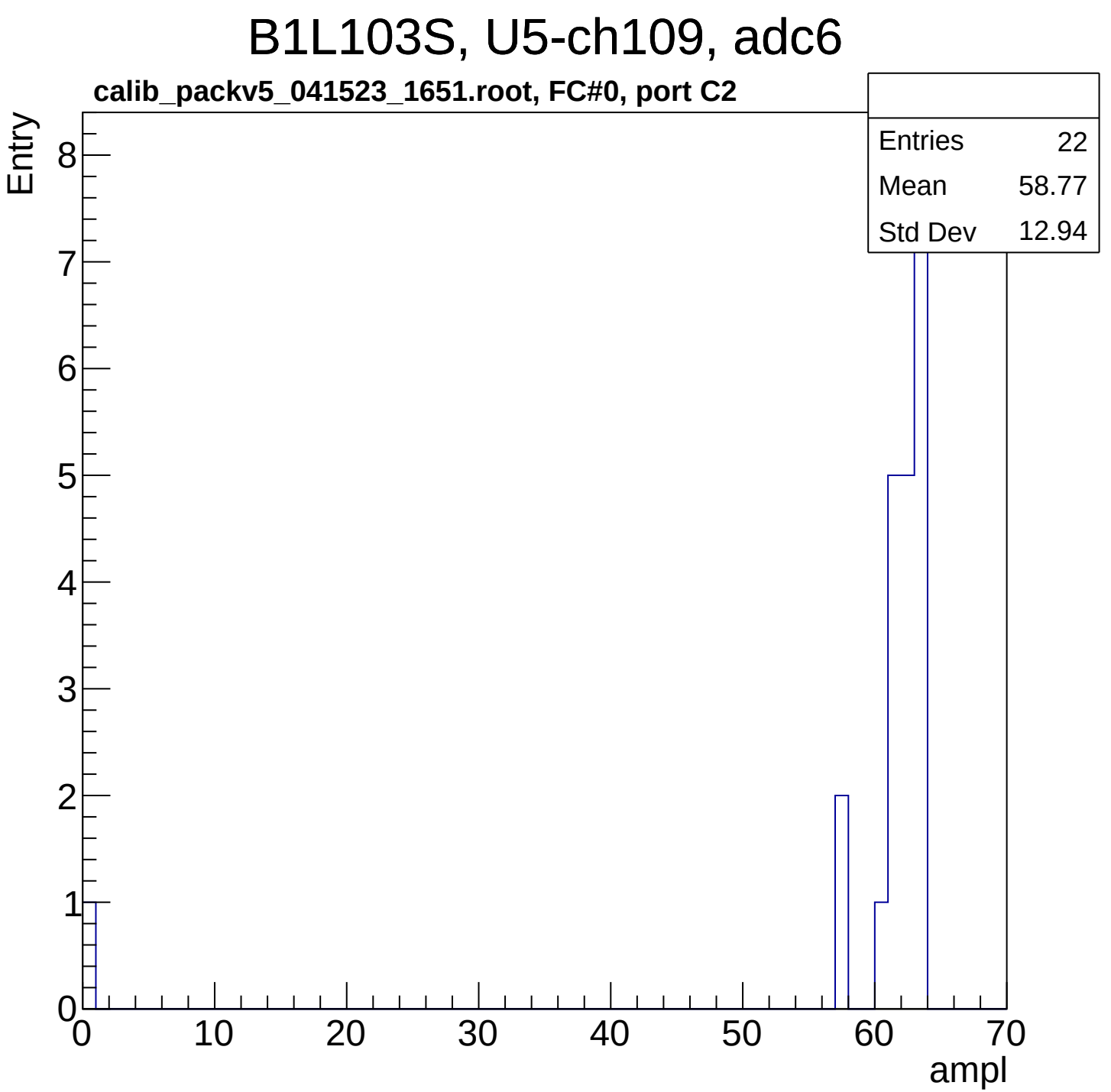
B1L103S, U5-ch109, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.77
Std Dev 12.94
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
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60
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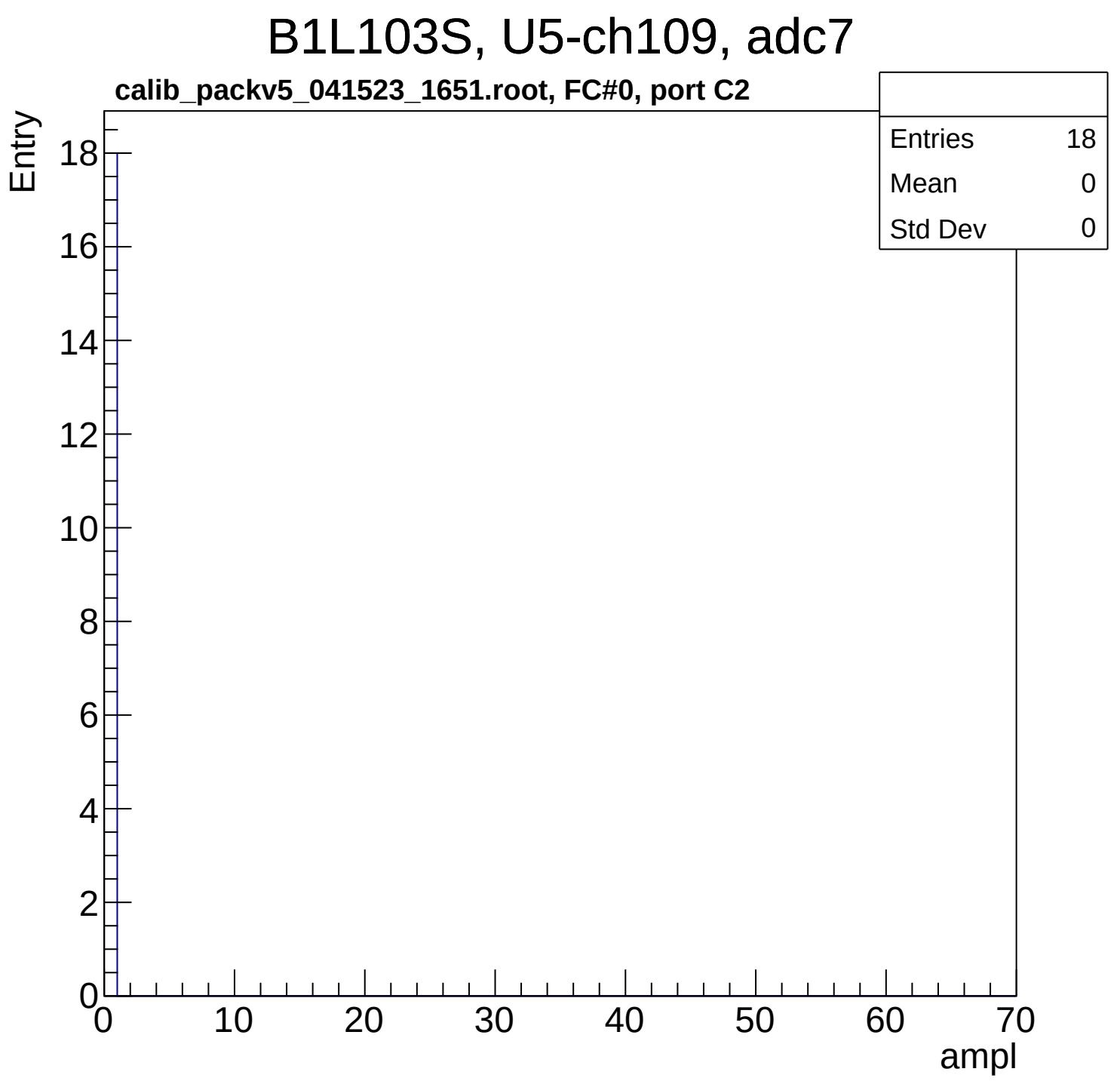
B1L103S, U5-ch109, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
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10
20
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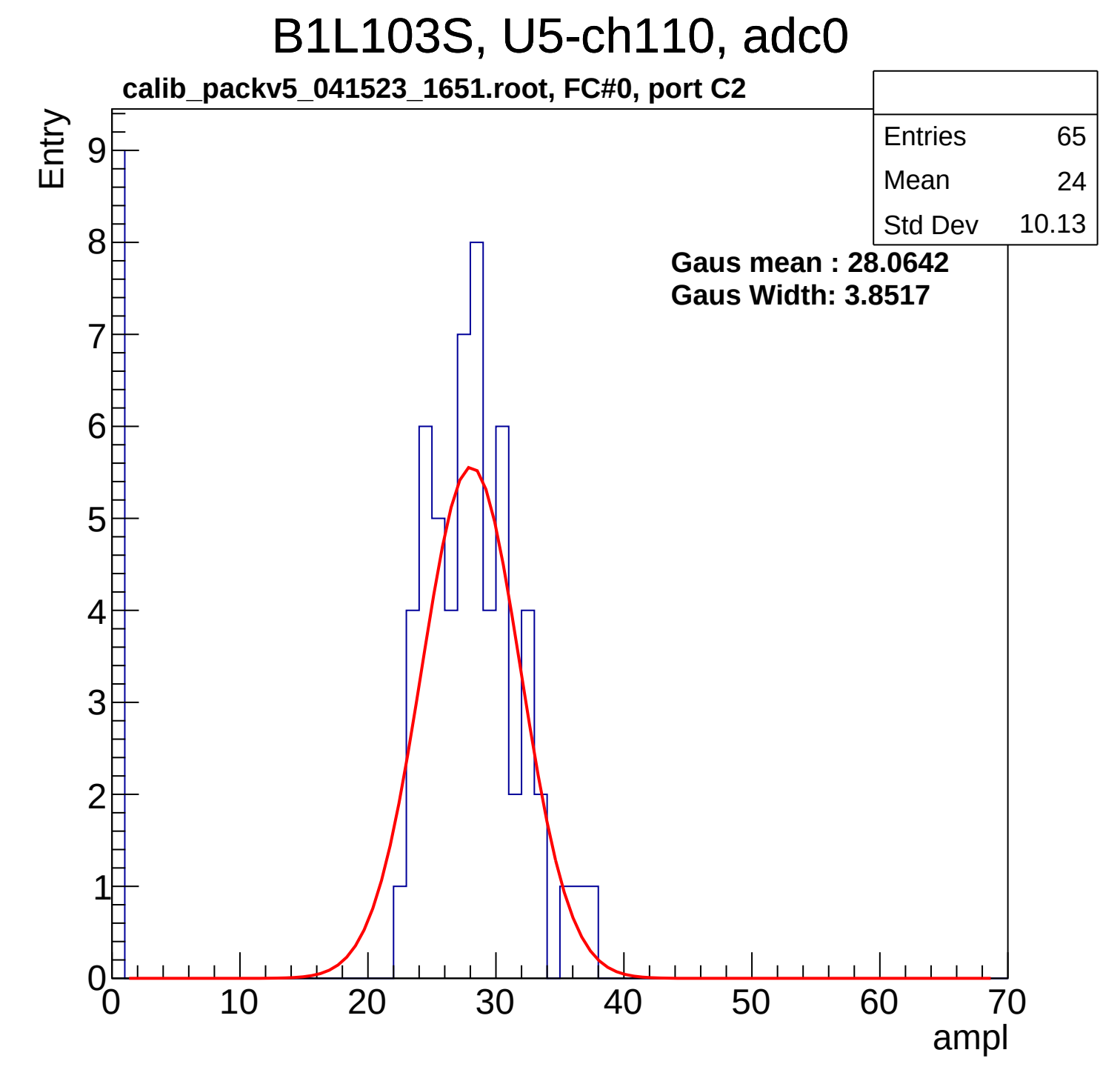
40
50
60
70
ampl


B1L103S, U5-ch110, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 24
Std Dev 10.13
Gaus mean : 28.0642
Gaus Width: 3.8517
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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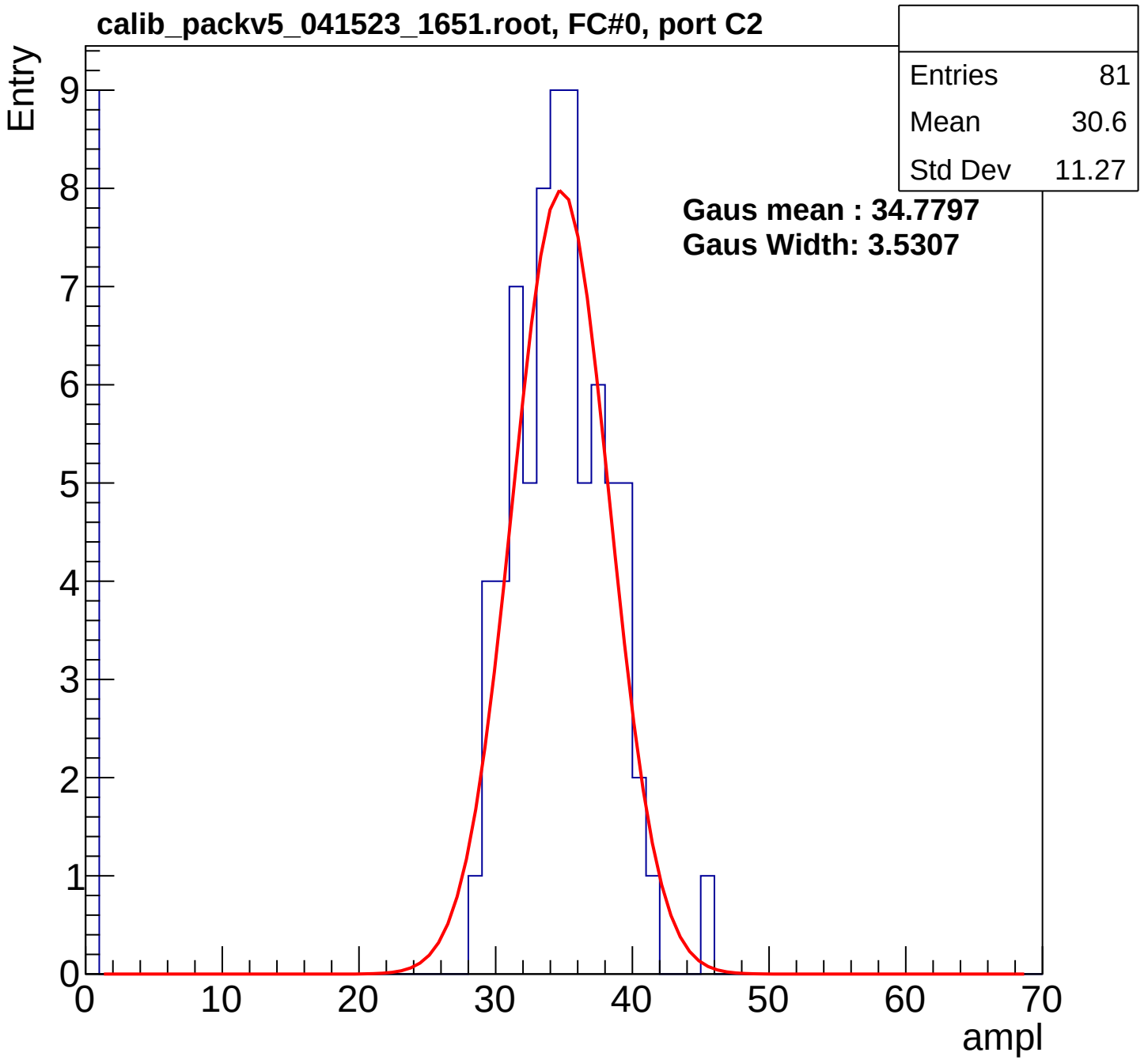
B1L103S, U5-ch110, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 30.6
Std Dev 11.27
Gaus mean : 34.7797
Gaus Width: 3.5307
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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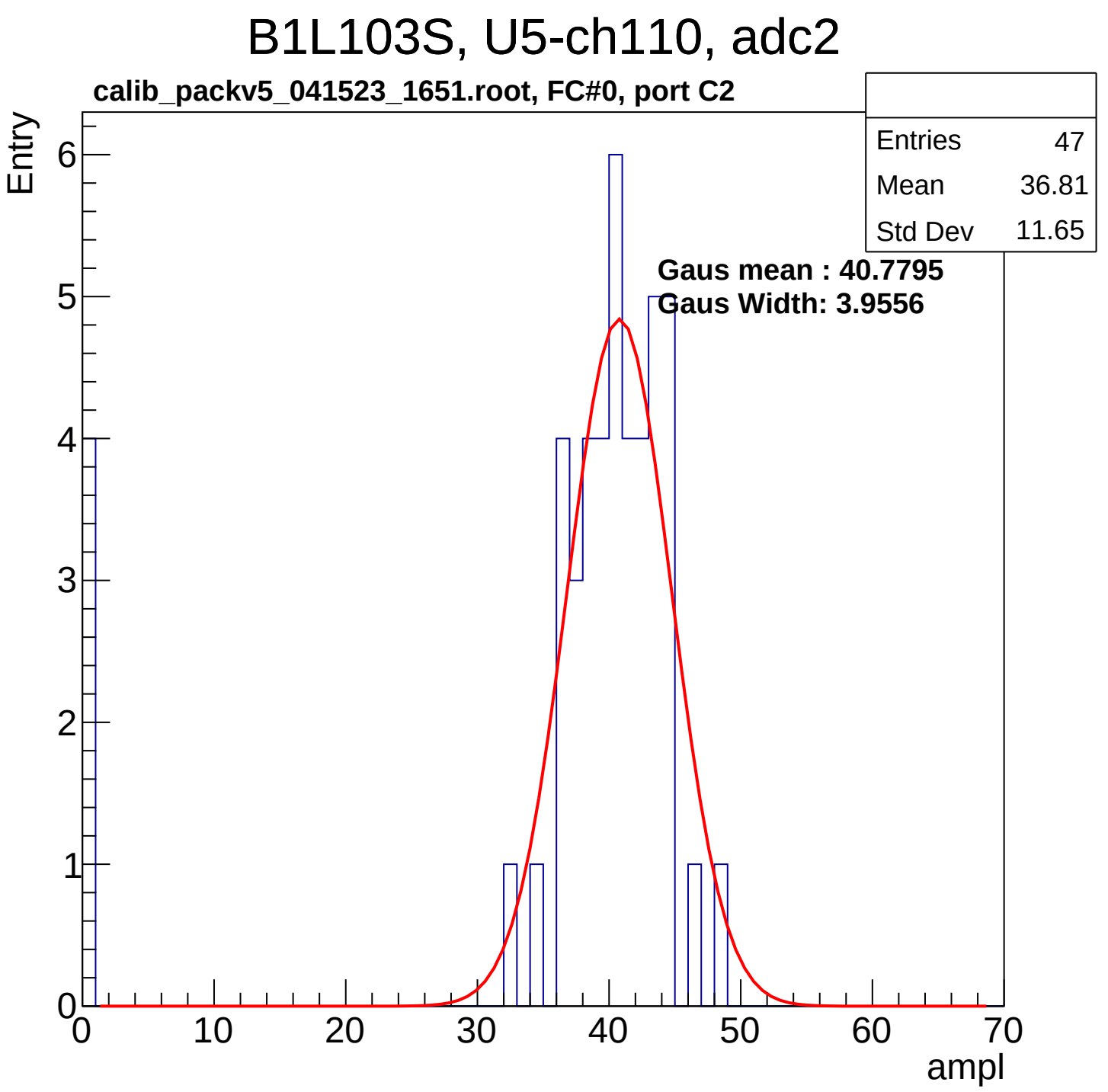
B1L103S, U5-ch110, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 36.81
Std Dev 11.65
Gaus mean : 40.7795
Gaus Width: 3.9556
Entry
ampl
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1
2
3
4
5
6
0
10
20
30
40
50
60
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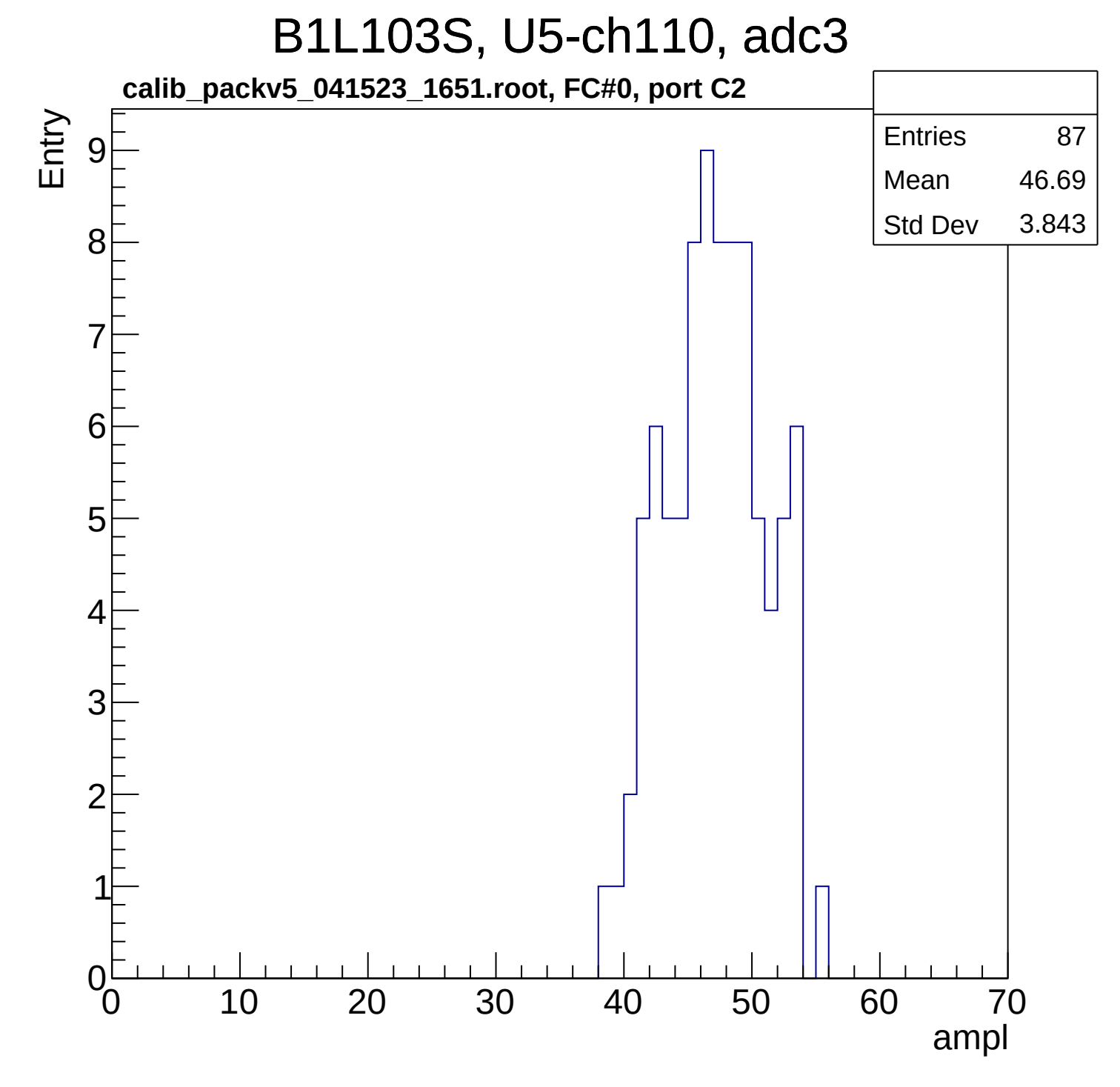
B1L103S, U5-ch110, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 46.69
Std Dev 3.843
Entry
ampl
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2
3
4
5
6
7
8
9
0
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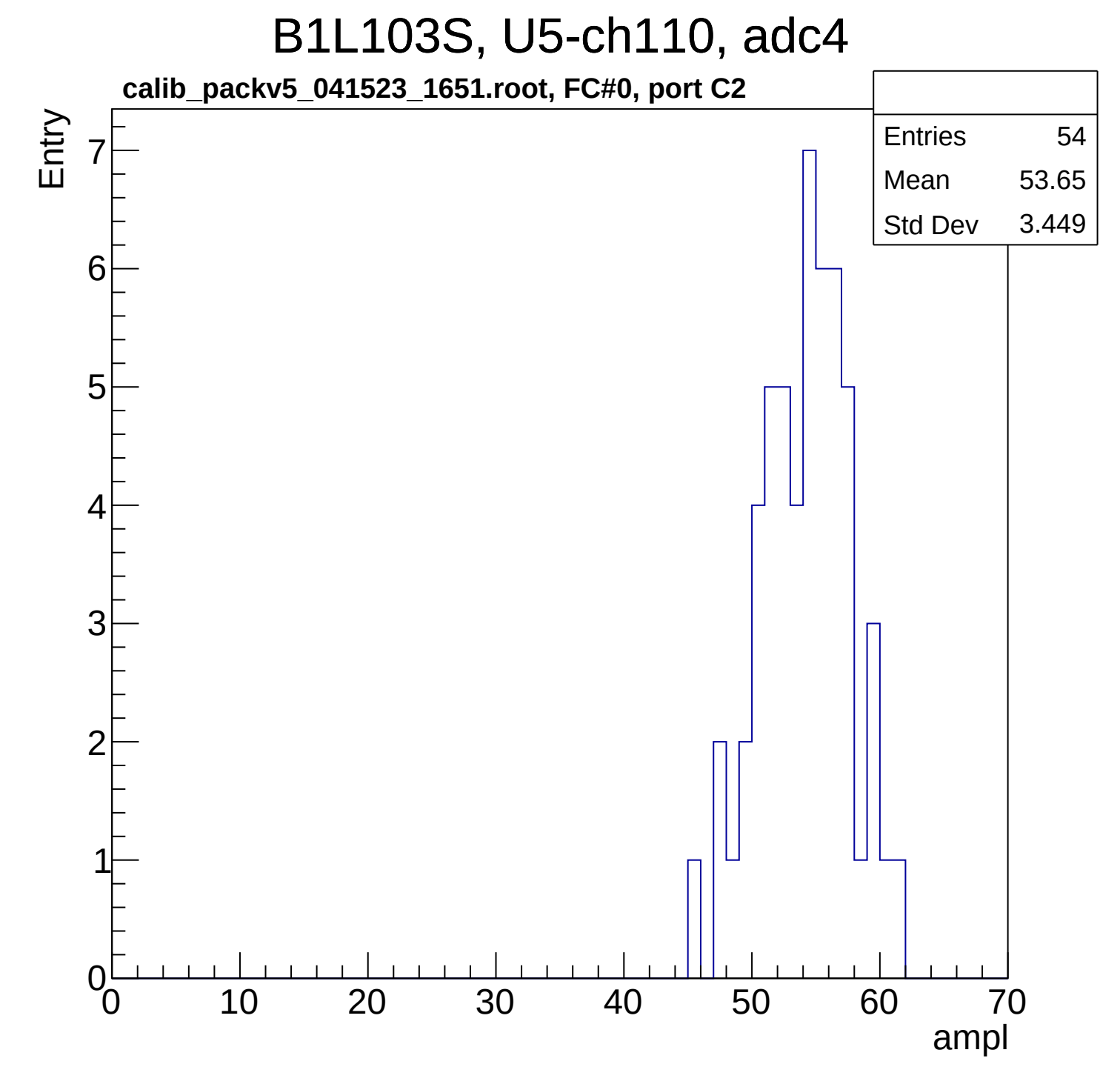
B1L103S, U5-ch110, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 53.65
Std Dev 3.449
Entry
ampl
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4
5
6
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0
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20
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40
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60
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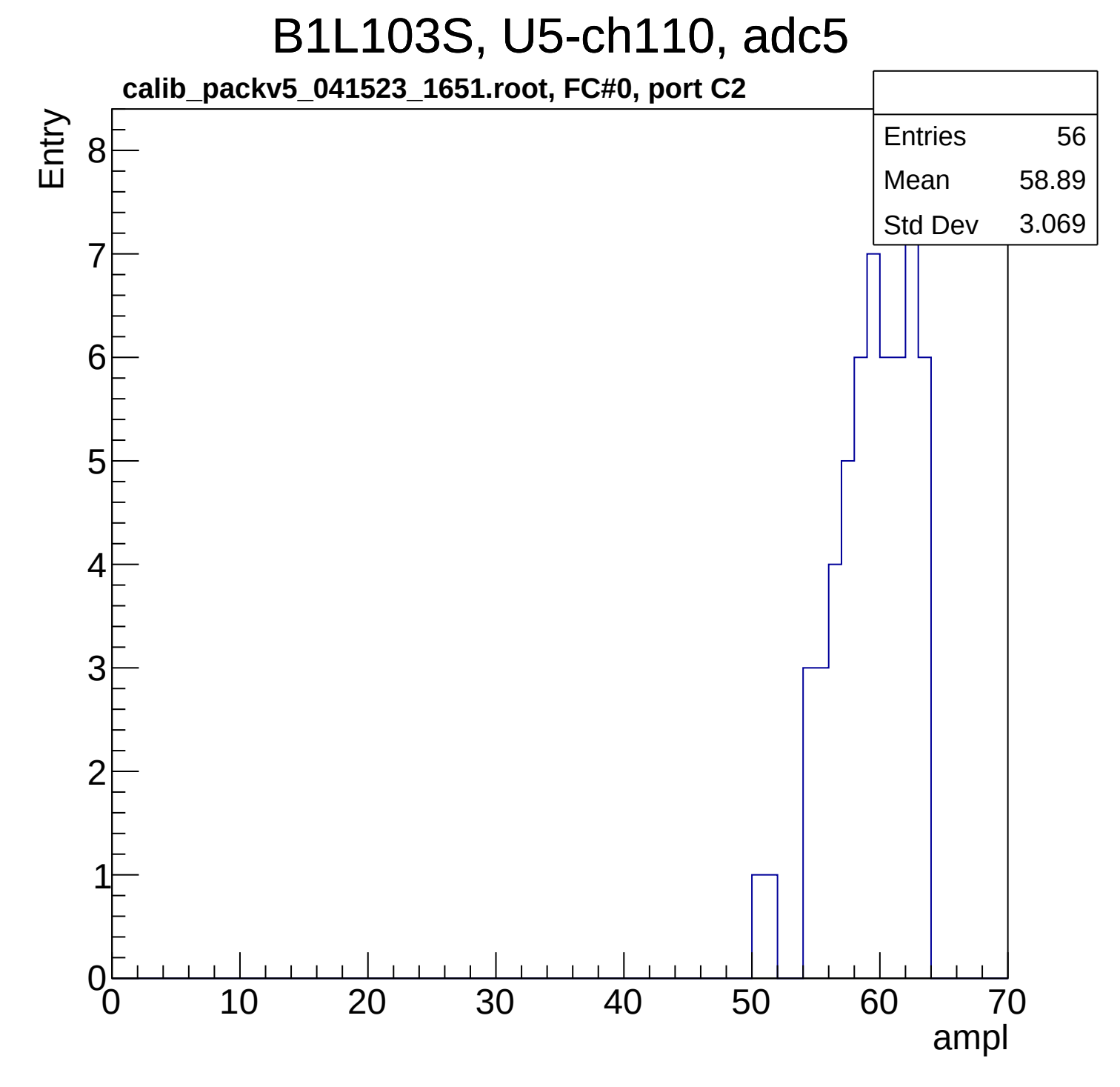
B1L103S, U5-ch110, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.89
Std Dev 3.069
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
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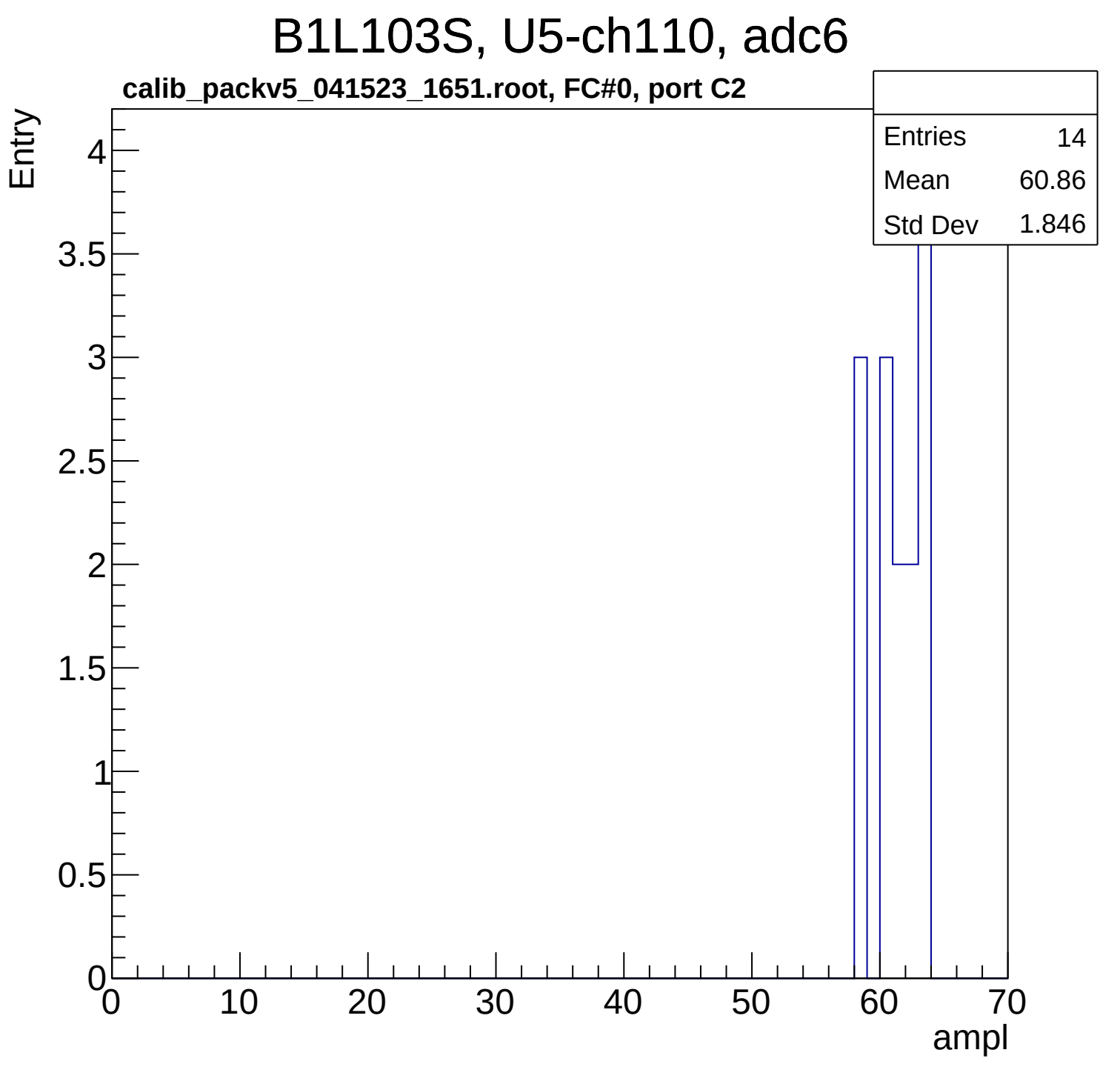
B1L103S, U5-ch110, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 60.86
Std Dev 1.846
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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20
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60
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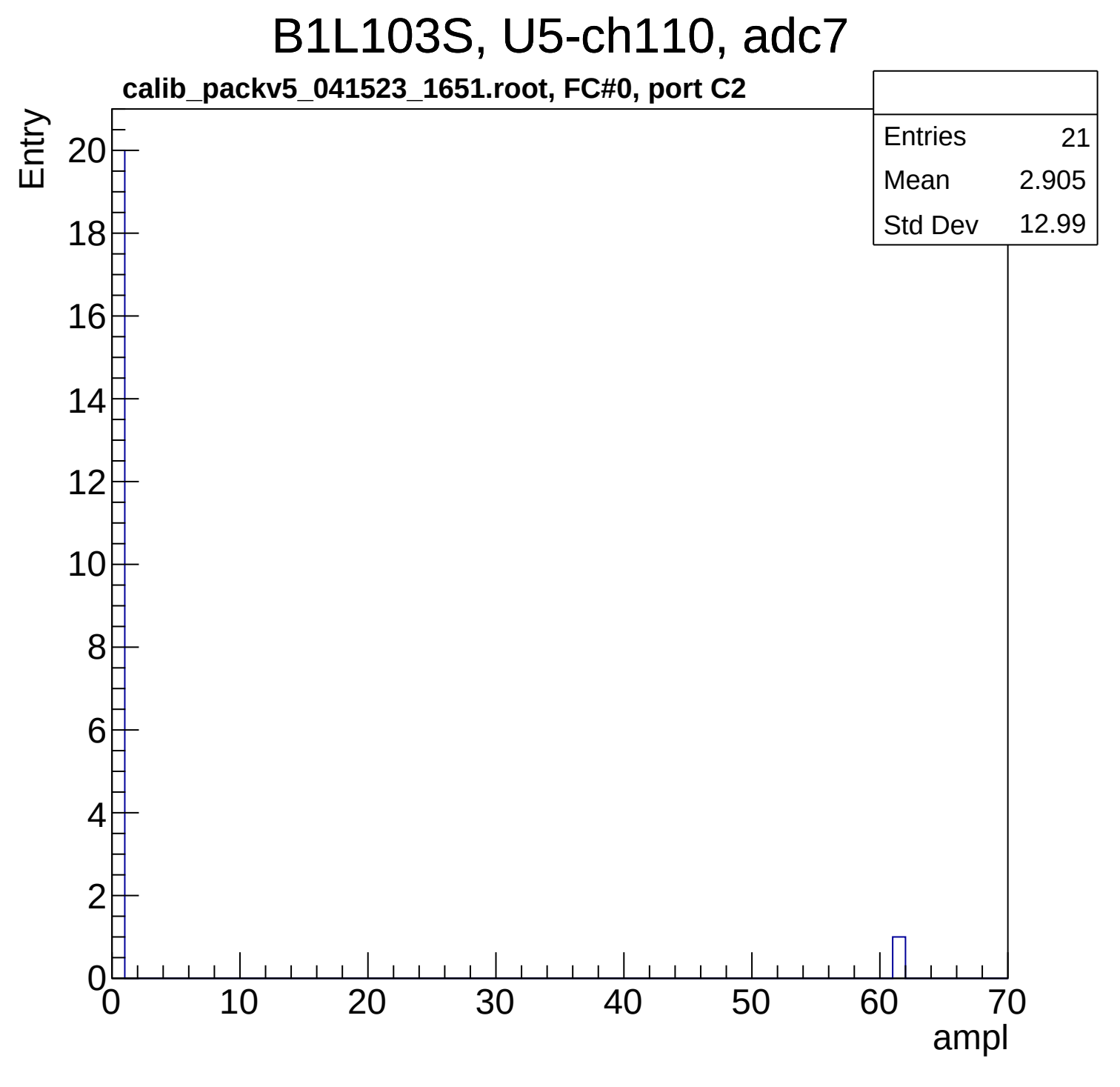
B1L103S, U5-ch110, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 2.905
Std Dev 12.99
Entry
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16
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20
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10
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30
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50
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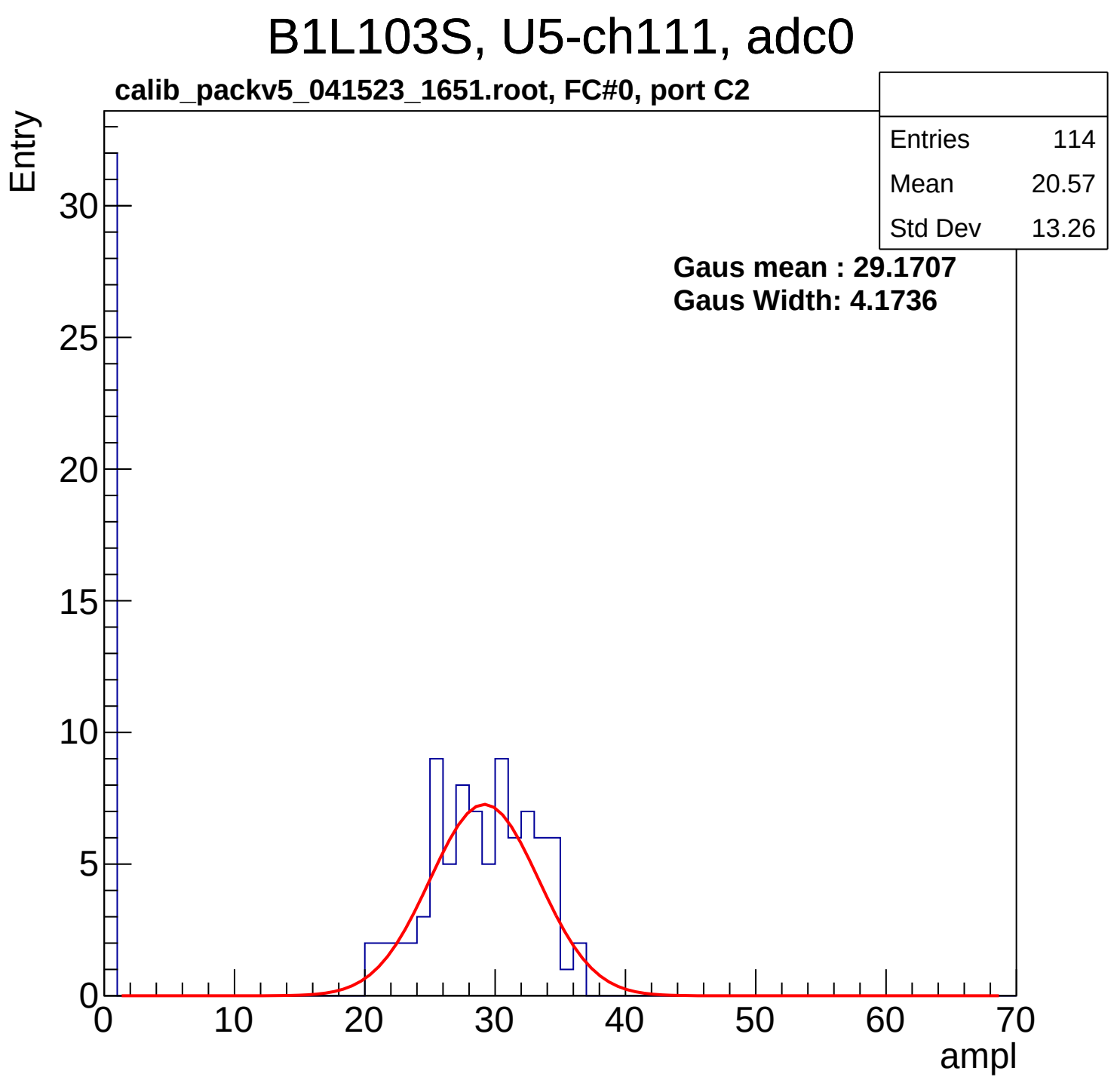
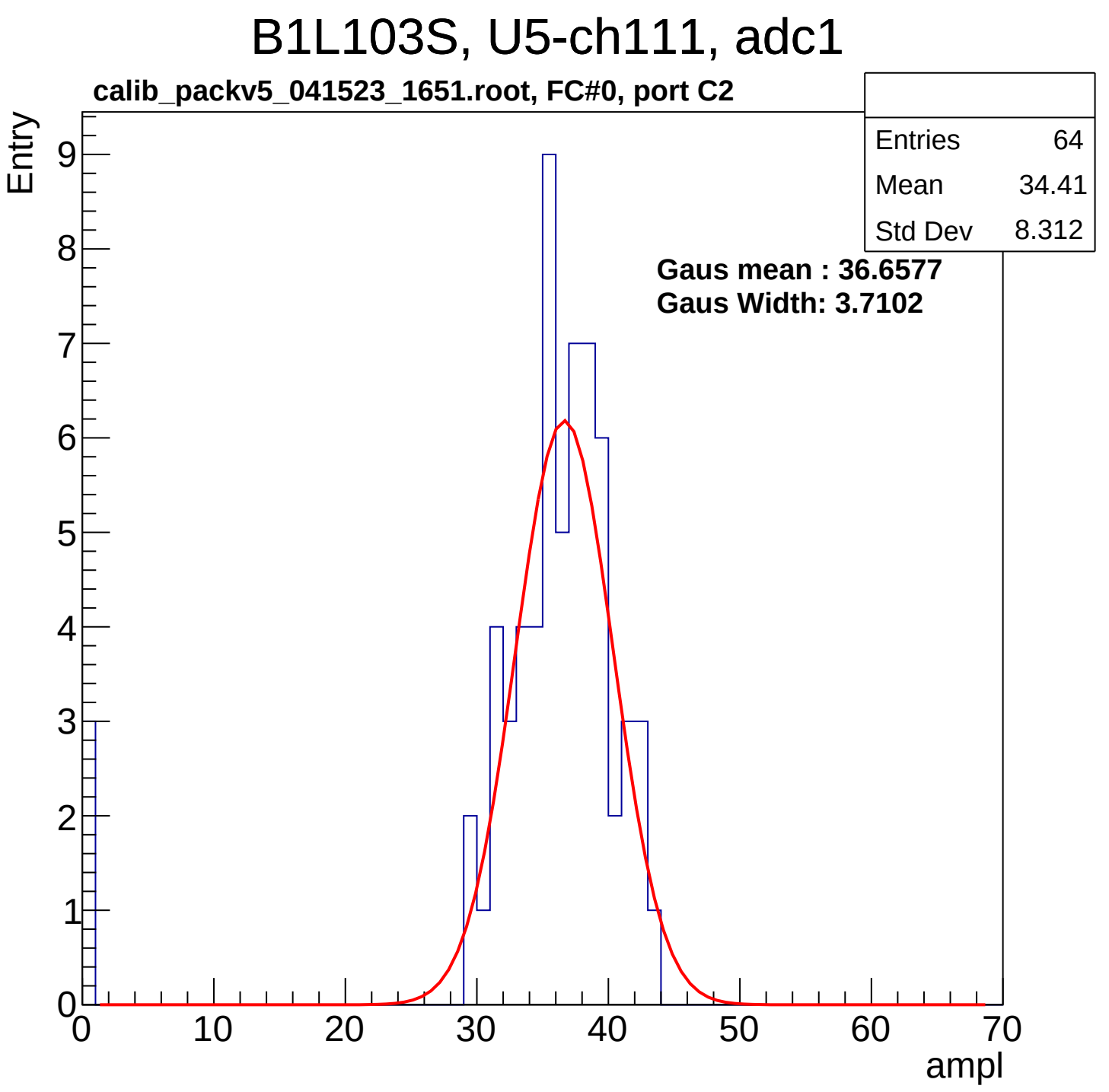
70
ampl


B1L103S, U5-ch111, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 114
Mean 20.57
Std Dev 13.26
Gaus mean : 29.1707
Gaus Width: 4.1736
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70


B1L103S, U5-ch111, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 34.41
Std Dev 8.312
Gaus mean : 36.6577
Gaus Width: 3.7102
Entry
ampl
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10
20
30
40
50
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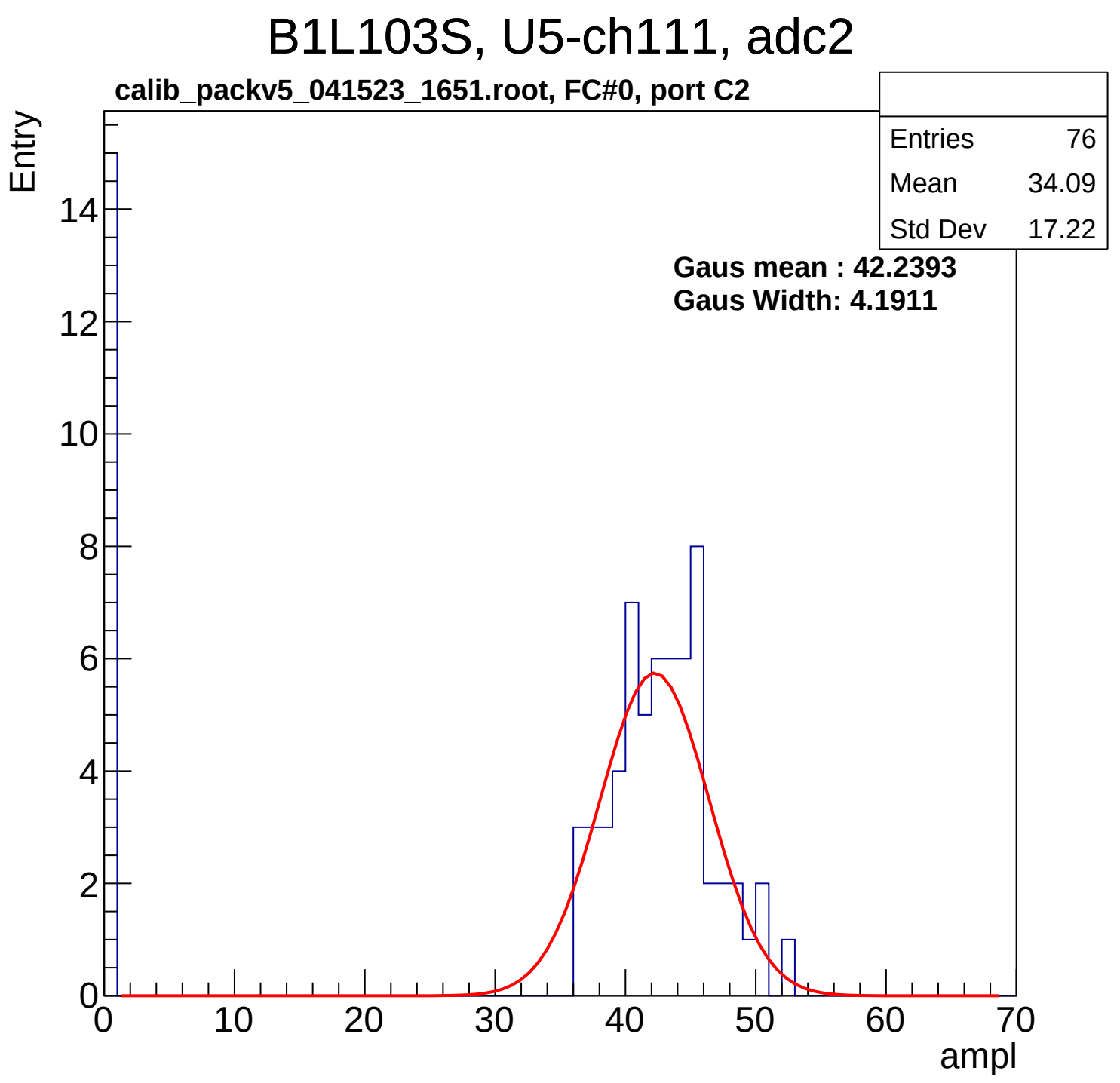
1
2
3
4
5
6
7
8
9


B1L103S, U5-ch111, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 34.09
Std Dev 17.22
Gaus mean : 42.2393
Gaus Width: 4.1911
Entry
ampl
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4
6
8
10
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14
0
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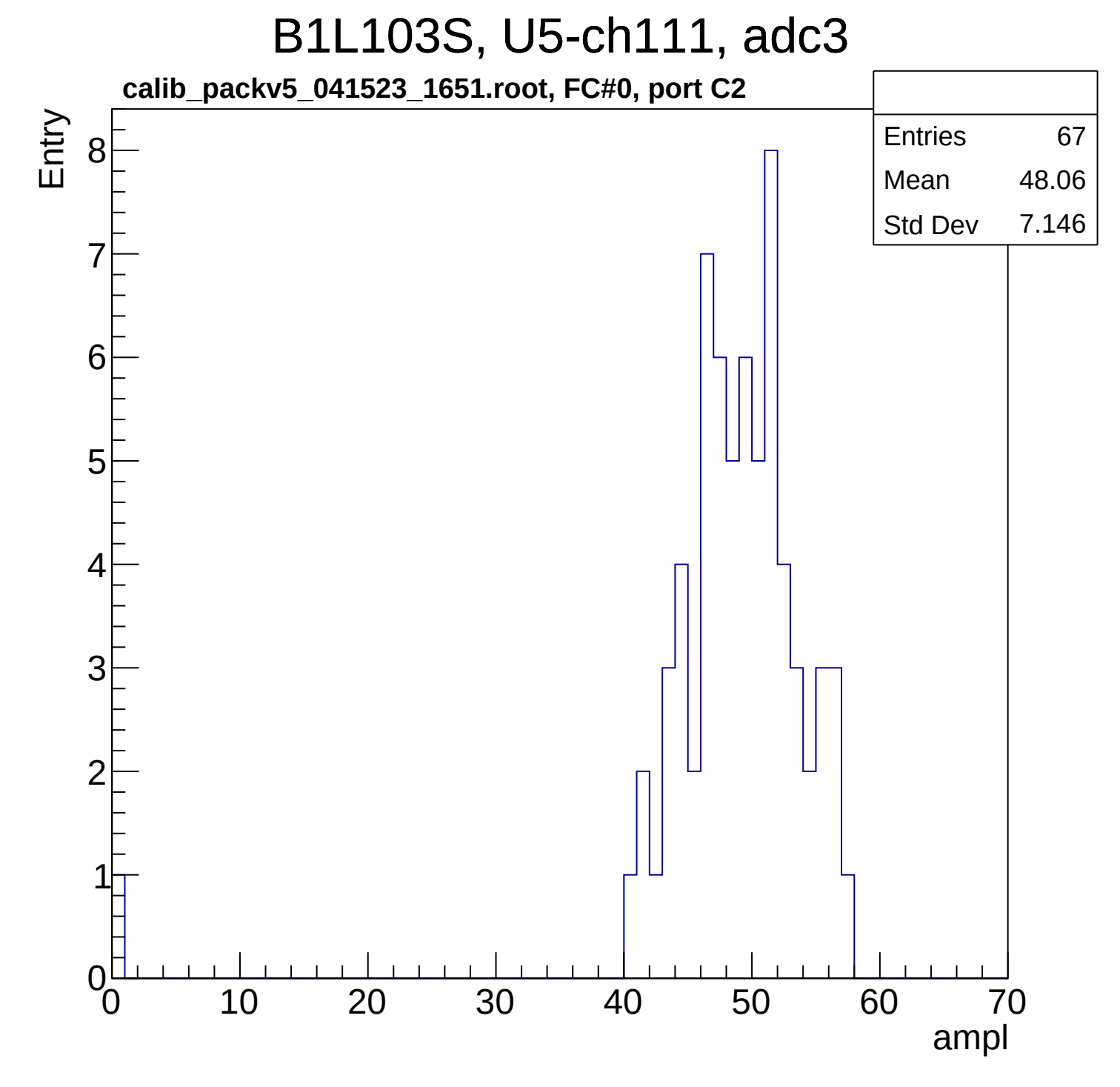
B1L103S, U5-ch111, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 48.06
Std Dev 7.146
Entry
ampl
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60
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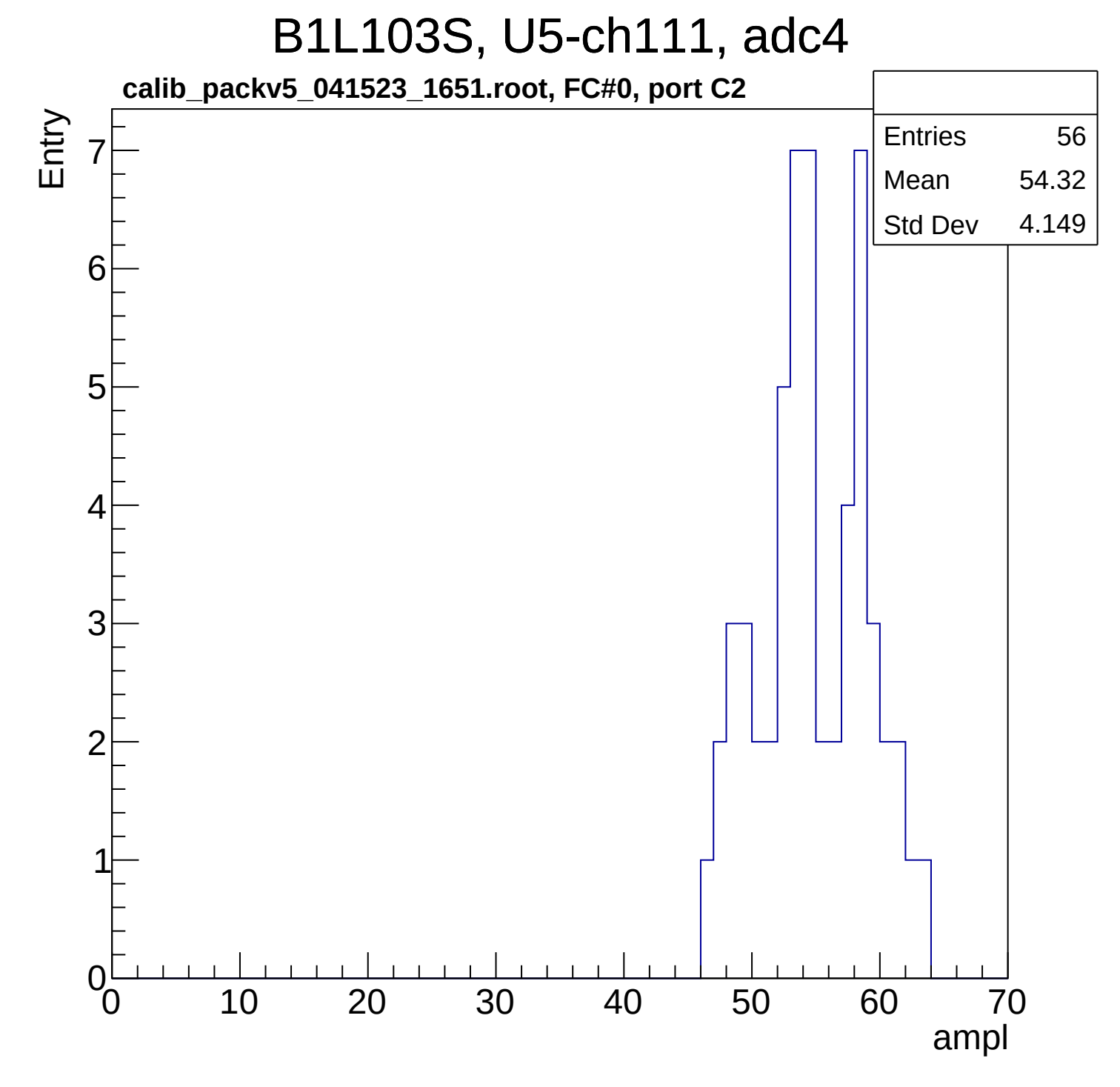
B1L103S, U5-ch111, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 54.32
Std Dev 4.149
Entry
ampl
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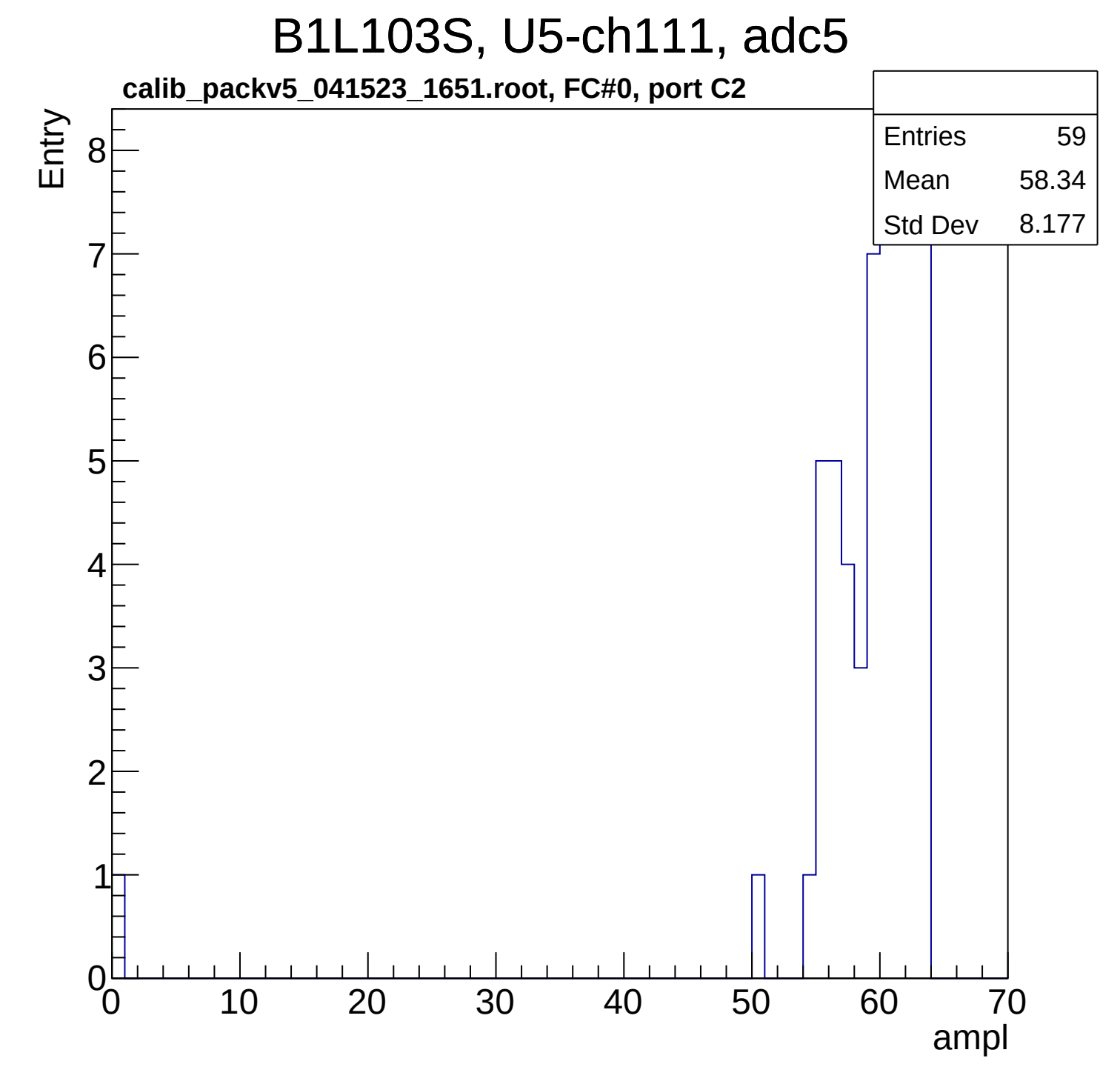
B1L103S, U5-ch111, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 58.34
Std Dev 8.177
Entry
ampl
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2
3
4
5
6
7
8
0
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60
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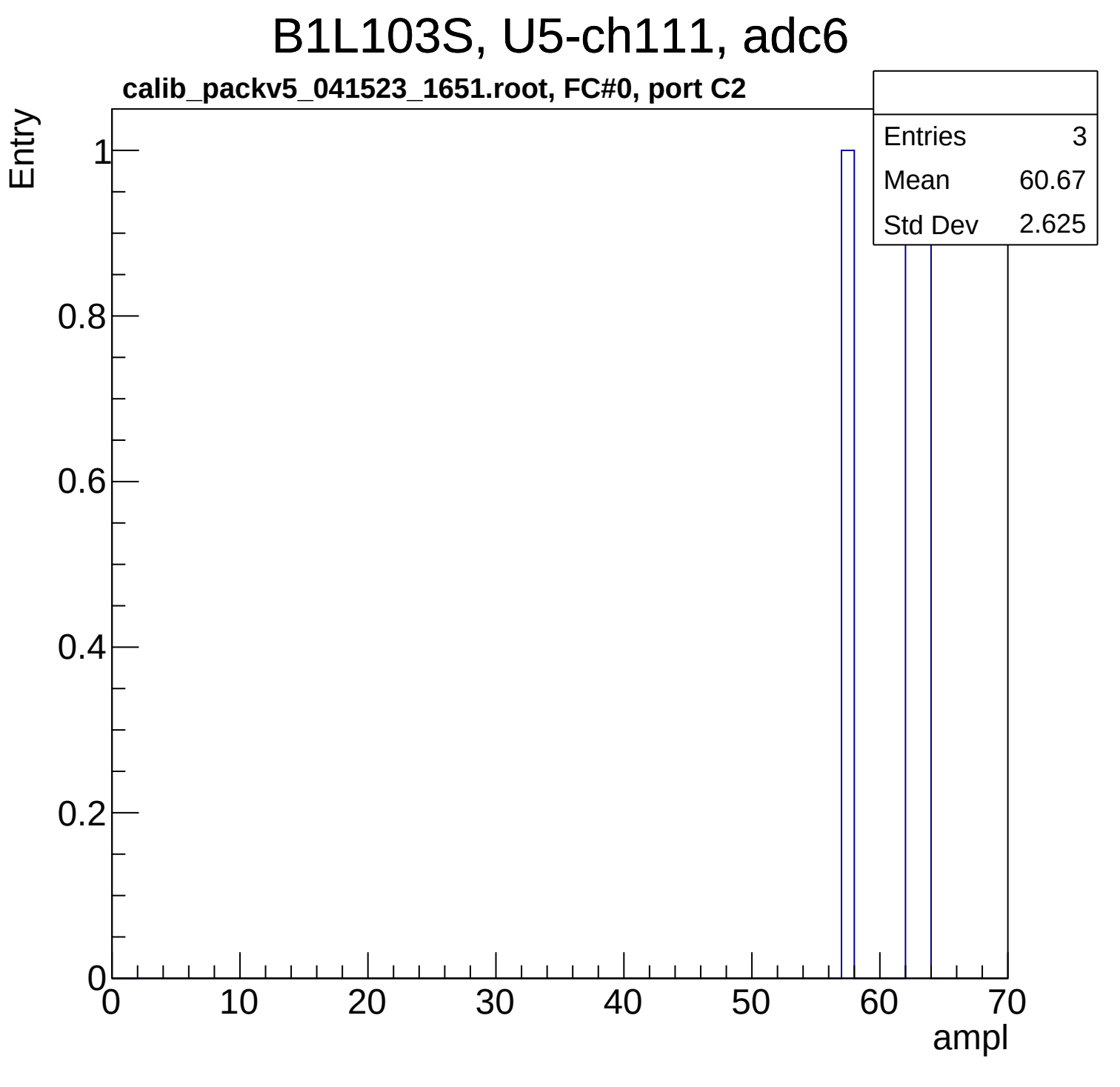
B1L103S, U5-ch111, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 60.67
Std Dev 2.625
Entry
ampl
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0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
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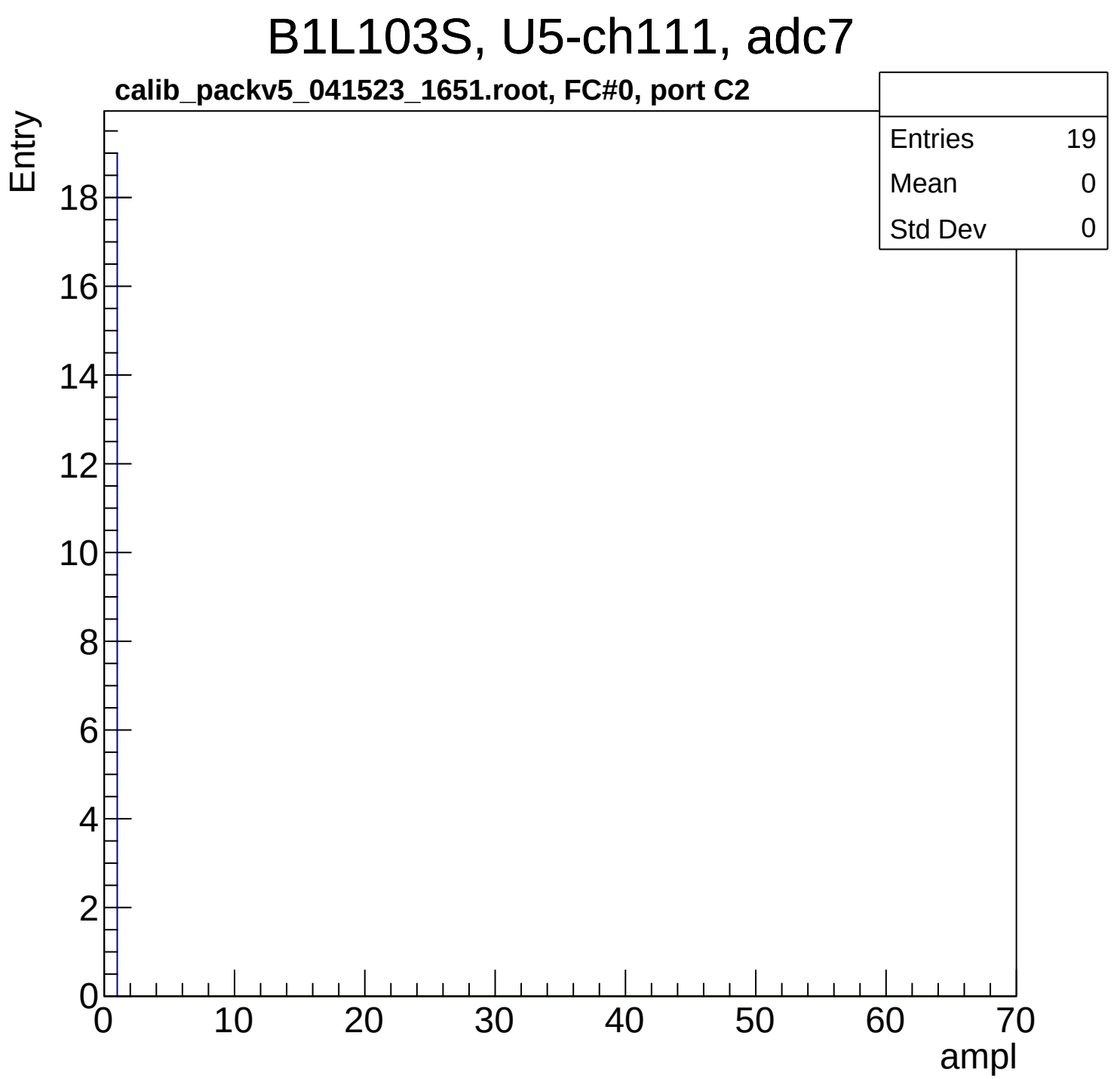
B1L103S, U5-ch111, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
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10
20
30
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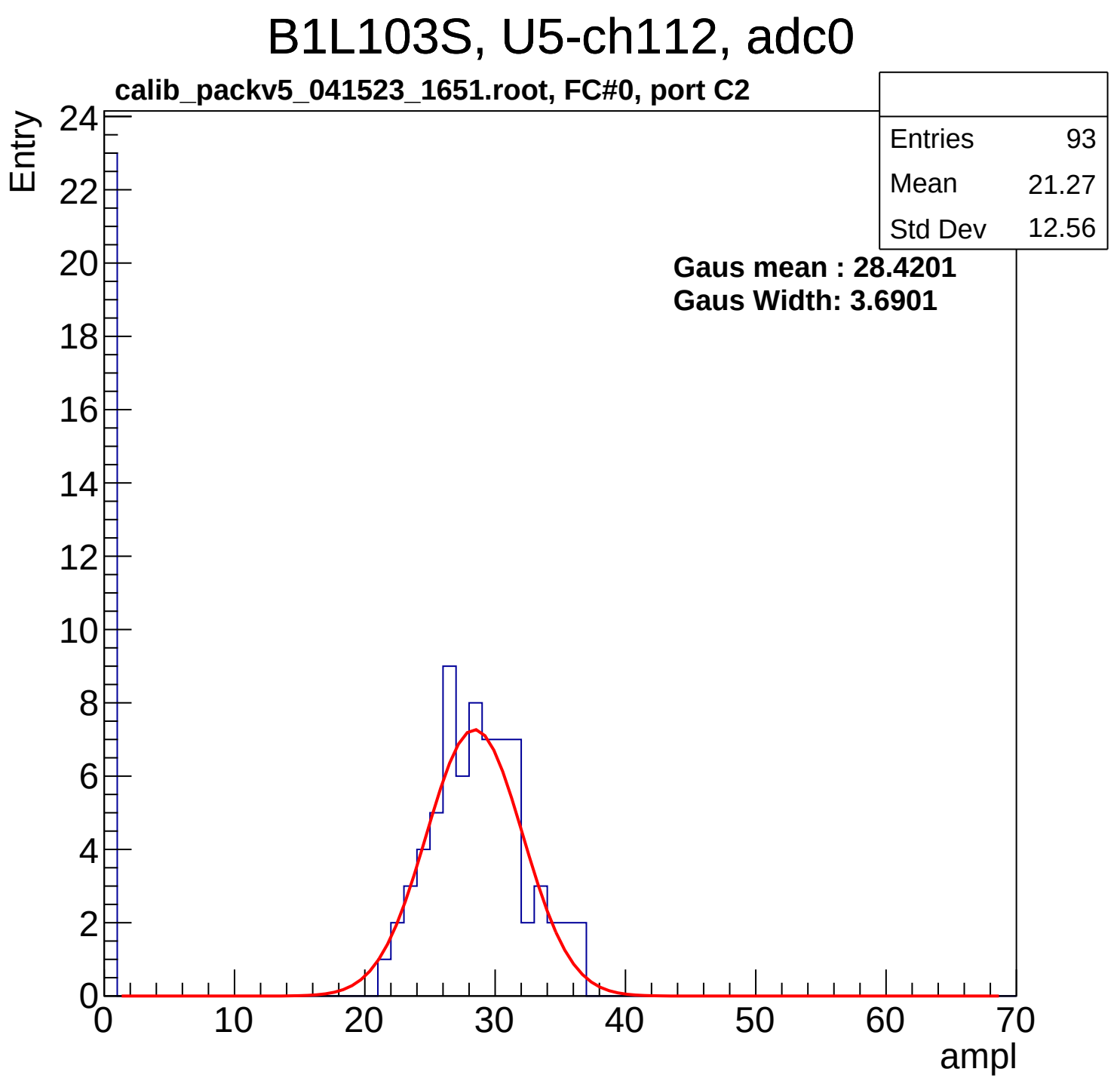
50
60
70
ampl


B1L103S, U5-ch112, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 21.27
Std Dev 12.56
Gaus mean : 28.4201
Gaus Width: 3.6901
Entry
ampl
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2
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10
12
14
16
18
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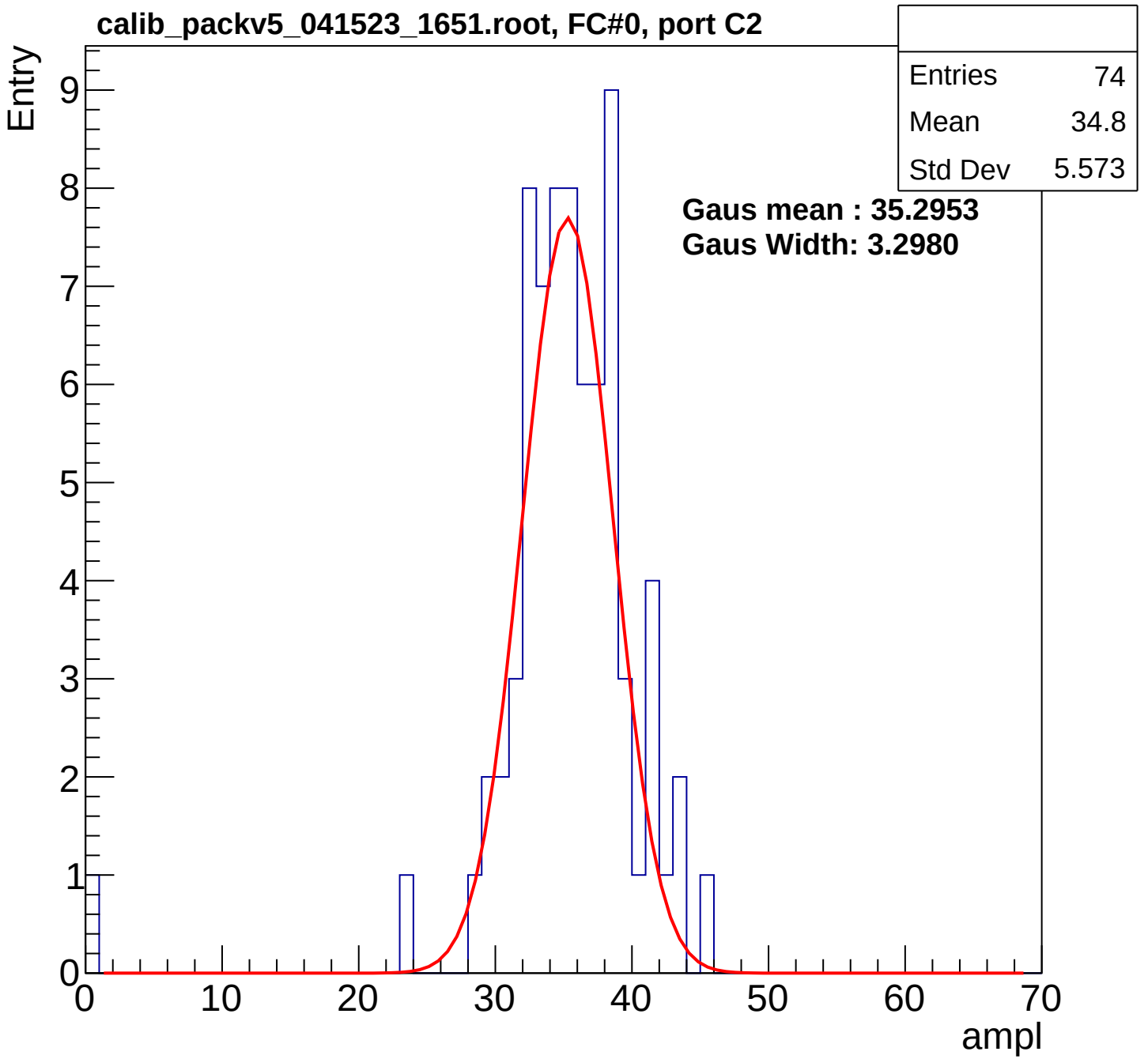
B1L103S, U5-ch112, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 34.8
Std Dev 5.573
Gaus mean : 35.2953
Gaus Width: 3.2980
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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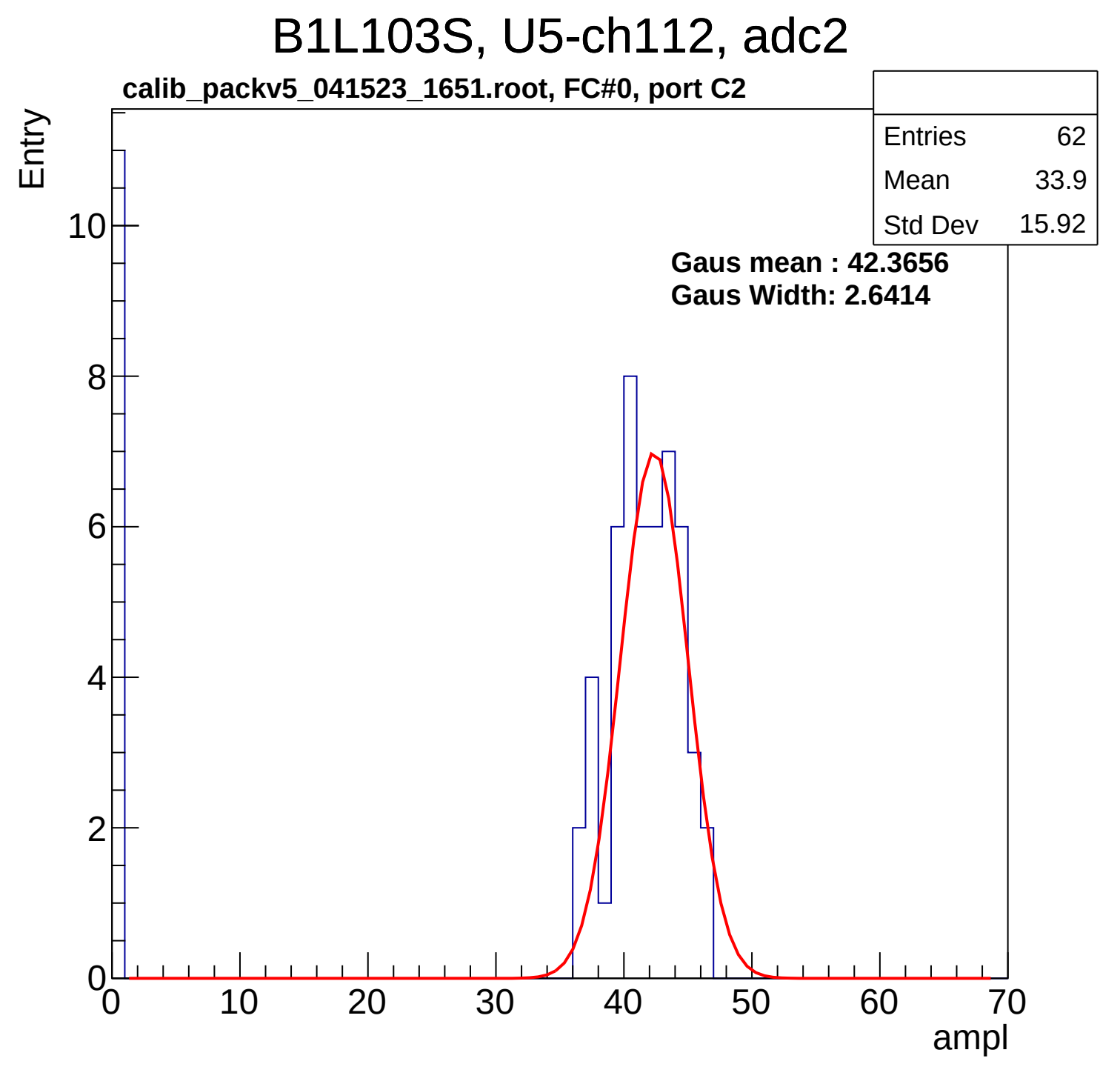
B1L103S, U5-ch112, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 33.9
Std Dev 15.92
Gaus mean : 42.3656
Gaus Width: 2.6414
Entry
ampl
0
2
4
6
8
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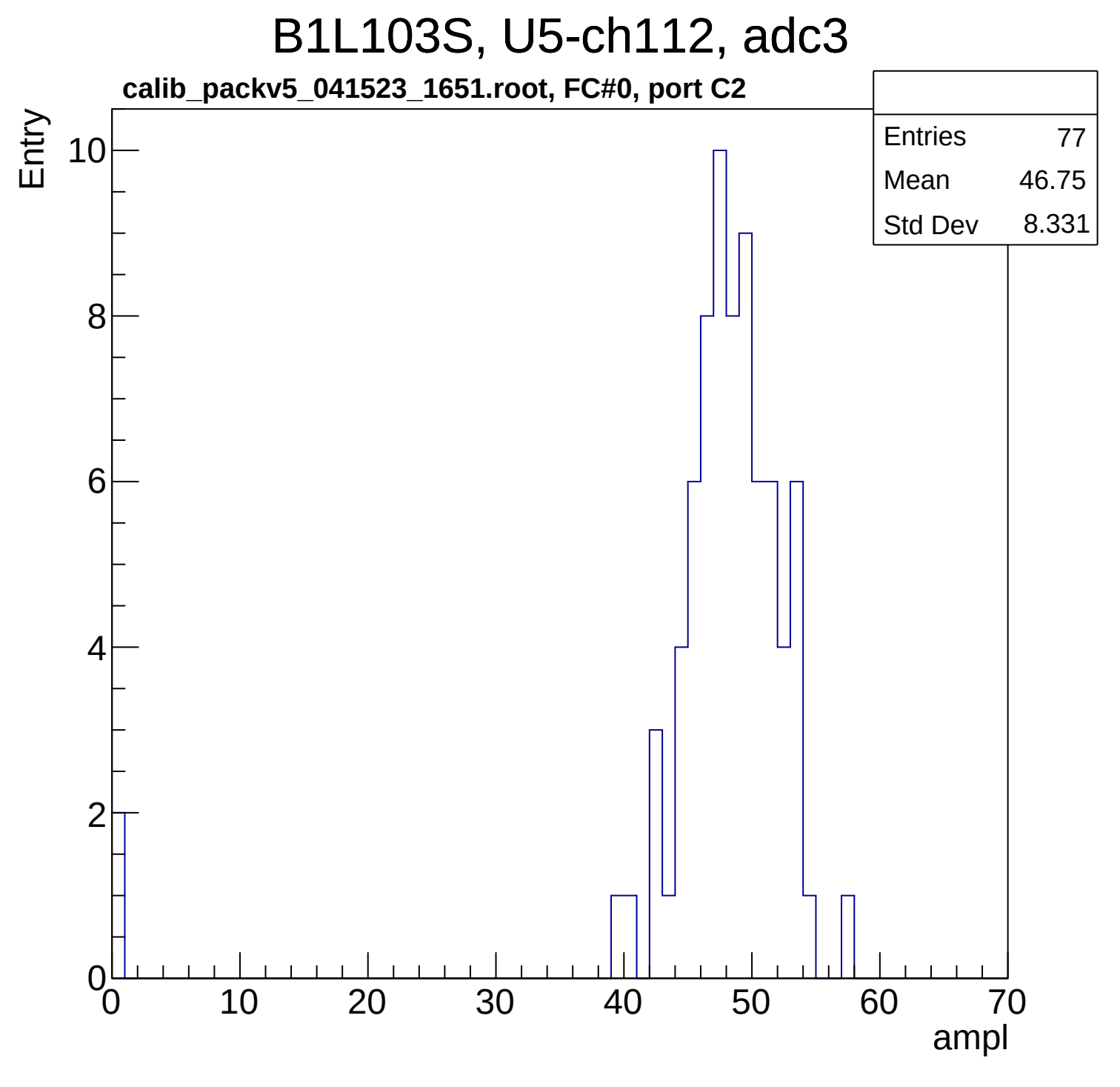
B1L103S, U5-ch112, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 46.75
Std Dev 8.331
Entry
ampl
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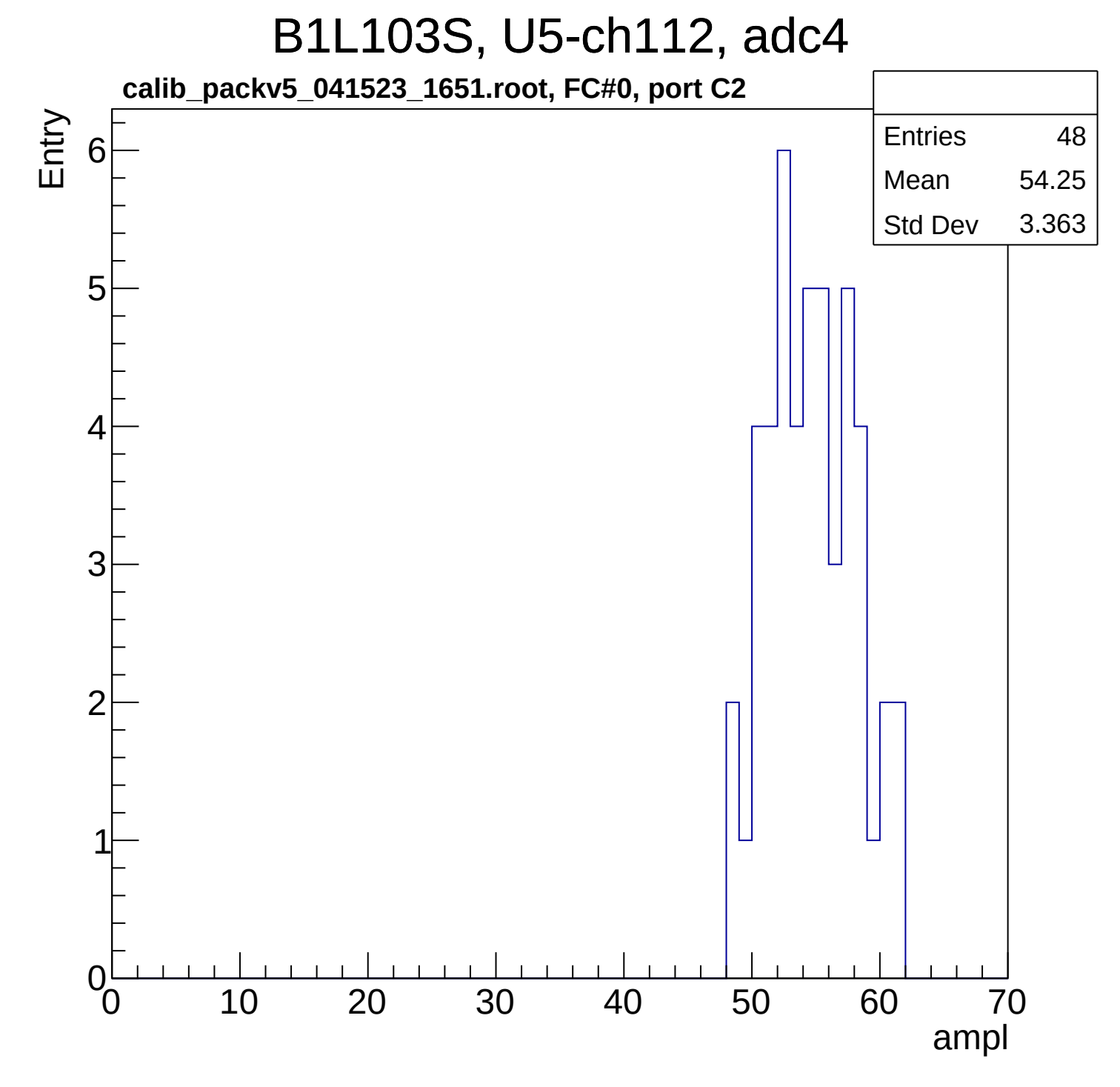
B1L103S, U5-ch112, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 54.25
Std Dev 3.363
Entry
ampl
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1
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3
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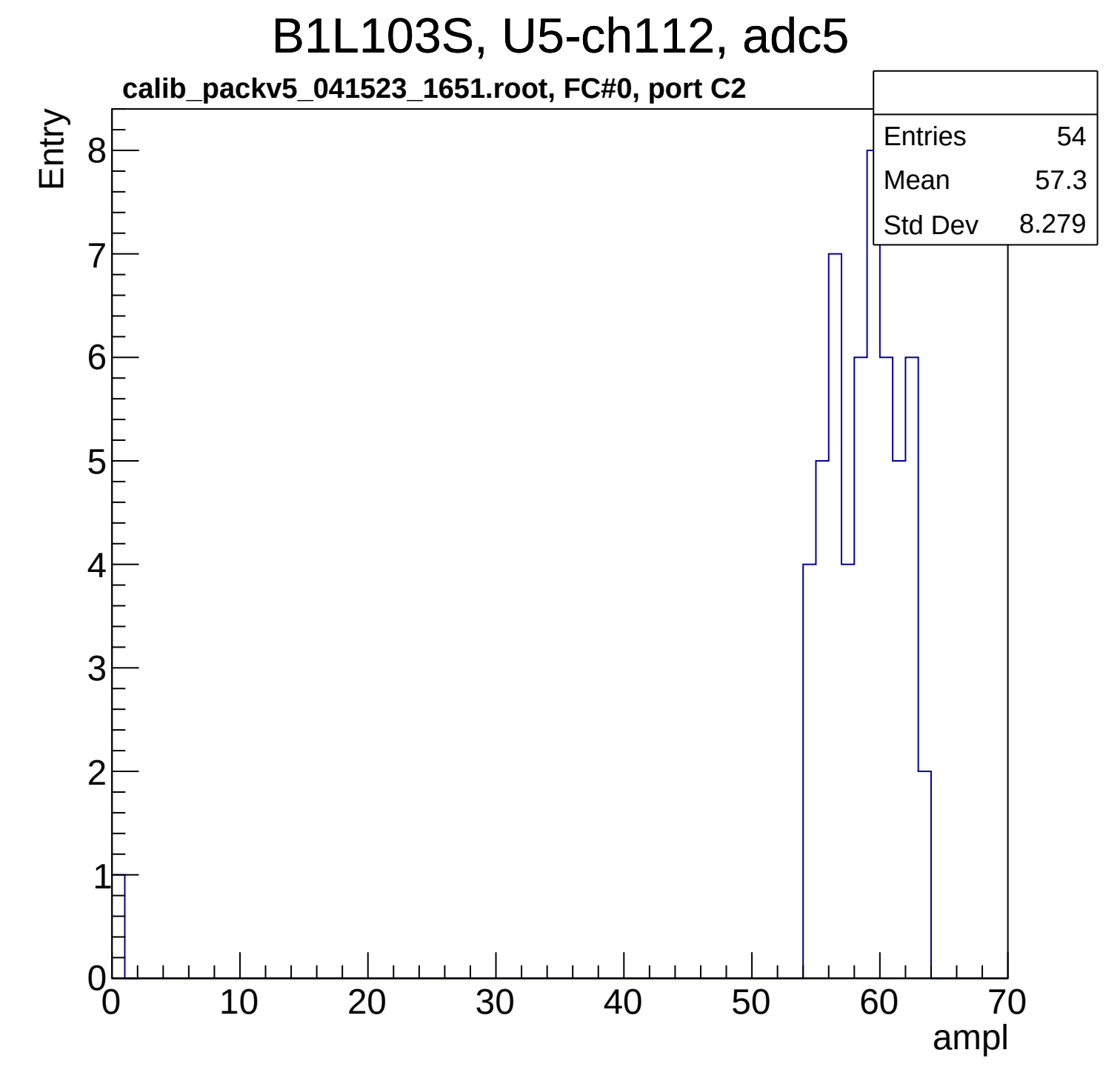
B1L103S, U5-ch112, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.3
Std Dev 8.279
Entry
ampl
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3
4
5
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0
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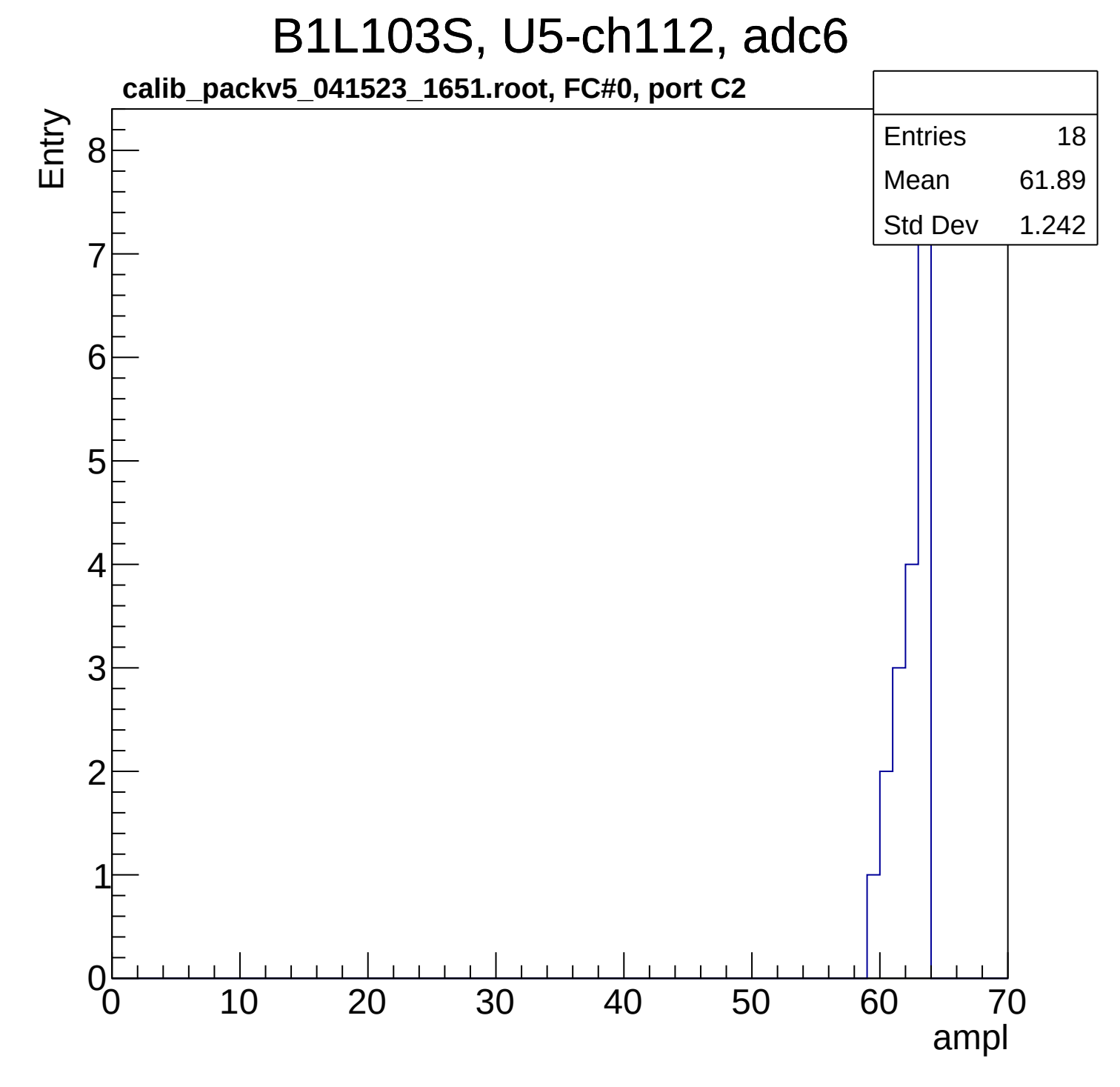
B1L103S, U5-ch112, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 61.89
Std Dev 1.242
Entry
ampl
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1
2
3
4
5
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7
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0
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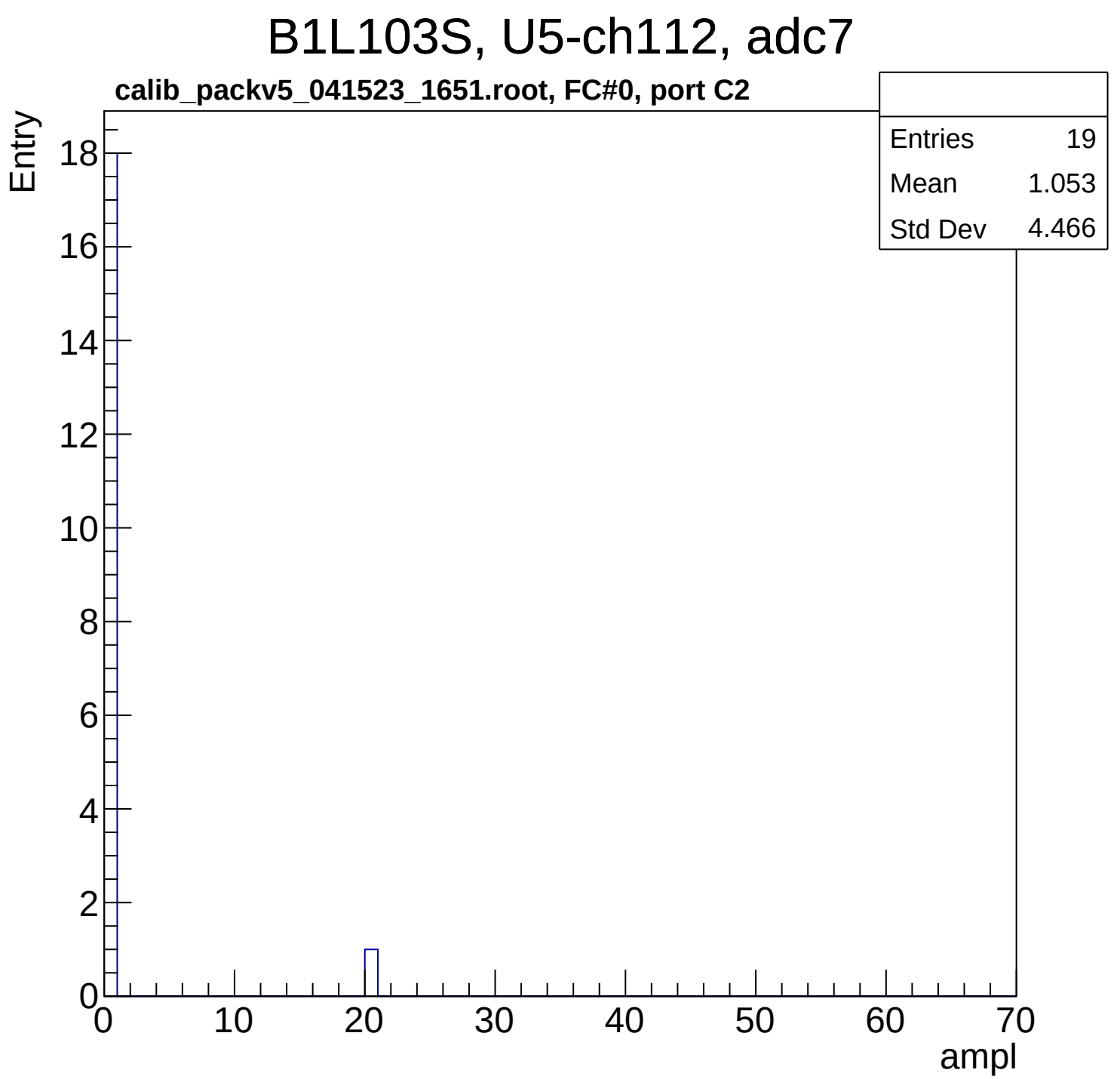
B1L103S, U5-ch112, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.053
Std Dev 4.466
Entry
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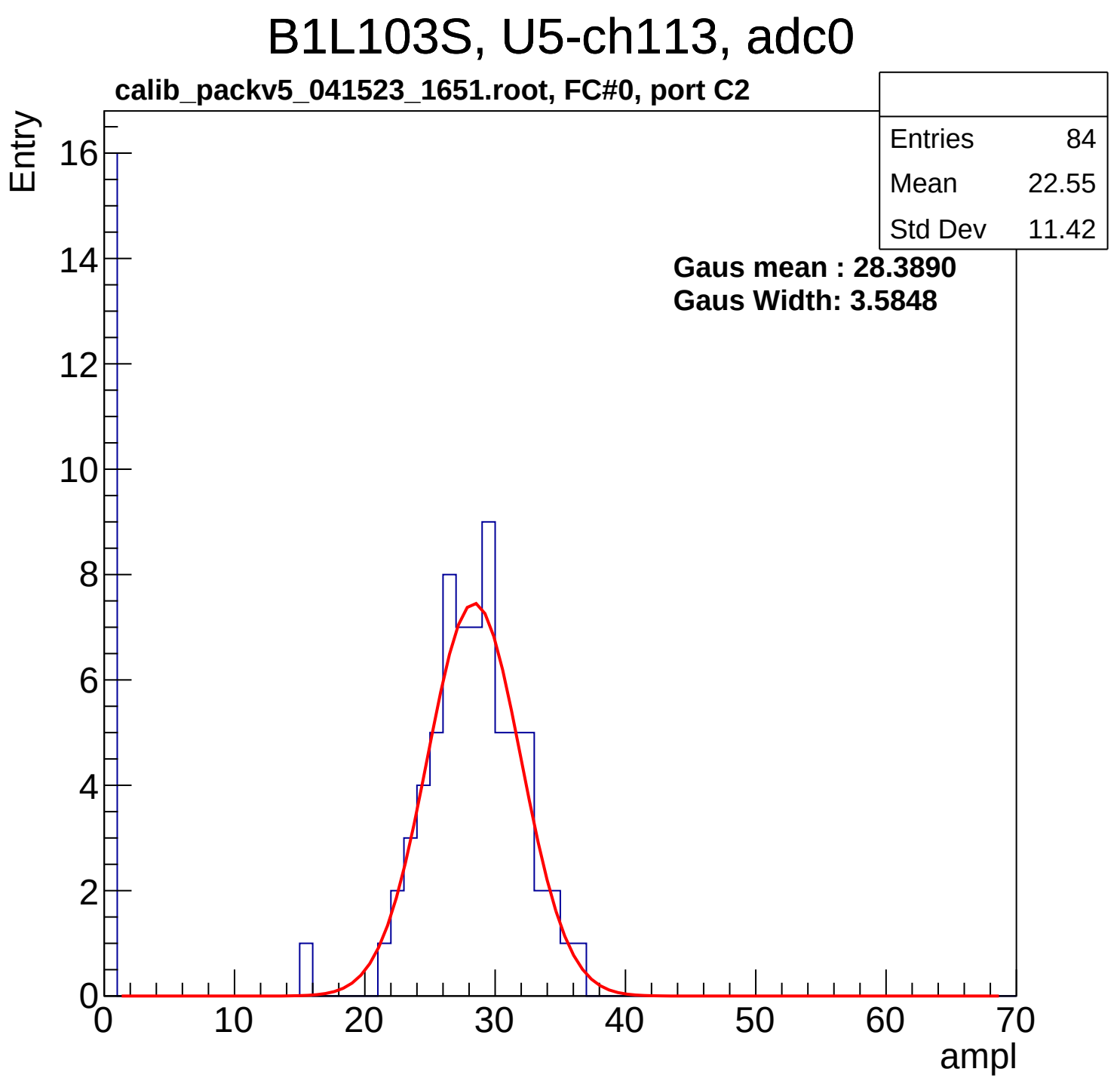
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch113, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 22.55
Std Dev 11.42
Gaus mean : 28.3890
Gaus Width: 3.5848
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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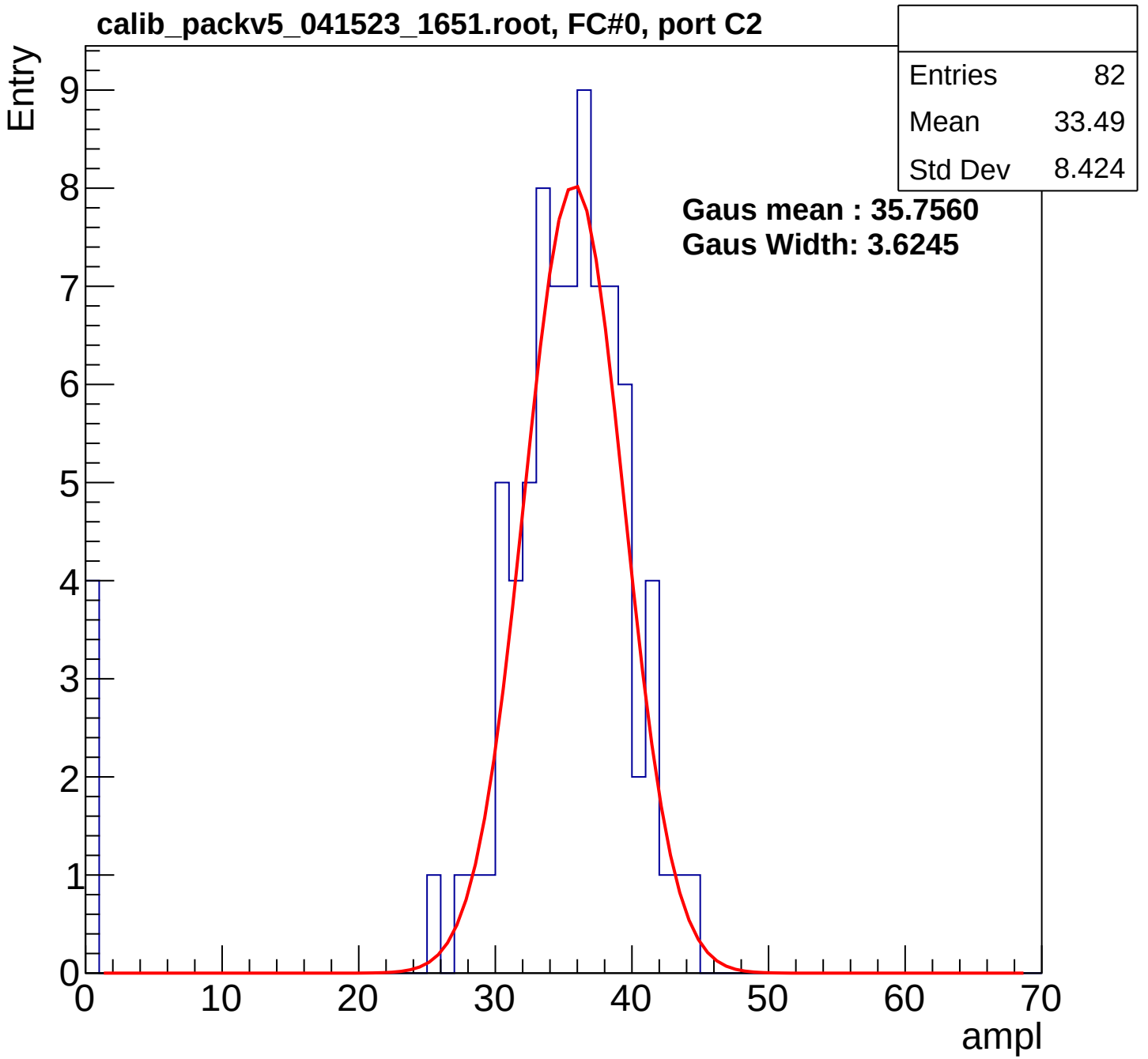
B1L103S, U5-ch113, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 33.49
Std Dev 8.424
Gaus mean : 35.7560
Gaus Width: 3.6245
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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40
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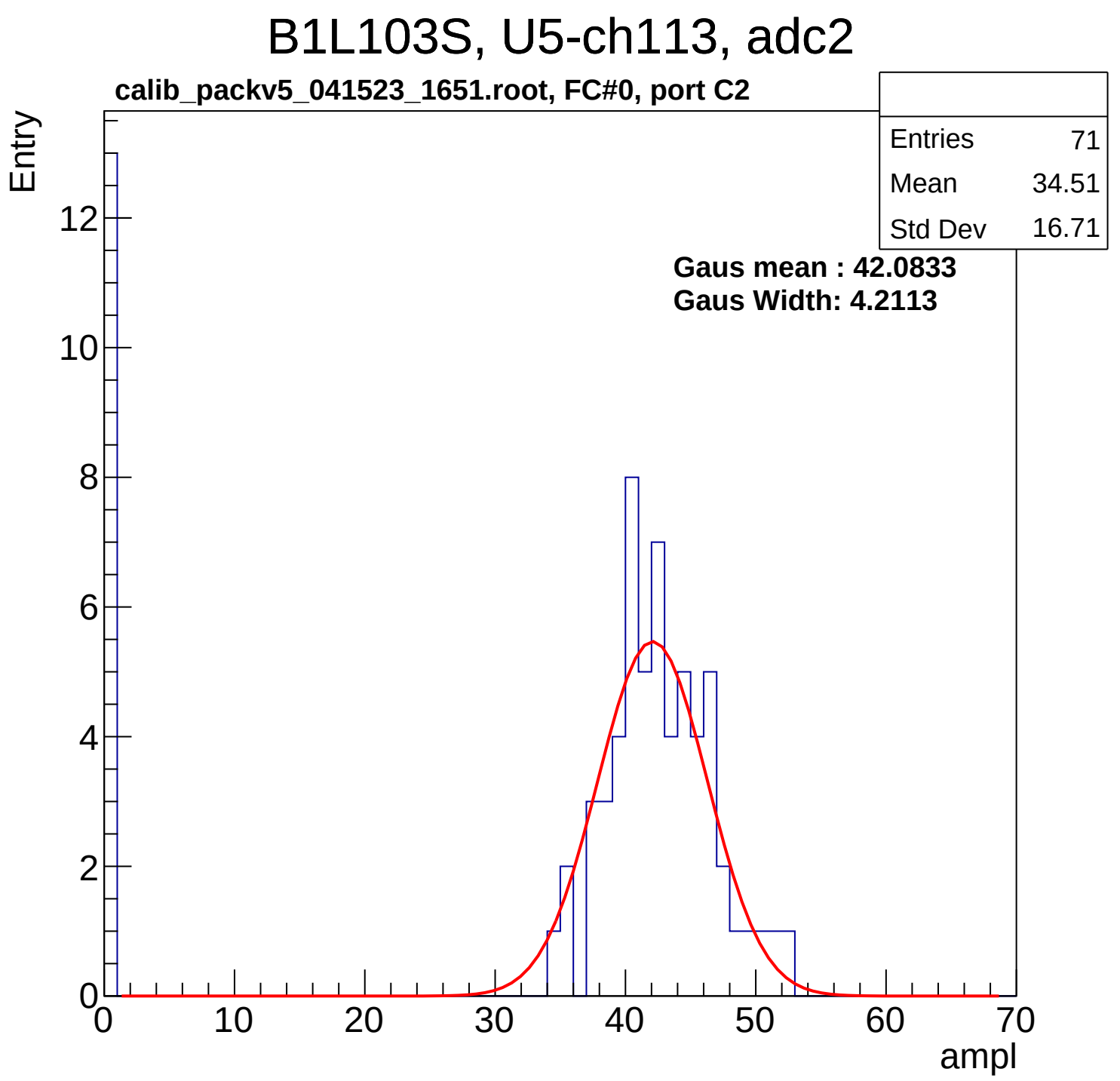
B1L103S, U5-ch113, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 34.51
Std Dev 16.71
Gaus mean : 42.0833
Gaus Width: 4.2113
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
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60
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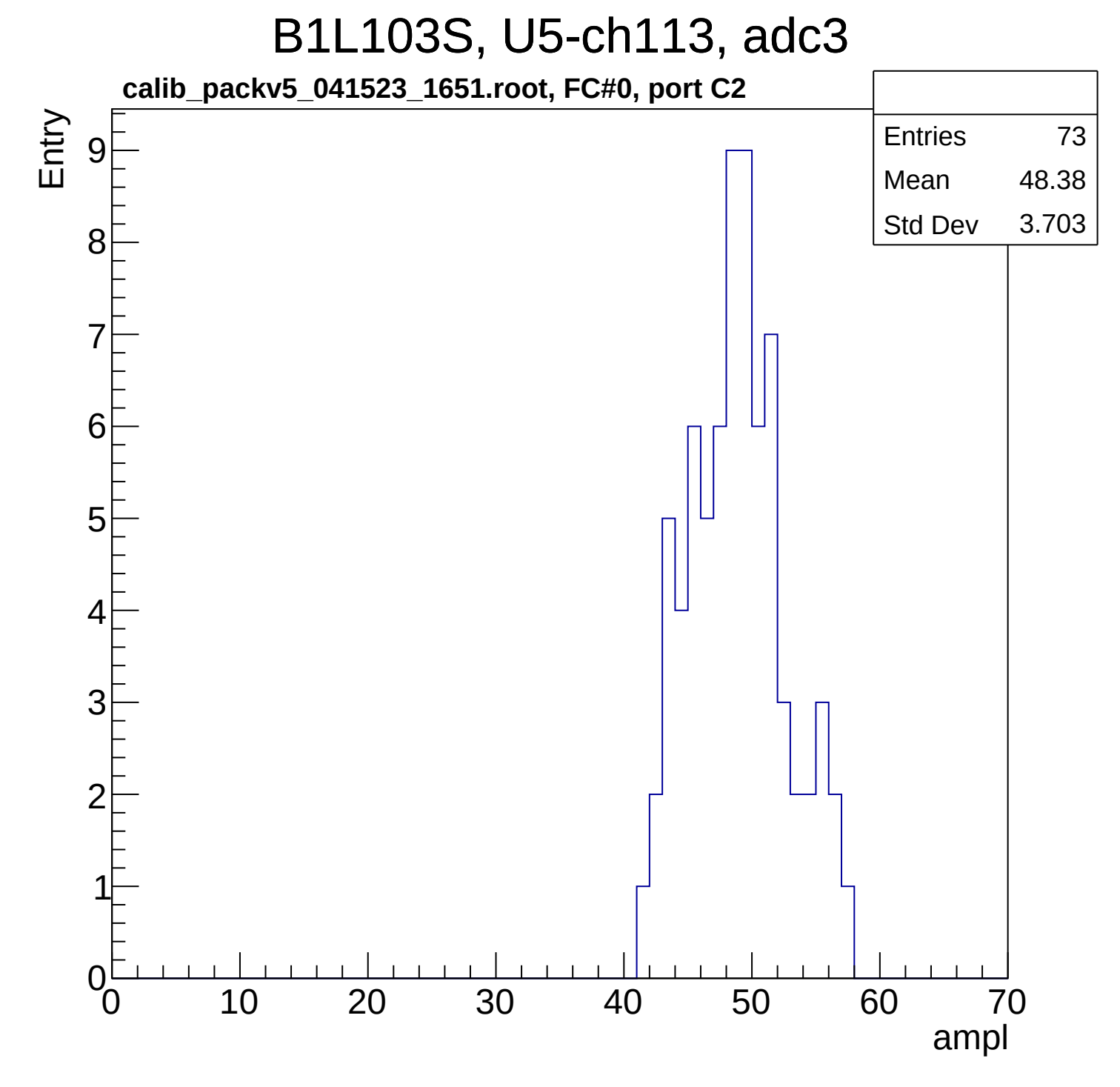
B1L103S, U5-ch113, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 48.38
Std Dev 3.703
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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40
50
60
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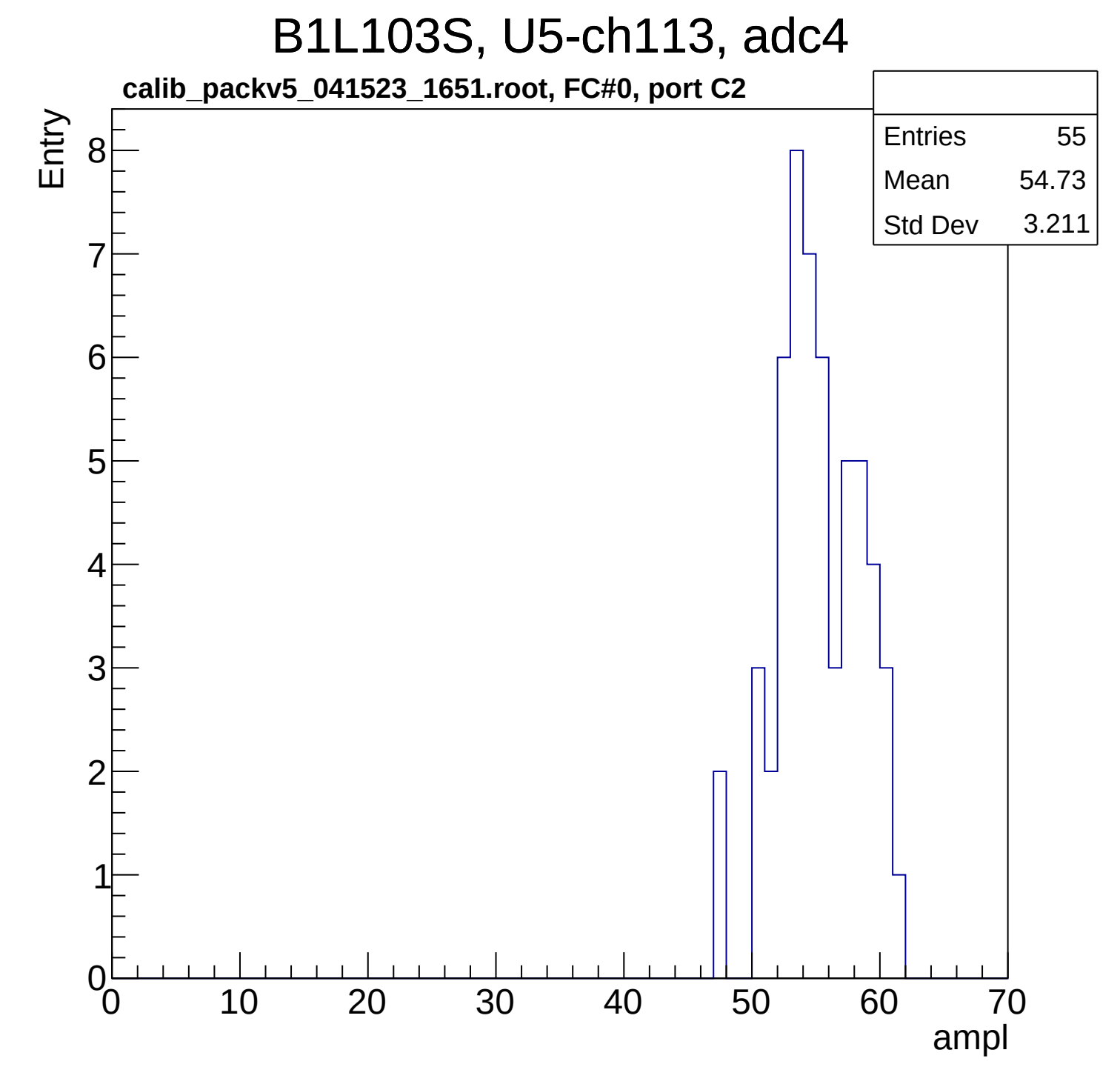
B1L103S, U5-ch113, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 54.73
Std Dev 3.211
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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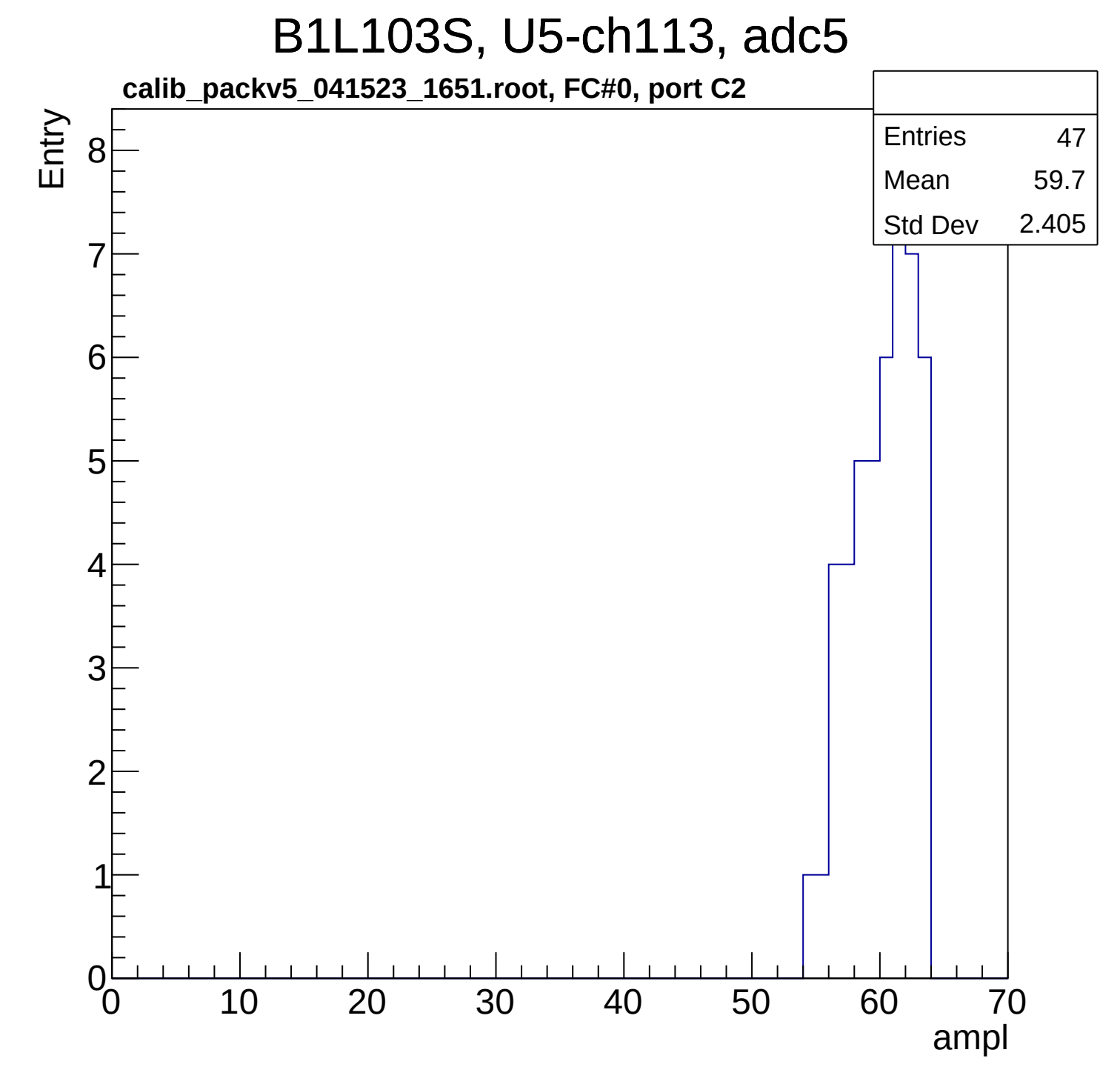
B1L103S, U5-ch113, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 59.7
Std Dev 2.405
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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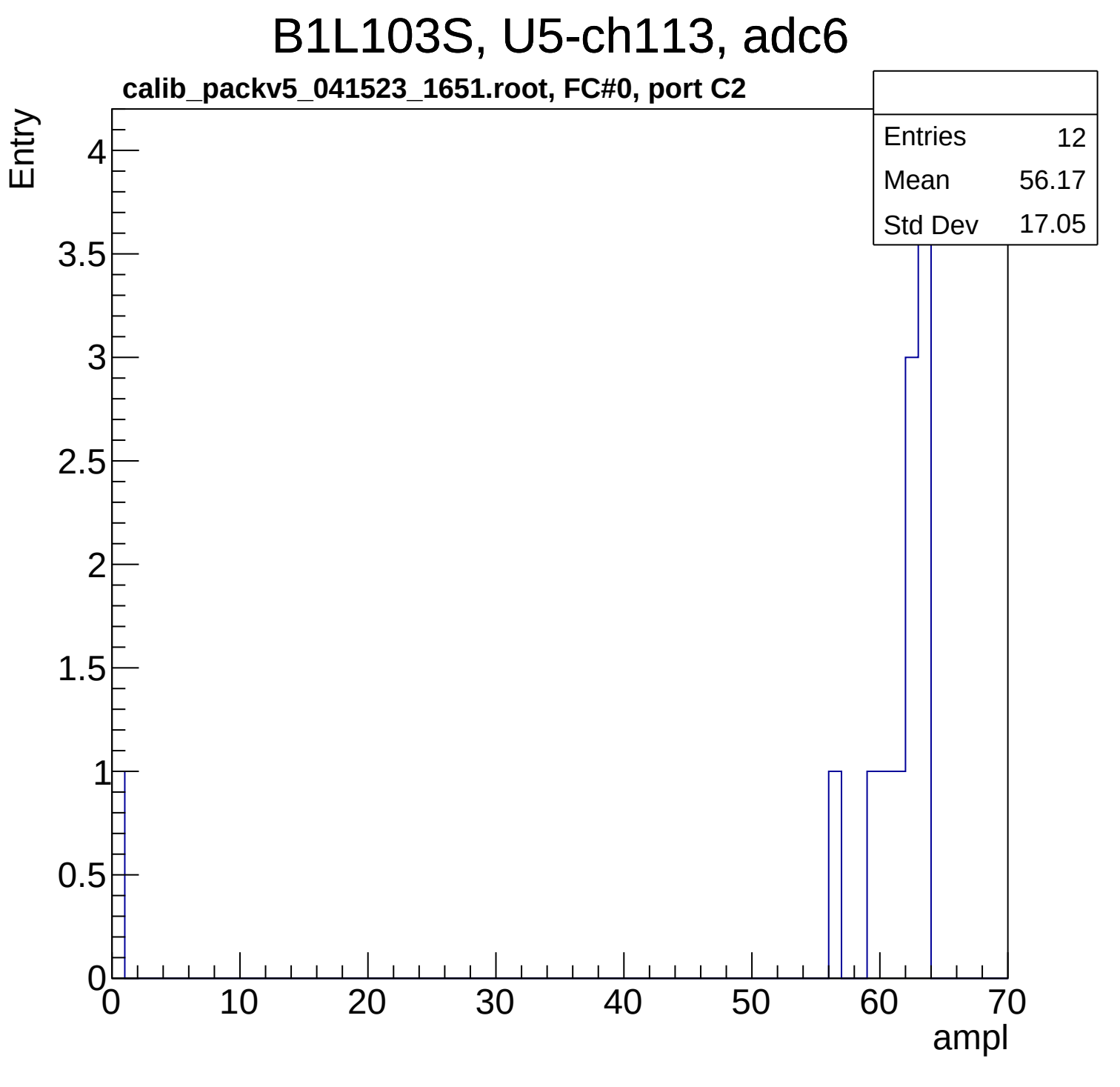
B1L103S, U5-ch113, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.17
Std Dev 17.05
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
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60
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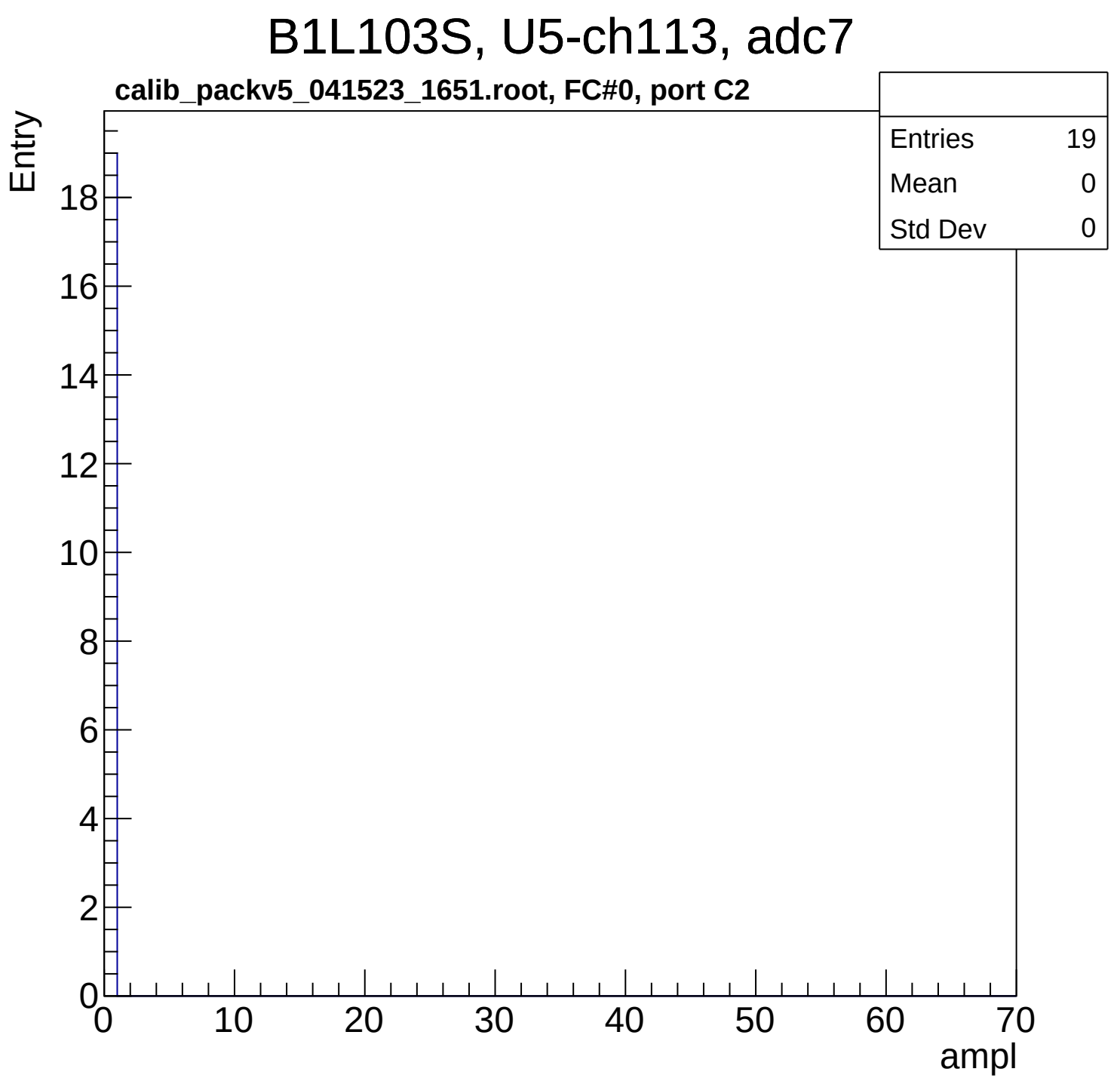
B1L103S, U5-ch113, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
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20
30
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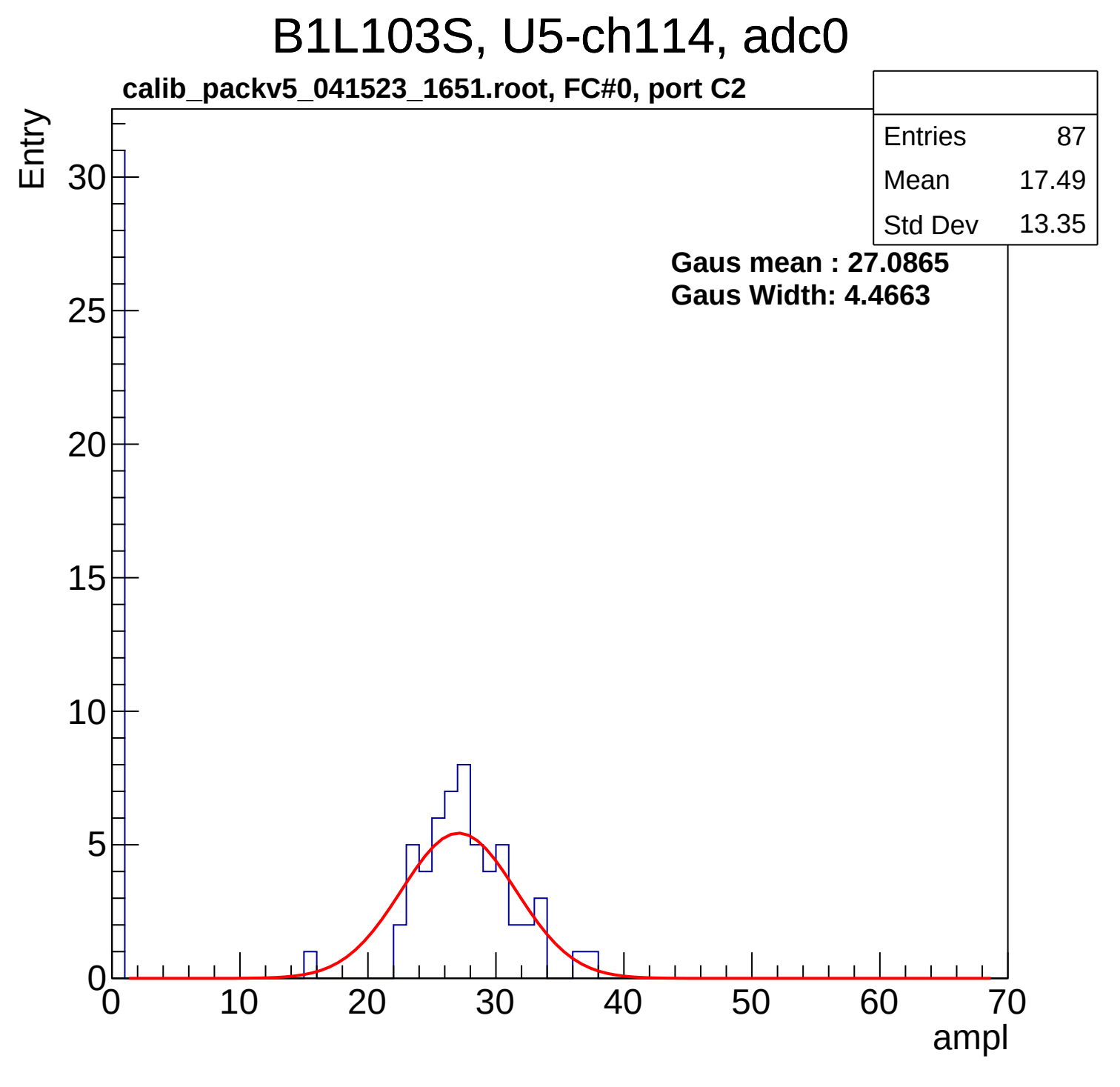
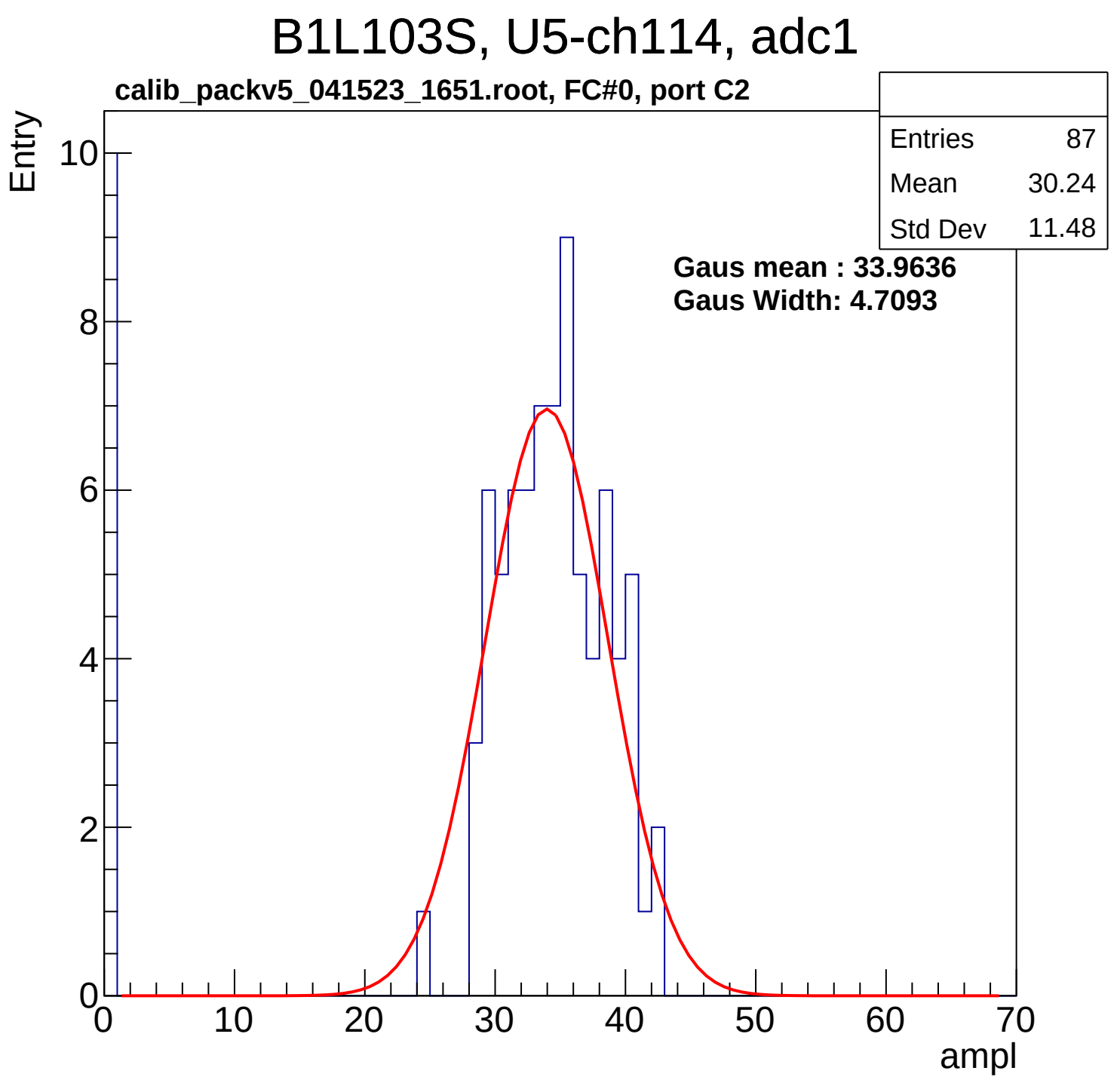
50
60
70
ampl


B1L103S, U5-ch114, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 17.49
Std Dev 13.35
Gaus mean : 27.0865
Gaus Width: 4.4663
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70


B1L103S, U5-ch114, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 30.24
Std Dev 11.48
Gaus mean : 33.9636
Gaus Width: 4.7093
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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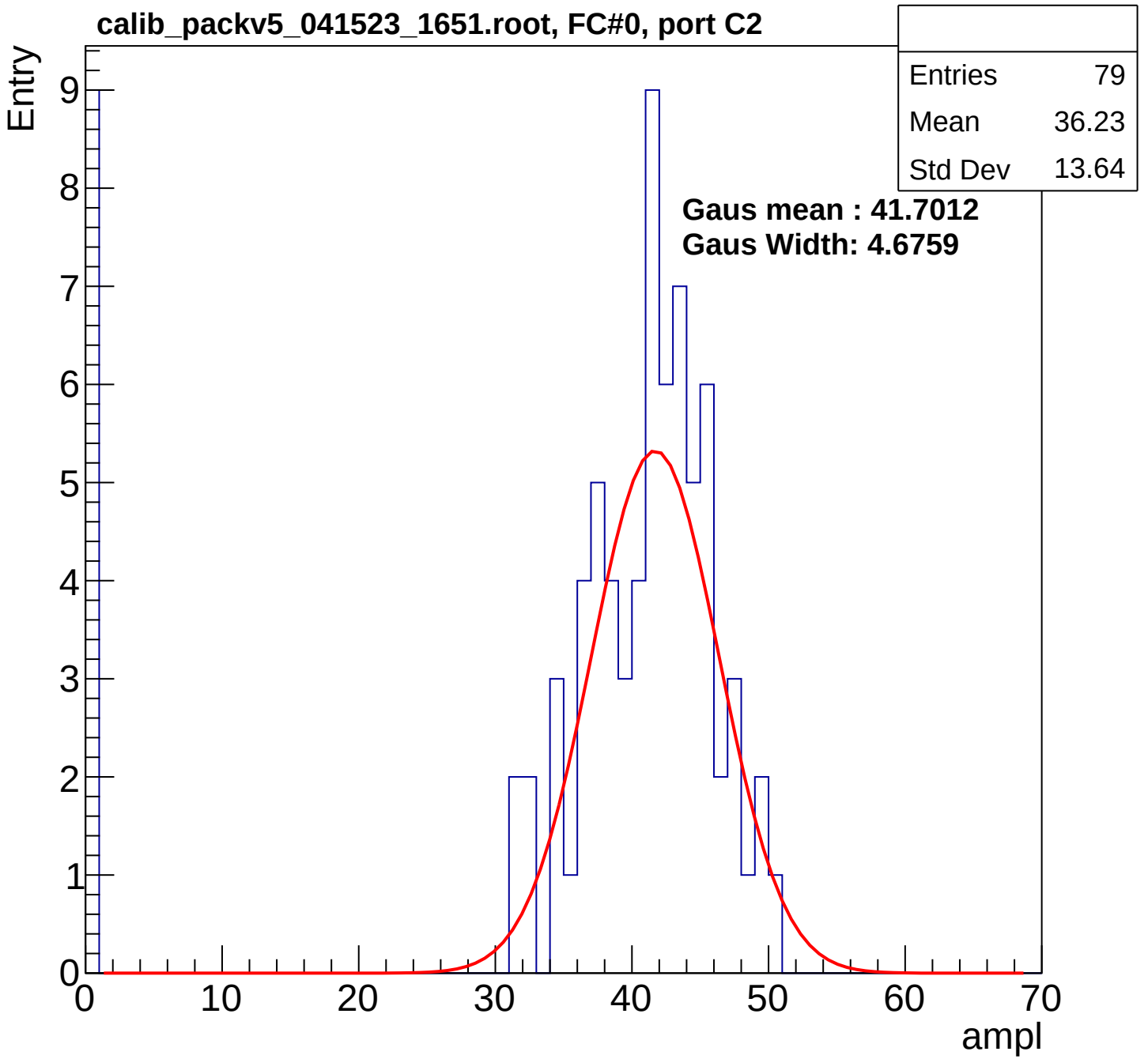
B1L103S, U5-ch114, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 36.23
Std Dev 13.64
Gaus mean : 41.7012
Gaus Width: 4.6759
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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40
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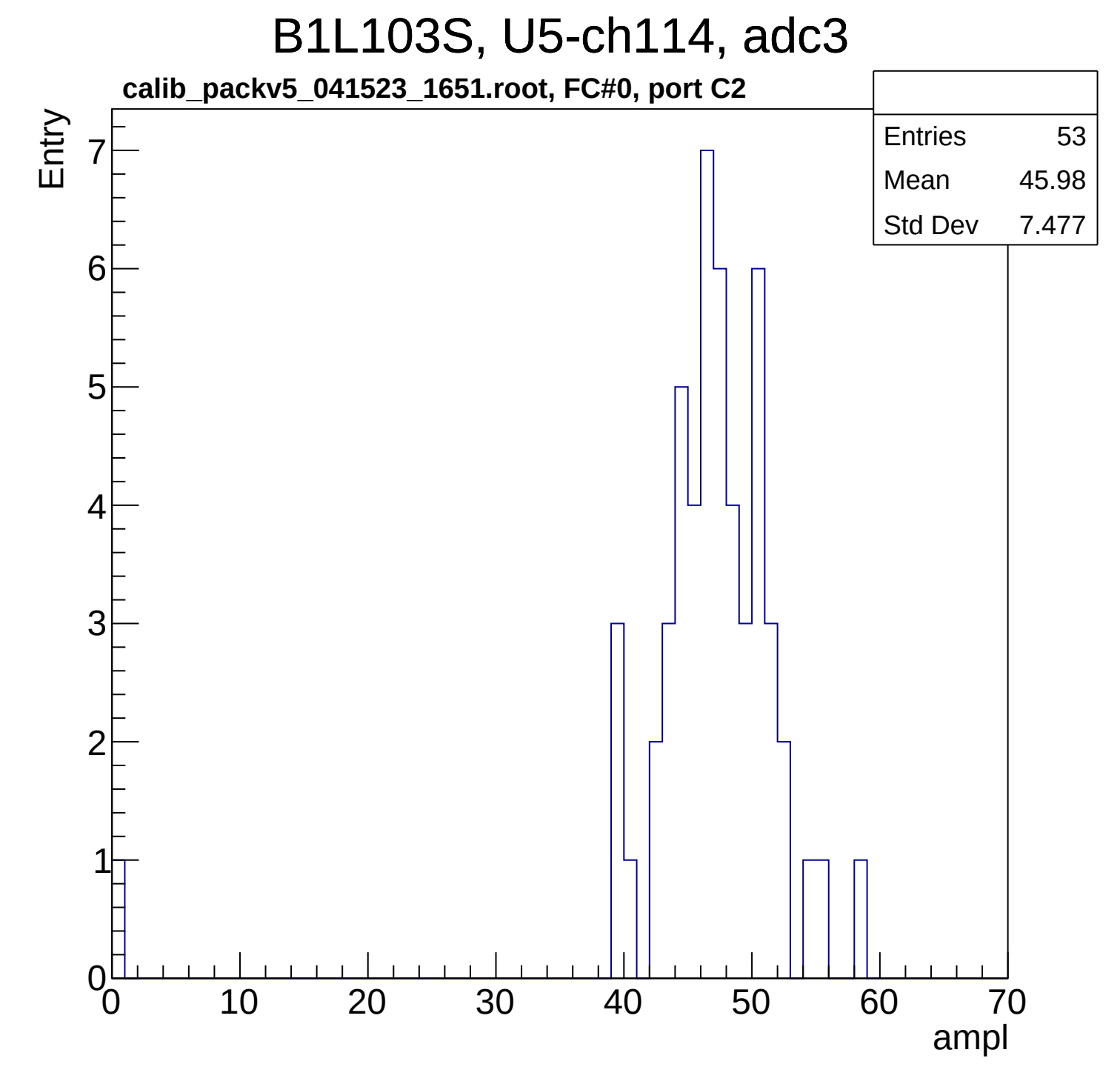
B1L103S, U5-ch114, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 45.98
Std Dev 7.477
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
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60
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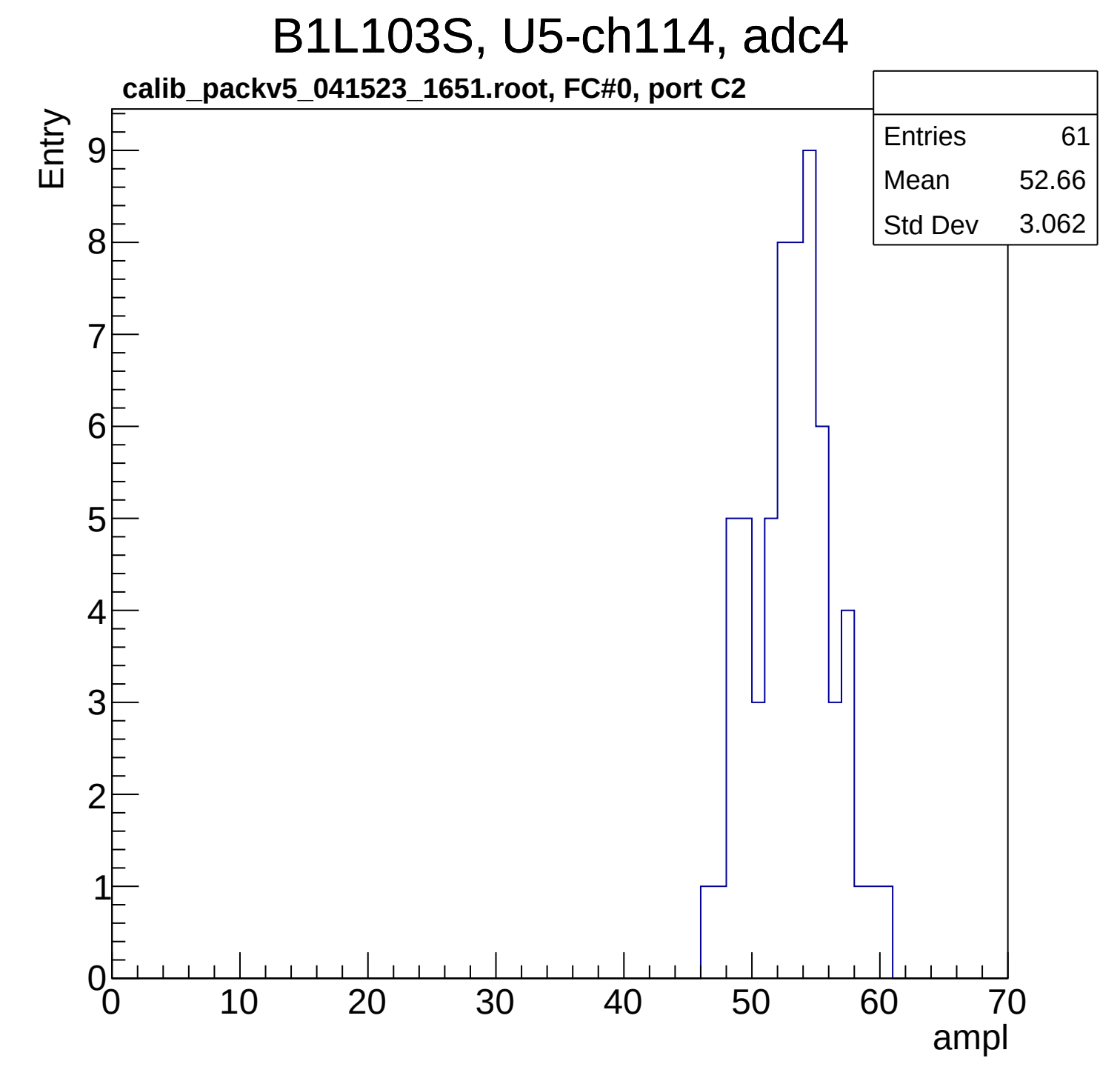
B1L103S, U5-ch114, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 52.66
Std Dev 3.062
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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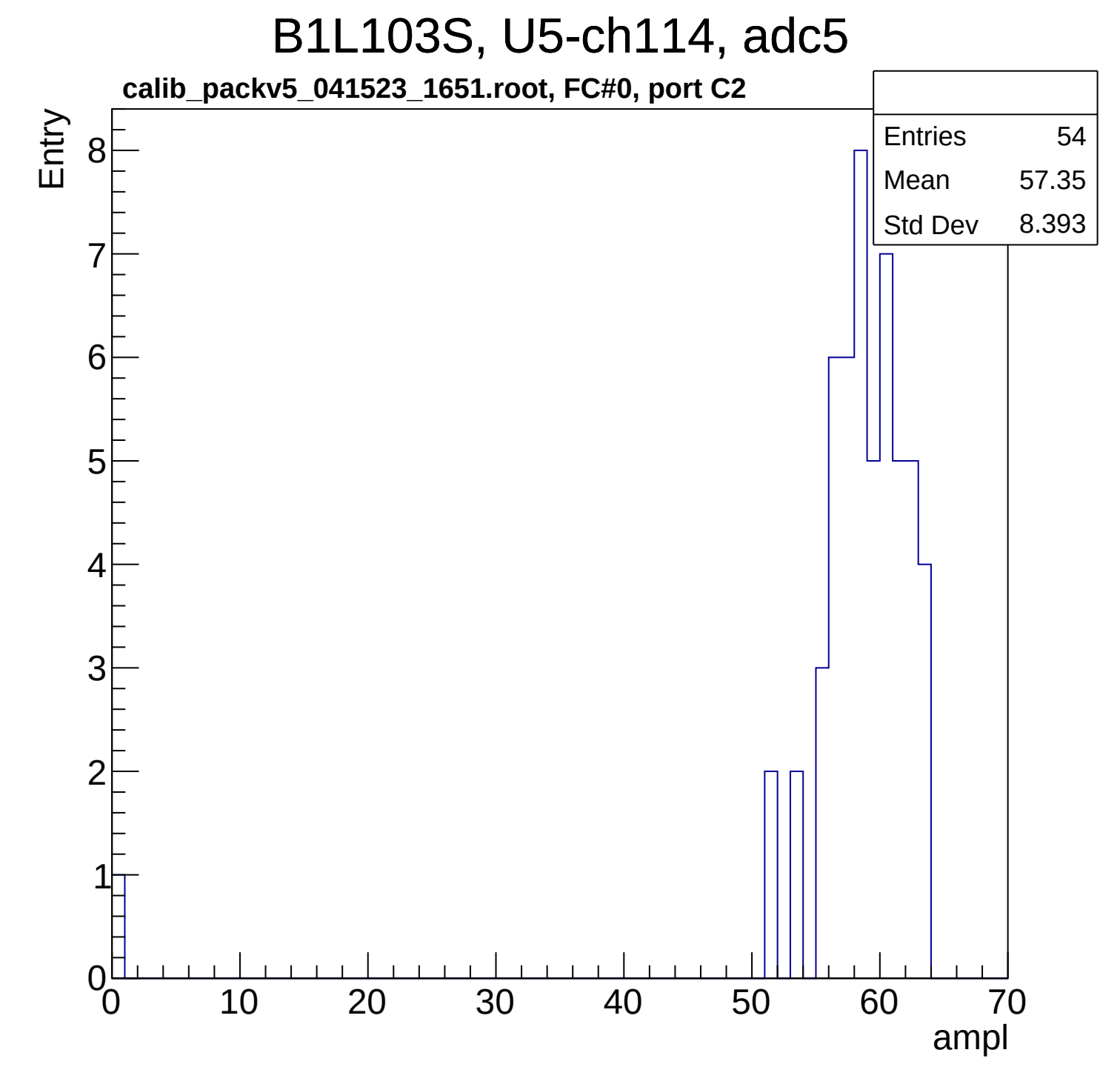
B1L103S, U5-ch114, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.35
Std Dev 8.393
Entry
ampl
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2
3
4
5
6
7
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0
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60
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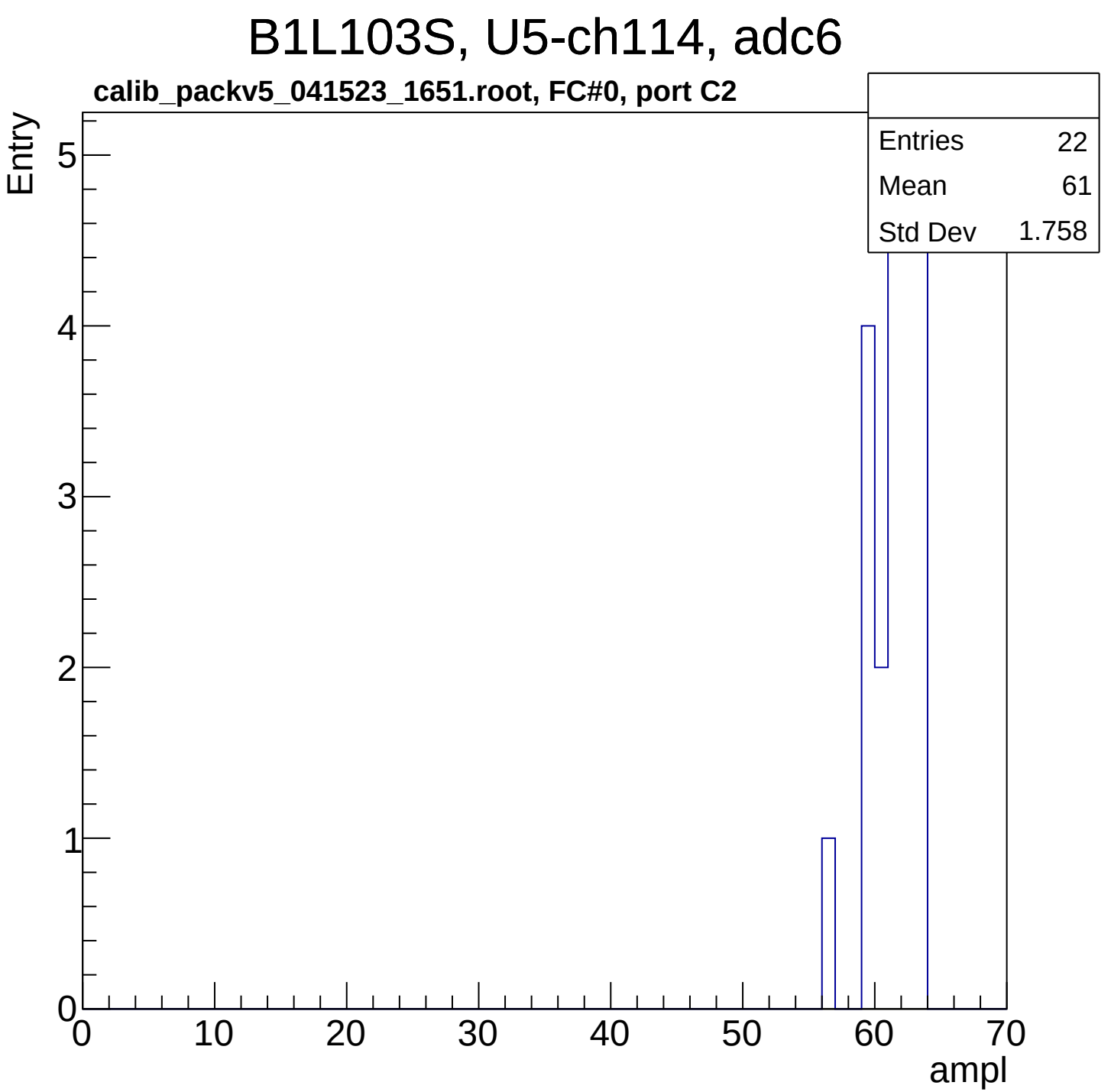
B1L103S, U5-ch114, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 61
Std Dev 1.758
Entry
ampl
0
1
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4
5
0
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20
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40
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60
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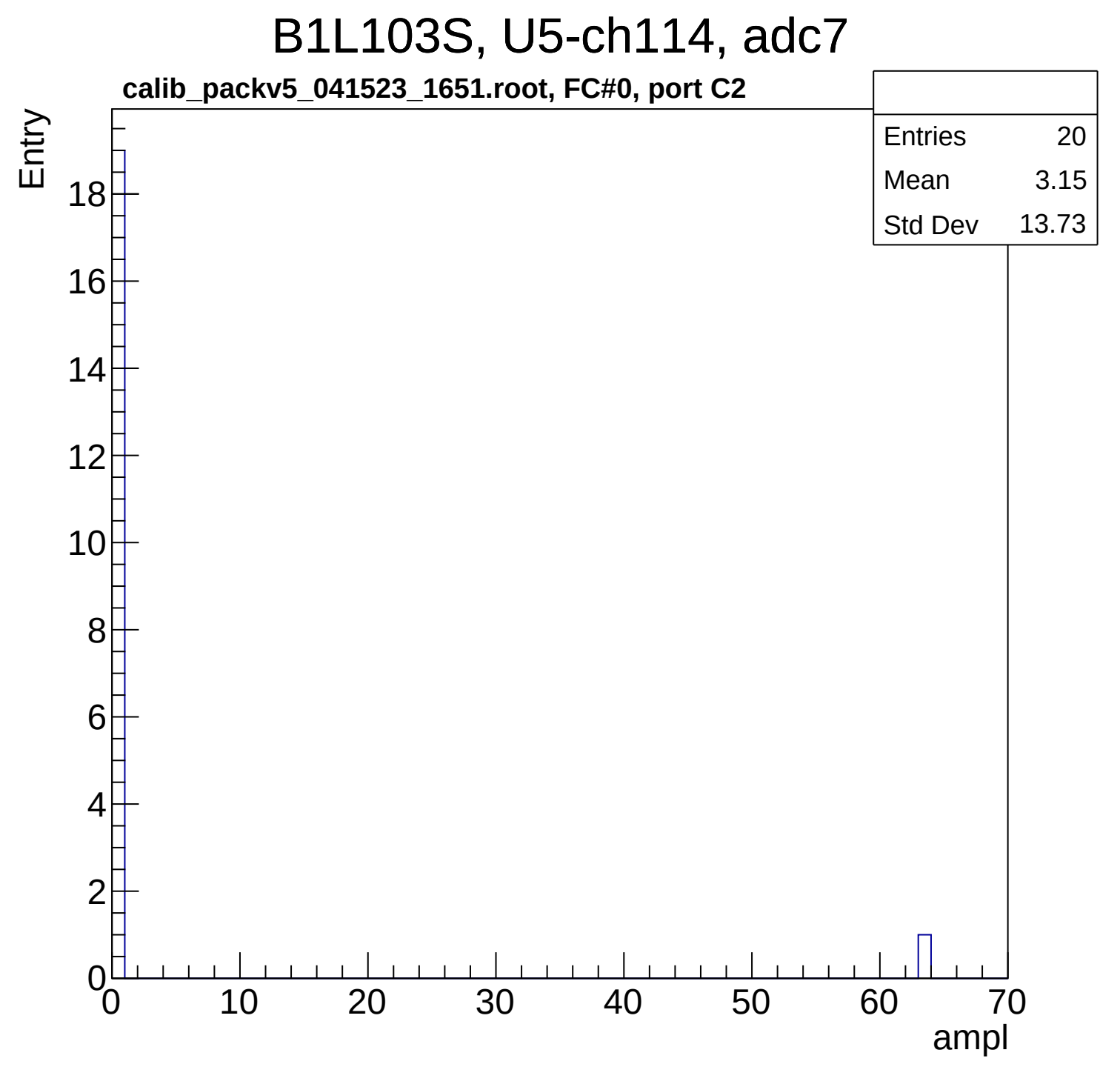
B1L103S, U5-ch114, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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6
8
10
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14
16
18
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10
20
30
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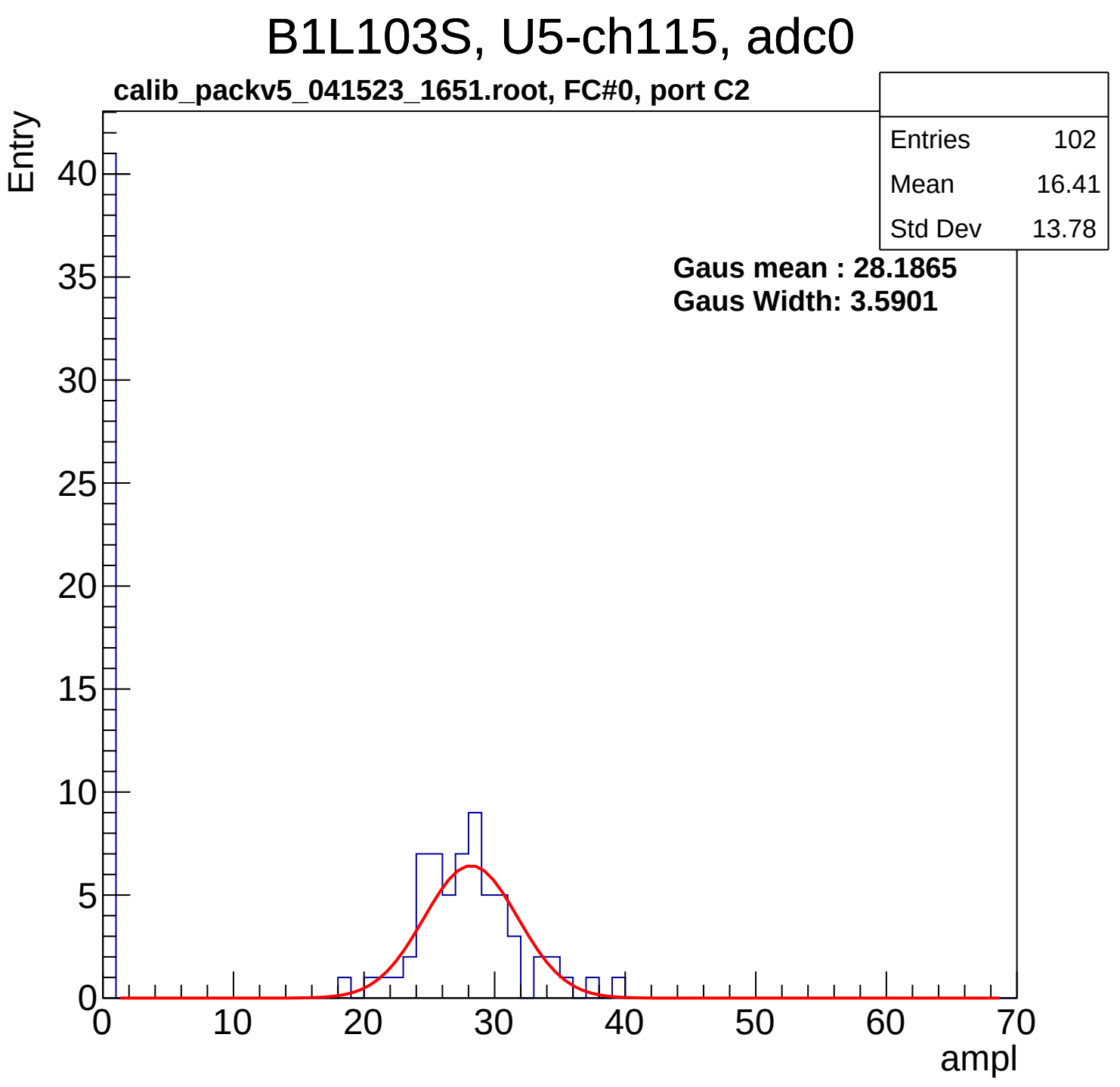
50
60
70
ampl


B1L103S, U5-ch115, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 16.41
Std Dev 13.78
Gaus mean : 28.1865
Gaus Width: 3.5901
Entry
ampl
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5
10
15
20
25
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35
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0
10
20
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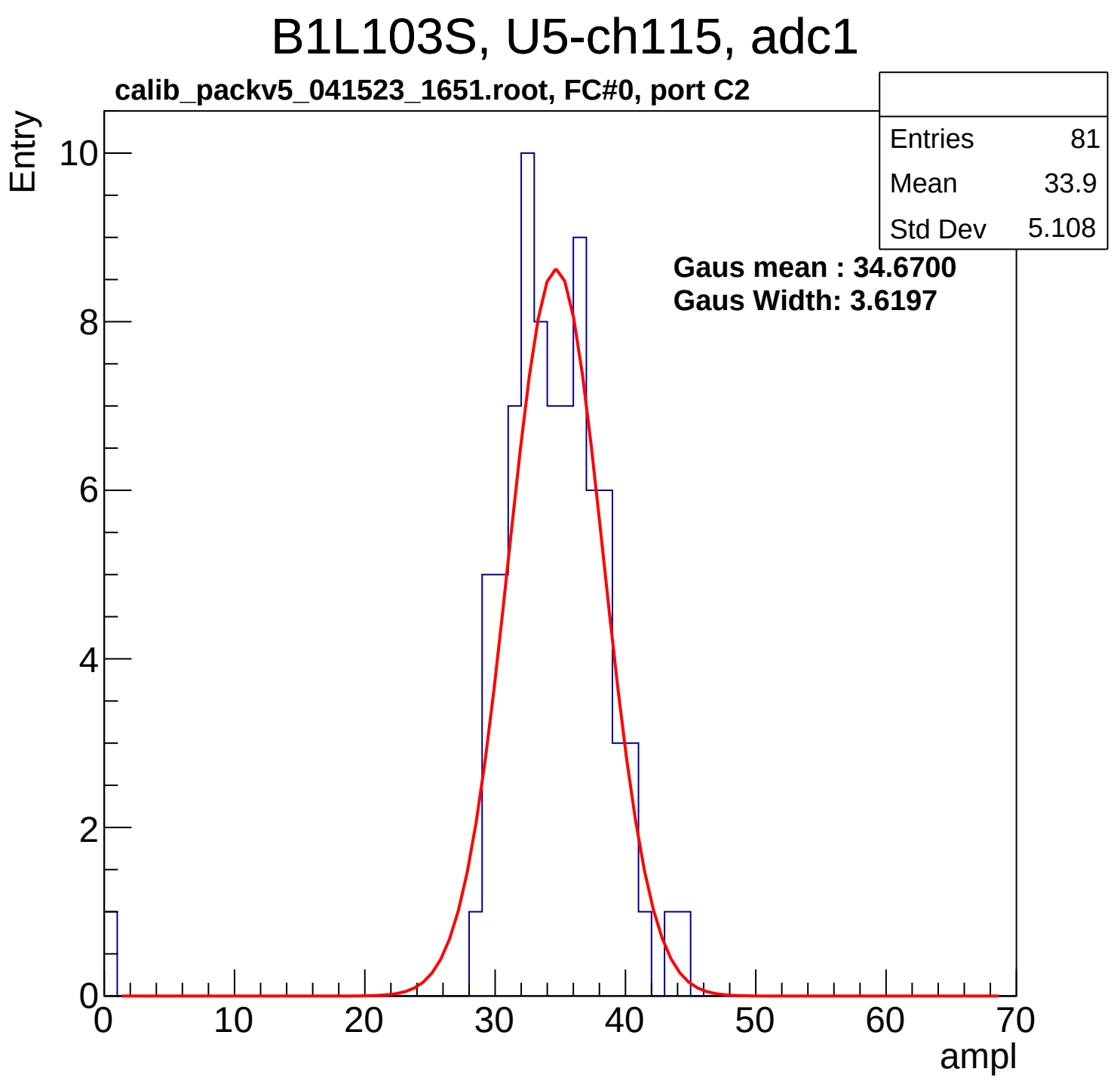
40
50
60
70


B1L103S, U5-ch115, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 33.9
Std Dev 5.108
Gaus mean : 34.6700
Gaus Width: 3.6197
Entry
ampl
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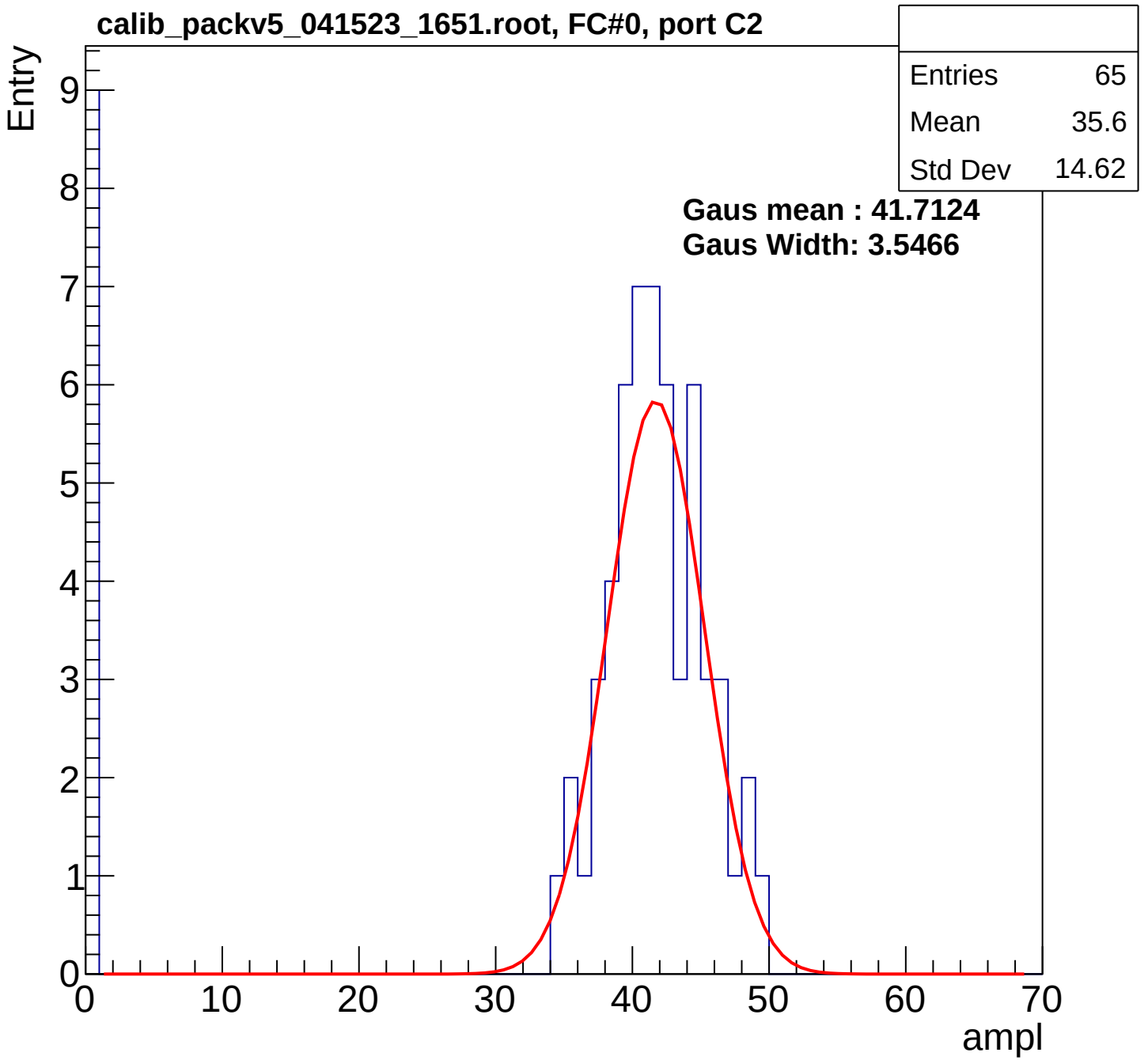
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U5-ch115, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 35.6
Std Dev 14.62
Gaus mean : 41.7124
Gaus Width: 3.5466
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
30
40
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60
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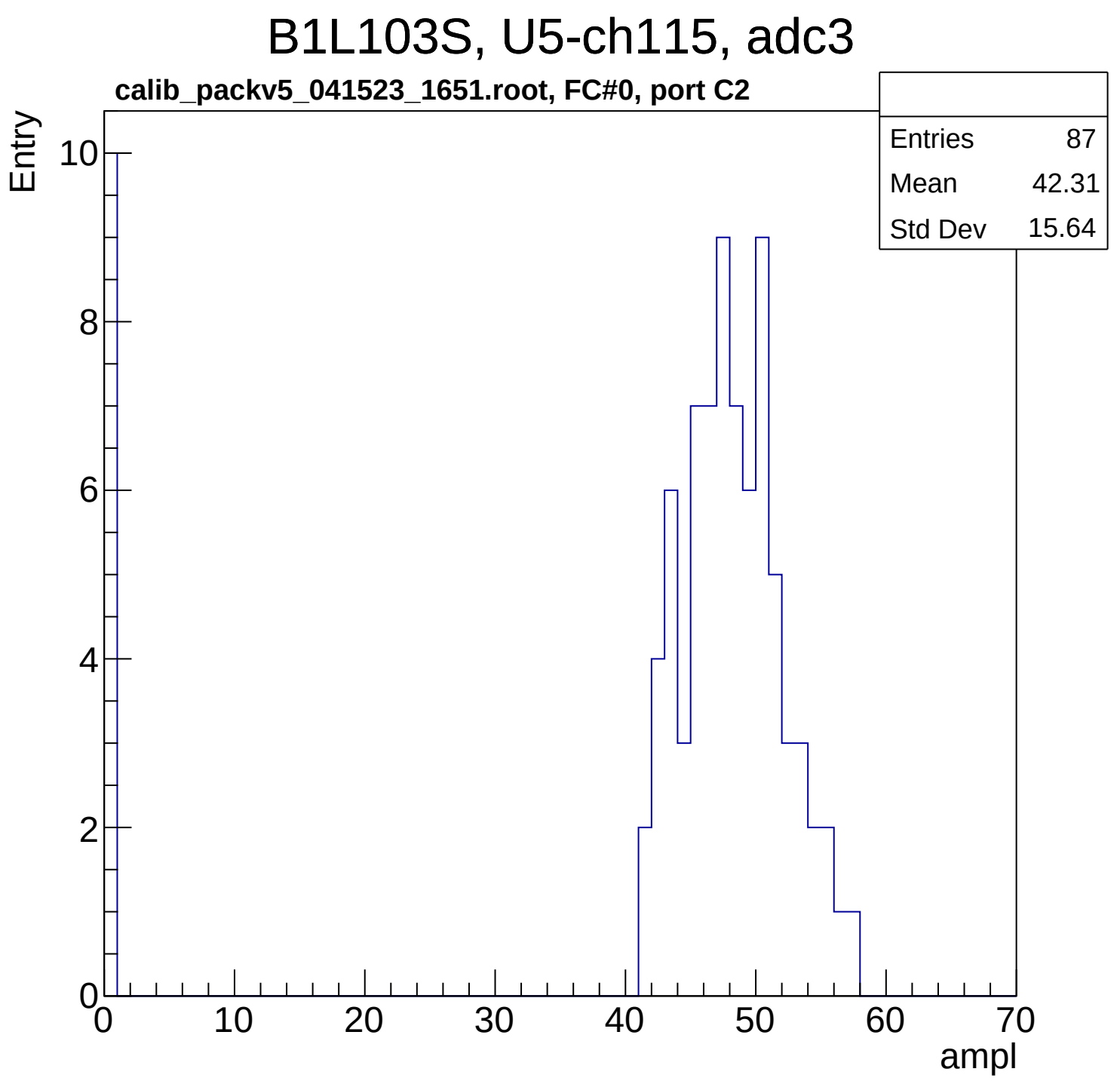
B1L103S, U5-ch115, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 42.31
Std Dev 15.64
Entry
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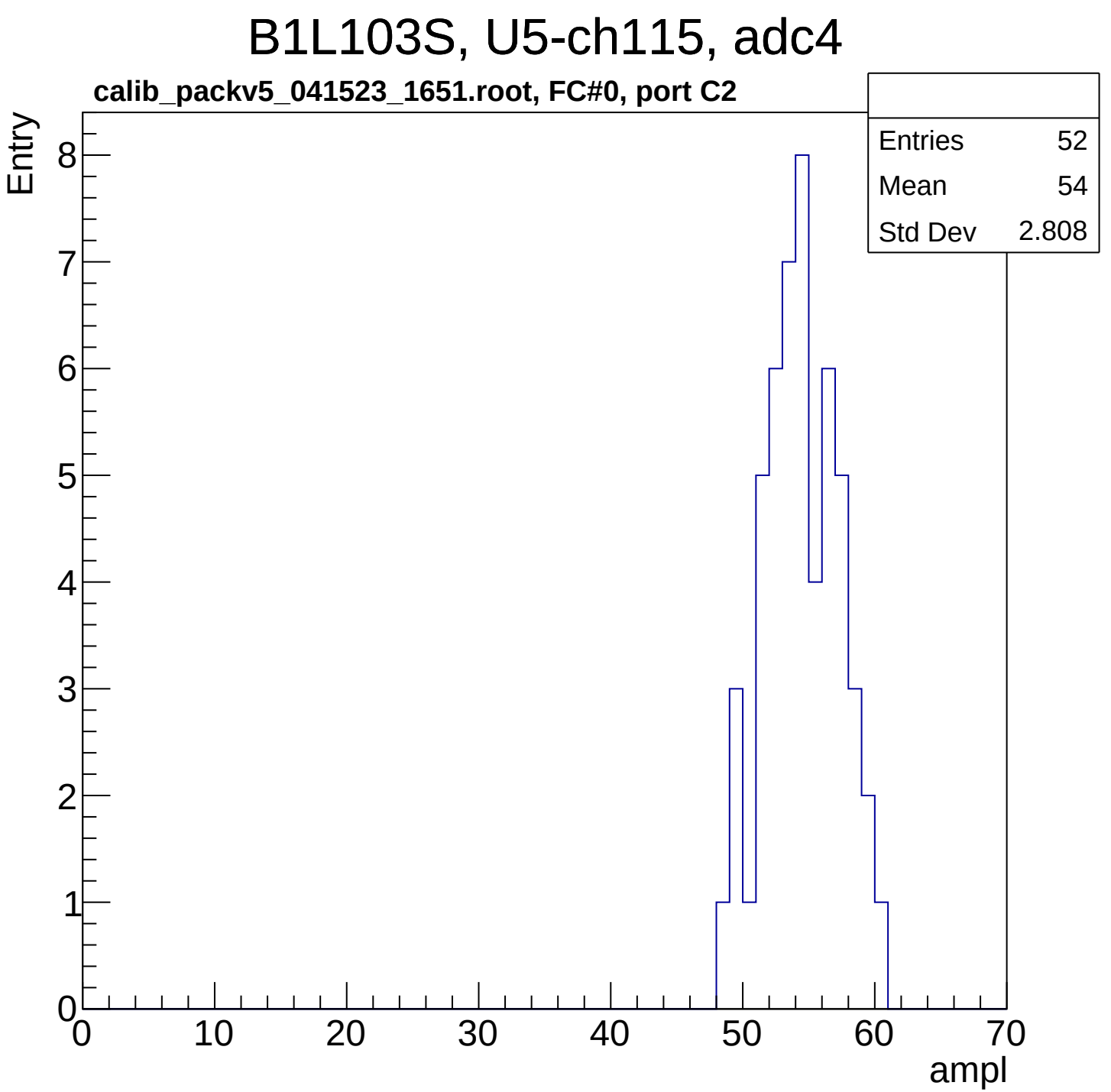
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch115, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 54
Std Dev 2.808
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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60
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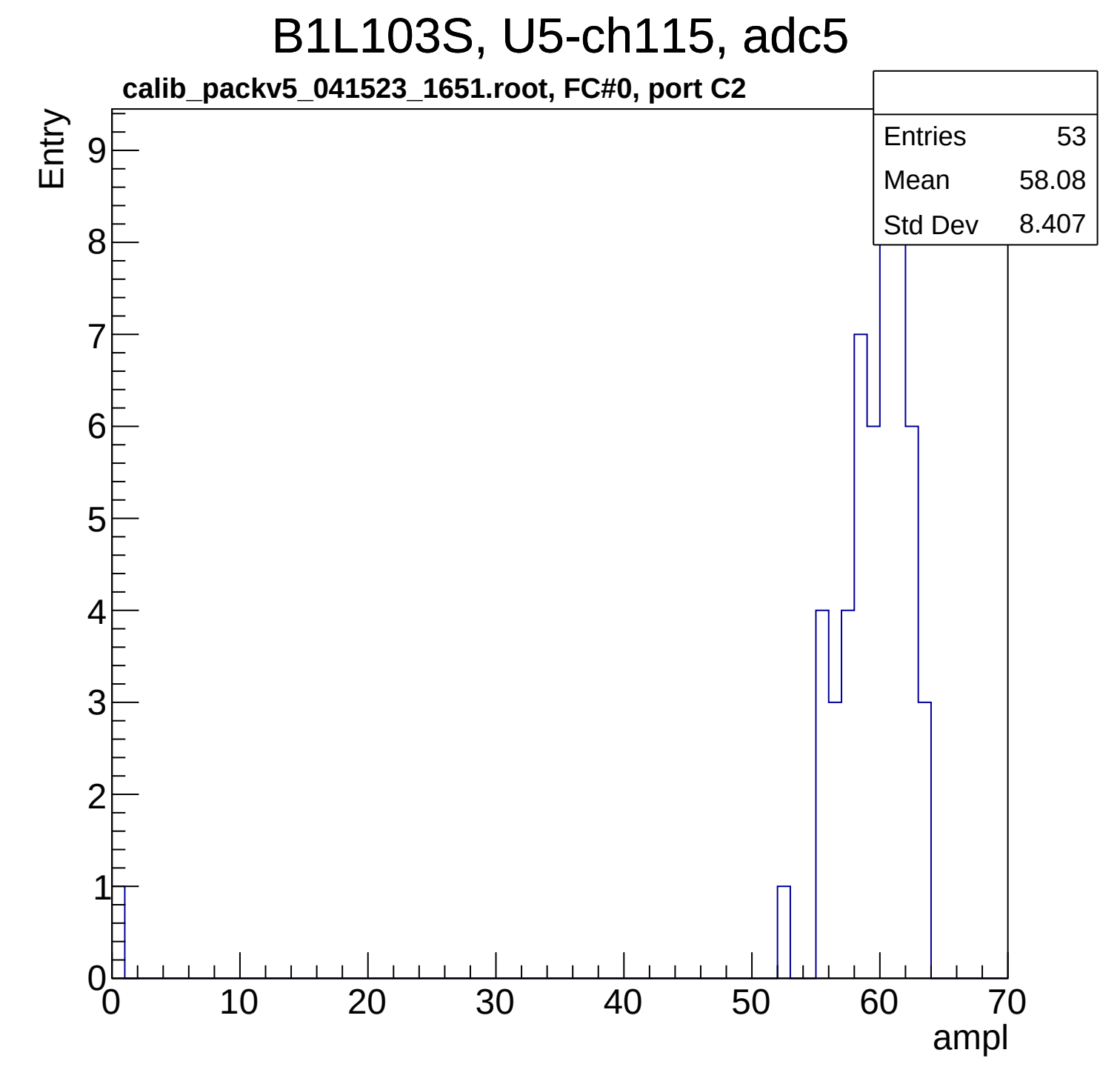
B1L103S, U5-ch115, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.08
Std Dev 8.407
Entry
ampl
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2
3
4
5
6
7
8
9
0
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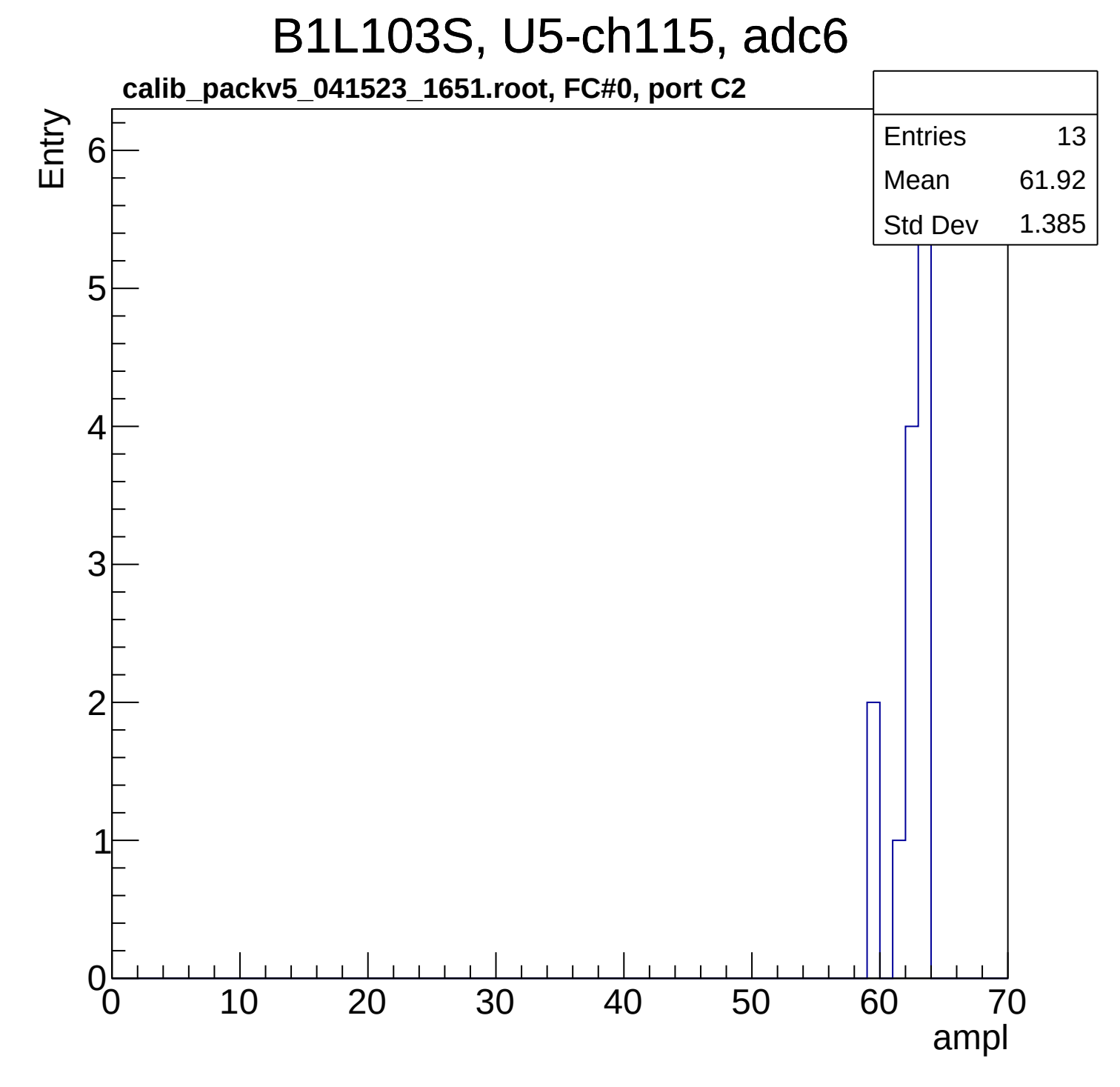
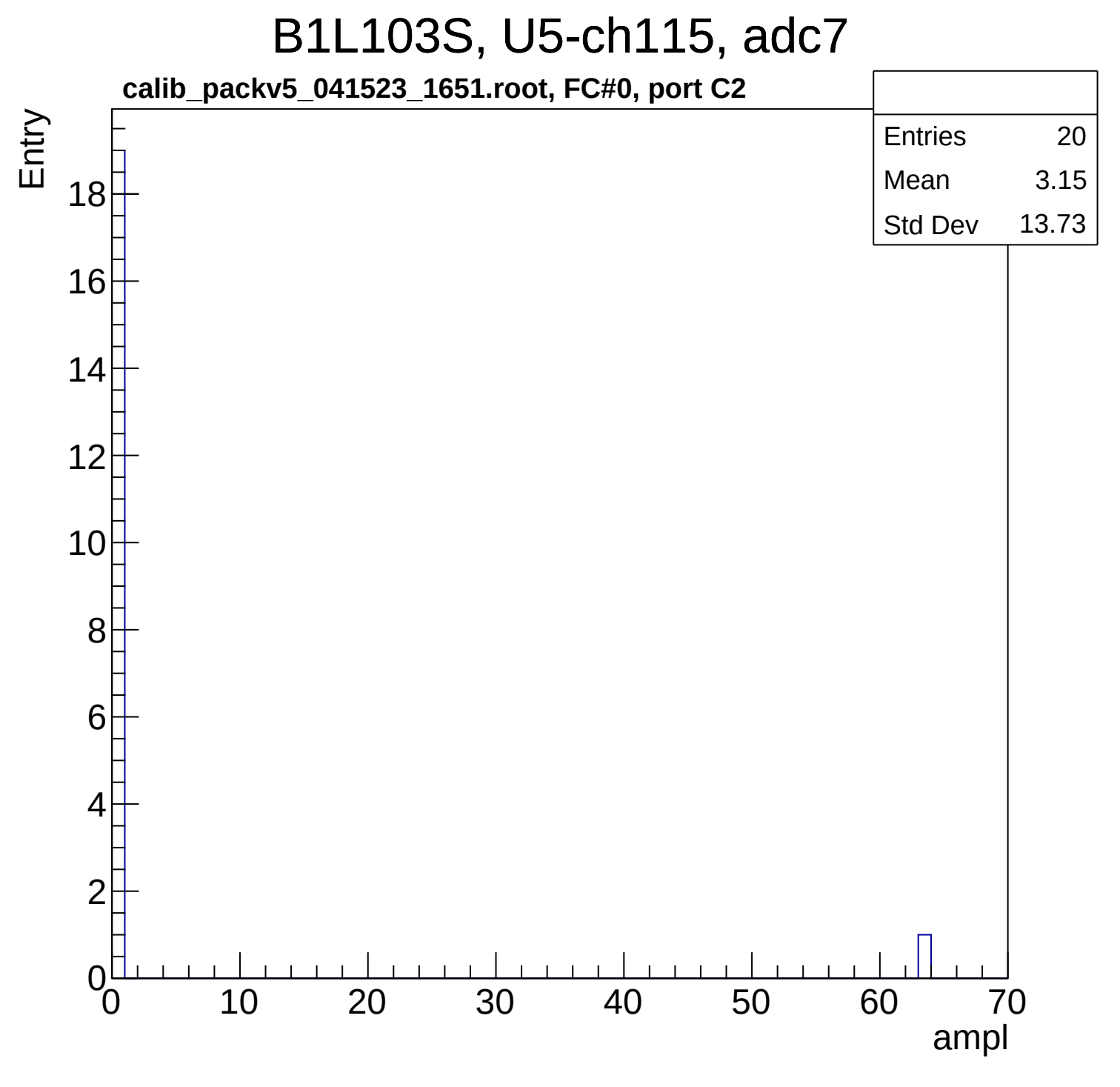

B1L103S, U5-ch115, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.92
Std Dev 1.385
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U5-ch115, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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8
10
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14
16
18
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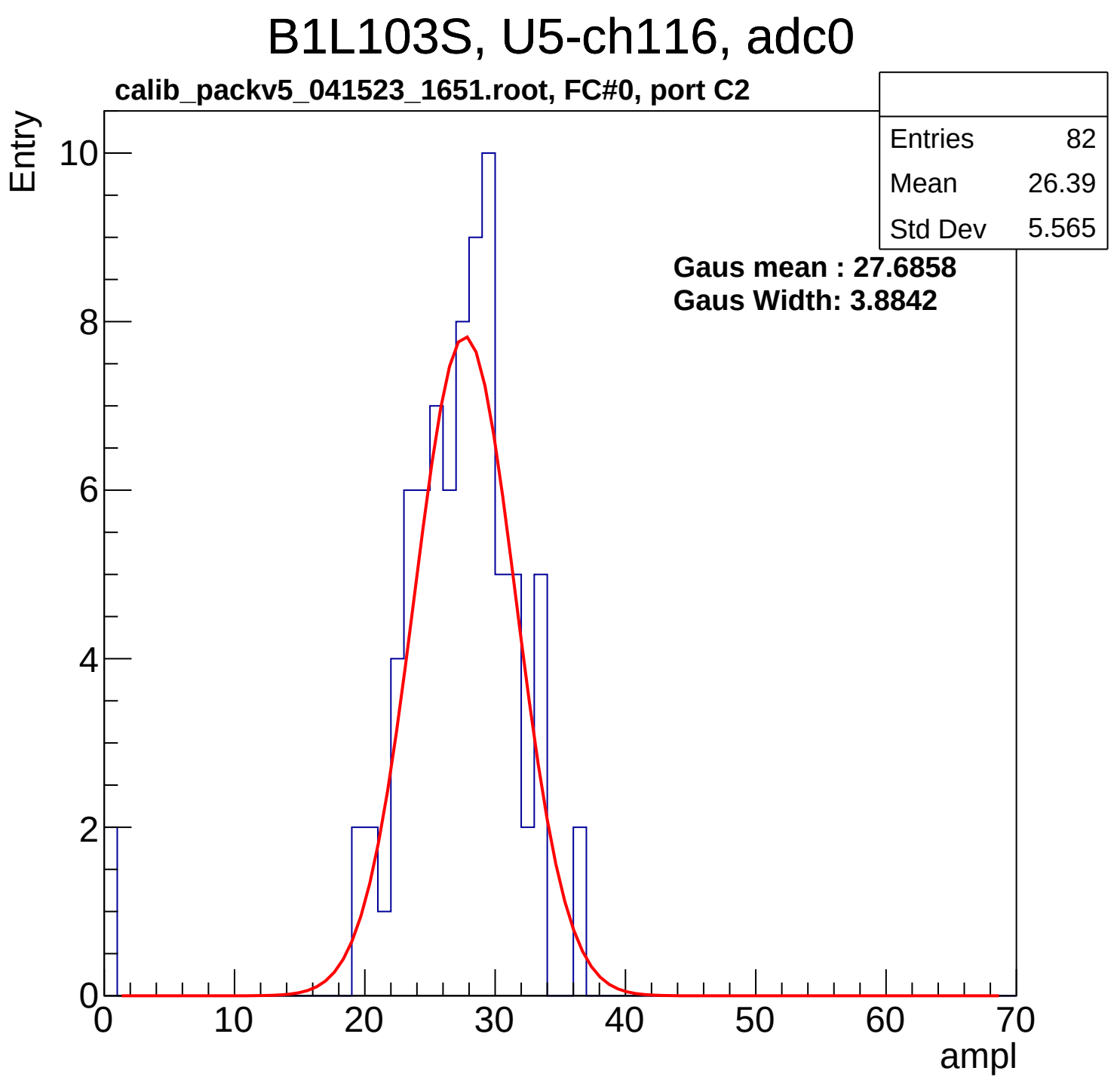
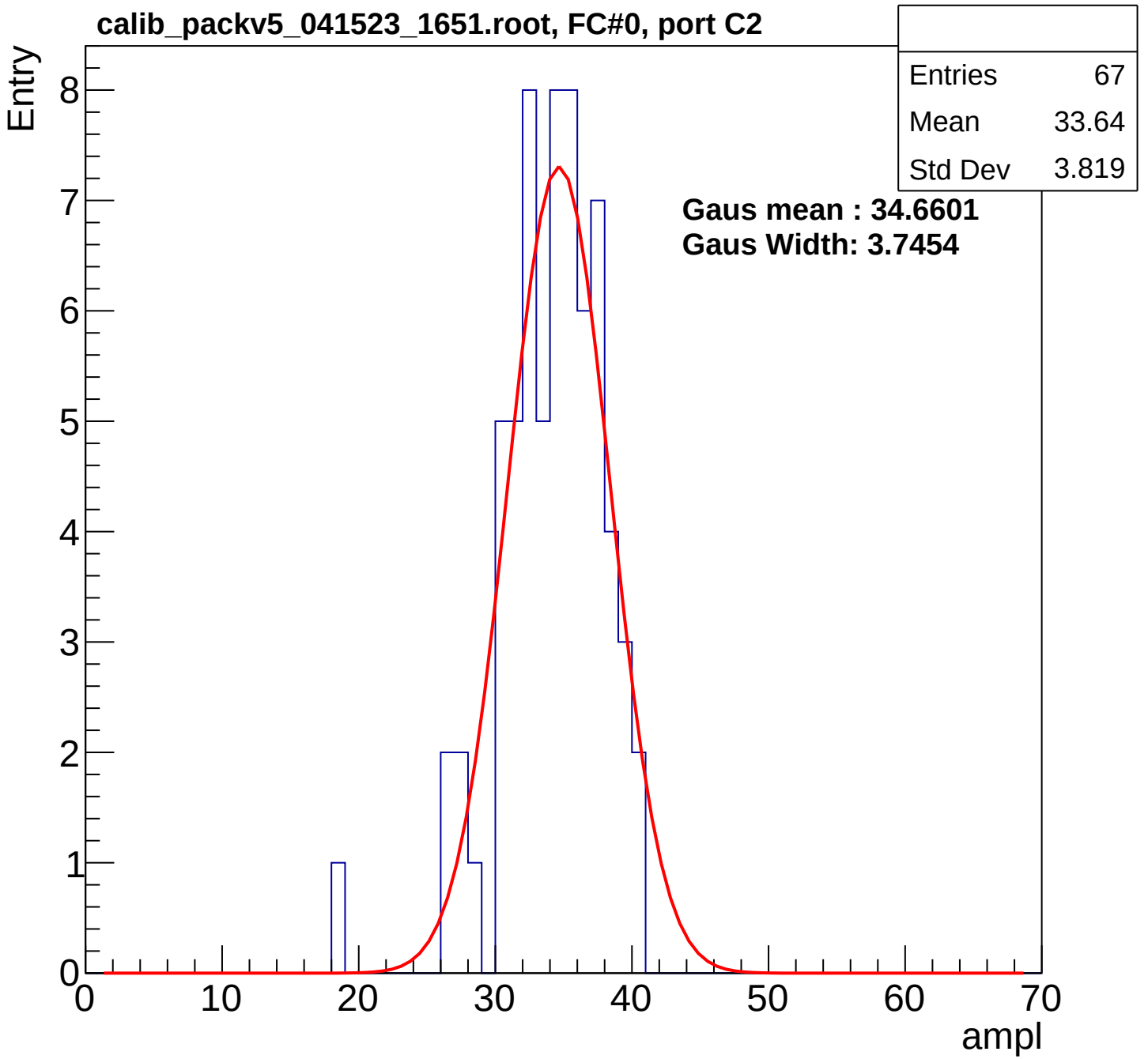
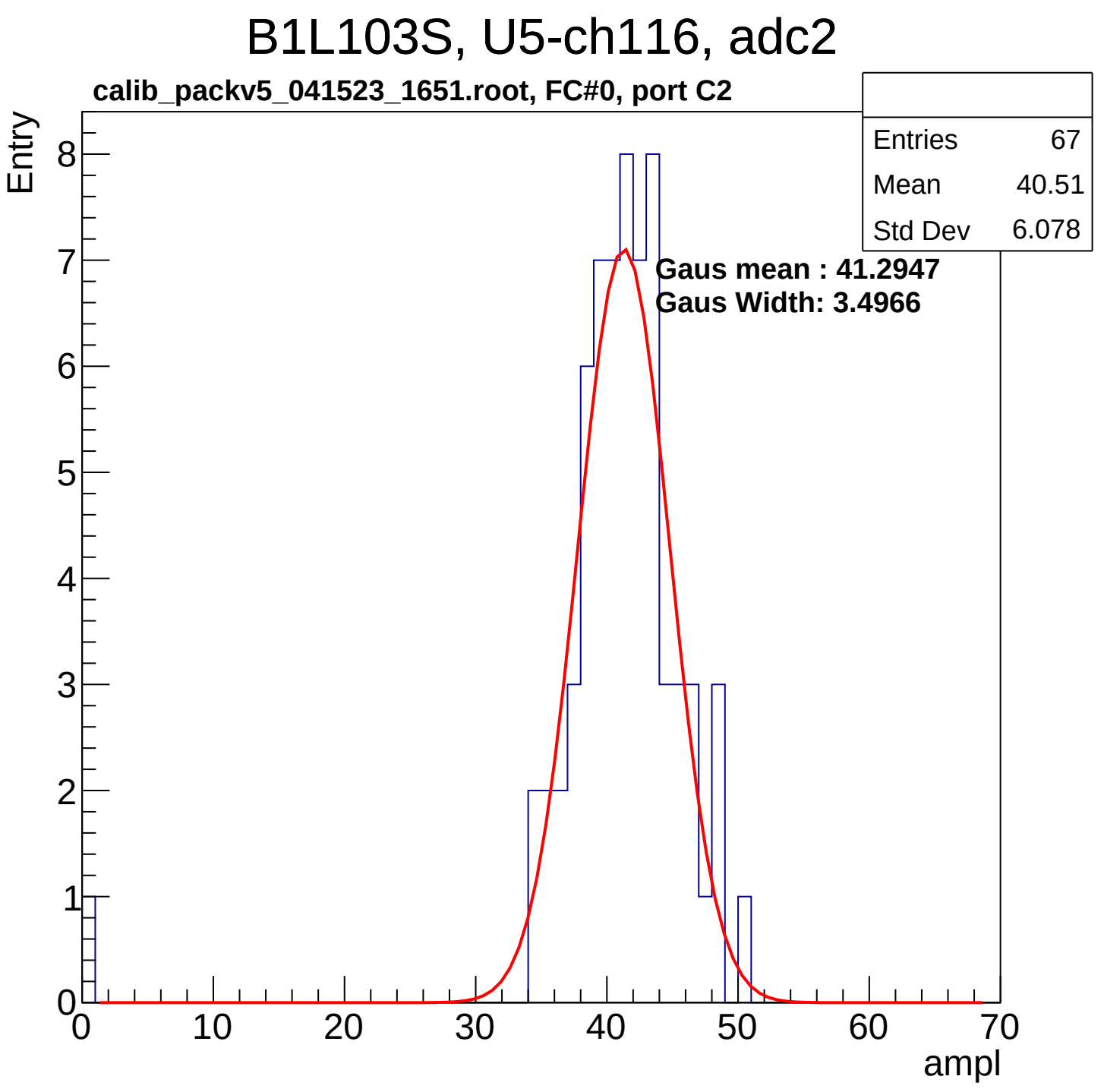
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch116, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 26.39
Std Dev 5.565
Gaus mean : 27.6858
Gaus Width: 3.8842
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U5-ch116, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 33.64
Std Dev 3.819
Gaus mean : 34.6601
Gaus Width: 3.7454
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U5-ch116, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 40.51
Std Dev 6.078
Gaus mean : 41.2947
Gaus Width: 3.4966
Entry
ampl
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2
3
4
5
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0
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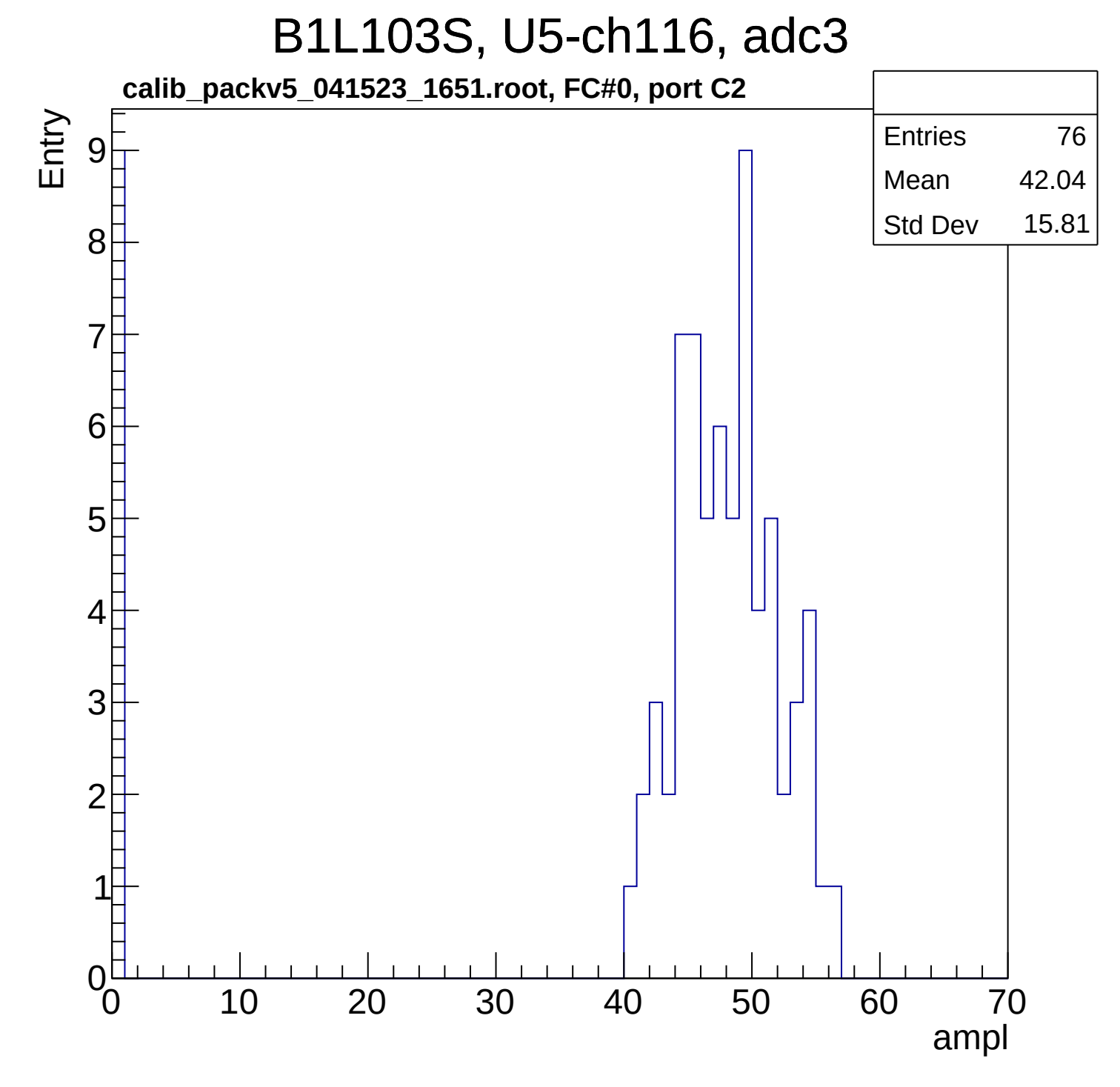
B1L103S, U5-ch116, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 42.04
Std Dev 15.81
Entry
ampl
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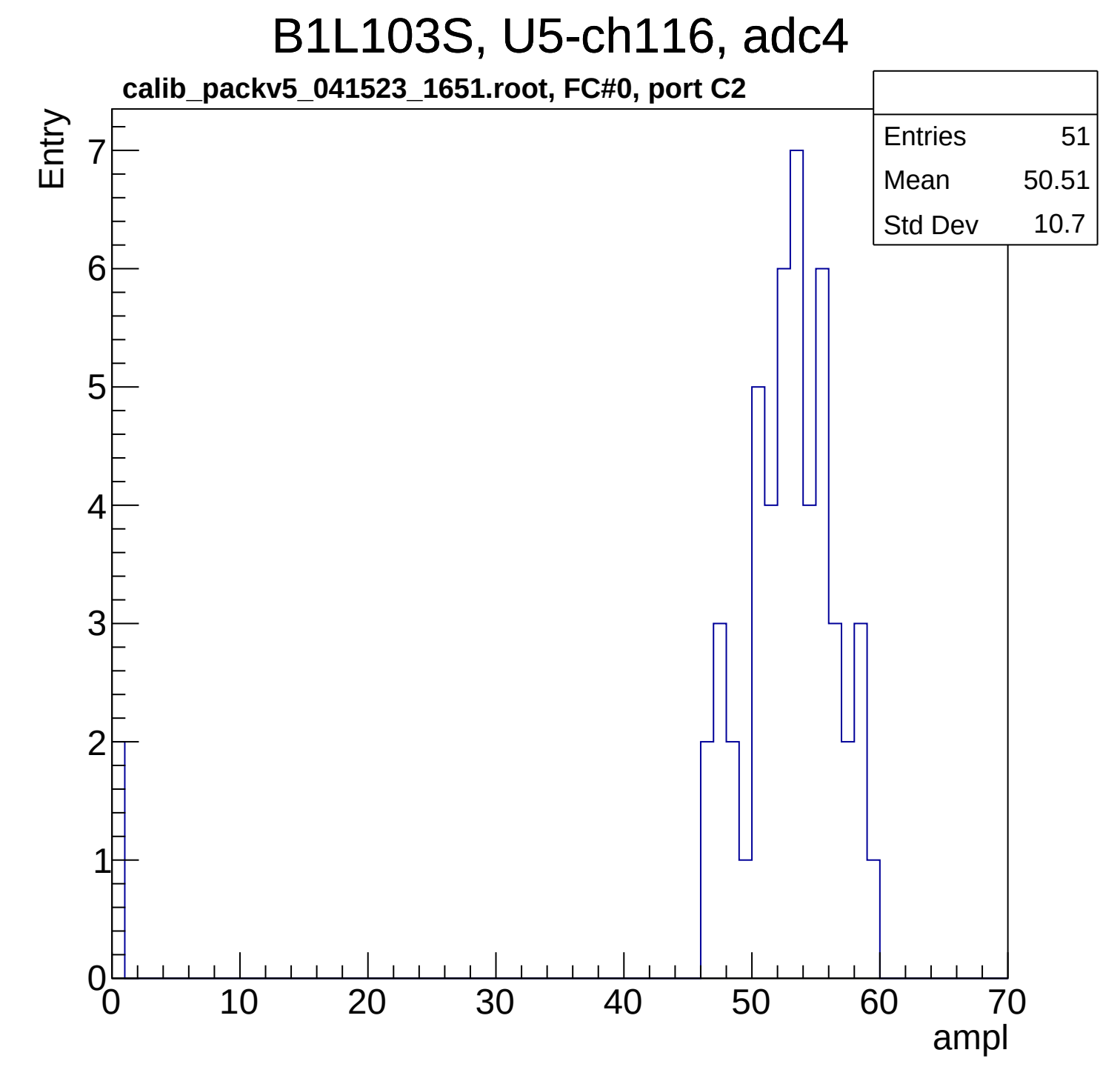
B1L103S, U5-ch116, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 50.51
Std Dev 10.7
Entry
ampl
0
1
2
3
4
5
6
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0
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60
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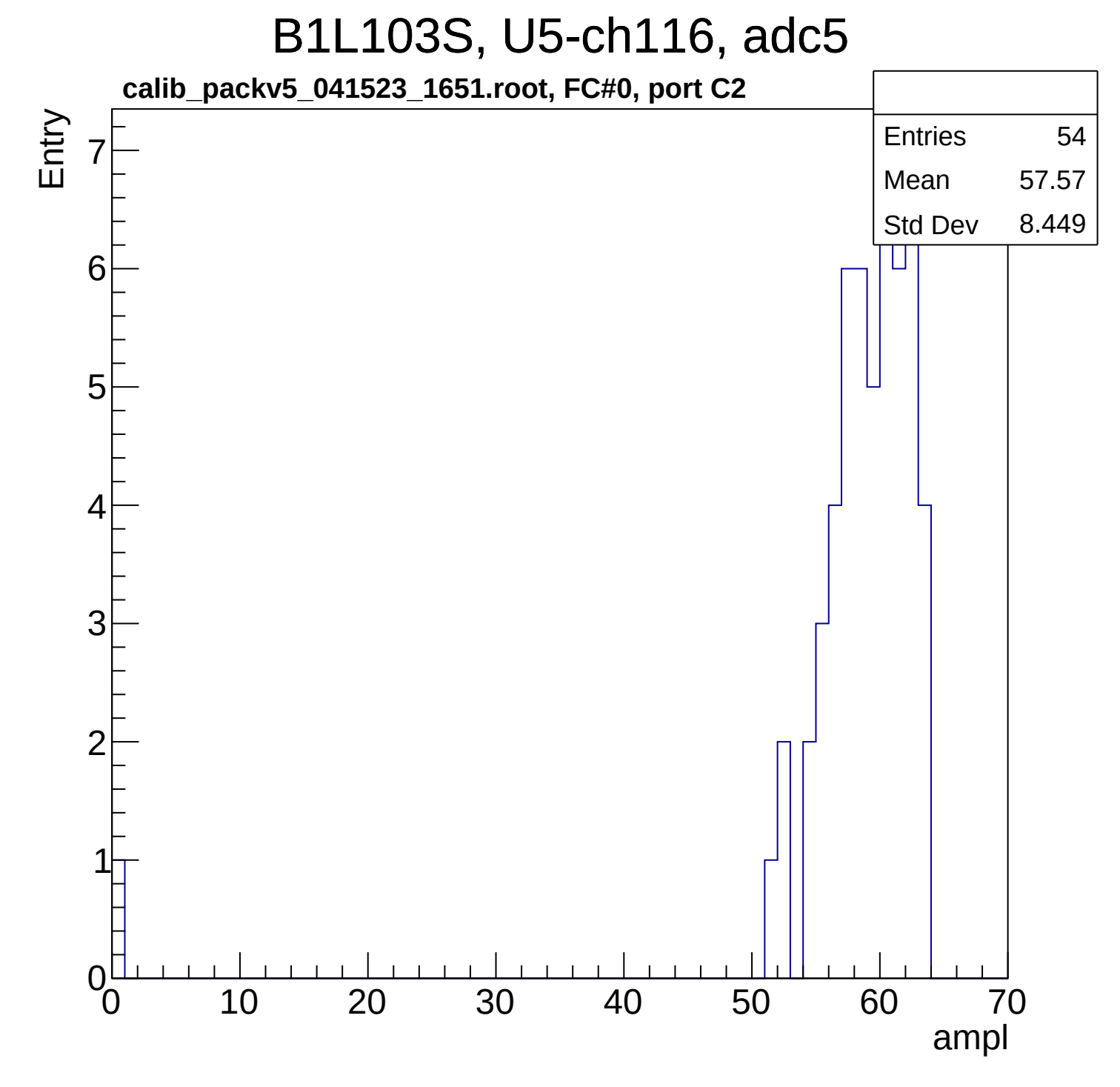
B1L103S, U5-ch116, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.57
Std Dev 8.449
Entry
ampl
0
1
2
3
4
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0
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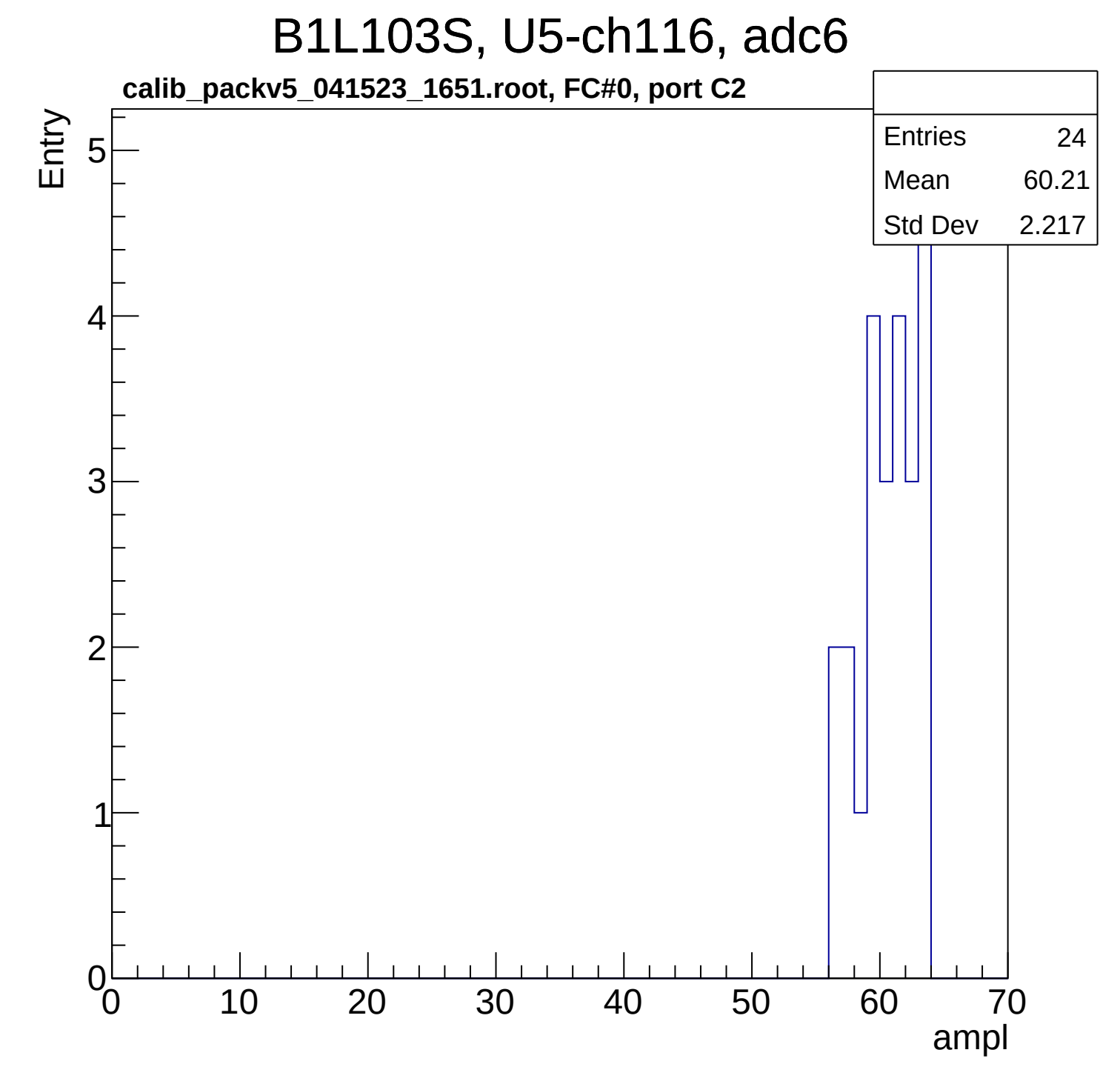
B1L103S, U5-ch116, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 60.21
Std Dev 2.217
Entry
ampl
0
1
2
3
4
5
0
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20
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40
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60
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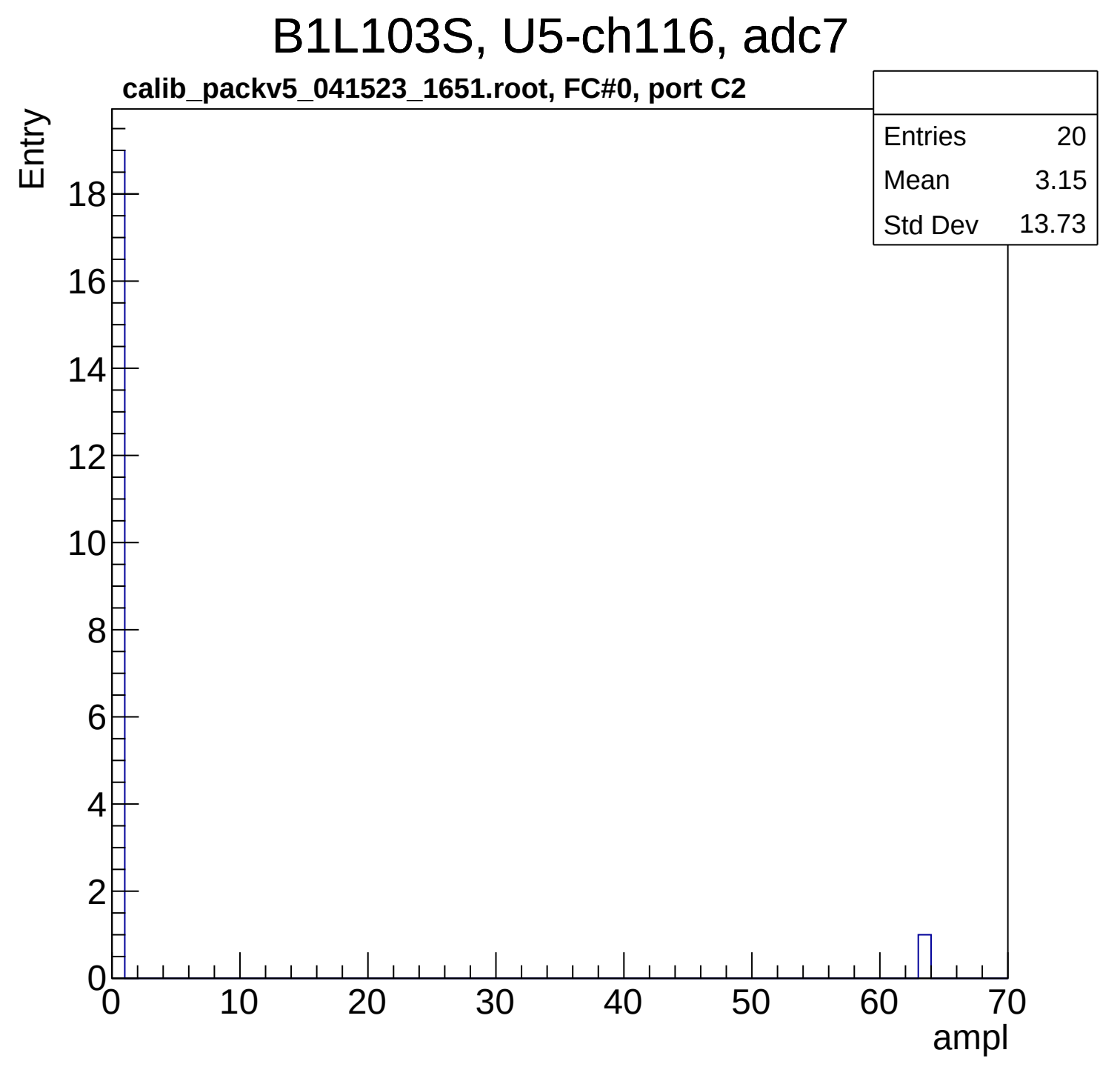
B1L103S, U5-ch116, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
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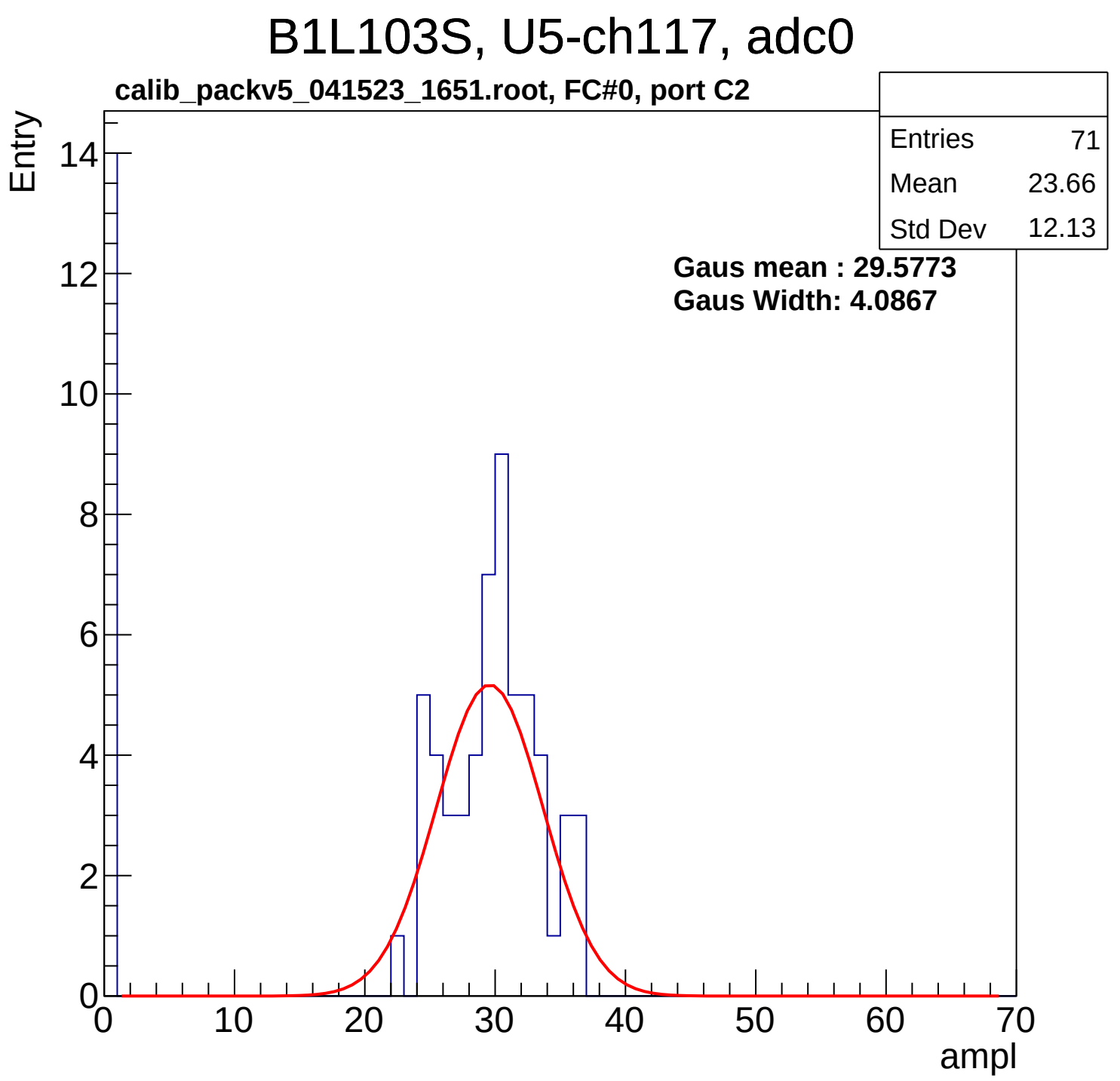
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch117, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 23.66
Std Dev 12.13
Gaus mean : 29.5773
Gaus Width: 4.0867
Entry
ampl
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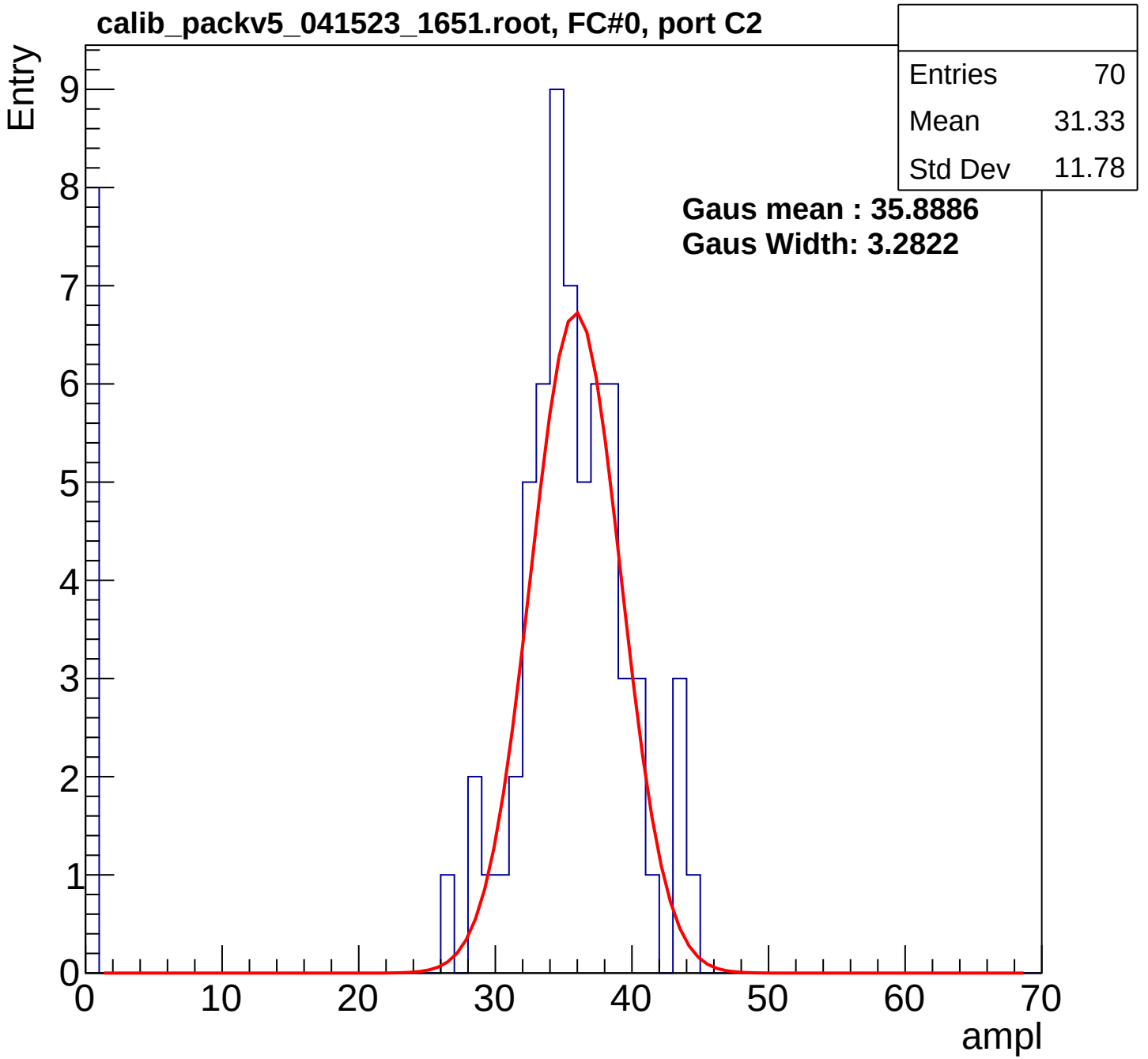
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U5-ch117, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 31.33
Std Dev 11.78
Gaus mean : 35.8886
Gaus Width: 3.2822
Entry
ampl
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3
4
5
6
7
8
9
0
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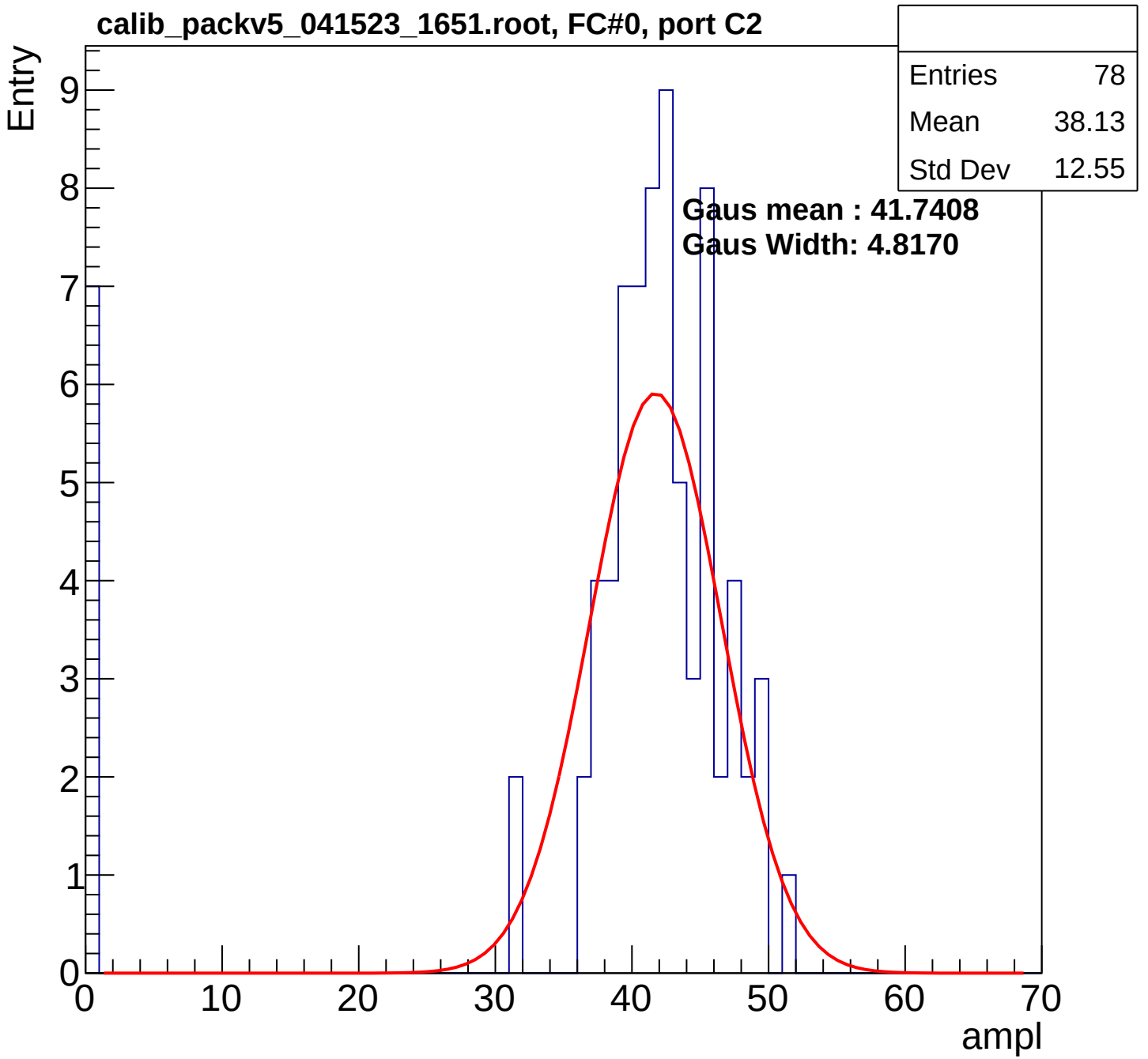
B1L103S, U5-ch117, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 38.13
Std Dev 12.55
Gaus mean : 41.7408
Gaus Width: 4.8170
Entry
ampl
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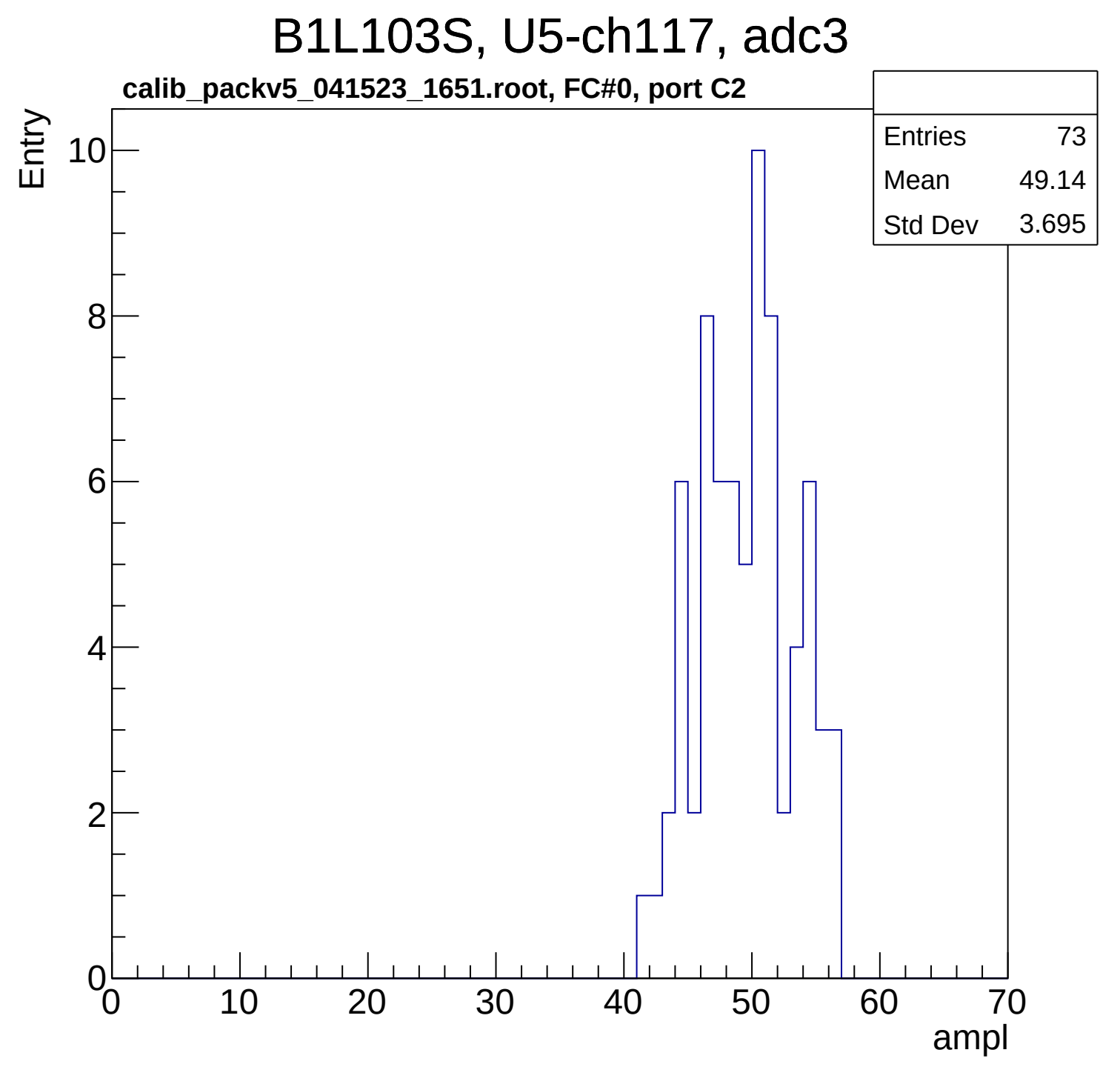
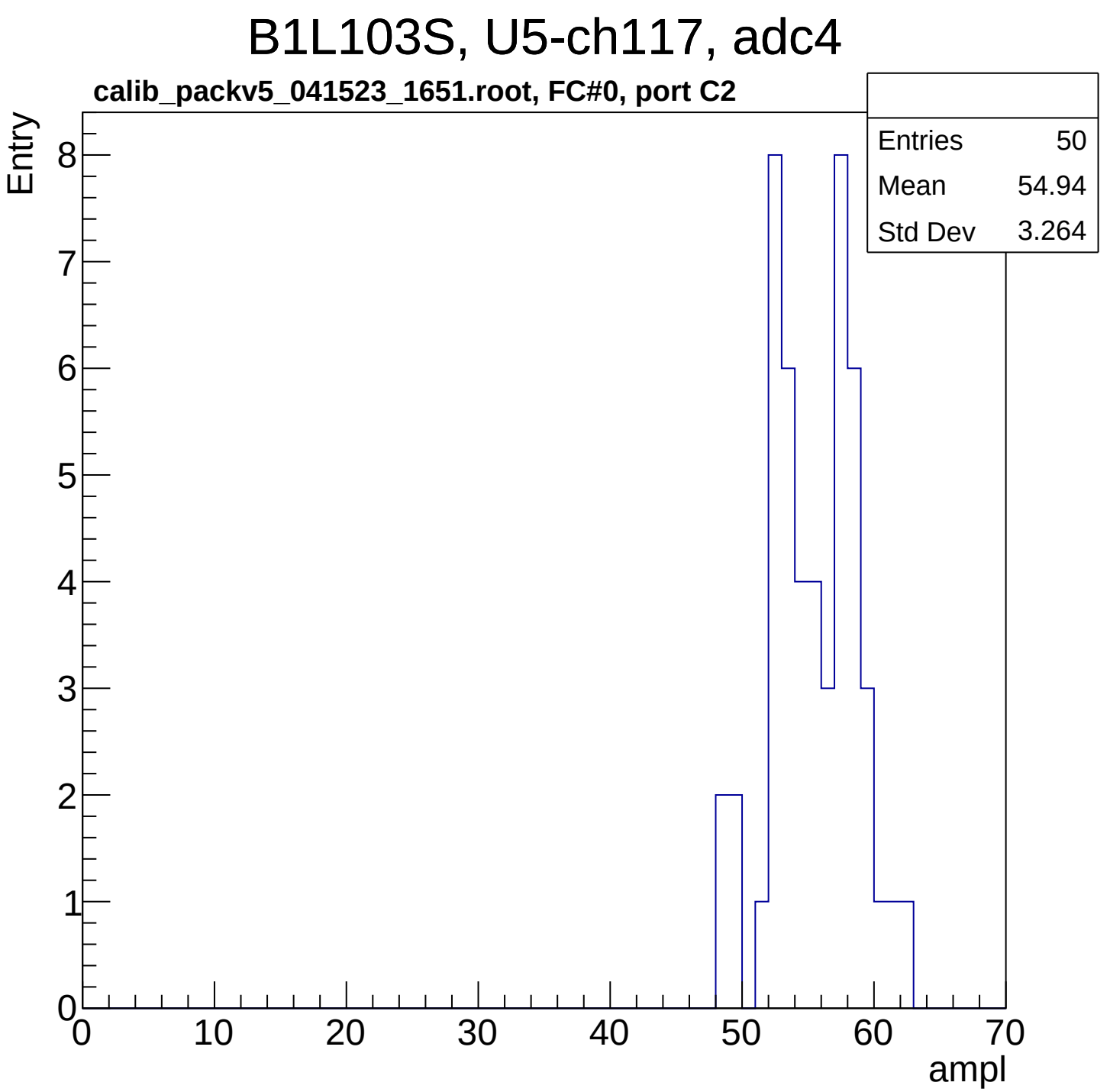
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U5-ch117, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 49.14
Std Dev 3.695
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U5-ch117, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 54.94
Std Dev 3.264
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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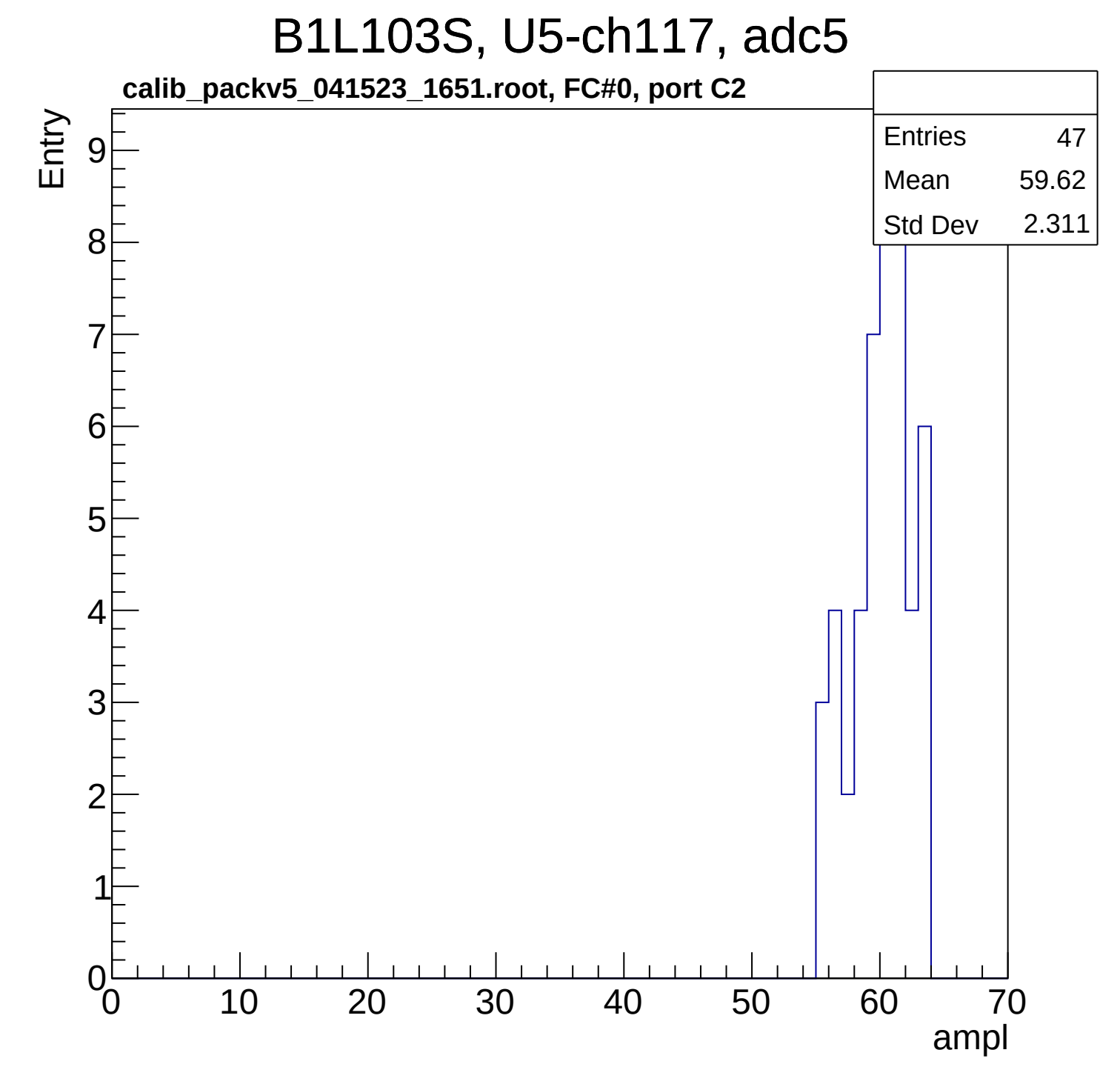
B1L103S, U5-ch117, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 59.62
Std Dev 2.311
Entry
ampl
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3
4
5
6
7
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0
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40
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60
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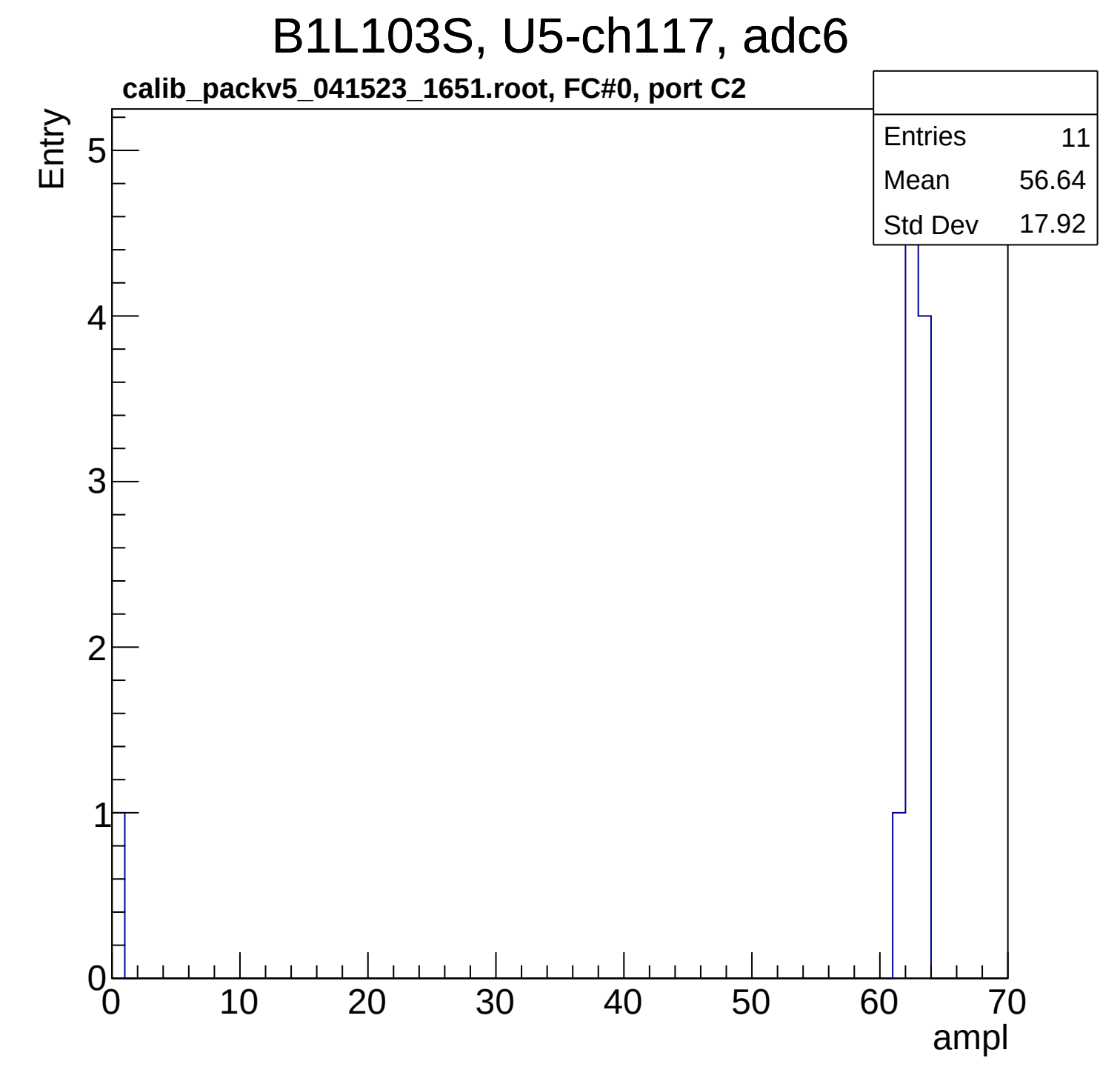
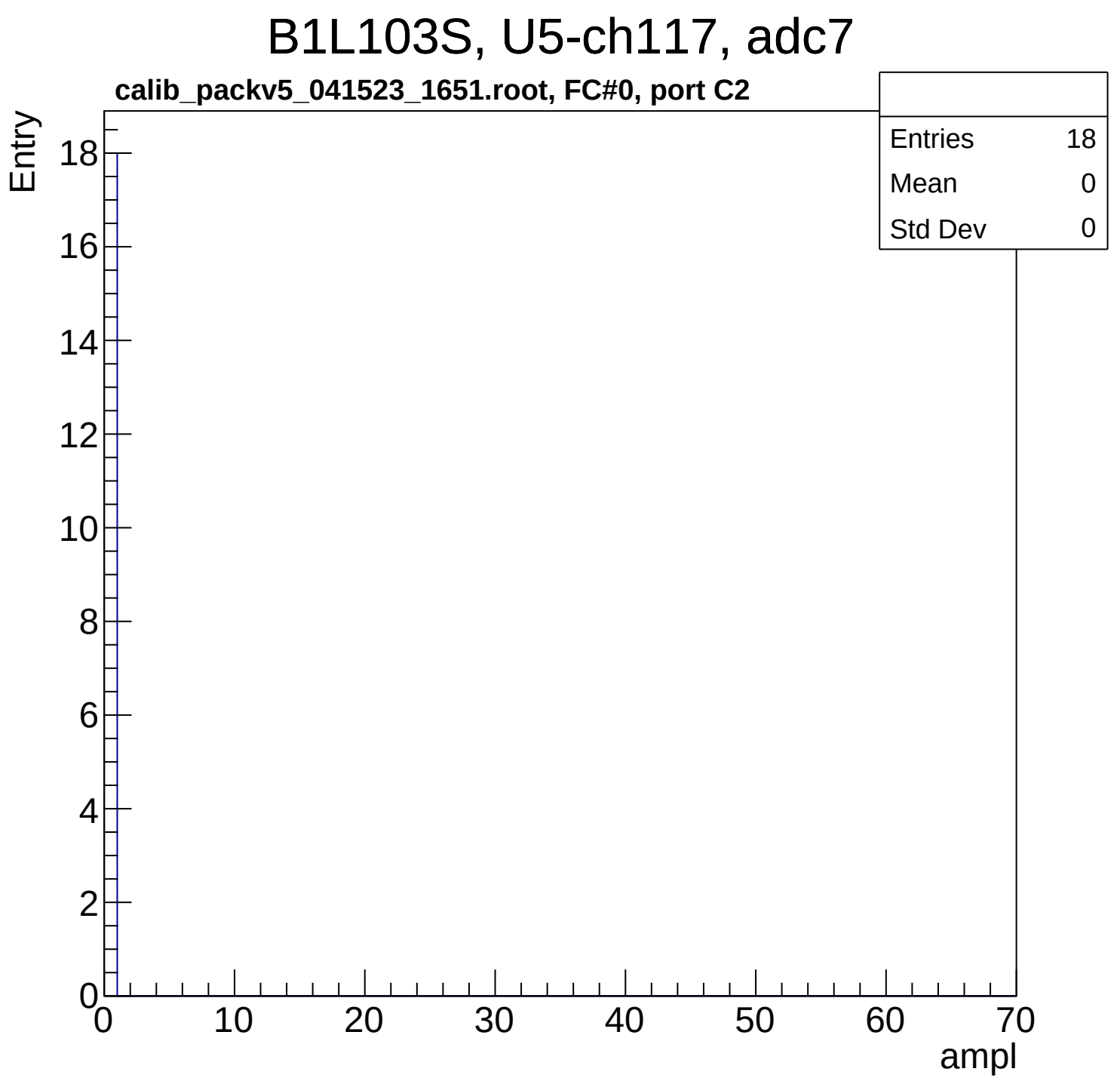

B1L103S, U5-ch117, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 56.64
Std Dev 17.92
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch117, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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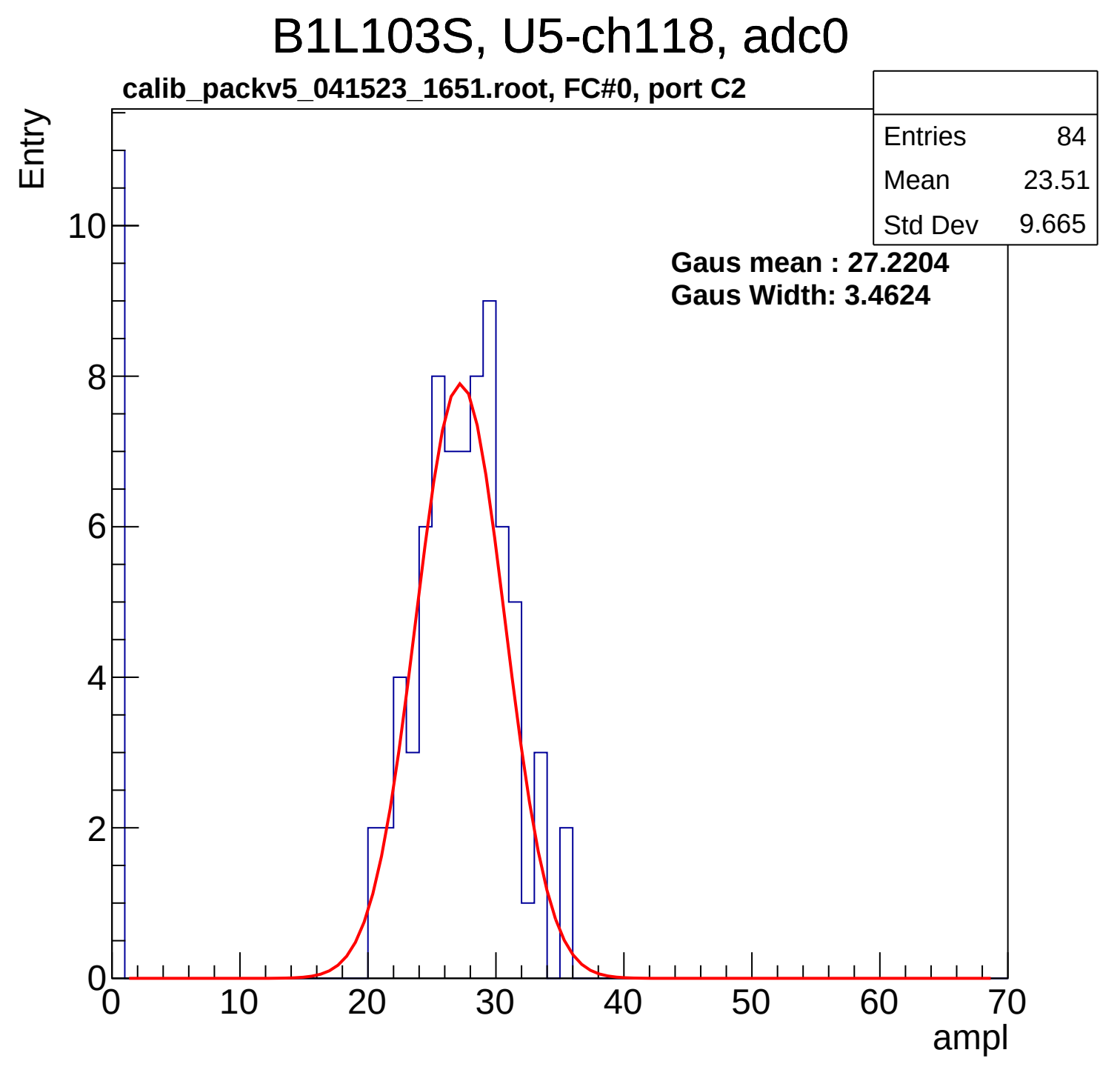
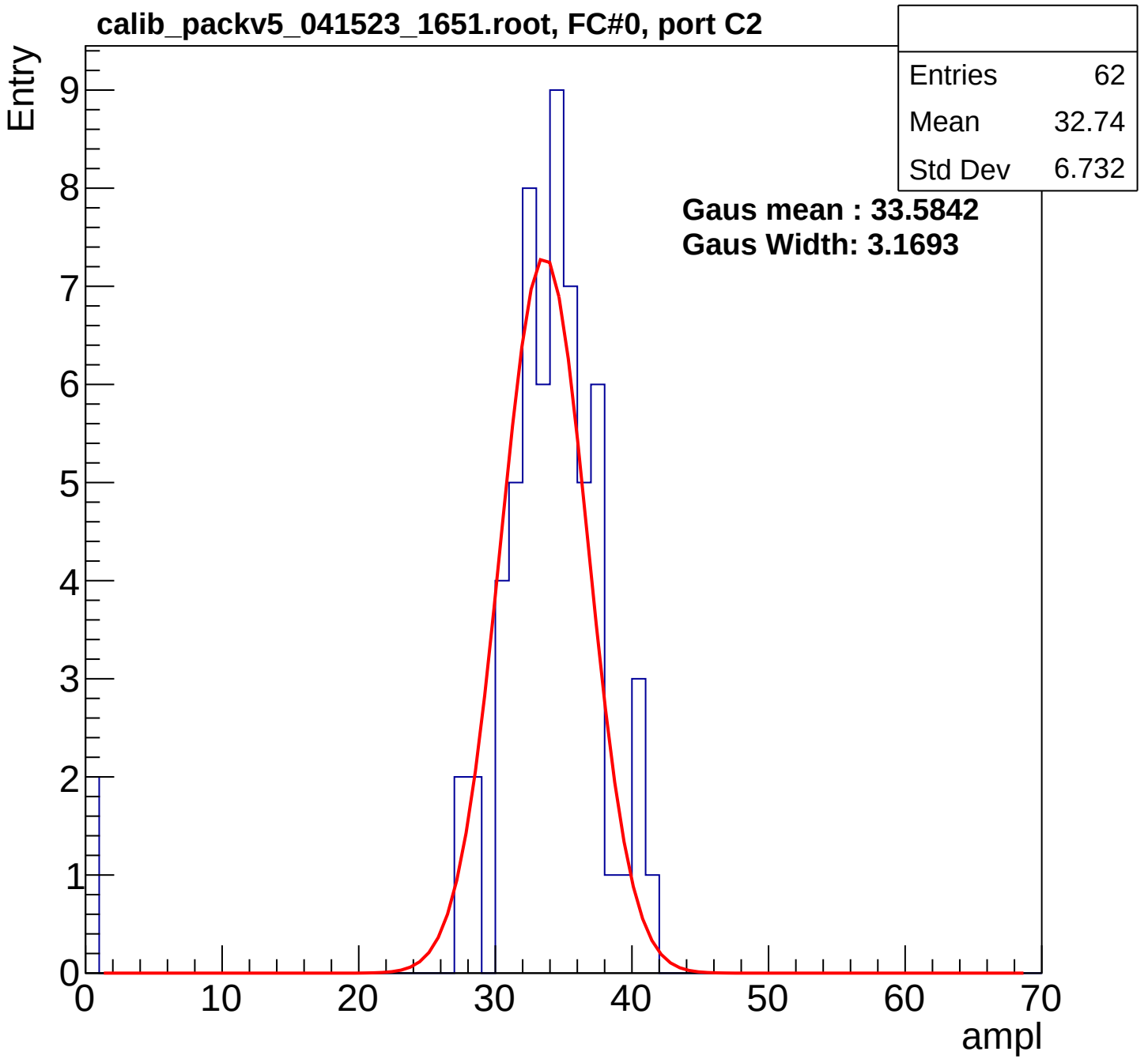
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch118, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 23.51
Std Dev 9.665
Gaus mean : 27.2204
Gaus Width: 3.4624
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U5-ch118, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 32.74
Std Dev 6.732
Gaus mean : 33.5842
Gaus Width: 3.1693
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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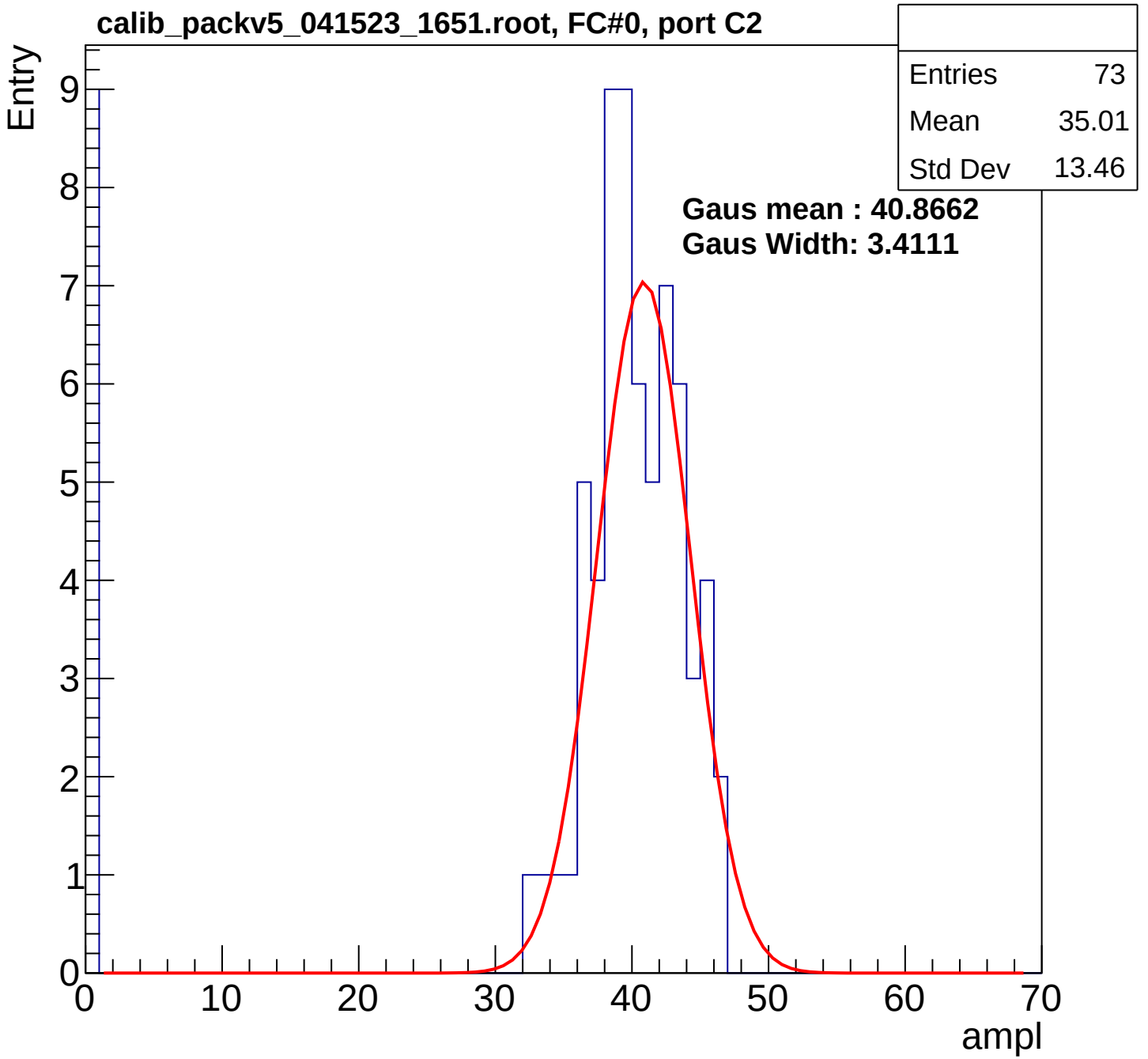
B1L103S, U5-ch118, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 35.01
Std Dev 13.46
Gaus mean : 40.8662
Gaus Width: 3.4111
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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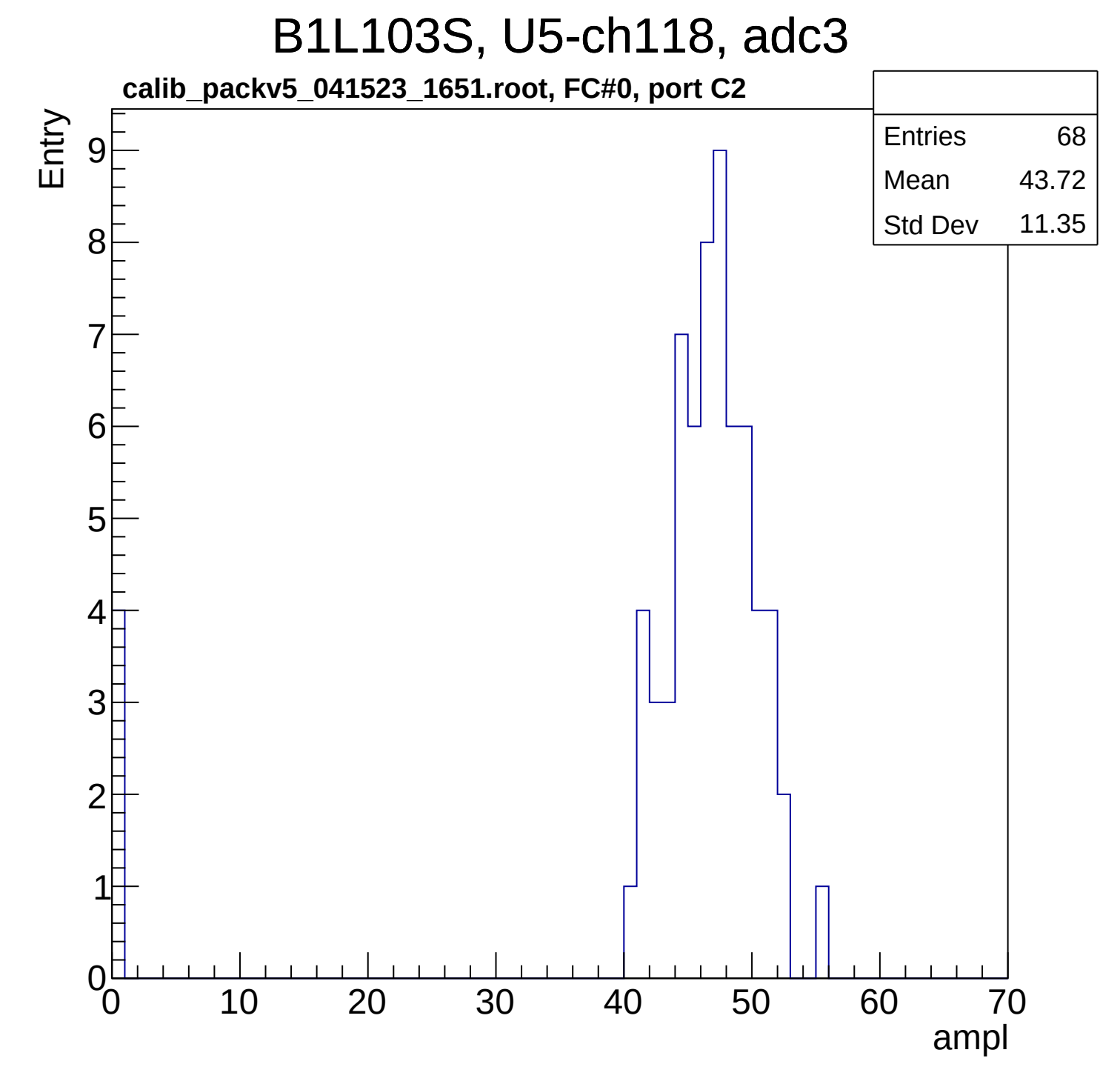
B1L103S, U5-ch118, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 43.72
Std Dev 11.35
Entry
ampl
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3
4
5
6
7
8
9
0
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20
30
40
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60
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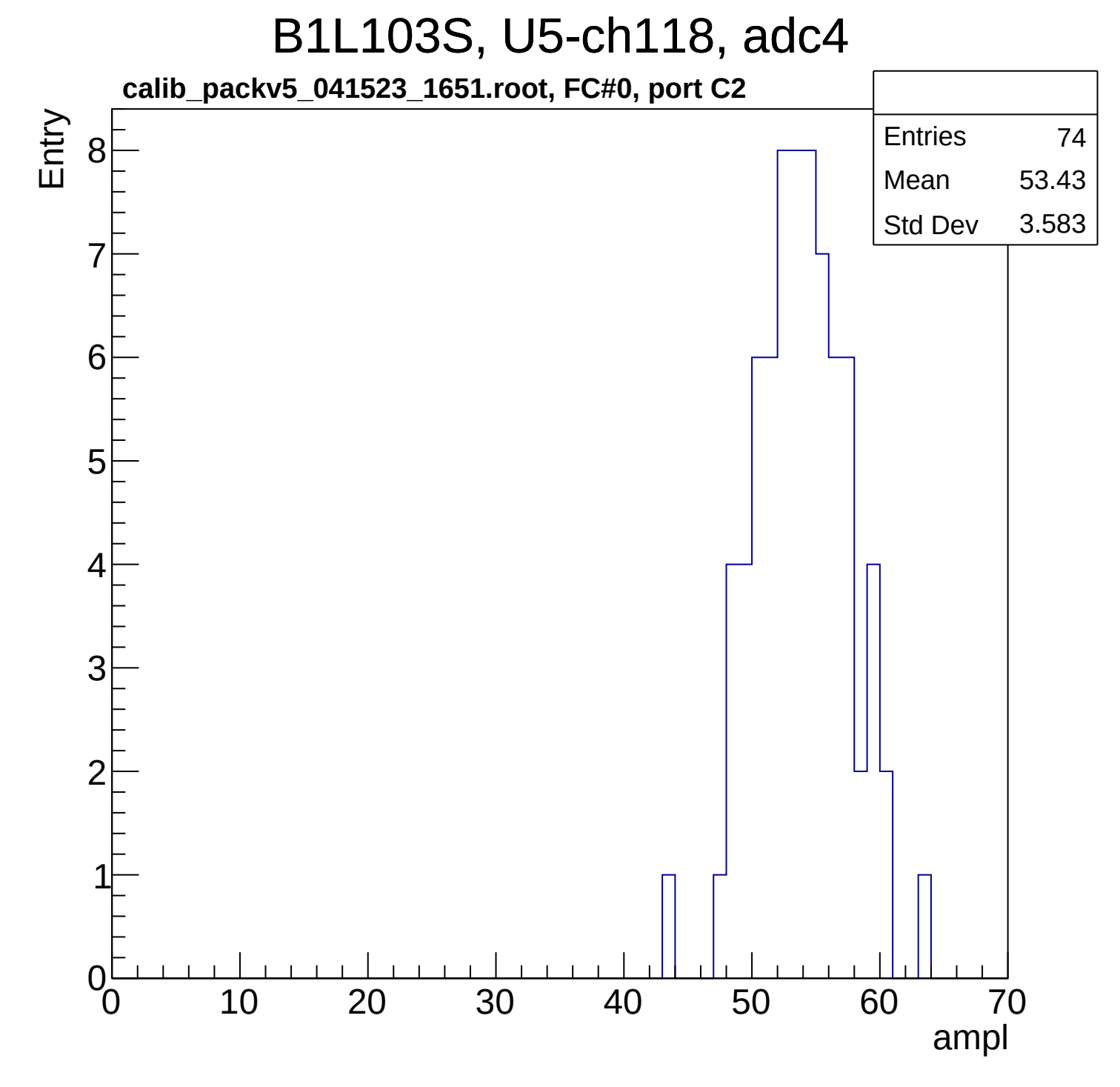
B1L103S, U5-ch118, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 53.43
Std Dev 3.583
Entry
ampl
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2
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4
5
6
7
8
0
10
20
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40
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60
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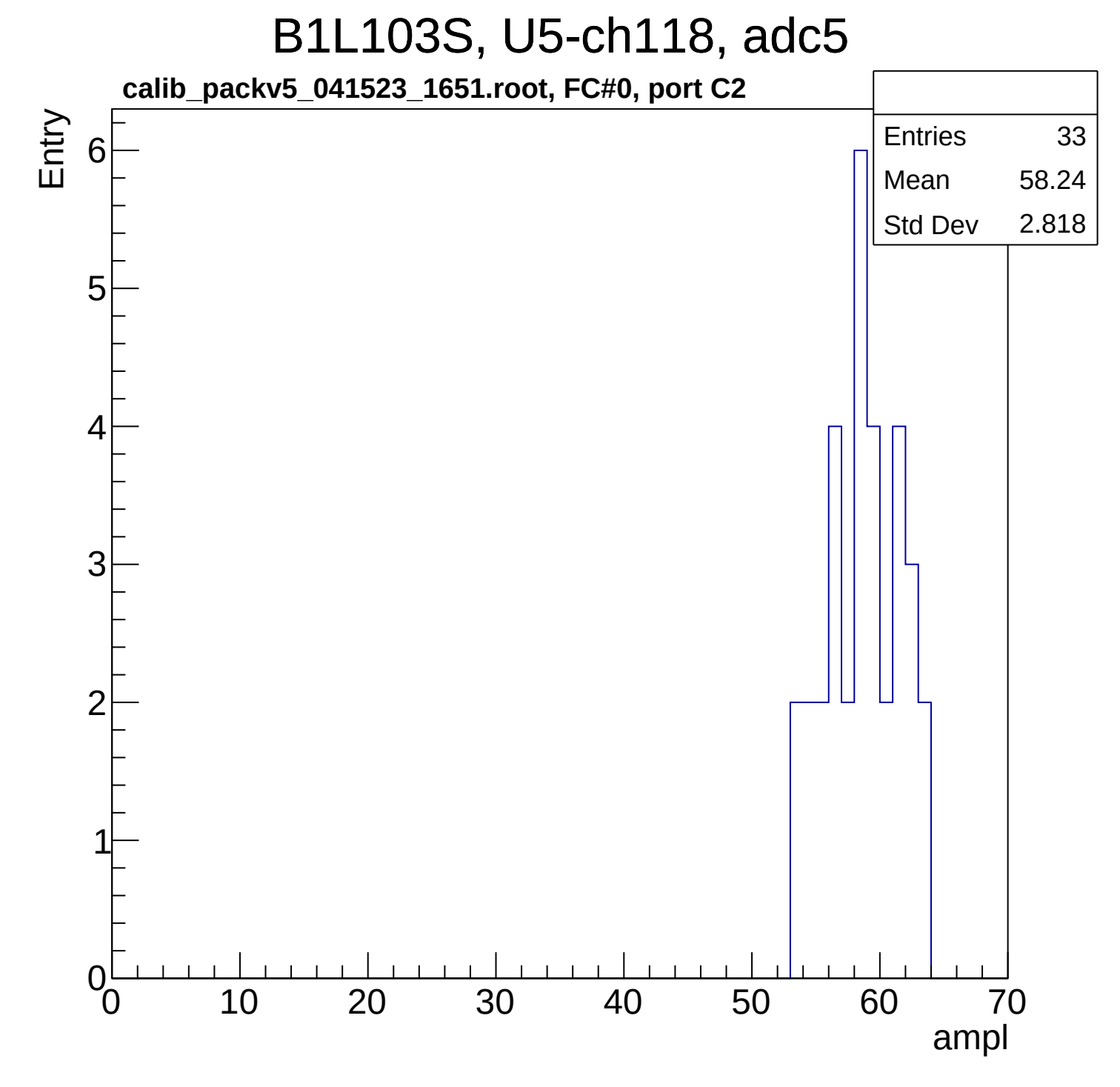
B1L103S, U5-ch118, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 58.24
Std Dev 2.818
Entry
ampl
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1
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3
4
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0
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40
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60
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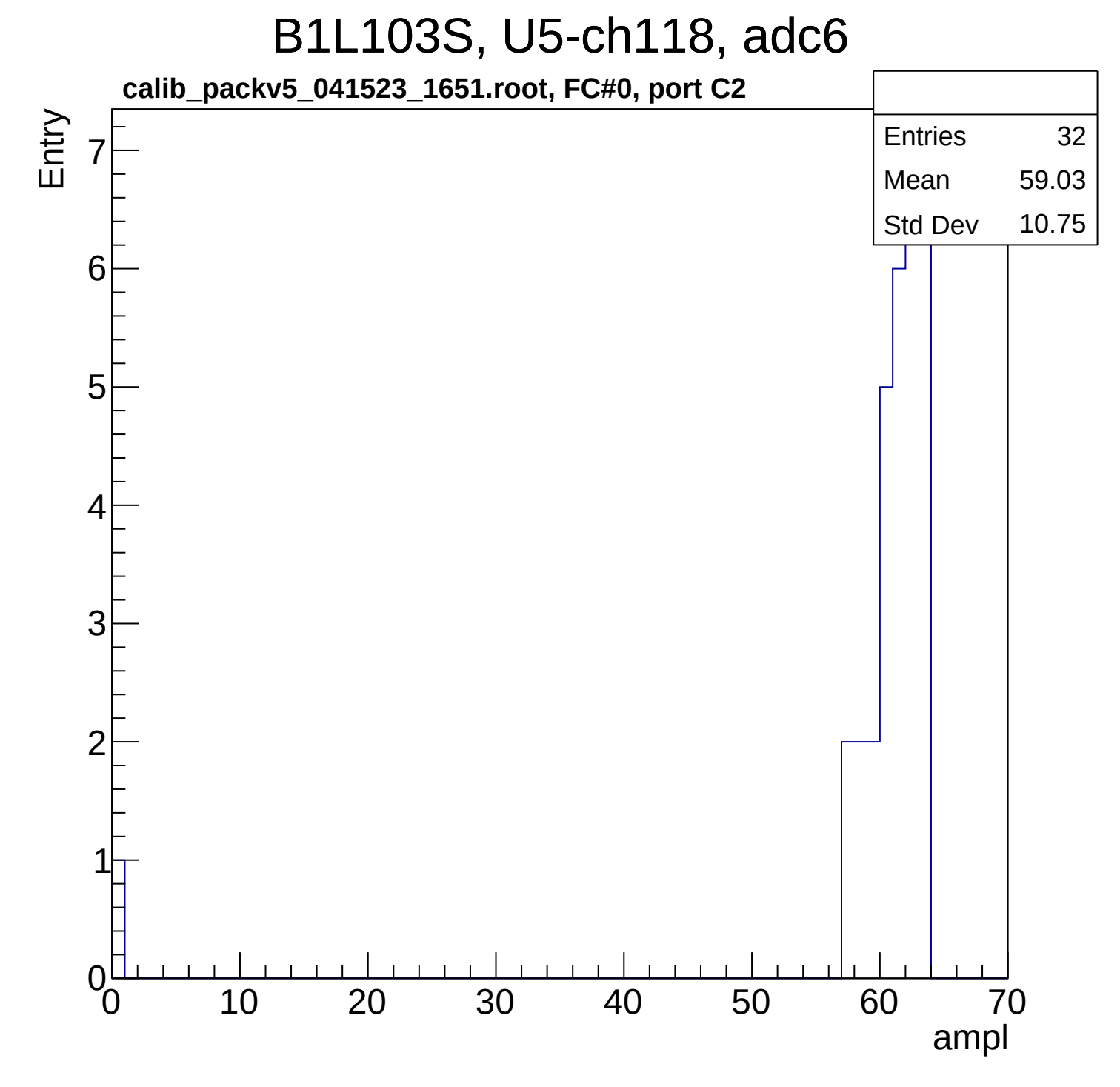
B1L103S, U5-ch118, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 59.03
Std Dev 10.75
Entry
ampl
0
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2
3
4
5
6
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0
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40
50
60
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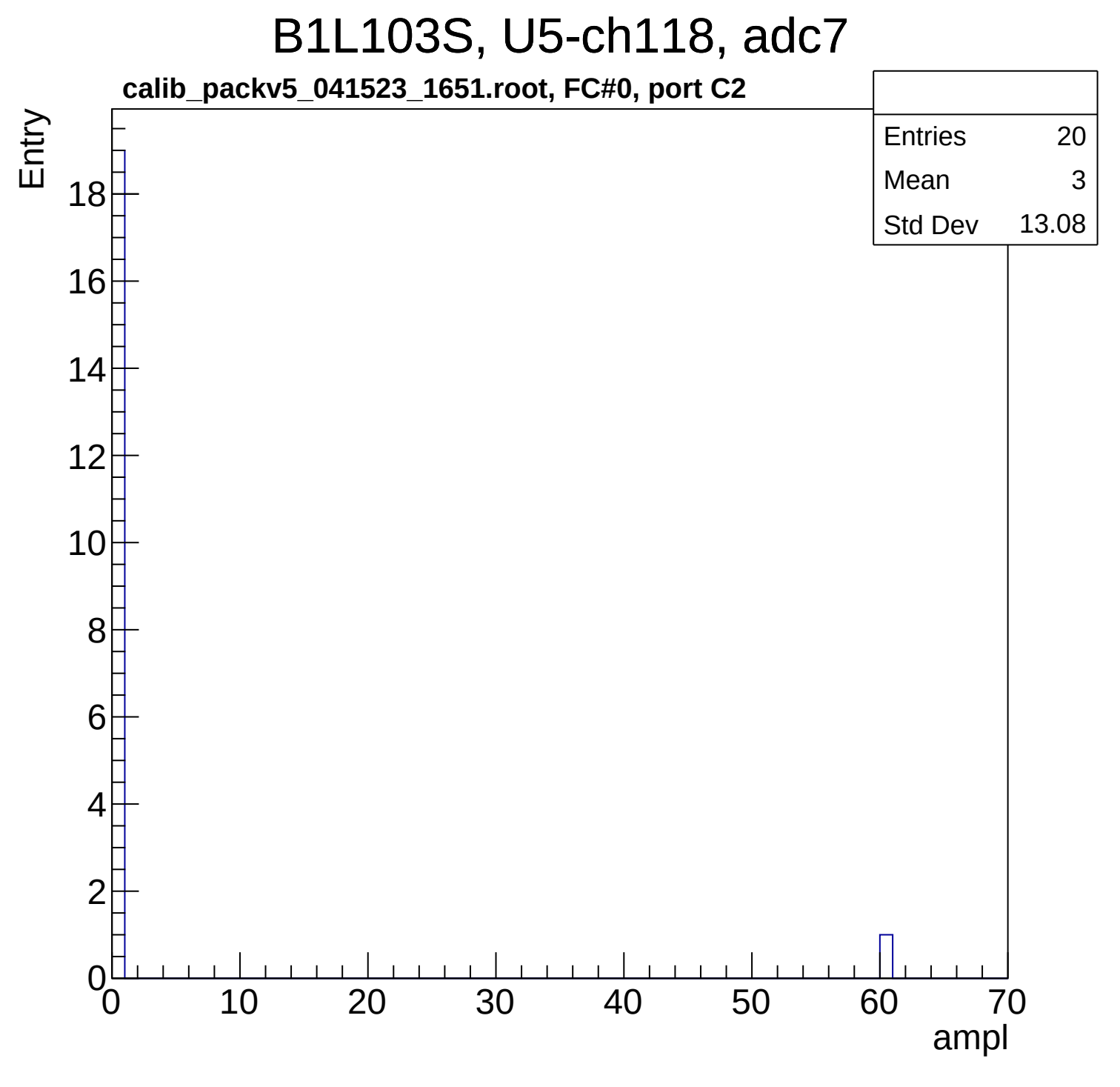
B1L103S, U5-ch118, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3
Std Dev 13.08
Entry
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10
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14
16
18
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10
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30
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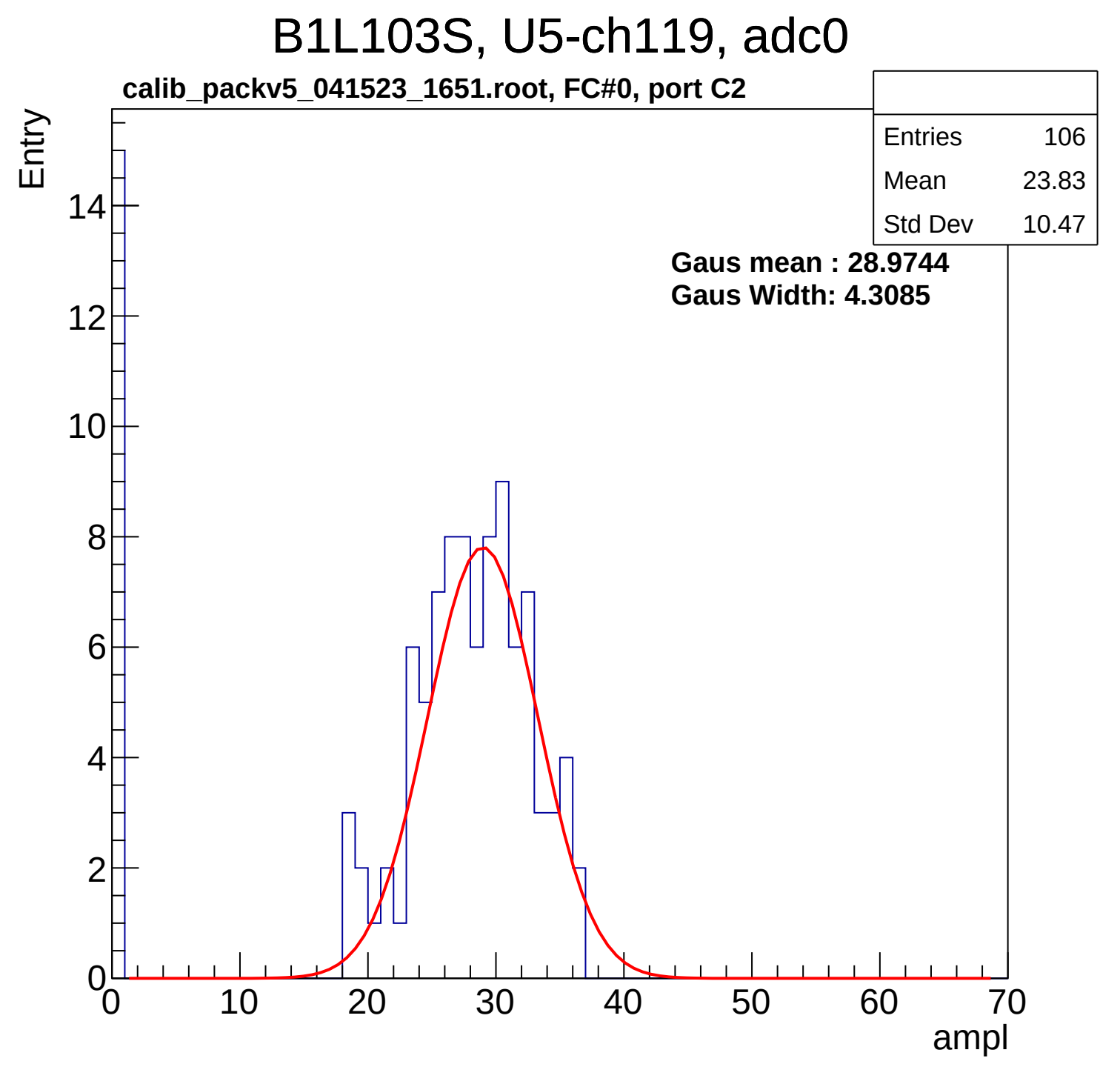
50
60
70
ampl


B1L103S, U5-ch119, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 106
Mean 23.83
Std Dev 10.47
Gaus mean : 28.9744
Gaus Width: 4.3085
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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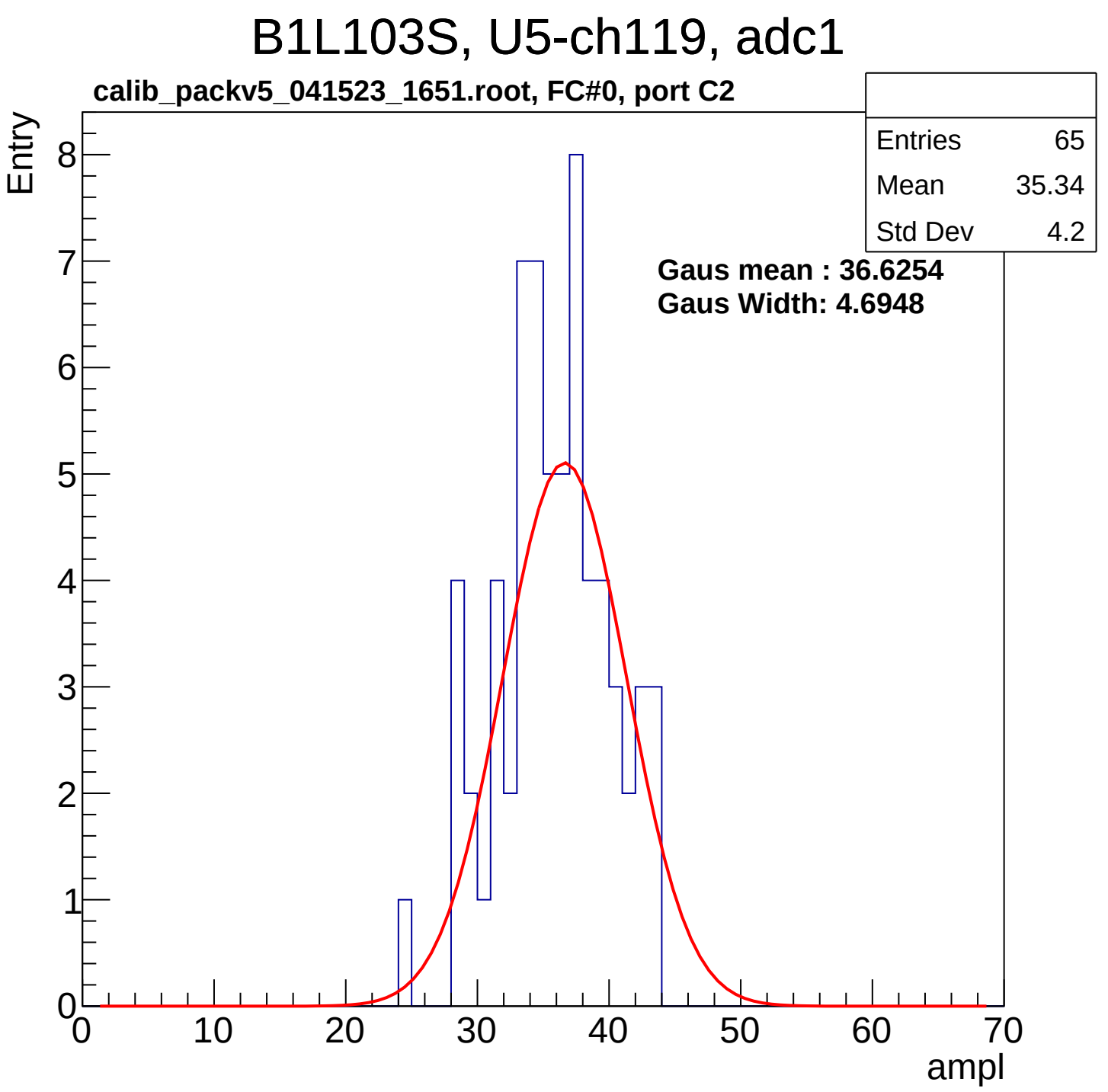
B1L103S, U5-ch119, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 35.34
Std Dev 4.2
Gaus mean : 36.6254
Gaus Width: 4.6948
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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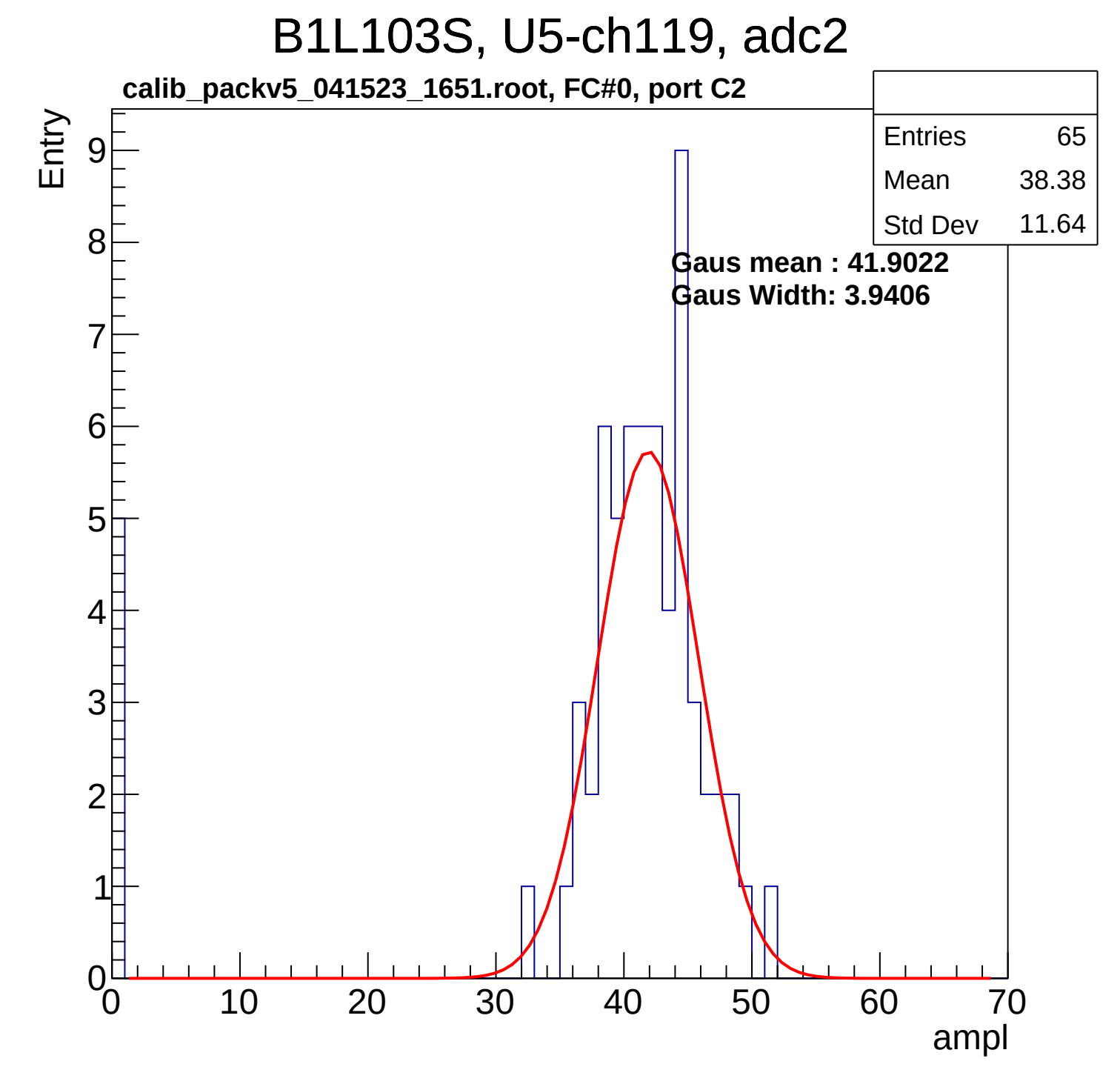
B1L103S, U5-ch119, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 38.38
Std Dev 11.64
Gaus mean : 41.9022
Gaus Width: 3.9406
Entry
ampl
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10
20
30
40
50
60
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1
2
3
4
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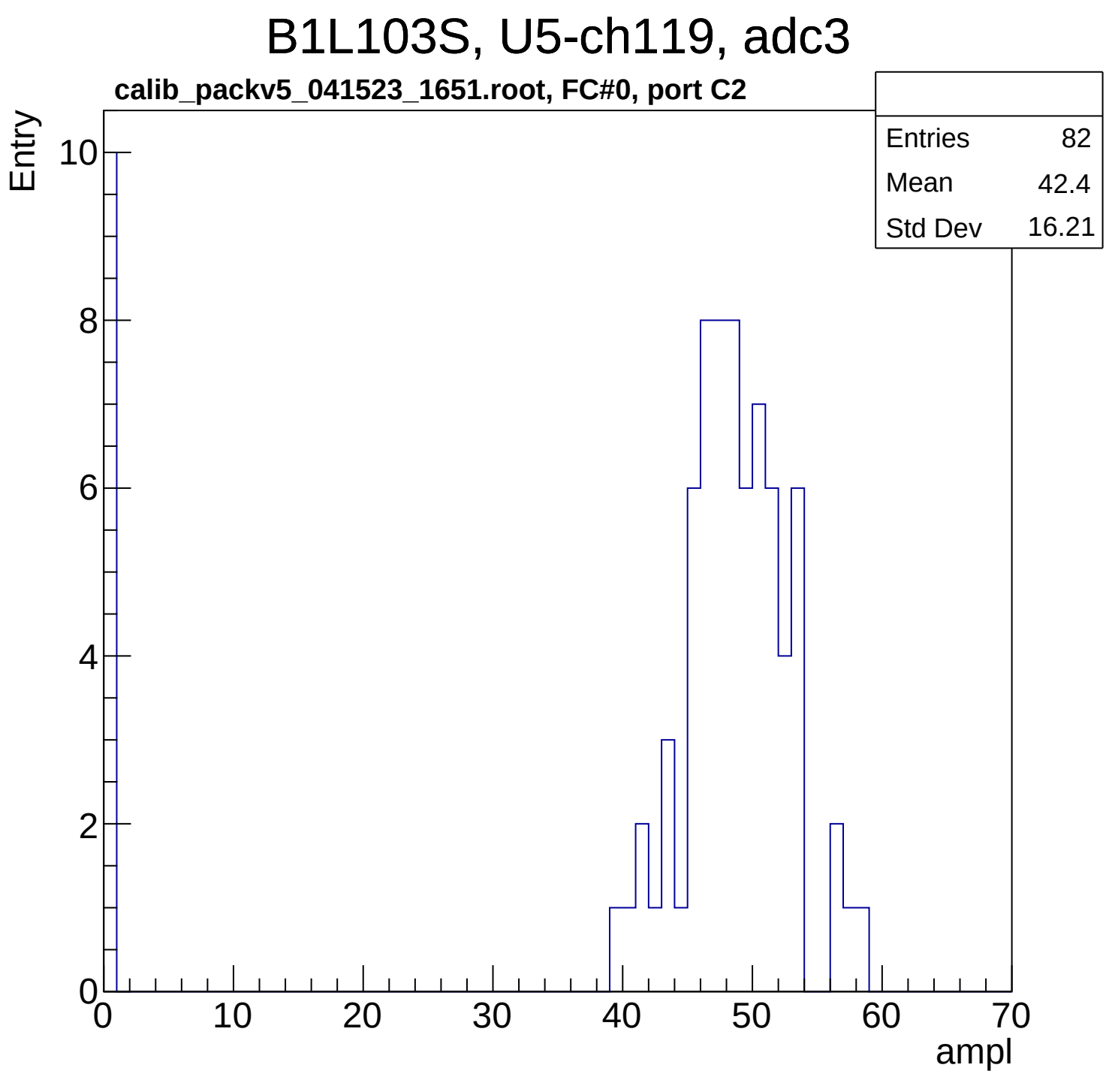
6
7
8
9


B1L103S, U5-ch119, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 42.4
Std Dev 16.21
Entry
ampl
0
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4
6
8
10
0
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20
30
40
50
60
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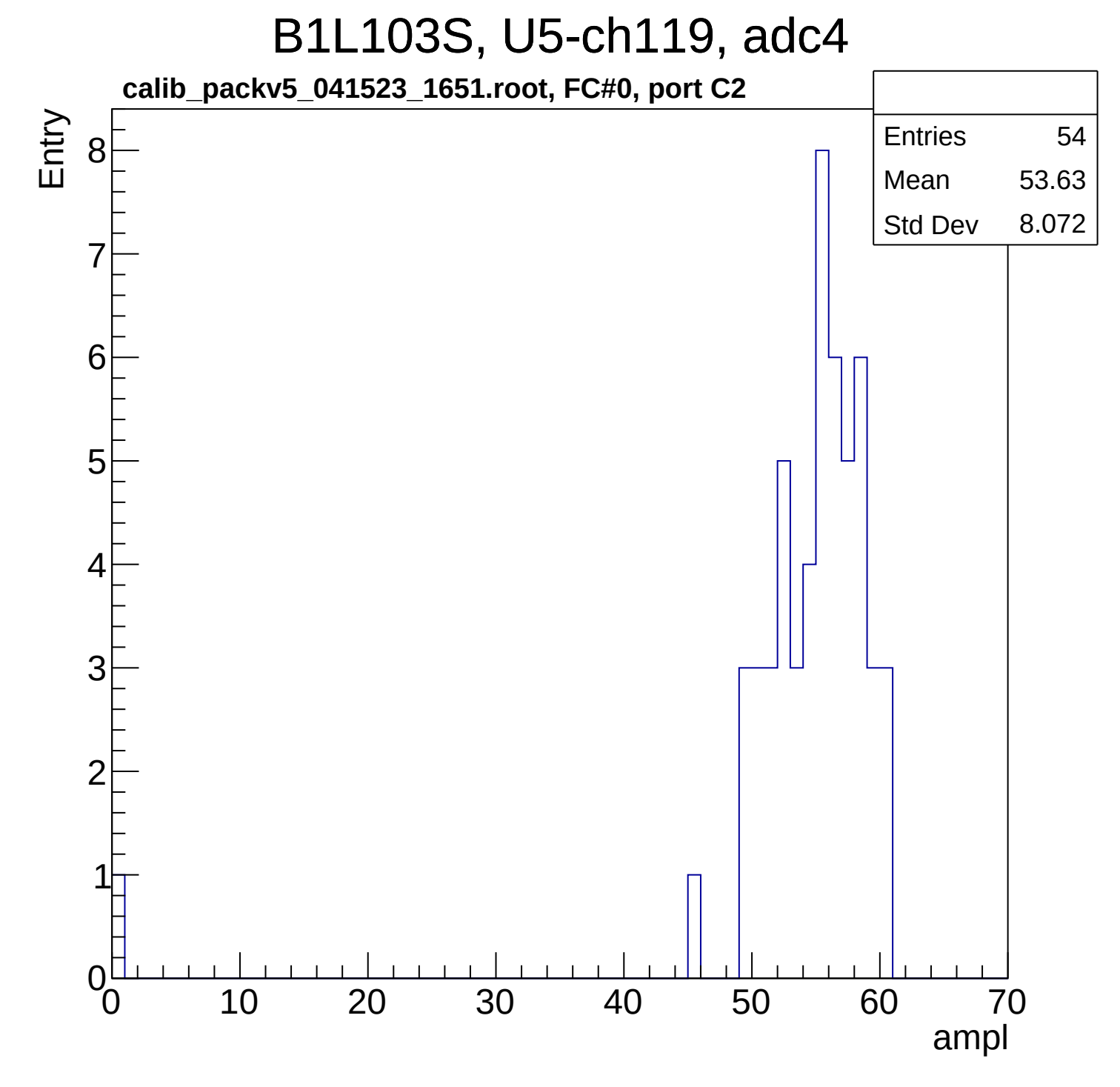
B1L103S, U5-ch119, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 53.63
Std Dev 8.072
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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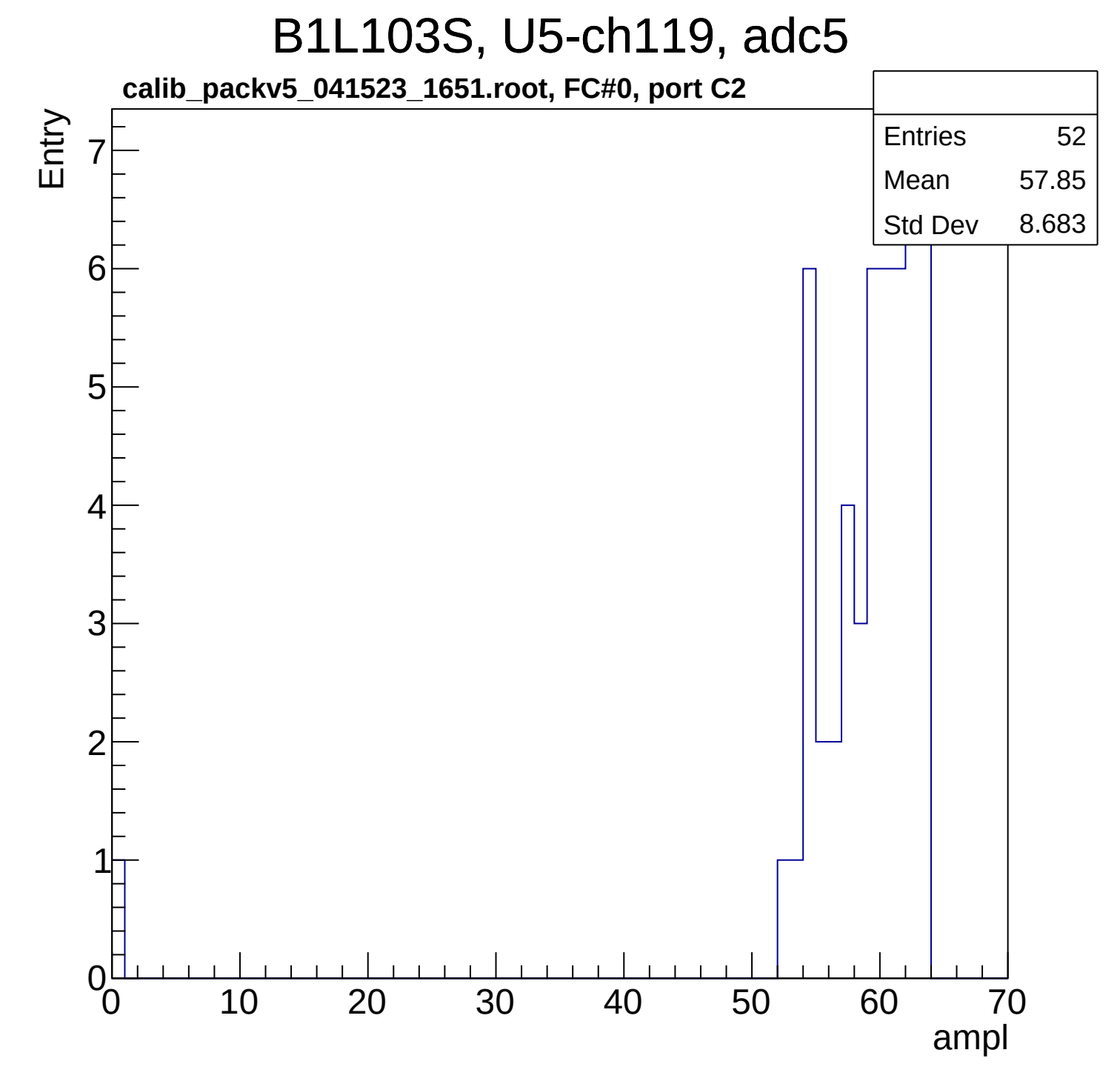
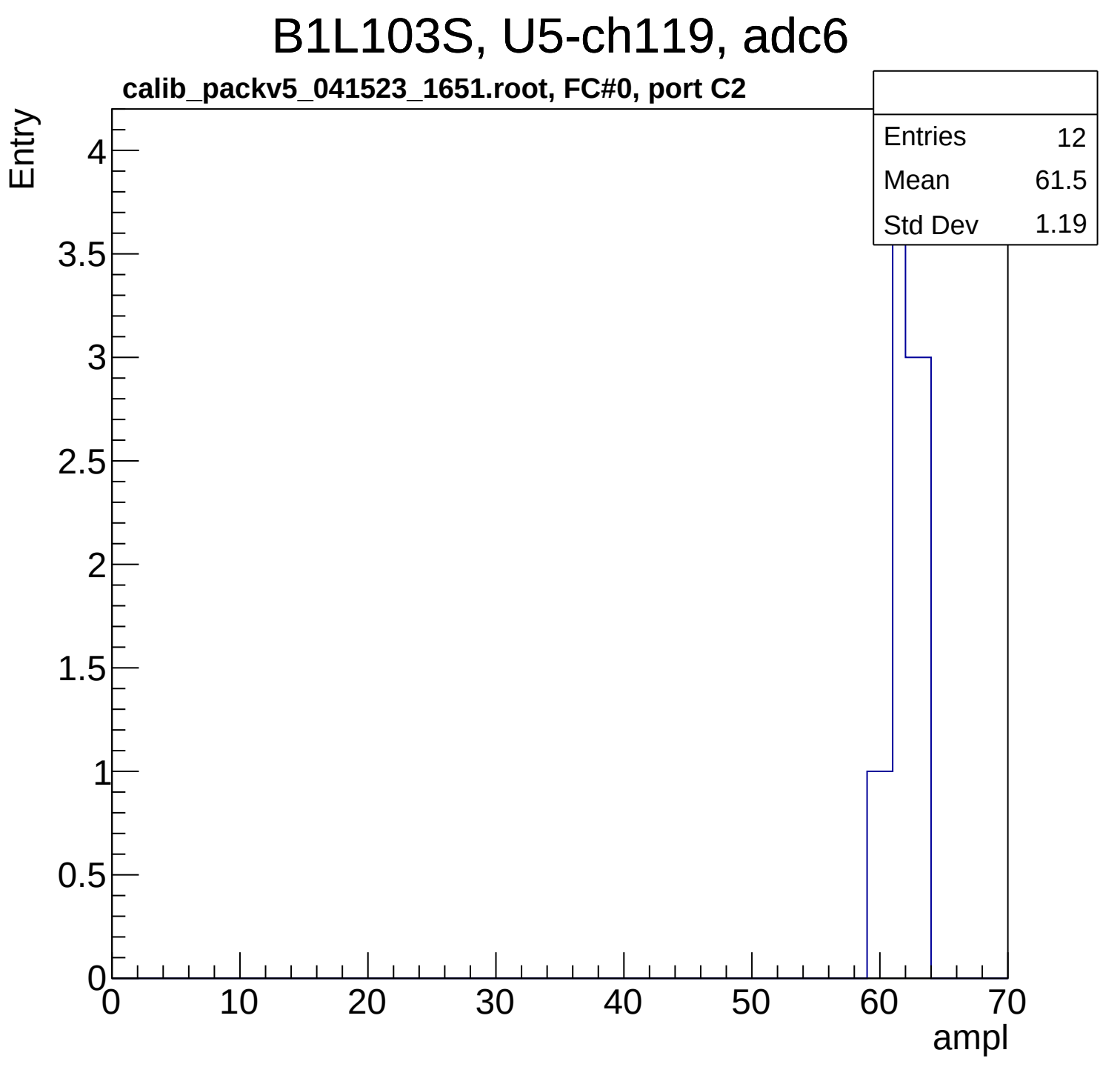

B1L103S, U5-ch119, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 57.85
Std Dev 8.683
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U5-ch119, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.5
Std Dev 1.19
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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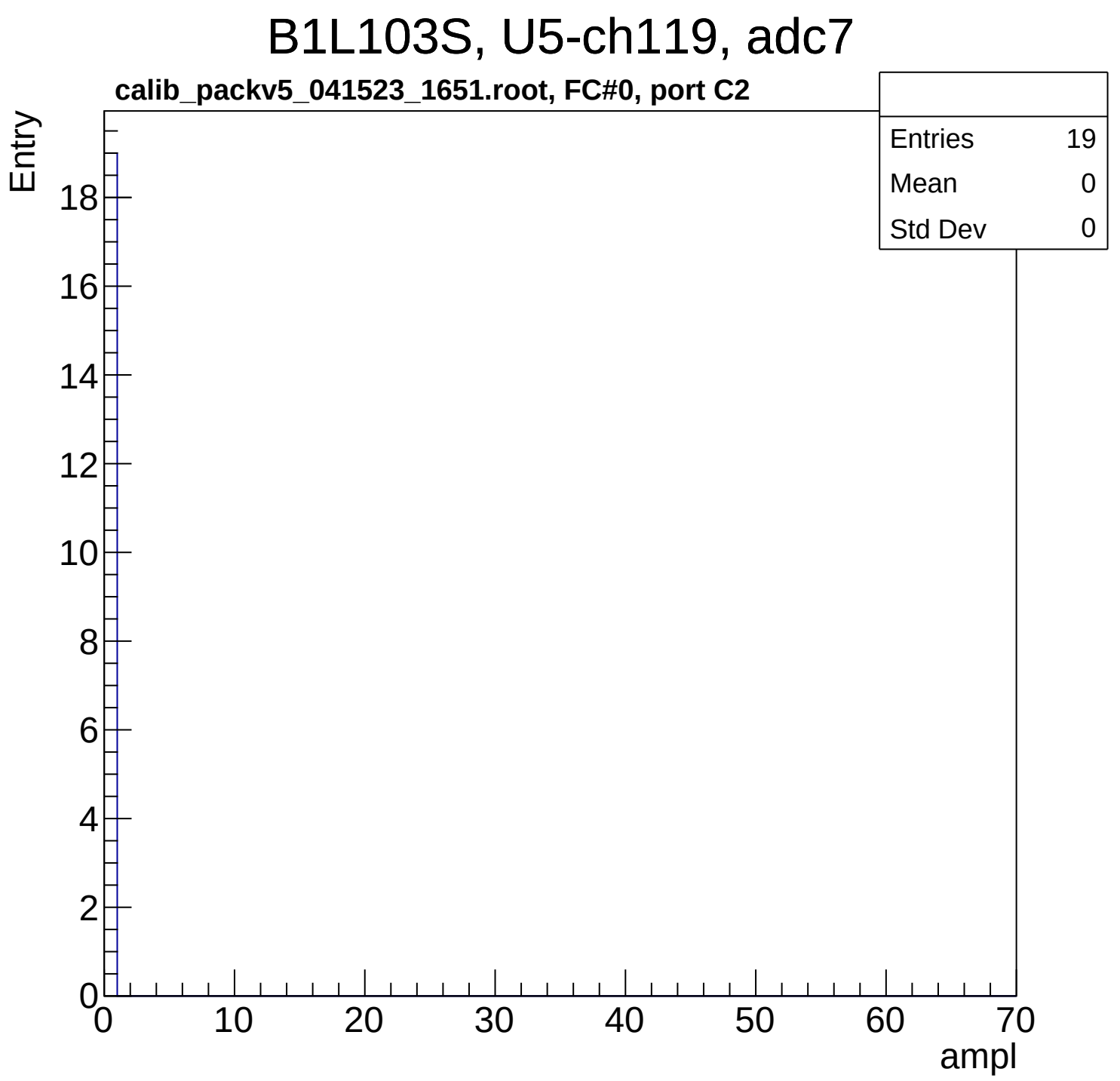
B1L103S, U5-ch119, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
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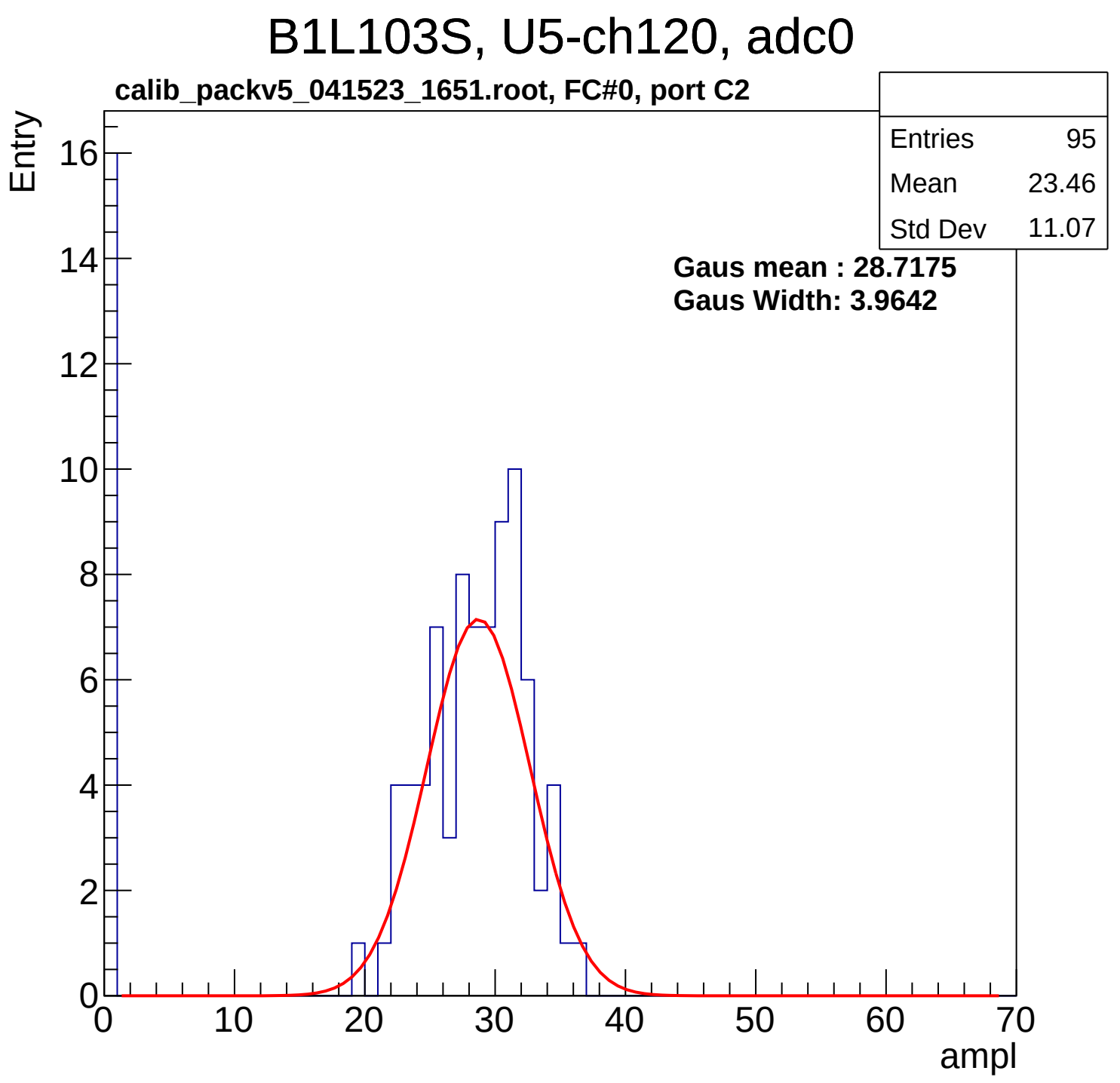
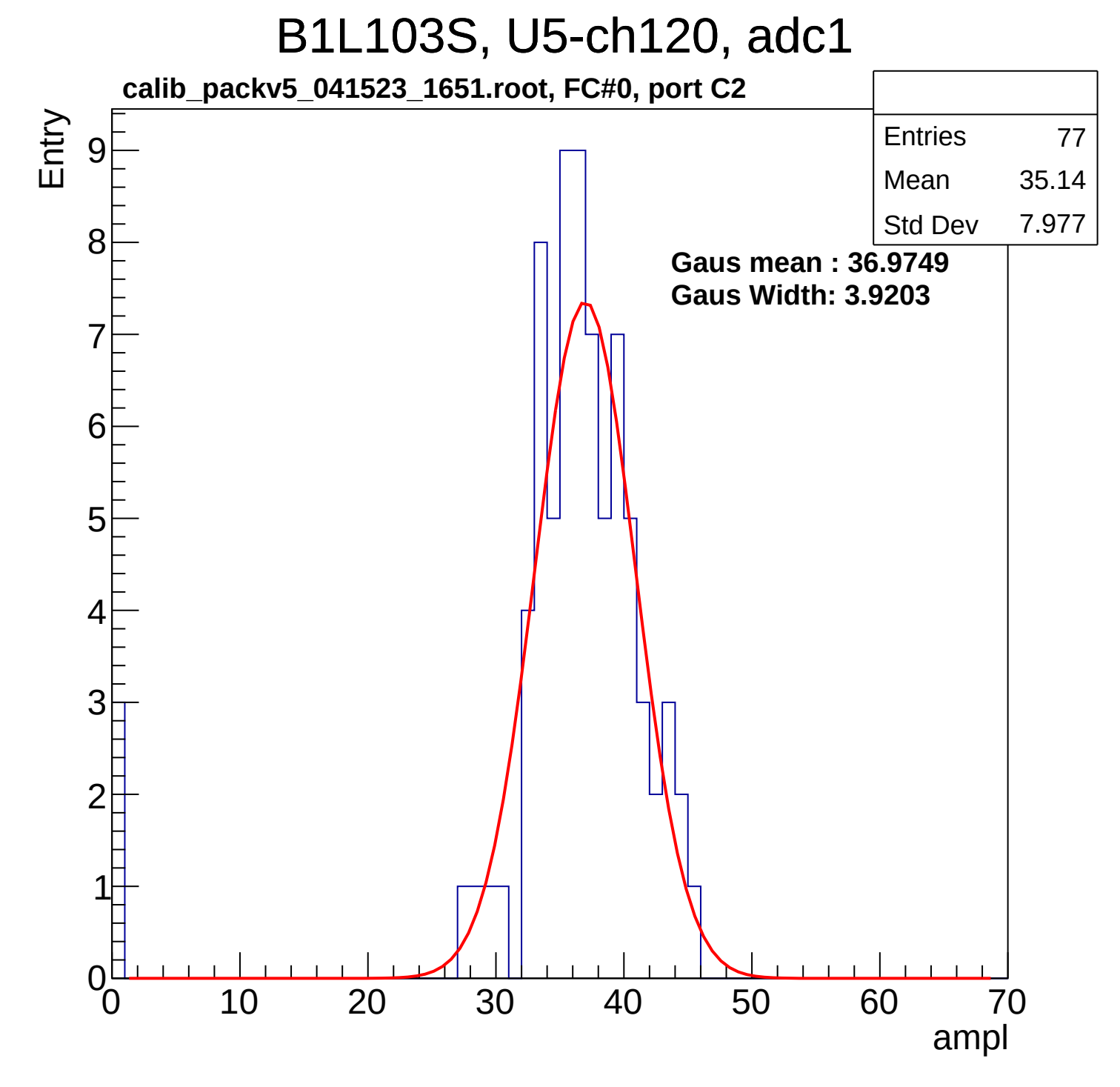
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch120, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 23.46
Std Dev 11.07
Gaus mean : 28.7175
Gaus Width: 3.9642
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U5-ch120, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 35.14
Std Dev 7.977
Gaus mean : 36.9749
Gaus Width: 3.9203
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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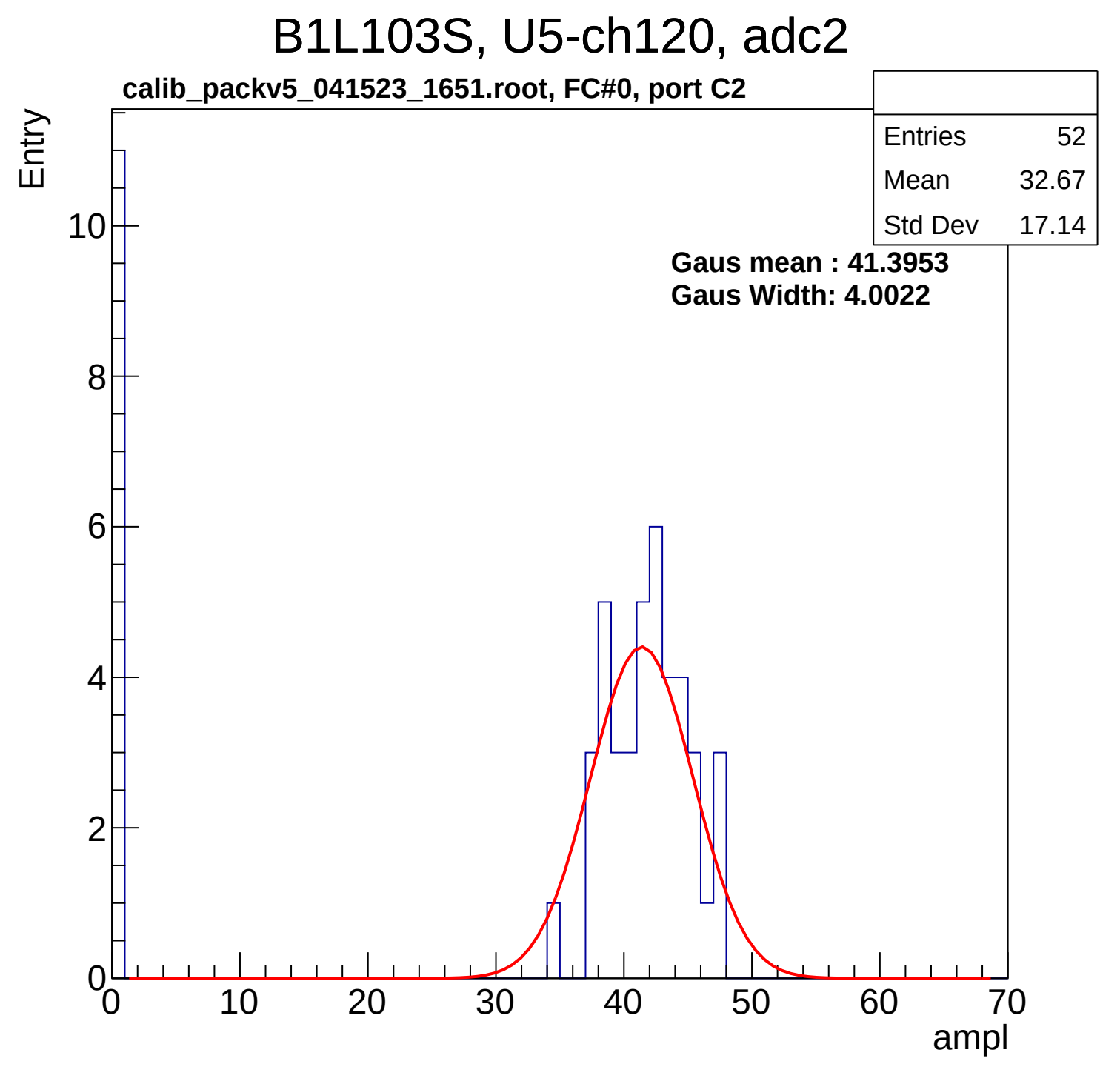
B1L103S, U5-ch120, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 32.67
Std Dev 17.14
Gaus mean : 41.3953
Gaus Width: 4.0022
Entry
ampl
0
2
4
6
8
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0
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20
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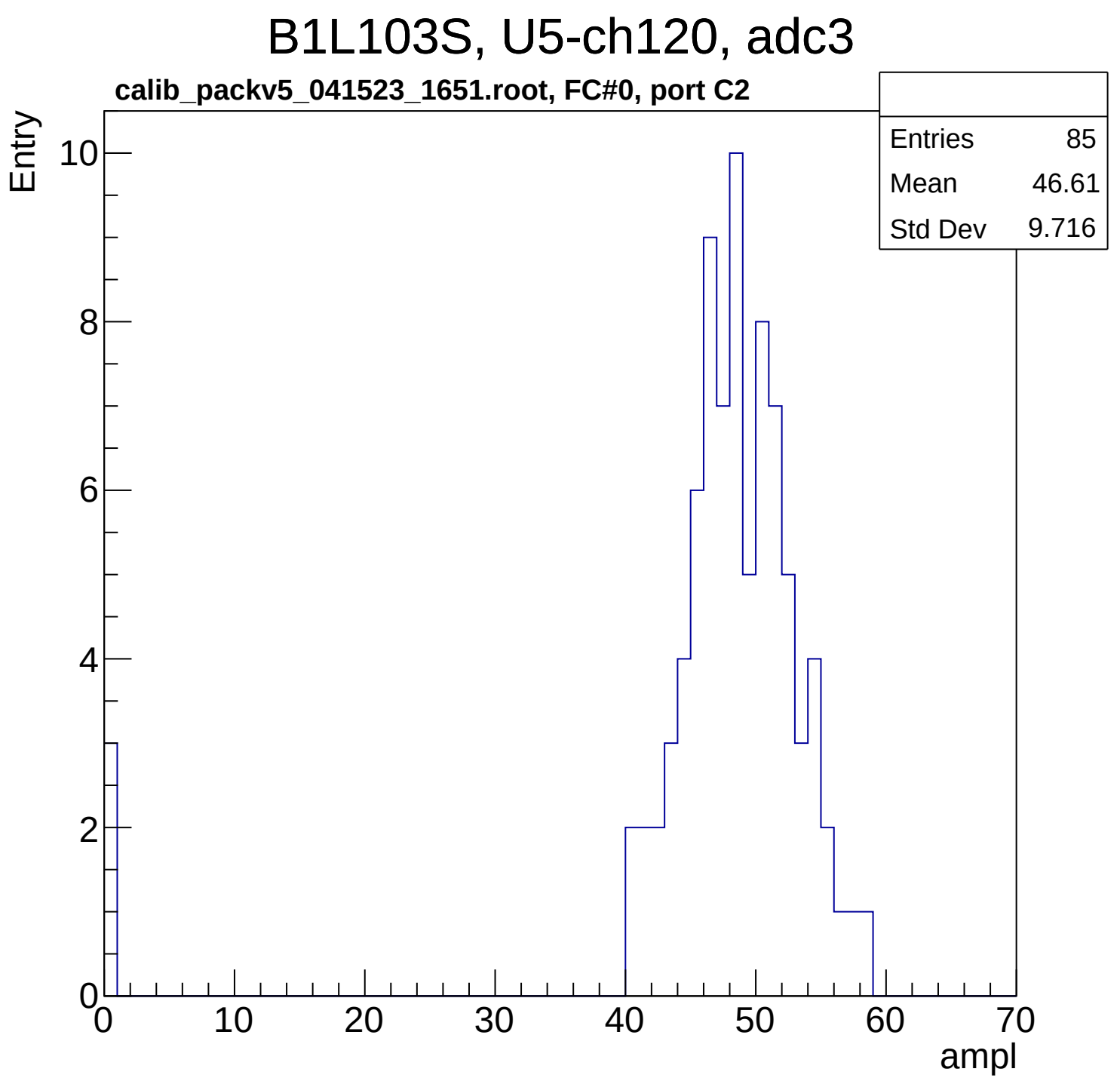
B1L103S, U5-ch120, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 46.61
Std Dev 9.716
Entry
ampl
0
2
4
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8
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0
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40
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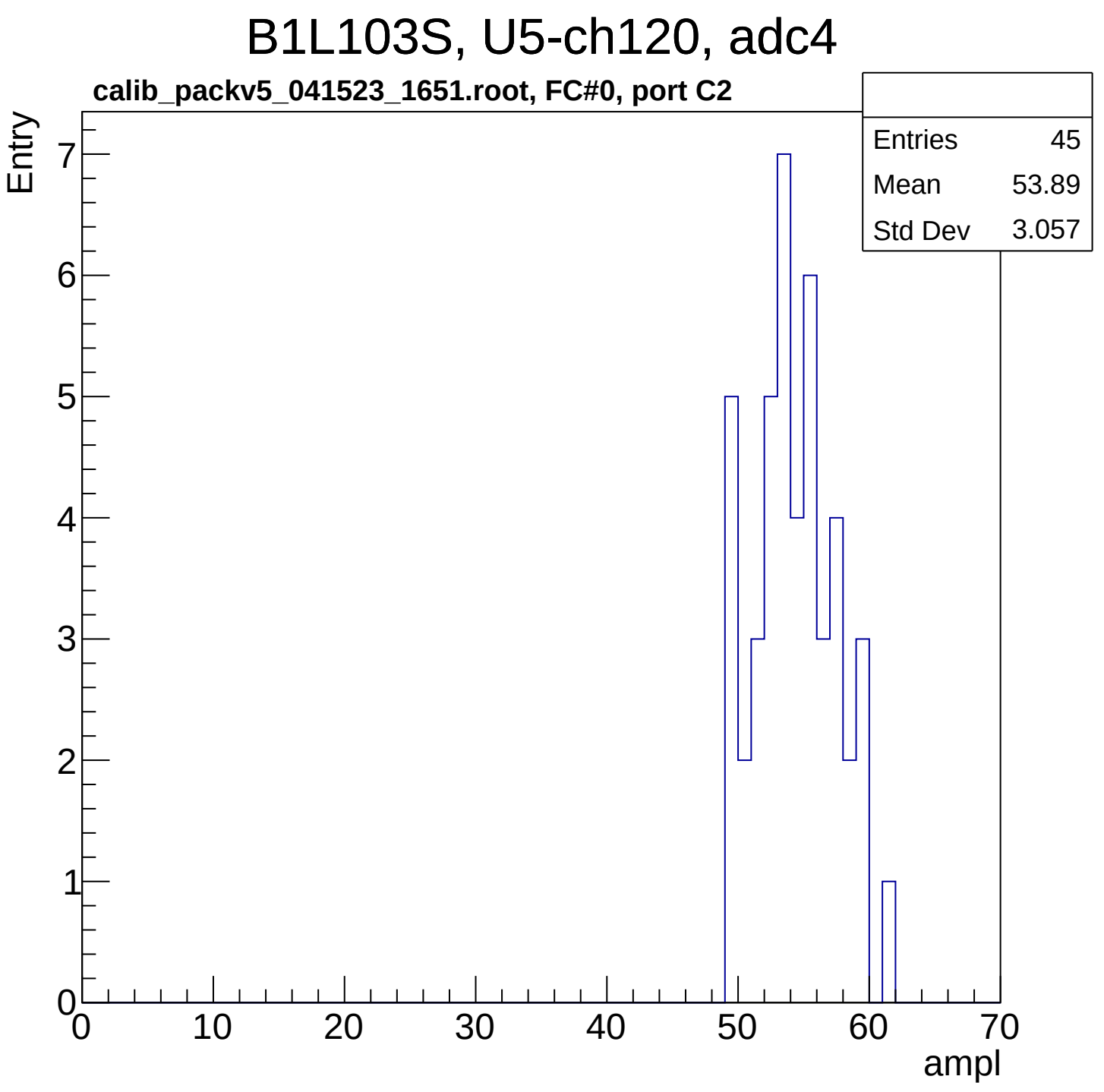
B1L103S, U5-ch120, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 53.89
Std Dev 3.057
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
30
40
50
60
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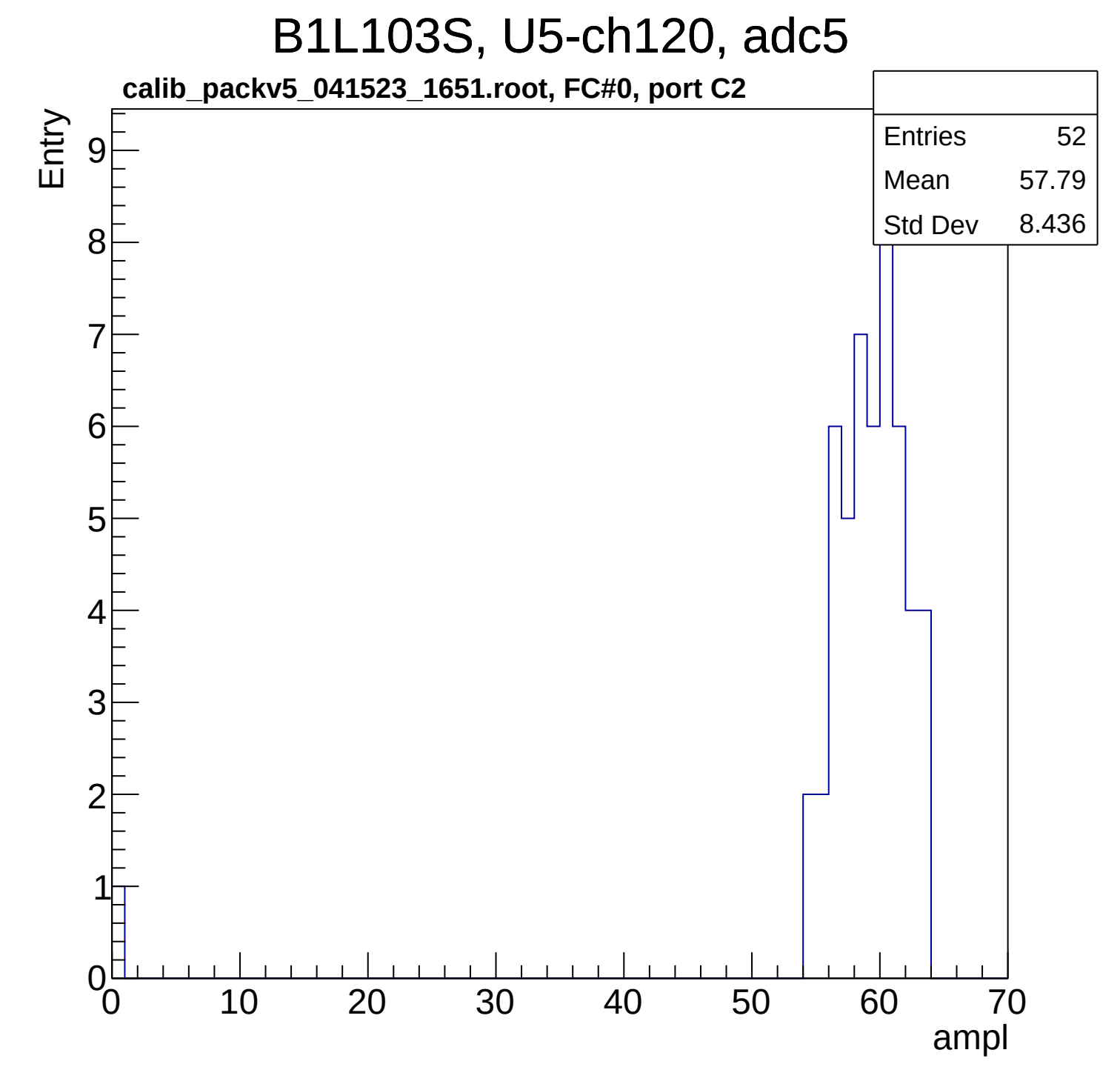
B1L103S, U5-ch120, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 57.79
Std Dev 8.436
Entry
ampl
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3
4
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6
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0
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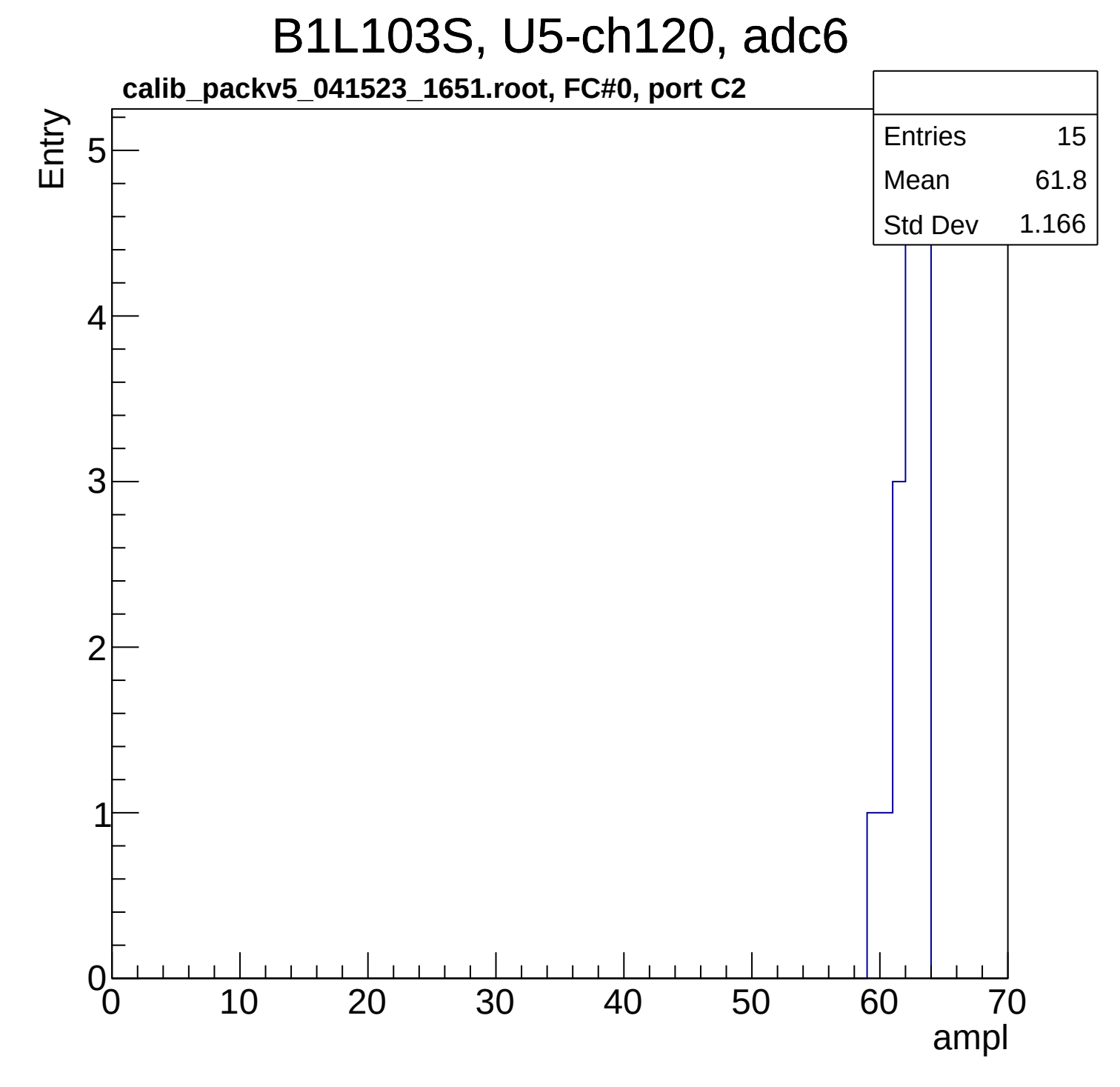
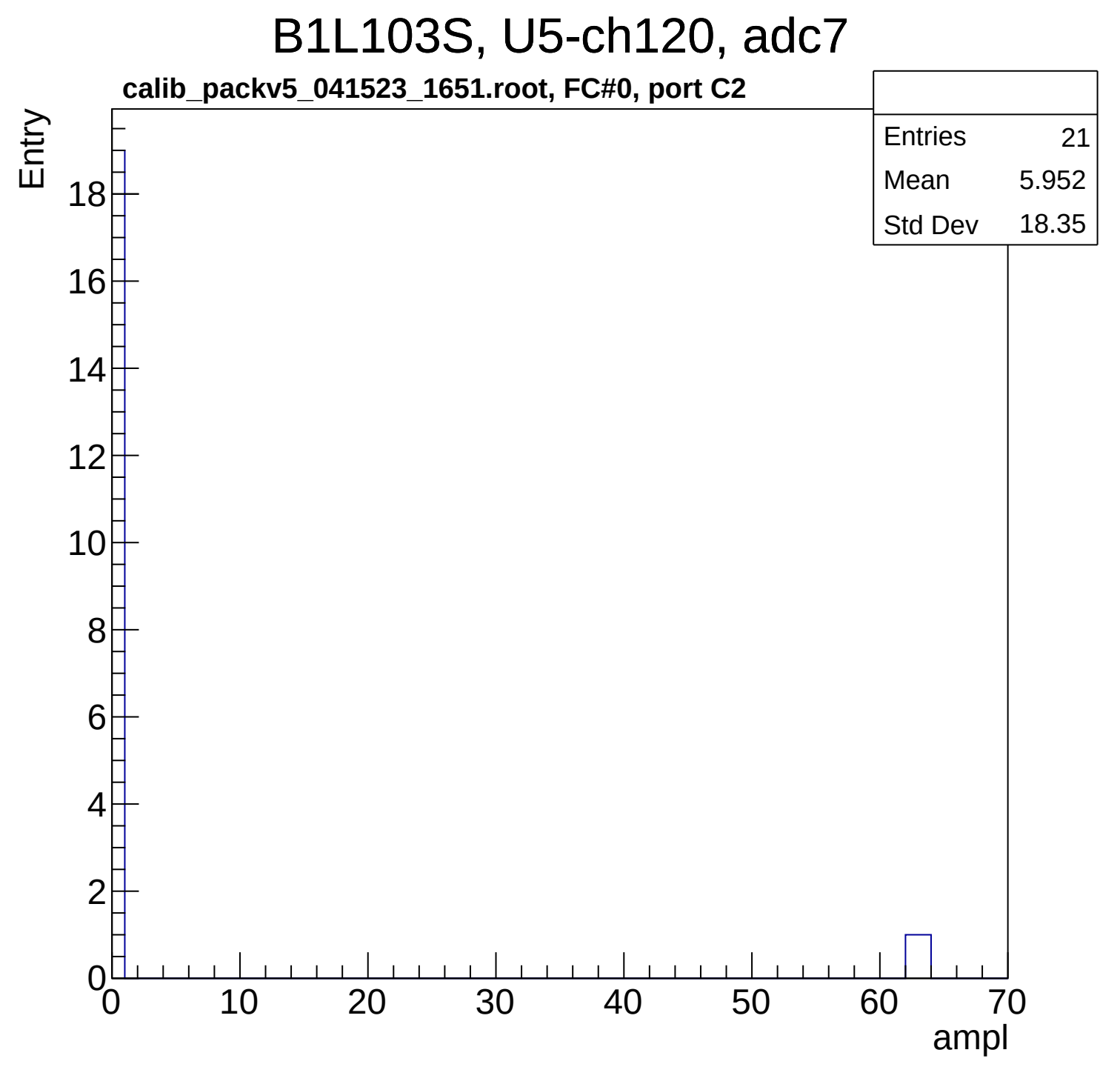
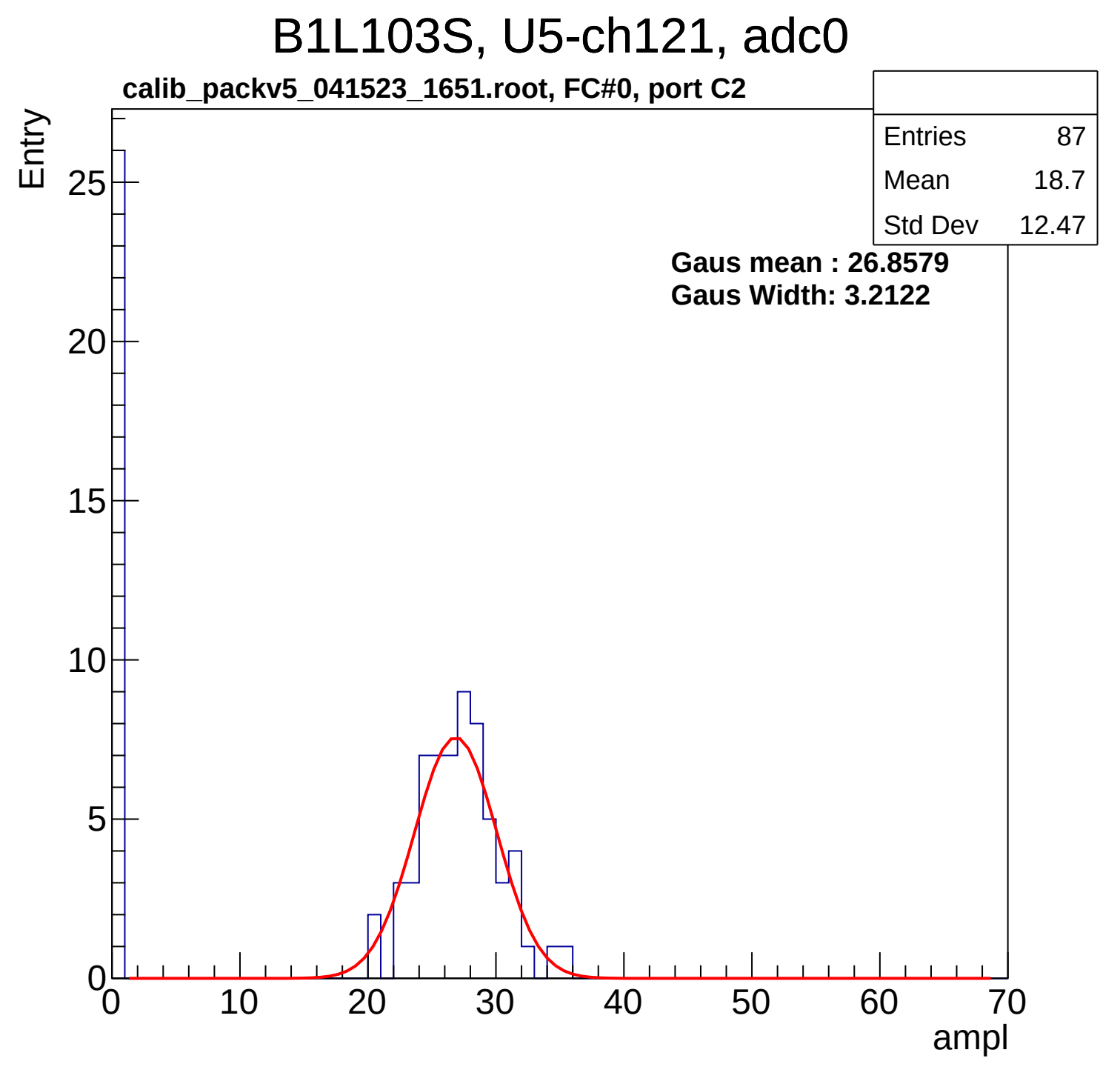
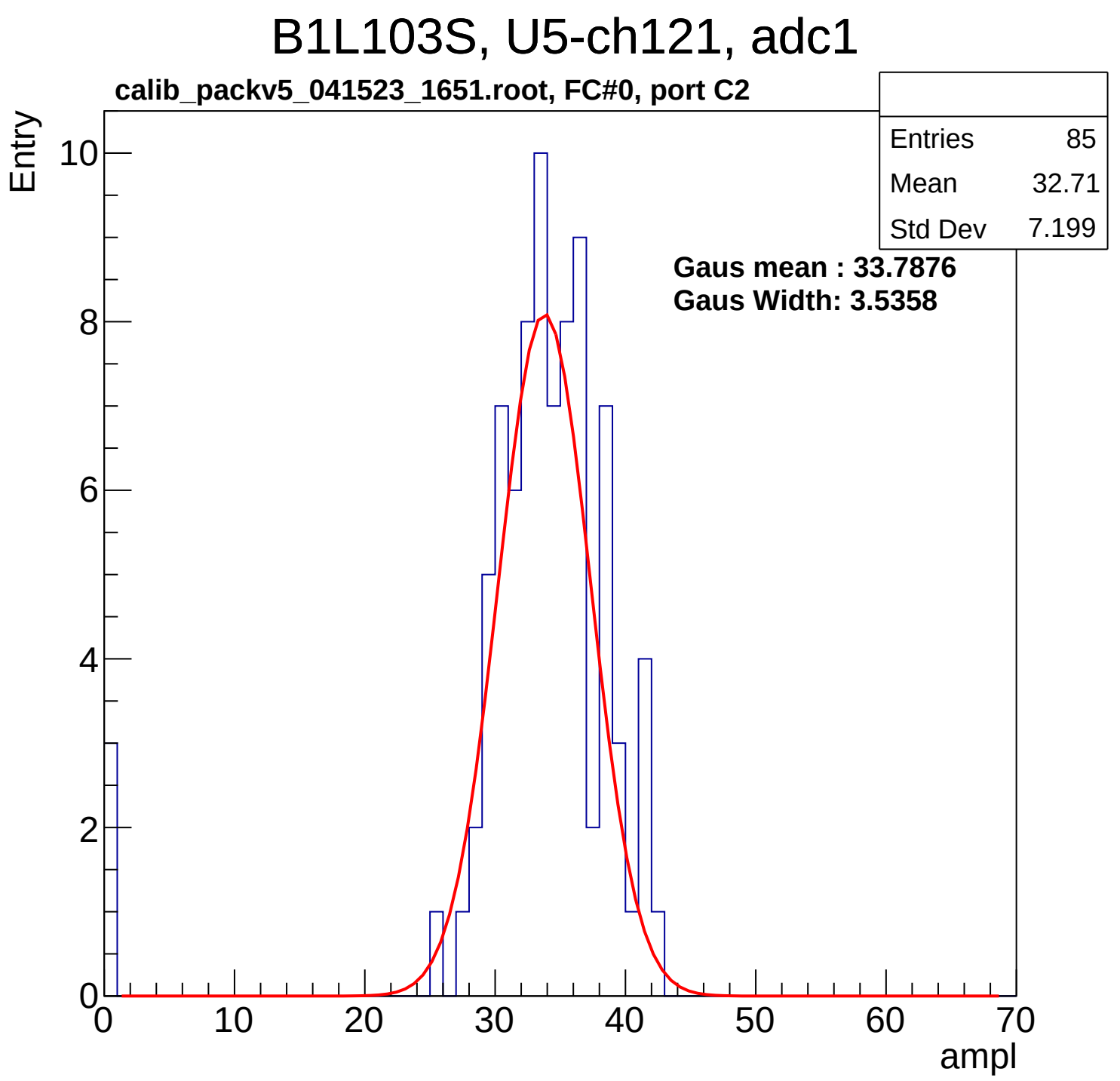

B1L103S, U5-ch120, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.8
Std Dev 1.166
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch120, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch121, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 18.7
Std Dev 12.47
Gaus mean : 26.8579
Gaus Width: 3.2122
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U5-ch121, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 32.71
Std Dev 7.199
Gaus mean : 33.7876
Gaus Width: 3.5358
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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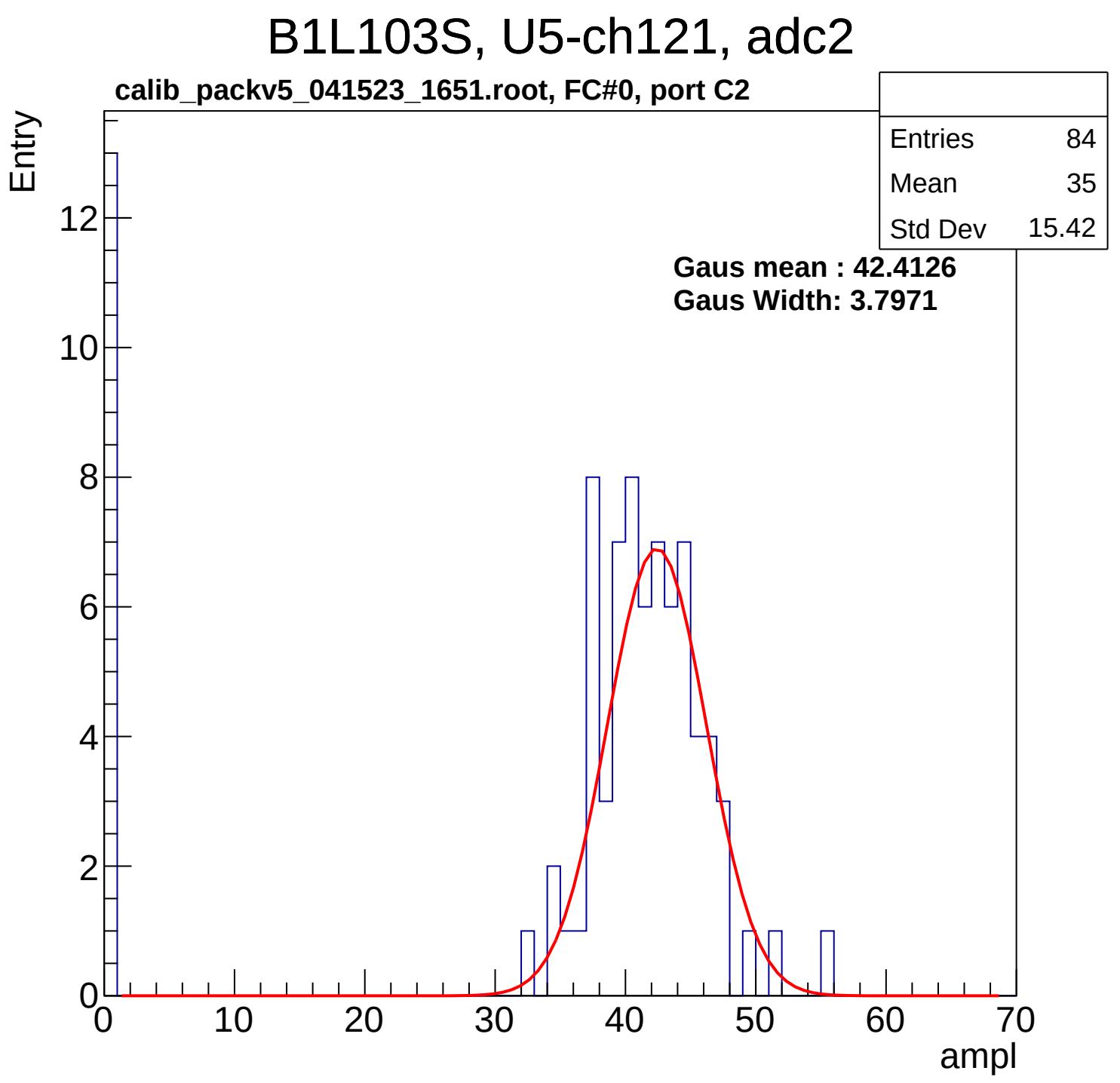
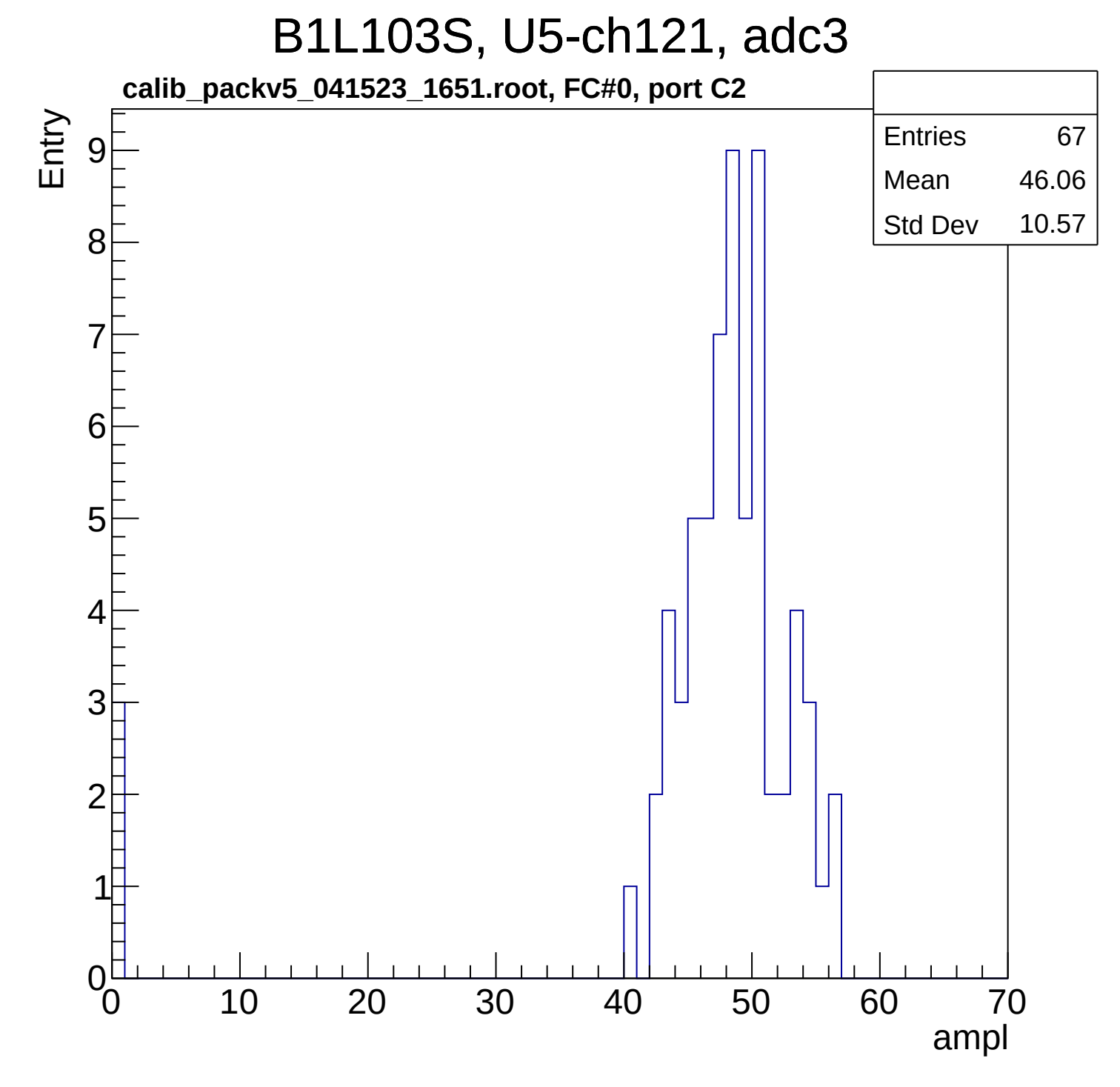

B1L103S, U5-ch121, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 35
Std Dev 15.42
Gaus mean : 42.4126
Gaus Width: 3.7971
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U5-ch121, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 46.06
Std Dev 10.57
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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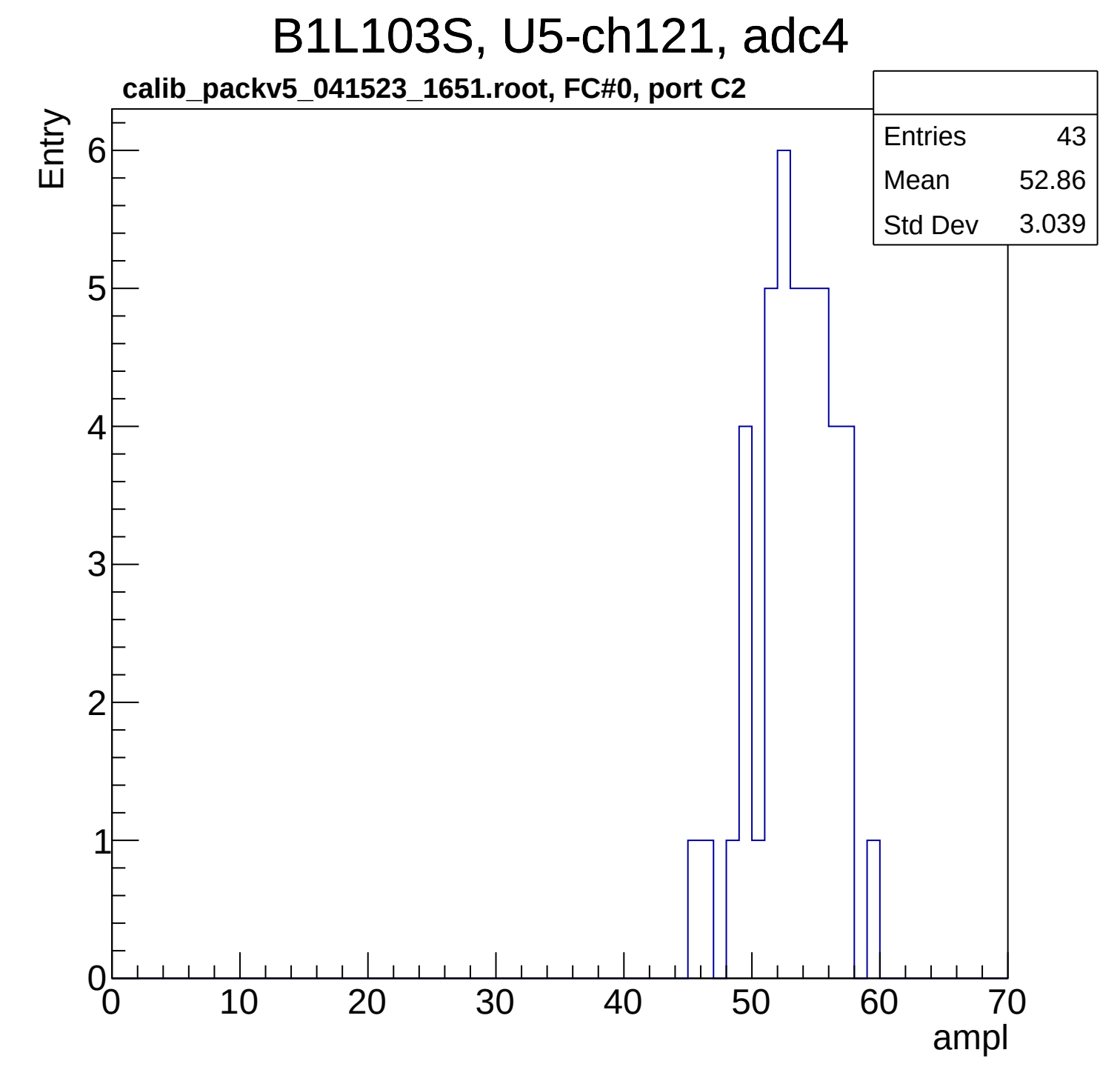
B1L103S, U5-ch121, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 52.86
Std Dev 3.039
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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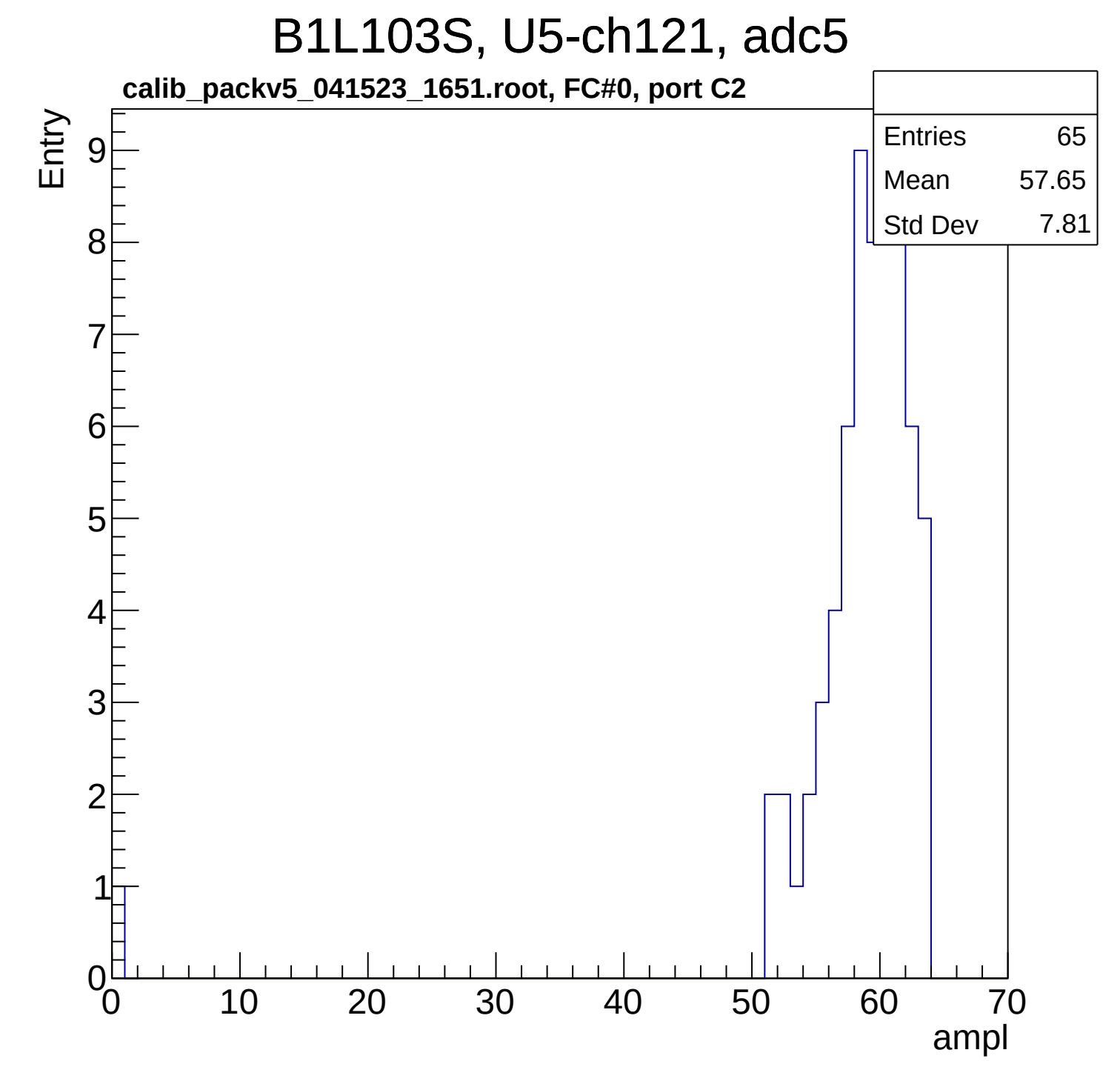
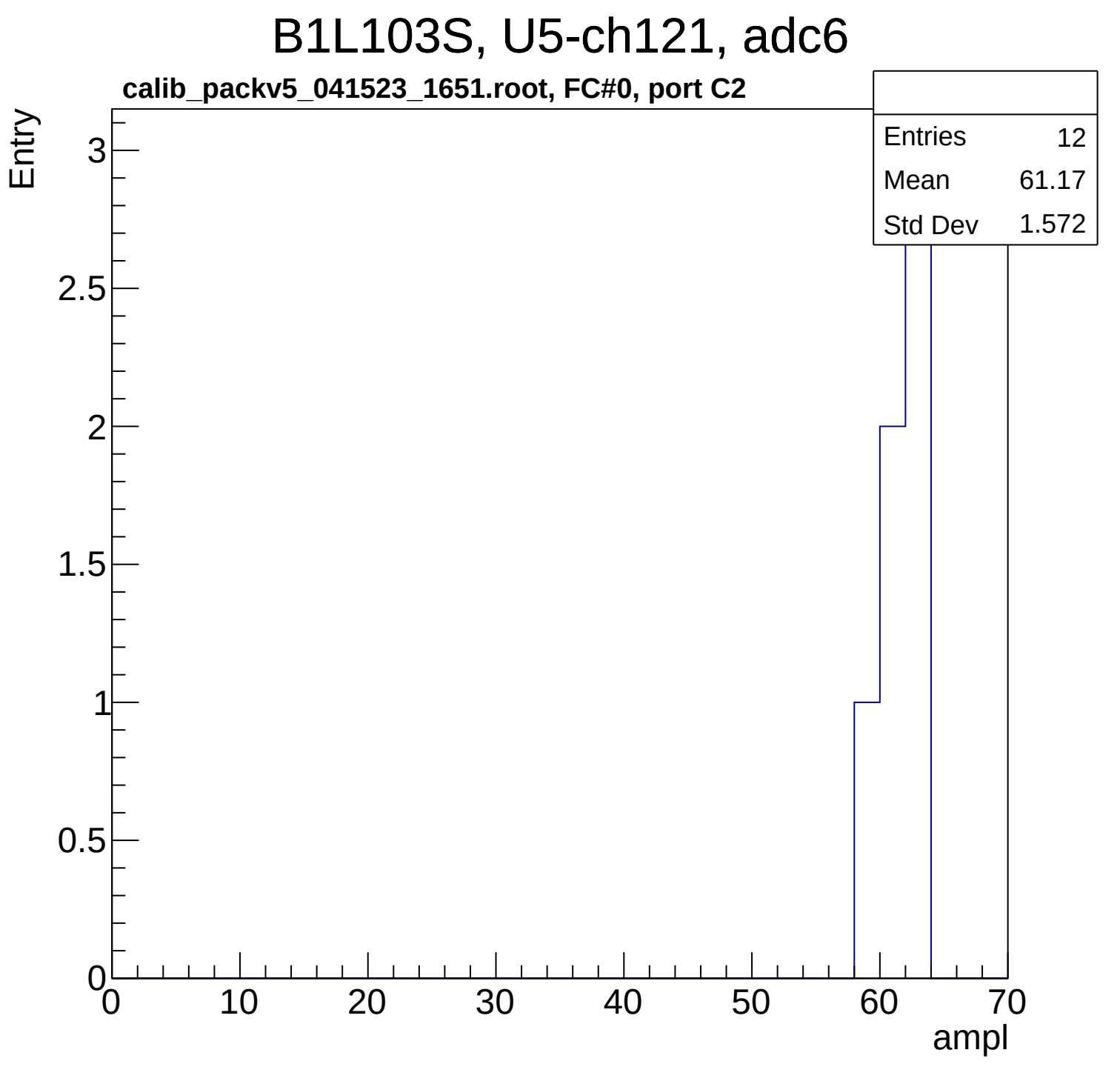

B1L103S, U5-ch121, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 57.65
Std Dev 7.81
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U5-ch121, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.17
Std Dev 1.572
Entry
ampl
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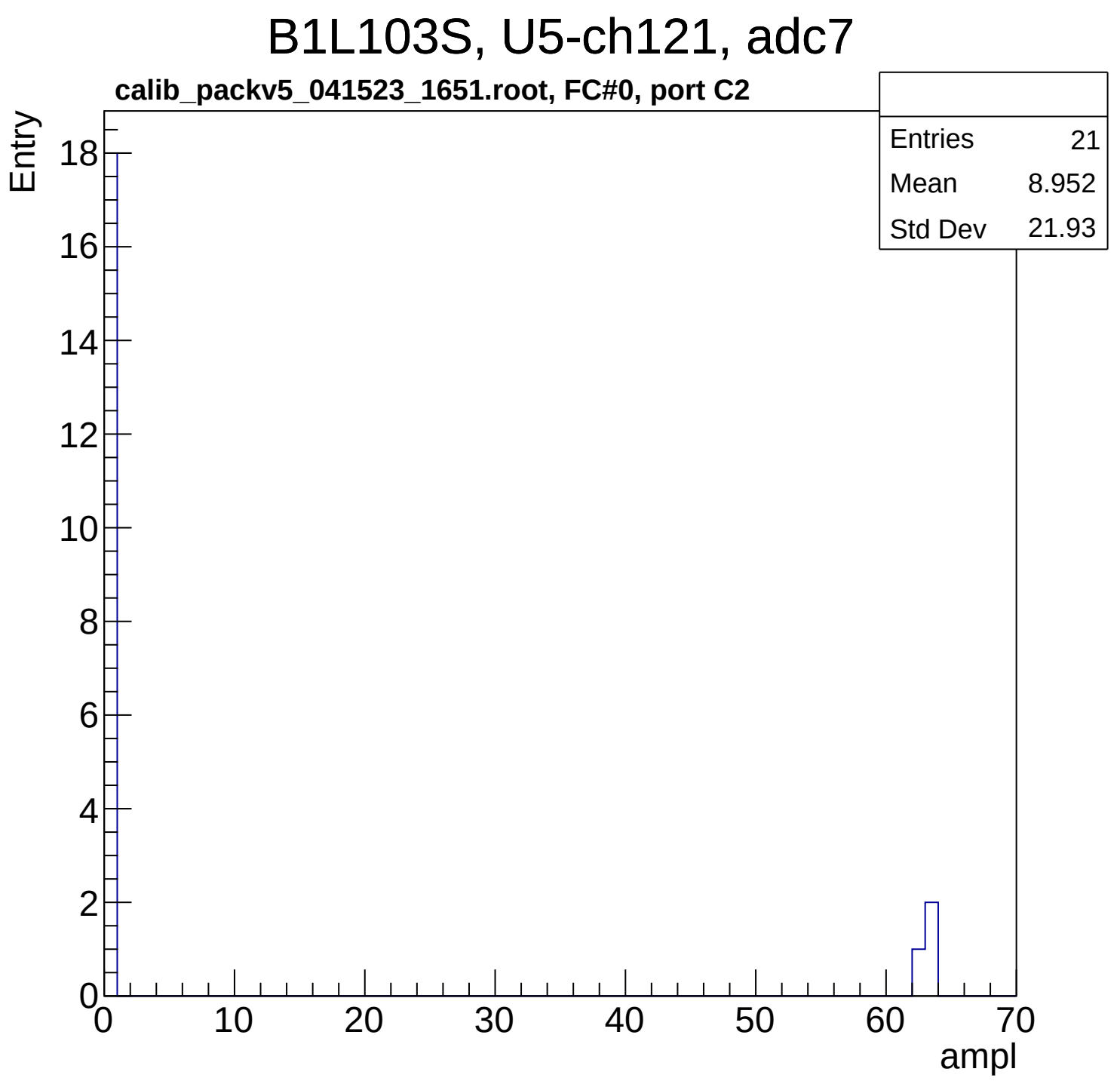
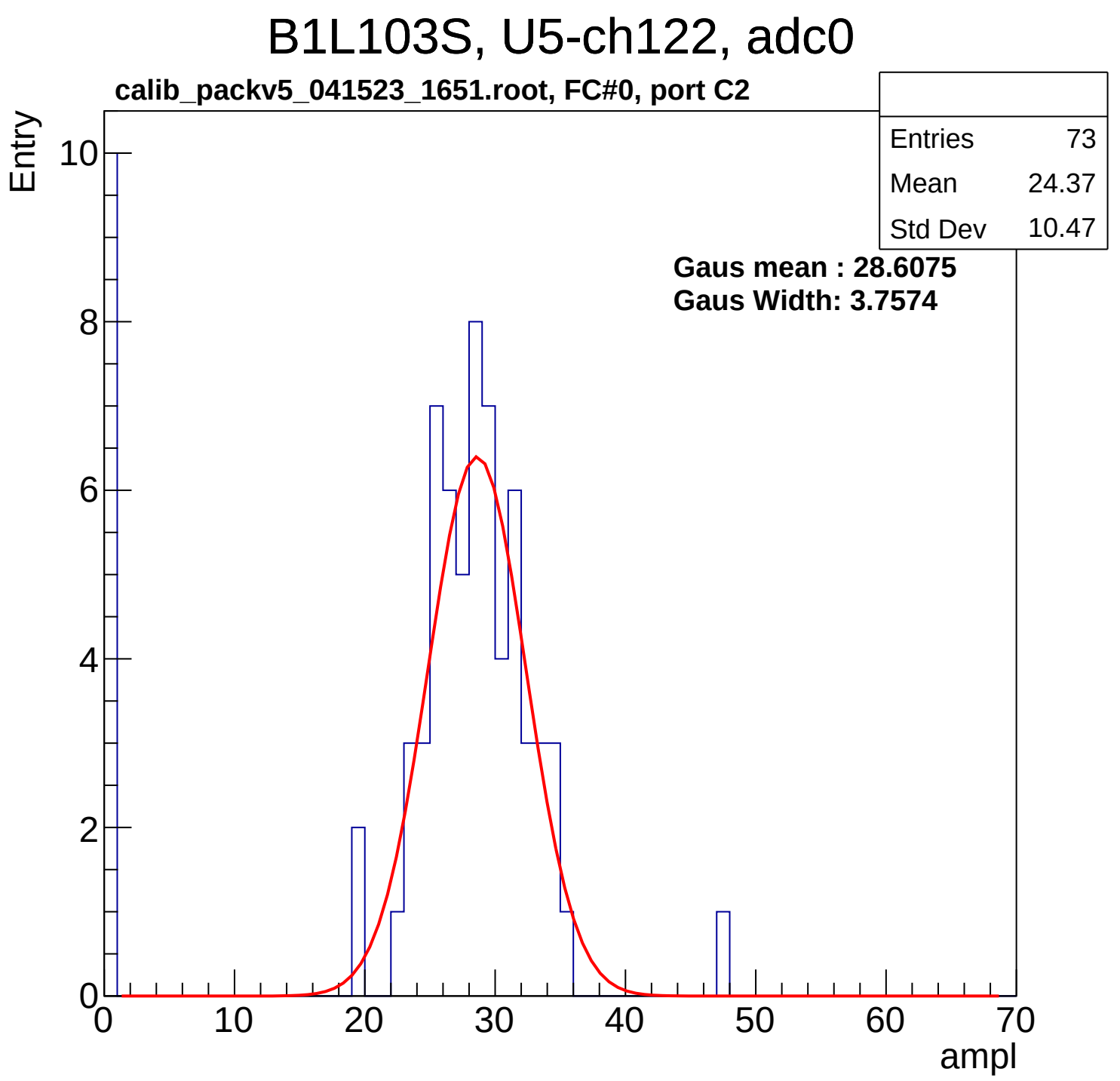
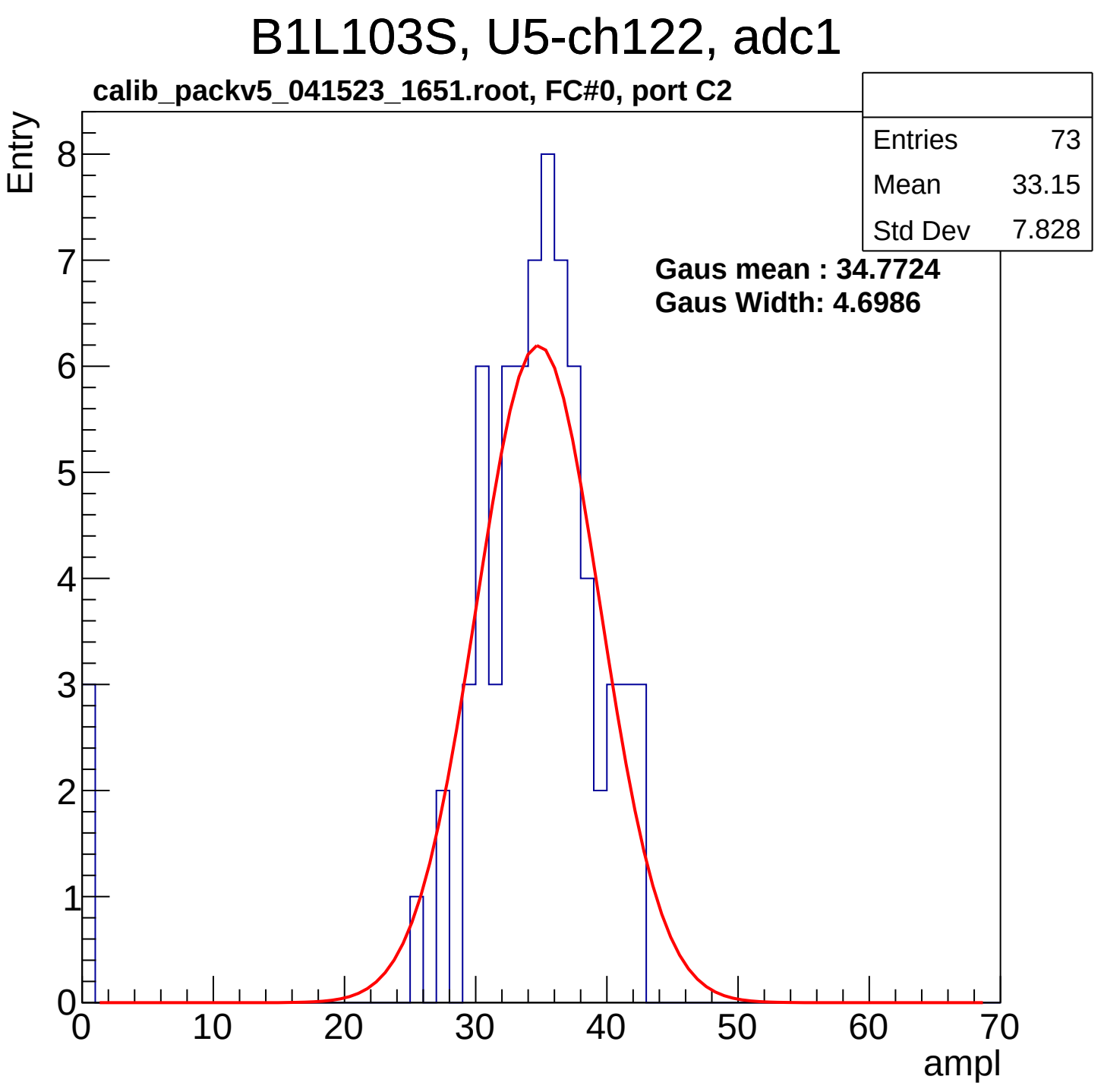
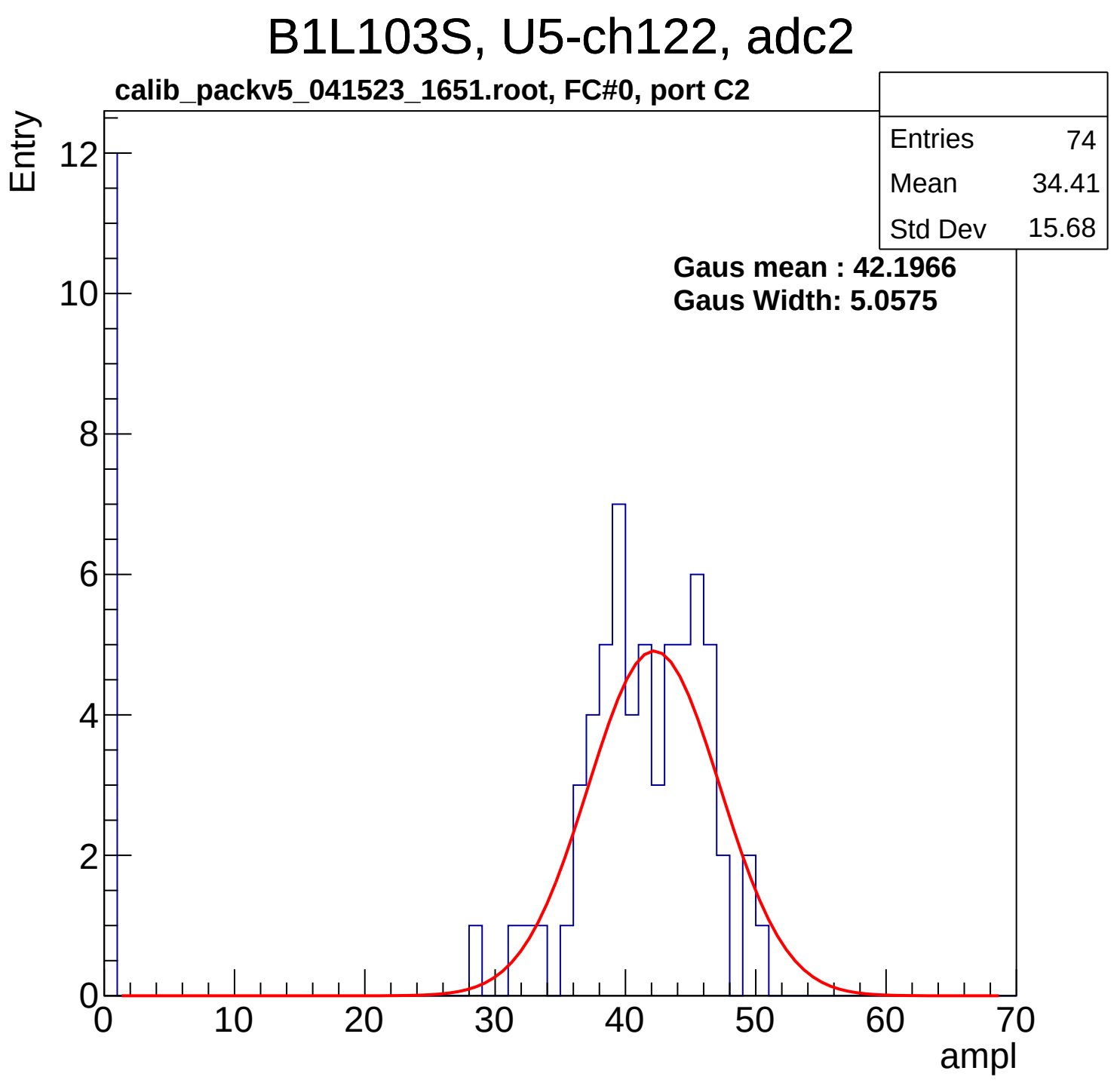
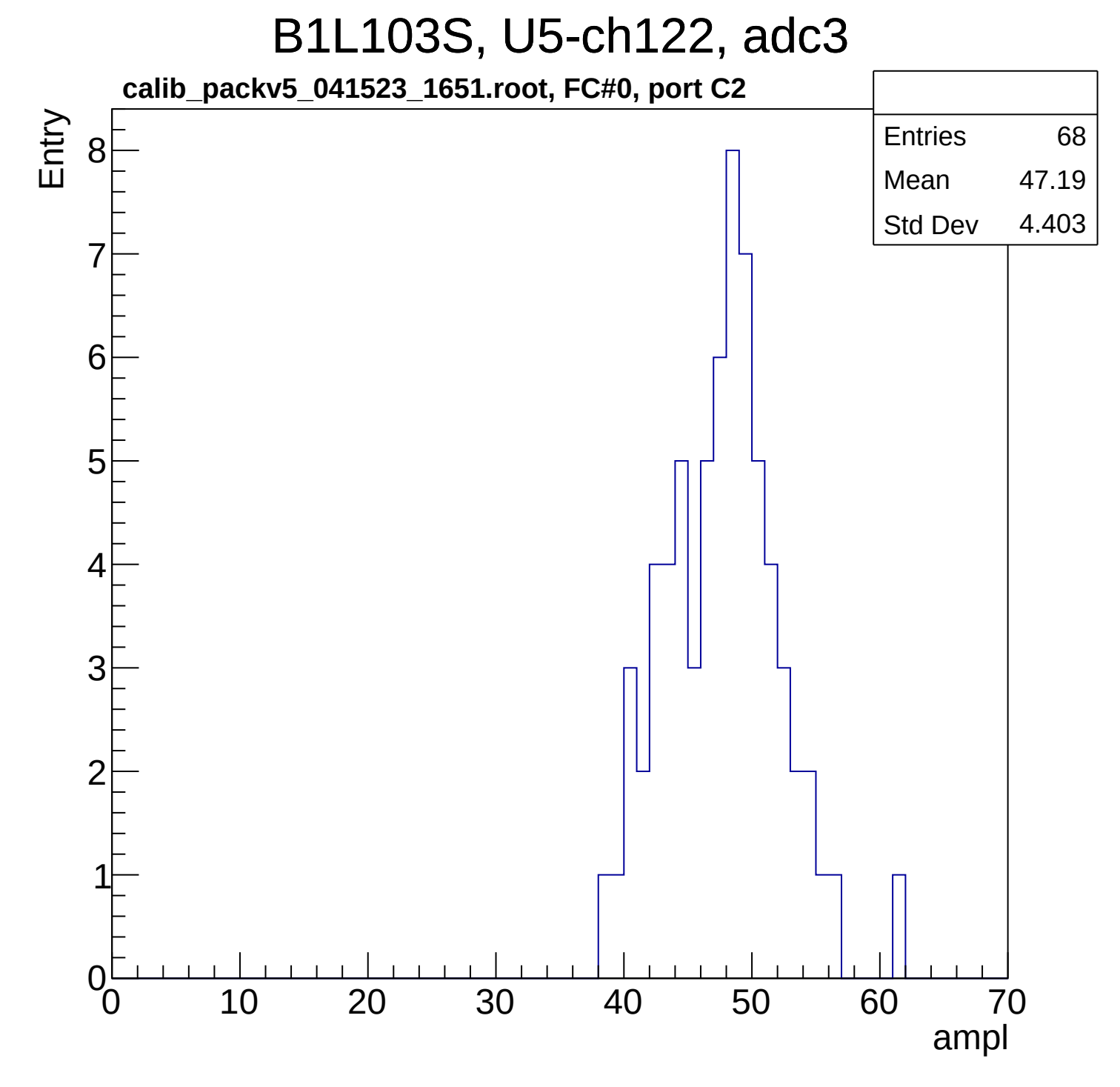
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

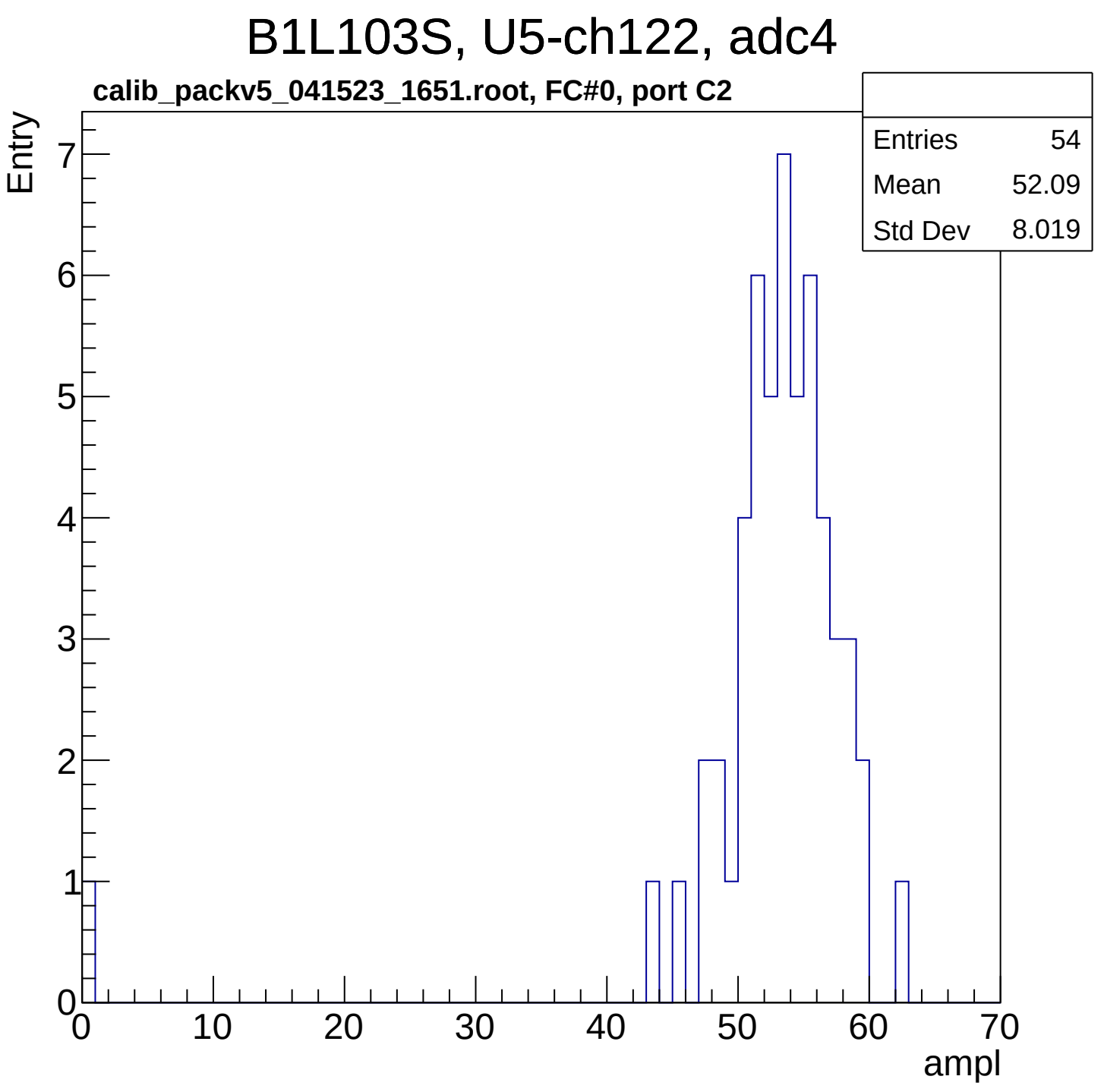

B1L103S, U5-ch121, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 8.952
Std Dev 21.93
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

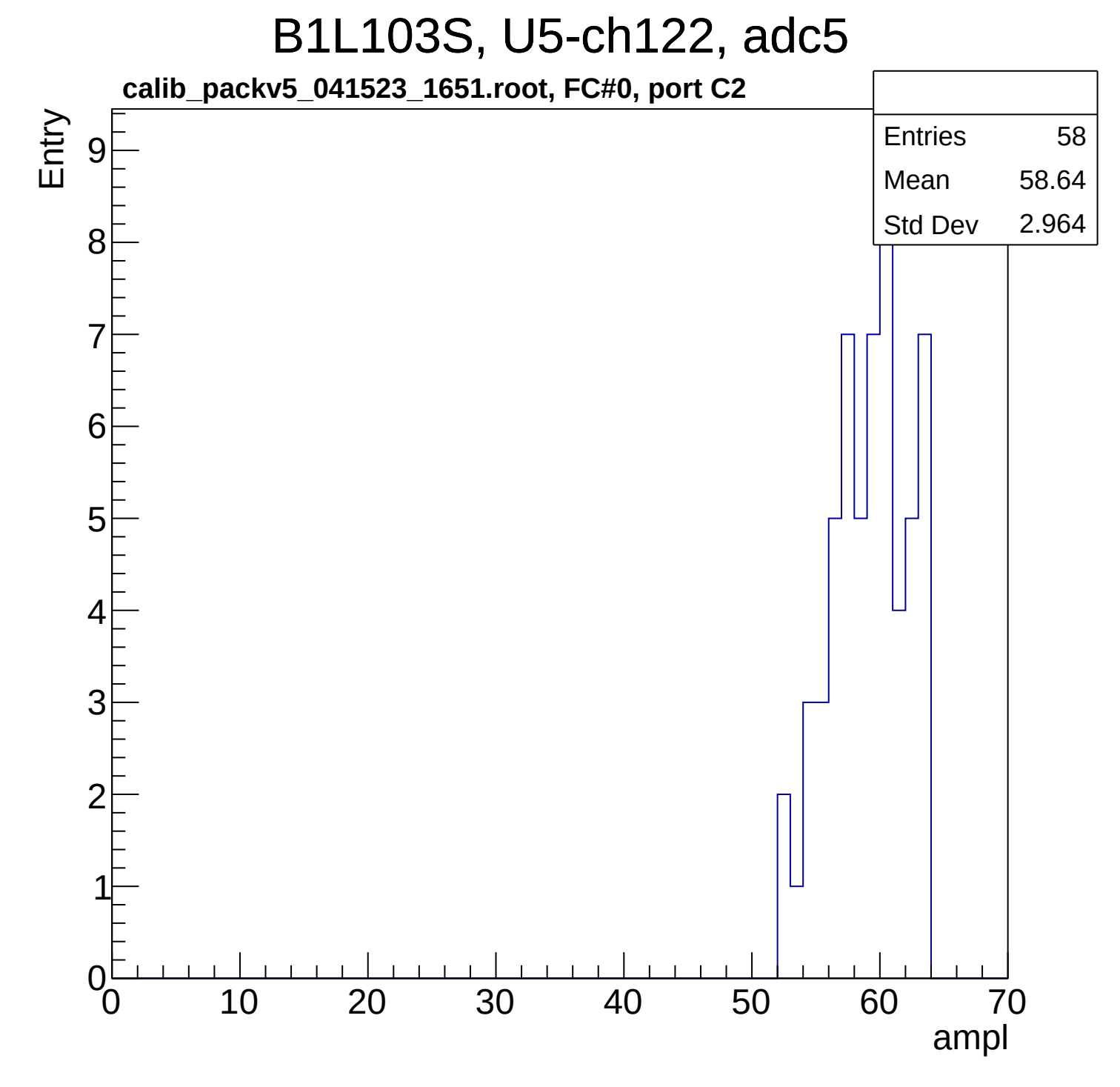

B1L103S, U5-ch122, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 24.37
Std Dev 10.47
Gaus mean : 28.6075
Gaus Width: 3.7574
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U5-ch122, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 33.15
Std Dev 7.828
Gaus mean : 34.7724
Gaus Width: 4.6986
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U5-ch122, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 34.41
Std Dev 15.68
Gaus mean : 42.1966
Gaus Width: 5.0575
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U5-ch122, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 47.19
Std Dev 4.403
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U5-ch122, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 52.09
Std Dev 8.019
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U5-ch122, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.64
Std Dev 2.964
Entry
ampl
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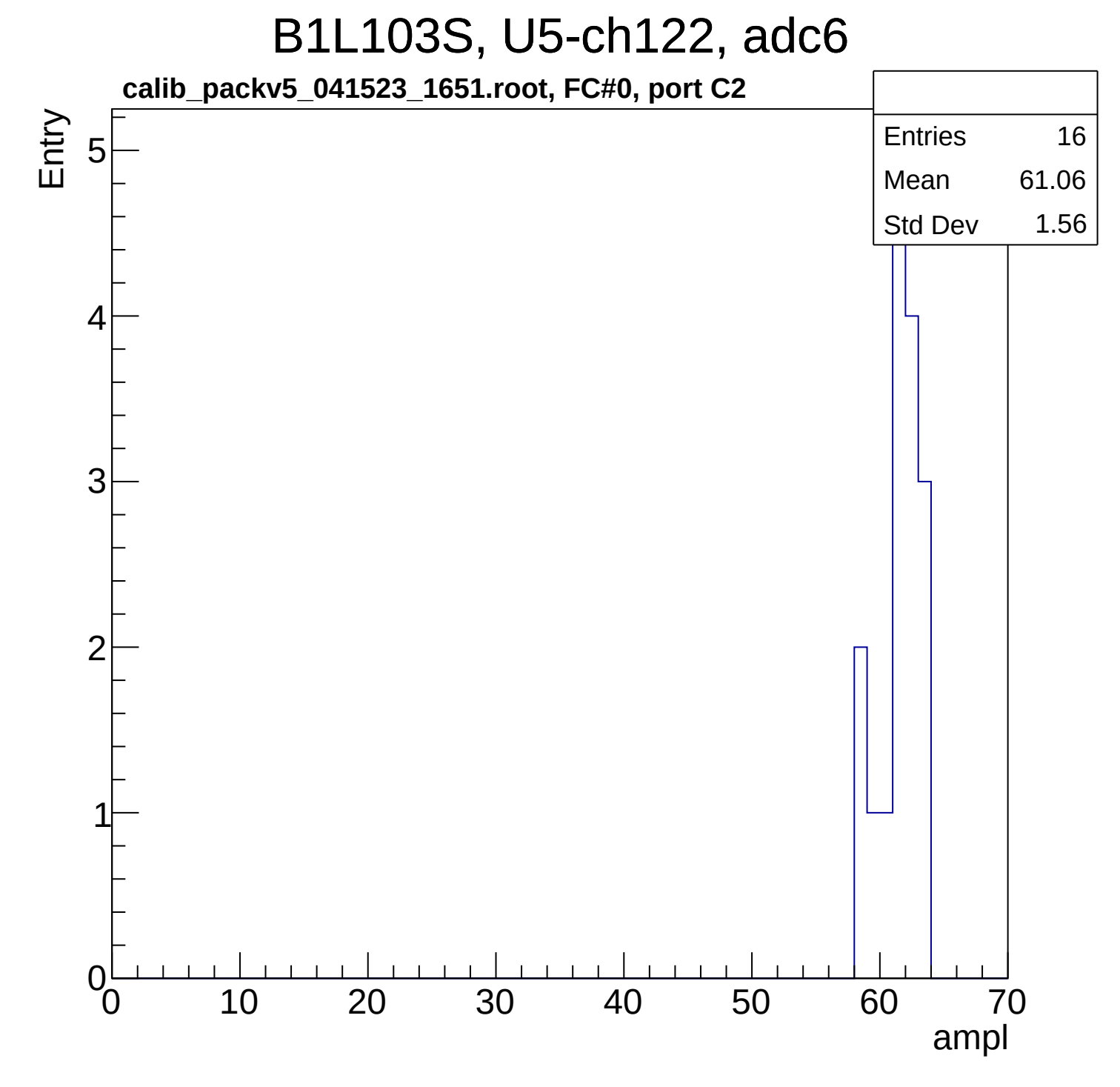
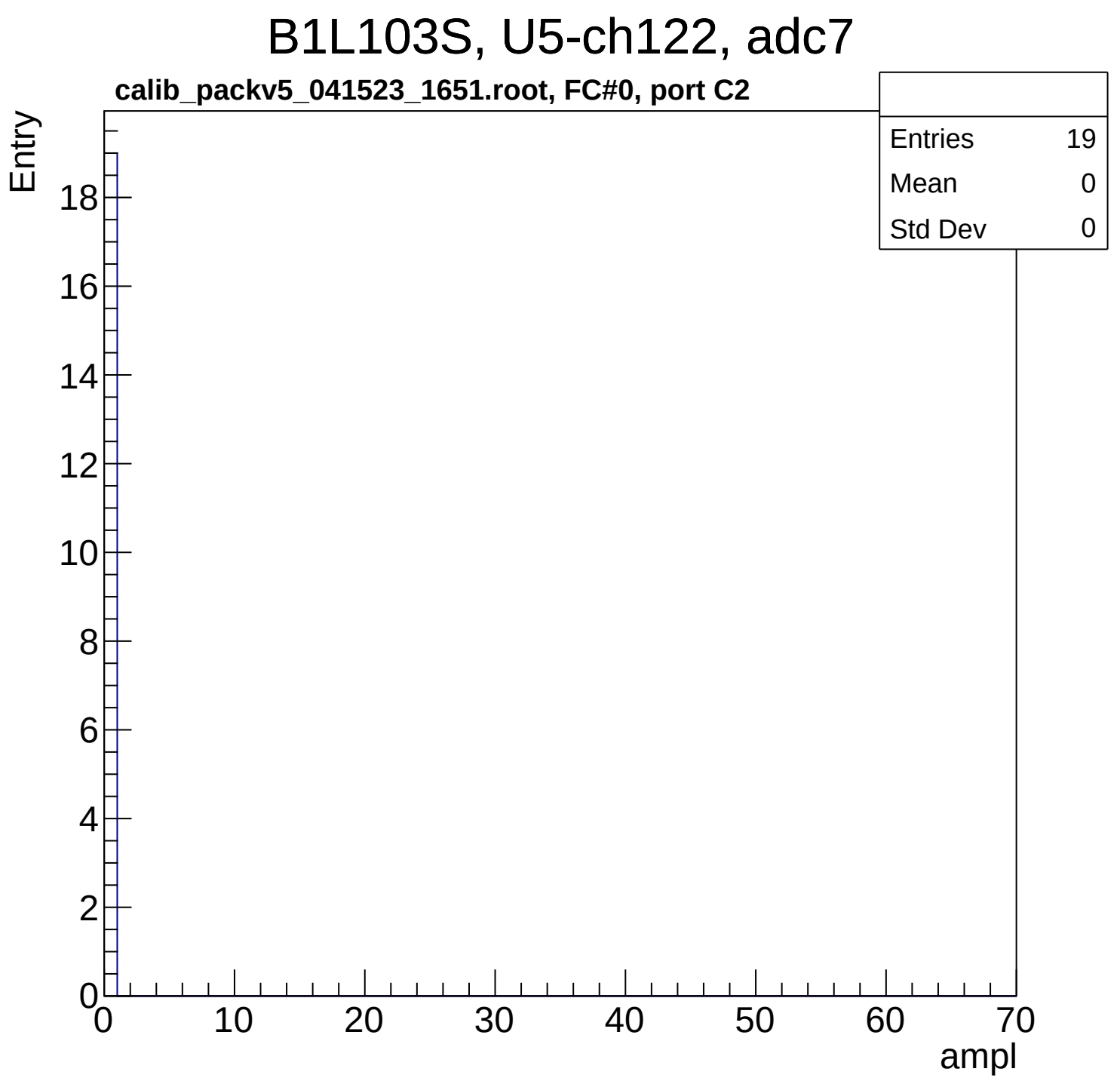
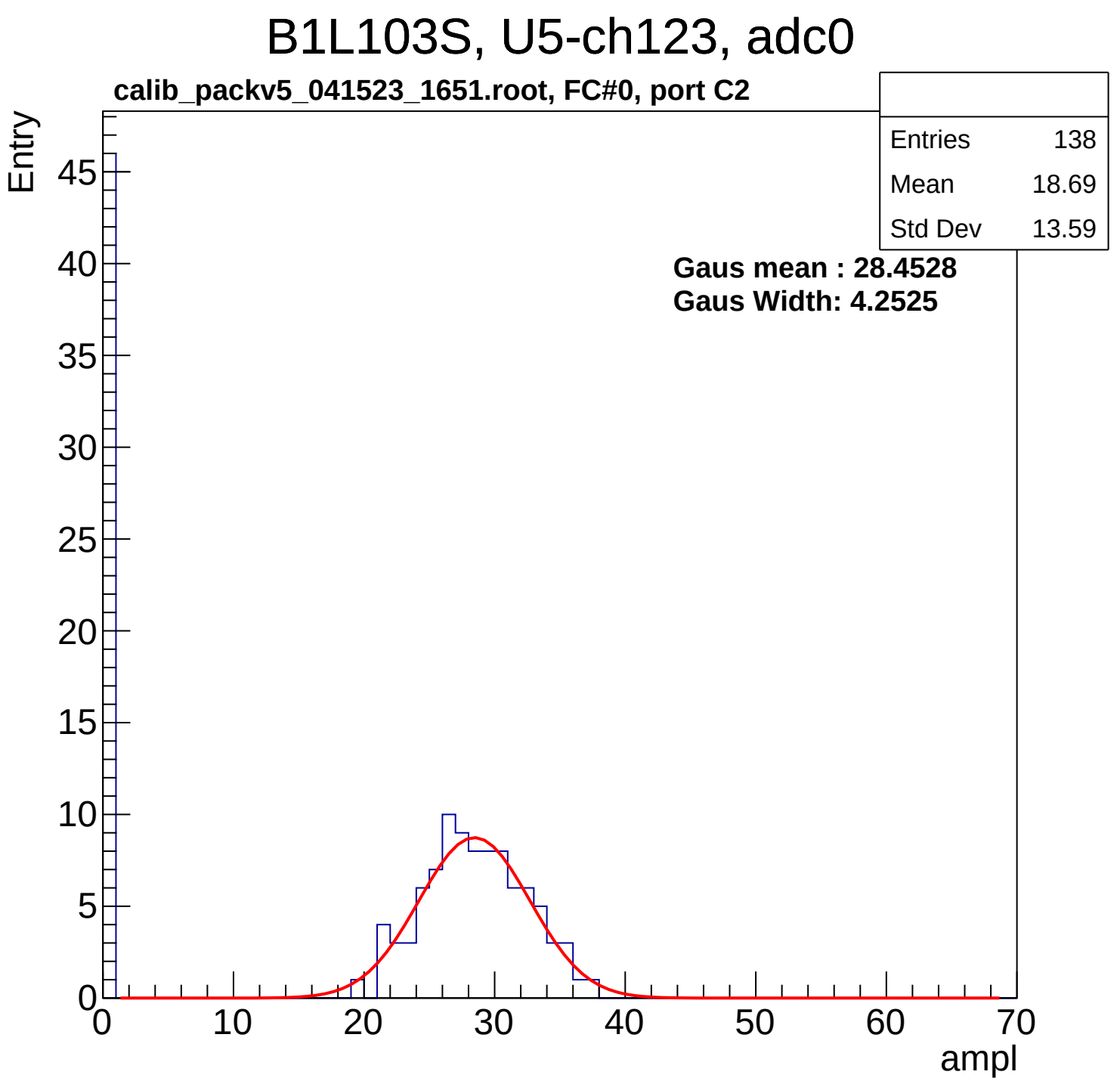
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U5-ch122, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 61.06
Std Dev 1.56
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U5-ch122, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch123, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 138
Mean 18.69
Std Dev 13.59
Gaus mean : 28.4528
Gaus Width: 4.2525
Entry
ampl
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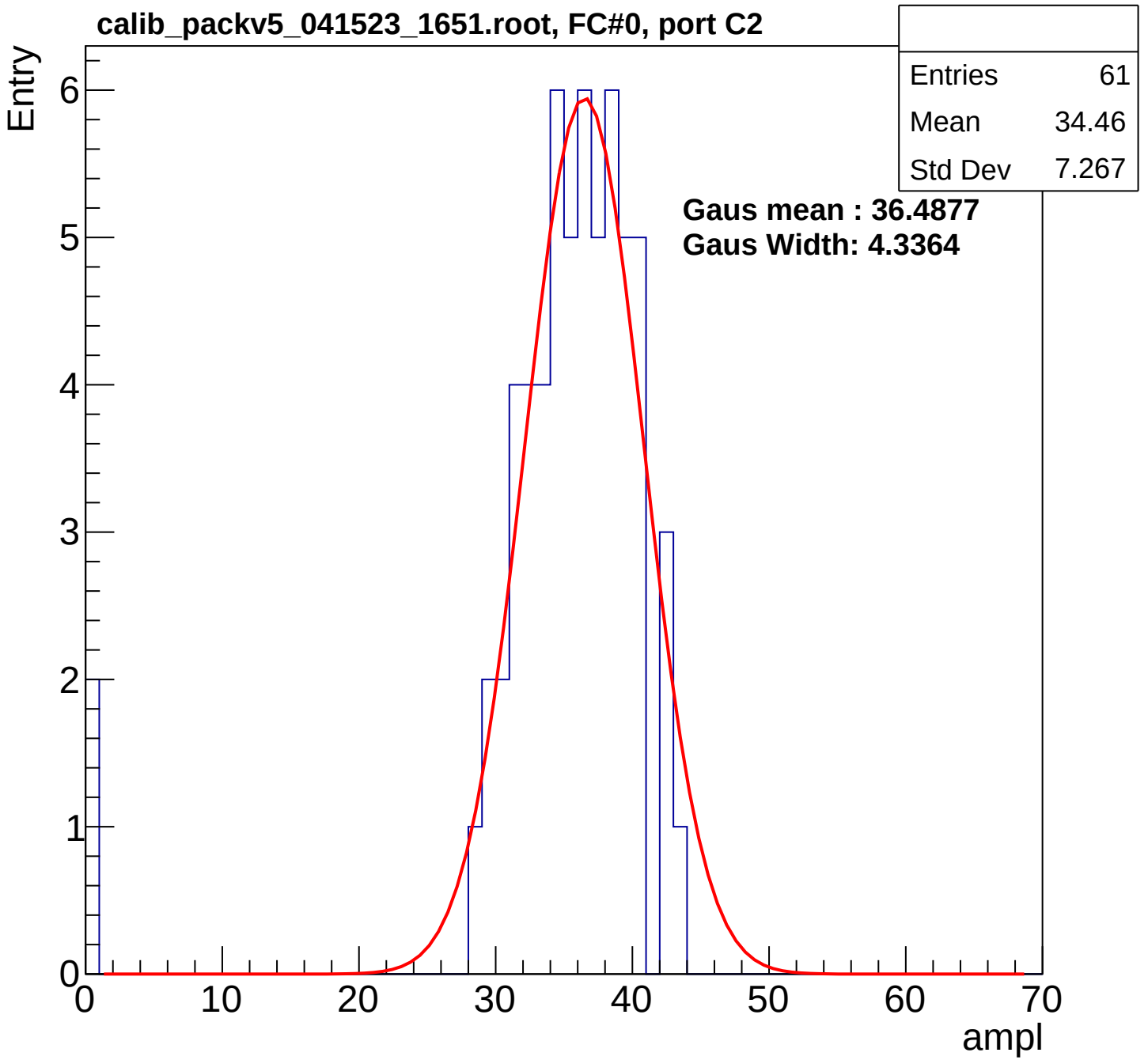
5
10
15
20
25
30
35
40
45
0
10
20
30
40
50
60
70


B1L103S, U5-ch123, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 34.46
Std Dev 7.267
Gaus mean : 36.4877
Gaus Width: 4.3364
Entry
ampl
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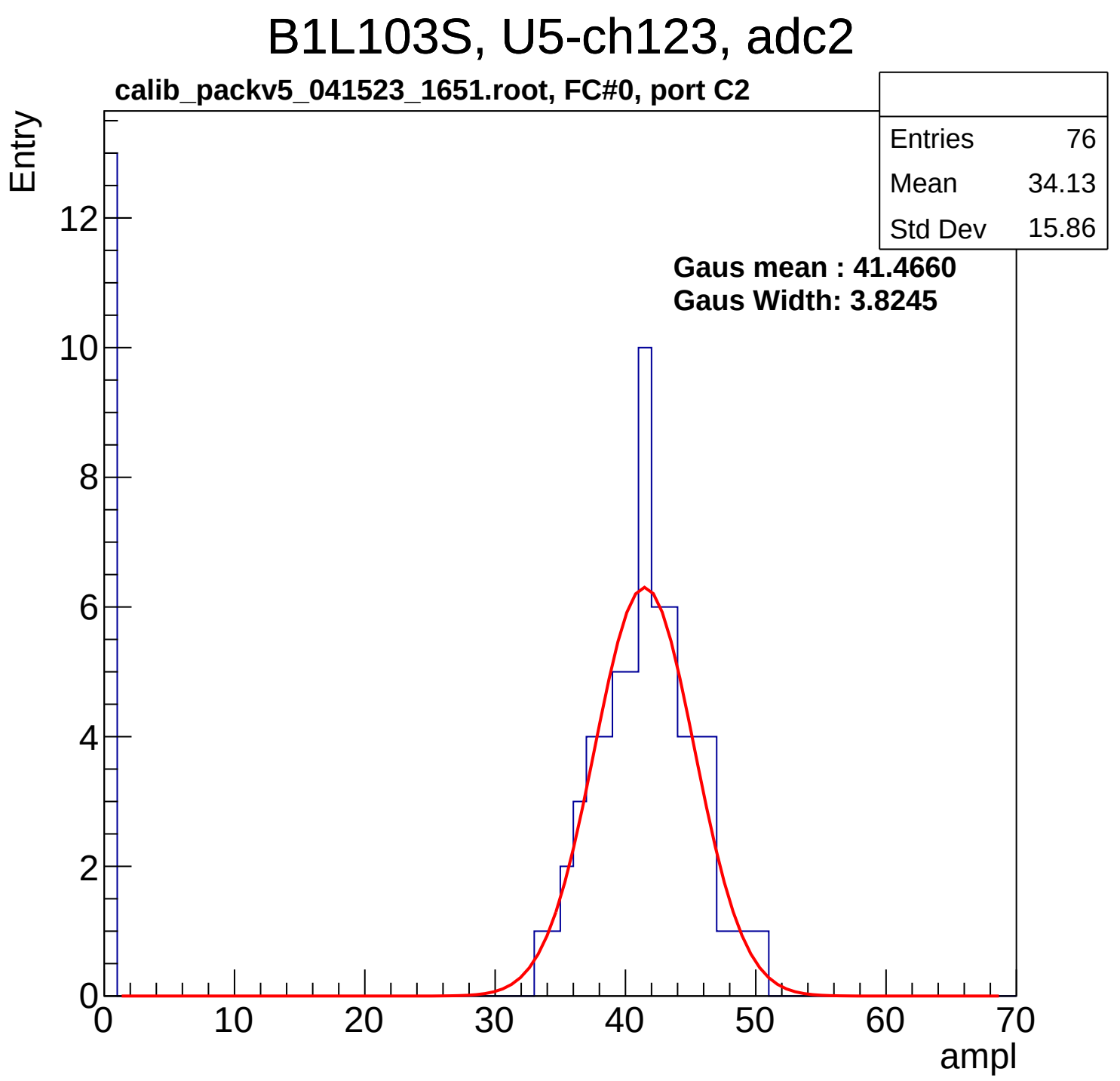
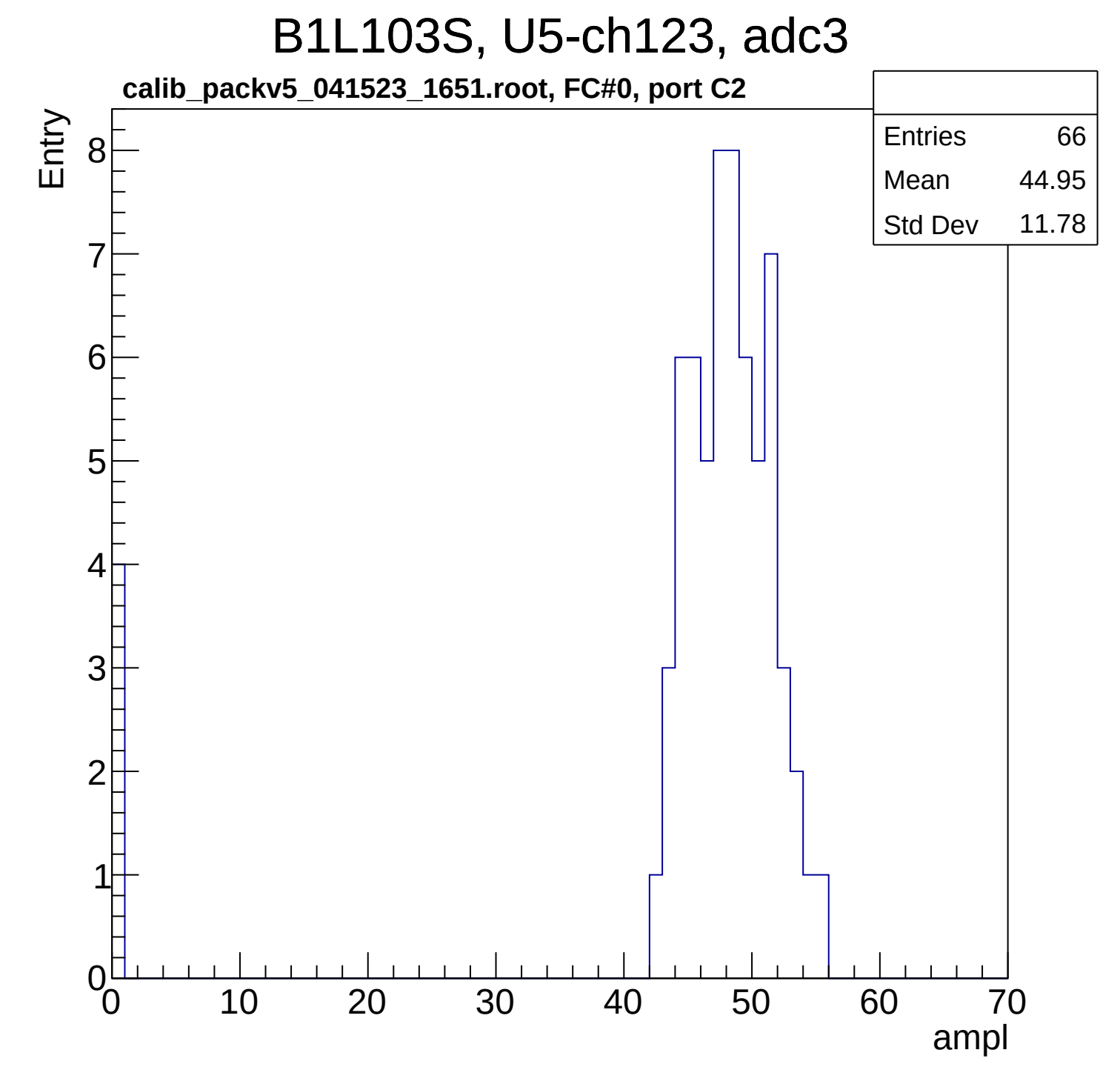
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U5-ch123, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 34.13
Std Dev 15.86
Gaus mean : 41.4660
Gaus Width: 3.8245
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U5-ch123, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 44.95
Std Dev 11.78
Entry
0
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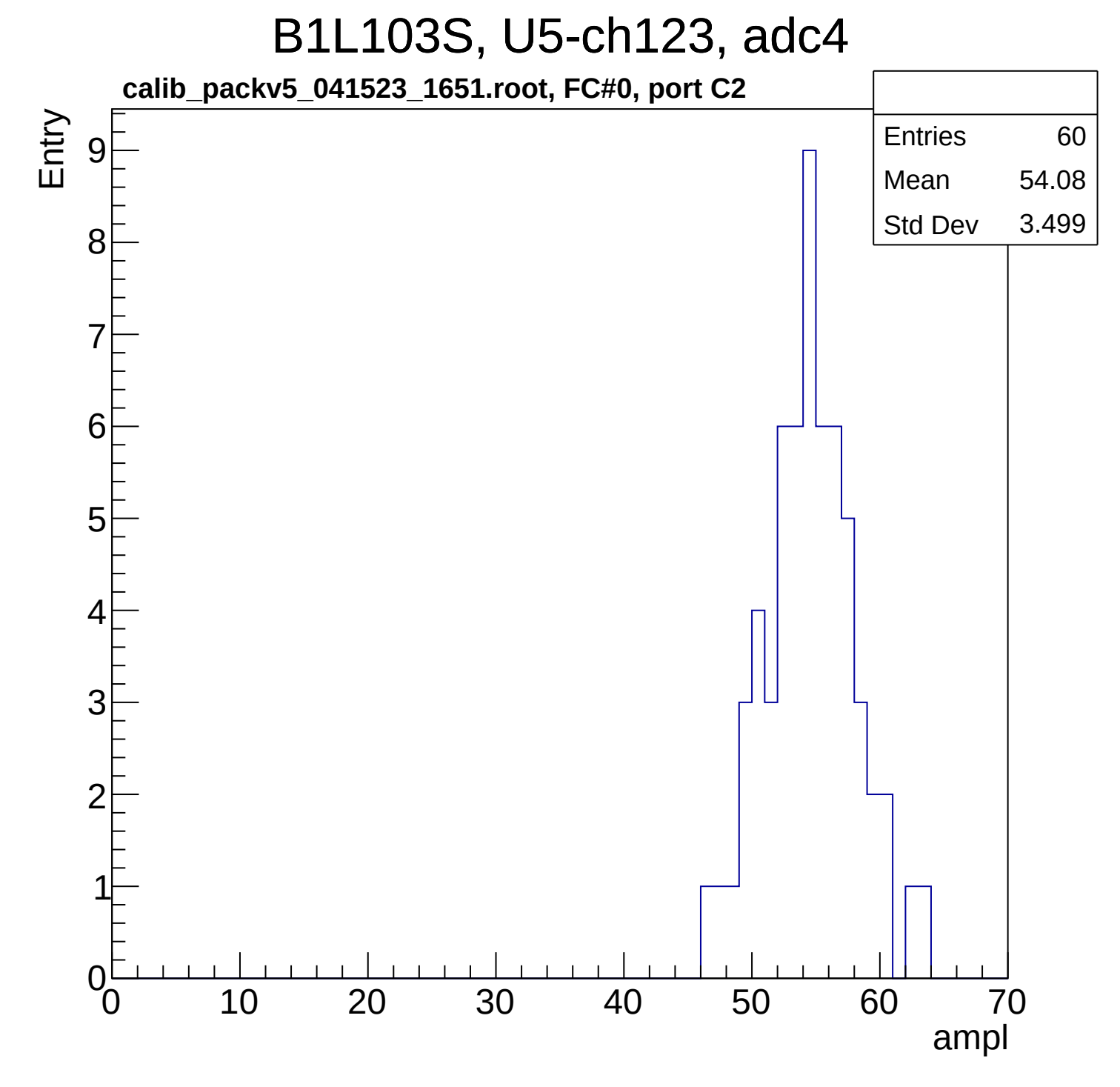
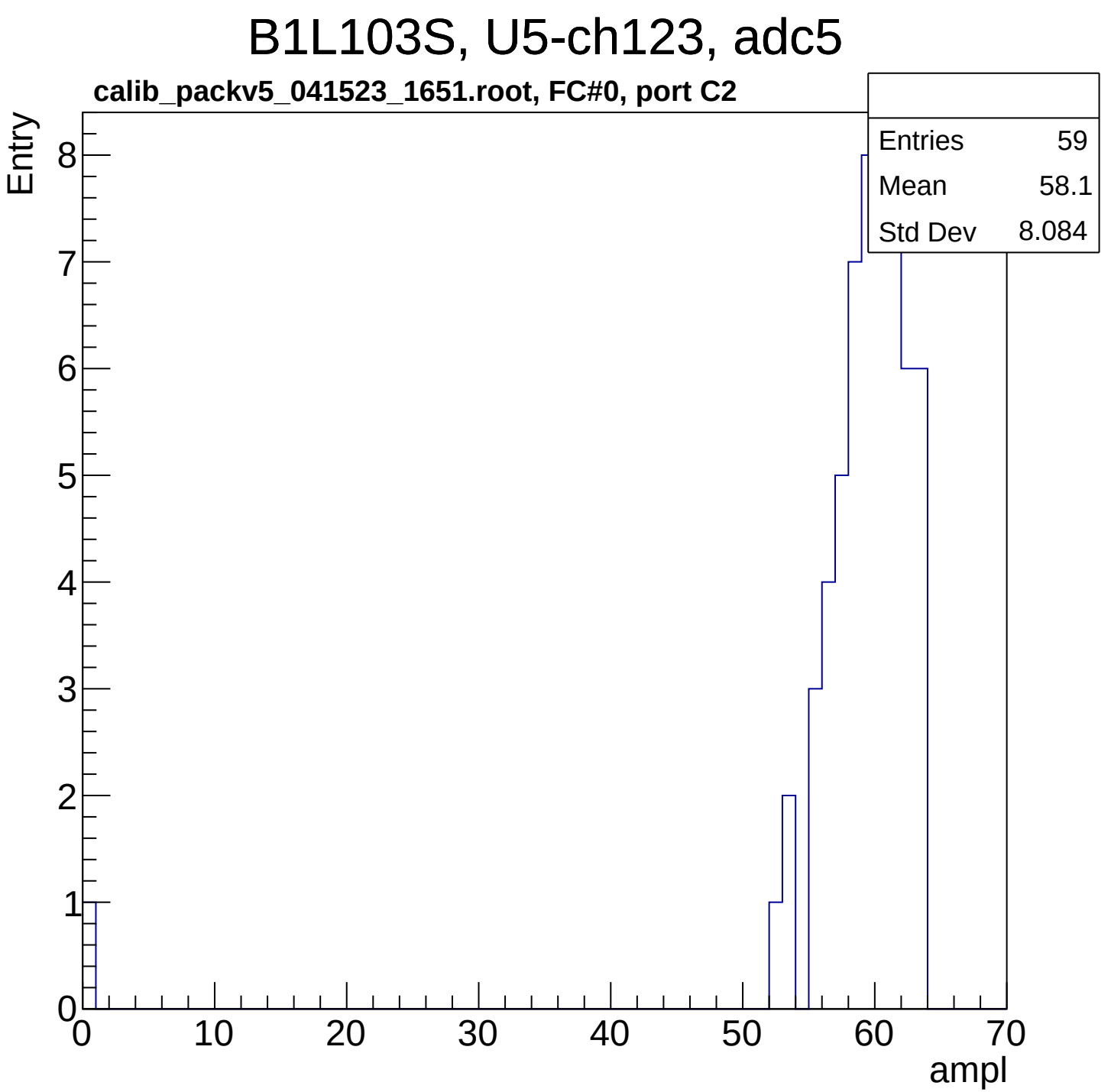
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch123, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 54.08
Std Dev 3.499
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U5-ch123, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 58.1
Std Dev 8.084
Entry
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2
3
4
5
6
7
8
0
10
20
30
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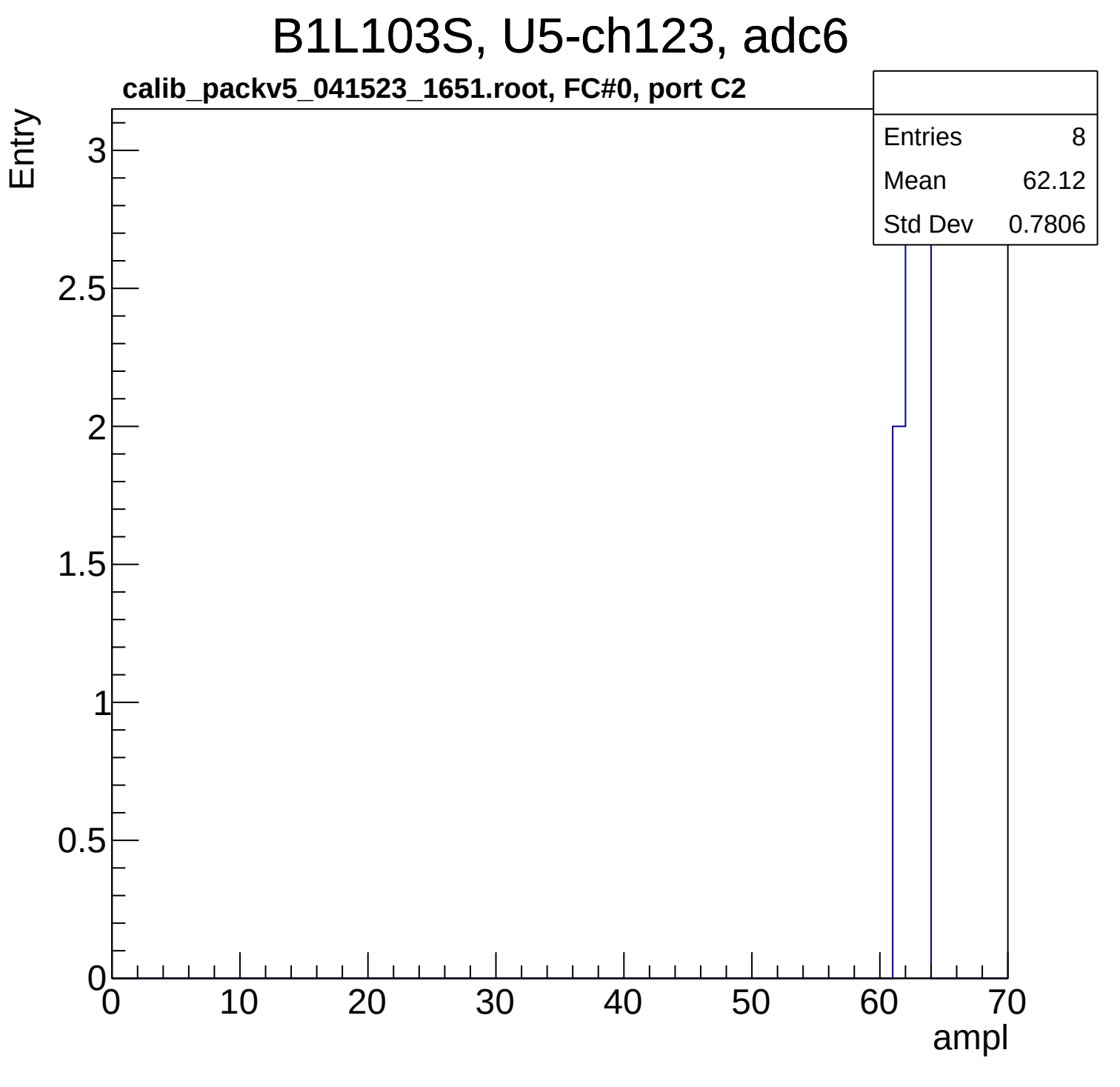
50
60
70
ampl


B1L103S, U5-ch123, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62.12
Std Dev 0.7806
Entry
ampl
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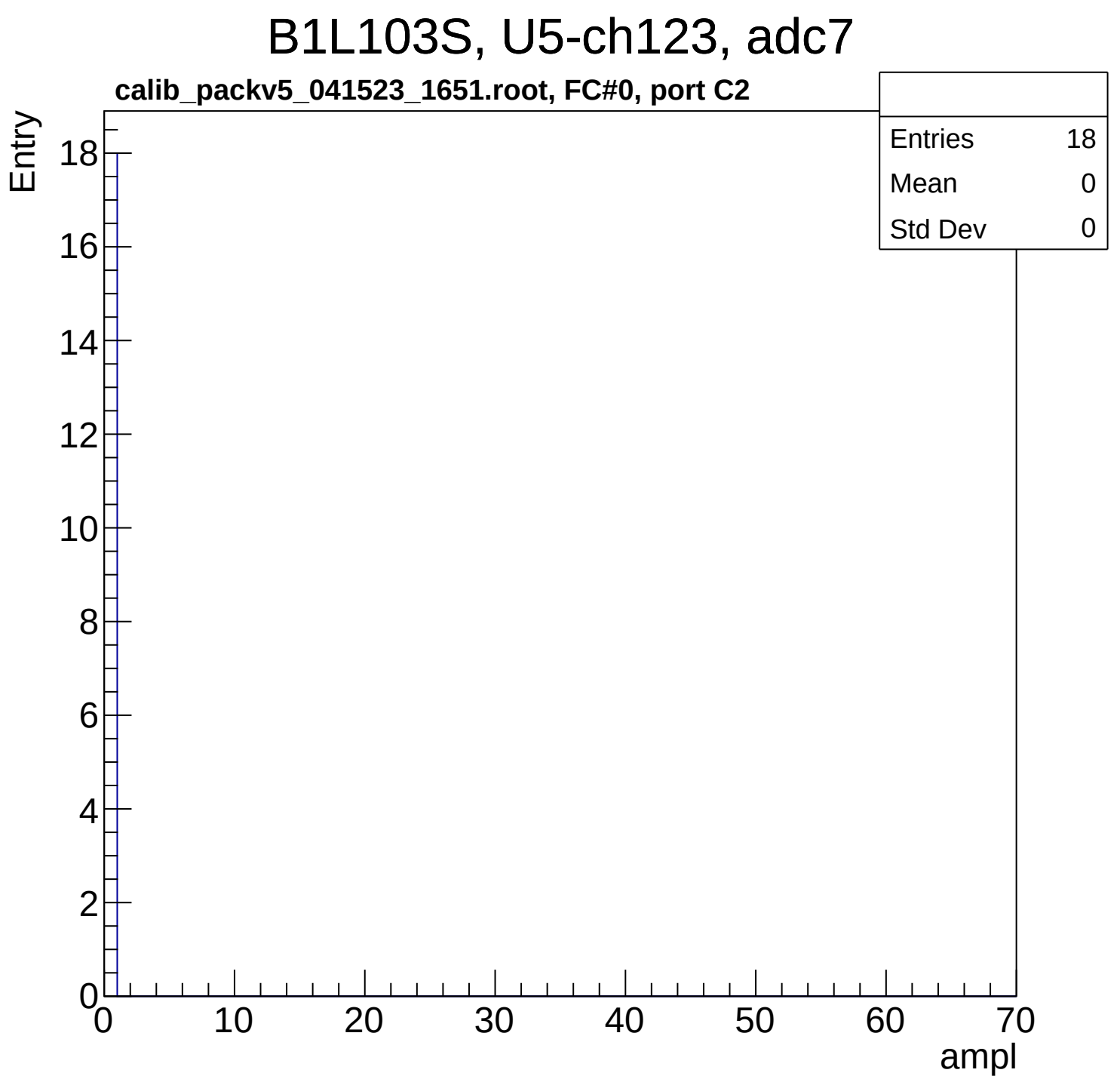
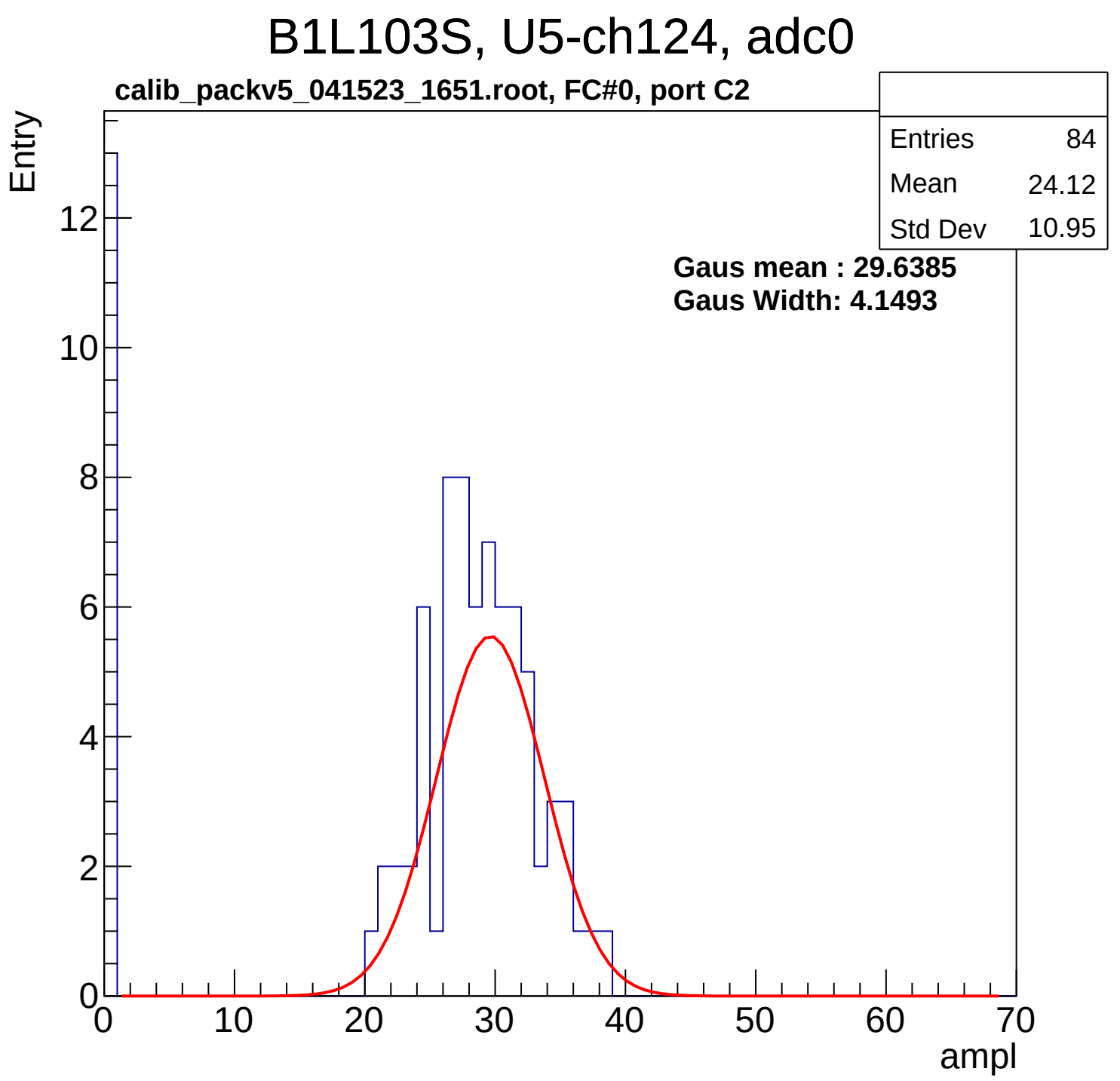
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U5-ch123, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U5-ch124, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 24.12
Std Dev 10.95
Gaus mean : 29.6385
Gaus Width: 4.1493
Entry
ampl
0
2
4
6
8
10
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0
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60
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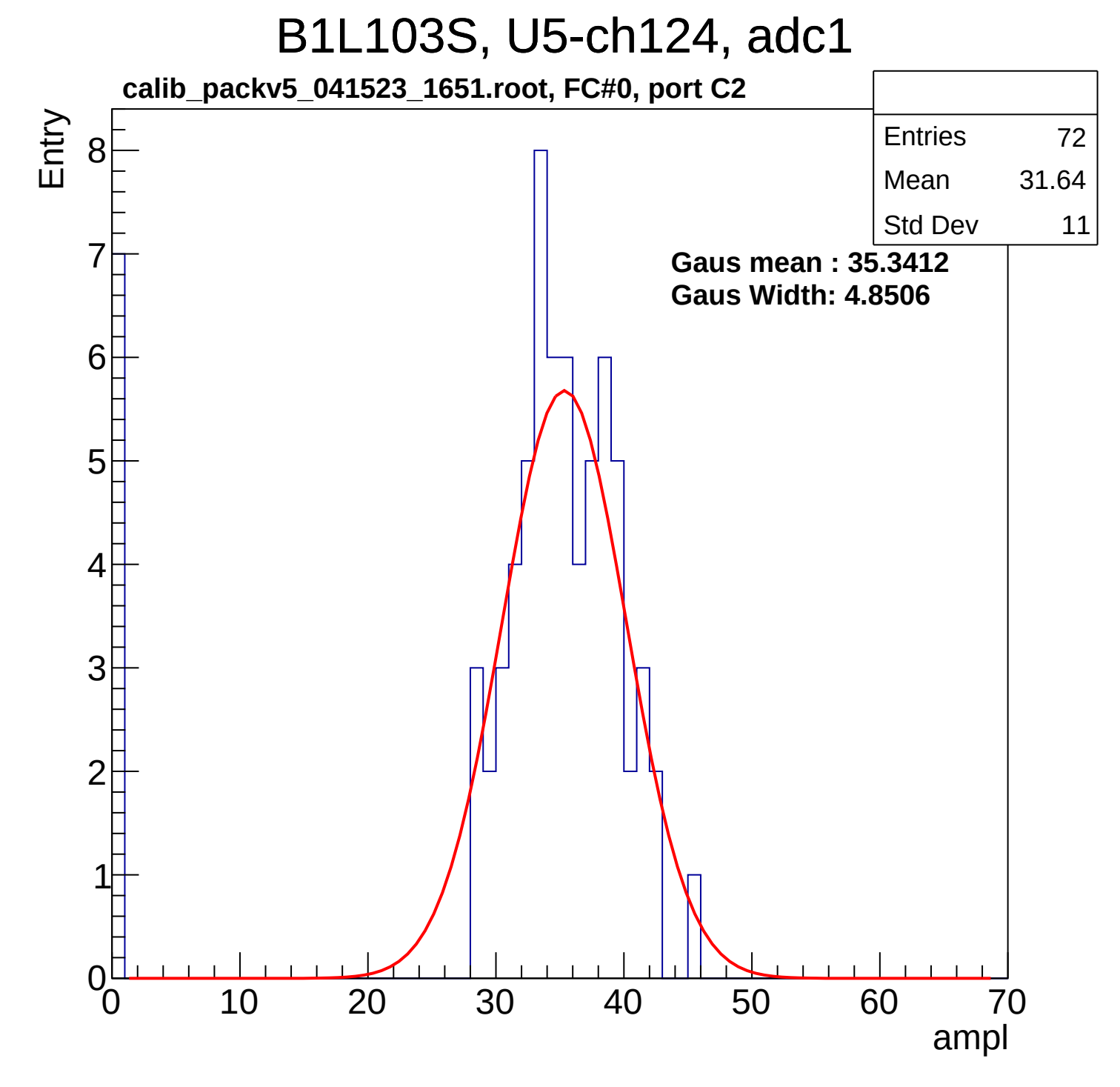
B1L103S, U5-ch124, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 31.64
Std Dev 11
Gaus mean : 35.3412
Gaus Width: 4.8506
Entry
ampl
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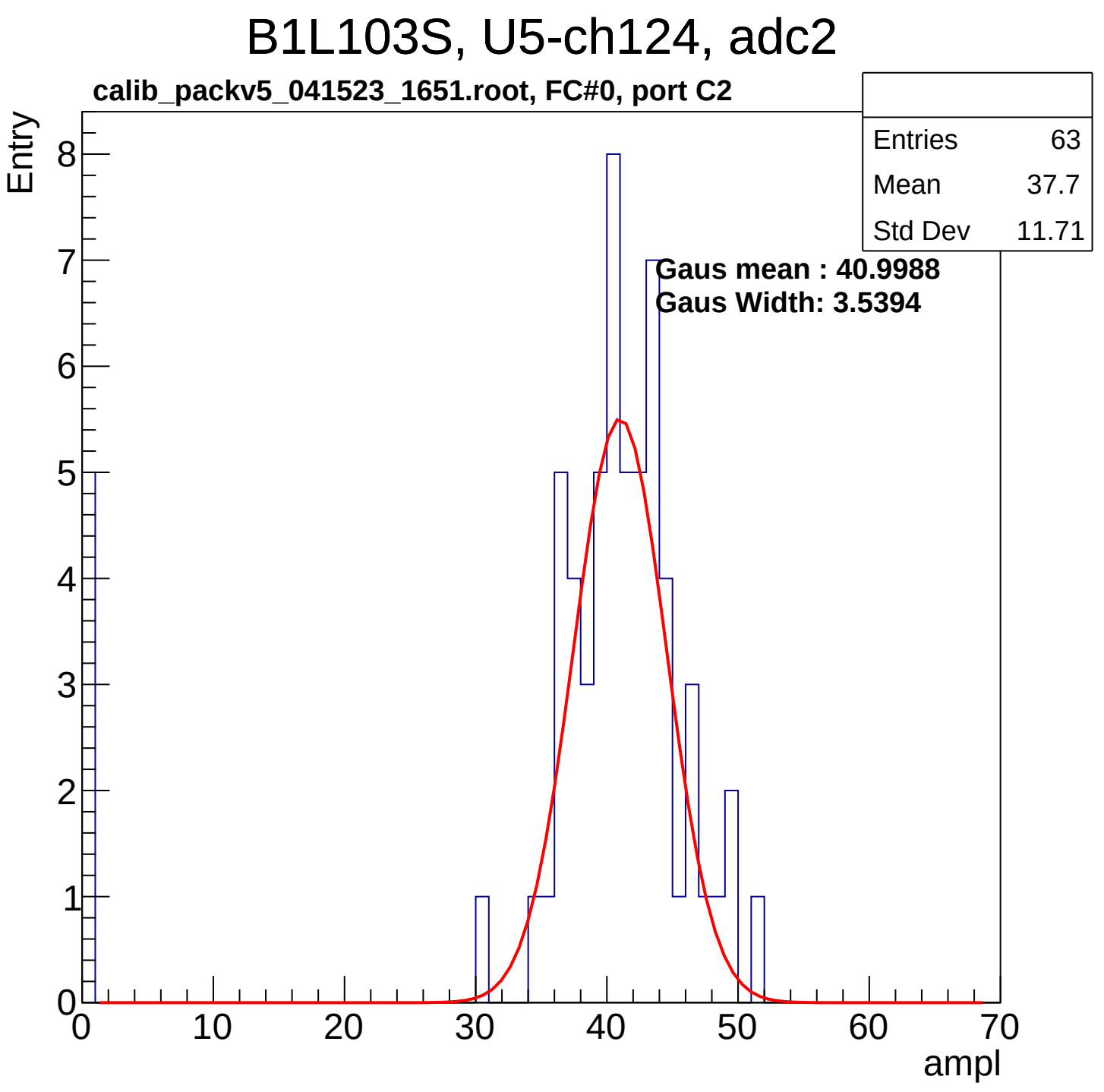
B1L103S, U5-ch124, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 37.7
Std Dev 11.71
Gaus mean : 40.9988
Gaus Width: 3.5394
Entry
ampl
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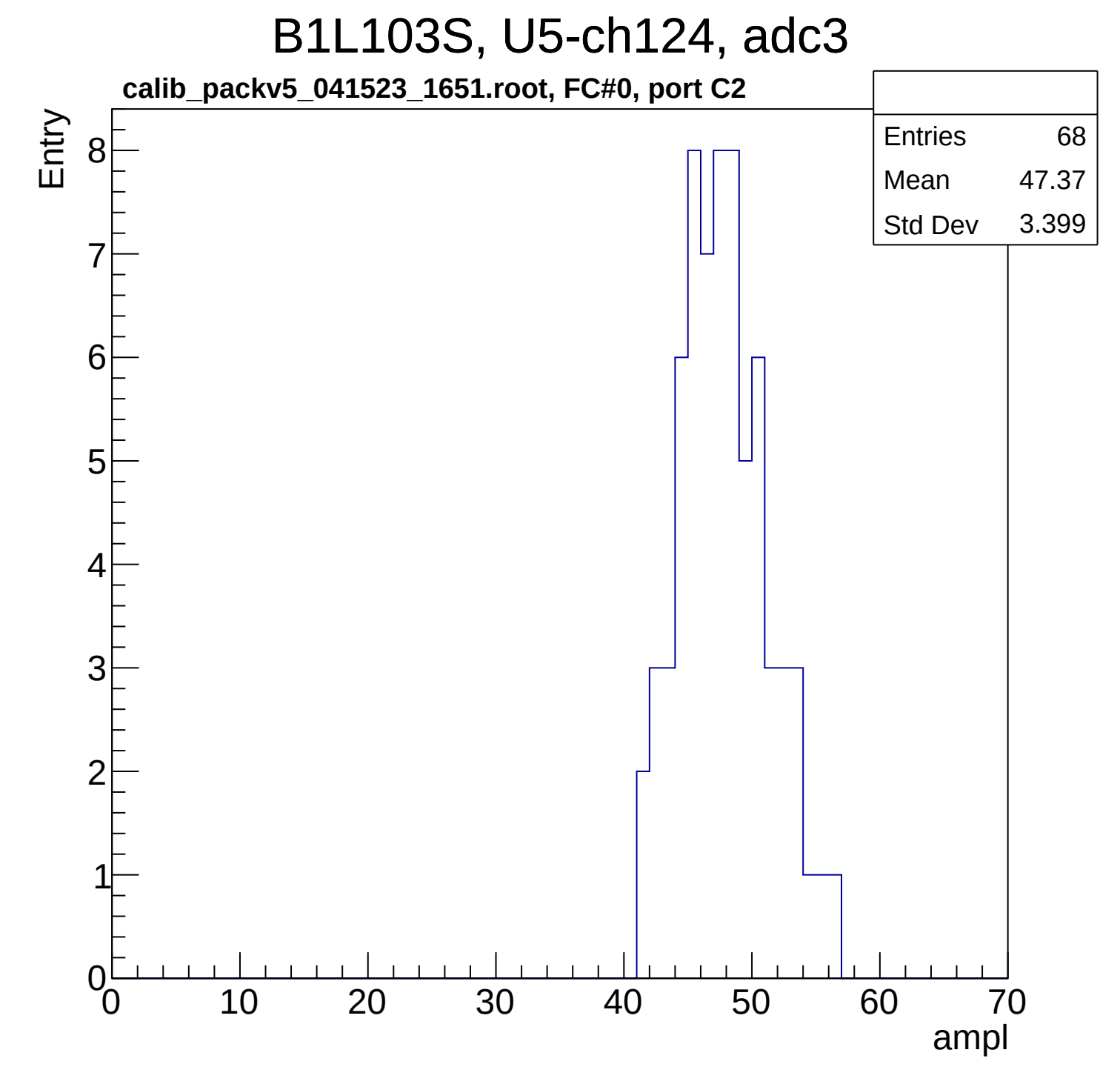
B1L103S, U5-ch124, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 47.37
Std Dev 3.399
Entry
ampl
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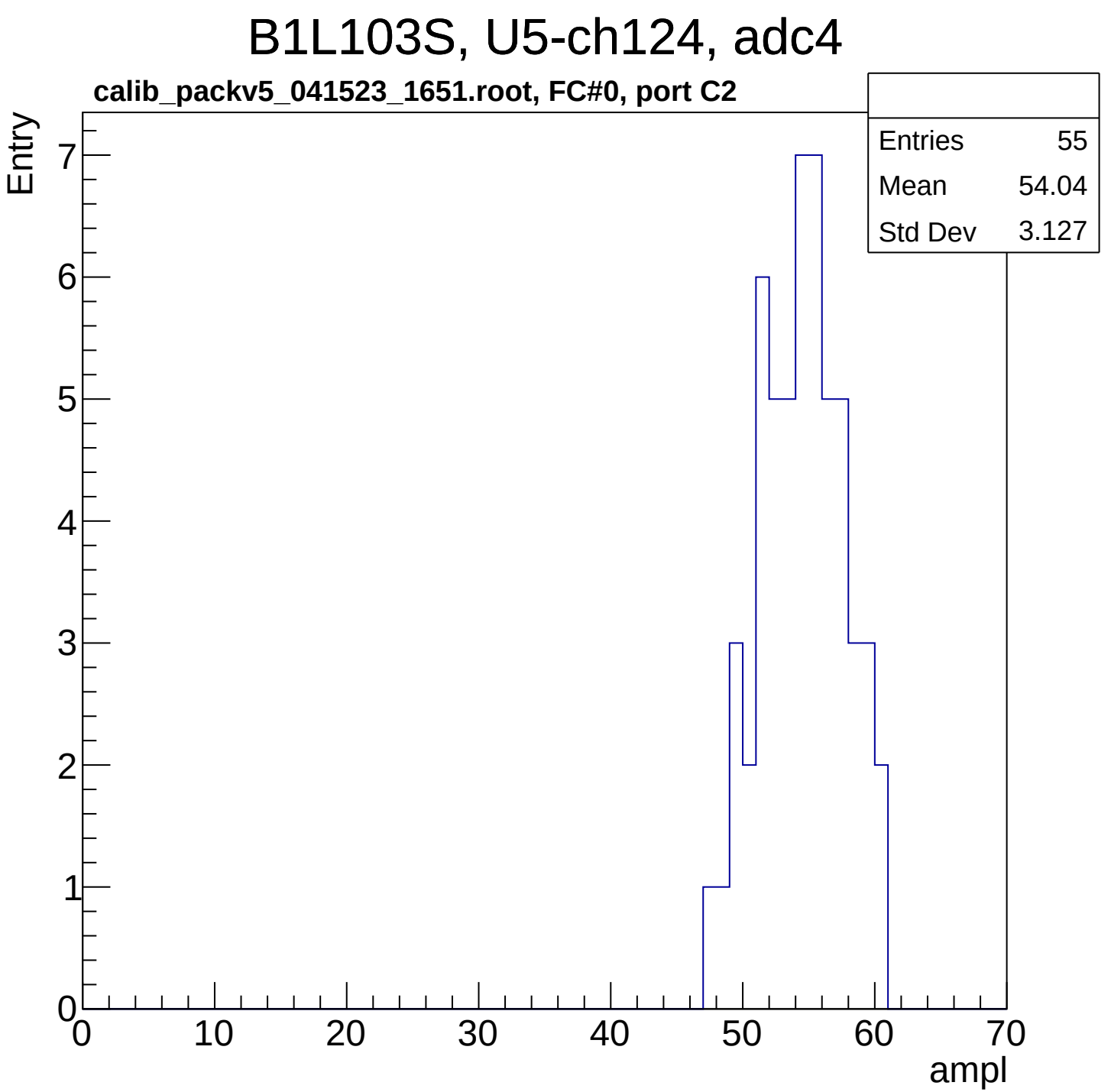
B1L103S, U5-ch124, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 54.04
Std Dev 3.127
Entry
ampl
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3
4
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0
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40
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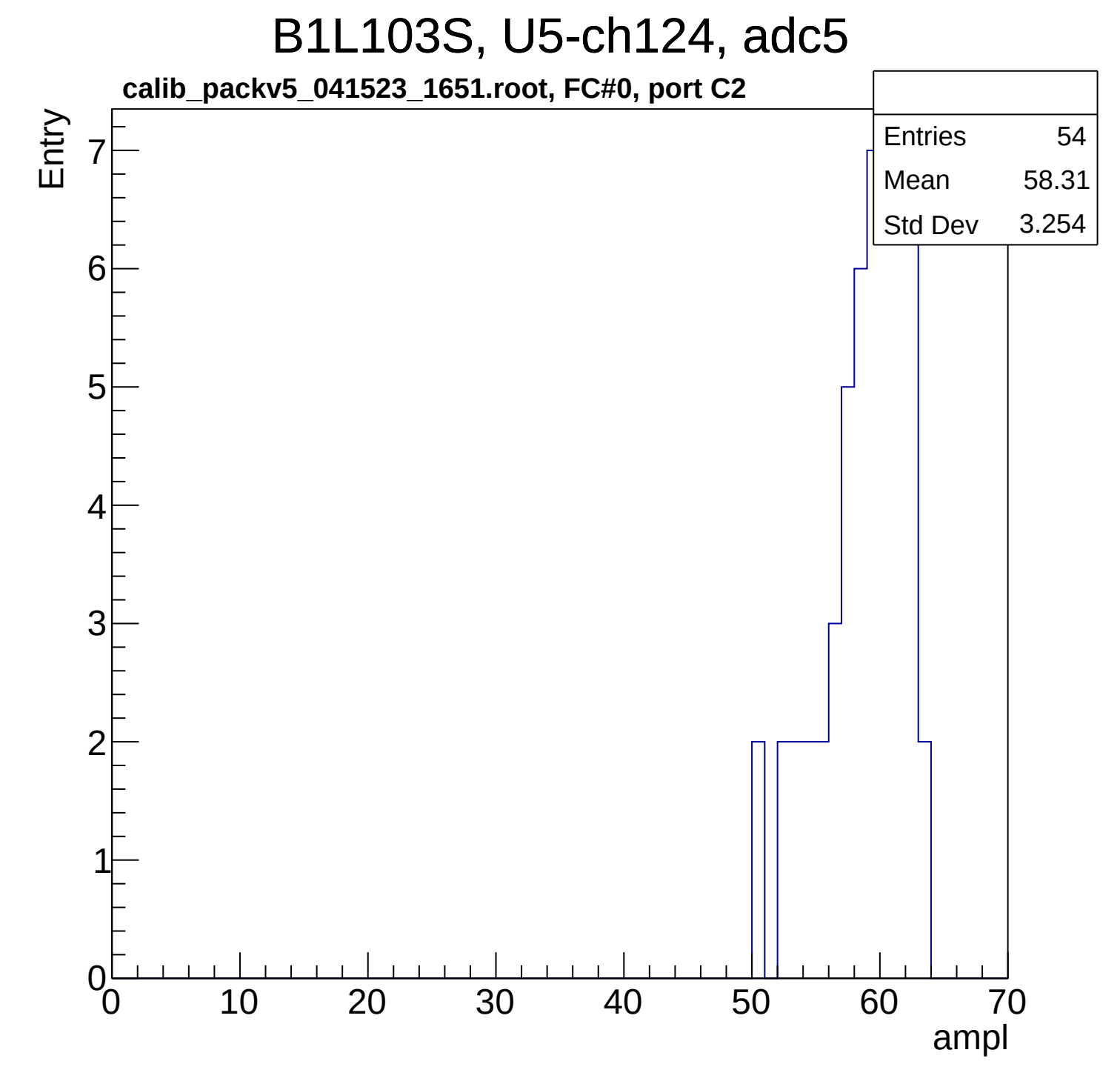
B1L103S, U5-ch124, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.31
Std Dev 3.254
Entry
ampl
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1
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3
4
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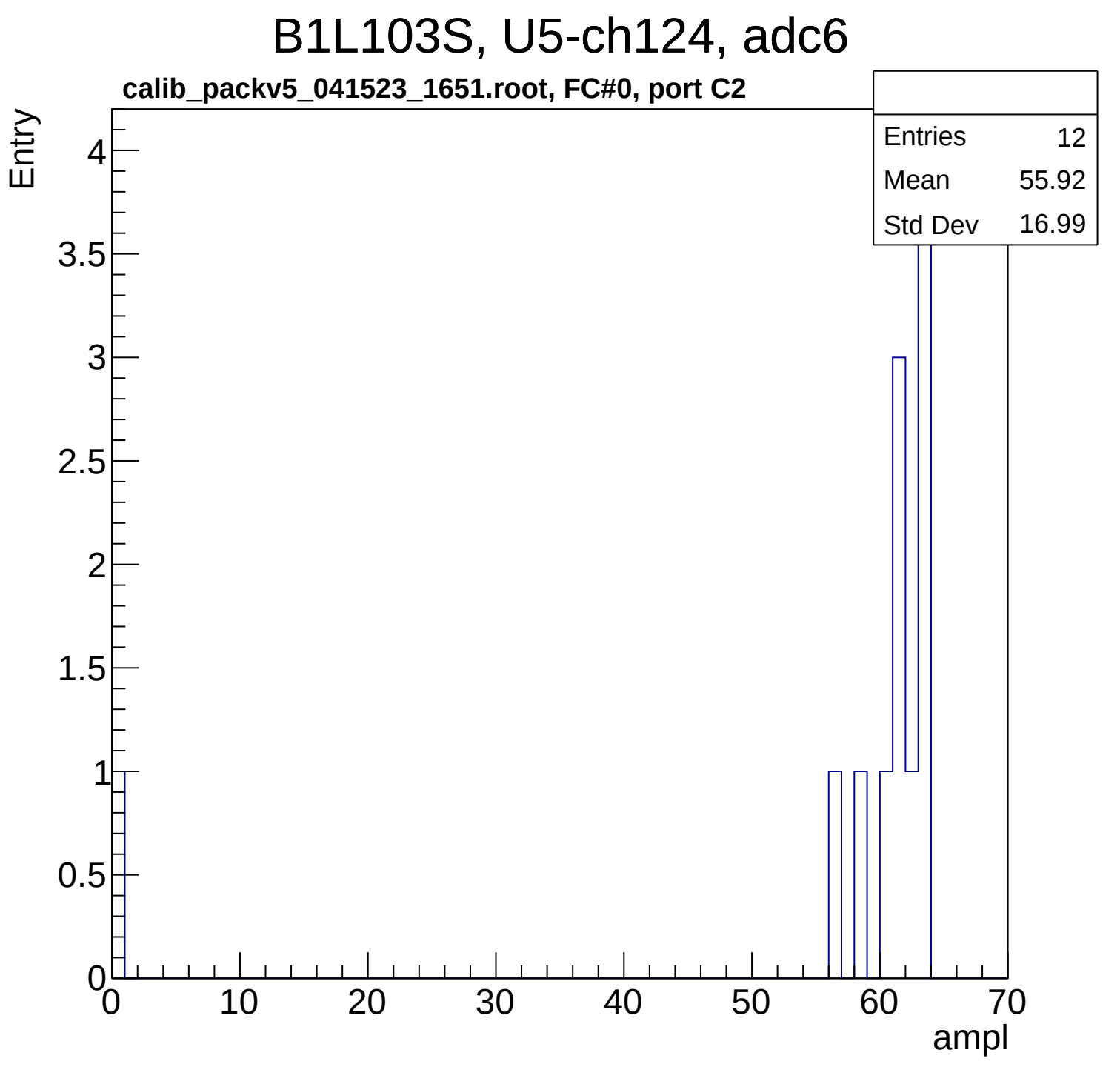
B1L103S, U5-ch124, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 55.92
Std Dev 16.99
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
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60
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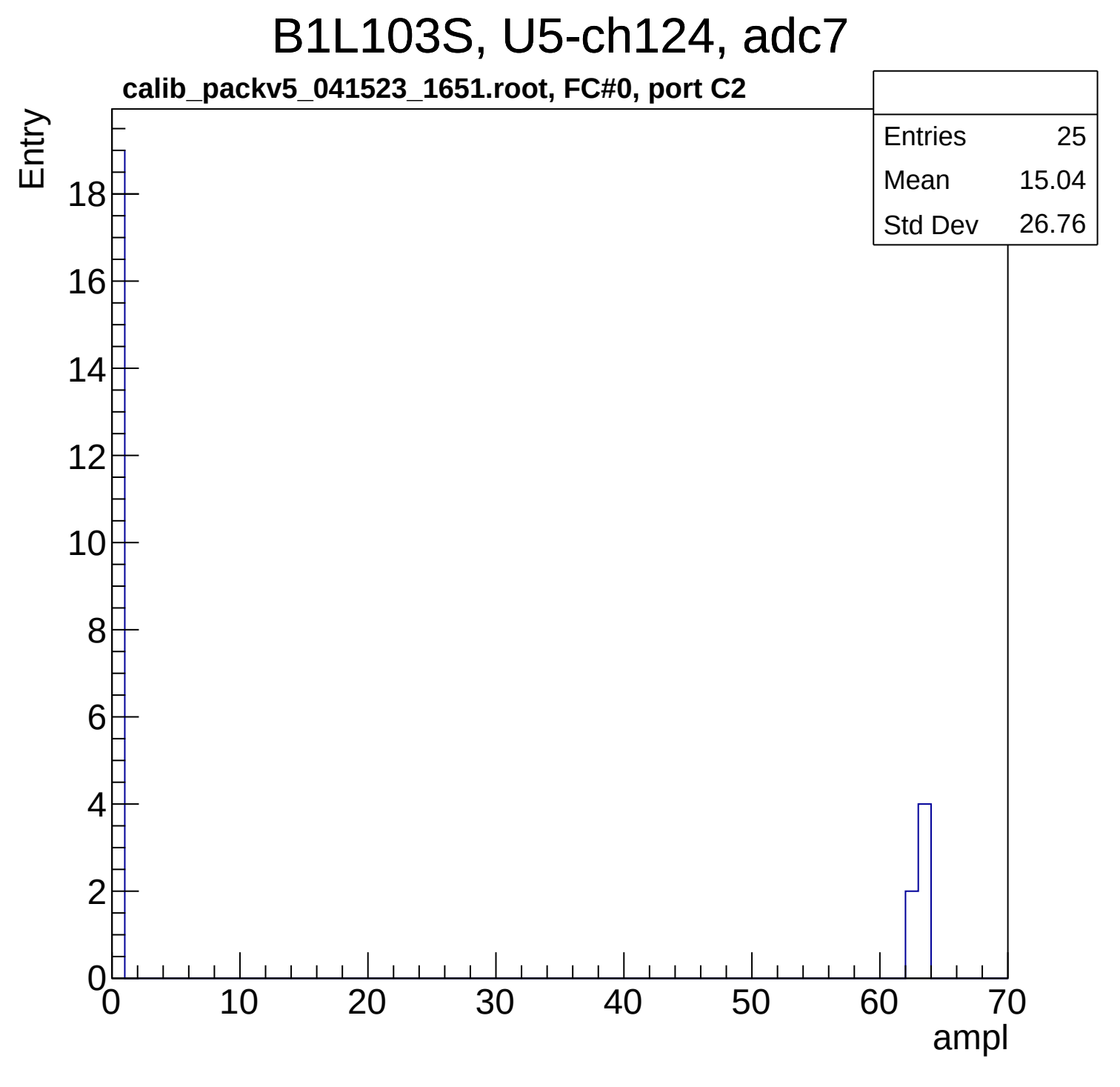
B1L103S, U5-ch124, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 15.04
Std Dev 26.76
Entry
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6
8
10
12
14
16
18
0
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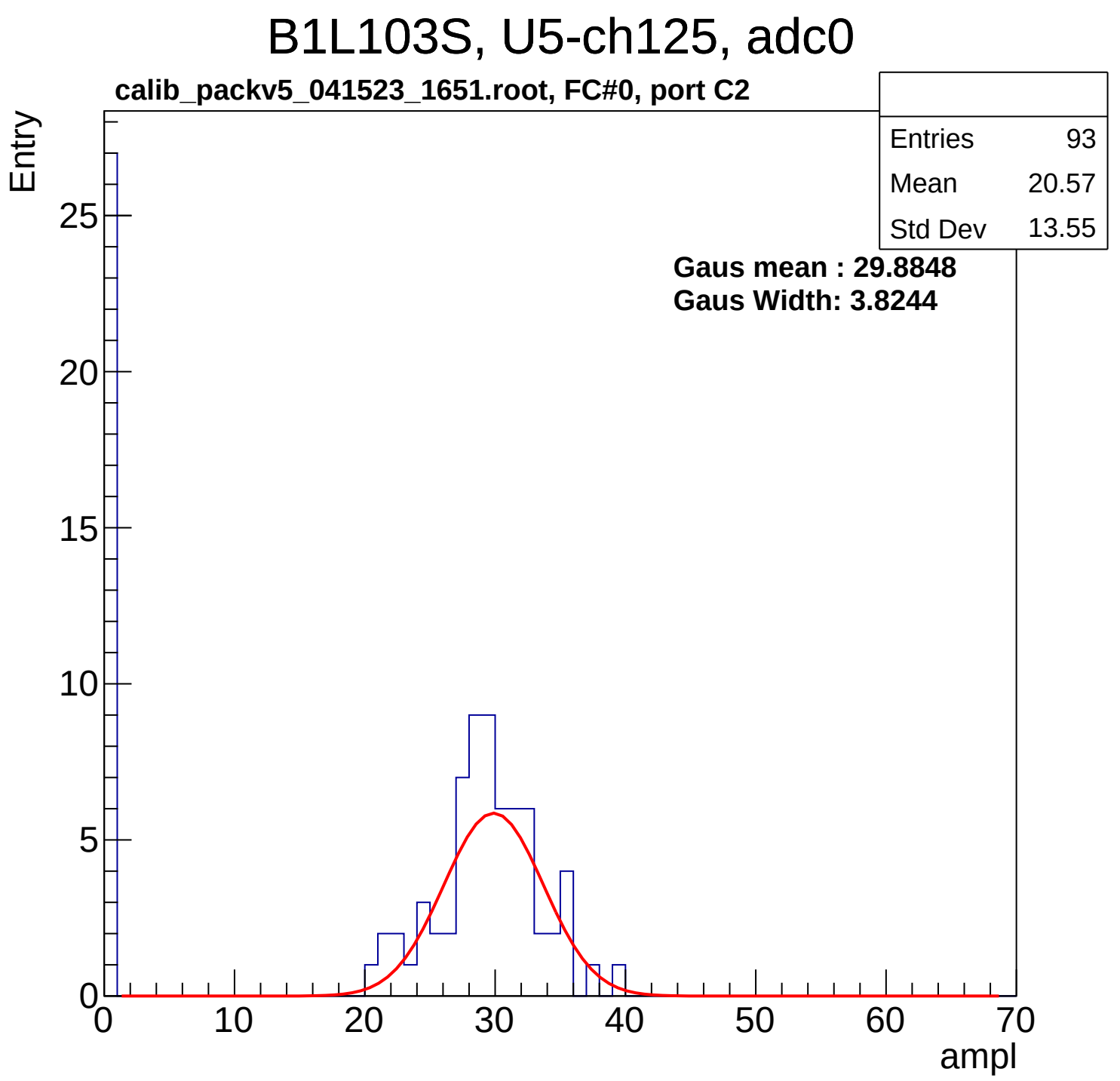
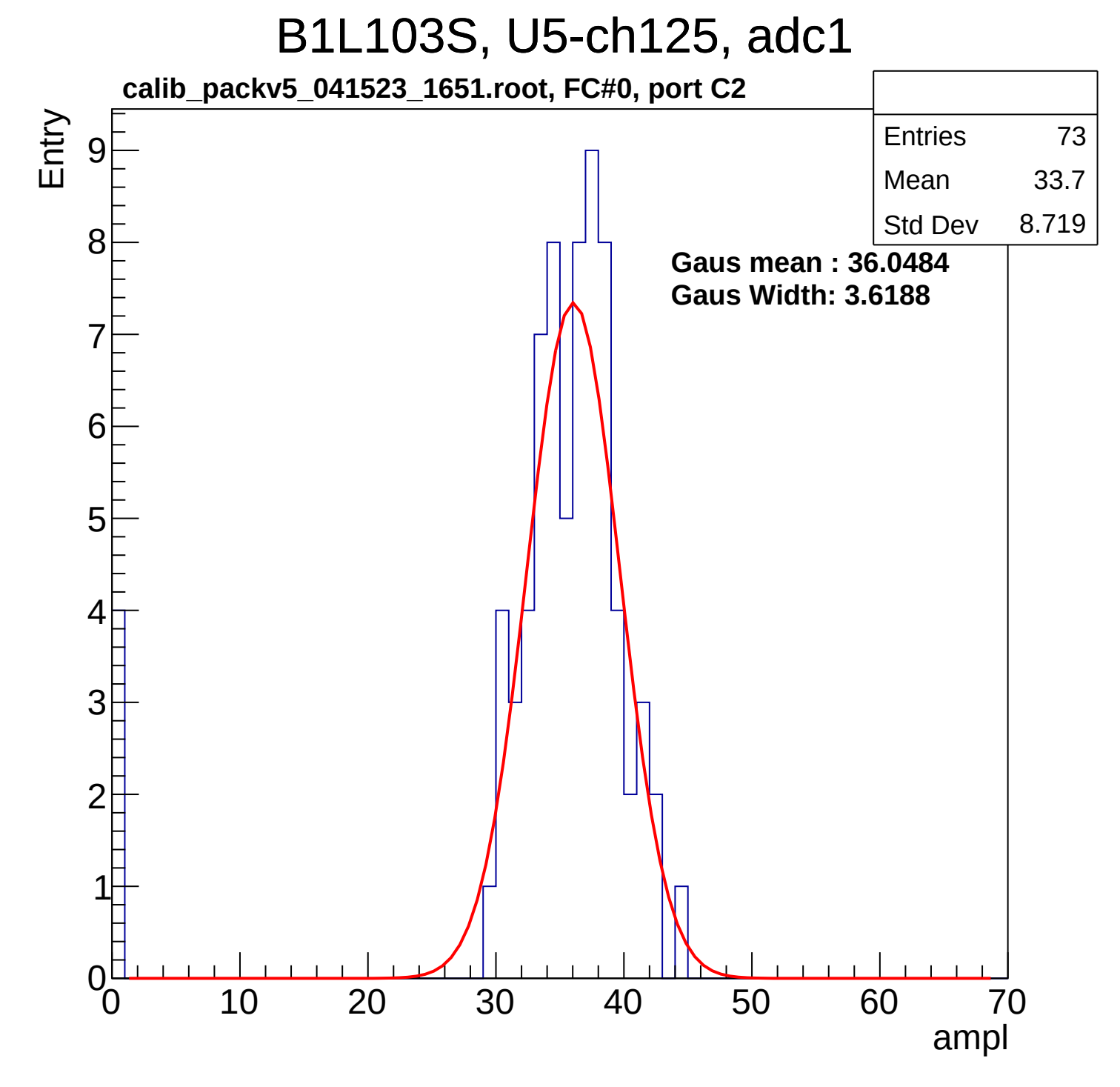
50
60
70
ampl


B1L103S, U5-ch125, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 20.57
Std Dev 13.55
Gaus mean : 29.8848
Gaus Width: 3.8244
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U5-ch125, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 33.7
Std Dev 8.719
Gaus mean : 36.0484
Gaus Width: 3.6188
Entry
ampl
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3
4
5
6
7
8
9
0
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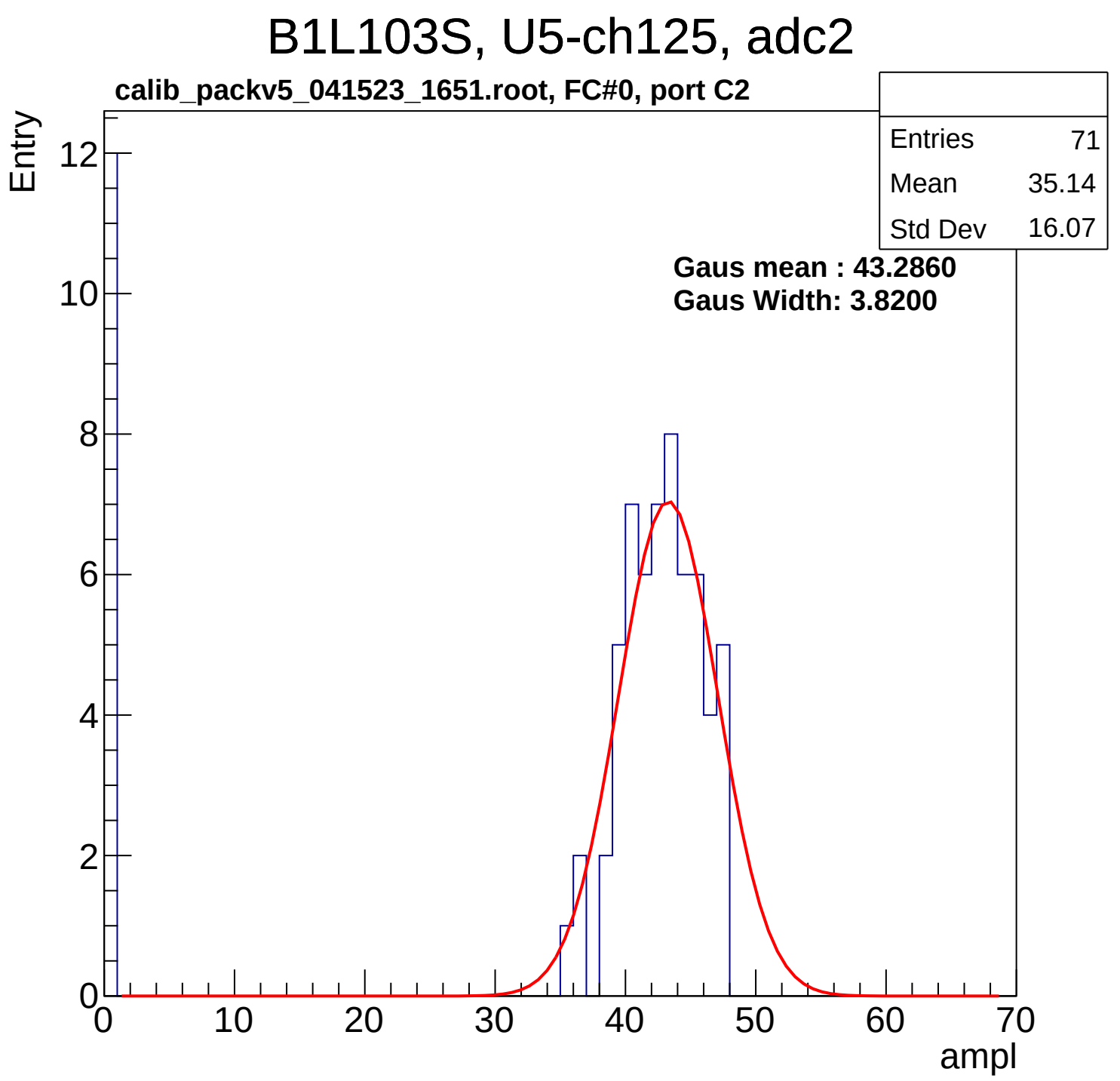
B1L103S, U5-ch125, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 35.14
Std Dev 16.07
Gaus mean : 43.2860
Gaus Width: 3.8200
Entry
ampl
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4
6
8
10
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0
10
20
30
40
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60
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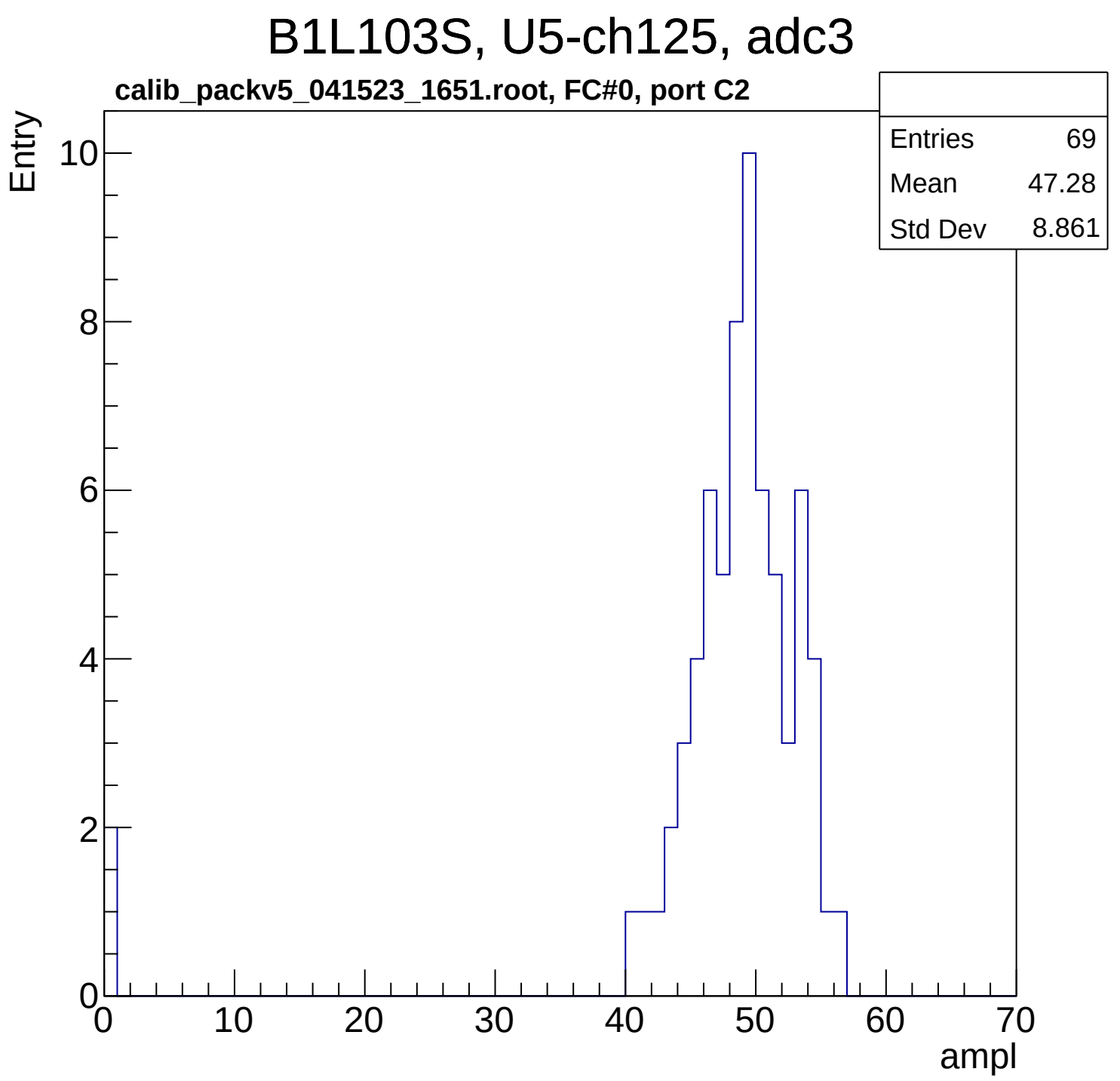
B1L103S, U5-ch125, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 47.28
Std Dev 8.861
Entry
ampl
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0
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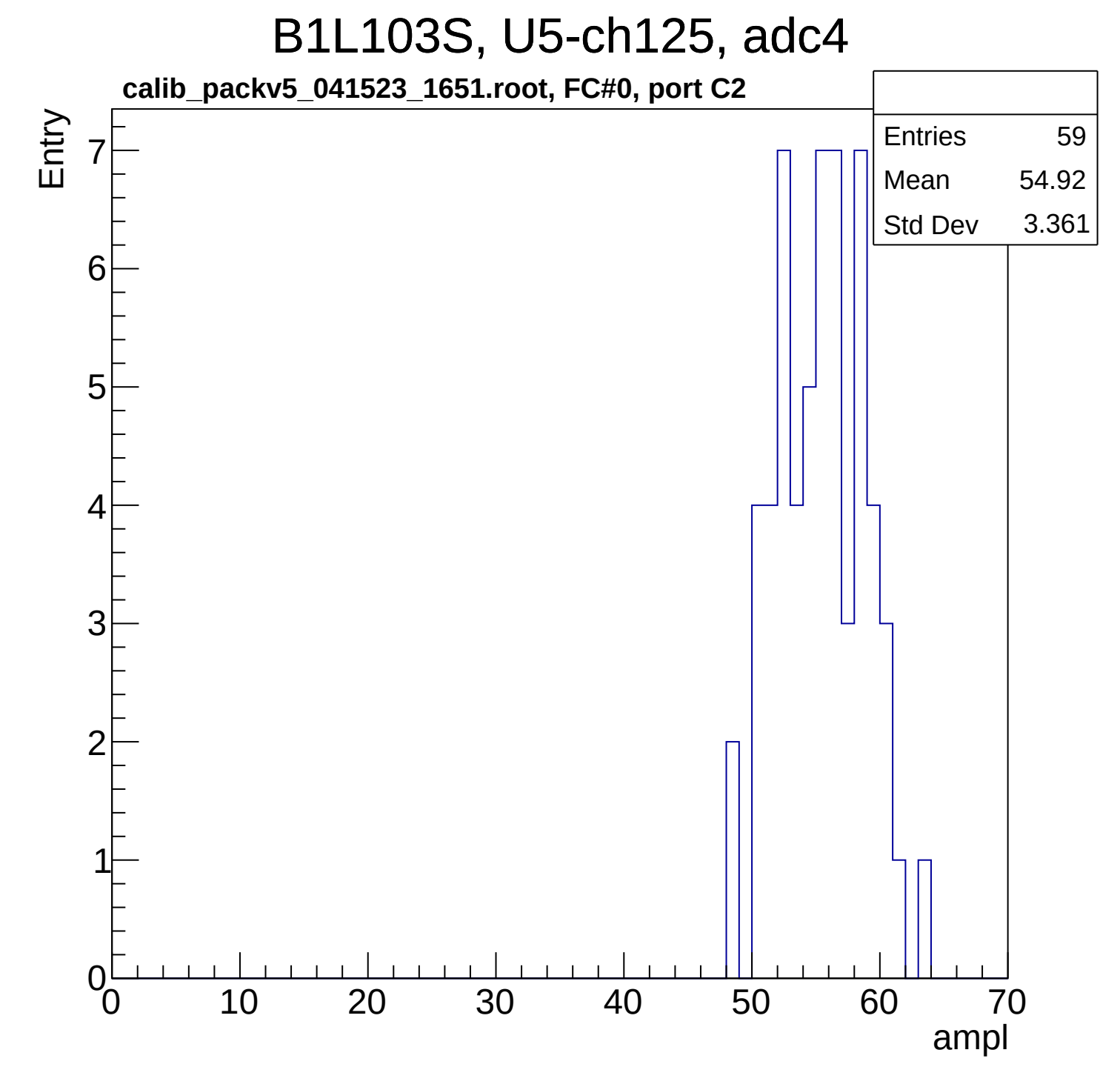
B1L103S, U5-ch125, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.92
Std Dev 3.361
Entry
ampl
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2
3
4
5
6
7
0
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20
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60
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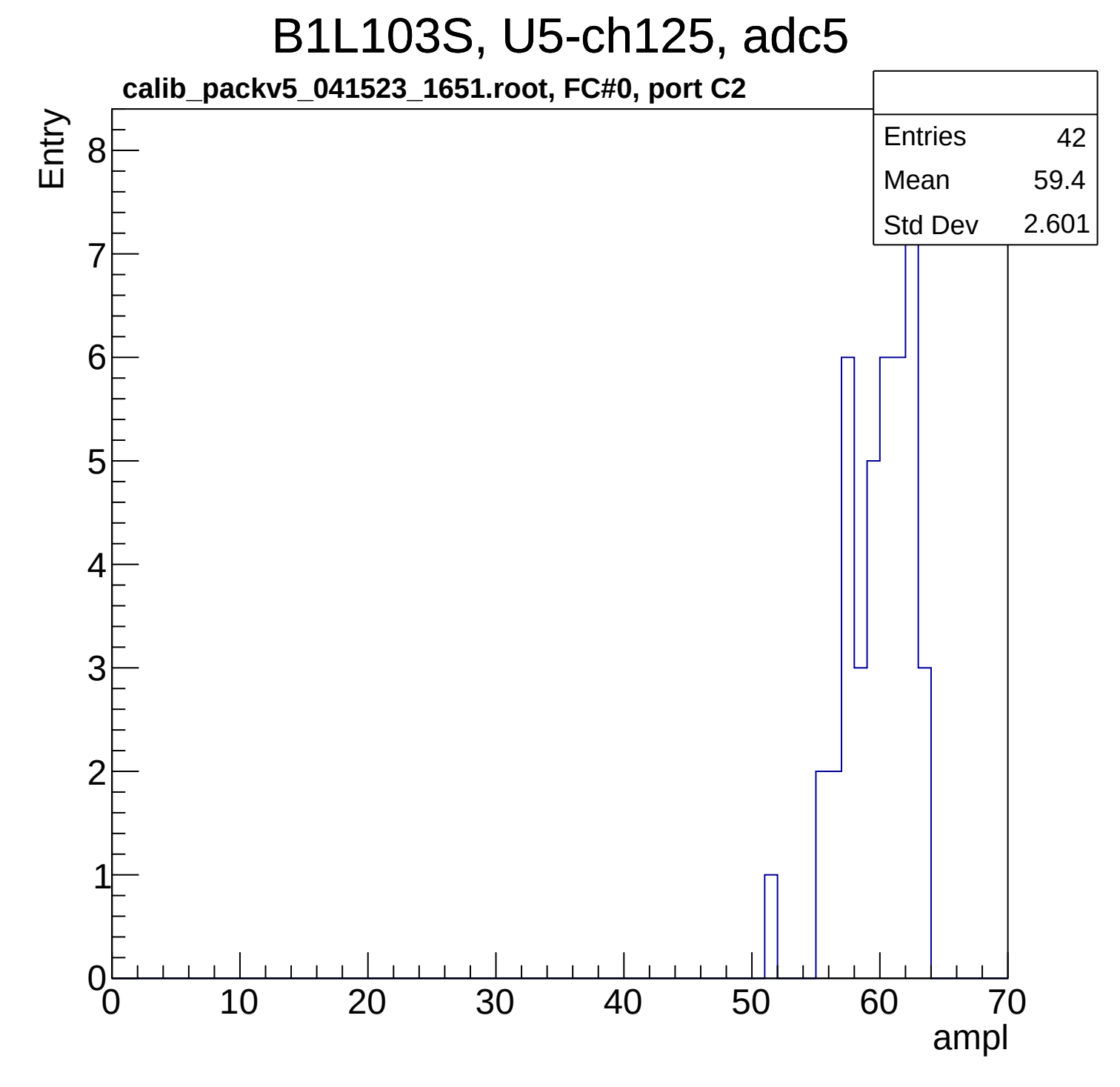
B1L103S, U5-ch125, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 59.4
Std Dev 2.601
Entry
ampl
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2
3
4
5
6
7
8
0
10
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60
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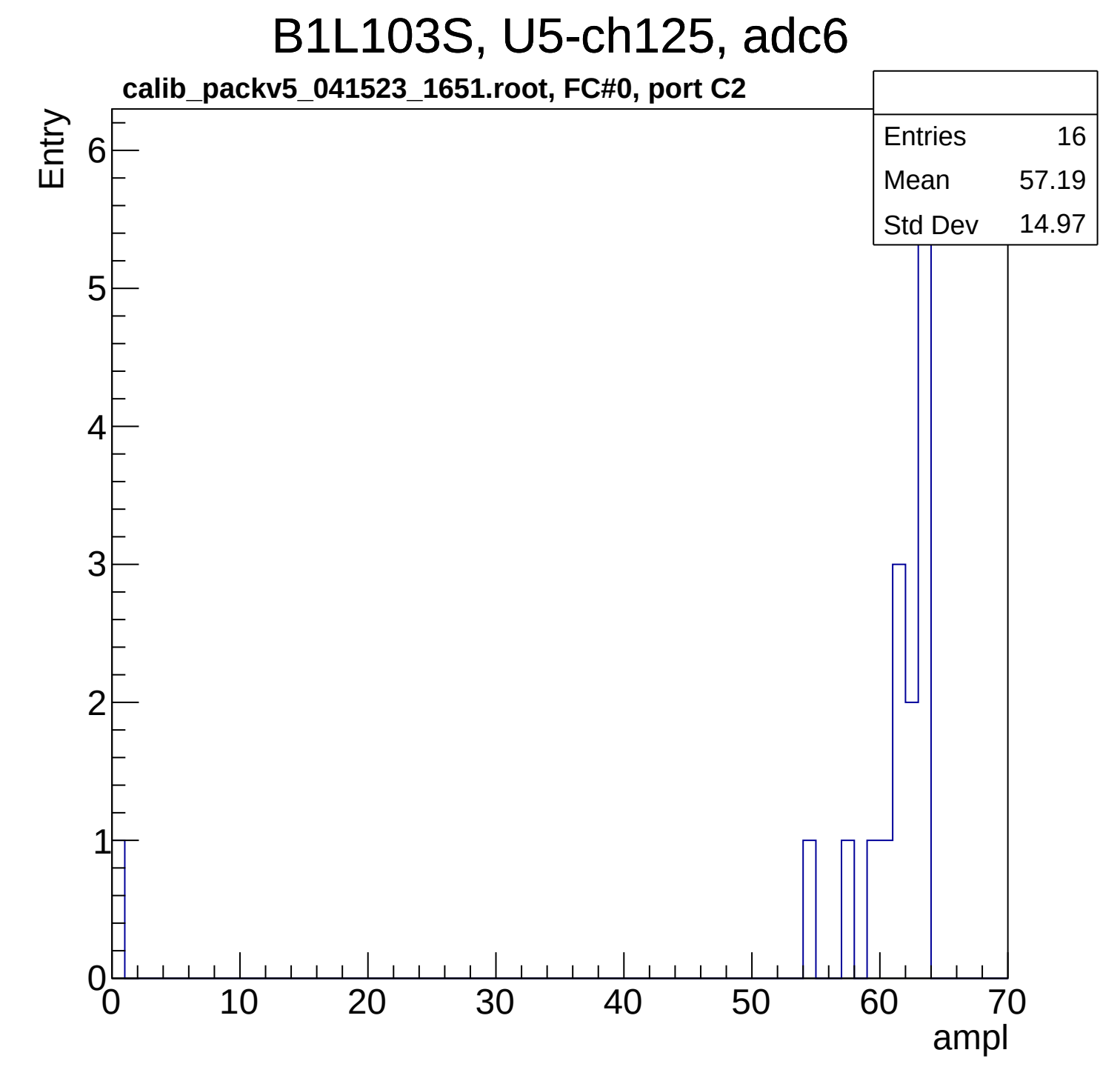
B1L103S, U5-ch125, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.19
Std Dev 14.97
Entry
0
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2
3
4
5
6
0
10
20
30
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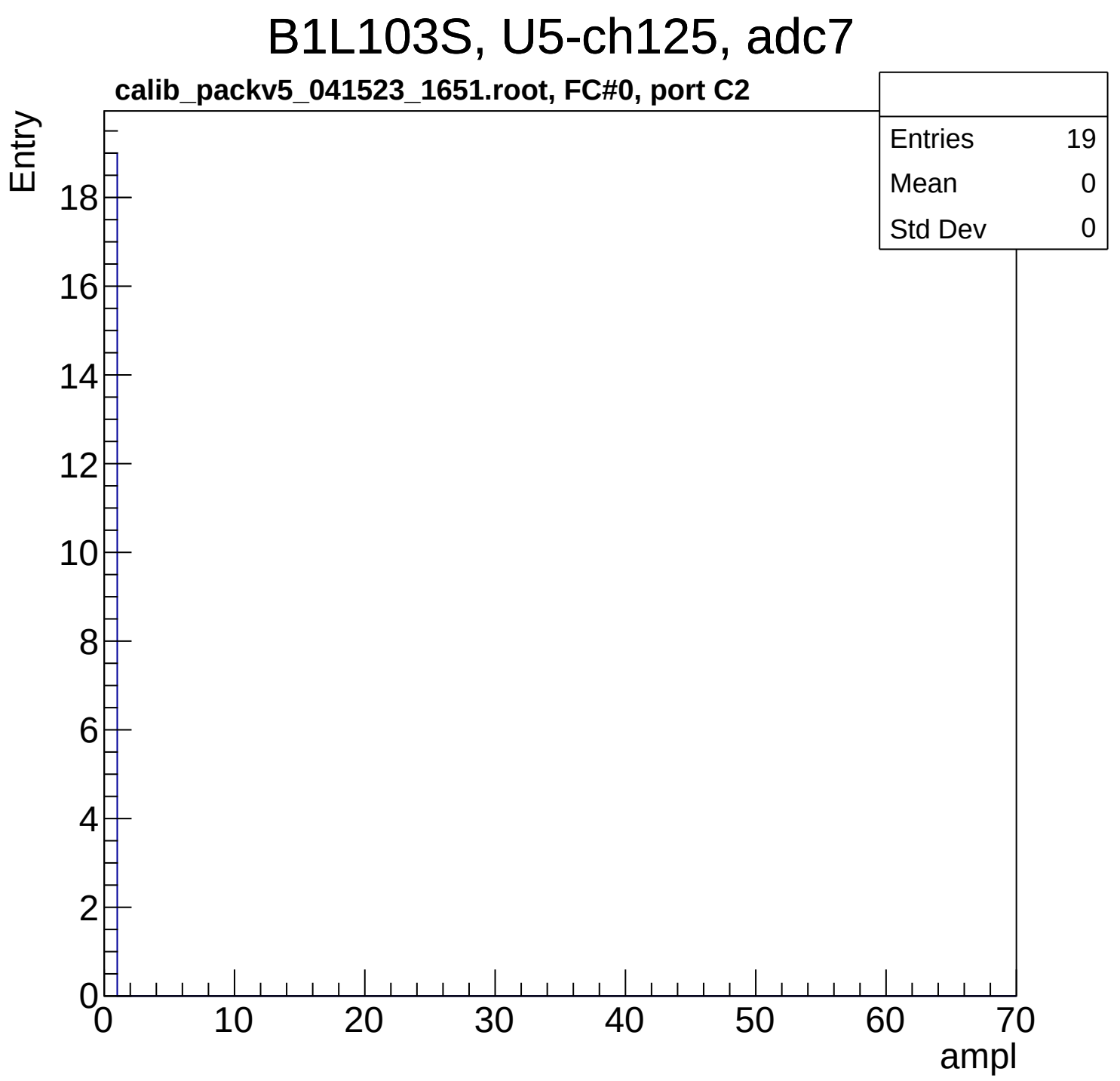
50
60
70
ampl


B1L103S, U5-ch125, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
0
10
20
30
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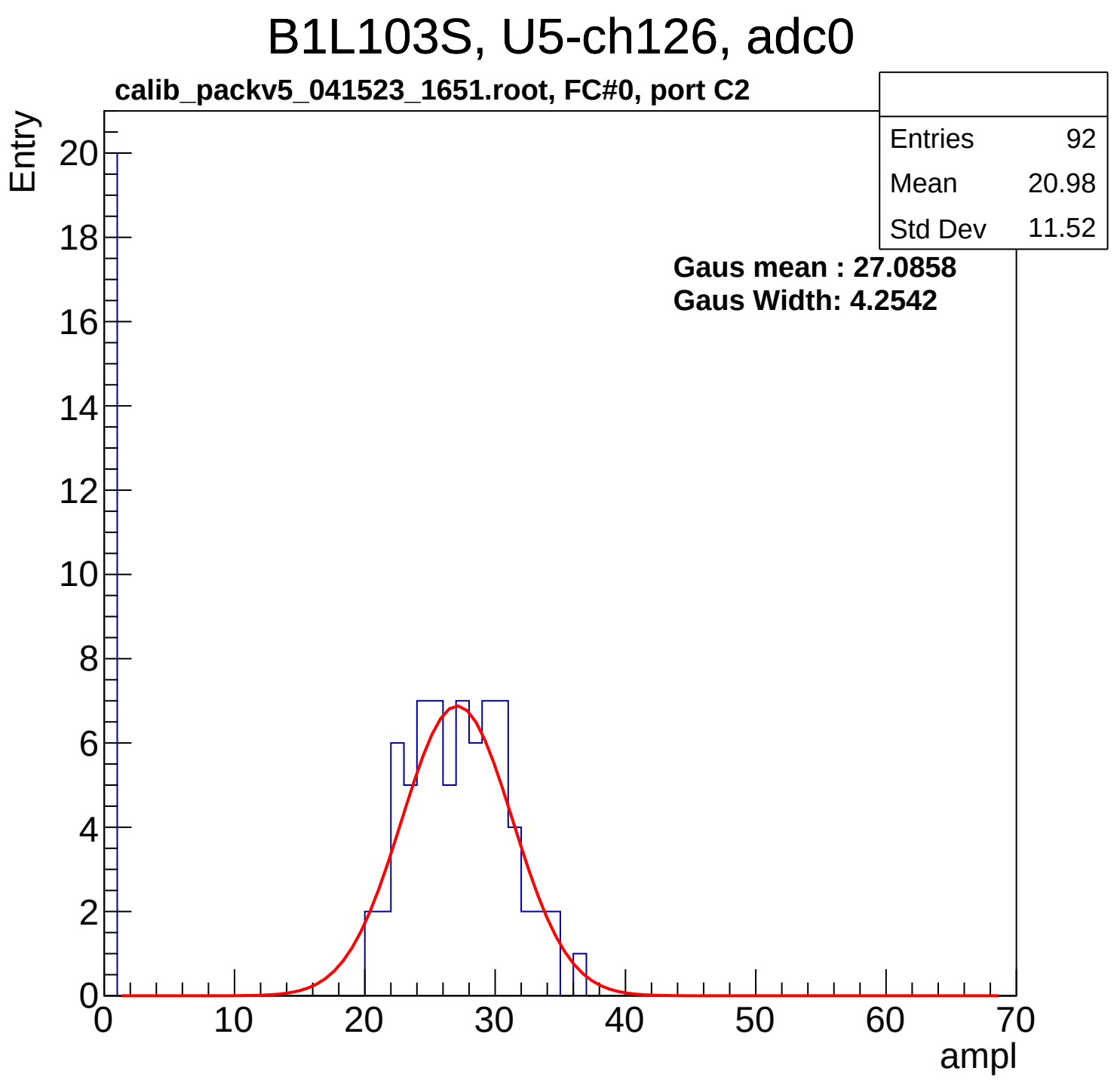
50
60
70
ampl


B1L103S, U5-ch126, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 20.98
Std Dev 11.52
Gaus mean : 27.0858
Gaus Width: 4.2542
Entry
ampl
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6
8
10
12
14
16
18
20
0
10
20
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40
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60
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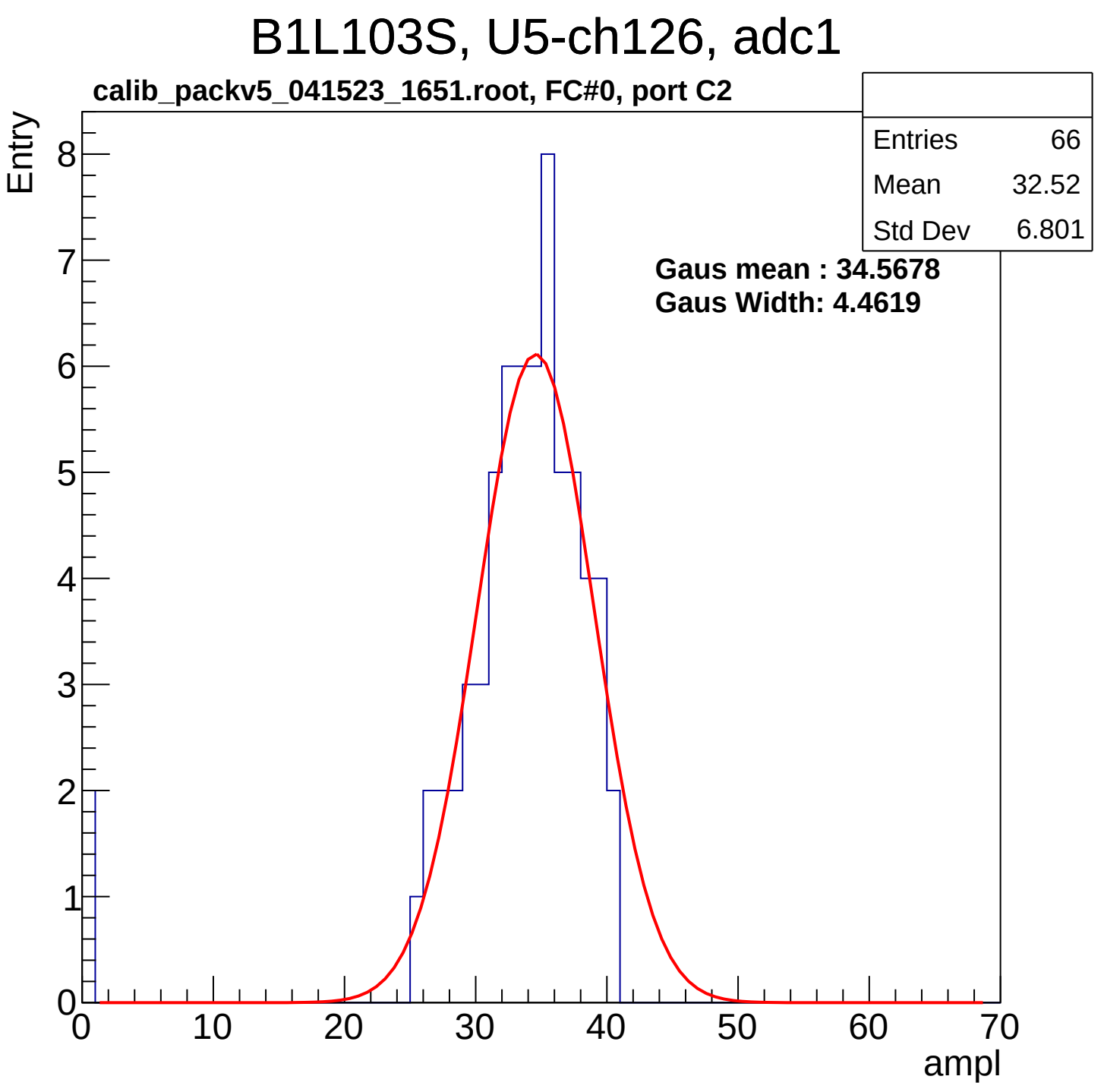
B1L103S, U5-ch126, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 32.52
Std Dev 6.801
Gaus mean : 34.5678
Gaus Width: 4.4619
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
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60
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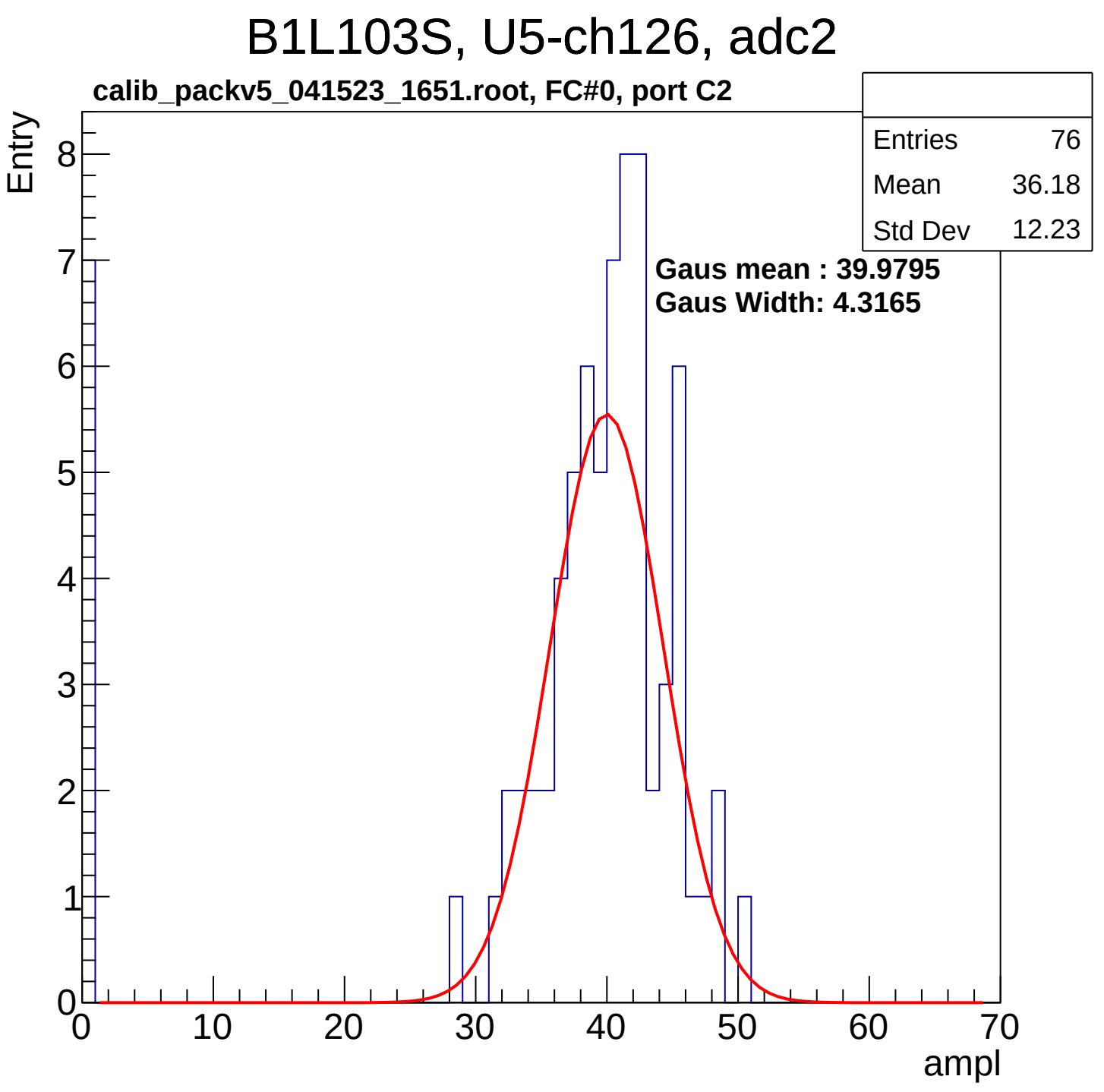
B1L103S, U5-ch126, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 36.18
Std Dev 12.23
Gaus mean : 39.9795
Gaus Width: 4.3165
Entry
ampl
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4
5
6
7
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0
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20
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60
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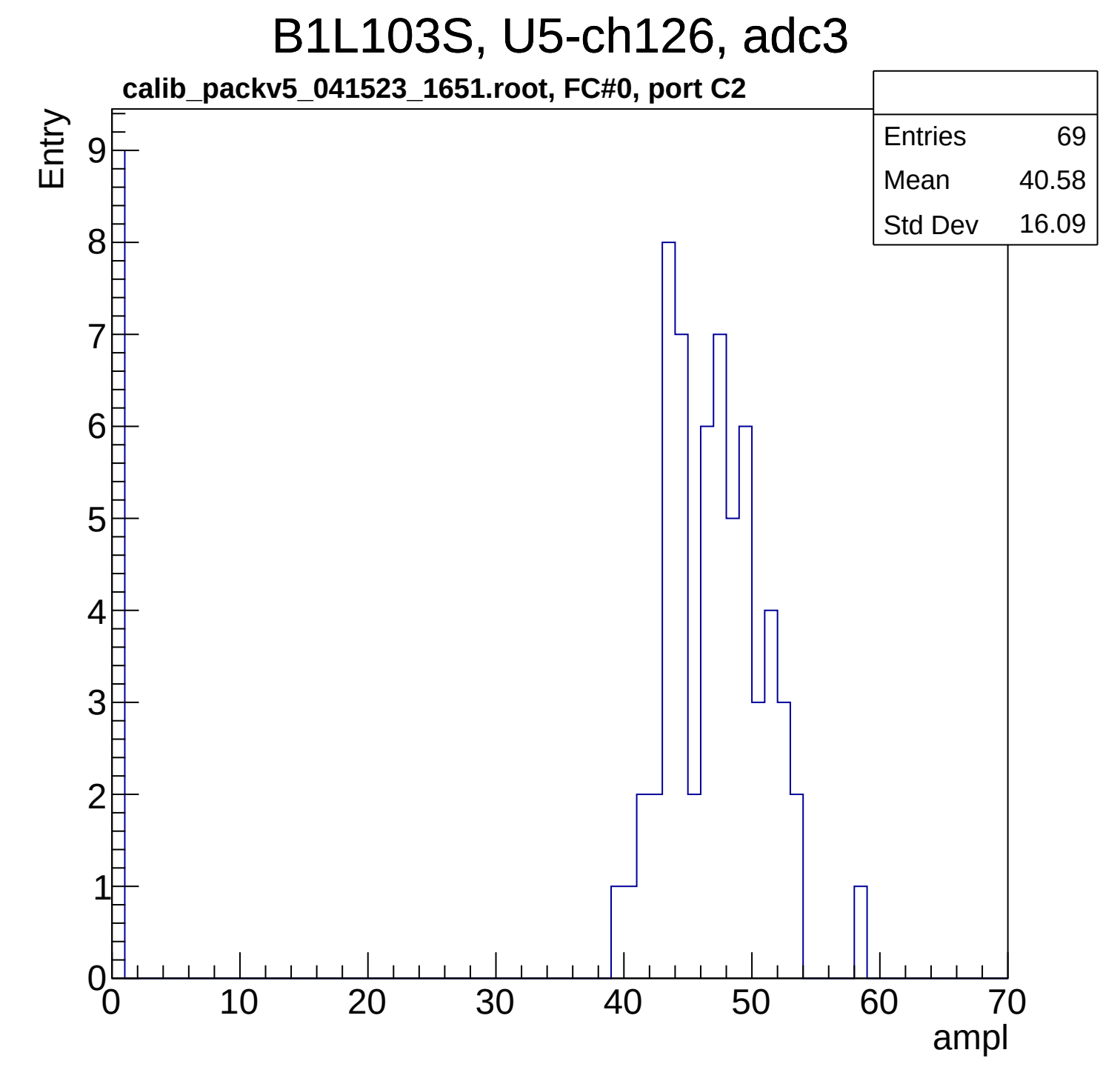
B1L103S, U5-ch126, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 40.58
Std Dev 16.09
Entry
ampl
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3
4
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6
7
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0
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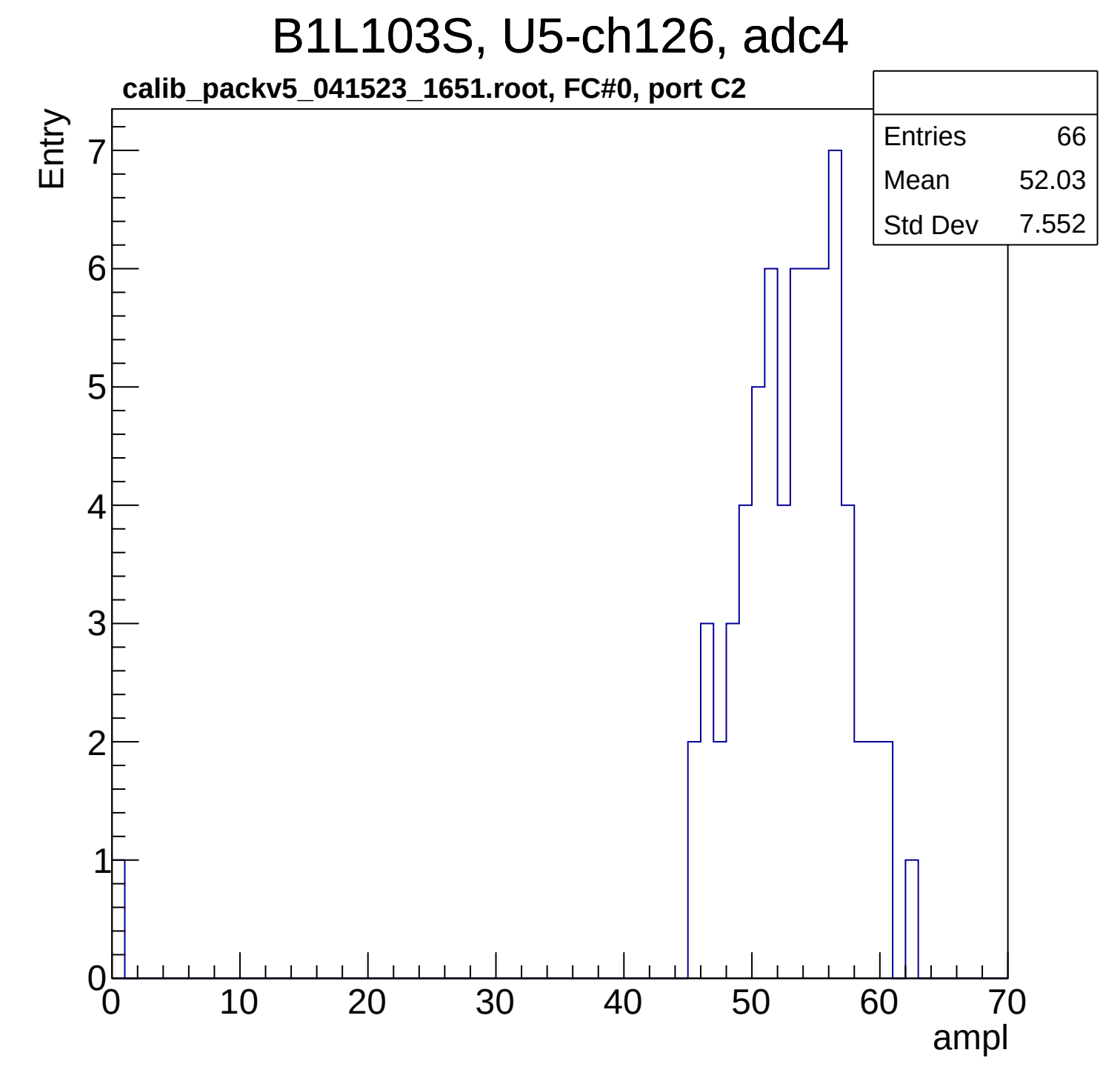
B1L103S, U5-ch126, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 52.03
Std Dev 7.552
Entry
ampl
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4
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0
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60
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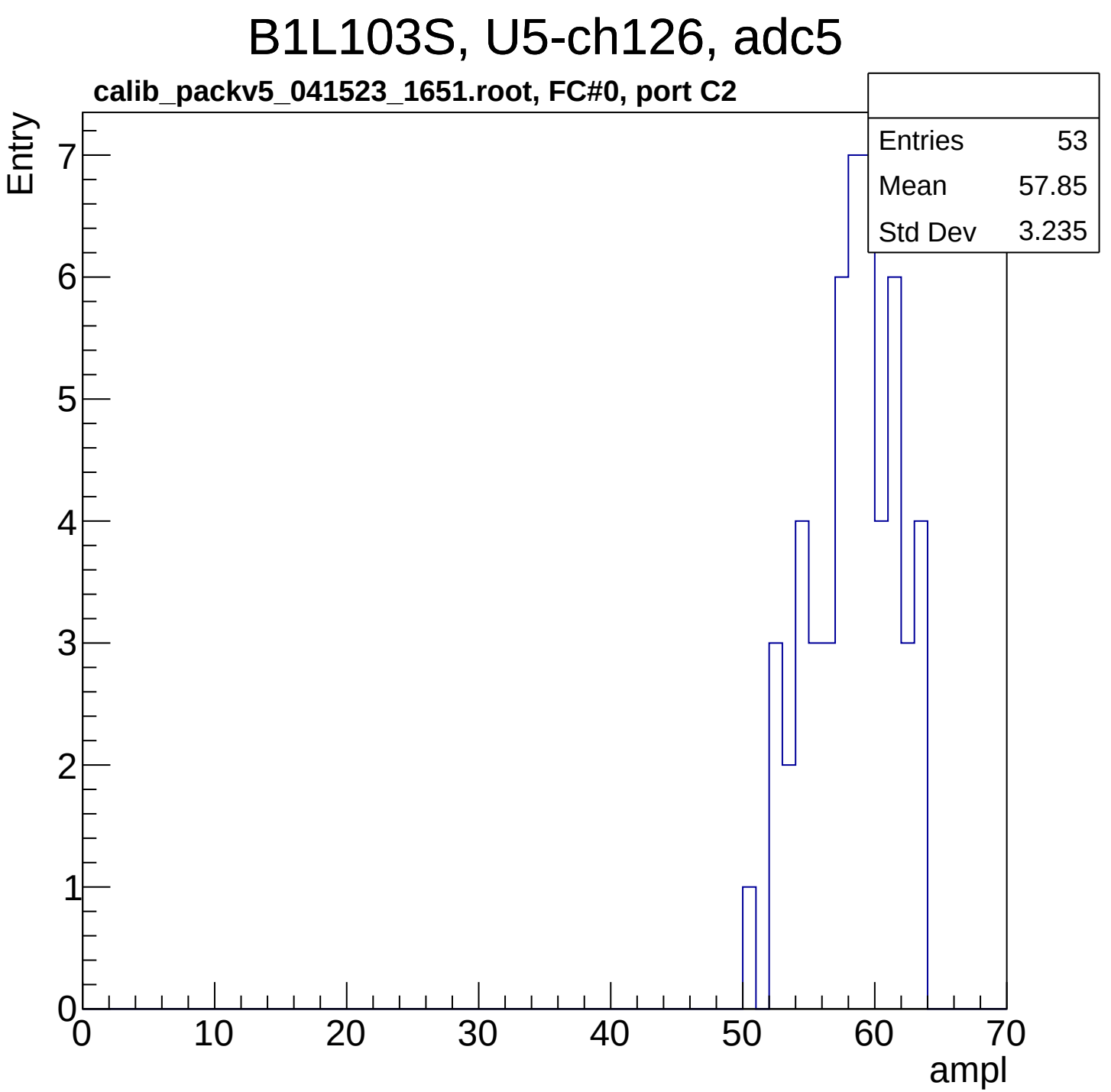
B1L103S, U5-ch126, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 57.85
Std Dev 3.235
Entry
ampl
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6
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0
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20
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60
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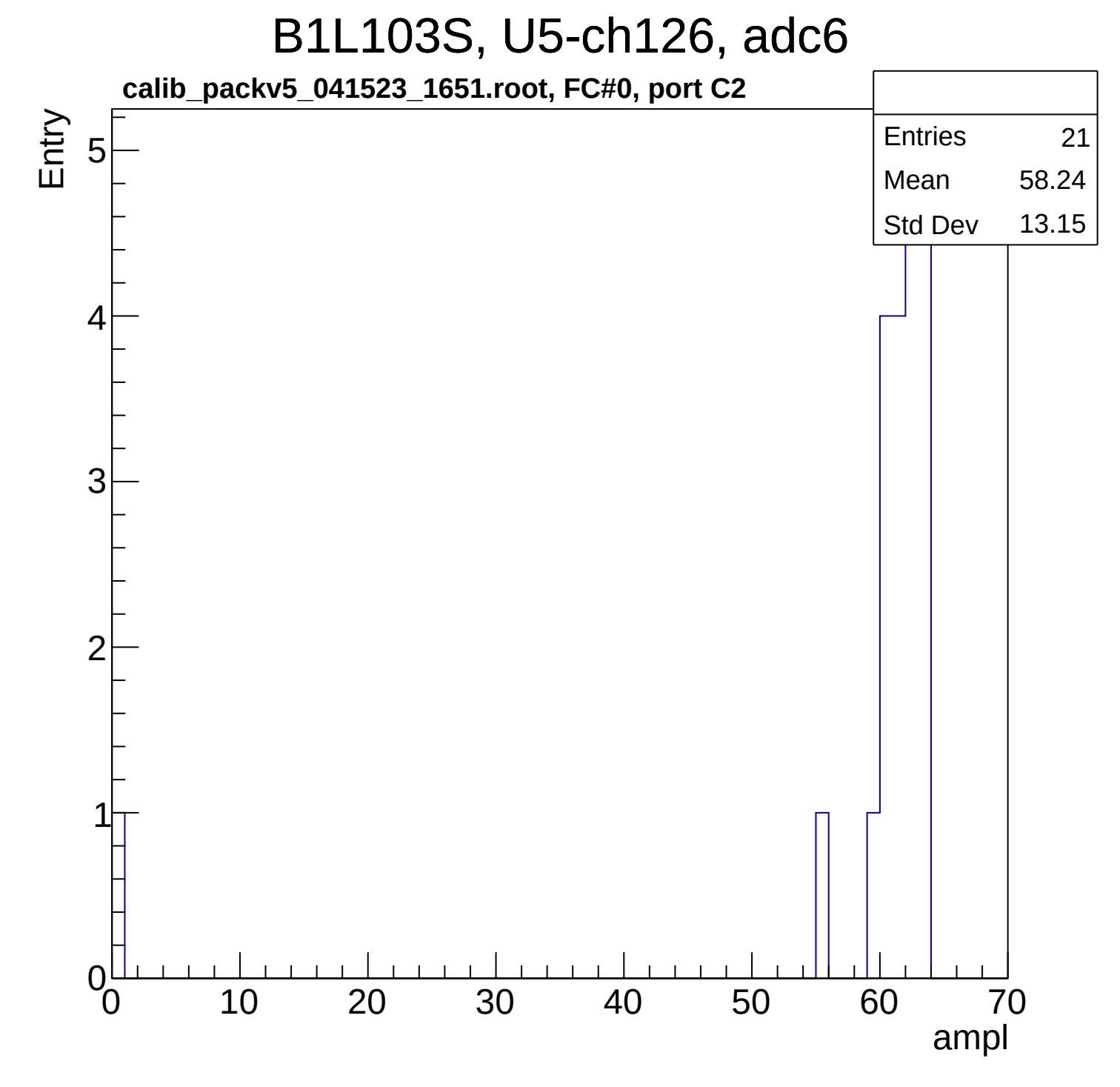
B1L103S, U5-ch126, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 58.24
Std Dev 13.15
Entry
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3
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5
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10
20
30
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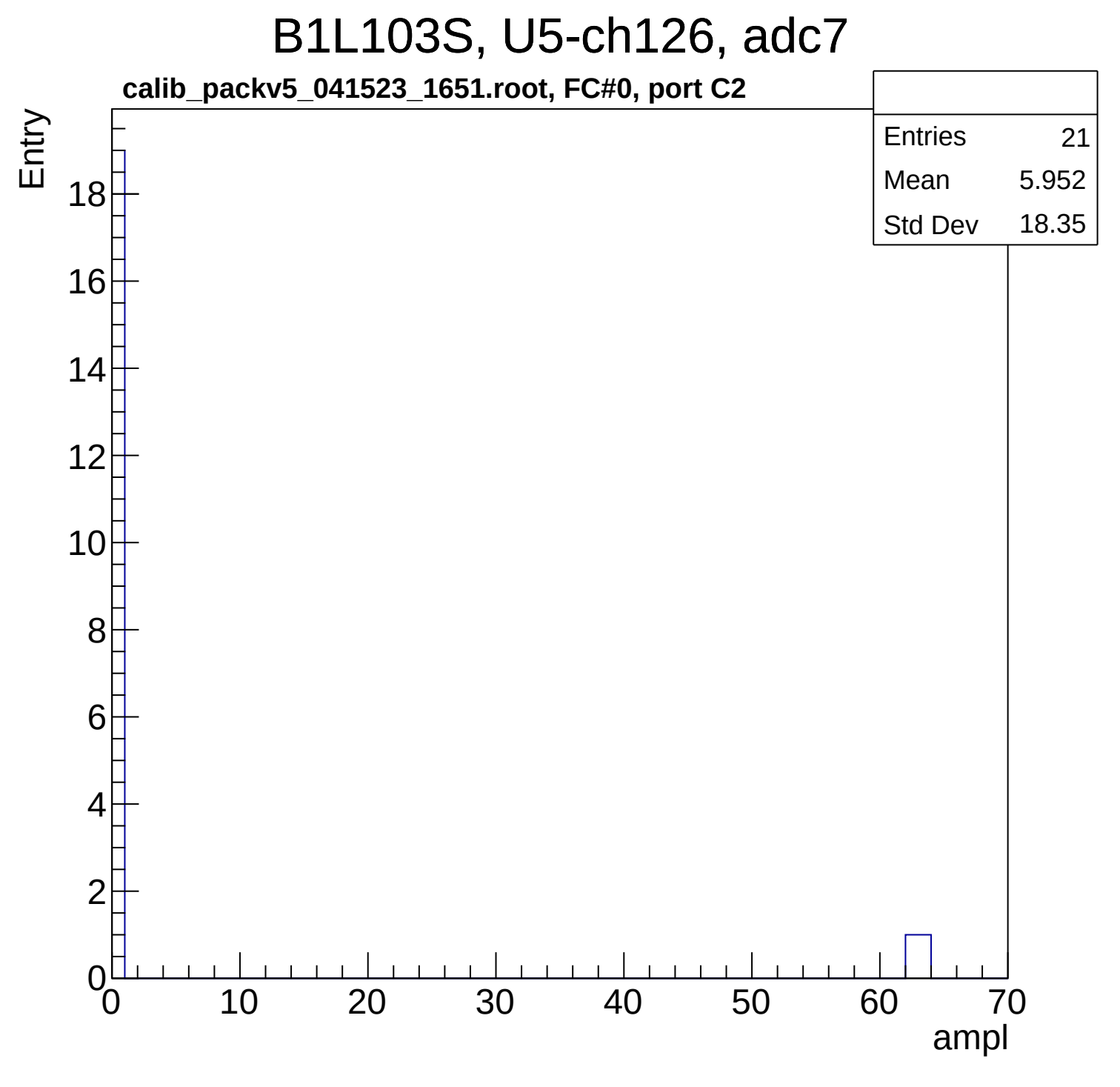
50
60
70
ampl


B1L103S, U5-ch126, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
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10
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14
16
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10
20
30
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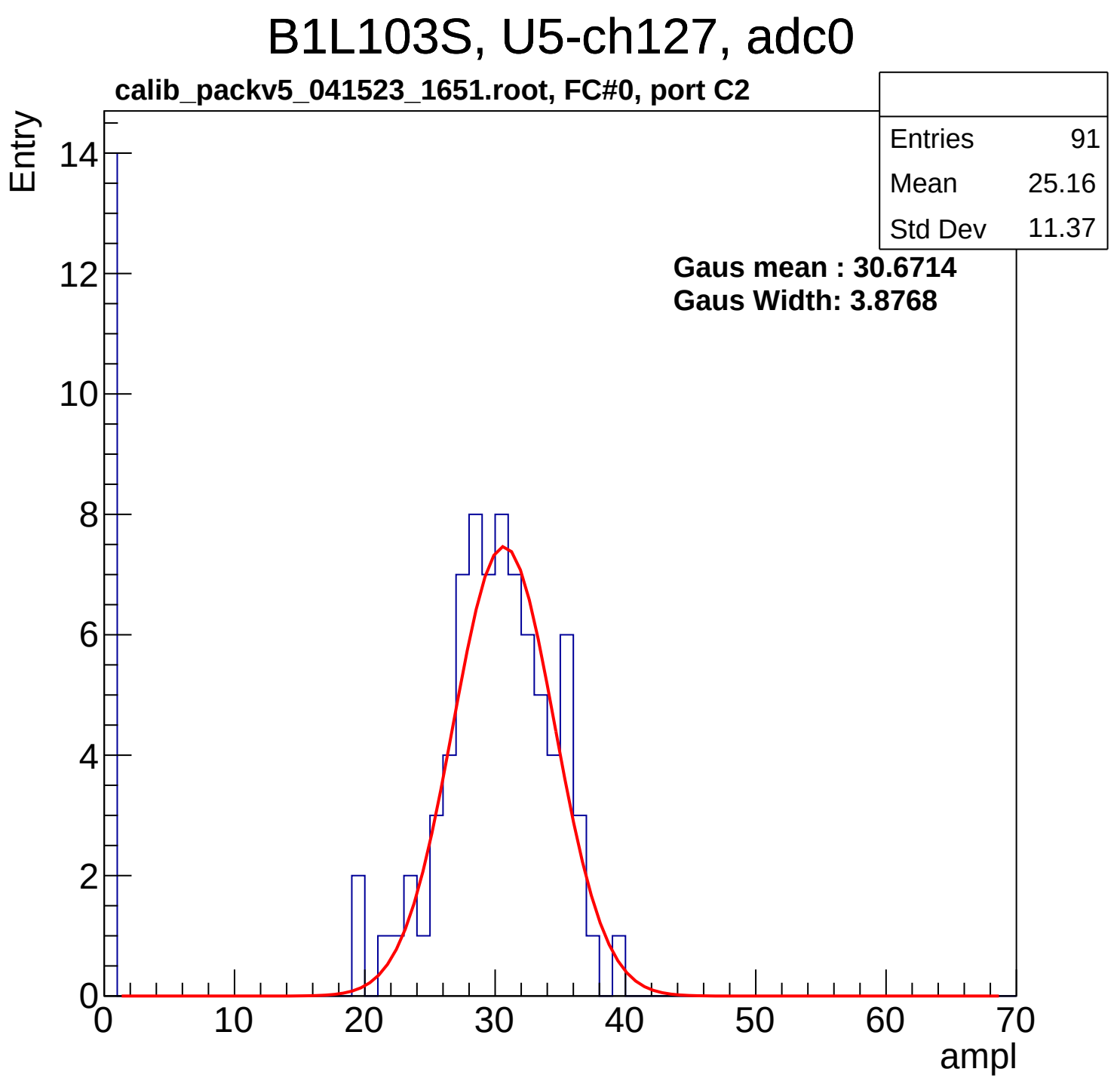
50
60
70
ampl


B1L103S, U5-ch127, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 25.16
Std Dev 11.37
Gaus mean : 30.6714
Gaus Width: 3.8768
Entry
ampl
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6
8
10
12
14
0
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20
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40
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60
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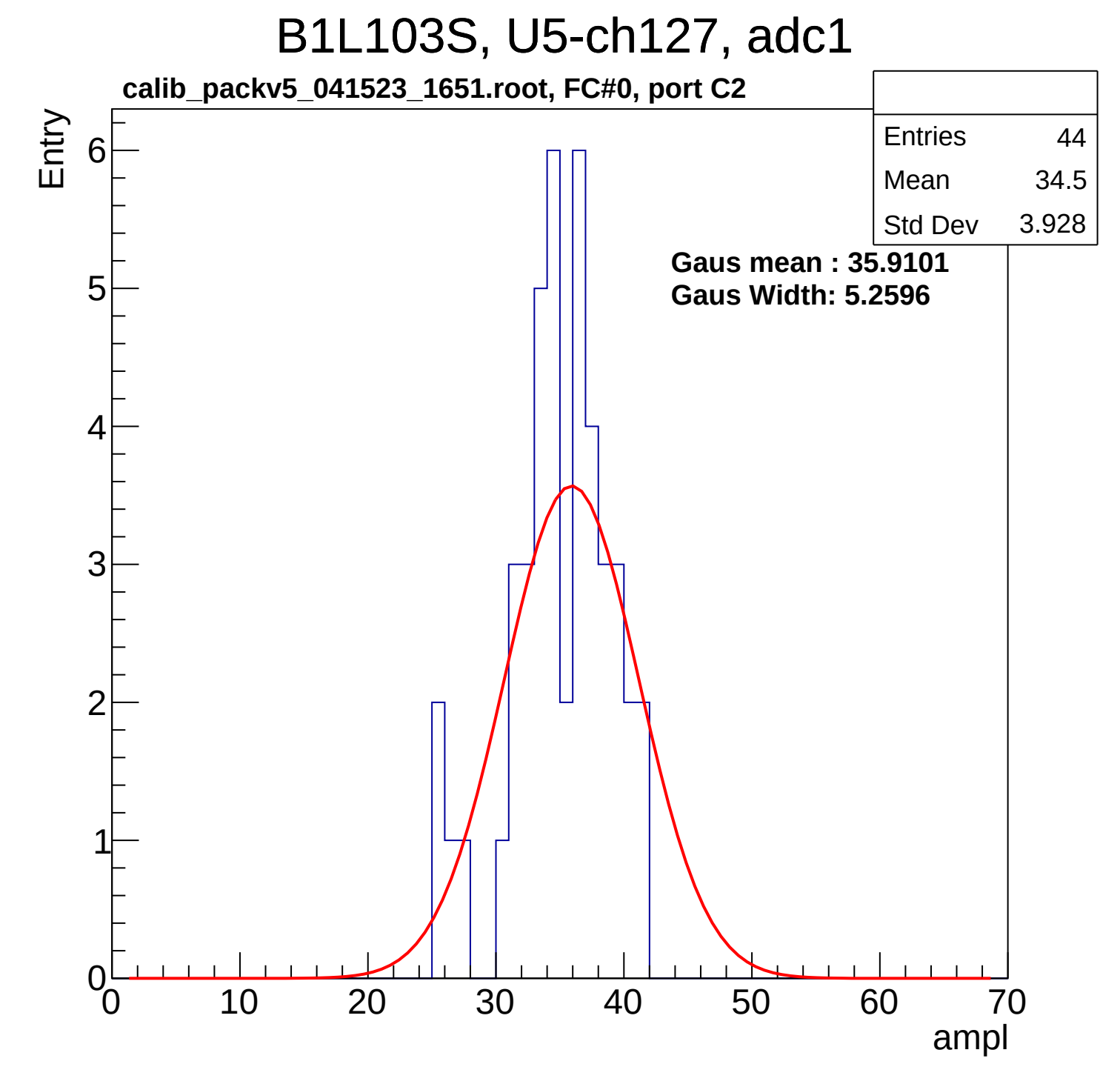
B1L103S, U5-ch127, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 34.5
Std Dev 3.928
Gaus mean : 35.9101
Gaus Width: 5.2596
Entry
ampl
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2
3
4
5
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0
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20
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40
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60
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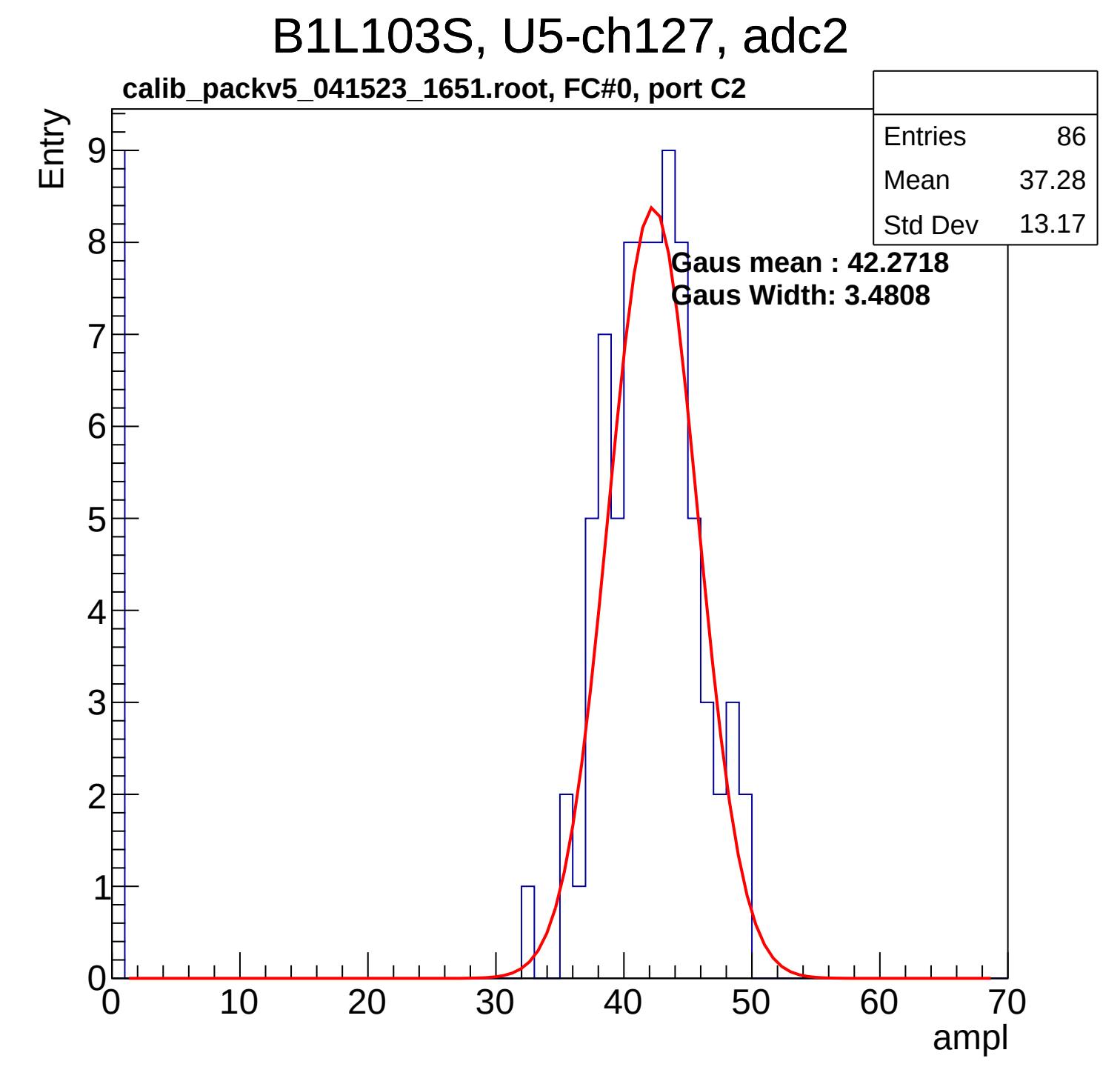
B1L103S, U5-ch127, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 37.28
Std Dev 13.17
Gaus mean : 42.2718
Gaus Width: 3.4808
Entry
ampl
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2
3
4
5
6
7
8
9
0
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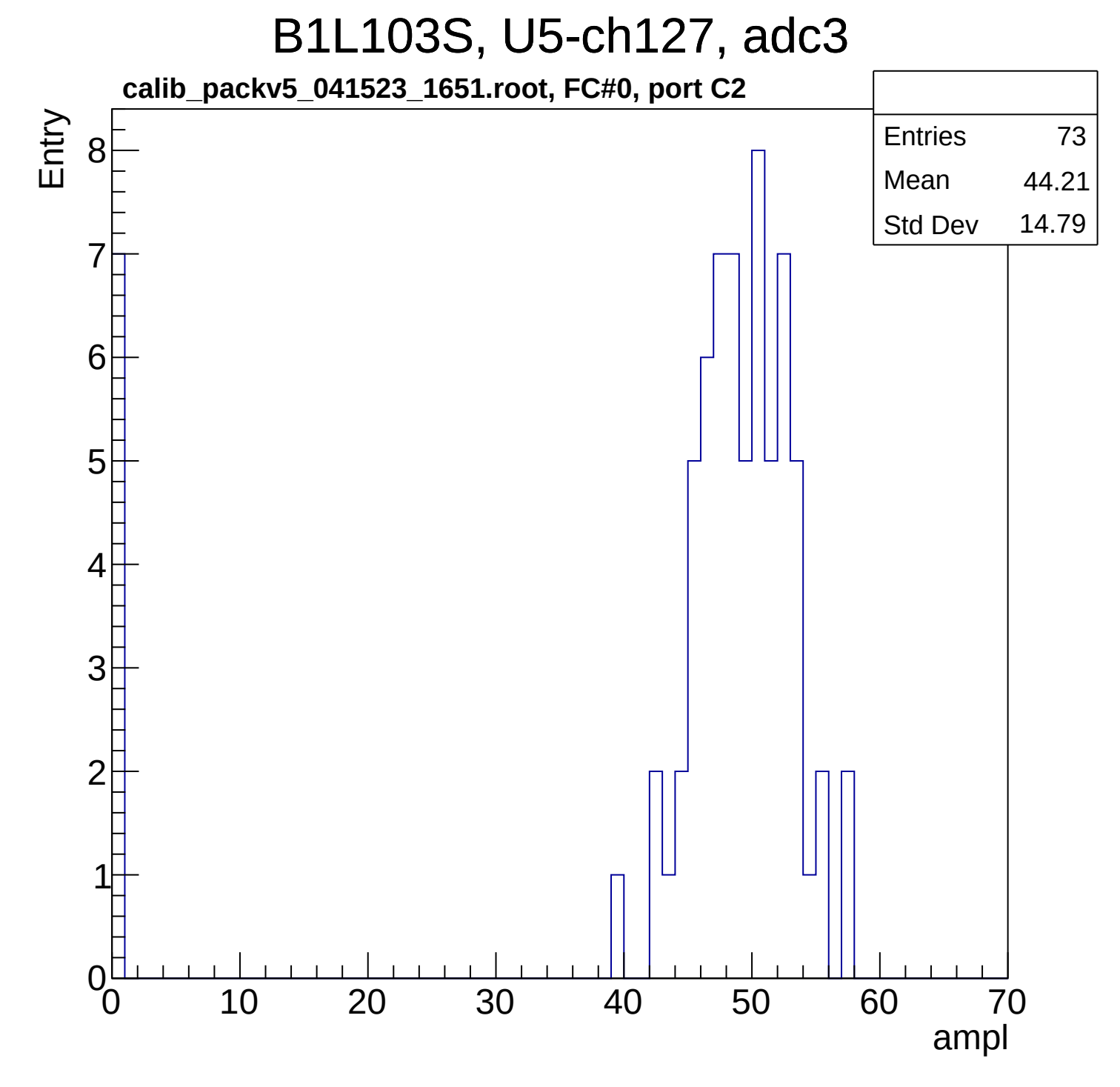
B1L103S, U5-ch127, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 44.21
Std Dev 14.79
Entry
ampl
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4
5
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7
8
0
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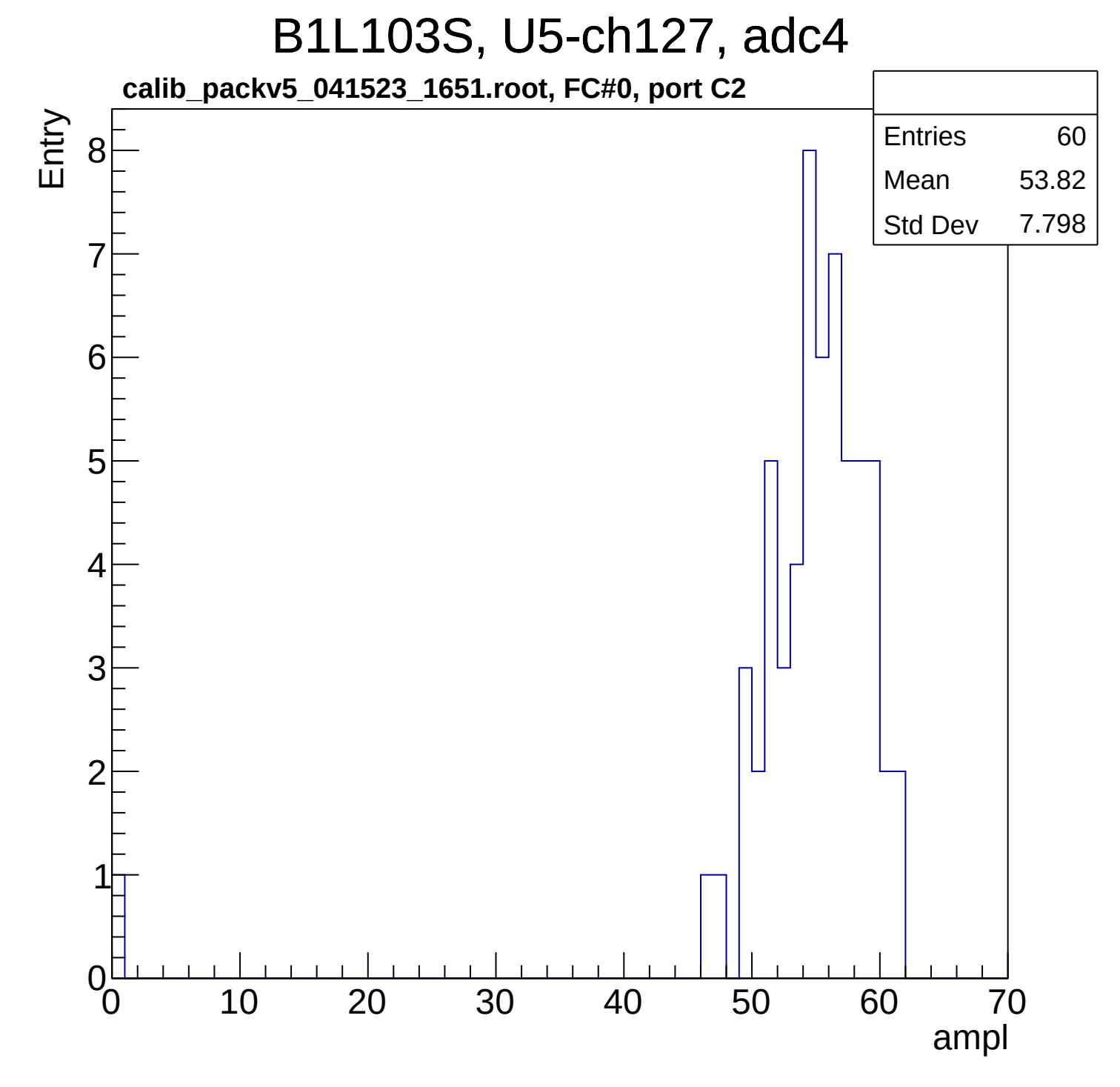
B1L103S, U5-ch127, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 53.82
Std Dev 7.798
Entry
ampl
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4
5
6
7
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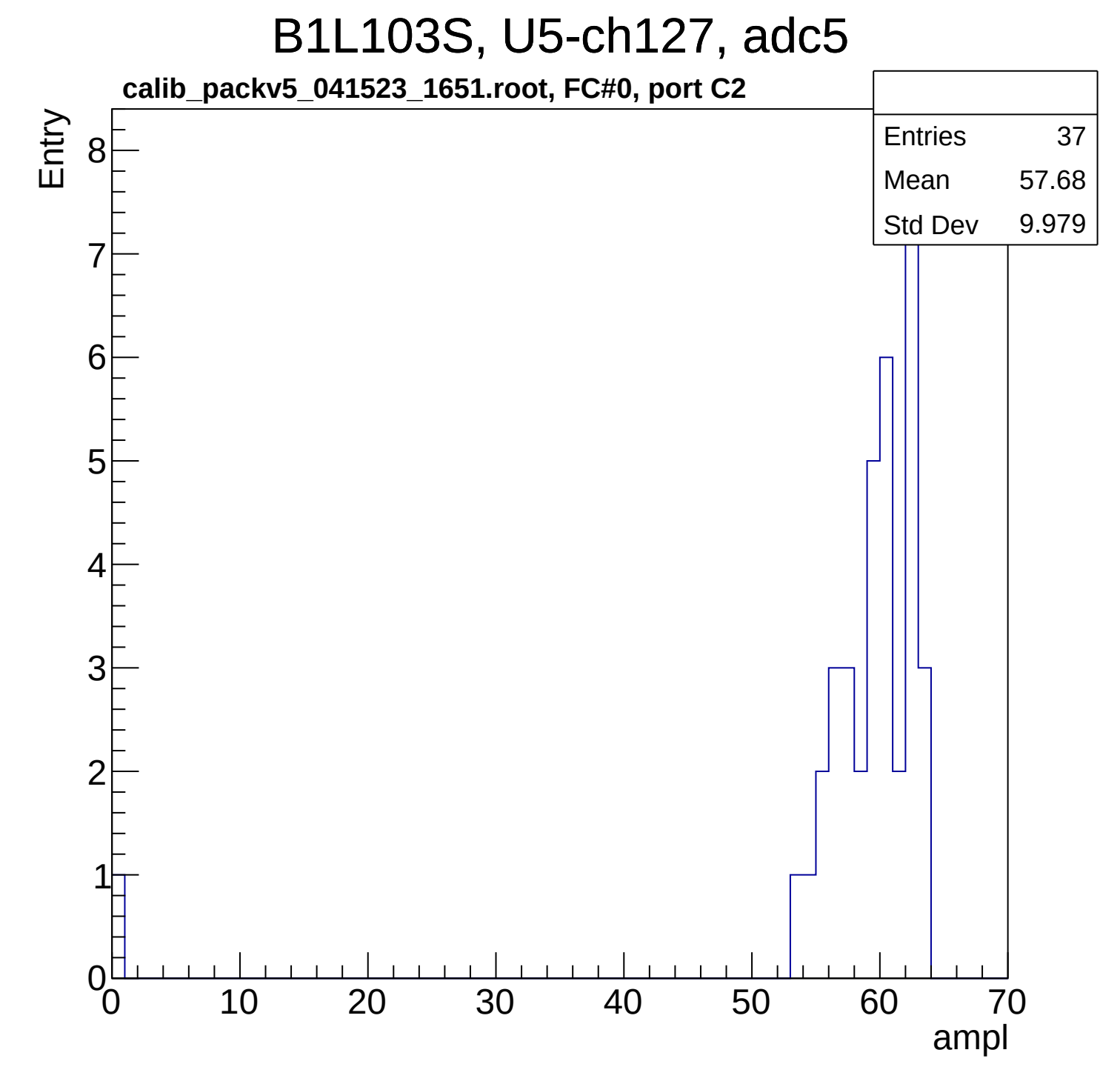
B1L103S, U5-ch127, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 57.68
Std Dev 9.979
Entry
ampl
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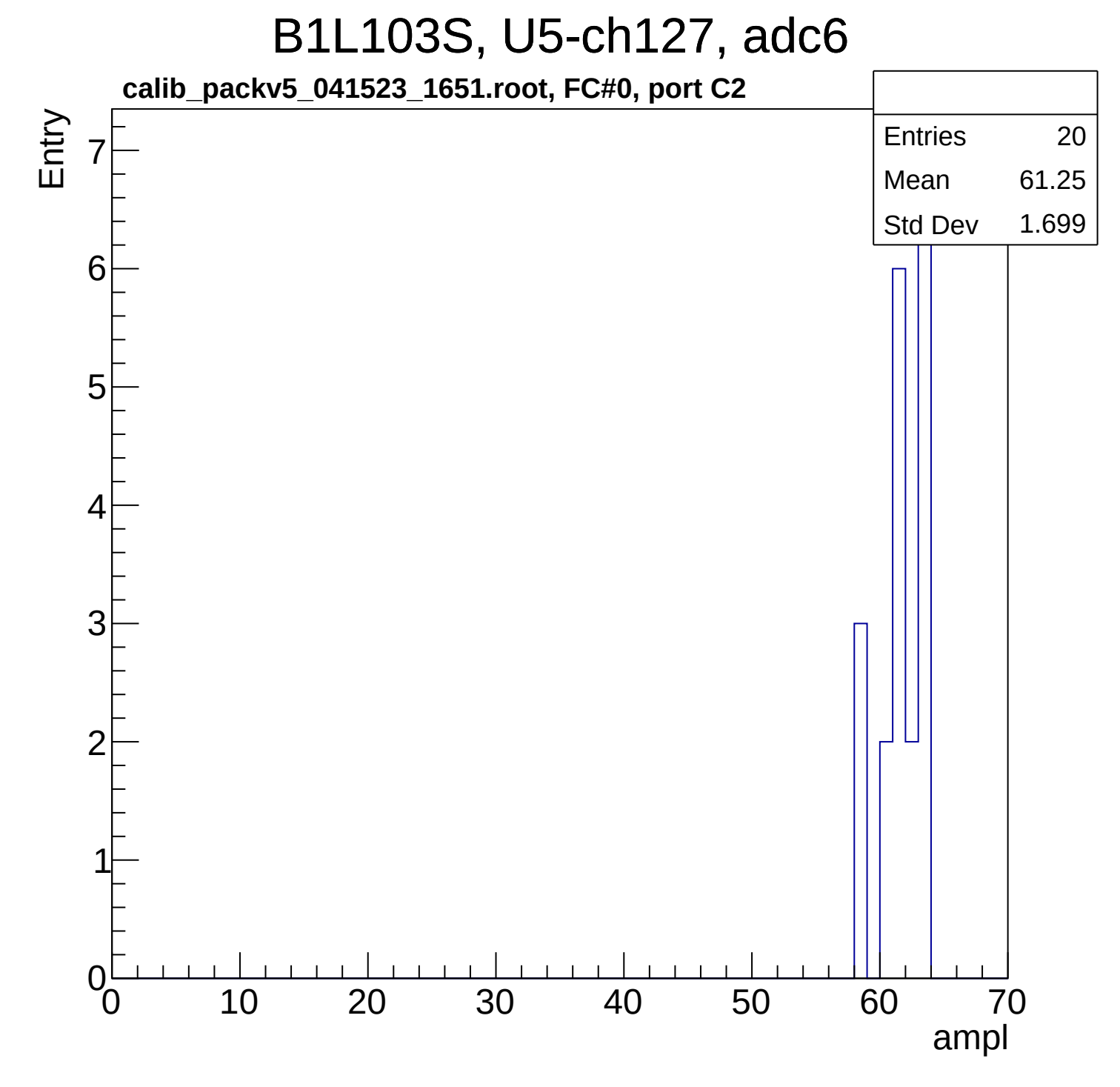
B1L103S, U5-ch127, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 61.25
Std Dev 1.699
Entry
ampl
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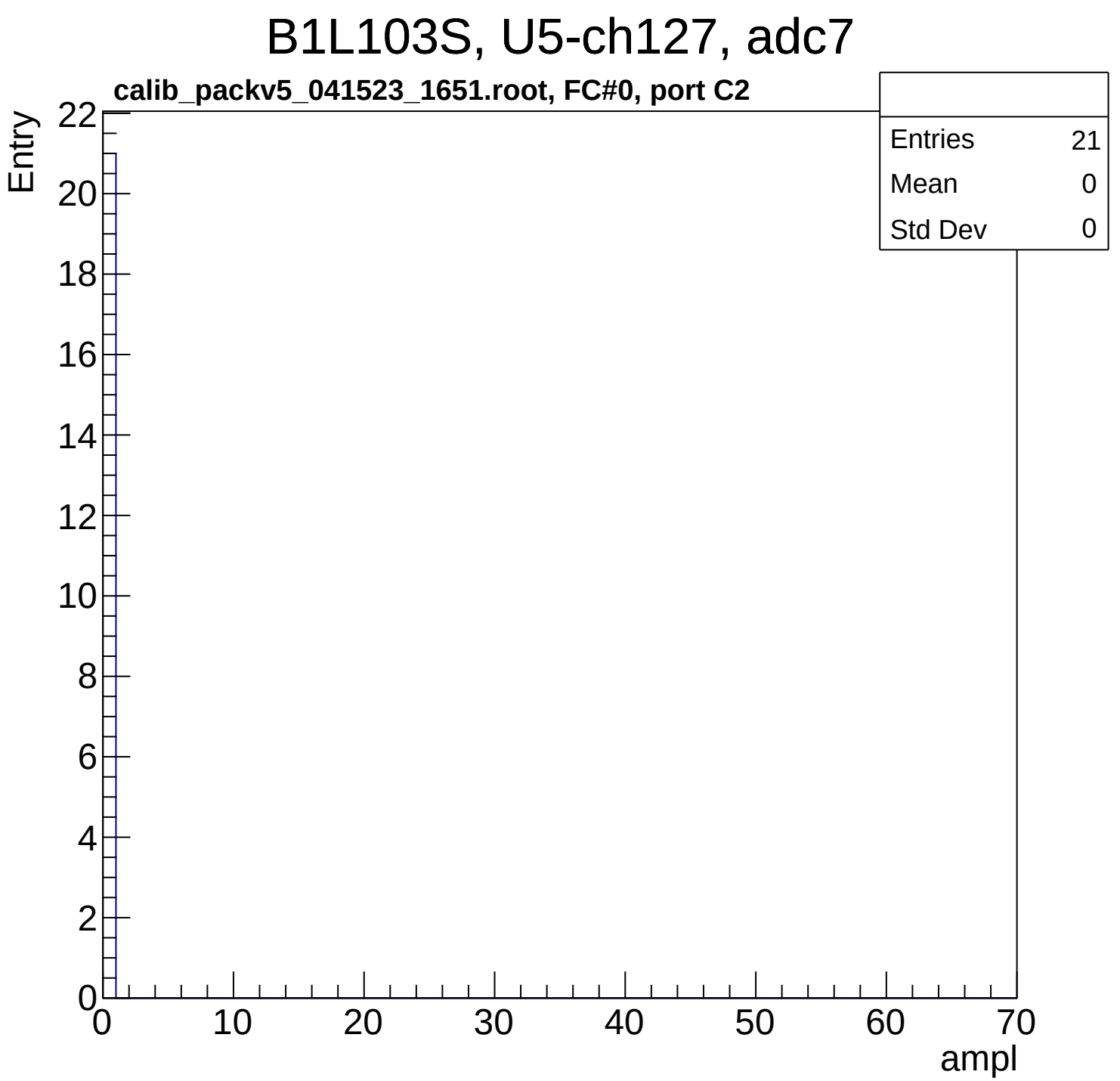
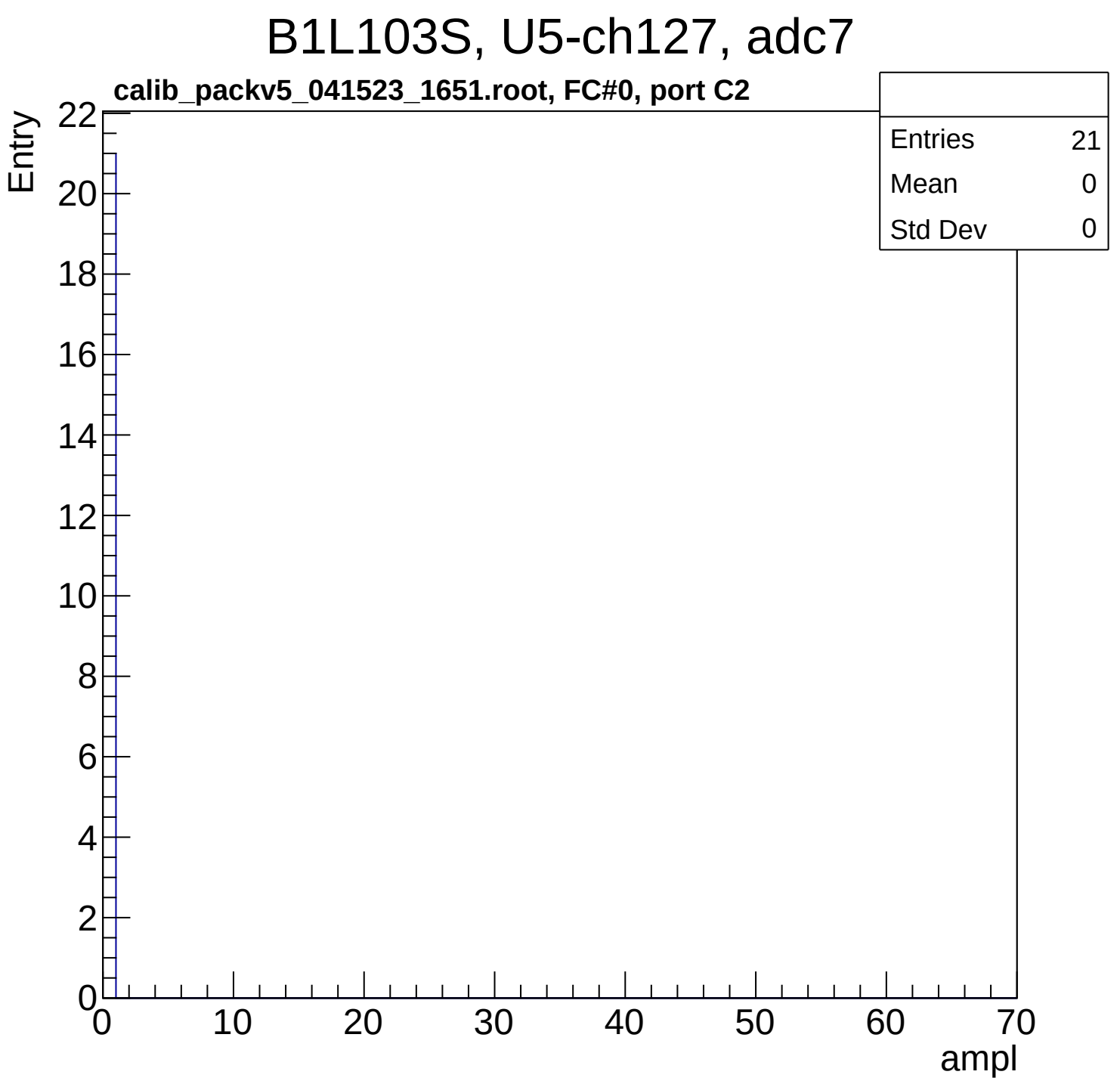
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U5-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 0
Std Dev 0
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70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Entries 21
Mean 0
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