



# B0L000S, U7-ch0, adc0

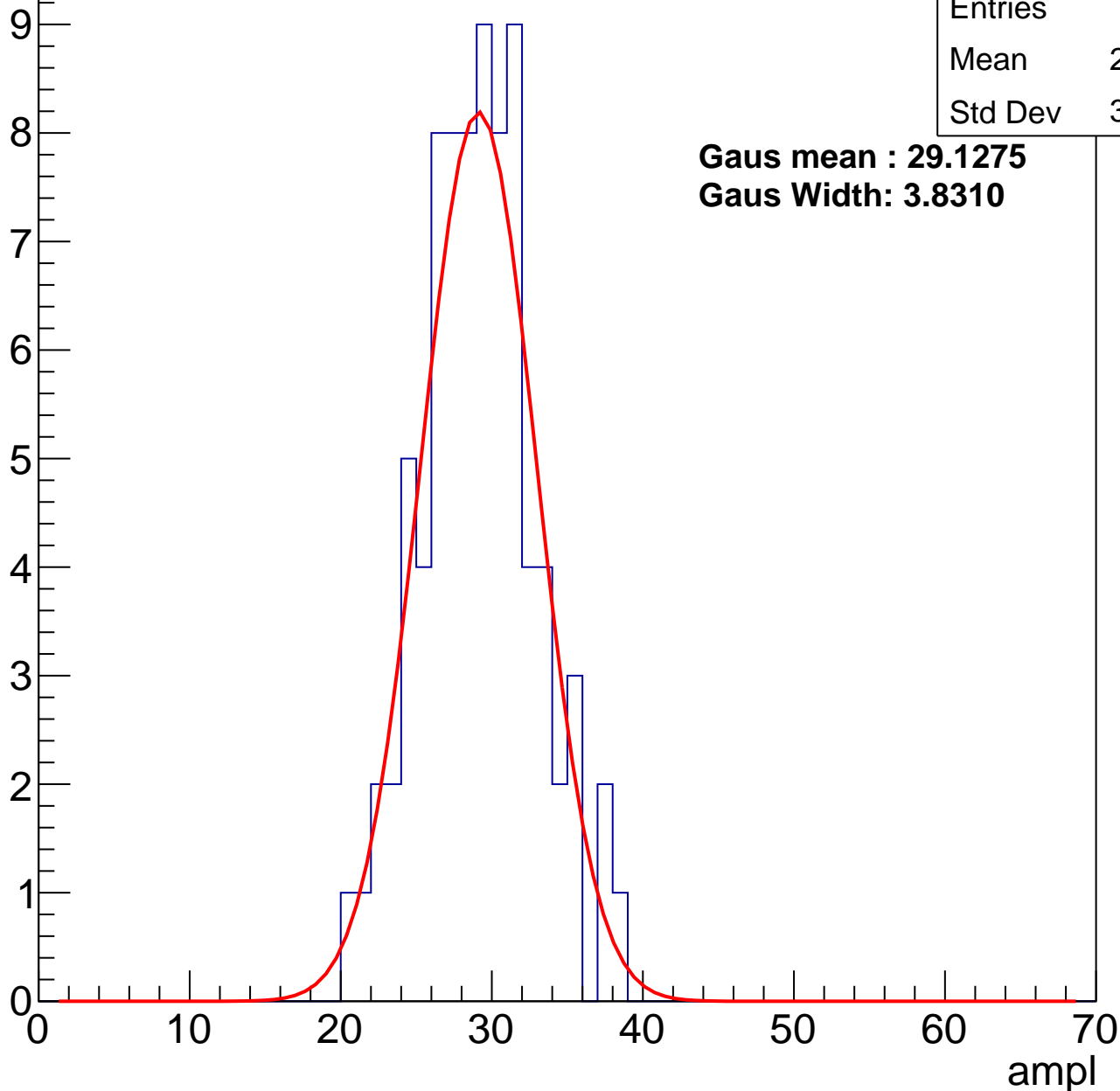
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	81
Mean	28.69
Std Dev	3.717

**Gaus mean : 29.1275**

**Gaus Width: 3.8310**



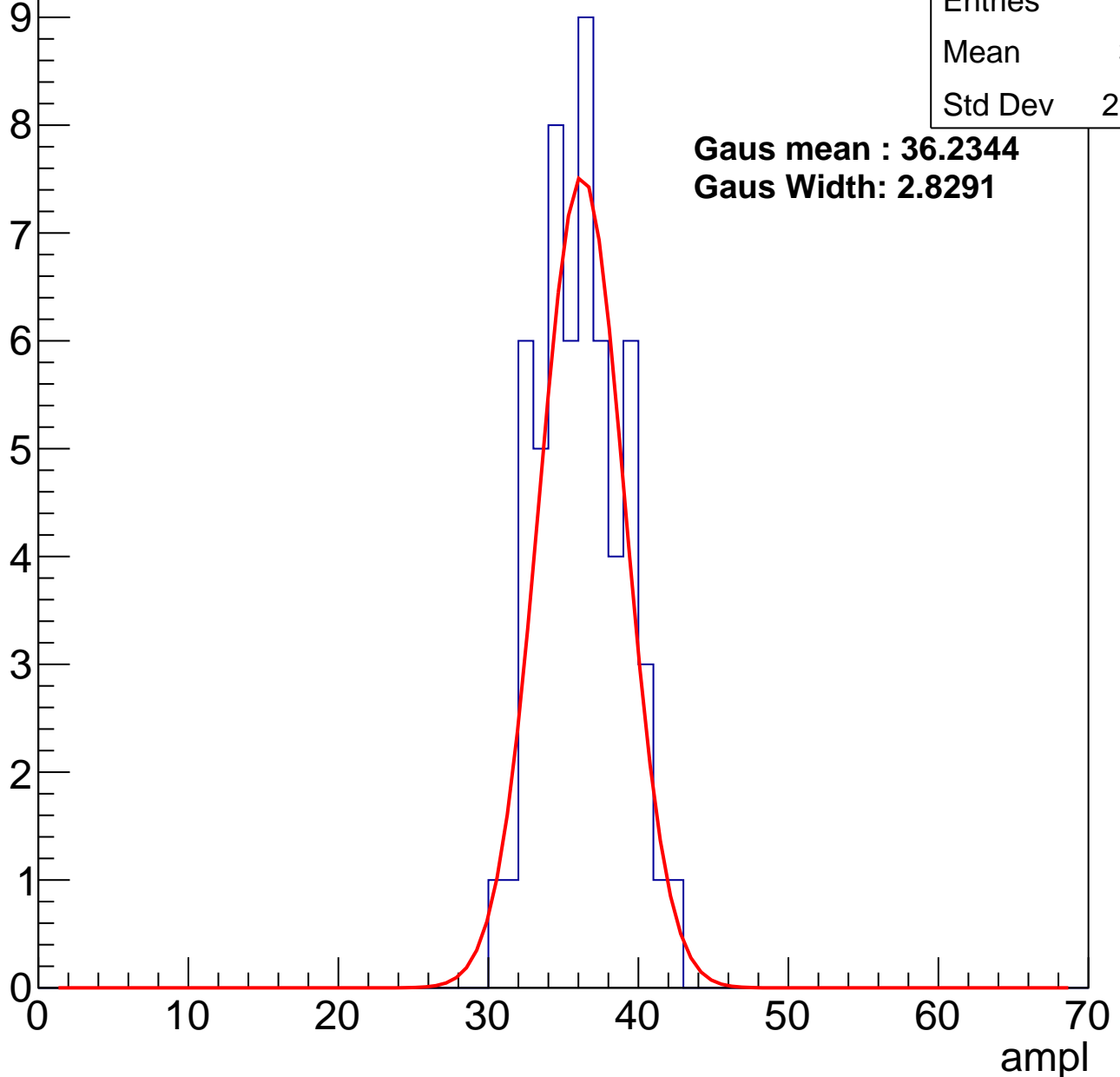
# B0L000S, U7-ch0, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	57
Mean	35.7
Std Dev	2.714

**Gaus mean : 36.2344**  
**Gaus Width: 2.8291**



# B0L000S, U7-ch0, adc2

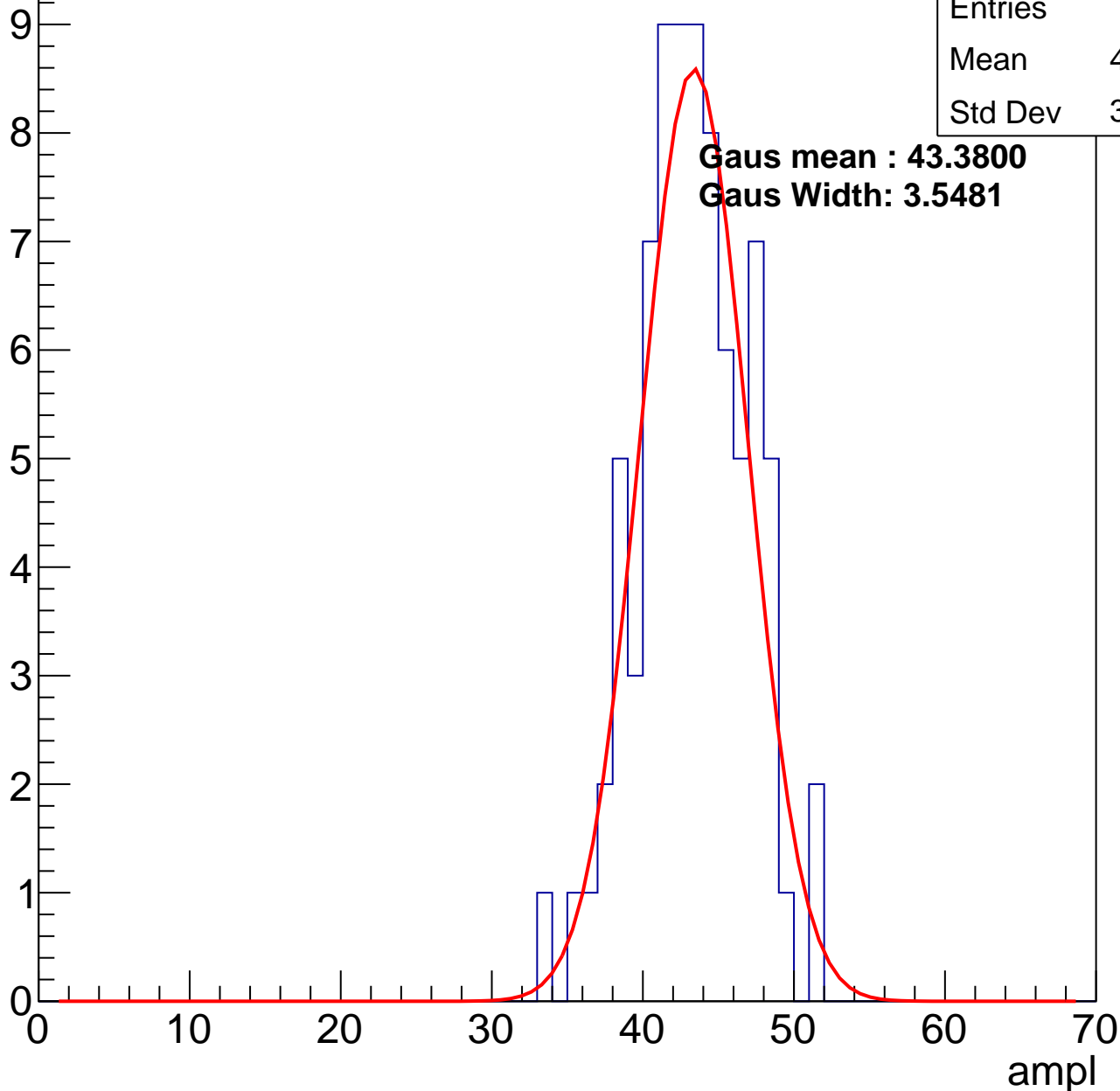
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	81
Mean	42.85
Std Dev	3.587

**Gaus mean : 43.3800**

**Gaus Width: 3.5481**

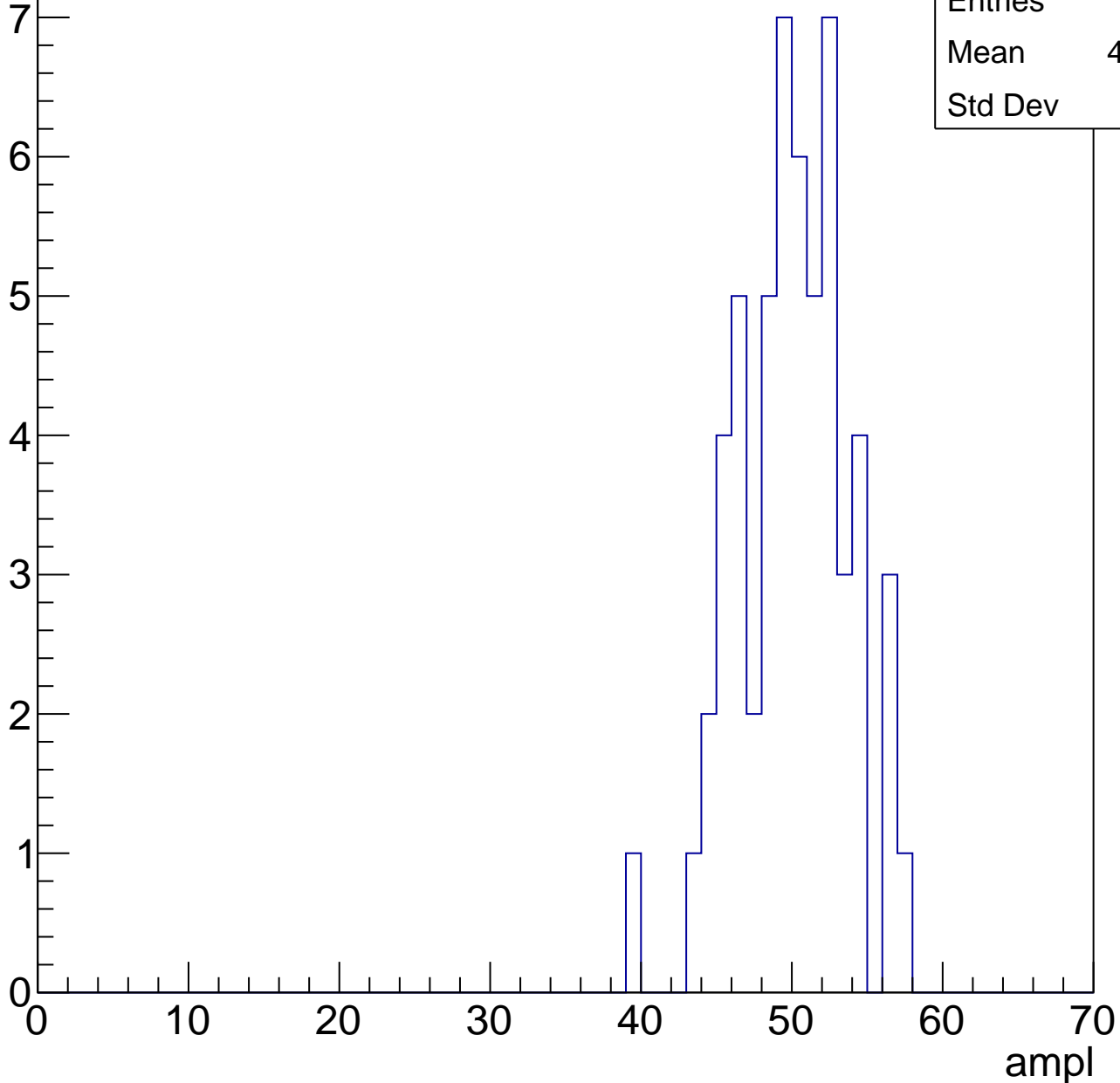


# B0L000S, U7-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	56
Mean	49.57
Std Dev	3.63

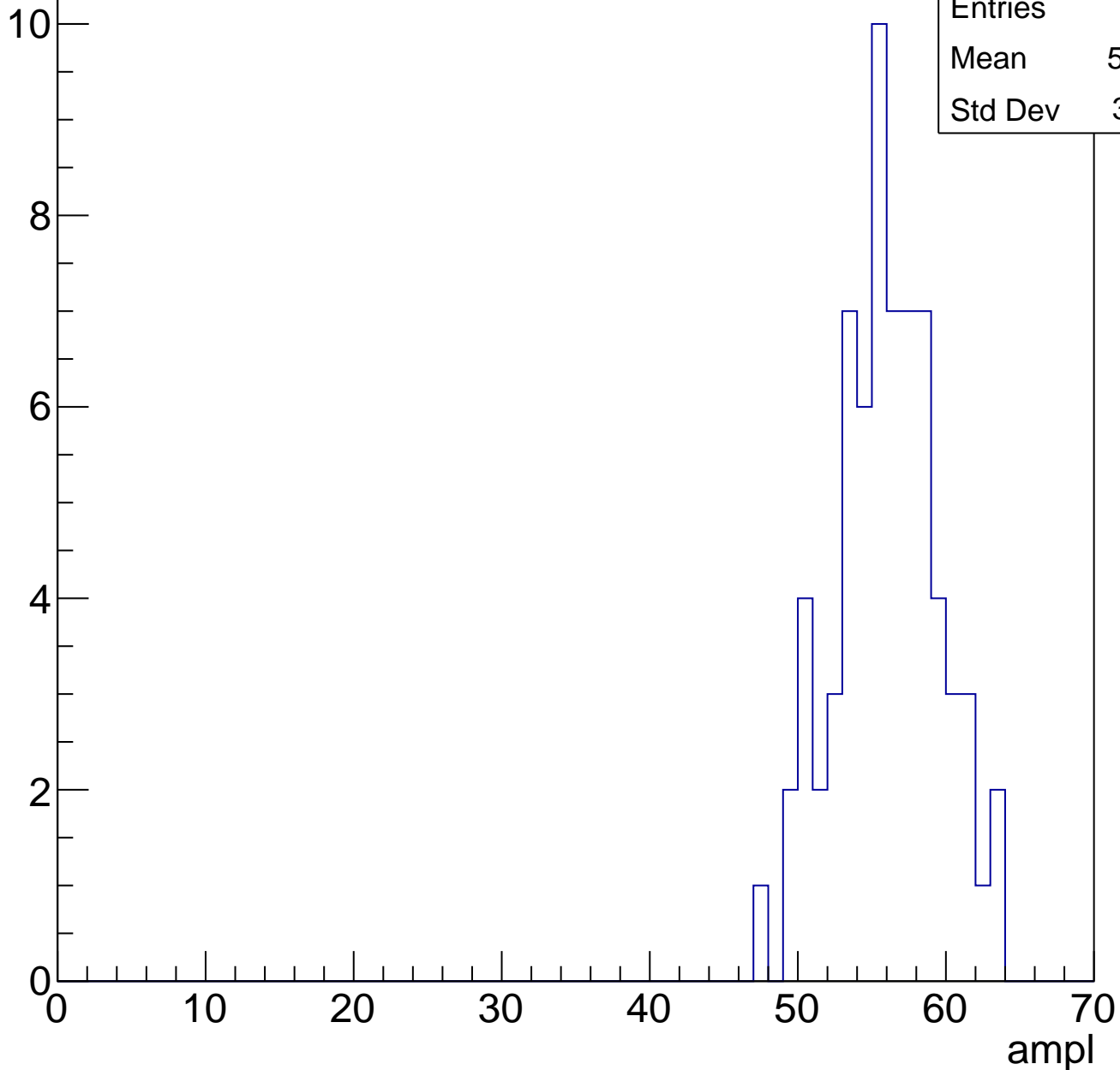


# B0L000S, U7-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	69
Mean	55.54
Std Dev	3.471

Entry

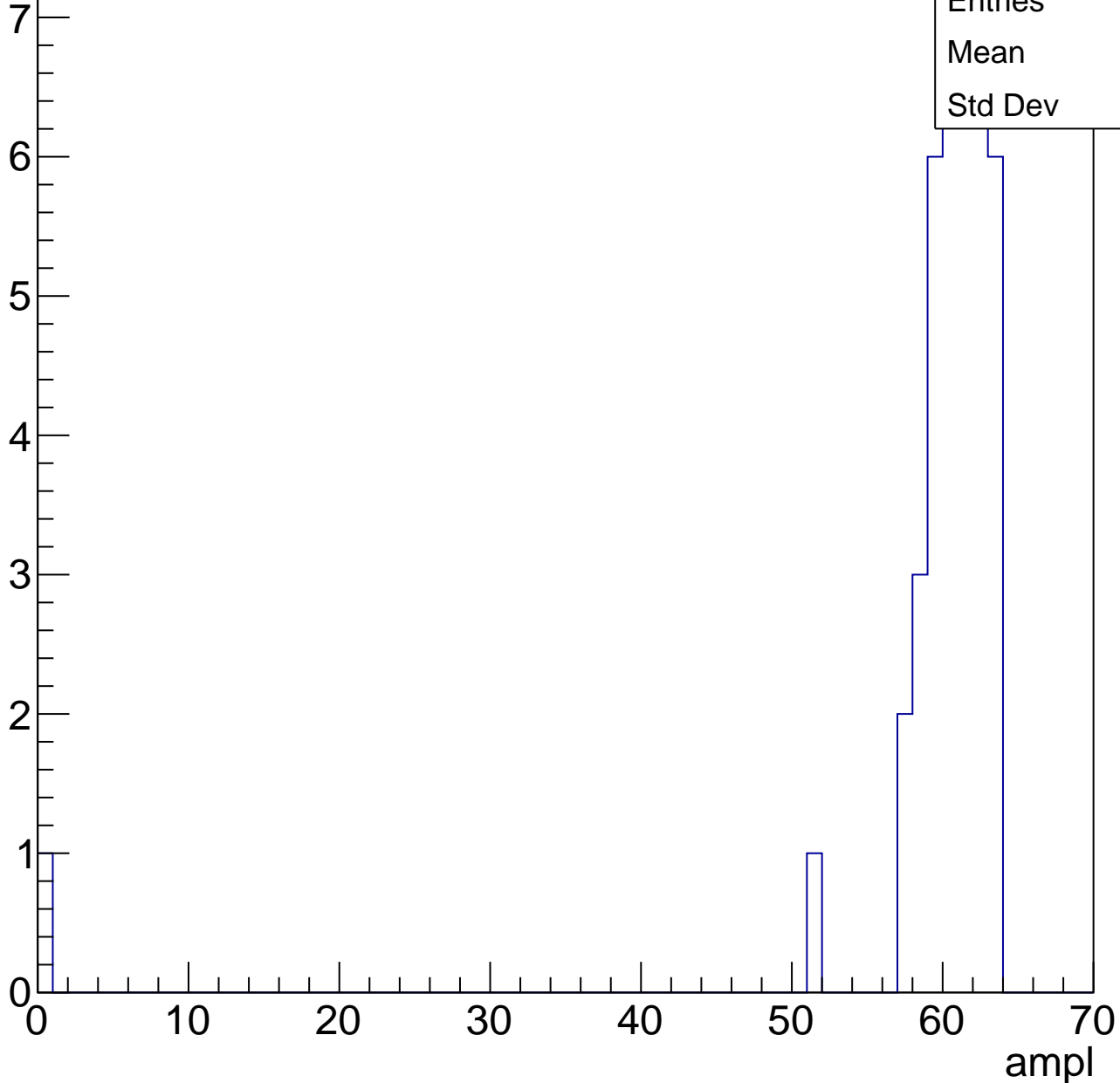


# B0L000S, U7-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	40
Mean	58.8
Std Dev	9.68



# B0L000S, U7-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

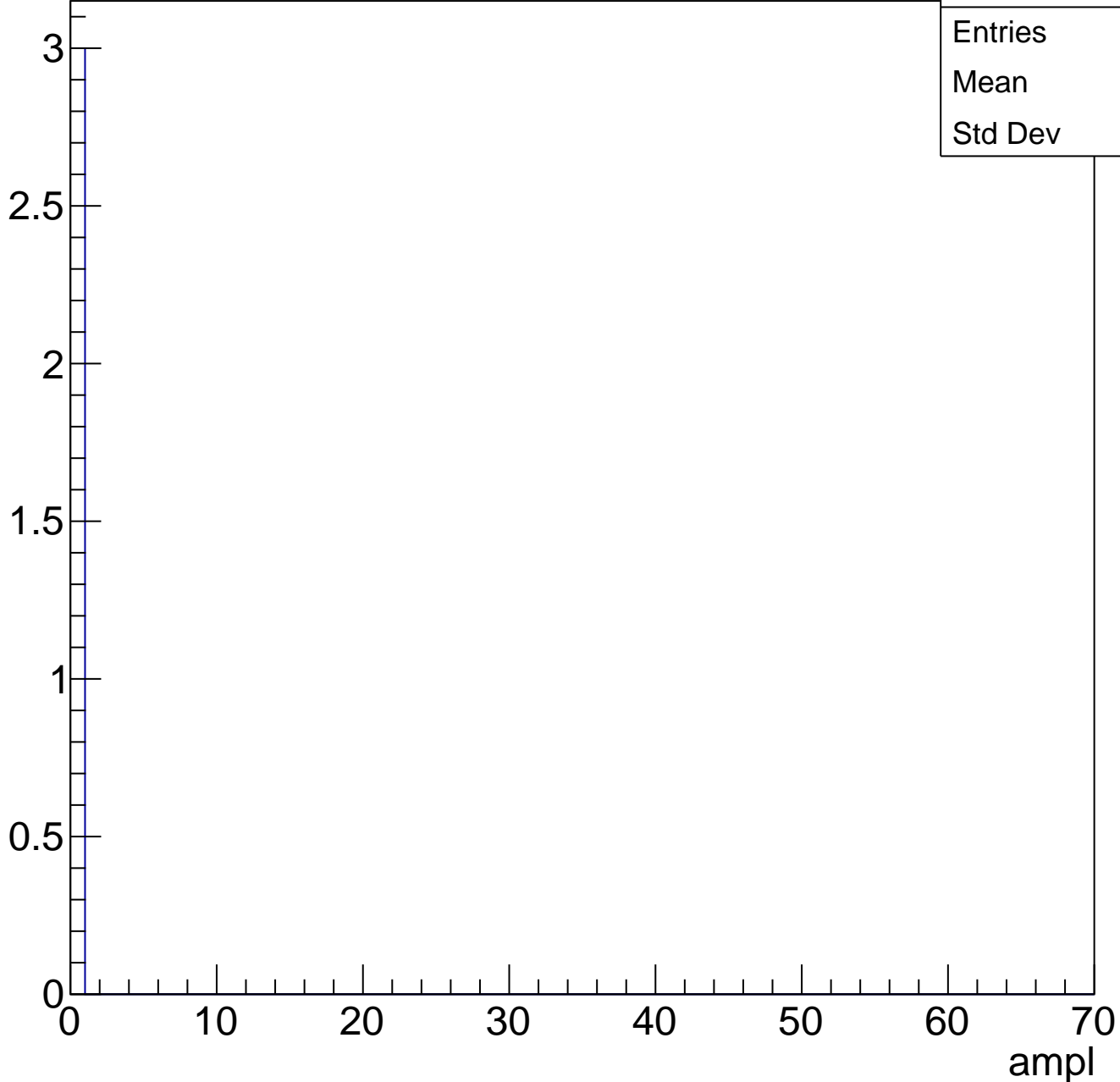




# B0L000S, U7-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L000S, U7-ch1, adc0

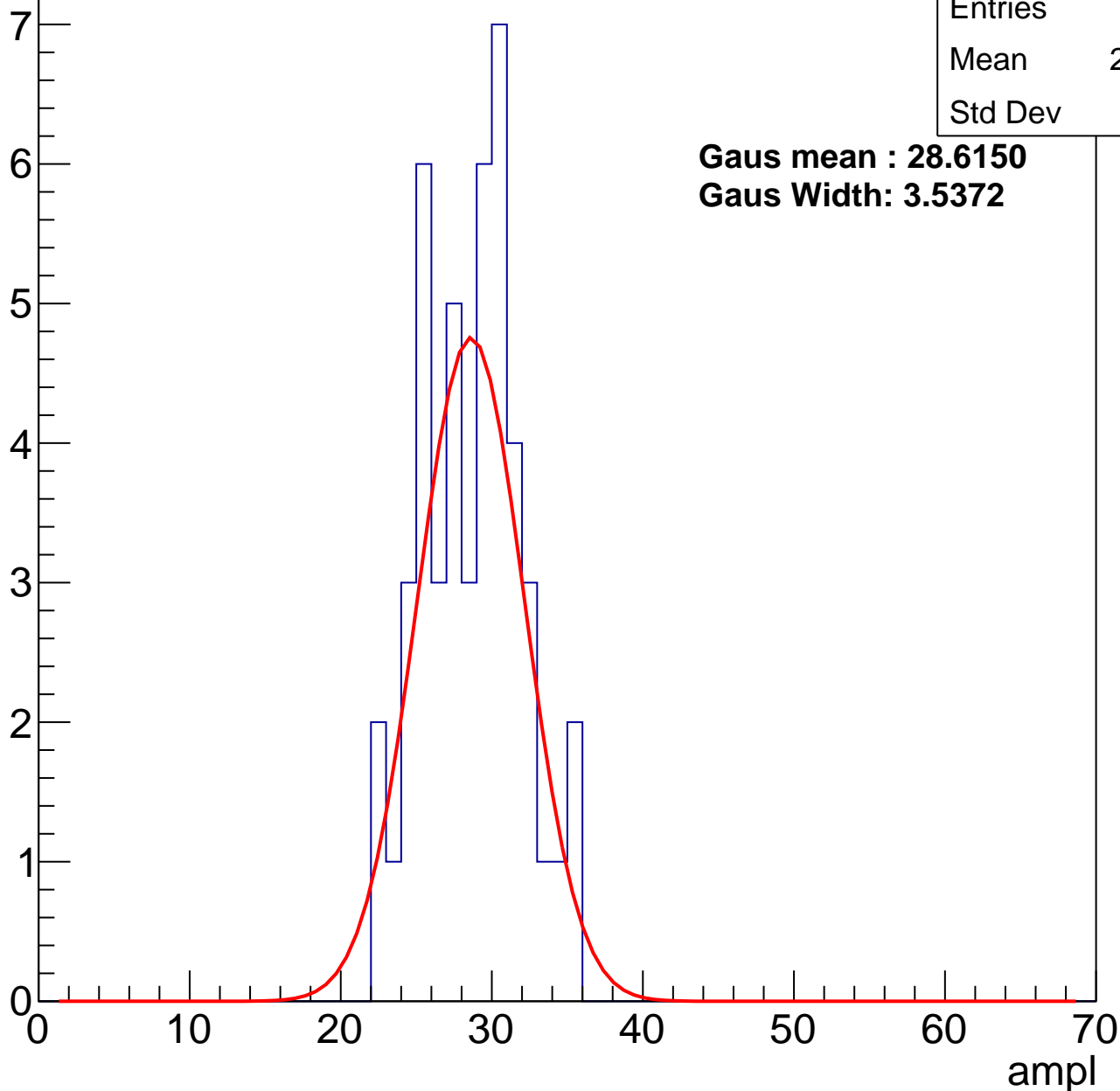
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	47
Mean	28.23
Std Dev	3.23

**Gaus mean : 28.6150**

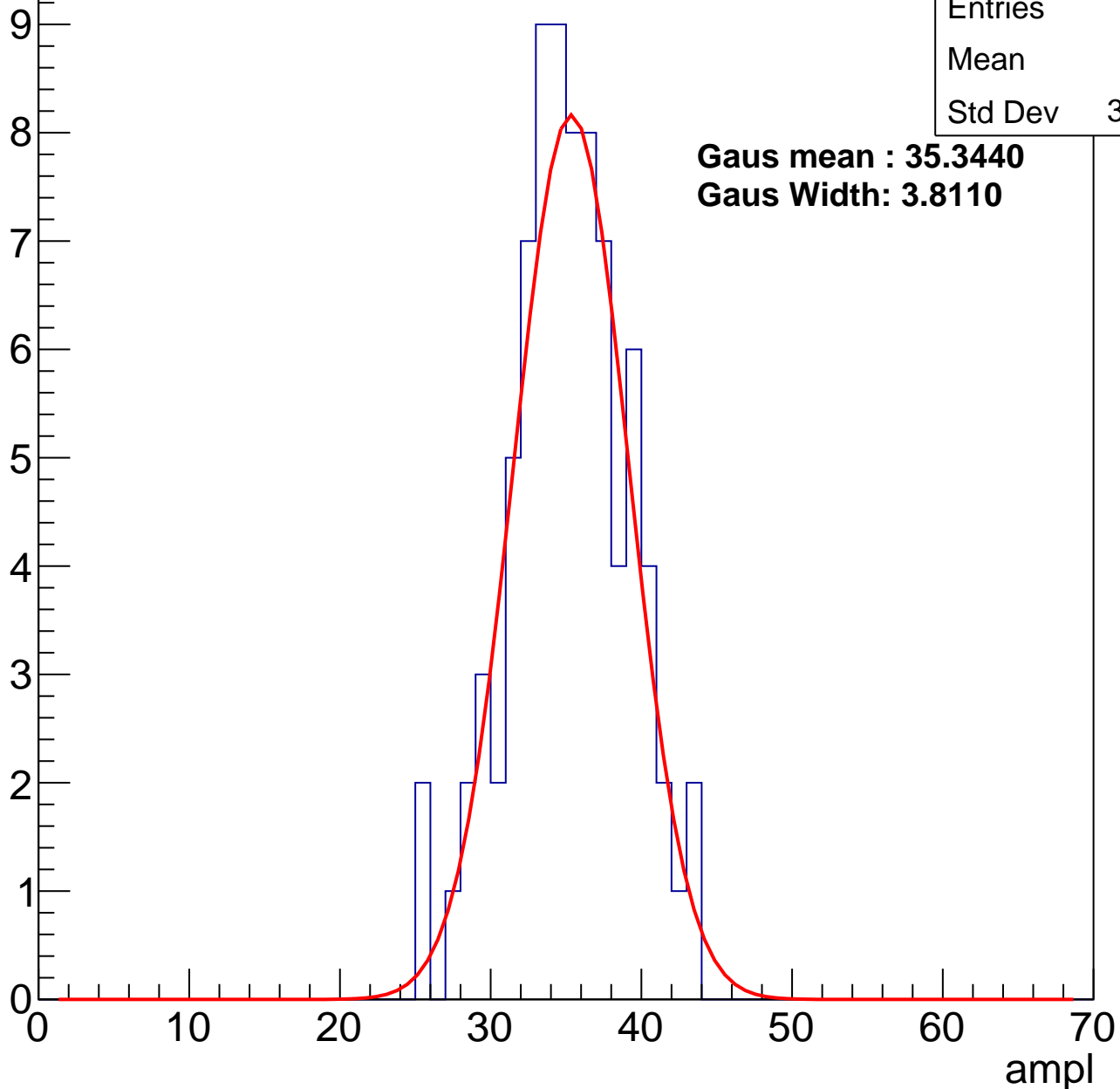
**Gaus Width: 3.5372**



# B0L000S, U7-ch1, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	82
Mean	34.7
Std Dev	3.853

**Gaus mean : 35.3440**

**Gaus Width: 3.8110**

# B0L000S, U7-ch1, adc2

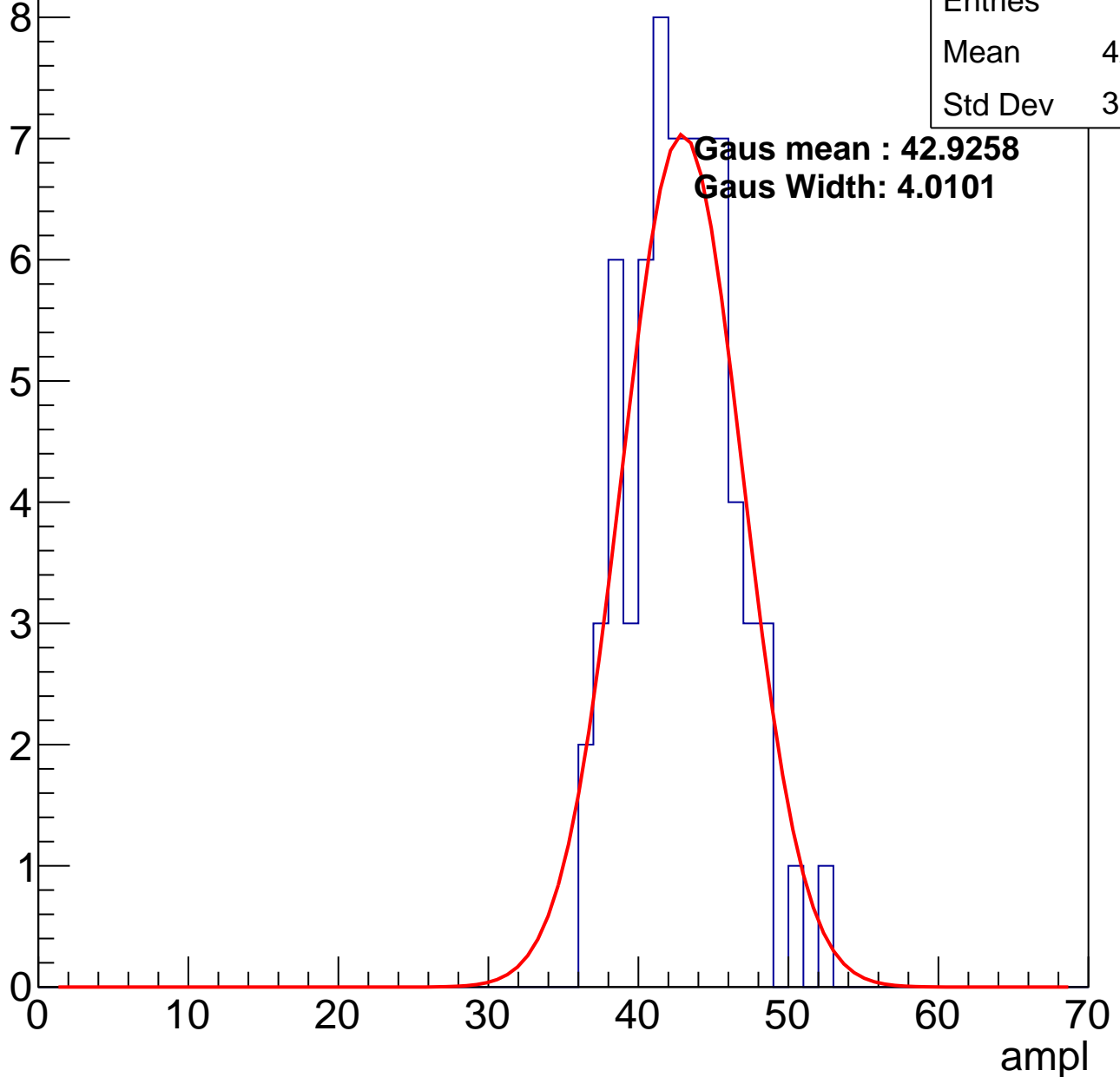
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	68
Mean	42.43
Std Dev	3.427

**Gaus mean : 42.9258**

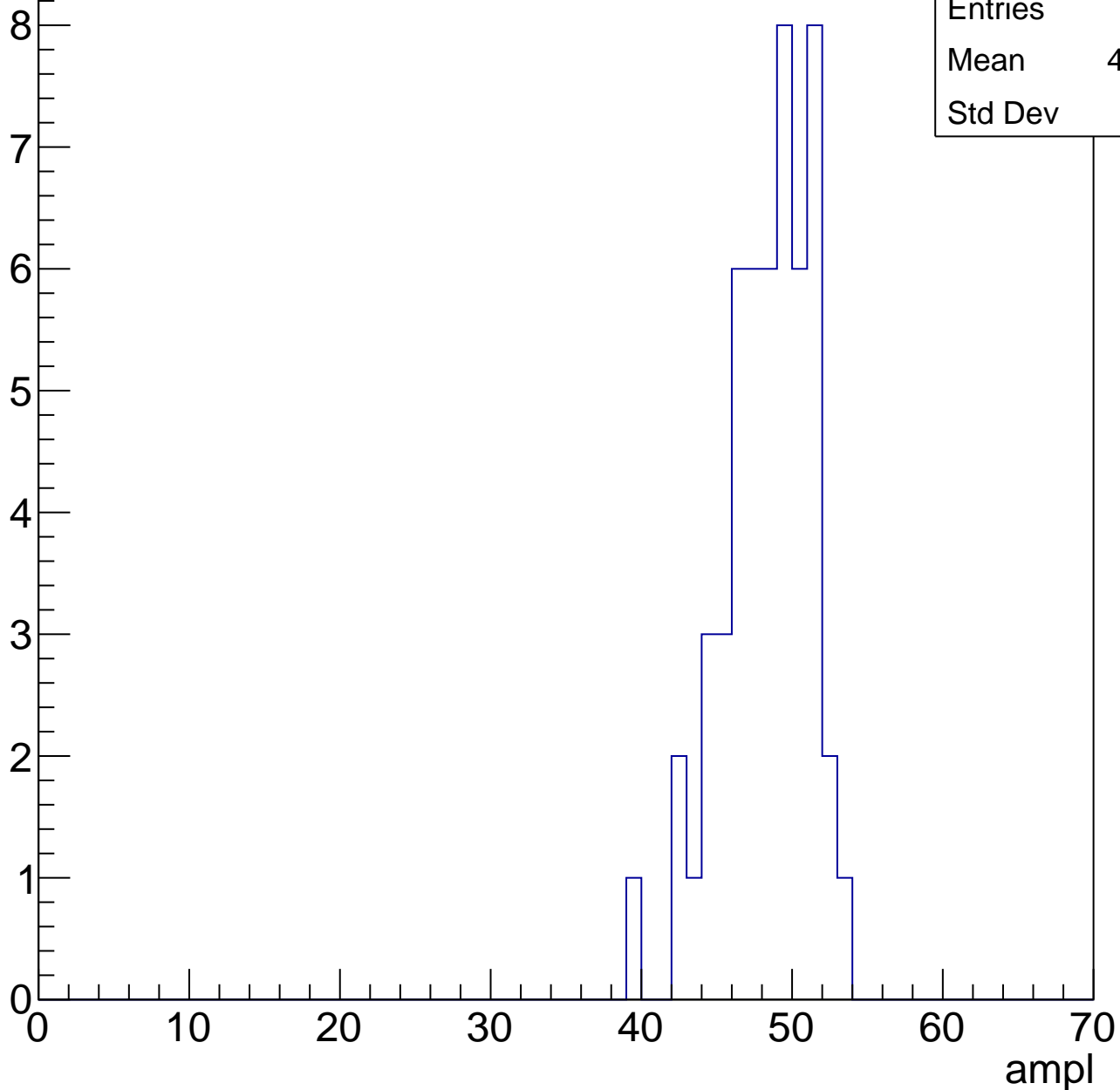
**Gaus Width: 4.0101**



# B0L000S, U7-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

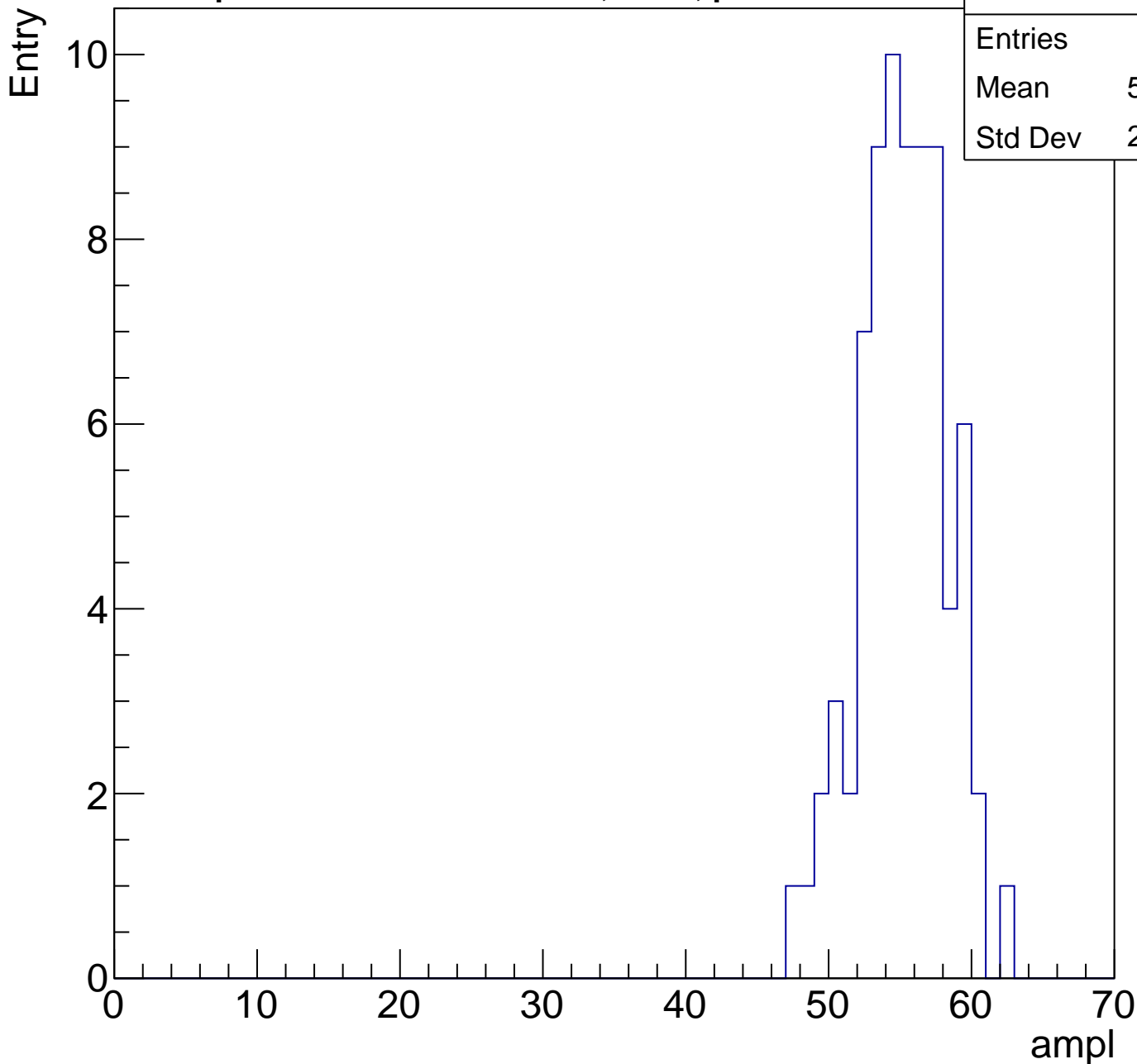
Entry



# B0L000S, U7-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	75
Mean	54.75
Std Dev	2.994



# B0L000S, U7-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	59.25
Std Dev	8.866

ampl

0

10

20

30

40

50

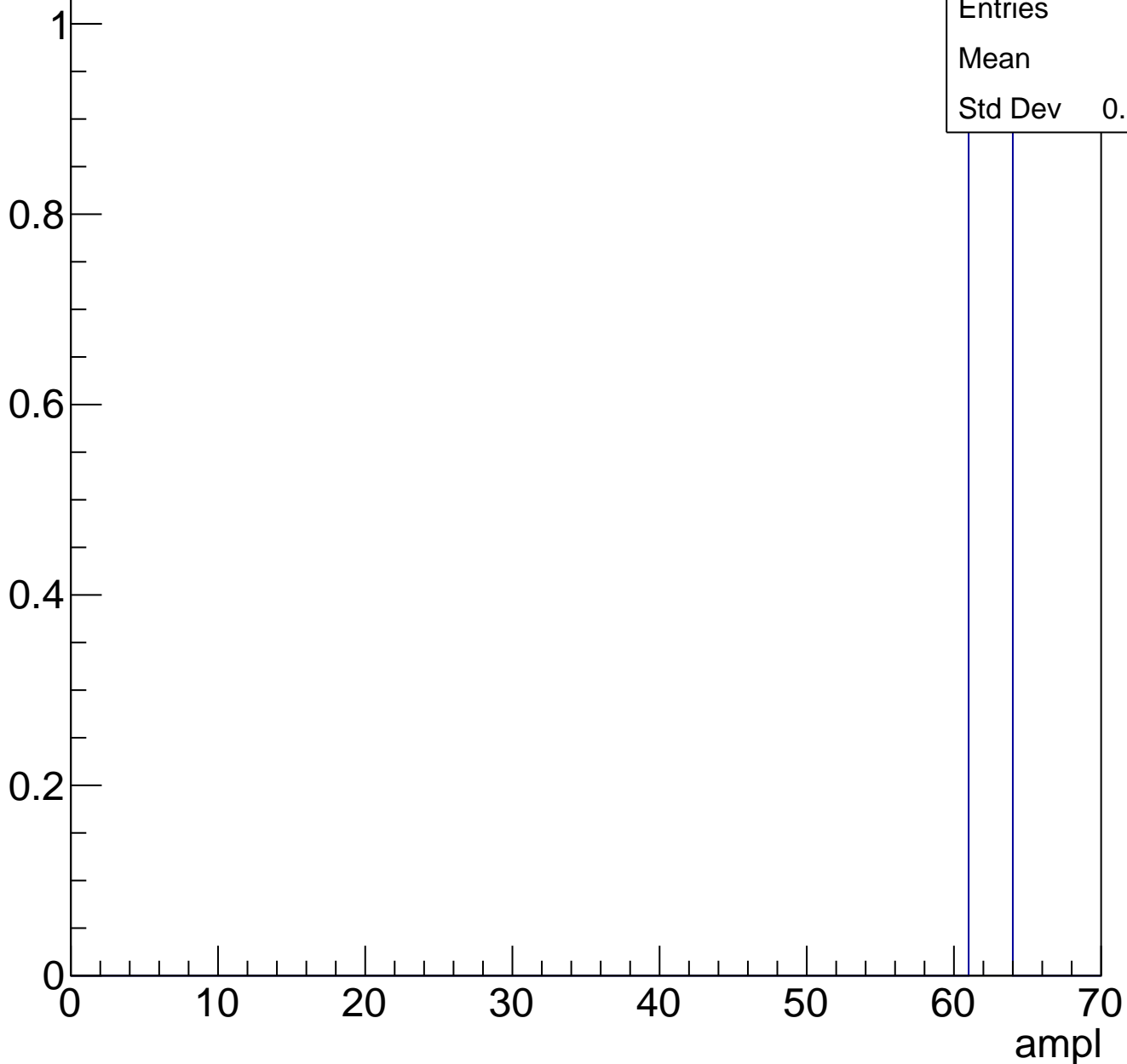
60

70

# B0L000S, U7-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

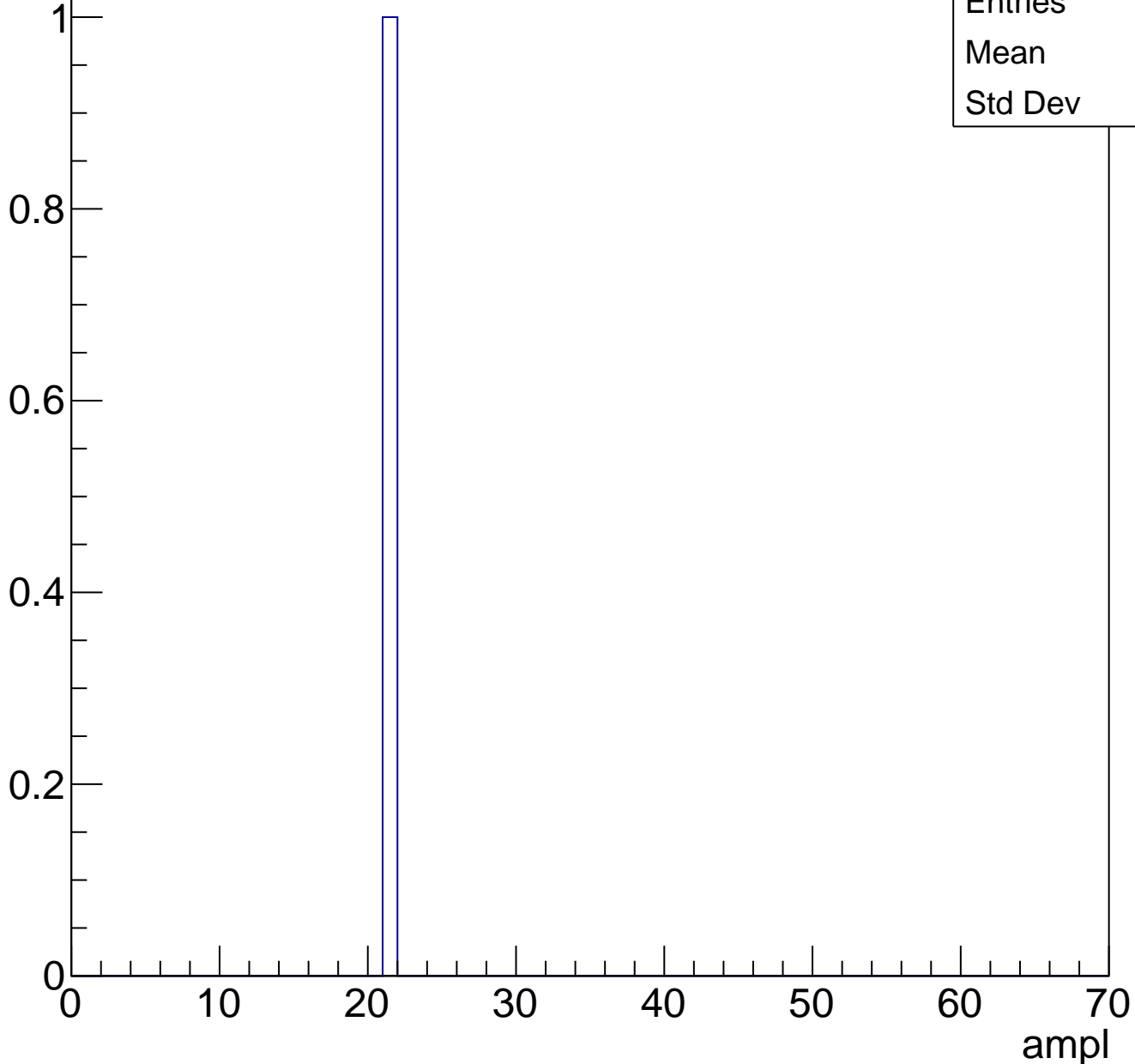




# B0L000S, U7-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	1
Mean	21
Std Dev	0

# B0L000S, U7-ch2, adc0

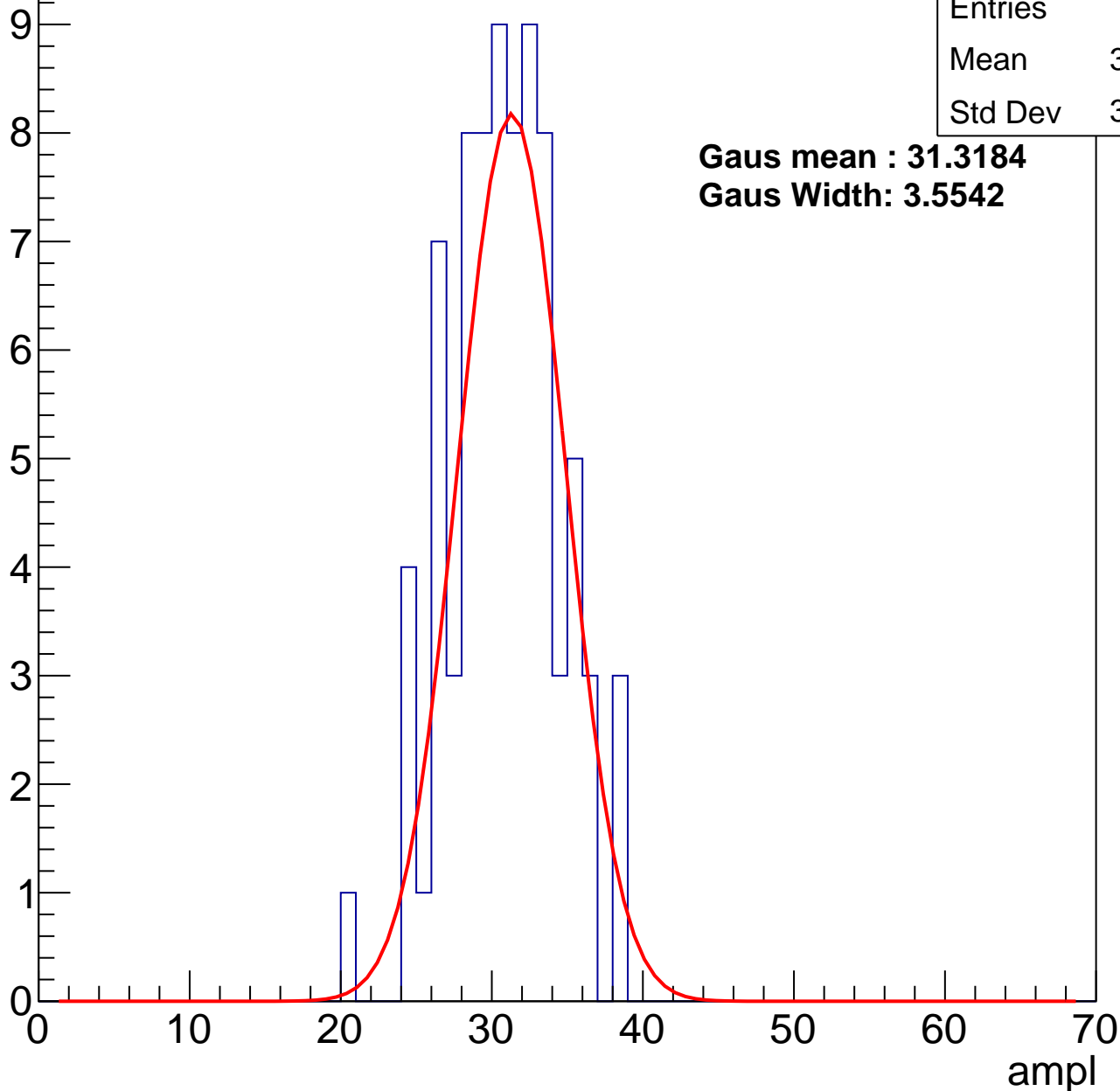
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	80
Mean	30.36
Std Dev	3.582

**Gaus mean : 31.3184**

**Gaus Width: 3.5542**



# B0L000S, U7-ch2, adc1

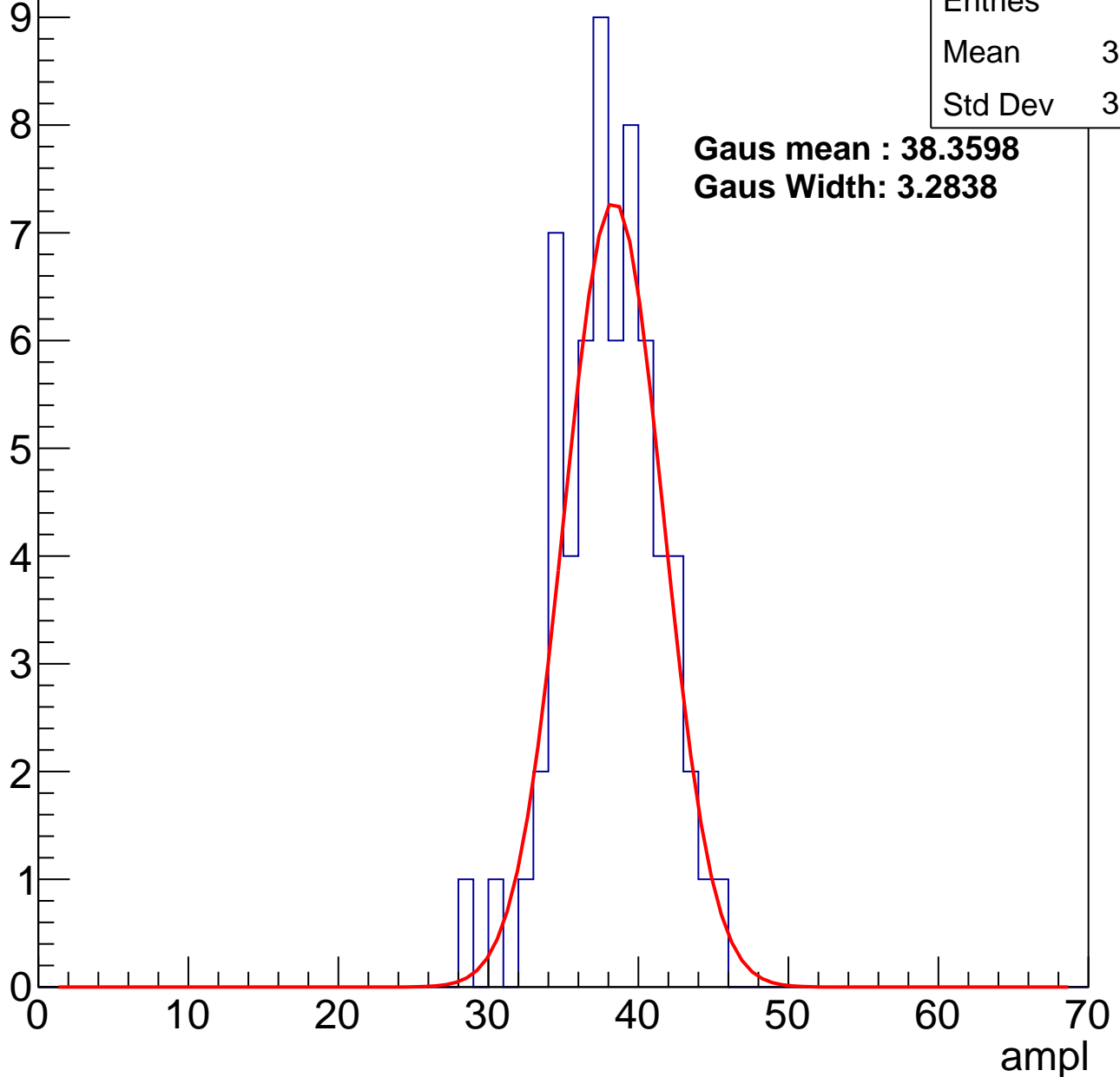
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	63
Mean	37.62
Std Dev	3.307

**Gaus mean : 38.3598**

**Gaus Width: 3.2838**



# B0L000S, U7-ch2, adc2

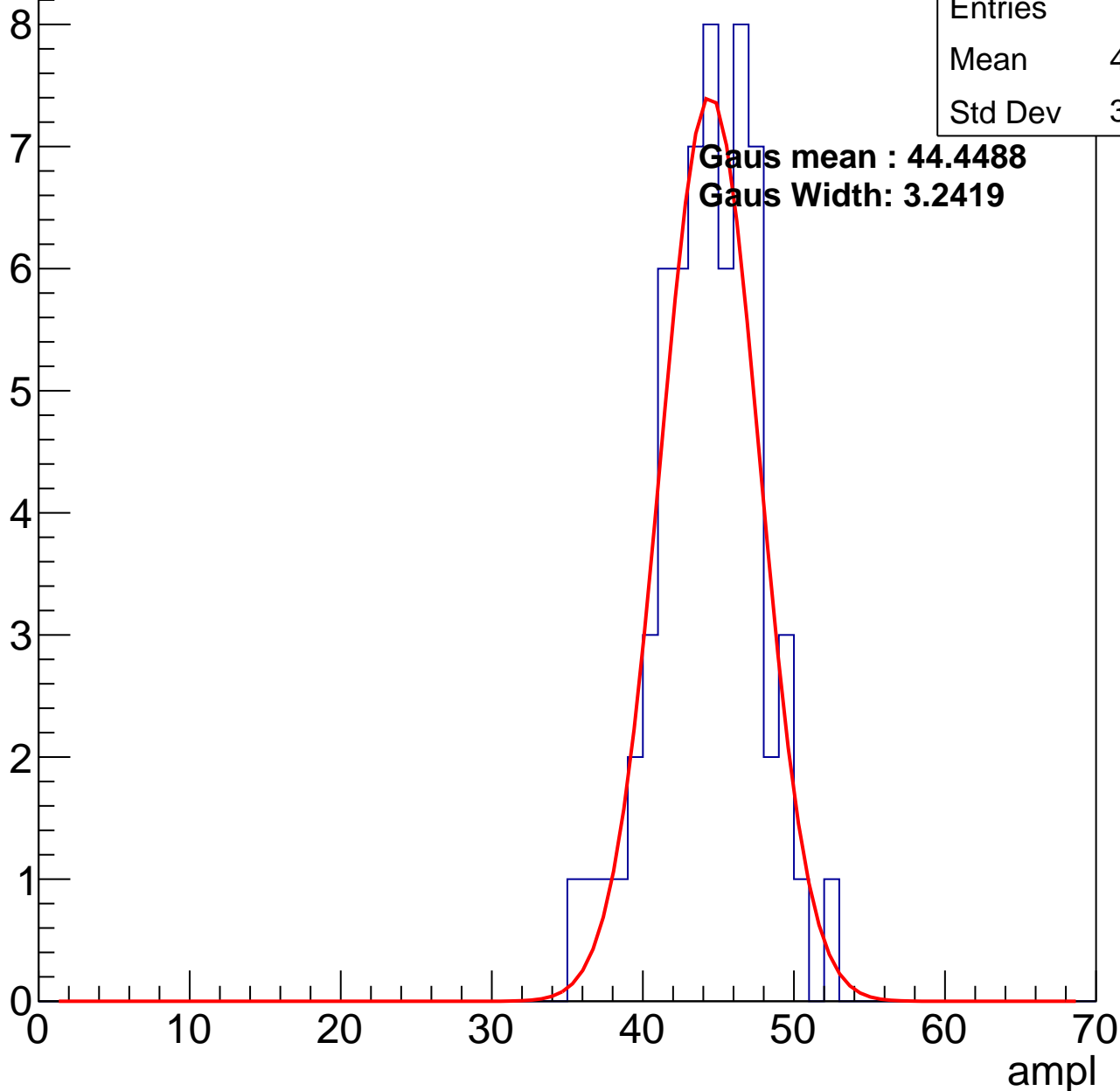
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	64
Mean	43.86
Std Dev	3.353

**Gaus mean : 44.4488**

**Gaus Width: 3.2419**

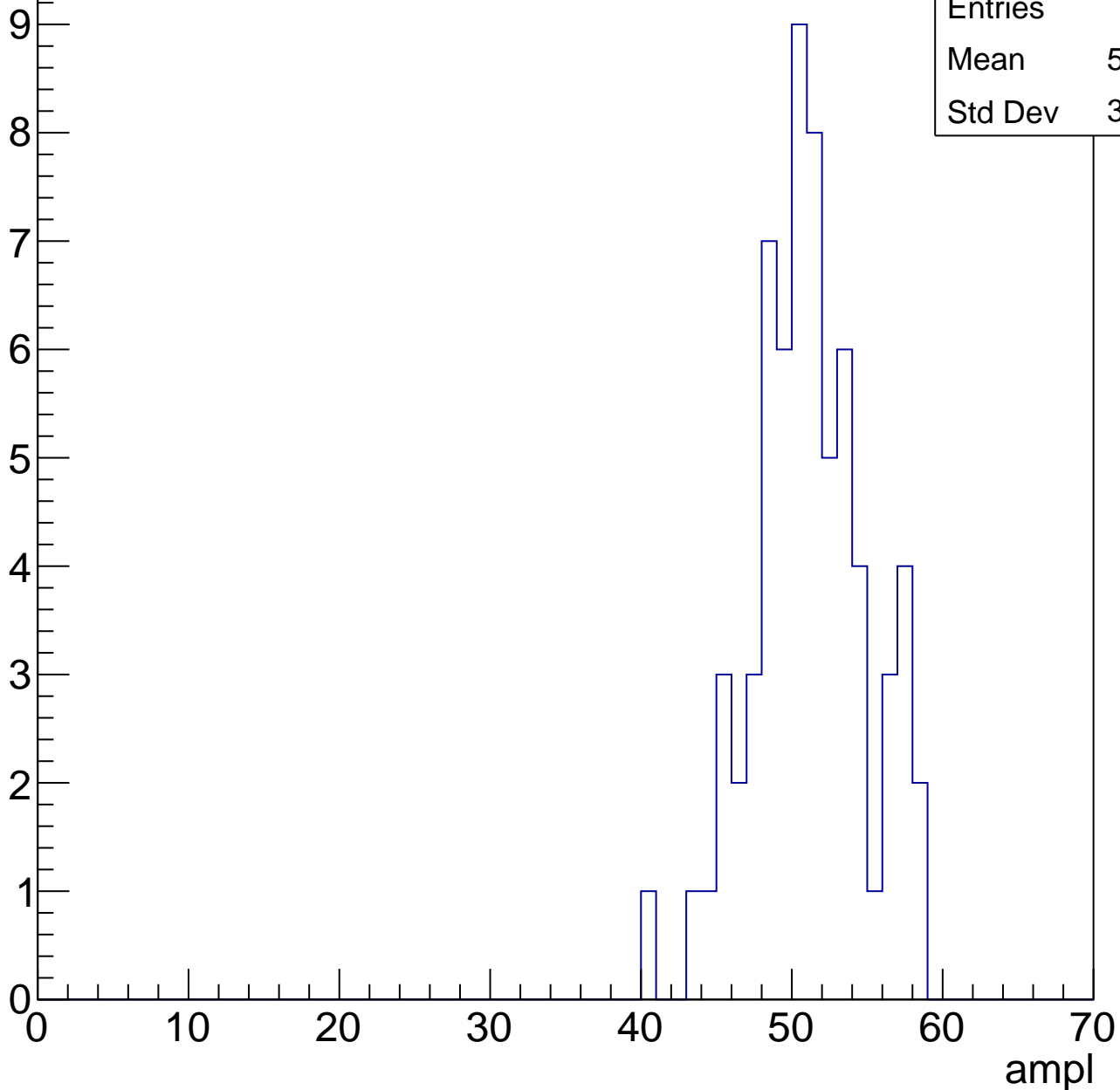


# B0L000S, U7-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	66
Mean	50.67
Std Dev	3.747

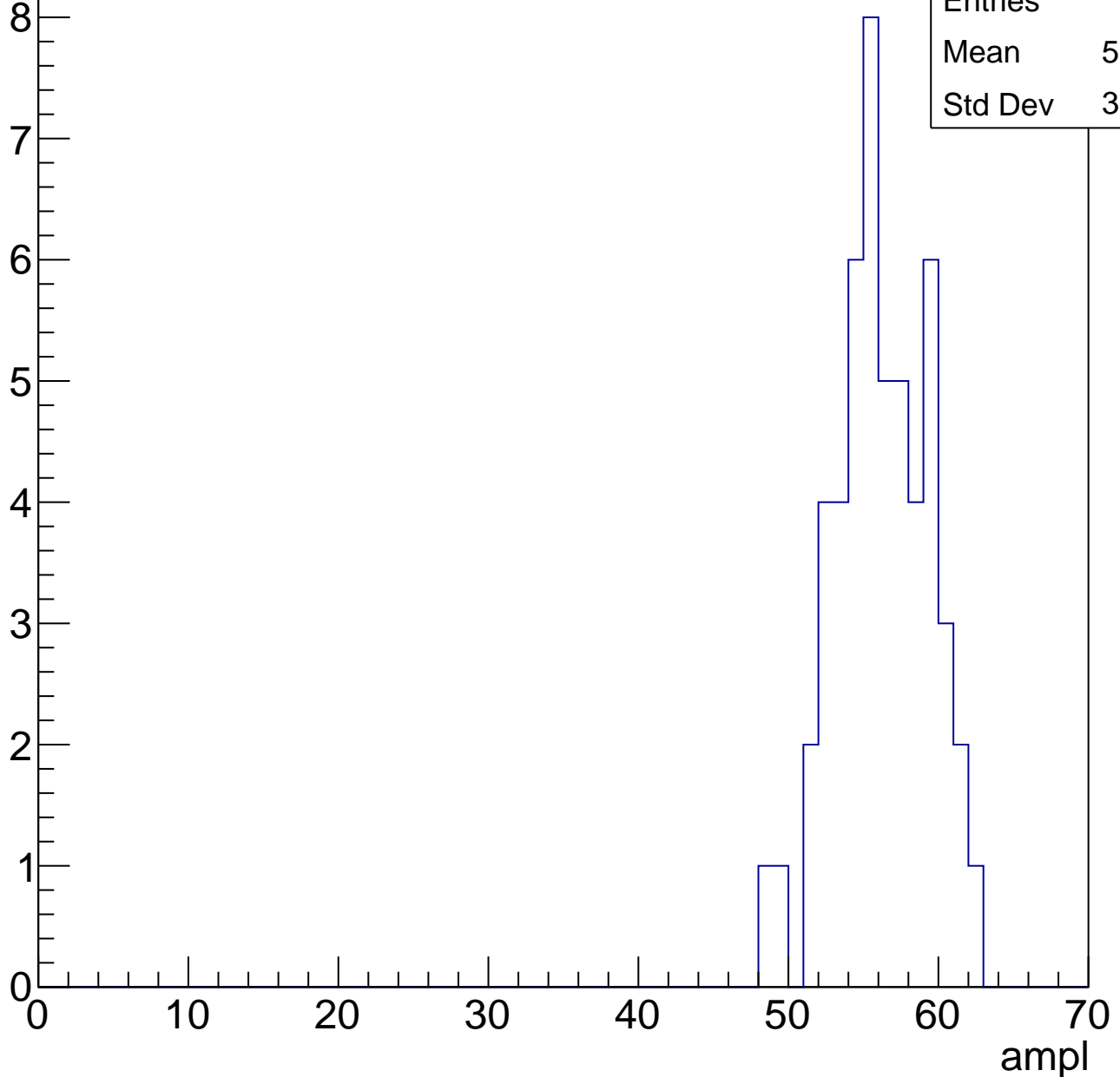


# B0L000S, U7-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

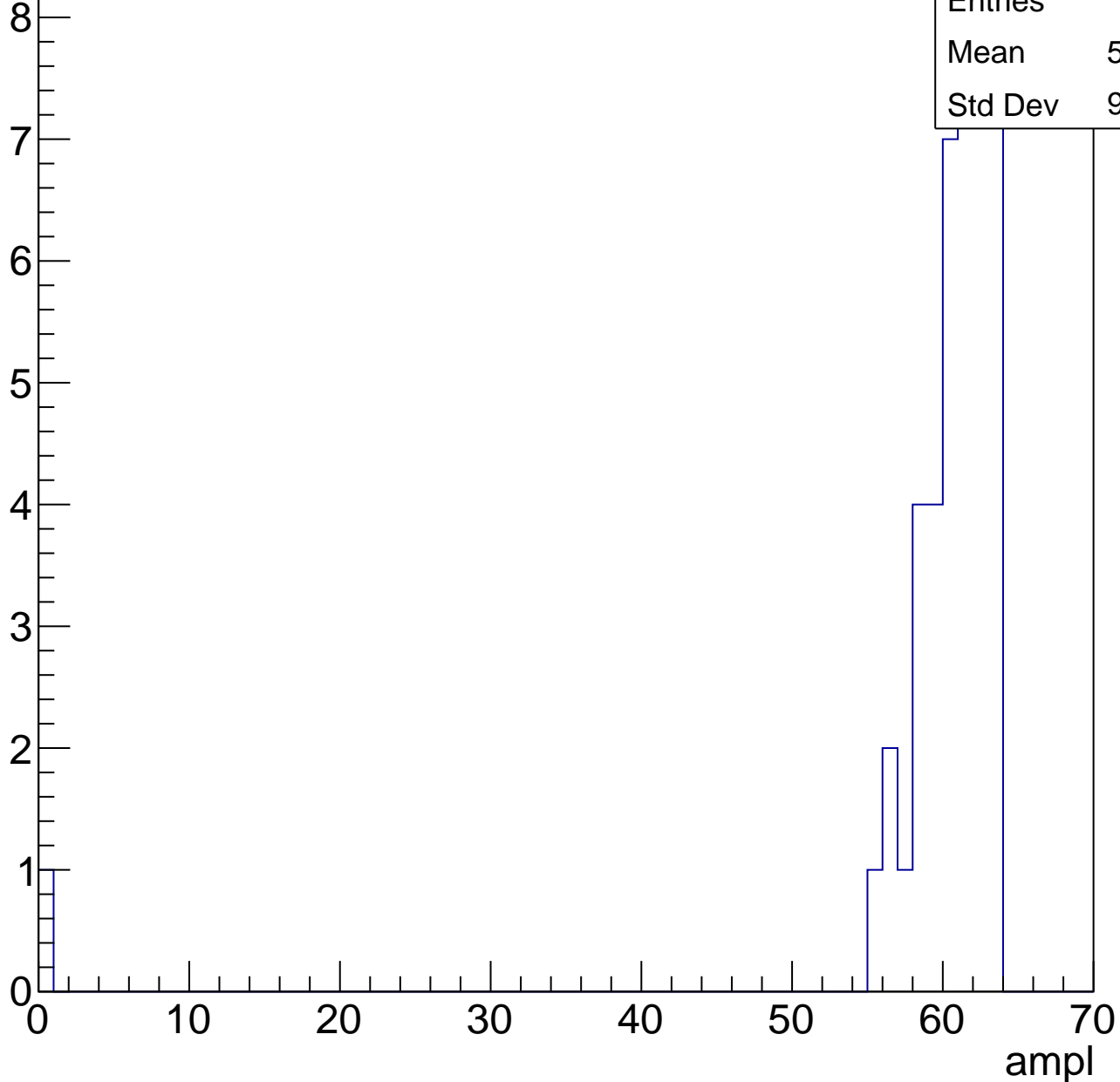
Entries	52
Mean	55.73
Std Dev	3.102



# B0L000S, U7-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

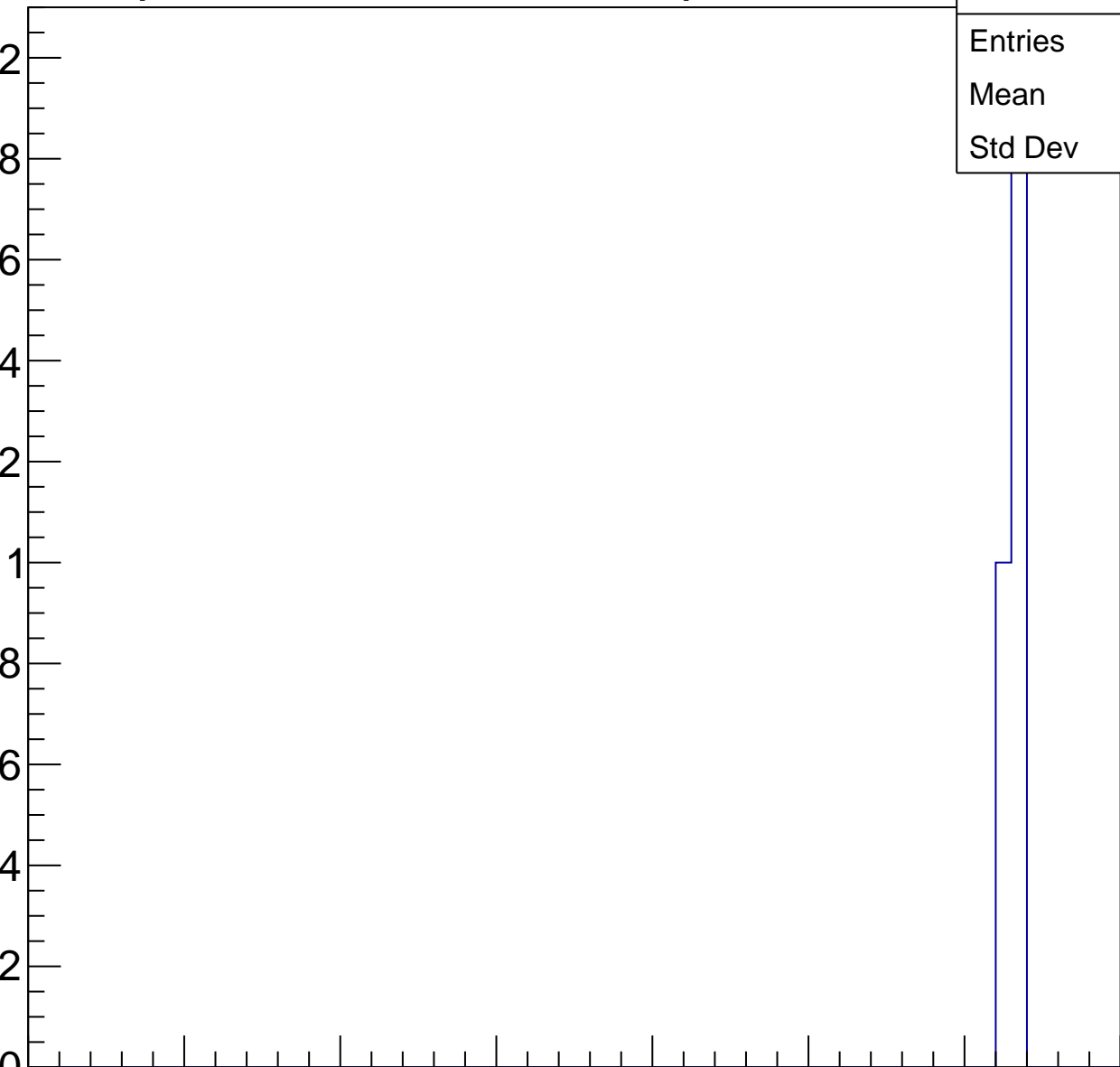
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

0 10 20 30 40 50 60 70

ampl





# B0L000S, U7-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L000S, U7-ch3, adc0

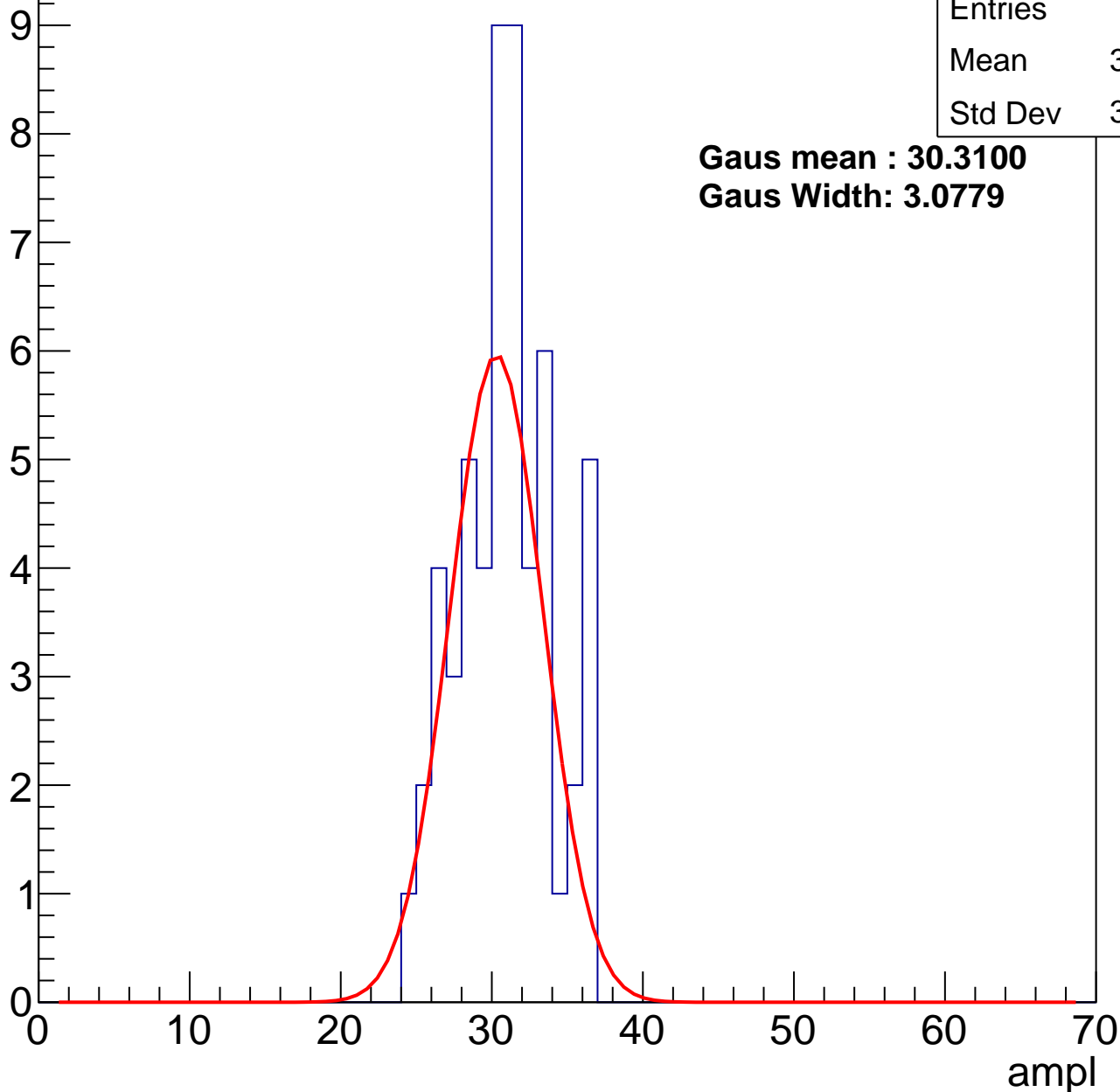
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	55
Mean	30.44
Std Dev	3.062

**Gaus mean : 30.3100**

**Gaus Width: 3.0779**



# B0L000S, U7-ch3, adc1

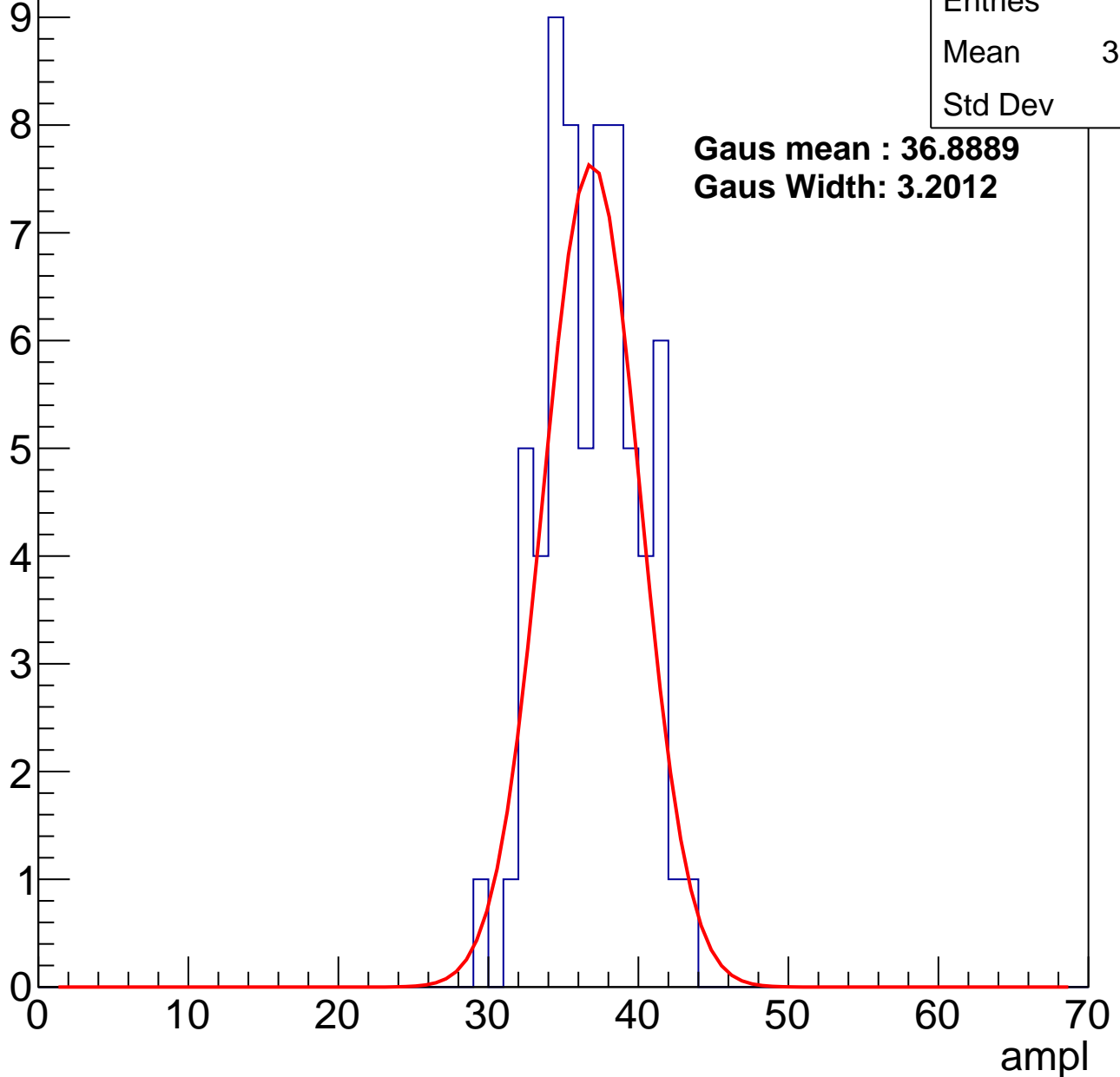
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	66
Mean	36.42
Std Dev	3.03

**Gaus mean : 36.8889**

**Gaus Width: 3.2012**



# B0L000S, U7-ch3, adc2

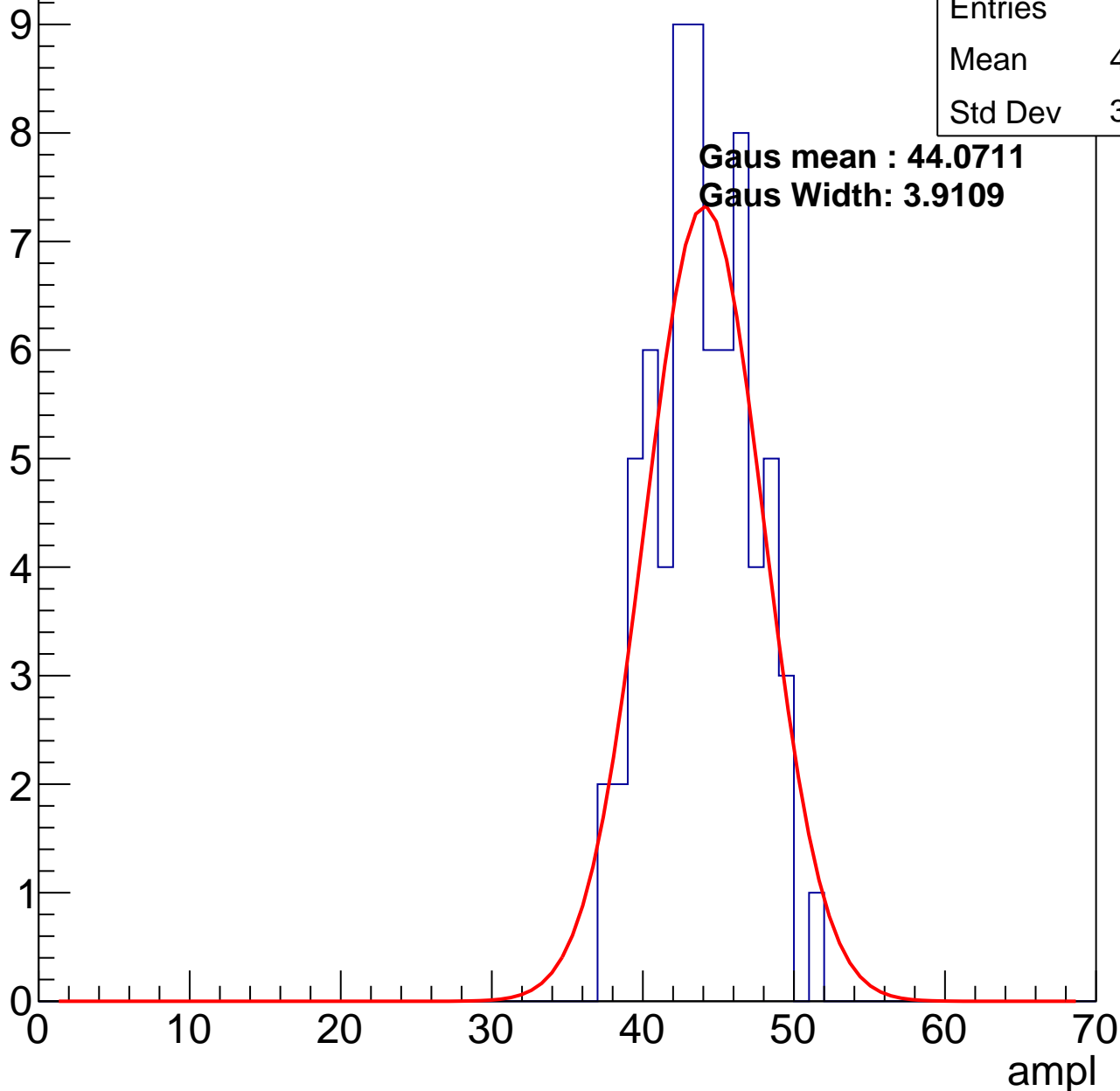
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	70
Mean	43.46
Std Dev	3.228

**Gaus mean : 44.0711**

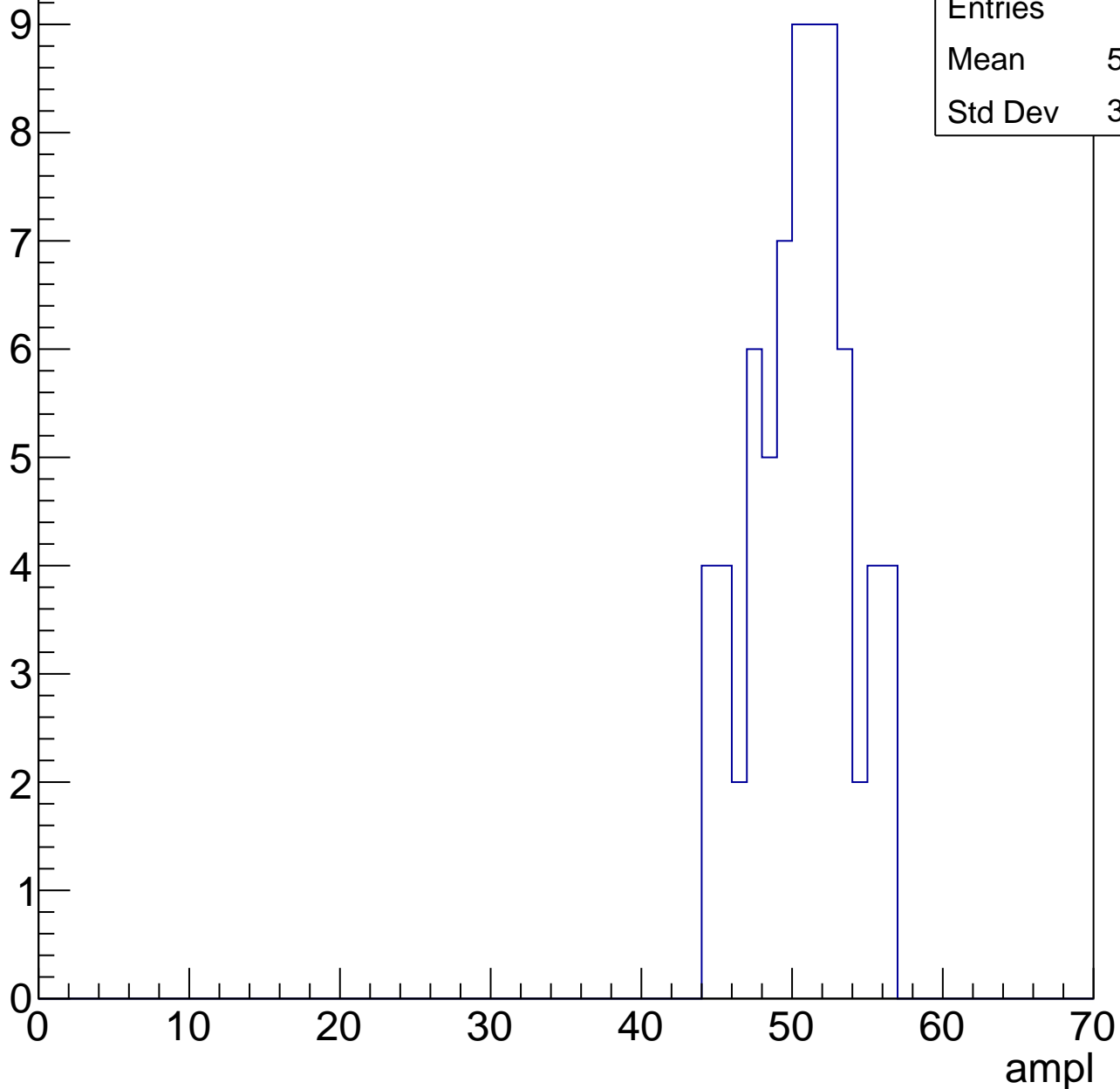
**Gaus Width: 3.9109**



# B0L000S, U7-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



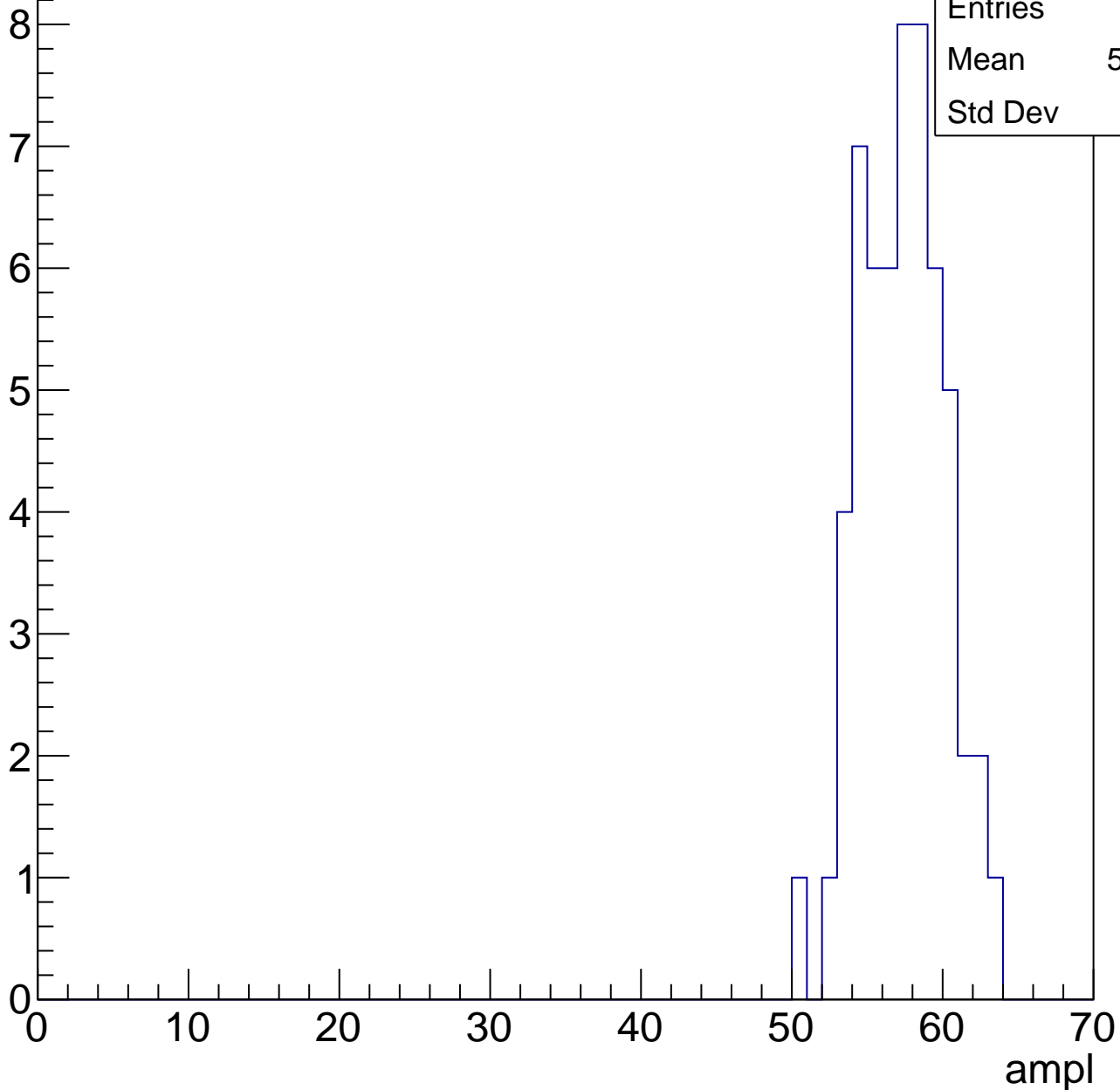
Entries	71
Mean	50.14
Std Dev	3.208

# B0L000S, U7-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	57
Mean	56.86
Std Dev	2.73

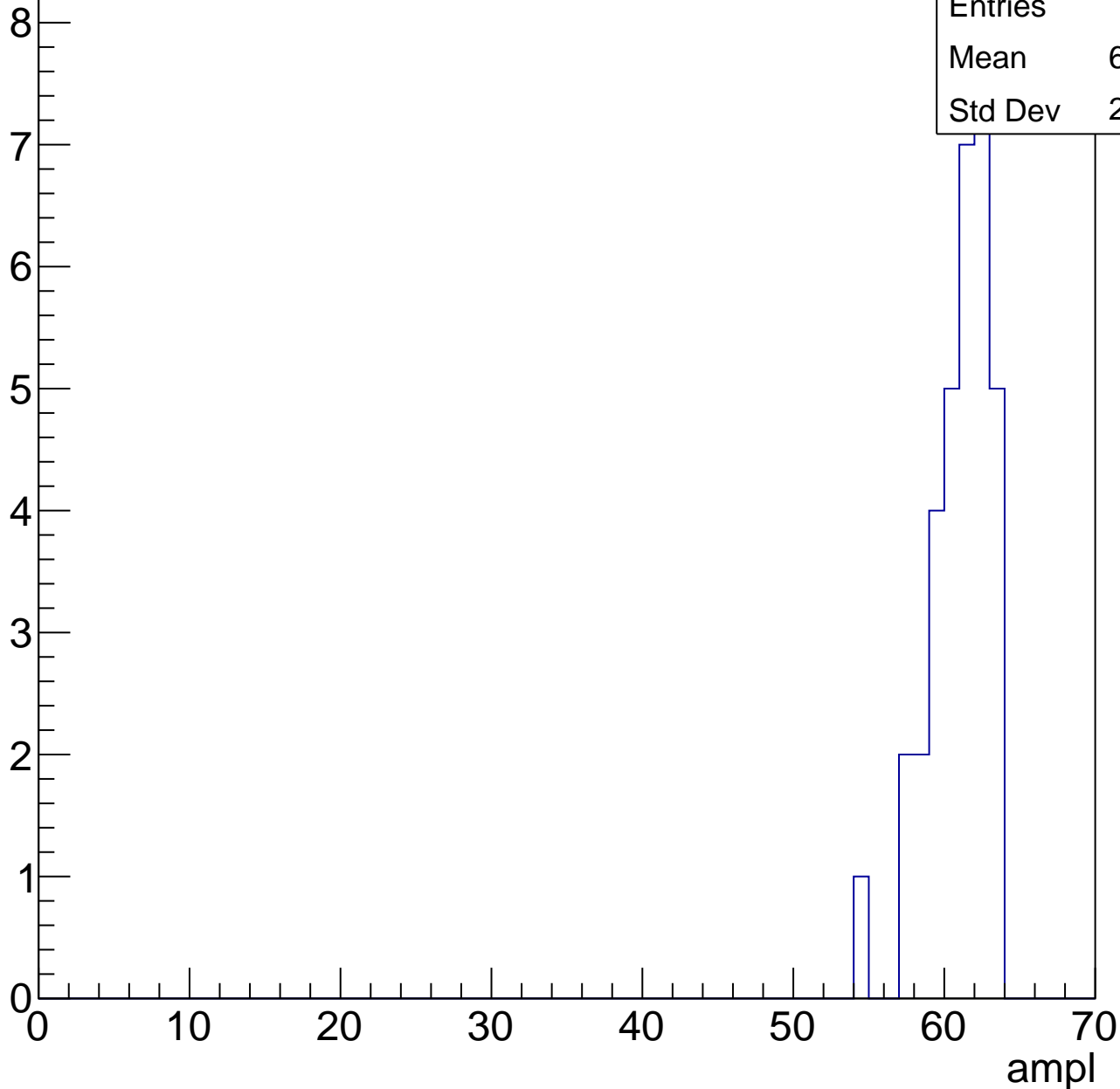


# B0L000S, U7-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

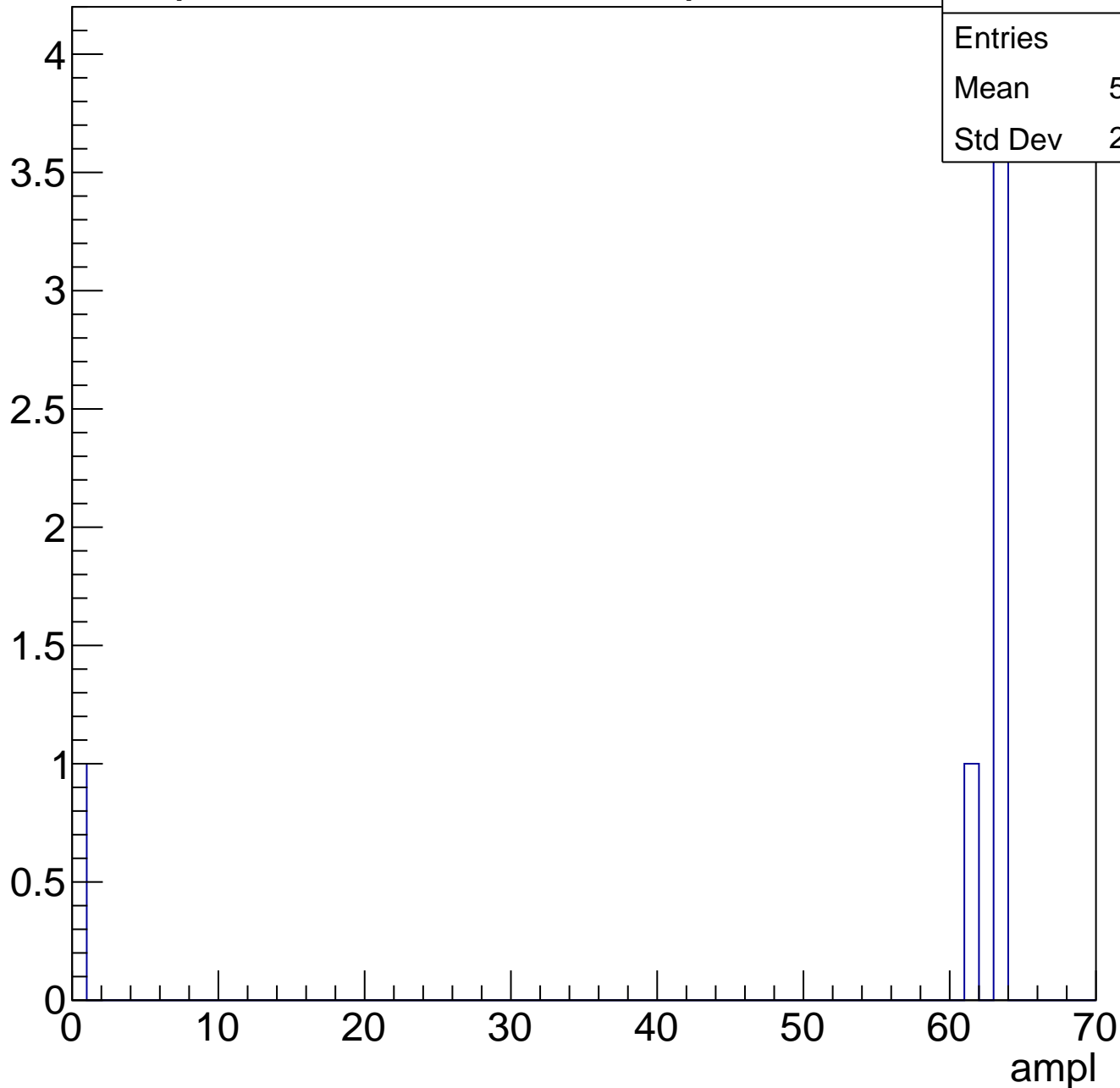
Entries	34
Mean	60.53
Std Dev	2.033



# B0L000S, U7-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

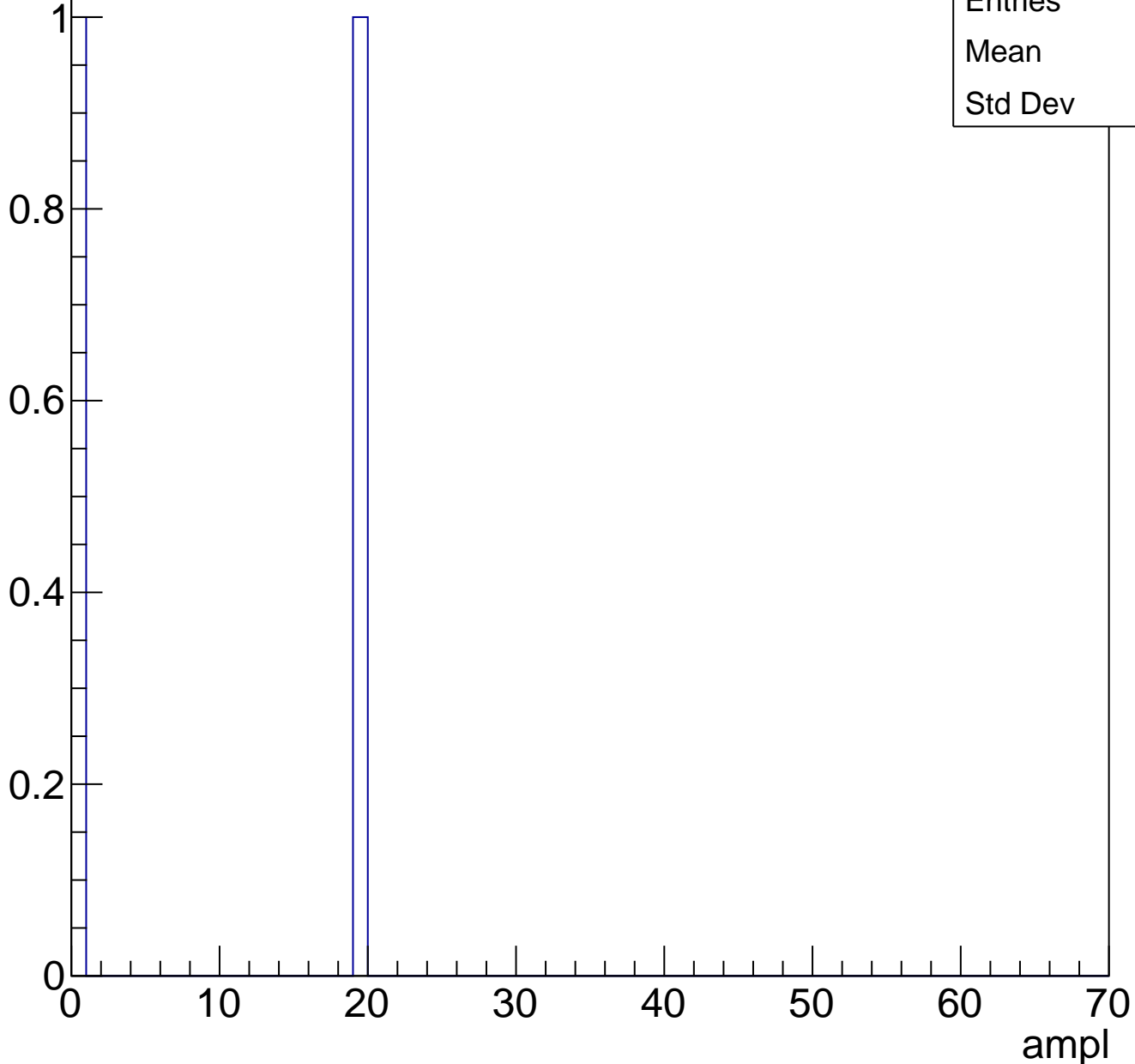




# B0L000S, U7-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	2
Mean	9.5
Std Dev	9.5

# B0L000S, U7-ch4, adc0

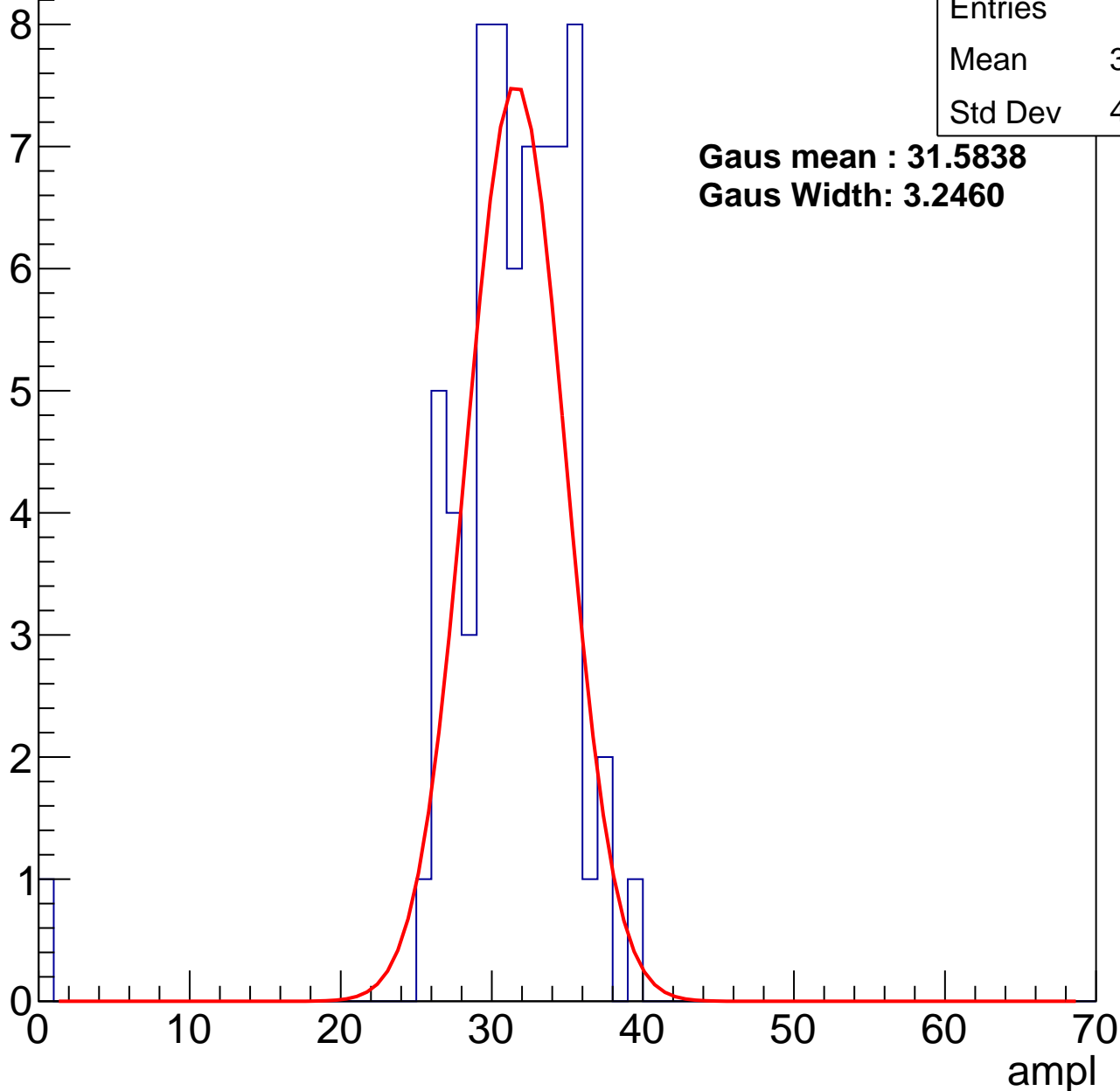
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	69
Mean	30.83
Std Dev	4.872

**Gaus mean : 31.5838**

**Gaus Width: 3.2460**



# B0L000S, U7-ch4, adc1

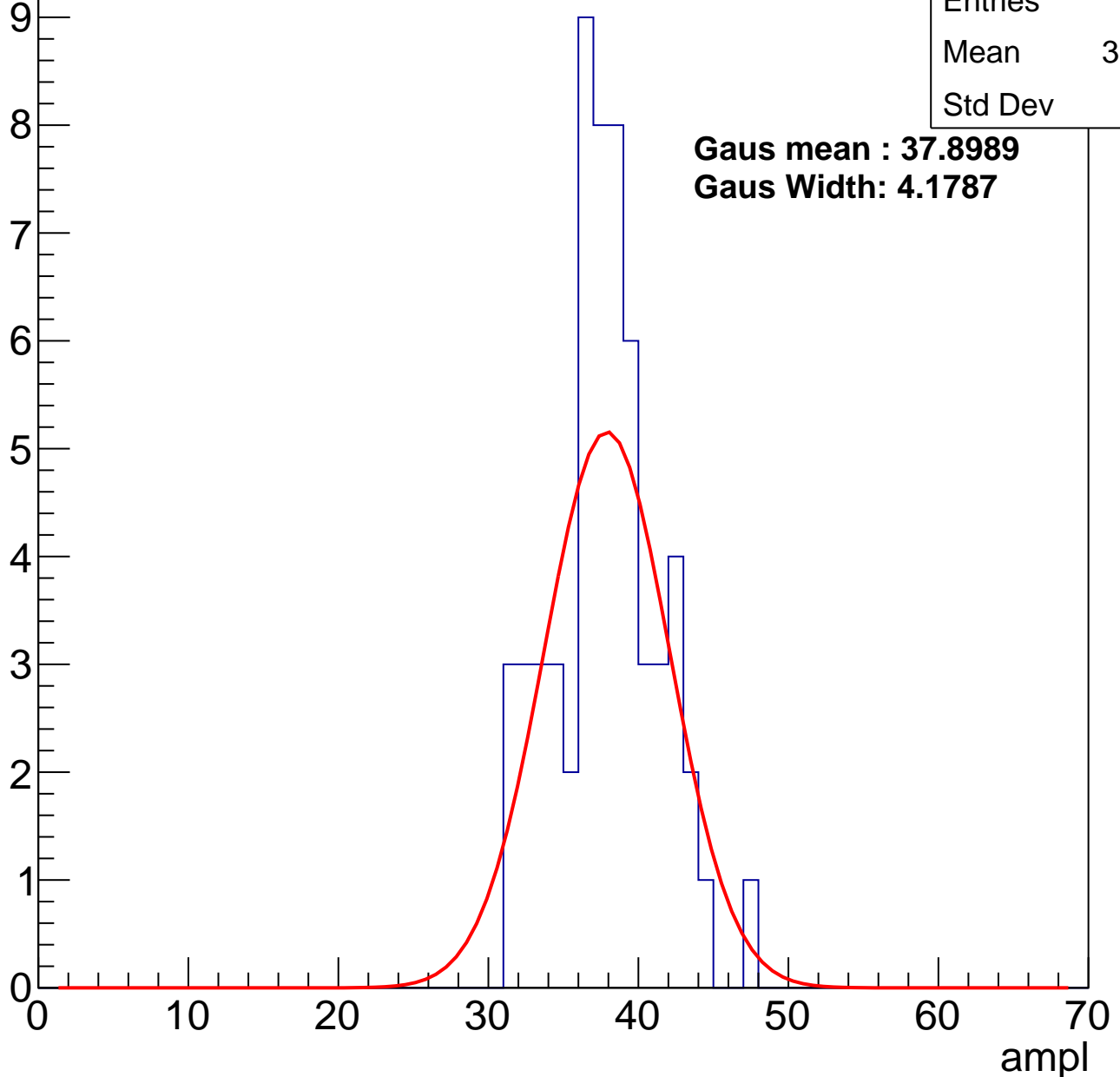
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	59
Mean	37.39
Std Dev	3.43

**Gaus mean : 37.8989**

**Gaus Width: 4.1787**



# B0L000S, U7-ch4, adc2

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	75
Mean	44.12
Std Dev	3.081

**Gaus mean : 44.3981**

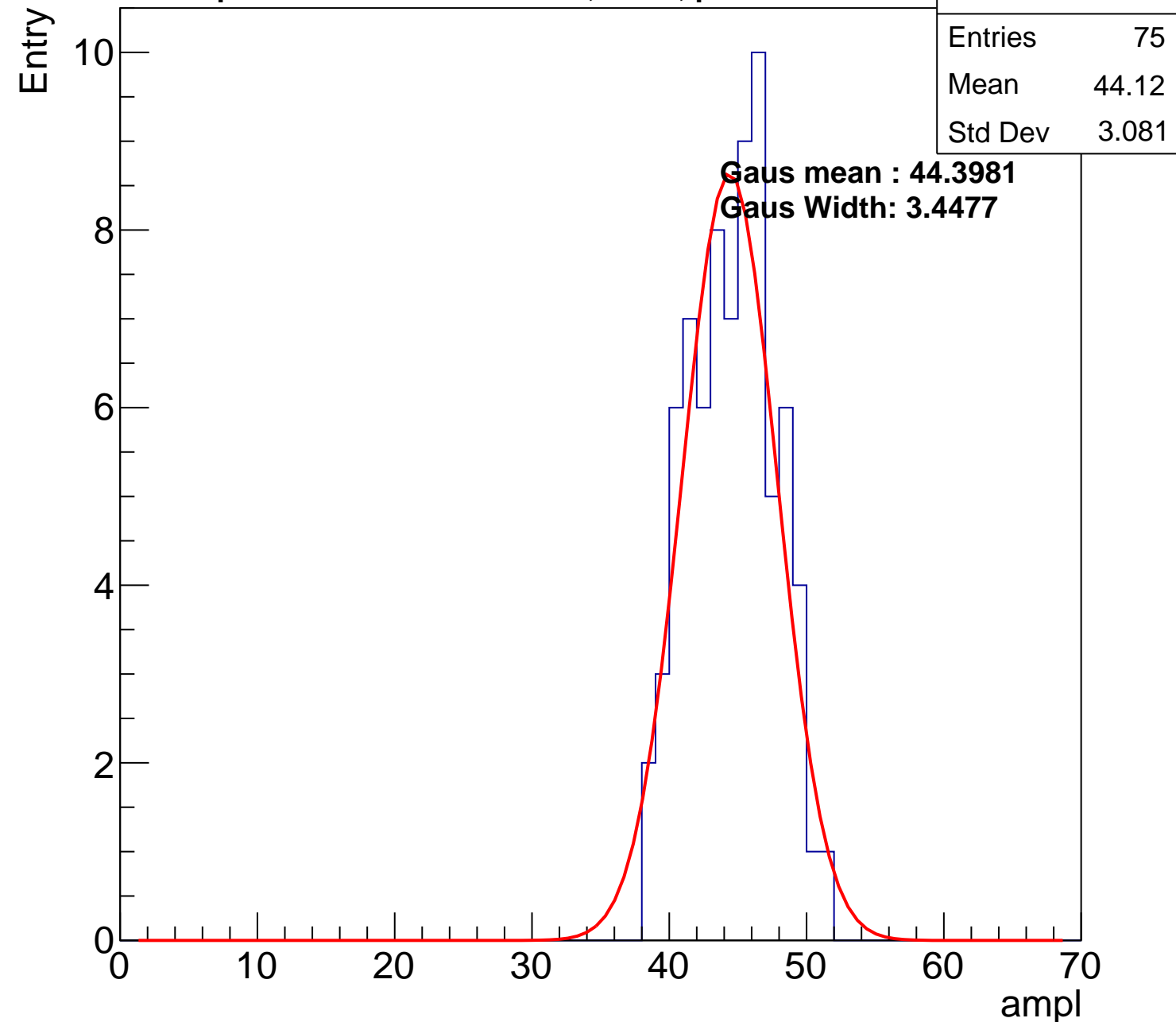
**Gaus Width: 3.4477**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L000S, U7-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

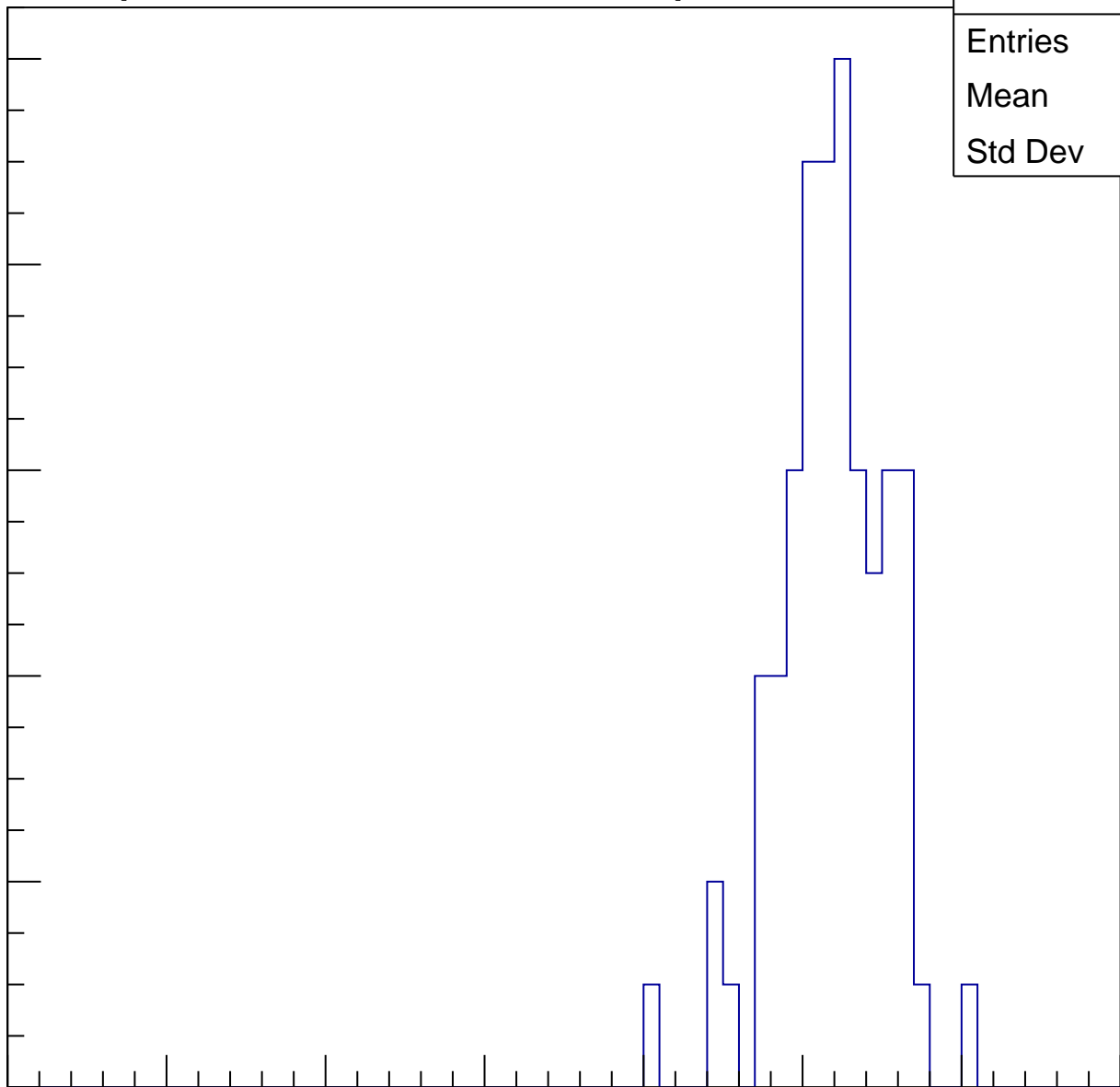
Entries	71
Mean	51.37
Std Dev	3.399

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

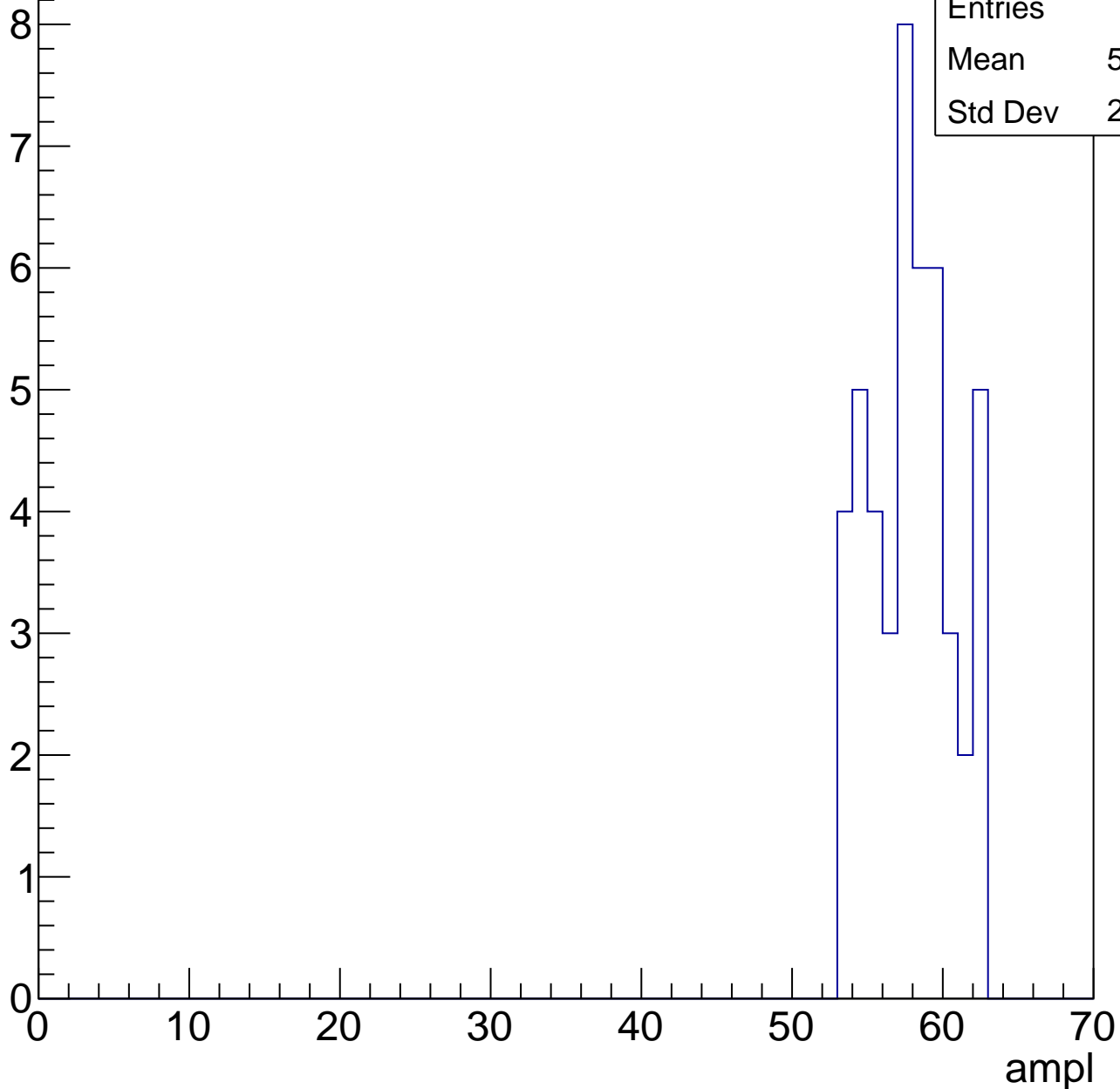
ampl



# B0L000S, U7-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

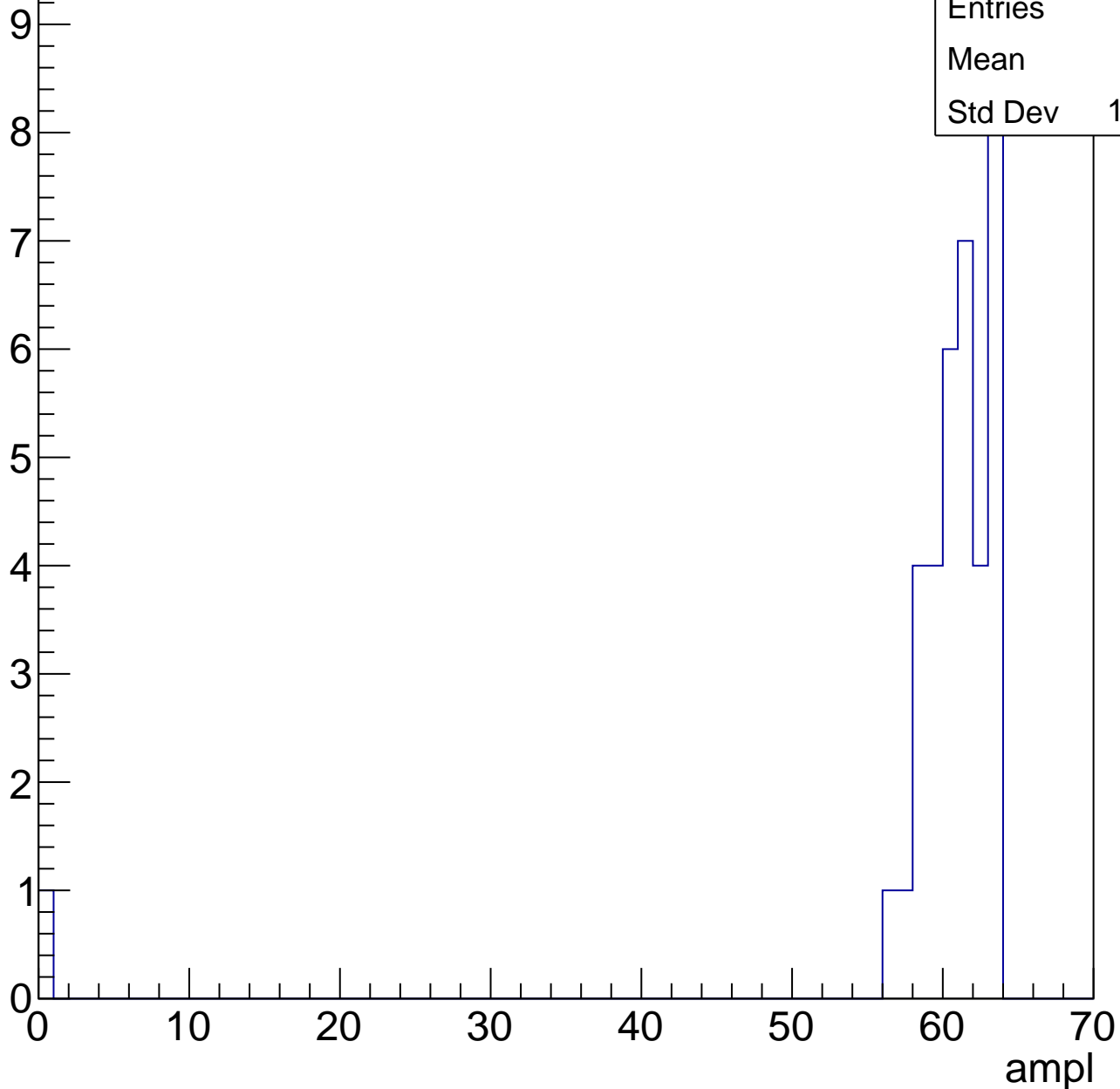


# B0L000S, U7-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

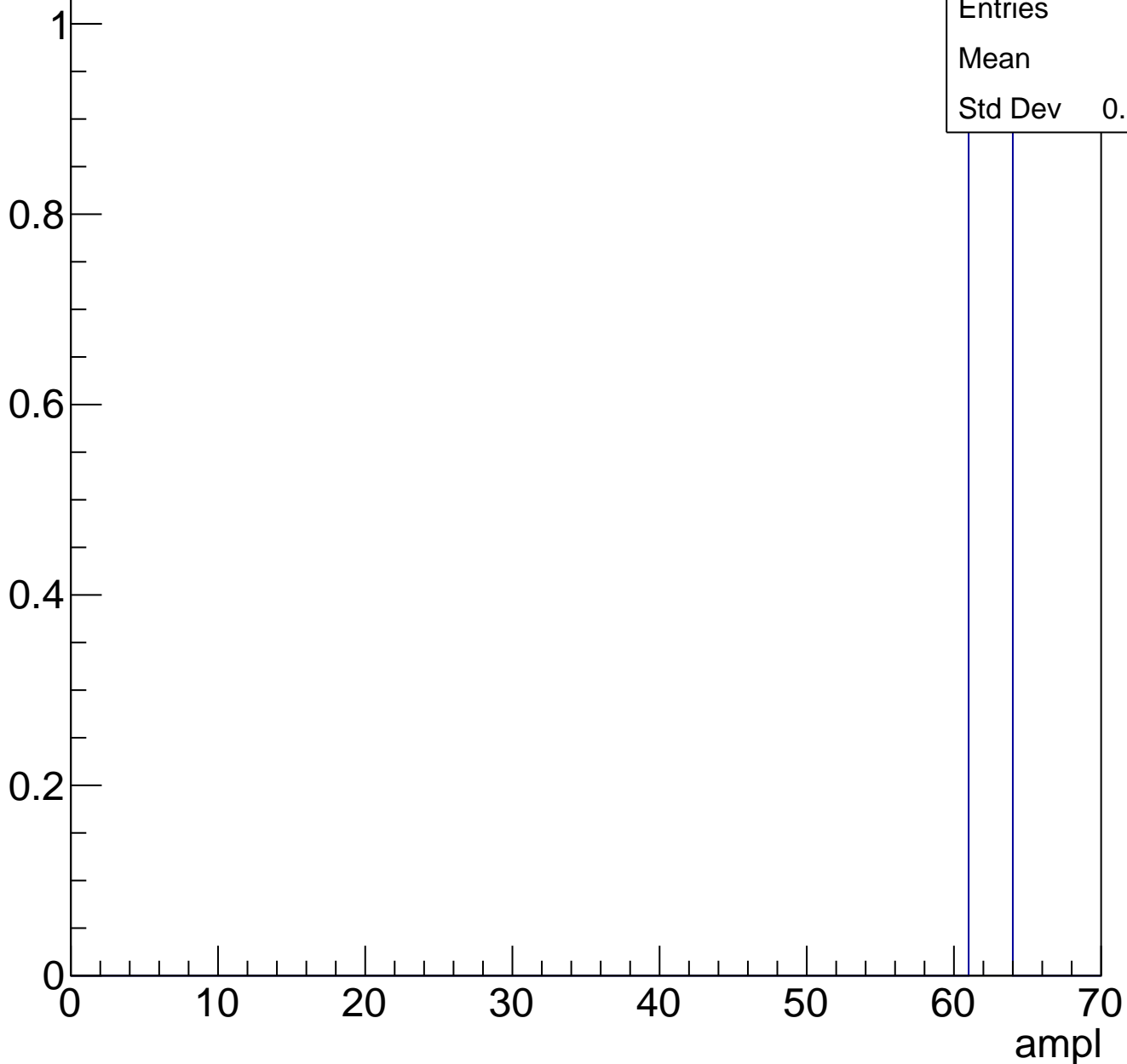
Entries	37
Mean	59
Std Dev	10.02



# B0L000S, U7-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch5, adc0

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	93
Mean	30.09
Std Dev	5.696

**Gaus mean : 30.7715**

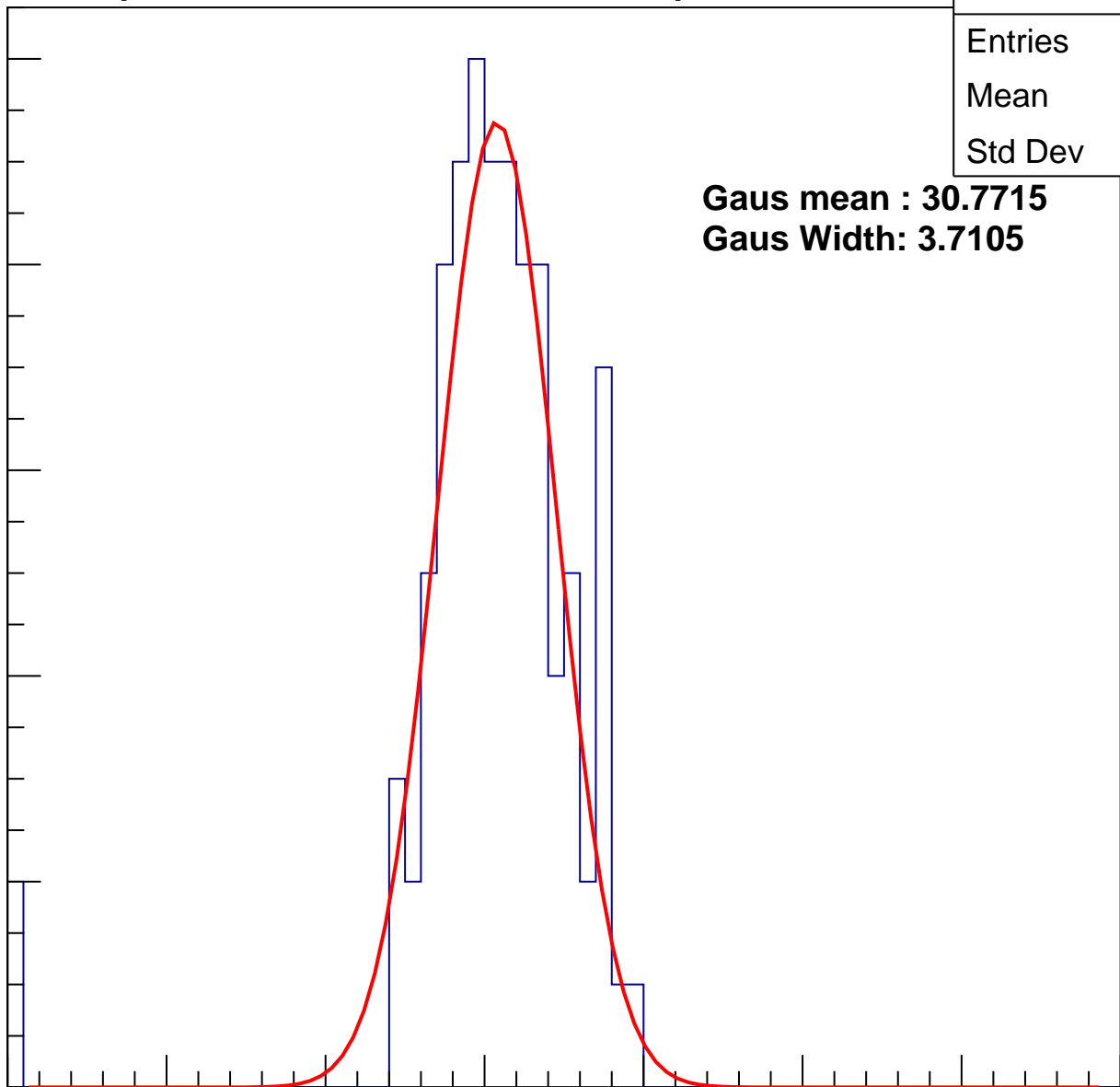
**Gaus Width: 3.7105**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L000S, U7-ch5, adc1

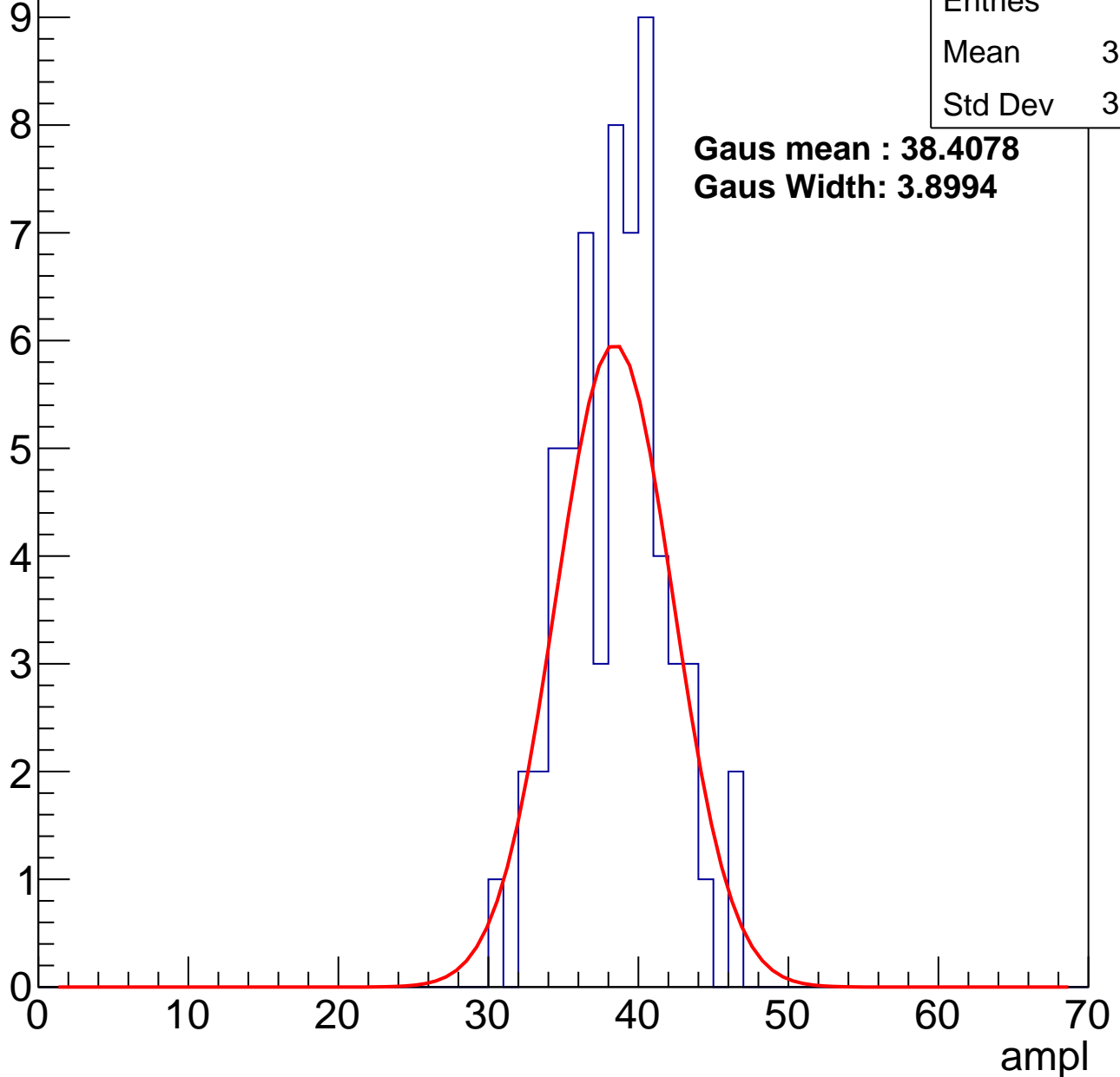
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	62
Mean	38.06
Std Dev	3.379

**Gaus mean : 38.4078**

**Gaus Width: 3.8994**



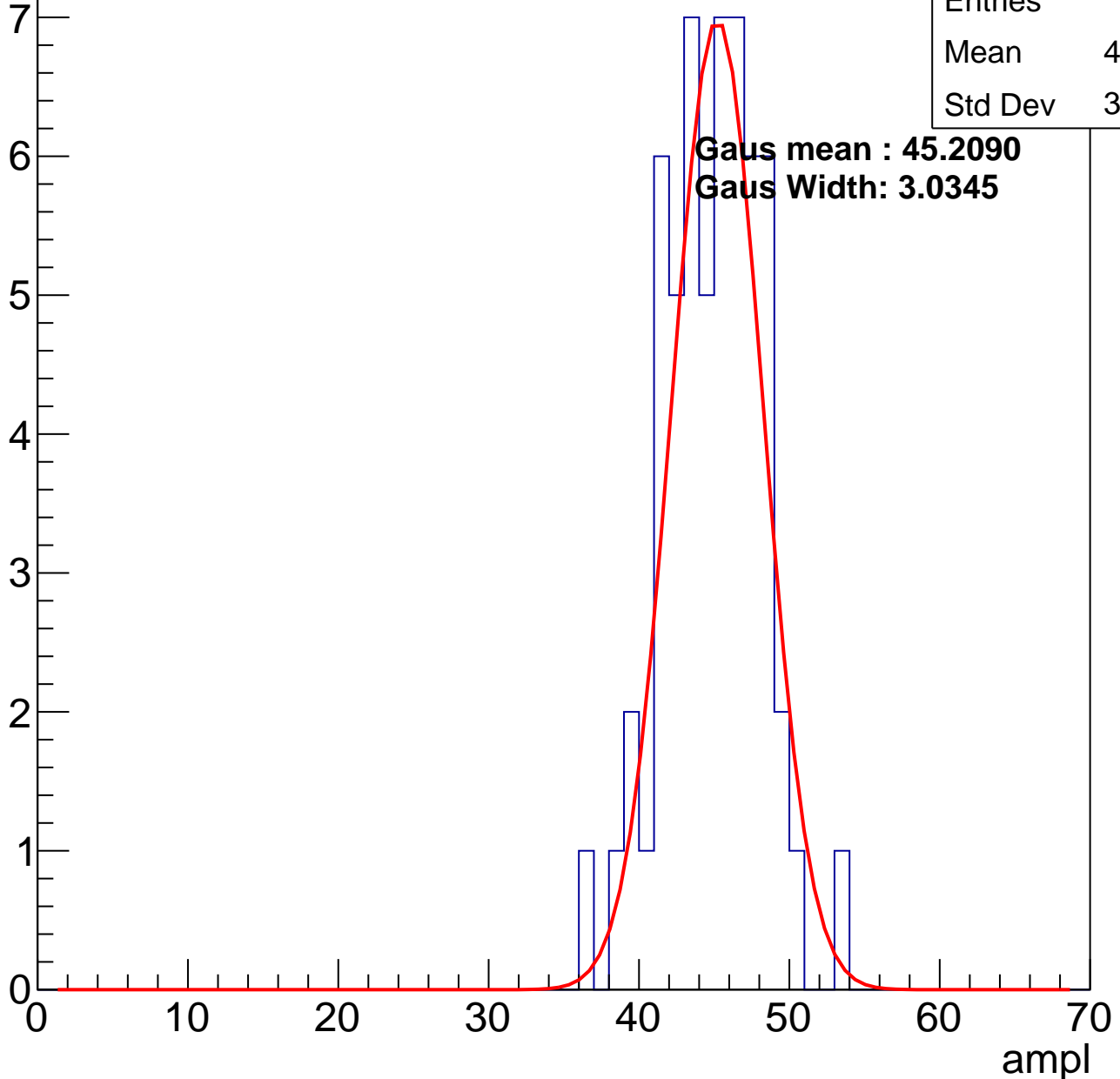
# B0L000S, U7-ch5, adc2

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	58
Mean	44.43
Std Dev	3.185

**Gaus mean : 45.2090**  
**Gaus Width: 3.0345**

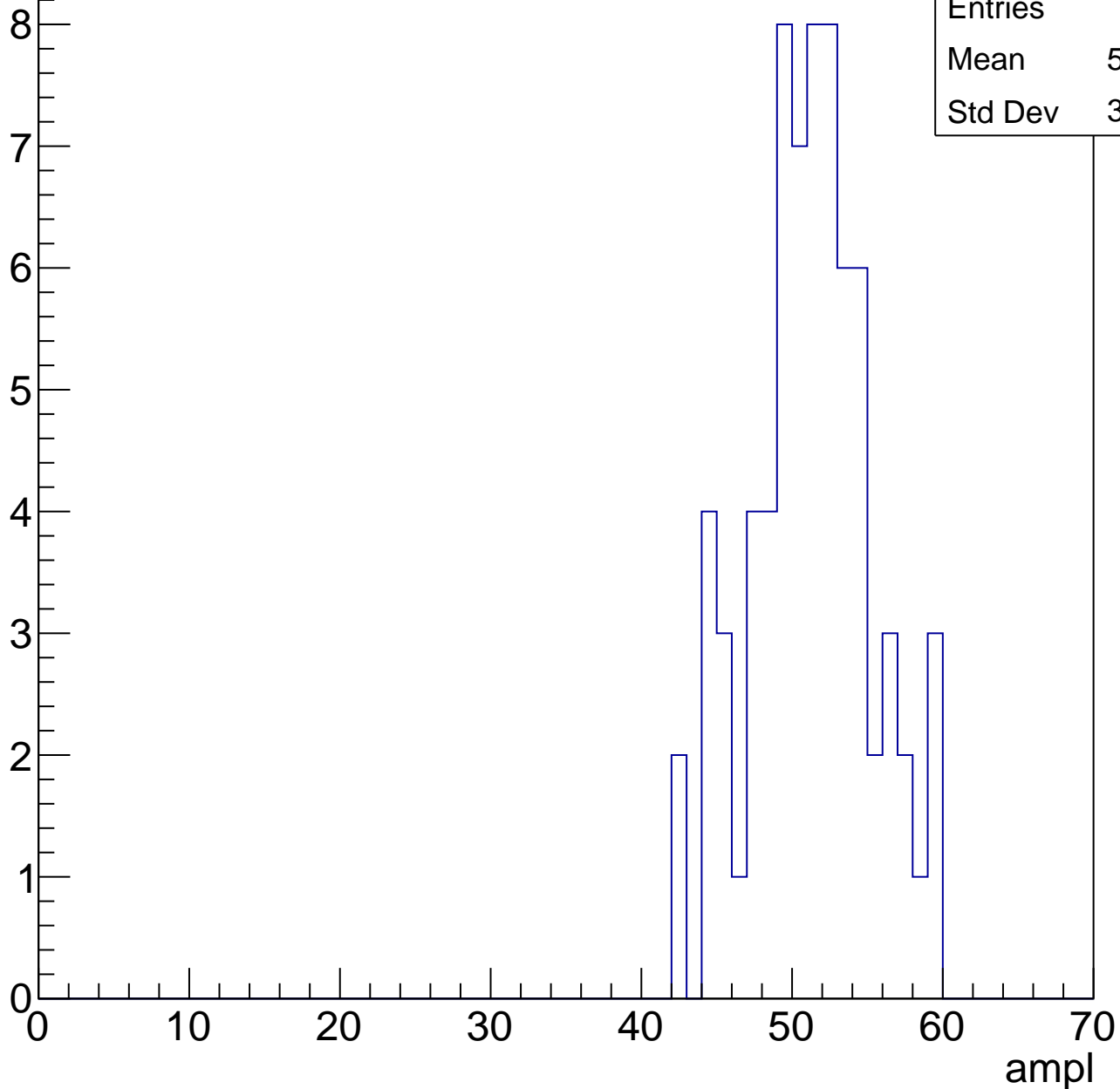


# B0L000S, U7-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

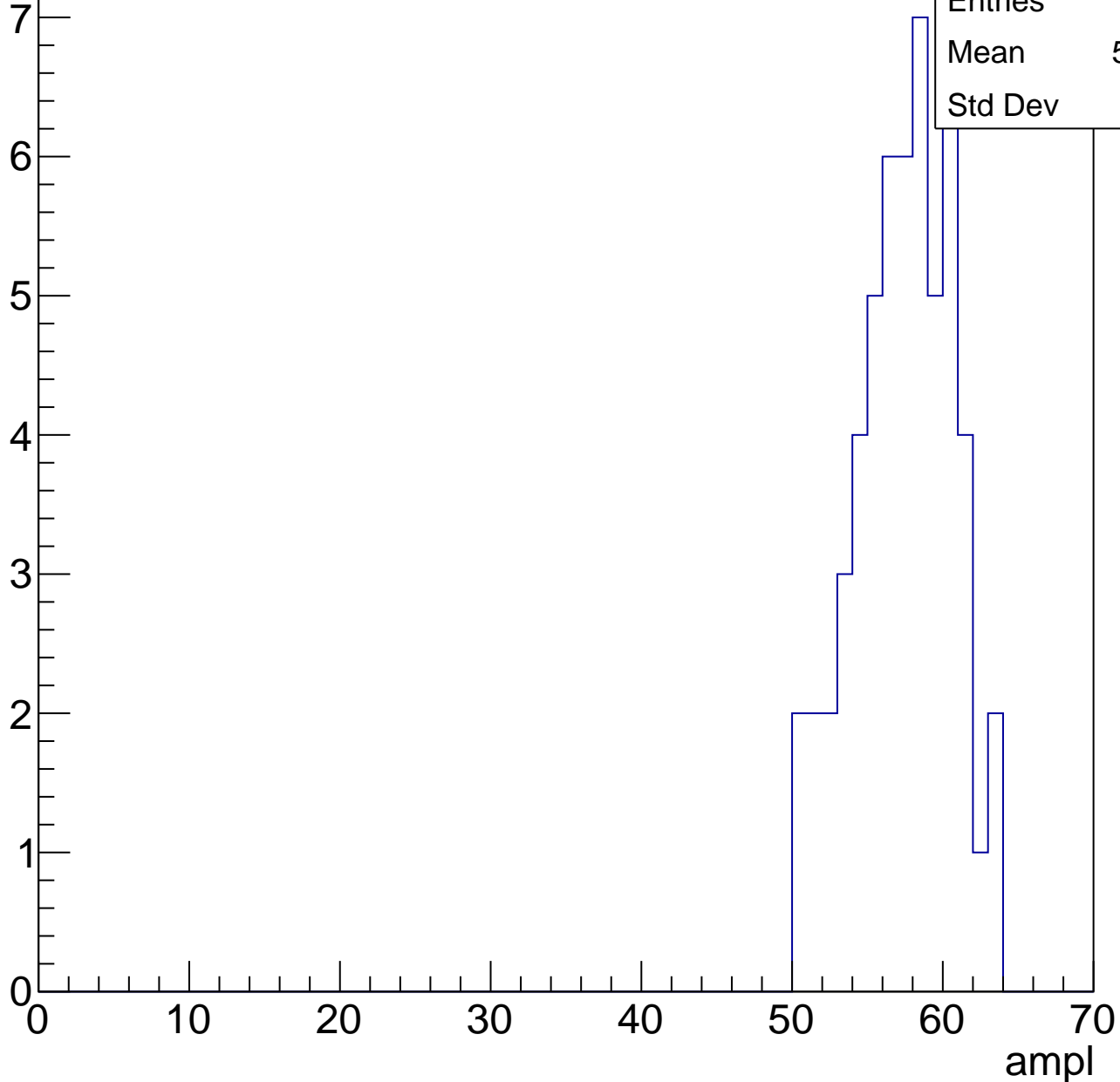
Entries	72
Mean	50.78
Std Dev	3.966



# B0L000S, U7-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

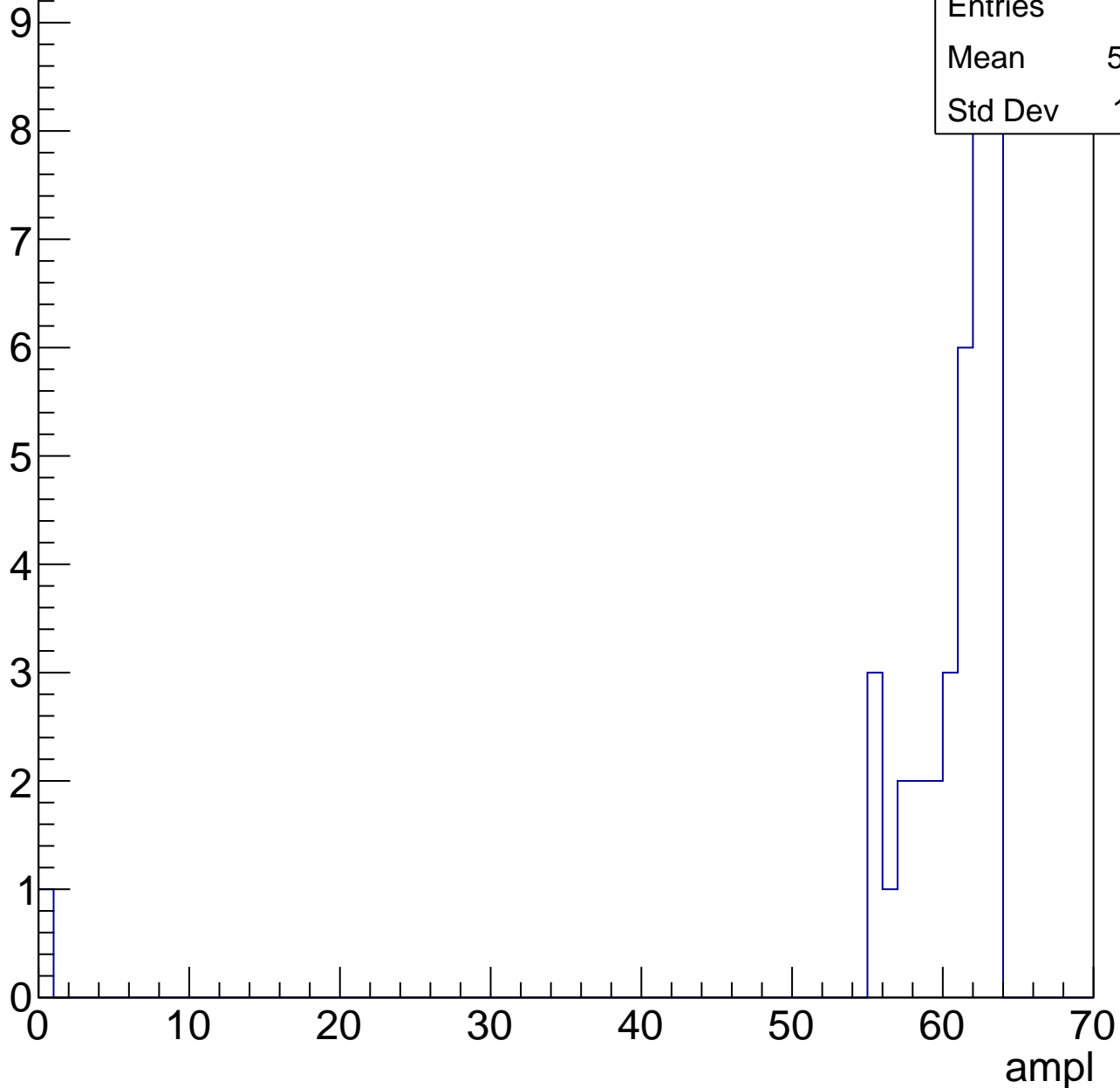
Entry



# B0L000S, U7-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L000S, U7-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L000S, U7-ch6, adc0

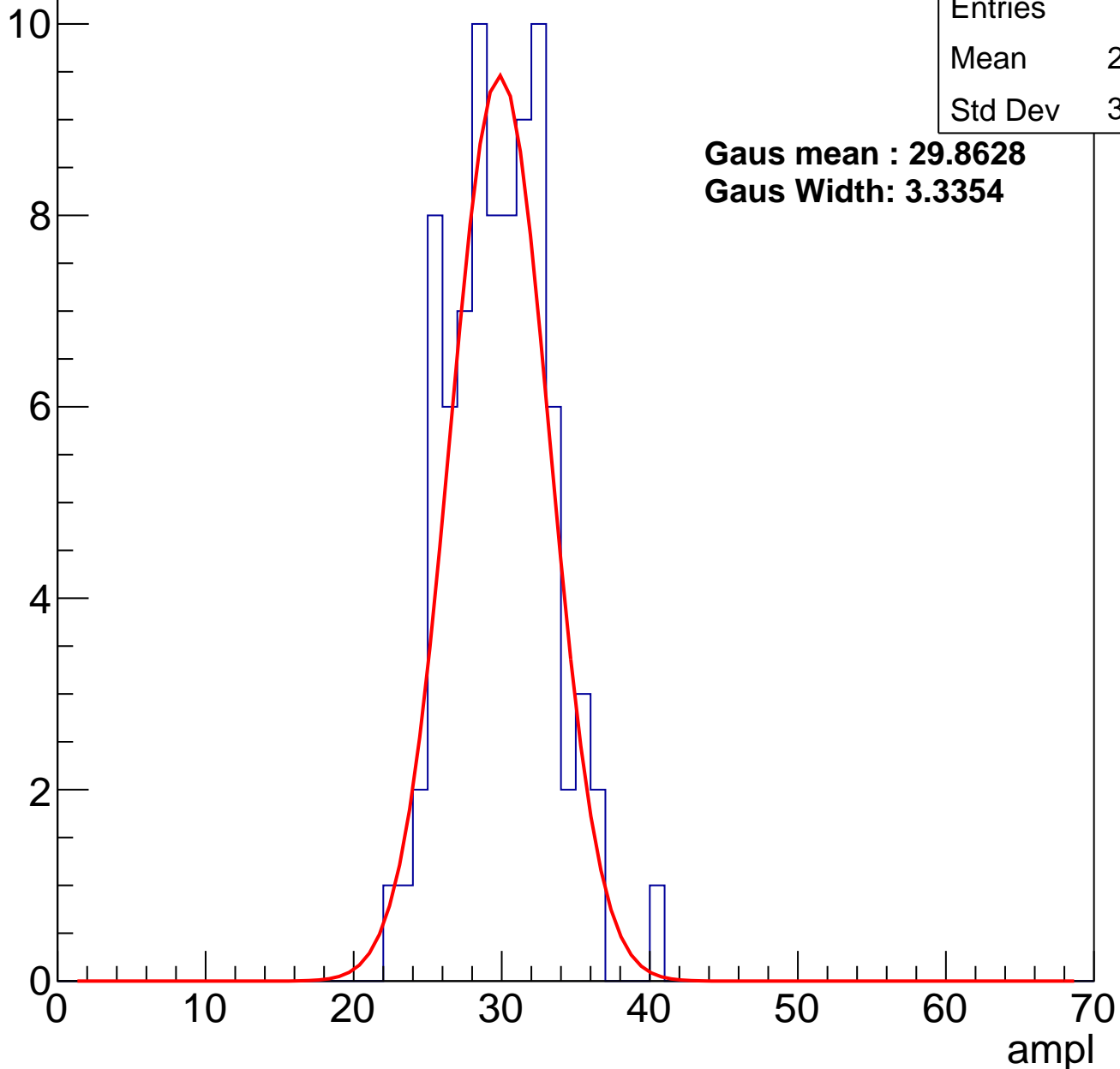
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	84
Mean	29.43
Std Dev	3.357

**Gaus mean : 29.8628**

**Gaus Width: 3.3354**

Entry

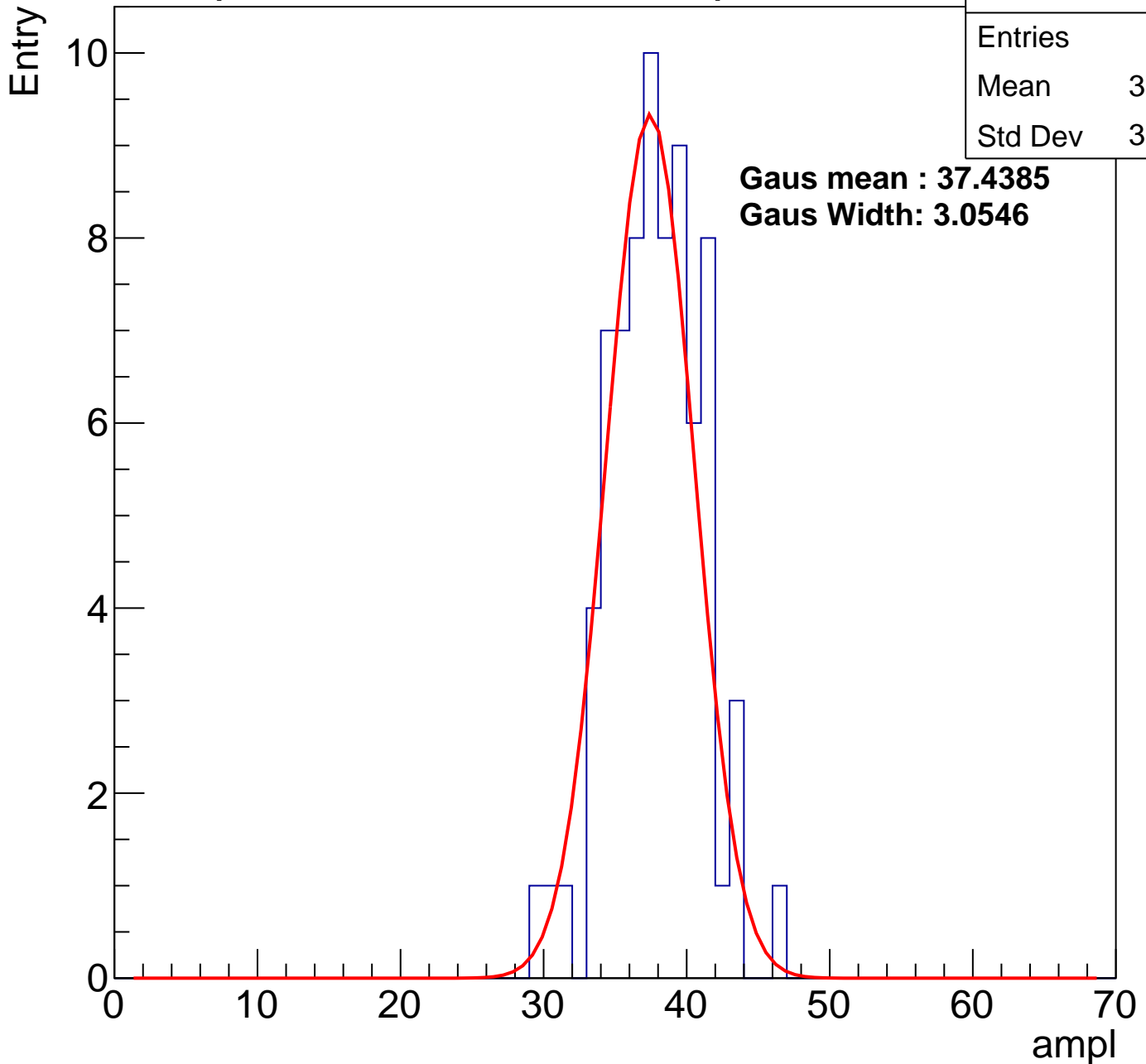


# B0L000S, U7-ch6, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	75
Mean	37.37
Std Dev	3.144

**Gaus mean : 37.4385**  
**Gaus Width: 3.0546**



# B0L000S, U7-ch6, adc2

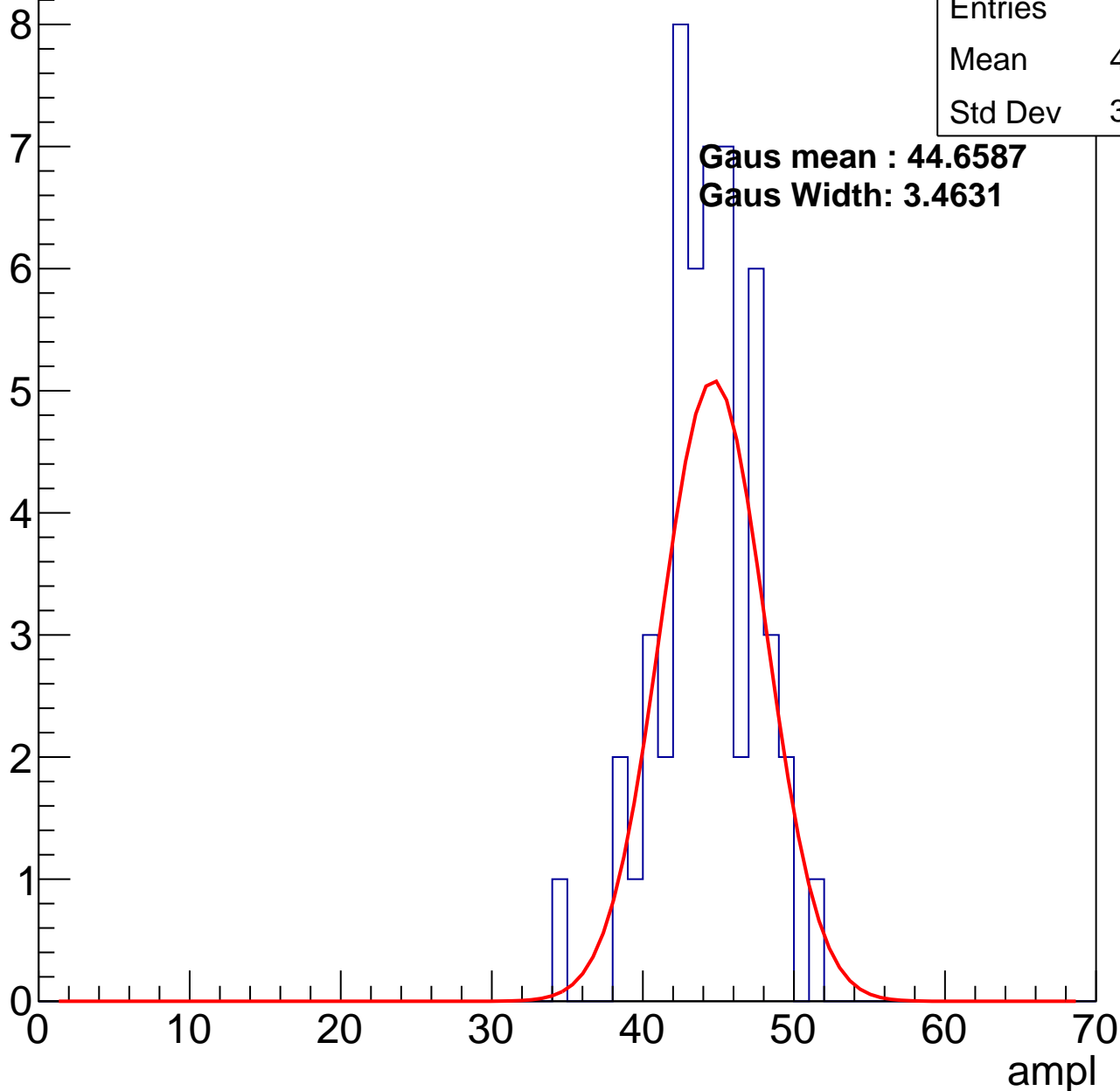
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	51
Mean	43.82
Std Dev	3.179

**Gaus mean : 44.6587**

**Gaus Width: 3.4631**



# B0L000S, U7-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

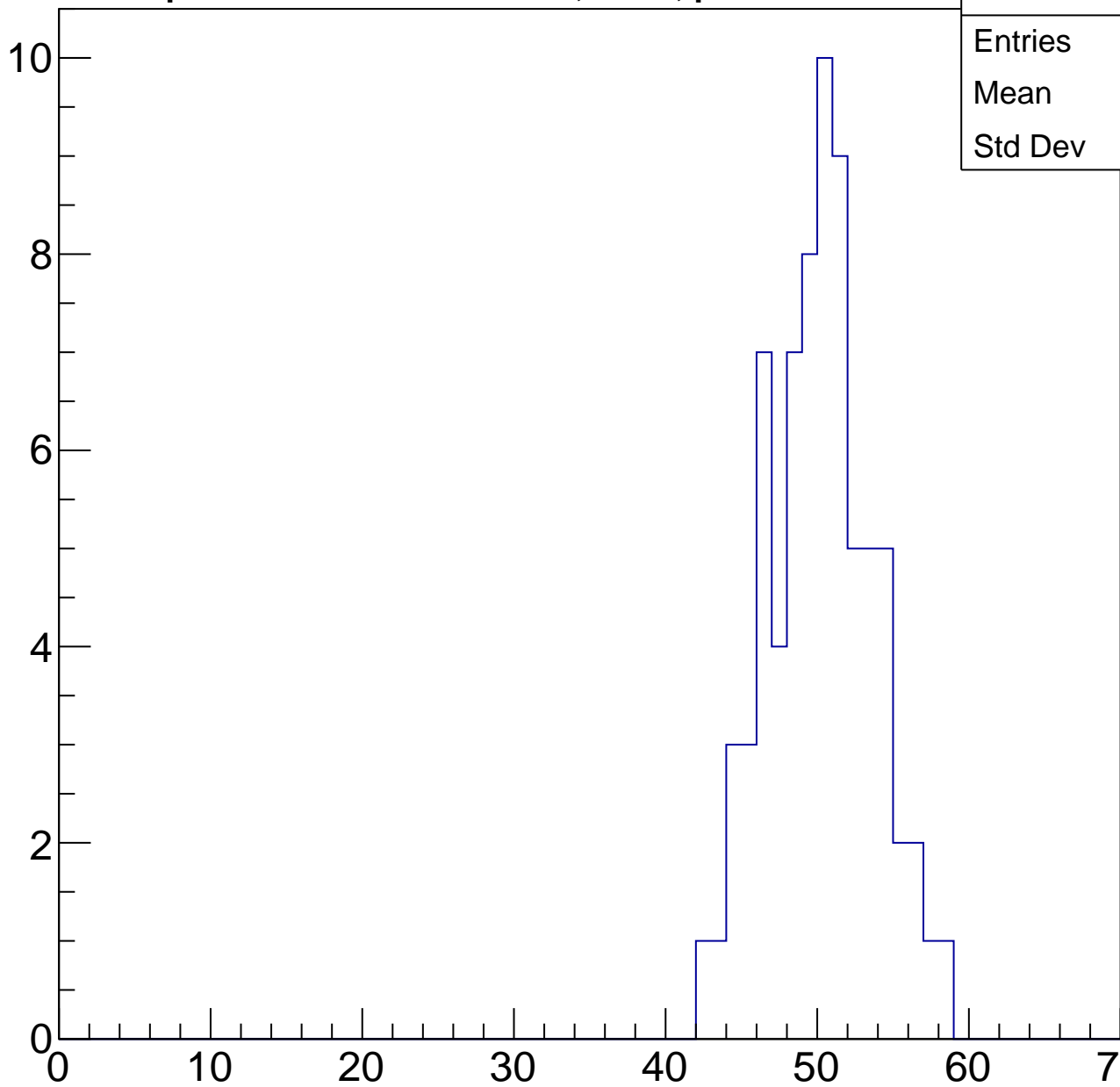
Entries	74
Mean	49.74
Std Dev	3.417

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

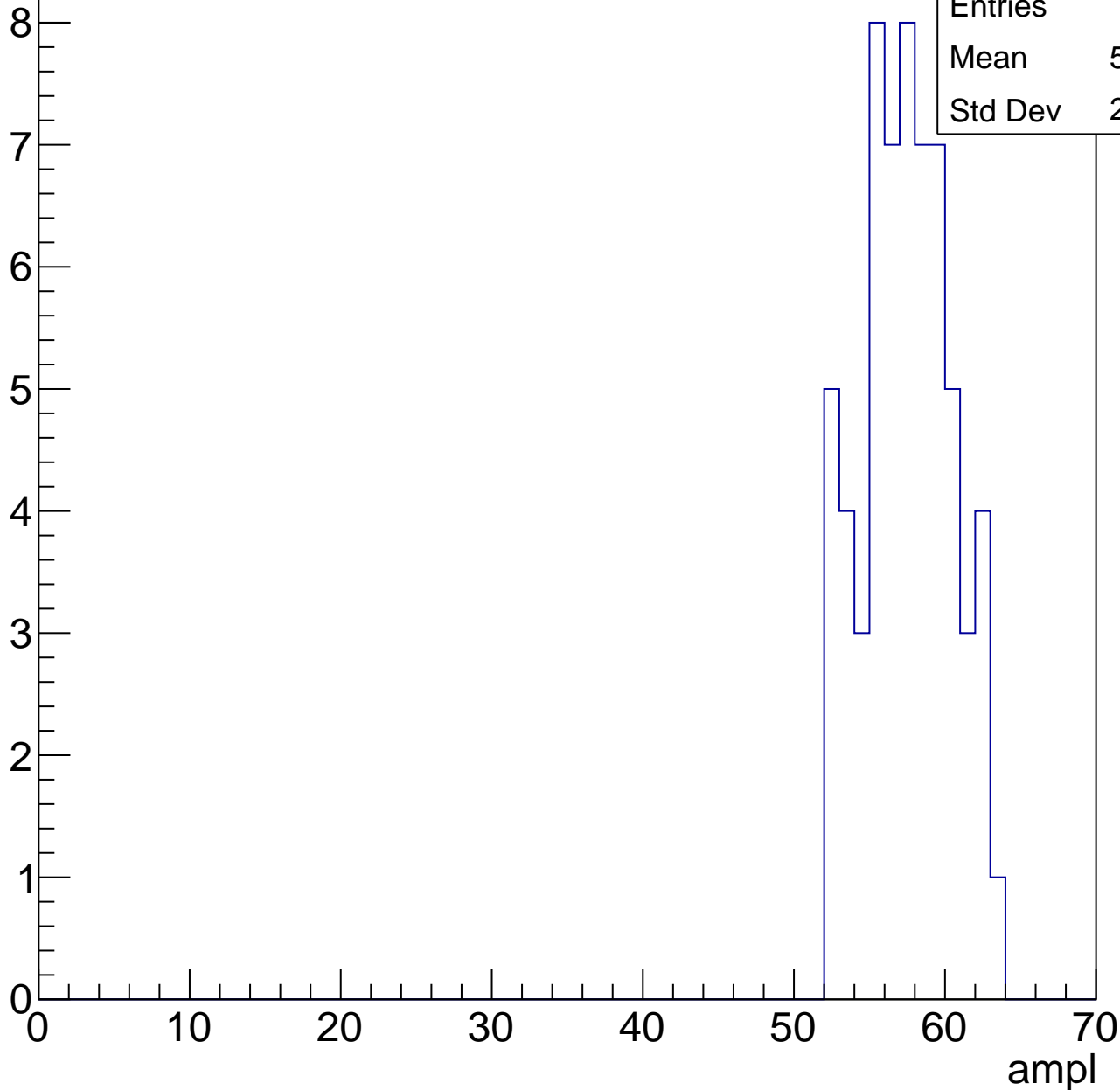
ampl



# B0L000S, U7-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



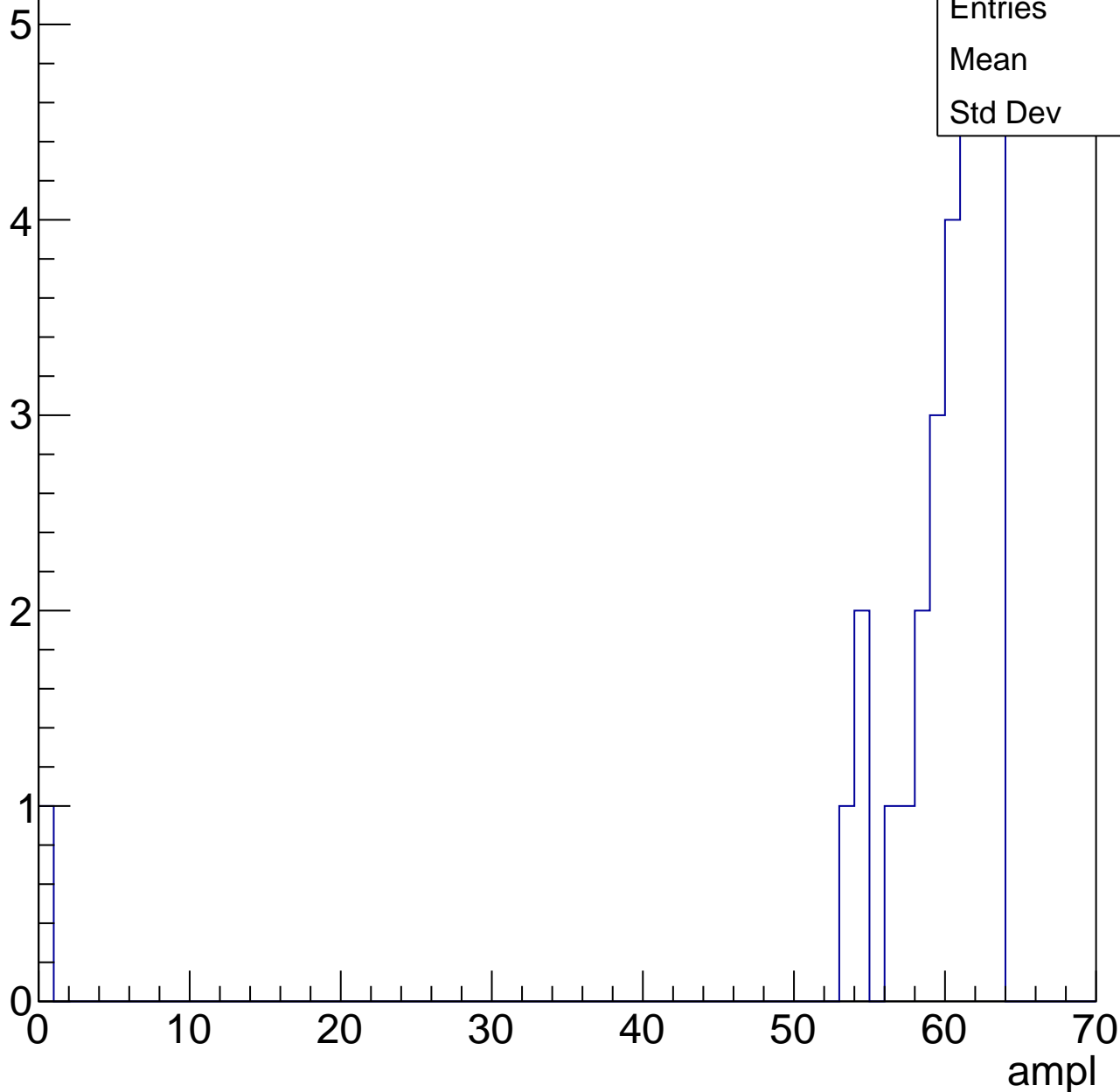
Entries	62
Mean	57.02
Std Dev	2.893

# B0L000S, U7-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

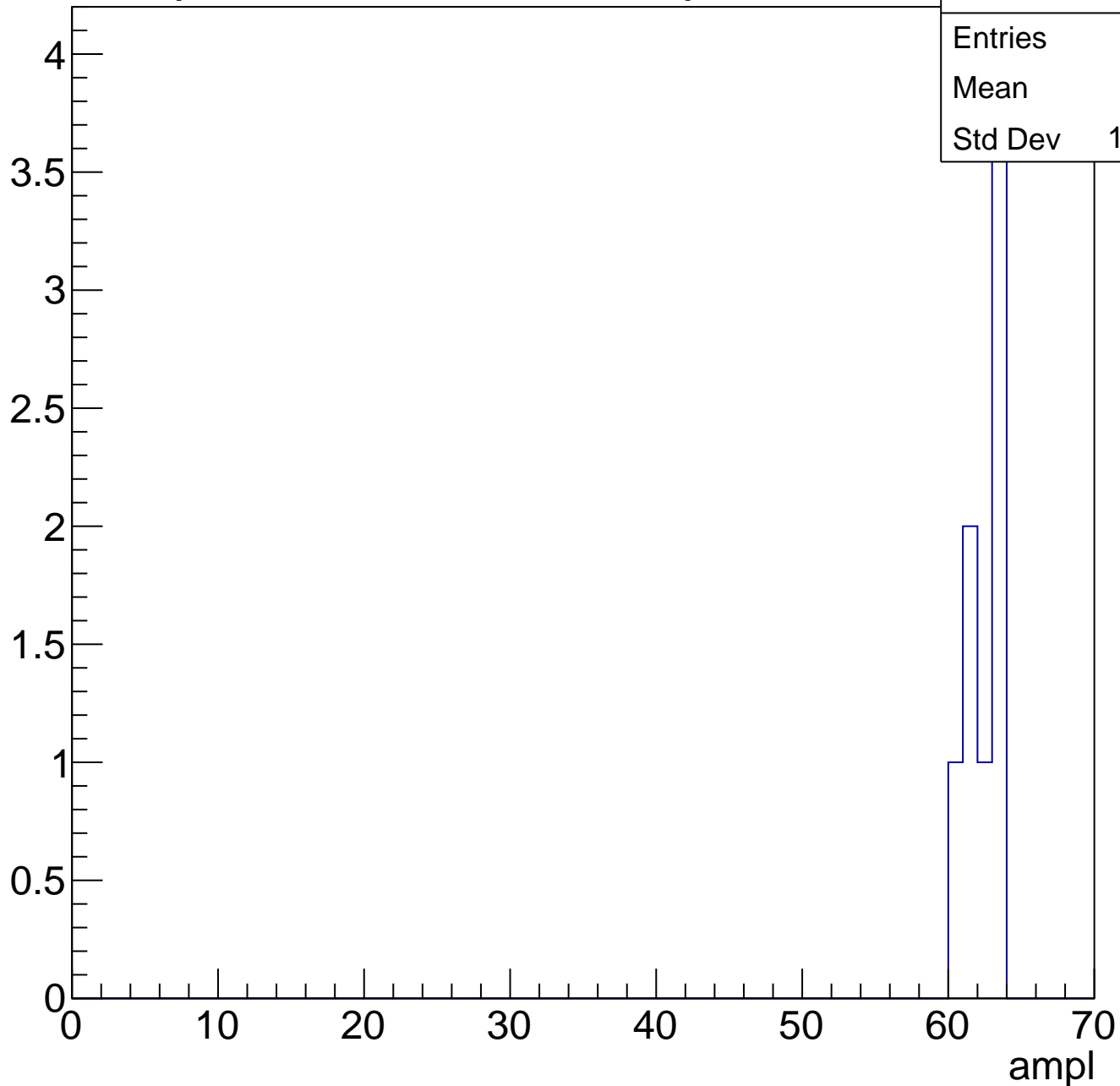
Entries	30
Mean	57.9
Std Dev	11.1



# B0L000S, U7-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L000S, U7-ch7, adc0

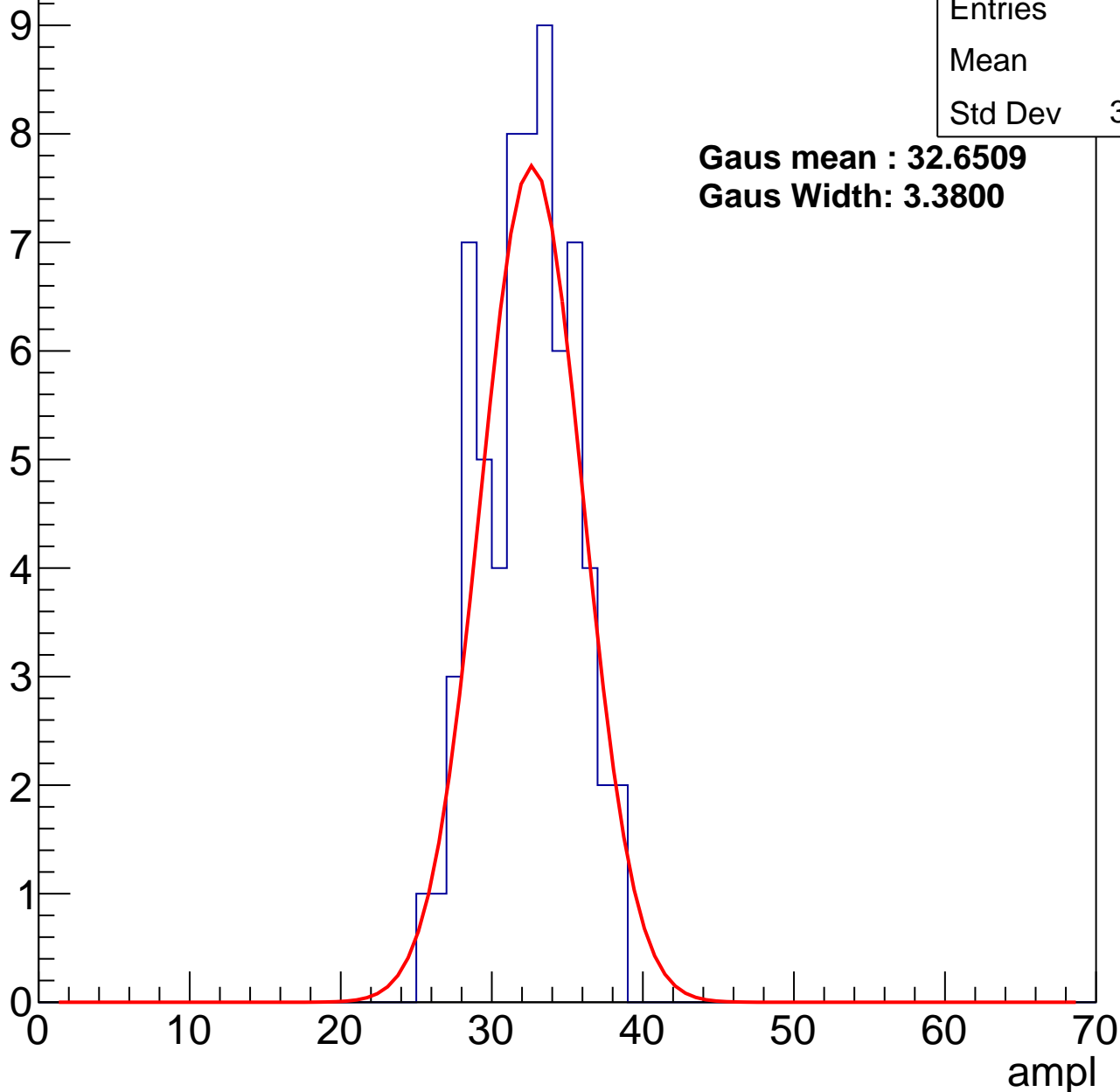
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	67
Mean	31.9
Std Dev	3.048

**Gaus mean : 32.6509**

**Gaus Width: 3.3800**



# B0L000S, U7-ch7, adc1

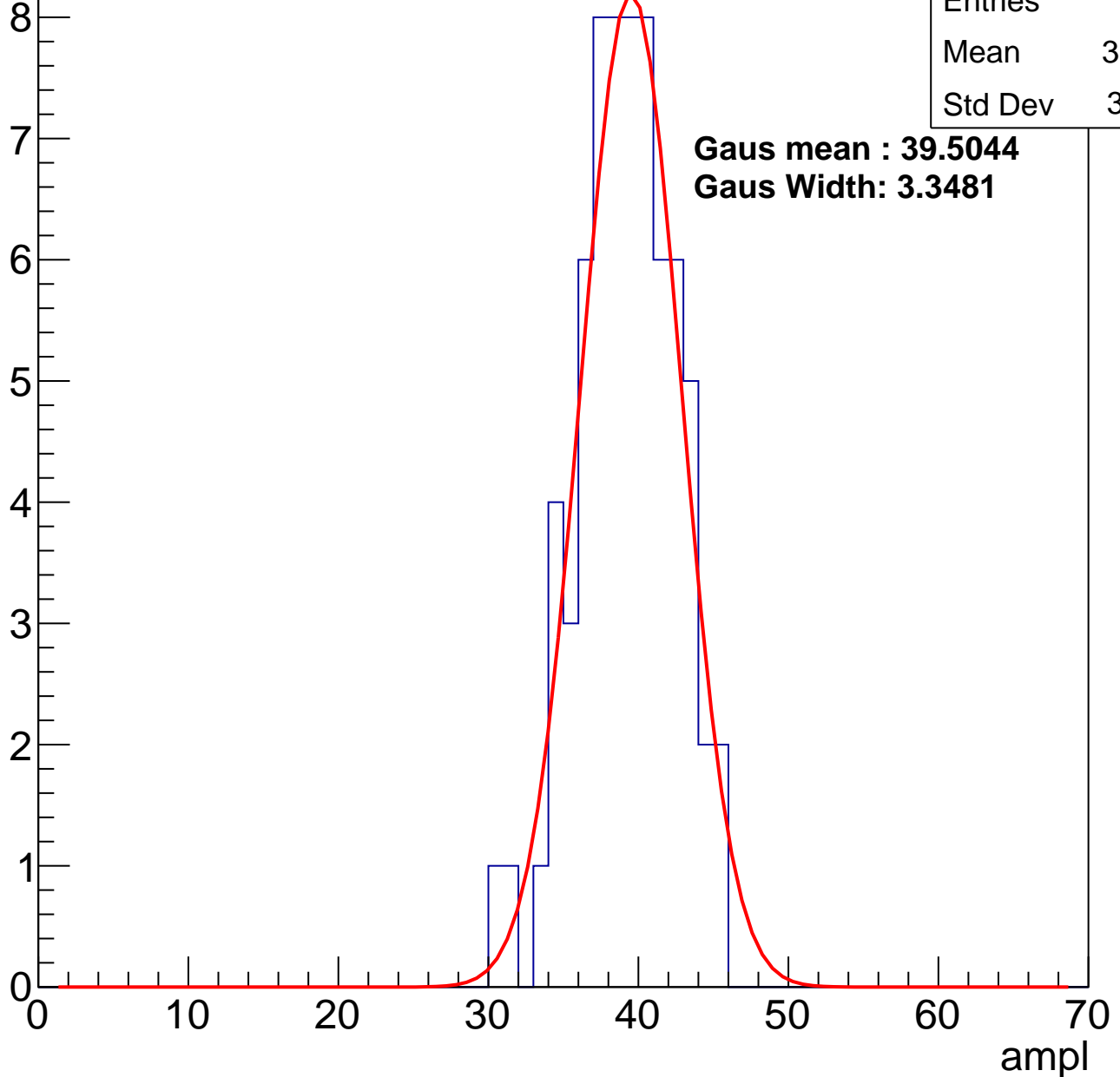
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	69
Mean	38.75
Std Dev	3.201

**Gaus mean : 39.5044**

**Gaus Width: 3.3481**



# B0L000S, U7-ch7, adc2

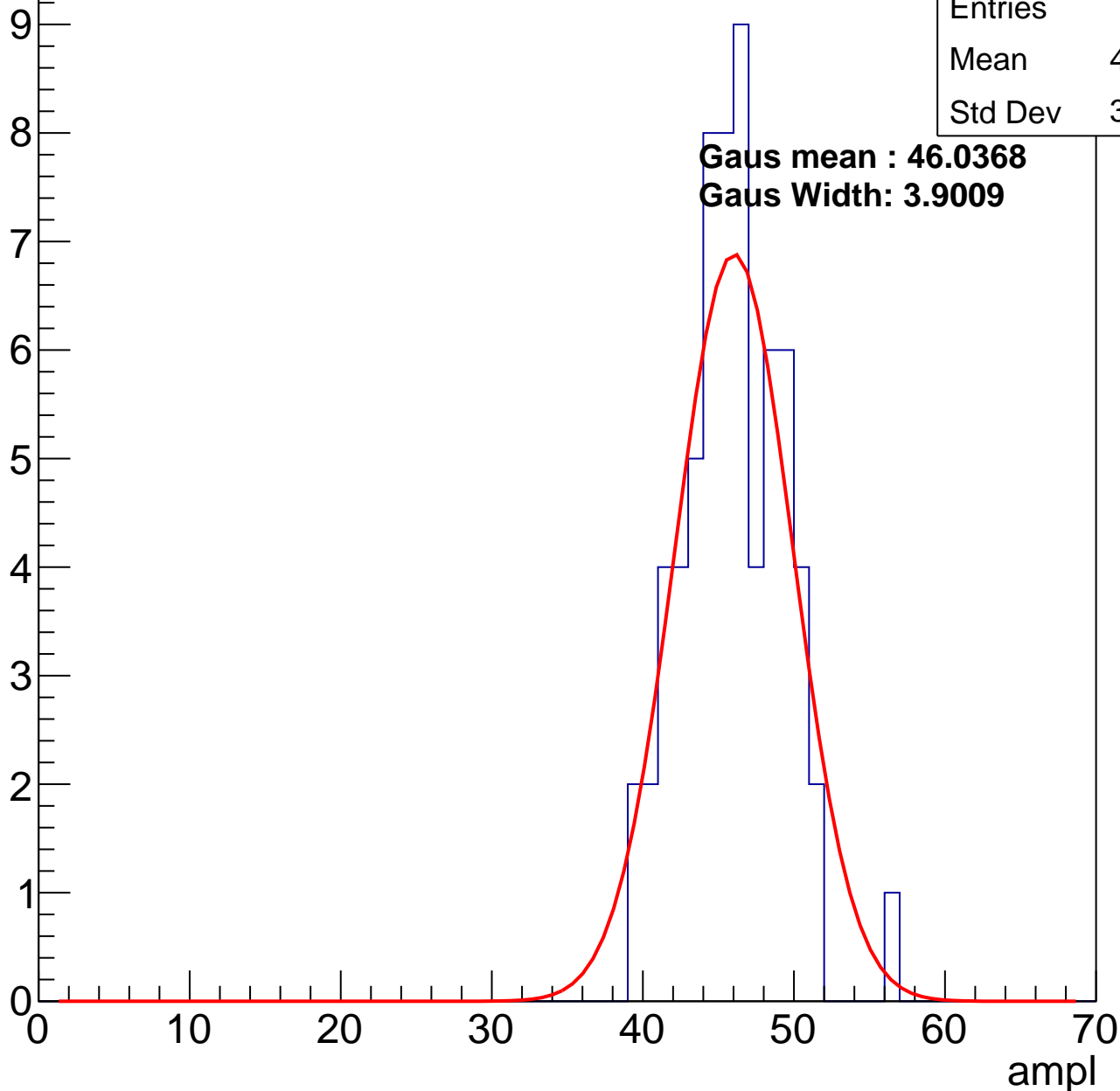
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	65
Mean	45.52
Std Dev	3.282

**Gaus mean : 46.0368**

**Gaus Width: 3.9009**

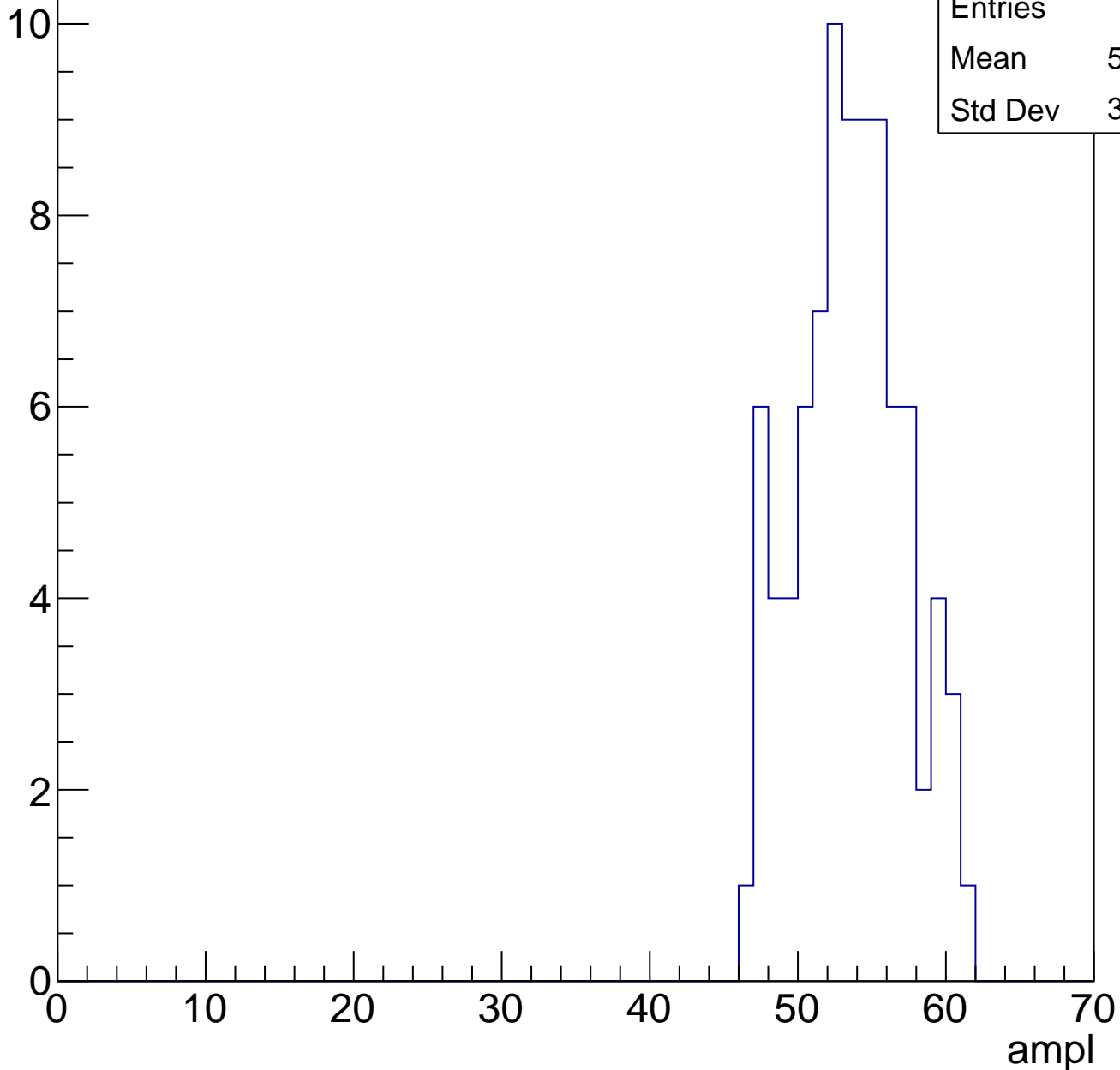


# B0L000S, U7-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	87
Mean	53.13
Std Dev	3.587

Entry

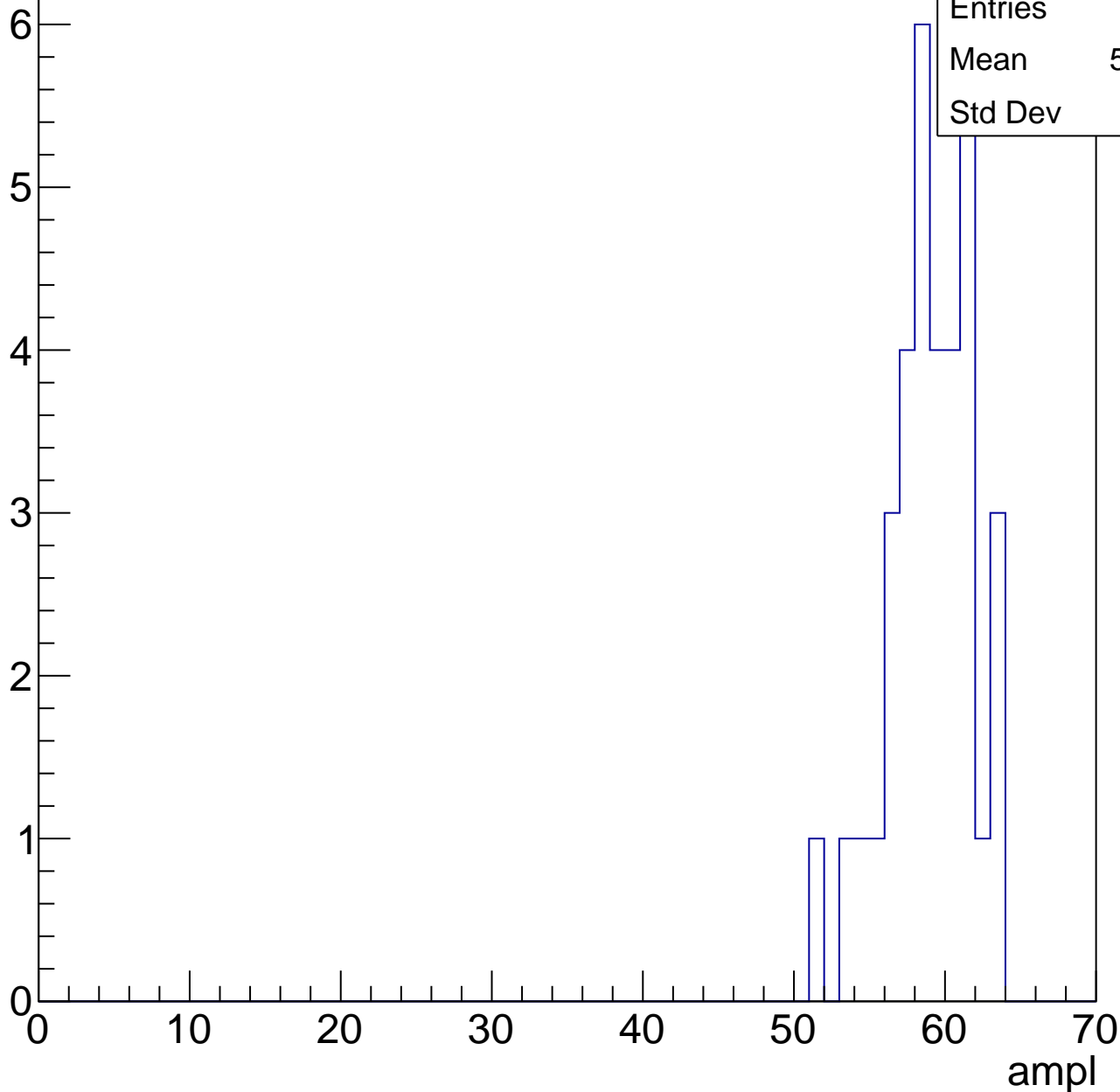


# B0L000S, U7-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	35
Mean	58.57
Std Dev	2.77

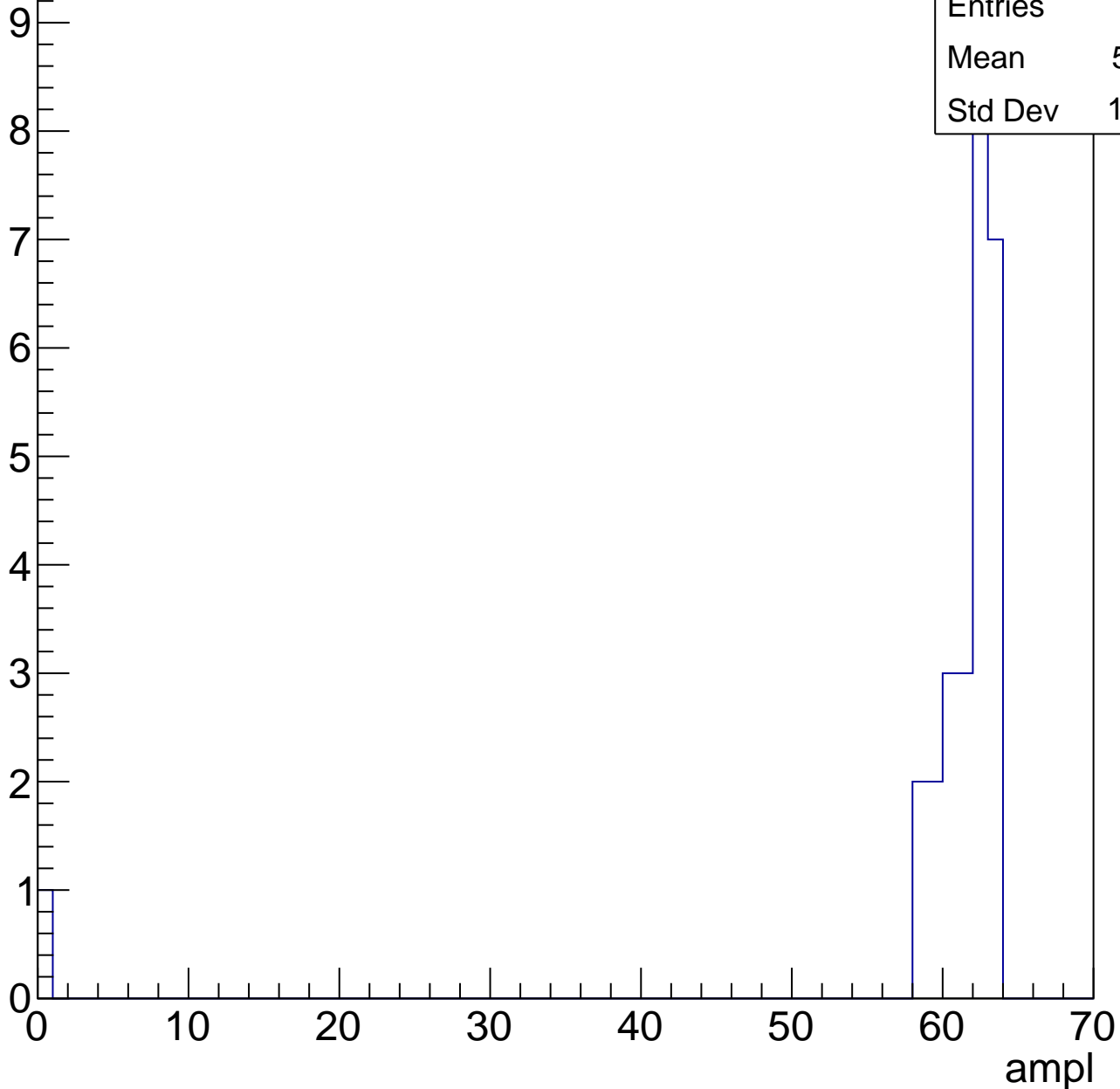


# B0L000S, U7-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	27
Mean	59.11
Std Dev	11.69



# B0L000S, U7-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L000S, U7-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L000S, U7-ch8, adc0

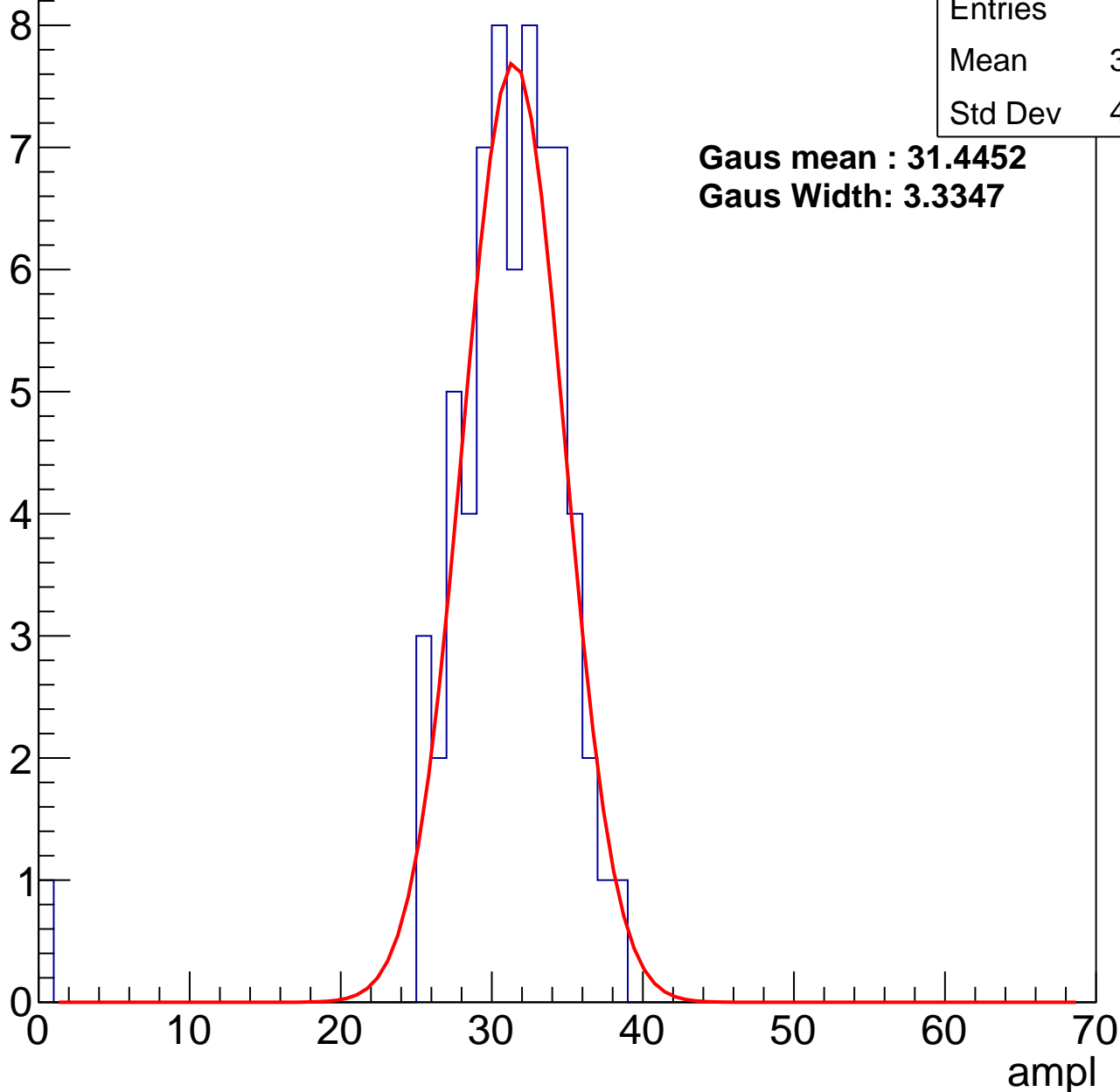
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	66
Mean	30.53
Std Dev	4.853

**Gaus mean : 31.4452**

**Gaus Width: 3.3347**



# B0L000S, U7-ch8, adc1

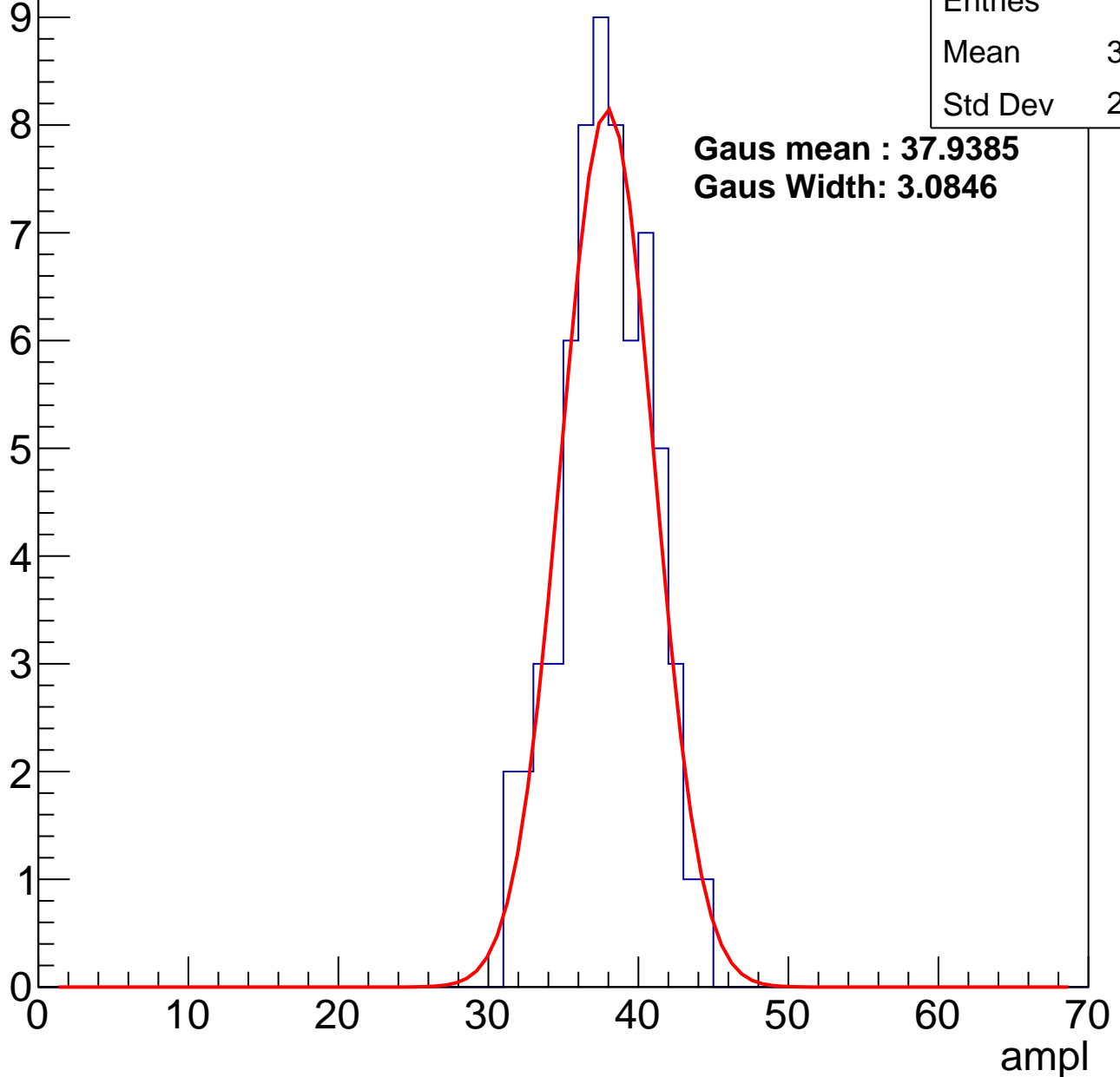
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	64
Mean	37.41
Std Dev	2.941

**Gaus mean : 37.9385**

**Gaus Width: 3.0846**



# B0L000S, U7-ch8, adc2

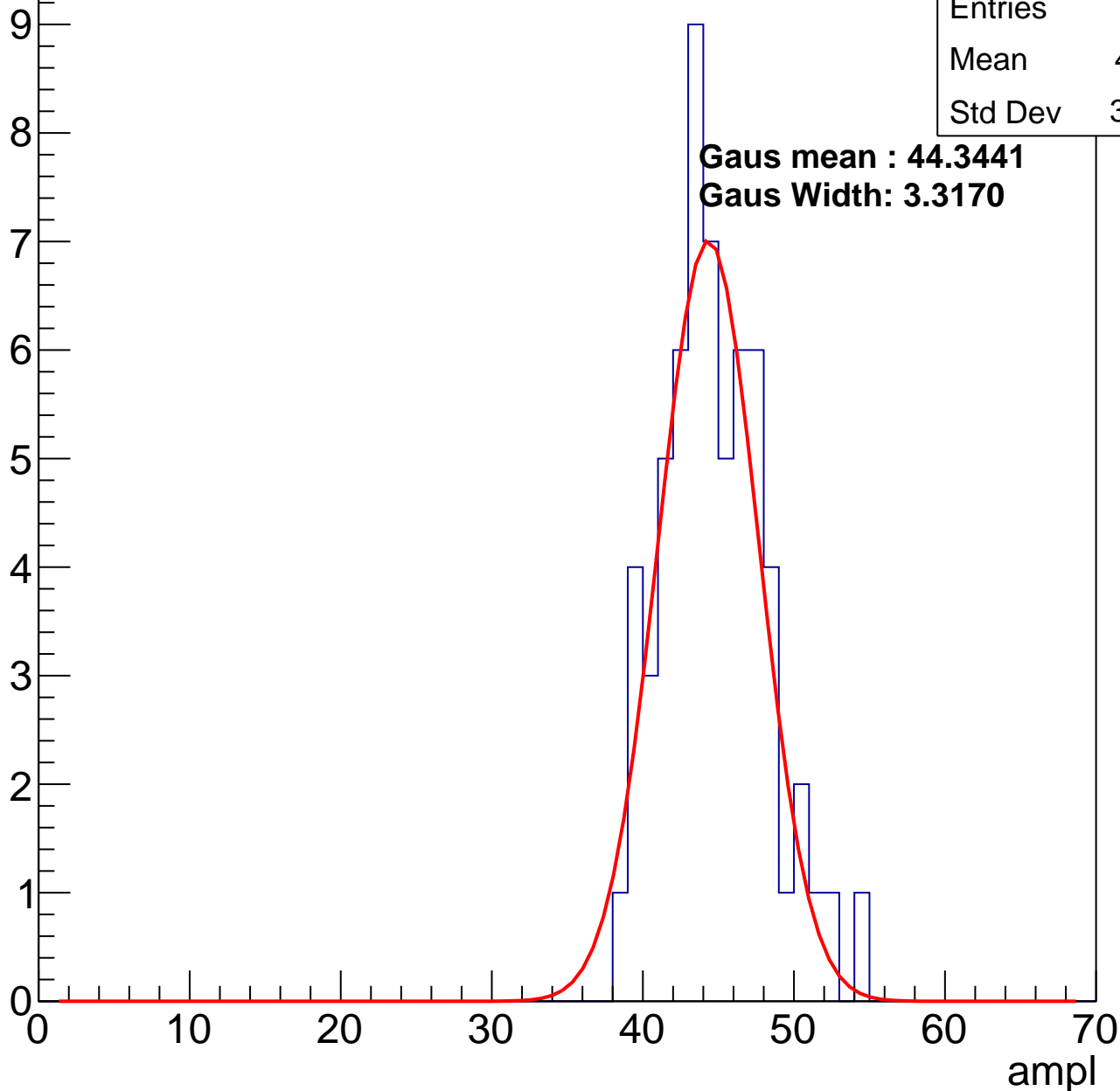
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	62
Mean	44.31
Std Dev	3.392

**Gaus mean : 44.3441**

**Gaus Width: 3.3170**

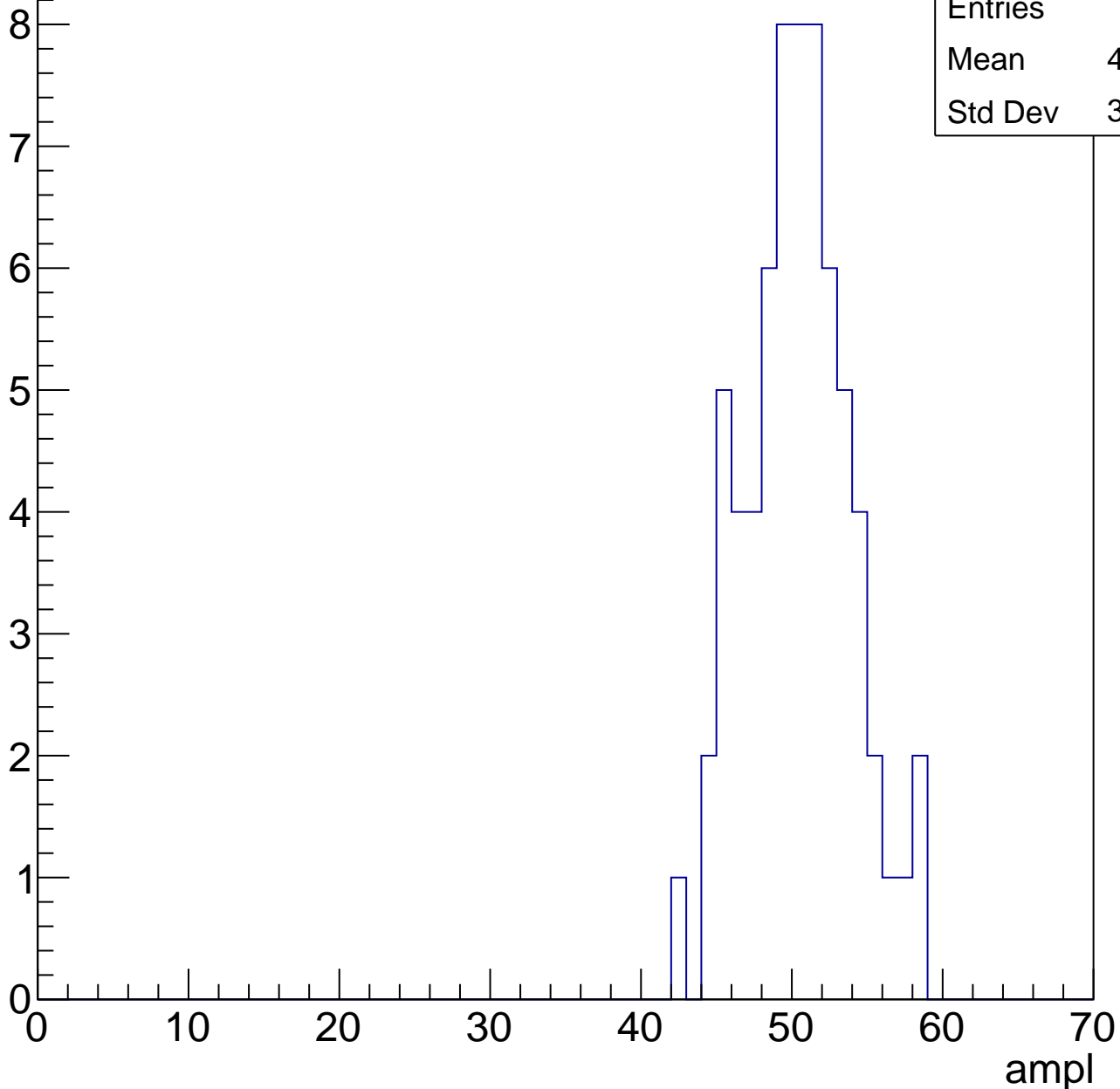


# B0L000S, U7-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	67
Mean	49.96
Std Dev	3.449

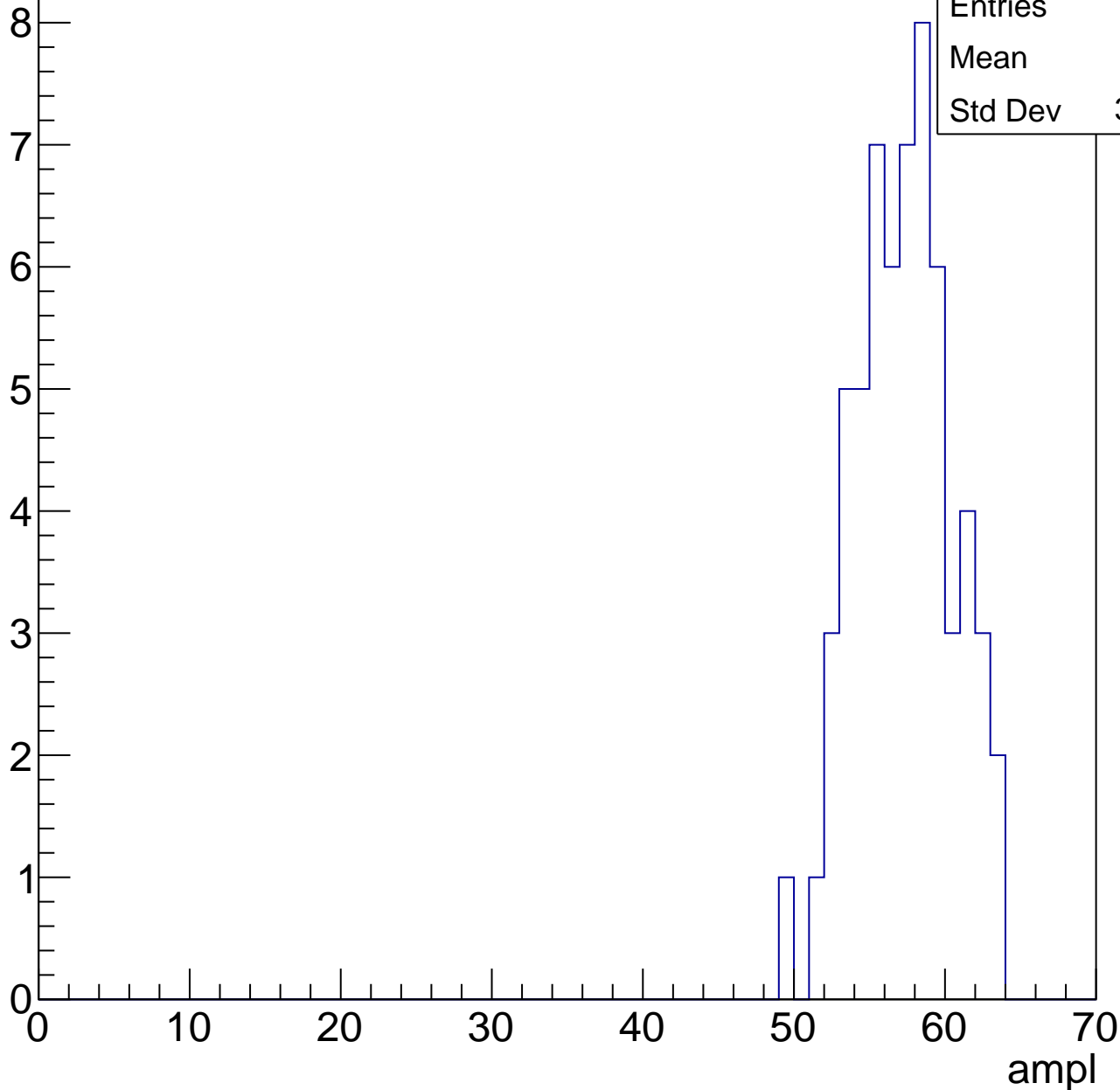


# B0L000S, U7-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

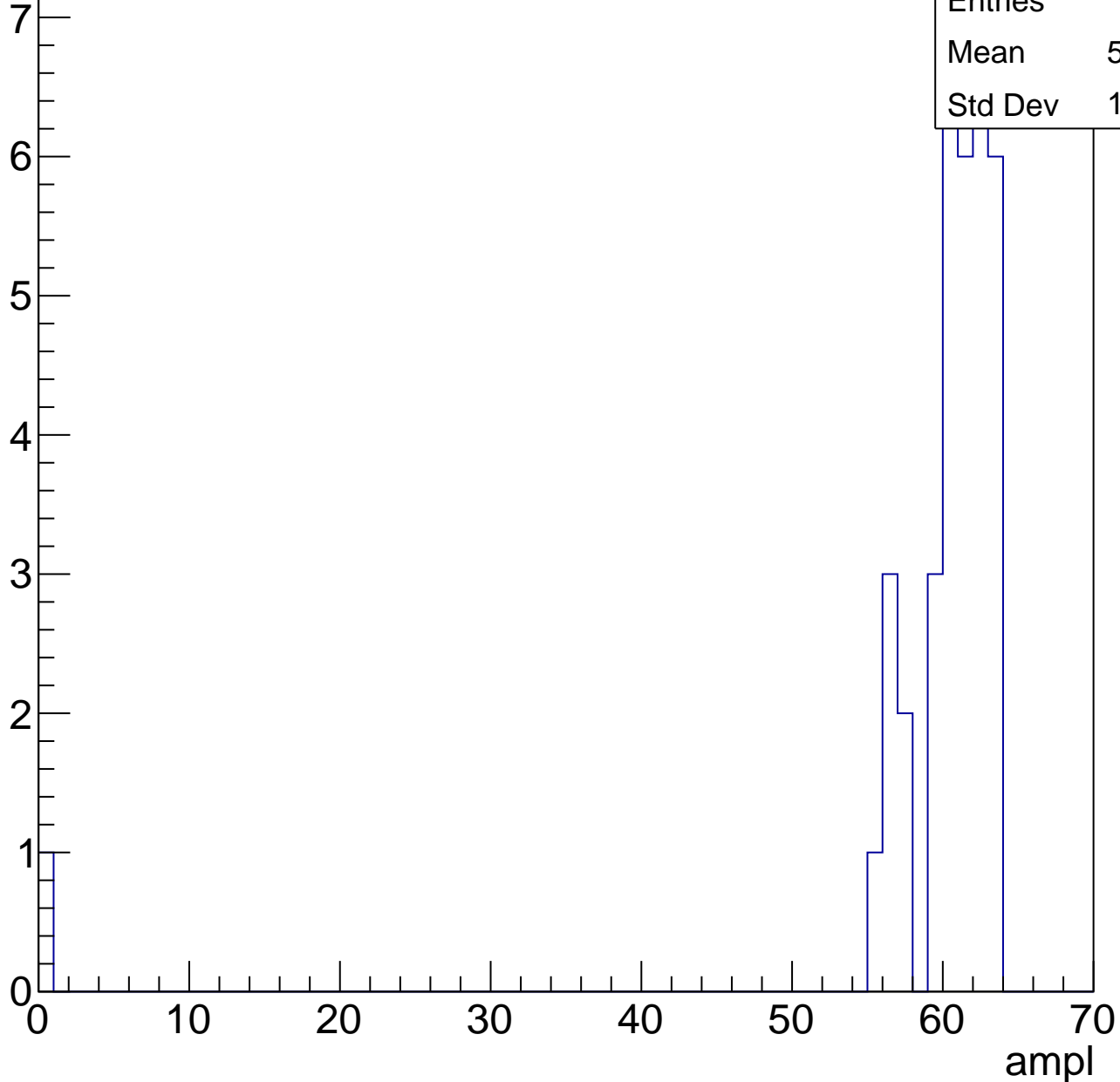
Entries	61
Mean	56.8
Std Dev	3.141



# B0L000S, U7-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

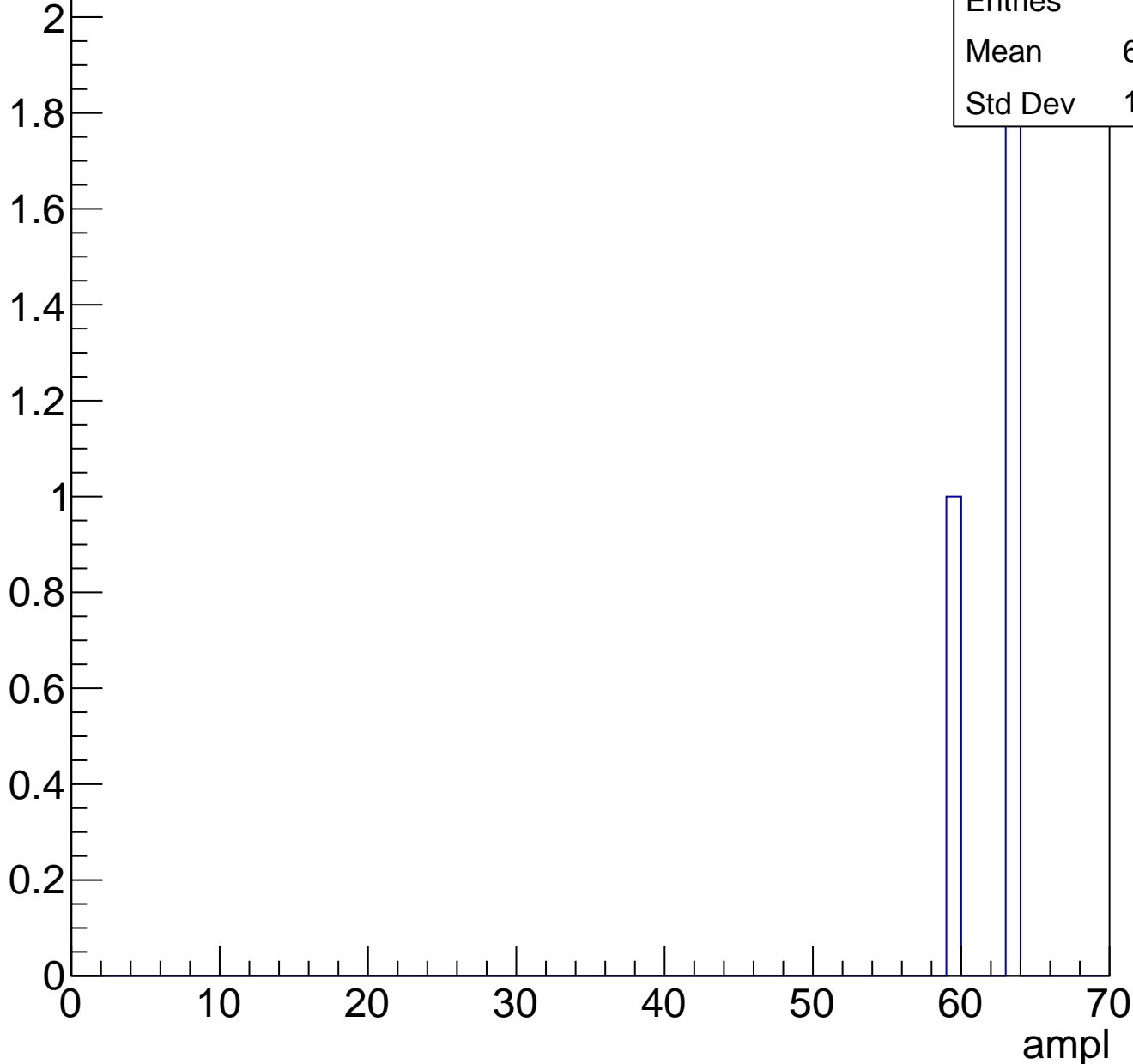
Entry



# B0L000S, U7-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

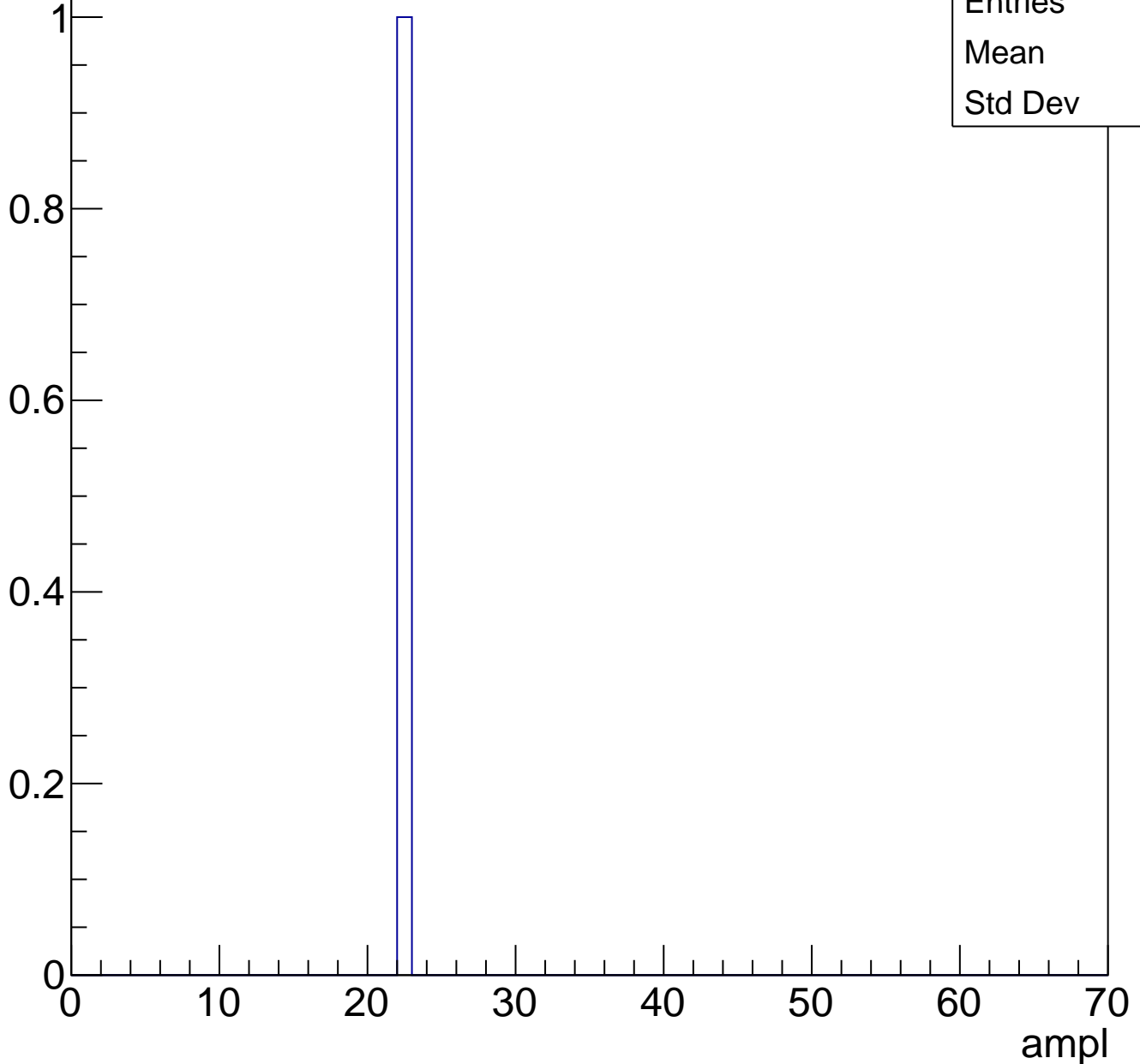




# B0L000S, U7-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch9, adc0

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	62
Mean	31.5
Std Dev	5.098

**Gaus mean : 31.8497**

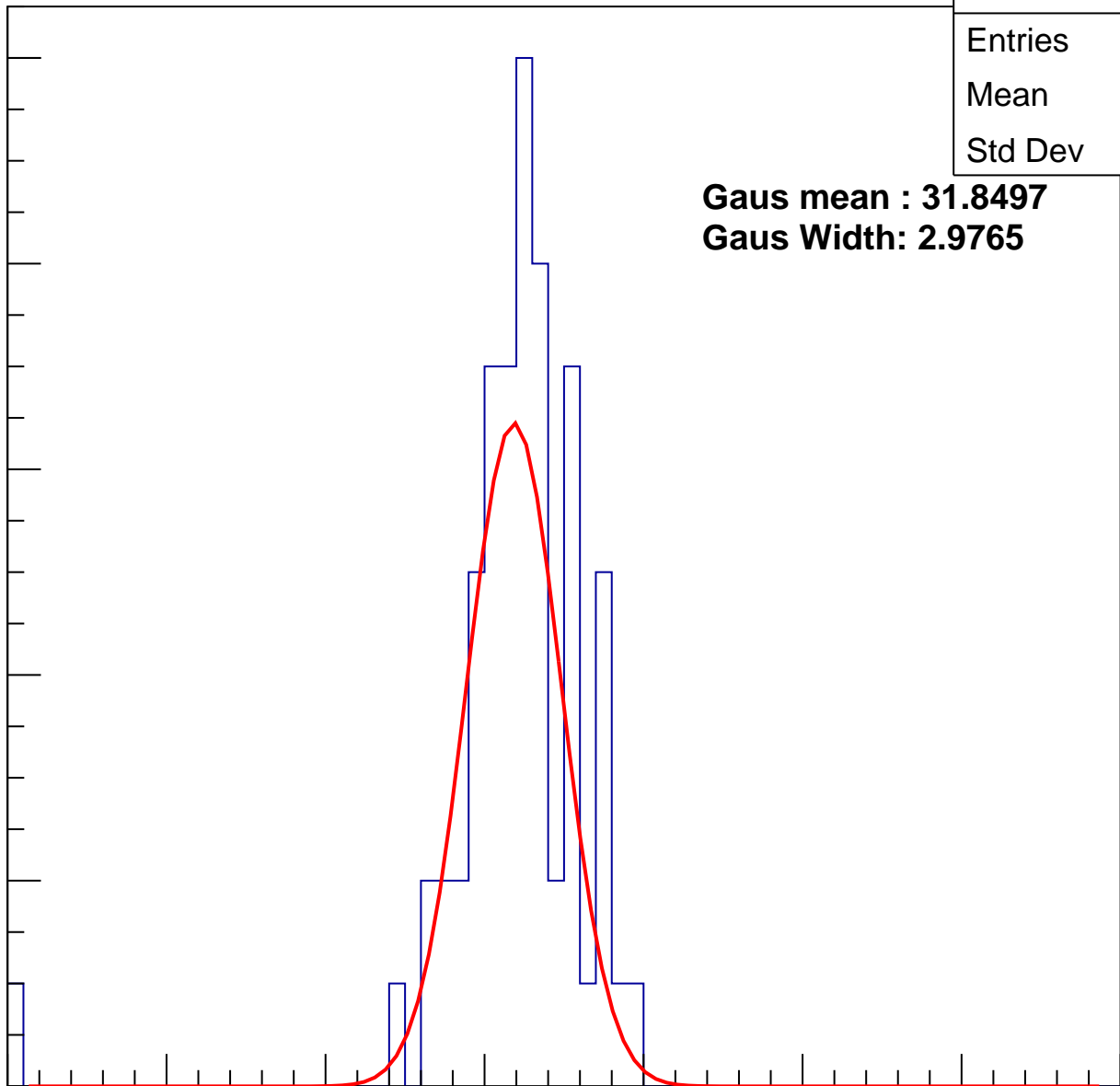
**Gaus Width: 2.9765**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L000S, U7-ch9, adc1

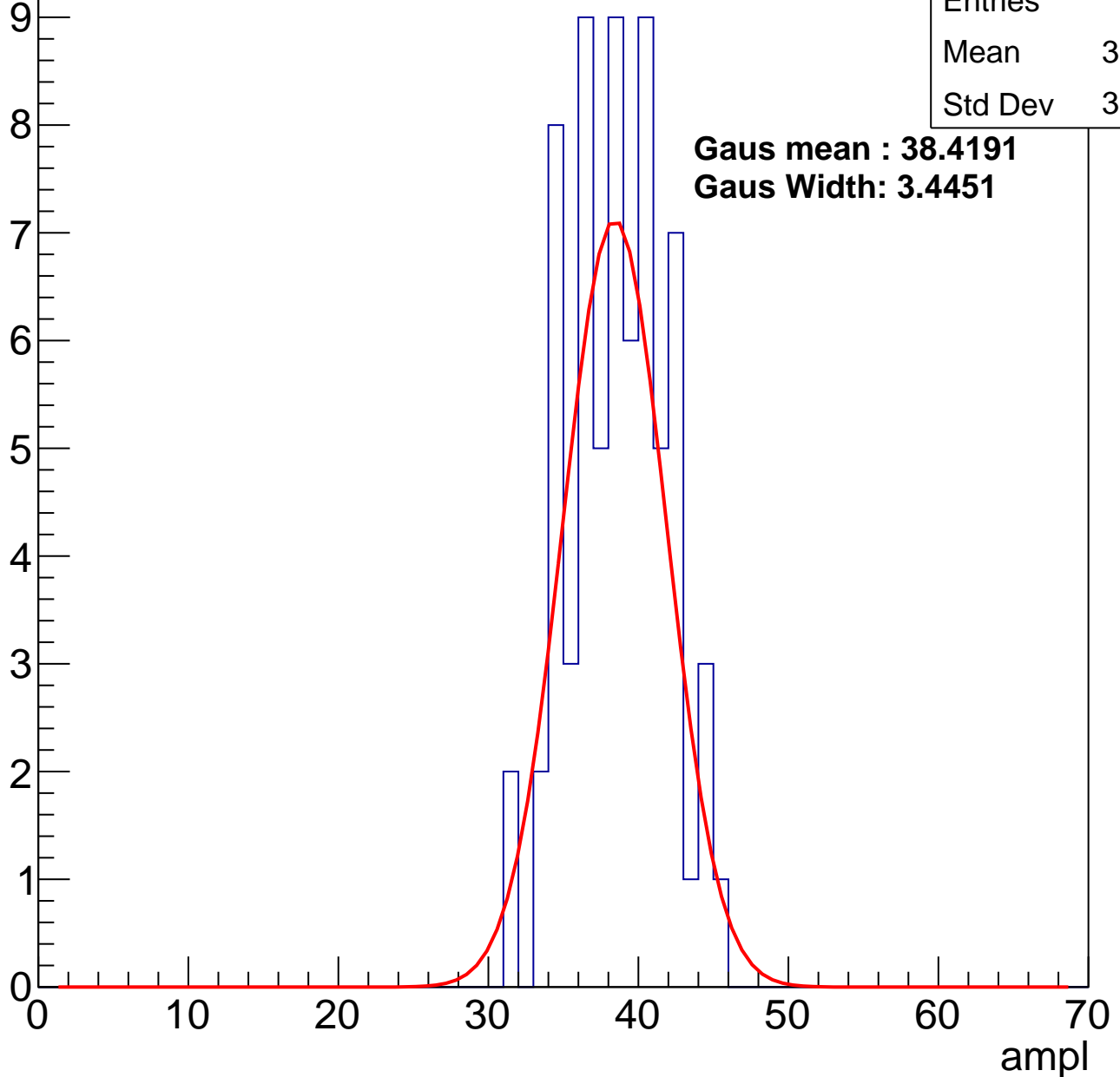
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	70
Mean	38.13
Std Dev	3.216

**Gaus mean : 38.4191**

**Gaus Width: 3.4451**



# B0L000S, U7-ch9, adc2

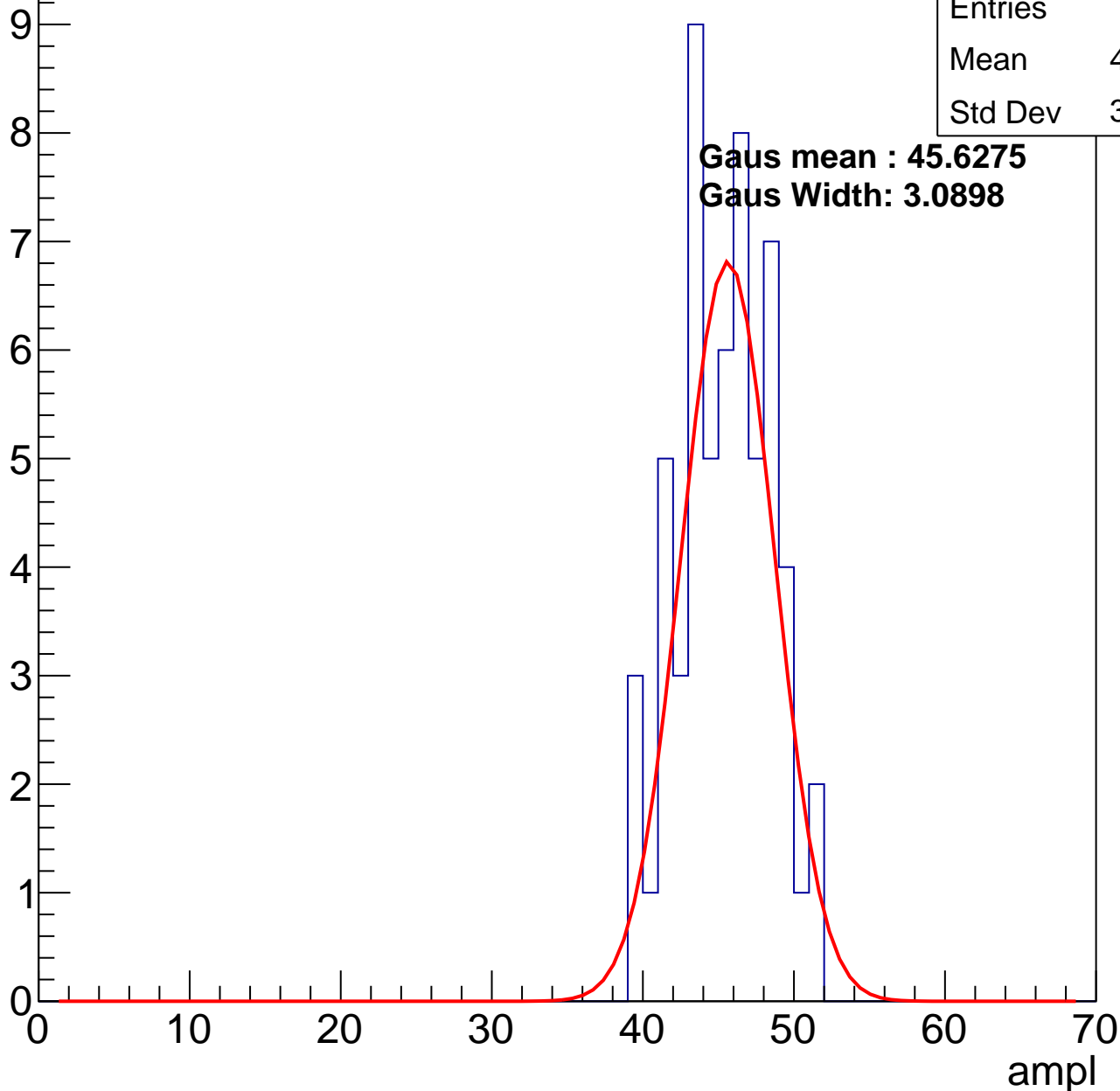
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	59
Mean	44.95
Std Dev	3.005

**Gaus mean : 45.6275**

**Gaus Width: 3.0898**

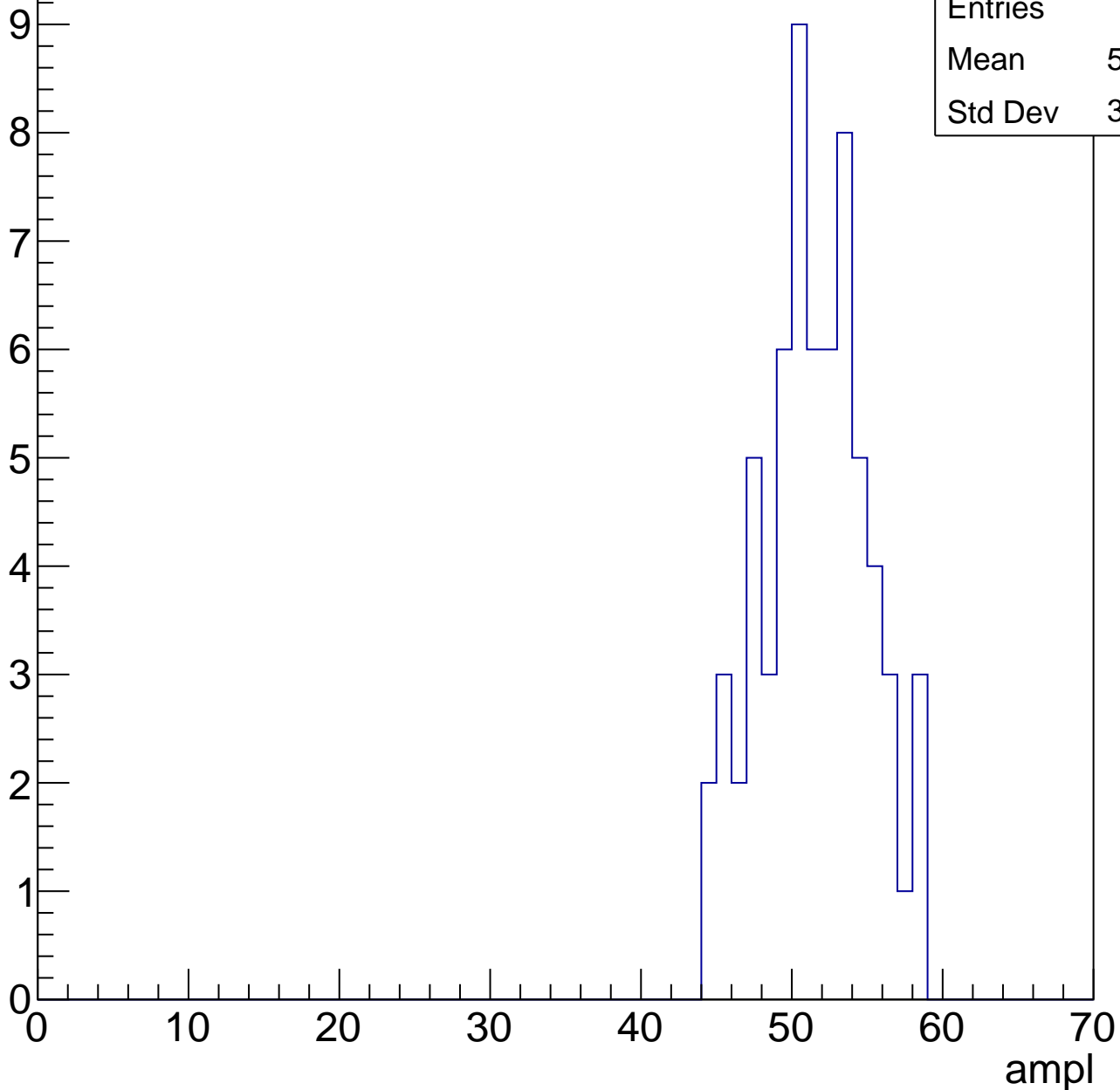


# B0L000S, U7-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	66
Mean	51.05
Std Dev	3.483



# B0L000S, U7-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	77
Mean	57.87
Std Dev	3.151

Entry

10

8

6

4

2

0

0

10

20

30

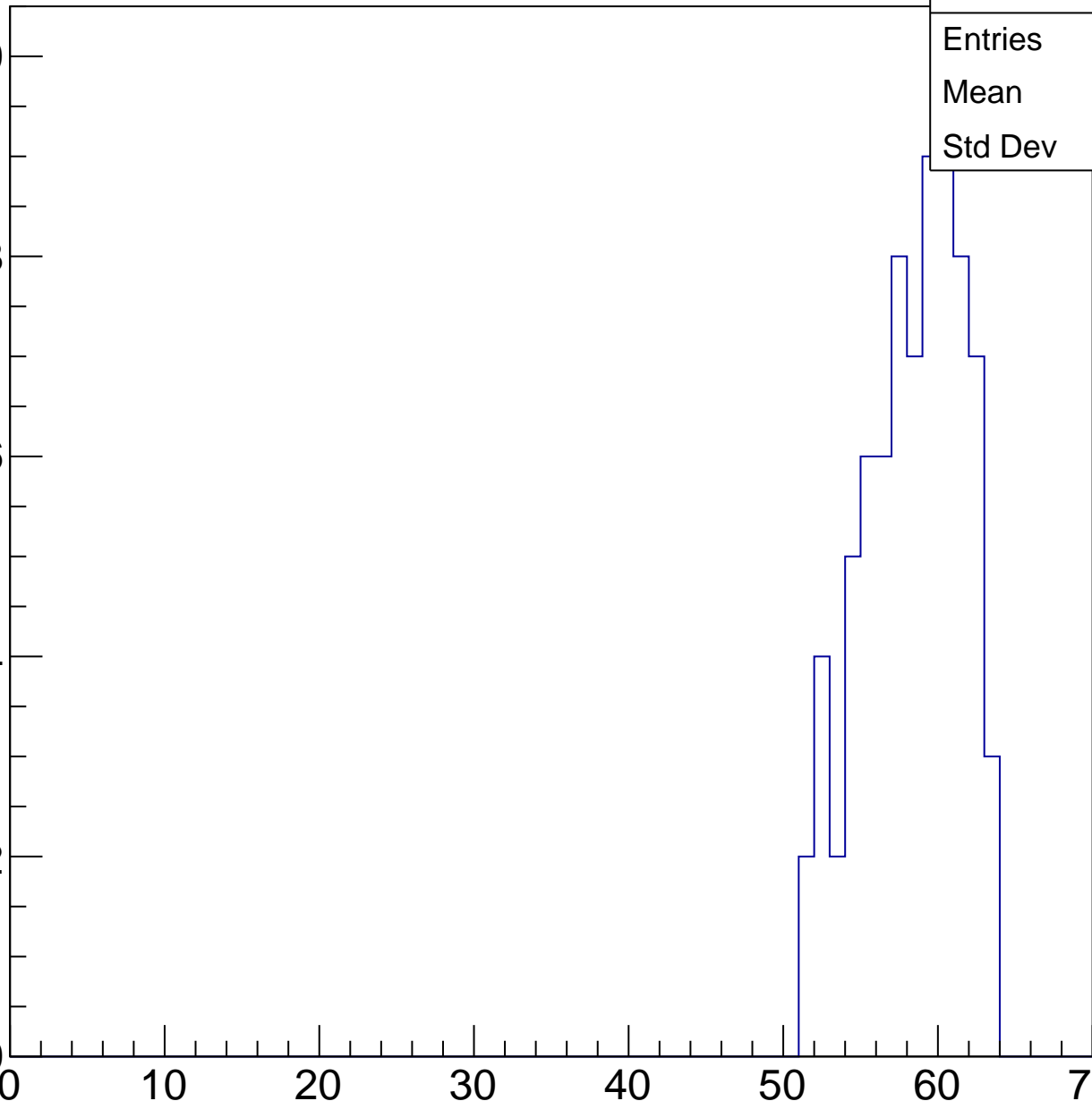
40

50

60

70

ampl

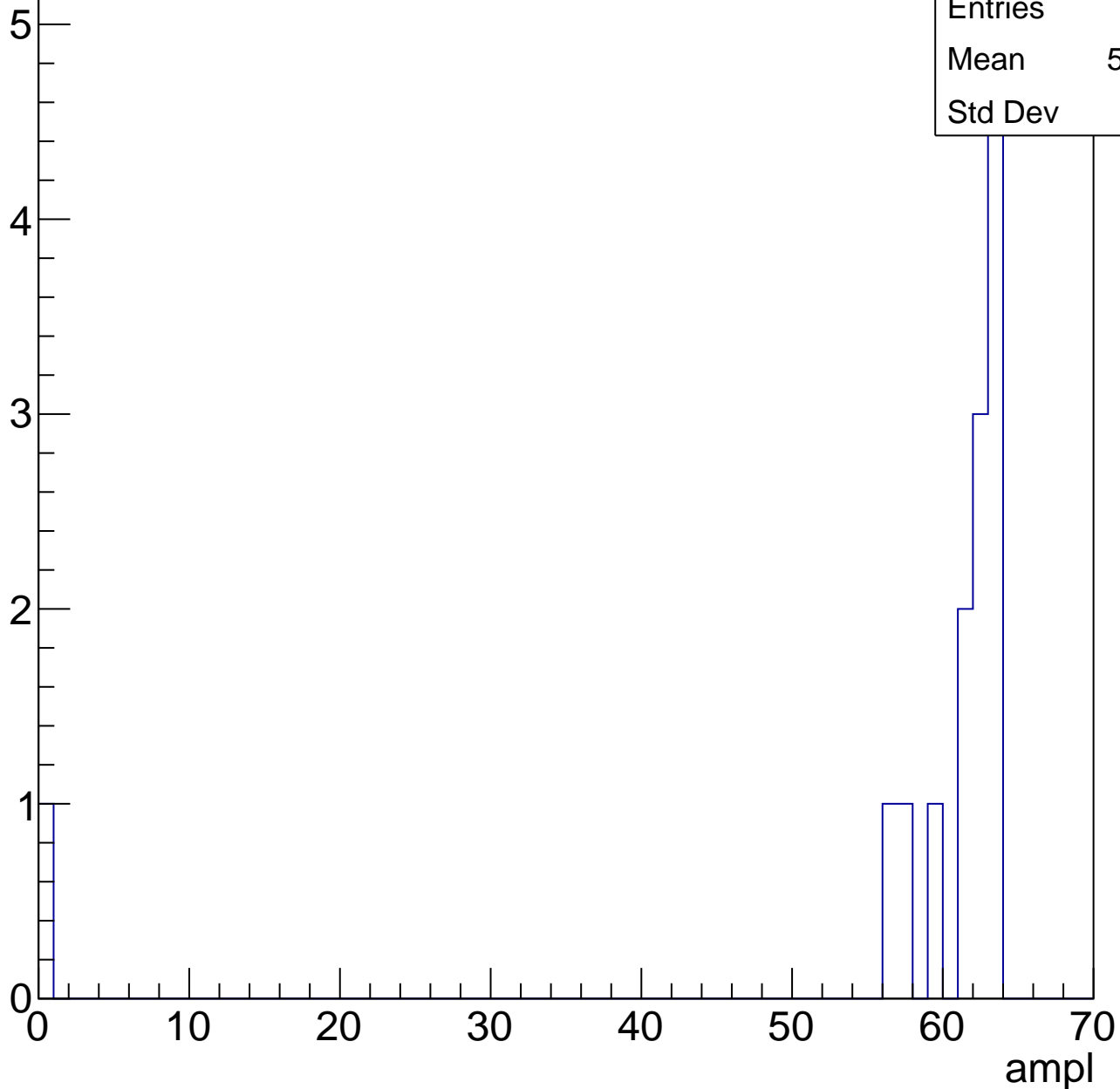


# B0L000S, U7-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	14
Mean	56.79
Std Dev	15.9



# B0L000S, U7-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

0 10 20 30 40 50 60 70

ampl



# B0L000S, U7-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L000S, U7-ch10, adc0

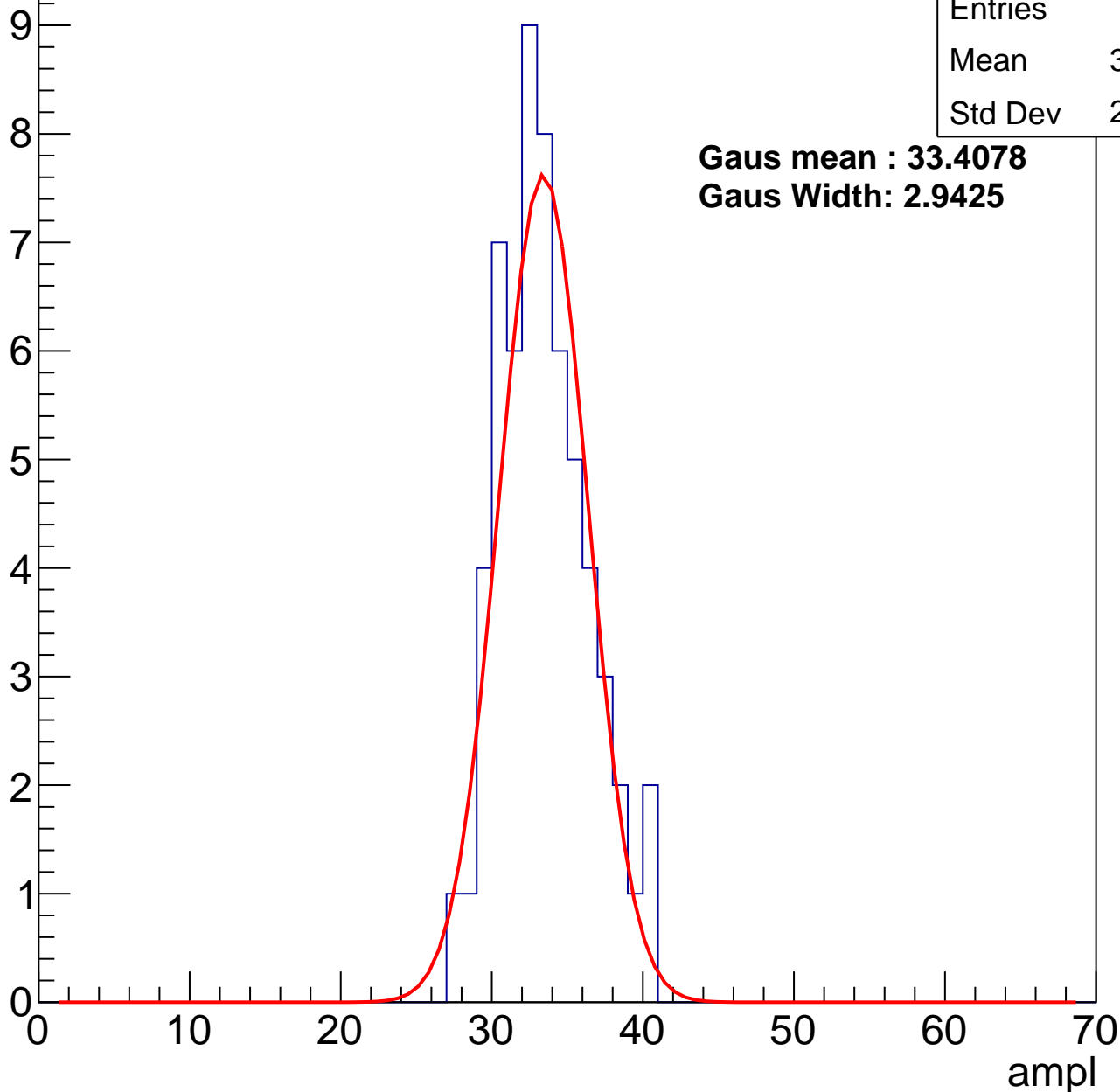
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	59
Mean	33.02
Std Dev	2.954

**Gaus mean : 33.4078**

**Gaus Width: 2.9425**



# B0L000S, U7-ch10, adc1

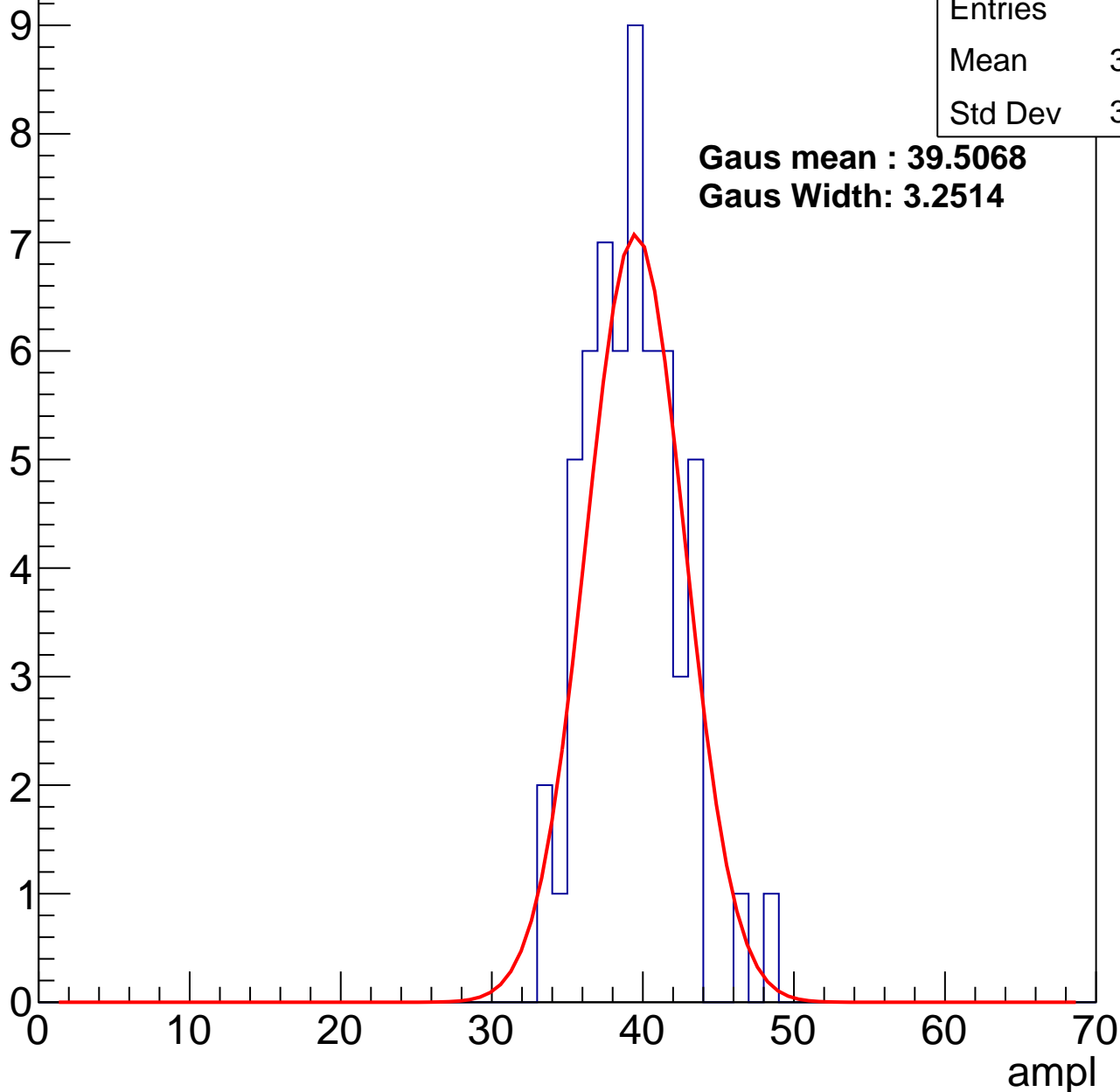
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	58
Mean	38.79
Std Dev	3.022

**Gaus mean : 39.5068**

**Gaus Width: 3.2514**



# B0L000S, U7-ch10, adc2

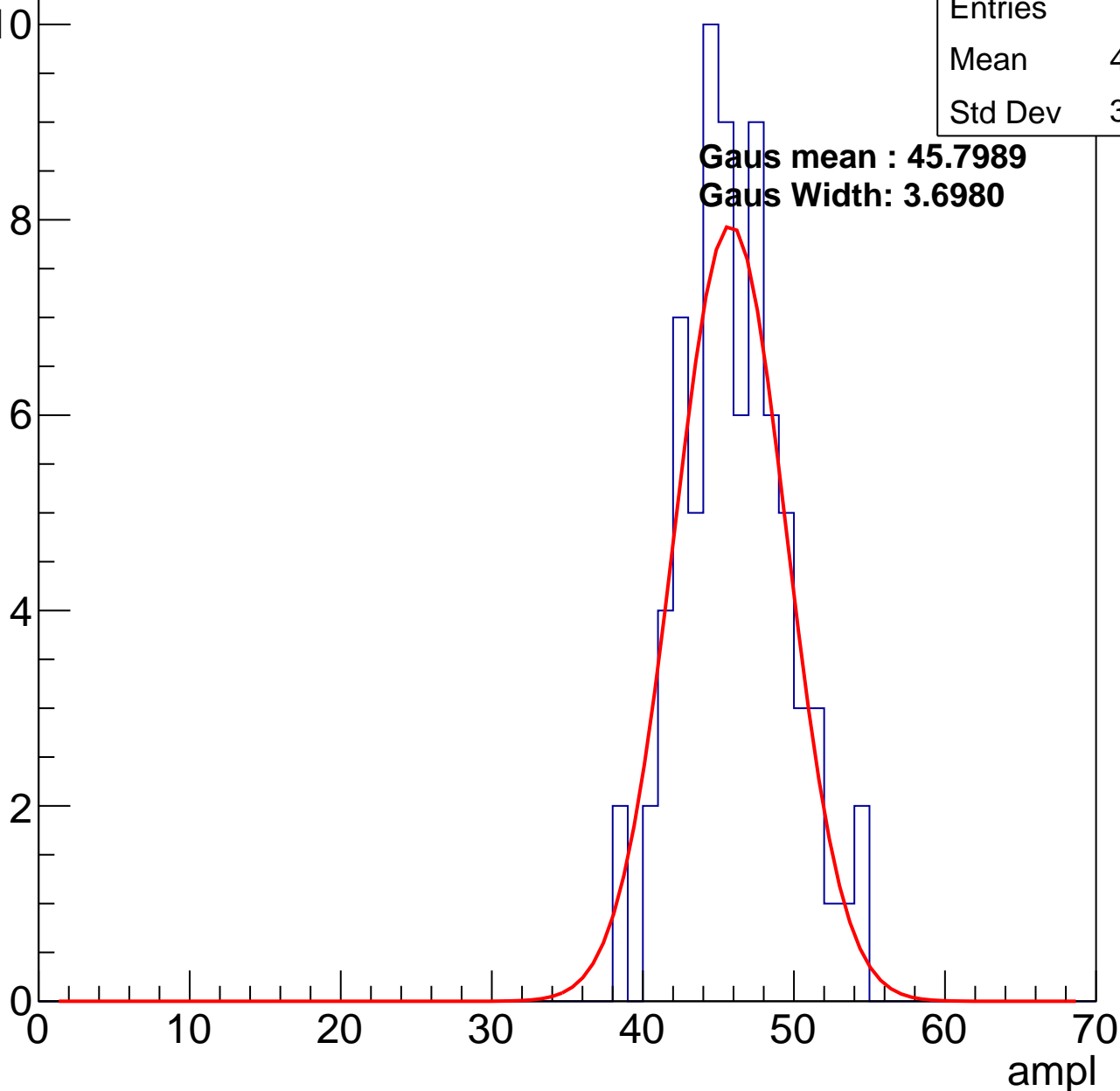
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	75
Mean	45.63
Std Dev	3.482

**Gaus mean : 45.7989**

**Gaus Width: 3.6980**

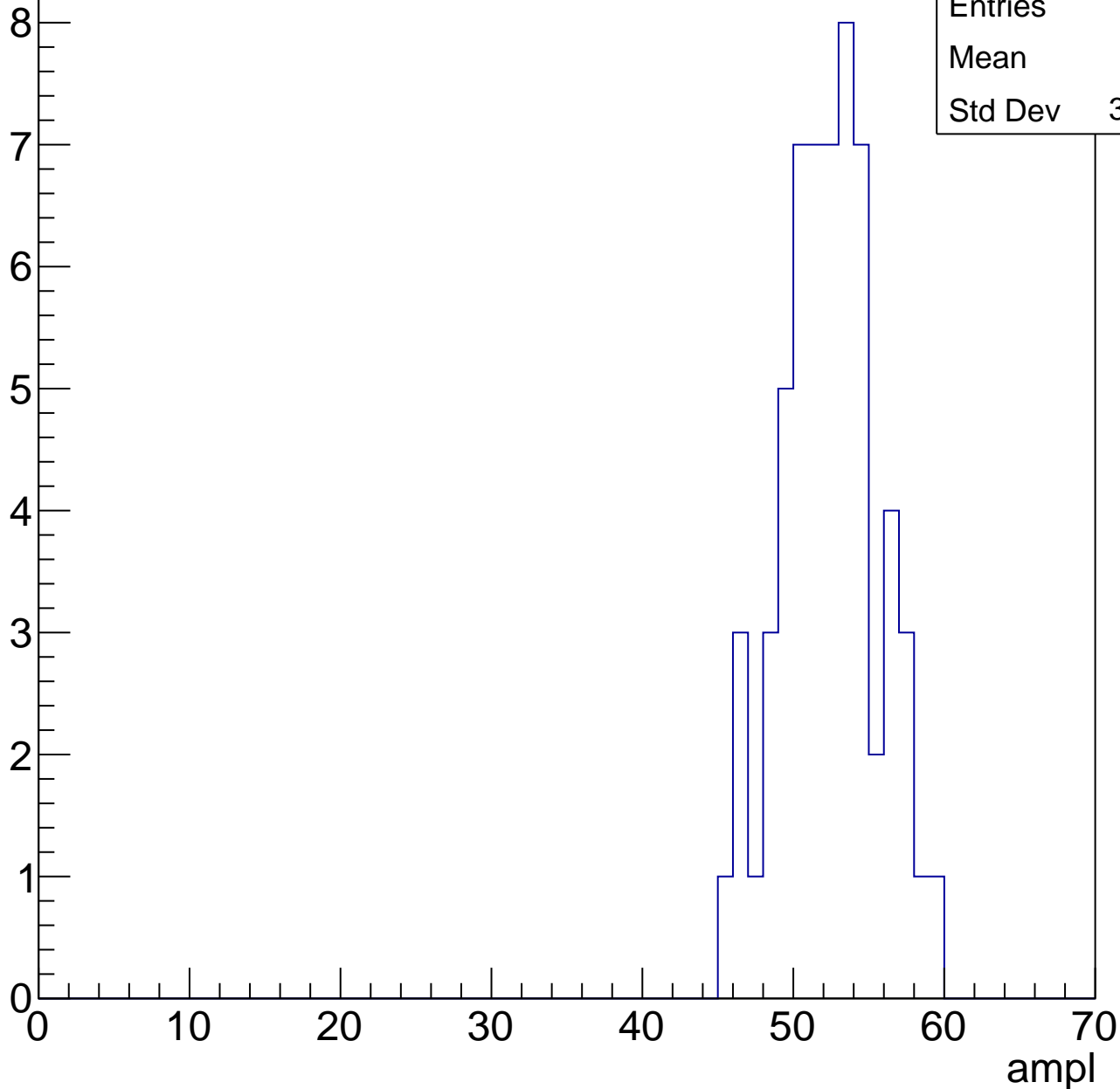


# B0L000S, U7-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	60
Mean	51.9
Std Dev	3.129

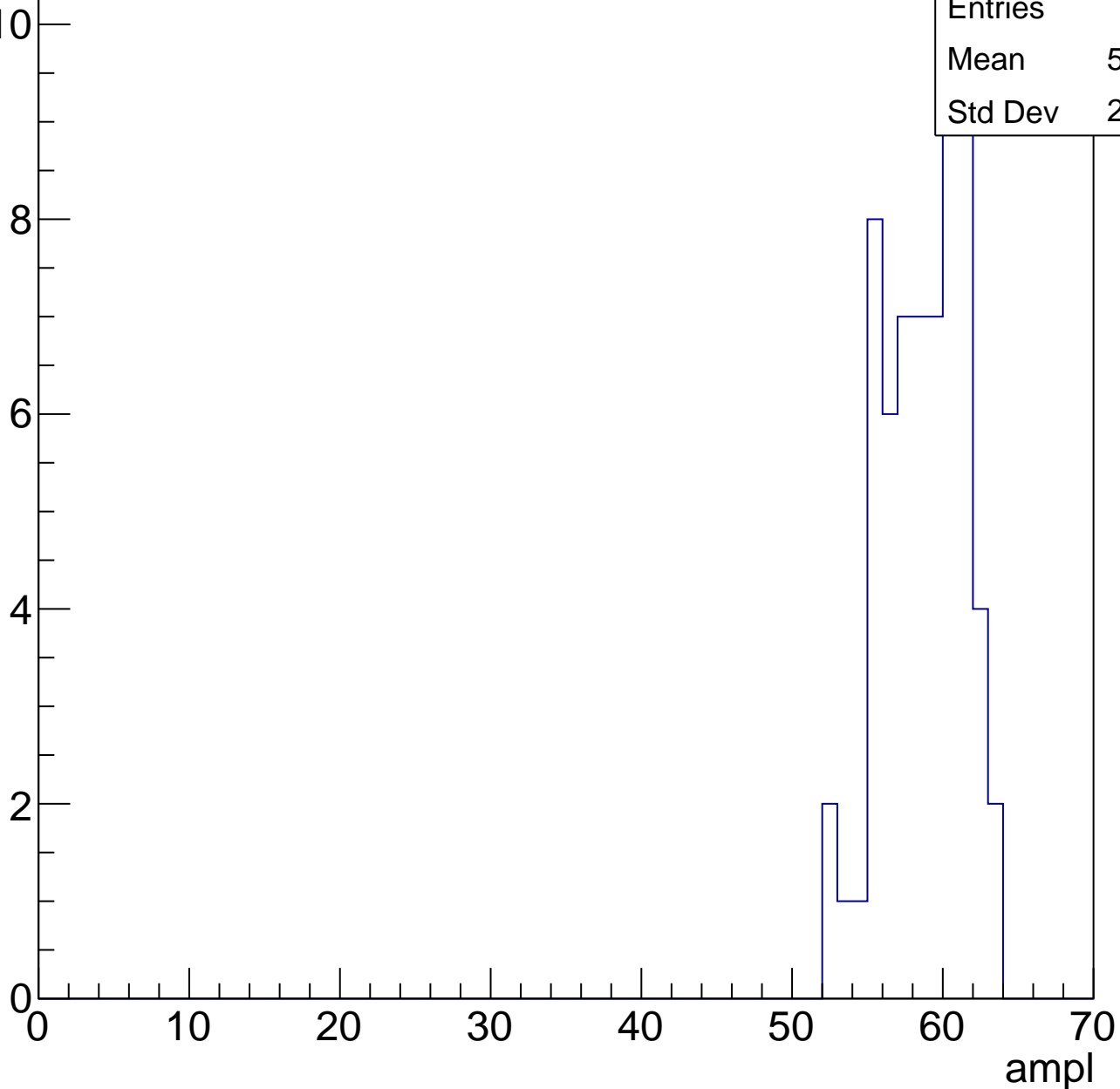


# B0L000S, U7-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	65
Mean	58.29
Std Dev	2.664

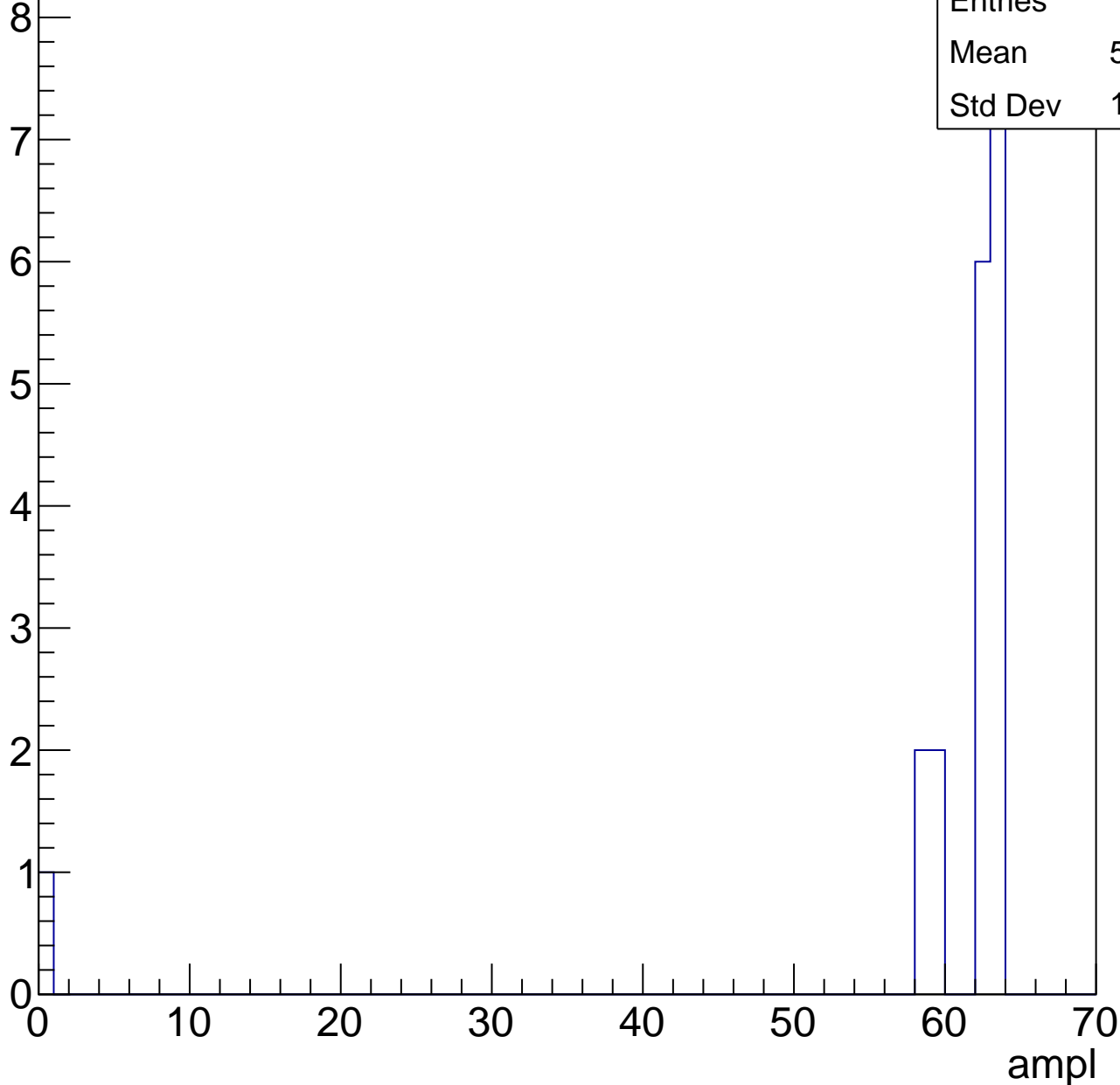


# B0L000S, U7-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	19
Mean	58.42
Std Dev	13.88



# B0L000S, U7-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L000S, U7-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch11, adc0

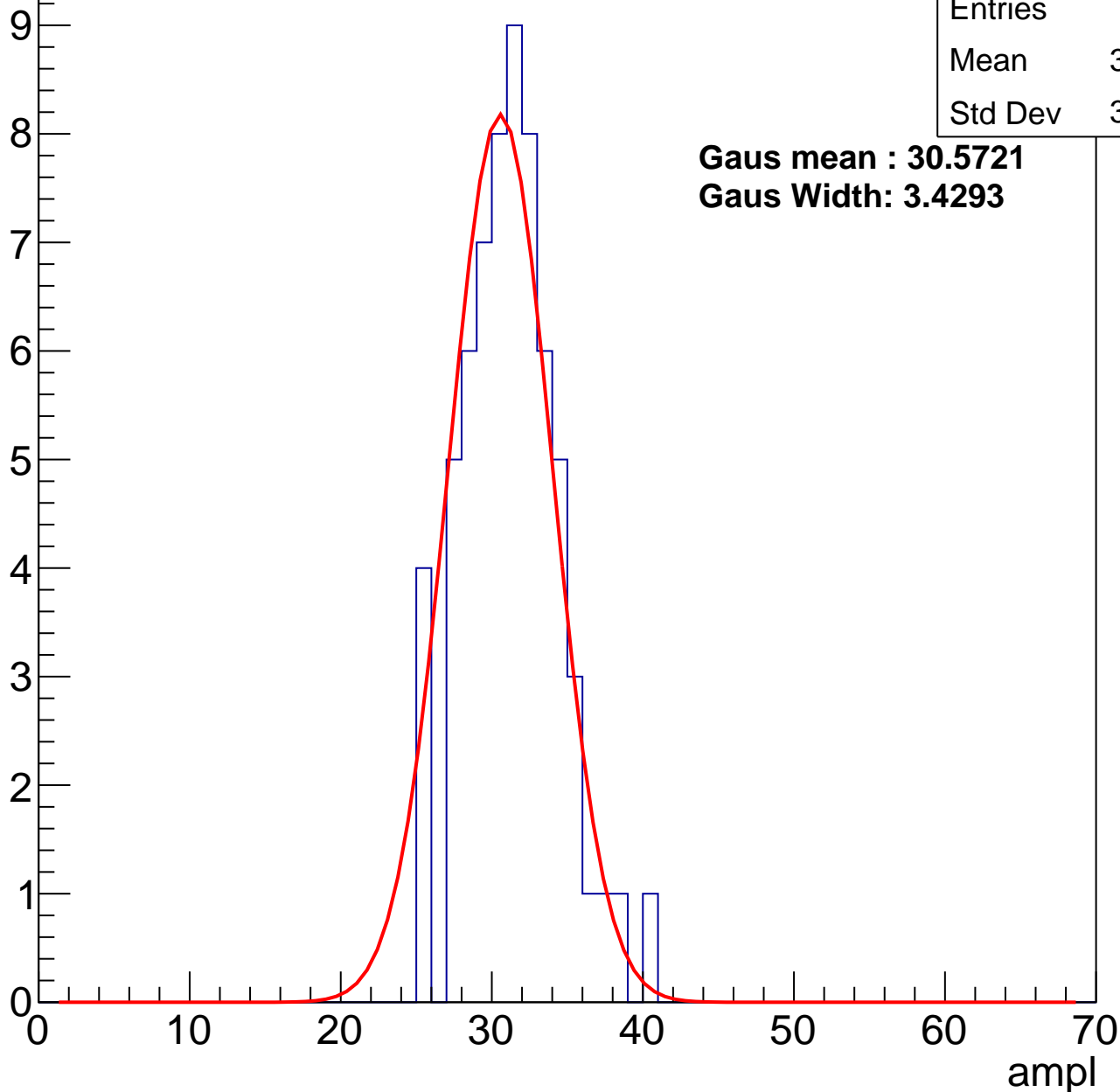
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	65
Mean	30.85
Std Dev	3.109

**Gaus mean : 30.5721**

**Gaus Width: 3.4293**



# B0L000S, U7-ch11, adc1

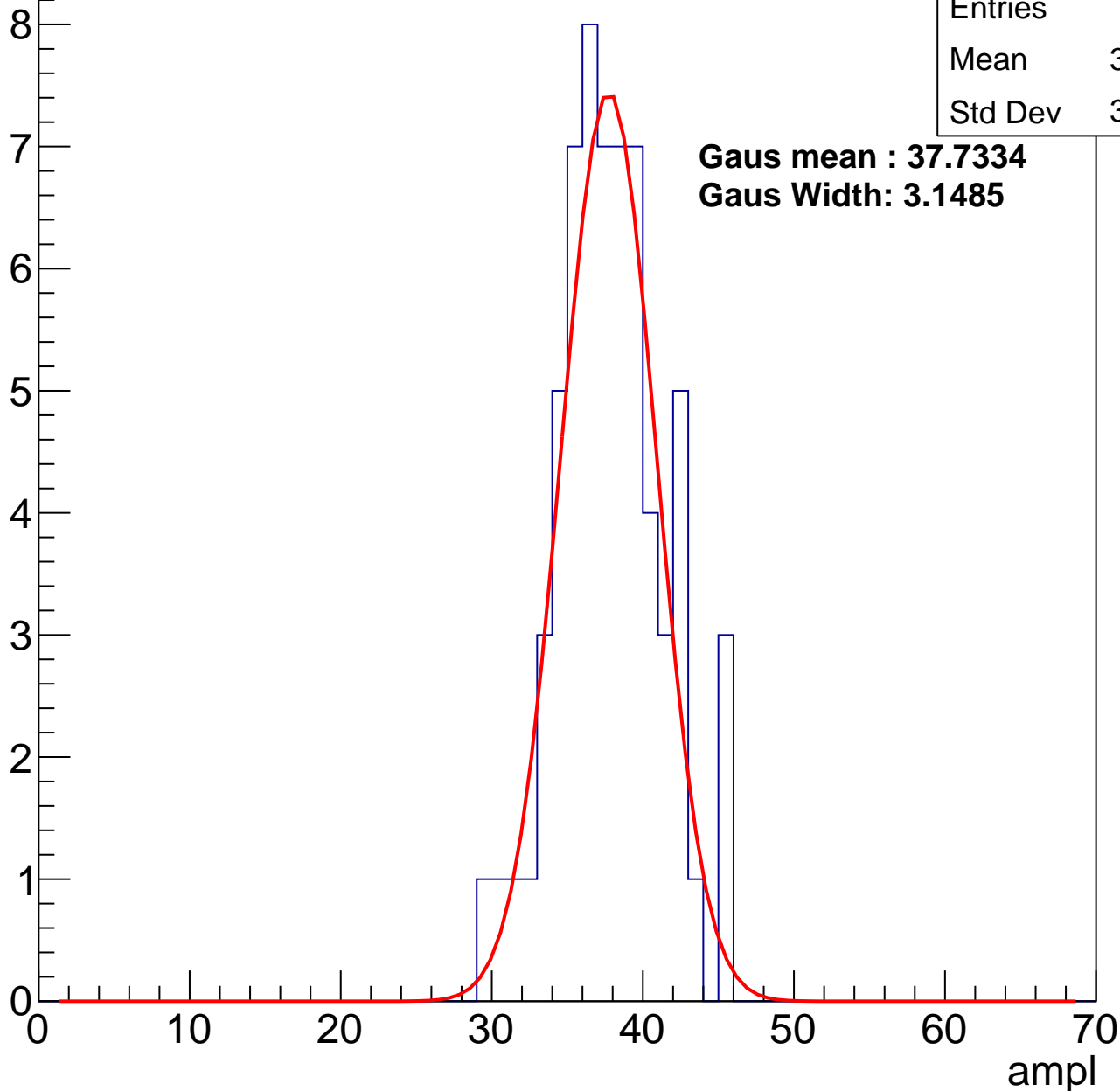
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	64
Mean	37.39
Std Dev	3.458

**Gaus mean : 37.7334**

**Gaus Width: 3.1485**



# B0L000S, U7-ch11, adc2

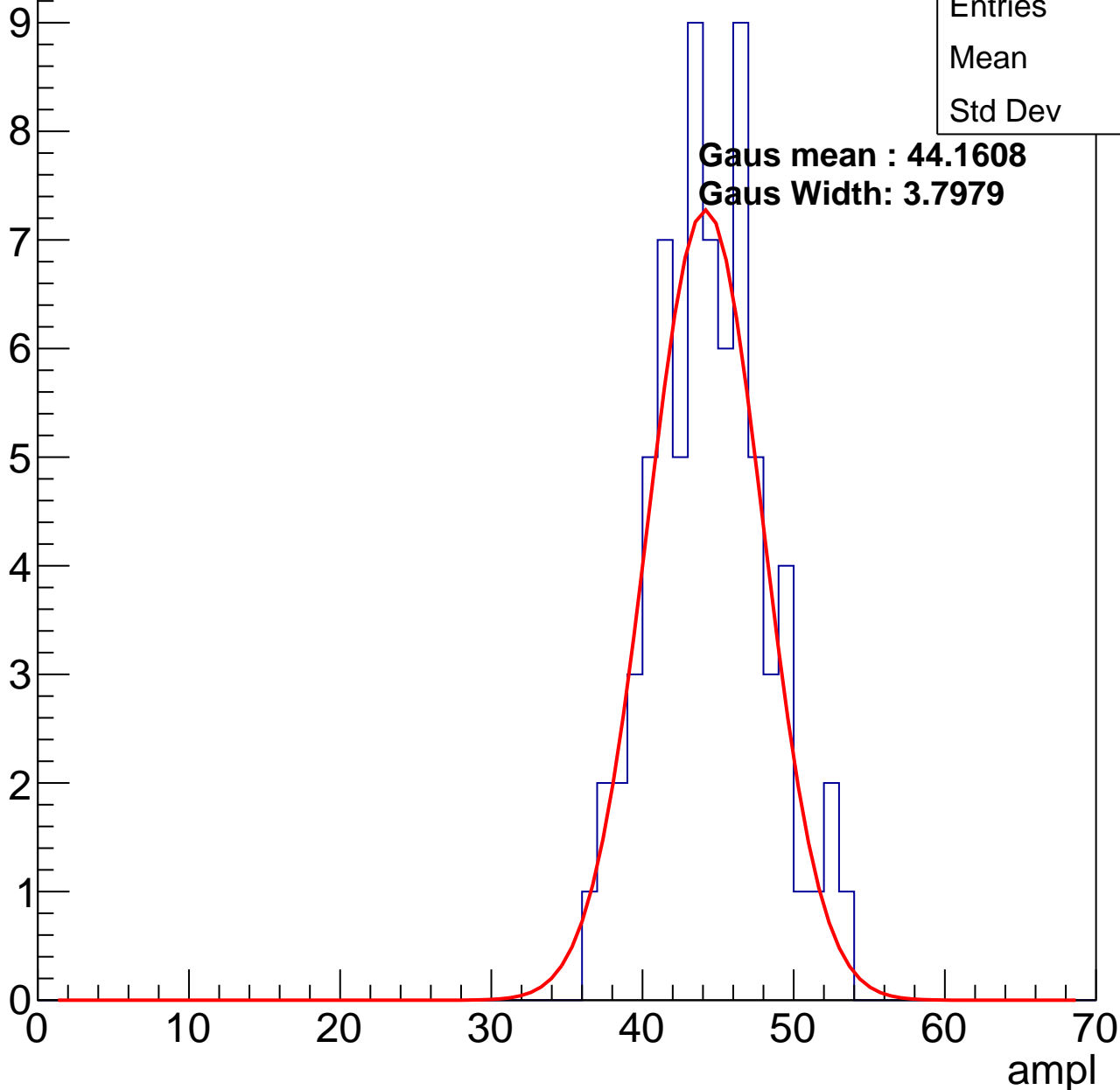
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	73
Mean	44
Std Dev	3.72

**Gaus mean : 44.1608**

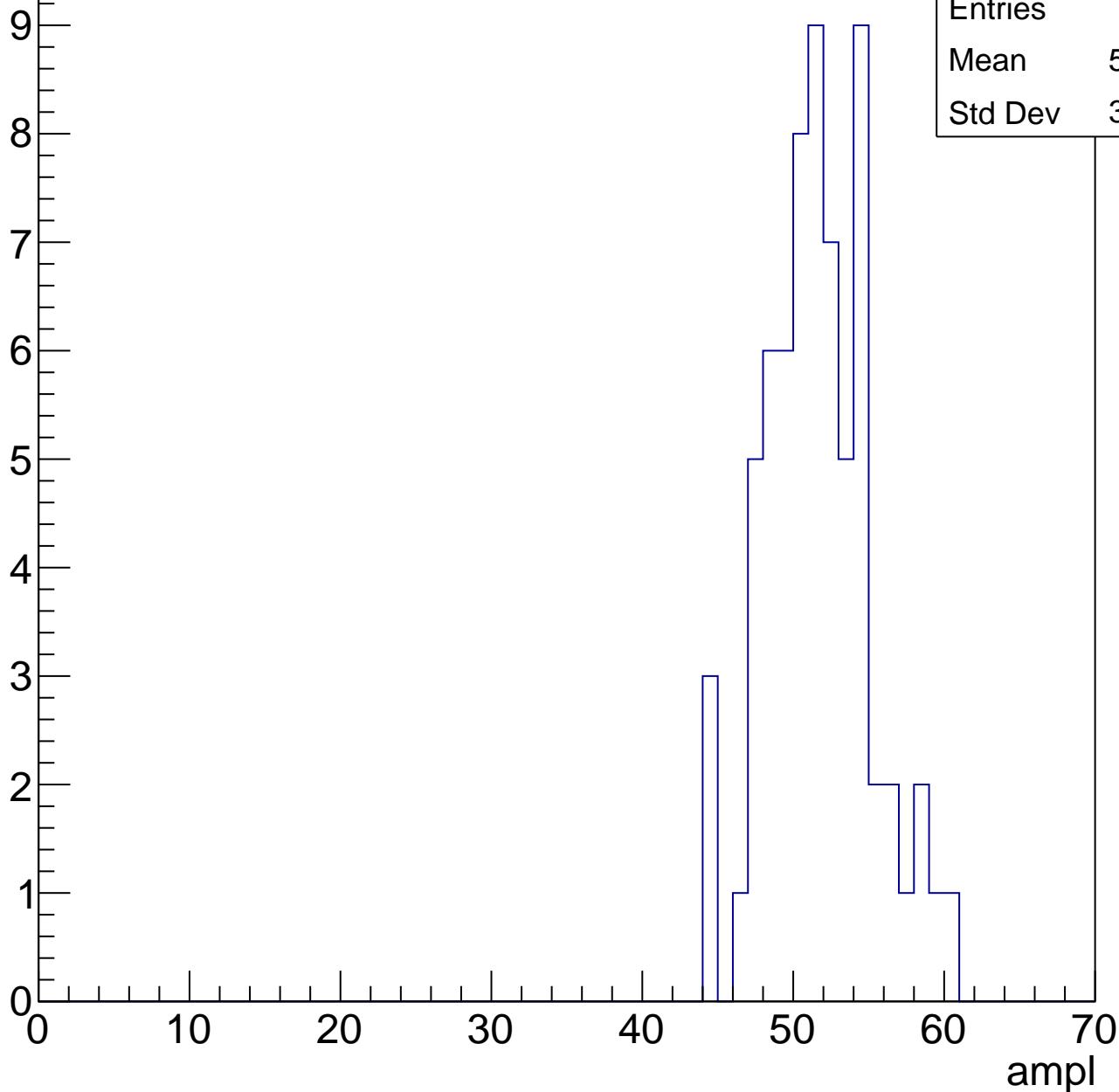
**Gaus Width: 3.7979**



# B0L000S, U7-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

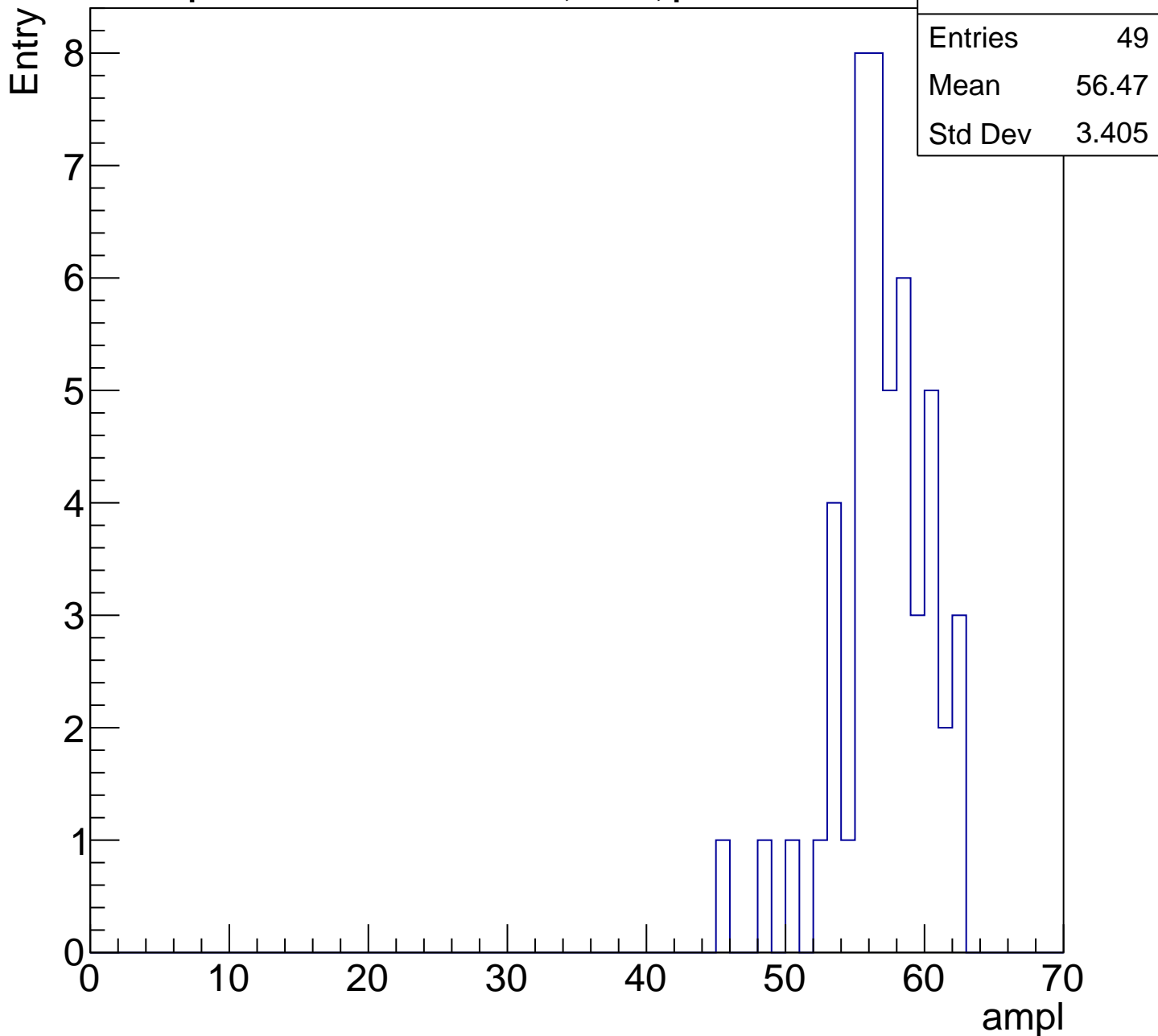
Entry



Entries	68
Mean	51.22
Std Dev	3.438

# B0L000S, U7-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

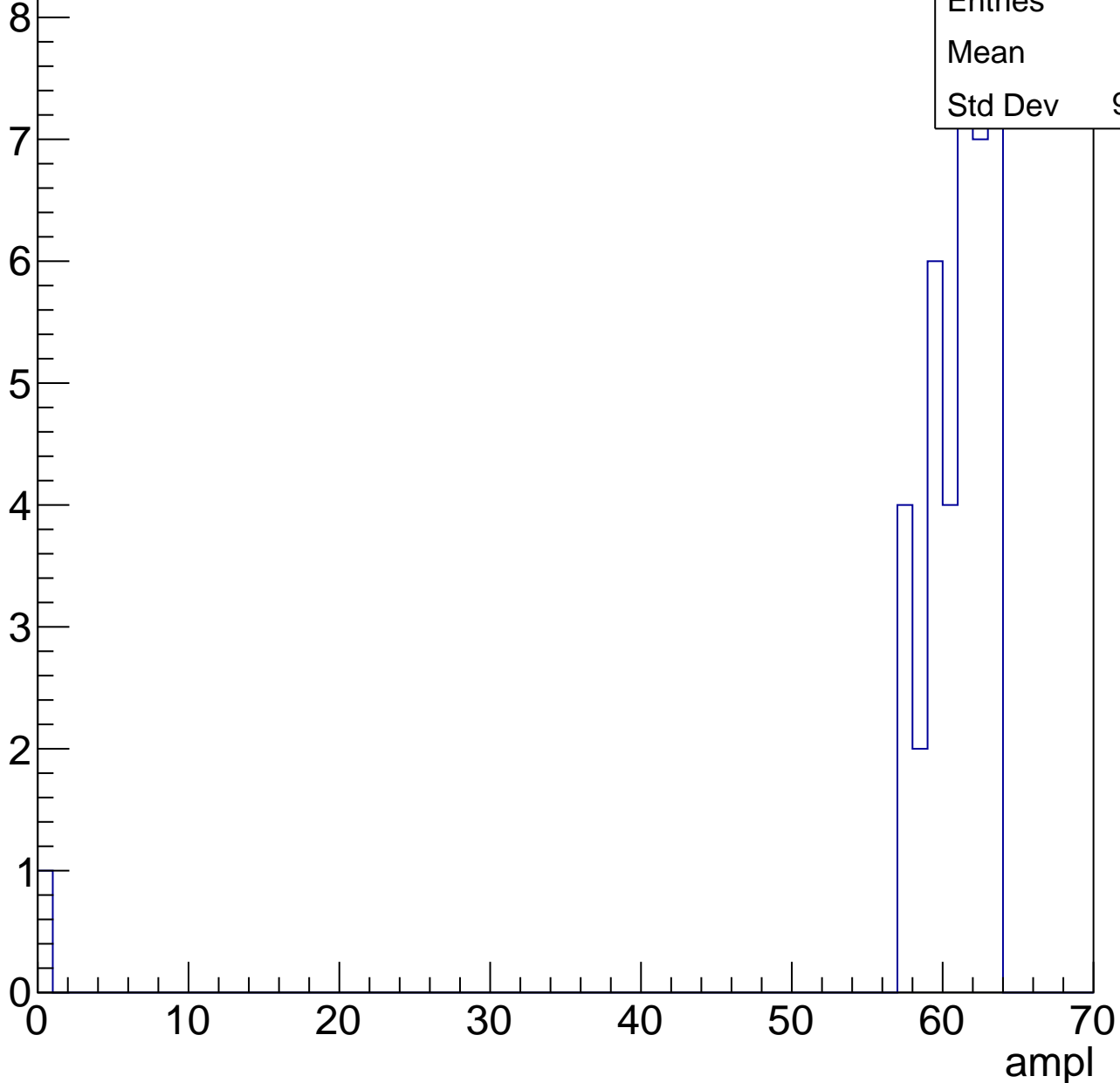


# B0L000S, U7-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	40
Mean	59.1
Std Dev	9.651



# B0L000S, U7-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	1
Mean	24
Std Dev	0

# B0L000S, U7-ch12, adc0

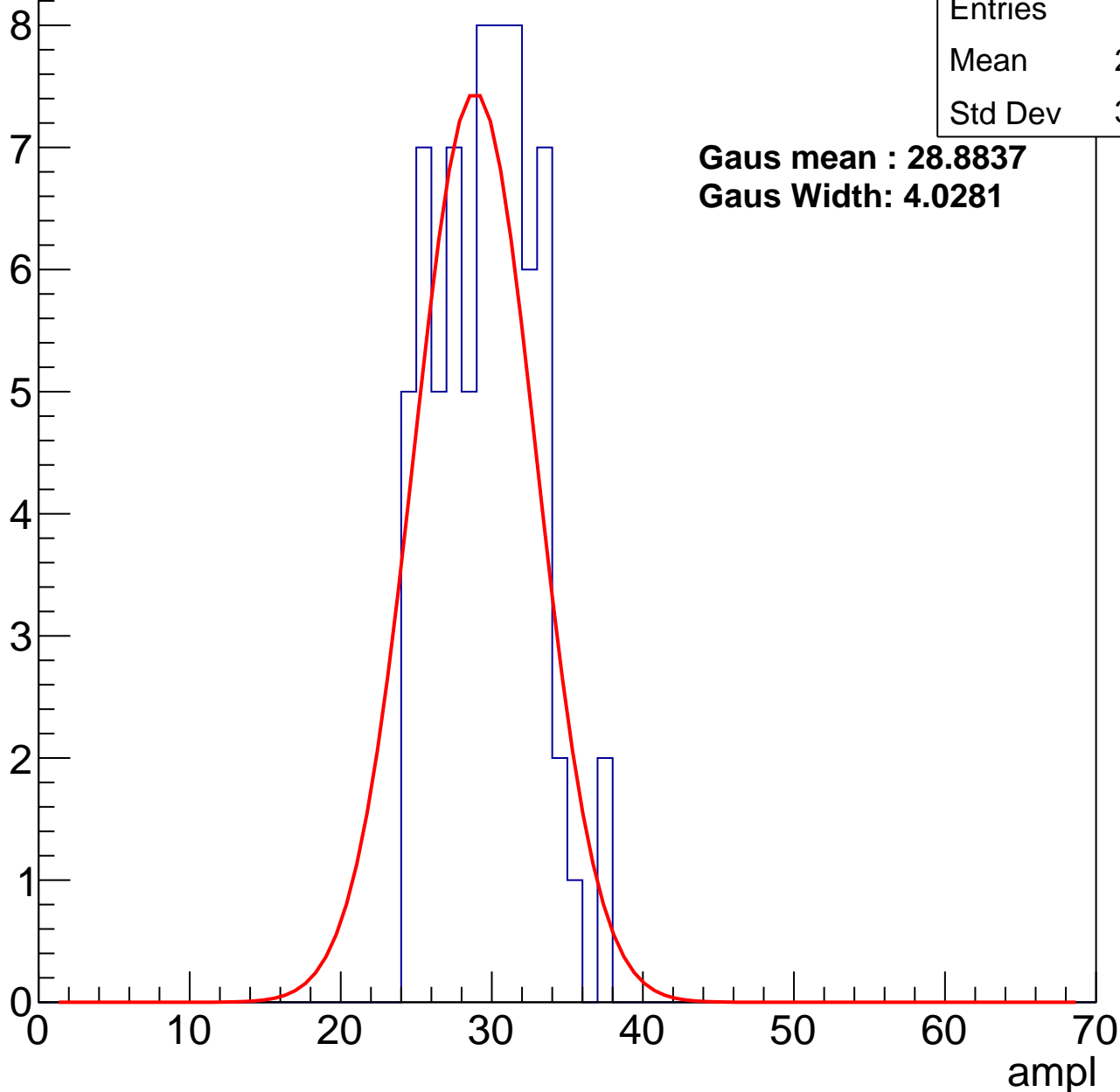
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	71
Mean	29.21
Std Dev	3.211

**Gaus mean : 28.8837**

**Gaus Width: 4.0281**



# B0L000S, U7-ch12, adc1

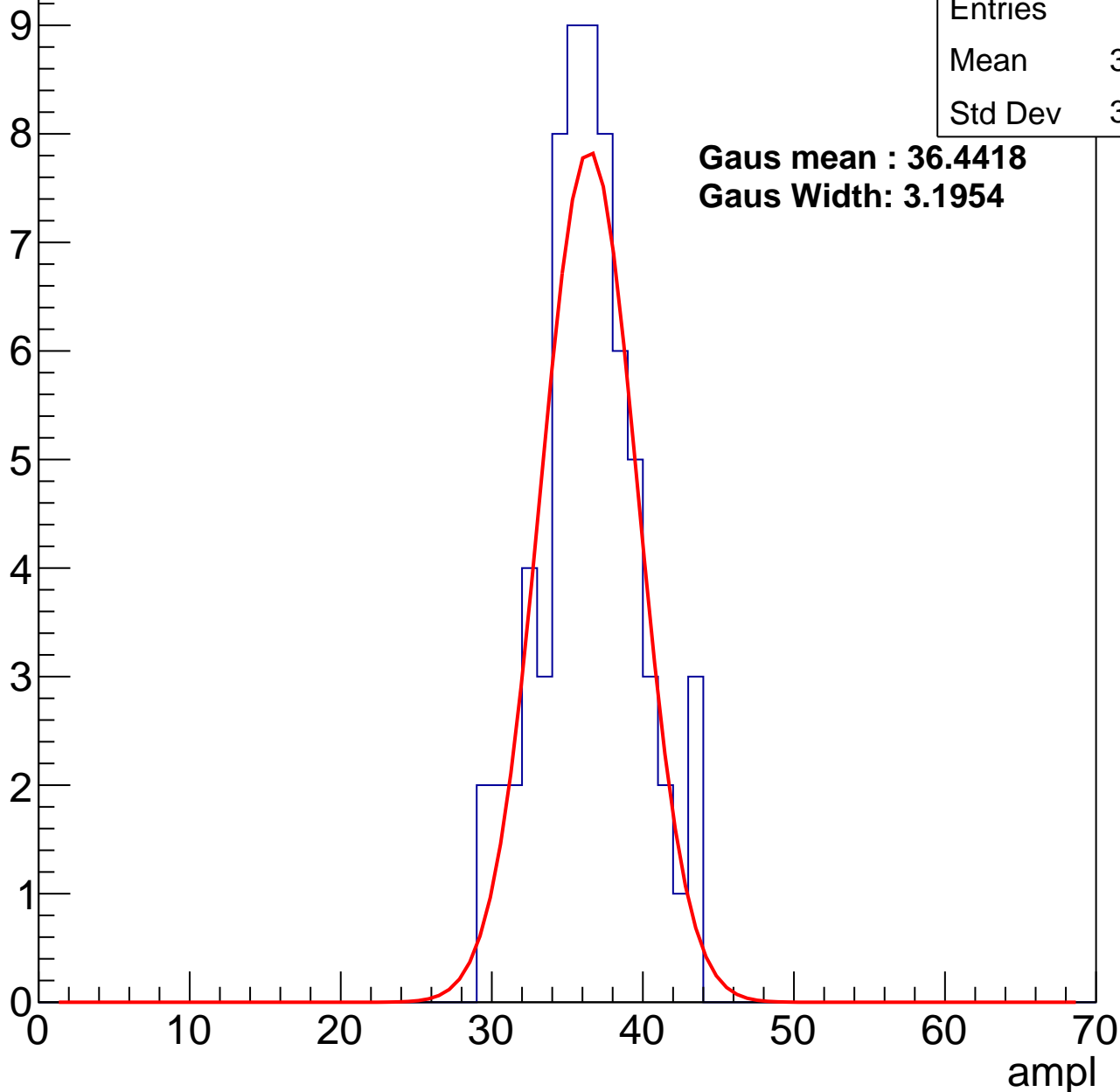
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	67
Mean	35.97
Std Dev	3.255

**Gaus mean : 36.4418**

**Gaus Width: 3.1954**



# B0L000S, U7-ch12, adc2

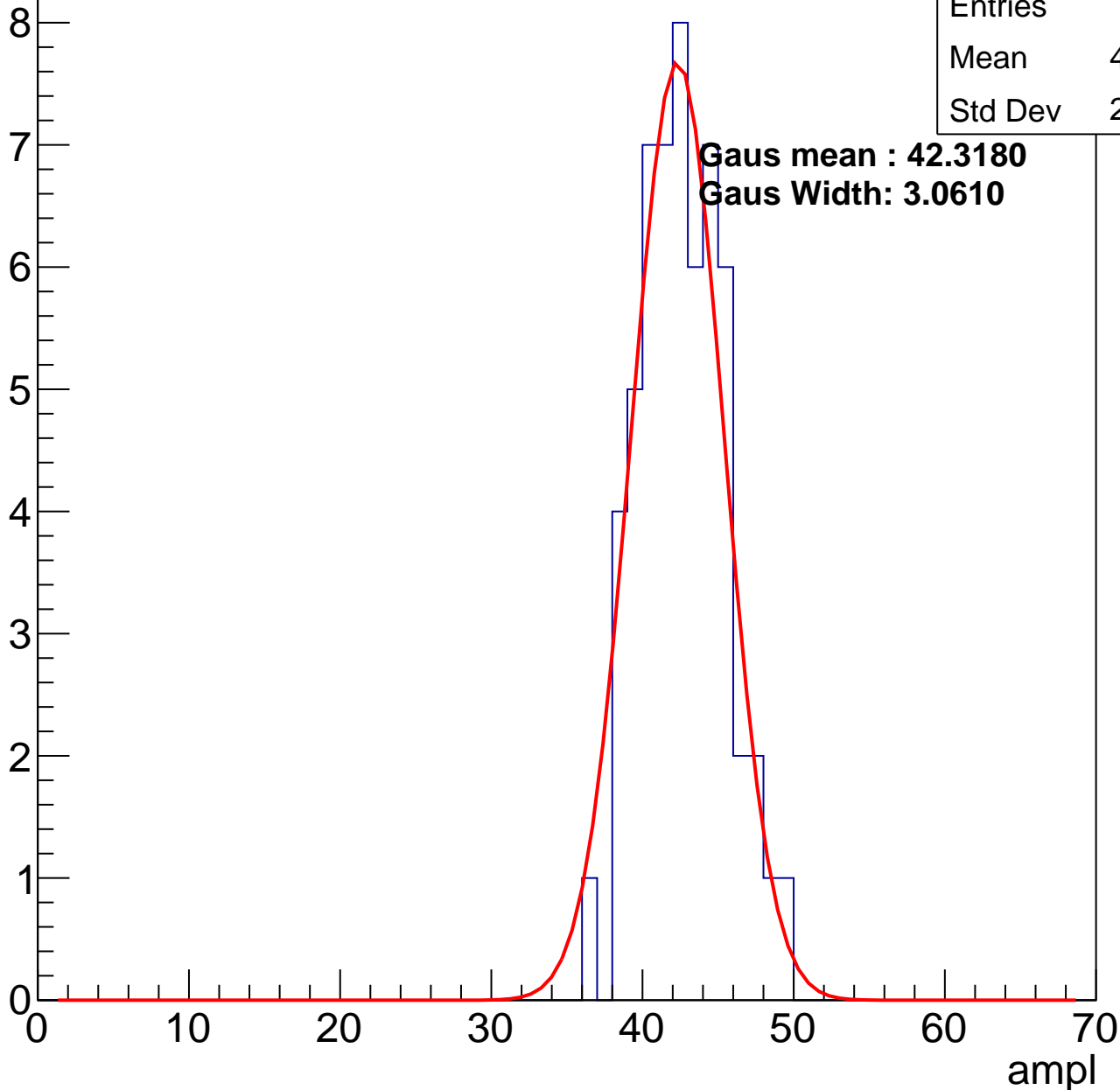
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	57
Mean	42.19
Std Dev	2.756

**Gaus mean : 42.3180**

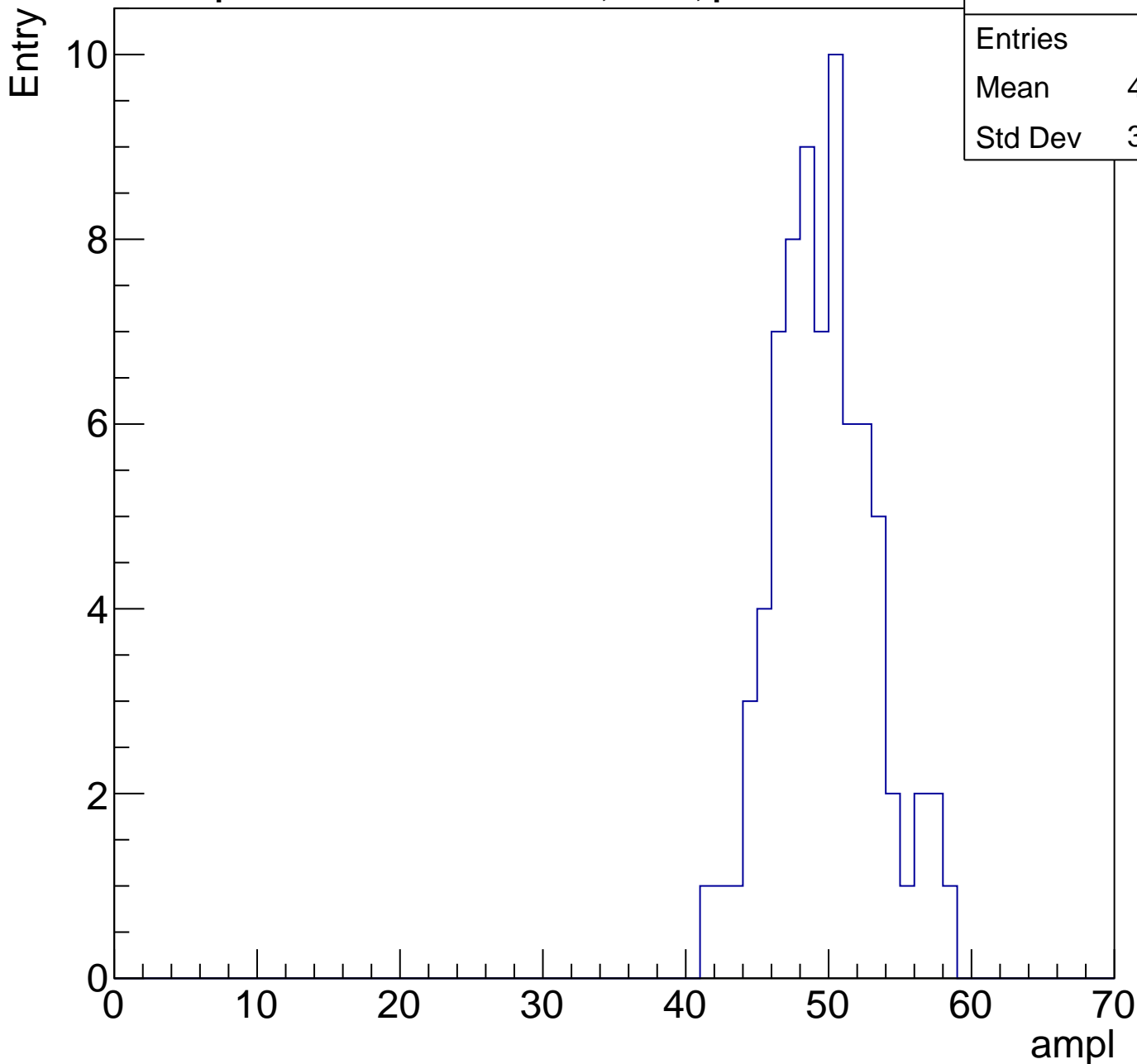
**Gaus Width: 3.0610**



# B0L000S, U7-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

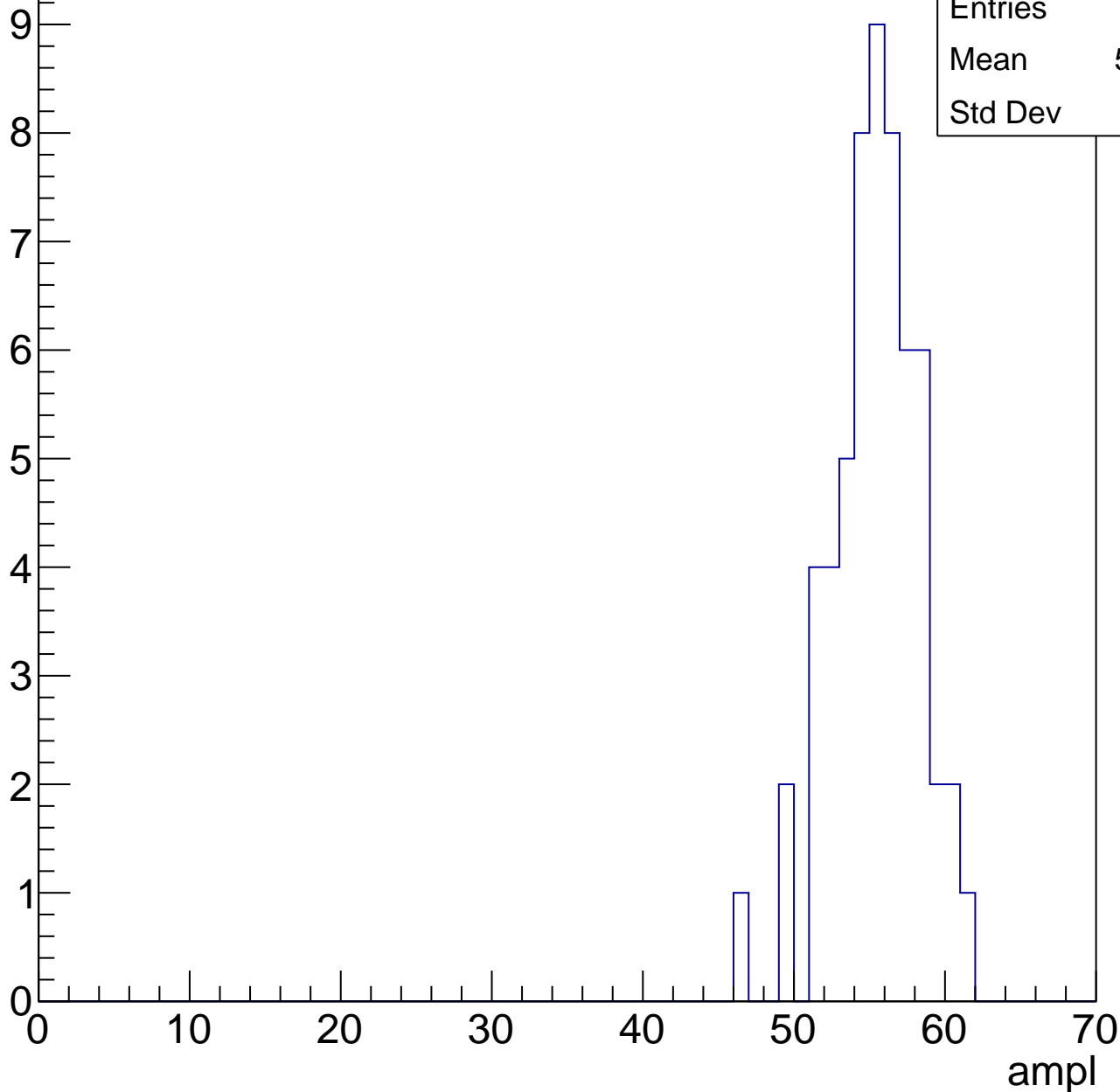
Entries	76
Mean	49.22
Std Dev	3.534



# B0L000S, U7-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	58
Mean	54.91
Std Dev	2.89

# B0L000S, U7-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

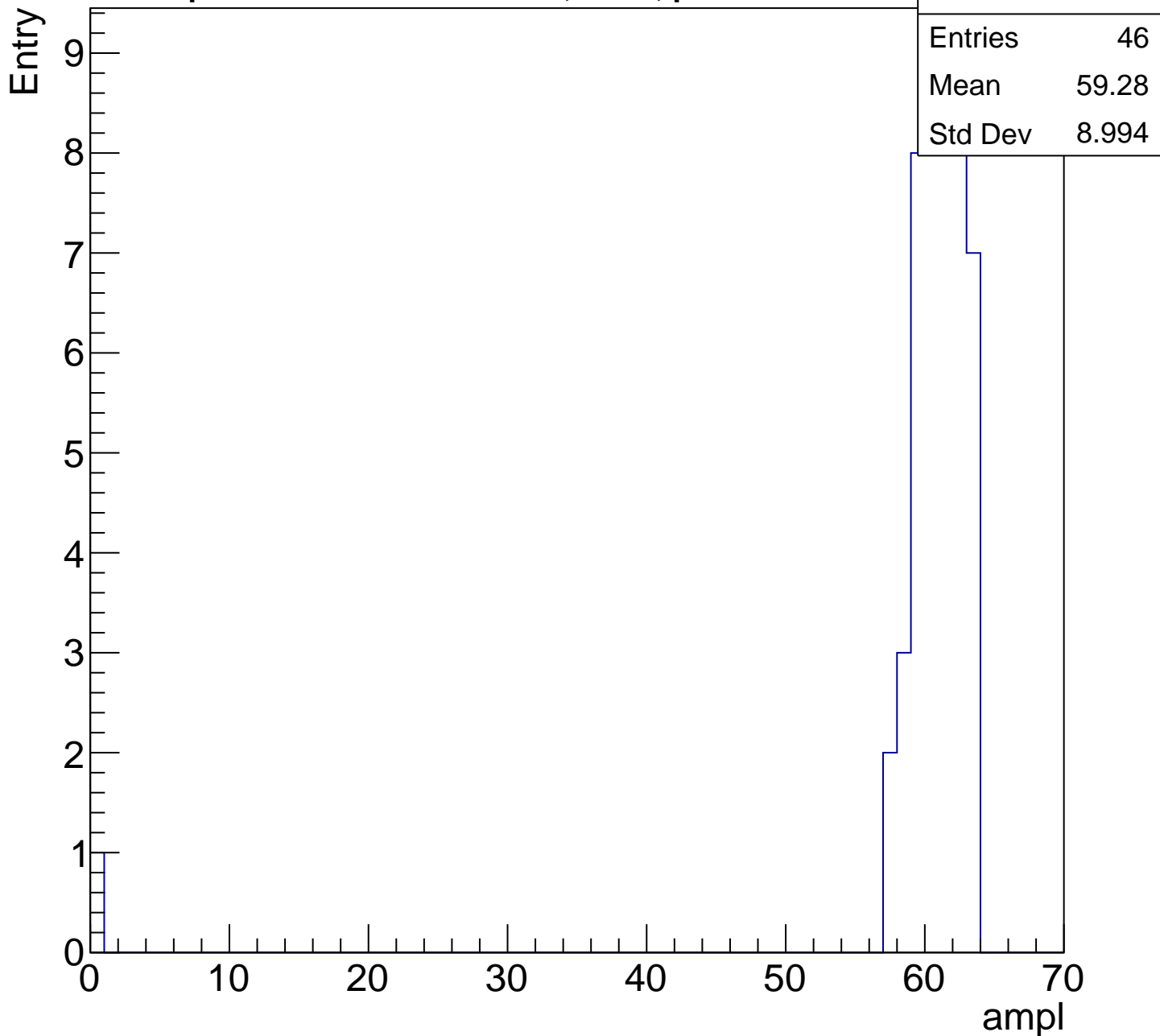
Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	46
Mean	59.28
Std Dev	8.994

ampl

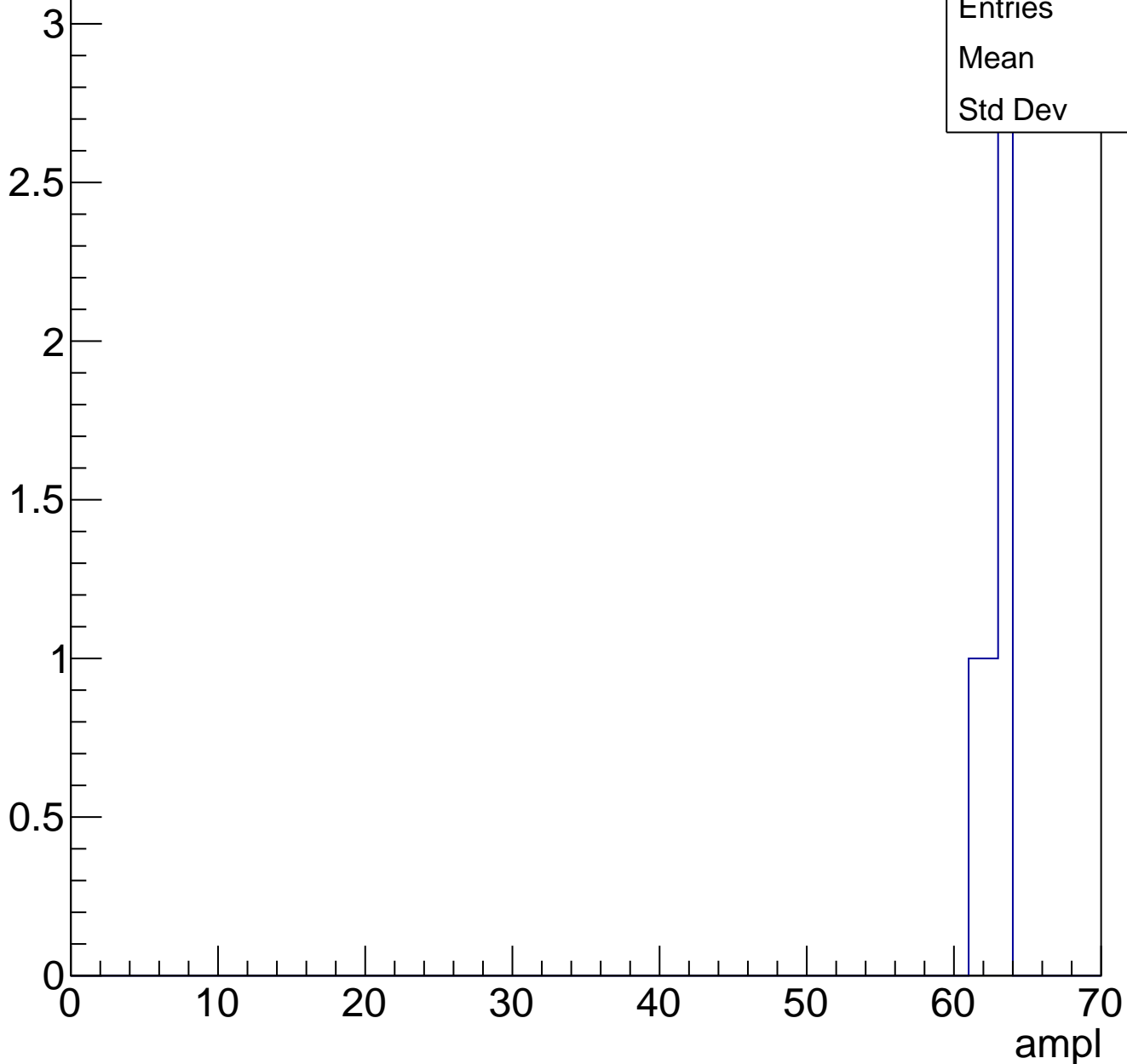
0 10 20 30 40 50 60 70



# B0L000S, U7-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L000S, U7-ch13, adc0

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	75
Mean	31.25
Std Dev	3.414

**Gaus mean : 31.9868**

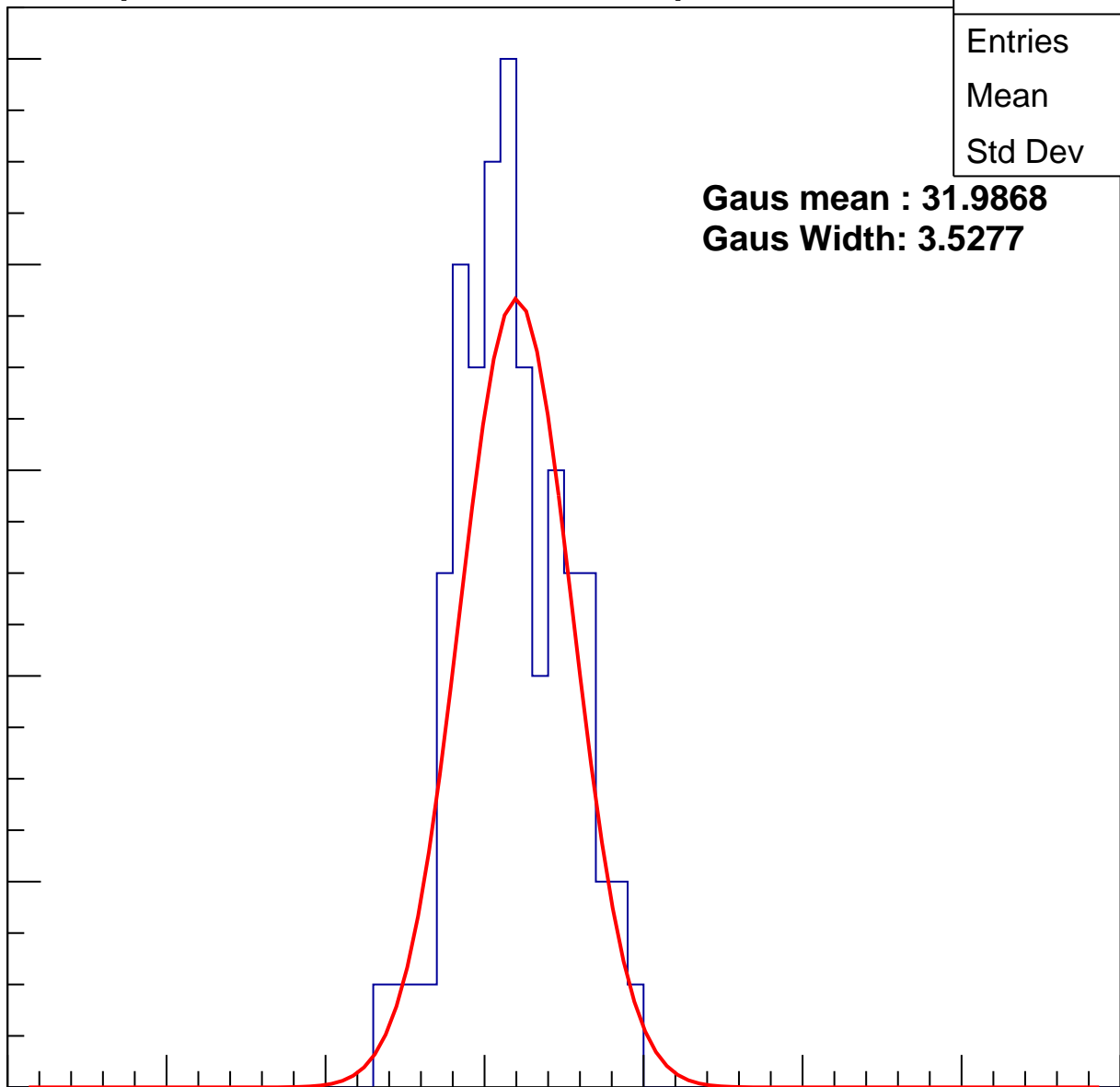
**Gaus Width: 3.5277**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L000S, U7-ch13, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	75
Mean	38.37
Std Dev	3.463

**Gaus mean : 38.7591**

**Gaus Width: 4.6108**

10

8

6

4

2

0

0

10

20

30

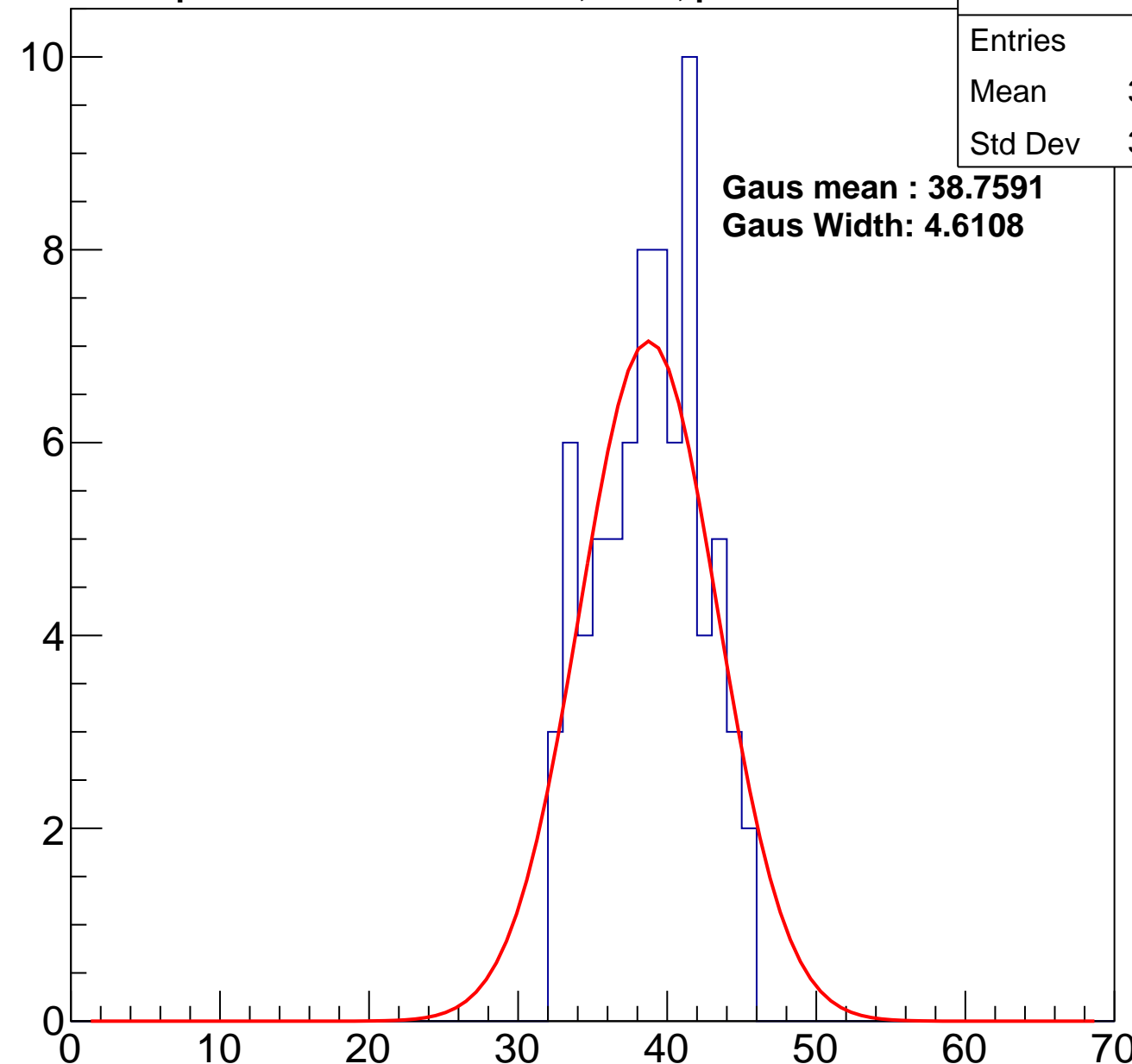
40

50

60

70

ampl

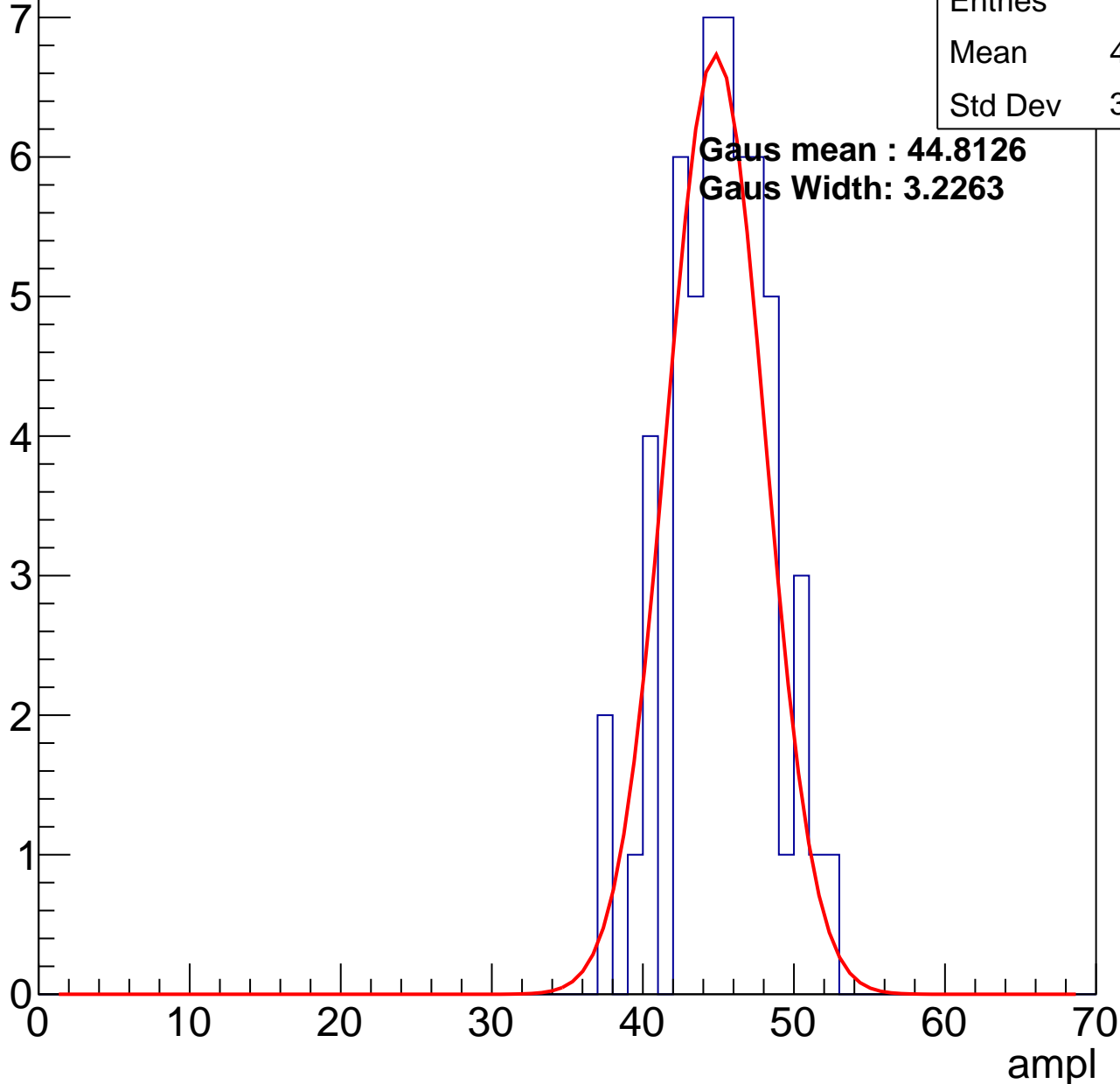


# B0L000S, U7-ch13, adc2

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

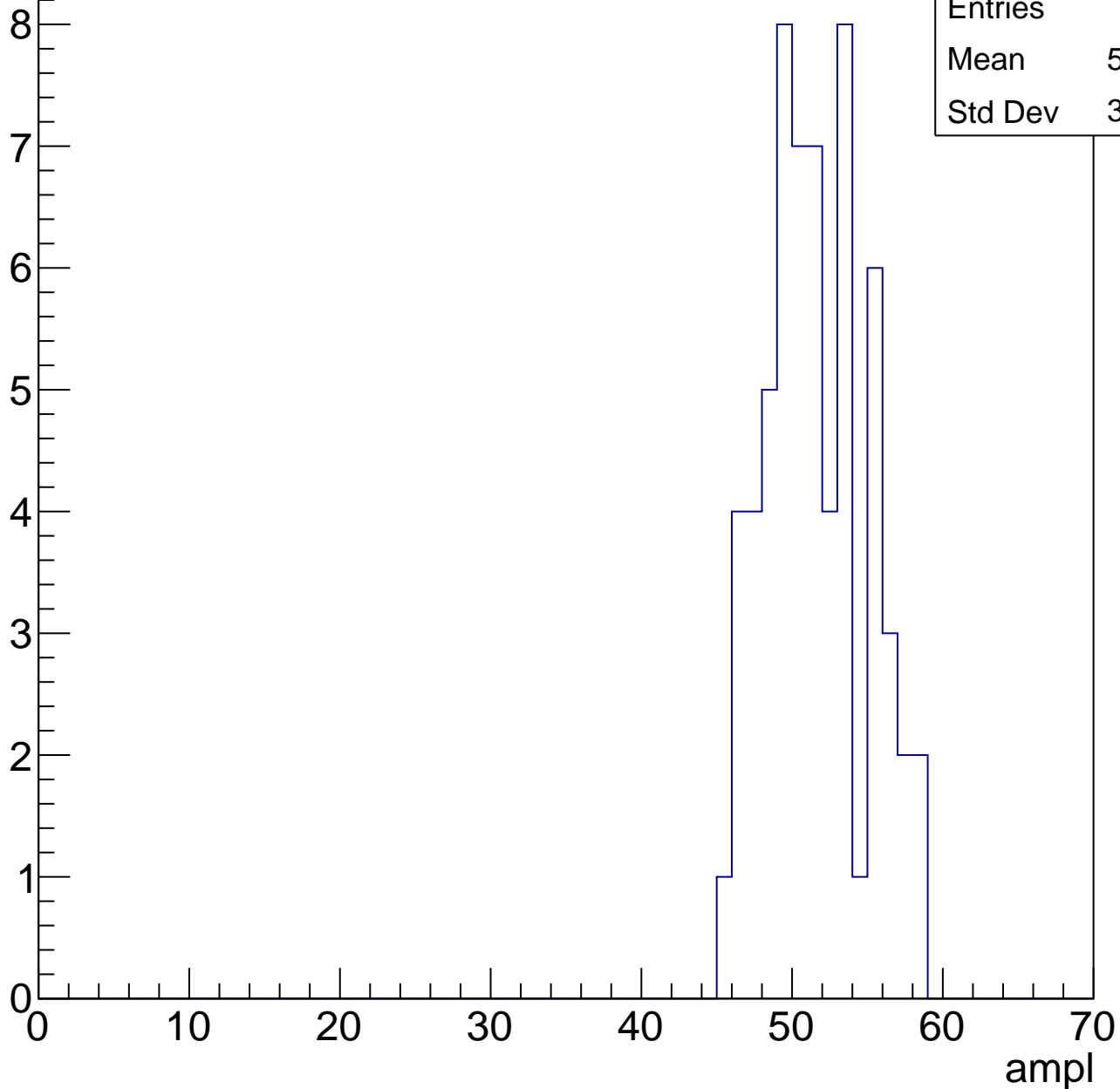
Entries	55
Mean	44.78
Std Dev	3.285



# B0L000S, U7-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

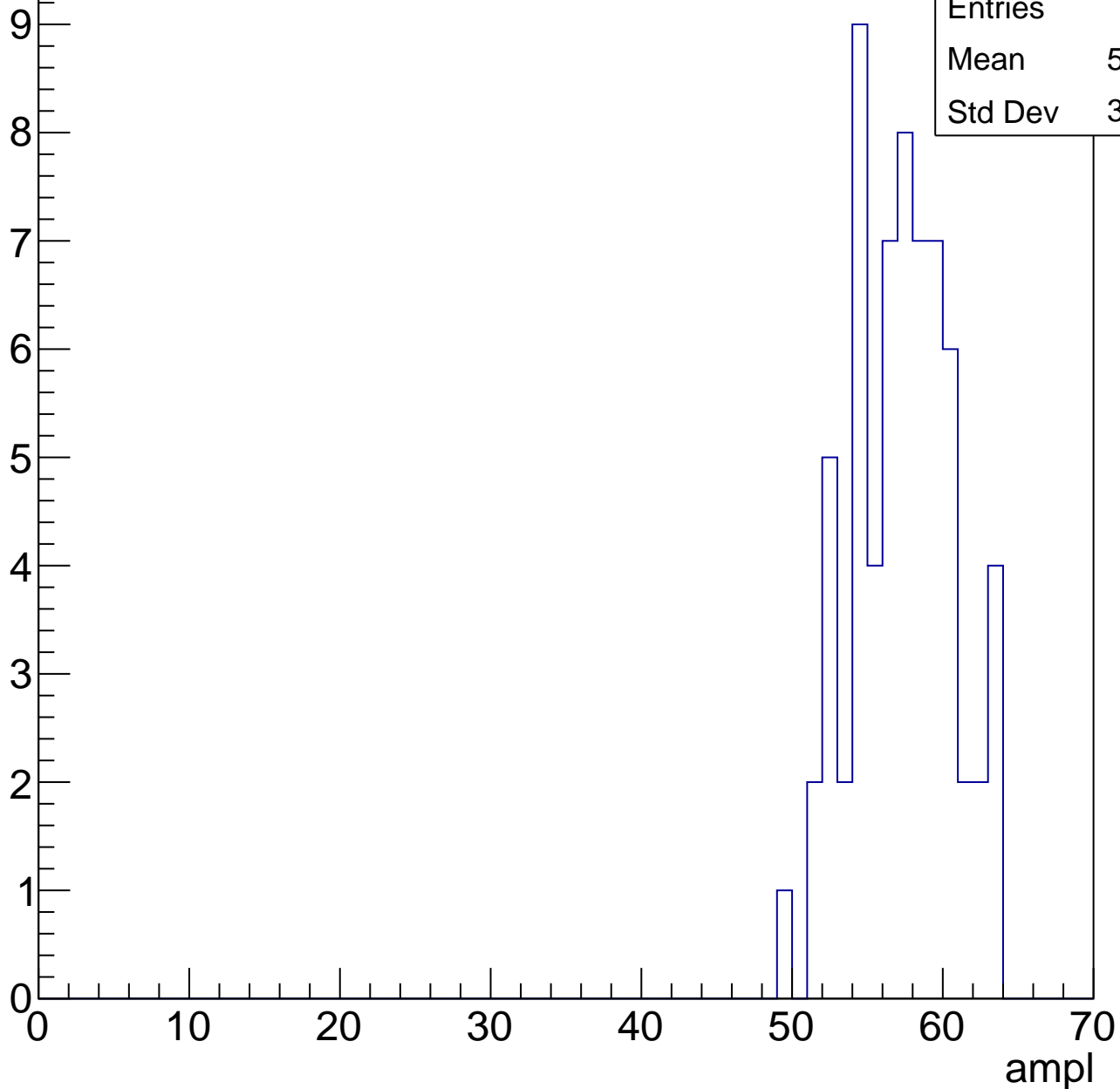
Entry



# B0L000S, U7-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



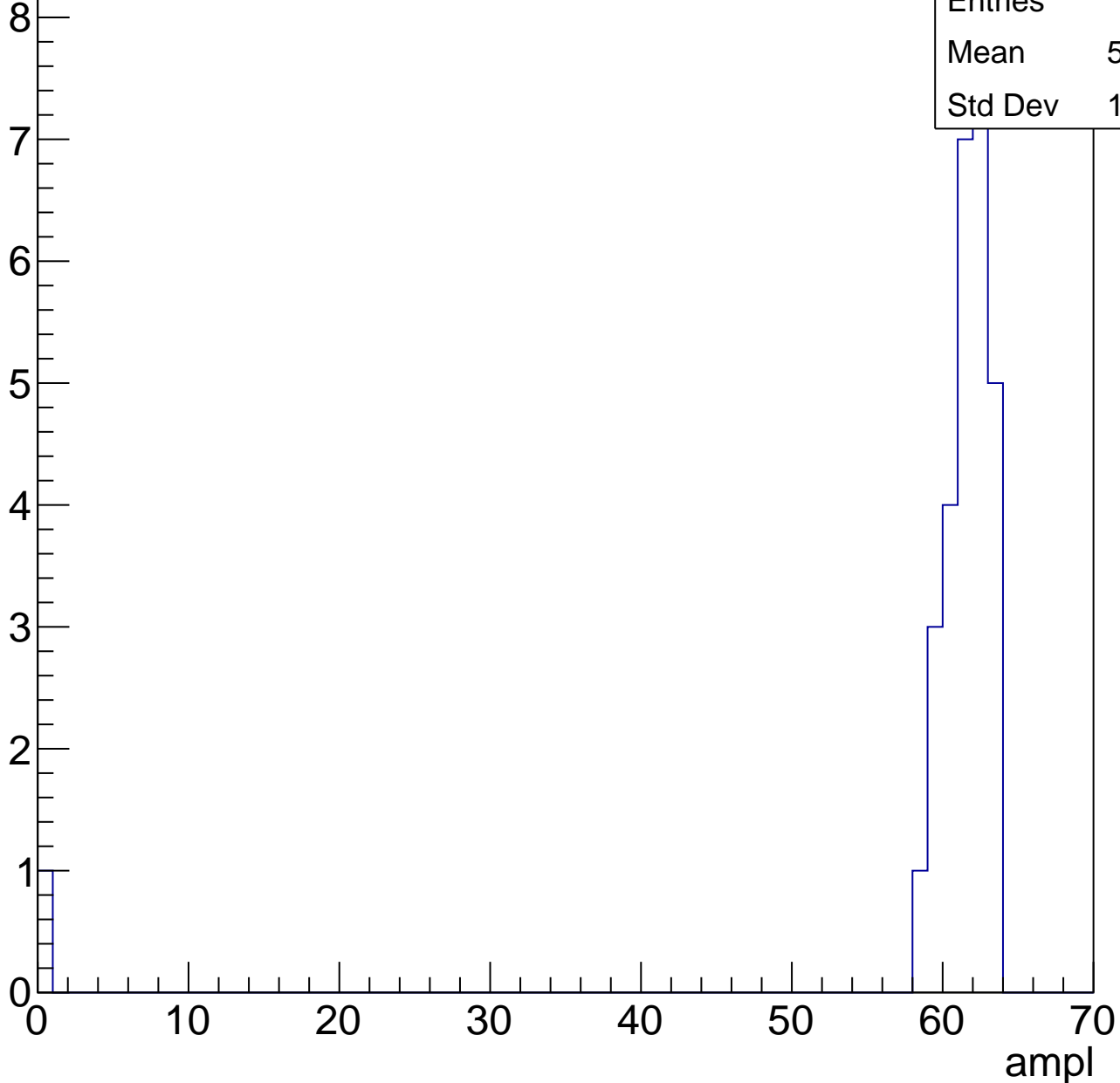
Entries	66
Mean	56.79
Std Dev	3.278

# B0L000S, U7-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	29
Mean	59.07
Std Dev	11.24



# B0L000S, U7-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L000S, U7-ch14, adc0

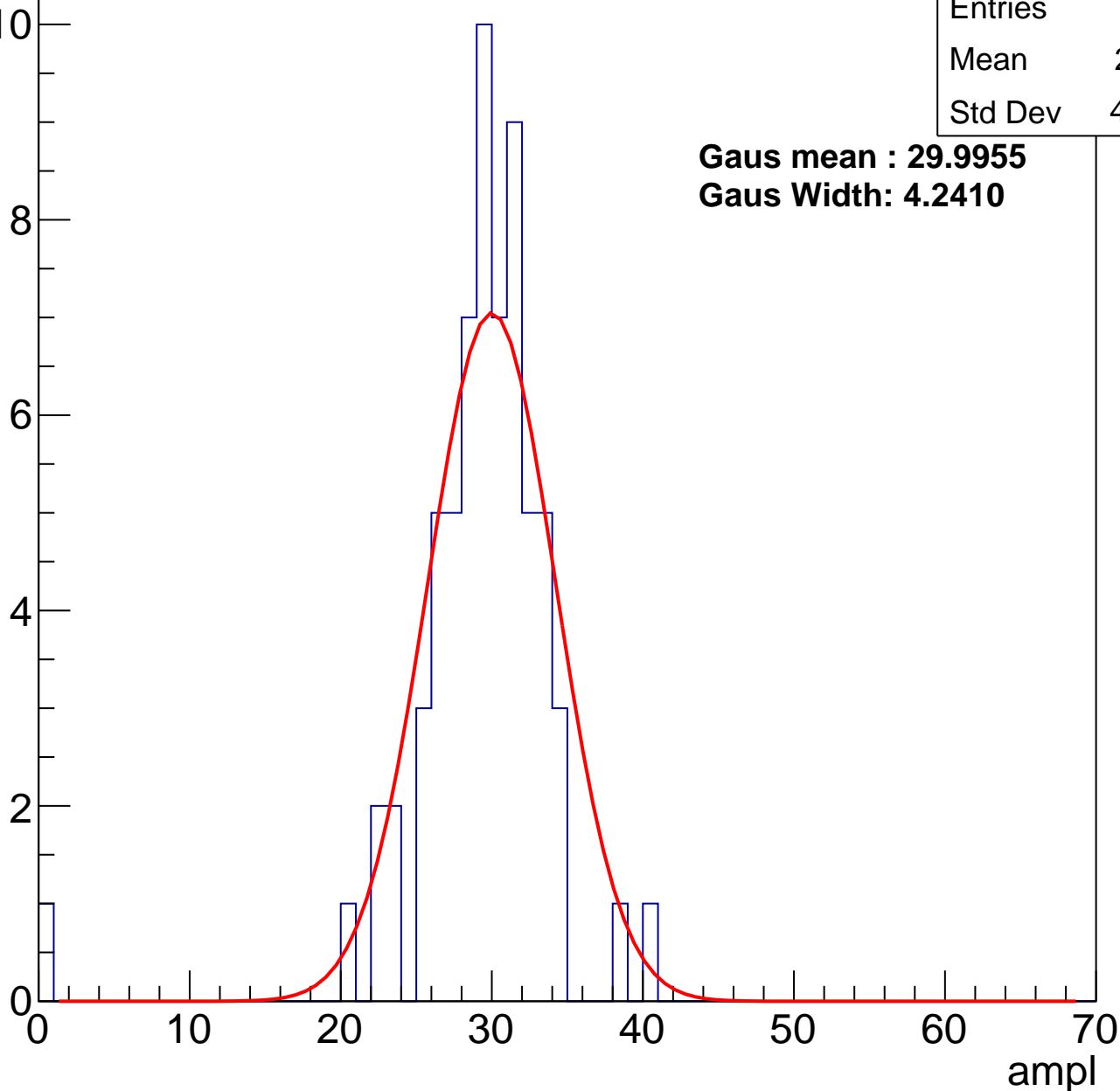
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	67
Mean	28.81
Std Dev	4.969

**Gaus mean : 29.9955**

**Gaus Width: 4.2410**



# B0L000S, U7-ch14, adc1

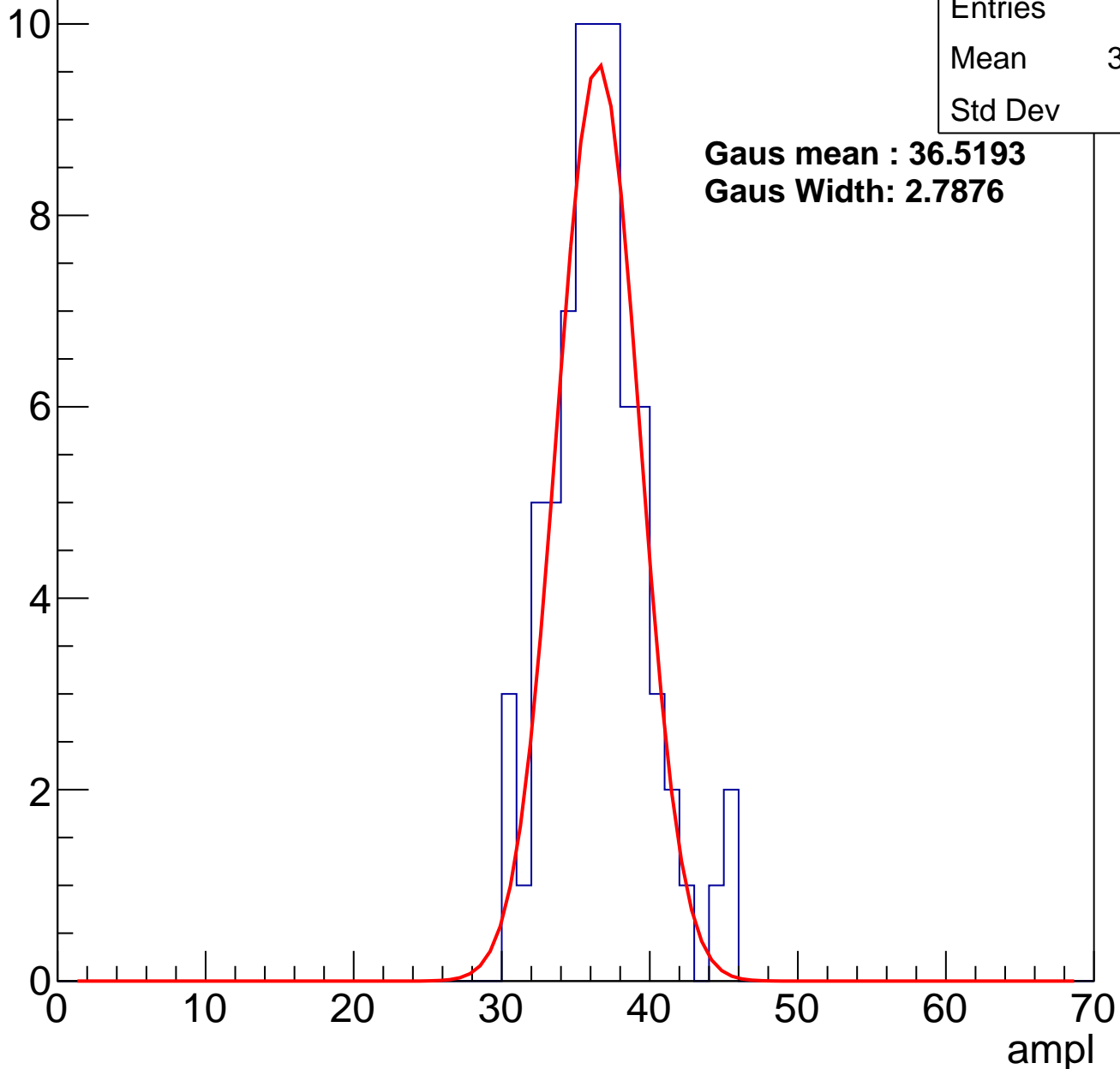
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	72
Mean	36.17
Std Dev	3.21

**Gaus mean : 36.5193**

**Gaus Width: 2.7876**

Entry



# B0L000S, U7-ch14, adc2

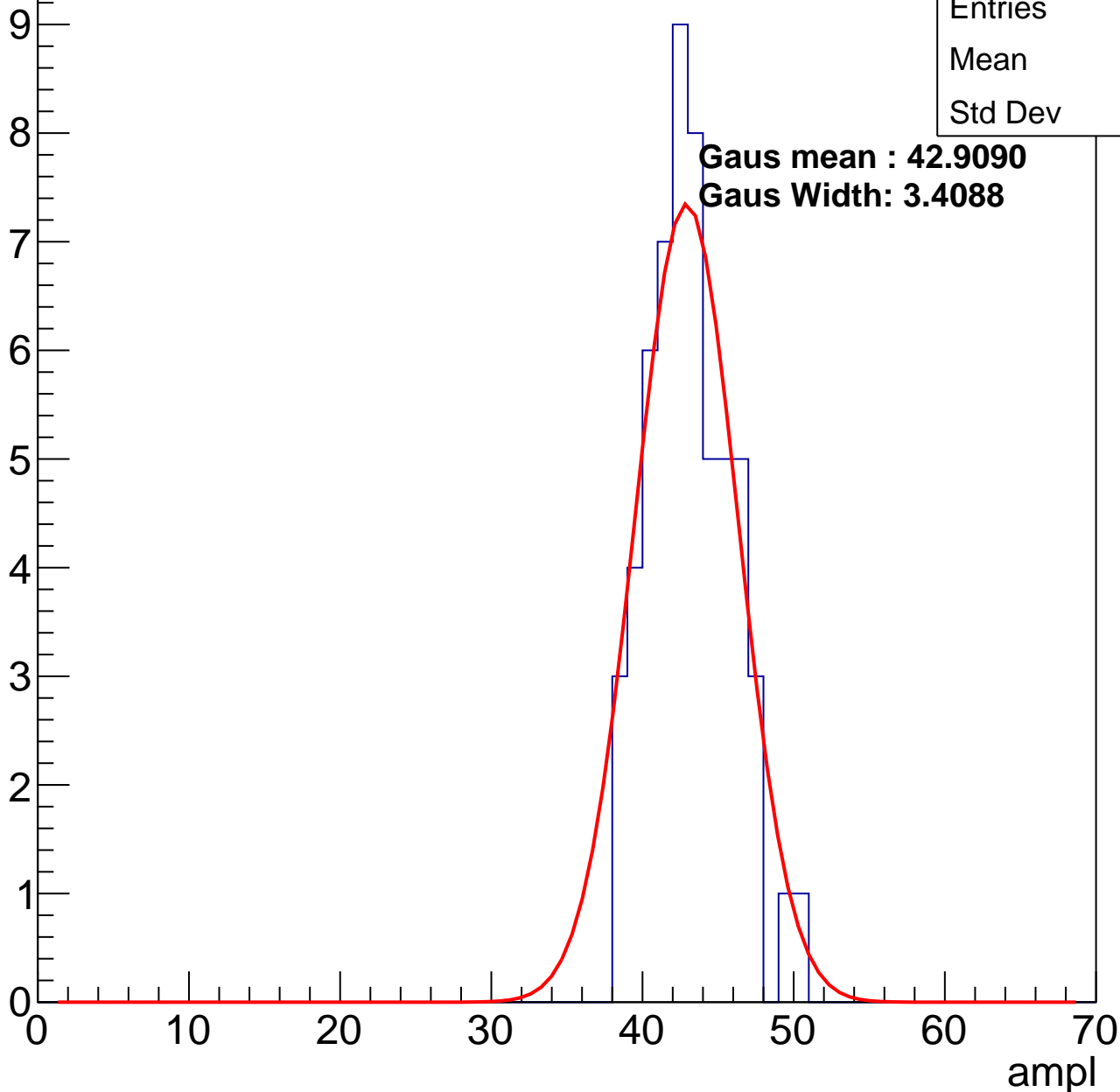
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	57
Mean	42.7
Std Dev	2.74

**Gaus mean : 42.9090**

**Gaus Width: 3.4088**



# B0L000S, U7-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	80
Mean	49.58
Std Dev	3.478

Entry

10

8

6

4

2

0

0

10

20

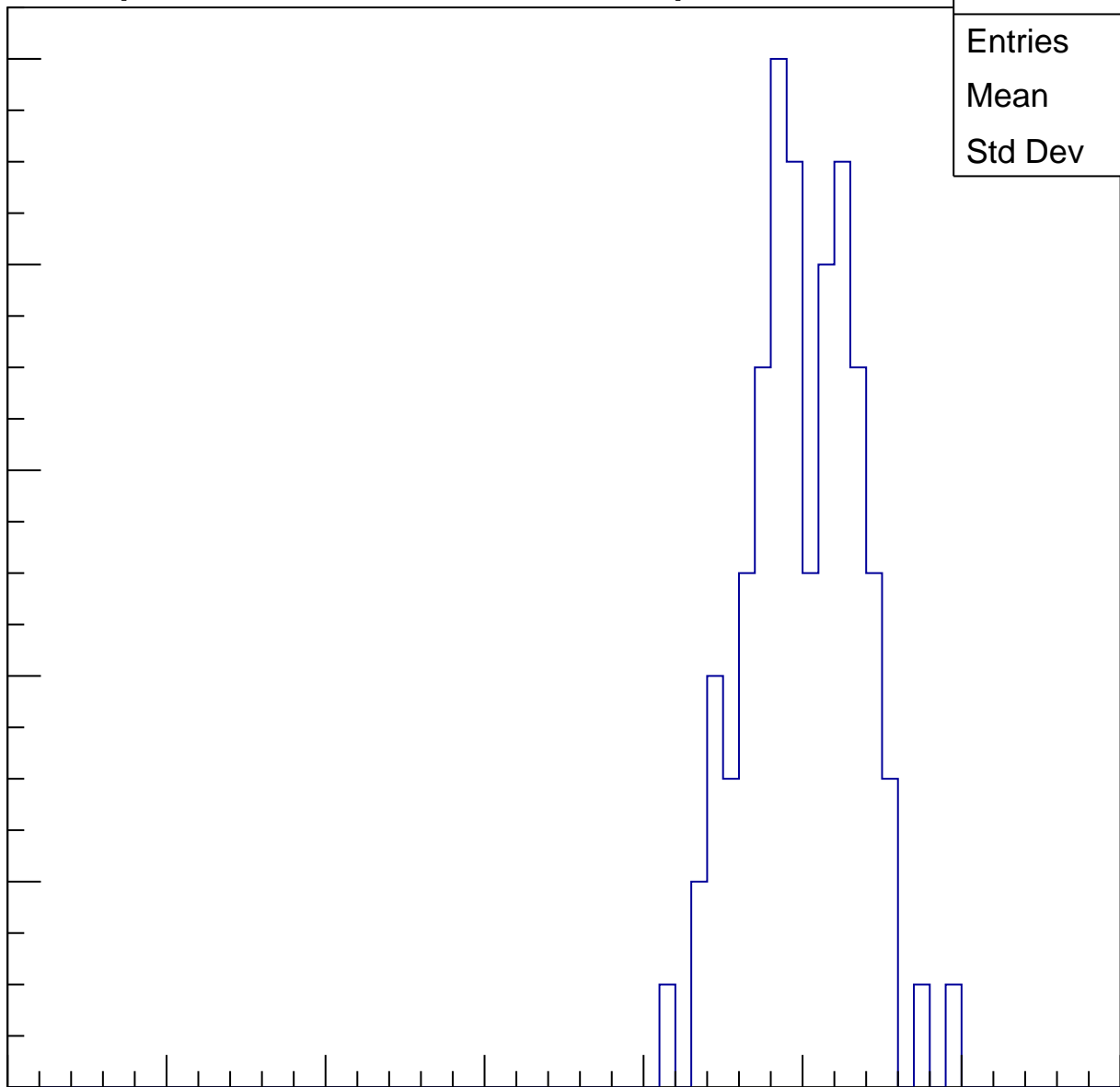
30

40

50

60

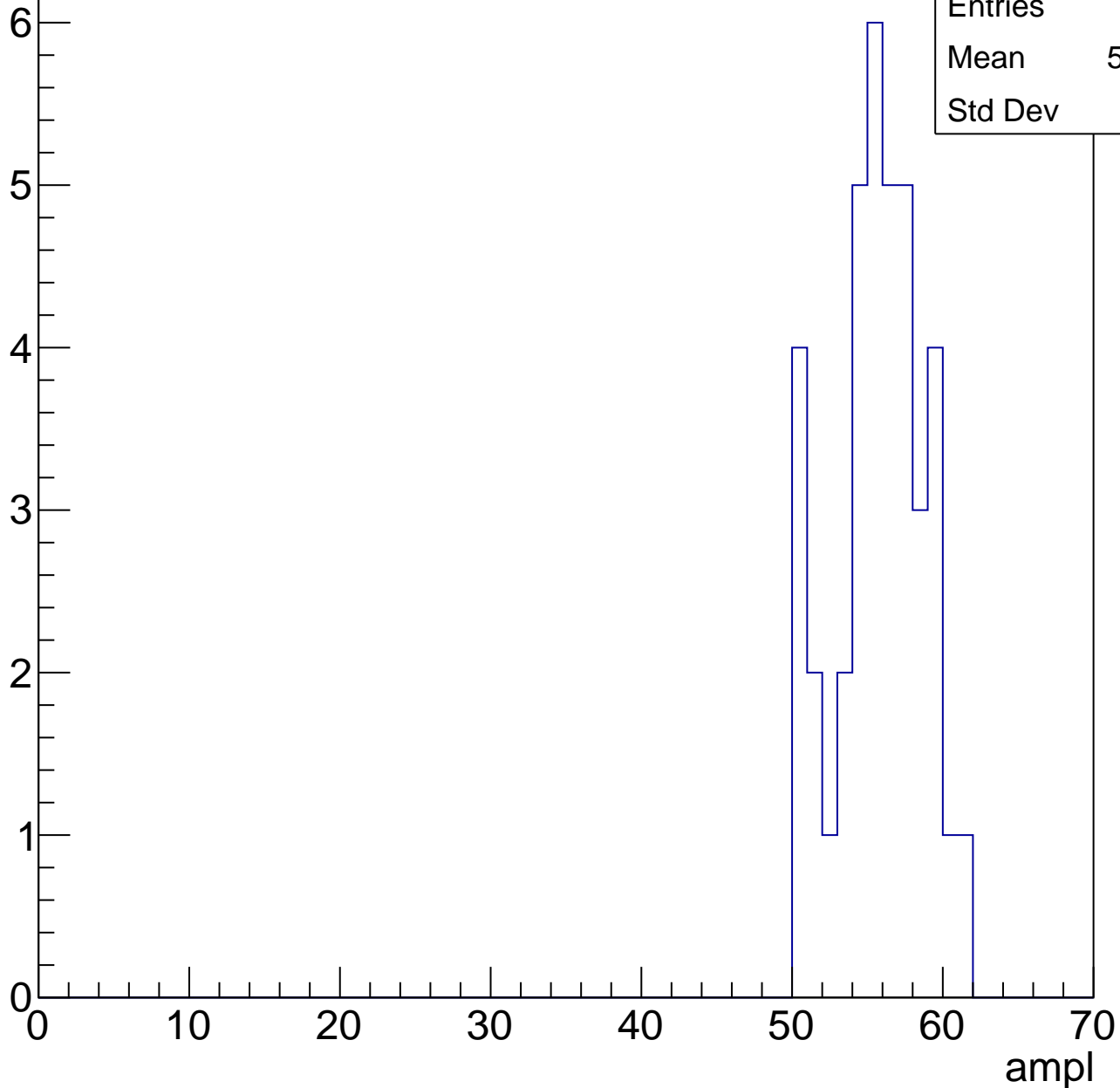
ampl



# B0L000S, U7-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



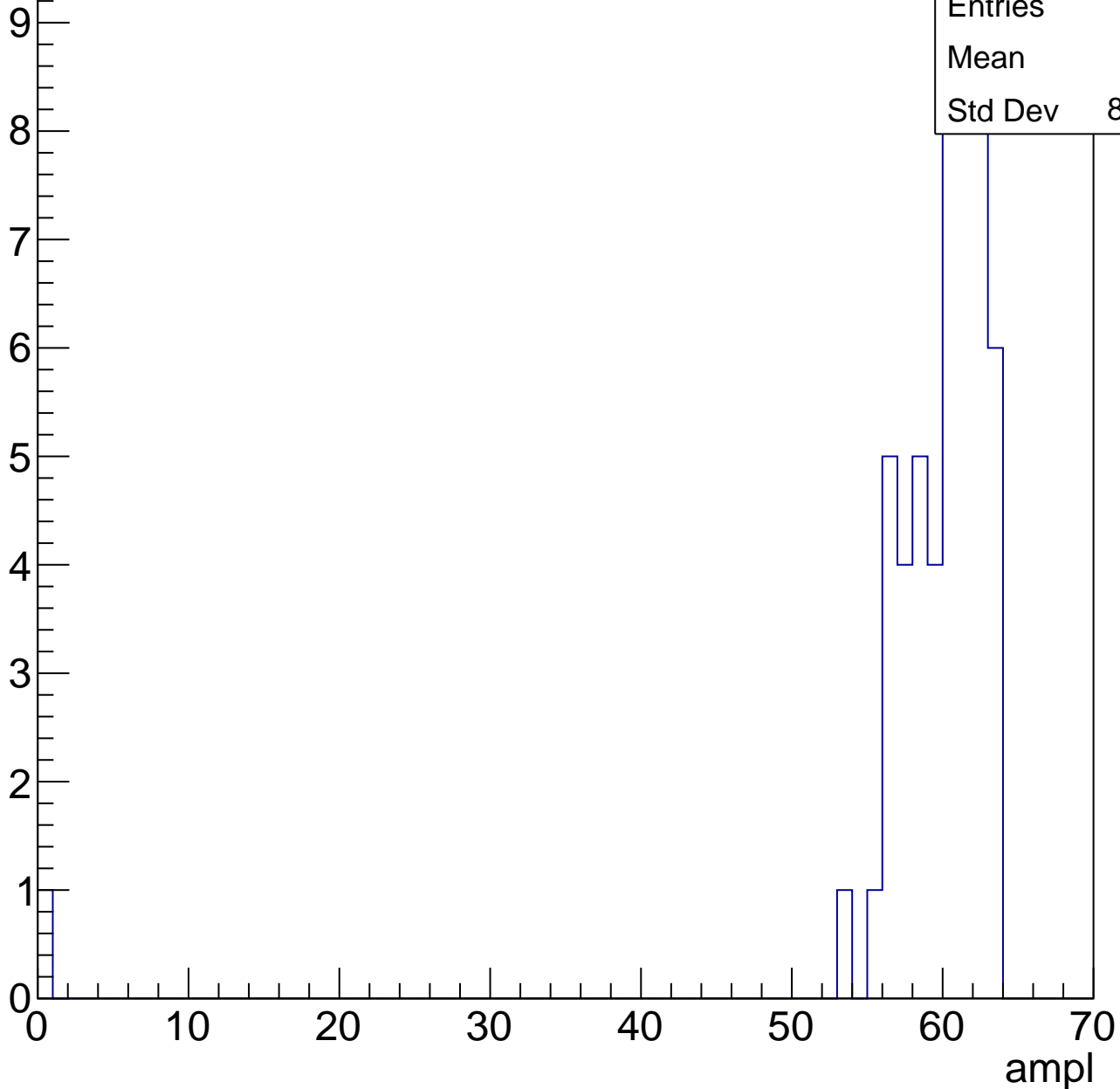
Entries	39
Mean	55.28
Std Dev	2.9

# B0L000S, U7-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

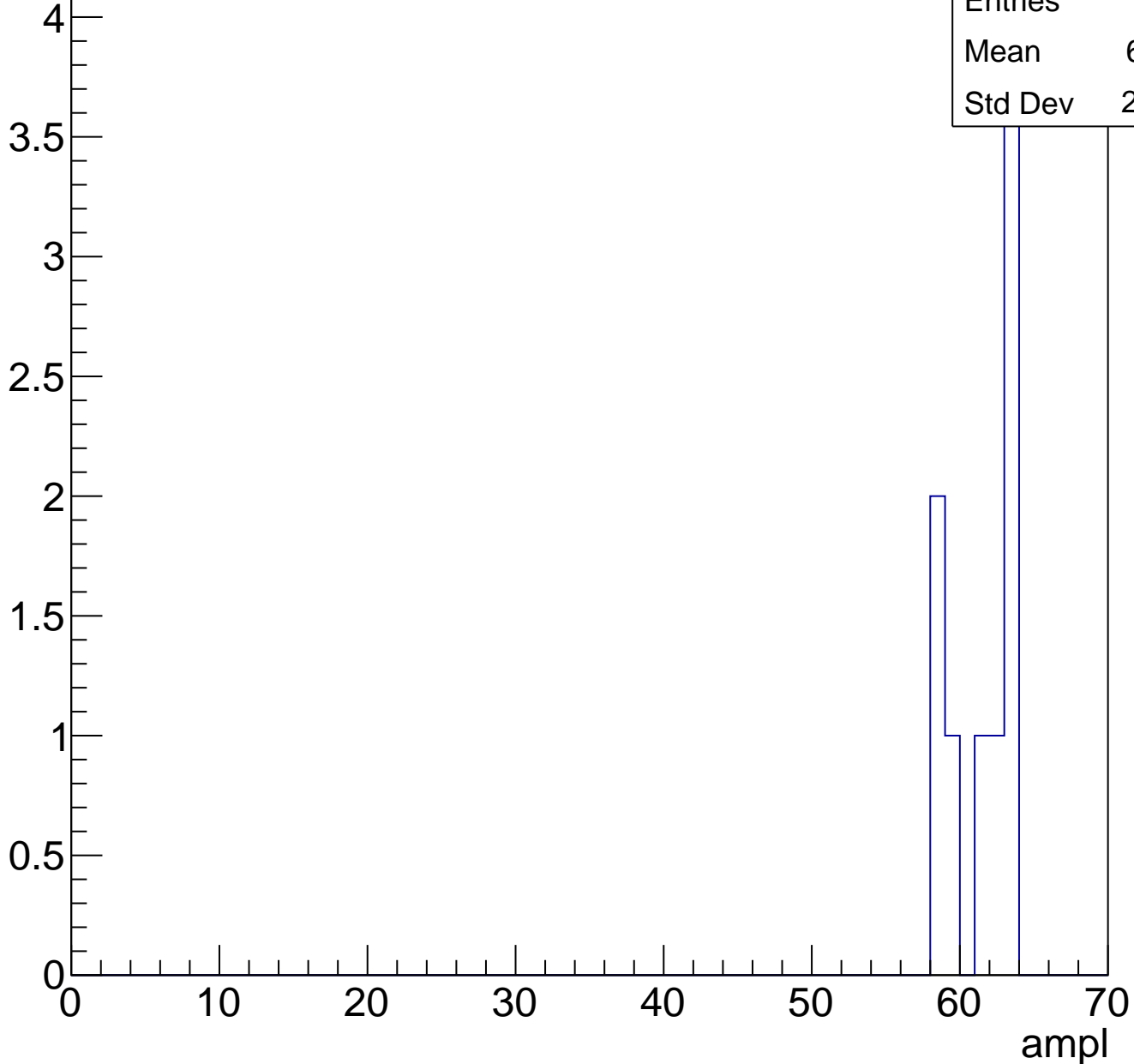
Entries	53
Mean	58.6
Std Dev	8.477



# B0L000S, U7-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L000S, U7-ch15, adc0

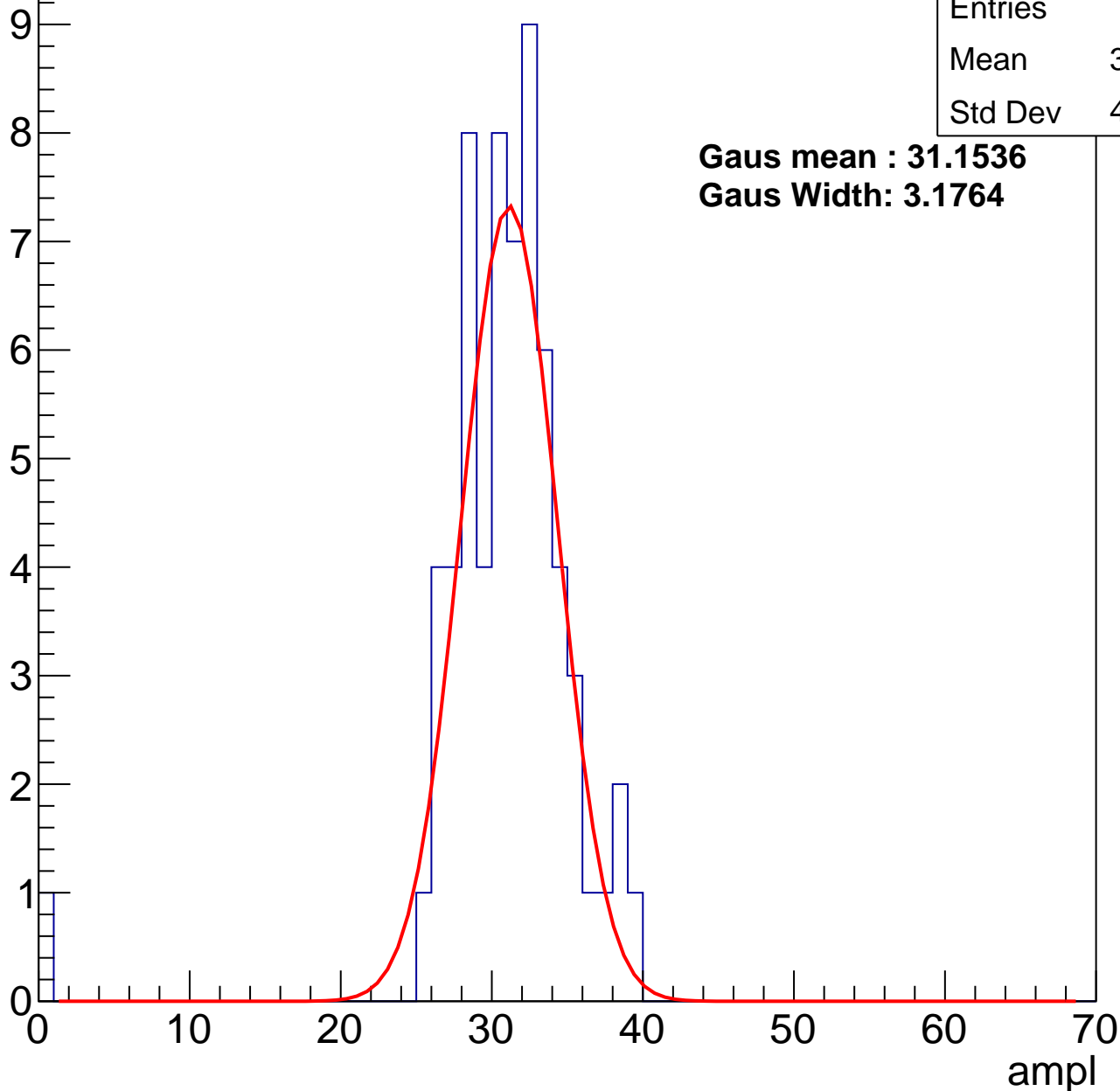
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	64
Mean	30.45
Std Dev	4.965

**Gaus mean : 31.1536**

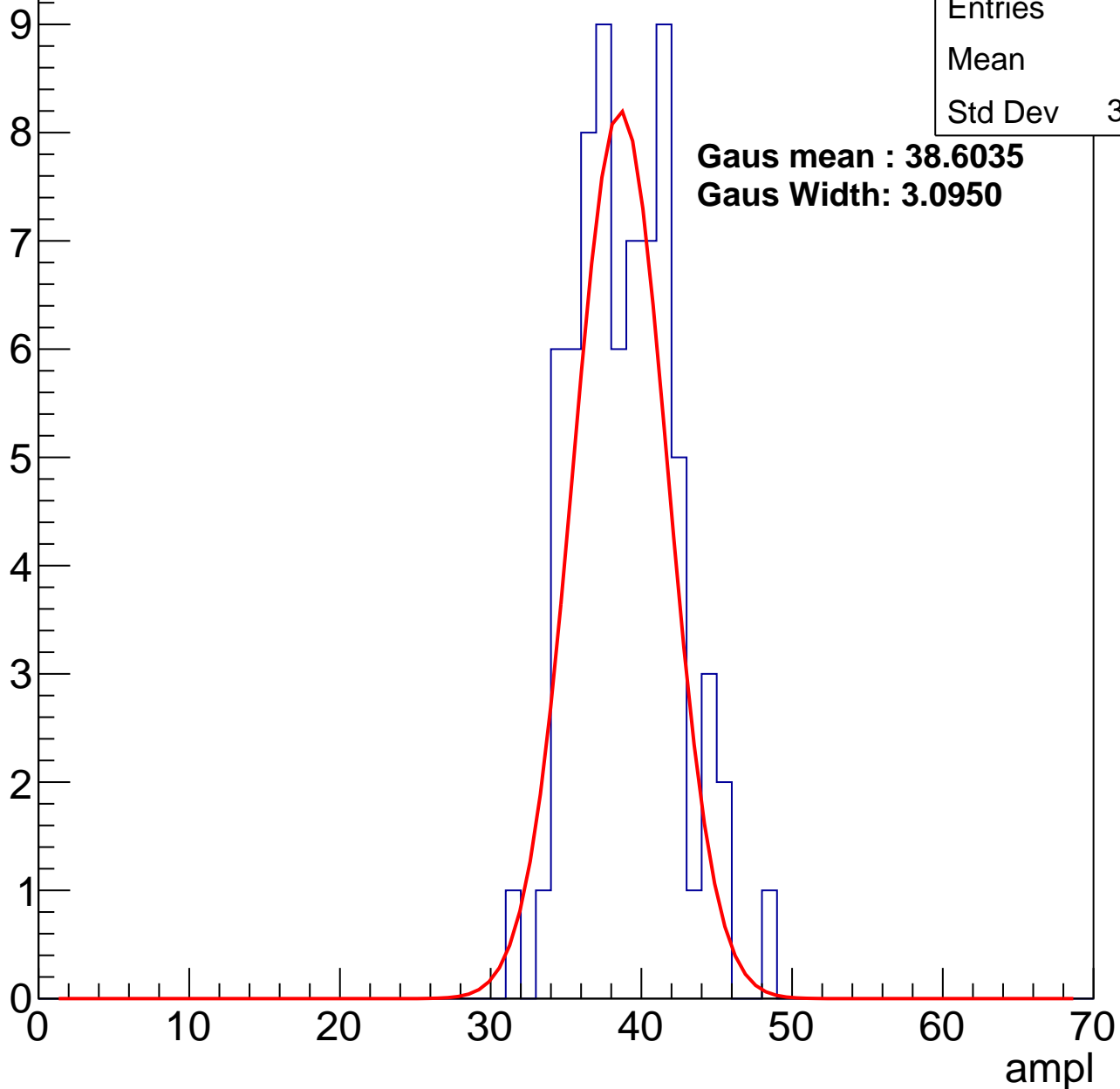
**Gaus Width: 3.1764**



# B0L000S, U7-ch15, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch15, adc2

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	71
Mean	44.56
Std Dev	3.707

**Gaus mean : 46.2487**

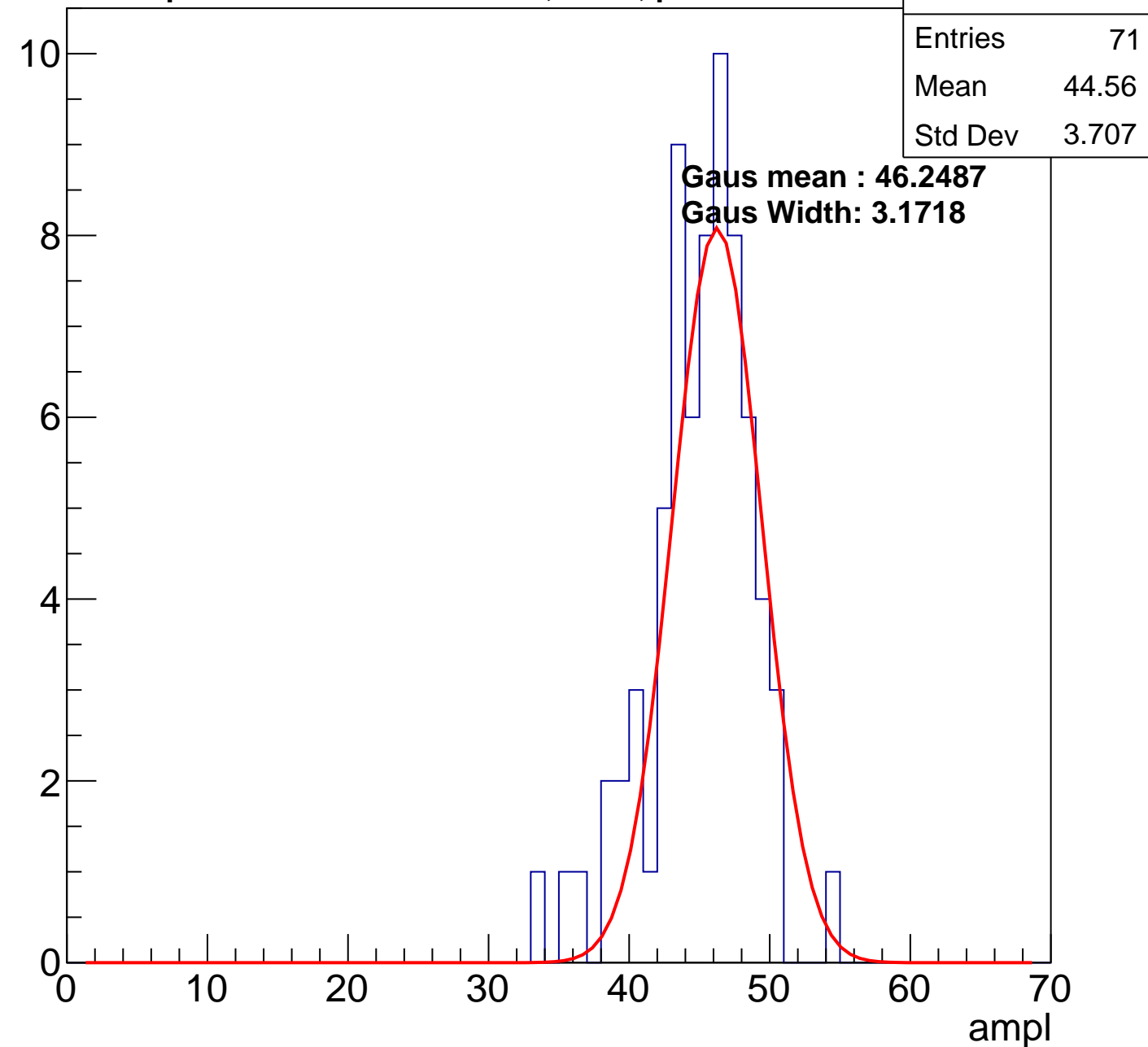
**Gaus Width: 3.1718**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L000S, U7-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

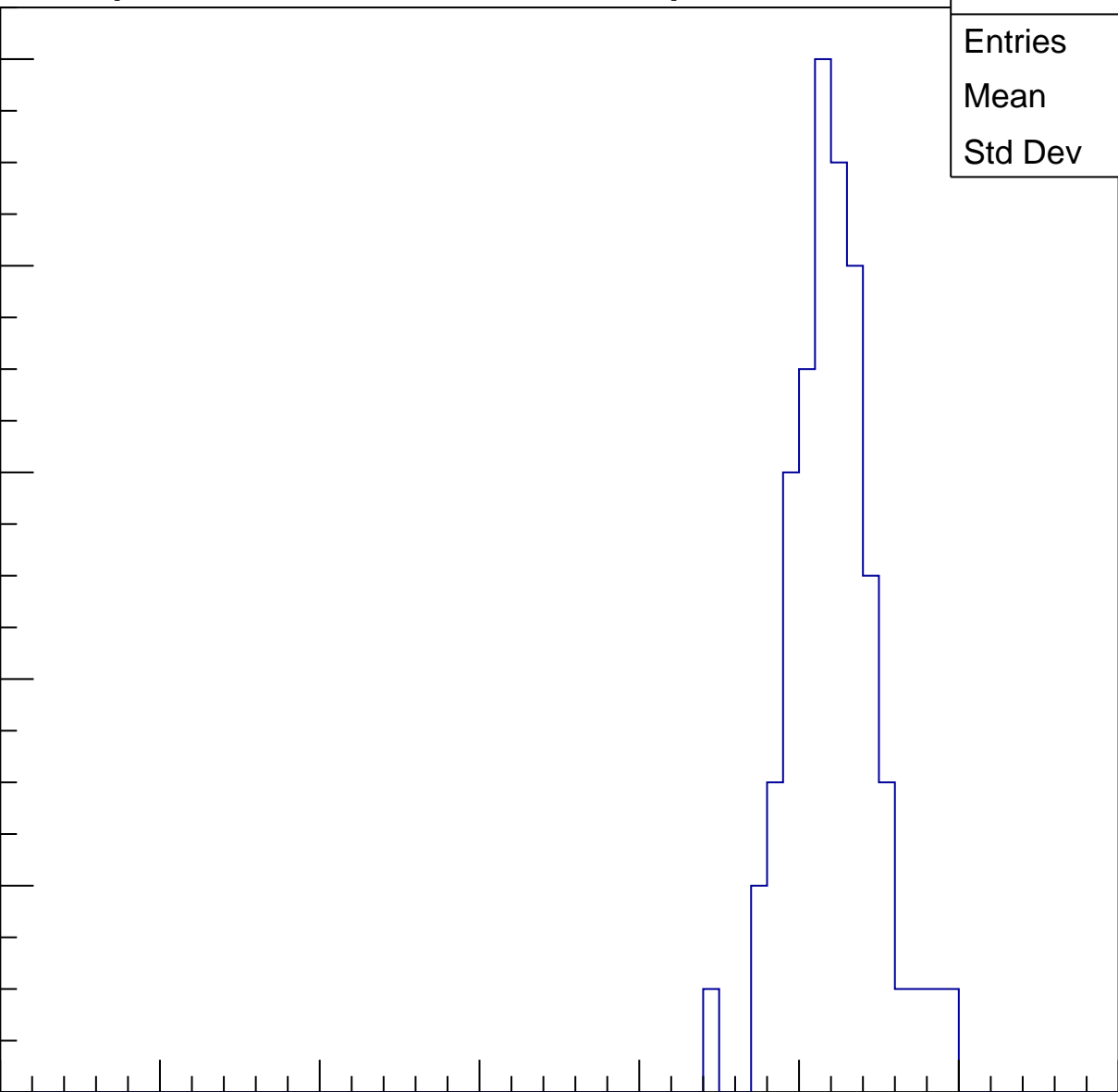
Entries	58
Mean	51.6
Std Dev	2.71

Entry

10  
8  
6  
4  
2  
0

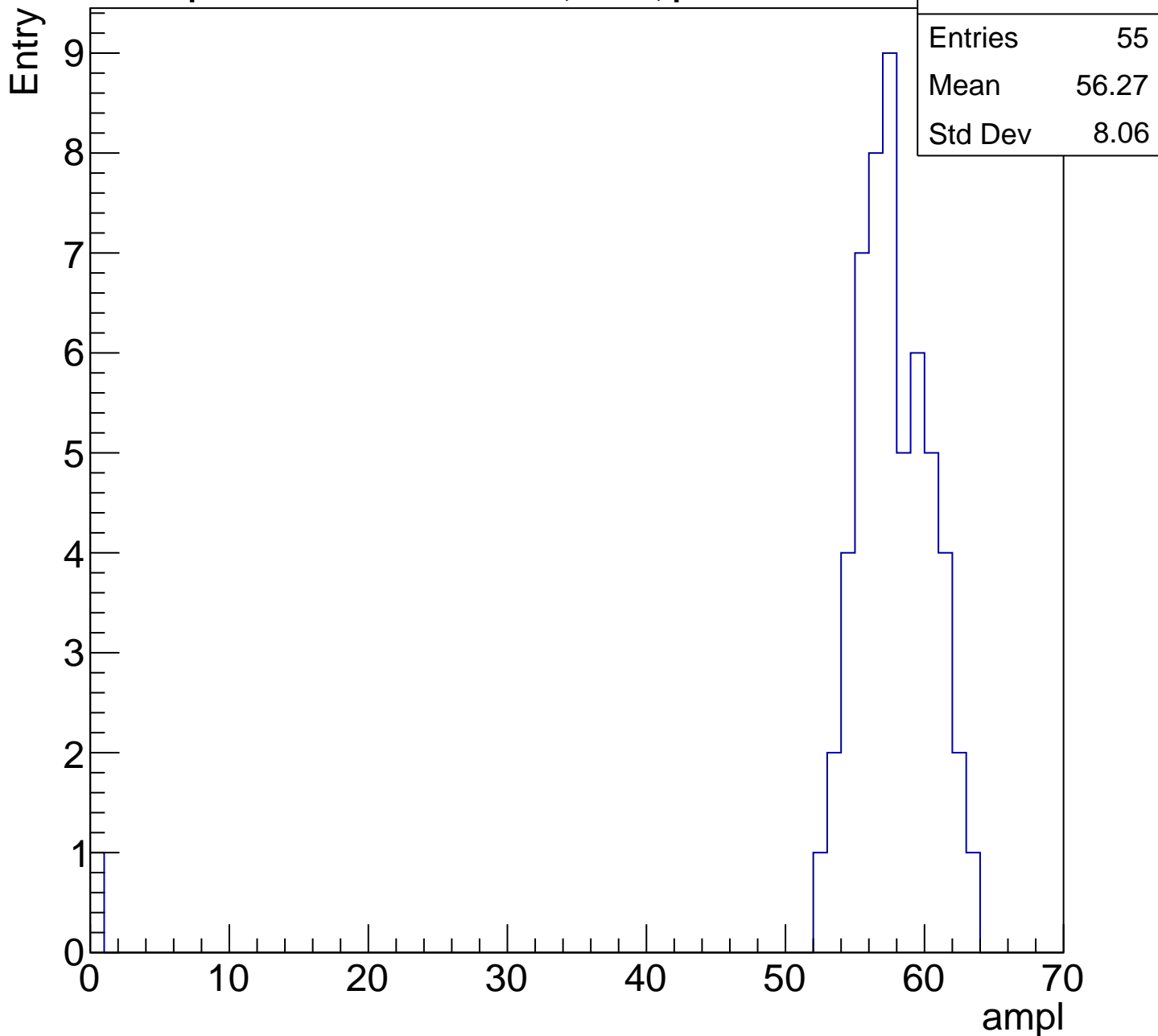
0 10 20 30 40 50 60 70

ampl



# B0L000S, U7-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

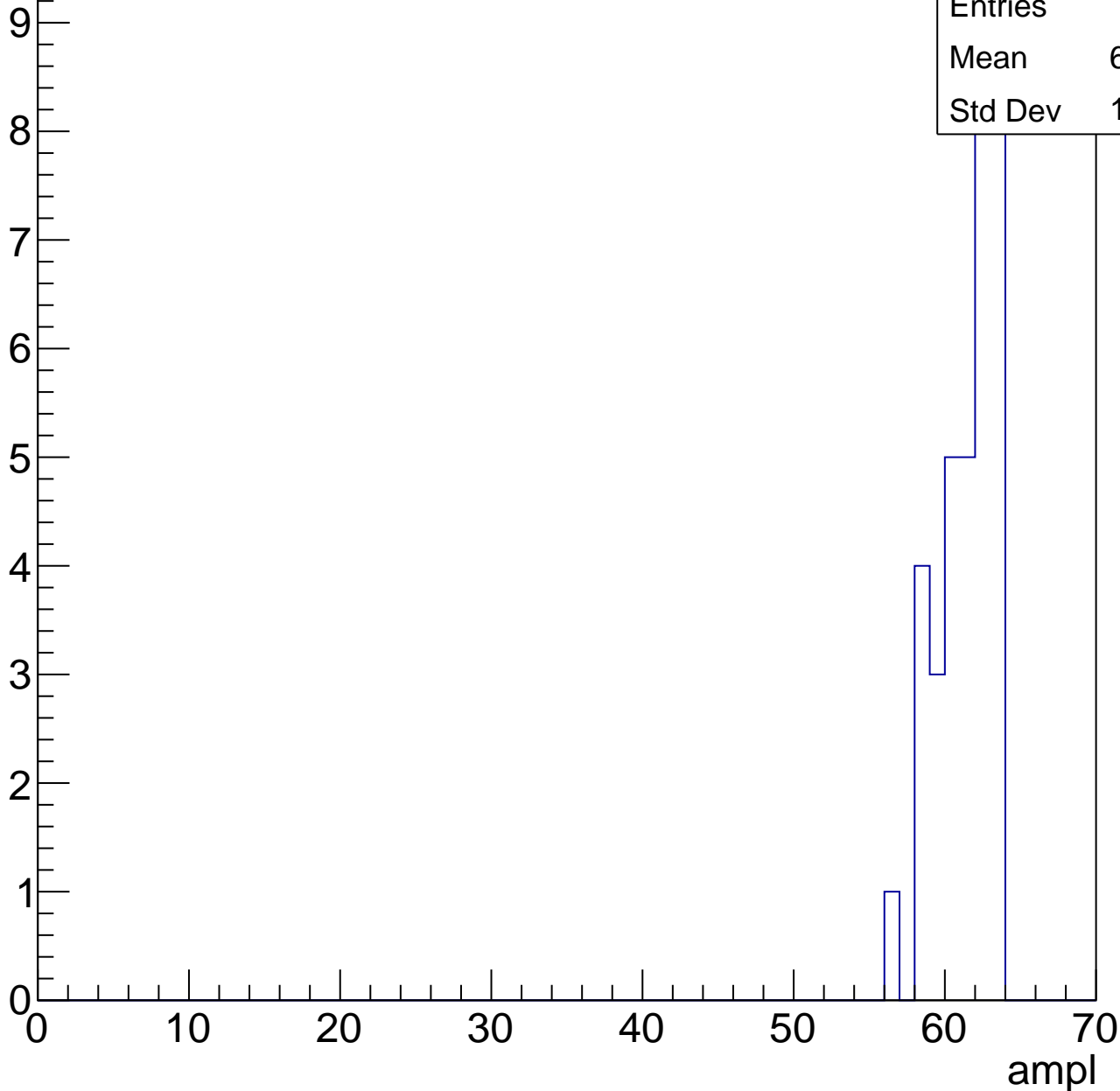


# B0L000S, U7-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	35
Mean	60.94
Std Dev	1.866



# B0L000S, U7-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch16, adc0

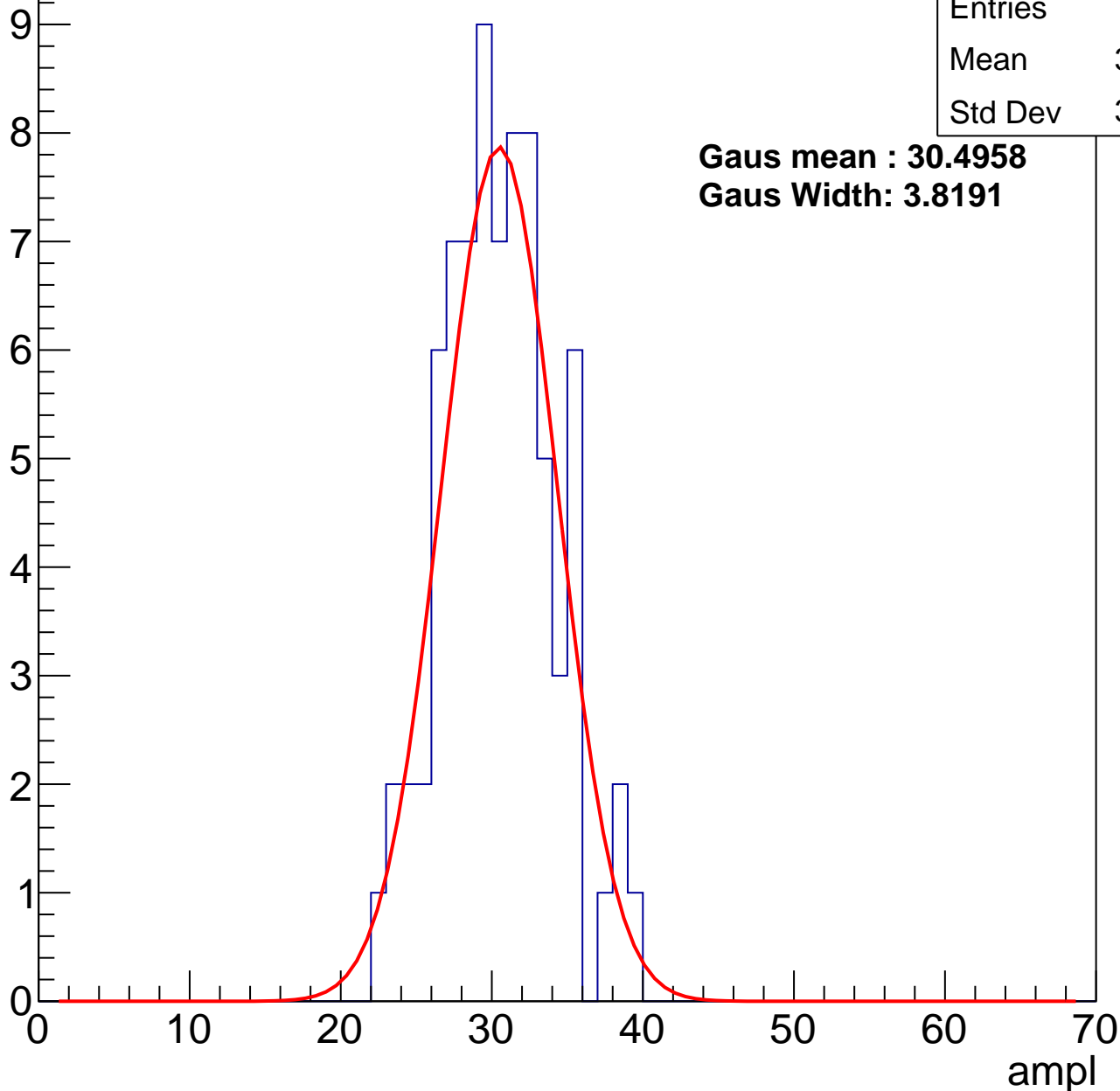
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	77
Mean	30.01
Std Dev	3.641

**Gaus mean : 30.4958**

**Gaus Width: 3.8191**



# B0L000S, U7-ch16, adc1

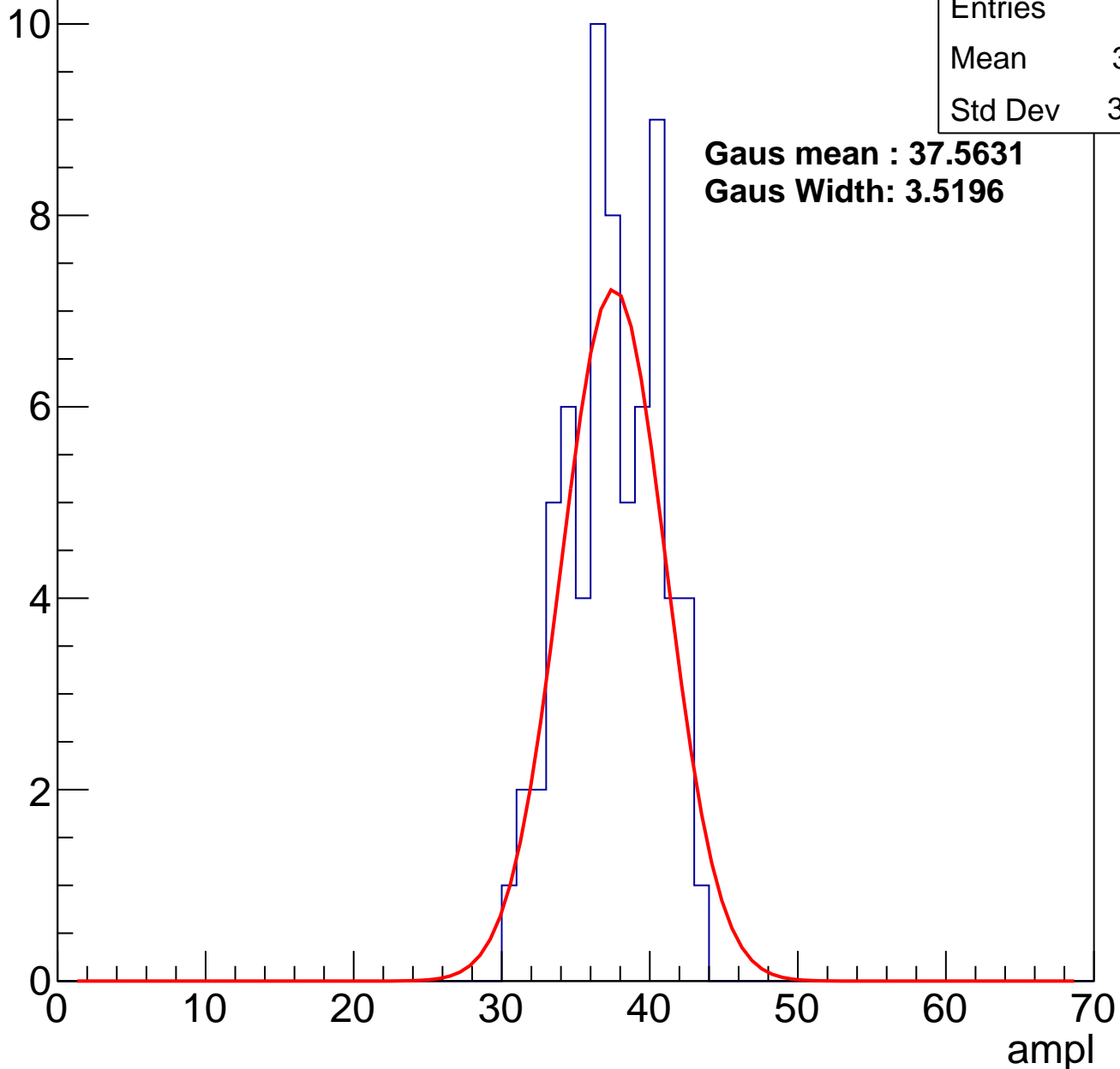
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	67
Mean	37.01
Std Dev	3.093

**Gaus mean : 37.5631**

**Gaus Width: 3.5196**

Entry



# B0L000S, U7-ch16, adc2

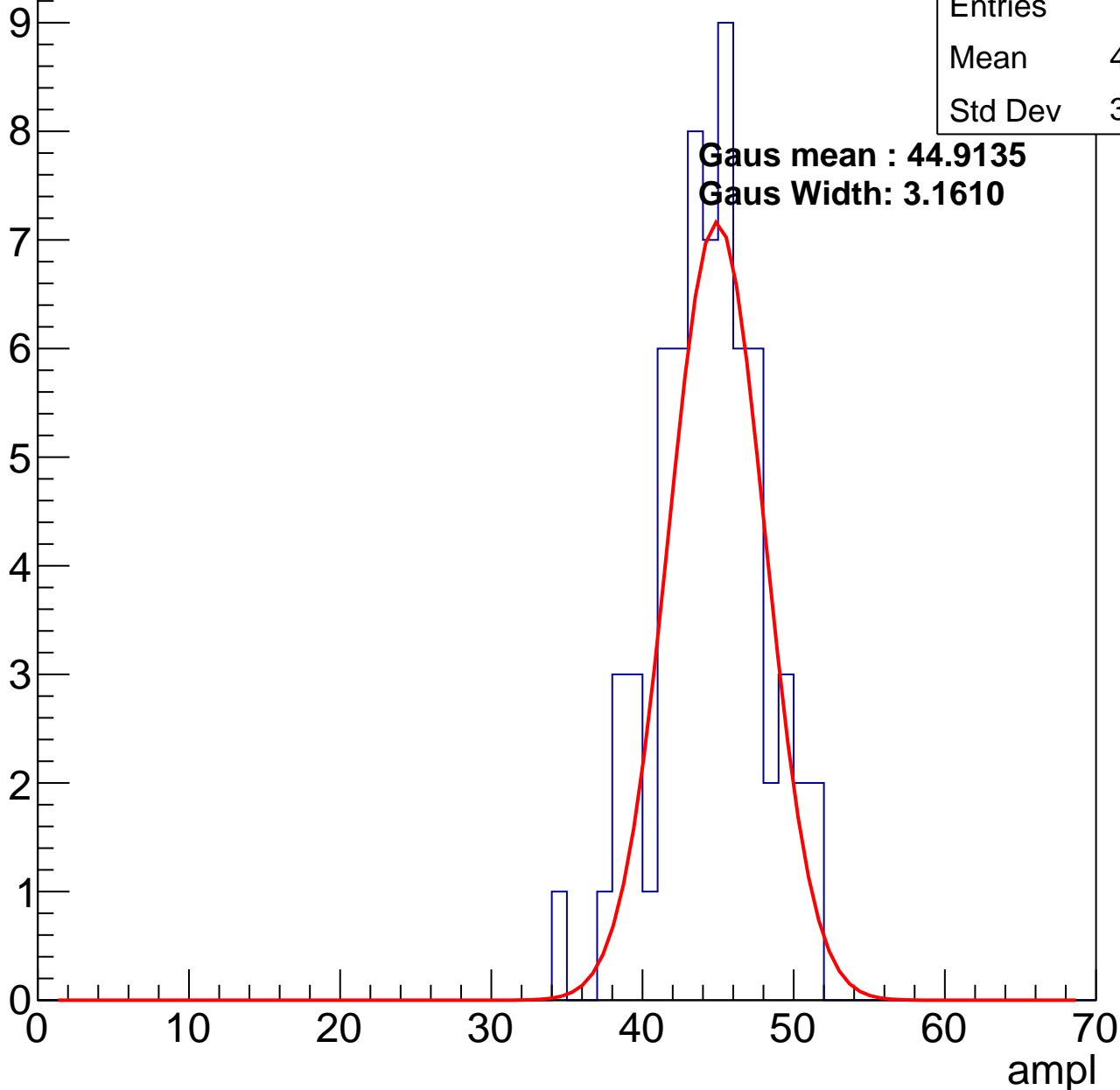
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	66
Mean	43.94
Std Dev	3.477

**Gaus mean : 44.9135**

**Gaus Width: 3.1610**

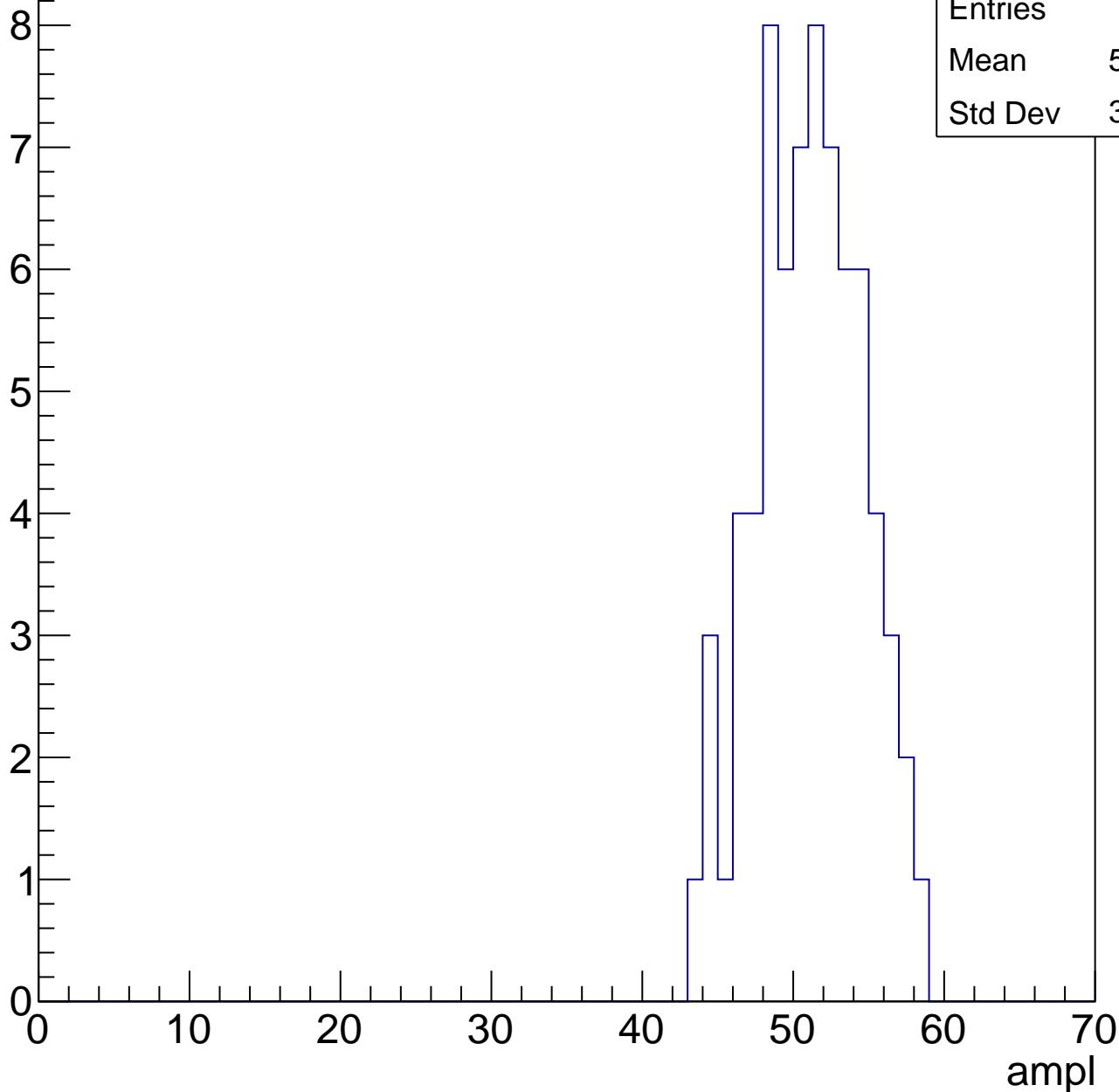


# B0L000S, U7-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	71
Mean	50.62
Std Dev	3.457

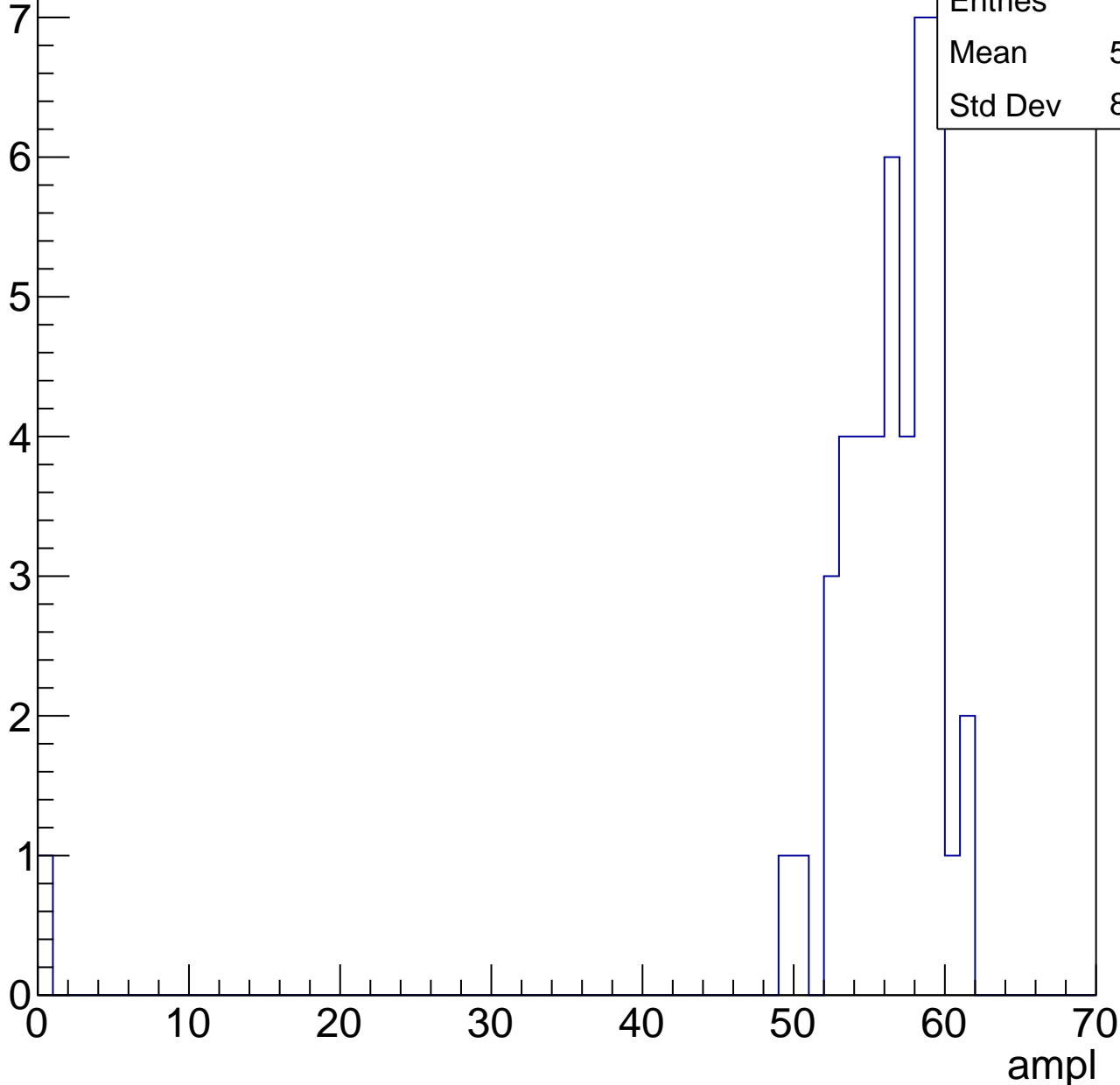


# B0L000S, U7-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	45
Mean	54.84
Std Dev	8.725

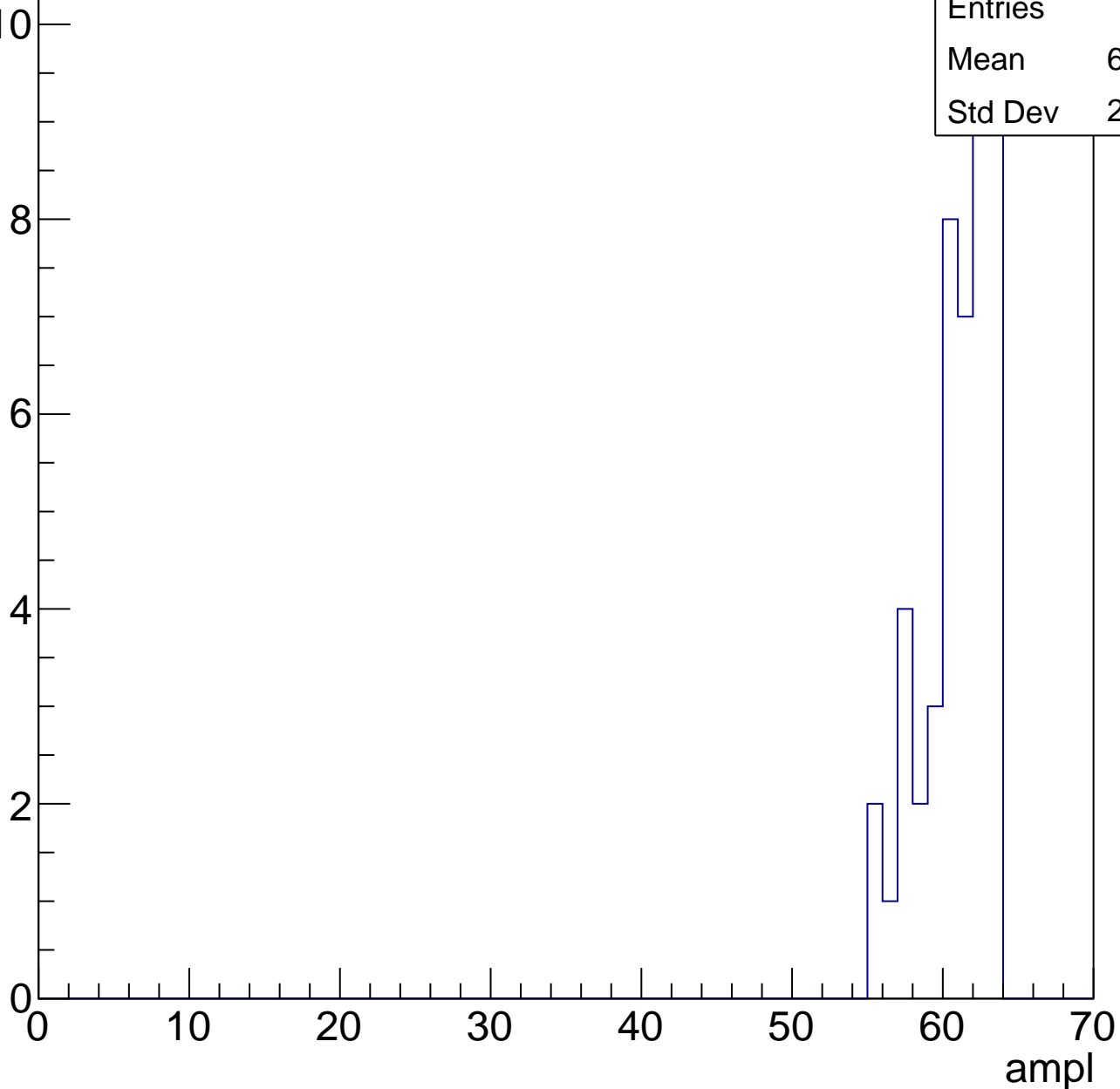


# B0L000S, U7-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	46
Mean	60.46
Std Dev	2.243



# B0L000S, U7-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L000S, U7-ch17, adc0

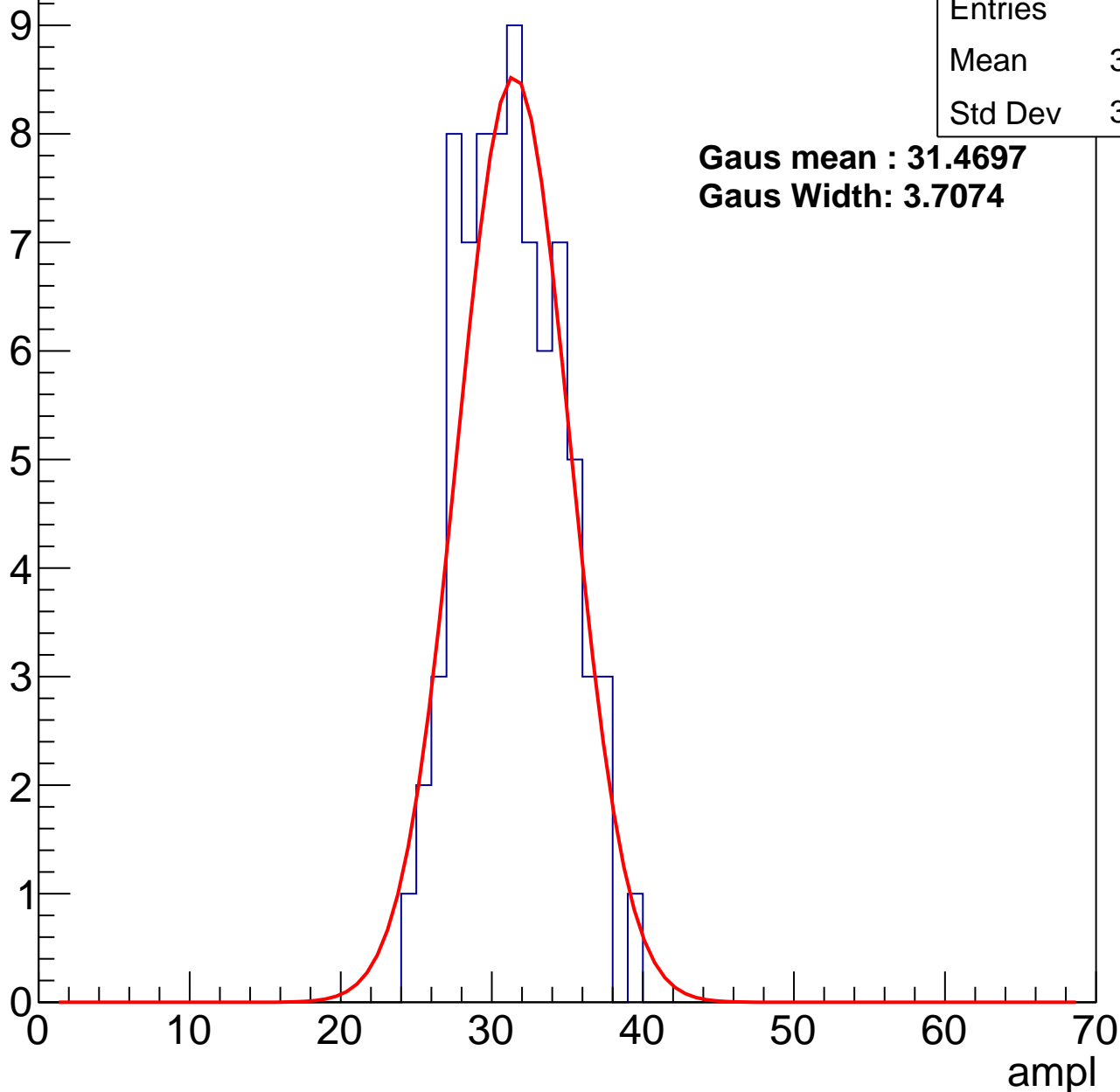
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	78
Mean	30.87
Std Dev	3.295

**Gaus mean : 31.4697**

**Gaus Width: 3.7074**



# B0L000S, U7-ch17, adc1

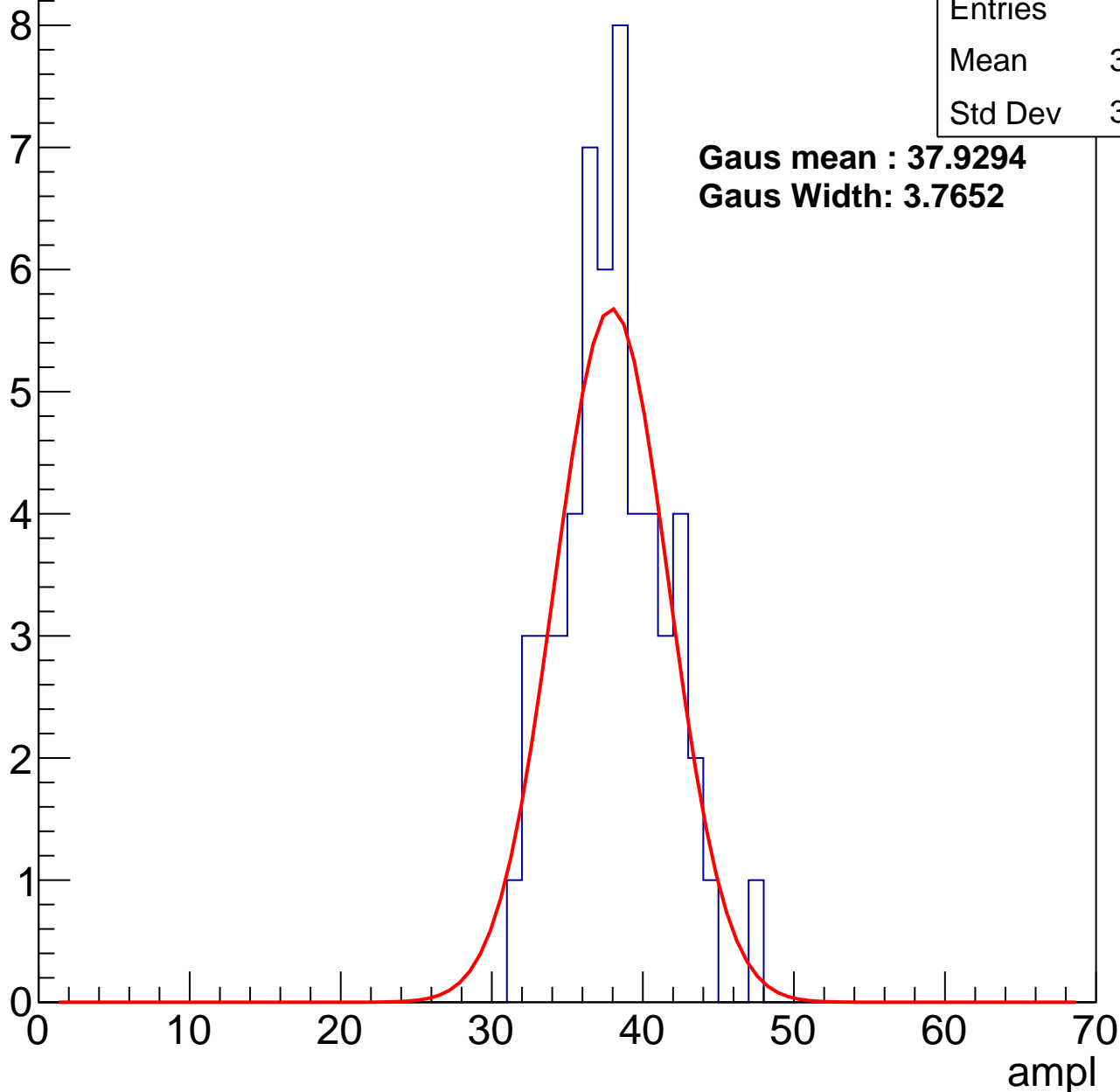
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	54
Mean	37.59
Std Dev	3.386

**Gaus mean : 37.9294**

**Gaus Width: 3.7652**



# B0L000S, U7-ch17, adc2

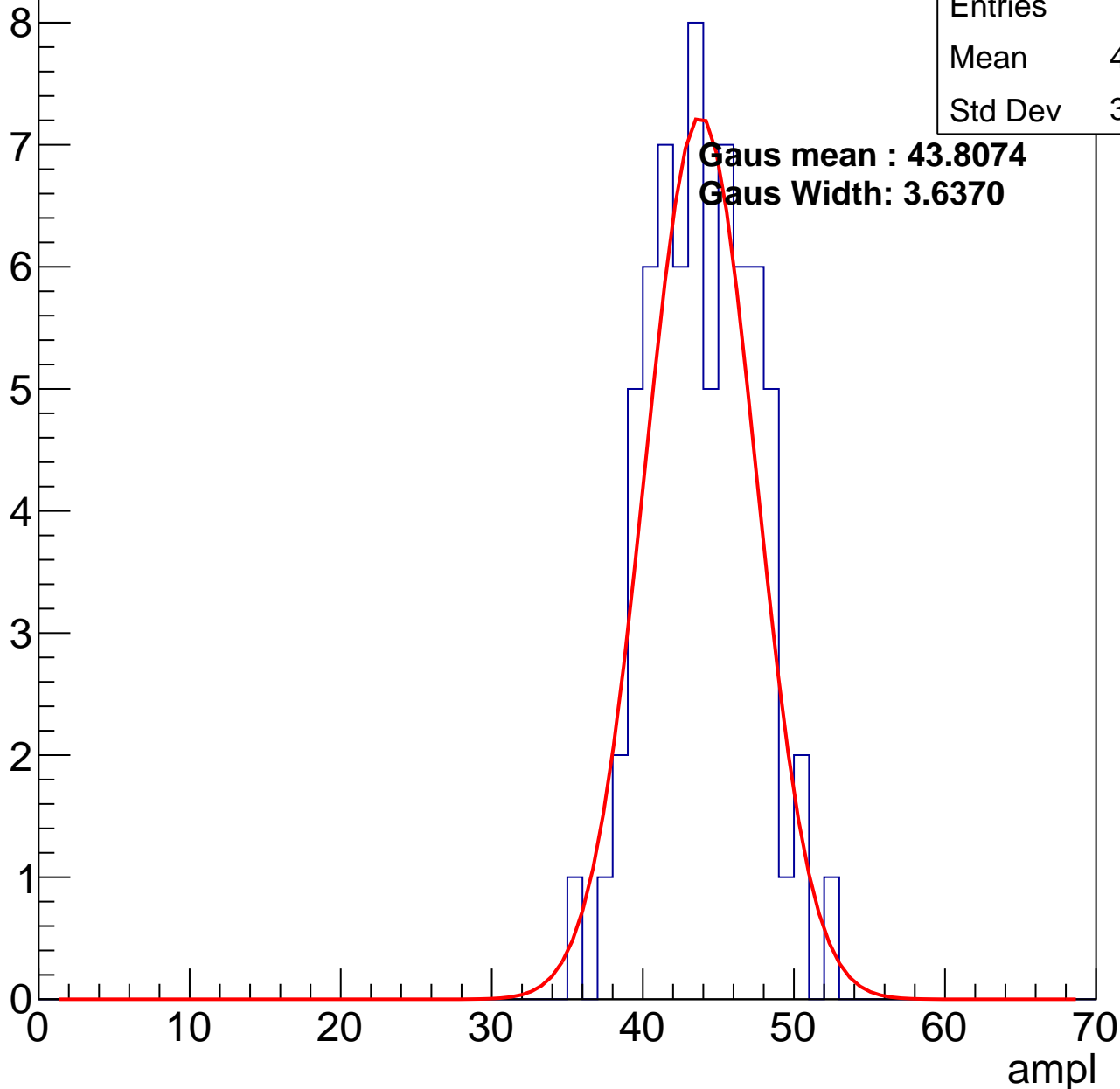
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	69
Mean	43.48
Std Dev	3.458

**Gaus mean : 43.8074**

**Gaus Width: 3.6370**

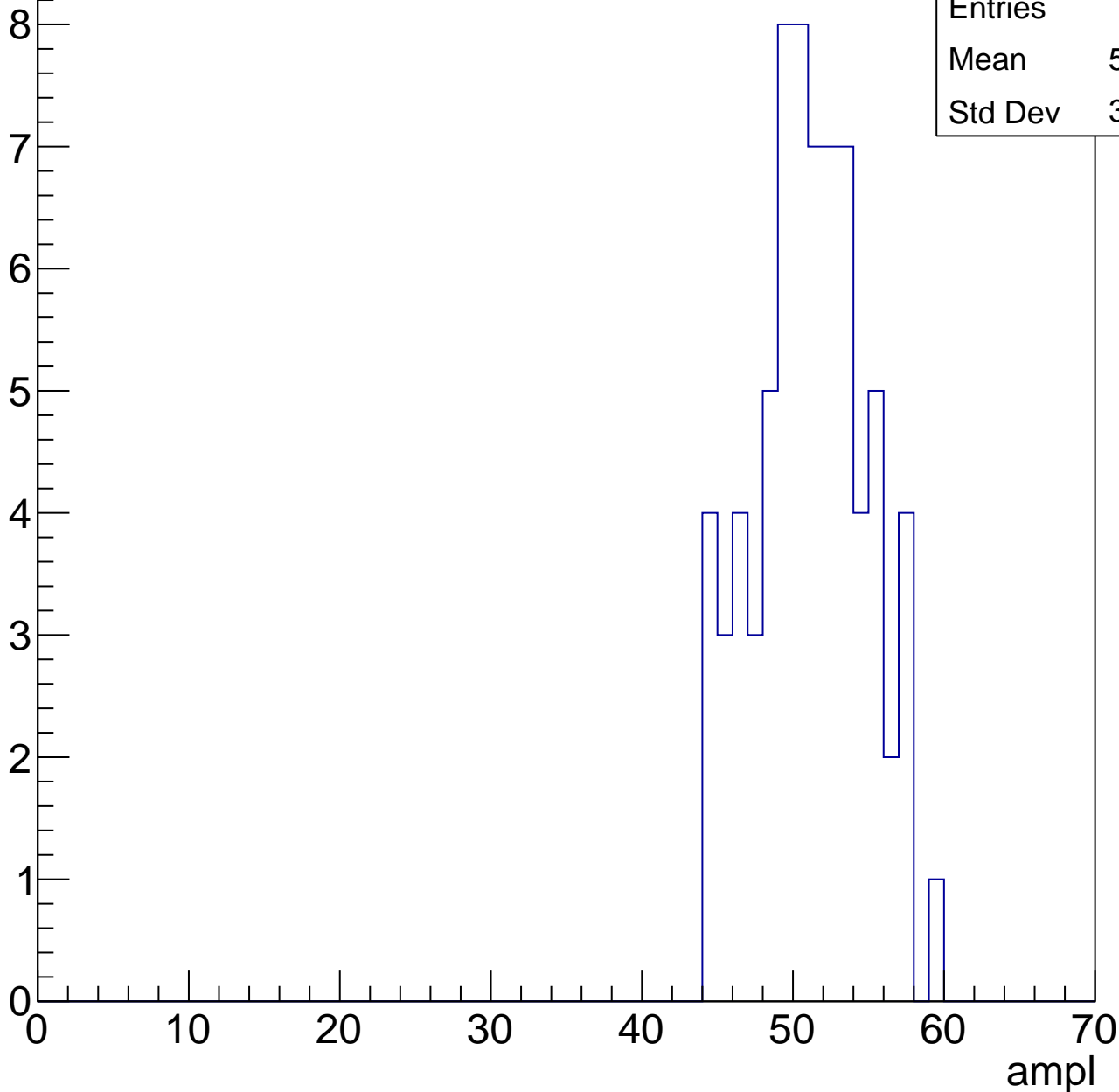


# B0L000S, U7-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	72
Mean	50.69
Std Dev	3.612

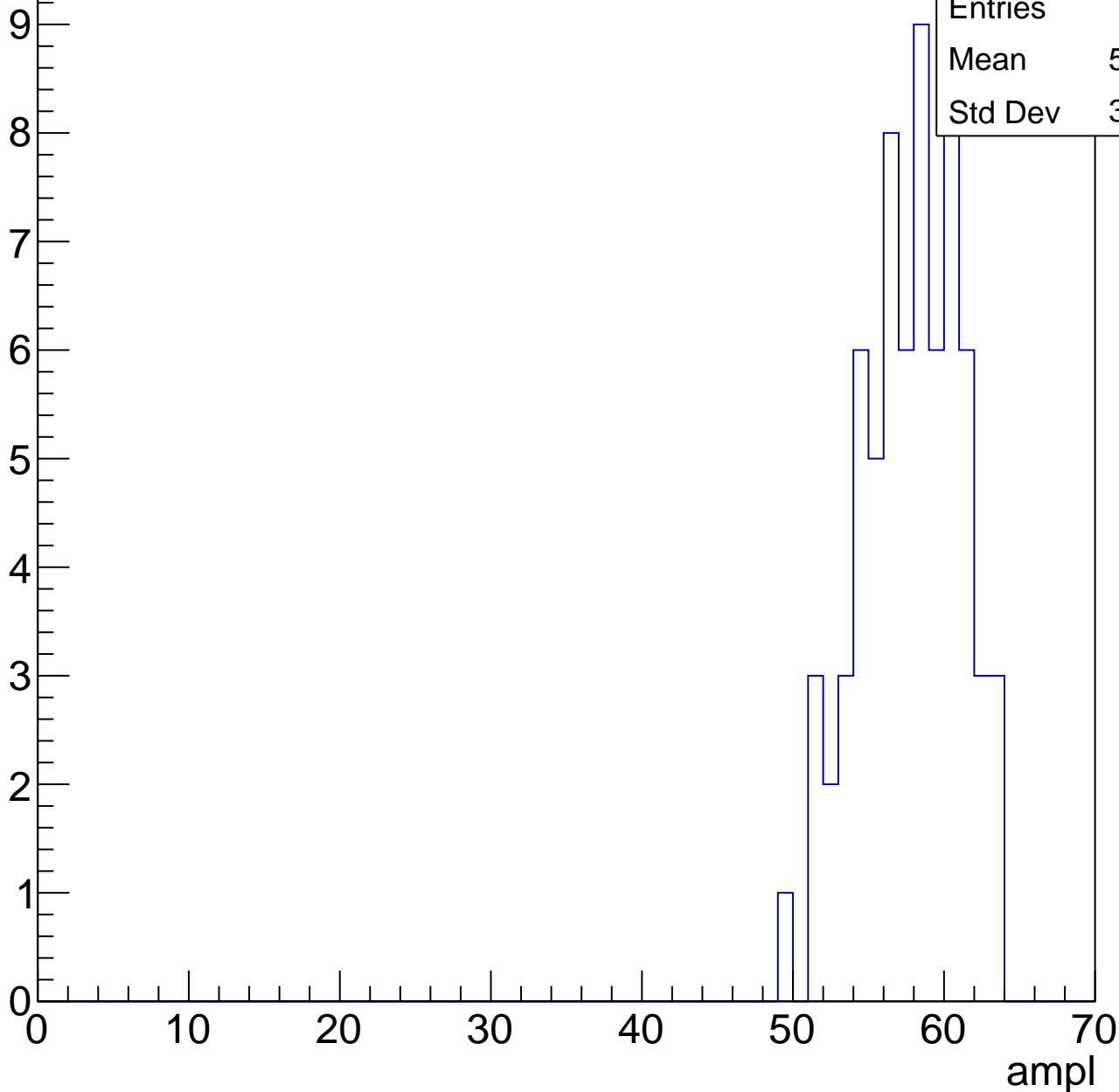


# B0L000S, U7-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	69
Mean	57.26
Std Dev	3.256

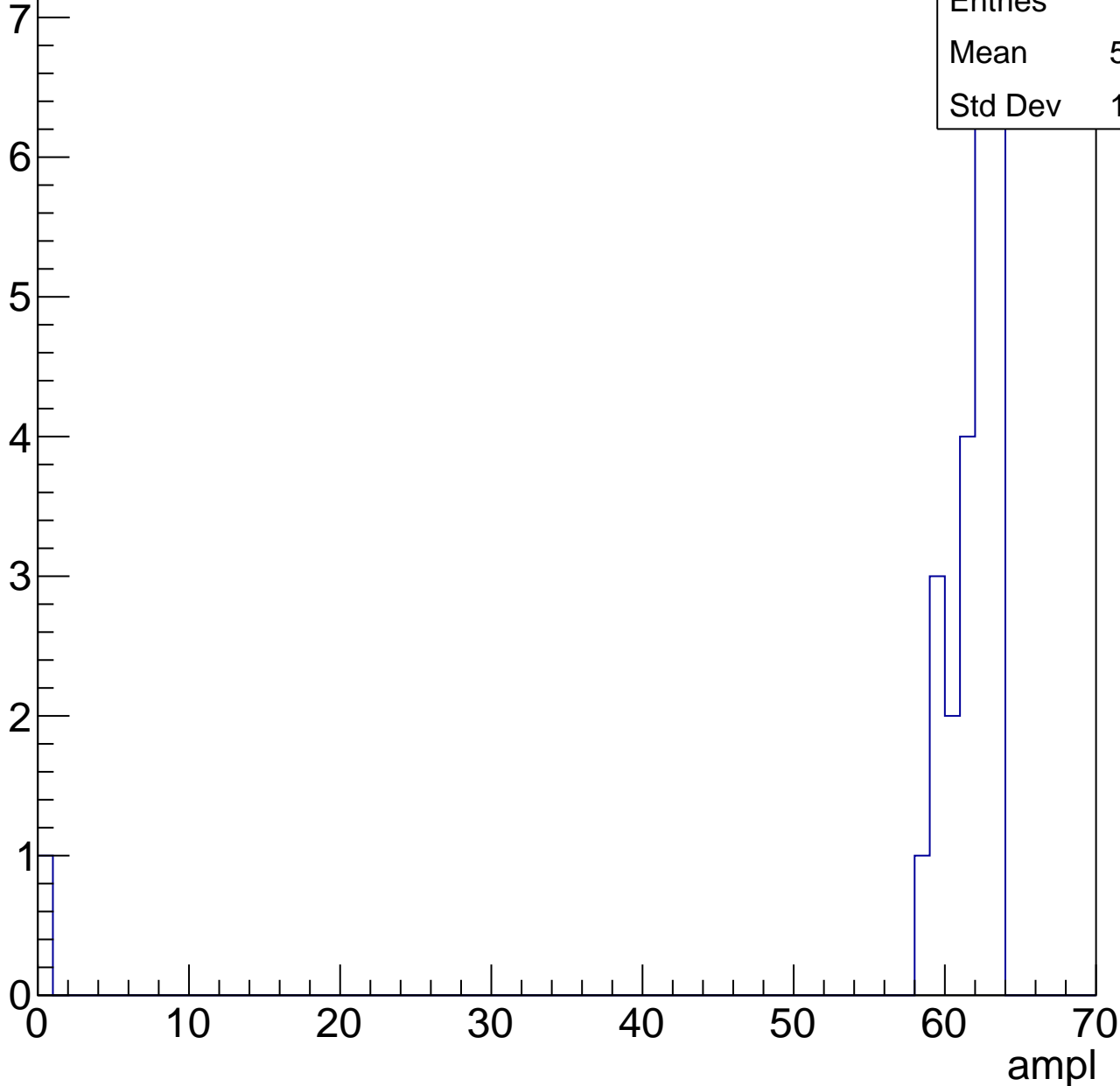


# B0L000S, U7-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	25
Mean	58.96
Std Dev	12.12



# B0L000S, U7-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



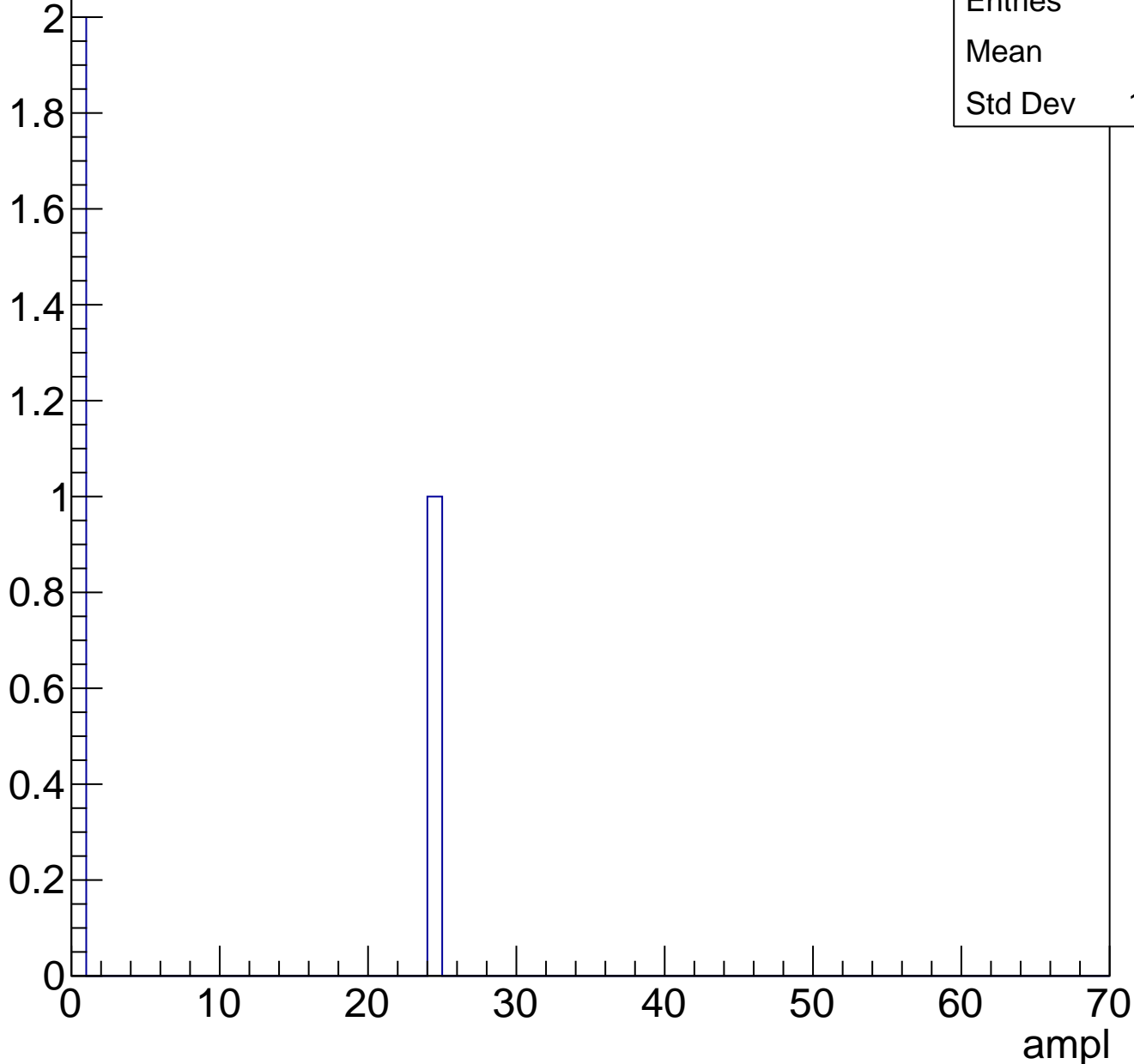
Entries	0
Mean	0
Std Dev	0



# B0L000S, U7-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch18, adc0

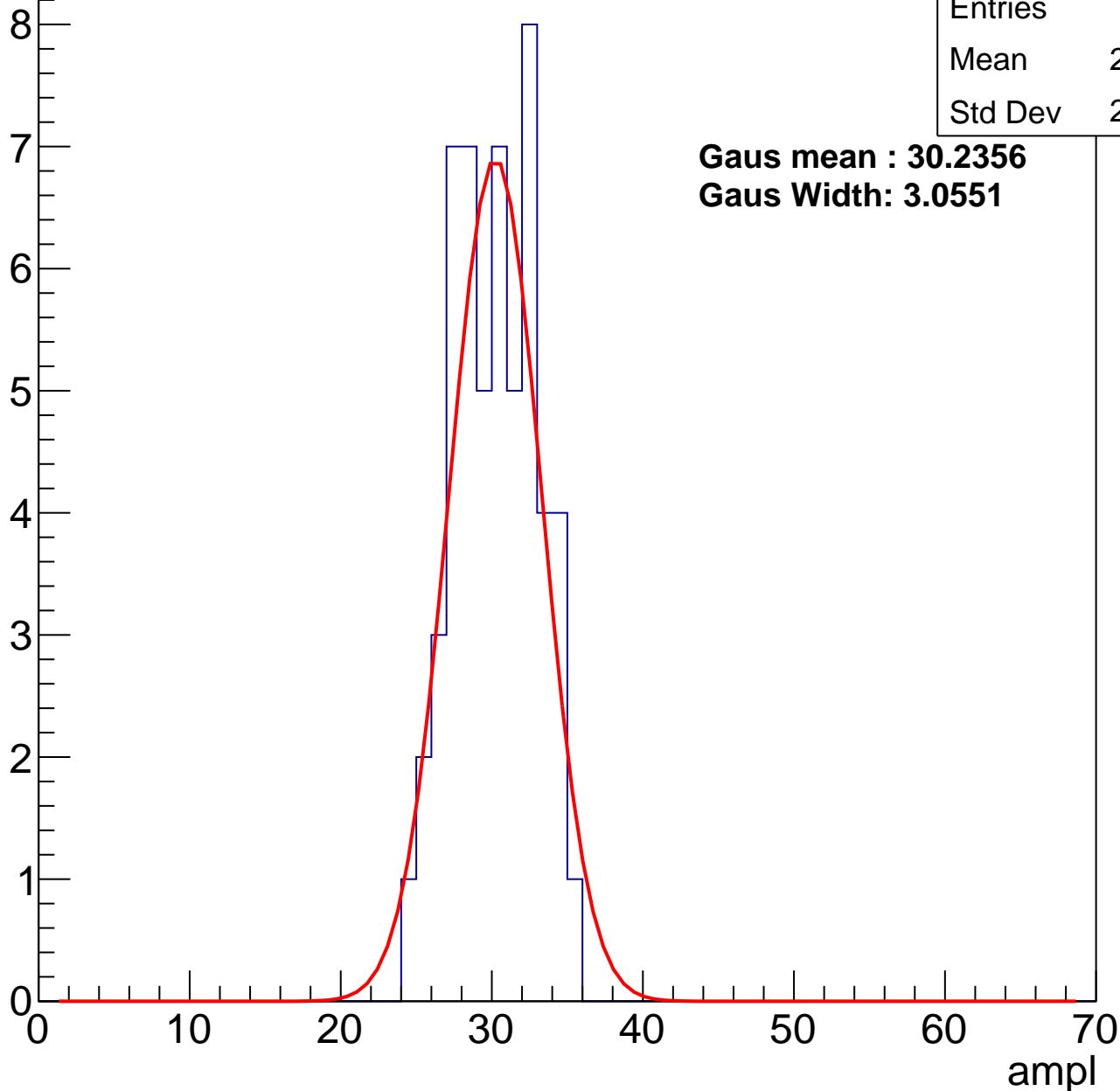
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	54
Mean	29.74
Std Dev	2.682

**Gaus mean : 30.2356**

**Gaus Width: 3.0551**



# B0L000S, U7-ch18, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	76
Mean	36.3
Std Dev	3.325

**Gaus mean : 36.9671**

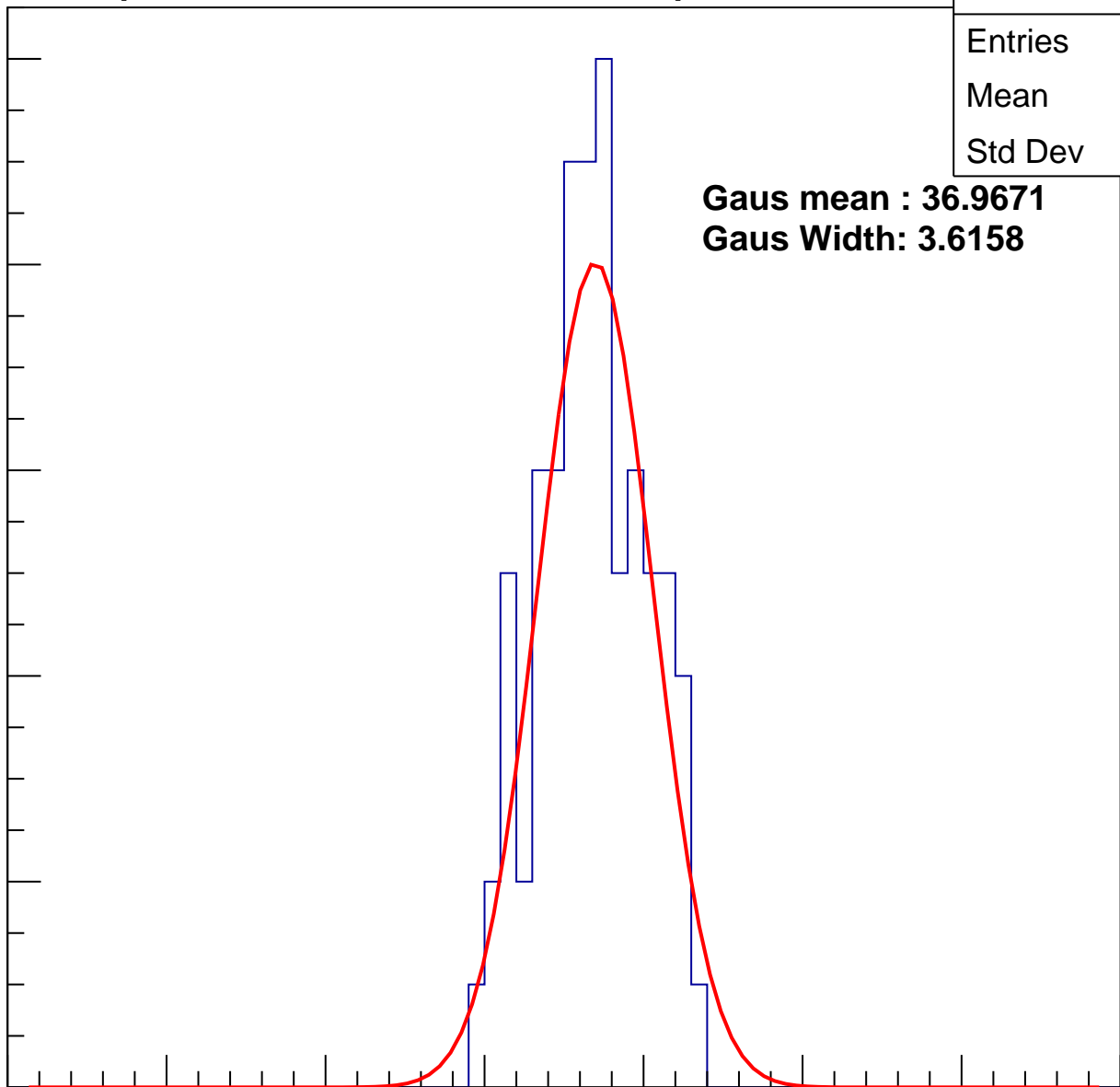
**Gaus Width: 3.6158**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L000S, U7-ch18, adc2

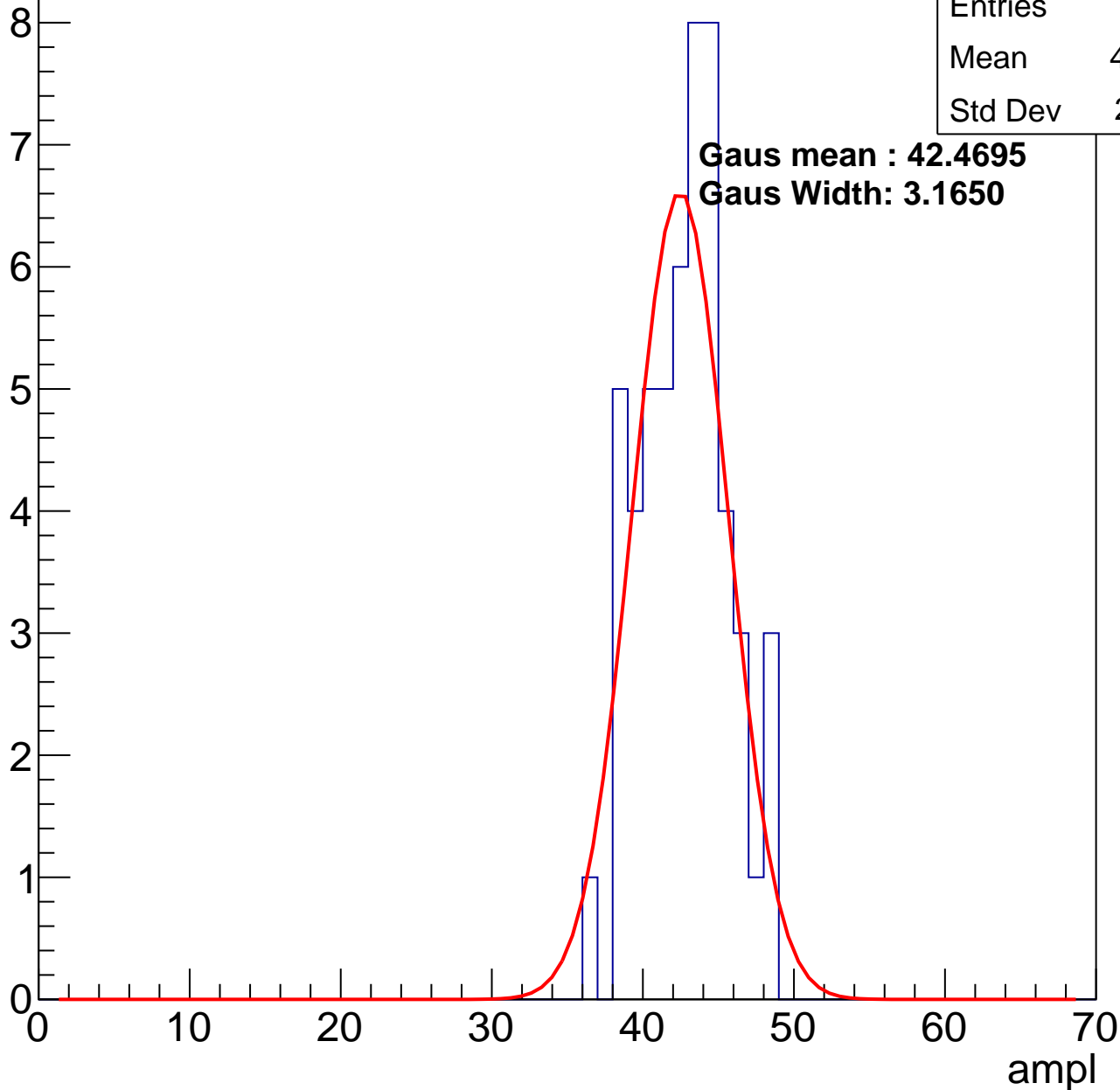
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	53
Mean	42.34
Std Dev	2.841

**Gaus mean : 42.4695**

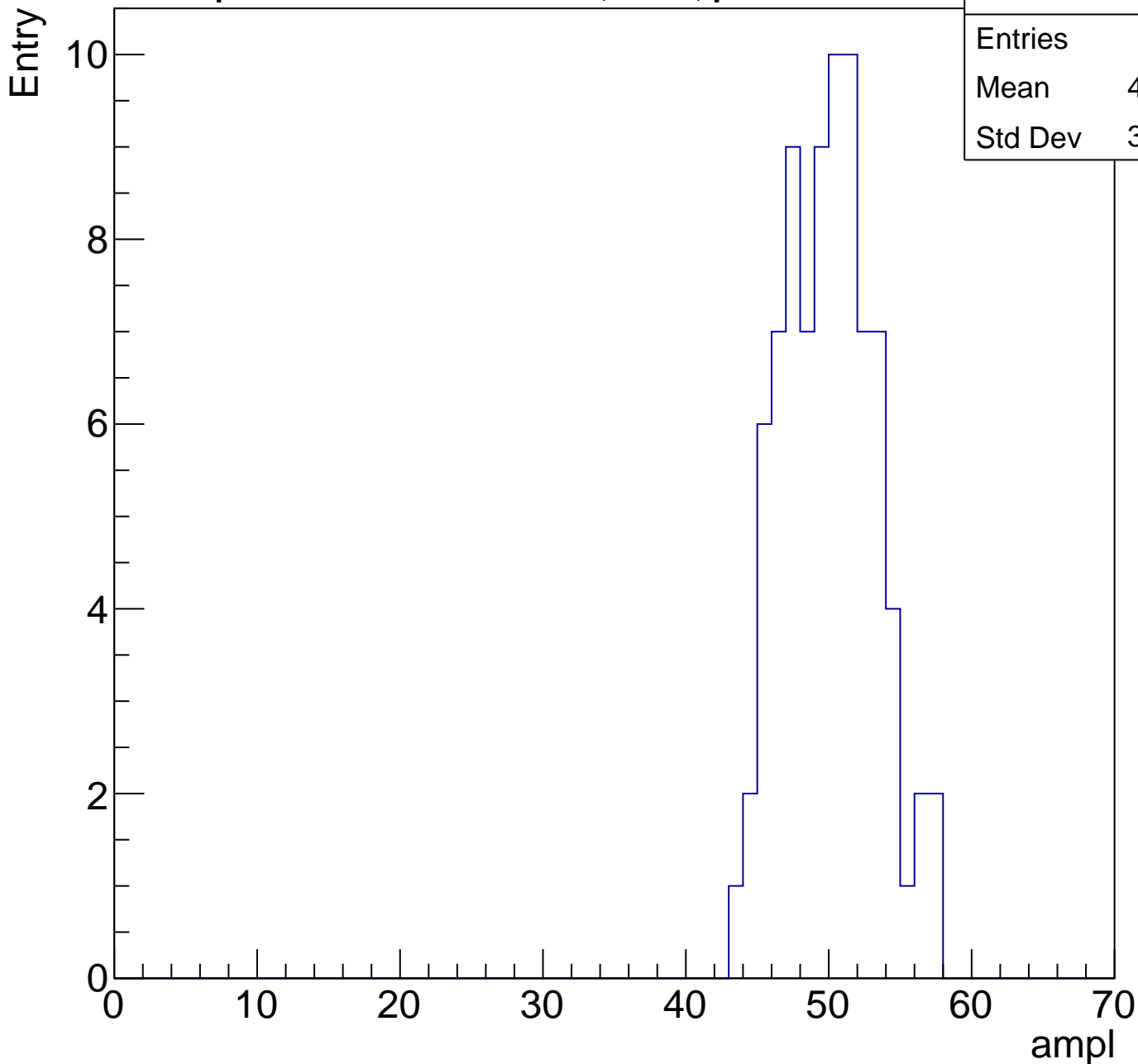
**Gaus Width: 3.1650**



# B0L000S, U7-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

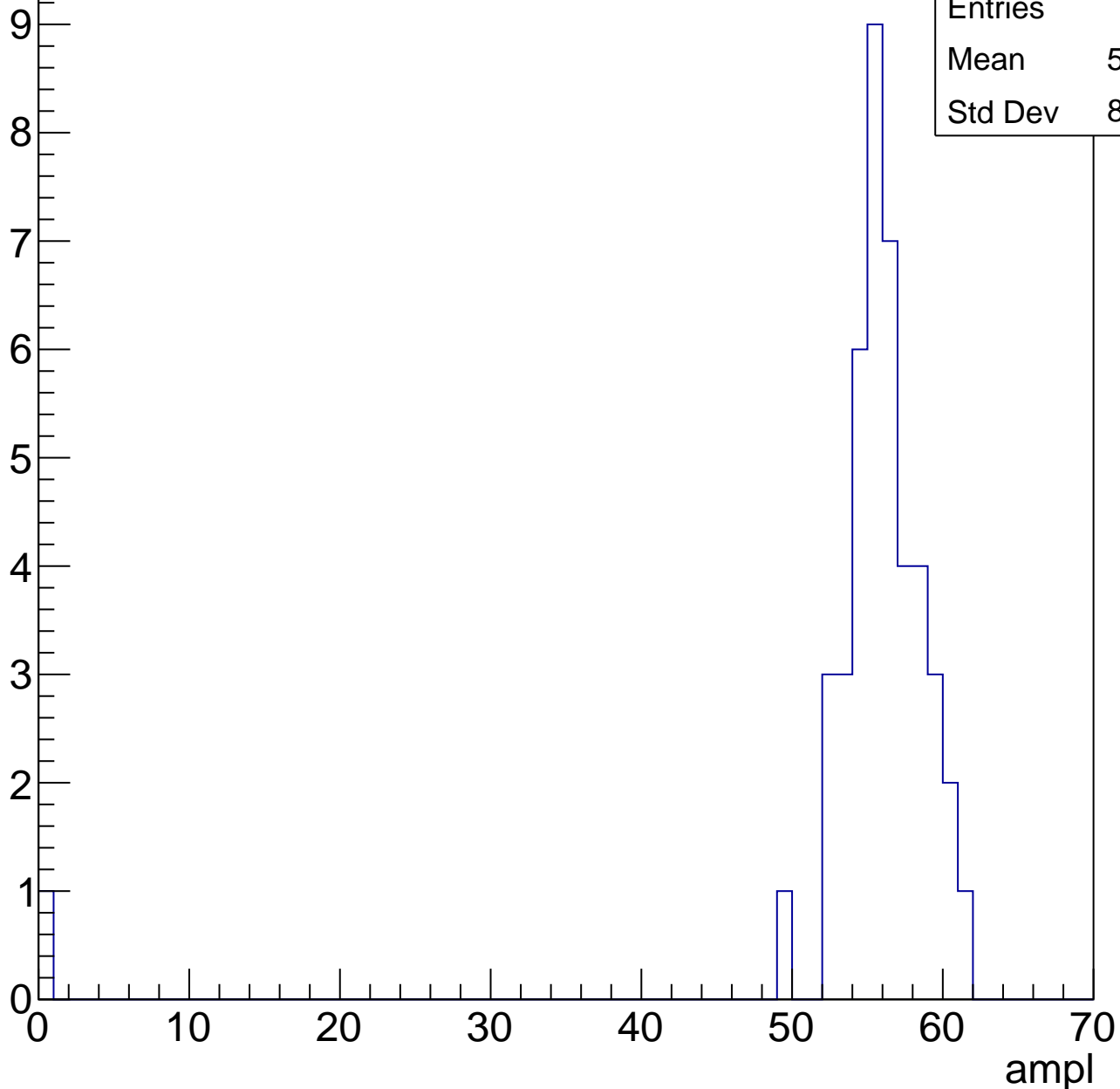
Entries	84
Mean	49.58
Std Dev	3.174



# B0L000S, U7-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

Entries	52
Mean	60.4
Std Dev	2.002

# B0L000S, U7-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L000S, U7-ch19, adc0

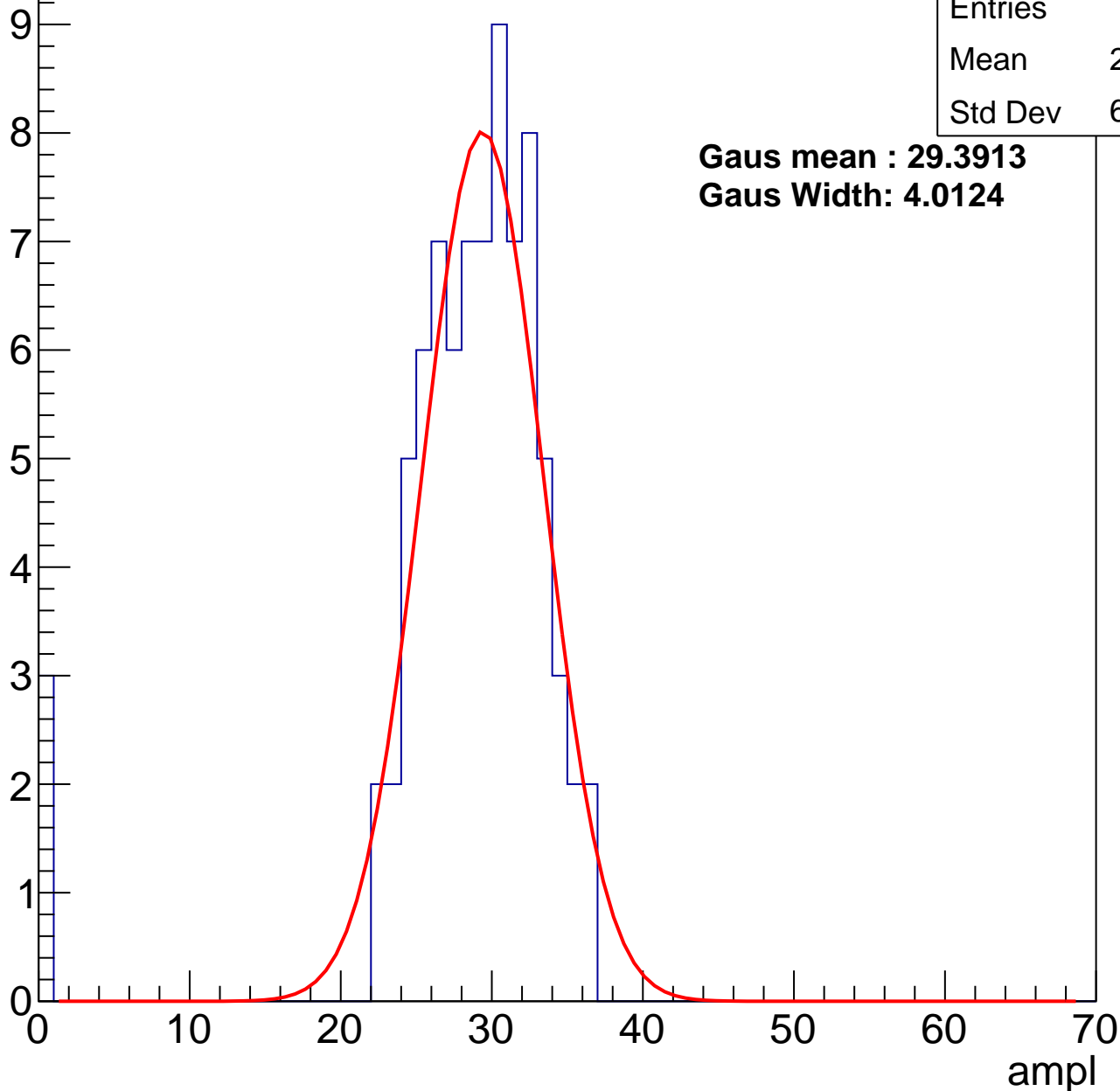
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	81
Mean	27.84
Std Dev	6.415

**Gaus mean : 29.3913**

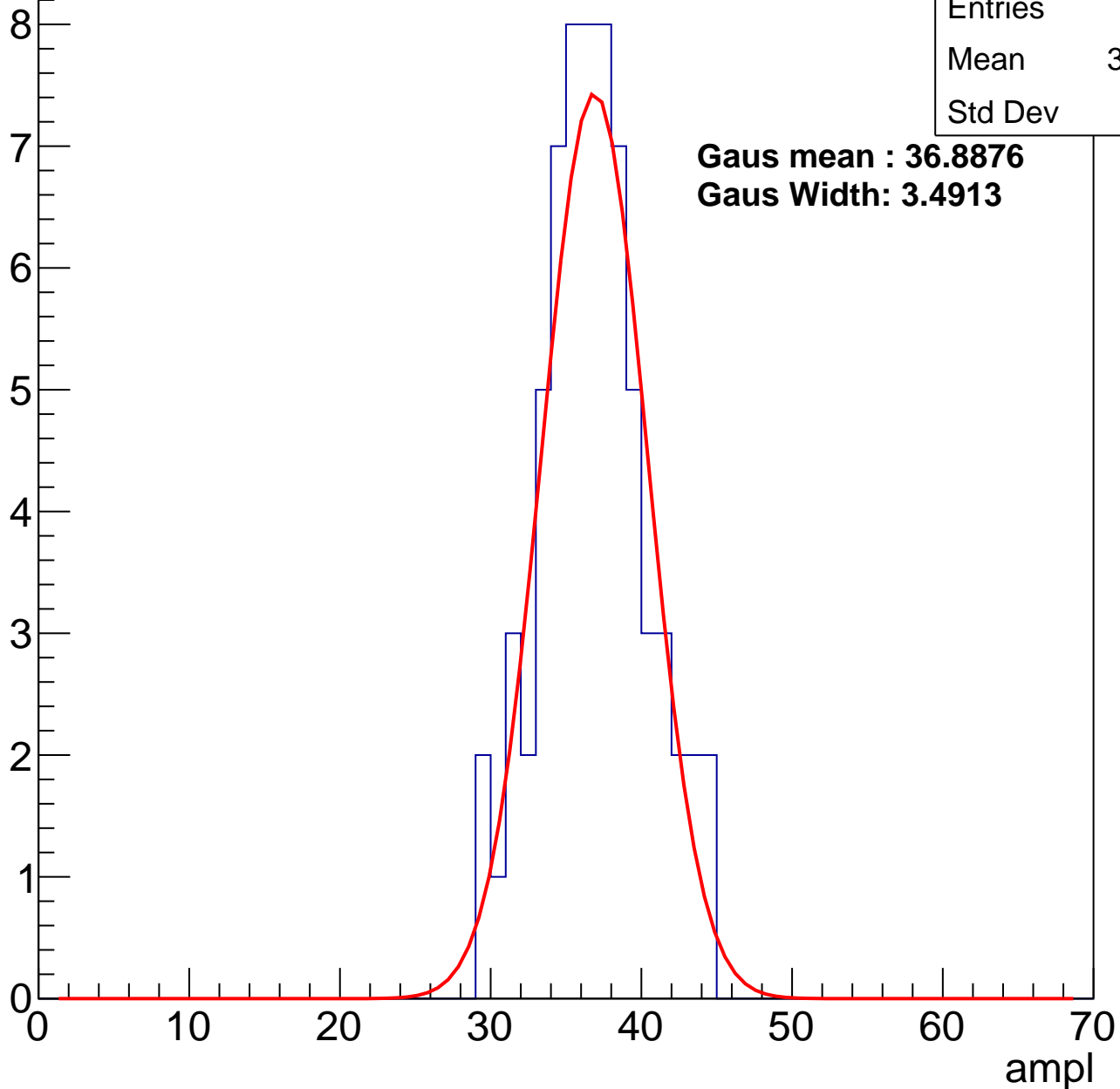
**Gaus Width: 4.0124**



# B0L000S, U7-ch19, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch19, adc2

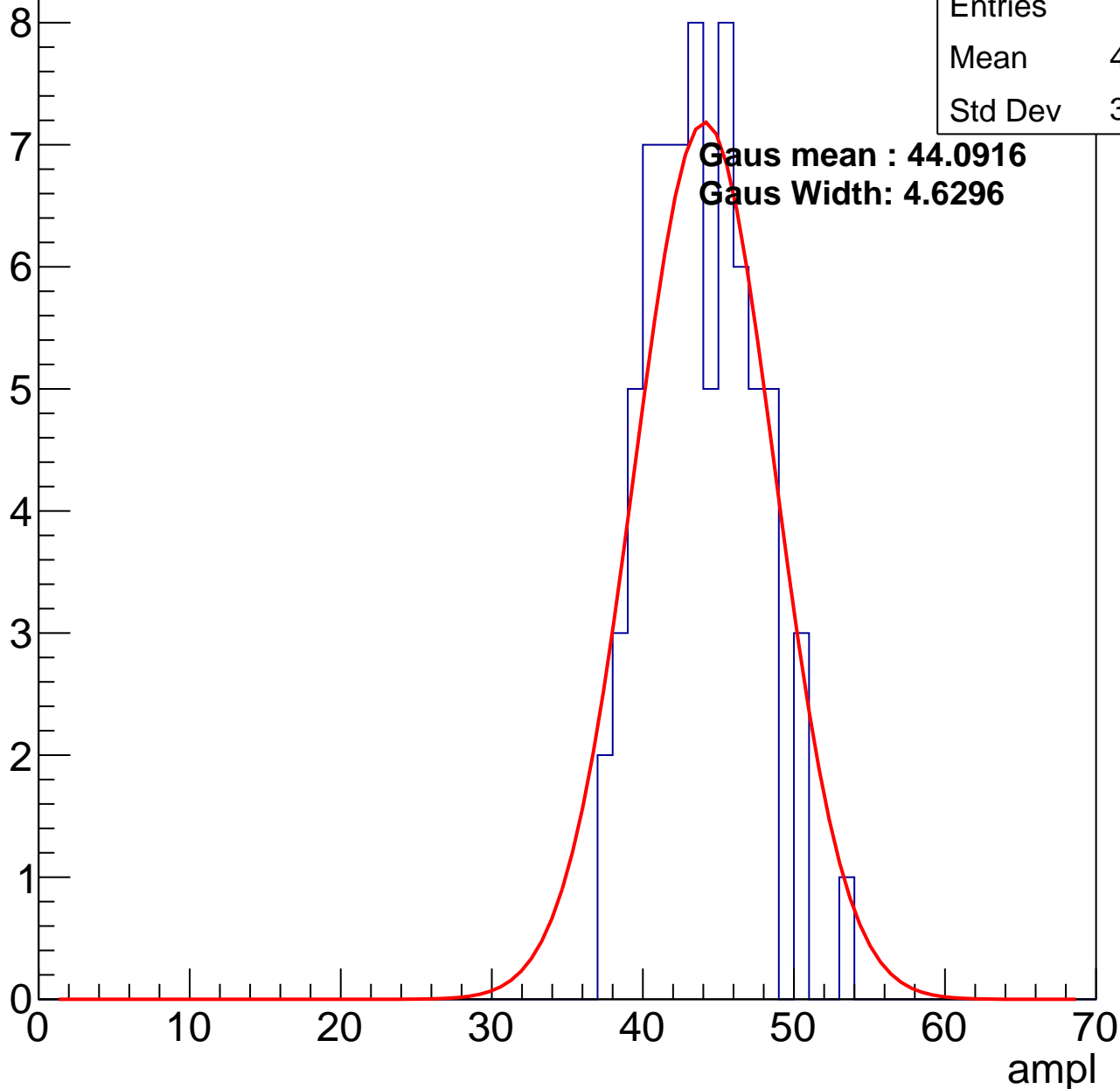
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	72
Mean	43.36
Std Dev	3.453

**Gaus mean : 44.0916**

**Gaus Width: 4.6296**

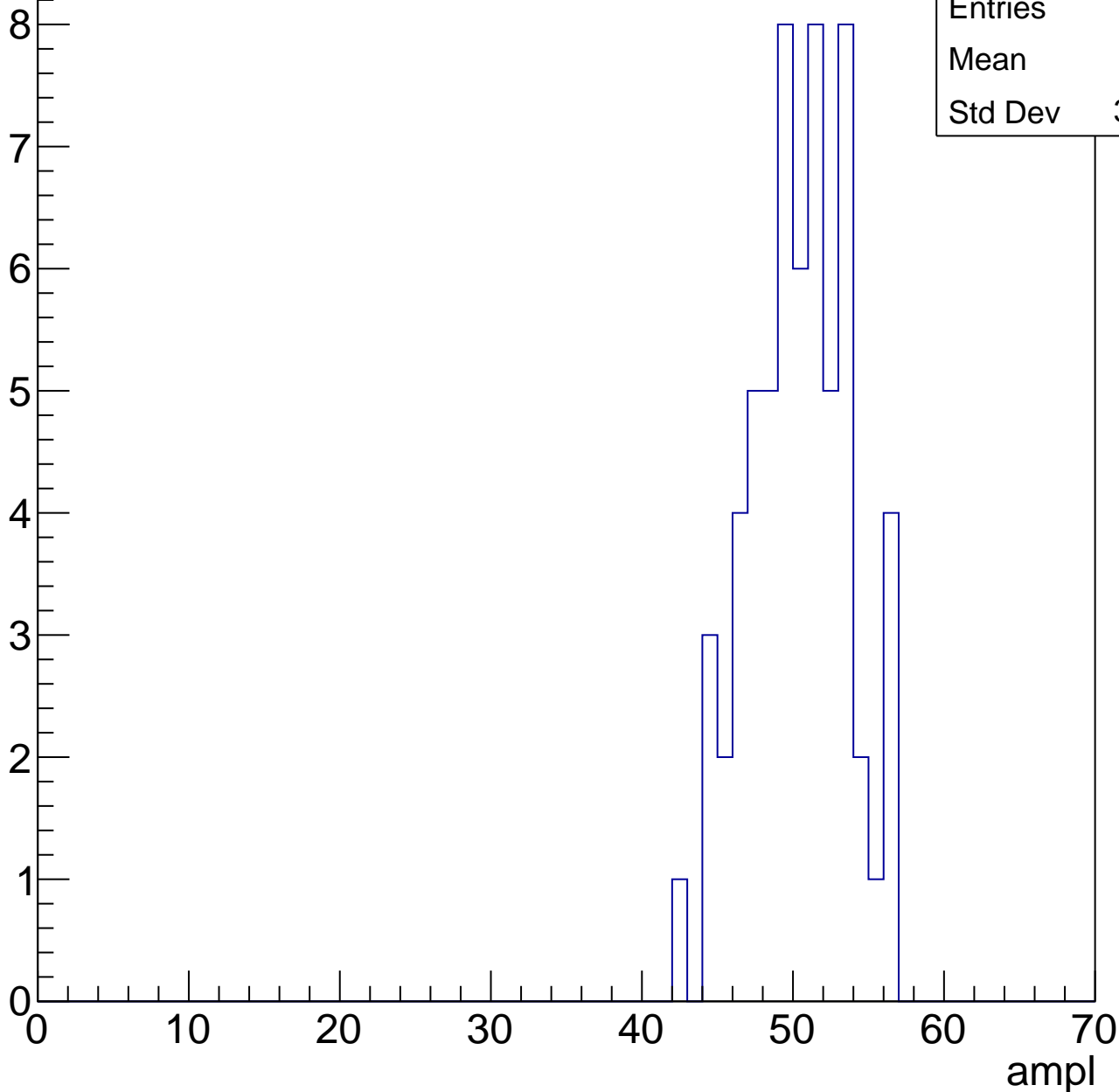


# B0L000S, U7-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

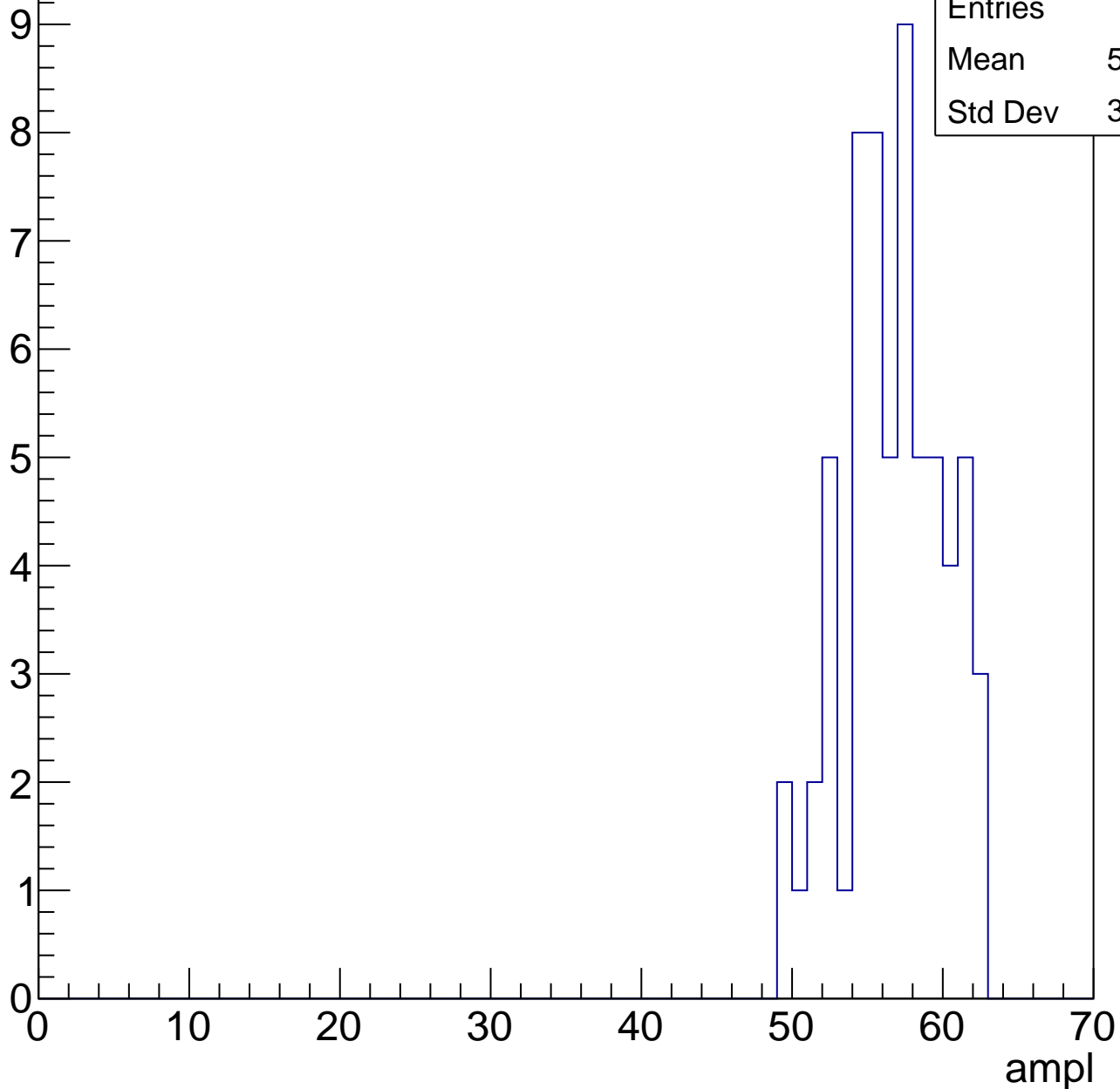
Entries	62
Mean	49.9
Std Dev	3.261



# B0L000S, U7-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

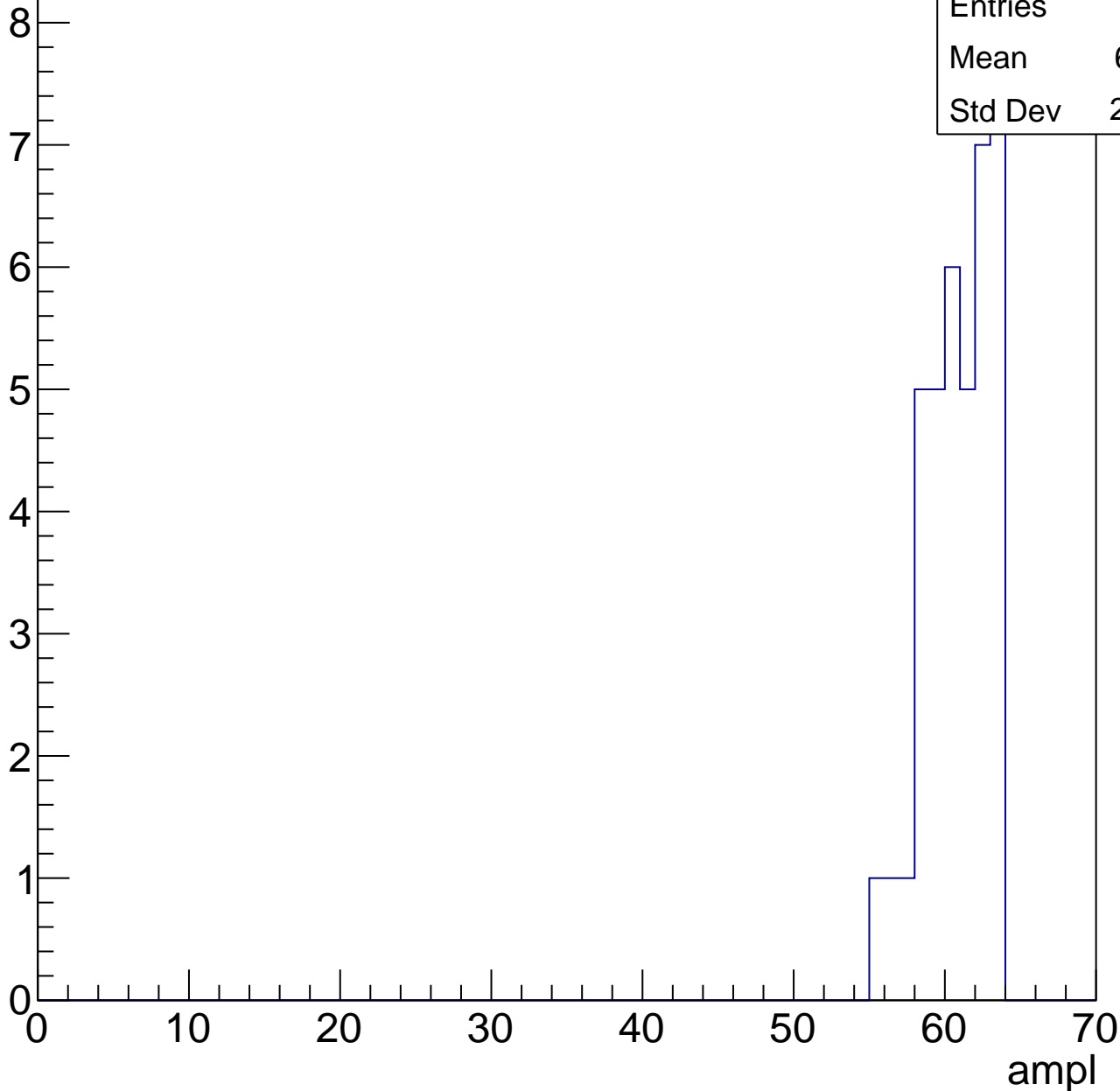


# B0L000S, U7-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	39
Mean	60.41
Std Dev	2.109



# B0L000S, U7-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L000S, U7-ch20, adc0

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	77
Mean	30.62
Std Dev	3.24

**Gaus mean : 31.1415**

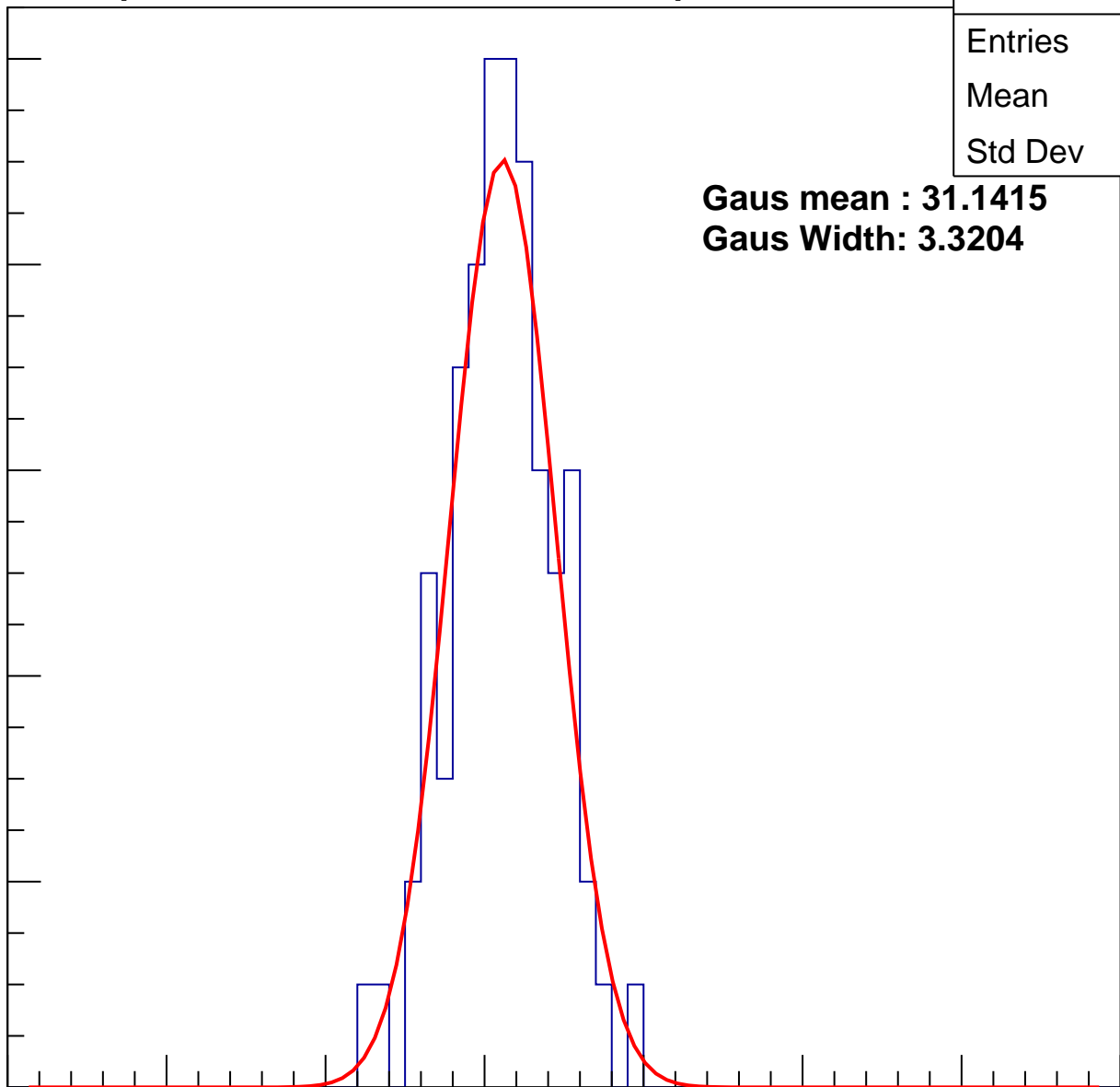
**Gaus Width: 3.3204**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L000S, U7-ch20, adc1

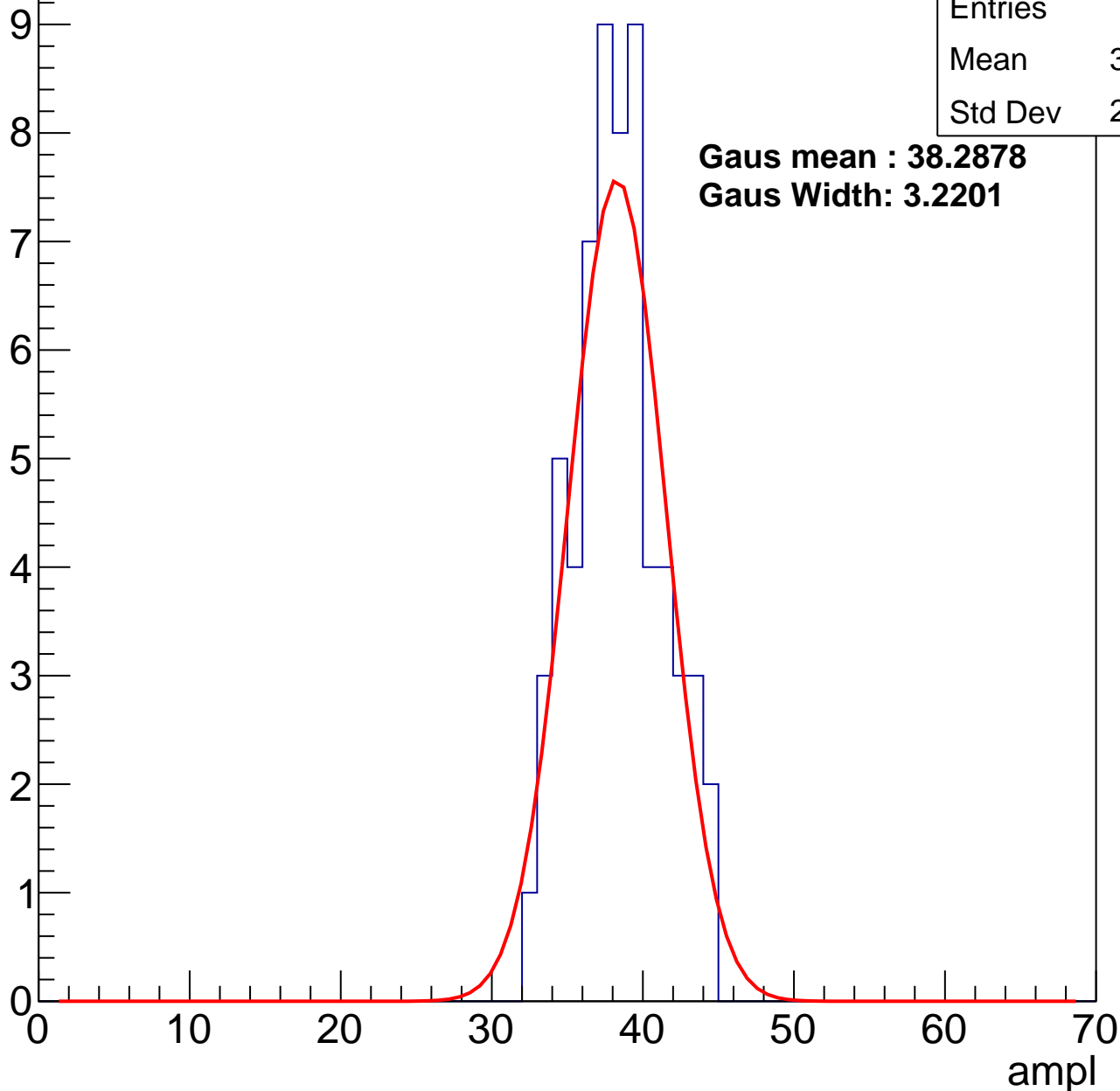
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	62
Mean	37.87
Std Dev	2.893

**Gaus mean : 38.2878**

**Gaus Width: 3.2201**



# B0L000S, U7-ch20, adc2

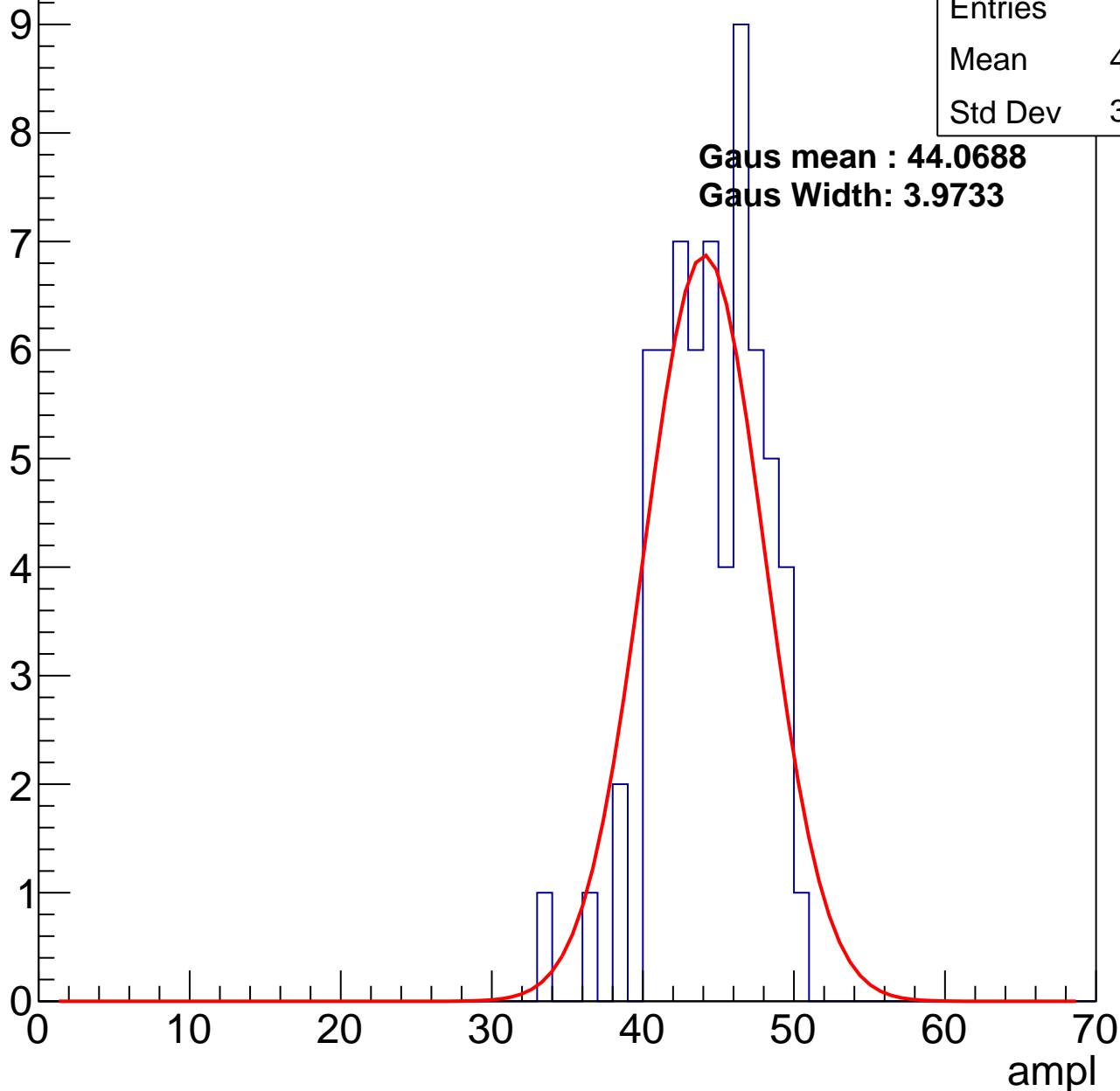
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	65
Mean	43.89
Std Dev	3.397

**Gaus mean : 44.0688**

**Gaus Width: 3.9733**

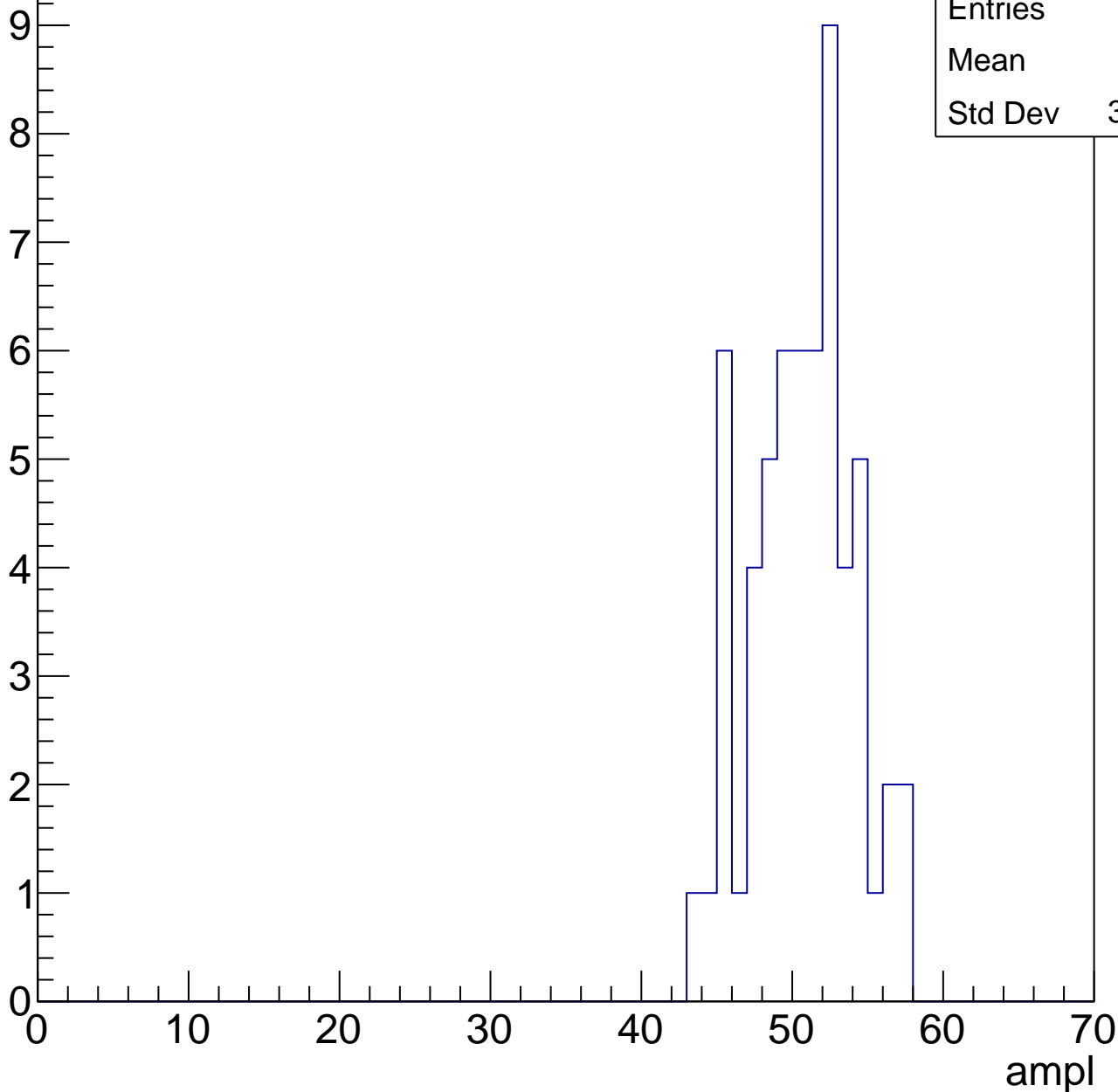


# B0L000S, U7-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

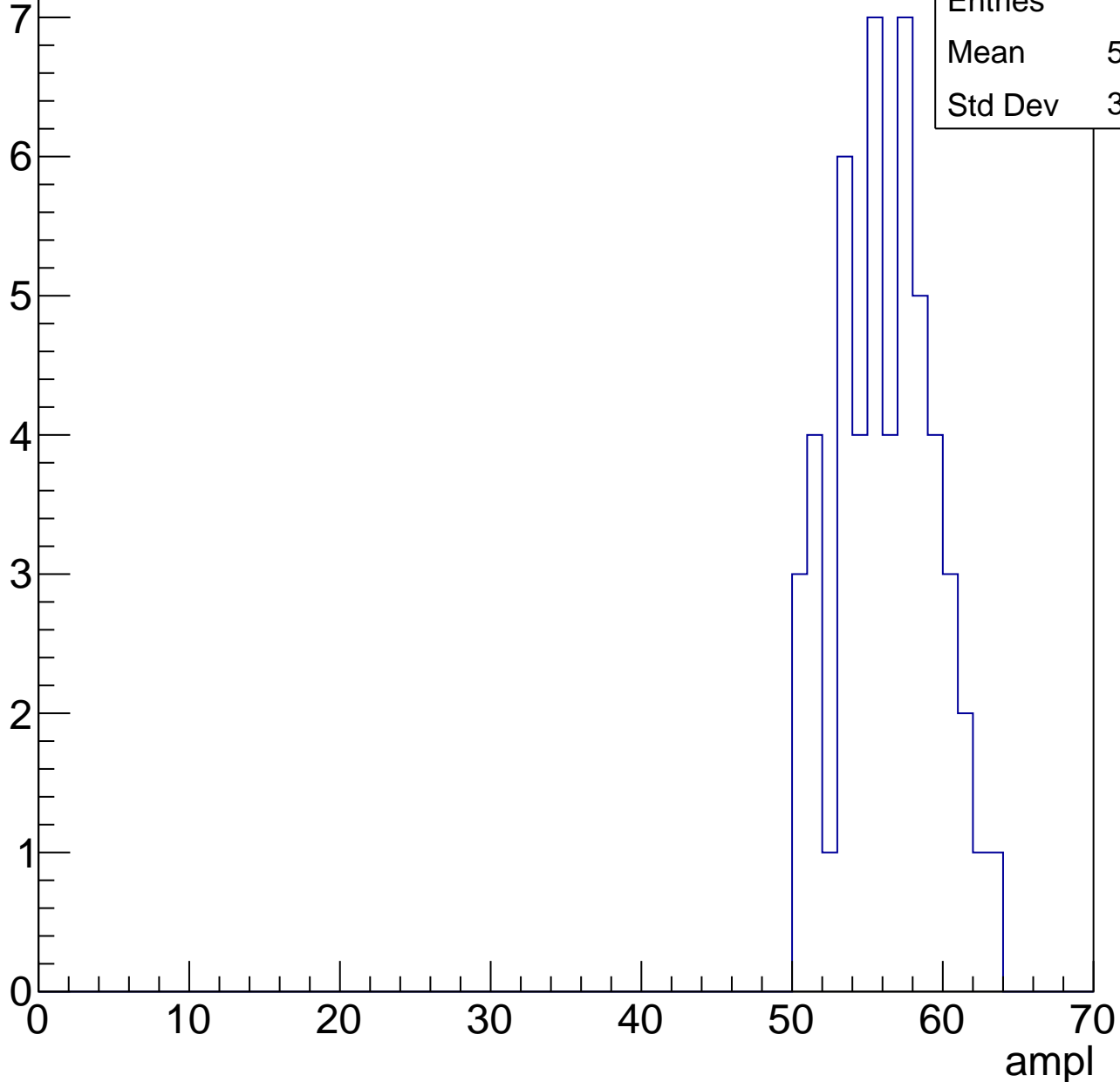
Entries	59
Mean	50.2
Std Dev	3.354



# B0L000S, U7-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



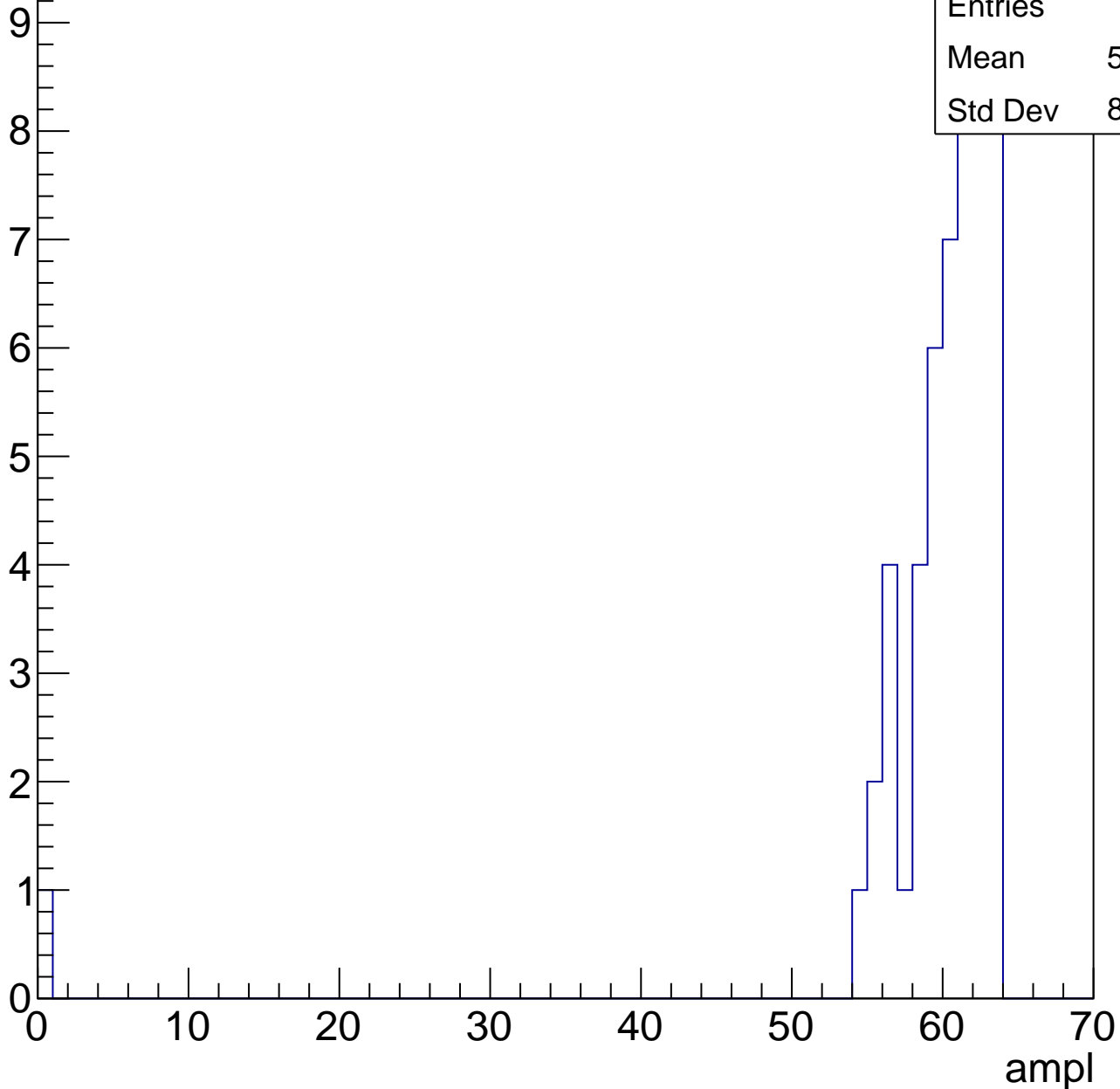
Entries	52
Mean	55.79
Std Dev	3.236

# B0L000S, U7-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	51
Mean	58.84
Std Dev	8.664



# B0L000S, U7-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

2

Mean

60.5

Std Dev

2.5



# B0L000S, U7-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L000S, U7-ch21, adc0

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	73
Mean	30.75
Std Dev	3.297

**Gaus mean : 31.5155**

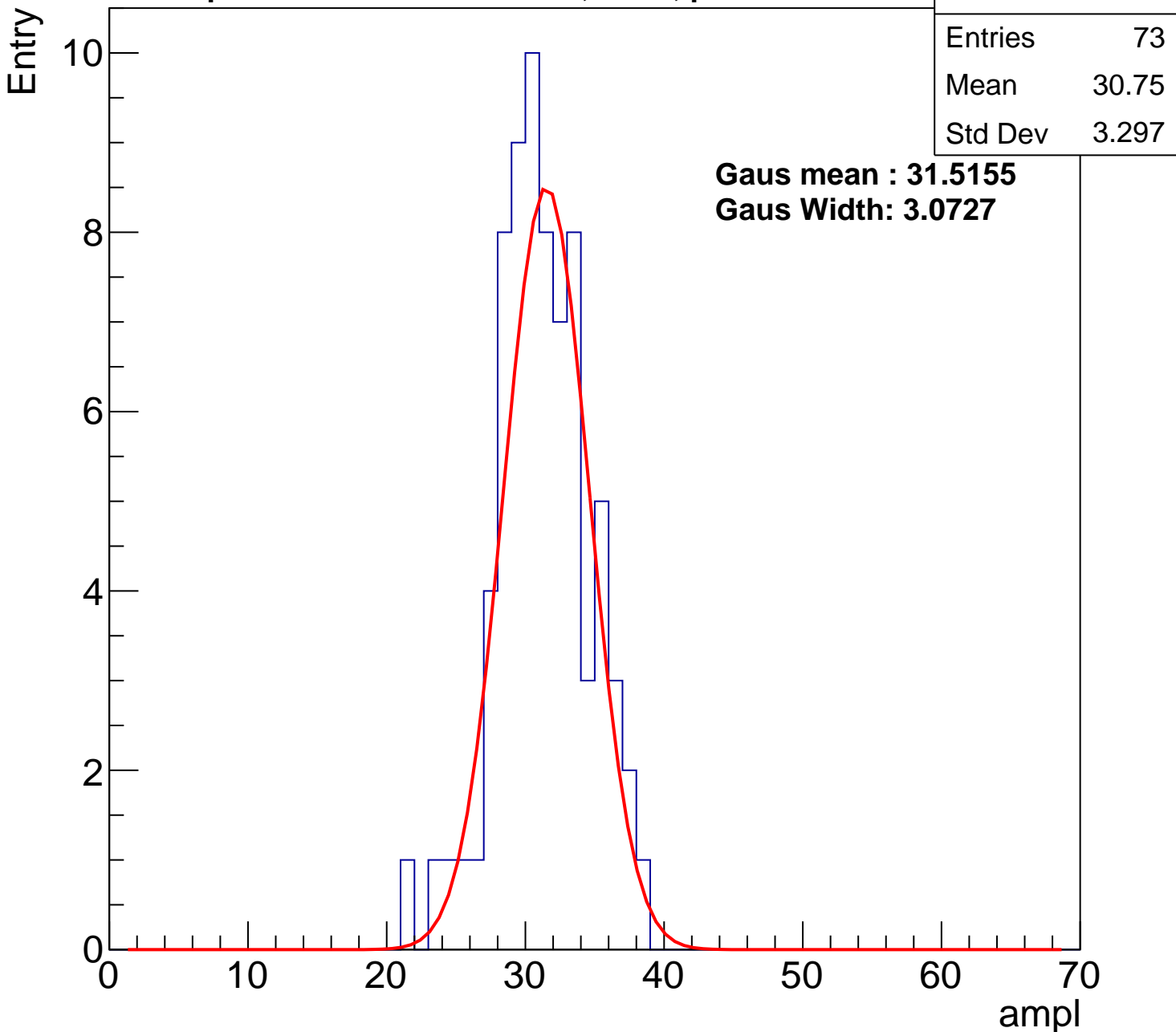
**Gaus Width: 3.0727**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L000S, U7-ch21, adc1

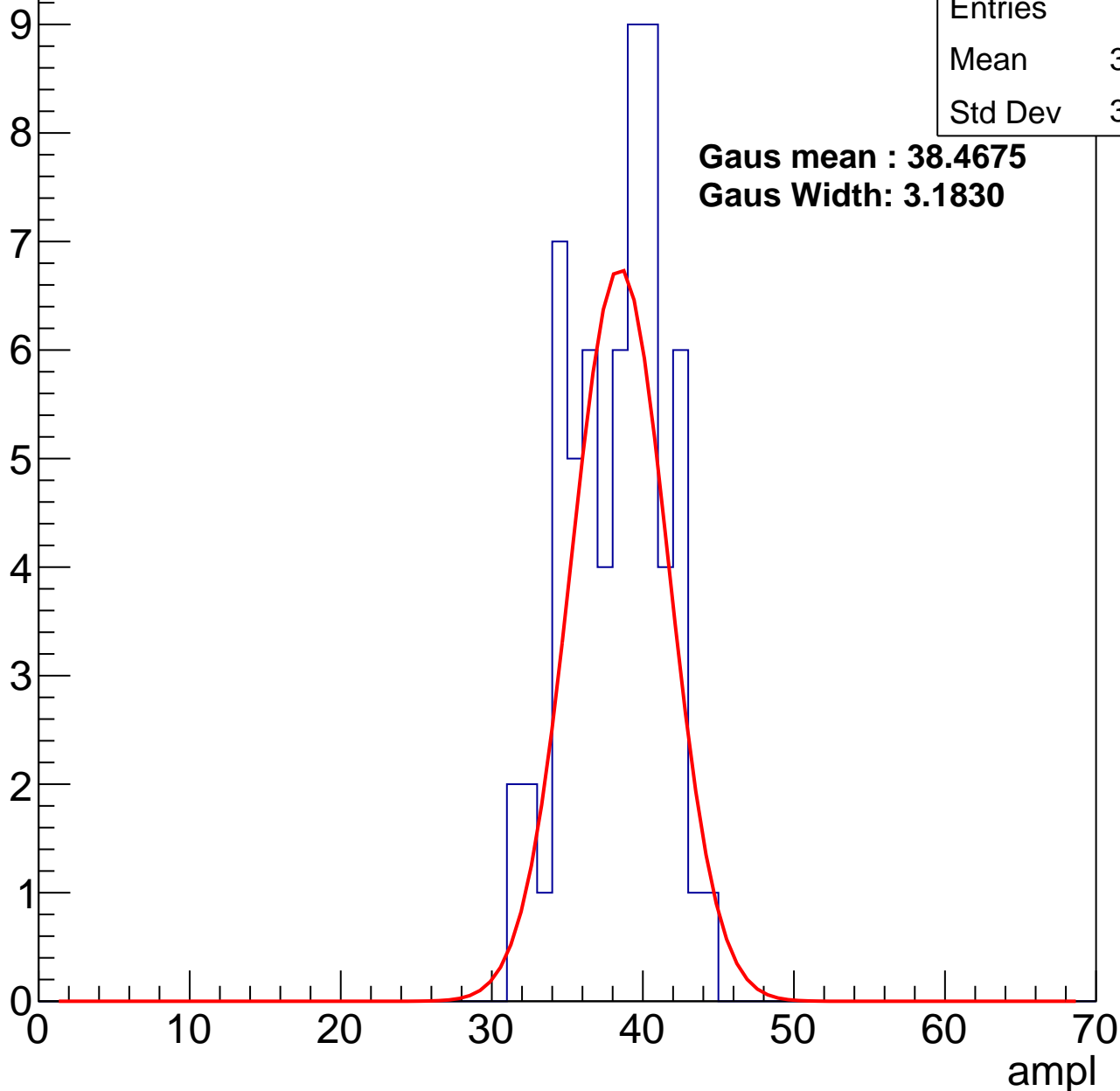
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	63
Mean	37.75
Std Dev	3.122

**Gaus mean : 38.4675**

**Gaus Width: 3.1830**



# B0L000S, U7-ch21, adc2

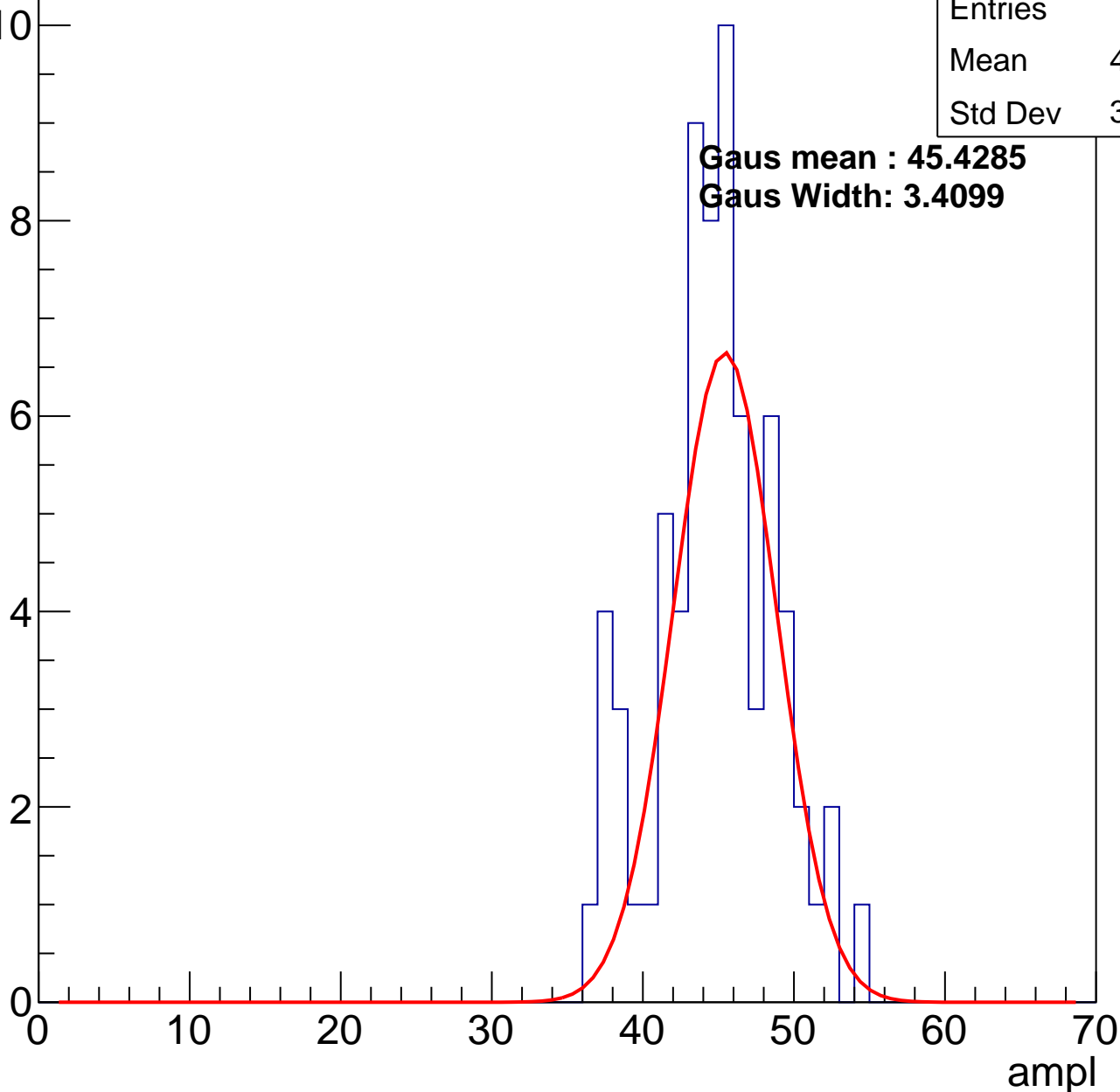
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	71
Mean	44.35
Std Dev	3.893

**Gaus mean : 45.4285**

**Gaus Width: 3.4099**

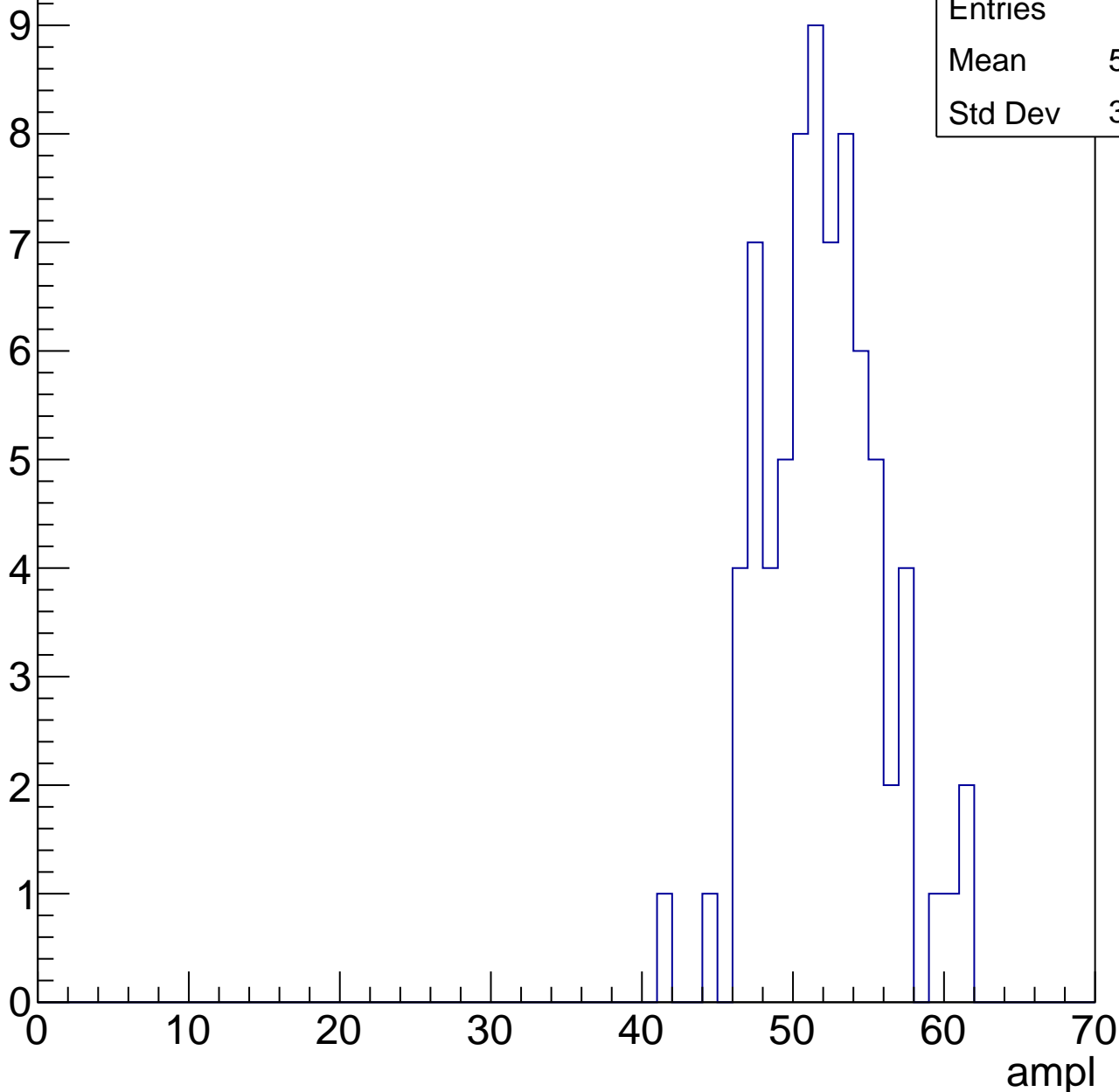


# B0L000S, U7-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	75
Mean	51.49
Std Dev	3.862

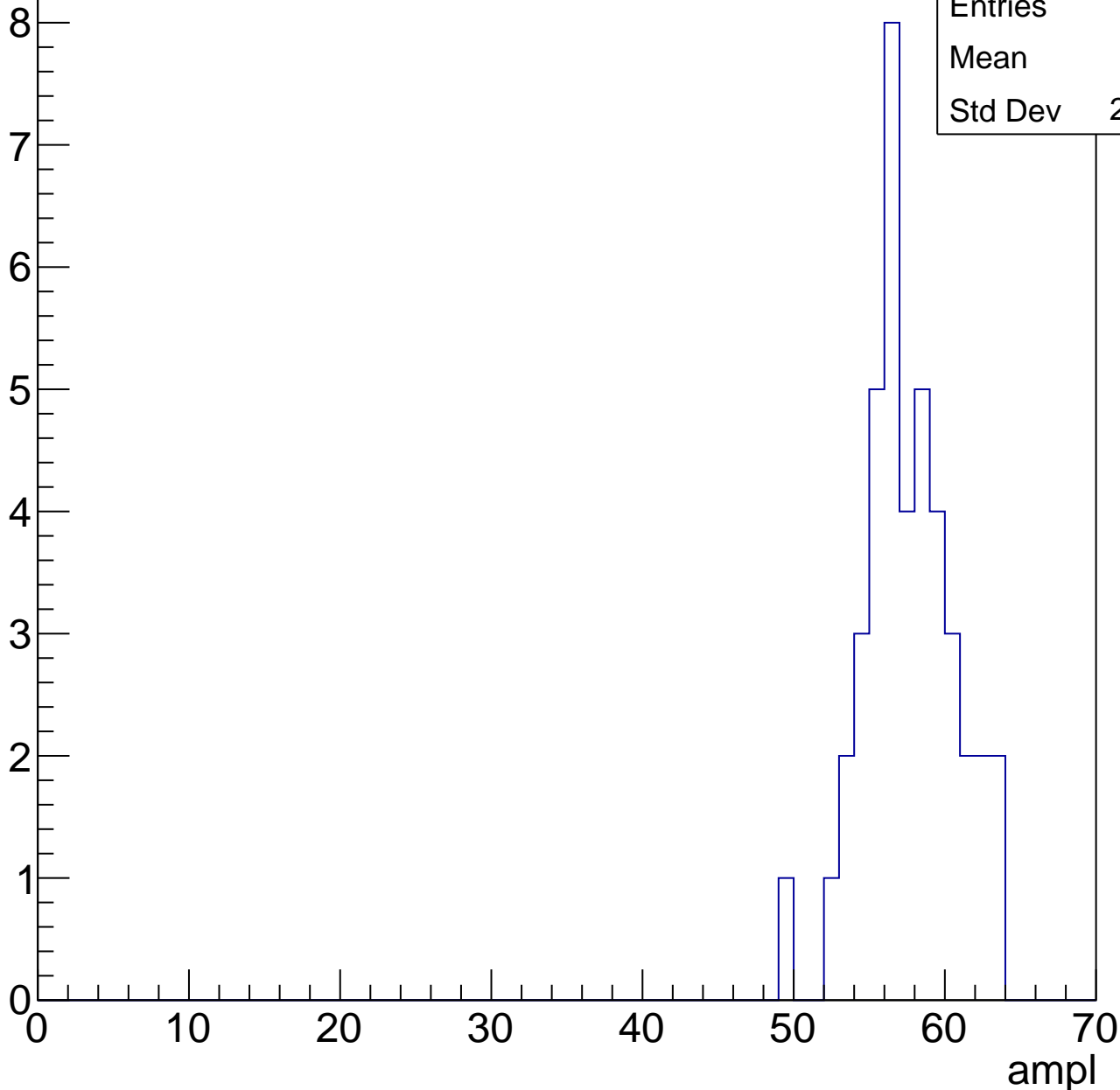


# B0L000S, U7-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	42
Mean	57.1
Std Dev	2.998

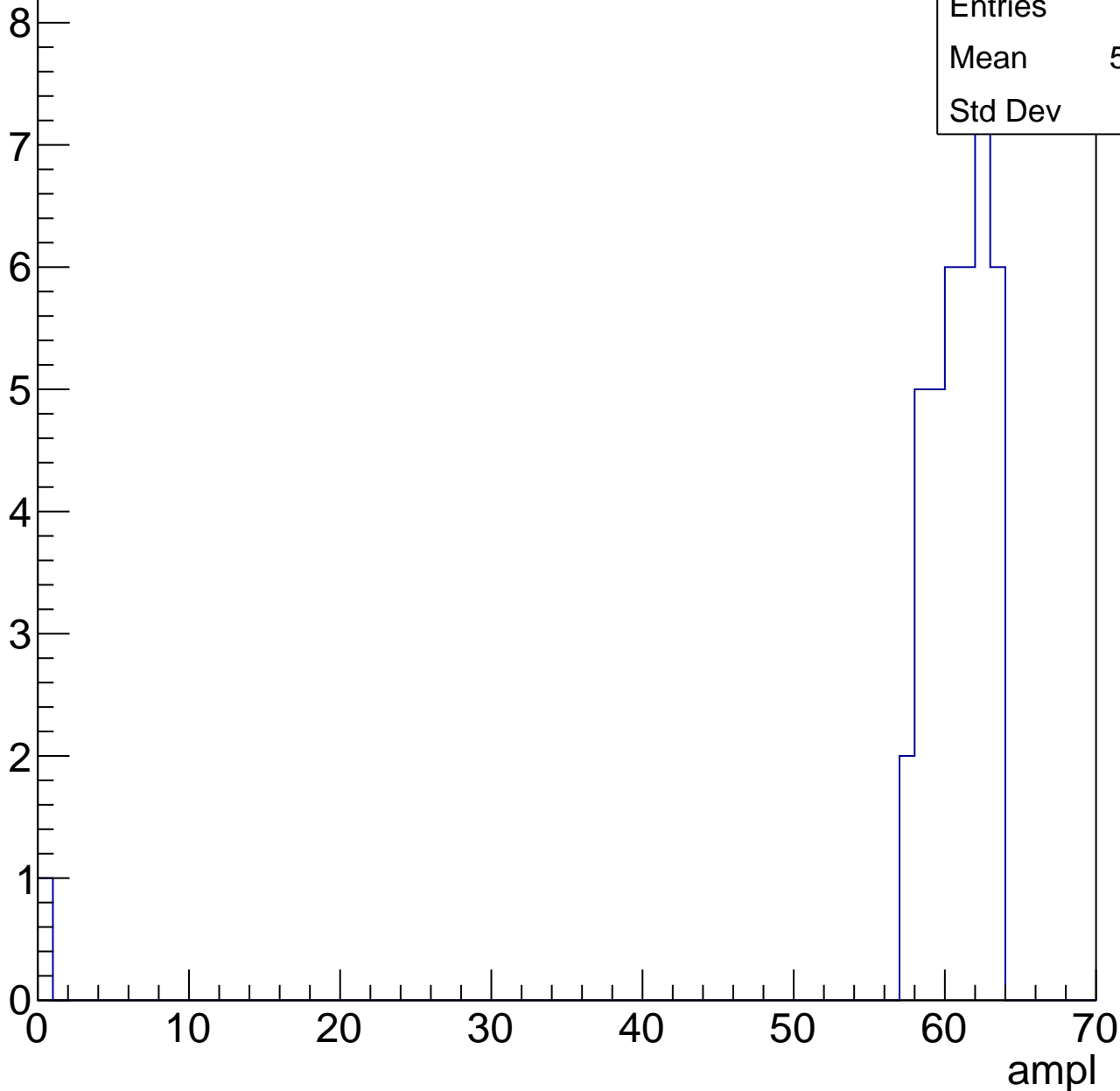


# B0L000S, U7-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	39
Mean	58.95
Std Dev	9.73



# B0L000S, U7-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L000S, U7-ch22, adc0

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	78
Mean	31.59
Std Dev	3.248

**Gaus mean : 32.0061**

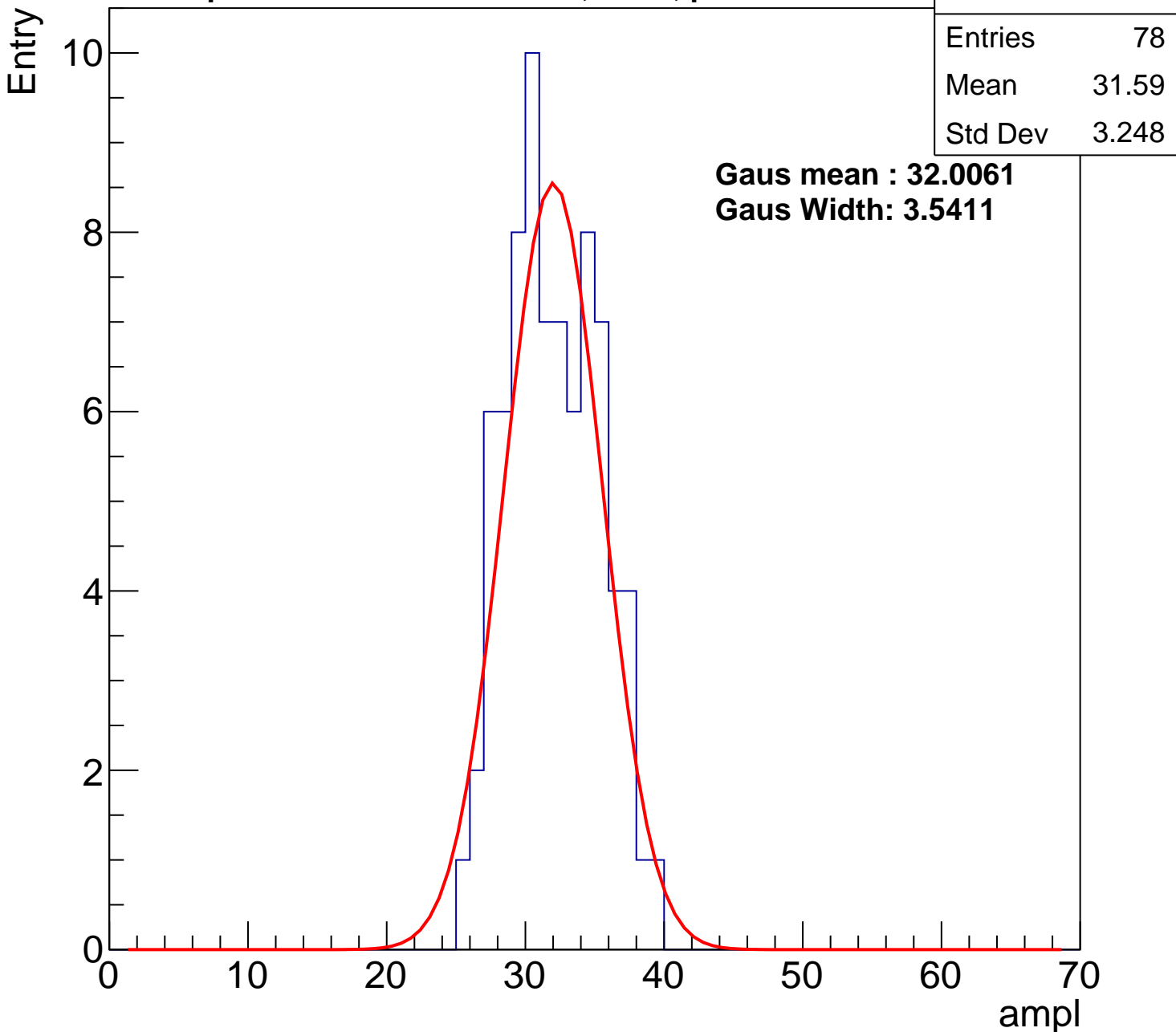
**Gaus Width: 3.5411**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L000S, U7-ch22, adc1

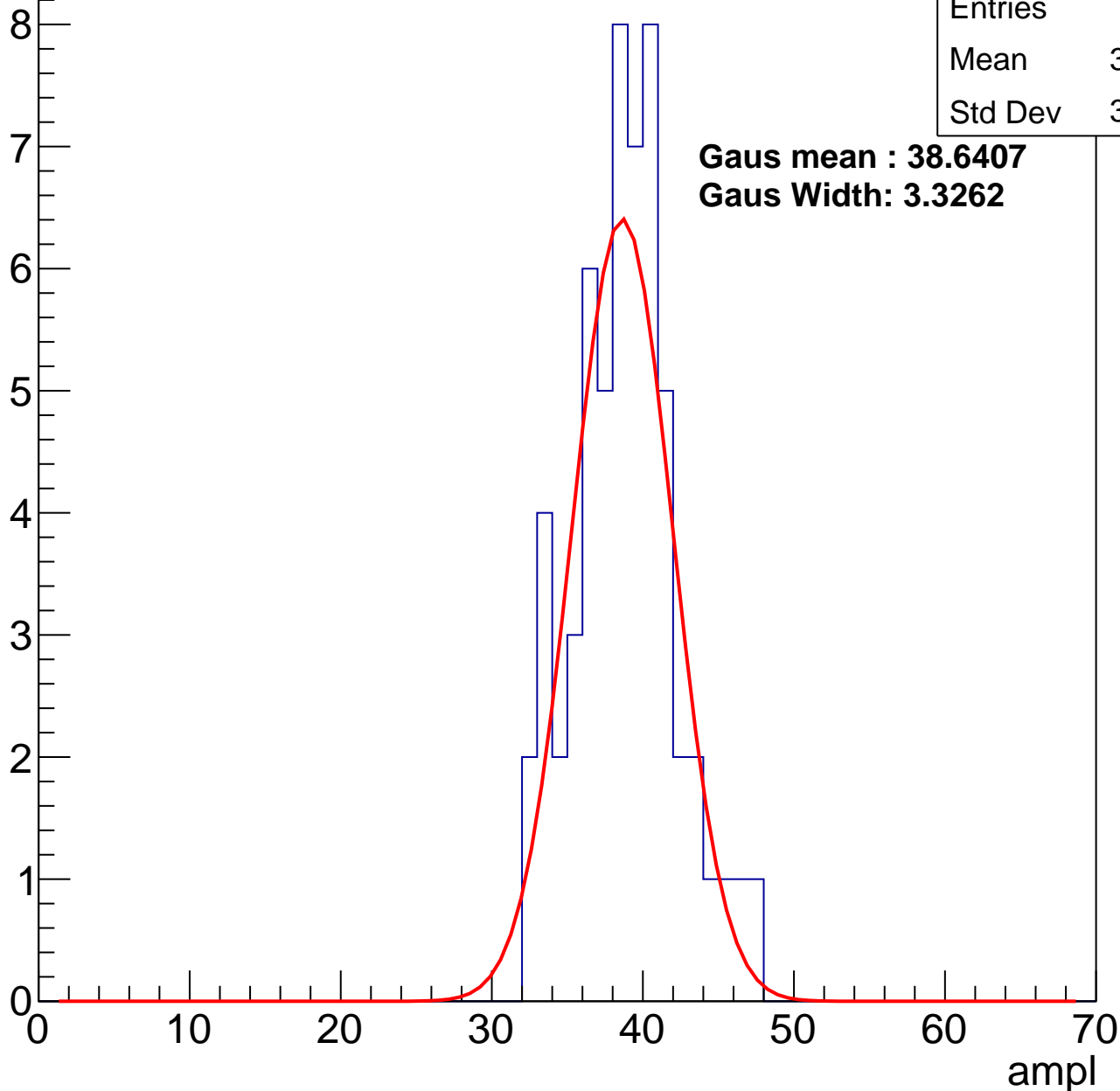
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	58
Mean	38.34
Std Dev	3.345

**Gaus mean : 38.6407**

**Gaus Width: 3.3262**



# B0L000S, U7-ch22, adc2

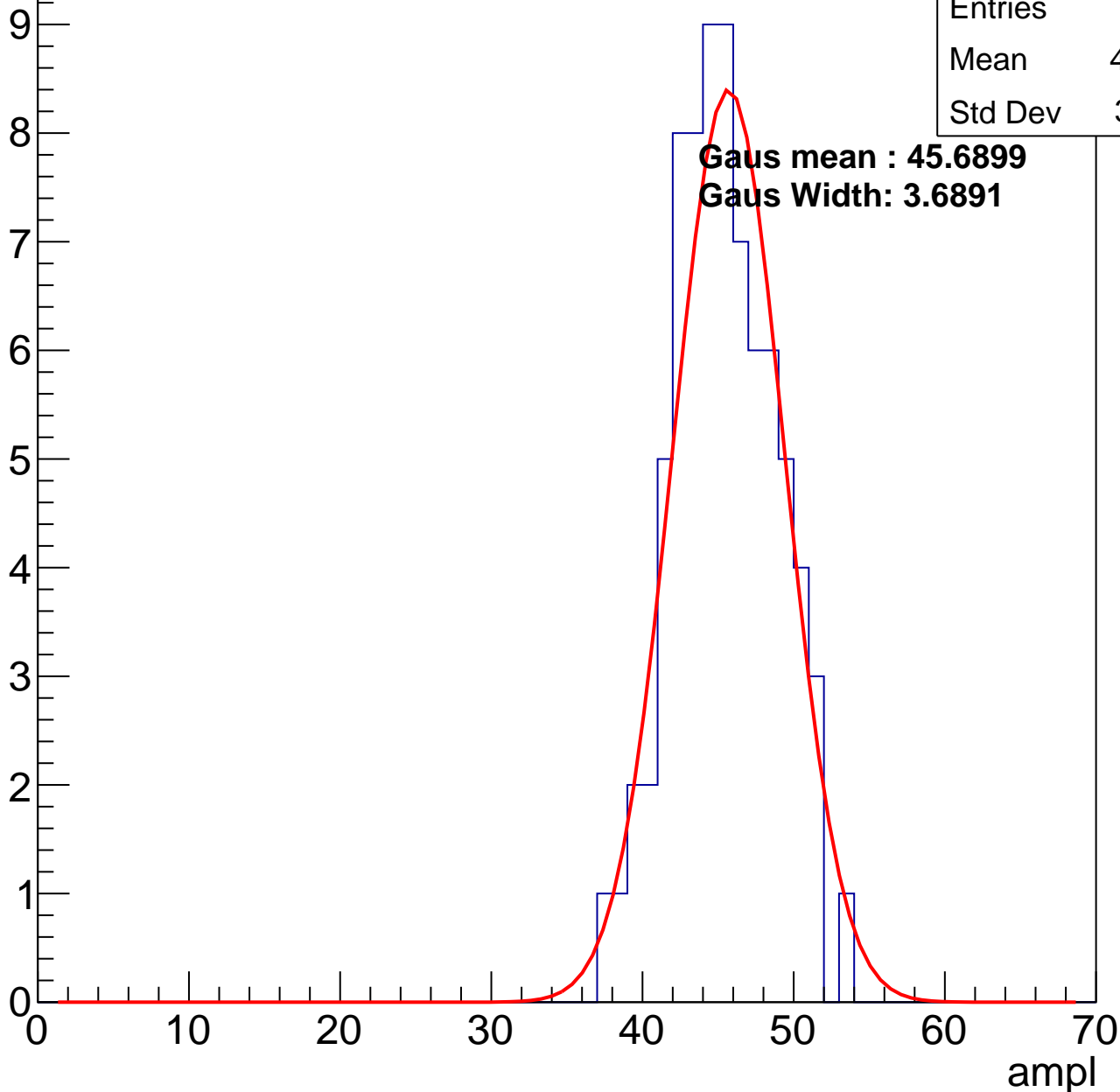
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	77
Mean	44.96
Std Dev	3.351

**Gaus mean : 45.6899**

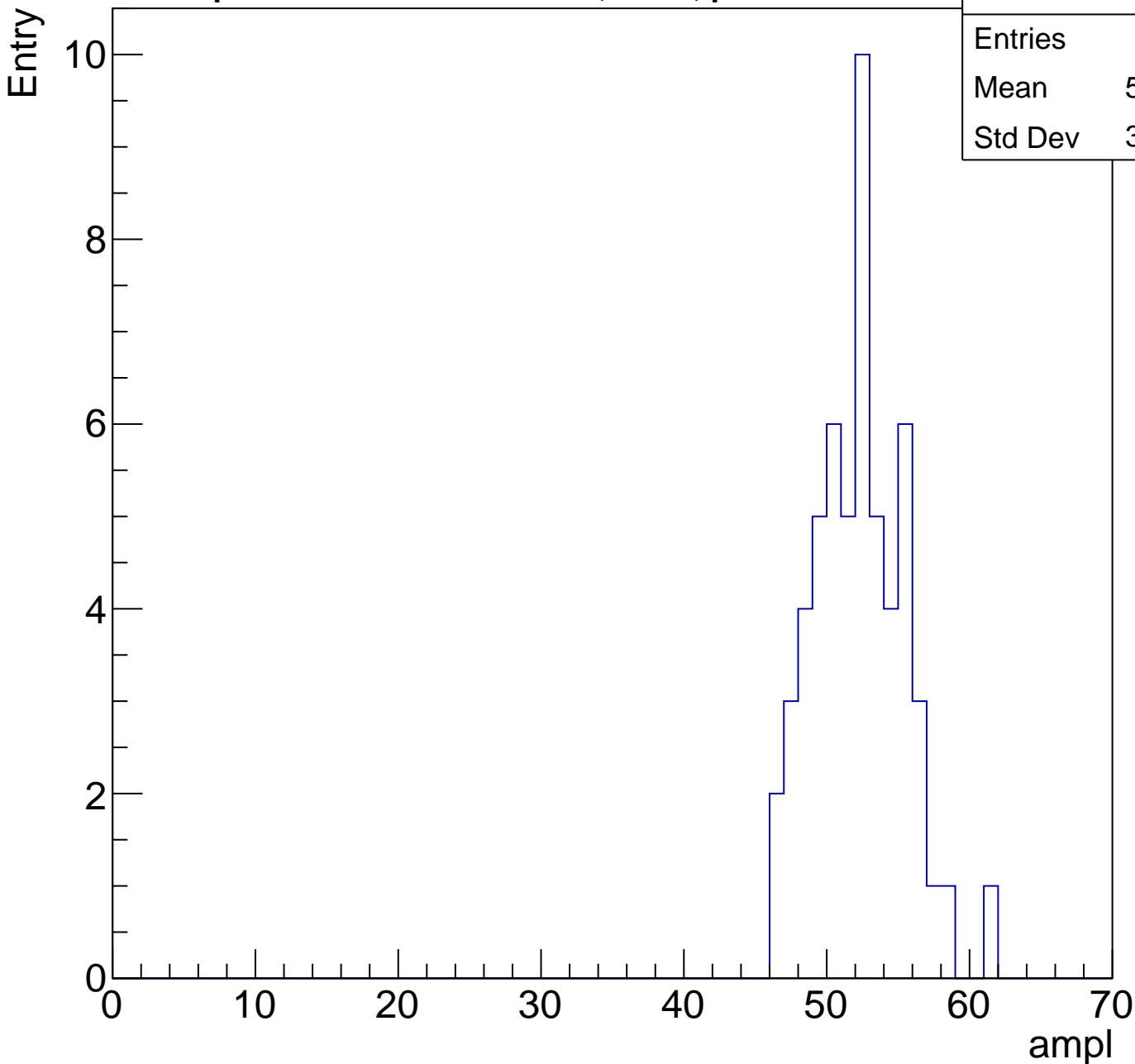
**Gaus Width: 3.6891**



# B0L000S, U7-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

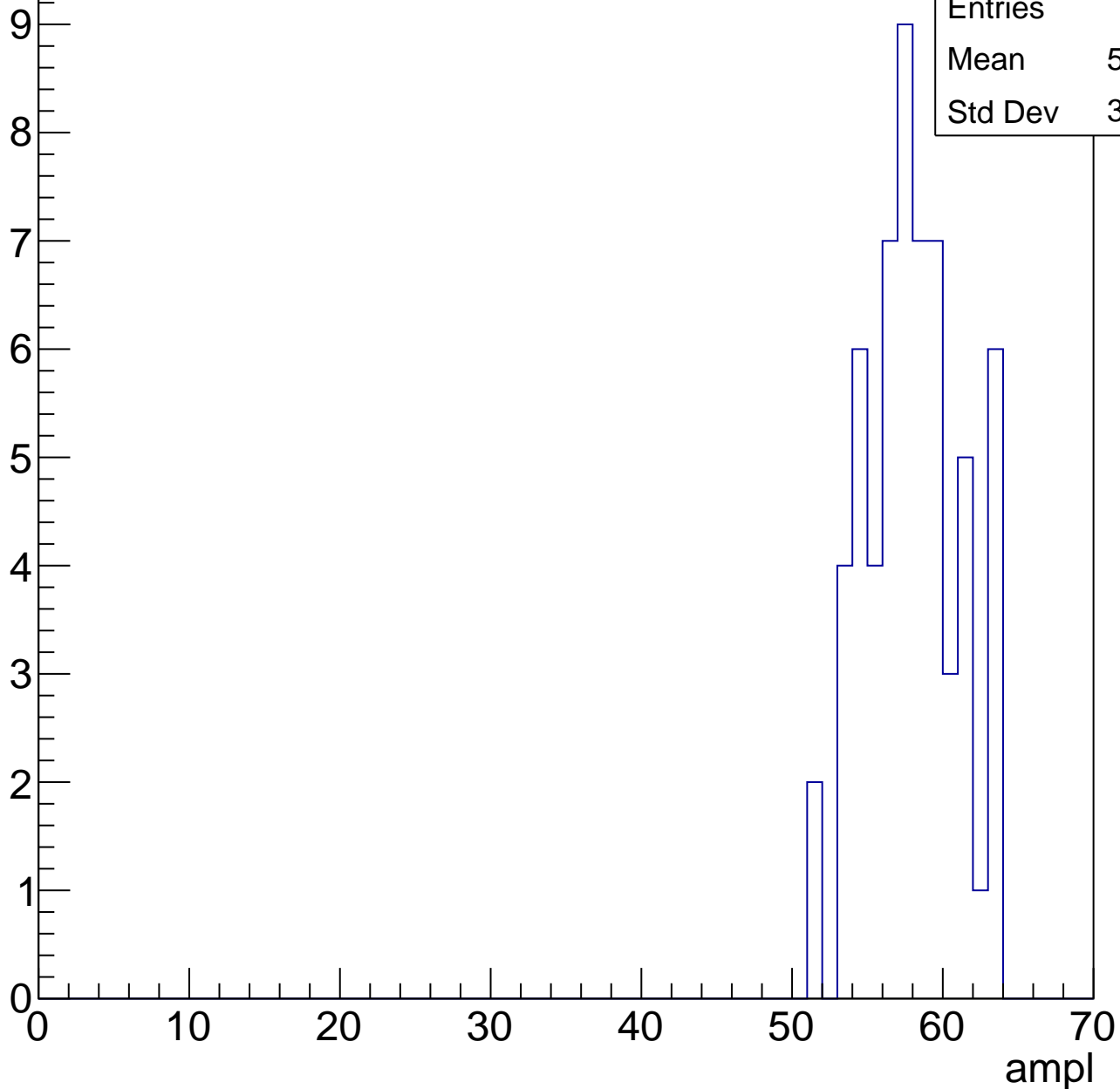
Entries	56
Mean	51.79
Std Dev	3.127



# B0L000S, U7-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

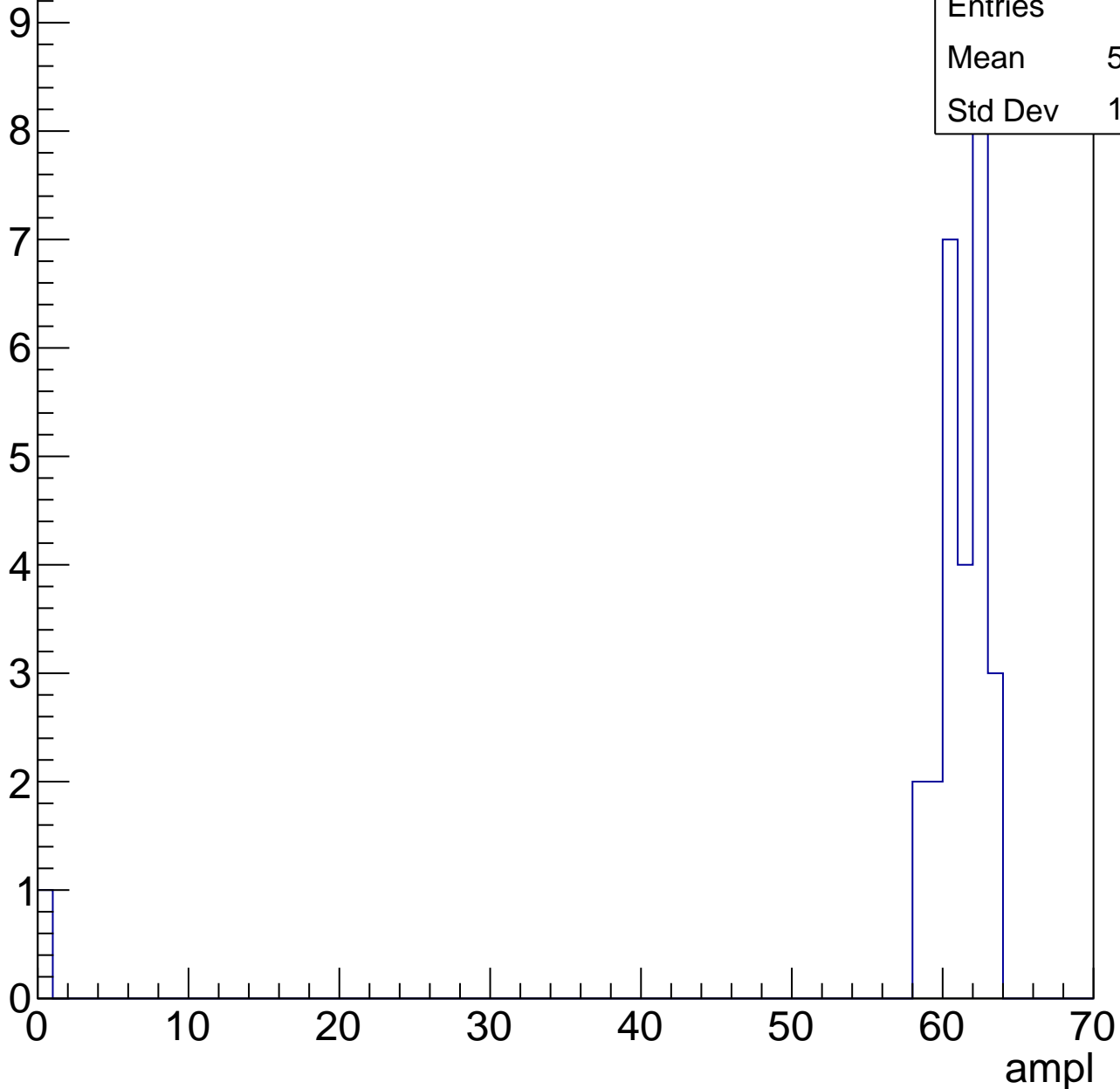


# B0L000S, U7-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	28
Mean	58.75
Std Dev	11.39



# B0L000S, U7-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

2

Mean

61

Std Dev

2



# B0L000S, U7-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	2
Mean	12.5
Std Dev	12.5

# B0L000S, U7-ch23, adc0

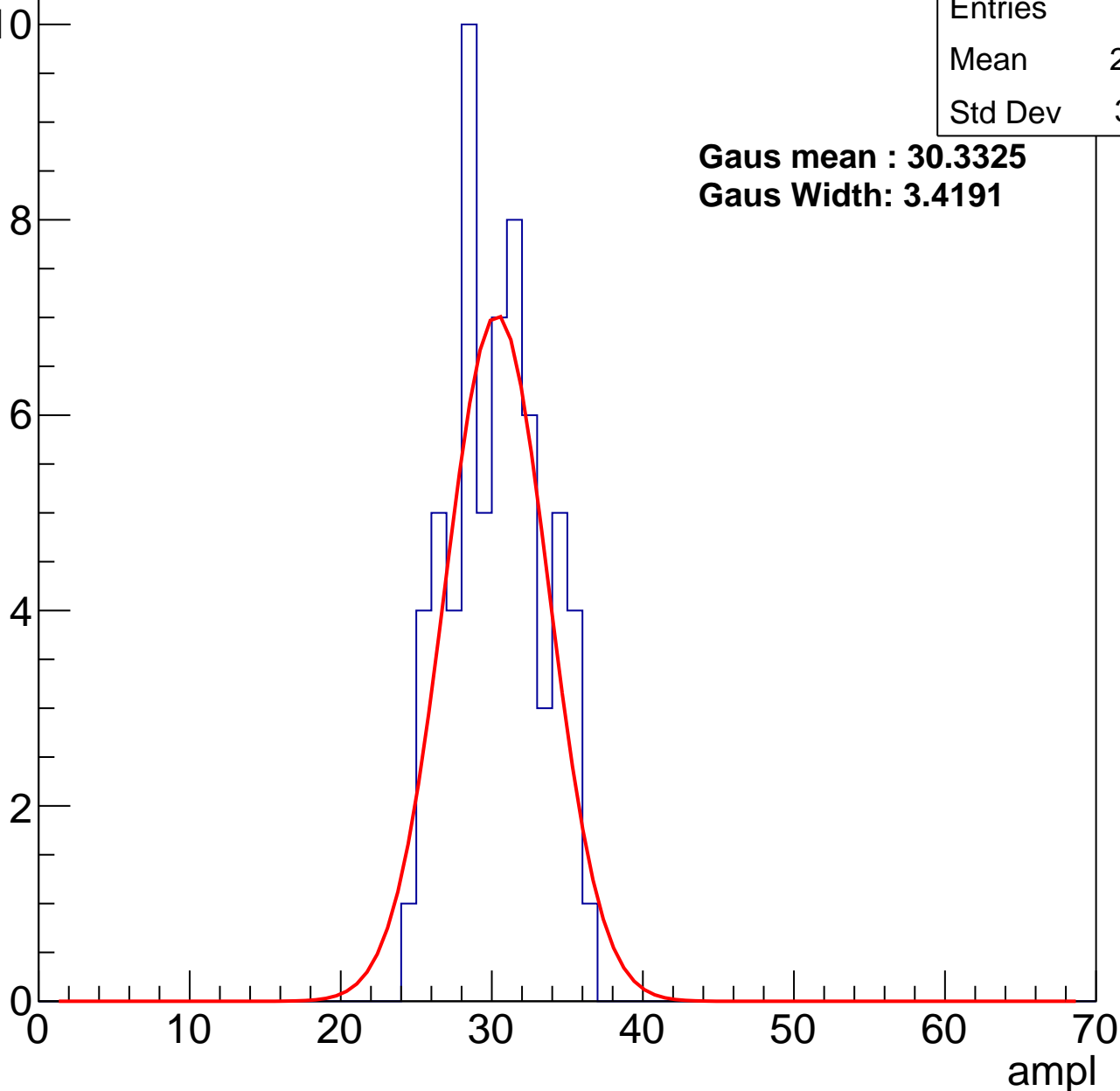
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	63
Mean	29.87
Std Dev	3.011

**Gaus mean : 30.3325**

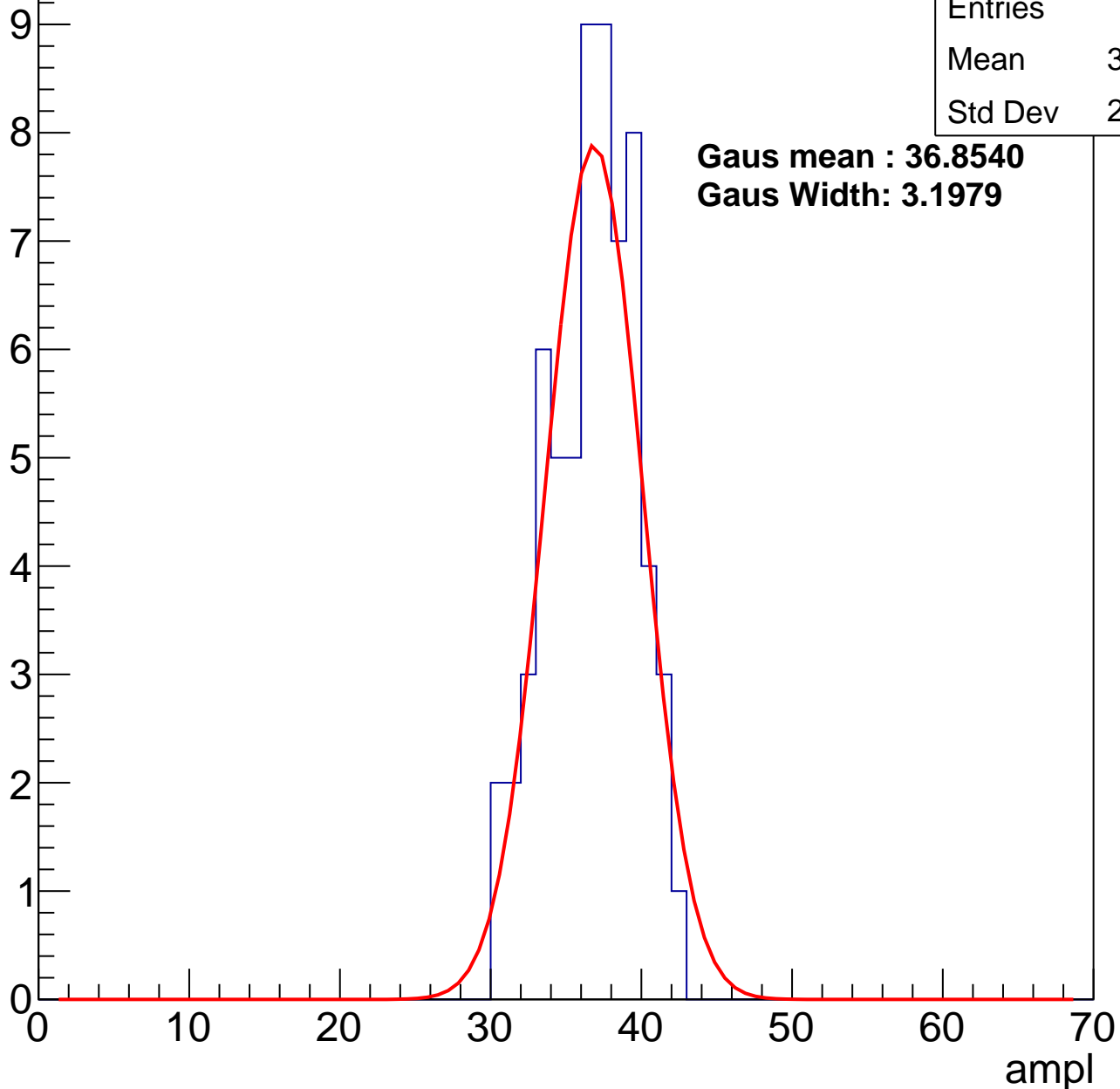
**Gaus Width: 3.4191**



# B0L000S, U7-ch23, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch23, adc2

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	83
Mean	43.86
Std Dev	3.279

**Gaus mean : 44.5188**

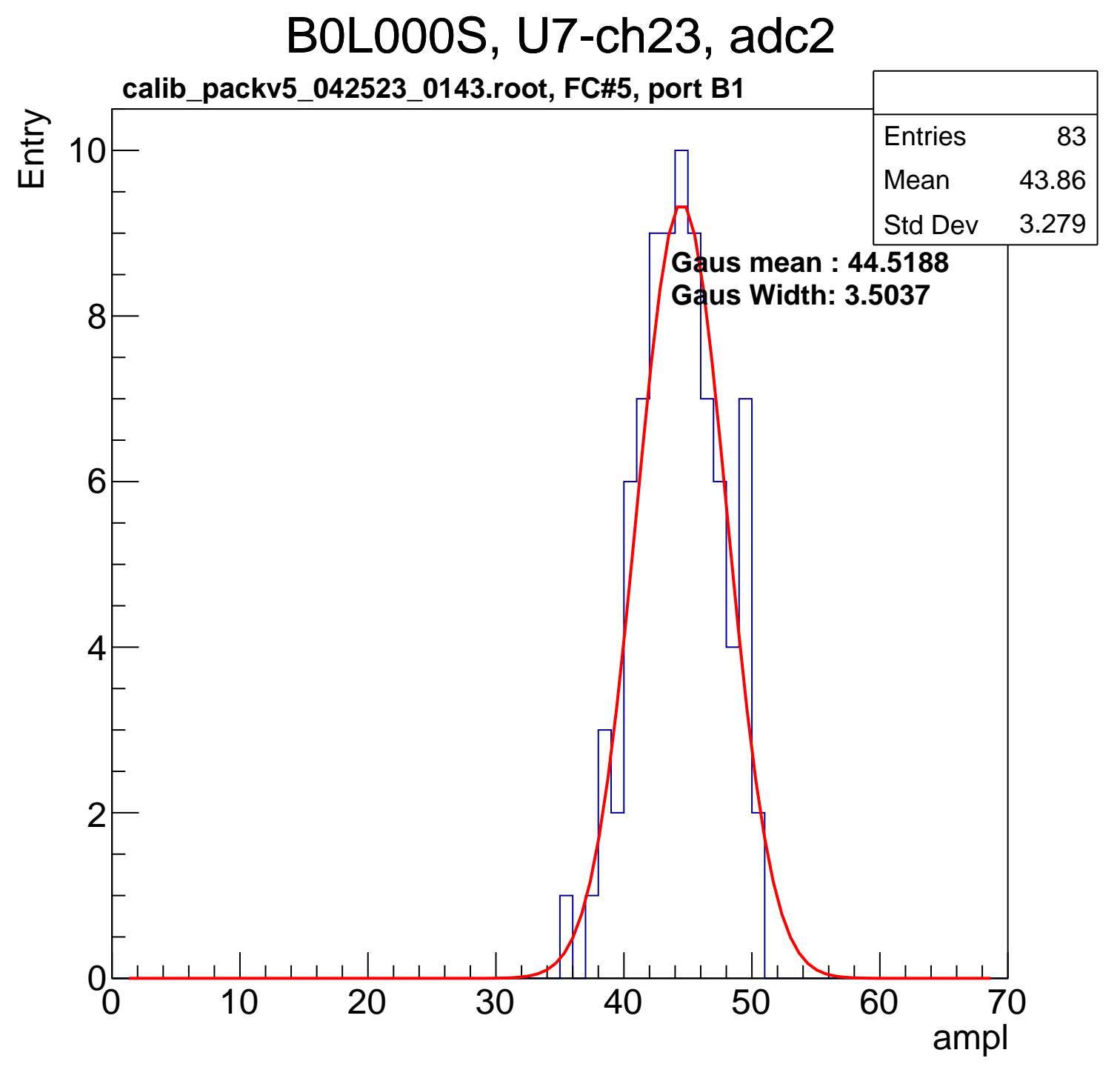
**Gaus Width: 3.5037**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

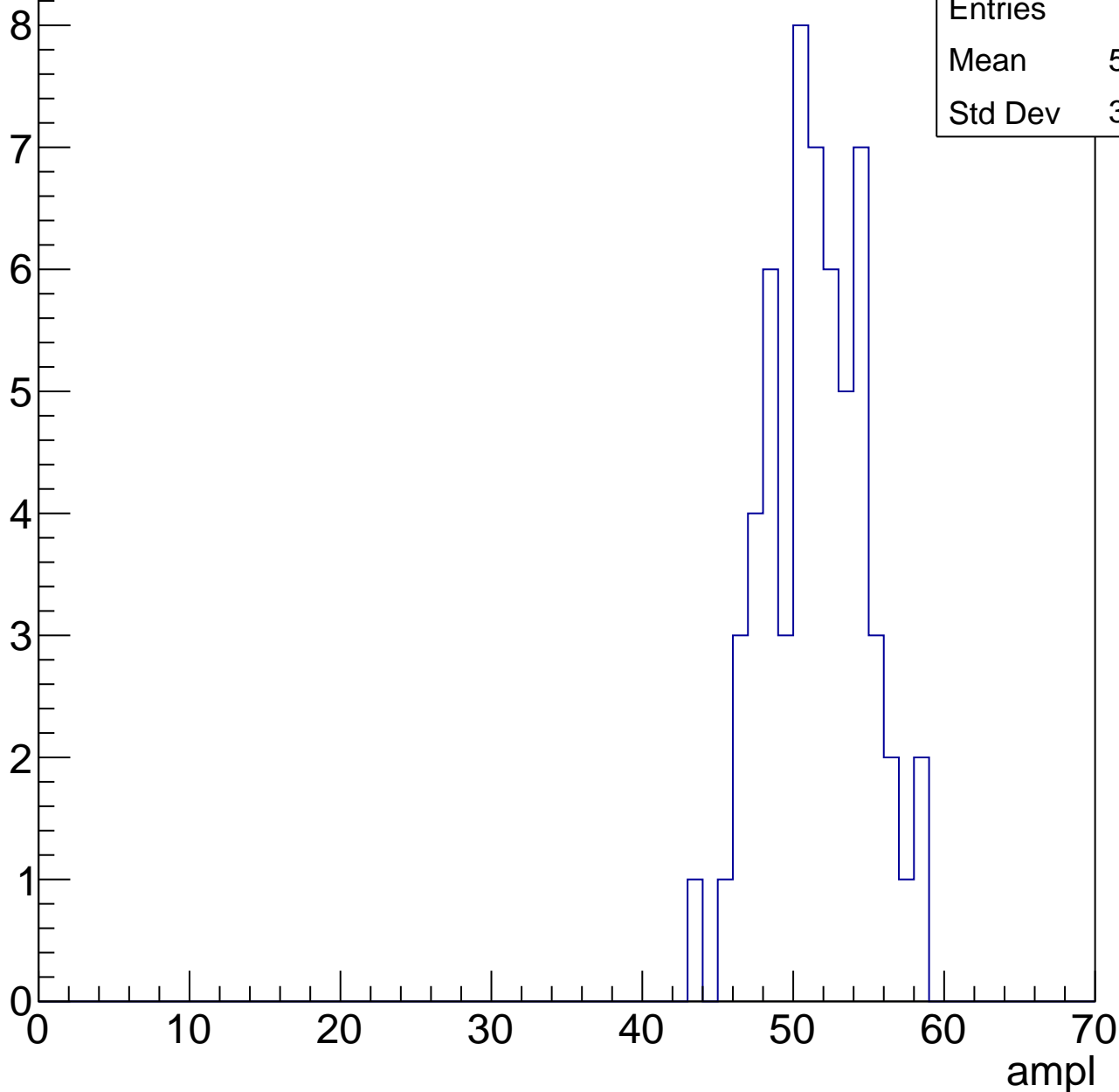


# B0L000S, U7-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	59
Mean	51.03
Std Dev	3.278



# B0L000S, U7-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

7

6

5

4

3

2

1

0

0

10

20

30

40

50

60

70

ampl

Entries	59
Mean	56.46
Std Dev	2.948

# B0L000S, U7-ch23, adc5

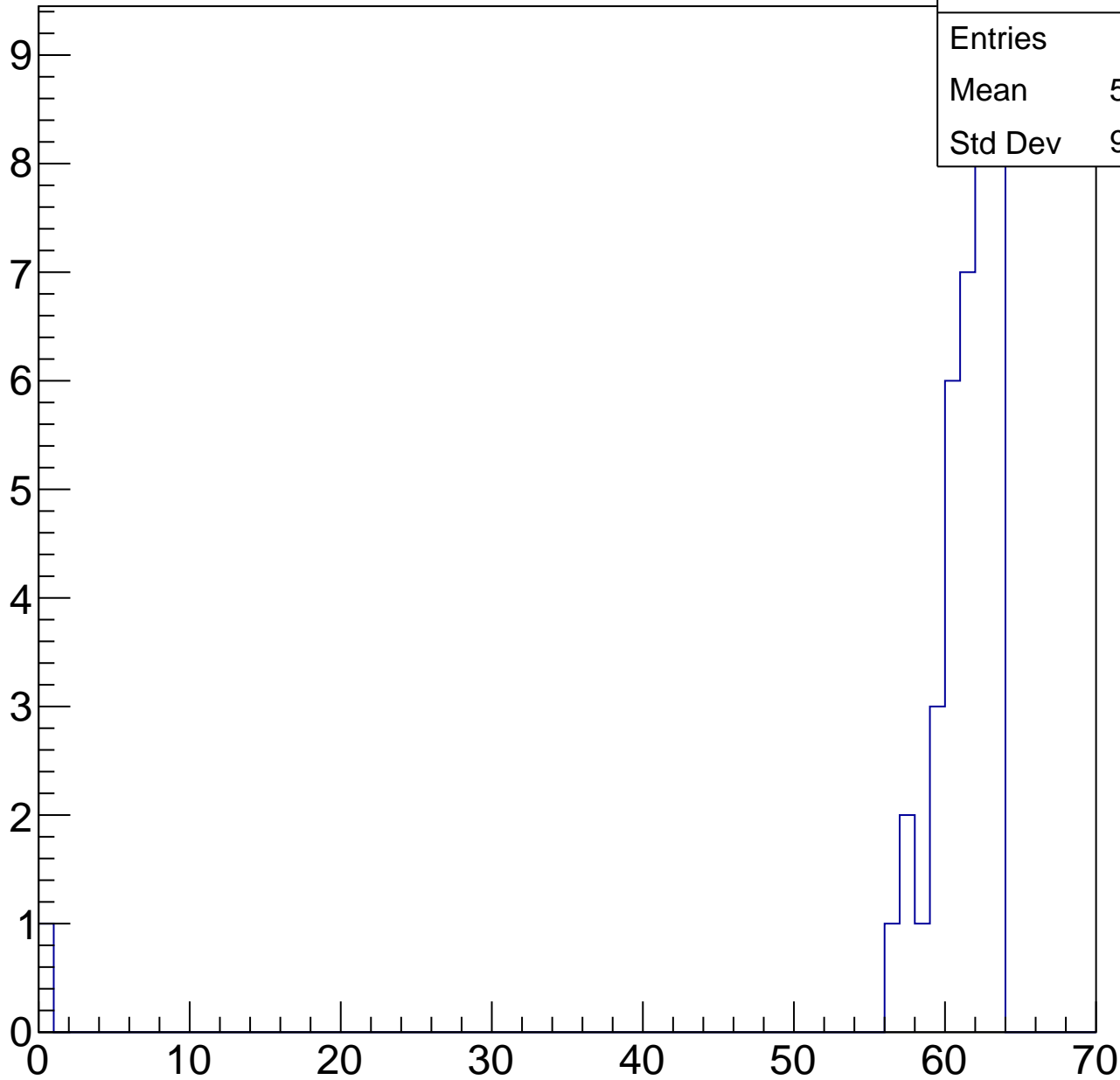
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	38
Mean	59.32
Std Dev	9.918

ampl



# B0L000S, U7-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	1
Mean	23
Std Dev	0

# B0L000S, U7-ch24, adc0

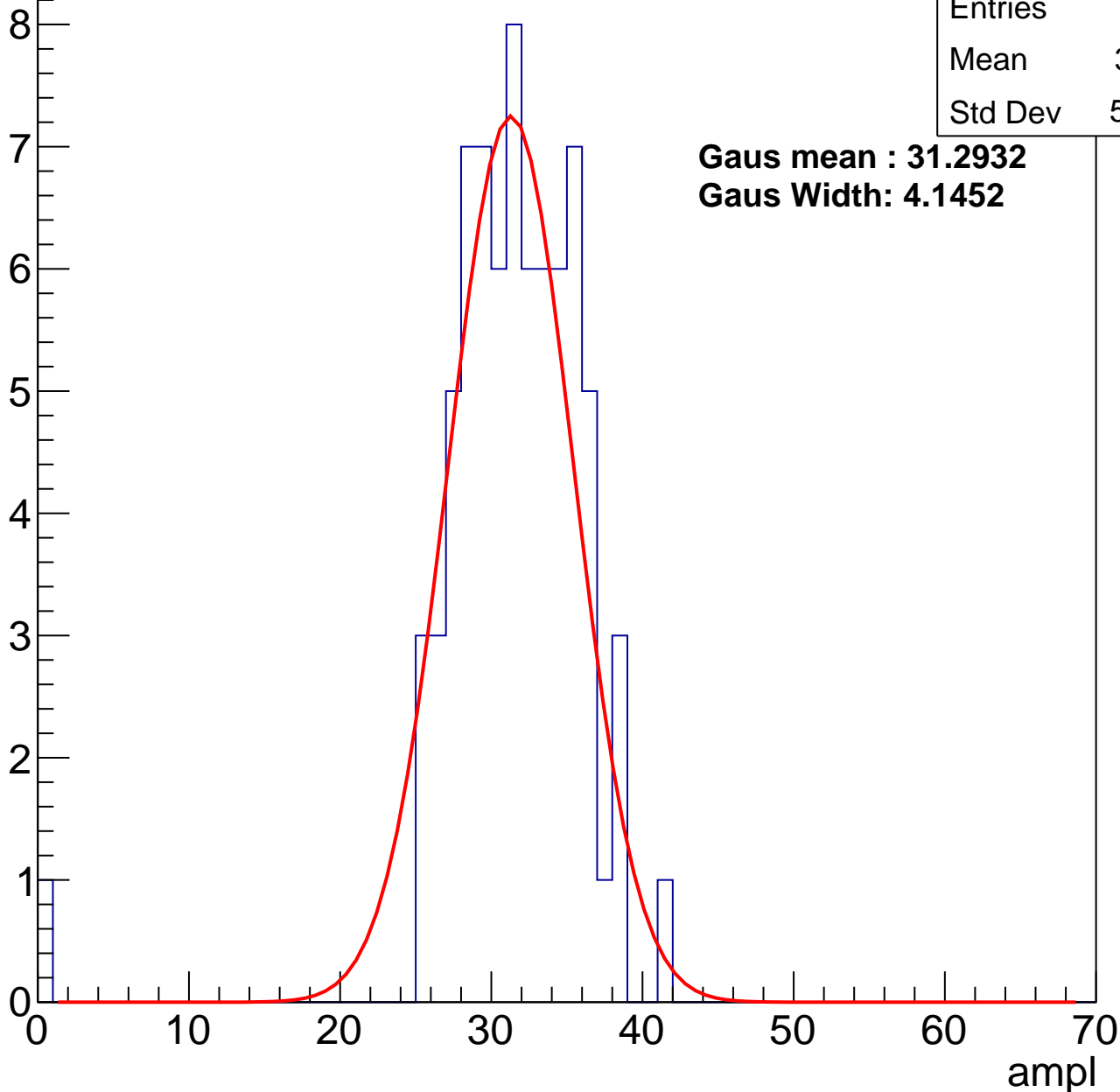
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	75
Mean	31.01
Std Dev	5.066

**Gaus mean : 31.2932**

**Gaus Width: 4.1452**



# B0L000S, U7-ch24, adc1

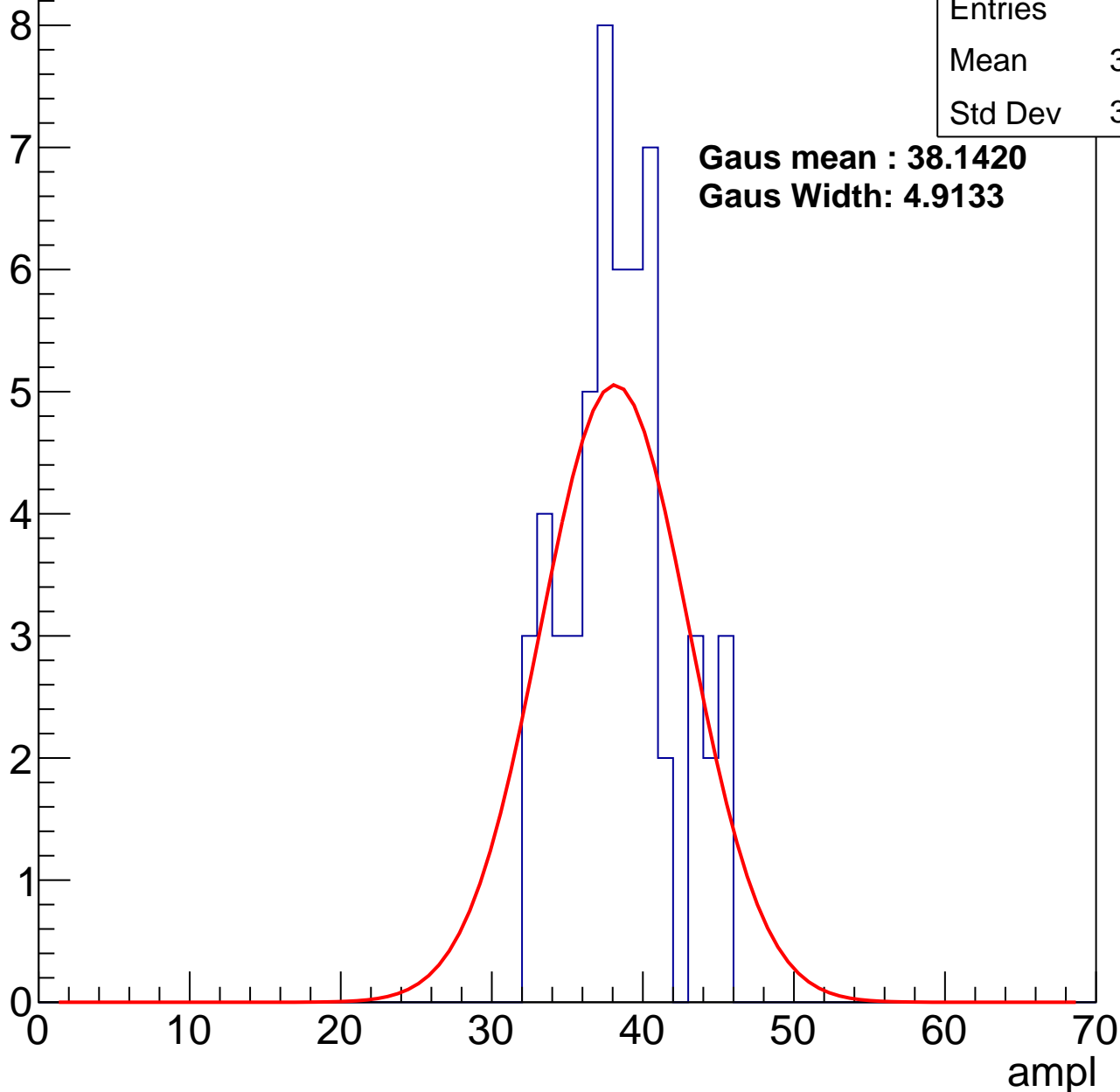
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	55
Mean	37.95
Std Dev	3.456

**Gaus mean : 38.1420**

**Gaus Width: 4.9133**



# B0L000S, U7-ch24, adc2

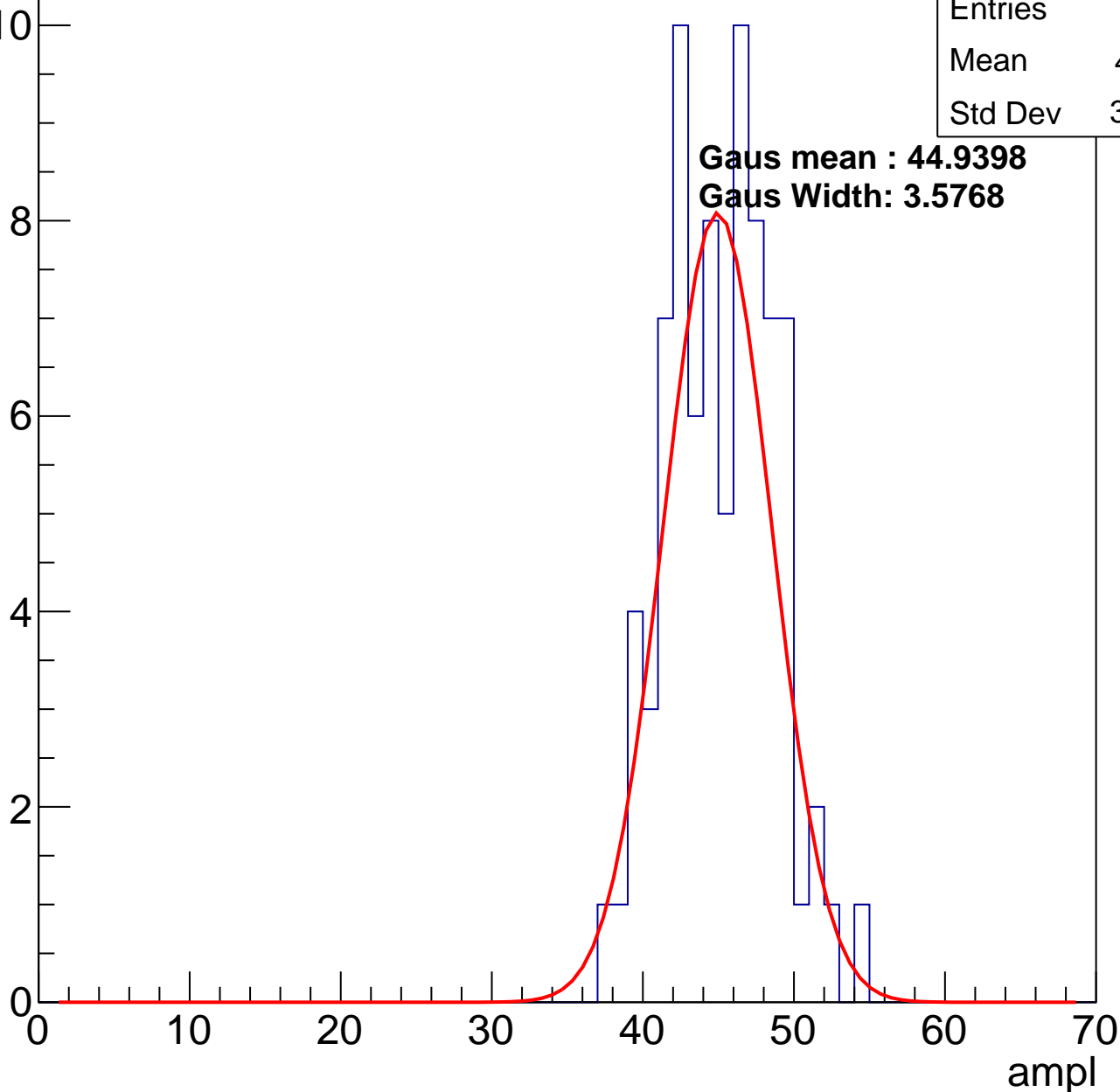
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	82
Mean	44.71
Std Dev	3.497

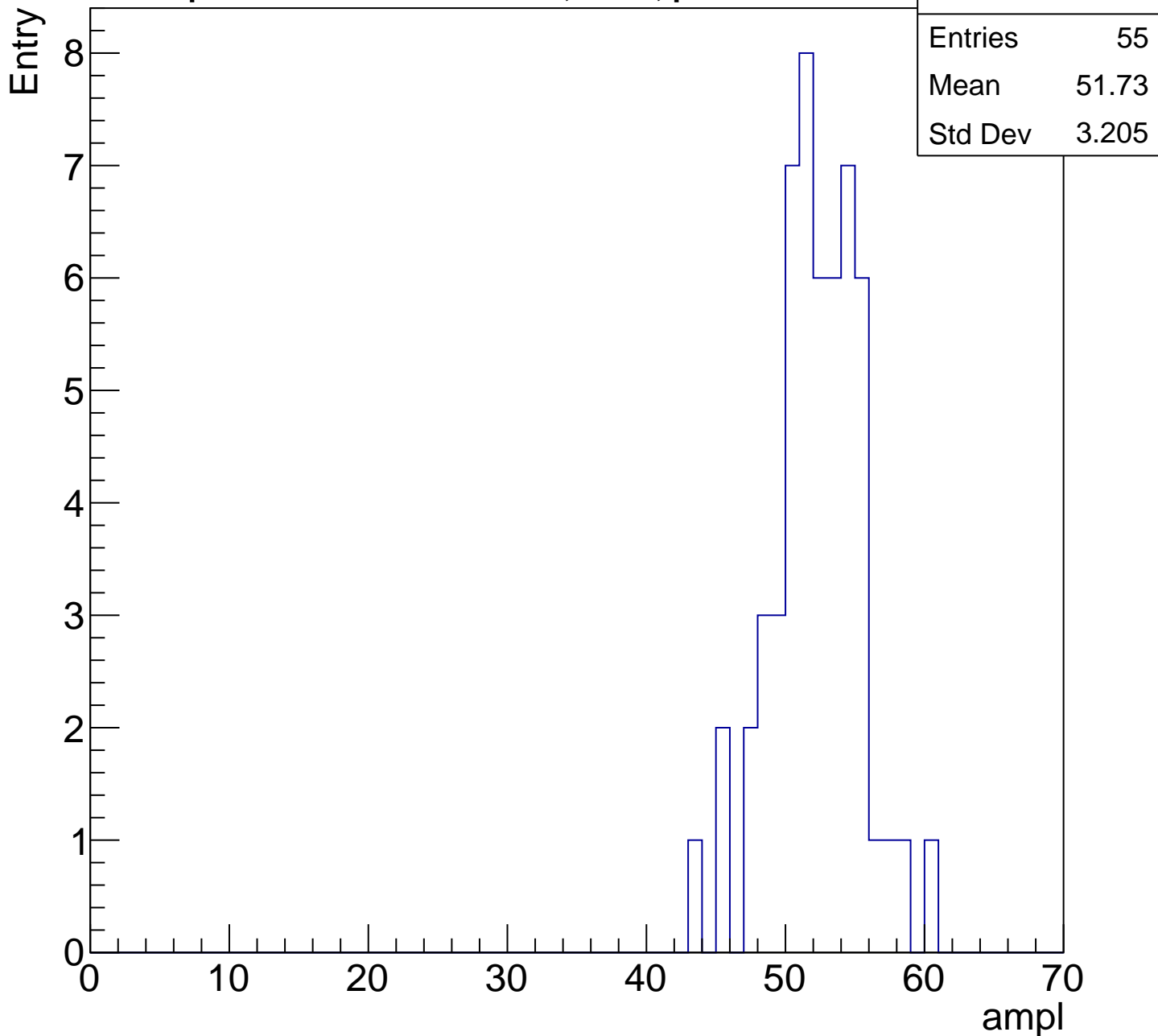
**Gaus mean : 44.9398**

**Gaus Width: 3.5768**



# B0L000S, U7-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

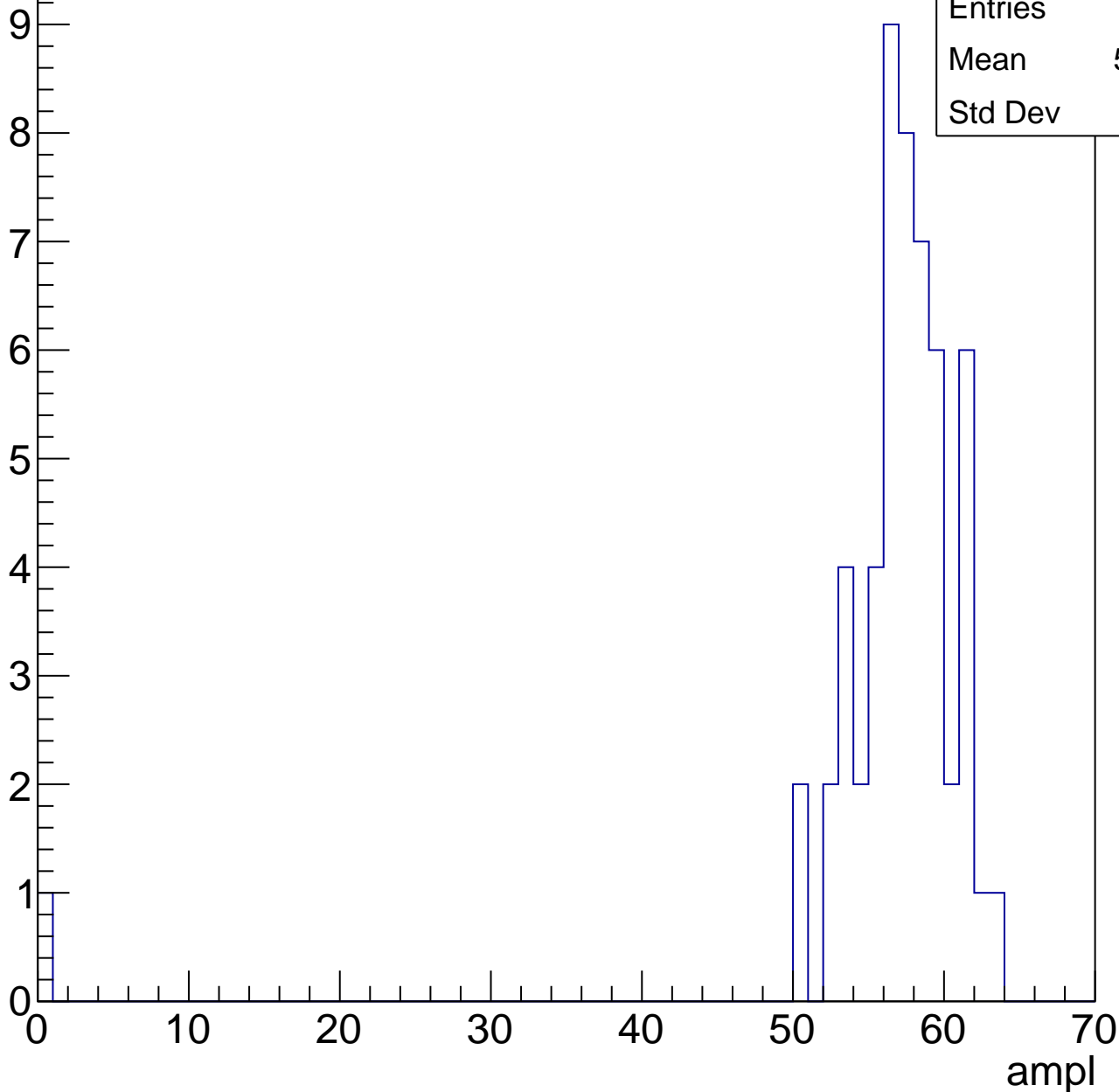


# B0L000S, U7-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	55
Mean	55.91
Std Dev	8.14

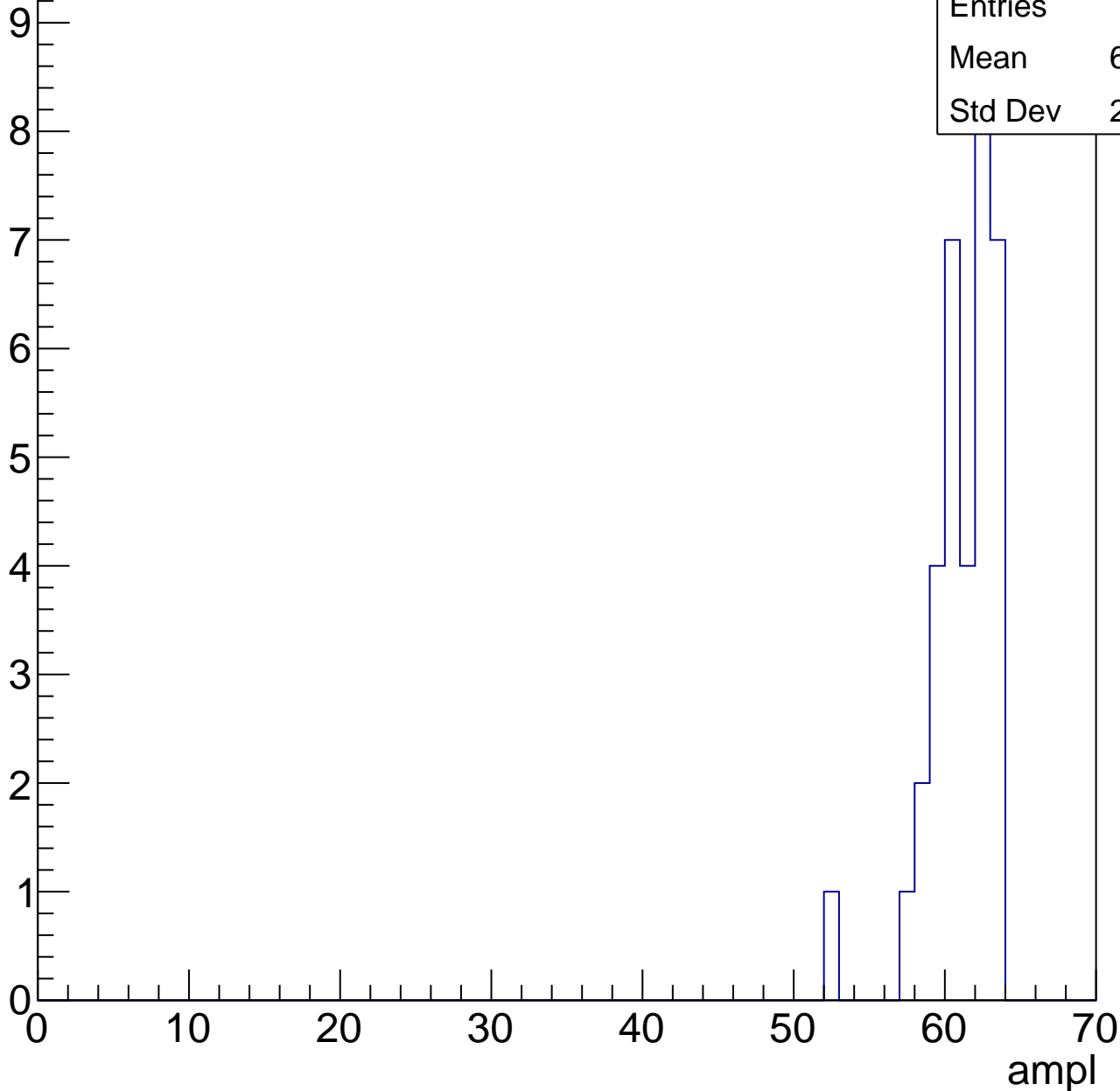


# B0L000S, U7-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	35
Mean	60.69
Std Dev	2.214



# B0L000S, U7-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L000S, U7-ch25, adc0

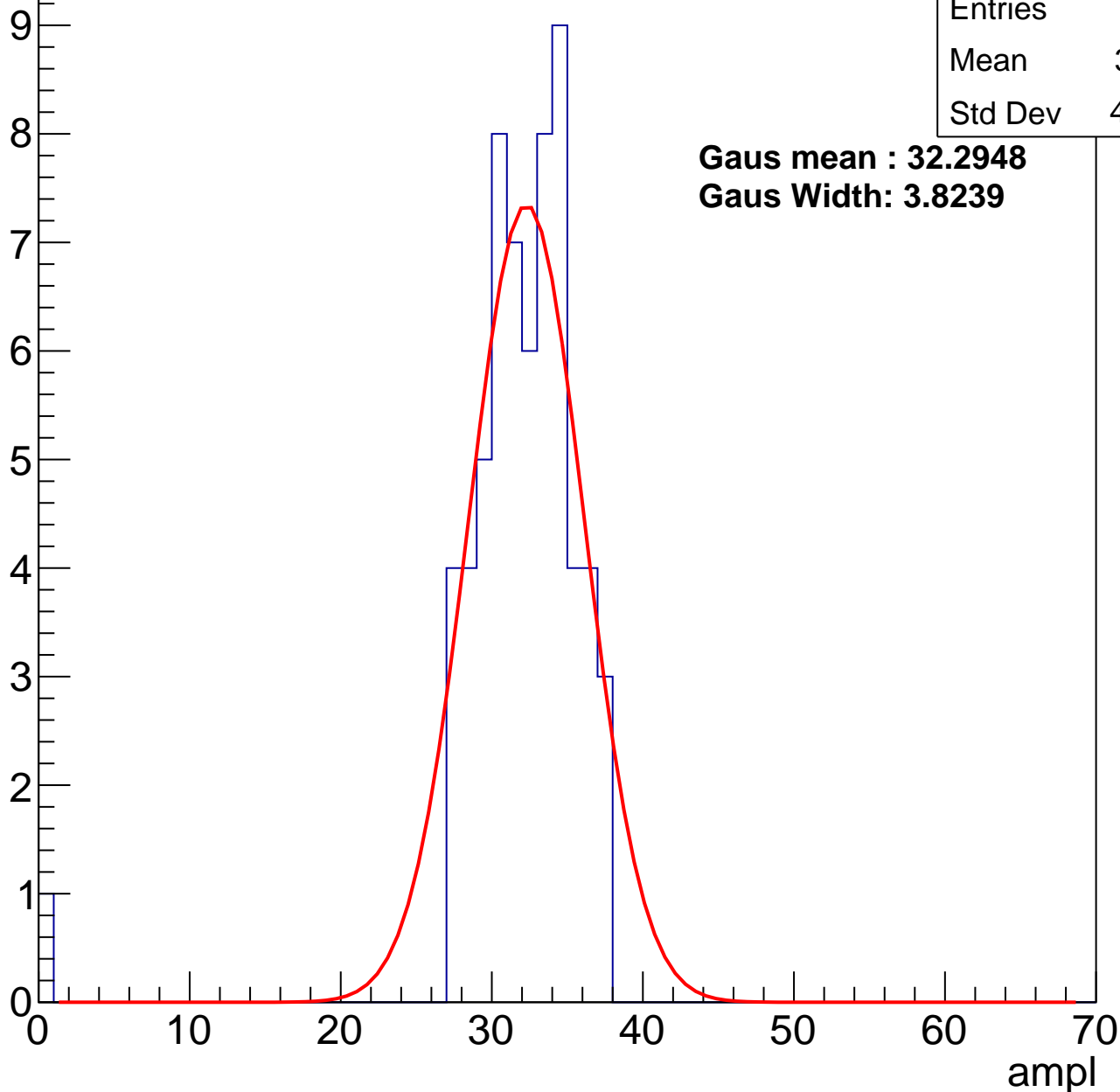
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	63
Mean	31.41
Std Dev	4.829

**Gaus mean : 32.2948**

**Gaus Width: 3.8239**



# B0L000S, U7-ch25, adc1

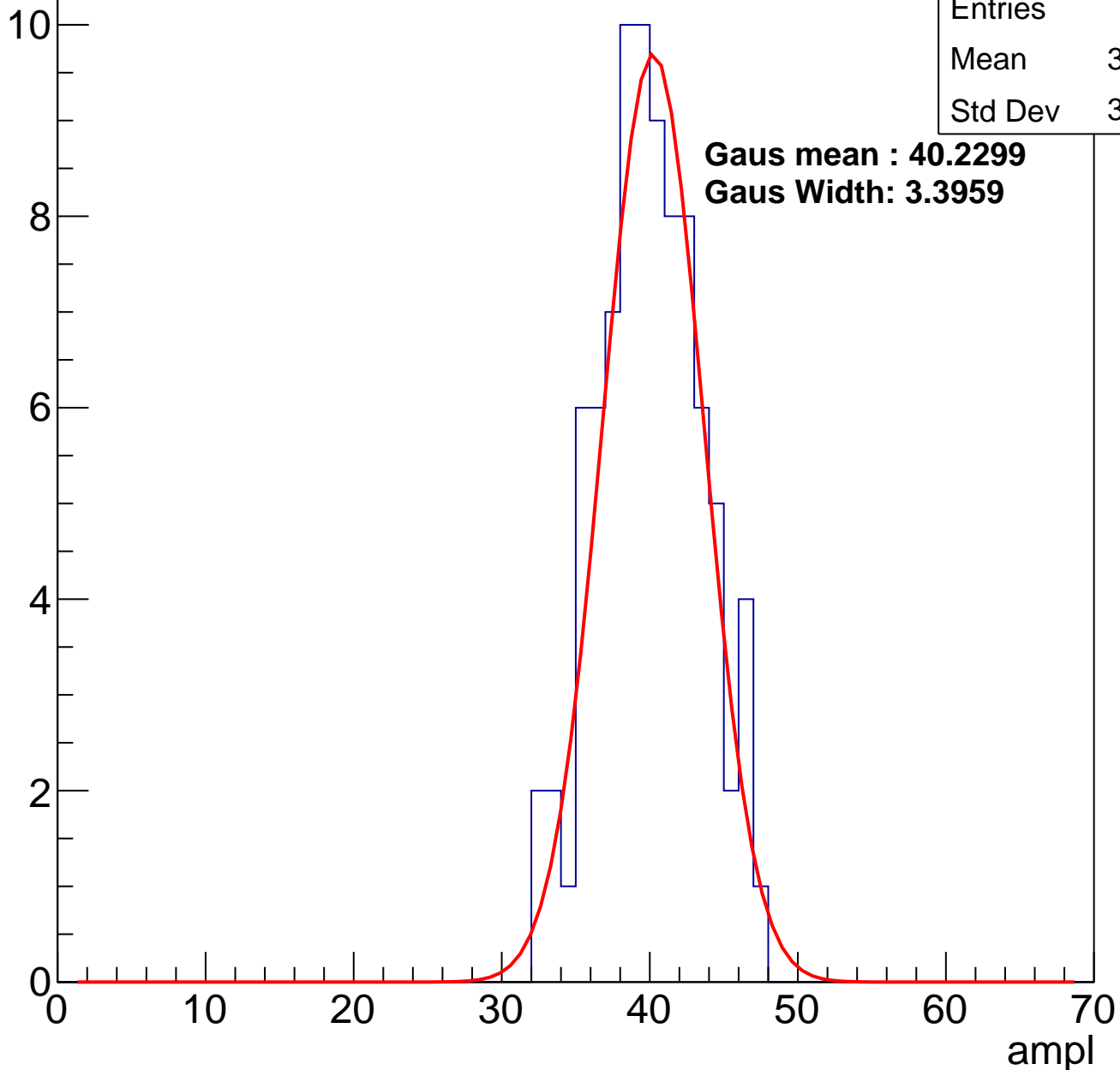
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	87
Mean	39.56
Std Dev	3.426

**Gaus mean : 40.2299**

**Gaus Width: 3.3959**

Entry



# B0L000S, U7-ch25, adc2

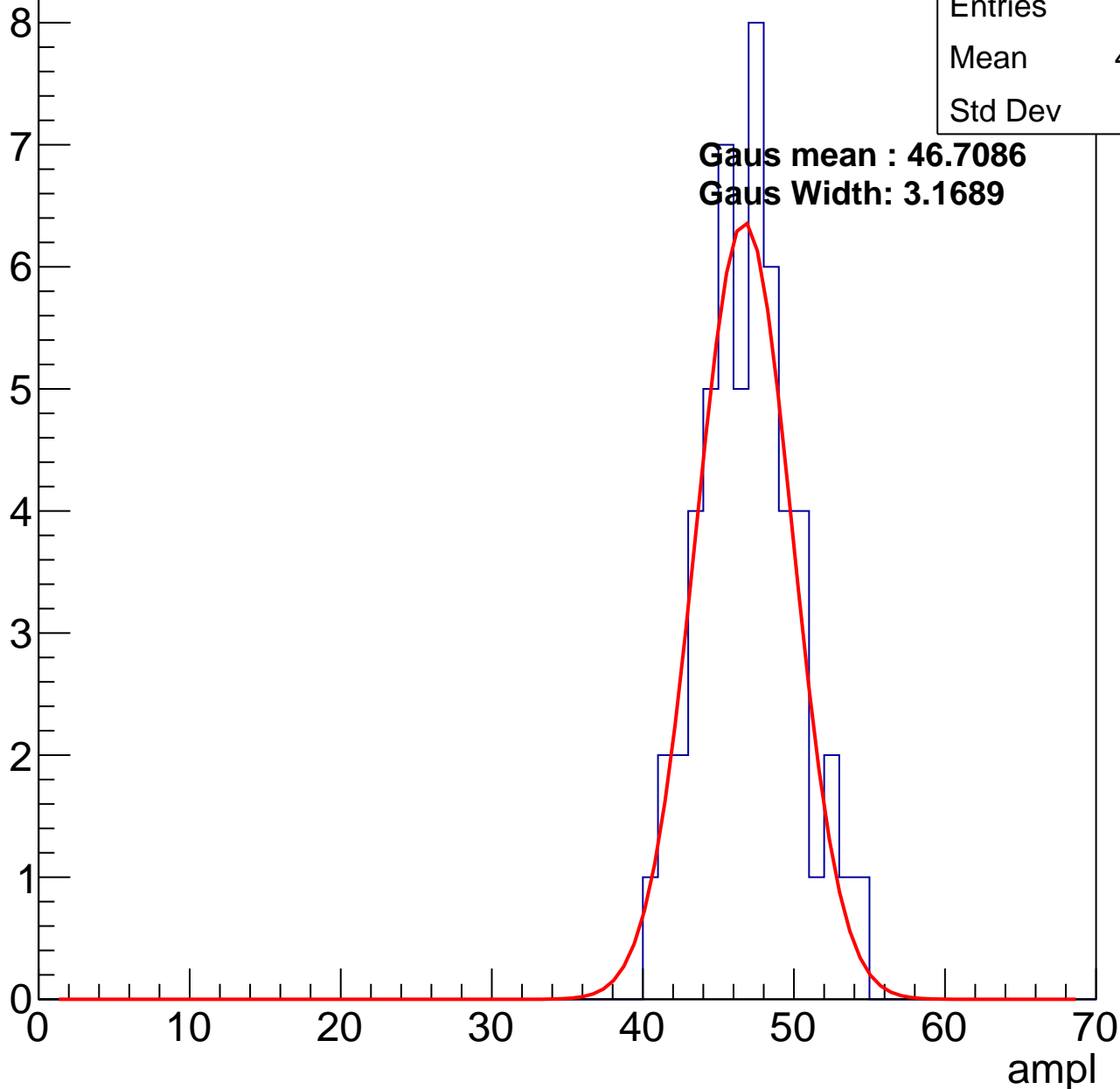
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	53
Mean	46.51
Std Dev	3.1

**Gaus mean : 46.7086**

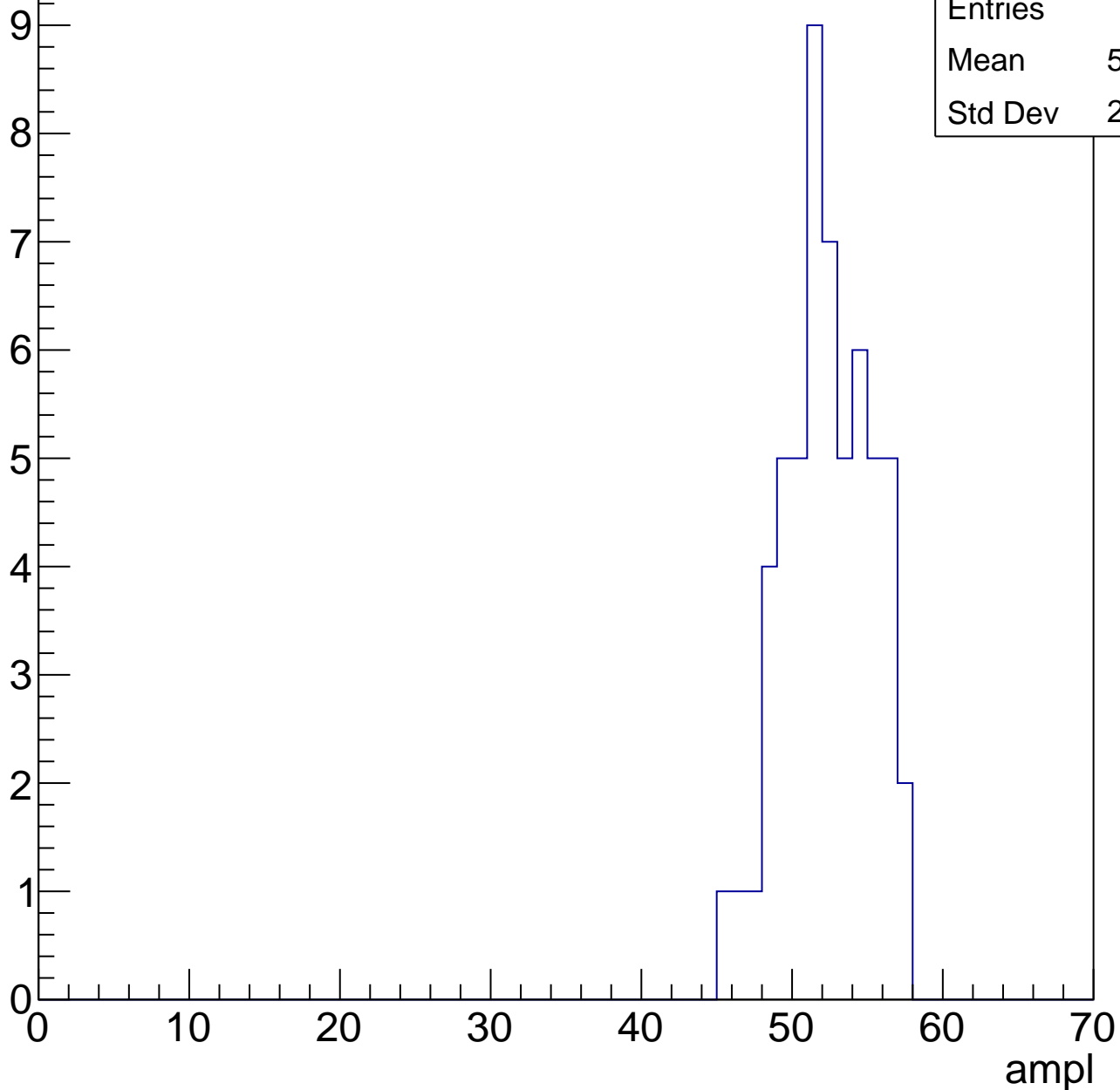
**Gaus Width: 3.1689**



# B0L000S, U7-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

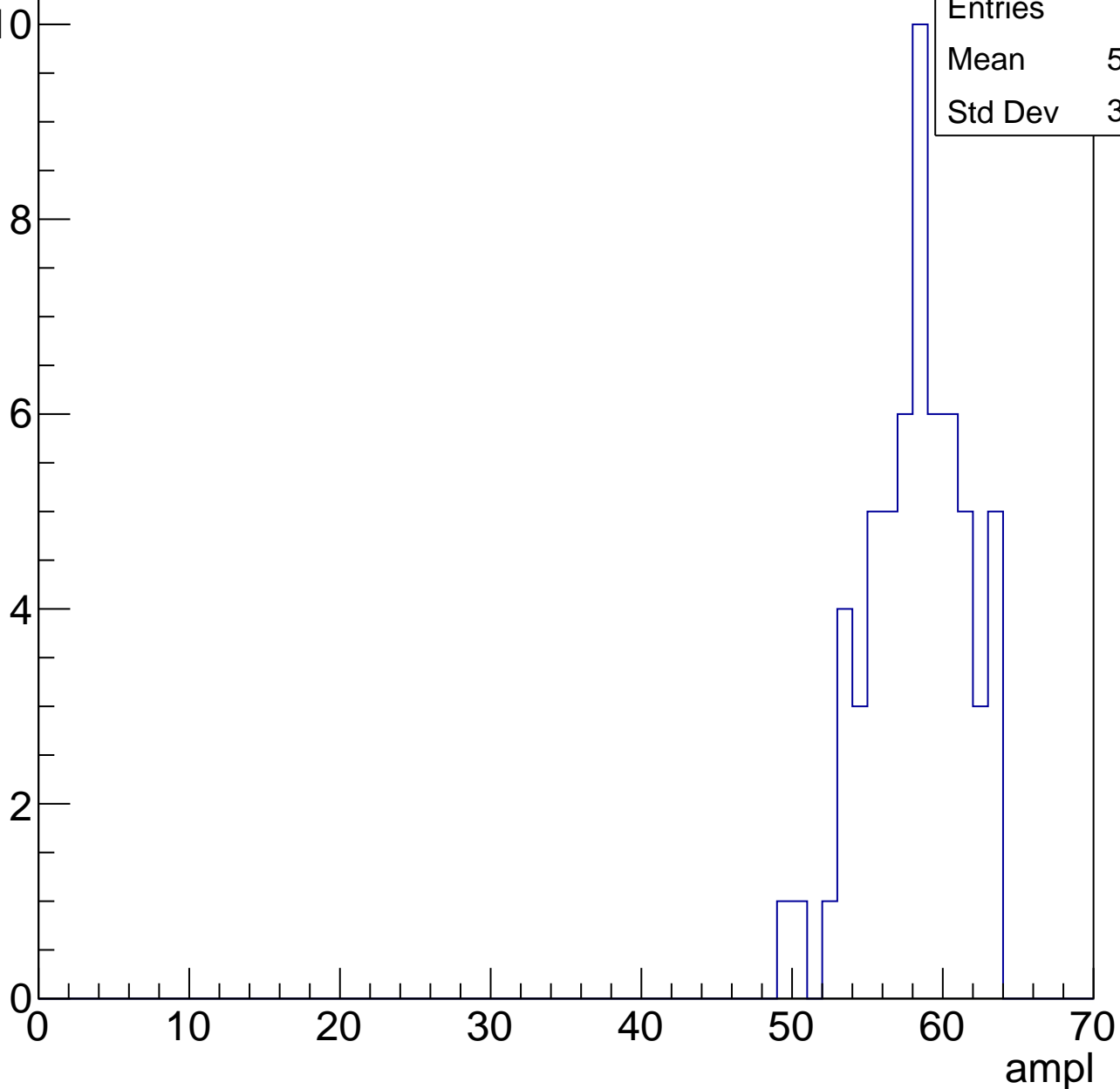


# B0L000S, U7-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	61
Mean	57.74
Std Dev	3.249

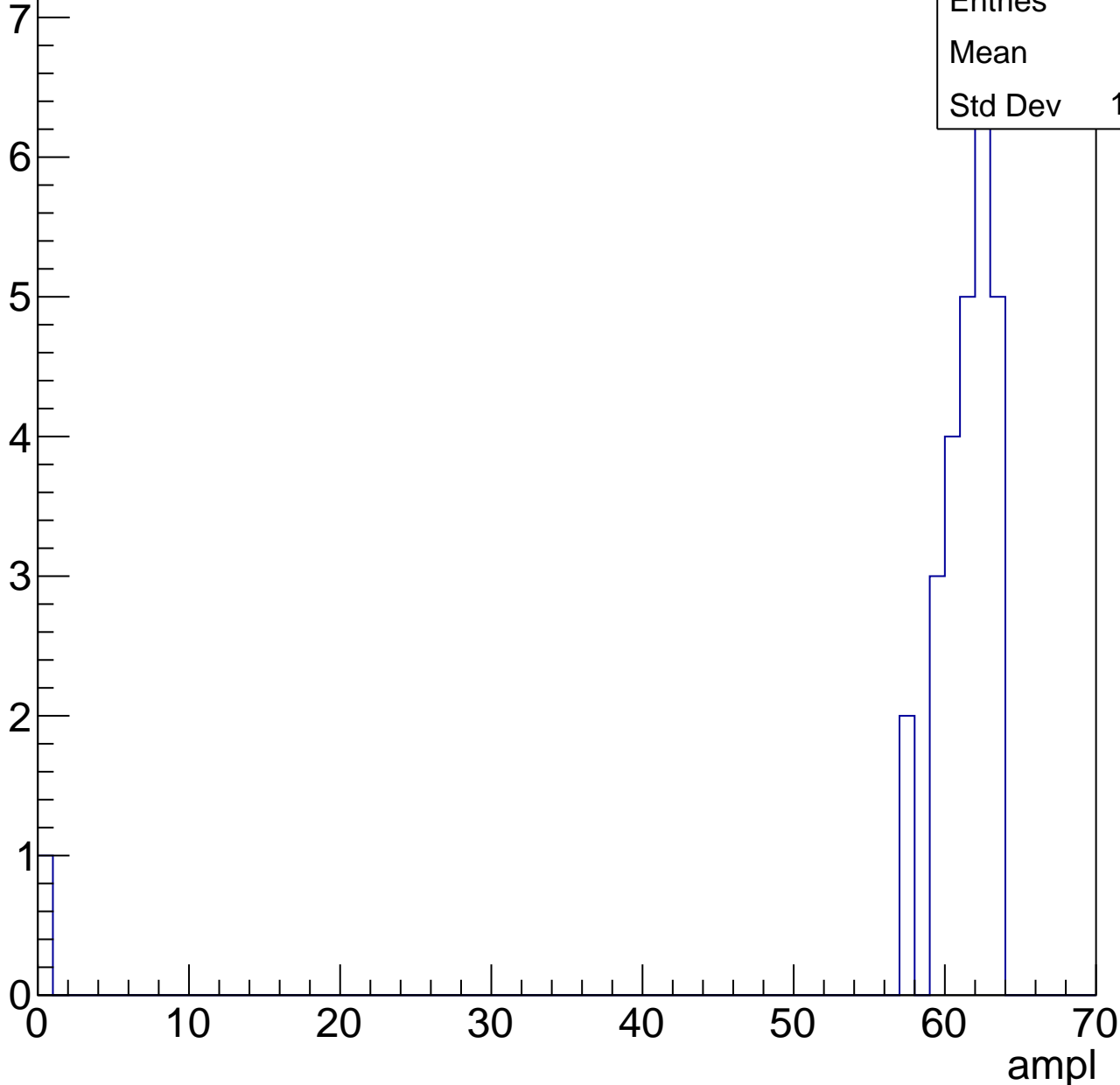


# B0L000S, U7-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

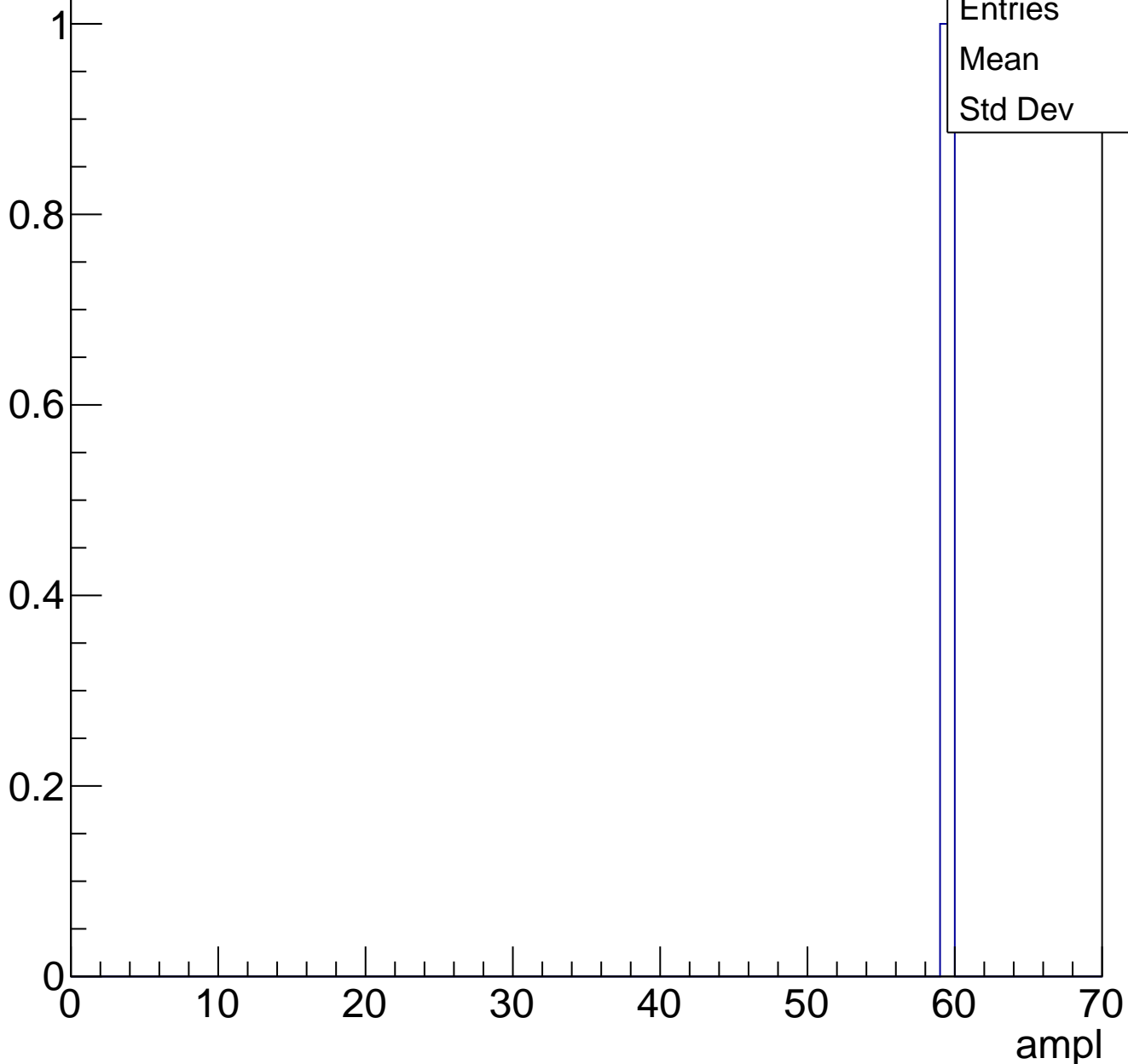
Entries	27
Mean	58.7
Std Dev	11.63



# B0L000S, U7-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

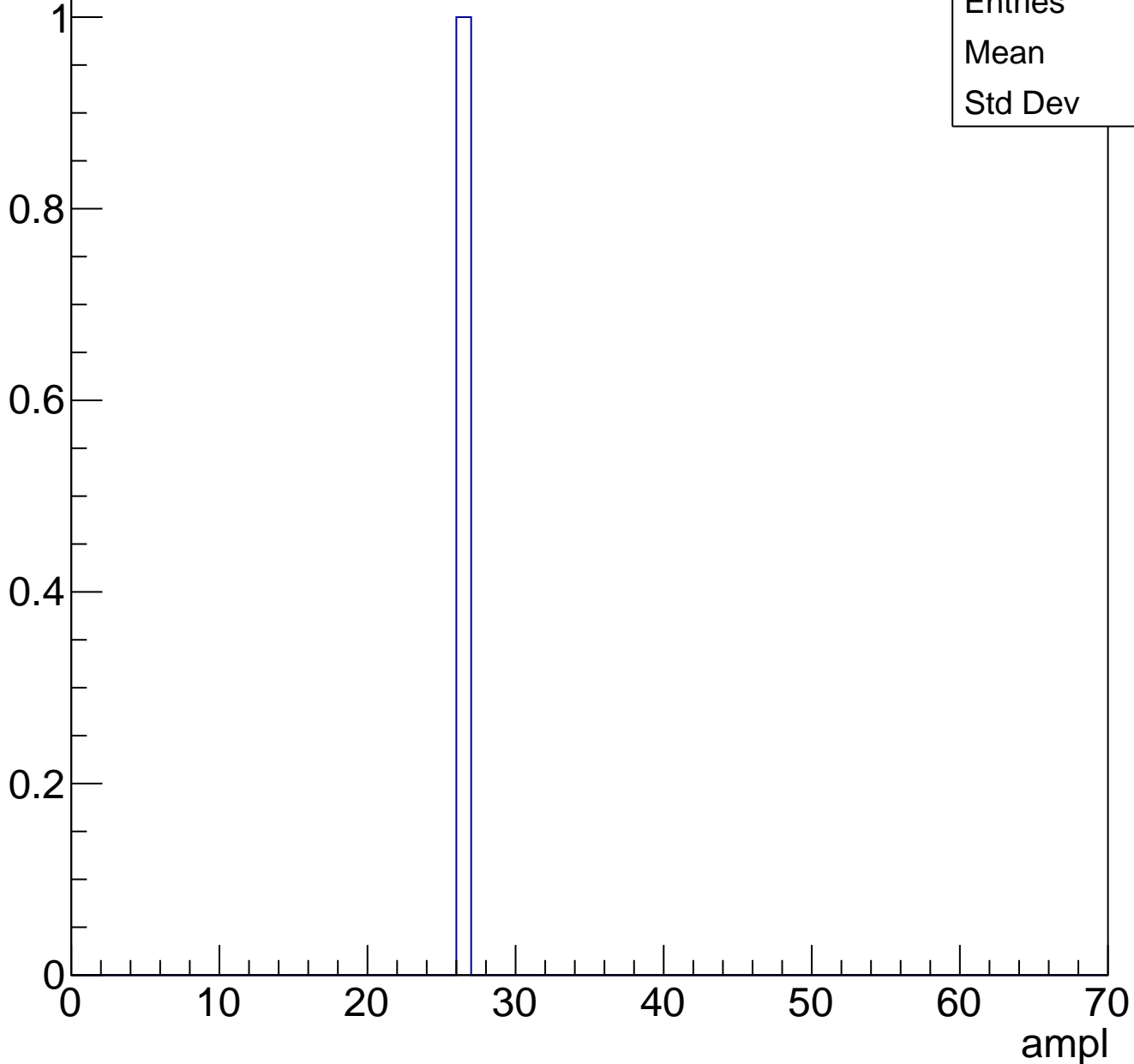




# B0L000S, U7-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	1
Mean	26
Std Dev	0

# B0L000S, U7-ch26, adc0

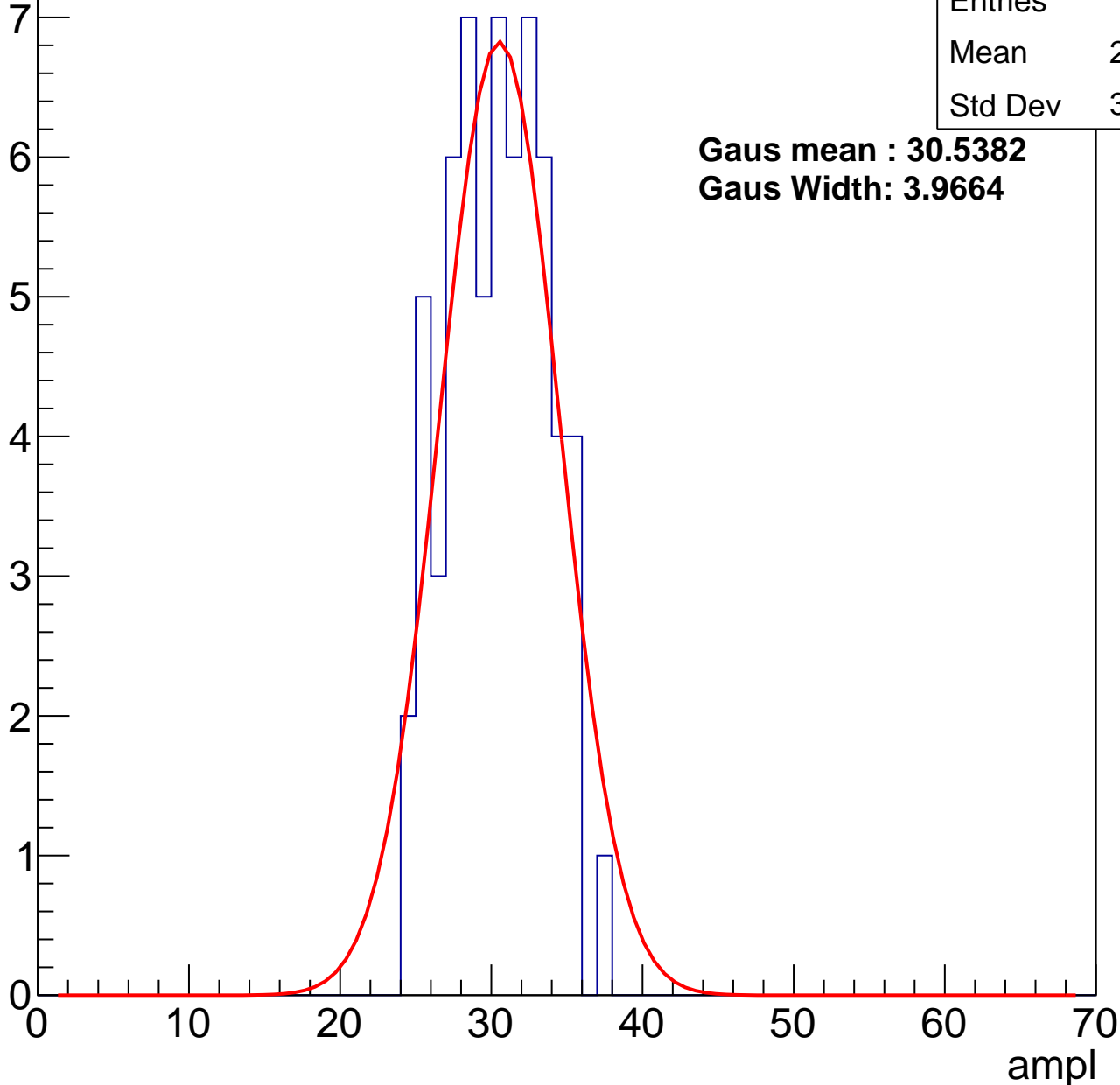
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	63
Mean	29.92
Std Dev	3.169

**Gaus mean : 30.5382**

**Gaus Width: 3.9664**



# B0L000S, U7-ch26, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	75
Mean	36.91
Std Dev	3.379

**Gaus mean : 37.7830**

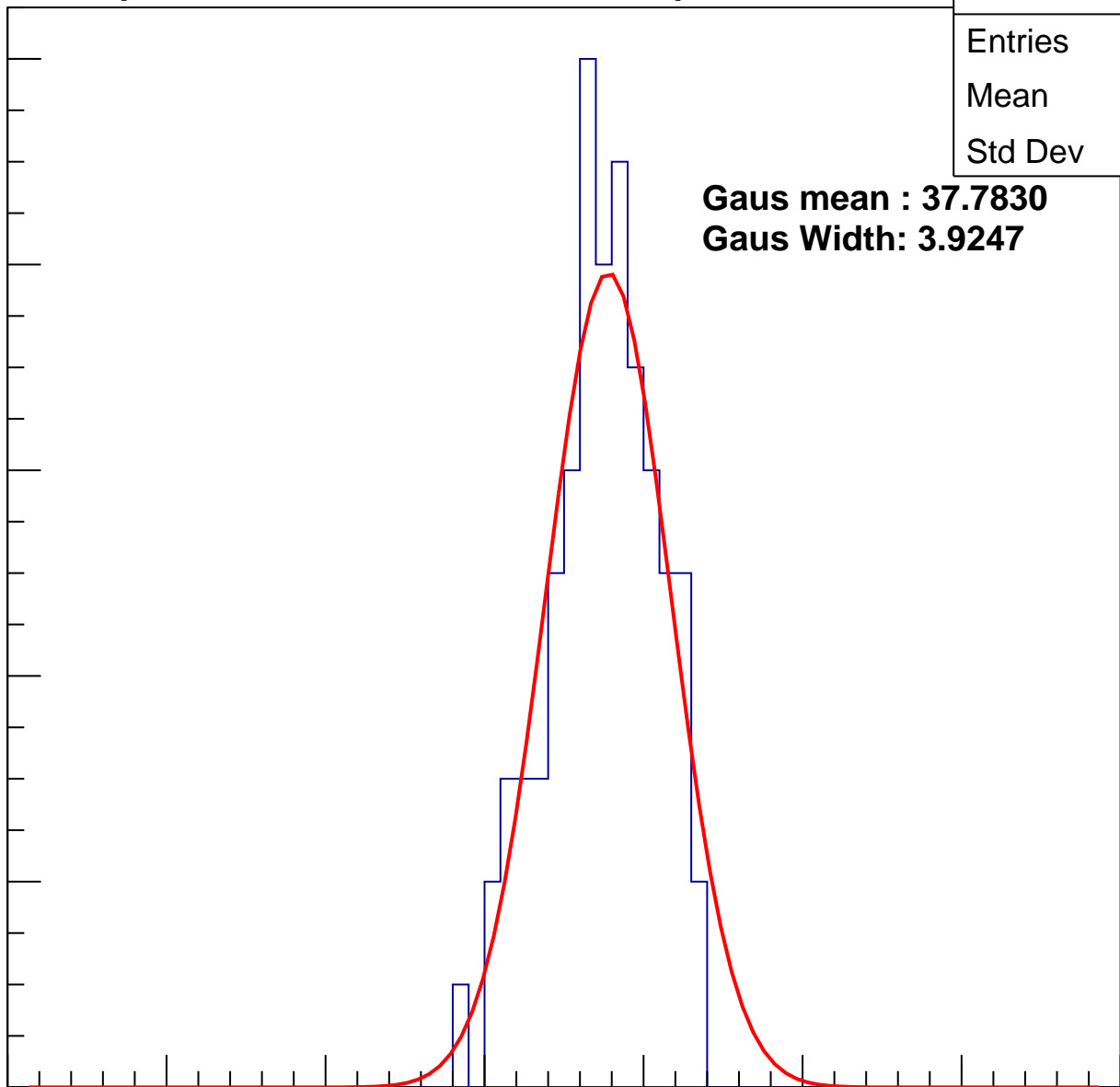
**Gaus Width: 3.9247**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L000S, U7-ch26, adc2

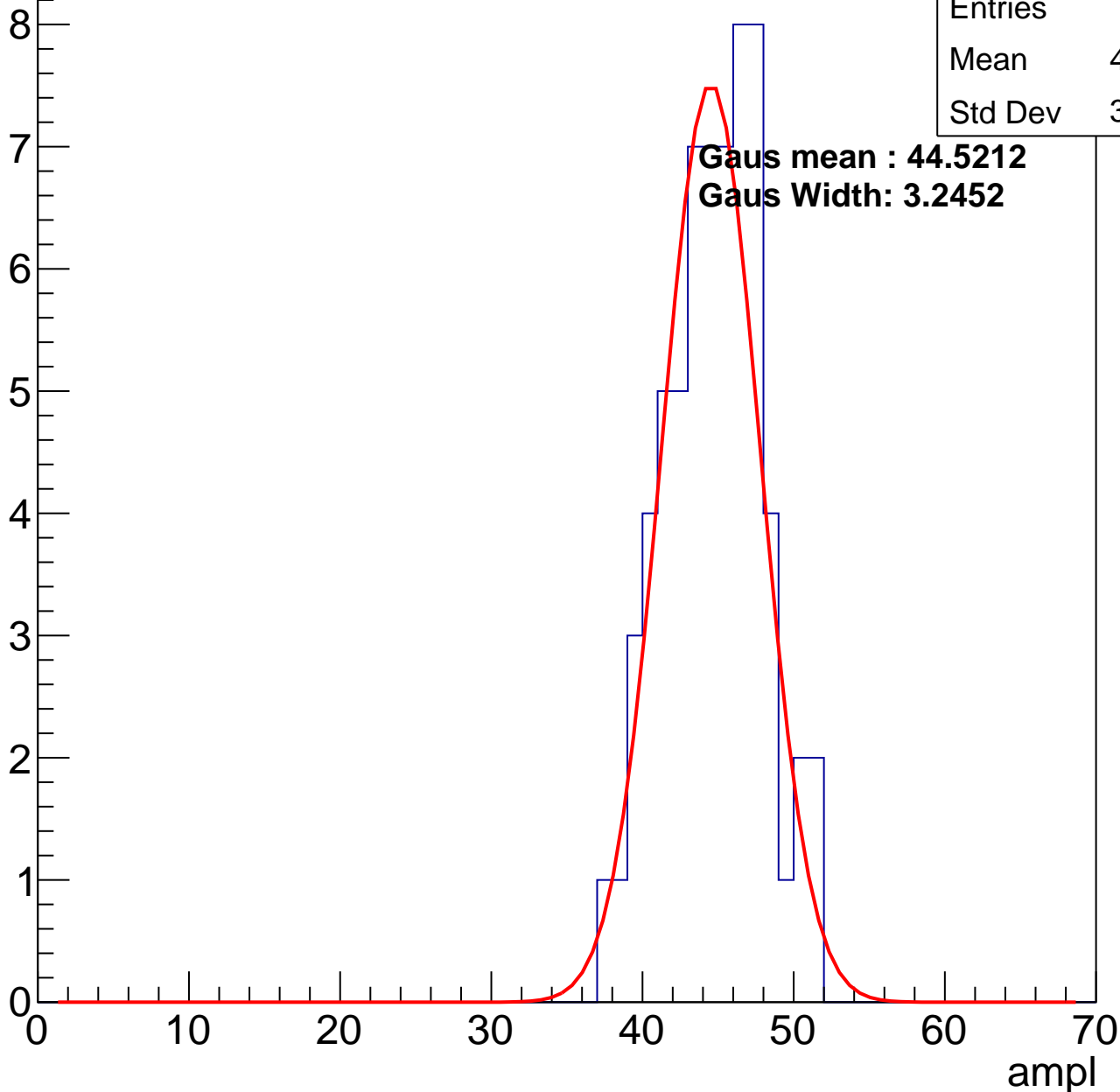
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	65
Mean	44.28
Std Dev	3.189

**Gaus mean : 44.5212**

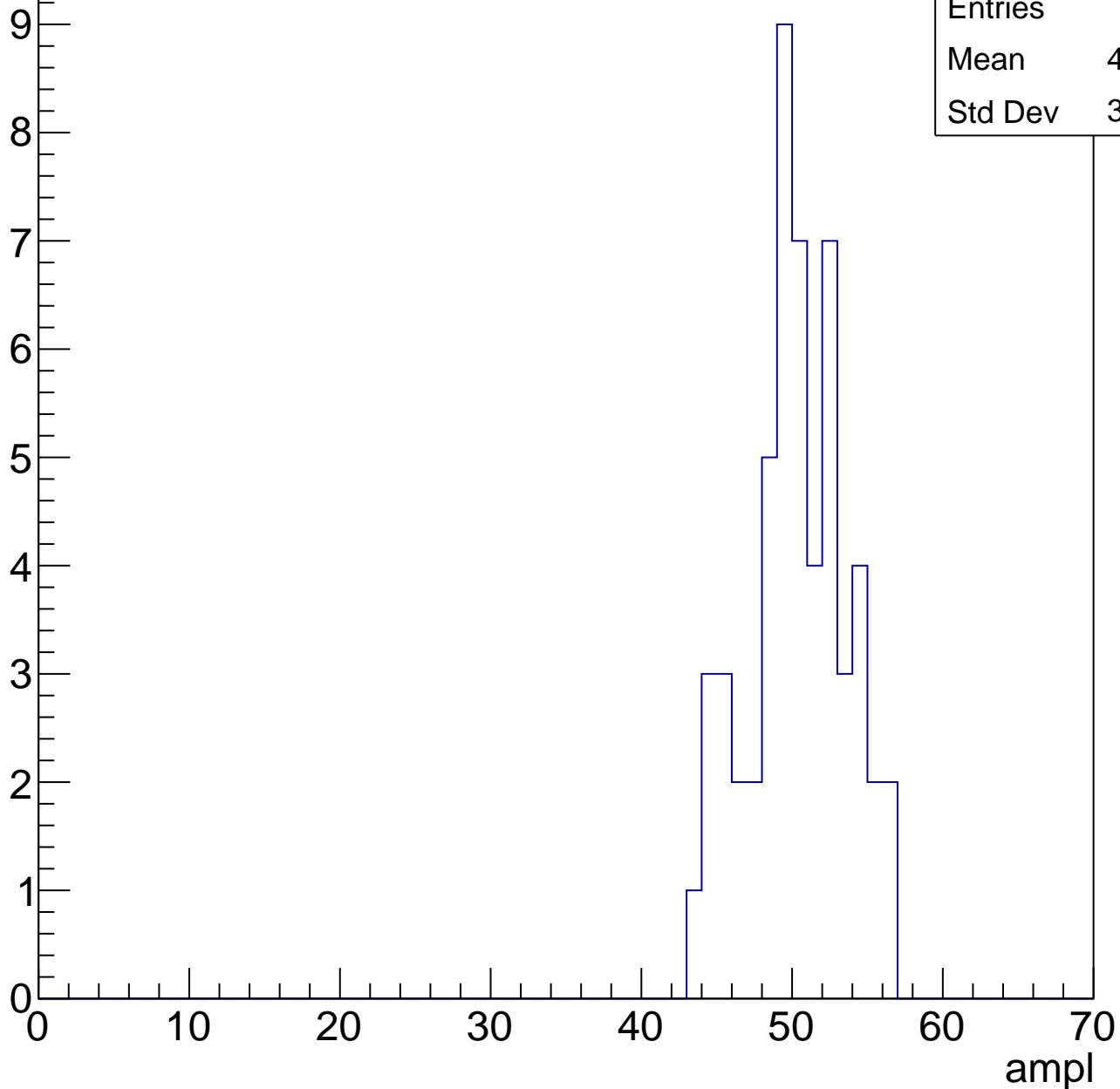
**Gaus Width: 3.2452**



# B0L000S, U7-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



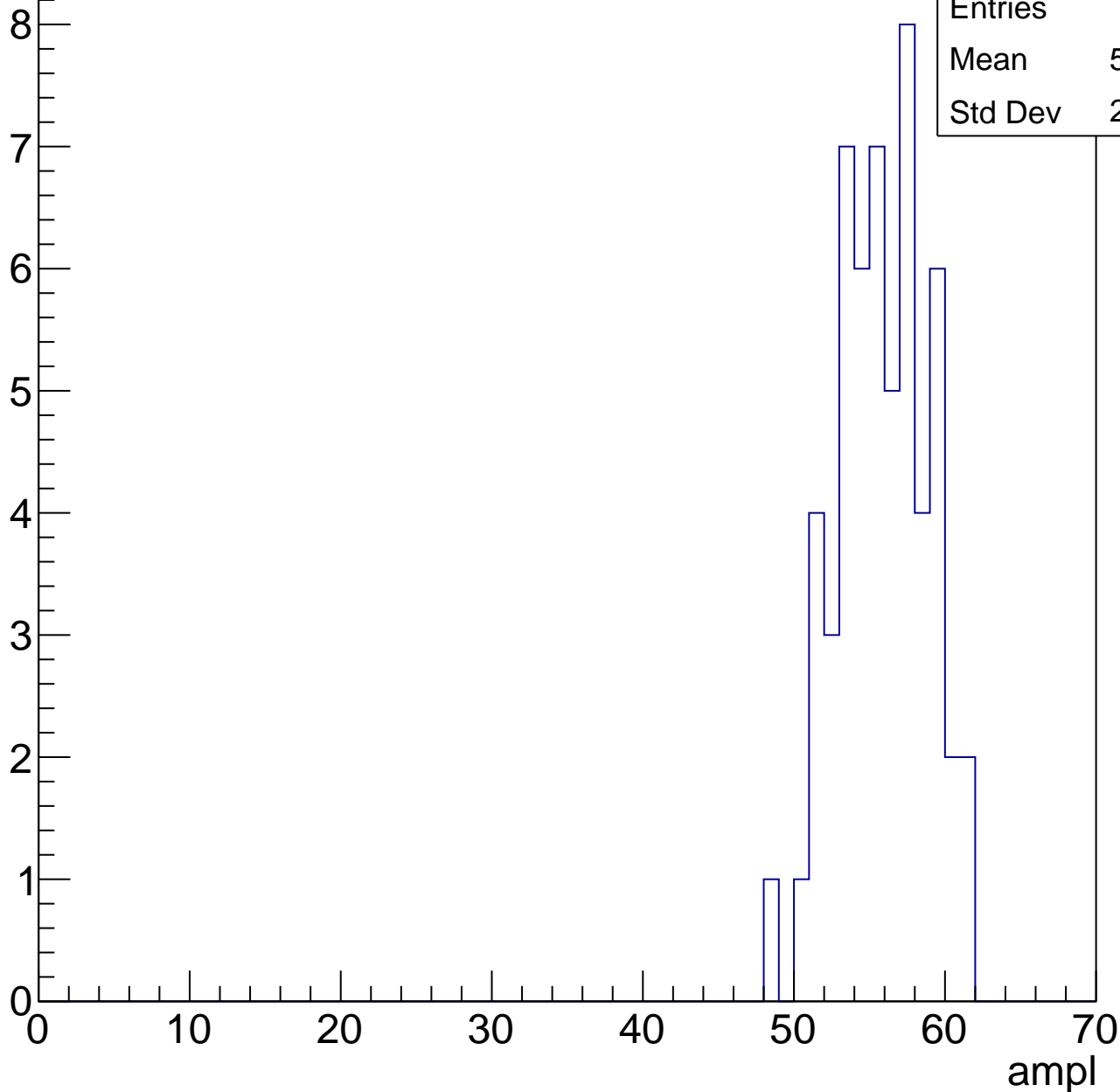
Entries	54
Mean	49.85
Std Dev	3.205

# B0L000S, U7-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	56
Mean	55.39
Std Dev	2.932



# B0L000S, U7-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

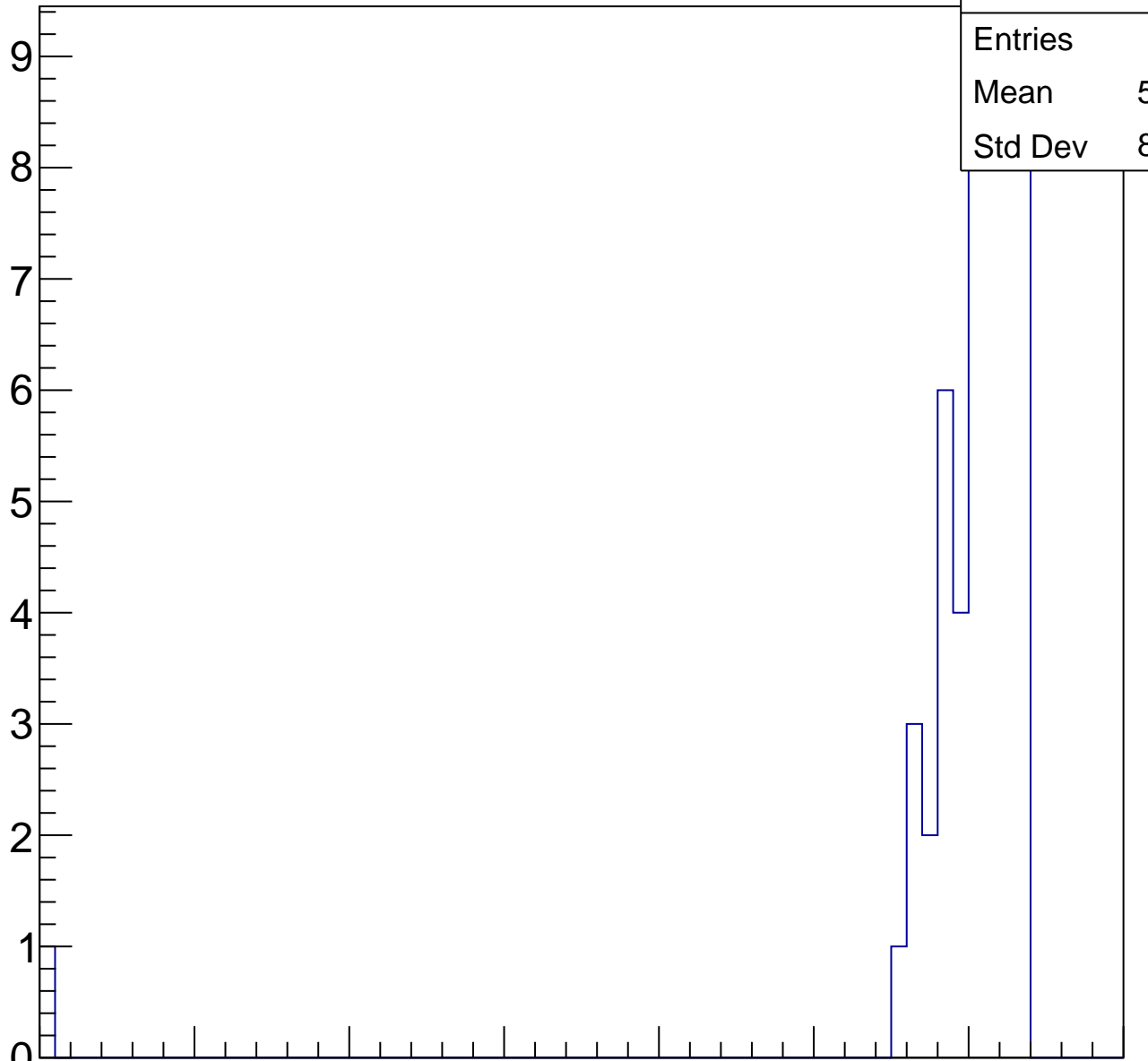
Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	50
Mean	59.02
Std Dev	8.703

ampl

0 10 20 30 40 50 60 70



# B0L000S, U7-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B0L000S, U7-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L000S, U7-ch27, adc0

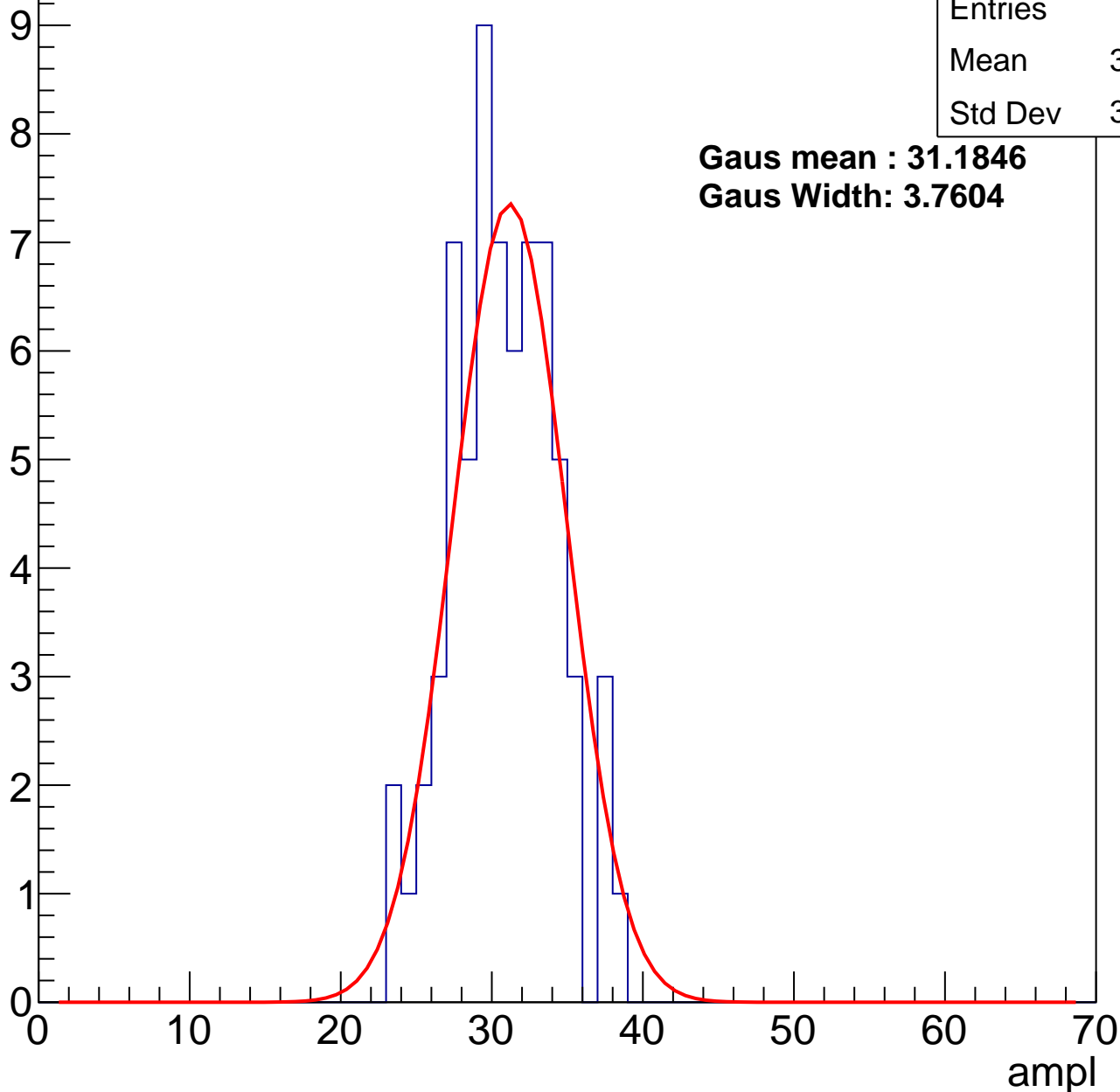
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	68
Mean	30.34
Std Dev	3.385

**Gaus mean : 31.1846**

**Gaus Width: 3.7604**



# B0L000S, U7-ch27, adc1

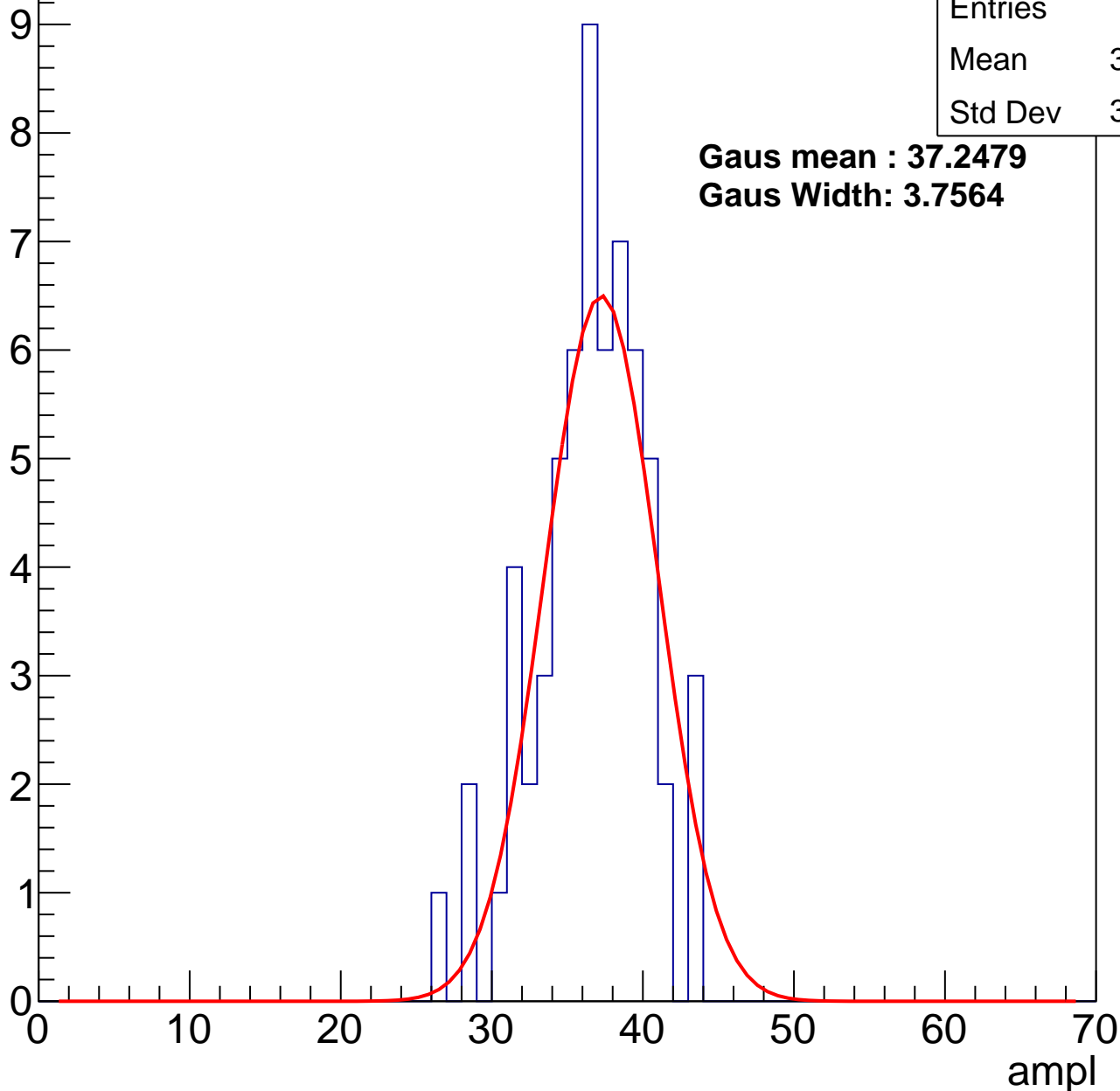
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	62
Mean	36.06
Std Dev	3.623

**Gaus mean : 37.2479**

**Gaus Width: 3.7564**



# B0L000S, U7-ch27, adc2

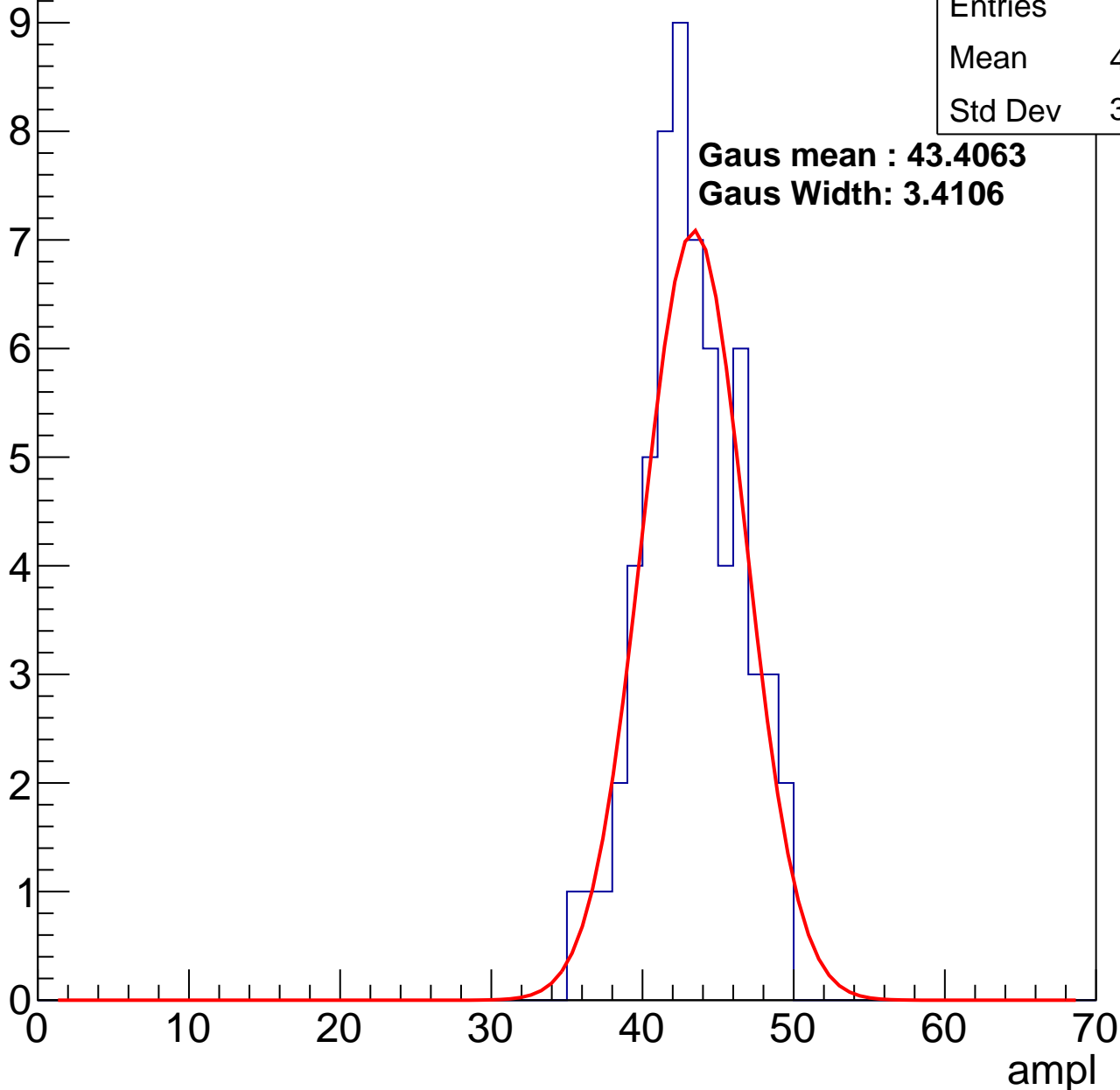
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	62
Mean	42.74
Std Dev	3.152

**Gaus mean : 43.4063**

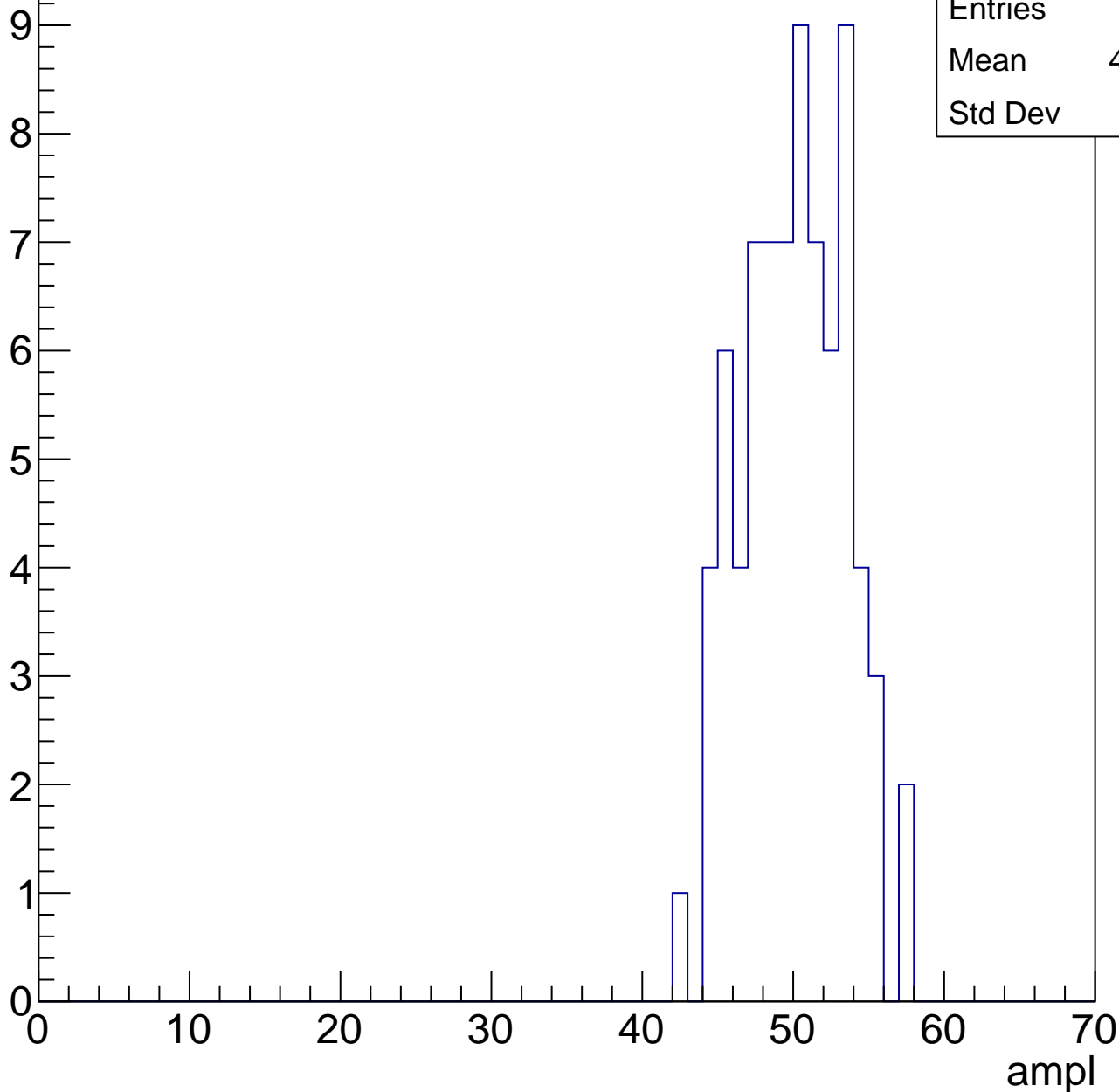
**Gaus Width: 3.4106**



# B0L000S, U7-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	76
Mean	49.62
Std Dev	3.36

# B0L000S, U7-ch27, adc4

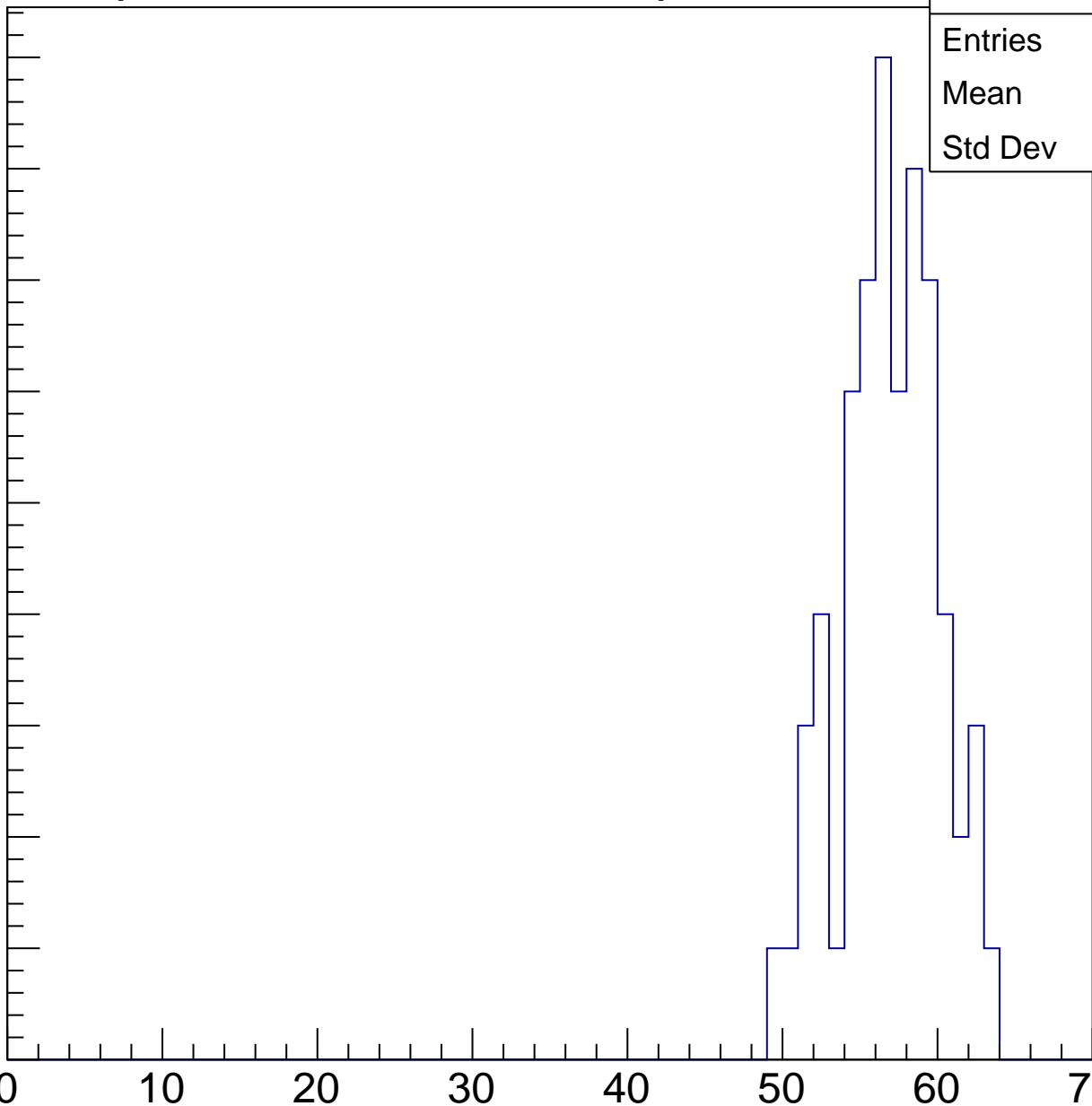
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	63
Mean	56.44
Std Dev	3.146

ampl



# B0L000S, U7-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

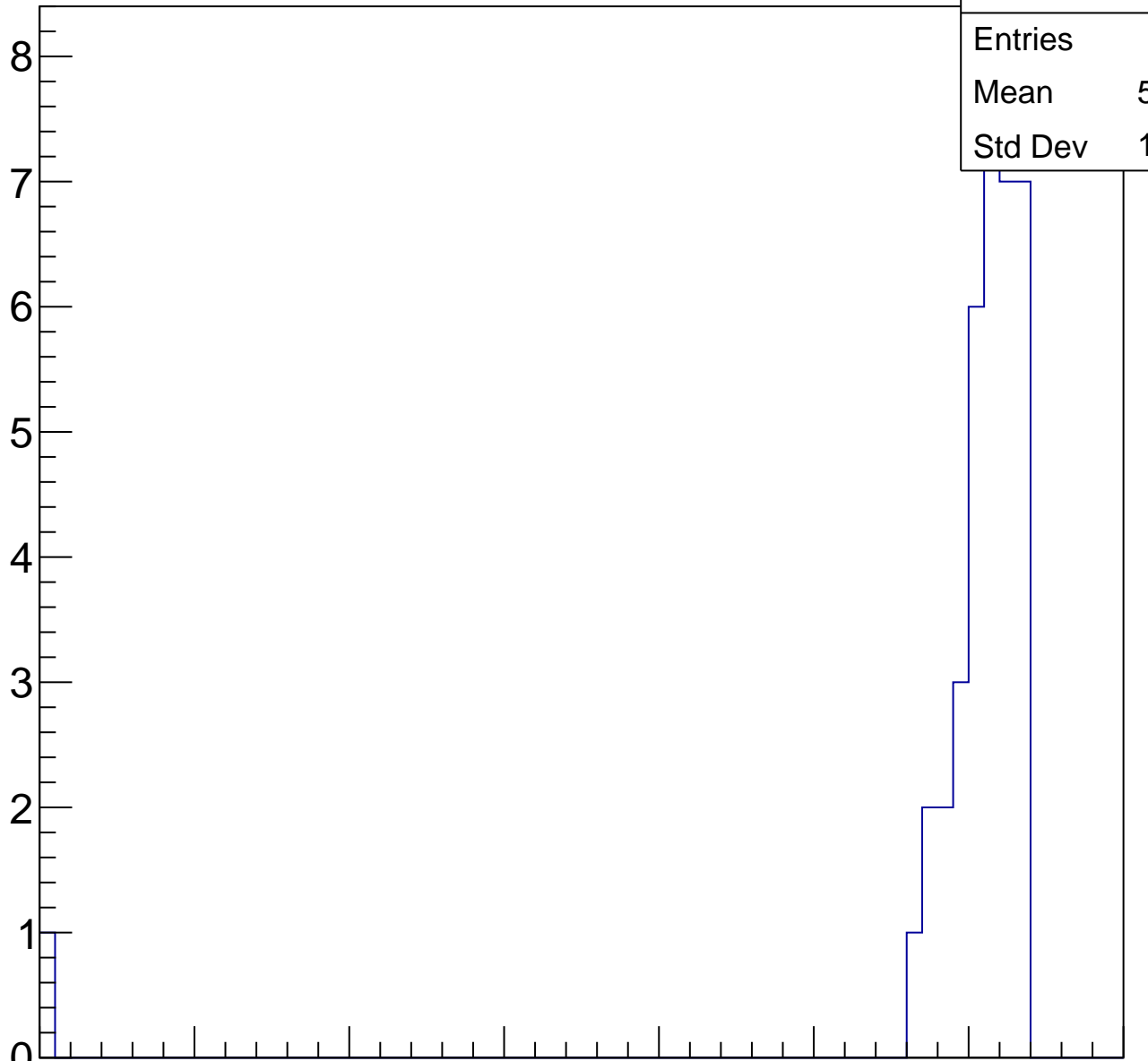
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	37
Mean	59.08
Std Dev	10.02

ampl

0 10 20 30 40 50 60 70



# B0L000S, U7-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch28, adc0

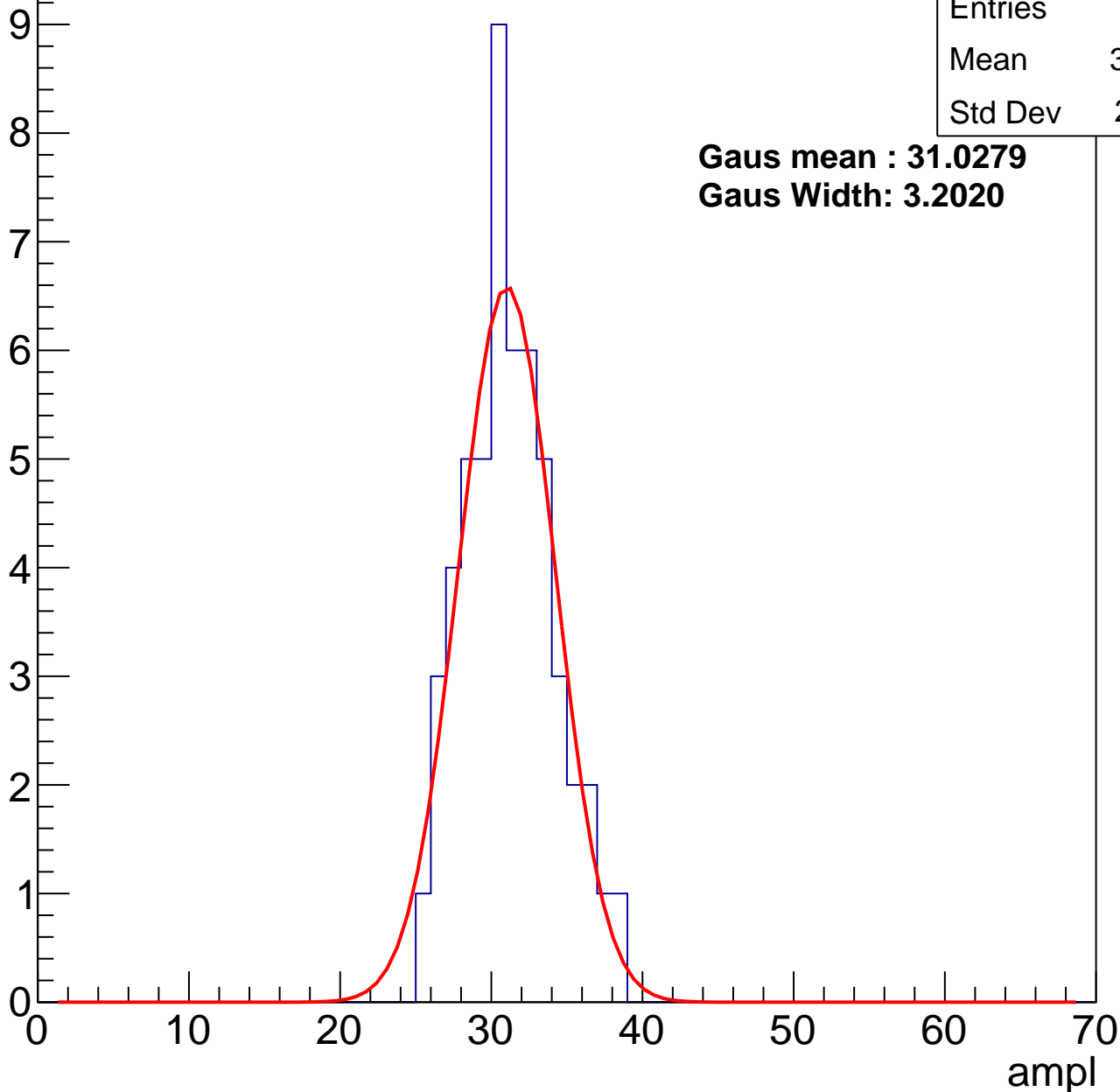
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	53
Mean	30.72
Std Dev	2.961

**Gaus mean : 31.0279**

**Gaus Width: 3.2020**



# B0L000S, U7-ch28, adc1

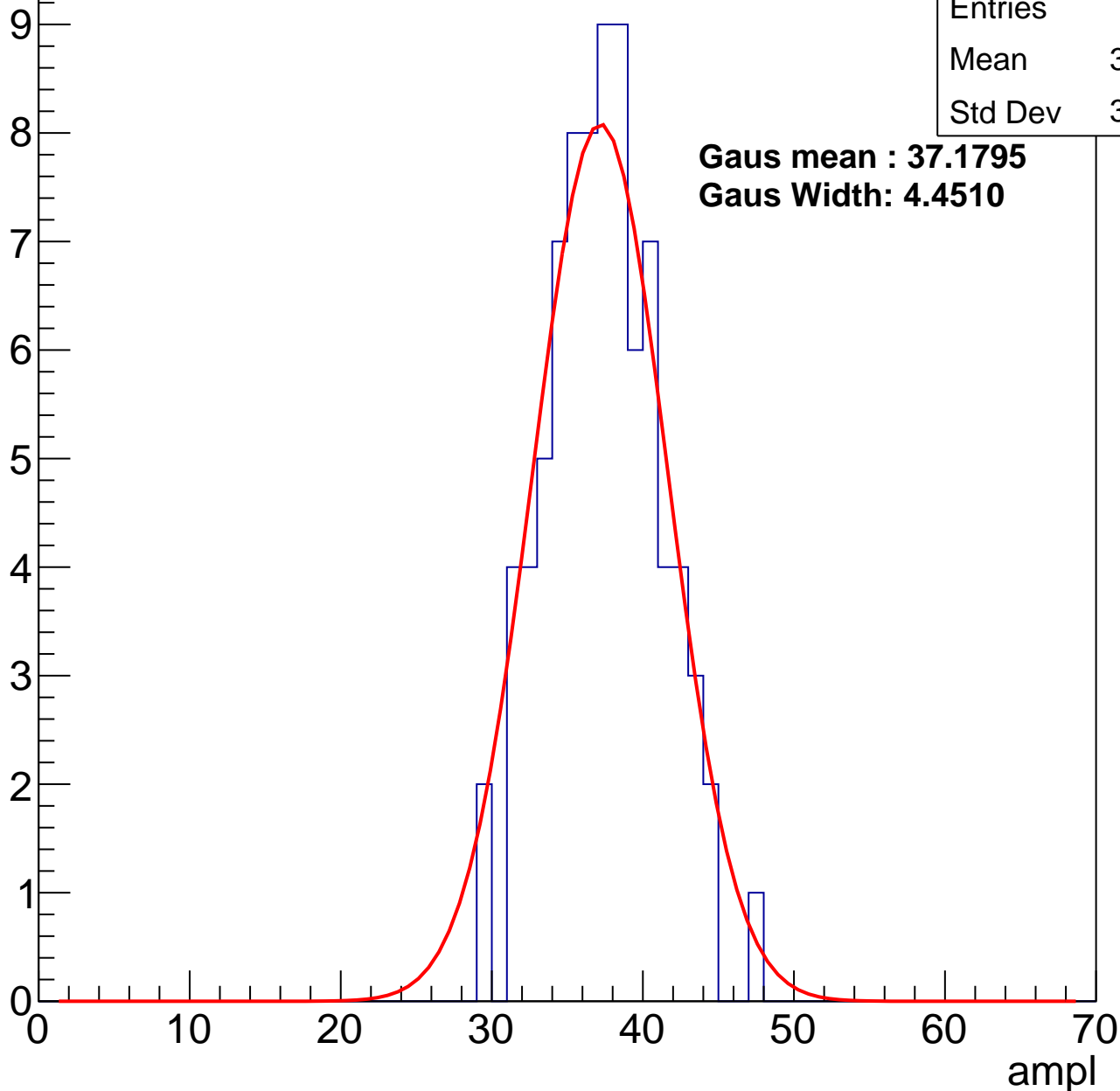
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	83
Mean	36.94
Std Dev	3.675

**Gaus mean : 37.1795**

**Gaus Width: 4.4510**



# B0L000S, U7-ch28, adc2

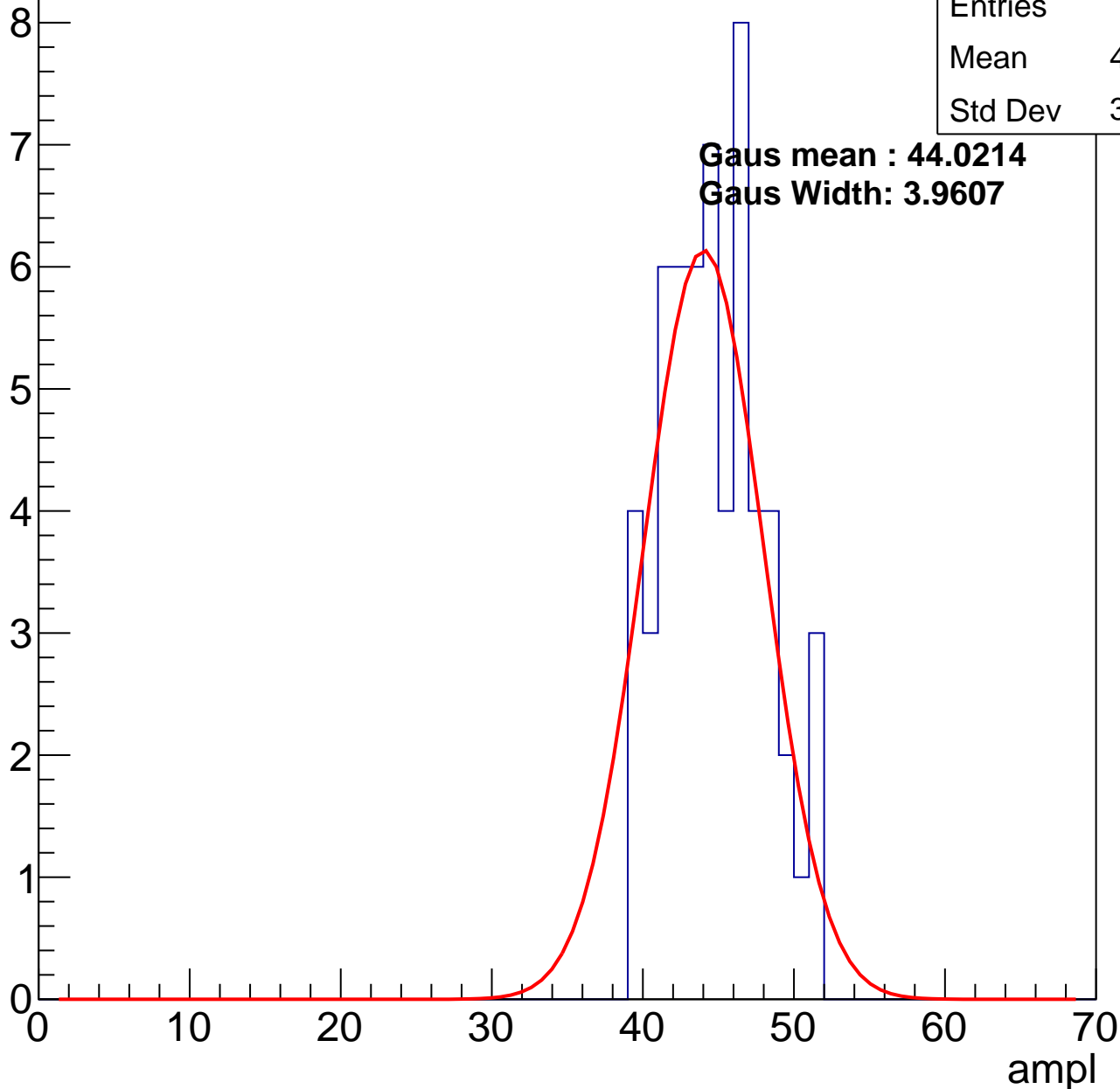
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	58
Mean	44.29
Std Dev	3.206

**Gaus mean : 44.0214**

**Gaus Width: 3.9607**

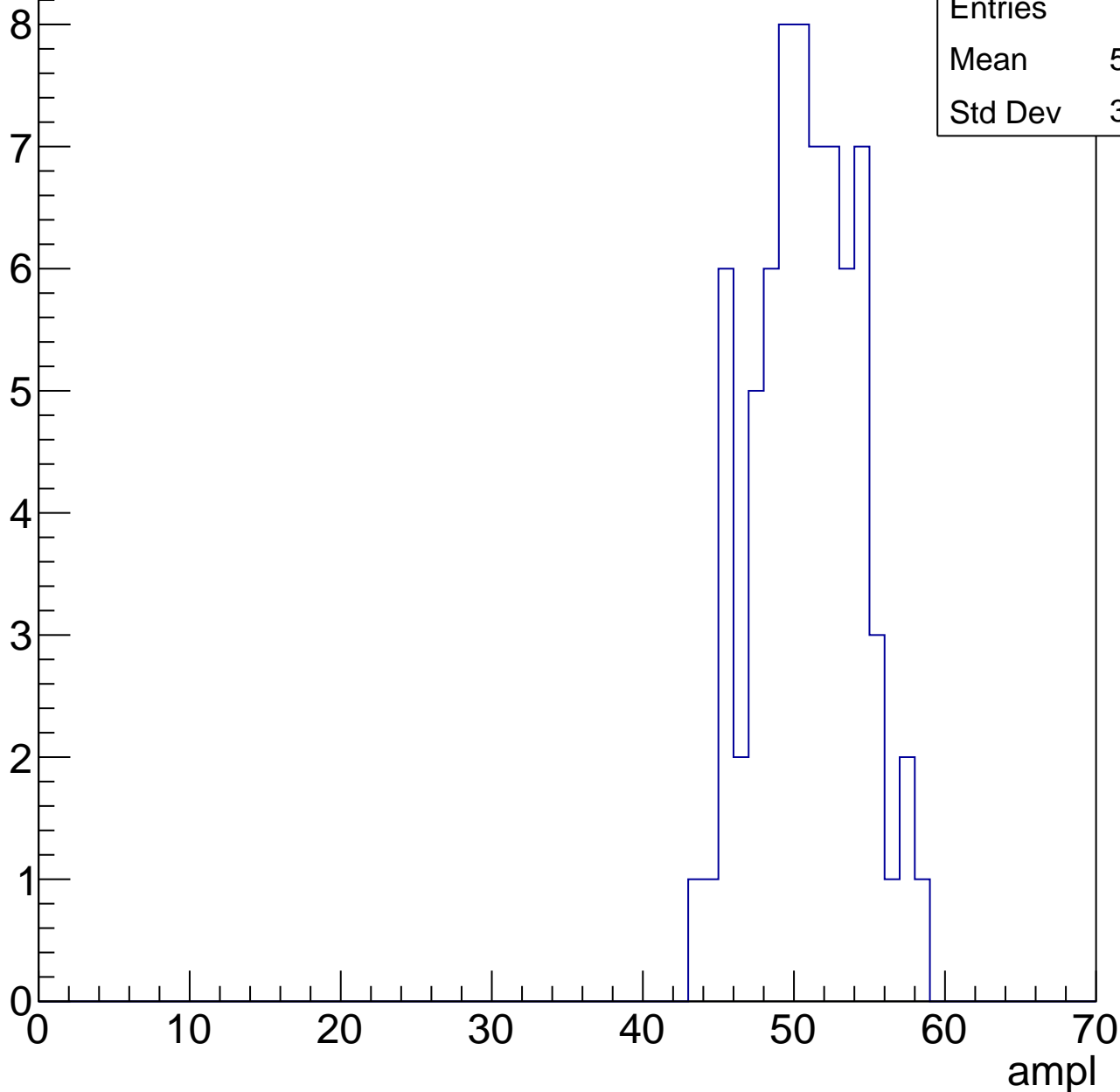


# B0L000S, U7-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	71
Mean	50.34
Std Dev	3.377

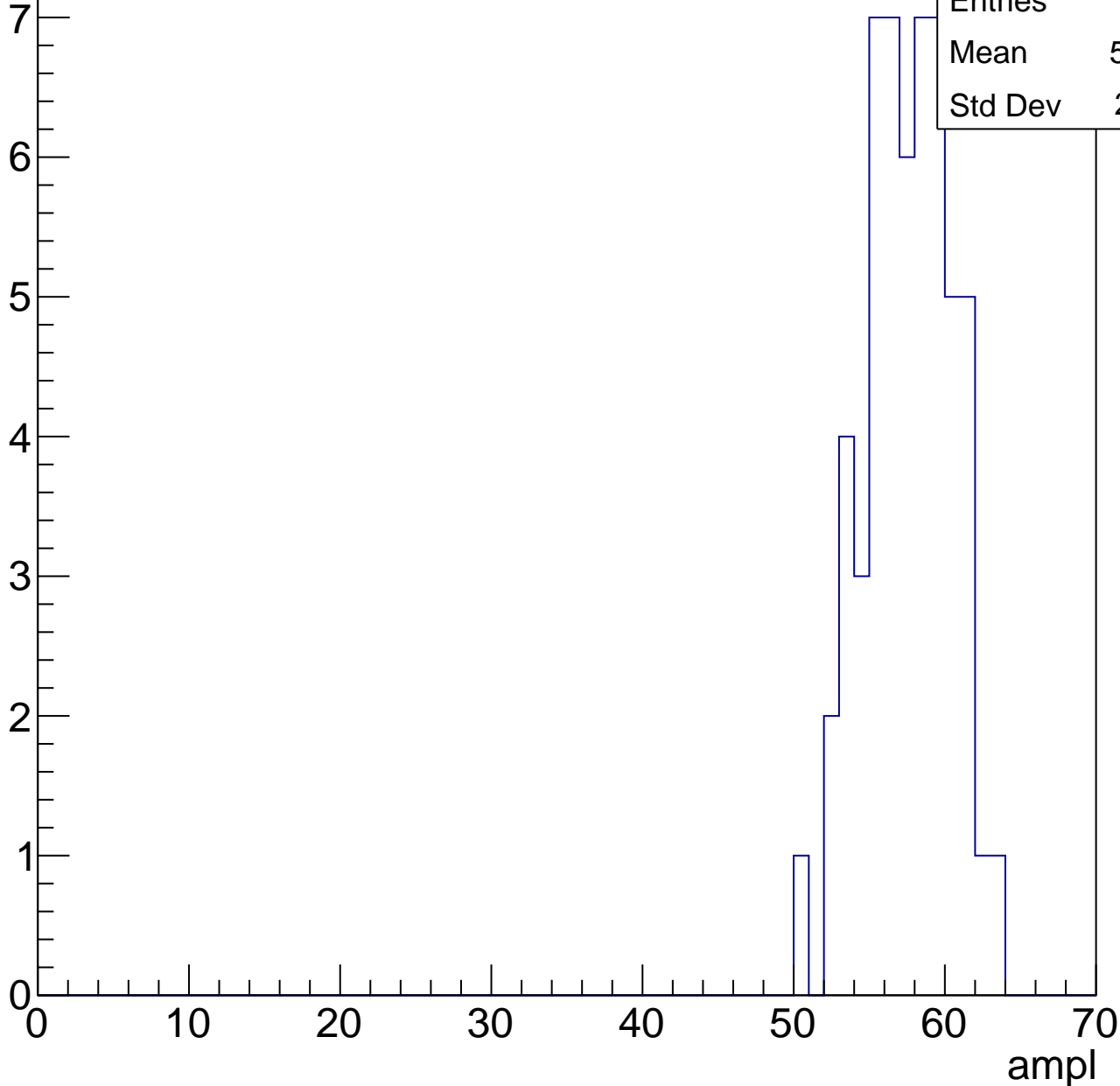


# B0L000S, U7-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	56
Mean	57.07
Std Dev	2.821

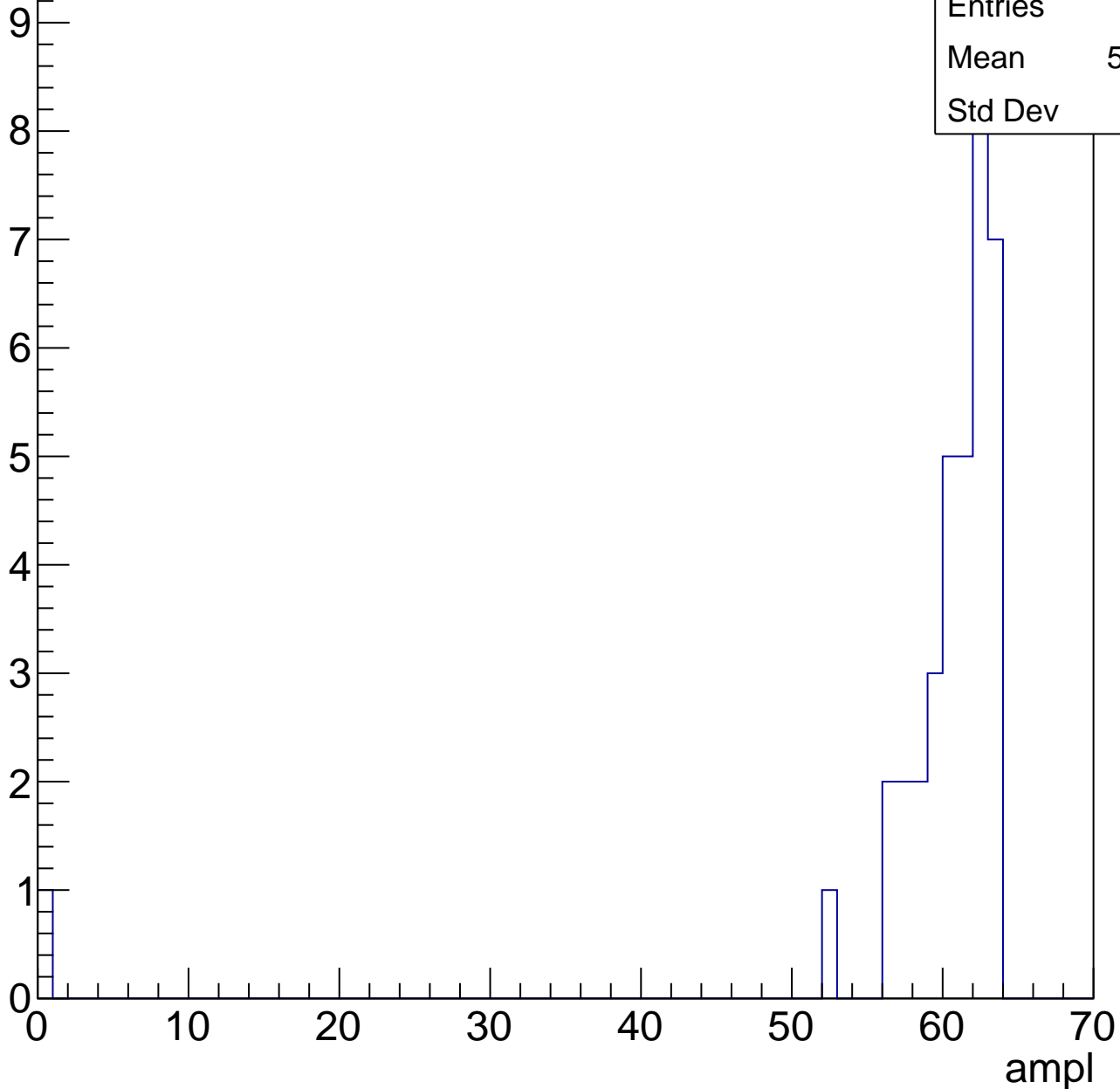


# B0L000S, U7-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	37
Mean	58.78
Std Dev	10.1



# B0L000S, U7-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	2
Mean	63
Std Dev	0



# B0L000S, U7-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch29, adc0

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	71
Mean	30.56
Std Dev	4.91

**Gaus mean : 31.3299**

**Gaus Width: 3.0127**

Entry

10  
8  
6  
4  
2  
0

ampl

0

10

20

30

40

50

60

70

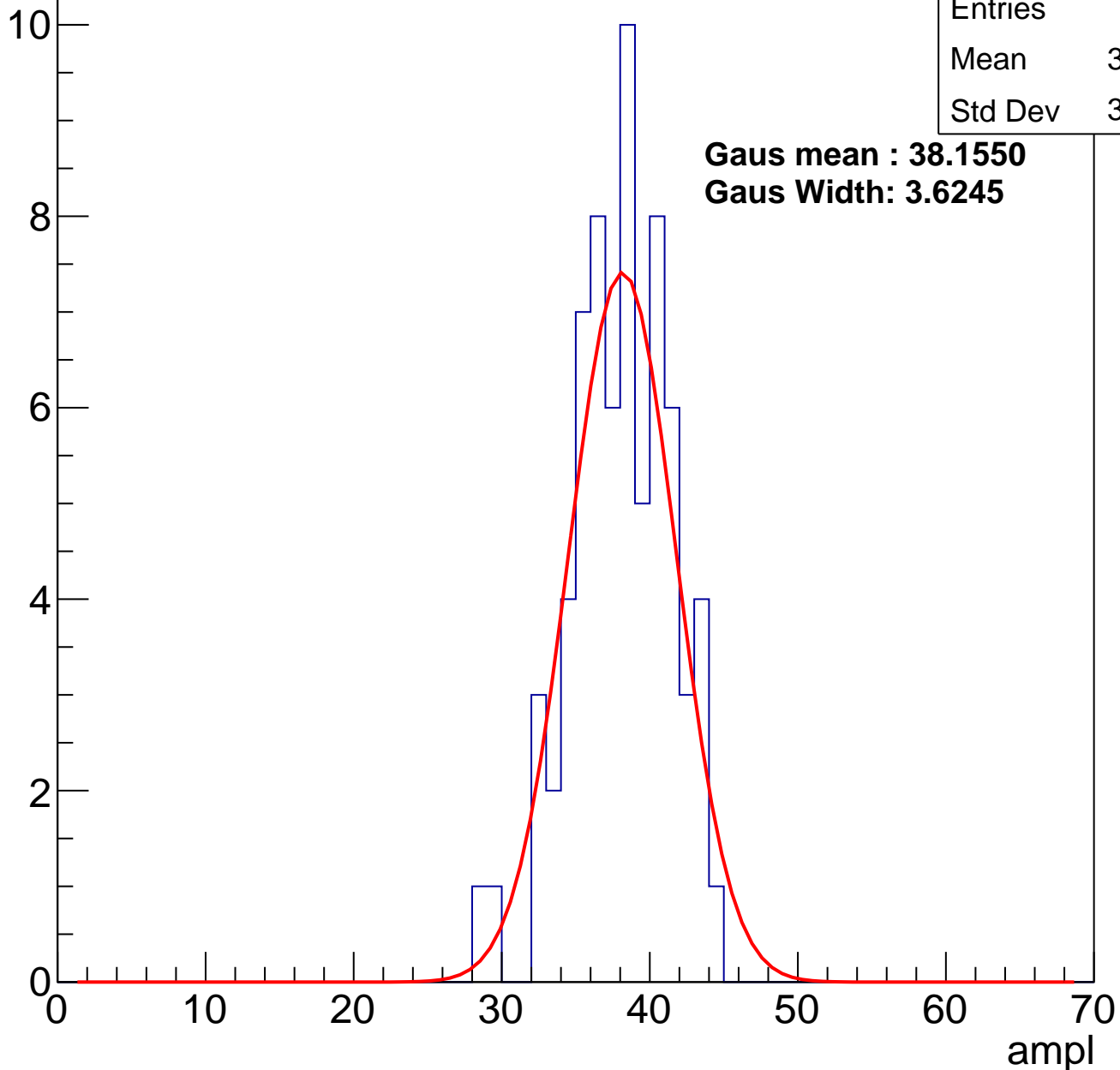
# B0L000S, U7-ch29, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	69
Mean	37.58
Std Dev	3.334

**Gaus mean : 38.1550**  
**Gaus Width: 3.6245**

Entry



# B0L000S, U7-ch29, adc2

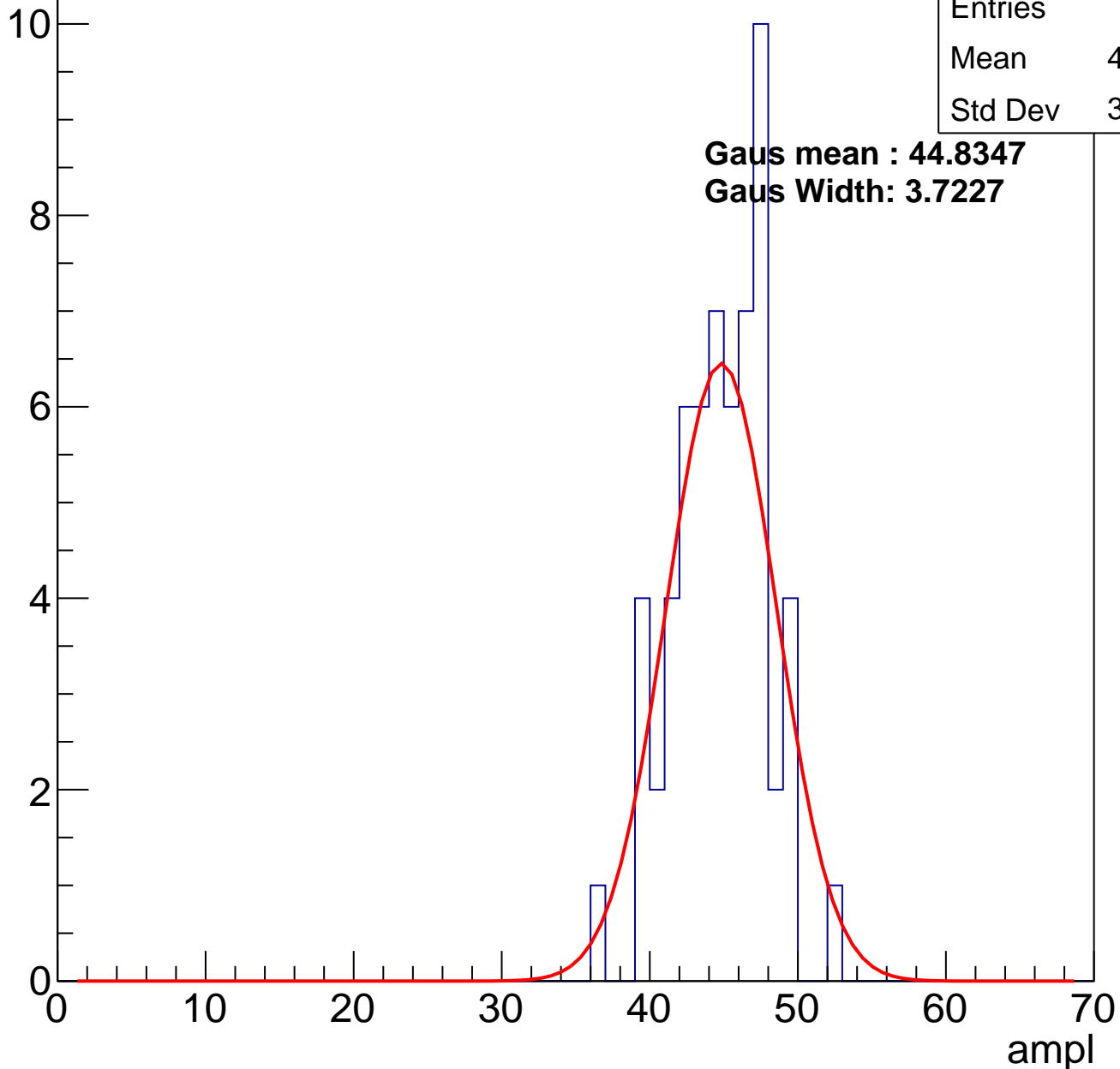
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	60
Mean	44.33
Std Dev	3.097

**Gaus mean : 44.8347**

**Gaus Width: 3.7227**

Entry

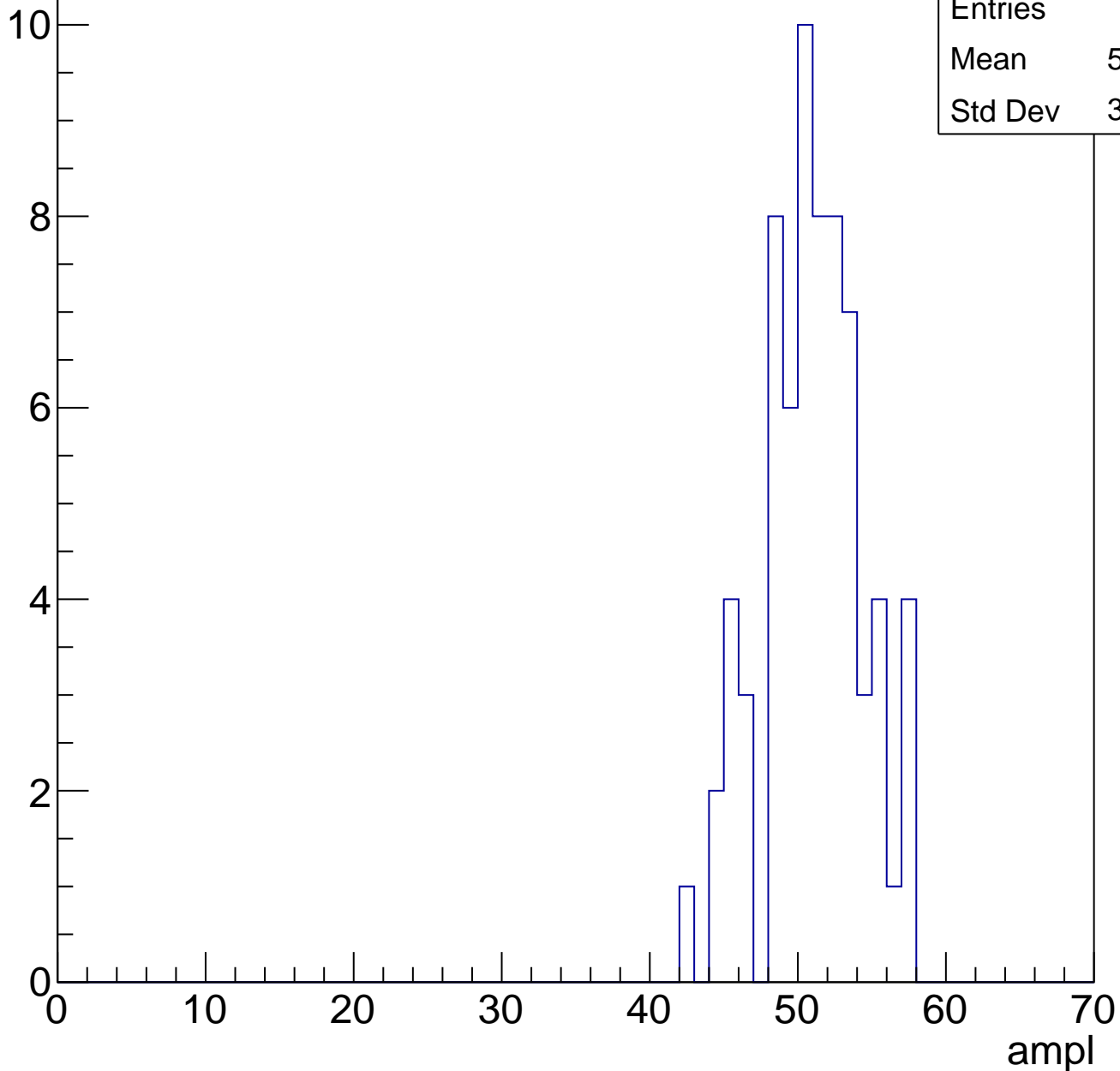


# B0L000S, U7-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

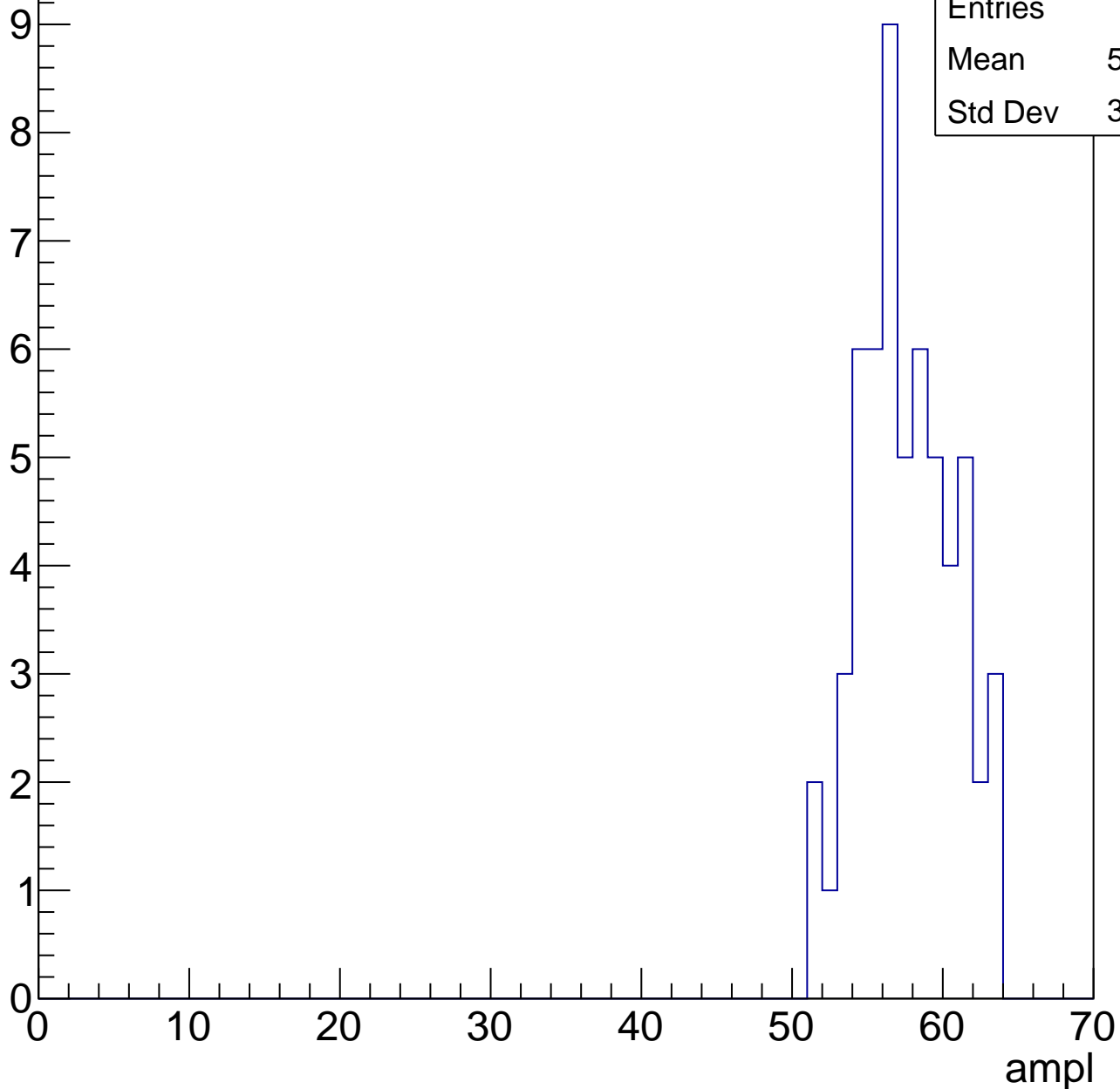
Entries	69
Mean	50.54
Std Dev	3.373



# B0L000S, U7-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

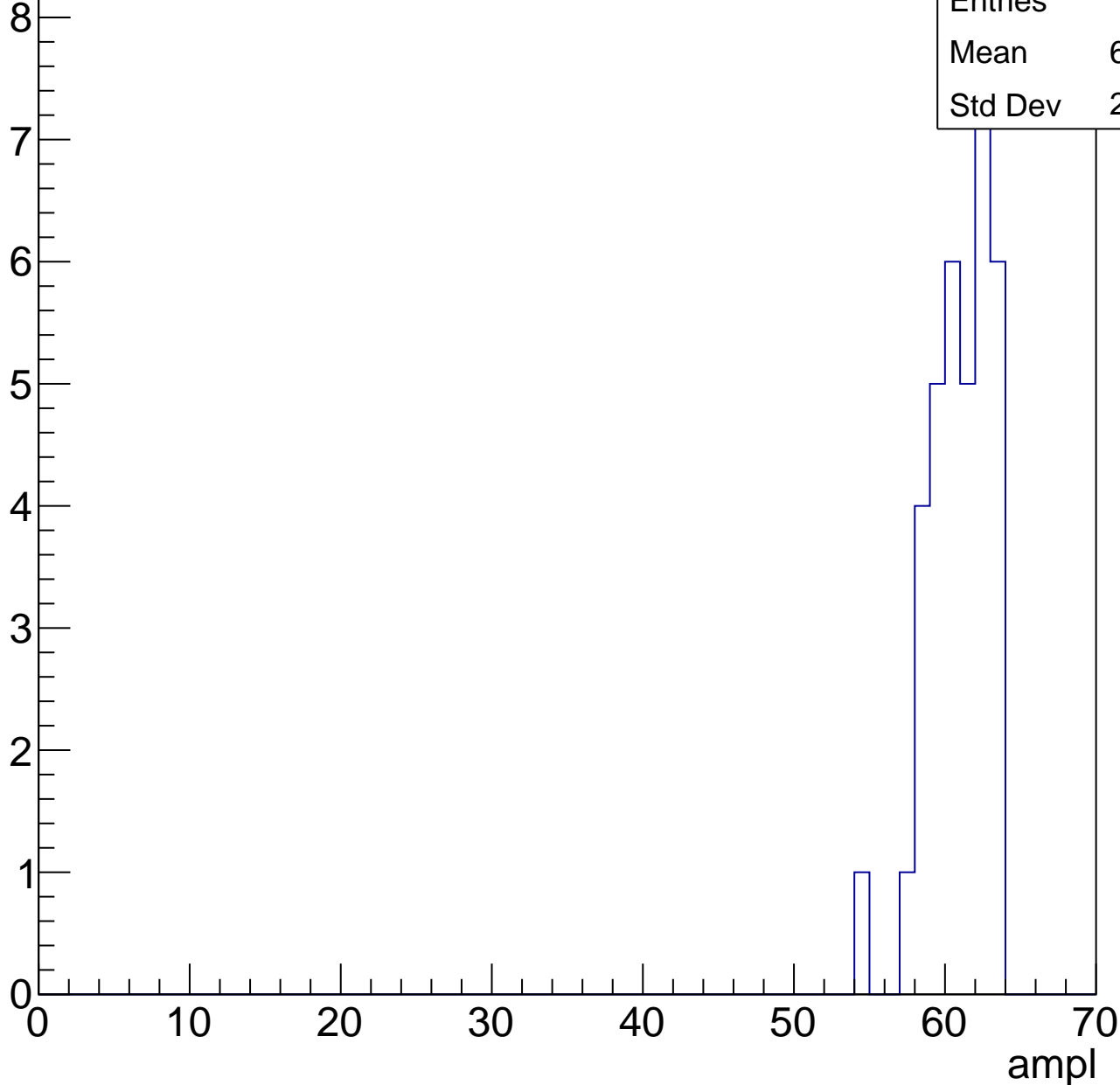


# B0L000S, U7-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	36
Mean	60.47
Std Dev	2.034



# B0L000S, U7-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L000S, U7-ch30, adc0

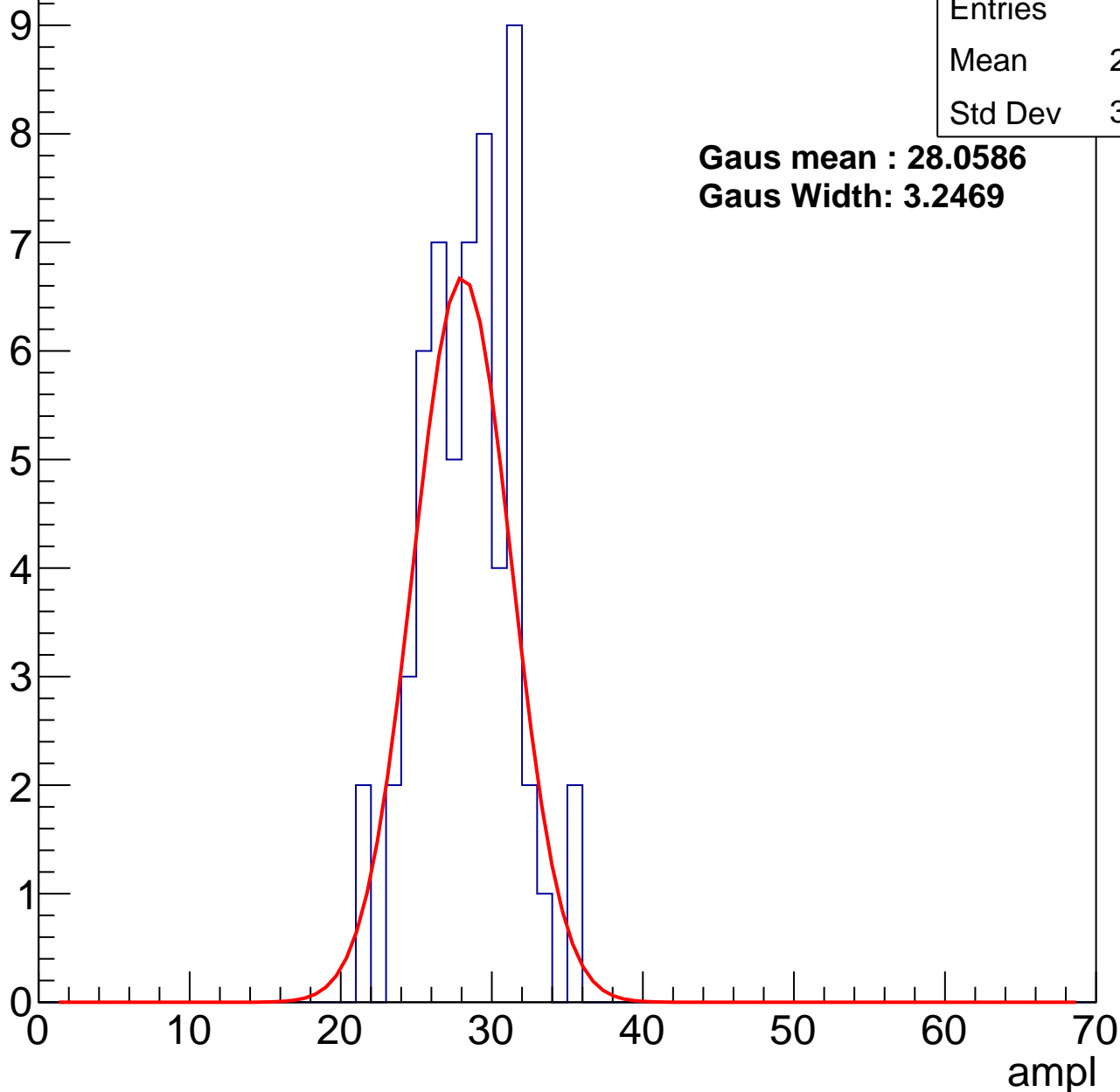
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	58
Mean	27.95
Std Dev	3.059

**Gaus mean : 28.0586**

**Gaus Width: 3.2469**



# B0L000S, U7-ch30, adc1

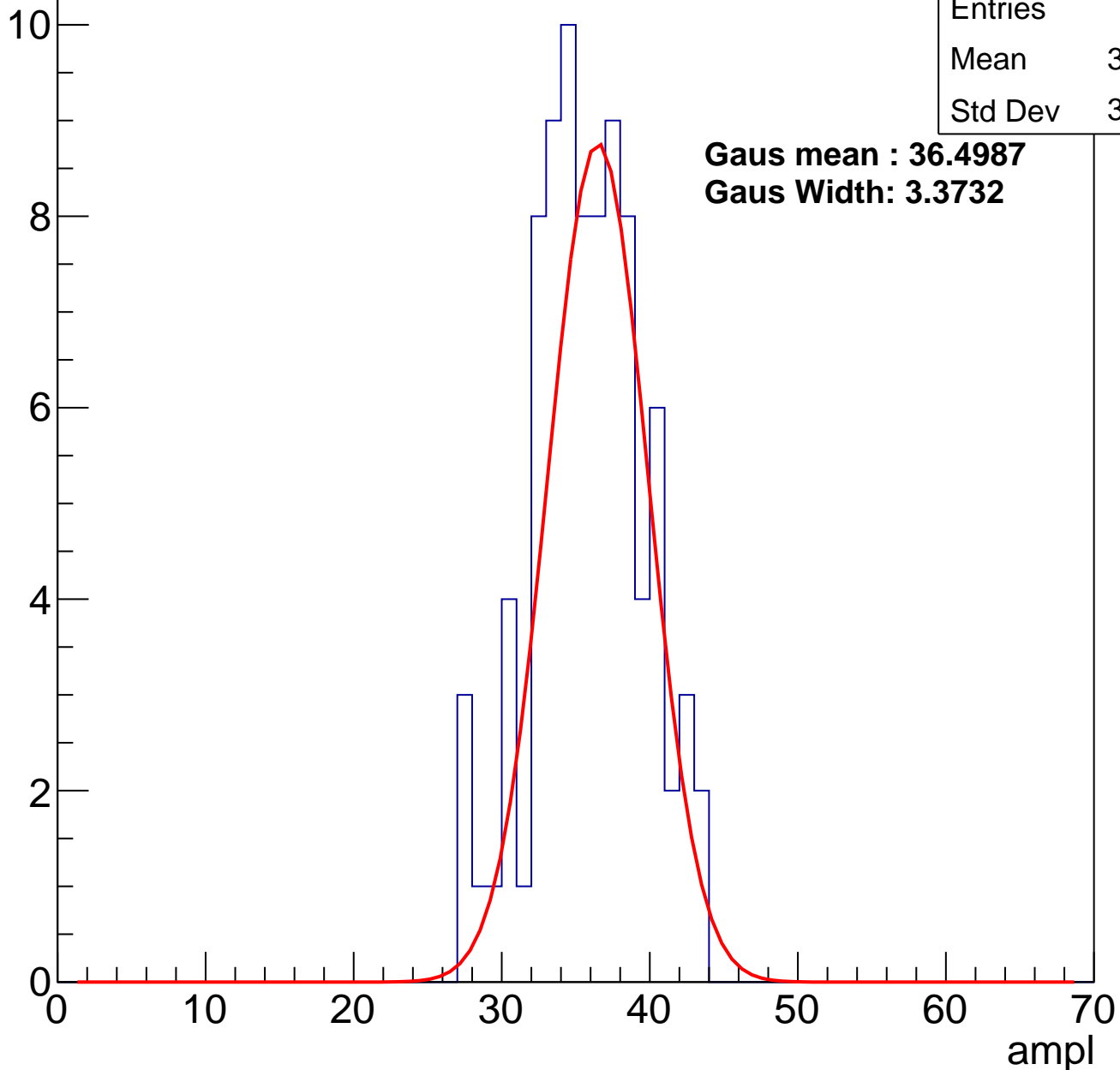
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	87
Mean	35.37
Std Dev	3.677

**Gaus mean : 36.4987**

**Gaus Width: 3.3732**

Entry



# B0L000S, U7-ch30, adc2

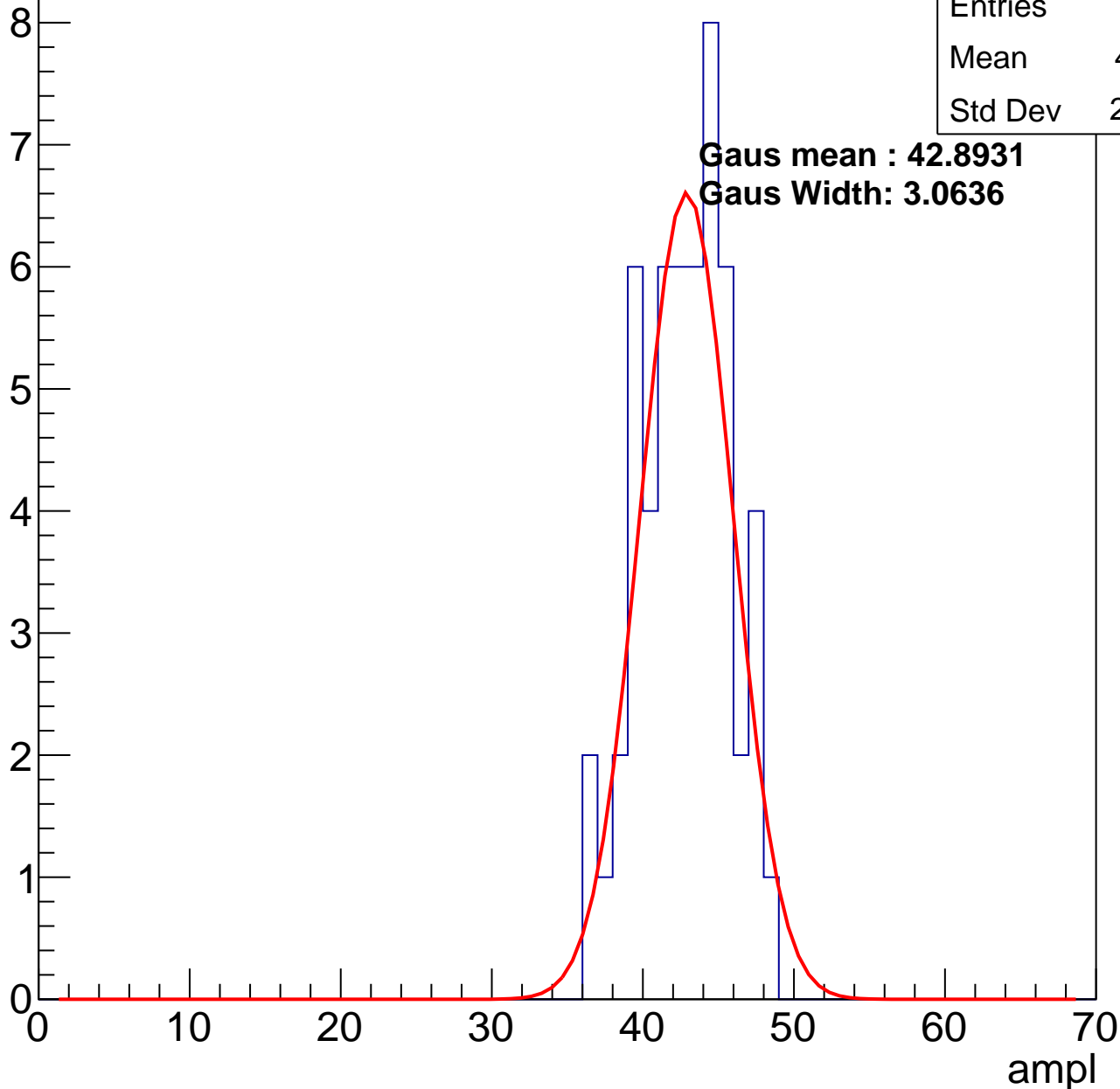
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	54
Mean	42.31
Std Dev	2.918

**Gaus mean : 42.8931**

**Gaus Width: 3.0636**



# B0L000S, U7-ch30, adc3

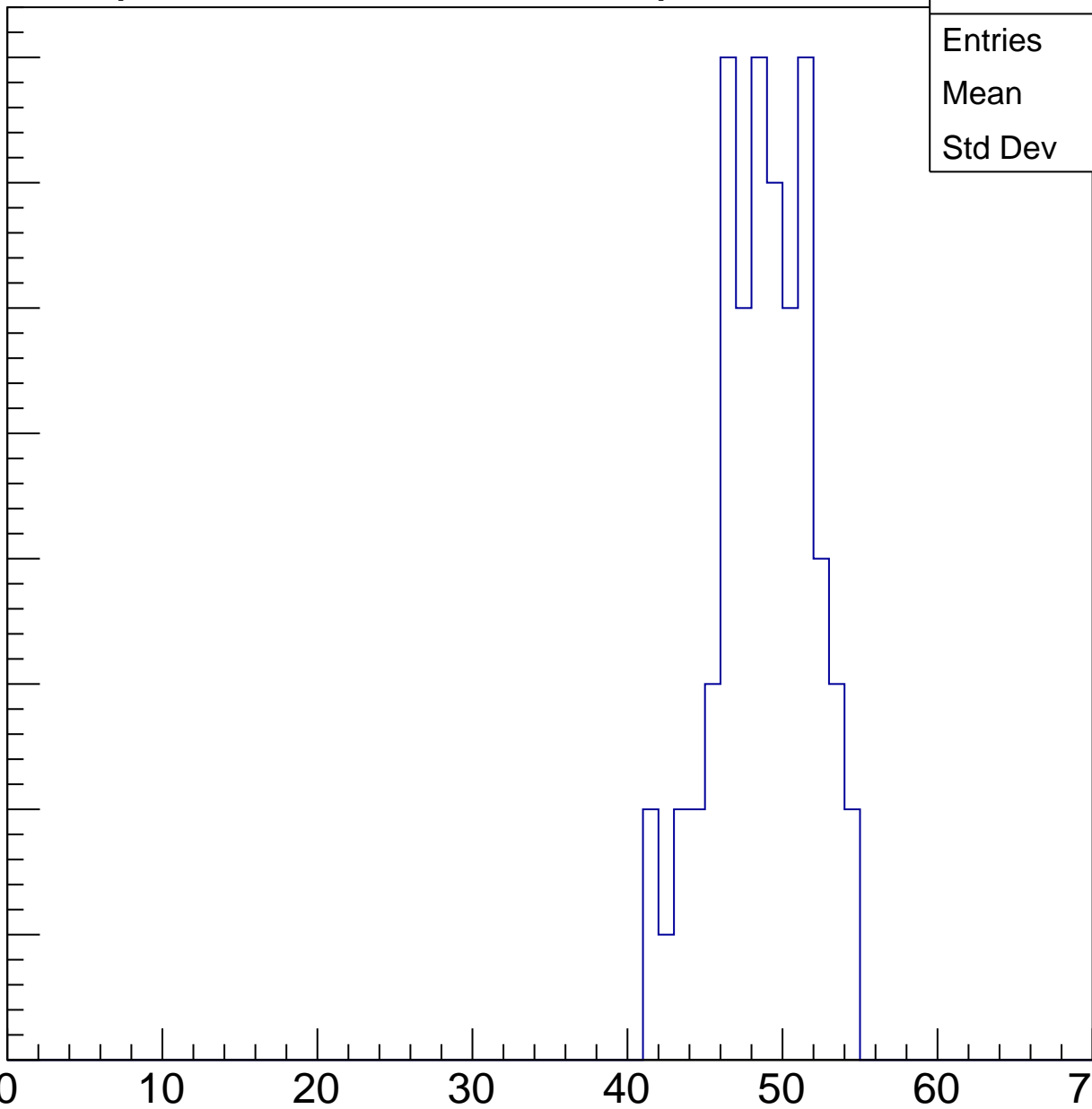
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

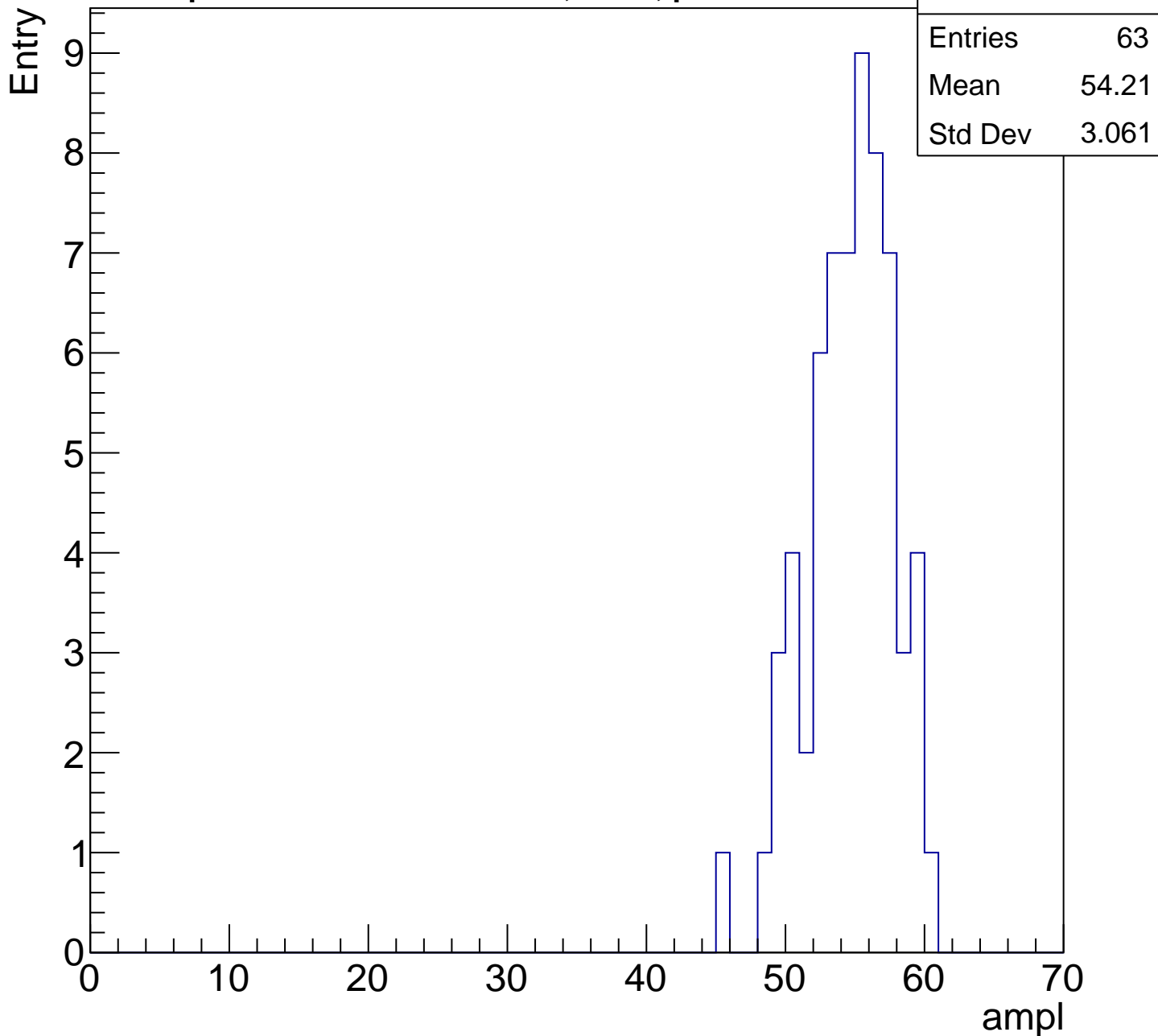
Entries	62
Mean	48.27
Std Dev	3.086

ampl



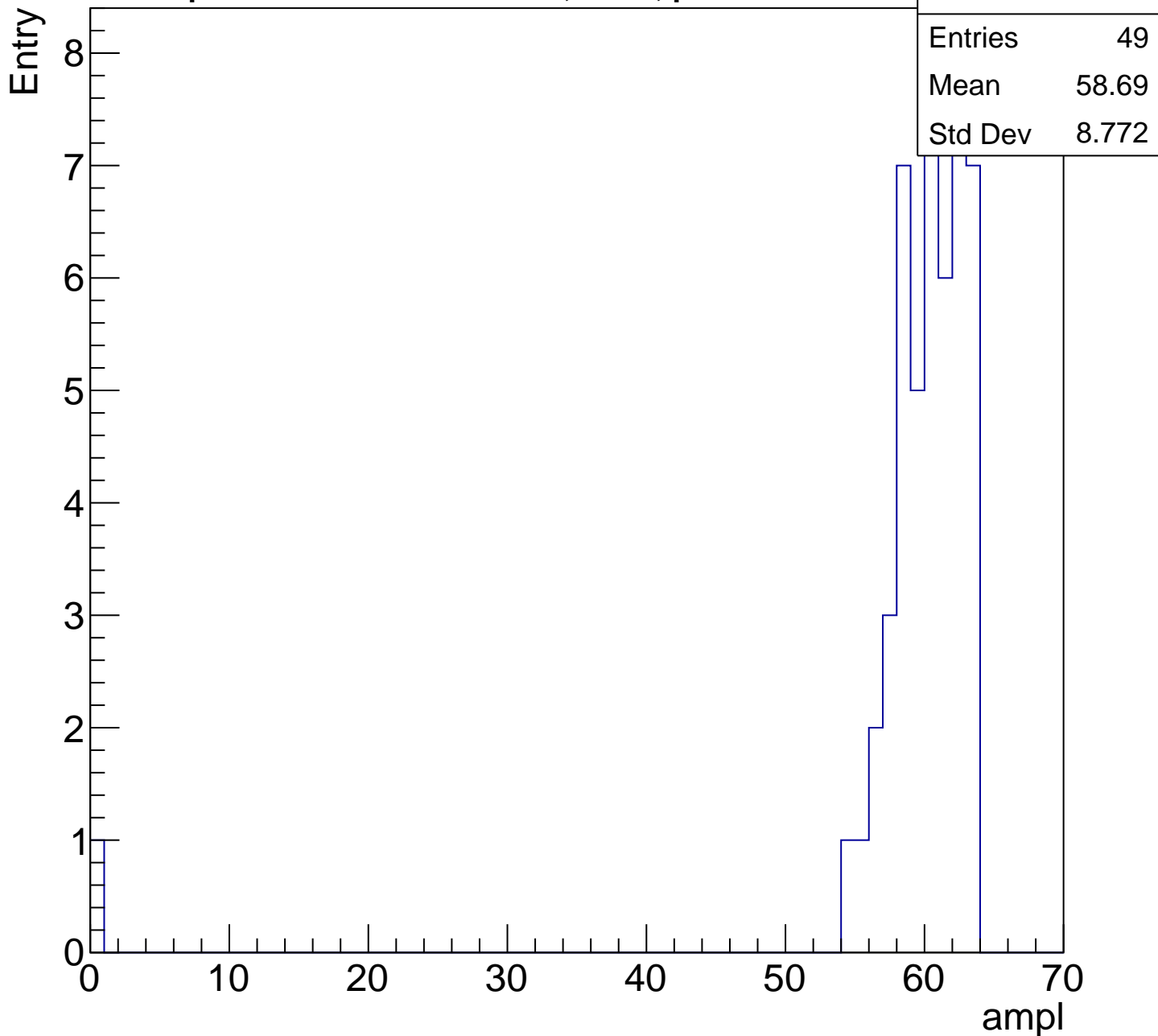
# B0L000S, U7-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1



# B0L000S, U7-ch30, adc5

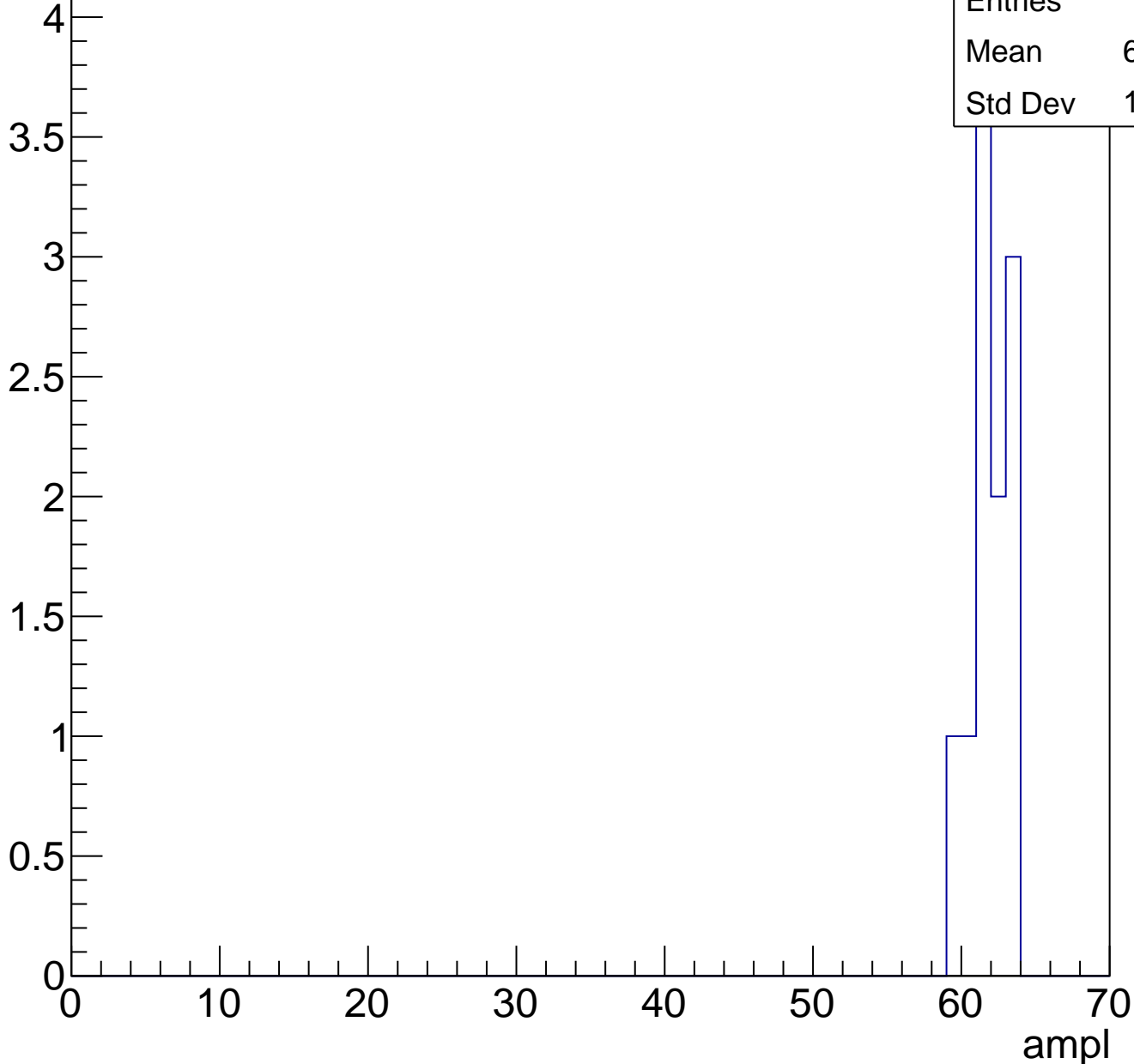
calib\_packv5\_042523\_0143.root, FC#5, port B1



# B0L000S, U7-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

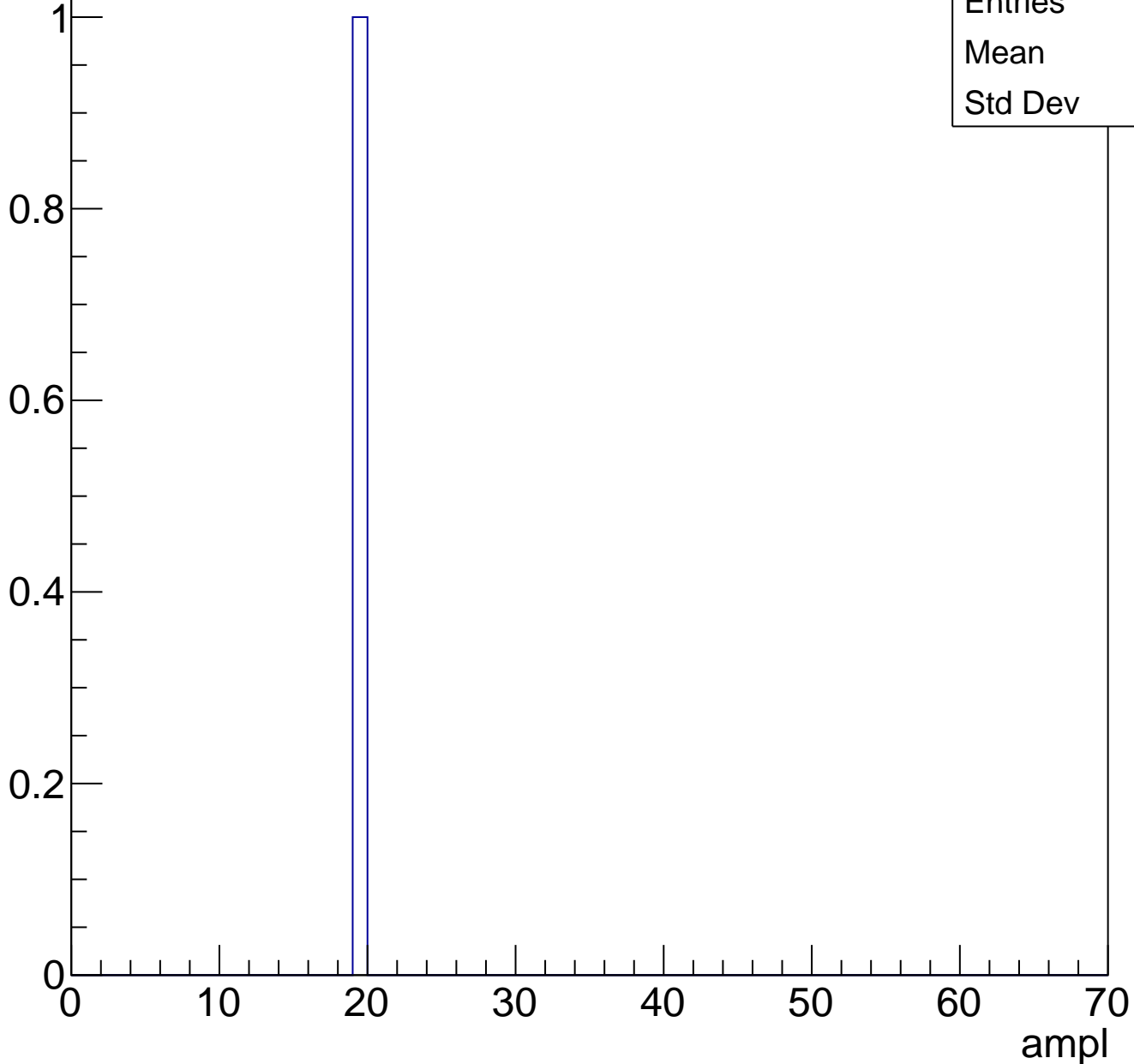




# B0L000S, U7-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch31, adc0

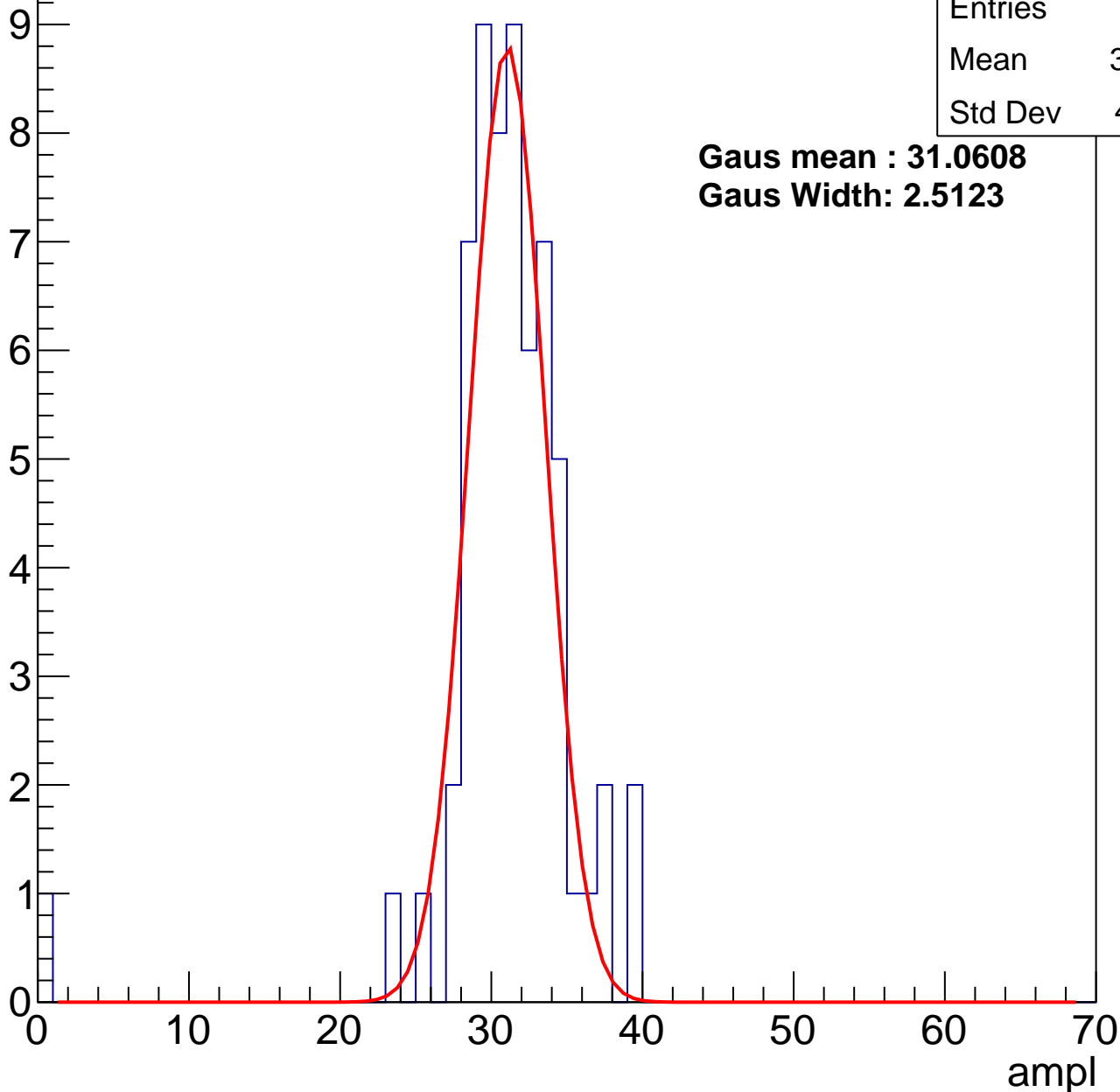
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	62
Mean	30.55
Std Dev	4.931

**Gaus mean : 31.0608**

**Gaus Width: 2.5123**



# B0L000S, U7-ch31, adc1

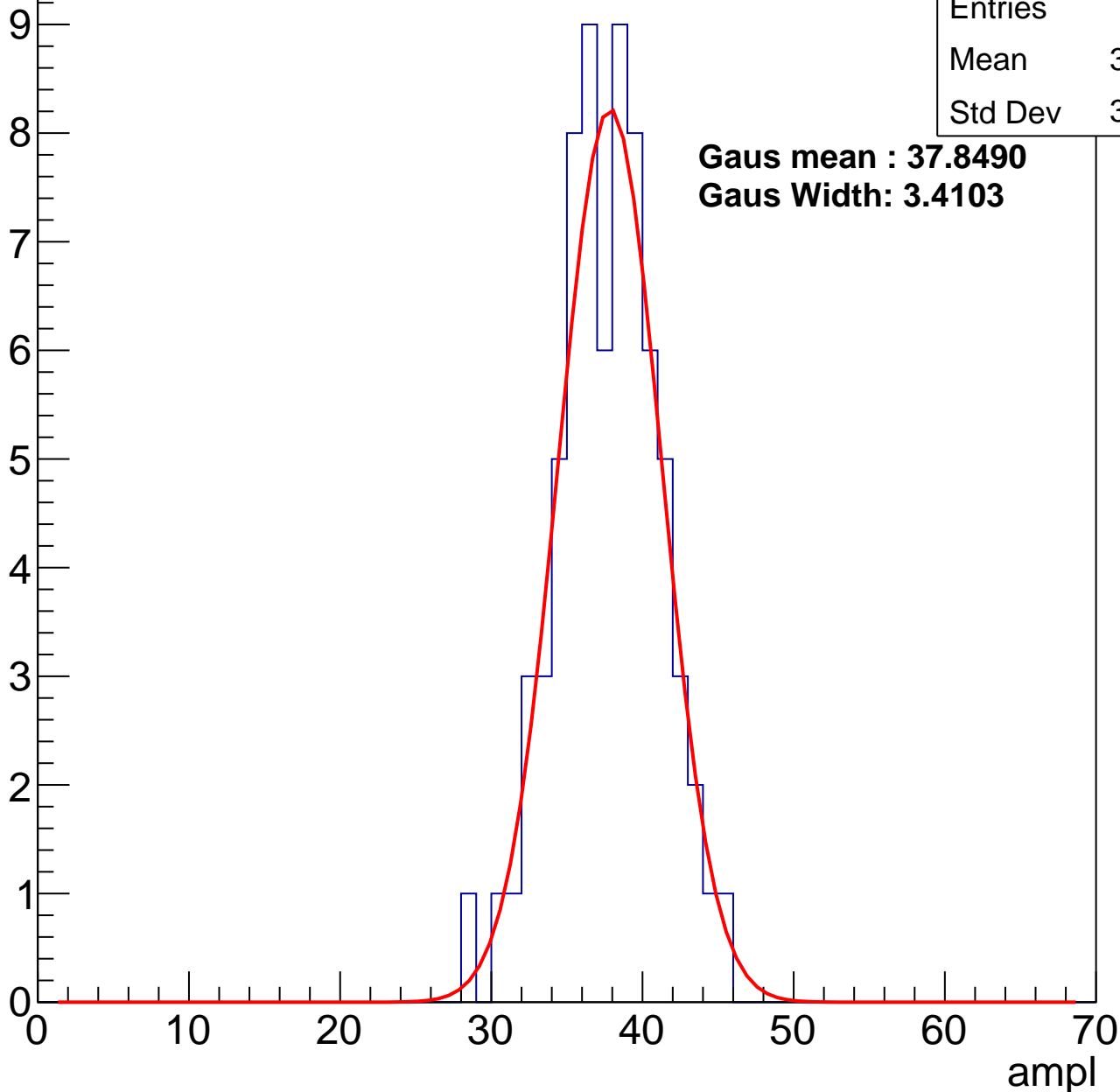
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	72
Mean	37.22
Std Dev	3.347

**Gaus mean : 37.8490**

**Gaus Width: 3.4103**



# B0L000S, U7-ch31, adc2

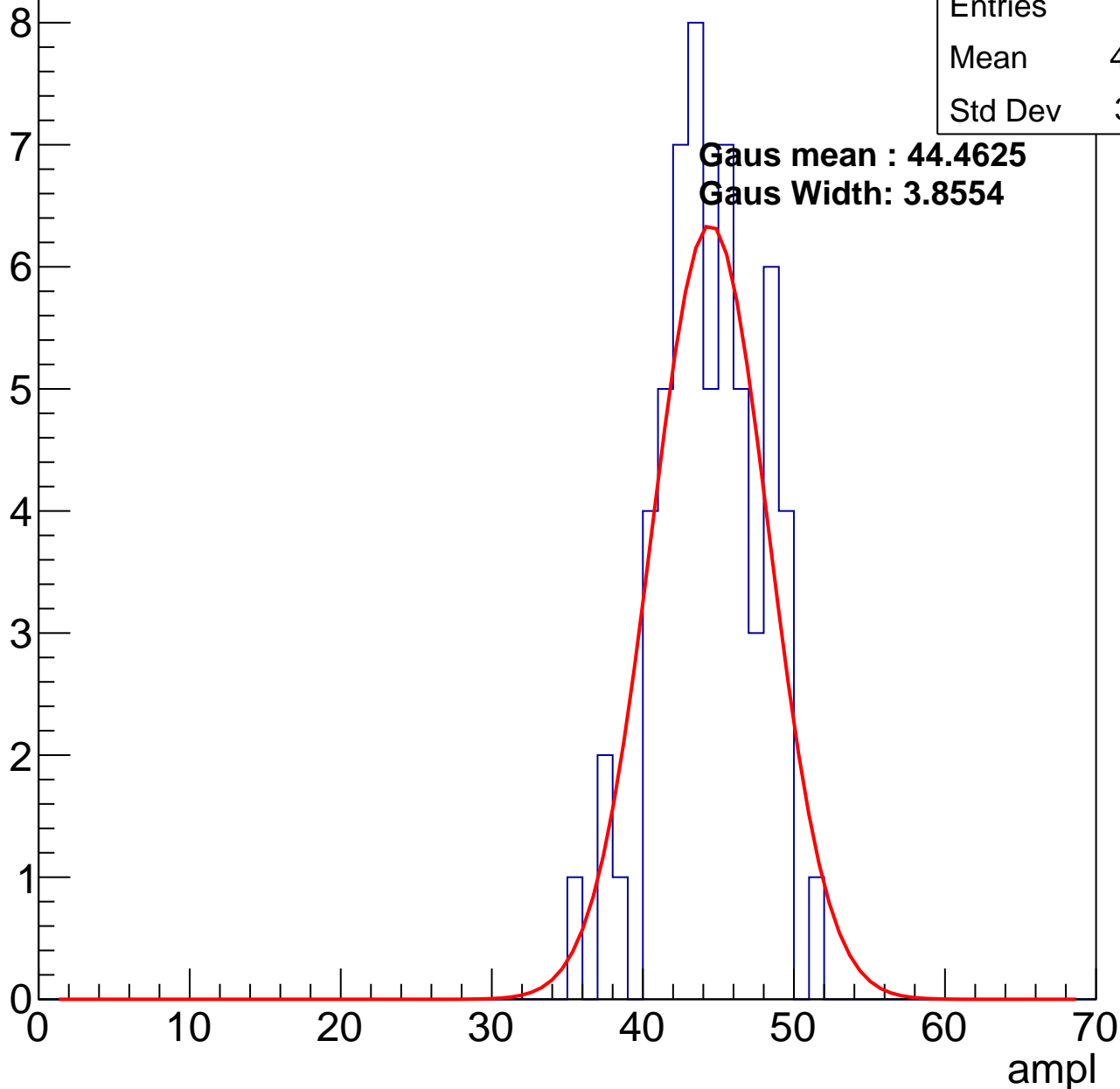
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	59
Mean	43.92
Std Dev	3.341

**Gaus mean : 44.4625**

**Gaus Width: 3.8554**

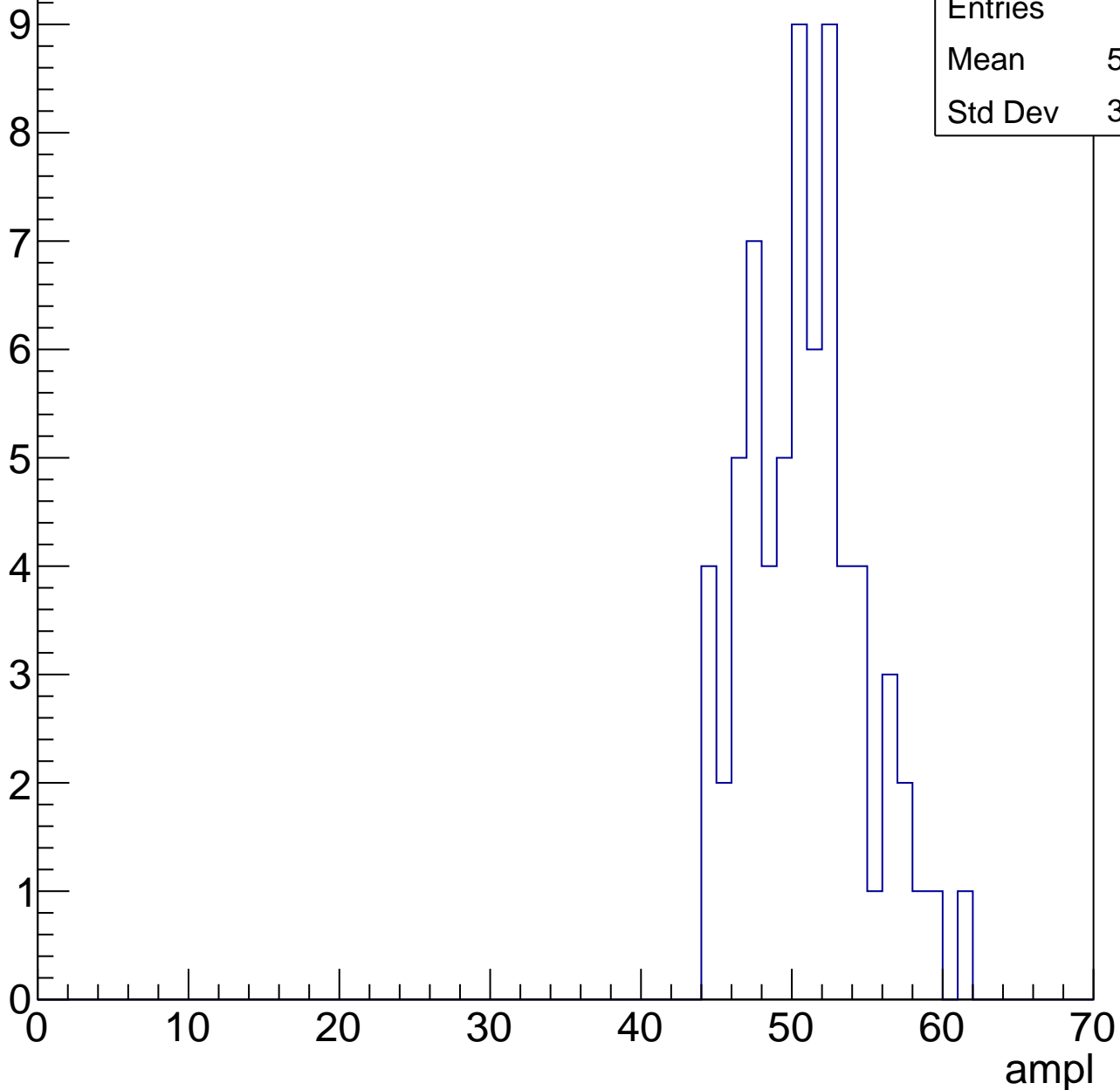


# B0L000S, U7-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	68
Mean	50.43
Std Dev	3.805

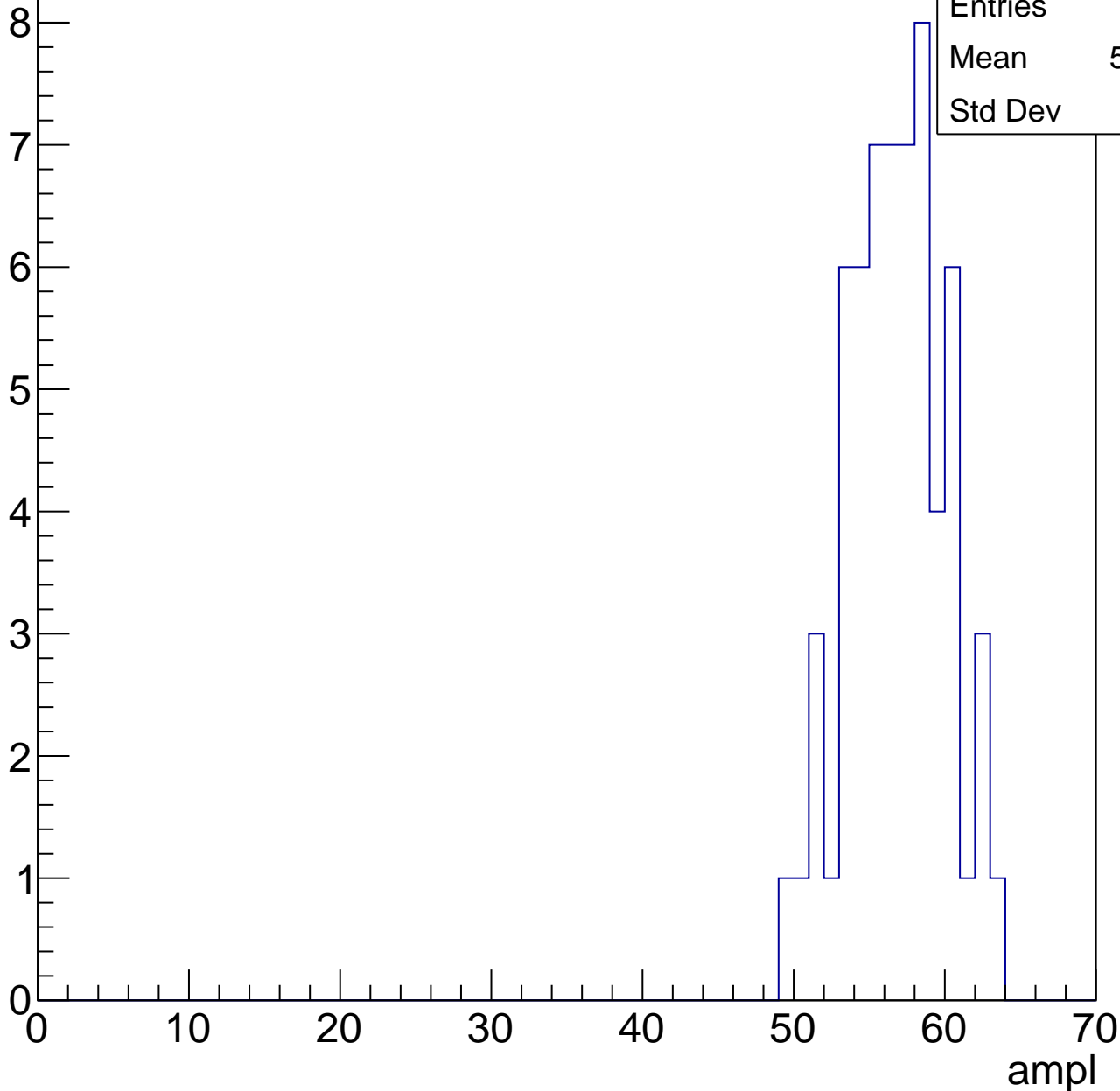


# B0L000S, U7-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	62
Mean	56.32
Std Dev	3.13

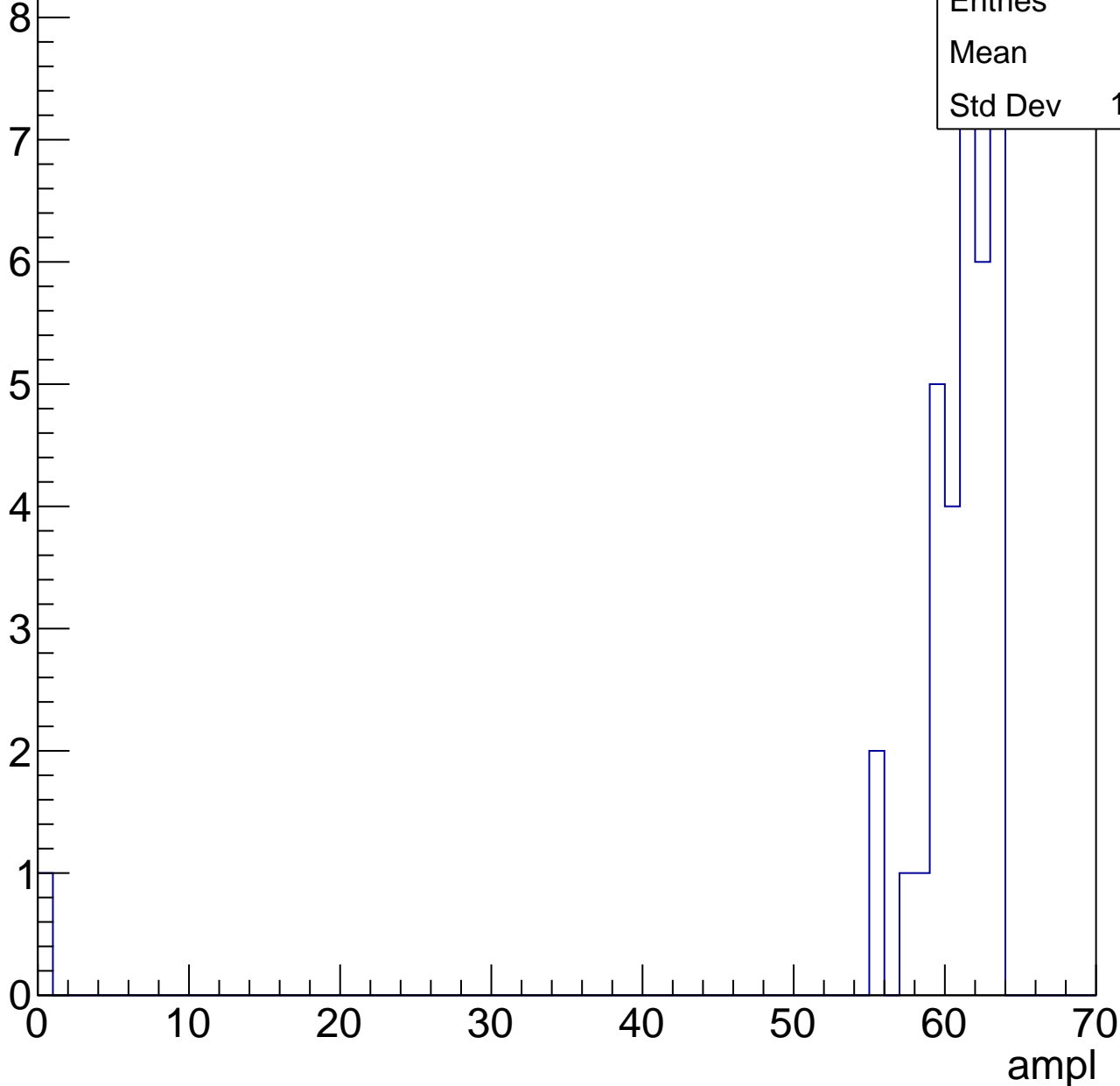


# B0L000S, U7-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

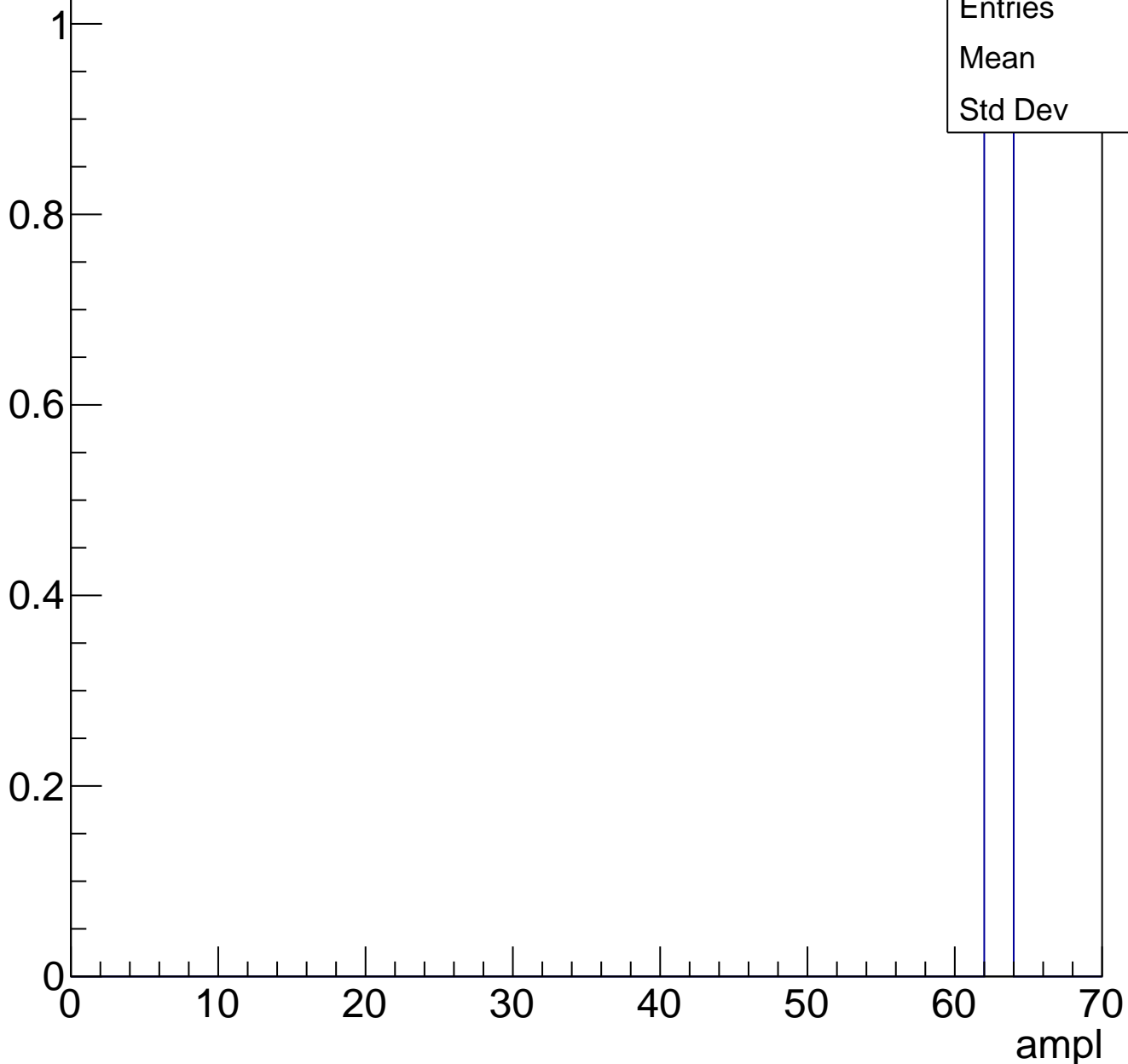
Entries	36
Mean	59
Std Dev	10.19



# B0L000S, U7-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L000S, U7-ch32, adc0

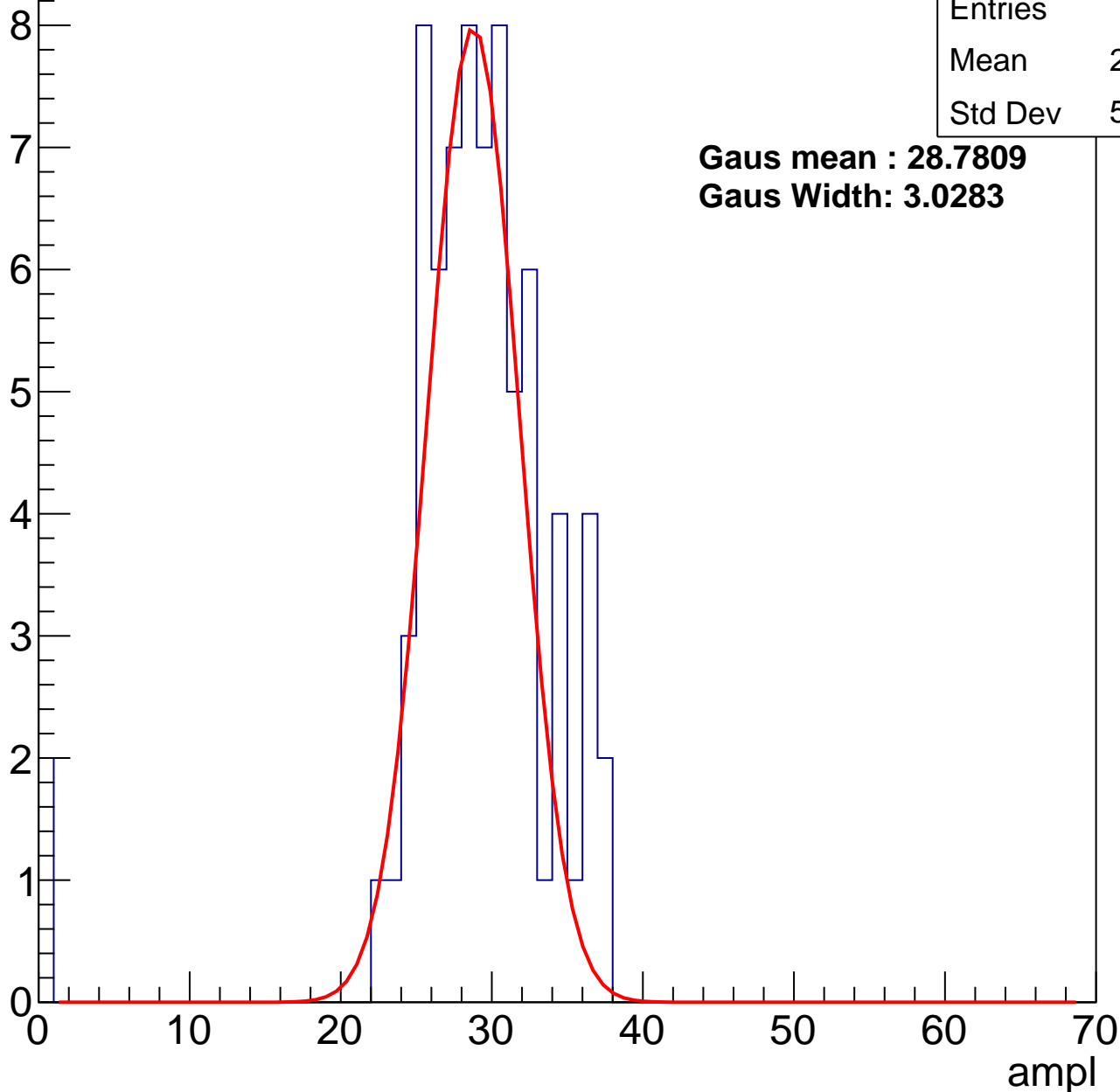
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	74
Mean	28.35
Std Dev	5.912

**Gaus mean : 28.7809**

**Gaus Width: 3.0283**



# B0L000S, U7-ch32, adc1

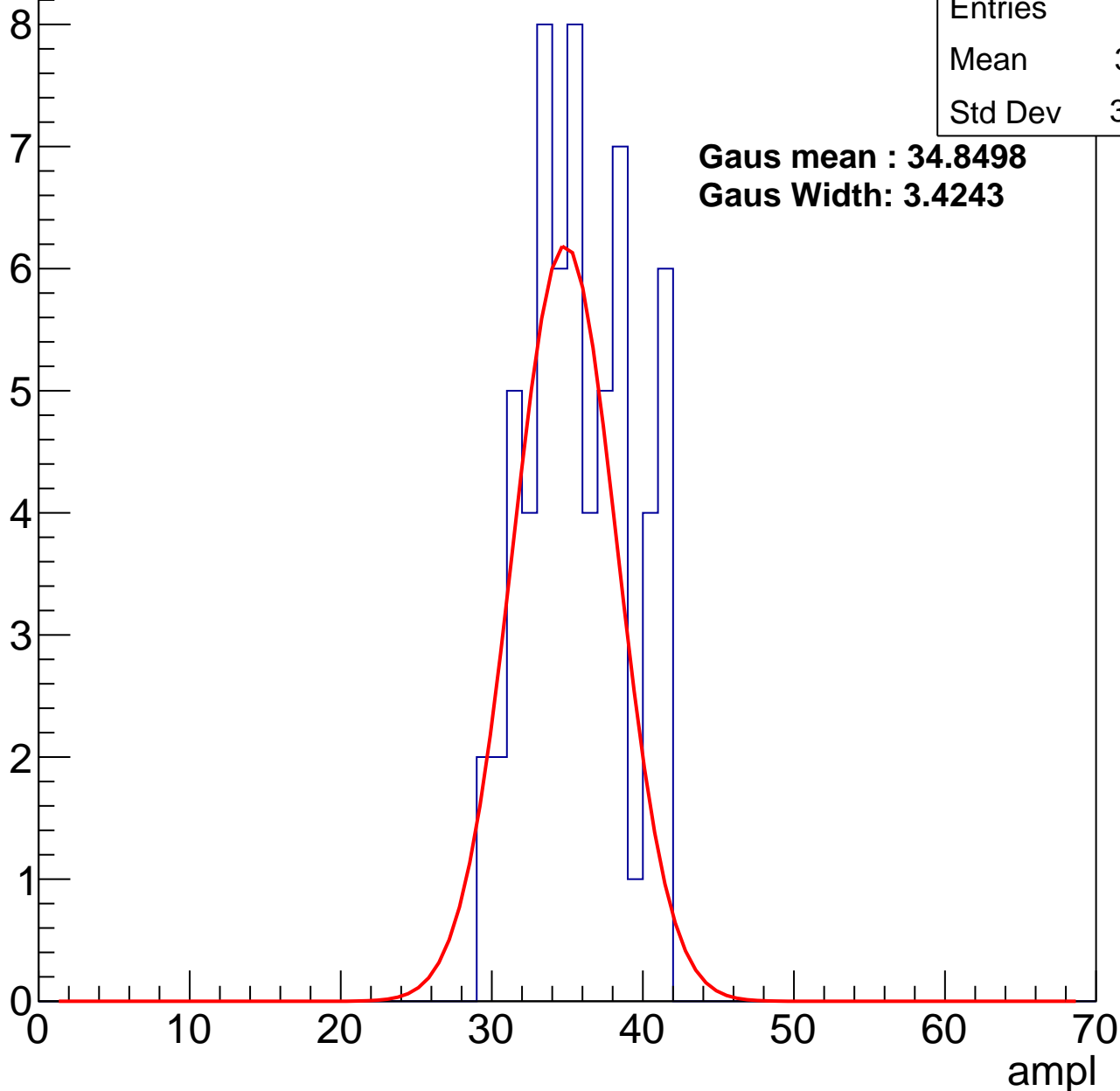
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	62
Mean	35.31
Std Dev	3.334

**Gaus mean : 34.8498**

**Gaus Width: 3.4243**



# B0L000S, U7-ch32, adc2

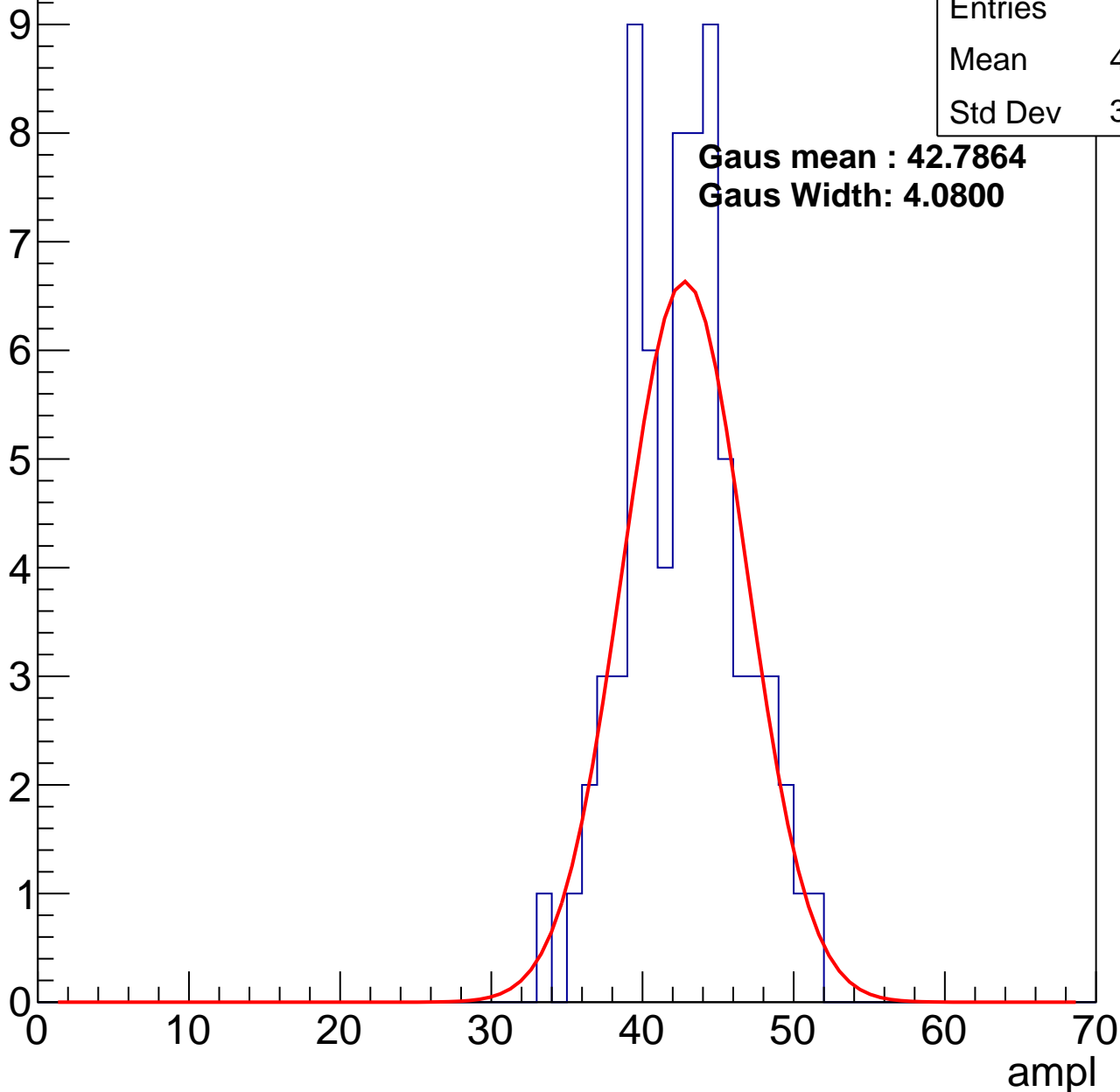
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	72
Mean	42.26
Std Dev	3.712

**Gaus mean : 42.7864**

**Gaus Width: 4.0800**

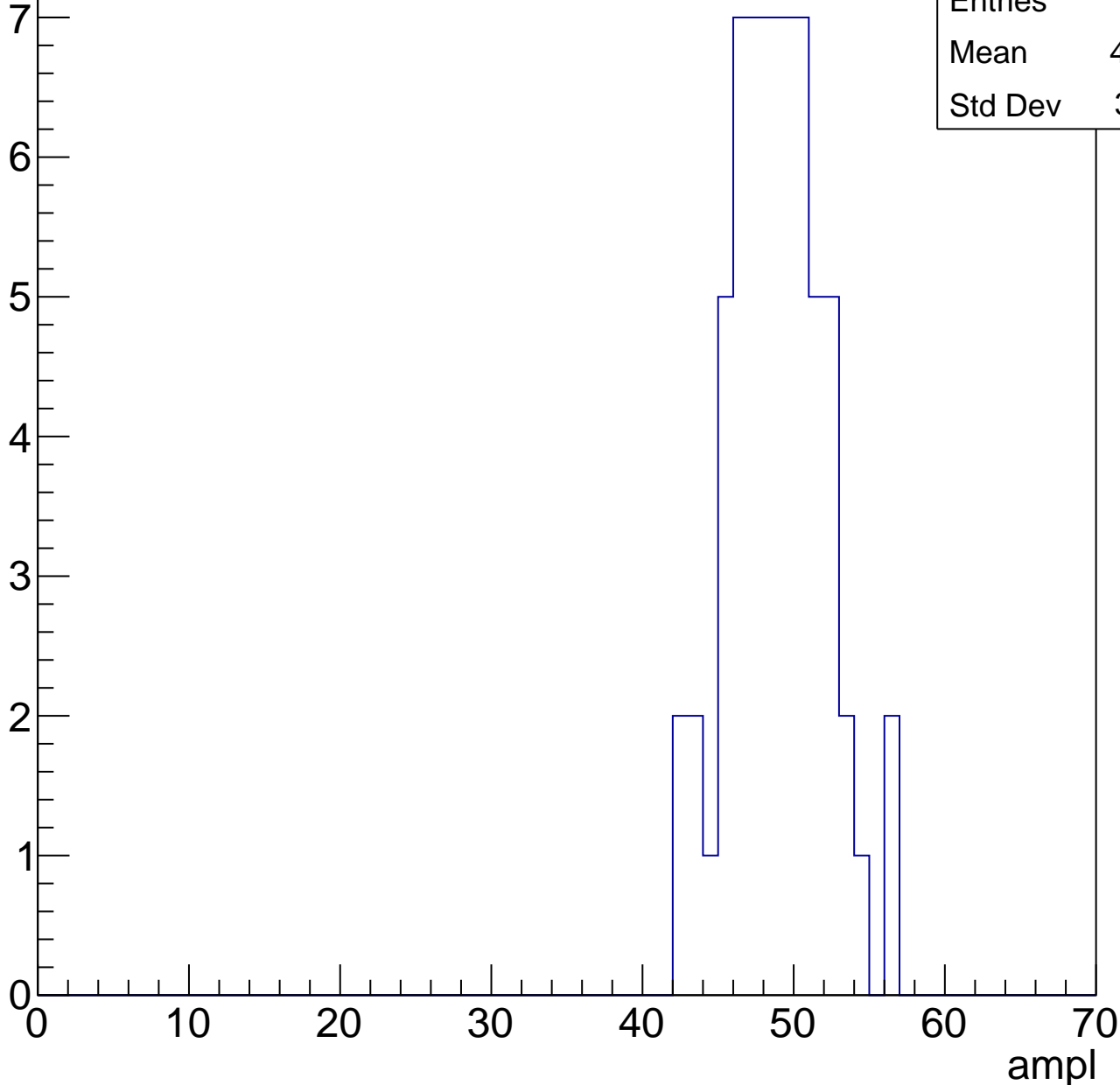


# B0L000S, U7-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	60
Mean	48.43
Std Dev	3.111

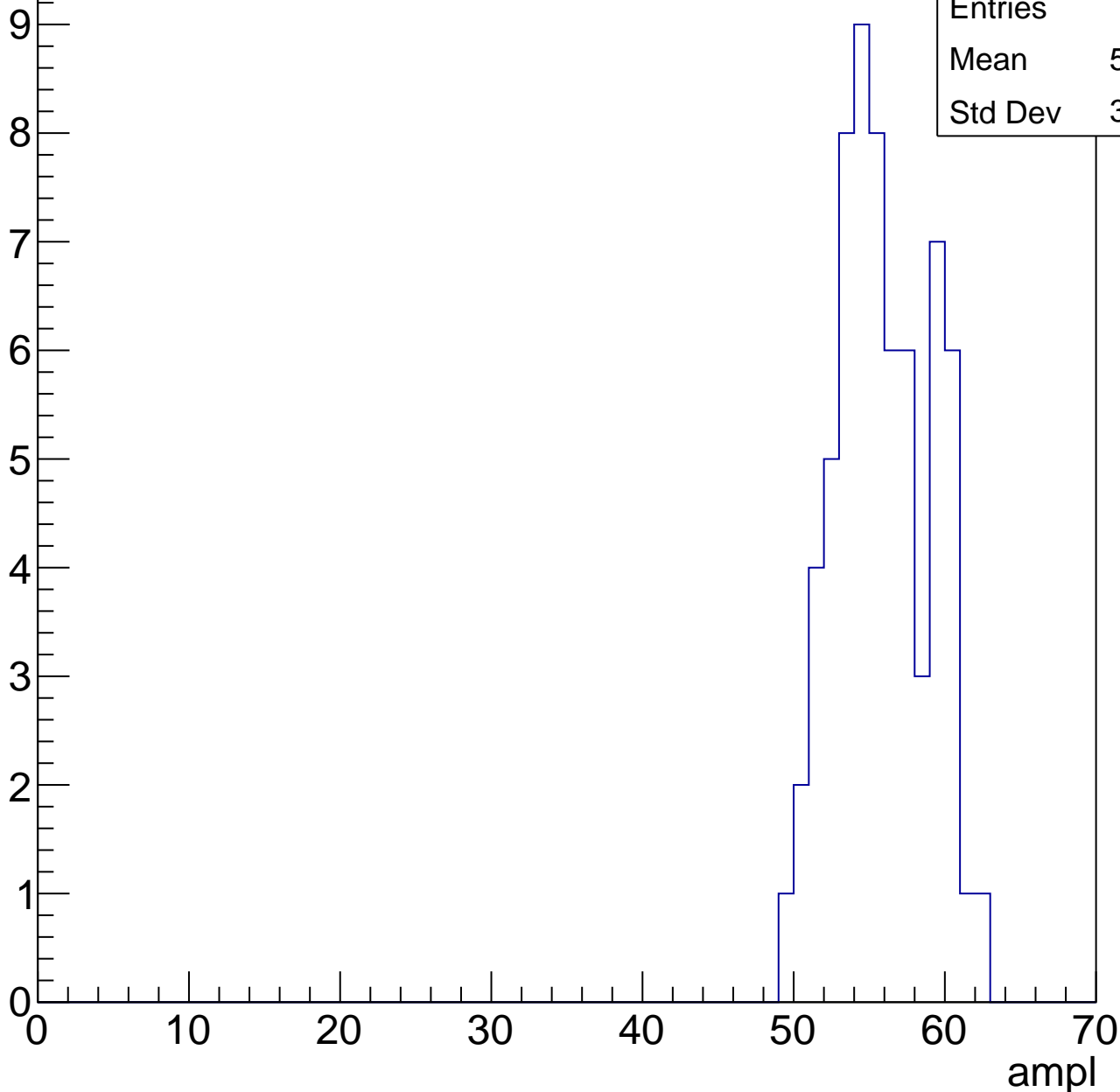


# B0L000S, U7-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	67
Mean	55.39
Std Dev	3.066



# B0L000S, U7-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

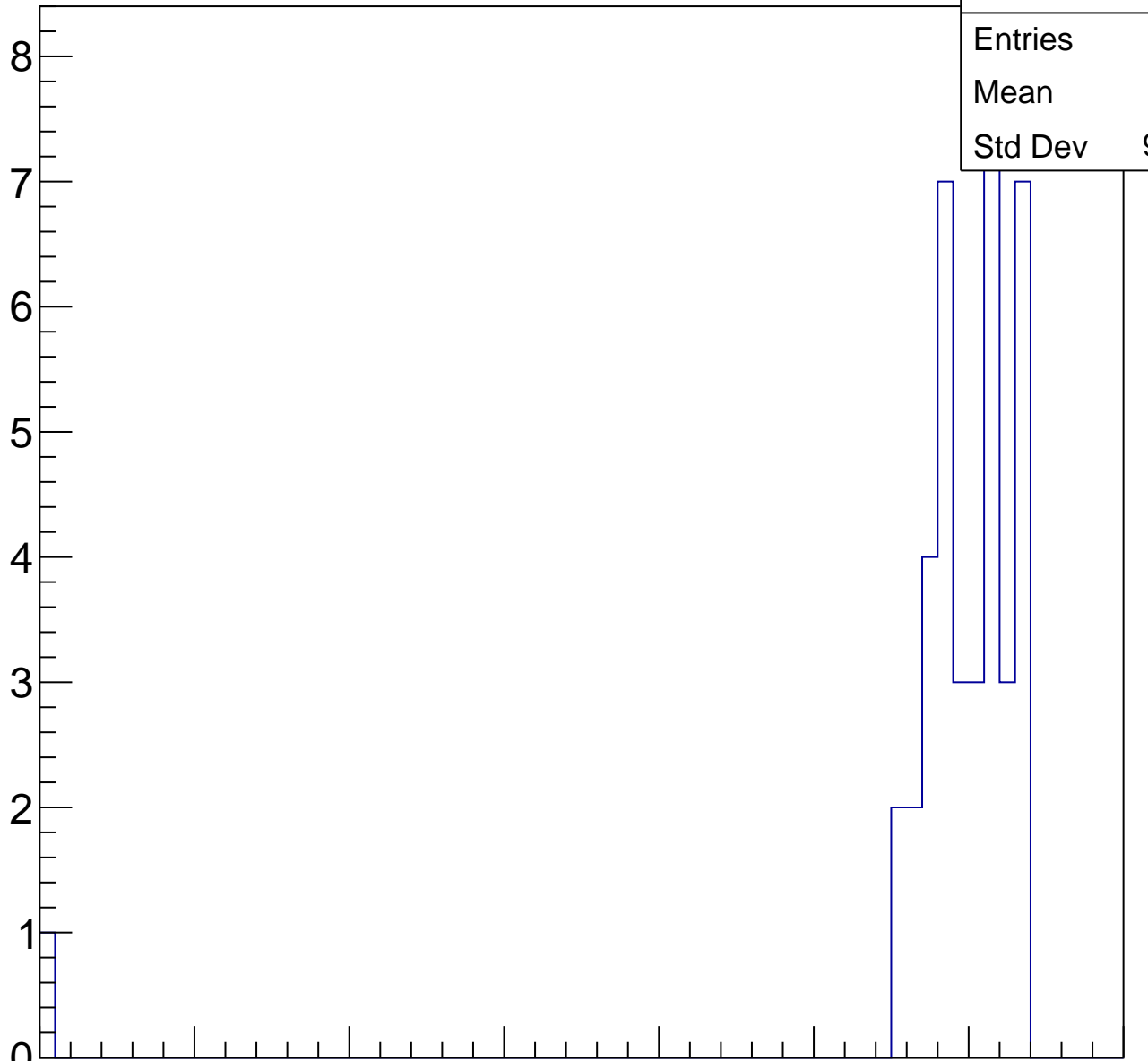
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	40
Mean	58.2
Std Dev	9.621

ampl

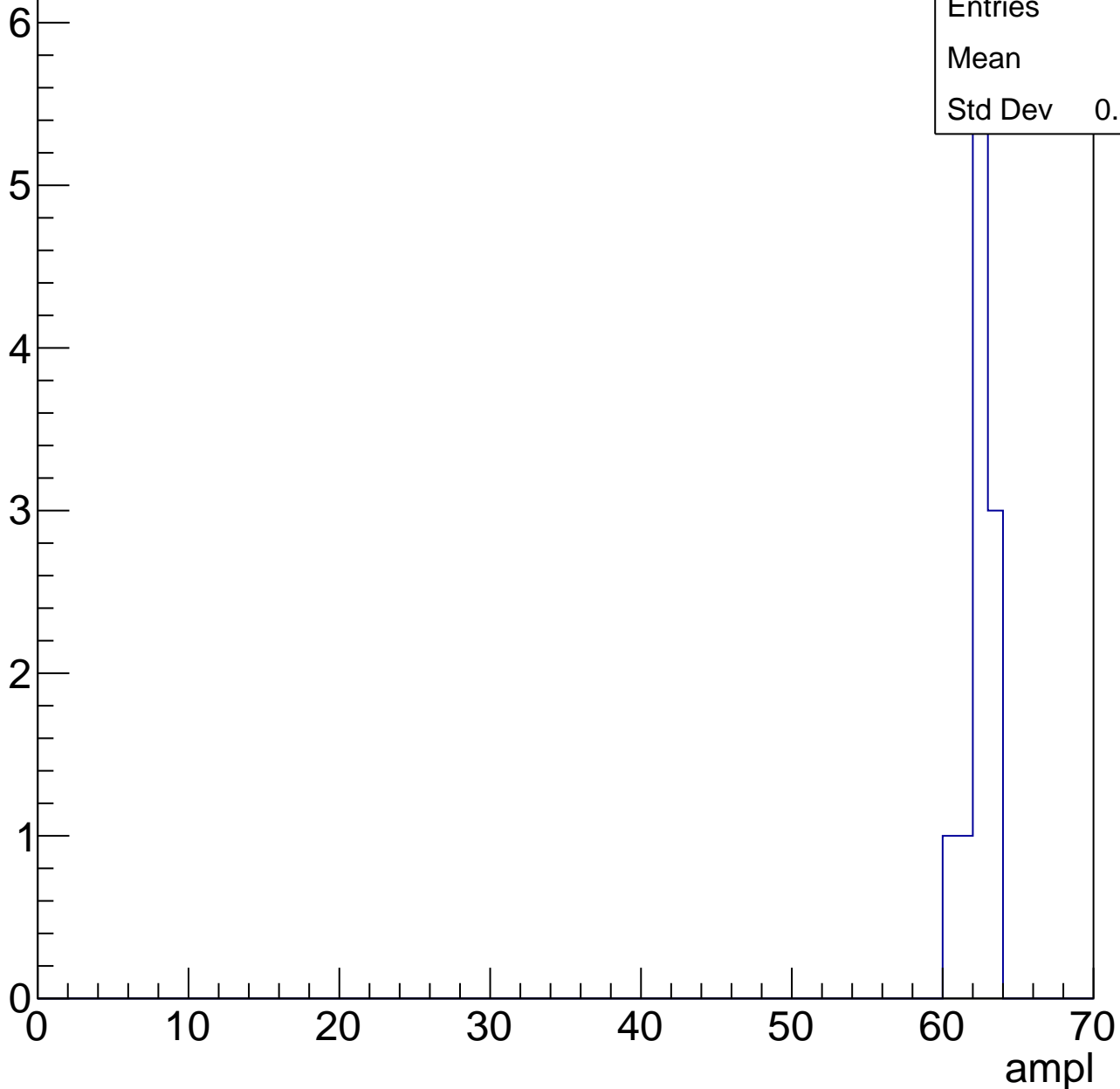
0 10 20 30 40 50 60 70



# B0L000S, U7-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch33, adc0

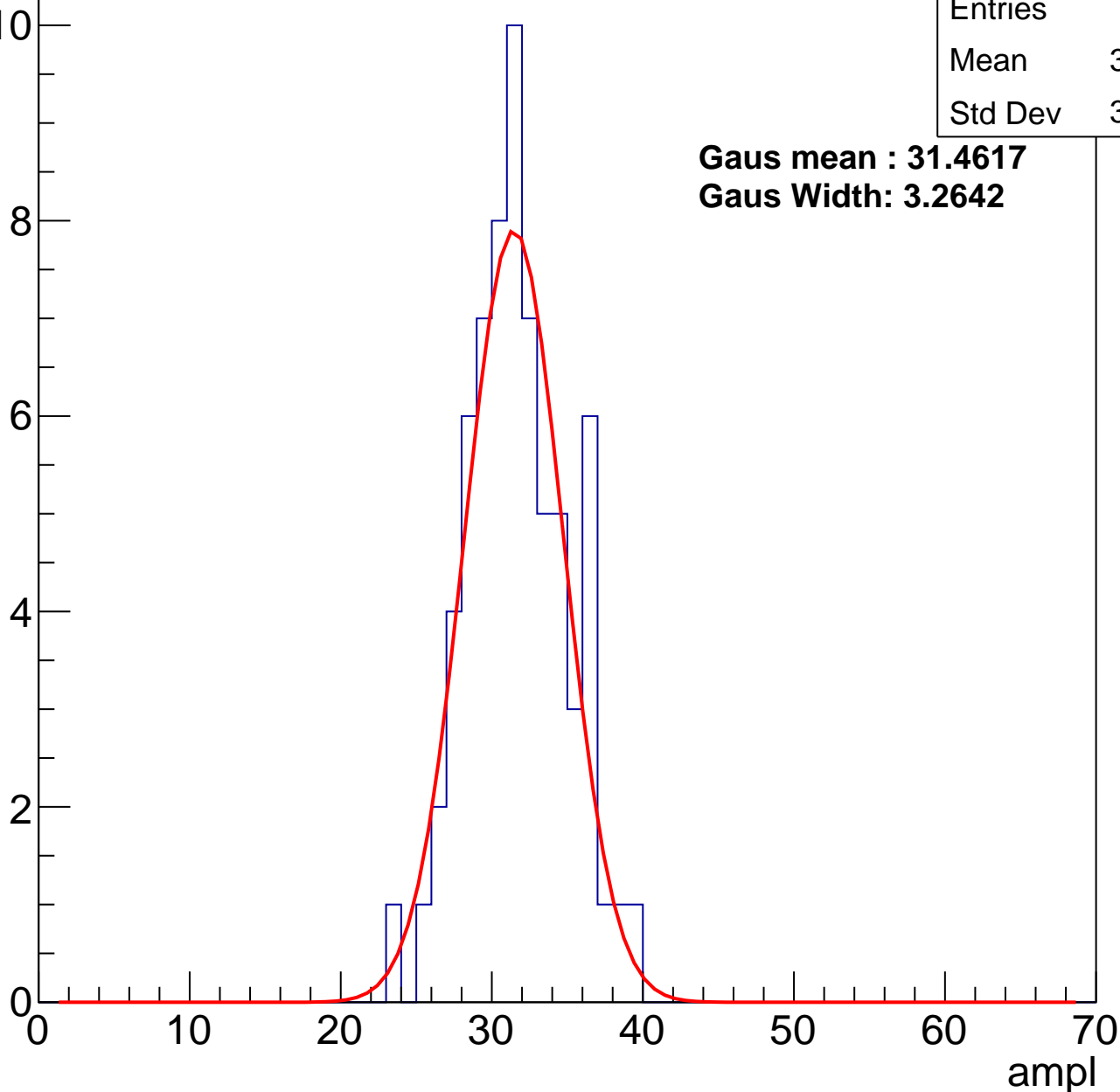
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	68
Mean	31.22
Std Dev	3.253

**Gaus mean : 31.4617**

**Gaus Width: 3.2642**



# B0L000S, U7-ch33, adc1

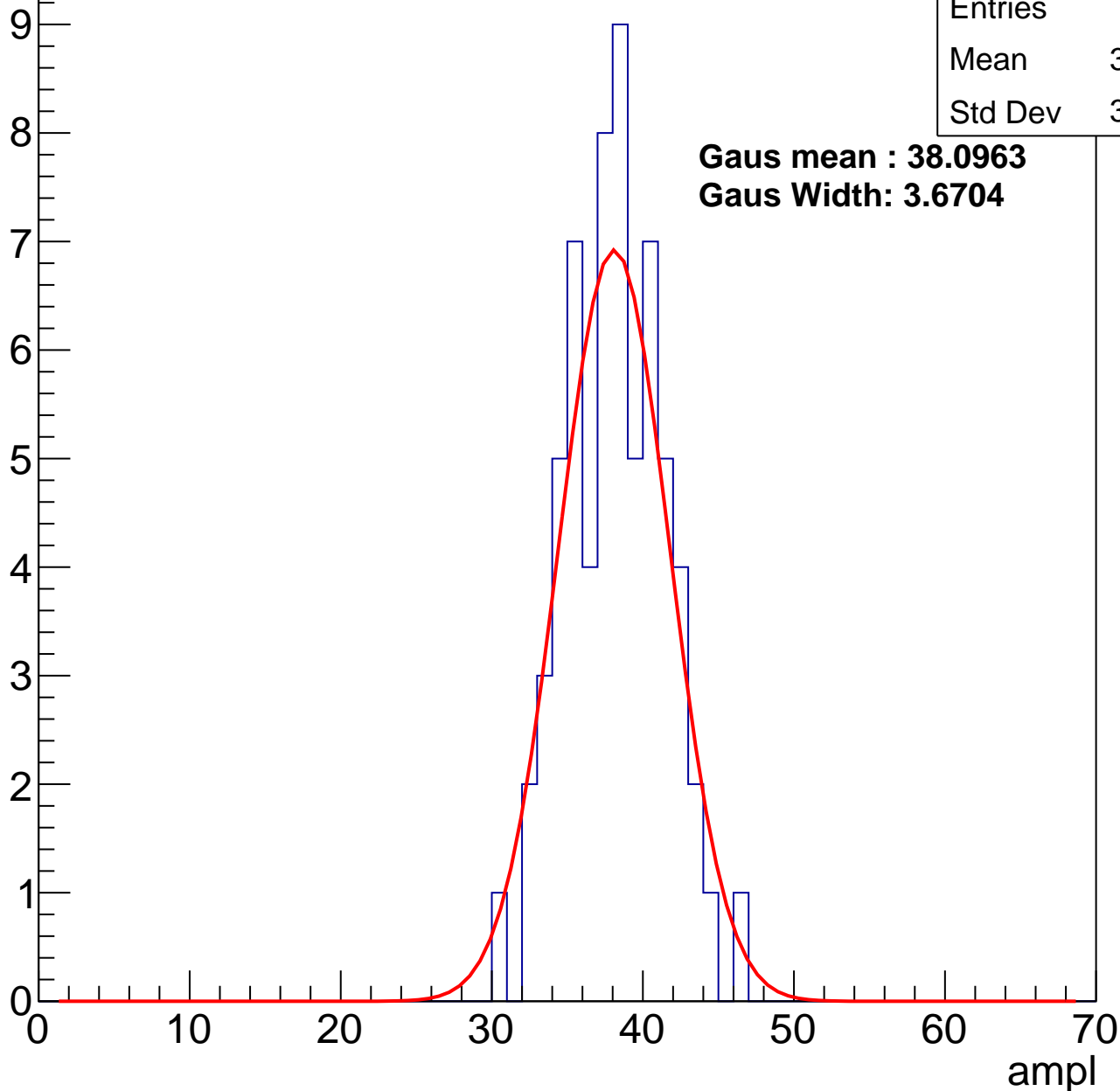
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	64
Mean	37.72
Std Dev	3.223

**Gaus mean : 38.0963**

**Gaus Width: 3.6704**



# B0L000S, U7-ch33, adc2

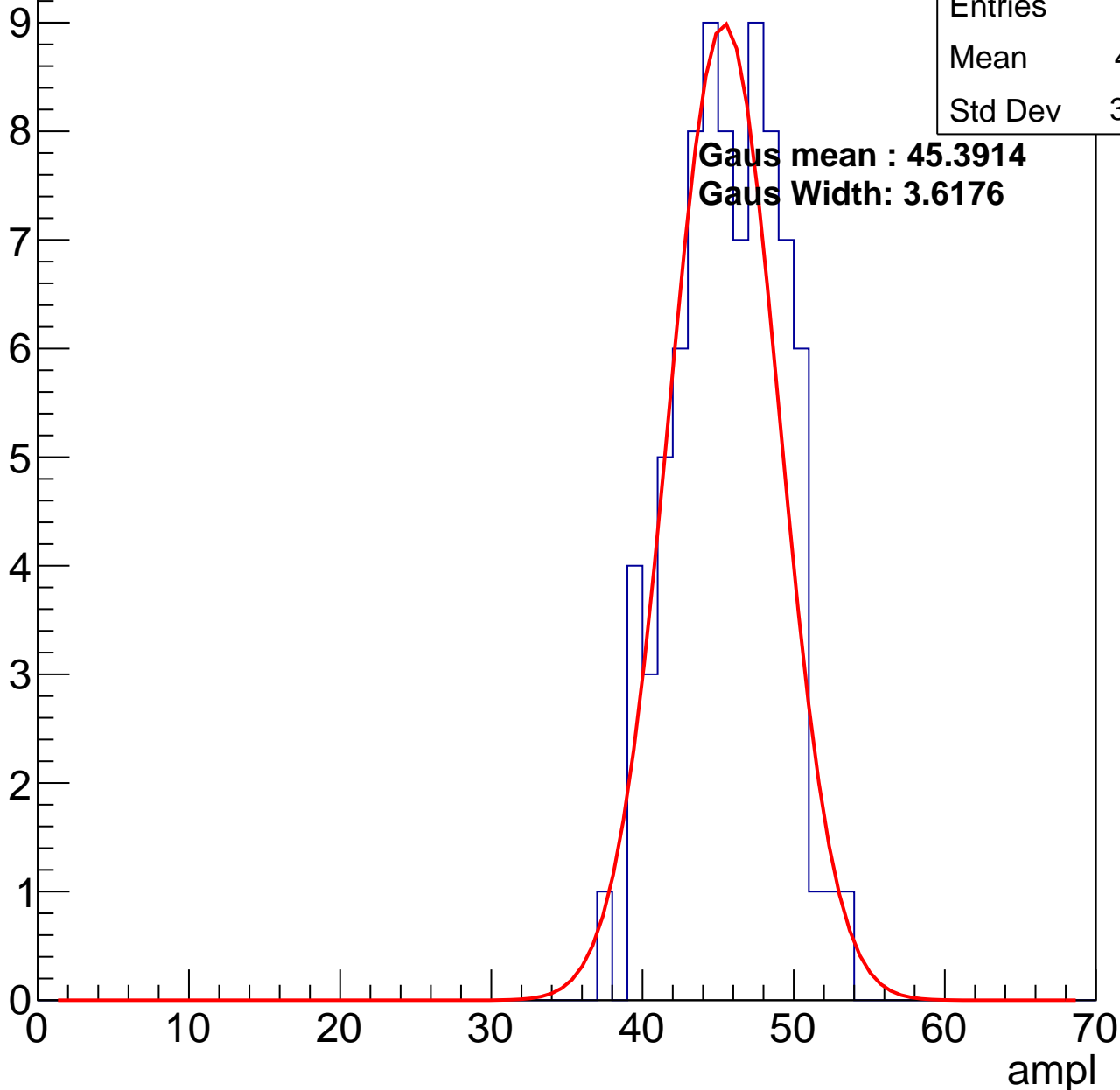
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	84
Mean	45.21
Std Dev	3.416

**Gaus mean : 45.3914**

**Gaus Width: 3.6176**

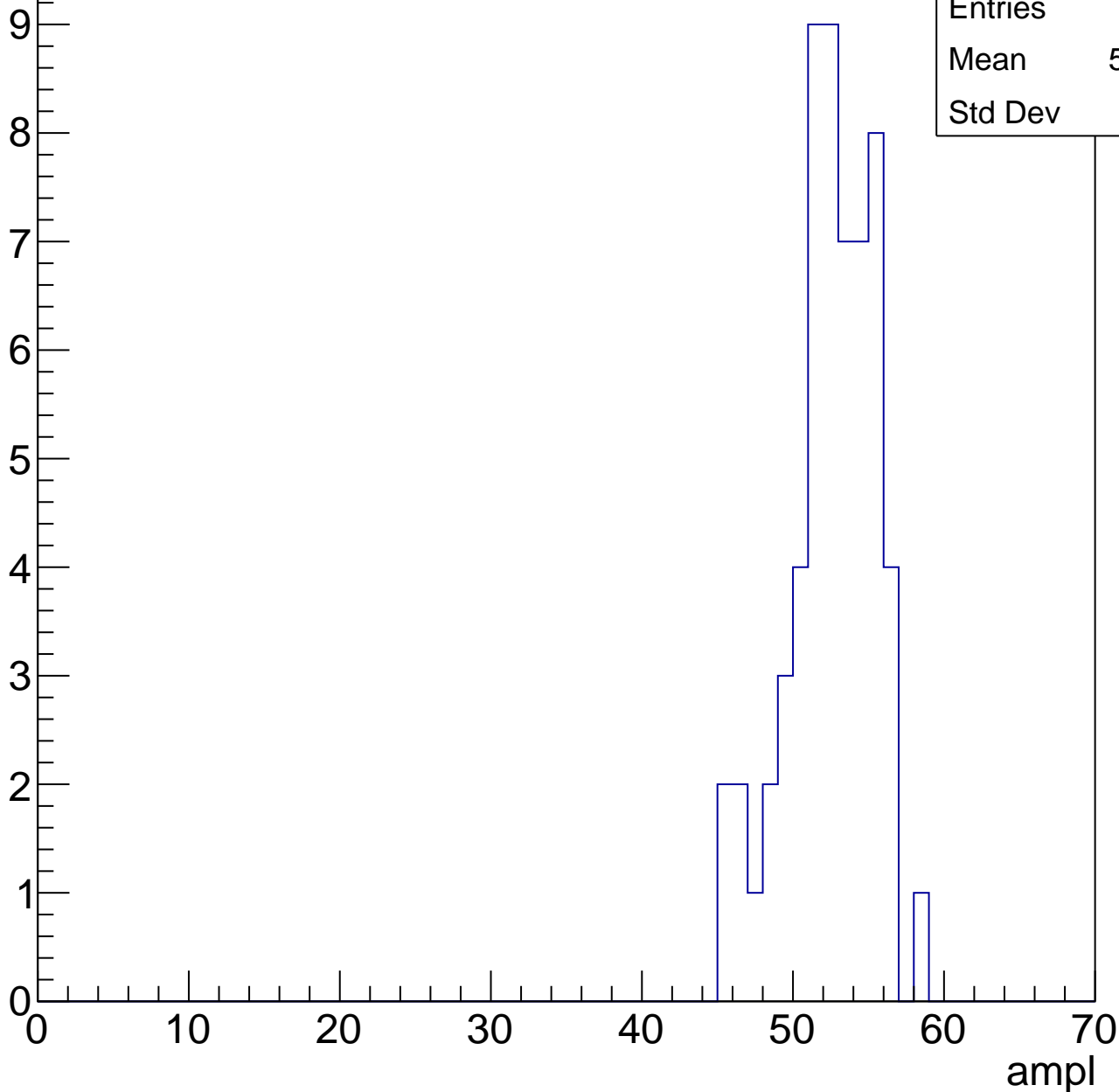


# B0L000S, U7-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	59
Mean	52.03
Std Dev	2.87

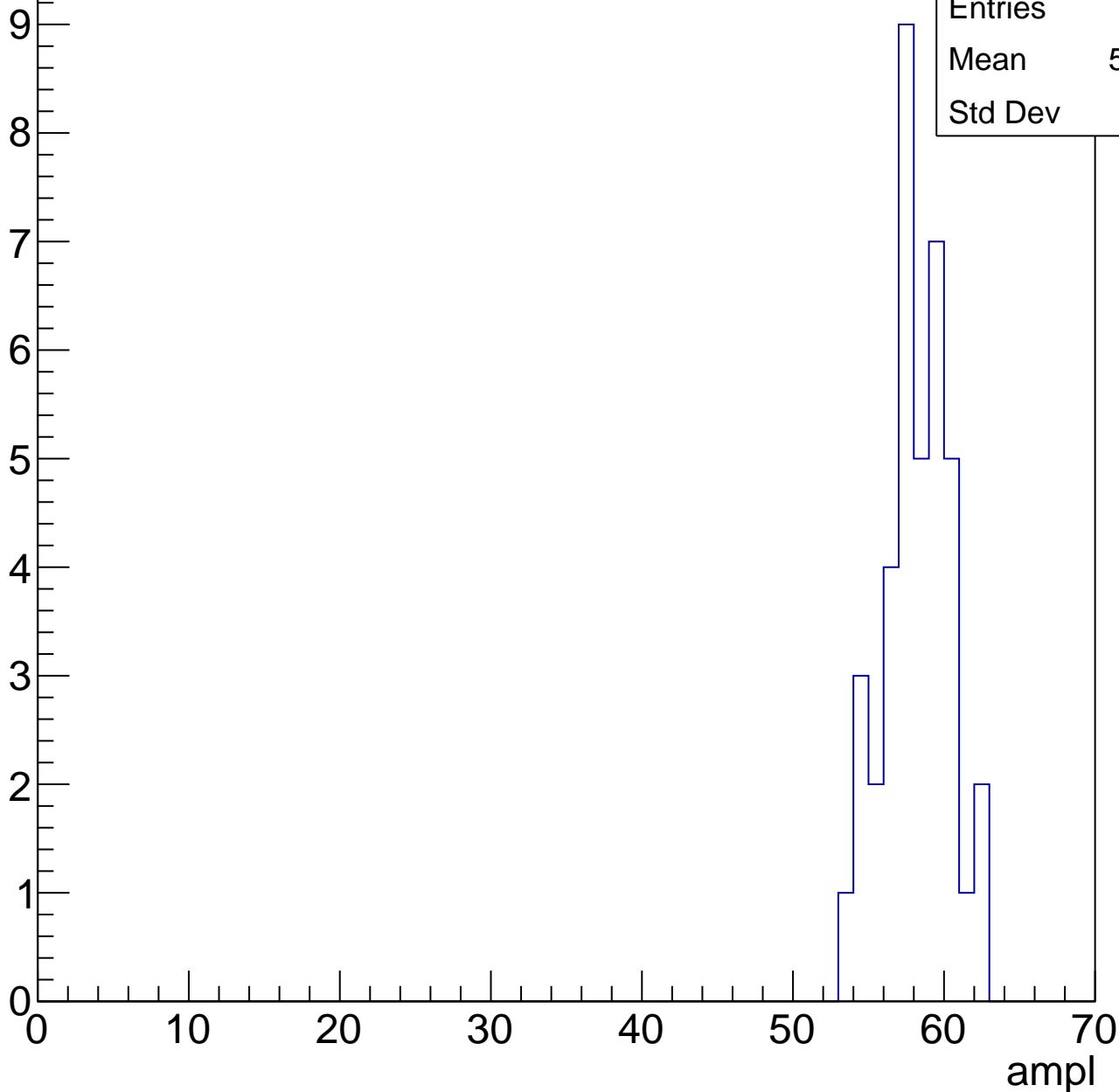


# B0L000S, U7-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	39
Mean	57.69
Std Dev	2.15



# B0L000S, U7-ch33, adc5

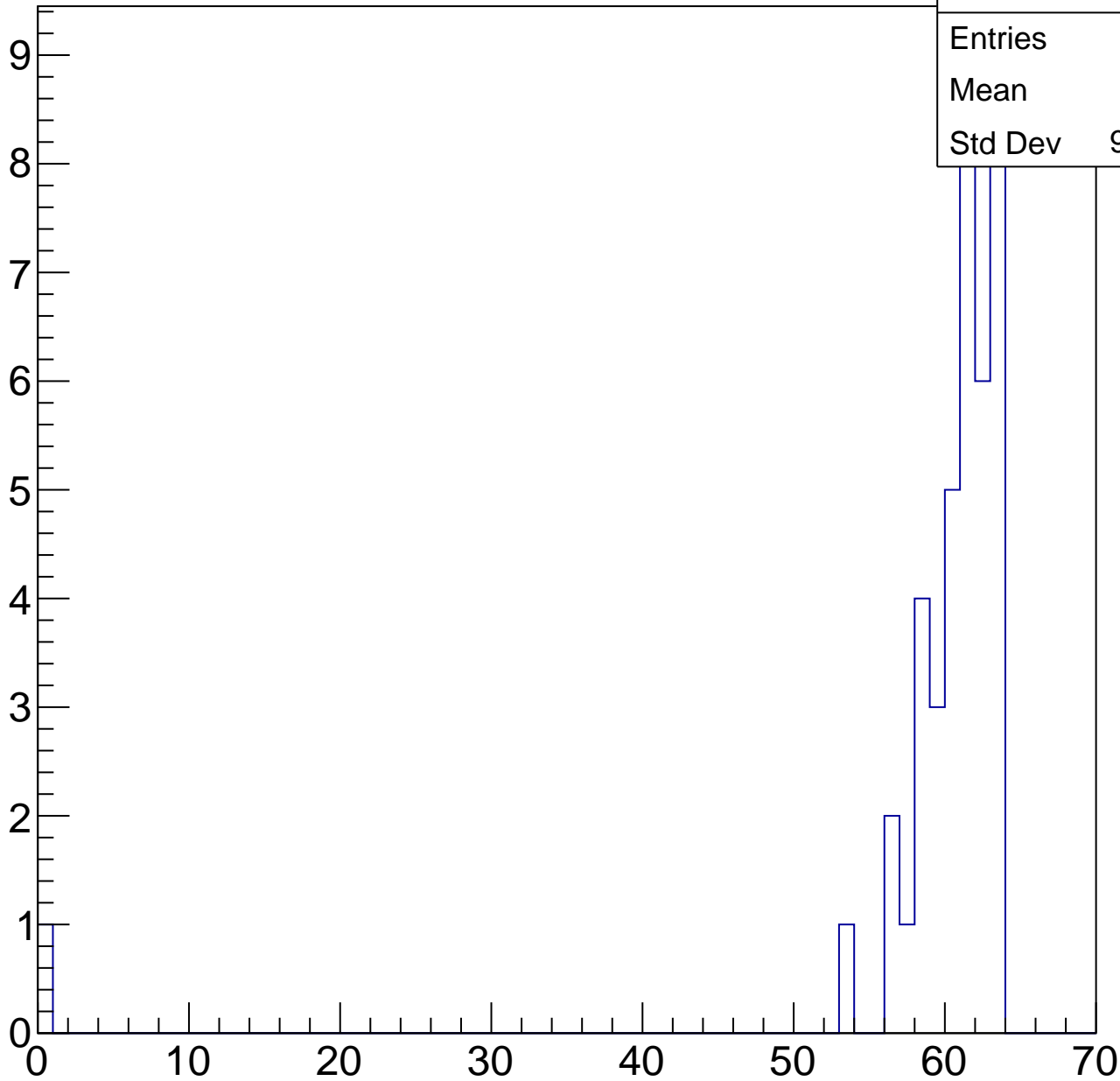
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	41
Mean	59
Std Dev	9.604

ampl



# B0L000S, U7-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.4714

ampl



# B0L000S, U7-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch34, adc0

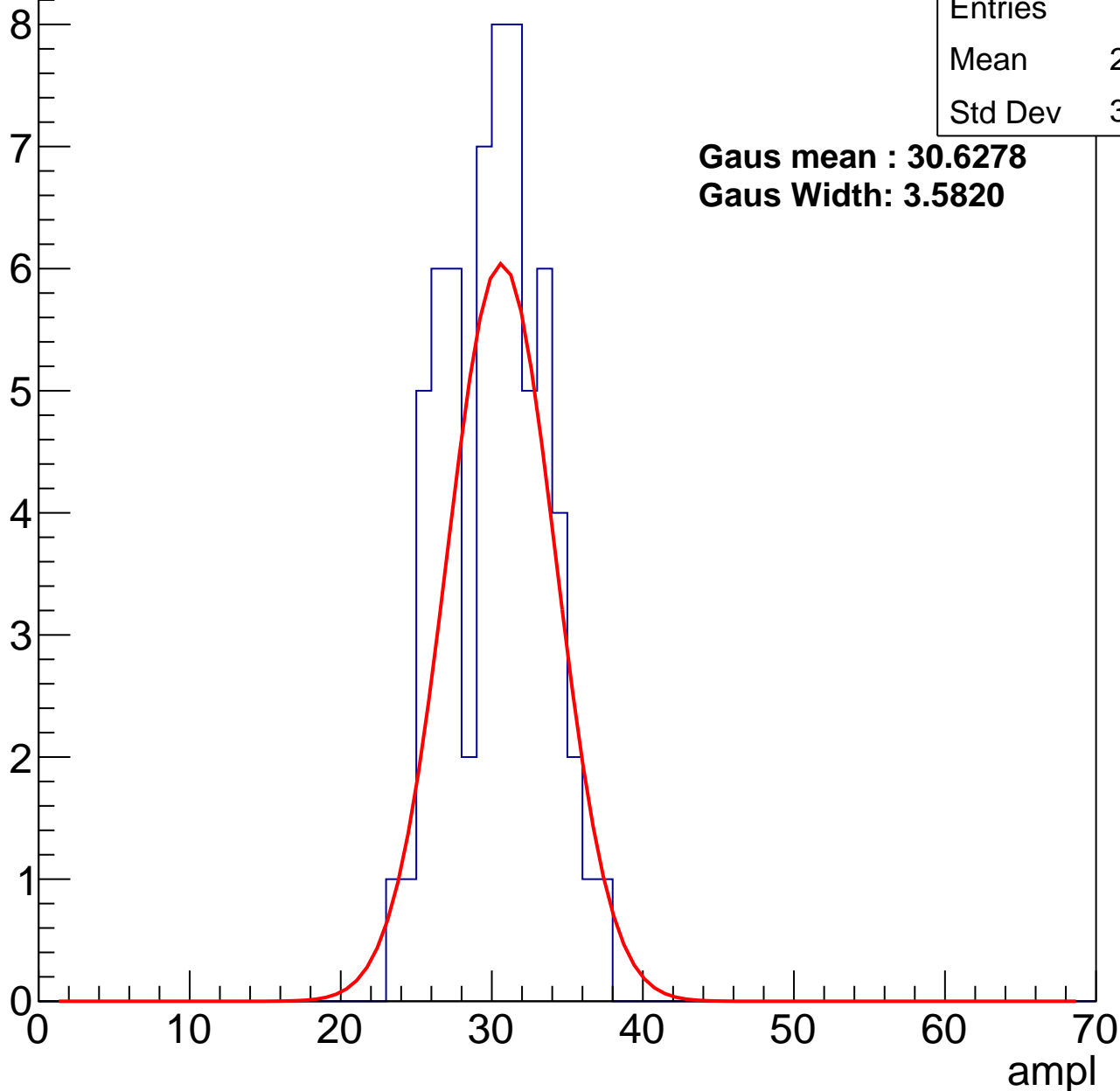
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	63
Mean	29.75
Std Dev	3.217

**Gaus mean : 30.6278**

**Gaus Width: 3.5820**



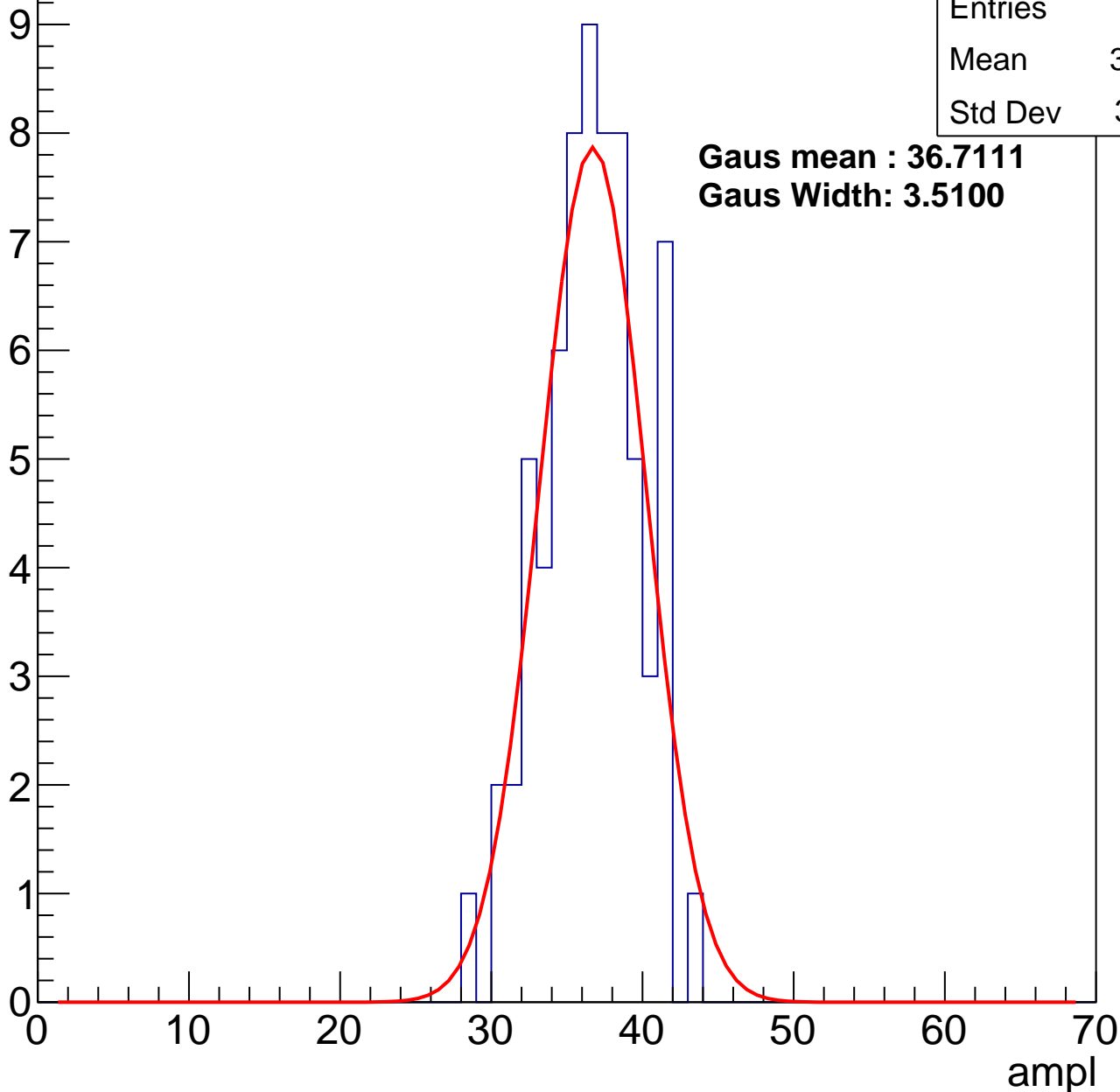
# B0L000S, U7-ch34, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	69
Mean	36.16
Std Dev	3.161

**Gaus mean : 36.7111**  
**Gaus Width: 3.5100**



# B0L000S, U7-ch34, adc2

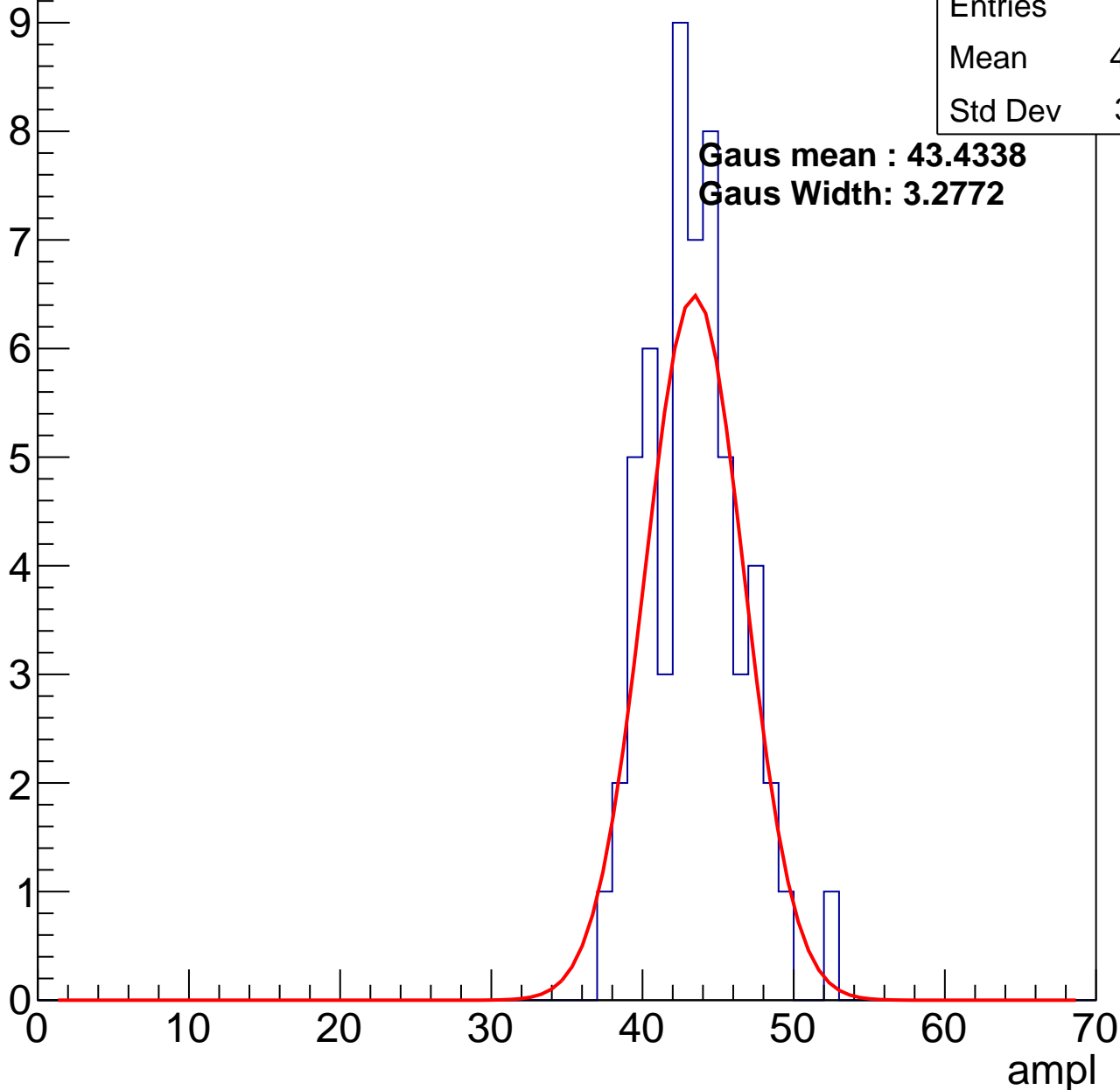
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	57
Mean	42.98
Std Dev	3.041

**Gaus mean : 43.4338**

**Gaus Width: 3.2772**

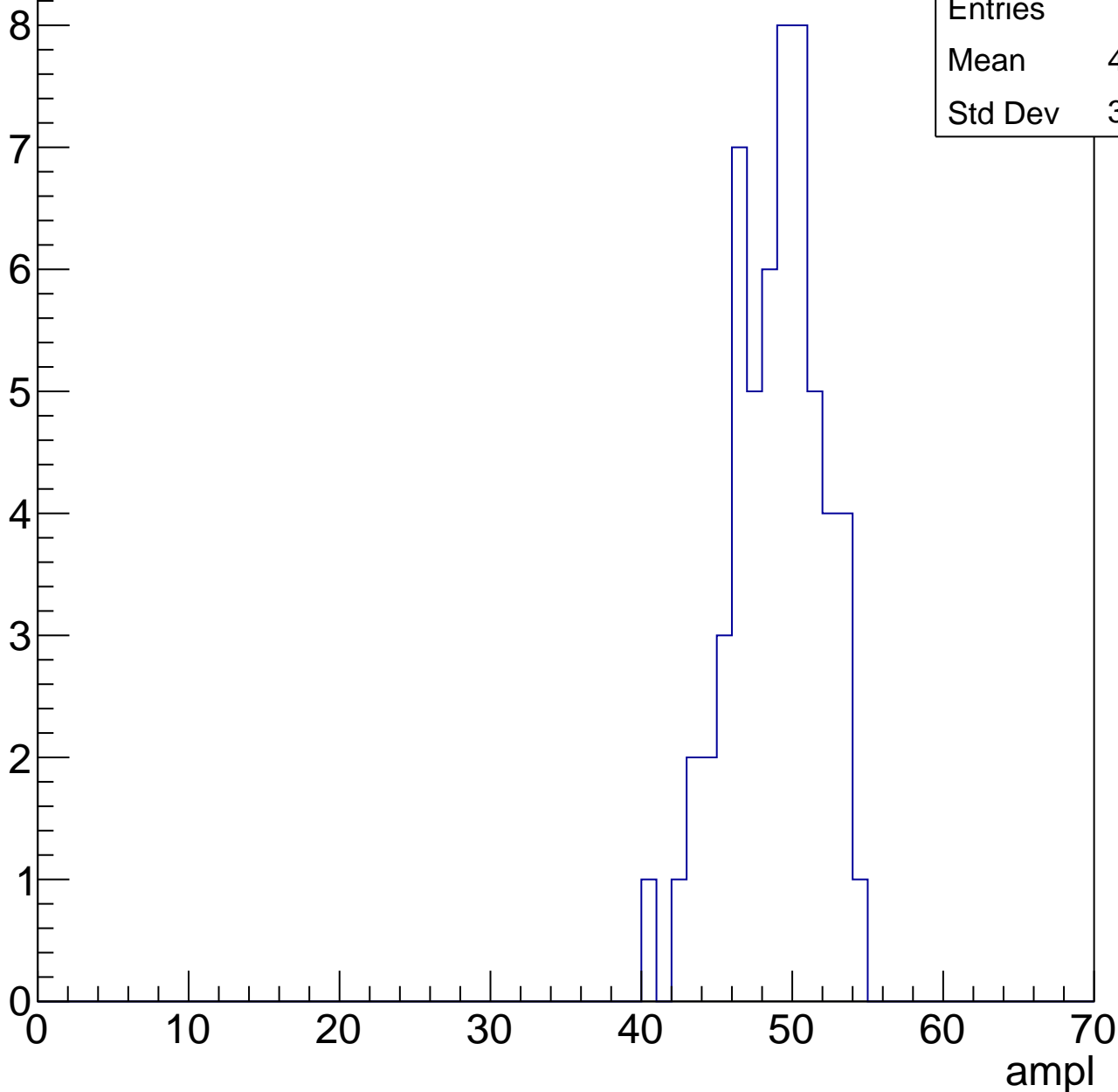


# B0L000S, U7-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	57
Mean	48.37
Std Dev	3.018

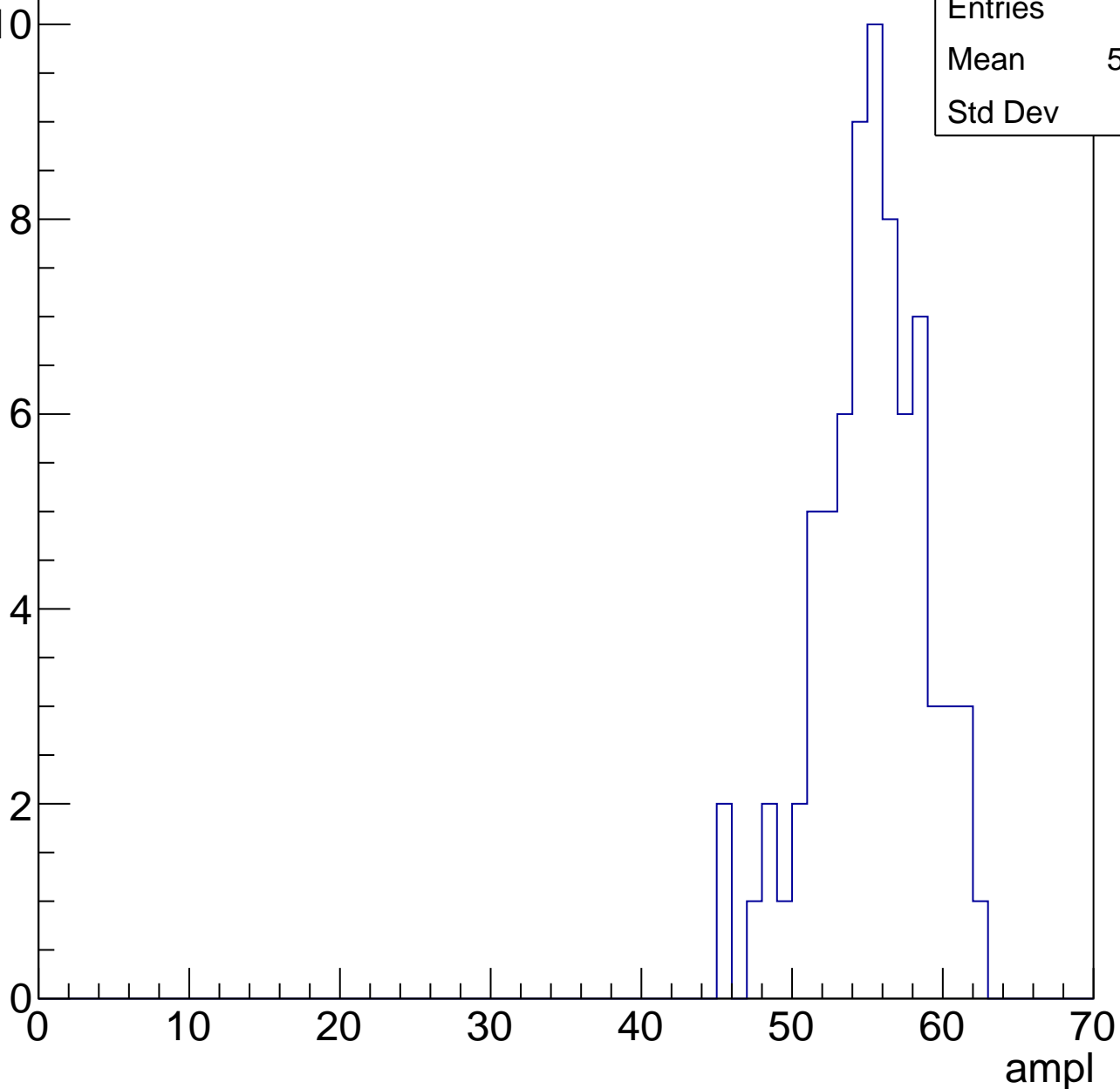


# B0L000S, U7-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	74
Mean	54.72
Std Dev	3.63

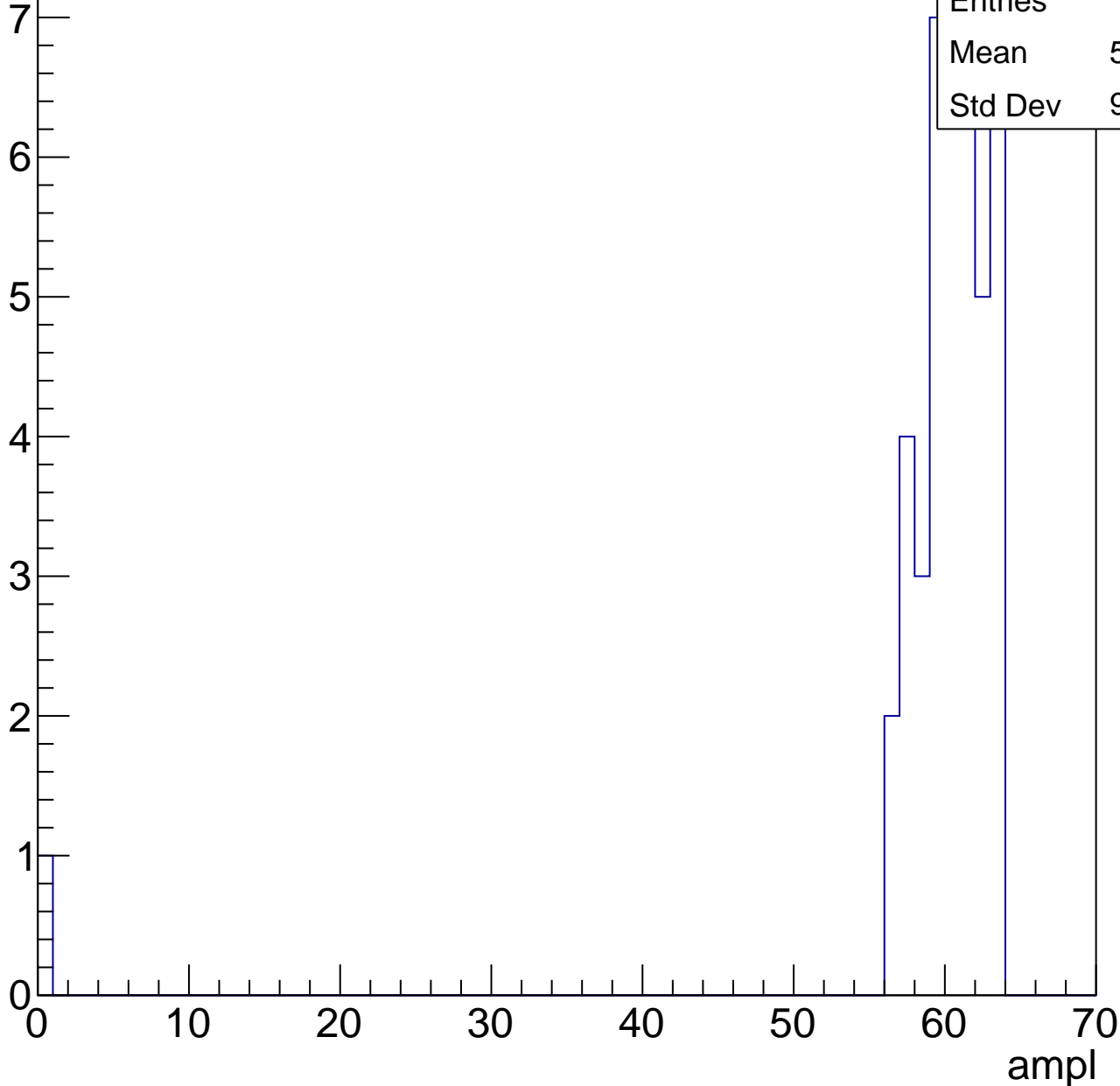


# B0L000S, U7-ch34, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

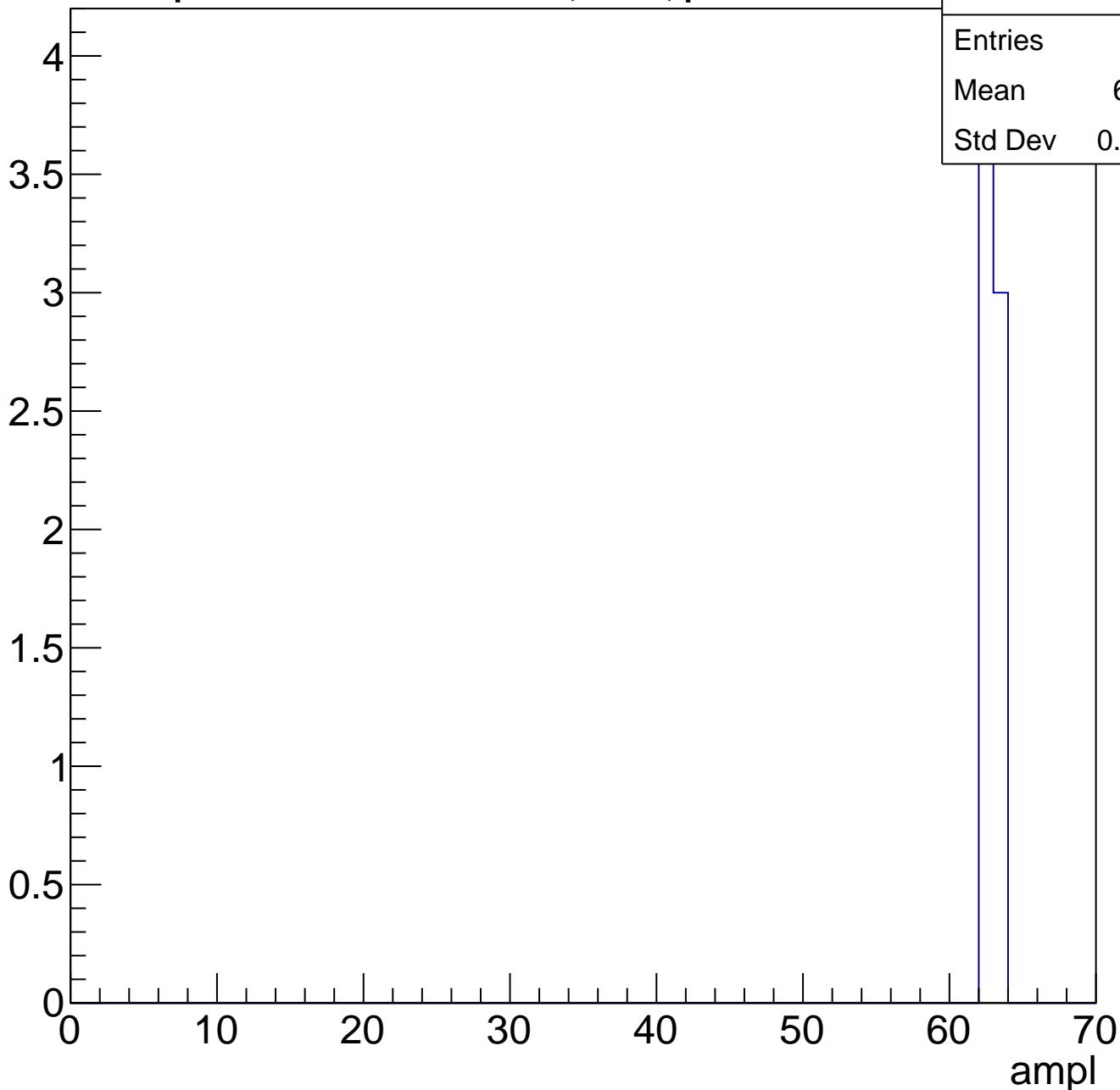
Entries	43
Mean	58.72
Std Dev	9.284



# B0L000S, U7-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	7
Mean	62.43
Std Dev	0.4949



# B0L000S, U7-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	2
Mean	11
Std Dev	11

# B0L000S, U7-ch35, adc0

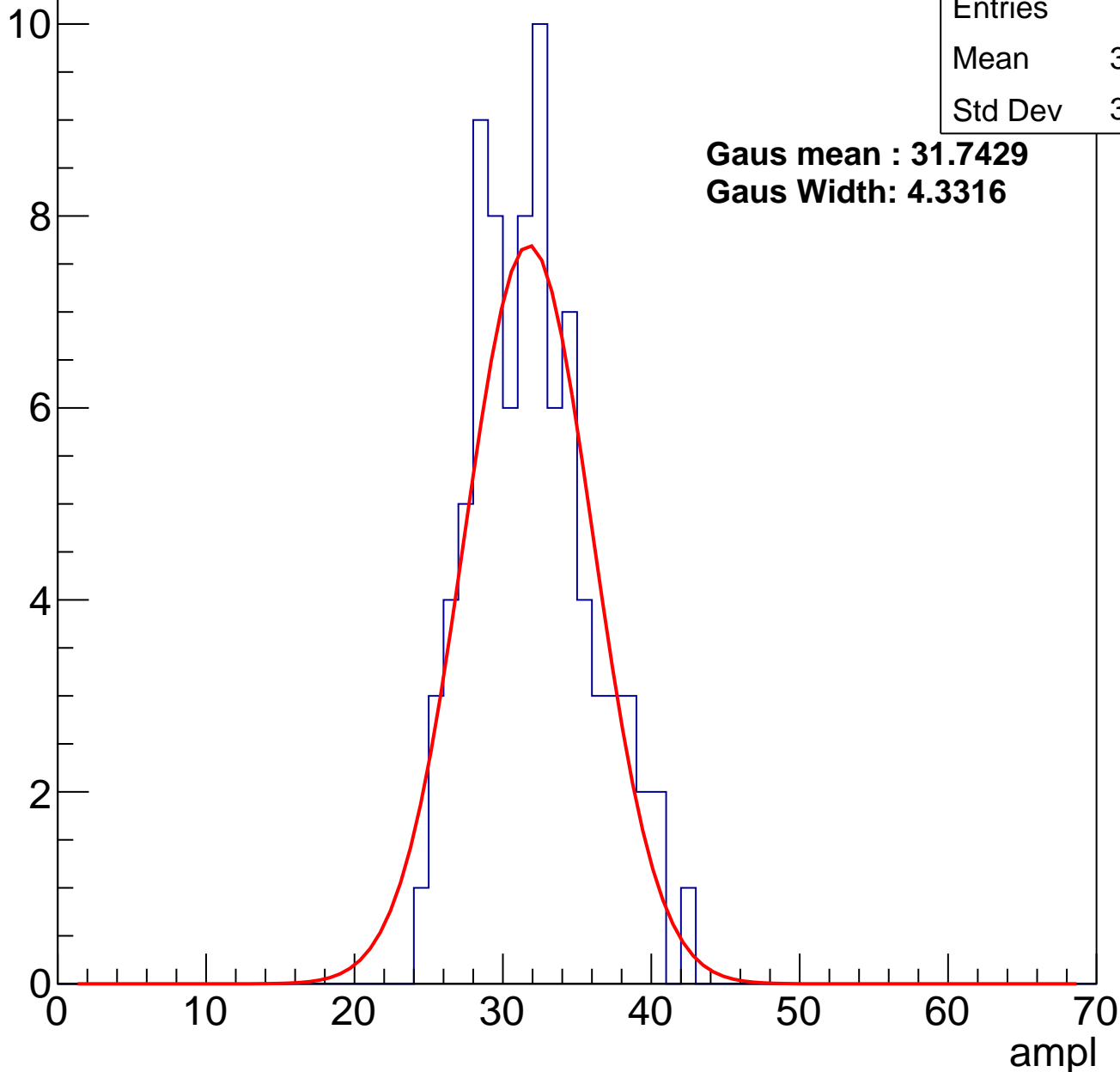
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	85
Mean	31.52
Std Dev	3.963

**Gaus mean : 31.7429**

**Gaus Width: 4.3316**

Entry



# B0L000S, U7-ch35, adc1

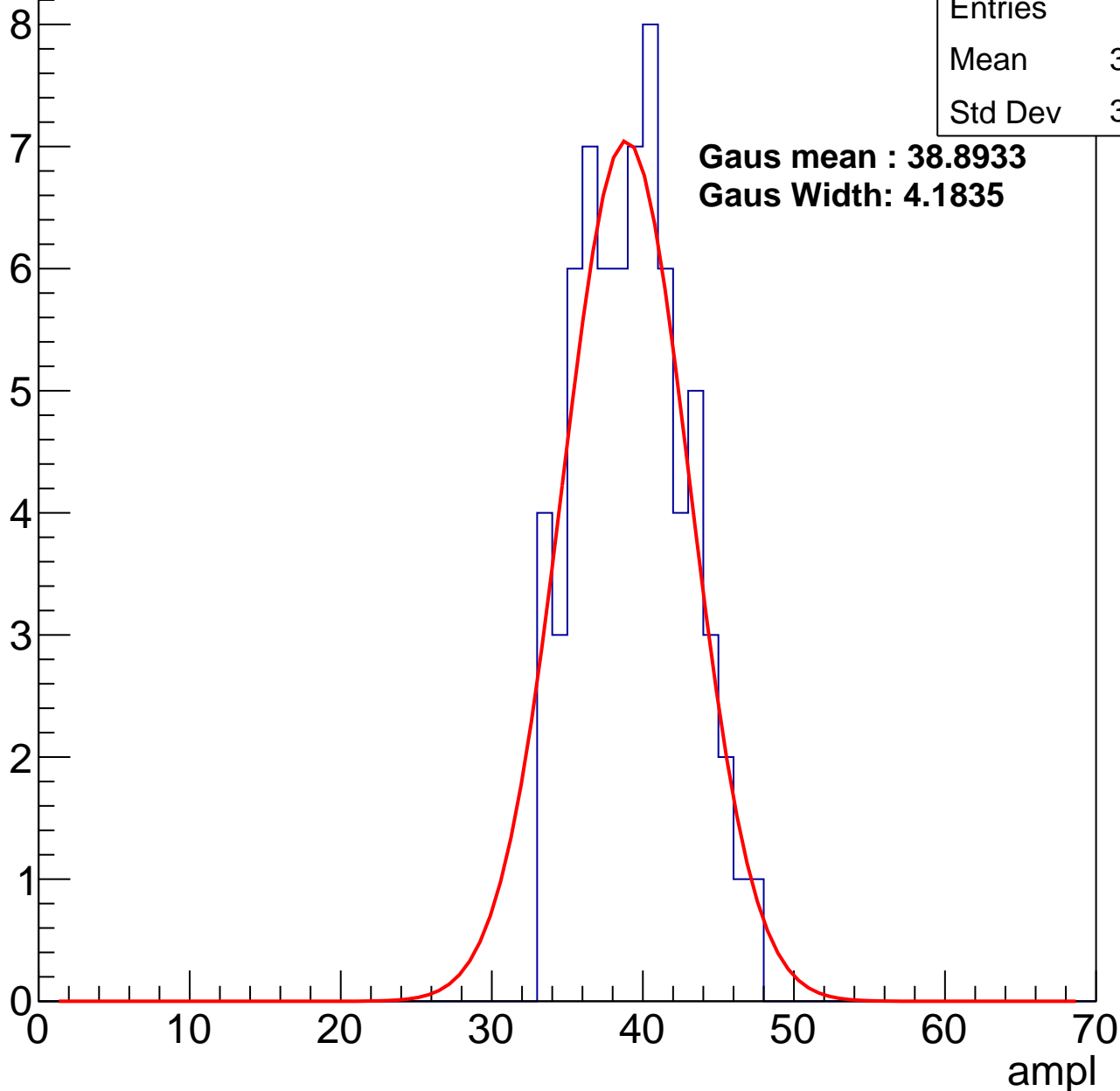
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	69
Mean	38.88
Std Dev	3.437

**Gaus mean : 38.8933**

**Gaus Width: 4.1835**



# B0L000S, U7-ch35, adc2

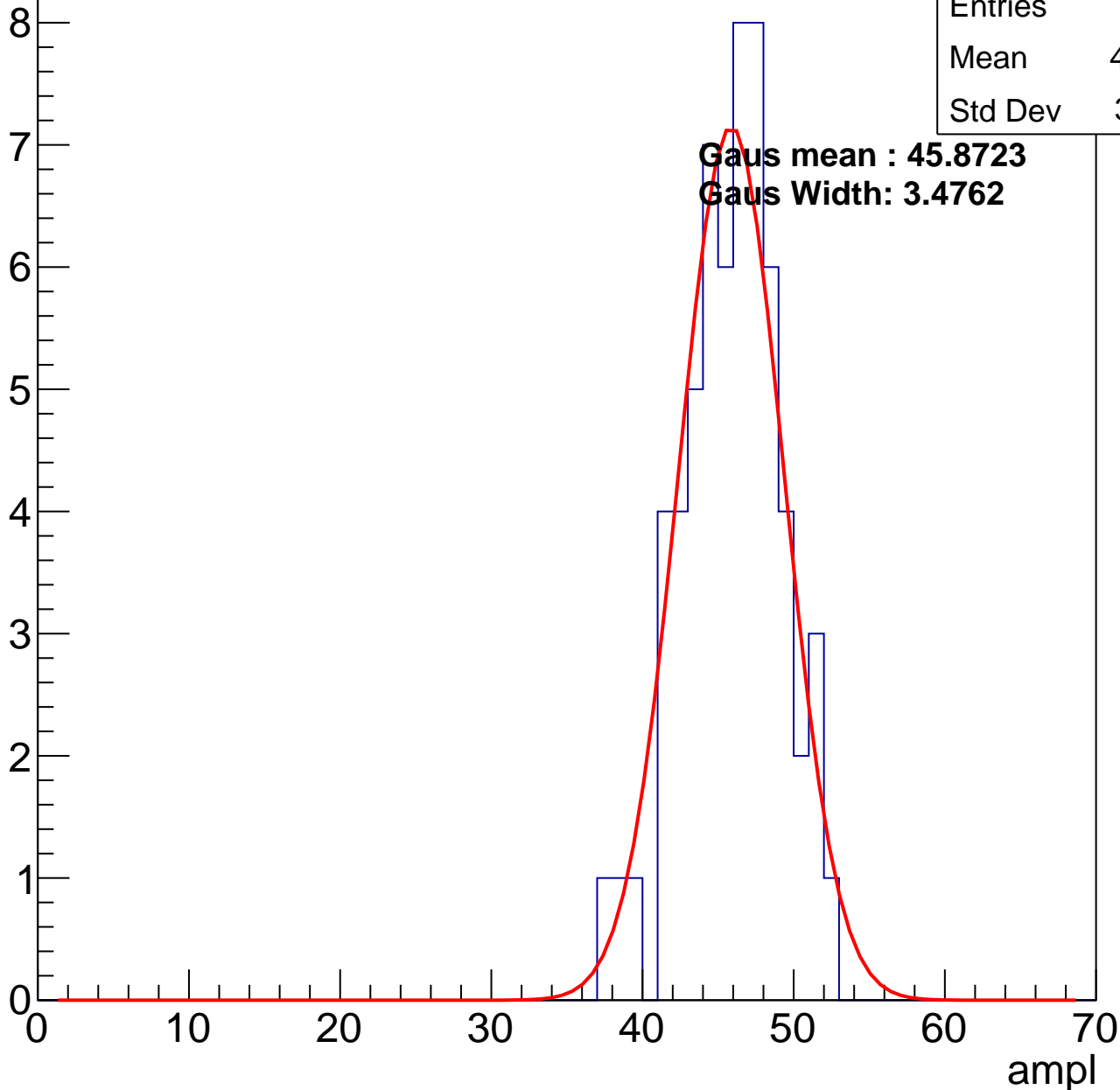
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	61
Mean	45.44
Std Dev	3.211

**Gaus mean : 45.8723**

**Gaus Width: 3.4762**

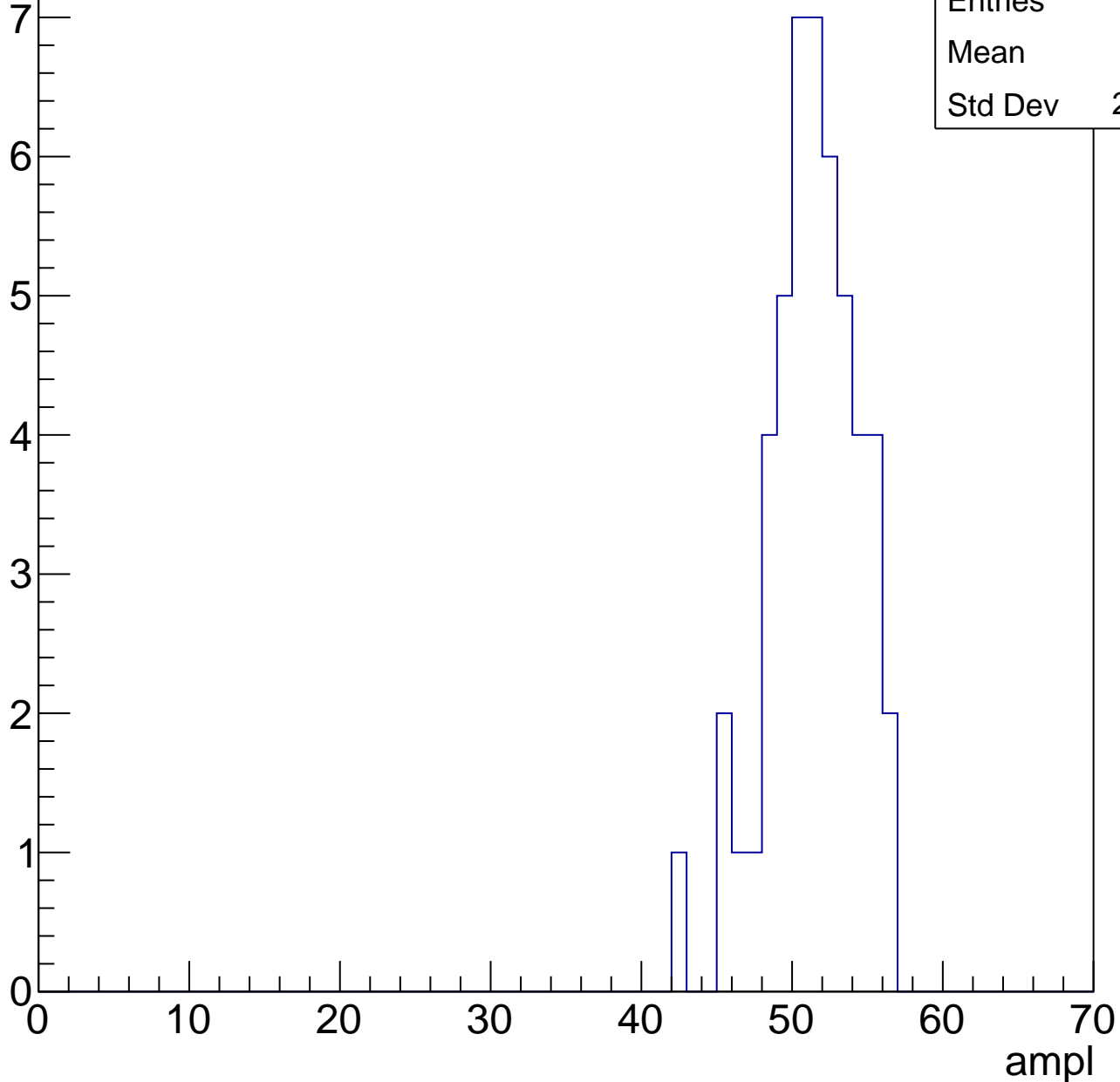


# B0L000S, U7-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	49
Mean	50.9
Std Dev	2.971



# B0L000S, U7-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

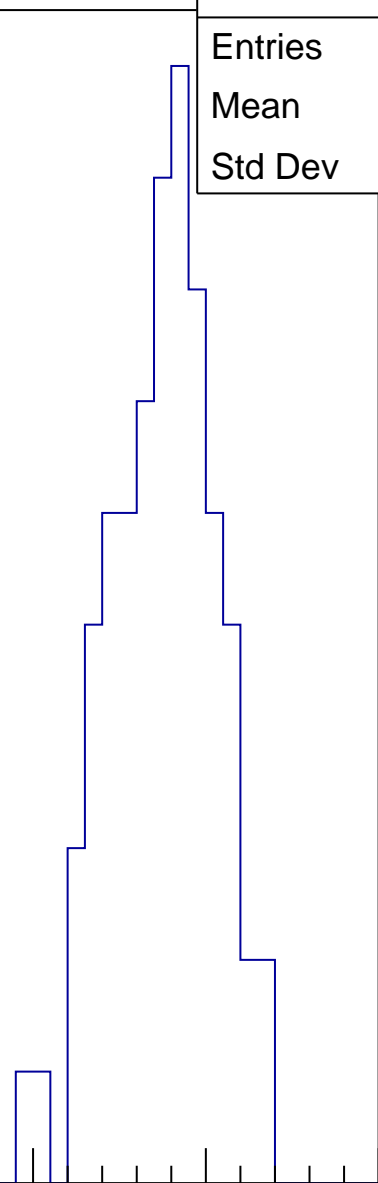
Entries	71
Mean	56.99
Std Dev	3.028

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

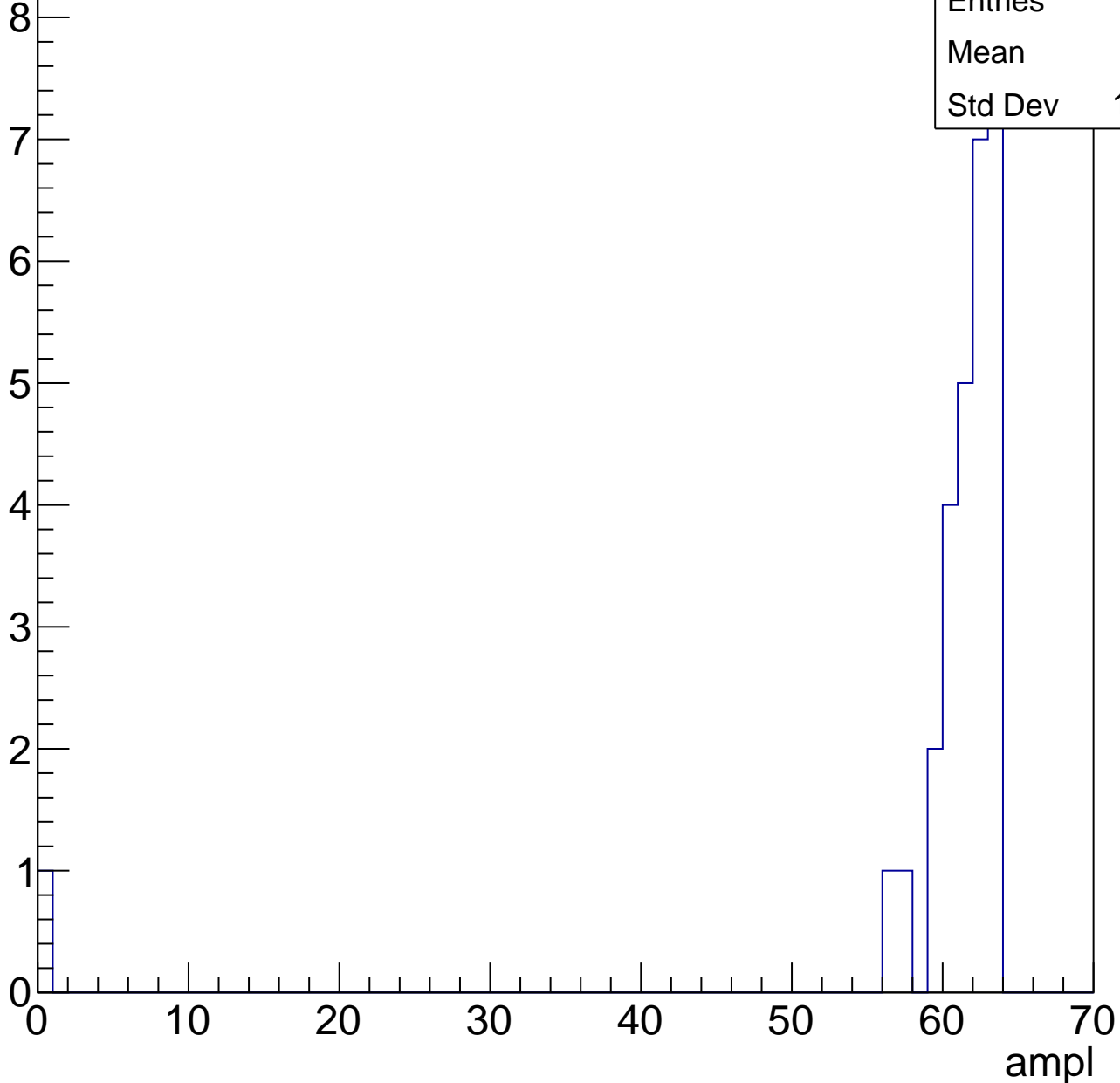


# B0L000S, U7-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	29
Mean	59.1
Std Dev	11.31



# B0L000S, U7-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch36, adc0

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	76
Mean	32.59
Std Dev	3.301

**Gaus mean : 33.1273**

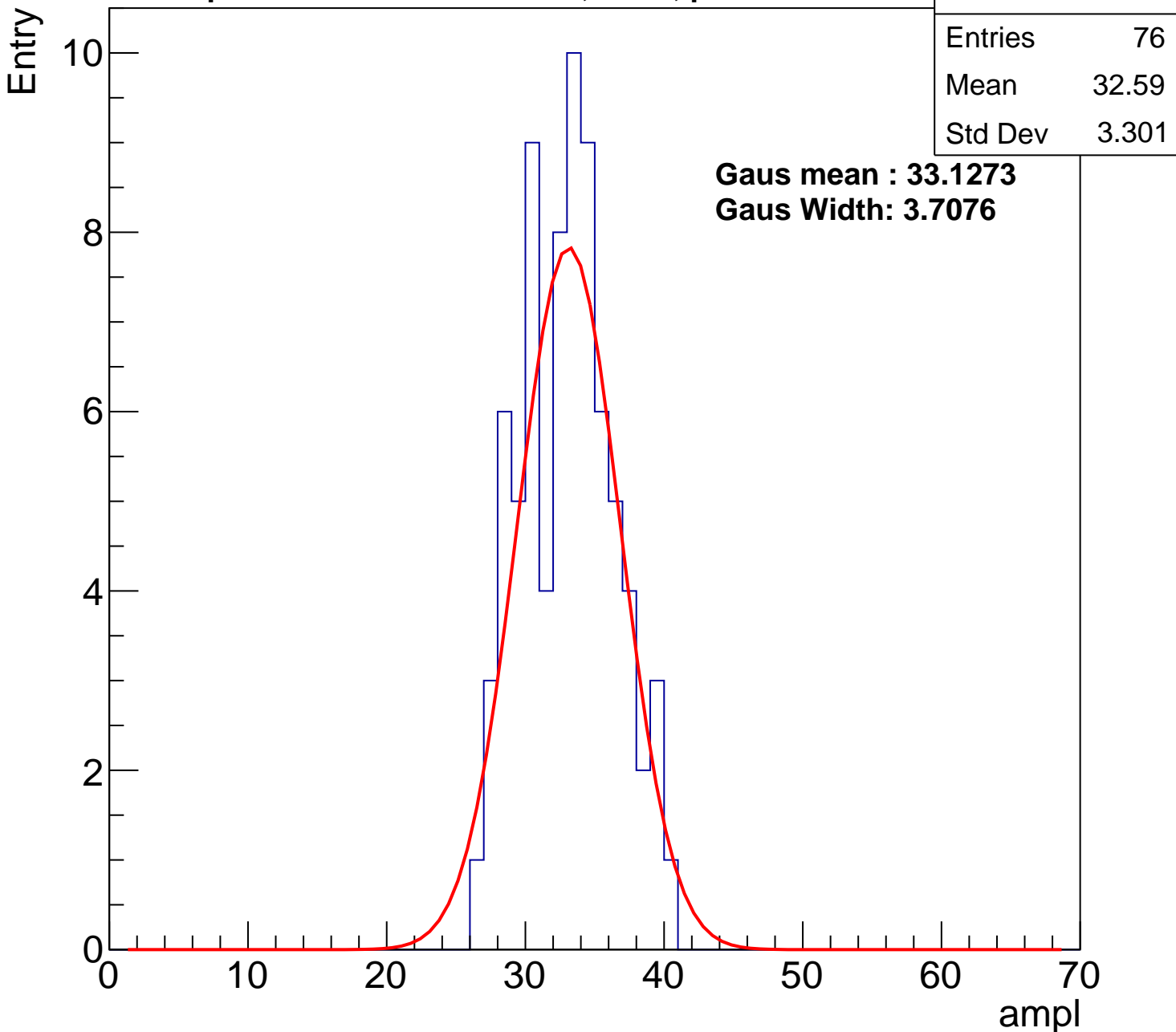
**Gaus Width: 3.7076**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L000S, U7-ch36, adc1

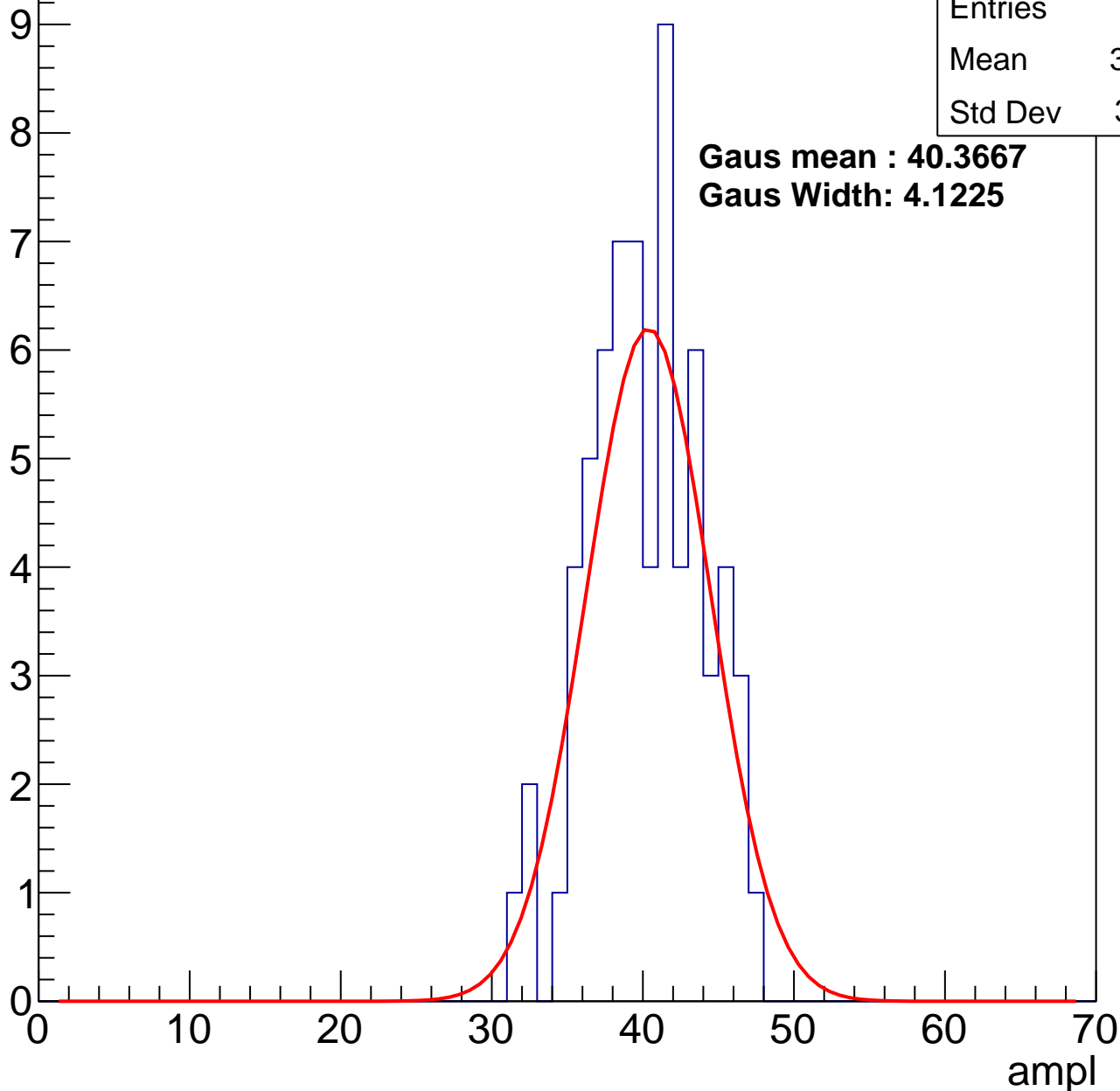
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	67
Mean	39.73
Std Dev	3.651

**Gaus mean : 40.3667**

**Gaus Width: 4.1225**



# B0L000S, U7-ch36, adc2

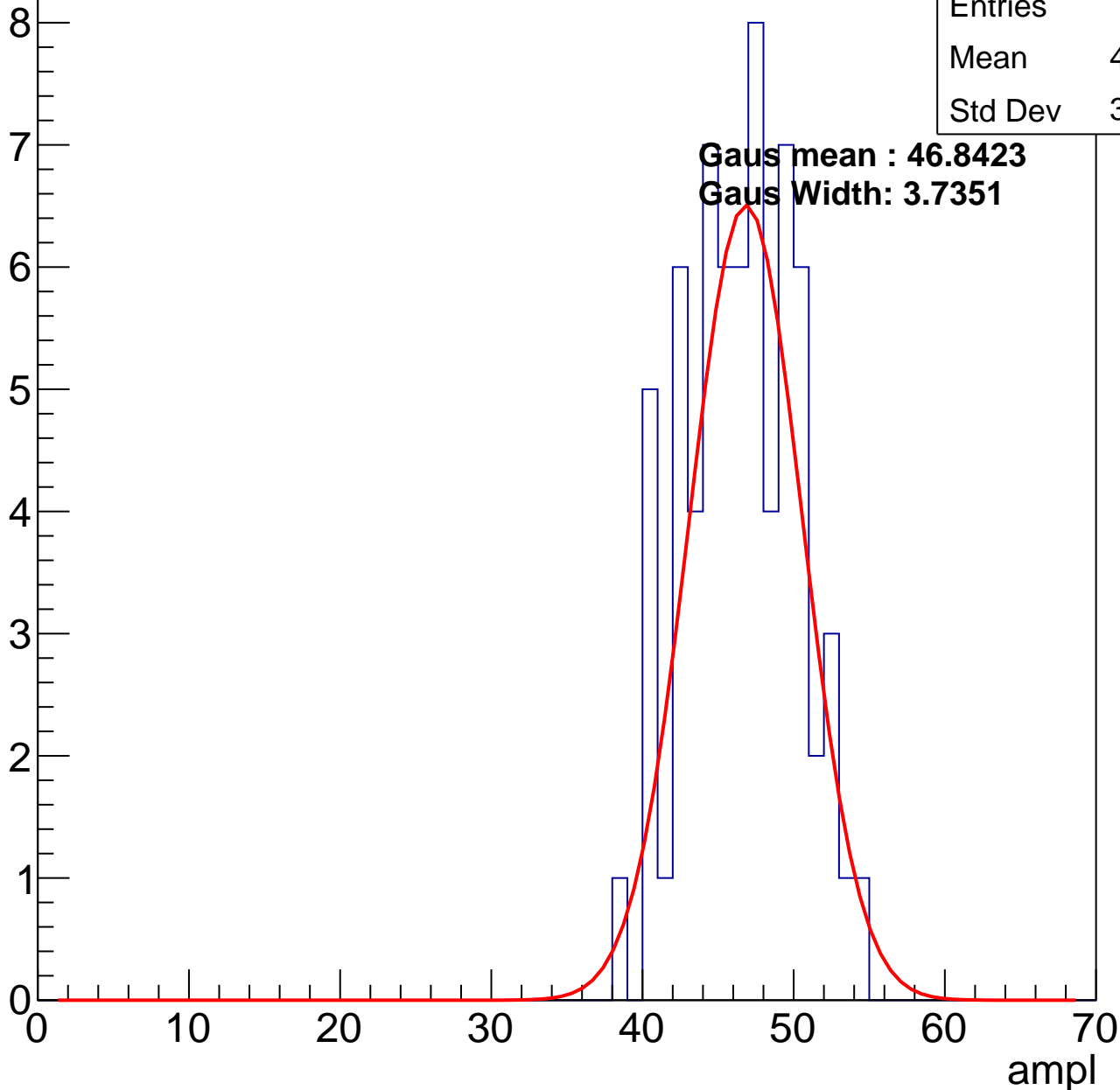
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	68
Mean	46.07
Std Dev	3.615

Gaus mean : 46.8423

Gaus Width: 3.7351

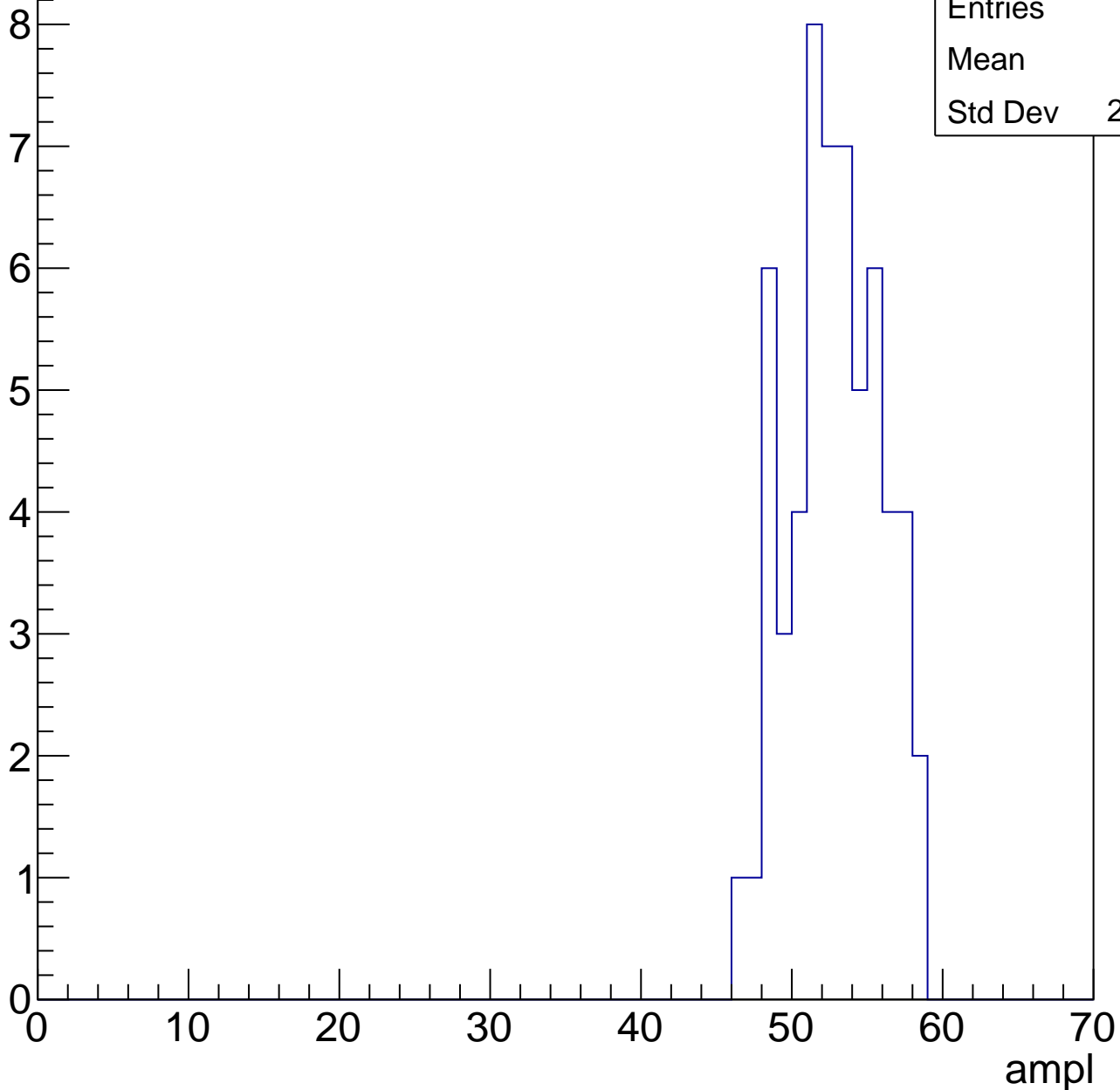


# B0L000S, U7-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

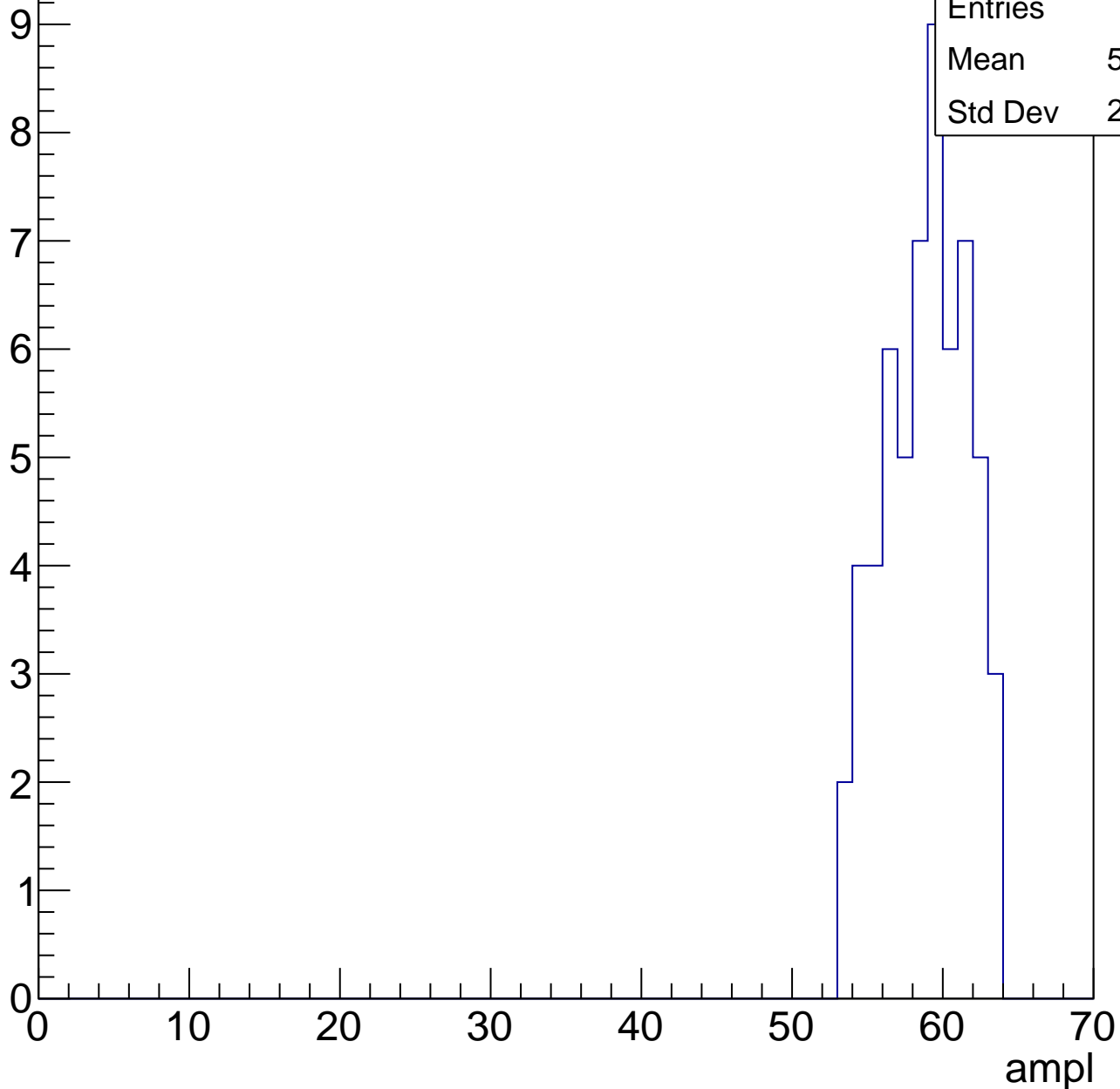
Entries	58
Mean	52.4
Std Dev	2.982



# B0L000S, U7-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

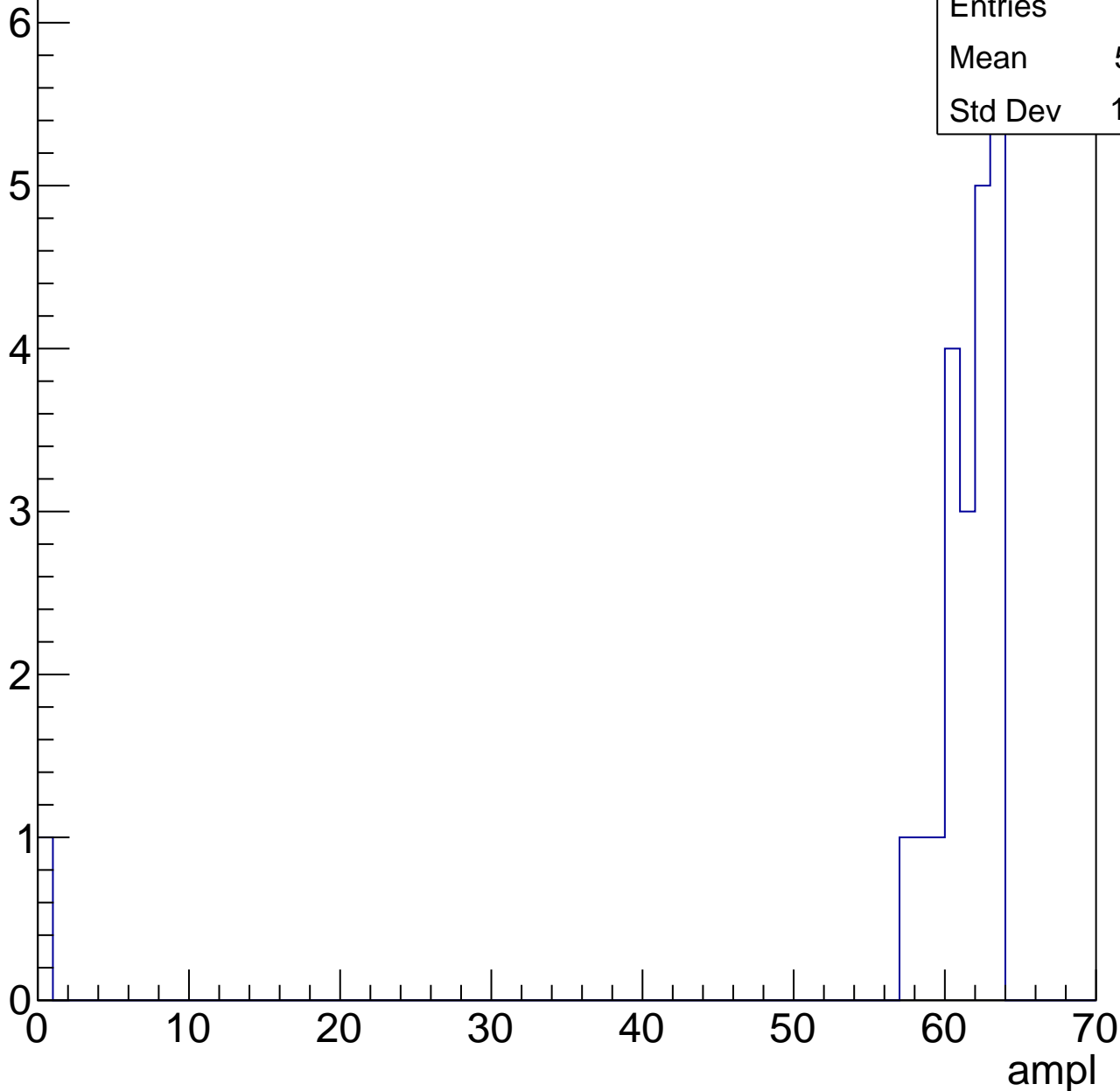


# B0L000S, U7-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	22
Mean	58.41
Std Dev	12.85



# B0L000S, U7-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

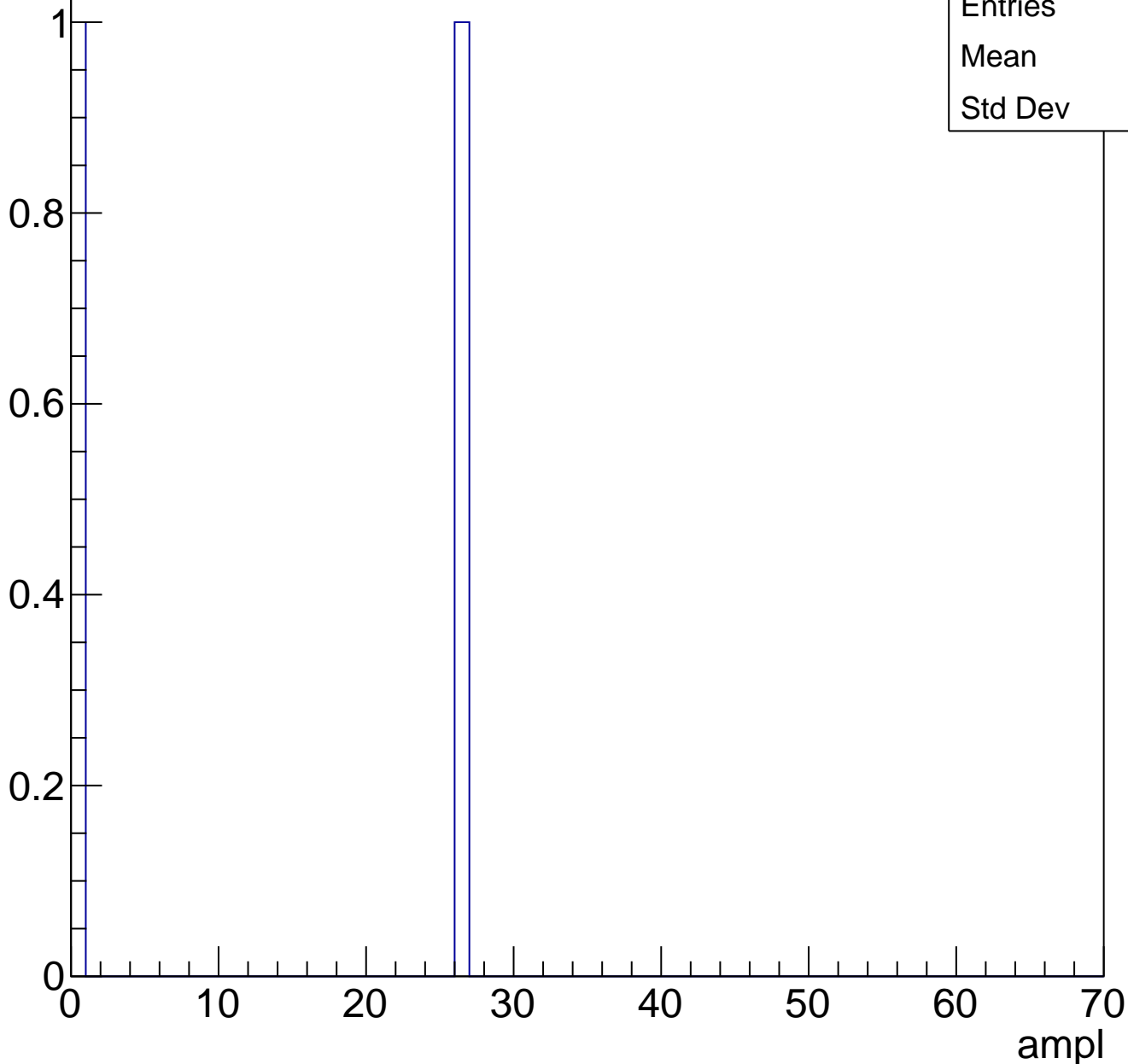




# B0L000S, U7-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	2
Mean	13
Std Dev	13

# B0L000S, U7-ch37, adc0

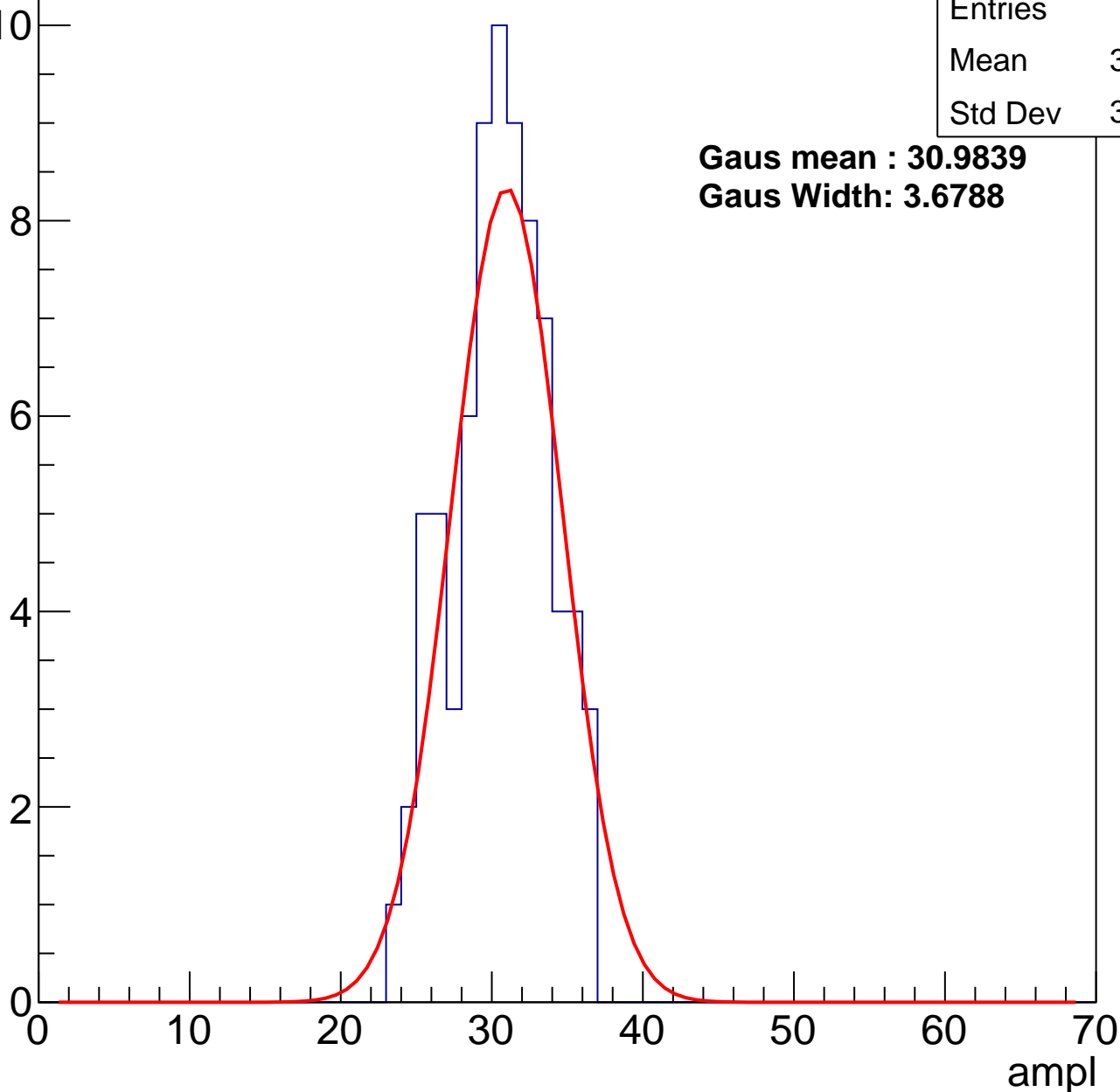
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	76
Mean	30.08
Std Dev	3.165

**Gaus mean : 30.9839**

**Gaus Width: 3.6788**



# B0L000S, U7-ch37, adc1

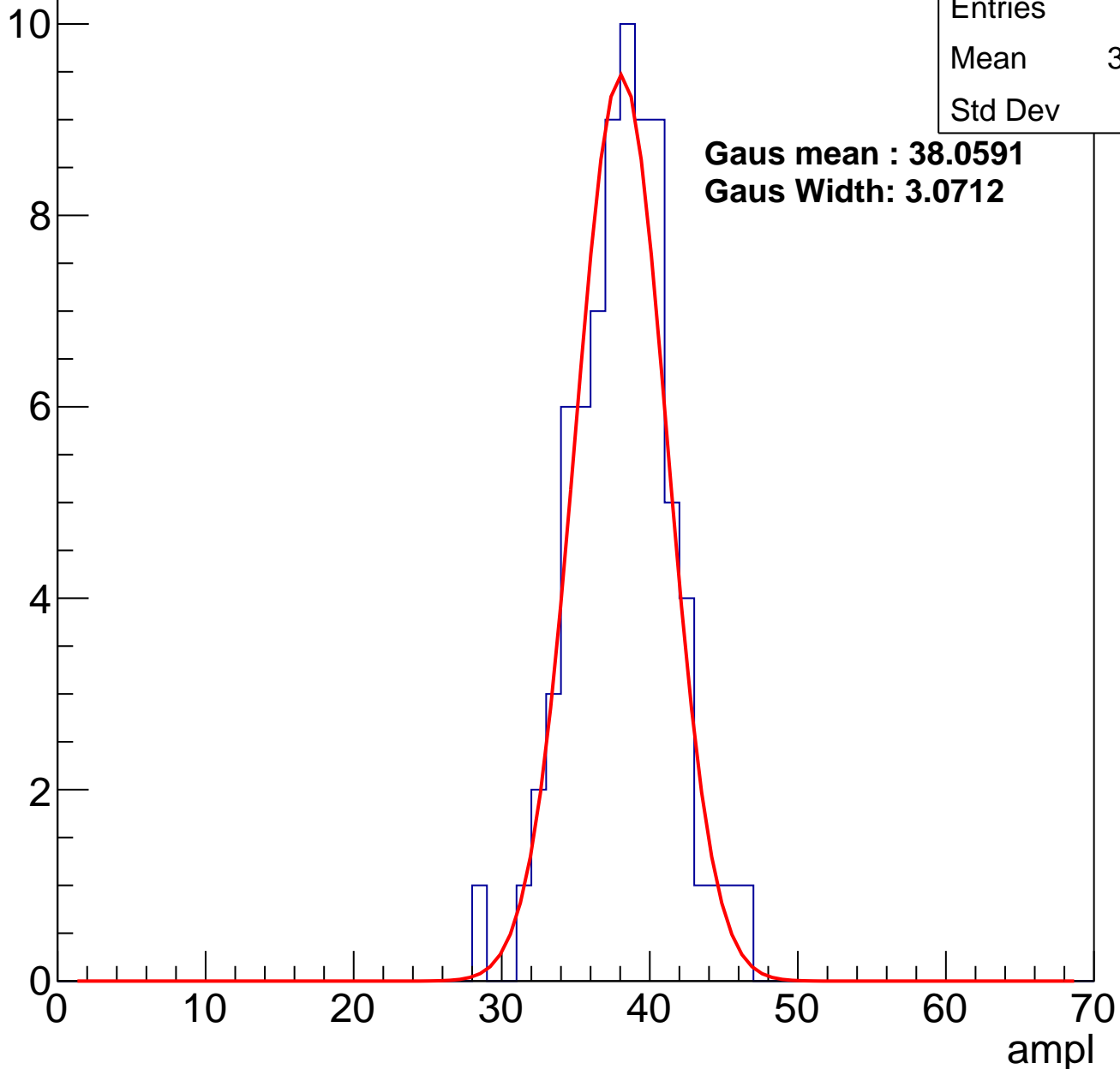
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	76
Mean	37.67
Std Dev	3.25

**Gaus mean : 38.0591**

**Gaus Width: 3.0712**

Entry



# B0L000S, U7-ch37, adc2

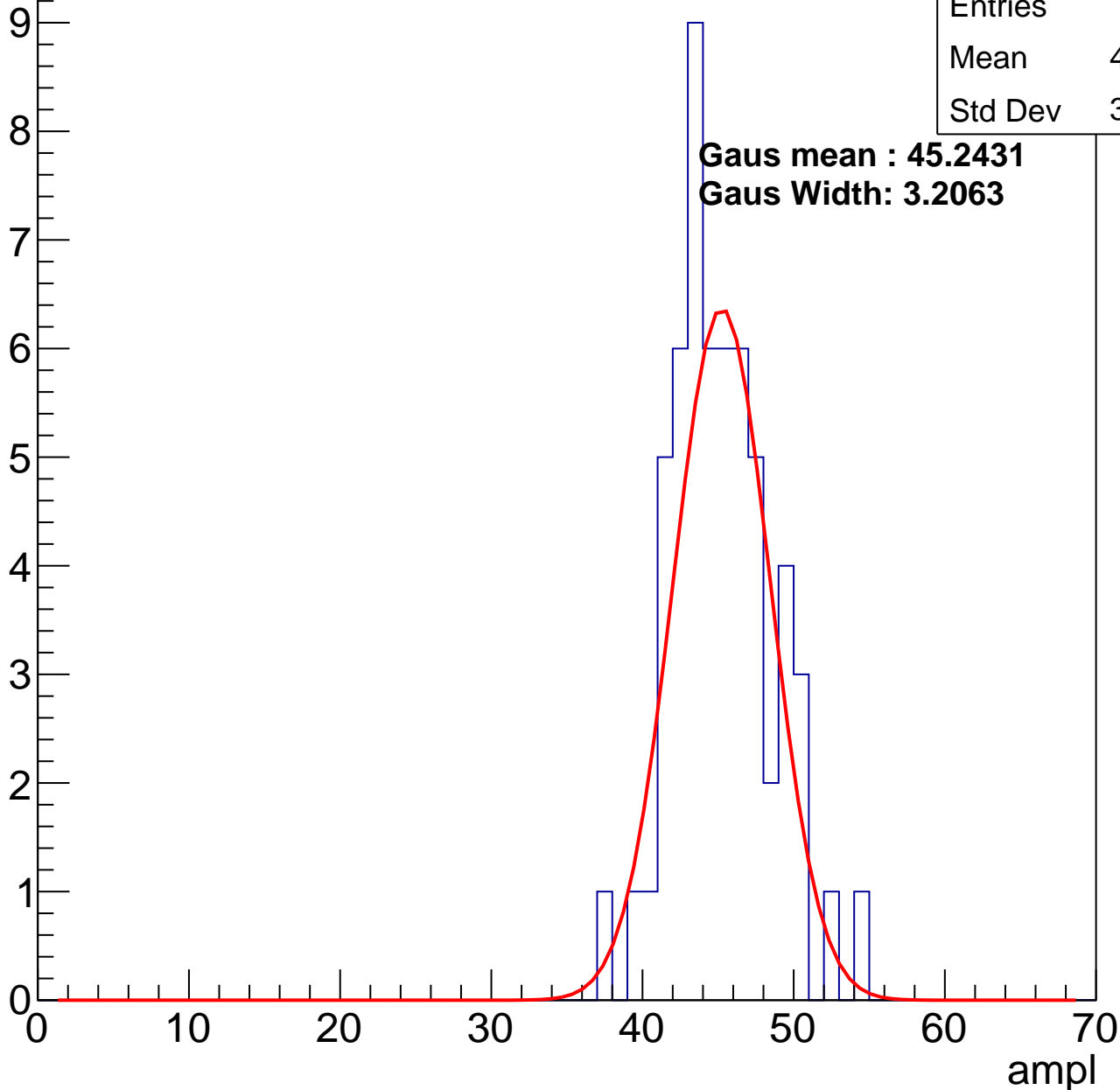
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	57
Mean	44.79
Std Dev	3.275

**Gaus mean : 45.2431**

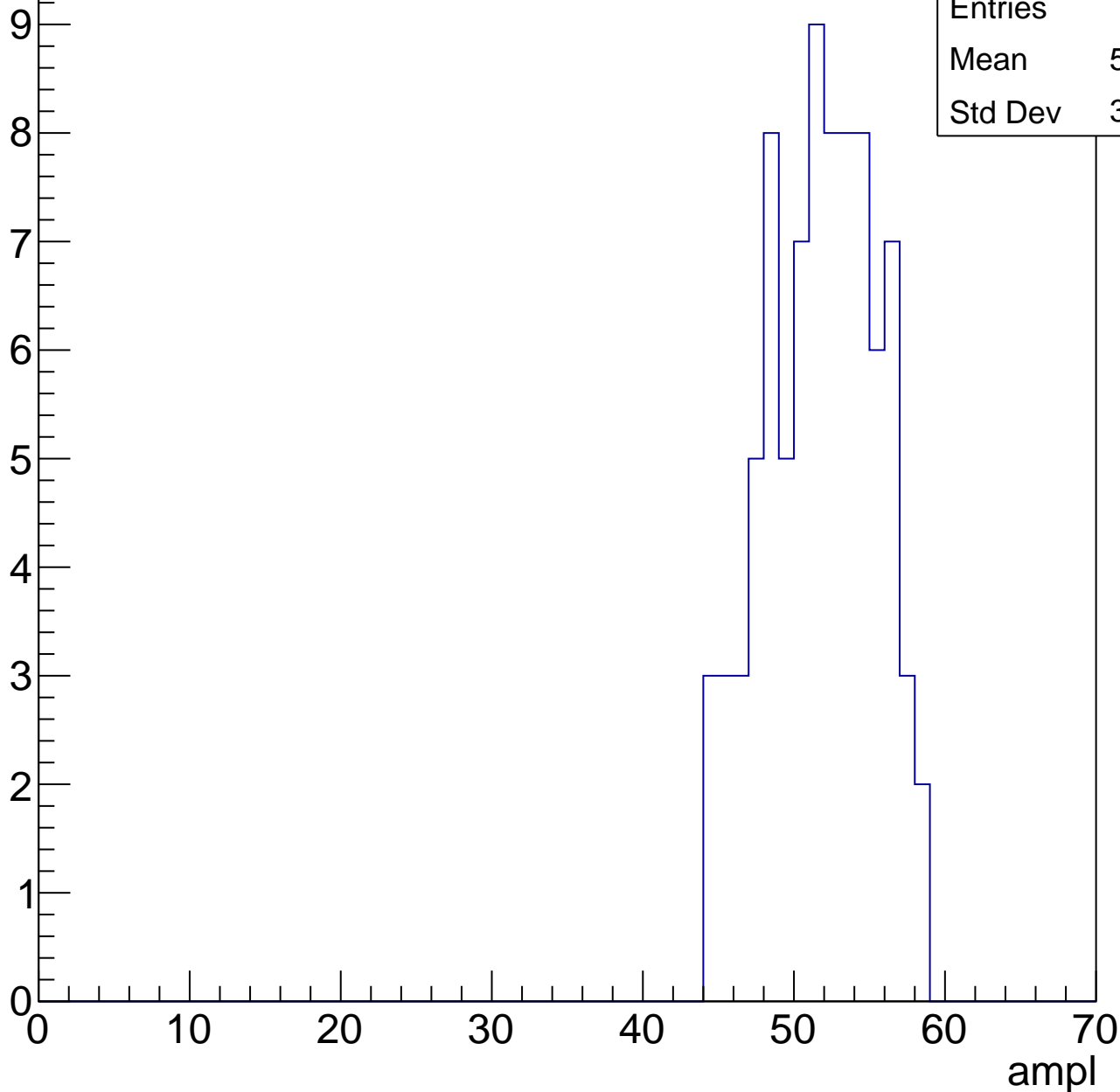
**Gaus Width: 3.2063**



# B0L000S, U7-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



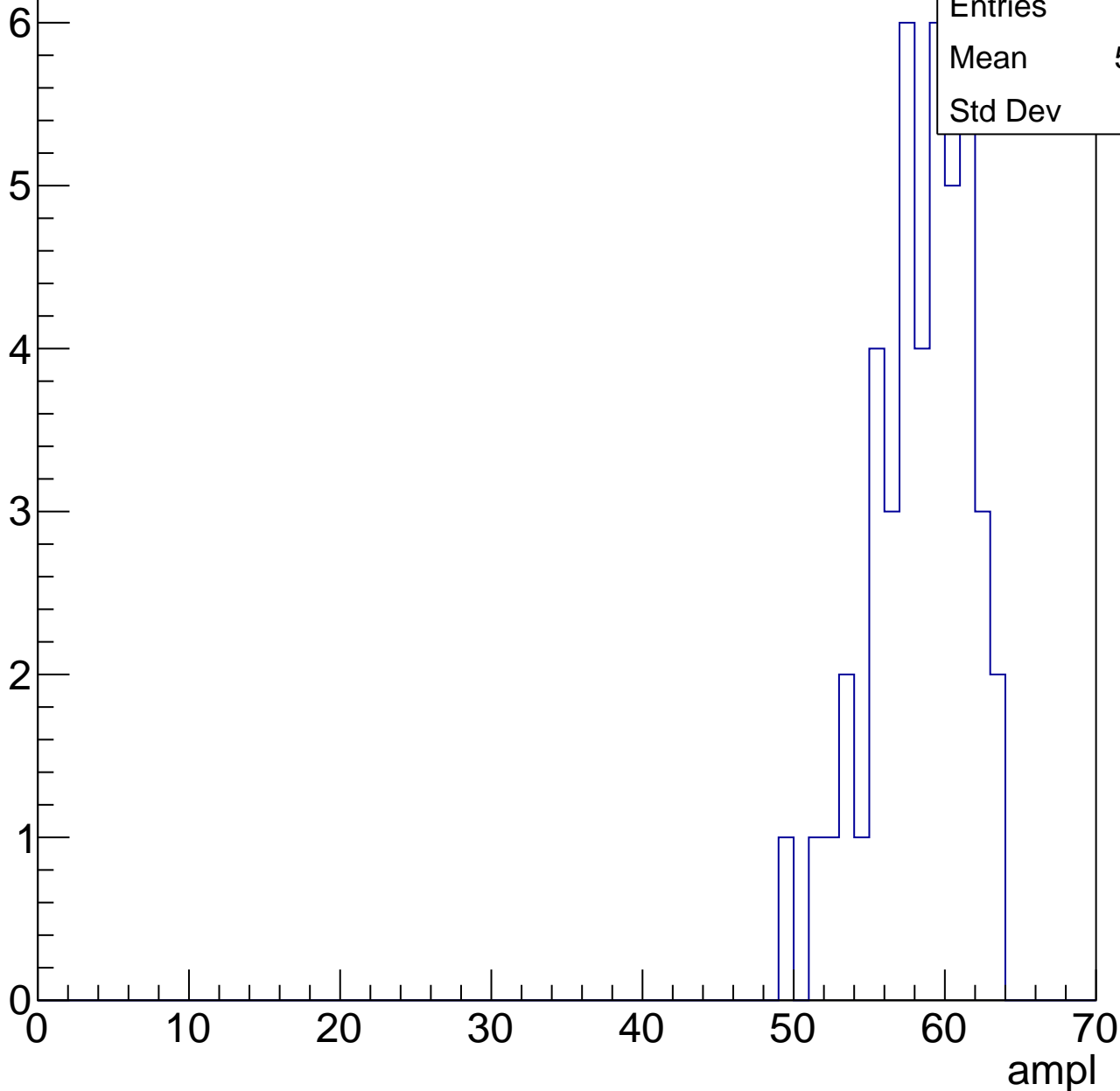
Entries	85
Mean	51.28
Std Dev	3.583

# B0L000S, U7-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	45
Mean	57.91
Std Dev	3.21

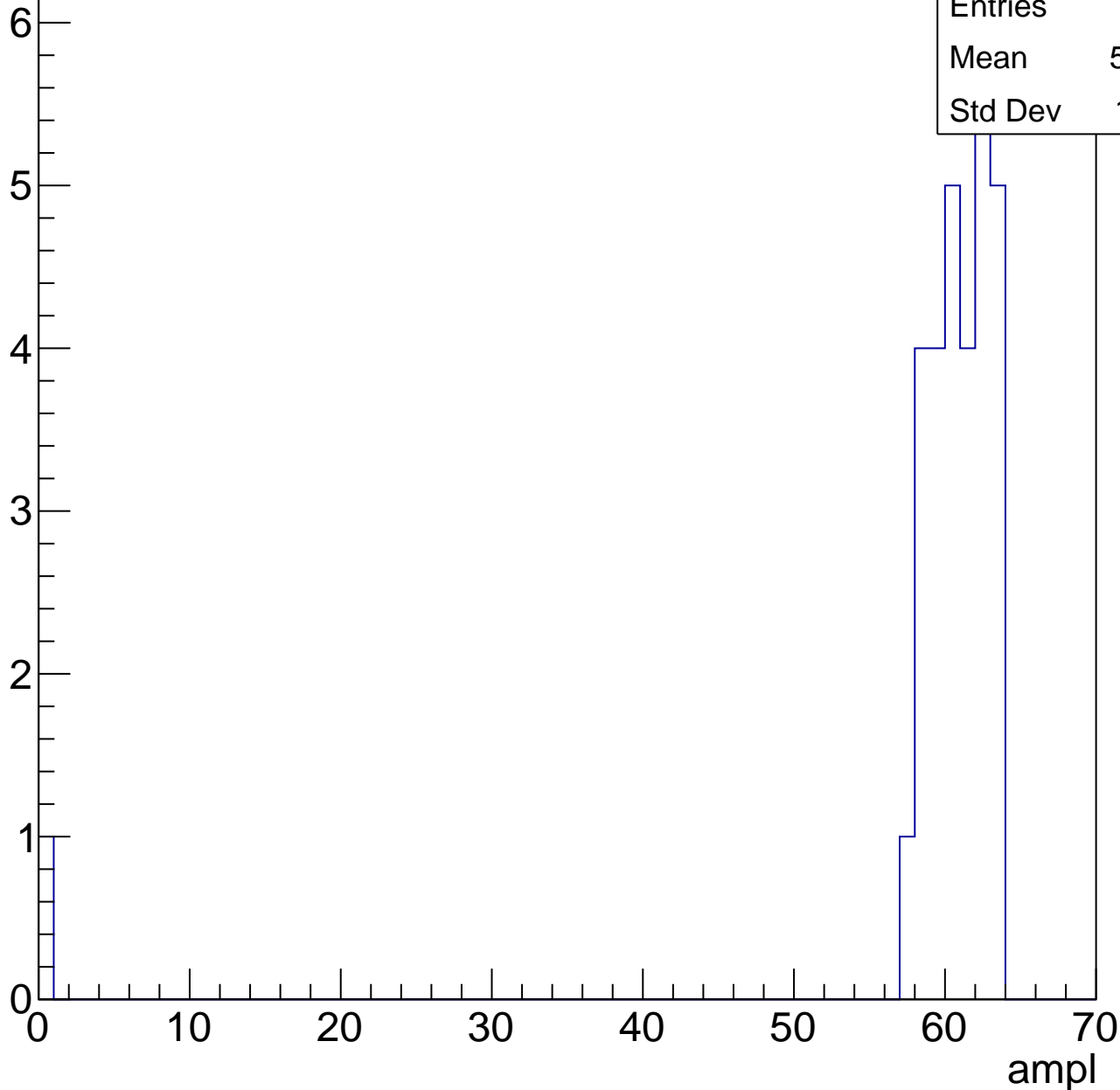


# B0L000S, U7-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

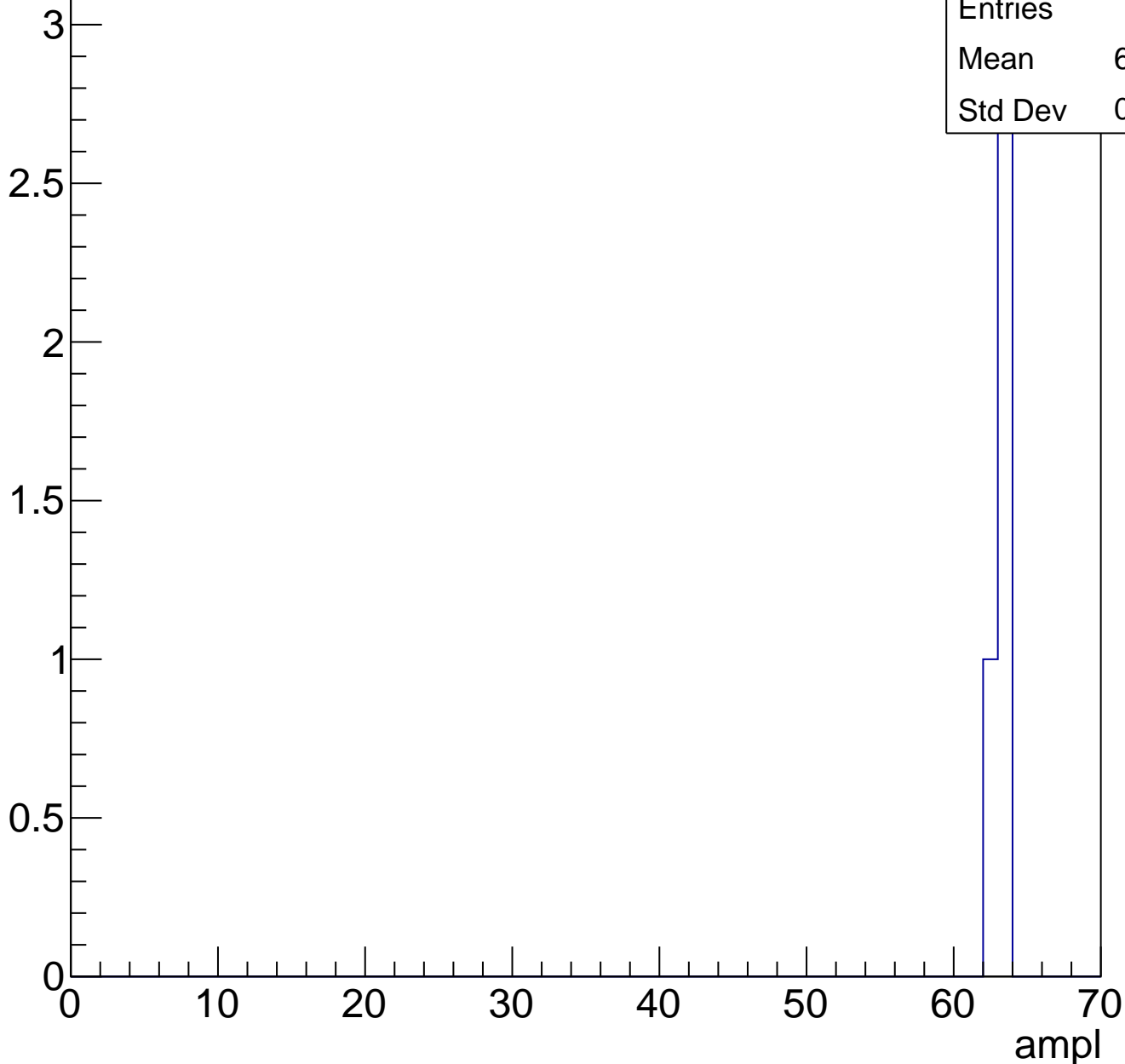
Entries	30
Mean	58.53
Std Dev	11.01



# B0L000S, U7-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	2
Mean	11.5
Std Dev	11.5

# B0L000S, U7-ch38, adc0

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	84
Mean	29.77
Std Dev	3.51

**Gaus mean : 30.2645**

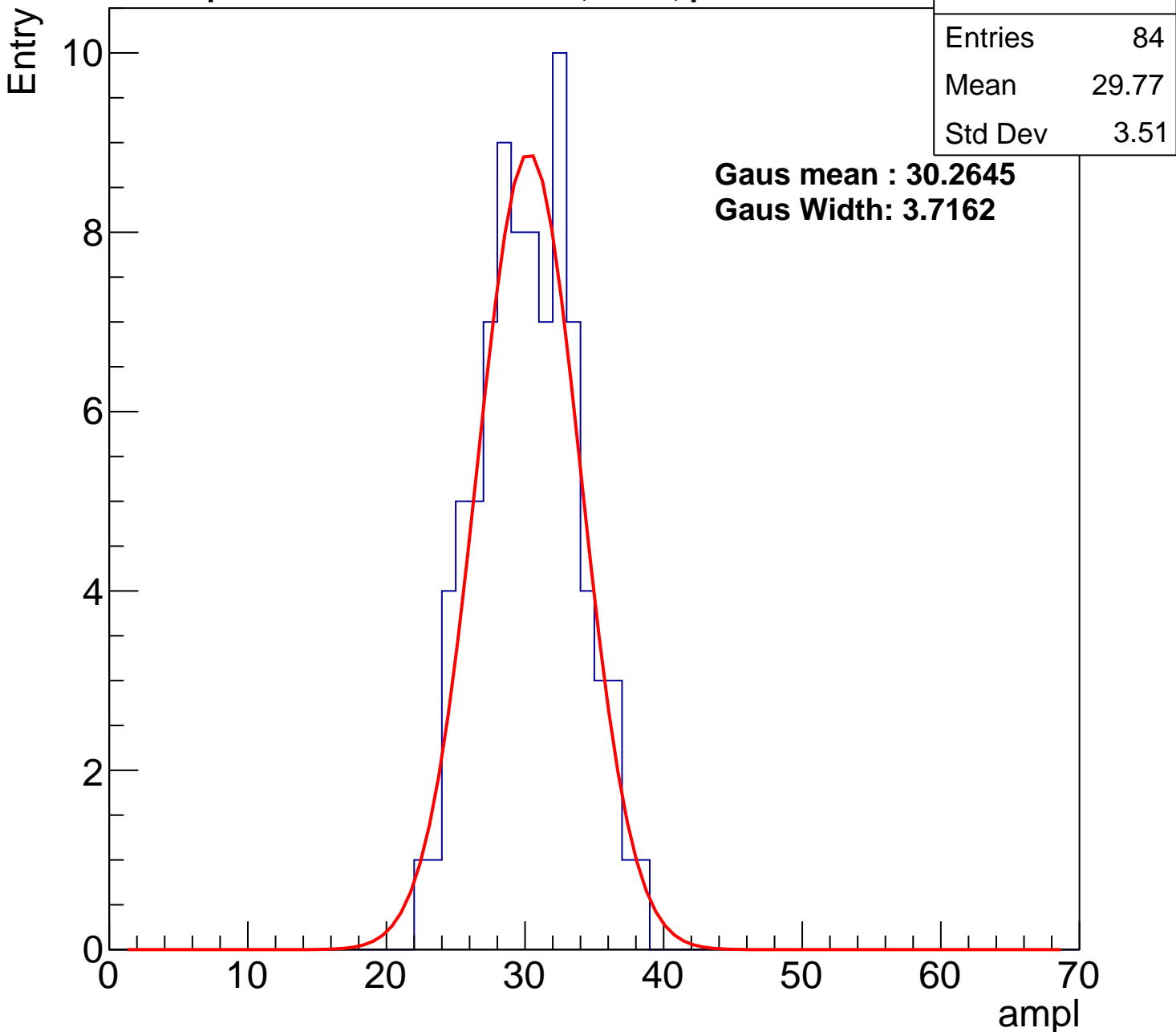
**Gaus Width: 3.7162**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L000S, U7-ch38, adc1

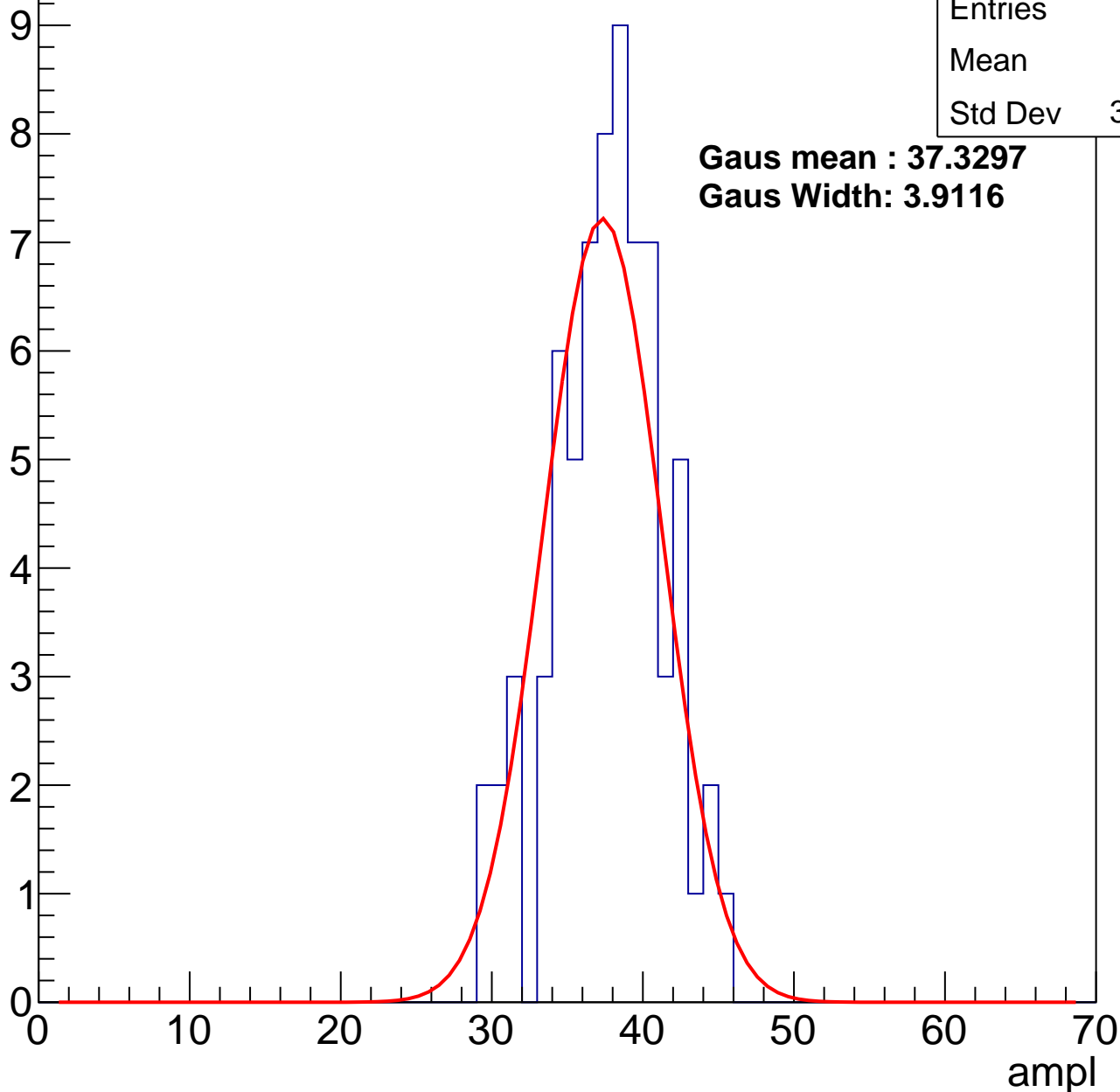
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	71
Mean	37.2
Std Dev	3.622

**Gaus mean : 37.3297**

**Gaus Width: 3.9116**



# B0L000S, U7-ch38, adc2

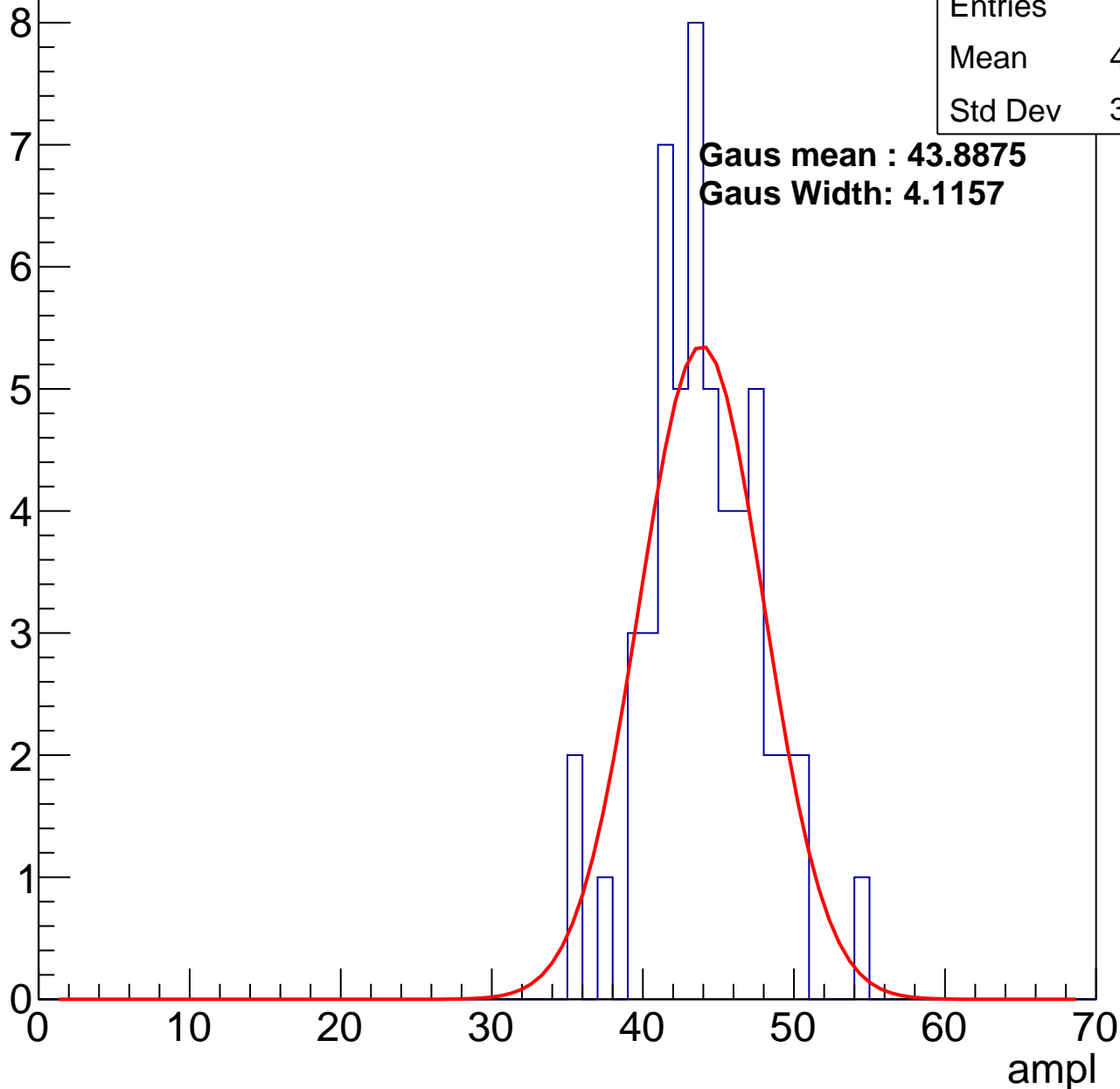
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	54
Mean	43.56
Std Dev	3.685

**Gaus mean : 43.8875**

**Gaus Width: 4.1157**

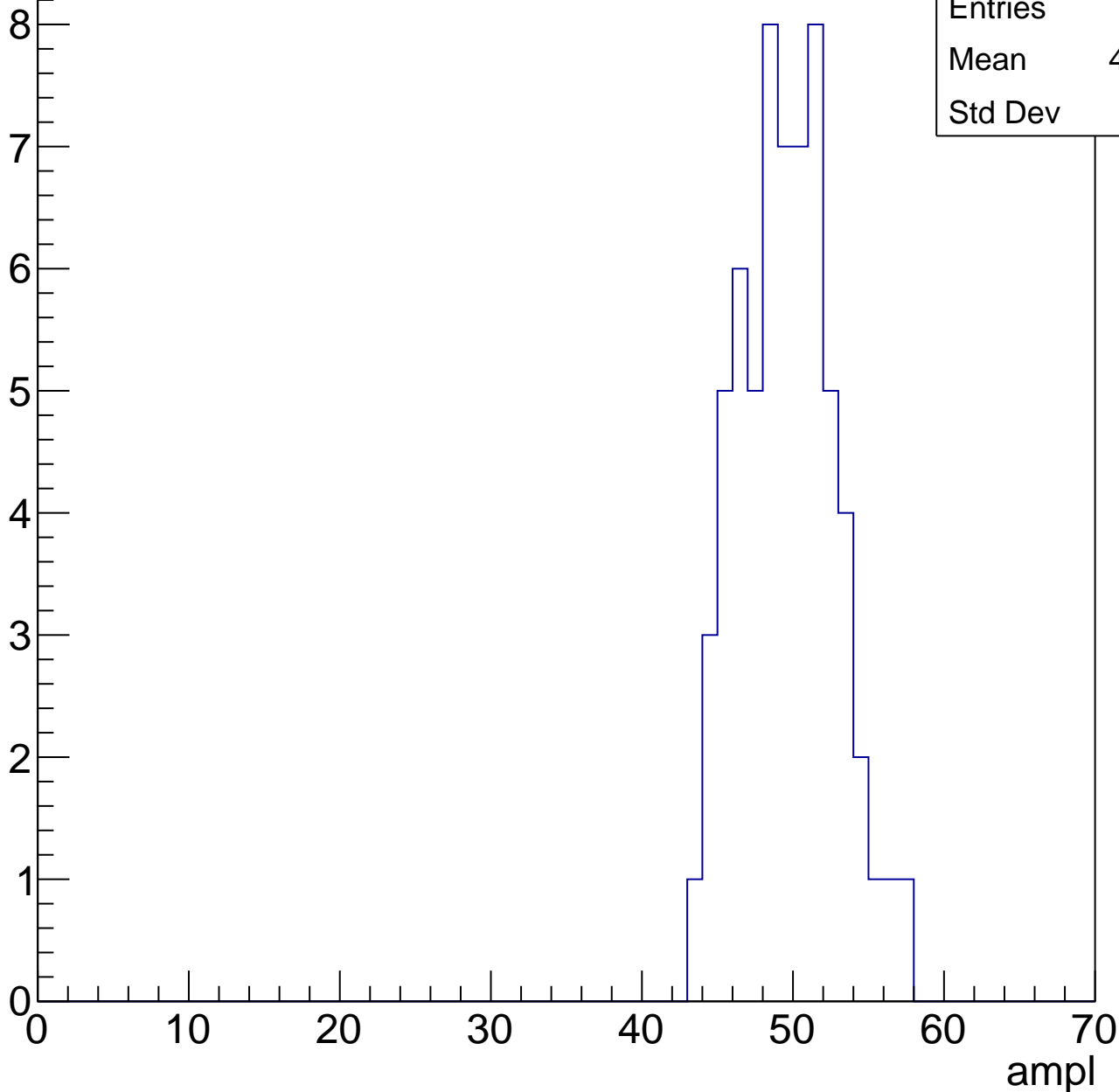


# B0L000S, U7-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	64
Mean	49.12
Std Dev	3.11

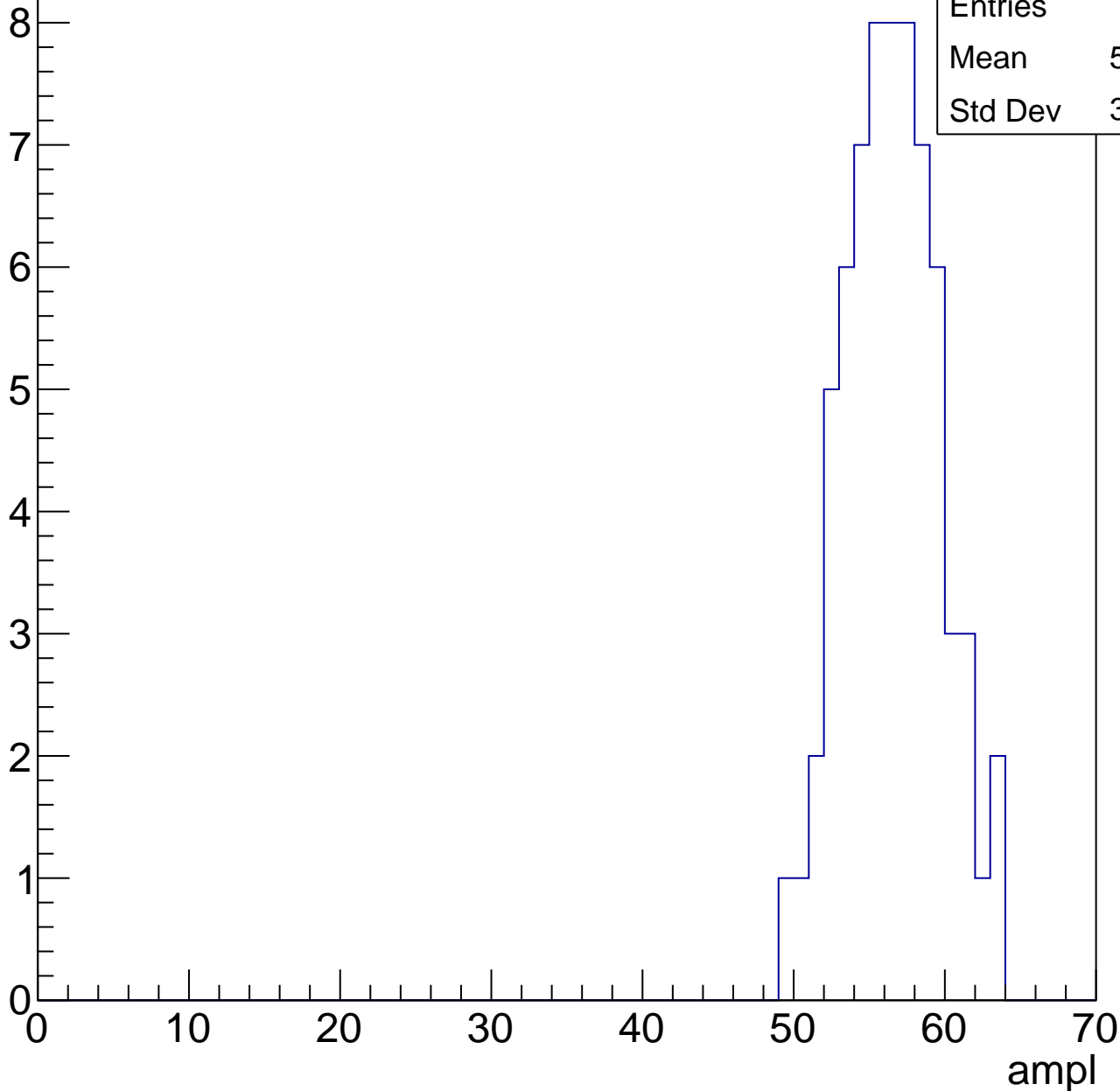


# B0L000S, U7-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	68
Mean	56.06
Std Dev	3.096



# B0L000S, U7-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

7

6

5

4

3

2

1

0

Entries	35
Mean	58.66
Std Dev	10.24

0

10

20

30

40

50

60

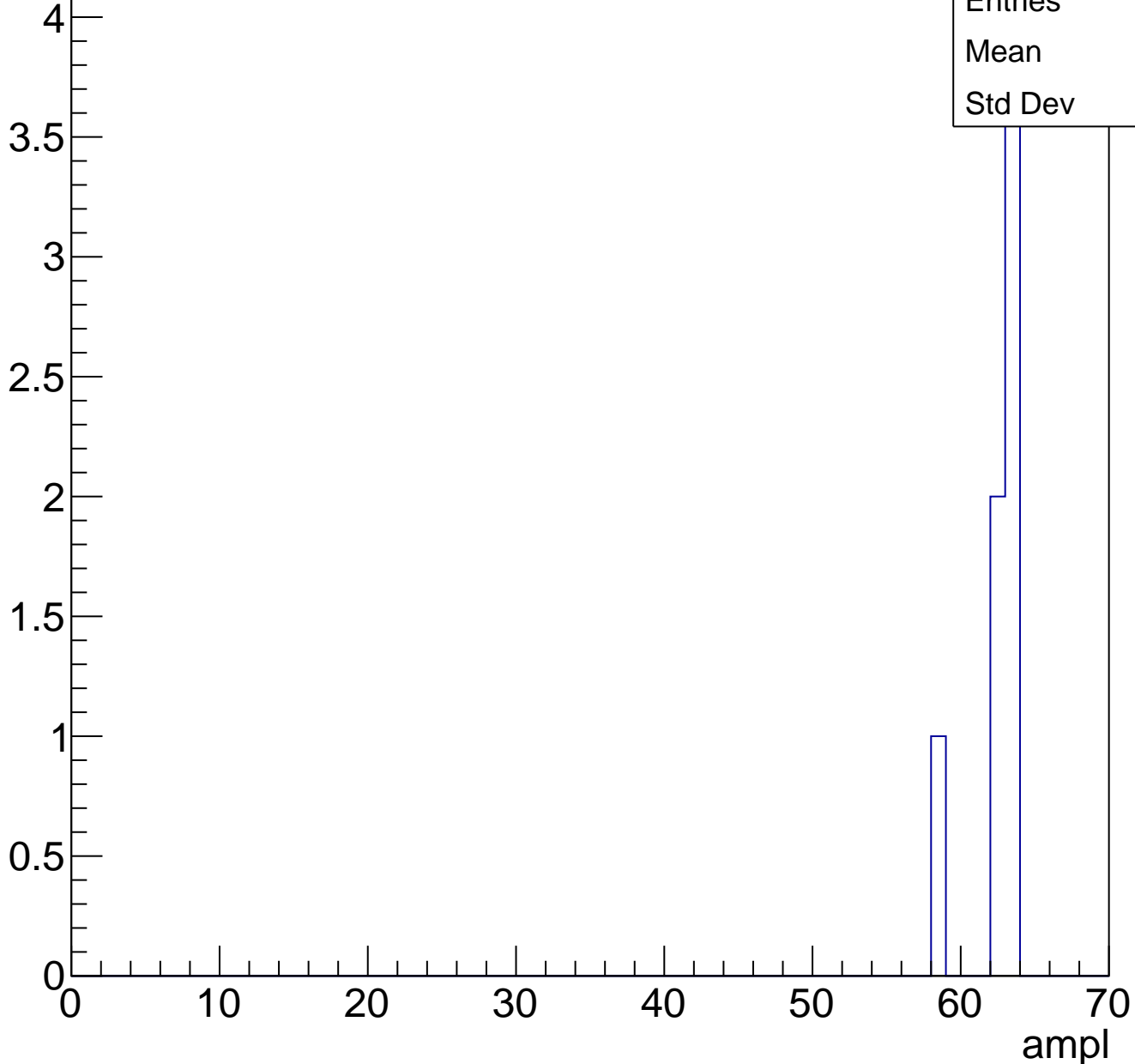
70

ampl

# B0L000S, U7-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch39, adc0

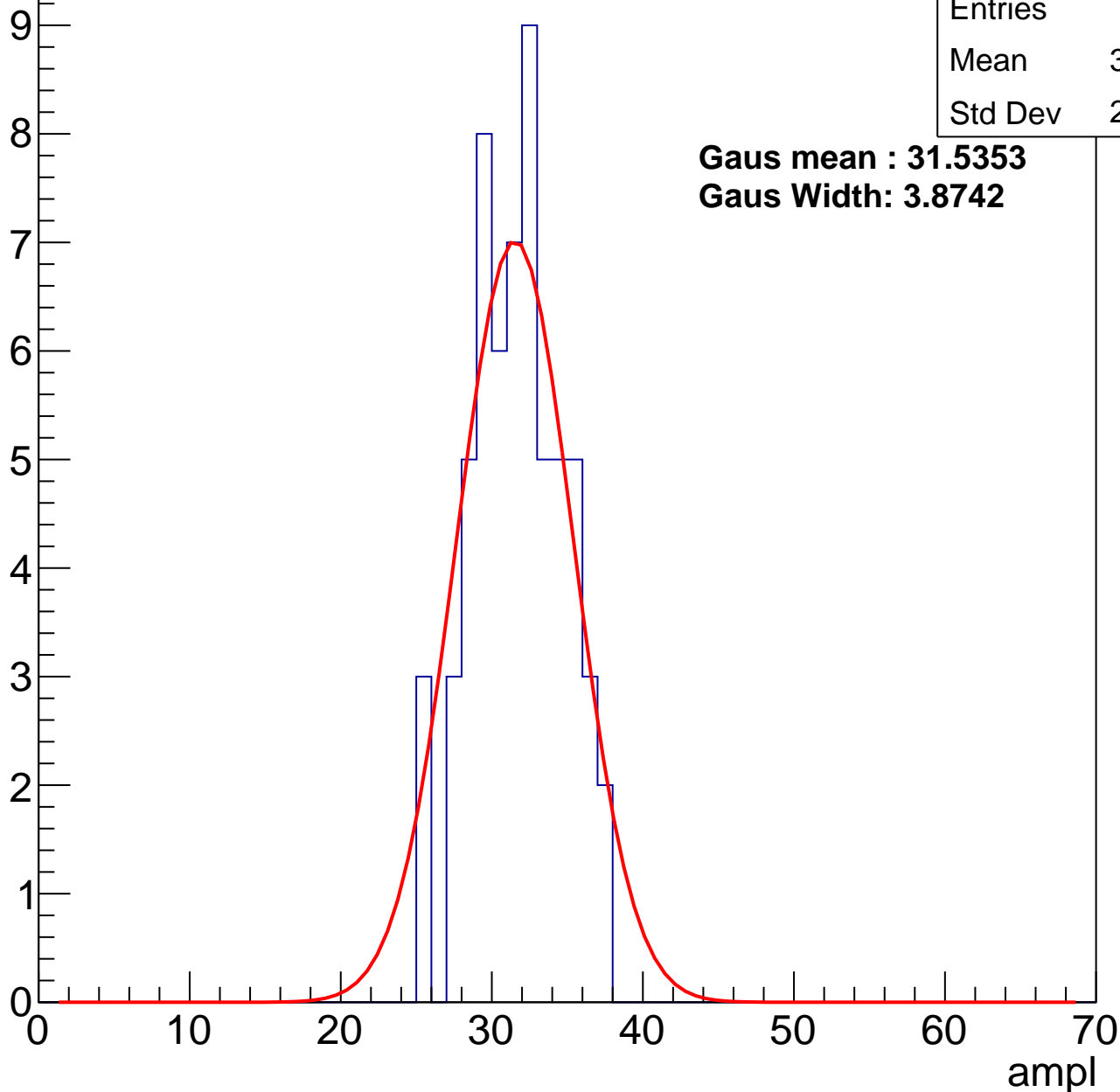
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	61
Mean	31.23
Std Dev	2.966

**Gaus mean : 31.5353**

**Gaus Width: 3.8742**



# B0L000S, U7-ch39, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	77
Mean	38
Std Dev	3.509

**Gaus mean : 38.4780**

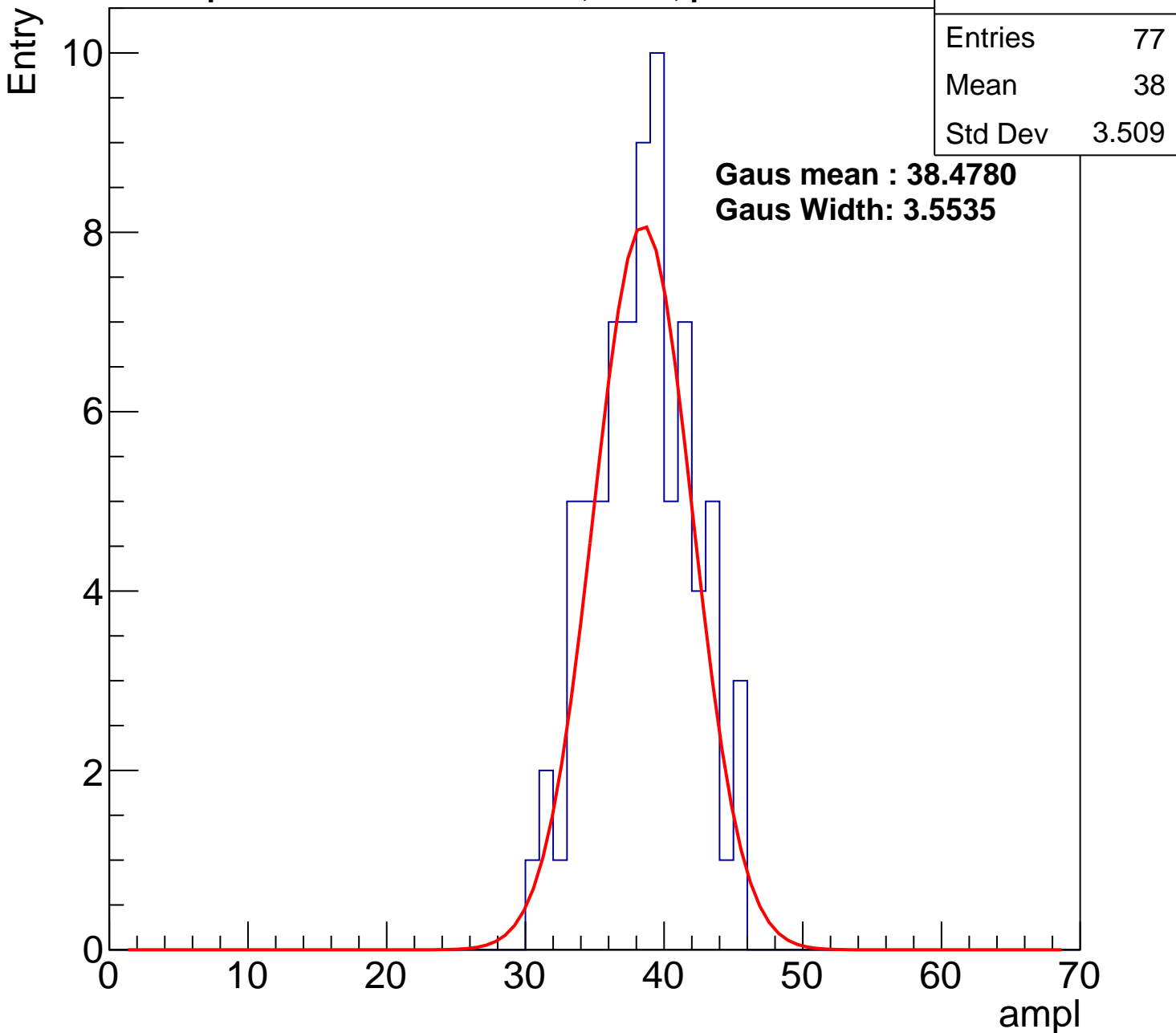
**Gaus Width: 3.5535**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L000S, U7-ch39, adc2

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	82
Mean	45.83
Std Dev	3.618

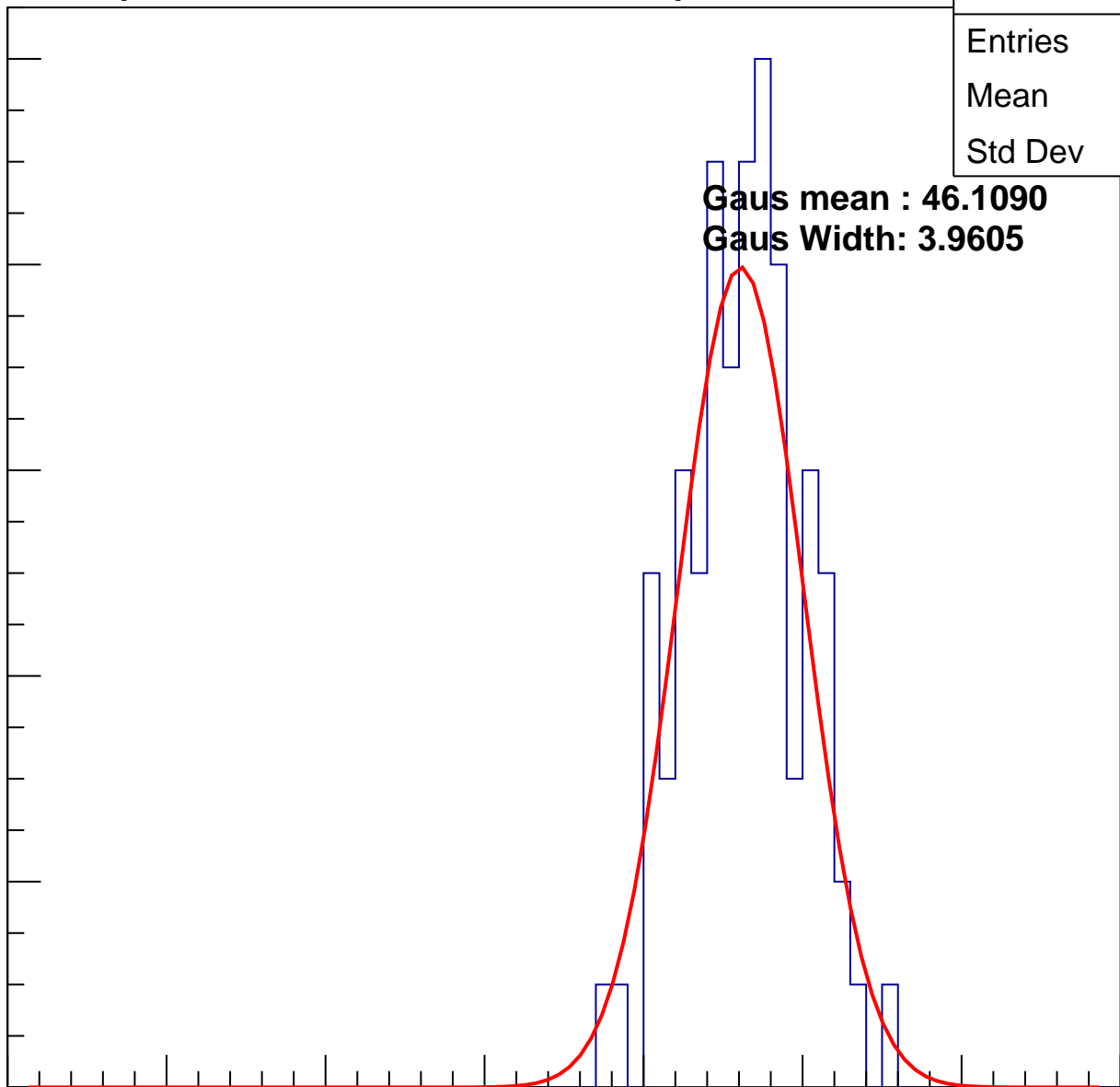
**Gaus mean : 46.1090**

**Gaus Width: 3.9605**

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

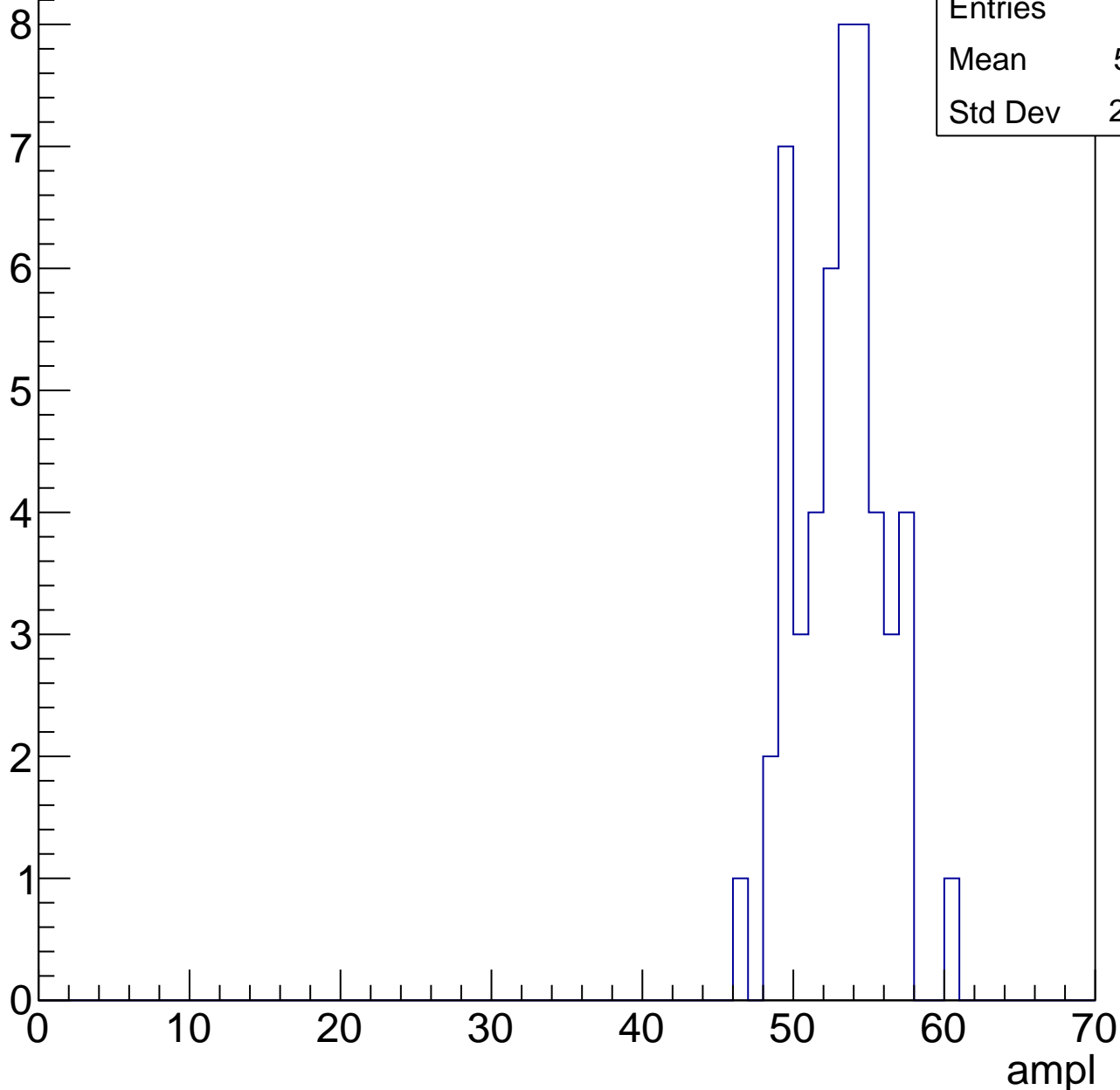


# B0L000S, U7-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	51
Mean	52.61
Std Dev	2.857



# B0L000S, U7-ch39, adc4

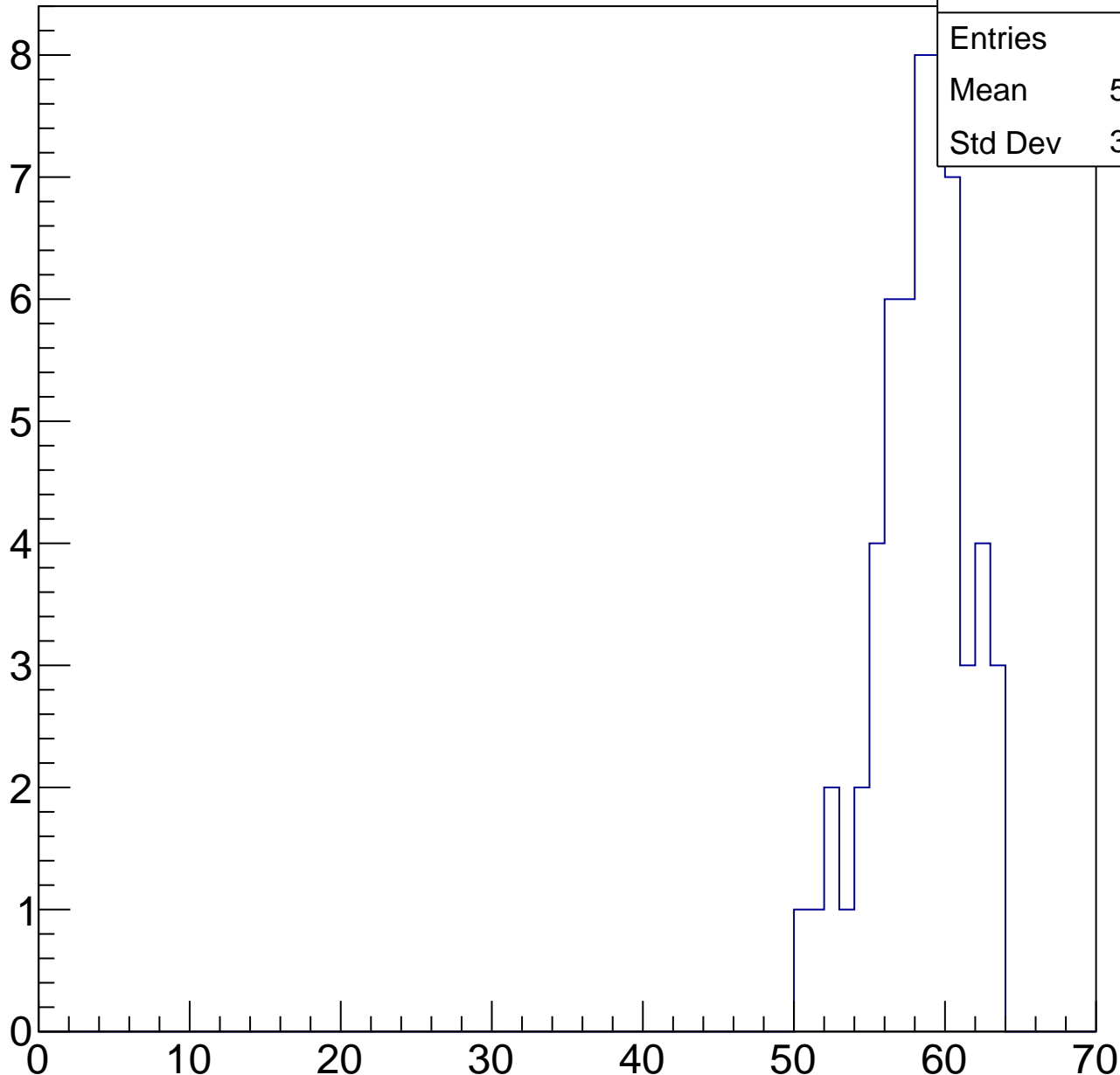
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	56
Mean	57.86
Std Dev	3.014

ampl

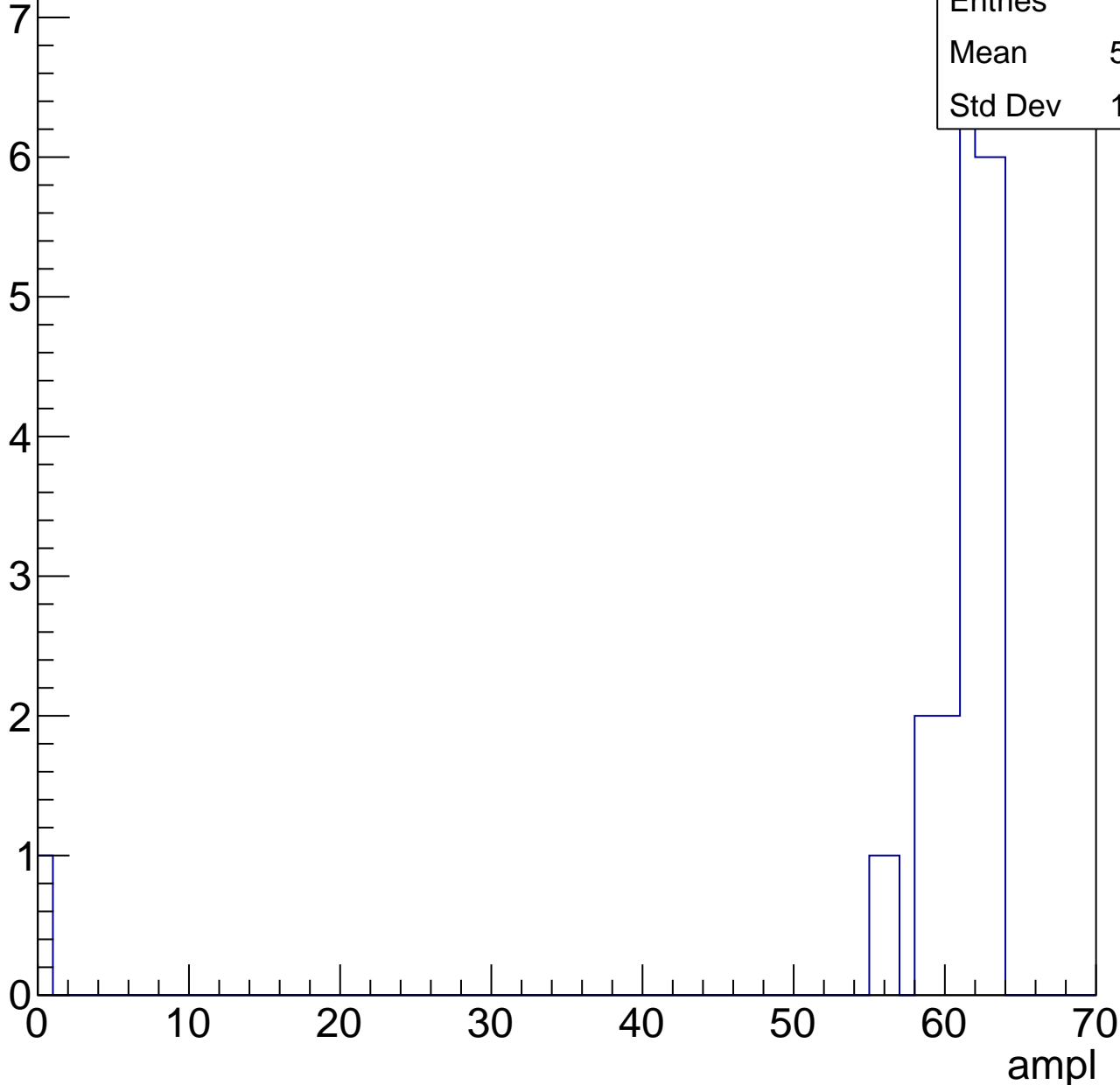


# B0L000S, U7-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	28
Mean	58.64
Std Dev	11.47



# B0L000S, U7-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch40, adc0

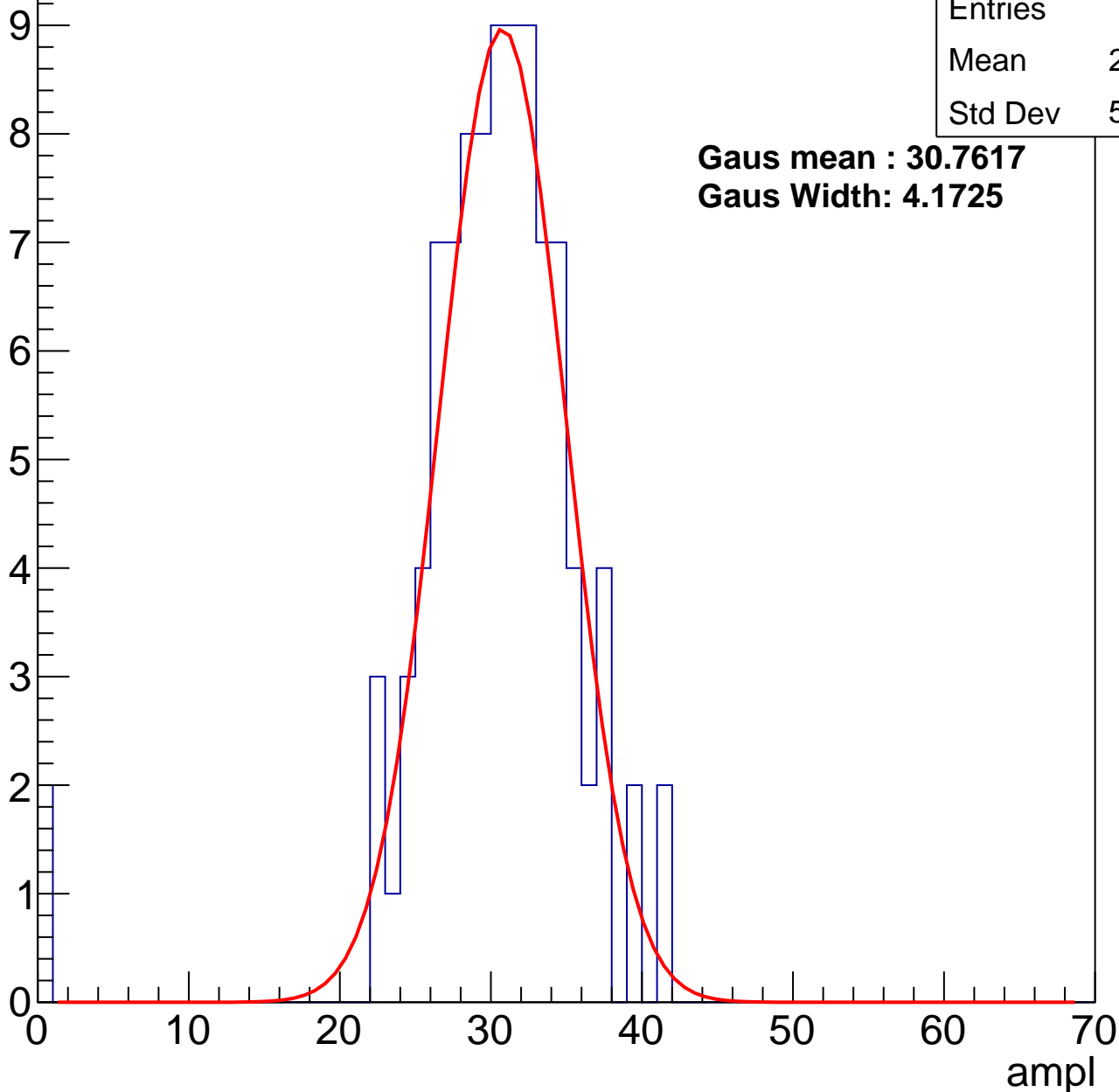
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	98
Mean	29.73
Std Dev	5.933

**Gaus mean : 30.7617**

**Gaus Width: 4.1725**



# B0L000S, U7-ch40, adc1

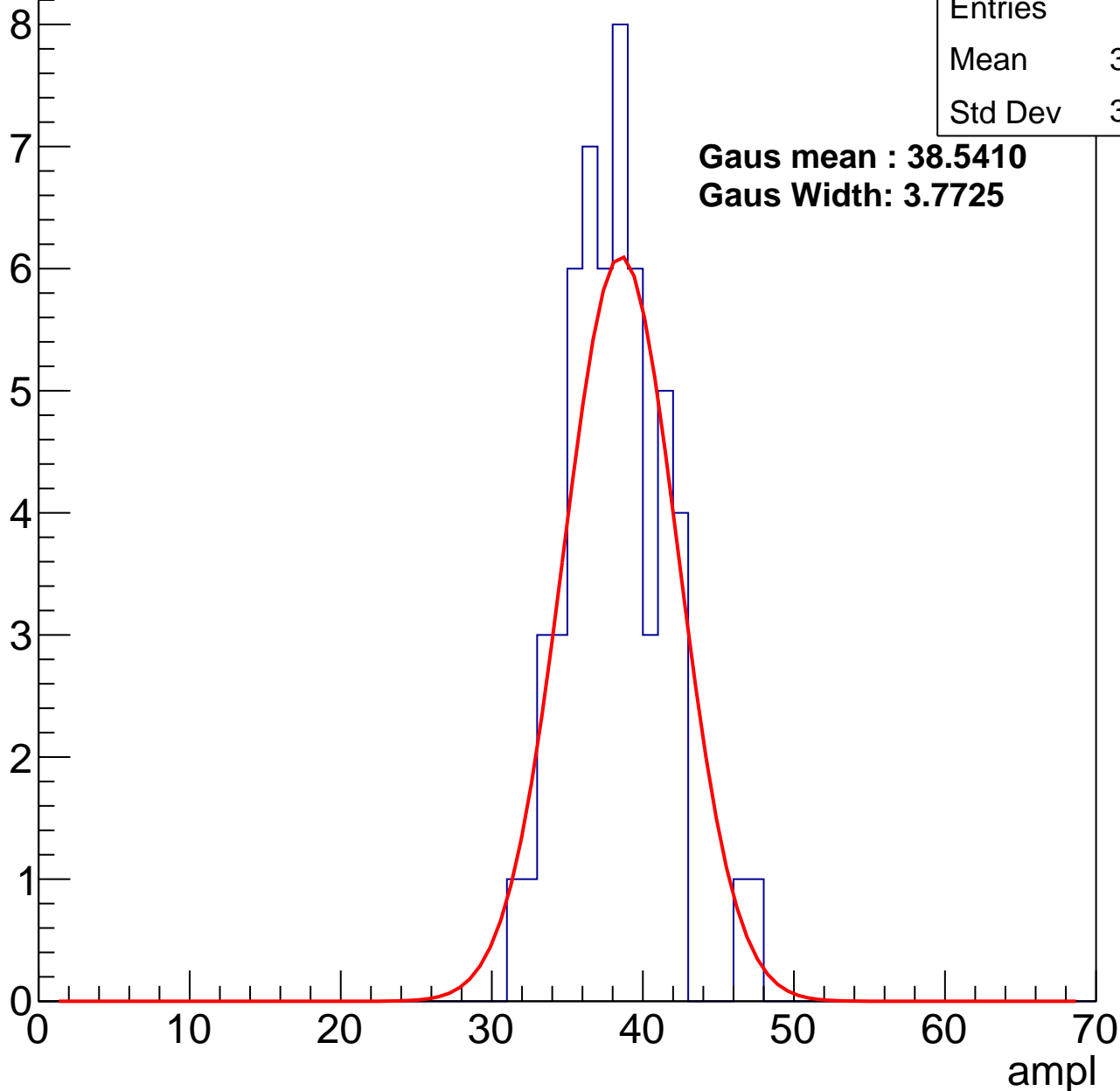
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	55
Mean	37.67
Std Dev	3.197

**Gaus mean : 38.5410**

**Gaus Width: 3.7725**



# B0L000S, U7-ch40, adc2

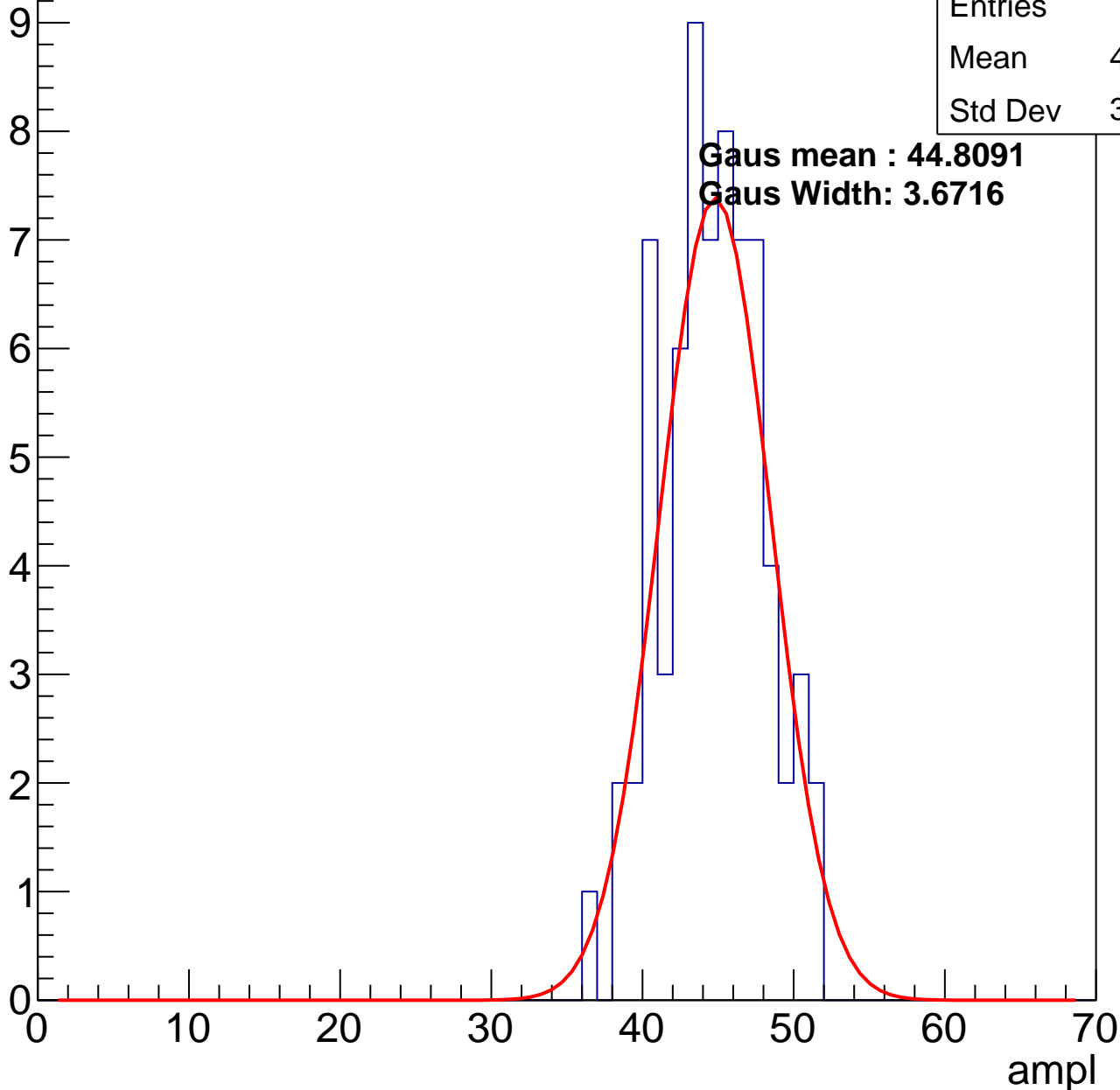
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	70
Mean	44.19
Std Dev	3.326

**Gaus mean : 44.8091**

**Gaus Width: 3.6716**

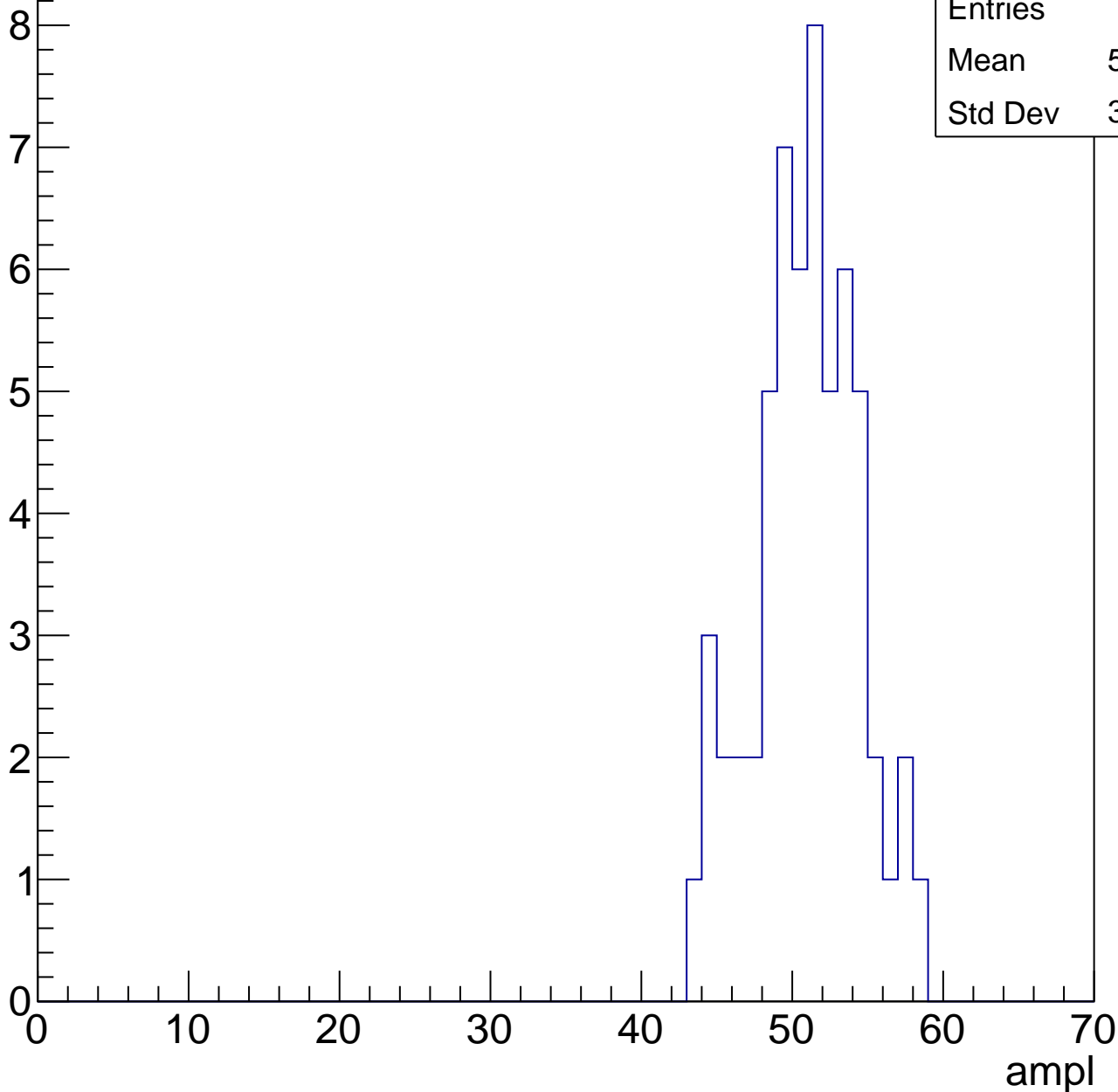


# B0L000S, U7-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

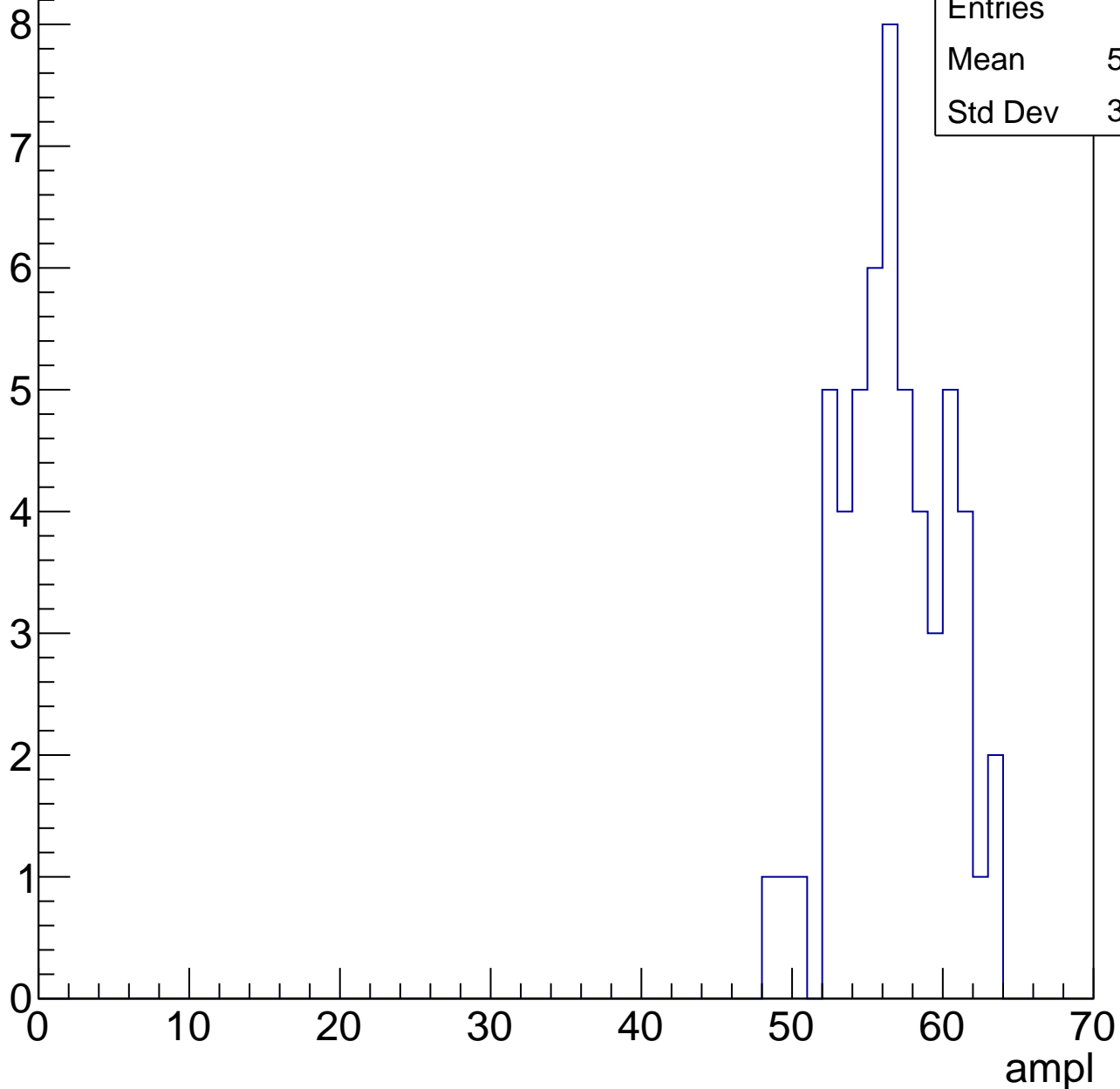
Entries	58
Mean	50.48
Std Dev	3.425



# B0L000S, U7-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



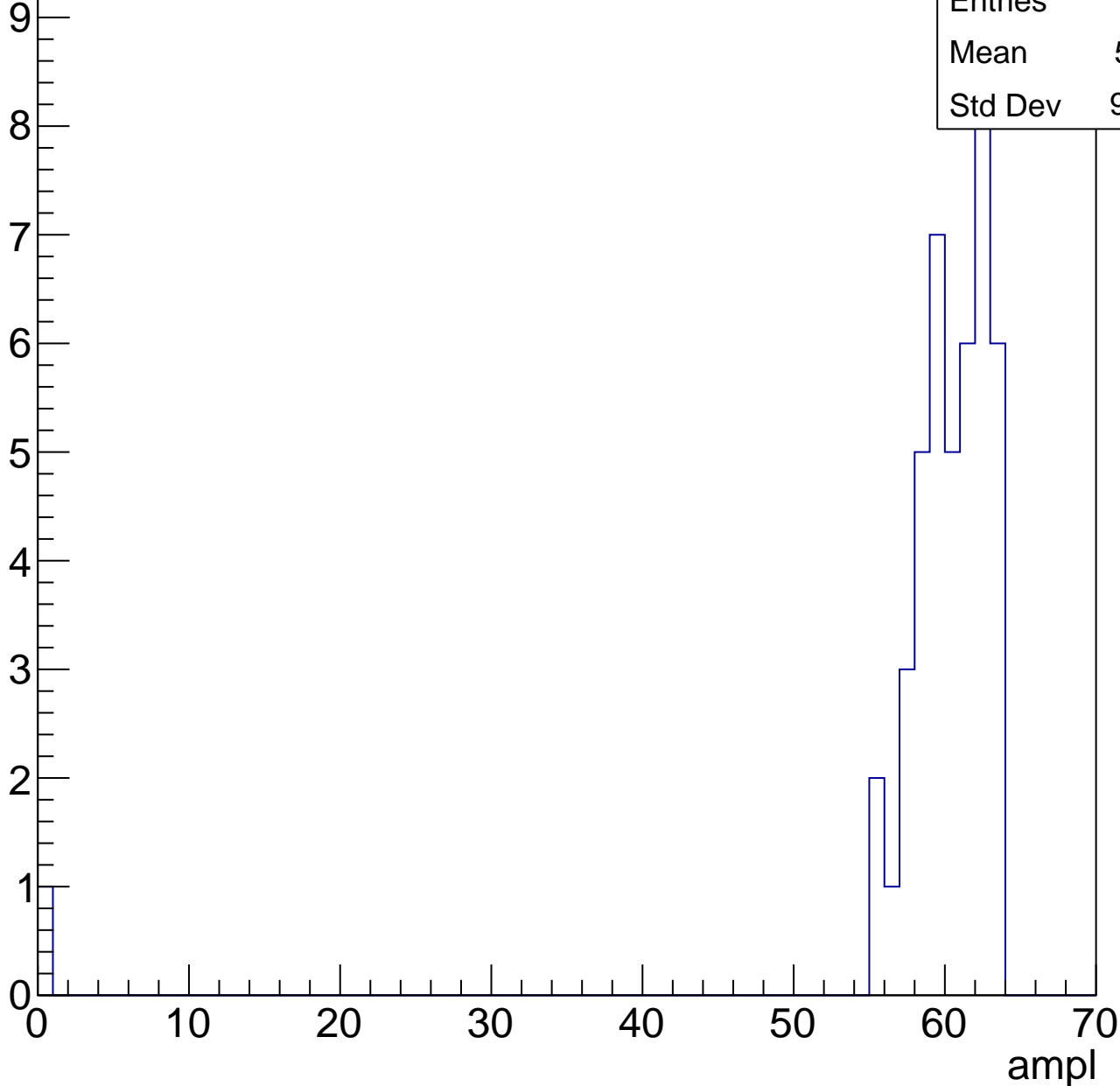
Entries	55
Mean	56.24
Std Dev	3.438

# B0L000S, U7-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	45
Mean	58.71
Std Dev	9.118



# B0L000S, U7-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch41, adc0

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	86
Mean	29.2
Std Dev	4.783

**Gaus mean : 29.9751**

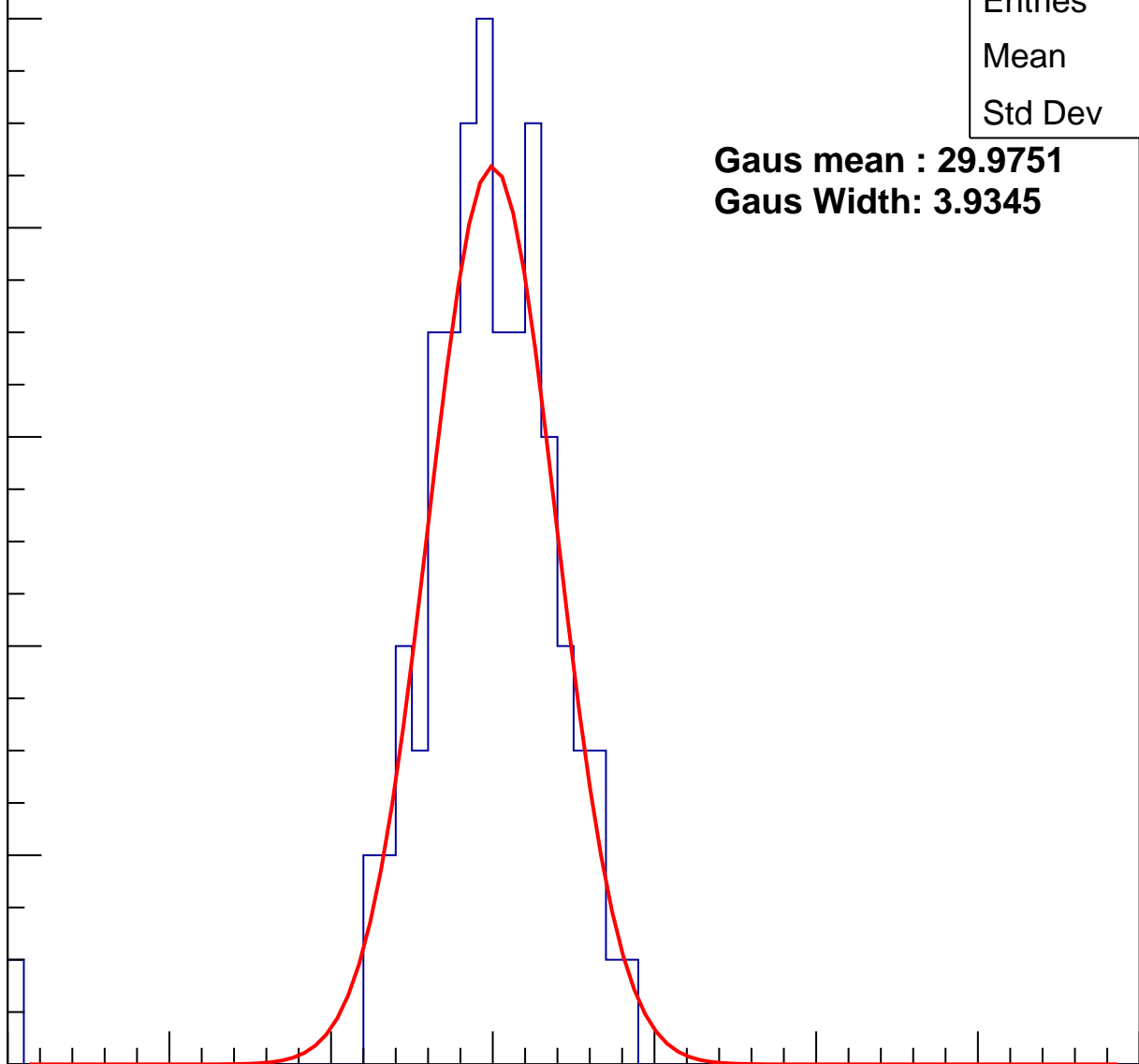
**Gaus Width: 3.9345**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L000S, U7-ch41, adc1

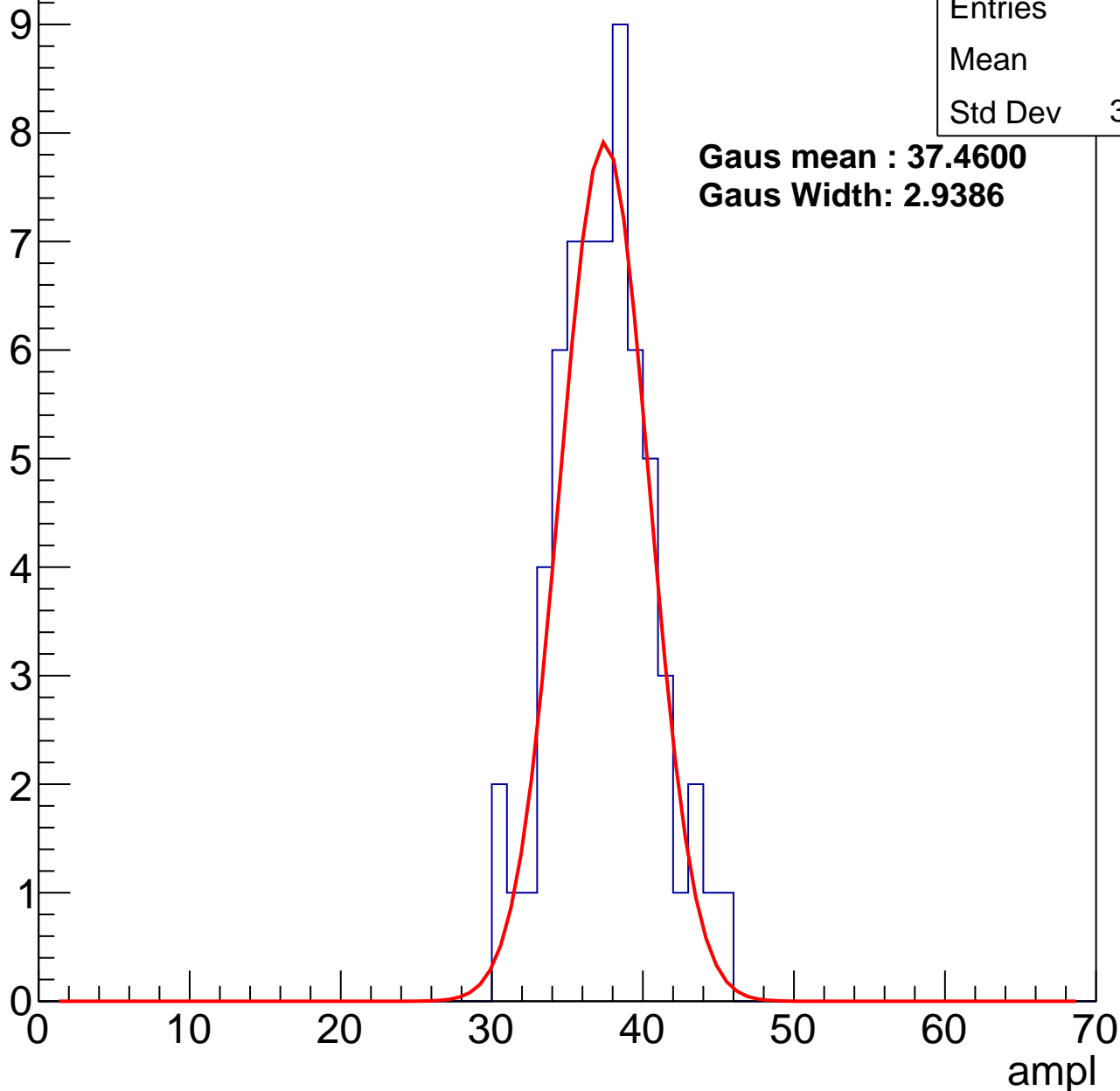
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	63
Mean	37
Std Dev	3.207

**Gaus mean : 37.4600**

**Gaus Width: 2.9386**



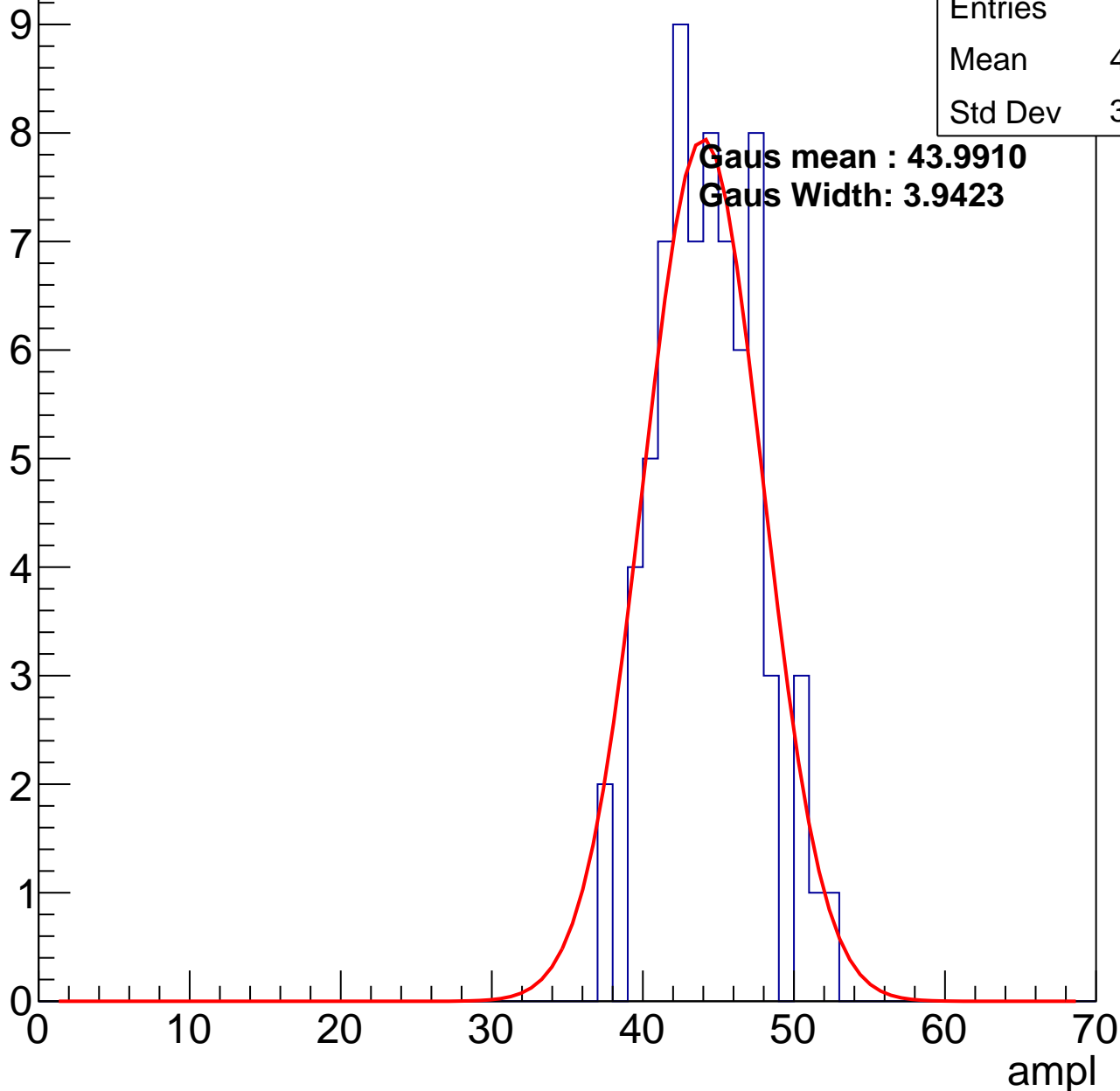
# B0L000S, U7-ch41, adc2

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	71
Mean	43.83
Std Dev	3.259

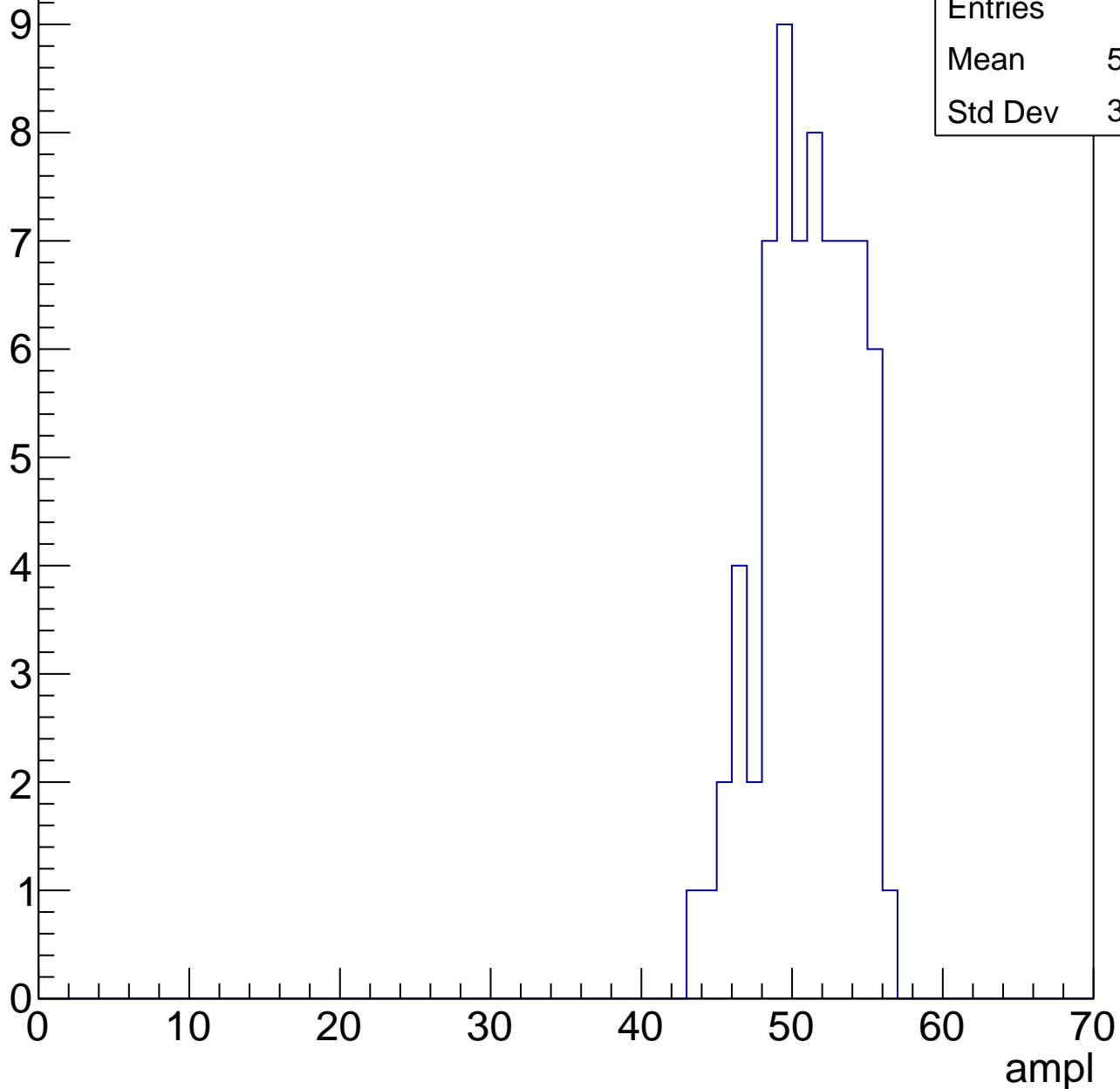
**Gaus mean : 43.9910**  
**Gaus Width: 3.9423**



# B0L000S, U7-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	69
Mean	50.57
Std Dev	3.019

# B0L000S, U7-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	61
Mean	57.44
Std Dev	3.011

Entry

10

8

6

4

2

0

0

10

20

30

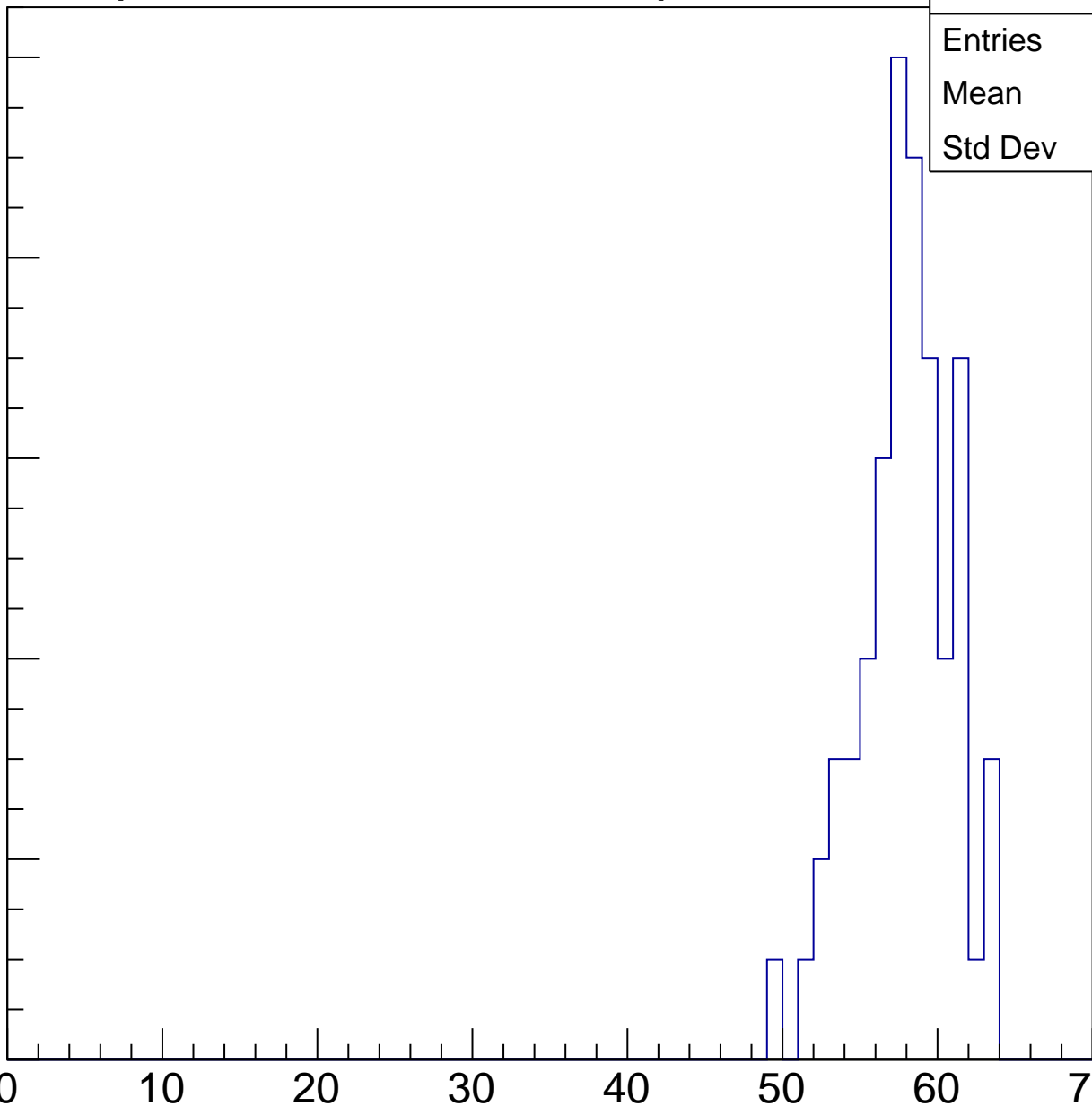
40

50

60

70

ampl

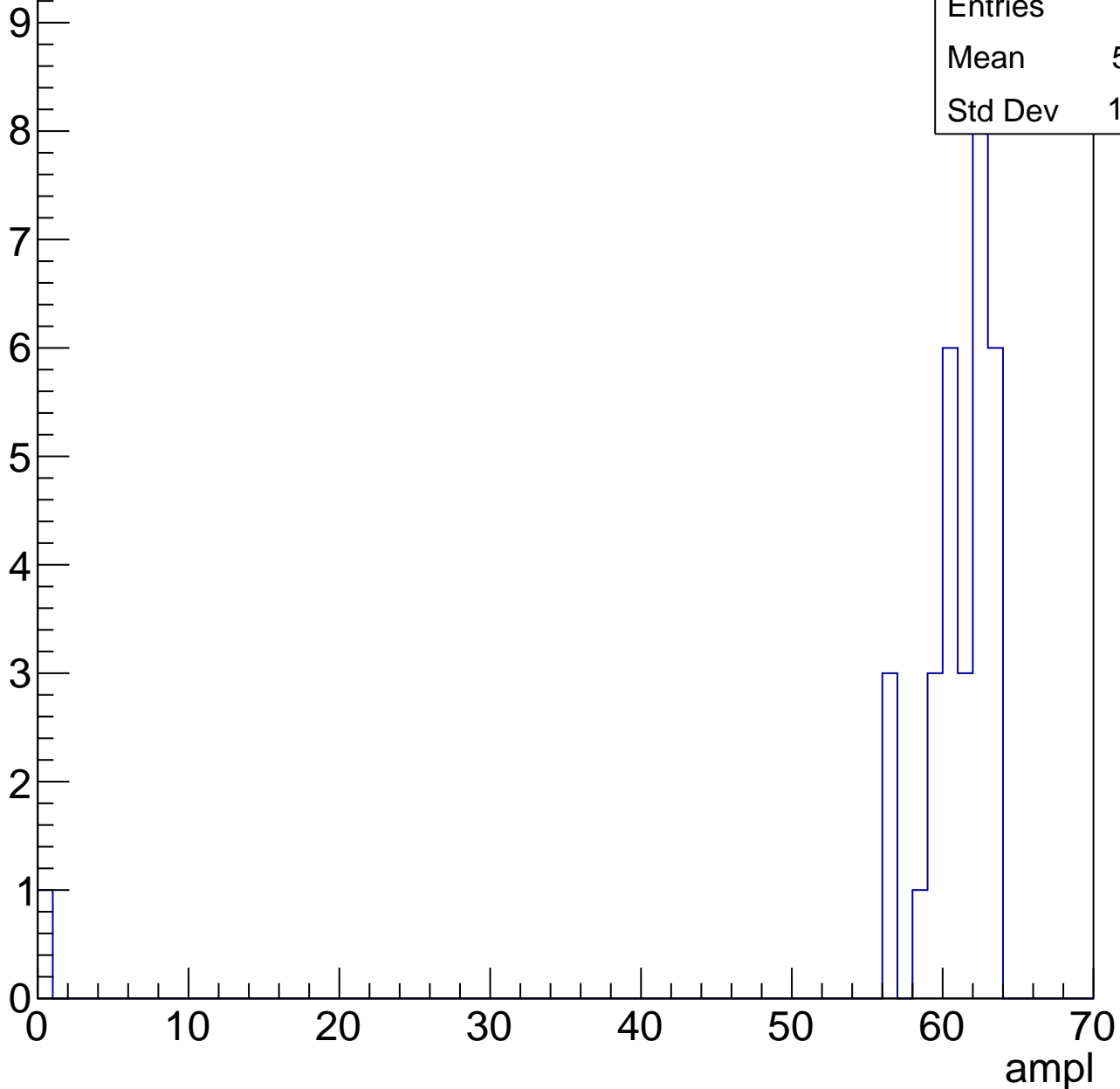


# B0L000S, U7-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

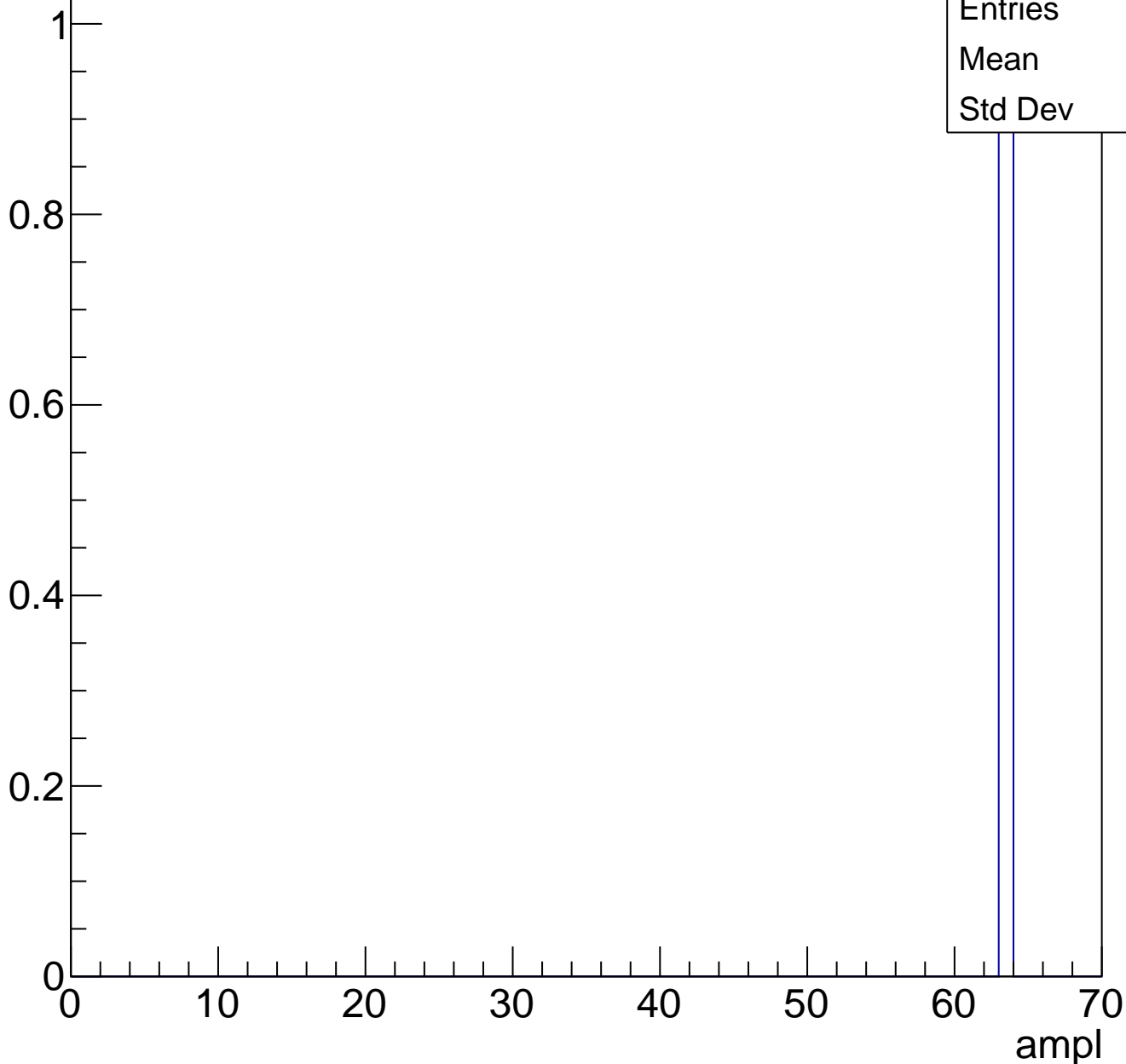
Entries	32
Mean	58.81
Std Dev	10.76



# B0L000S, U7-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	1
Mean	63
Std Dev	0



# B0L000S, U7-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch42, adc0

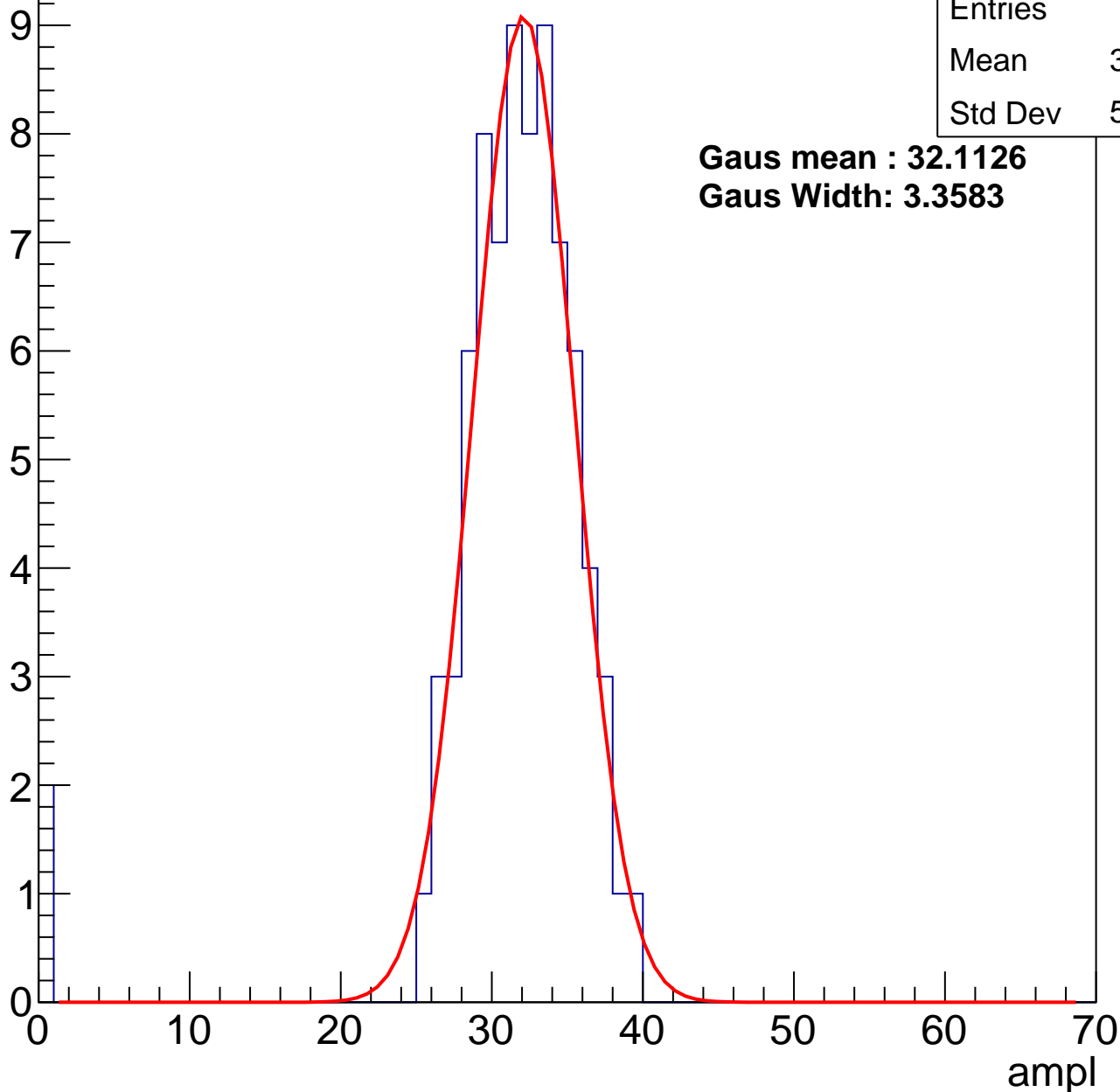
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	78
Mean	30.85
Std Dev	5.879

**Gaus mean : 32.1126**

**Gaus Width: 3.3583**



# B0L000S, U7-ch42, adc1

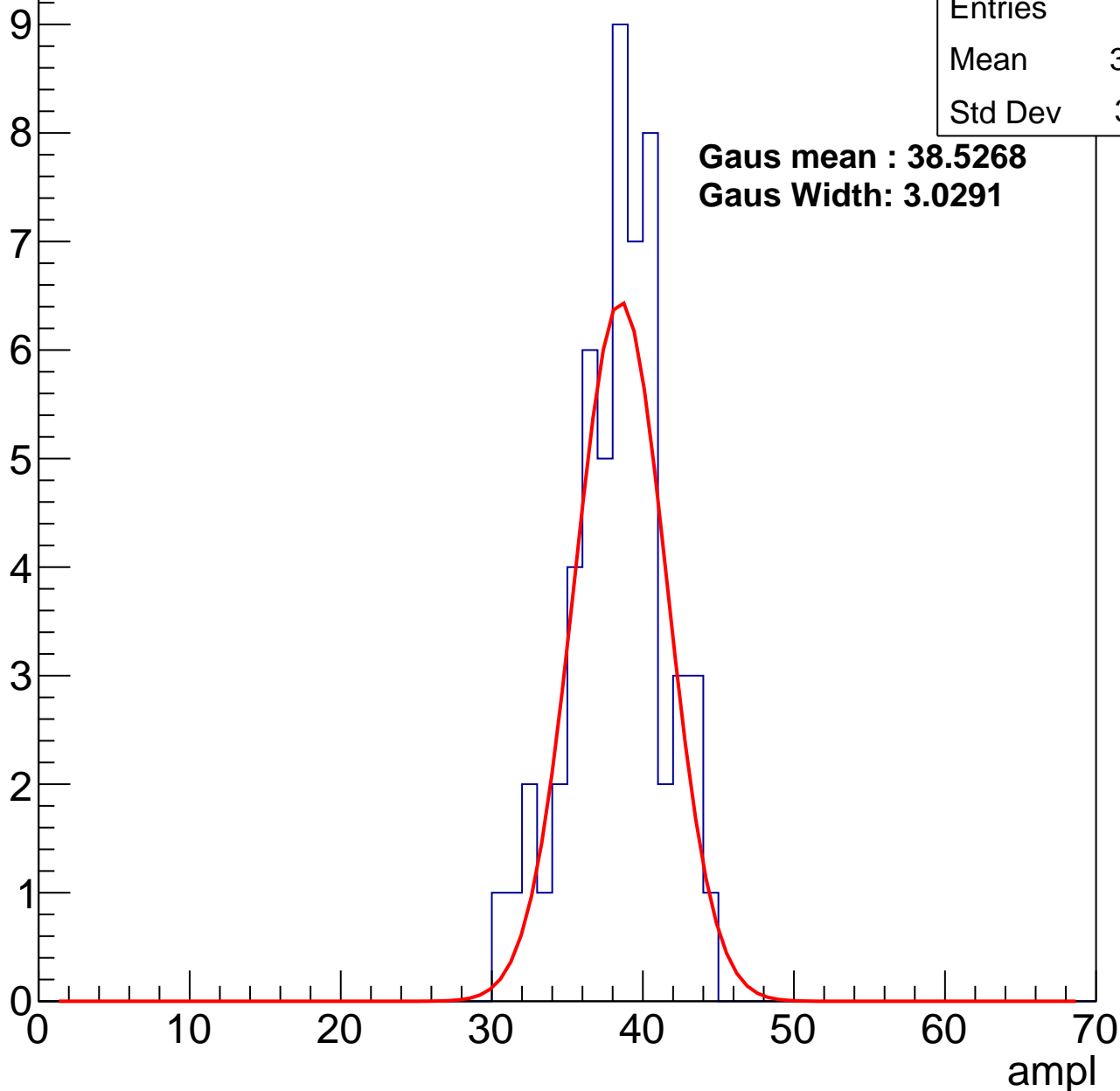
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	55
Mean	37.87
Std Dev	3.081

**Gaus mean : 38.5268**

**Gaus Width: 3.0291**



# B0L000S, U7-ch42, adc2

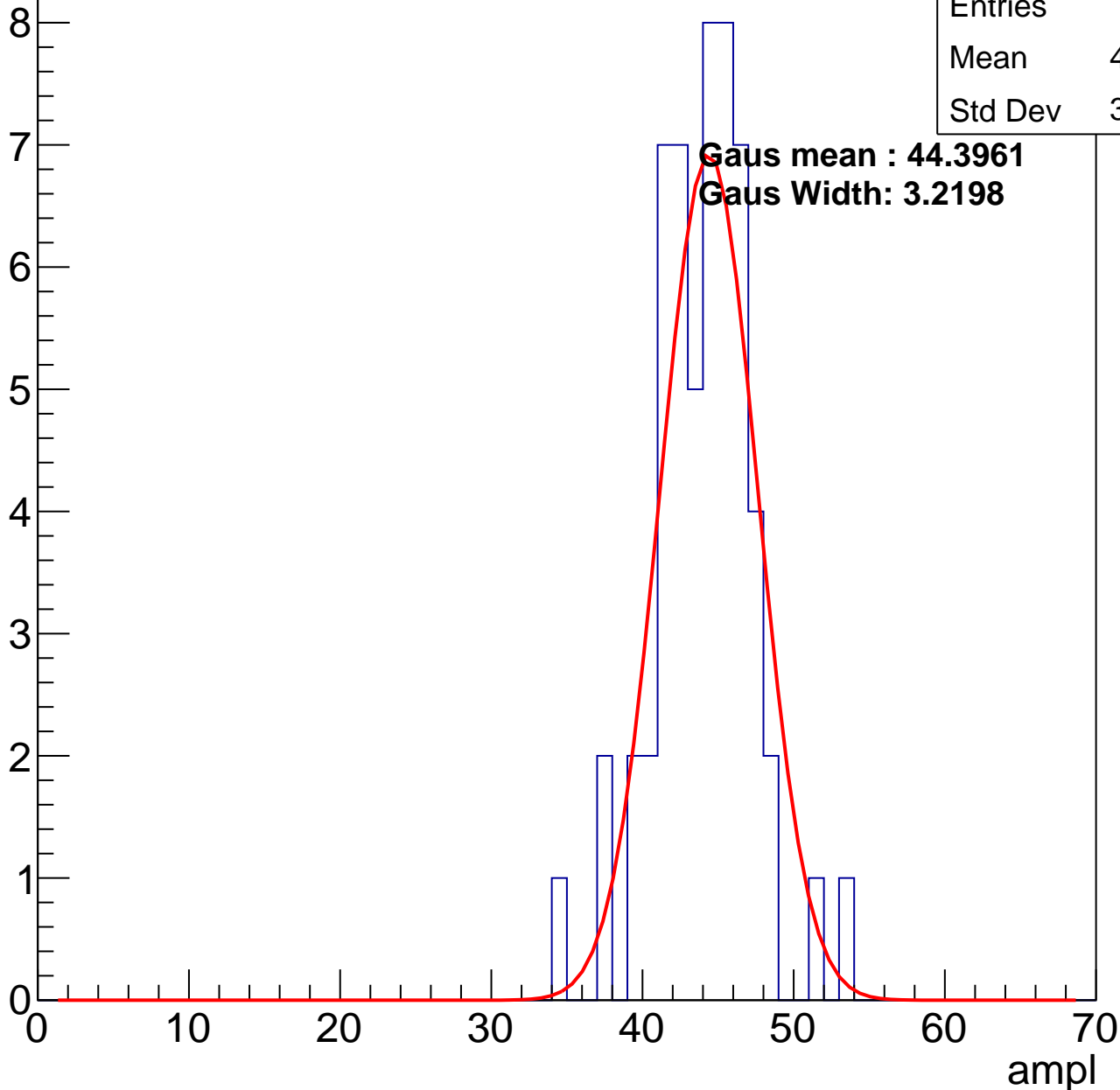
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	57
Mean	43.58
Std Dev	3.244

**Gaus mean : 44.3961**

**Gaus Width: 3.2198**



# B0L000S, U7-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

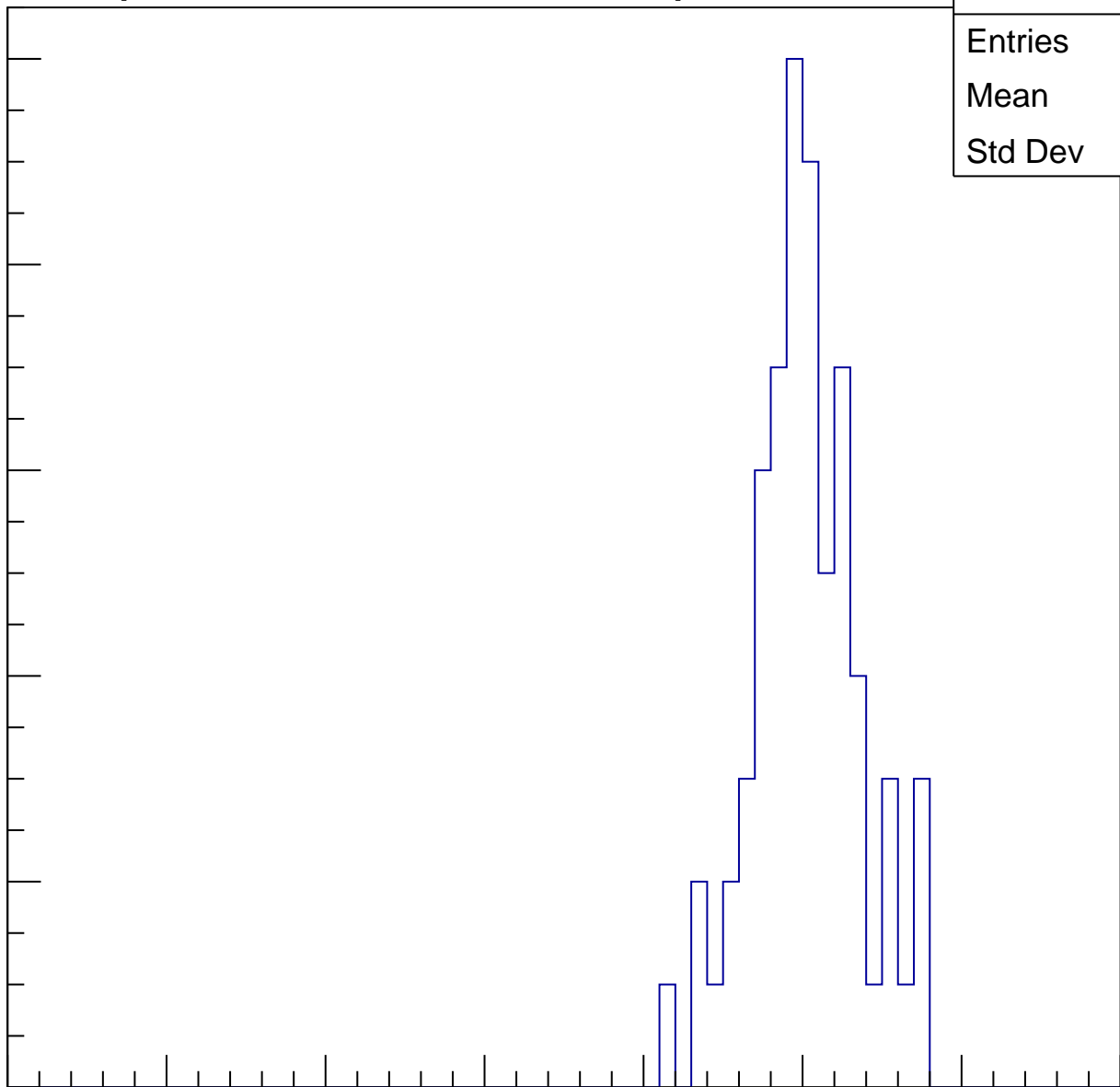
Entries	65
Mean	49.75
Std Dev	3.383

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

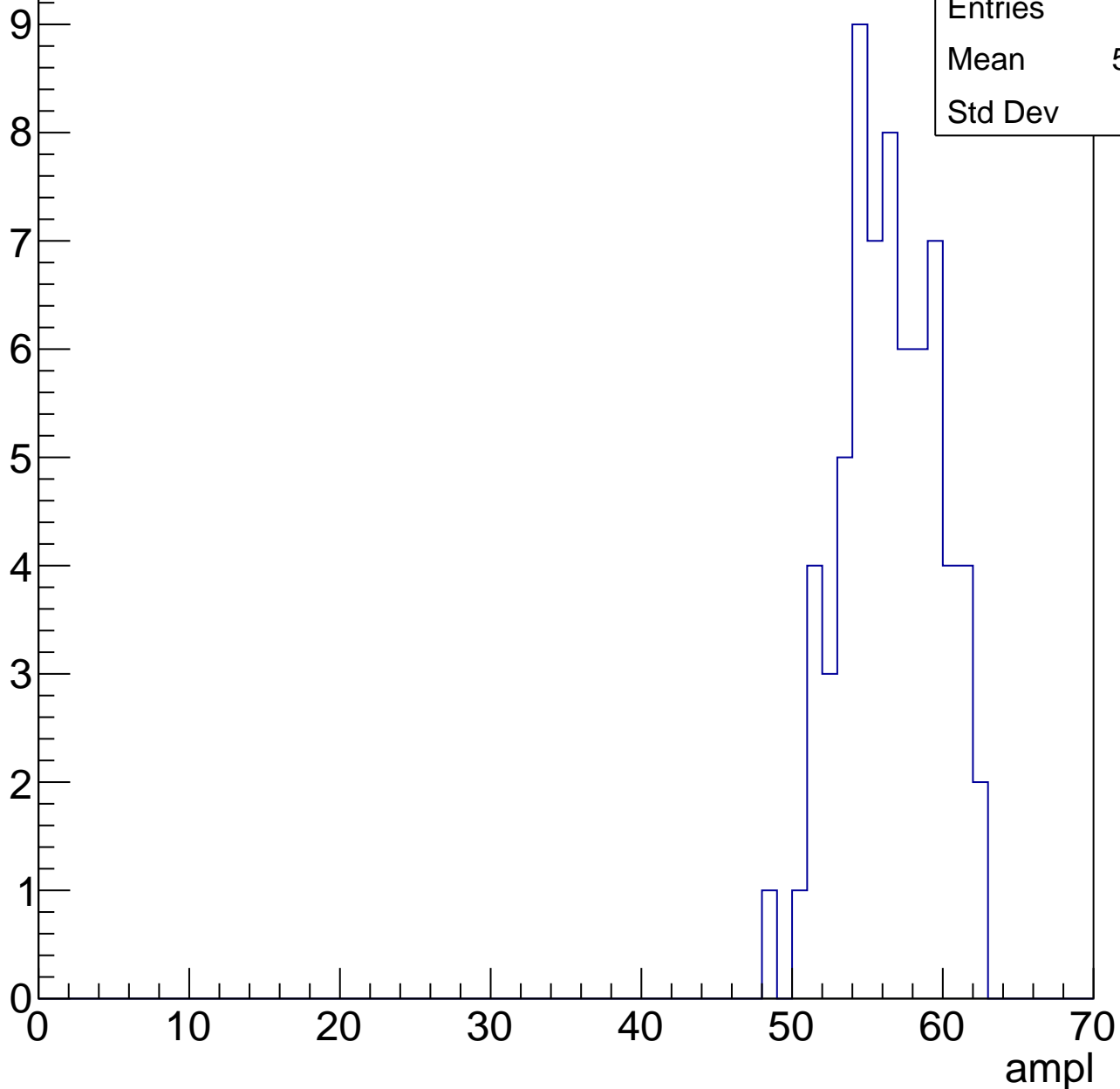
ampl



# B0L000S, U7-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



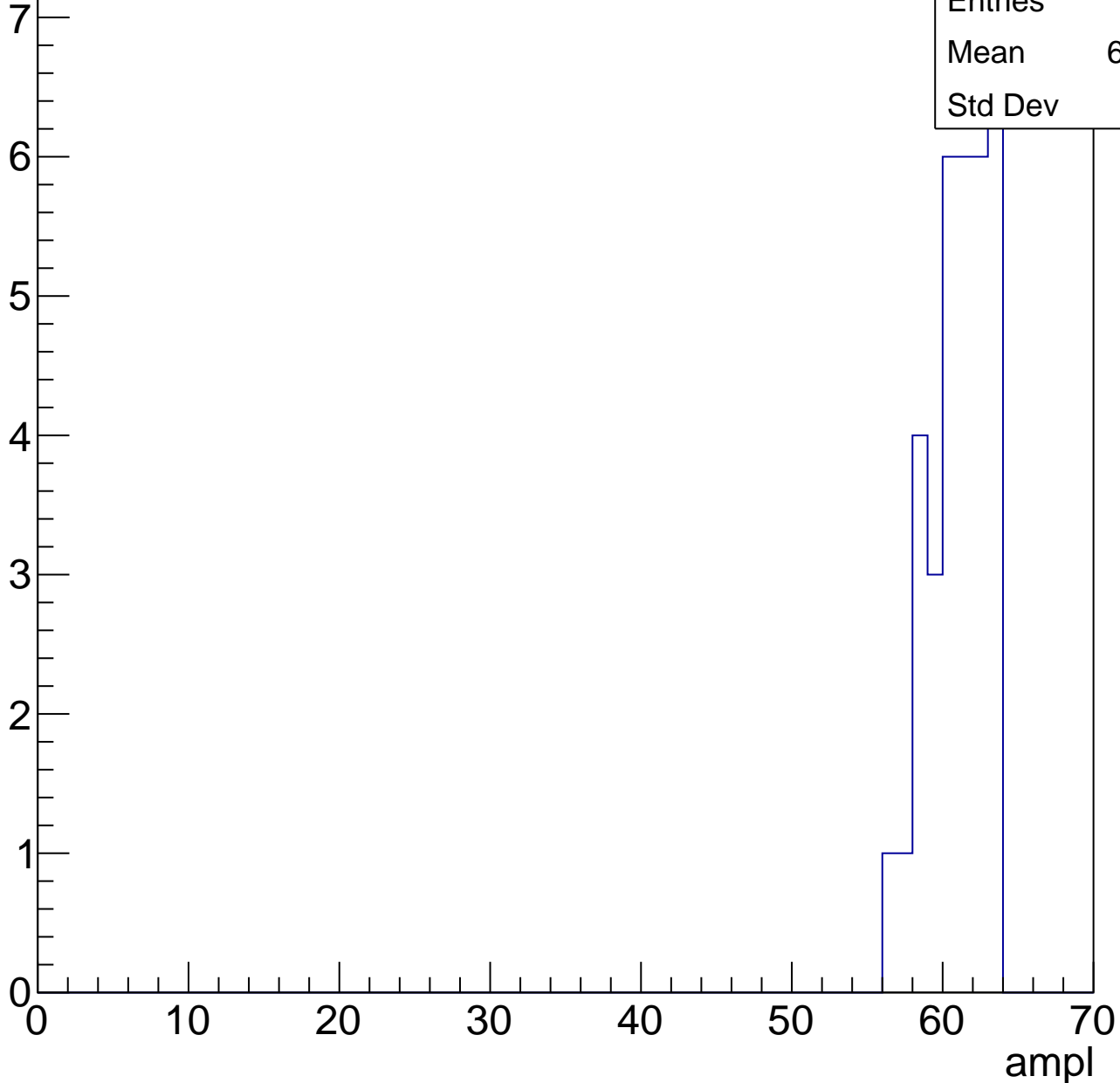
Entries	67
Mean	56.01
Std Dev	3.15

# B0L000S, U7-ch42, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

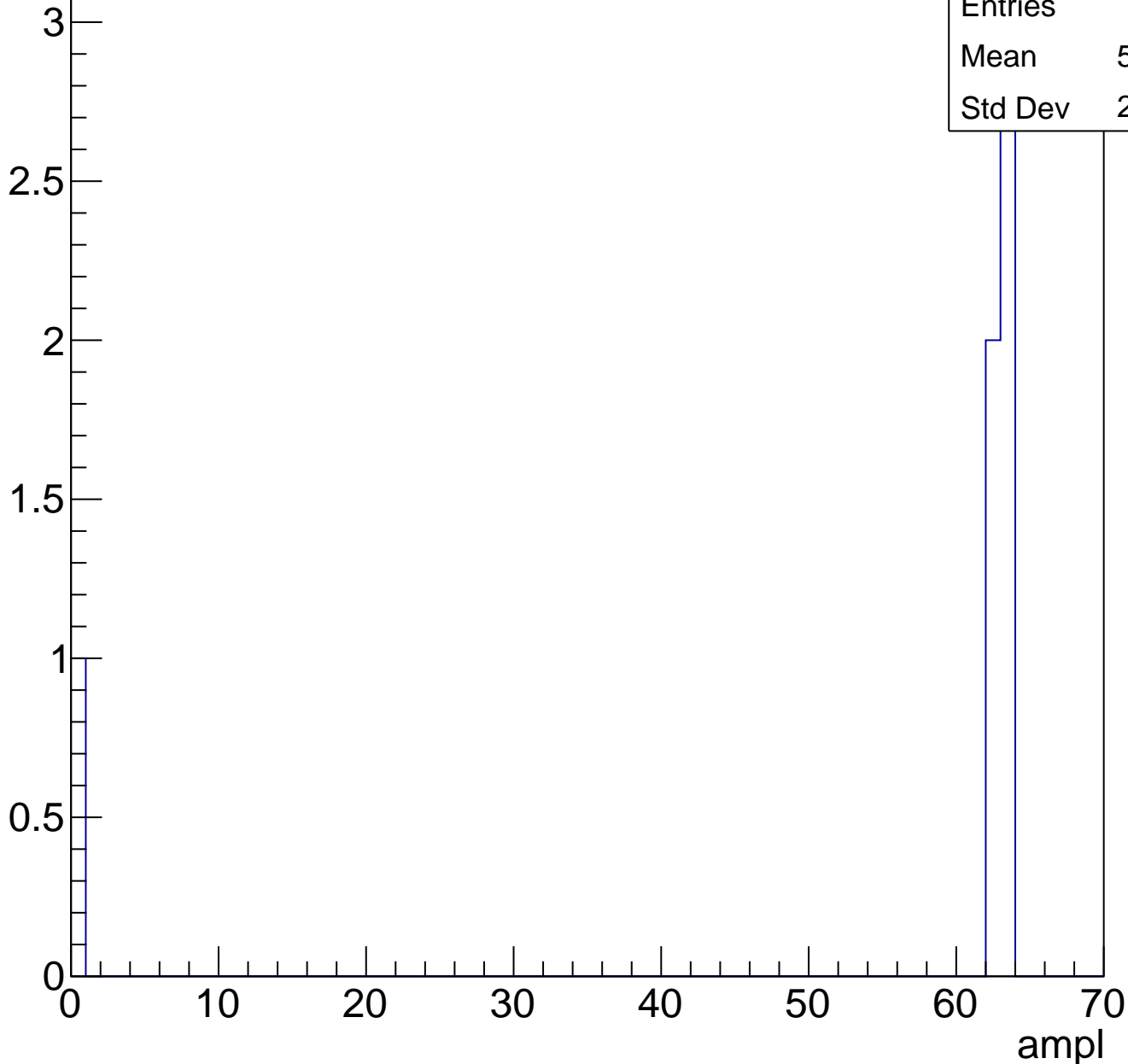
Entries	34
Mean	60.62
Std Dev	1.91



# B0L000S, U7-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

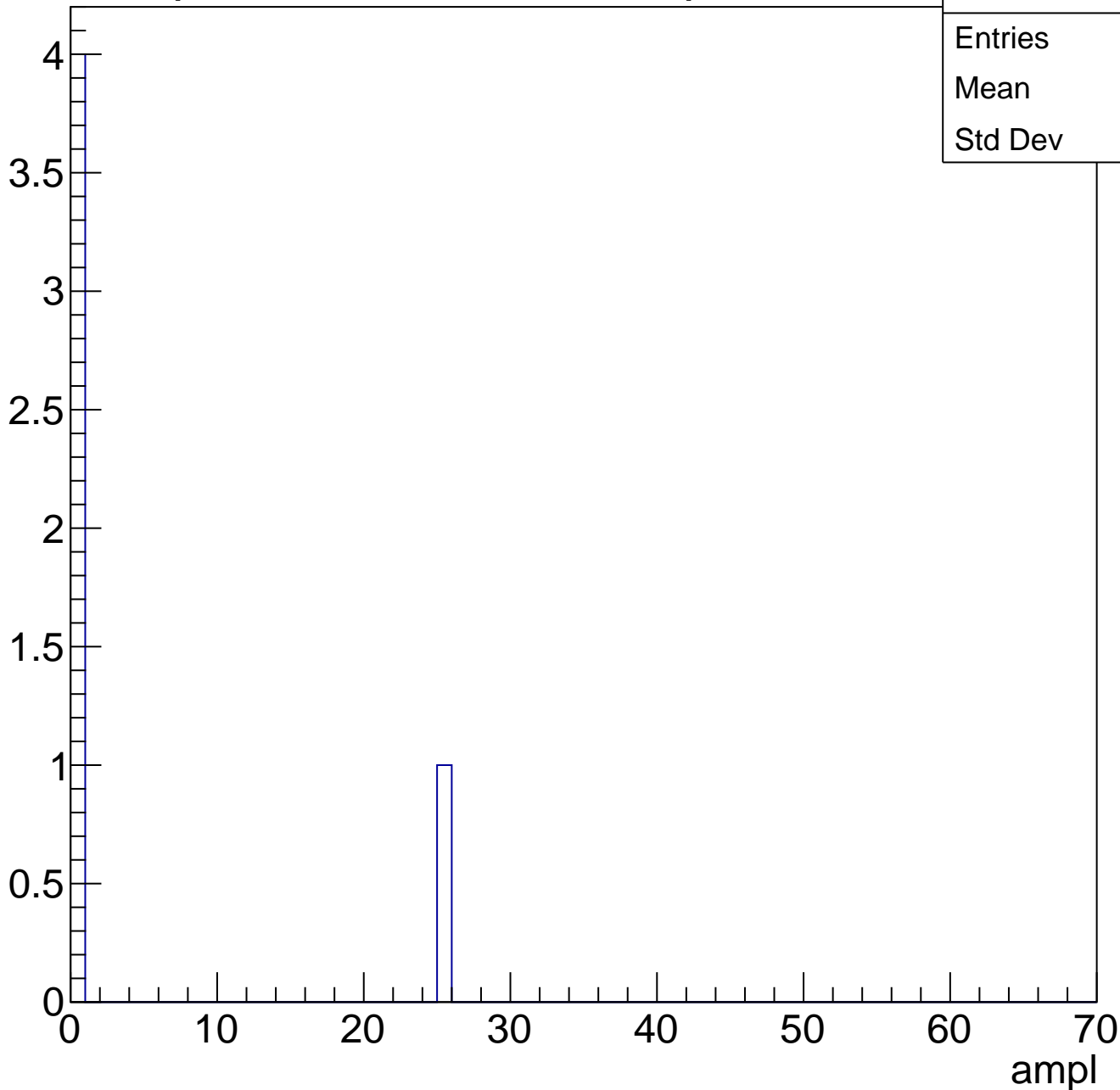




# B0L000S, U7-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	5
Mean	5
Std Dev	10

# B0L000S, U7-ch43, adc0

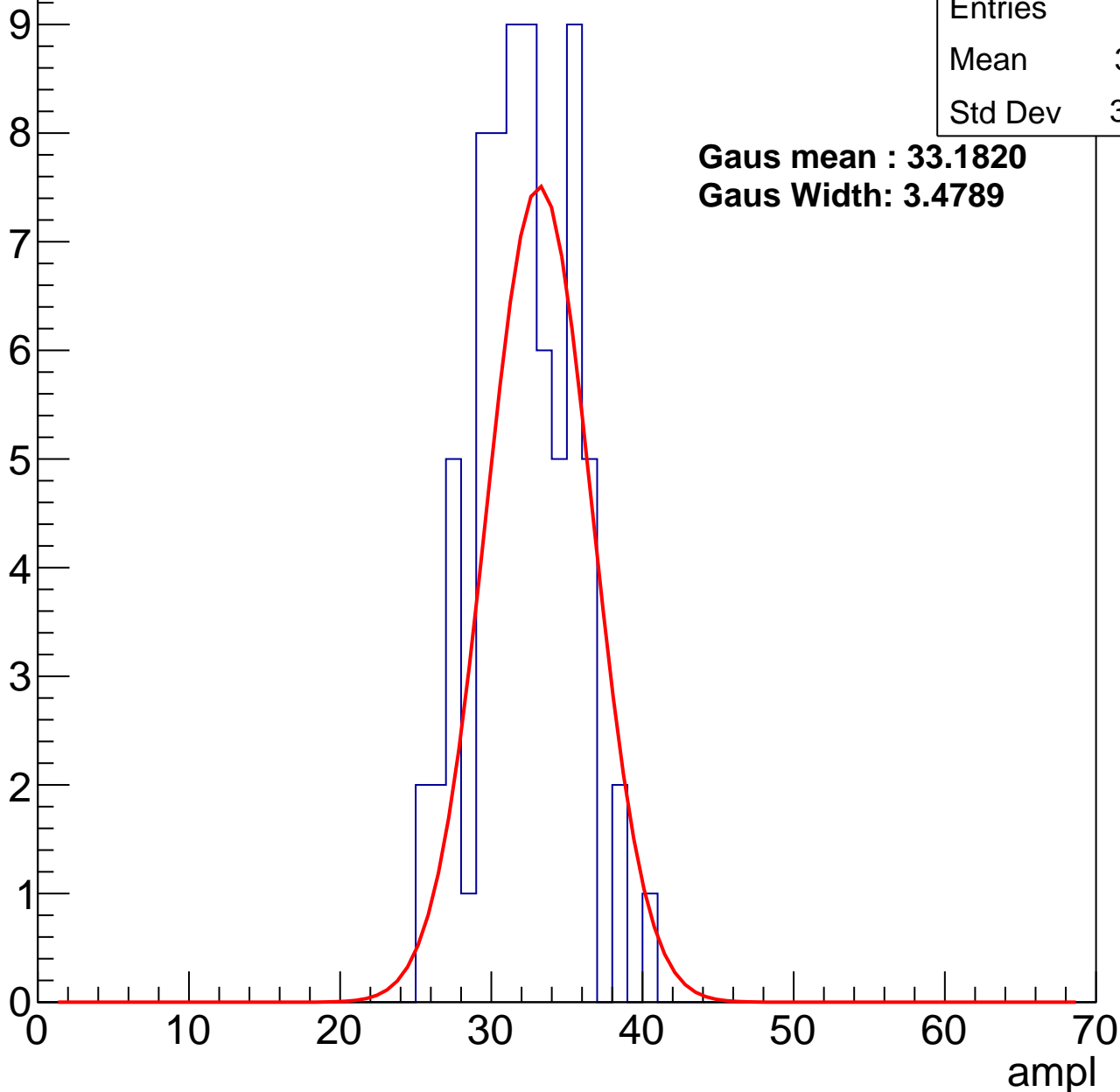
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	72
Mean	31.71
Std Dev	3.208

**Gaus mean : 33.1820**

**Gaus Width: 3.4789**



# B0L000S, U7-ch43, adc1

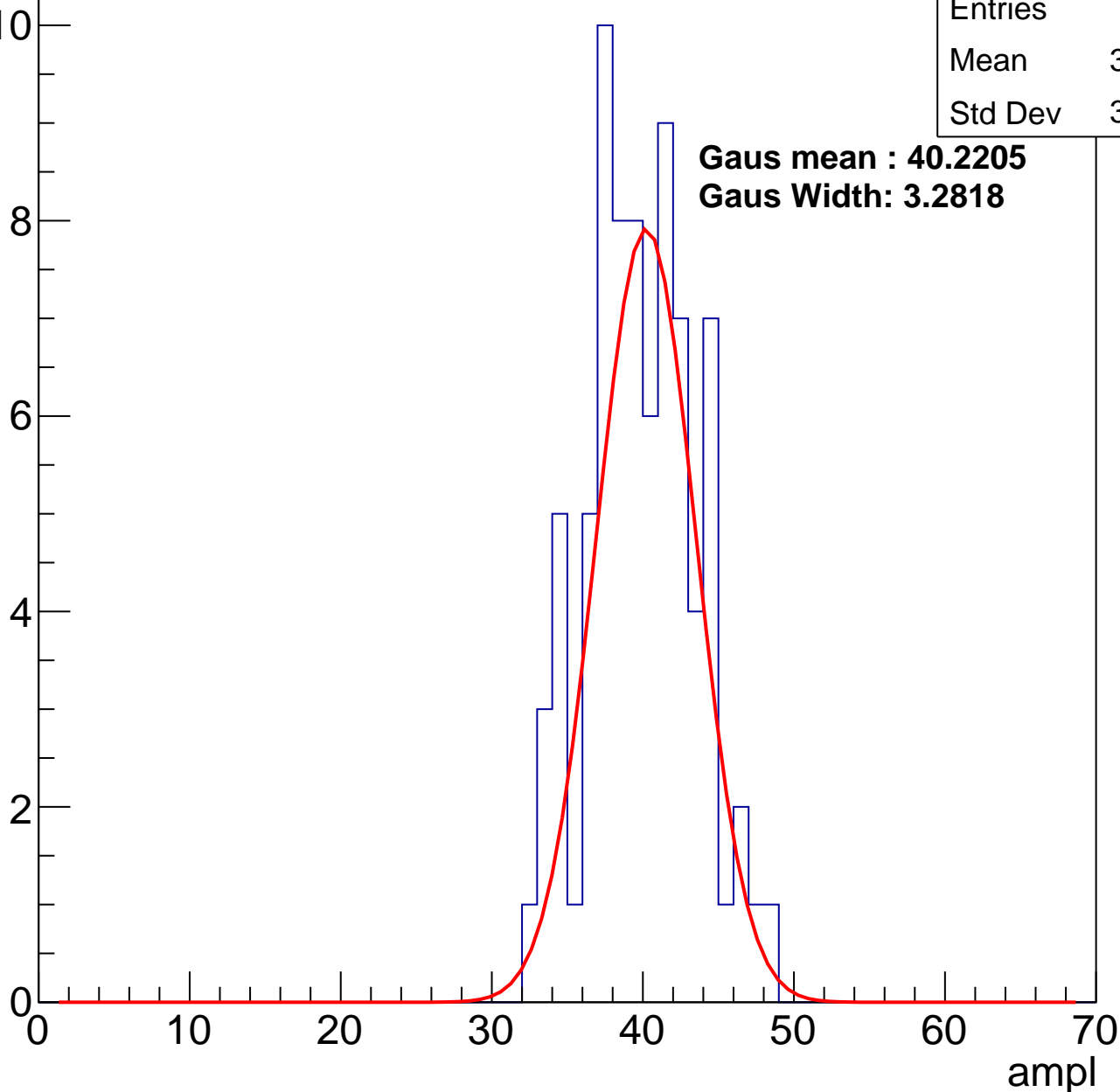
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	79
Mean	39.46
Std Dev	3.554

**Gaus mean : 40.2205**

**Gaus Width: 3.2818**



# B0L000S, U7-ch43, adc2

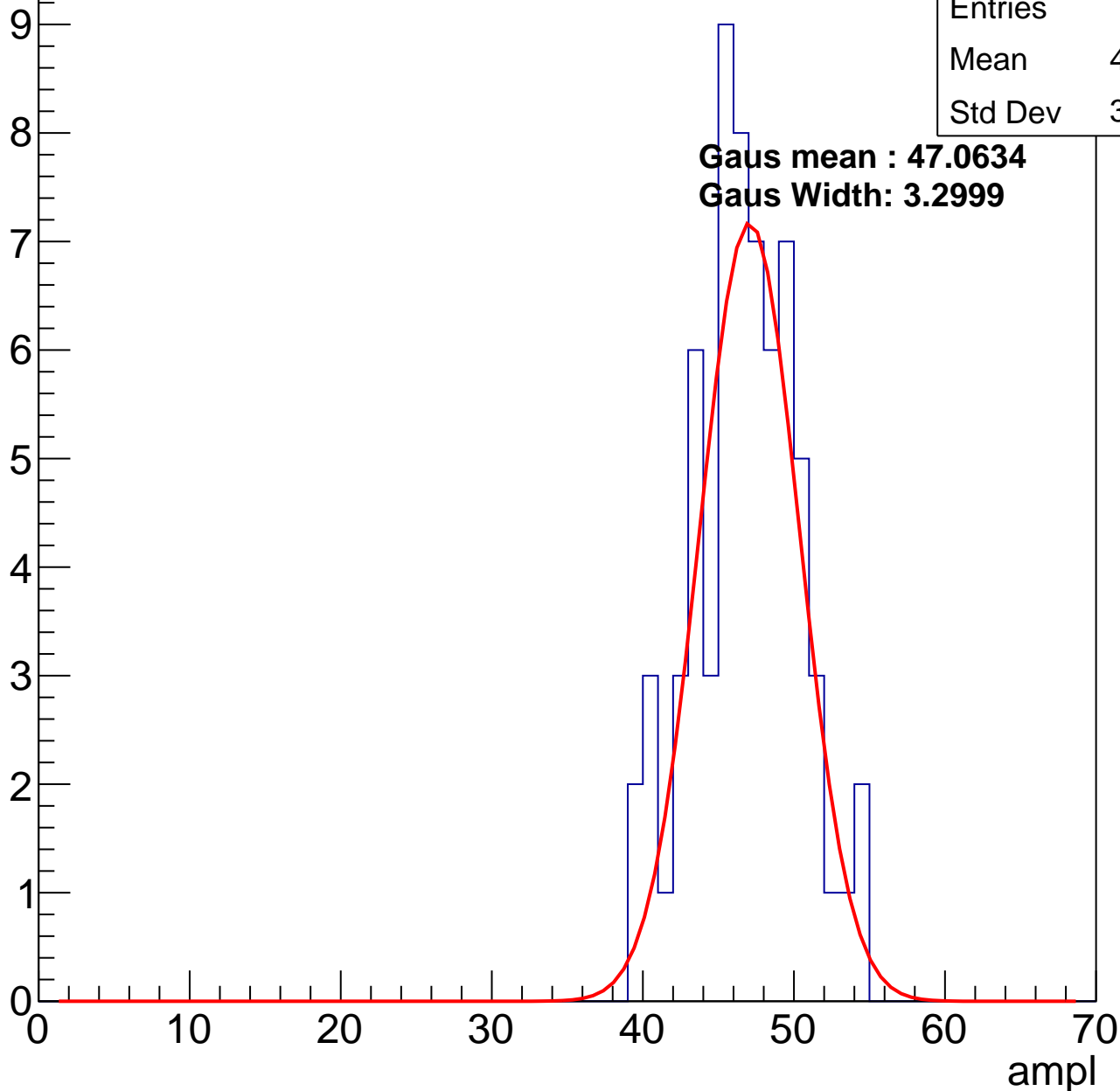
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	67
Mean	46.33
Std Dev	3.474

**Gaus mean : 47.0634**

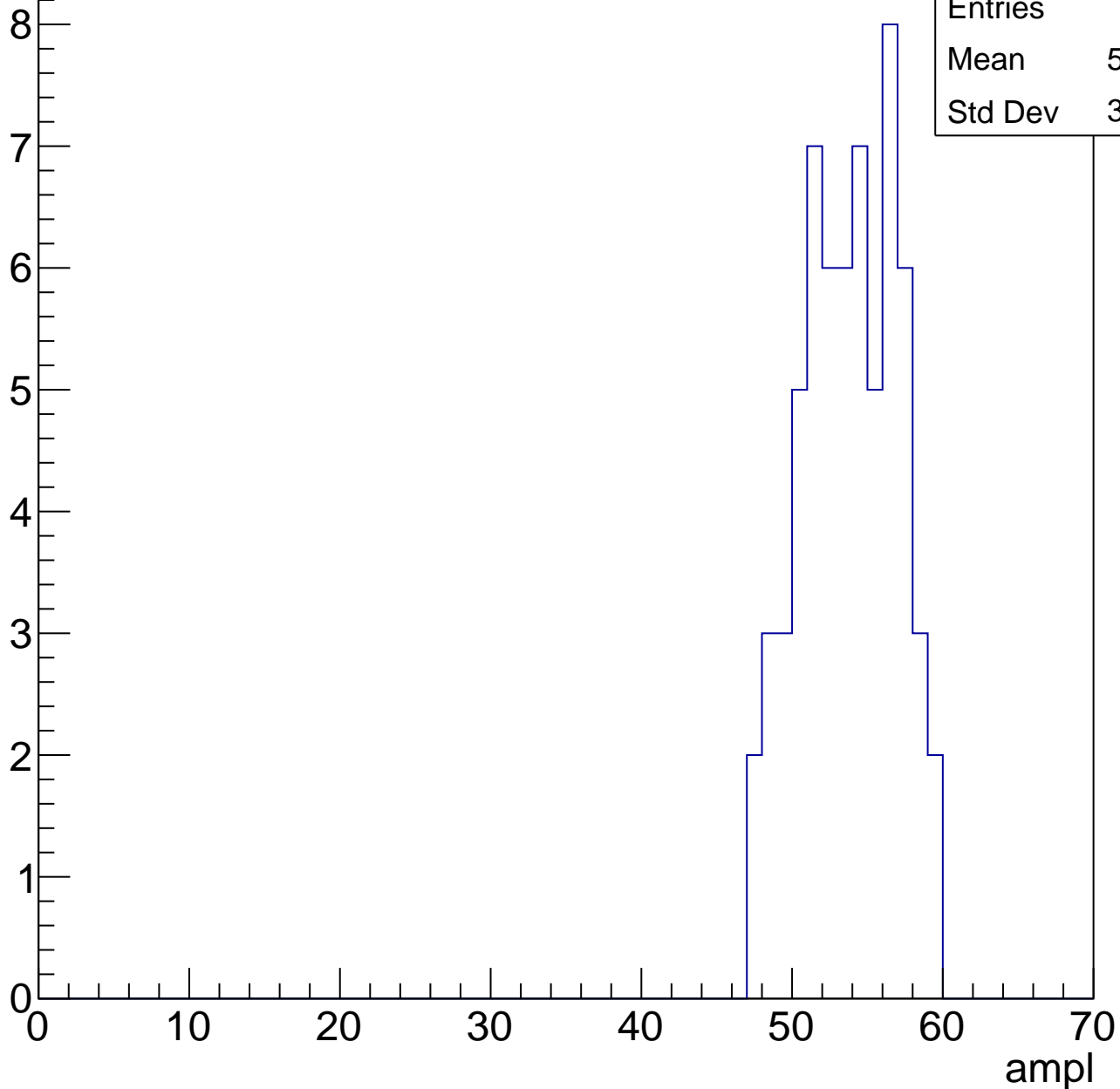
**Gaus Width: 3.2999**



# B0L000S, U7-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	63
Mean	53.29
Std Dev	3.114

# B0L000S, U7-ch43, adc4

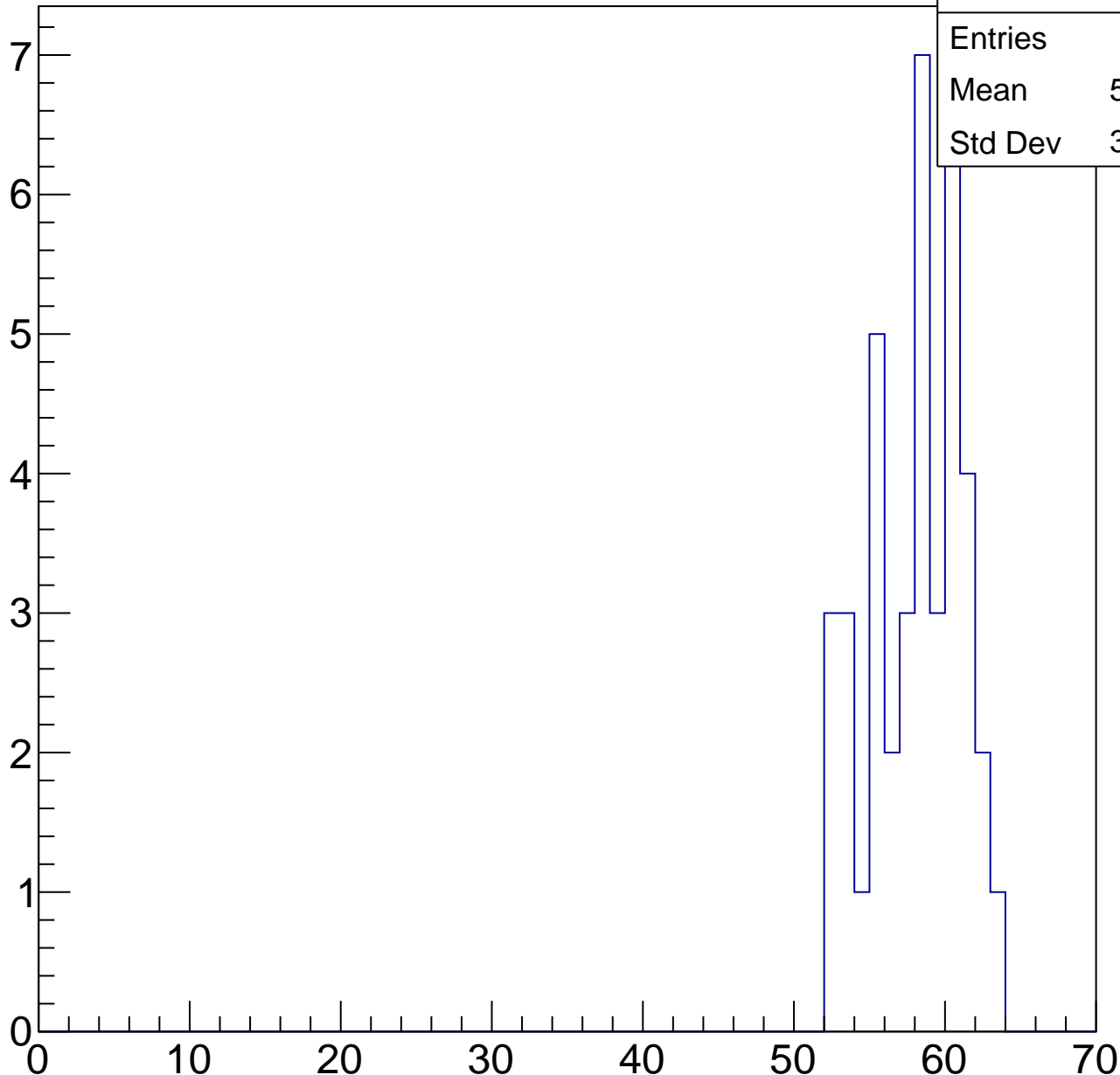
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	41
Mean	57.59
Std Dev	3.012

ampl

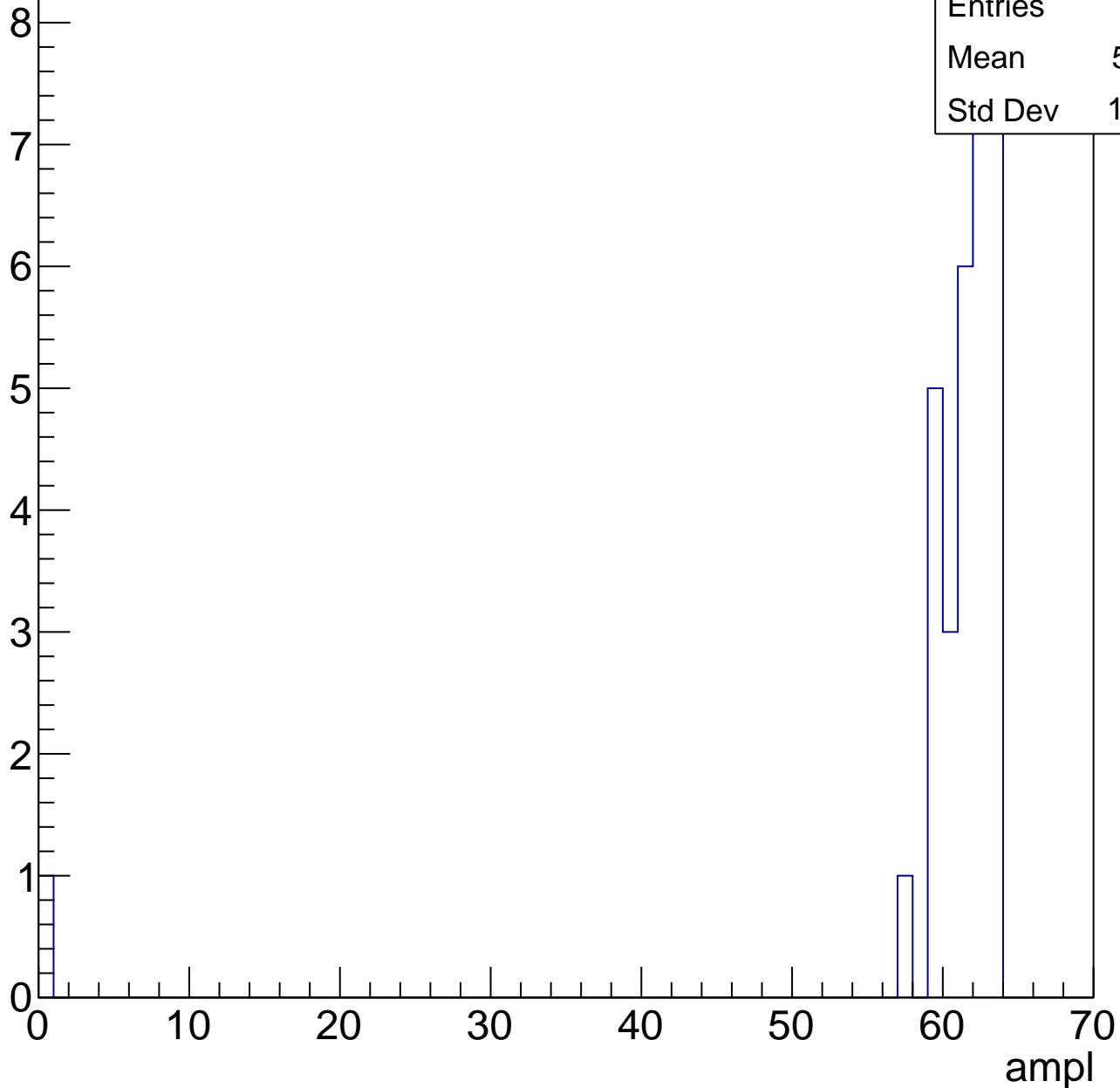


# B0L000S, U7-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	32
Mean	59.31
Std Dev	10.77



# B0L000S, U7-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	63
Std Dev	0

ampl



# B0L000S, U7-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L000S, U7-ch44, adc0

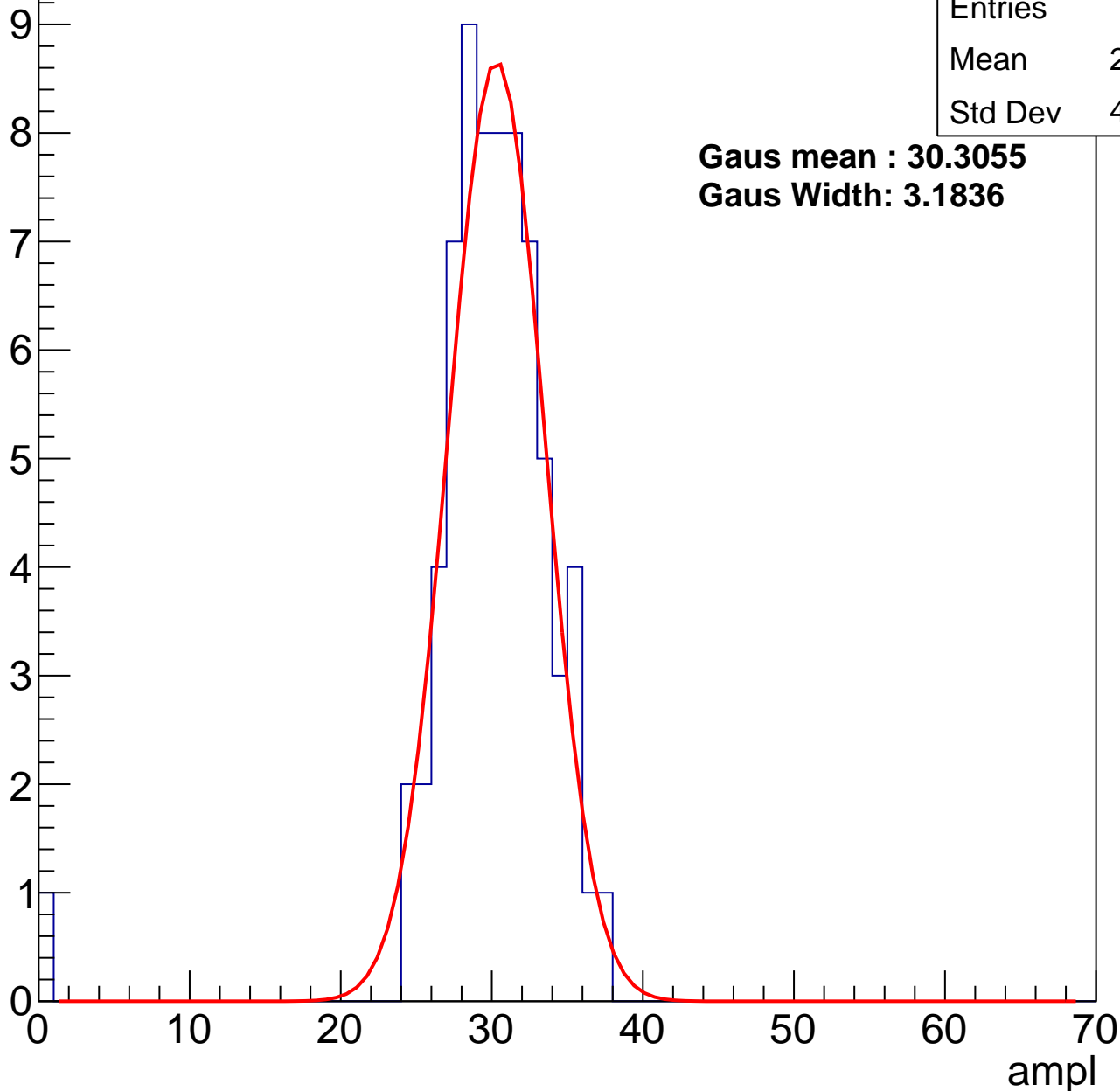
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	70
Mean	29.53
Std Dev	4.616

**Gaus mean : 30.3055**

**Gaus Width: 3.1836**



# B0L000S, U7-ch44, adc1

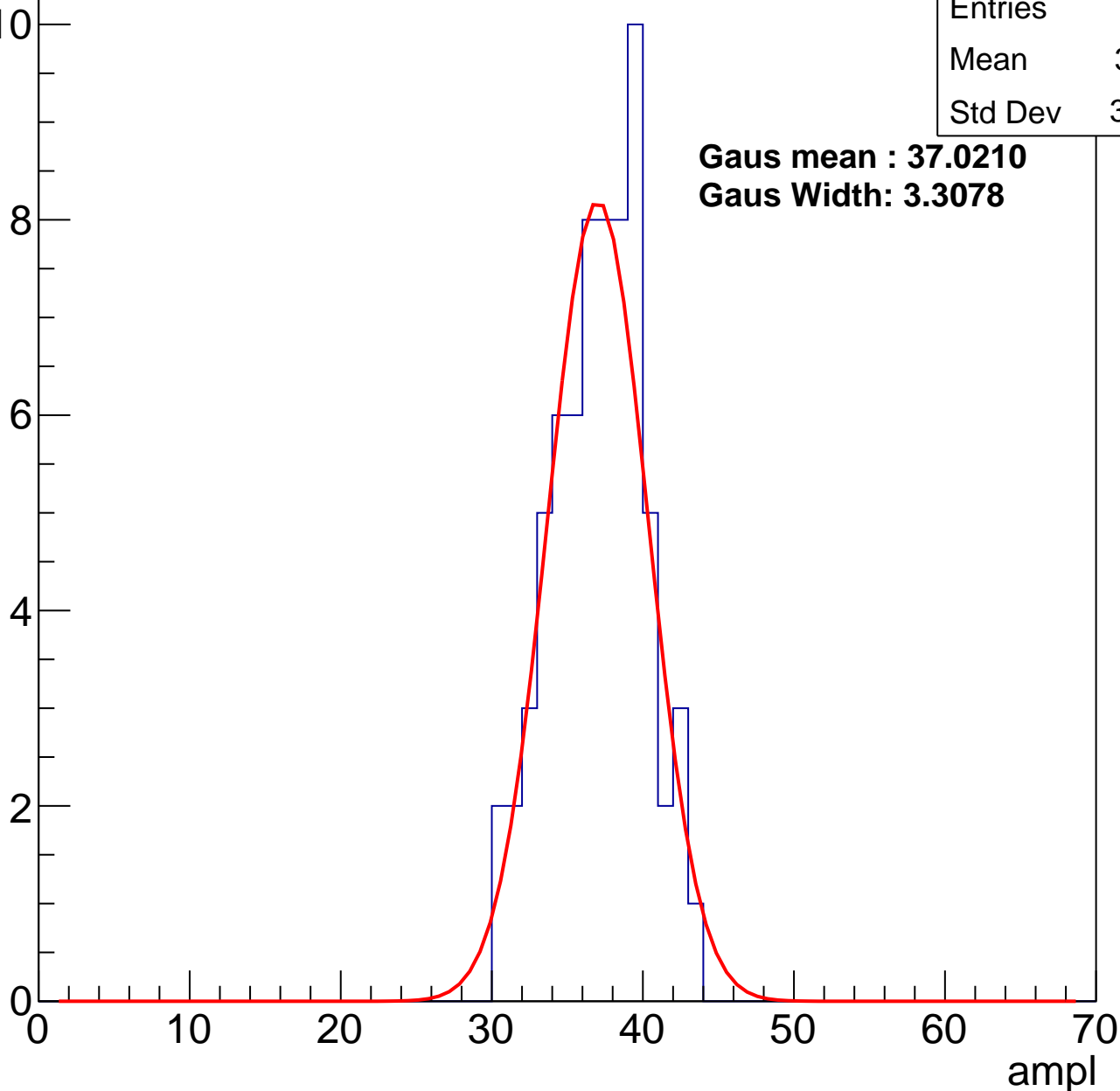
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	69
Mean	36.61
Std Dev	3.037

**Gaus mean : 37.0210**

**Gaus Width: 3.3078**



# B0L000S, U7-ch44, adc2

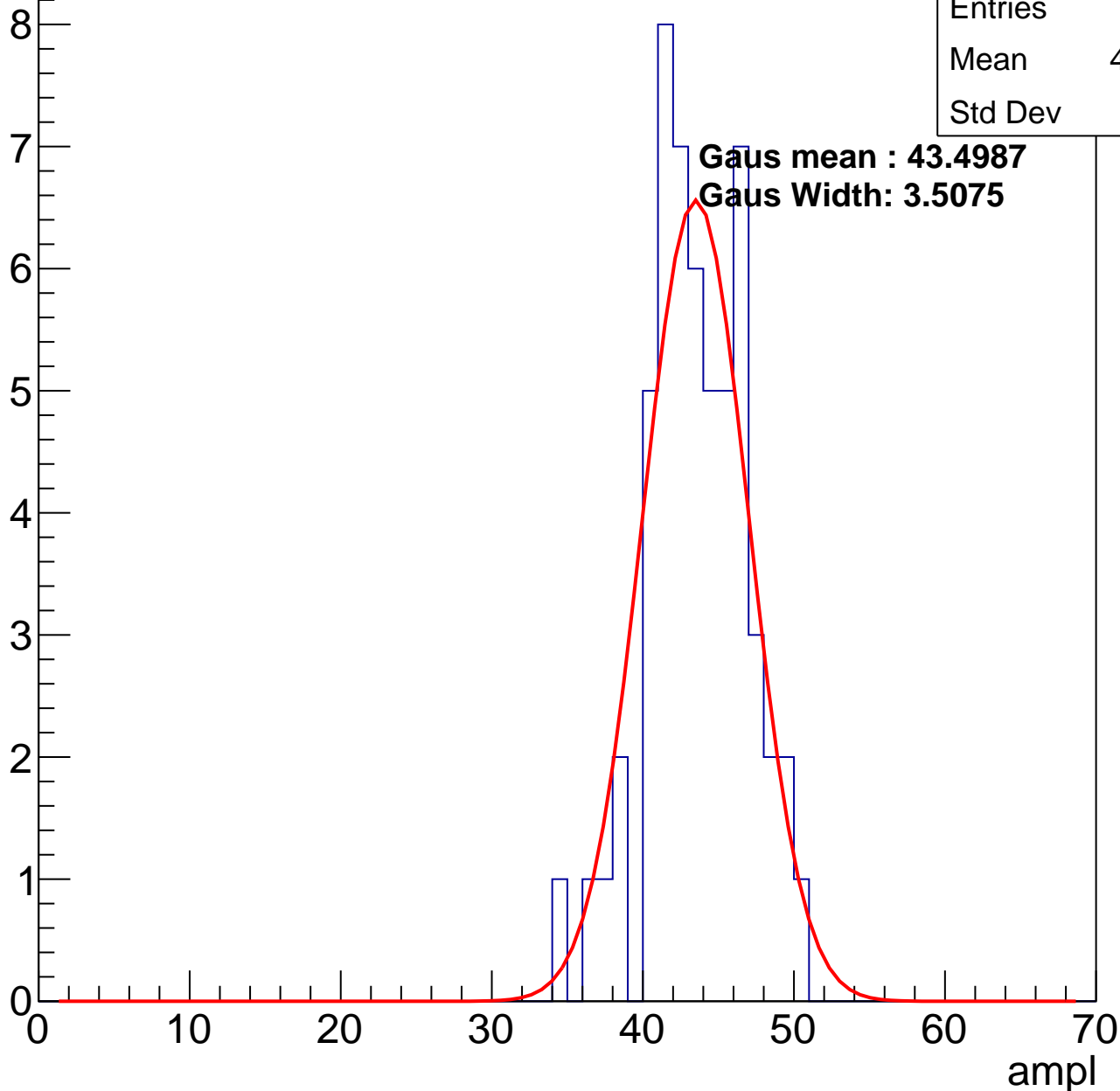
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	56
Mean	43.12
Std Dev	3.29

**Gaus mean : 43.4987**

**Gaus Width: 3.5075**

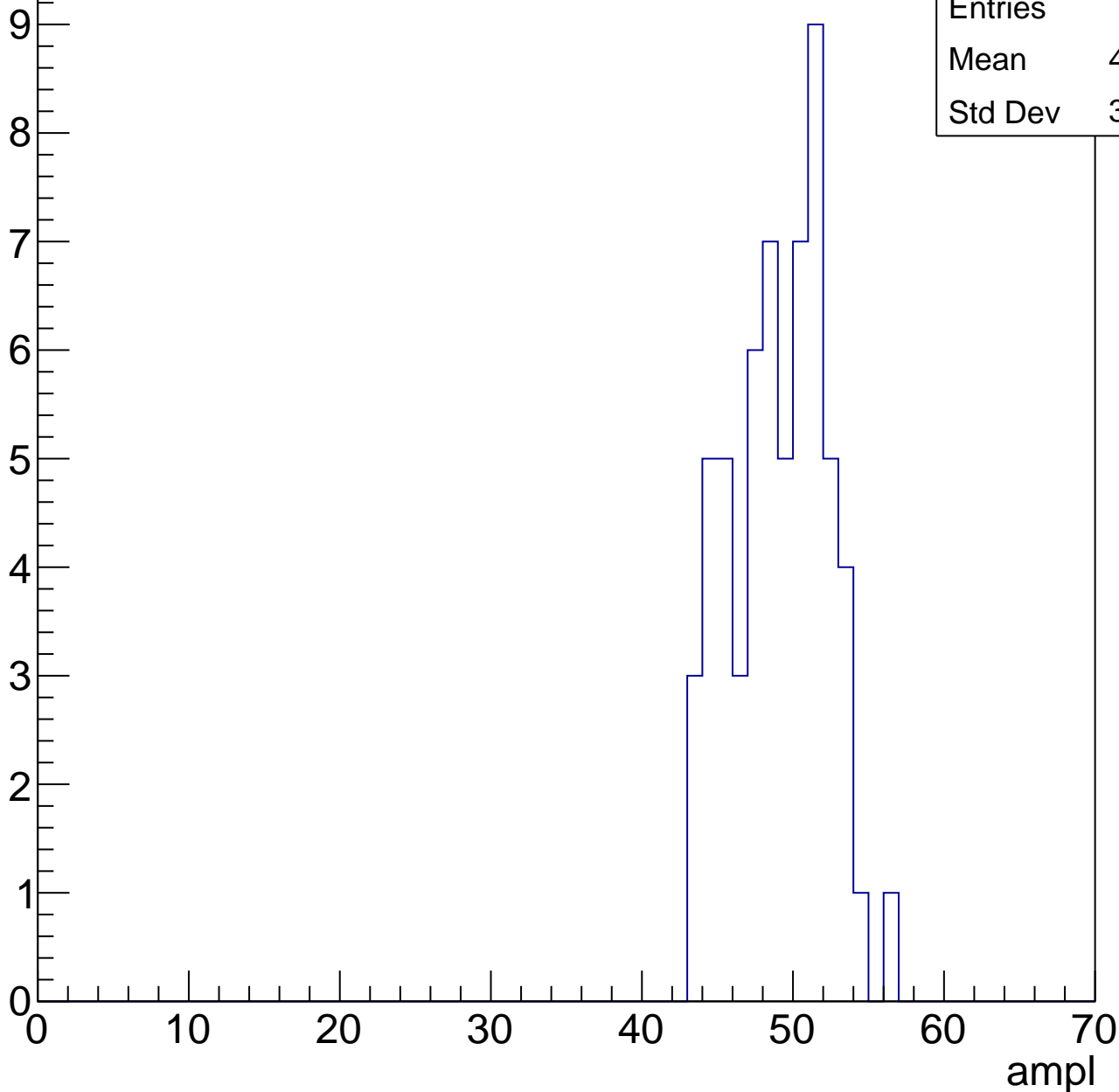


# B0L000S, U7-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

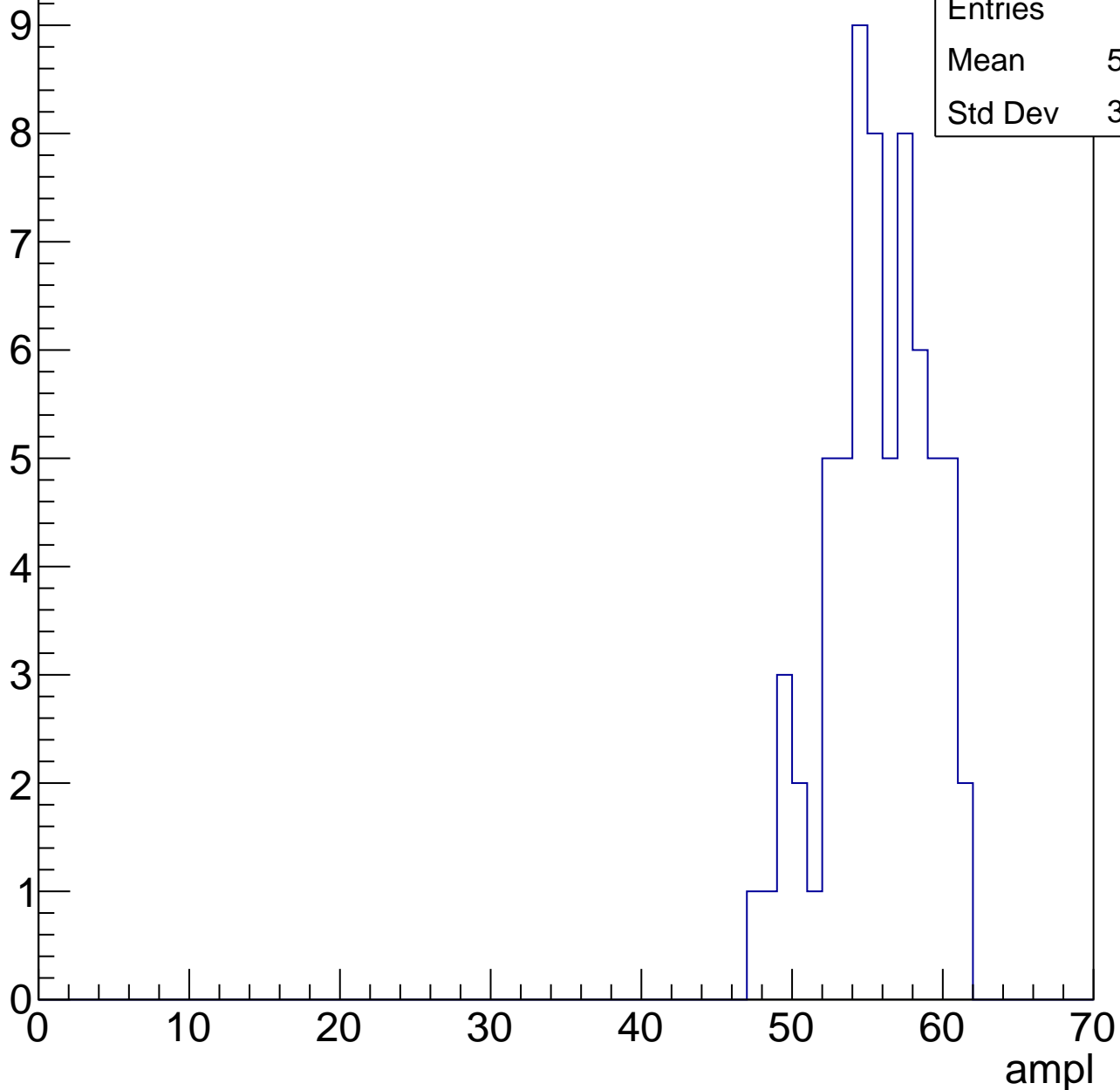
Entries	61
Mean	48.62
Std Dev	3.106



# B0L000S, U7-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



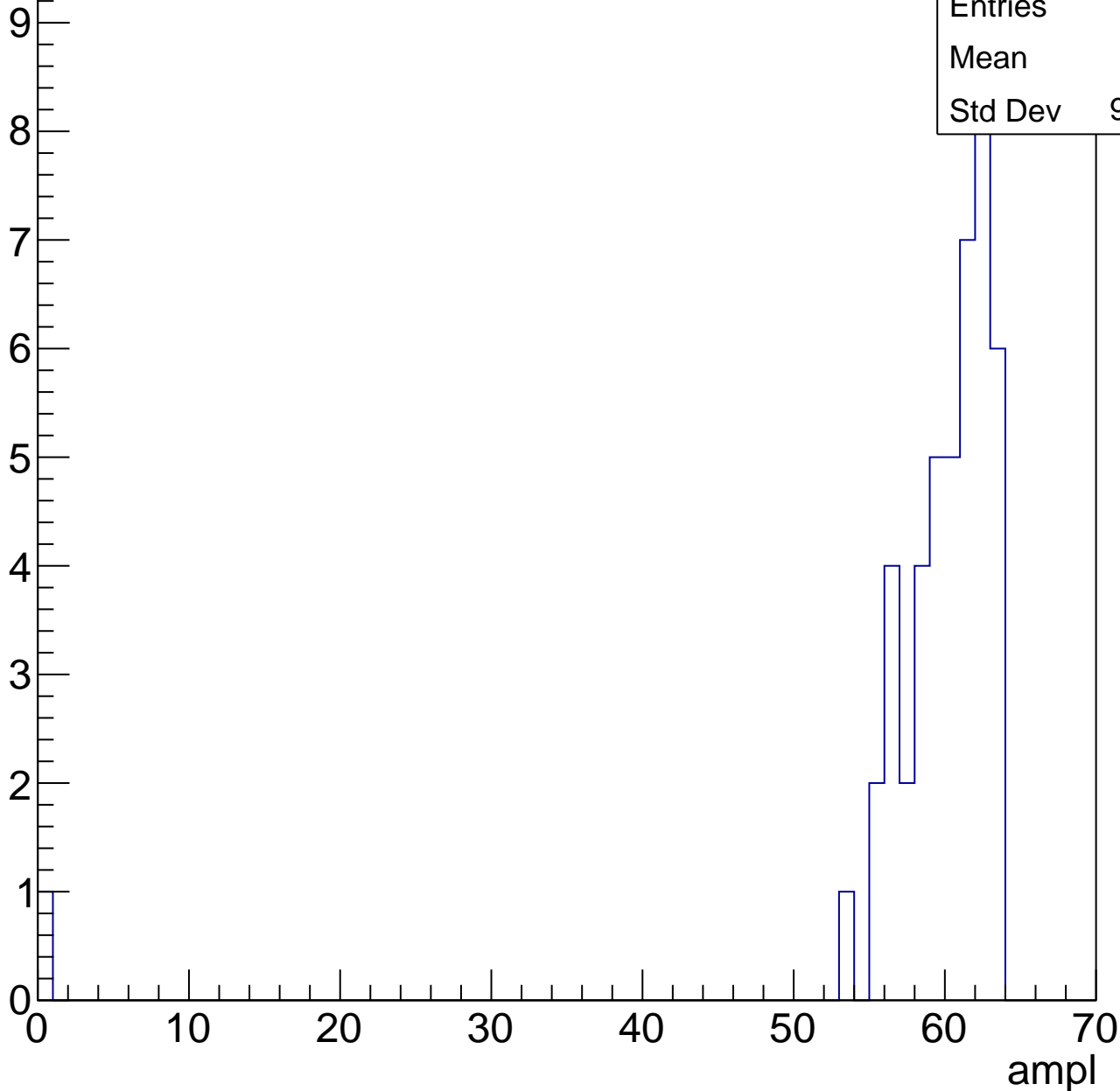
Entries	66
Mean	55.23
Std Dev	3.316

# B0L000S, U7-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

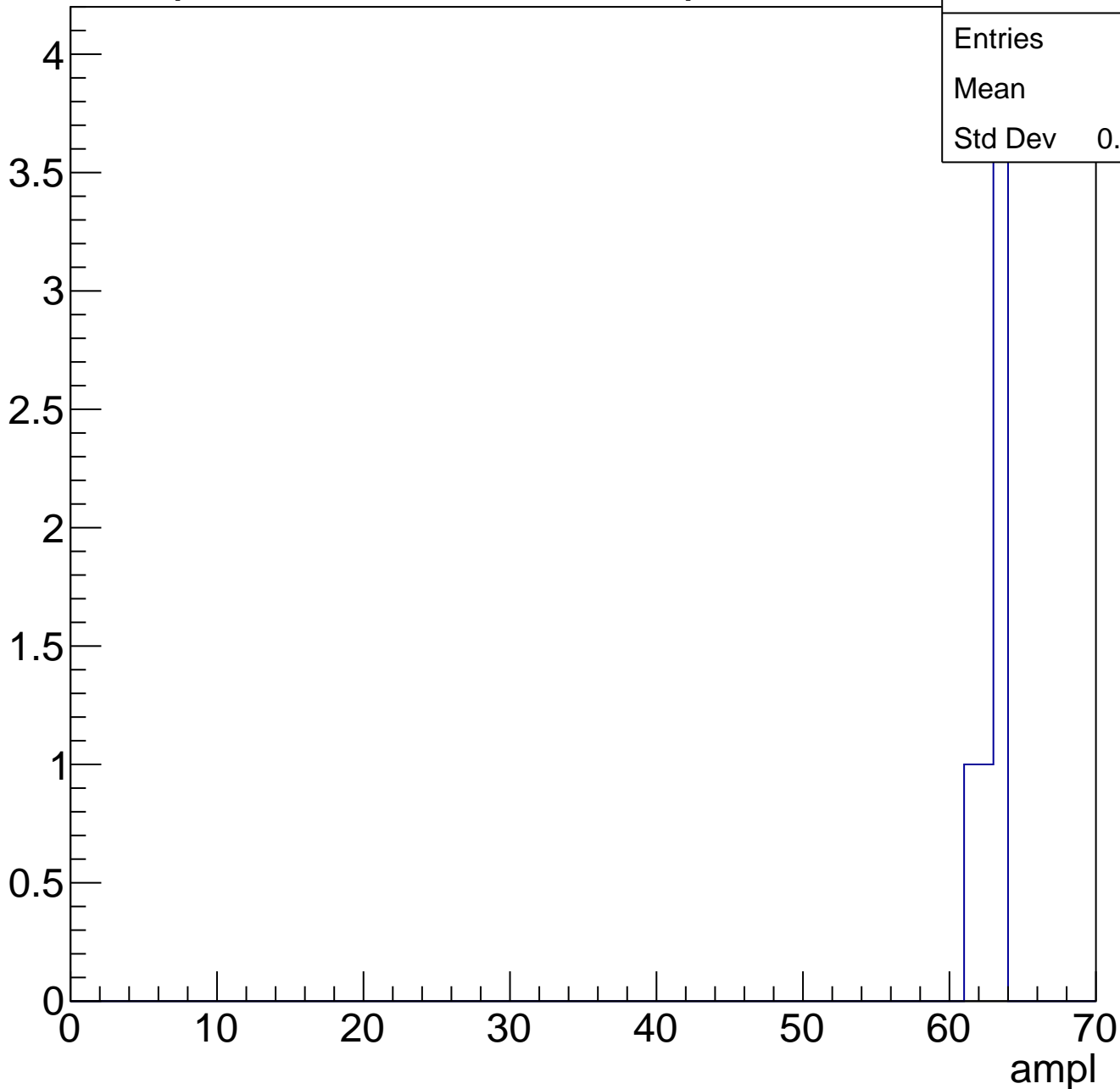
Entries	46
Mean	58.5
Std Dev	9.084



# B0L000S, U7-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	6
Mean	62.5
Std Dev	0.7638



# B0L000S, U7-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch45, adc0

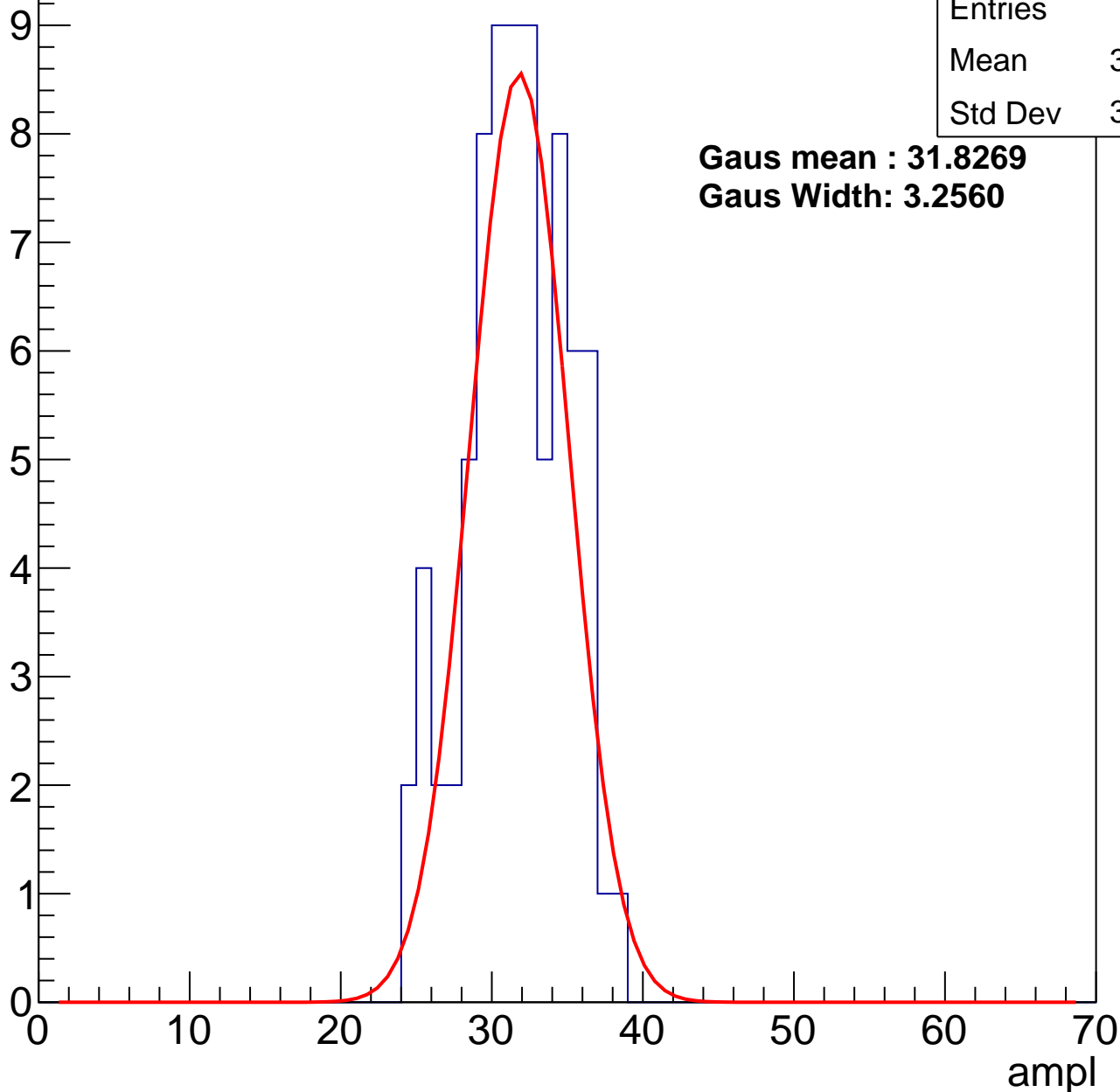
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	77
Mean	31.18
Std Dev	3.302

**Gaus mean : 31.8269**

**Gaus Width: 3.2560**



# B0L000S, U7-ch45, adc1

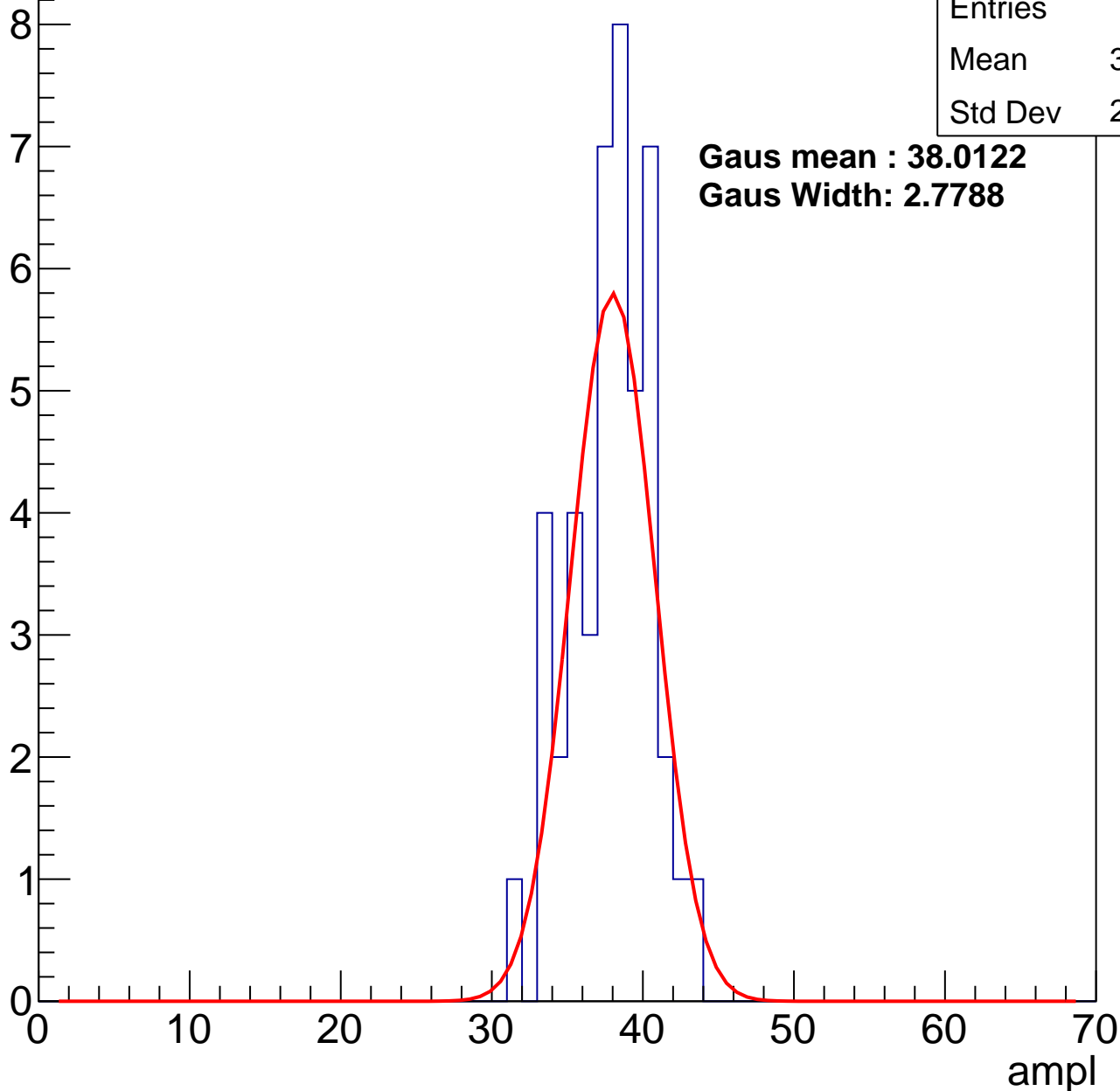
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	45
Mean	37.42
Std Dev	2.637

**Gaus mean : 38.0122**

**Gaus Width: 2.7788**



# B0L000S, U7-ch45, adc2

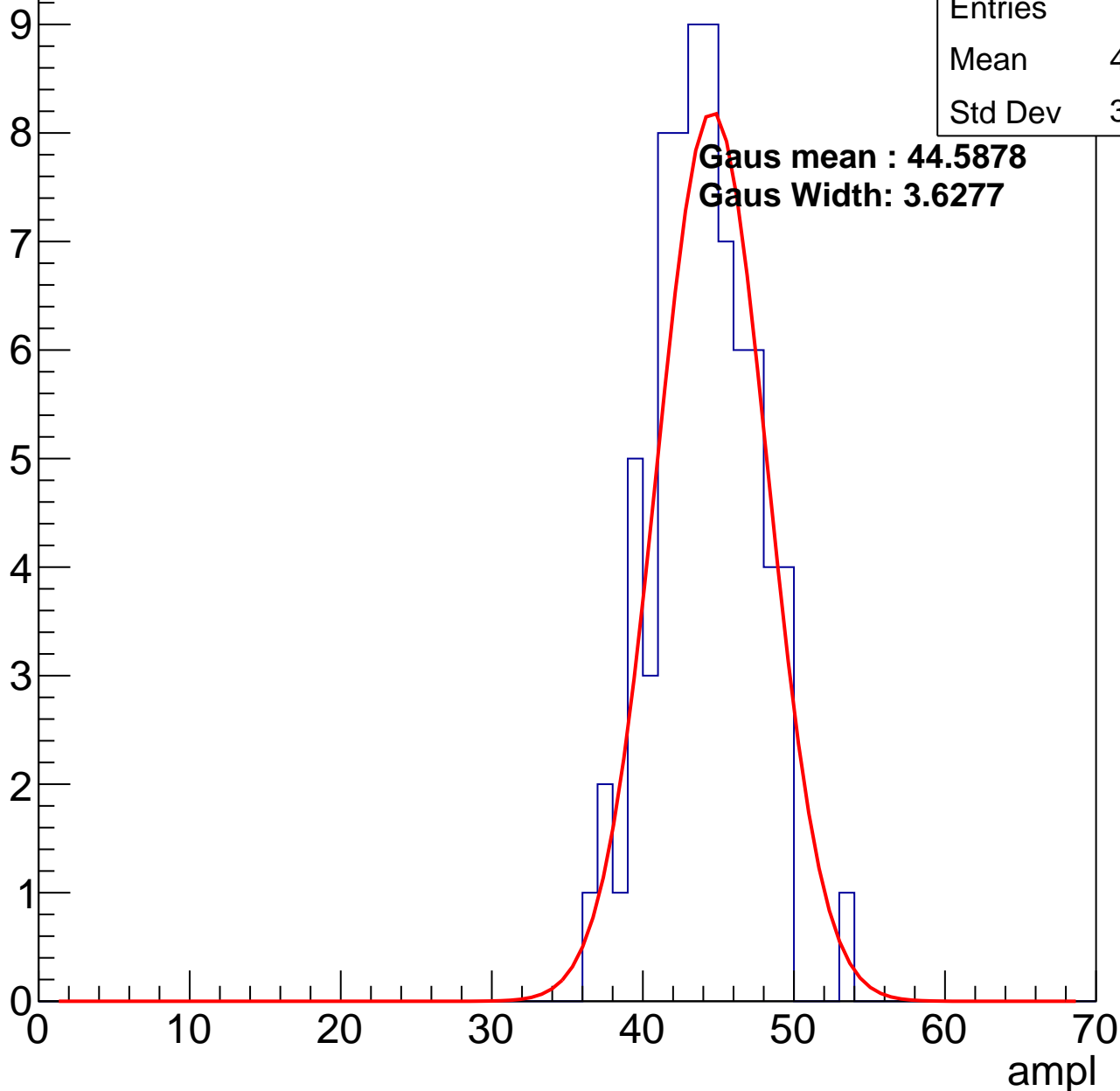
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	74
Mean	43.57
Std Dev	3.288

**Gaus mean : 44.5878**

**Gaus Width: 3.6277**

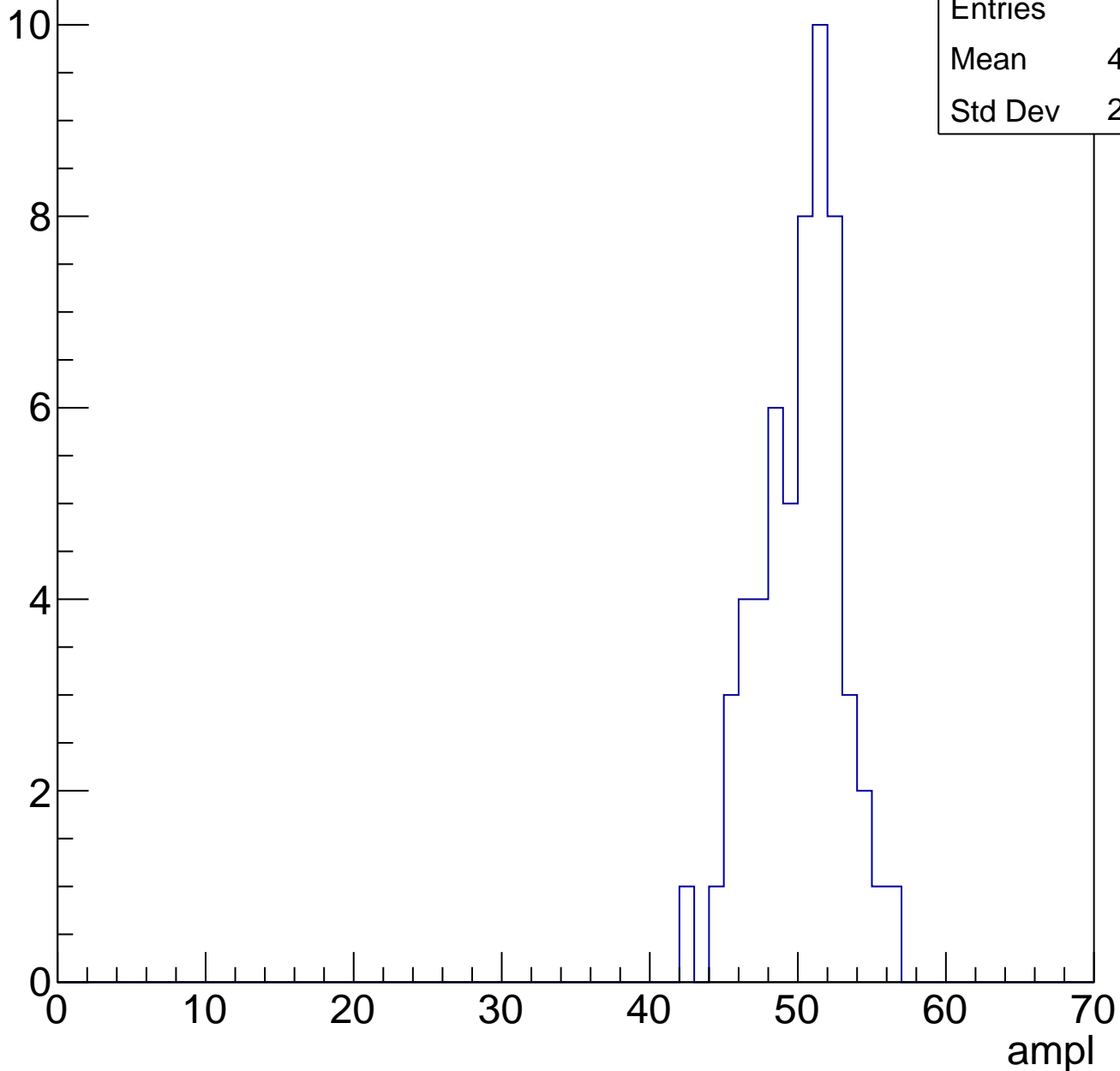


# B0L000S, U7-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	57
Mean	49.65
Std Dev	2.838

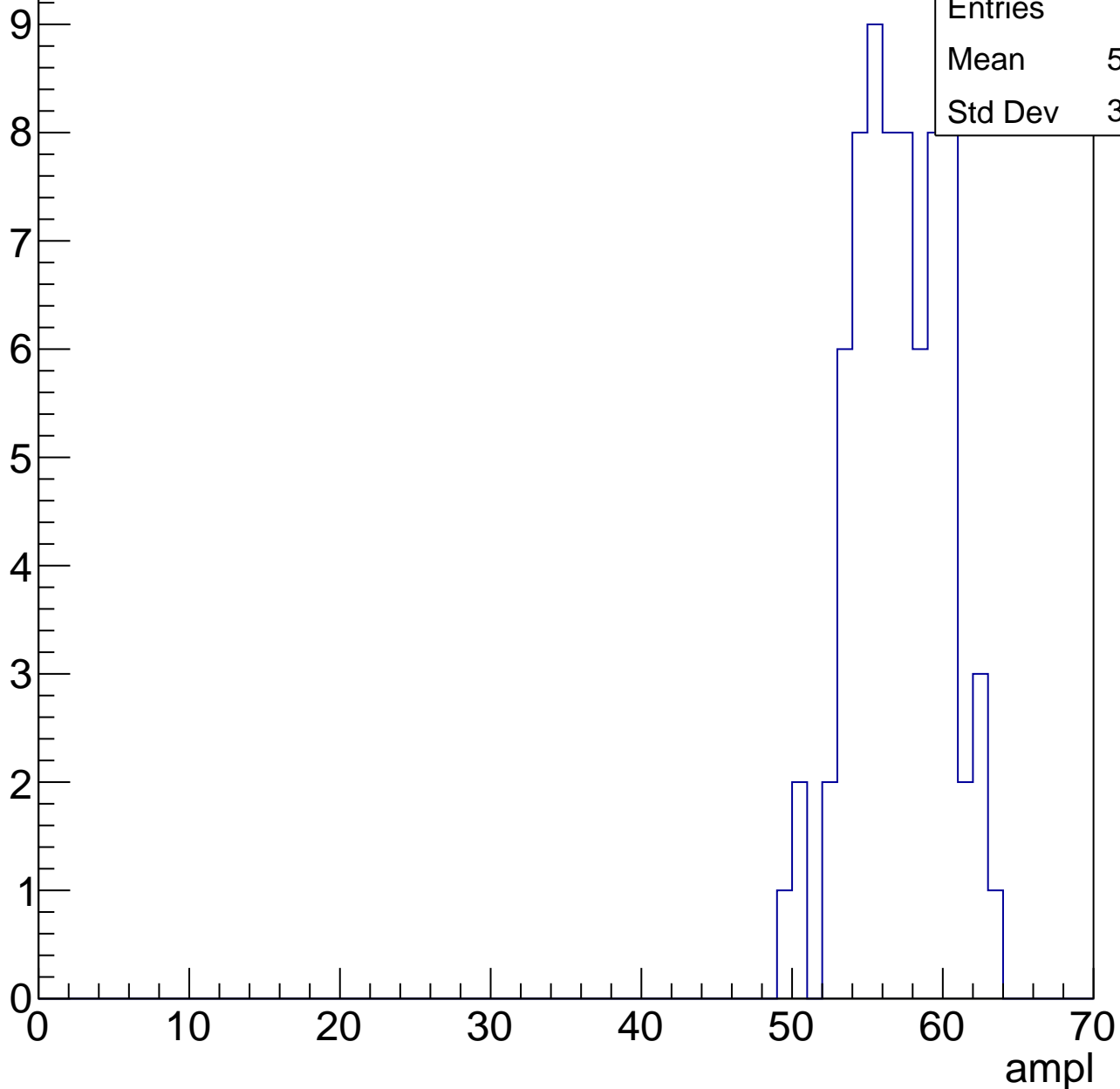
Entry



# B0L000S, U7-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

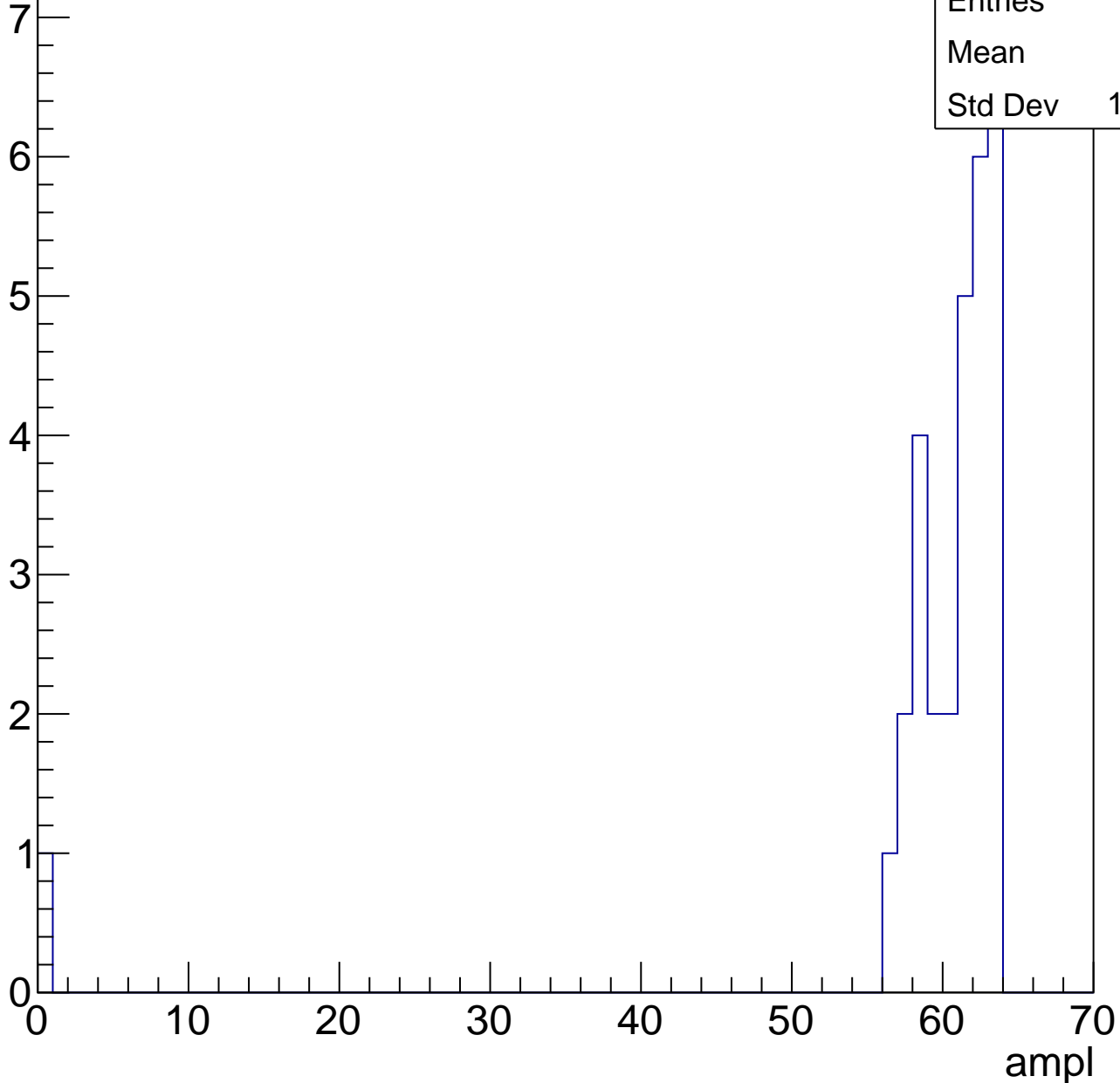


# B0L000S, U7-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	30
Mean	58.6
Std Dev	11.08



# B0L000S, U7-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

6

Mean

61.83

Std Dev

0.8975

Entries	6
Mean	61.83
Std Dev	0.8975



# B0L000S, U7-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	1
Mean	23
Std Dev	0

# B0L000S, U7-ch46, adc0

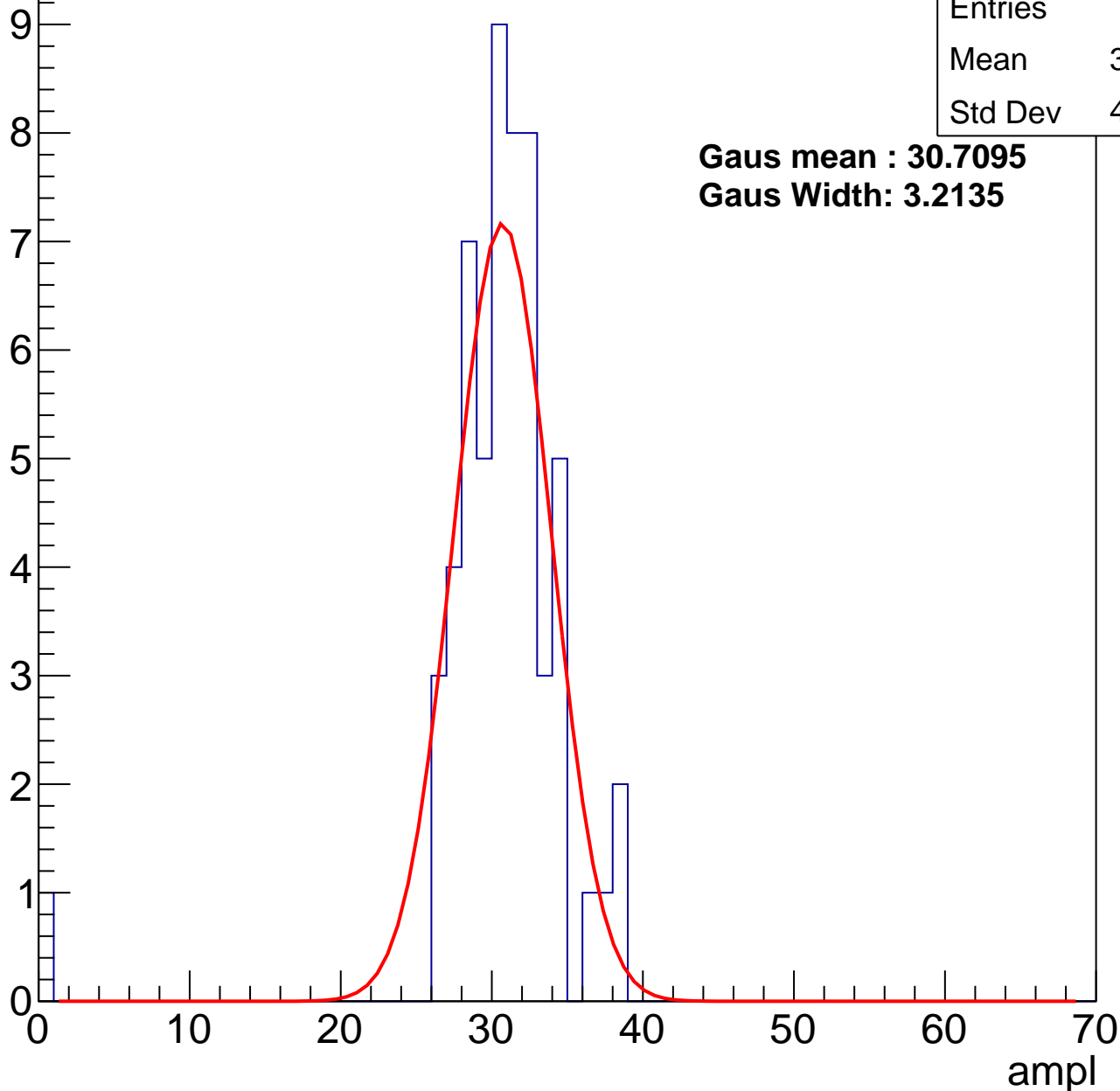
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	57
Mean	30.16
Std Dev	4.913

**Gaus mean : 30.7095**

**Gaus Width: 3.2135**



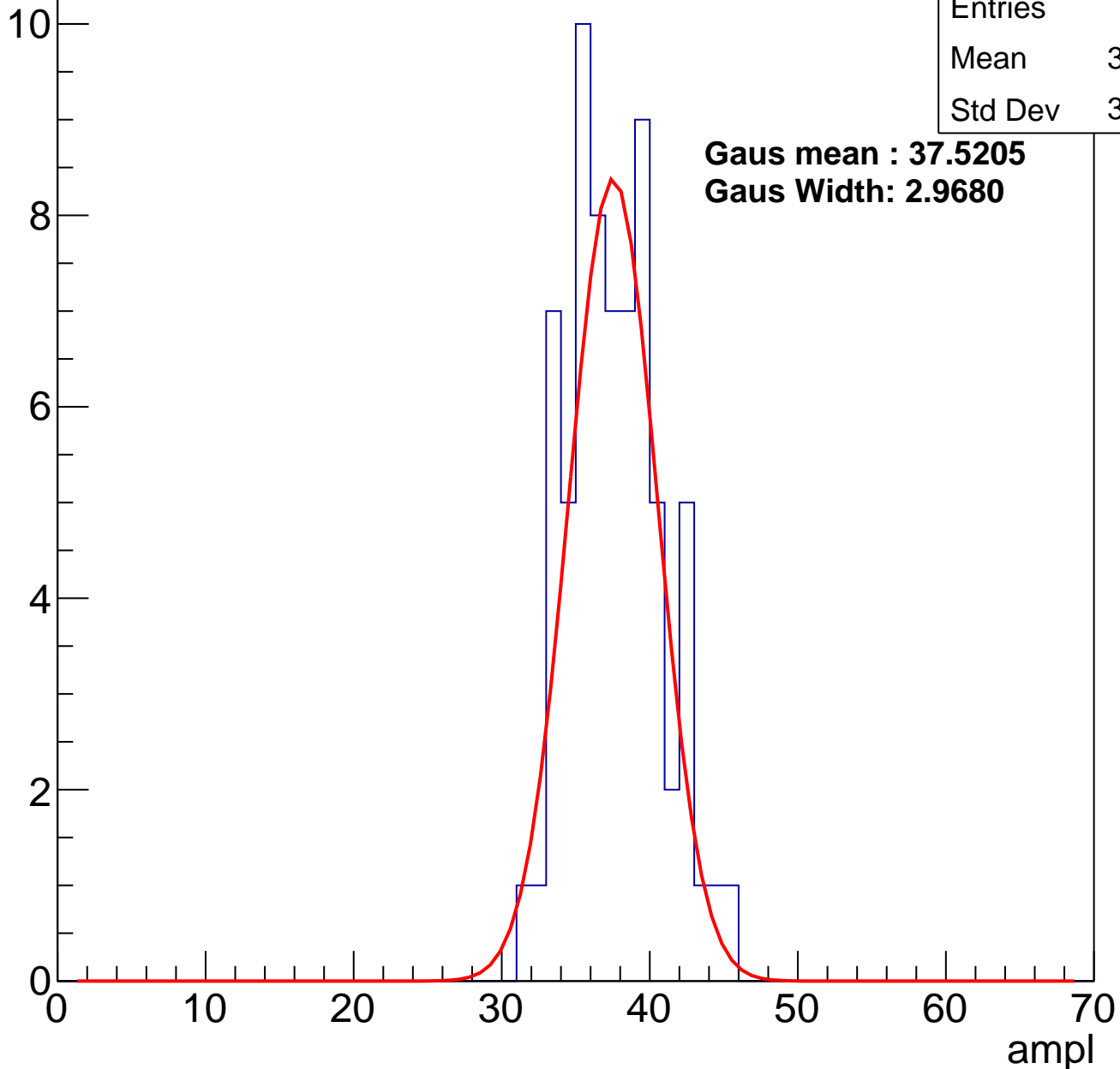
# B0L000S, U7-ch46, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	70
Mean	37.17
Std Dev	3.066

**Gaus mean : 37.5205**  
**Gaus Width: 2.9680**

Entry



# B0L000S, U7-ch46, adc2

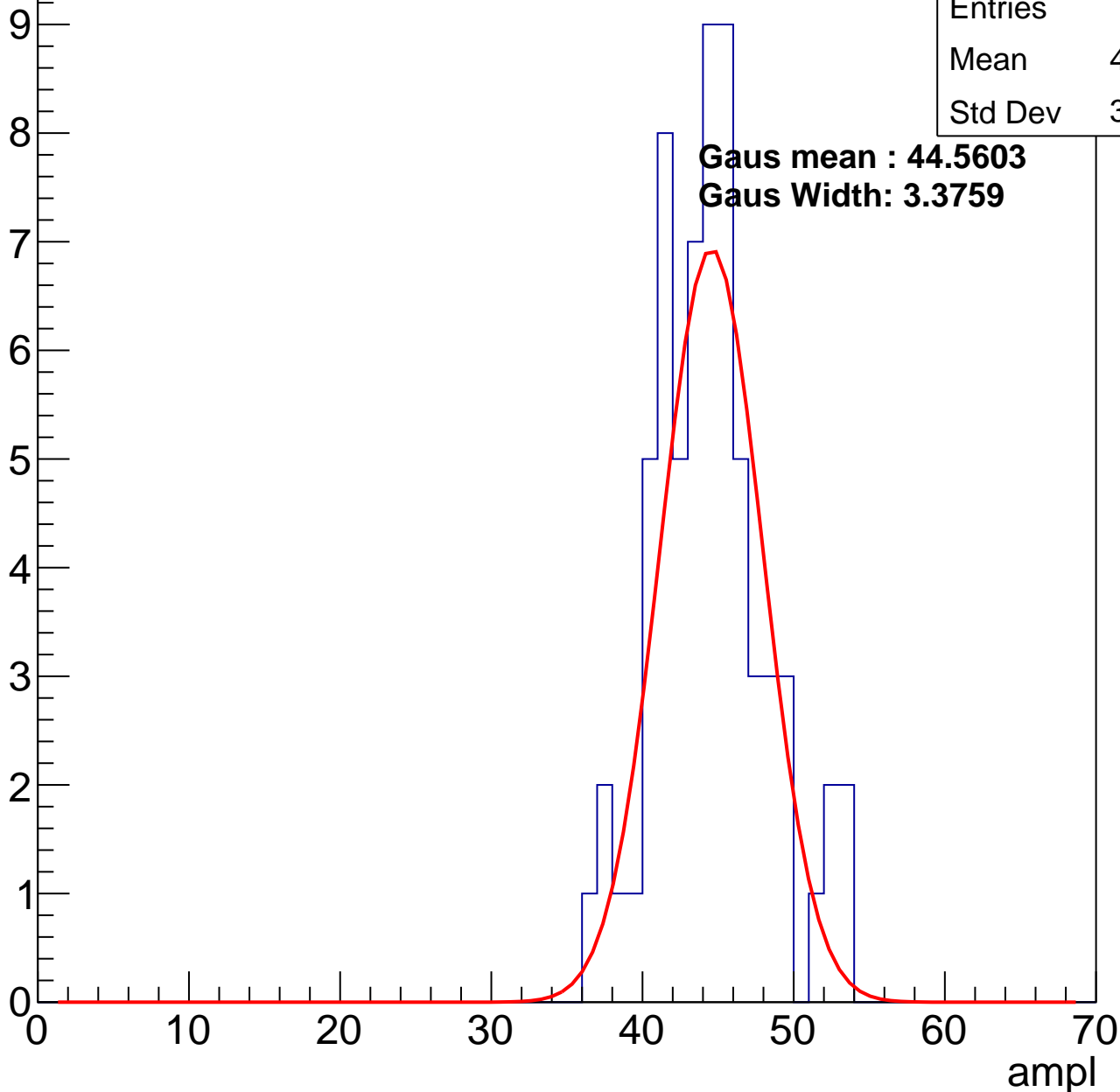
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	67
Mean	44.03
Std Dev	3.705

**Gaus mean : 44.5603**

**Gaus Width: 3.3759**

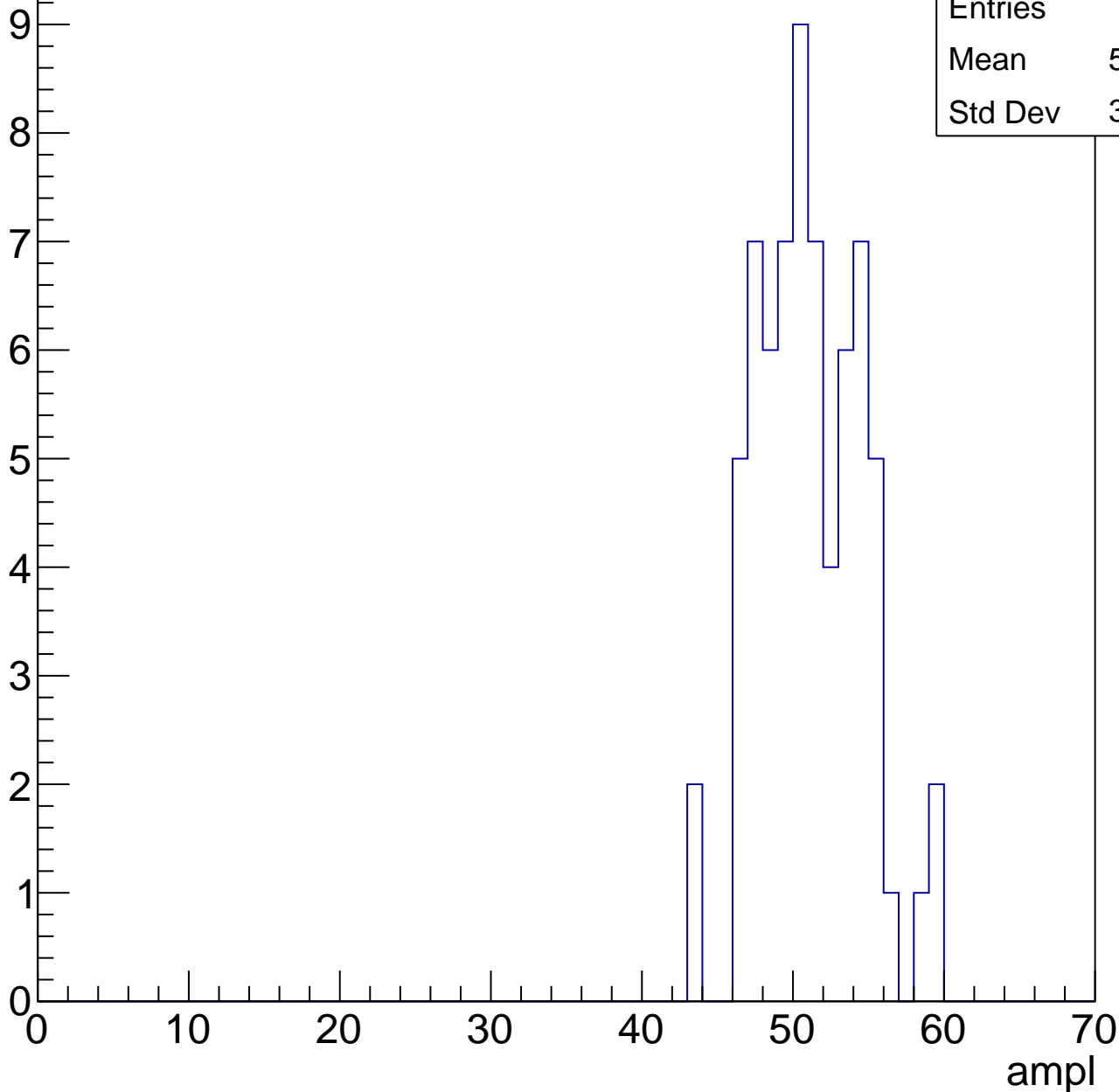


# B0L000S, U7-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	69
Mean	50.64
Std Dev	3.447

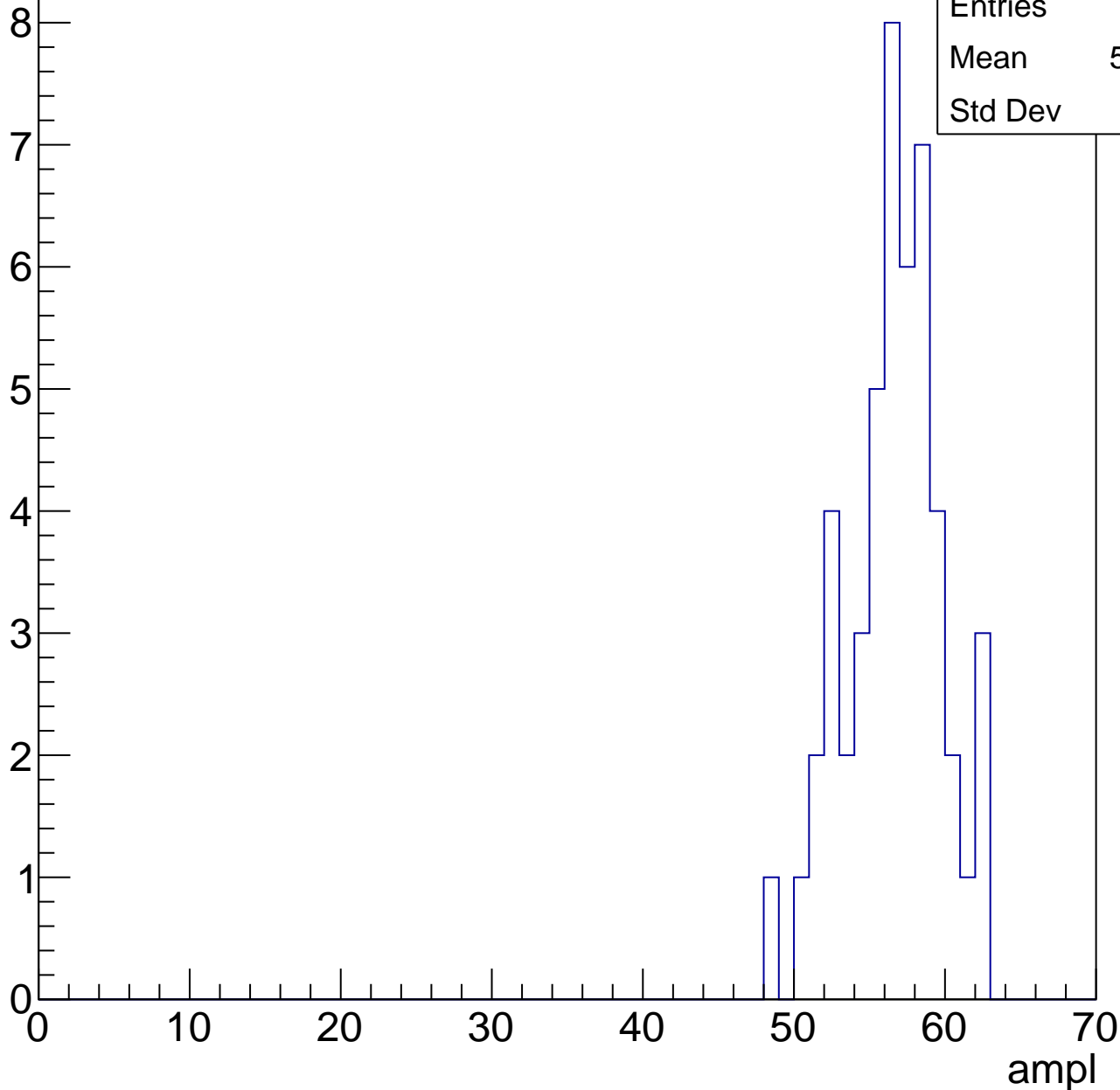


# B0L000S, U7-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	49
Mean	56.12
Std Dev	3.14



# B0L000S, U7-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

10

8

6

4

2

0

0

10

20

30

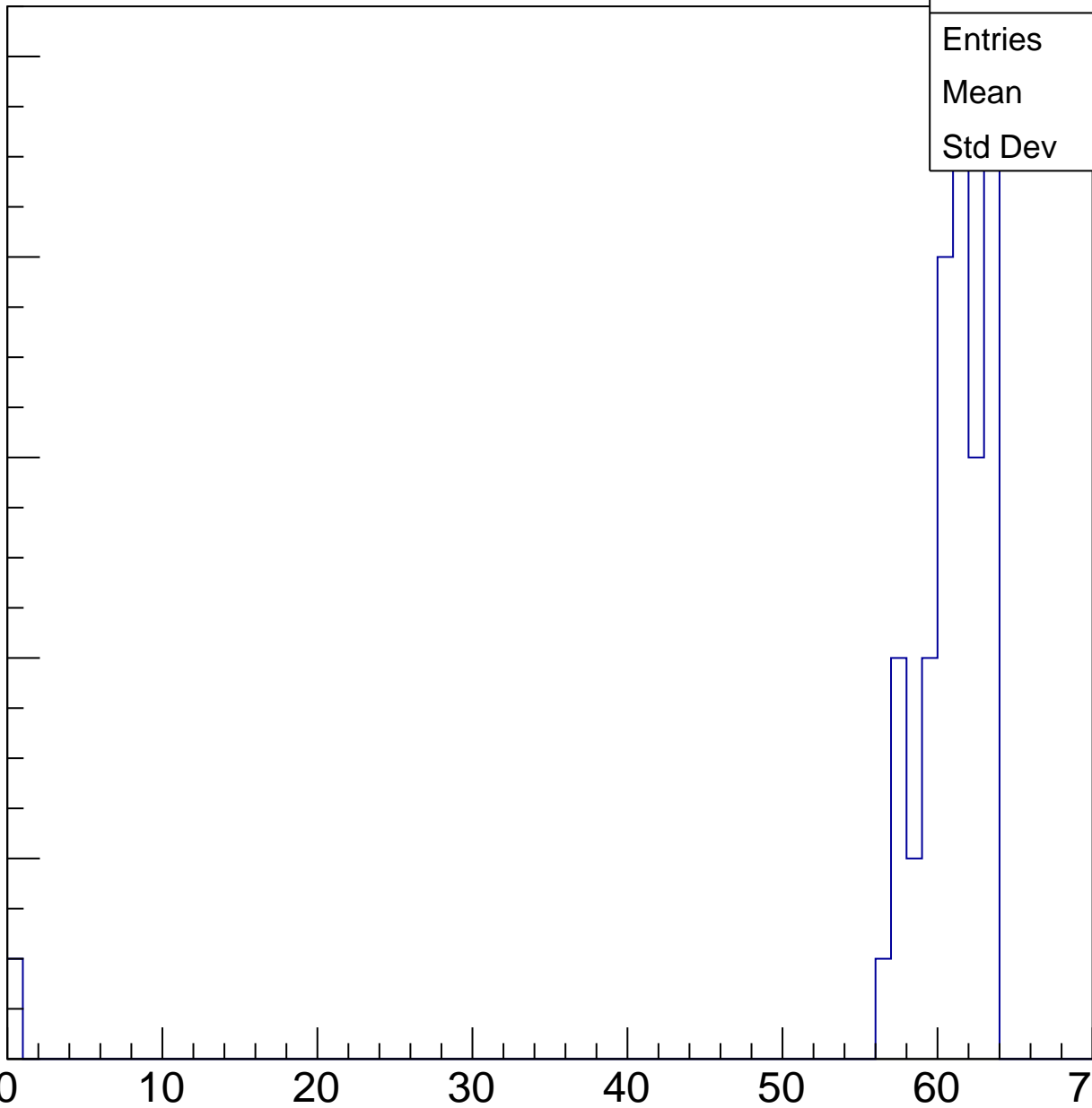
40

50

60

ampl

Entries	45
Mean	59.27
Std Dev	9.144



# B0L000S, U7-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch47, adc0

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	76
Mean	30.79
Std Dev	3.423

**Gaus mean : 30.9669**

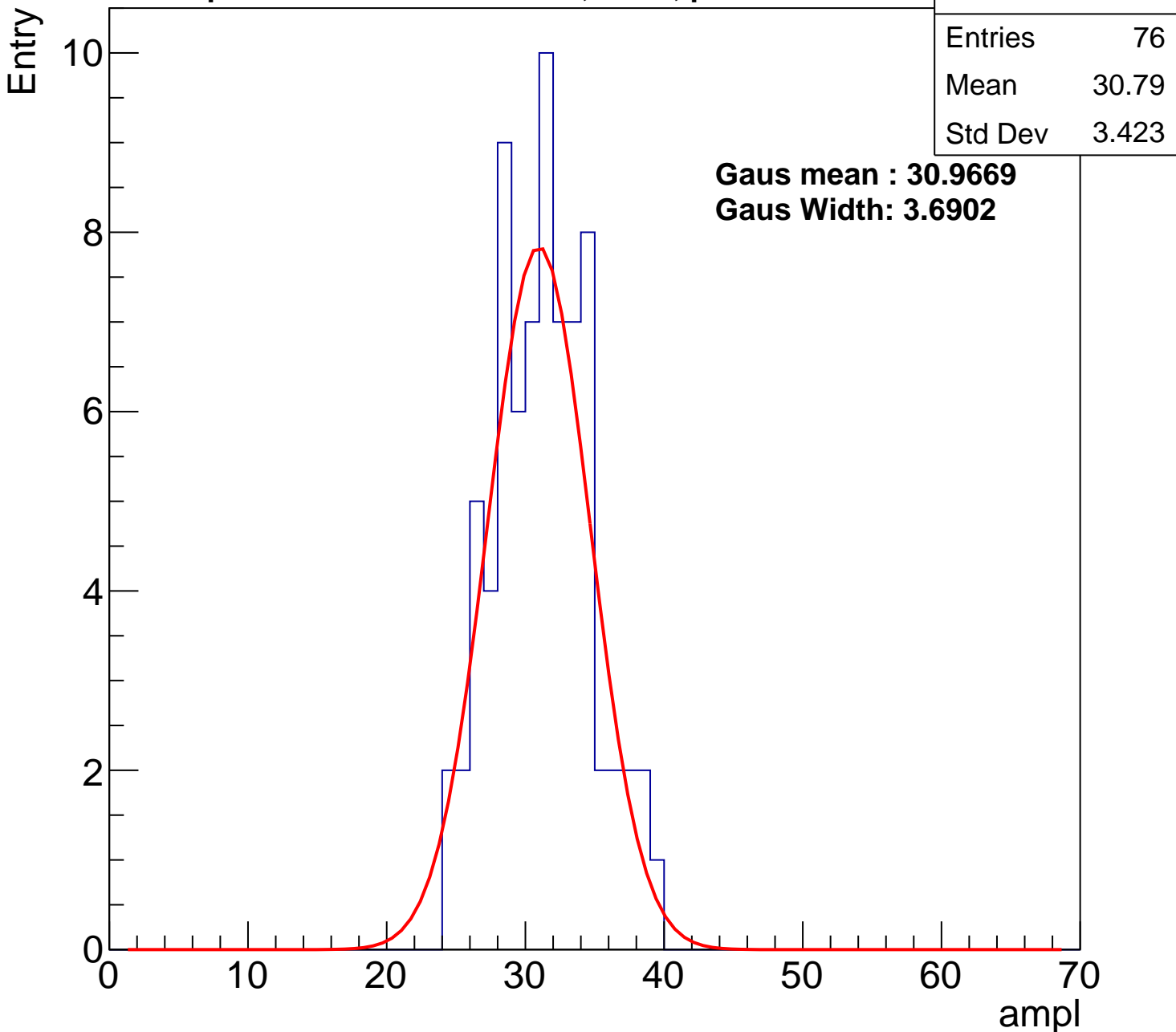
**Gaus Width: 3.6902**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L000S, U7-ch47, adc1

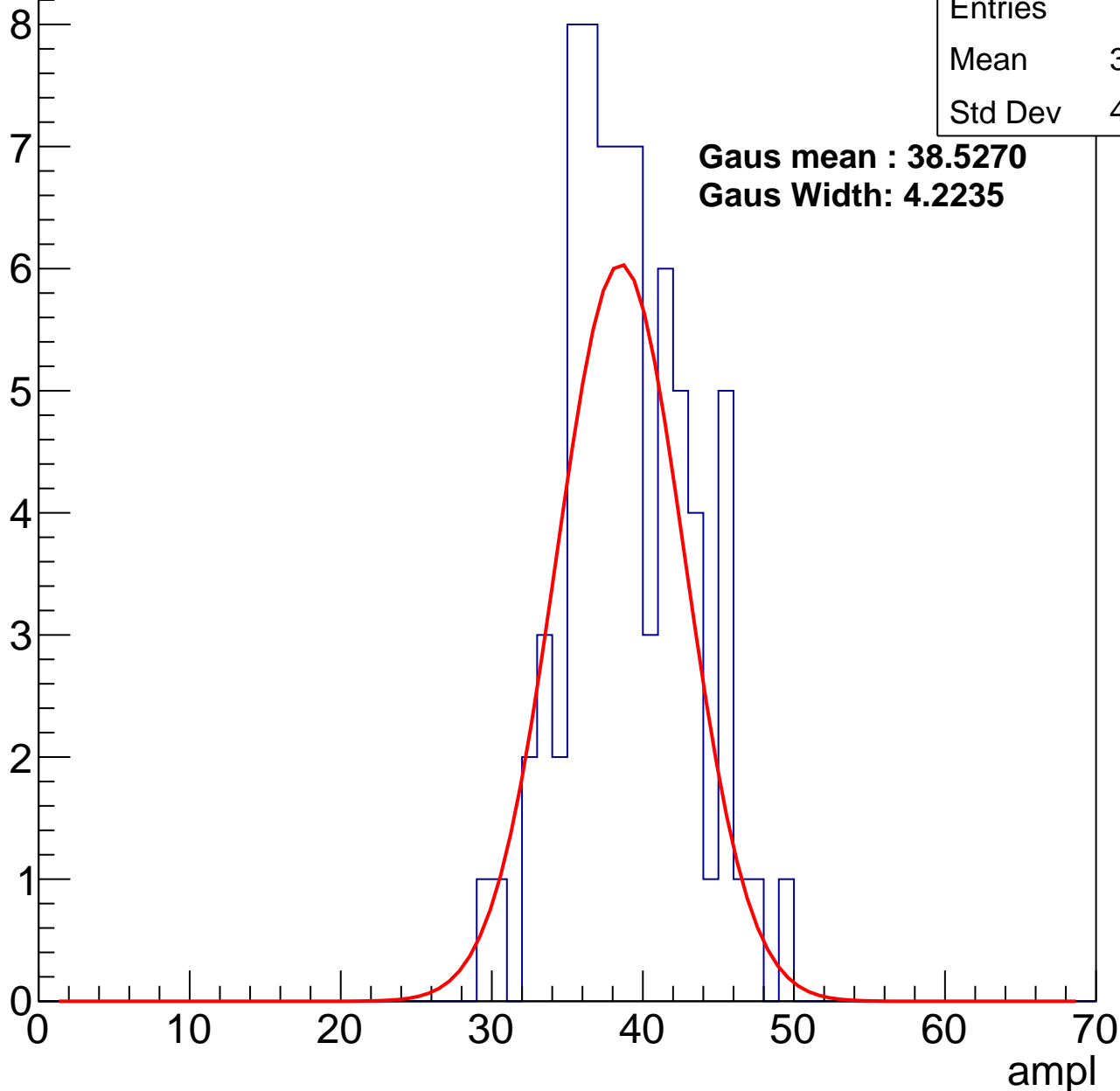
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	73
Mean	38.56
Std Dev	4.075

**Gaus mean : 38.5270**

**Gaus Width: 4.2235**



# B0L000S, U7-ch47, adc2

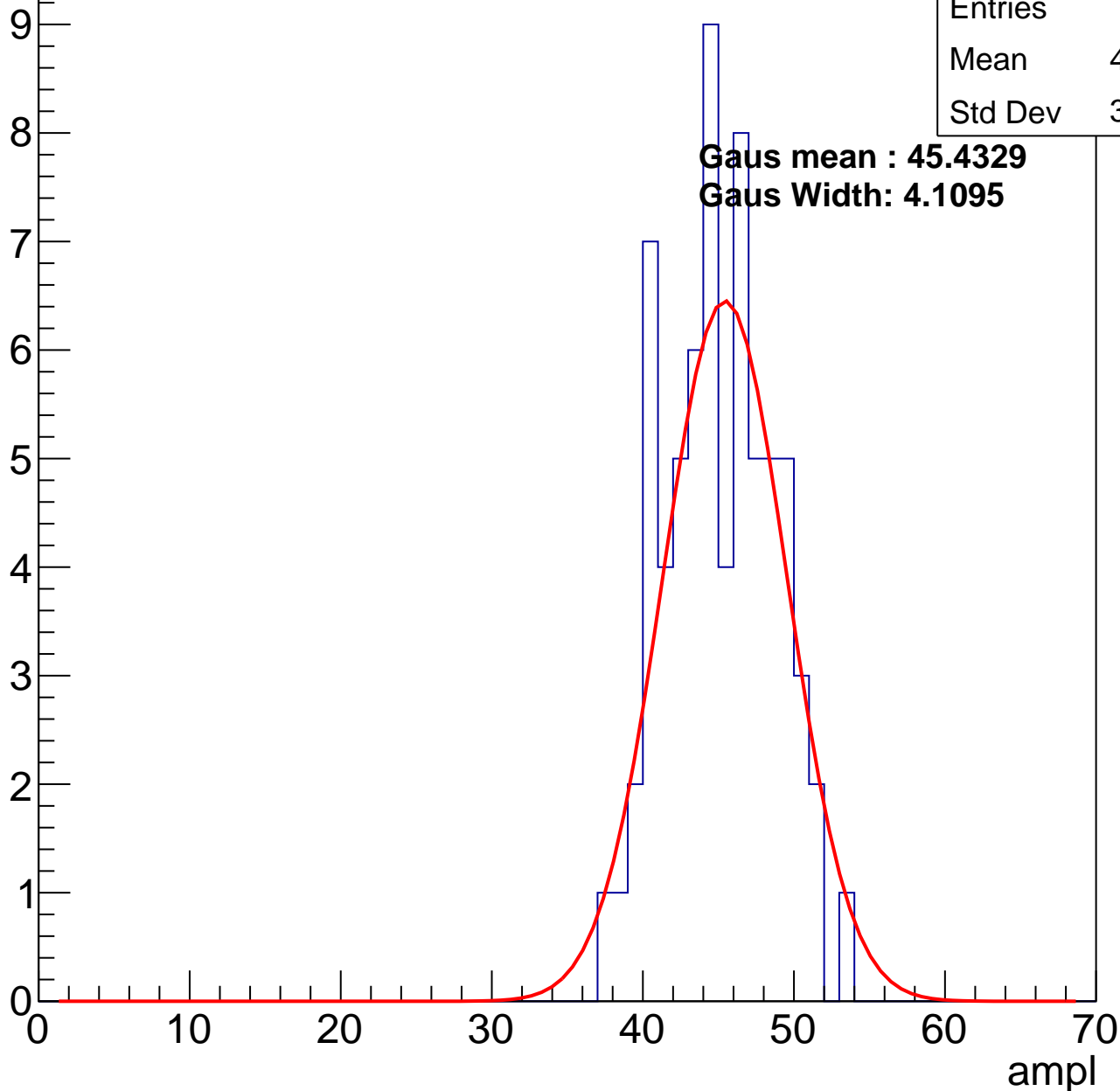
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	68
Mean	44.62
Std Dev	3.548

**Gaus mean : 45.4329**

**Gaus Width: 4.1095**

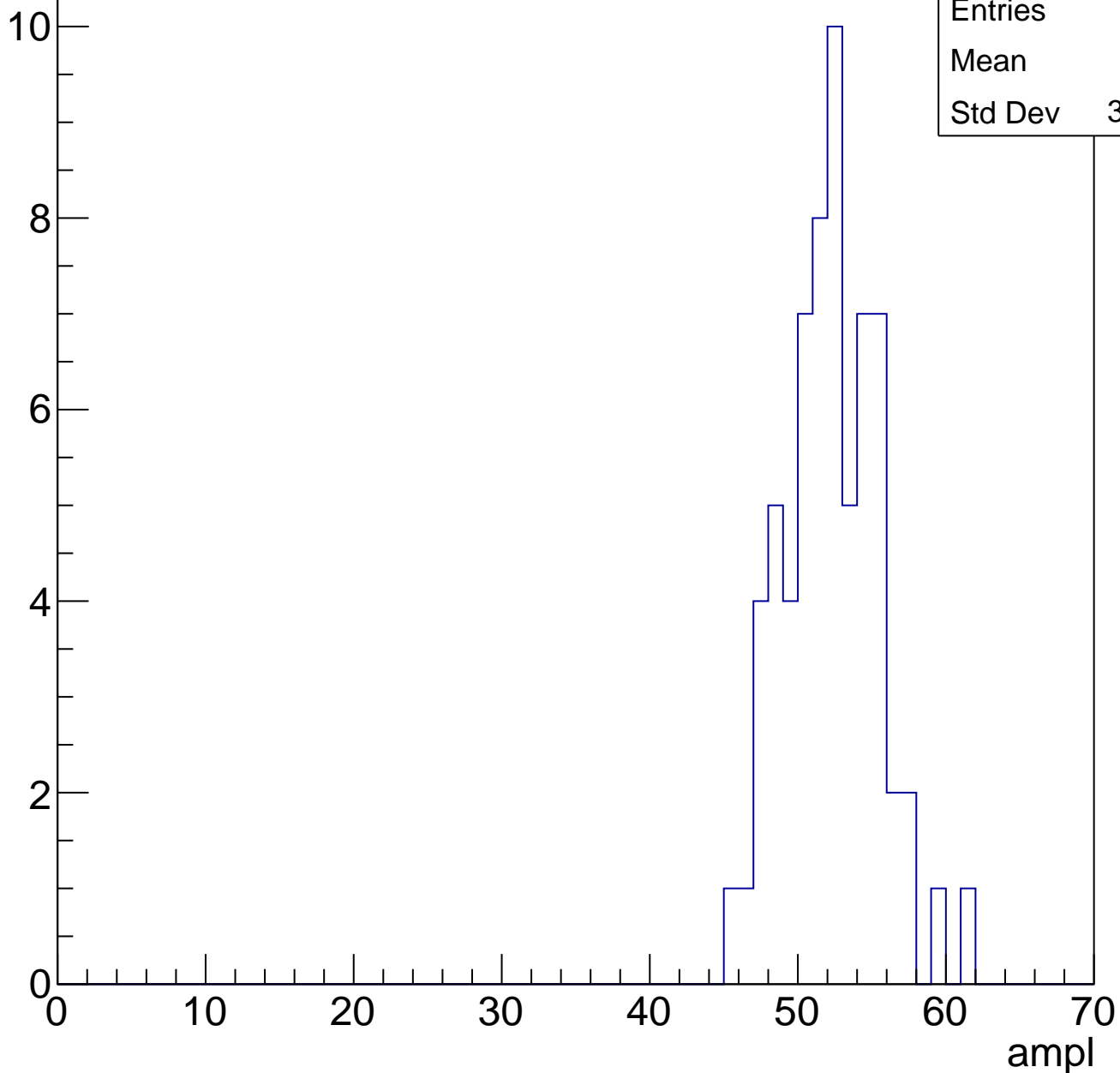


# B0L000S, U7-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	65
Mean	51.8
Std Dev	3.144



# B0L000S, U7-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

10

Entries 65

Mean 57.25

Std Dev 7.6

8

6

4

2

0

ampl

0

10

20

30

40

50

60

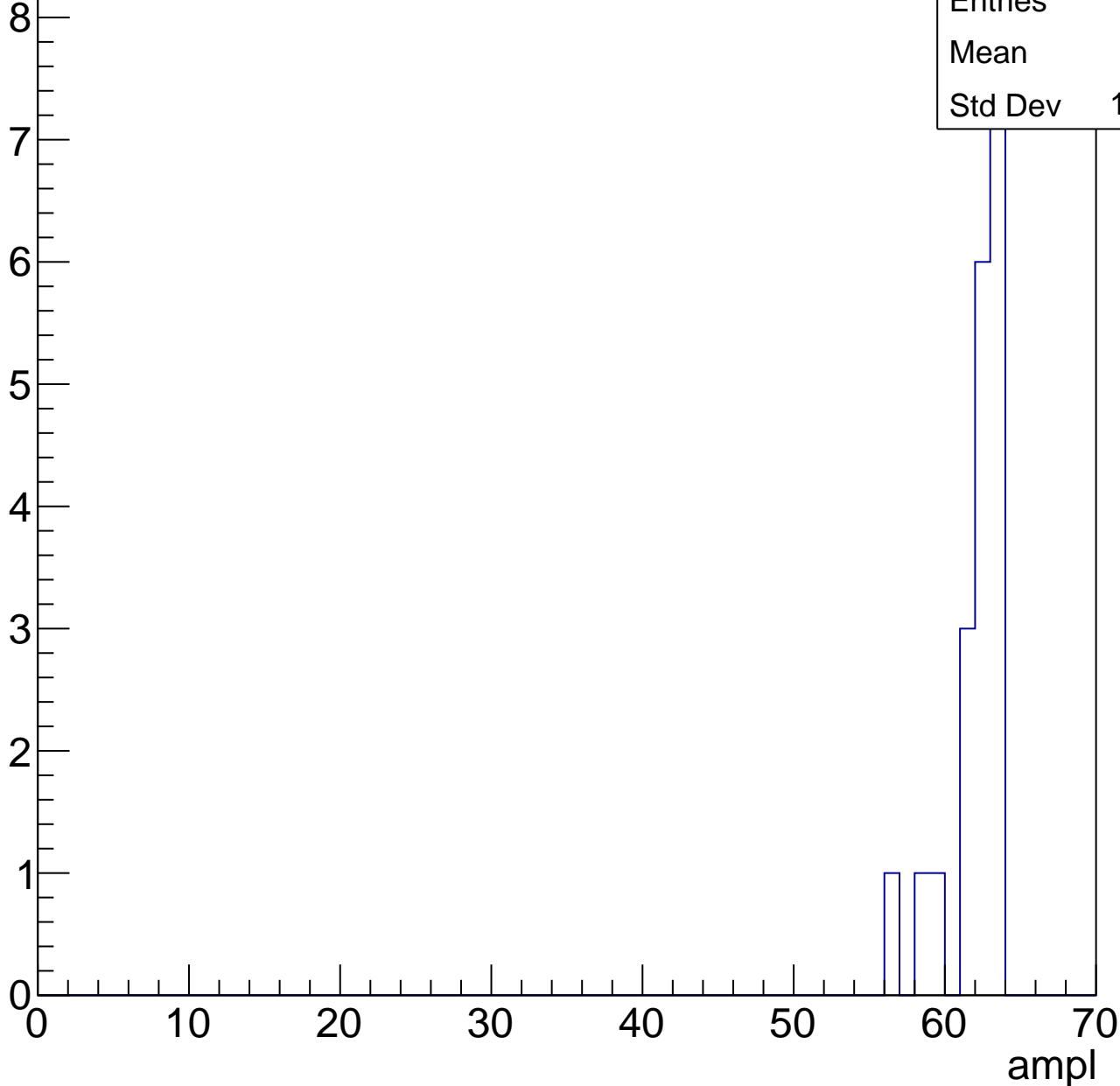
70

# B0L000S, U7-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	20
Mean	61.6
Std Dev	1.855



# B0L000S, U7-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L000S, U7-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch48, adc0

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	85
Mean	29.88
Std Dev	5.771

**Gaus mean : 31.4719**

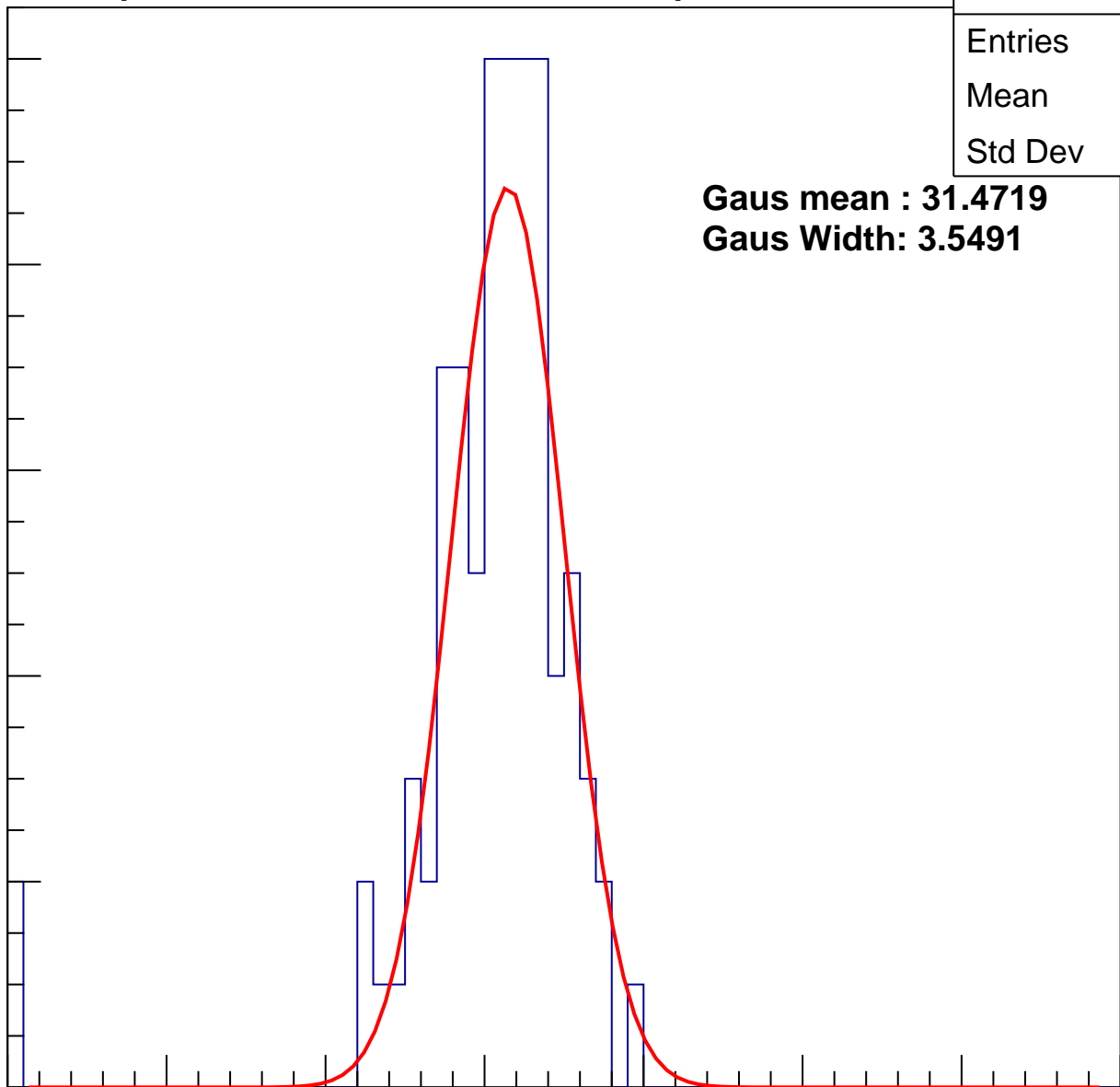
**Gaus Width: 3.5491**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L000S, U7-ch48, adc1

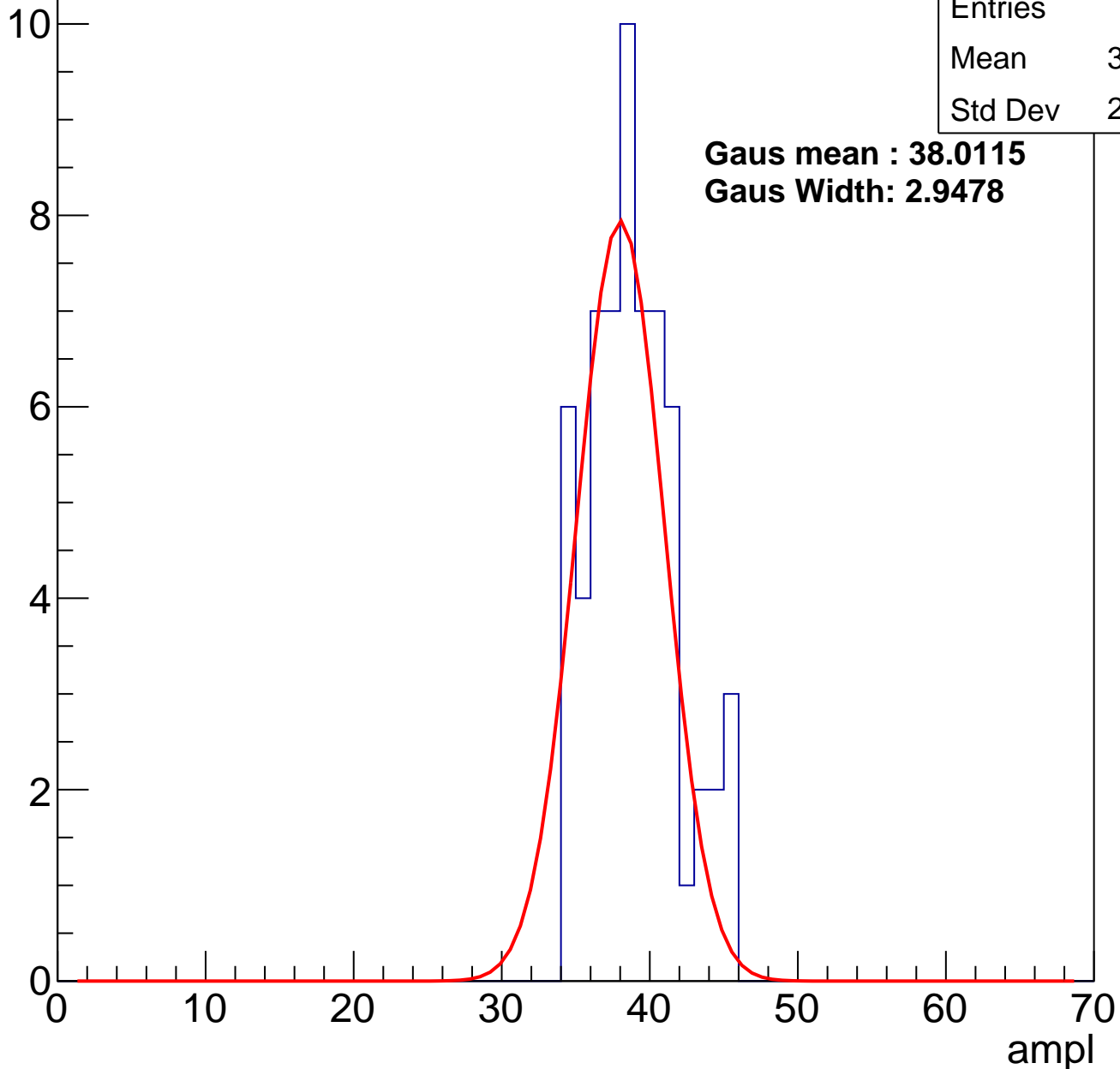
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	62
Mean	38.47
Std Dev	2.917

**Gaus mean : 38.0115**

**Gaus Width: 2.9478**

Entry



# B0L000S, U7-ch48, adc2

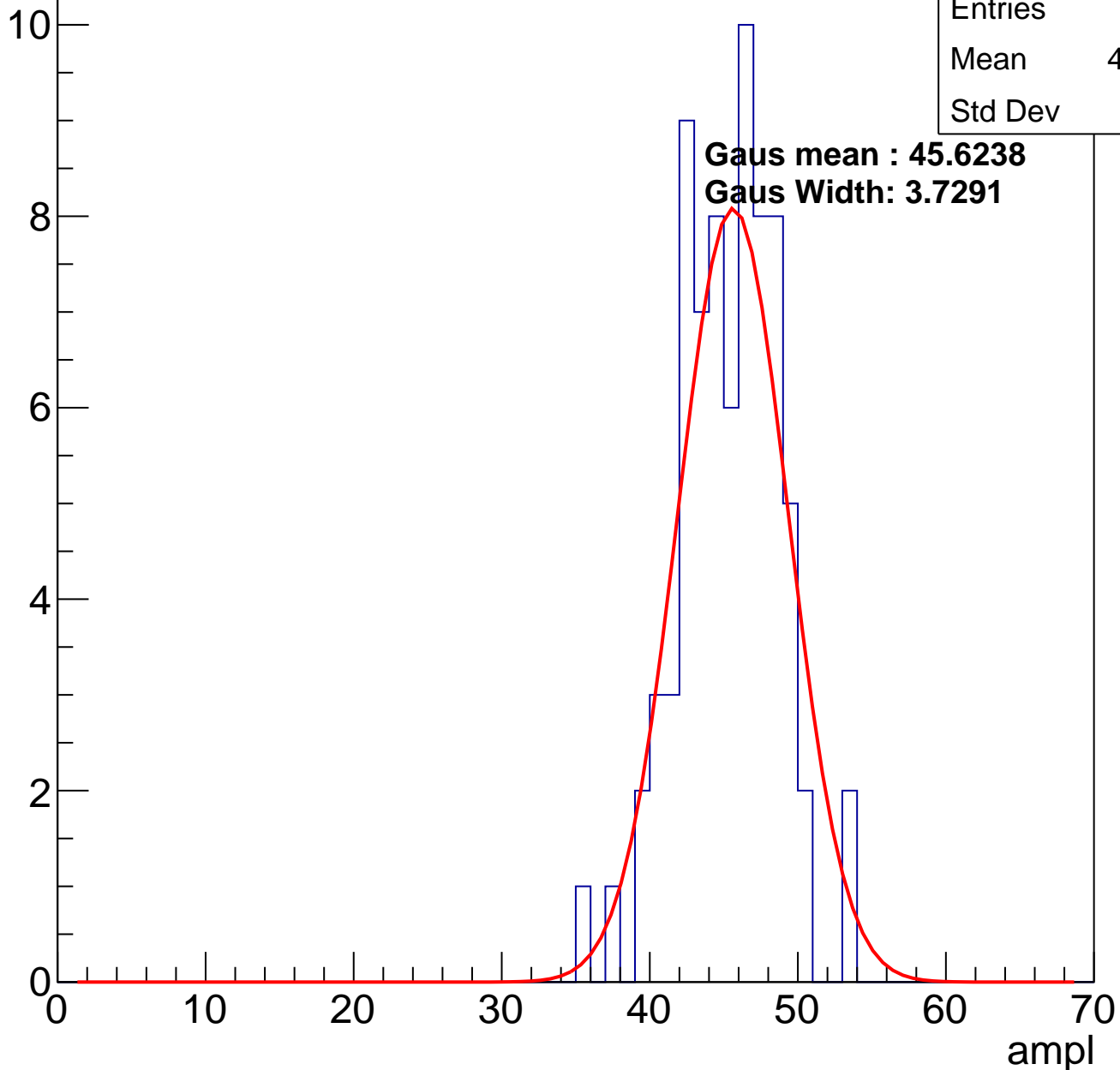
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	75
Mean	44.87
Std Dev	3.36

**Gaus mean : 45.6238**

**Gaus Width: 3.7291**

Entry

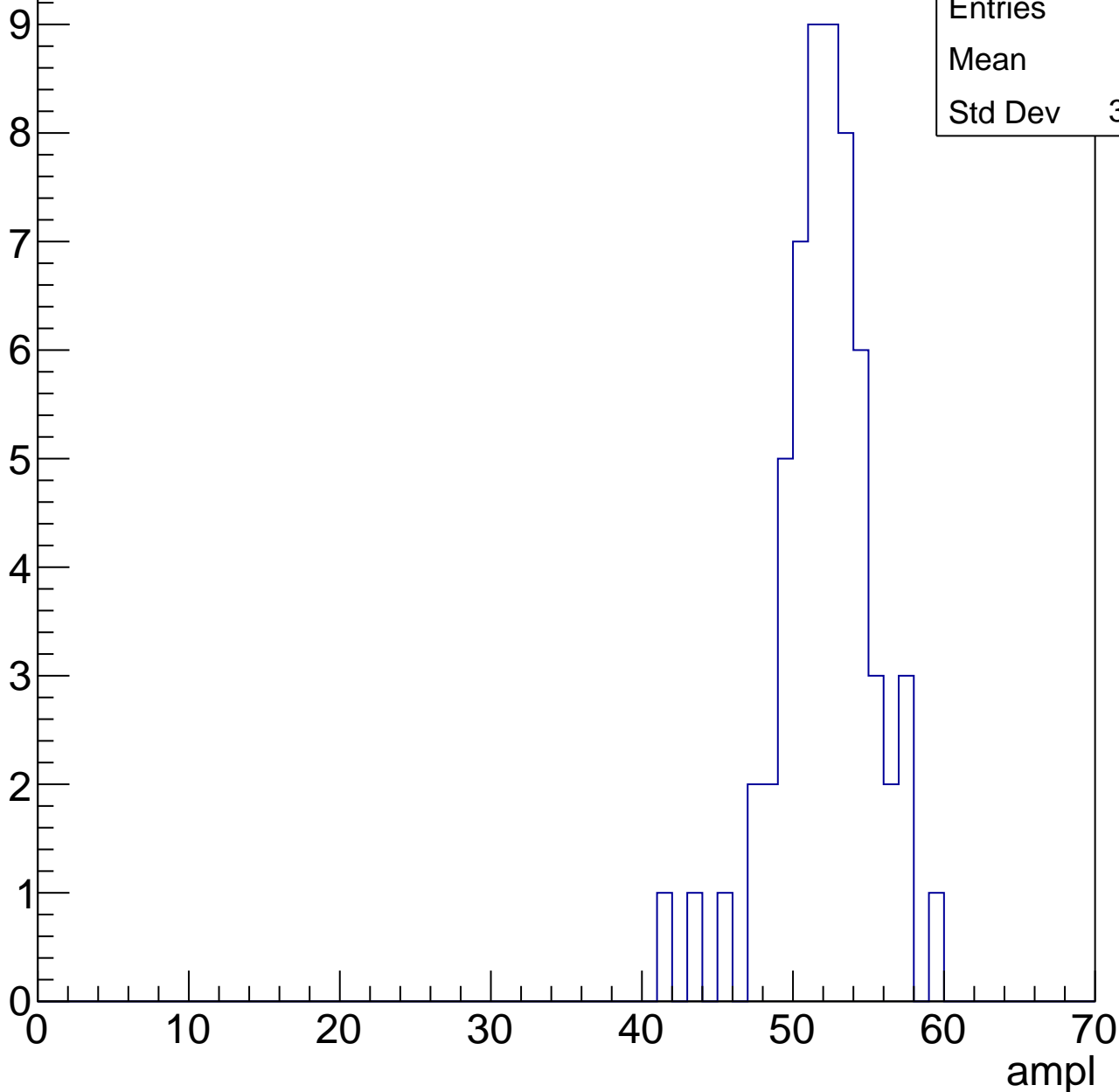


# B0L000S, U7-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	60
Mean	51.6
Std Dev	3.216

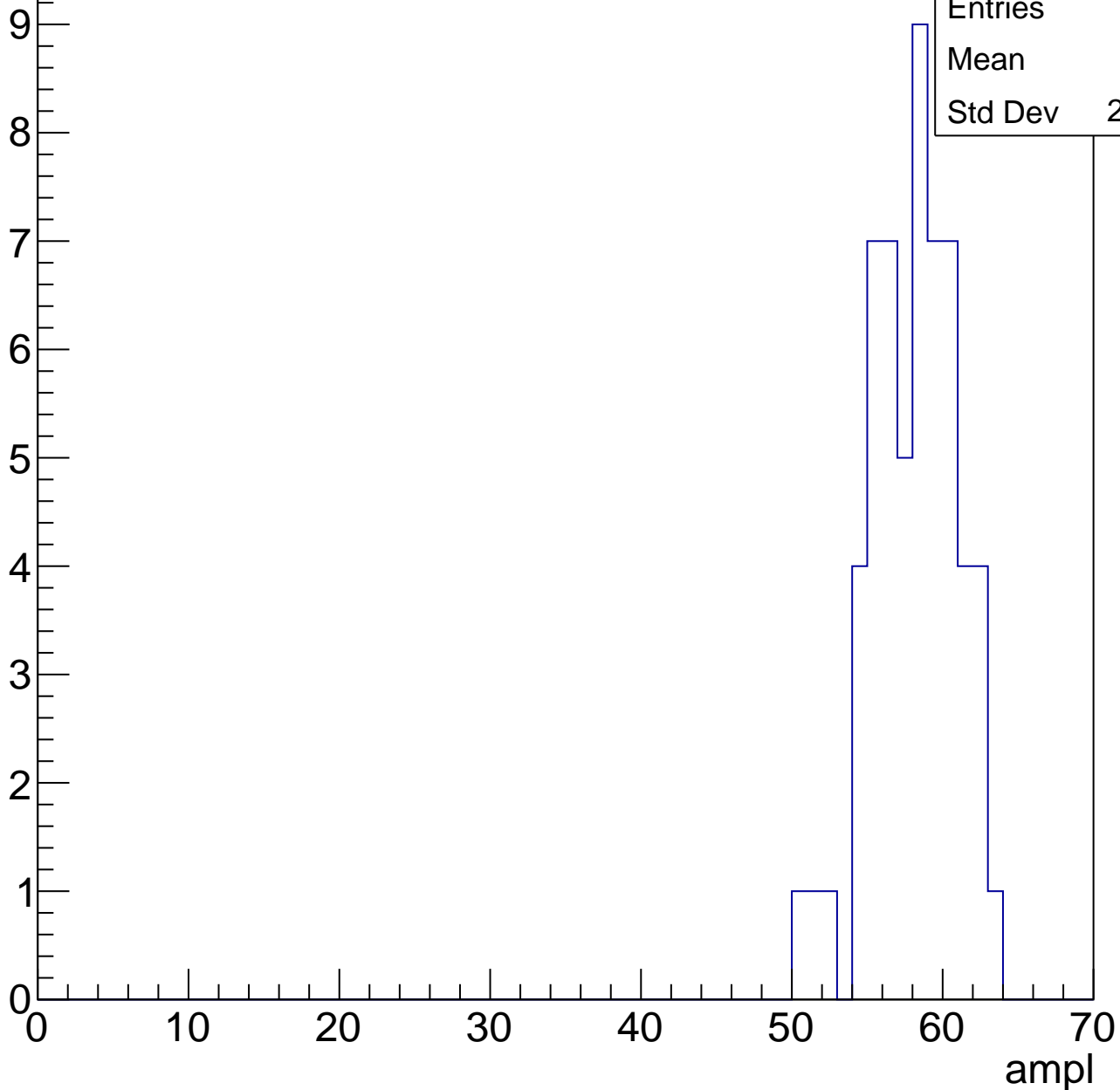


# B0L000S, U7-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	58
Mean	57.6
Std Dev	2.816

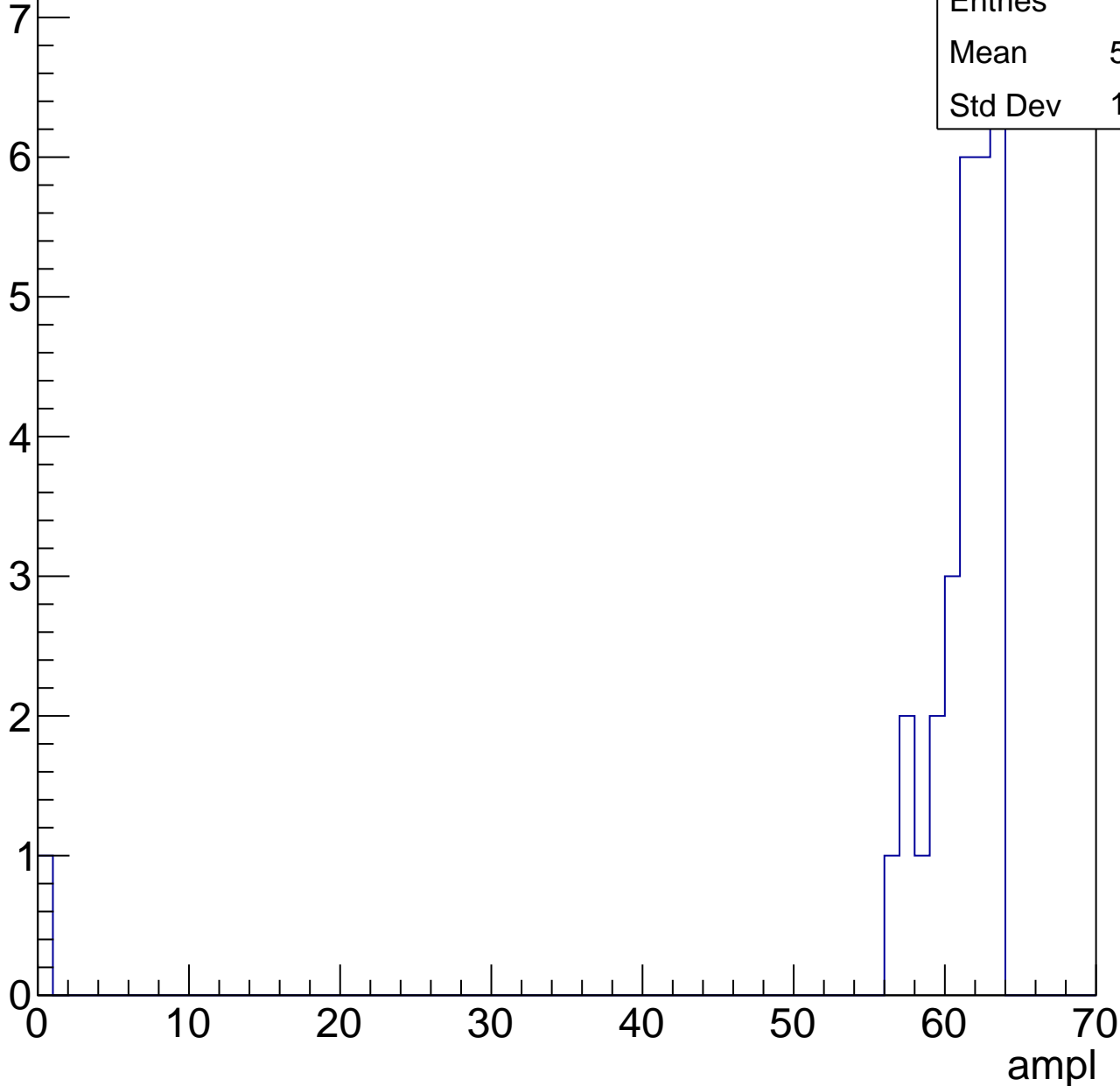


# B0L000S, U7-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	29
Mean	58.79
Std Dev	11.28



# B0L000S, U7-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	2
Mean	63
Std Dev	0



# B0L000S, U7-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch49, adc0

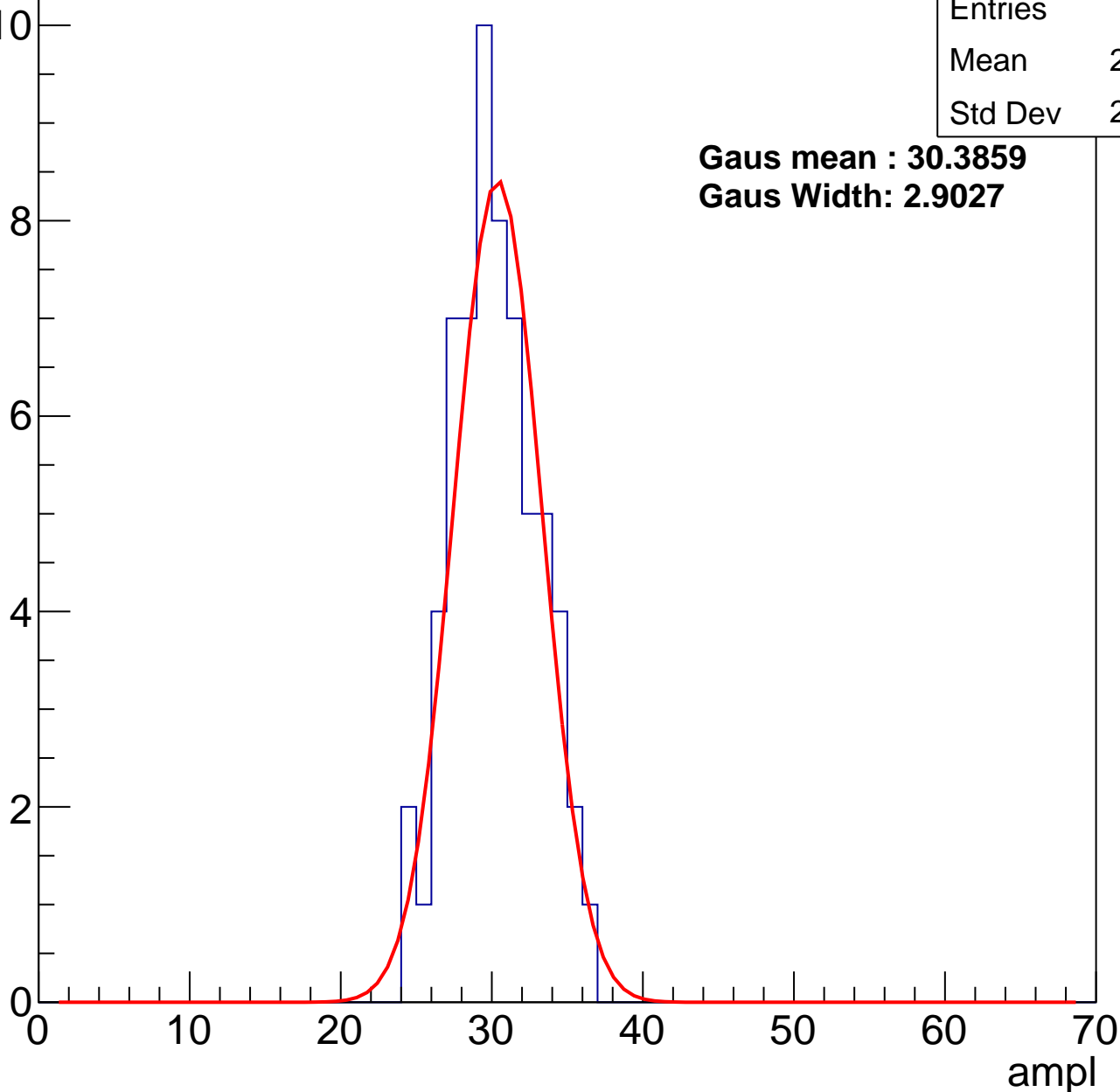
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	63
Mean	29.78
Std Dev	2.763

**Gaus mean : 30.3859**

**Gaus Width: 2.9027**



# B0L000S, U7-ch49, adc1

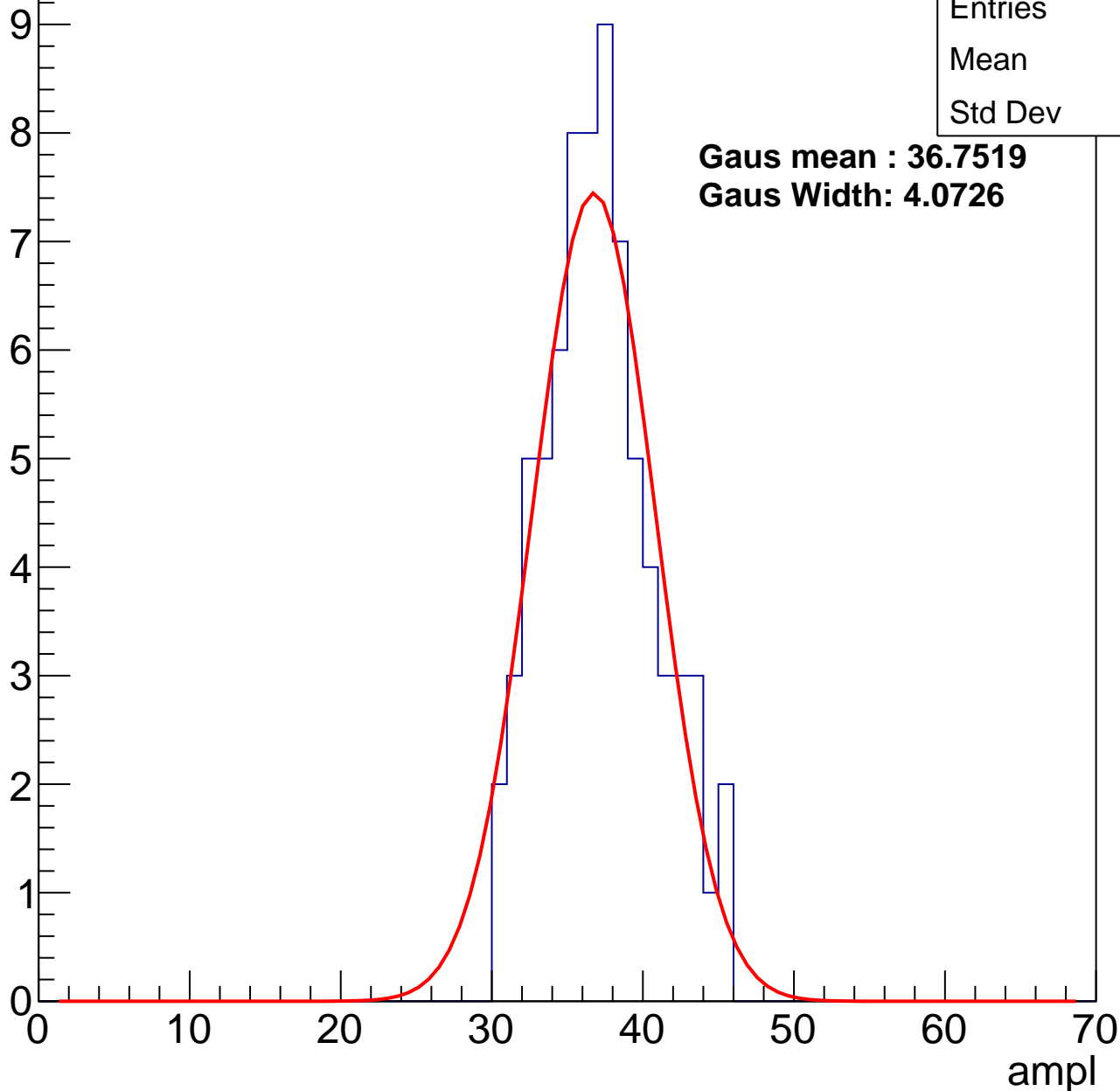
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	74
Mean	36.7
Std Dev	3.62

**Gaus mean : 36.7519**

**Gaus Width: 4.0726**



# B0L000S, U7-ch49, adc2

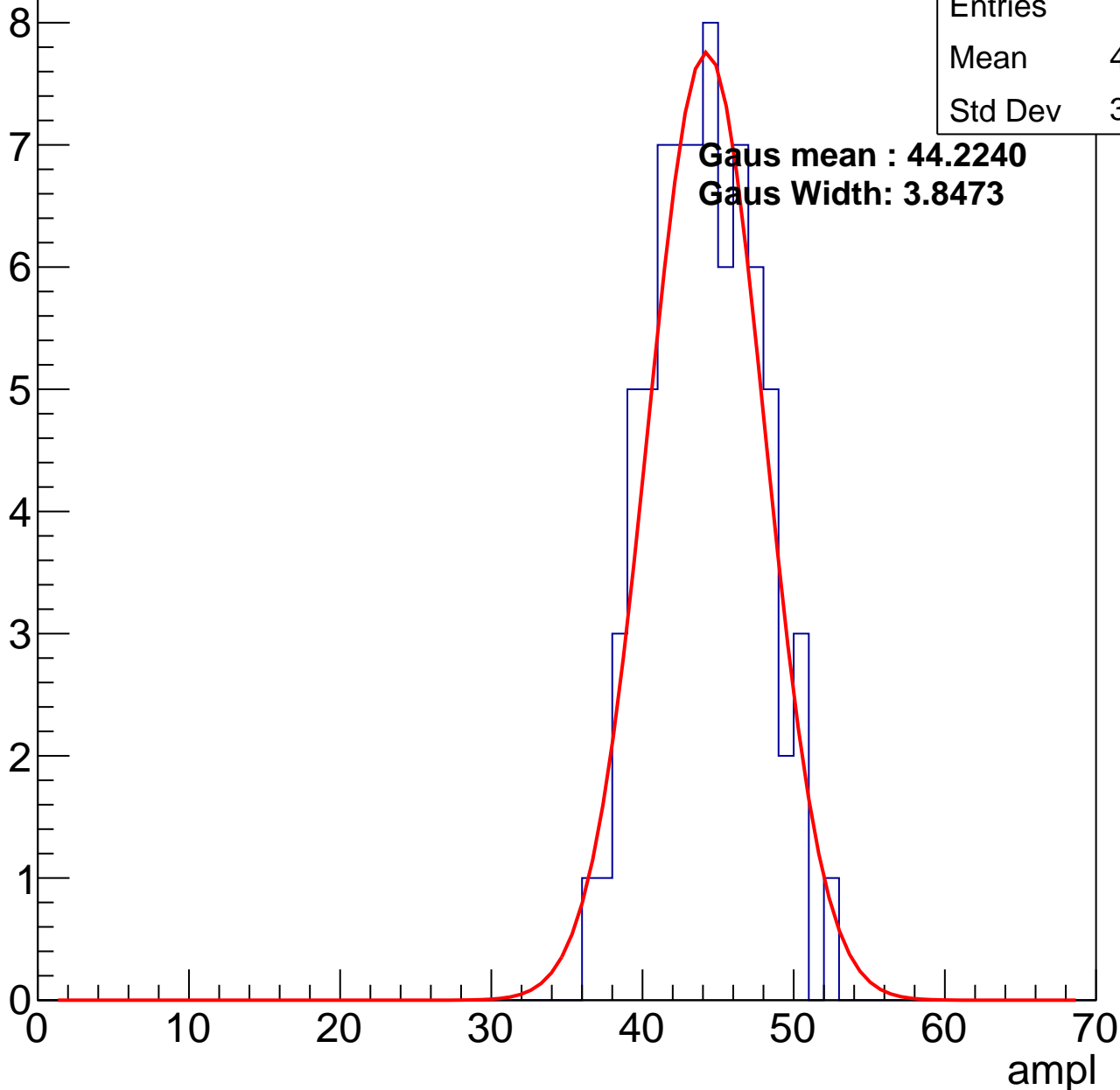
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	74
Mean	43.65
Std Dev	3.497

**Gaus mean : 44.2240**

**Gaus Width: 3.8473**

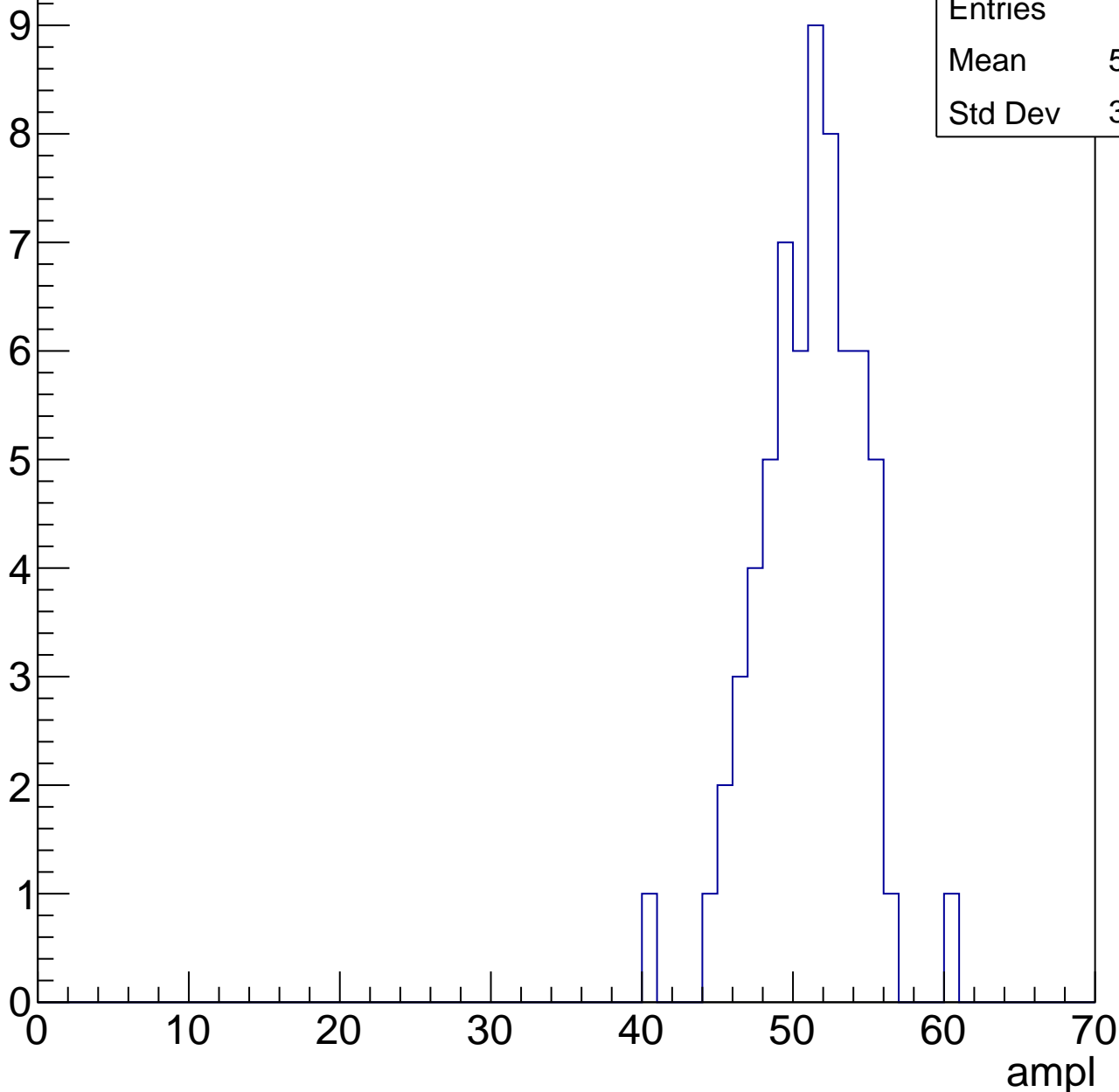


# B0L000S, U7-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	65
Mean	50.63
Std Dev	3.335

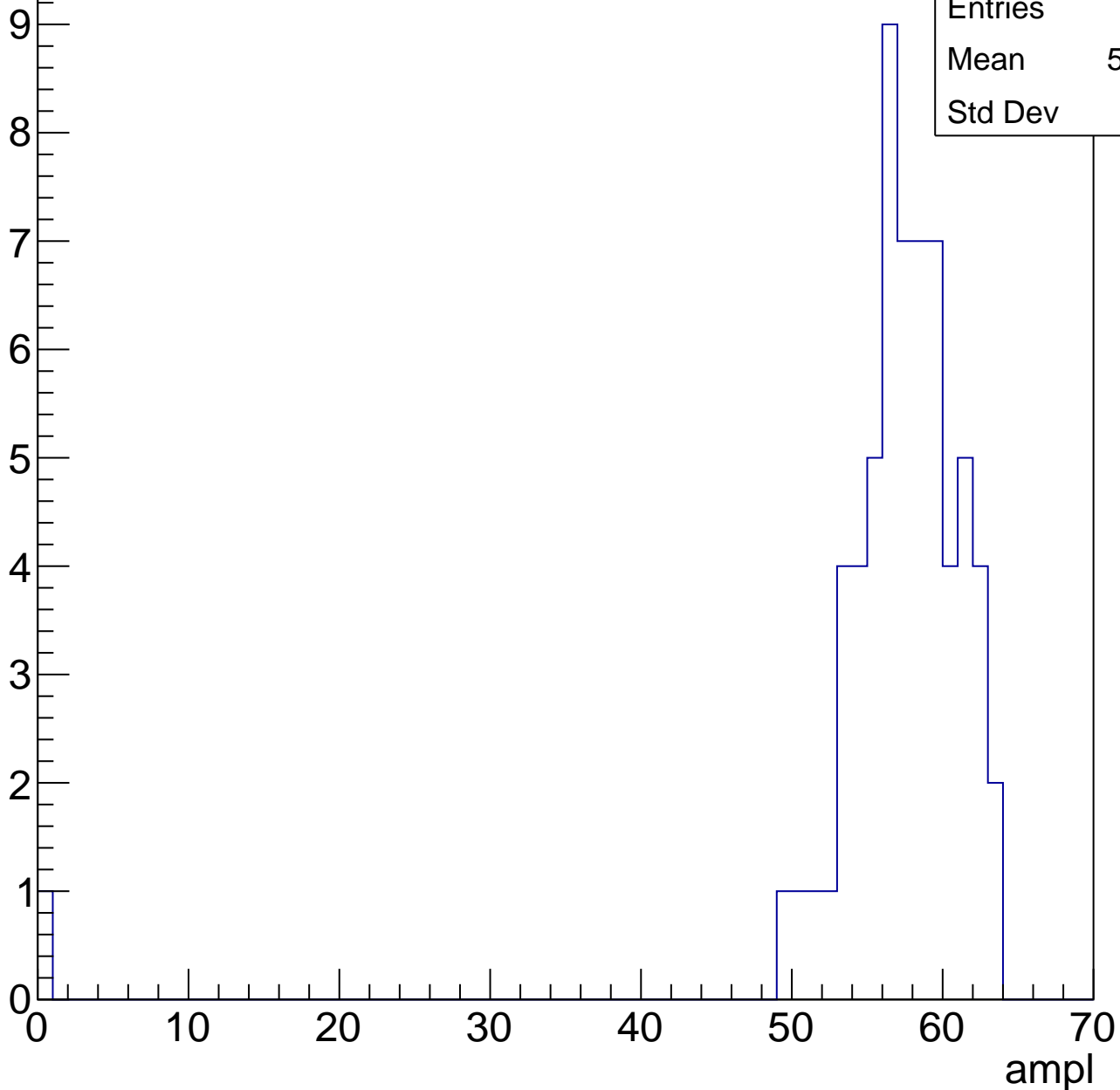


# B0L000S, U7-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	63
Mean	56.29
Std Dev	7.81



# B0L000S, U7-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	32
Mean	60.66
Std Dev	1.978

ampl

0

10

20

30

40

50

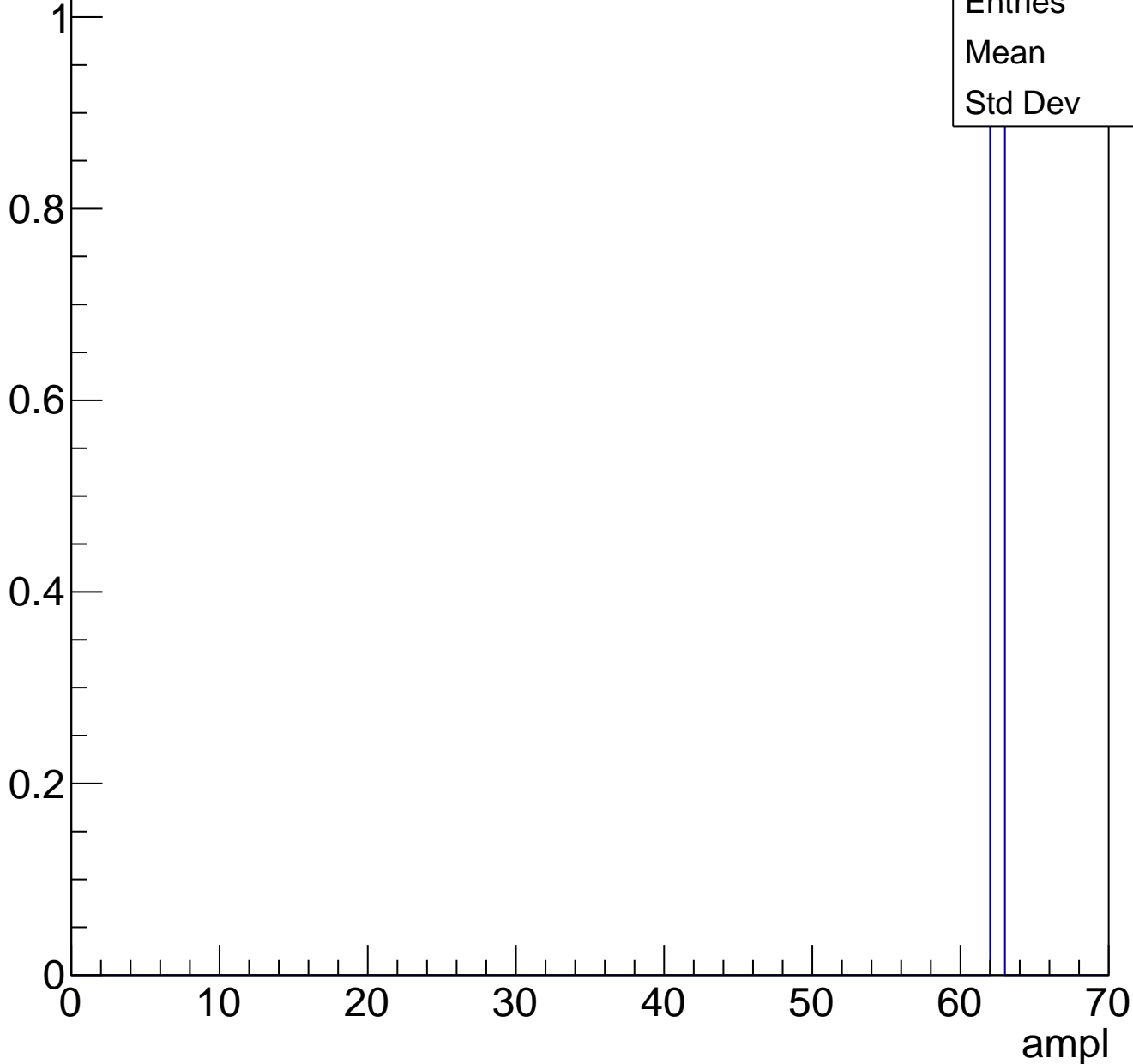
60

70

# B0L000S, U7-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	3
Mean	7.333
Std Dev	10.37

# B0L000S, U7-ch50, adc0

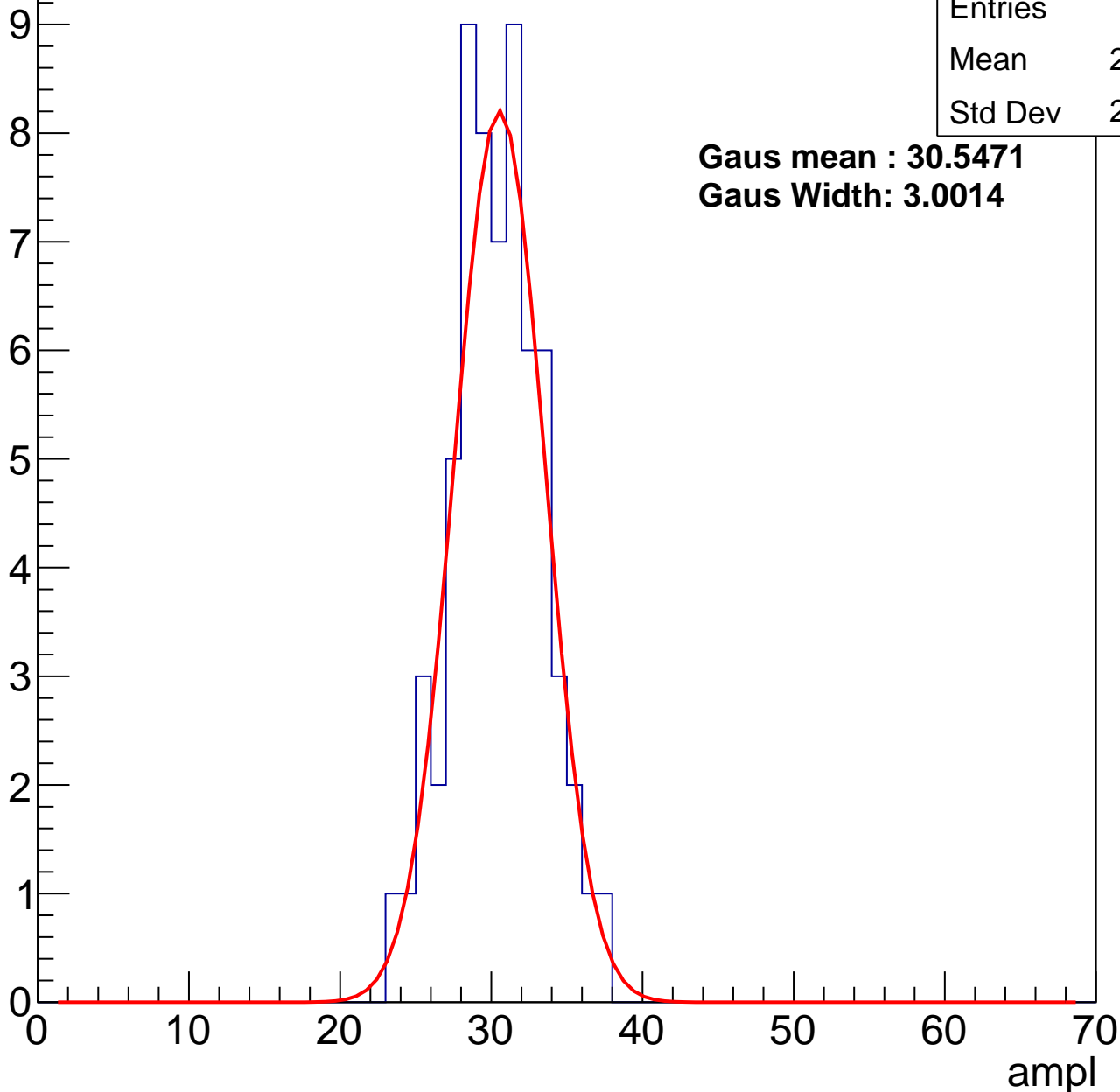
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	64
Mean	29.95
Std Dev	2.934

**Gaus mean : 30.5471**

**Gaus Width: 3.0014**



# B0L000S, U7-ch50, adc1

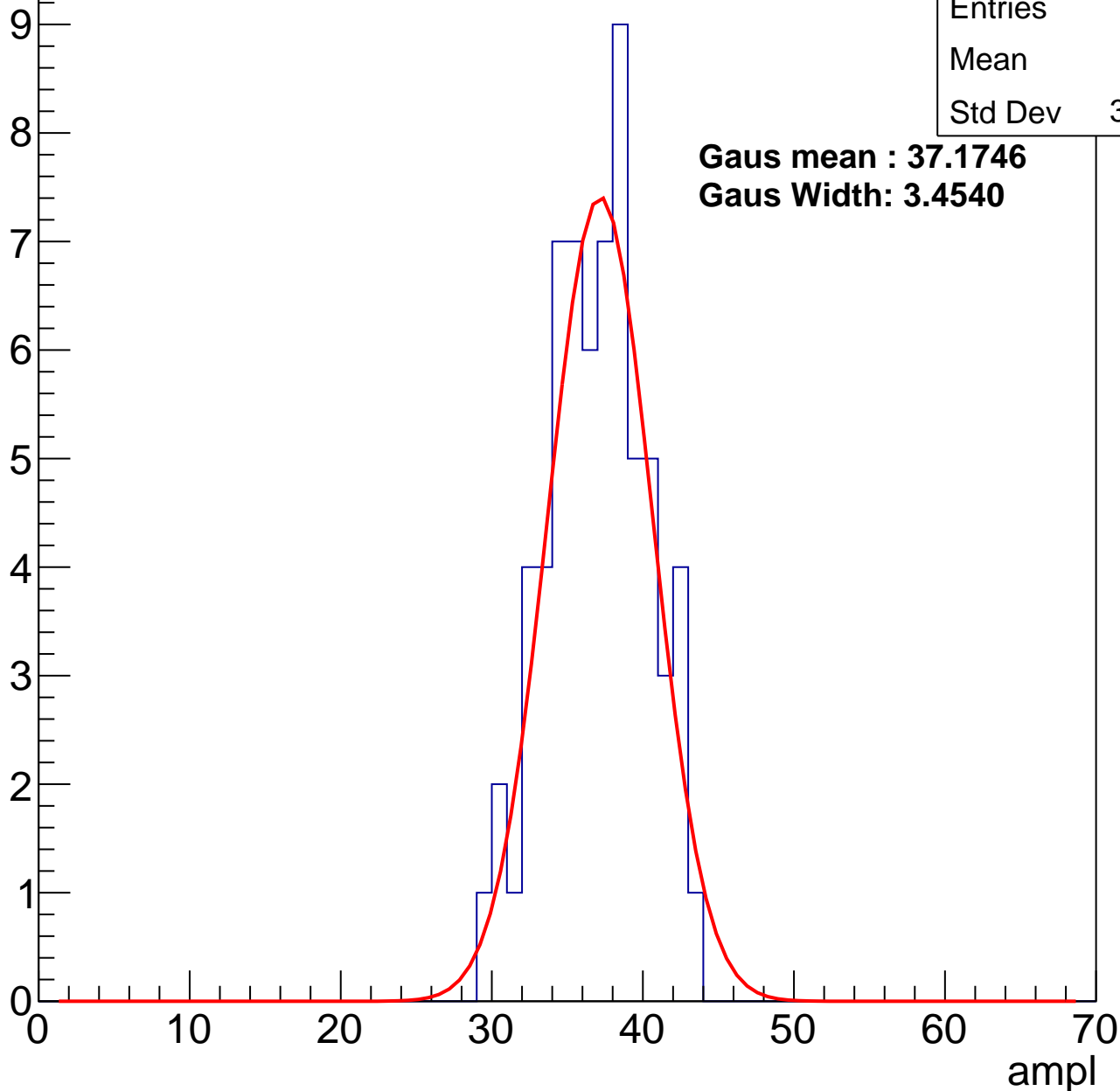
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	66
Mean	36.5
Std Dev	3.258

**Gaus mean : 37.1746**

**Gaus Width: 3.4540**

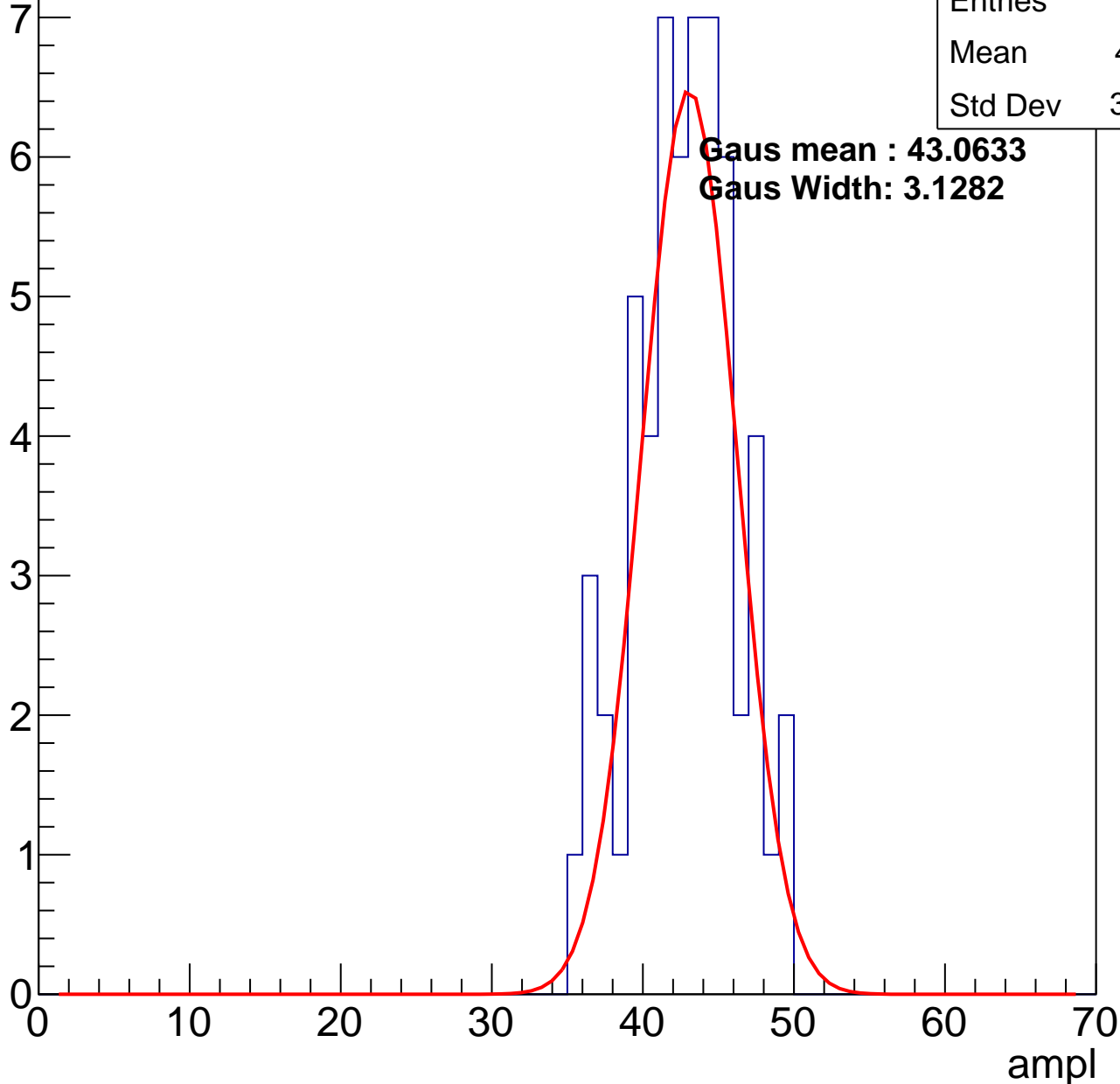


# B0L000S, U7-ch50, adc2

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	58
Mean	42.31
Std Dev	3.323

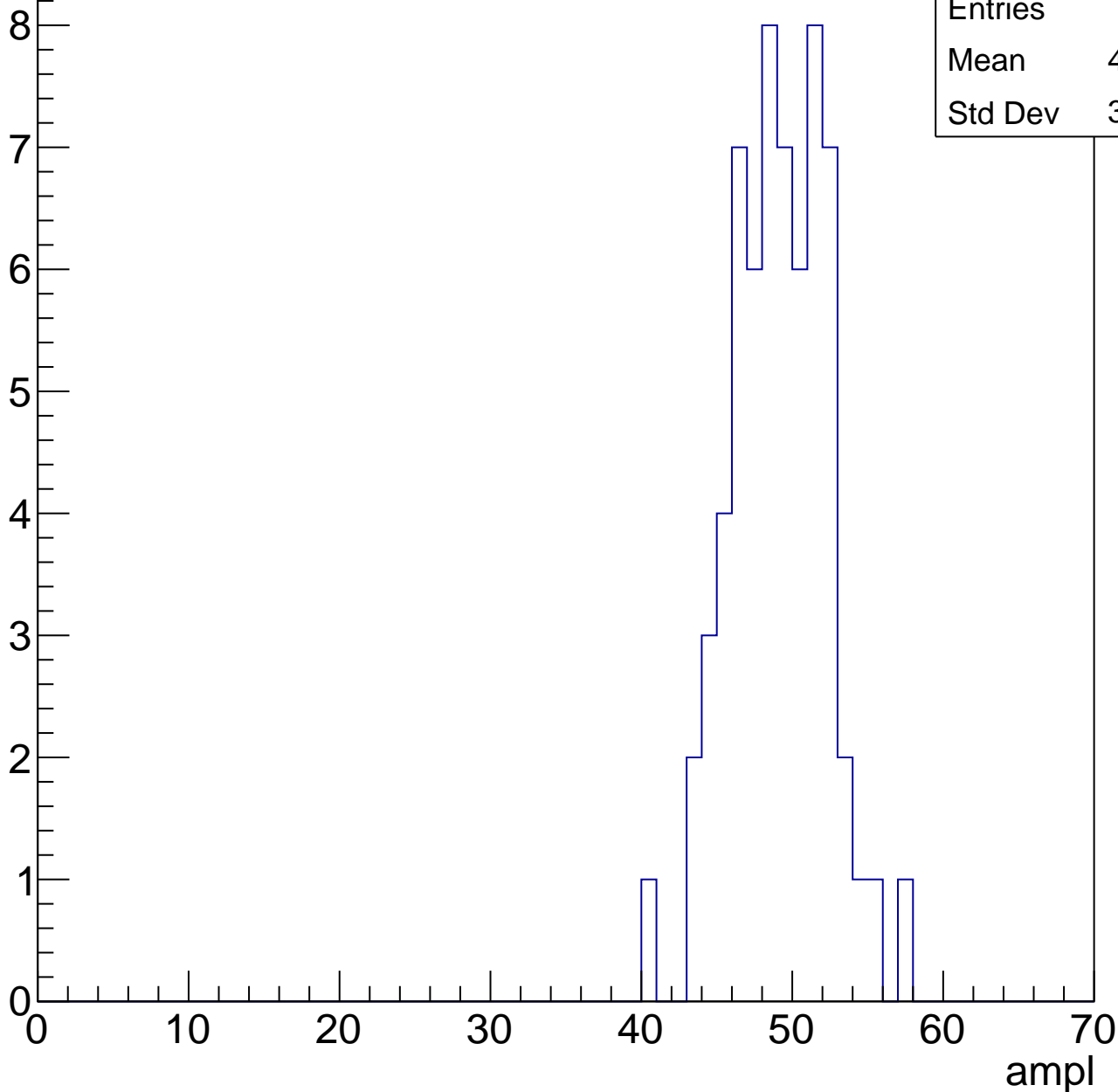


# B0L000S, U7-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	64
Mean	48.64
Std Dev	3.154

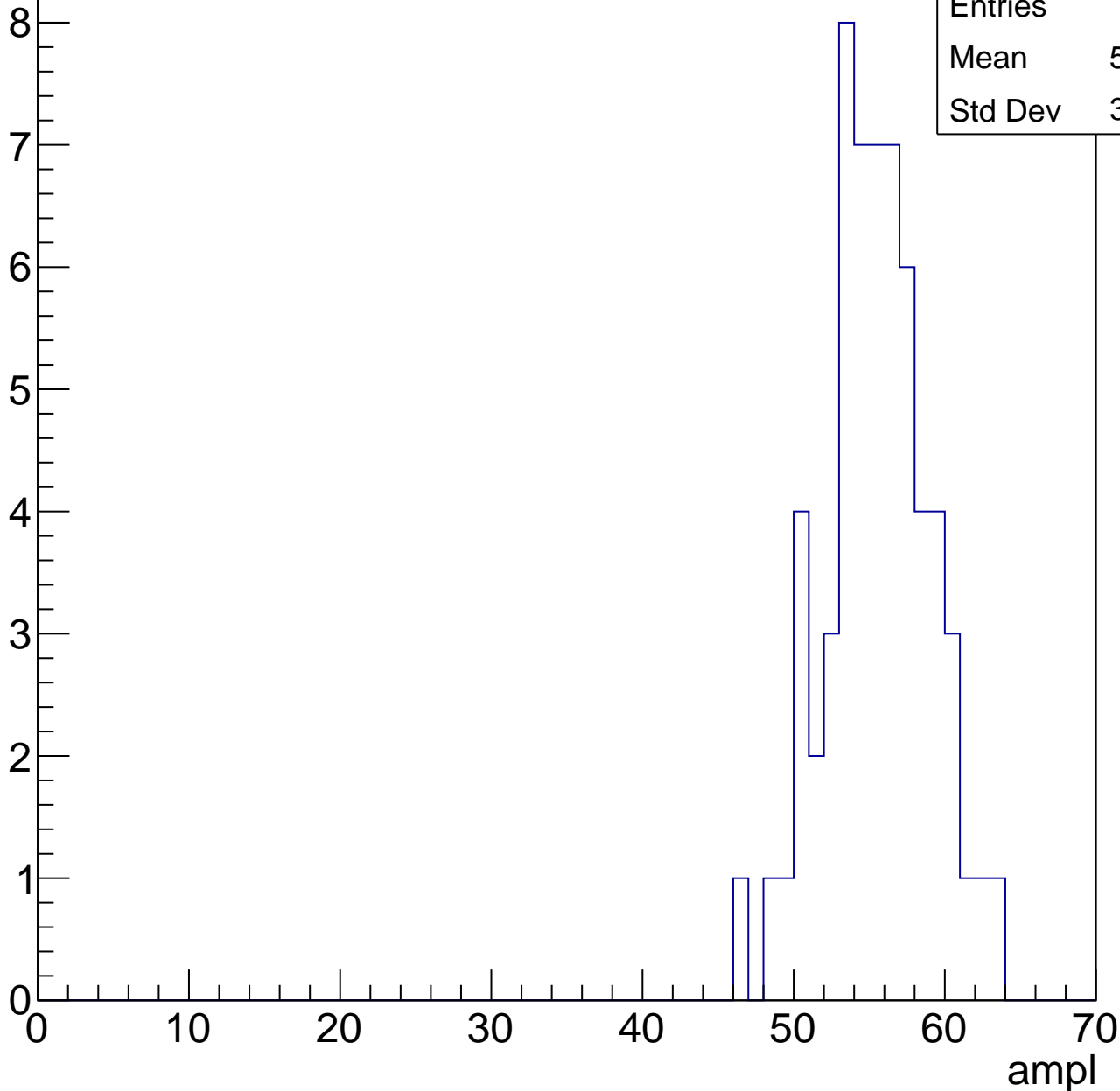


# B0L000S, U7-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

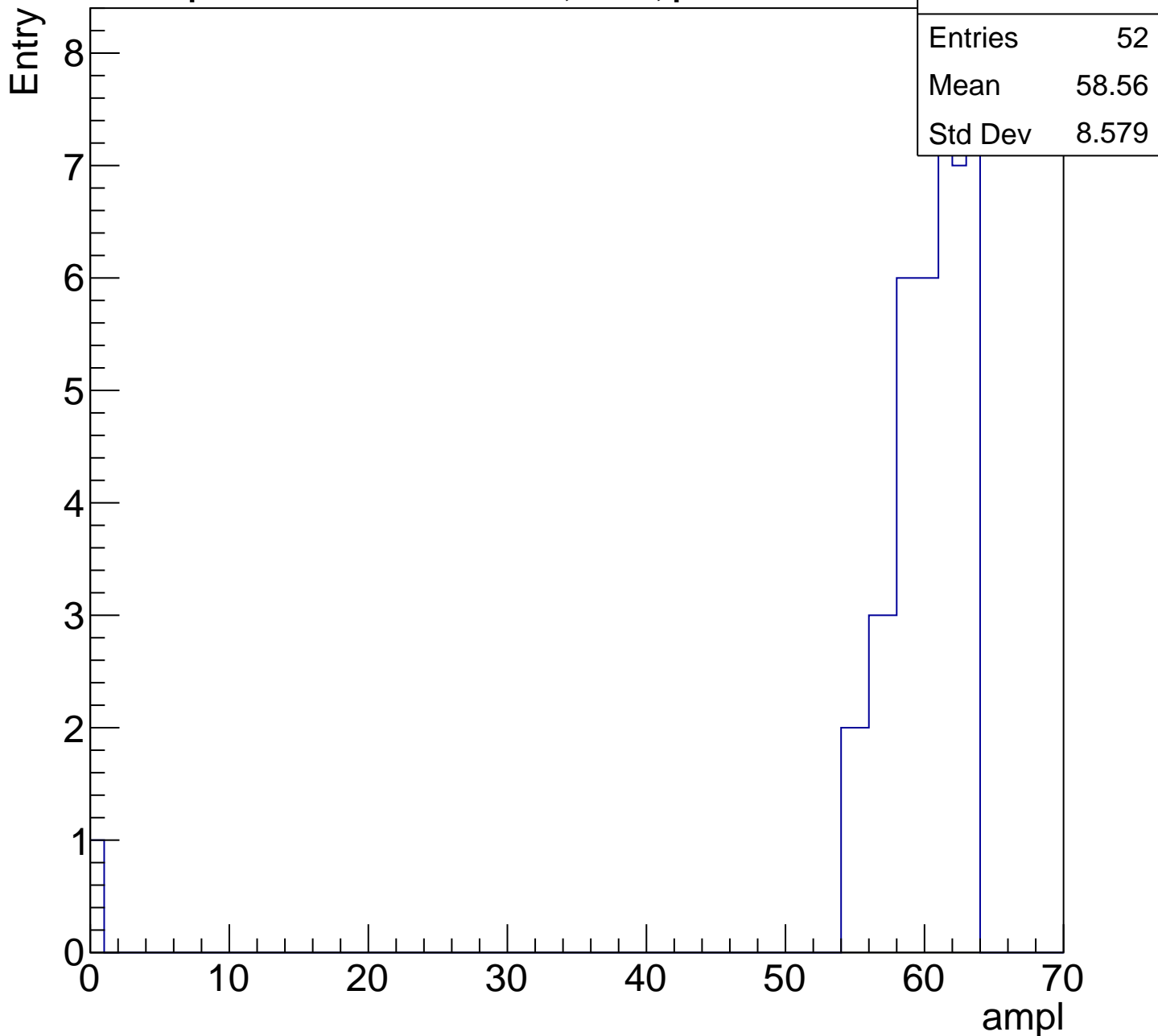
Entry

Entries	61
Mean	55.02
Std Dev	3.433



# B0L000S, U7-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1



# B0L000S, U7-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

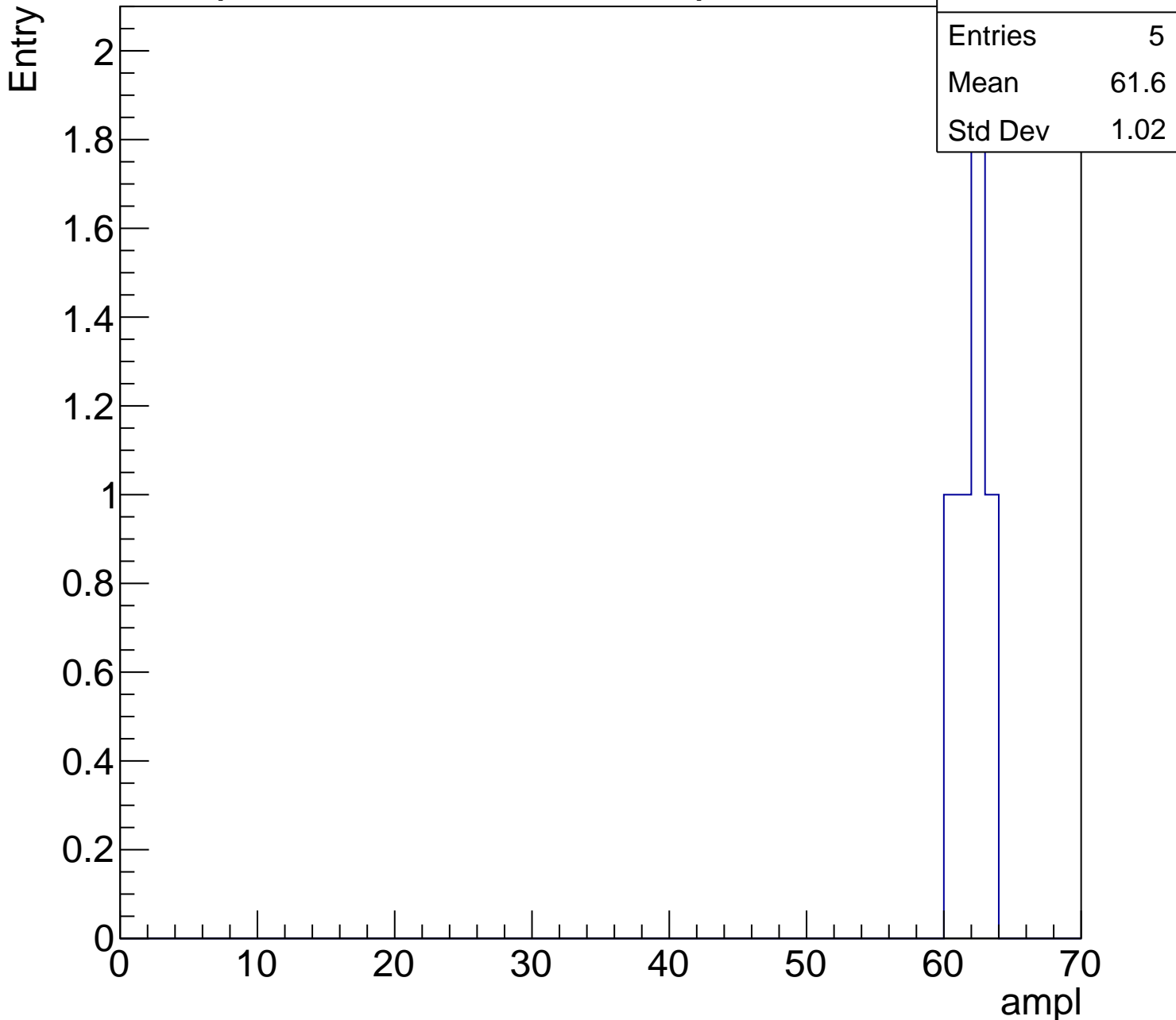
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.6
Std Dev	1.02

0 10 20 30 40 50 60 70

ampl





# B0L000S, U7-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch51, adc0

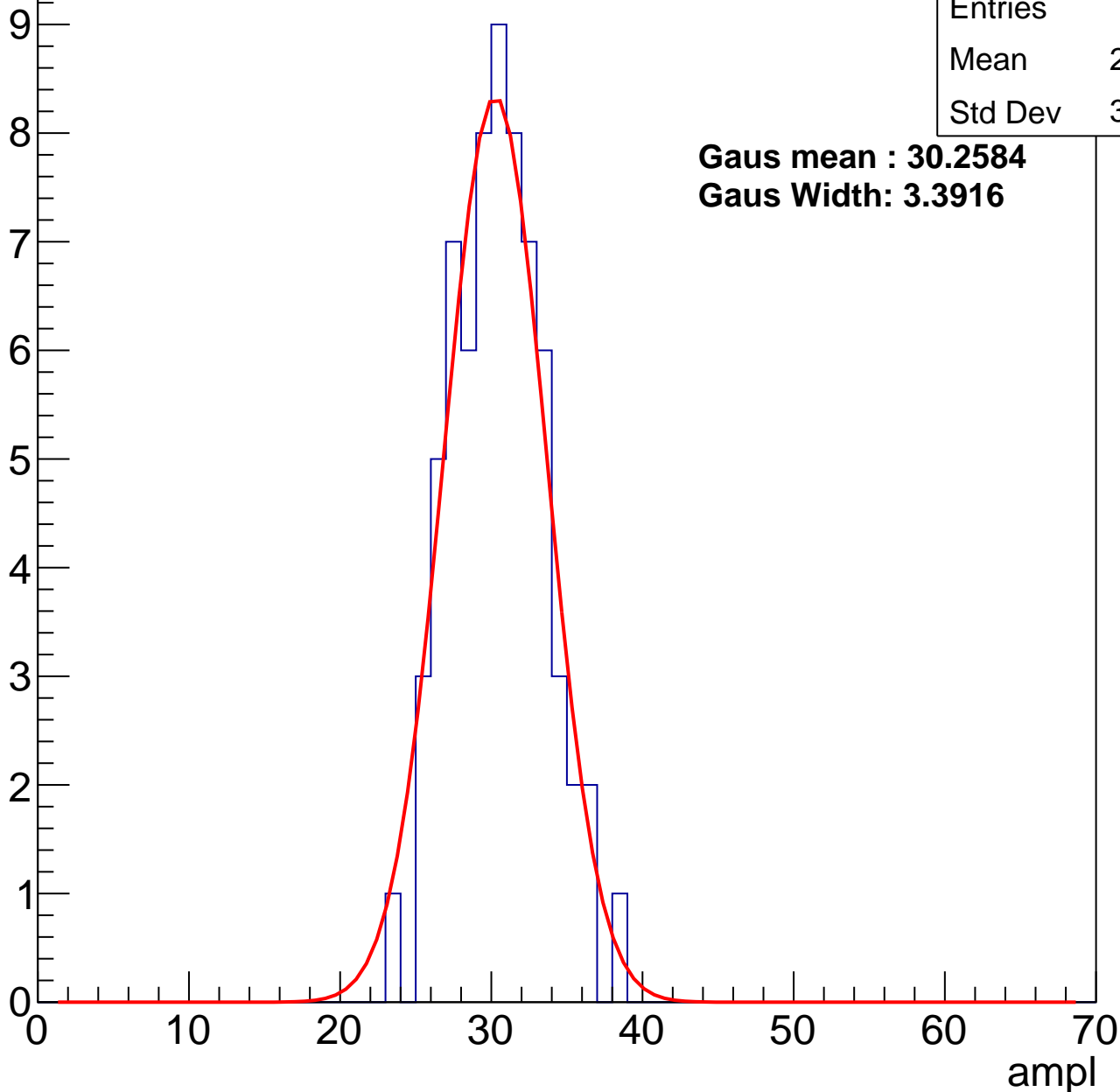
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	68
Mean	29.99
Std Dev	3.027

**Gaus mean : 30.2584**

**Gaus Width: 3.3916**



# B0L000S, U7-ch51, adc1

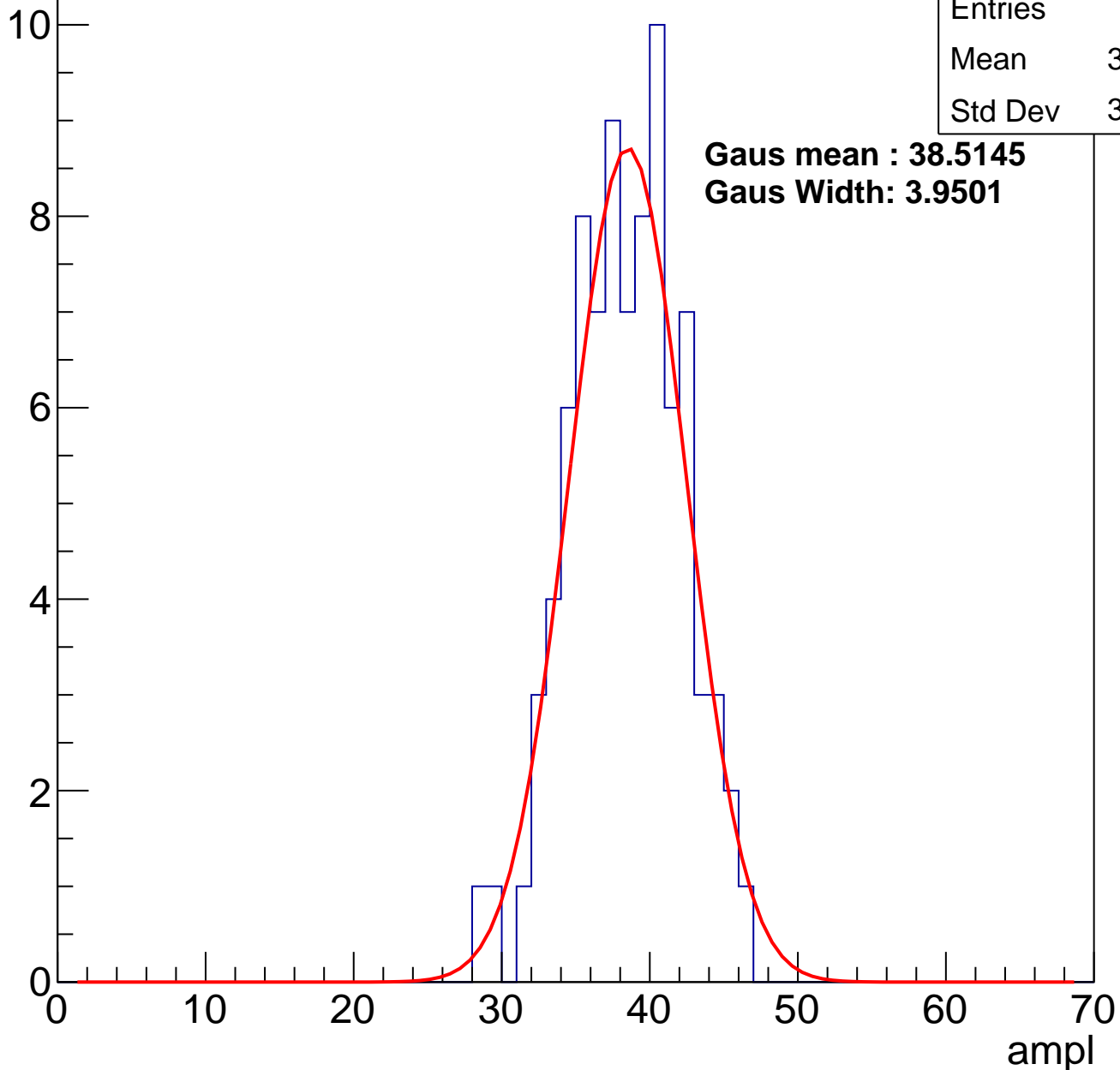
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	87
Mean	37.93
Std Dev	3.716

**Gaus mean : 38.5145**

**Gaus Width: 3.9501**

Entry



# B0L000S, U7-ch51, adc2

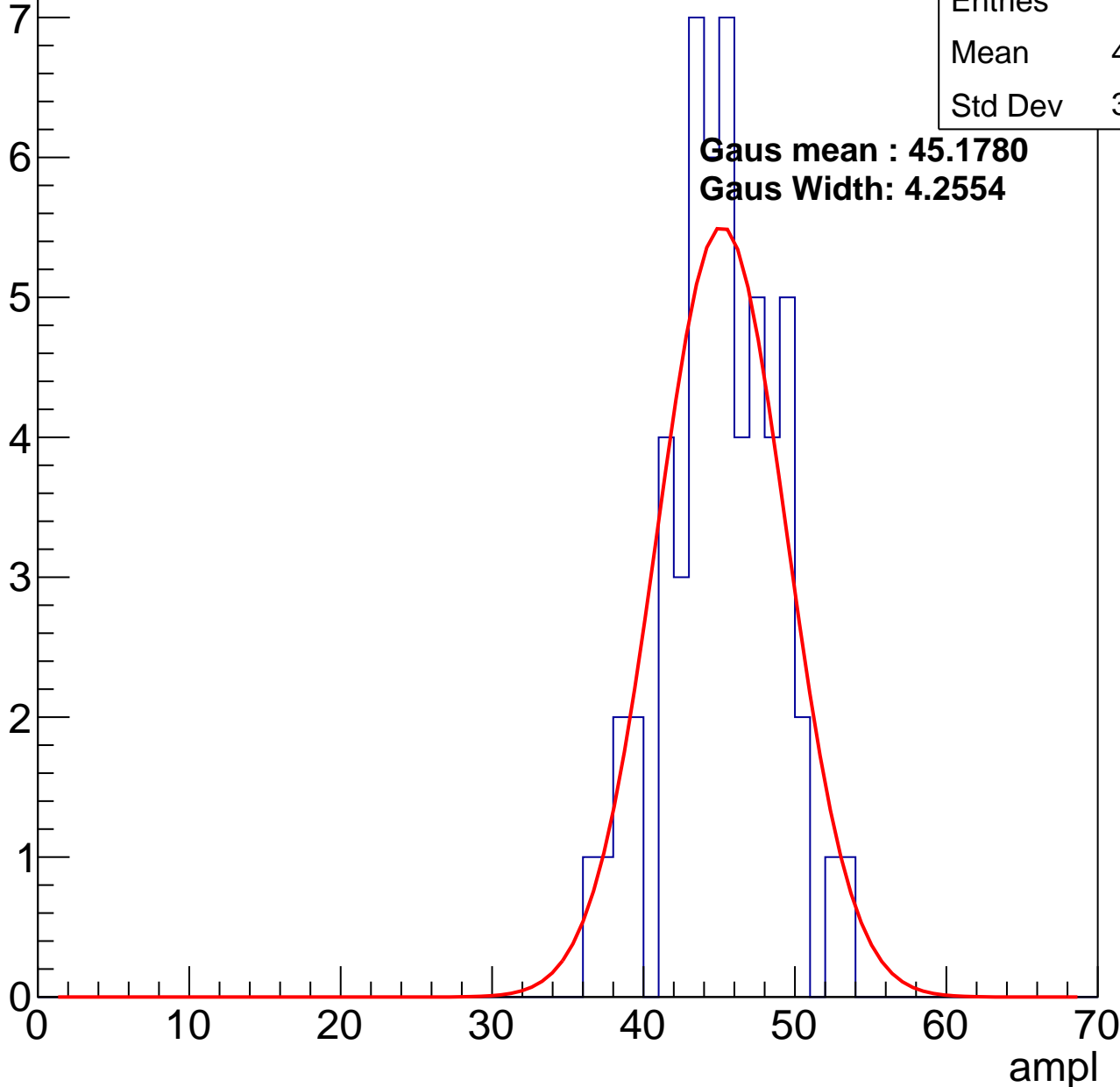
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	55
Mean	44.69
Std Dev	3.662

**Gaus mean : 45.1780**

**Gaus Width: 4.2554**

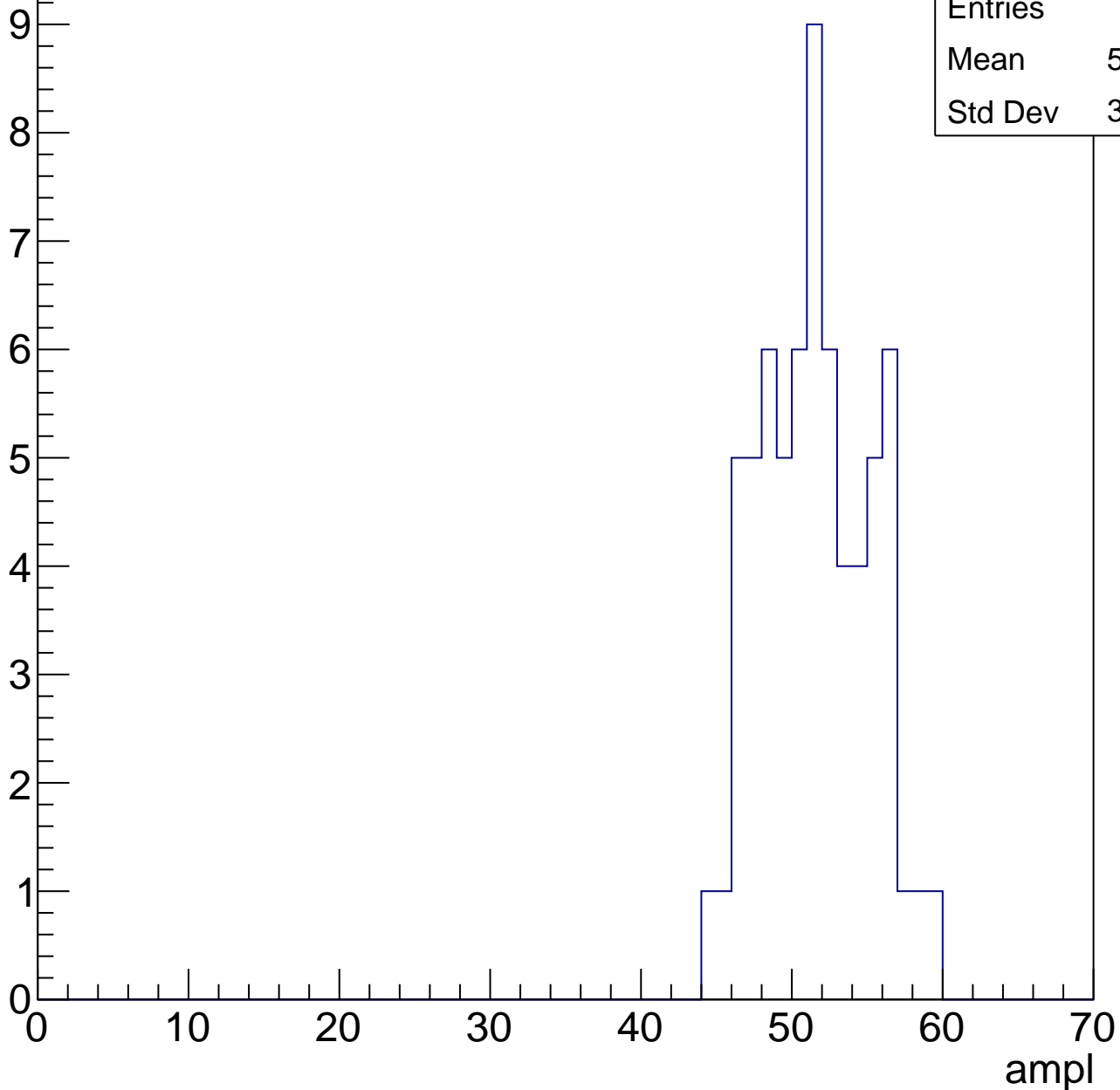


# B0L000S, U7-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

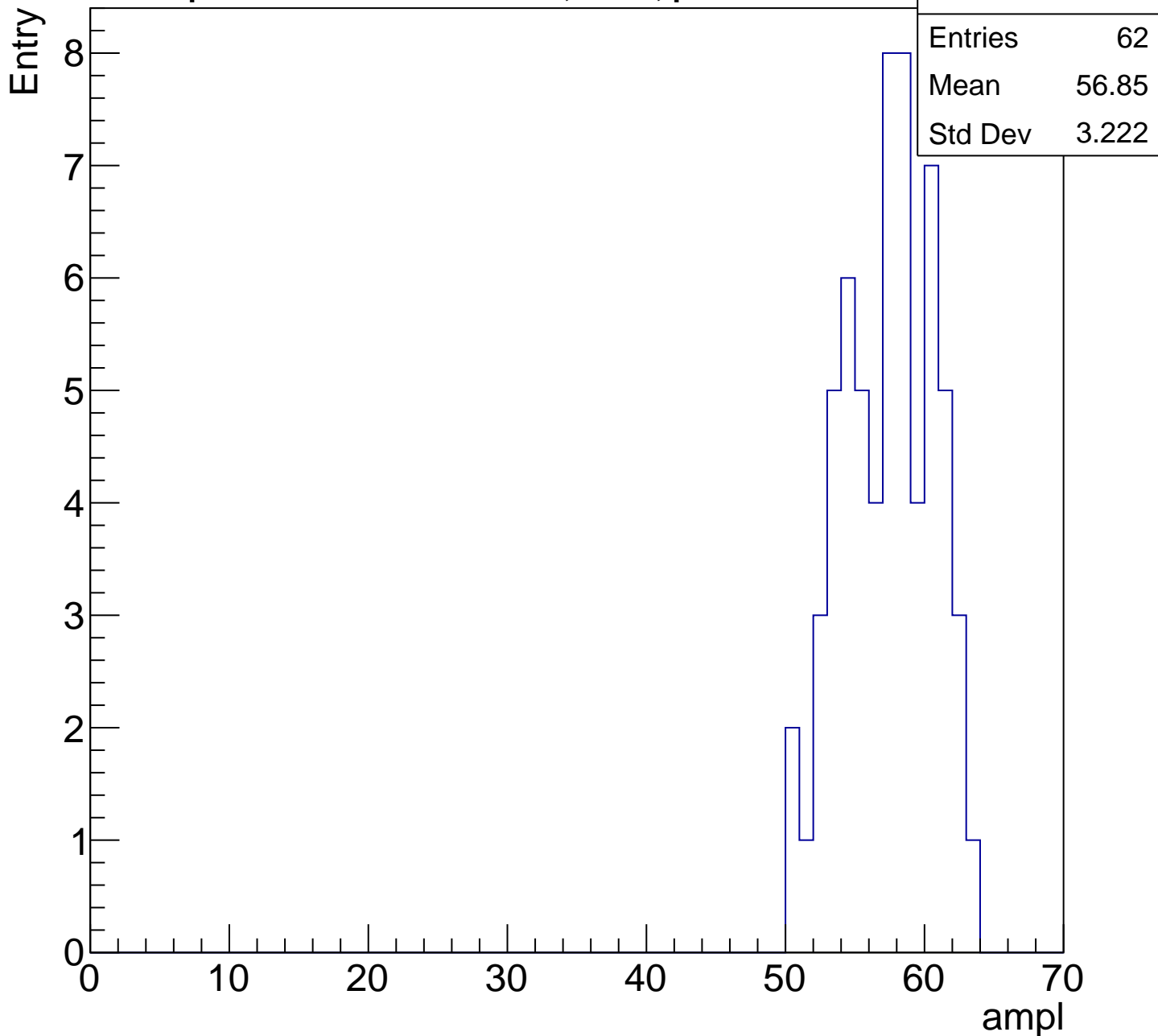
Entry

Entries	66
Mean	51.08
Std Dev	3.496



# B0L000S, U7-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

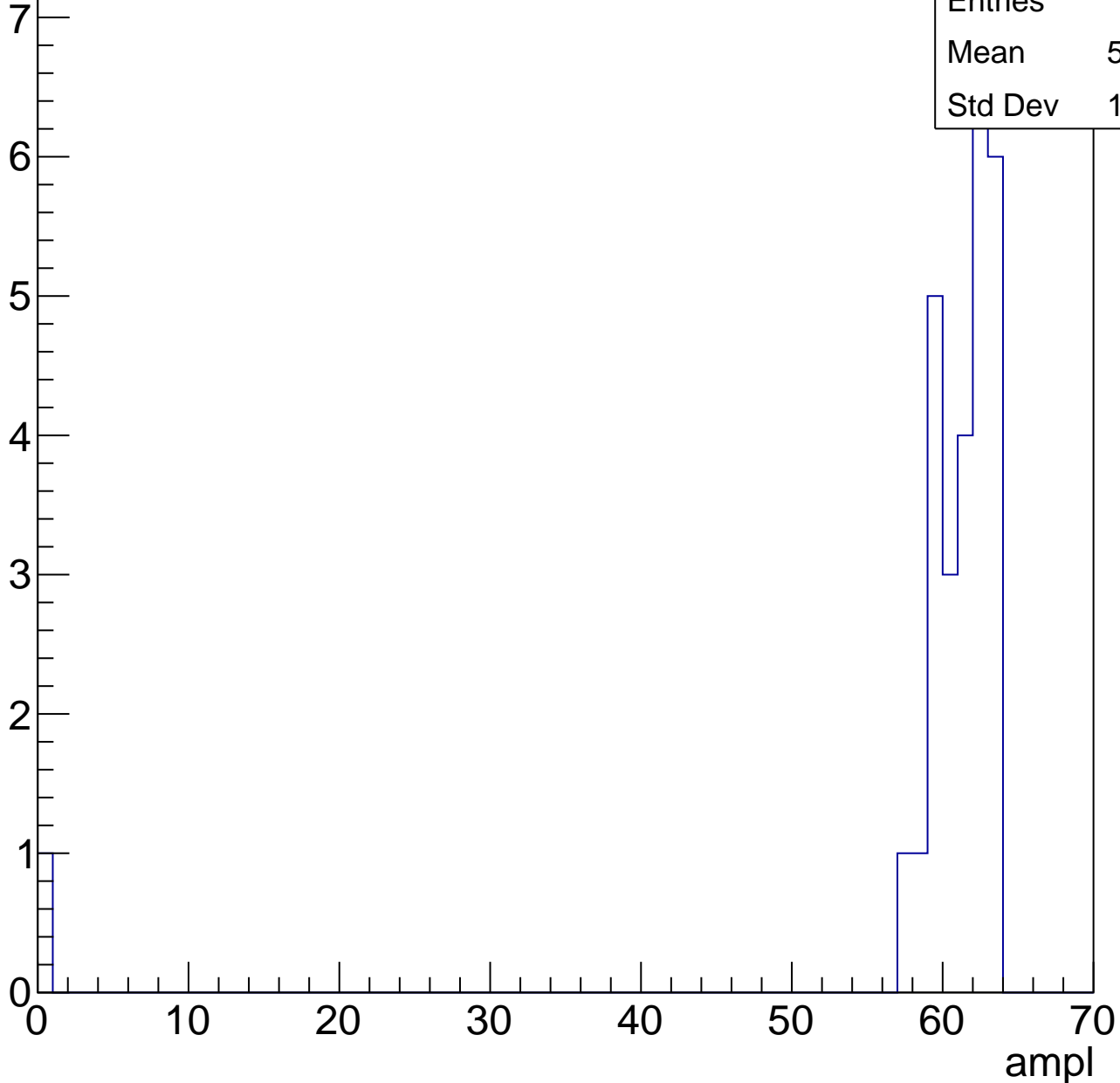


# B0L000S, U7-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	28
Mean	58.79
Std Dev	11.44



# B0L000S, U7-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L000S, U7-ch52, adc0

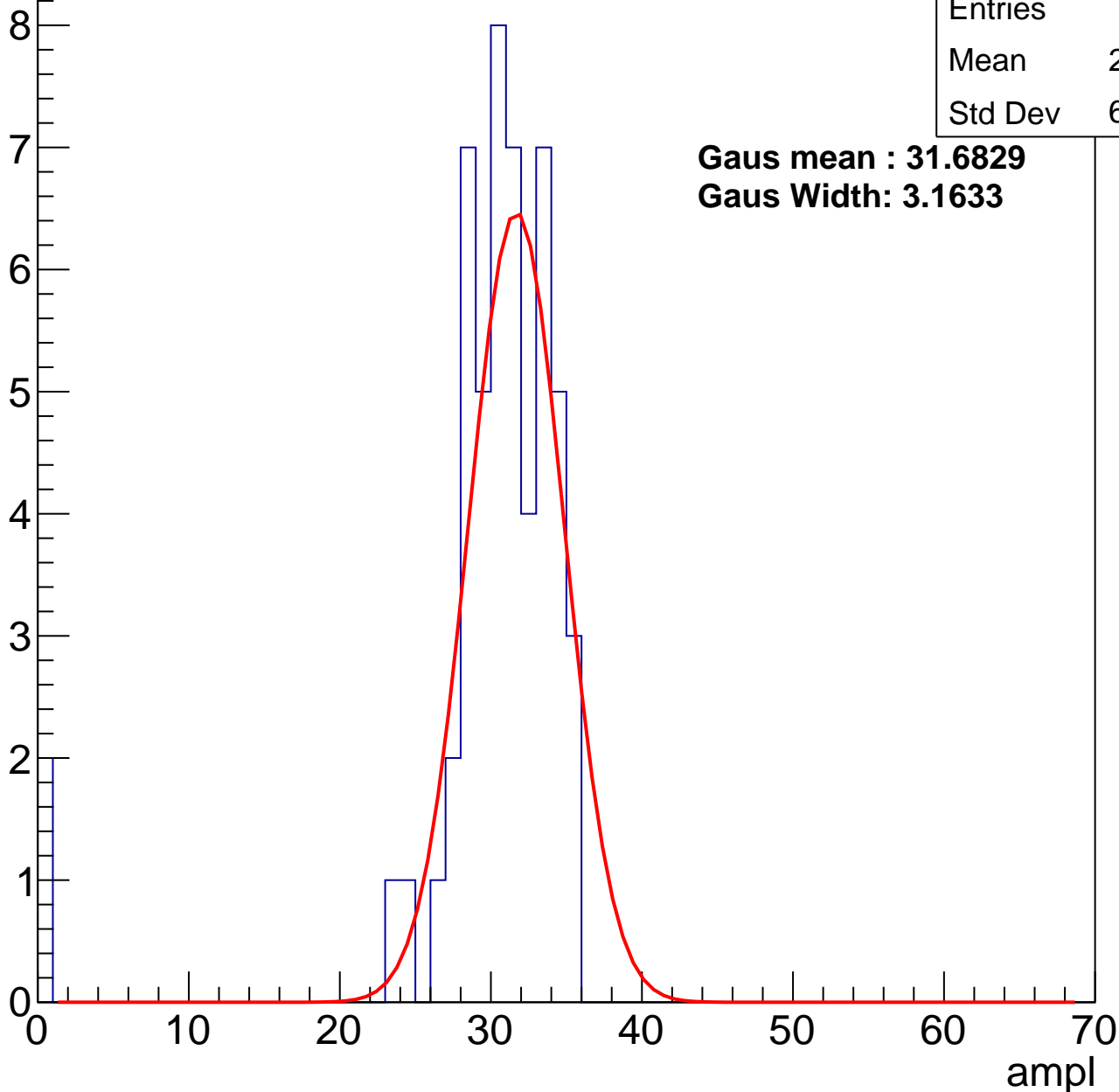
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	53
Mean	29.42
Std Dev	6.406

**Gaus mean : 31.6829**

**Gaus Width: 3.1633**



# B0L000S, U7-ch52, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

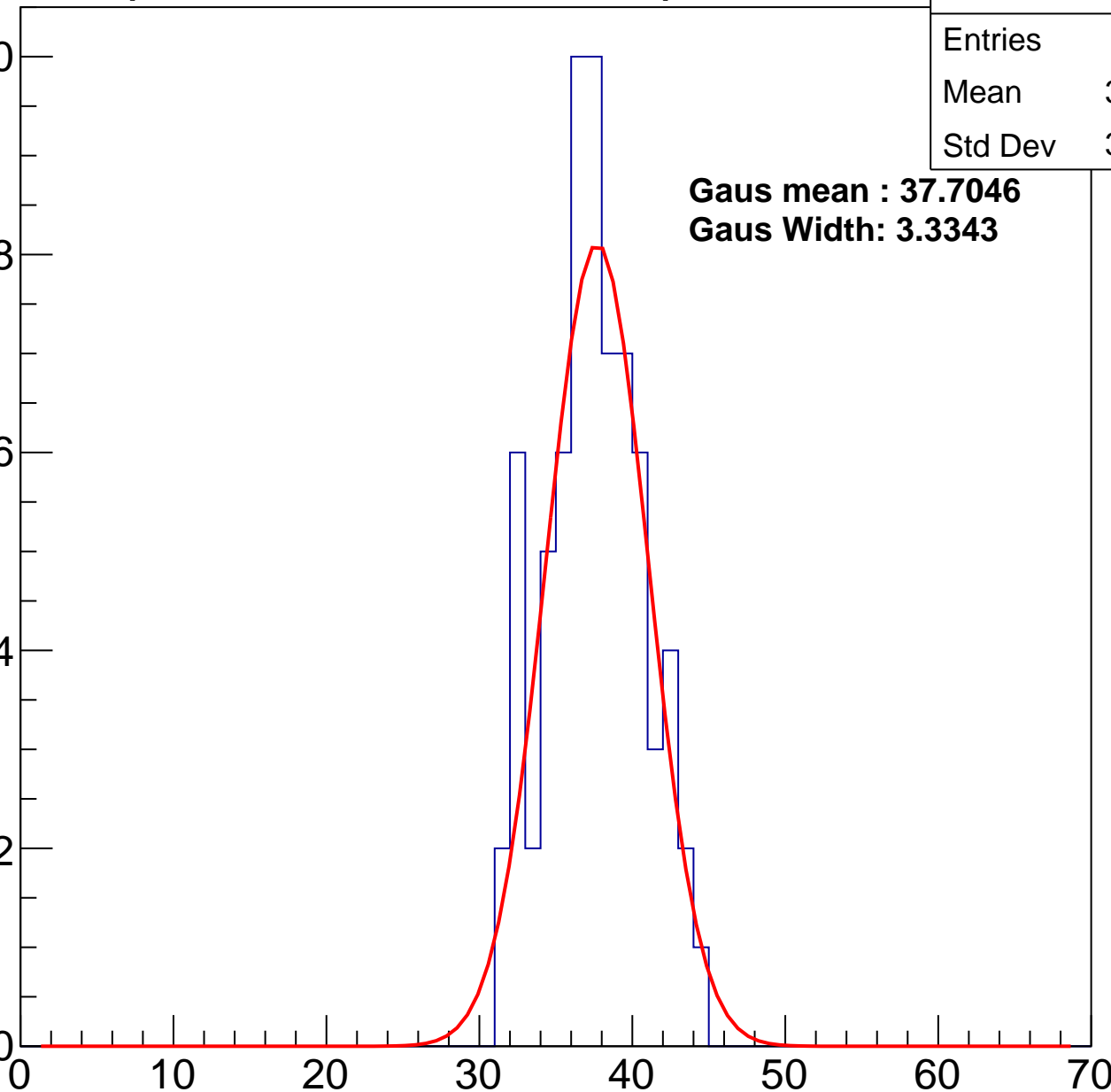
Entries	71
Mean	37.04
Std Dev	3.119

**Gaus mean : 37.7046**

**Gaus Width: 3.3343**

10  
8  
6  
4  
2  
0

ampl



# B0L000S, U7-ch52, adc2

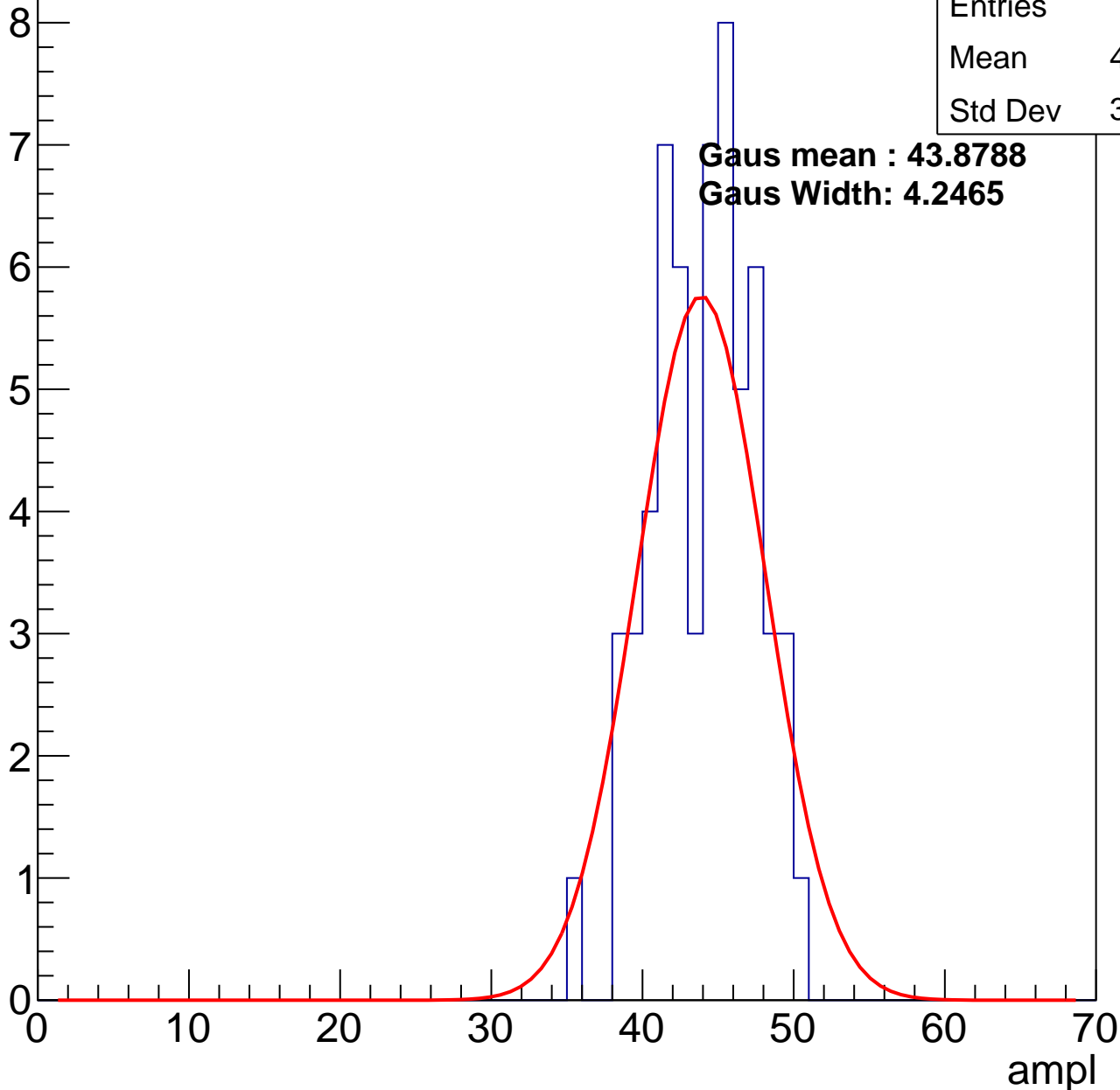
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	60
Mean	43.58
Std Dev	3.288

**Gaus mean : 43.8788**

**Gaus Width: 4.2465**

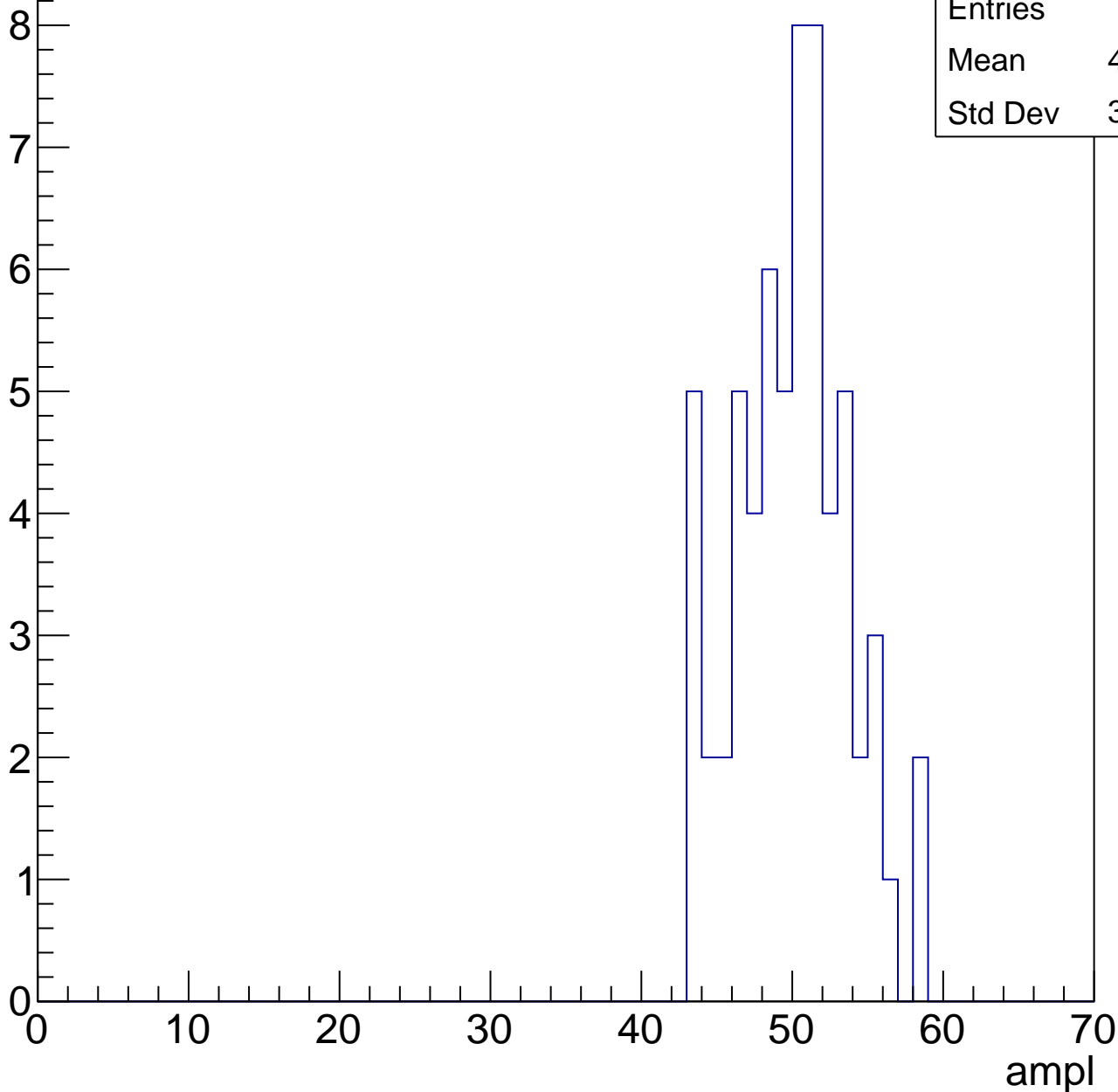


# B0L000S, U7-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

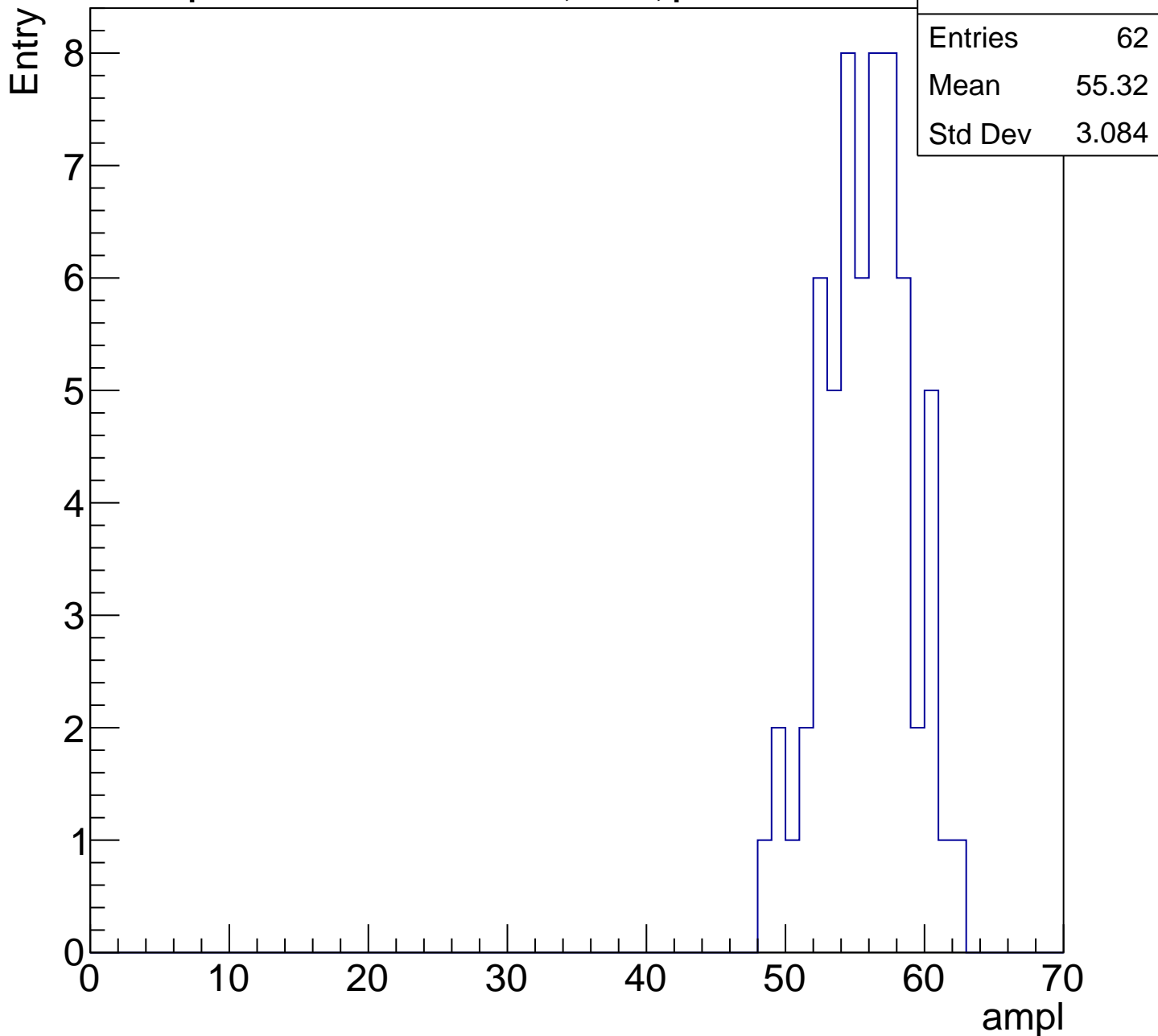
Entry

Entries	62
Mean	49.52
Std Dev	3.675



# B0L000S, U7-ch52, adc4

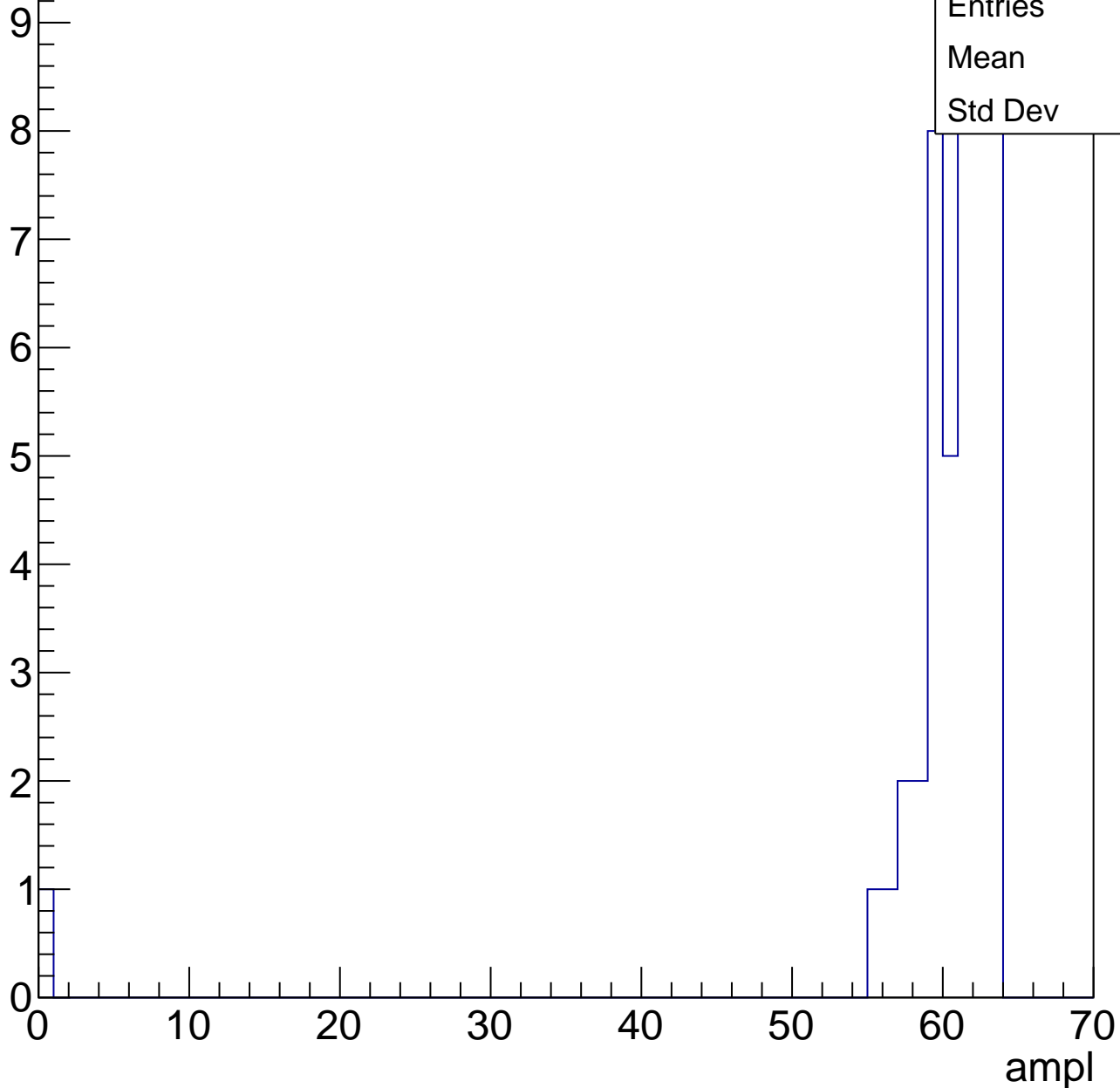
calib\_packv5\_042523\_0143.root, FC#5, port B1



# B0L000S, U7-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L000S, U7-ch53, adc0

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	71
Mean	30.27
Std Dev	4.959

**Gaus mean : 30.4270**

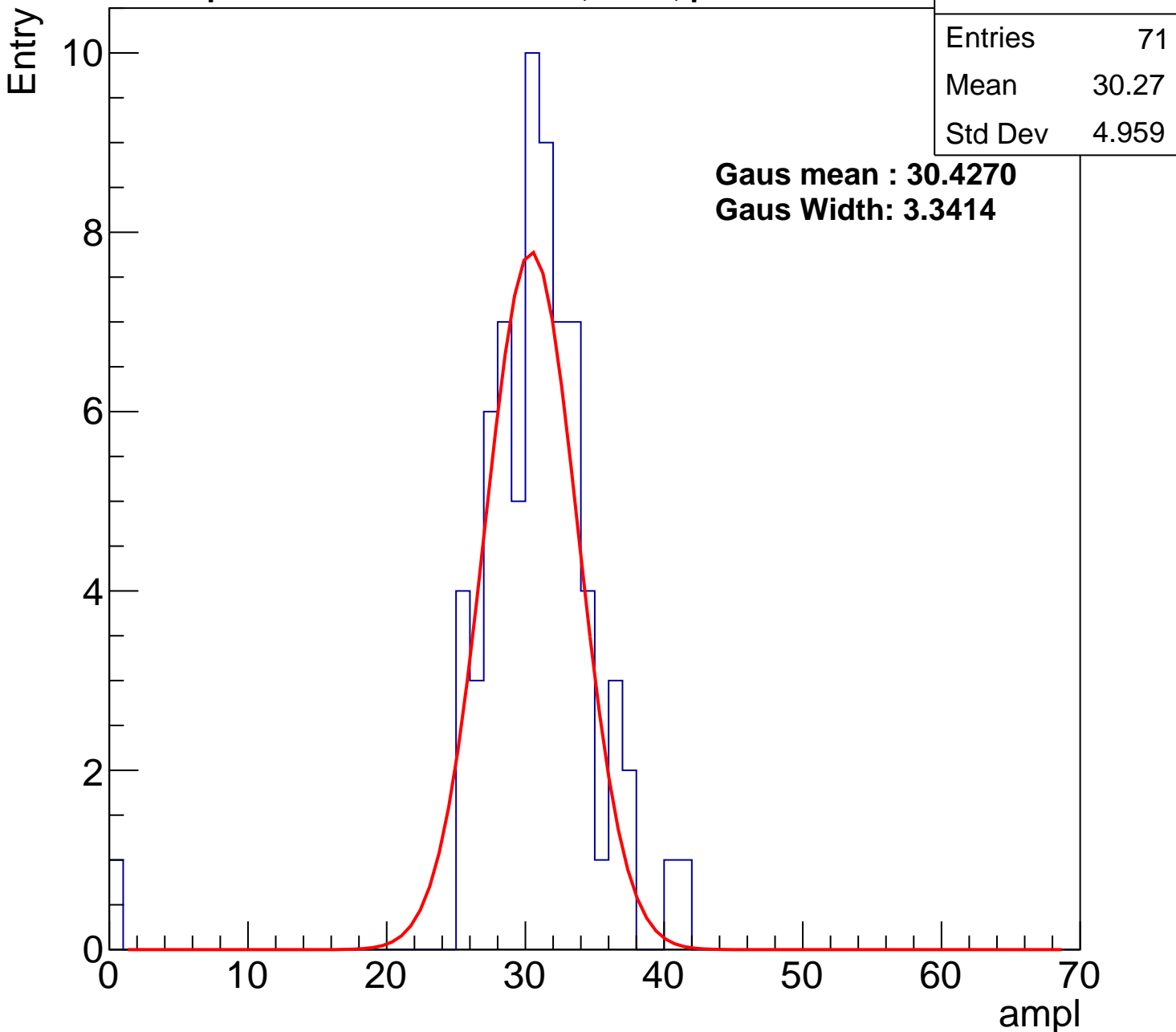
**Gaus Width: 3.3414**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

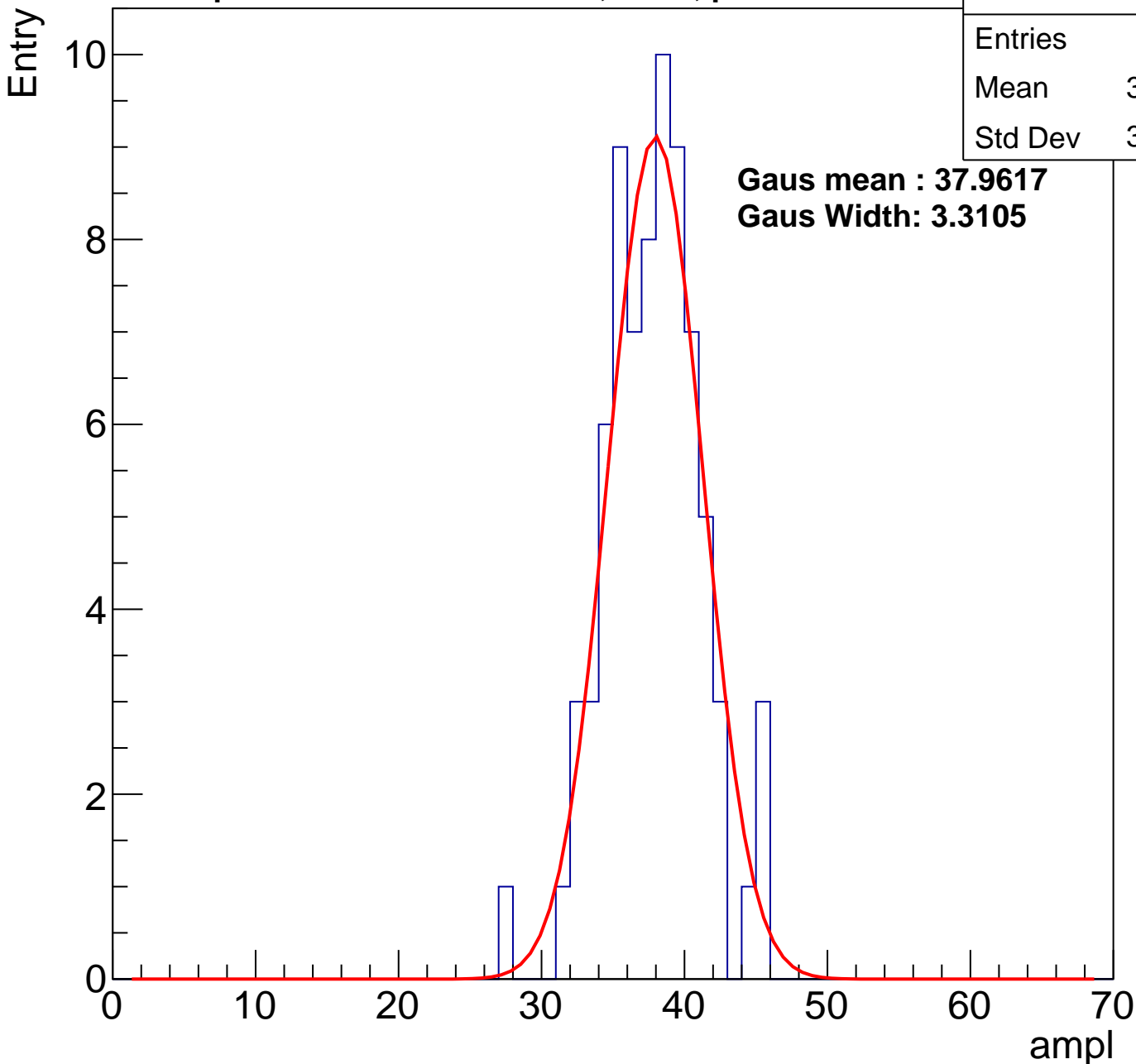


# B0L000S, U7-ch53, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	76
Mean	37.38
Std Dev	3.344

**Gaus mean : 37.9617**  
**Gaus Width: 3.3105**



# B0L000S, U7-ch53, adc2

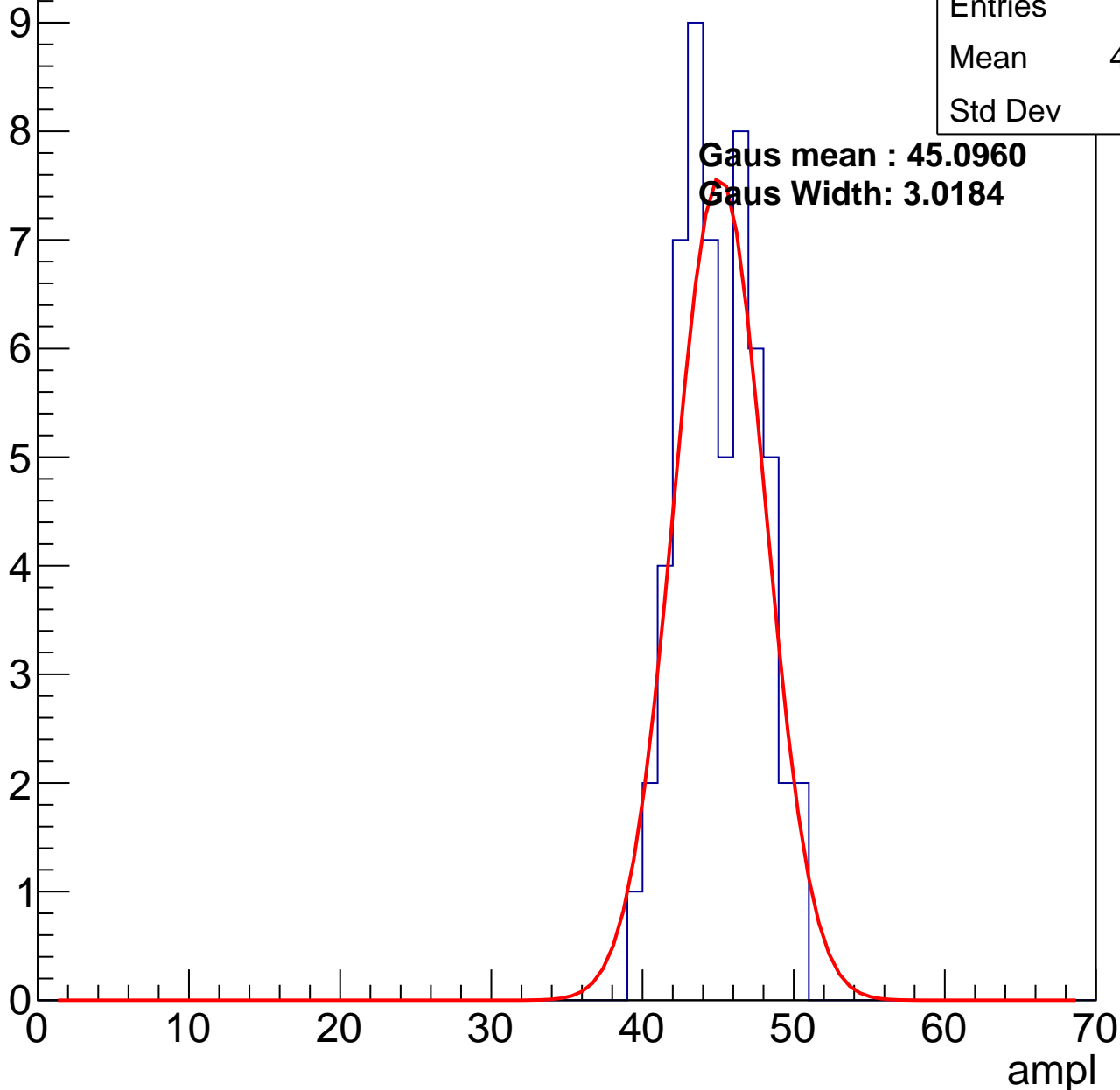
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	58
Mean	44.57
Std Dev	2.64

**Gaus mean : 45.0960**

**Gaus Width: 3.0184**

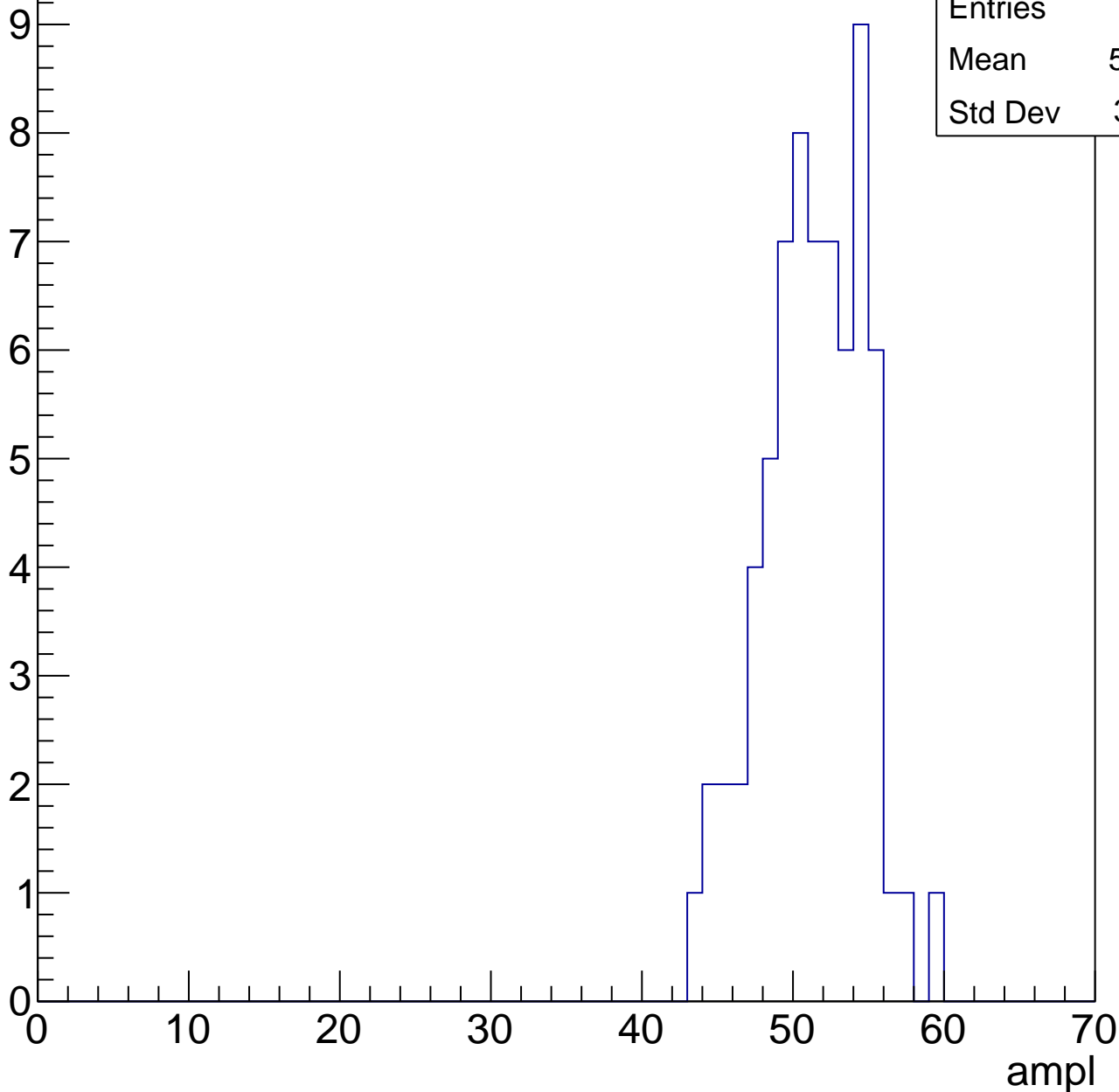


# B0L000S, U7-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	69
Mean	50.88
Std Dev	3.321

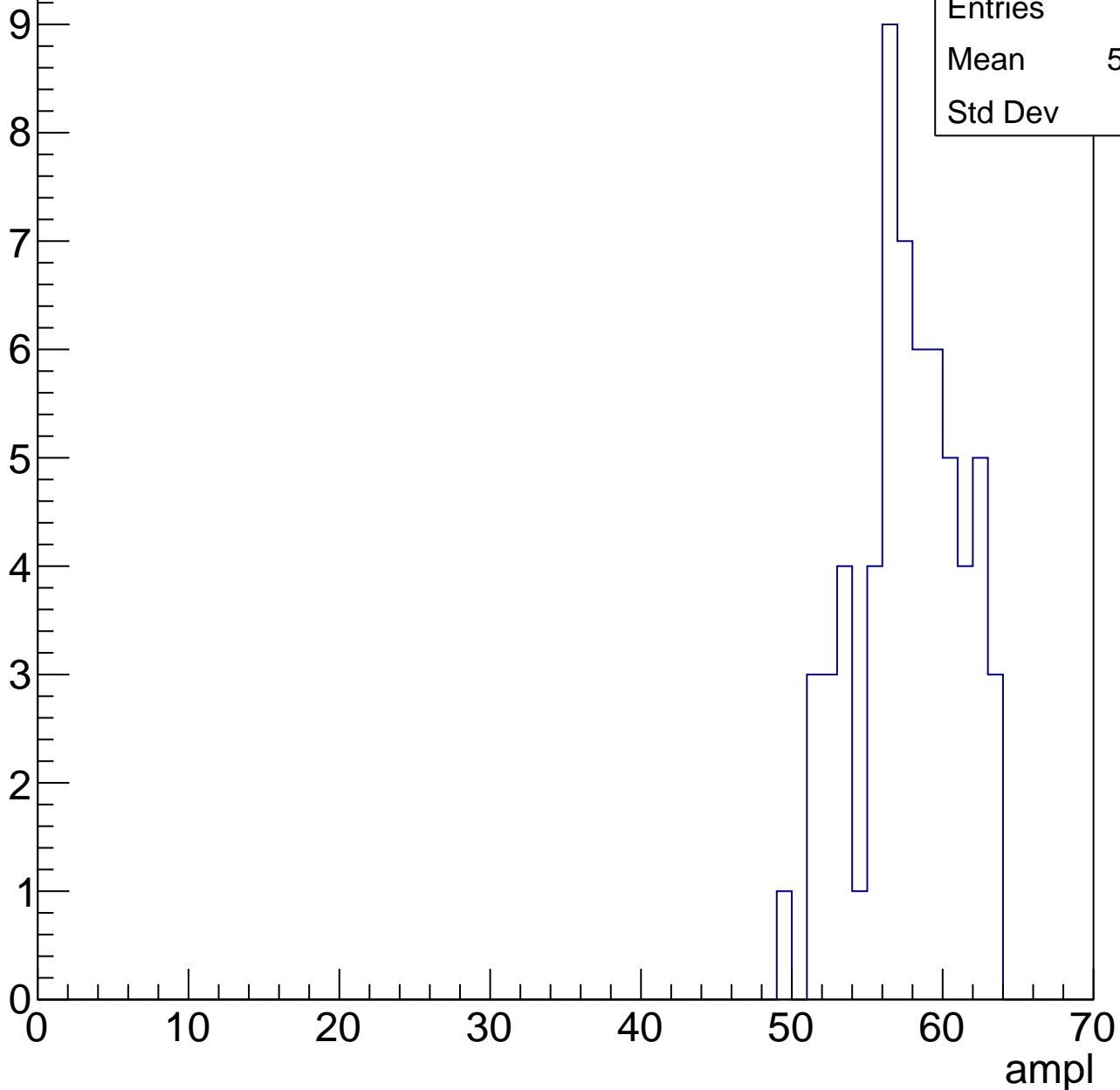


# B0L000S, U7-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

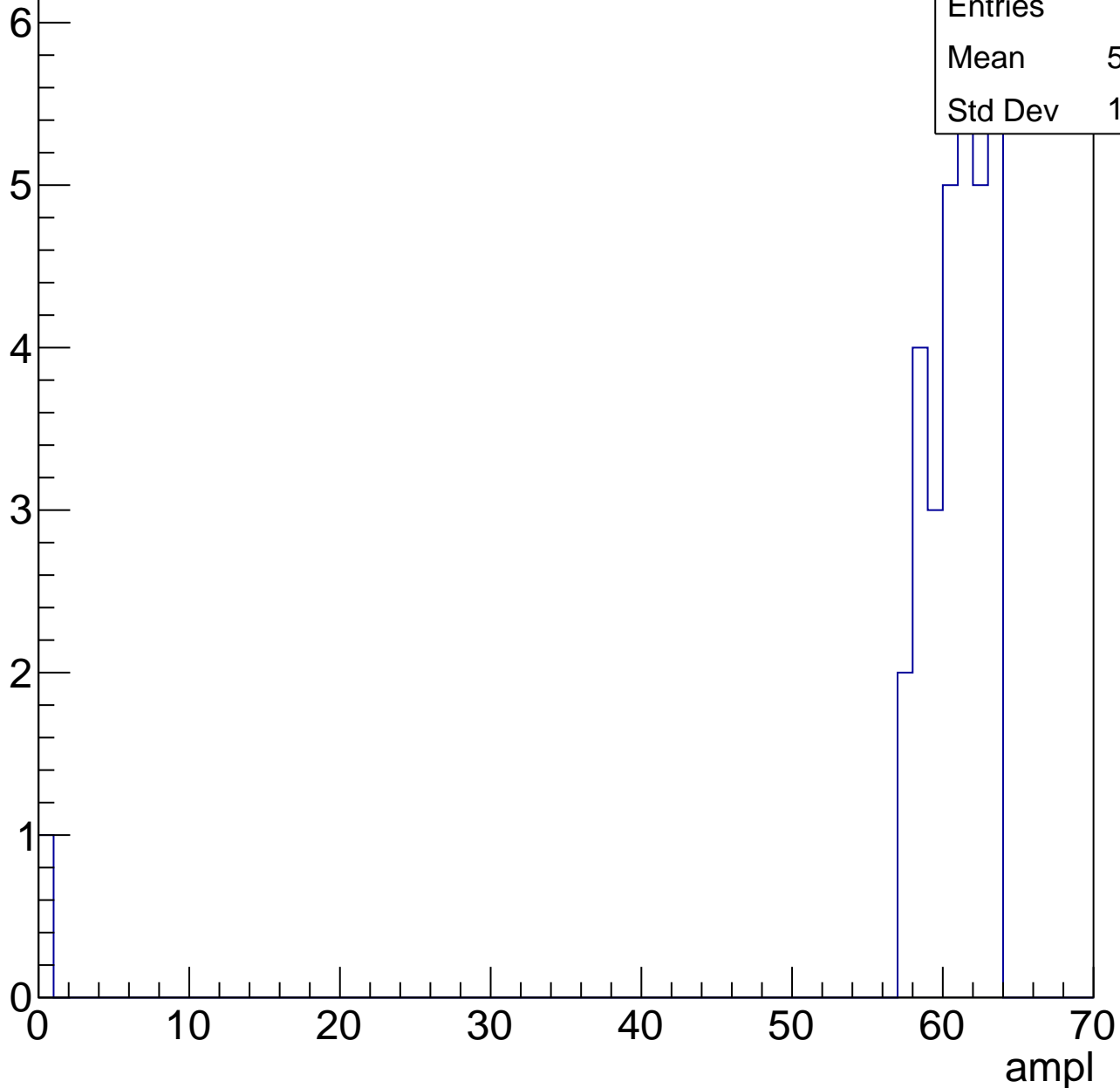
Entries	61
Mean	57.25
Std Dev	3.42



# B0L000S, U7-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch54, adc0

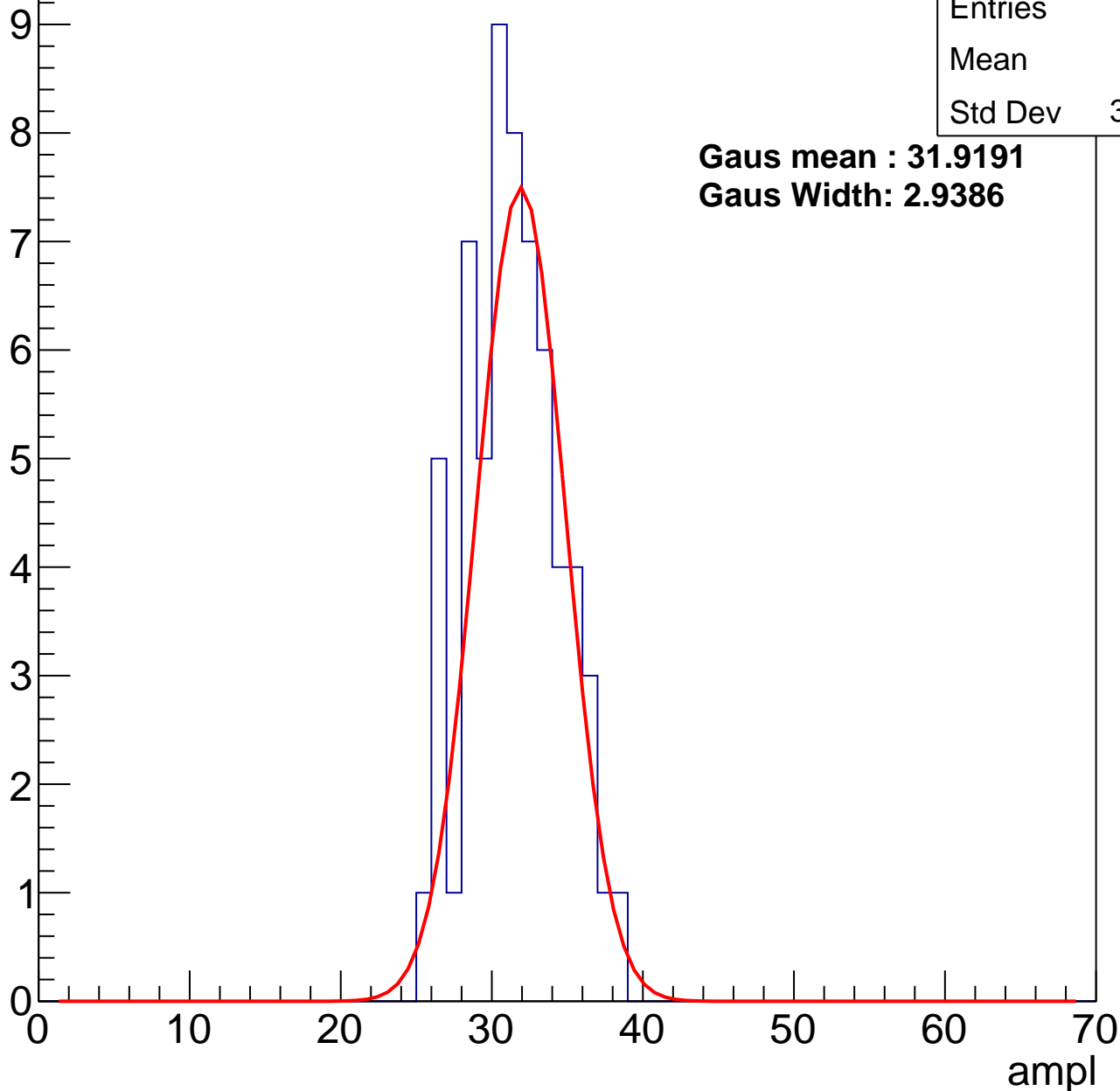
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	62
Mean	31
Std Dev	3.005

**Gaus mean : 31.9191**

**Gaus Width: 2.9386**



# B0L000S, U7-ch54, adc1

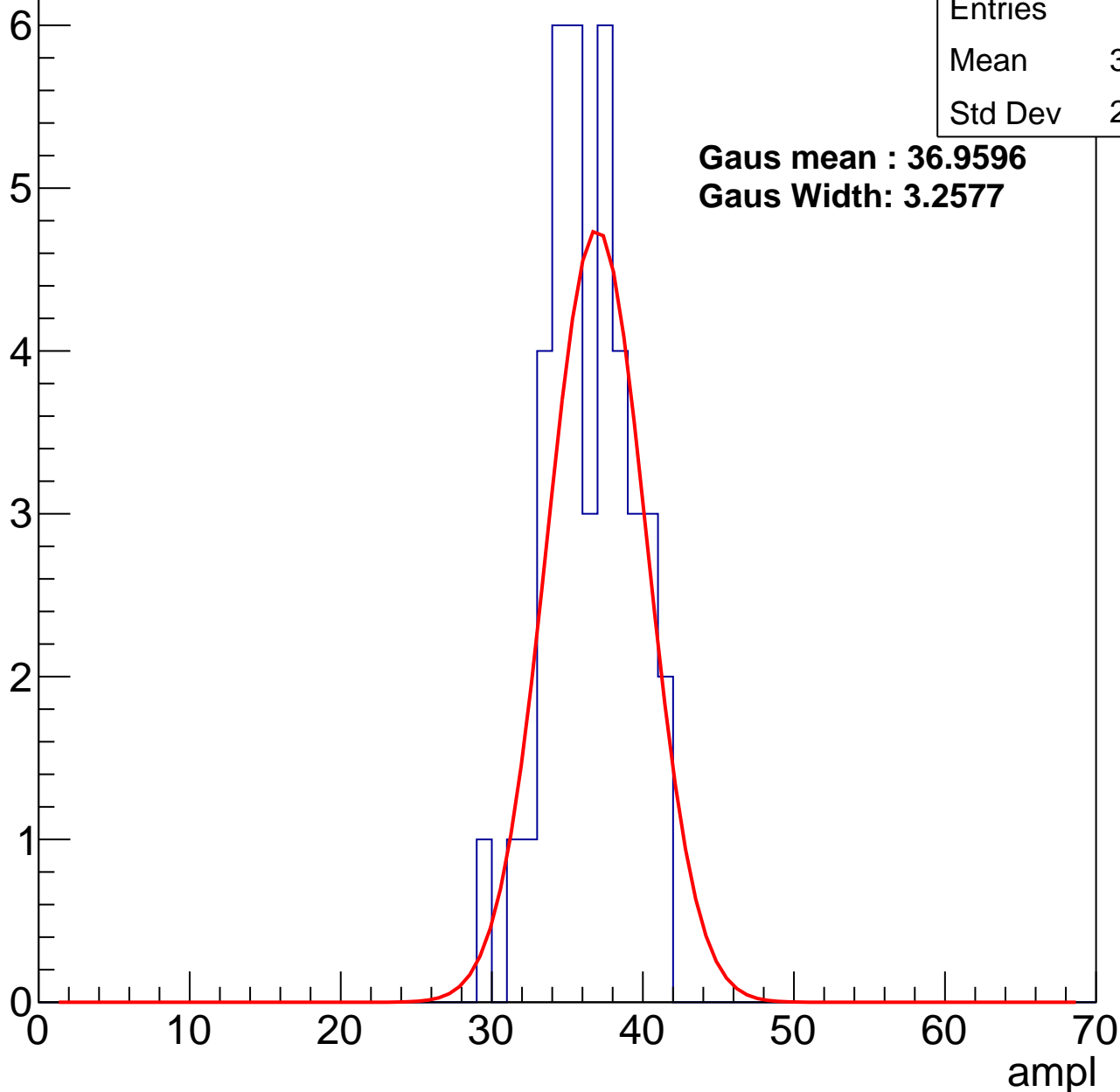
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	40
Mean	35.98
Std Dev	2.752

**Gaus mean : 36.9596**

**Gaus Width: 3.2577**



# B0L000S, U7-ch54, adc2

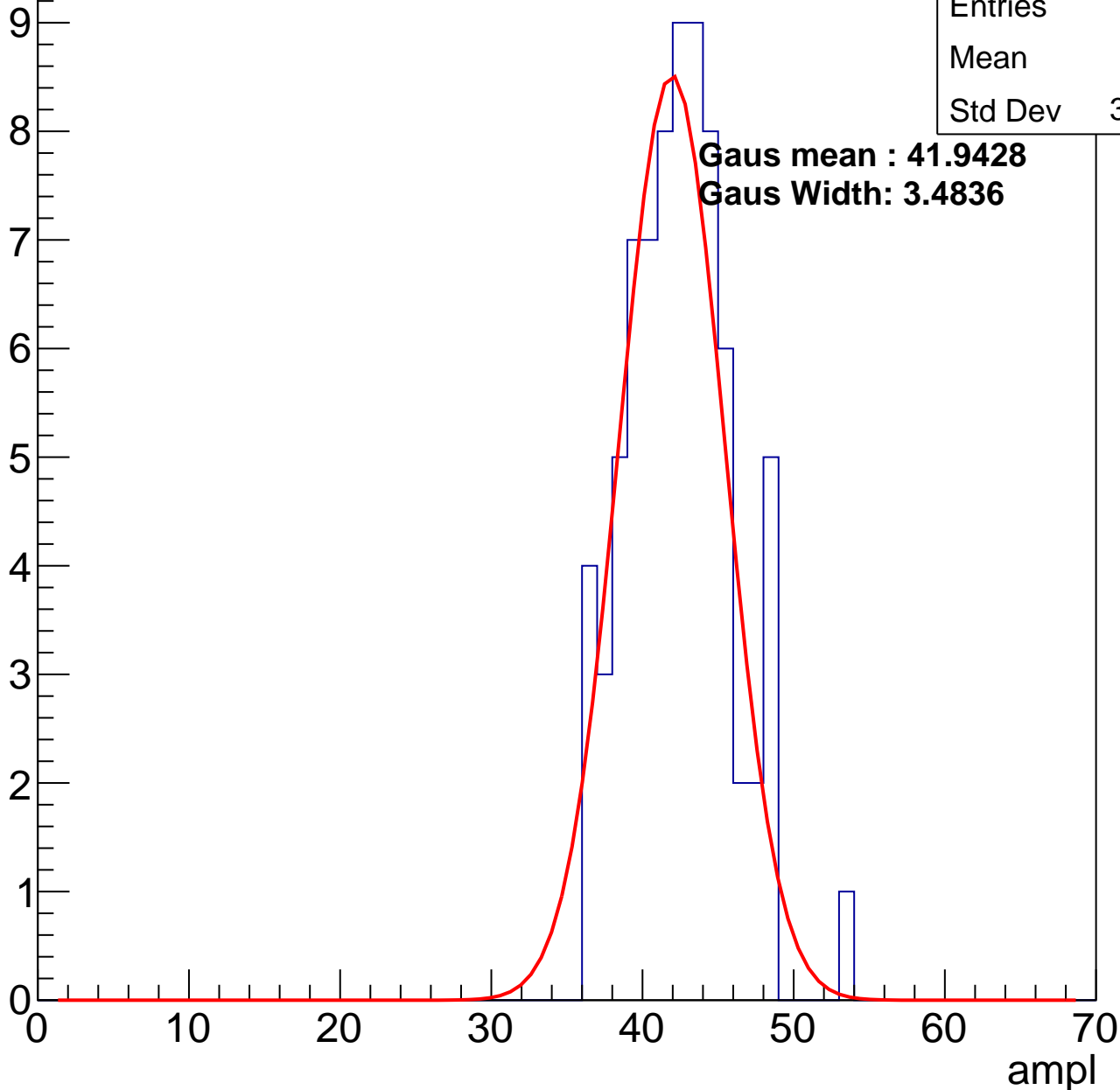
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	76
Mean	42
Std Dev	3.395

**Gaus mean : 41.9428**

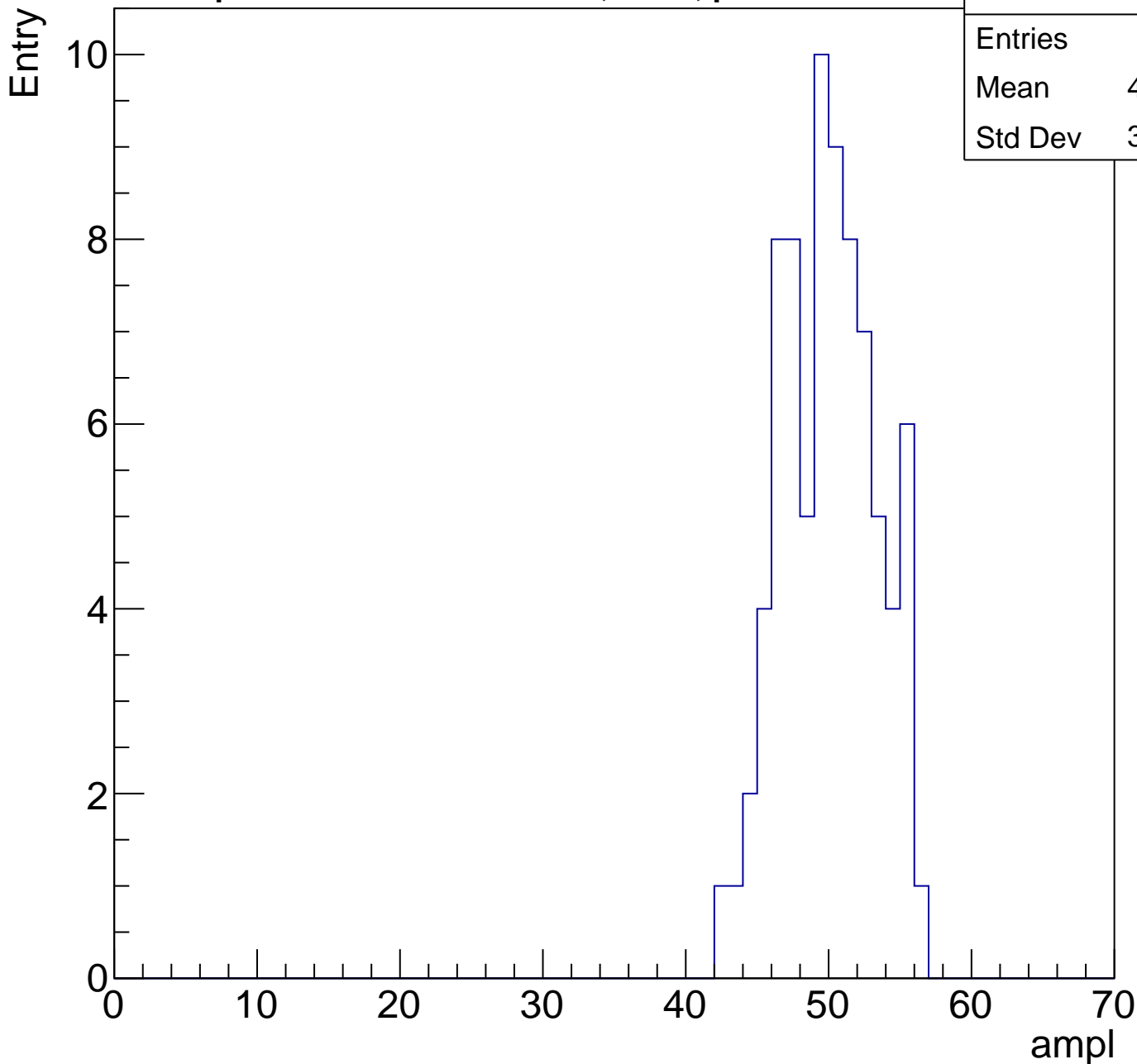
**Gaus Width: 3.4836**



# B0L000S, U7-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	79
Mean	49.57
Std Dev	3.244

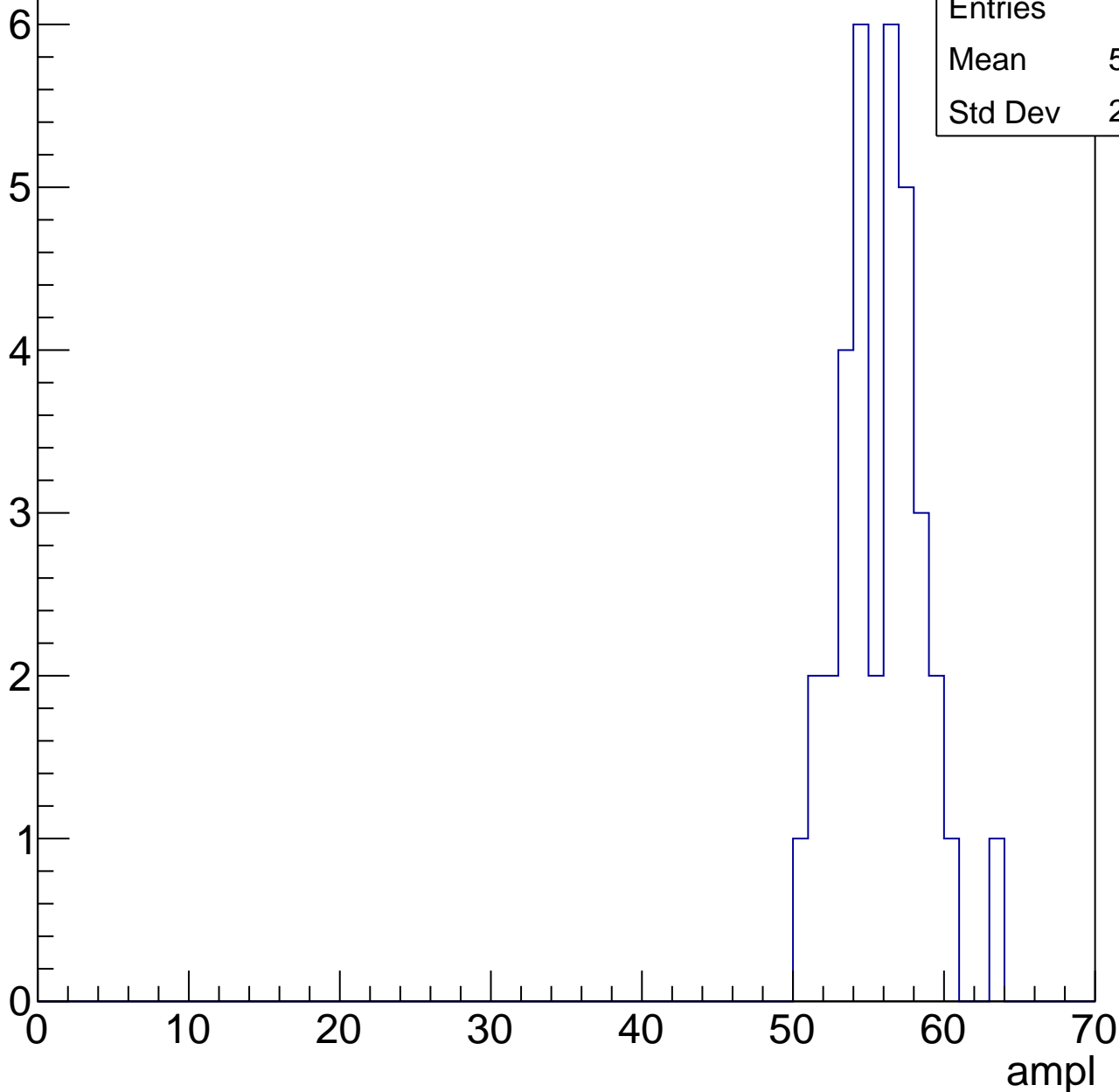


# B0L000S, U7-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	35
Mean	55.37
Std Dev	2.758



# B0L000S, U7-ch54, adc5

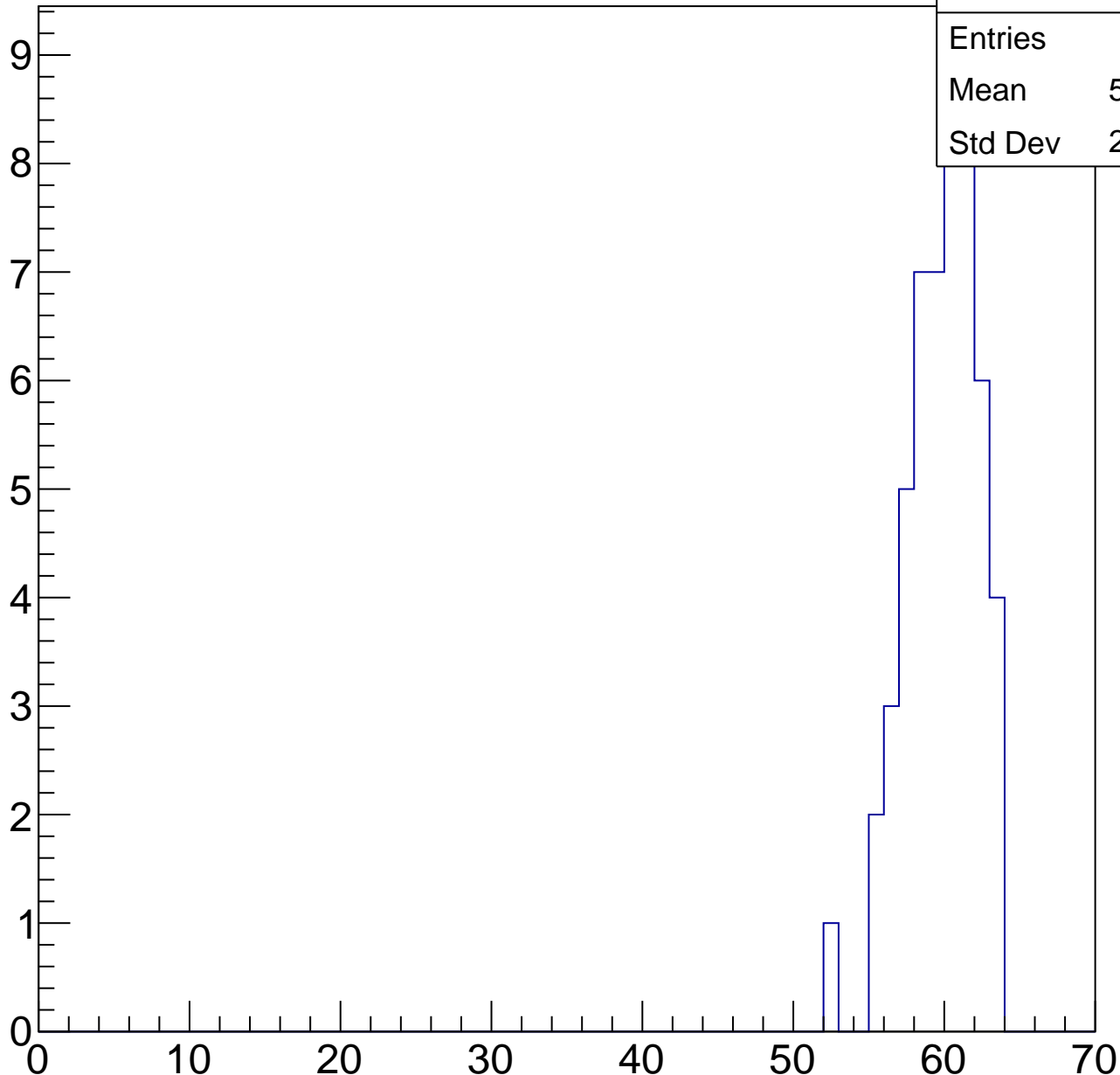
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	52
Mean	59.37
Std Dev	2.362

ampl

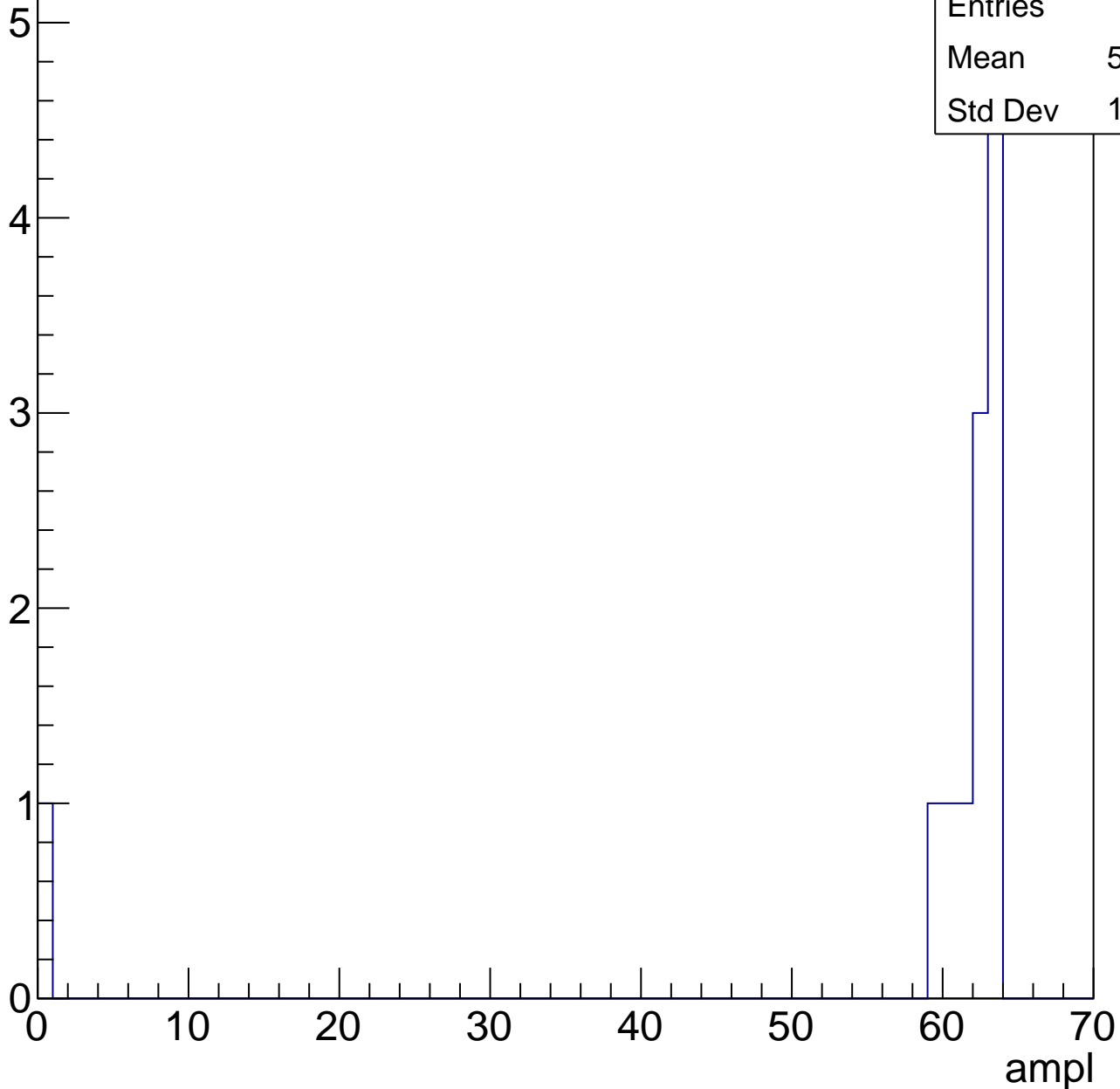


# B0L000S, U7-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	12
Mean	56.75
Std Dev	17.16

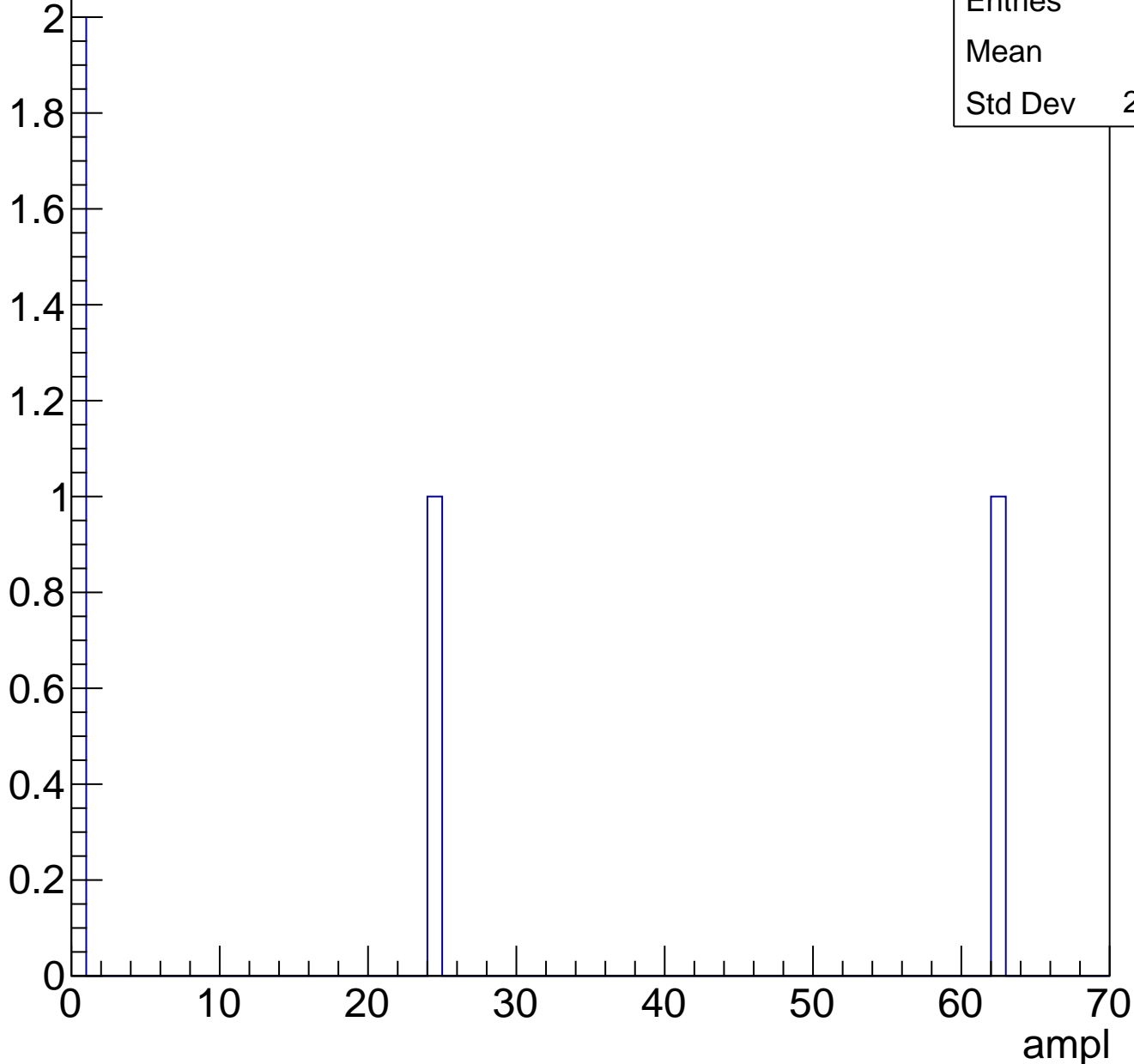




# B0L000S, U7-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	4
Mean	21.5
Std Dev	25.35

# B0L000S, U7-ch55, adc0

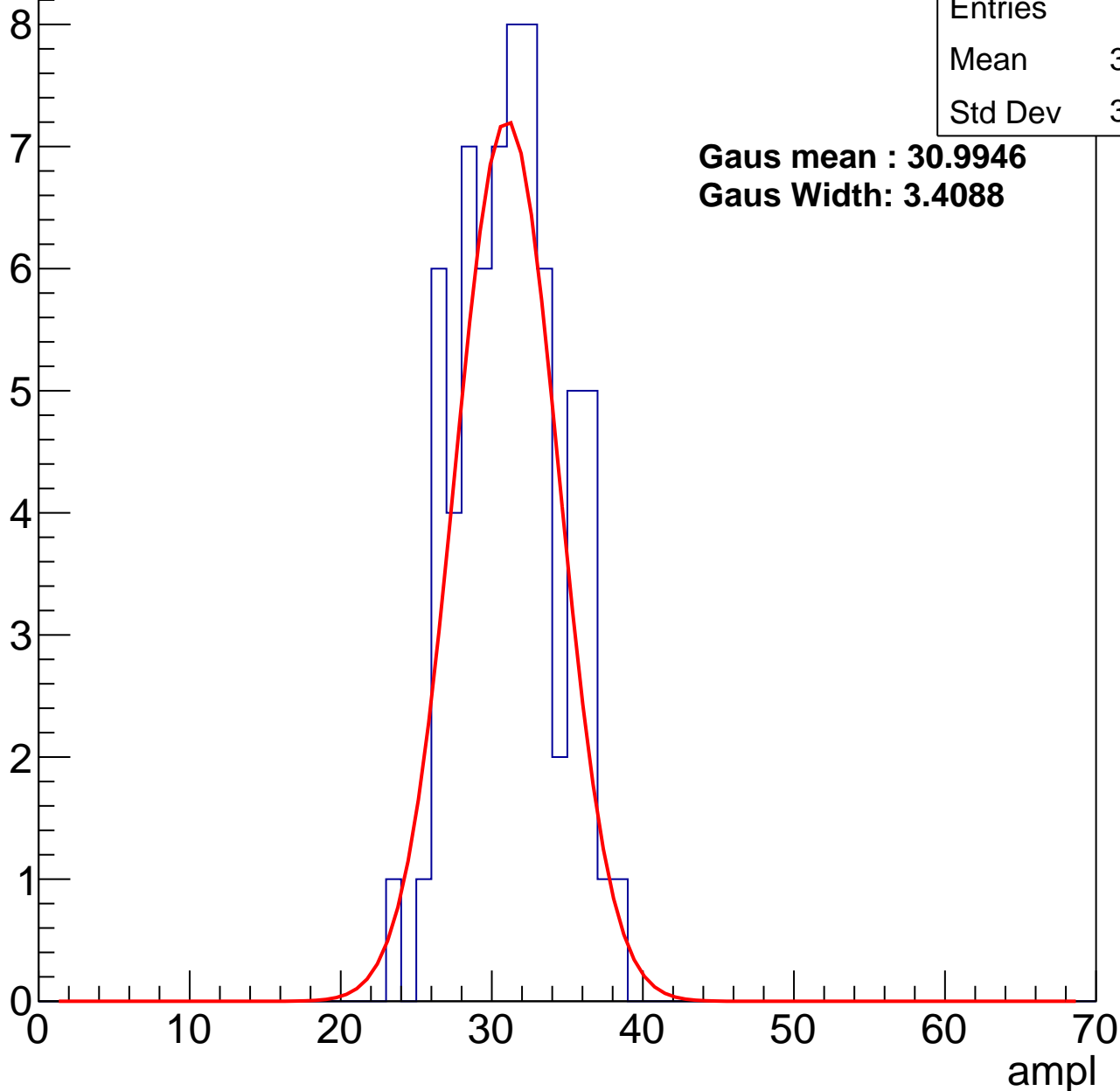
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	68
Mean	30.76
Std Dev	3.308

**Gaus mean : 30.9946**

**Gaus Width: 3.4088**



# B0L000S, U7-ch55, adc1

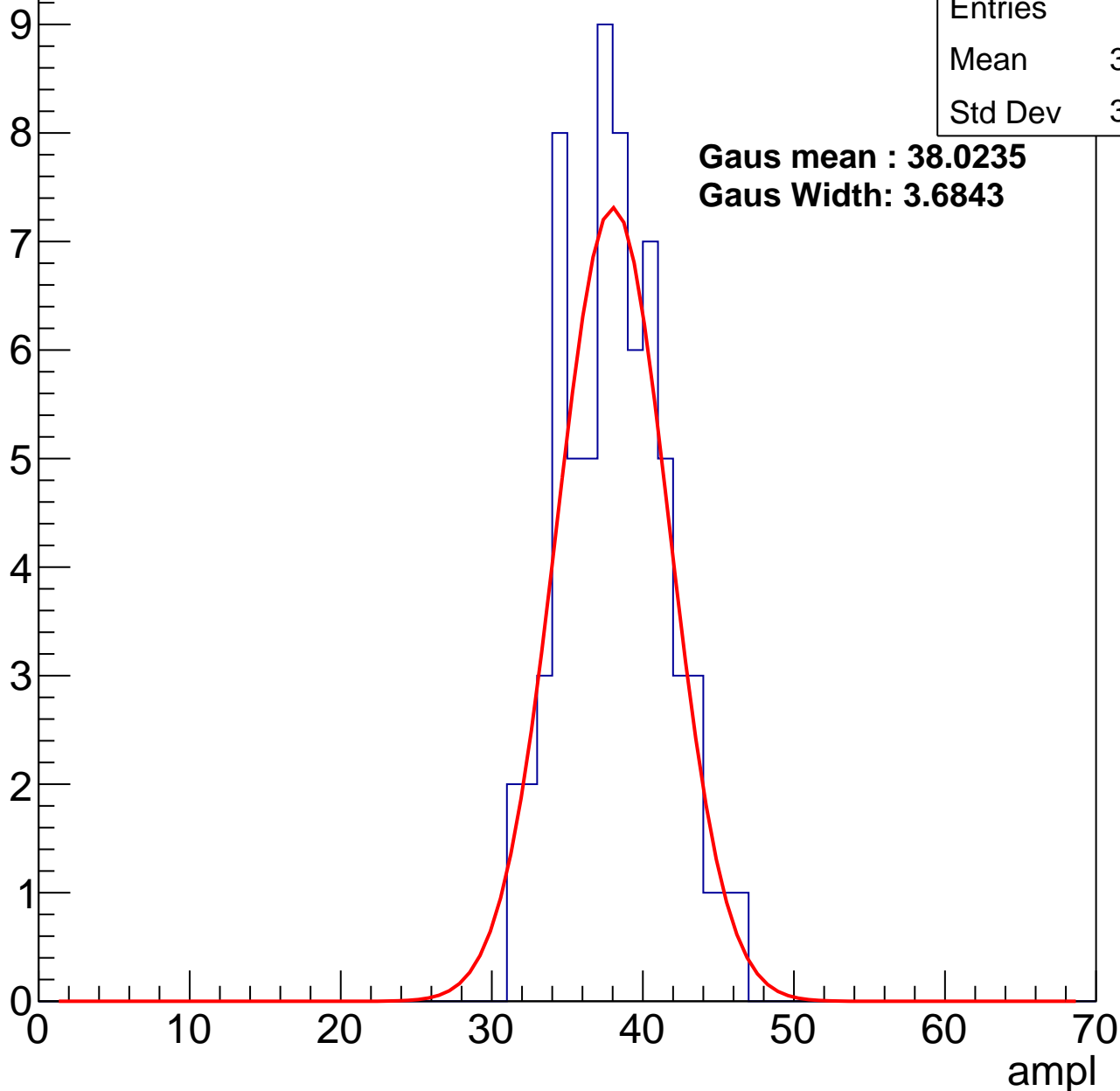
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	69
Mean	37.65
Std Dev	3.383

**Gaus mean : 38.0235**

**Gaus Width: 3.6843**



# B0L000S, U7-ch55, adc2

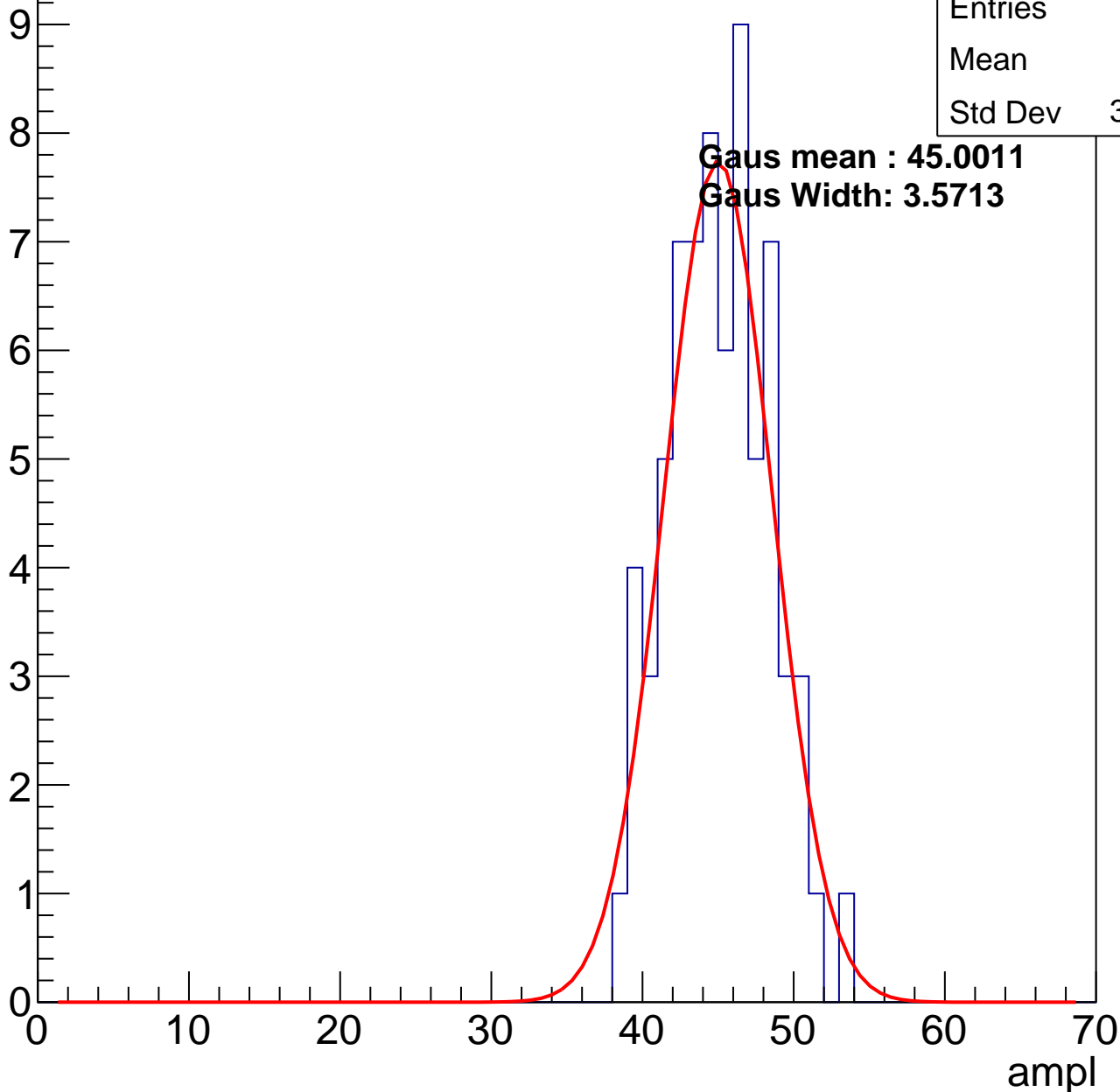
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	70
Mean	44.6
Std Dev	3.275

**Gaus mean : 45.0011**

**Gaus Width: 3.5713**

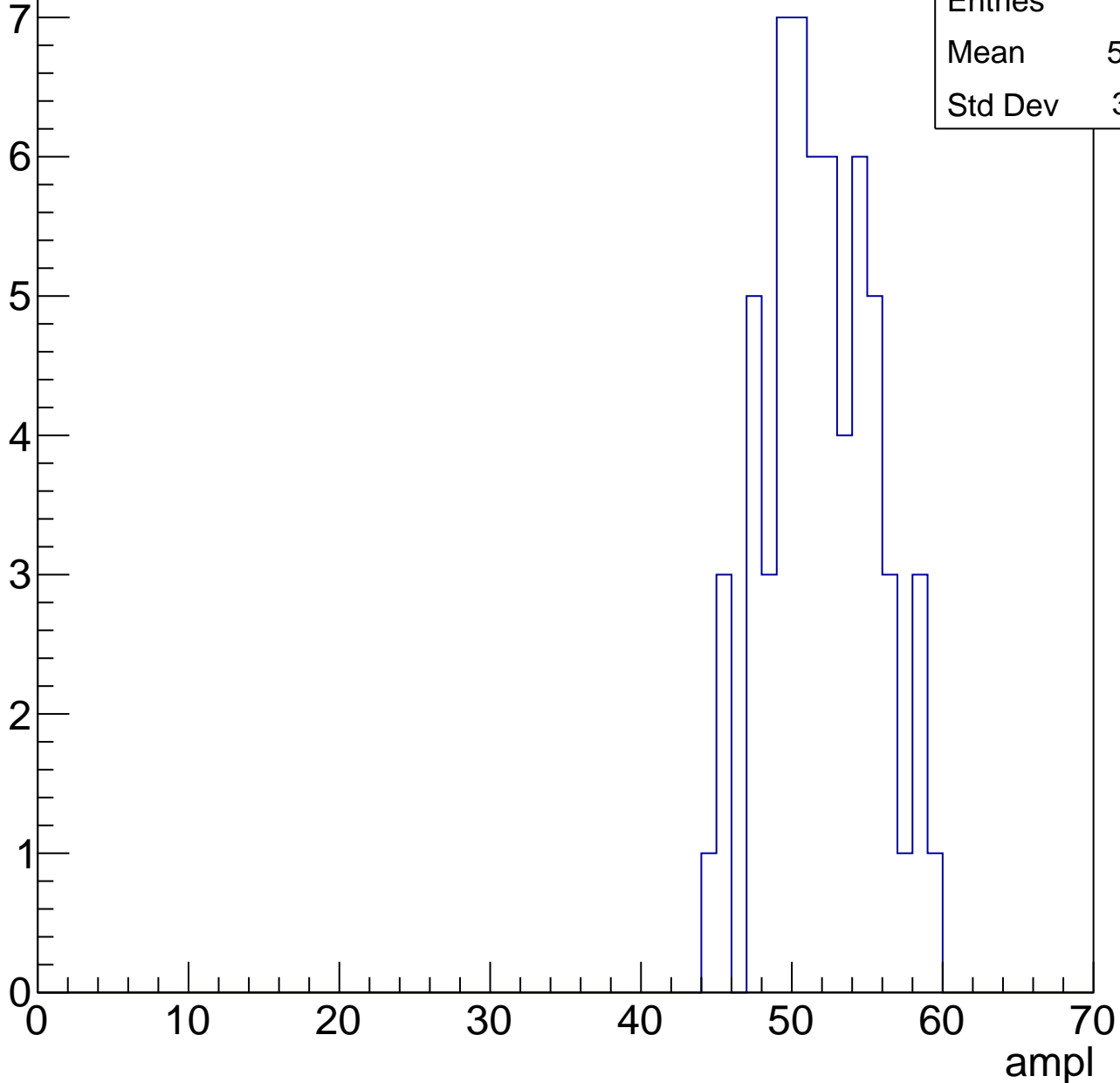


# B0L000S, U7-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

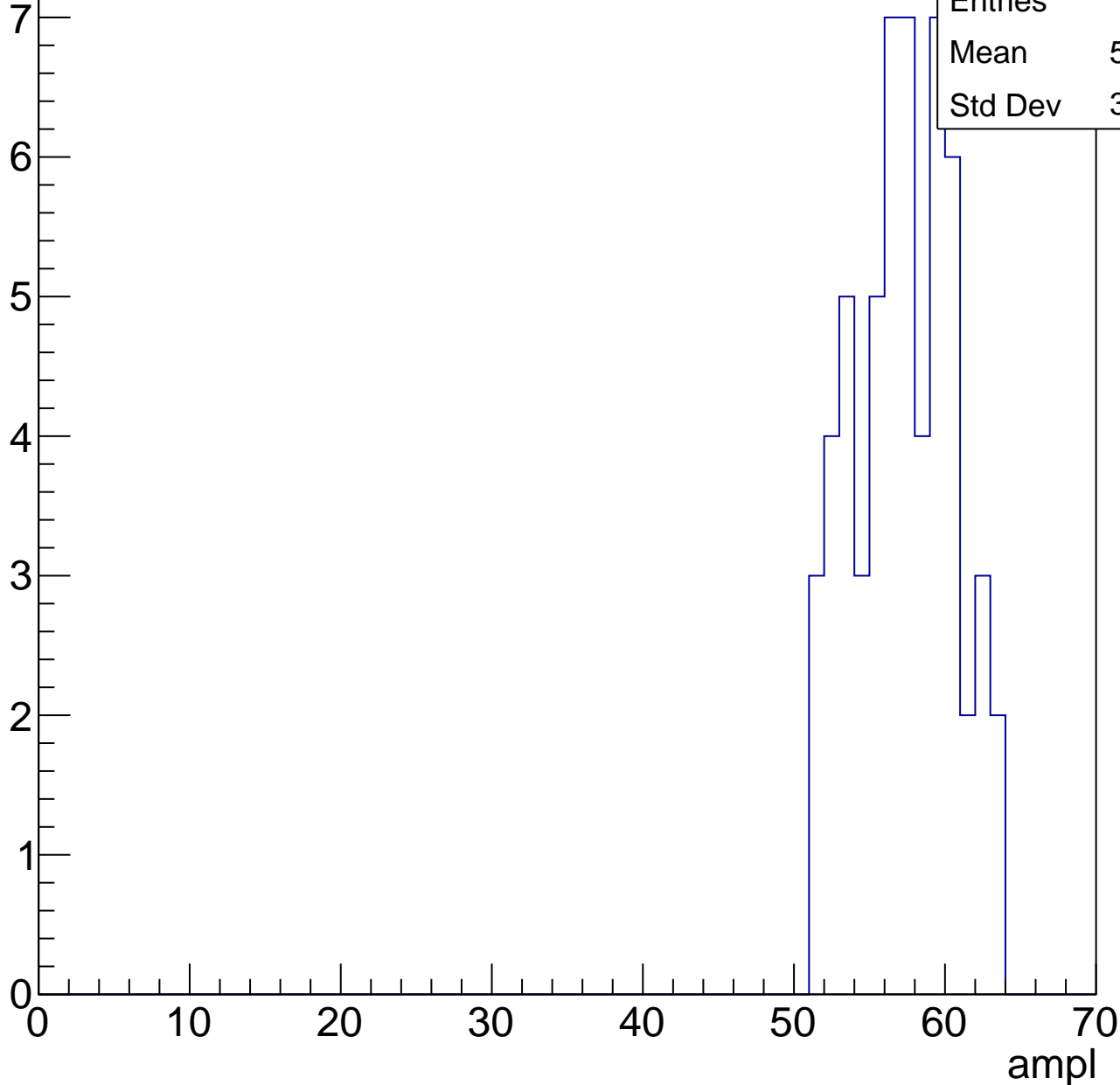
Entries	61
Mean	51.44
Std Dev	3.541



# B0L000S, U7-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

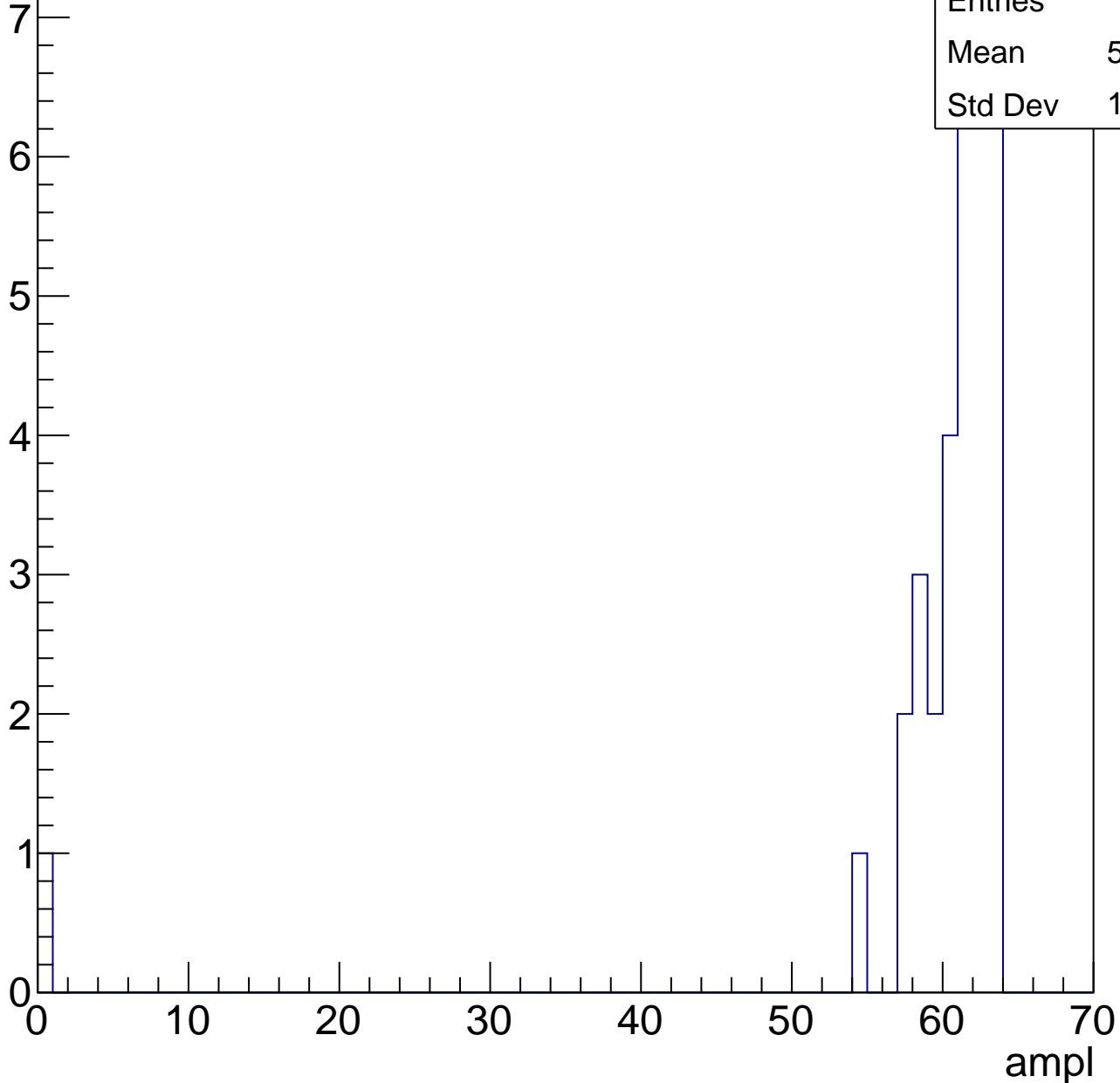


# B0L000S, U7-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	34
Mean	58.88
Std Dev	10.46



# B0L000S, U7-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L000S, U7-ch56, adc0

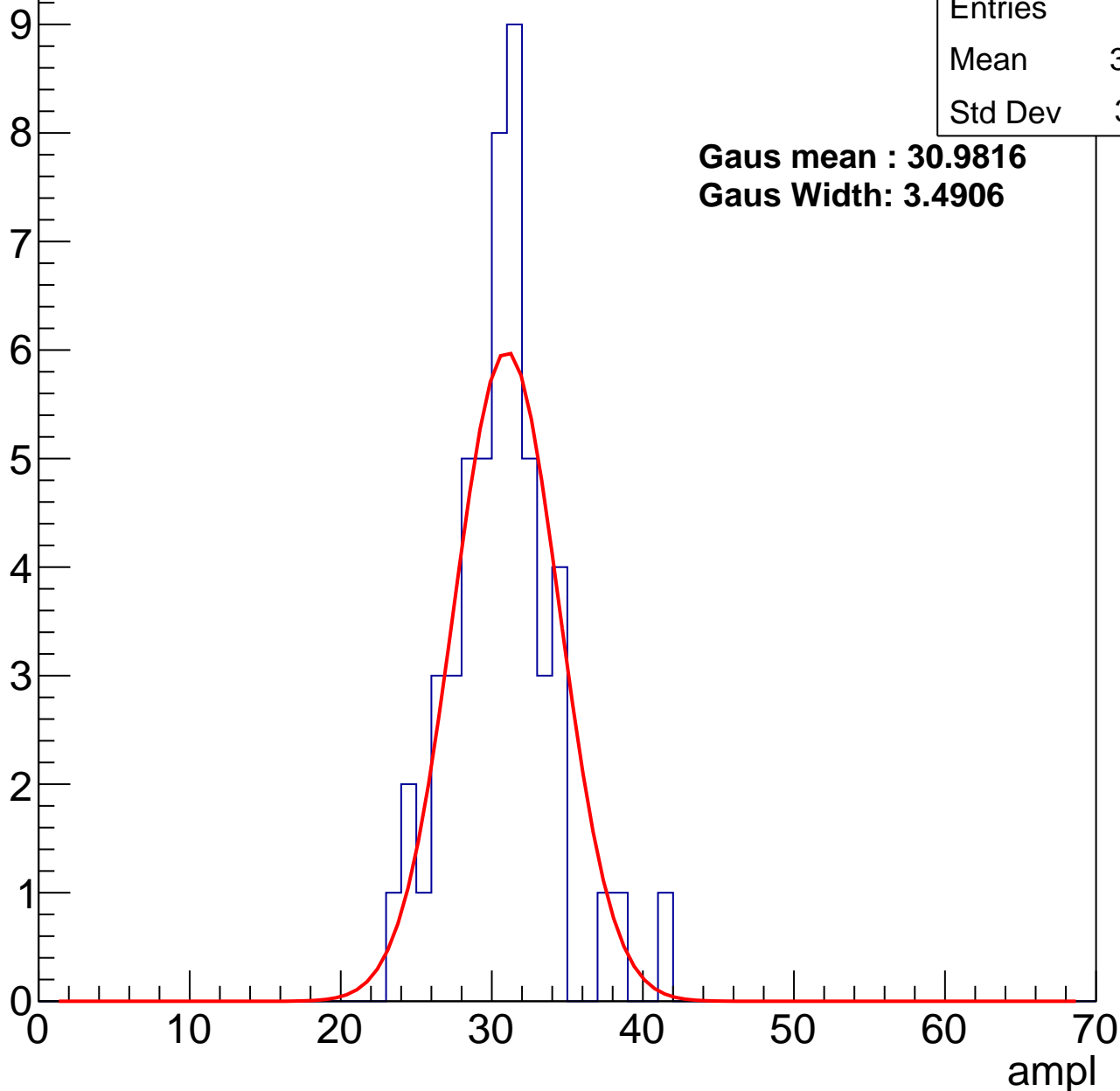
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	52
Mean	30.19
Std Dev	3.391

**Gaus mean : 30.9816**

**Gaus Width: 3.4906**



# B0L000S, U7-ch56, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	88
Mean	37.5
Std Dev	3.757

**Gaus mean : 37.6962**

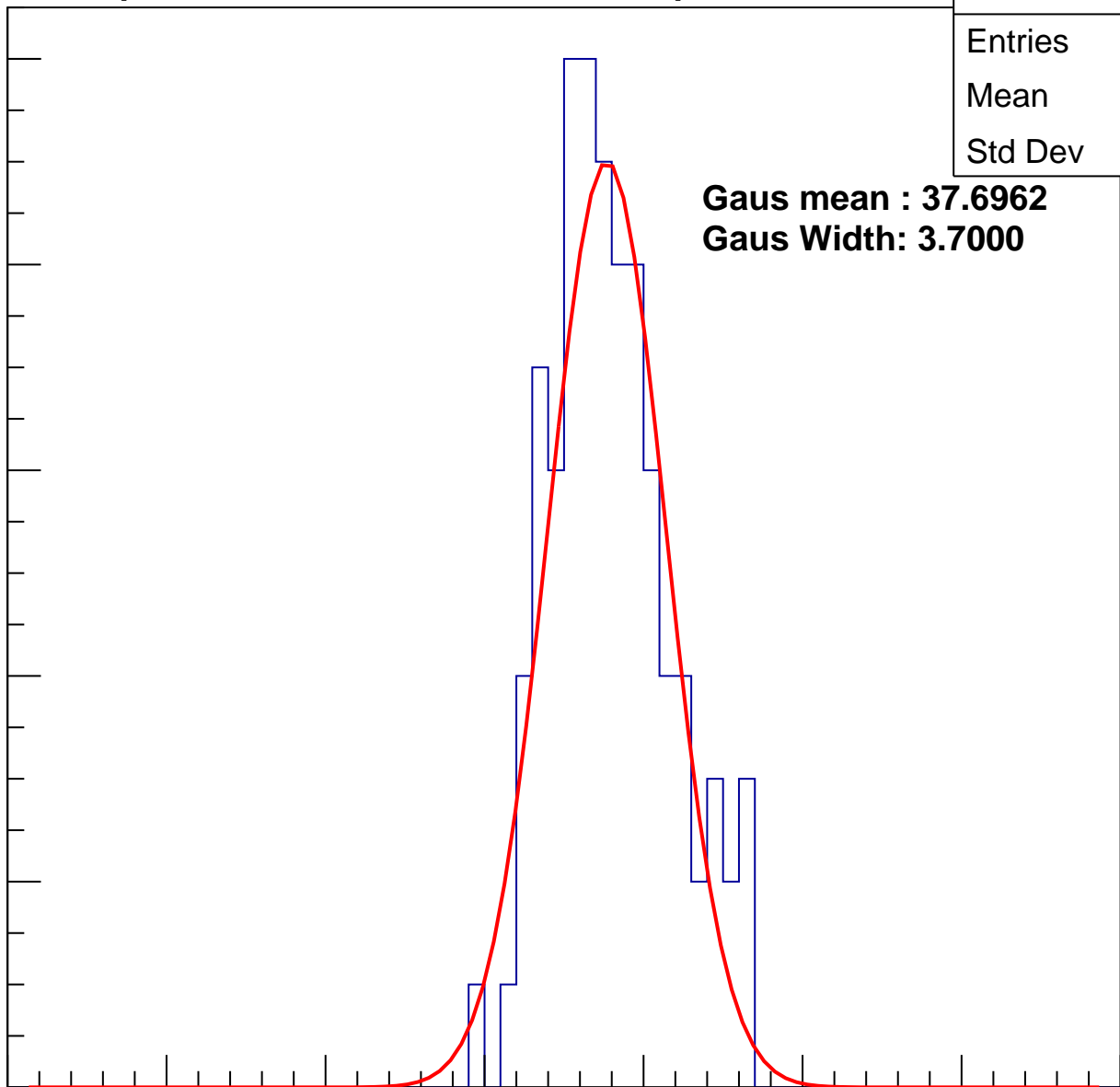
**Gaus Width: 3.7000**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L000S, U7-ch56, adc2

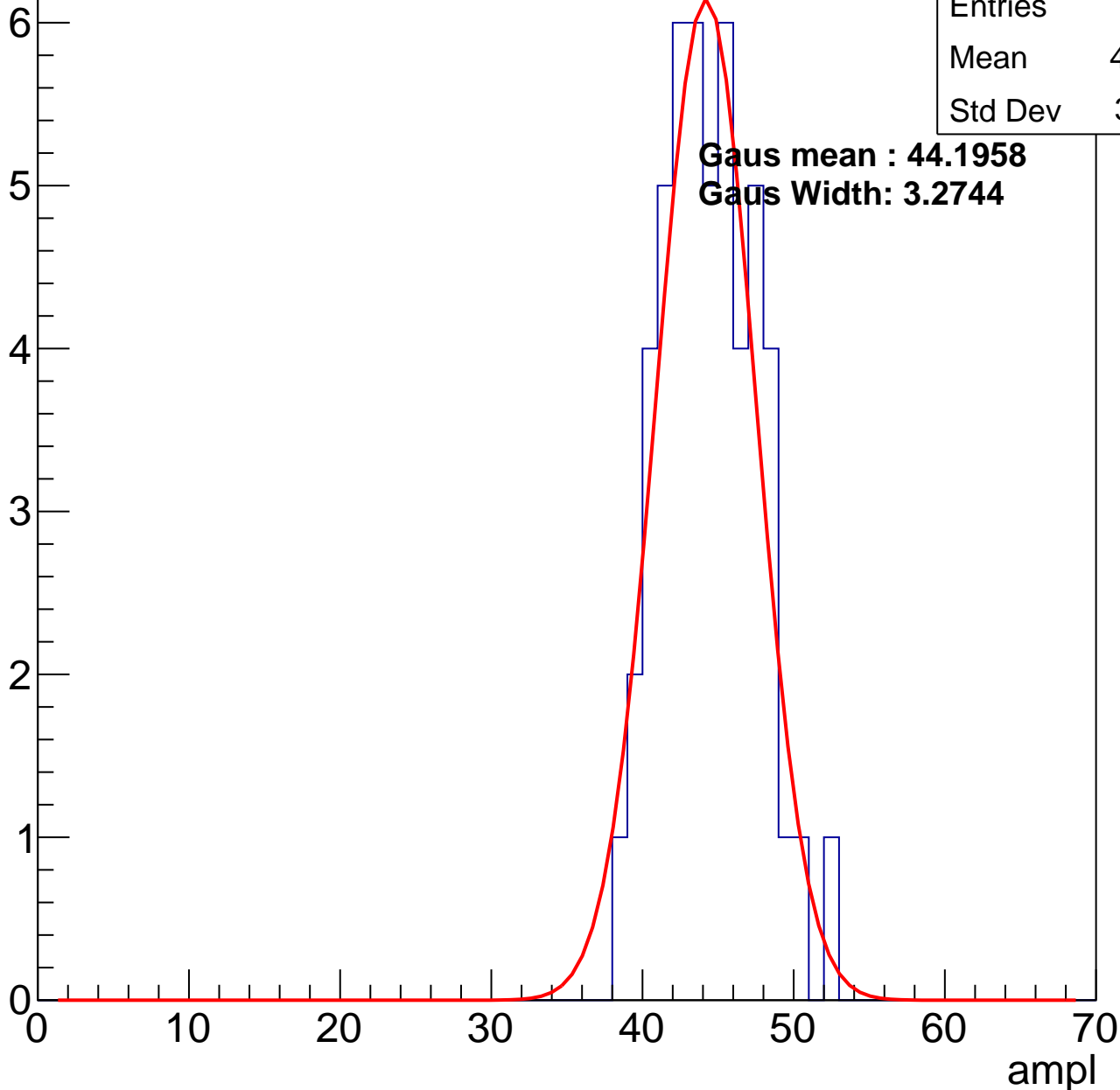
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	51
Mean	43.98
Std Dev	3.071

**Gaus mean : 44.1958**

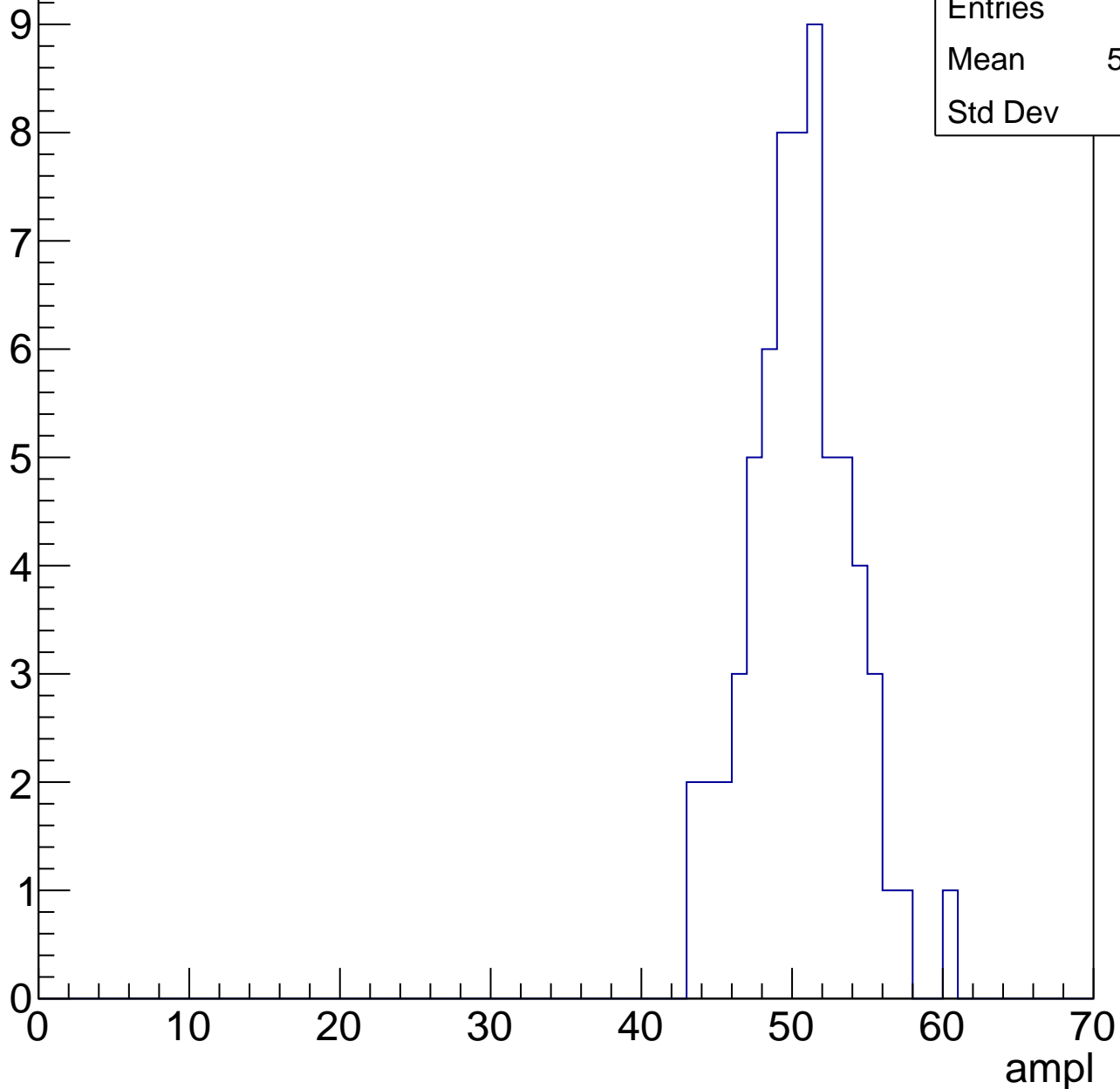
**Gaus Width: 3.2744**



# B0L000S, U7-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

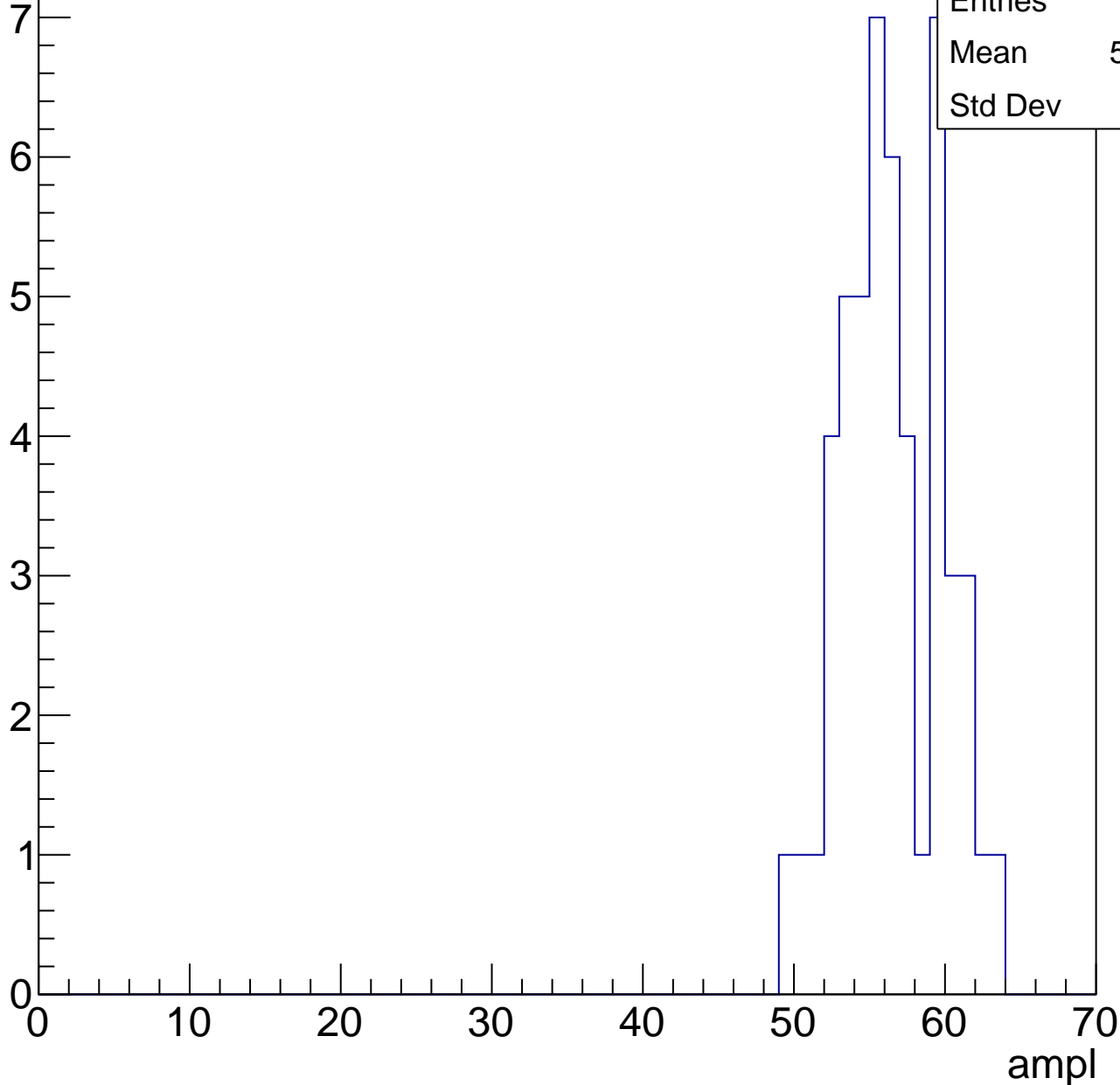


Entries	65
Mean	50.08
Std Dev	3.38

# B0L000S, U7-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

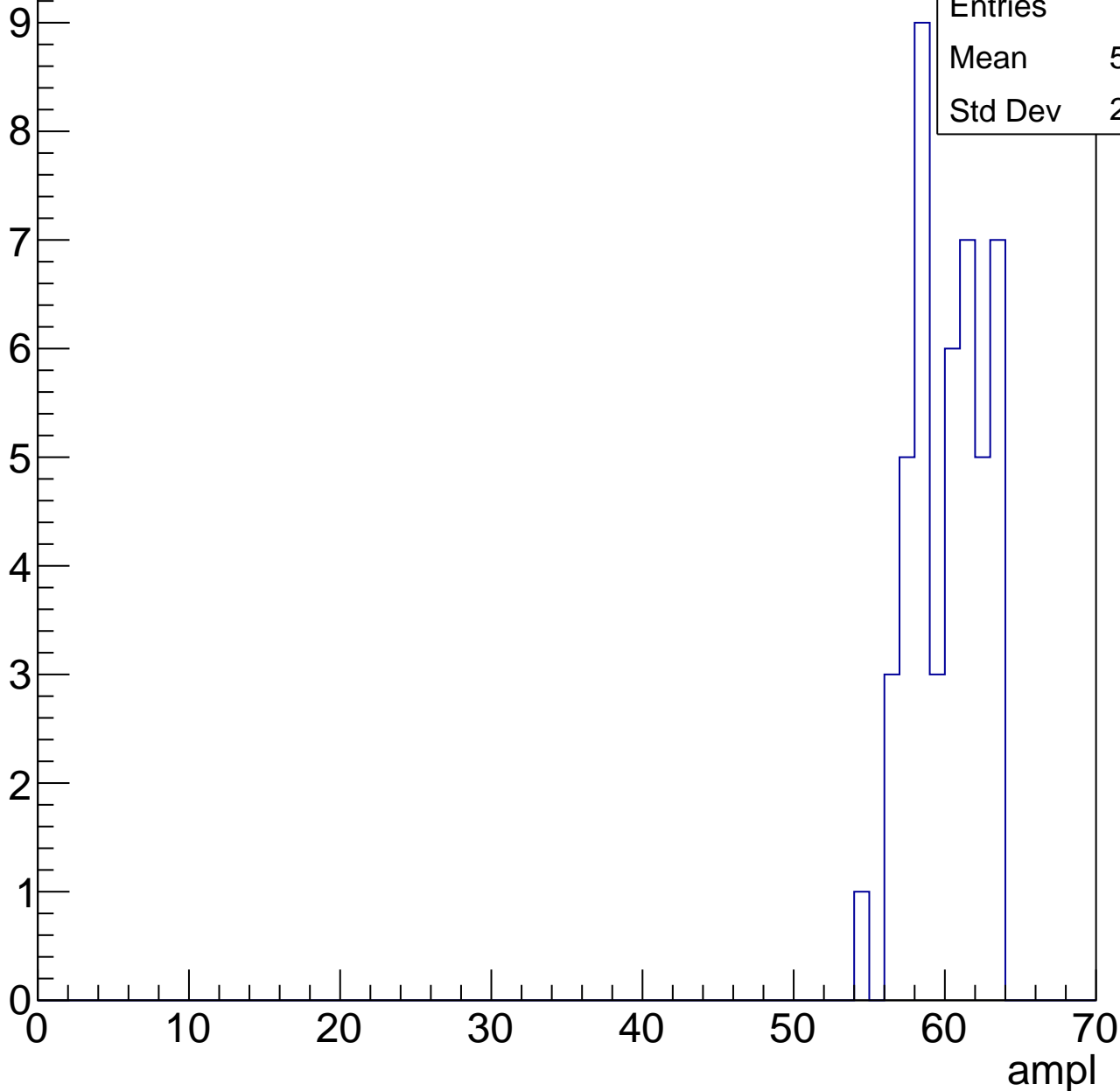


# B0L000S, U7-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

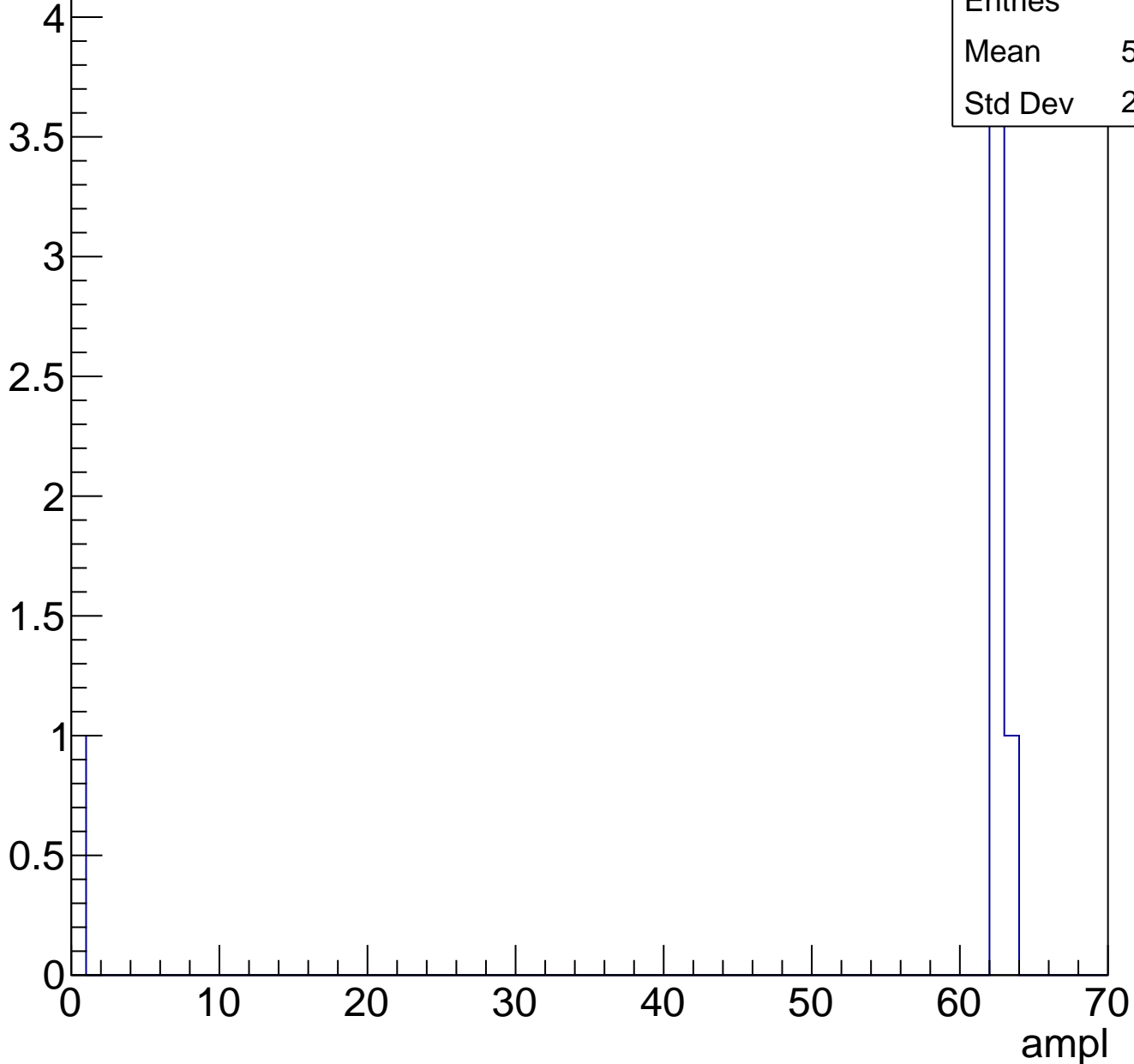
Entries	46
Mean	59.65
Std Dev	2.343



# B0L000S, U7-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch57, adc0

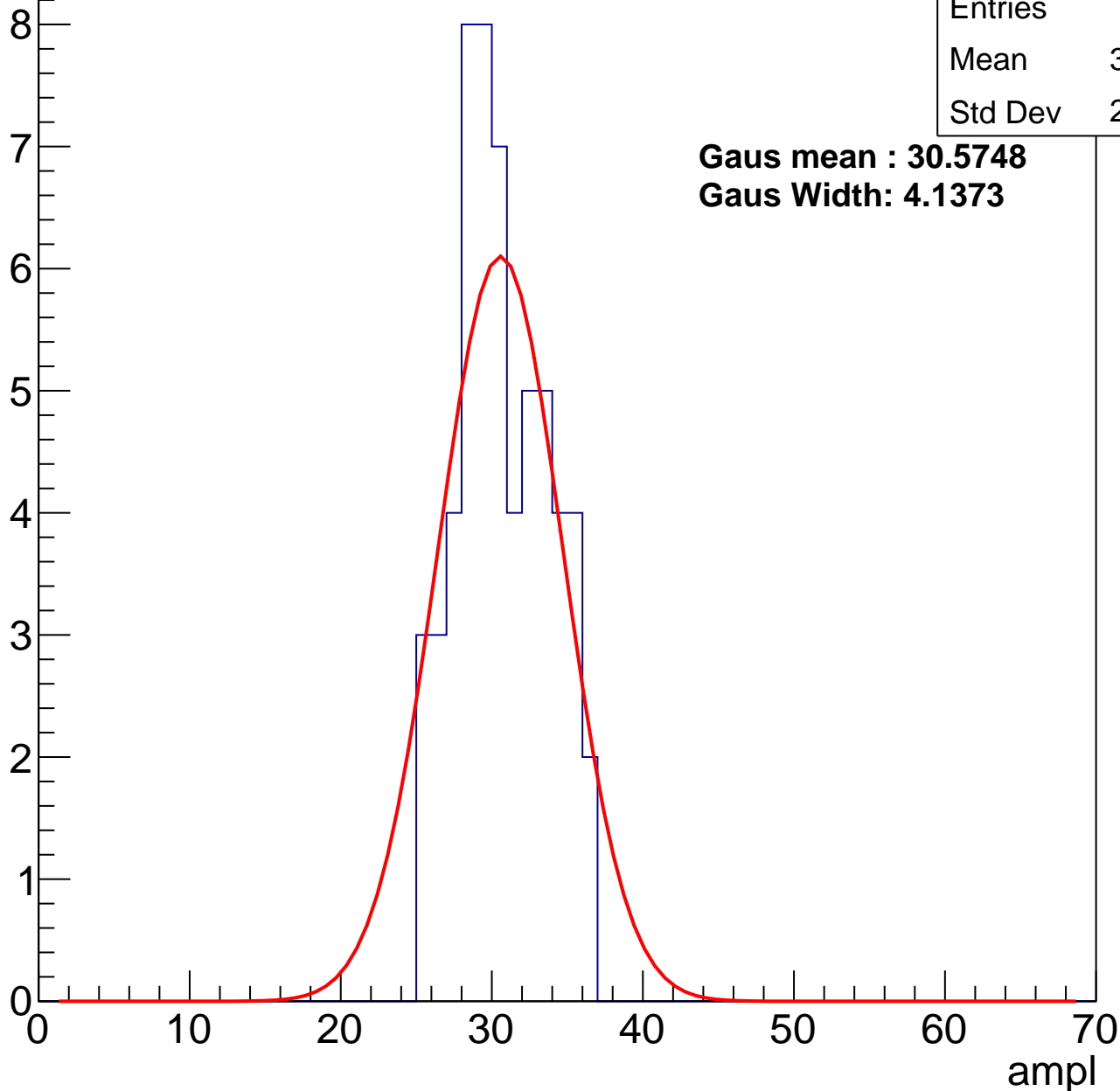
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	57
Mean	30.25
Std Dev	2.963

**Gaus mean : 30.5748**

**Gaus Width: 4.1373**



# B0L000S, U7-ch57, adc1

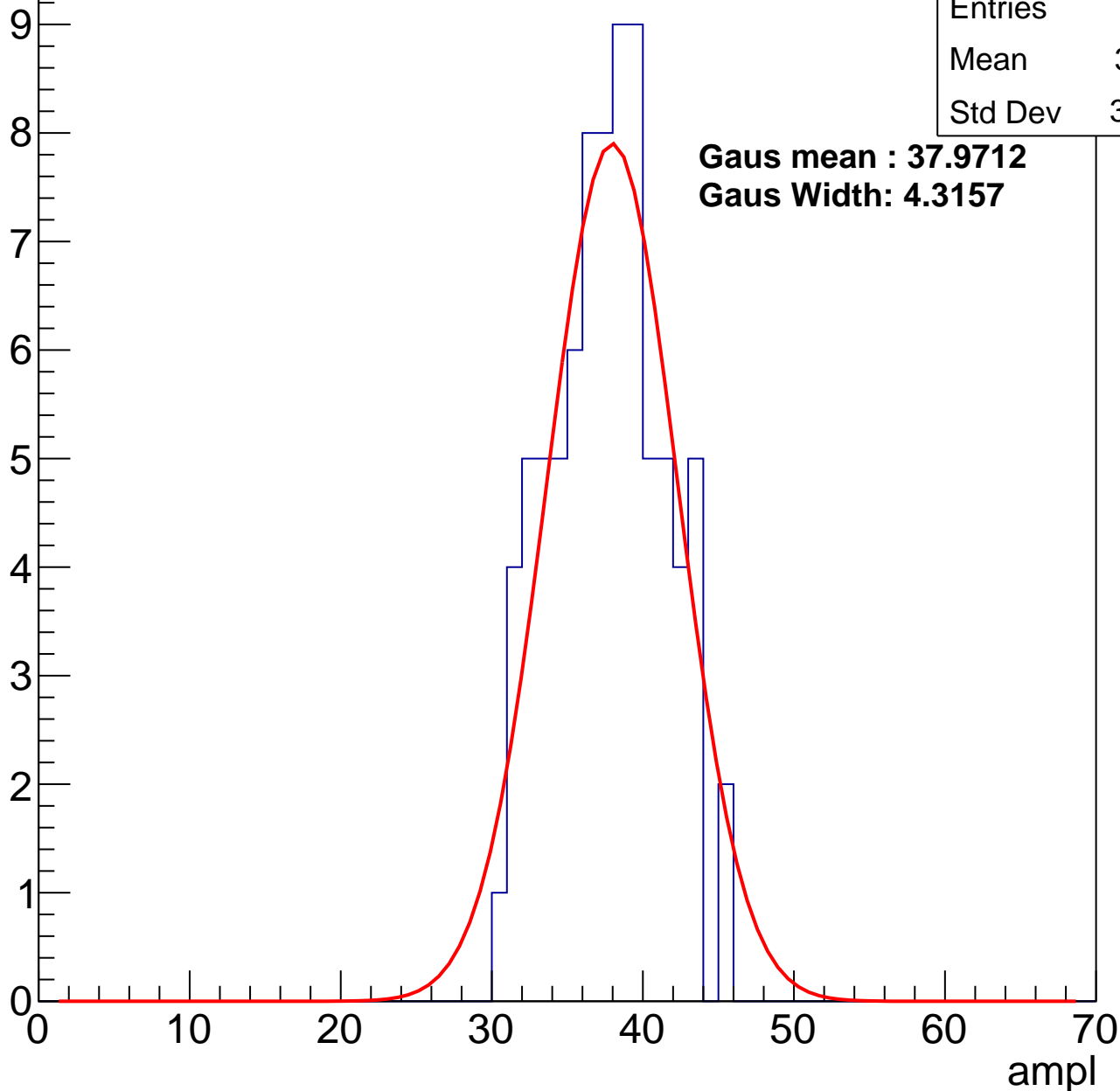
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	81
Mean	37.21
Std Dev	3.599

**Gaus mean : 37.9712**

**Gaus Width: 4.3157**



# B0L000S, U7-ch57, adc2

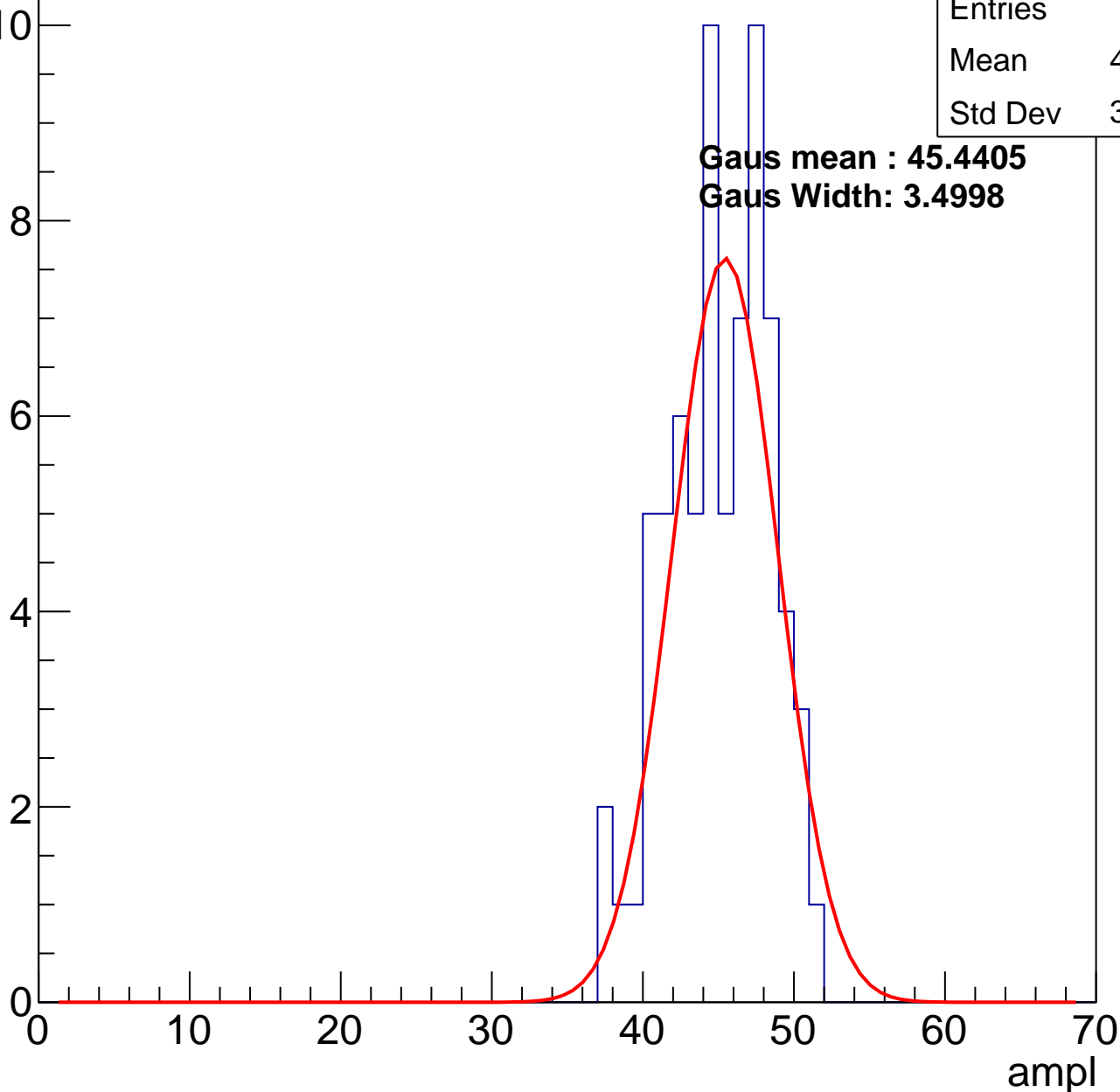
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	72
Mean	44.62
Std Dev	3.285

**Gaus mean : 45.4405**

**Gaus Width: 3.4998**

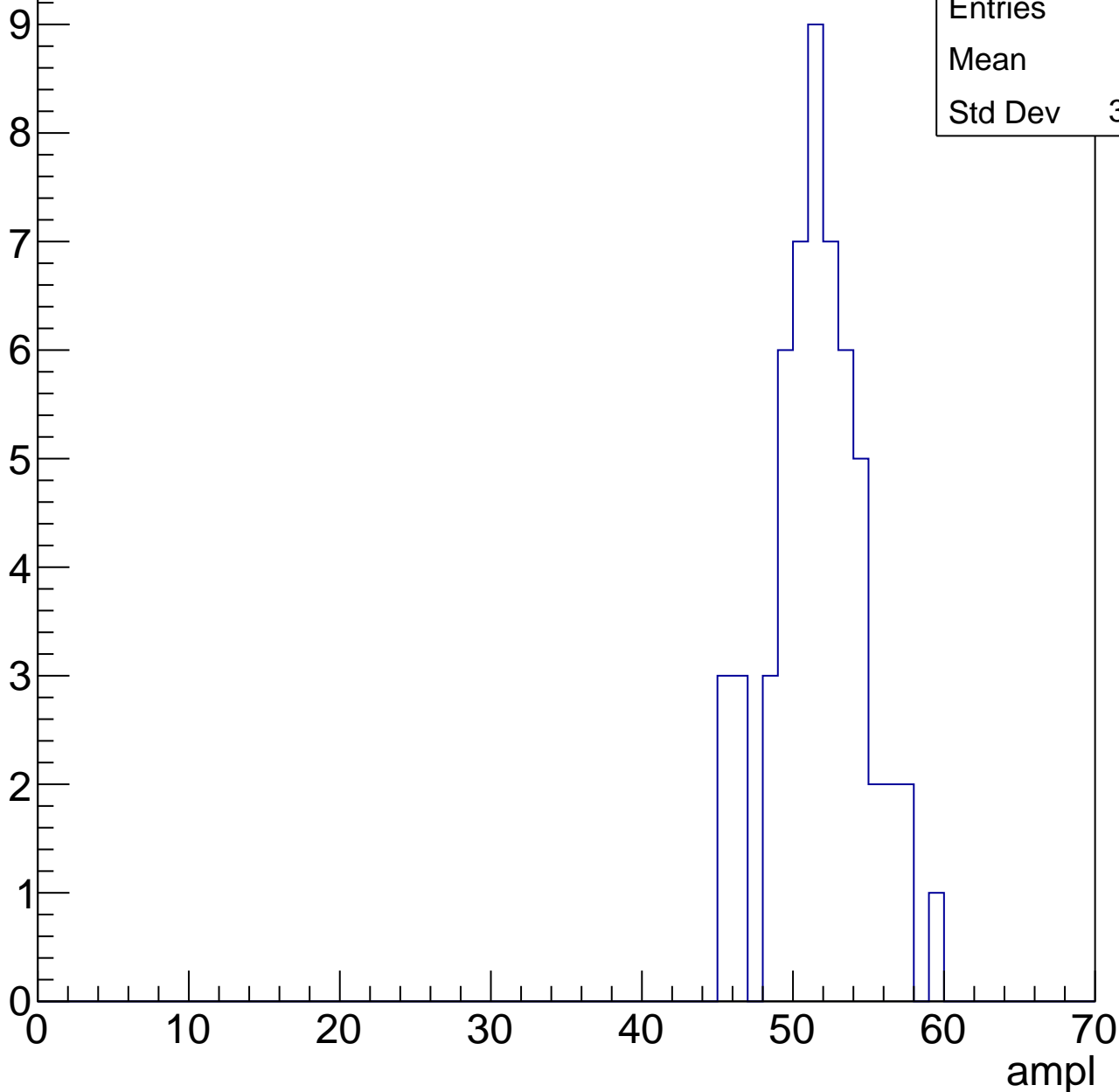


# B0L000S, U7-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	56
Mean	51.2
Std Dev	3.085

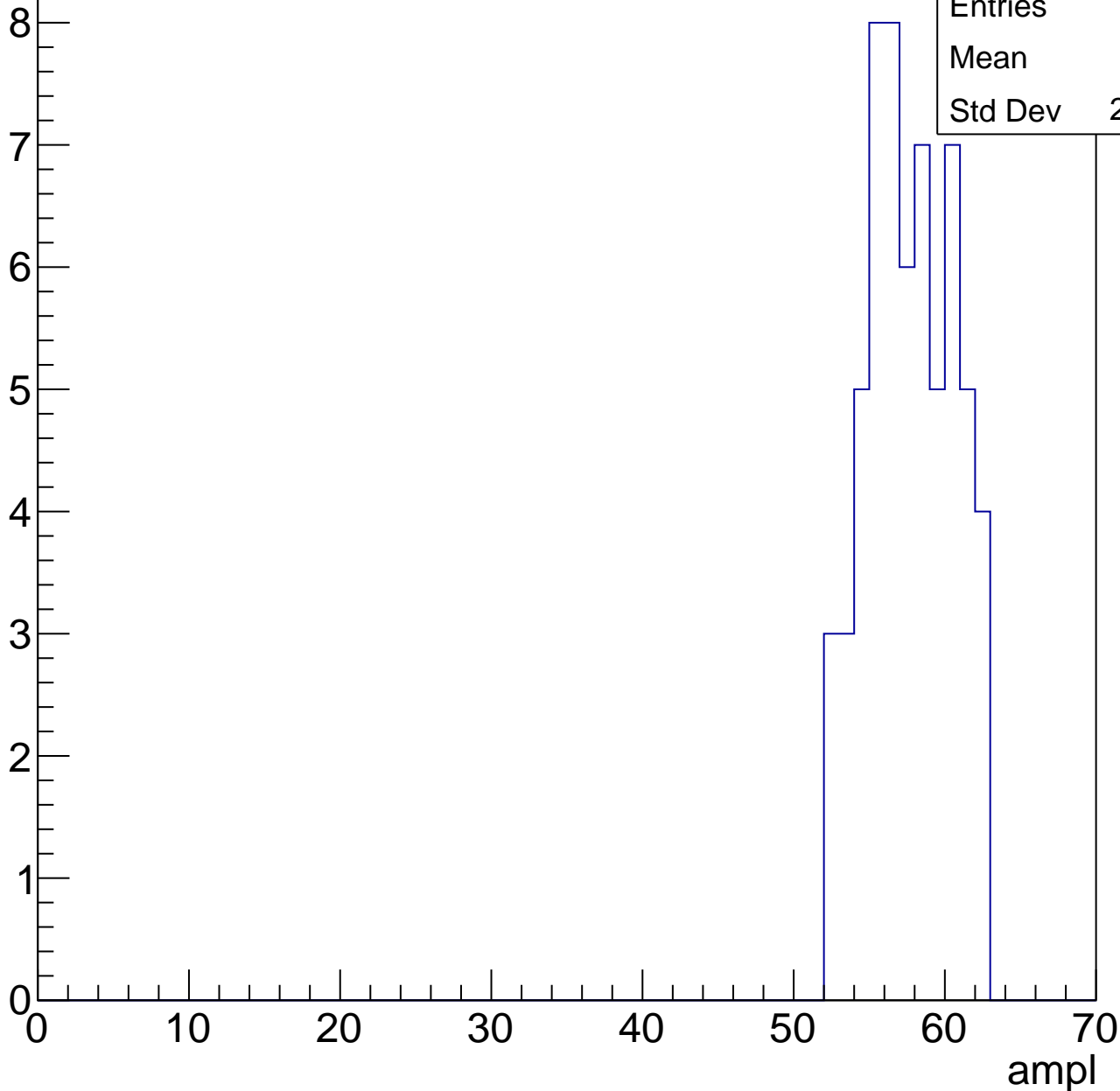


# B0L000S, U7-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	61
Mean	57.2
Std Dev	2.792

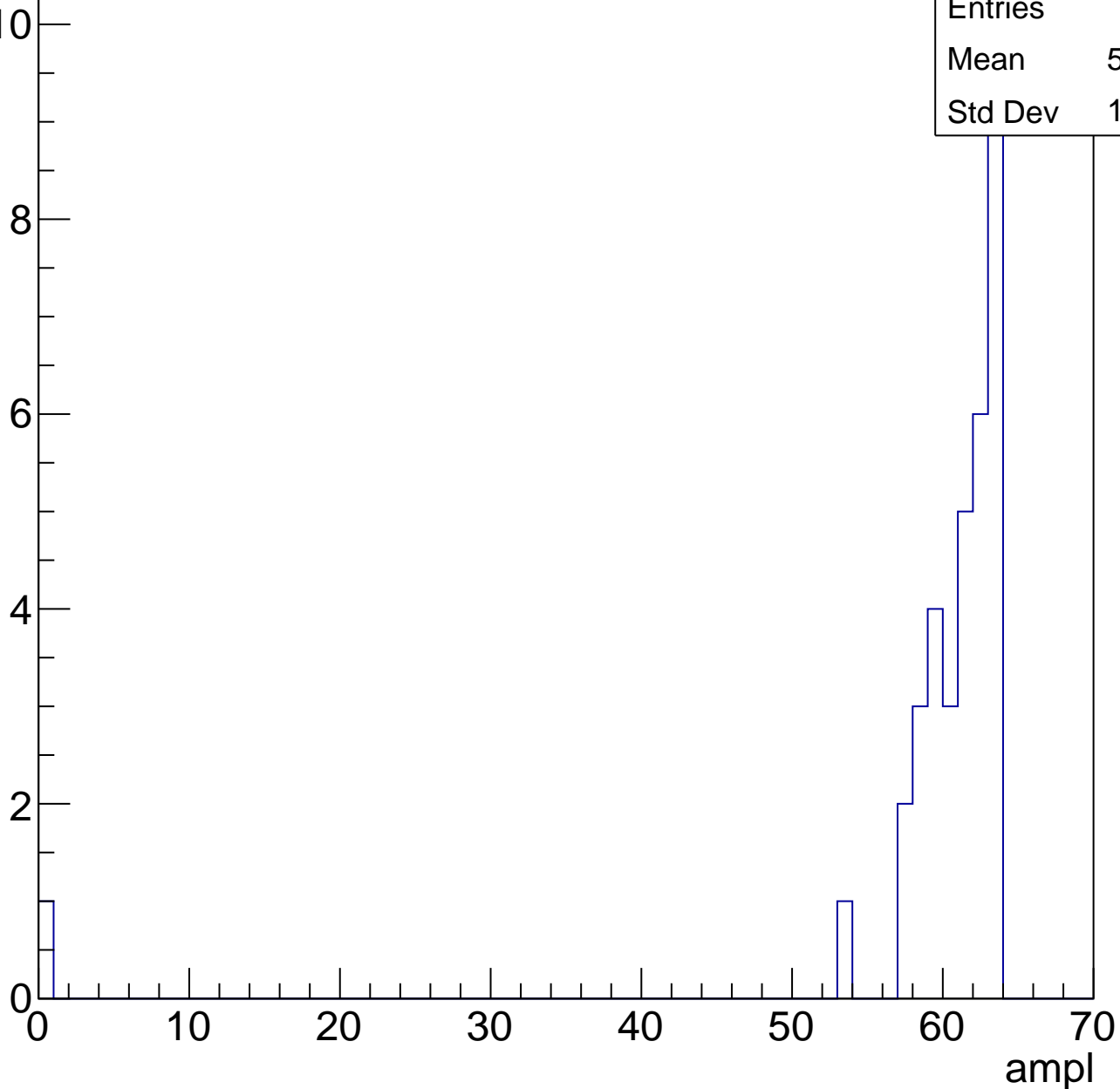


# B0L000S, U7-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	35
Mean	58.97
Std Dev	10.37



# B0L000S, U7-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L000S, U7-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L000S, U7-ch58, adc0

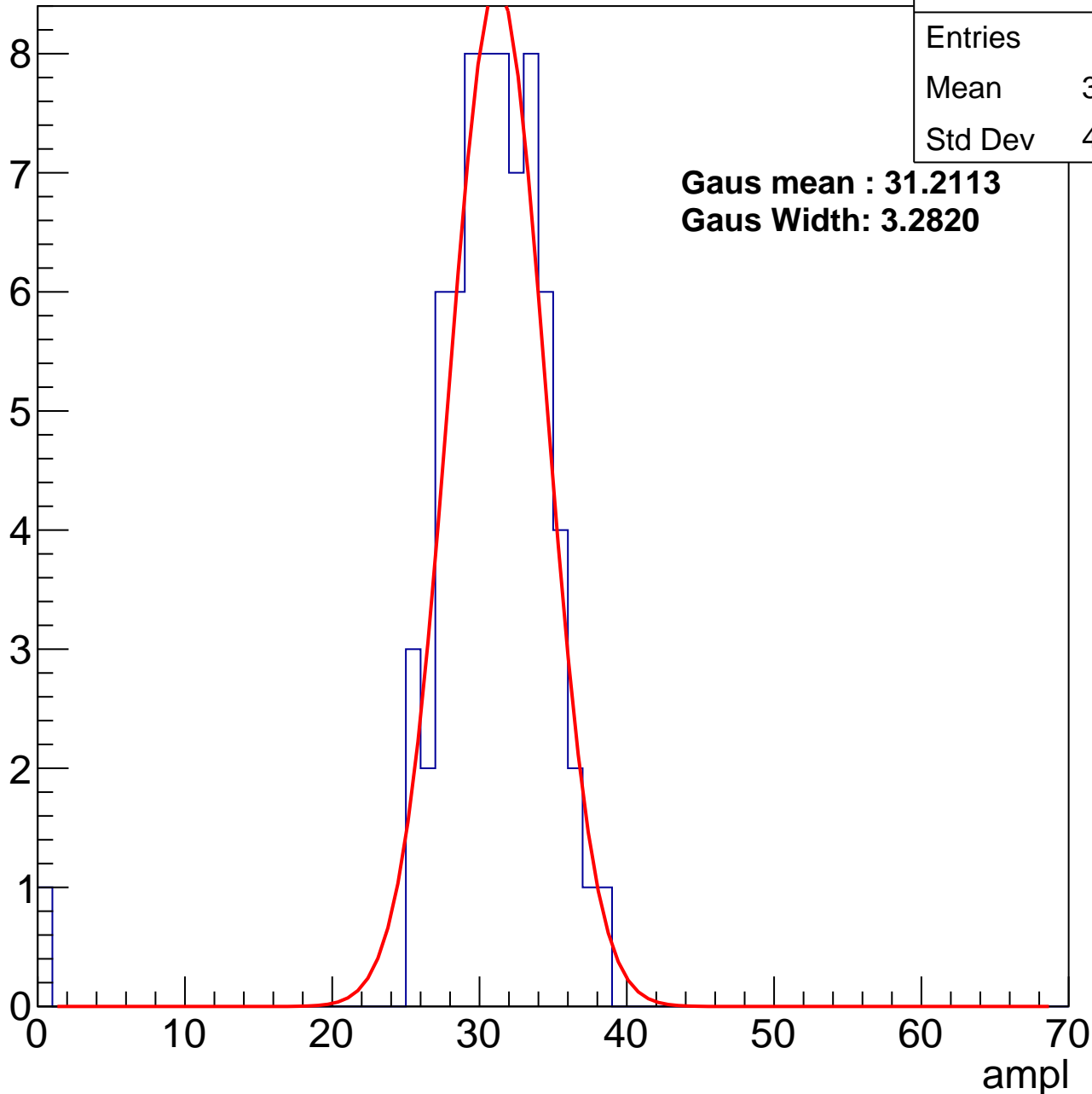
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	71
Mean	30.37
Std Dev	4.706

**Gaus mean : 31.2113**

**Gaus Width: 3.2820**



# B0L000S, U7-ch58, adc1

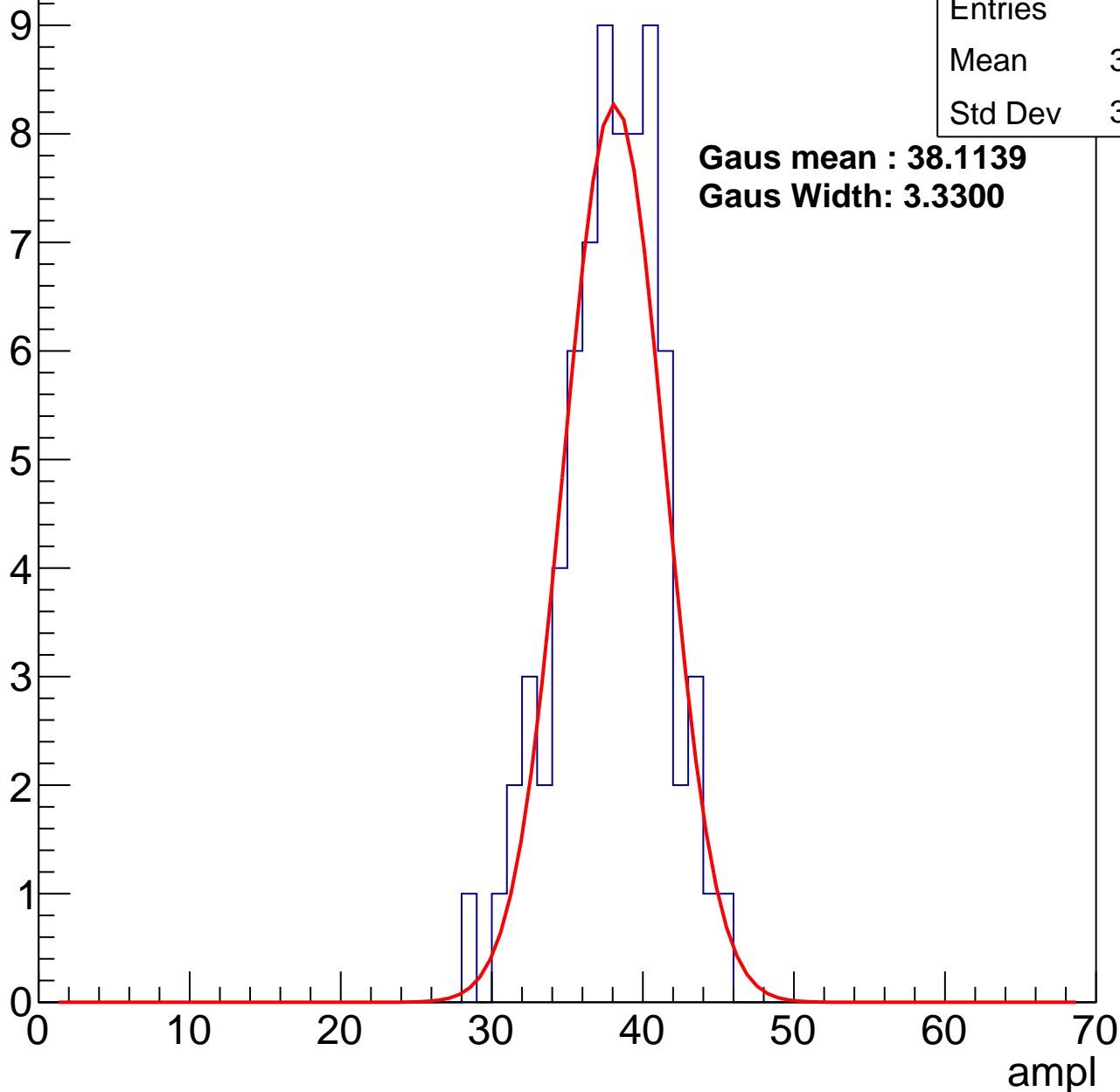
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	73
Mean	37.49
Std Dev	3.405

**Gaus mean : 38.1139**

**Gaus Width: 3.3300**



# B0L000S, U7-ch58, adc2

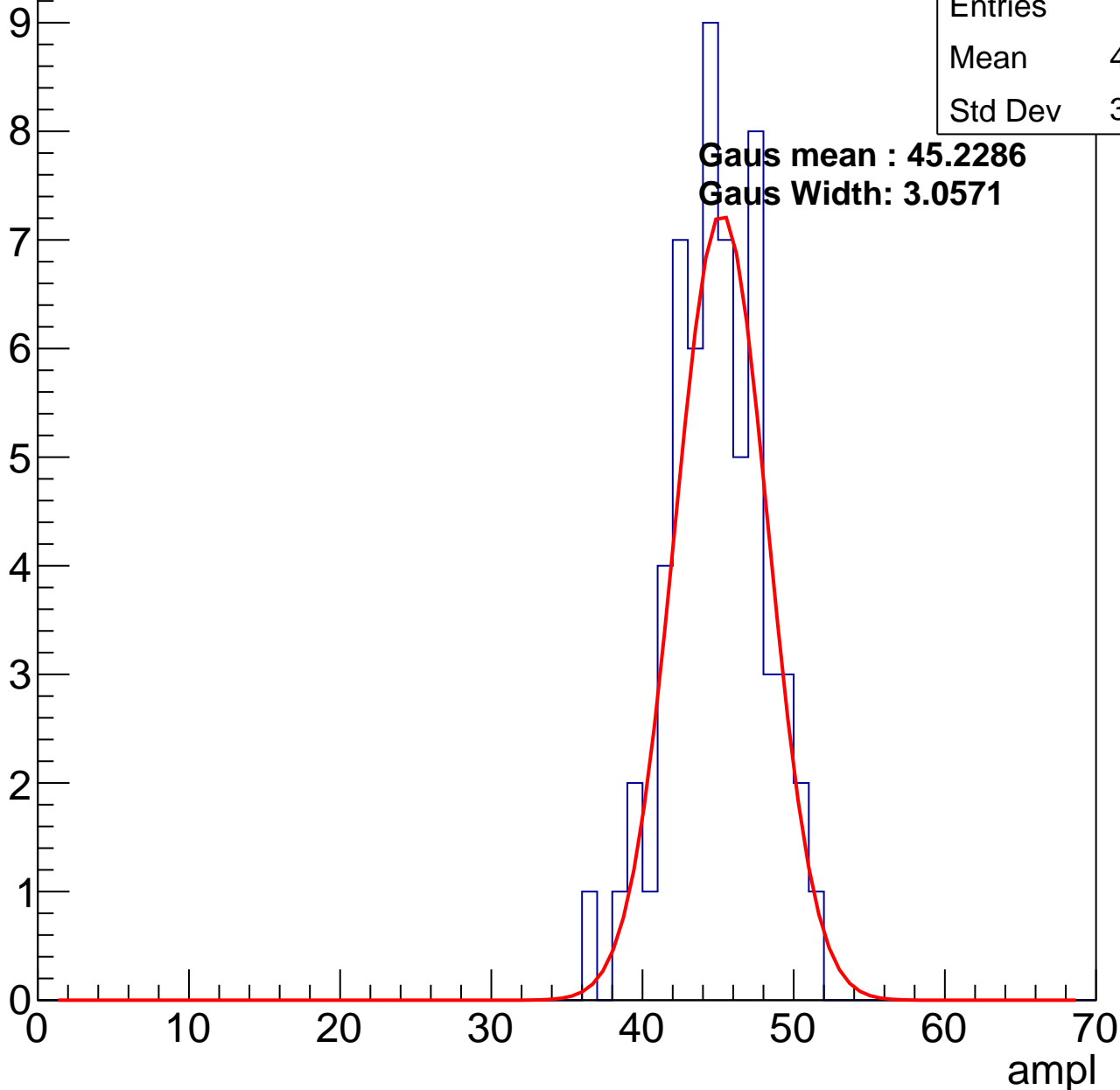
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	60
Mean	44.45
Std Dev	3.074

**Gaus mean : 45.2286**

**Gaus Width: 3.0571**

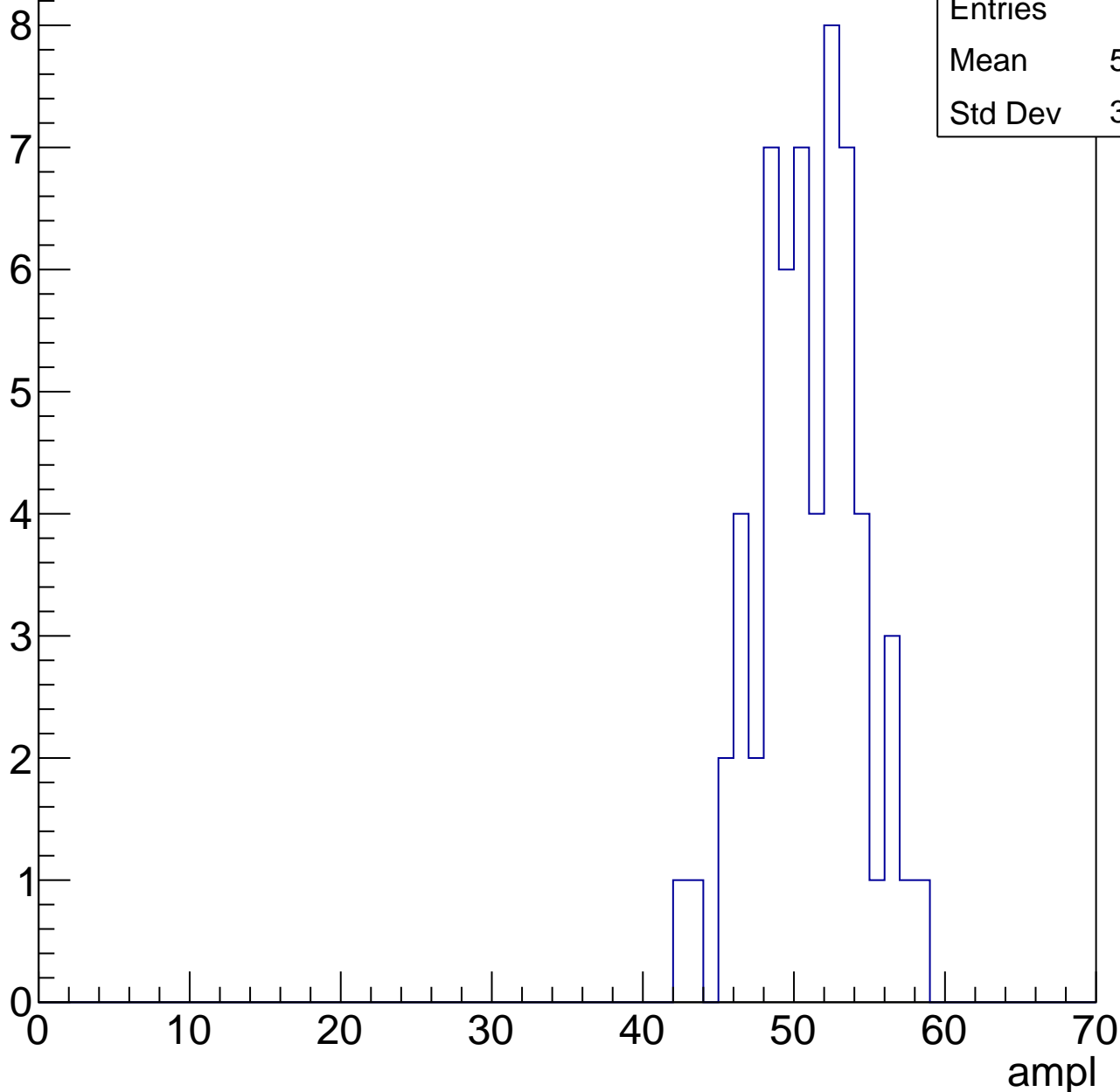


# B0L000S, U7-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	59
Mean	50.47
Std Dev	3.382



# B0L000S, U7-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

7

6

5

4

3

2

1

0

Entries	57
Mean	55.68
Std Dev	3.299

10

20

30

40

50

60

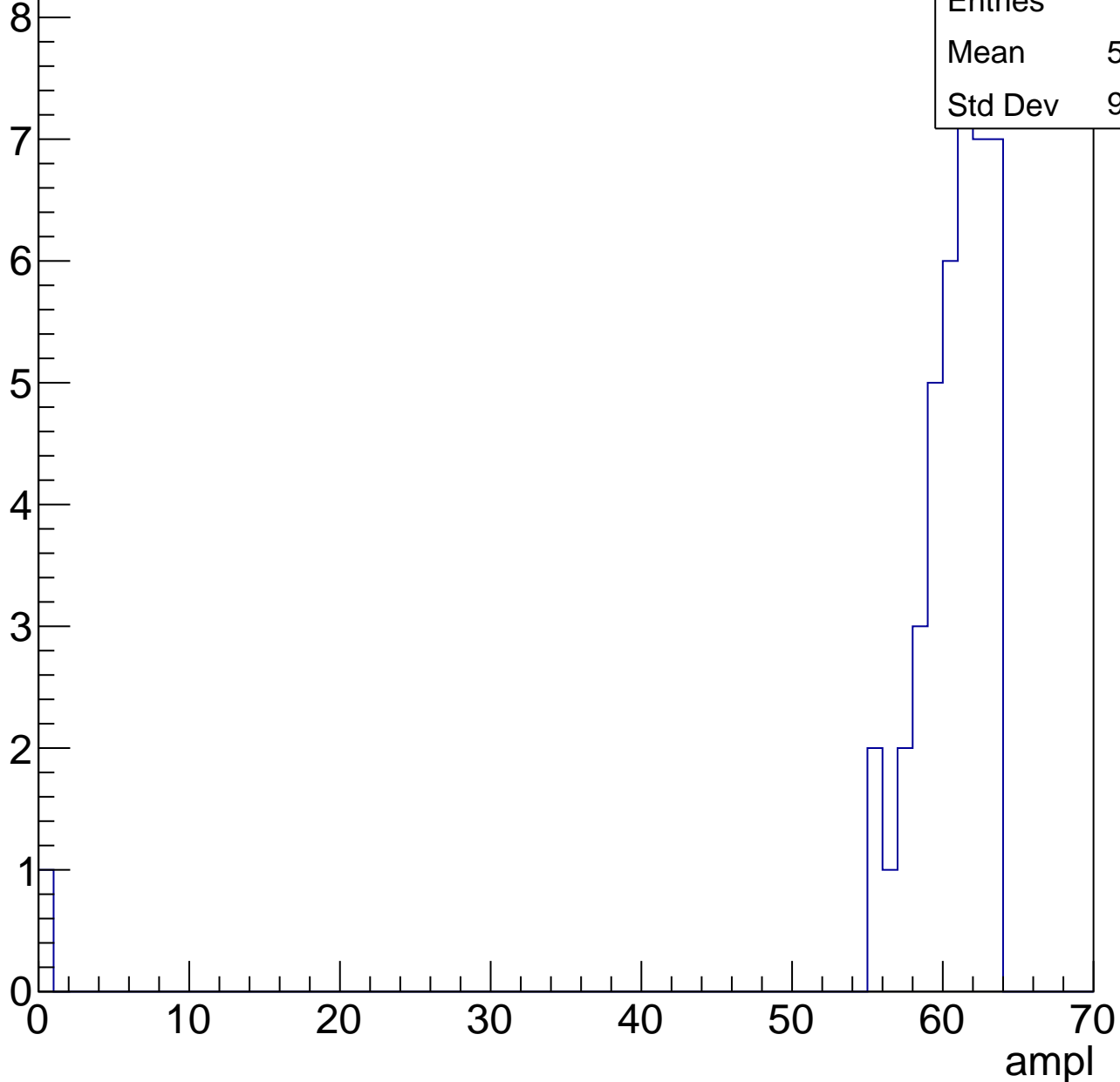
70

ampl

# B0L000S, U7-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

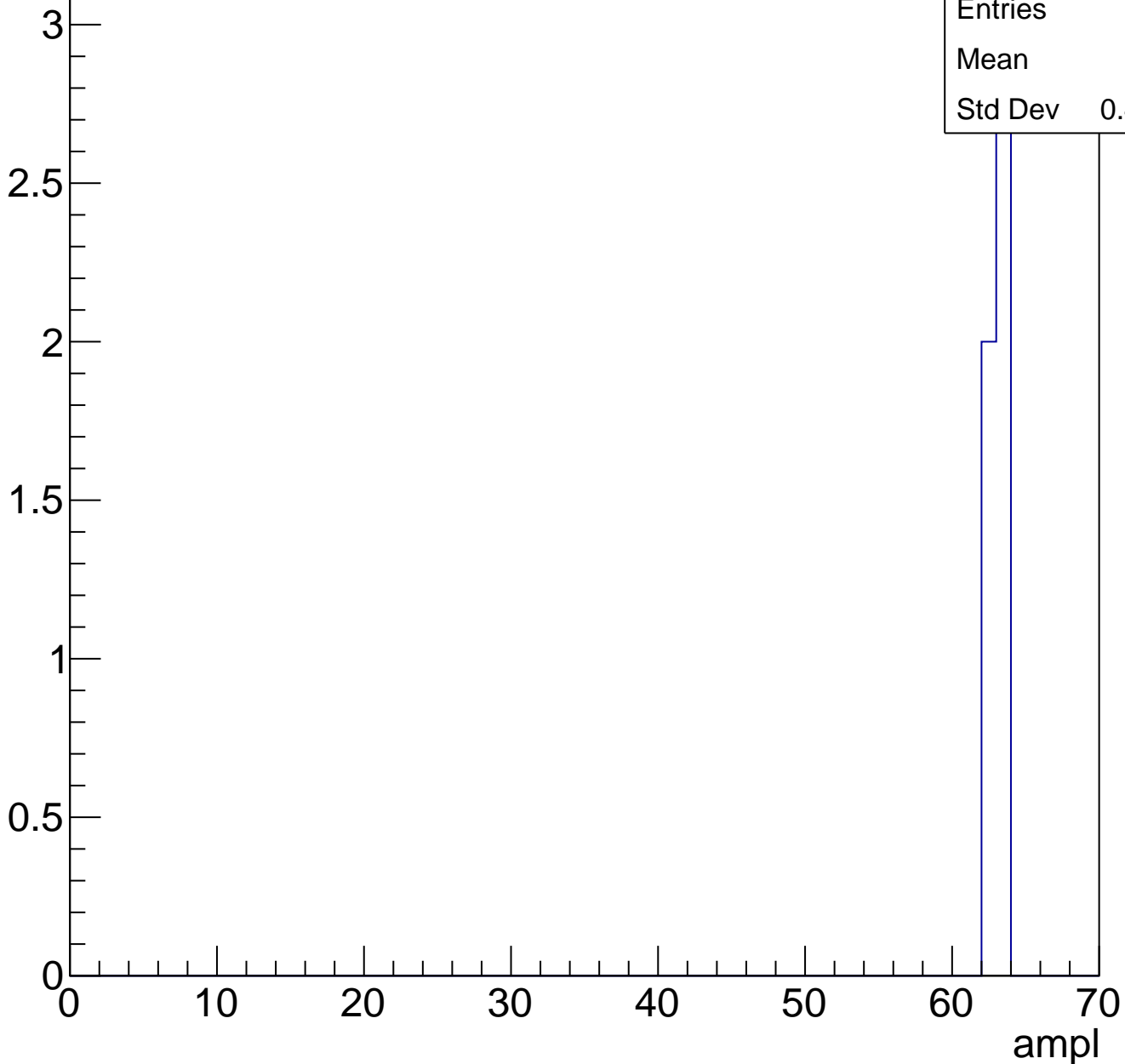
Entry



# B0L000S, U7-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch59, adc0

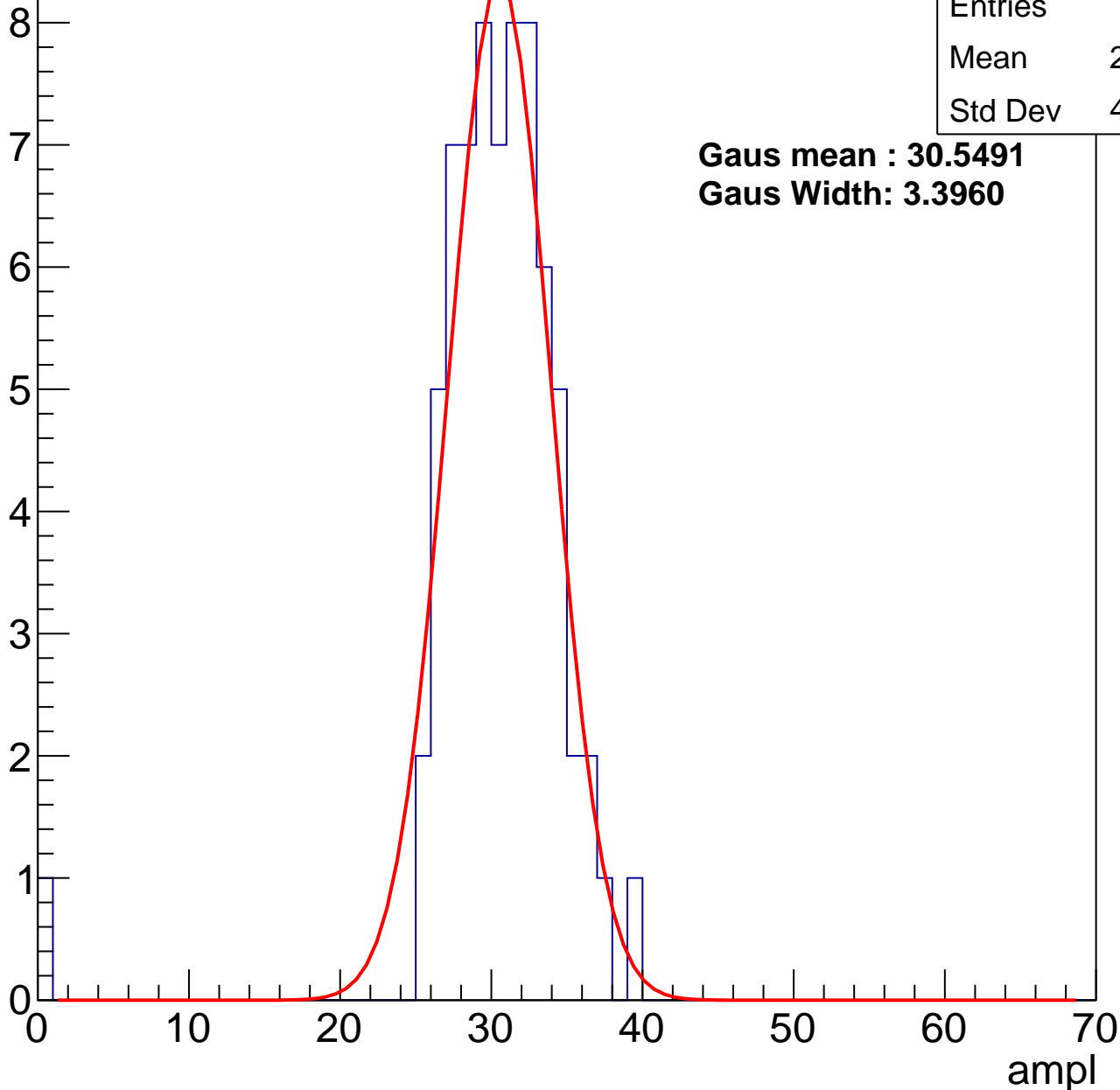
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	70
Mean	29.96
Std Dev	4.713

**Gaus mean : 30.5491**

**Gaus Width: 3.3960**



# B0L000S, U7-ch59, adc1

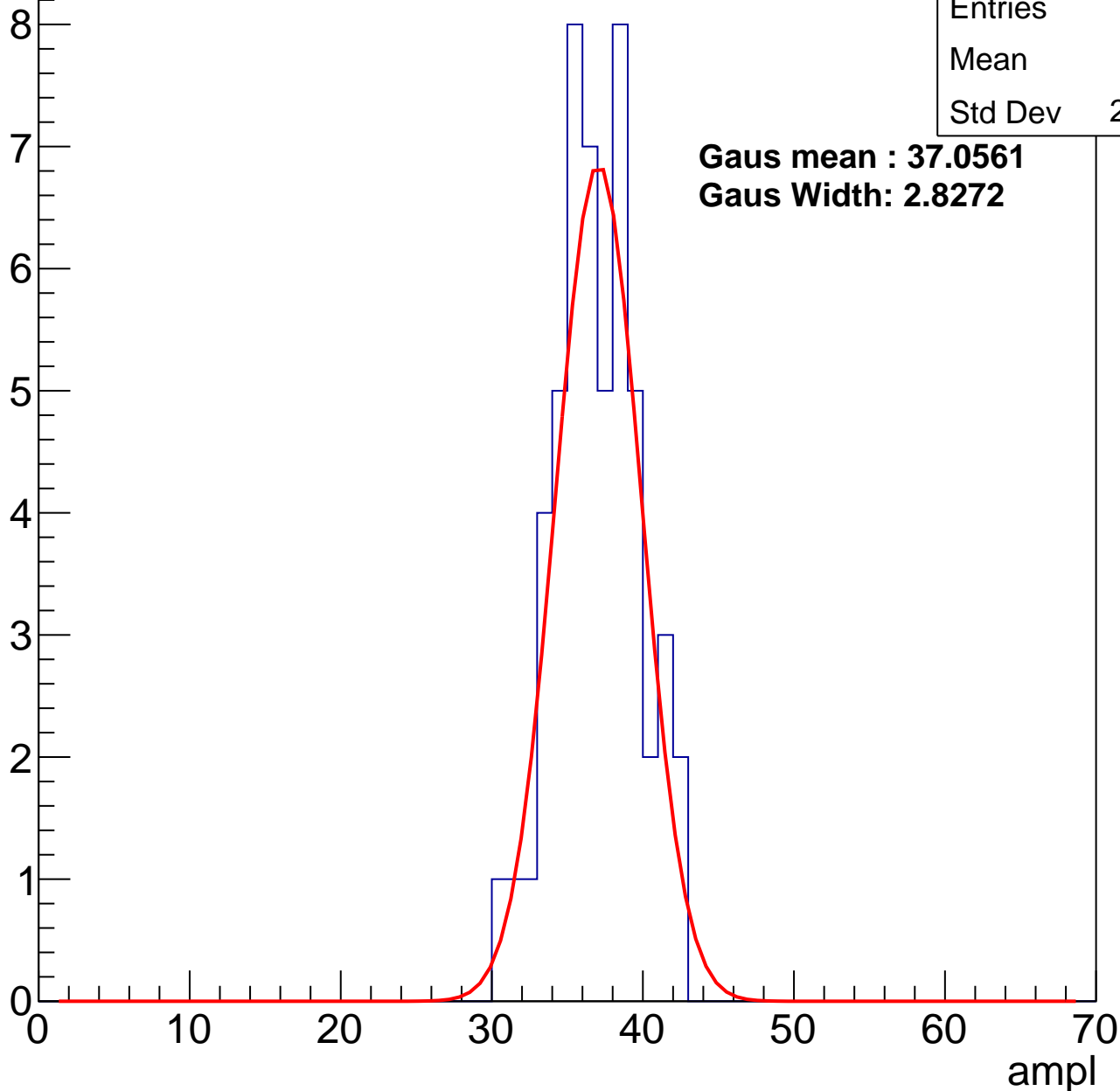
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	52
Mean	36.5
Std Dev	2.735

**Gaus mean : 37.0561**

**Gaus Width: 2.8272**



# B0L000S, U7-ch59, adc2

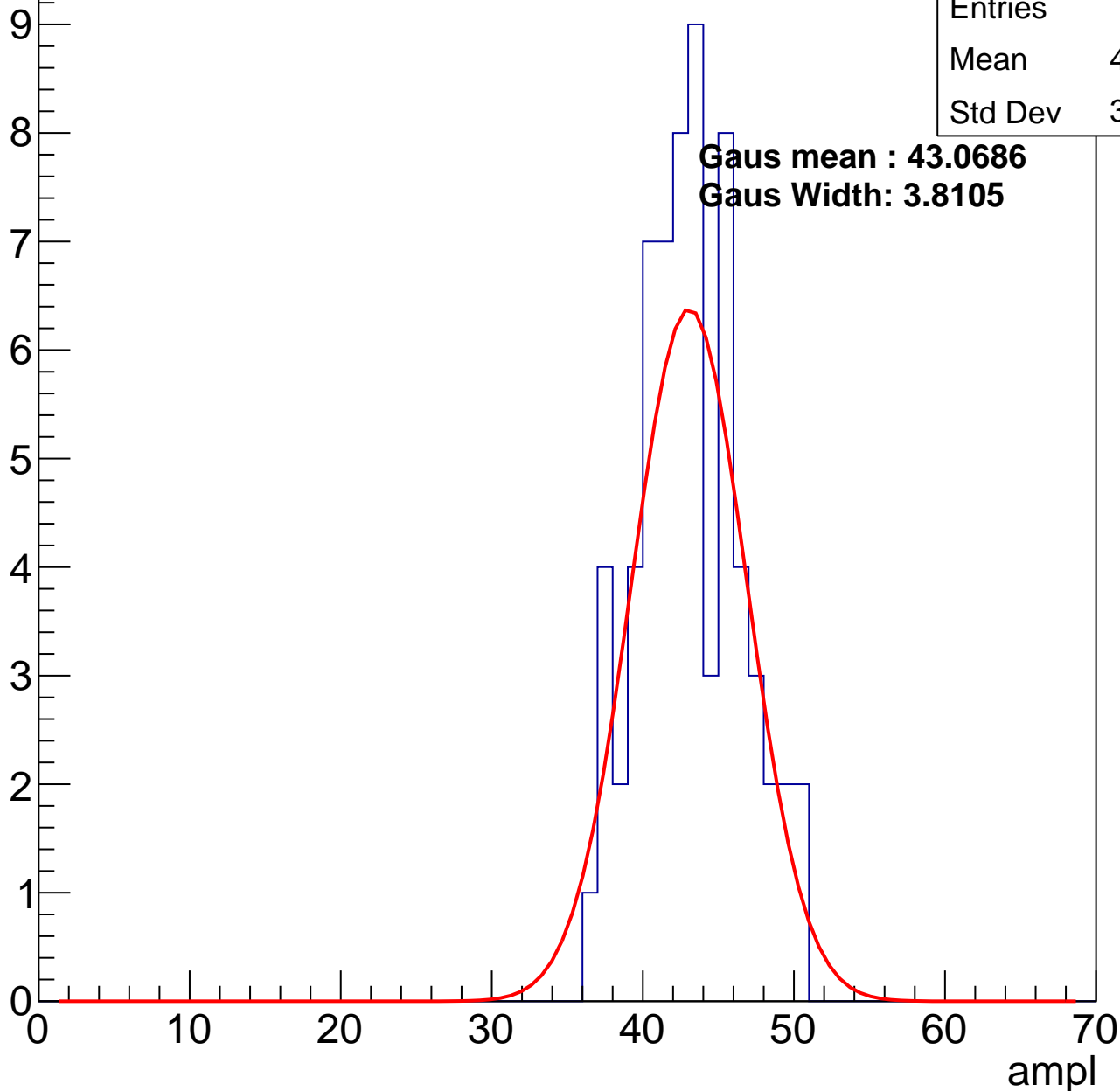
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	66
Mean	42.68
Std Dev	3.345

**Gaus mean : 43.0686**

**Gaus Width: 3.8105**

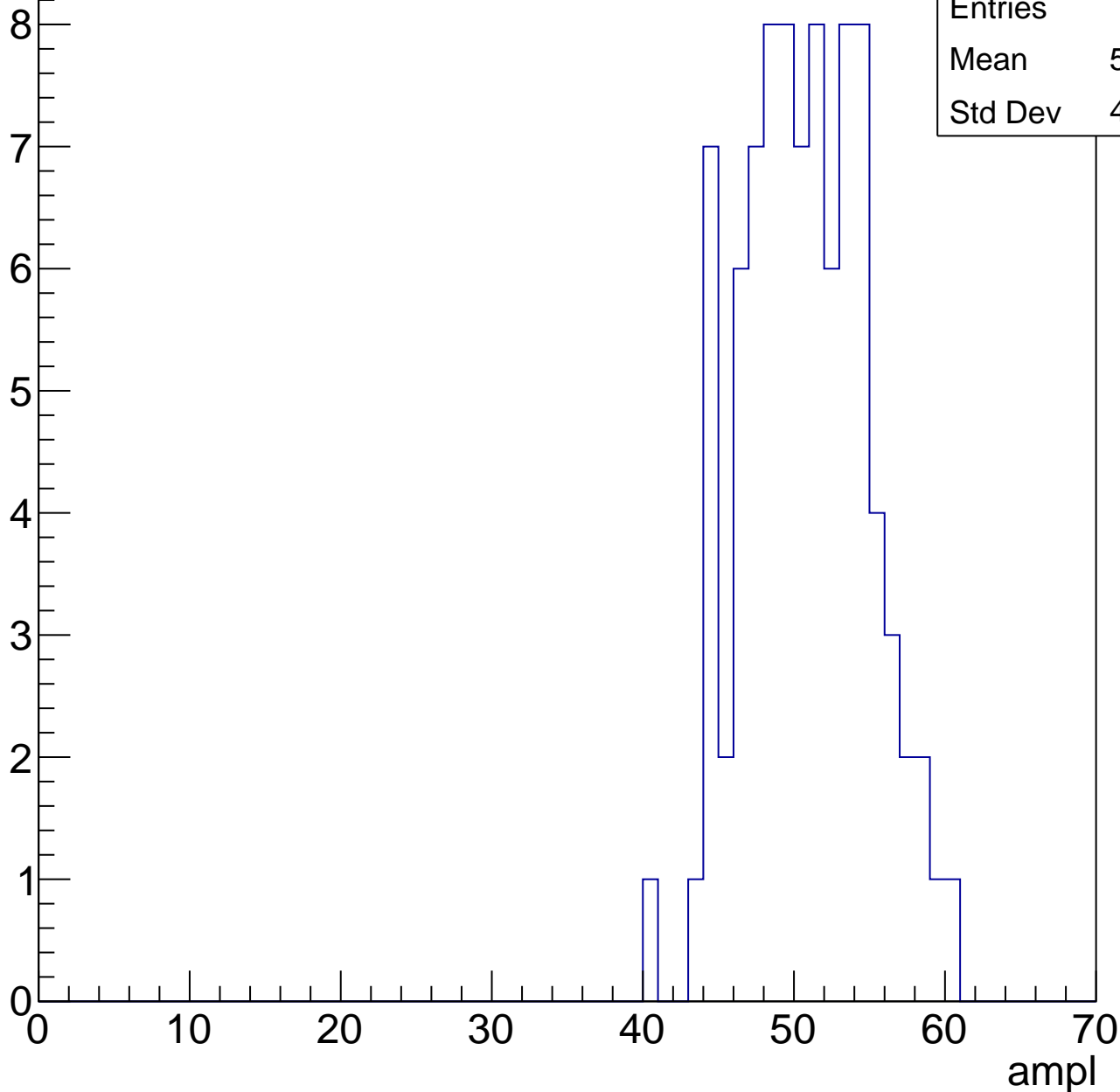


# B0L000S, U7-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	90
Mean	50.28
Std Dev	4.069

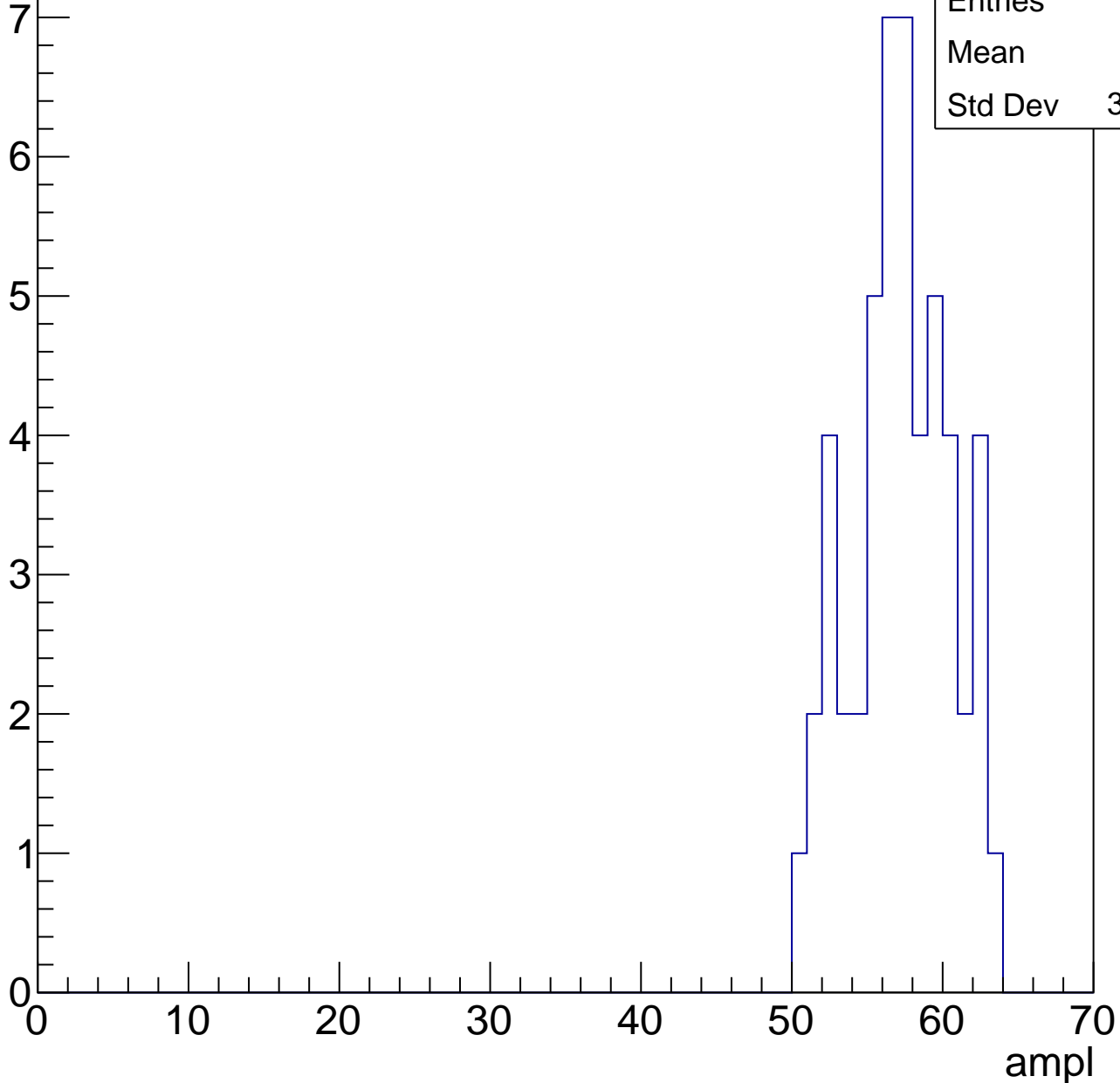


# B0L000S, U7-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	50
Mean	56.8
Std Dev	3.237

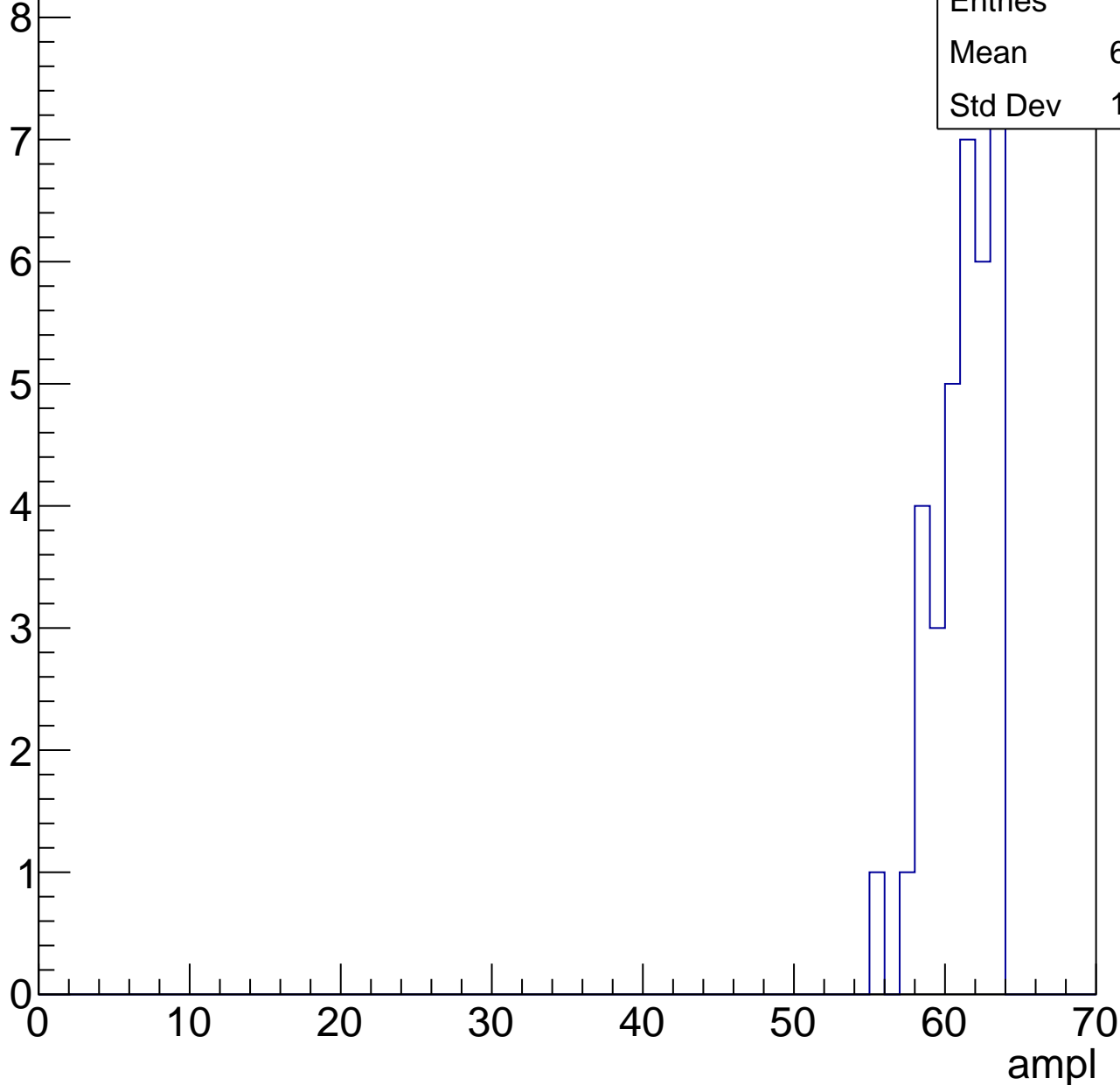


# B0L000S, U7-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

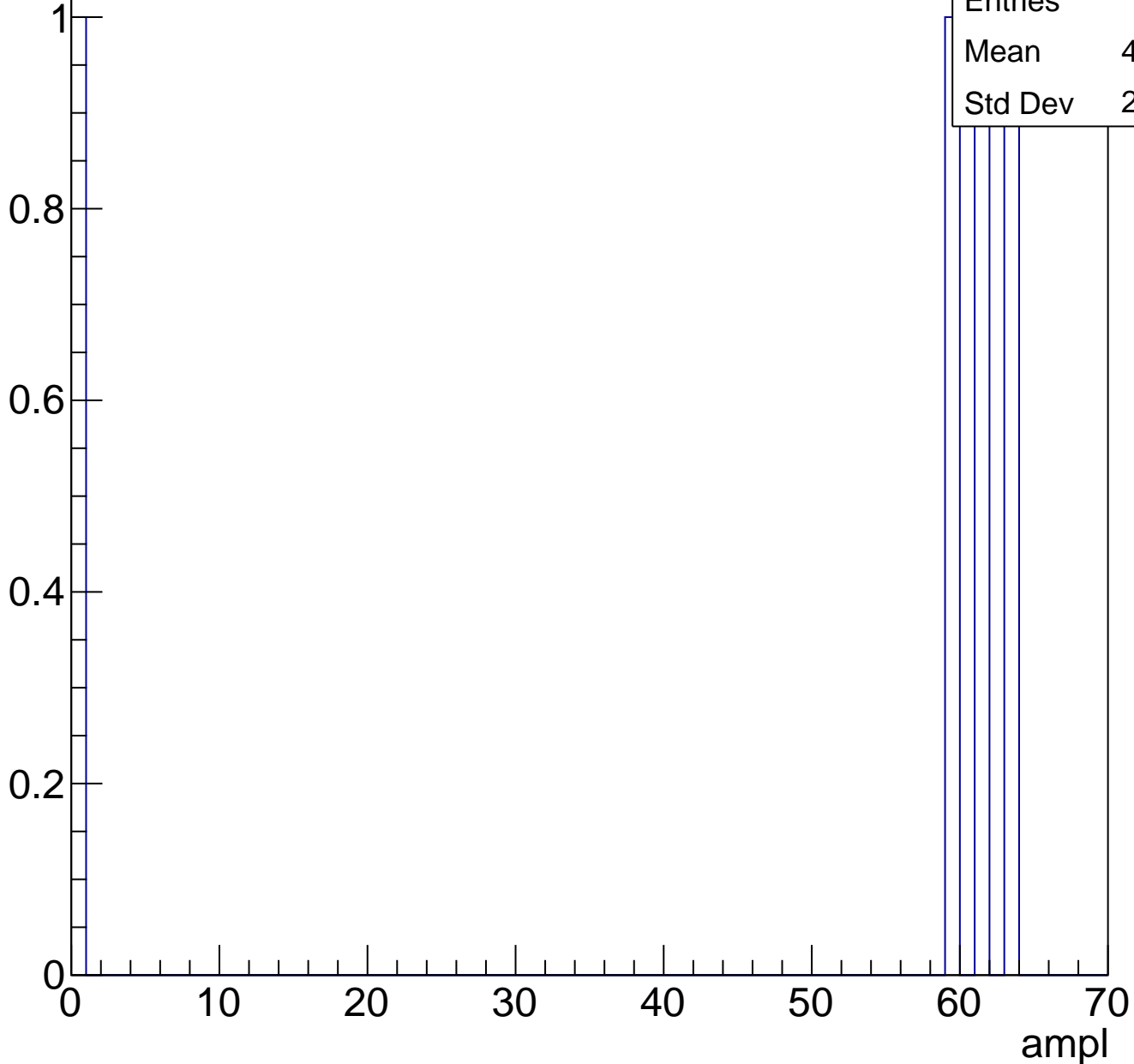
Entries	35
Mean	60.69
Std Dev	1.997



# B0L000S, U7-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch60, adc0

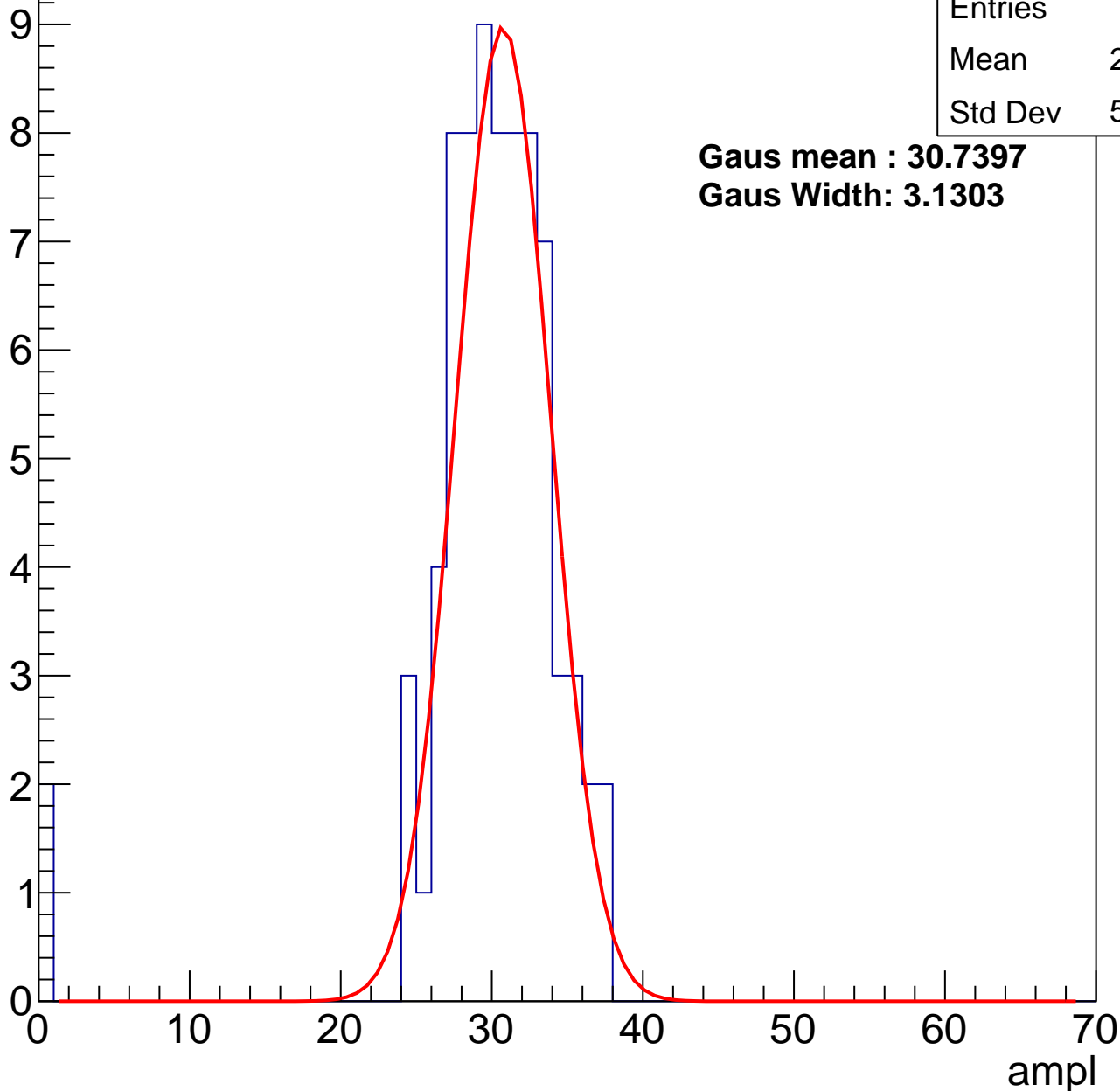
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	76
Mean	29.34
Std Dev	5.704

**Gaus mean : 30.7397**

**Gaus Width: 3.1303**



# B0L000S, U7-ch60, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	76
Mean	37.01
Std Dev	3.64

**Gaus mean : 37.5234**

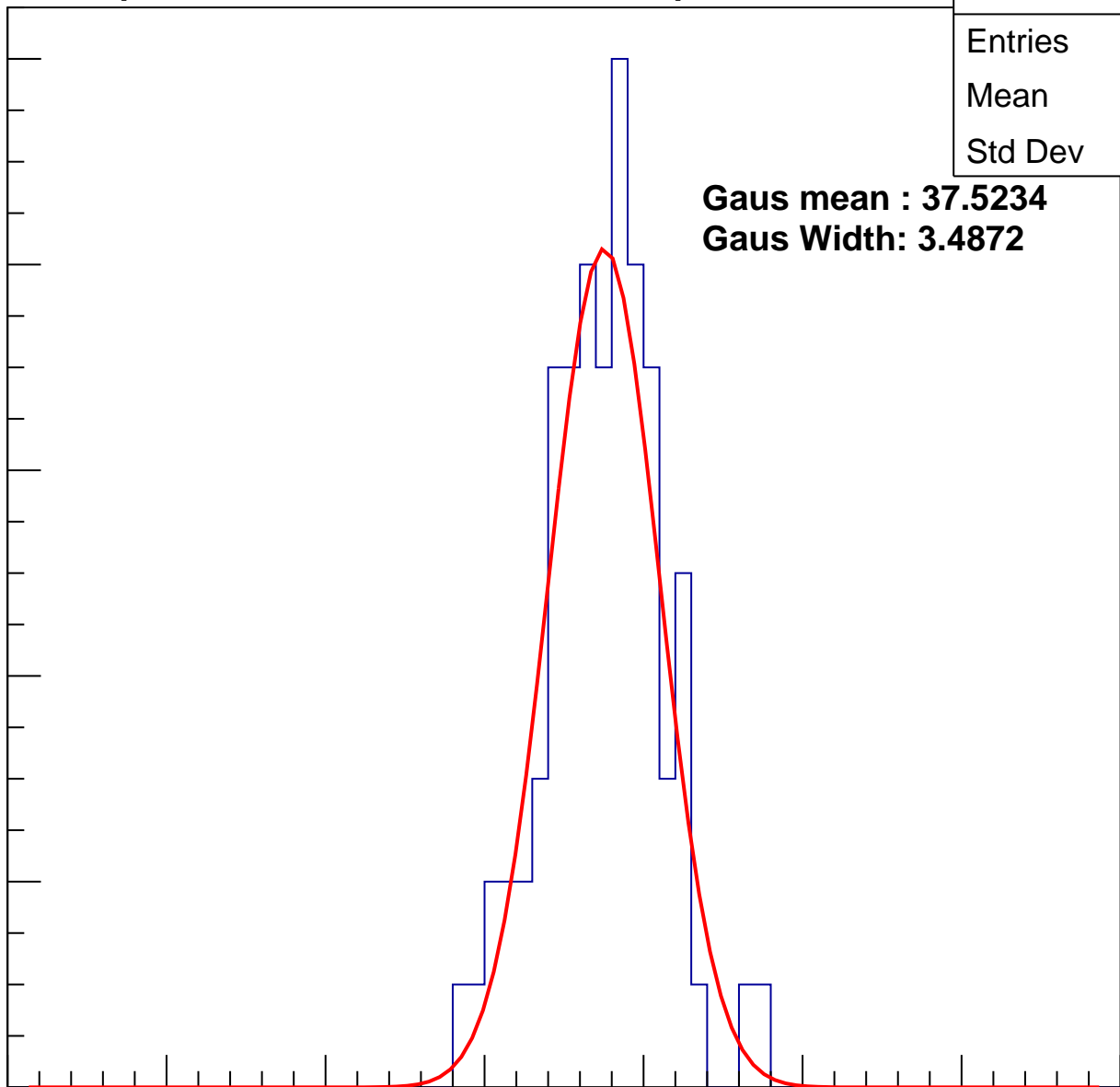
**Gaus Width: 3.4872**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L000S, U7-ch60, adc2

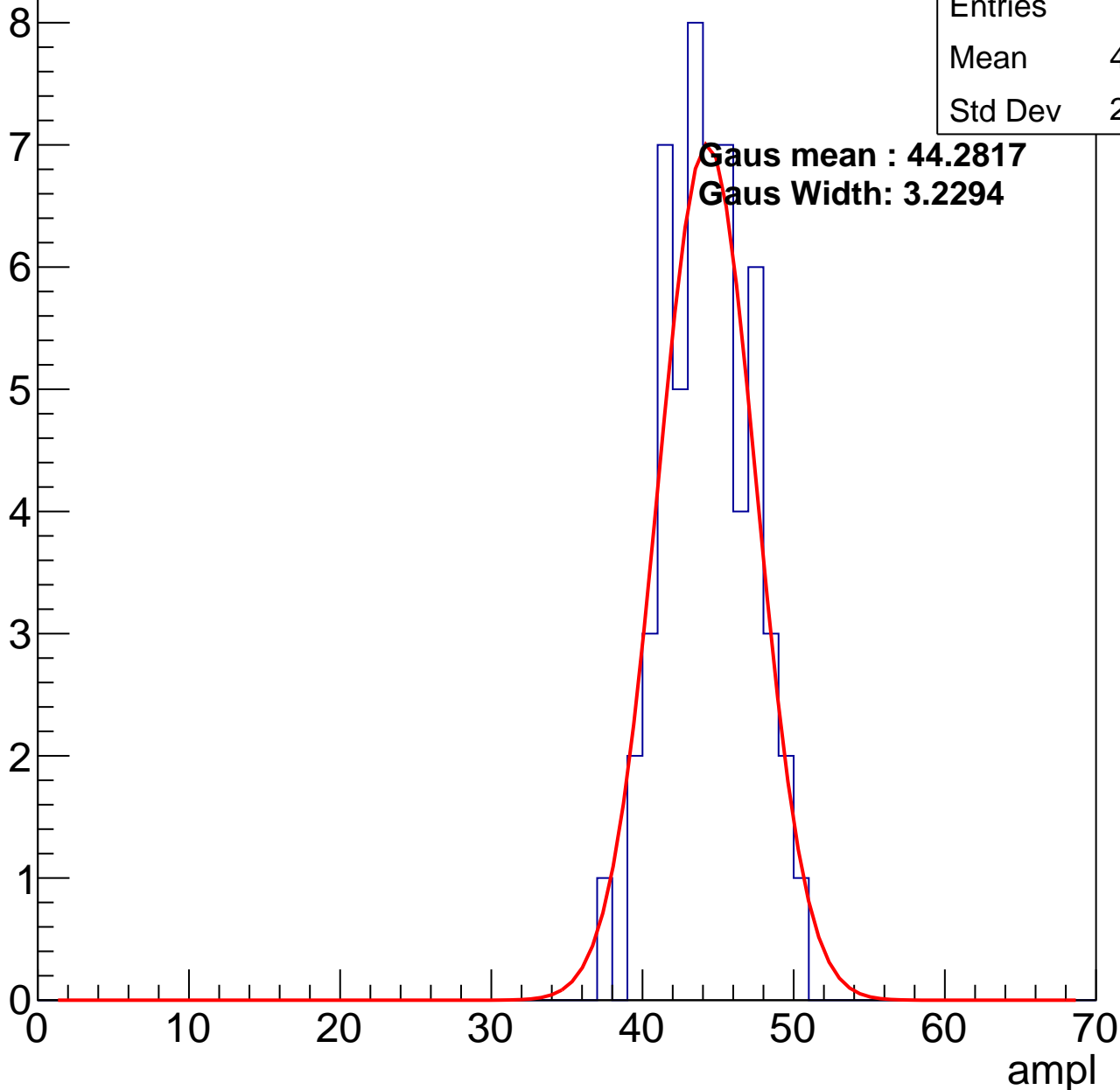
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	56
Mean	43.88
Std Dev	2.829

**Gaus mean : 44.2817**

**Gaus Width: 3.2294**

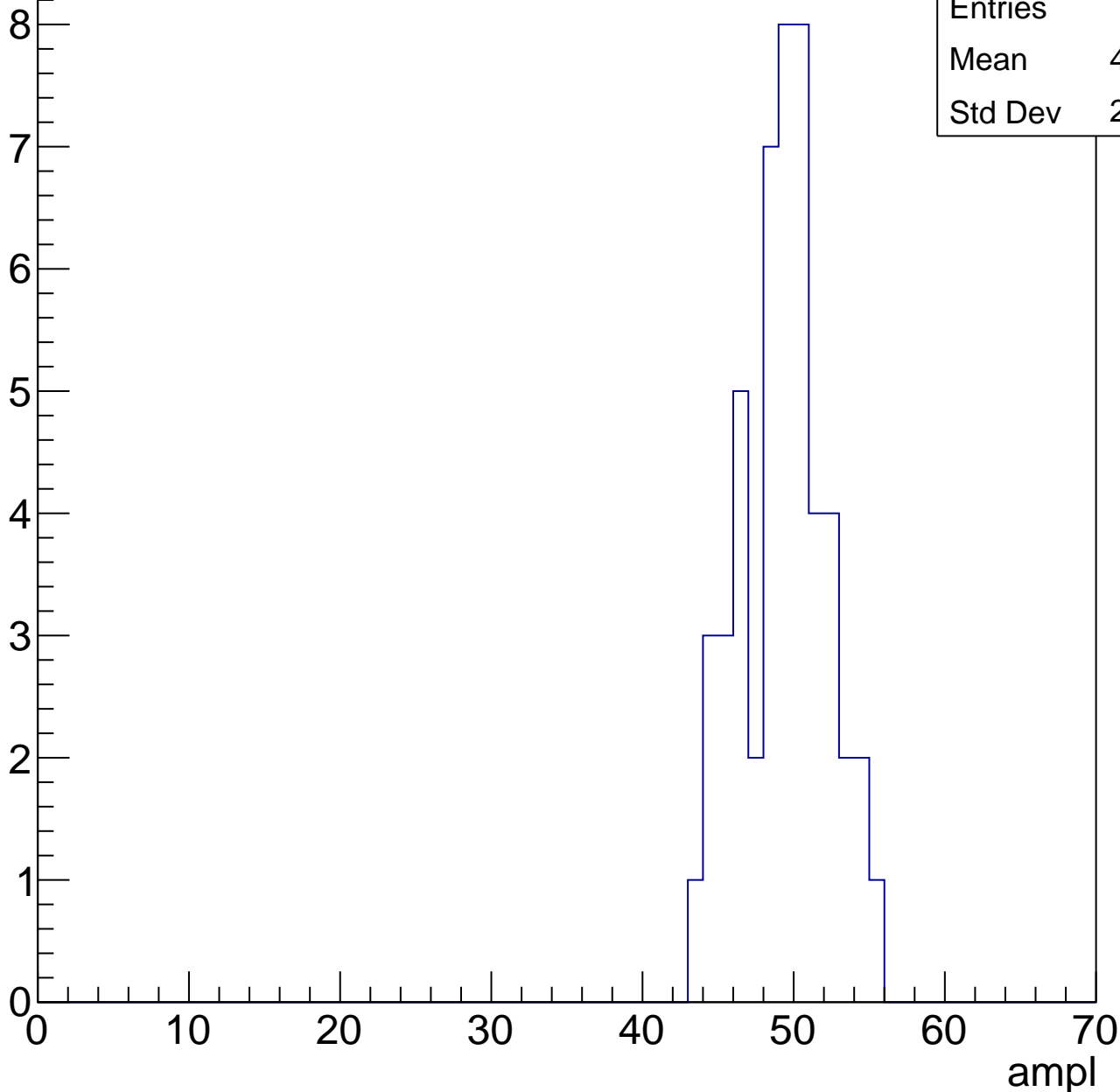


# B0L000S, U7-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	50
Mean	48.86
Std Dev	2.814

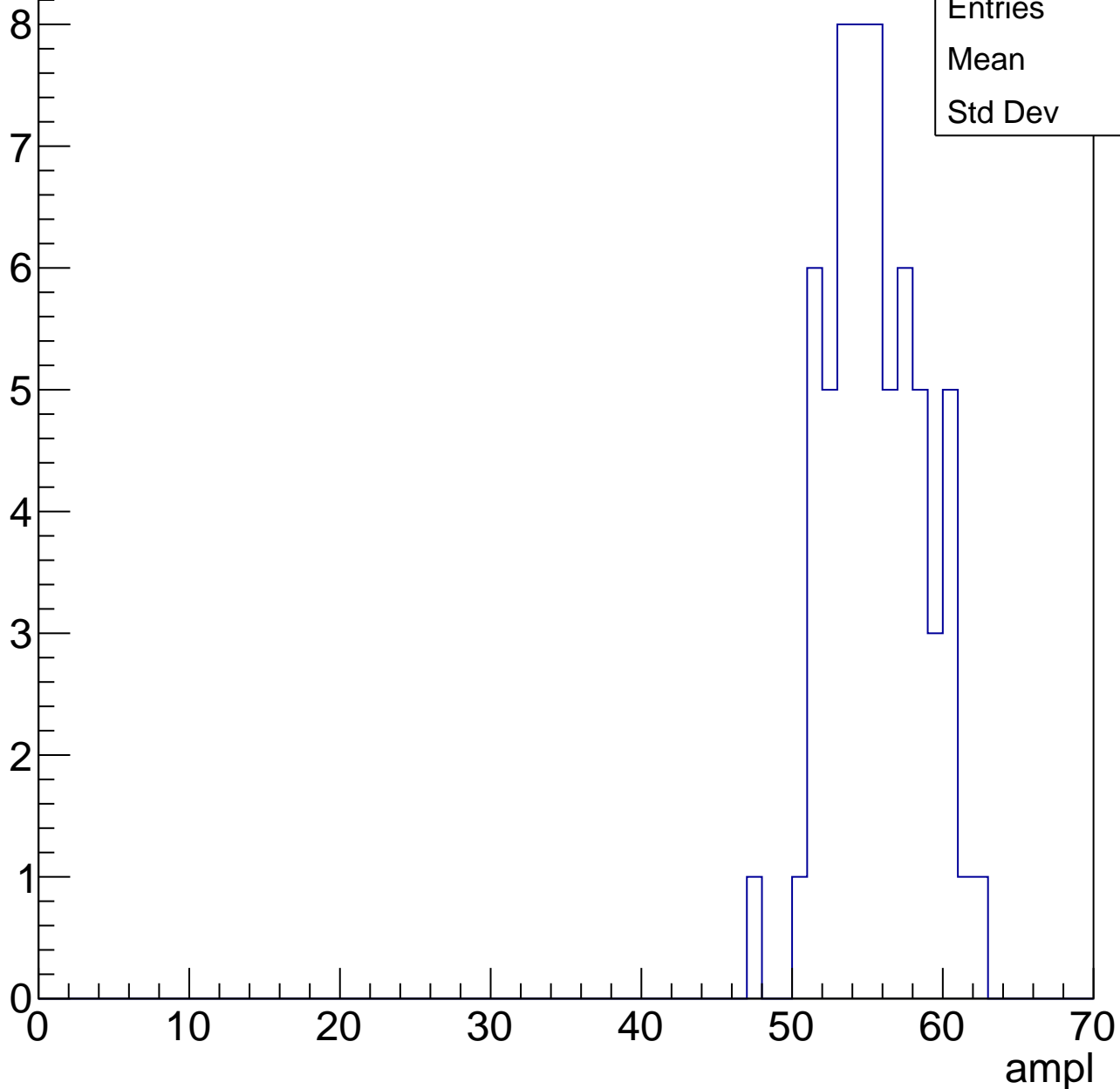


# B0L000S, U7-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	63
Mean	55.1
Std Dev	3.09

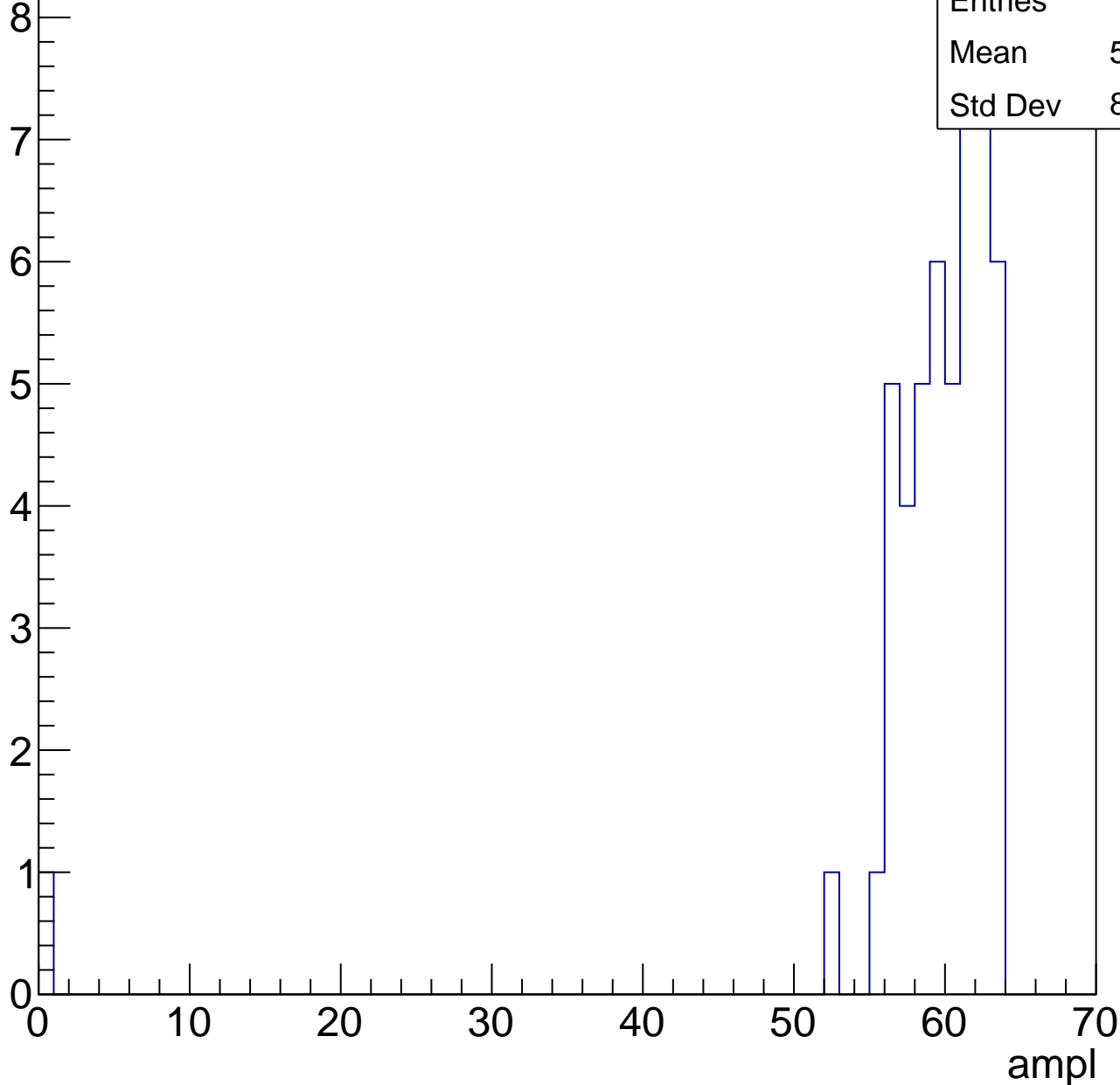


# B0L000S, U7-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

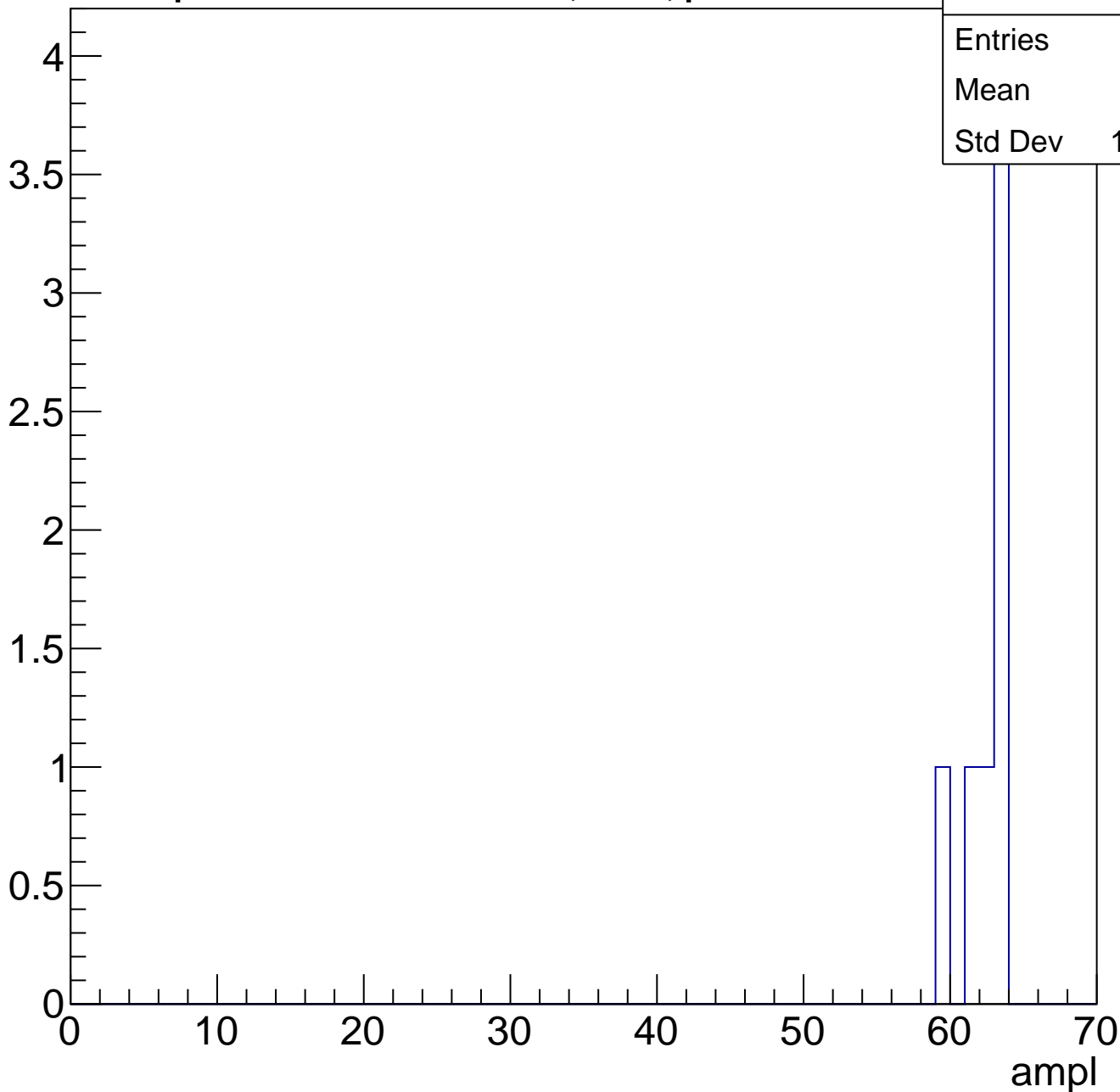
Entries	50
Mean	58.42
Std Dev	8.718



# B0L000S, U7-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L000S, U7-ch61, adc0

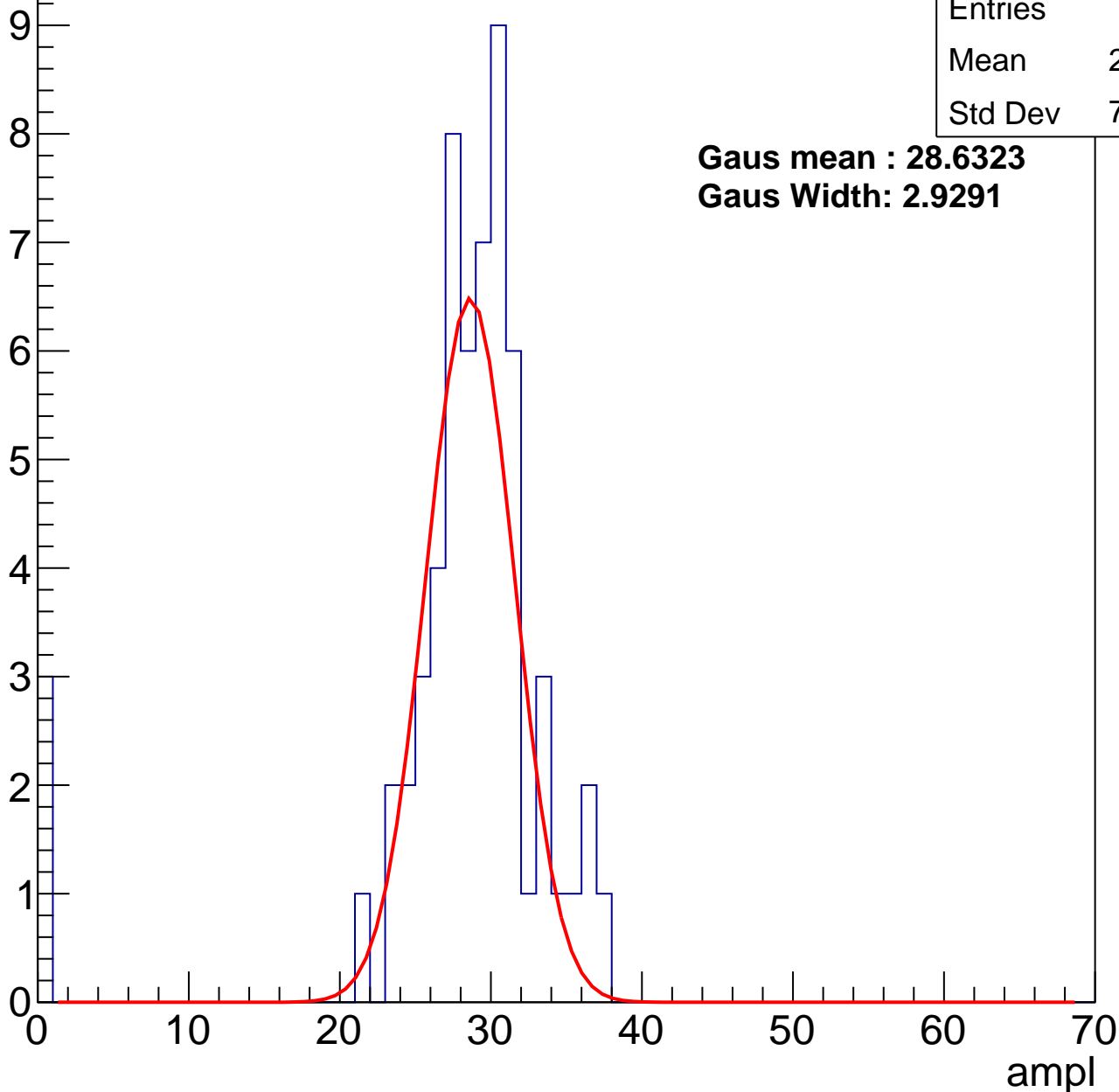
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	60
Mean	27.43
Std Dev	7.067

**Gaus mean : 28.6323**

**Gaus Width: 2.9291**



# B0L000S, U7-ch61, adc1

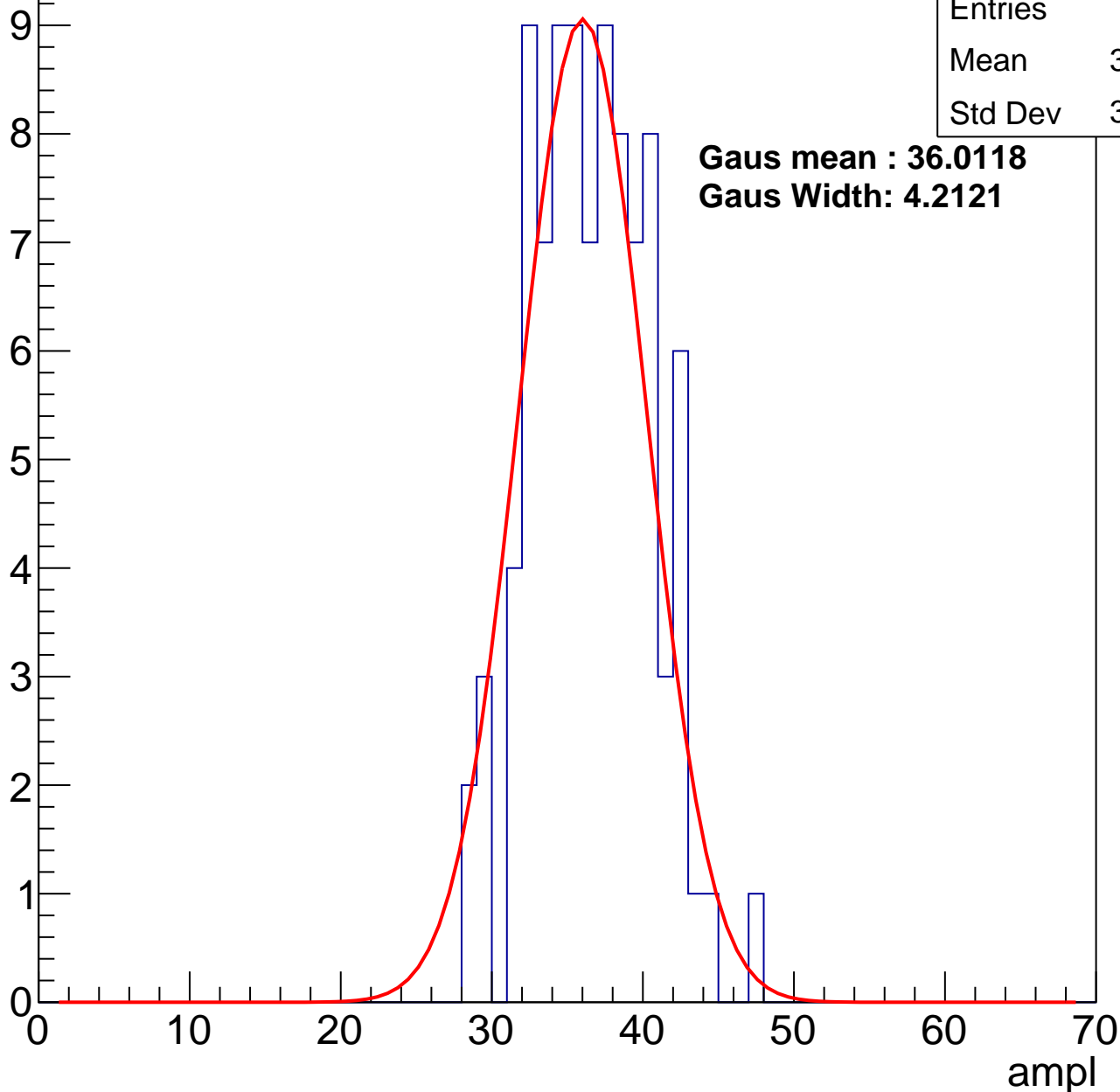
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	94
Mean	36.15
Std Dev	3.834

**Gaus mean : 36.0118**

**Gaus Width: 4.2121**



# B0L000S, U7-ch61, adc2

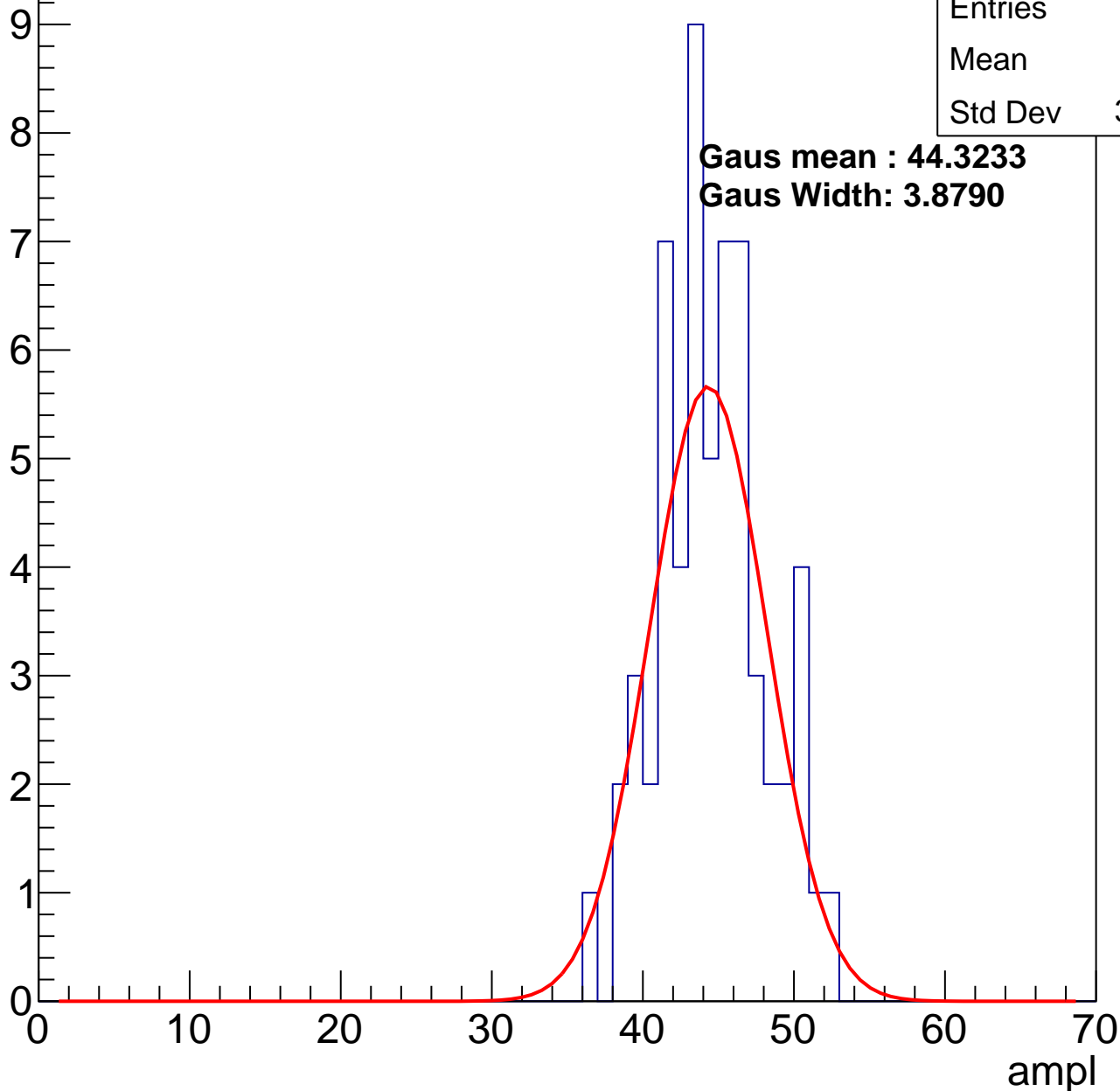
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	60
Mean	44.1
Std Dev	3.491

**Gaus mean : 44.3233**

**Gaus Width: 3.8790**



# B0L000S, U7-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

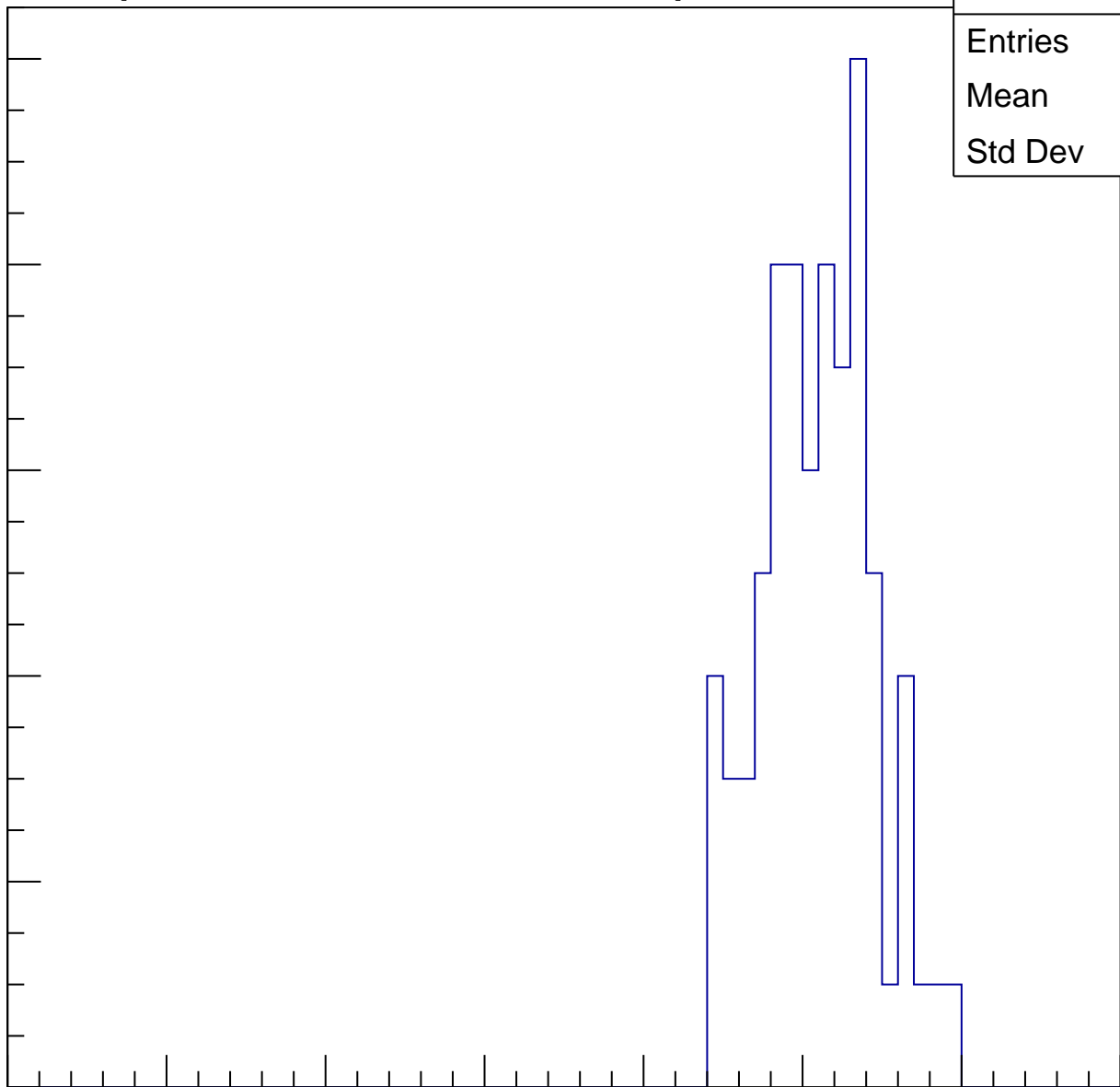
Entries	75
Mean	50.47
Std Dev	3.473

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

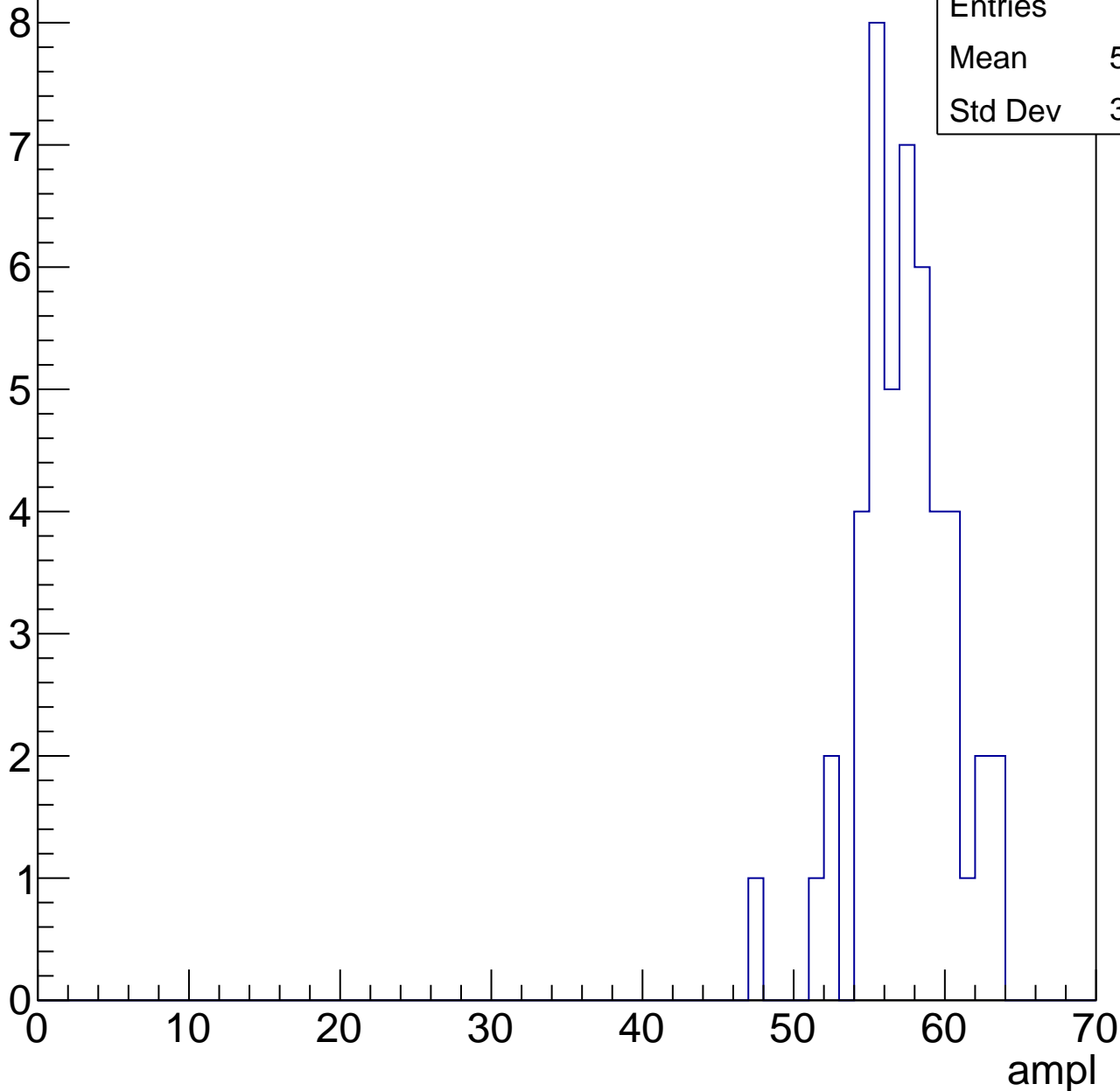


# B0L000S, U7-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	47
Mean	56.85
Std Dev	3.108

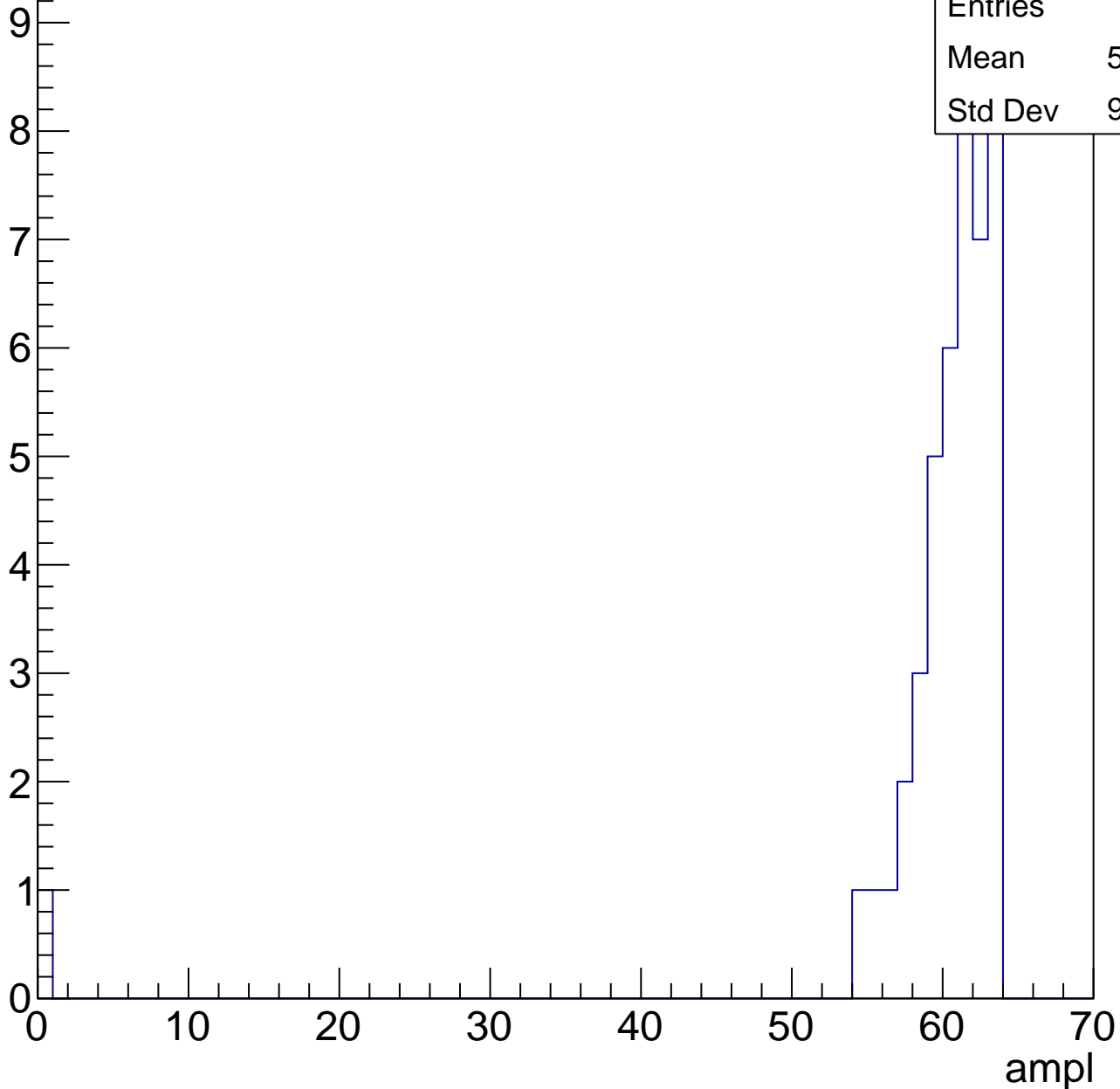


# B0L000S, U7-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	44
Mean	58.98
Std Dev	9.263



# B0L000S, U7-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L000S, U7-ch62, adc0

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	64
Mean	27.2
Std Dev	4.627

**Gaus mean : 28.3624**

**Gaus Width: 3.0577**

Entry

10  
8  
6  
4  
2  
0

ampl

0

10

20

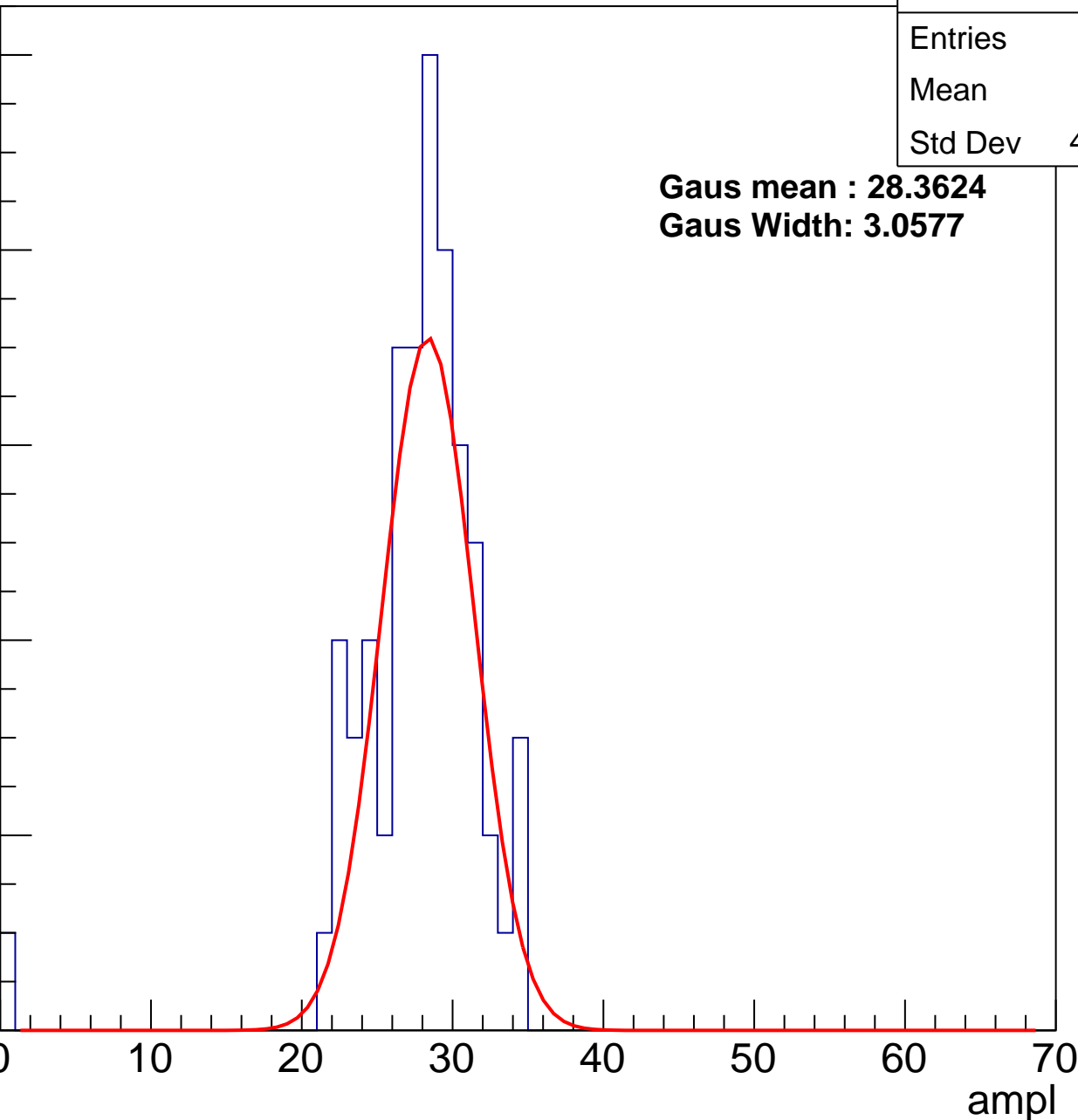
30

40

50

60

70



# B0L000S, U7-ch62, adc1

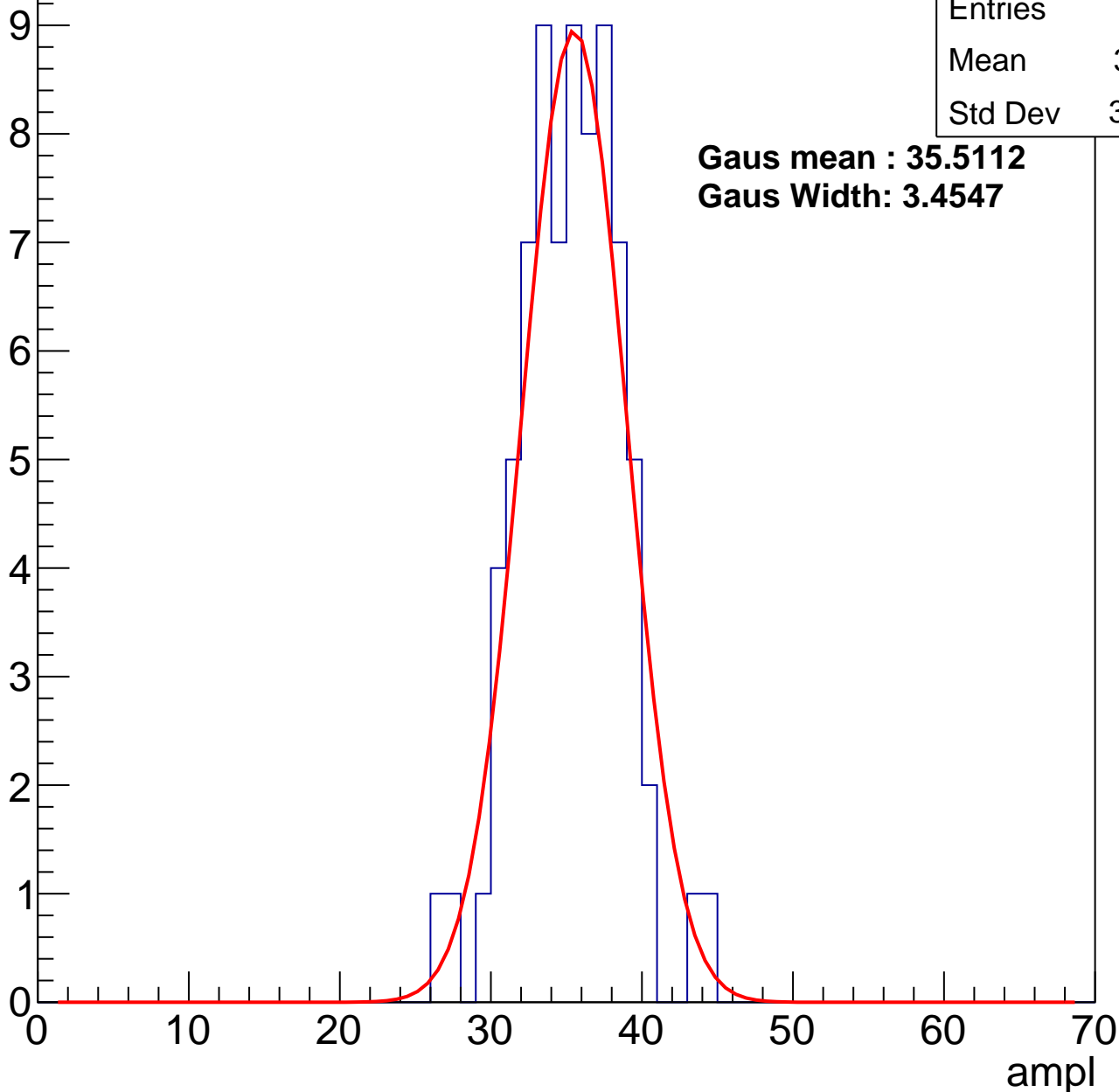
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	77
Mean	34.81
Std Dev	3.315

**Gaus mean : 35.5112**

**Gaus Width: 3.4547**



# B0L000S, U7-ch62, adc2

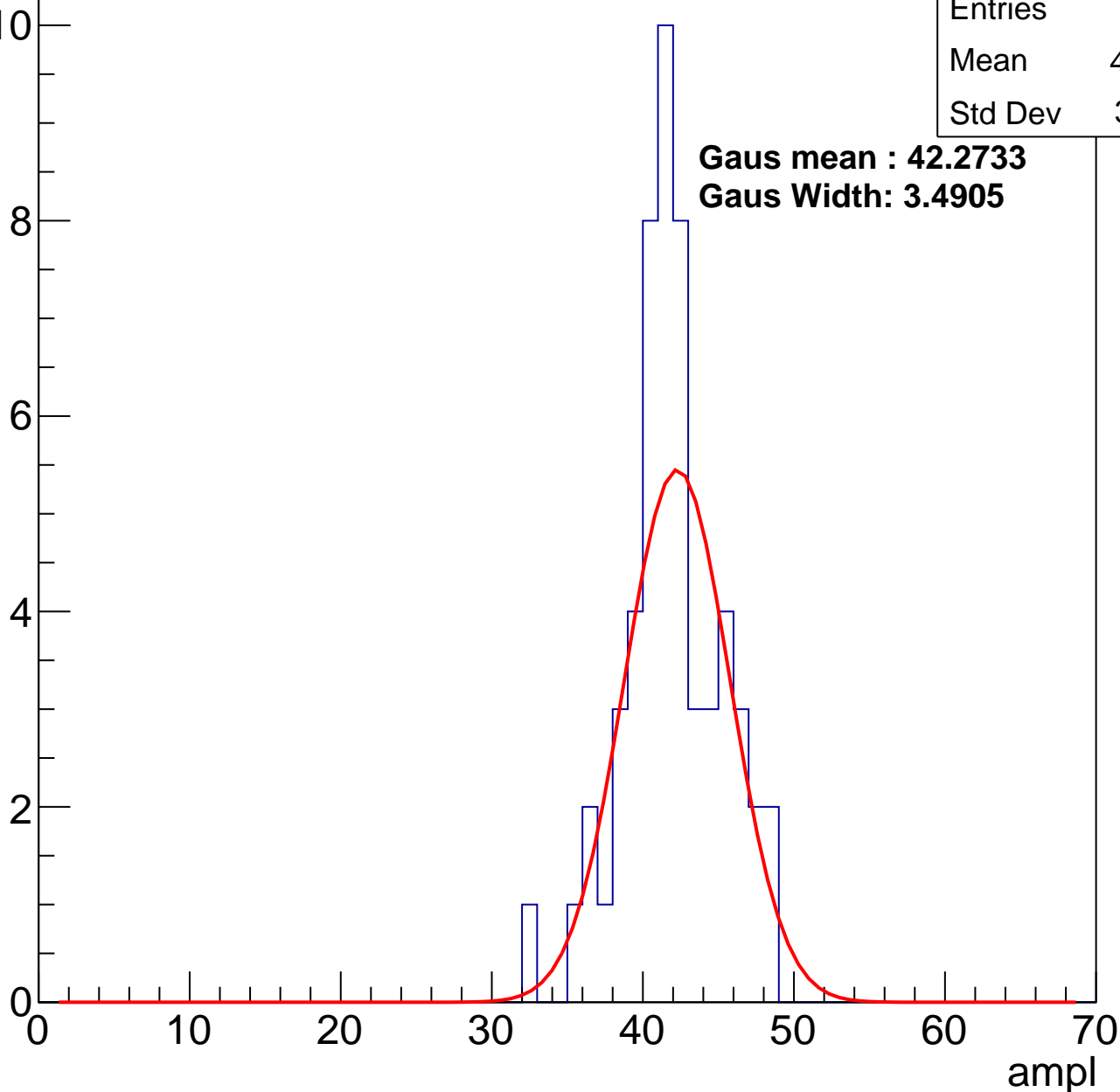
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	55
Mean	41.47
Std Dev	3.241

**Gaus mean : 42.2733**

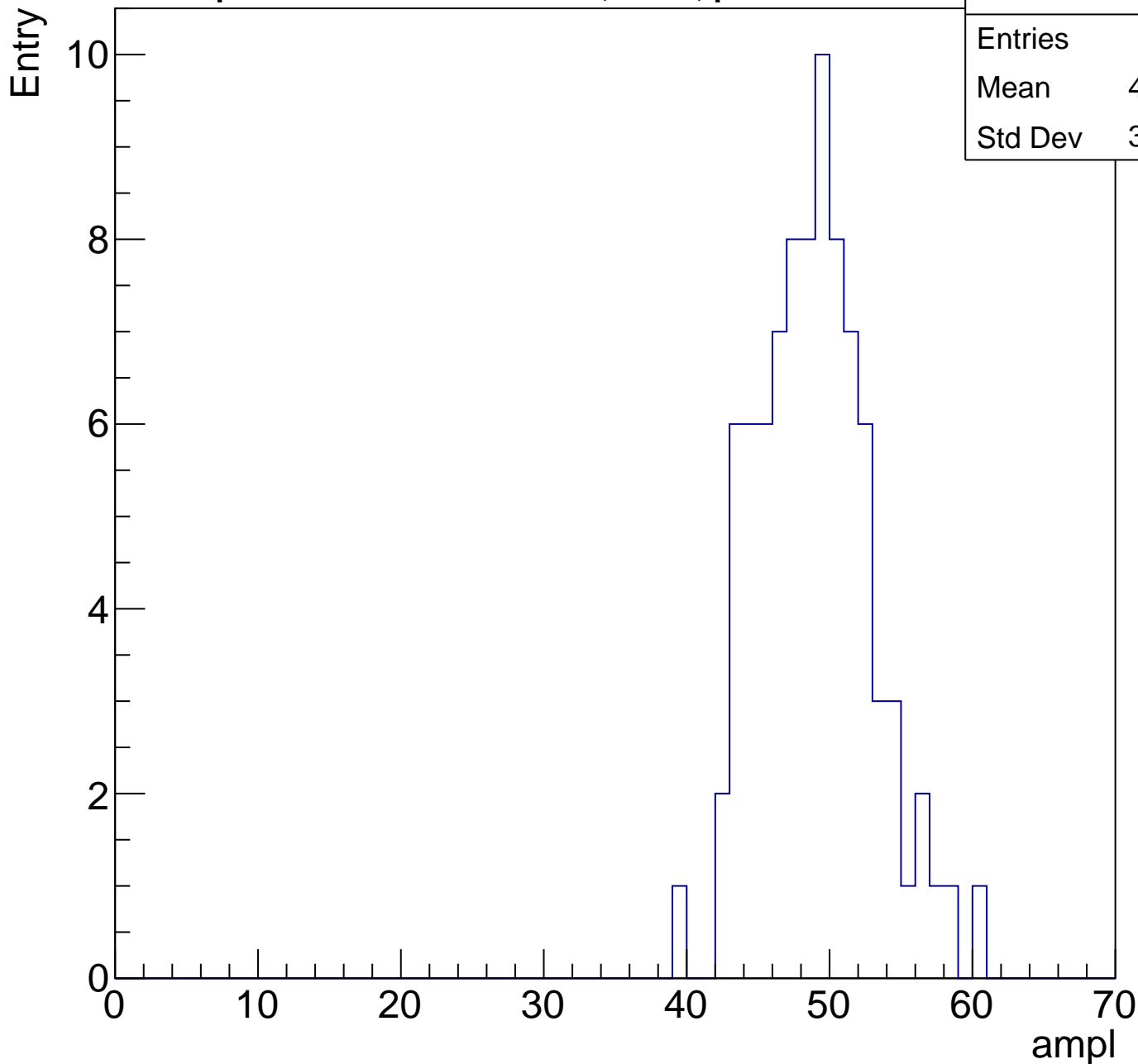
**Gaus Width: 3.4905**



# B0L000S, U7-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	87
Mean	48.49
Std Dev	3.945

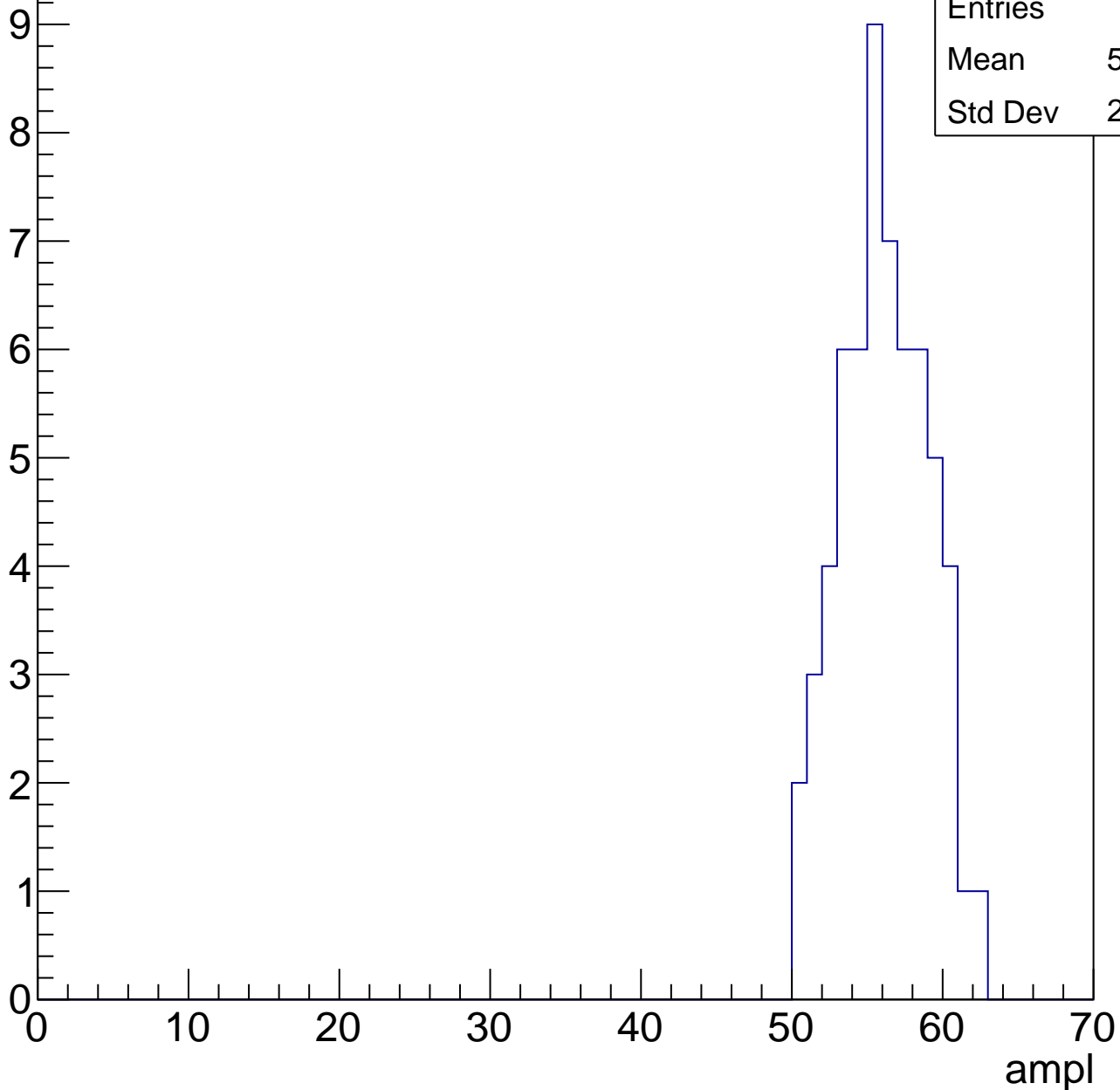


# B0L000S, U7-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	60
Mean	55.63
Std Dev	2.858

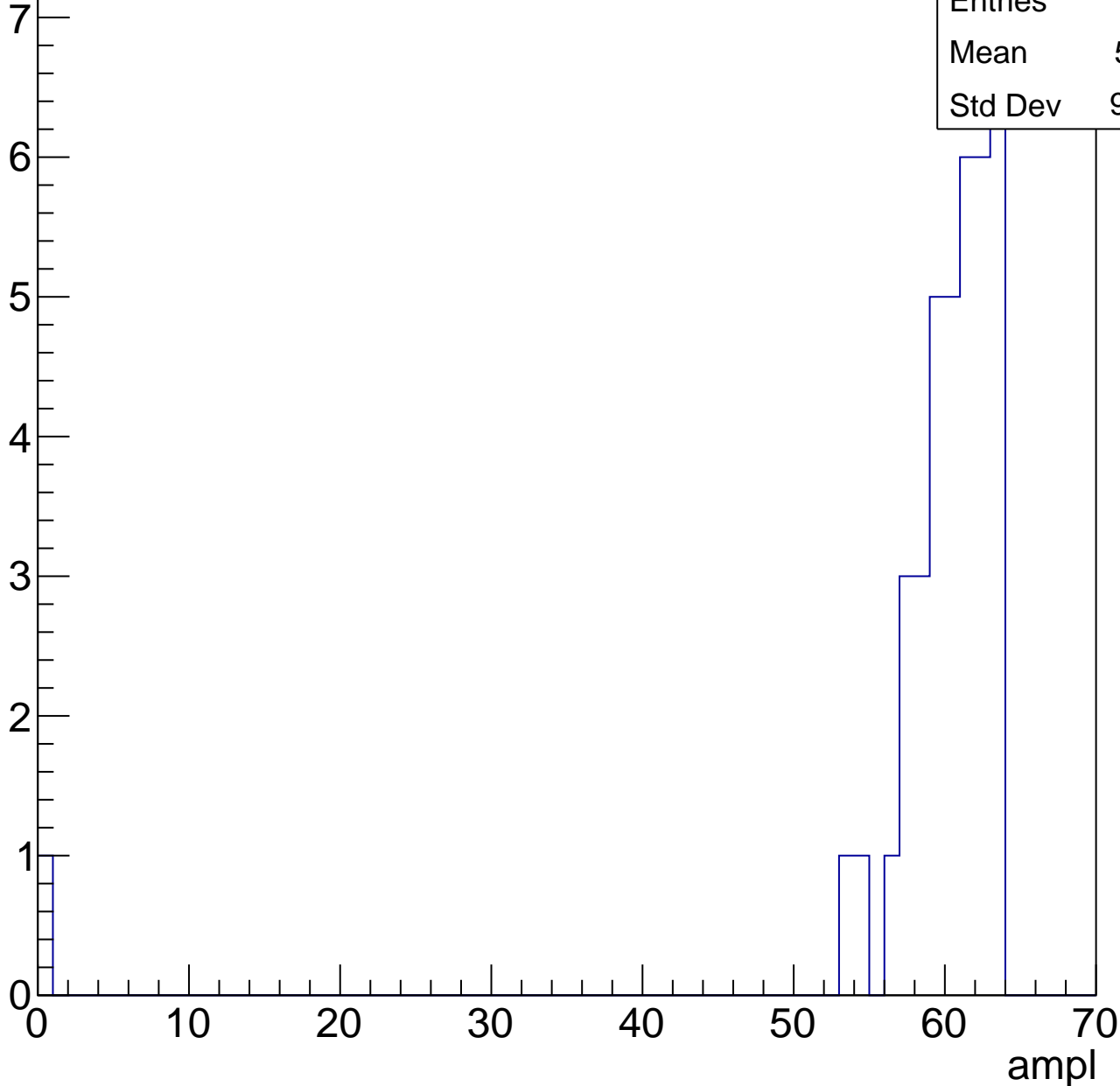


# B0L000S, U7-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

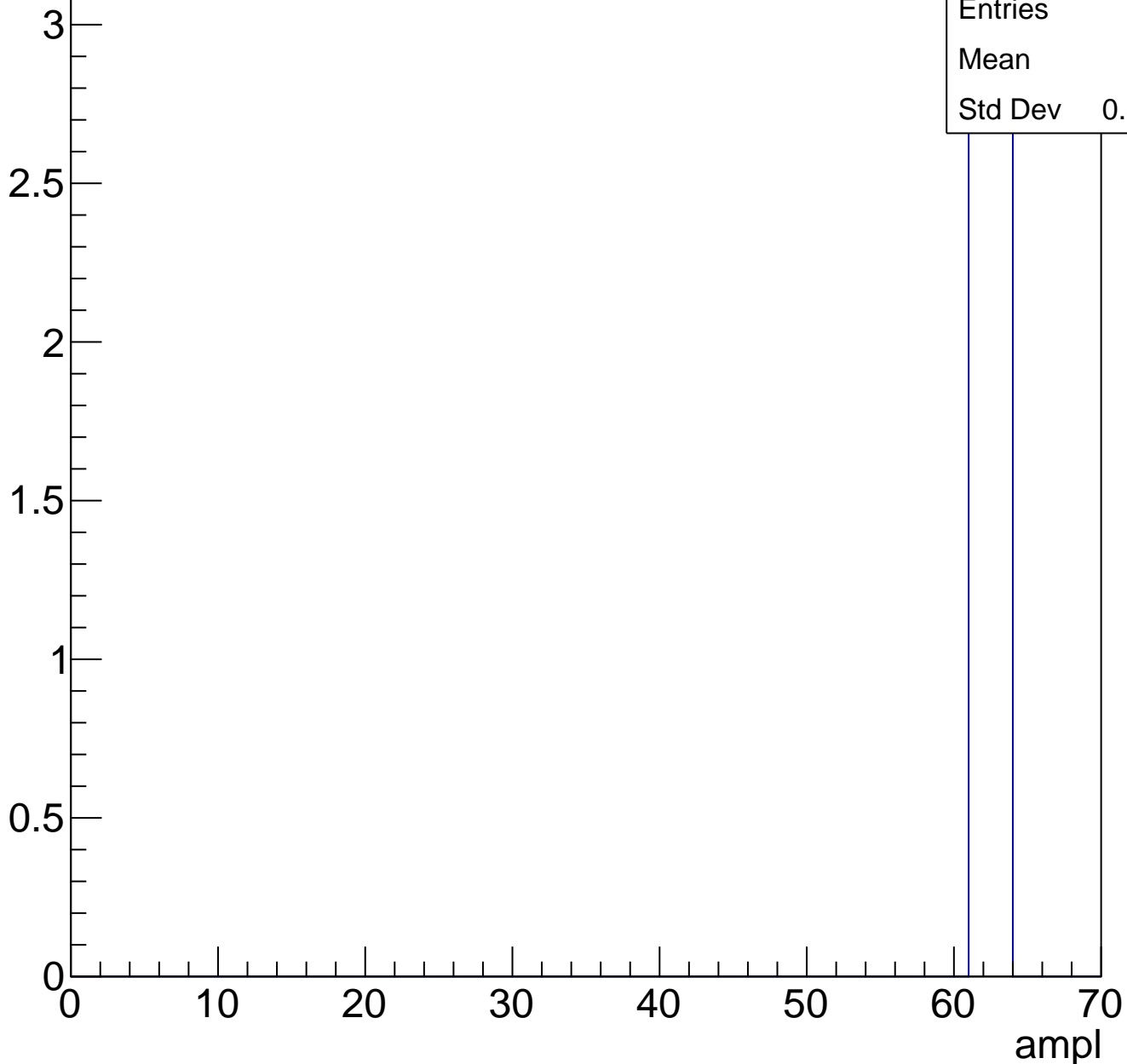
Entries	39
Mean	58.51
Std Dev	9.808



# B0L000S, U7-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L000S, U7-ch63, adc0

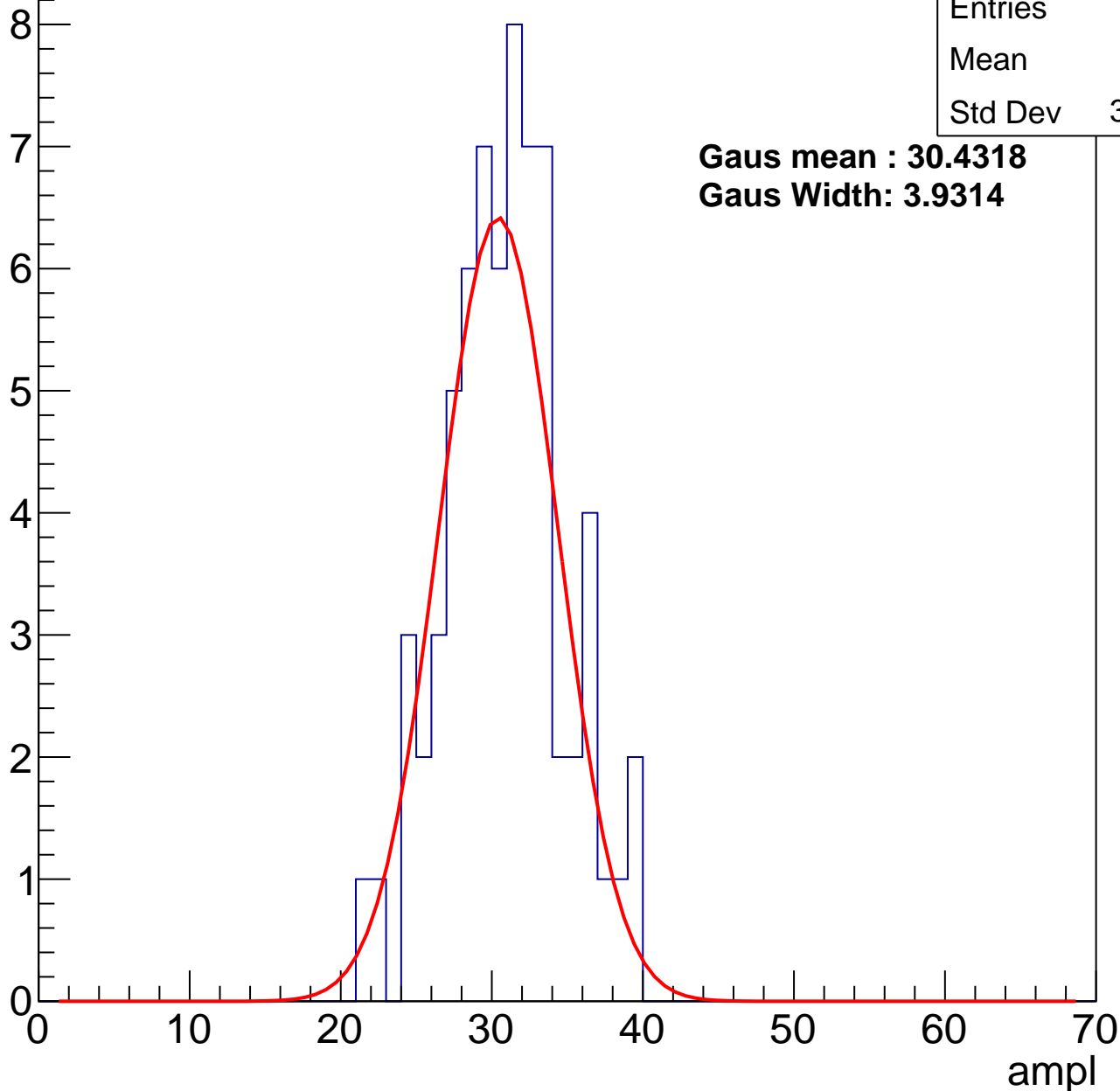
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	68
Mean	30.4
Std Dev	3.866

**Gaus mean : 30.4318**

**Gaus Width: 3.9314**



# B0L000S, U7-ch63, adc1

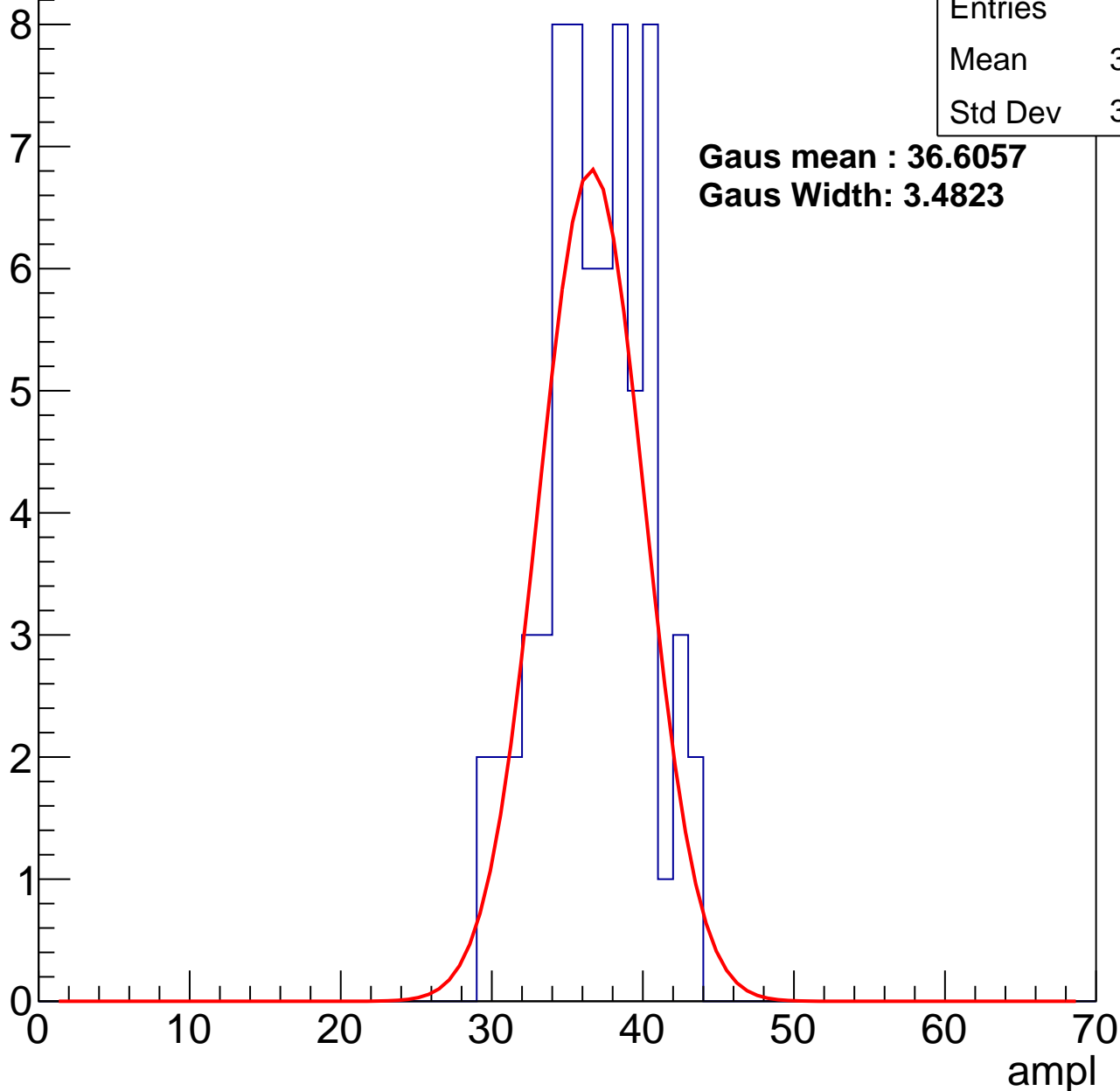
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	67
Mean	36.37
Std Dev	3.385

**Gaus mean : 36.6057**

**Gaus Width: 3.4823**



# B0L000S, U7-ch63, adc2

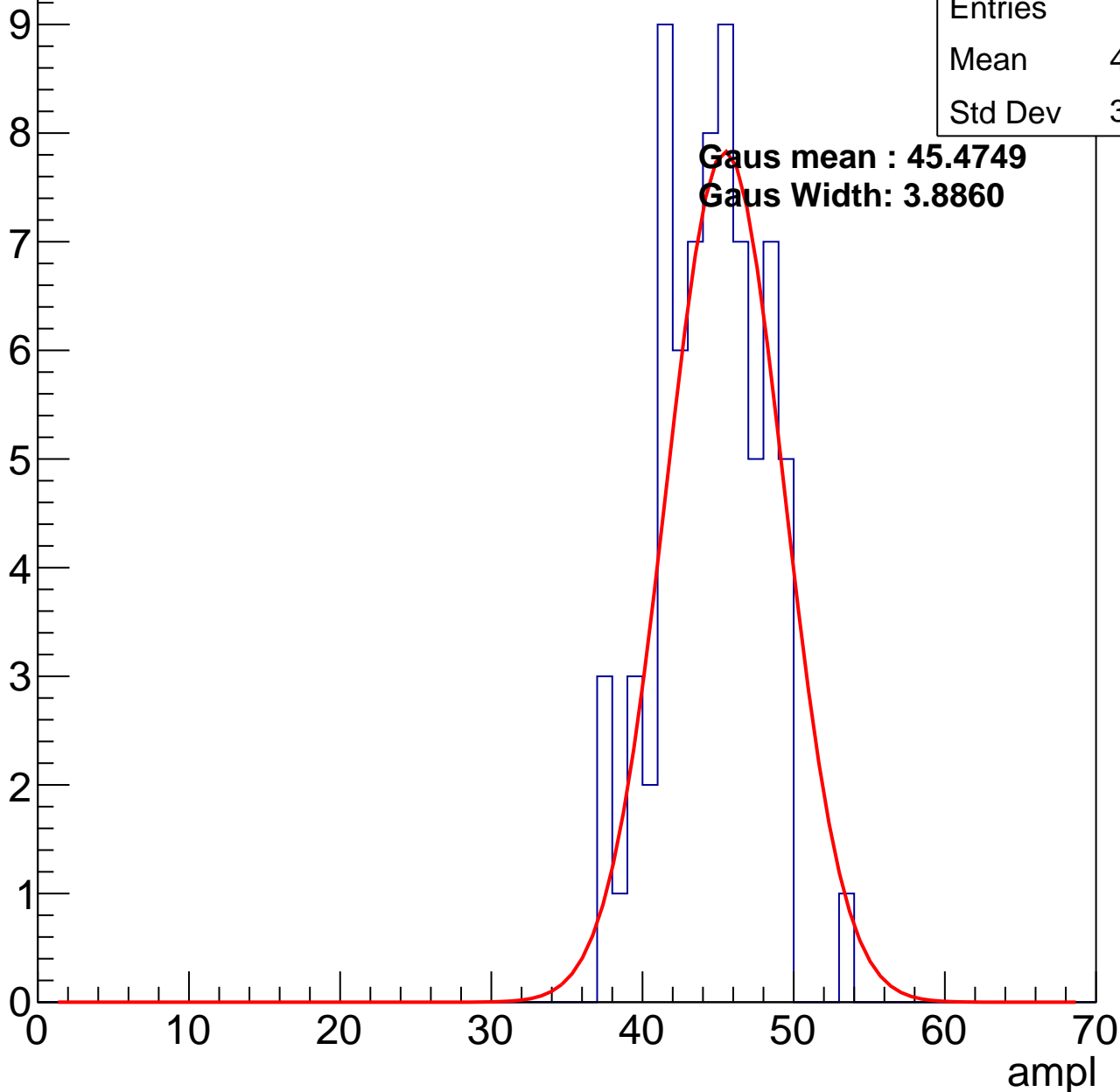
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	73
Mean	44.05
Std Dev	3.314

**Gaus mean : 45.4749**

**Gaus Width: 3.8860**

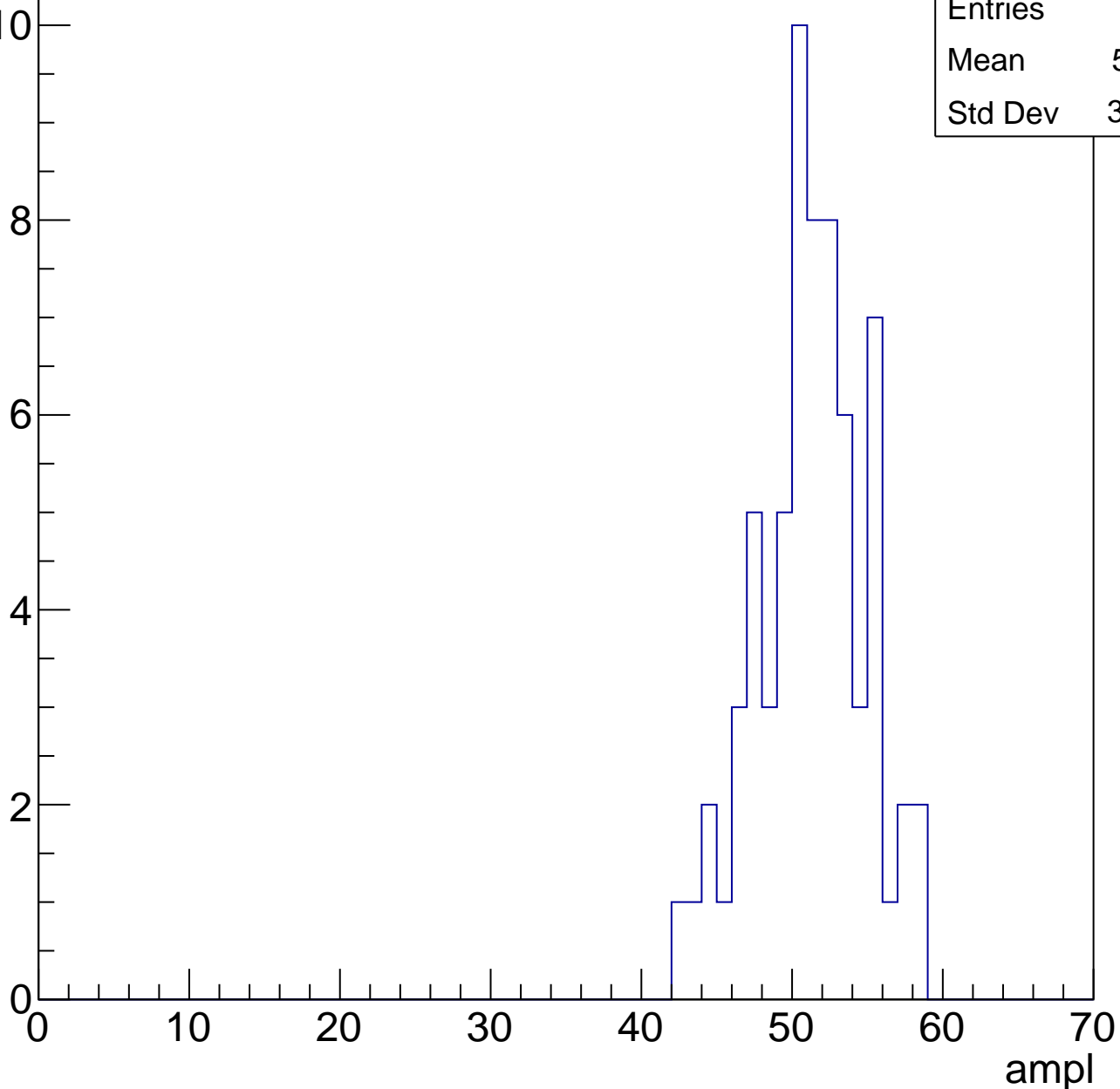


# B0L000S, U7-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	68
Mean	50.81
Std Dev	3.545

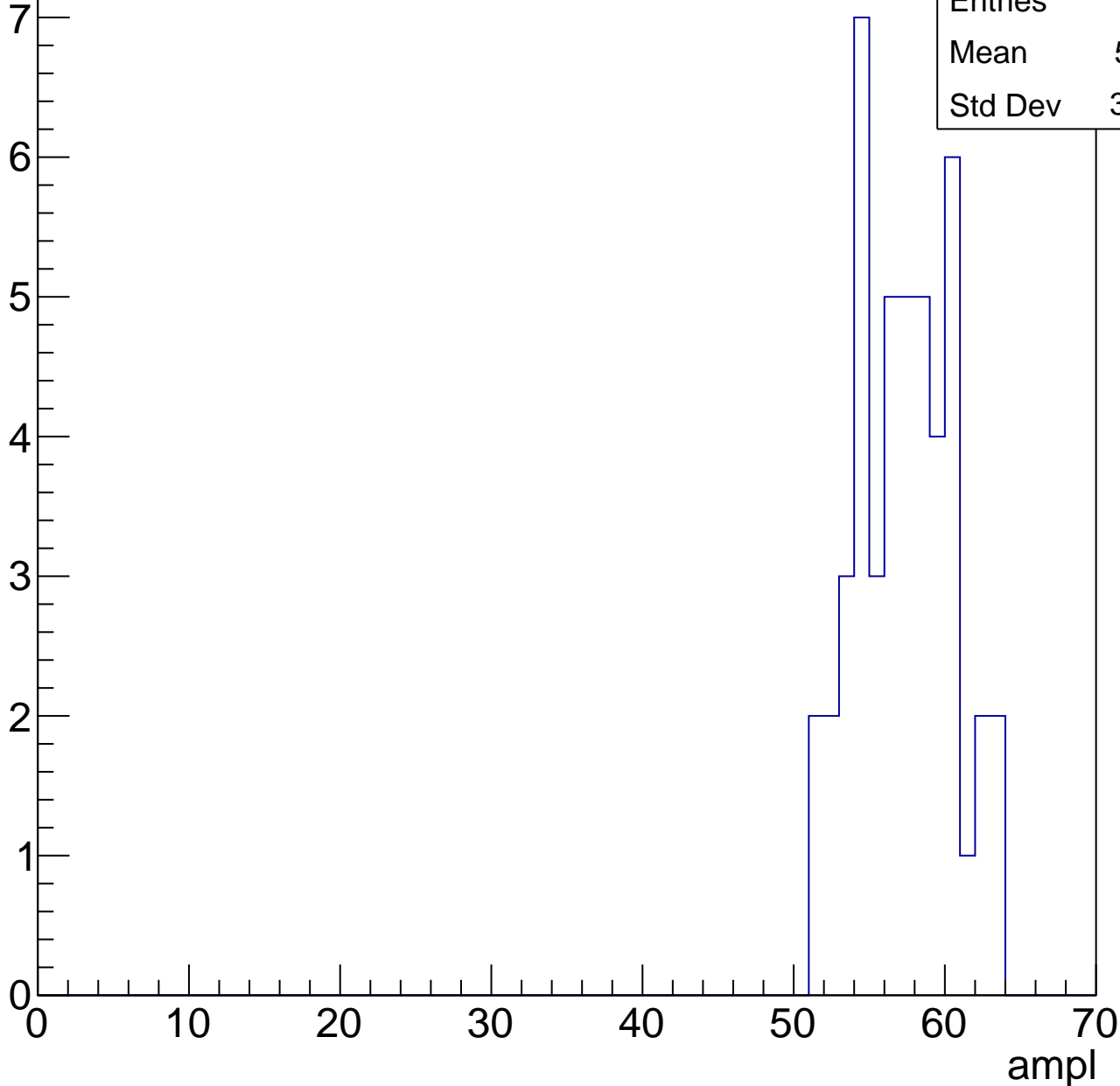


# B0L000S, U7-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	47
Mean	56.81
Std Dev	3.133

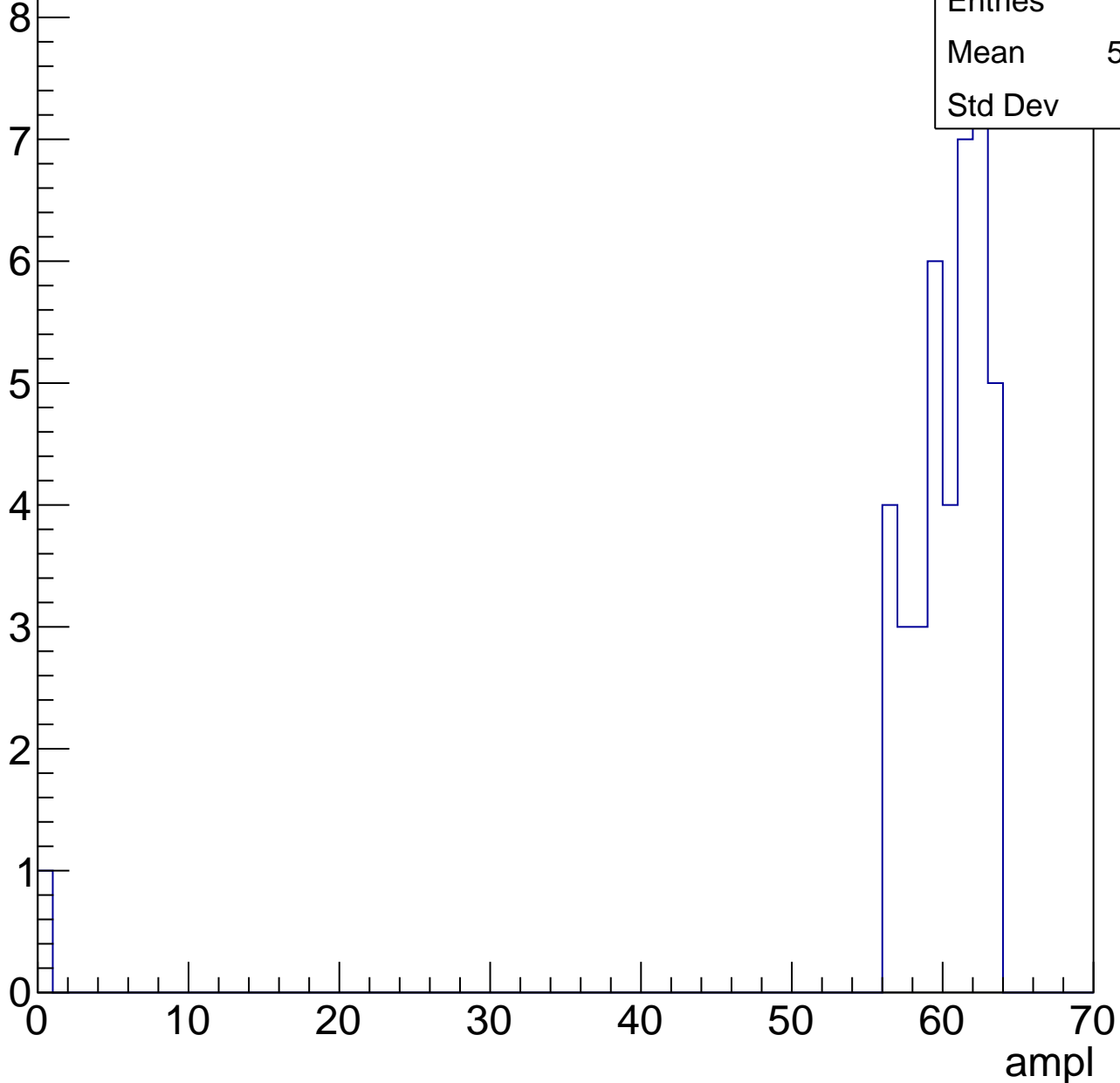


# B0L000S, U7-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

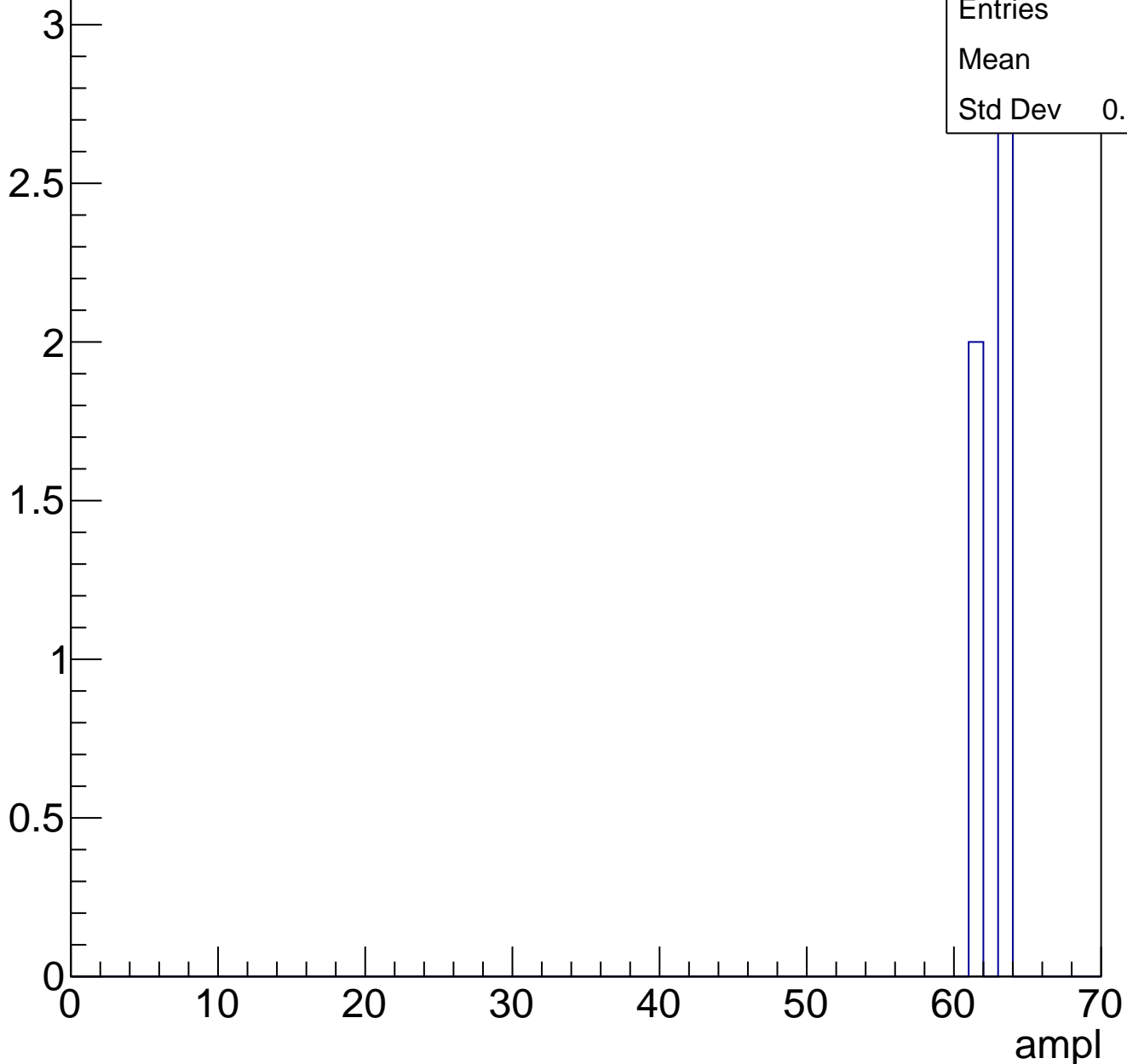
Entries	41
Mean	58.56
Std Dev	9.51



# B0L000S, U7-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L000S, U7-ch64, adc0

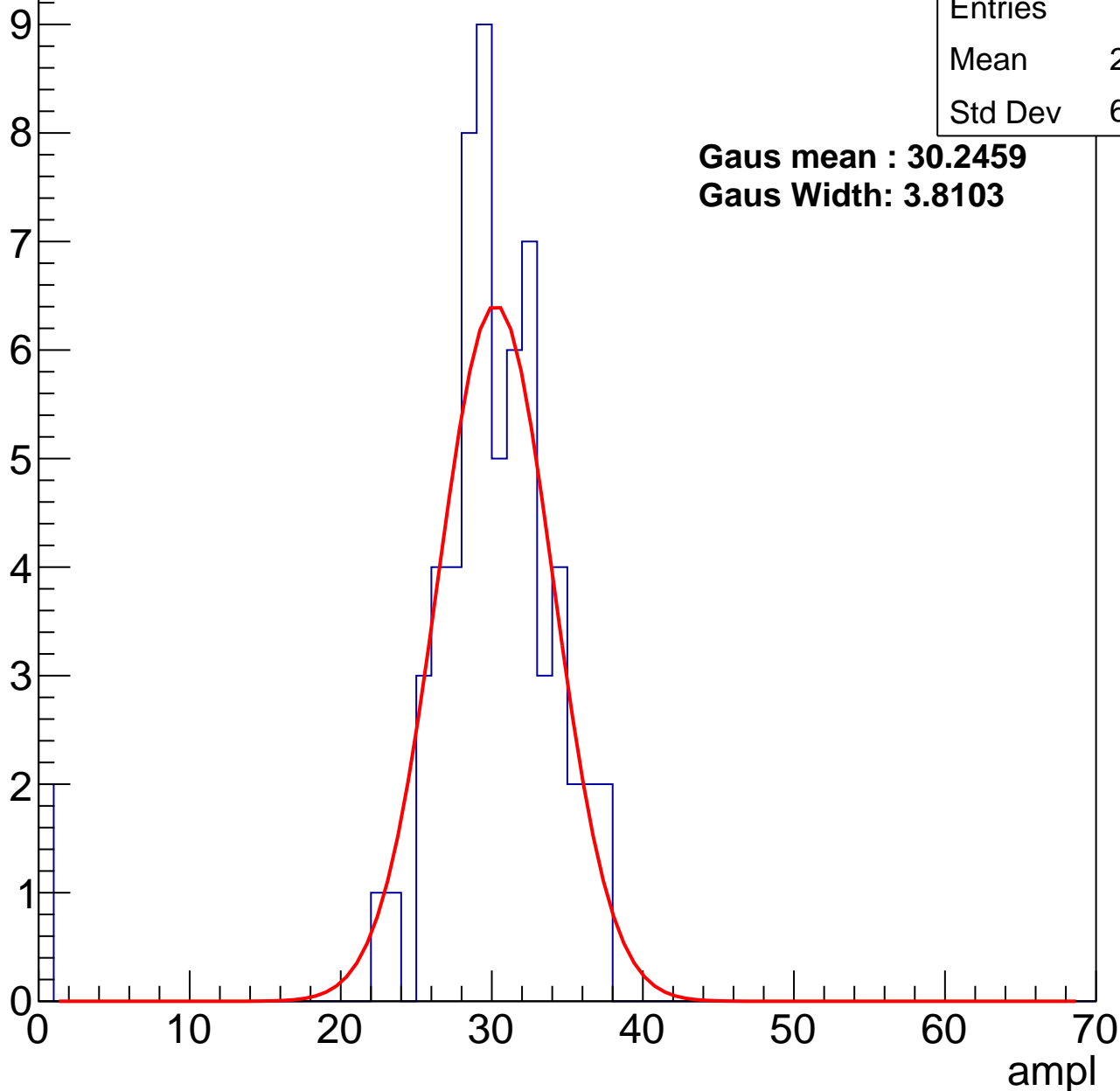
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	63
Mean	29.02
Std Dev	6.189

**Gaus mean : 30.2459**

**Gaus Width: 3.8103**



# B0L000S, U7-ch64, adc1

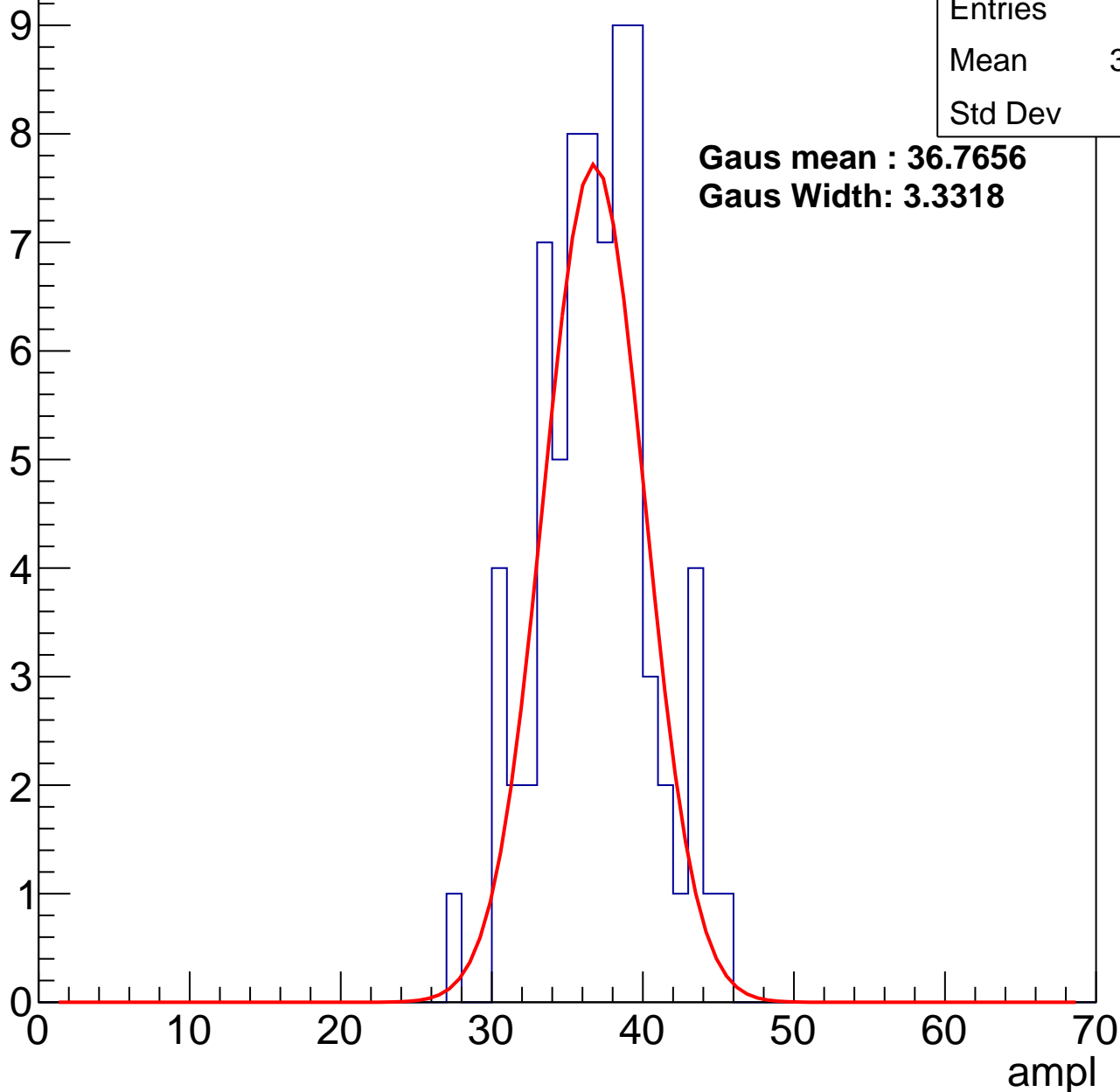
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	74
Mean	36.47
Std Dev	3.64

**Gaus mean : 36.7656**

**Gaus Width: 3.3318**



# B0L000S, U7-ch64, adc2

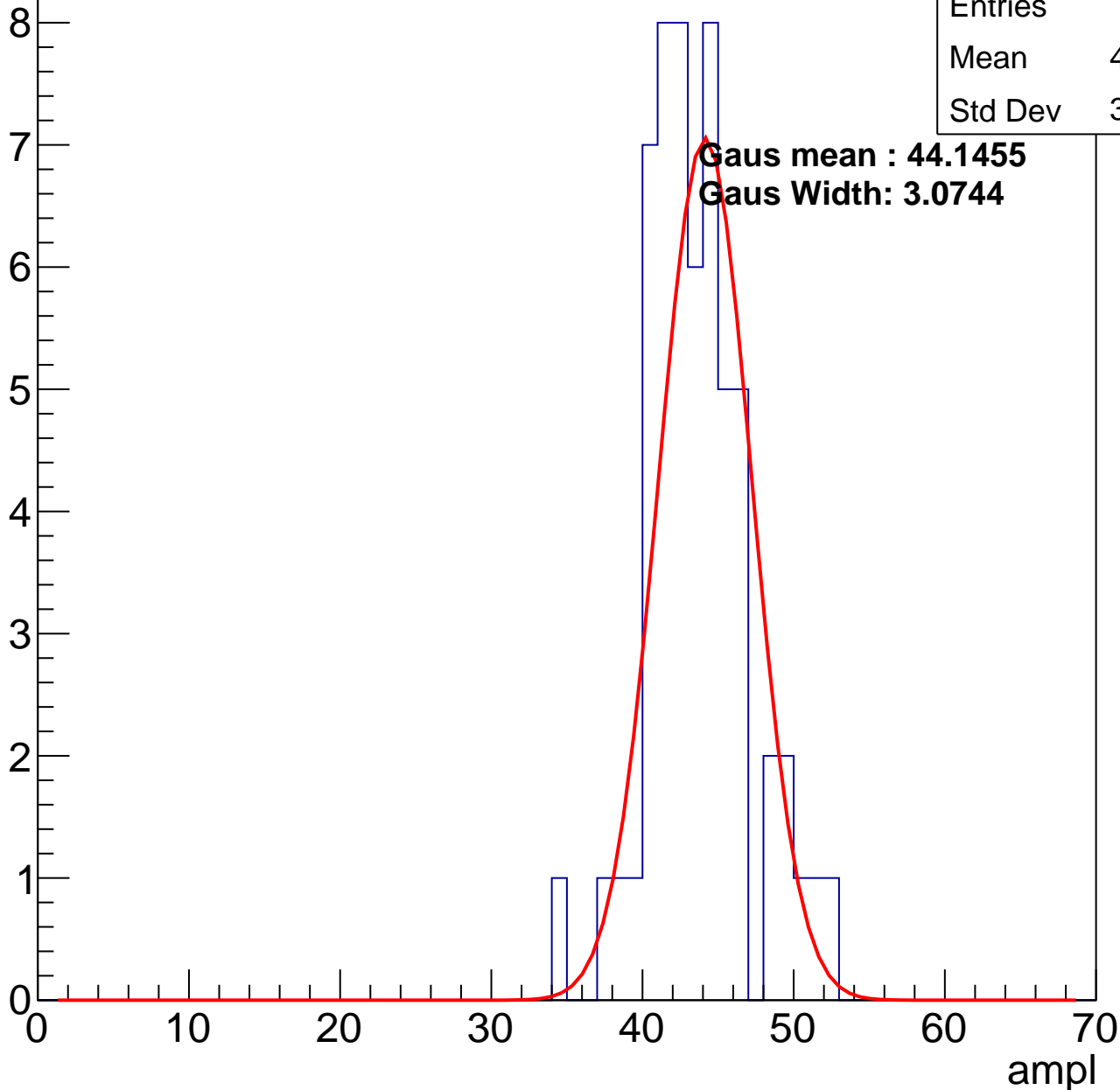
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	58
Mean	43.17
Std Dev	3.343

**Gaus mean : 44.1455**

**Gaus Width: 3.0744**



# B0L000S, U7-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

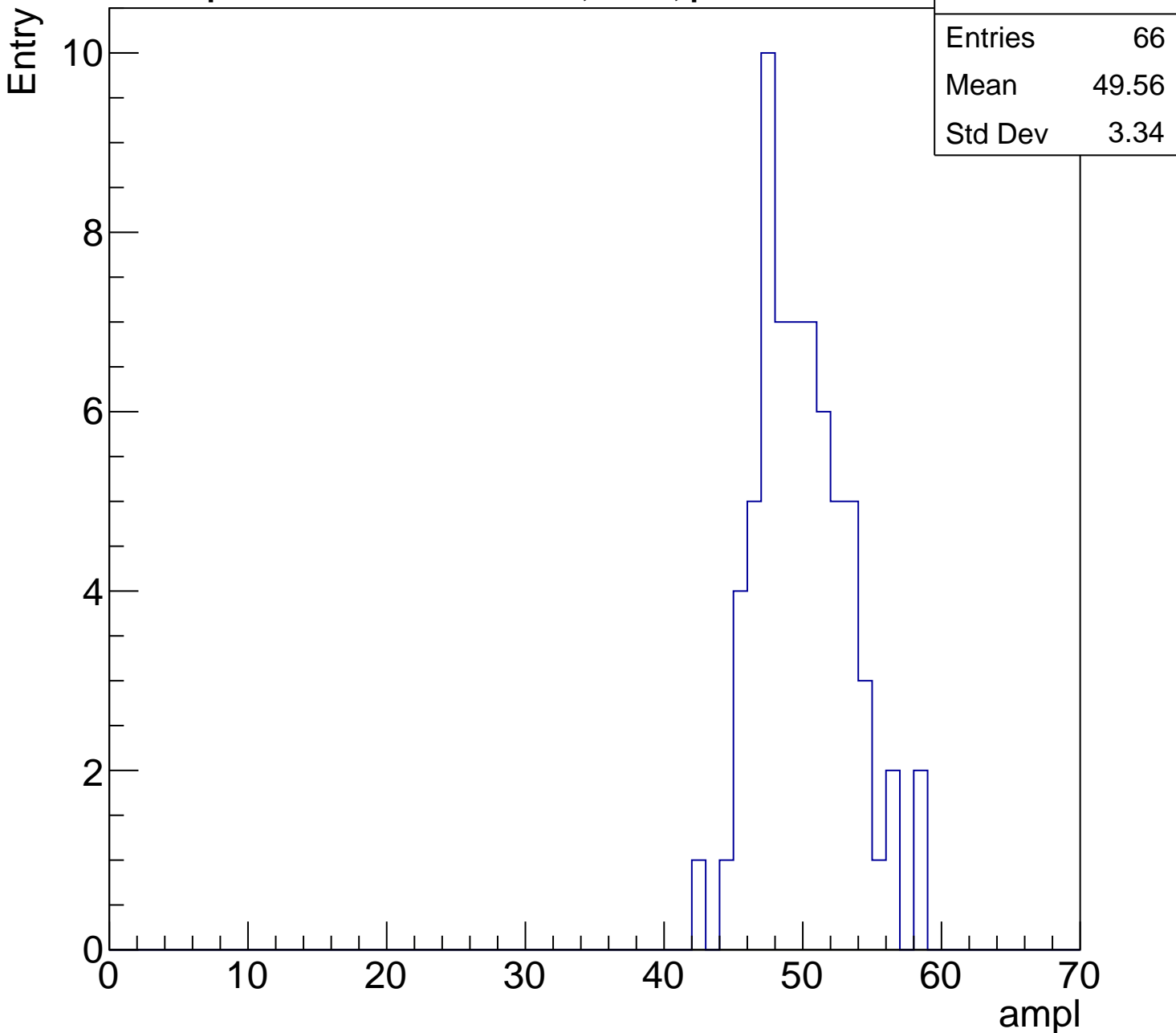
Entries	66
Mean	49.56
Std Dev	3.34

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

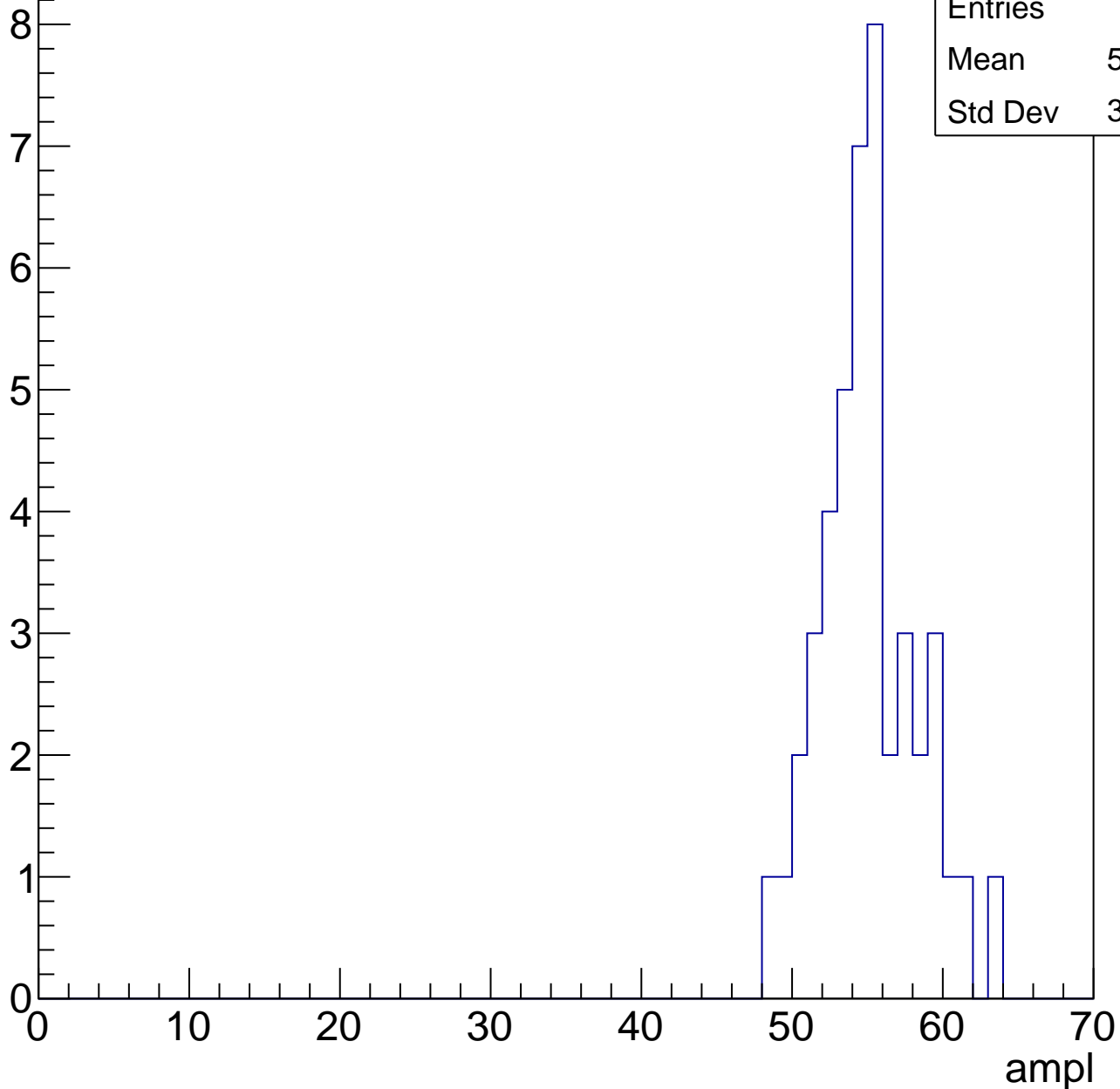
ampl



# B0L000S, U7-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	44
Mean	54.57
Std Dev	3.172

# B0L000S, U7-ch64, adc5

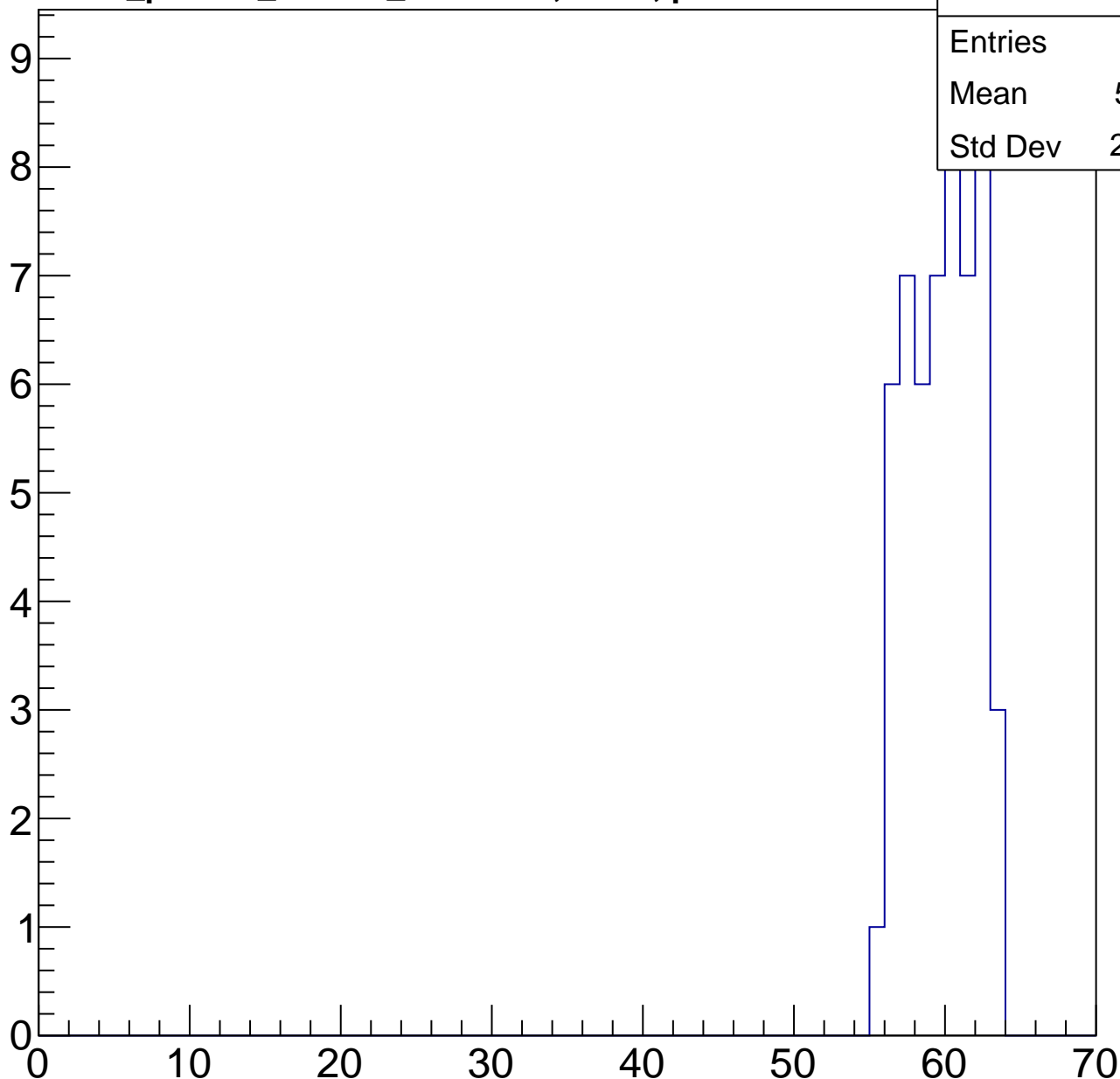
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	54
Mean	59.31
Std Dev	2.176

ampl

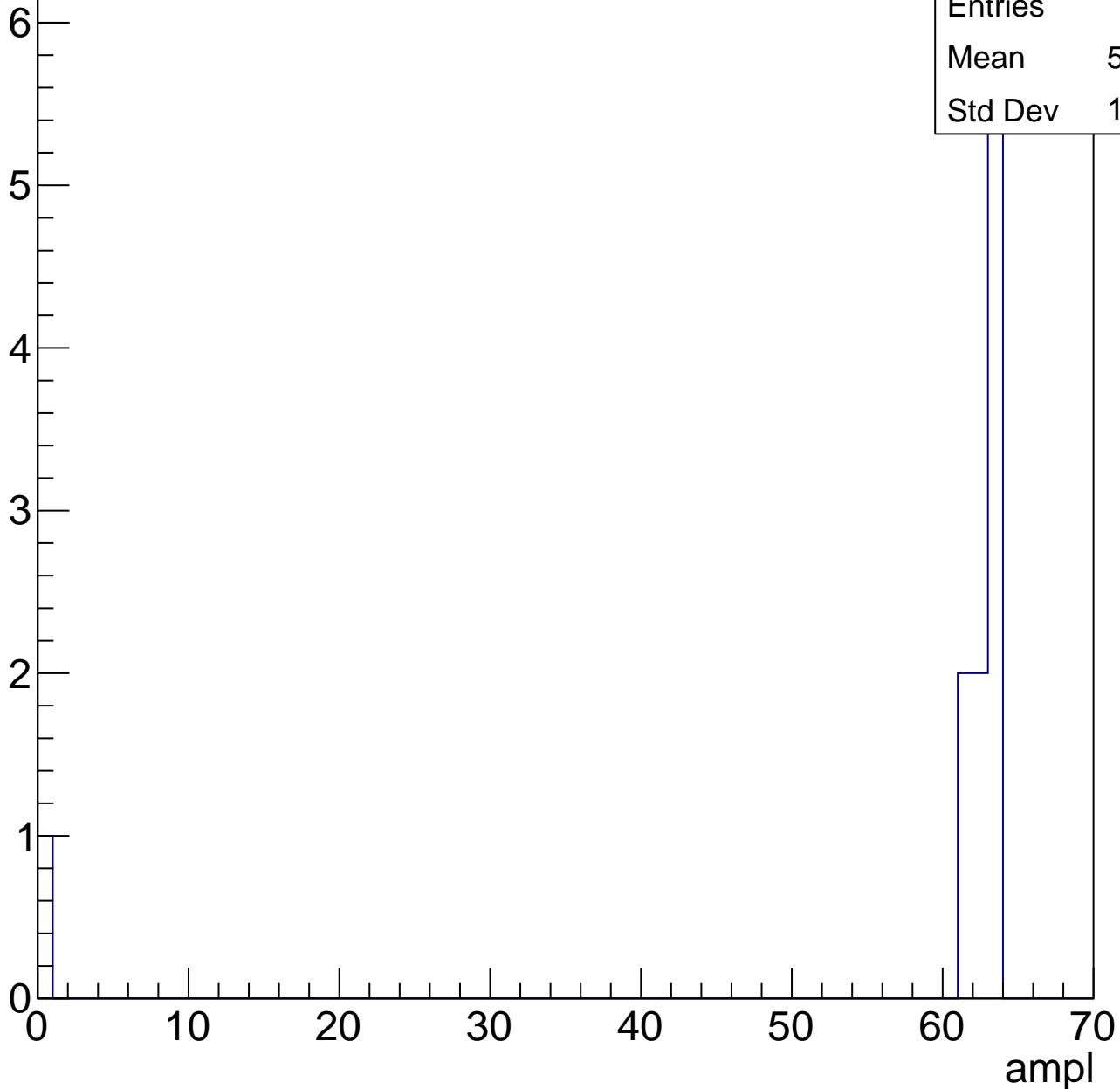


# B0L000S, U7-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	11
Mean	56.73
Std Dev	17.95





# B0L000S, U7-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch65, adc0

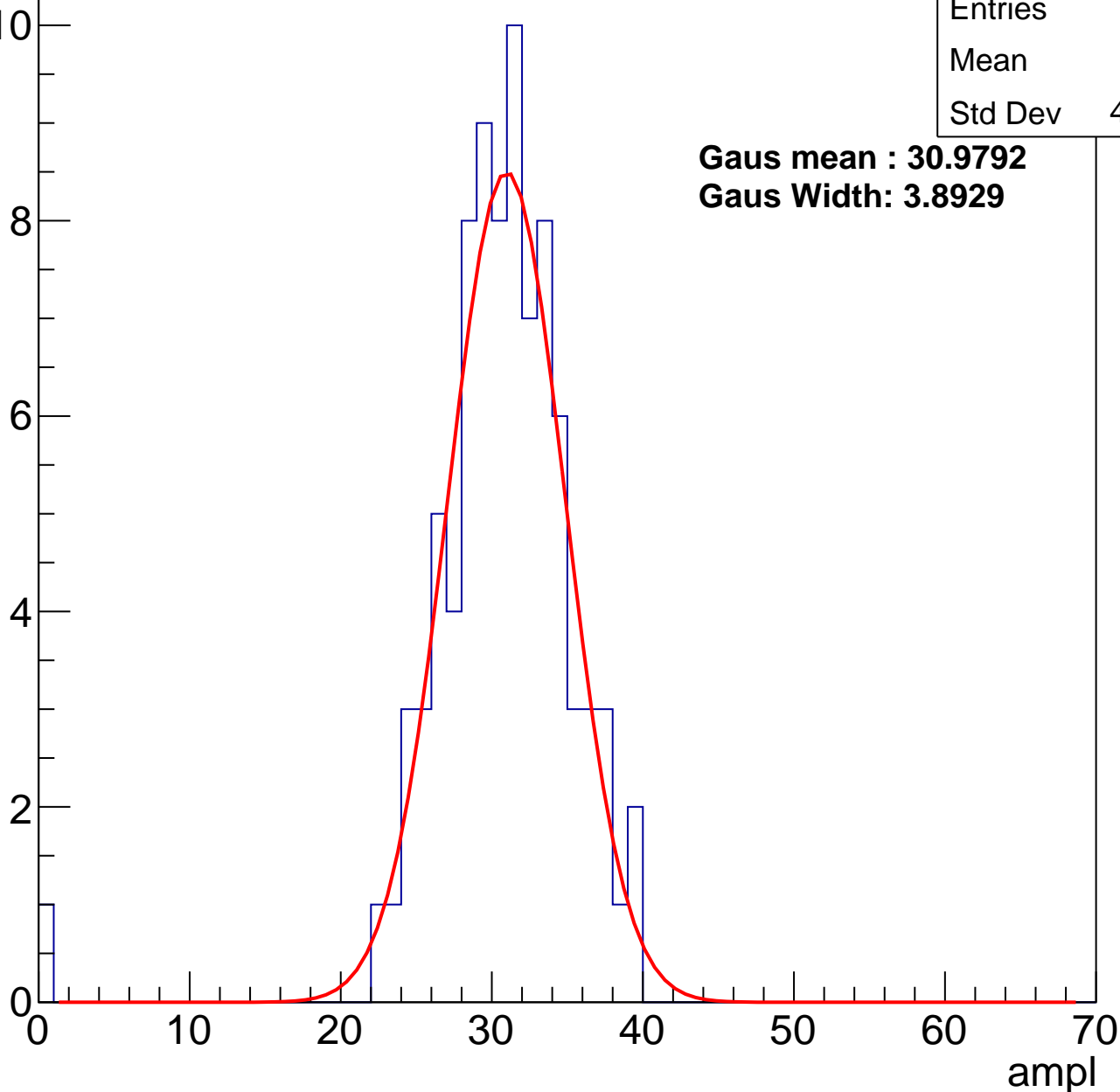
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	86
Mean	30.2
Std Dev	4.955

**Gaus mean : 30.9792**

**Gaus Width: 3.8929**



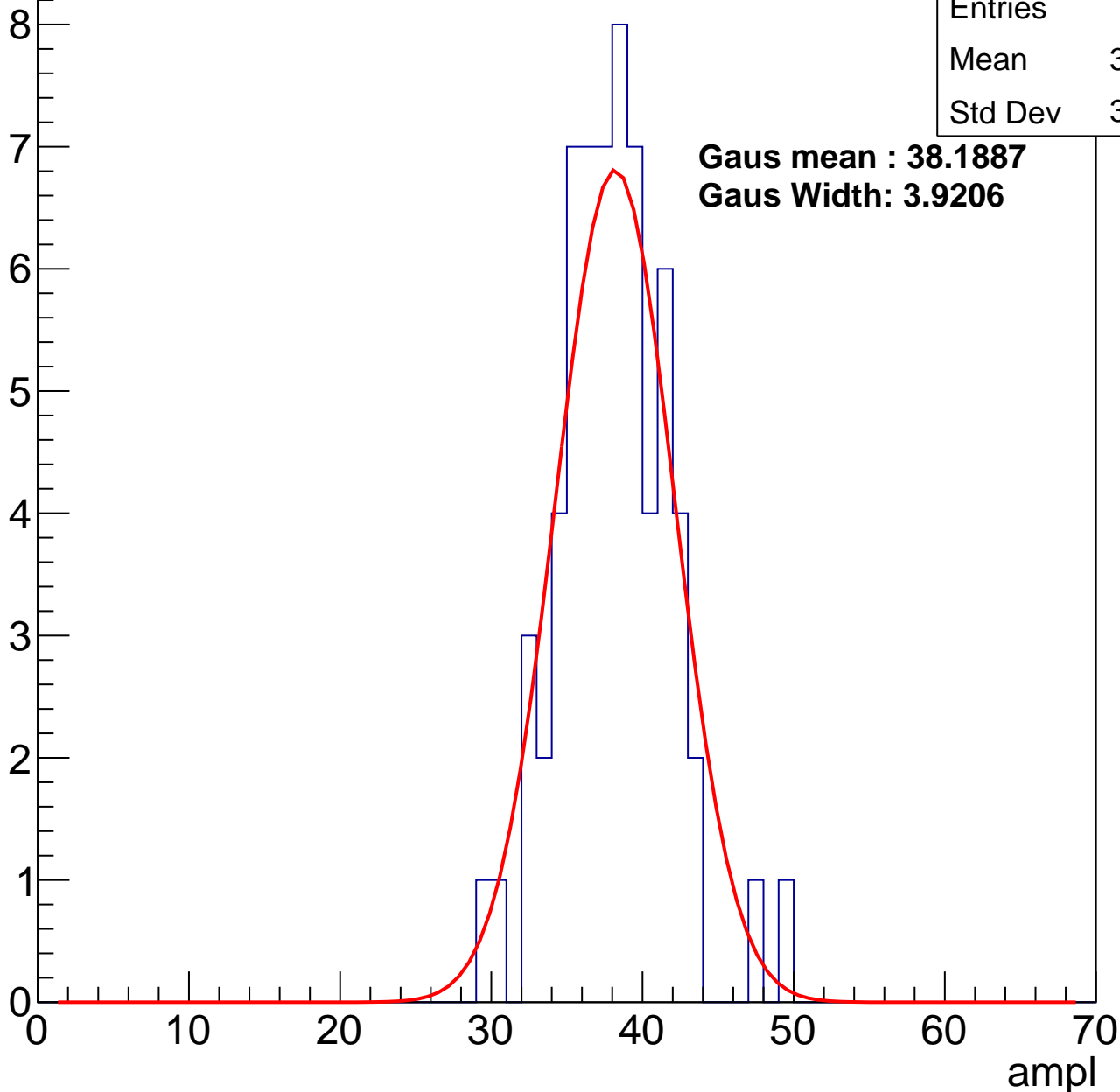
# B0L000S, U7-ch65, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	65
Mean	37.63
Std Dev	3.614

**Gaus mean : 38.1887**  
**Gaus Width: 3.9206**



# B0L000S, U7-ch65, adc2

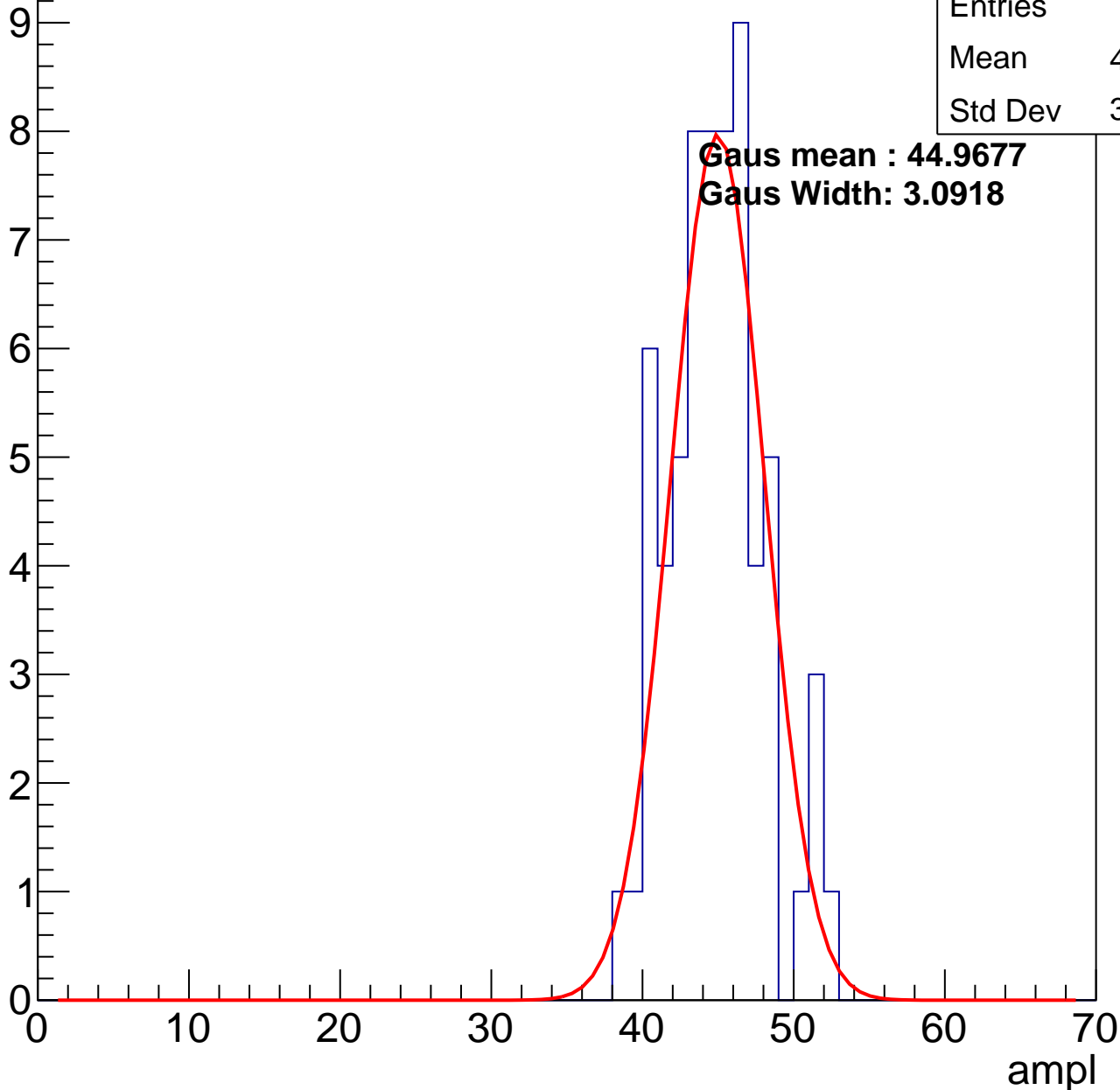
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	64
Mean	44.44
Std Dev	3.102

**Gaus mean : 44.9677**

**Gaus Width: 3.0918**

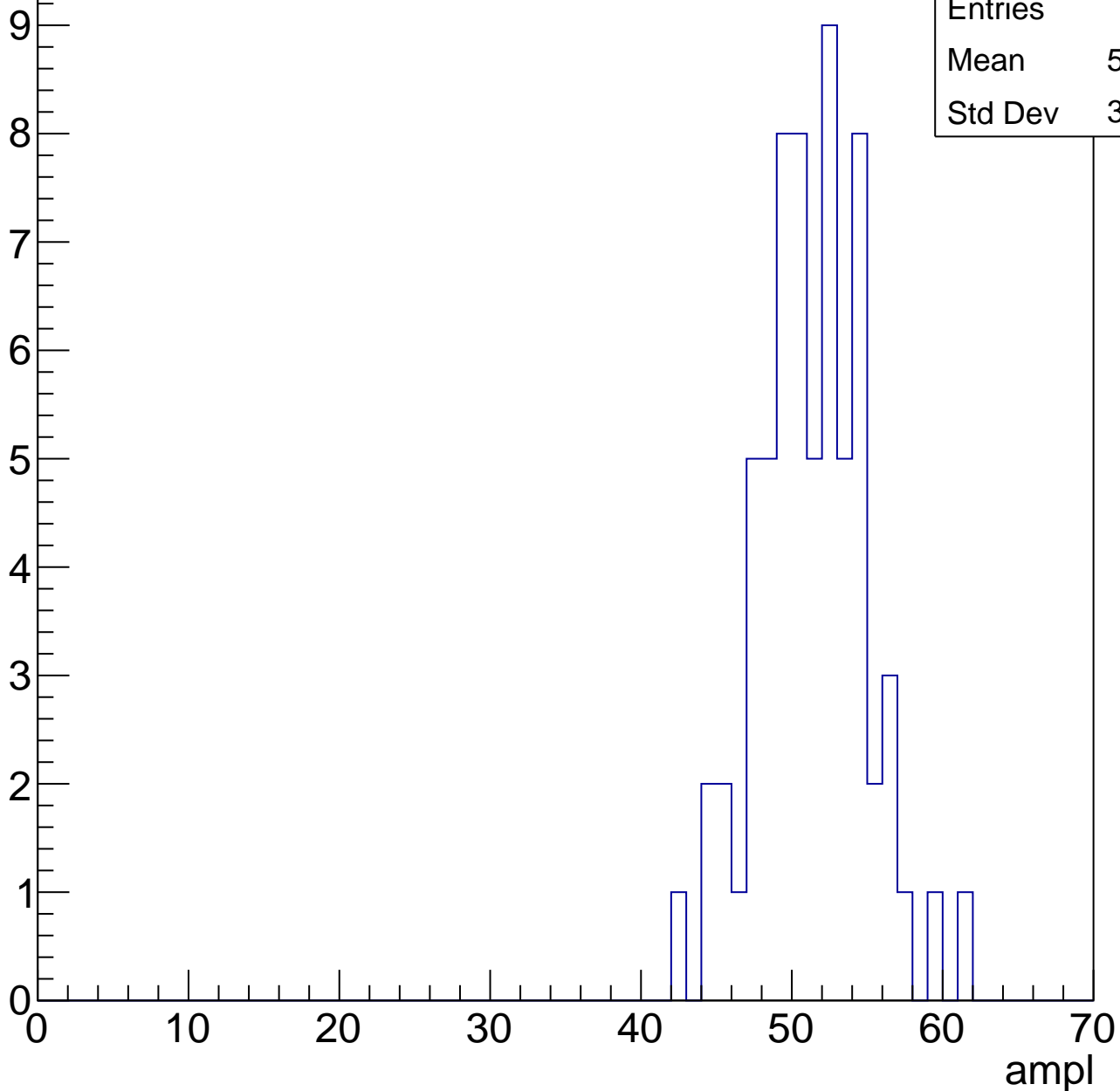


# B0L000S, U7-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	67
Mean	50.87
Std Dev	3.557

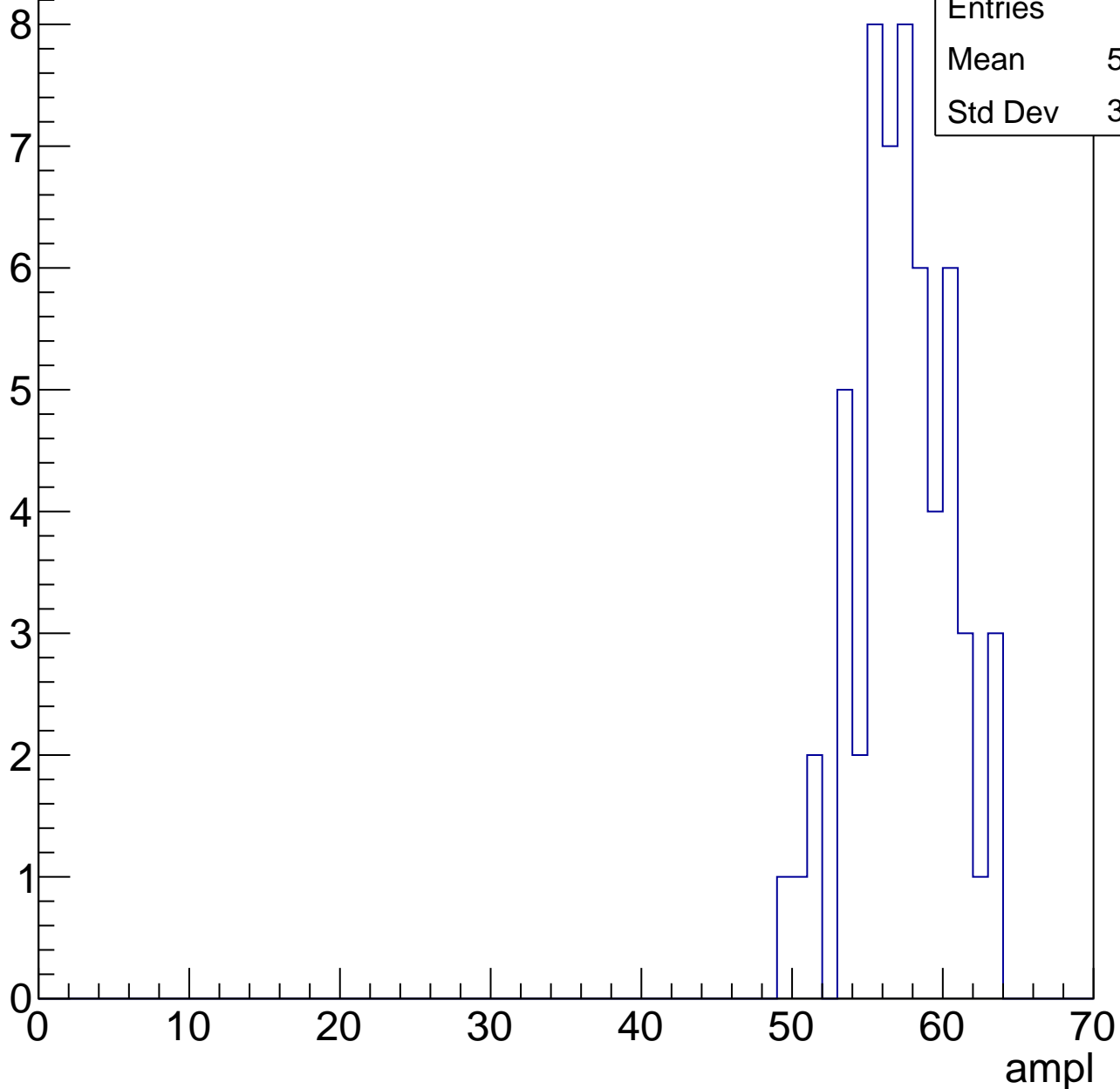


# B0L000S, U7-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	57
Mean	56.84
Std Dev	3.183

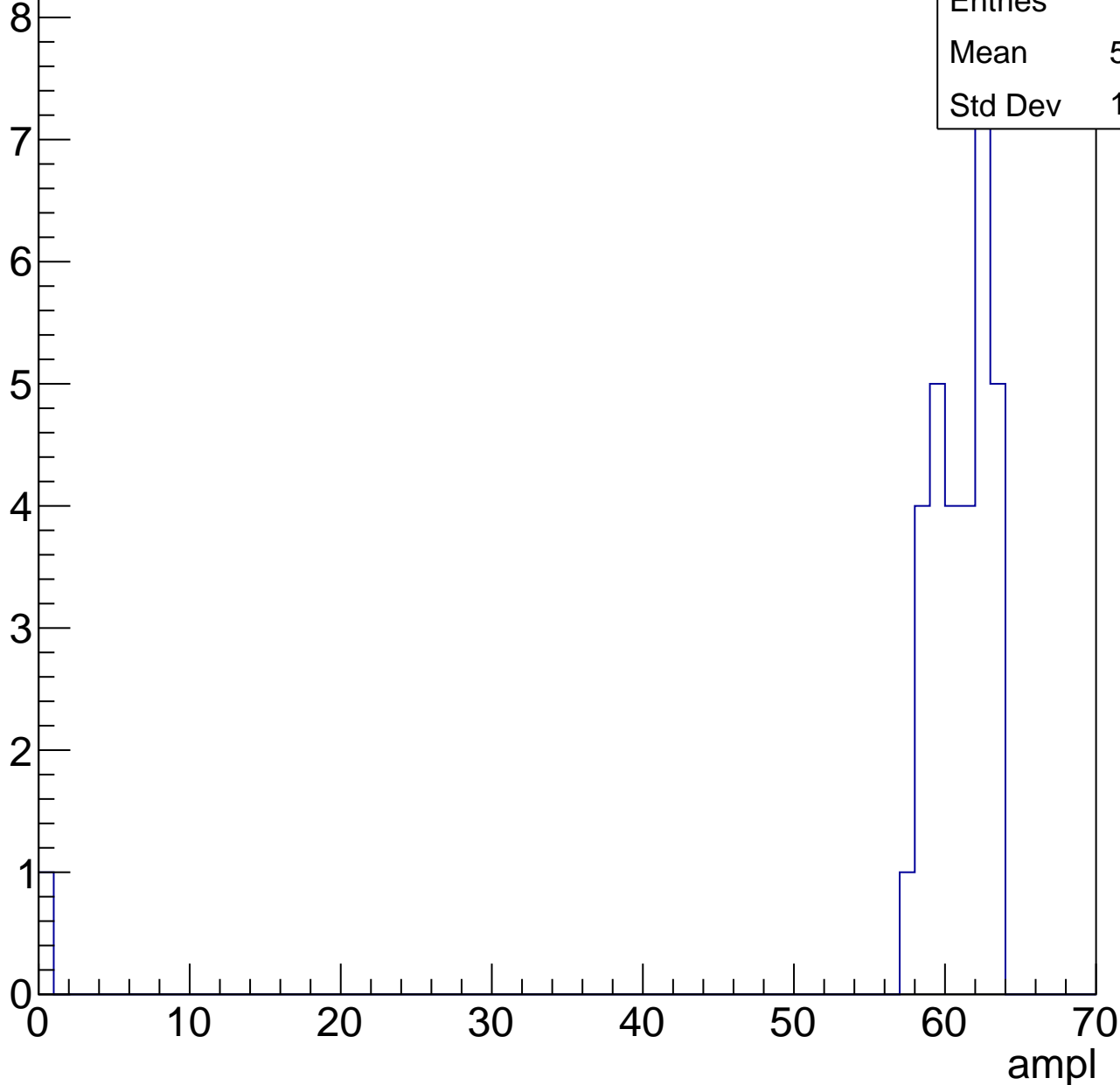


# B0L000S, U7-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

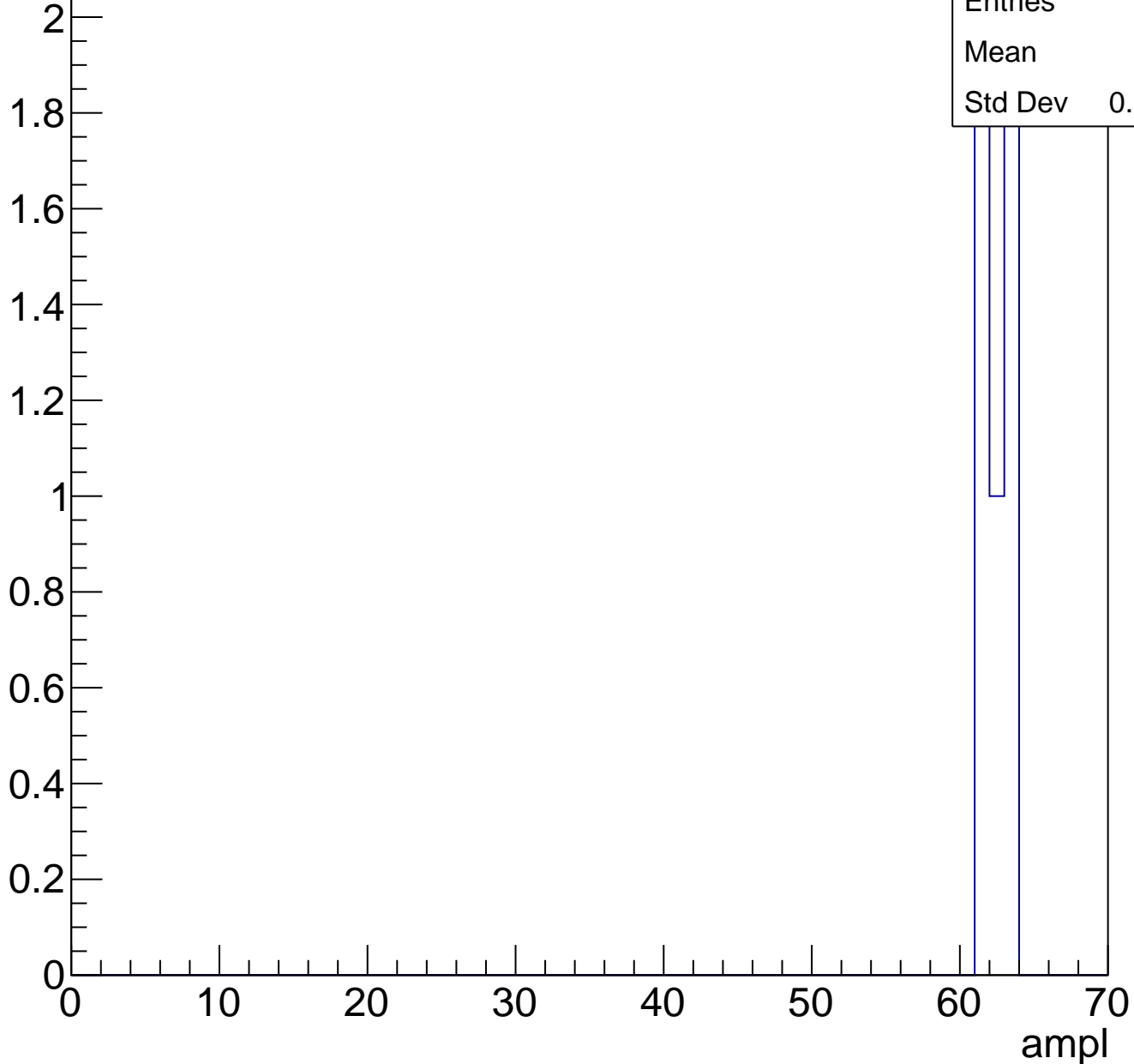
Entries	32
Mean	58.72
Std Dev	10.69



# B0L000S, U7-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	2
Mean	11
Std Dev	11

# B0L000S, U7-ch66, adc0

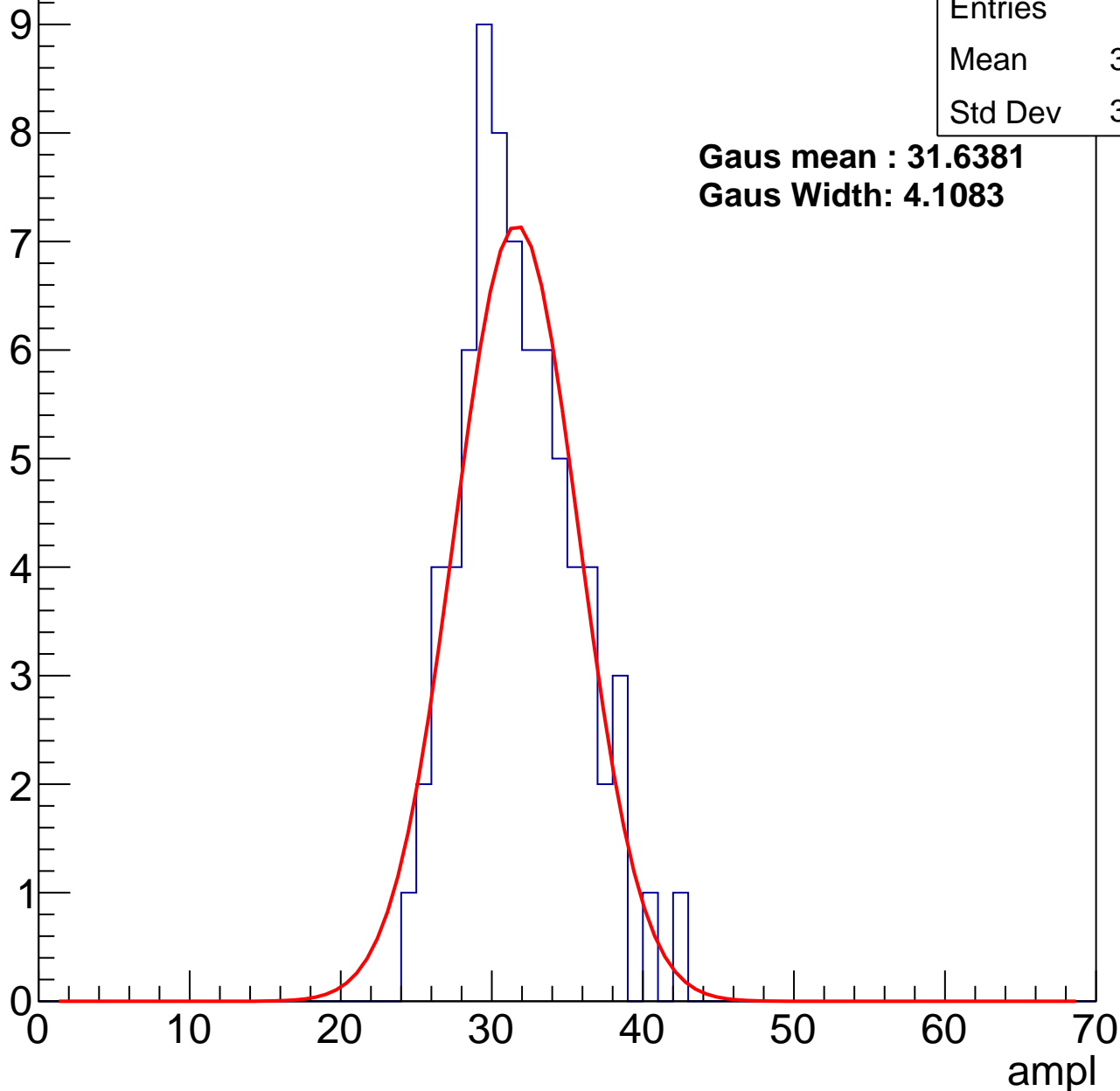
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	73
Mean	31.32
Std Dev	3.767

**Gaus mean : 31.6381**

**Gaus Width: 4.1083**



# B0L000S, U7-ch66, adc1

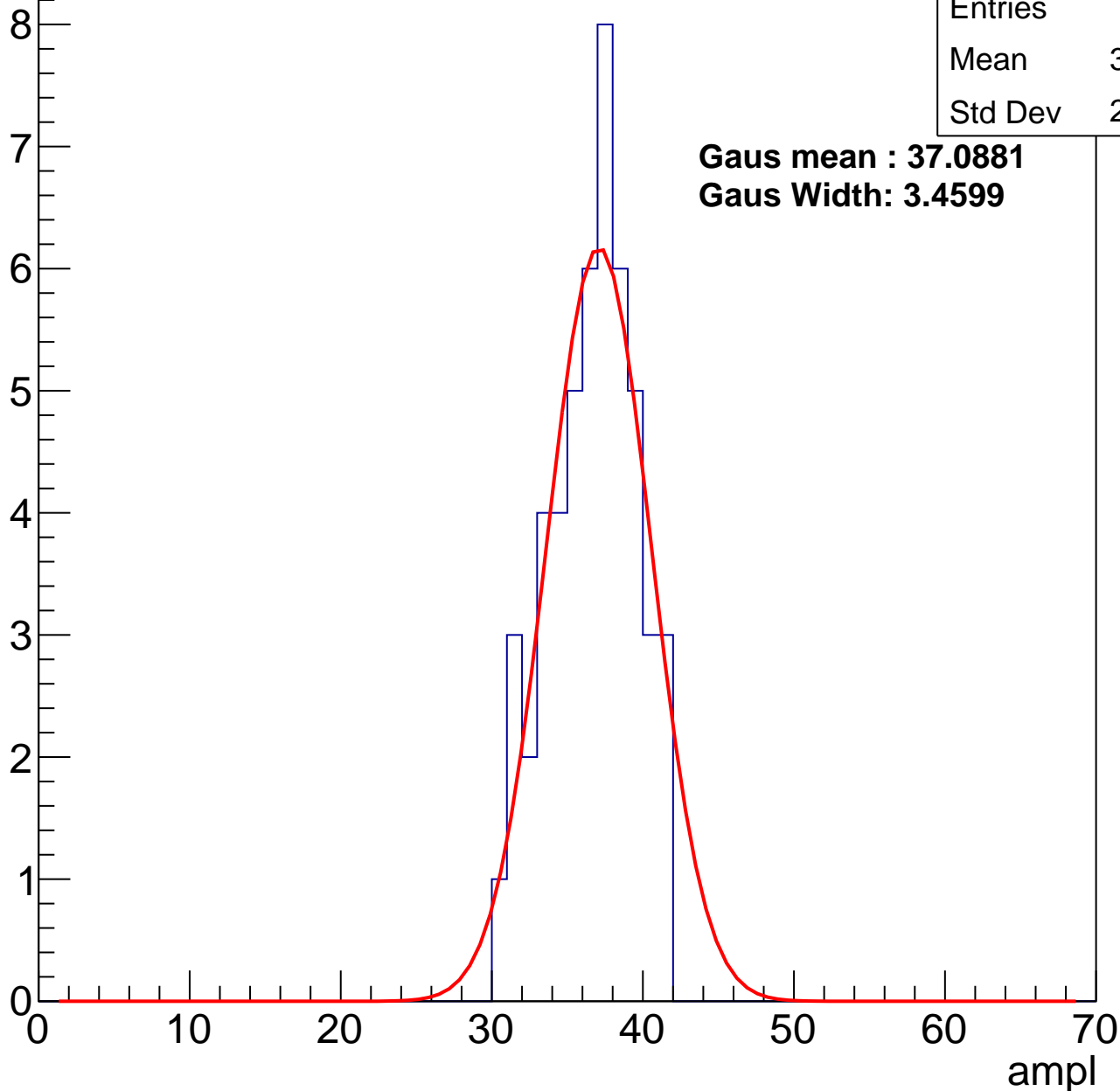
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	50
Mean	36.16
Std Dev	2.824

**Gaus mean : 37.0881**

**Gaus Width: 3.4599**



# B0L000S, U7-ch66, adc2

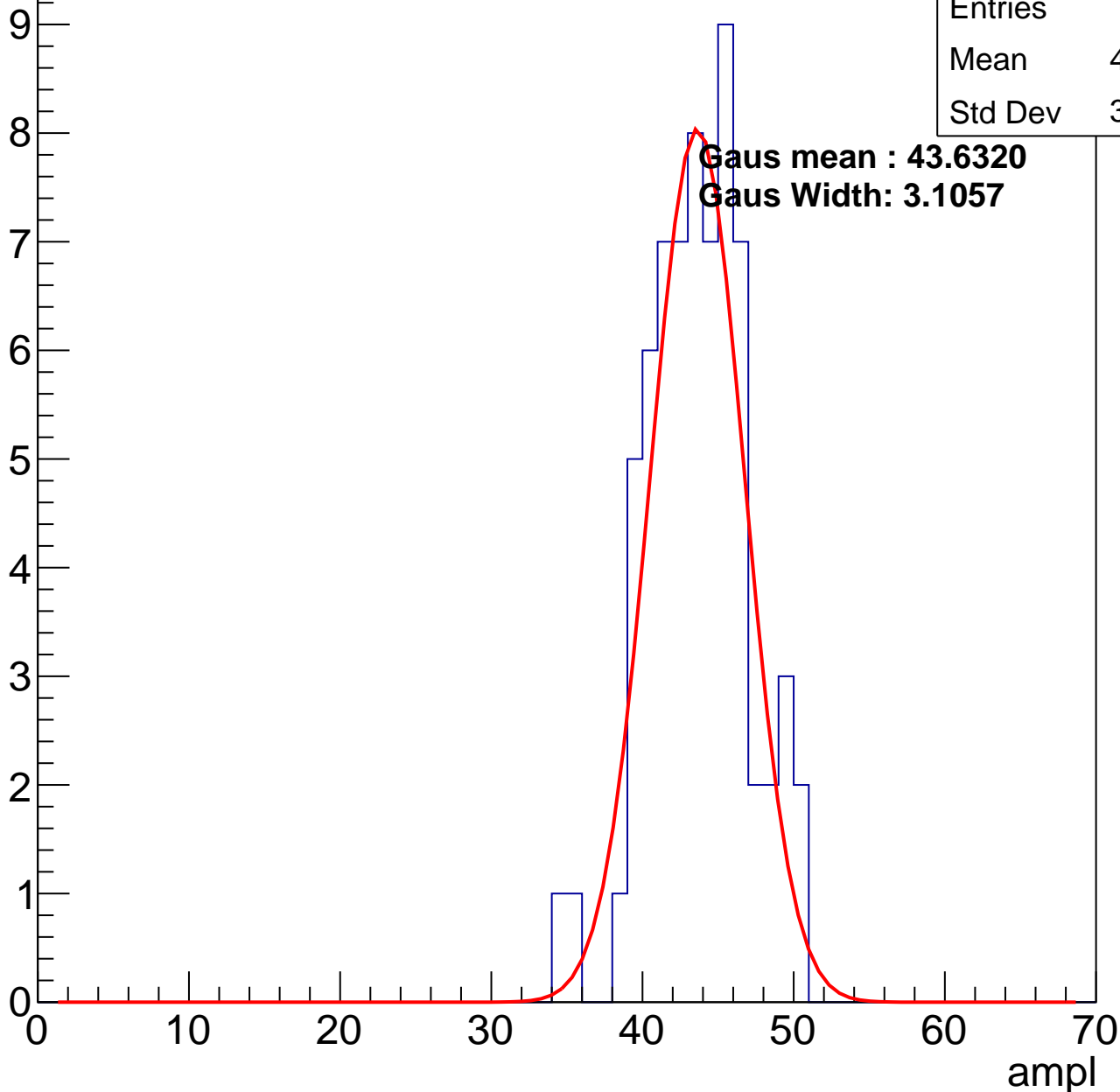
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	68
Mean	43.22
Std Dev	3.276

**Gaus mean : 43.6320**

**Gaus Width: 3.1057**



# B0L000S, U7-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

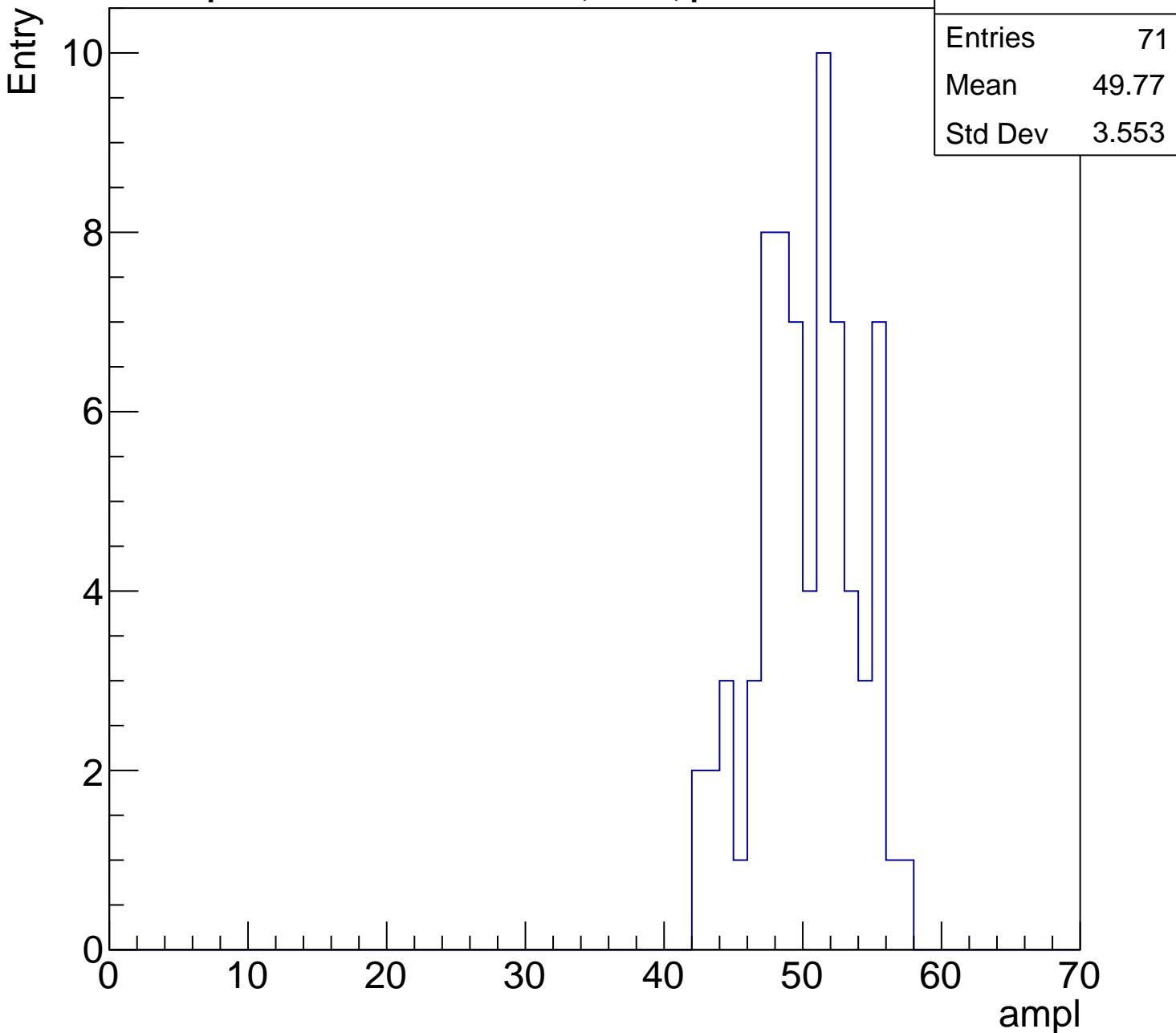
Entries	71
Mean	49.77
Std Dev	3.553

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

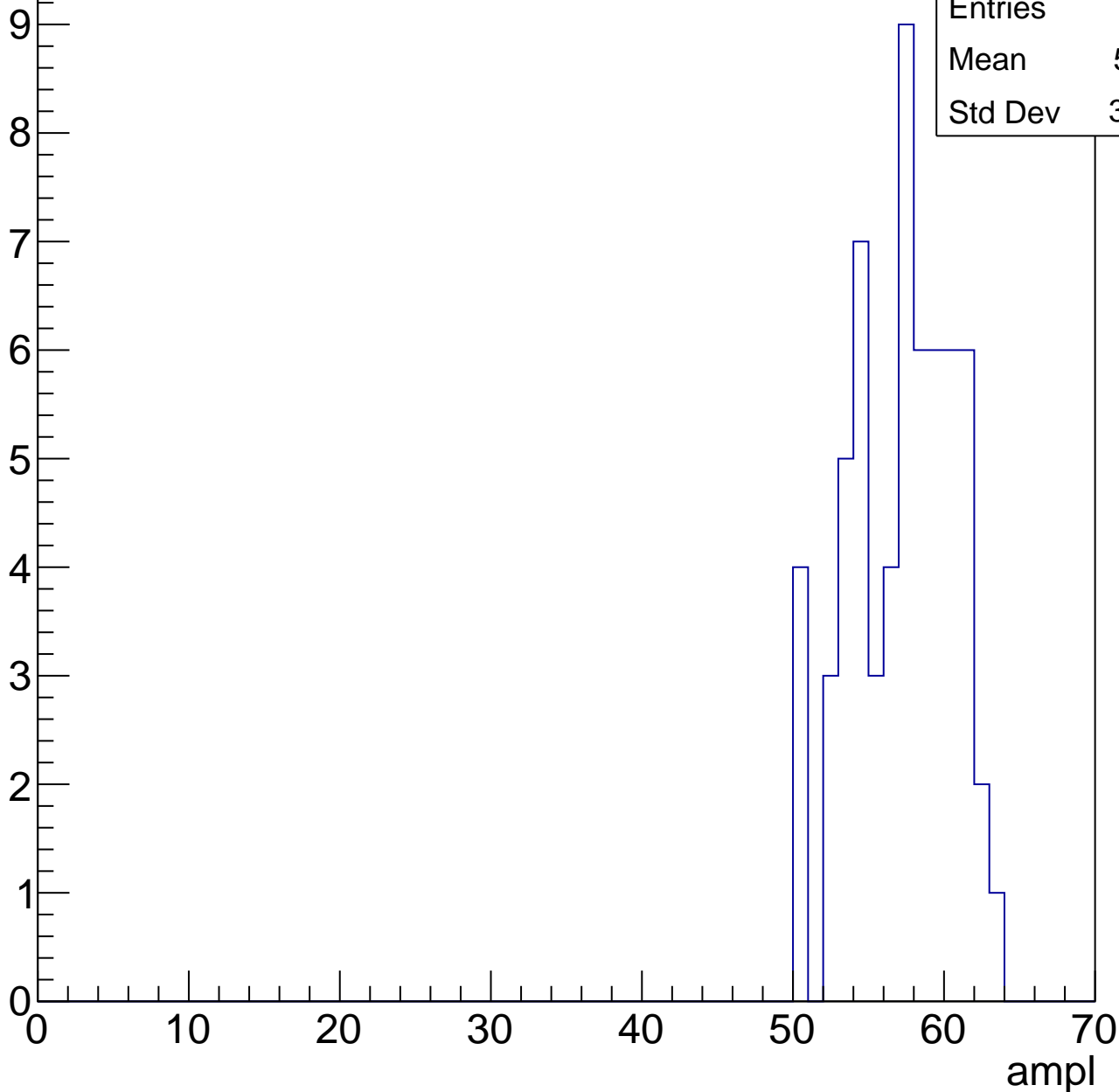


# B0L000S, U7-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	62
Mean	56.71
Std Dev	3.338

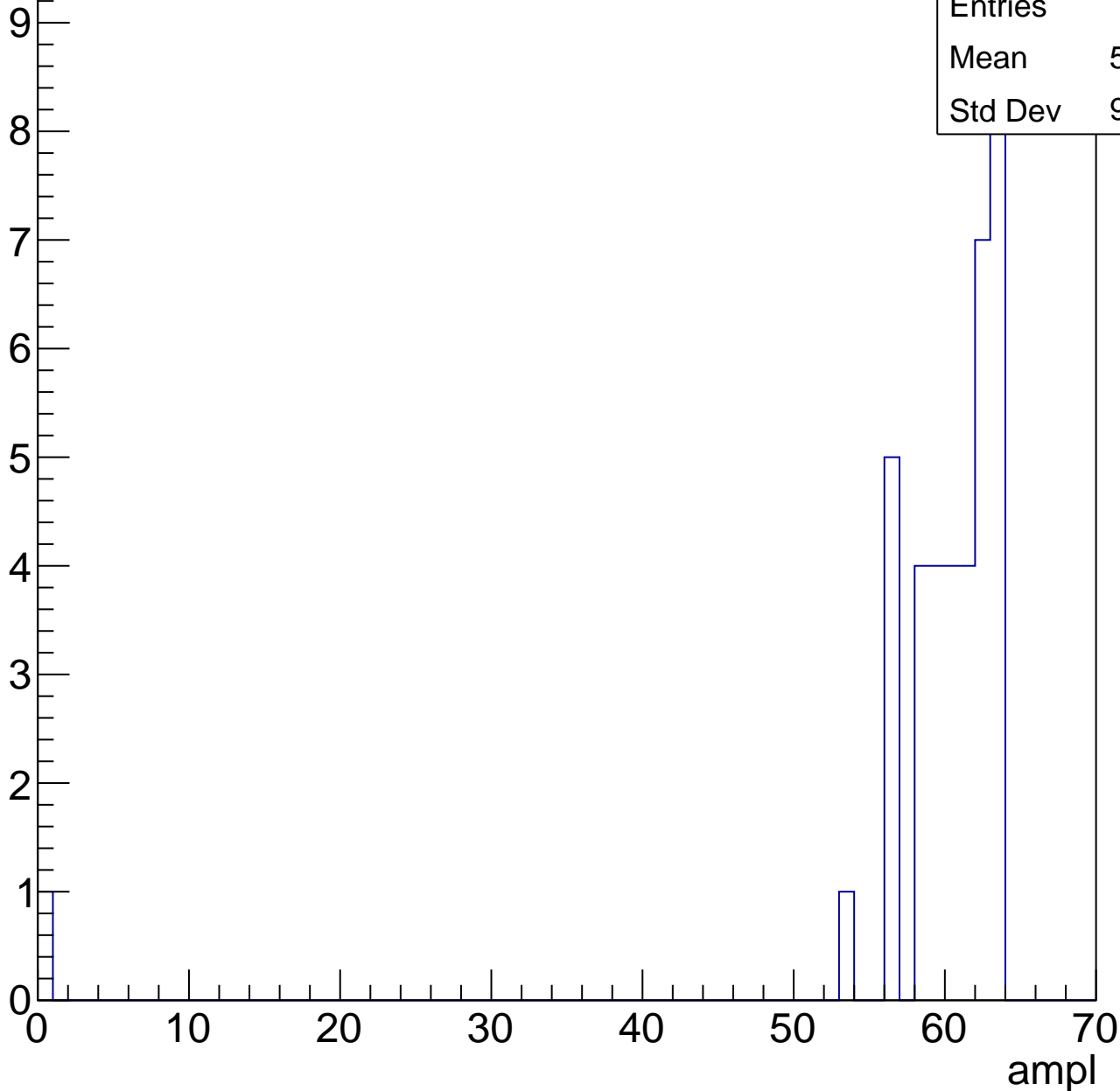


# B0L000S, U7-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	39
Mean	58.62
Std Dev	9.854



# B0L000S, U7-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	62
Std Dev	0

ampl



# B0L000S, U7-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	1
Mean	23
Std Dev	0

# B0L000S, U7-ch67, adc0

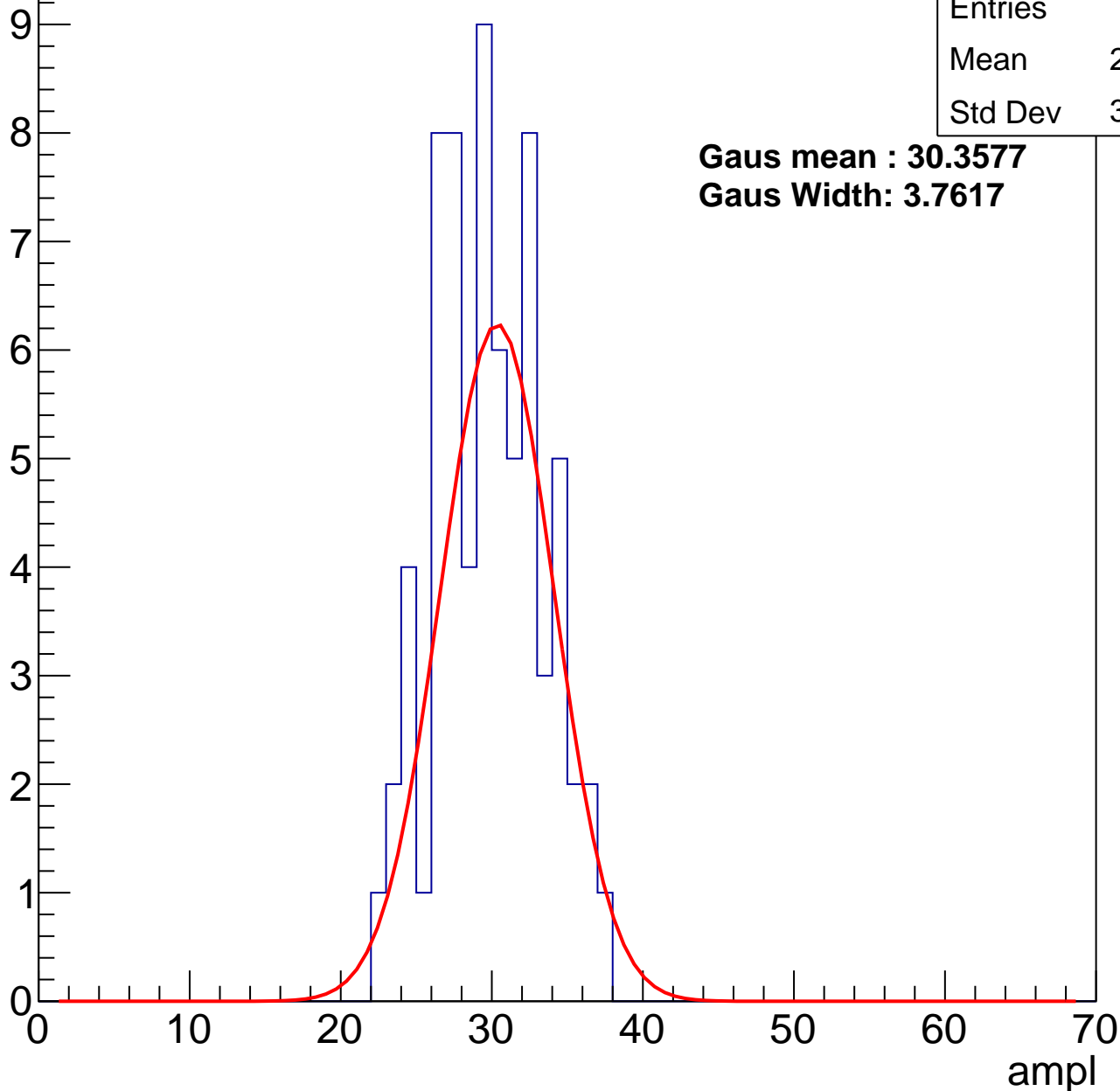
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	69
Mean	29.35
Std Dev	3.493

**Gaus mean : 30.3577**

**Gaus Width: 3.7617**



# B0L000S, U7-ch67, adc1

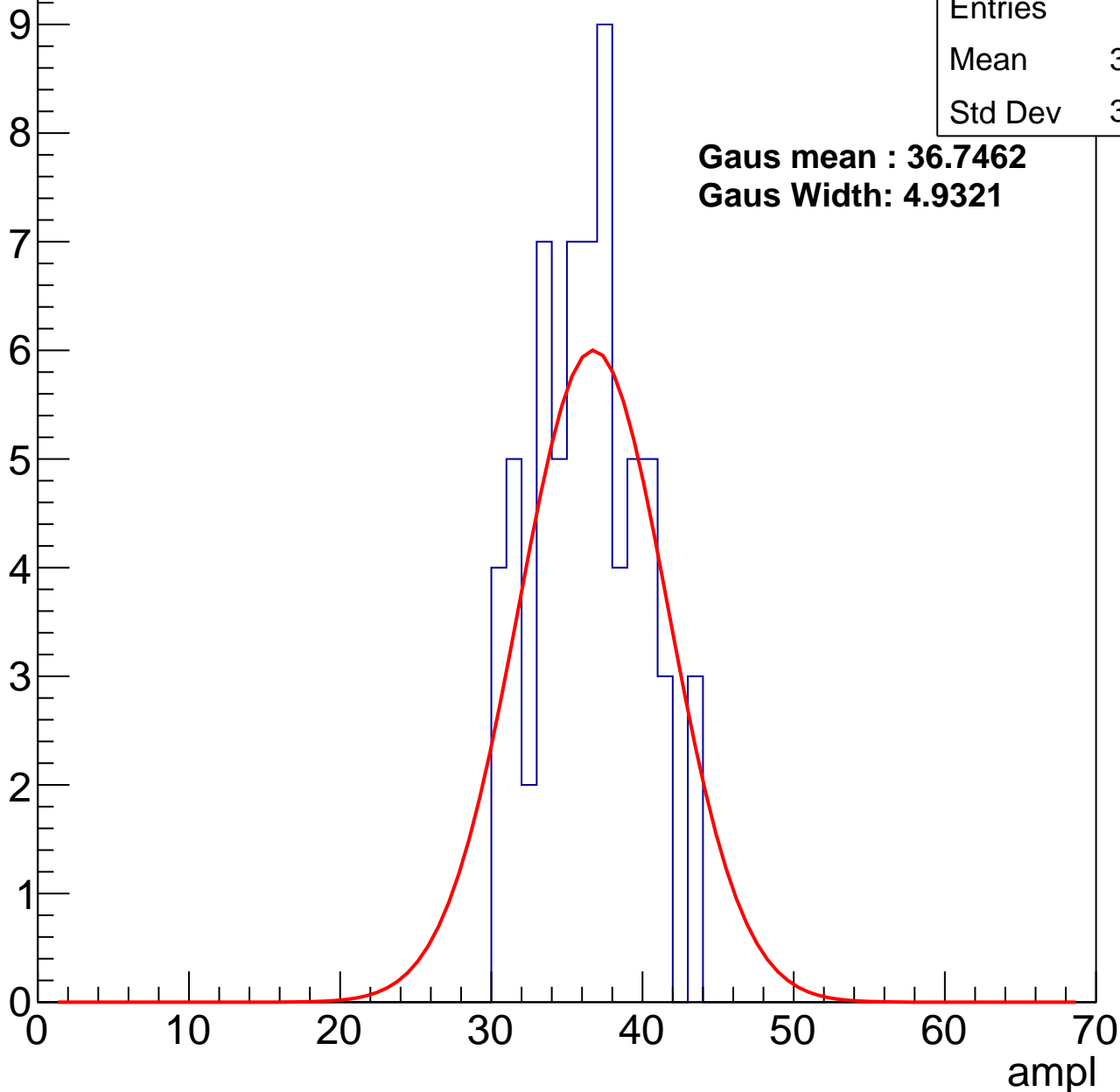
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	66
Mean	35.89
Std Dev	3.398

**Gaus mean : 36.7462**

**Gaus Width: 4.9321**



# B0L000S, U7-ch67, adc2

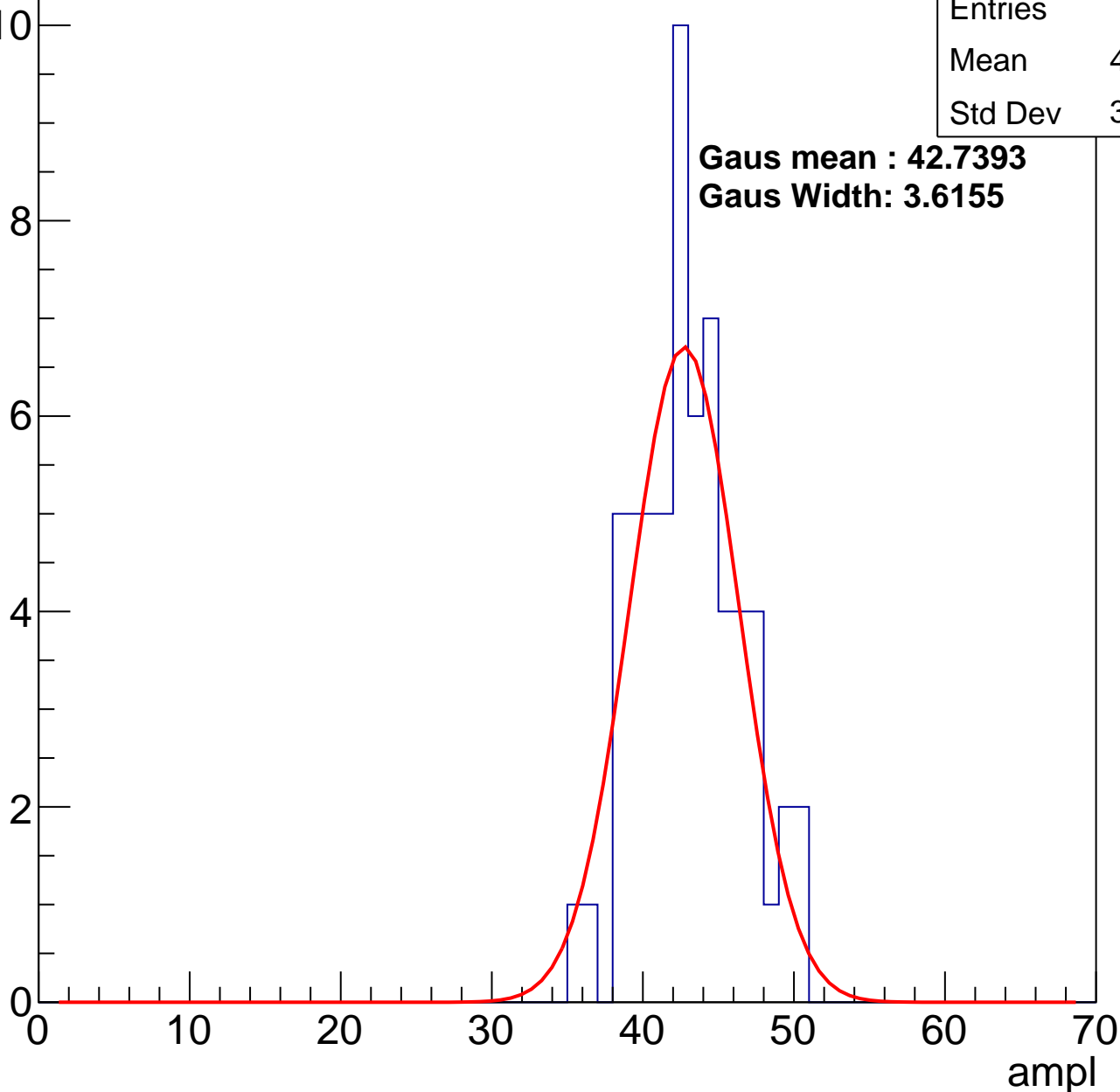
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	62
Mean	42.66
Std Dev	3.369

**Gaus mean : 42.7393**

**Gaus Width: 3.6155**

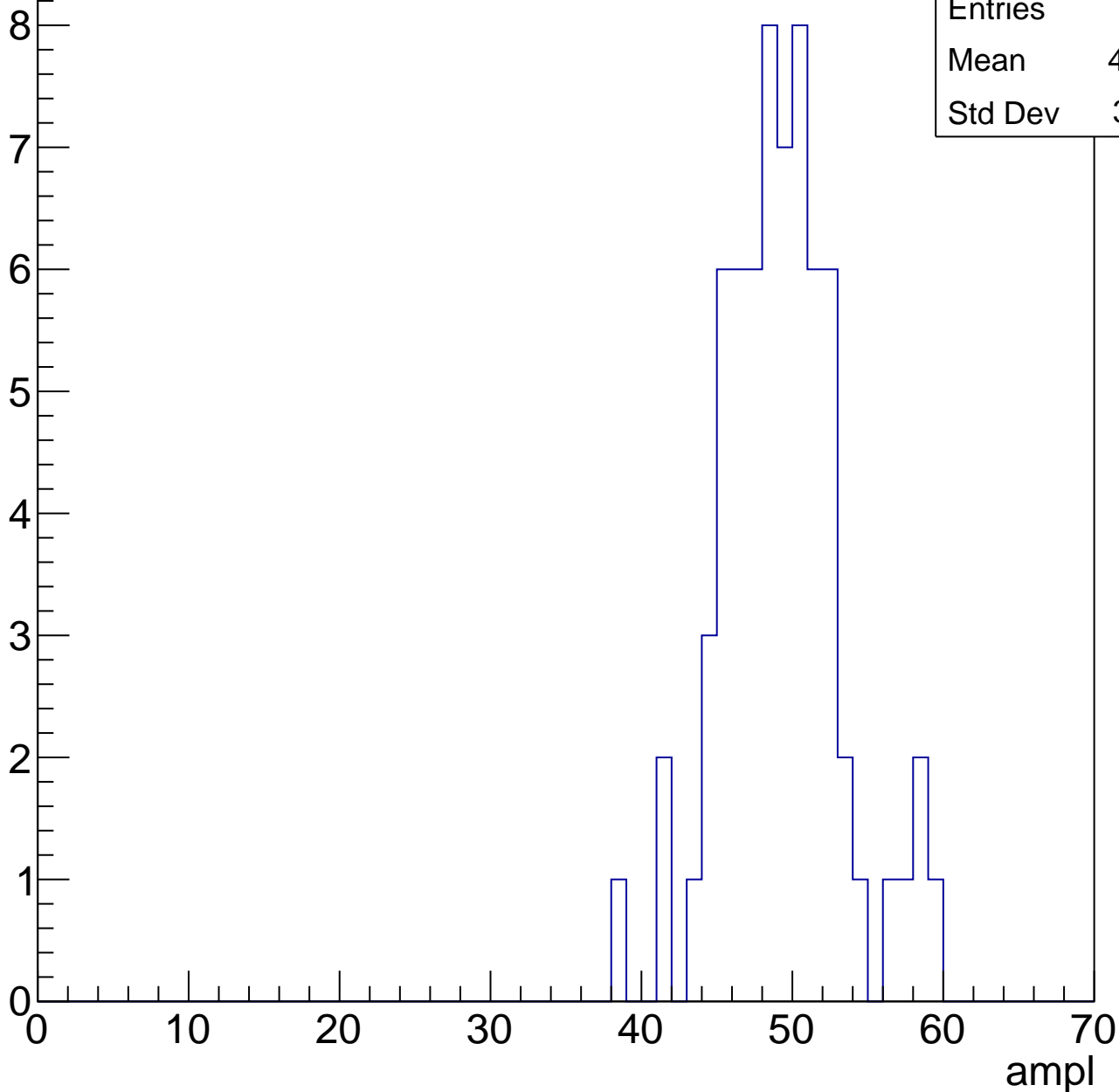


# B0L000S, U7-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

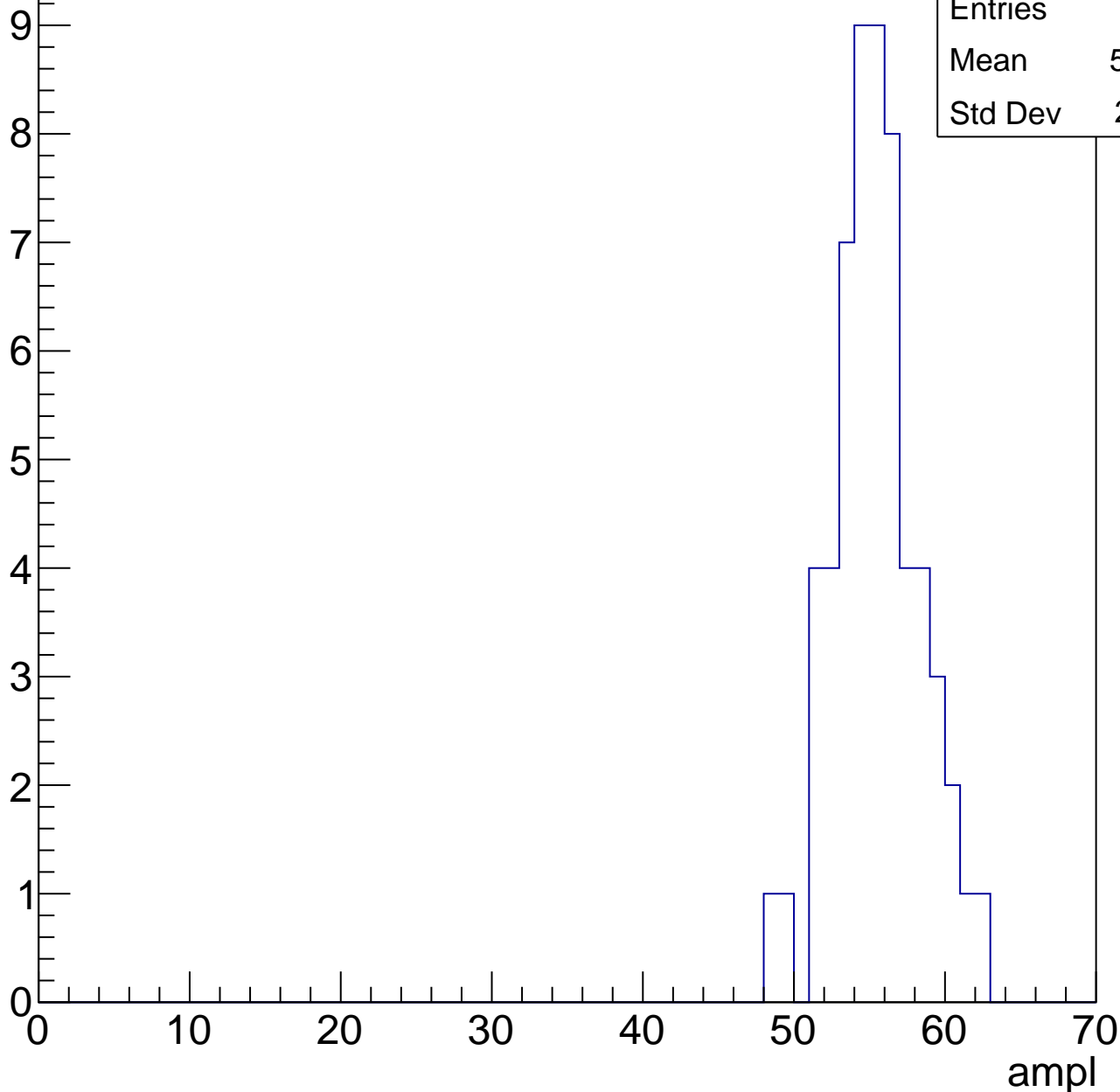
Entries	68
Mean	48.76
Std Dev	3.941



# B0L000S, U7-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



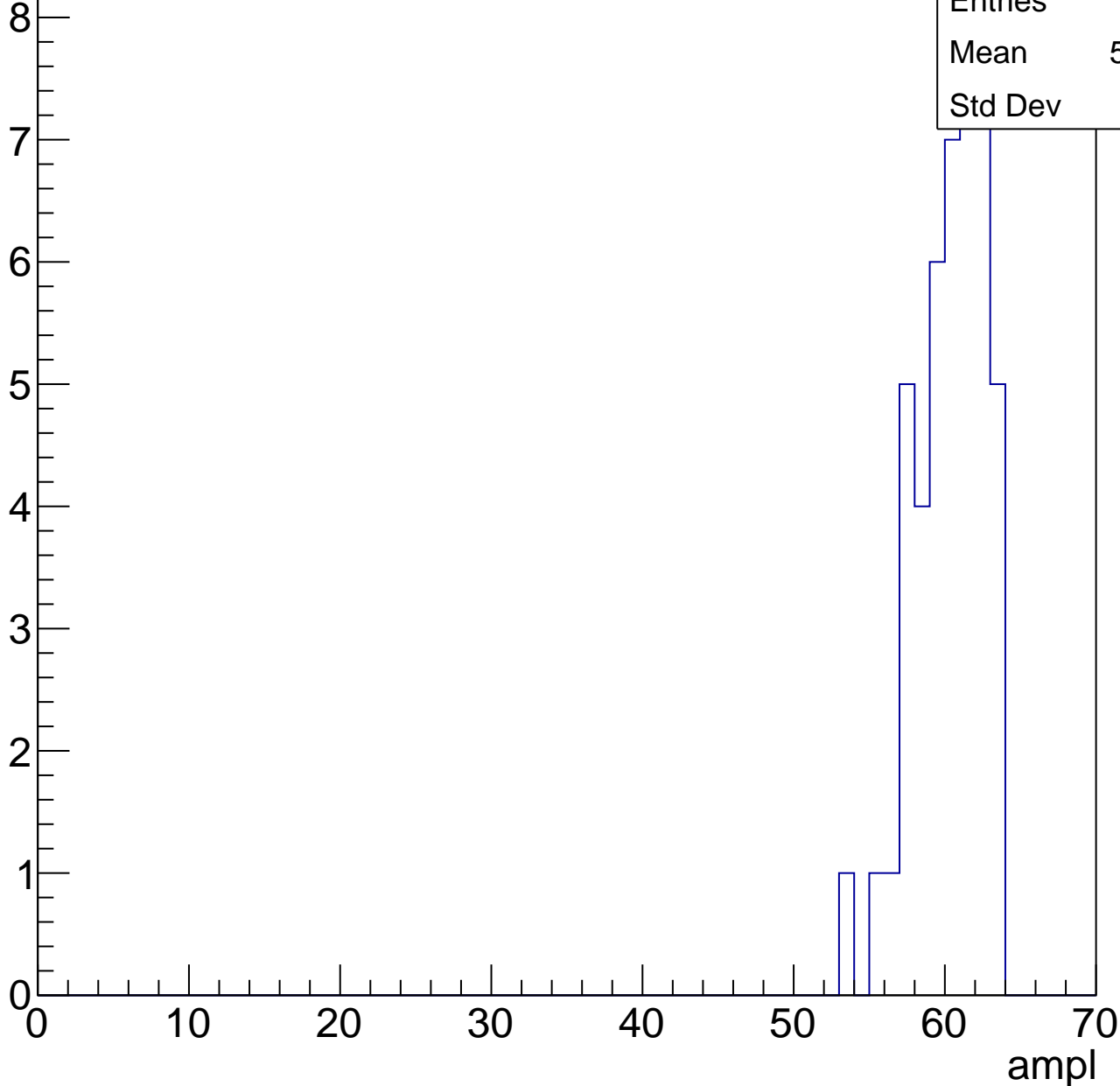
Entries	58
Mean	54.98
Std Dev	2.831

# B0L000S, U7-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	46
Mean	59.87
Std Dev	2.29

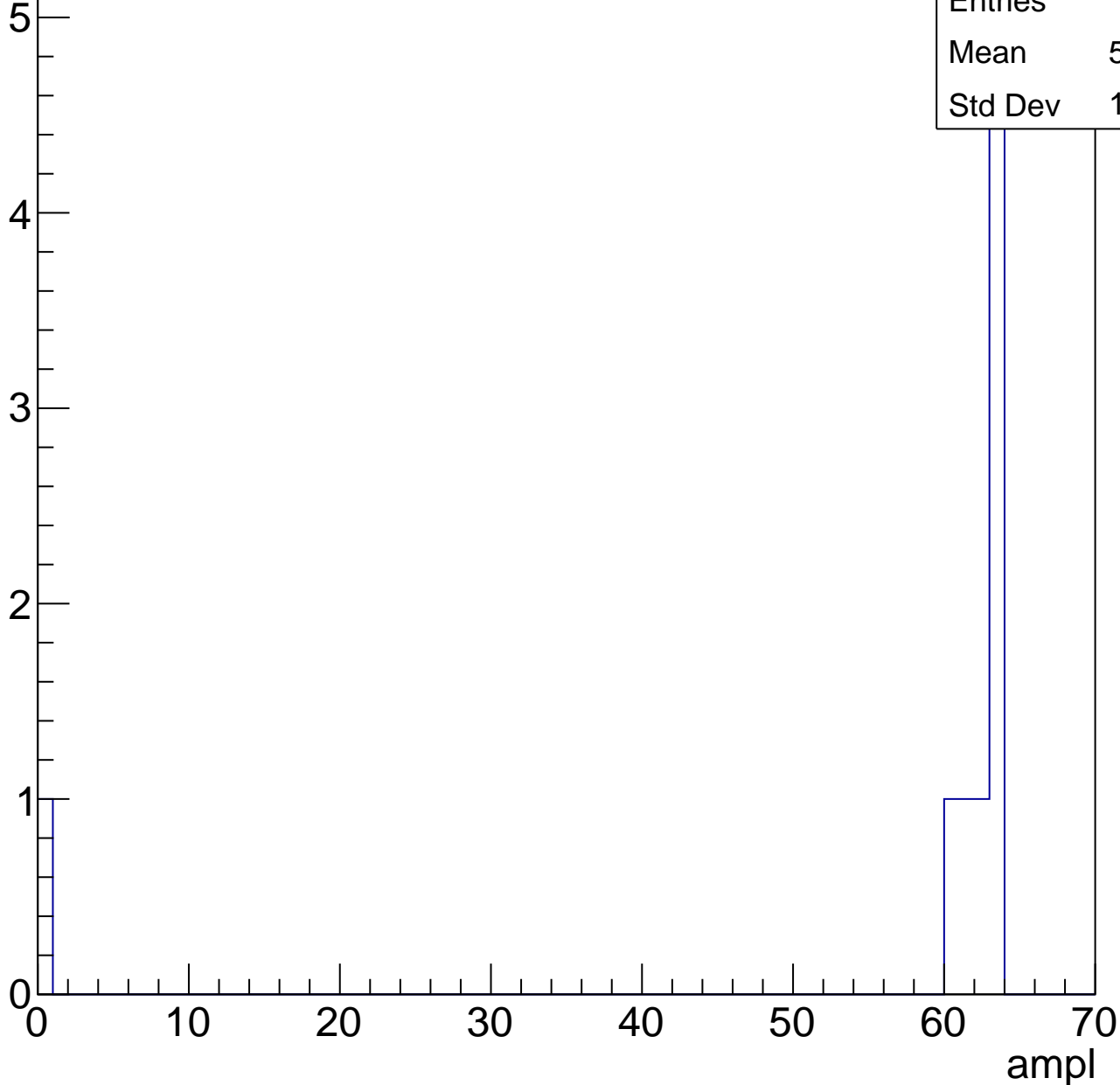


# B0L000S, U7-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	9
Mean	55.33
Std Dev	19.59





# B0L000S, U7-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	3
Mean	6.667
Std Dev	9.428

# B0L000S, U7-ch68, adc0

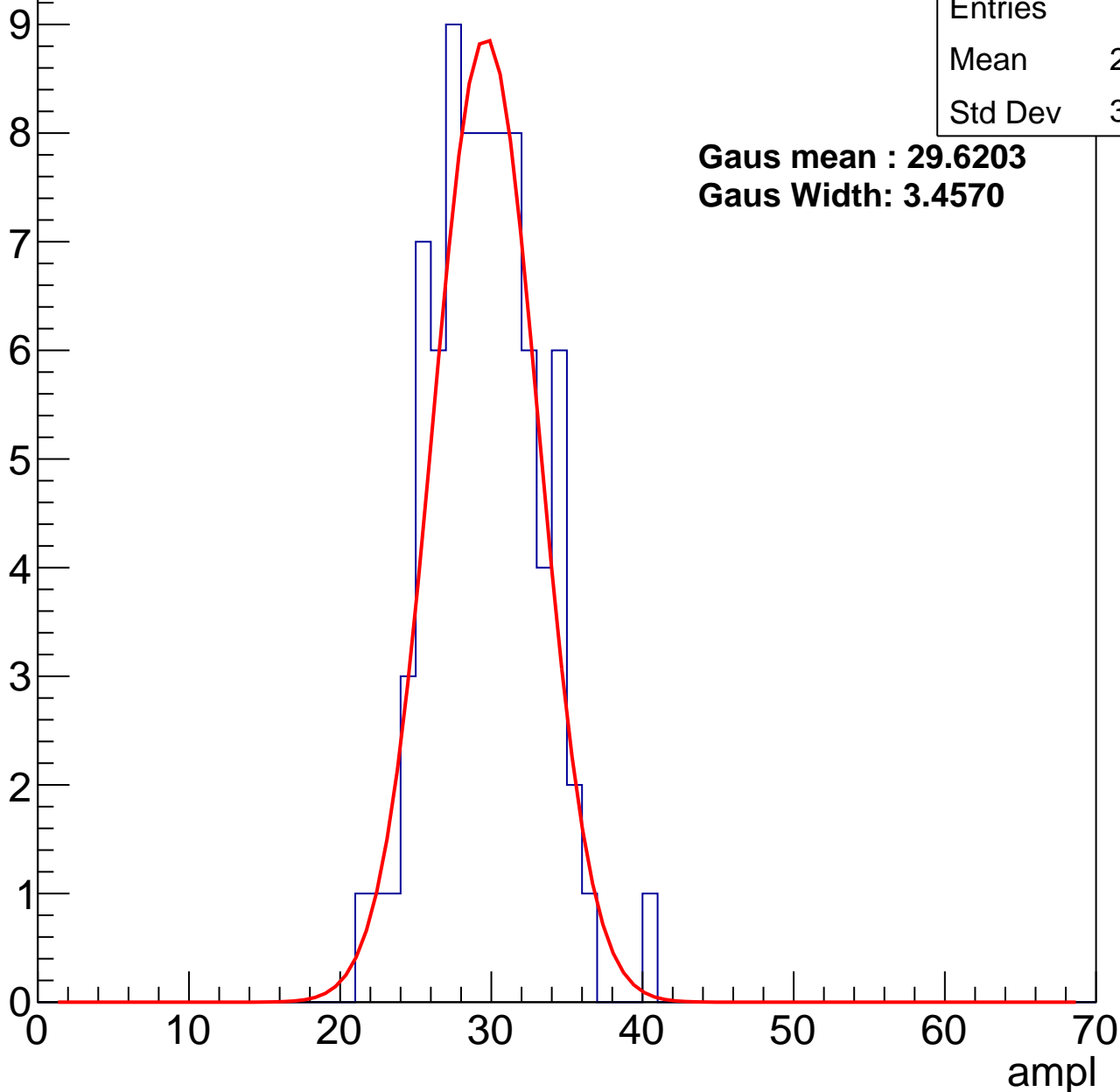
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	80
Mean	29.12
Std Dev	3.505

**Gaus mean : 29.6203**

**Gaus Width: 3.4570**



# B0L000S, U7-ch68, adc1

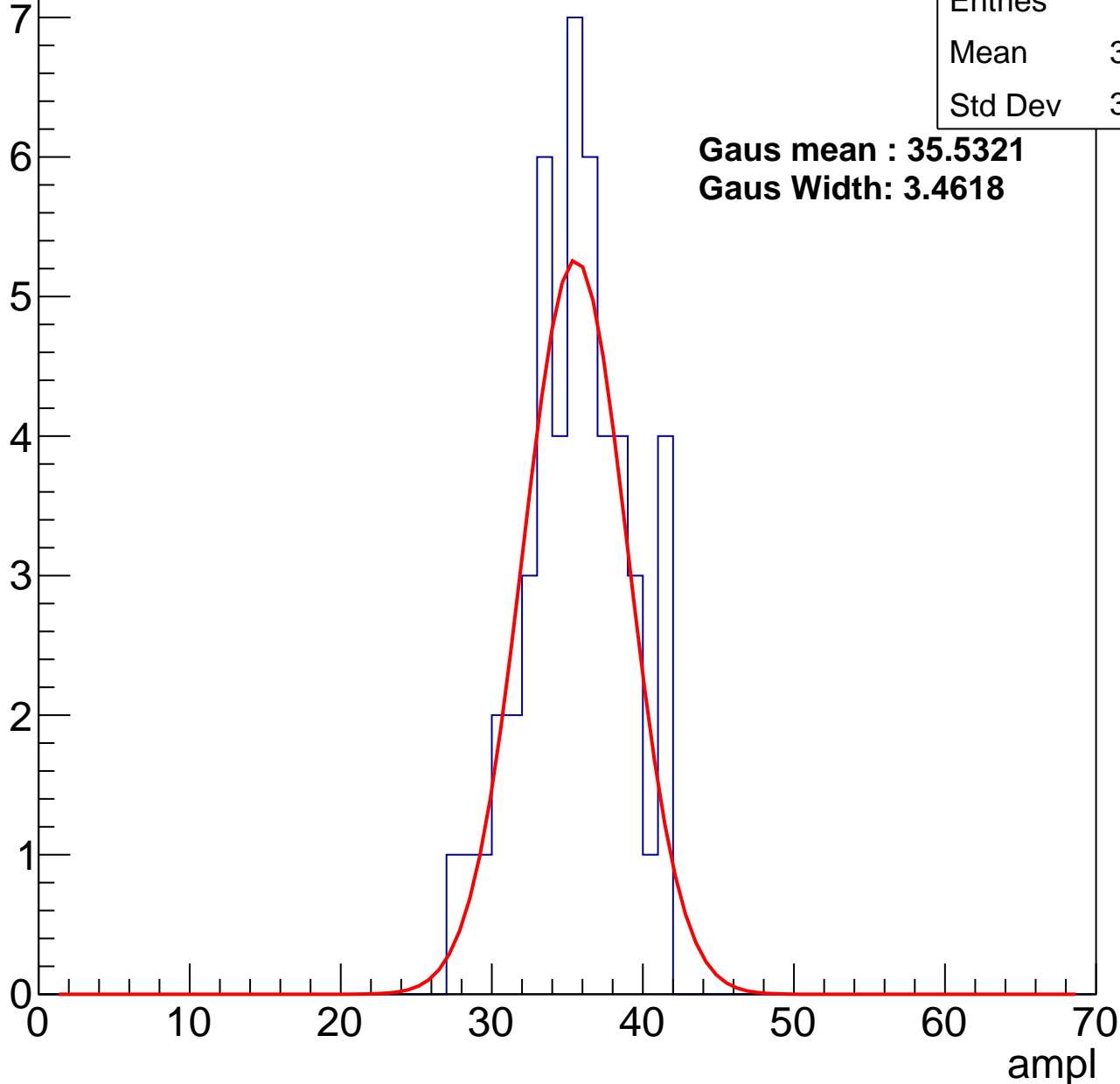
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	49
Mean	35.06
Std Dev	3.383

**Gaus mean : 35.5321**

**Gaus Width: 3.4618**



# B0L000S, U7-ch68, adc2

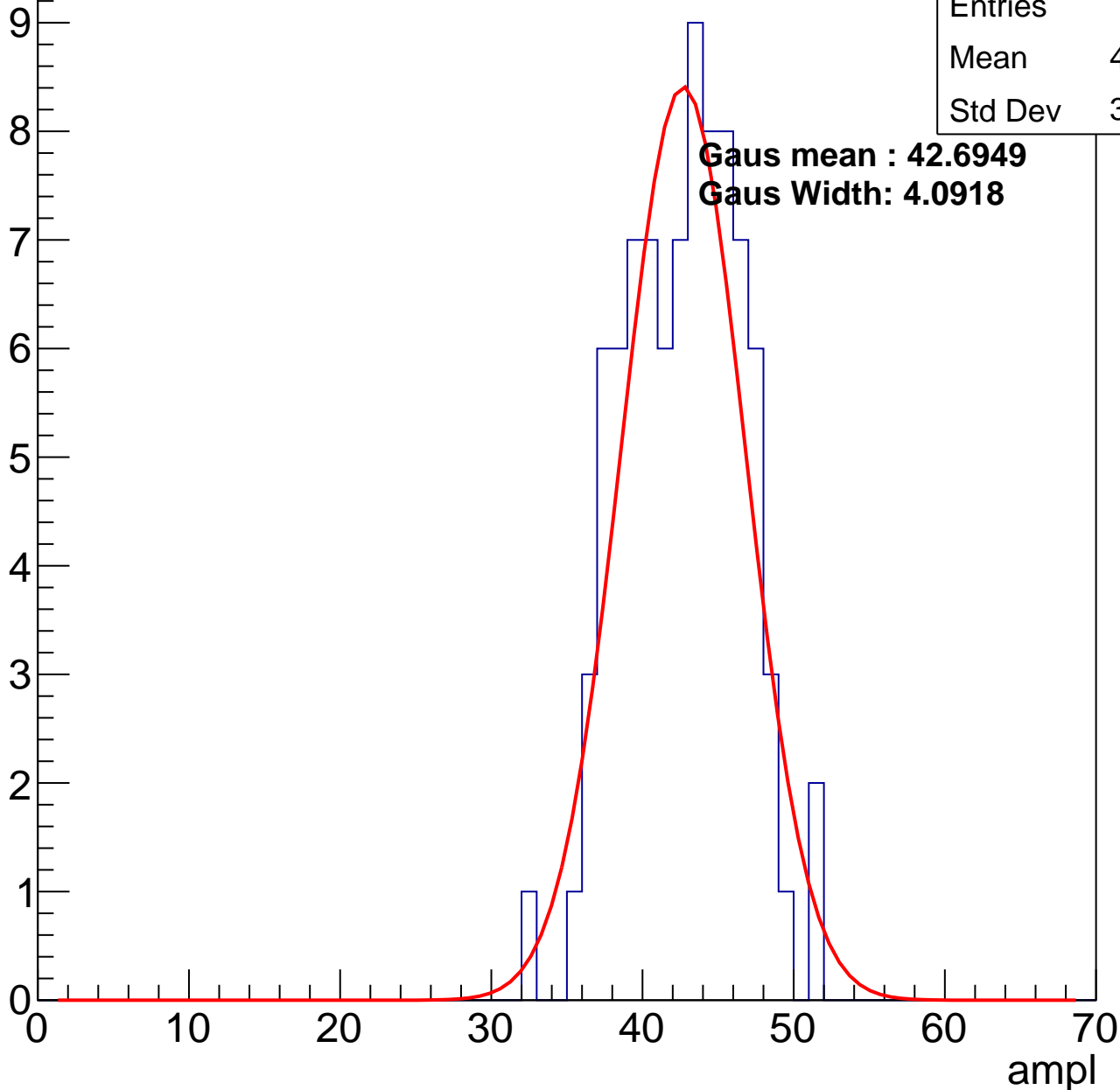
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	88
Mean	42.23
Std Dev	3.828

**Gaus mean : 42.6949**

**Gaus Width: 4.0918**

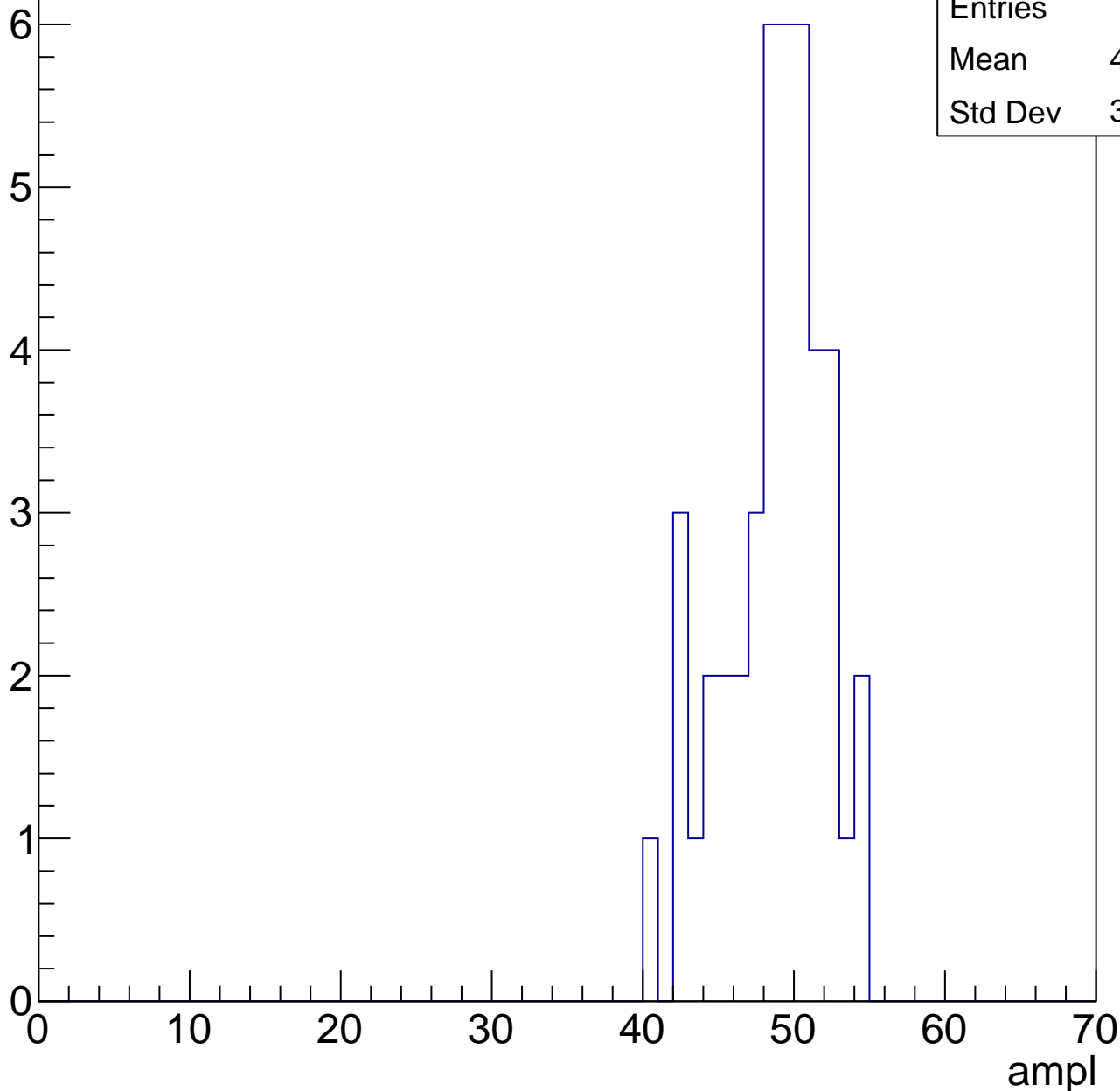


# B0L000S, U7-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	43
Mean	48.26
Std Dev	3.349

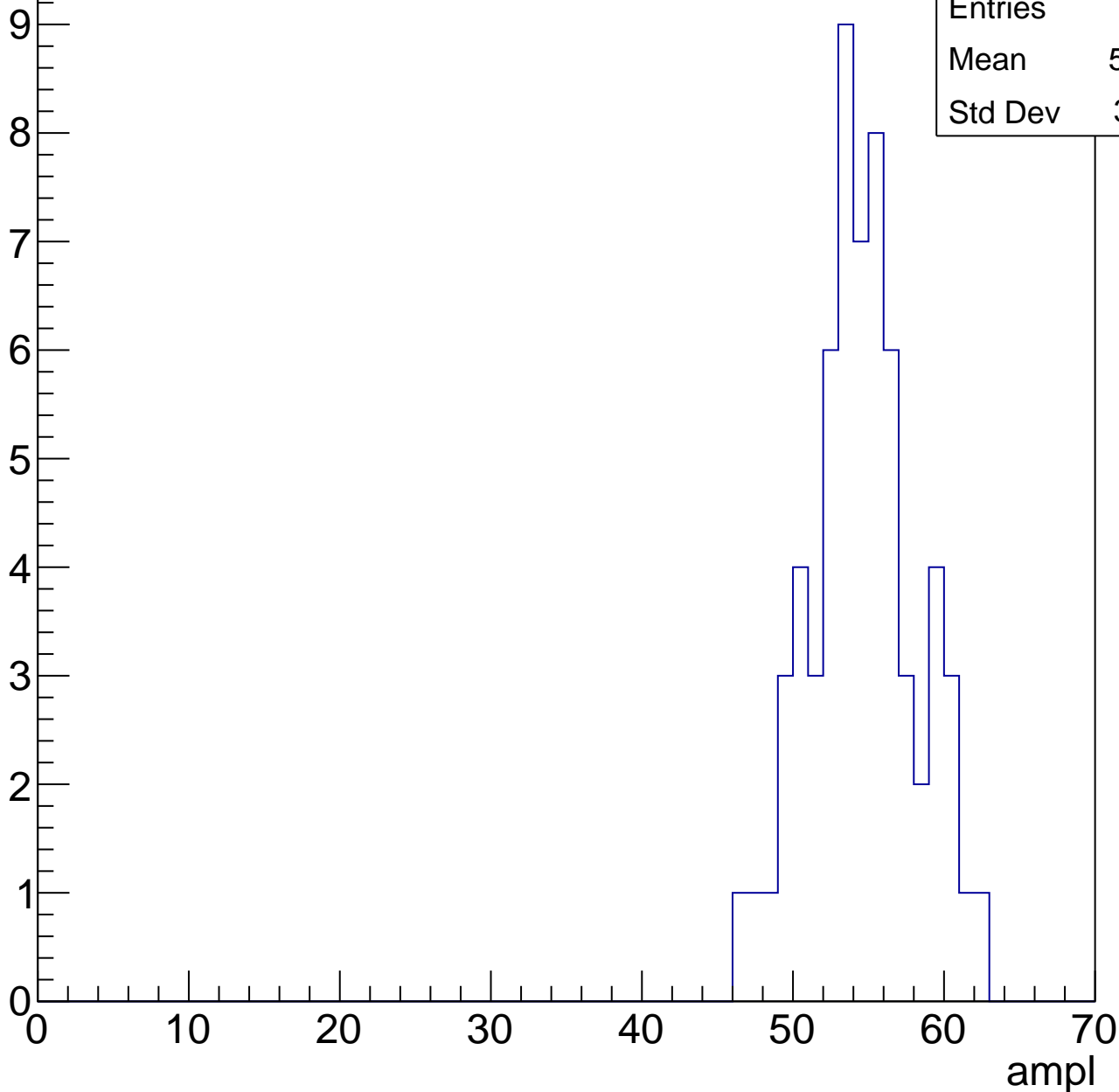


# B0L000S, U7-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

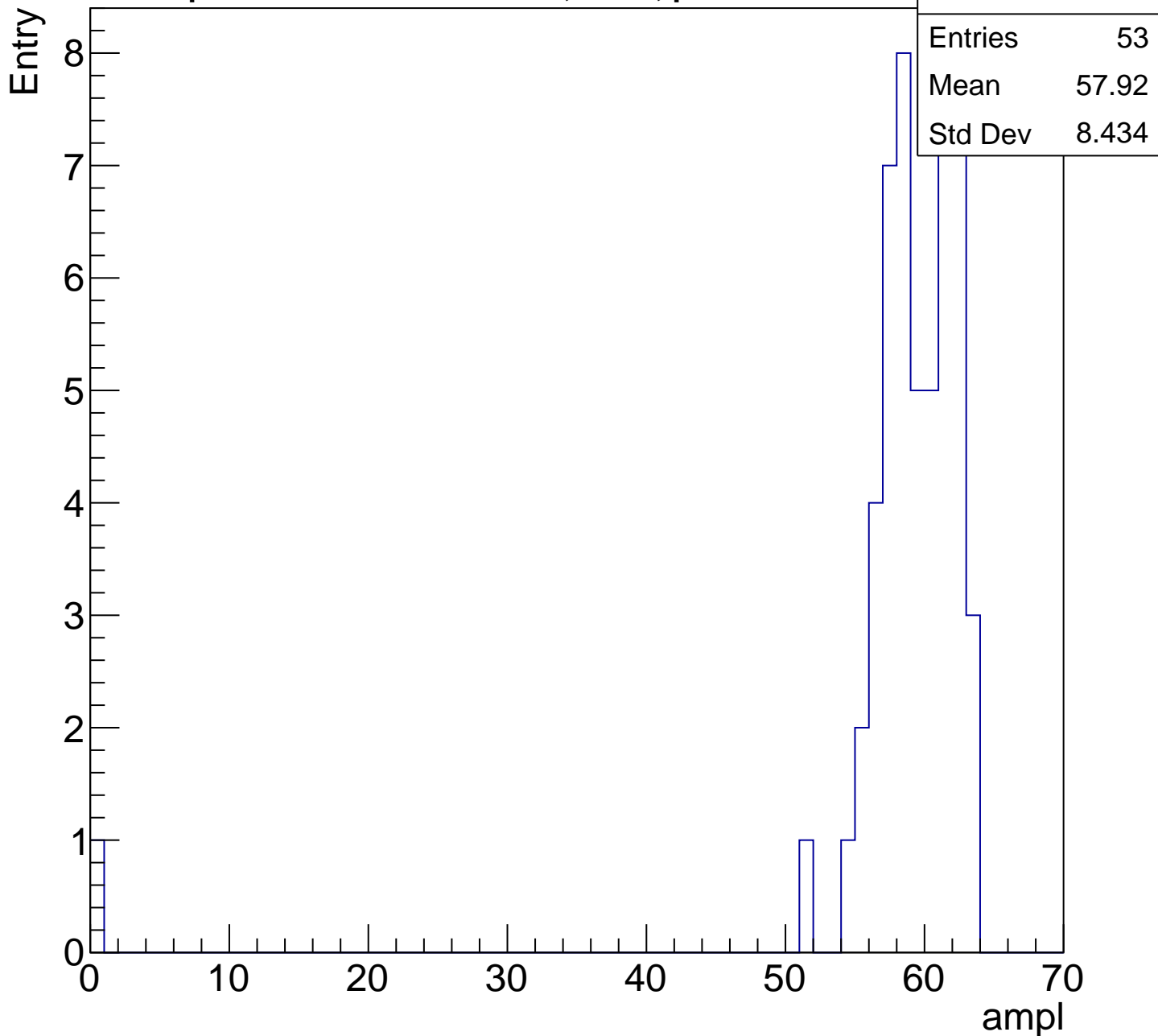
Entry

Entries	63
Mean	54.13
Std Dev	3.471



# B0L000S, U7-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

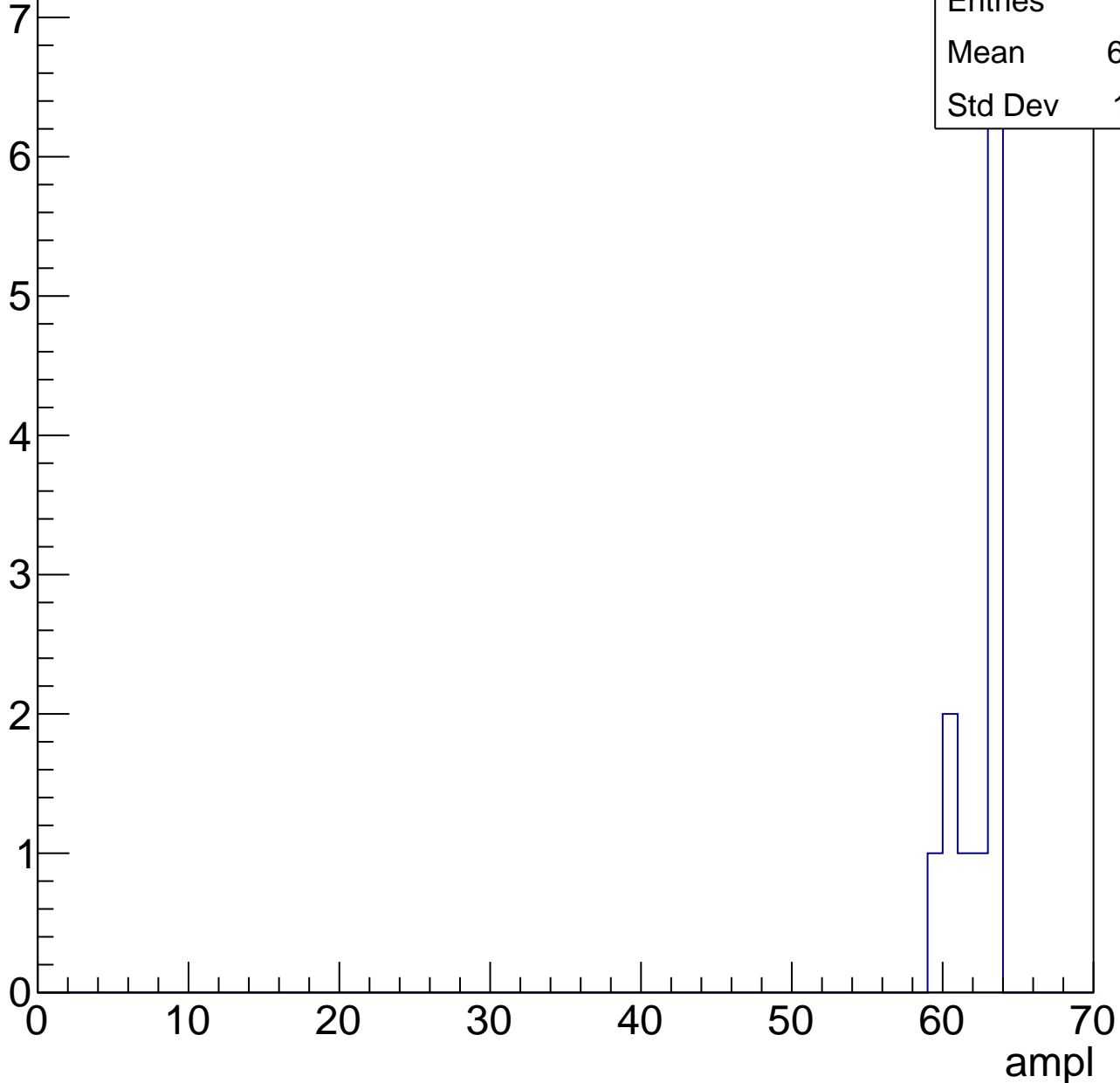


# B0L000S, U7-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	12
Mean	61.92
Std Dev	1.441





# B0L000S, U7-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch69, adc0

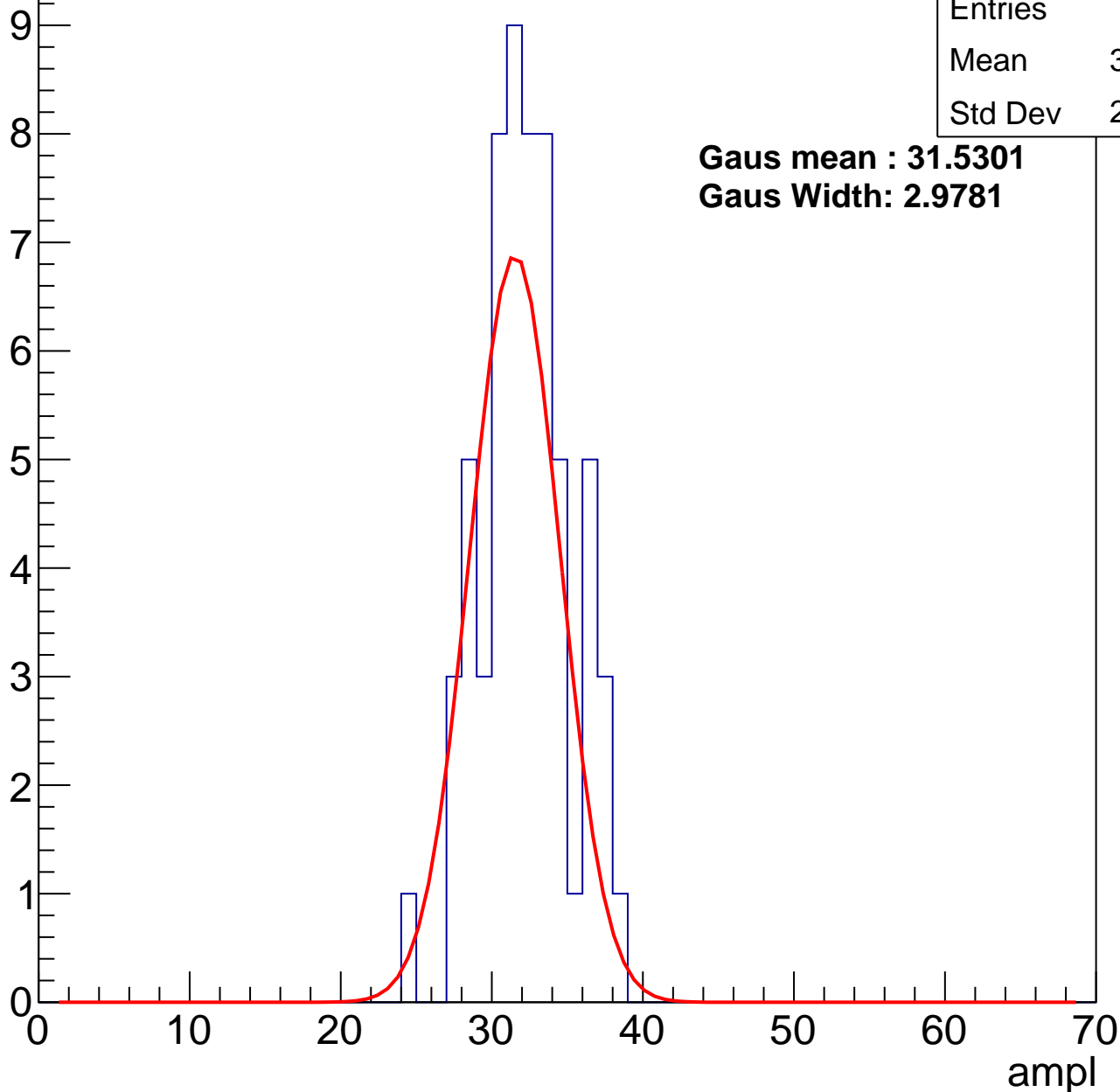
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	60
Mean	31.75
Std Dev	2.919

**Gaus mean : 31.5301**

**Gaus Width: 2.9781**



# B0L000S, U7-ch69, adc1

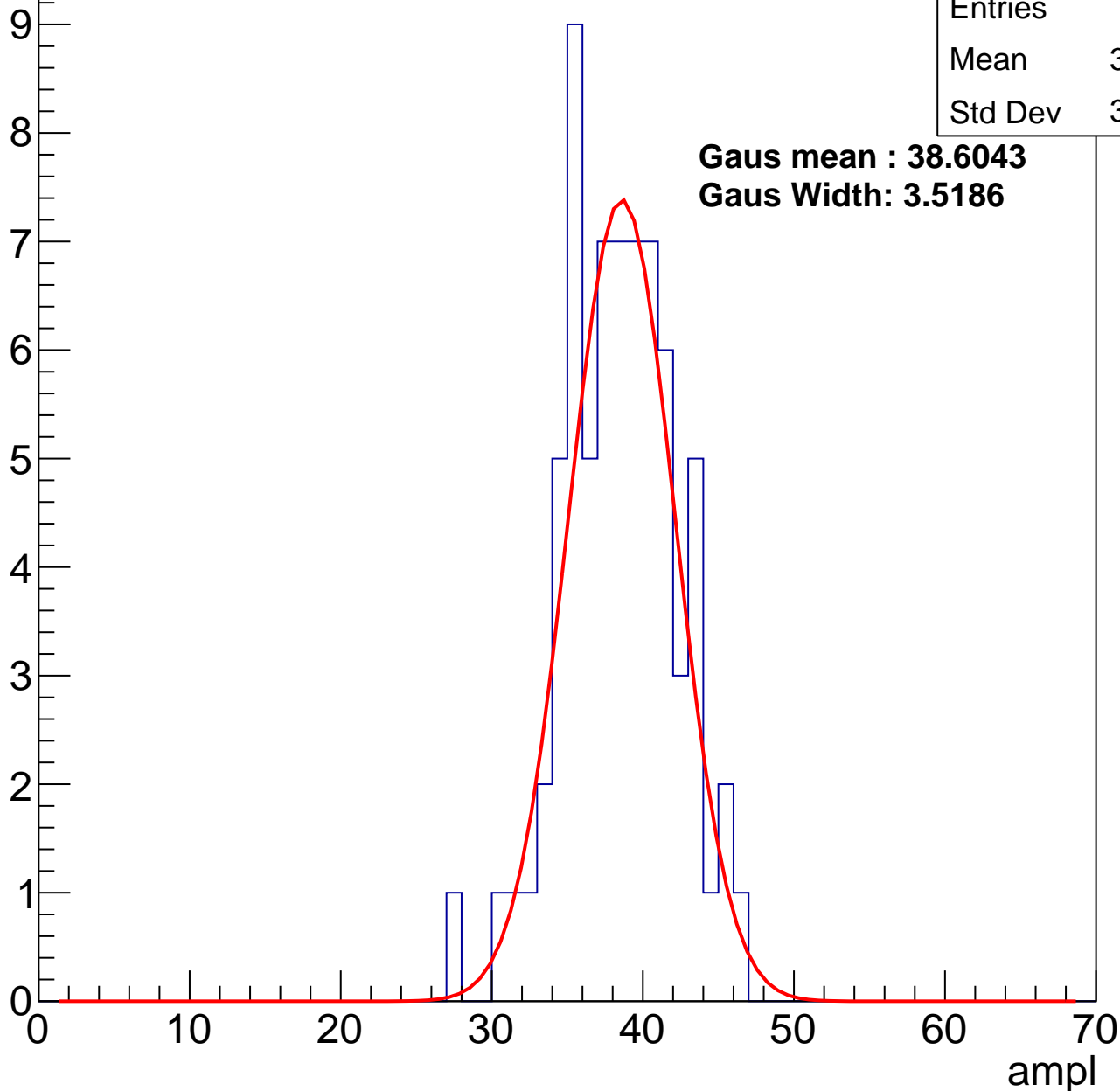
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	71
Mean	37.97
Std Dev	3.692

**Gaus mean : 38.6043**

**Gaus Width: 3.5186**



# B0L000S, U7-ch69, adc2

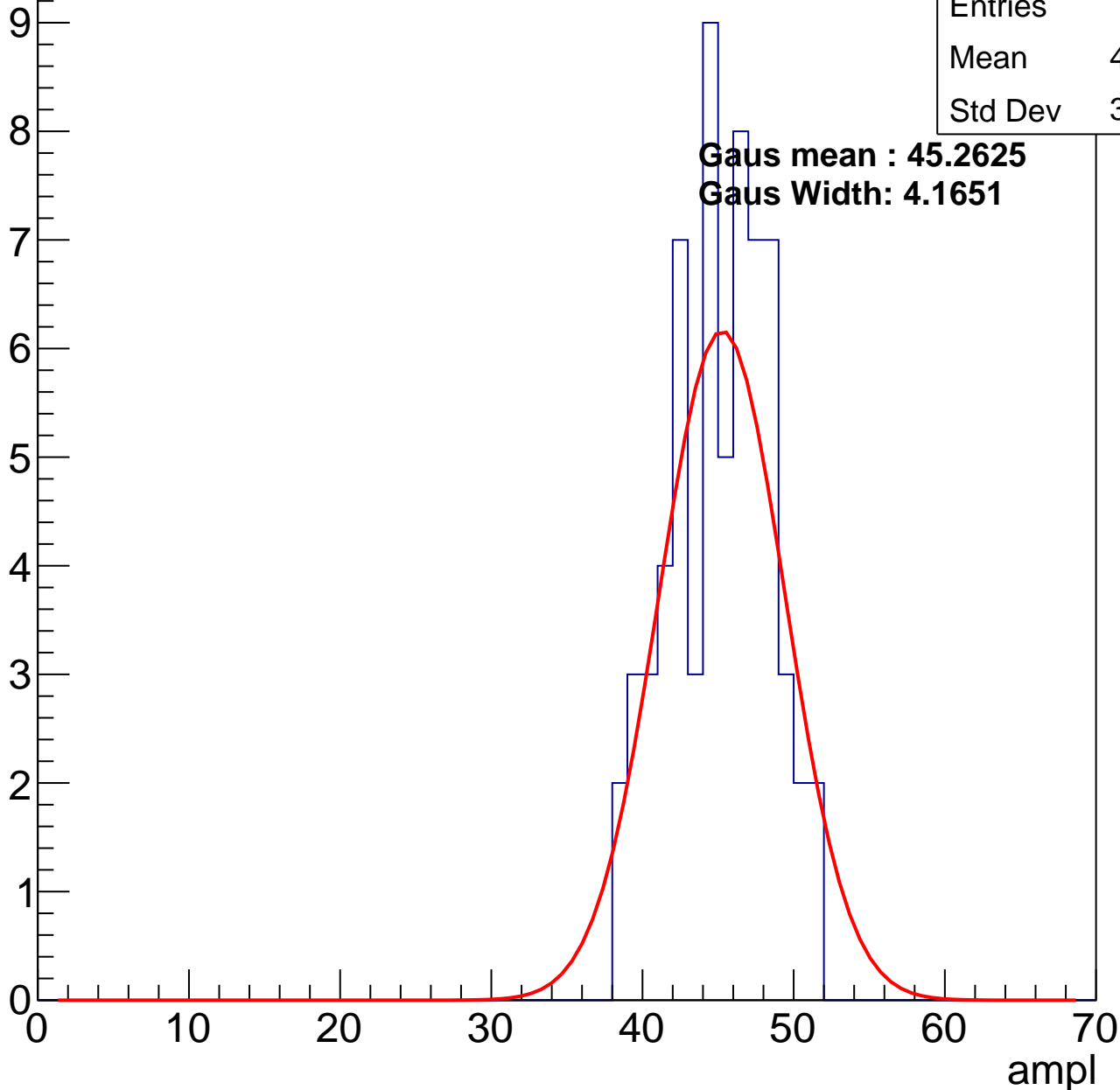
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	65
Mean	44.66
Std Dev	3.259

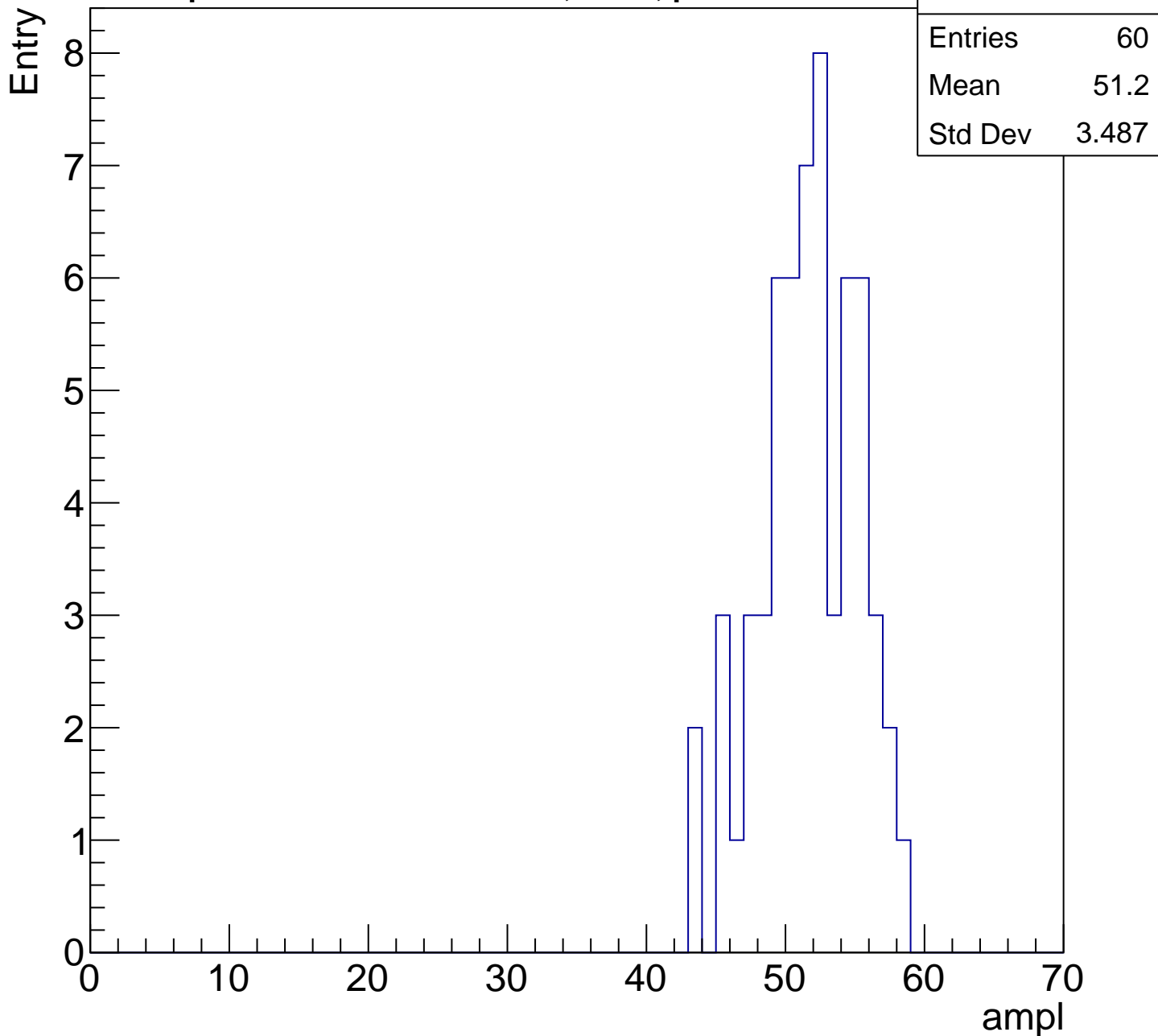
**Gaus mean : 45.2625**

**Gaus Width: 4.1651**



# B0L000S, U7-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

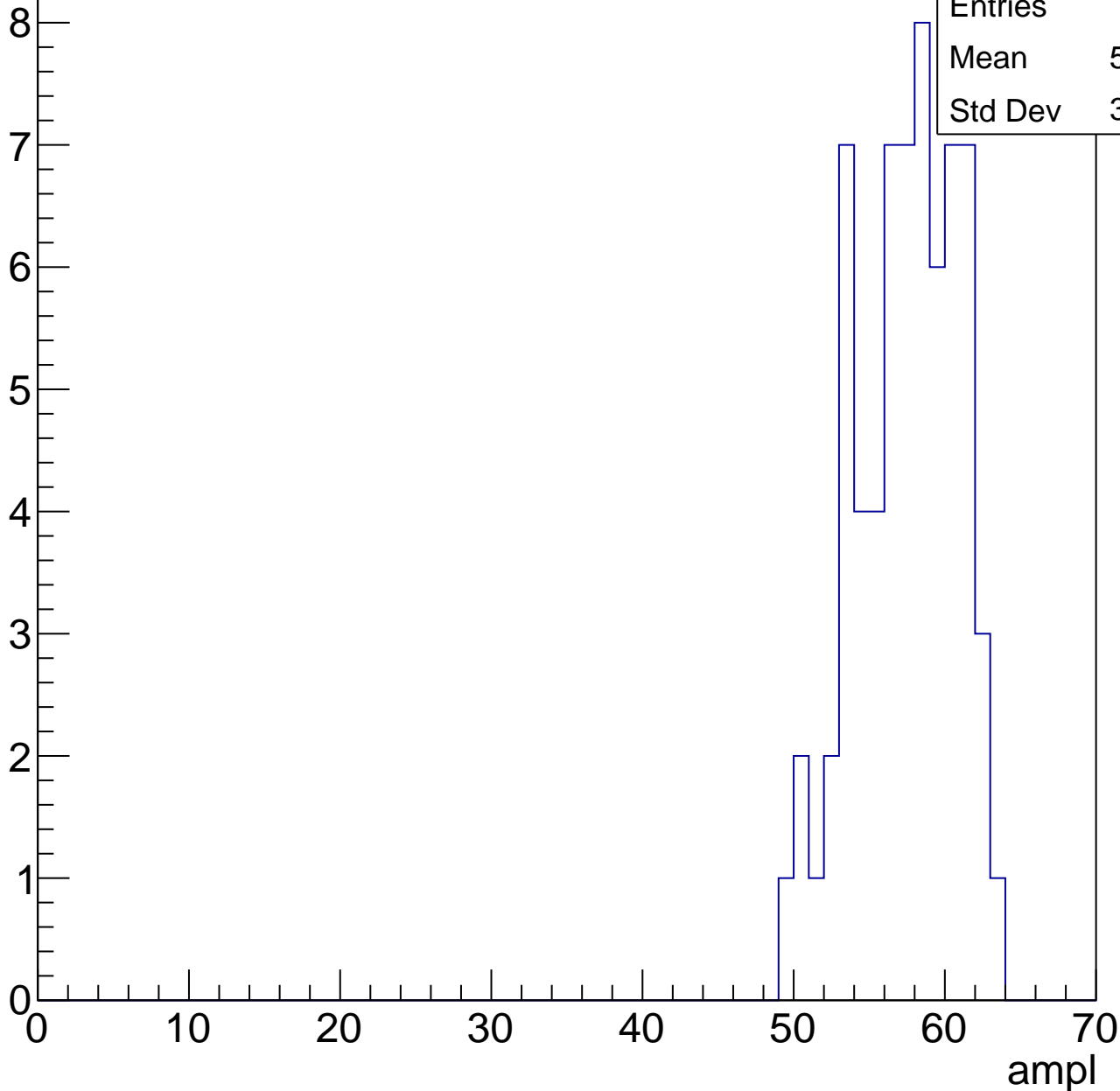


# B0L000S, U7-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	67
Mean	56.96
Std Dev	3.316



# B0L000S, U7-ch69, adc5

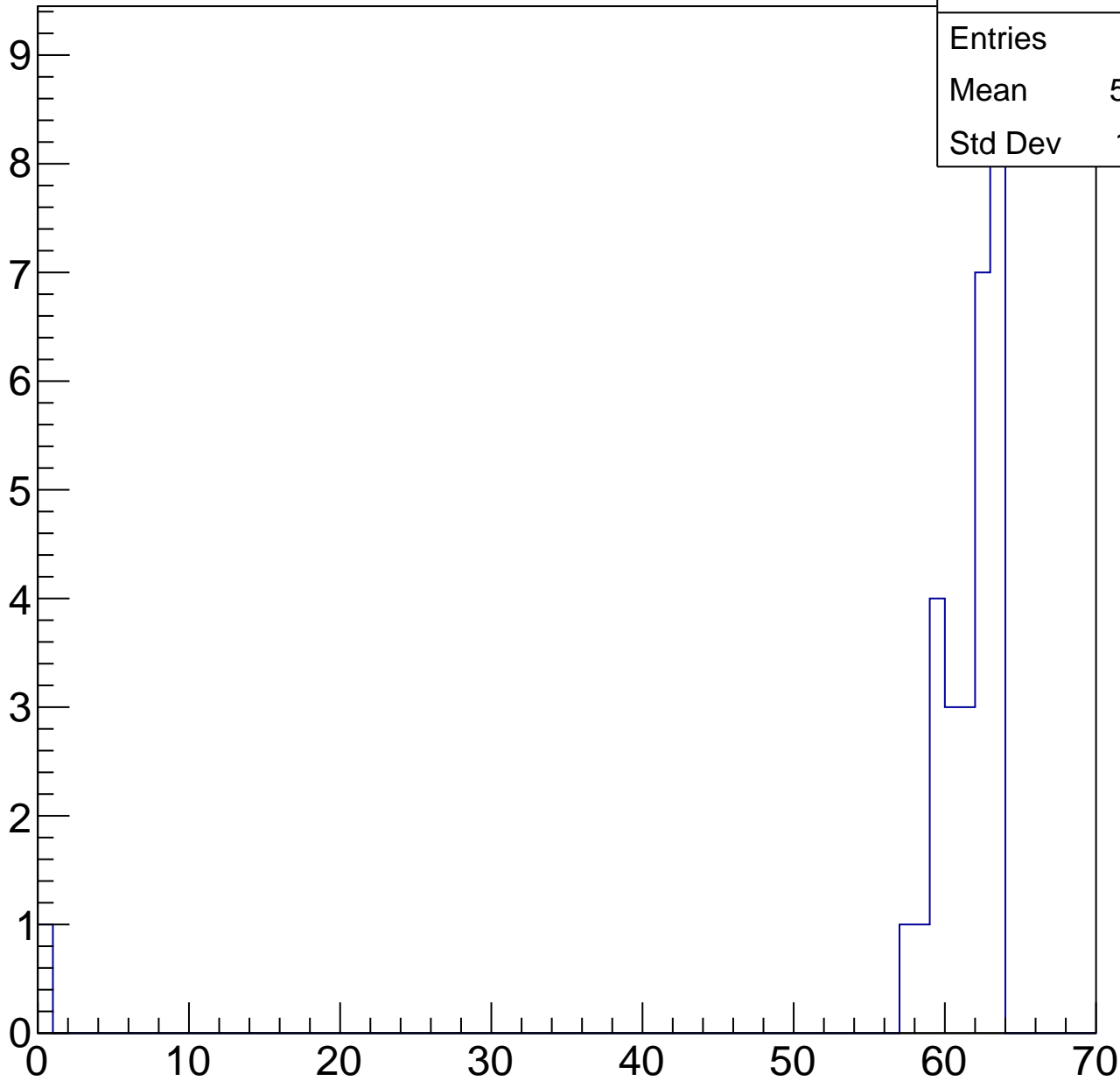
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	29
Mean	59.14
Std Dev	11.31

ampl



# B0L000S, U7-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L000S, U7-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch70, adc0

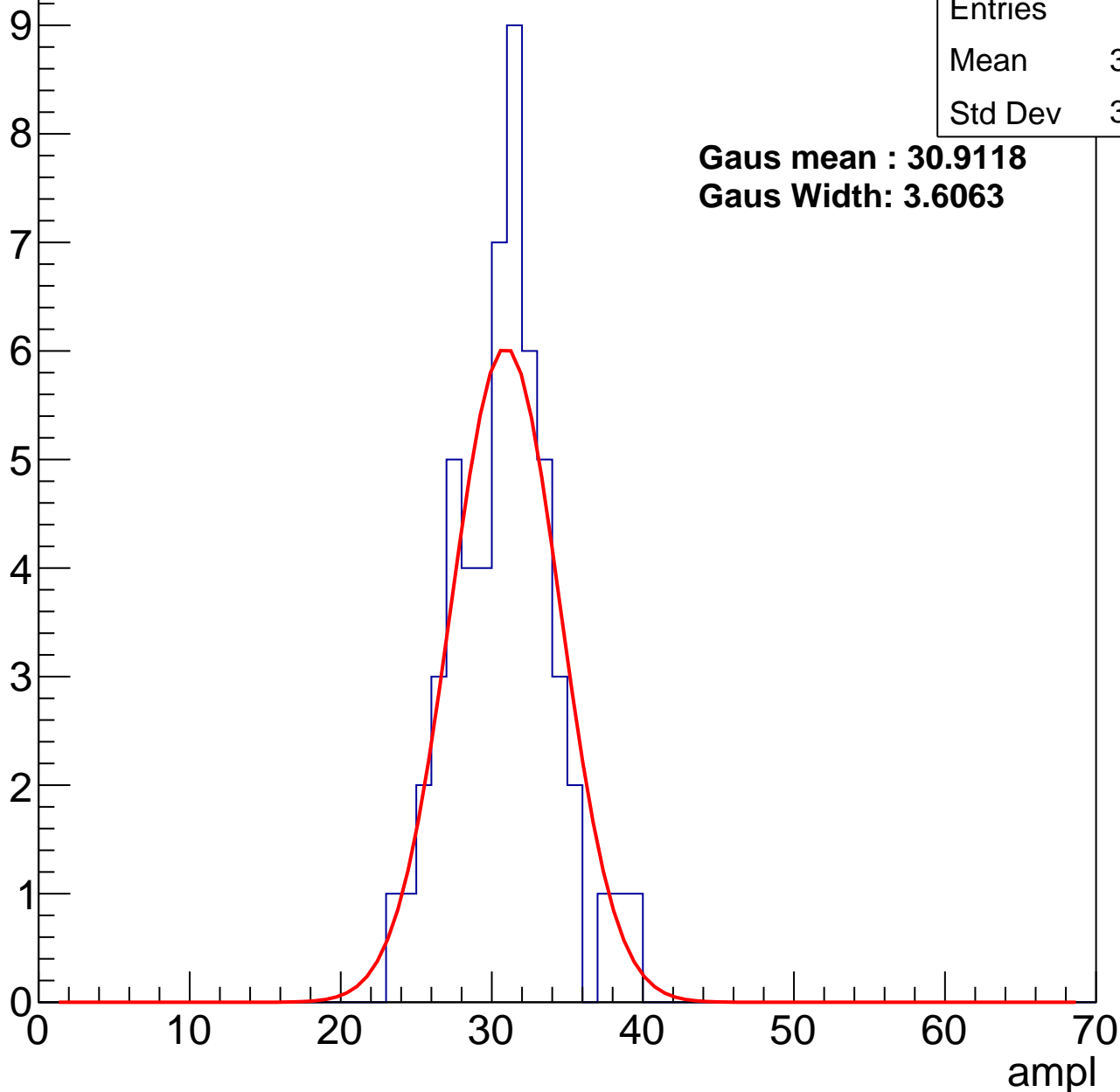
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	55
Mean	30.36
Std Dev	3.332

**Gaus mean : 30.9118**

**Gaus Width: 3.6063**



# B0L000S, U7-ch70, adc1

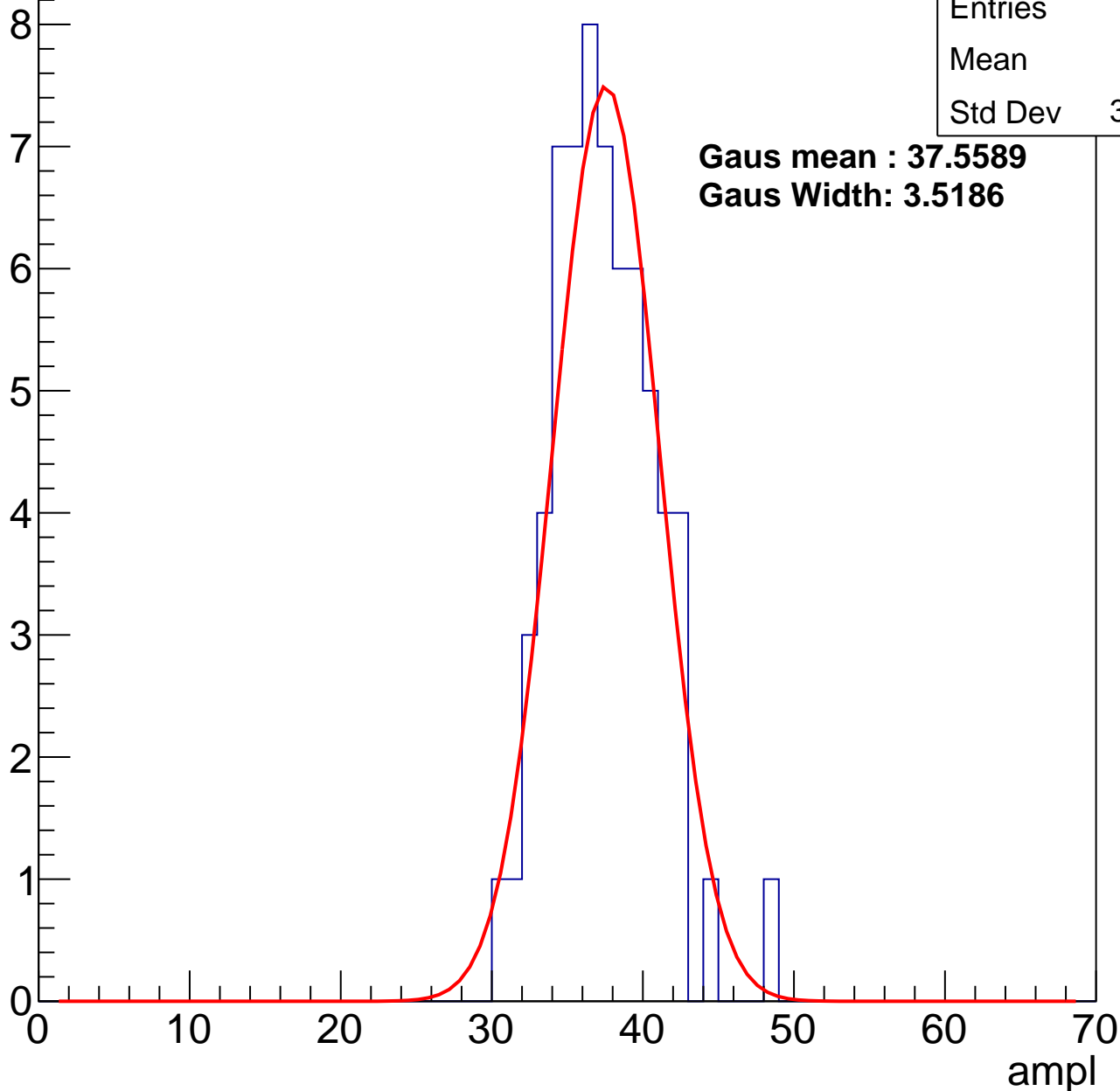
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	65
Mean	37
Std Dev	3.356

**Gaus mean : 37.5589**

**Gaus Width: 3.5186**



# B0L000S, U7-ch70, adc2

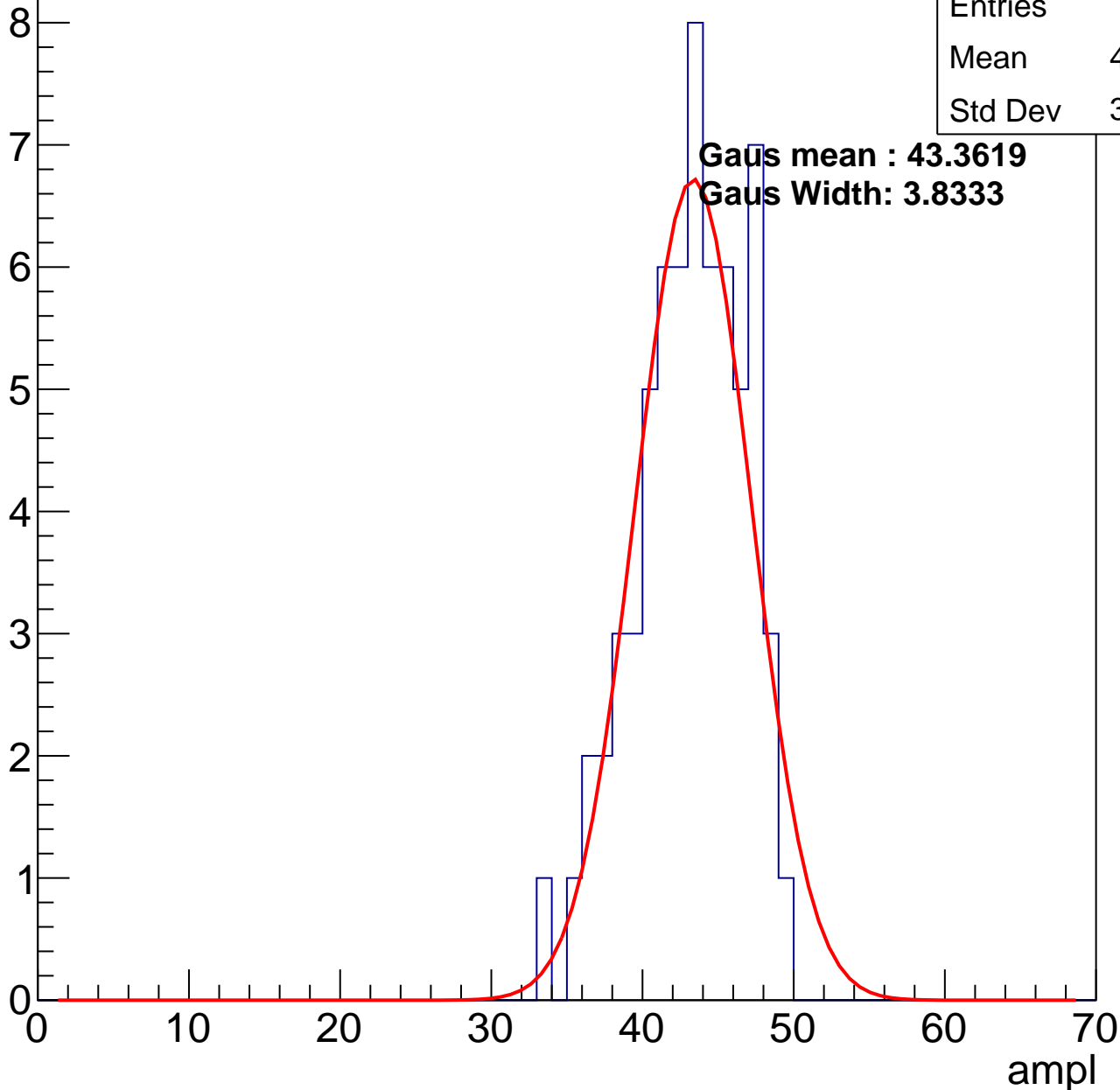
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	65
Mean	42.66
Std Dev	3.557

**Gaus mean : 43.3619**

**Gaus Width: 3.8333**

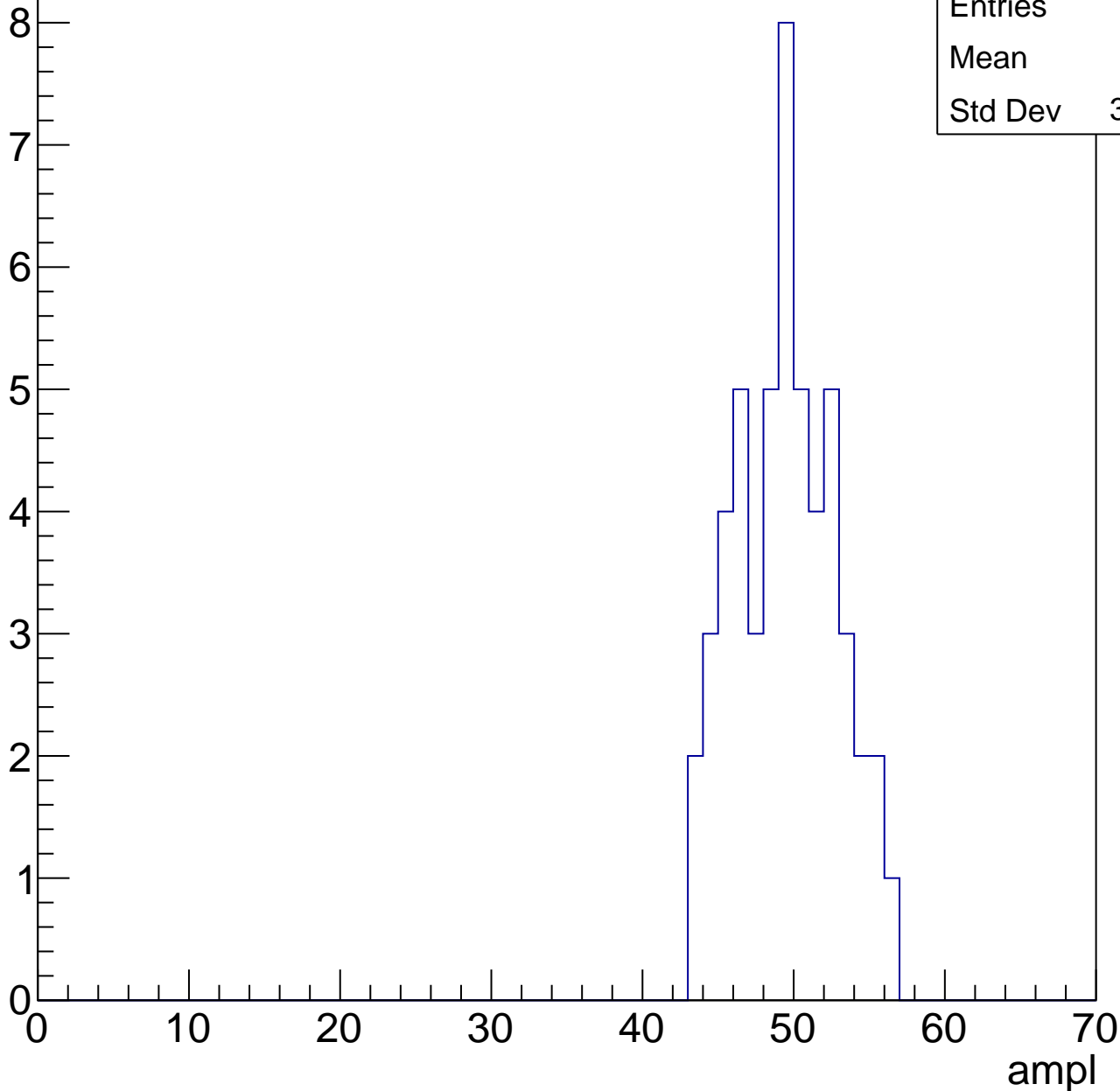


# B0L000S, U7-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	52
Mean	49
Std Dev	3.276

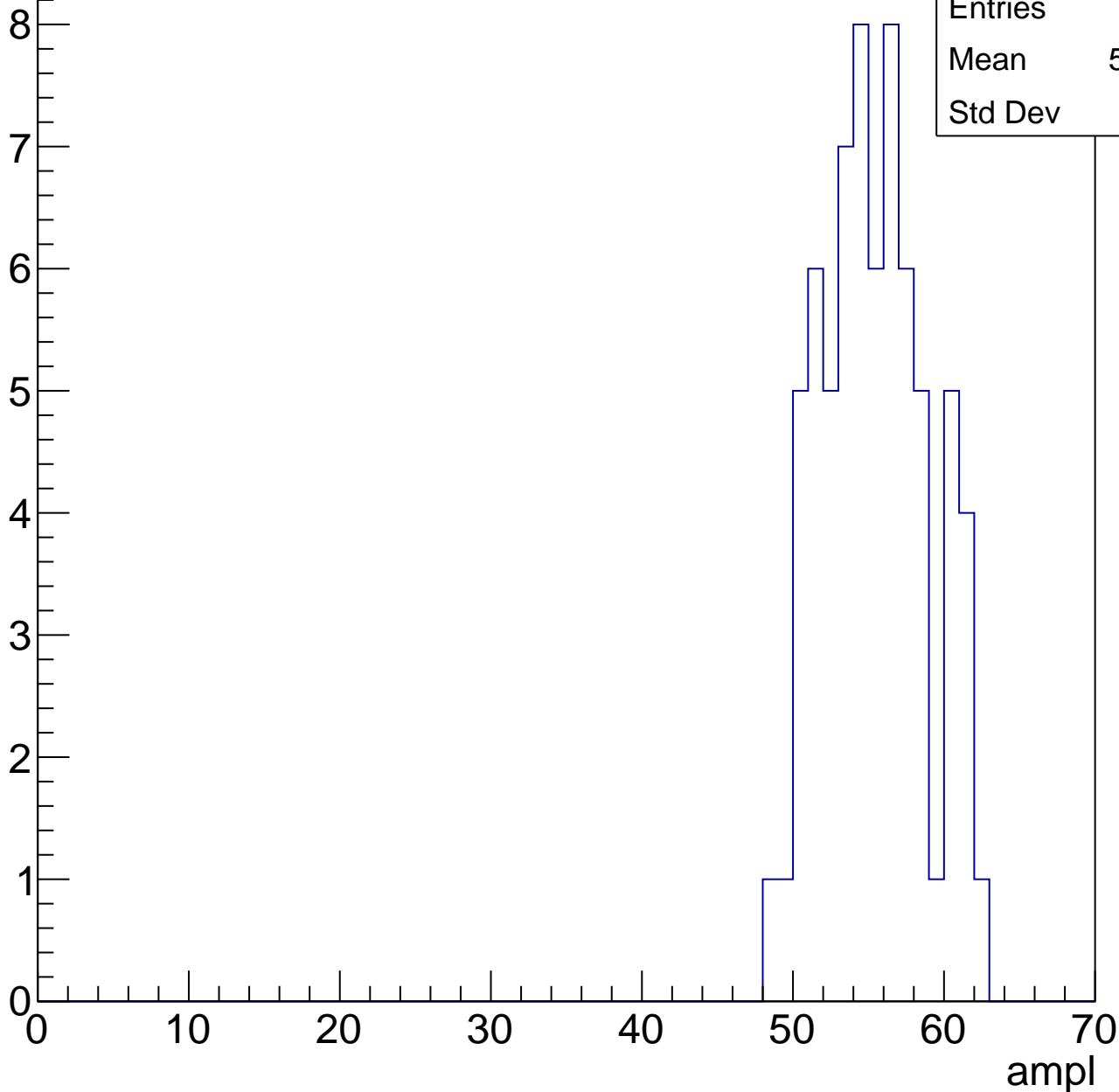


# B0L000S, U7-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	69
Mean	54.94
Std Dev	3.4



# B0L000S, U7-ch70, adc5

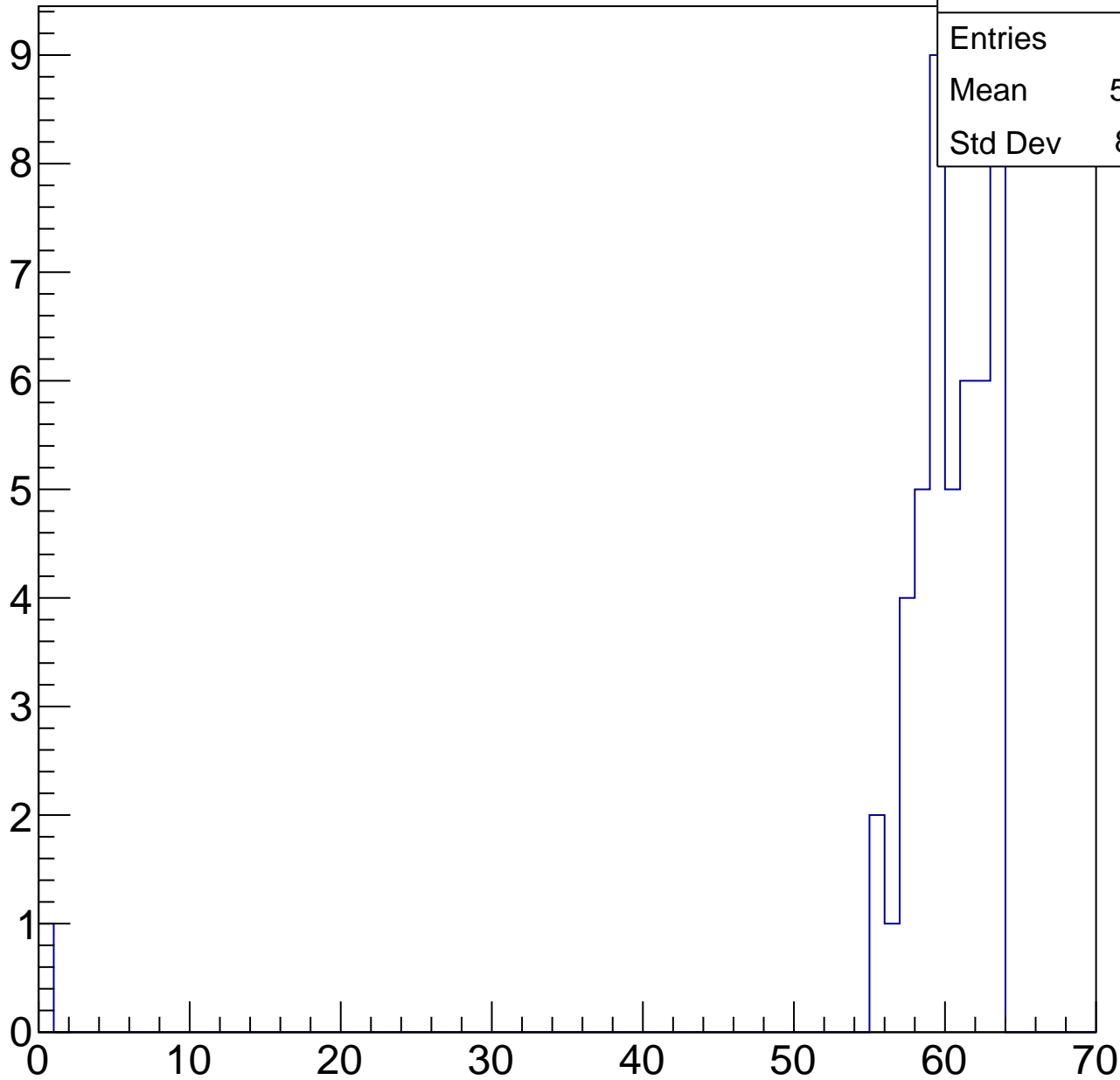
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	47
Mean	58.66
Std Dev	8.931

ampl



# B0L000S, U7-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

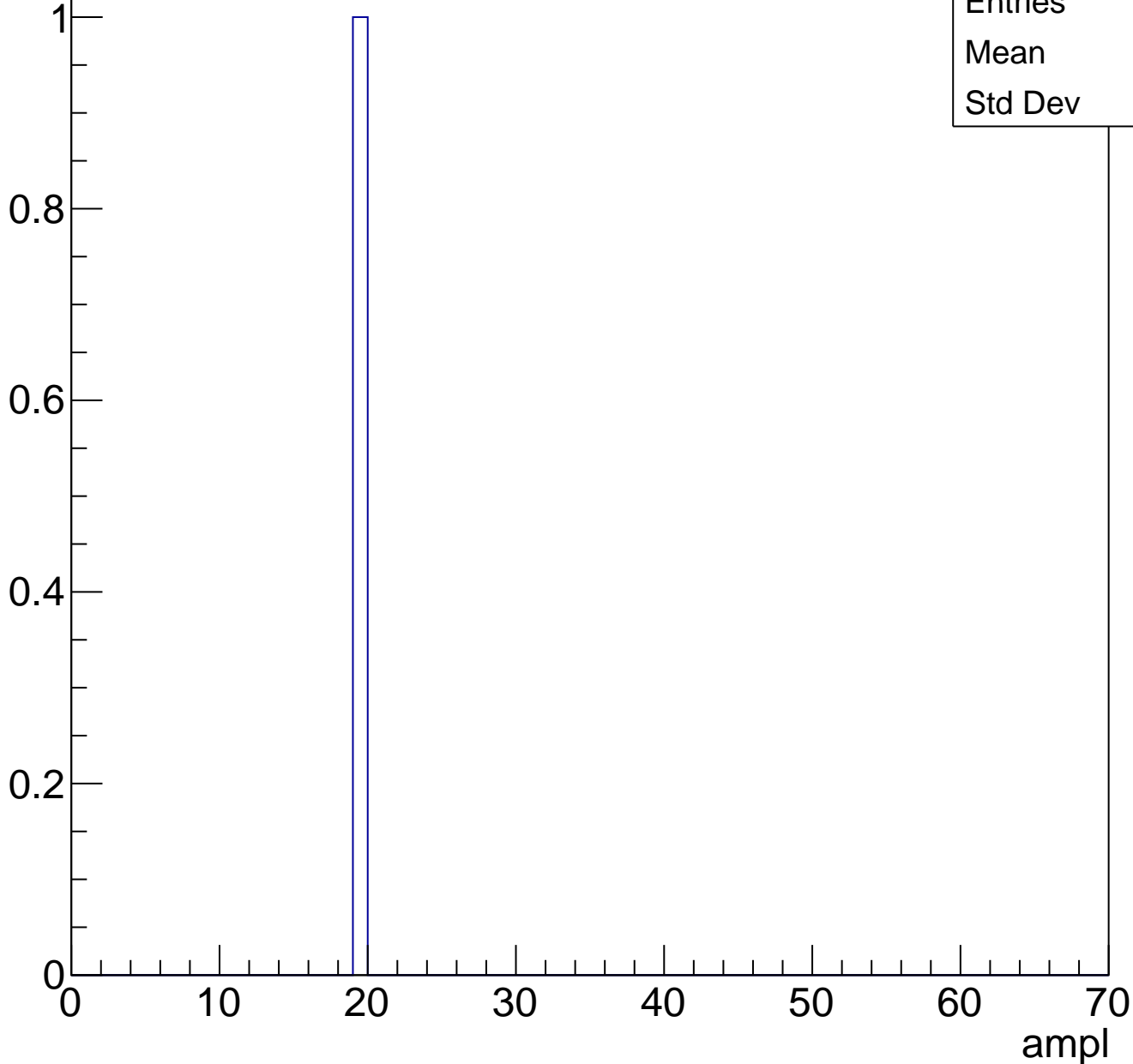




# B0L000S, U7-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch71, adc0

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	71
Mean	30.62
Std Dev	3.096

**Gaus mean : 31.3528**

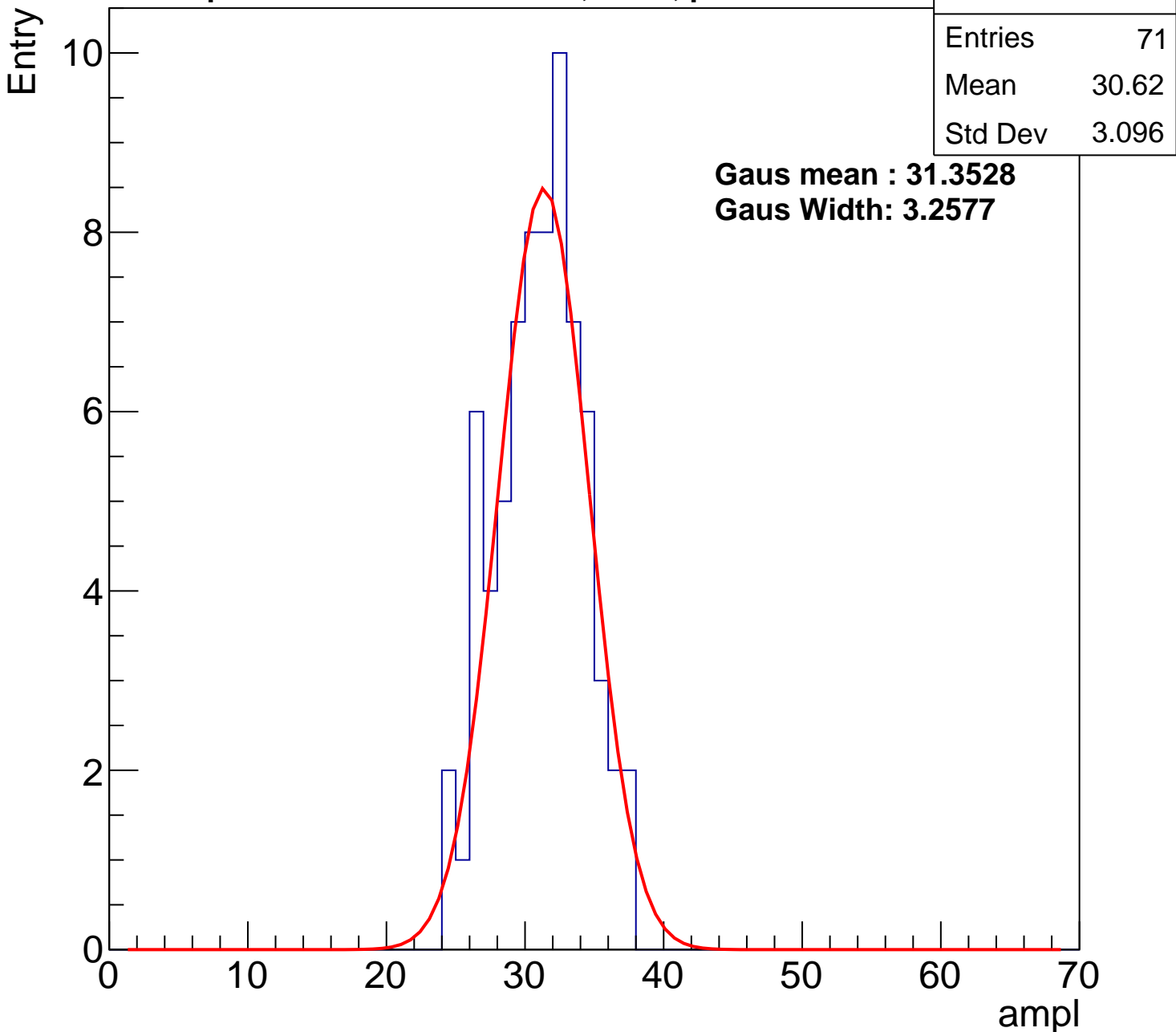
**Gaus Width: 3.2577**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L000S, U7-ch71, adc1

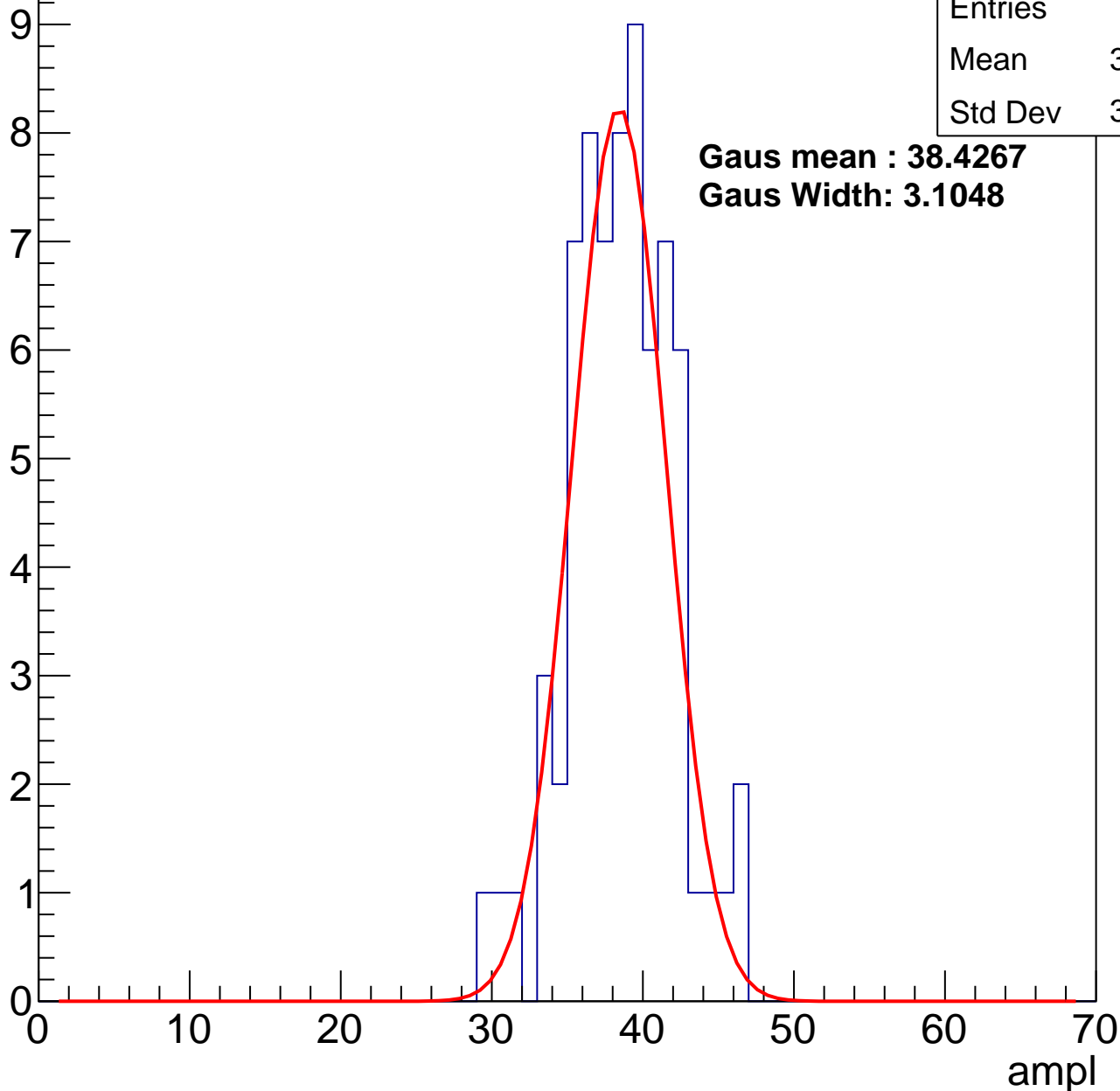
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	71
Mean	38.13
Std Dev	3.423

**Gaus mean : 38.4267**

**Gaus Width: 3.1048**



# B0L000S, U7-ch71, adc2

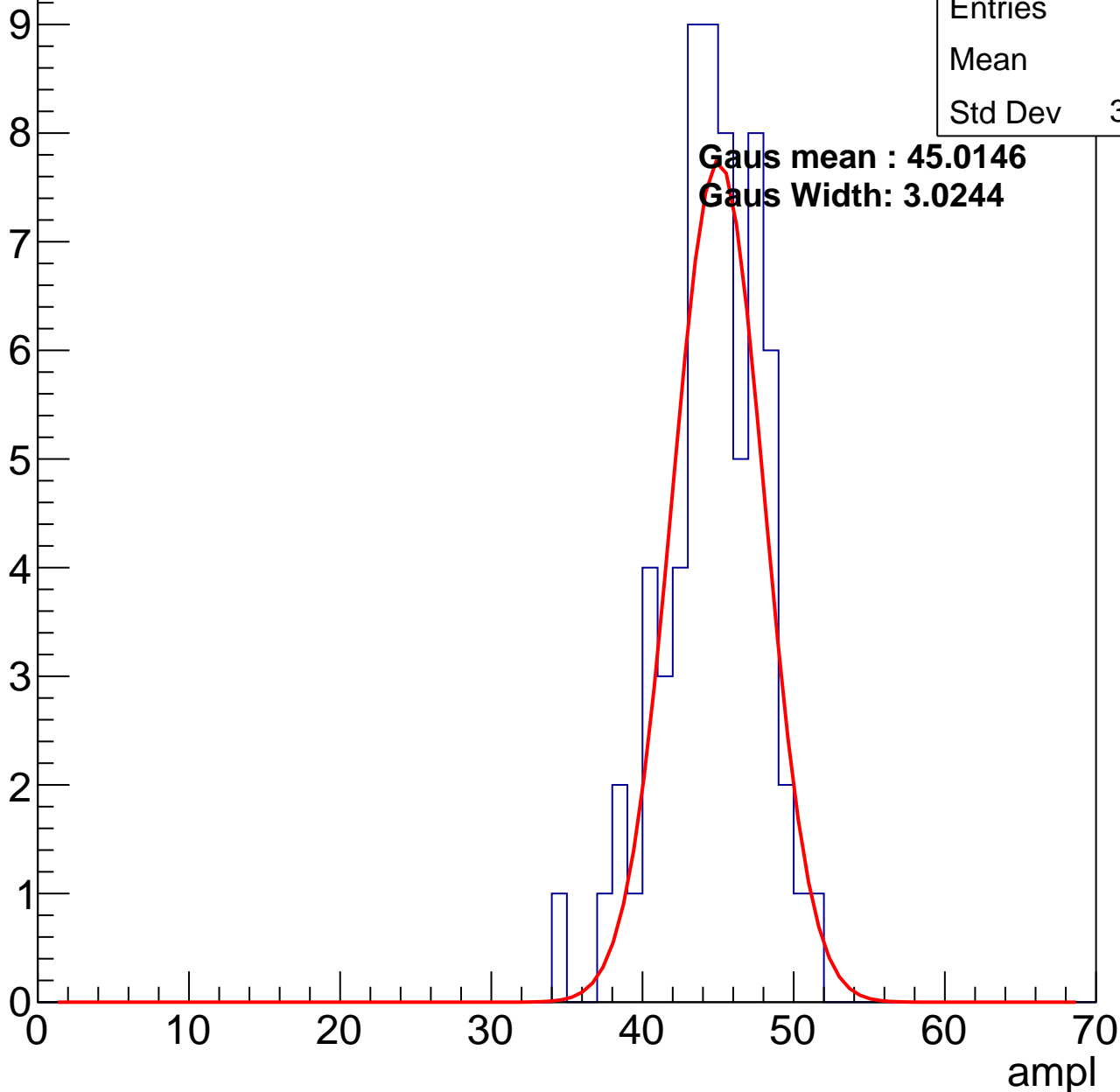
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	65
Mean	44.2
Std Dev	3.259

**Gaus mean : 45.0146**

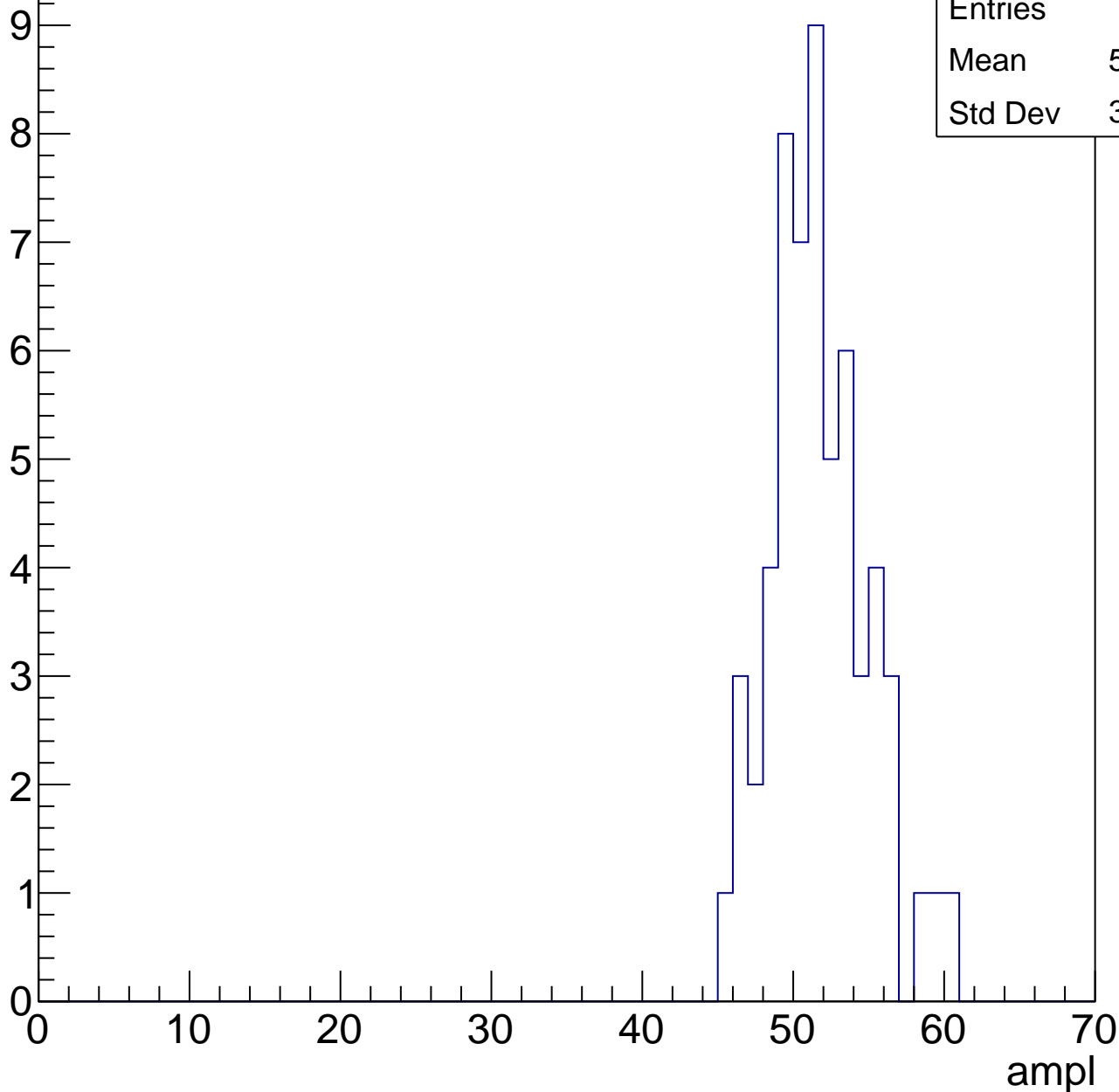
**Gaus Width: 3.0244**



# B0L000S, U7-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	70
Mean	56.94
Std Dev	3.171

Entry

10

8

6

4

2

0

0

10

20

30

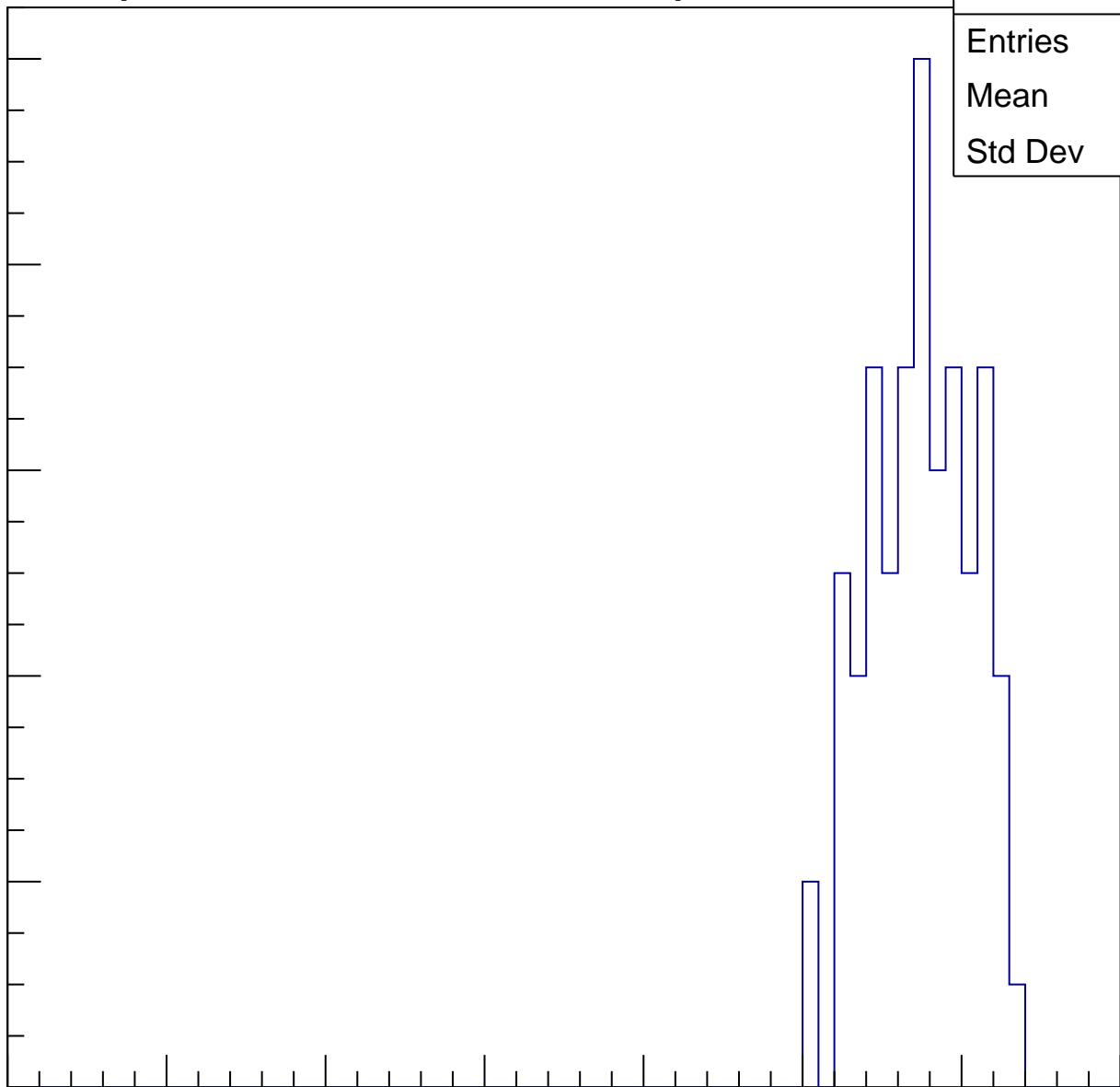
40

50

60

70

ampl

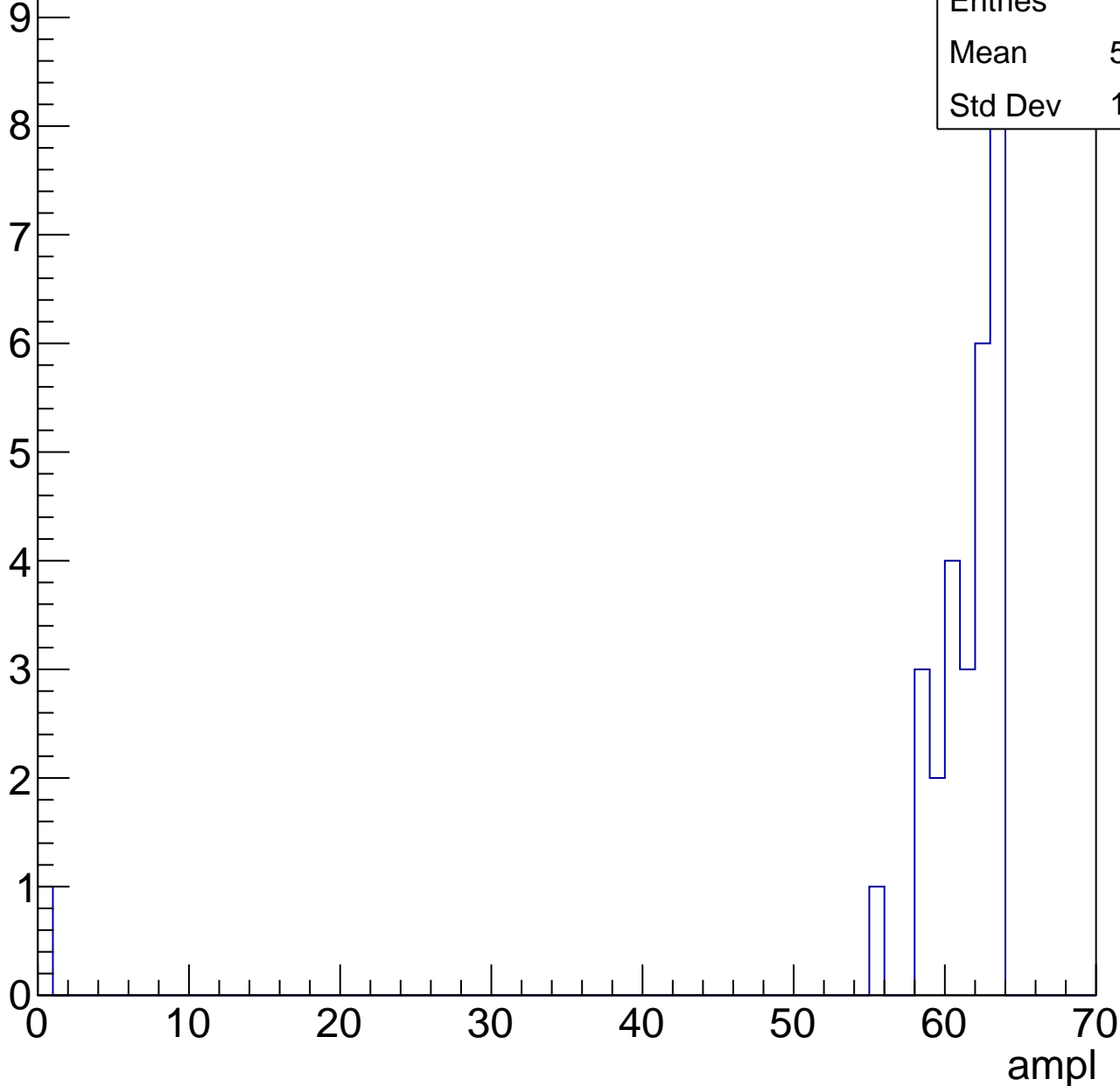


# B0L000S, U7-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	29
Mean	58.93
Std Dev	11.32



# B0L000S, U7-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L000S, U7-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	1
Mean	24
Std Dev	0

# B0L000S, U7-ch72, adc0

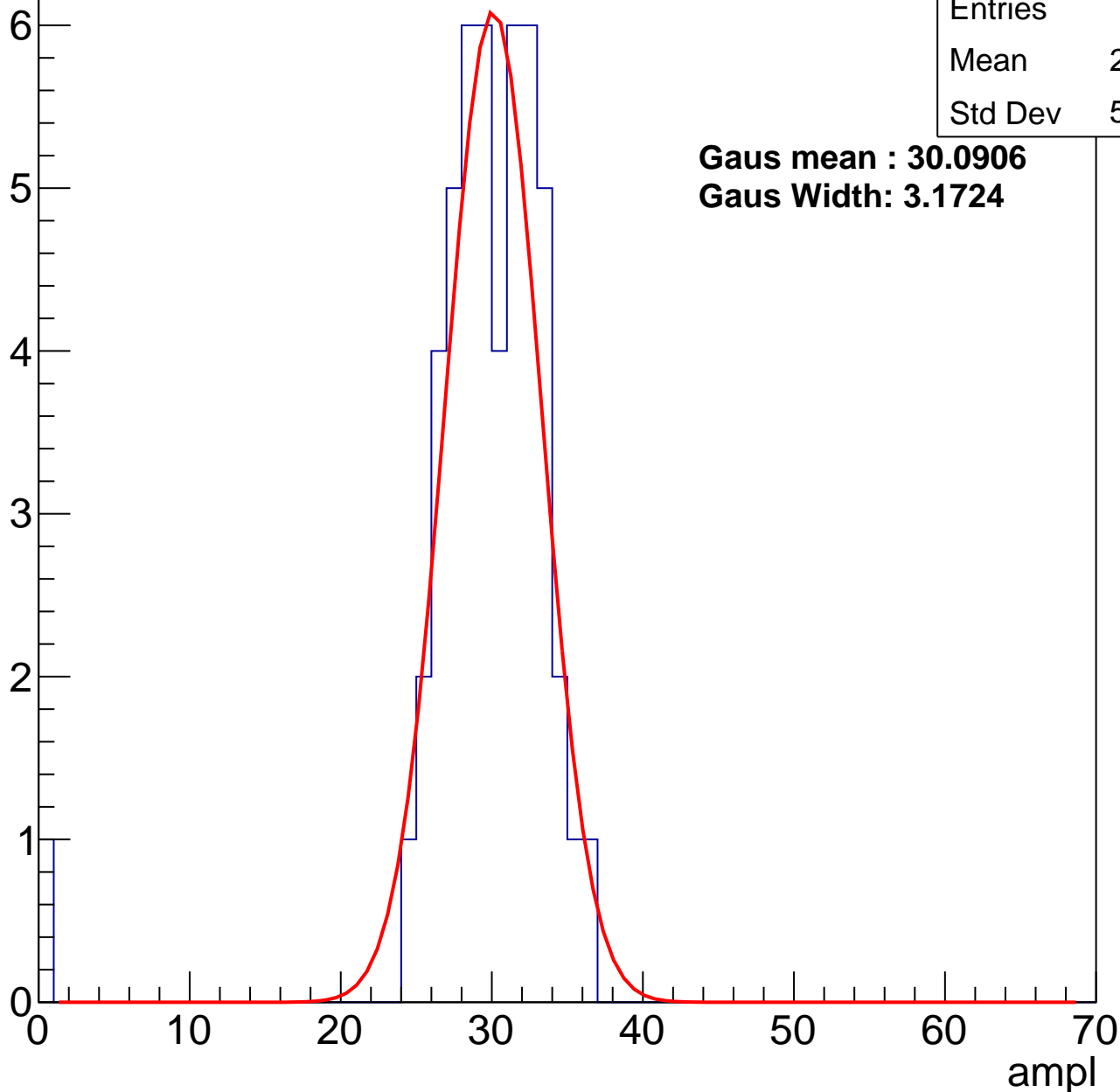
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	50
Mean	29.14
Std Dev	5.012

**Gaus mean : 30.0906**

**Gaus Width: 3.1724**



# B0L000S, U7-ch72, adc1

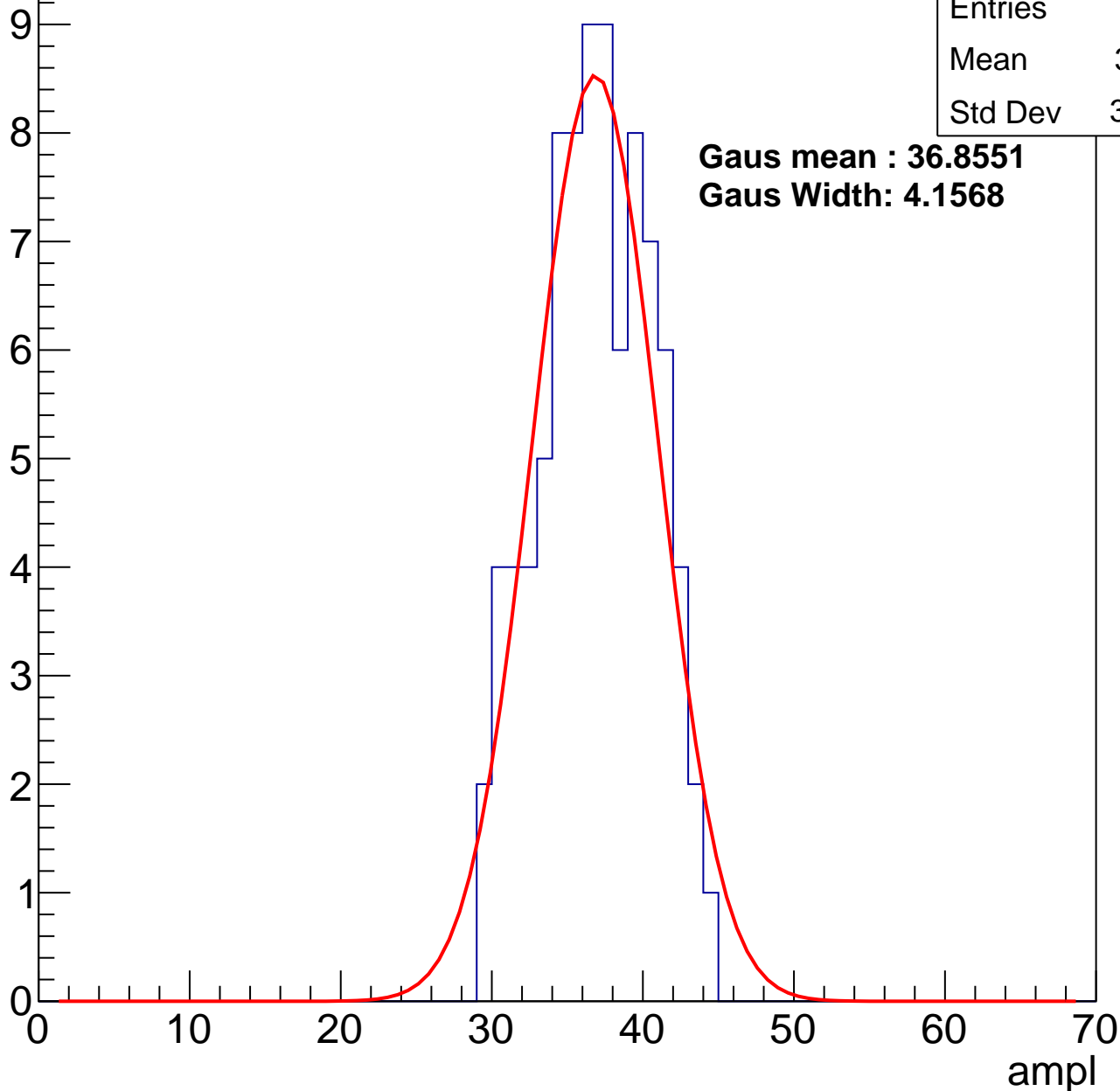
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	87
Mean	36.41
Std Dev	3.634

**Gaus mean : 36.8551**

**Gaus Width: 4.1568**



# B0L000S, U7-ch72, adc2

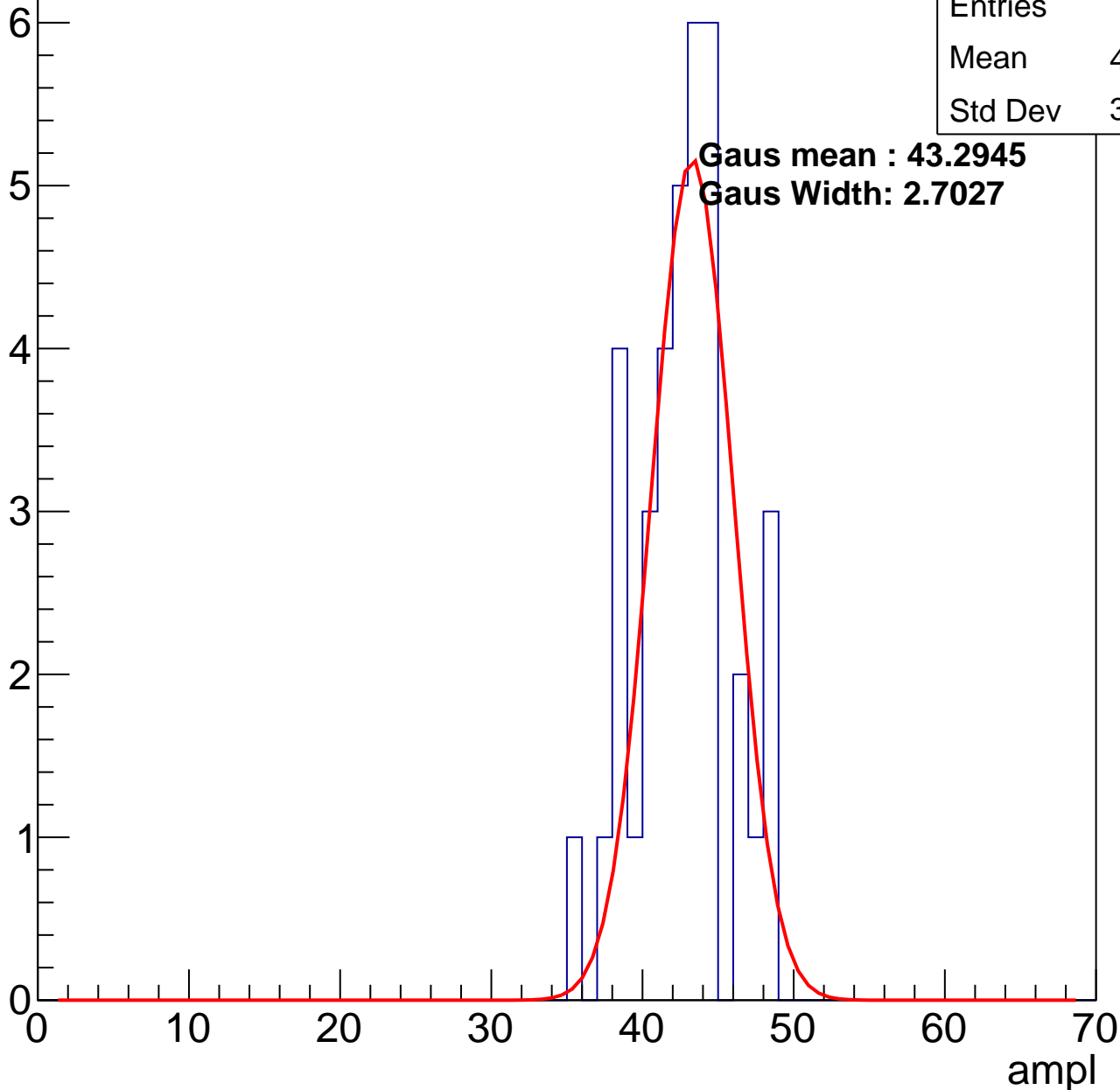
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	37
Mean	42.22
Std Dev	3.103

**Gaus mean : 43.2945**

**Gaus Width: 2.7027**

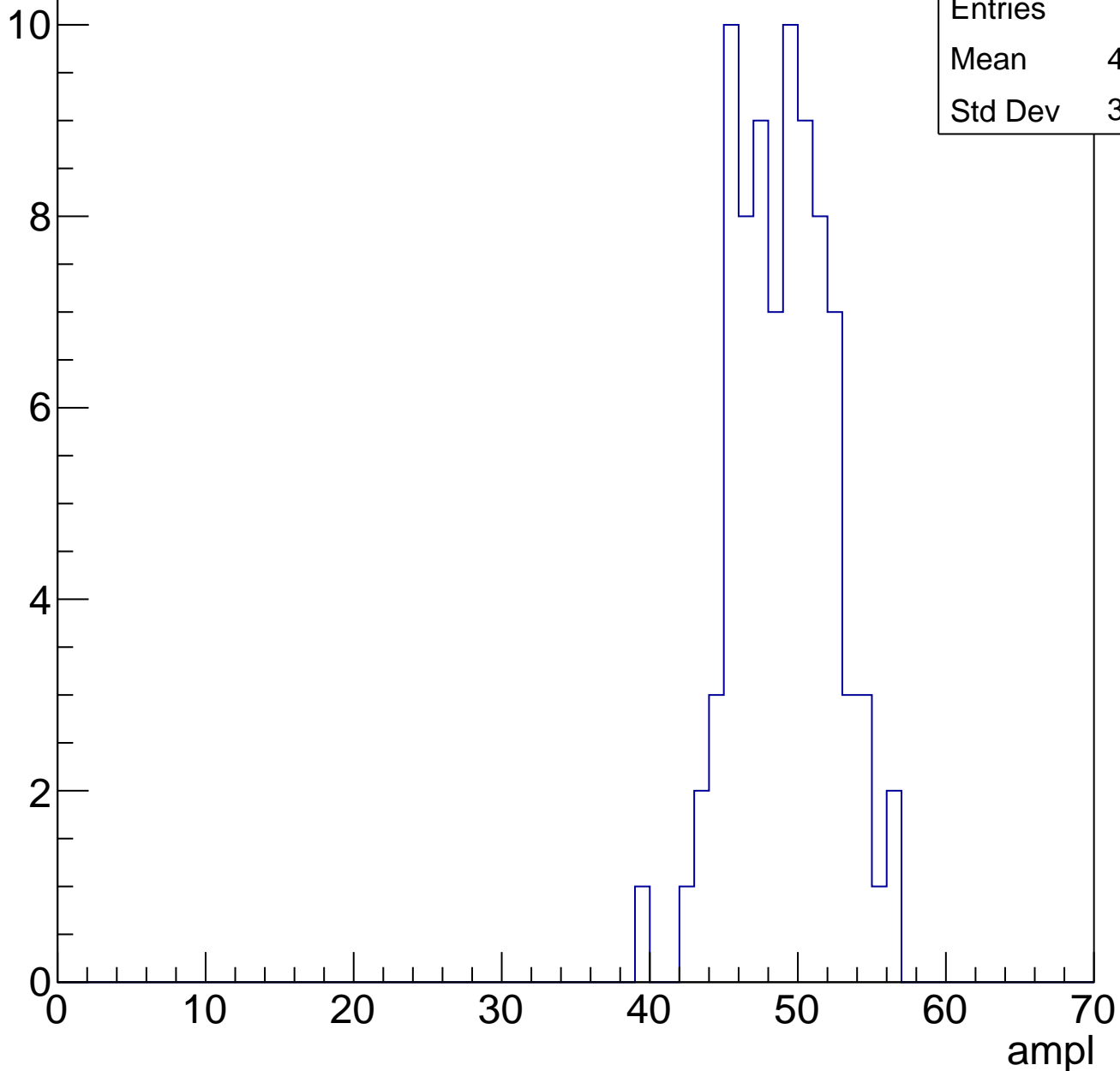


# B0L000S, U7-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	84
Mean	48.52
Std Dev	3.297

Entry

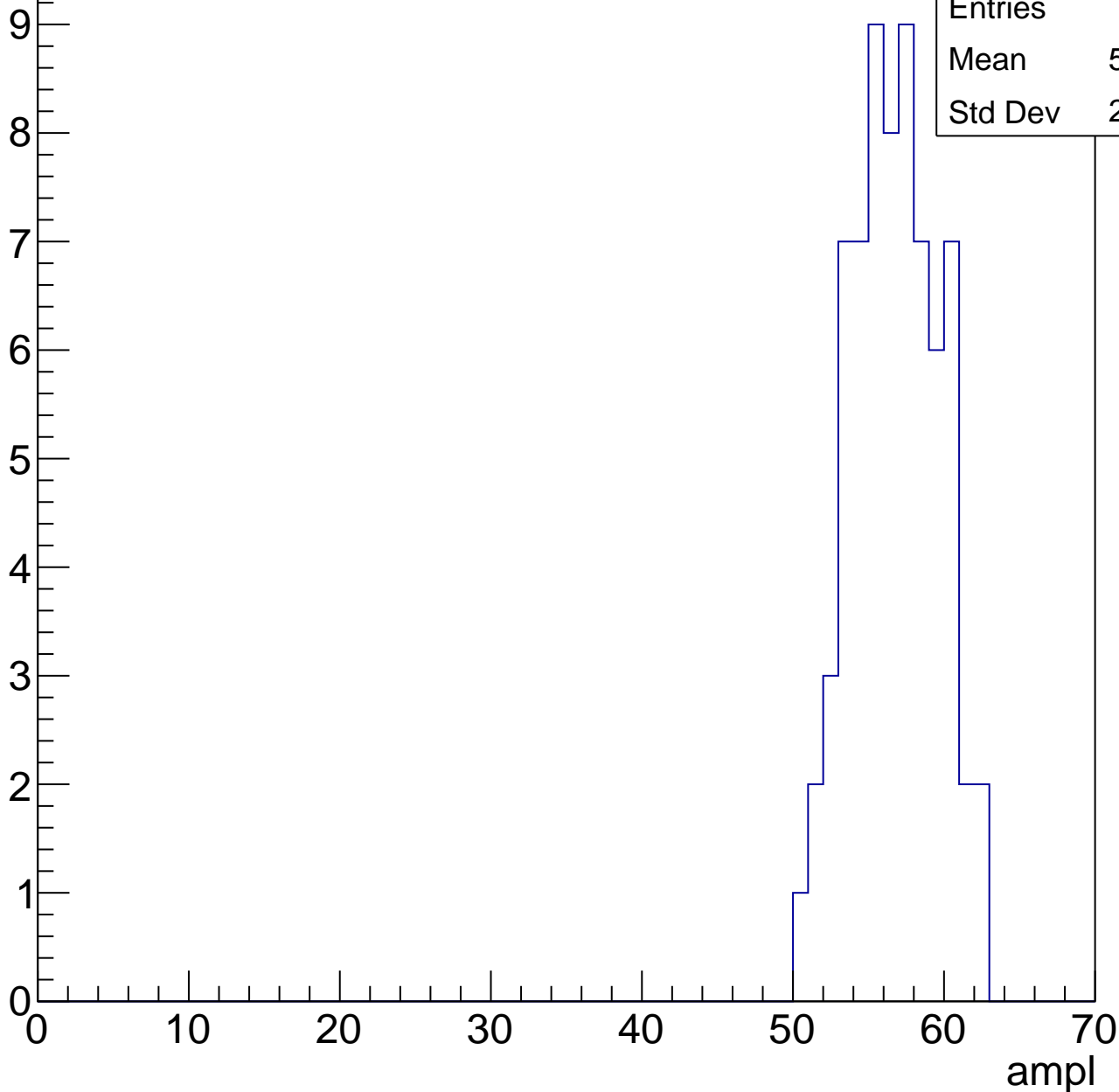


# B0L000S, U7-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	70
Mean	56.27
Std Dev	2.813



# B0L000S, U7-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	31
Mean	60.84
Std Dev	1.743

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

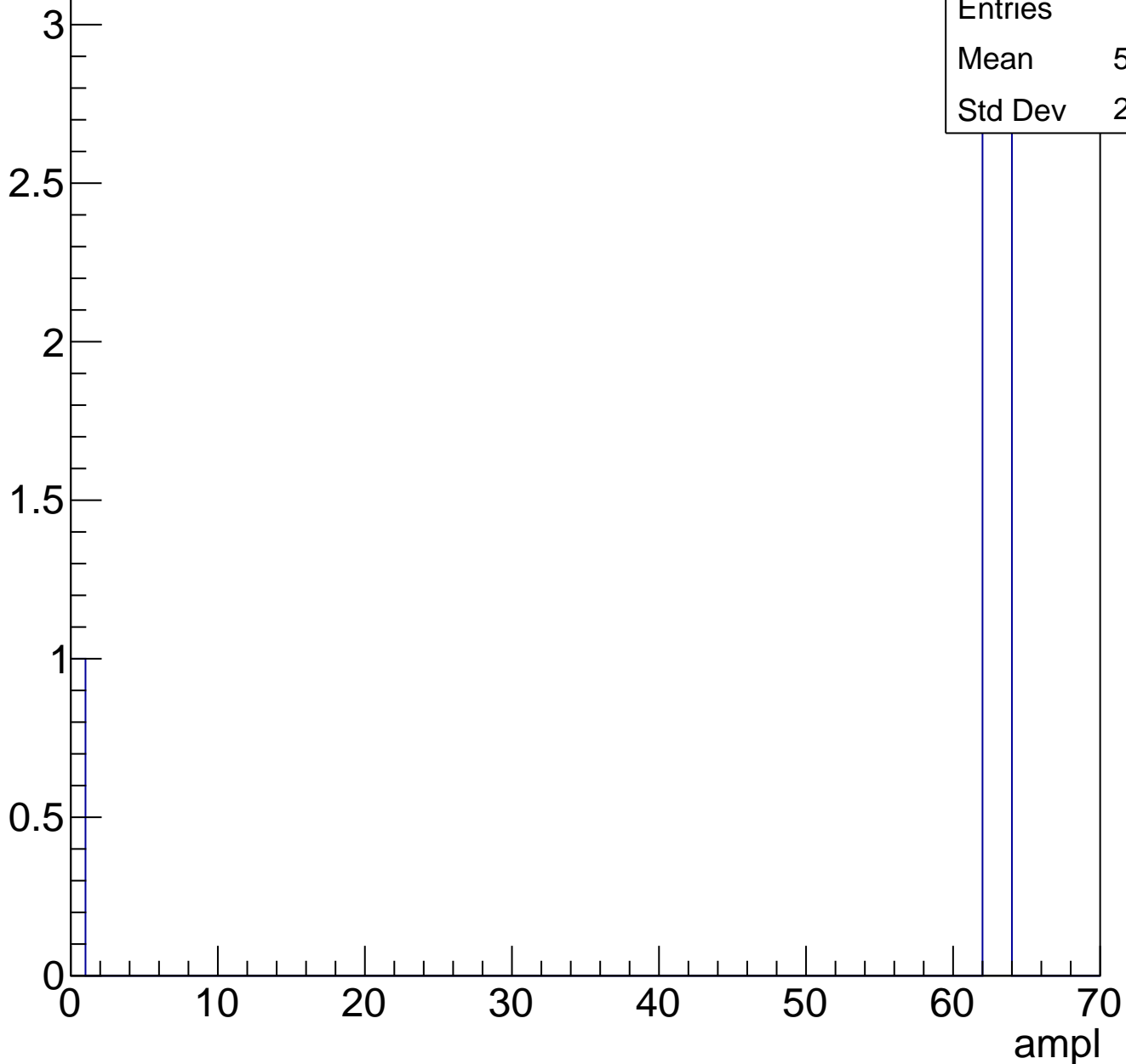
7

8

# B0L000S, U7-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch73, adc0

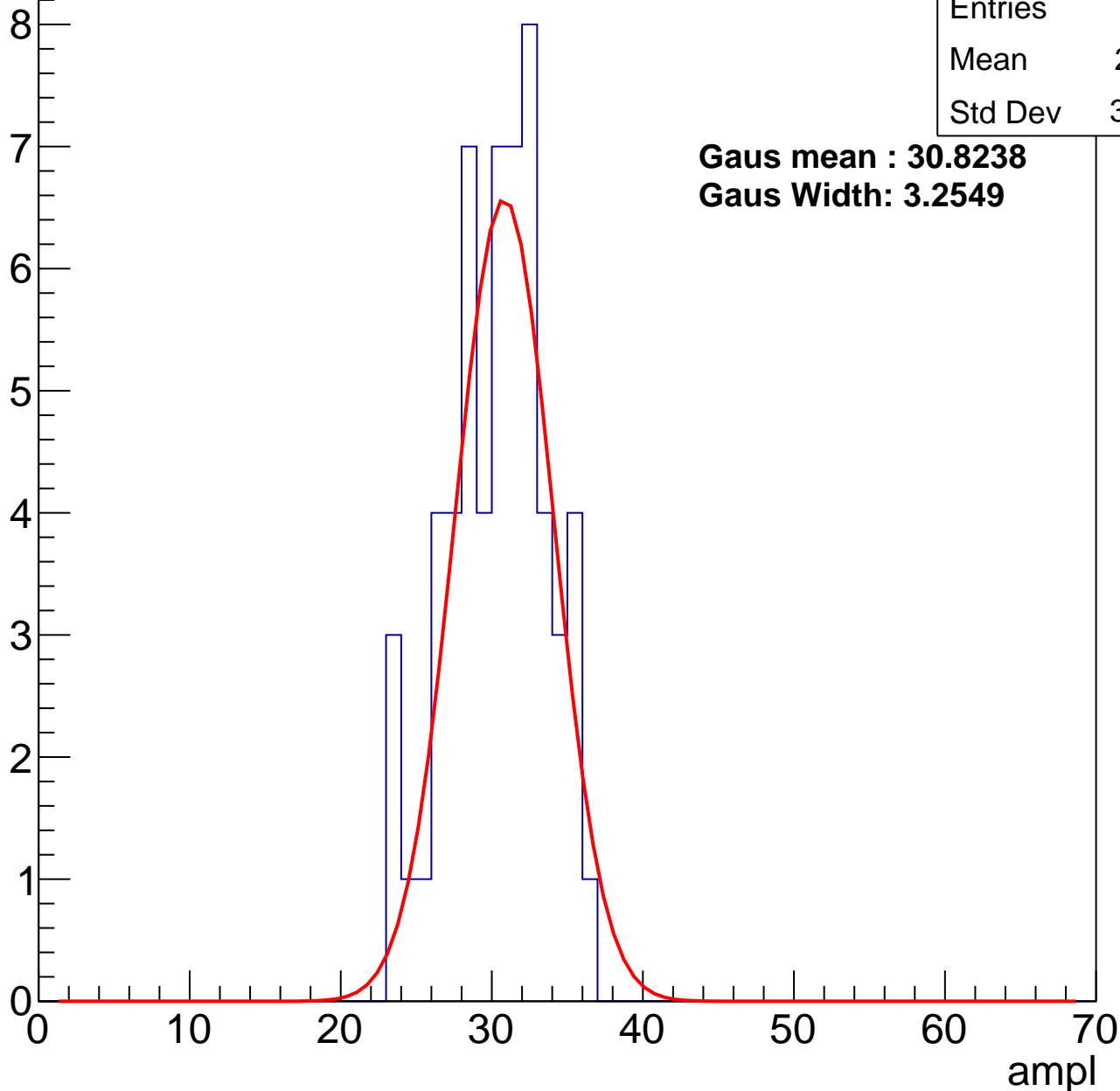
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	58
Mean	29.91
Std Dev	3.212

**Gaus mean : 30.8238**

**Gaus Width: 3.2549**



# B0L000S, U7-ch73, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	86
Mean	37.5
Std Dev	3.48

**Gaus mean : 38.0845**

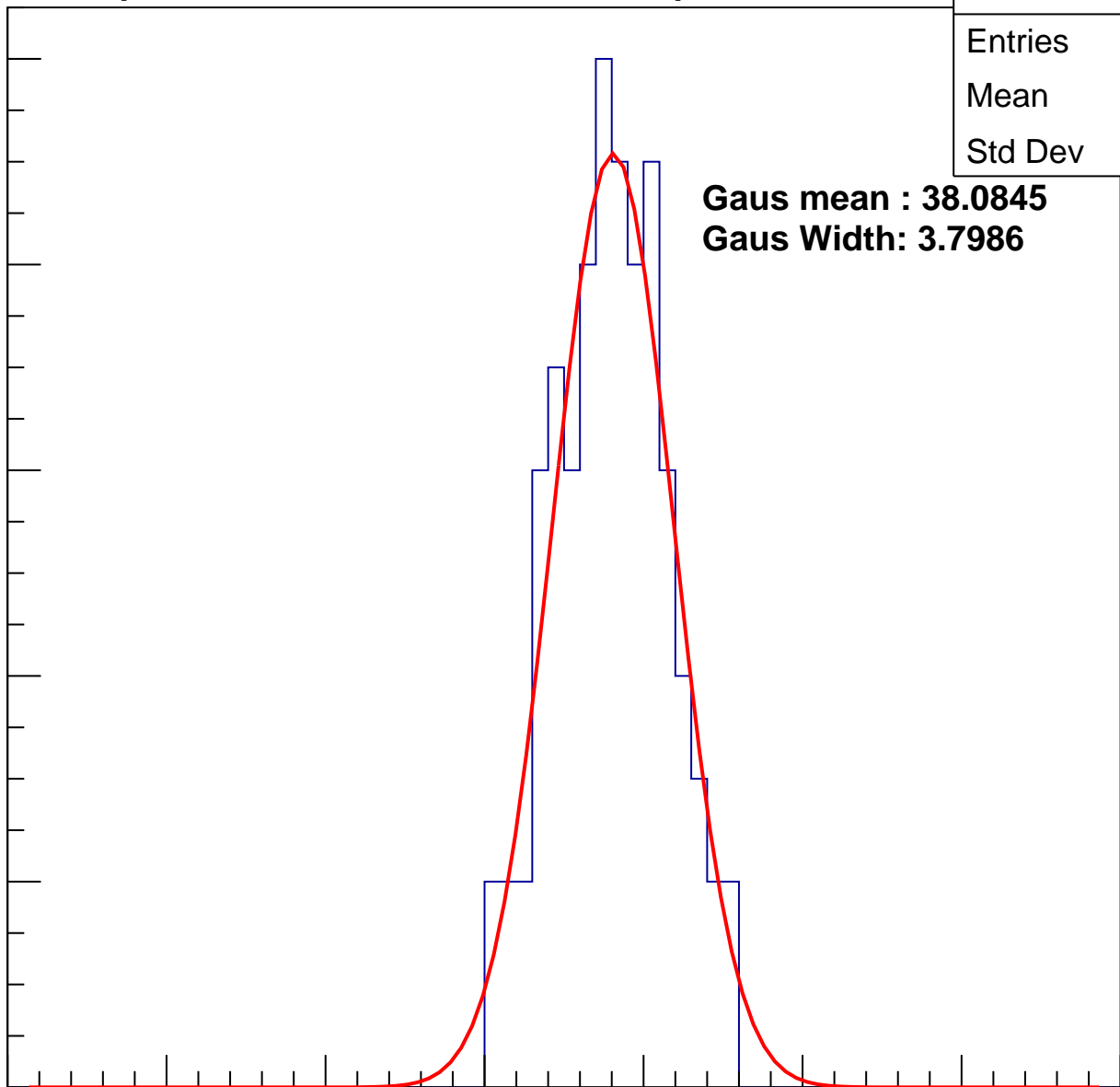
**Gaus Width: 3.7986**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L000S, U7-ch73, adc2

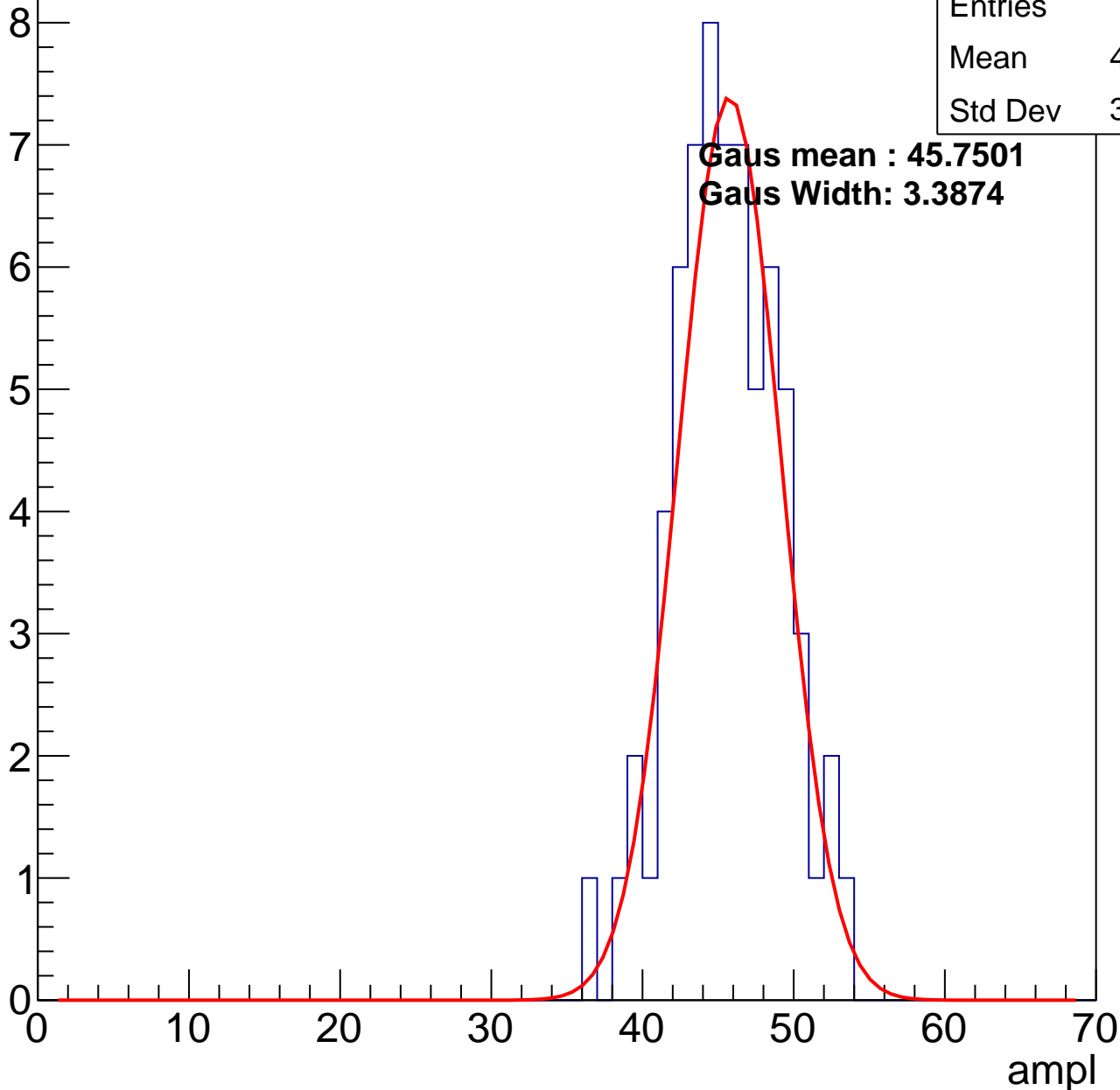
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	67
Mean	45.13
Std Dev	3.485

**Gaus mean : 45.7501**

**Gaus Width: 3.3874**

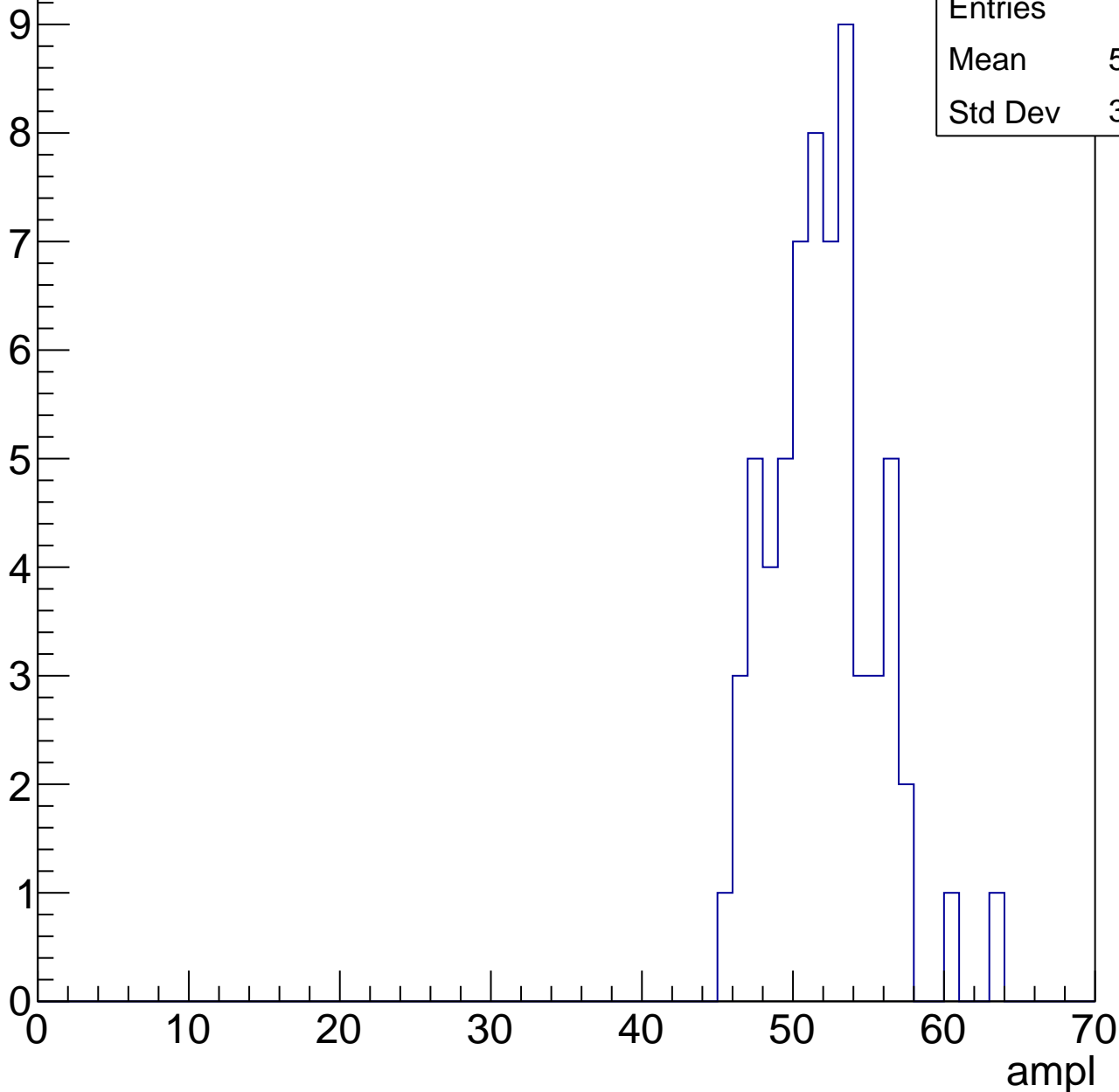


# B0L000S, U7-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	64
Mean	51.53
Std Dev	3.482

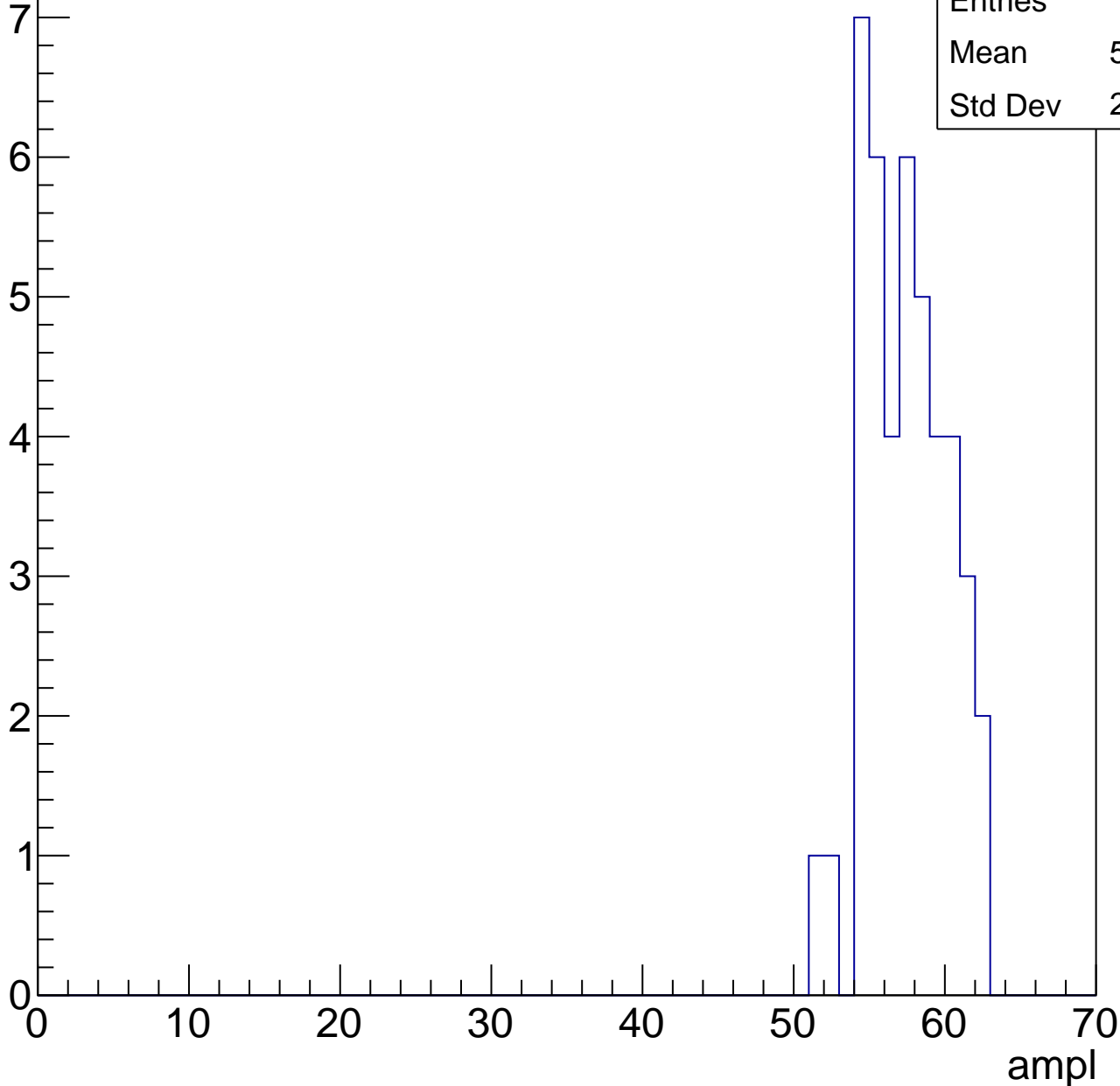


# B0L000S, U7-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	43
Mean	56.98
Std Dev	2.672



# B0L000S, U7-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	45
Mean	59.09
Std Dev	9.15

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

7

8

9

# B0L000S, U7-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L000S, U7-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L000S, U7-ch74, adc0

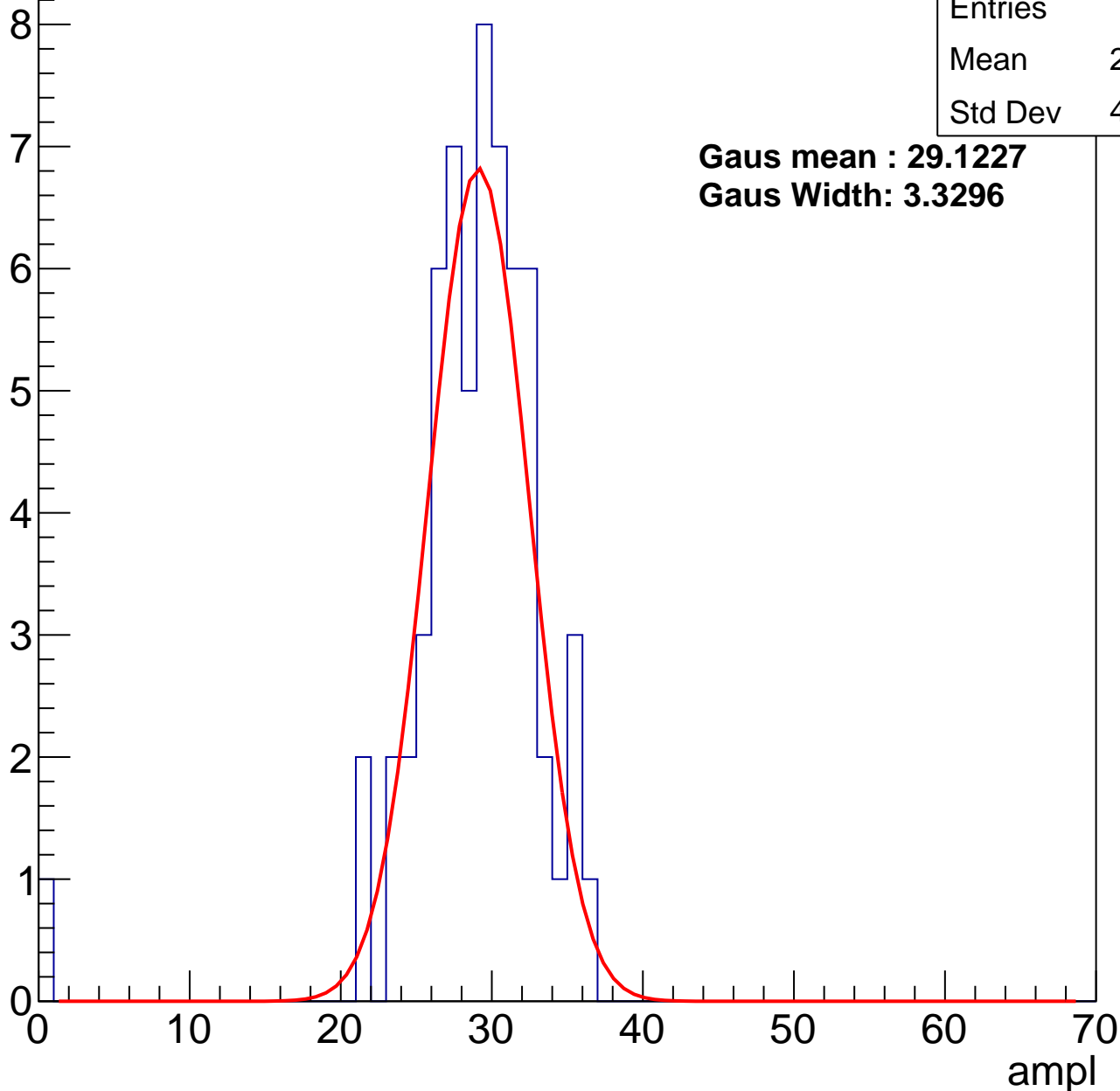
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	62
Mean	28.34
Std Dev	4.915

**Gaus mean : 29.1227**

**Gaus Width: 3.3296**



# B0L000S, U7-ch74, adc1

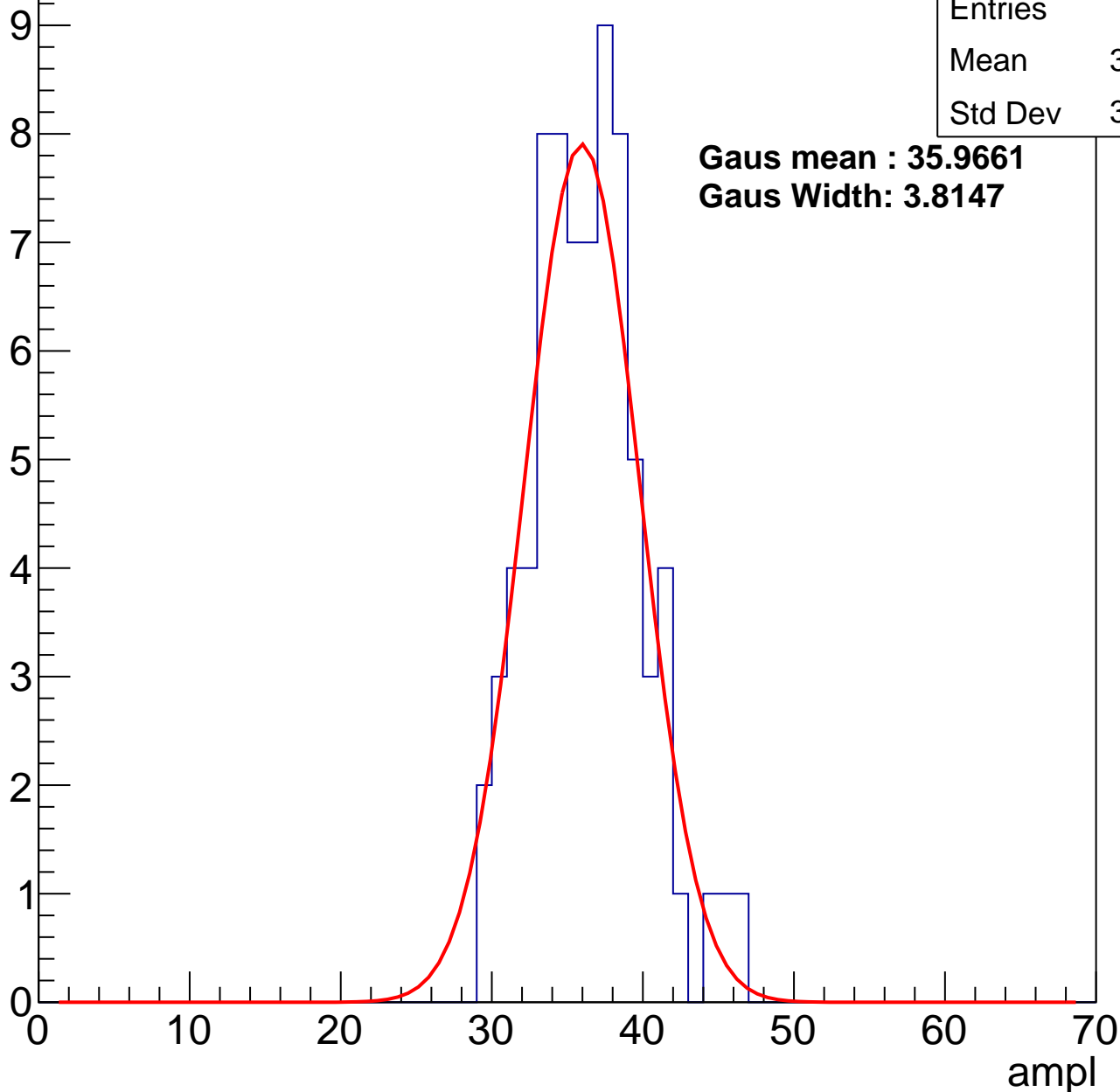
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	76
Mean	35.87
Std Dev	3.618

**Gaus mean : 35.9661**

**Gaus Width: 3.8147**



# B0L000S, U7-ch74, adc2

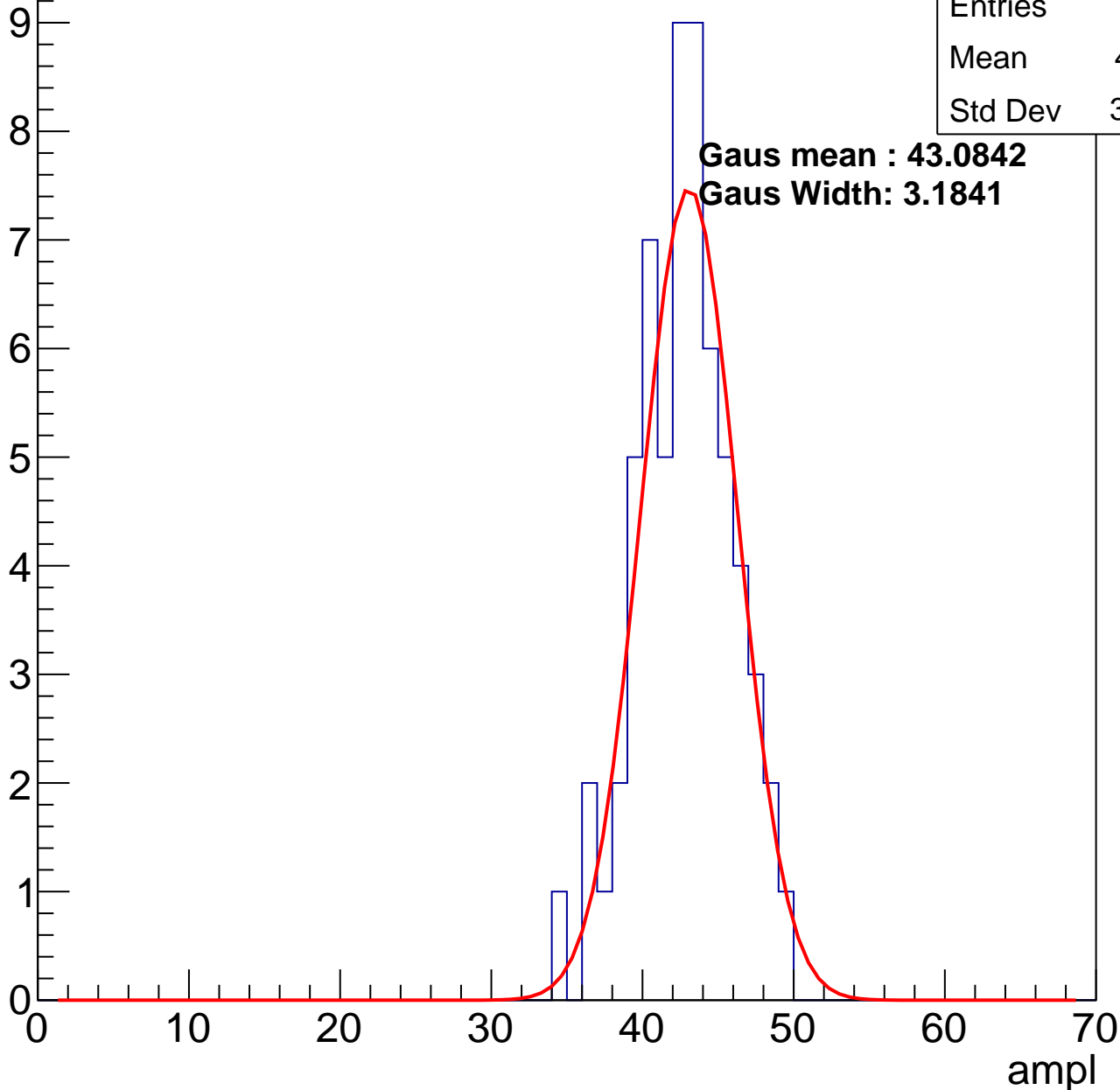
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	62
Mean	42.31
Std Dev	3.119

**Gaus mean : 43.0842**

**Gaus Width: 3.1841**

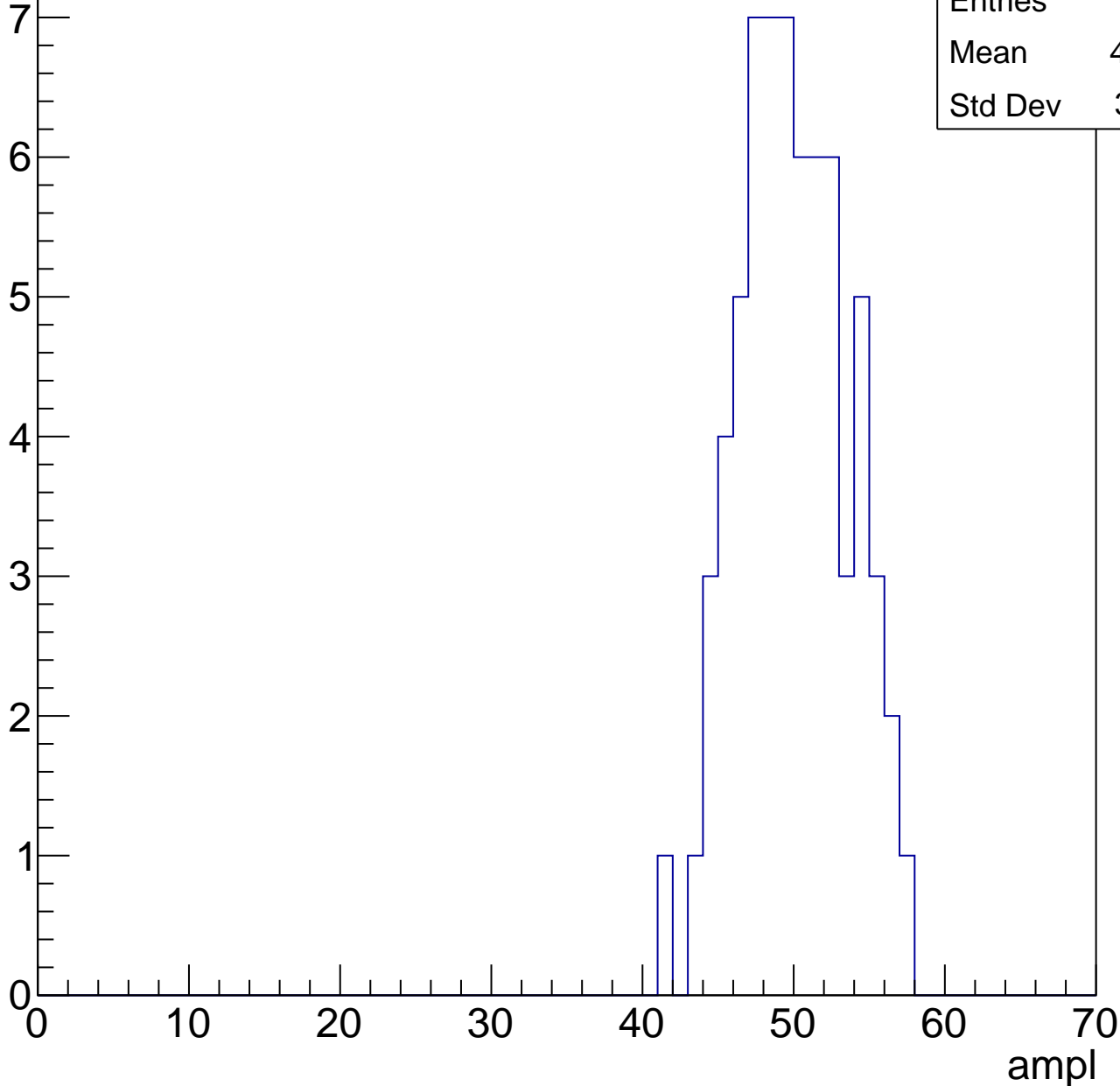


# B0L000S, U7-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	67
Mean	49.48
Std Dev	3.521



# B0L000S, U7-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

7

6

5

4

3

2

1

0

Entries 53

Mean 54.62

Std Dev 3.394

0

10

20

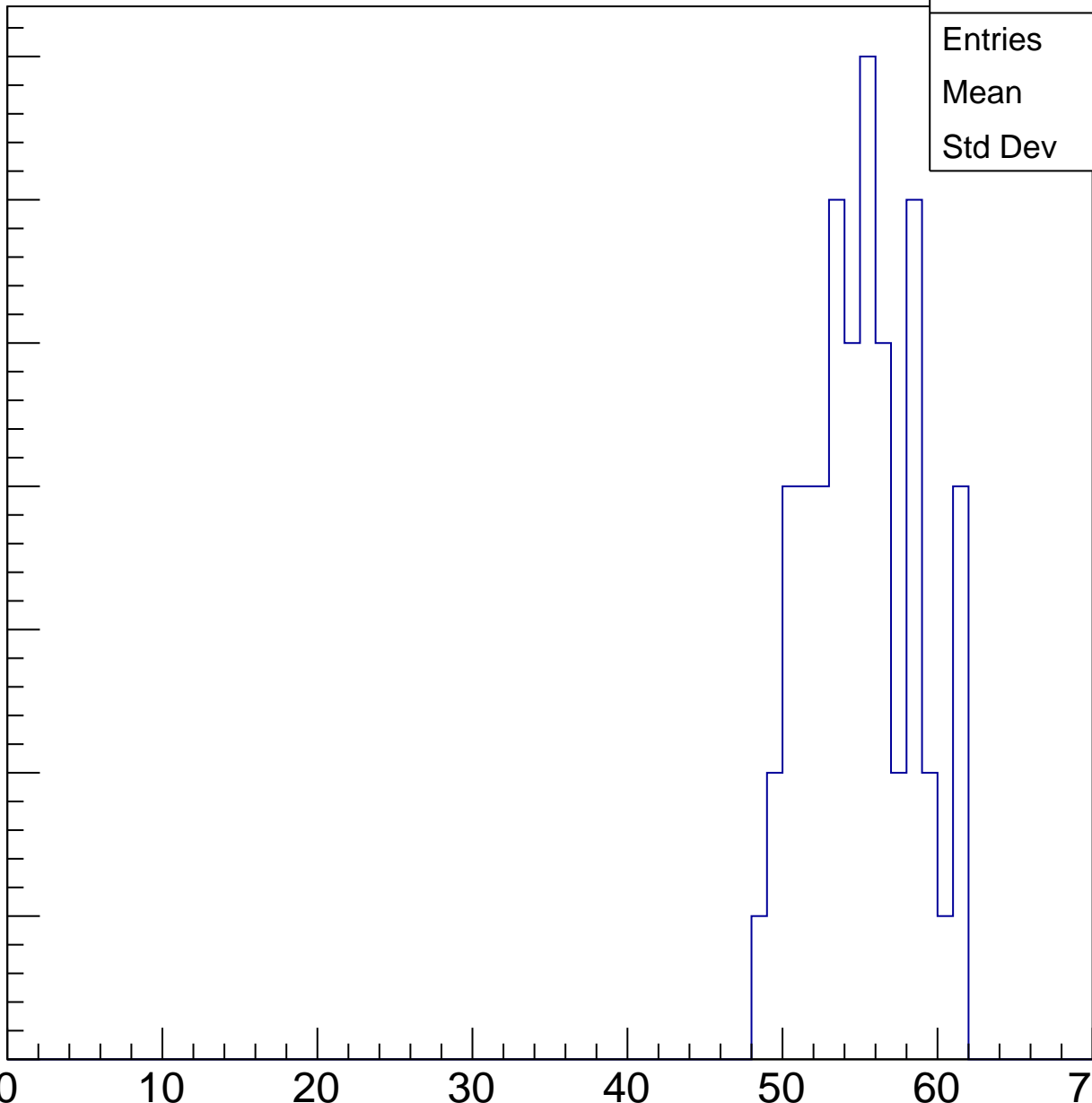
30

40

50

60

ampl



# B0L000S, U7-ch74, adc5

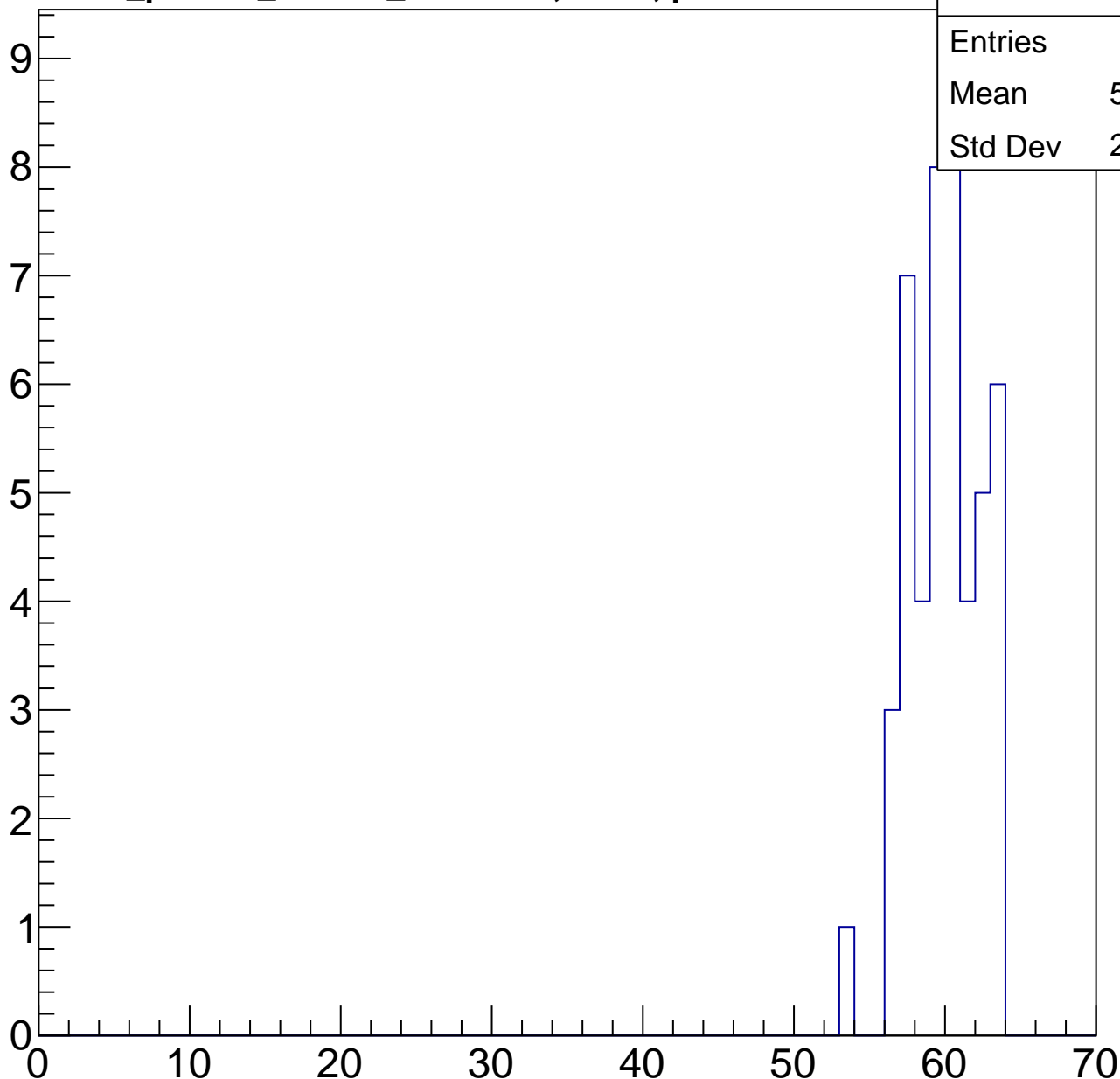
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	47
Mean	59.49
Std Dev	2.305

ampl

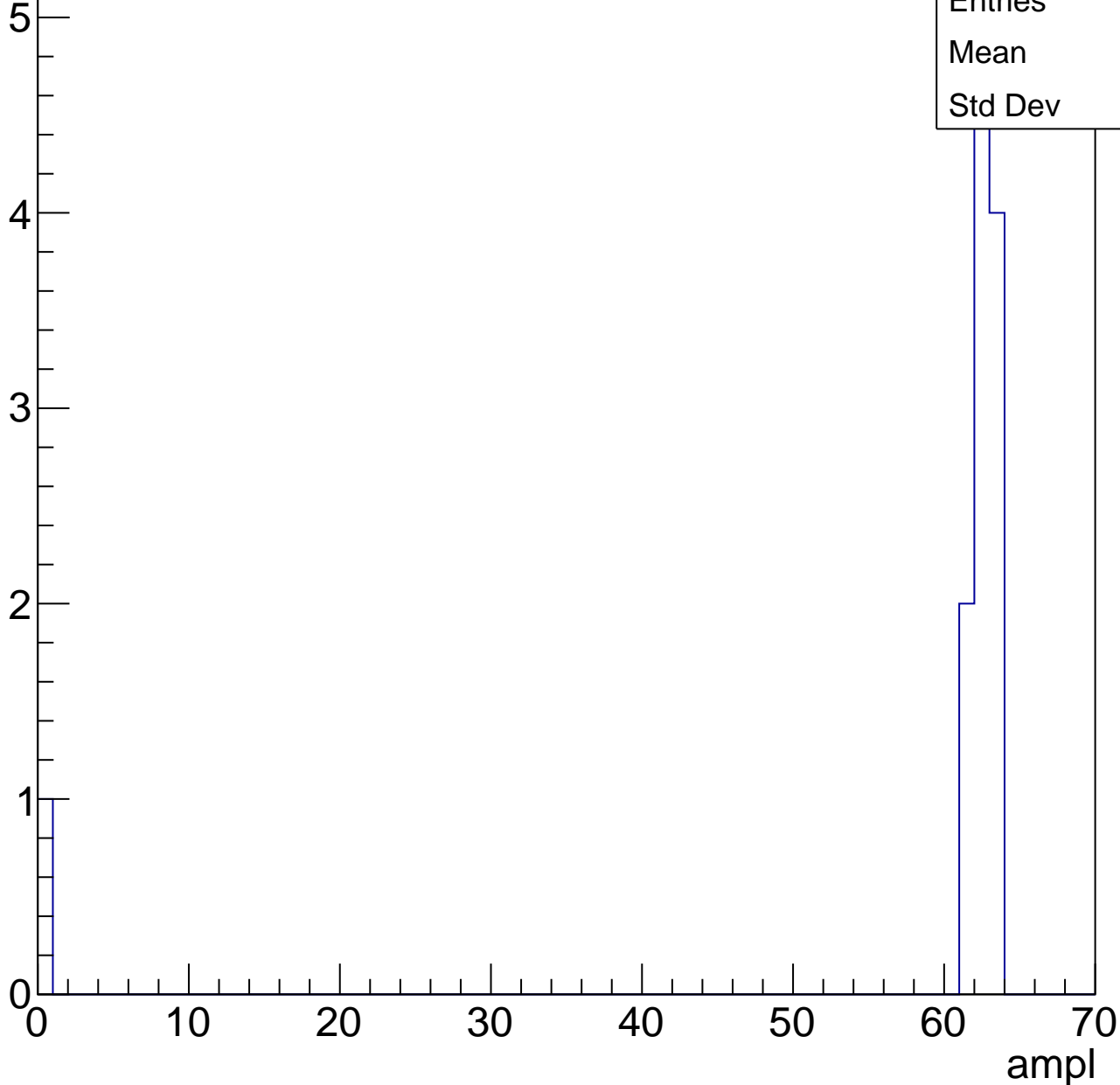


# B0L000S, U7-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	12
Mean	57
Std Dev	17.2





# B0L000S, U7-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L000S, U7-ch75, adc0

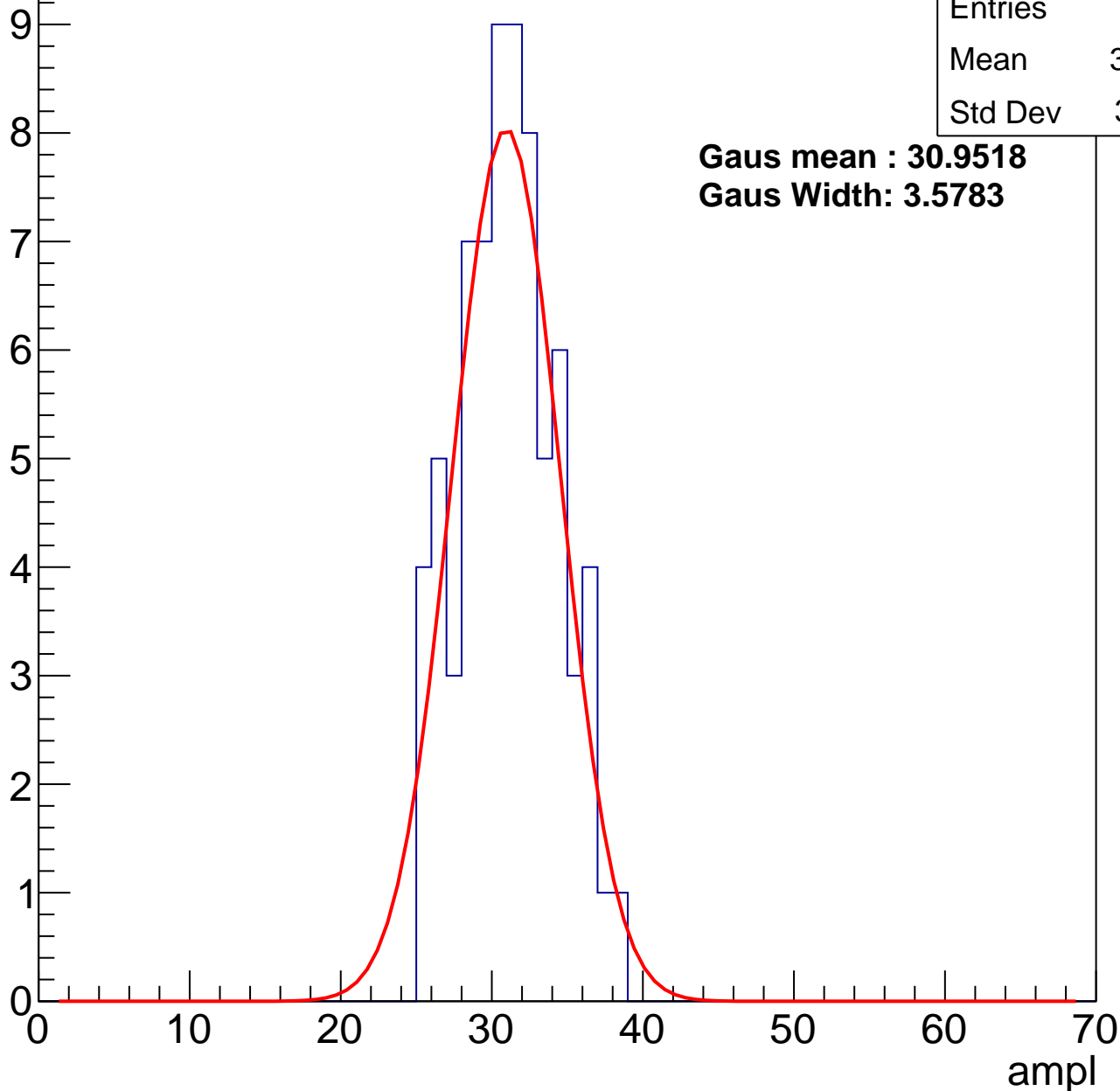
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	72
Mean	30.67
Std Dev	3.171

**Gaus mean : 30.9518**

**Gaus Width: 3.5783**



# B0L000S, U7-ch75, adc1

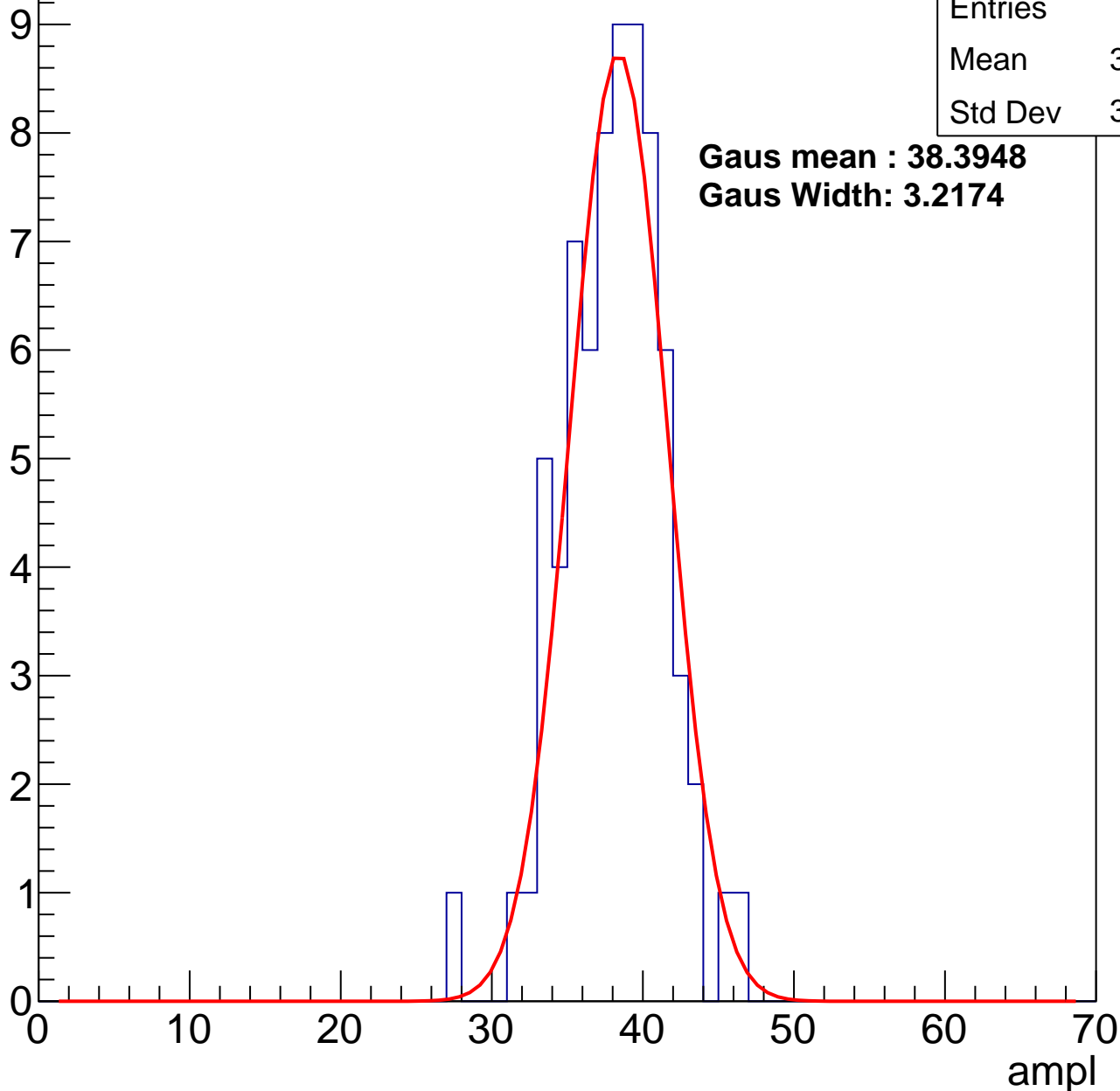
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	72
Mean	37.64
Std Dev	3.305

**Gaus mean : 38.3948**

**Gaus Width: 3.2174**



# B0L000S, U7-ch75, adc2

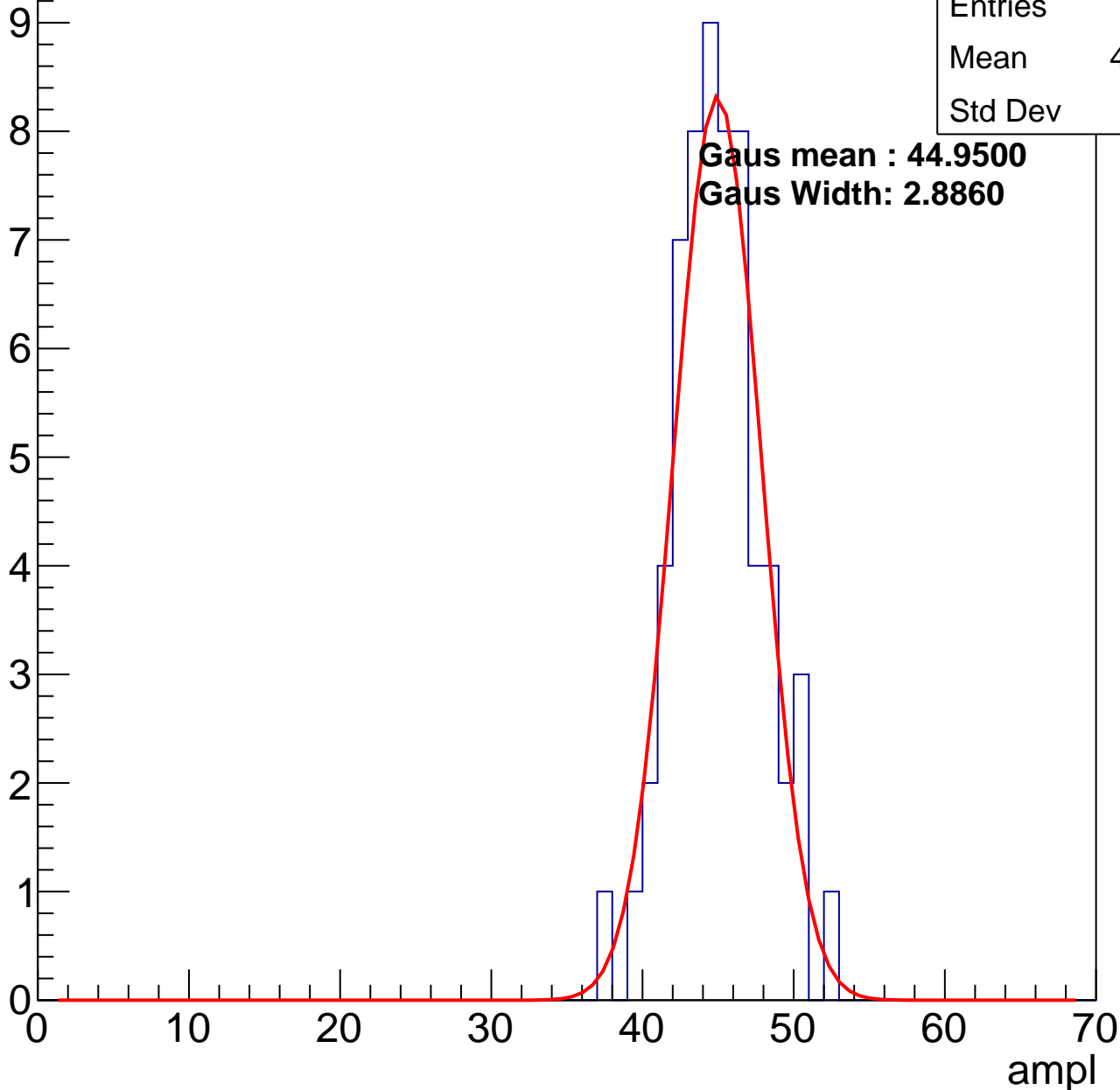
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	62
Mean	44.55
Std Dev	2.9

**Gaus mean : 44.9500**

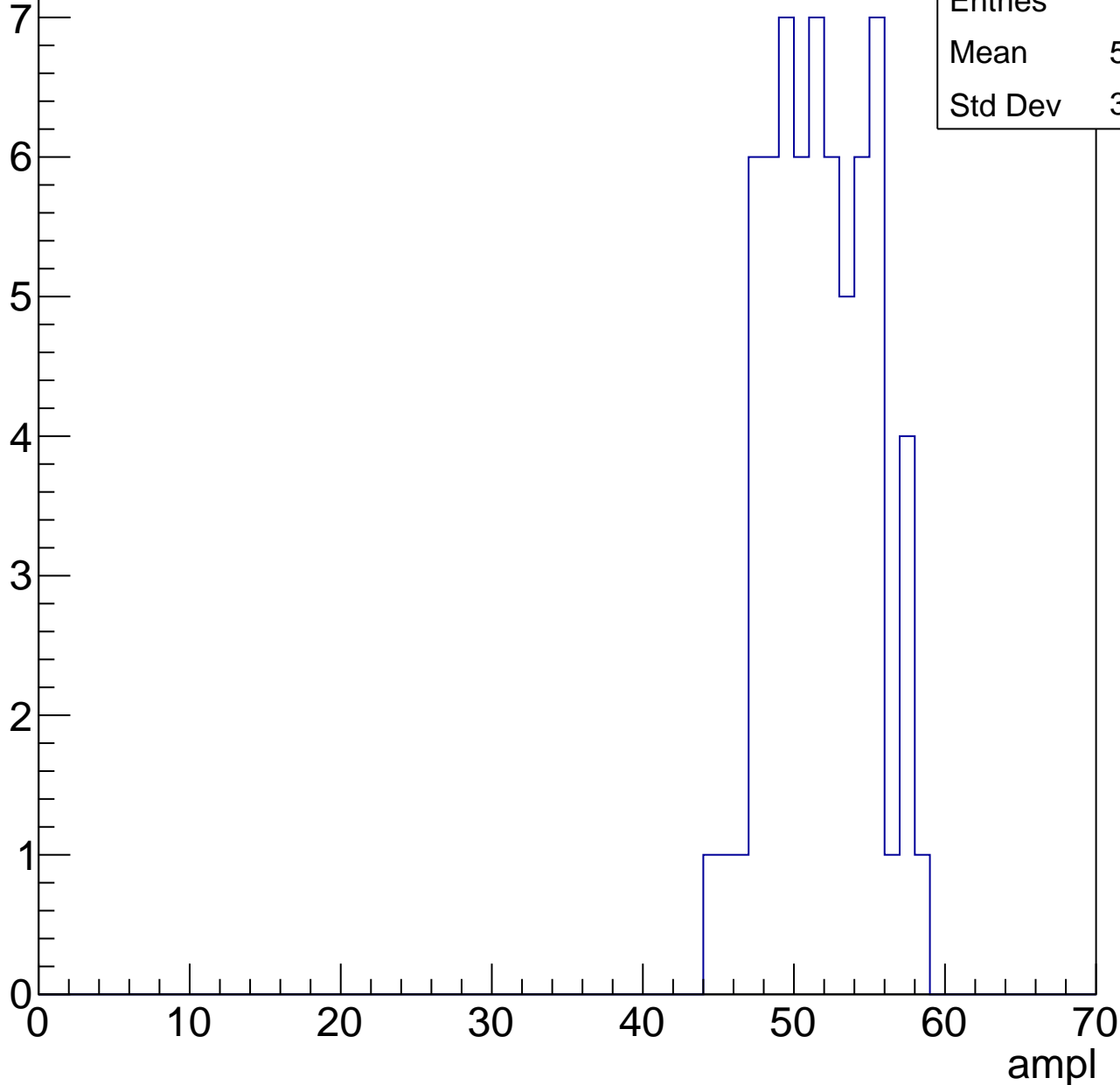
**Gaus Width: 2.8860**



# B0L000S, U7-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

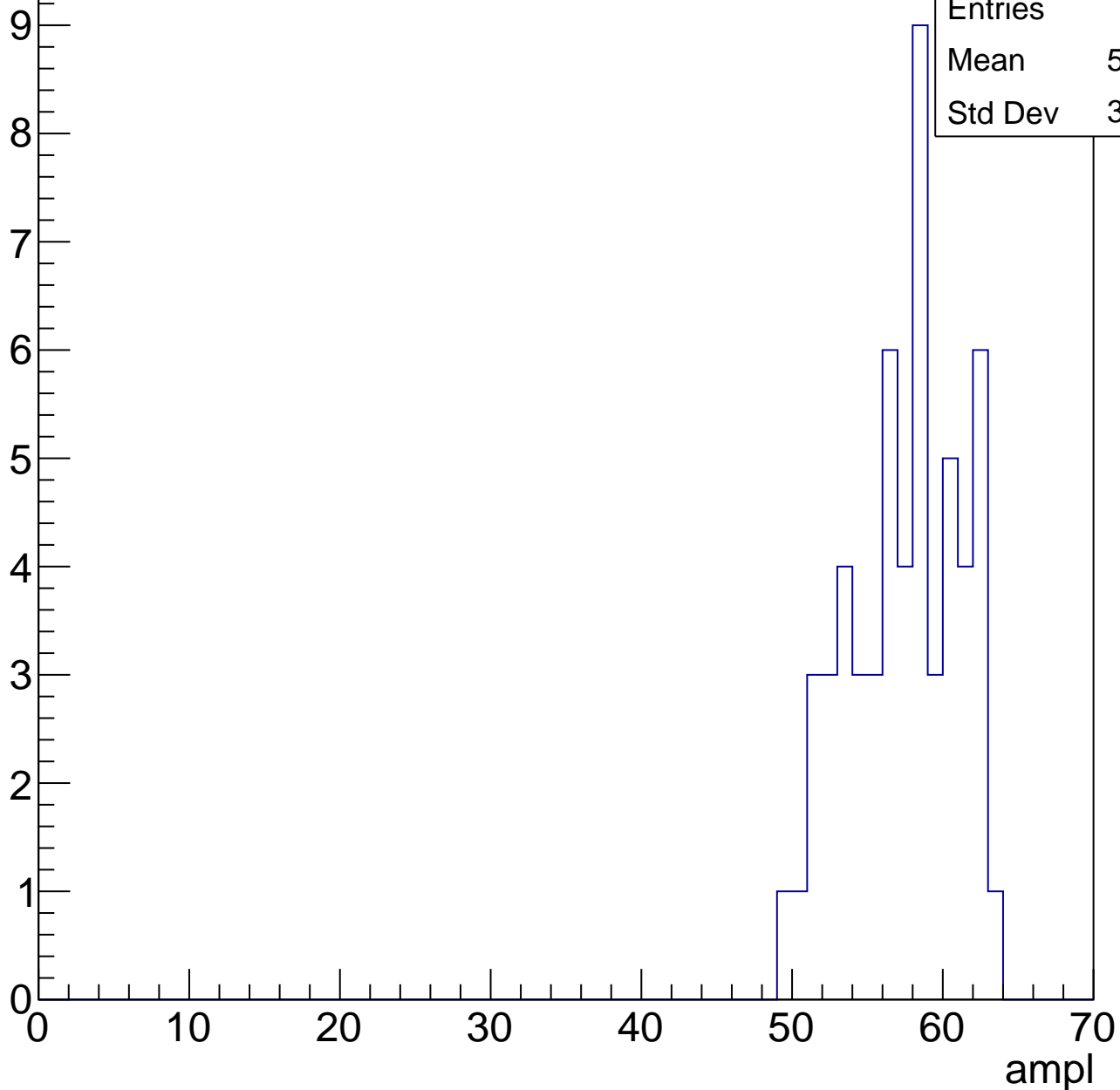


Entries	65
Mean	51.28
Std Dev	3.279

# B0L000S, U7-ch75, adc4

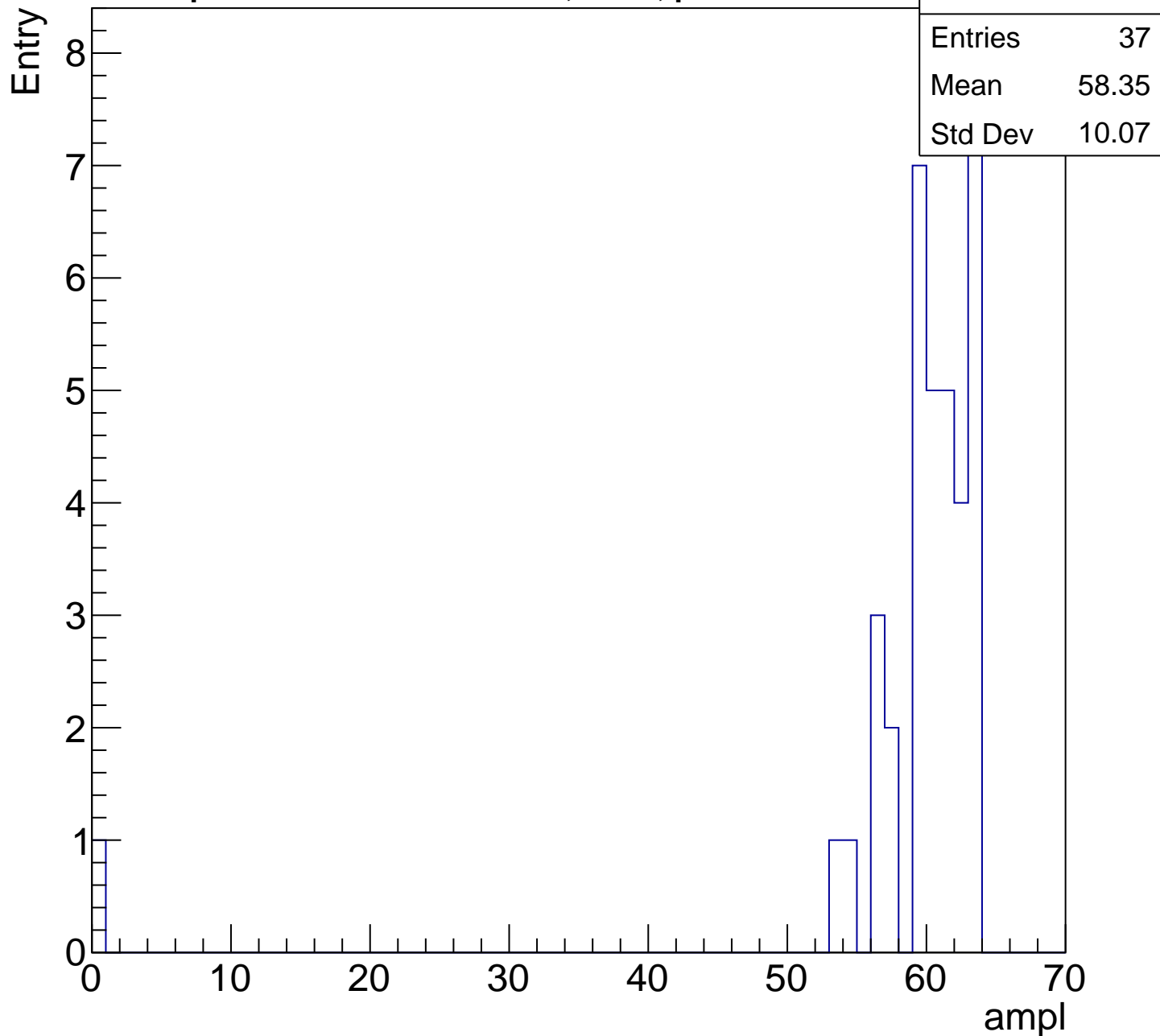
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1



# B0L000S, U7-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch76, adc0

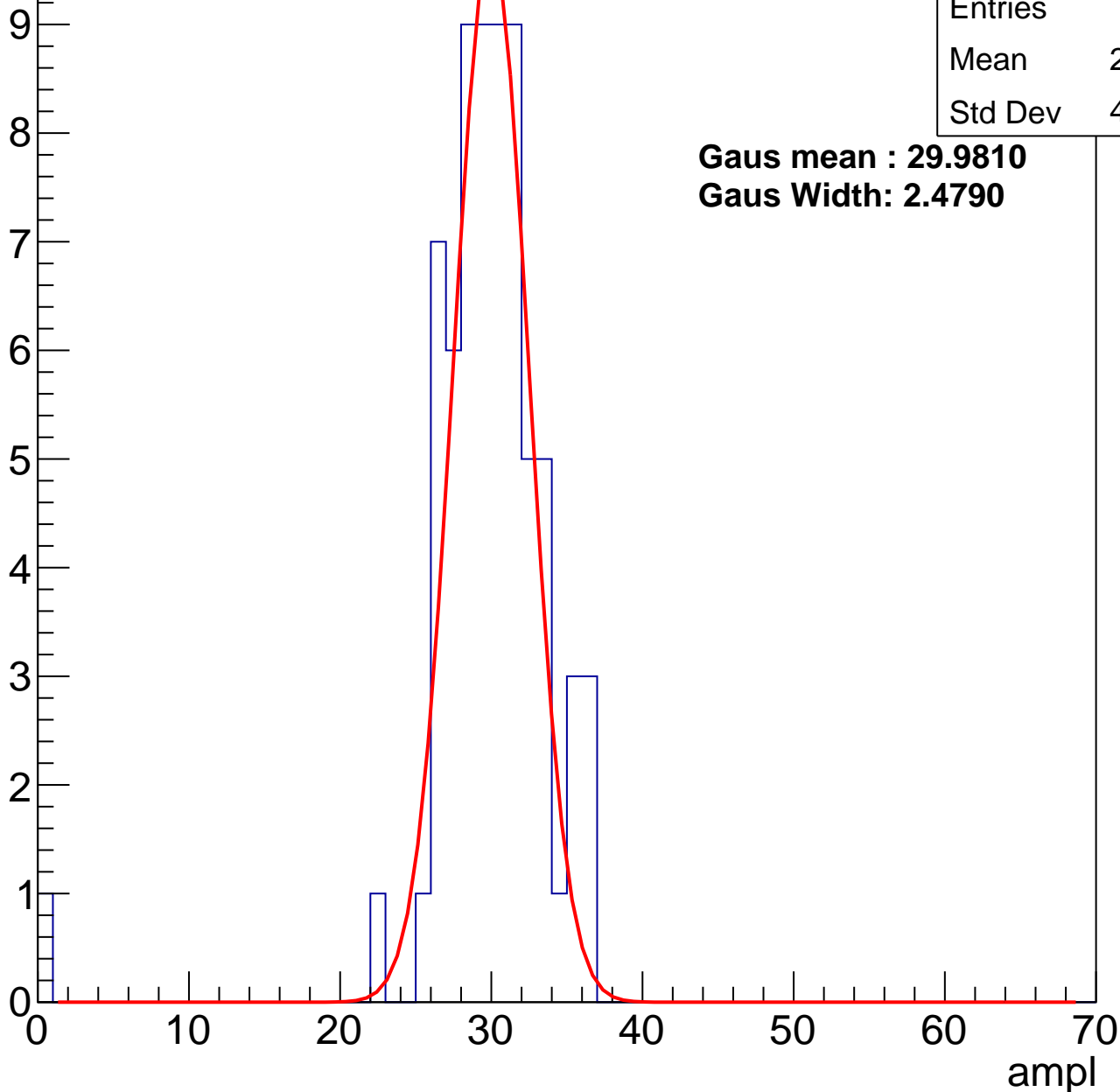
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	69
Mean	29.35
Std Dev	4.574

**Gaus mean : 29.9810**

**Gaus Width: 2.4790**

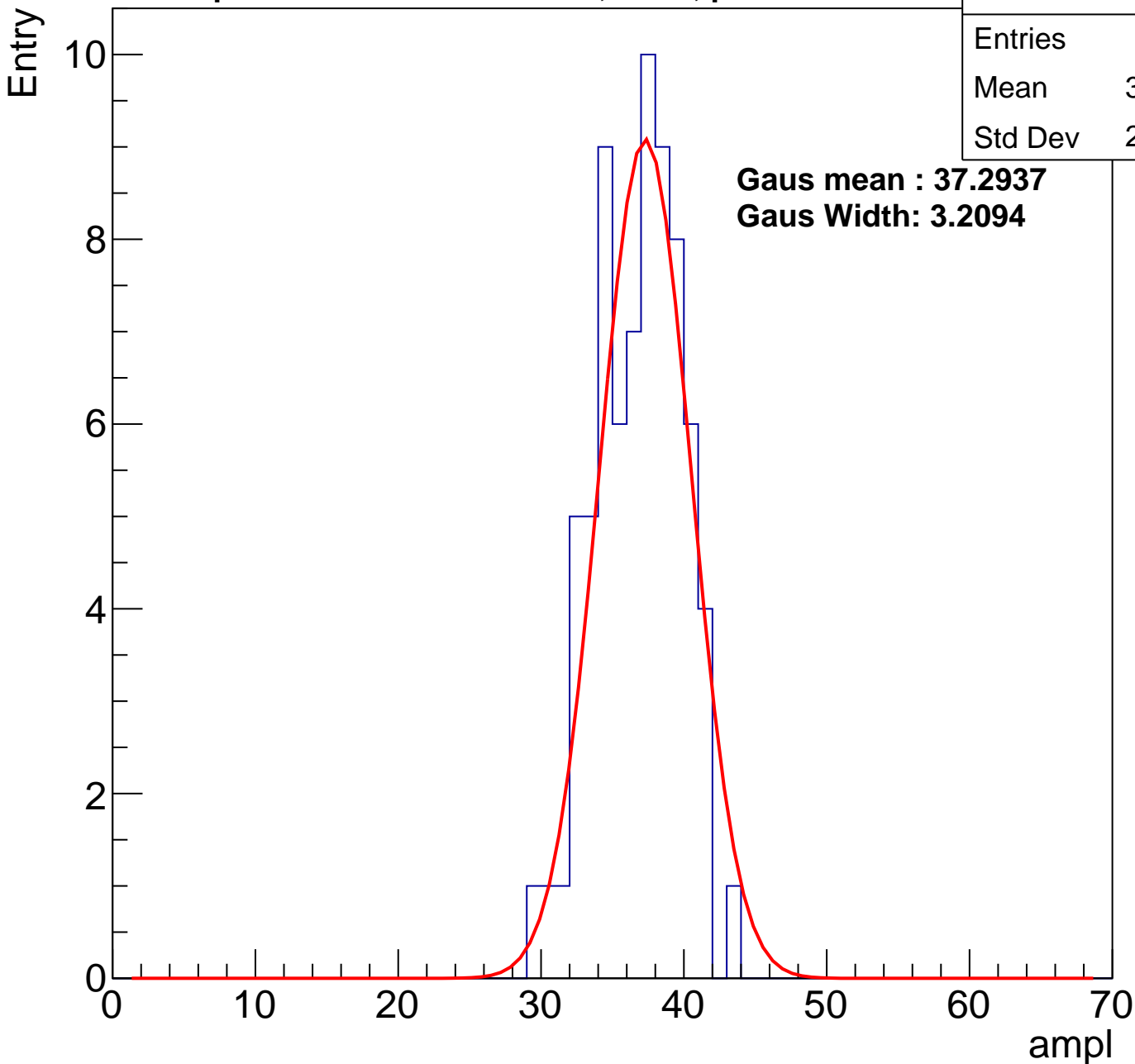


# B0L000S, U7-ch76, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	73
Mean	36.36
Std Dev	2.939

**Gaus mean : 37.2937**  
**Gaus Width: 3.2094**



# B0L000S, U7-ch76, adc2

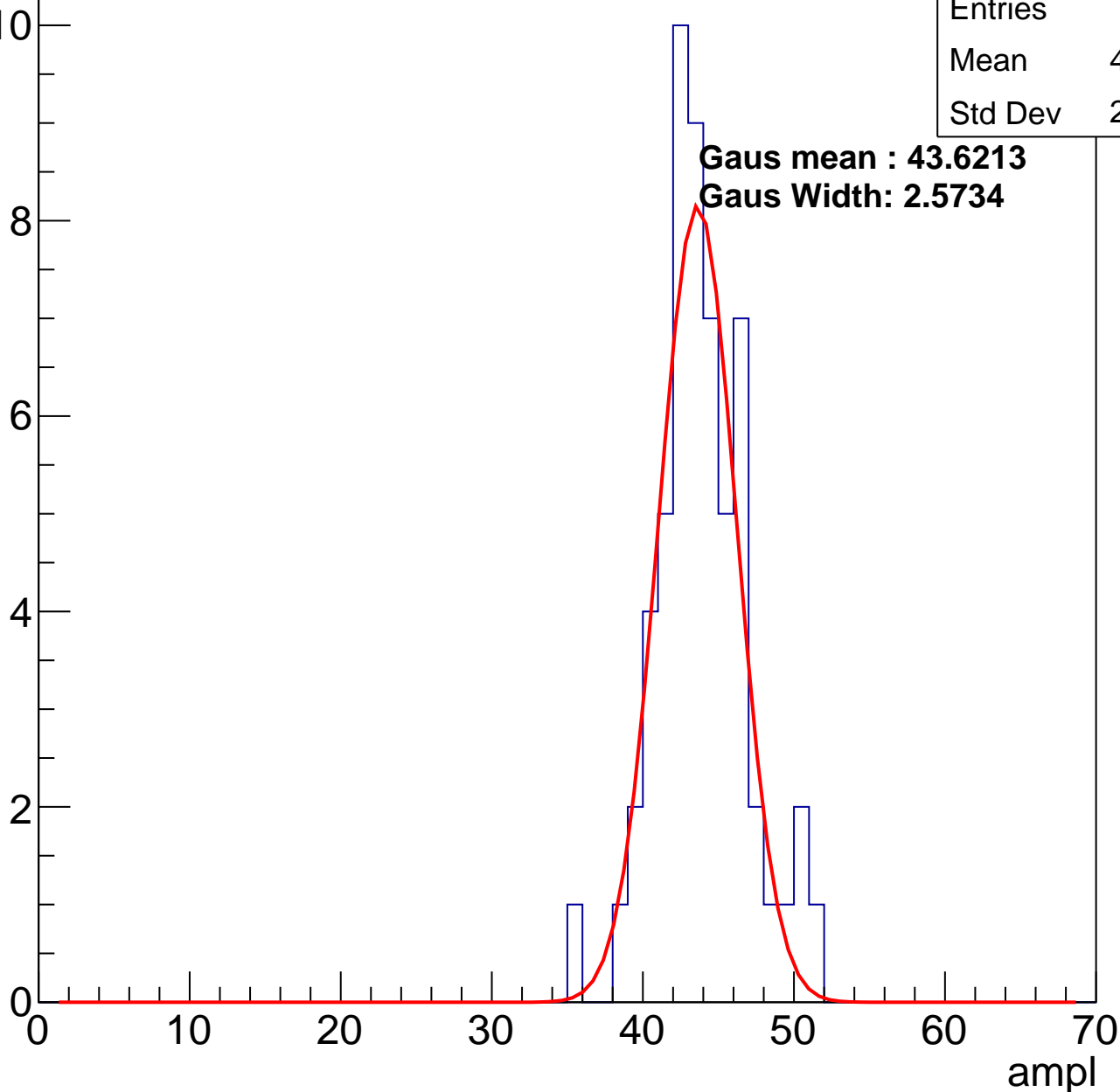
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	58
Mean	43.45
Std Dev	2.995

**Gaus mean : 43.6213**

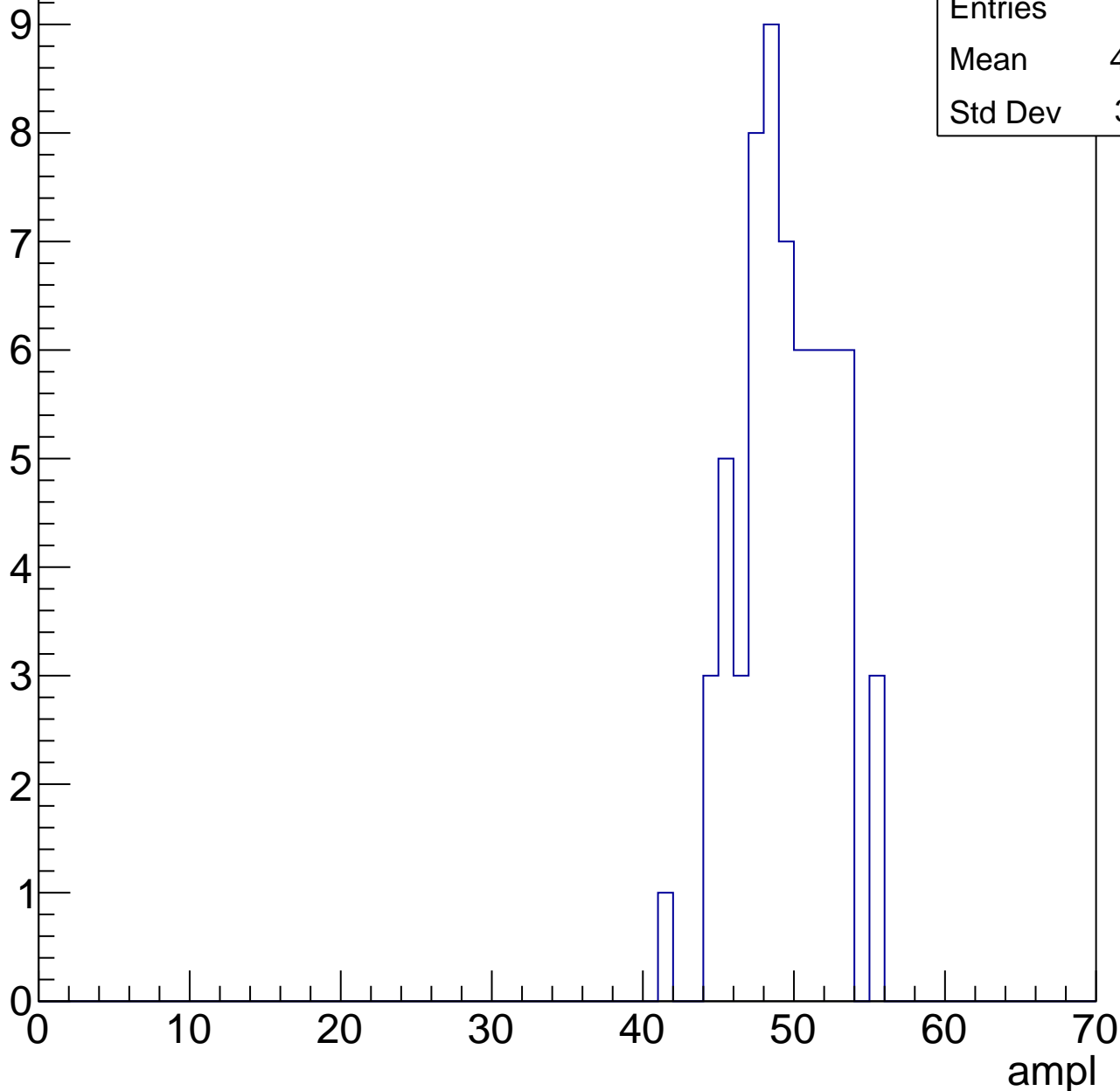
**Gaus Width: 2.5734**



# B0L000S, U7-ch76, adc3

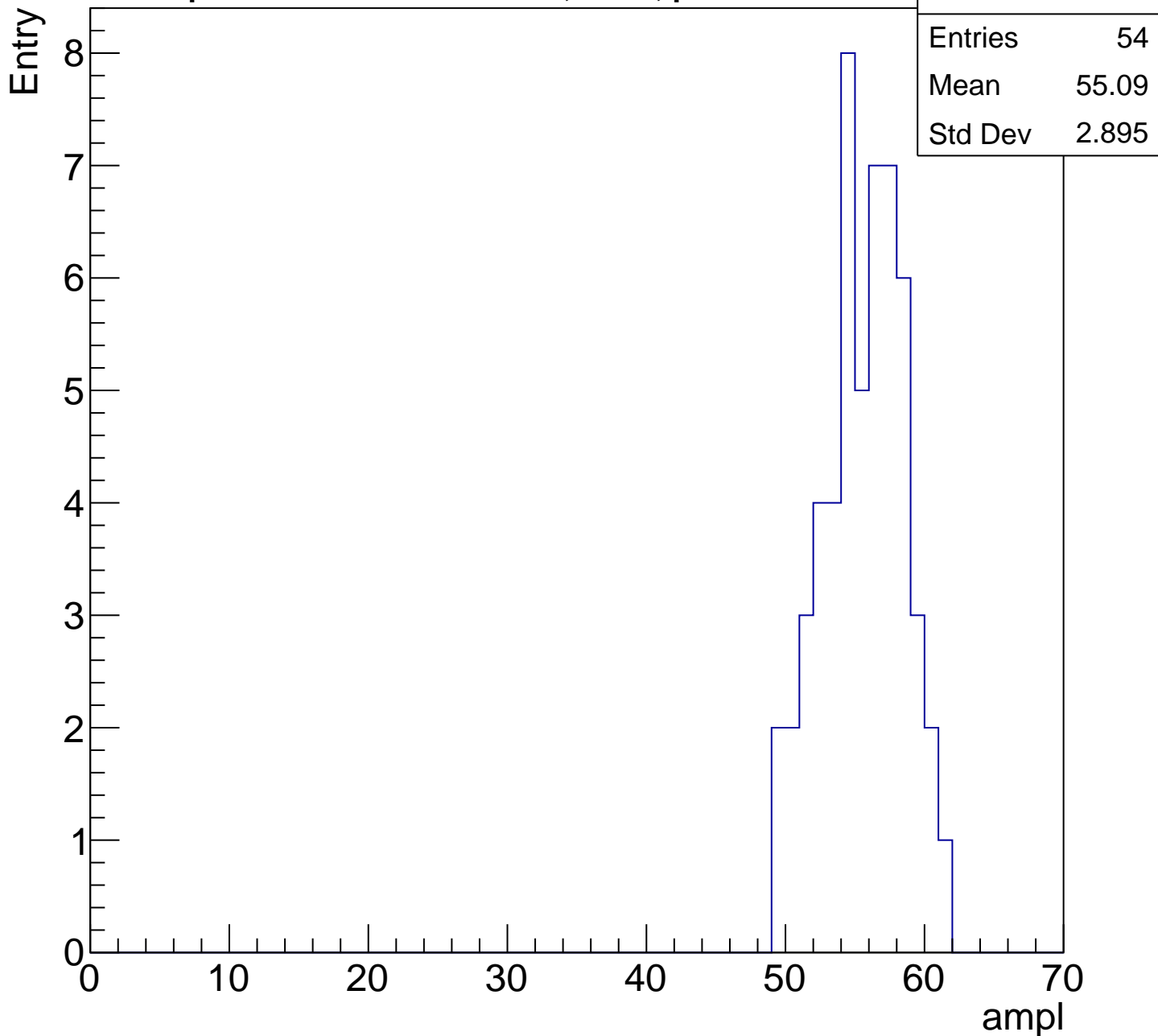
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1



# B0L000S, U7-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

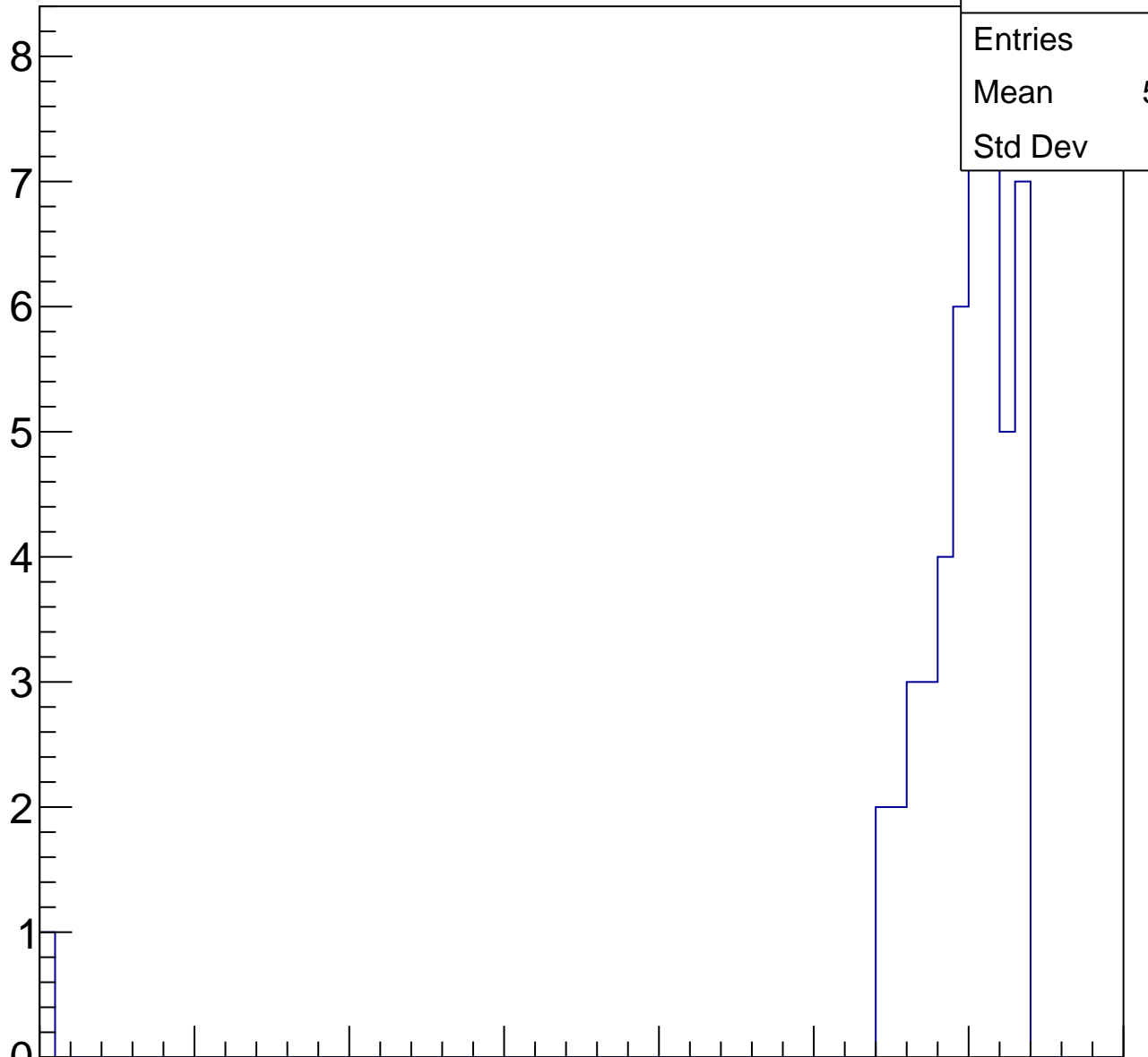
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	58.41
Std Dev	8.79

ampl

0 10 20 30 40 50 60 70

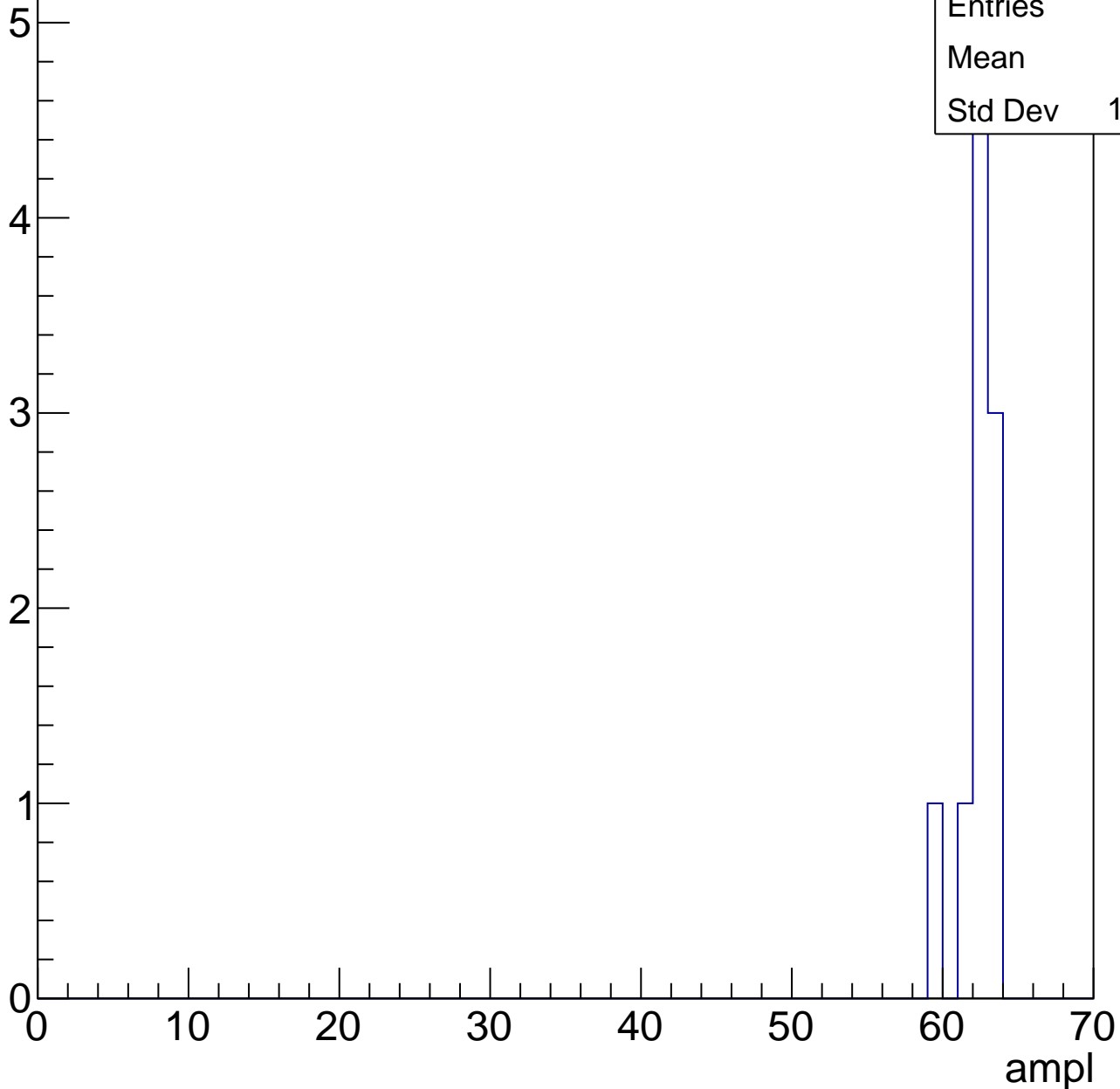


# B0L000S, U7-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	10
Mean	61.9
Std Dev	1.136





# B0L000S, U7-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L000S, U7-ch77, adc0

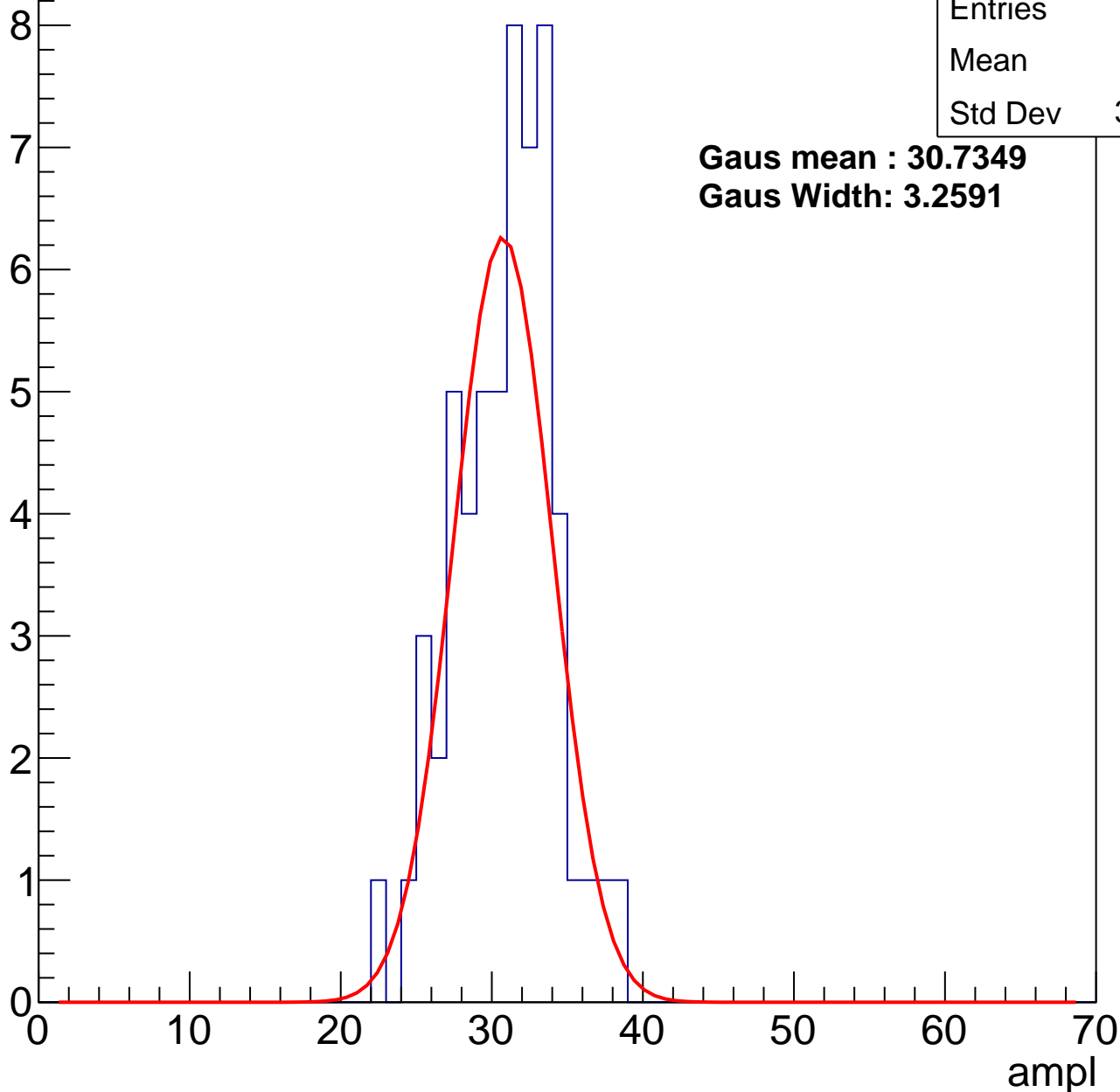
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	57
Mean	30.4
Std Dev	3.271

**Gaus mean : 30.7349**

**Gaus Width: 3.2591**



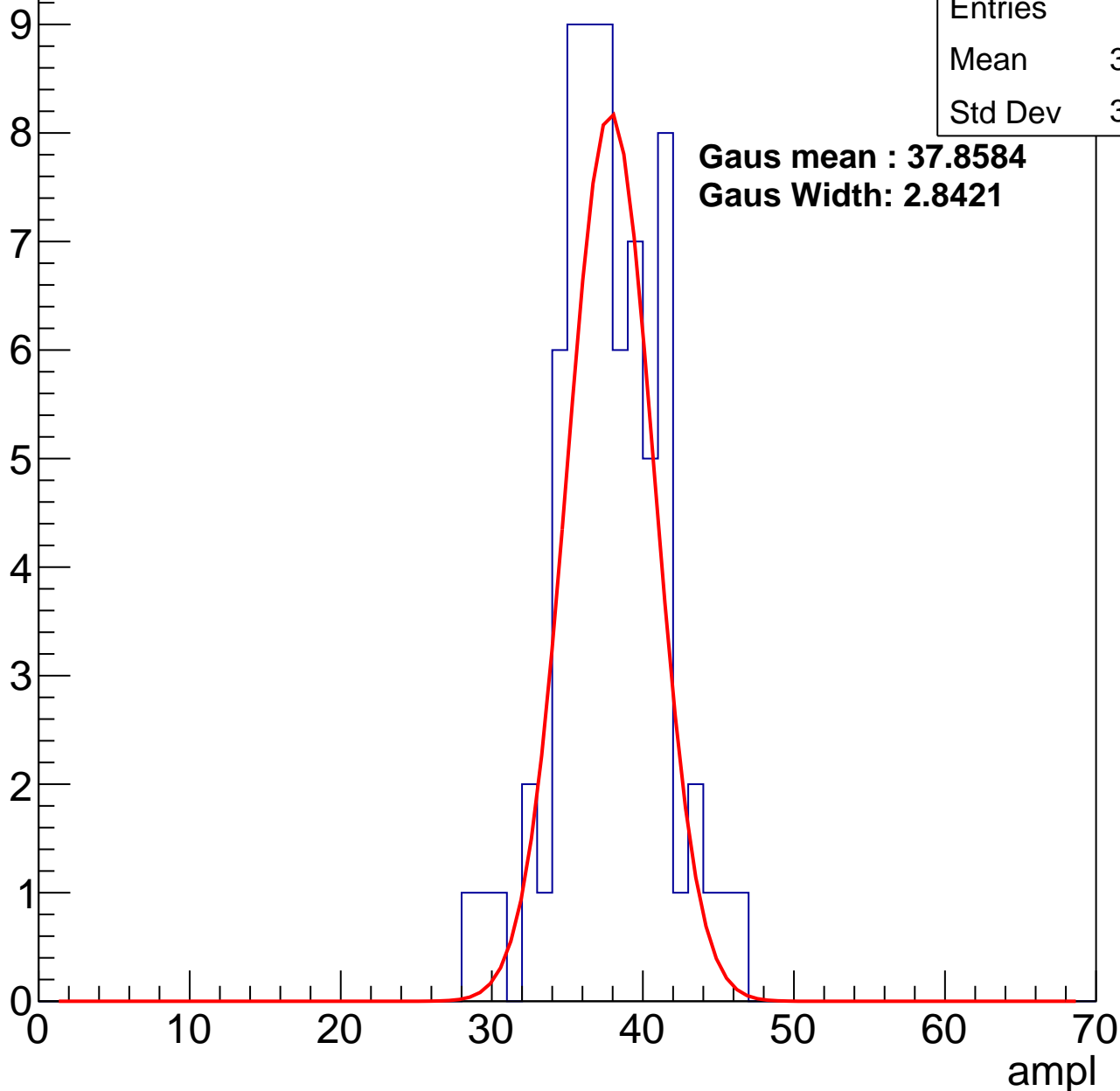
# B0L000S, U7-ch77, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	71
Mean	37.35
Std Dev	3.456

**Gaus mean : 37.8584**  
**Gaus Width: 2.8421**



# B0L000S, U7-ch77, adc2

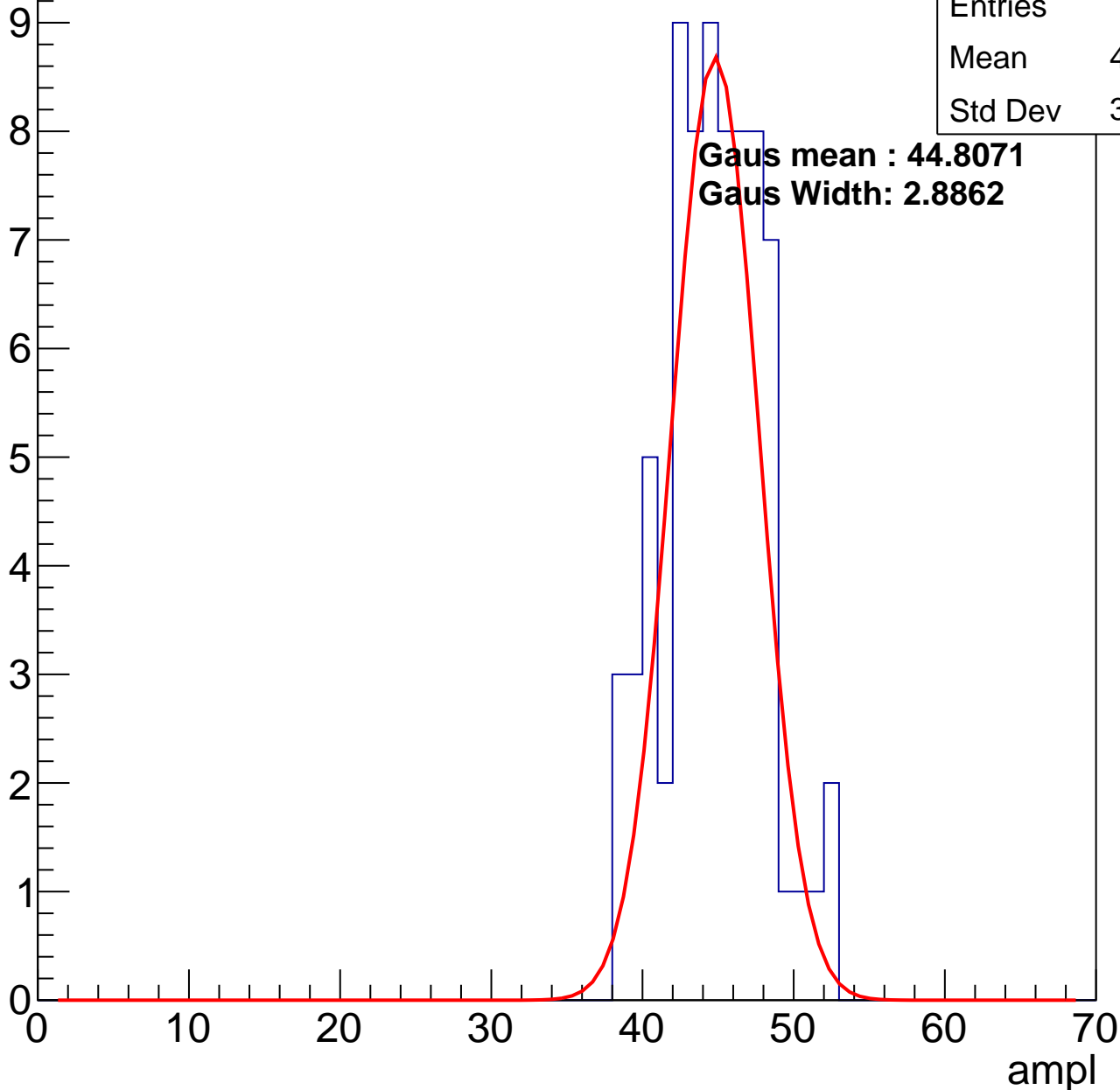
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	75
Mean	44.33
Std Dev	3.222

**Gaus mean : 44.8071**

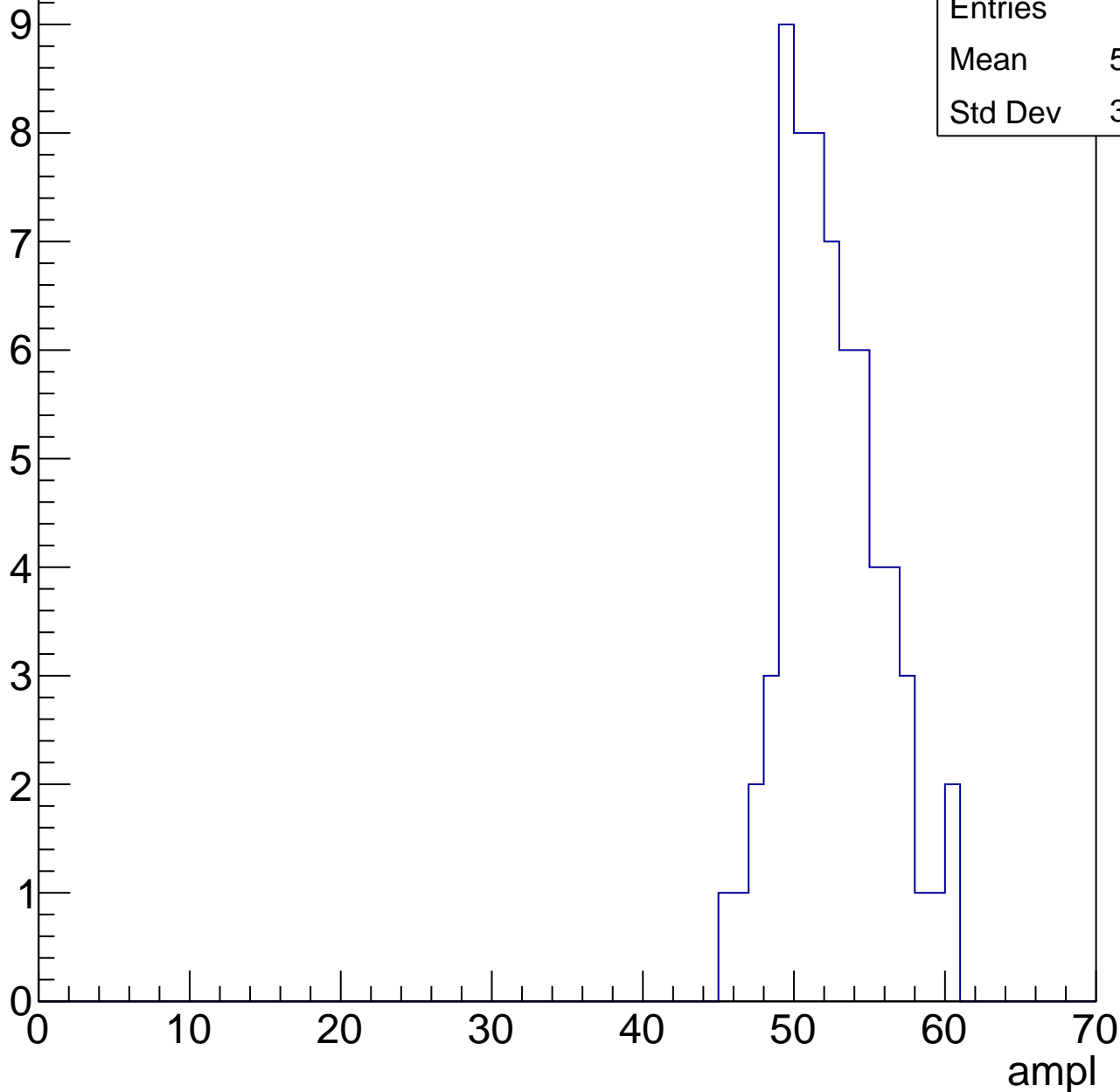
**Gaus Width: 2.8862**



# B0L000S, U7-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

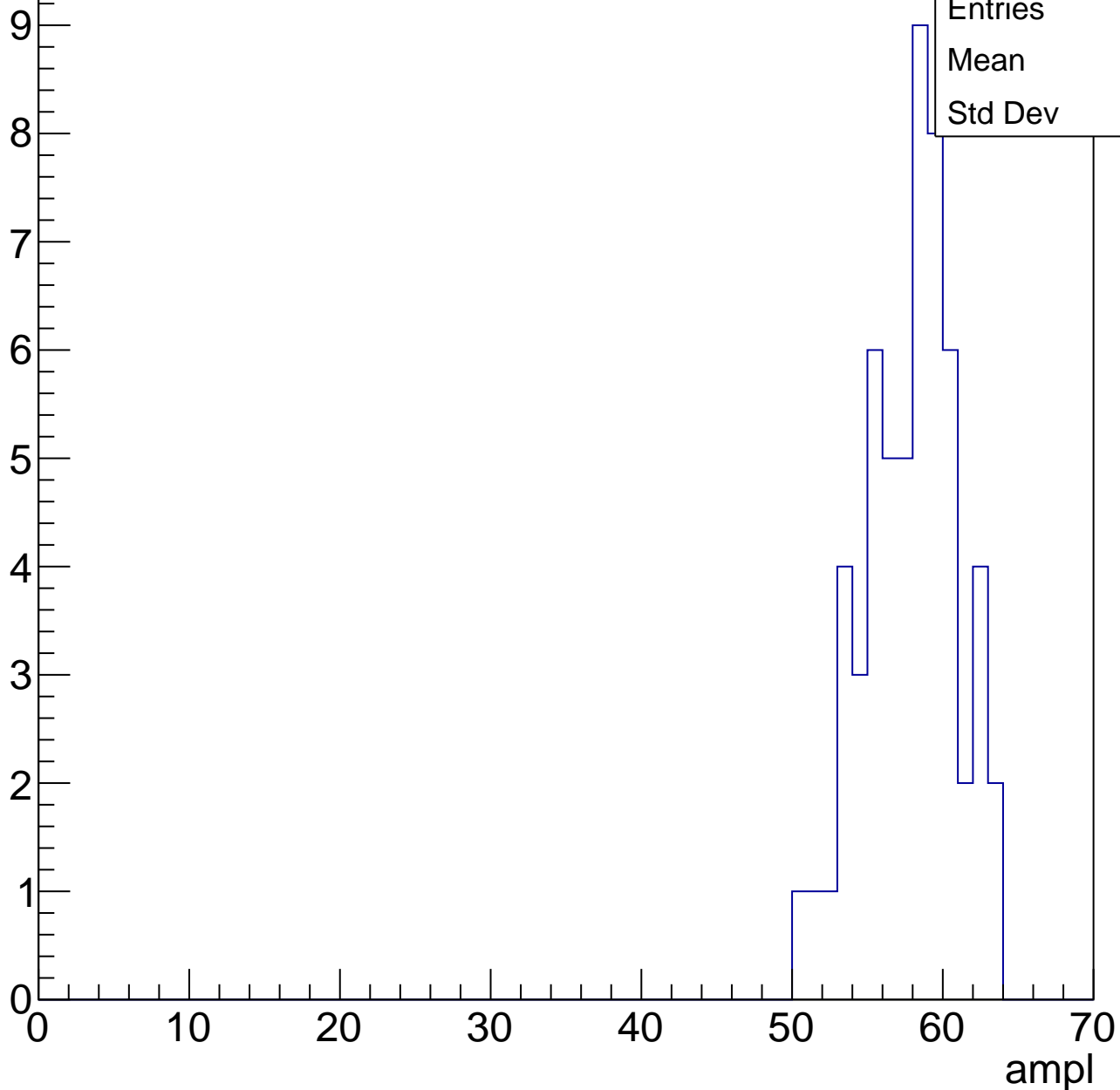
Entry



# B0L000S, U7-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

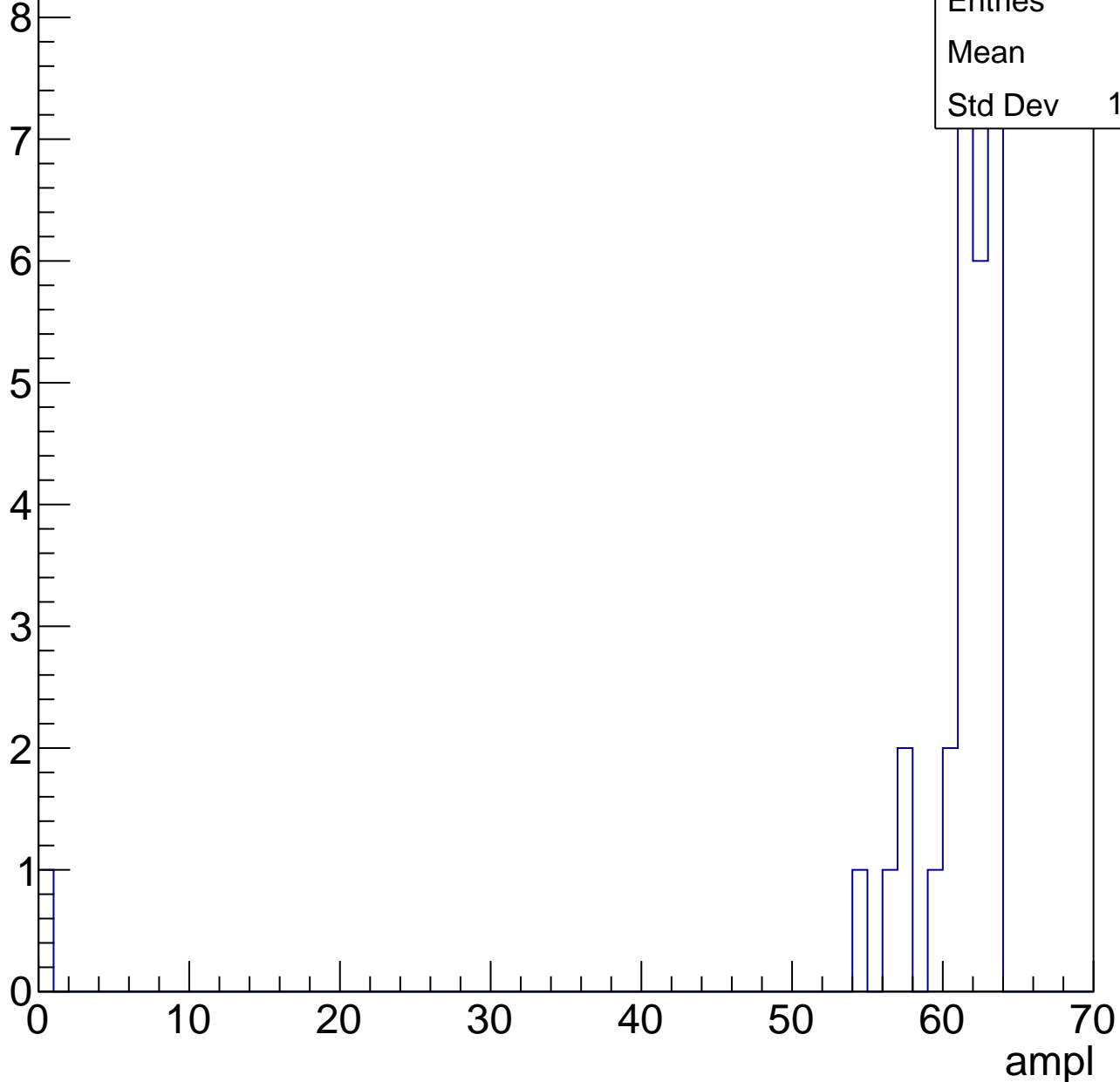
Entry



# B0L000S, U7-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L000S, U7-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L000S, U7-ch78, adc0

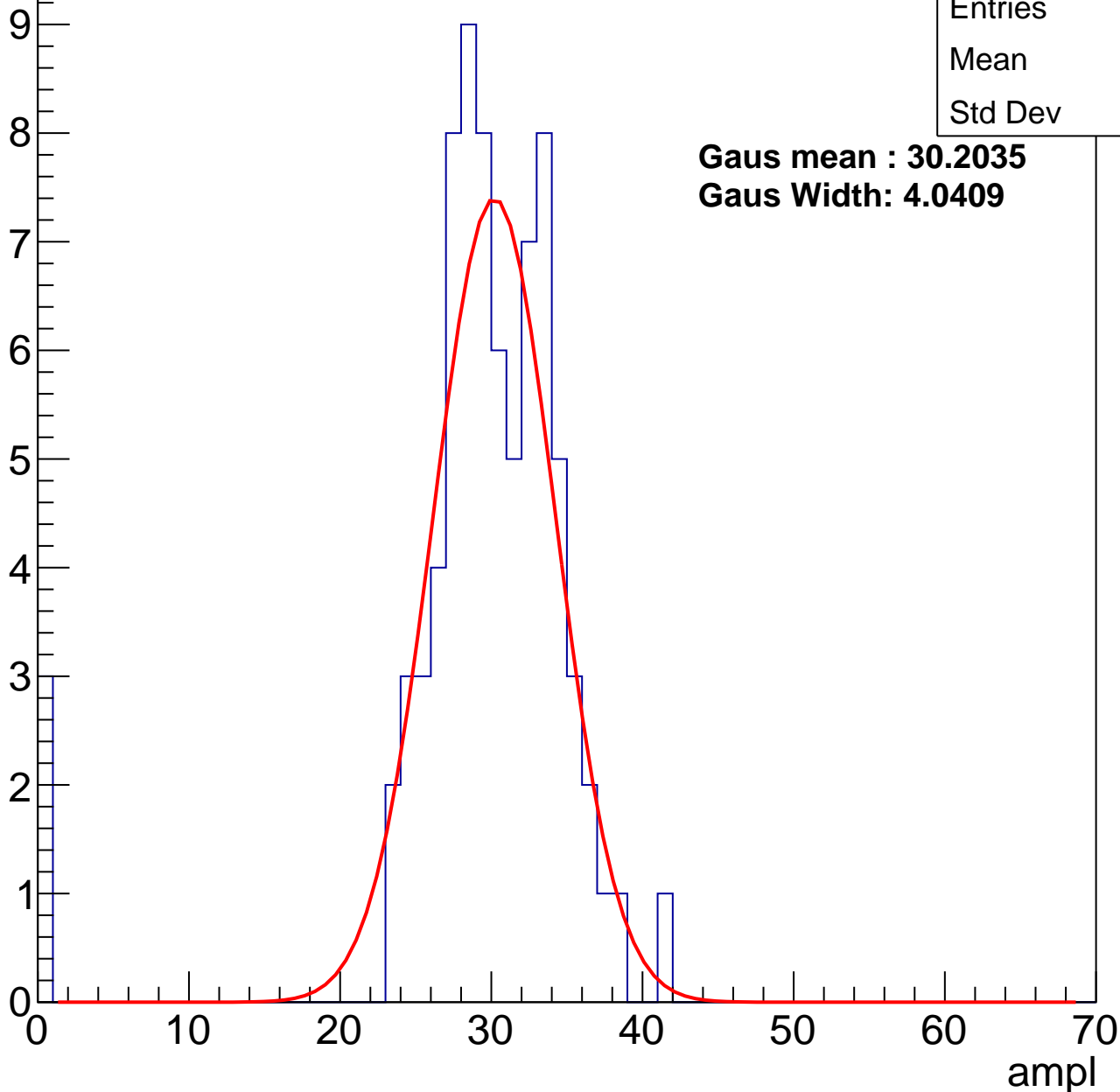
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	79
Mean	28.9
Std Dev	6.78

**Gaus mean : 30.2035**

**Gaus Width: 4.0409**



# B0L000S, U7-ch78, adc1

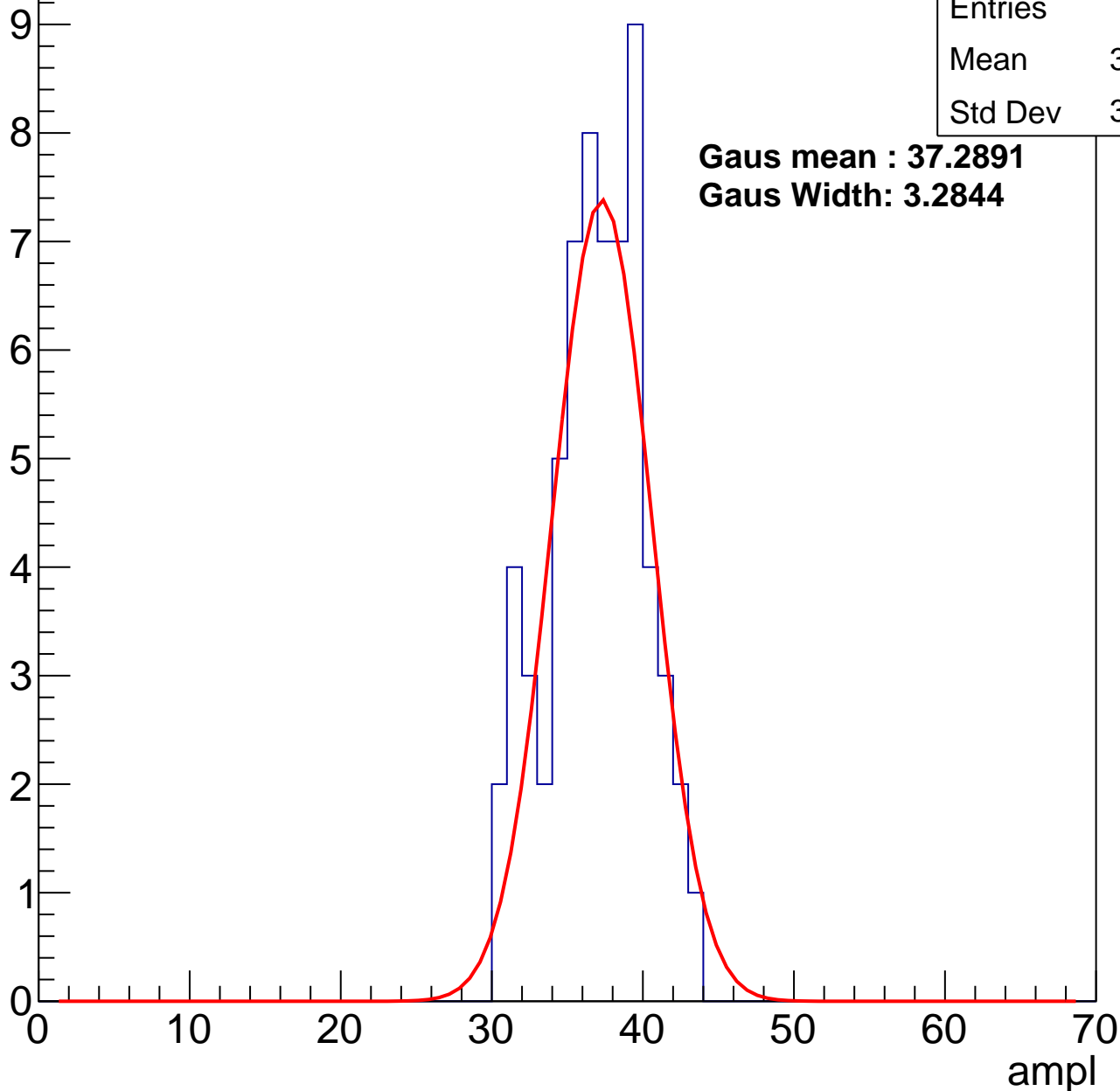
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	64
Mean	36.48
Std Dev	3.127

**Gaus mean : 37.2891**

**Gaus Width: 3.2844**



# B0L000S, U7-ch78, adc2

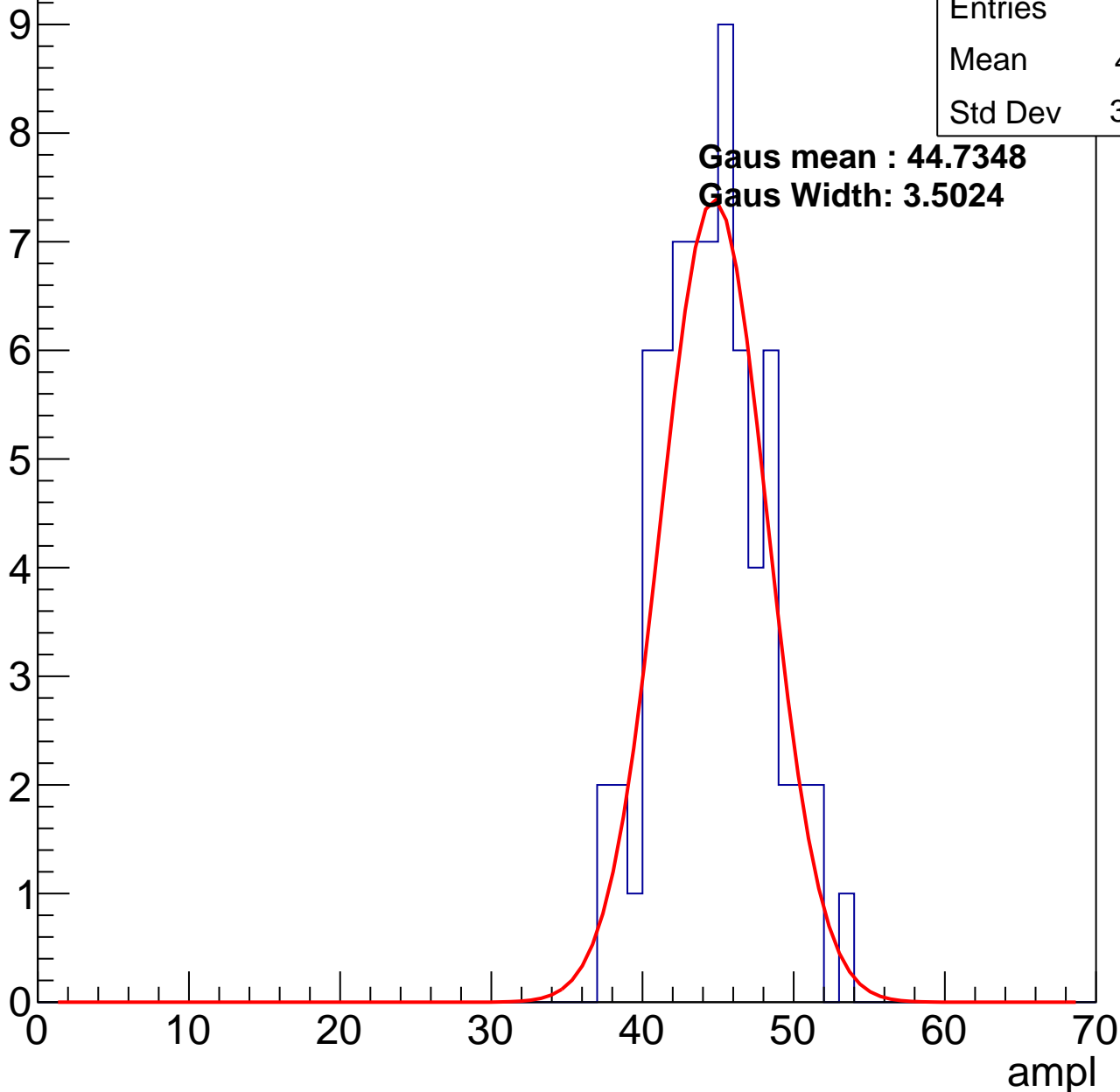
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	70
Mean	44.11
Std Dev	3.475

**Gaus mean : 44.7348**

**Gaus Width: 3.5024**

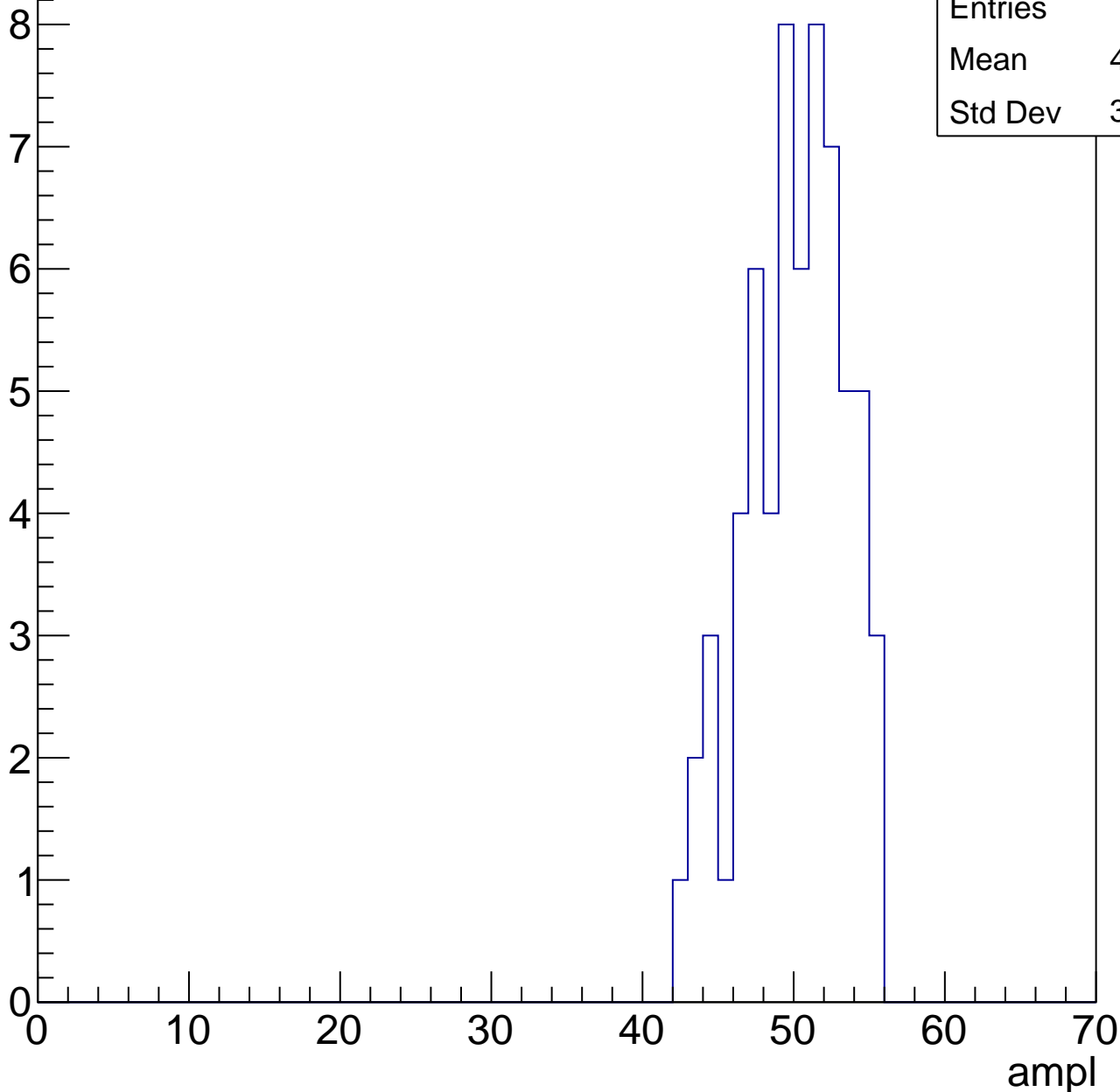


# B0L000S, U7-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	63
Mean	49.63
Std Dev	3.248

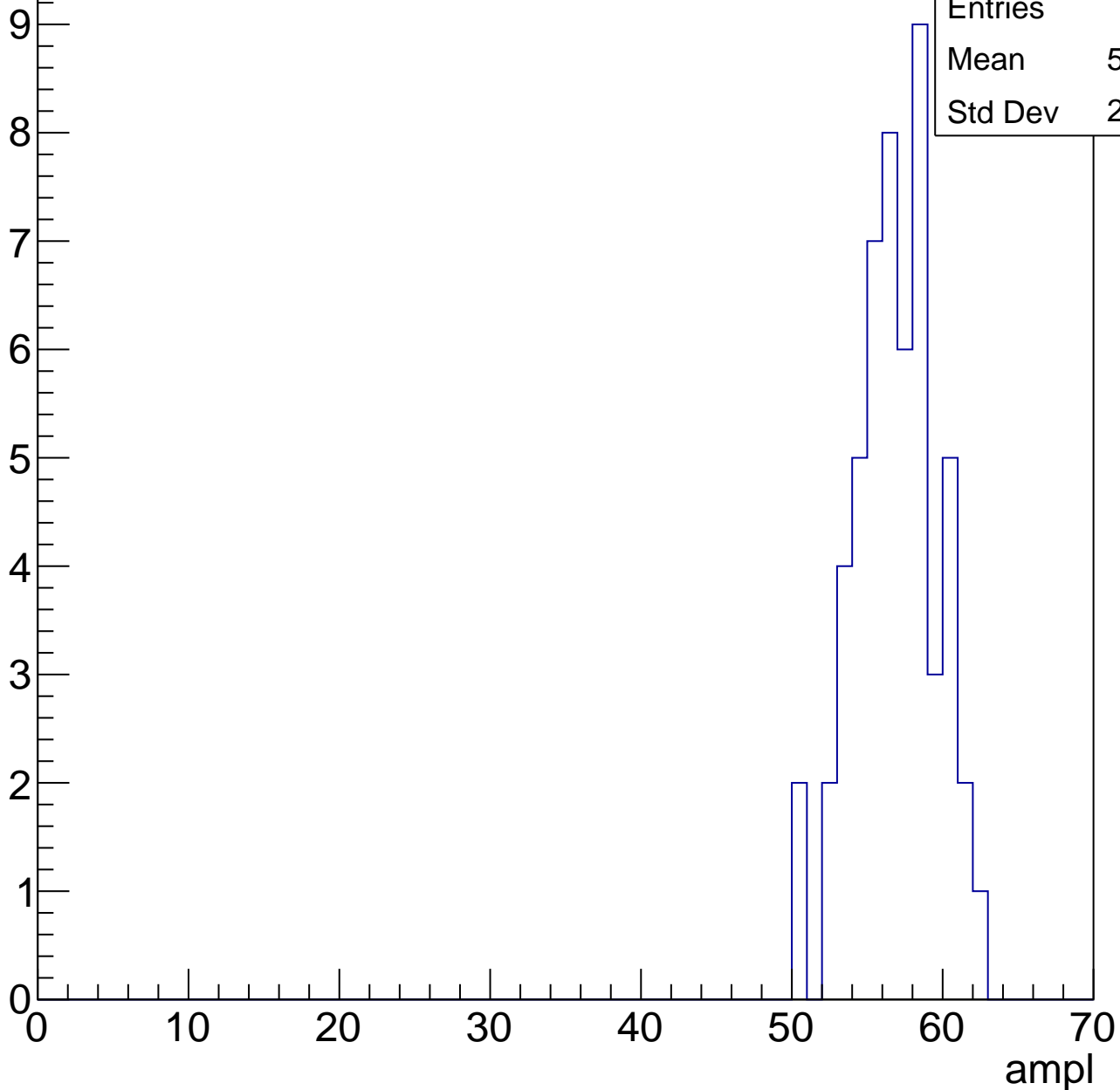


# B0L000S, U7-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	54
Mean	56.37
Std Dev	2.703

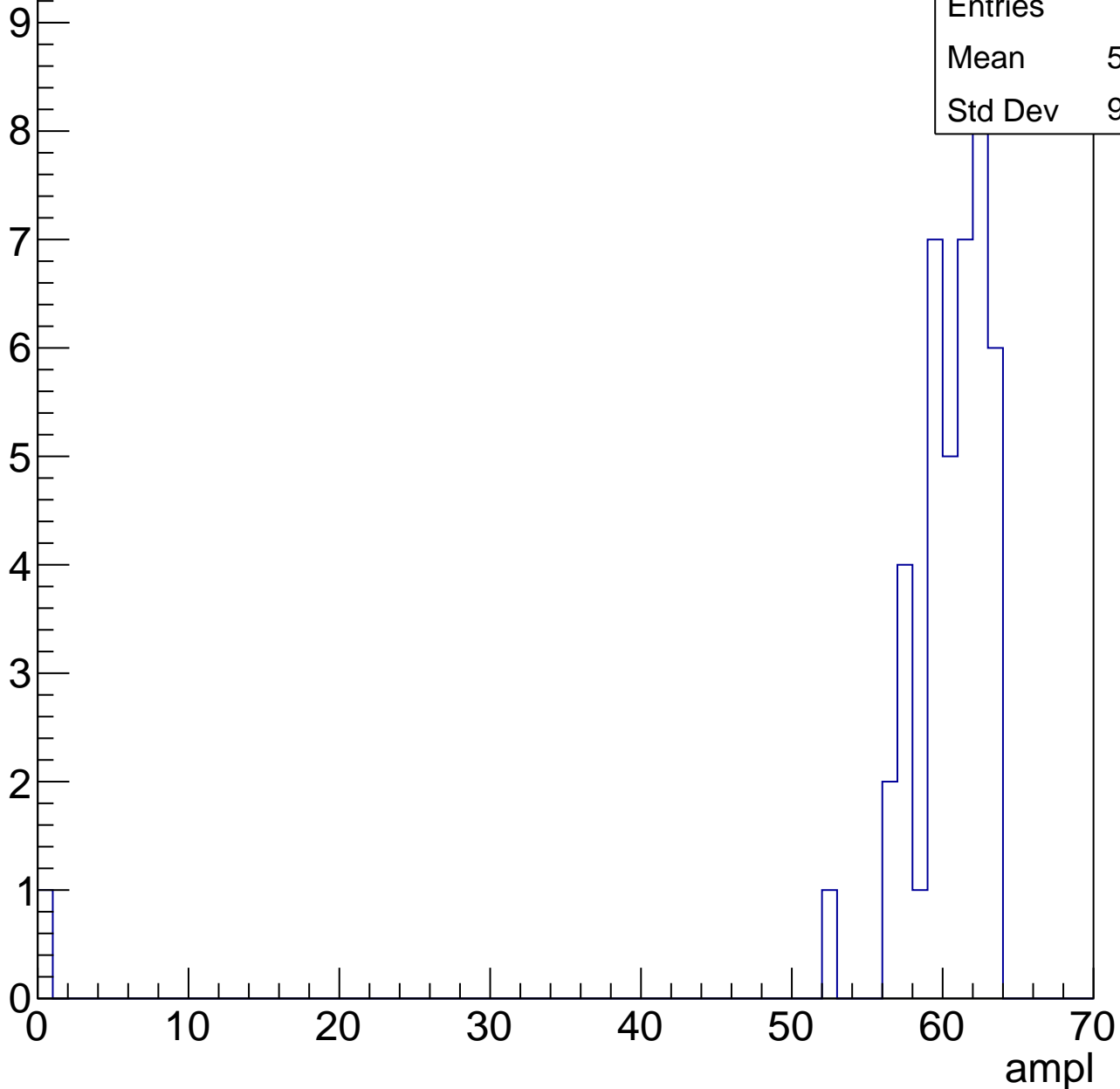


# B0L000S, U7-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

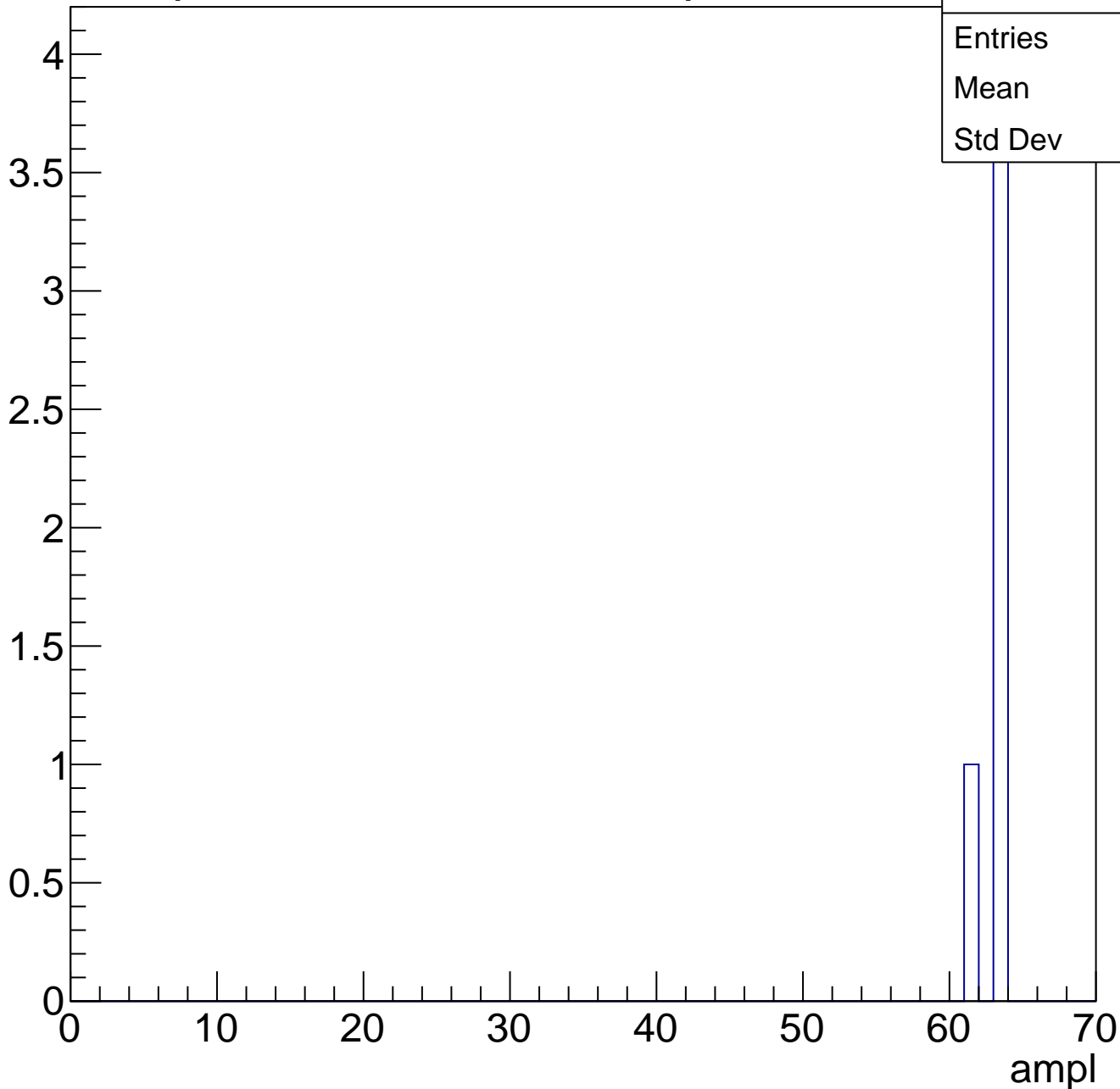
Entries	43
Mean	58.74
Std Dev	9.366



# B0L000S, U7-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L000S, U7-ch79, adc0

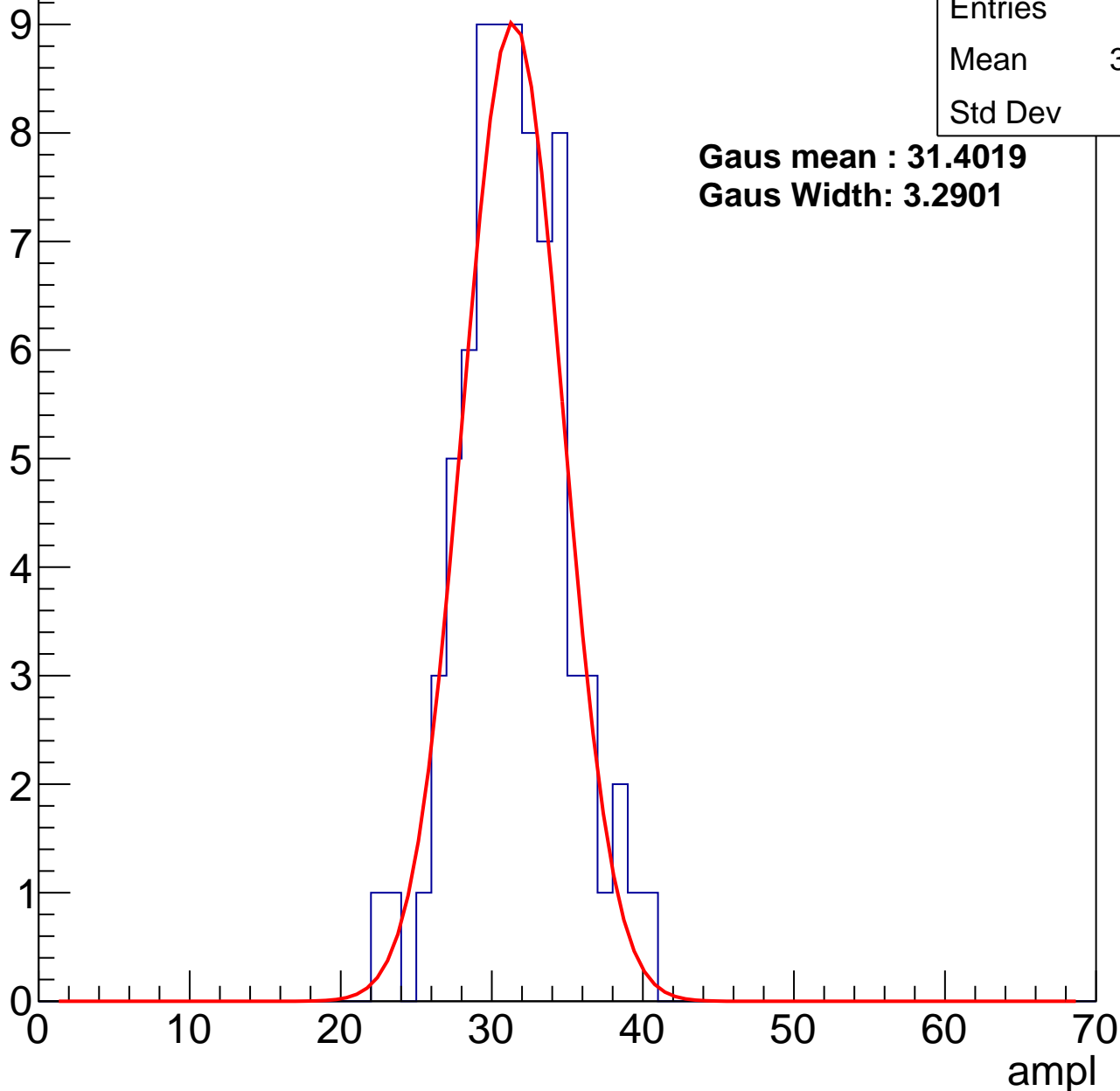
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	78
Mean	31.09
Std Dev	3.48

**Gaus mean : 31.4019**

**Gaus Width: 3.2901**



# B0L000S, U7-ch79, adc1

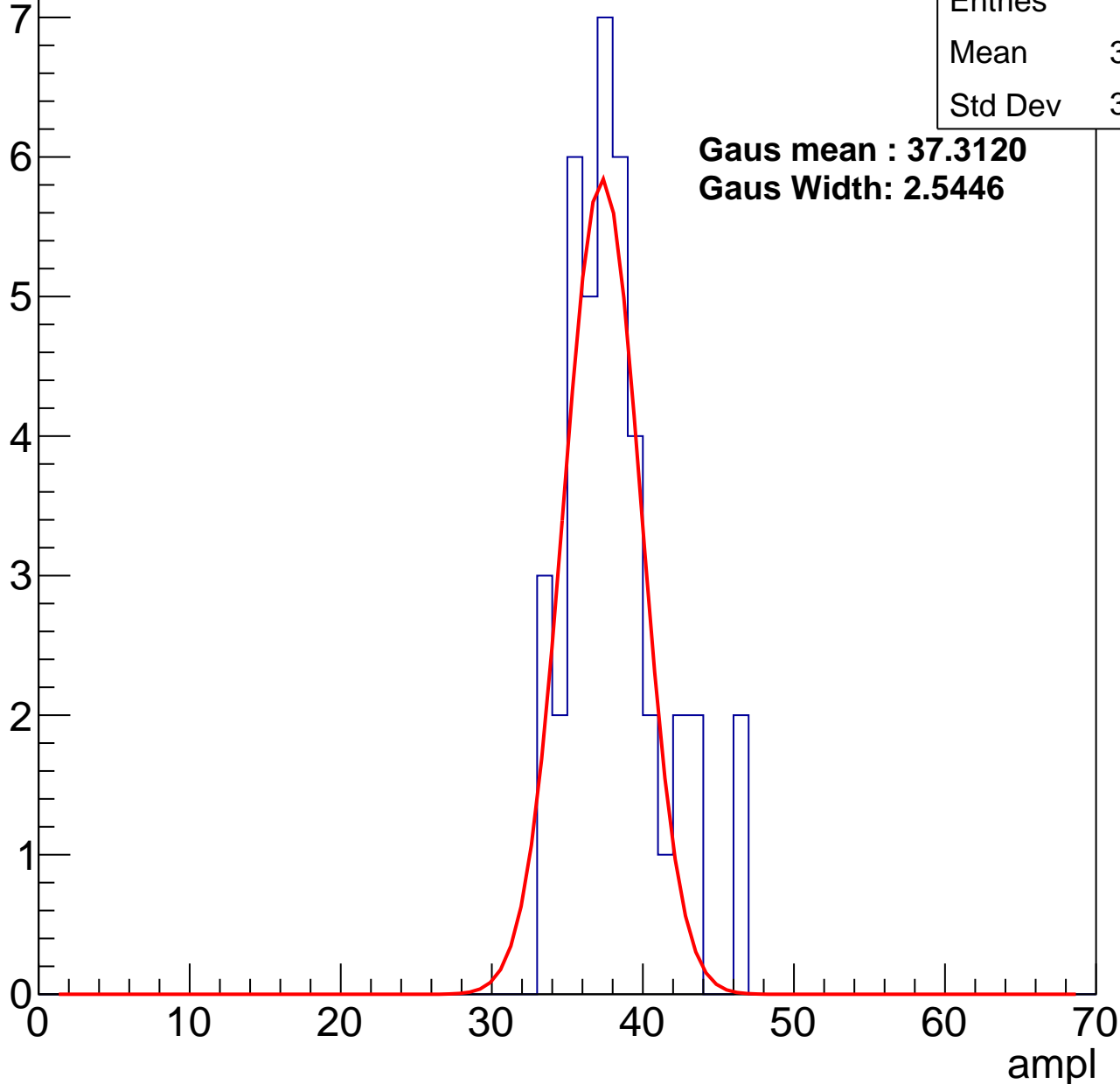
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	42
Mean	37.69
Std Dev	3.143

**Gaus mean : 37.3120**

**Gaus Width: 2.5446**



# B0L000S, U7-ch79, adc2

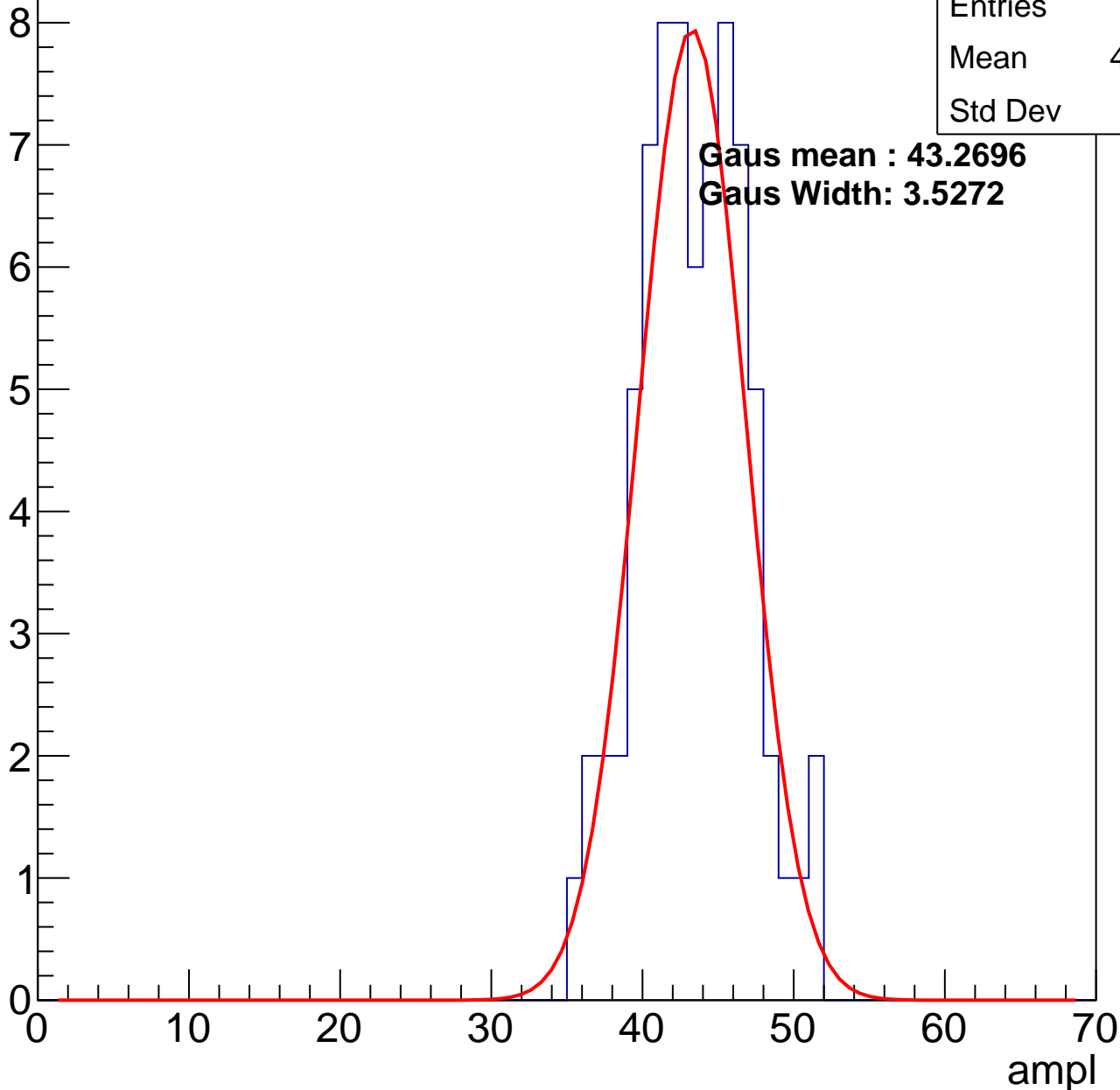
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	74
Mean	42.92
Std Dev	3.51

**Gaus mean : 43.2696**

**Gaus Width: 3.5272**

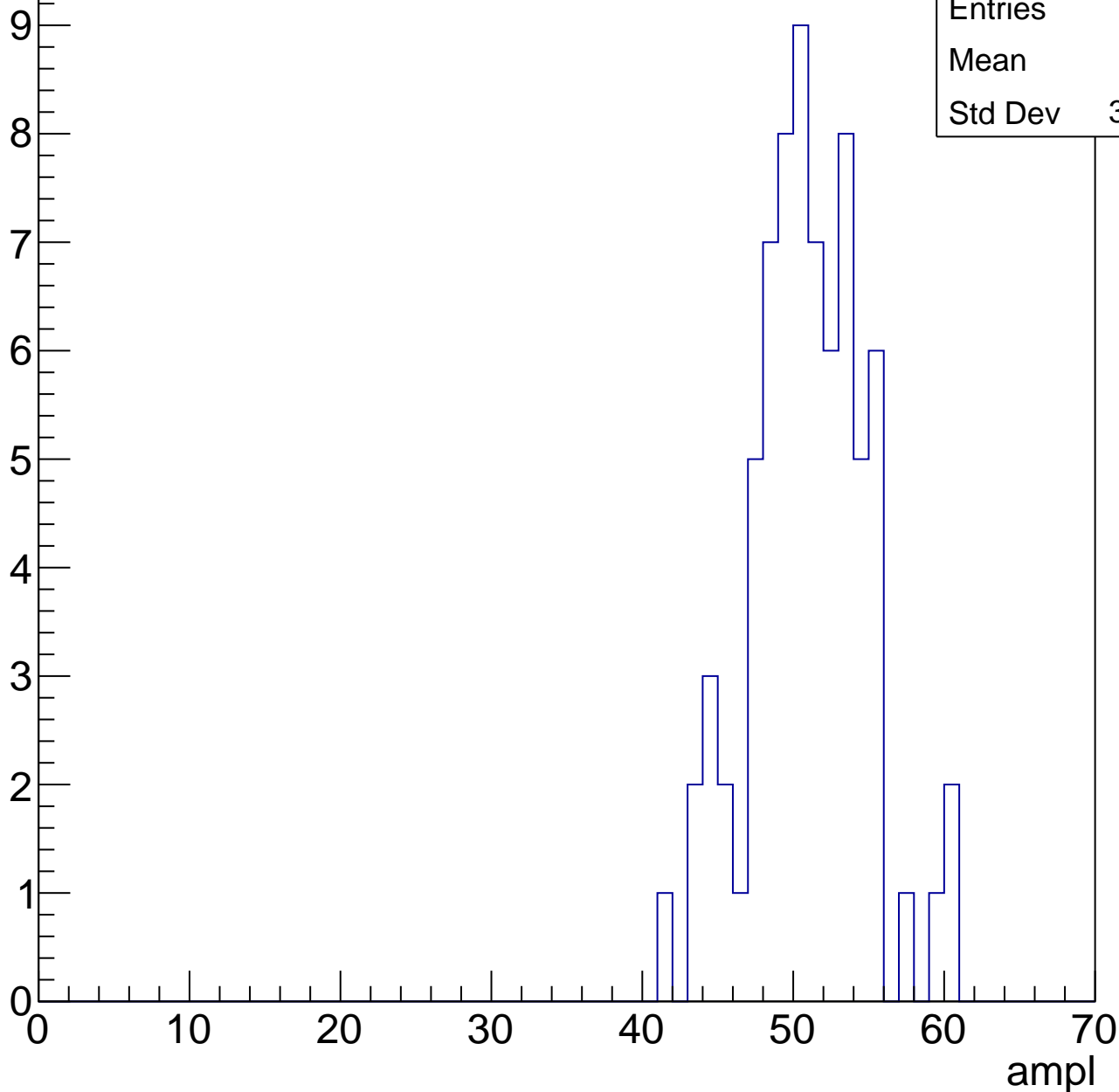


# B0L000S, U7-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

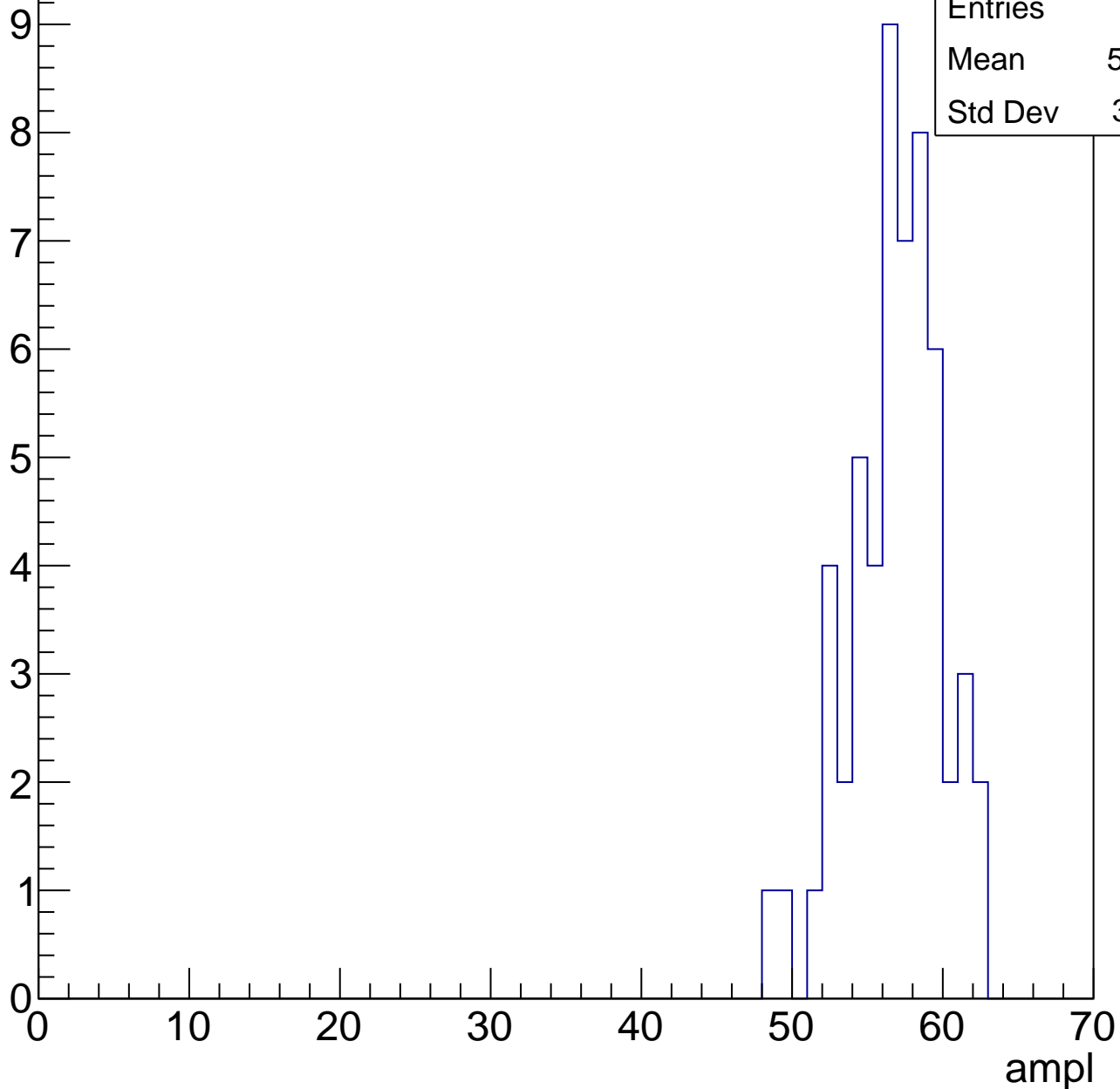
Entries	74
Mean	50.5
Std Dev	3.818



# B0L000S, U7-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

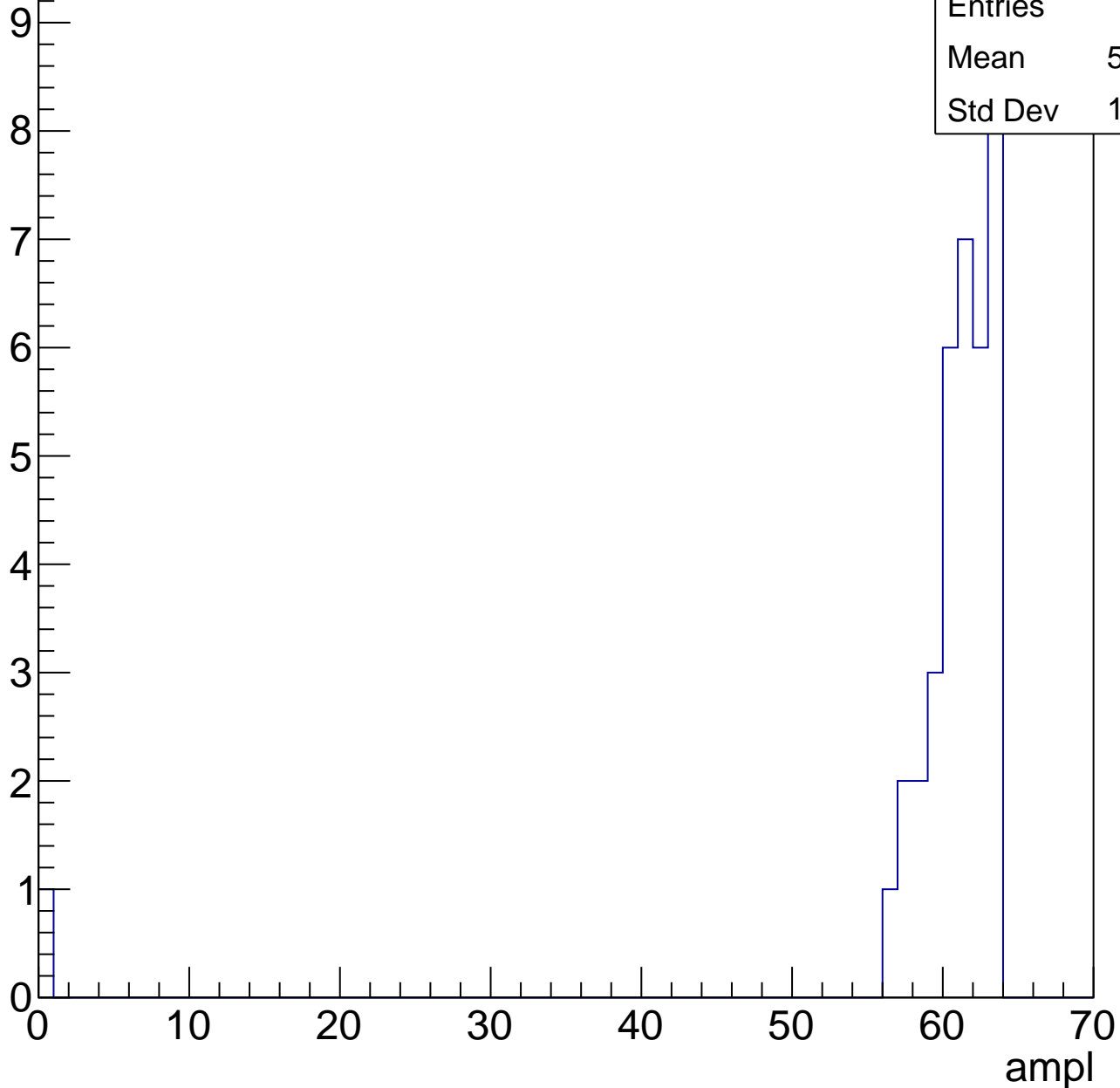
Entry



# B0L000S, U7-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

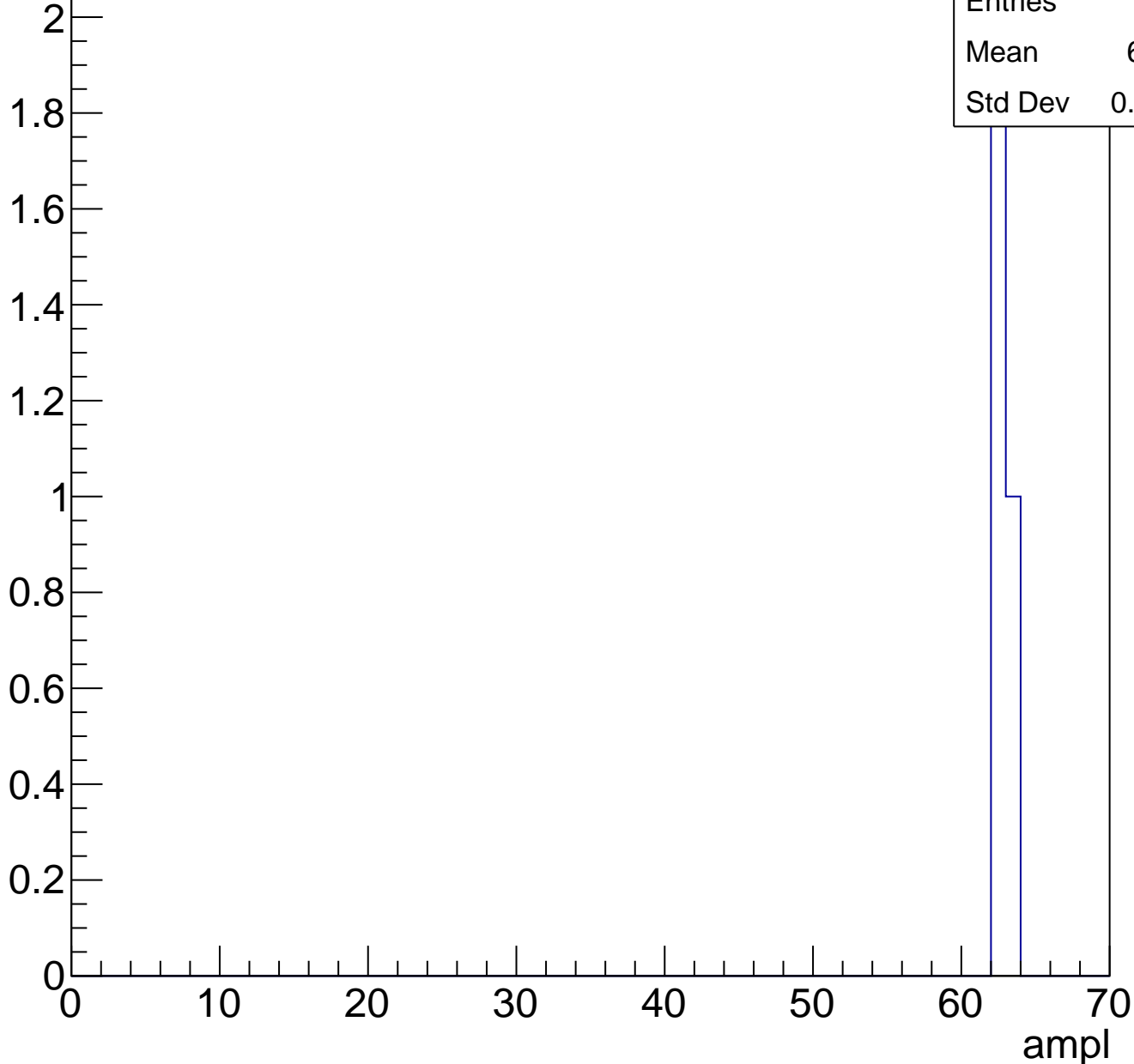
Entry



# B0L000S, U7-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L000S, U7-ch80, adc0

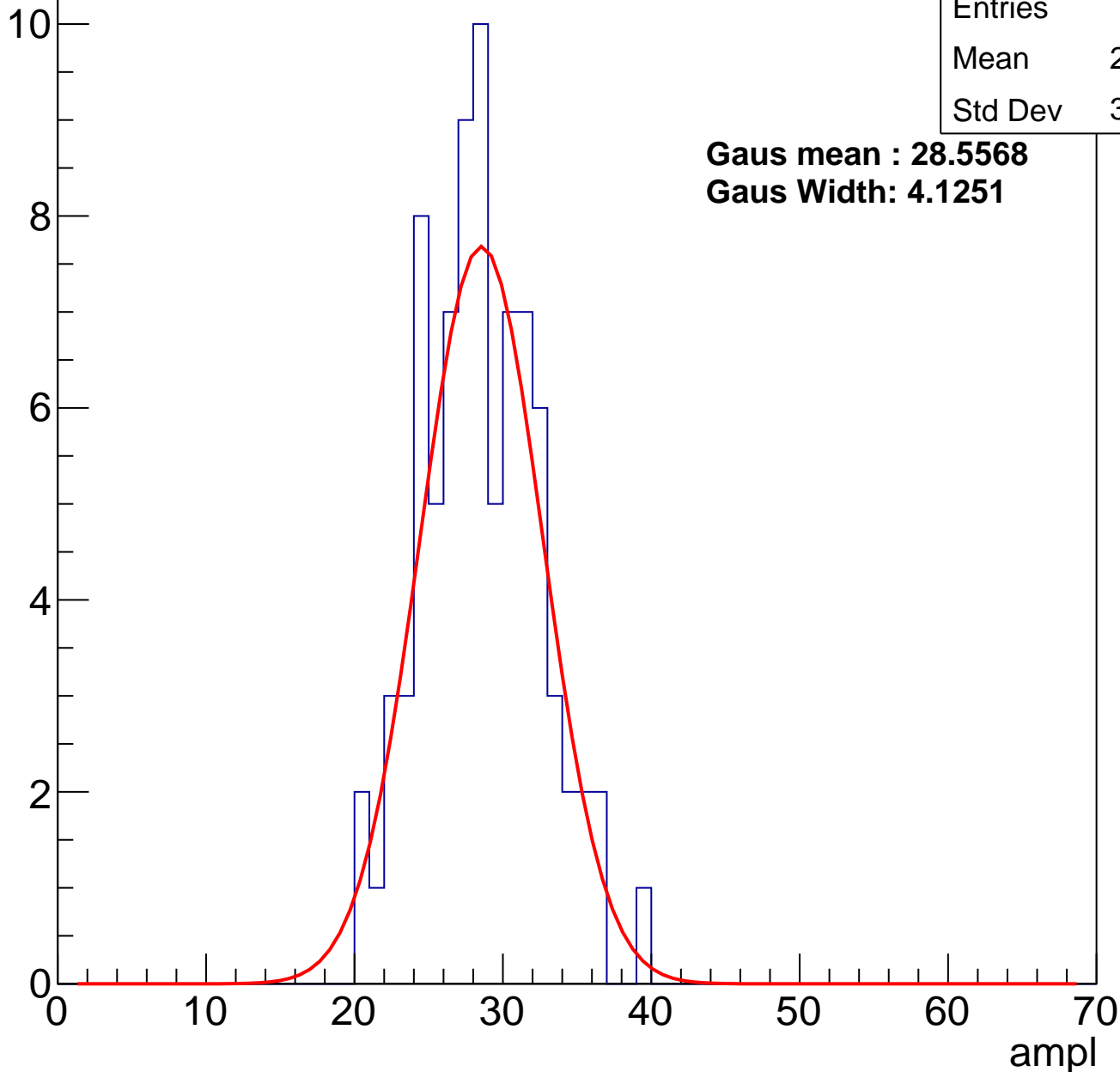
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	83
Mean	28.07
Std Dev	3.889

**Gaus mean : 28.5568**

**Gaus Width: 4.1251**

Entry



# B0L000S, U7-ch80, adc1

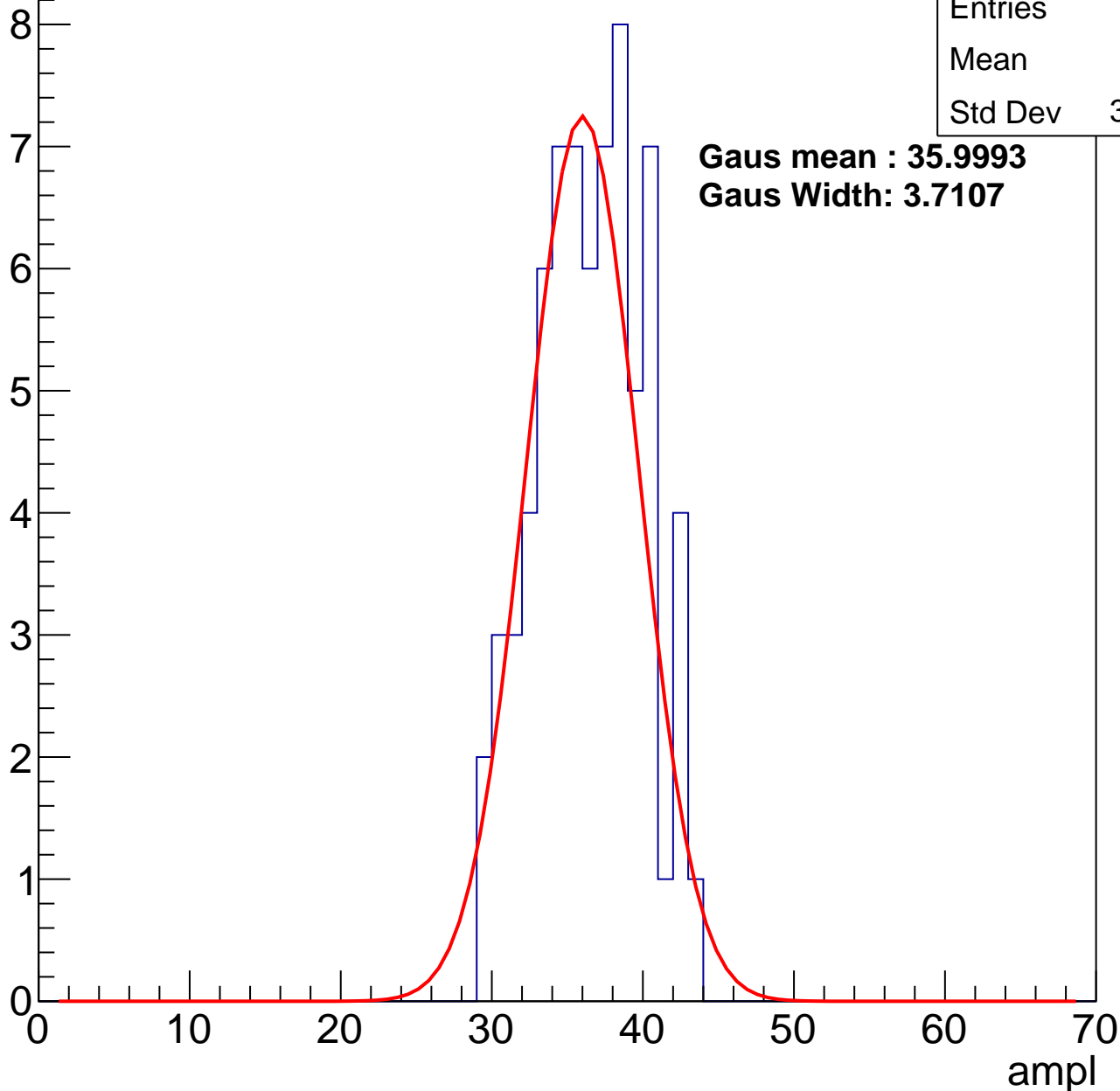
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	71
Mean	36
Std Dev	3.456

**Gaus mean : 35.9993**

**Gaus Width: 3.7107**



# B0L000S, U7-ch80, adc2

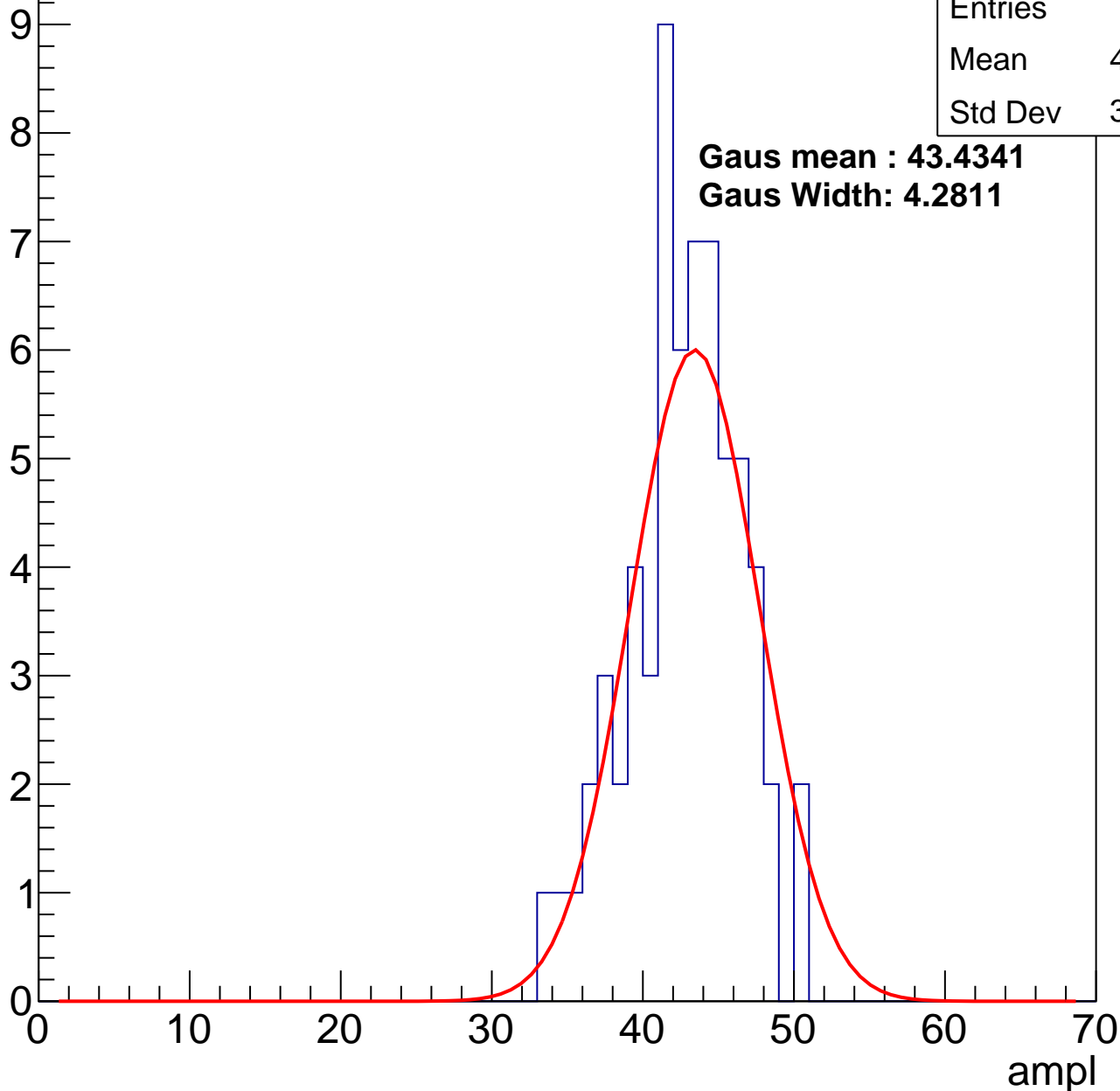
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	64
Mean	42.28
Std Dev	3.718

**Gaus mean : 43.4341**

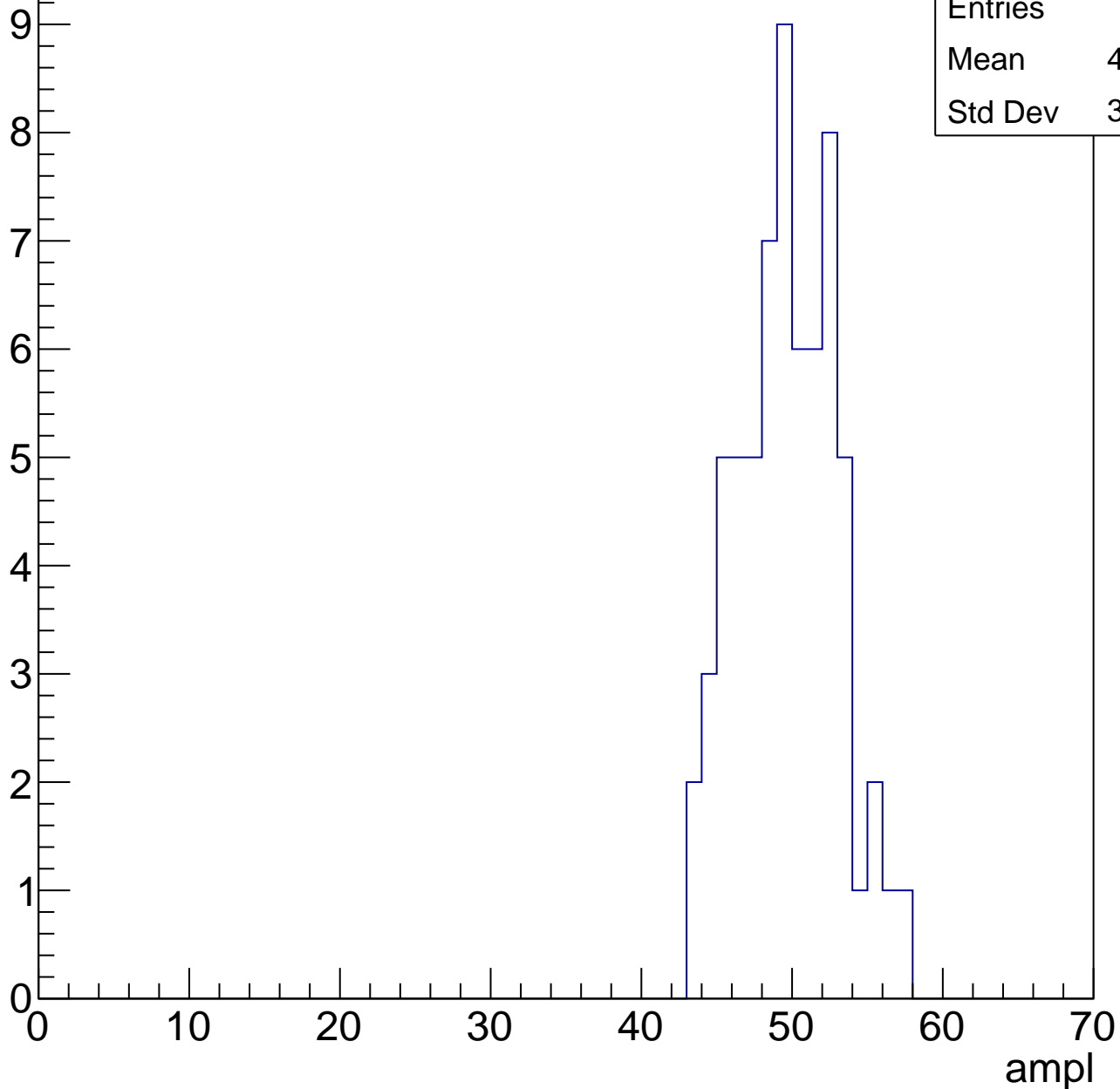
**Gaus Width: 4.2811**



# B0L000S, U7-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

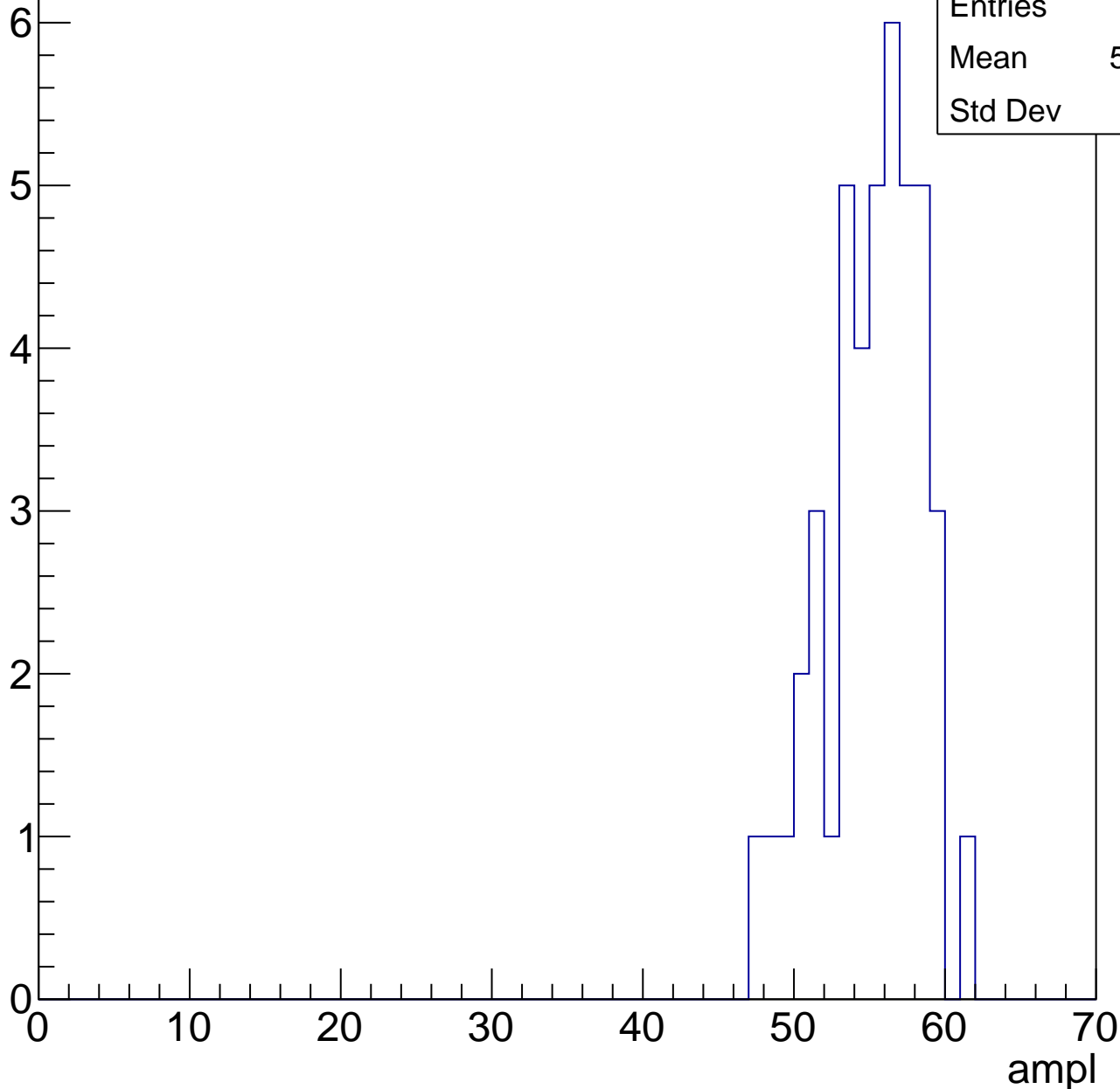


Entries	66
Mean	49.23
Std Dev	3.228

# B0L000S, U7-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

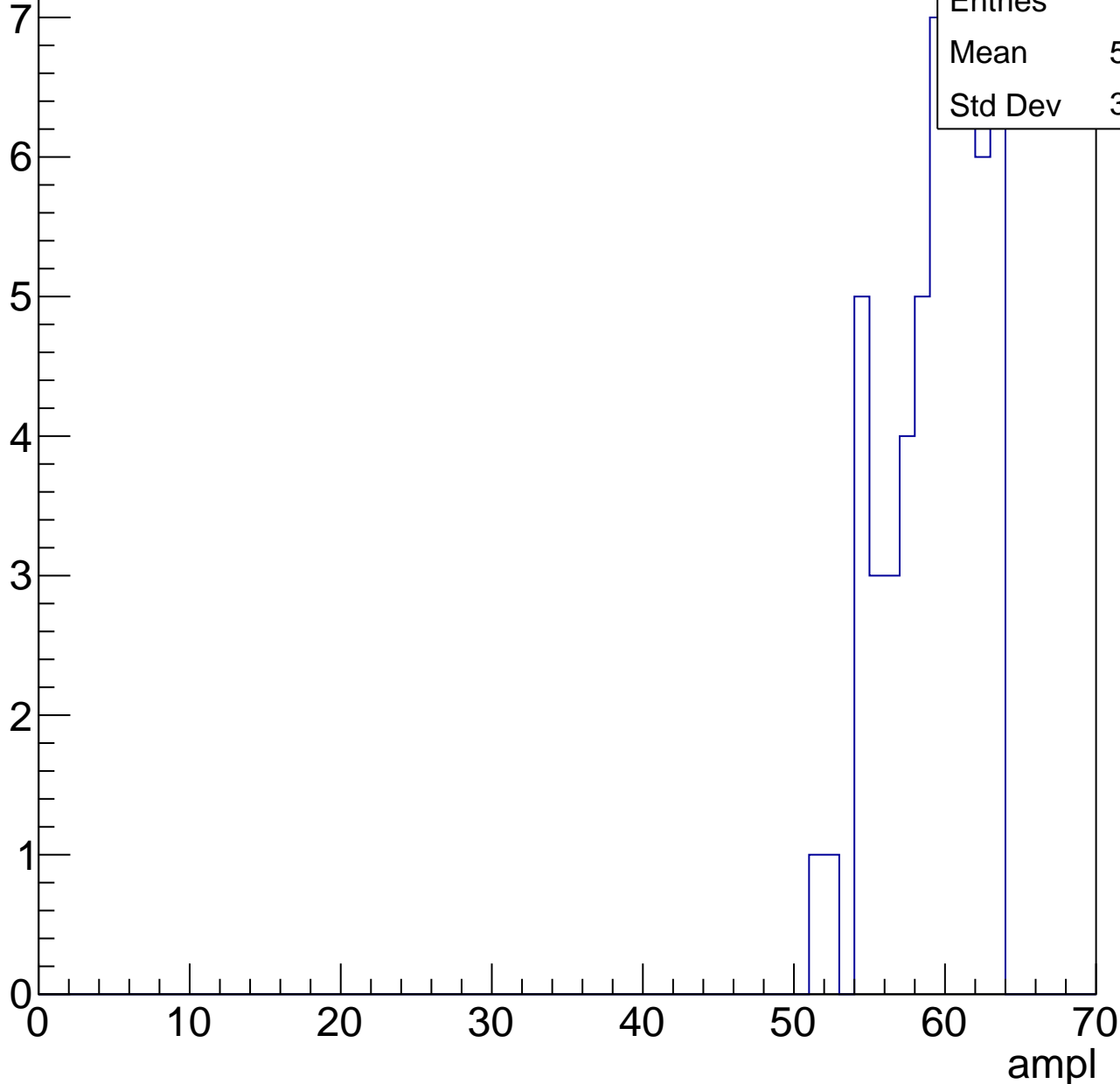


# B0L000S, U7-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

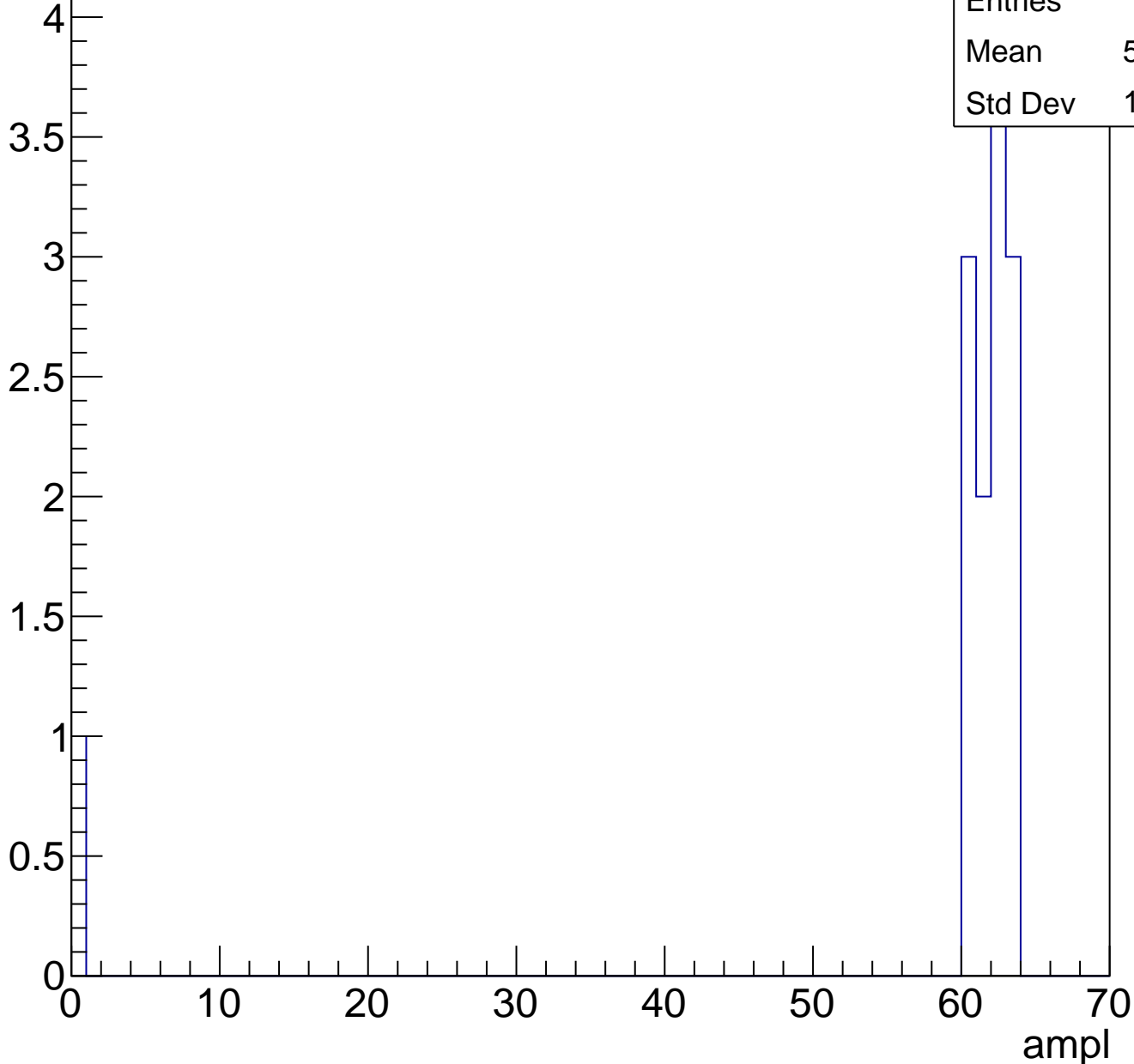
Entries	56
Mean	58.88
Std Dev	3.088



# B0L000S, U7-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	2
Mean	9.5
Std Dev	9.5

# B0L000S, U7-ch81, adc0

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	69
Mean	29.54
Std Dev	4.862

**Gaus mean : 30.9768**

**Gaus Width: 3.5120**

Entry

10  
8  
6  
4  
2  
0

ampl

0

10

20

30

40

50

60

70

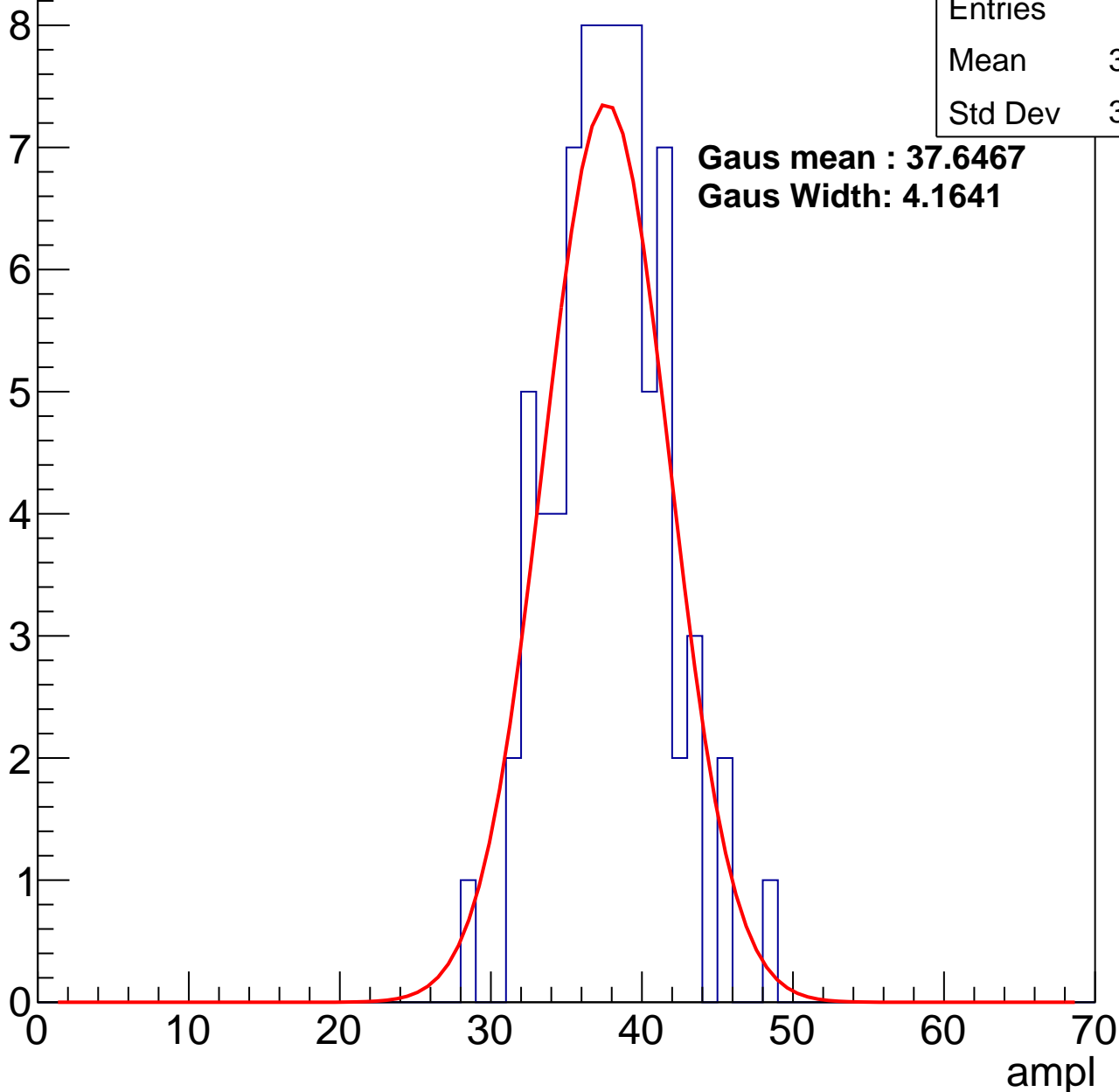
# B0L000S, U7-ch81, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	75
Mean	37.35
Std Dev	3.668

**Gaus mean : 37.6467**  
**Gaus Width: 4.1641**



# B0L000S, U7-ch81, adc2

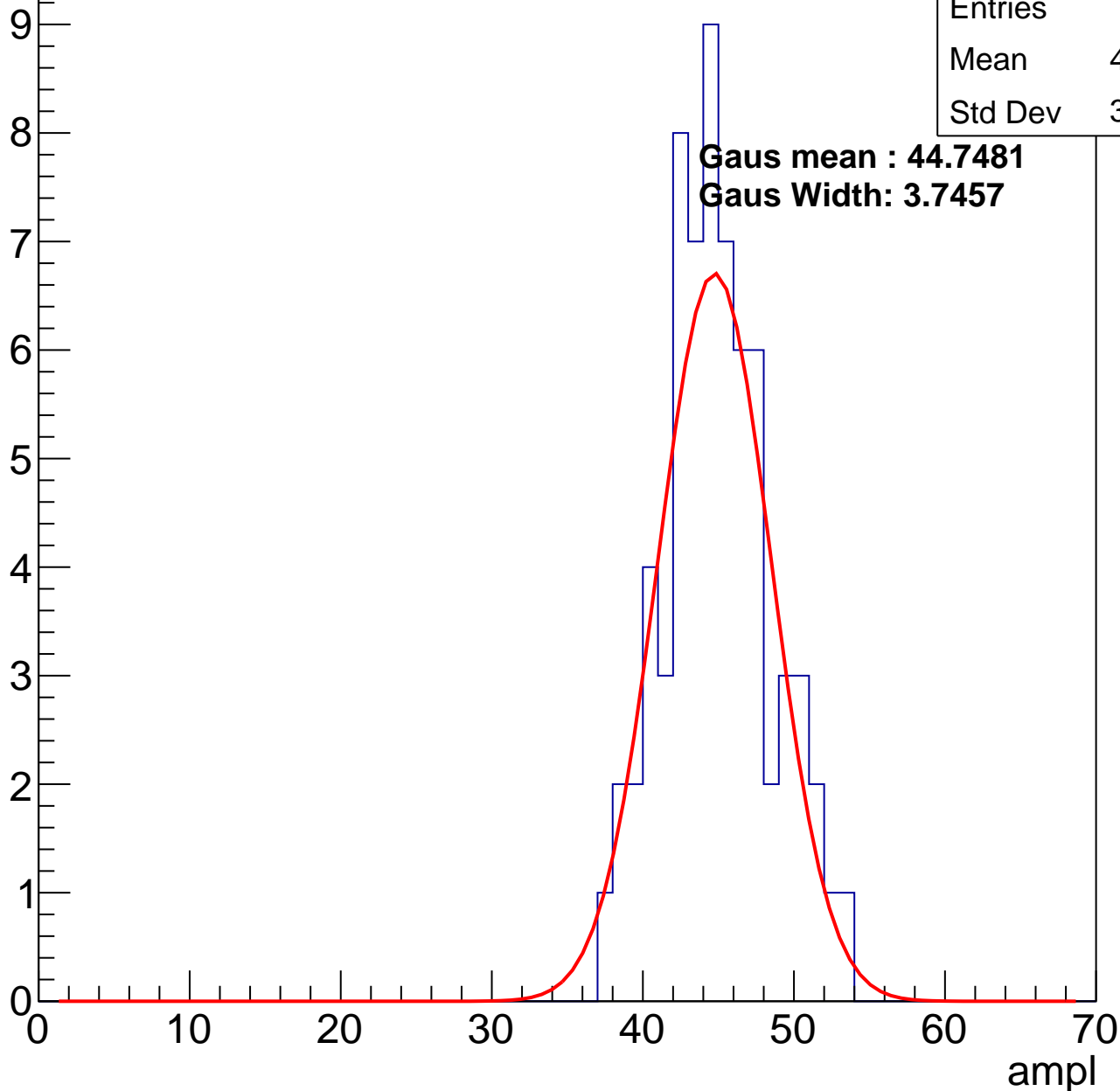
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	67
Mean	44.48
Std Dev	3.517

**Gaus mean : 44.7481**

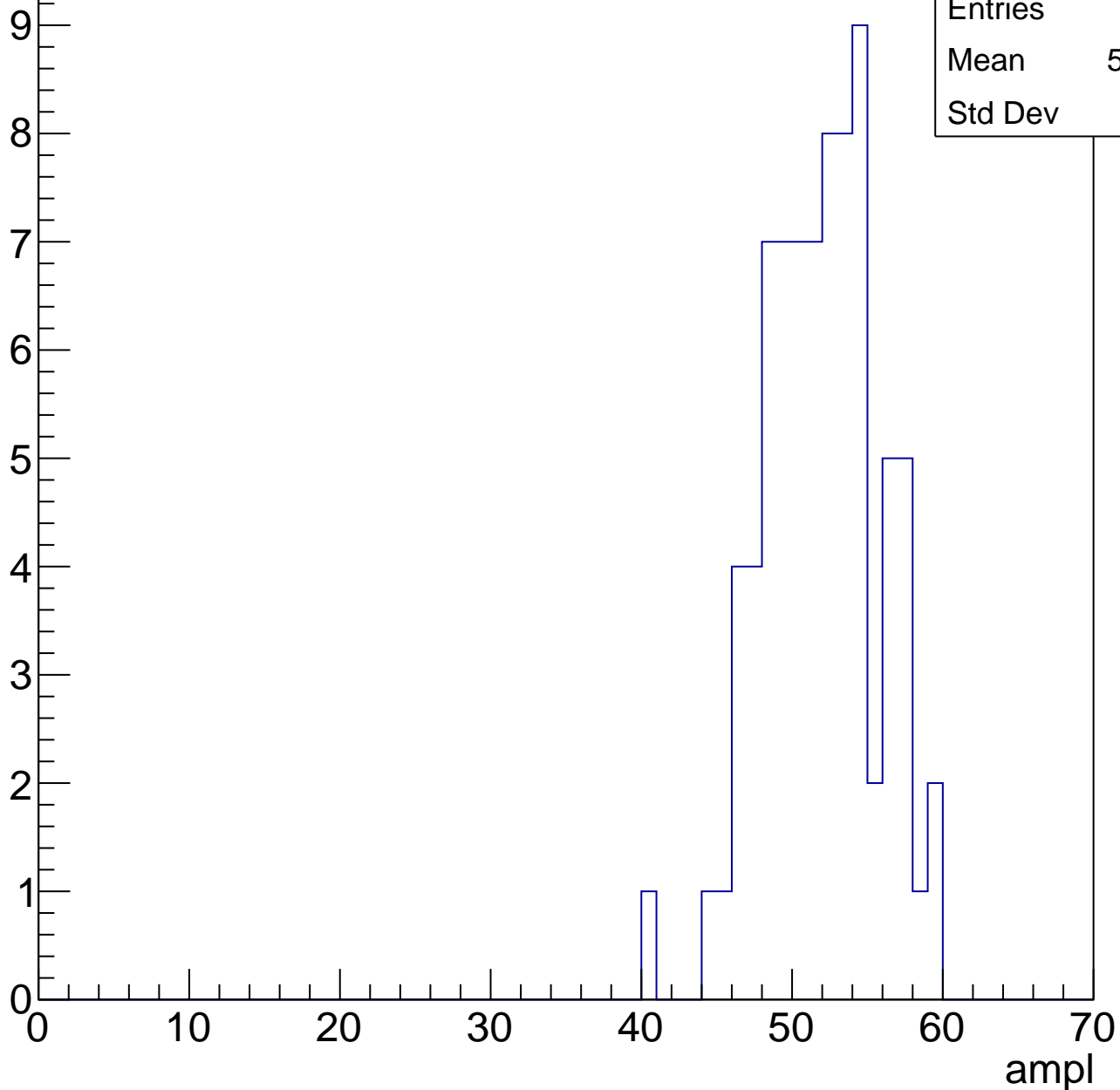
**Gaus Width: 3.7457**



# B0L000S, U7-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

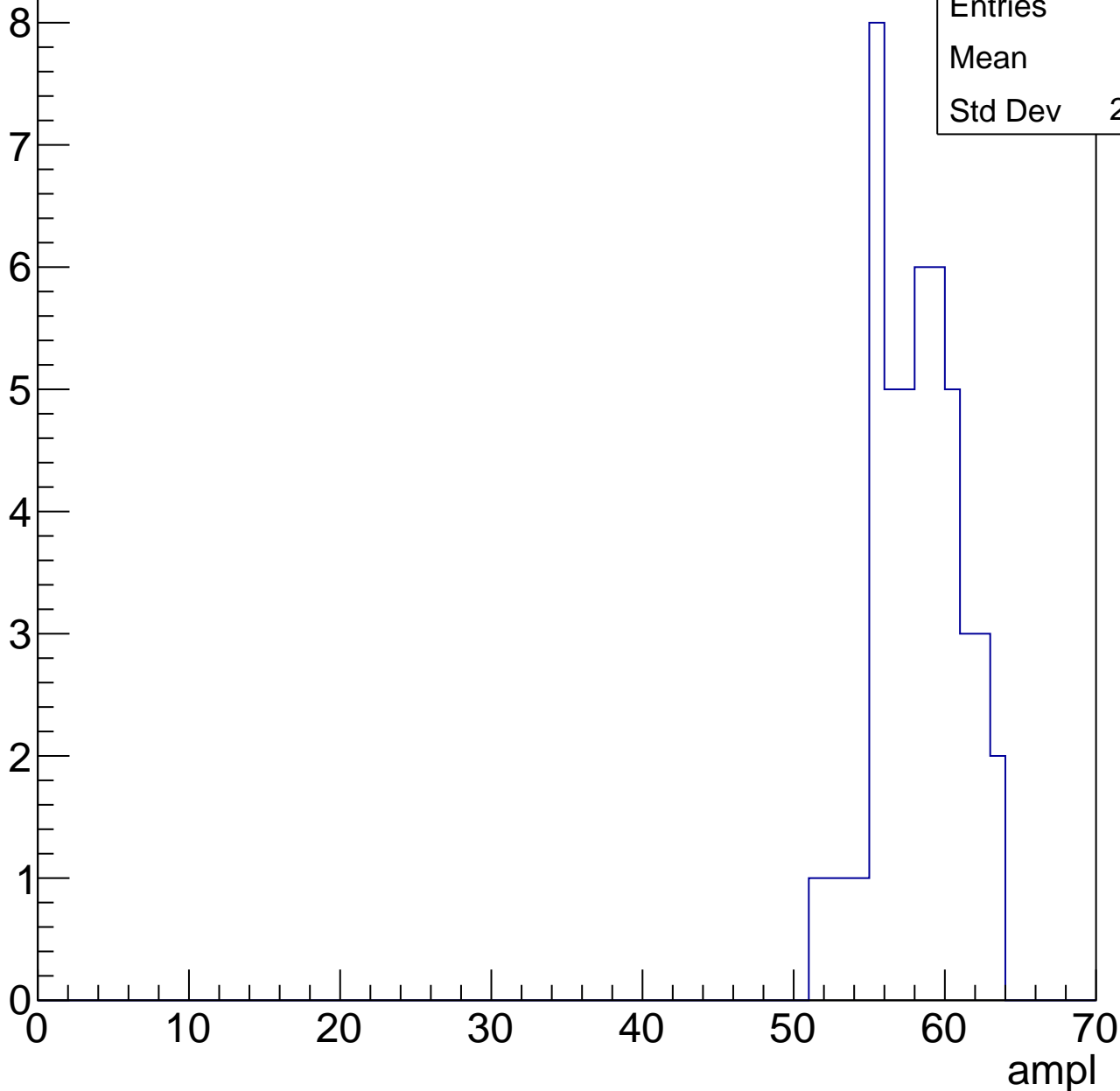


# B0L000S, U7-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	47
Mean	57.7
Std Dev	2.805

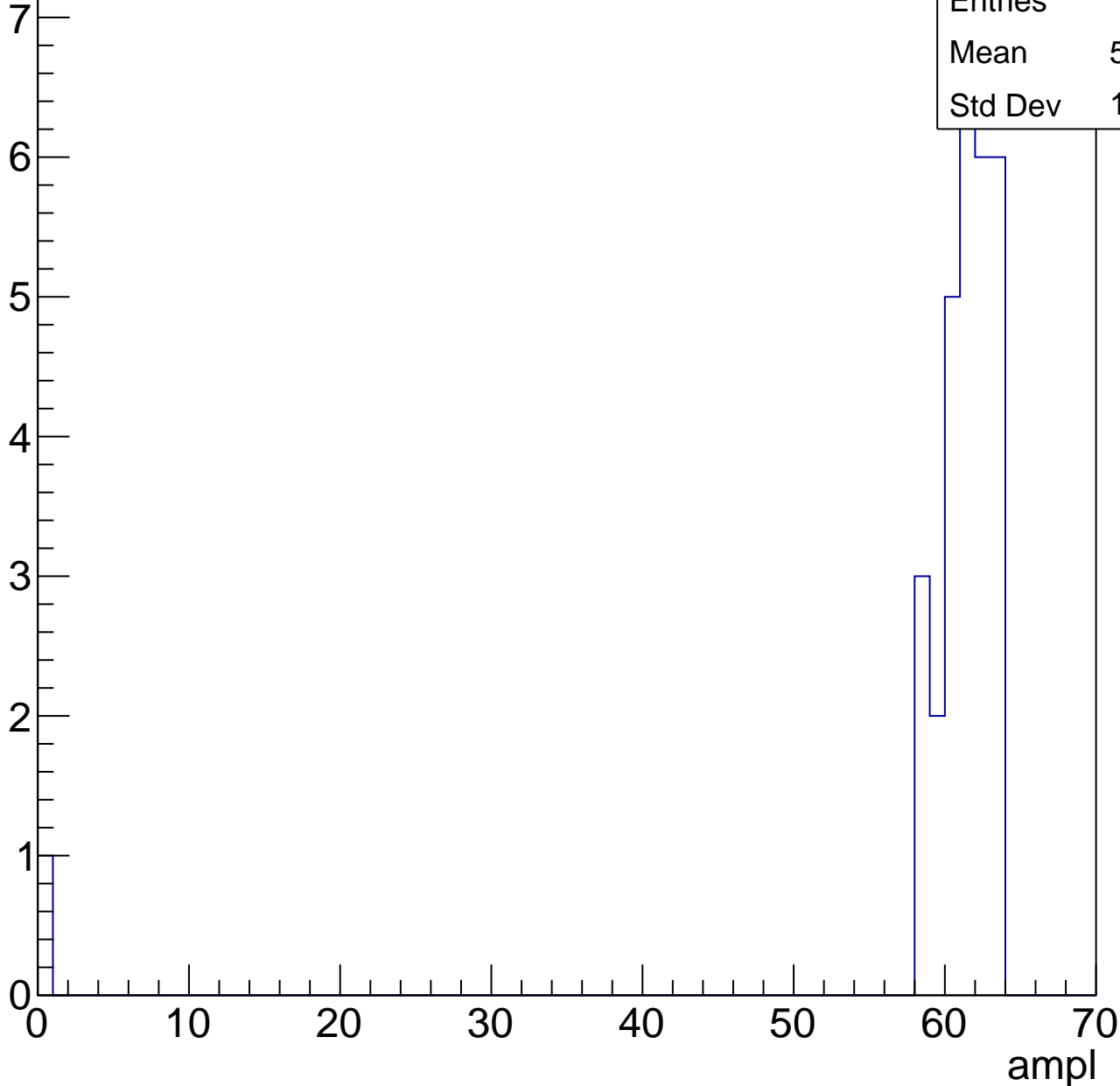


# B0L000S, U7-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	30
Mean	58.97
Std Dev	11.06



# B0L000S, U7-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch82, adc0

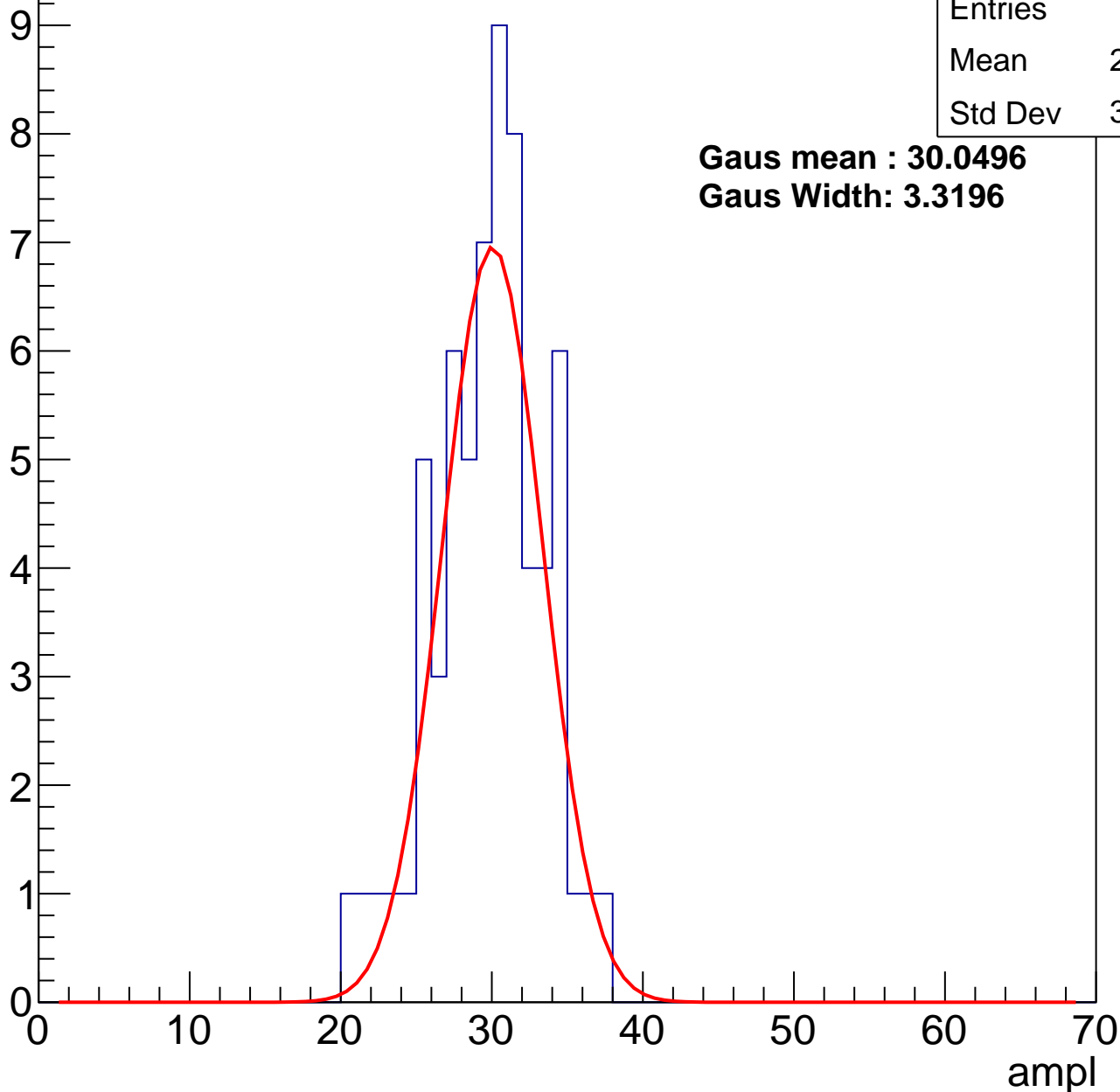
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	65
Mean	29.35
Std Dev	3.558

**Gaus mean : 30.0496**

**Gaus Width: 3.3196**



# B0L000S, U7-ch82, adc1

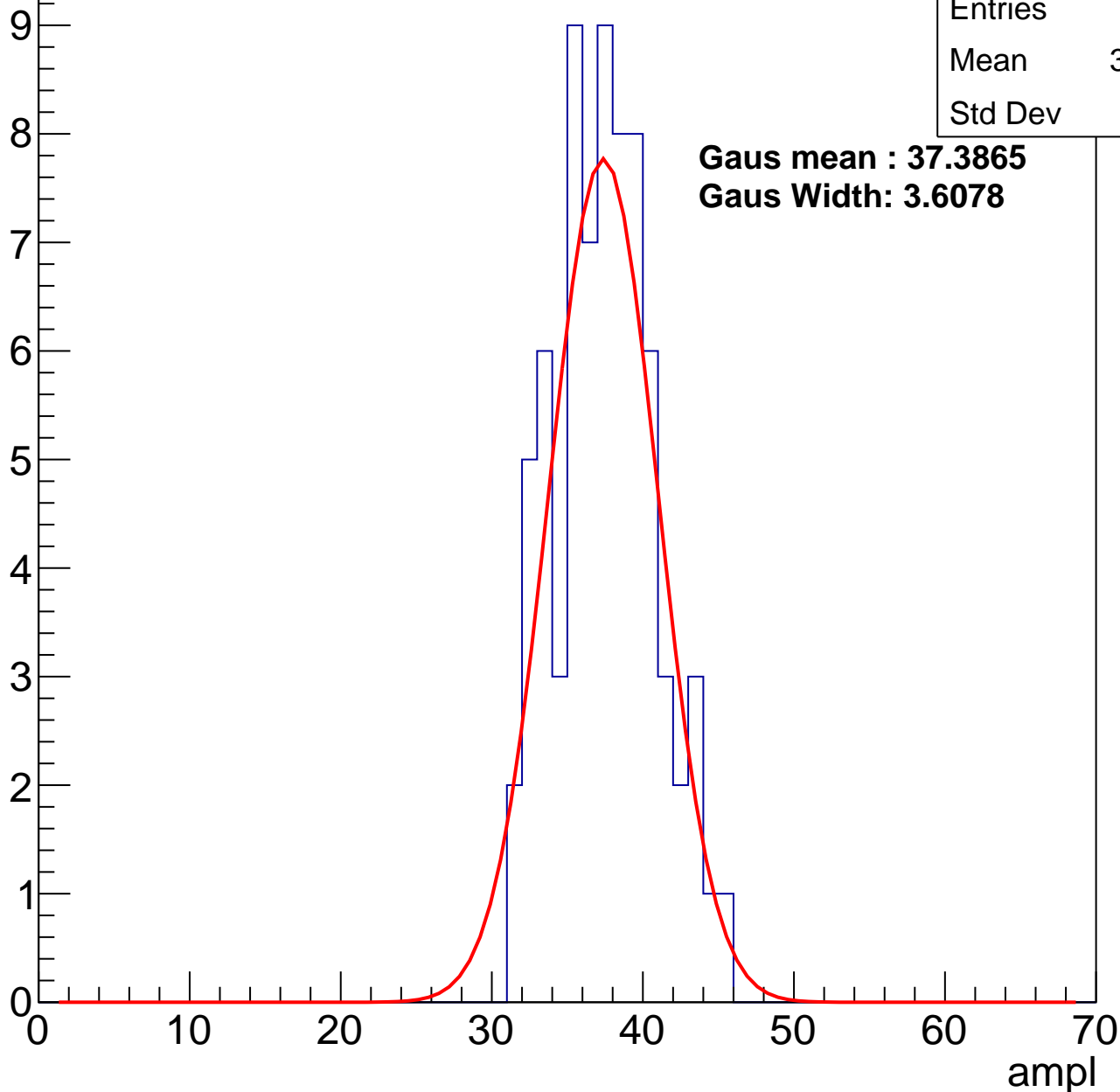
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	73
Mean	37.03
Std Dev	3.26

**Gaus mean : 37.3865**

**Gaus Width: 3.6078**



# B0L000S, U7-ch82, adc2

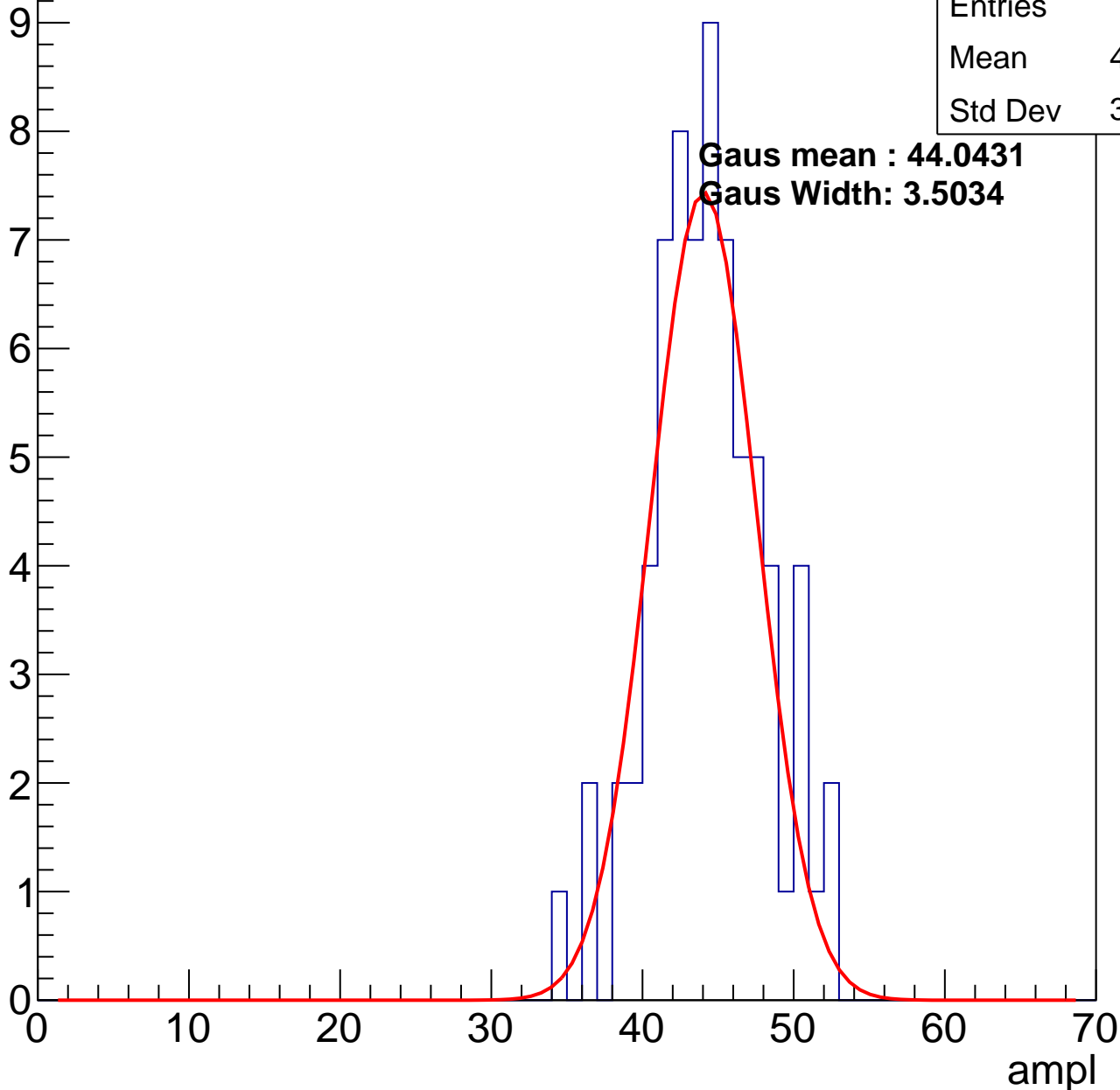
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	71
Mean	43.89
Std Dev	3.747

**Gaus mean : 44.0431**

**Gaus Width: 3.5034**

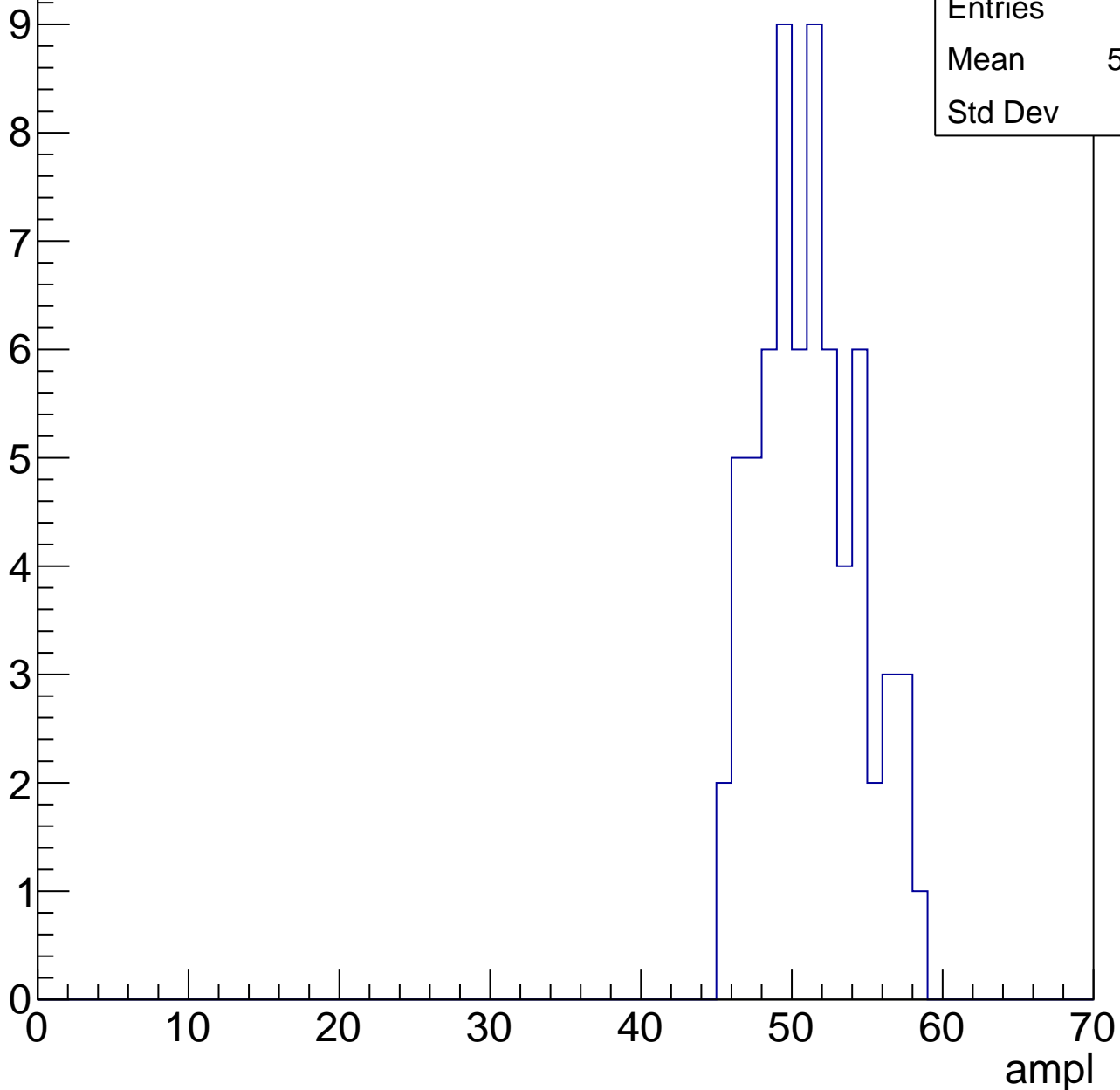


# B0L000S, U7-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	67
Mean	50.72
Std Dev	3.25

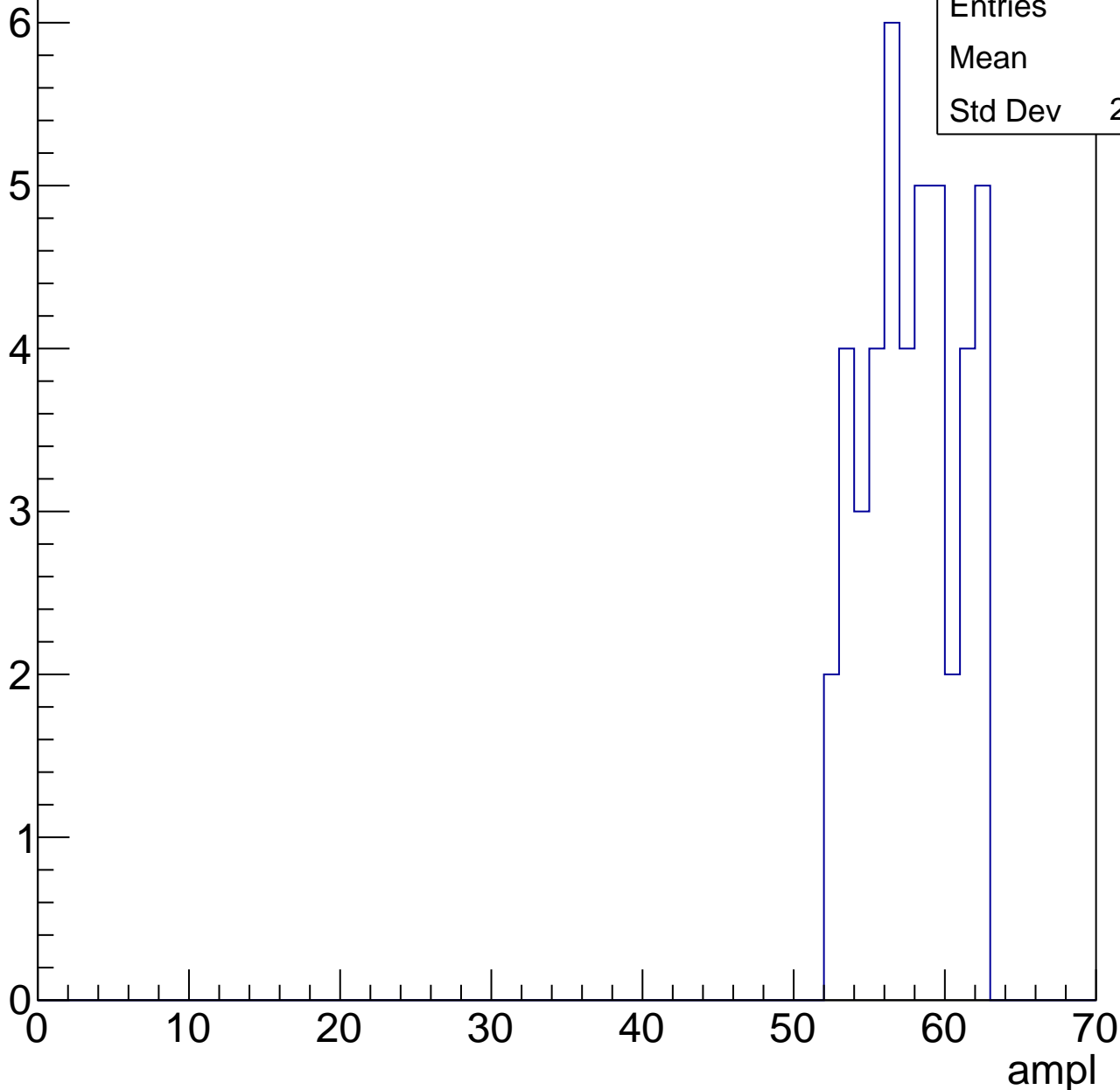


# B0L000S, U7-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	44
Mean	57.3
Std Dev	2.982



# B0L000S, U7-ch82, adc5

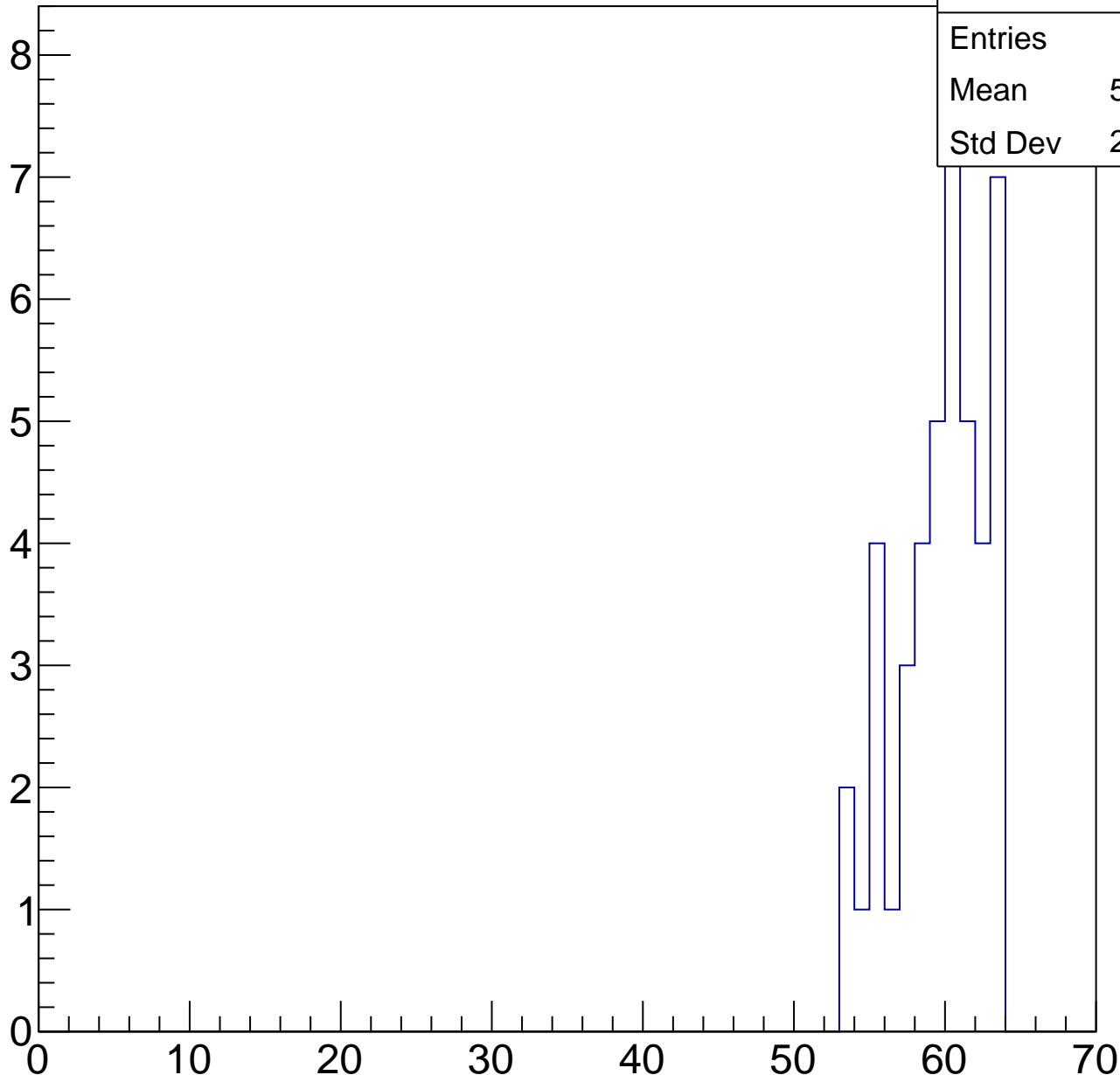
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	44
Mean	59.27
Std Dev	2.855

ampl



# B0L000S, U7-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	6
Mean	52
Std Dev	23.27



# B0L000S, U7-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L000S, U7-ch83, adc0

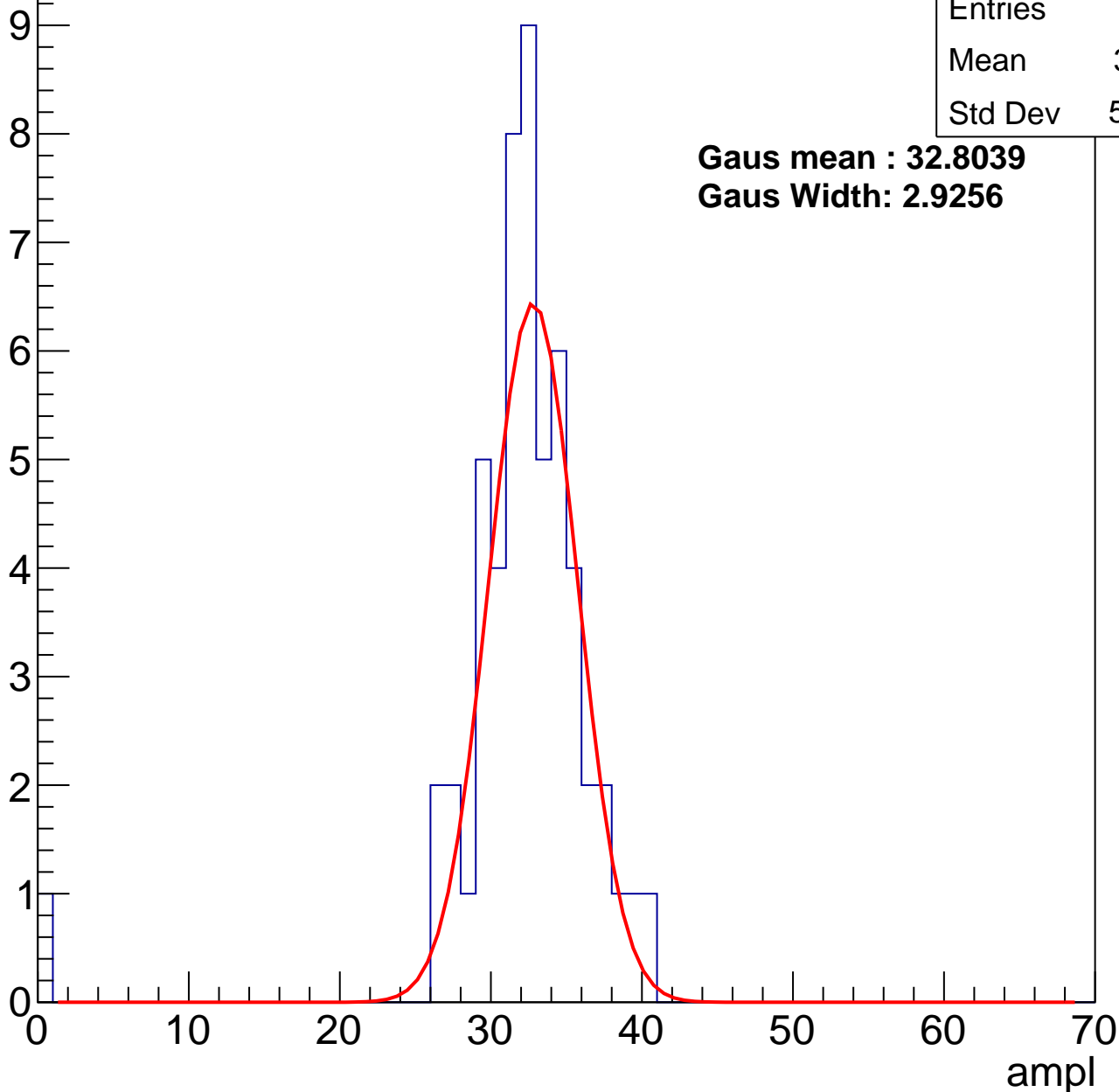
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	54
Mean	31.61
Std Dev	5.303

**Gaus mean : 32.8039**

**Gaus Width: 2.9256**



# B0L000S, U7-ch83, adc1

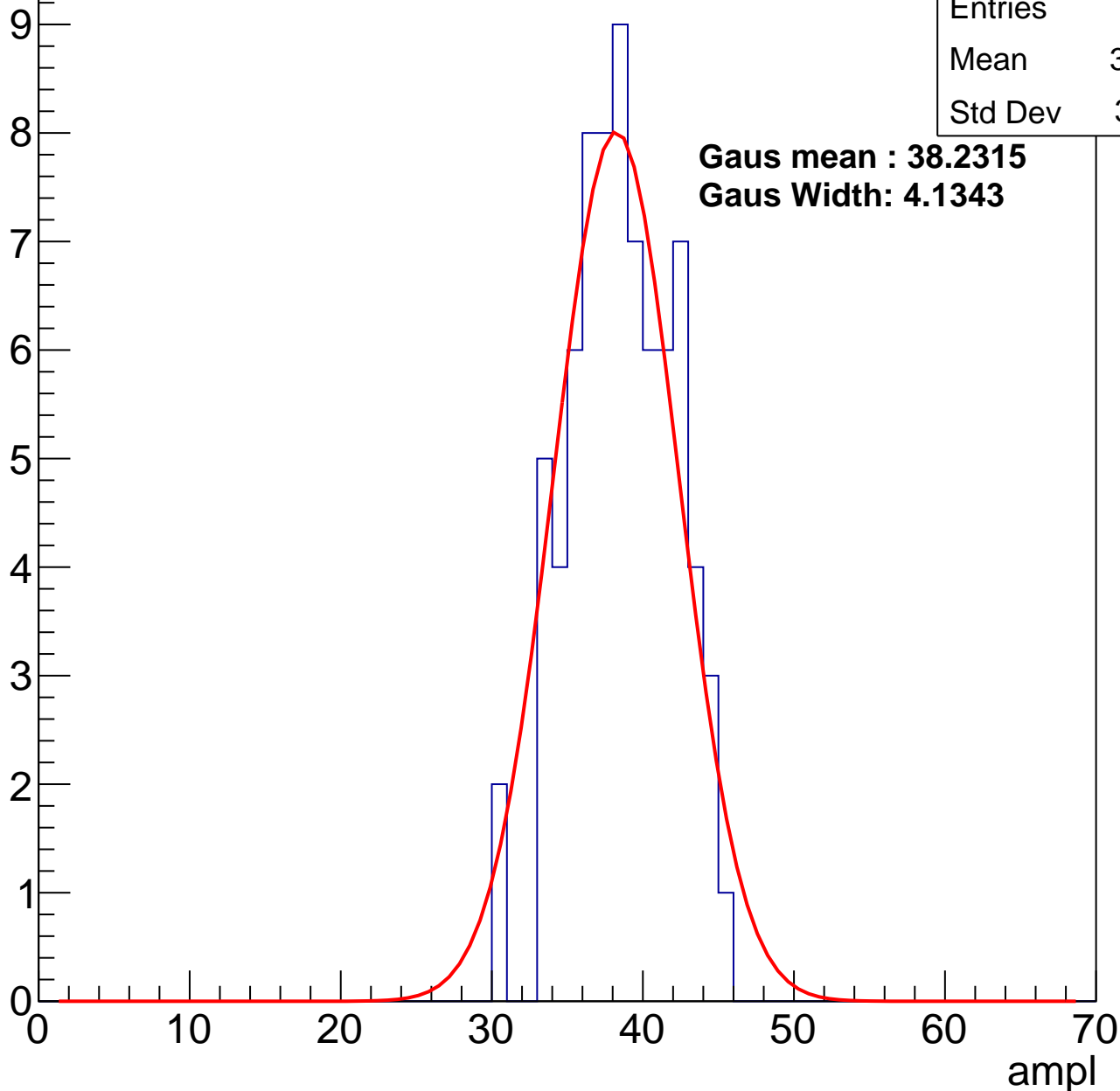
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	76
Mean	38.14
Std Dev	3.371

**Gaus mean : 38.2315**

**Gaus Width: 4.1343**



# B0L000S, U7-ch83, adc2

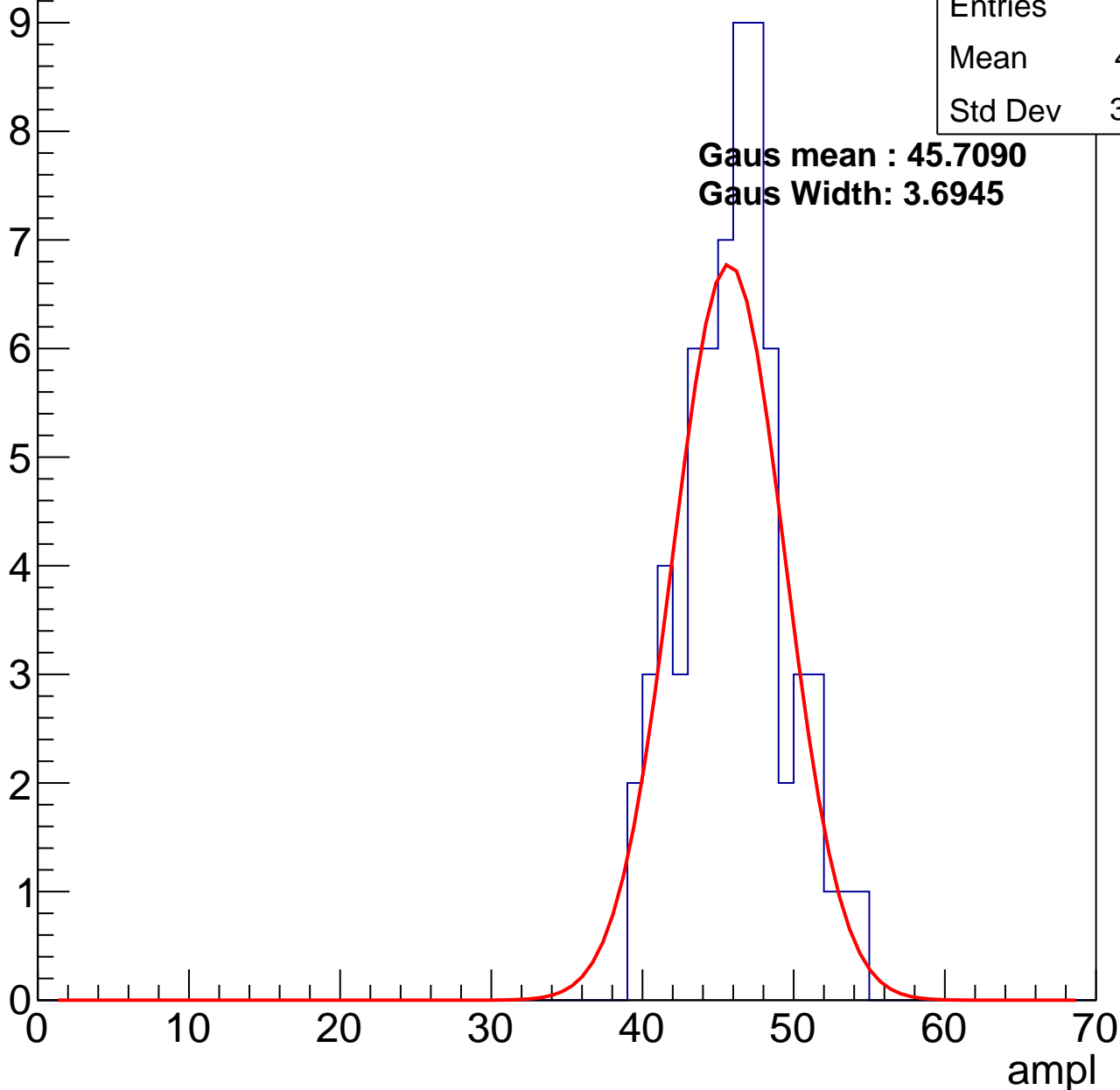
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	66
Mean	45.61
Std Dev	3.375

**Gaus mean : 45.7090**

**Gaus Width: 3.6945**

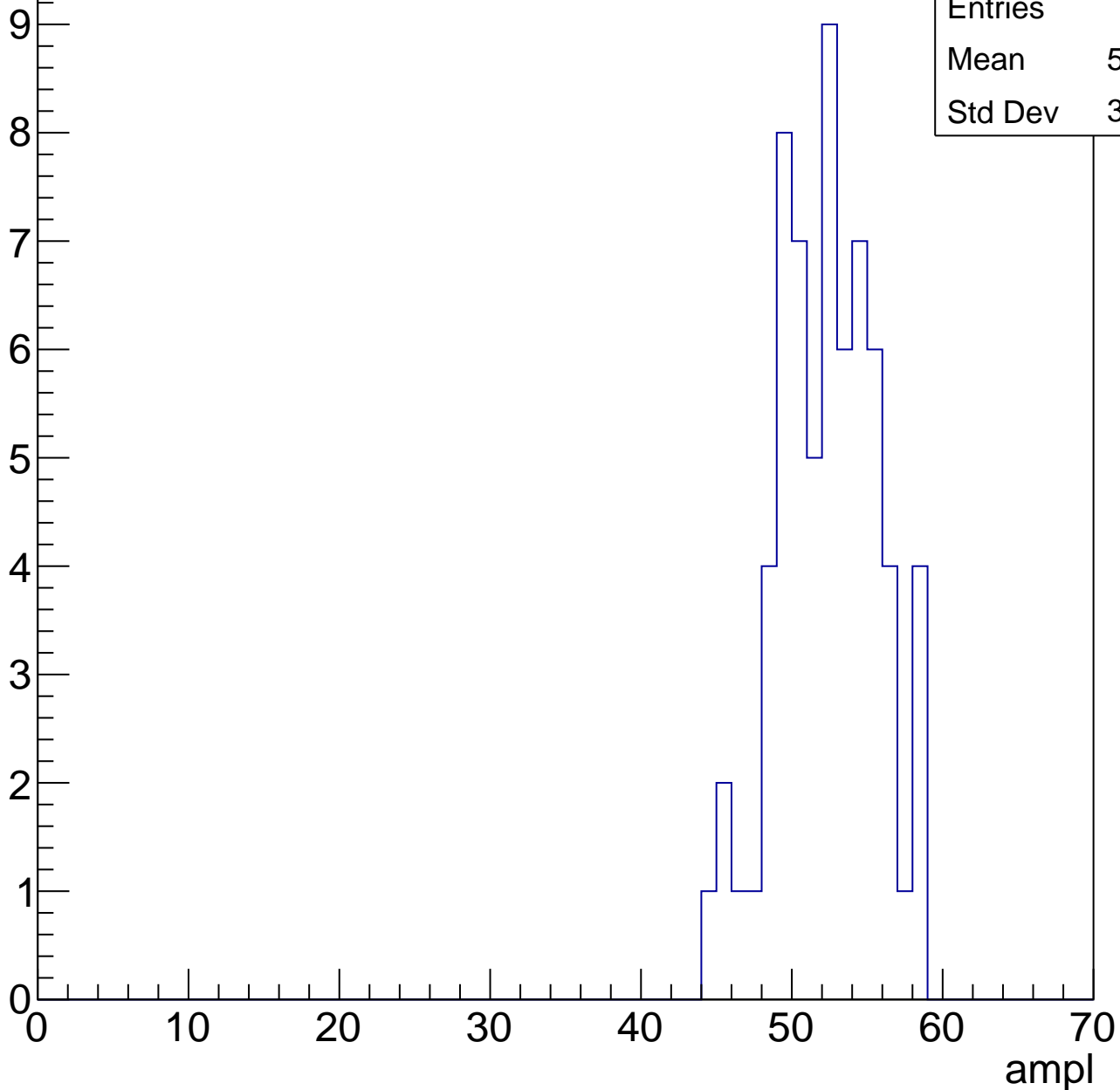


# B0L000S, U7-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	66
Mean	51.86
Std Dev	3.284

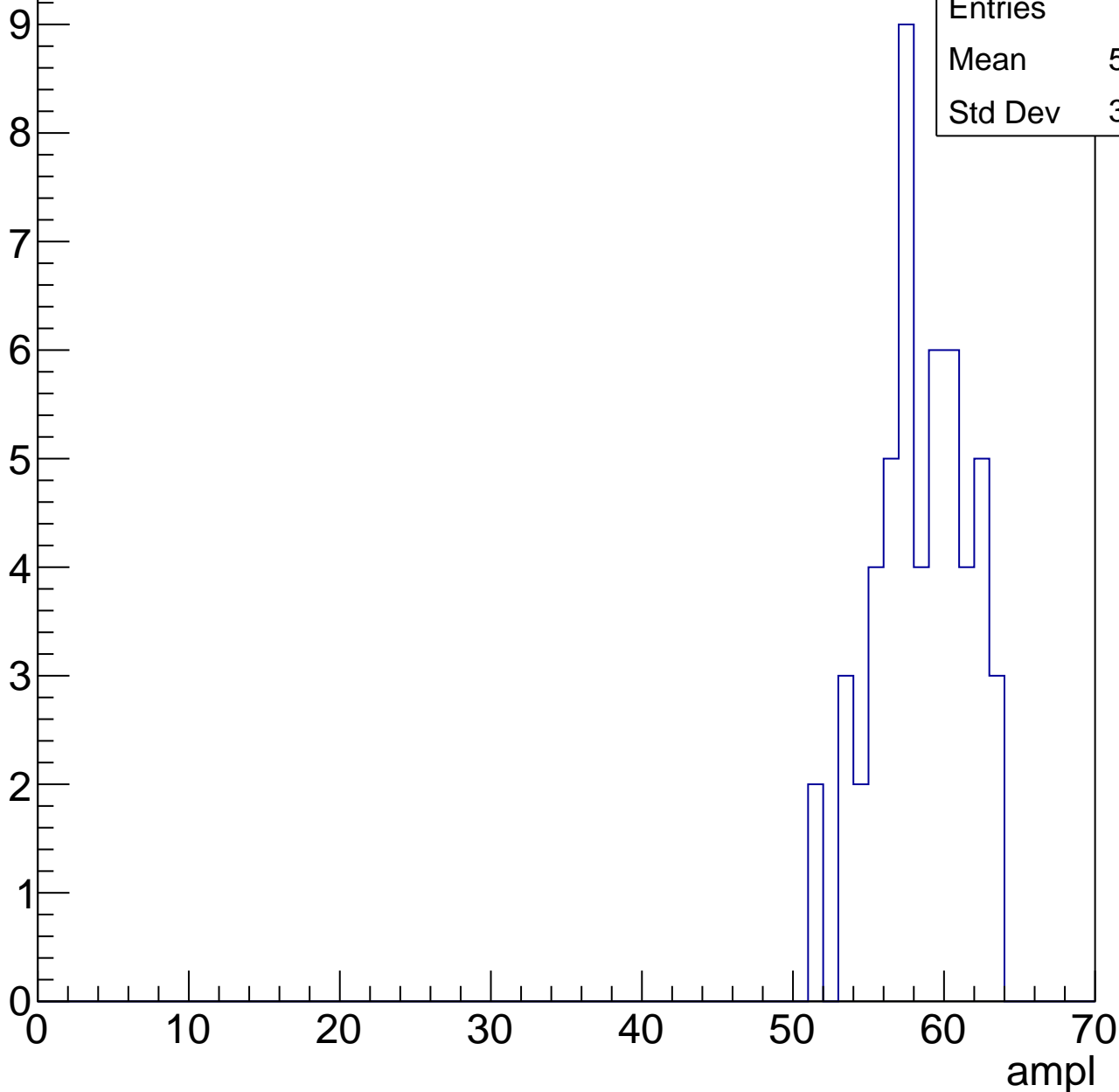


# B0L000S, U7-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	53
Mean	57.94
Std Dev	3.043

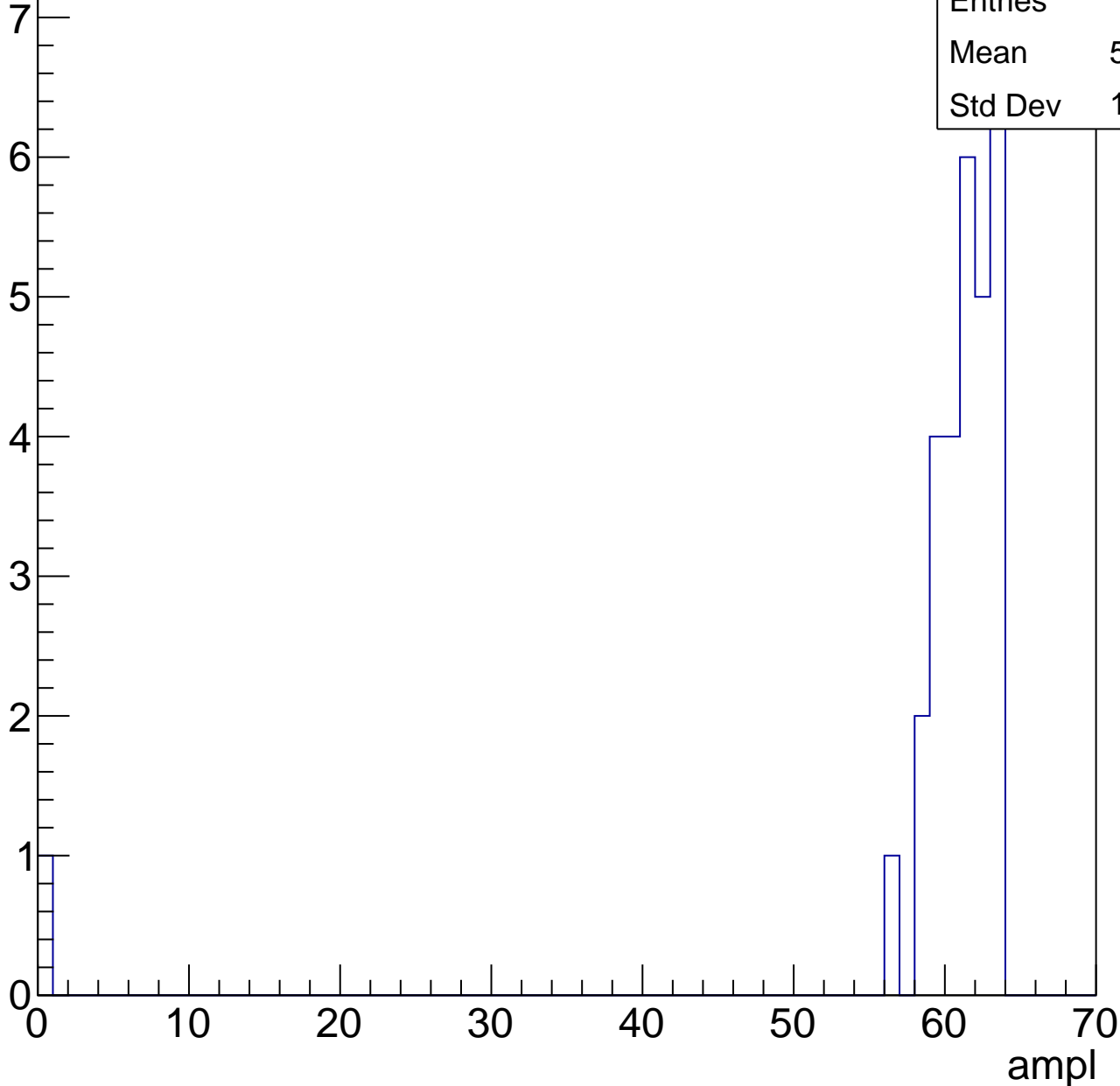


# B0L000S, U7-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	30
Mean	58.83
Std Dev	11.07



# B0L000S, U7-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L000S, U7-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	2
Mean	11
Std Dev	11

# B0L000S, U7-ch84, adc0

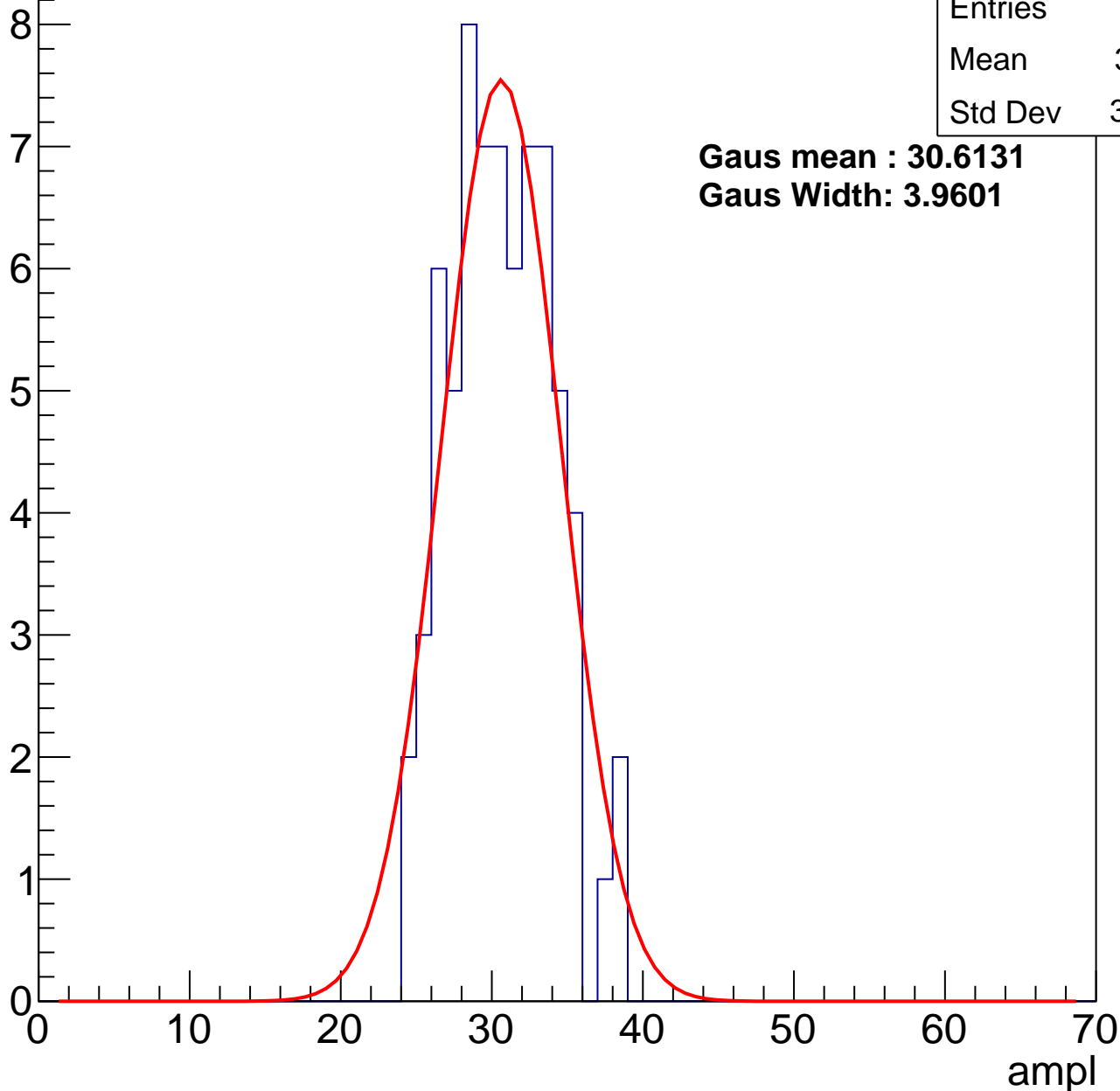
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	70
Mean	30.21
Std Dev	3.333

**Gaus mean : 30.6131**

**Gaus Width: 3.9601**



# B0L000S, U7-ch84, adc1

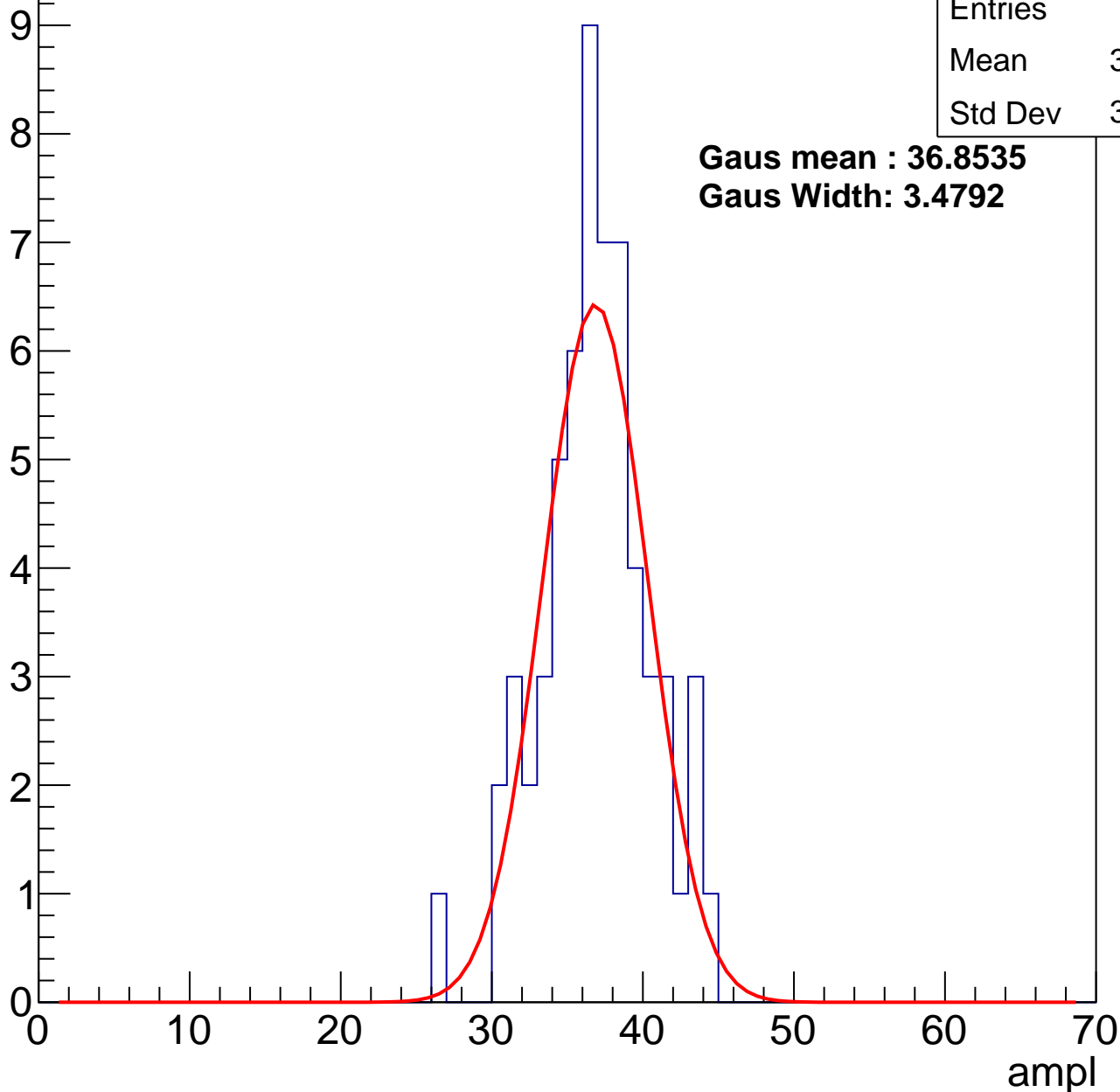
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	60
Mean	36.42
Std Dev	3.565

**Gaus mean : 36.8535**

**Gaus Width: 3.4792**



# B0L000S, U7-ch84, adc2

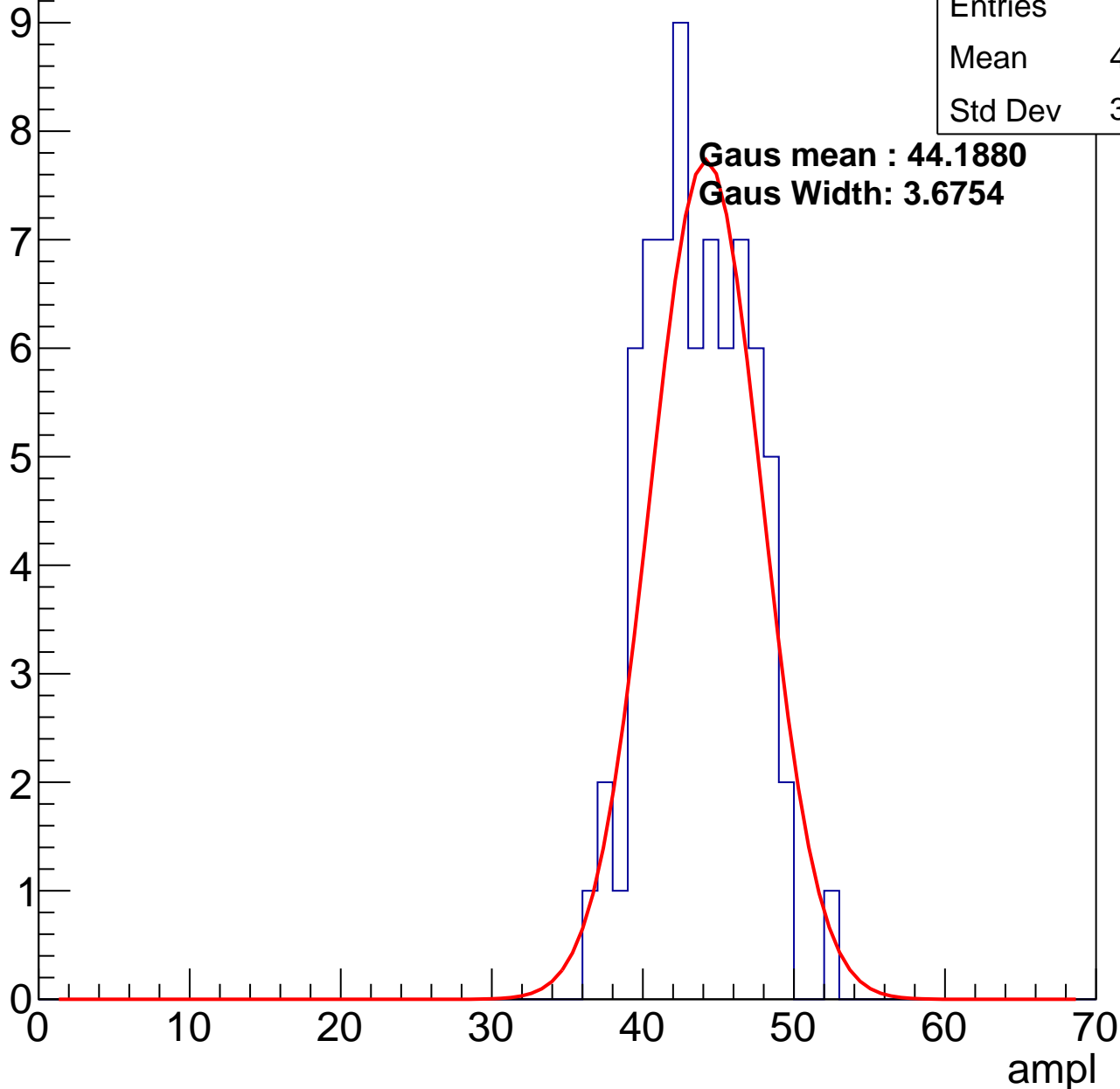
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	73
Mean	43.25
Std Dev	3.322

**Gaus mean : 44.1880**

**Gaus Width: 3.6754**

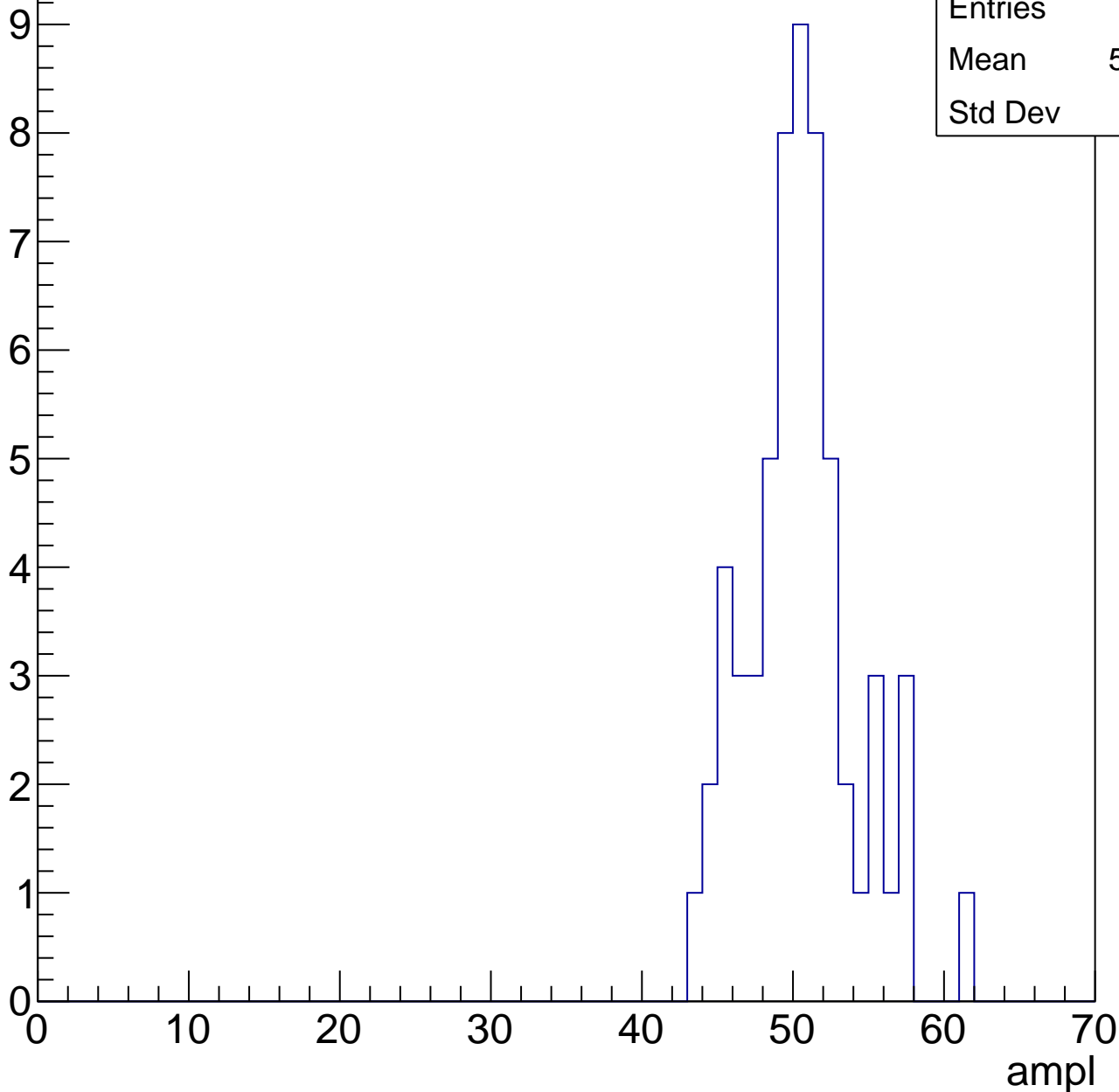


# B0L000S, U7-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	59
Mean	50.05
Std Dev	3.6

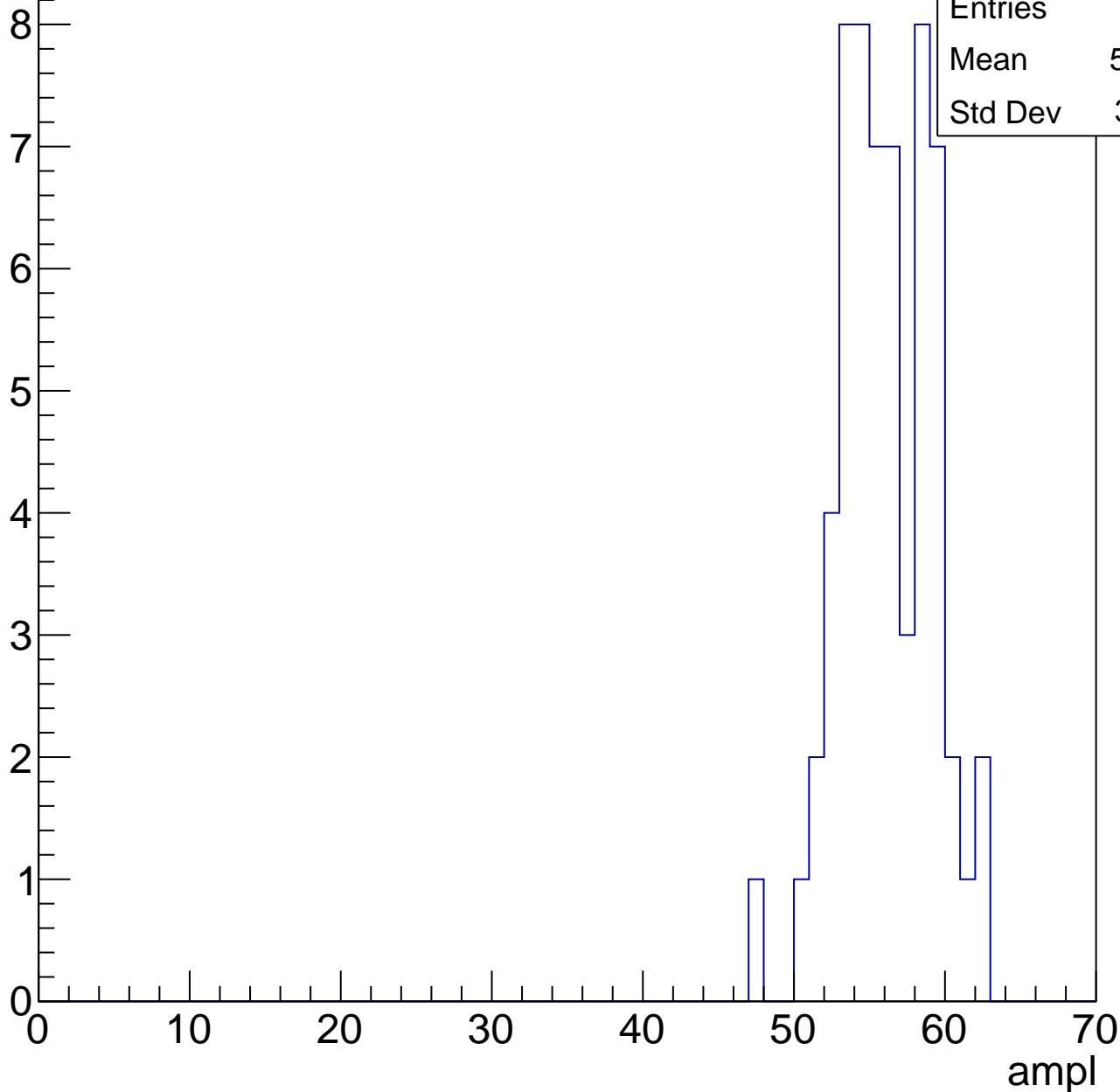


# B0L000S, U7-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	61
Mean	55.62
Std Dev	3.031



# B0L000S, U7-ch84, adc5

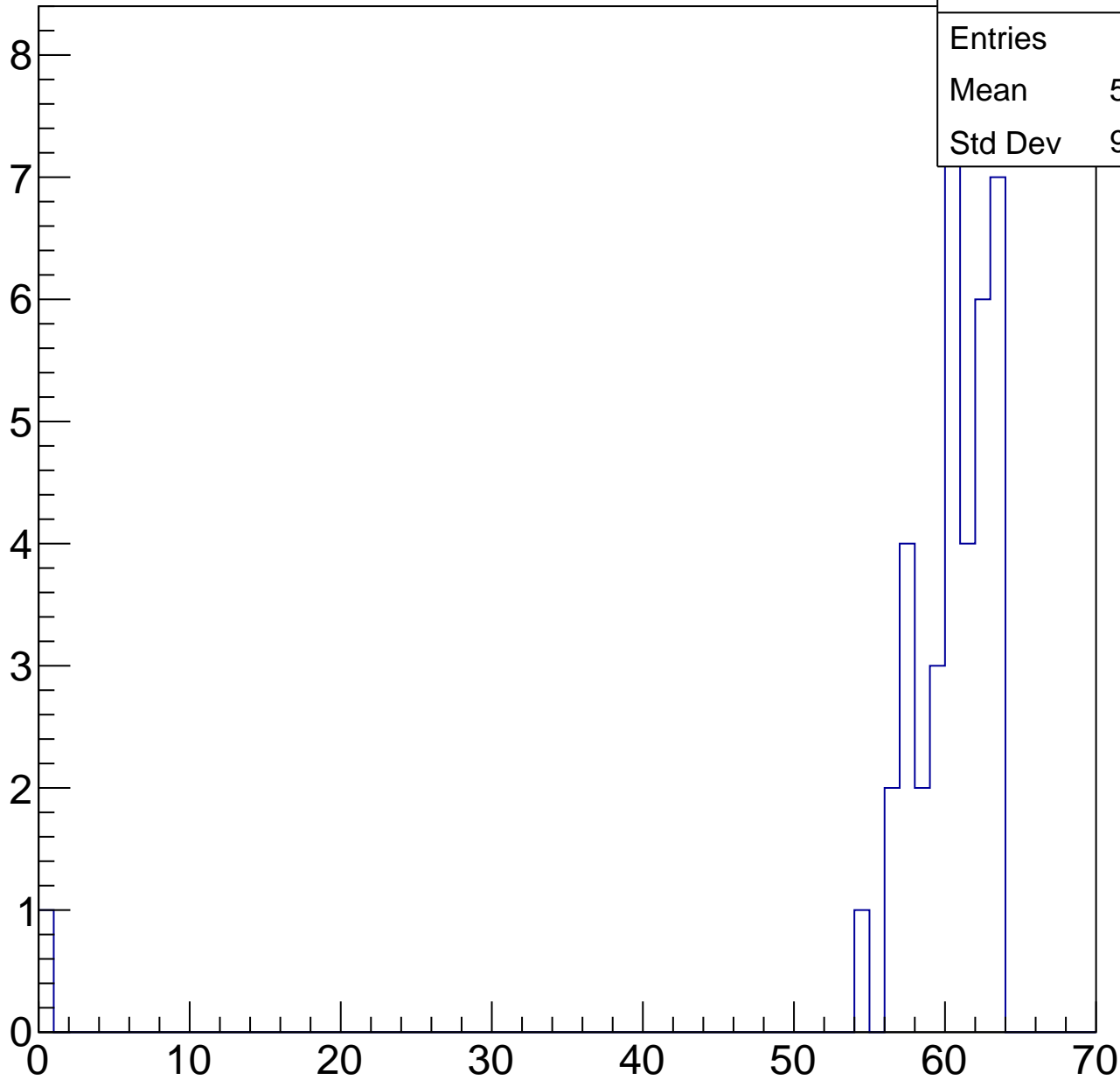
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	38
Mean	58.53
Std Dev	9.899

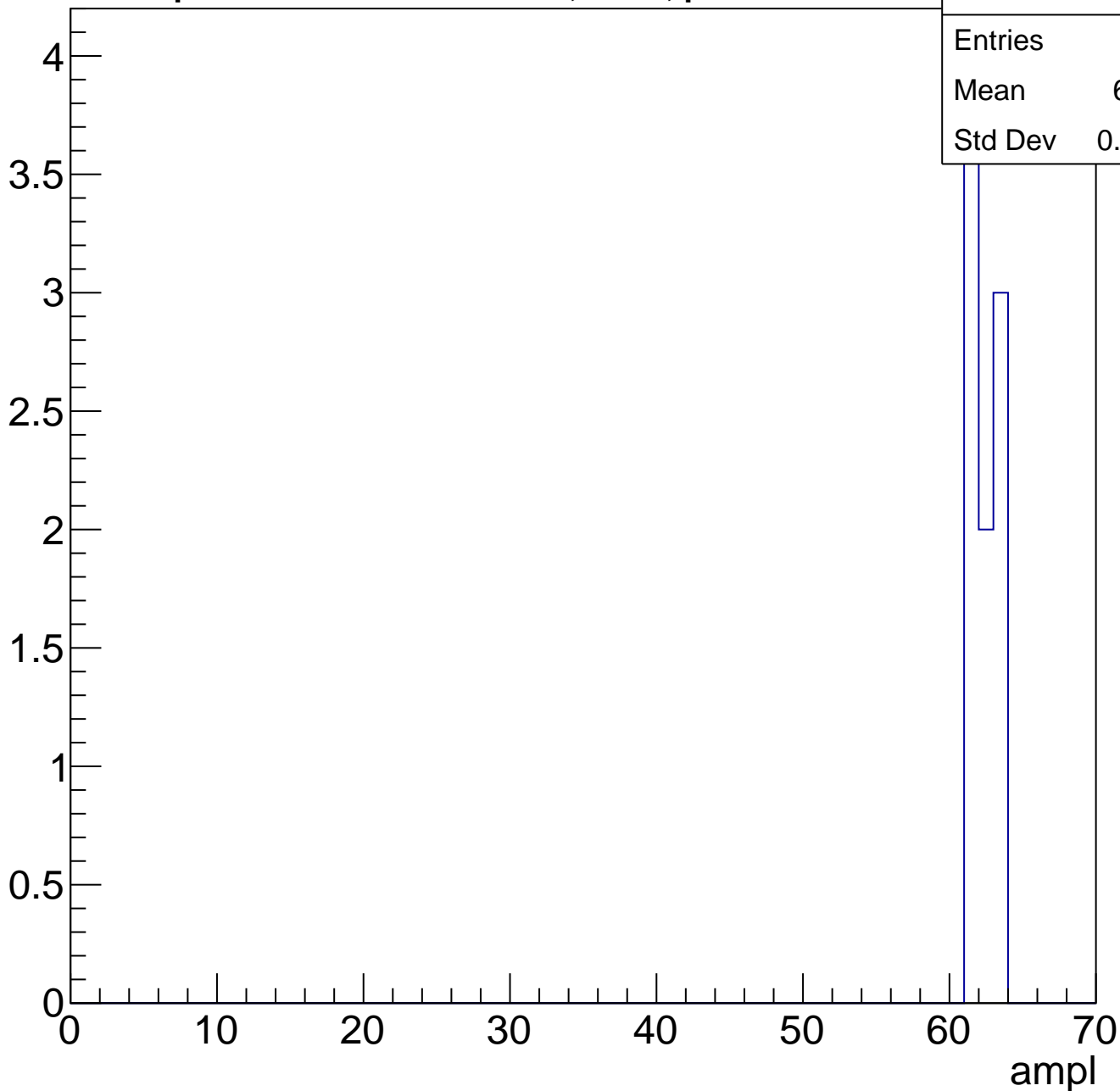
ampl



# B0L000S, U7-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch85, adc0

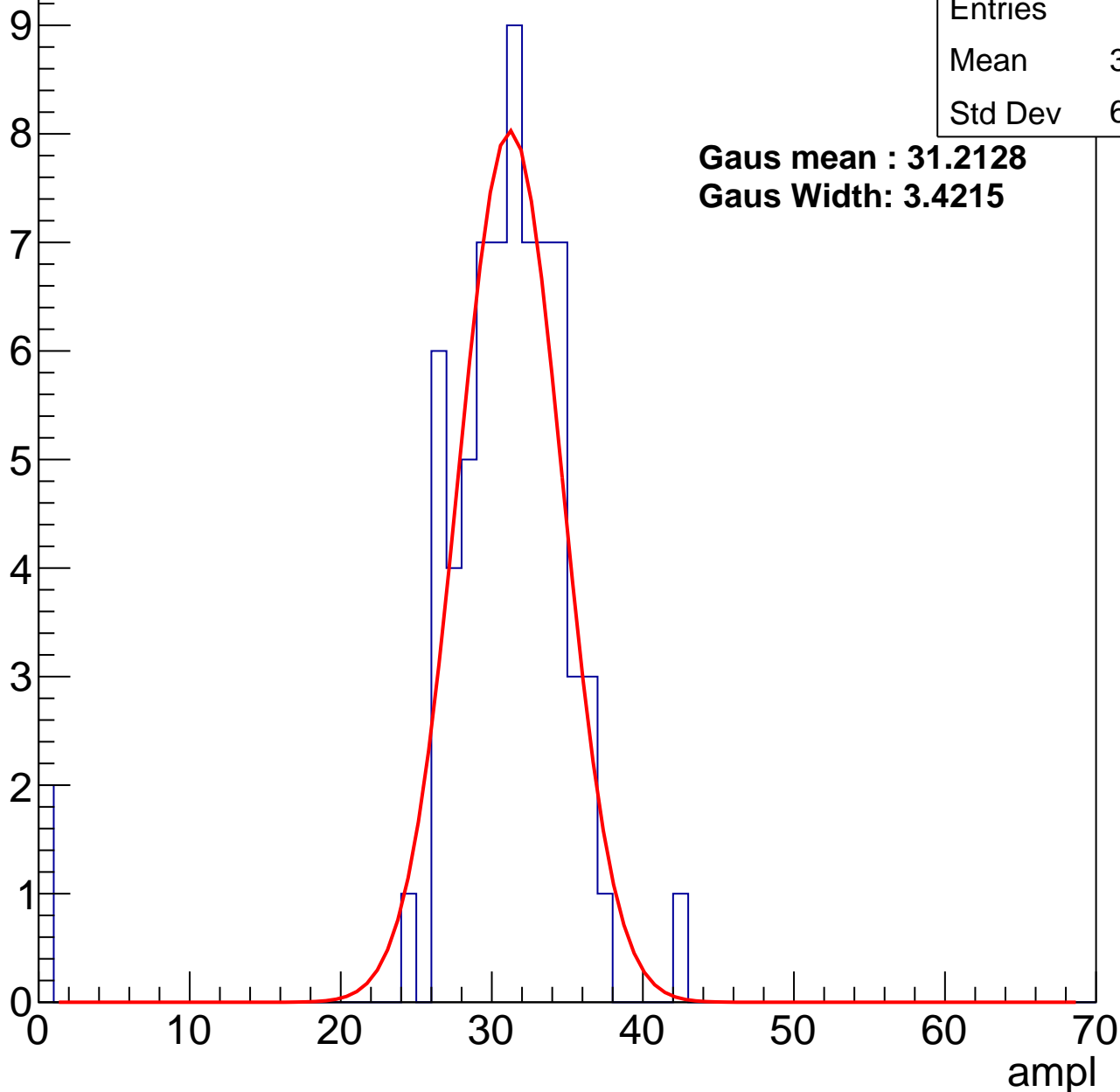
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	70
Mean	30.07
Std Dev	6.074

**Gaus mean : 31.2128**

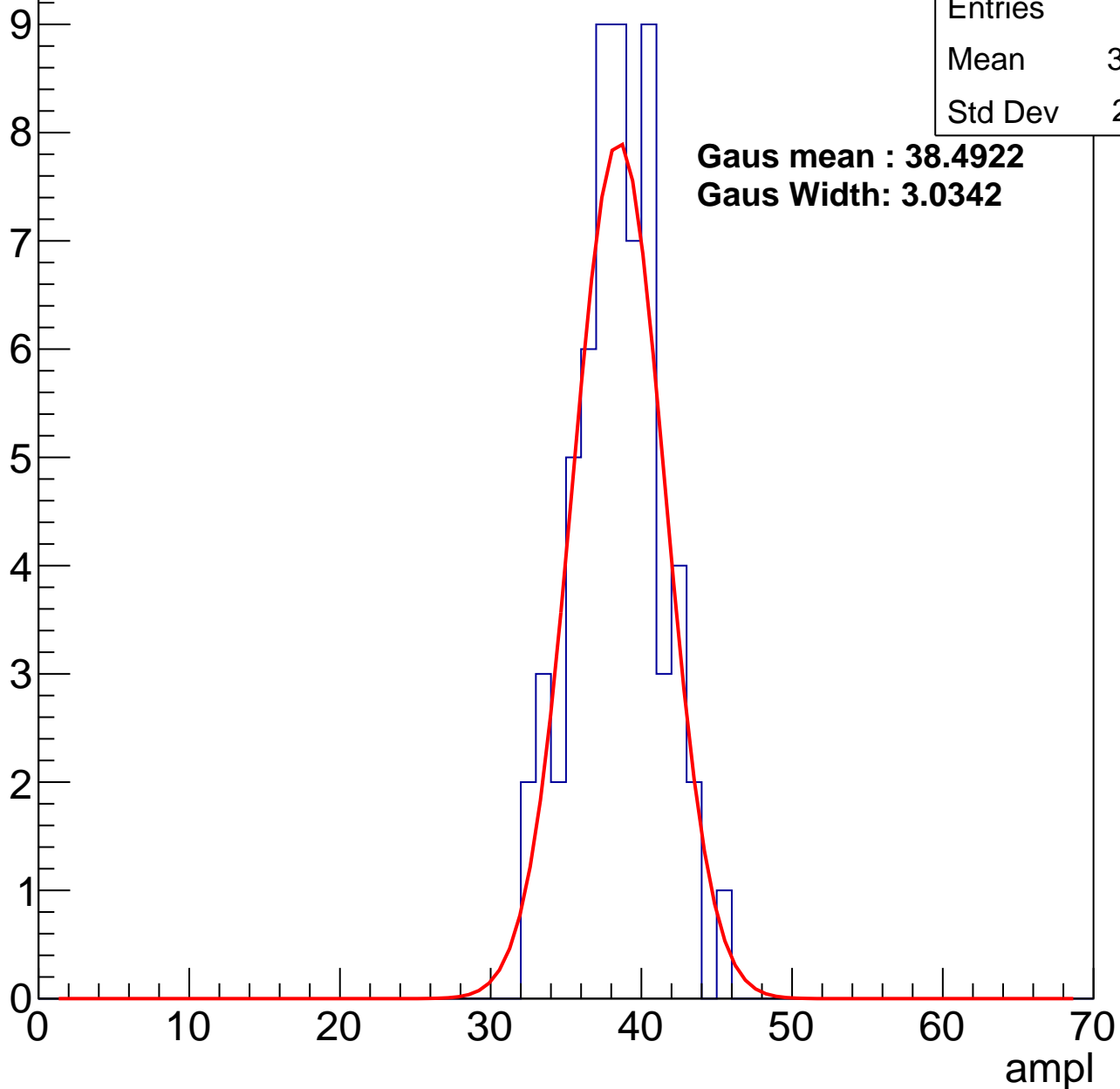
**Gaus Width: 3.4215**



# B0L000S, U7-ch85, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch85, adc2

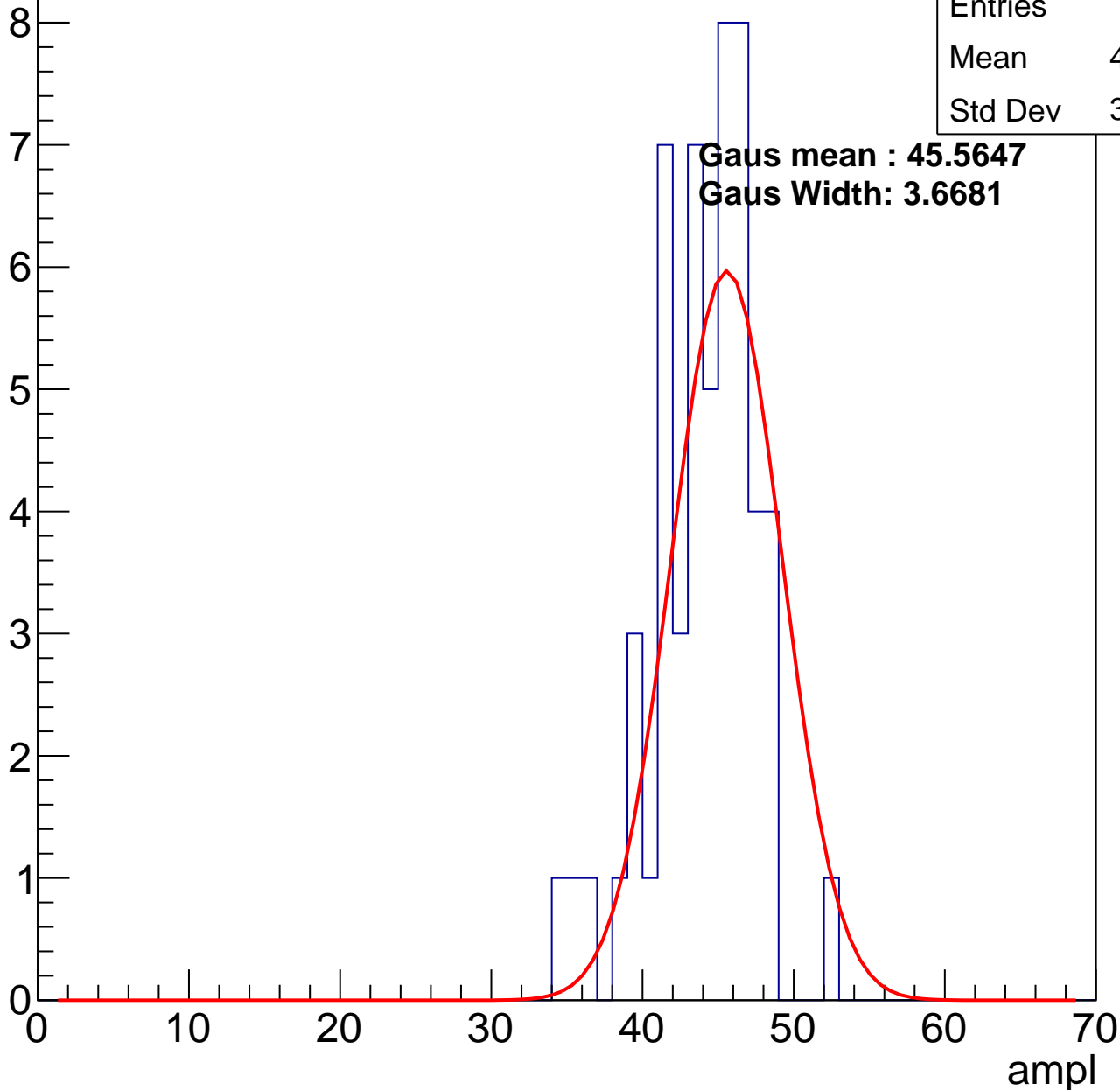
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	55
Mean	43.53
Std Dev	3.426

**Gaus mean : 45.5647**

**Gaus Width: 3.6681**

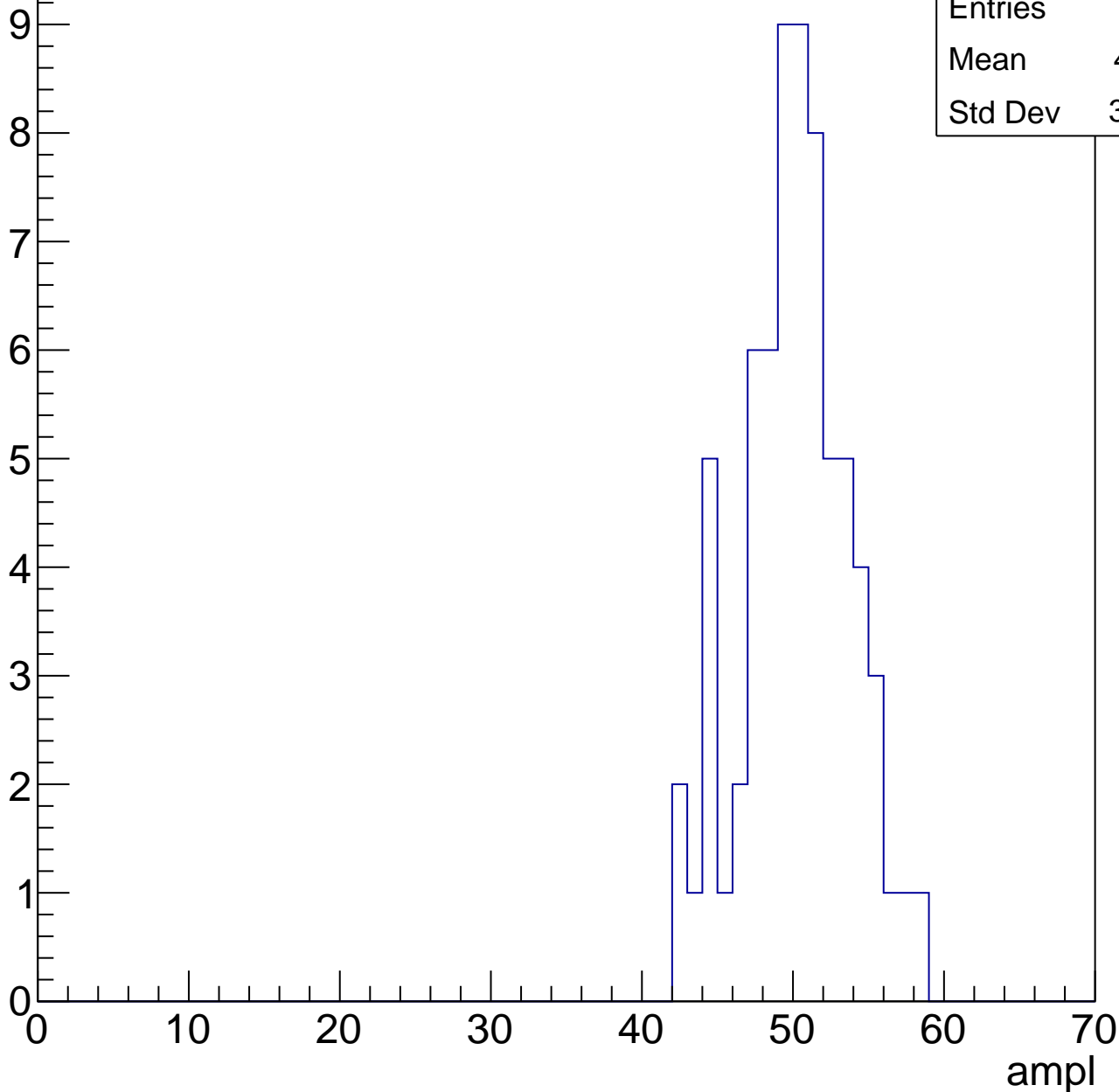


# B0L000S, U7-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	69
Mean	49.71
Std Dev	3.523

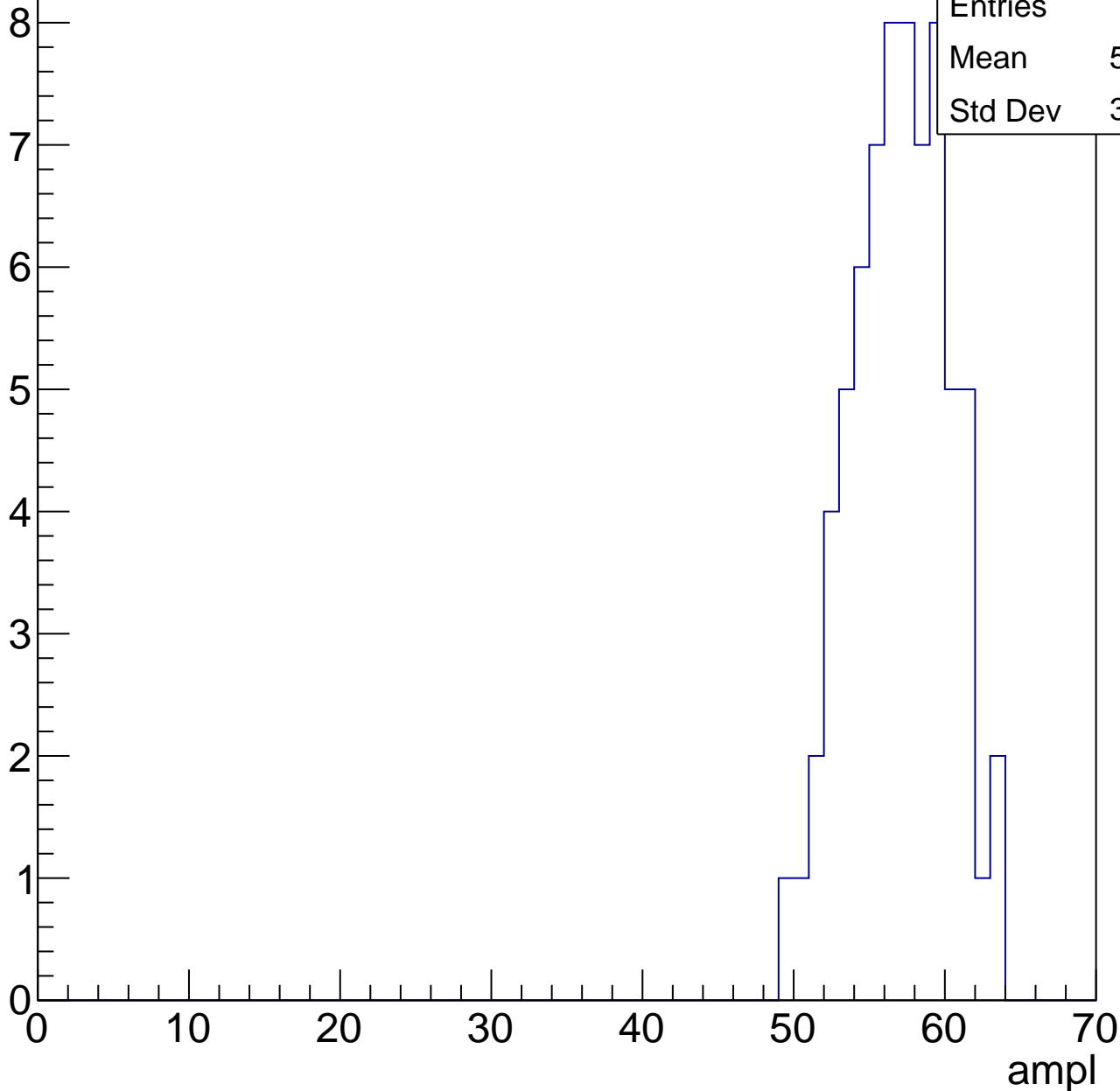


# B0L000S, U7-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

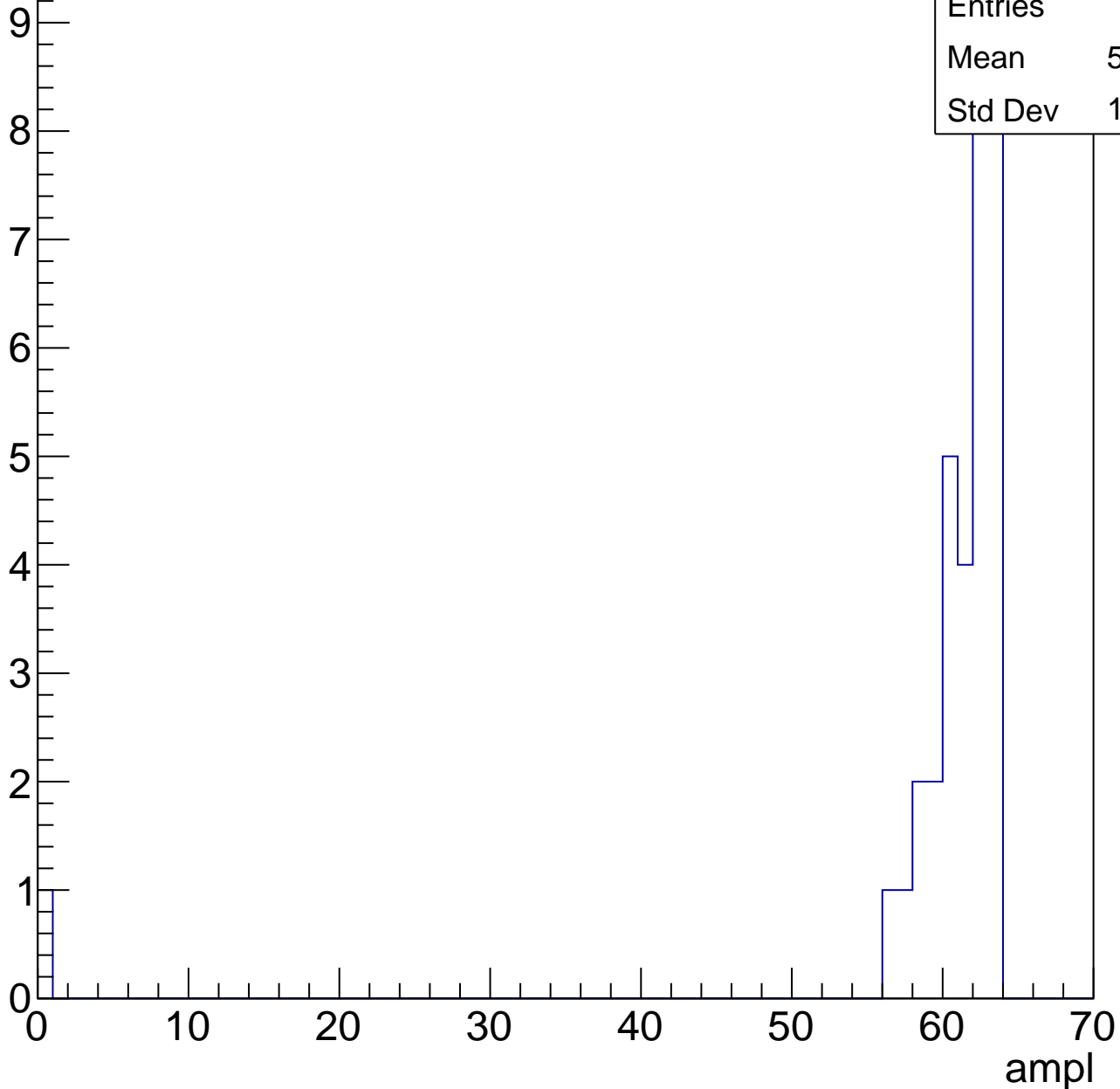
Entries	70
Mean	56.54
Std Dev	3.165



# B0L000S, U7-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L000S, U7-ch86, adc0

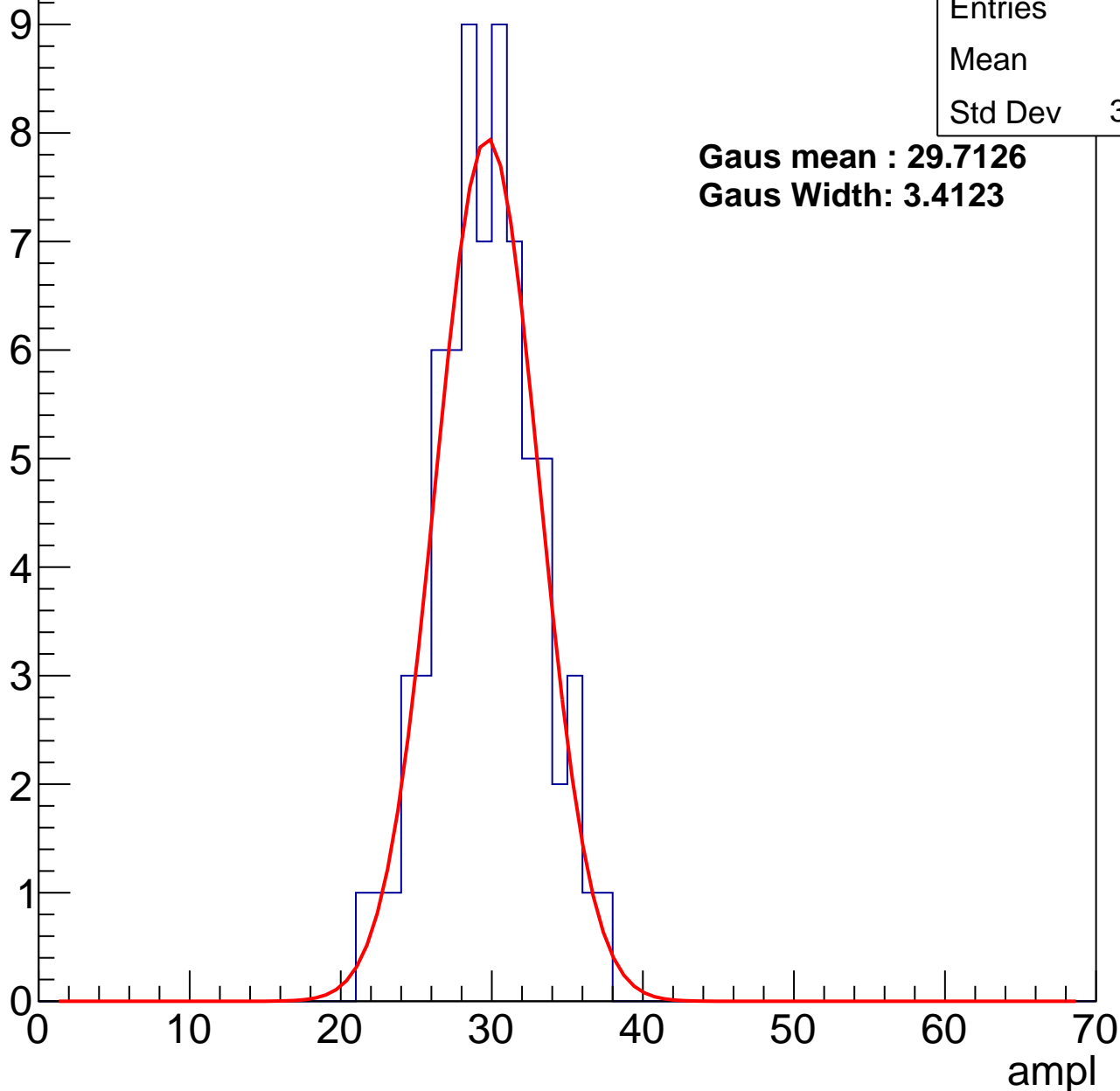
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	70
Mean	29.2
Std Dev	3.358

**Gaus mean : 29.7126**

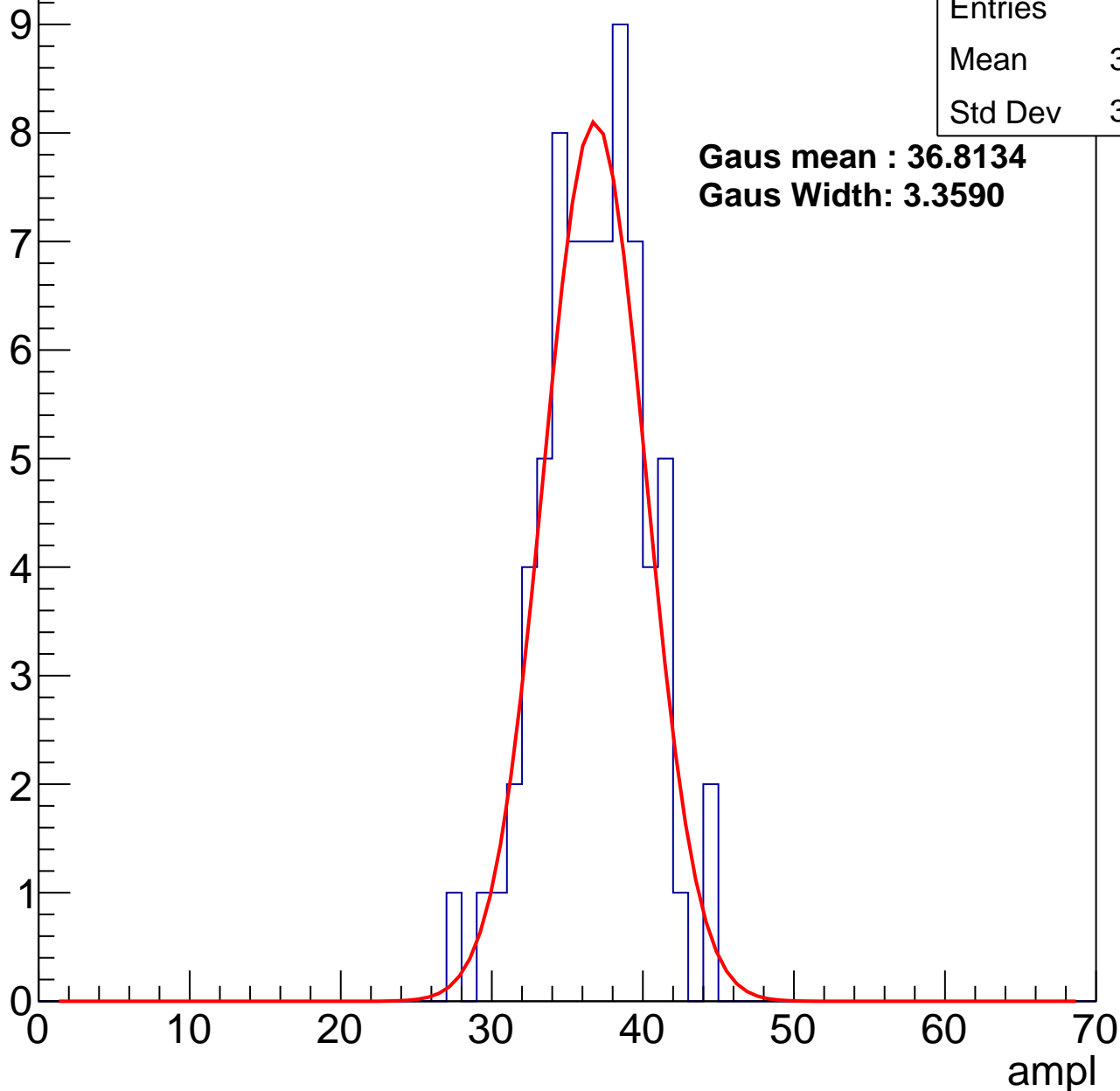
**Gaus Width: 3.4123**



# B0L000S, U7-ch86, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch86, adc2

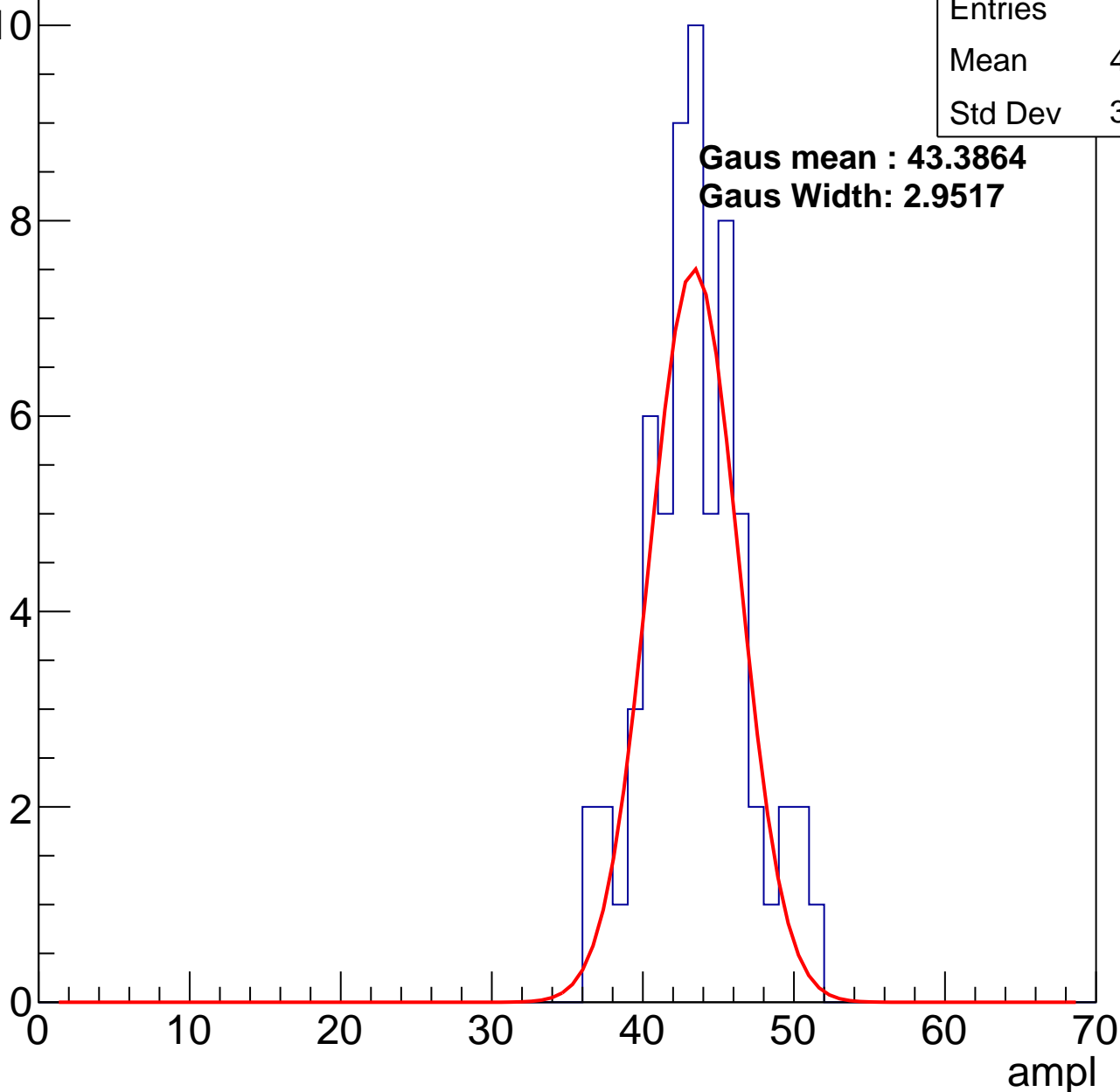
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	64
Mean	43.05
Std Dev	3.304

**Gaus mean : 43.3864**

**Gaus Width: 2.9517**

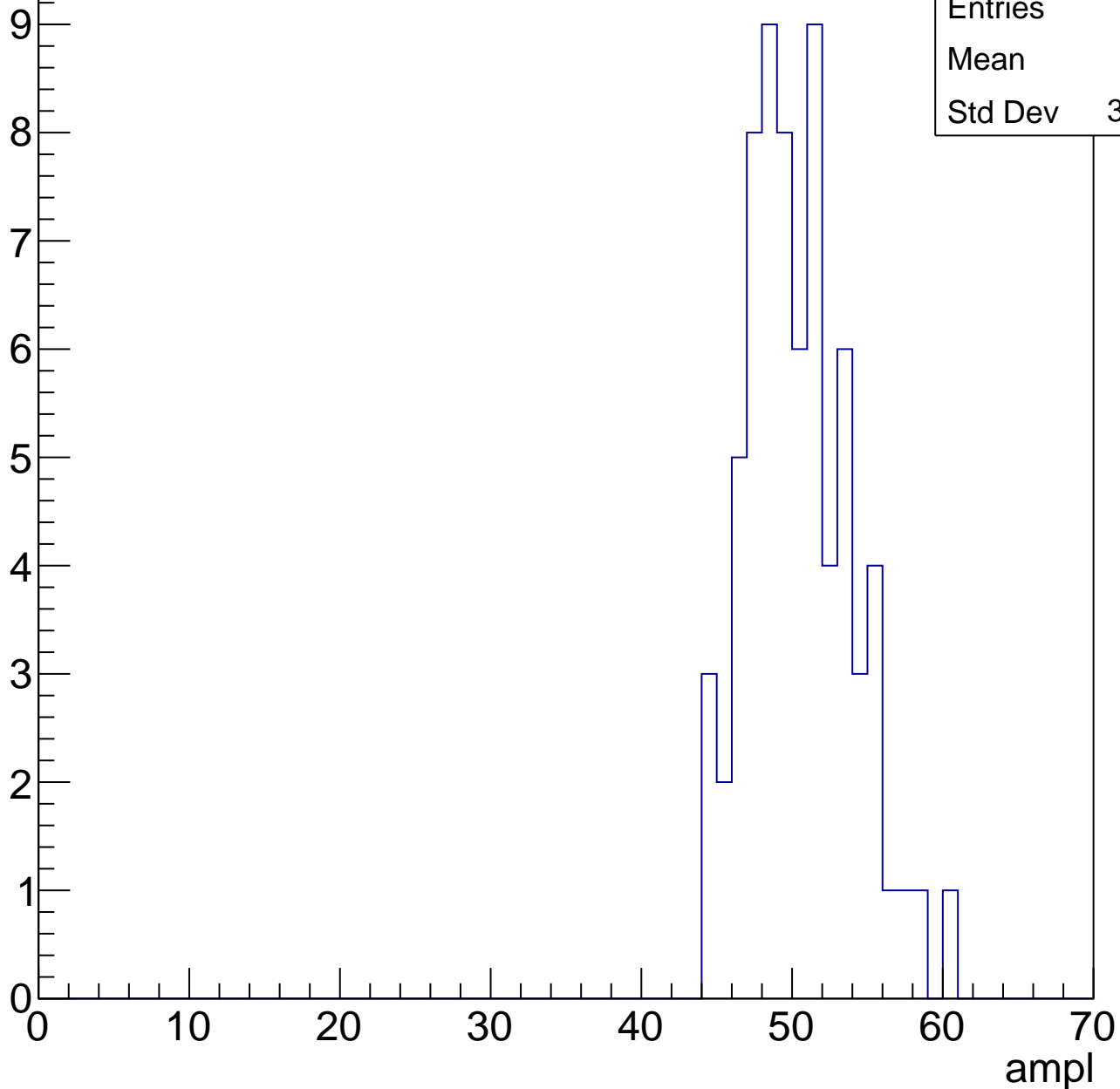


# B0L000S, U7-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	71
Mean	50
Std Dev	3.419

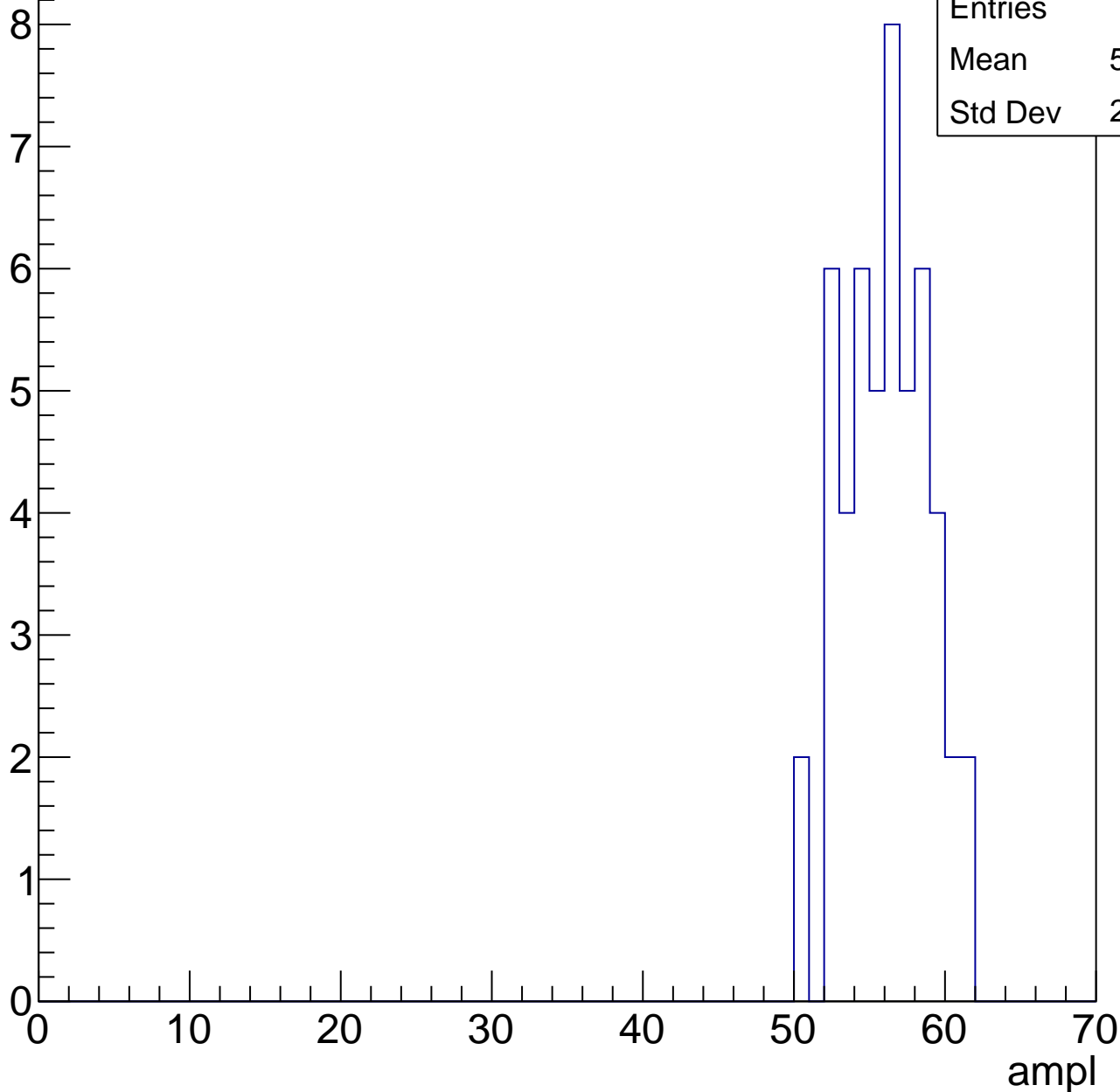


# B0L000S, U7-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	50
Mean	55.64
Std Dev	2.733

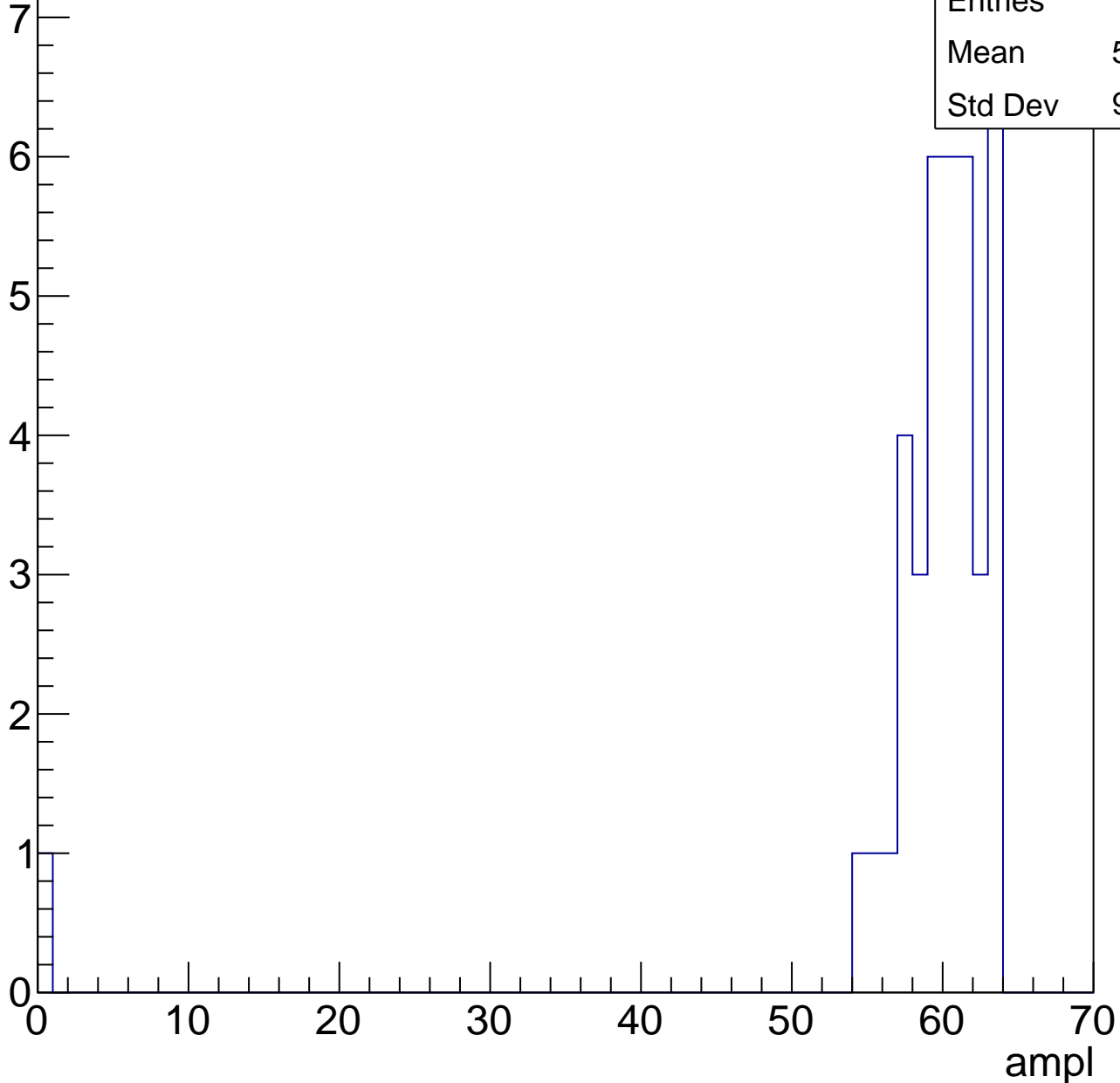


# B0L000S, U7-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	39
Mean	58.31
Std Dev	9.741

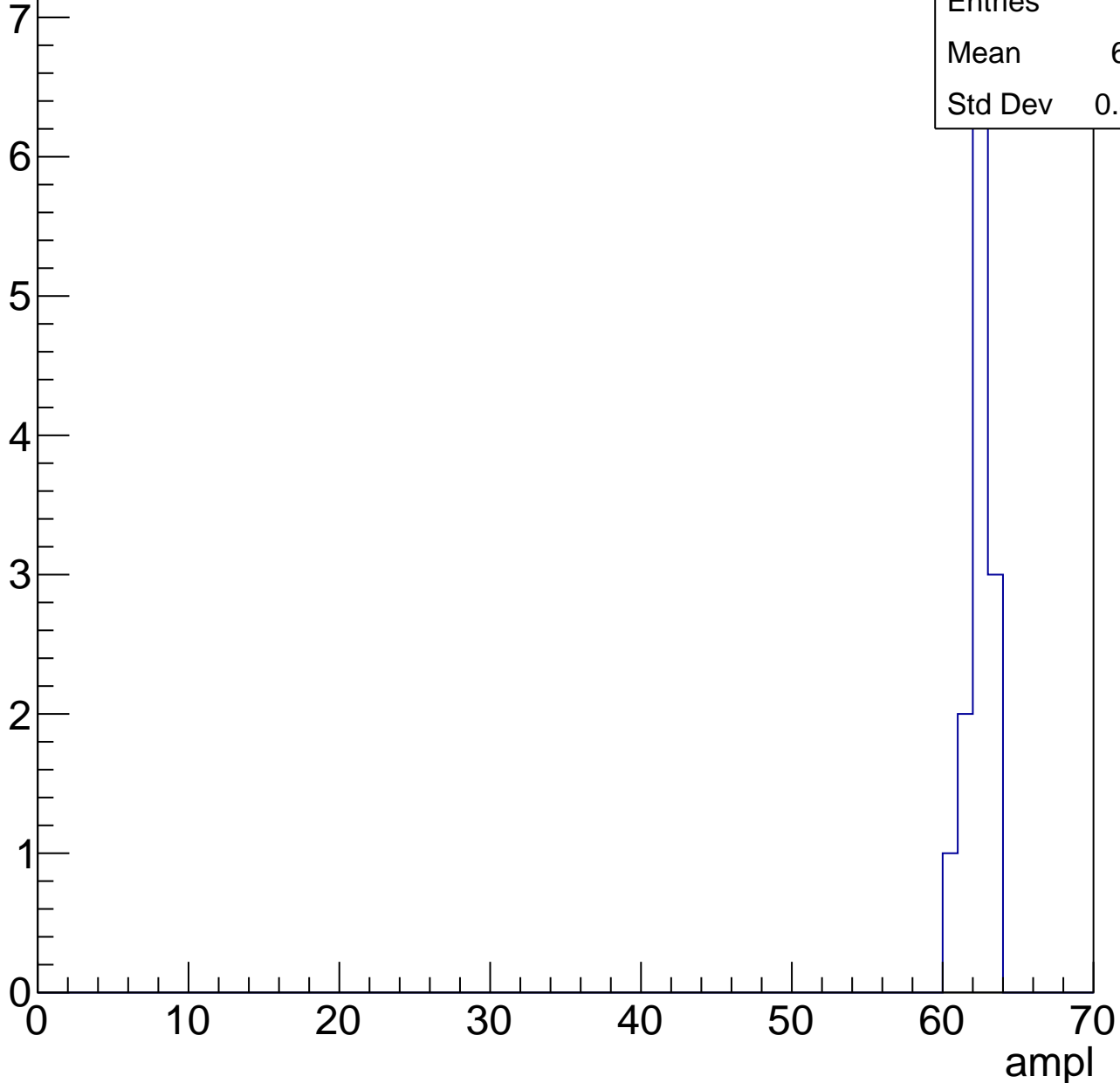


# B0L000S, U7-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	13
Mean	61.92
Std Dev	0.8285

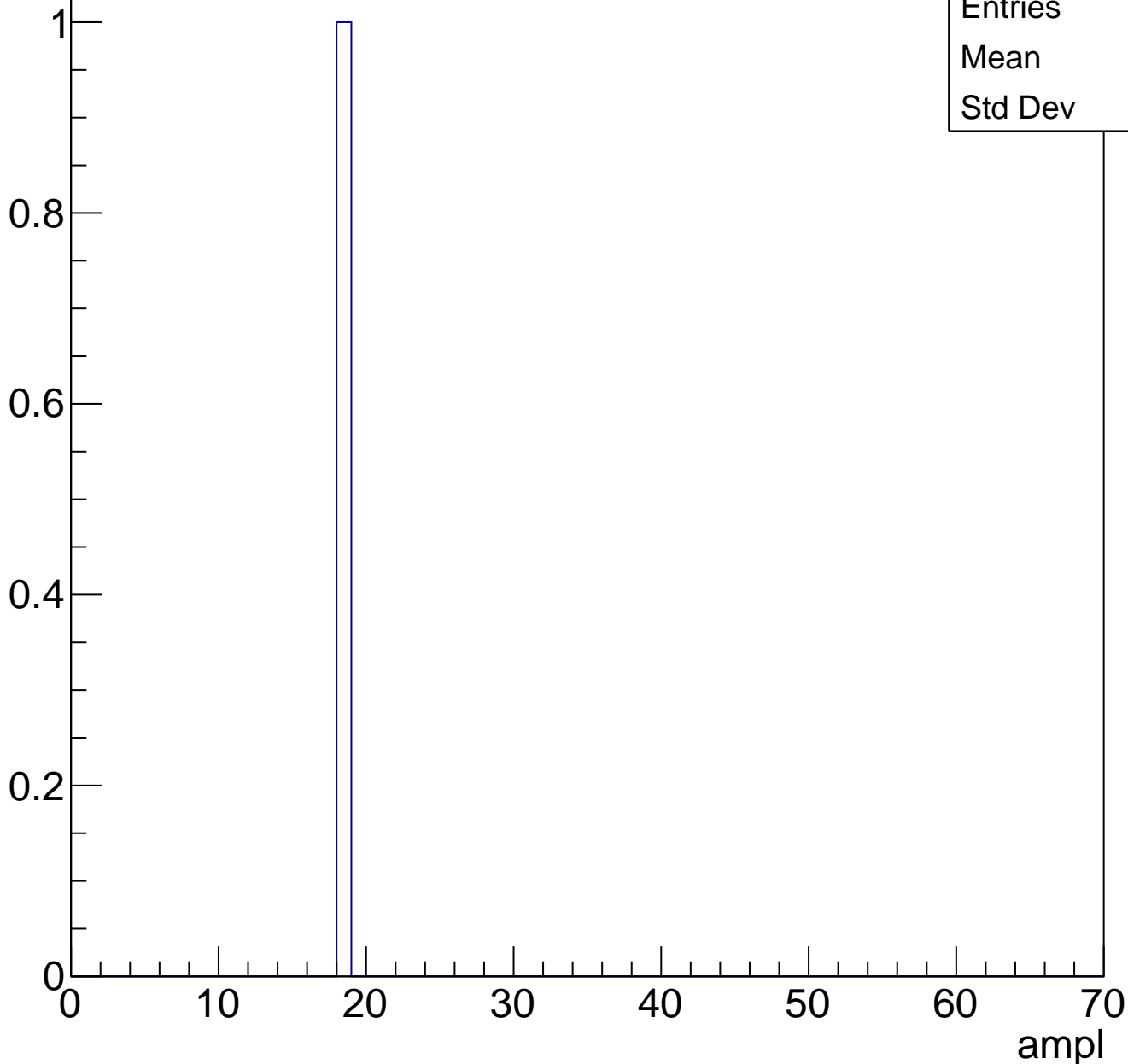




# B0L000S, U7-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch87, adc0

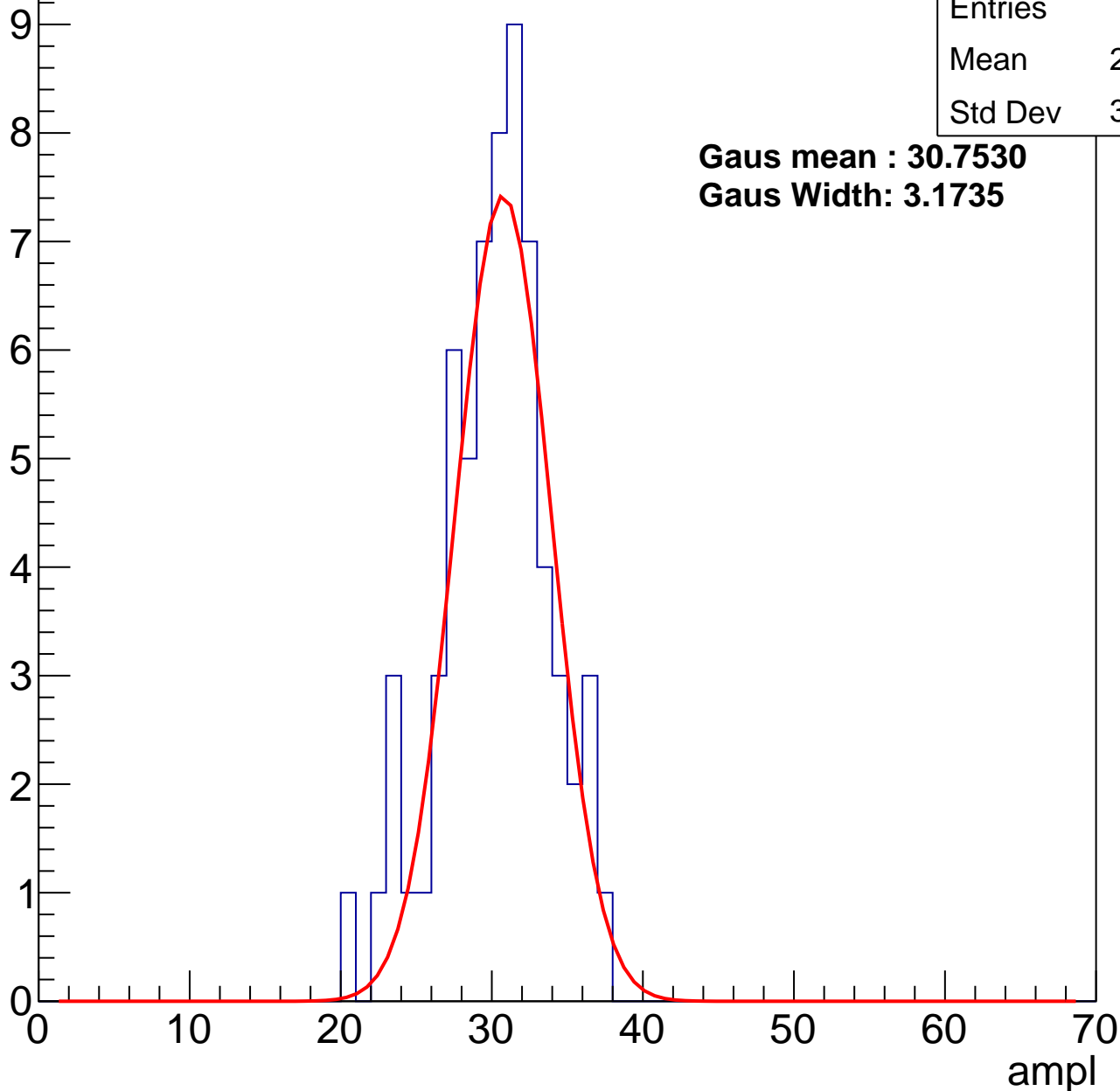
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	65
Mean	29.77
Std Dev	3.564

**Gaus mean : 30.7530**

**Gaus Width: 3.1735**



# B0L000S, U7-ch87, adc1

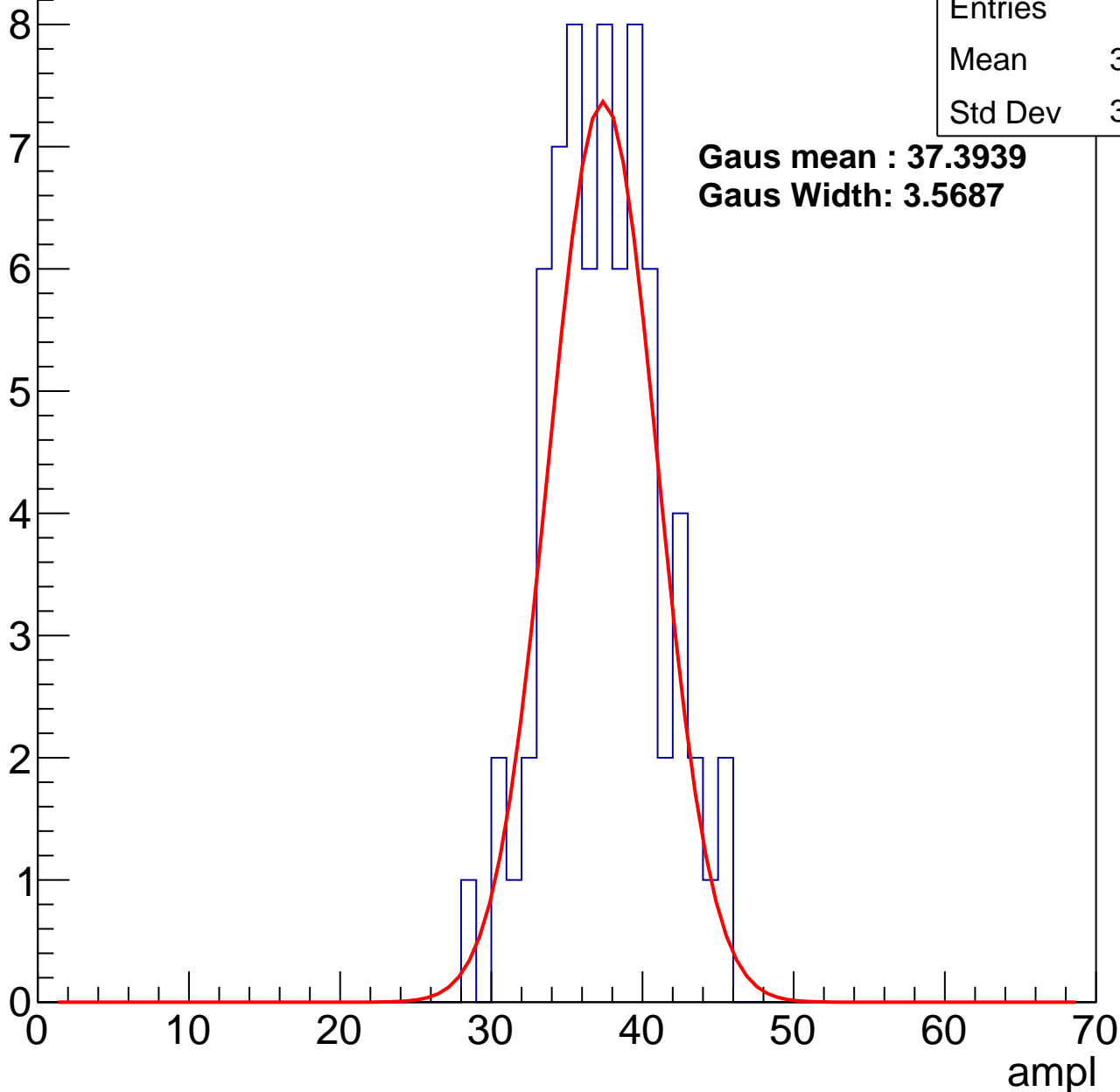
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	72
Mean	36.96
Std Dev	3.603

**Gaus mean : 37.3939**

**Gaus Width: 3.5687**



# B0L000S, U7-ch87, adc2

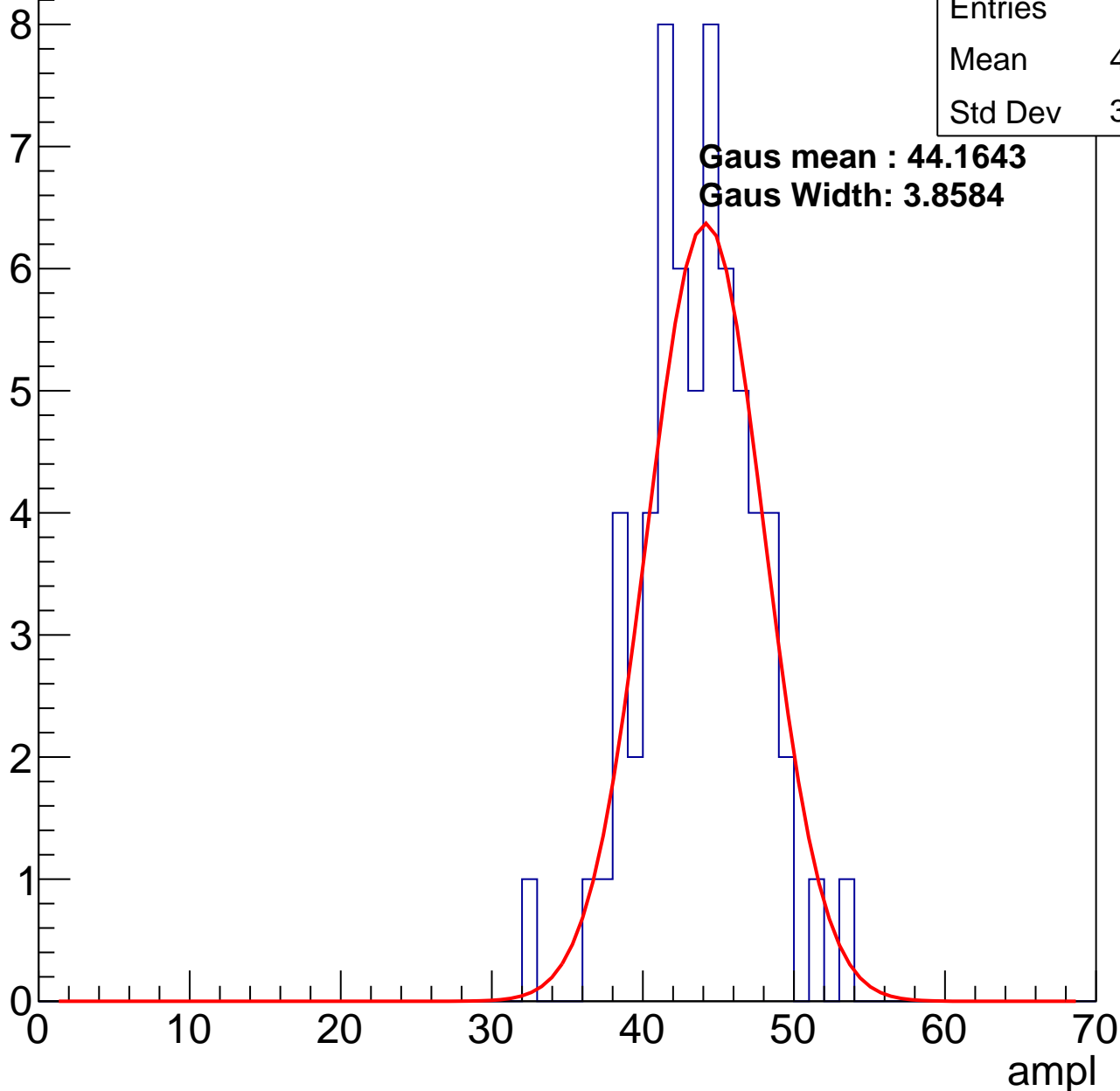
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	63
Mean	43.24
Std Dev	3.749

**Gaus mean : 44.1643**

**Gaus Width: 3.8584**

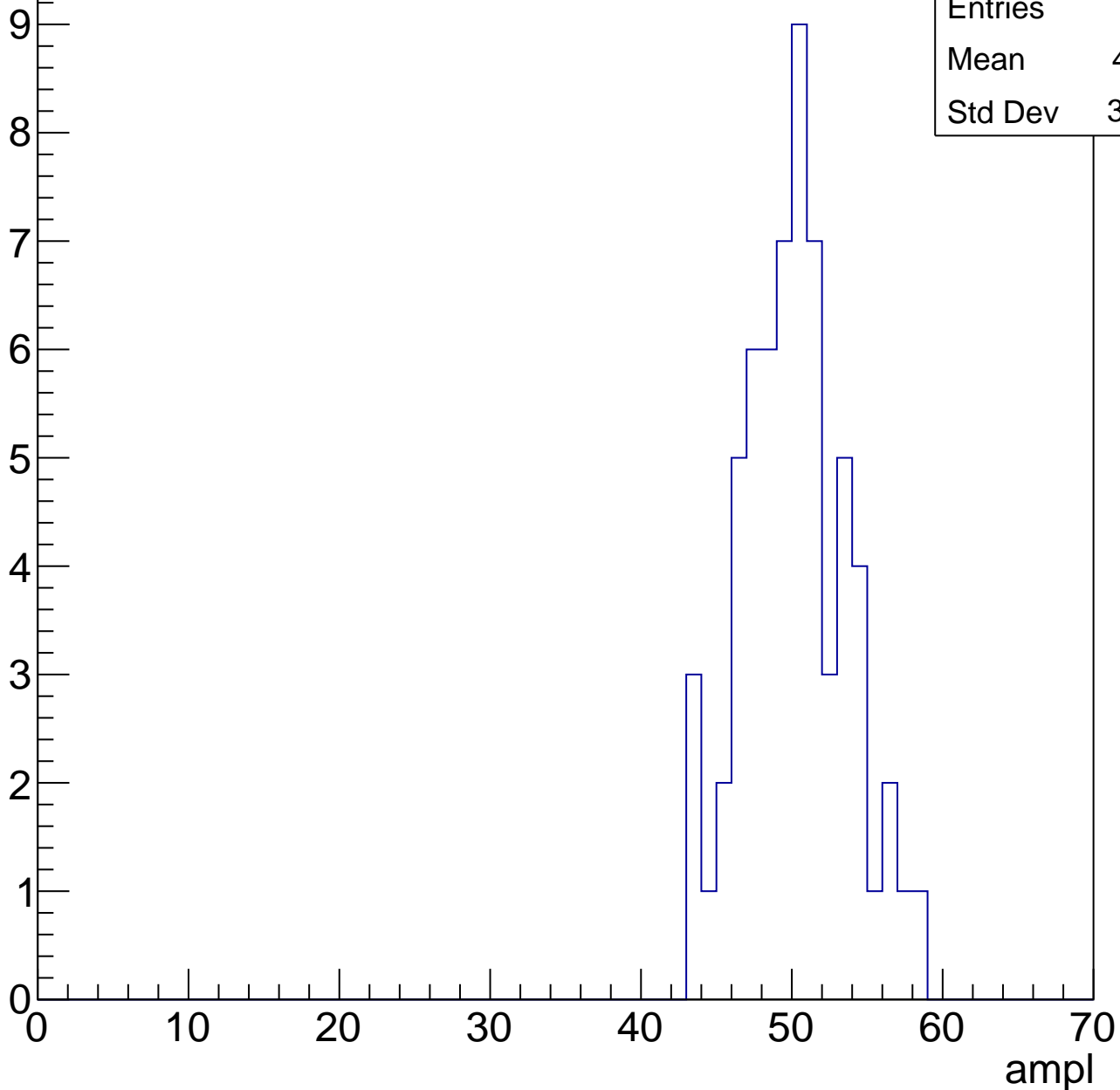


# B0L000S, U7-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	63
Mean	49.71
Std Dev	3.406

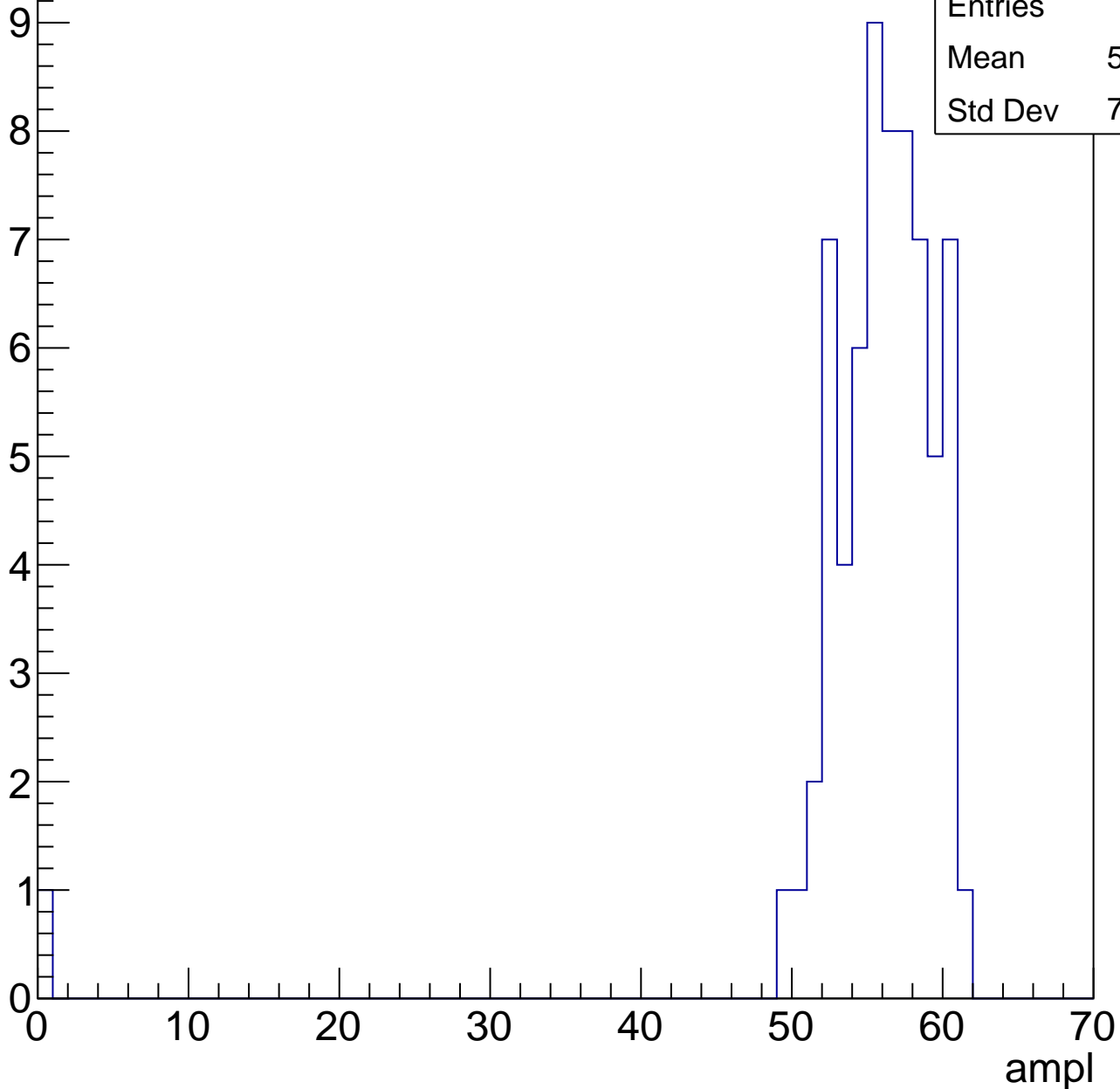


# B0L000S, U7-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	67
Mean	54.96
Std Dev	7.327

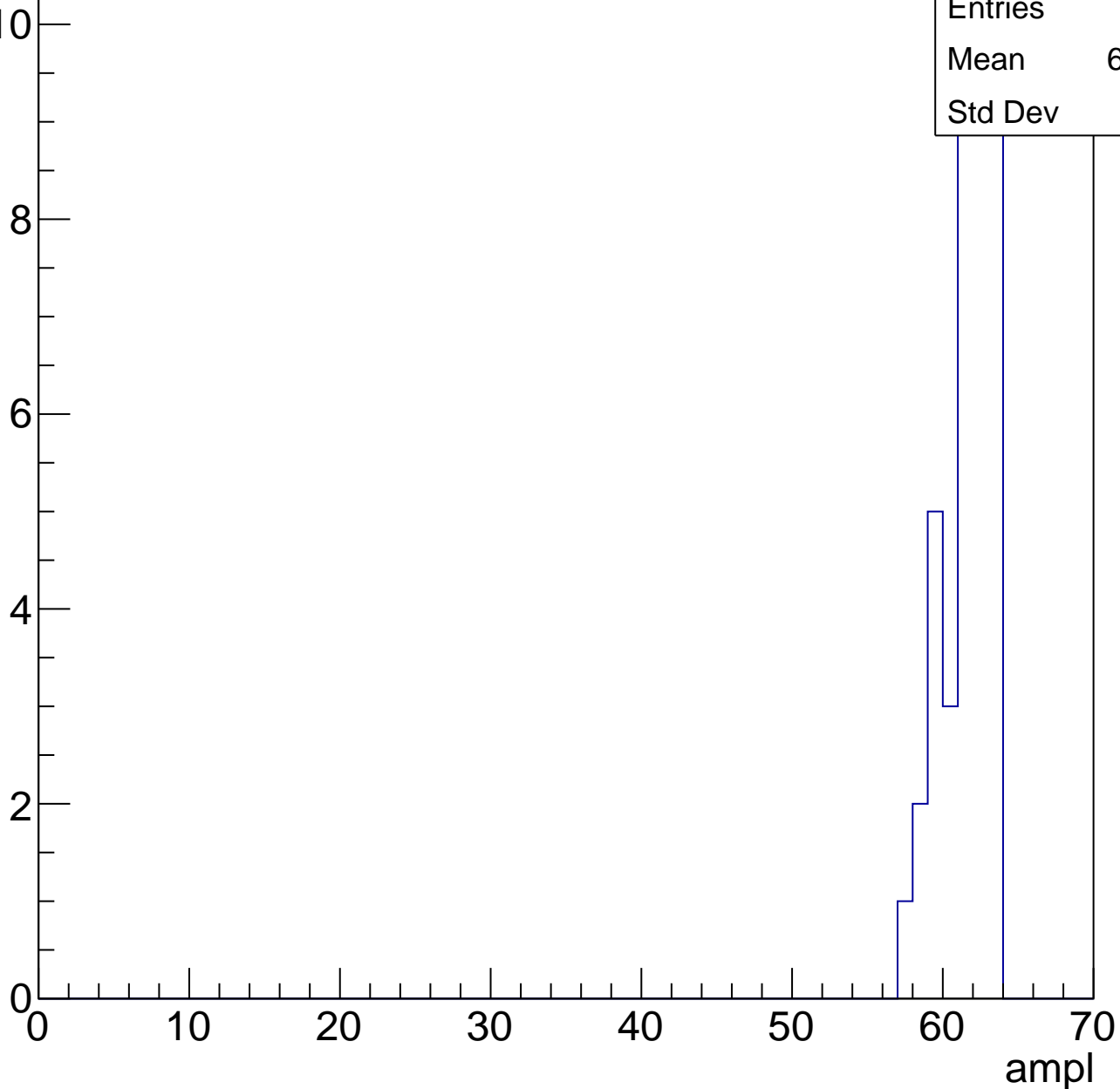


# B0L000S, U7-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	39
Mean	61.13
Std Dev	1.62



# B0L000S, U7-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch88, adc0

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	71
Mean	28.25
Std Dev	5.728

**Gaus mean : 29.3069**

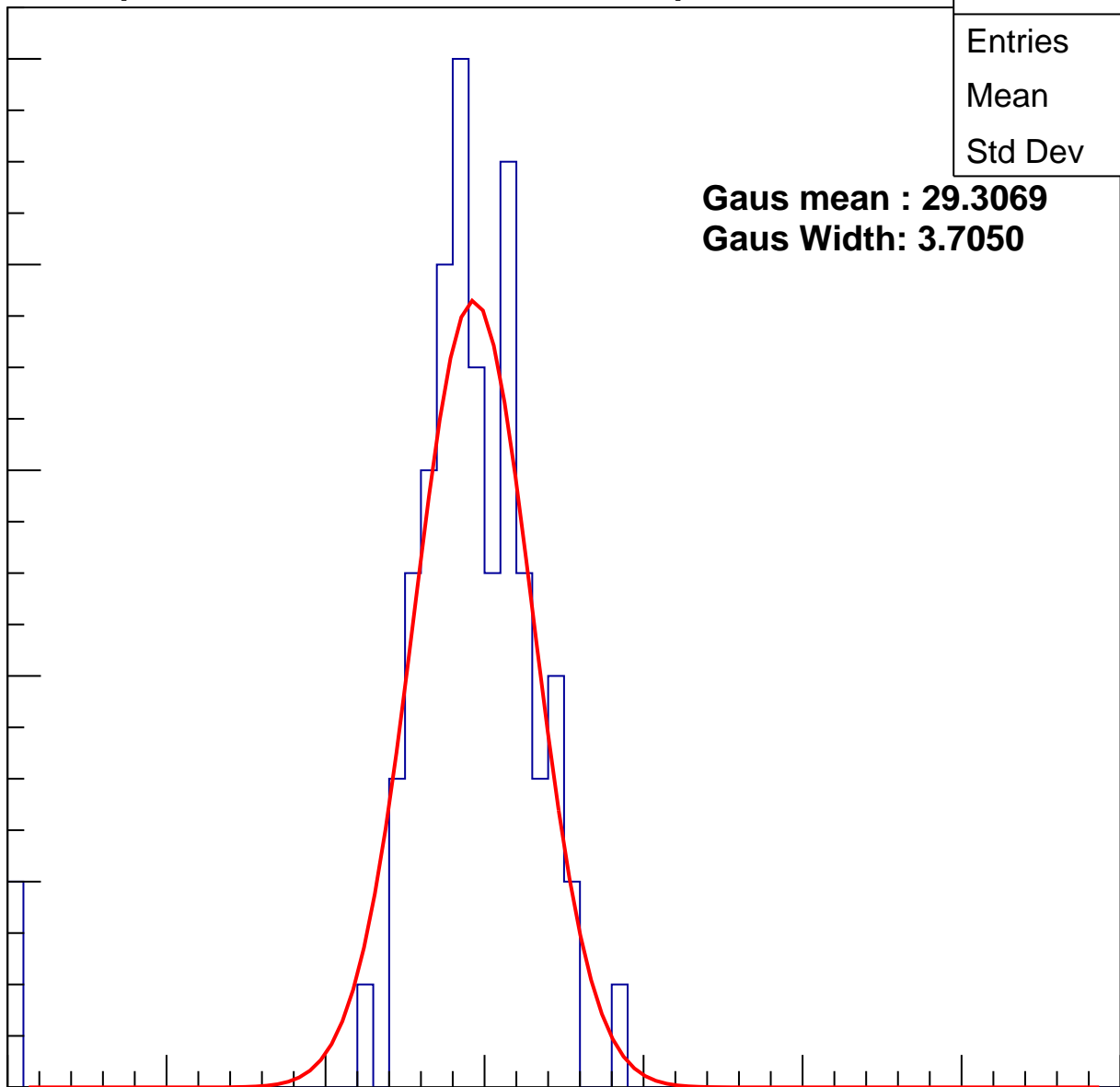
**Gaus Width: 3.7050**

Entry

10  
8  
6  
4  
2  
0

ampl

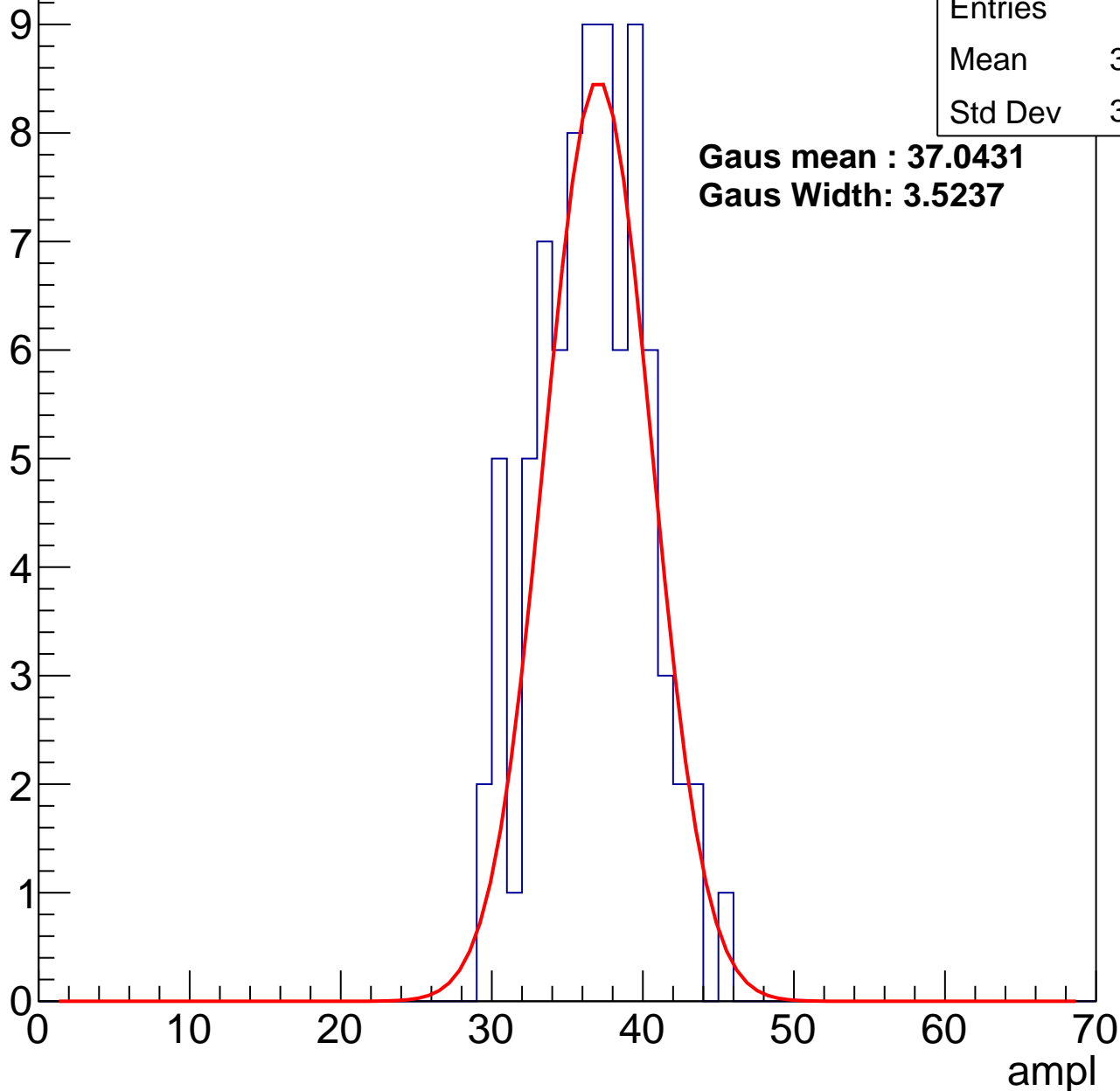
0 10 20 30 40 50 60 70



# B0L000S, U7-ch88, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch88, adc2

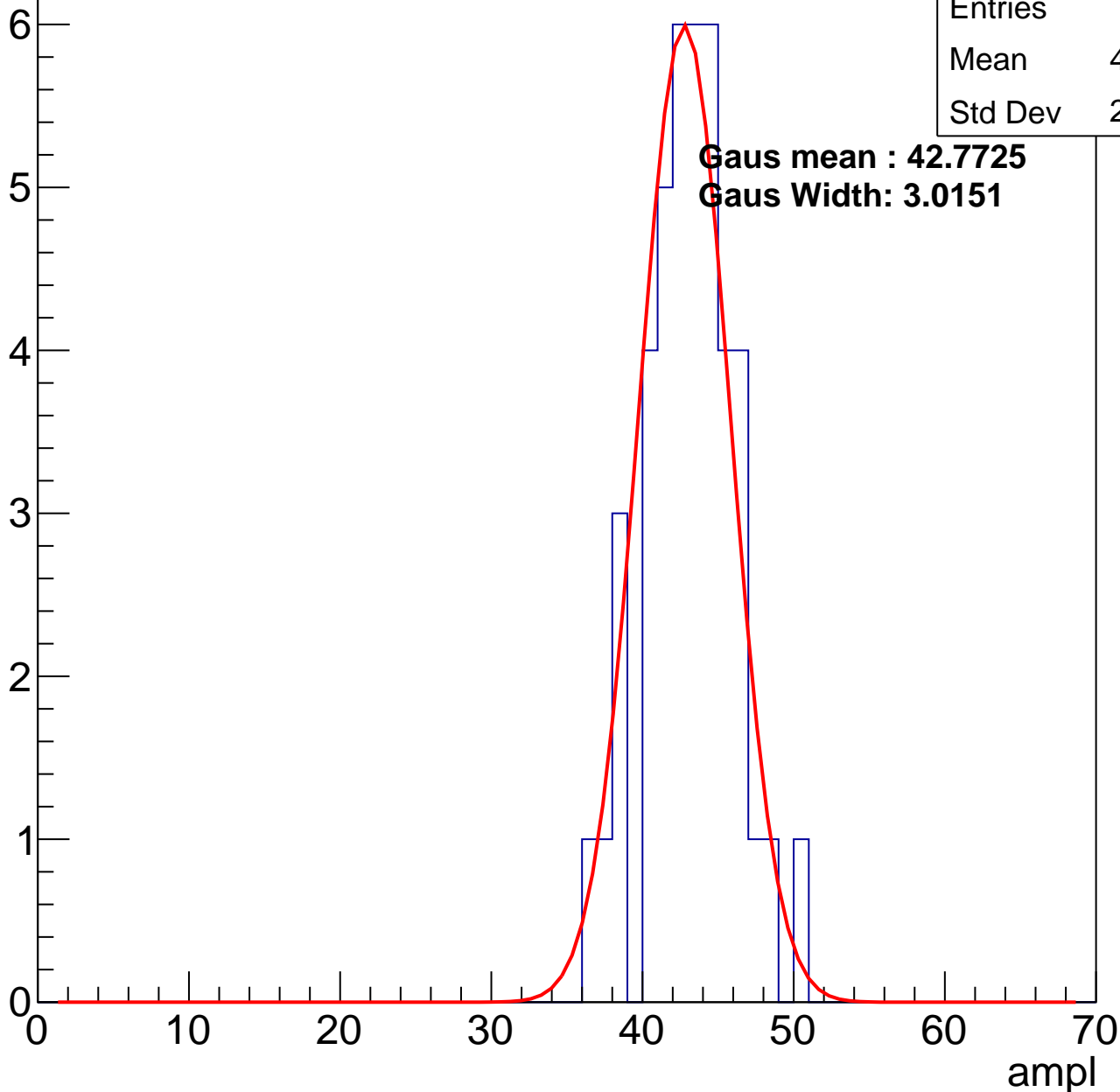
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	43
Mean	42.67
Std Dev	2.915

**Gaus mean : 42.7725**

**Gaus Width: 3.0151**

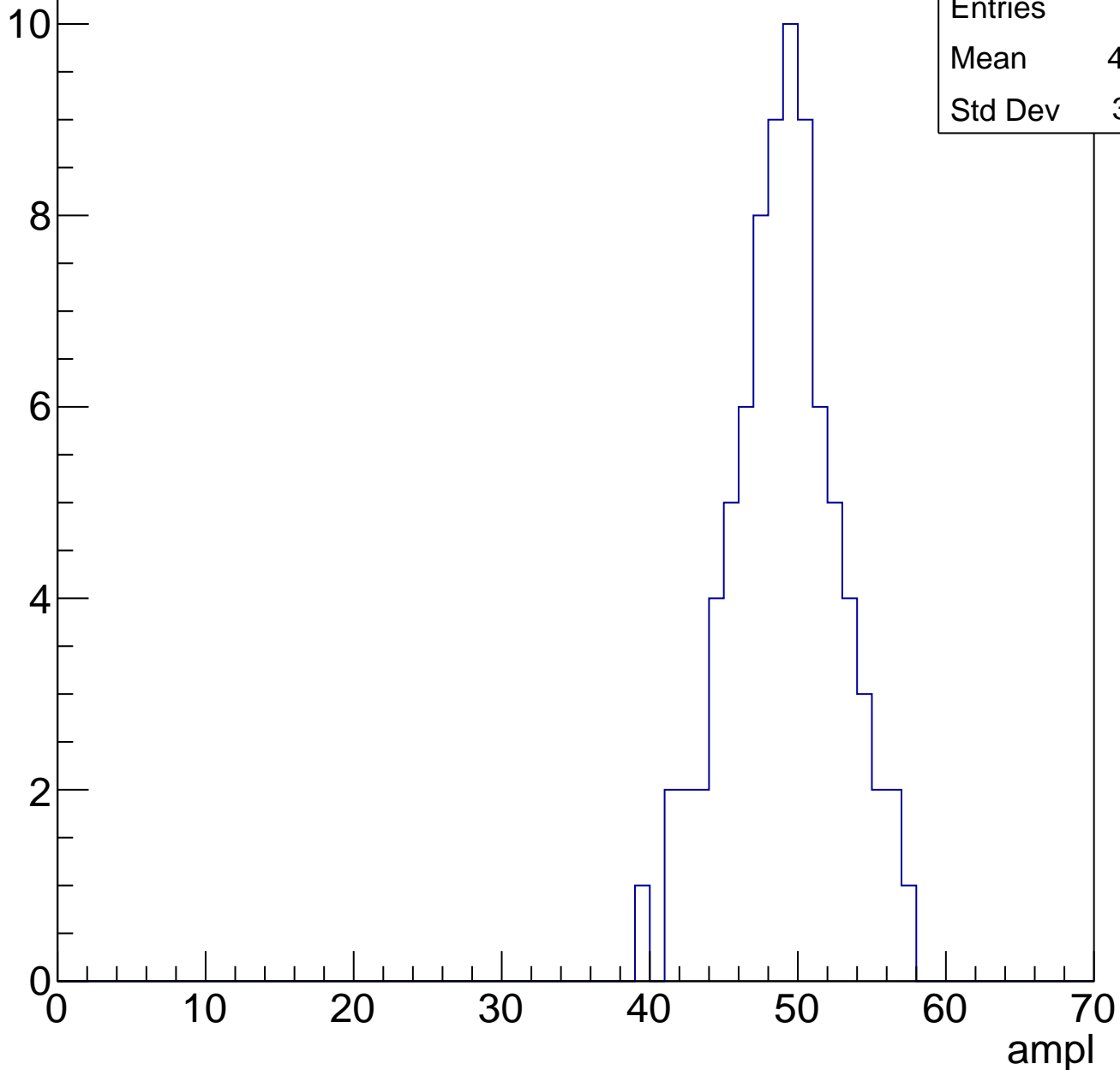


# B0L000S, U7-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

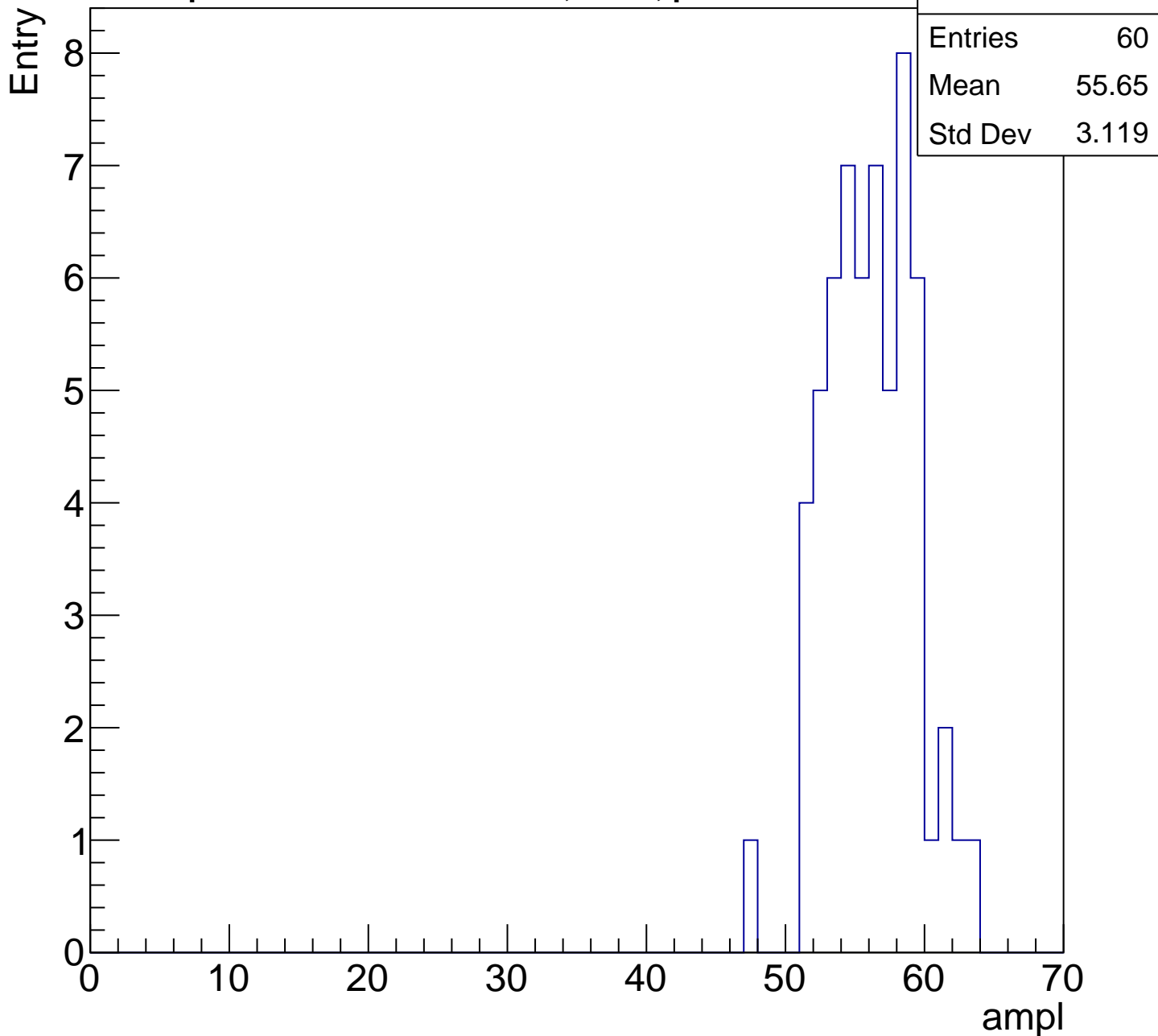
Entries	81
Mean	48.58
Std Dev	3.701

Entry



# B0L000S, U7-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1



# B0L000S, U7-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	42
Mean	58.76
Std Dev	9.451

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

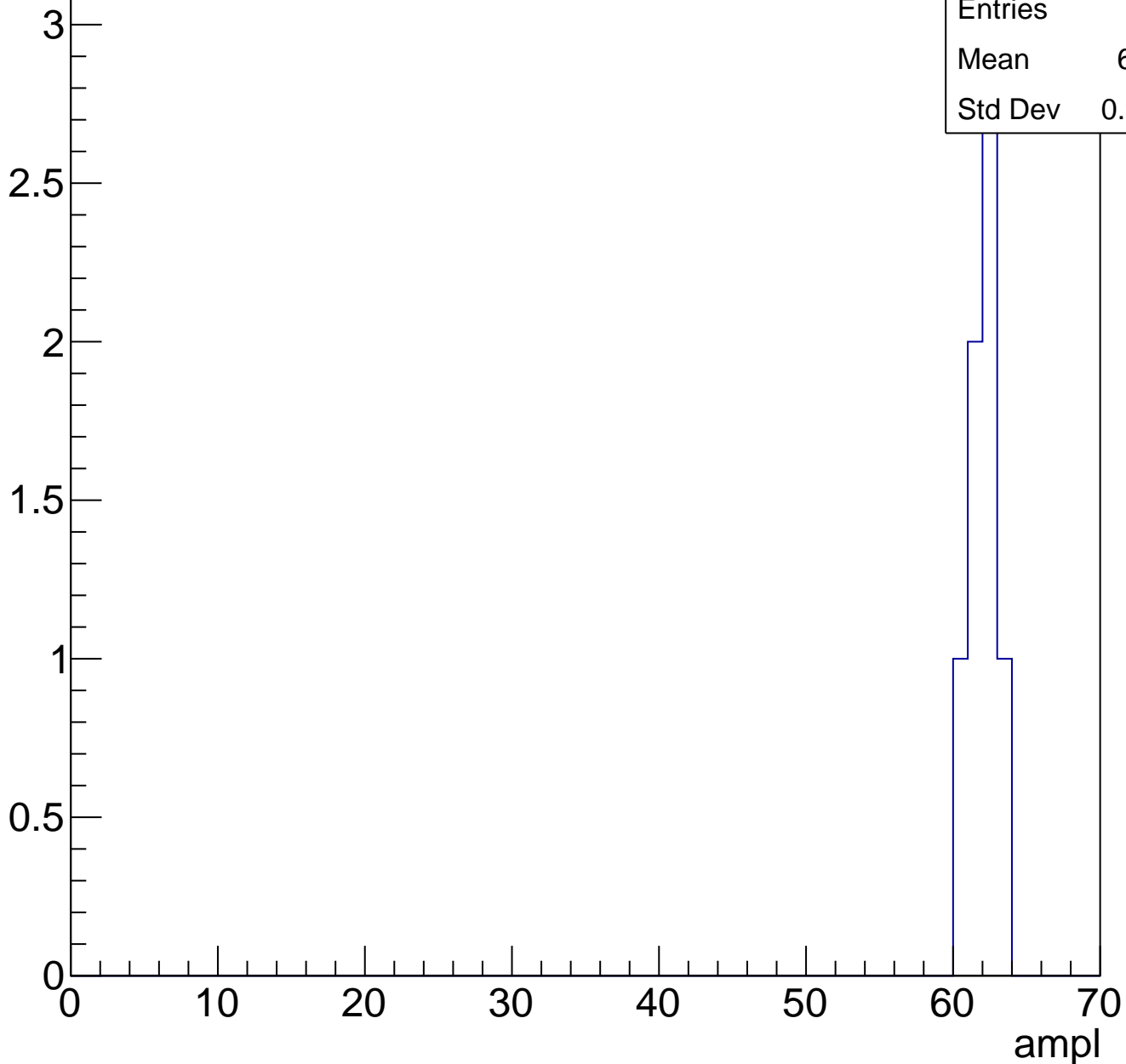
7

8

# B0L000S, U7-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L000S, U7-ch89, adc0

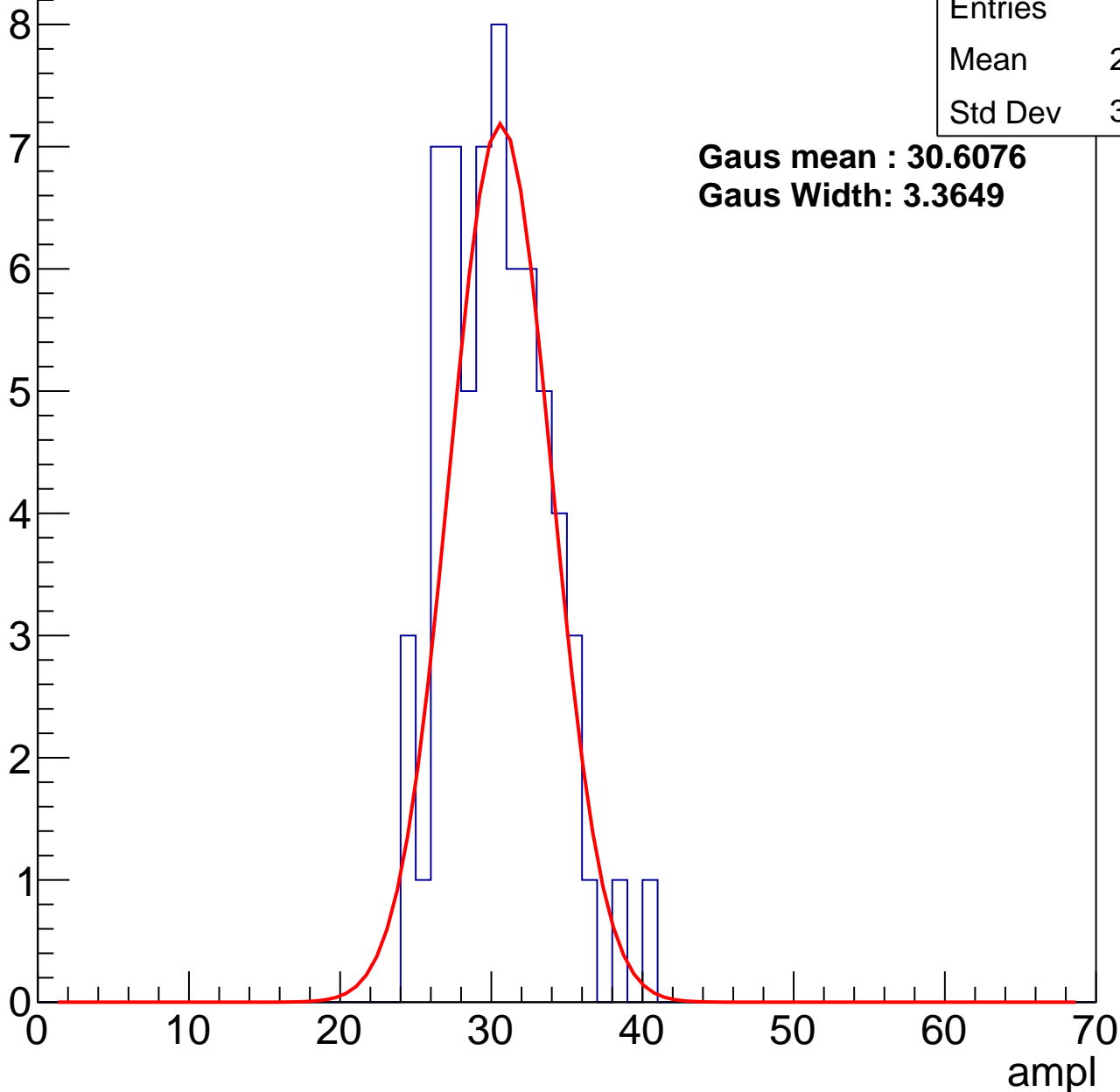
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	65
Mean	29.98
Std Dev	3.395

**Gaus mean : 30.6076**

**Gaus Width: 3.3649**



# B0L000S, U7-ch89, adc1

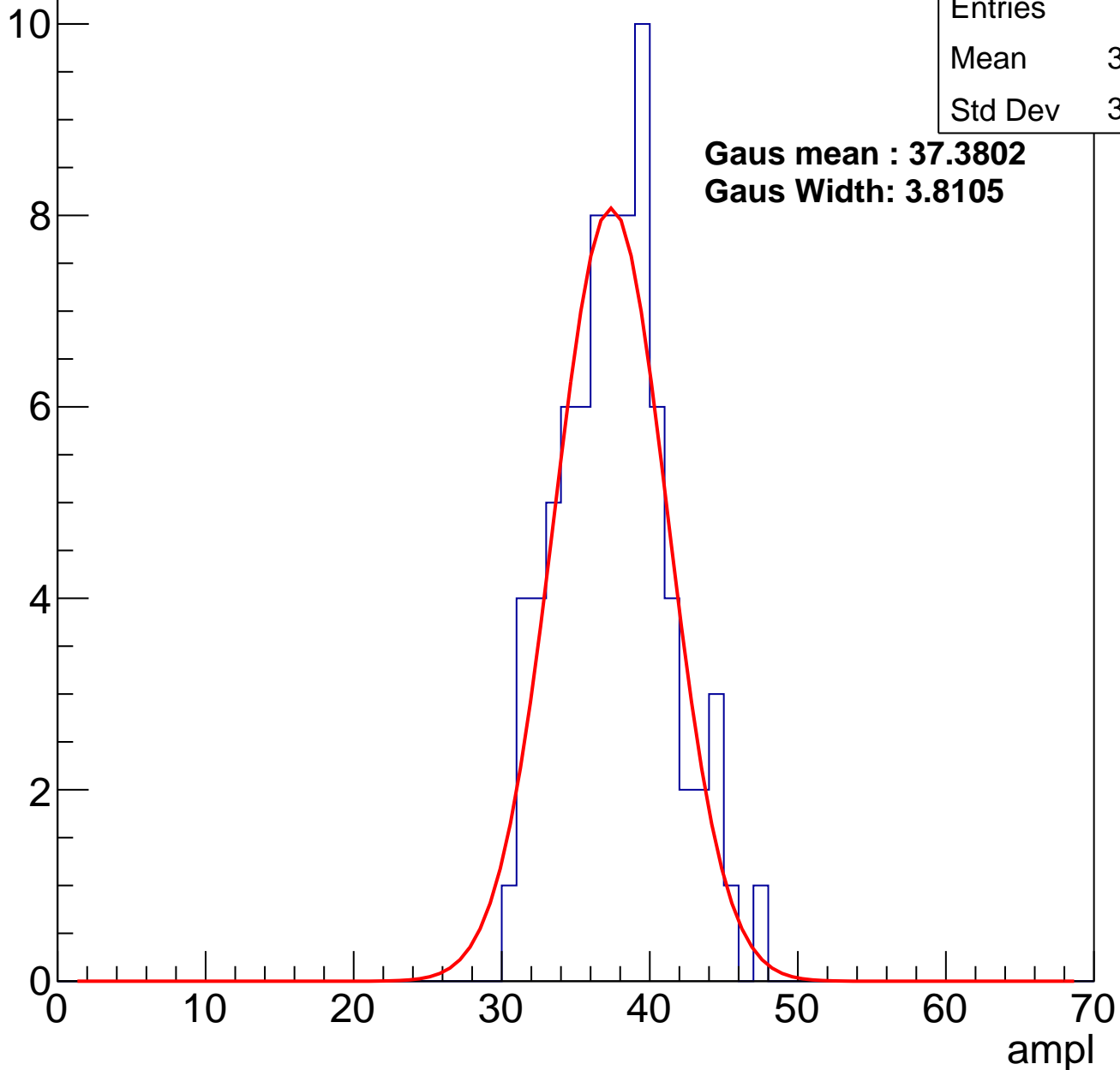
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	79
Mean	37.18
Std Dev	3.655

**Gaus mean : 37.3802**

**Gaus Width: 3.8105**

Entry

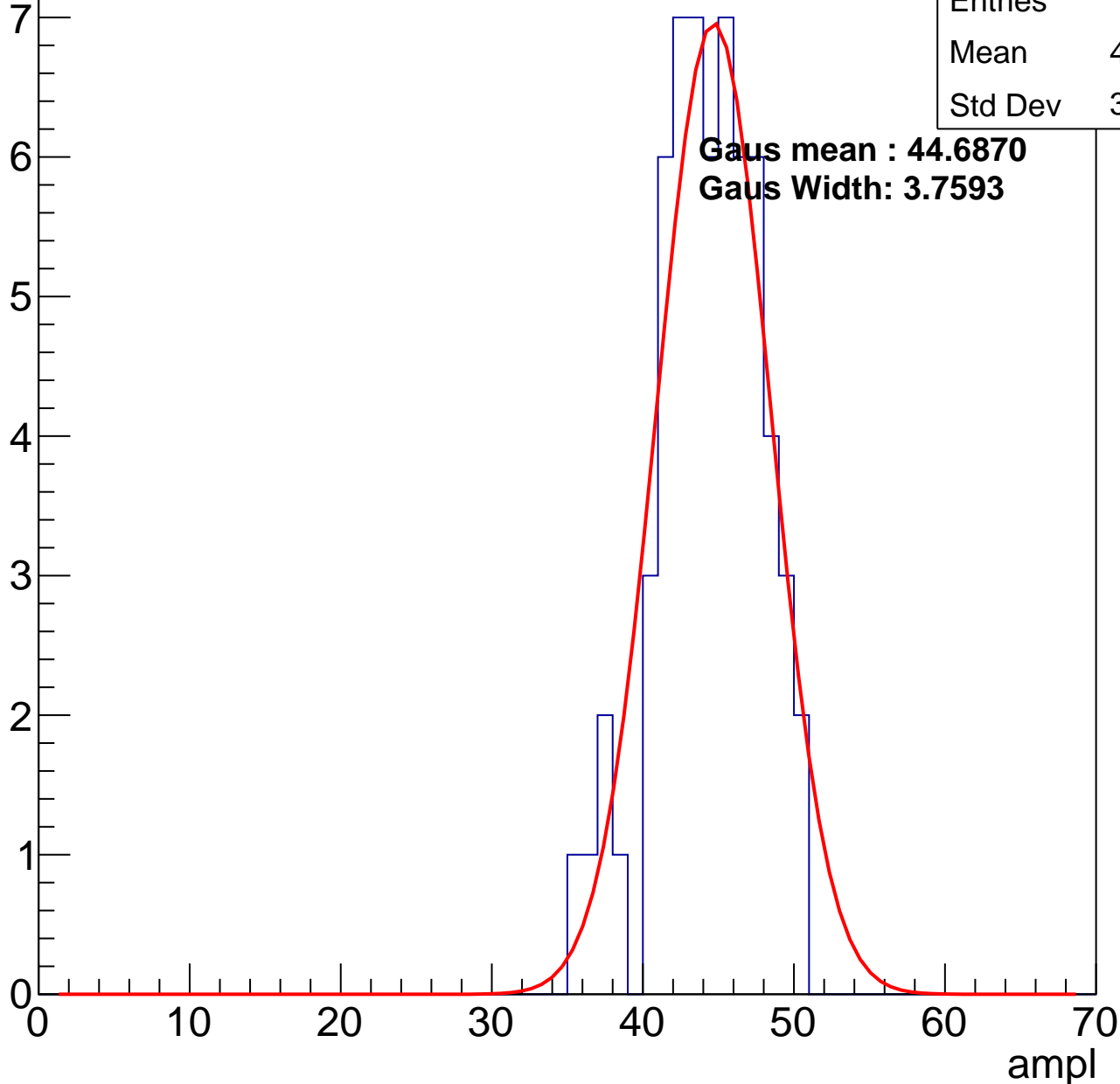


# B0L000S, U7-ch89, adc2

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	62
Mean	43.87
Std Dev	3.386

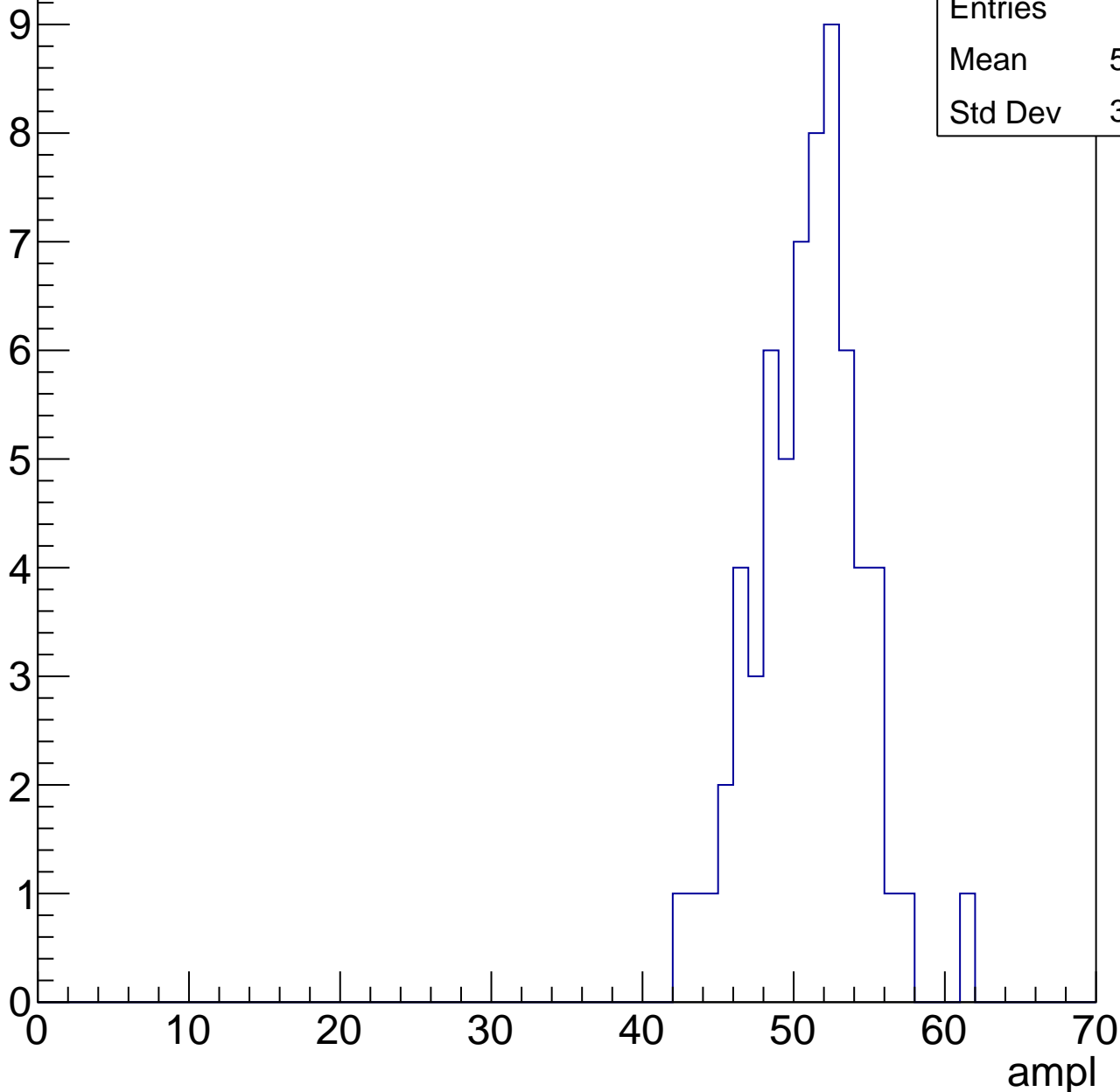


# B0L000S, U7-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

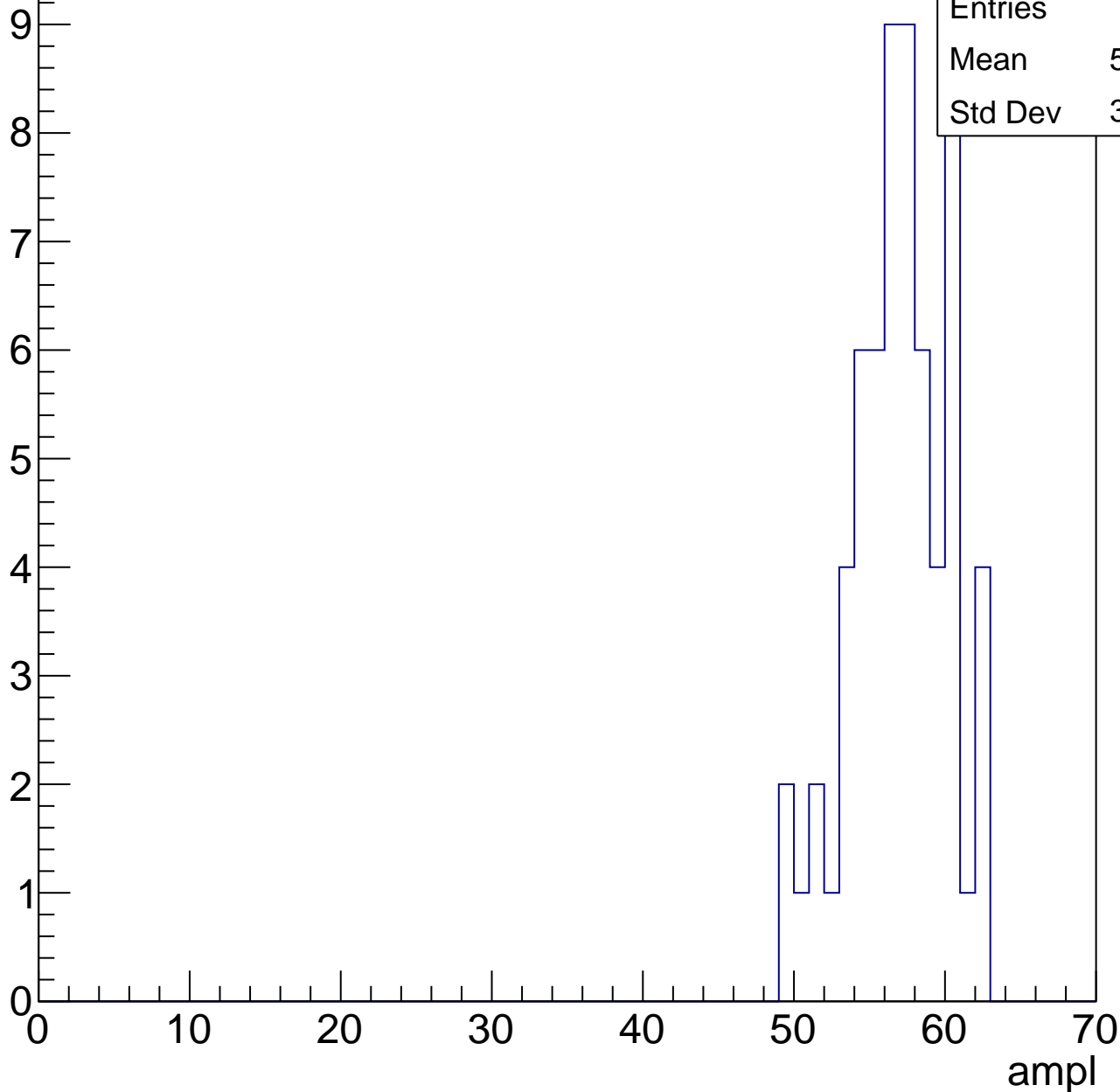
Entries	64
Mean	50.48
Std Dev	3.473



# B0L000S, U7-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

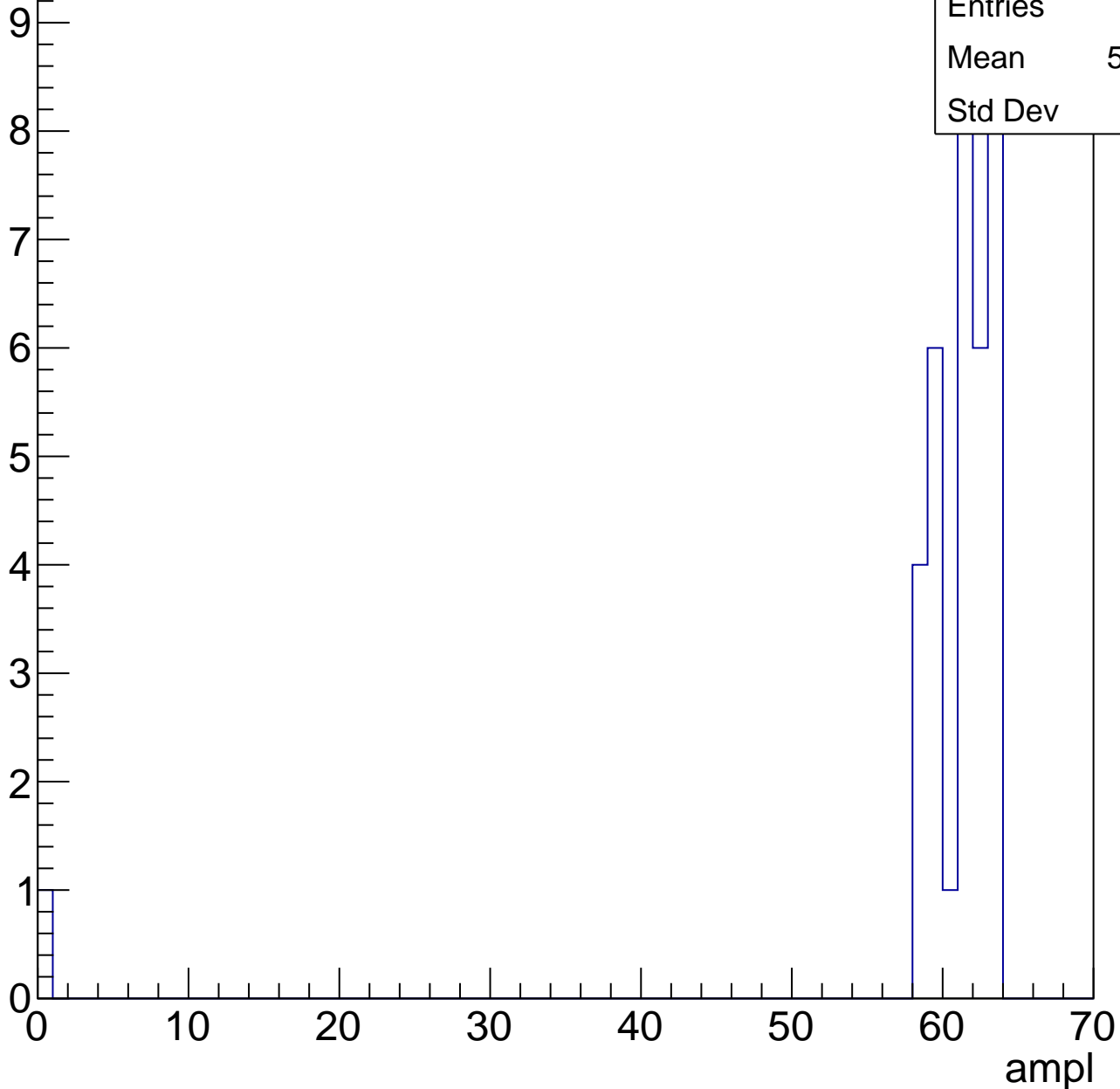
Entry



# B0L000S, U7-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch90, adc0

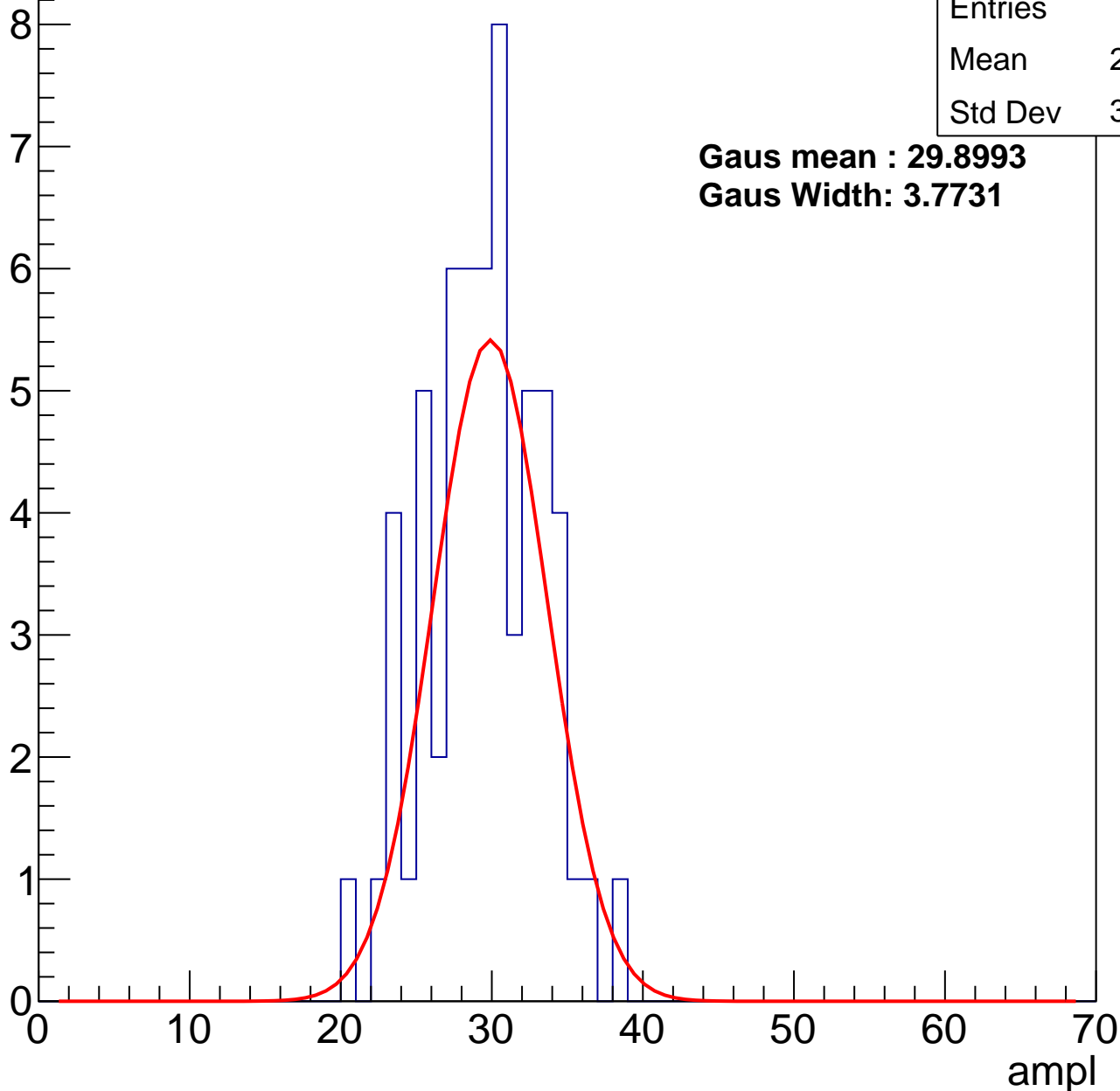
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	60
Mean	29.03
Std Dev	3.737

**Gaus mean : 29.8993**

**Gaus Width: 3.7731**



# B0L000S, U7-ch90, adc1

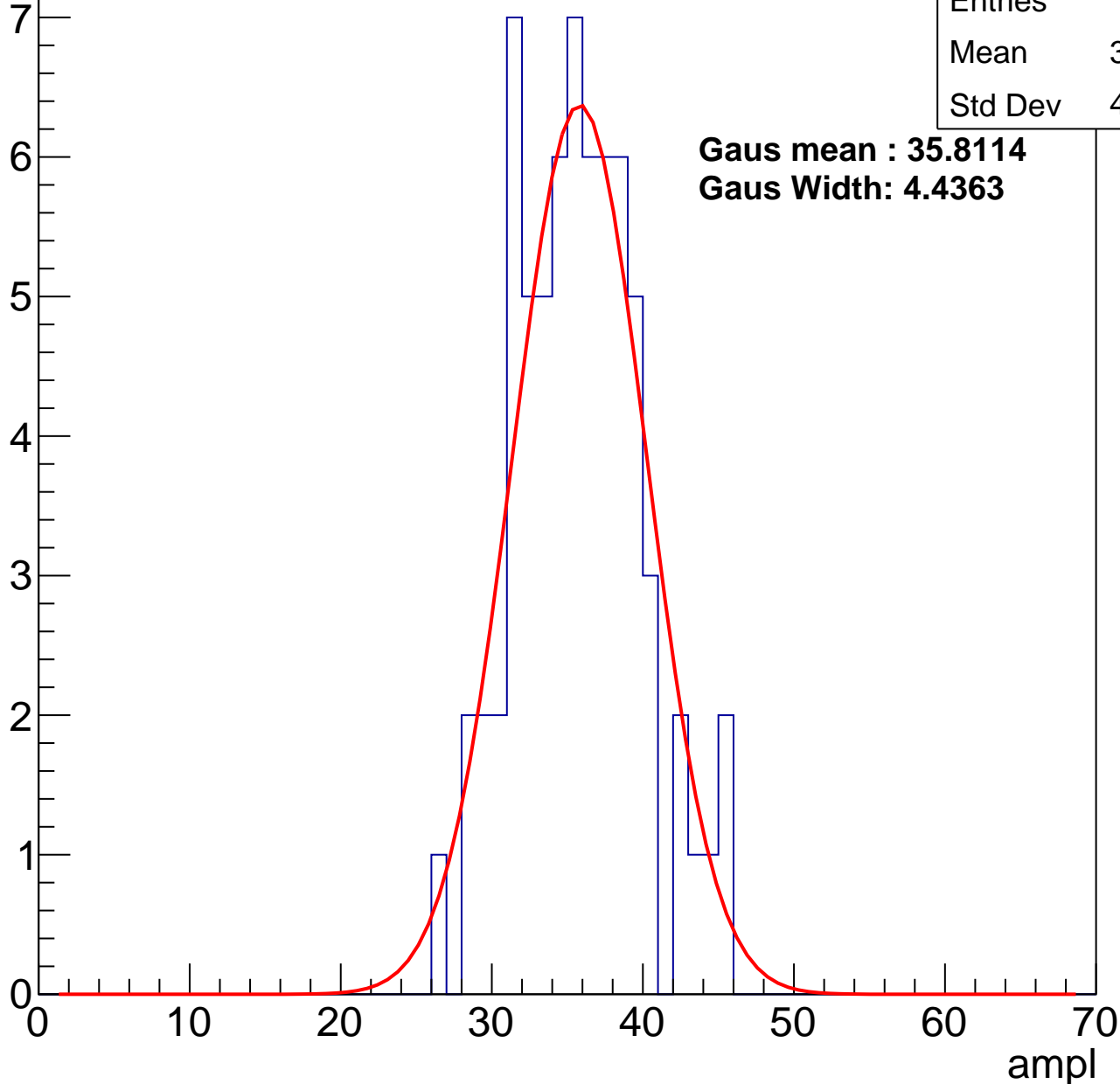
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	69
Mean	35.26
Std Dev	4.102

**Gaus mean : 35.8114**

**Gaus Width: 4.4363**



# B0L000S, U7-ch90, adc2

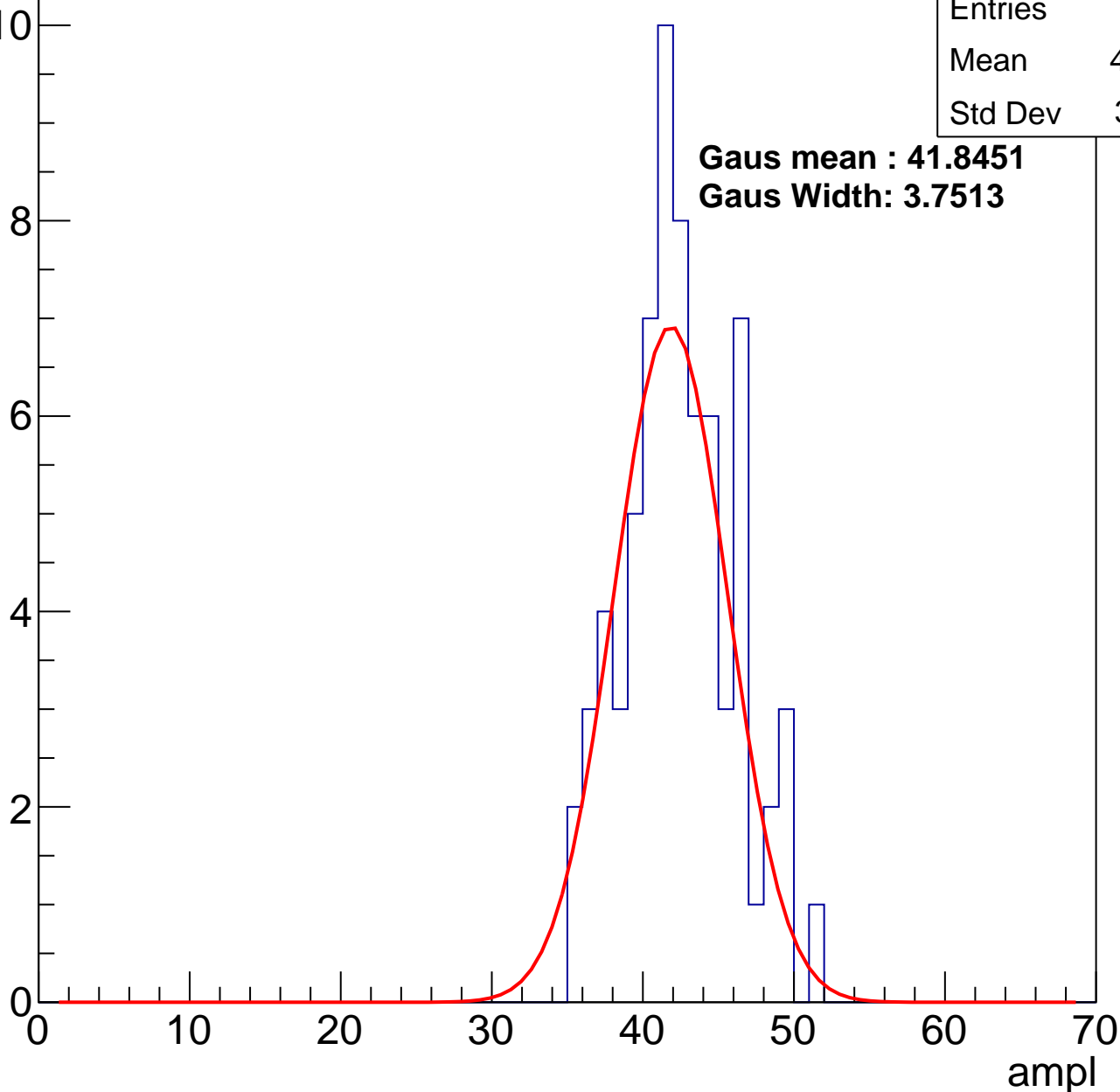
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	71
Mean	41.99
Std Dev	3.621

**Gaus mean : 41.8451**

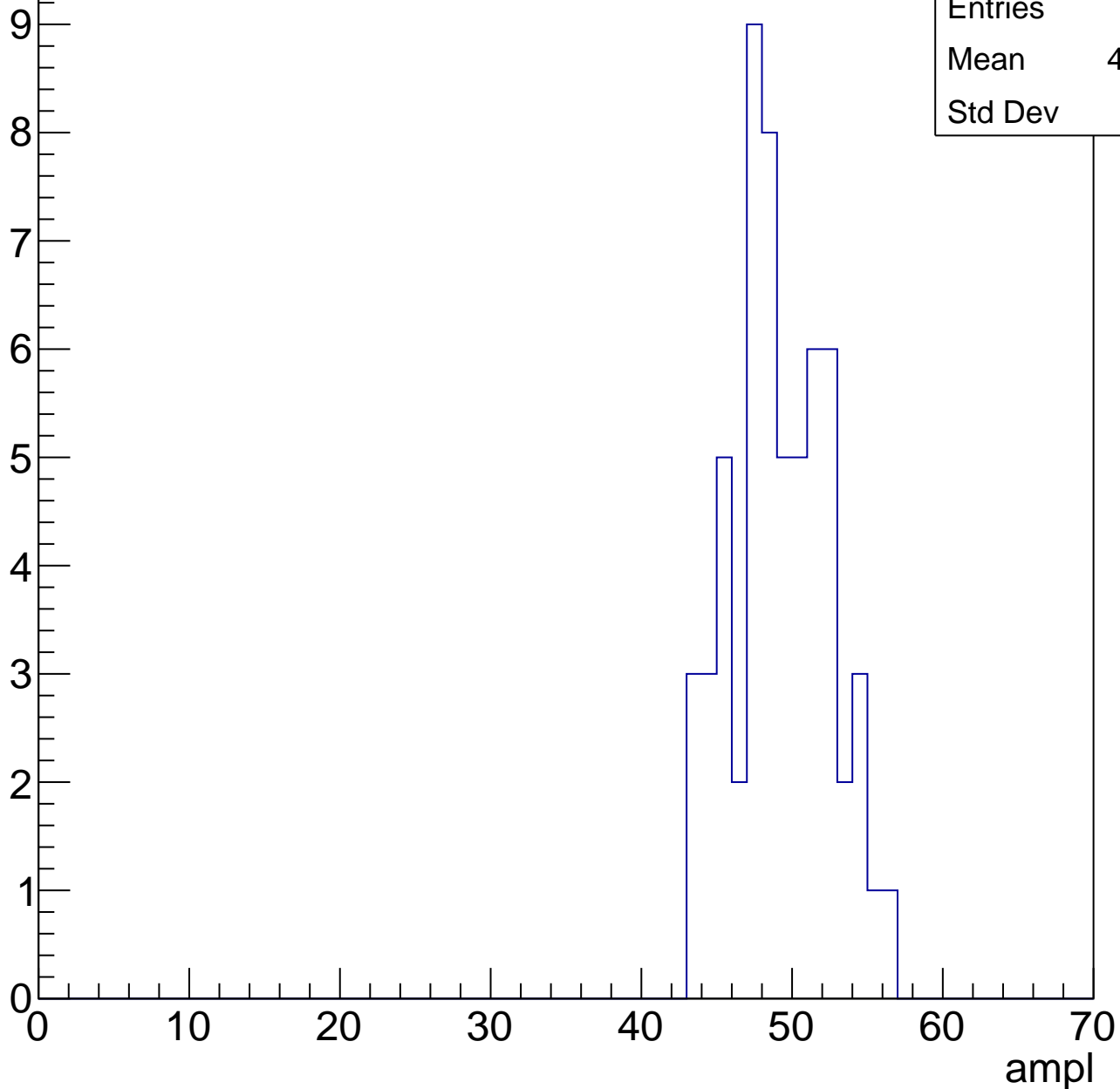
**Gaus Width: 3.7513**



# B0L000S, U7-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

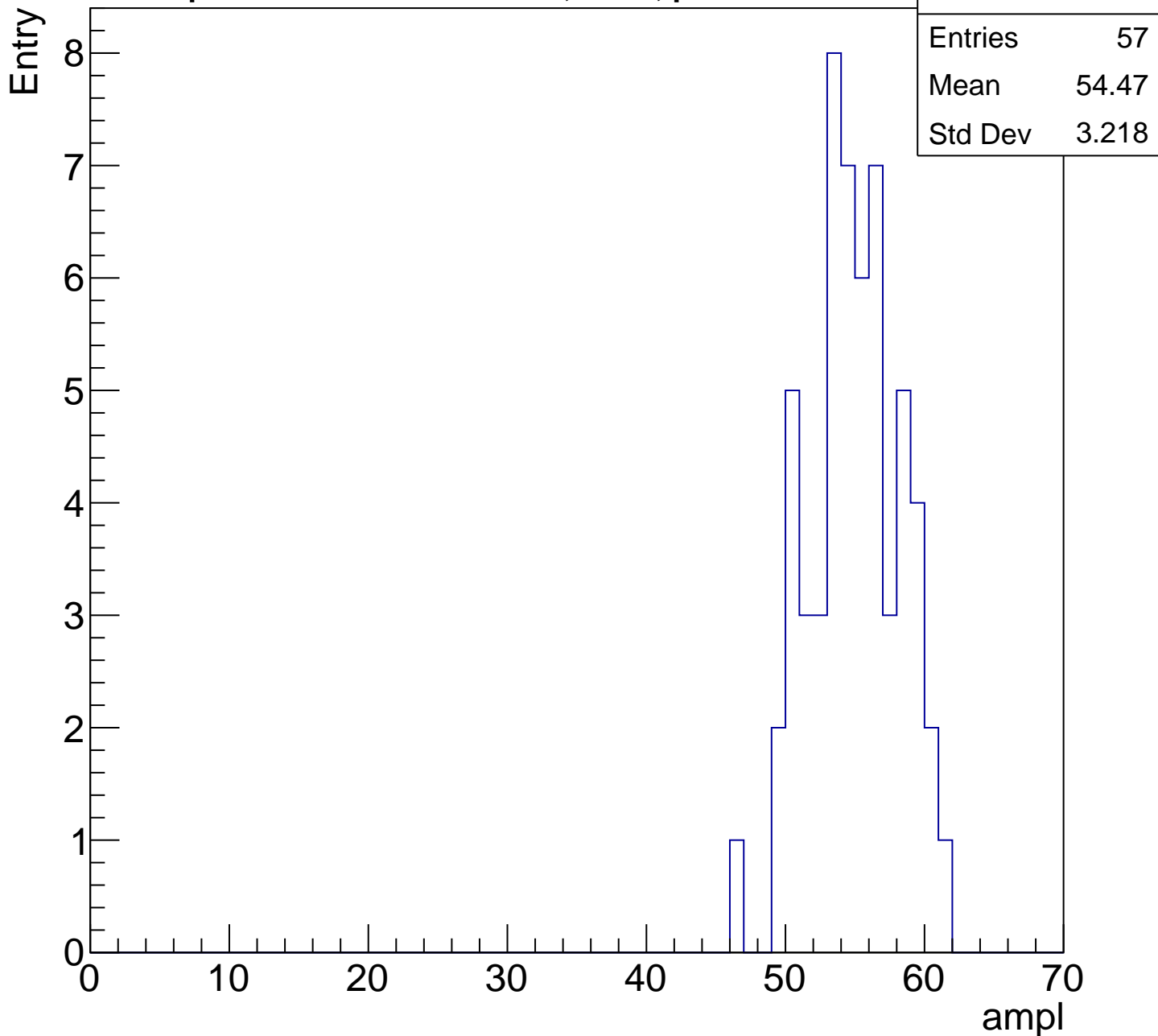
Entry



Entries	59
Mean	48.76
Std Dev	3.18

# B0L000S, U7-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

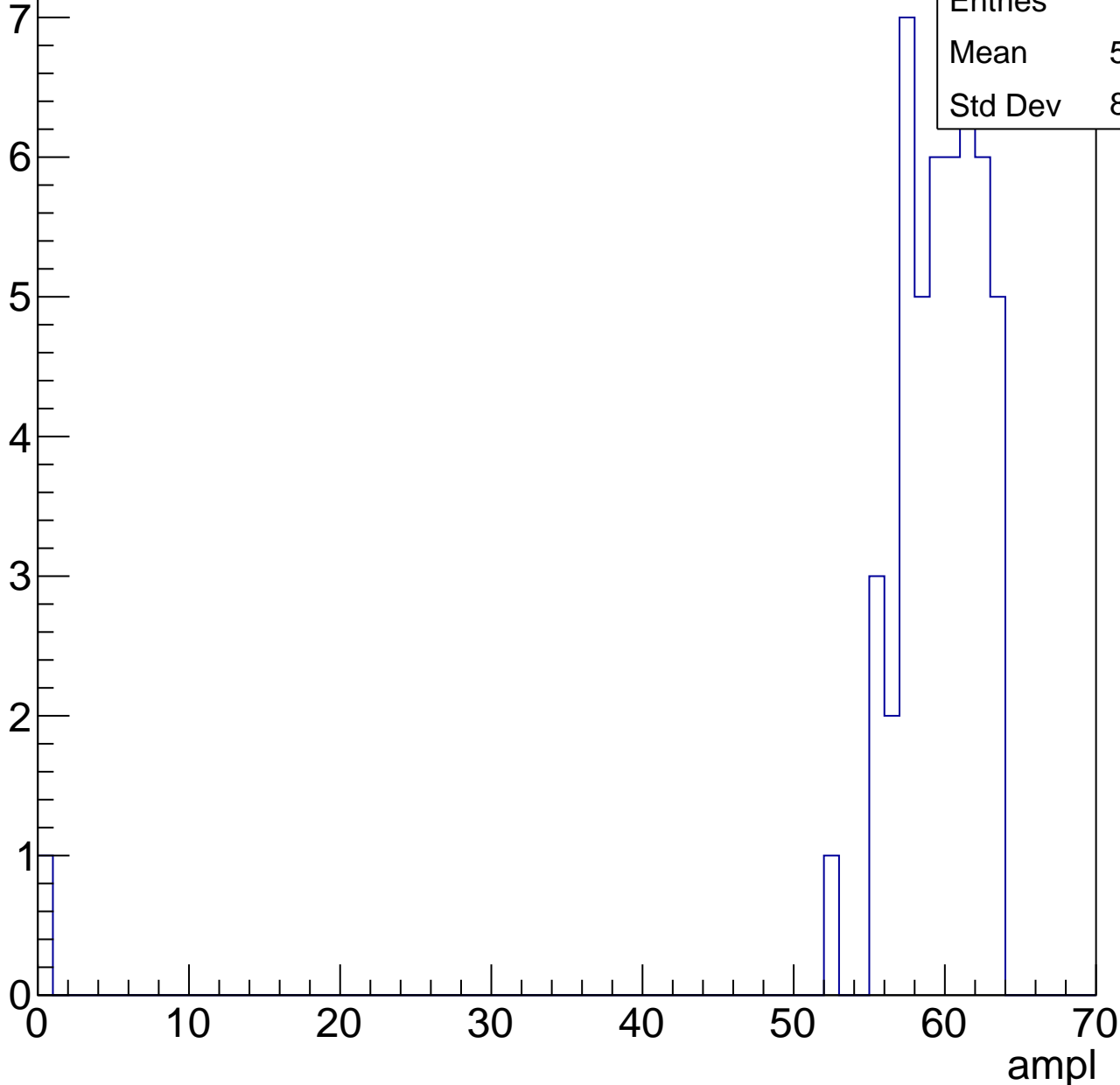


# B0L000S, U7-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	49
Mean	58.08
Std Dev	8.755

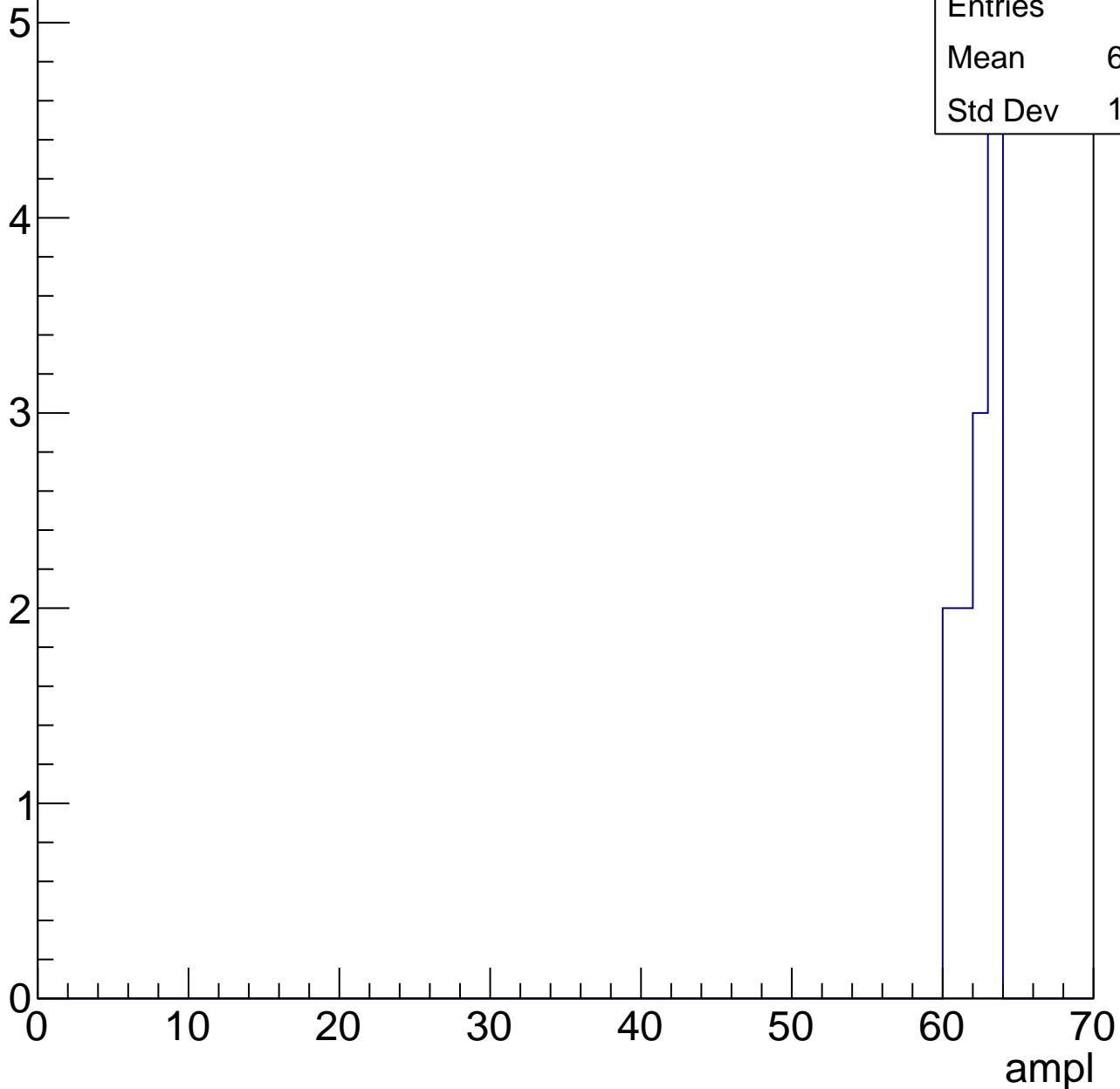


# B0L000S, U7-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	12
Mean	61.92
Std Dev	1.115

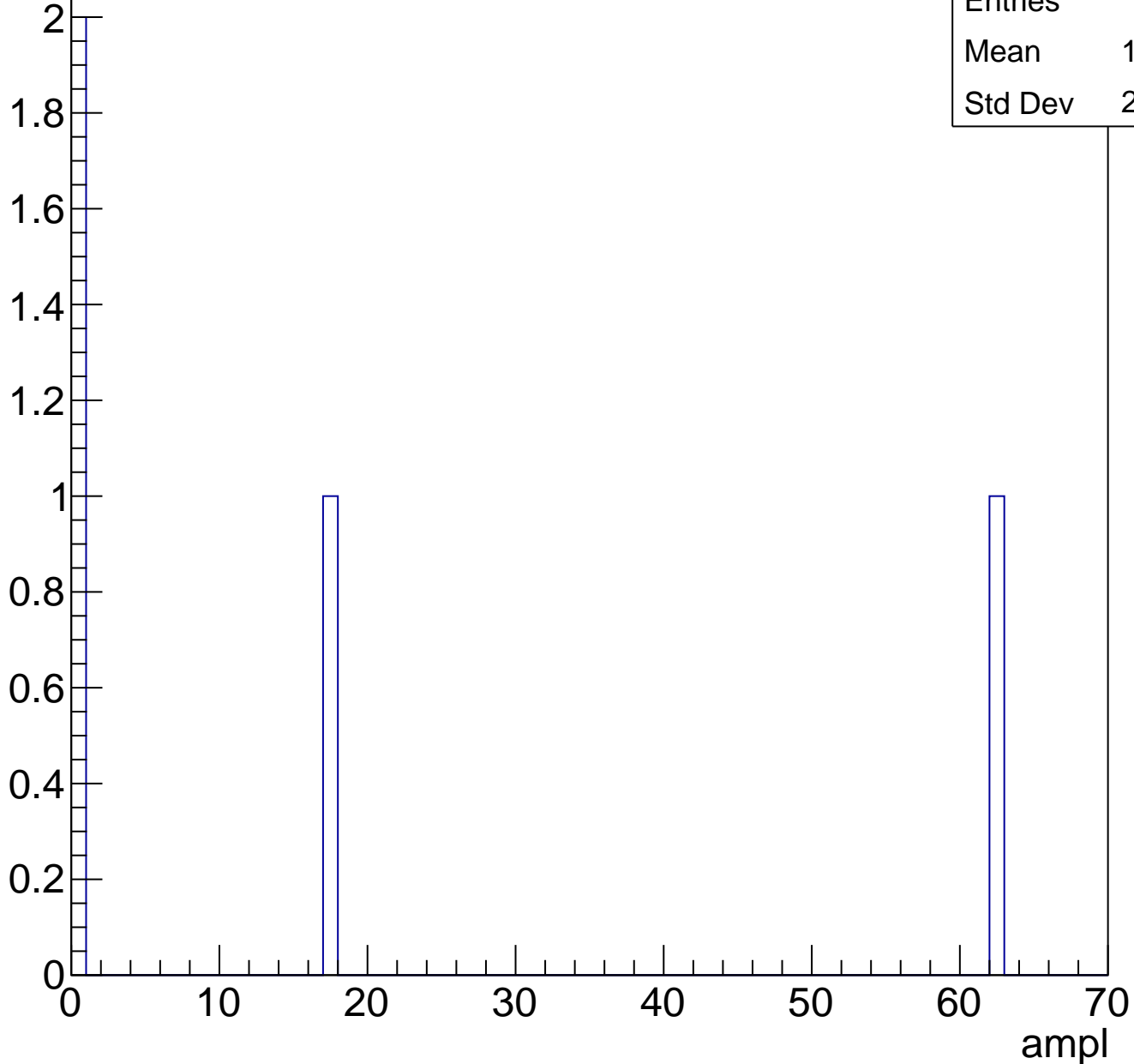




# B0L000S, U7-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	4
Mean	19.75
Std Dev	25.36

# B0L000S, U7-ch91, adc0

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	76
Mean	30.24
Std Dev	3.137

**Gaus mean : 30.6283**

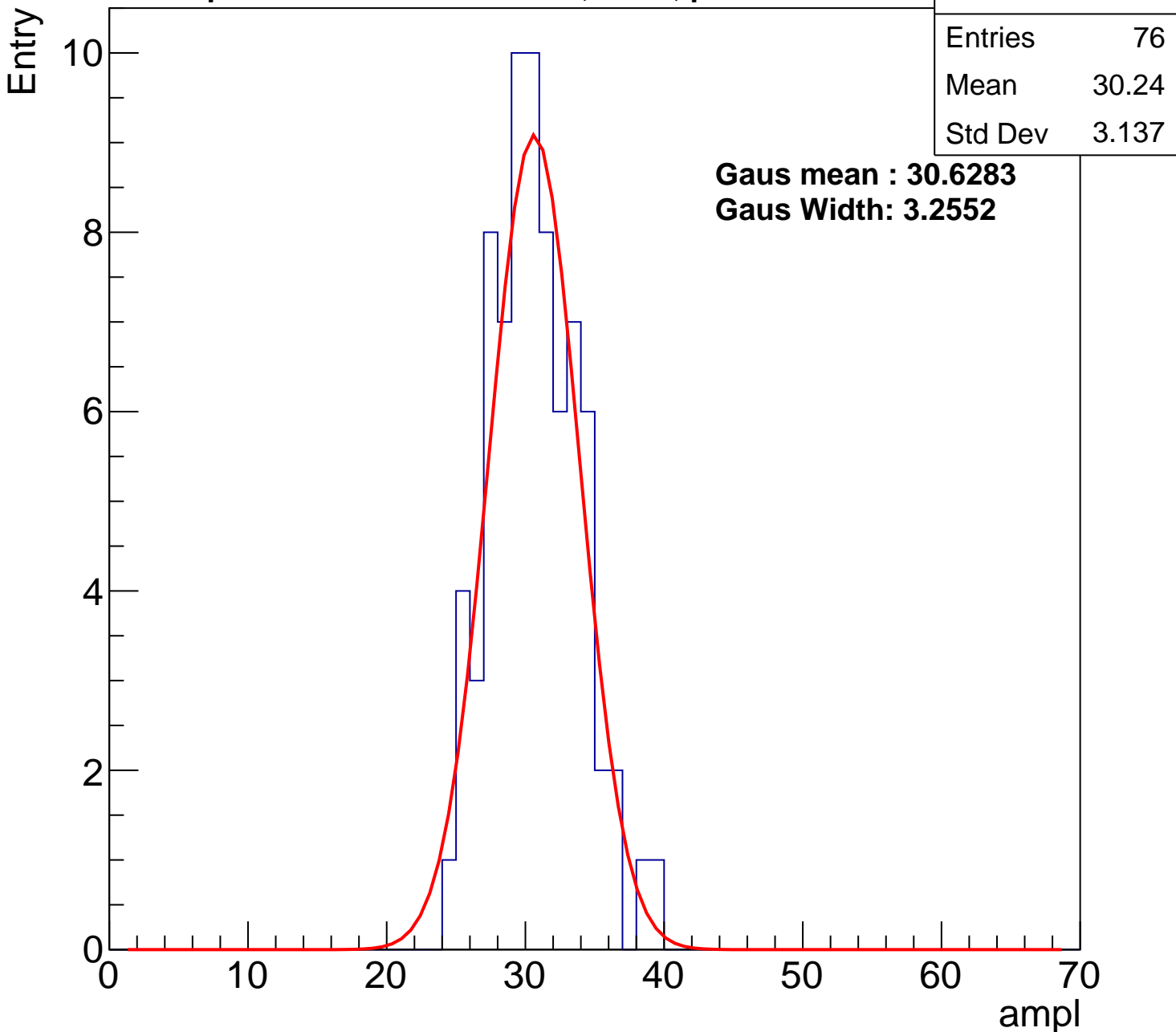
**Gaus Width: 3.2552**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L000S, U7-ch91, adc1

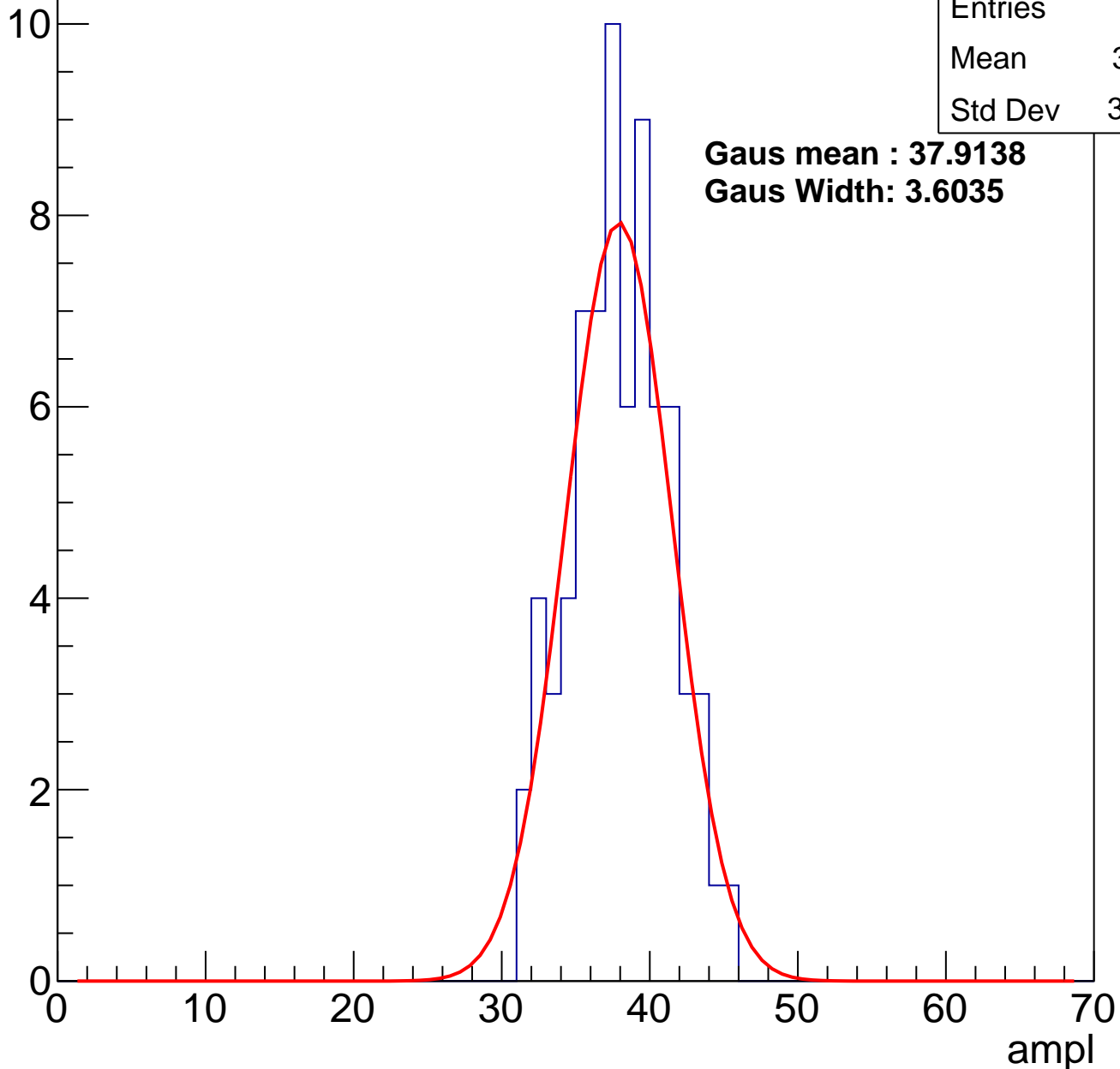
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	72
Mean	37.51
Std Dev	3.249

**Gaus mean : 37.9138**

**Gaus Width: 3.6035**

Entry



# B0L000S, U7-ch91, adc2

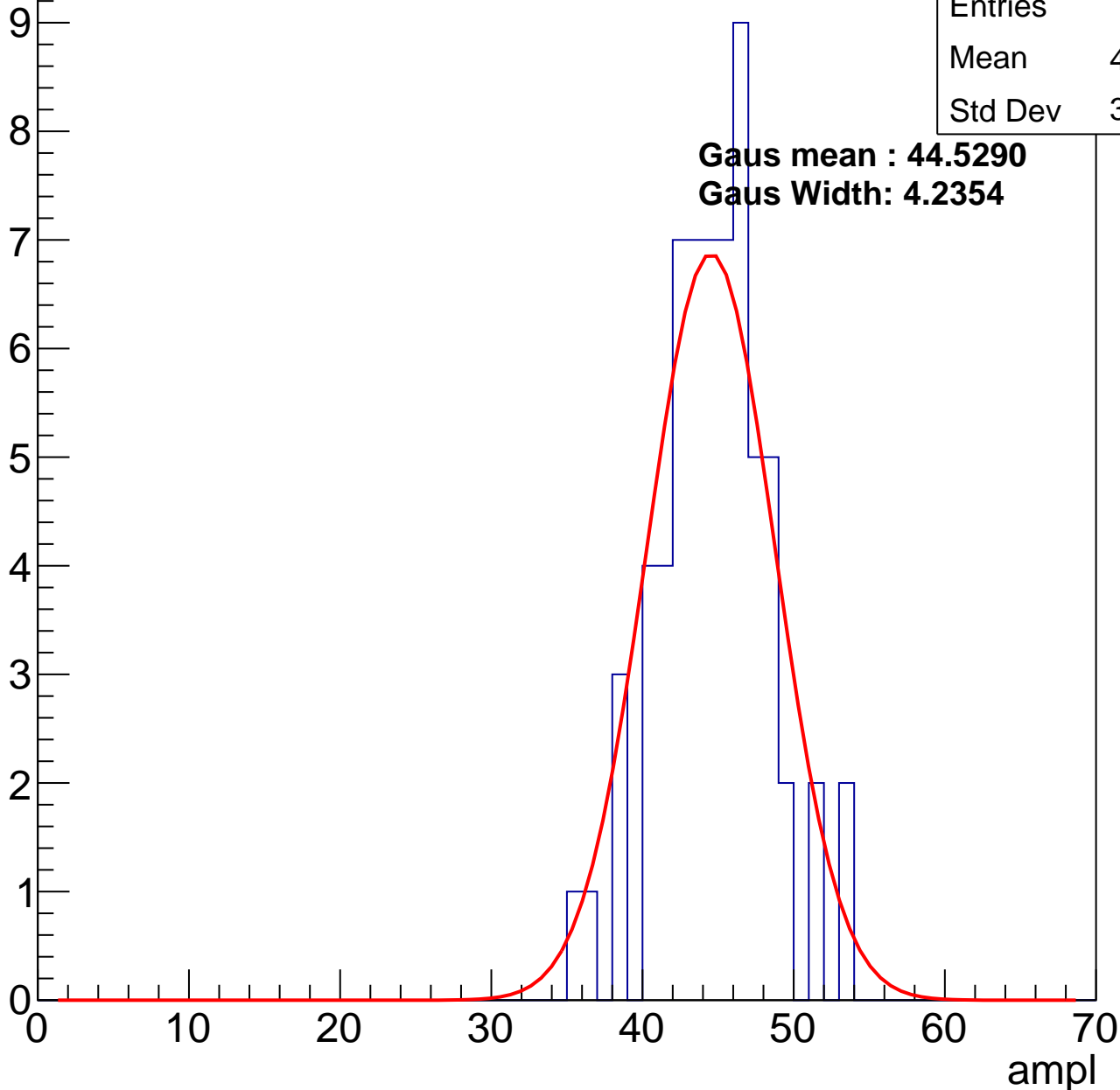
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	66
Mean	44.27
Std Dev	3.612

**Gaus mean : 44.5290**

**Gaus Width: 4.2354**

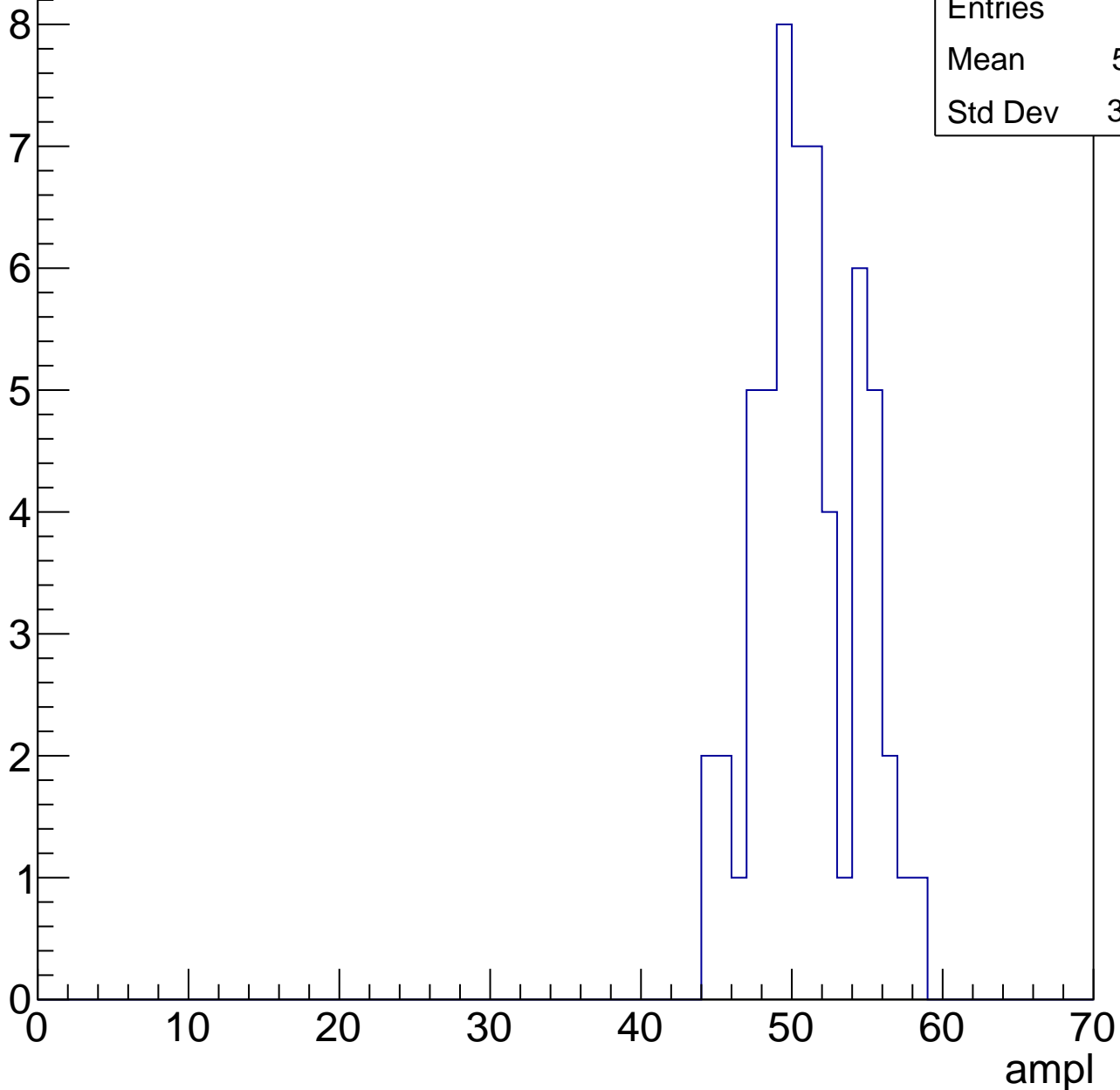


# B0L000S, U7-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

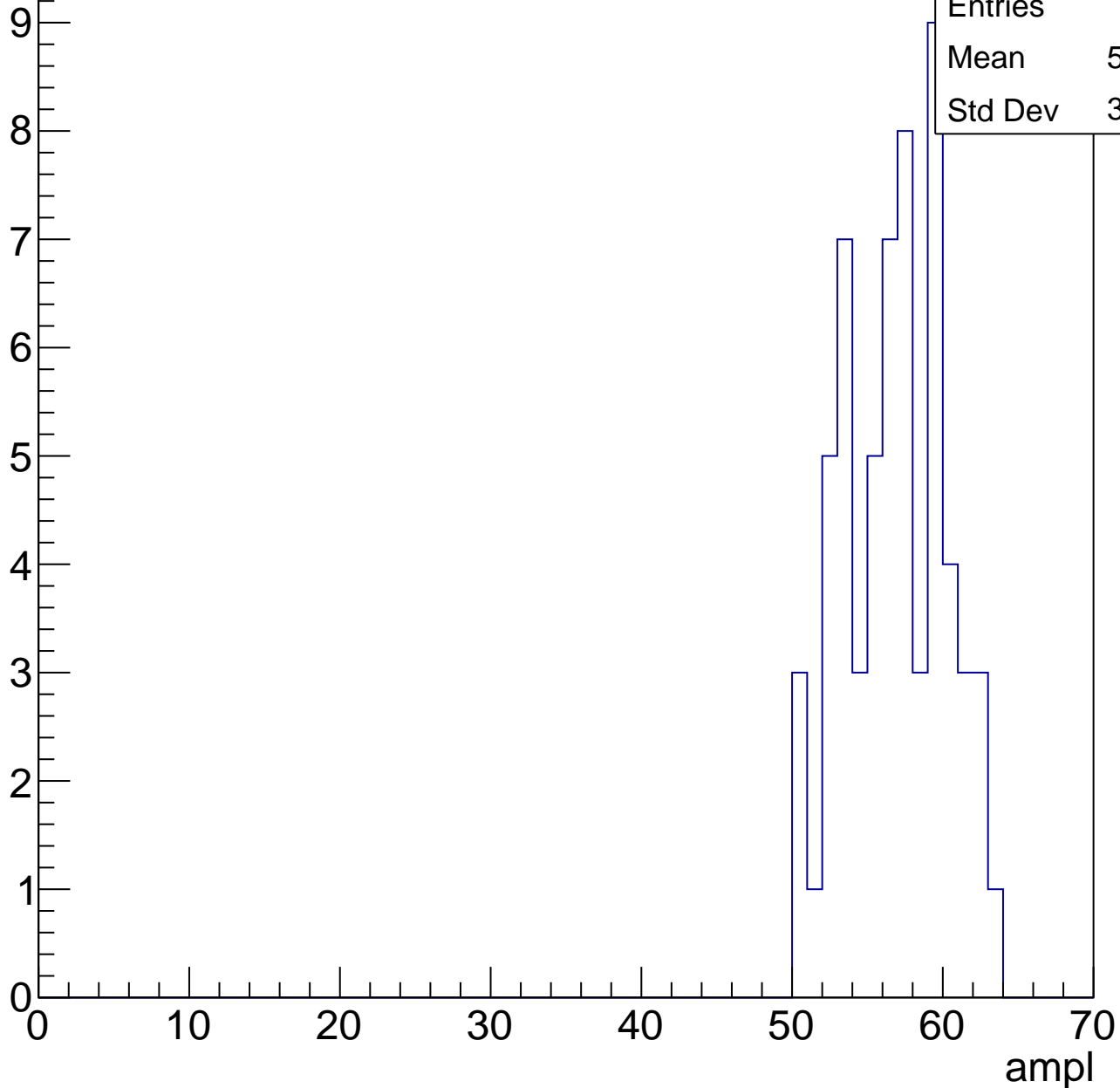
Entries	57
Mean	50.61
Std Dev	3.318



# B0L000S, U7-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

7

6

5

4

3

2

1

0

Entries 36

Mean 58.44

Std Dev 10.21

ampl

0

10

20

30

40

50

60

70

# B0L000S, U7-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch92, adc0

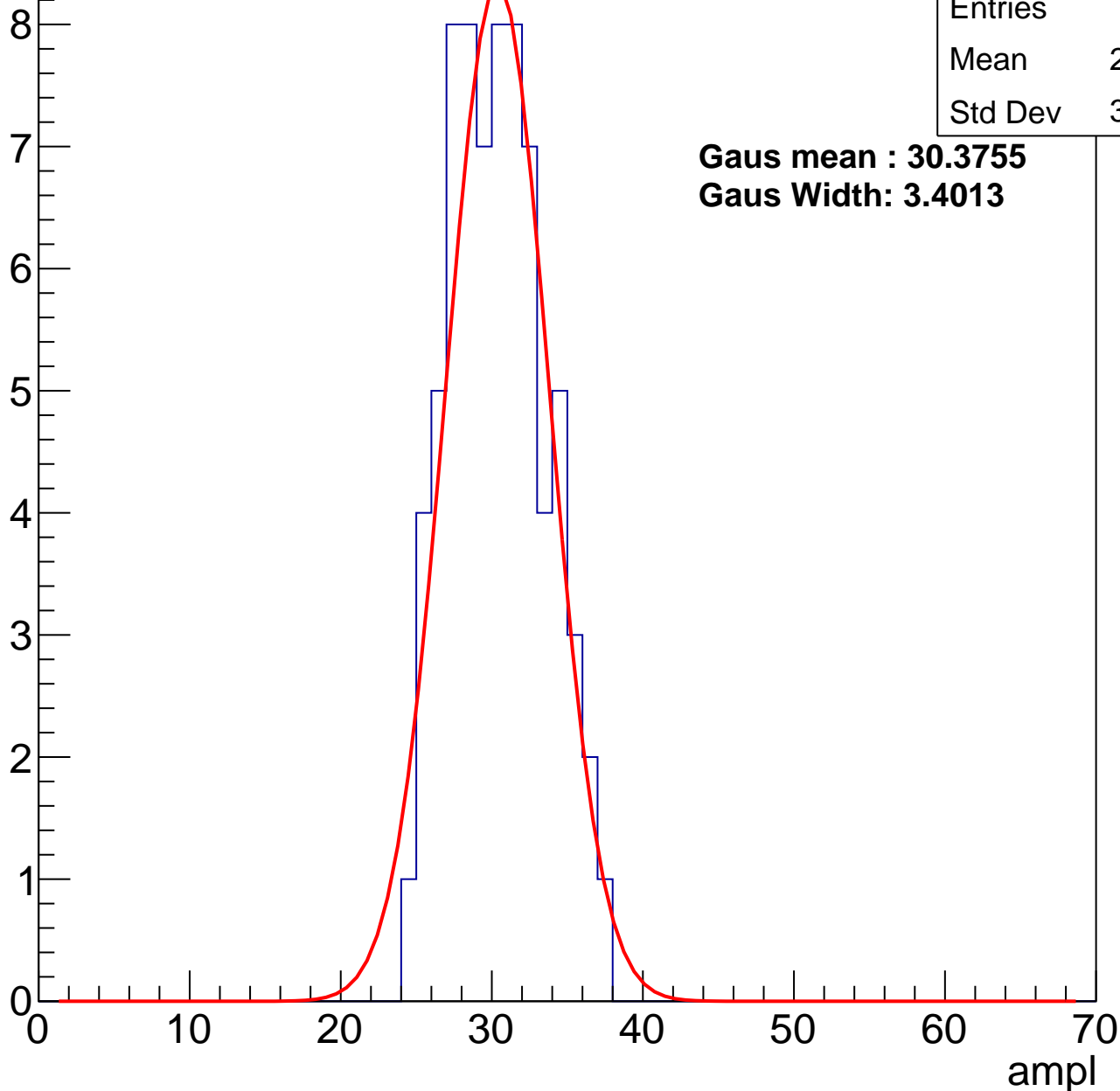
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	71
Mean	29.93
Std Dev	3.083

**Gaus mean : 30.3755**

**Gaus Width: 3.4013**



# B0L000S, U7-ch92, adc1

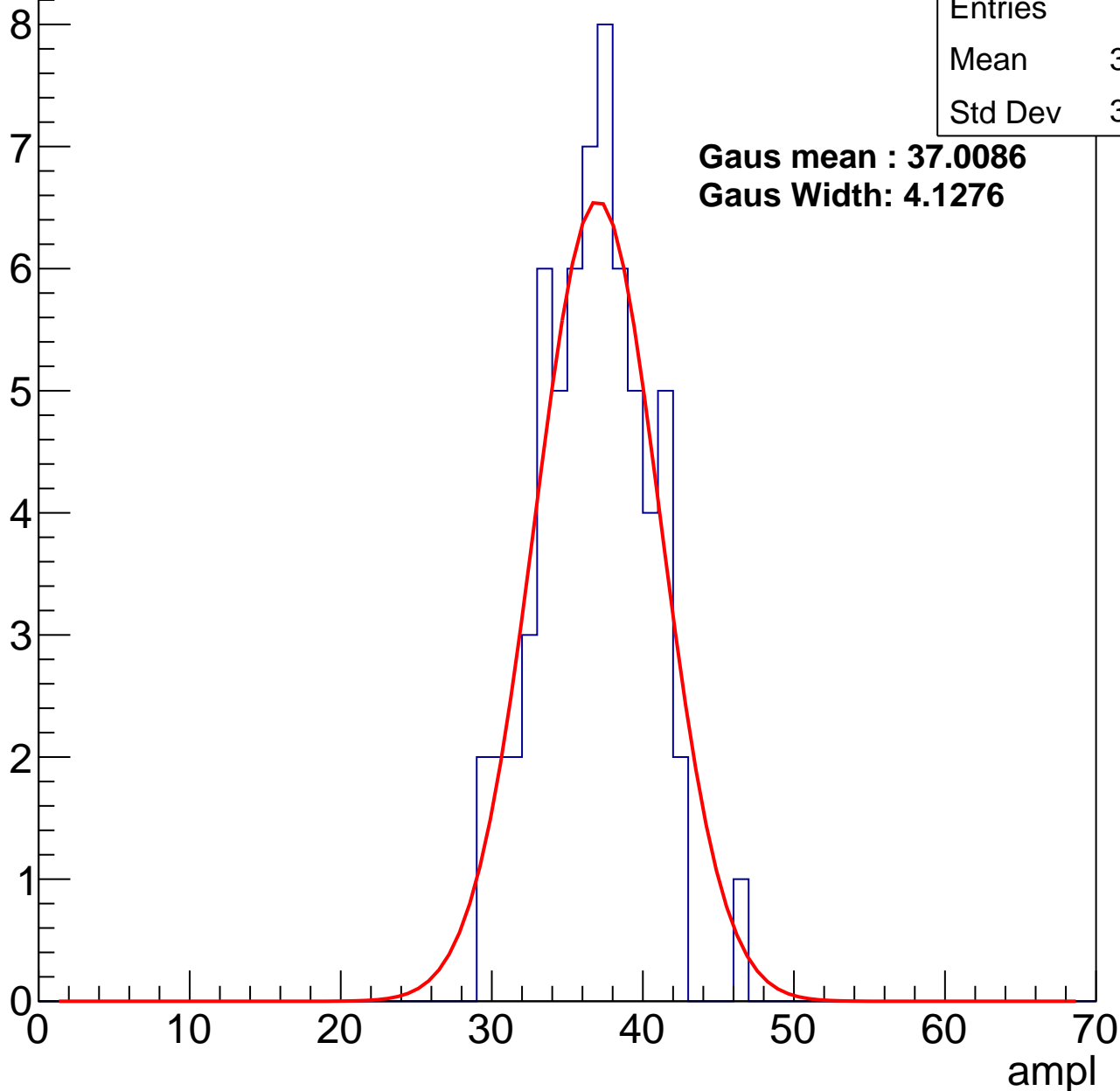
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	64
Mean	36.25
Std Dev	3.496

**Gaus mean : 37.0086**

**Gaus Width: 4.1276**



# B0L000S, U7-ch92, adc2

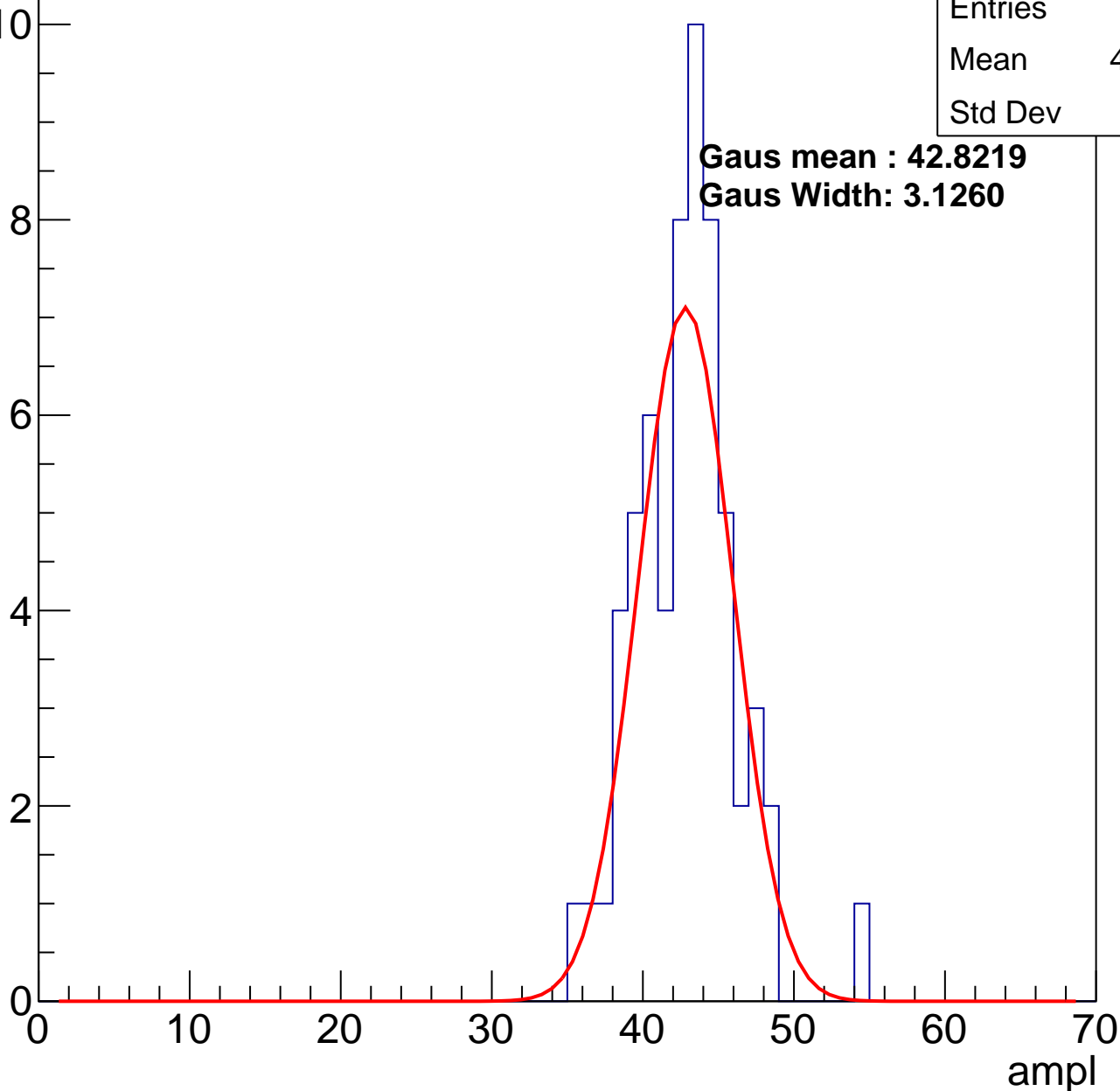
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	61
Mean	42.38
Std Dev	3.26

**Gaus mean : 42.8219**

**Gaus Width: 3.1260**

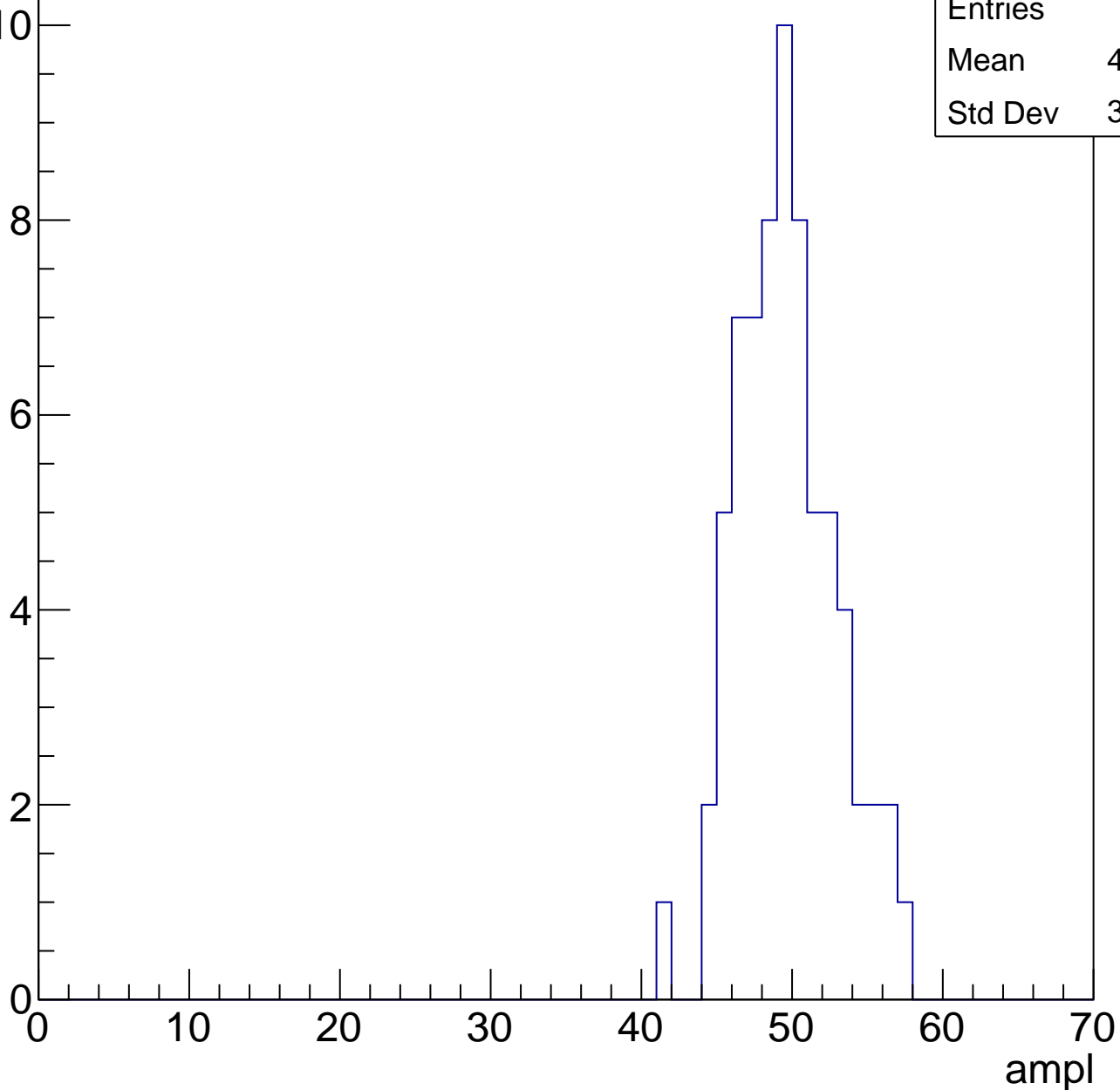


# B0L000S, U7-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	69
Mean	49.17
Std Dev	3.212

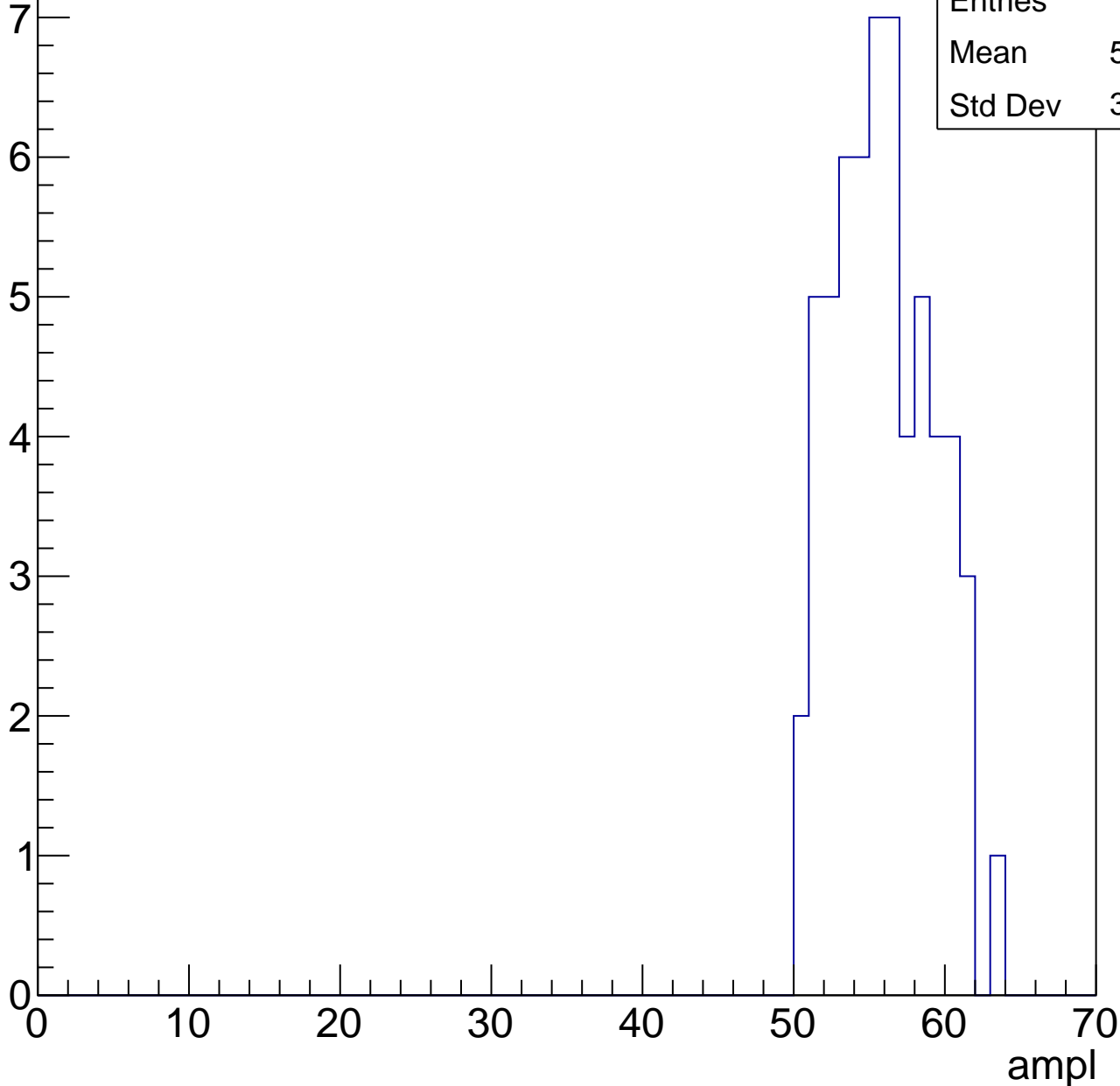


# B0L000S, U7-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	59
Mean	55.49
Std Dev	3.175

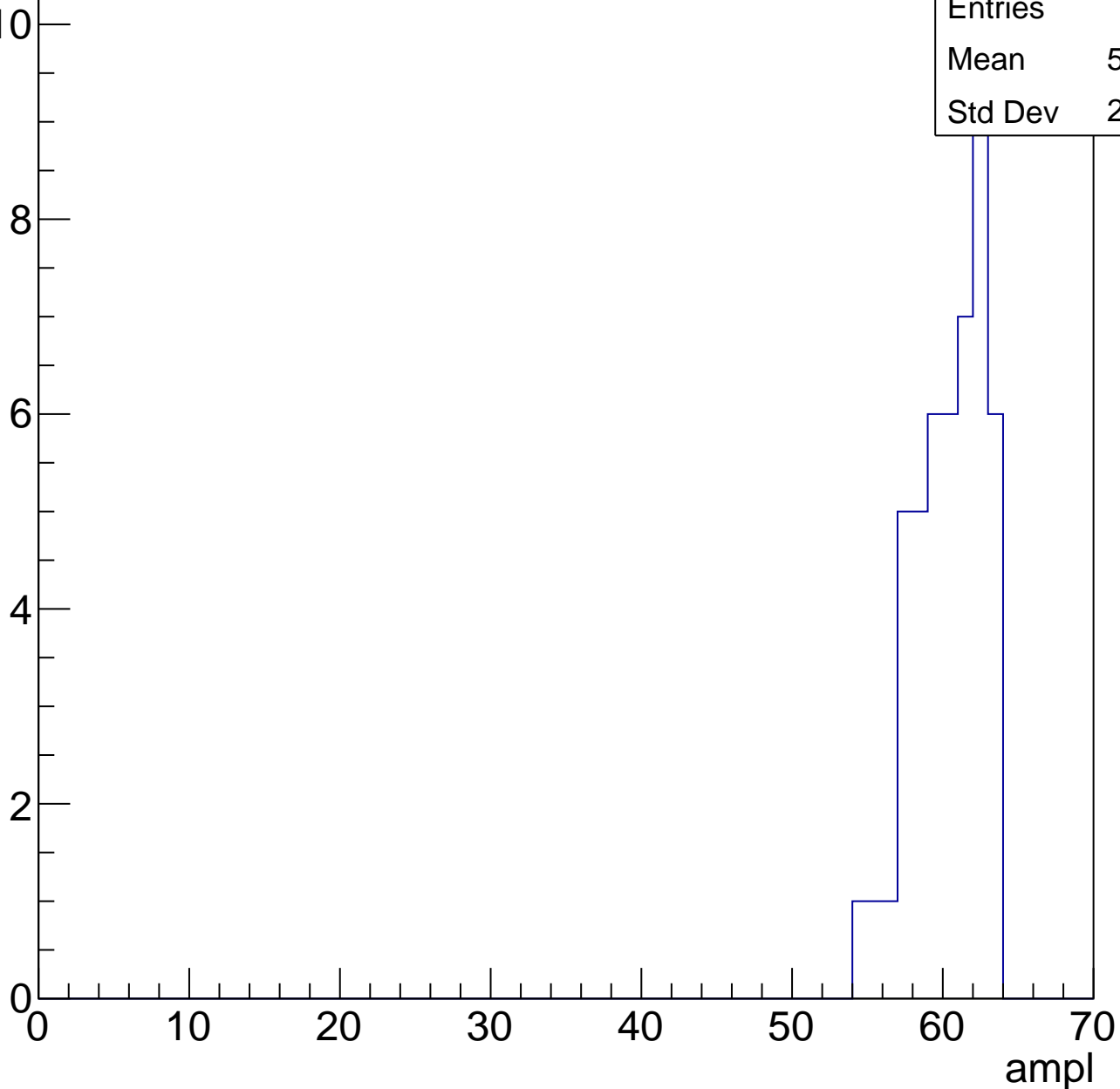


# B0L000S, U7-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

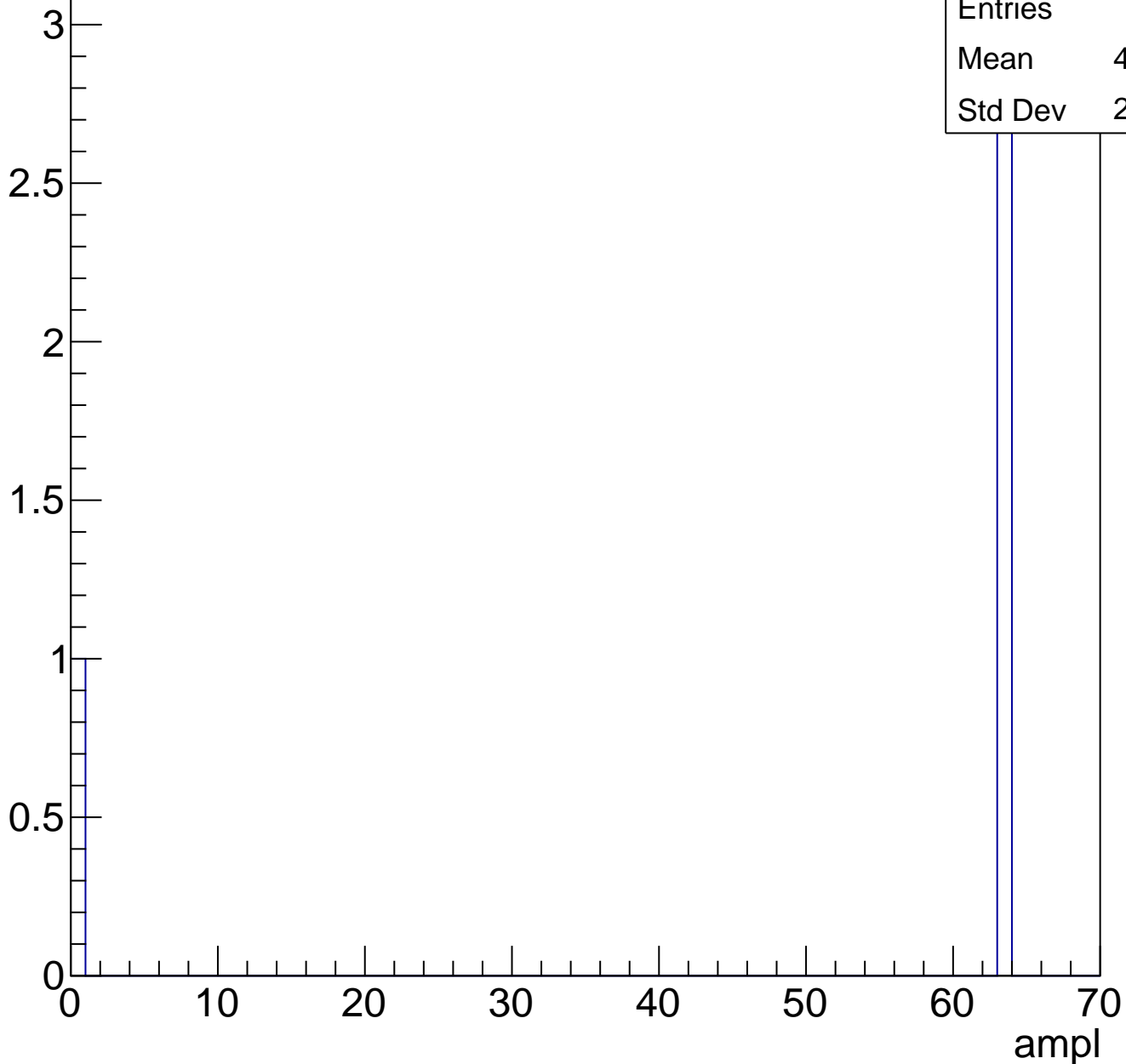
Entries	48
Mean	59.98
Std Dev	2.278



# B0L000S, U7-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L000S, U7-ch93, adc0

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	91
Mean	30.41
Std Dev	4.756

**Gaus mean : 30.9578**

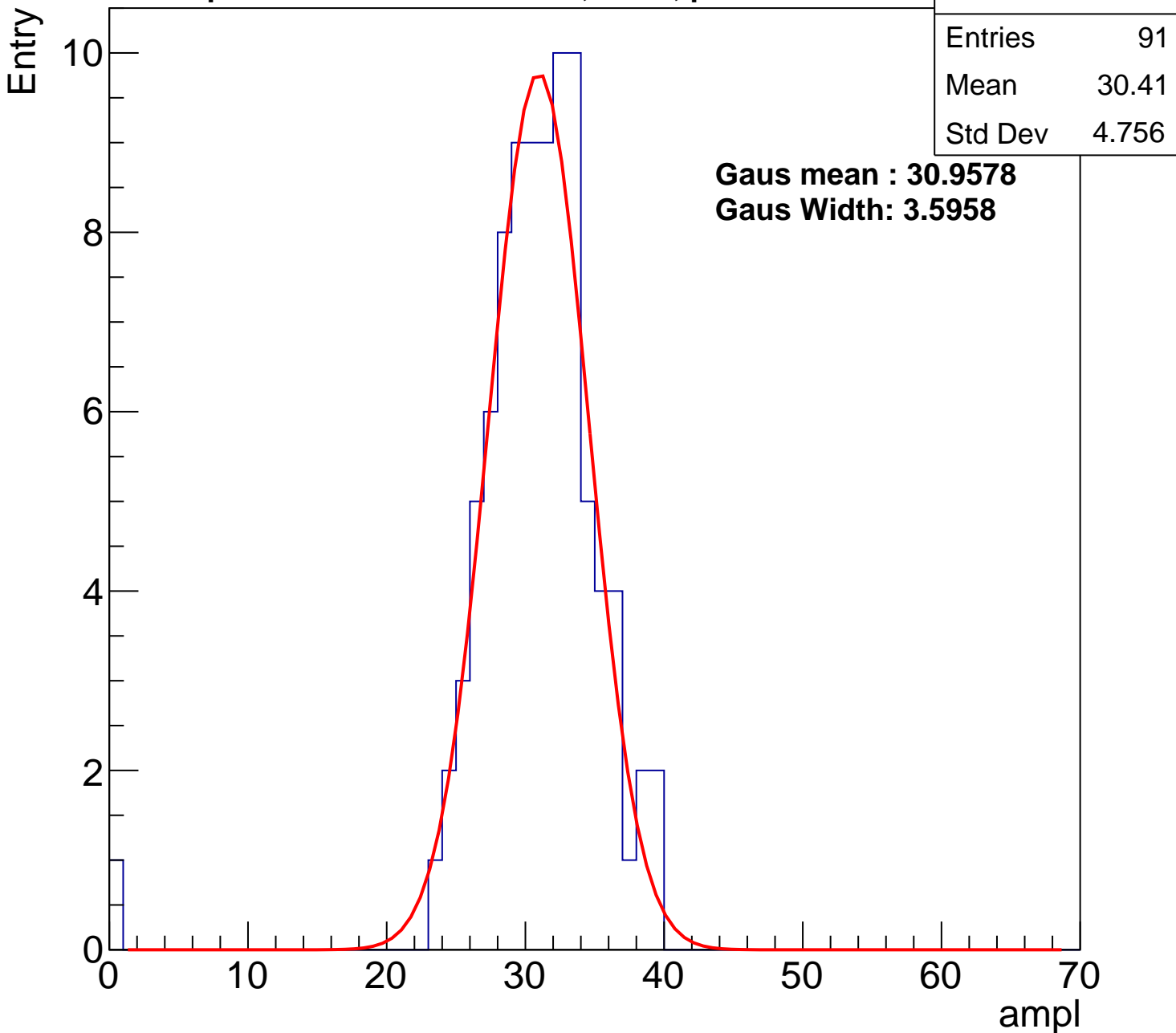
**Gaus Width: 3.5958**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L000S, U7-ch93, adc1

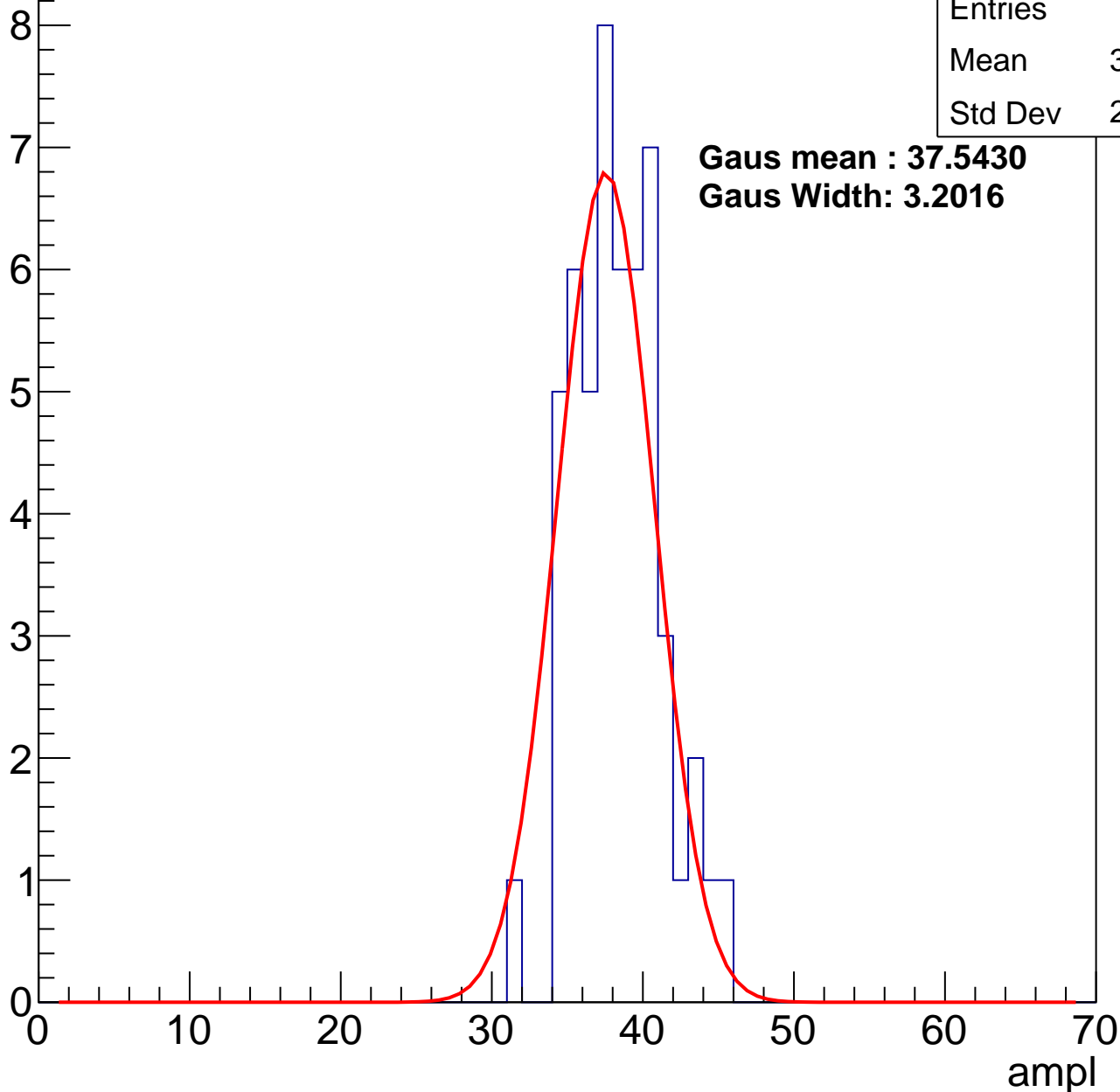
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	52
Mean	37.87
Std Dev	2.849

**Gaus mean : 37.5430**

**Gaus Width: 3.2016**

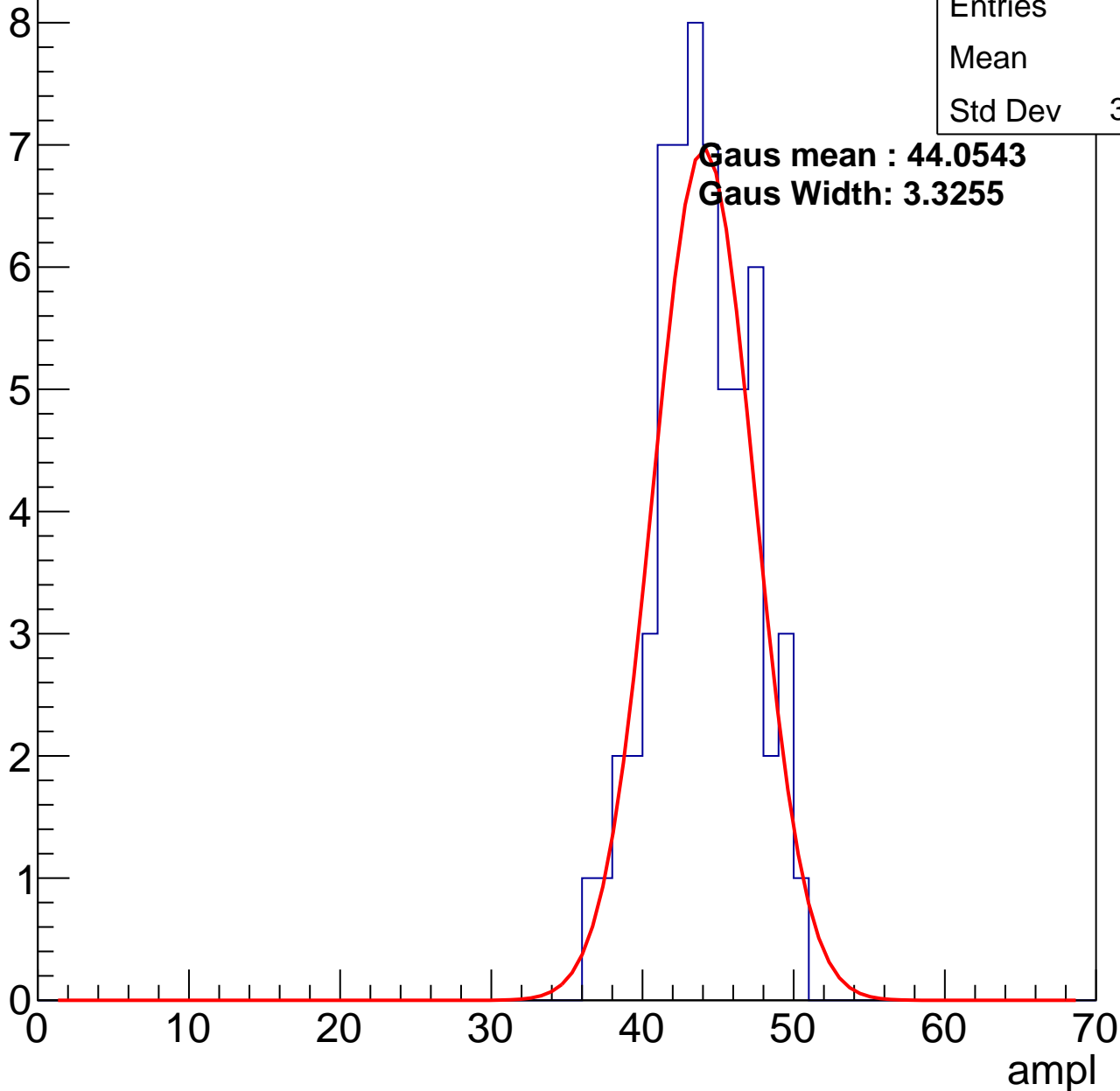


# B0L000S, U7-ch93, adc2

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	60
Mean	43.5
Std Dev	3.133

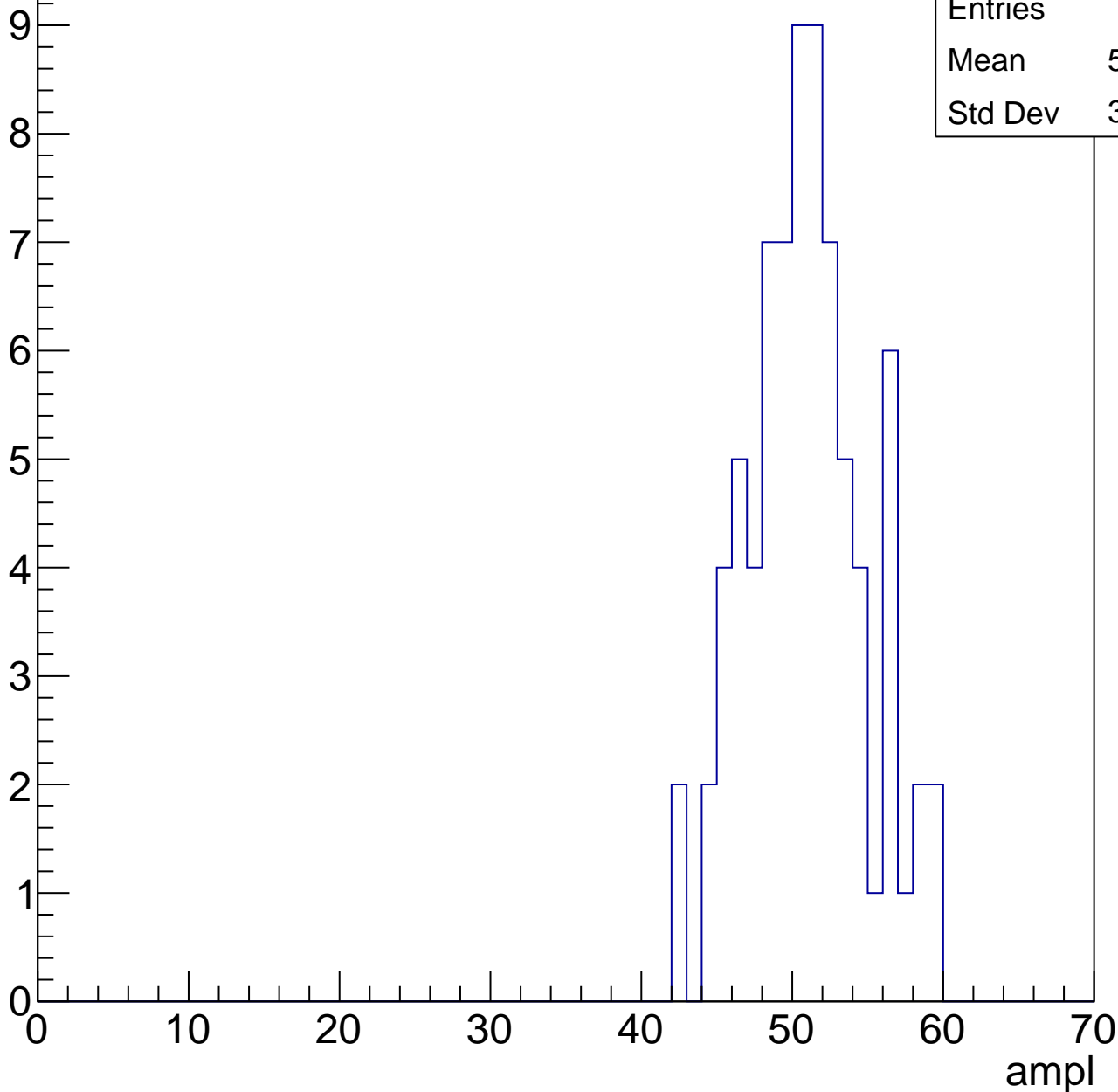


# B0L000S, U7-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	77
Mean	50.45
Std Dev	3.883

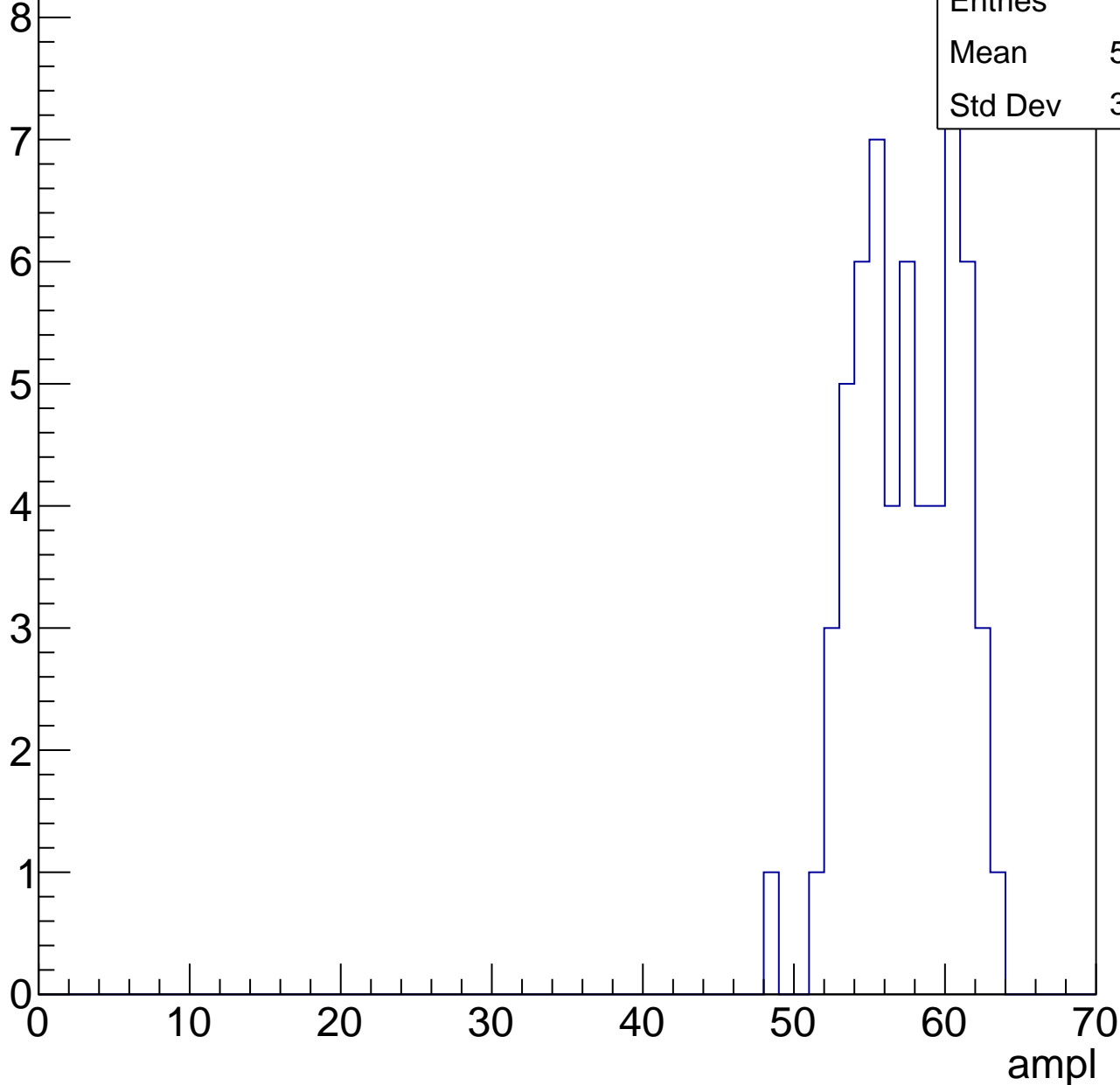


# B0L000S, U7-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	59
Mean	56.92
Std Dev	3.336

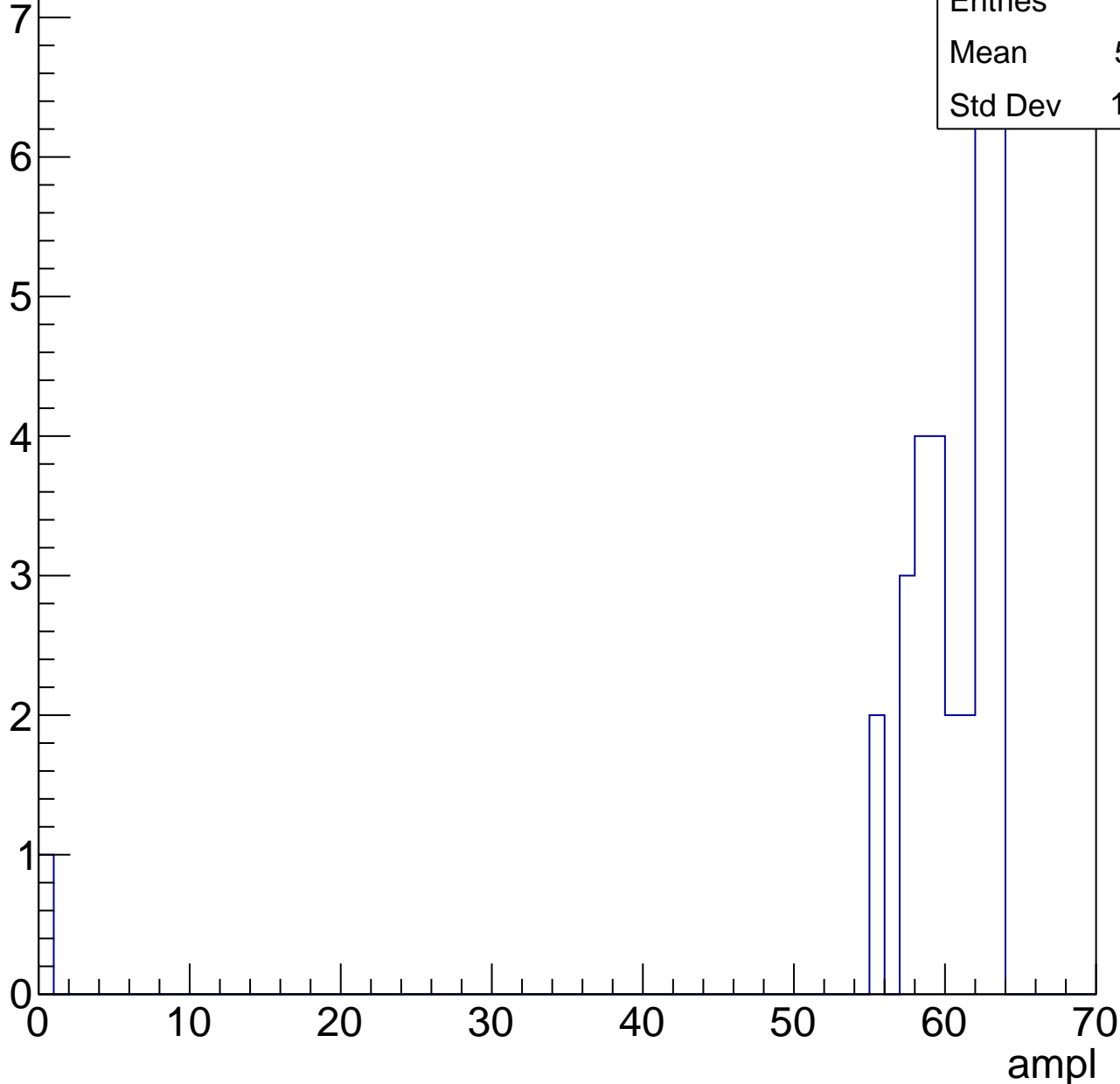


# B0L000S, U7-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	32
Mean	58.31
Std Dev	10.75



# B0L000S, U7-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

0

10

20

30

40

50

60

70

ampl

Entries

4

Mean

62

Std Dev

1



# B0L000S, U7-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch94, adc0

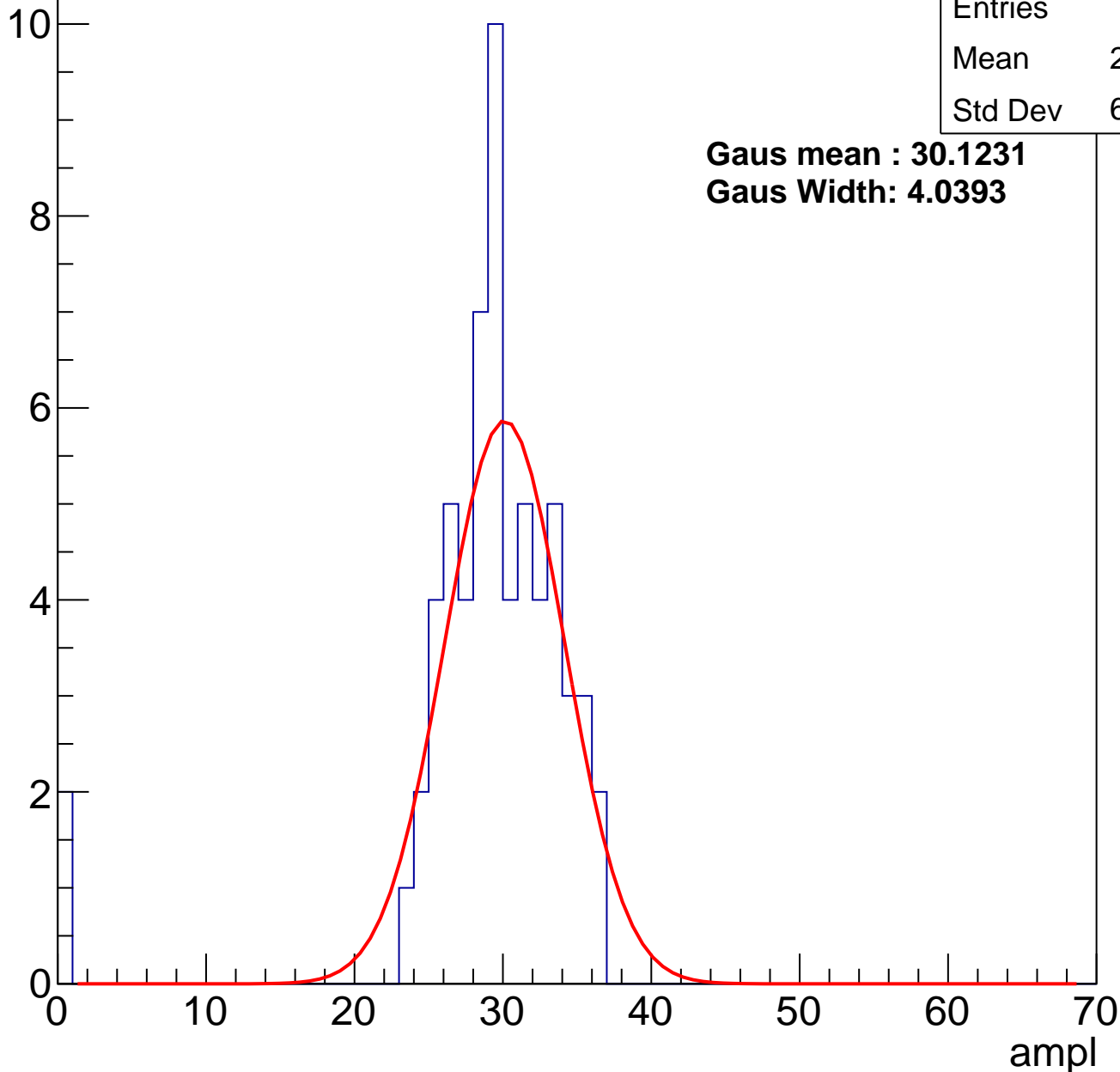
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	61
Mean	28.56
Std Dev	6.153

**Gaus mean : 30.1231**

**Gaus Width: 4.0393**

Entry



# B0L000S, U7-ch94, adc1

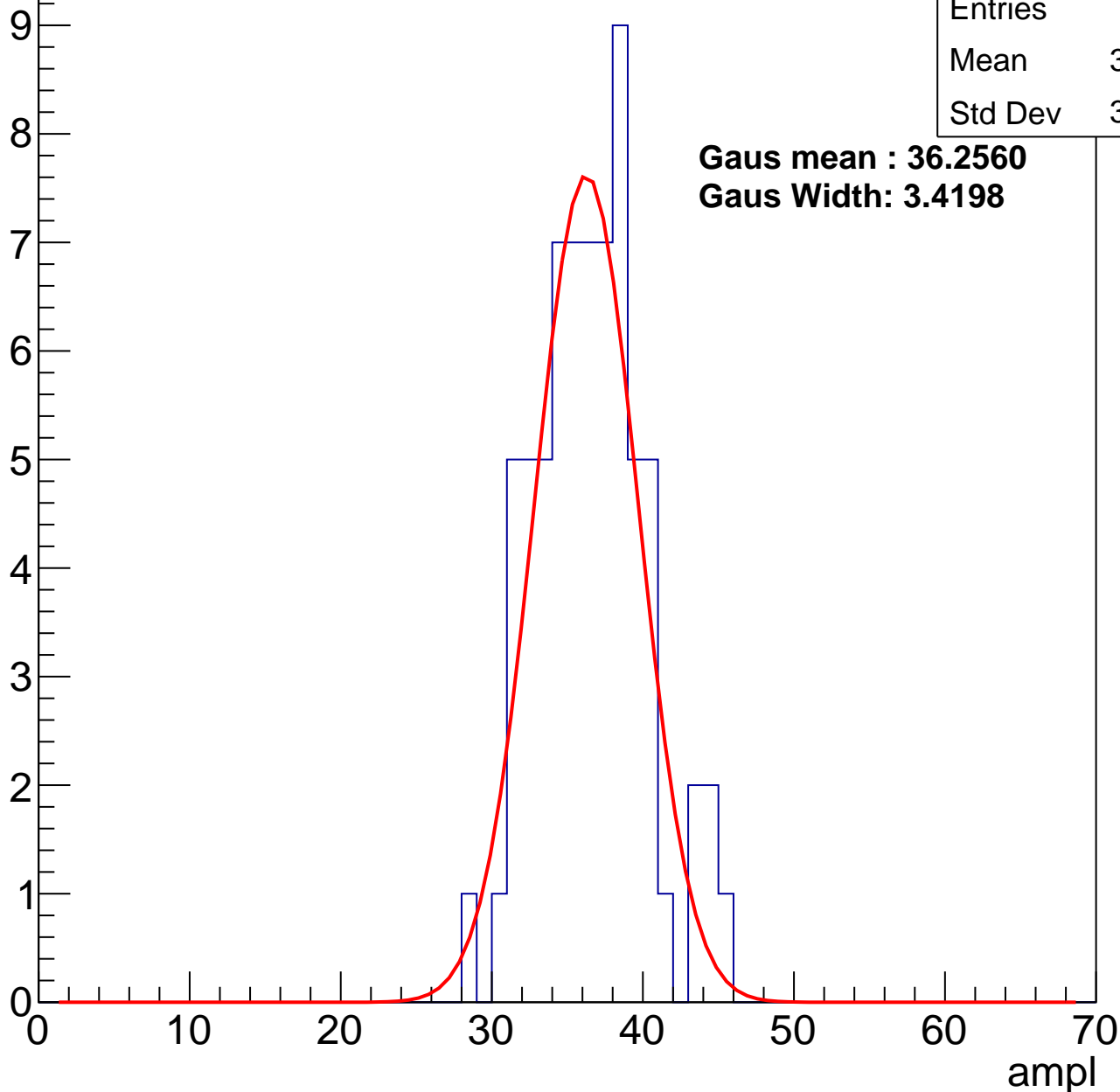
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	70
Mean	36.13
Std Dev	3.553

**Gaus mean : 36.2560**

**Gaus Width: 3.4198**



# B0L000S, U7-ch94, adc2

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	62
Mean	42.48
Std Dev	3.083

**Gaus mean : 43.0006**

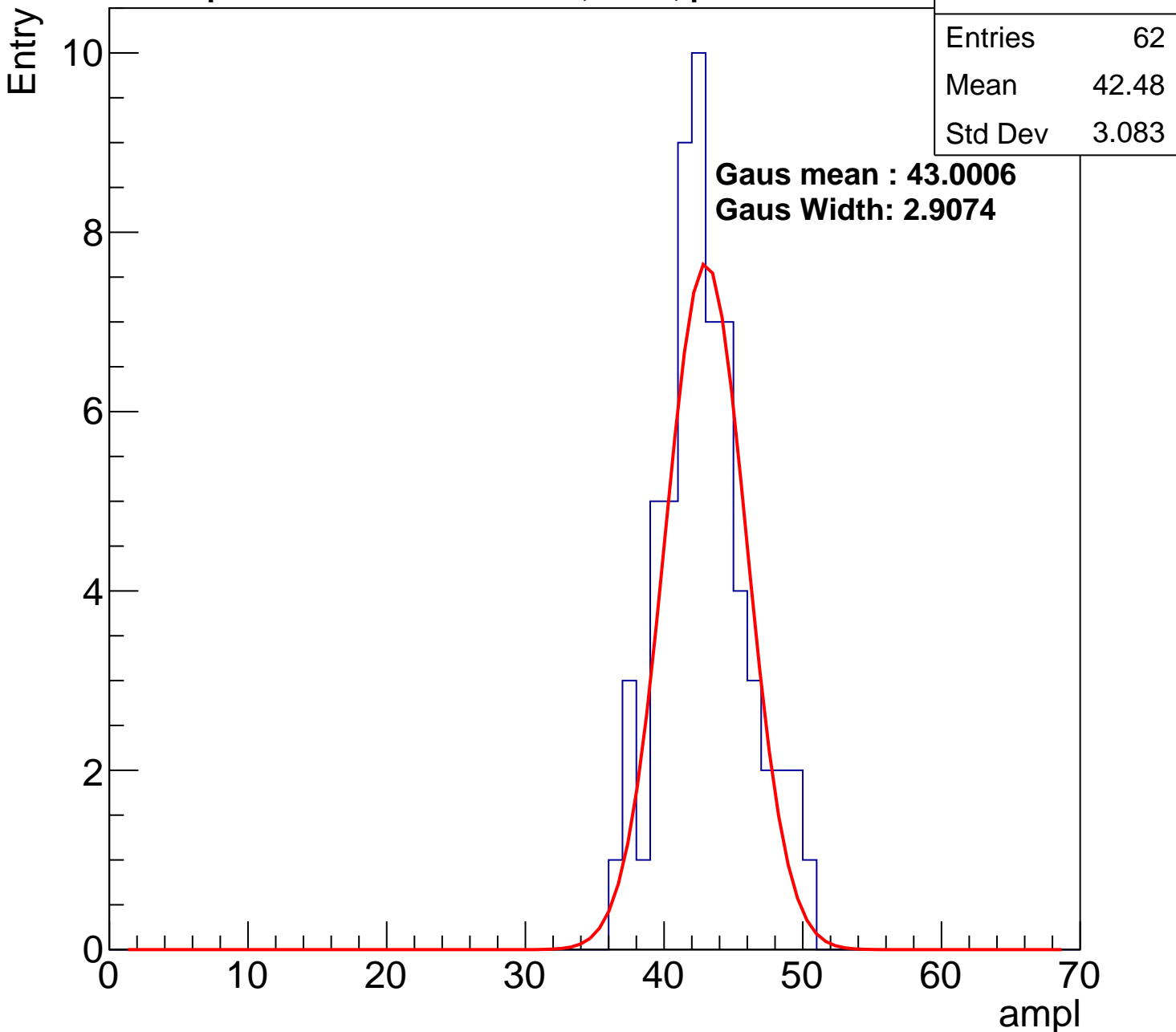
**Gaus Width: 2.9074**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

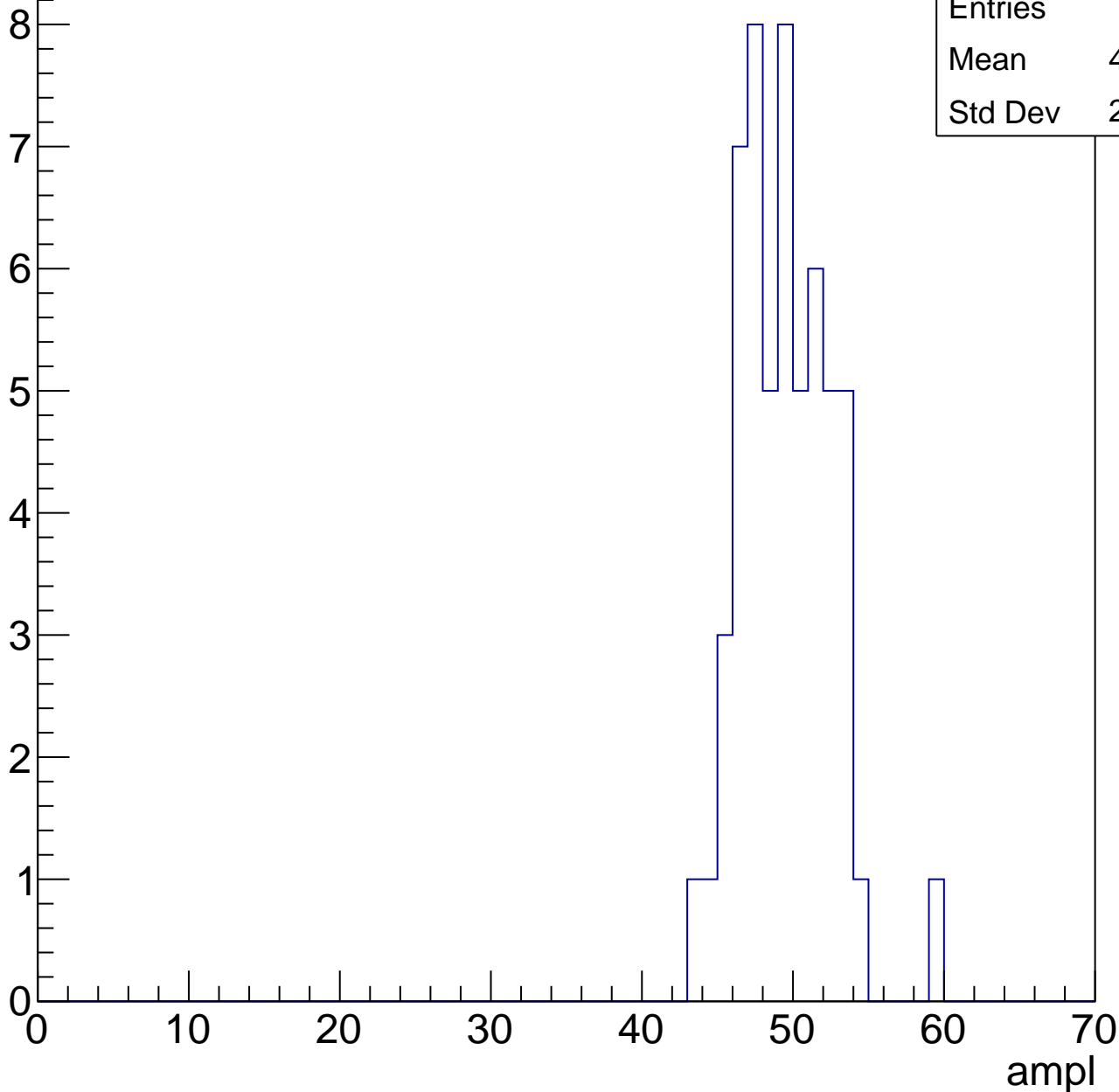


# B0L000S, U7-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	56
Mean	49.04
Std Dev	2.952

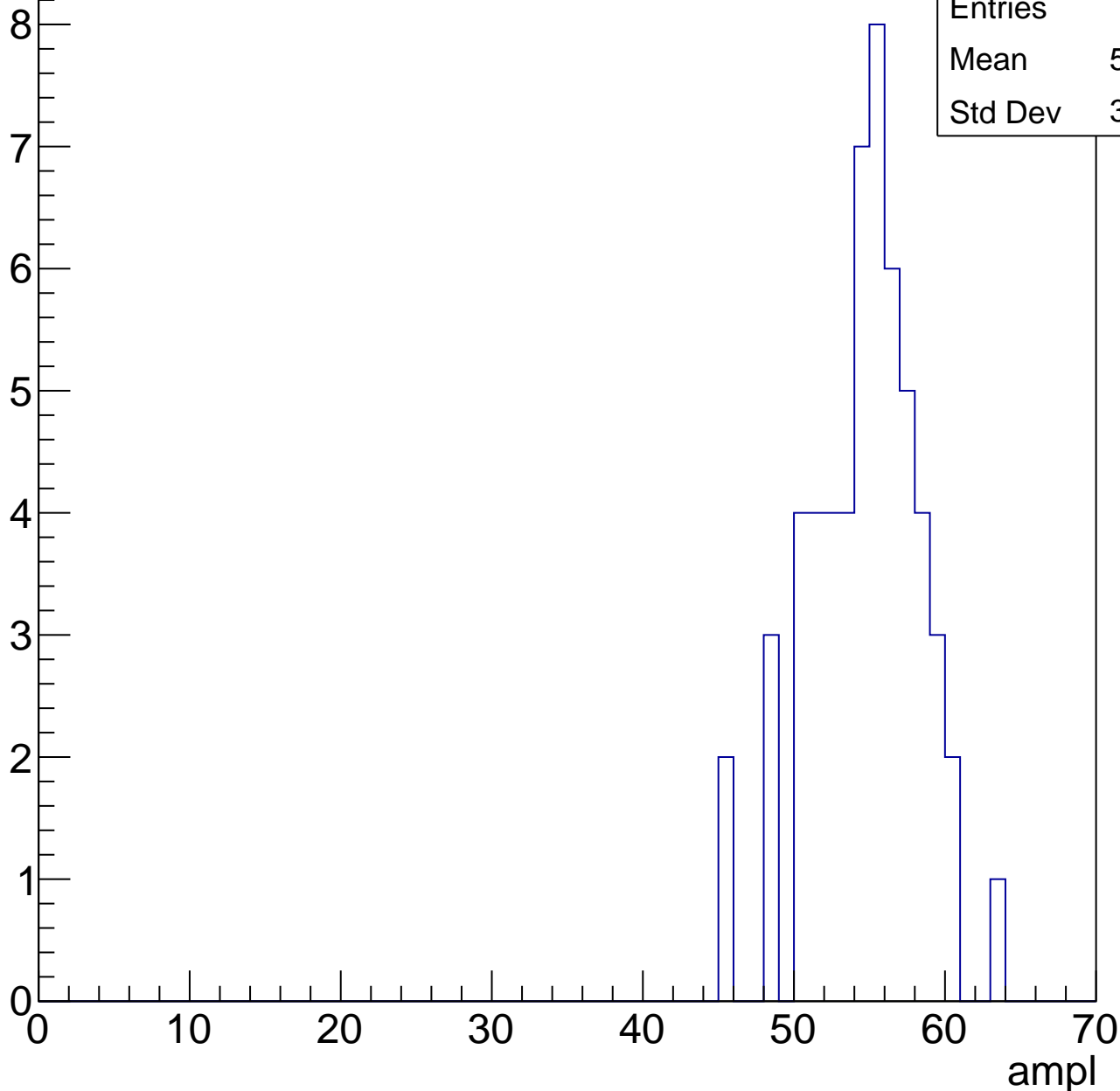


# B0L000S, U7-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

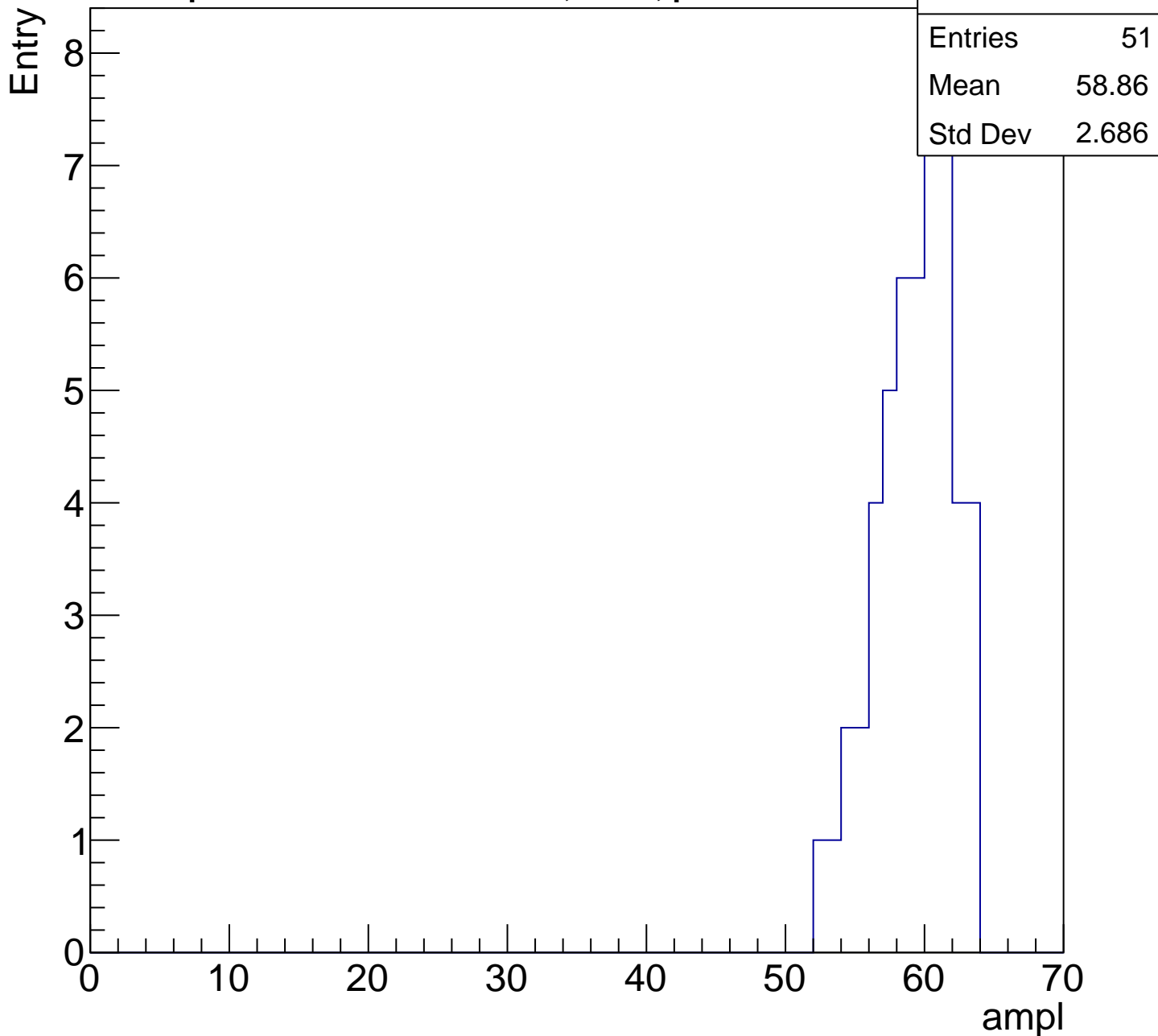
Entry

Entries	57
Mean	54.19
Std Dev	3.644



# B0L000S, U7-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

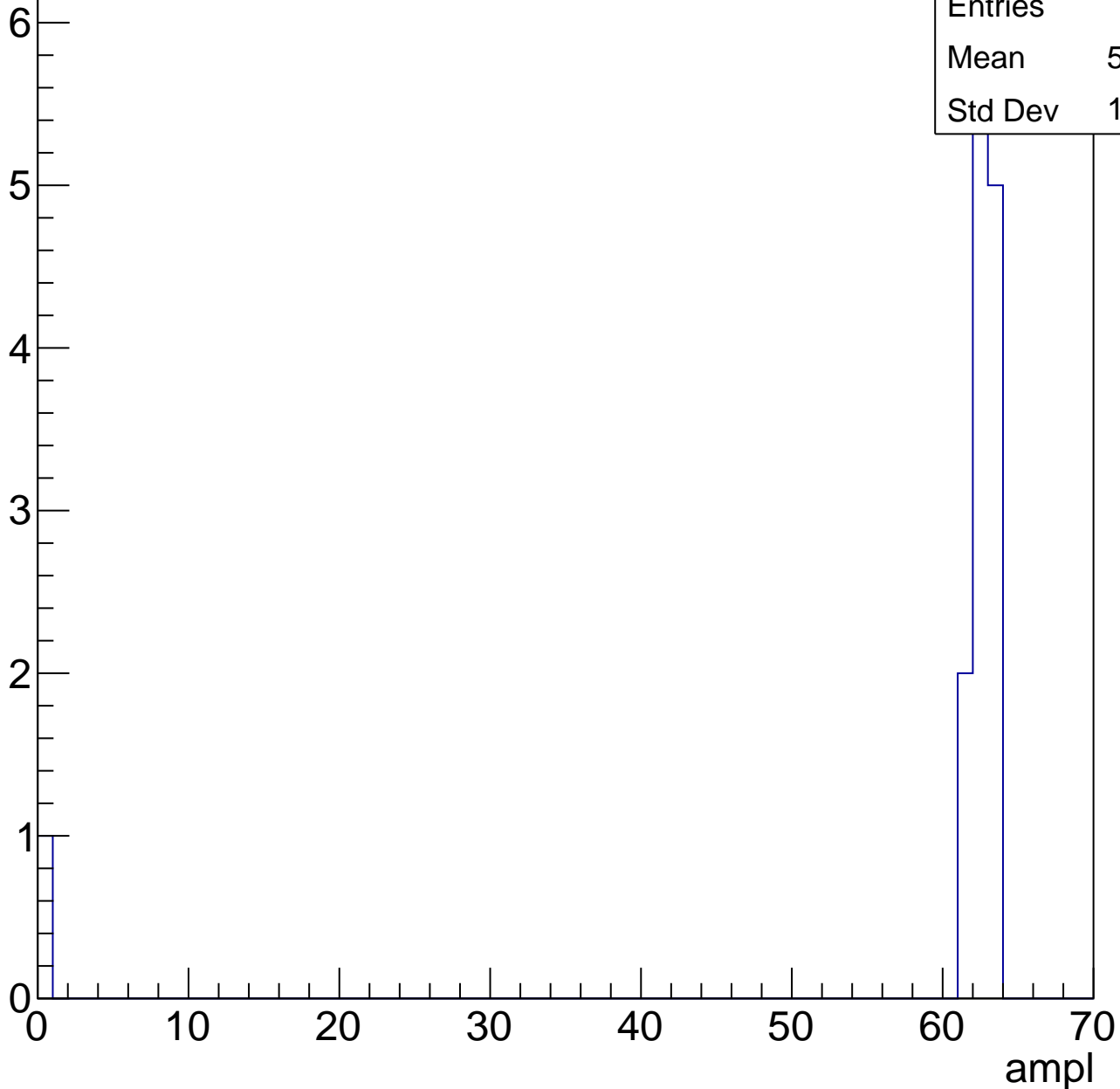


# B0L000S, U7-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	14
Mean	57.79
Std Dev	16.04





# B0L000S, U7-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

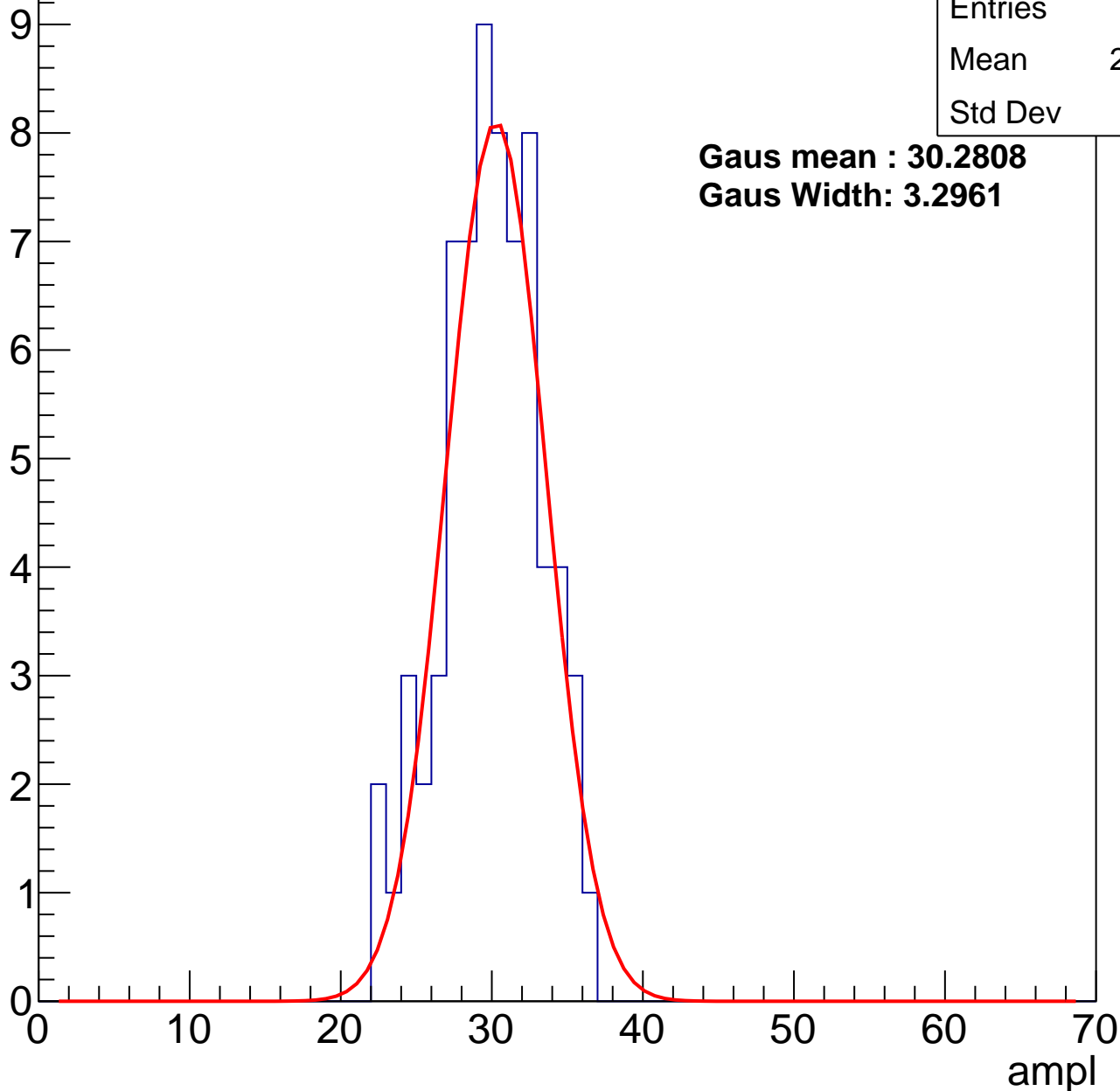


Entries	1
Mean	0
Std Dev	0

# B0L000S, U7-ch95, adc0

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch95, adc1

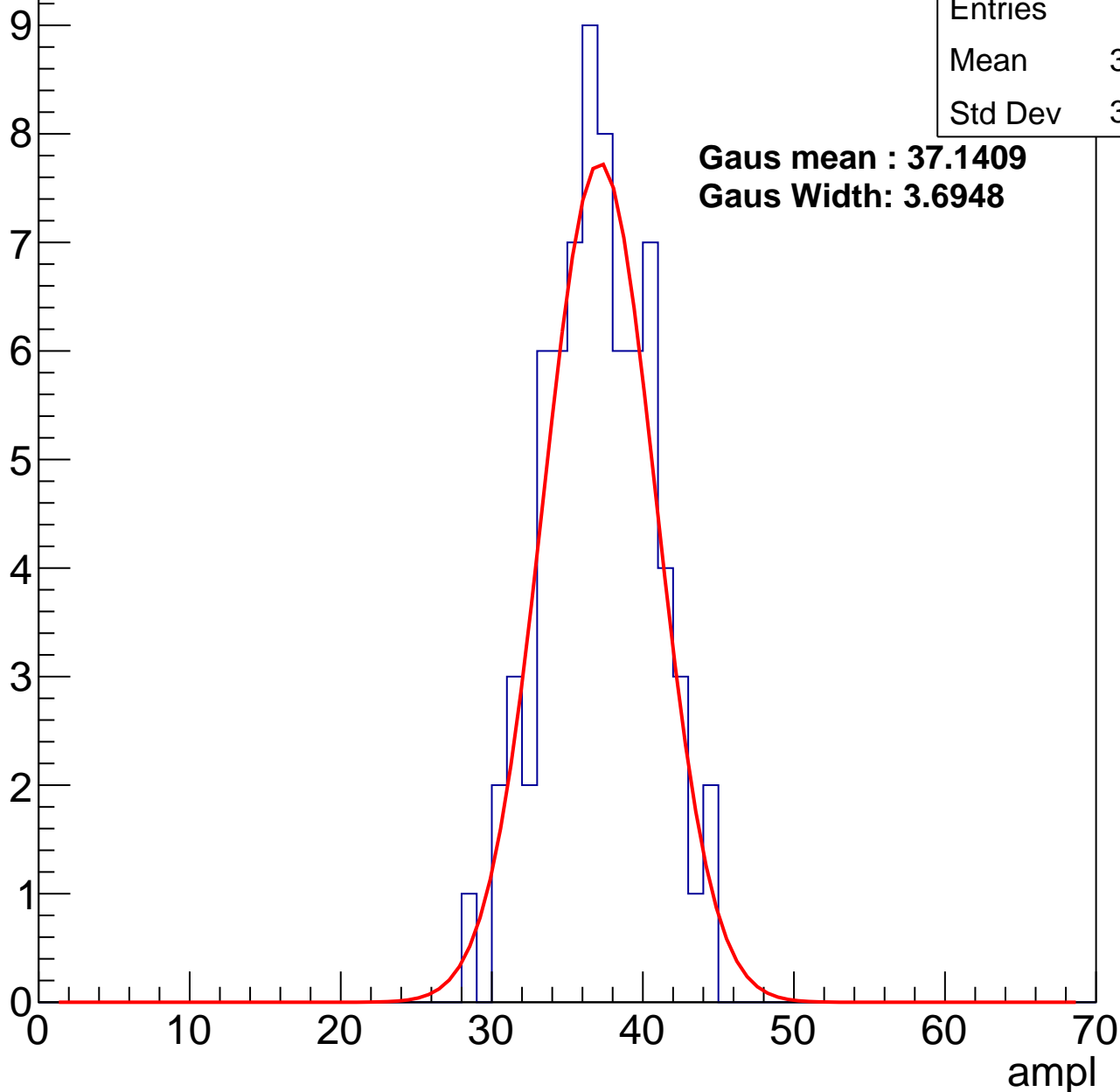
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	73
Mean	36.64
Std Dev	3.473

**Gaus mean : 37.1409**

**Gaus Width: 3.6948**



# B0L000S, U7-ch95, adc2

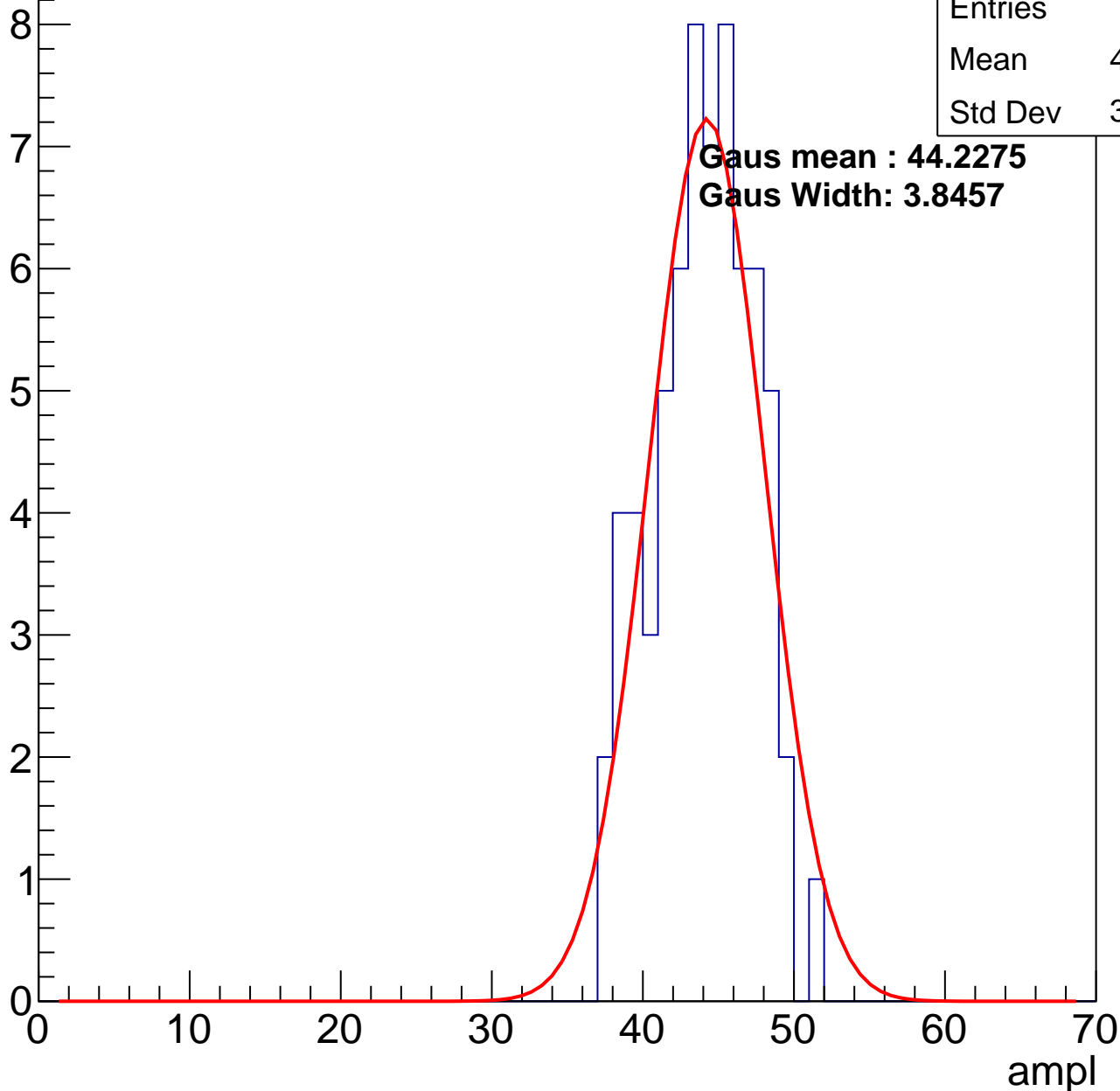
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	67
Mean	43.55
Std Dev	3.275

**Gaus mean : 44.2275**

**Gaus Width: 3.8457**

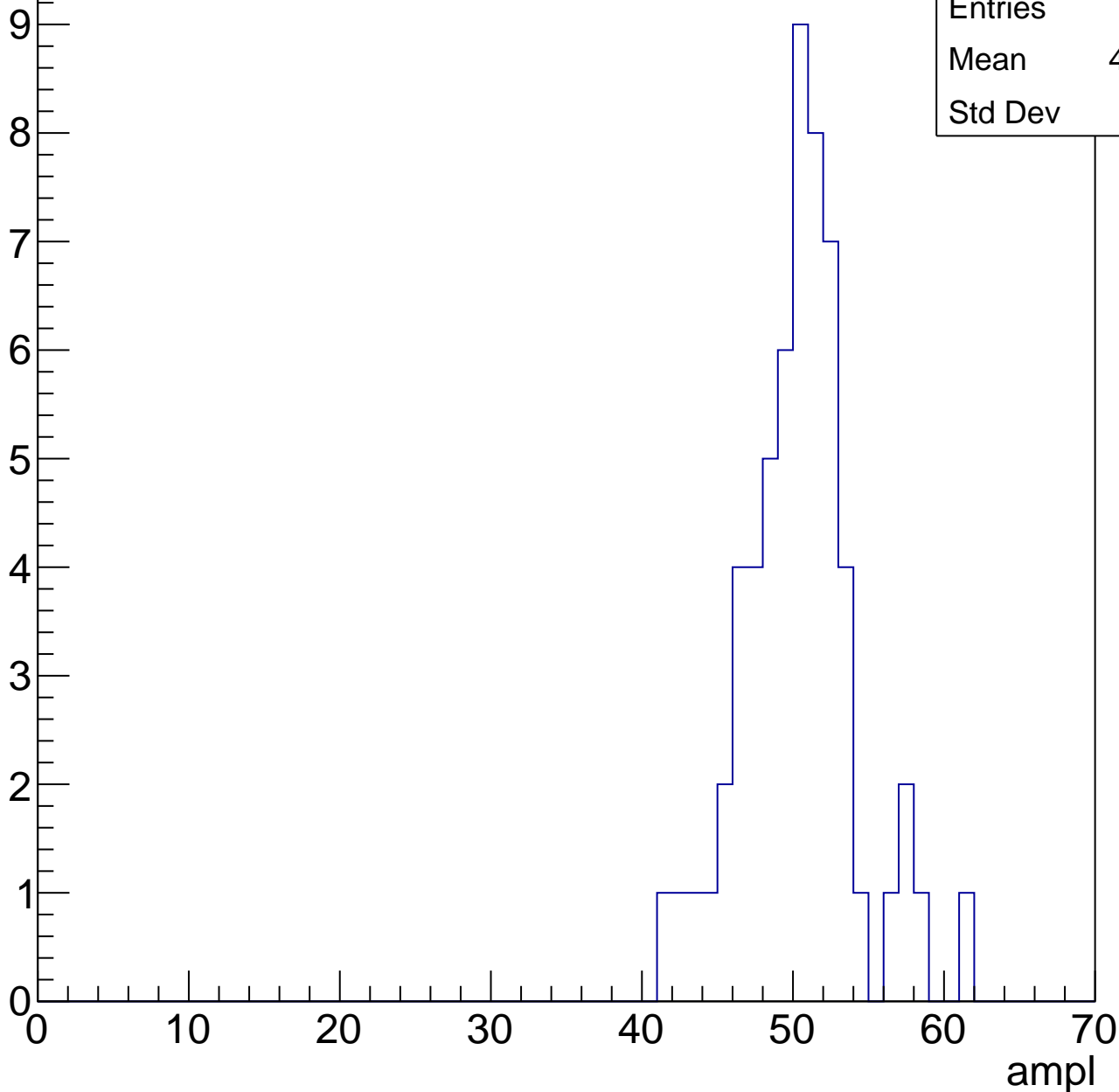


# B0L000S, U7-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	59
Mean	49.88
Std Dev	3.71



# B0L000S, U7-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

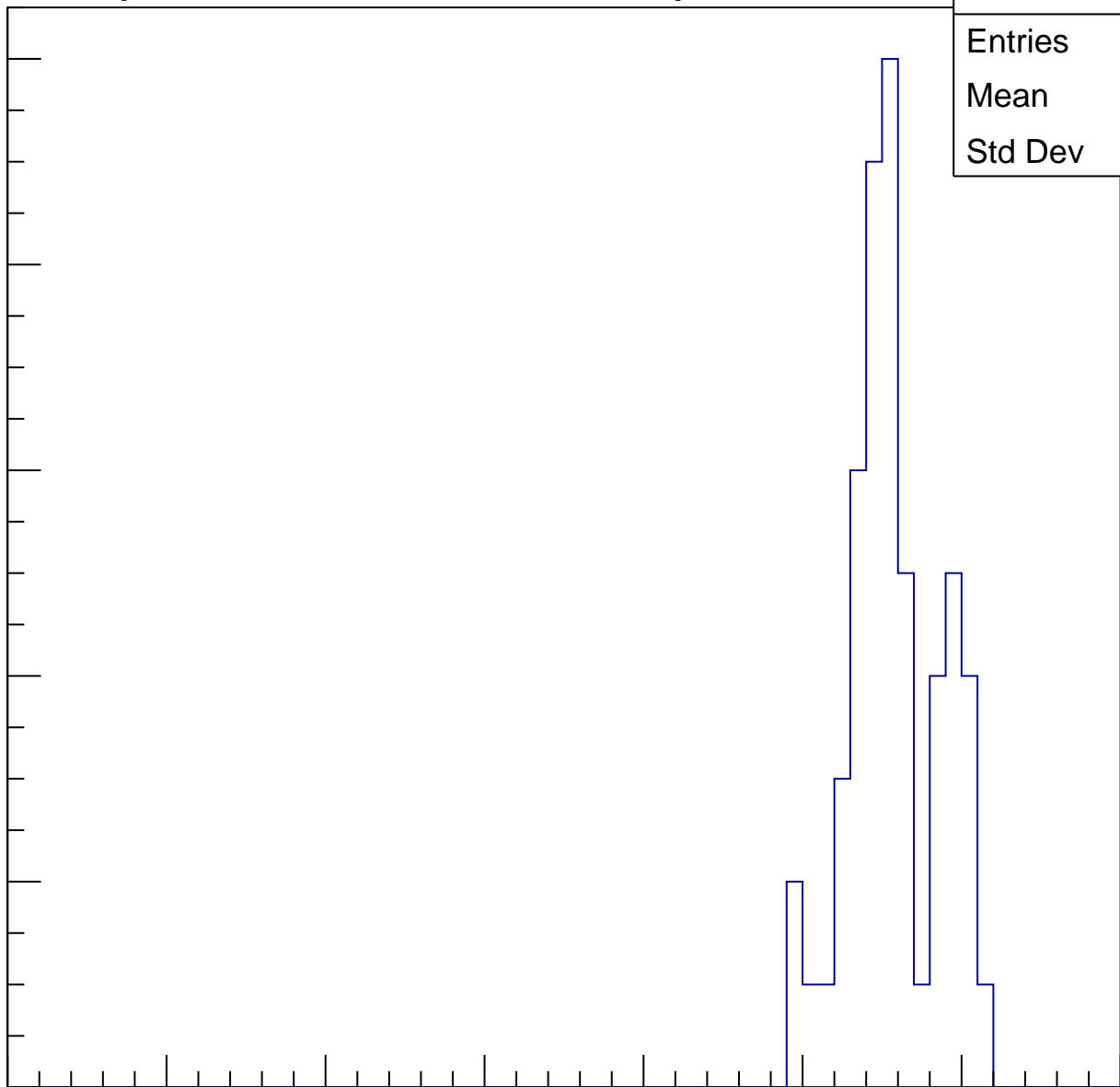
Entries	52
Mean	55.27
Std Dev	2.876

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

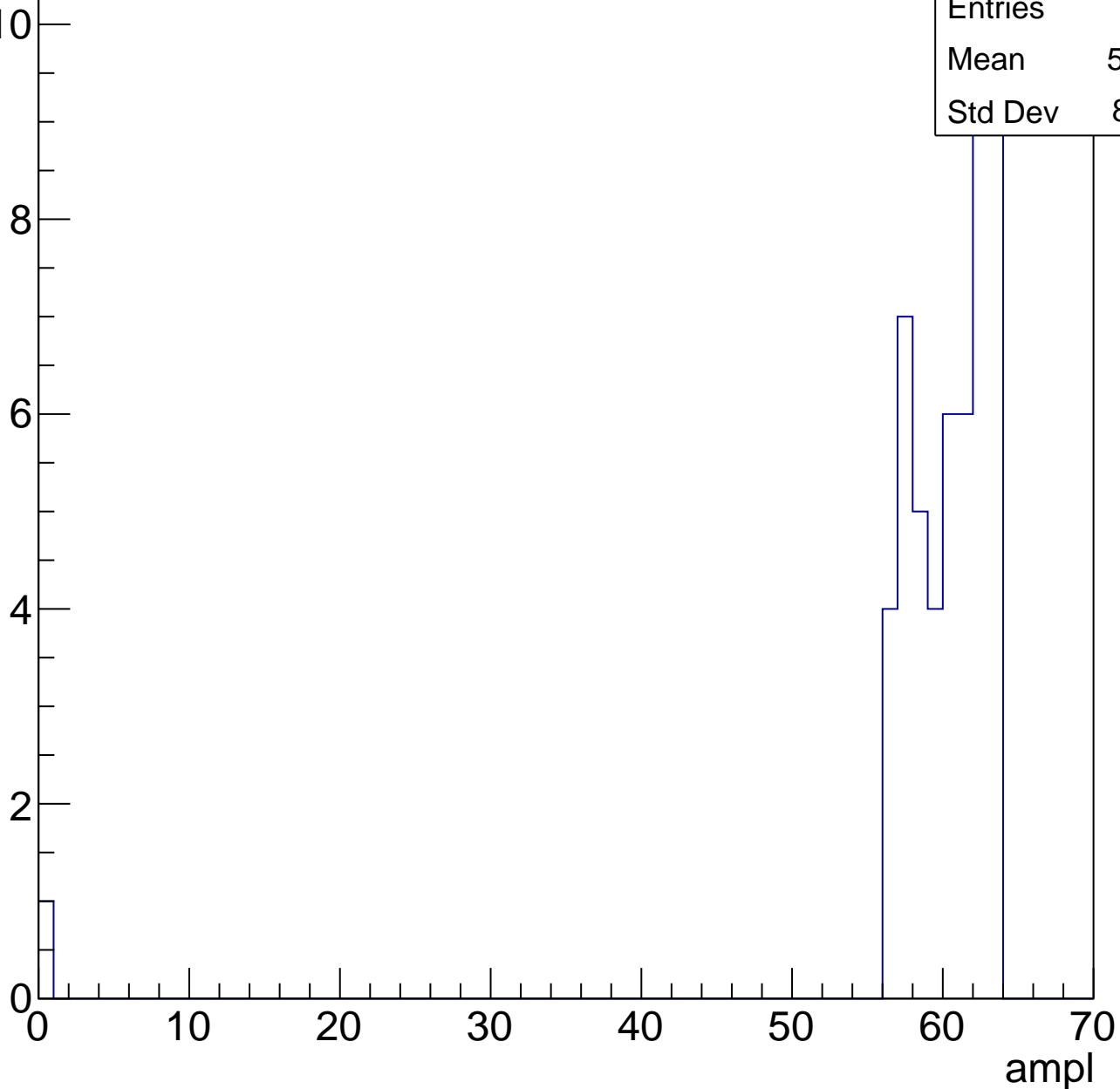


# B0L000S, U7-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

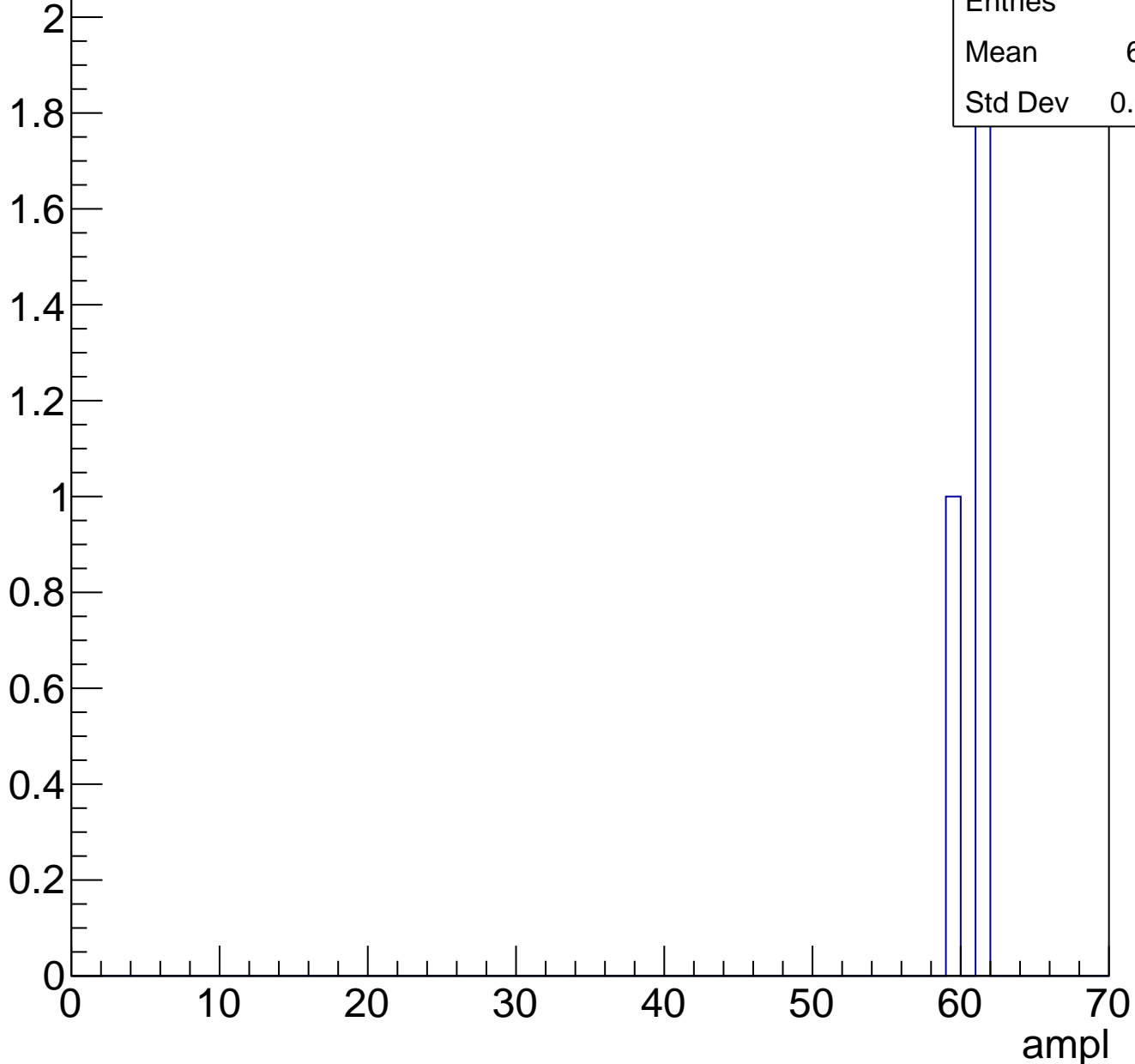
Entries	53
Mean	58.96
Std Dev	8.501



# B0L000S, U7-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L000S, U7-ch96, adc0

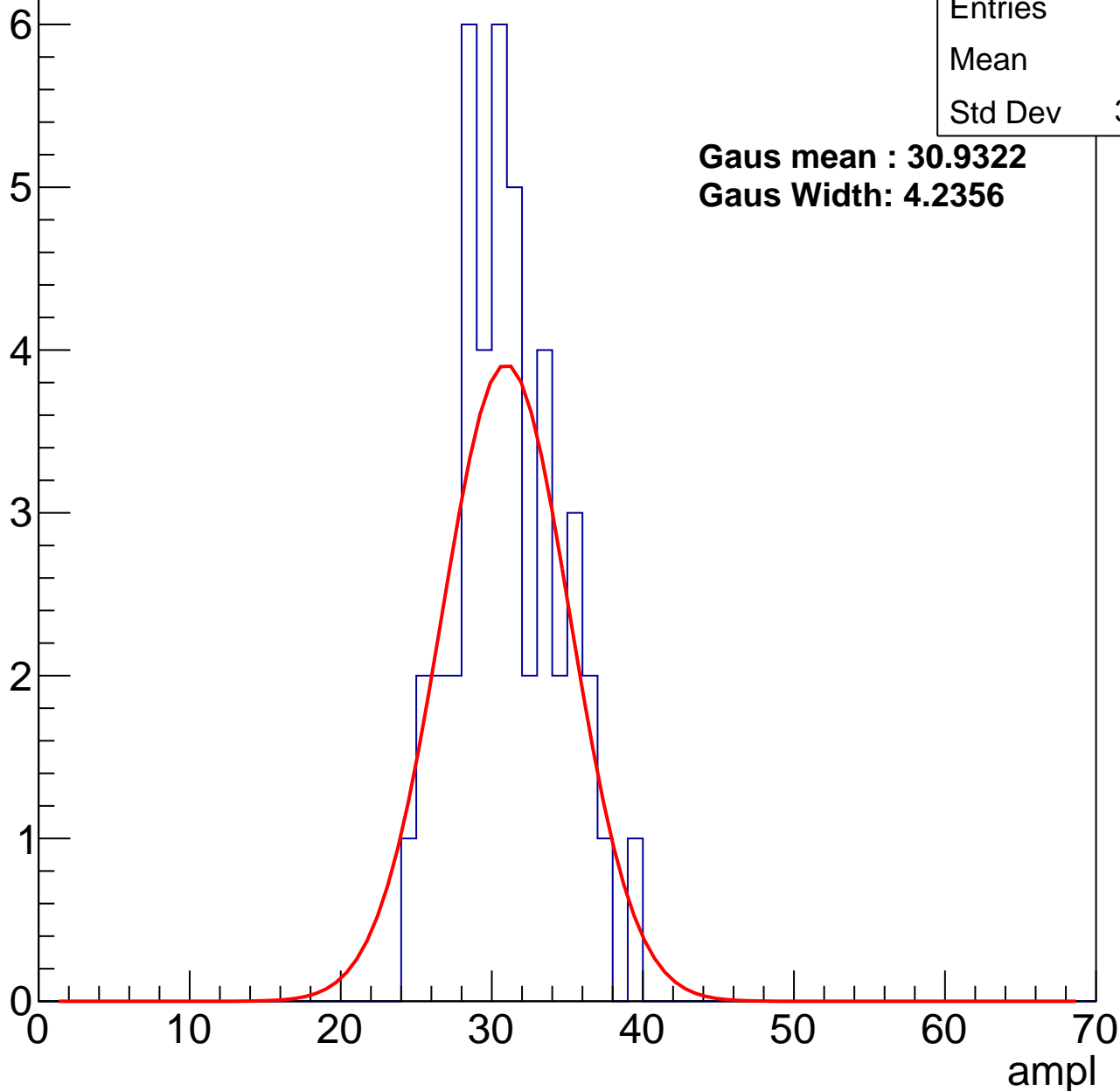
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	43
Mean	30.6
Std Dev	3.431

**Gaus mean : 30.9322**

**Gaus Width: 4.2356**



# B0L000S, U7-ch96, adc1

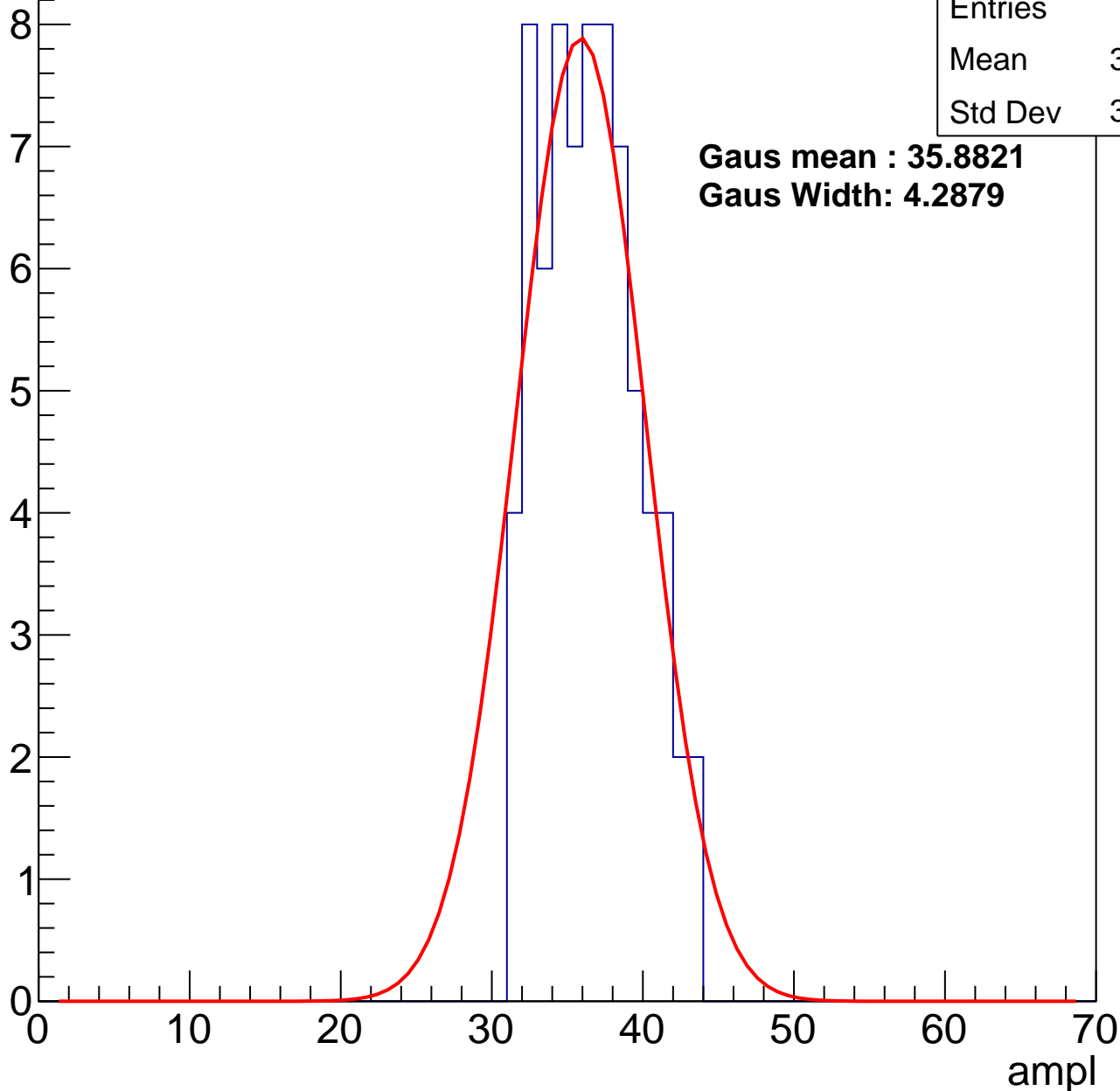
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	73
Mean	36.08
Std Dev	3.174

**Gaus mean : 35.8821**

**Gaus Width: 4.2879**

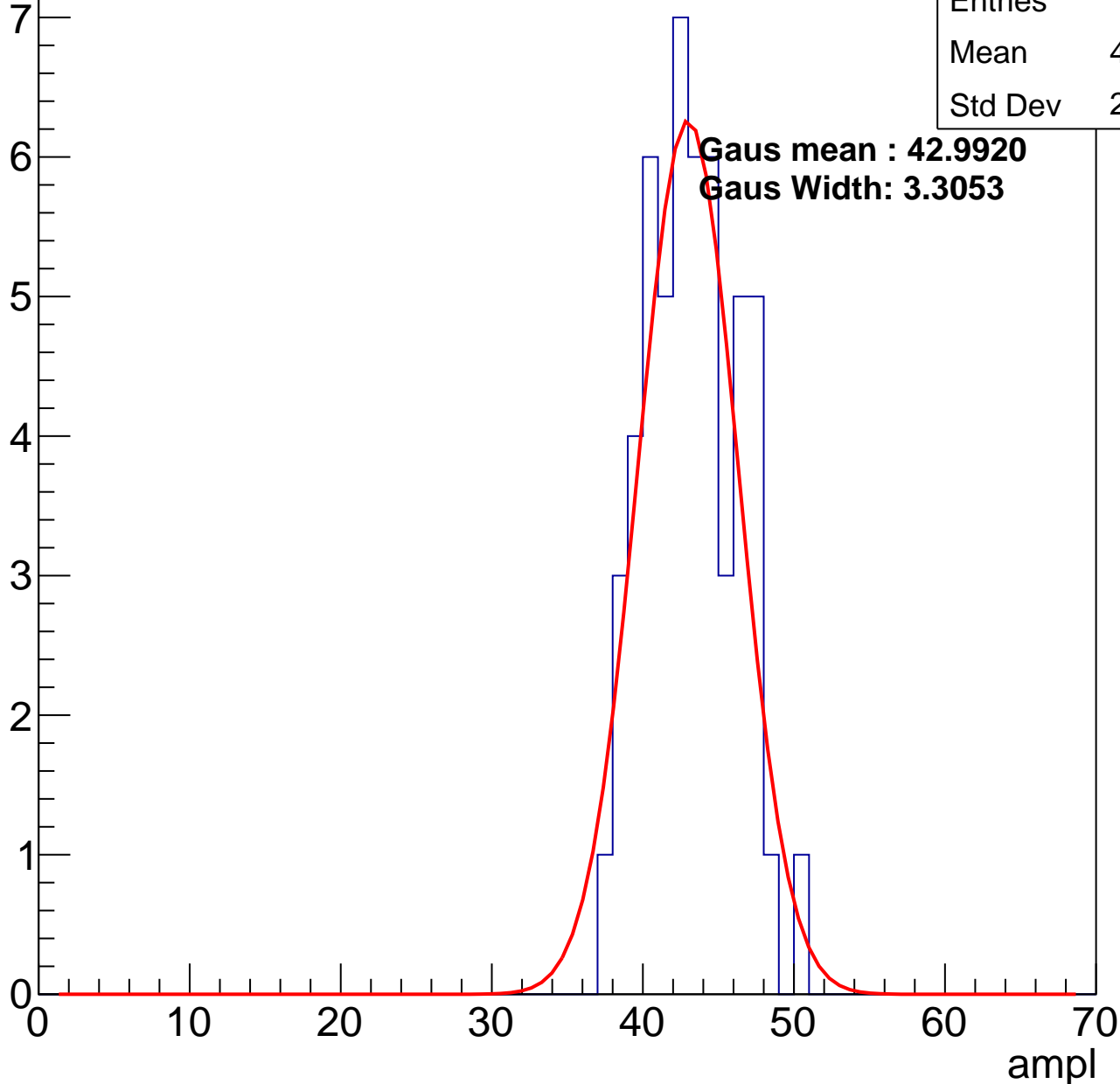


# B0L000S, U7-ch96, adc2

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	53
Mean	42.75
Std Dev	2.977



# B0L000S, U7-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	87
Mean	49.59
Std Dev	3.771

Entry

10

8

6

4

2

0

0

10

20

30

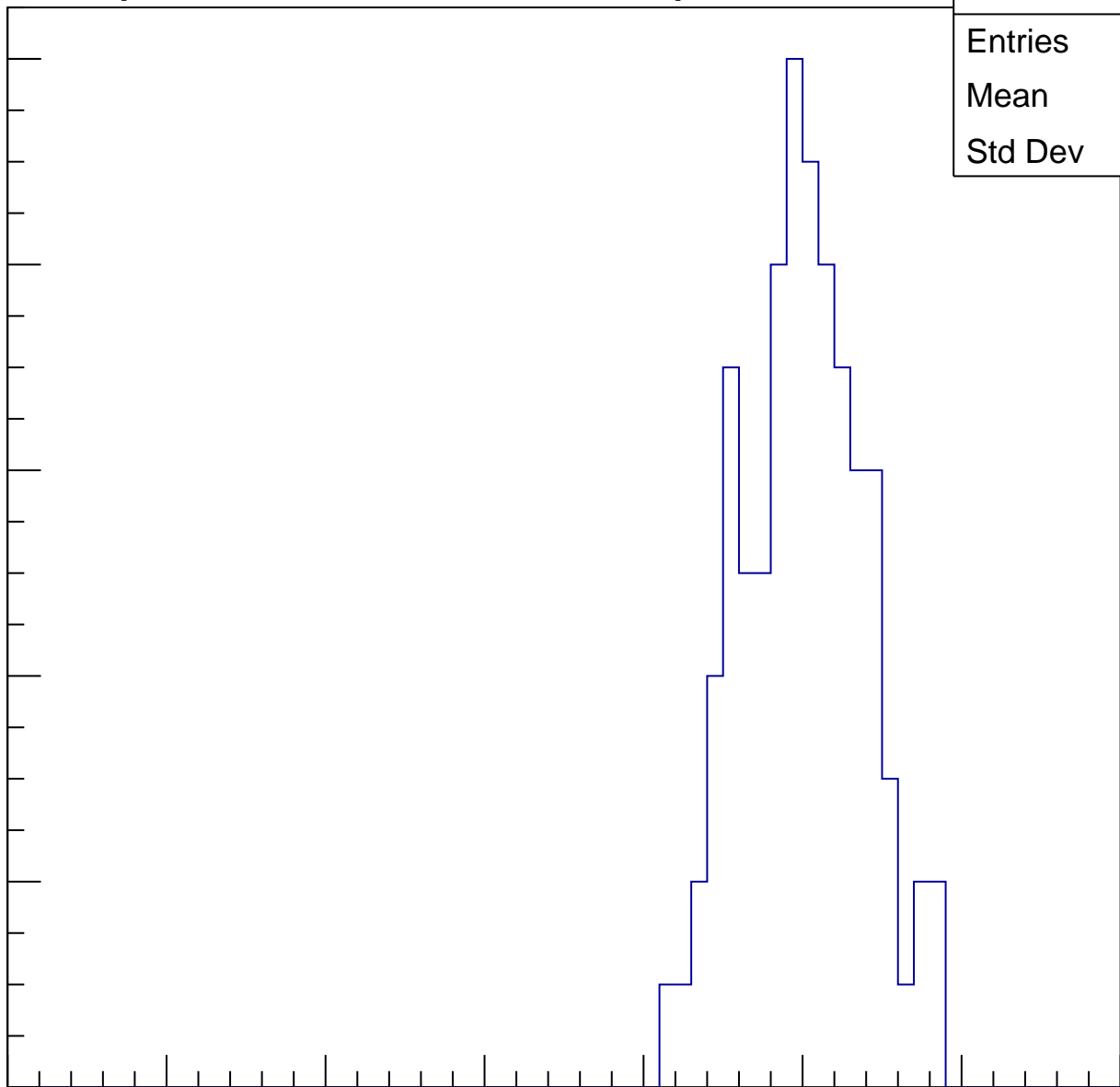
40

50

60

70

ampl

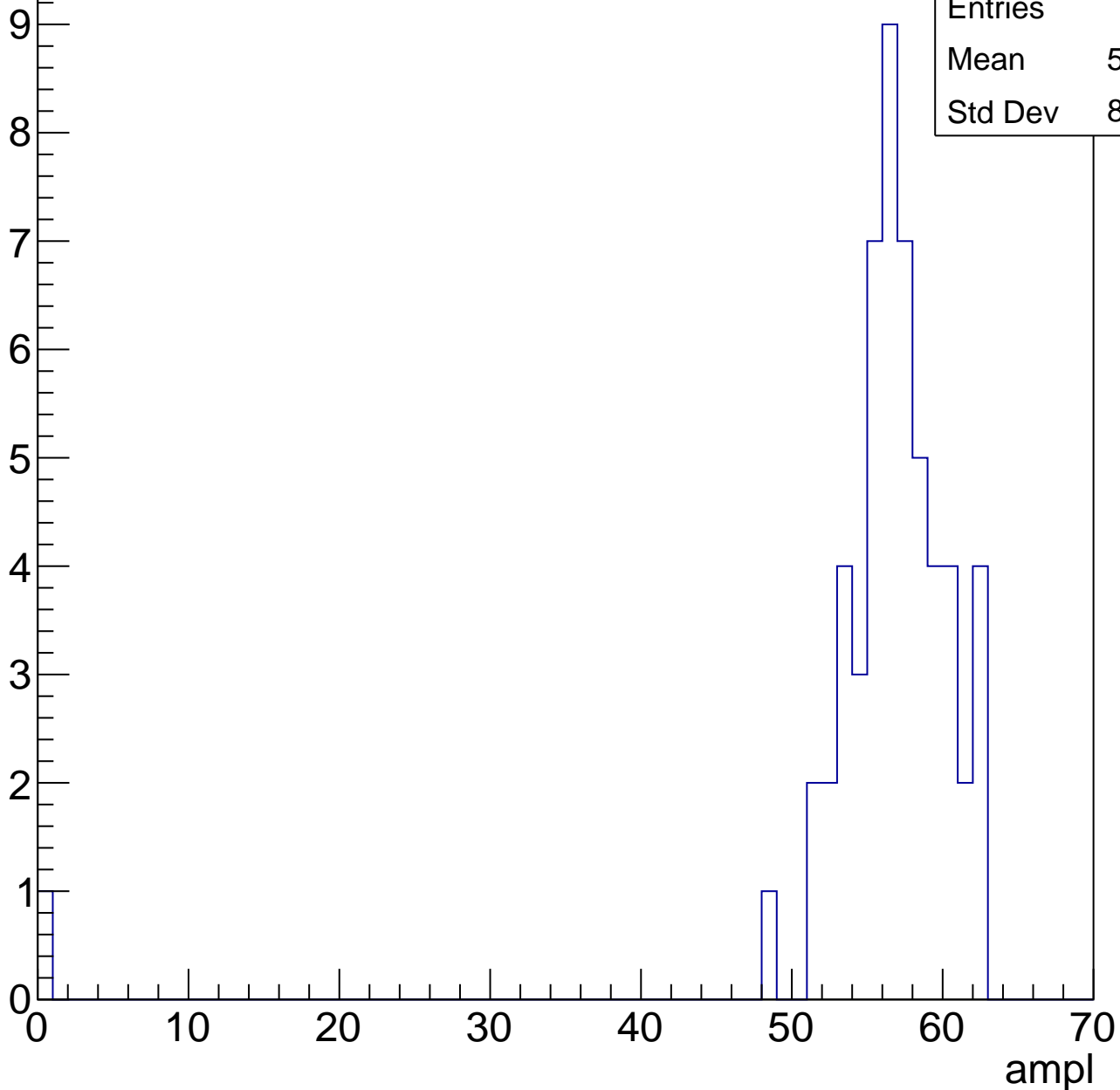


# B0L000S, U7-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	55
Mean	55.49
Std Dev	8.139



# B0L000S, U7-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

7

6

5

4

3

2

1

0

Entries	35
Mean	60.14
Std Dev	2.404

ampl

0

10

20

30

40

50

60

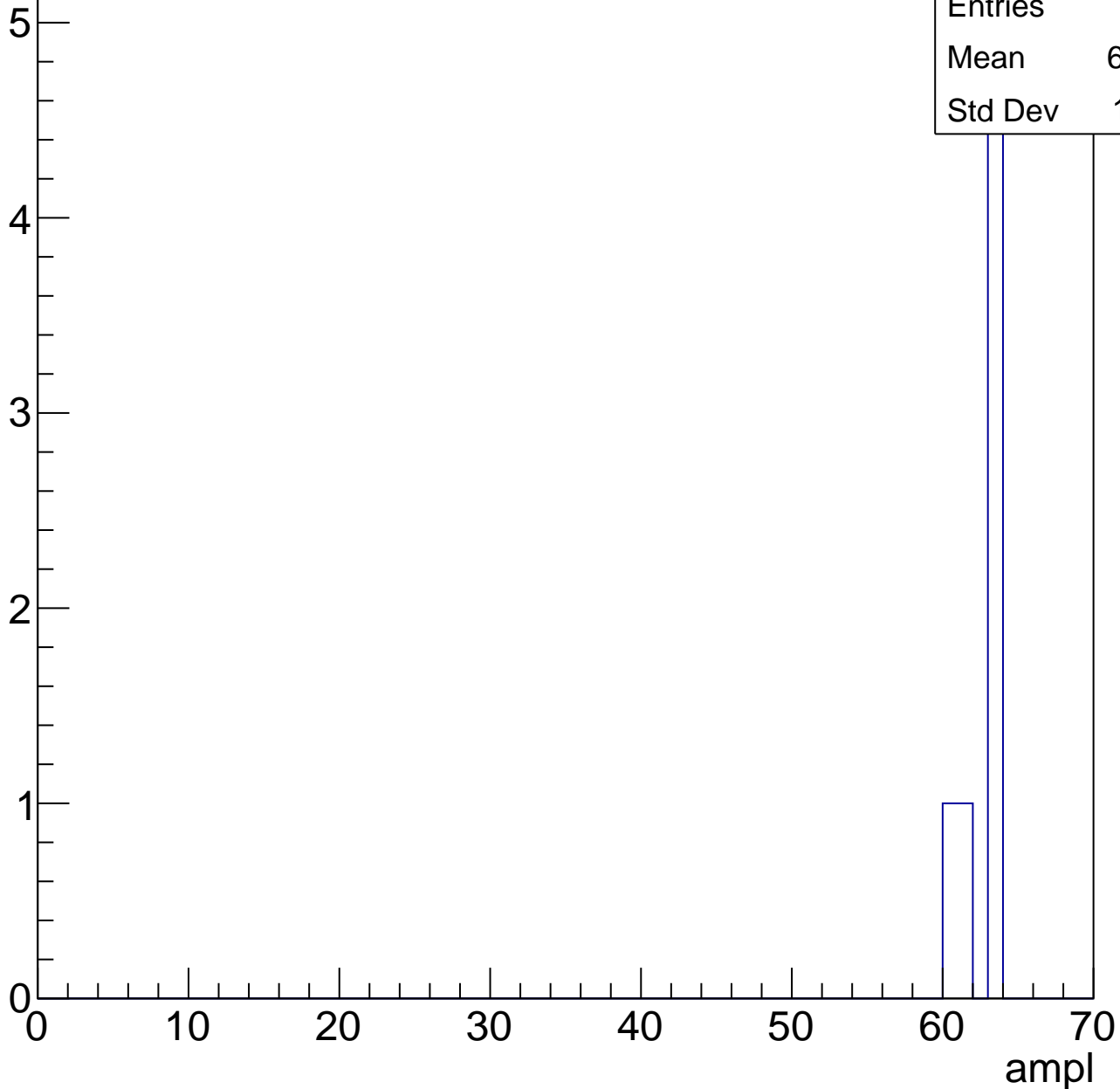
70

# B0L000S, U7-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	7
Mean	62.29
Std Dev	1.161





# B0L000S, U7-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L000S, U7-ch97, adc0

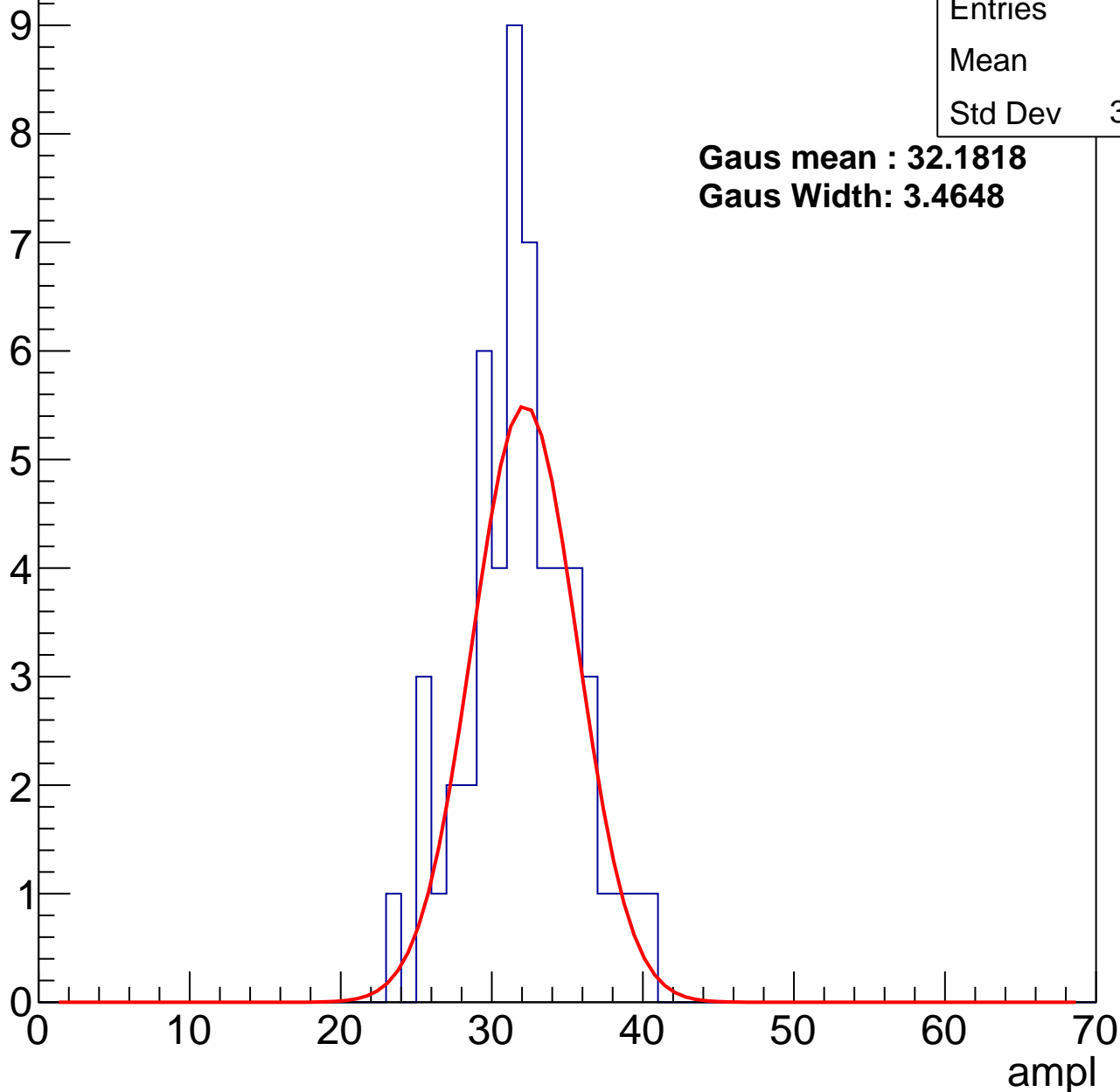
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	54
Mean	31.5
Std Dev	3.573

**Gaus mean : 32.1818**

**Gaus Width: 3.4648**



# B0L000S, U7-ch97, adc1

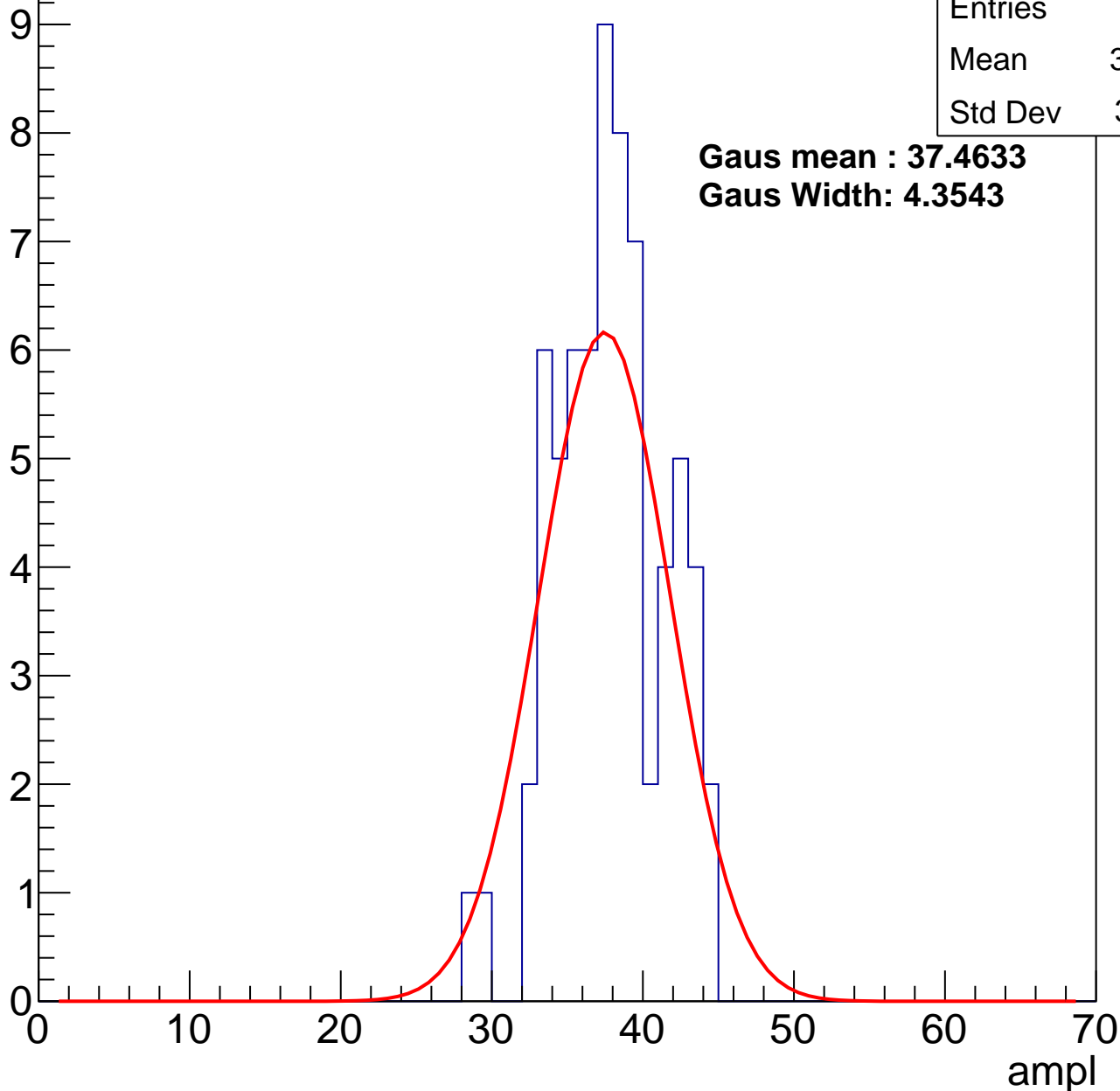
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	68
Mean	37.34
Std Dev	3.521

**Gaus mean : 37.4633**

**Gaus Width: 4.3543**



# B0L000S, U7-ch97, adc2

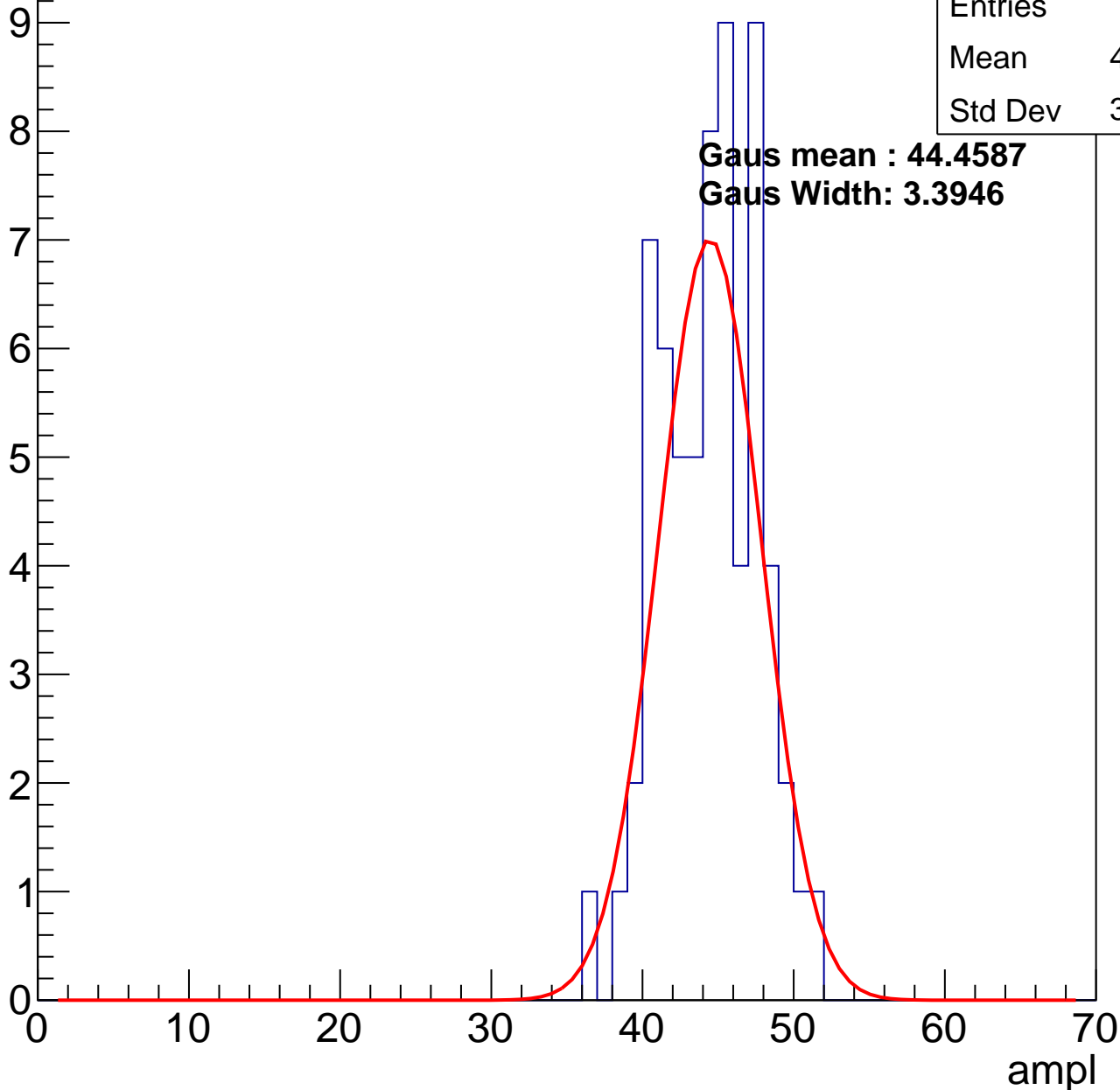
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	65
Mean	43.97
Std Dev	3.152

**Gaus mean : 44.4587**

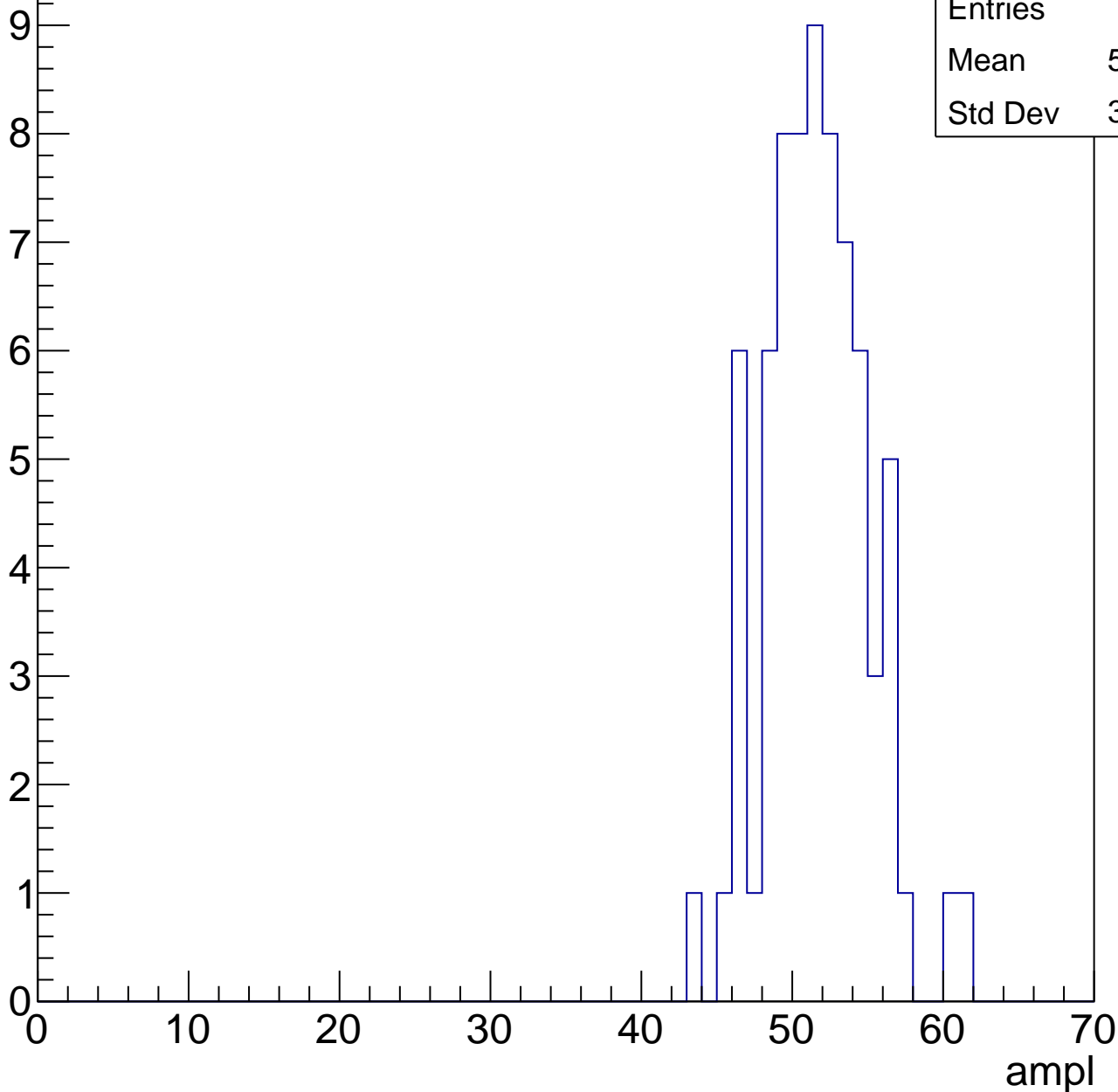
**Gaus Width: 3.3946**



# B0L000S, U7-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

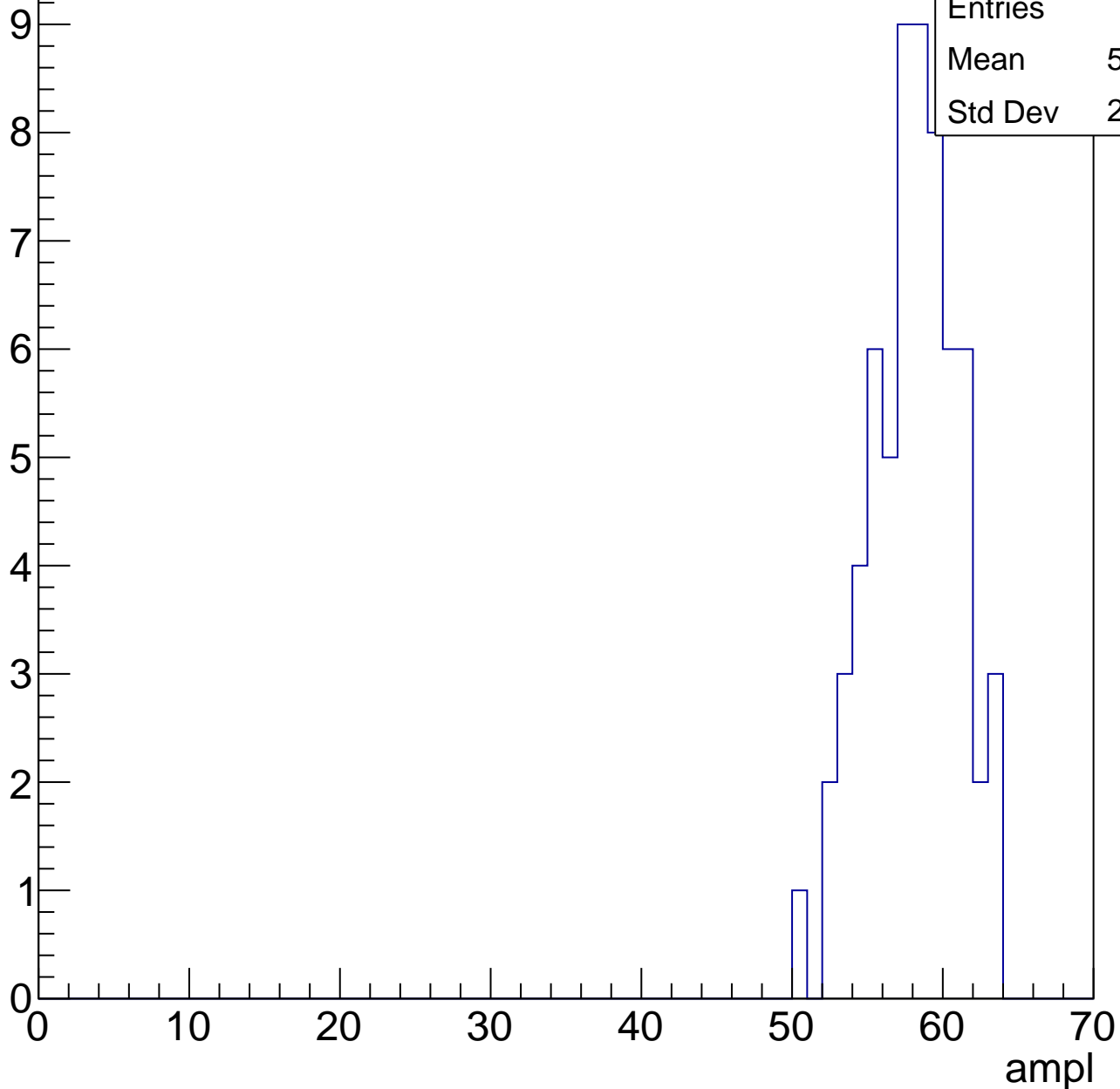
Entry



# B0L000S, U7-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



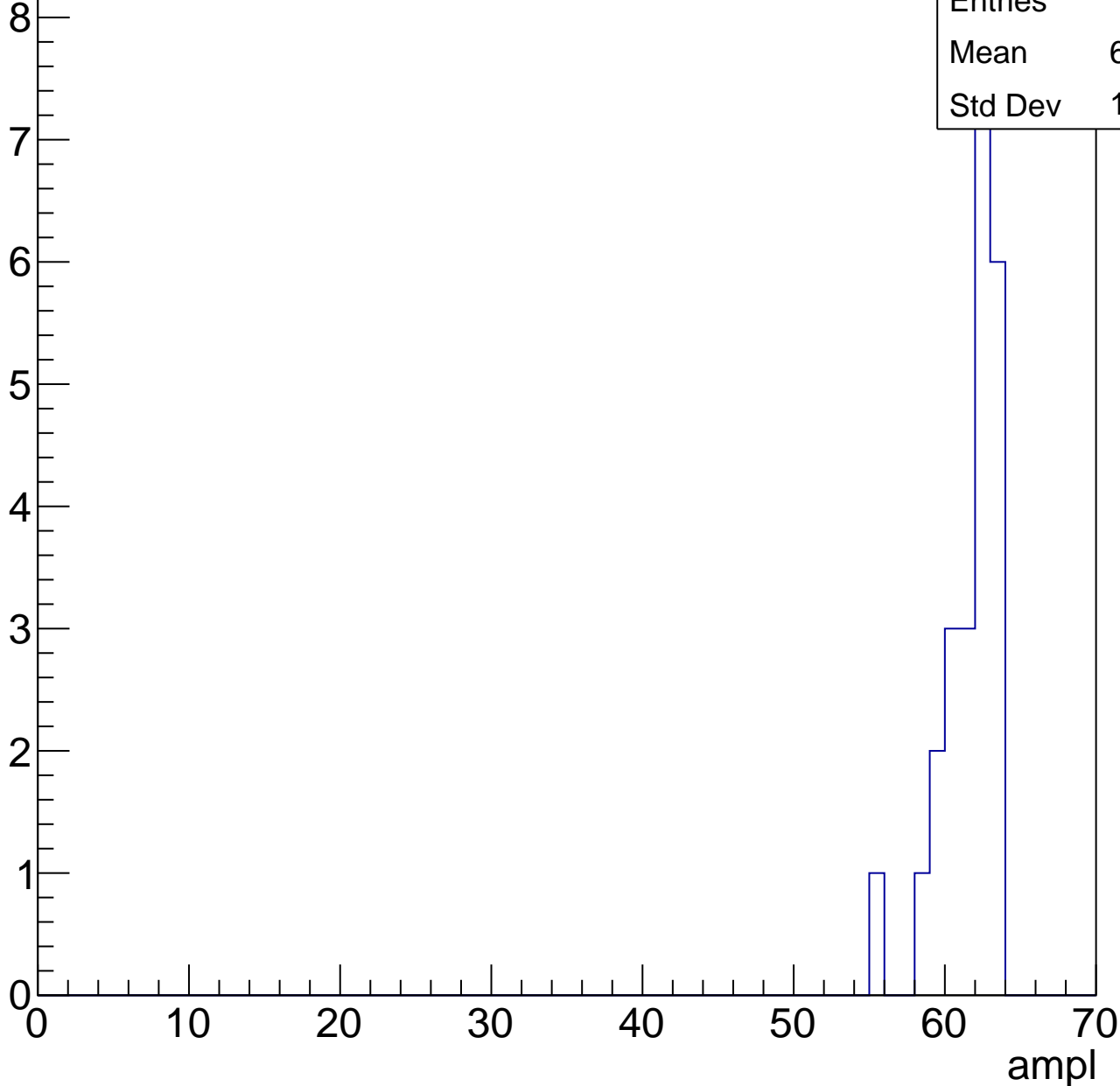
Entries	64
Mean	57.58
Std Dev	2.904

# B0L000S, U7-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

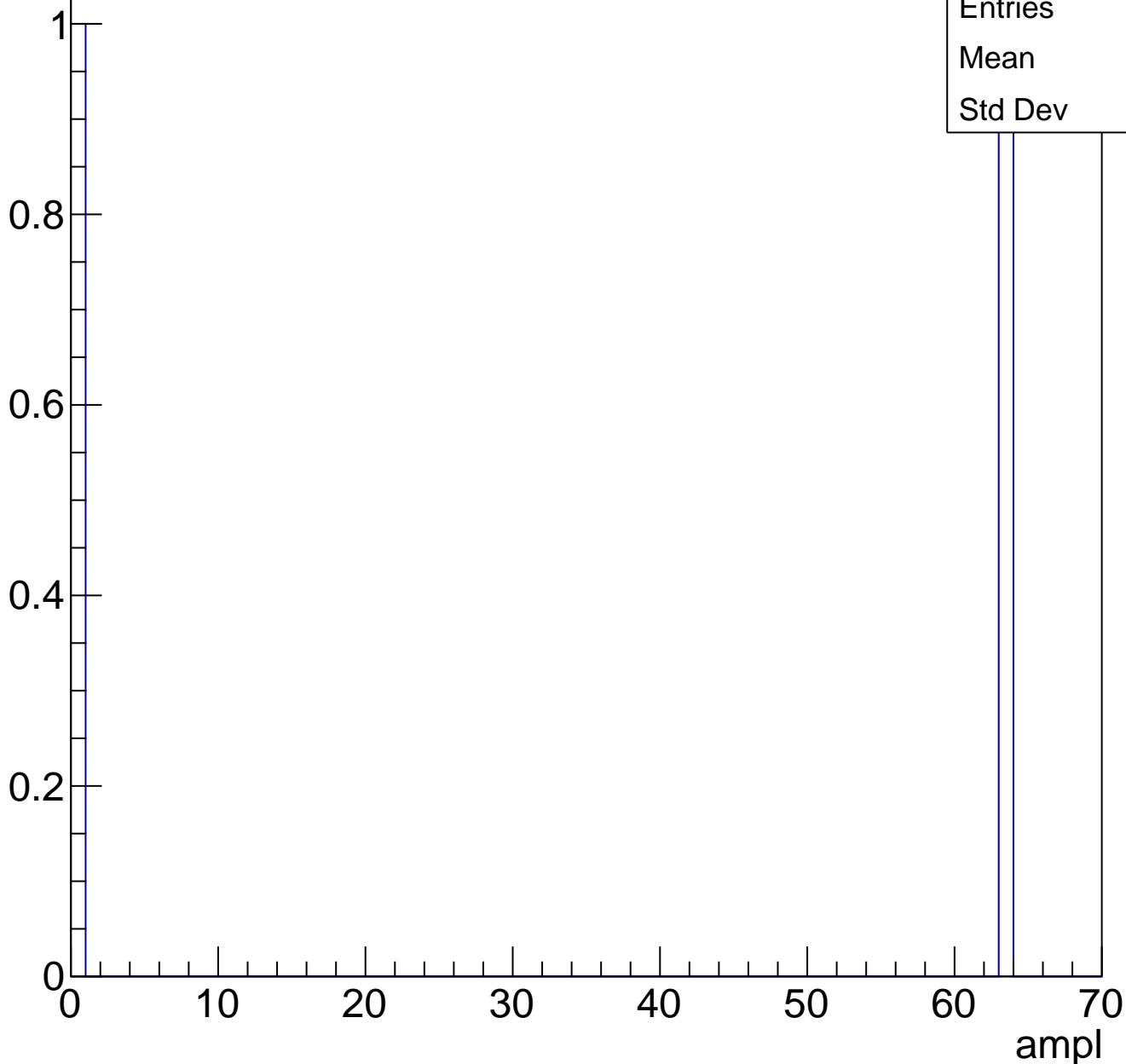
Entries	24
Mean	61.17
Std Dev	1.908



# B0L000S, U7-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch98, adc0

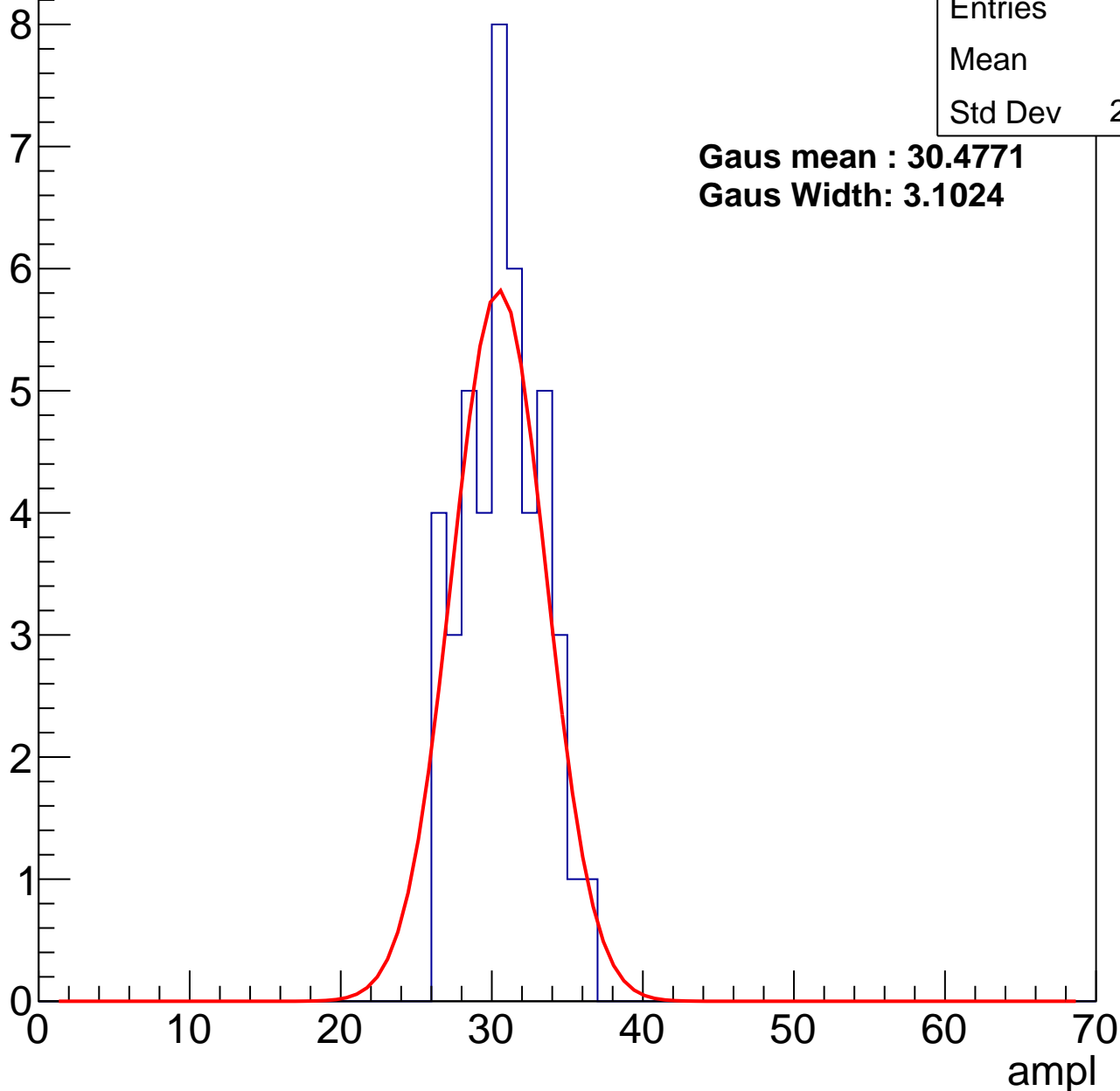
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	44
Mean	30.3
Std Dev	2.555

**Gaus mean : 30.4771**

**Gaus Width: 3.1024**



# B0L000S, U7-ch98, adc1

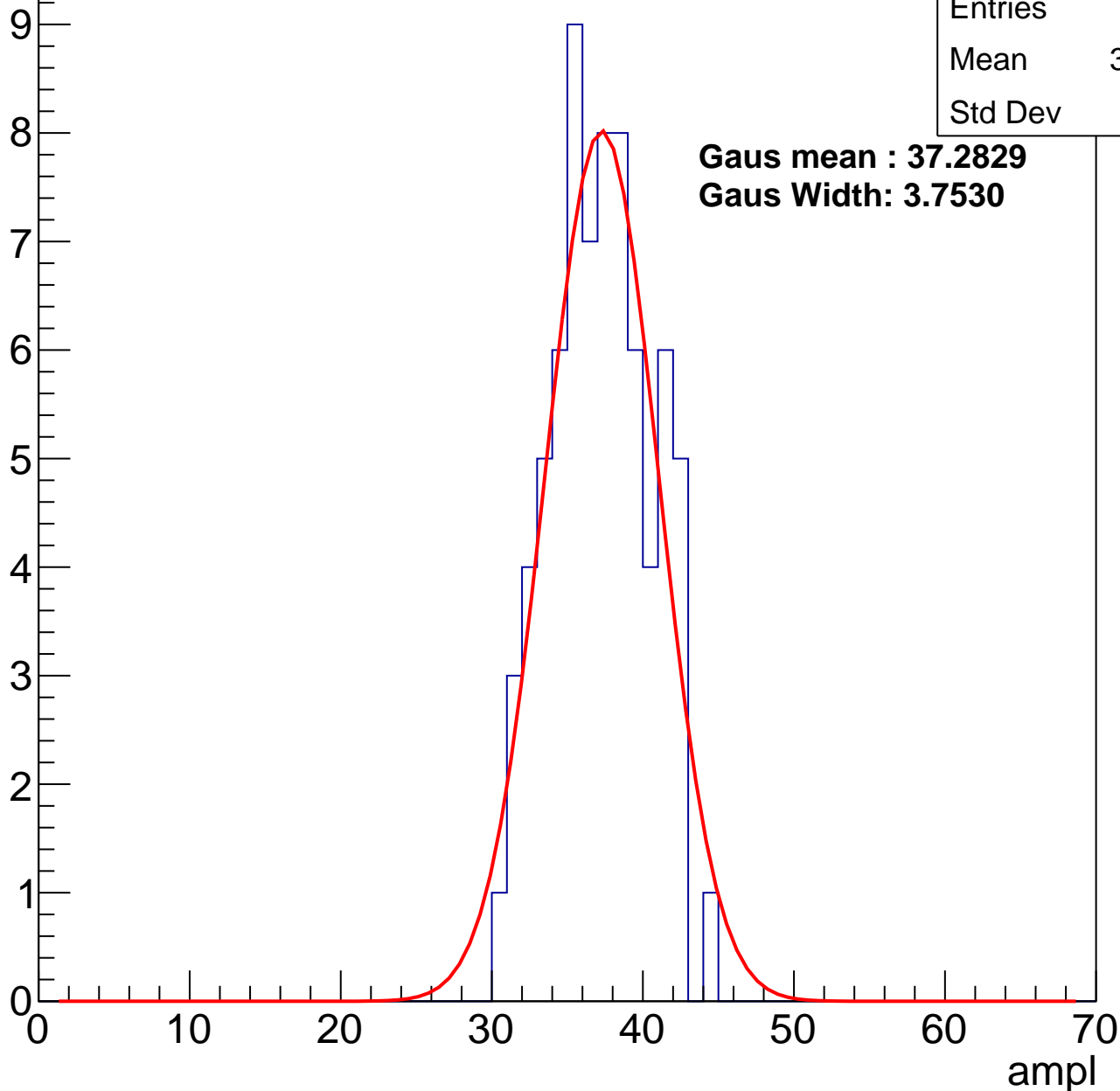
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	73
Mean	36.73
Std Dev	3.24

**Gaus mean : 37.2829**

**Gaus Width: 3.7530**



# B0L000S, U7-ch98, adc2

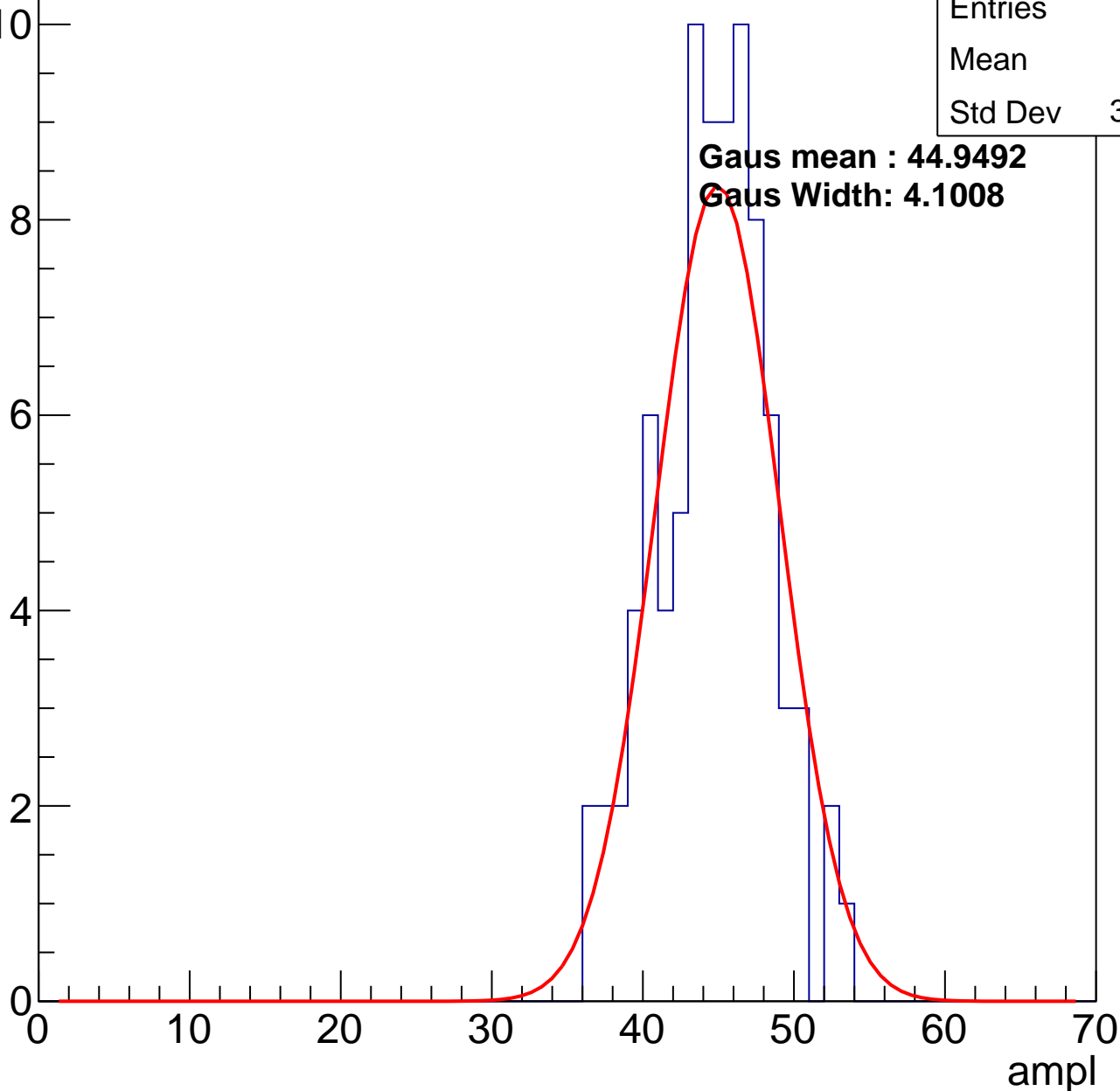
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	86
Mean	44.2
Std Dev	3.682

**Gaus mean : 44.9492**

**Gaus Width: 4.1008**

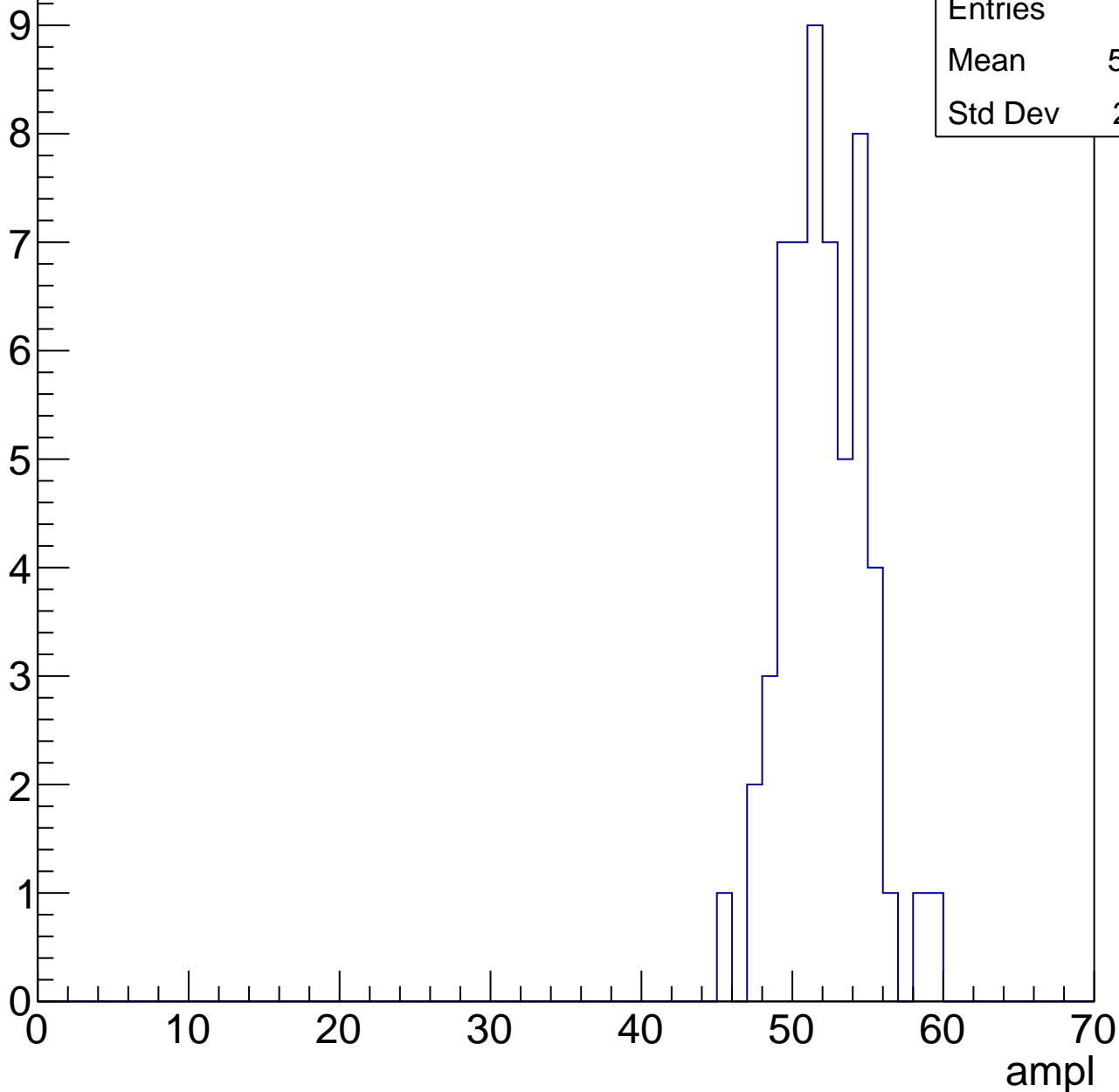


# B0L000S, U7-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	56
Mean	51.59
Std Dev	2.711

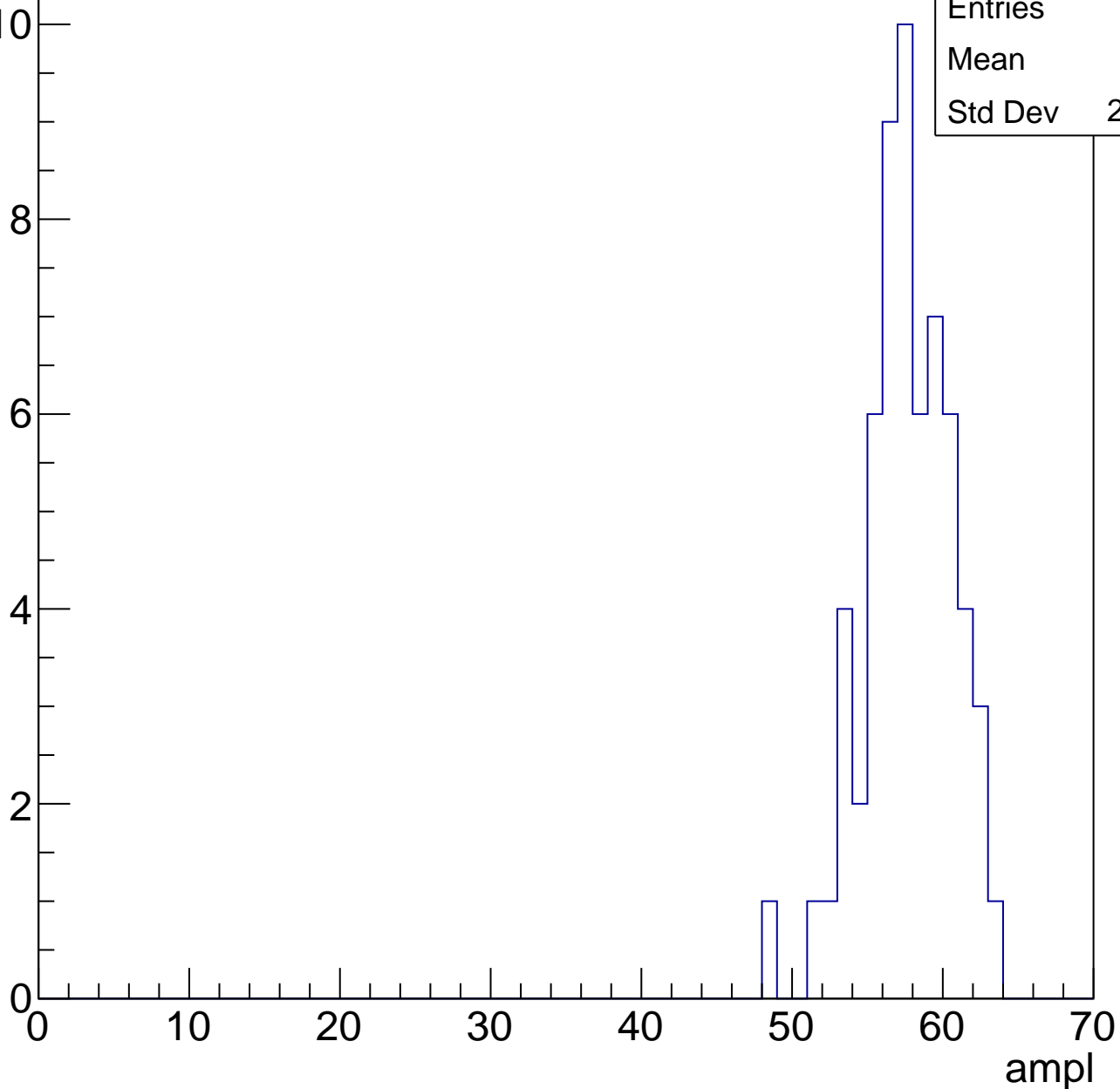


# B0L000S, U7-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	61
Mean	57.2
Std Dev	2.913

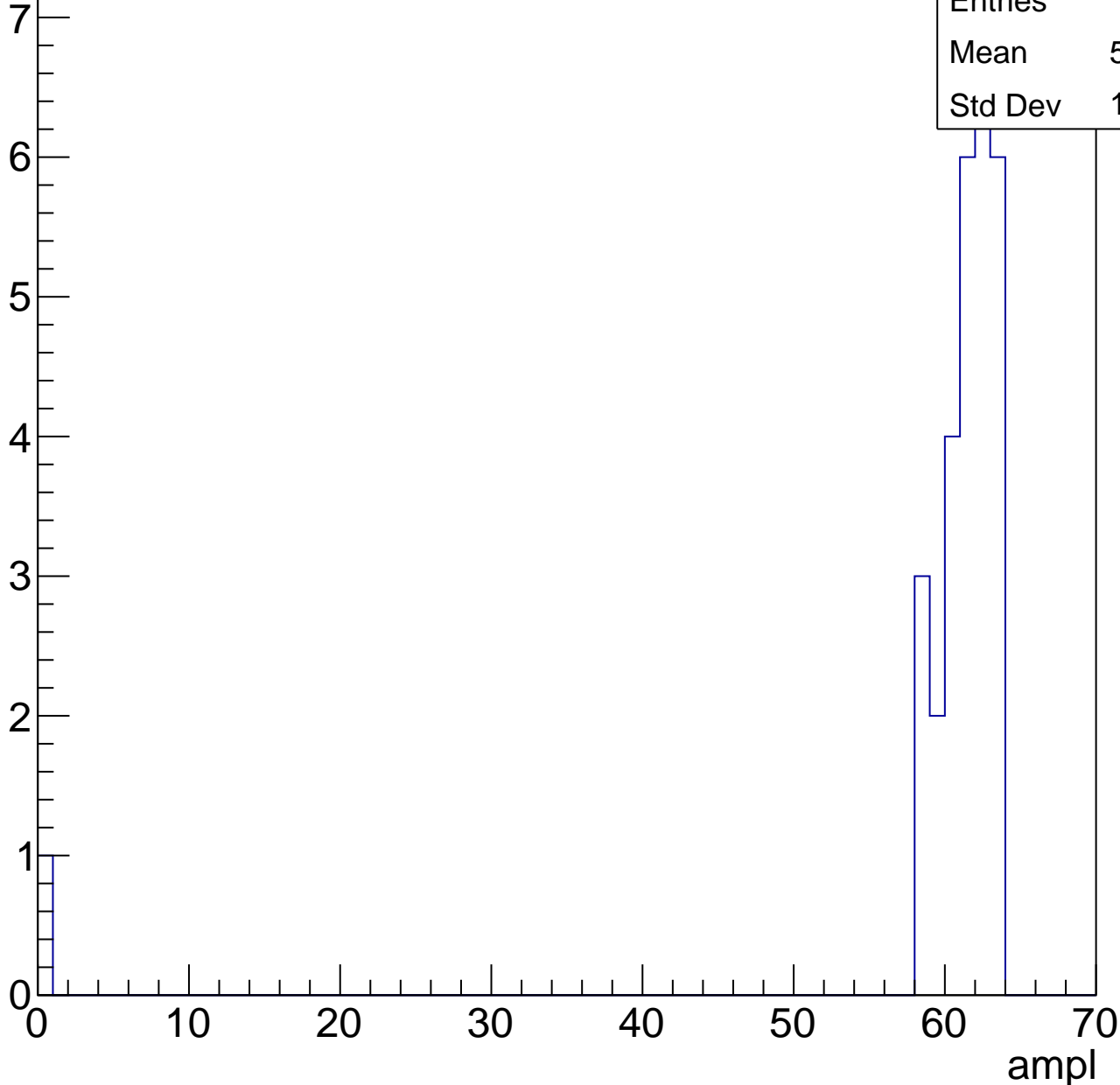


# B0L000S, U7-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

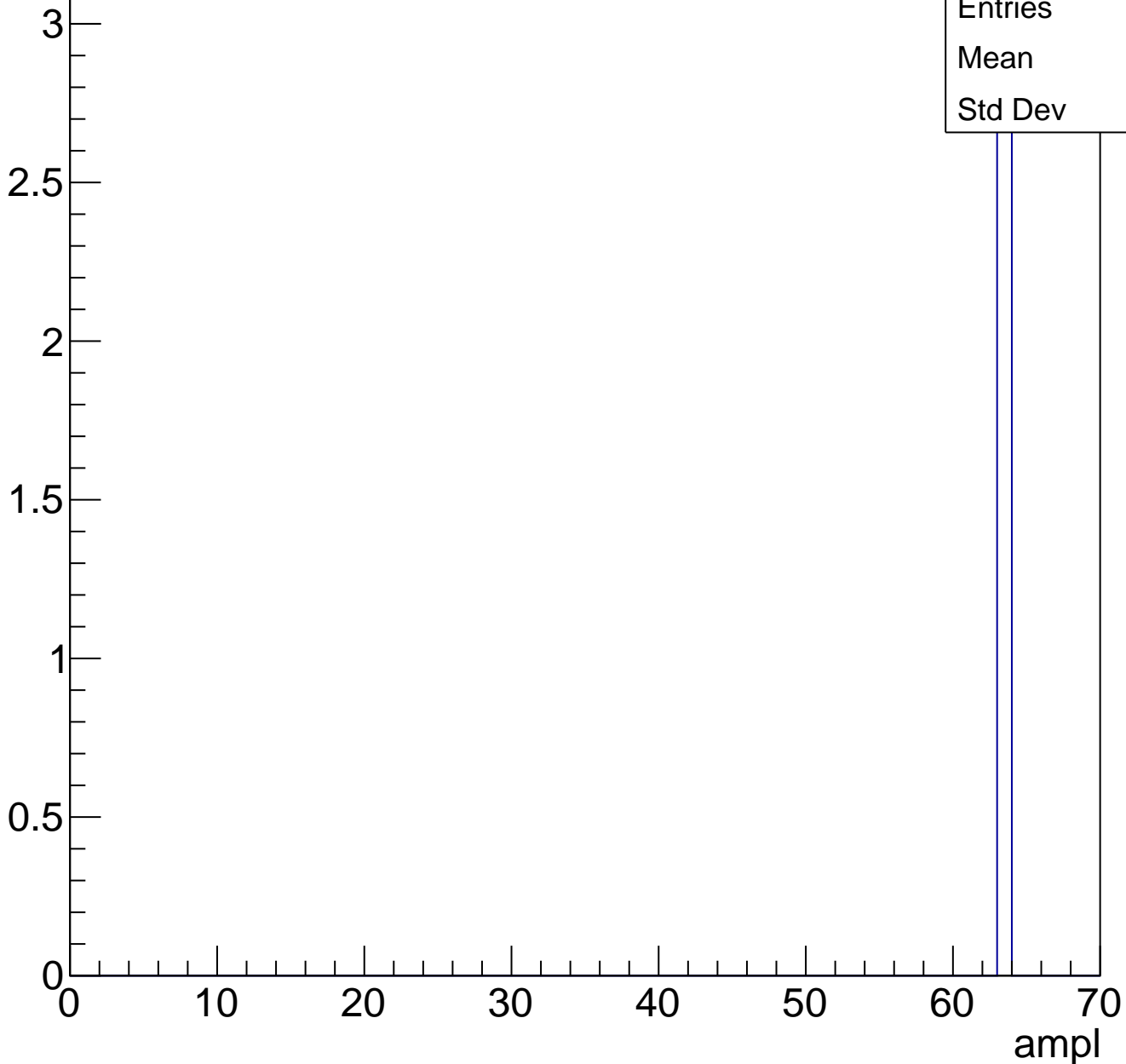
Entries	29
Mean	58.97
Std Dev	11.25



# B0L000S, U7-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch99, adc0

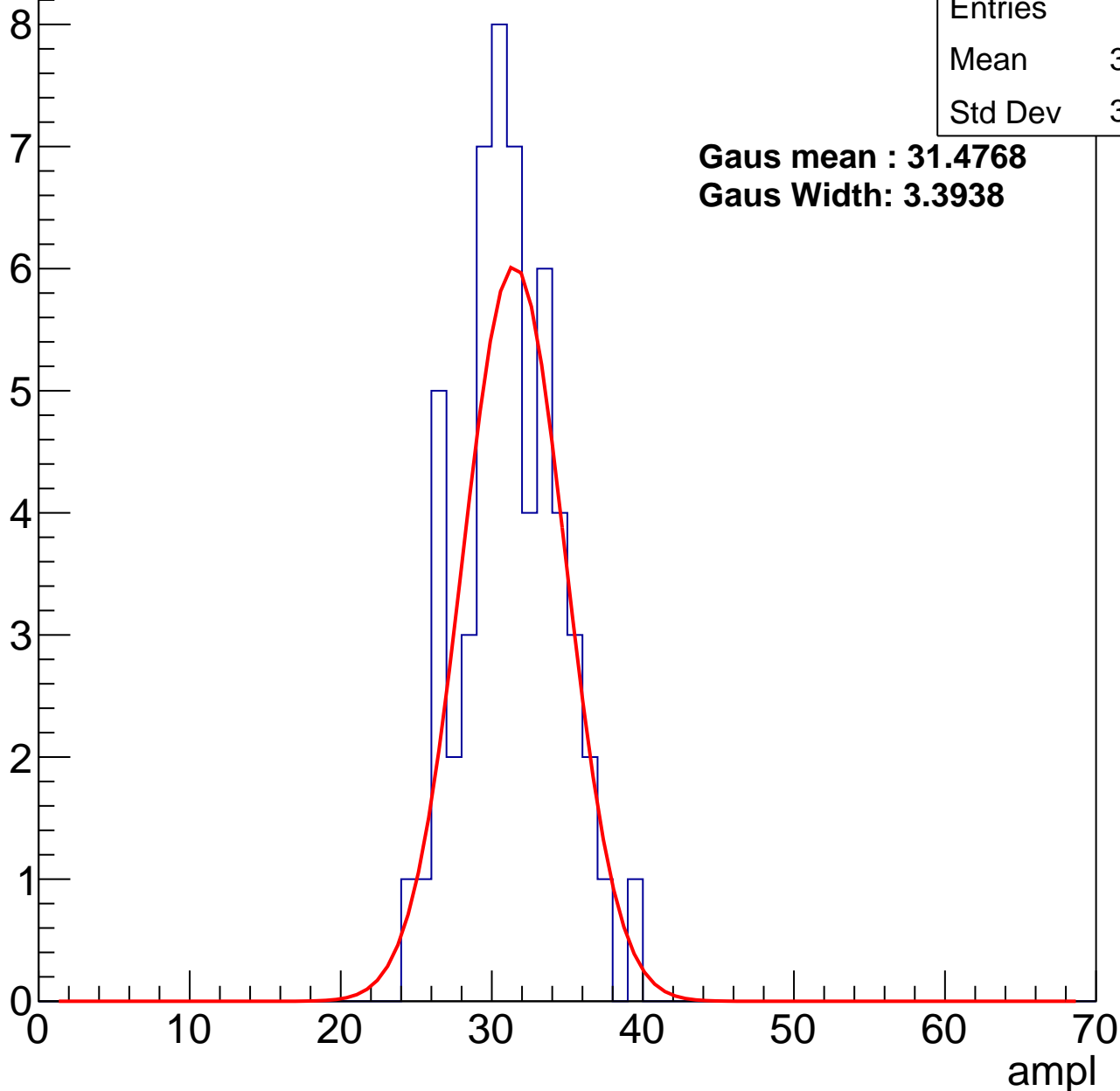
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	55
Mean	30.76
Std Dev	3.202

**Gaus mean : 31.4768**

**Gaus Width: 3.3938**



# B0L000S, U7-ch99, adc1

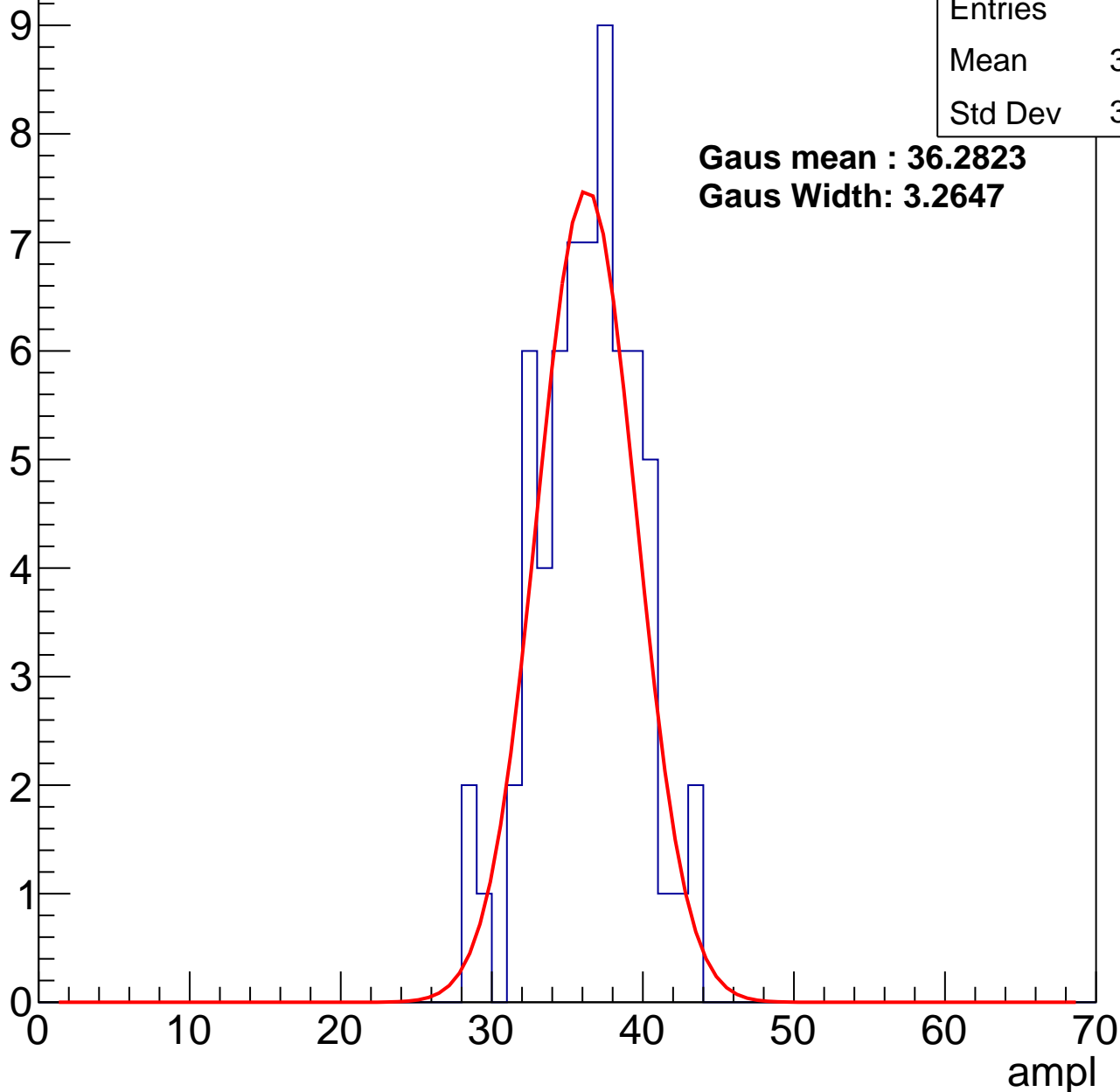
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	65
Mean	35.94
Std Dev	3.318

**Gaus mean : 36.2823**

**Gaus Width: 3.2647**



# B0L000S, U7-ch99, adc2

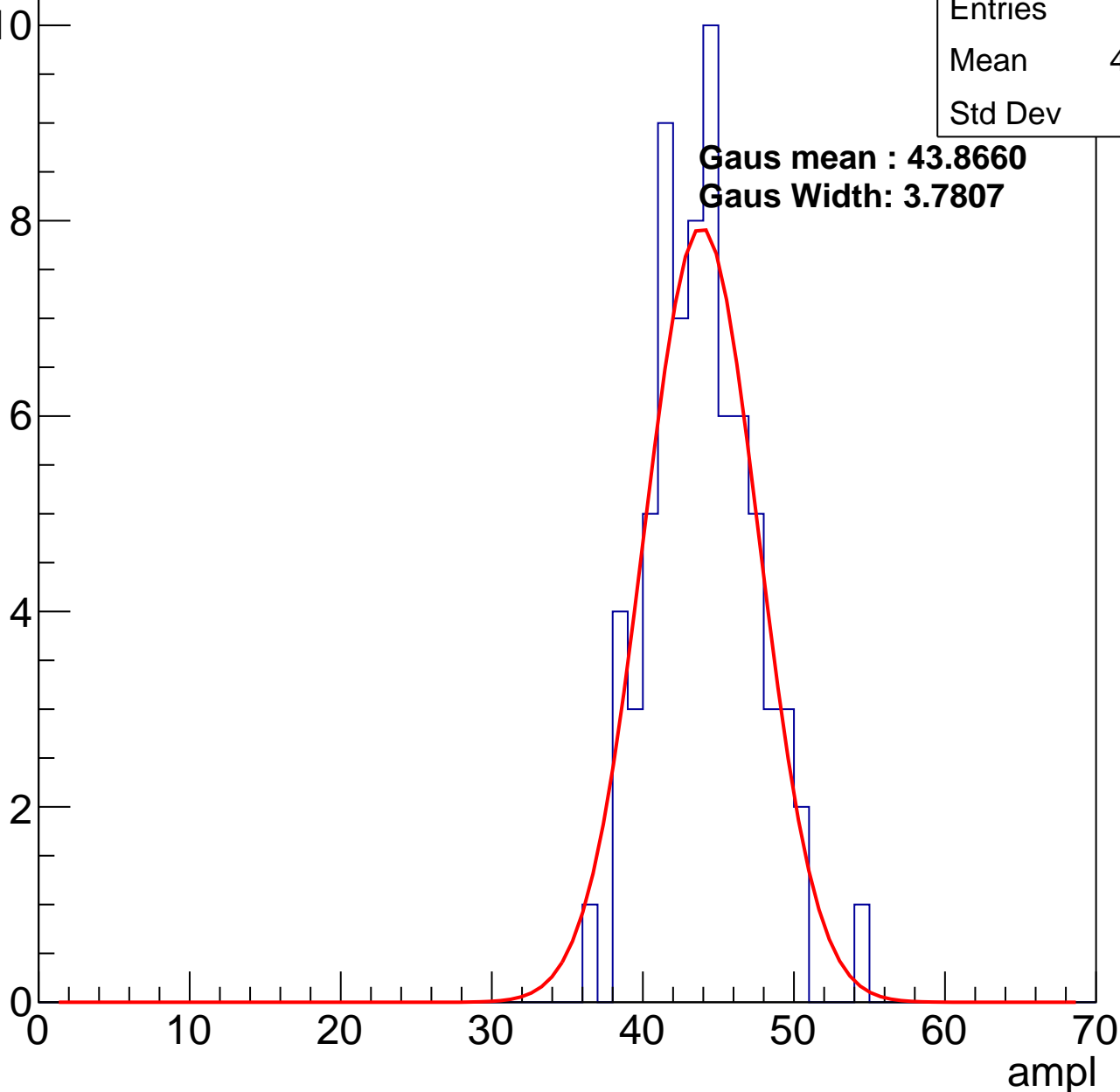
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	73
Mean	43.53
Std Dev	3.38

**Gaus mean : 43.8660**

**Gaus Width: 3.7807**

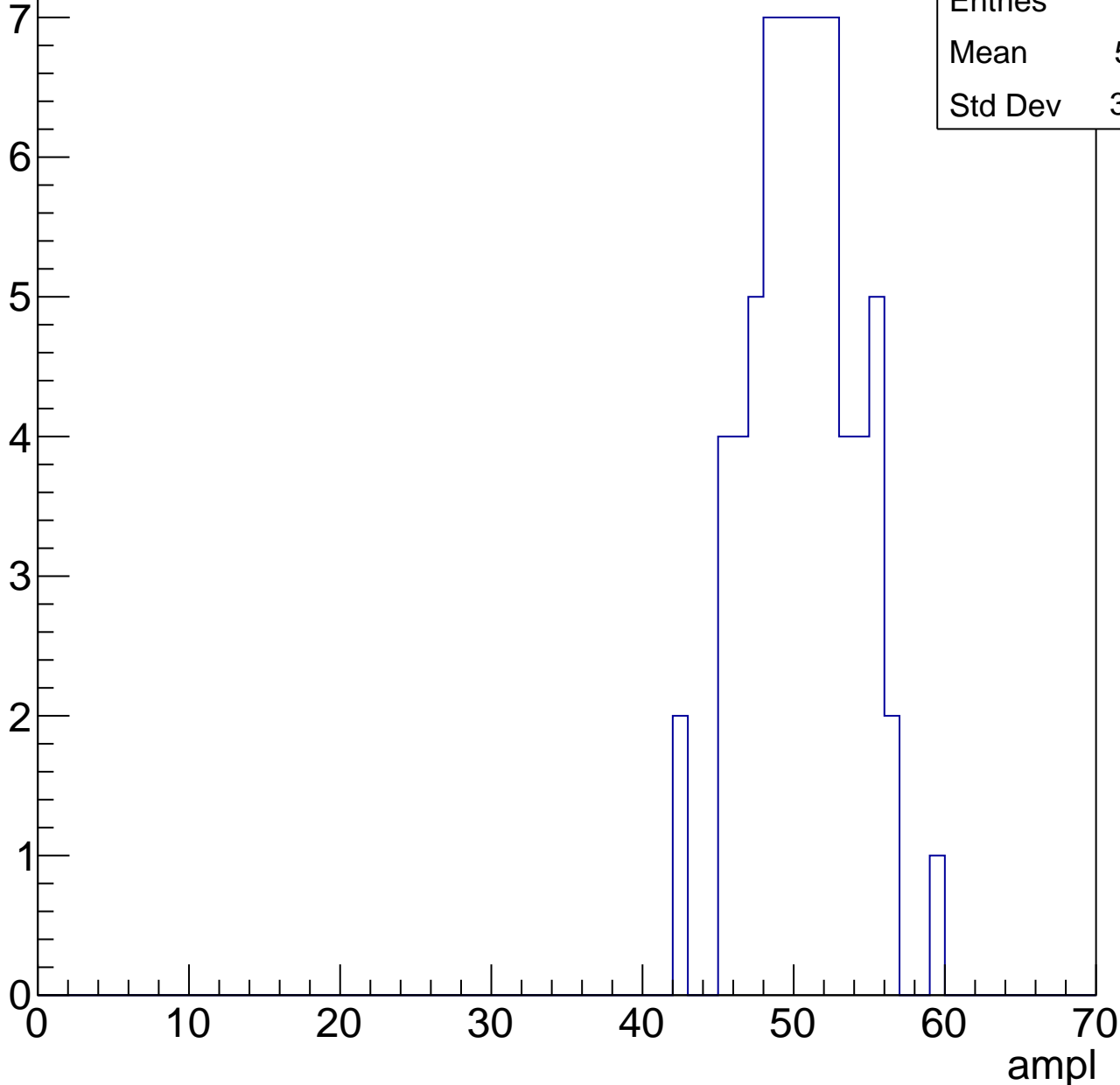


# B0L000S, U7-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	66
Mean	50.11
Std Dev	3.447

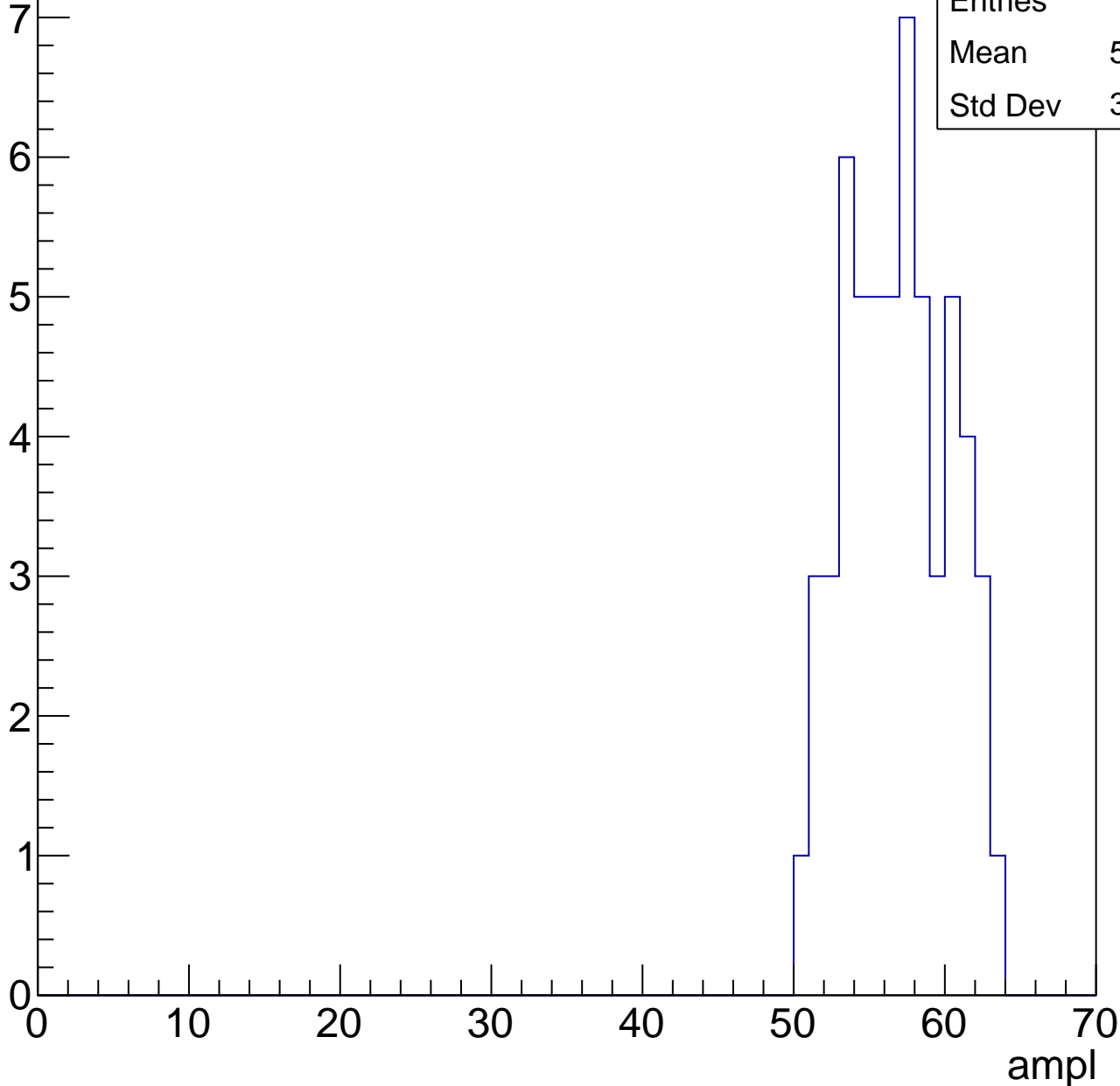


# B0L000S, U7-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	56
Mean	56.45
Std Dev	3.322

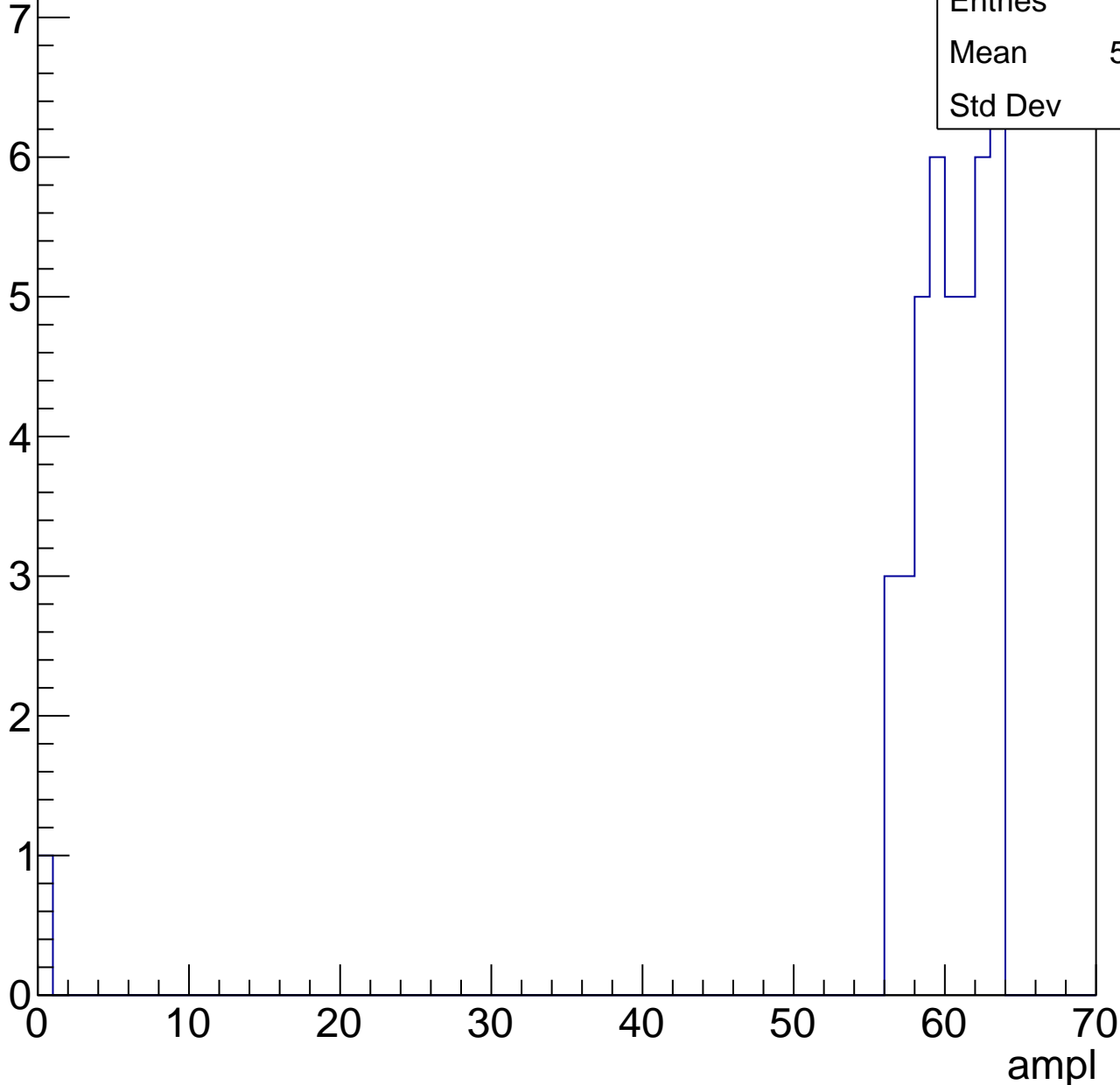


# B0L000S, U7-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	41
Mean	58.56
Std Dev	9.51



# B0L000S, U7-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	4
Mean	62.25
Std Dev	0.8292



# B0L000S, U7-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch100, adc0

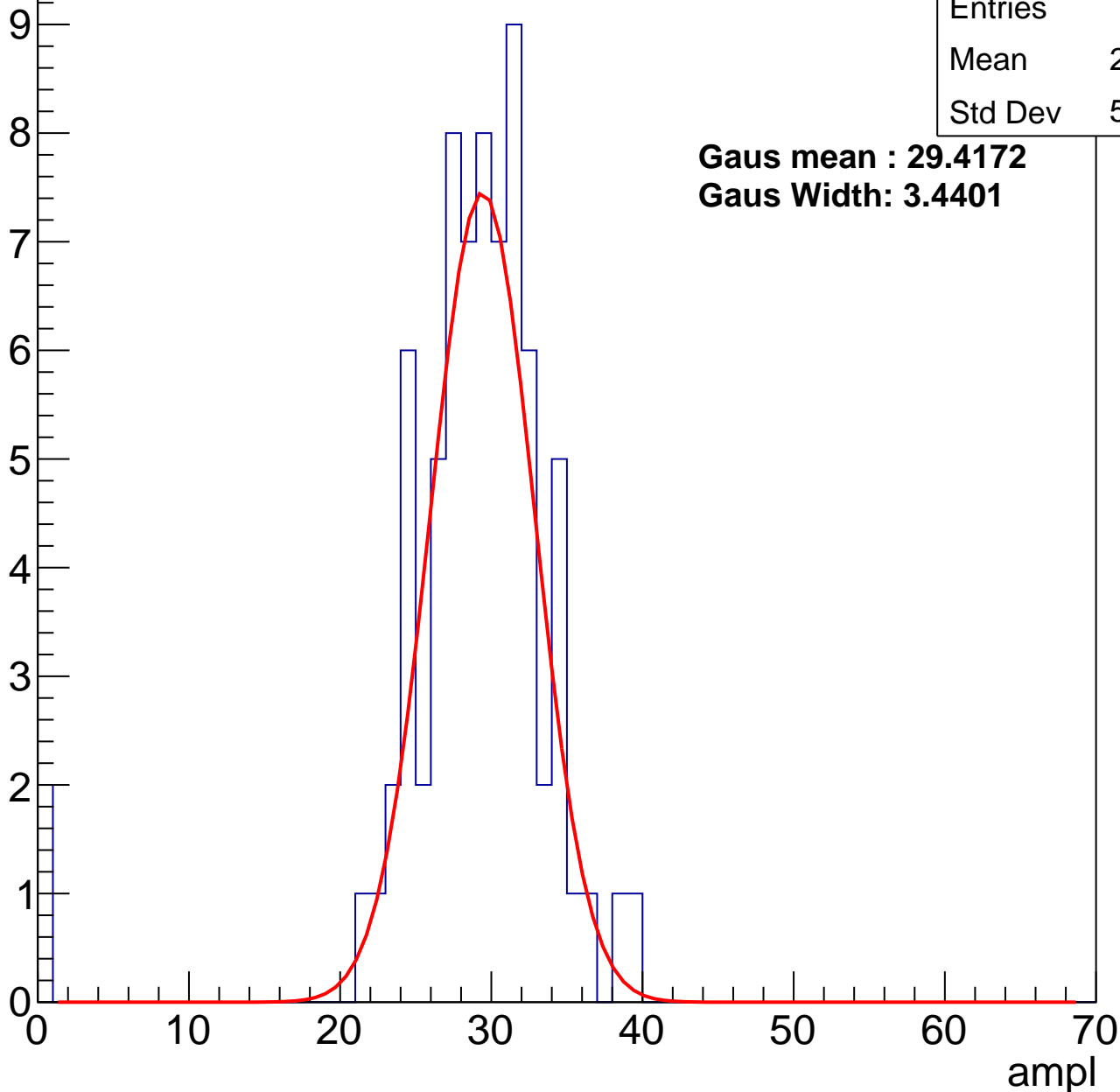
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	75
Mean	28.29
Std Dev	5.905

**Gaus mean : 29.4172**

**Gaus Width: 3.4401**



# B0L000S, U7-ch100, adc1

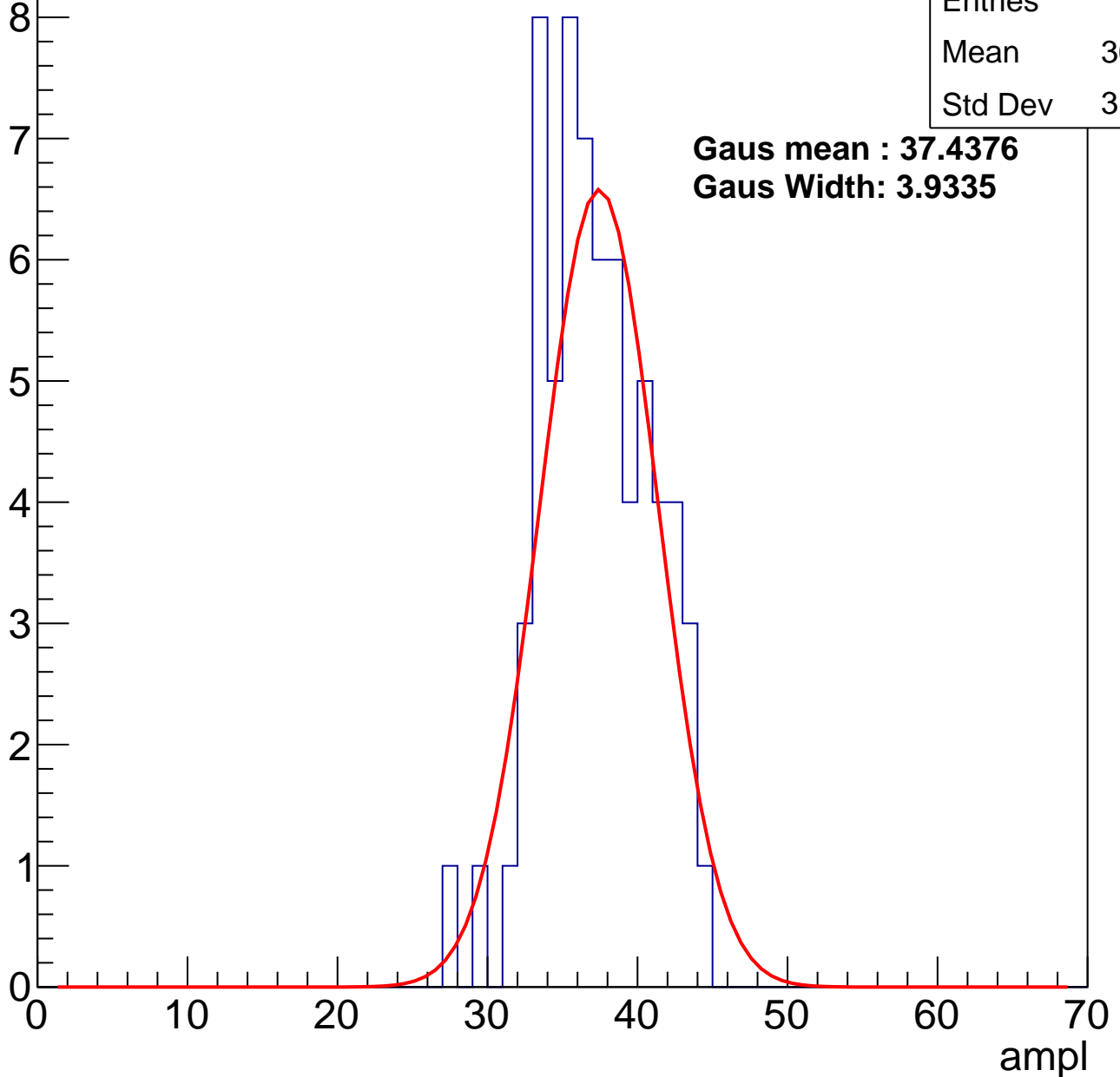
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	67
Mean	36.72
Std Dev	3.603

**Gaus mean : 37.4376**

**Gaus Width: 3.9335**



# B0L000S, U7-ch100, adc2

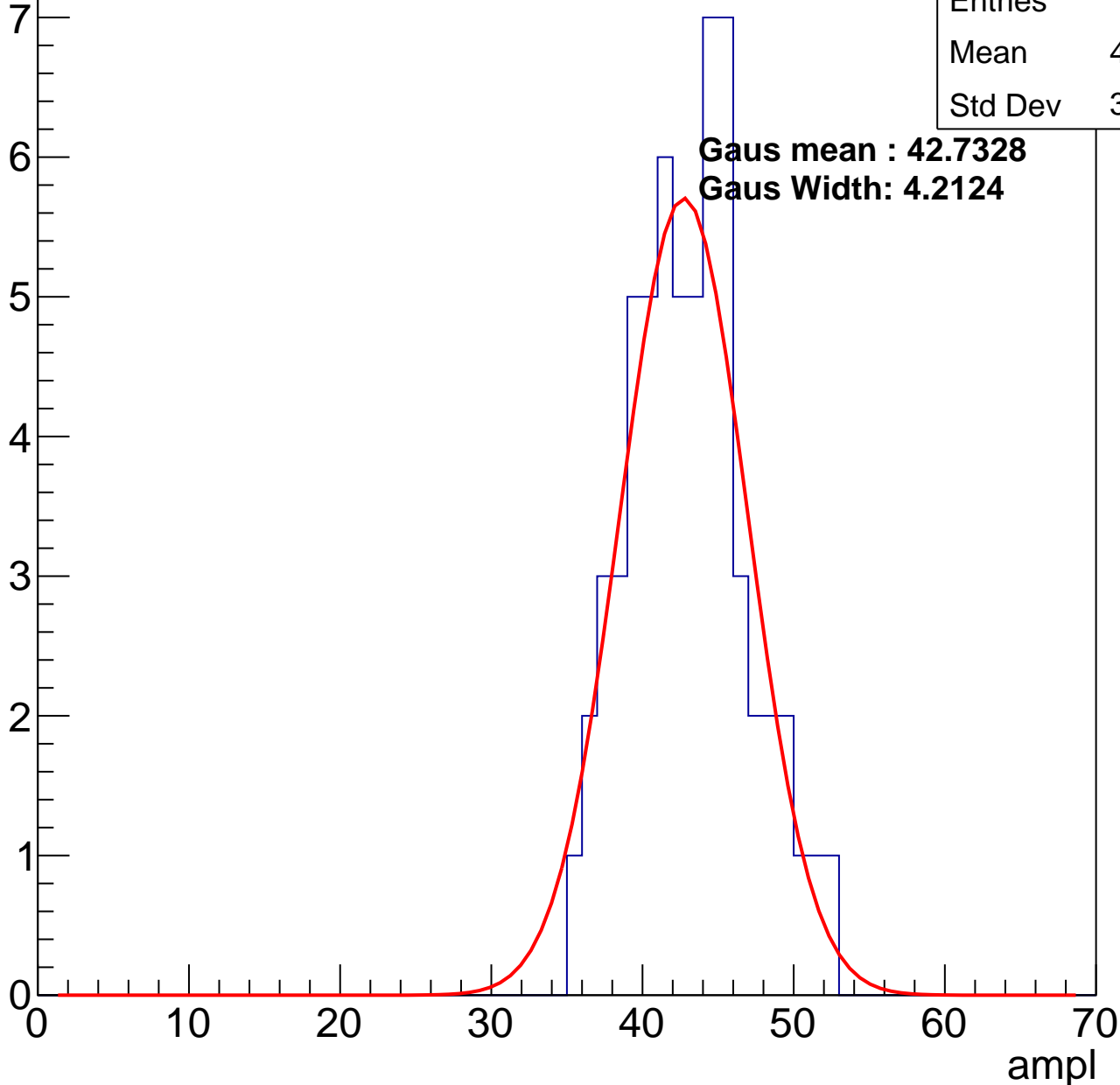
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	61
Mean	42.62
Std Dev	3.842

**Gaus mean : 42.7328**

**Gaus Width: 4.2124**

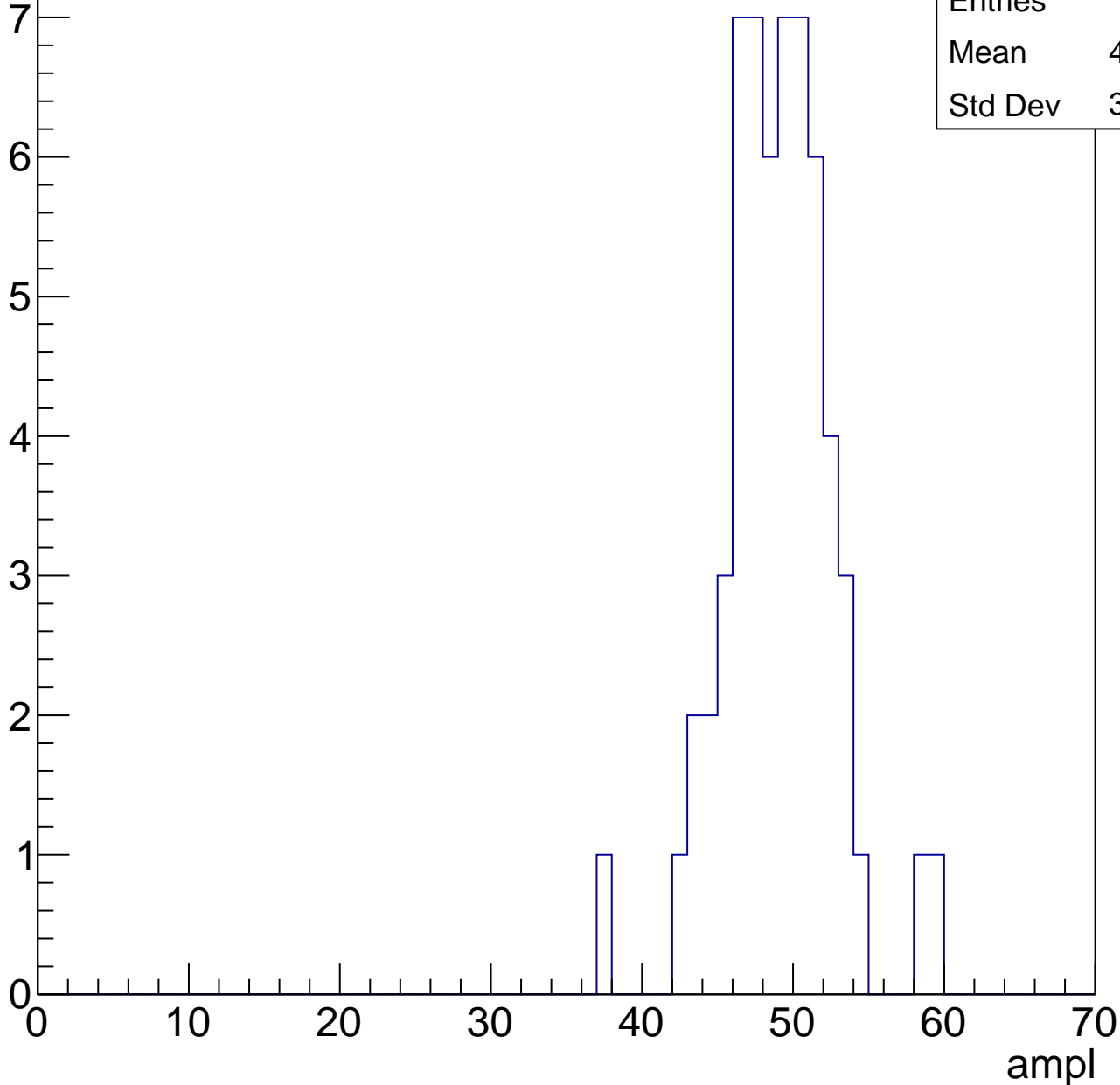


# B0L000S, U7-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	59
Mean	48.54
Std Dev	3.609

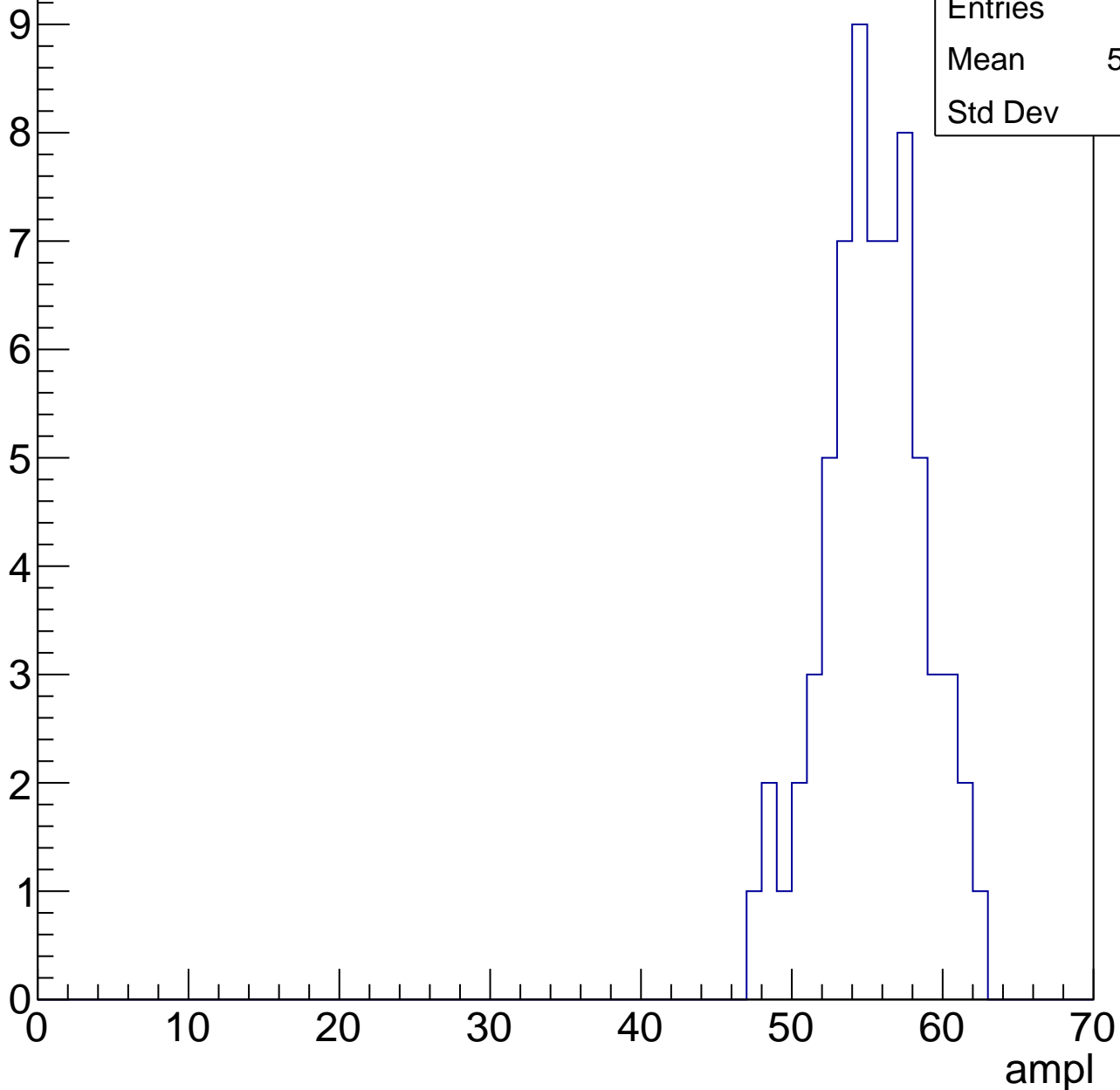


# B0L000S, U7-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	66
Mean	54.94
Std Dev	3.27

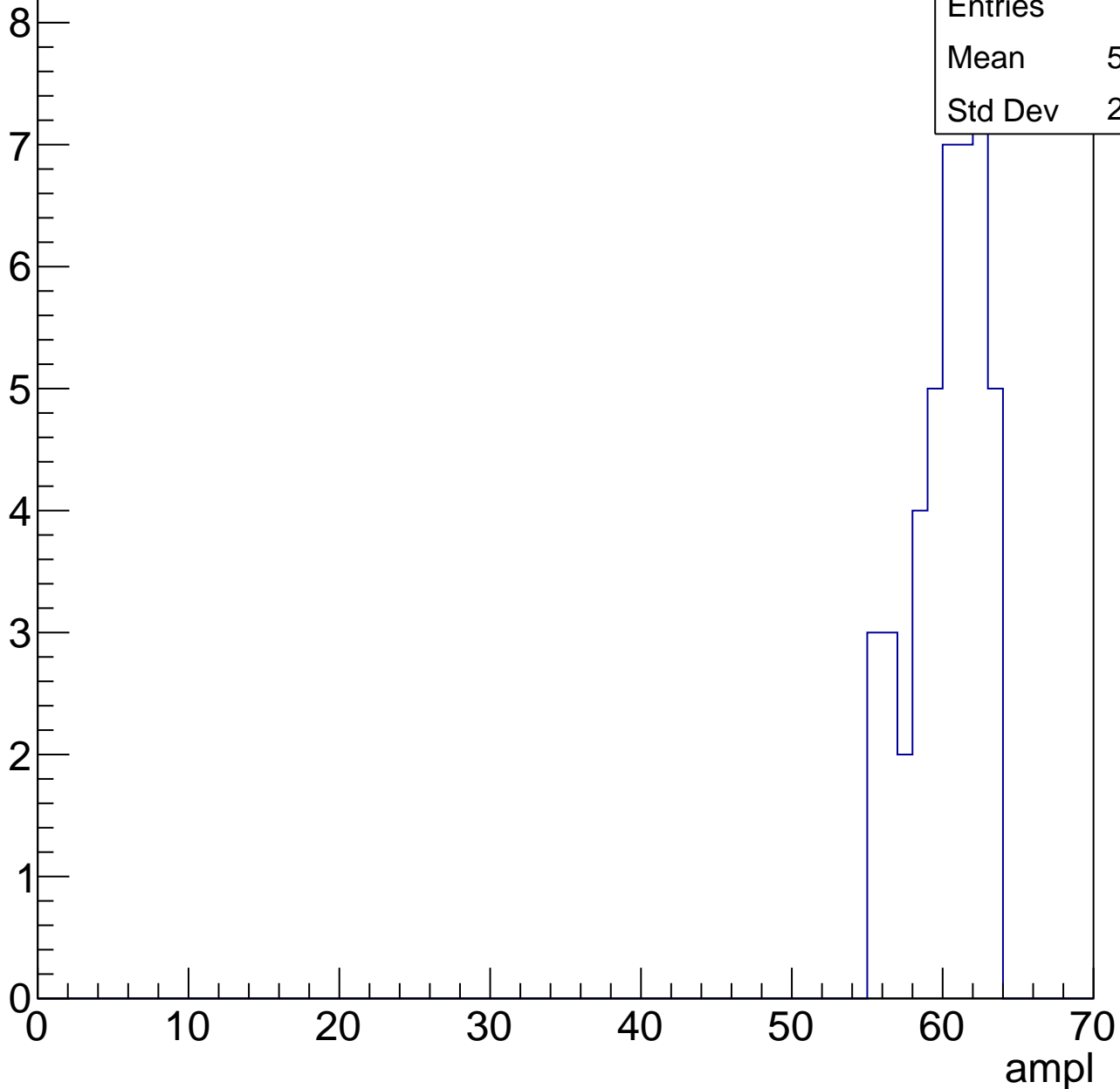


# B0L000S, U7-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	44
Mean	59.82
Std Dev	2.358

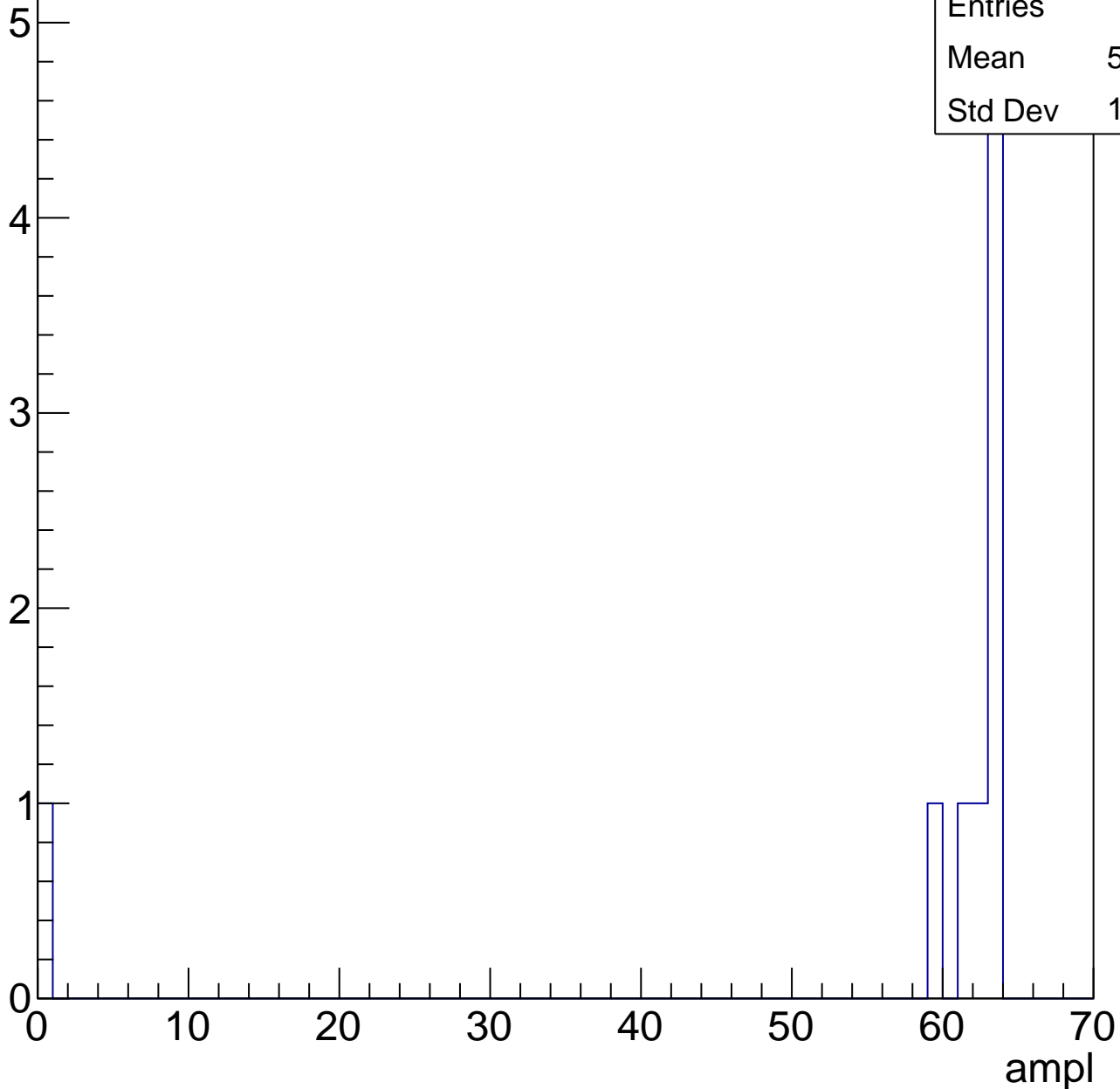


# B0L000S, U7-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	9
Mean	55.22
Std Dev	19.57





# B0L000S, U7-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L000S, U7-ch101, adc0

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	81
Mean	29.57
Std Dev	6.802

**Gaus mean : 31.2840**

**Gaus Width: 3.8037**

Entry

10  
8  
6  
4  
2  
0

ampl

0

10

20

30

40

50

60

70

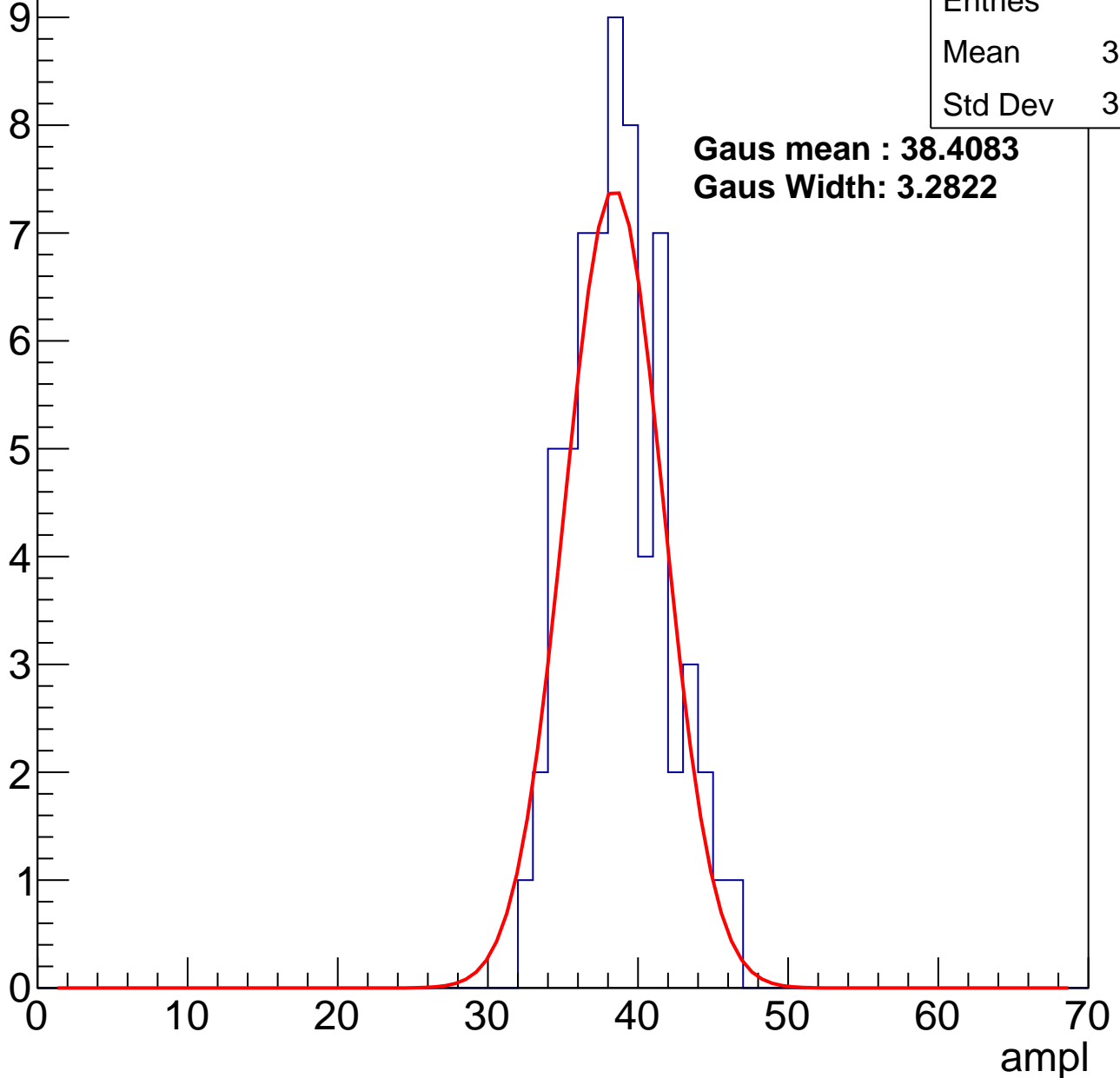
# B0L000S, U7-ch101, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	64
Mean	38.23
Std Dev	3.116

**Gaus mean : 38.4083**  
**Gaus Width: 3.2822**



# B0L000S, U7-ch101, adc2

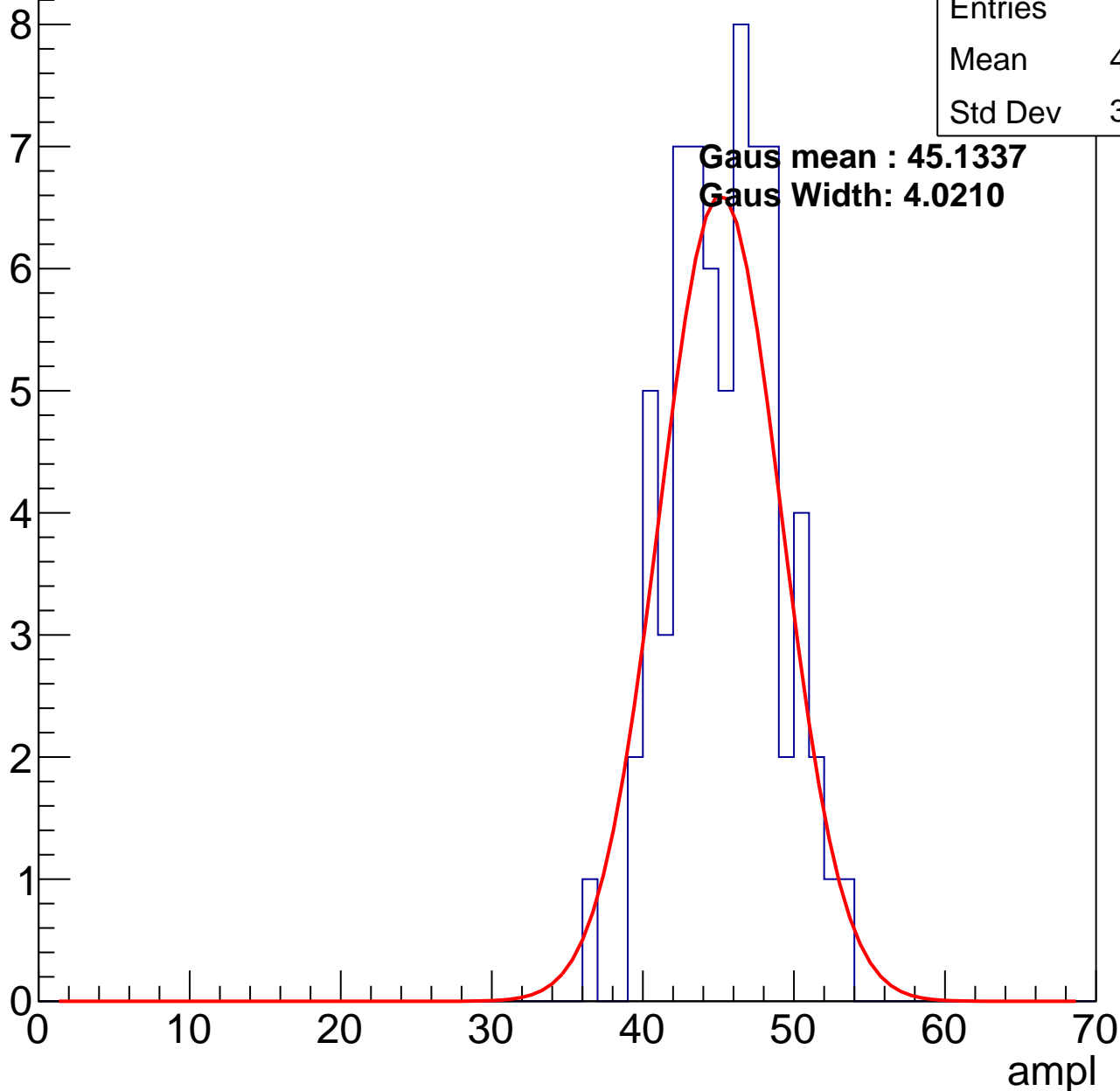
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	68
Mean	44.99
Std Dev	3.513

**Gaus mean : 45.1337**

**Gaus Width: 4.0210**

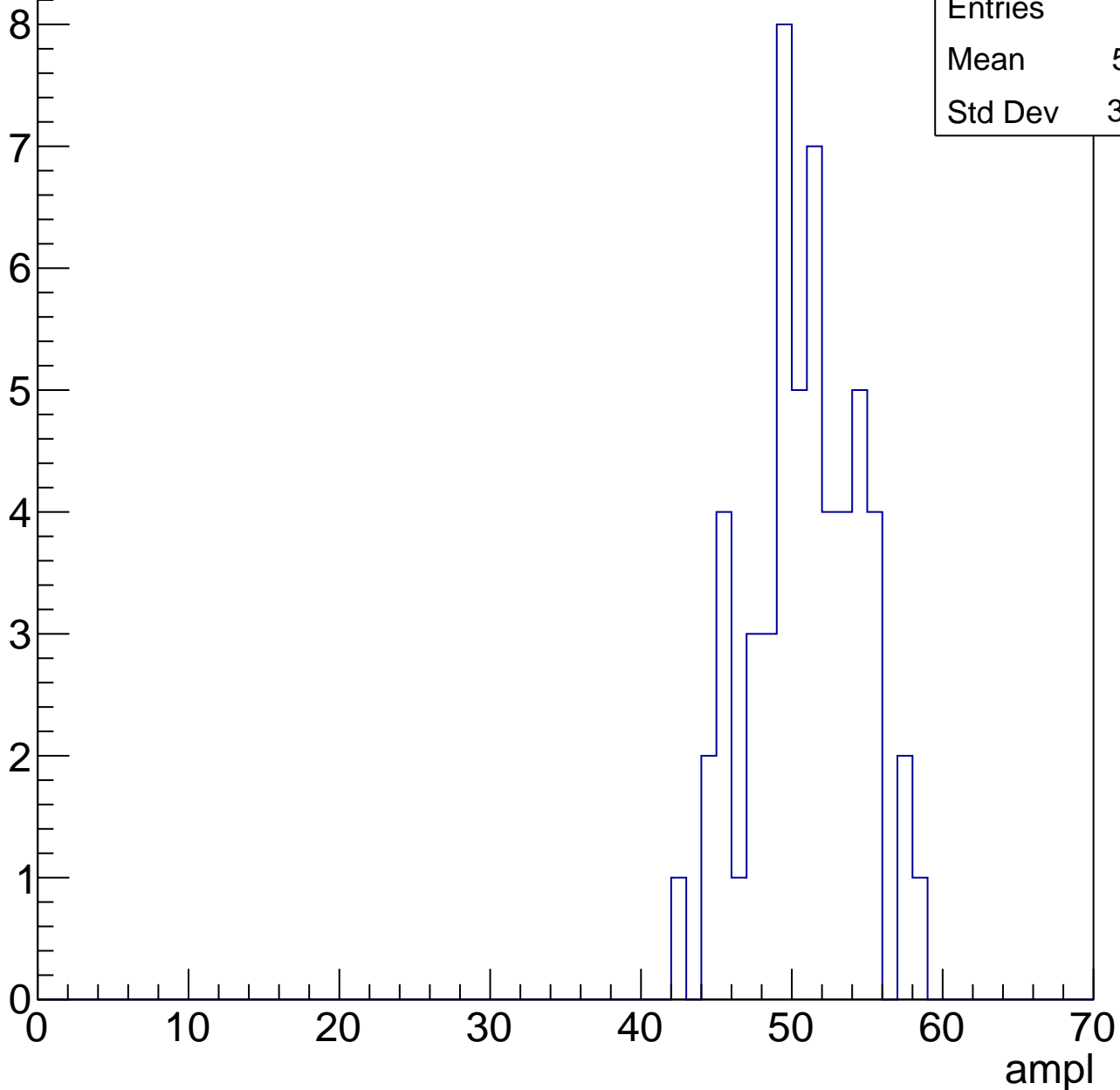


# B0L000S, U7-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	54
Mean	50.41
Std Dev	3.577



# B0L000S, U7-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

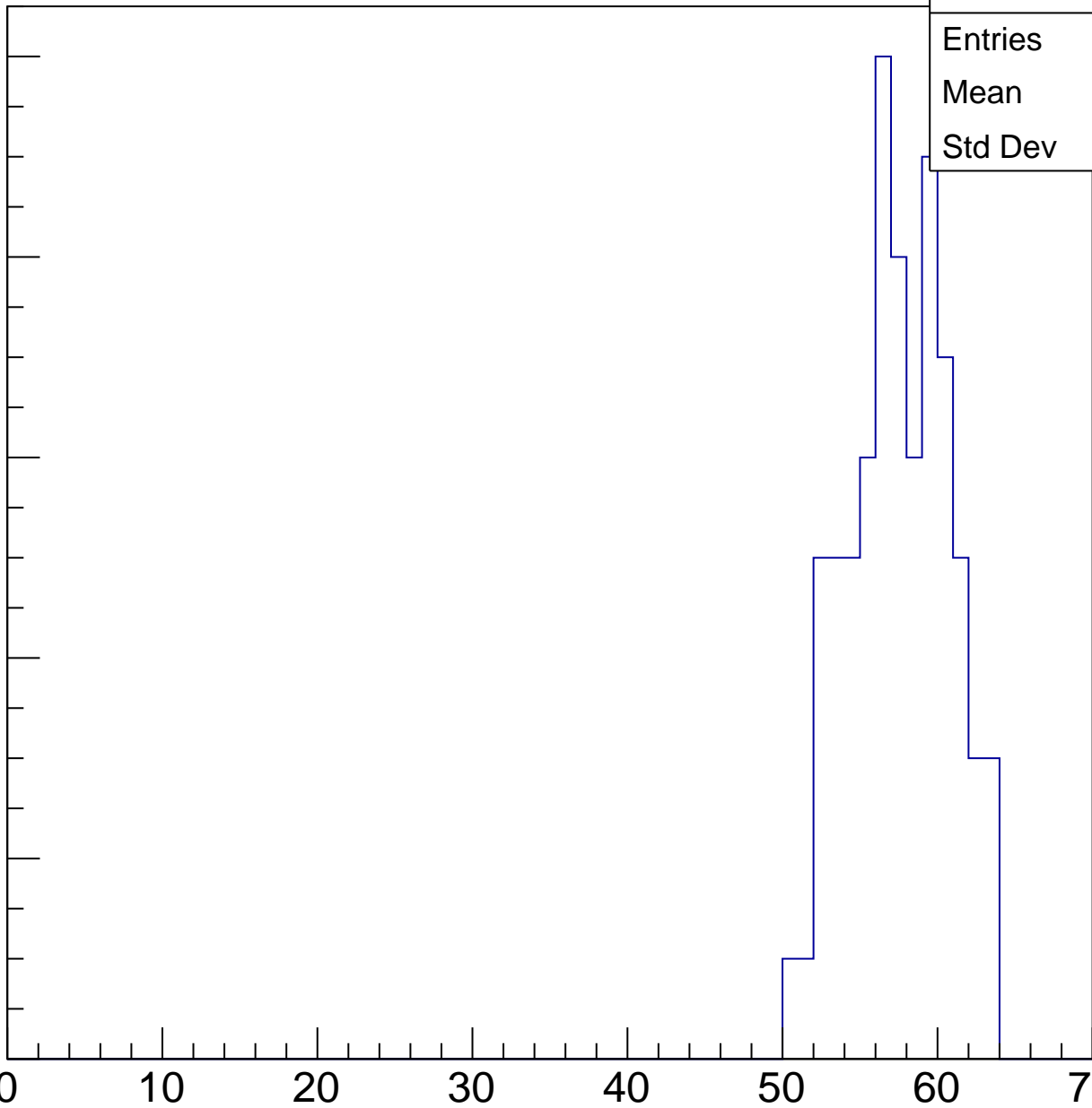
Entries	74
Mean	57.04
Std Dev	3.156

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

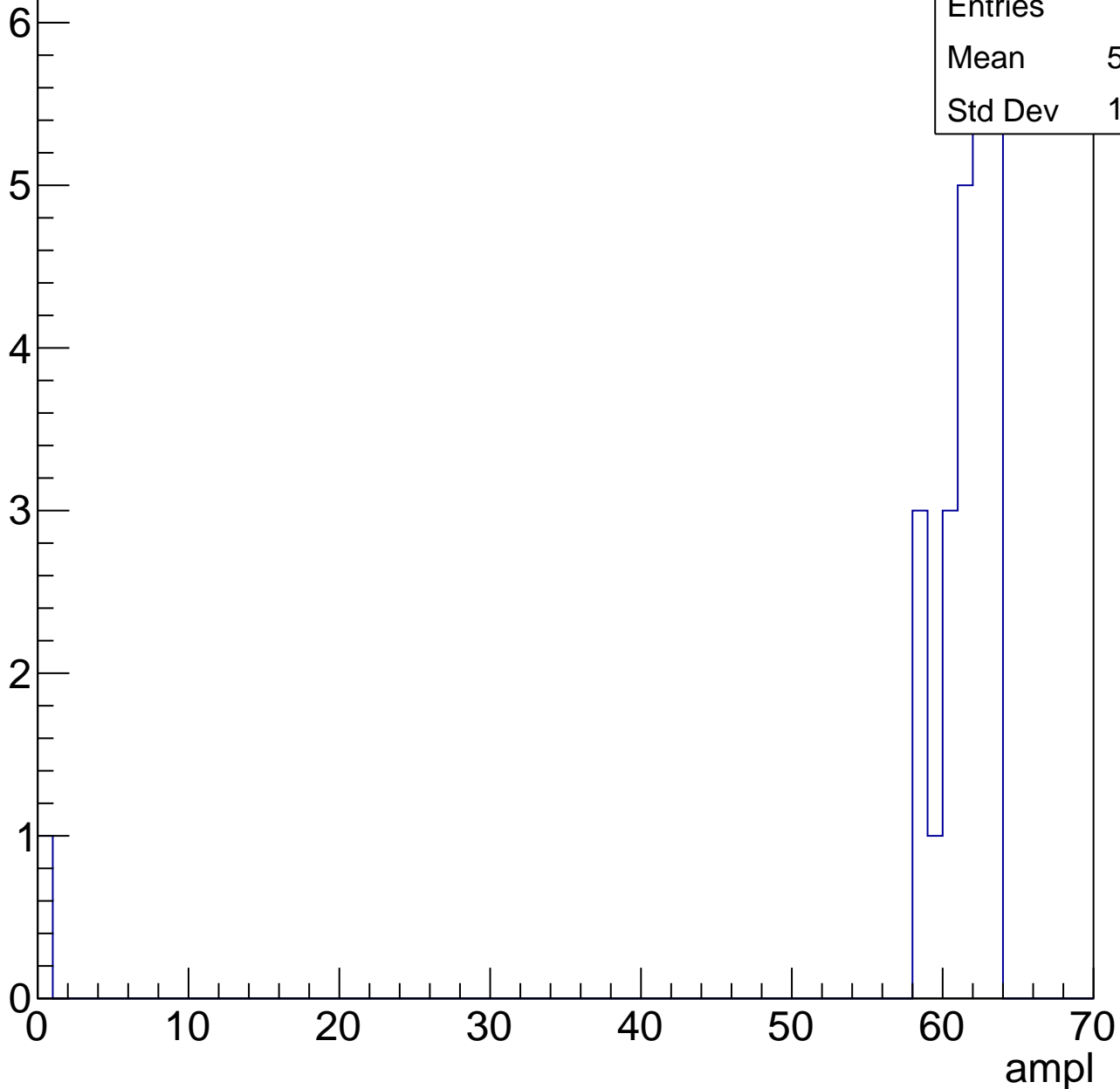


# B0L000S, U7-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

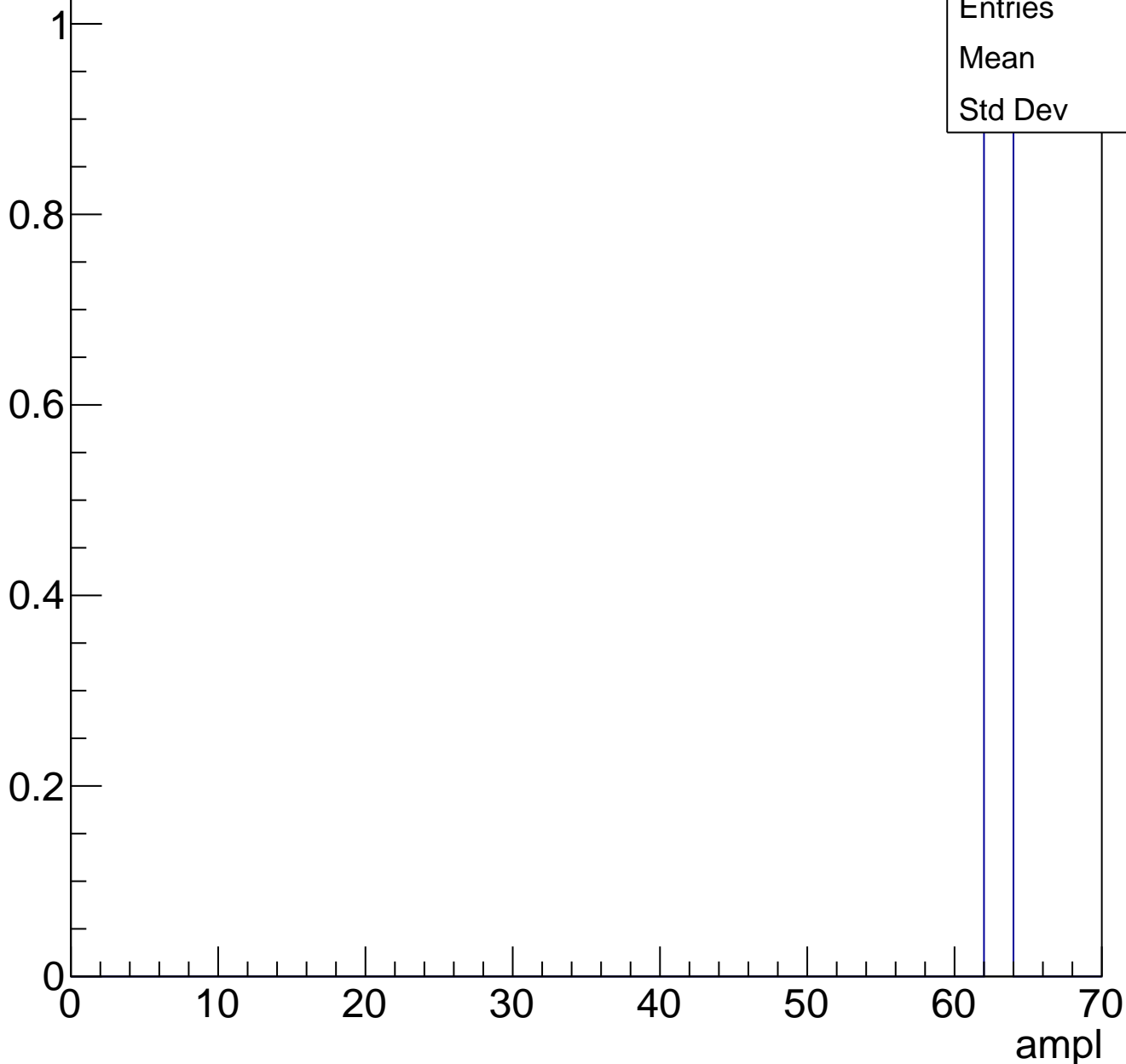
Entries	25
Mean	58.72
Std Dev	12.09



# B0L000S, U7-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

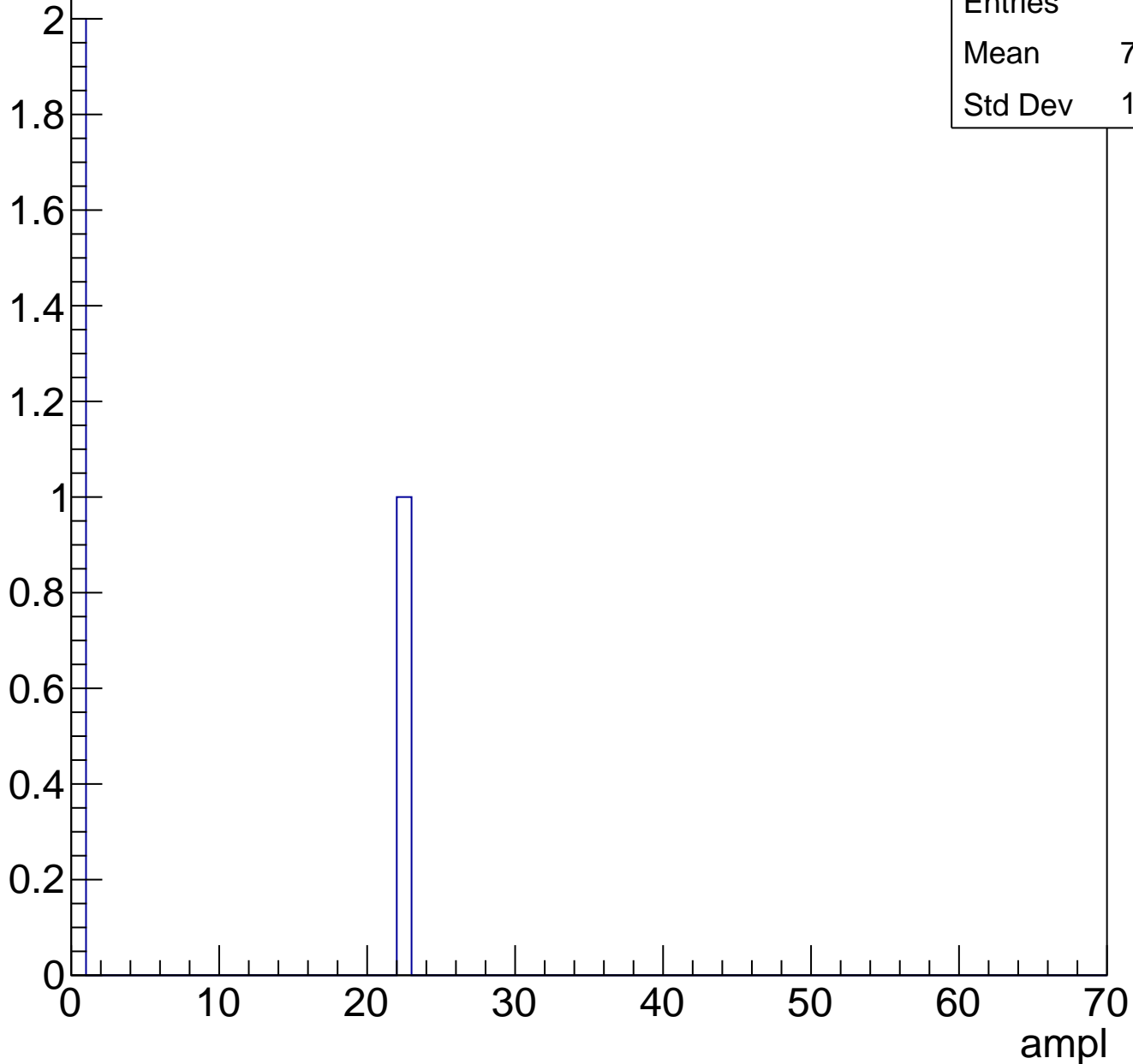




# B0L000S, U7-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	3
Mean	7.333
Std Dev	10.37

# B0L000S, U7-ch102, adc0

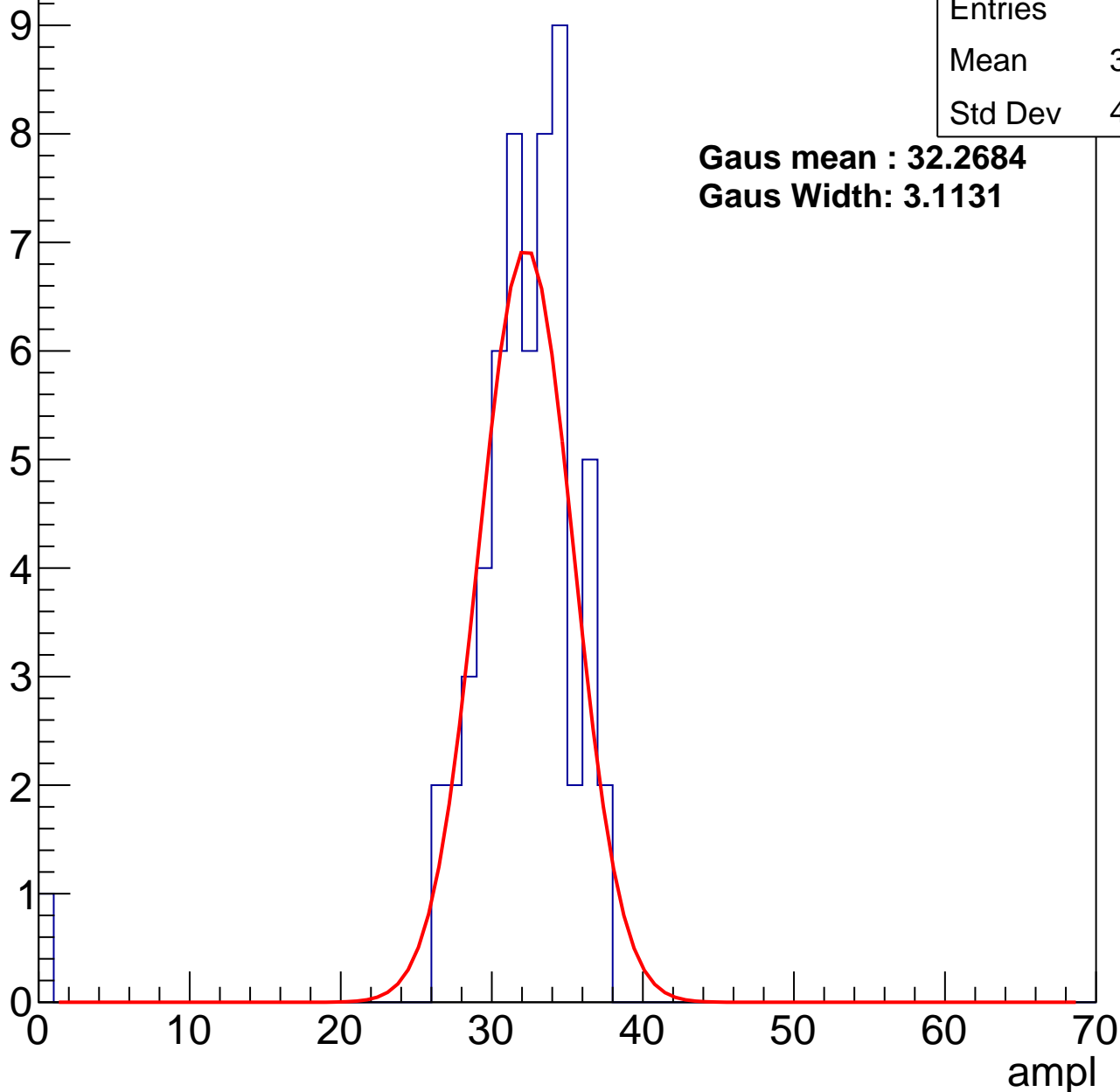
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	58
Mean	31.38
Std Dev	4.968

**Gaus mean : 32.2684**

**Gaus Width: 3.1131**

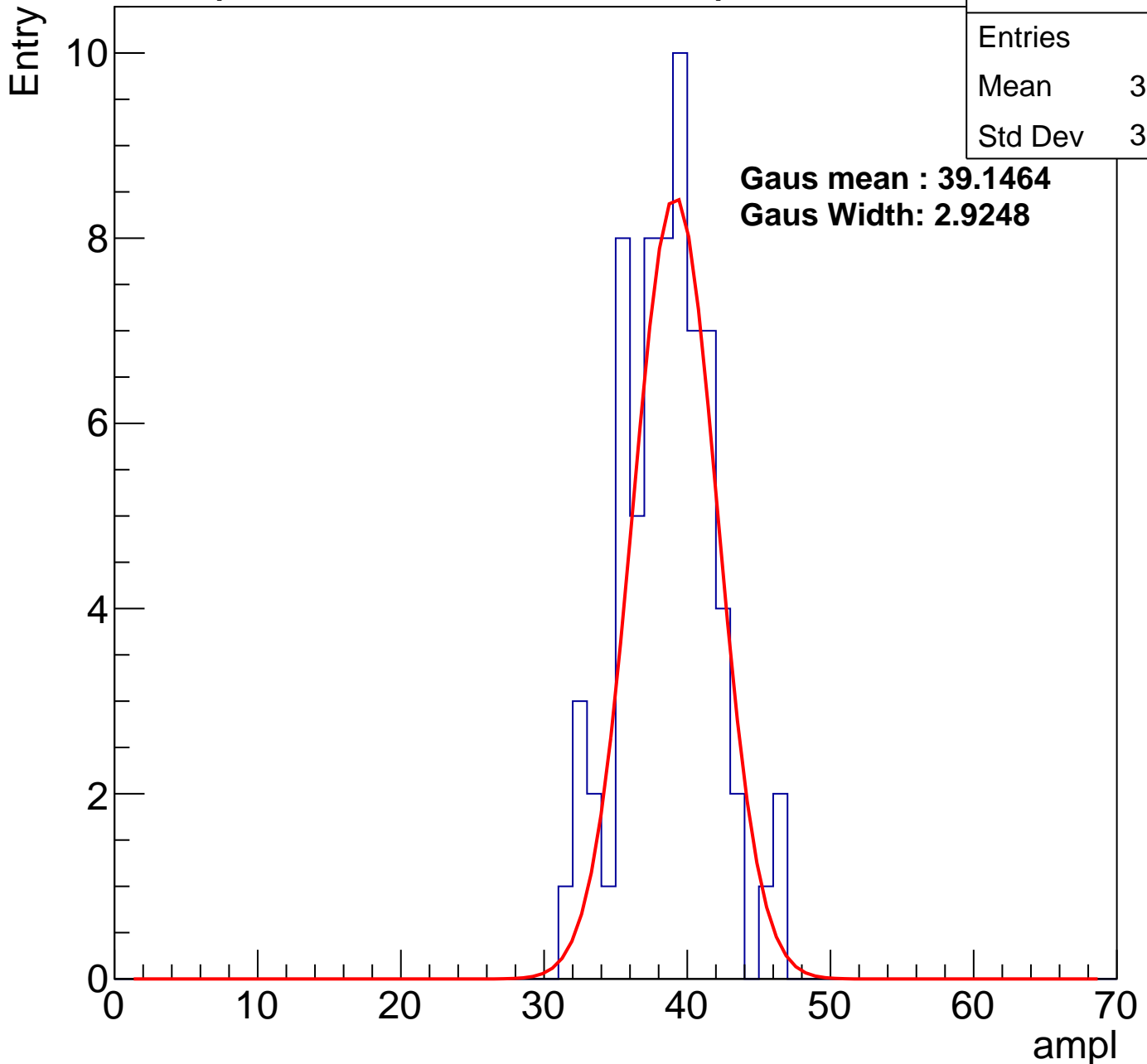


# B0L000S, U7-ch102, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	69
Mean	38.19
Std Dev	3.214

**Gaus mean : 39.1464**  
**Gaus Width: 2.9248**



# B0L000S, U7-ch102, adc2

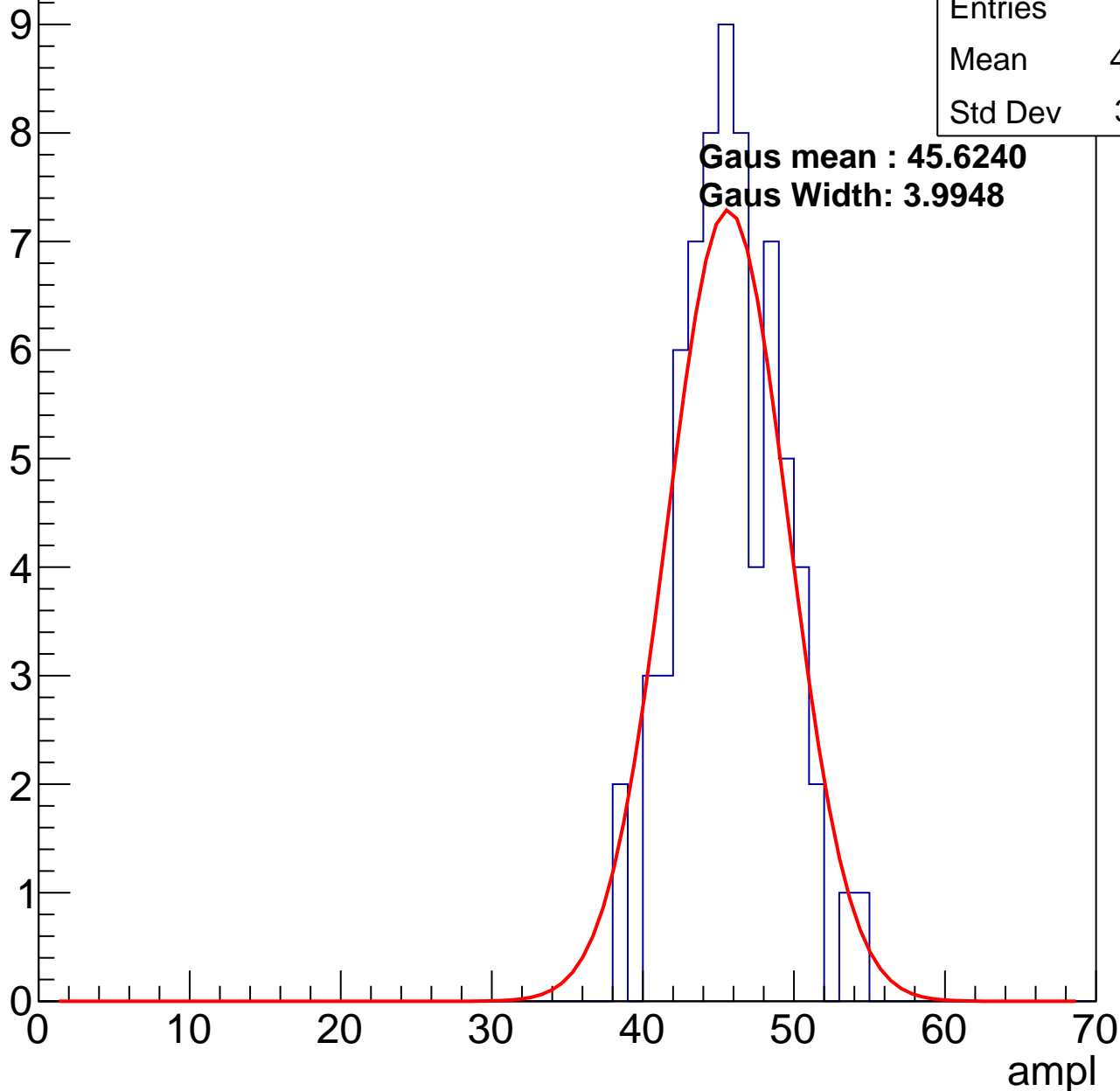
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	70
Mean	45.36
Std Dev	3.351

**Gaus mean : 45.6240**

**Gaus Width: 3.9948**

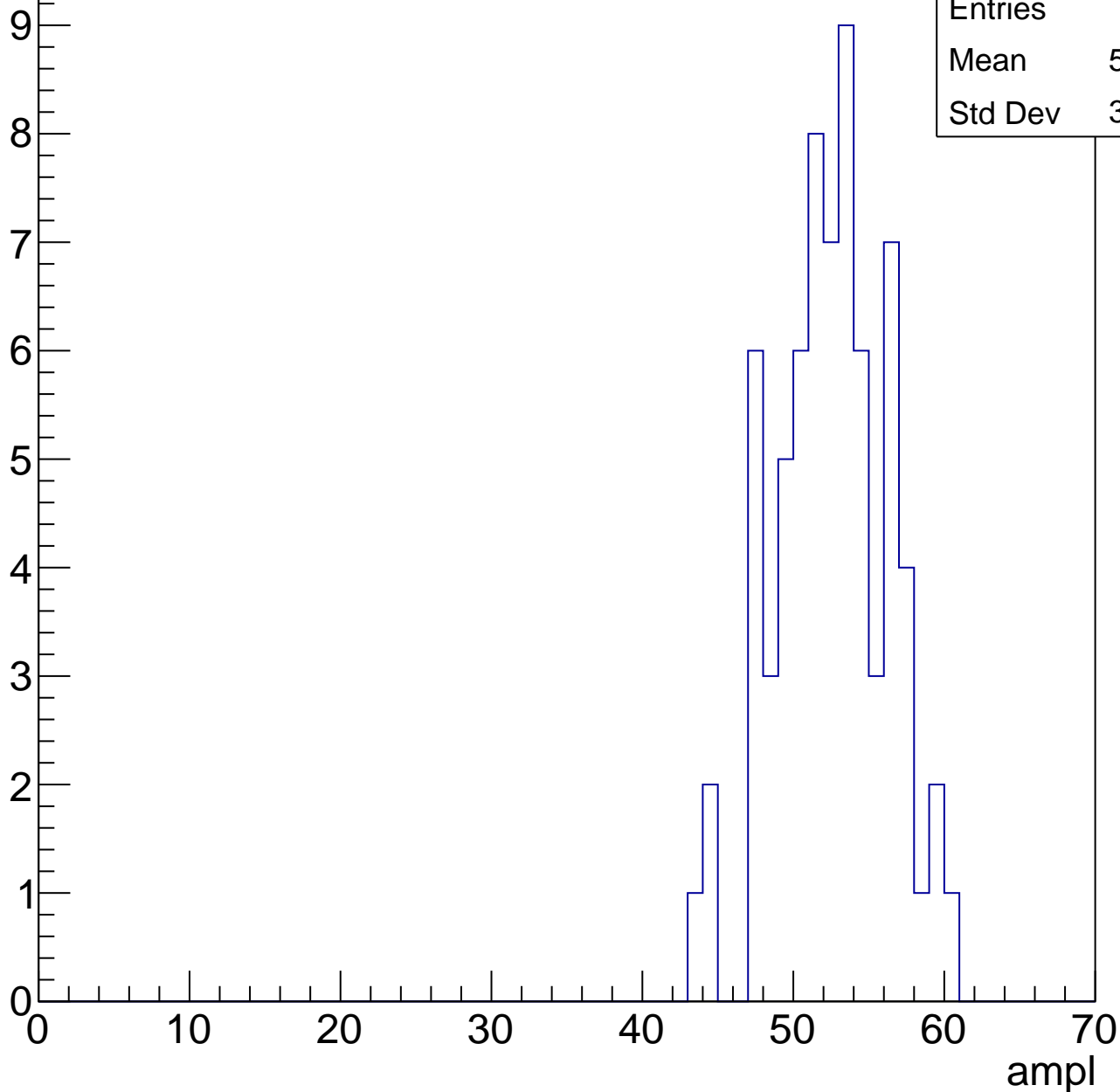


# B0L000S, U7-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

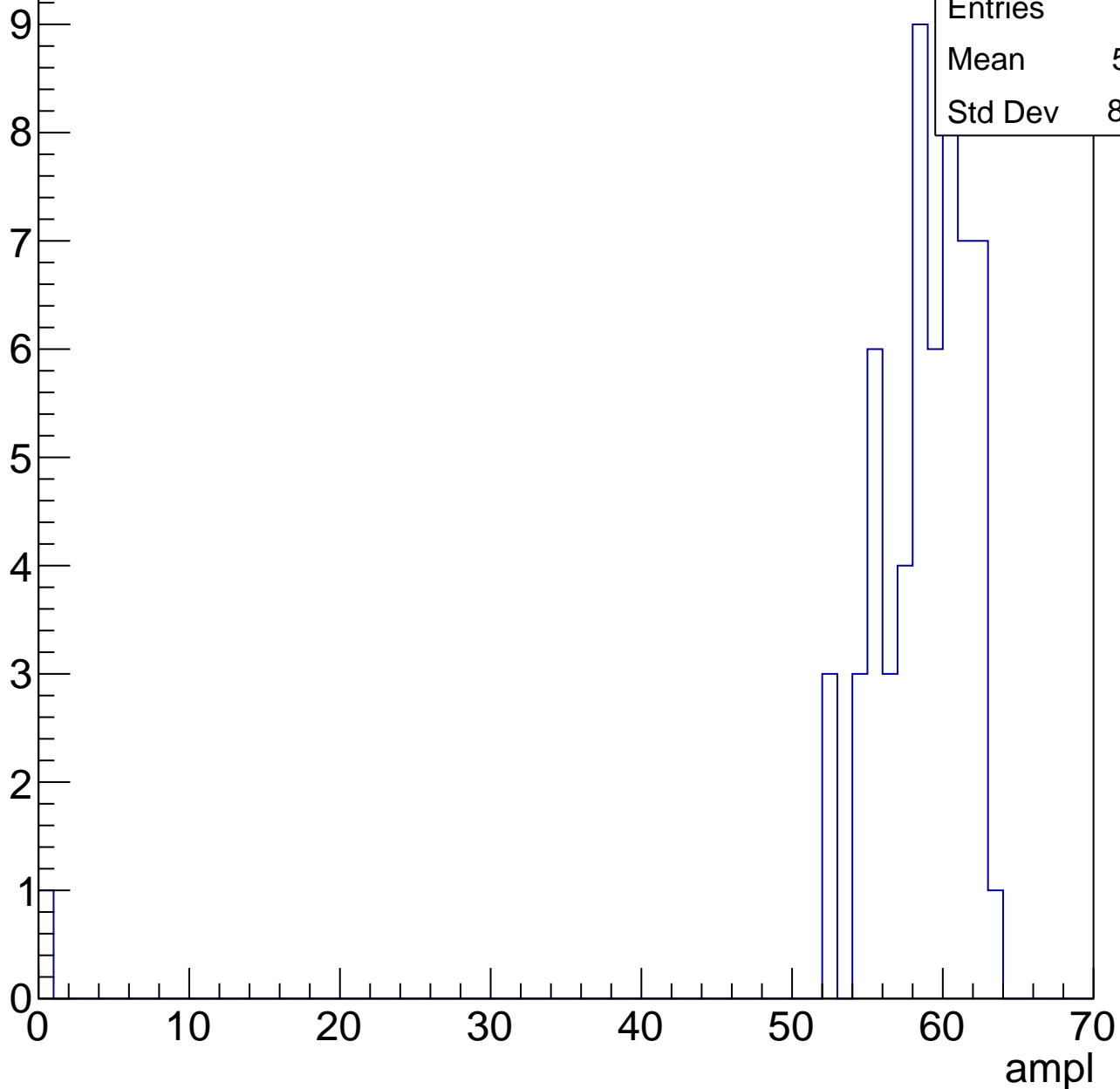
Entries	71
Mean	52.06
Std Dev	3.665



# B0L000S, U7-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

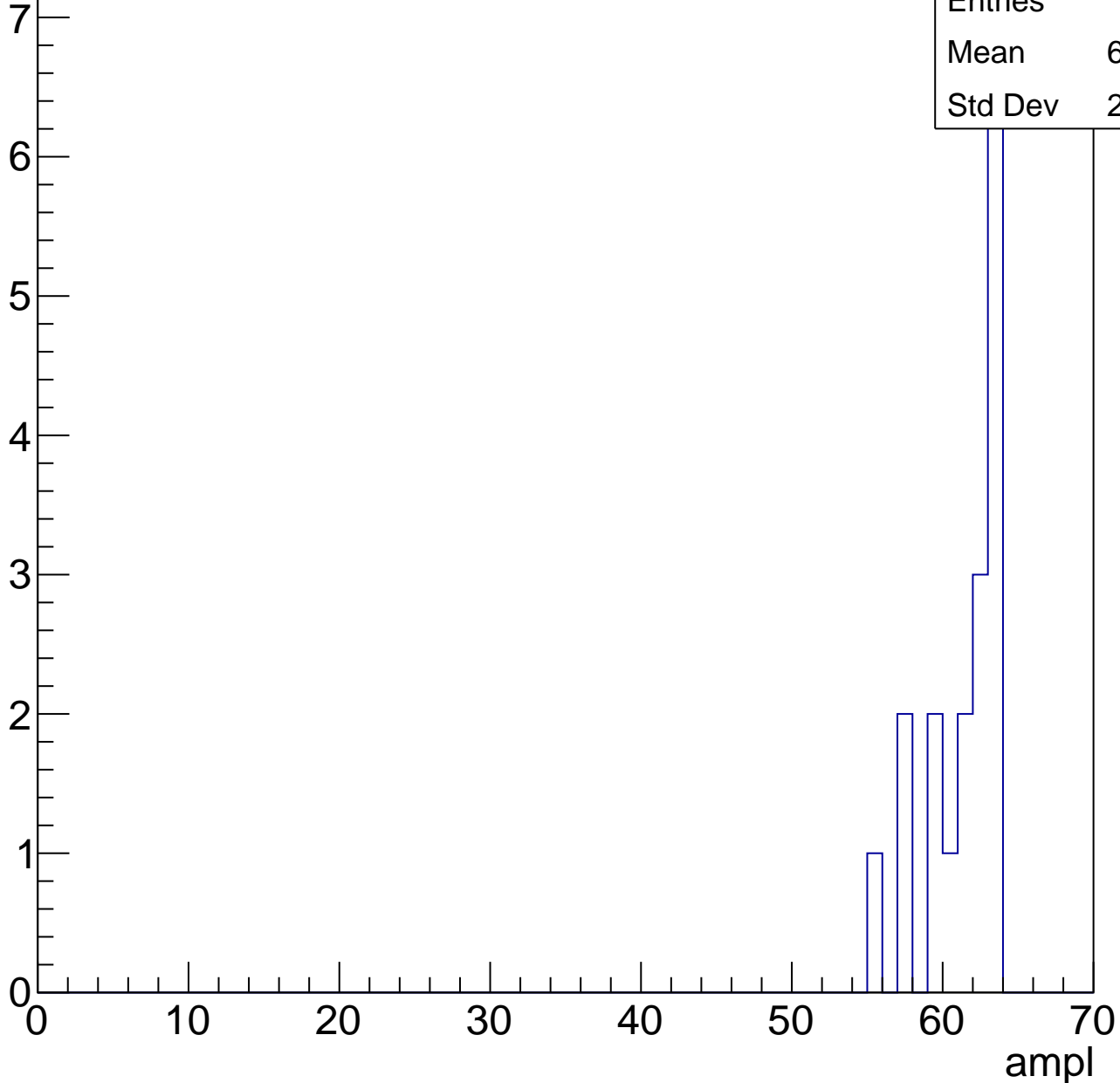


# B0L000S, U7-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	18
Mean	60.89
Std Dev	2.447



# B0L000S, U7-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

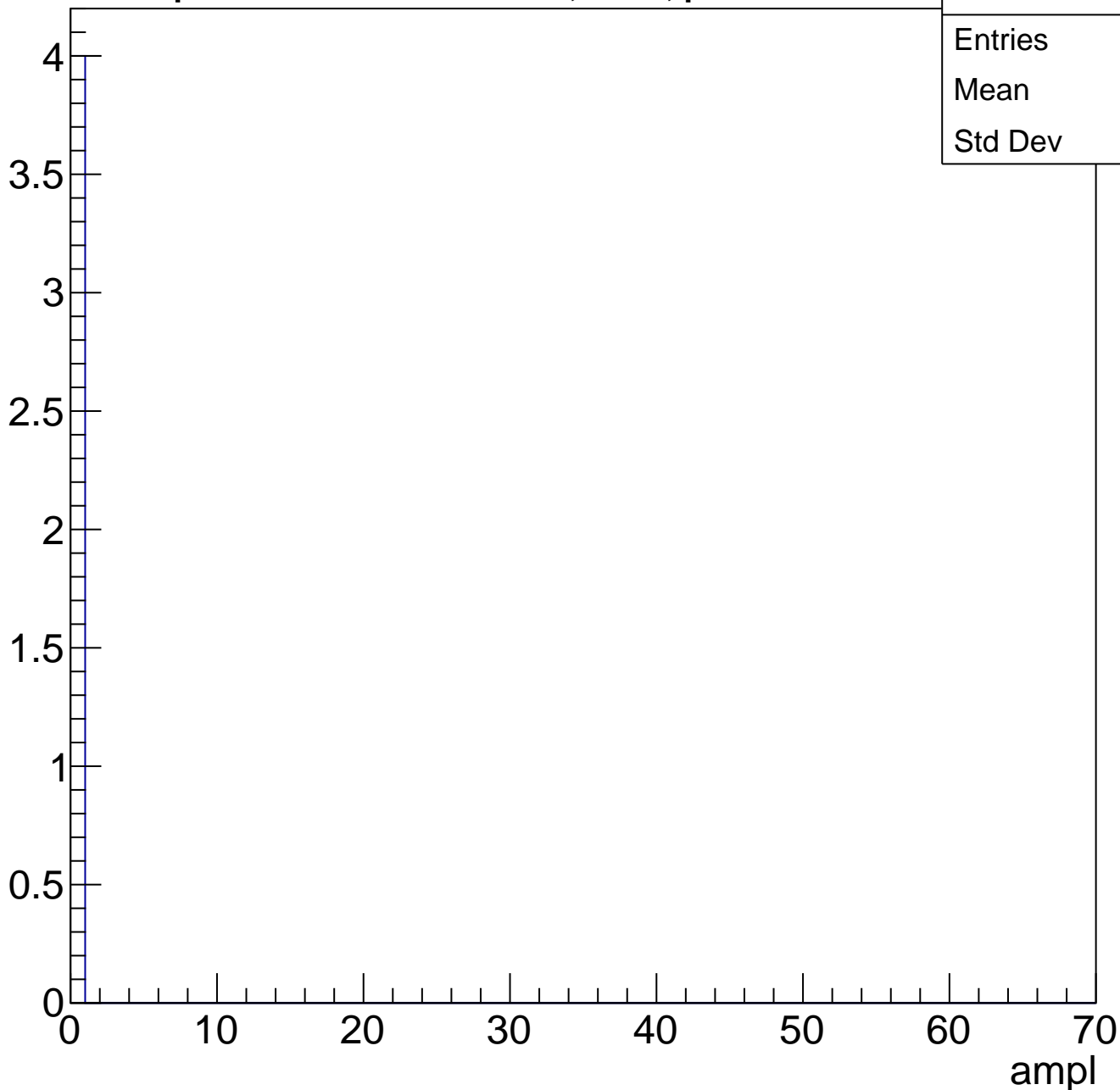




# B0L000S, U7-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	4
Mean	0
Std Dev	0

# B0L000S, U7-ch103, adc0

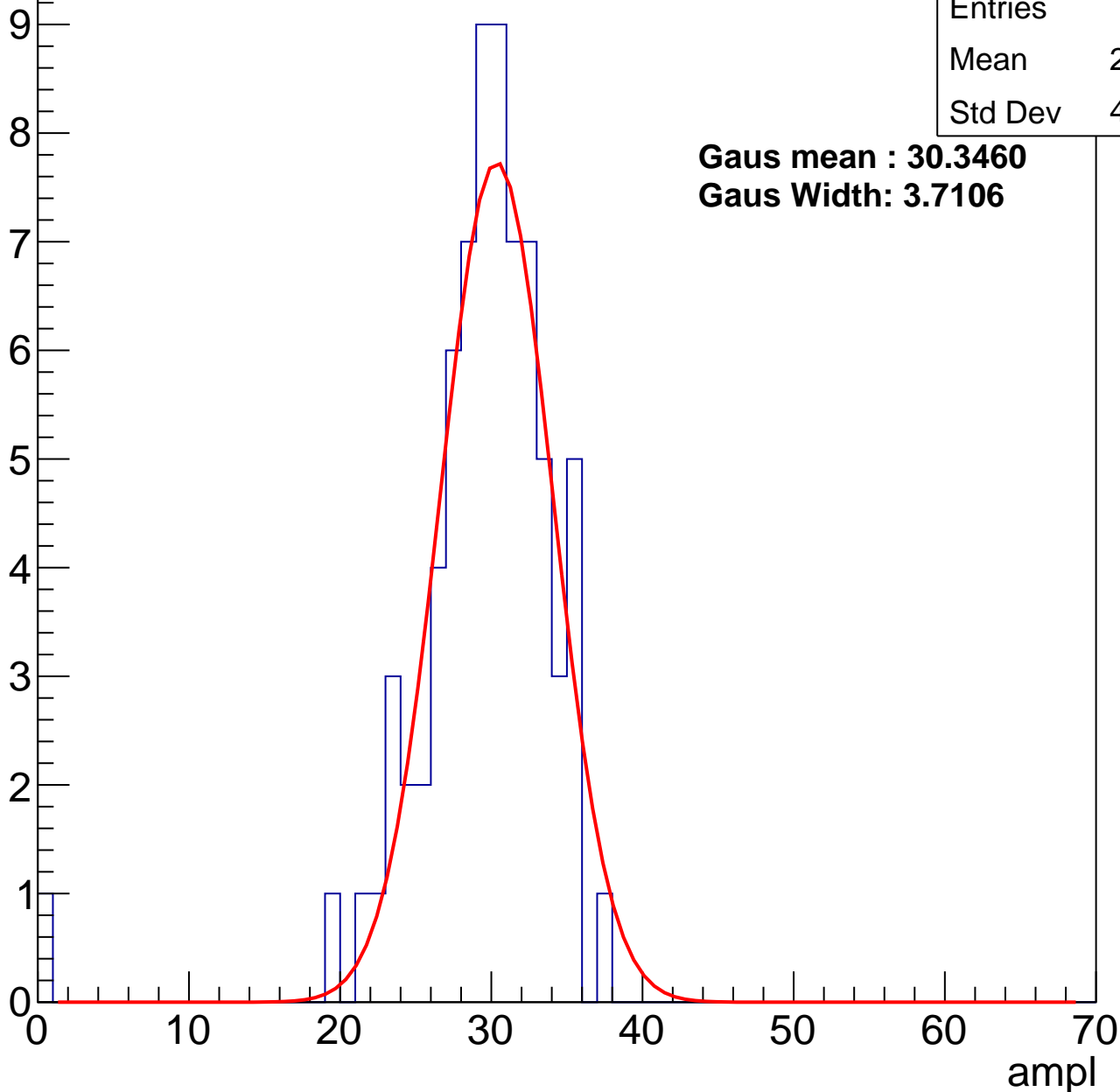
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	74
Mean	28.95
Std Dev	4.945

**Gaus mean : 30.3460**

**Gaus Width: 3.7106**

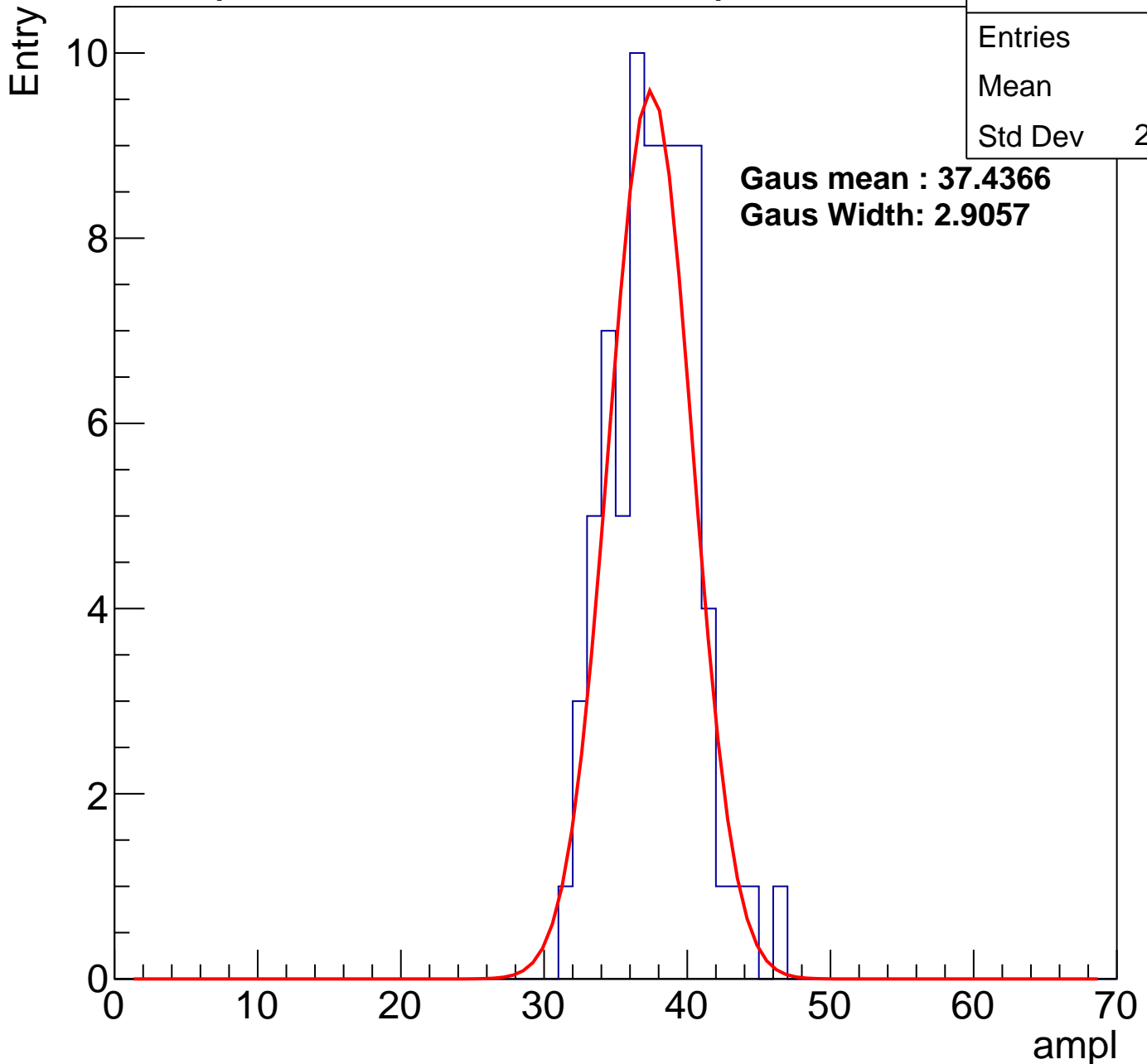


# B0L000S, U7-ch103, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	75
Mean	37.2
Std Dev	2.971

**Gaus mean : 37.4366**  
**Gaus Width: 2.9057**



# B0L000S, U7-ch103, adc2

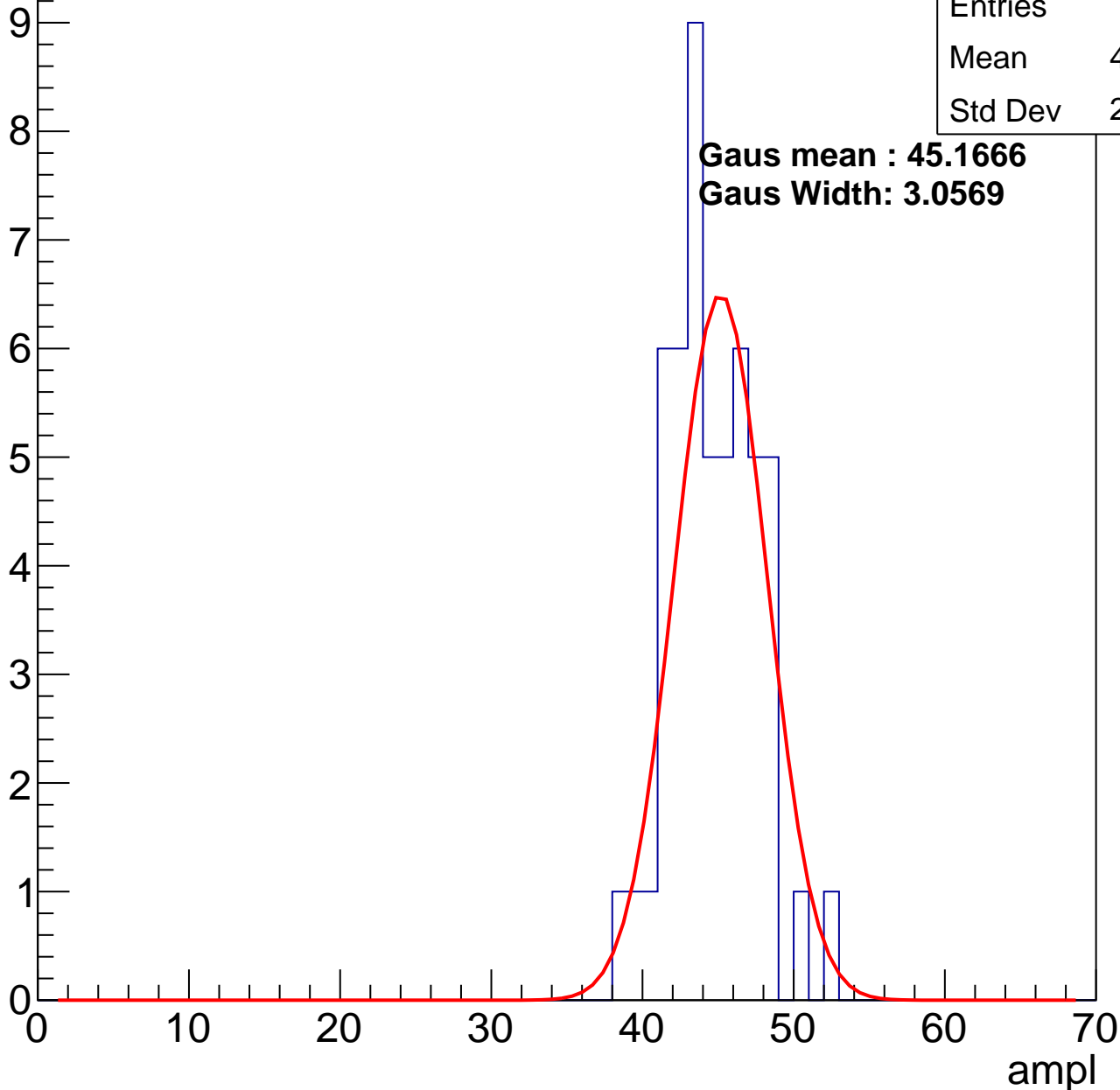
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	52
Mean	44.23
Std Dev	2.826

**Gaus mean : 45.1666**

**Gaus Width: 3.0569**



# B0L000S, U7-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

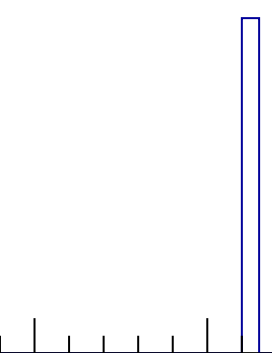
Entries	80
Mean	50.06
Std Dev	3.812

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

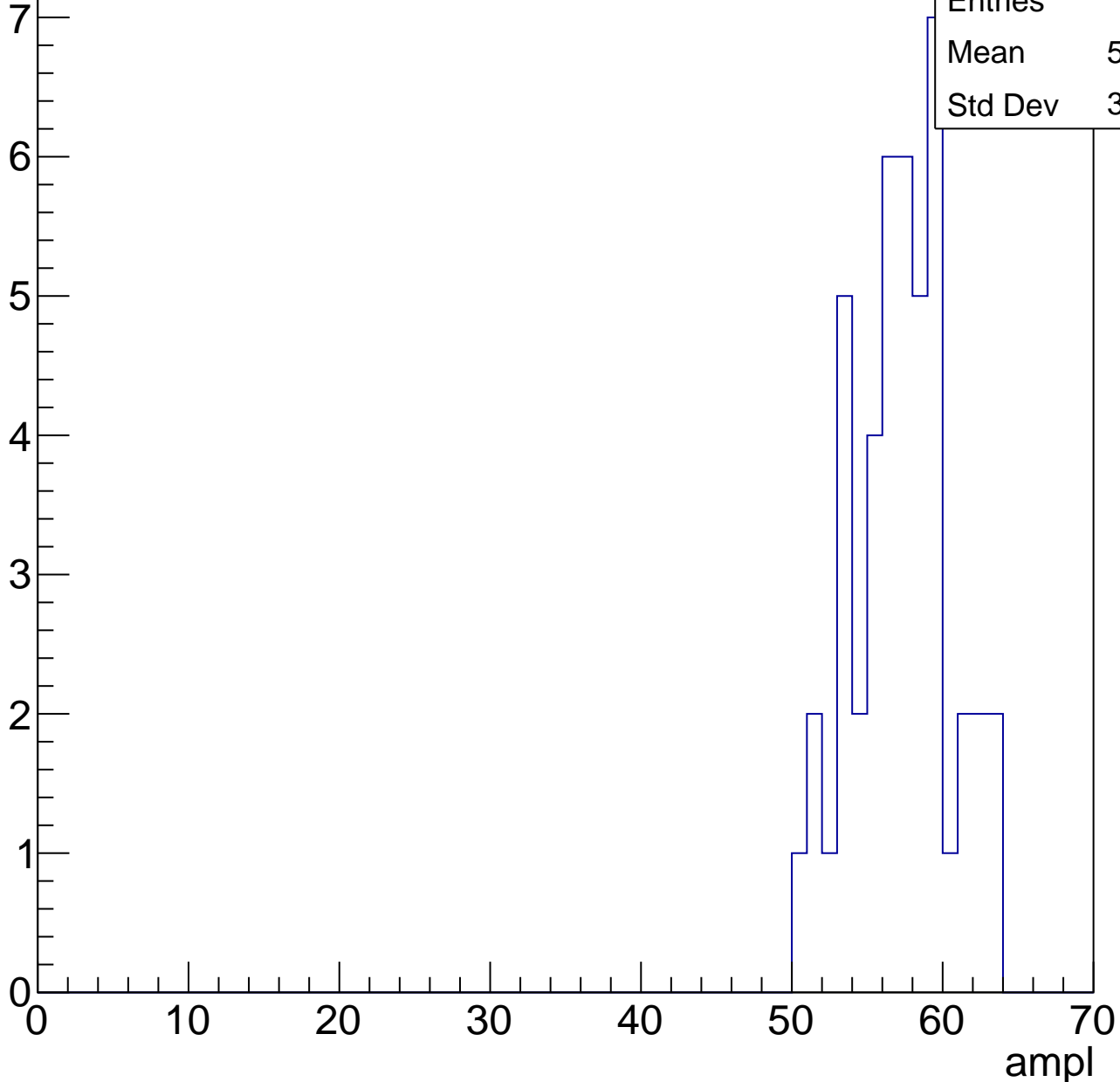


# B0L000S, U7-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

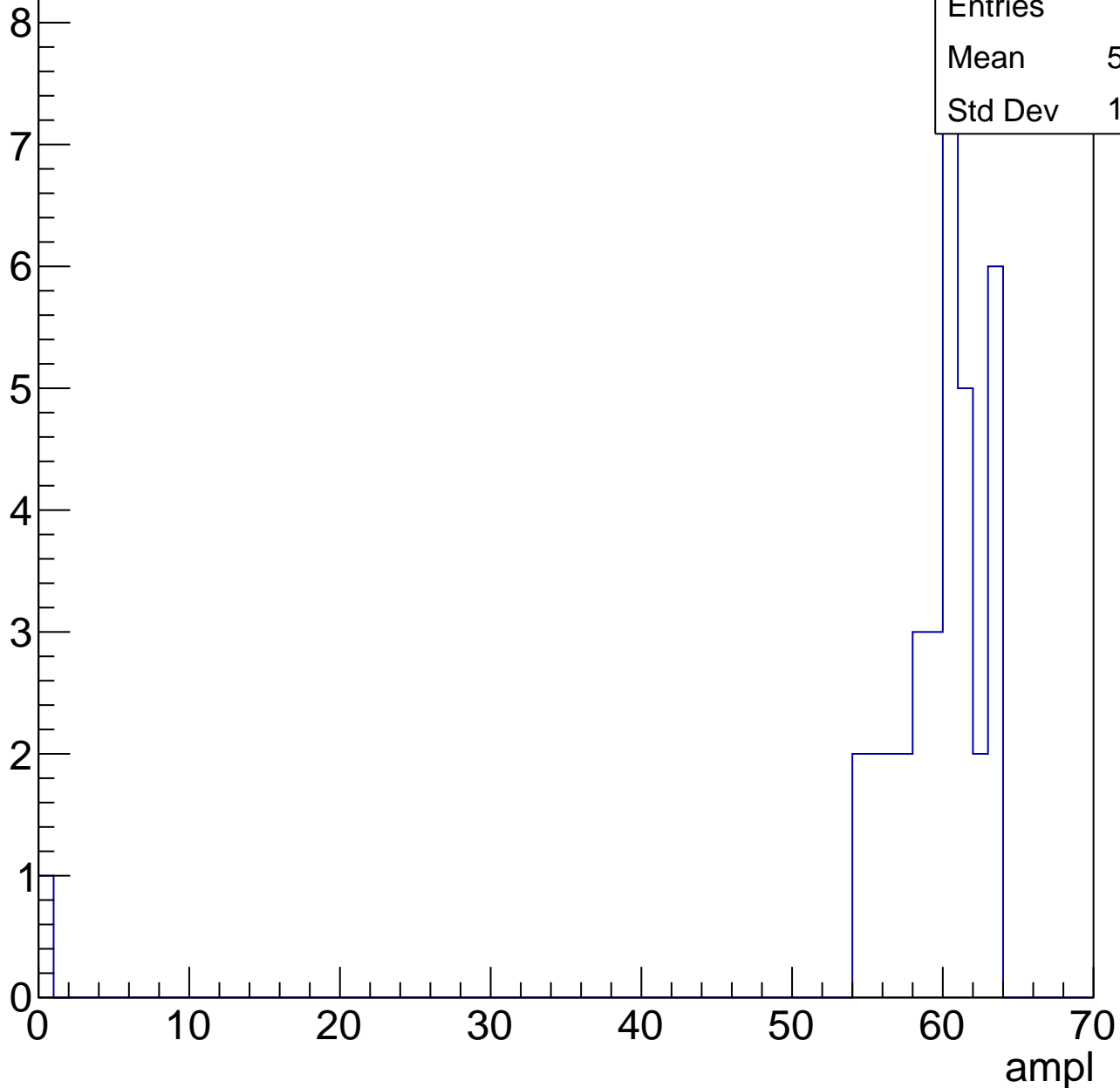
Entries	46
Mean	56.74
Std Dev	3.158



# B0L000S, U7-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

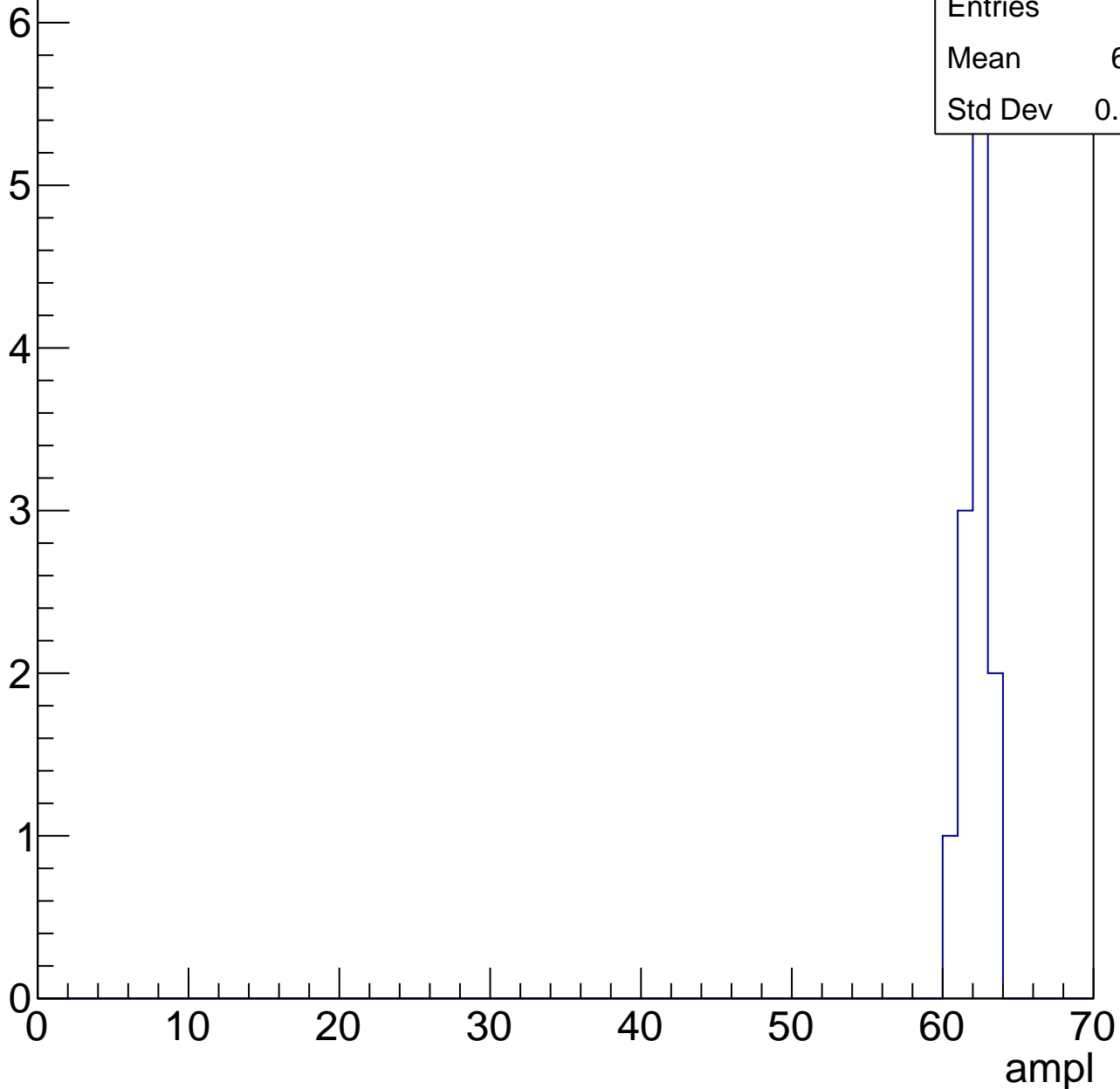


# B0L000S, U7-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	12
Mean	61.75
Std Dev	0.8292





# B0L000S, U7-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L000S, U7-ch104, adc0

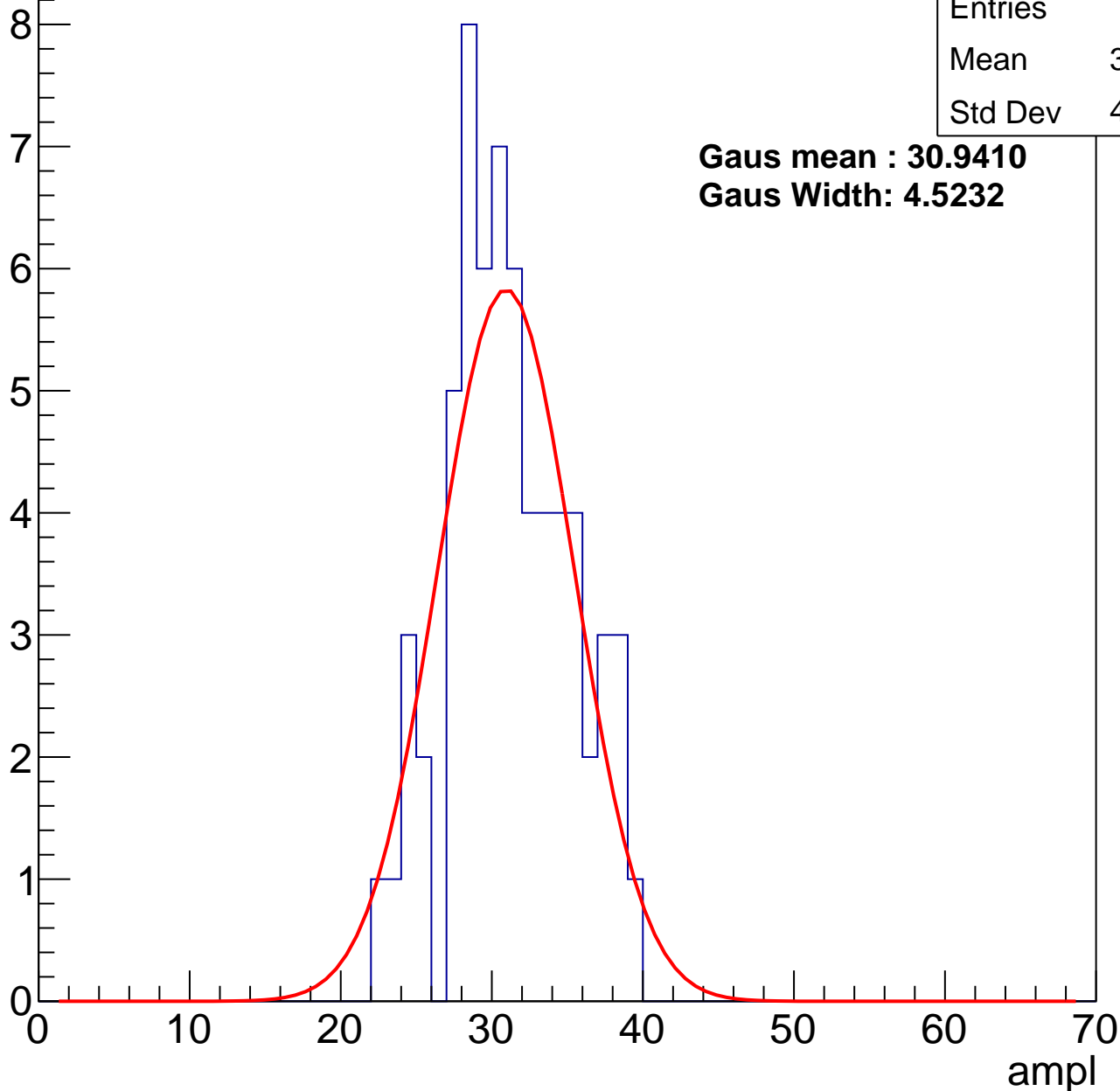
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	64
Mean	30.75
Std Dev	4.016

**Gaus mean : 30.9410**

**Gaus Width: 4.5232**



# B0L000S, U7-ch104, adc1

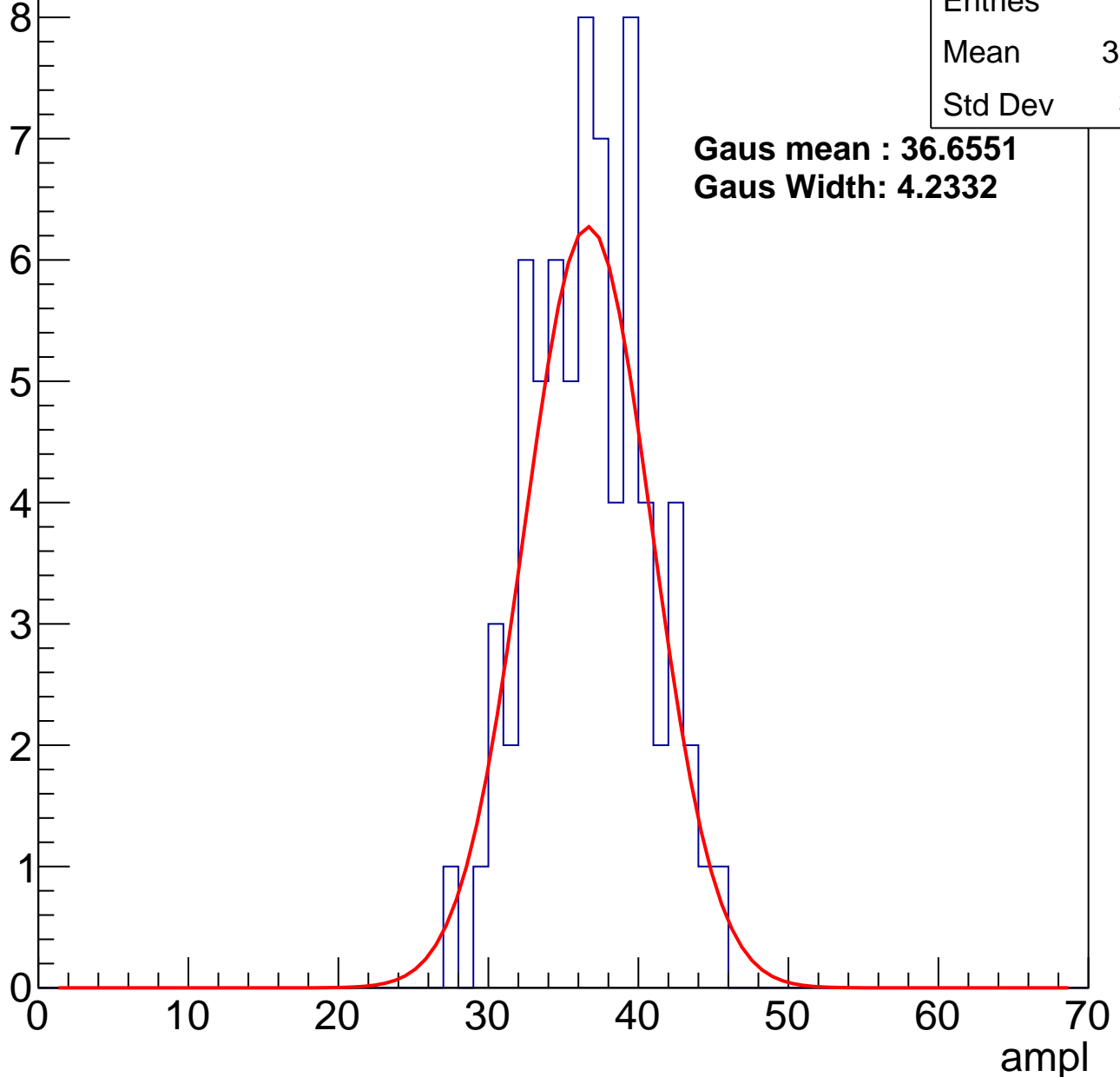
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	70
Mean	36.29
Std Dev	3.87

**Gaus mean : 36.6551**

**Gaus Width: 4.2332**



# B0L000S, U7-ch104, adc2

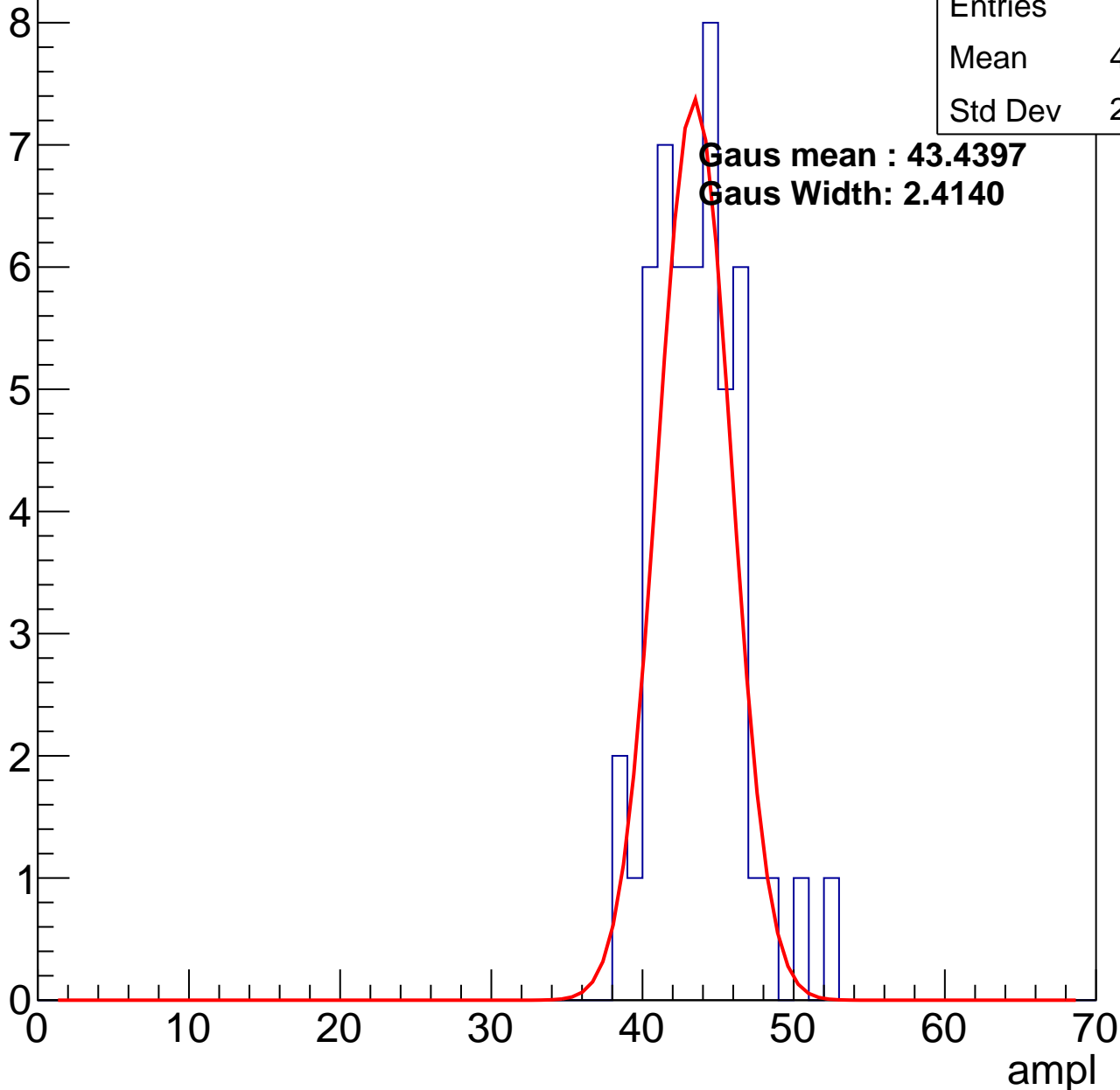
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	51
Mean	43.18
Std Dev	2.819

**Gaus mean : 43.4397**

**Gaus Width: 2.4140**

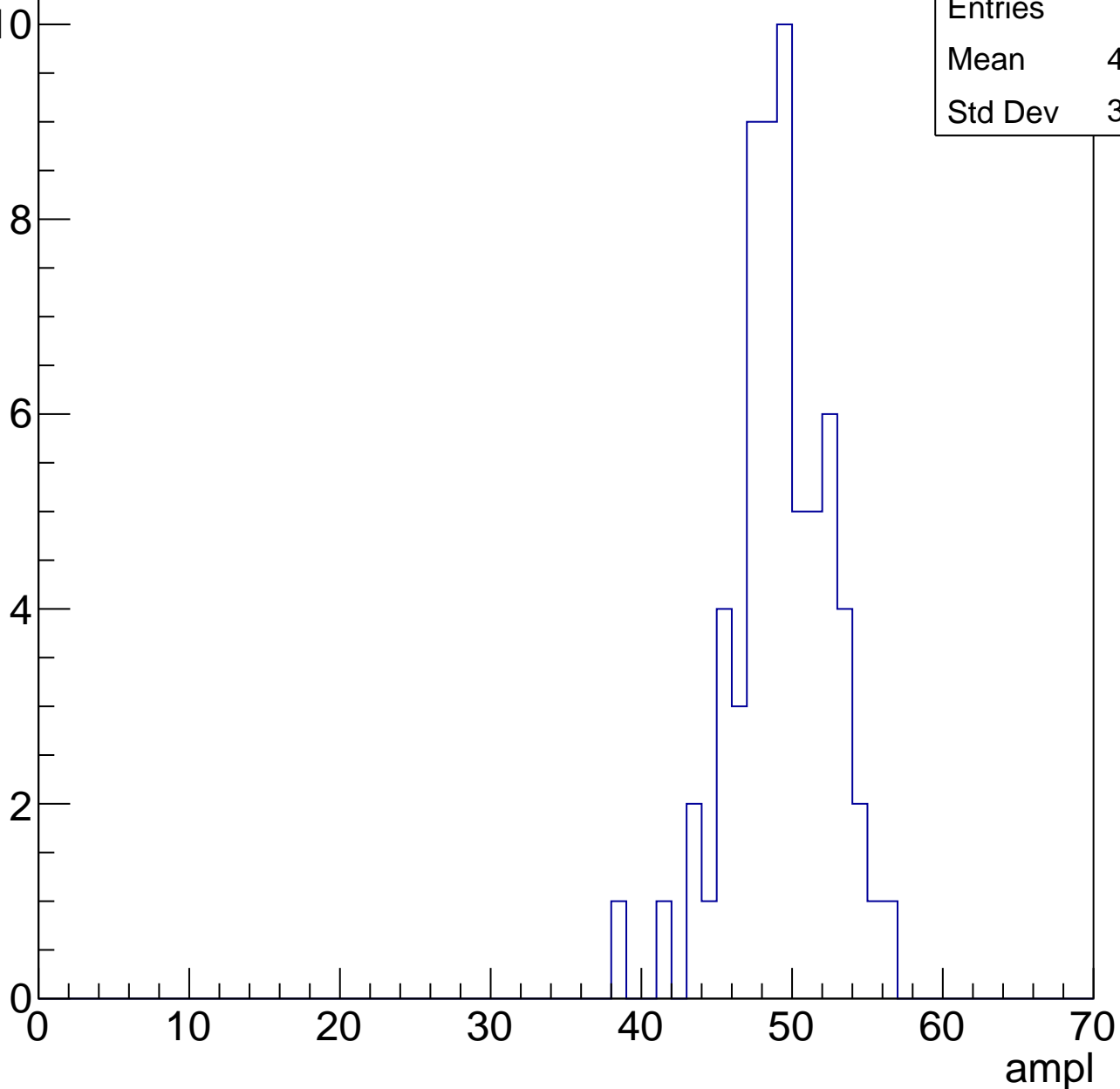


# B0L000S, U7-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	64
Mean	48.75
Std Dev	3.288

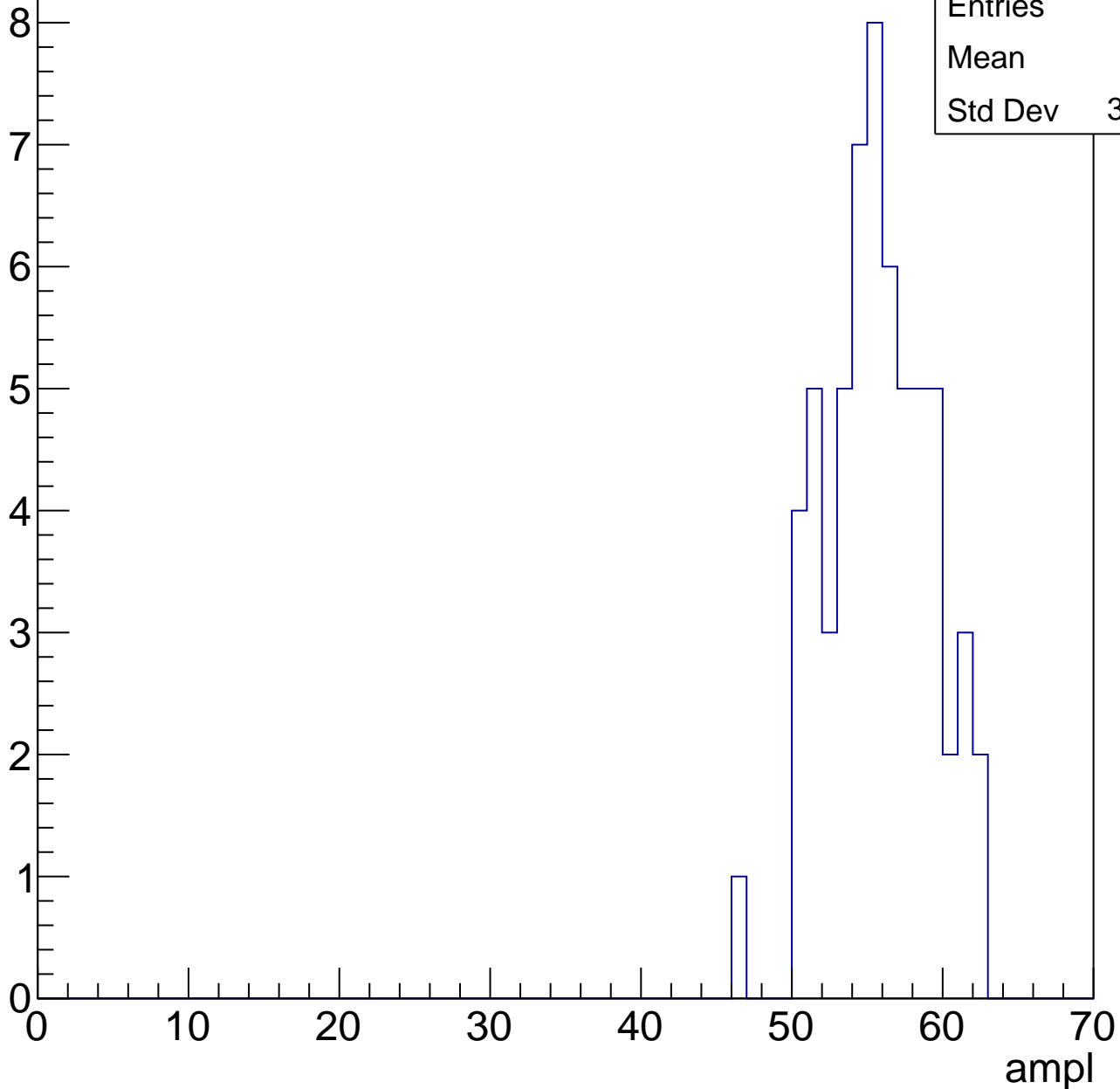


# B0L000S, U7-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	61
Mean	55.3
Std Dev	3.428



# B0L000S, U7-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	53
Mean	58.62
Std Dev	8.51

ampl

0

10

20

30

40

50

60

70

# B0L000S, U7-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L000S, U7-ch105, adc0

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	74
Mean	30.45
Std Dev	3.362

**Gaus mean : 31.0700**

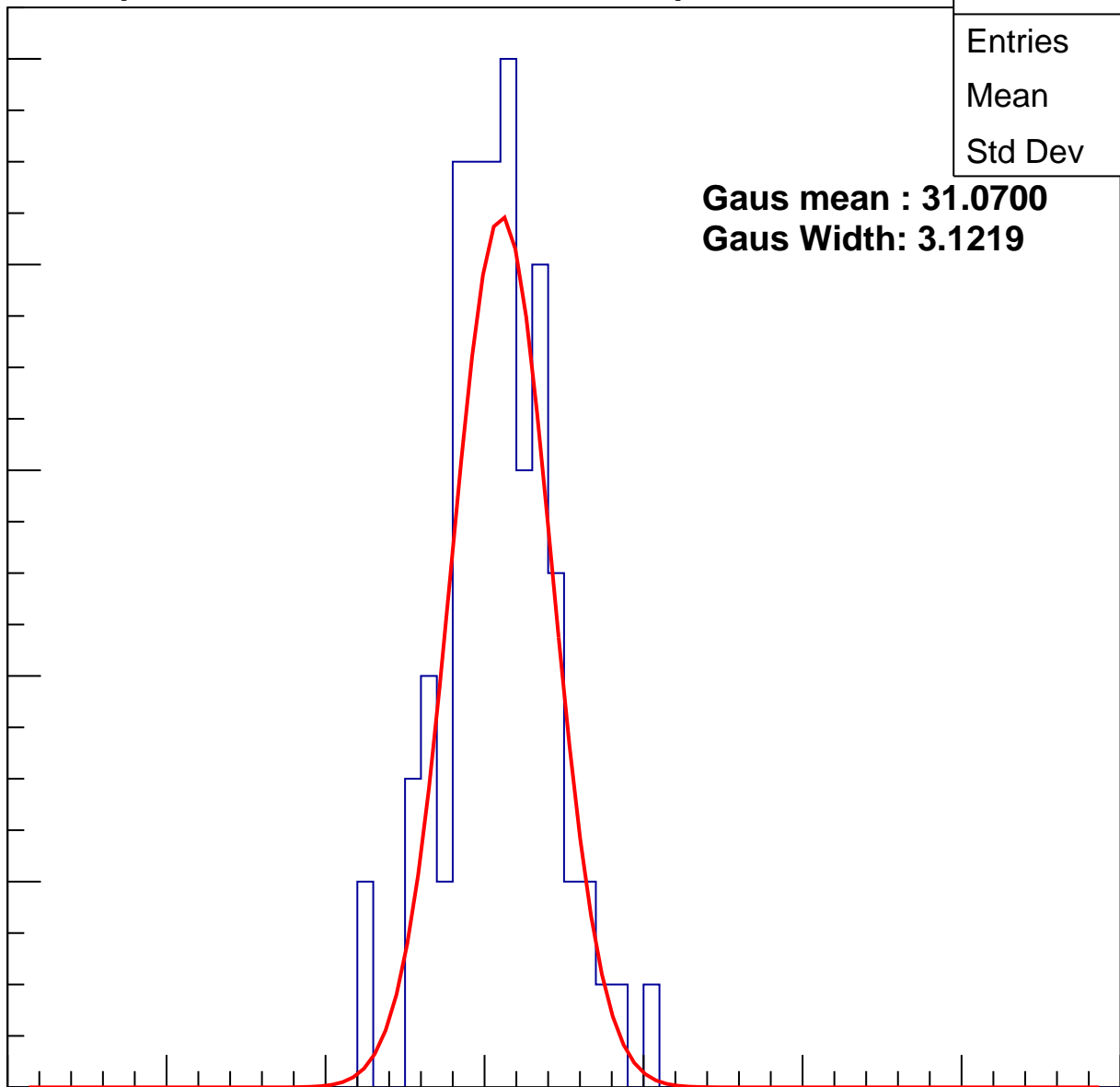
**Gaus Width: 3.1219**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L000S, U7-ch105, adc1

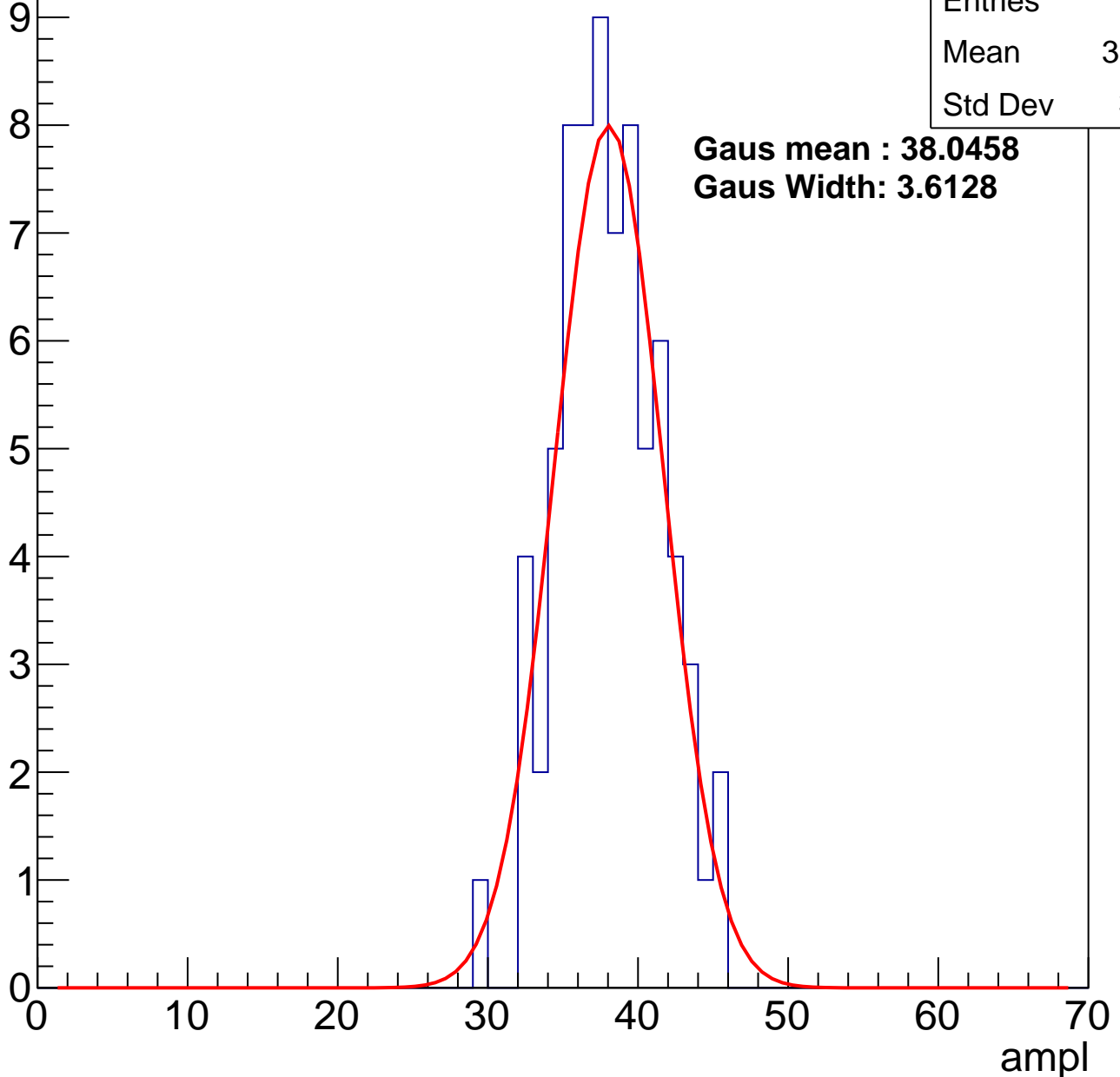
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	73
Mean	37.66
Std Dev	3.34

**Gaus mean : 38.0458**

**Gaus Width: 3.6128**



# B0L000S, U7-ch105, adc2

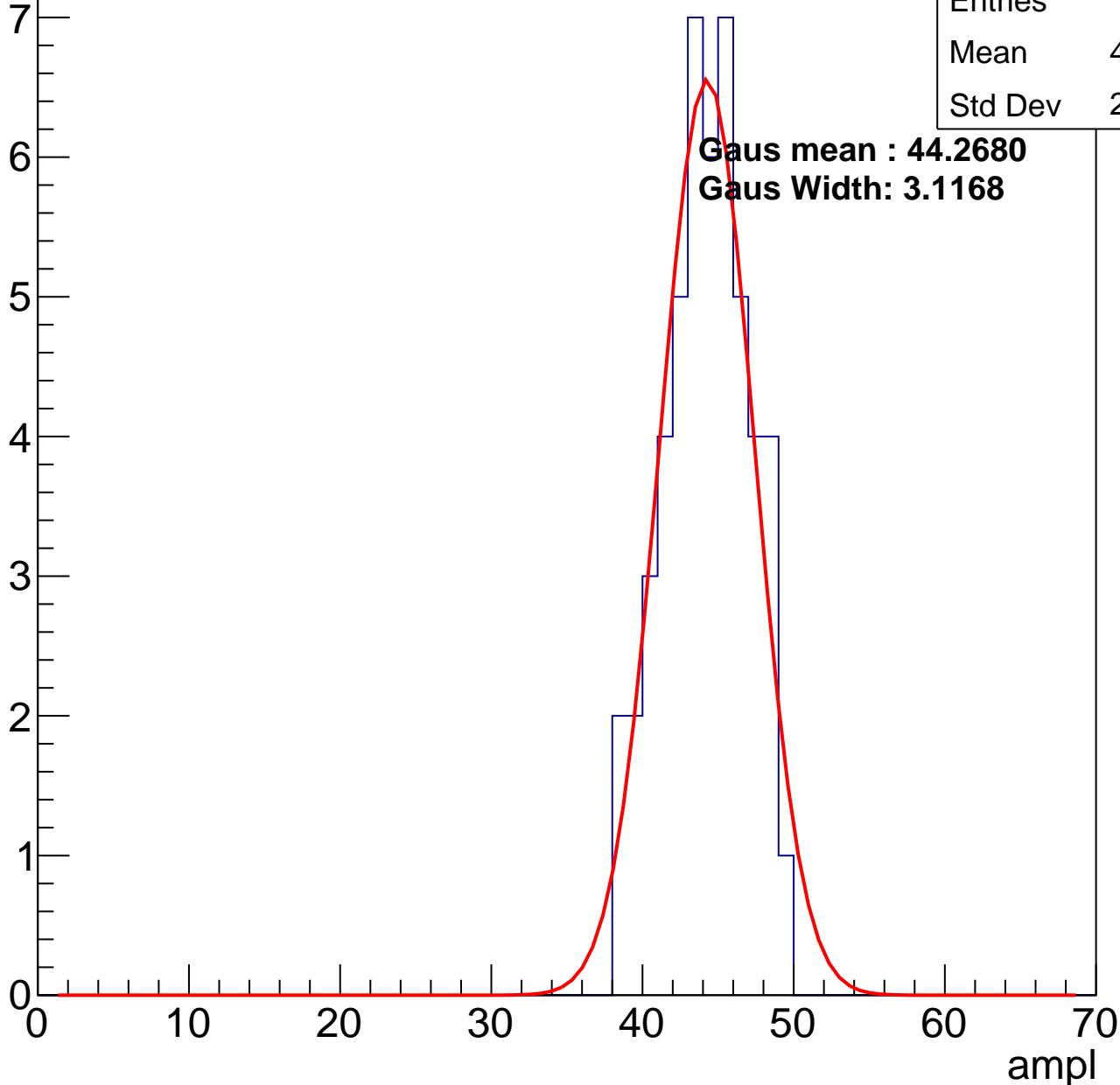
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	50
Mean	43.74
Std Dev	2.763

**Gaus mean : 44.2680**

**Gaus Width: 3.1168**

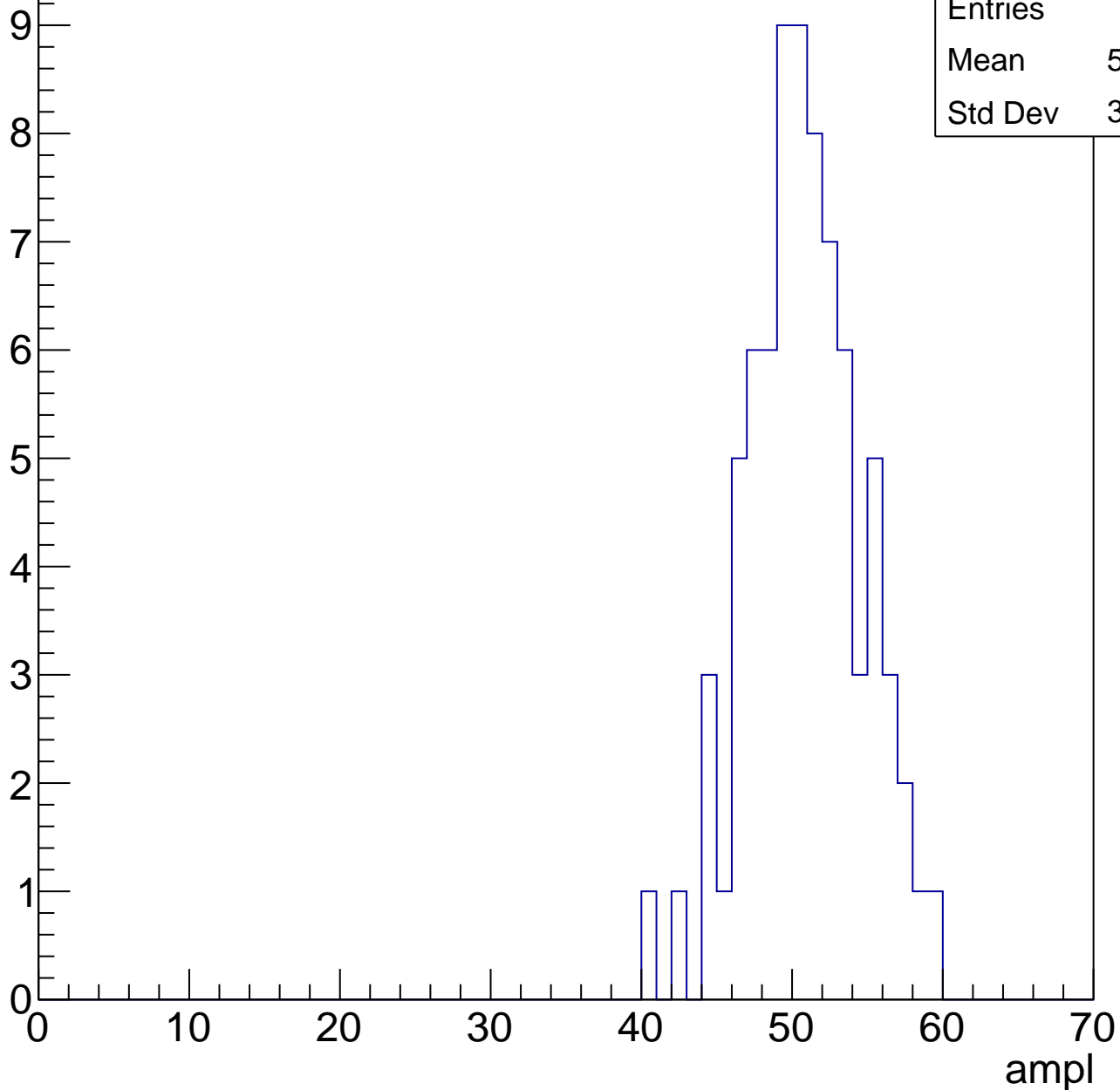


# B0L000S, U7-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

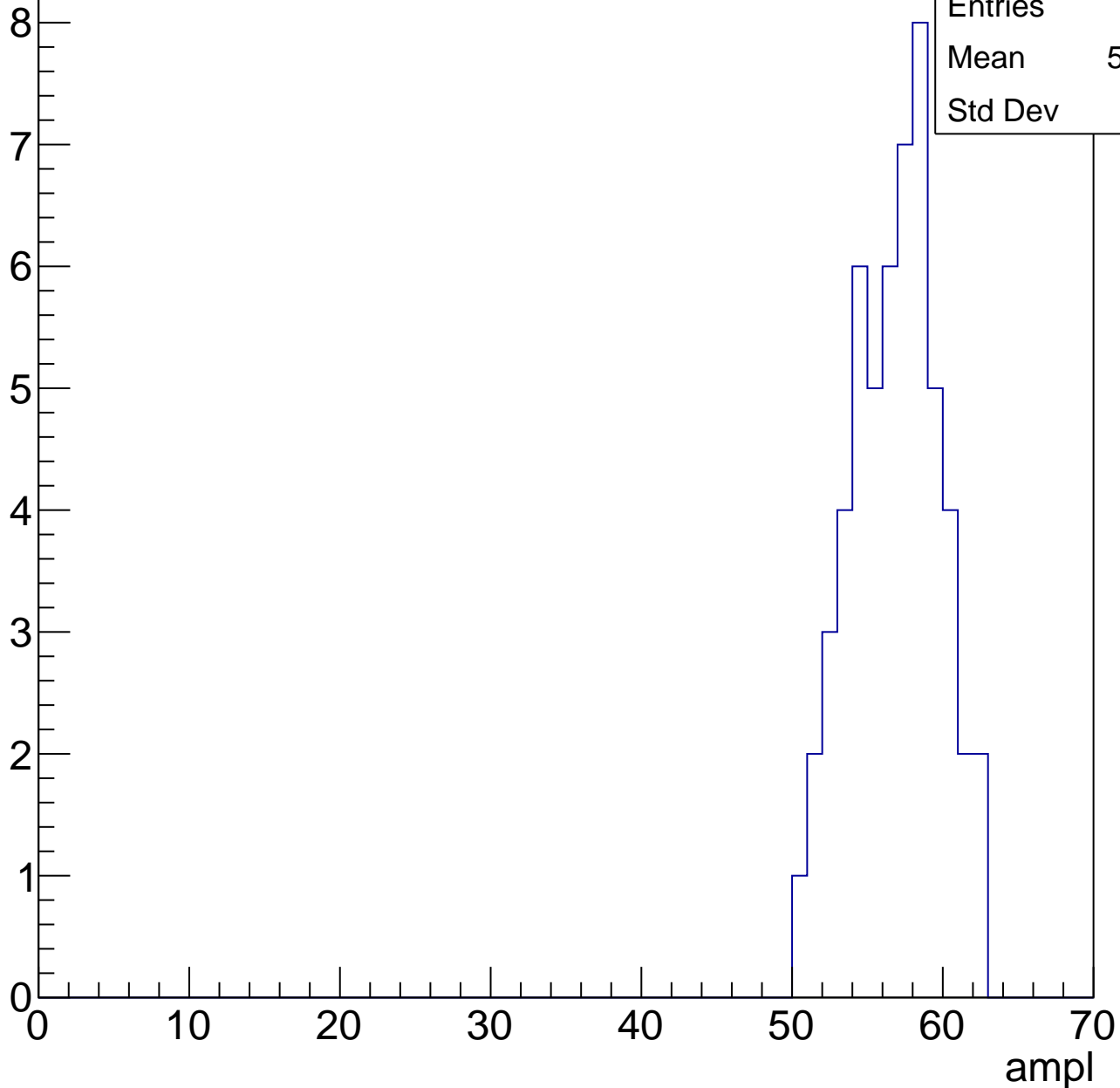
Entries	77
Mean	50.34
Std Dev	3.726



# B0L000S, U7-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

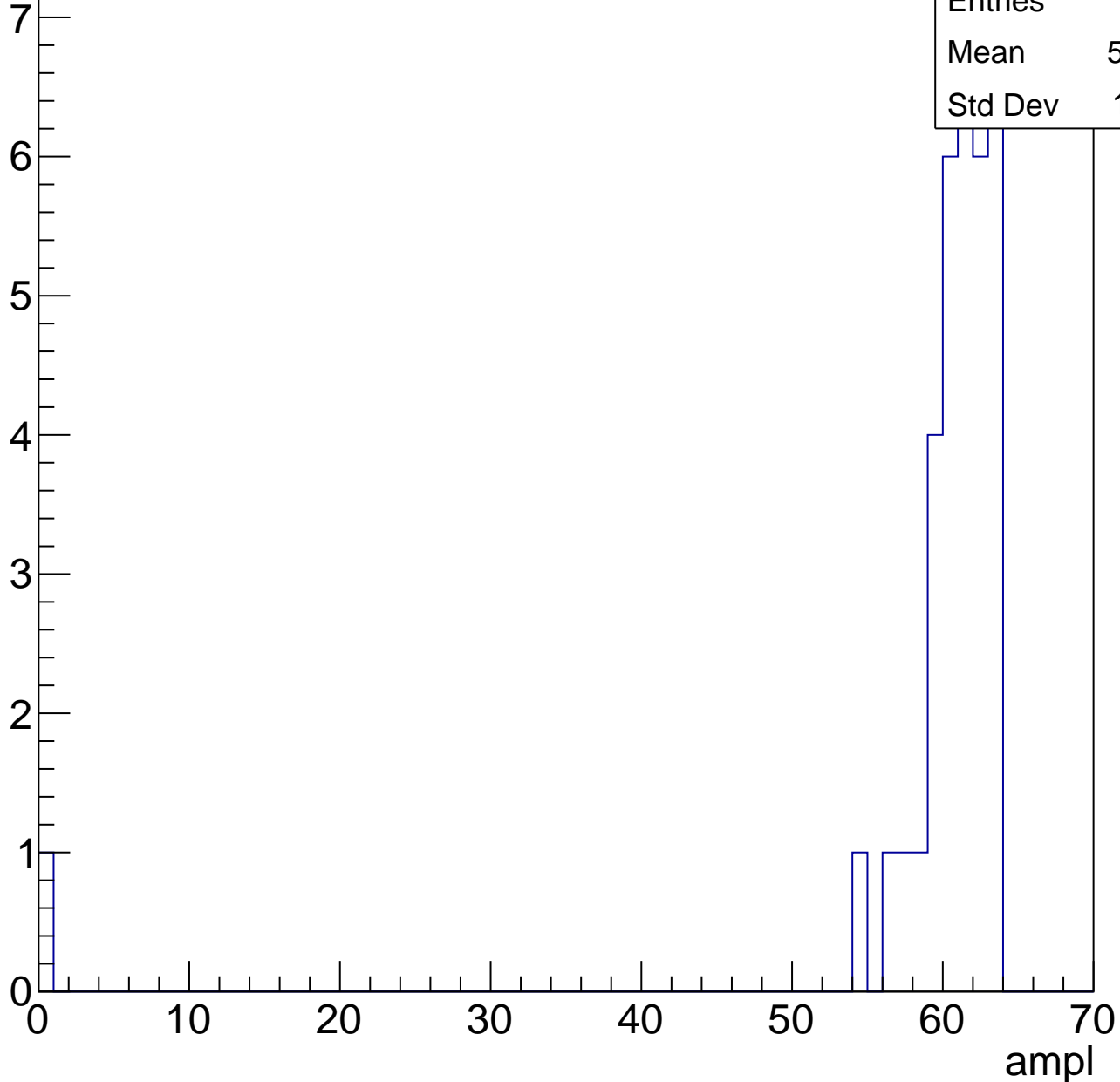
Entry



# B0L000S, U7-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

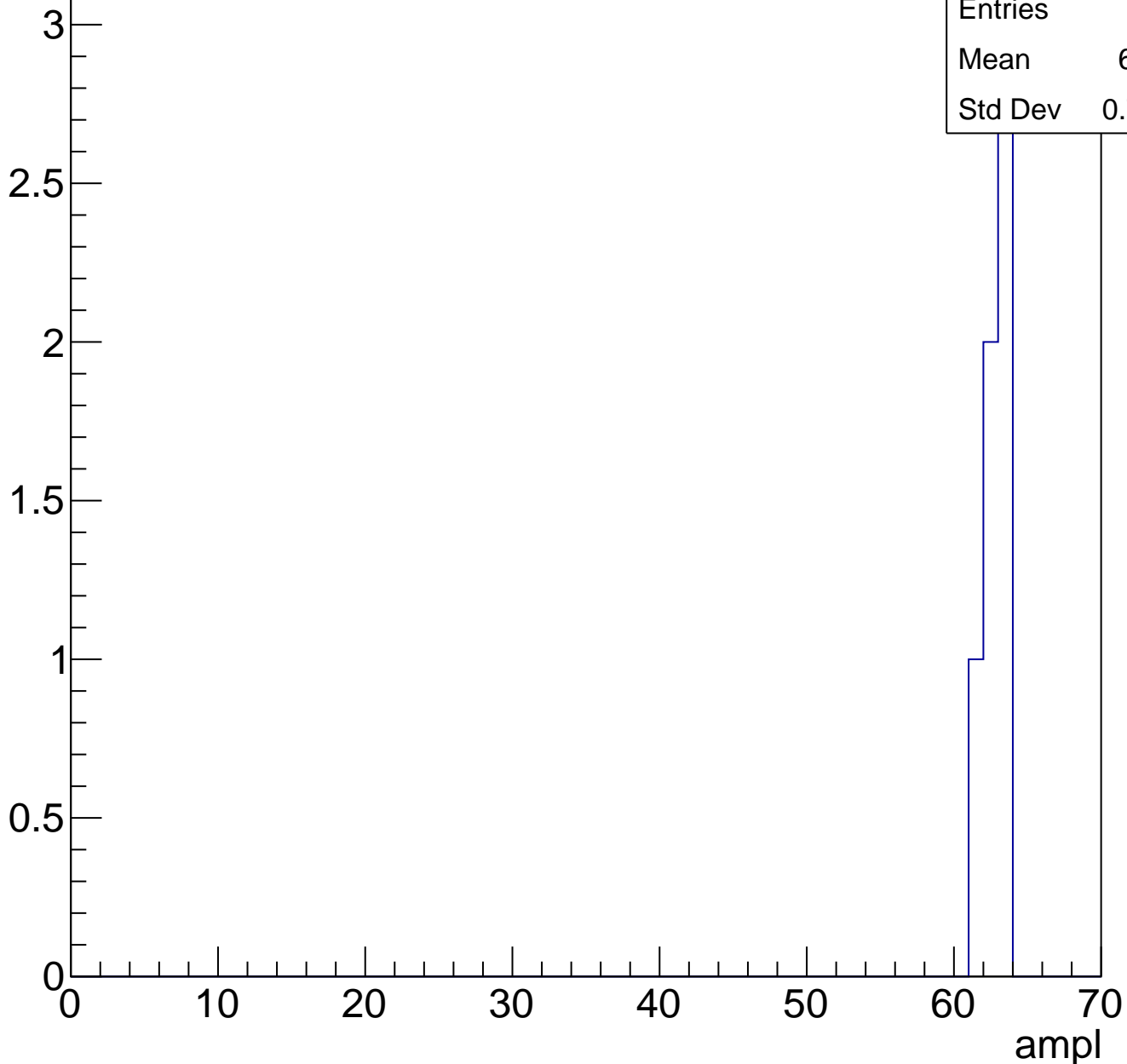
Entry



# B0L000S, U7-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



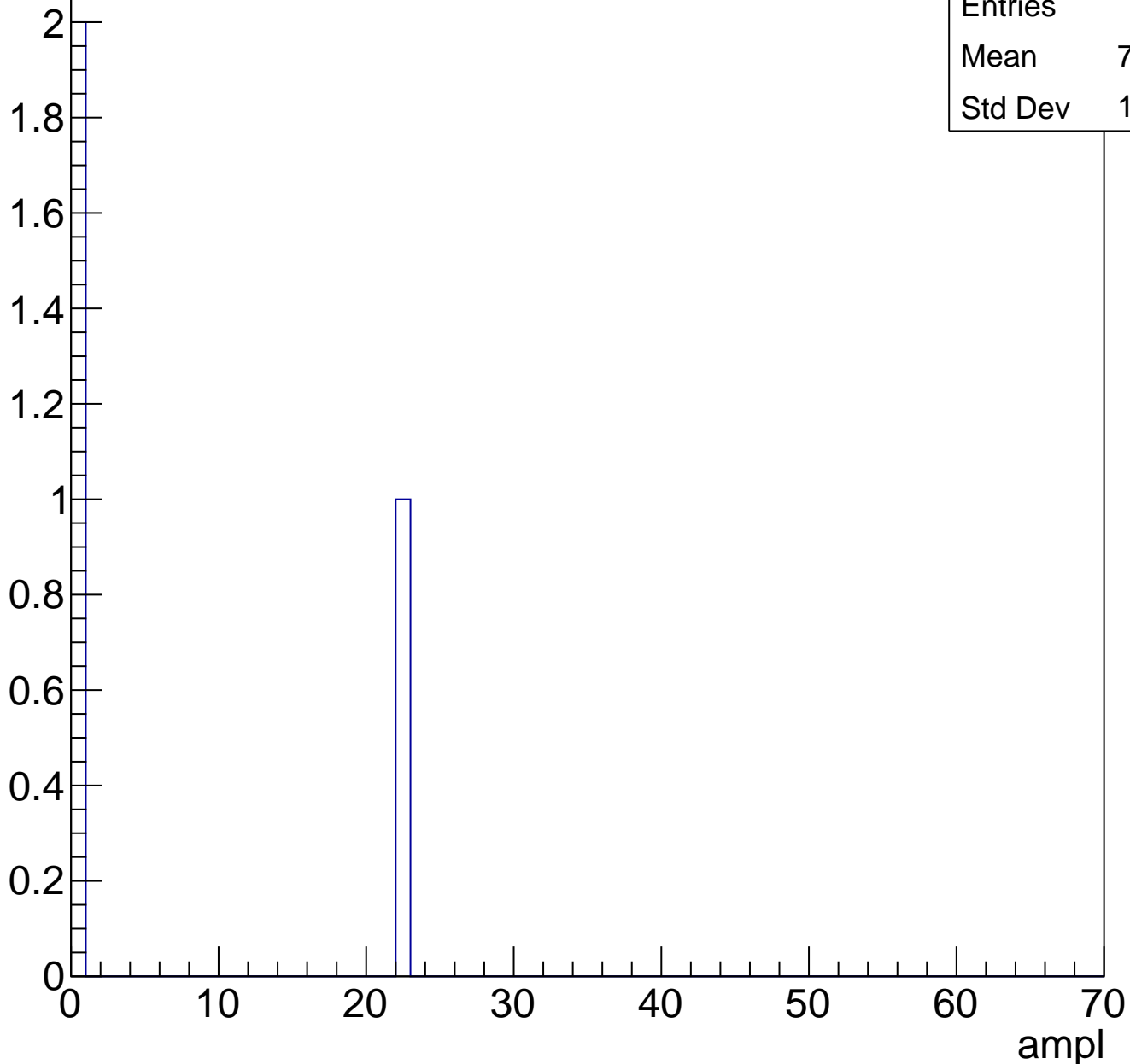
Entries	6
Mean	62.33
Std Dev	0.7454



# B0L000S, U7-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	3
Mean	7.333
Std Dev	10.37

# B0L000S, U7-ch106, adc0

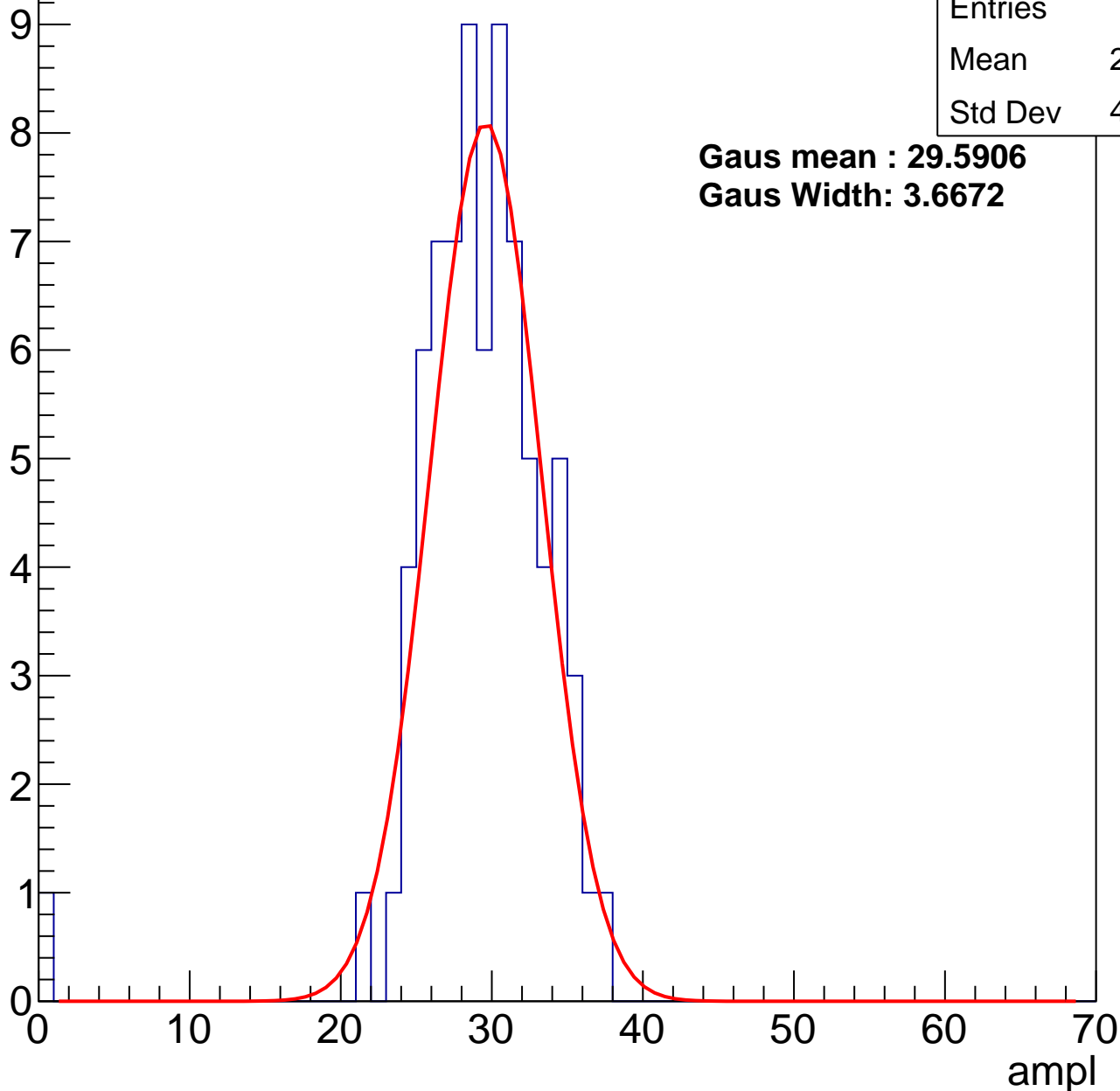
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	77
Mean	28.75
Std Dev	4.732

**Gaus mean : 29.5906**

**Gaus Width: 3.6672**



# B0L000S, U7-ch106, adc1

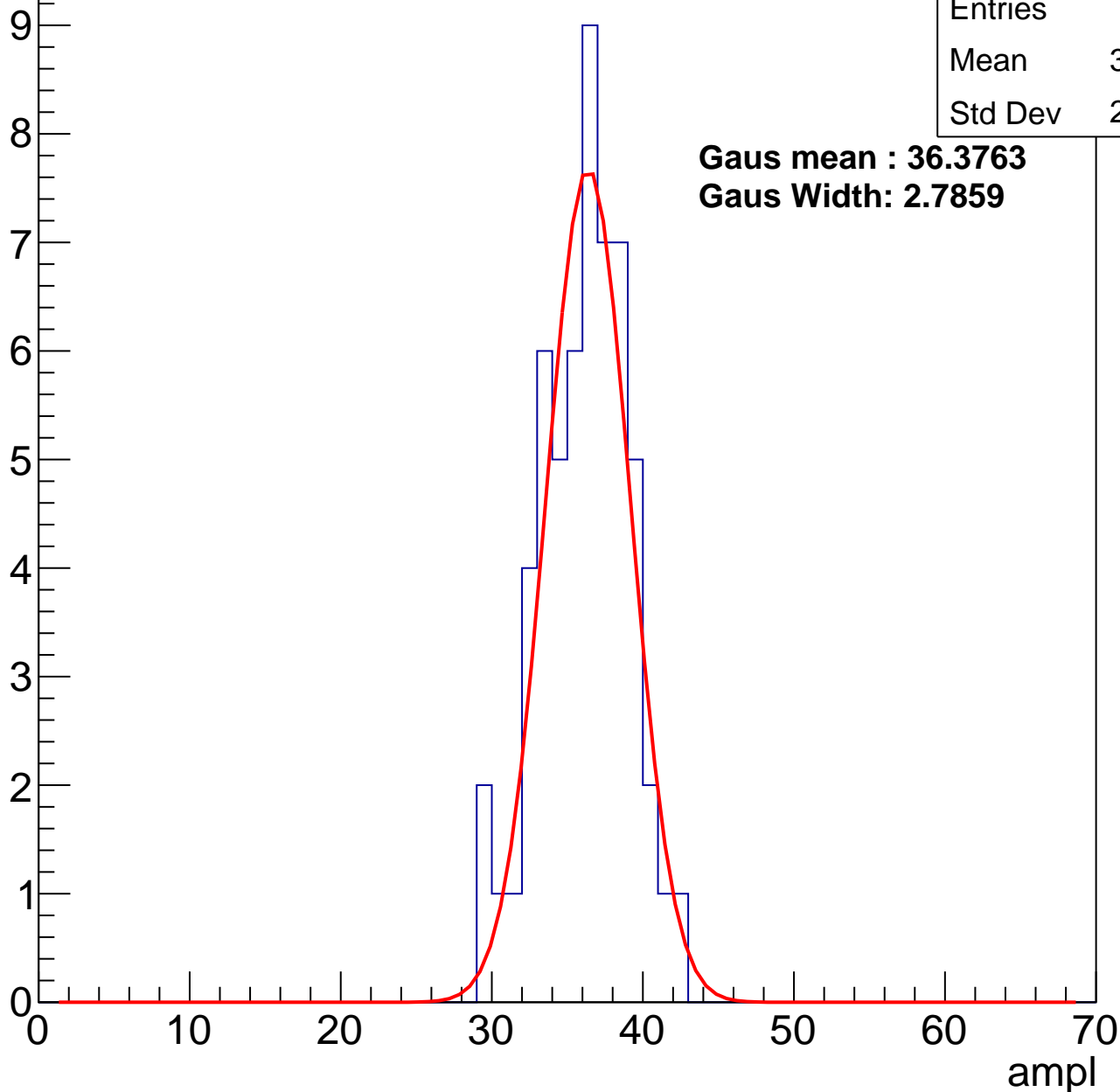
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	57
Mean	35.65
Std Dev	2.868

**Gaus mean : 36.3763**

**Gaus Width: 2.7859**



# B0L000S, U7-ch106, adc2

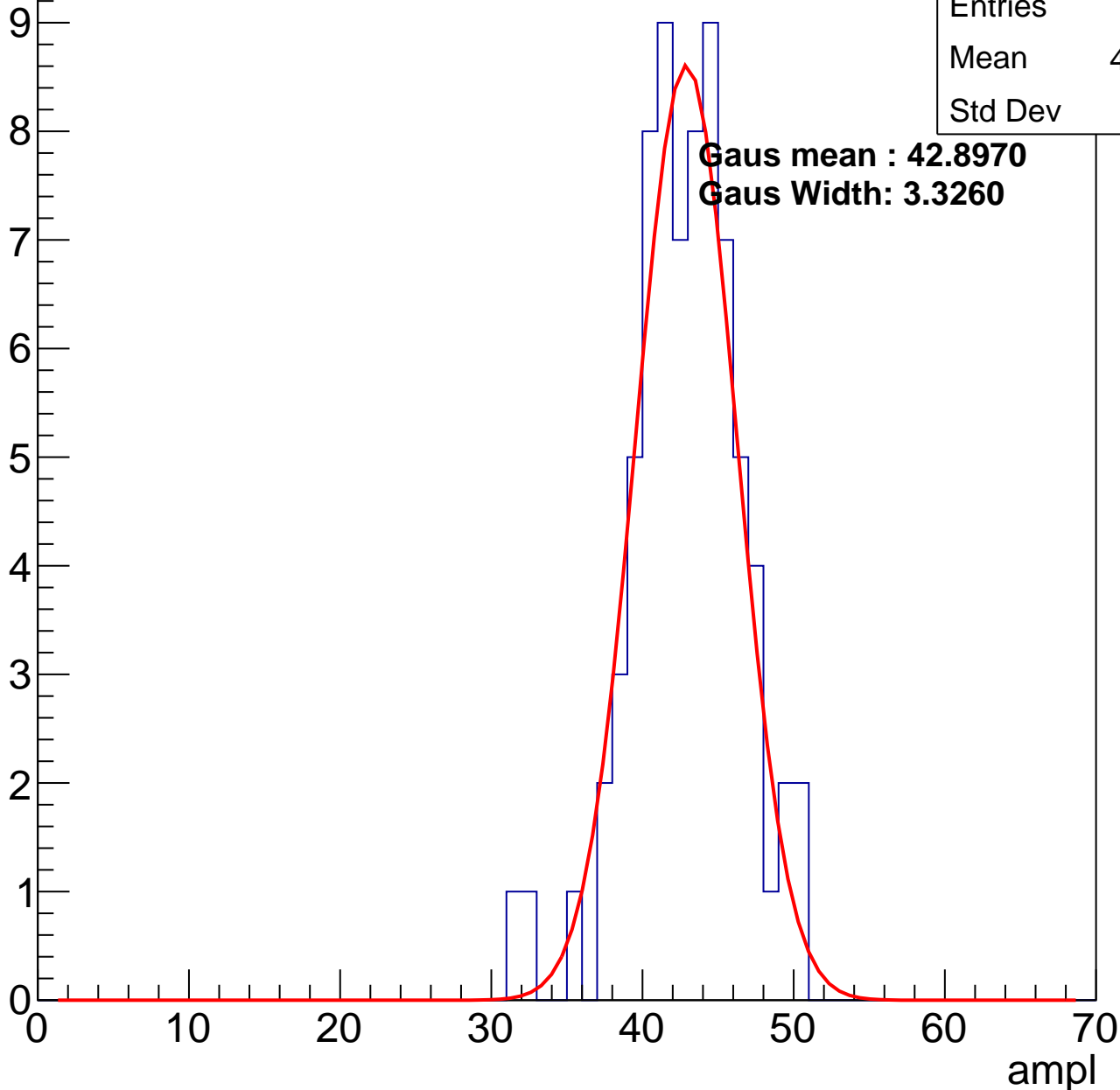
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	75
Mean	42.44
Std Dev	3.63

**Gaus mean : 42.8970**

**Gaus Width: 3.3260**

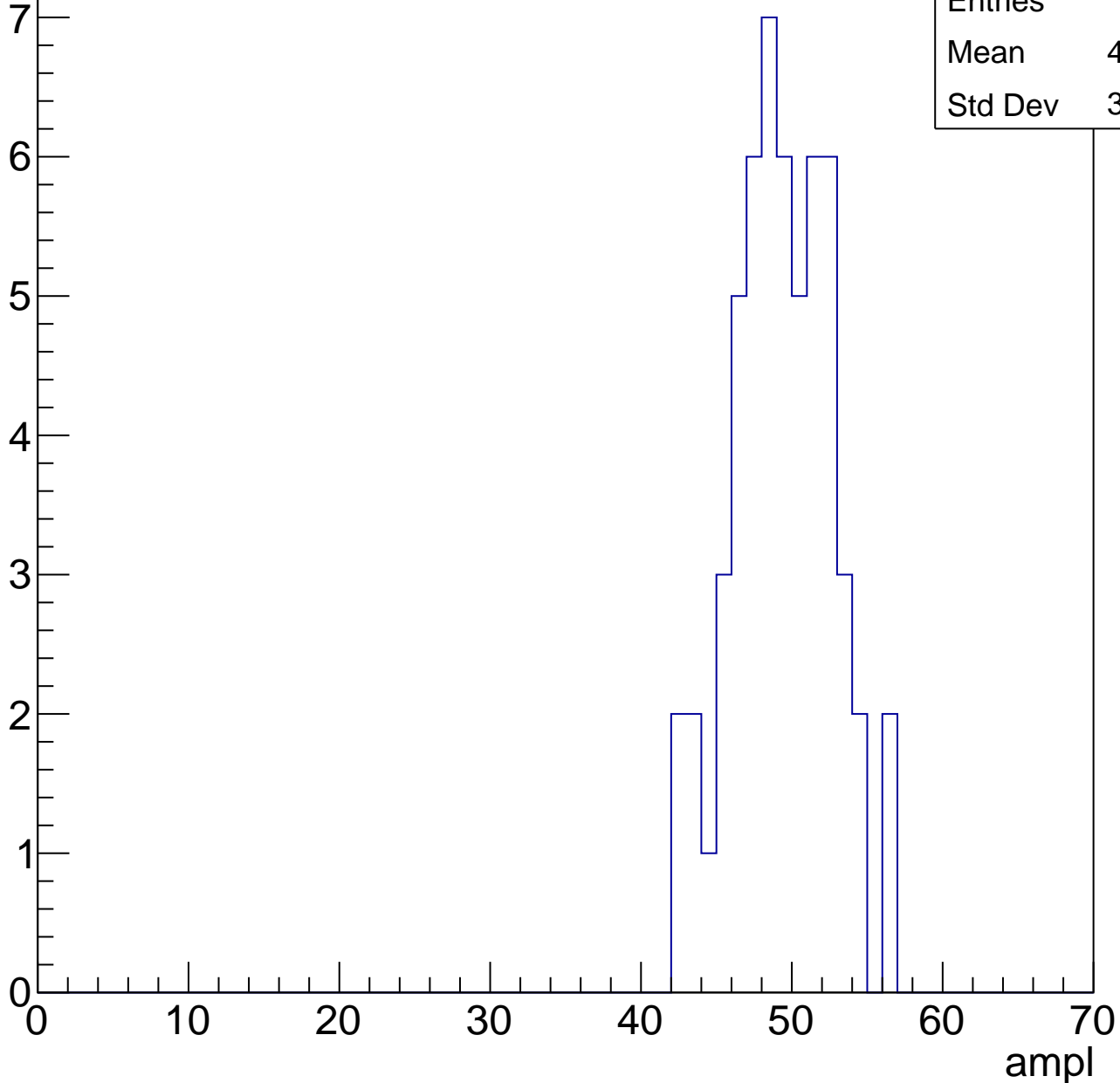


# B0L000S, U7-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

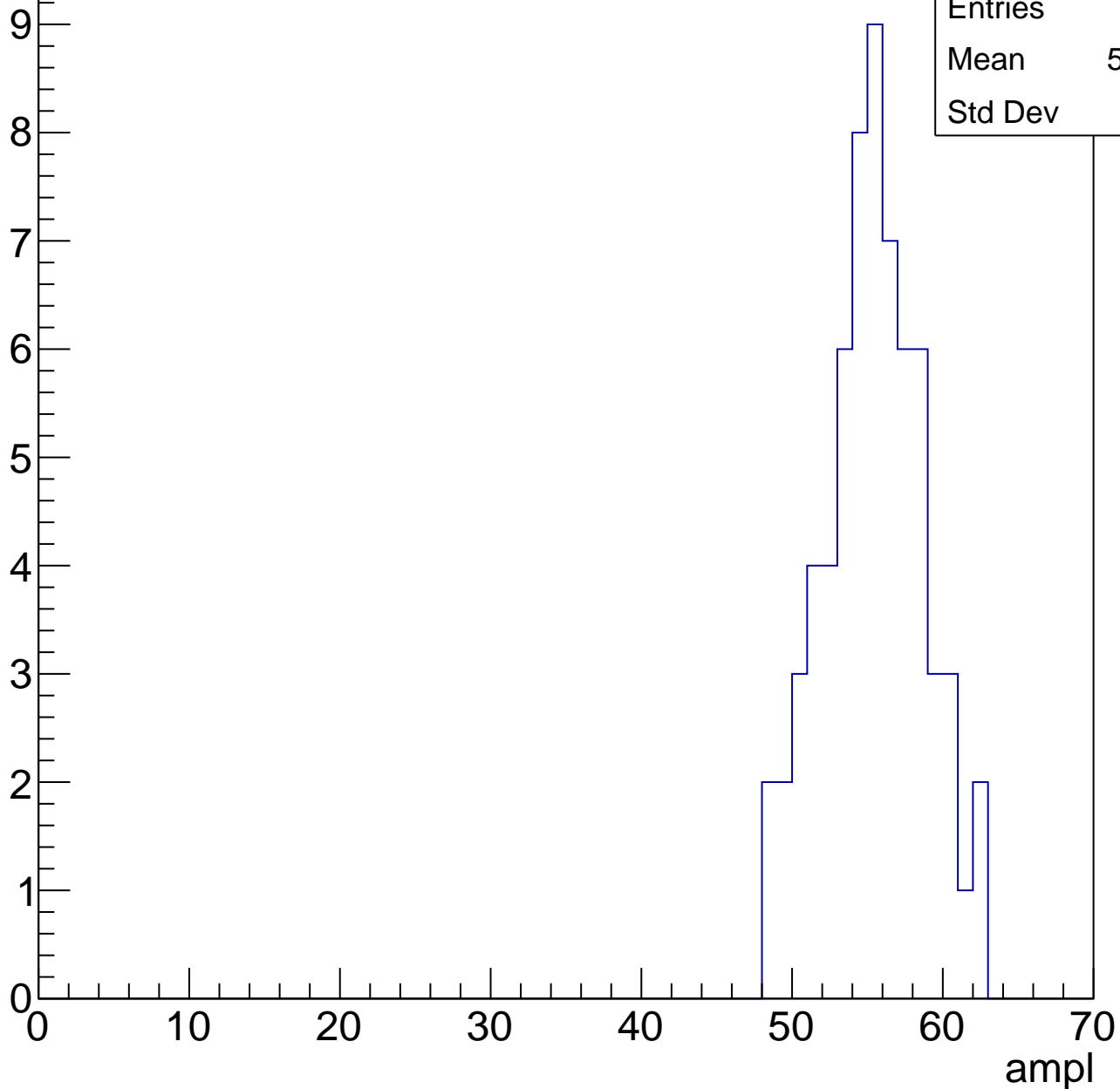
Entries	56
Mean	48.89
Std Dev	3.266



# B0L000S, U7-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

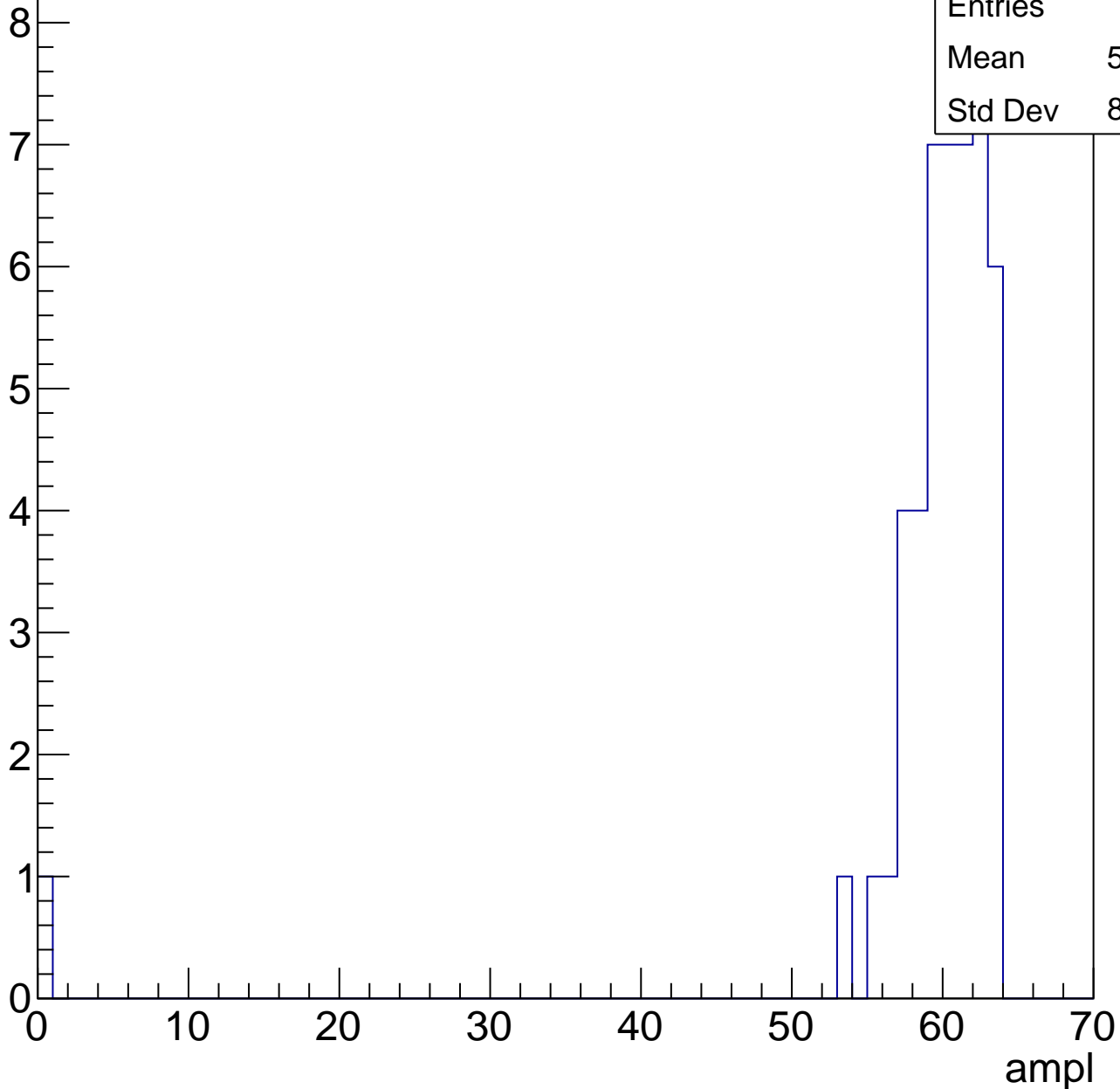


# B0L000S, U7-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

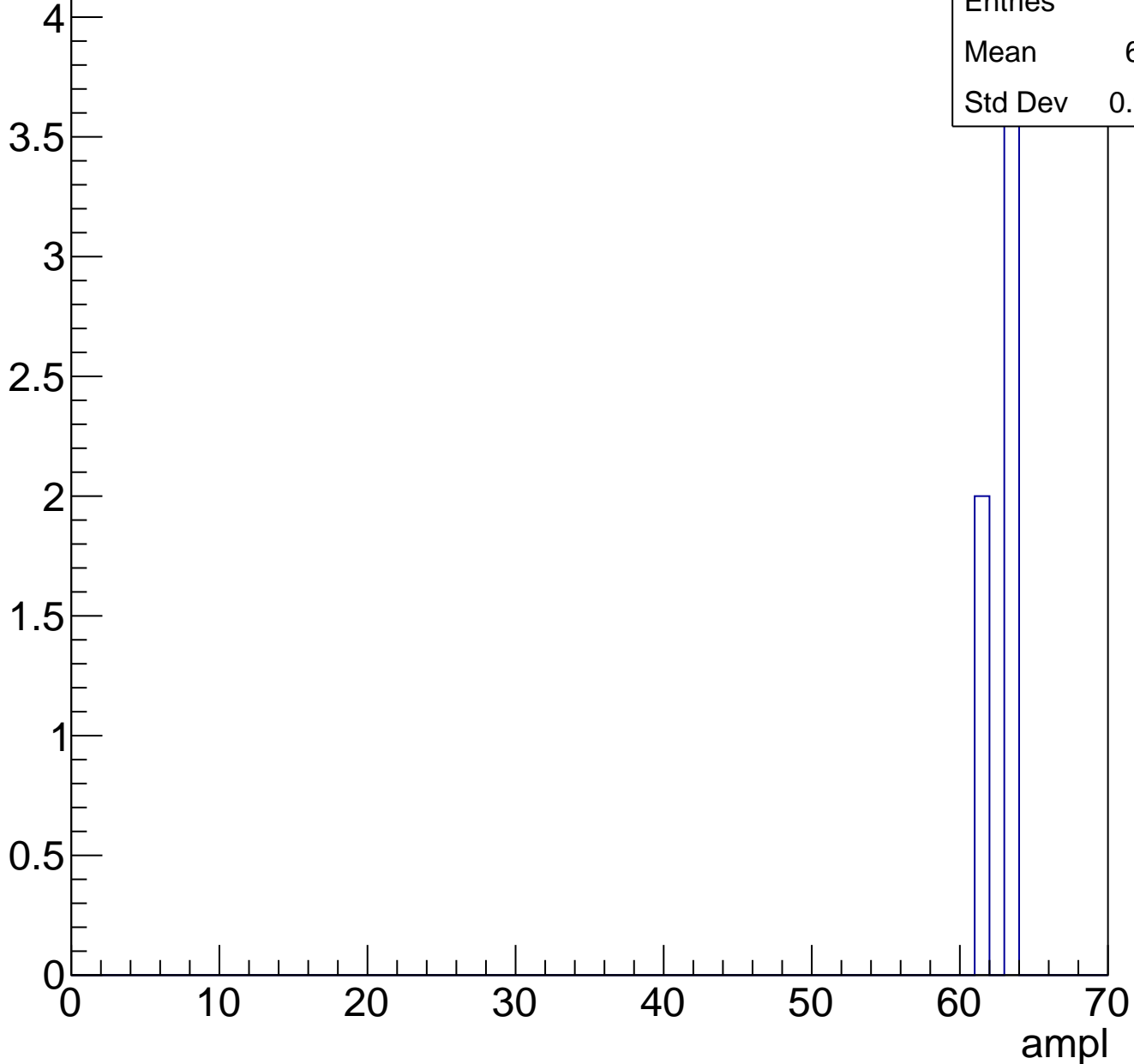
Entries	47
Mean	58.68
Std Dev	8.945



# B0L000S, U7-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L000S, U7-ch107, adc0

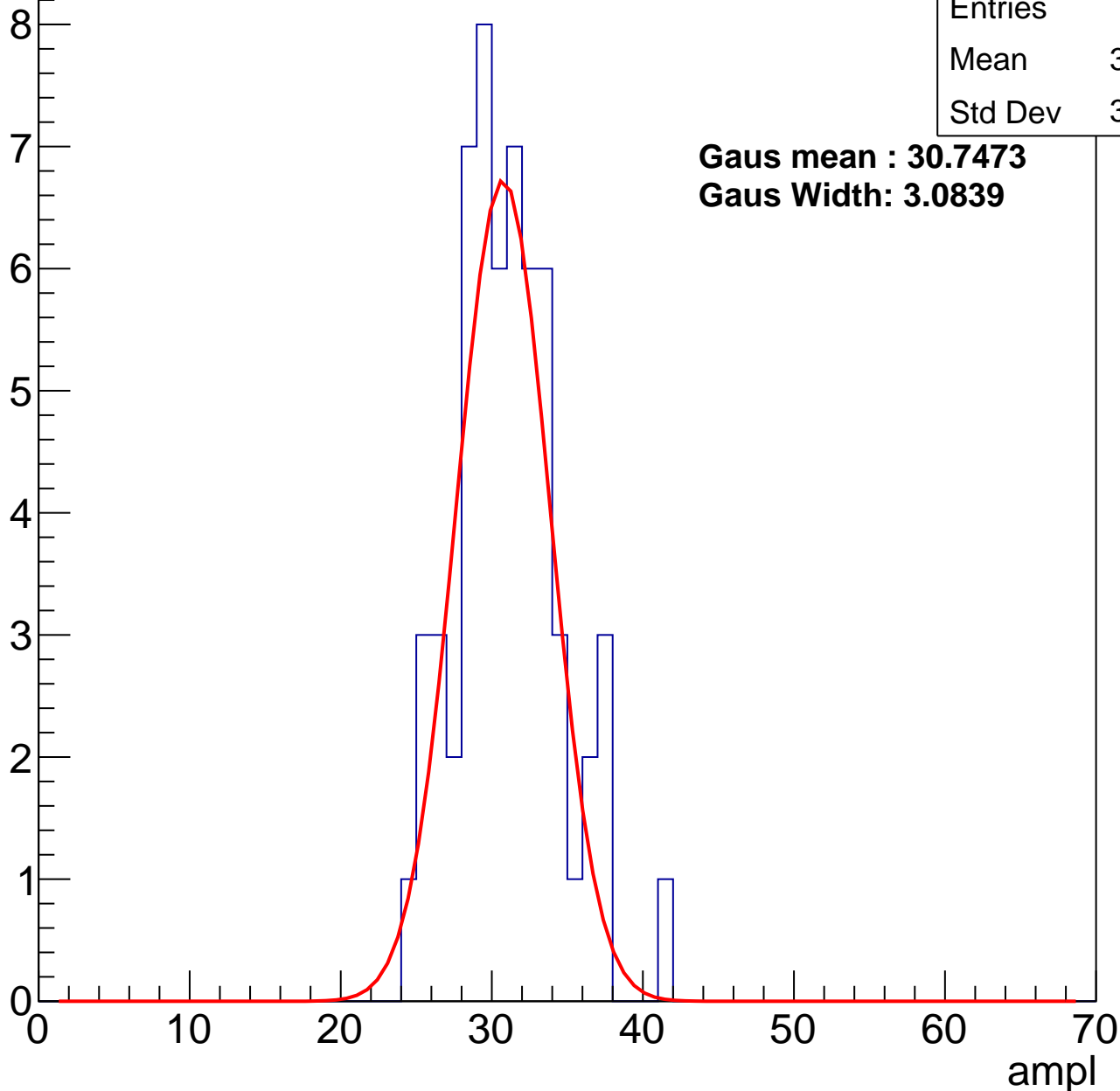
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	59
Mean	30.63
Std Dev	3.414

**Gaus mean : 30.7473**

**Gaus Width: 3.0839**



# B0L000S, U7-ch107, adc1

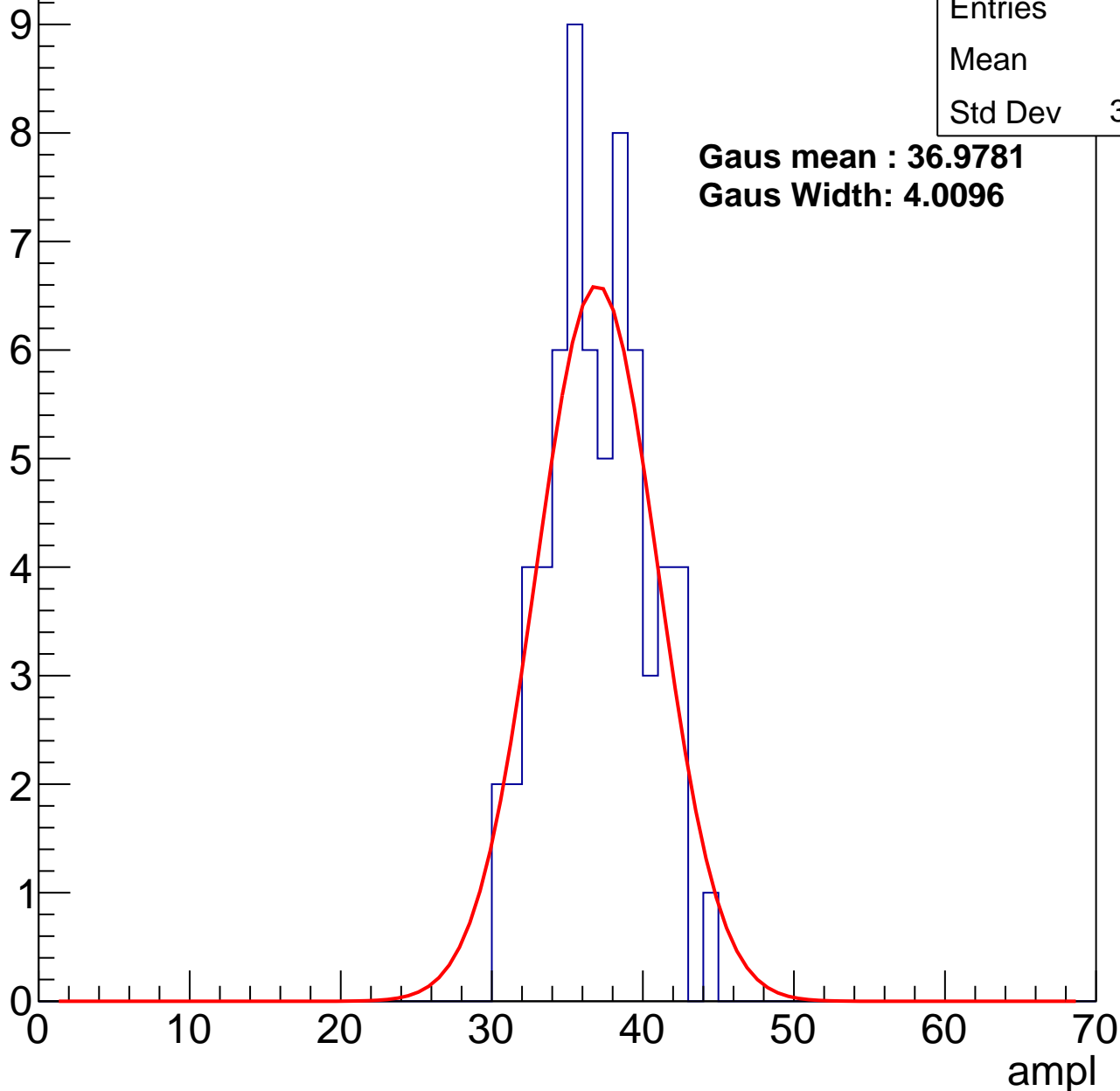
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	64
Mean	36.5
Std Dev	3.274

**Gaus mean : 36.9781**

**Gaus Width: 4.0096**



# B0L000S, U7-ch107, adc2

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	89
Mean	44.3
Std Dev	4.131

**Gaus mean : 44.6047**

**Gaus Width: 4.6269**

Entry

10

8

6

4

2

0

0

10

20

30

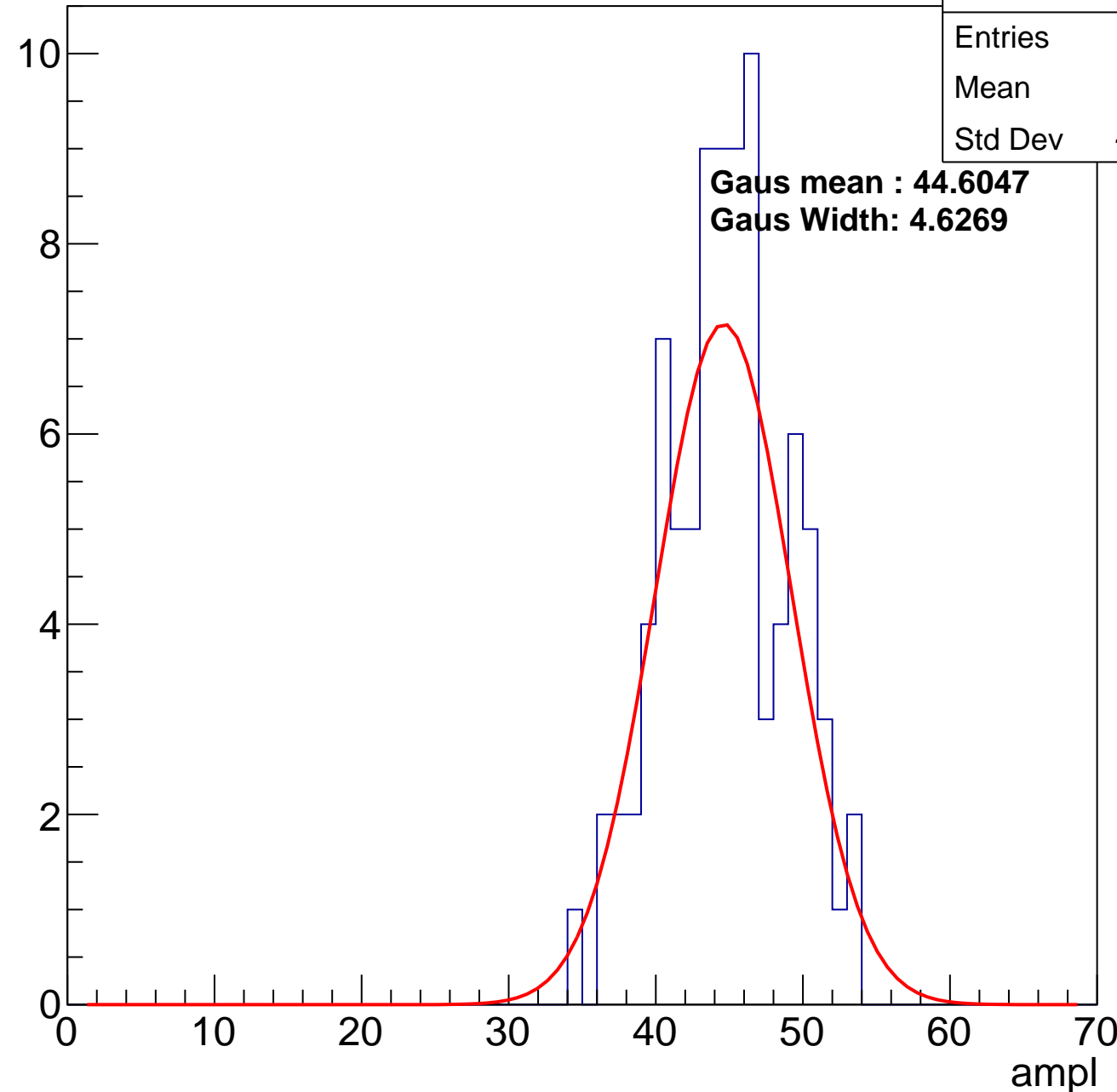
40

50

60

70

ampl

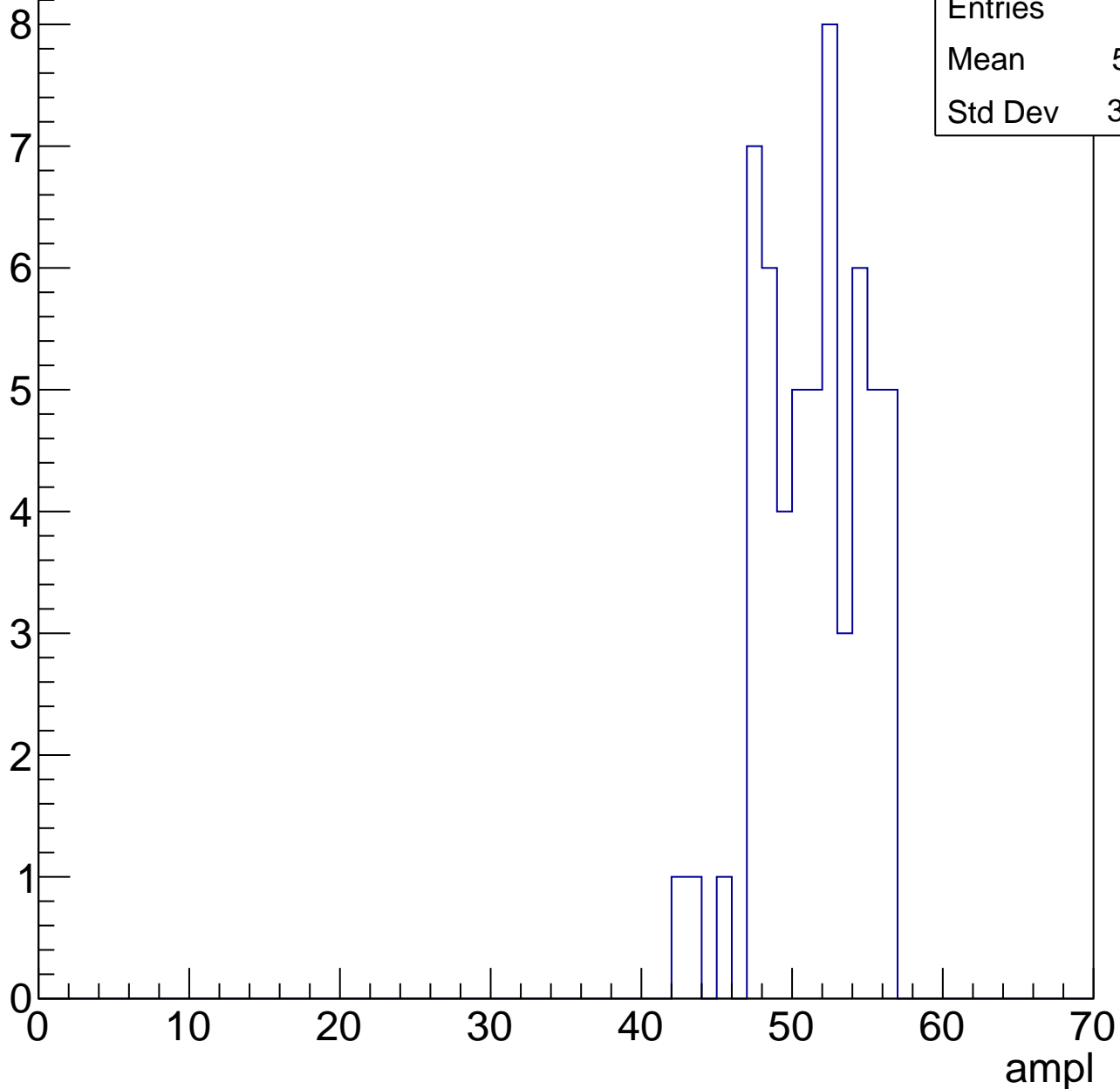


# B0L000S, U7-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	57
Mean	50.91
Std Dev	3.368

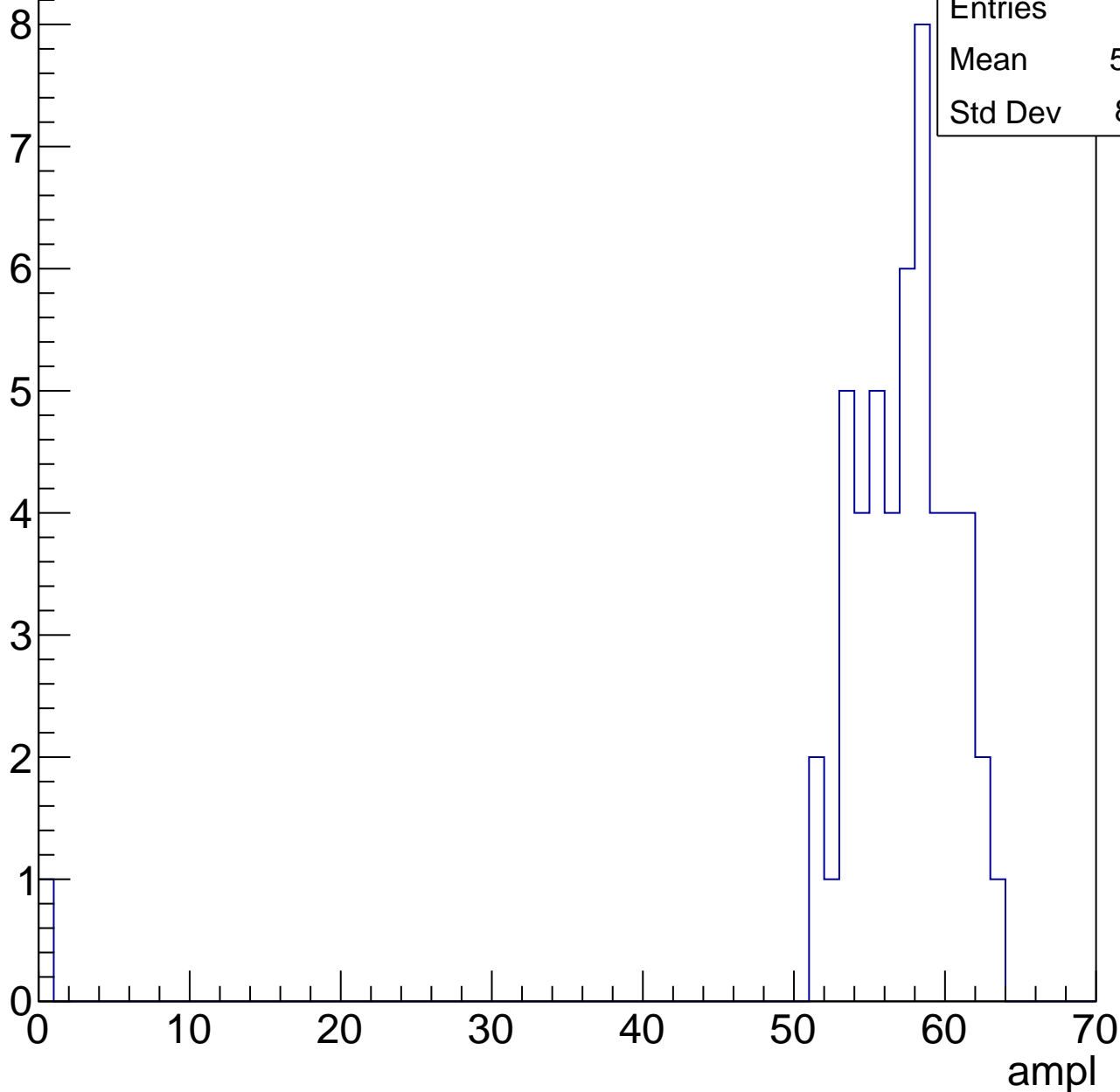


# B0L000S, U7-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	51
Mean	55.82
Std Dev	8.431

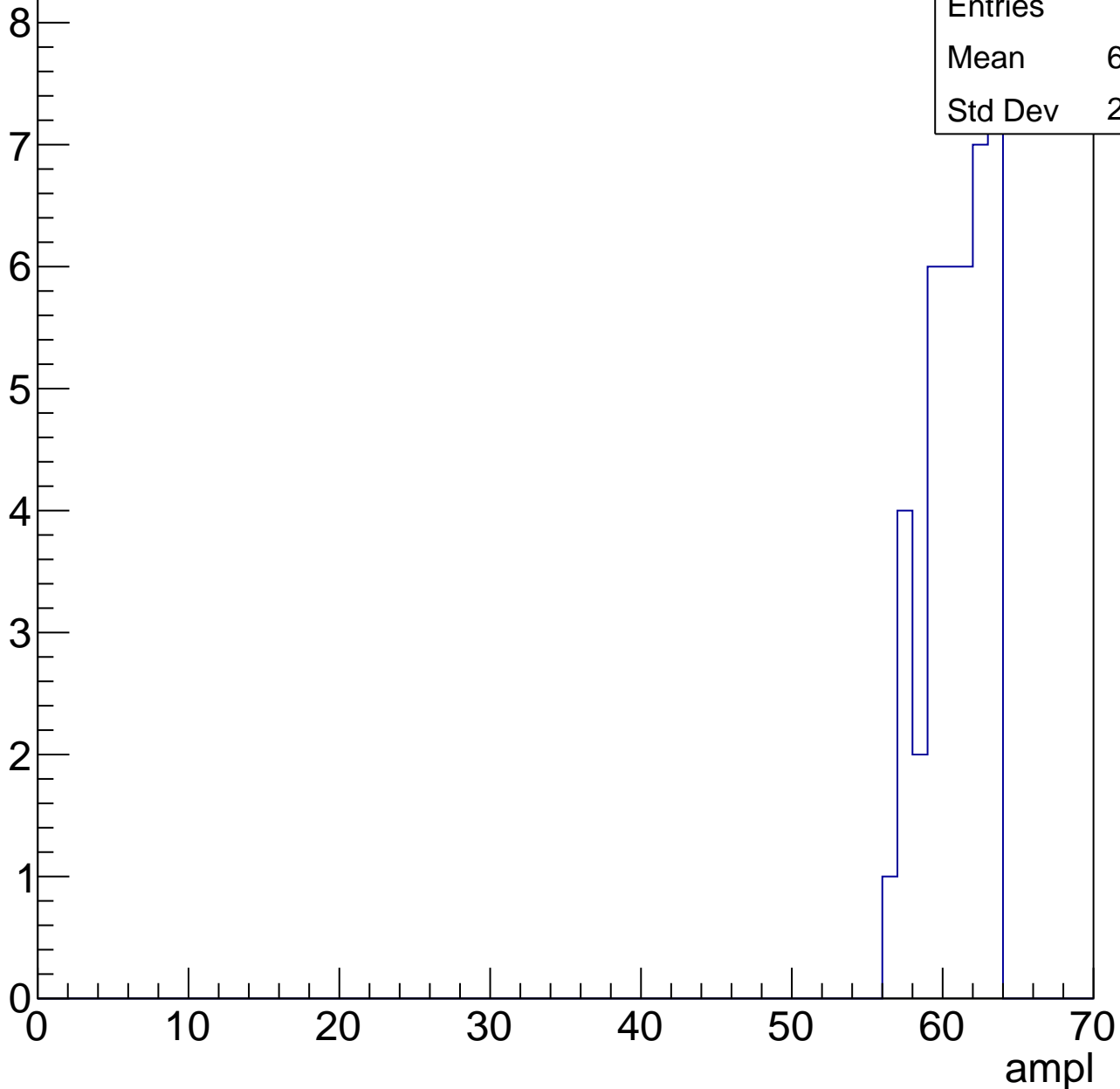


# B0L000S, U7-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	40
Mean	60.45
Std Dev	2.024



# B0L000S, U7-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

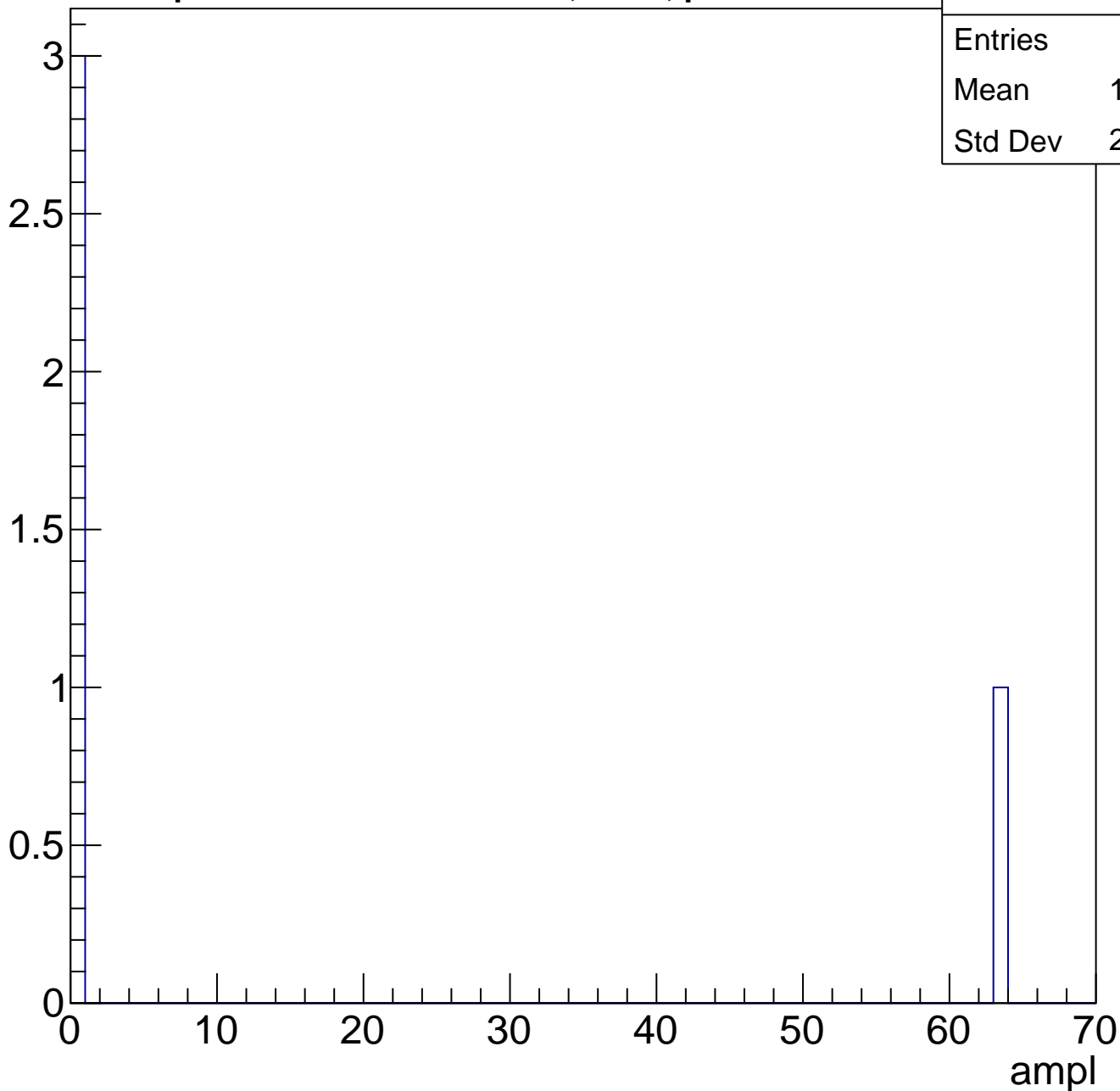




# B0L000S, U7-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch108, adc0

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	70
Mean	30.01
Std Dev	4.767

**Gaus mean : 31.2128**

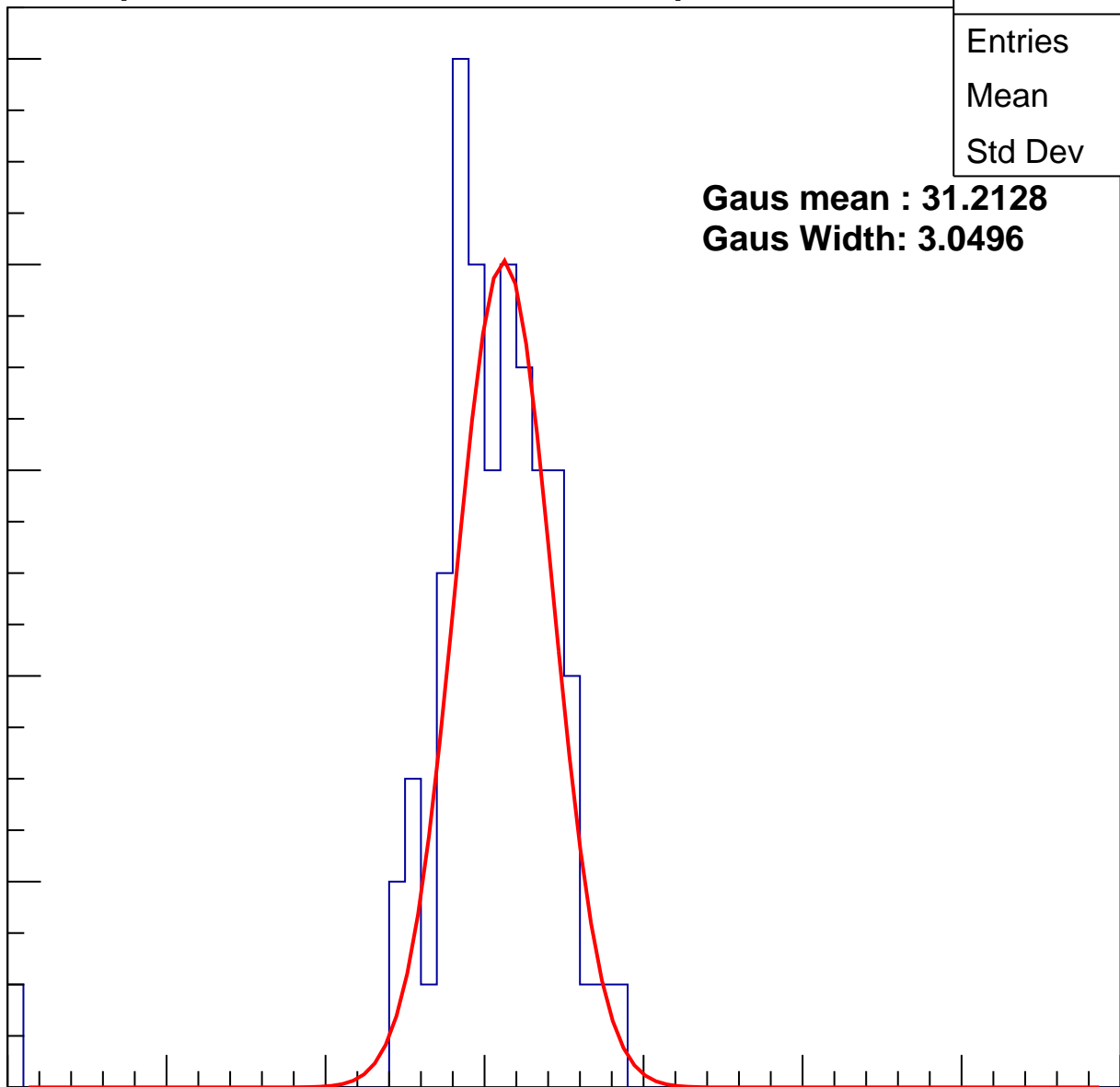
**Gaus Width: 3.0496**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L000S, U7-ch108, adc1

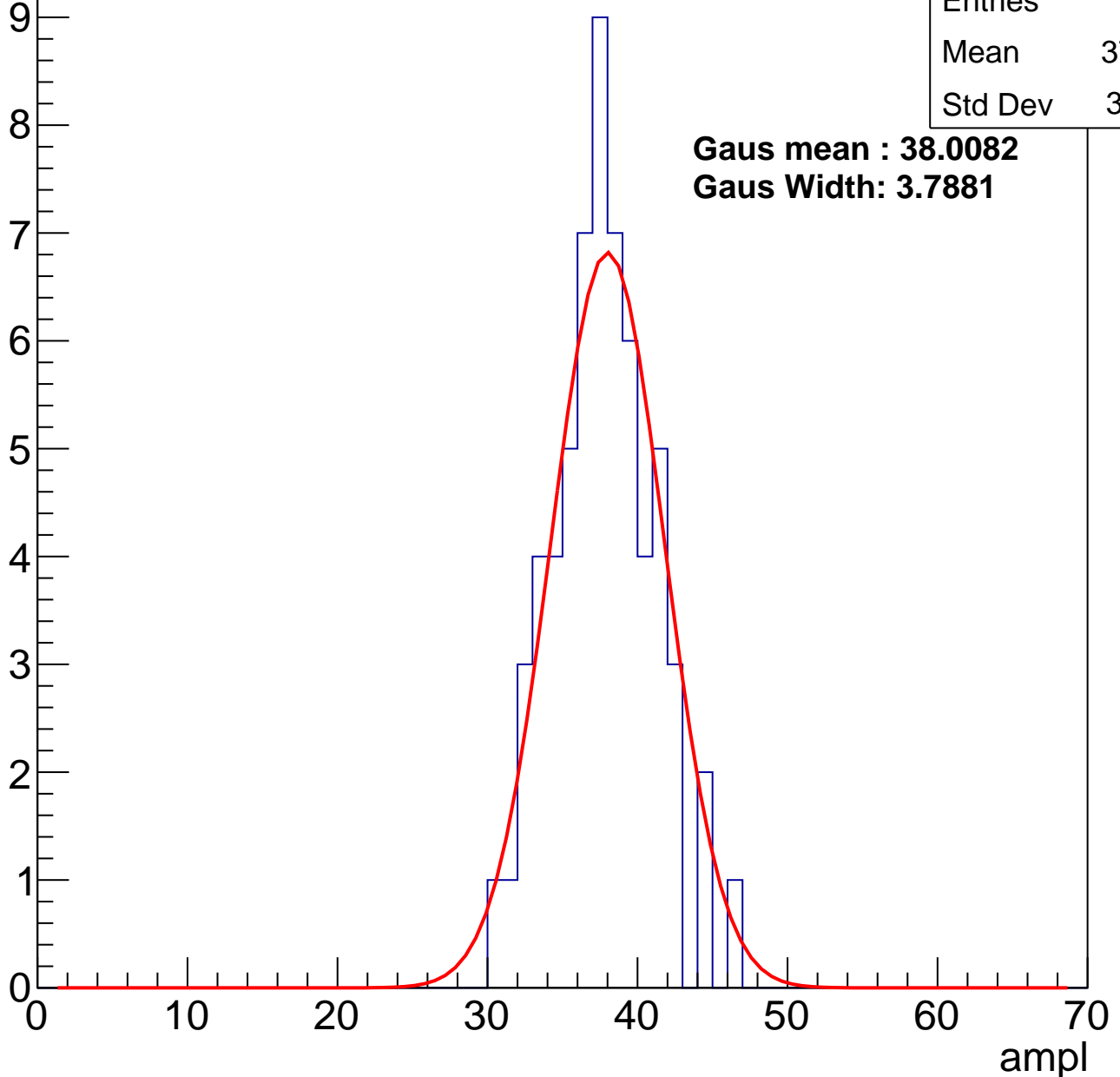
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	62
Mean	37.26
Std Dev	3.321

**Gaus mean : 38.0082**

**Gaus Width: 3.7881**



# B0L000S, U7-ch108, adc2

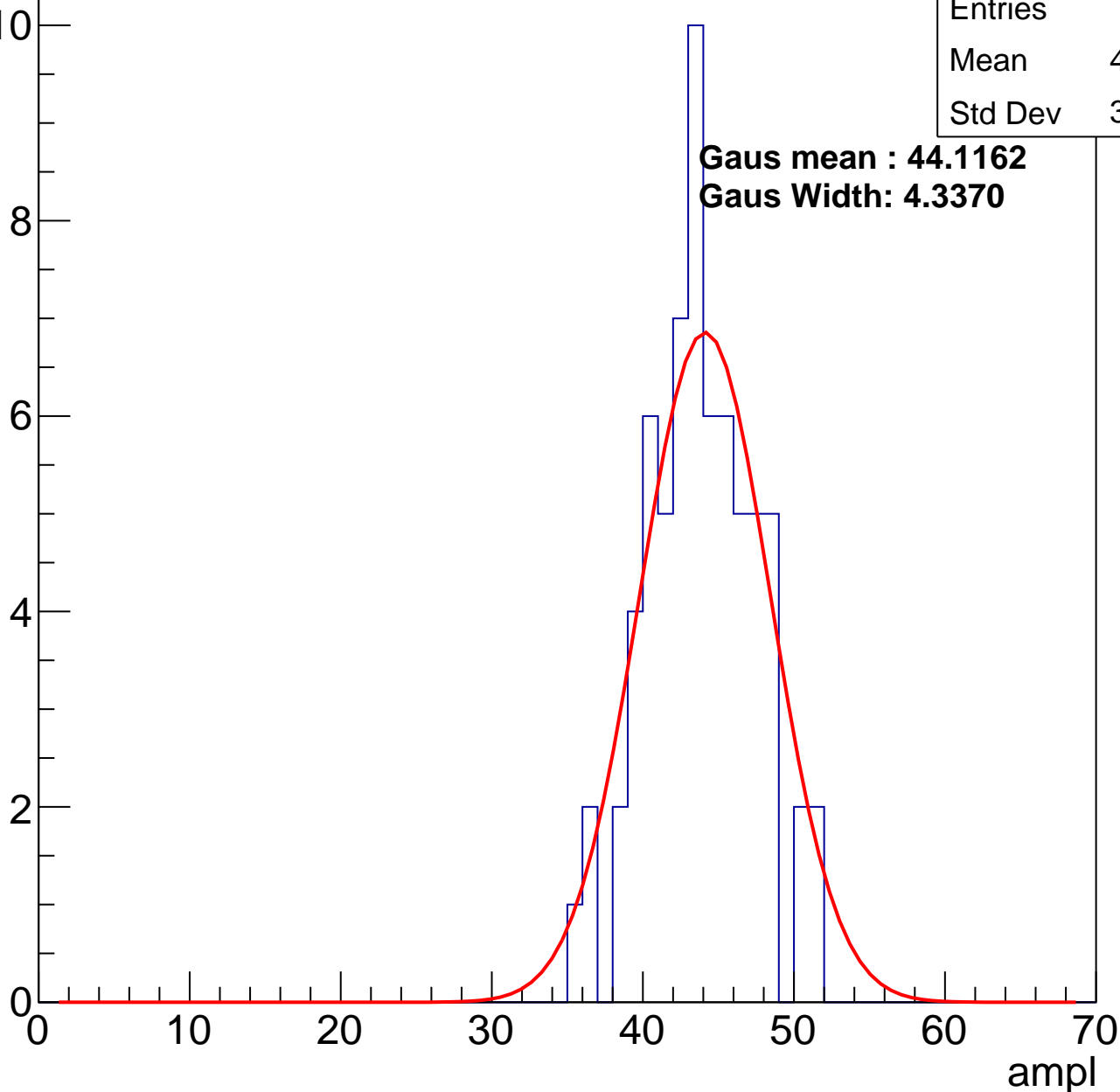
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	68
Mean	43.37
Std Dev	3.543

**Gaus mean : 44.1162**

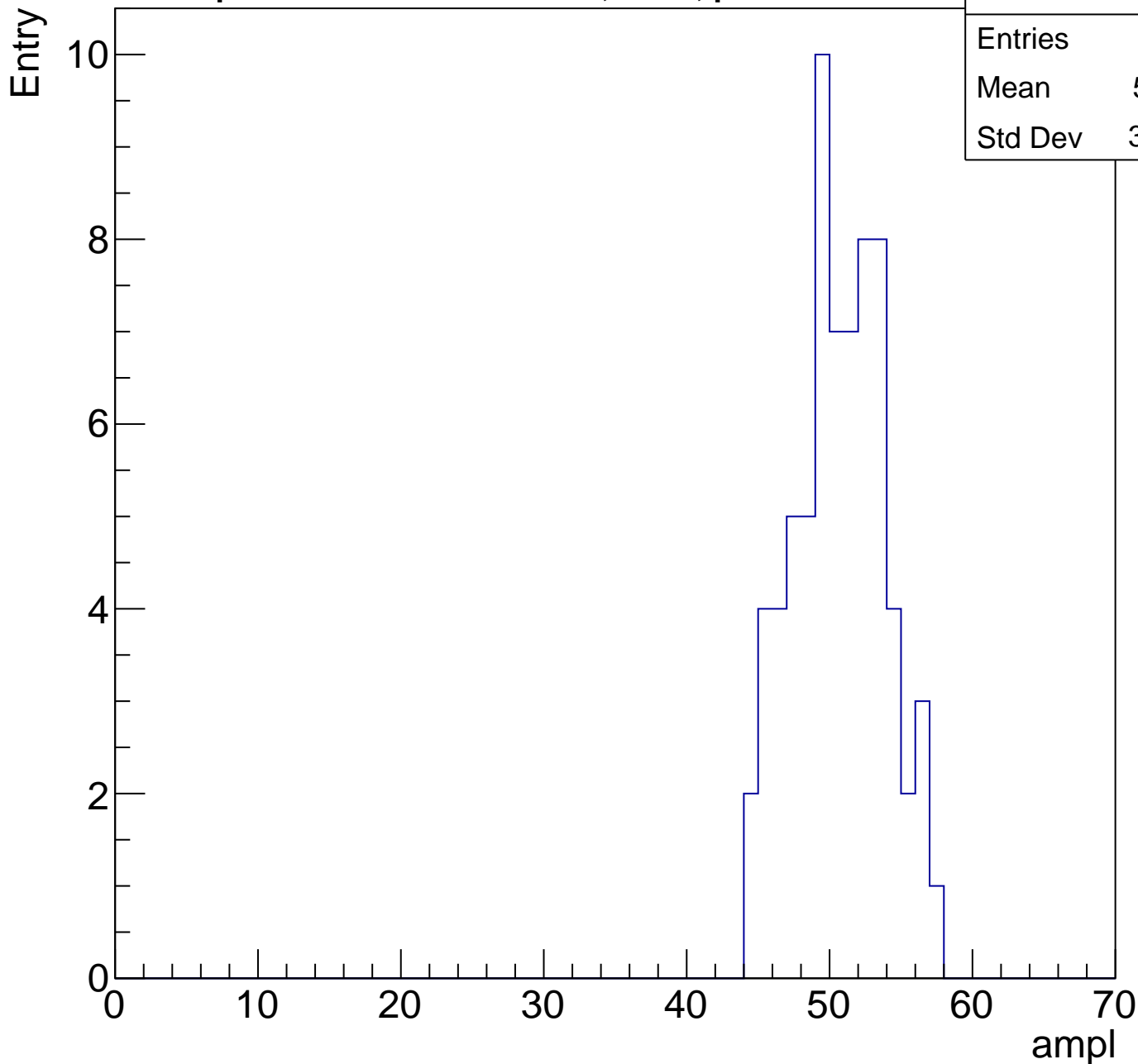
**Gaus Width: 4.3370**



# B0L000S, U7-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	70
Mean	50.21
Std Dev	3.139

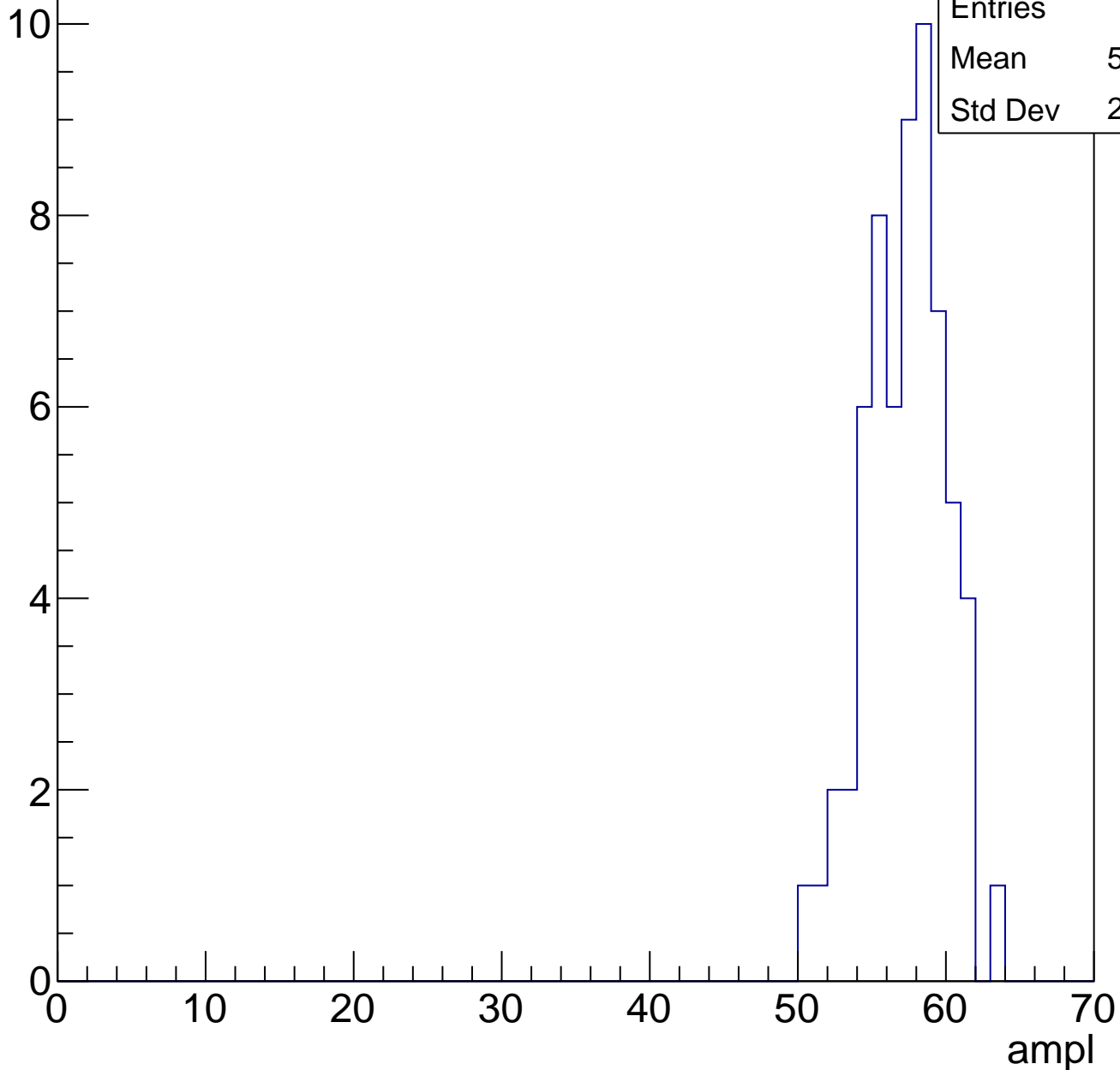


# B0L000S, U7-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	62
Mean	56.84
Std Dev	2.665

Entry

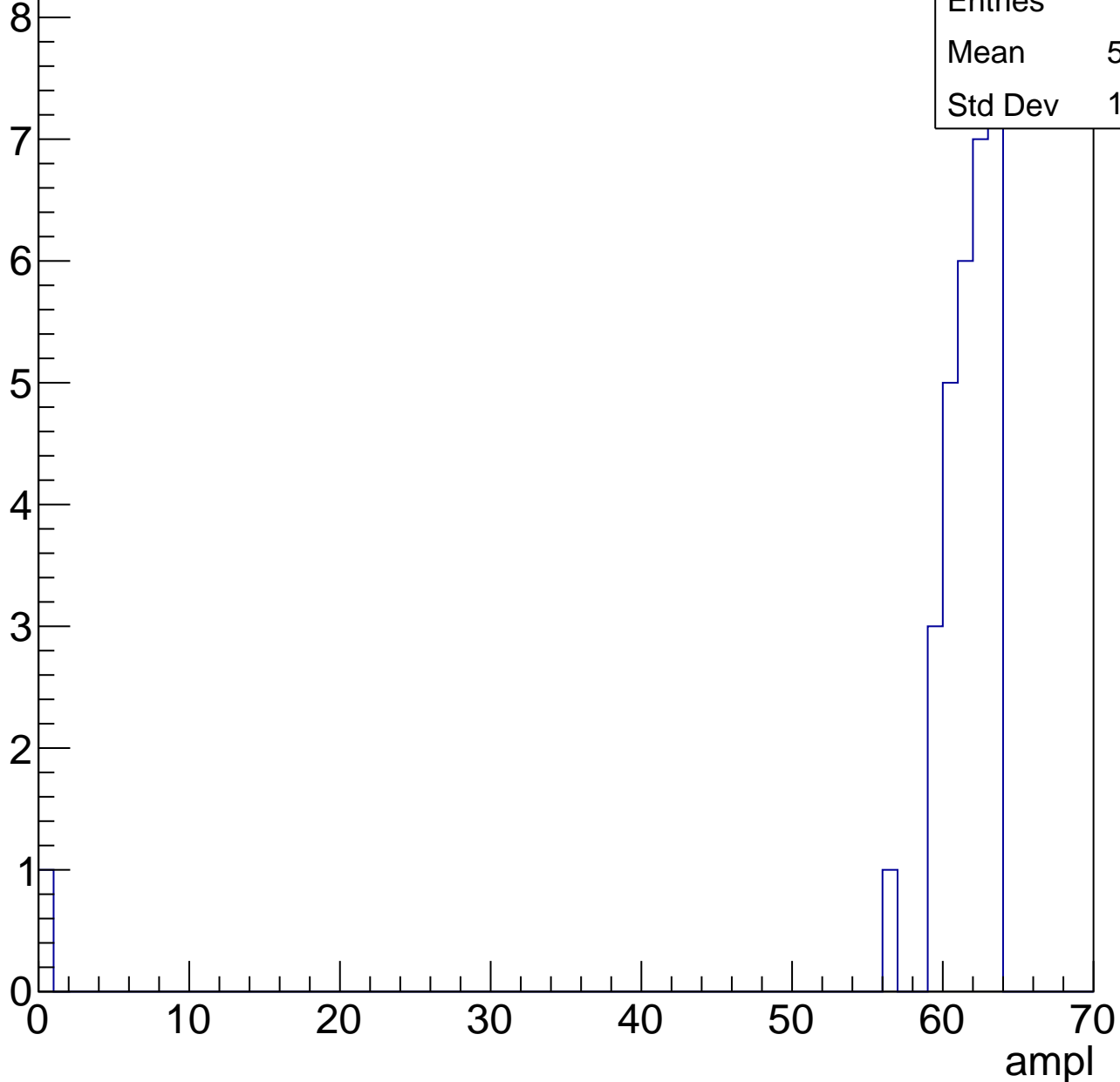


# B0L000S, U7-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	31
Mean	59.26
Std Dev	10.94



# B0L000S, U7-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L000S, U7-ch109, adc0

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	84
Mean	29.95
Std Dev	5.861

**Gaus mean : 31.4604**

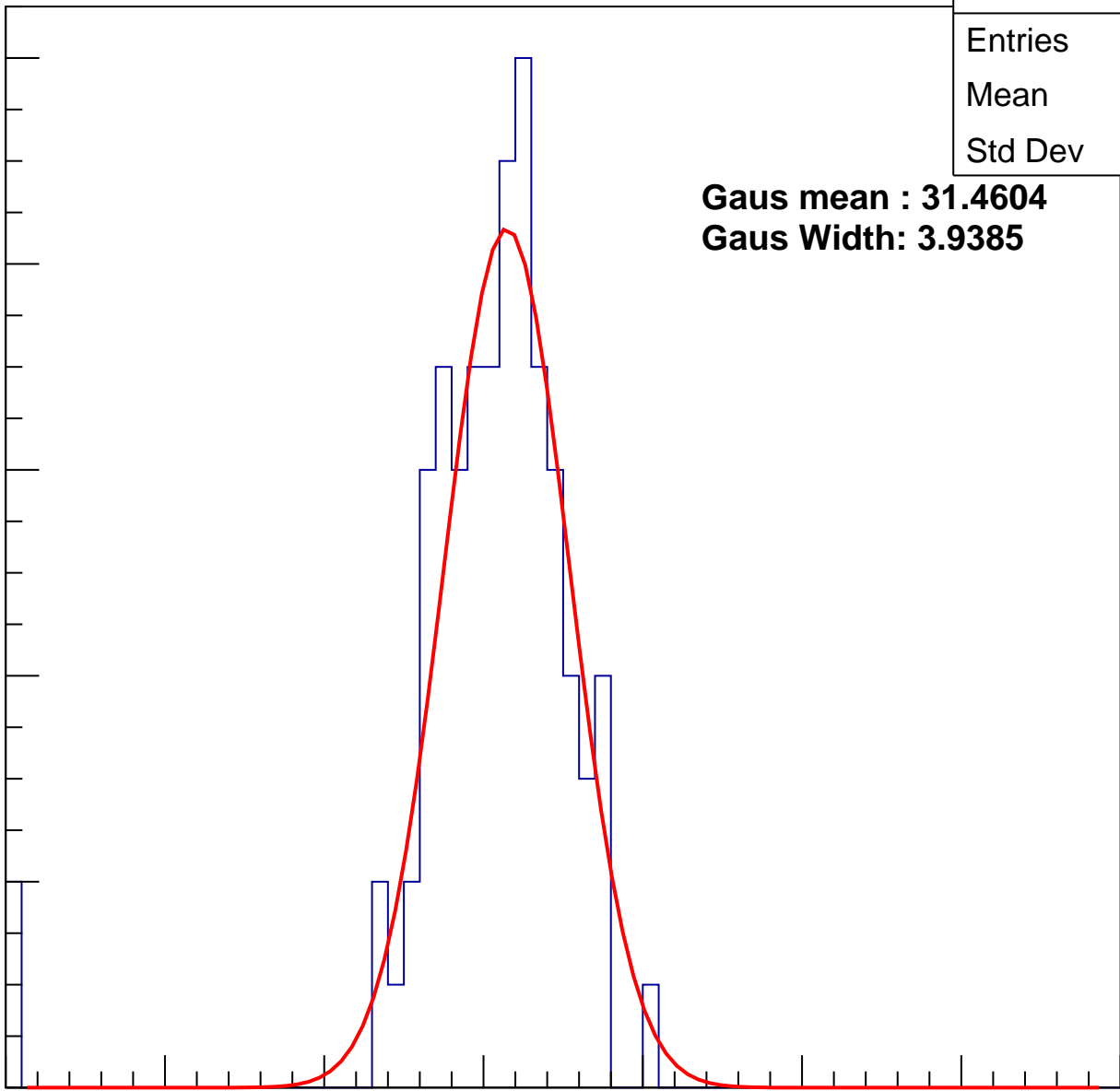
**Gaus Width: 3.9385**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L000S, U7-ch109, adc1

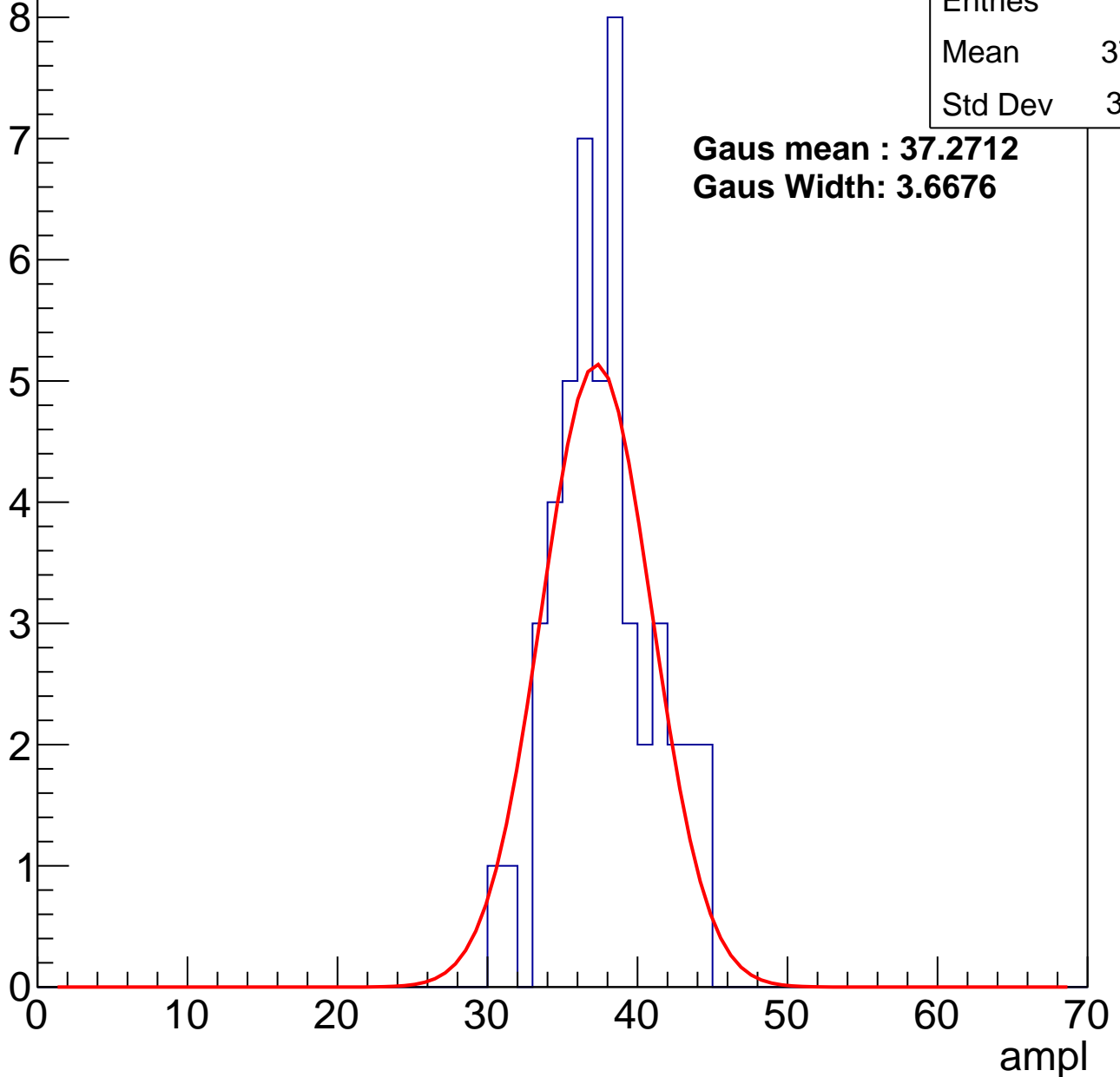
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	48
Mean	37.29
Std Dev	3.221

**Gaus mean : 37.2712**

**Gaus Width: 3.6676**



# B0L000S, U7-ch109, adc2

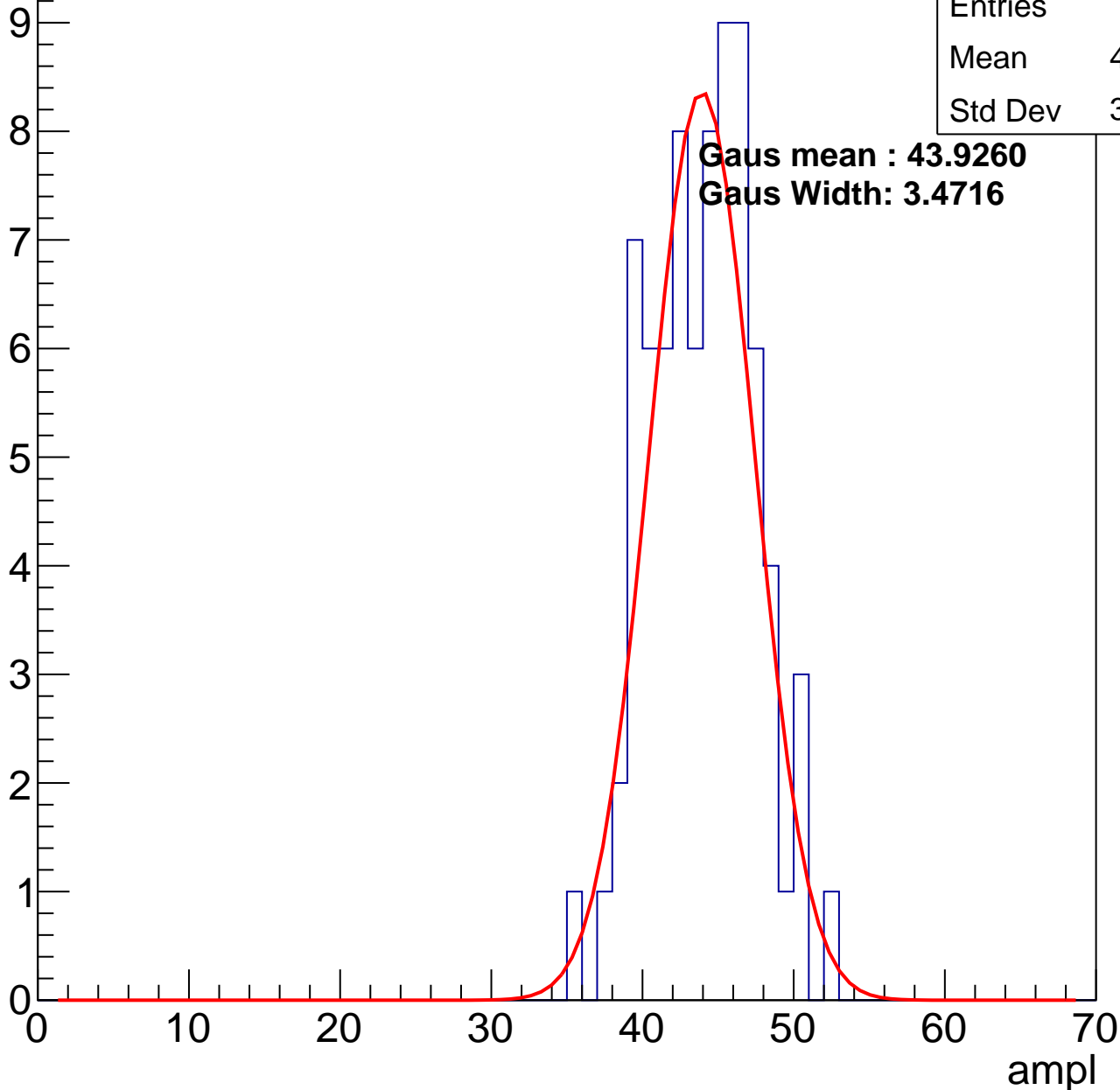
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	78
Mean	43.55
Std Dev	3.414

**Gaus mean : 43.9260**

**Gaus Width: 3.4716**

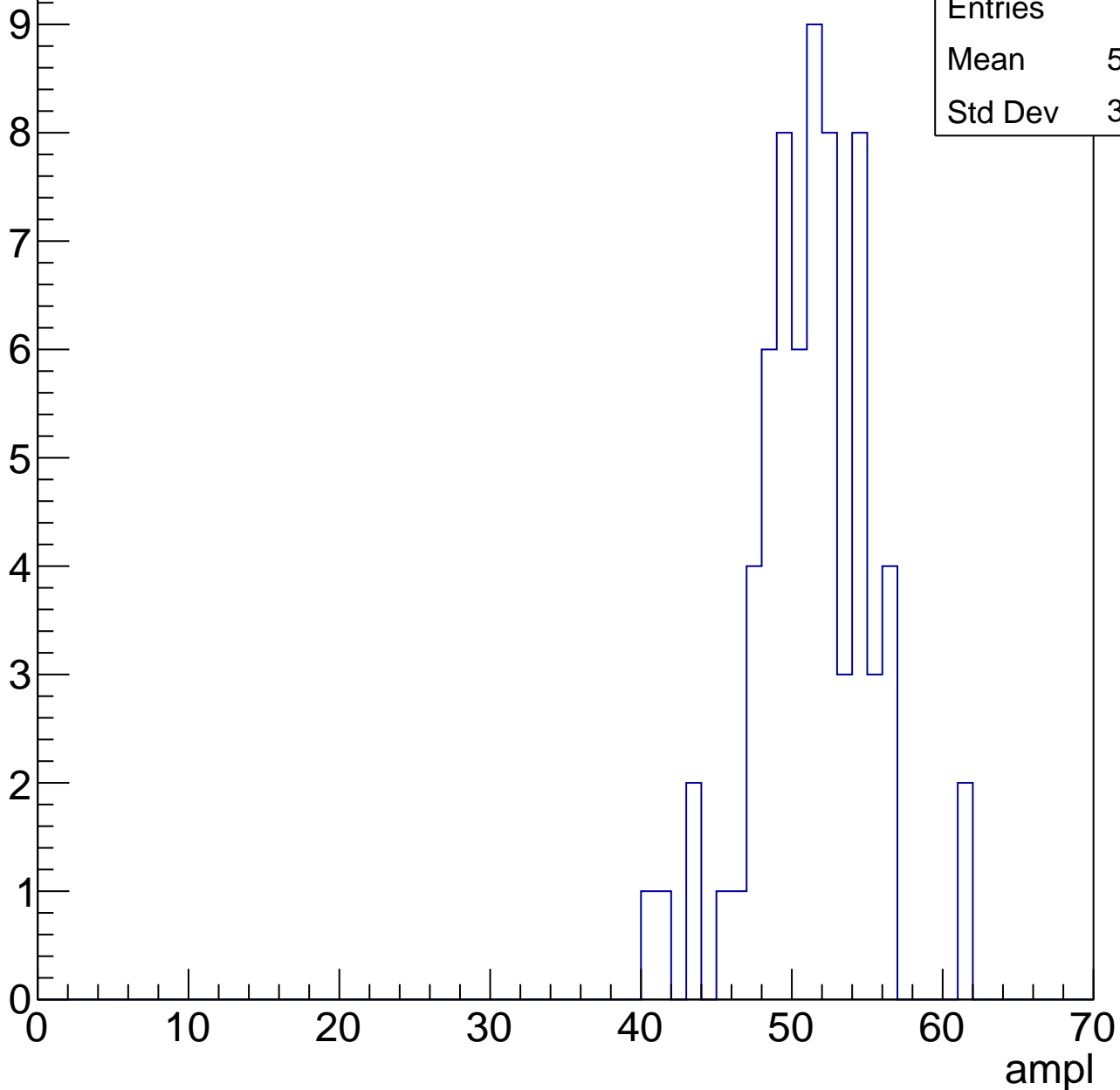


# B0L000S, U7-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	67
Mean	50.79
Std Dev	3.869



# B0L000S, U7-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

10

Entries 64

Mean 57.08

Std Dev 3.144

8

6

4

2

0

0

10

20

30

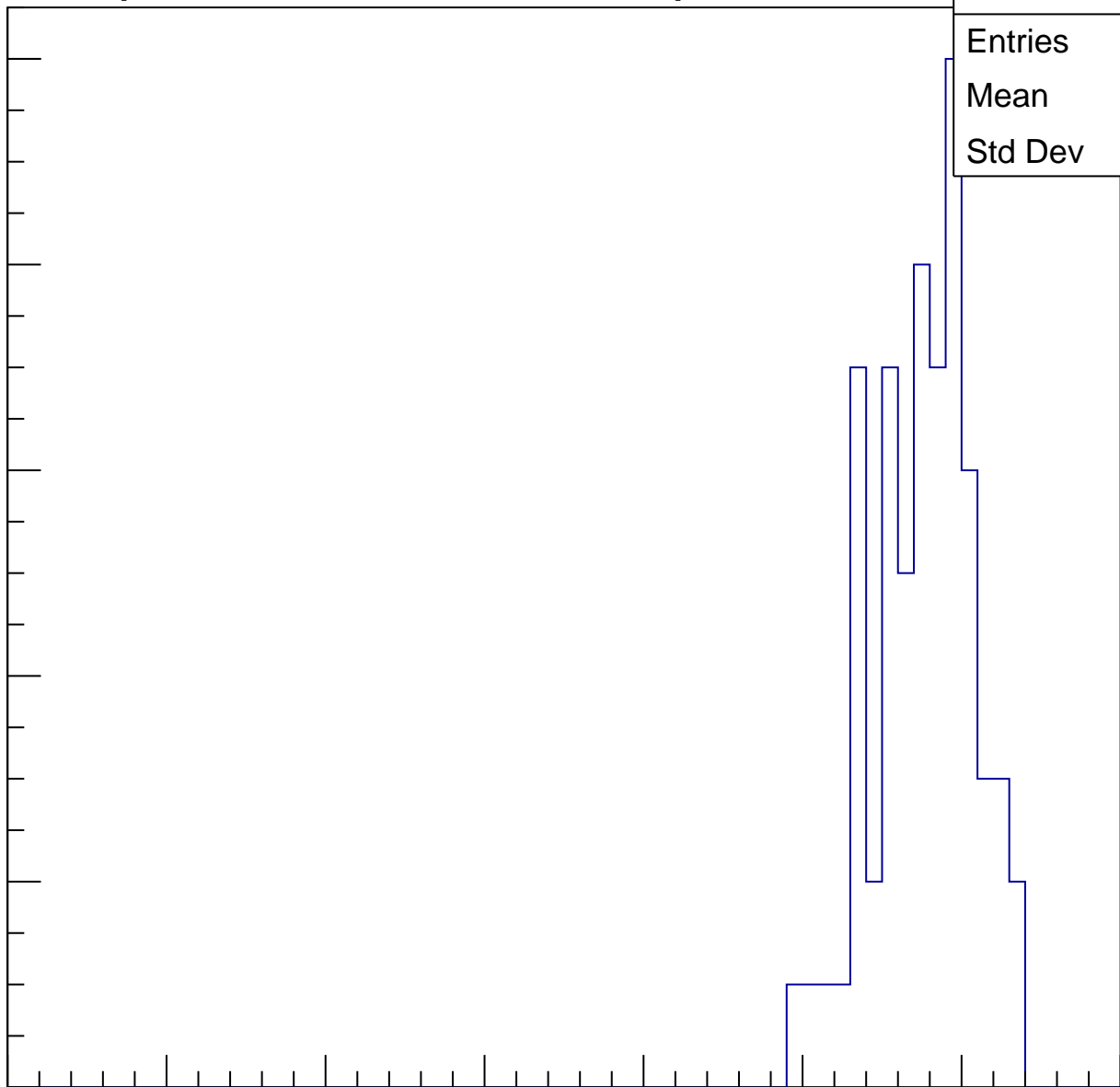
40

50

60

70

ampl

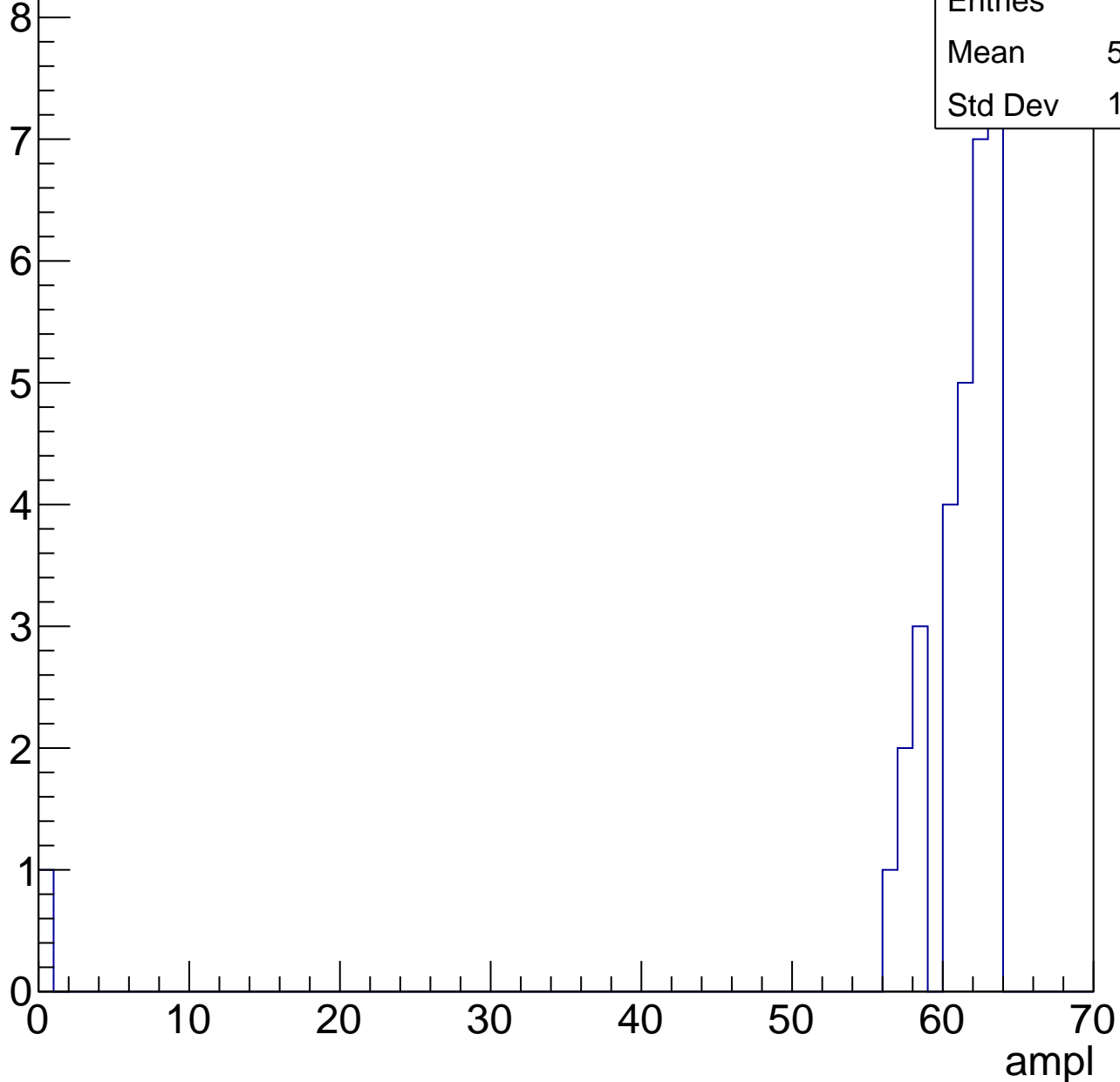


# B0L000S, U7-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	31
Mean	58.94
Std Dev	10.95



# B0L000S, U7-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L000S, U7-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch110, adc0

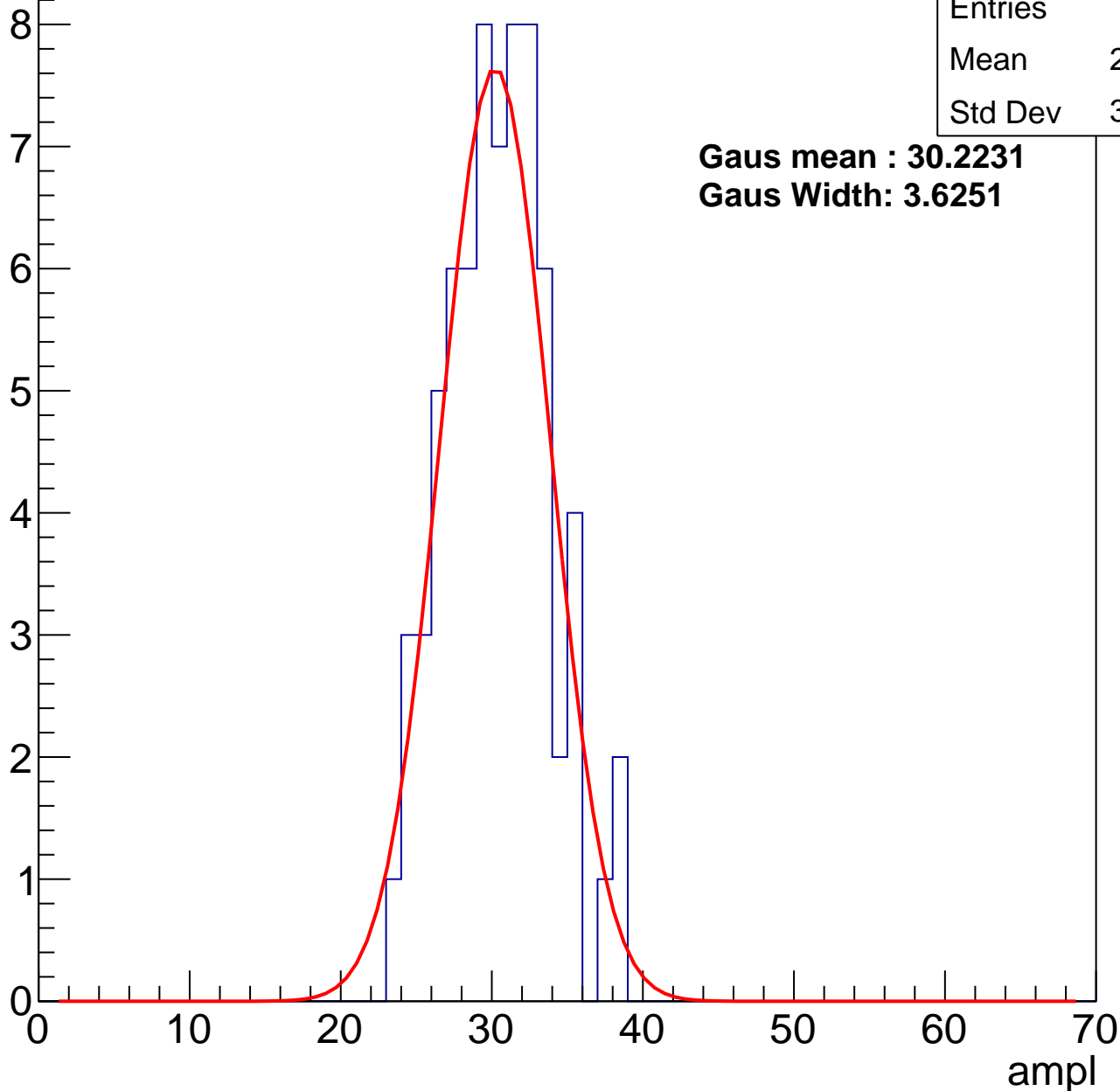
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	70
Mean	29.93
Std Dev	3.382

**Gaus mean : 30.2231**

**Gaus Width: 3.6251**



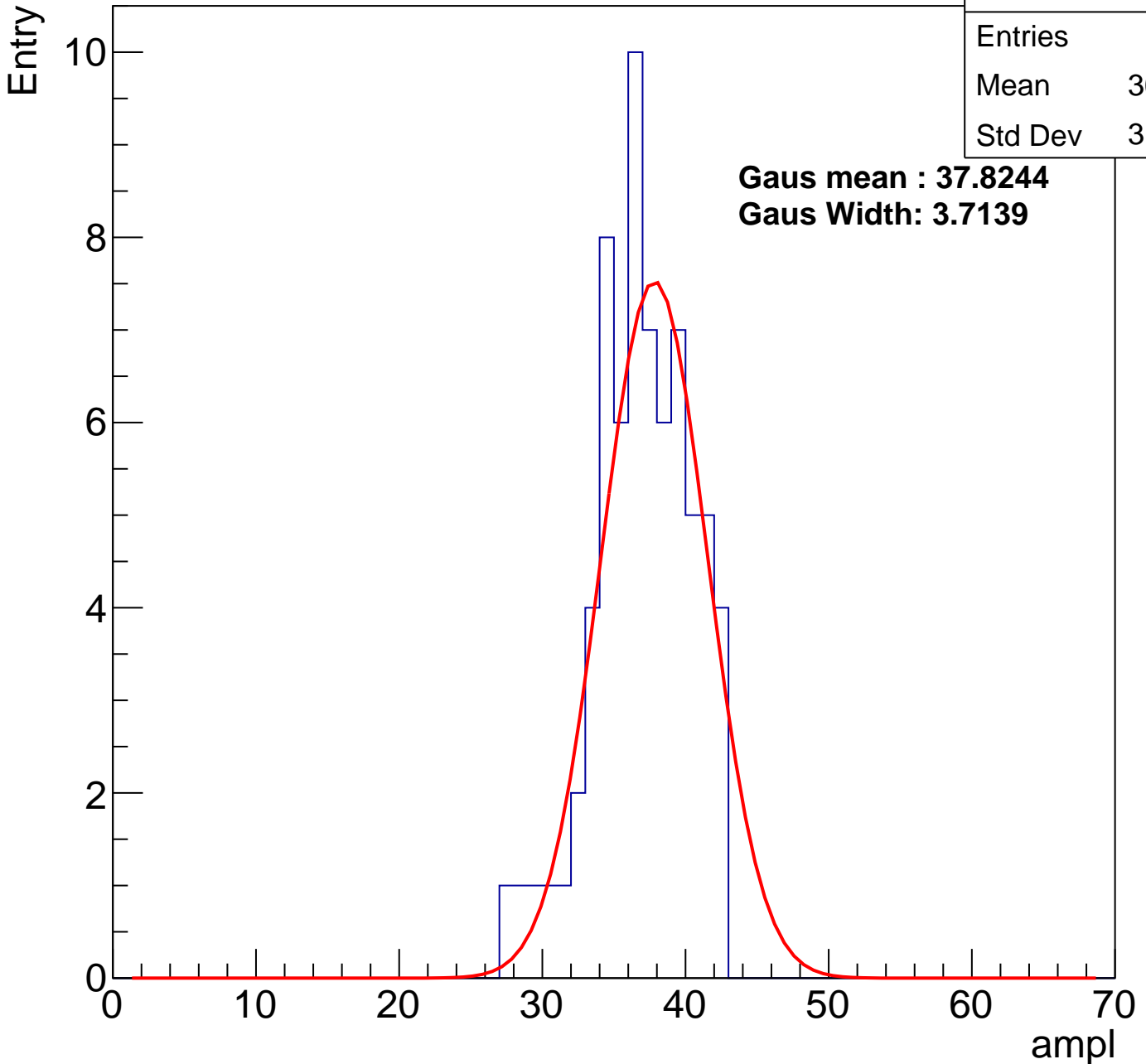
# B0L000S, U7-ch110, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	69
Mean	36.46
Std Dev	3.382

**Gaus mean : 37.8244**

**Gaus Width: 3.7139**



# B0L000S, U7-ch110, adc2

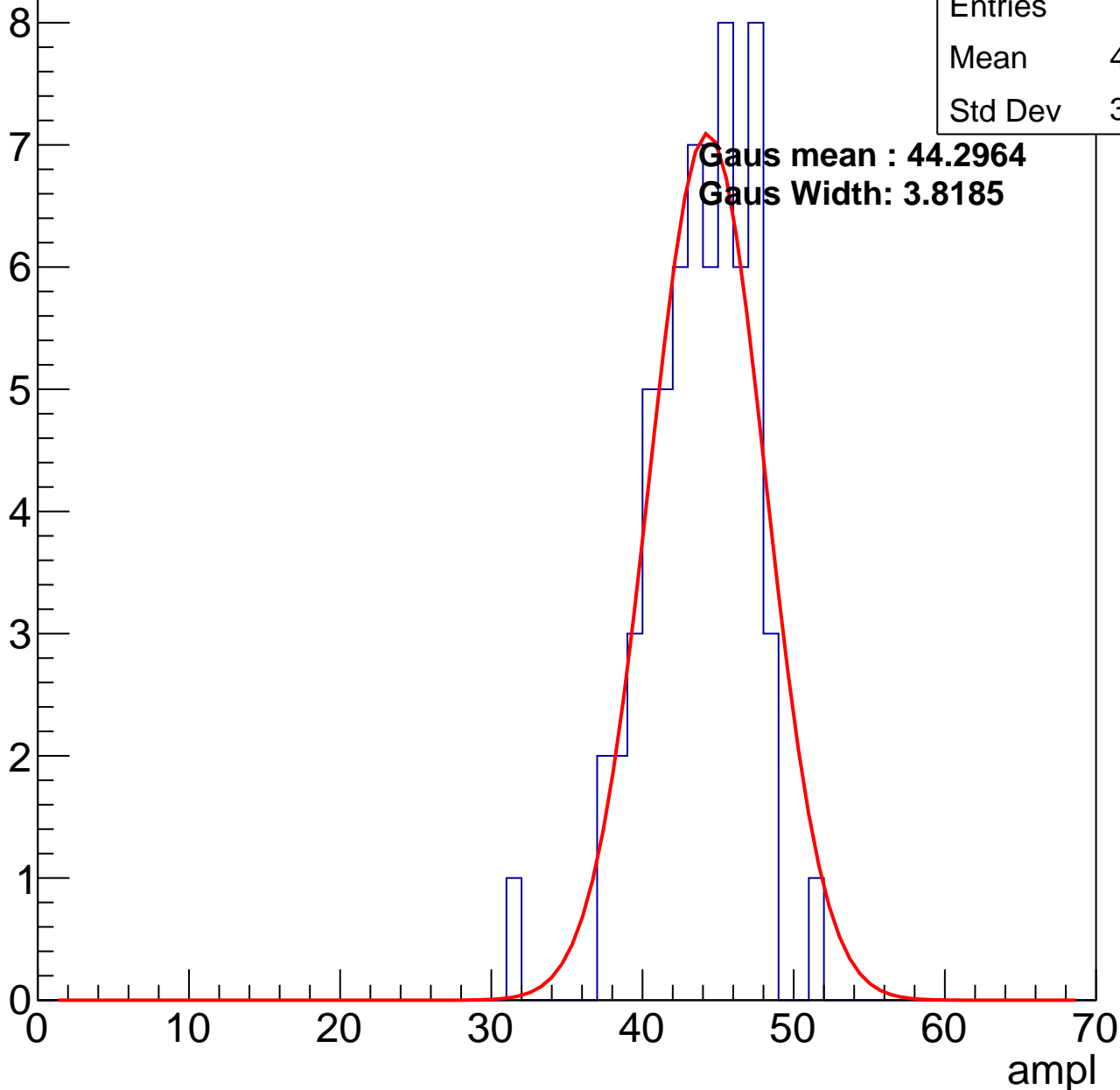
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	63
Mean	43.29
Std Dev	3.425

**Gaus mean : 44.2964**

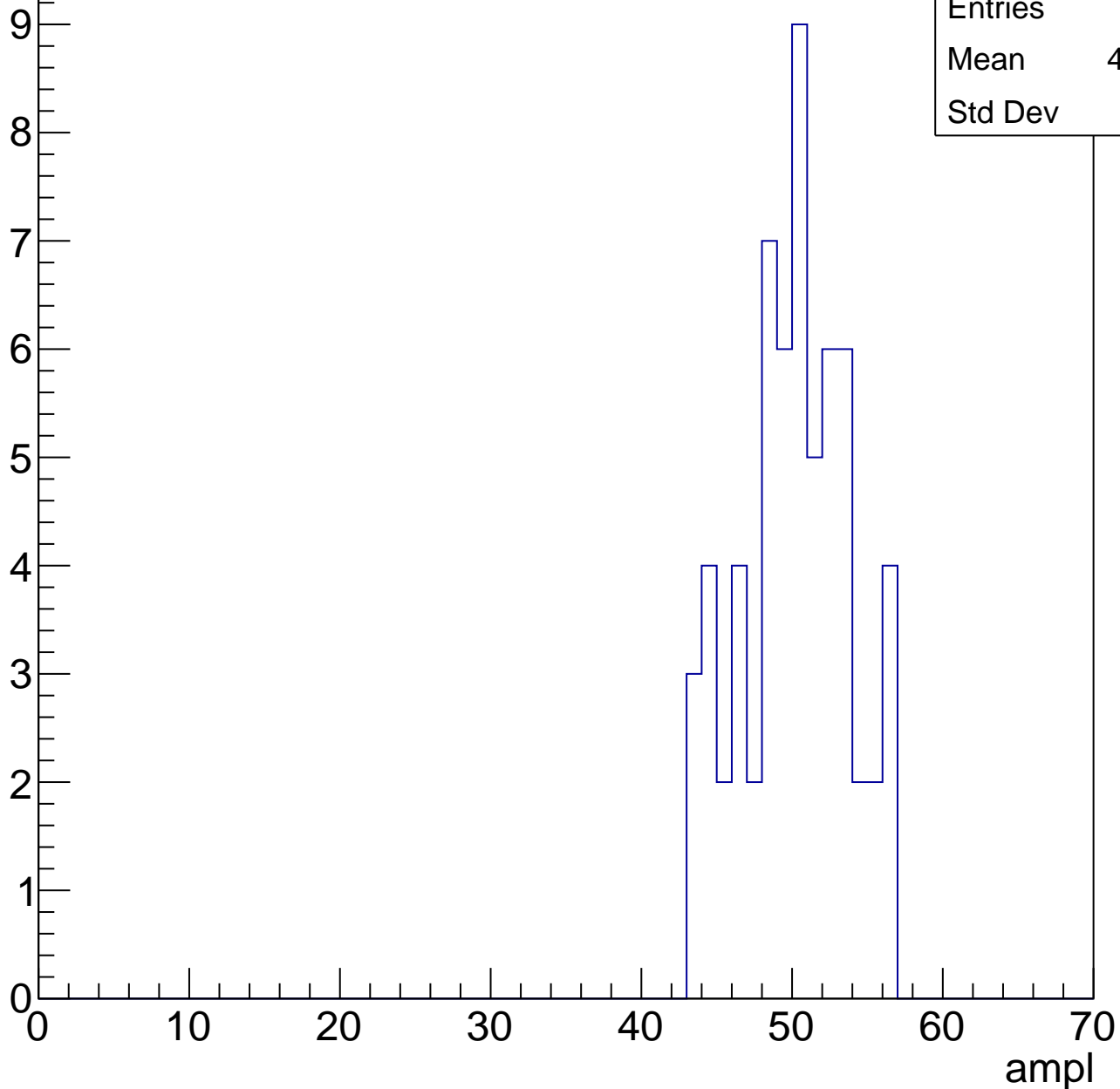
**Gaus Width: 3.8185**



# B0L000S, U7-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

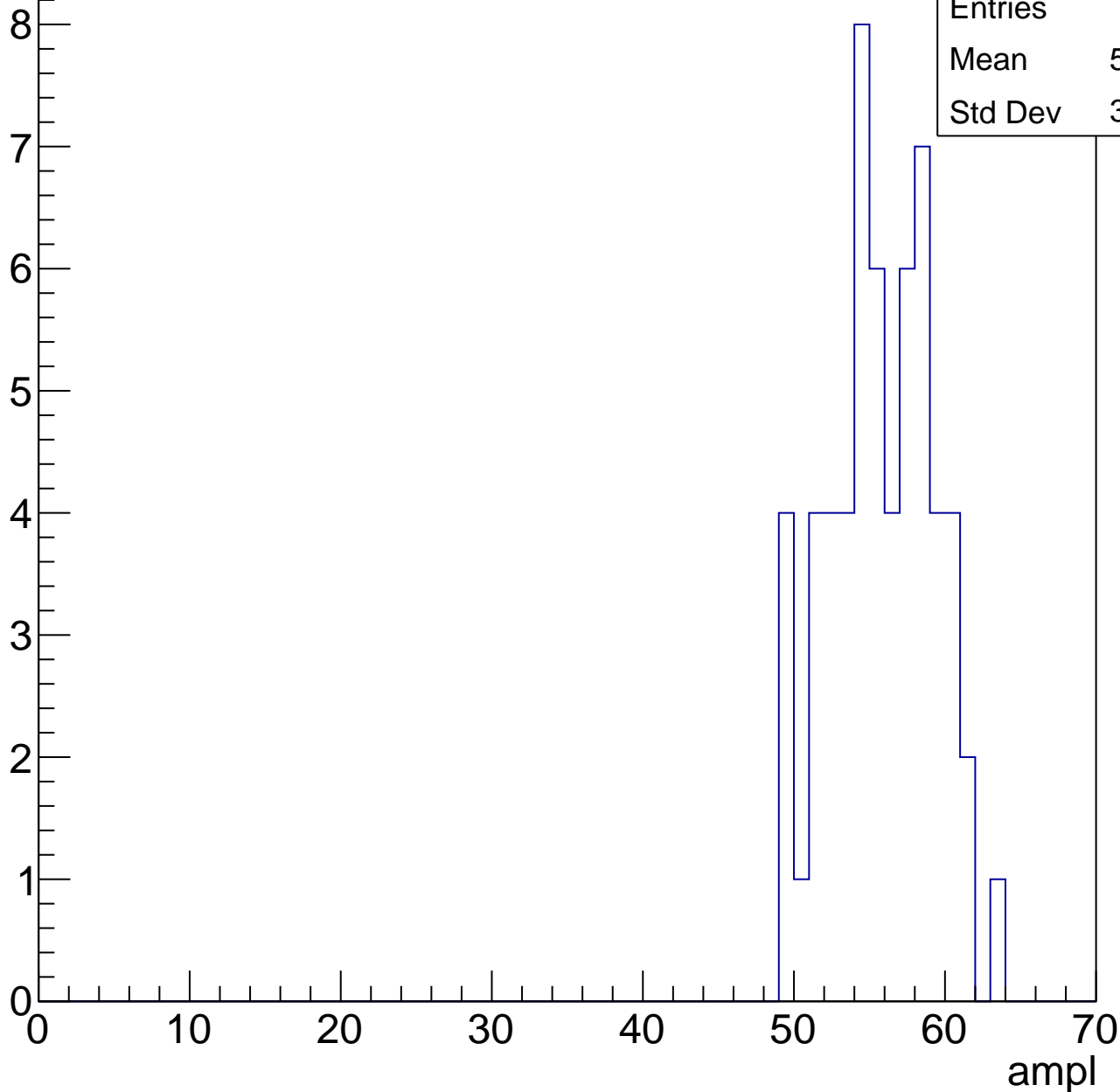


# B0L000S, U7-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	59
Mean	55.34
Std Dev	3.388

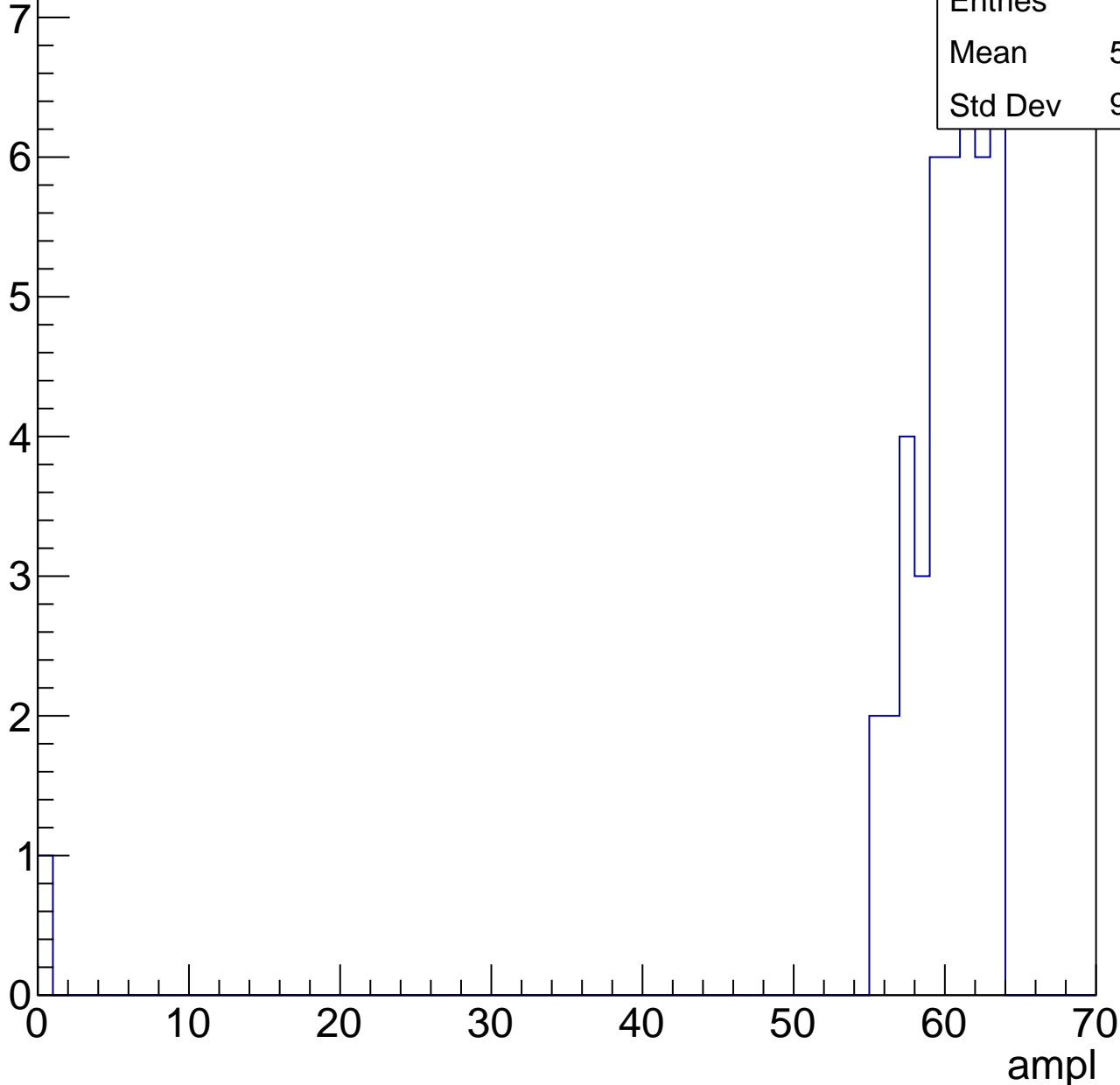


# B0L000S, U7-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	44
Mean	58.59
Std Dev	9.223



# B0L000S, U7-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch111, adc0

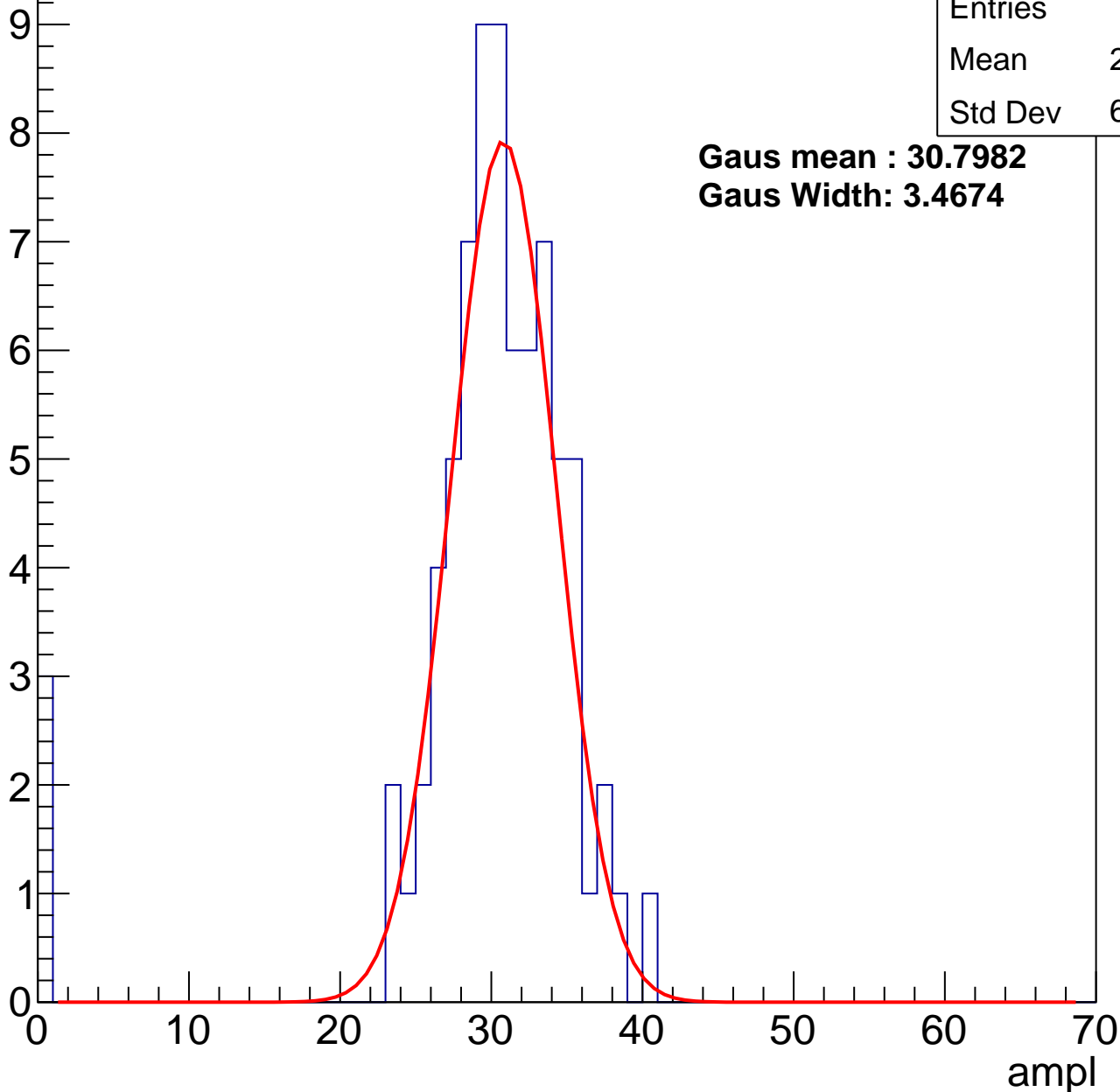
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	76
Mean	29.32
Std Dev	6.873

**Gaus mean : 30.7982**

**Gaus Width: 3.4674**



# B0L000S, U7-ch111, adc1

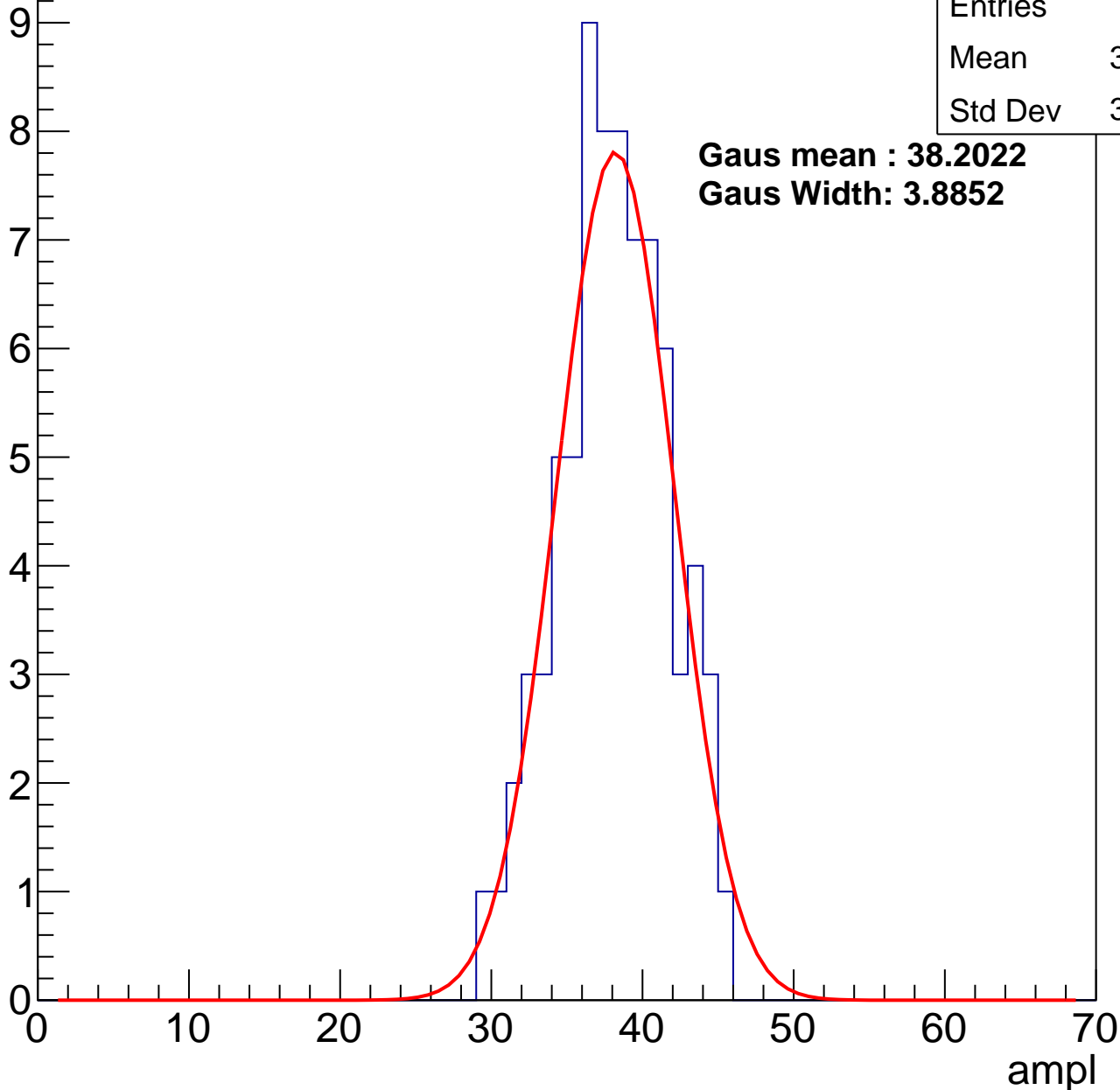
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	76
Mean	37.62
Std Dev	3.587

**Gaus mean : 38.2022**

**Gaus Width: 3.8852**



# B0L000S, U7-ch111, adc2

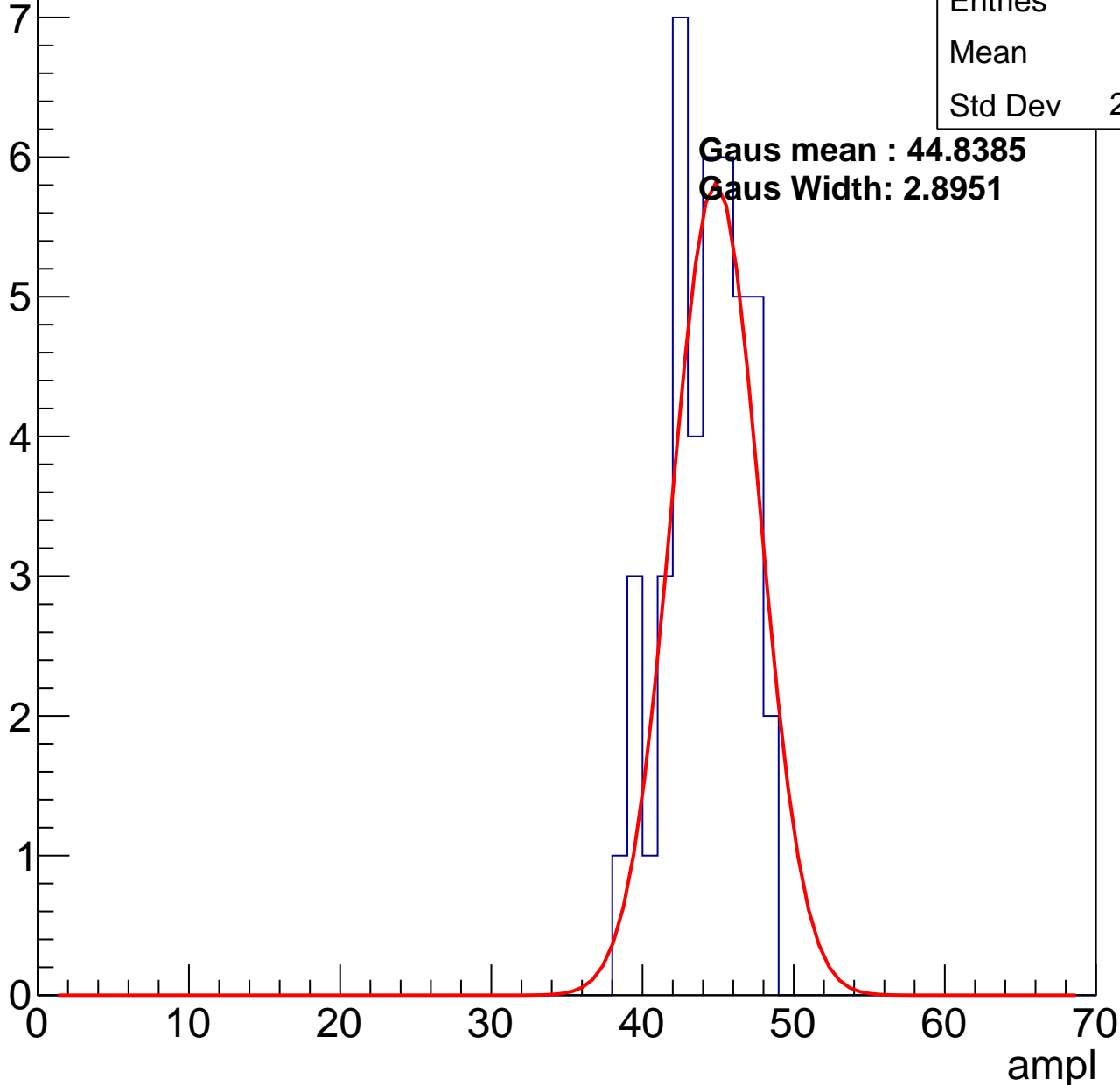
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	43
Mean	43.7
Std Dev	2.575

Gaus mean : 44.8385

Gaus Width: 2.8951



# B0L000S, U7-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

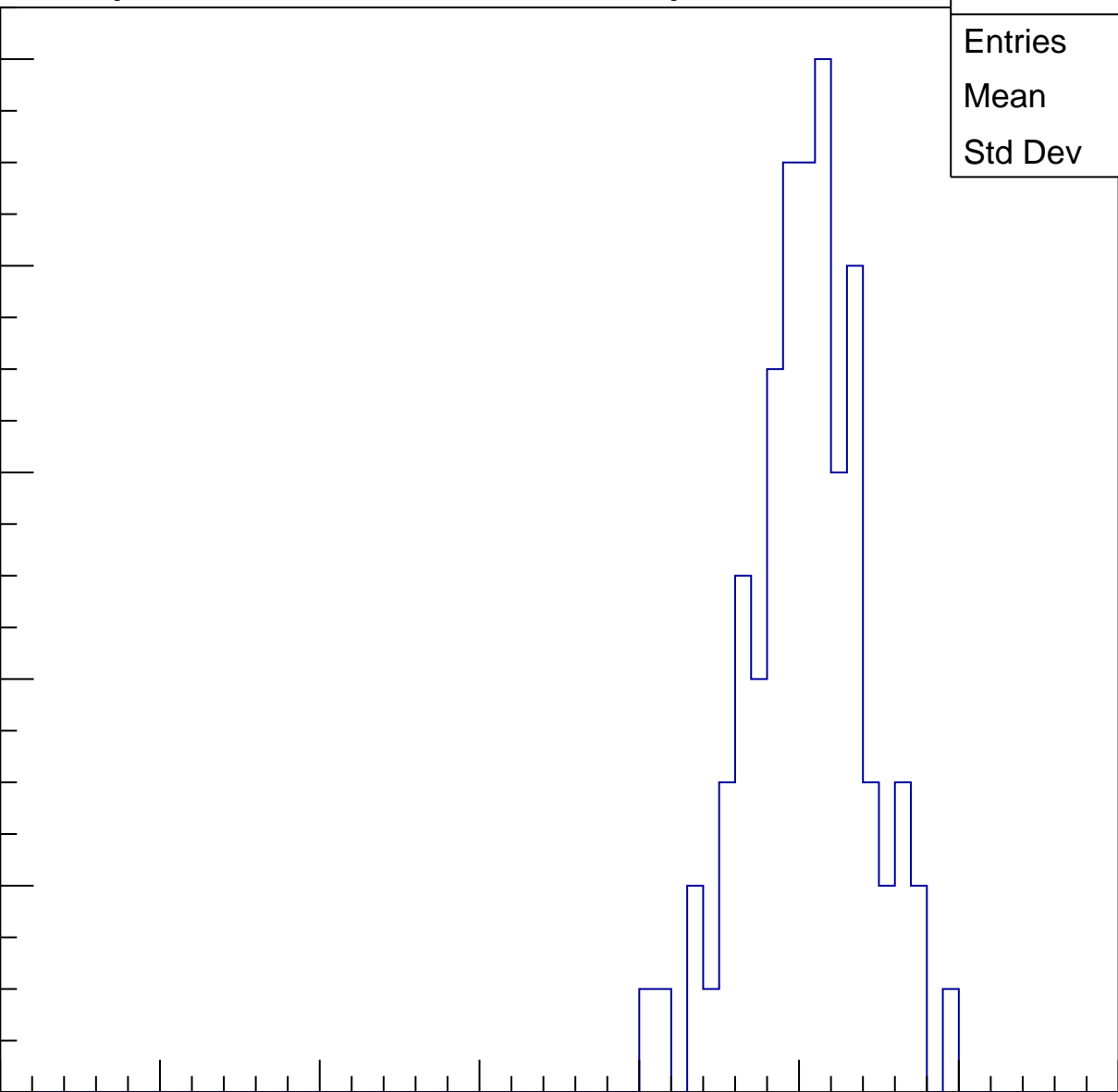
Entries	77
Mean	50
Std Dev	3.665

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

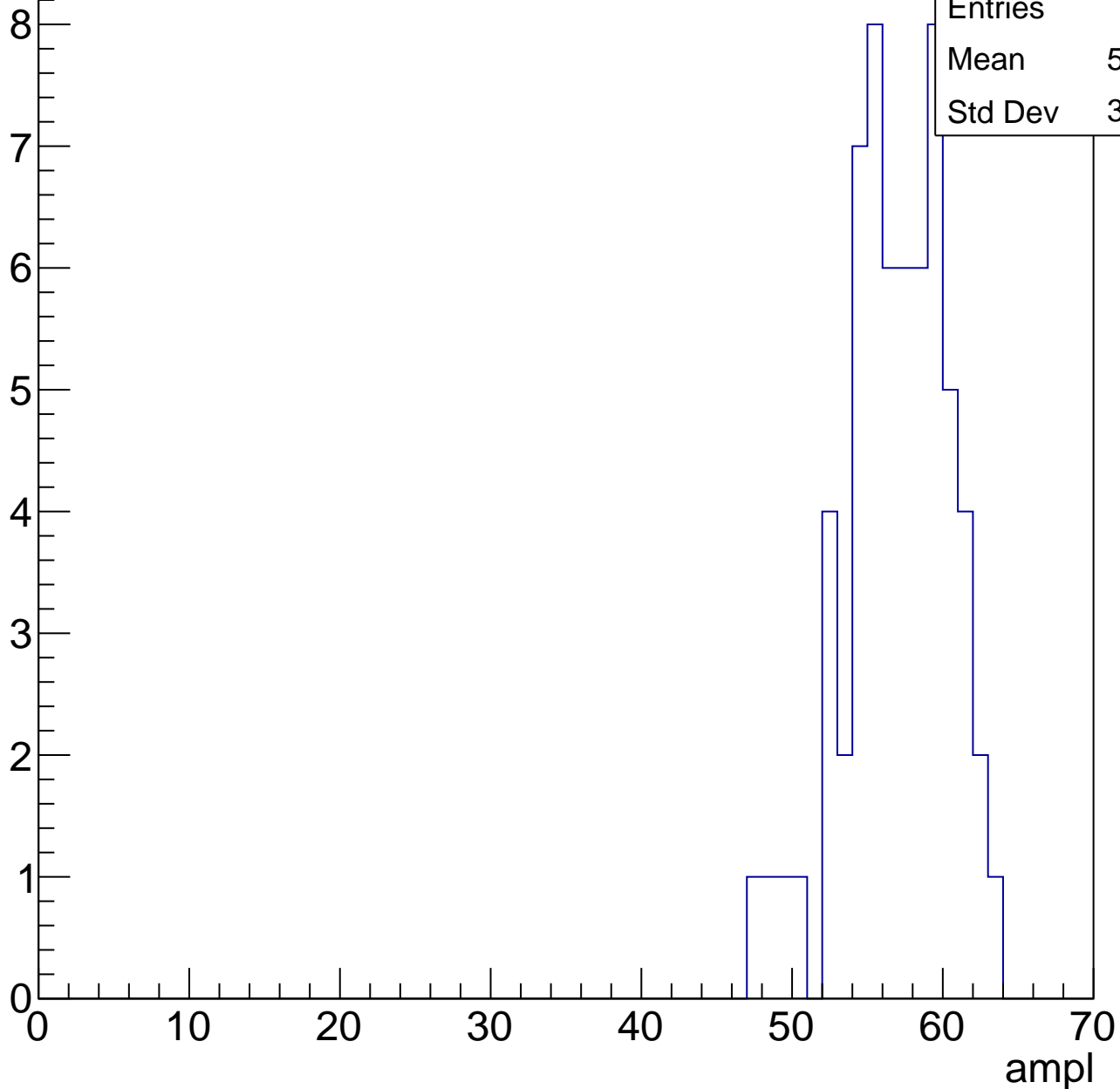
ampl



# B0L000S, U7-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



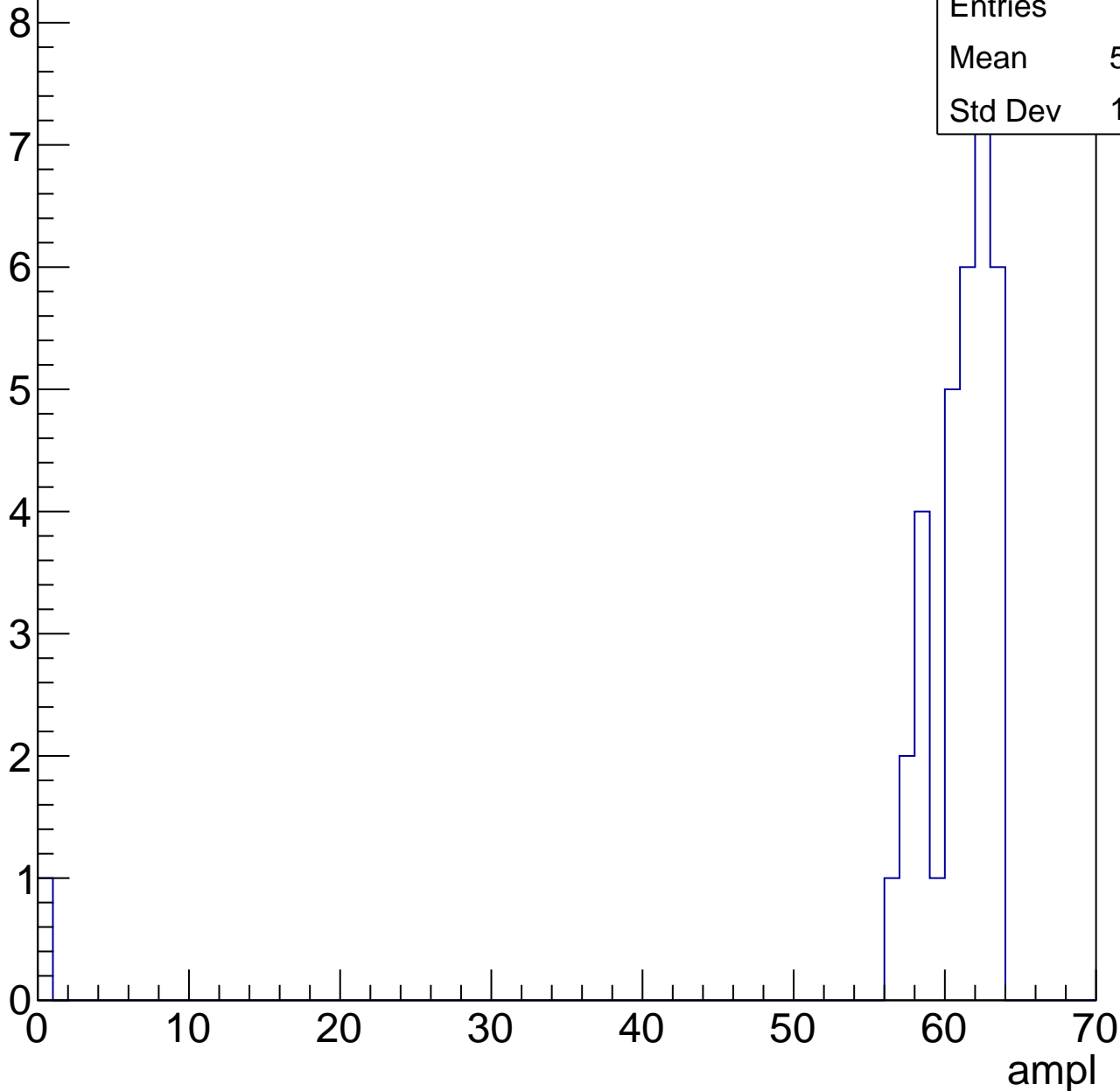
Entries	63
Mean	56.43
Std Dev	3.426

# B0L000S, U7-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	34
Mean	58.85
Std Dev	10.43



# B0L000S, U7-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch112, adc0

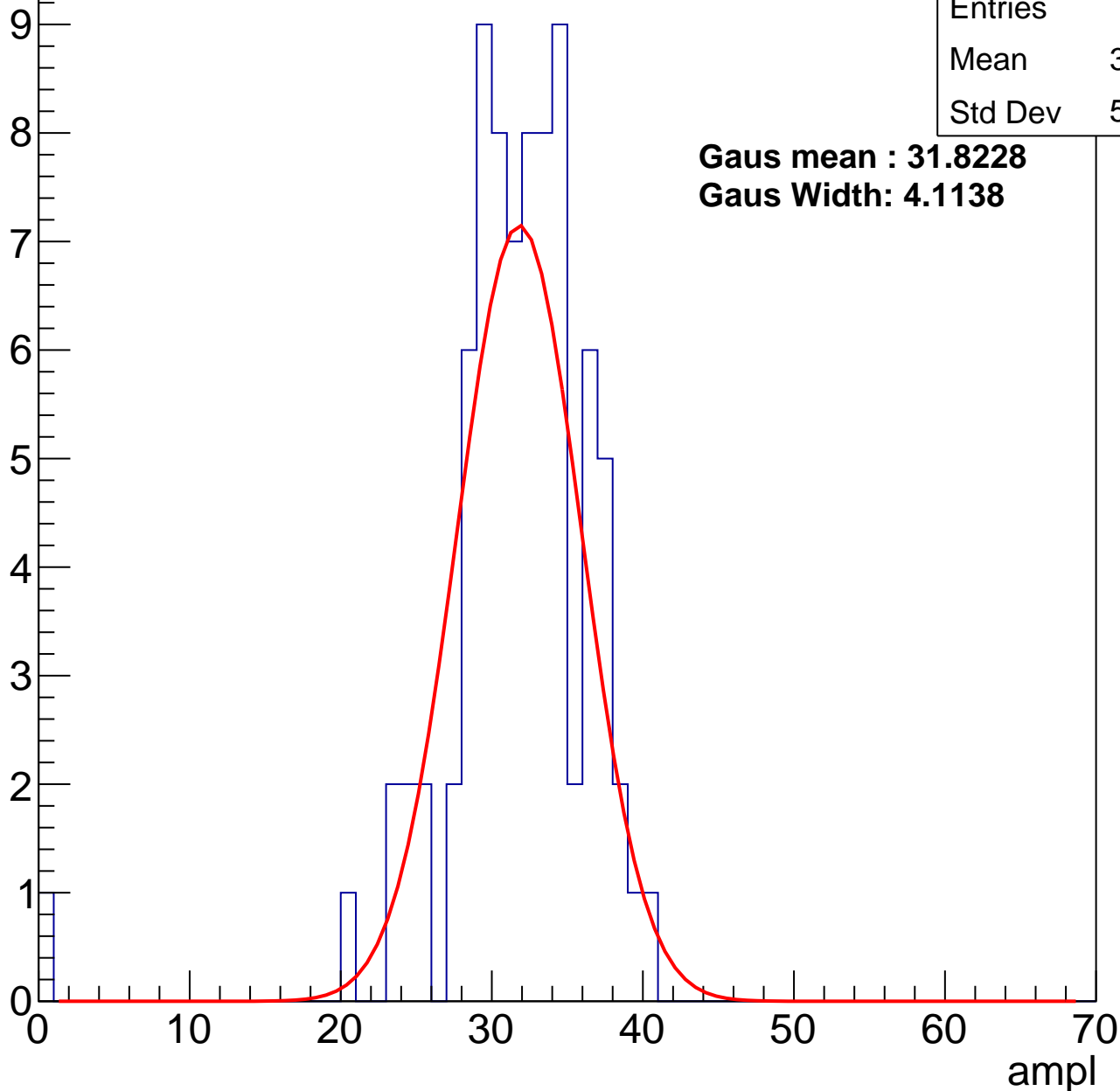
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	82
Mean	31.17
Std Dev	5.219

**Gaus mean : 31.8228**

**Gaus Width: 4.1138**



# B0L000S, U7-ch112, adc1

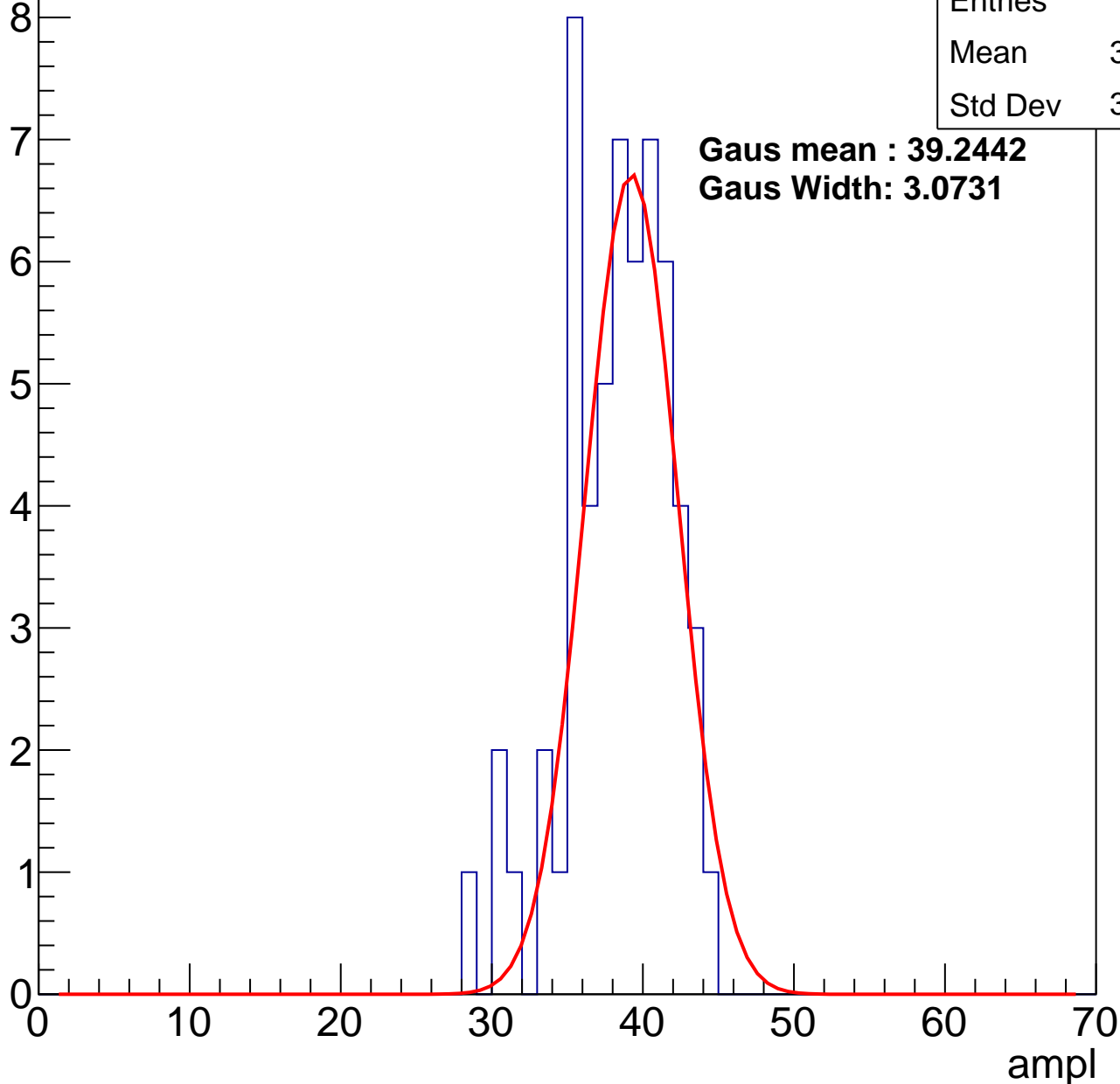
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	58
Mean	37.84
Std Dev	3.468

**Gaus mean : 39.2442**

**Gaus Width: 3.0731**



# B0L000S, U7-ch112, adc2

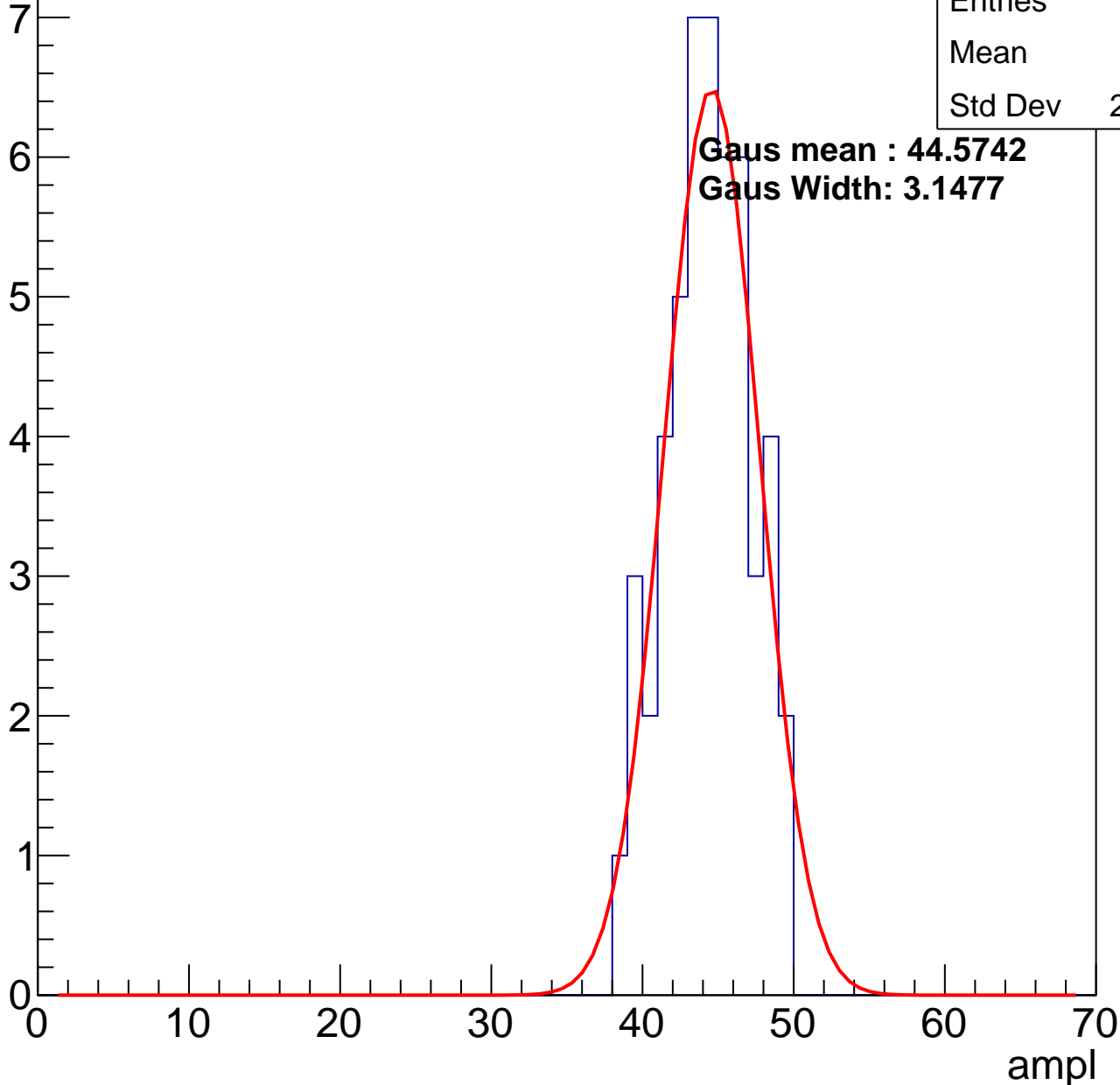
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	50
Mean	43.9
Std Dev	2.744

**Gaus mean : 44.5742**

**Gaus Width: 3.1477**

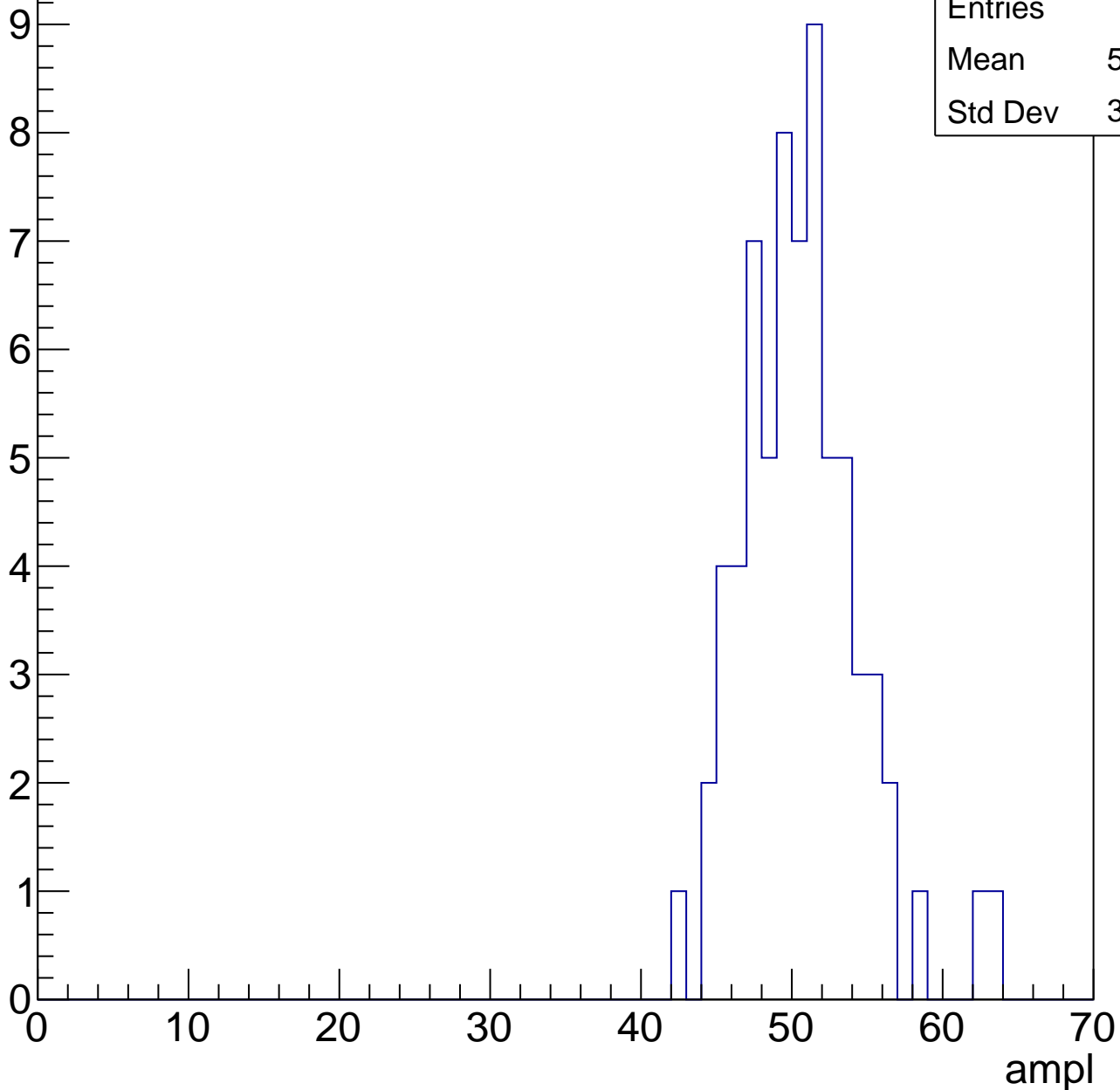


# B0L000S, U7-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	68
Mean	50.16
Std Dev	3.902

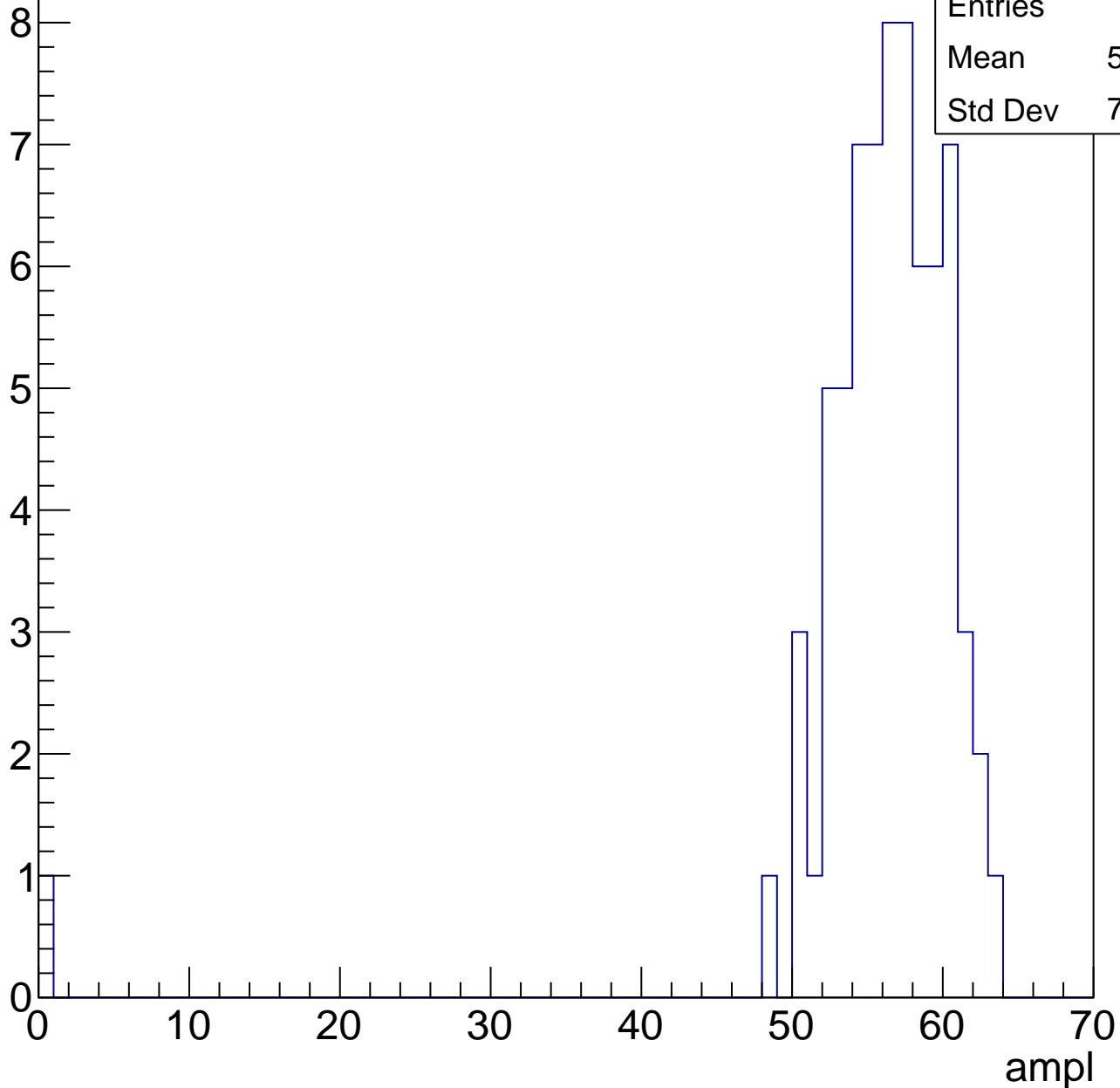


# B0L000S, U7-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	71
Mean	55.39
Std Dev	7.374

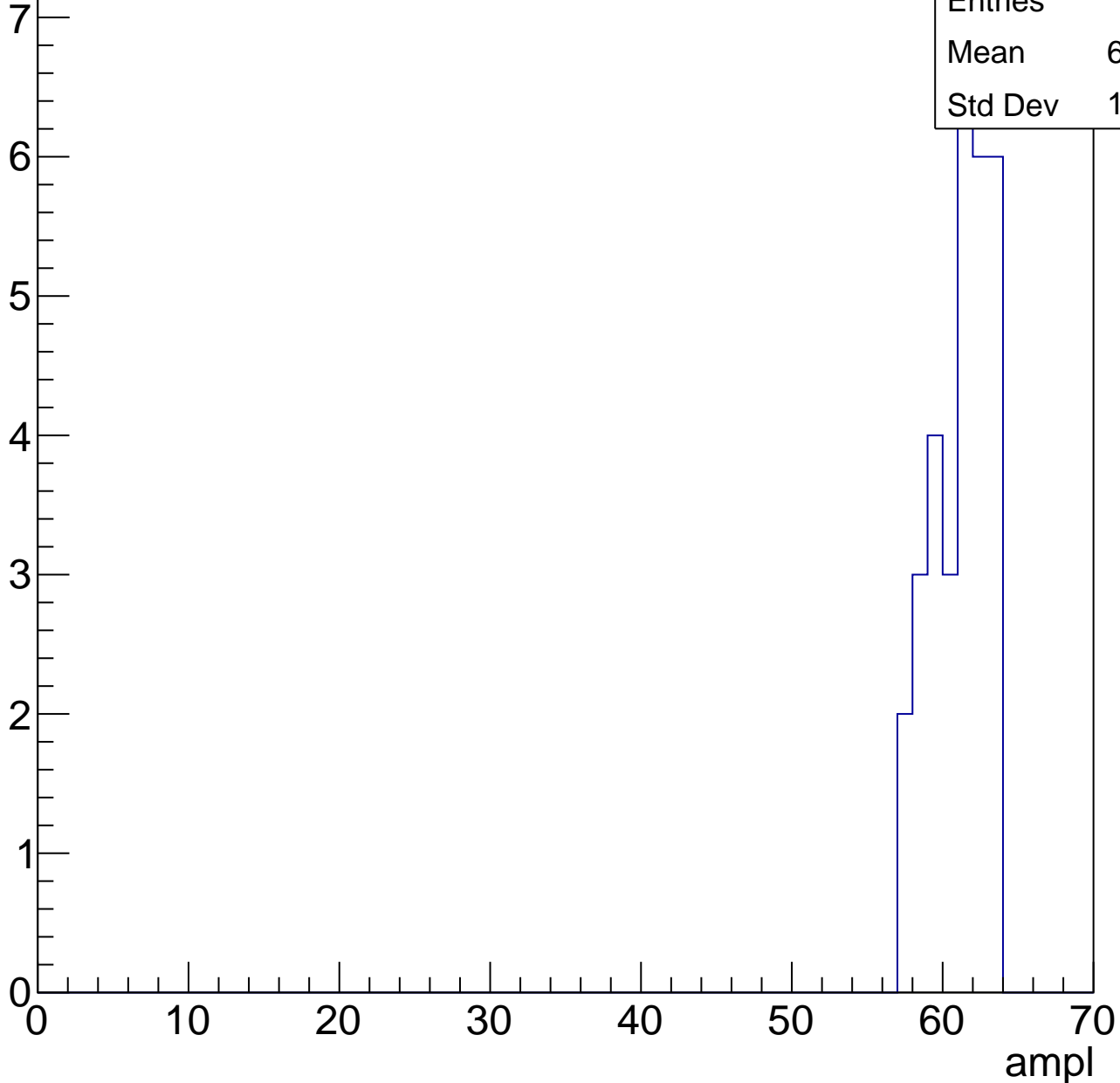


# B0L000S, U7-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	31
Mean	60.68
Std Dev	1.838



# B0L000S, U7-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch113, adc0

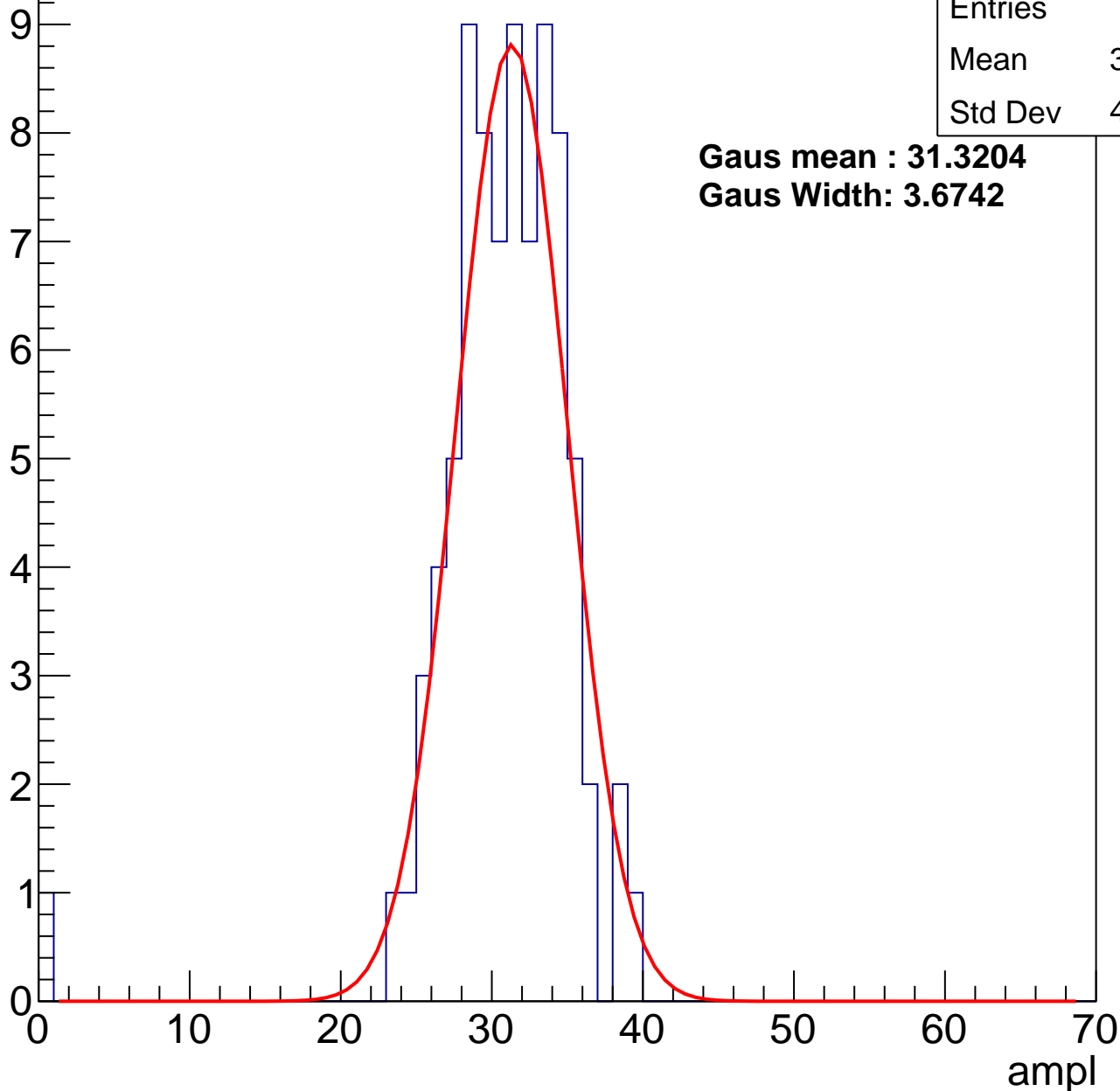
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	82
Mean	30.35
Std Dev	4.756

**Gaus mean : 31.3204**

**Gaus Width: 3.6742**



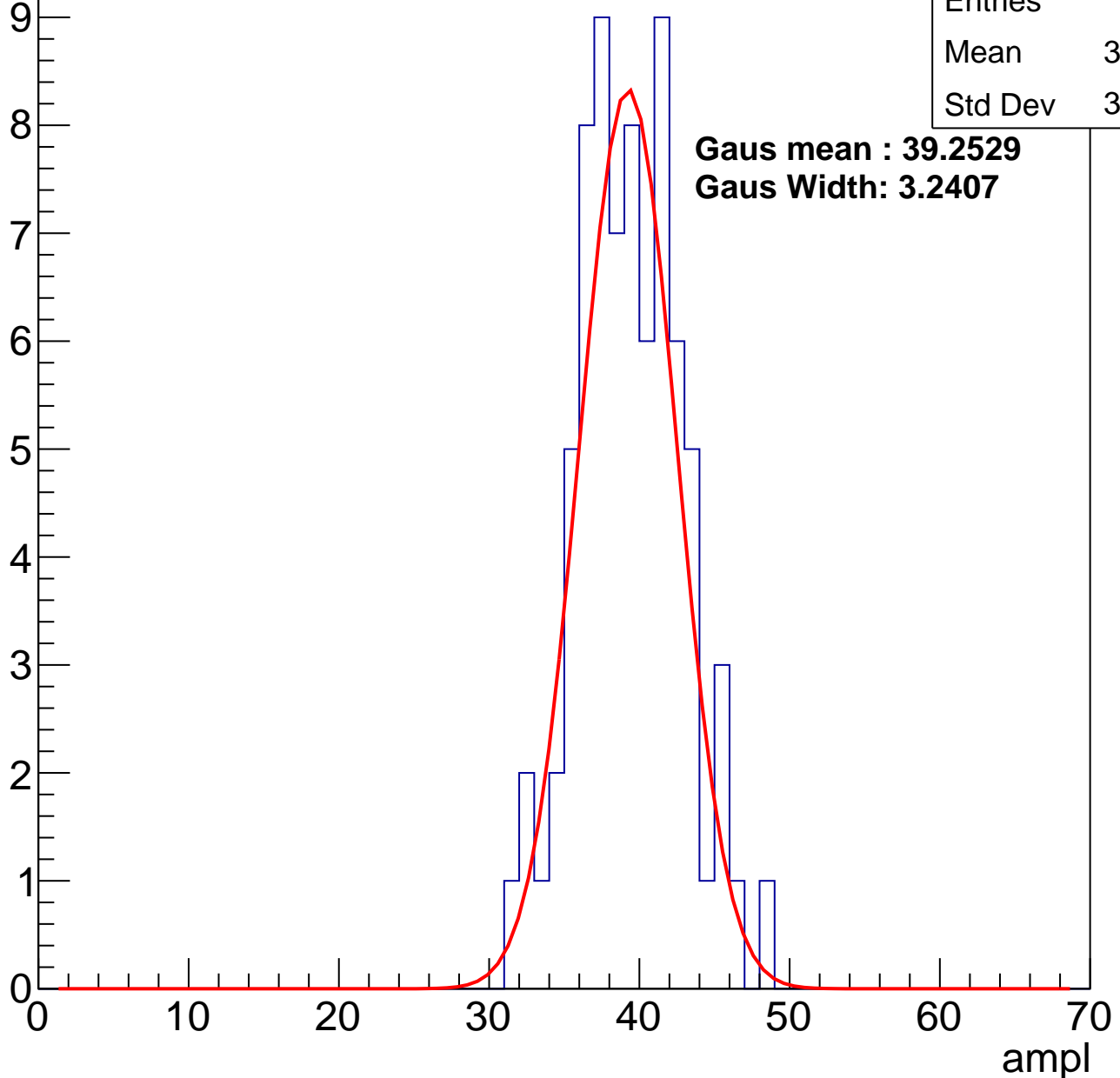
# B0L000S, U7-ch113, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	75
Mean	38.92
Std Dev	3.428

**Gaus mean : 39.2529**  
**Gaus Width: 3.2407**



# B0L000S, U7-ch113, adc2

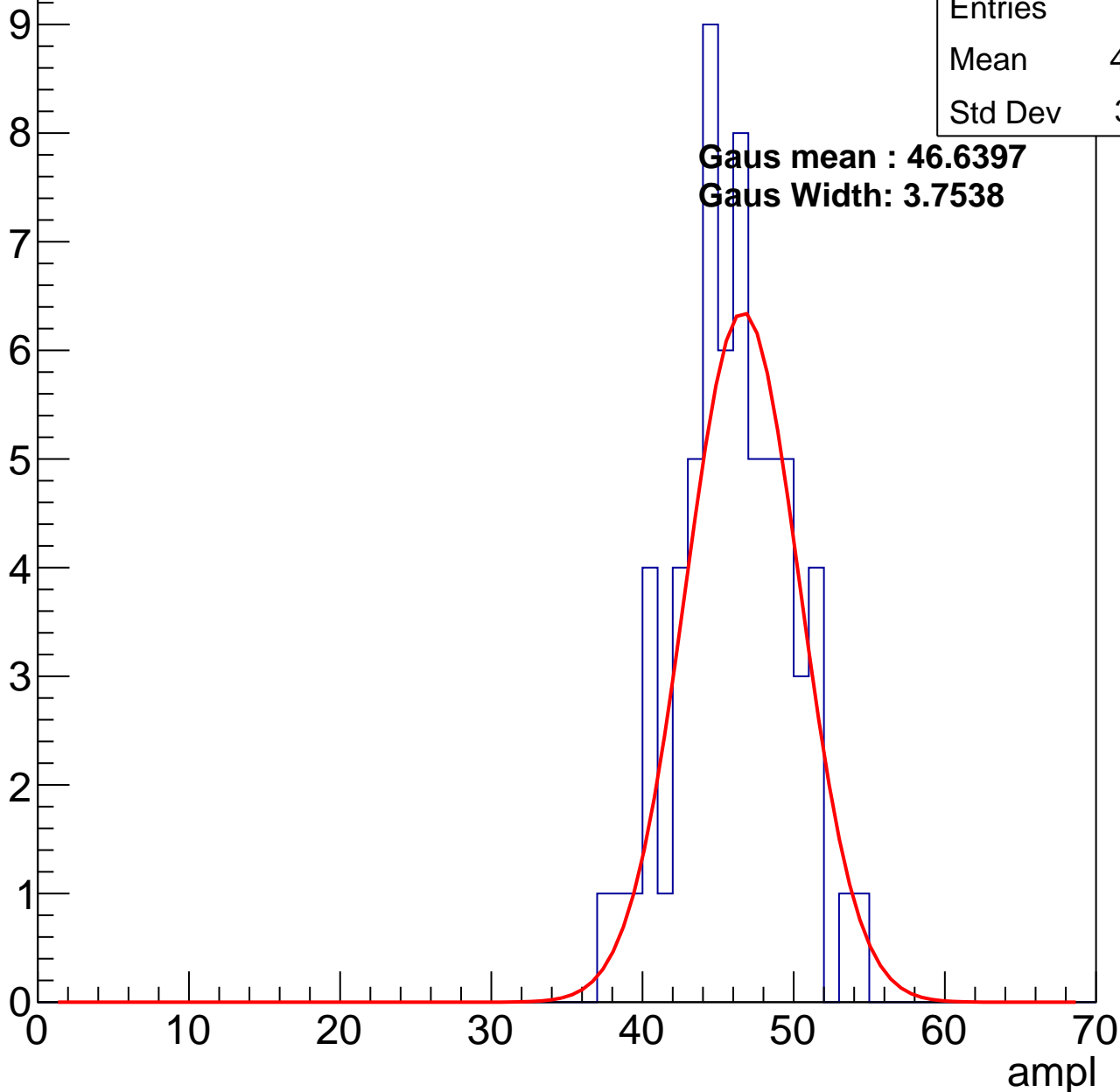
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	64
Mean	45.52
Std Dev	3.601

**Gaus mean : 46.6397**

**Gaus Width: 3.7538**

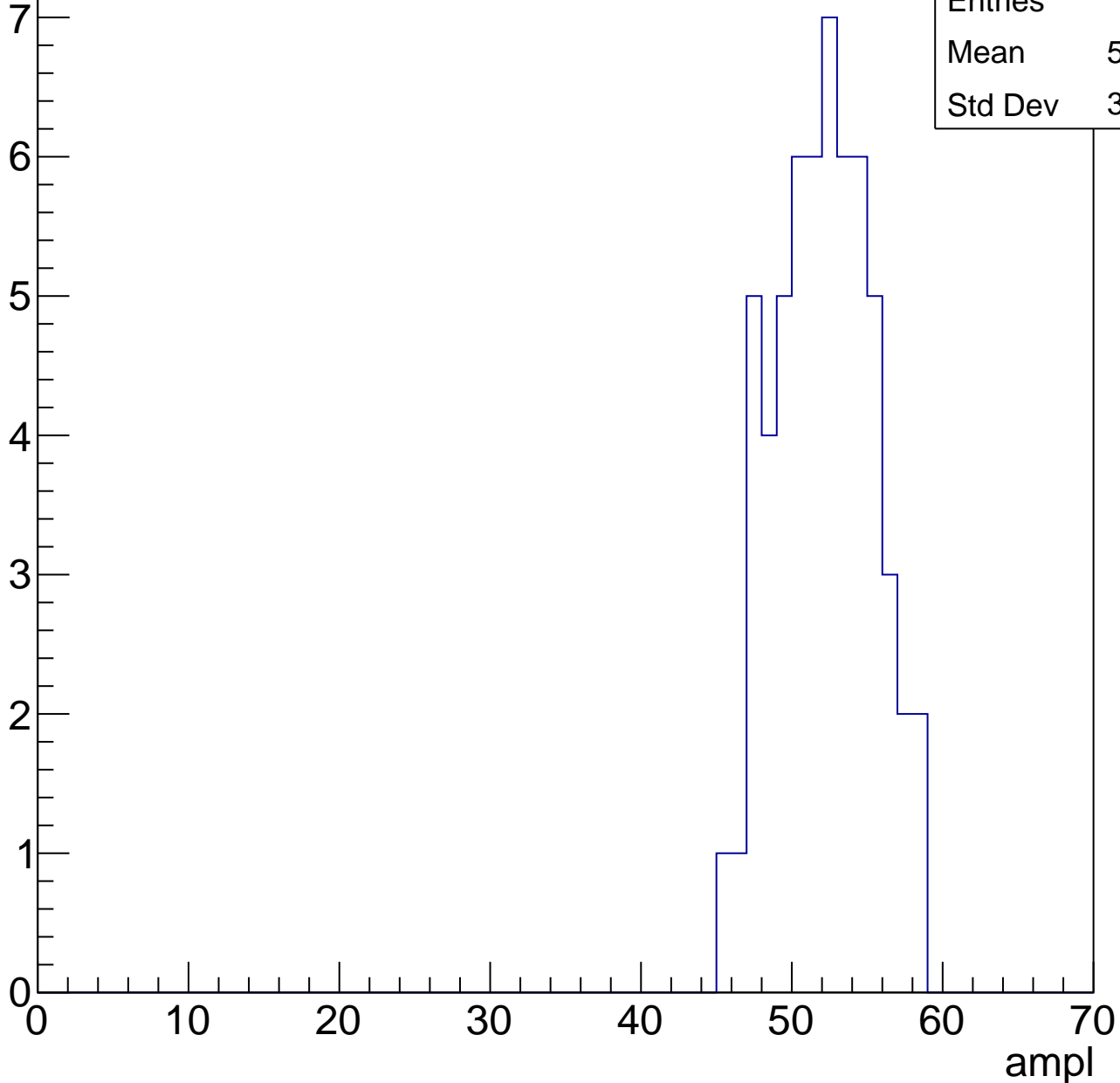


# B0L000S, U7-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	59
Mean	51.66
Std Dev	3.155

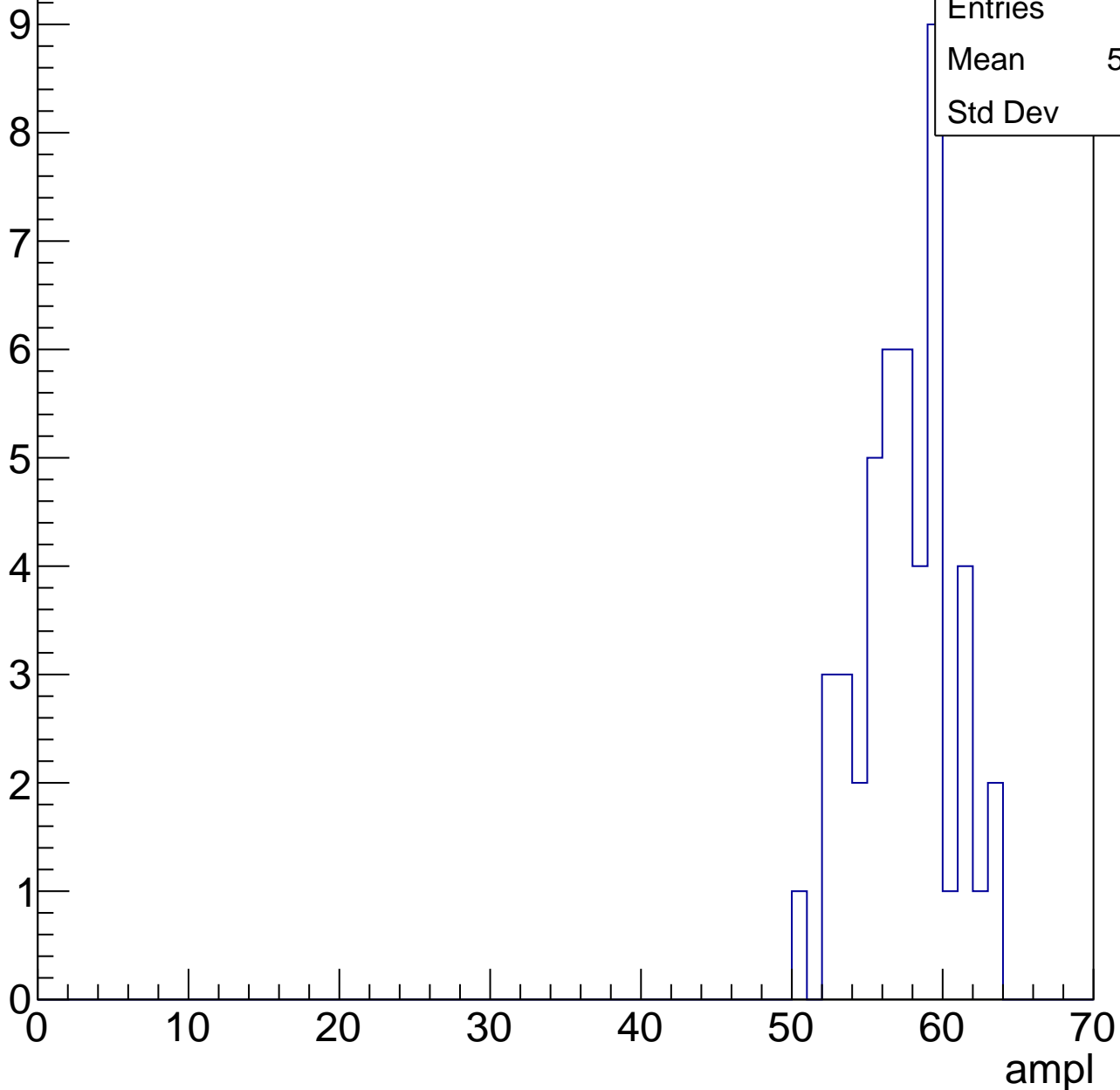


# B0L000S, U7-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

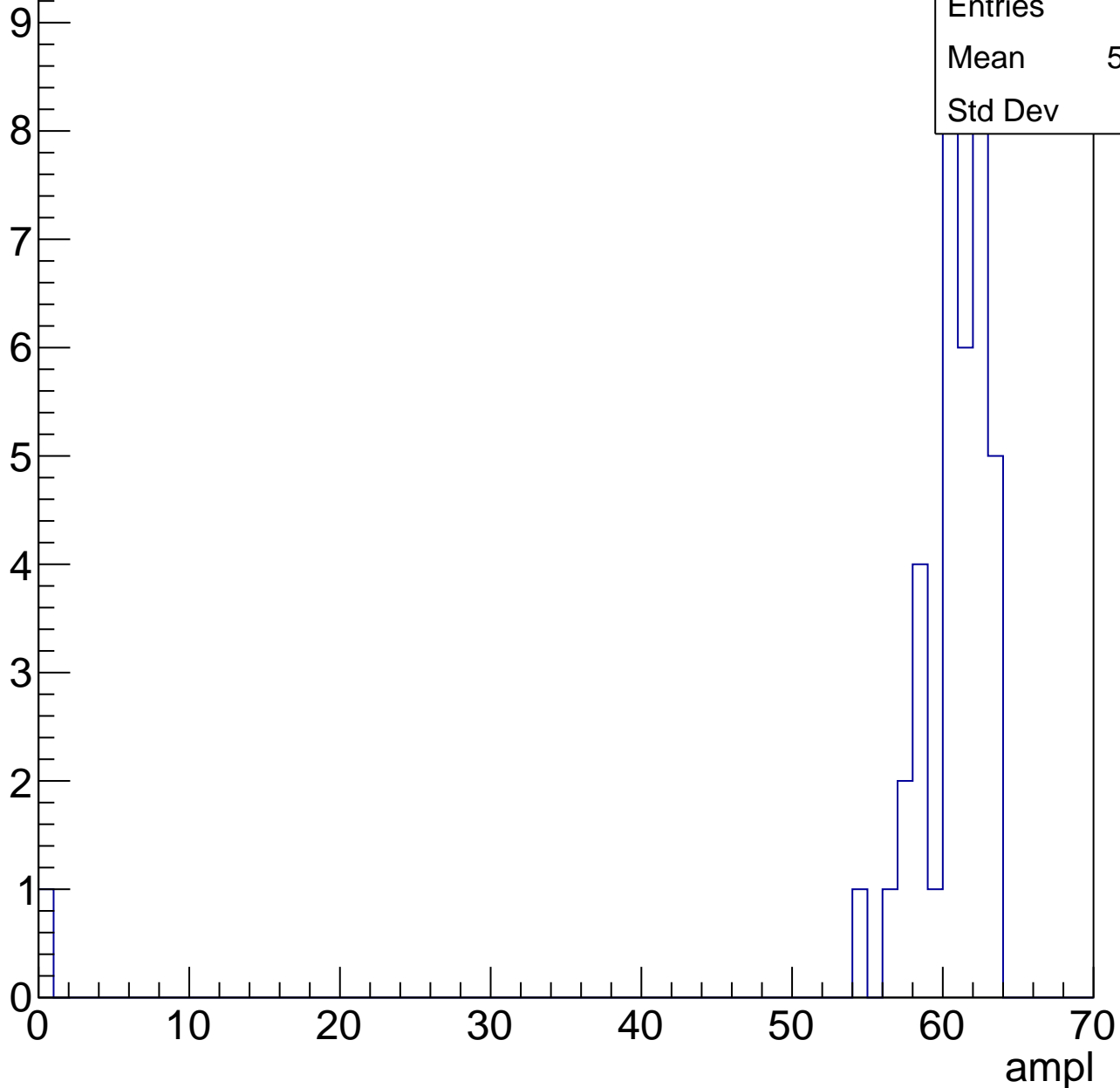
Entries	47
Mean	57.04
Std Dev	3.01



# B0L000S, U7-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L000S, U7-ch114, adc0

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	77
Mean	30.61
Std Dev	3.593

**Gaus mean : 31.0853**

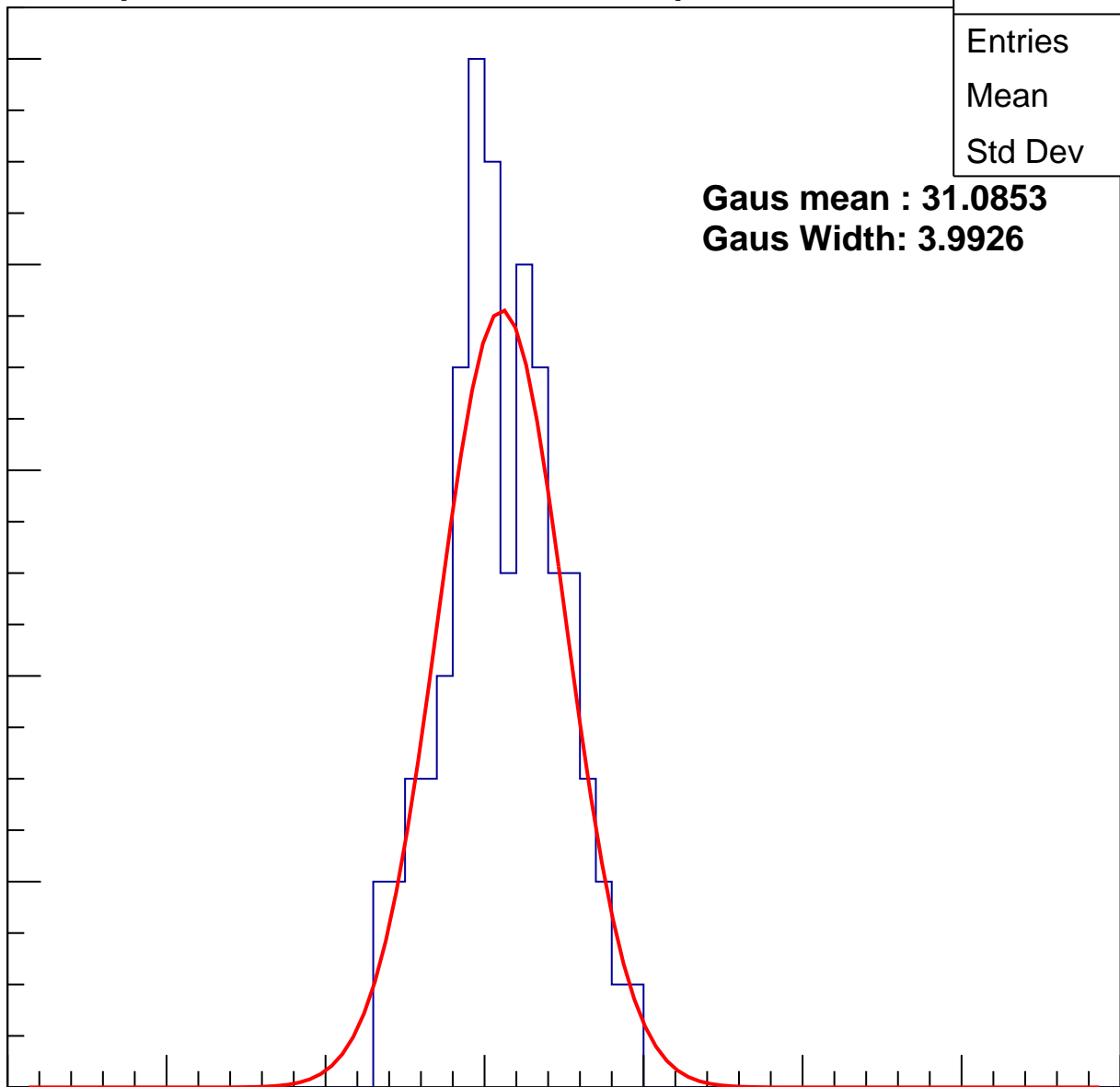
**Gaus Width: 3.9926**

Entry

10  
8  
6  
4  
2  
0

ampl

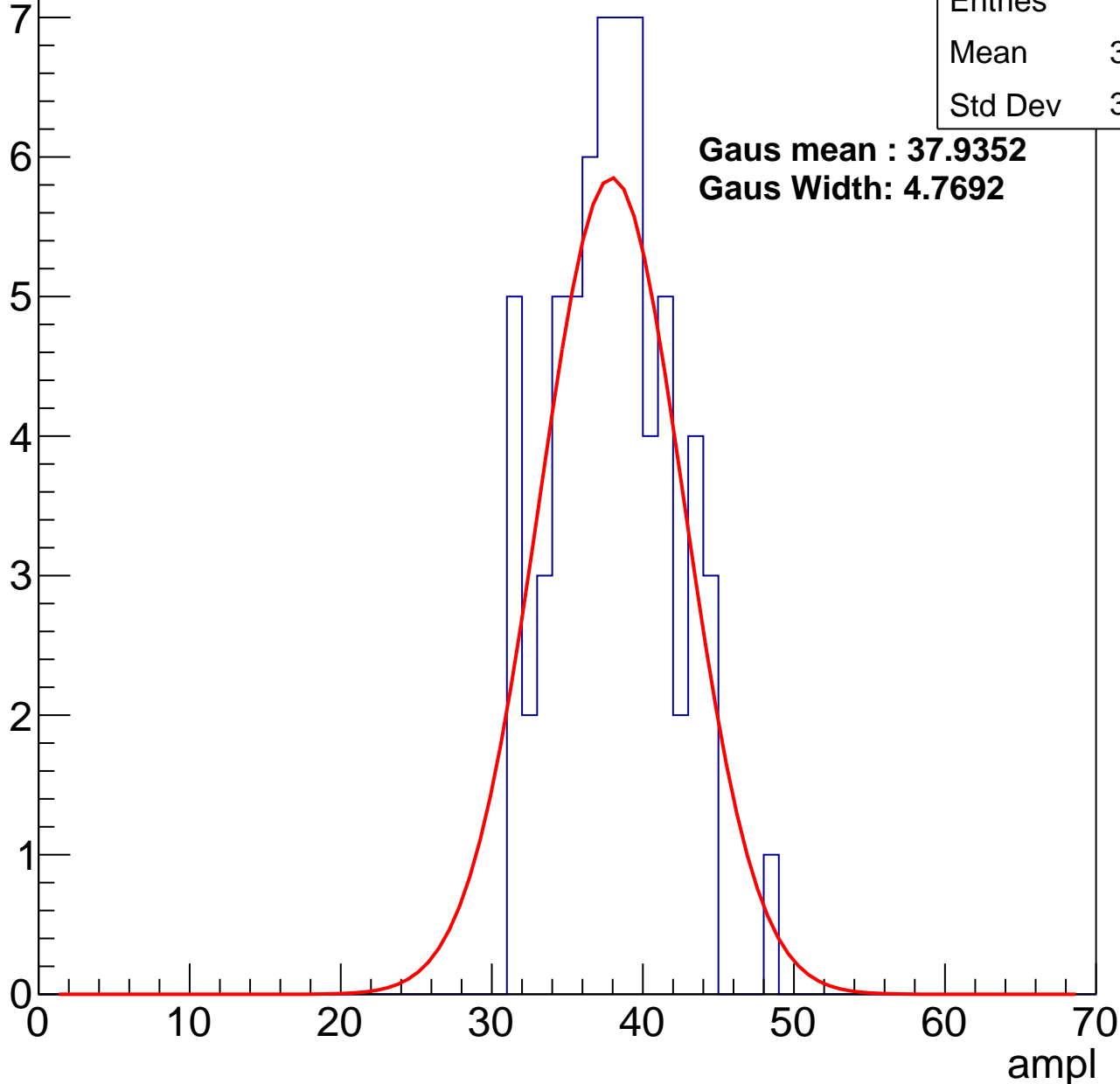
0 10 20 30 40 50 60 70



# B0L000S, U7-ch114, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch114, adc2

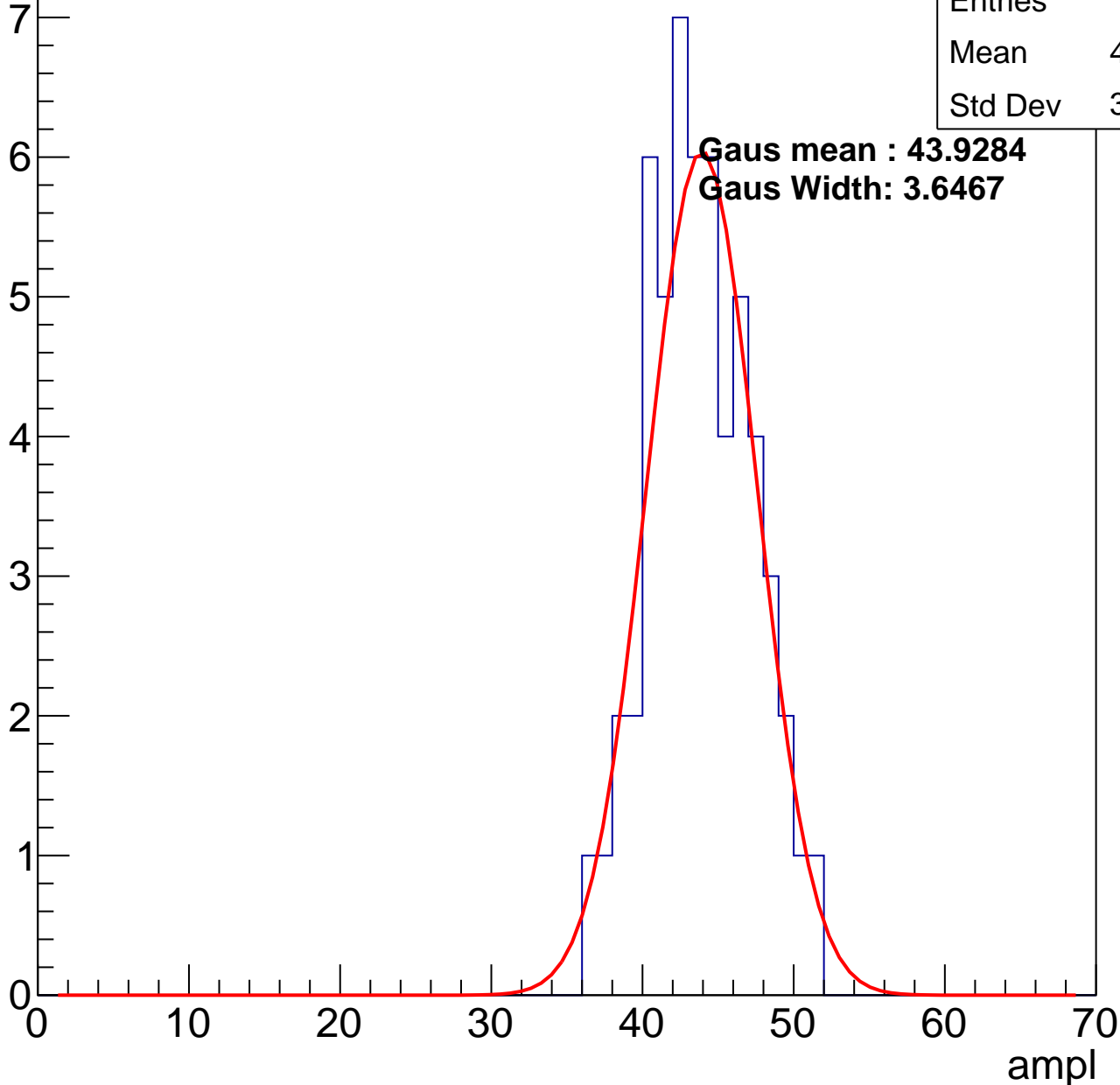
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	56
Mean	43.38
Std Dev	3.357

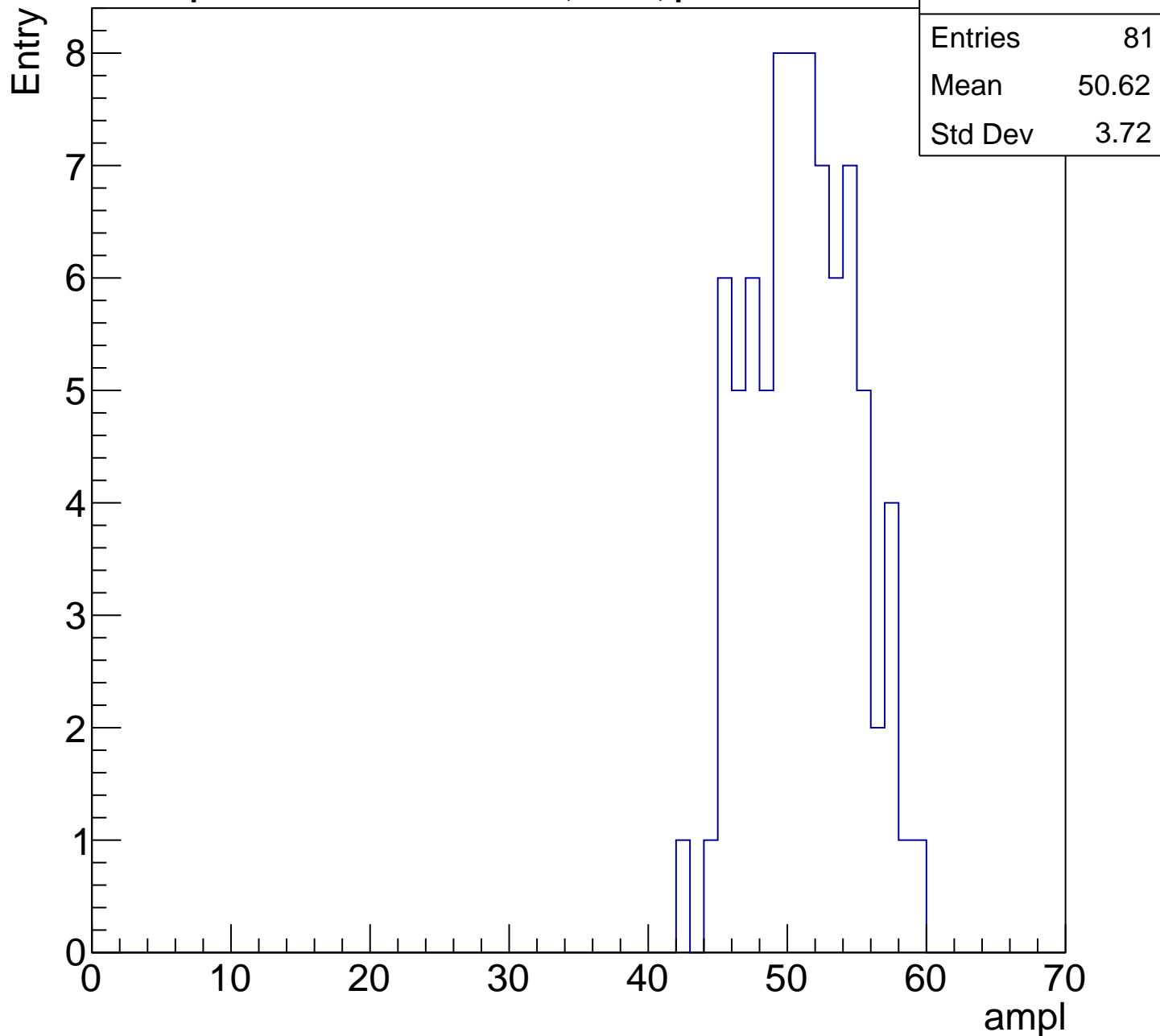
**Gaus mean : 43.9284**

**Gaus Width: 3.6467**



# B0L000S, U7-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

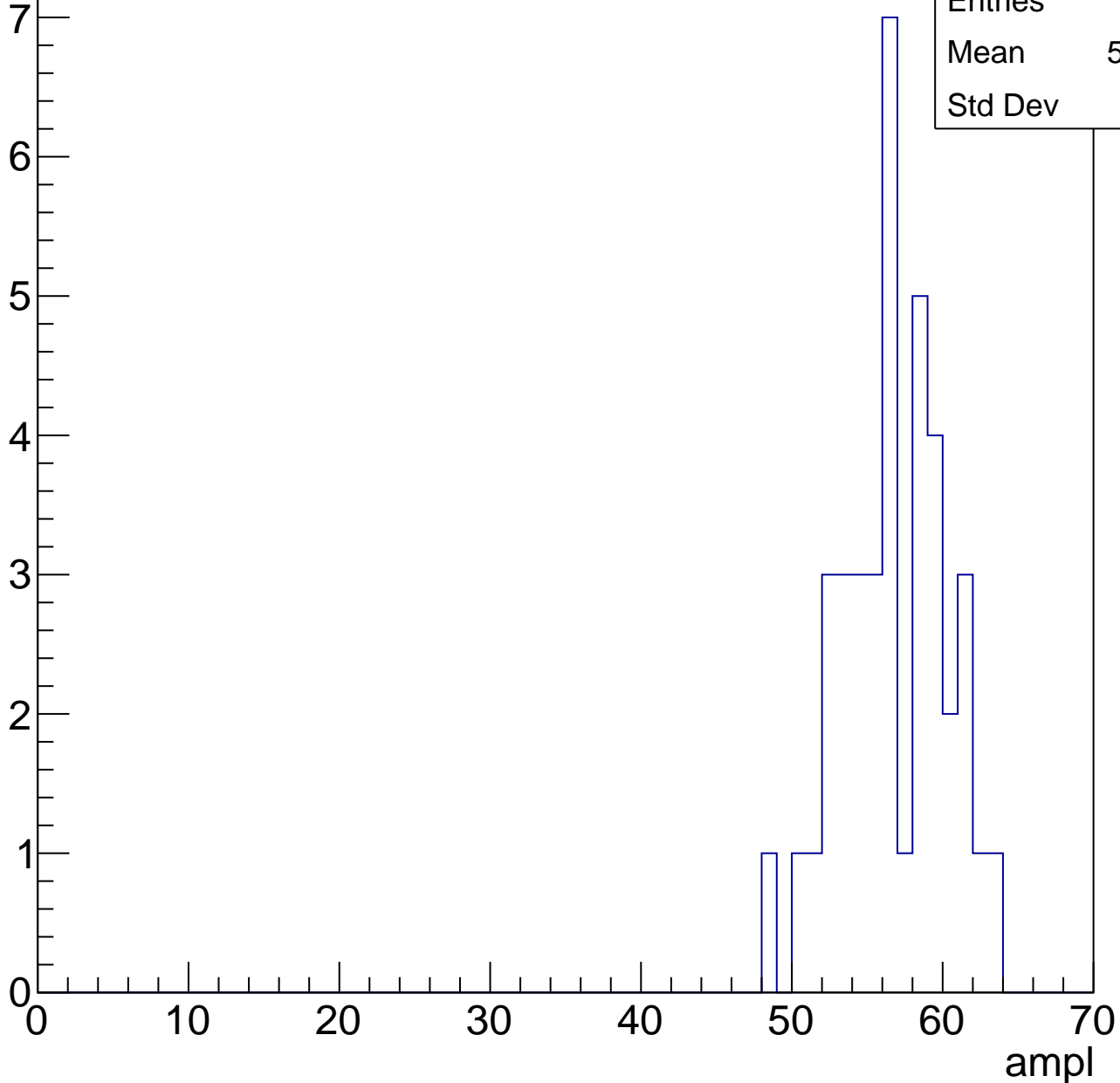


# B0L000S, U7-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

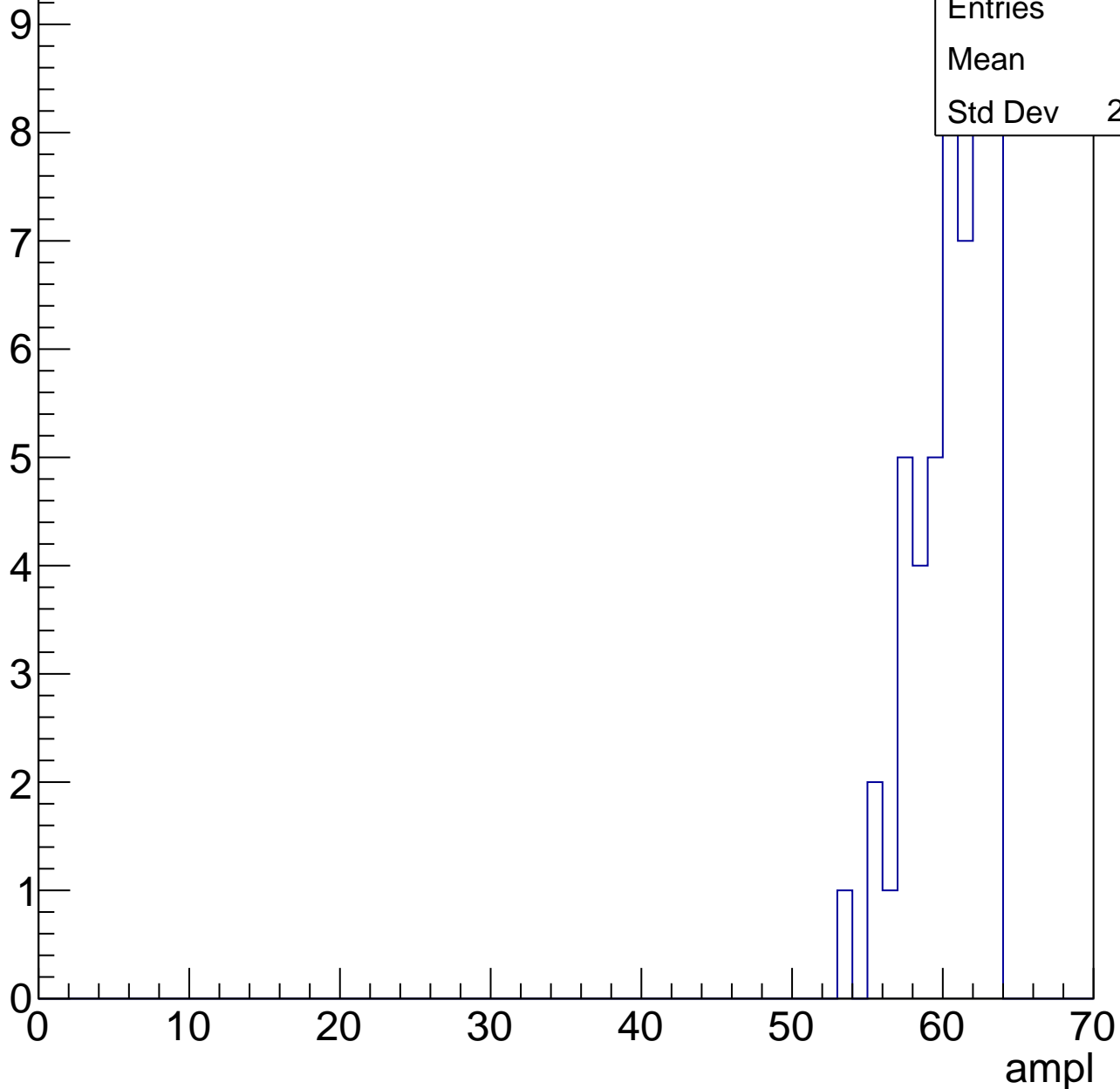
Entries	39
Mean	56.26
Std Dev	3.44



# B0L000S, U7-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

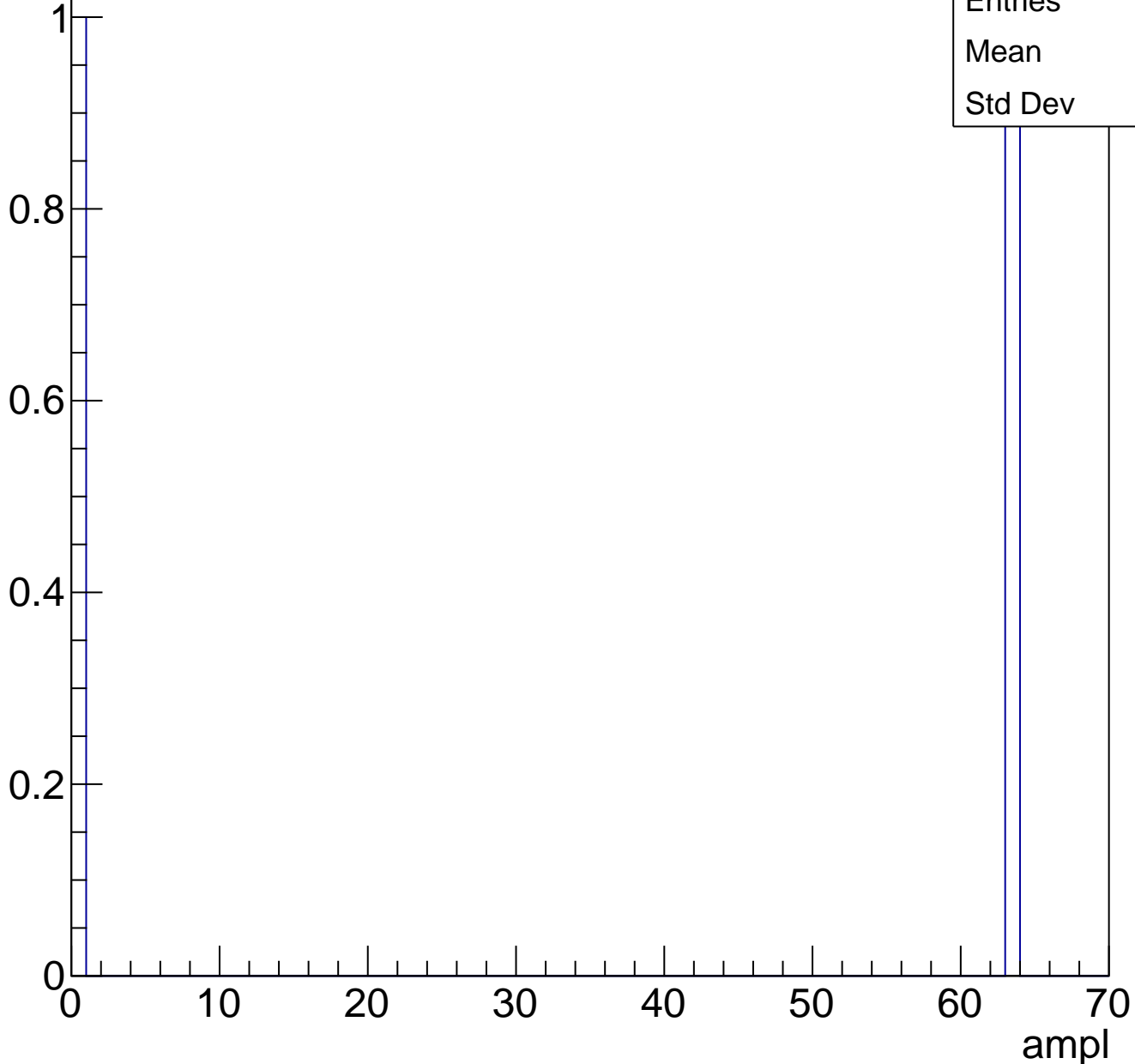
Entry



# B0L000S, U7-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	2
Mean	31.5
Std Dev	31.5



# B0L000S, U7-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	2
Mean	11
Std Dev	11

# B0L000S, U7-ch115, adc0

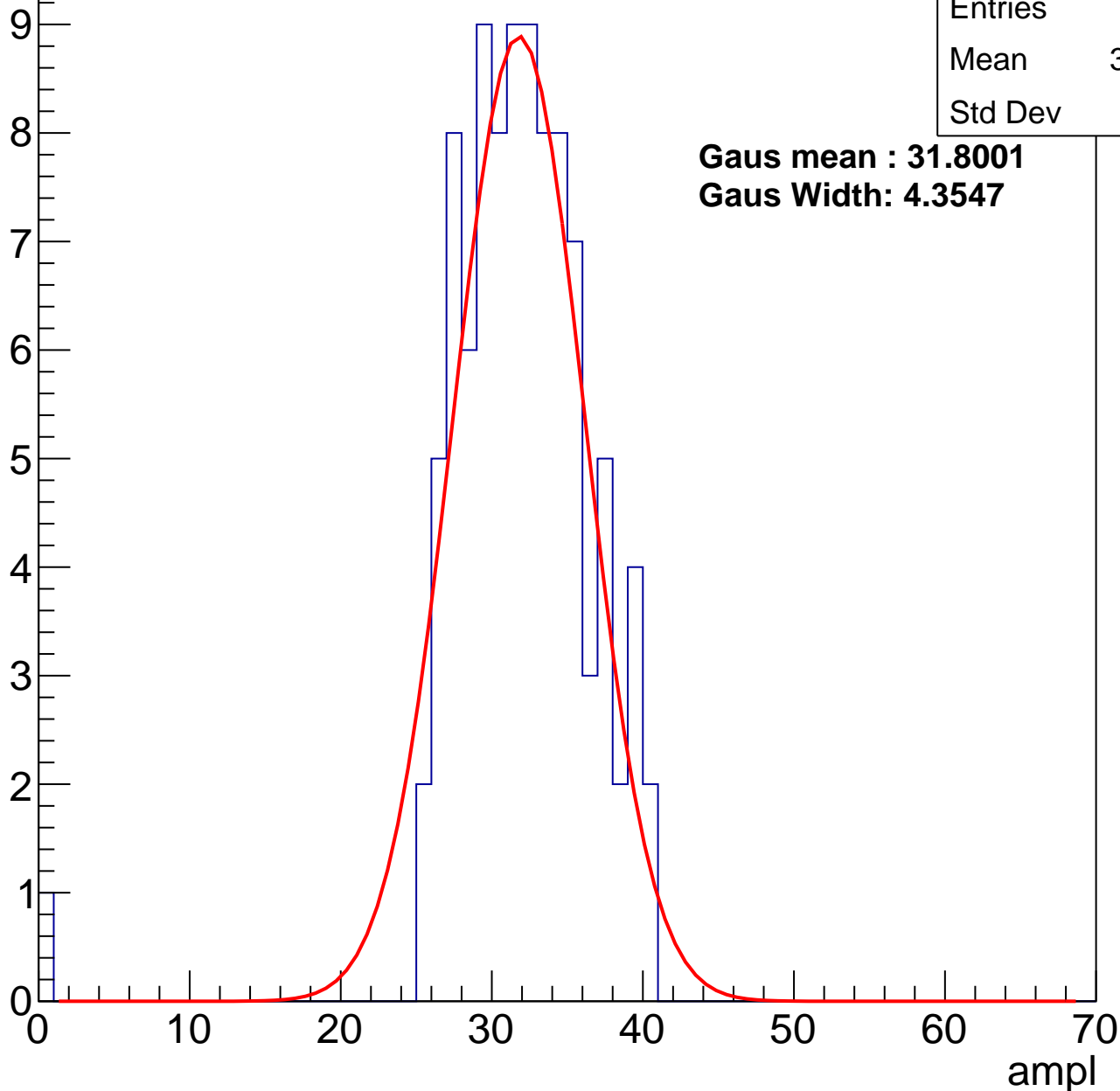
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	96
Mean	31.44
Std Dev	4.96

**Gaus mean : 31.8001**

**Gaus Width: 4.3547**



# B0L000S, U7-ch115, adc1

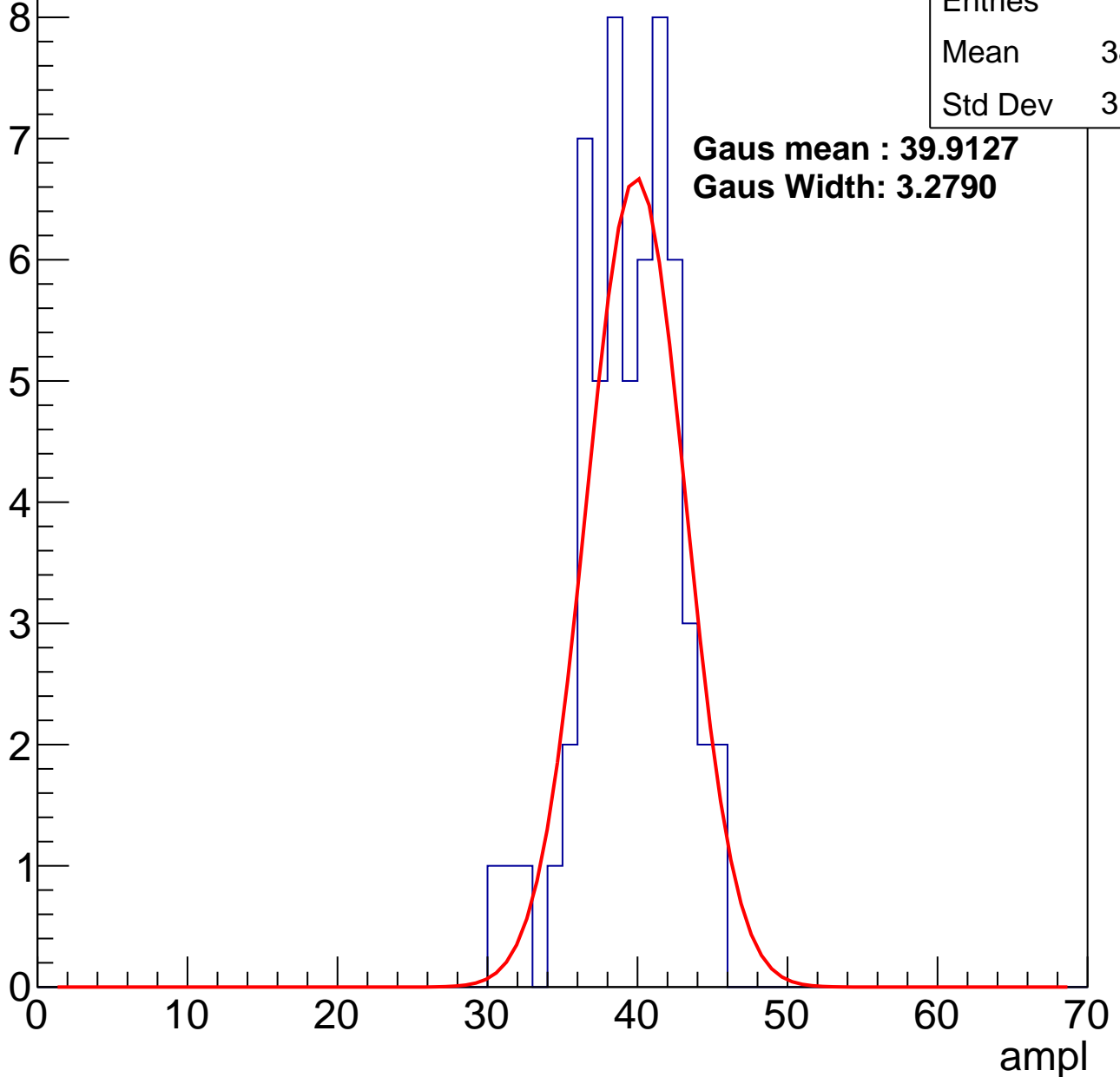
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	58
Mean	38.97
Std Dev	3.227

**Gaus mean : 39.9127**

**Gaus Width: 3.2790**



# B0L000S, U7-ch115, adc2

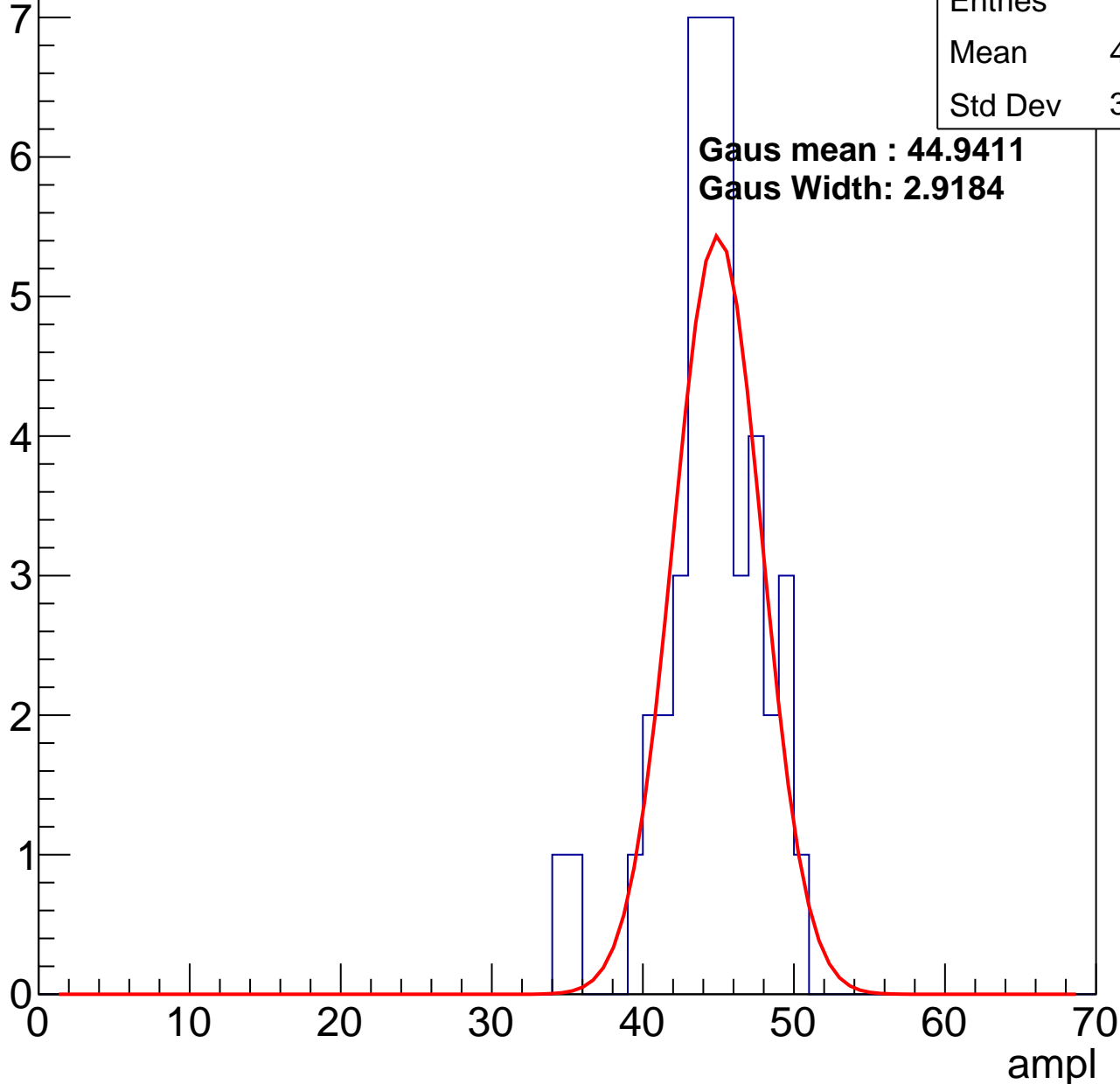
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	44
Mean	44.07
Std Dev	3.278

**Gaus mean : 44.9411**

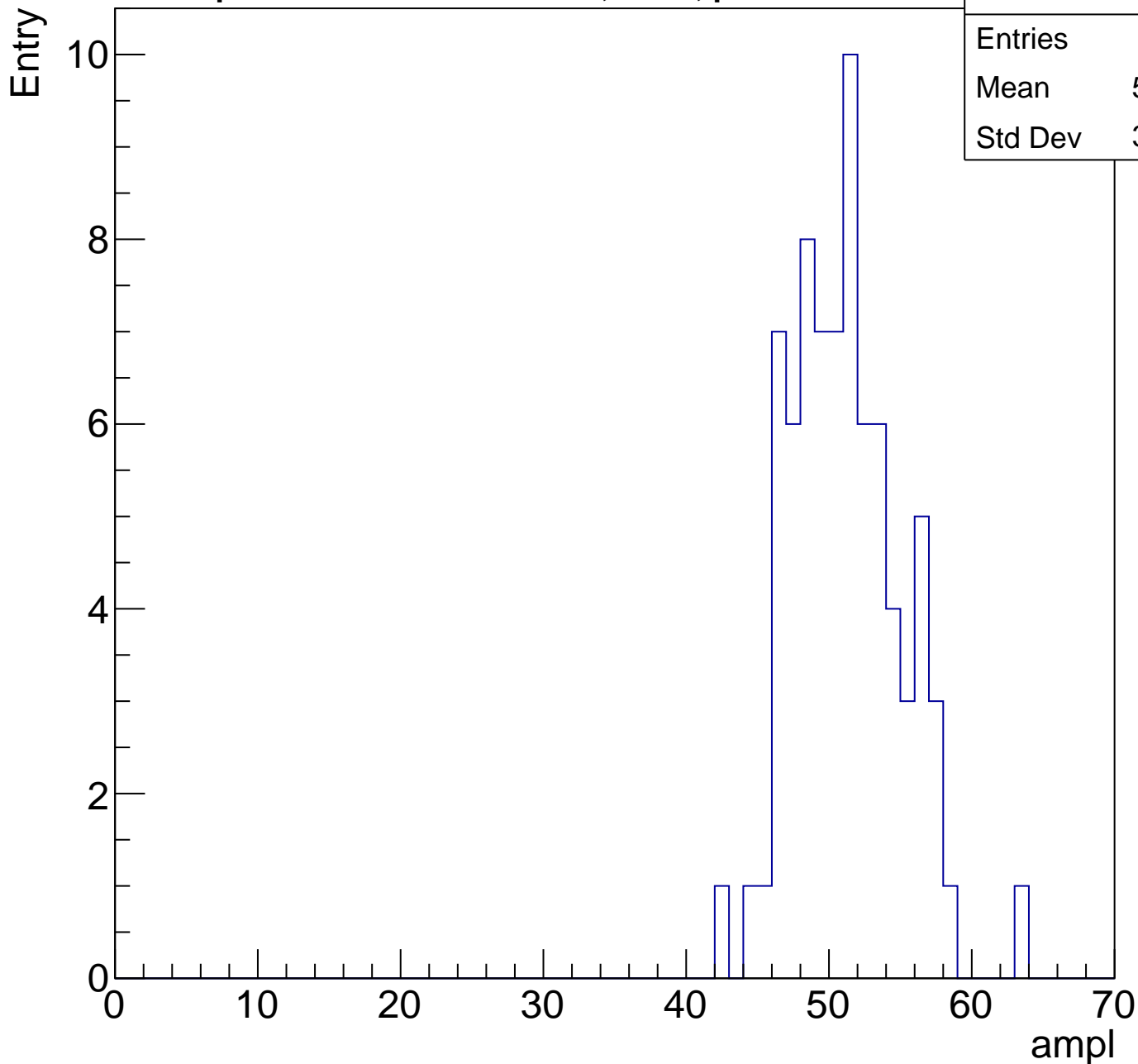
**Gaus Width: 2.9184**



# B0L000S, U7-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	77
Mean	50.71
Std Dev	3.741

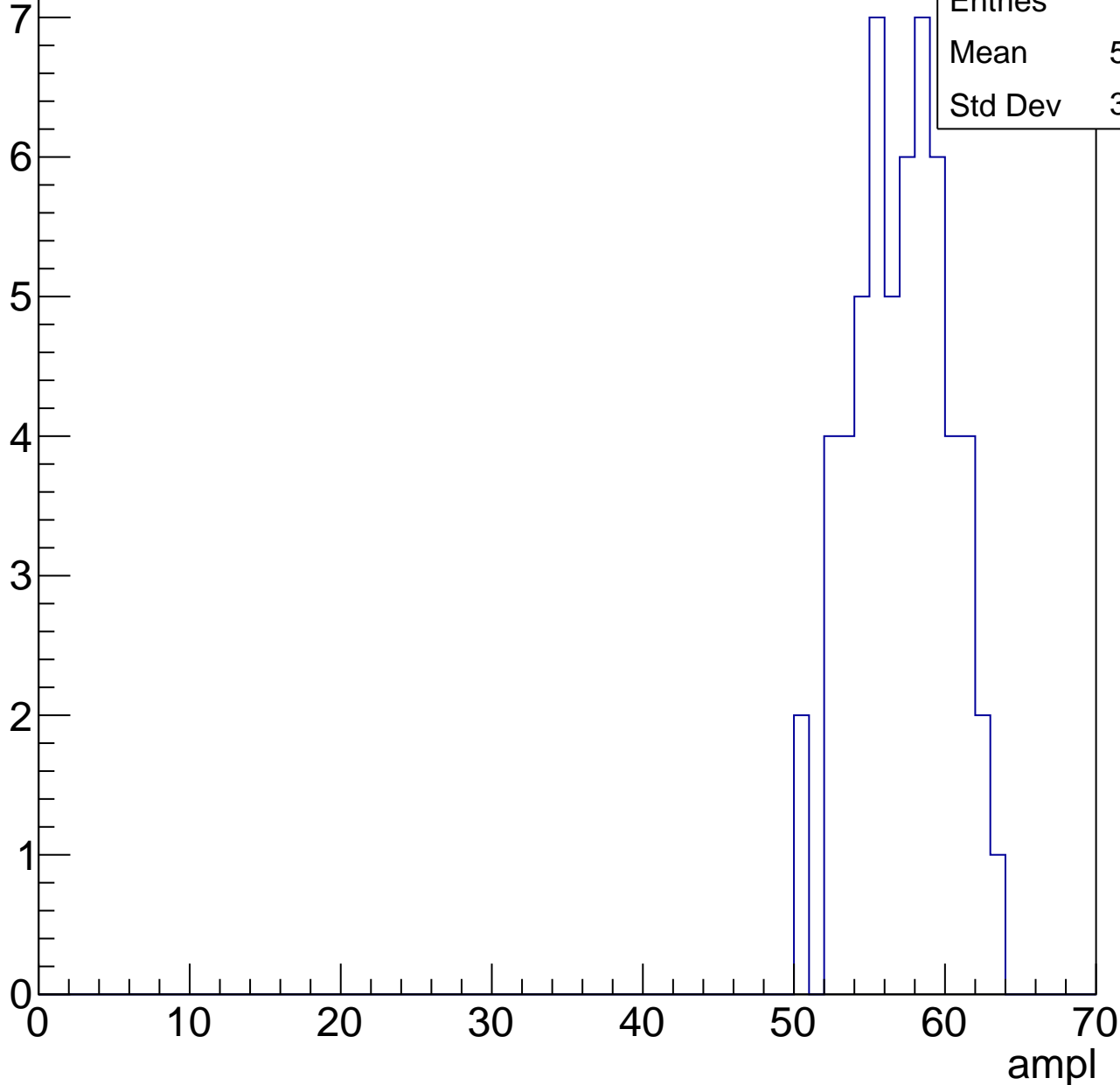


# B0L000S, U7-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	57
Mean	56.63
Std Dev	3.104

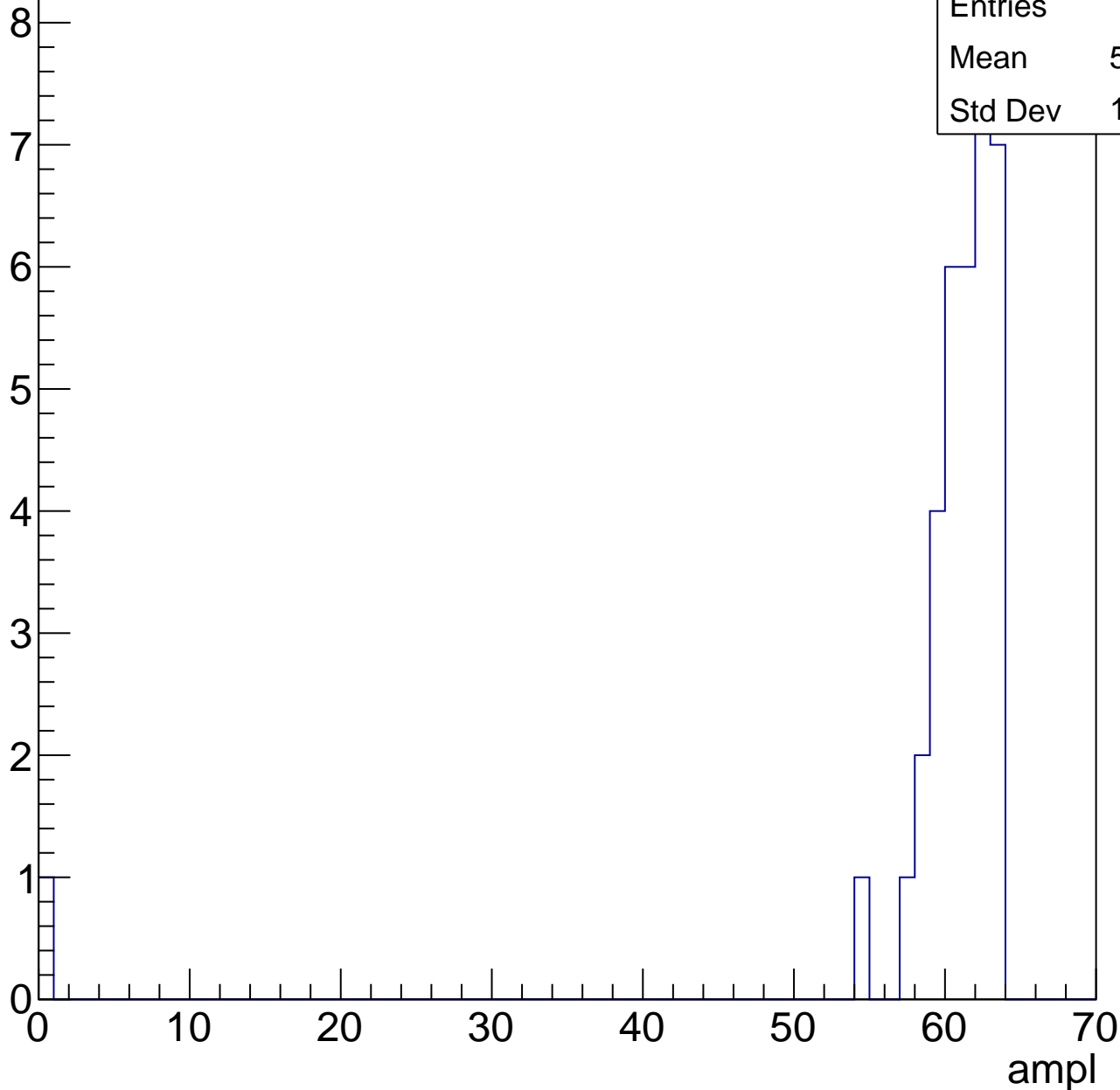


# B0L000S, U7-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	36
Mean	59.06
Std Dev	10.17



# B0L000S, U7-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L000S, U7-ch116, adc0

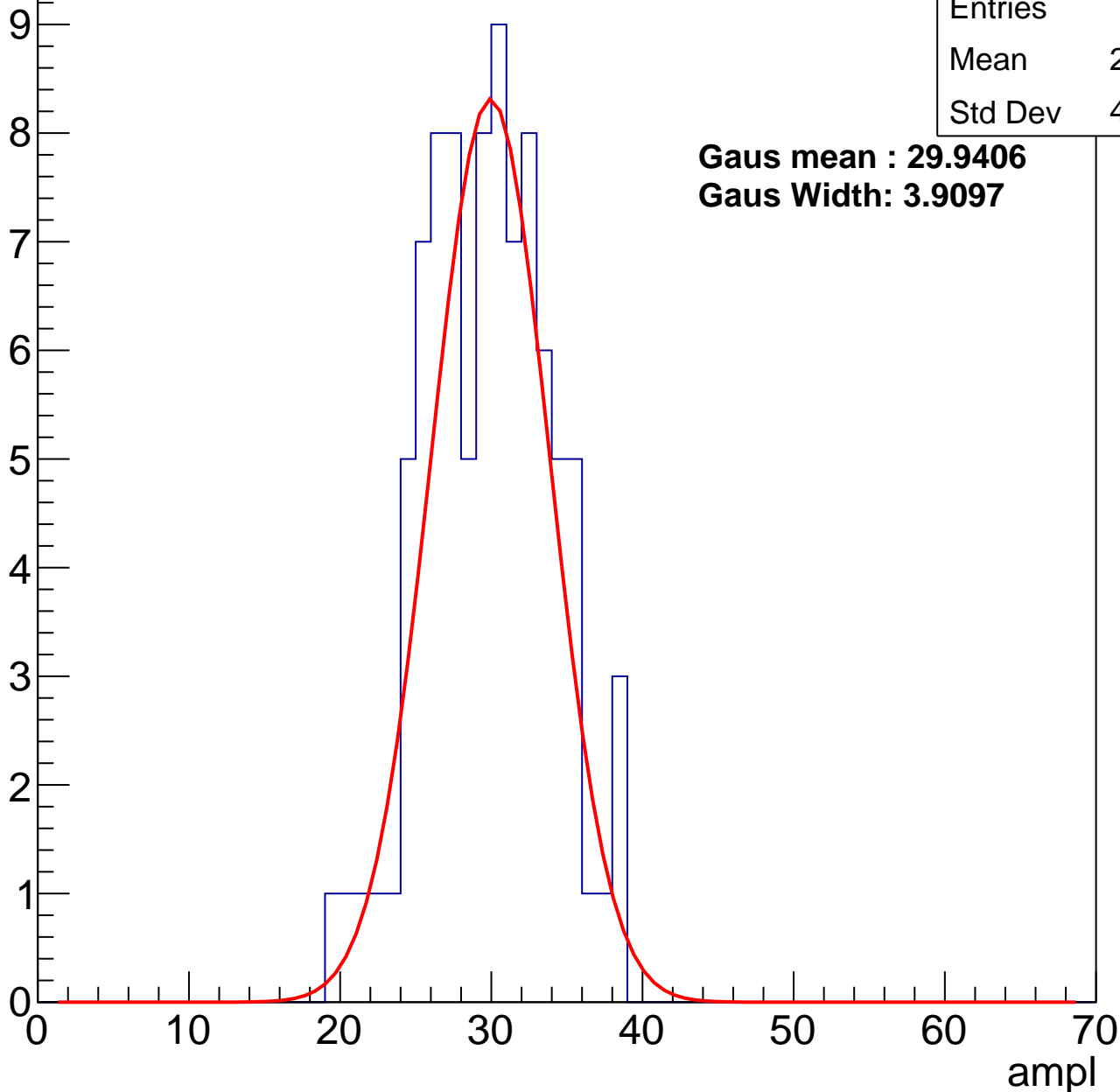
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	91
Mean	29.33
Std Dev	4.103

**Gaus mean : 29.9406**

**Gaus Width: 3.9097**



# B0L000S, U7-ch116, adc1

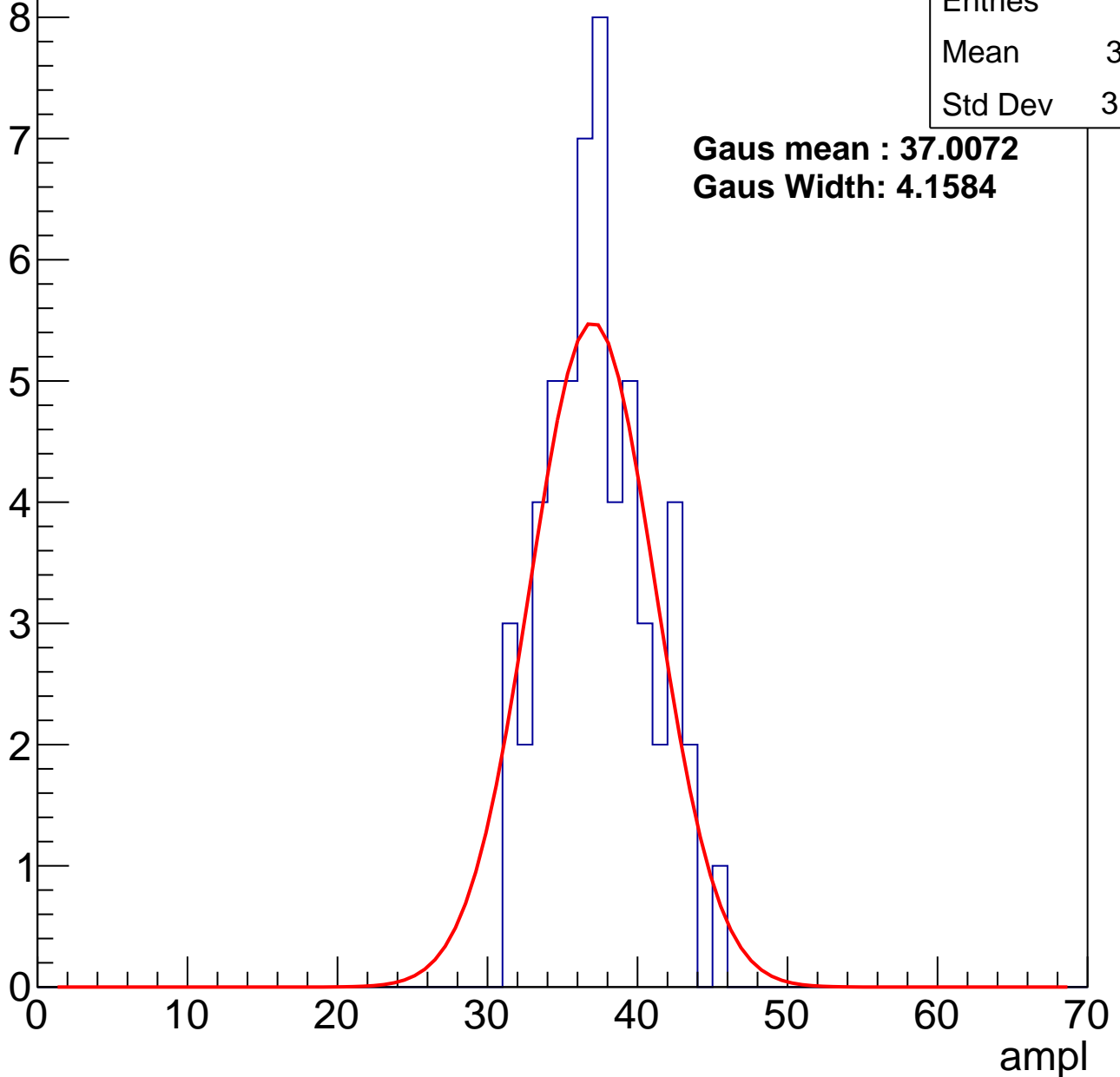
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	55
Mean	36.91
Std Dev	3.337

**Gaus mean : 37.0072**

**Gaus Width: 4.1584**



# B0L000S, U7-ch116, adc2

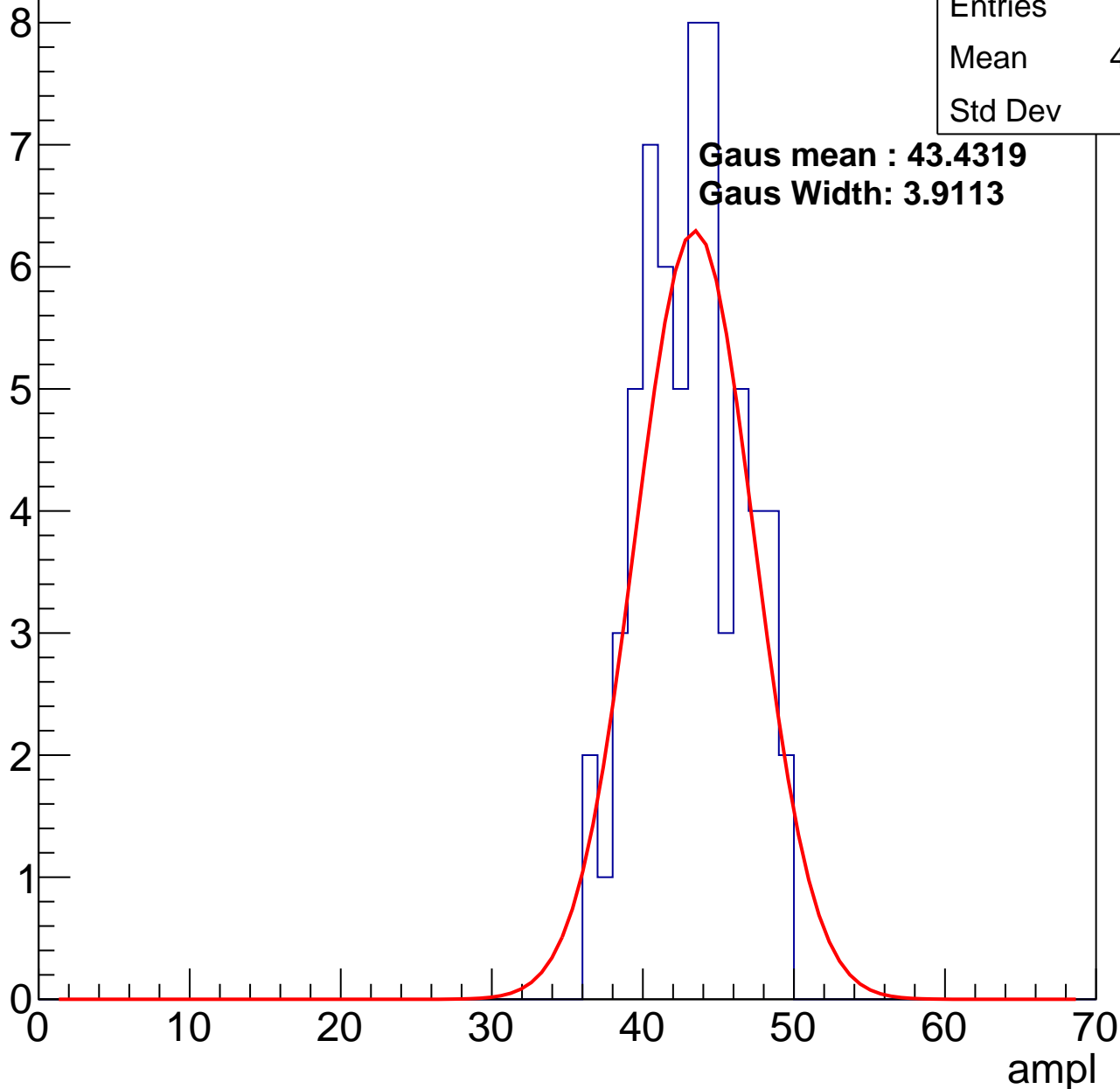
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	63
Mean	42.75
Std Dev	3.28

**Gaus mean : 43.4319**

**Gaus Width: 3.9113**

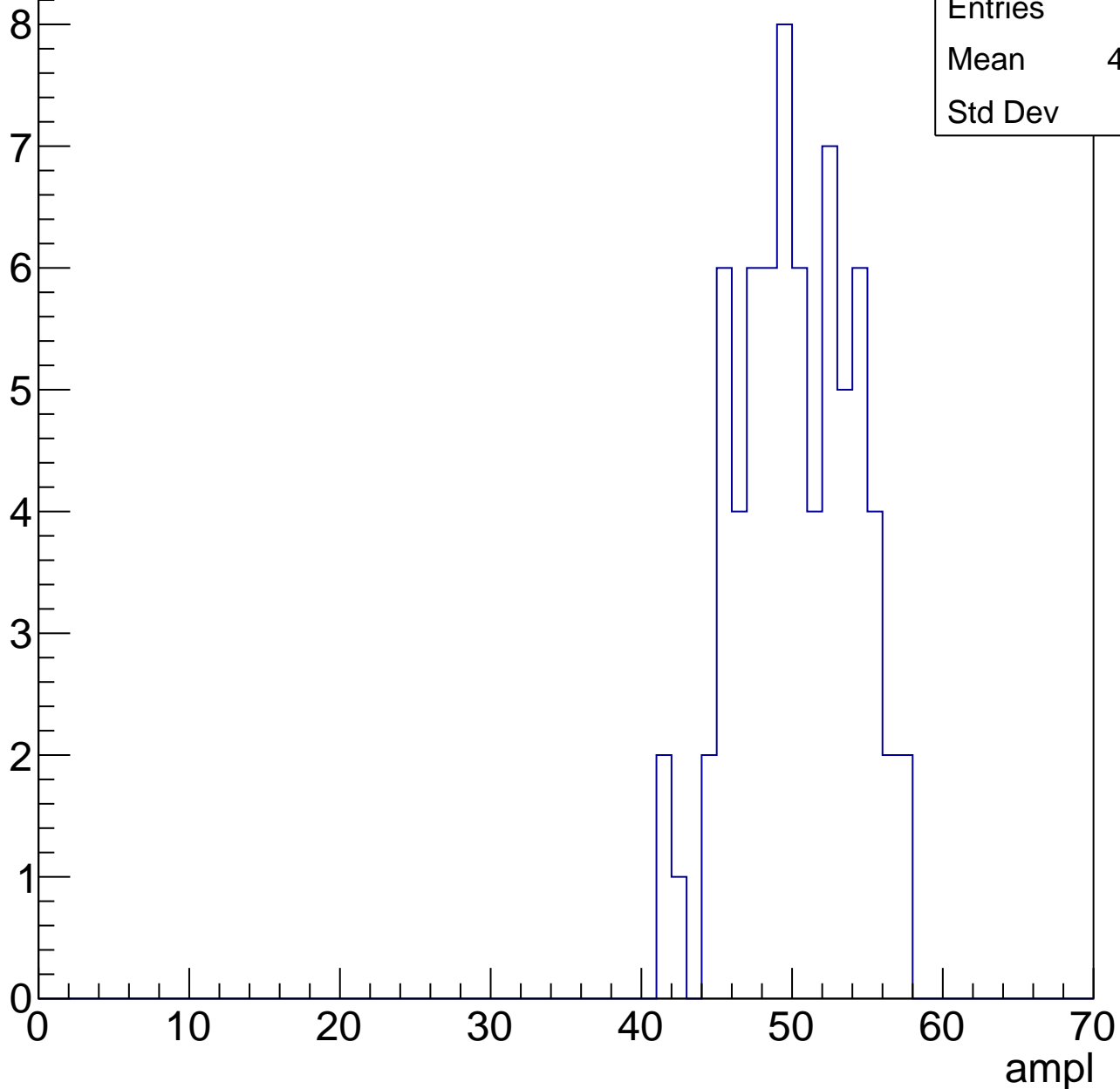


# B0L000S, U7-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	71
Mean	49.73
Std Dev	3.82

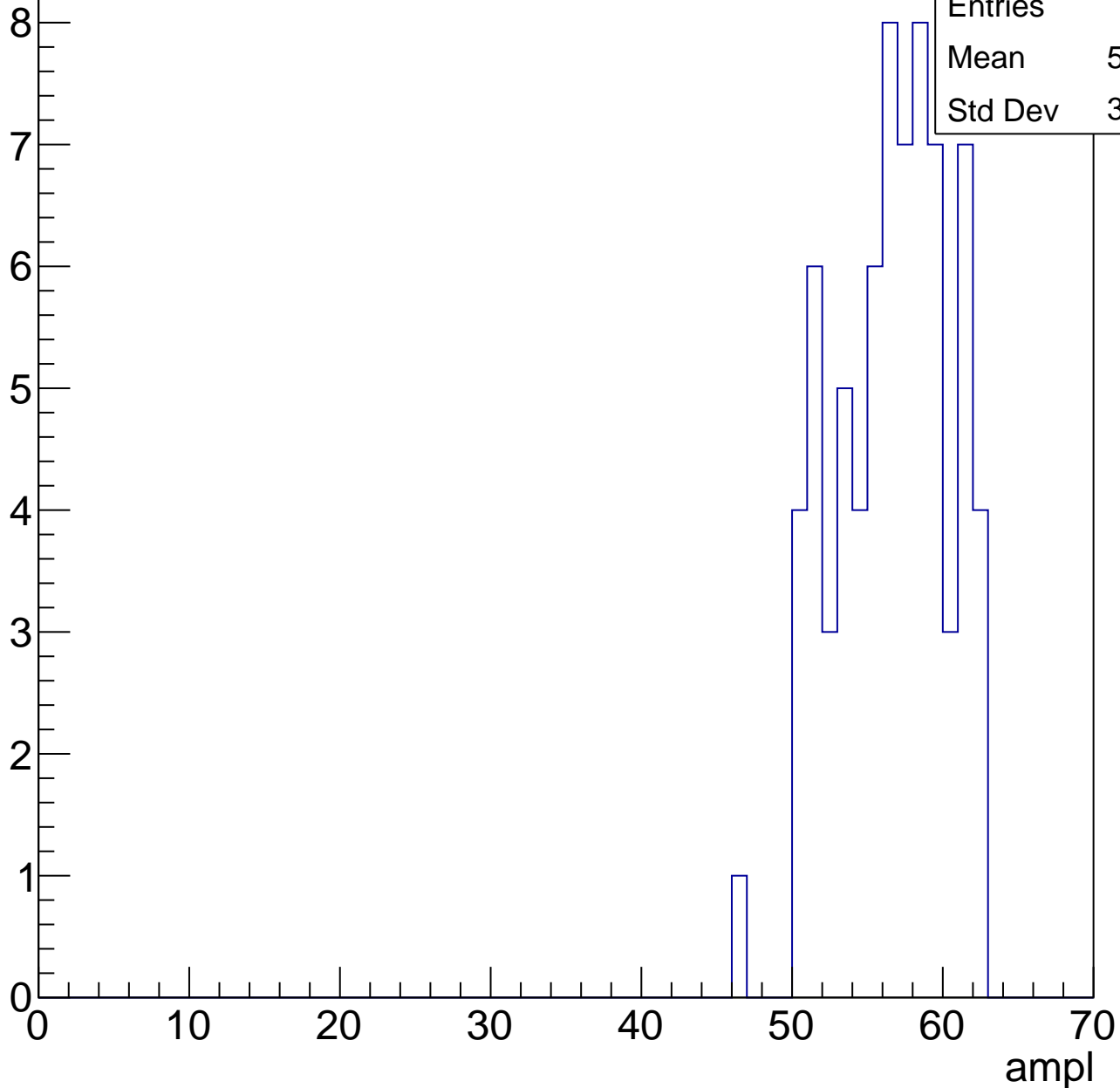


# B0L000S, U7-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	73
Mean	56.14
Std Dev	3.658

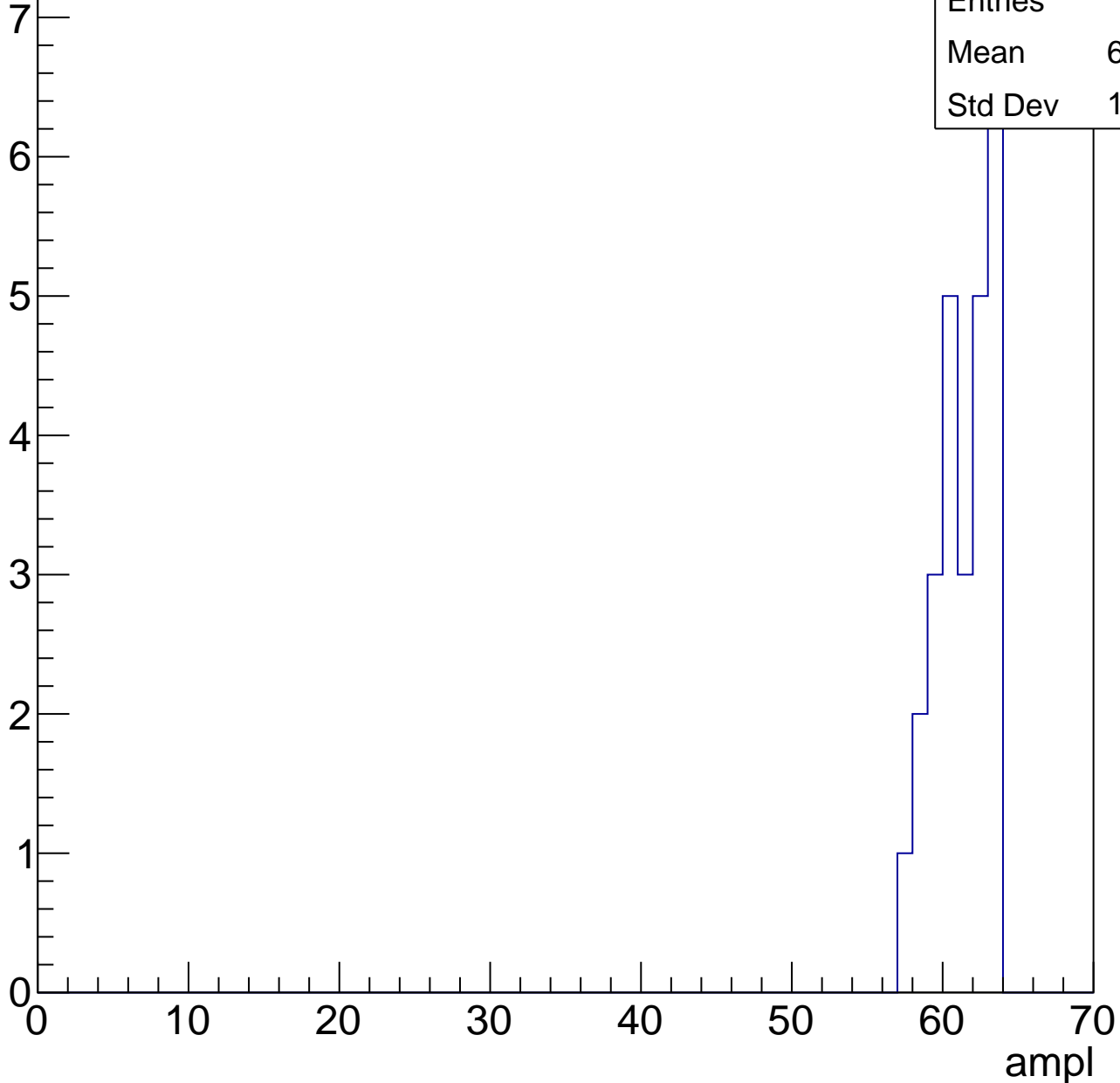


# B0L000S, U7-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	26
Mean	60.92
Std Dev	1.796



# B0L000S, U7-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

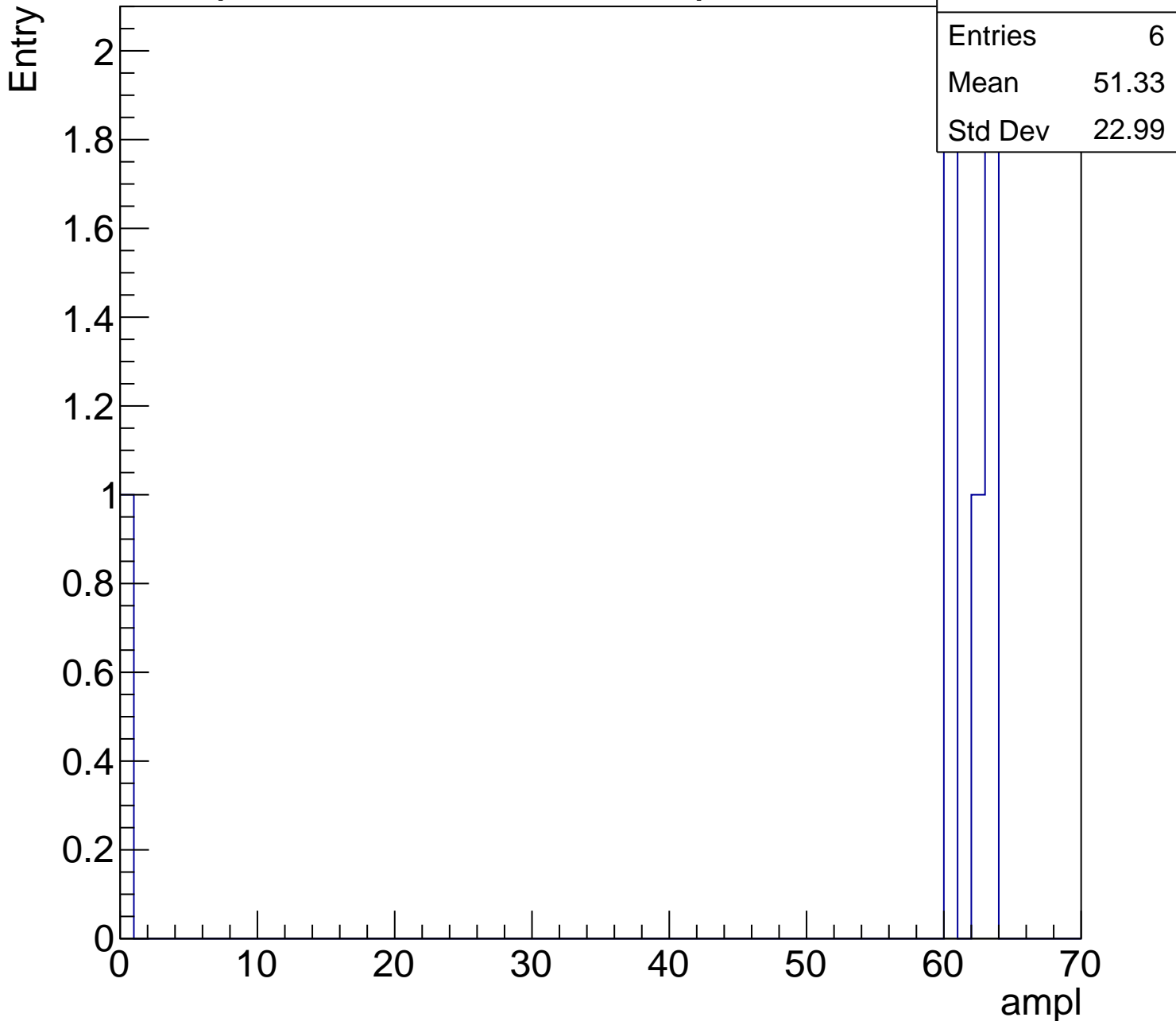
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	51.33
Std Dev	22.99

0 10 20 30 40 50 60 70

ampl





# B0L000S, U7-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch117, adc0

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	76
Mean	29.46
Std Dev	3.27

**Gaus mean : 29.6974**

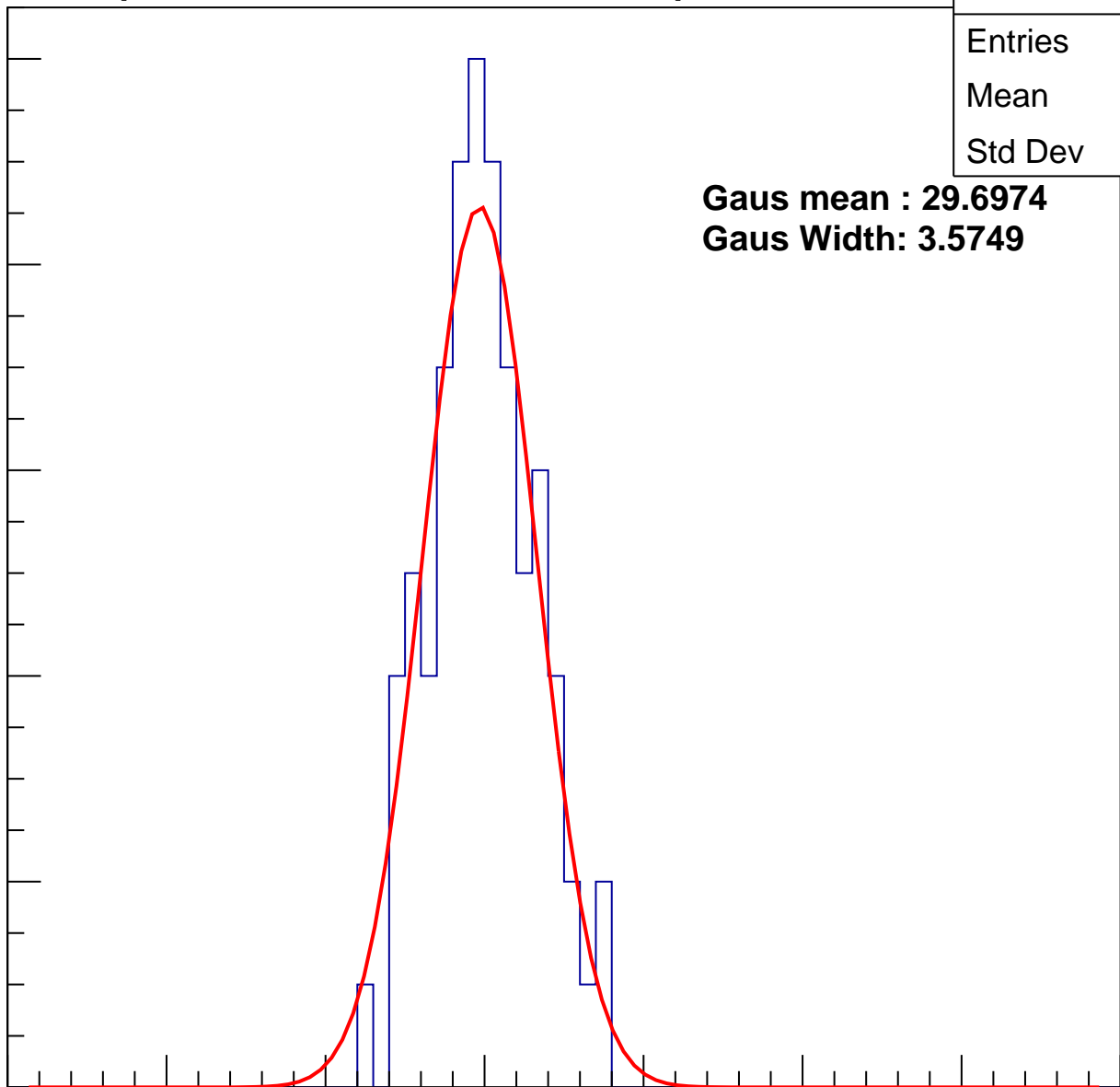
**Gaus Width: 3.5749**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L000S, U7-ch117, adc1

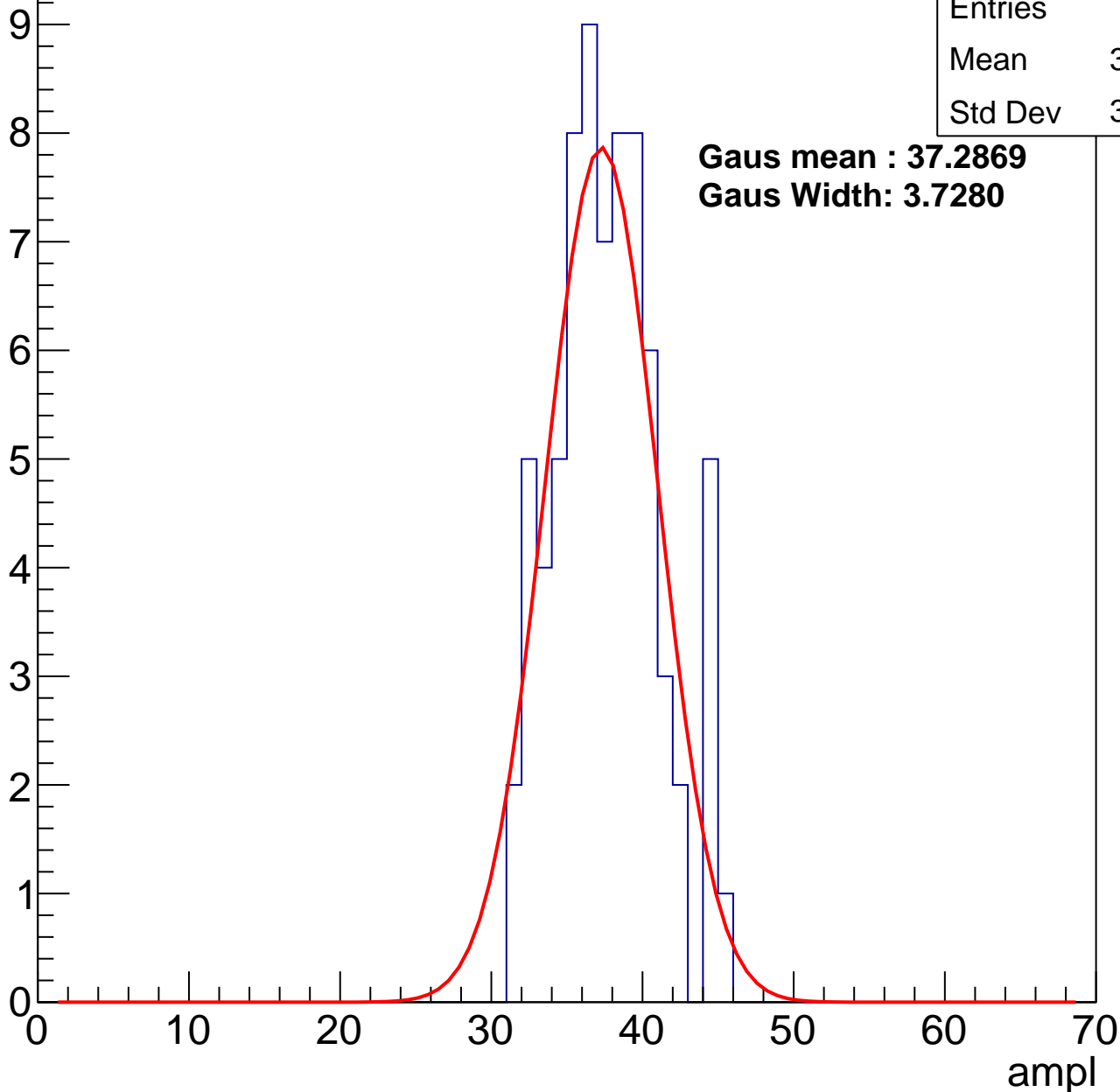
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	73
Mean	37.19
Std Dev	3.403

**Gaus mean : 37.2869**

**Gaus Width: 3.7280**



# B0L000S, U7-ch117, adc2

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	60
Mean	43.42
Std Dev	3.358

**Gaus mean : 43.2916**

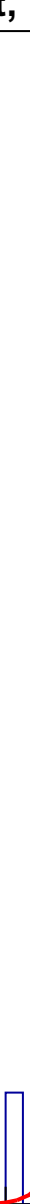
**Gaus Width: 2.6463**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

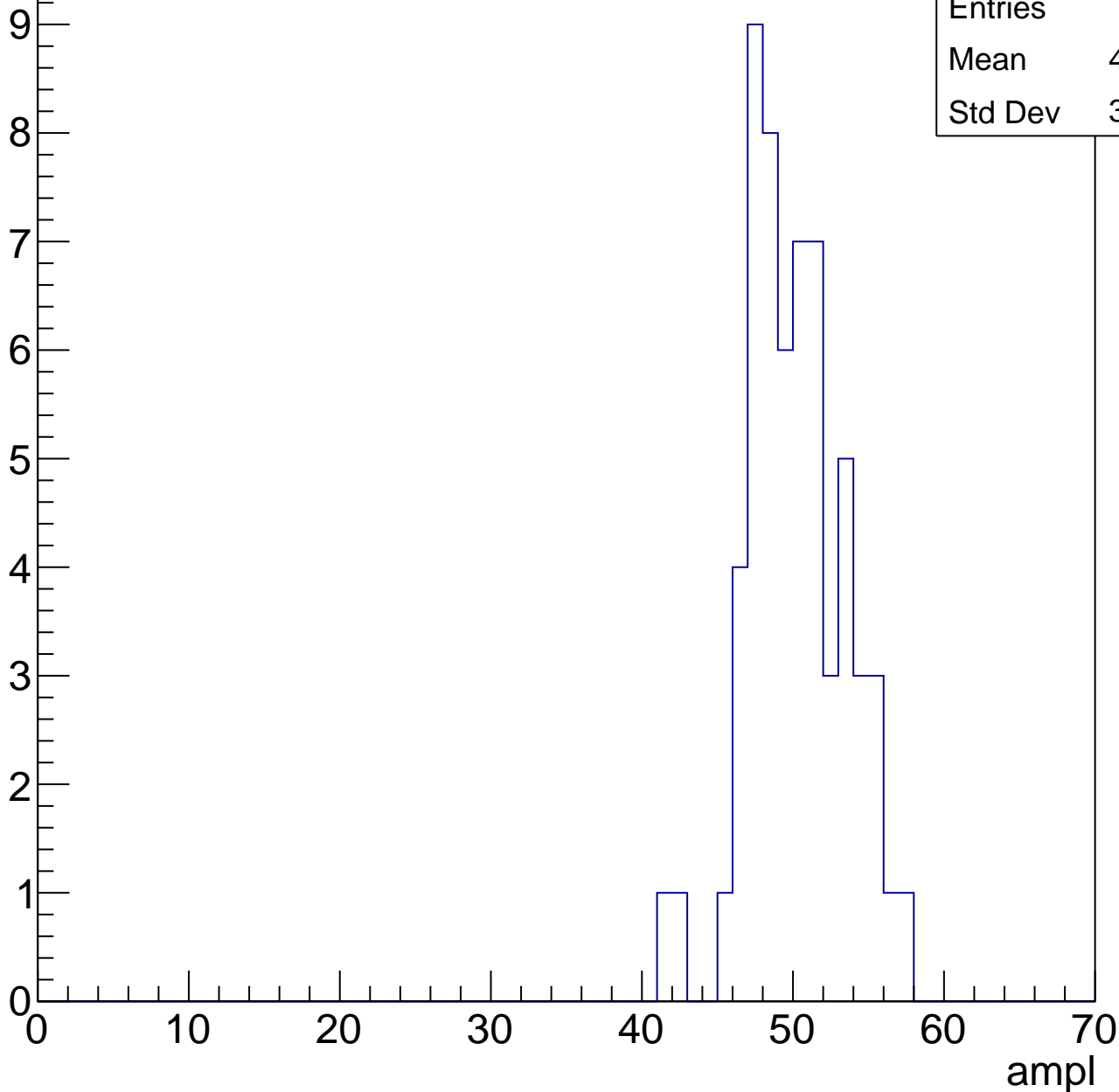


# B0L000S, U7-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	60
Mean	49.68
Std Dev	3.212

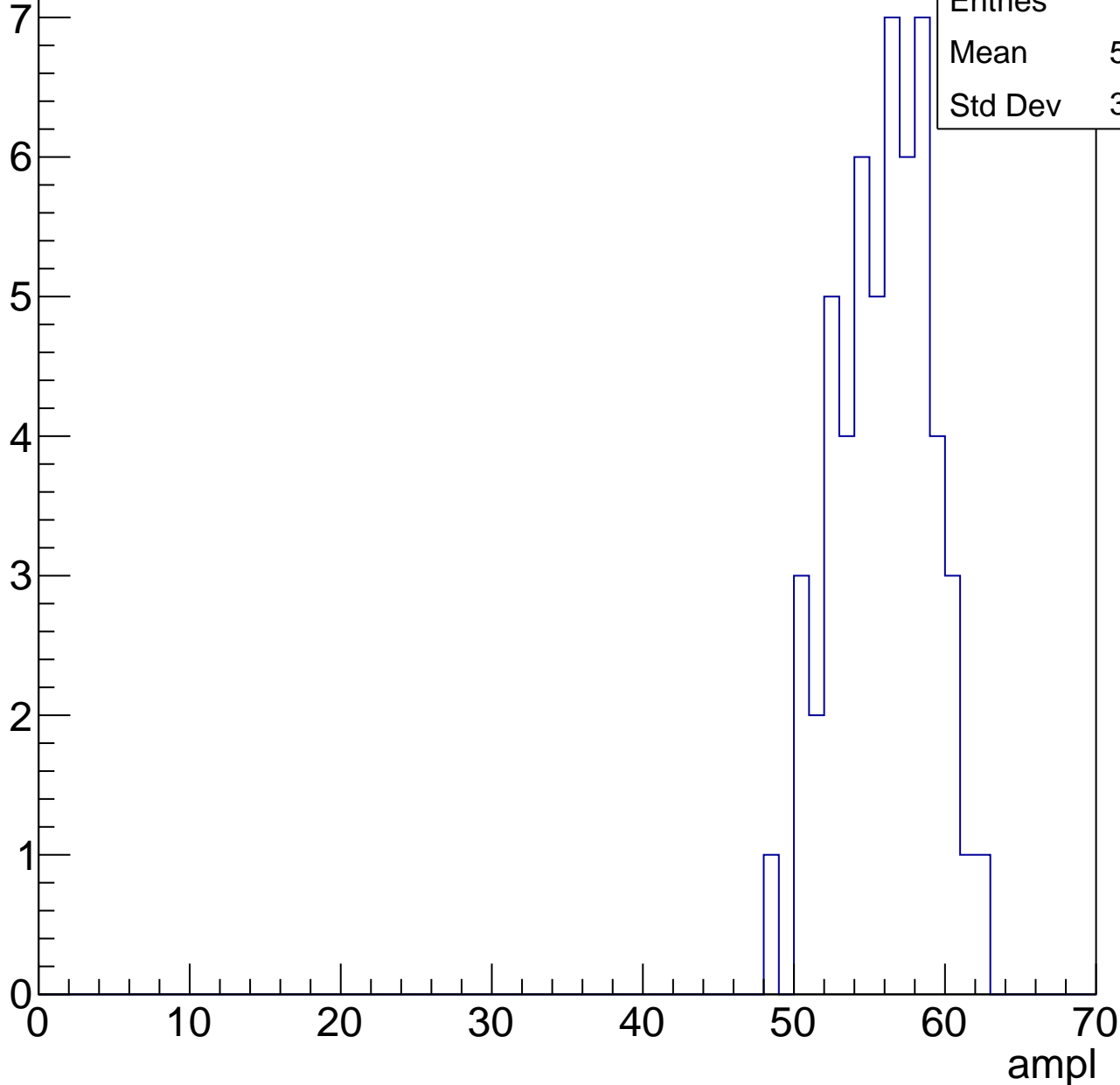


# B0L000S, U7-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	55
Mean	55.45
Std Dev	3.103



# B0L000S, U7-ch117, adc5

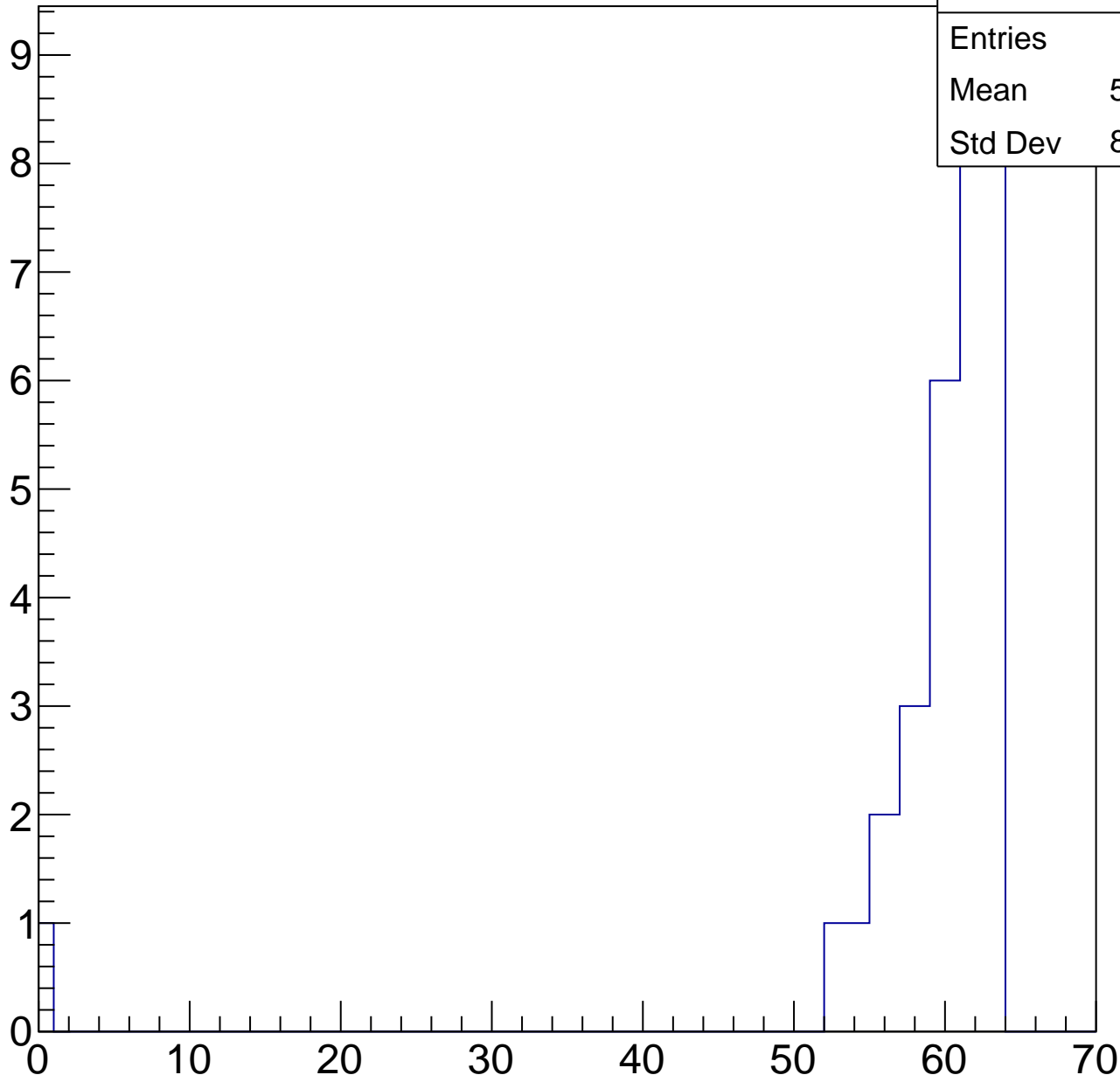
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	52
Mean	58.67
Std Dev	8.662

ampl



# B0L000S, U7-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L000S, U7-ch118, adc0

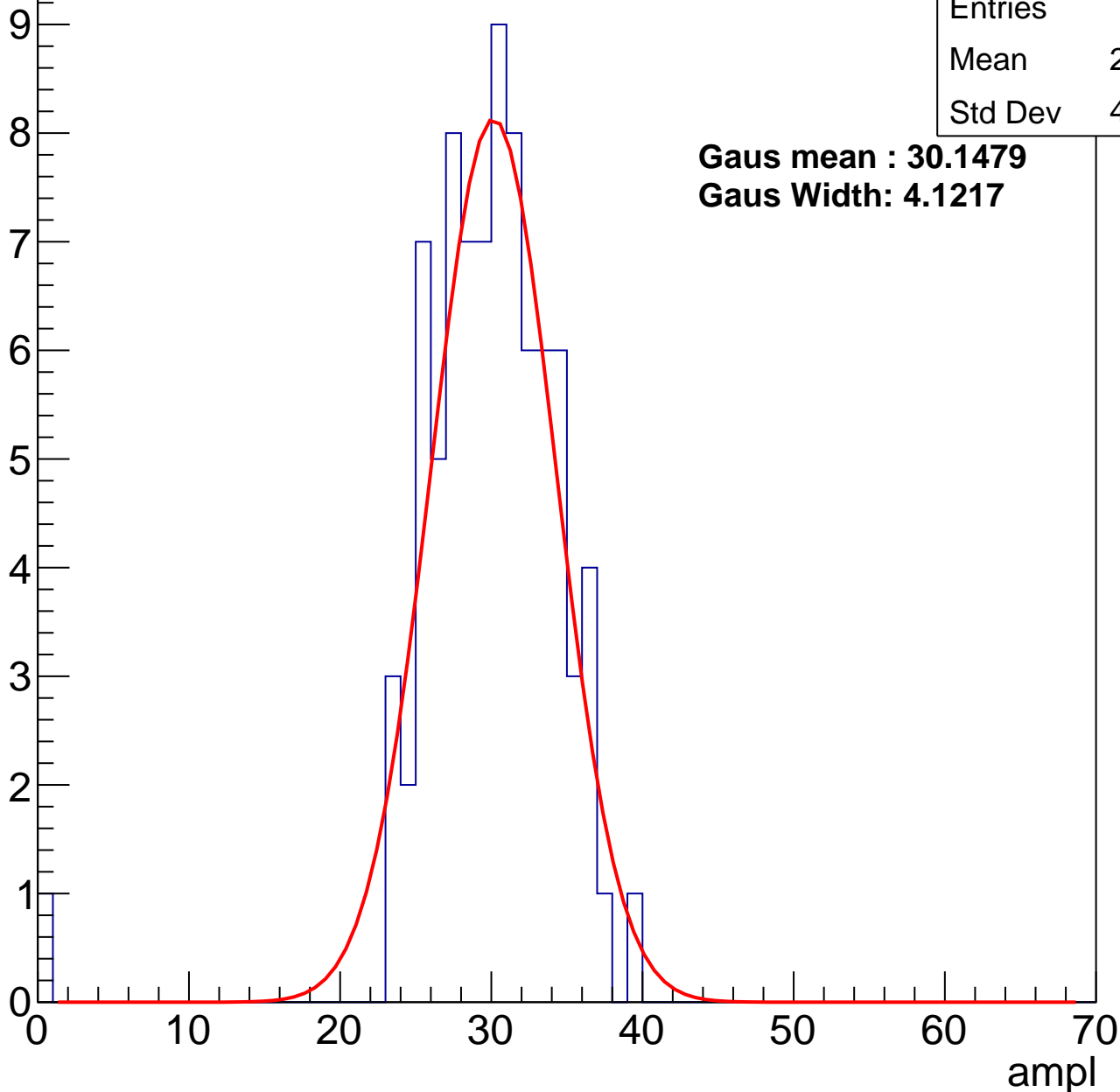
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	84
Mean	29.45
Std Dev	4.863

**Gaus mean : 30.1479**

**Gaus Width: 4.1217**



# B0L000S, U7-ch118, adc1

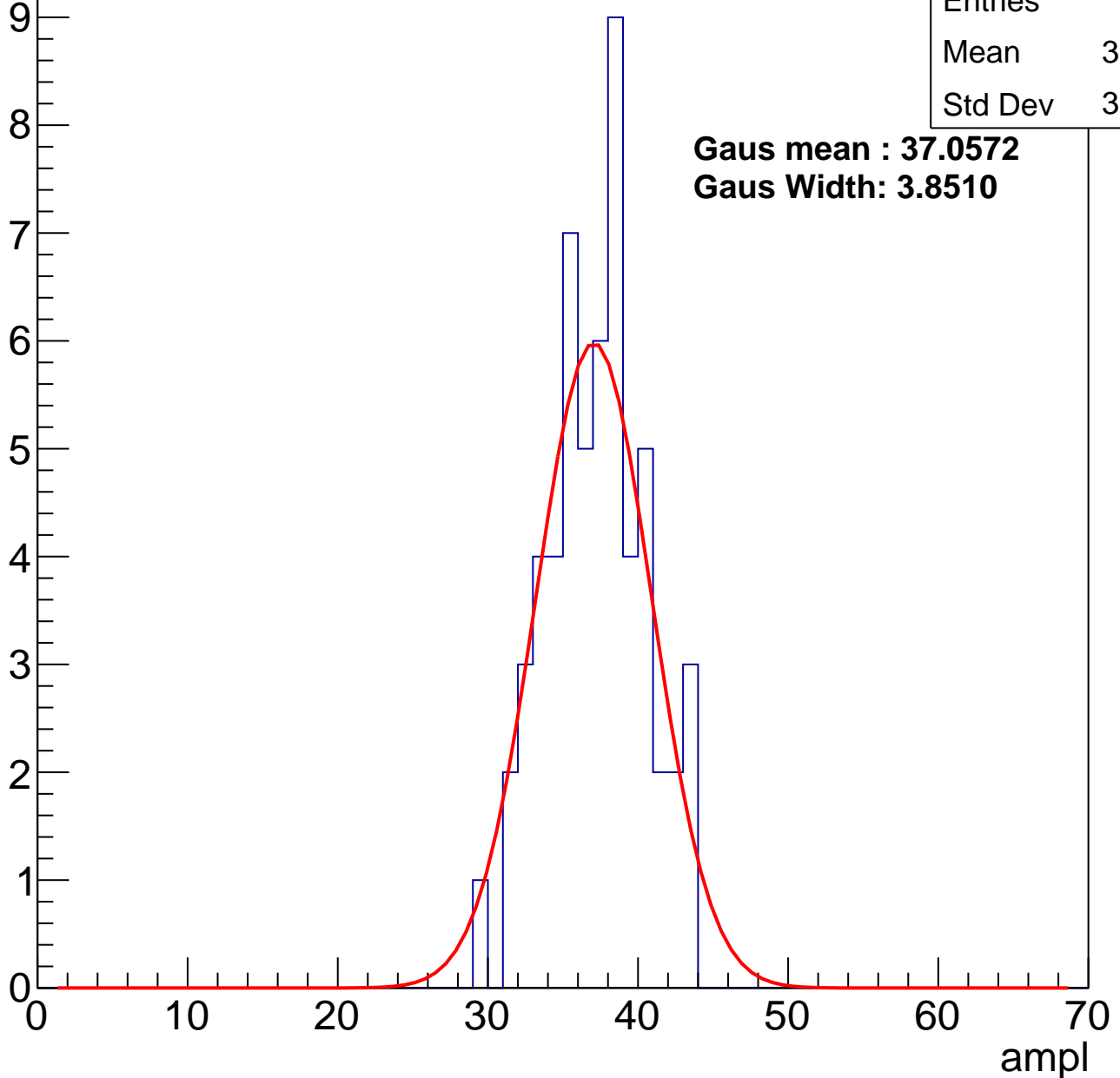
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	57
Mean	36.75
Std Dev	3.246

**Gaus mean : 37.0572**

**Gaus Width: 3.8510**



# B0L000S, U7-ch118, adc2

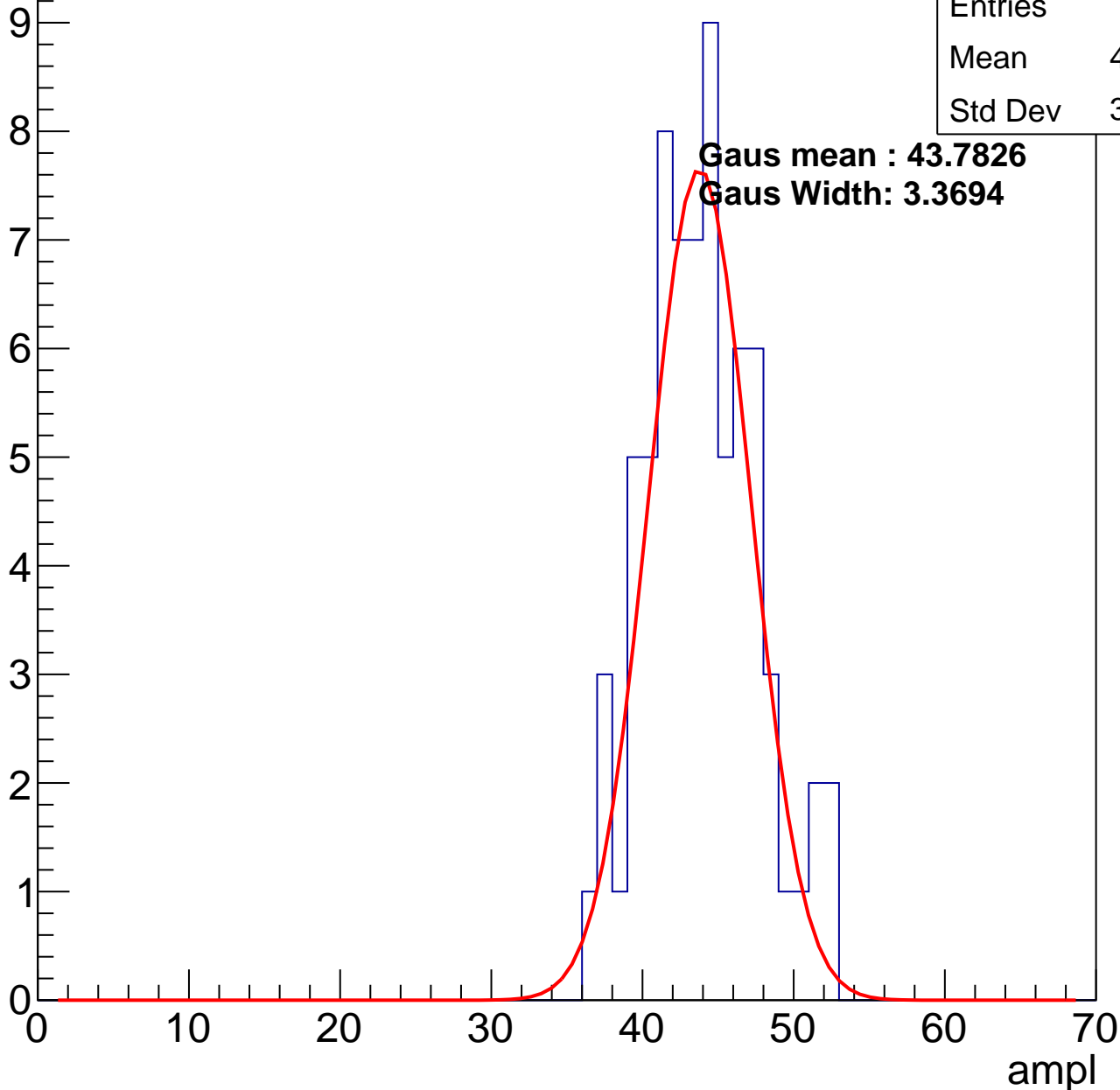
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	72
Mean	43.49
Std Dev	3.648

**Gaus mean : 43.7826**

**Gaus Width: 3.3694**

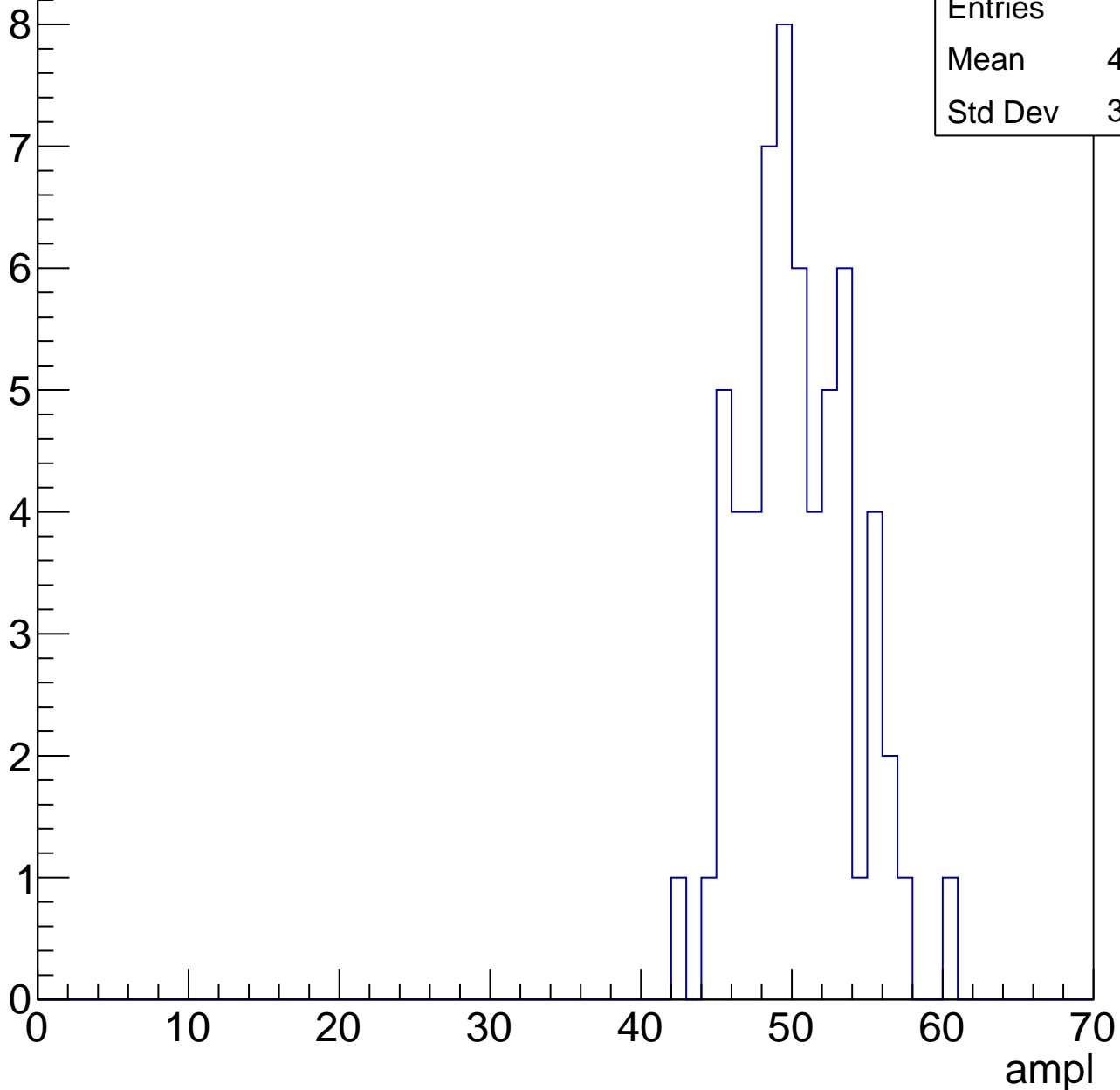


# B0L000S, U7-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	60
Mean	49.93
Std Dev	3.596

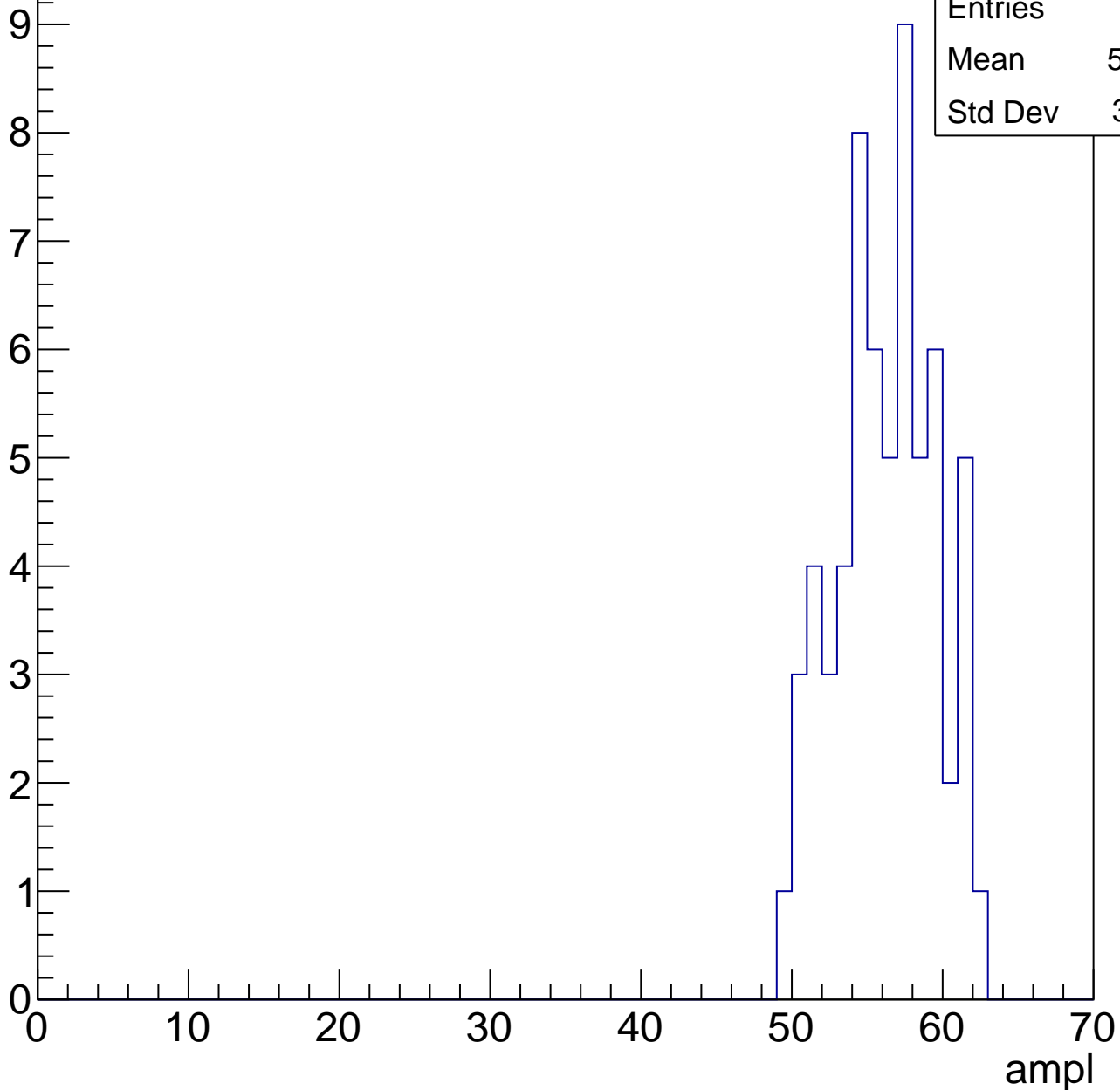


# B0L000S, U7-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	62
Mean	55.76
Std Dev	3.241

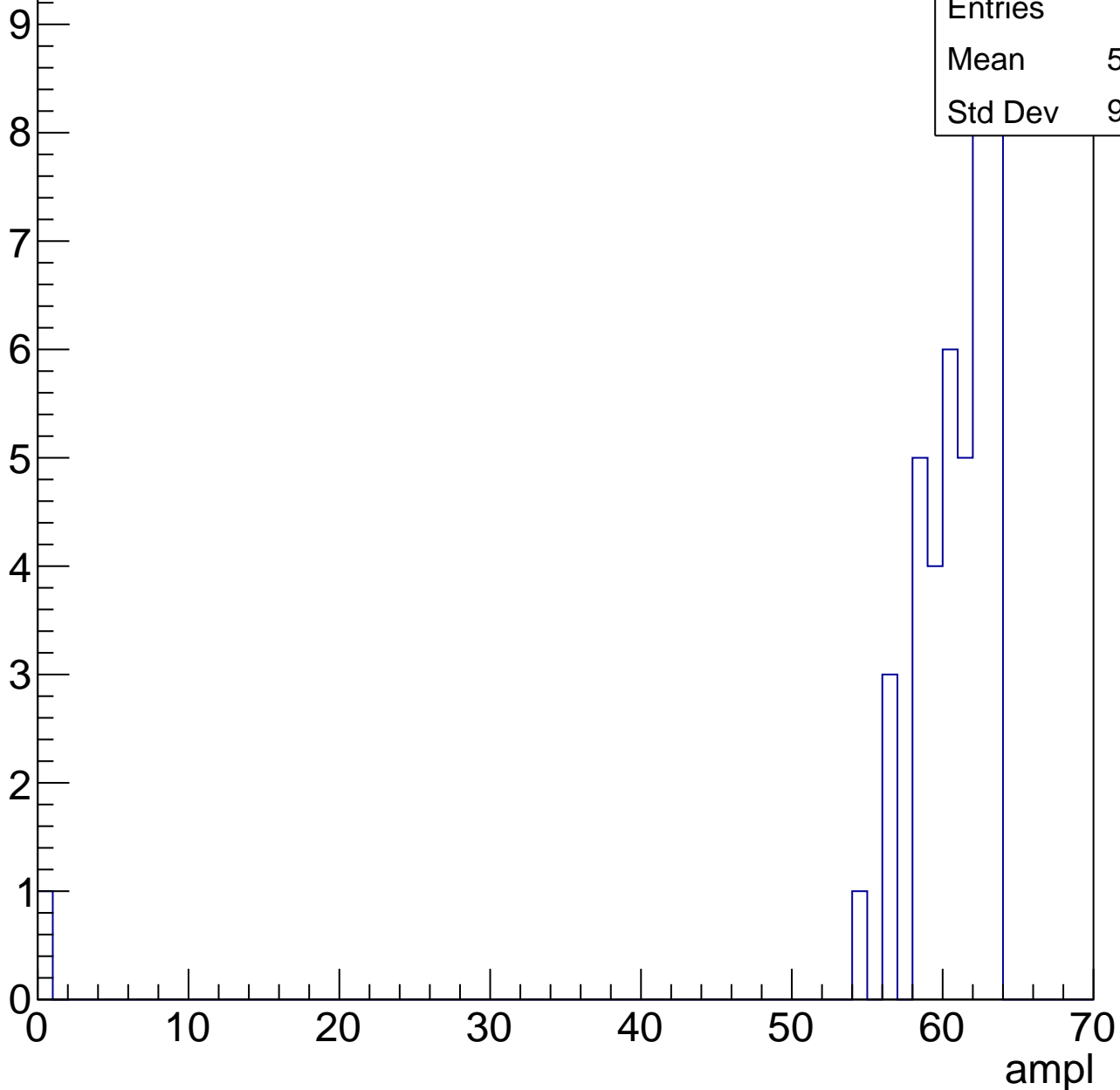


# B0L000S, U7-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	42
Mean	58.95
Std Dev	9.487



# B0L000S, U7-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch119, adc0

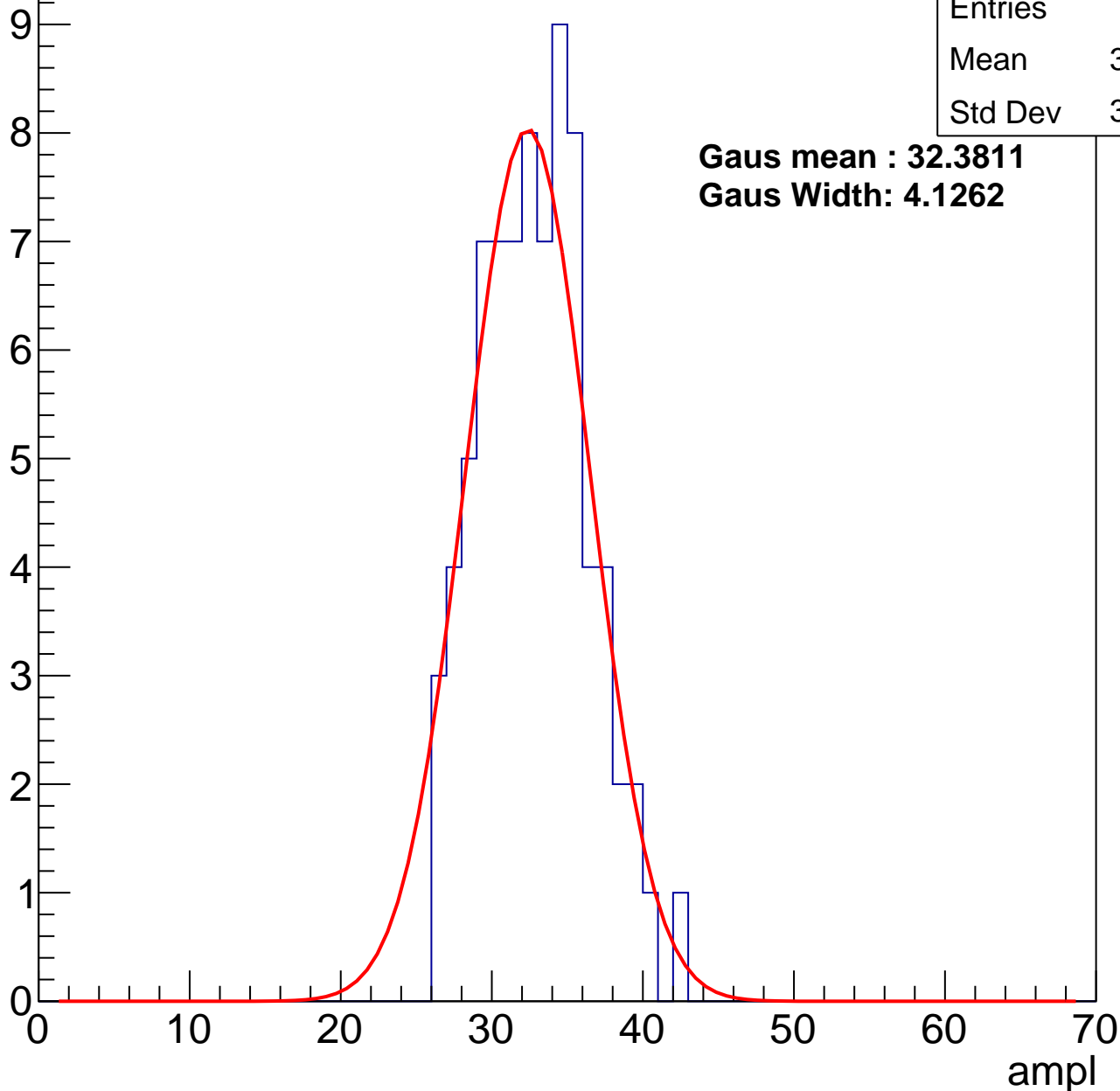
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	79
Mean	32.37
Std Dev	3.537

**Gaus mean : 32.3811**

**Gaus Width: 4.1262**



# B0L000S, U7-ch119, adc1

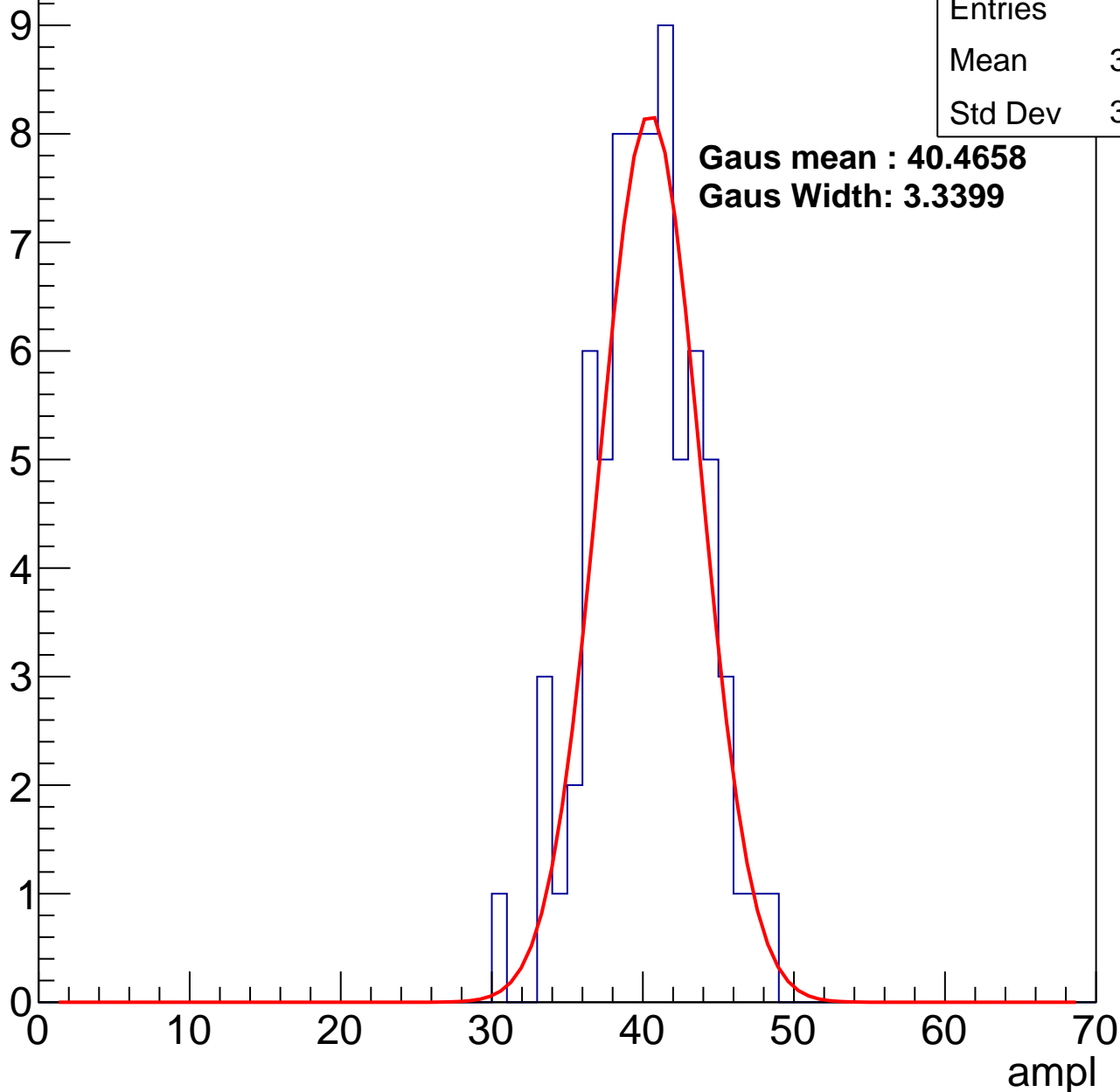
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	73
Mean	39.77
Std Dev	3.505

**Gaus mean : 40.4658**

**Gaus Width: 3.3399**



# B0L000S, U7-ch119, adc2

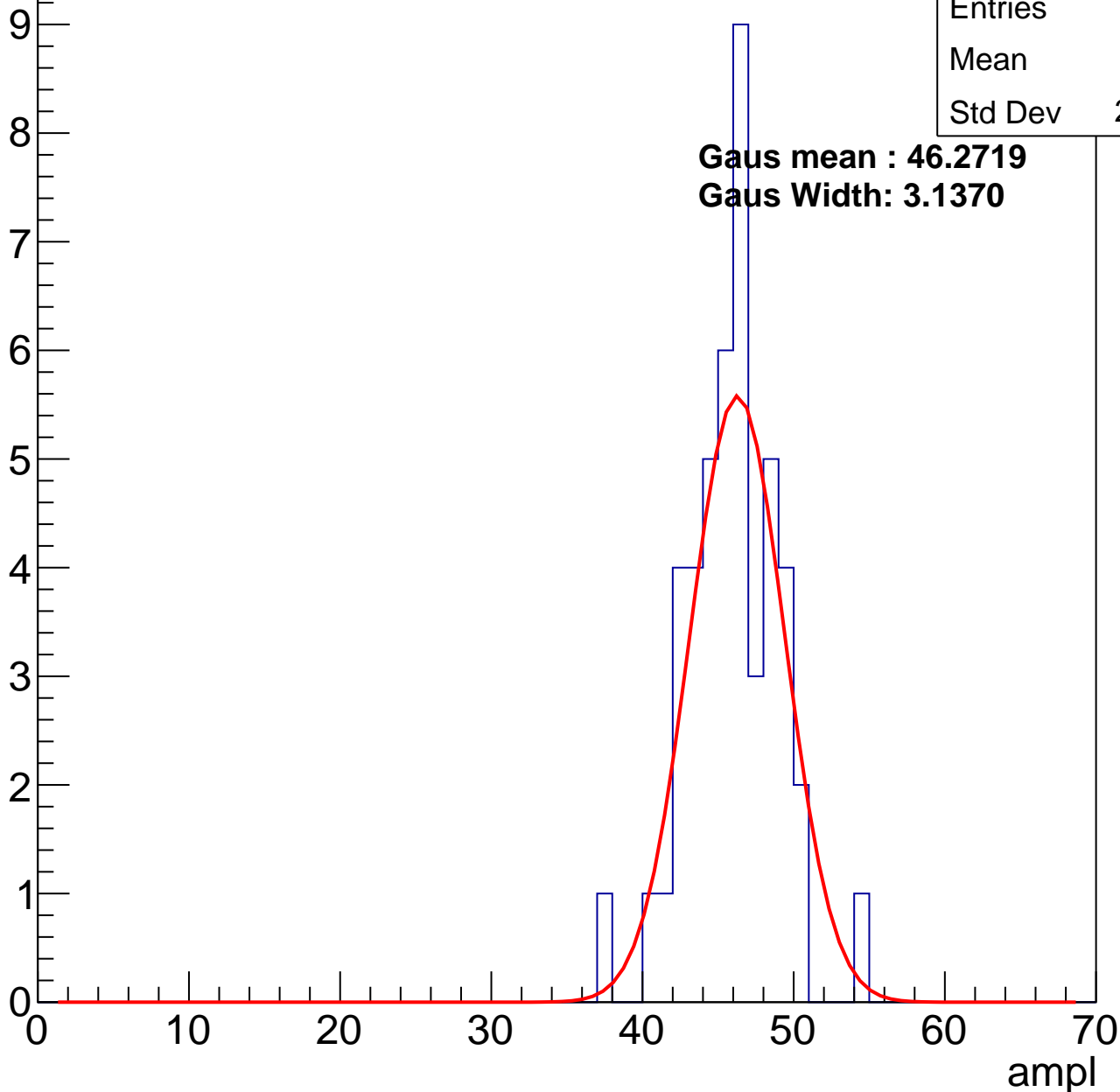
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	46
Mean	45.5
Std Dev	2.991

**Gaus mean : 46.2719**

**Gaus Width: 3.1370**

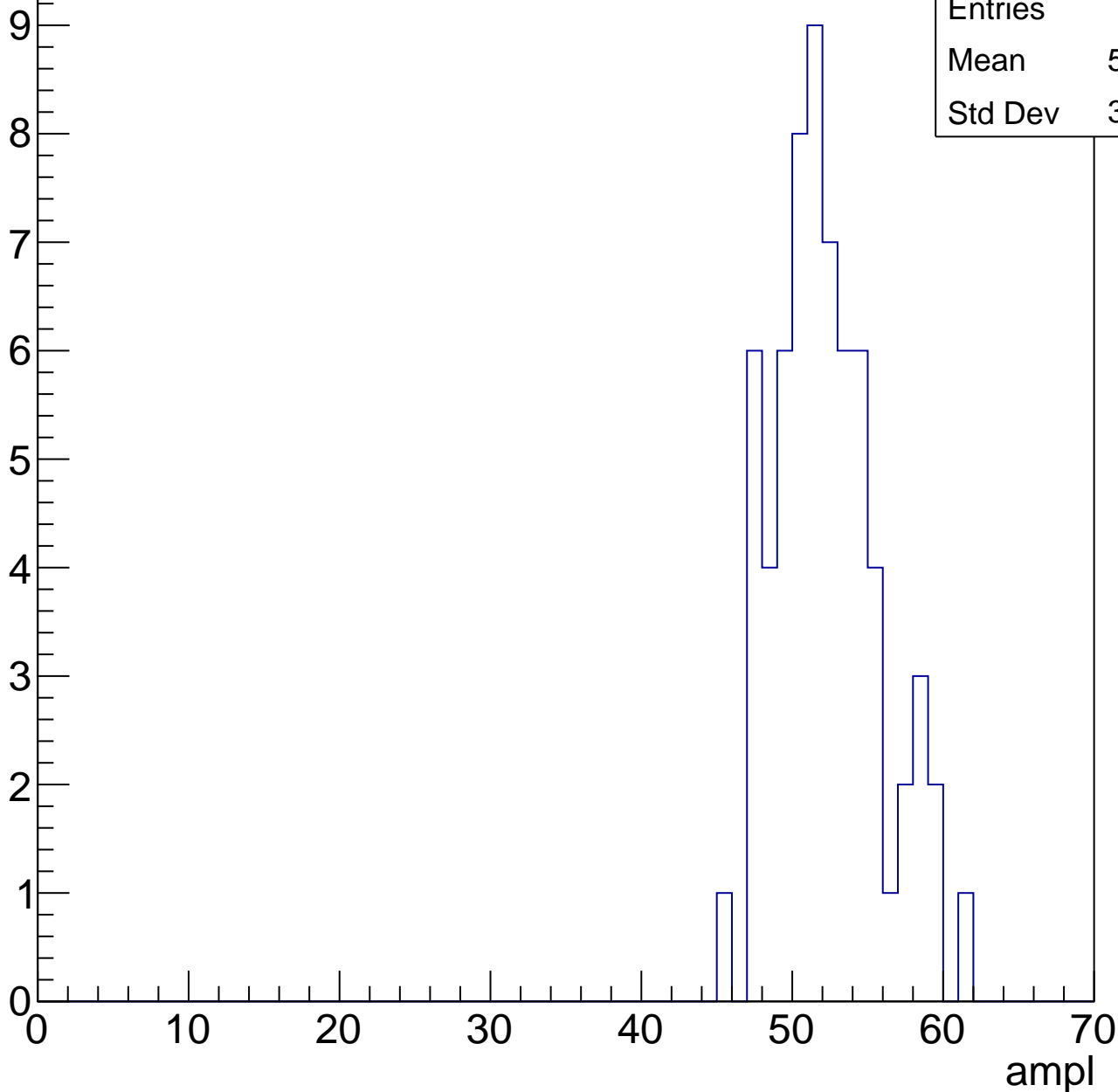


# B0L000S, U7-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	66
Mean	51.83
Std Dev	3.427

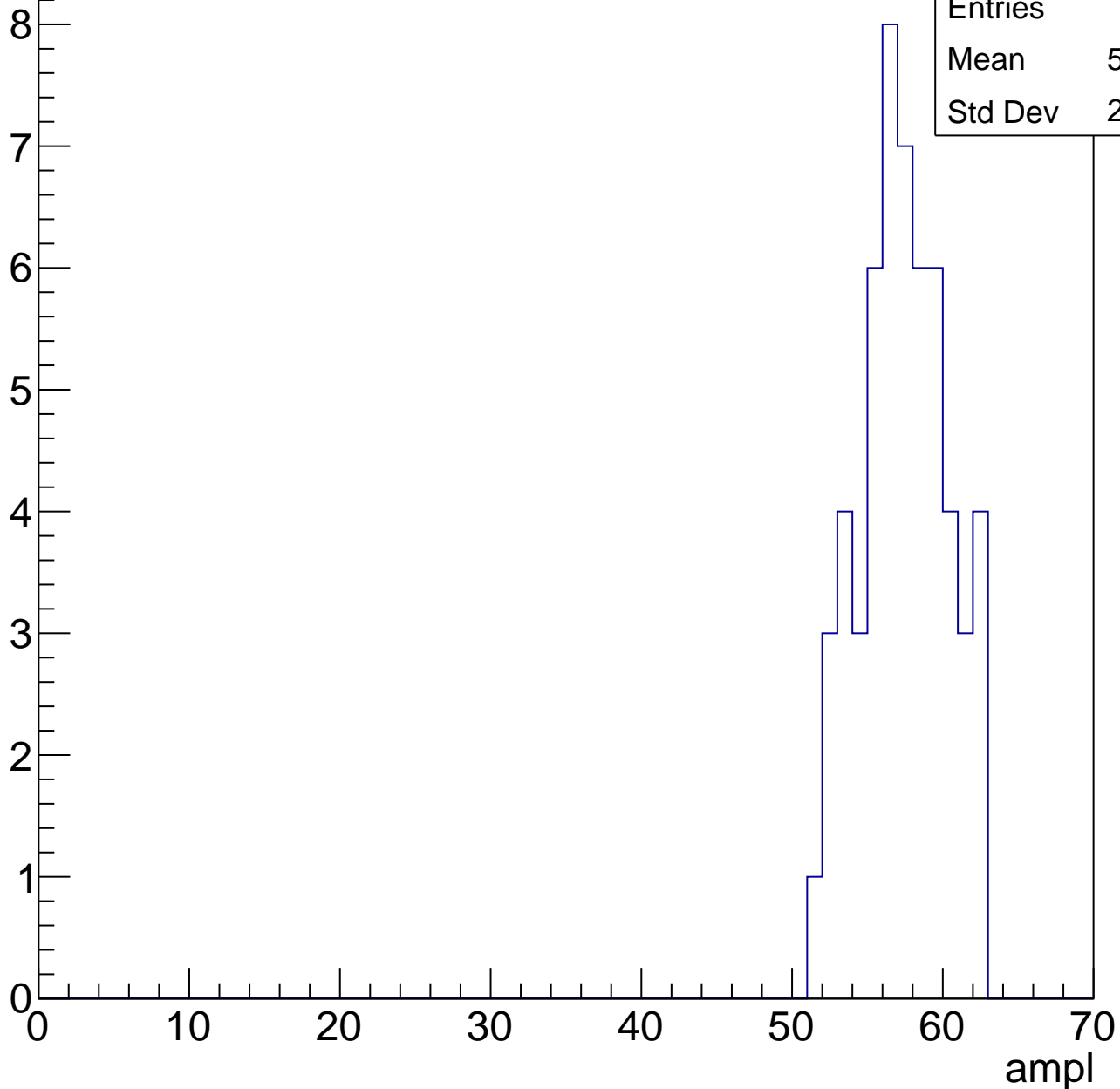


# B0L000S, U7-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	55
Mean	56.93
Std Dev	2.853

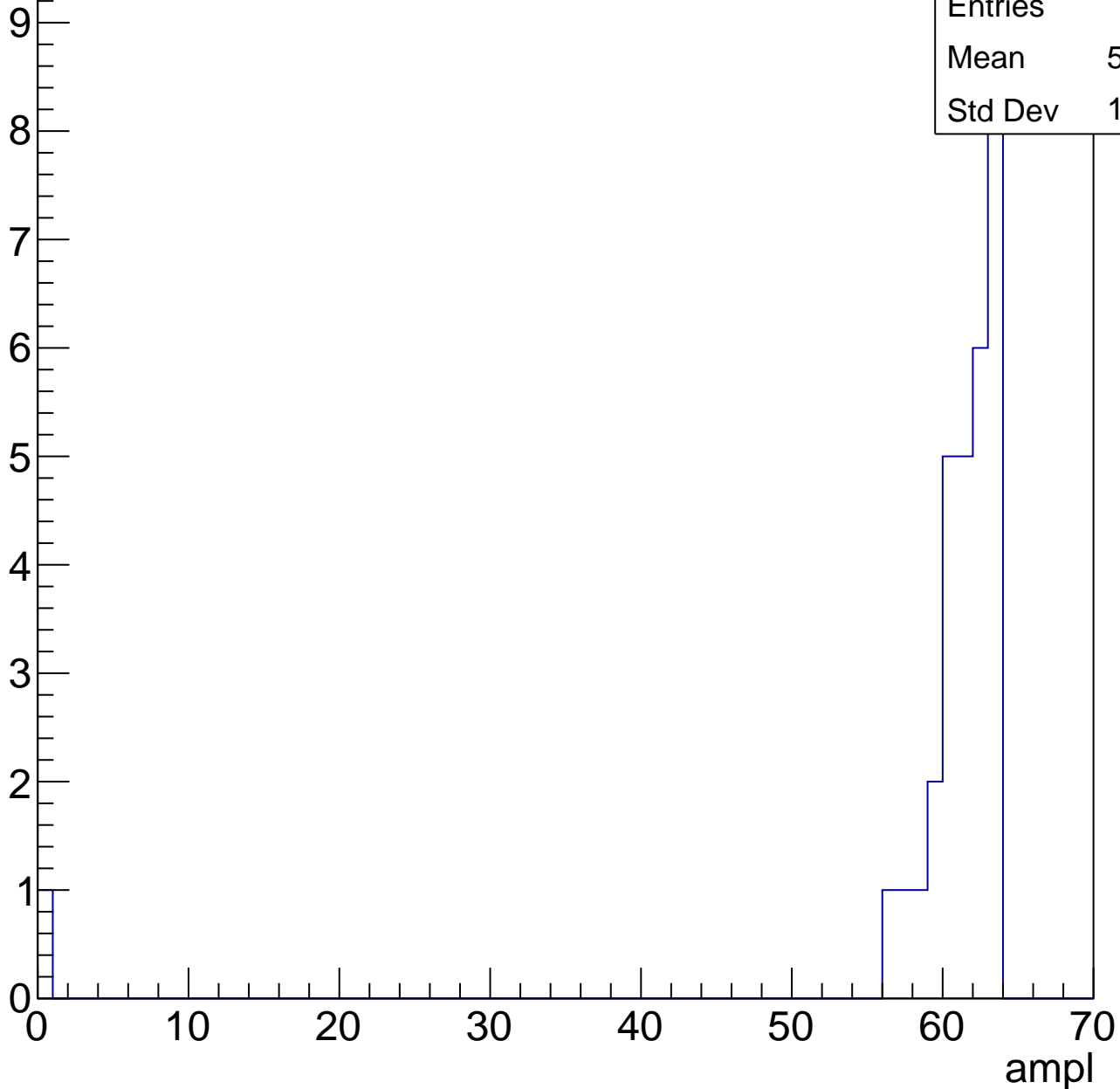


# B0L000S, U7-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	31
Mean	59.13
Std Dev	10.95



# B0L000S, U7-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	3
Mean	8.333
Std Dev	11.79

# B0L000S, U7-ch120, adc0

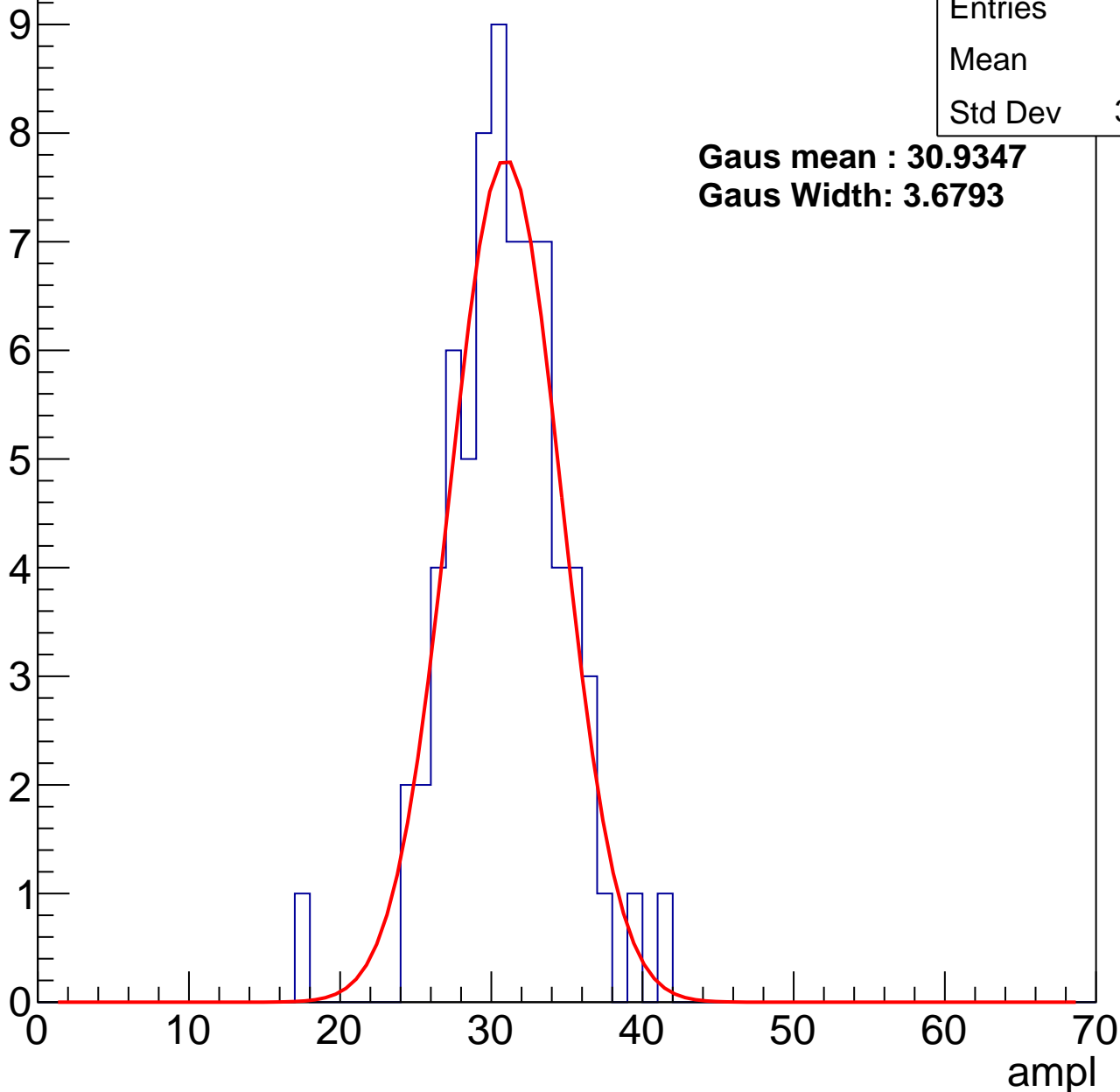
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	72
Mean	30.5
Std Dev	3.801

**Gaus mean : 30.9347**

**Gaus Width: 3.6793**



# B0L000S, U7-ch120, adc1

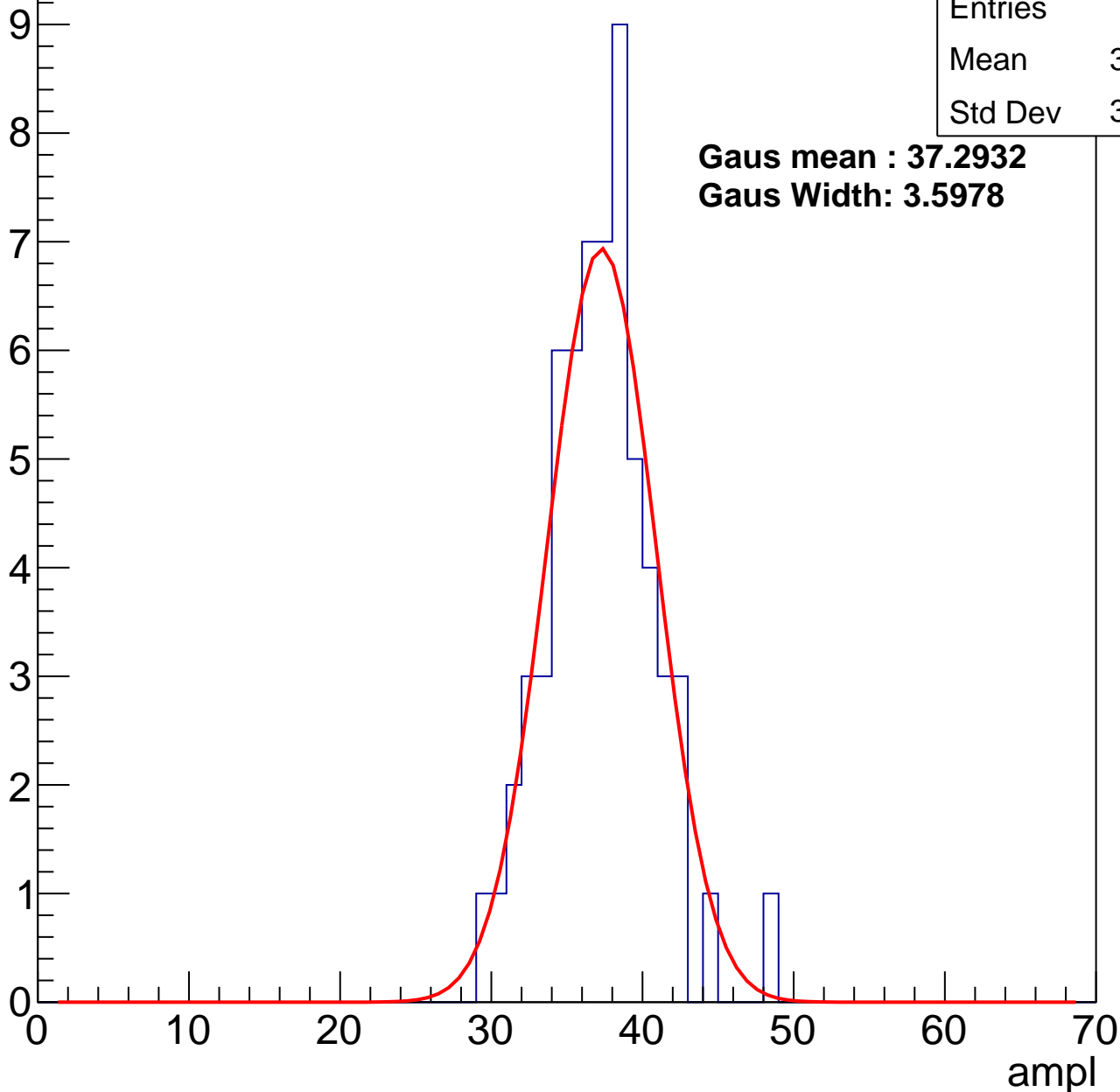
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	62
Mean	36.76
Std Dev	3.472

**Gaus mean : 37.2932**

**Gaus Width: 3.5978**



# B0L000S, U7-ch120, adc2

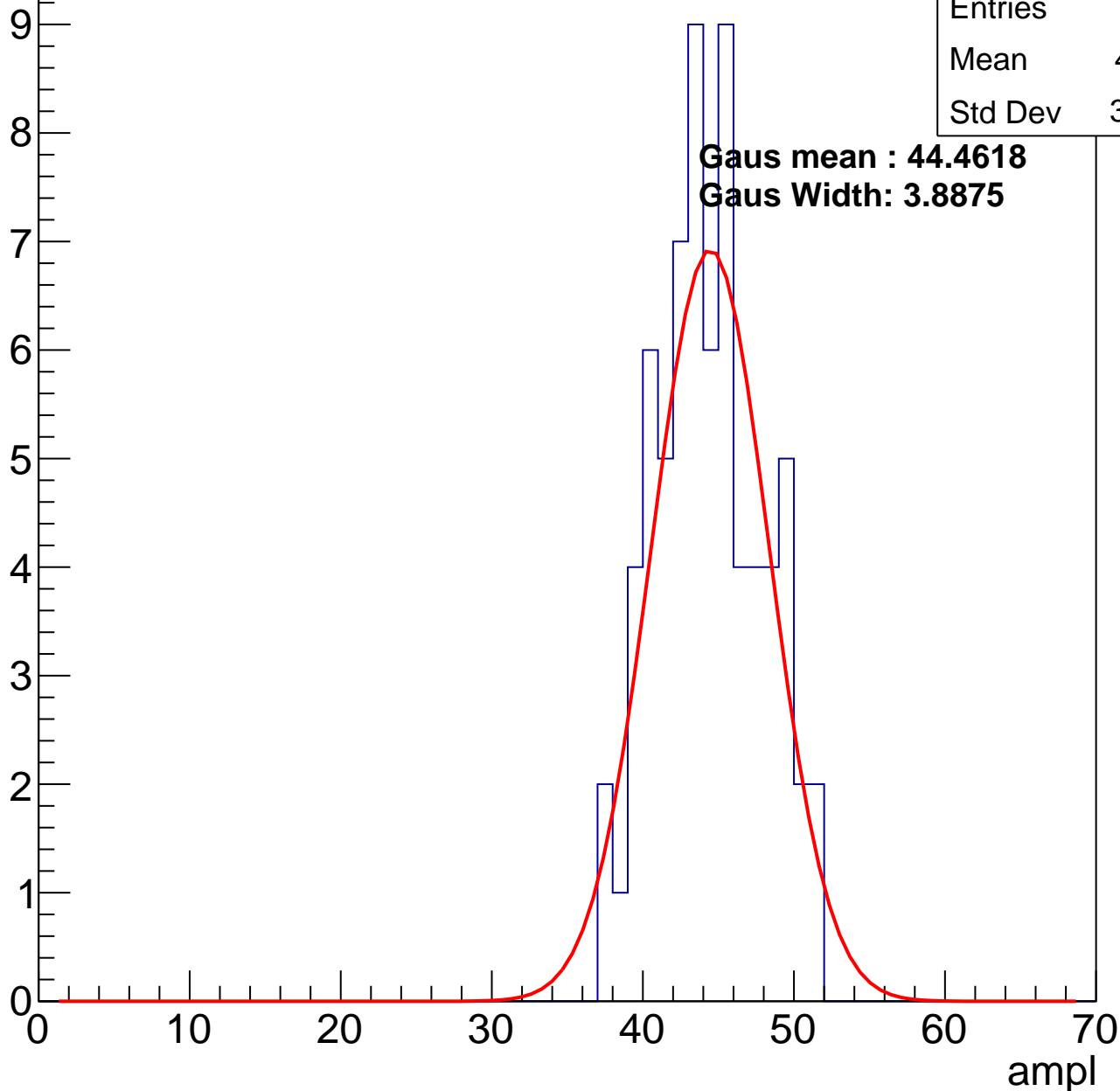
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	70
Mean	43.91
Std Dev	3.447

**Gaus mean : 44.4618**

**Gaus Width: 3.8875**

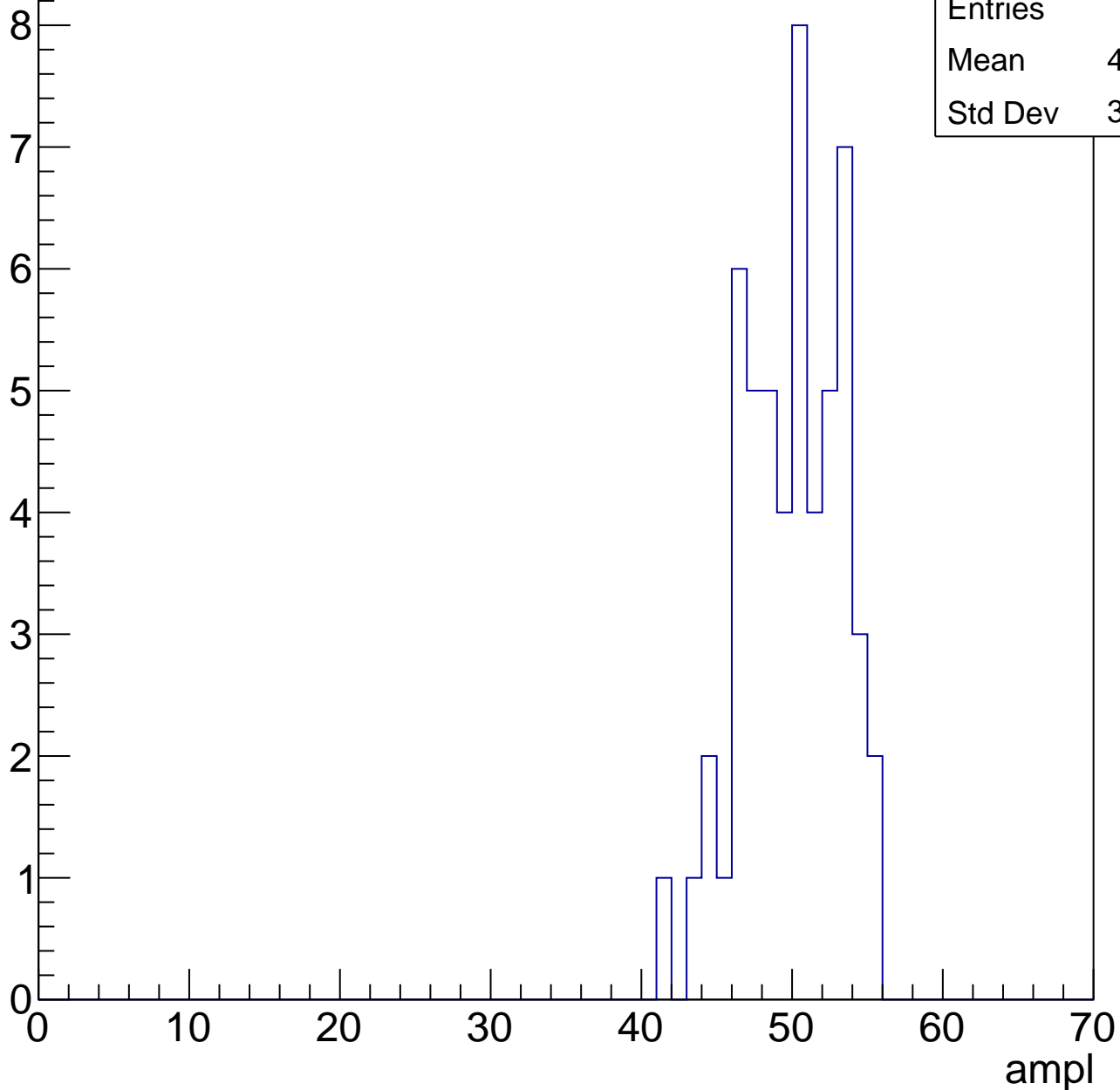


# B0L000S, U7-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	54
Mean	49.46
Std Dev	3.224

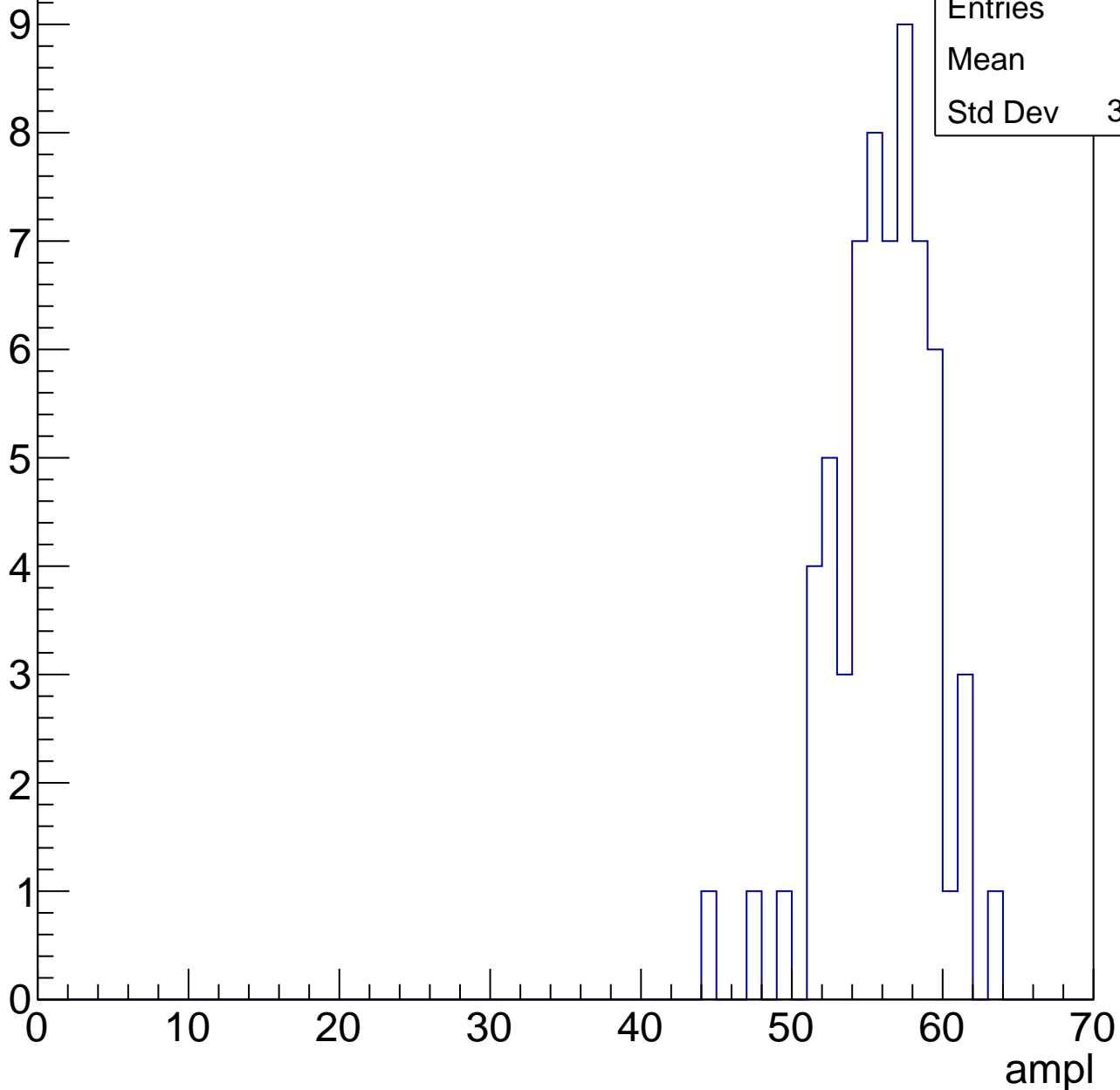


# B0L000S, U7-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

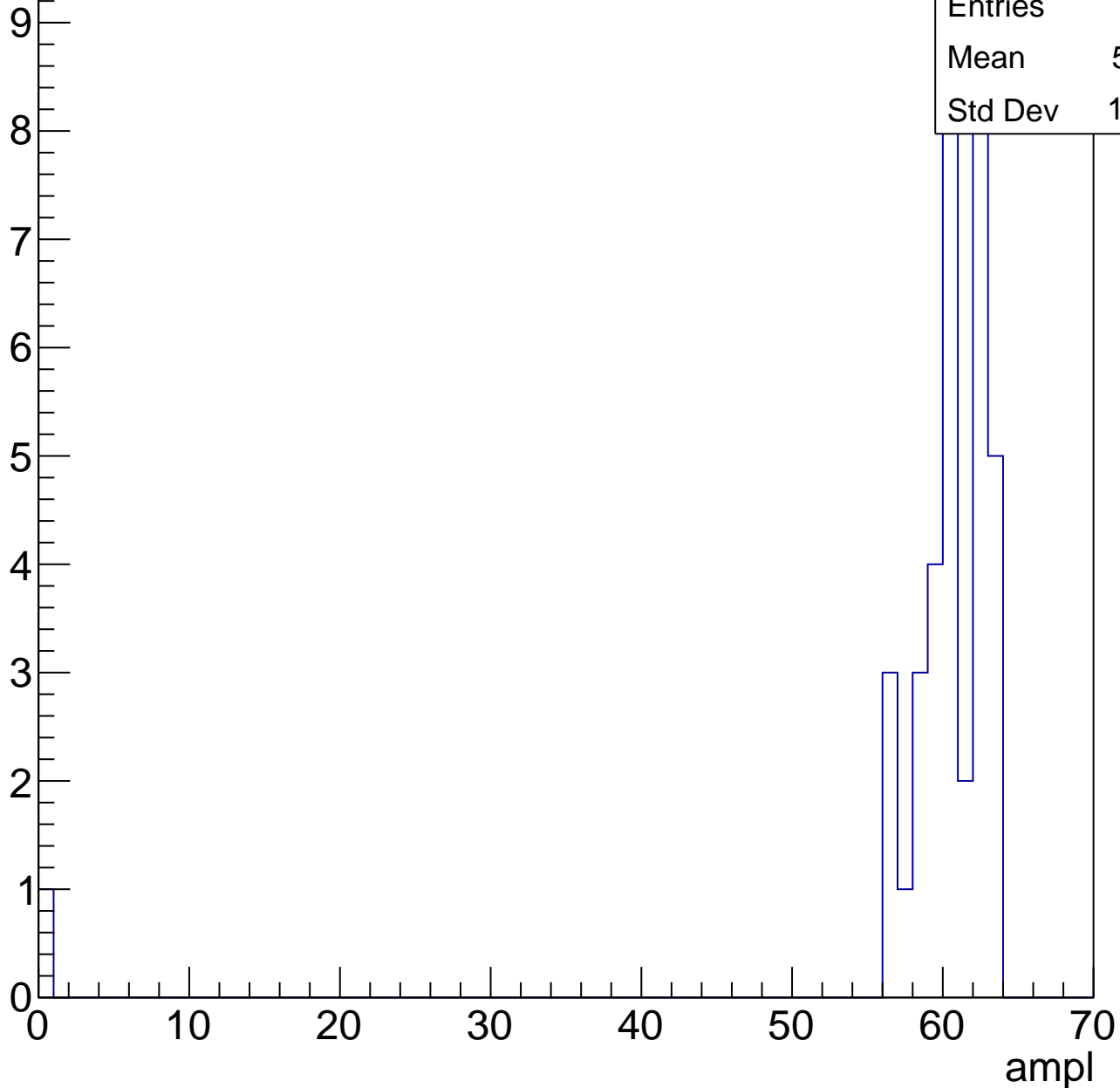
Entries	64
Mean	55.5
Std Dev	3.382



# B0L000S, U7-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

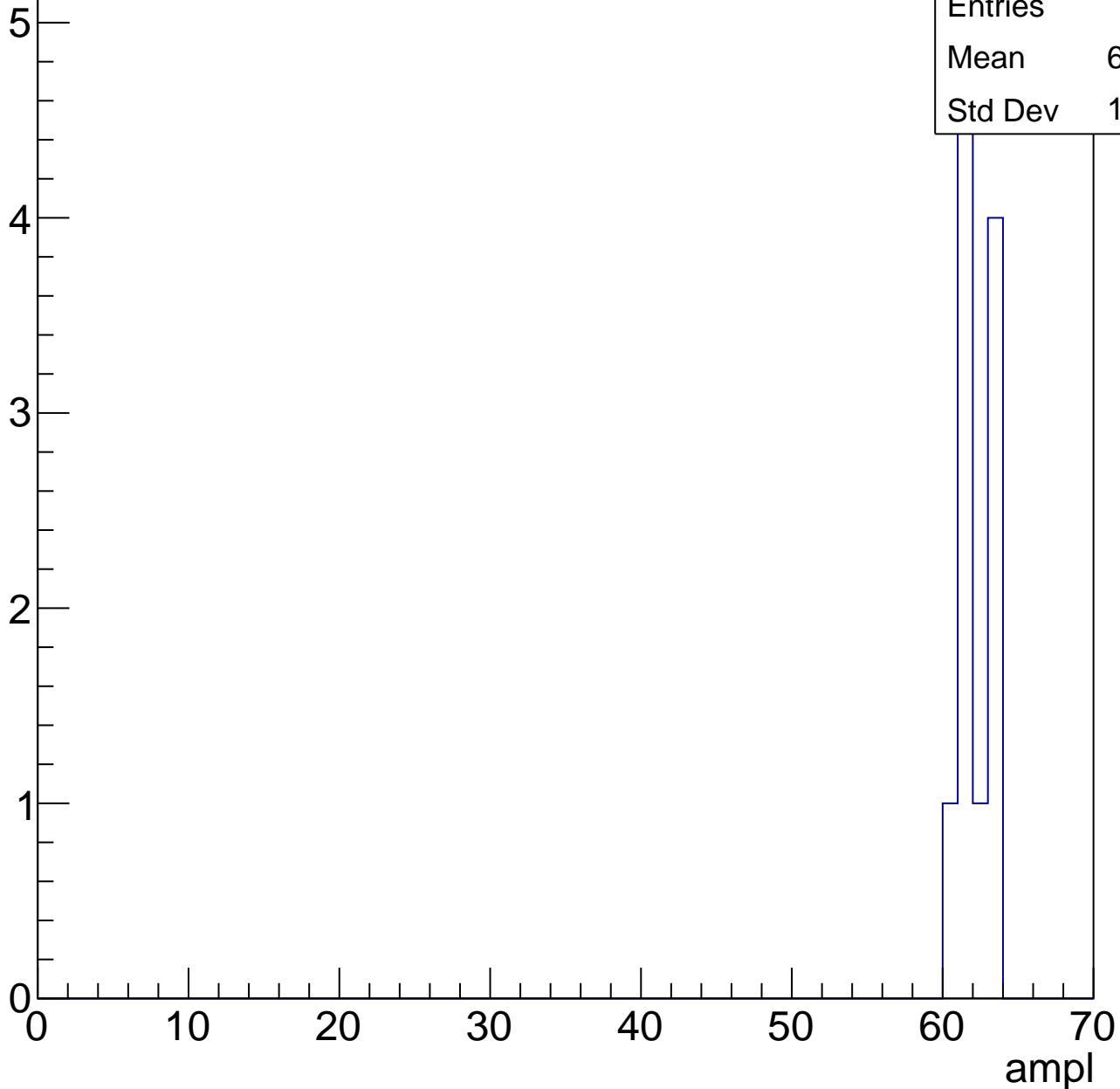


# B0L000S, U7-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	11
Mean	61.73
Std Dev	1.052





# B0L000S, U7-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch121, adc0

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	77
Mean	30.86
Std Dev	3.452

**Gaus mean : 31.6863**

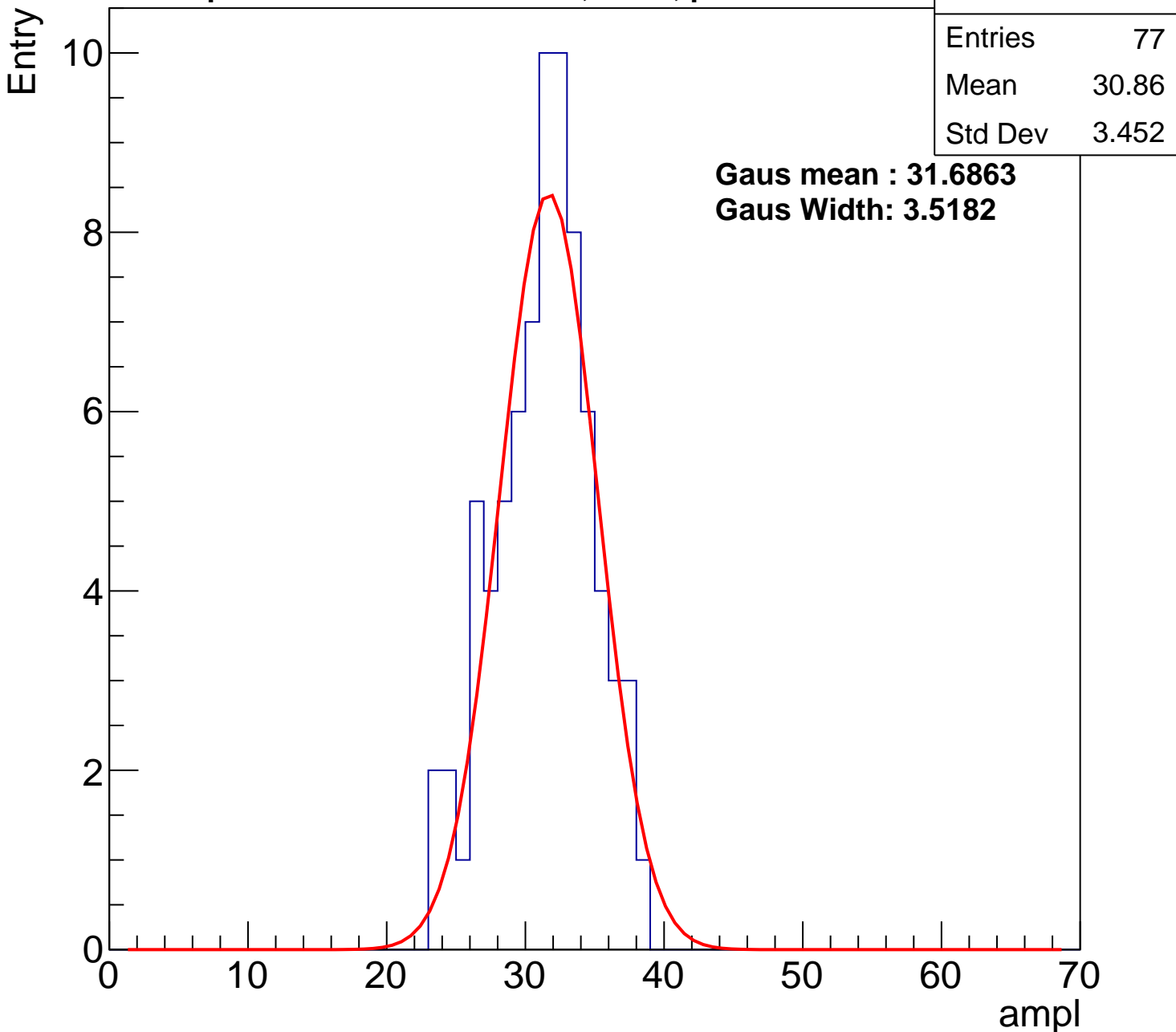
**Gaus Width: 3.5182**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

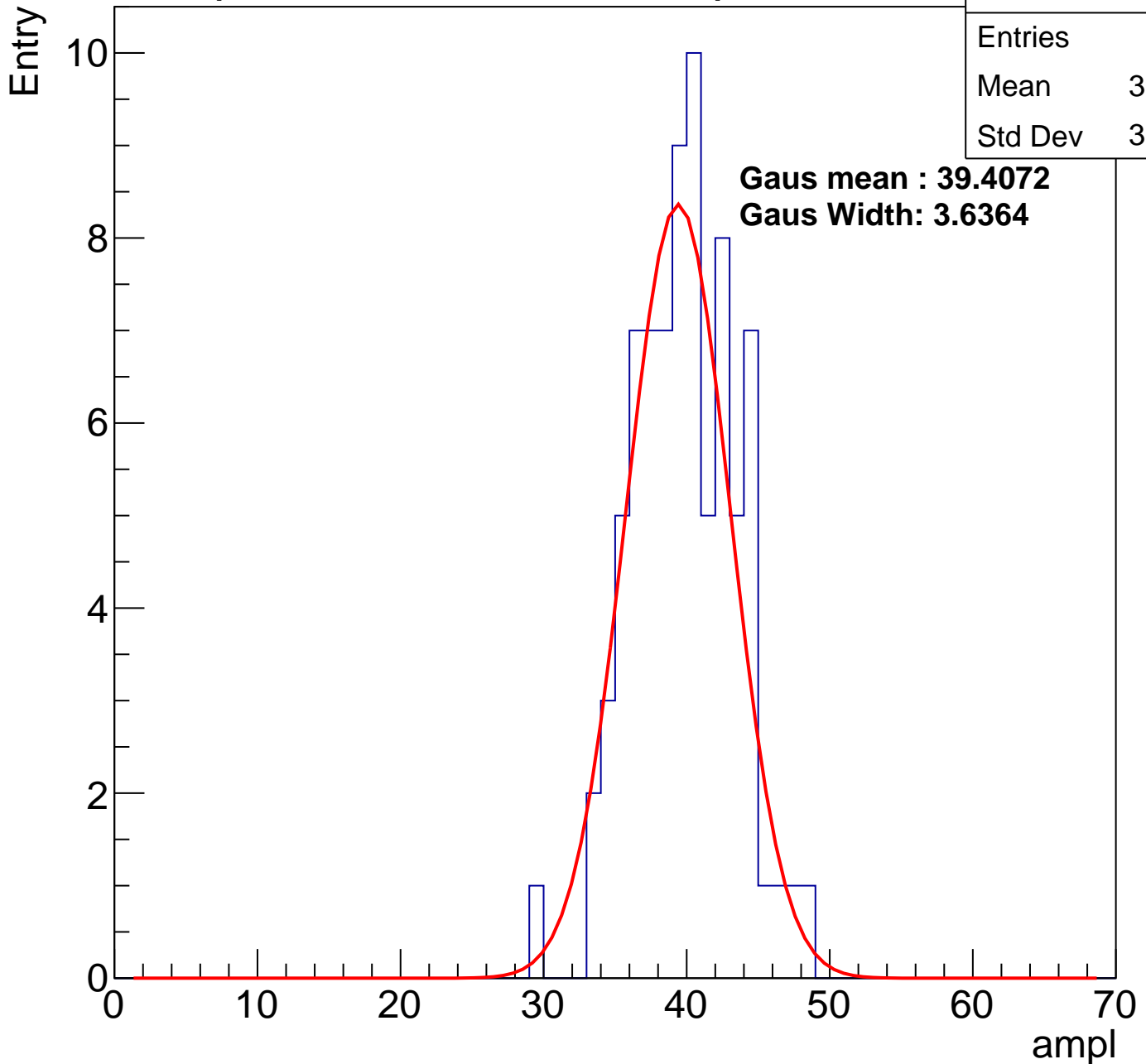


# B0L000S, U7-ch121, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	80
Mean	39.38
Std Dev	3.537

**Gaus mean : 39.4072**  
**Gaus Width: 3.6364**



# B0L000S, U7-ch121, adc2

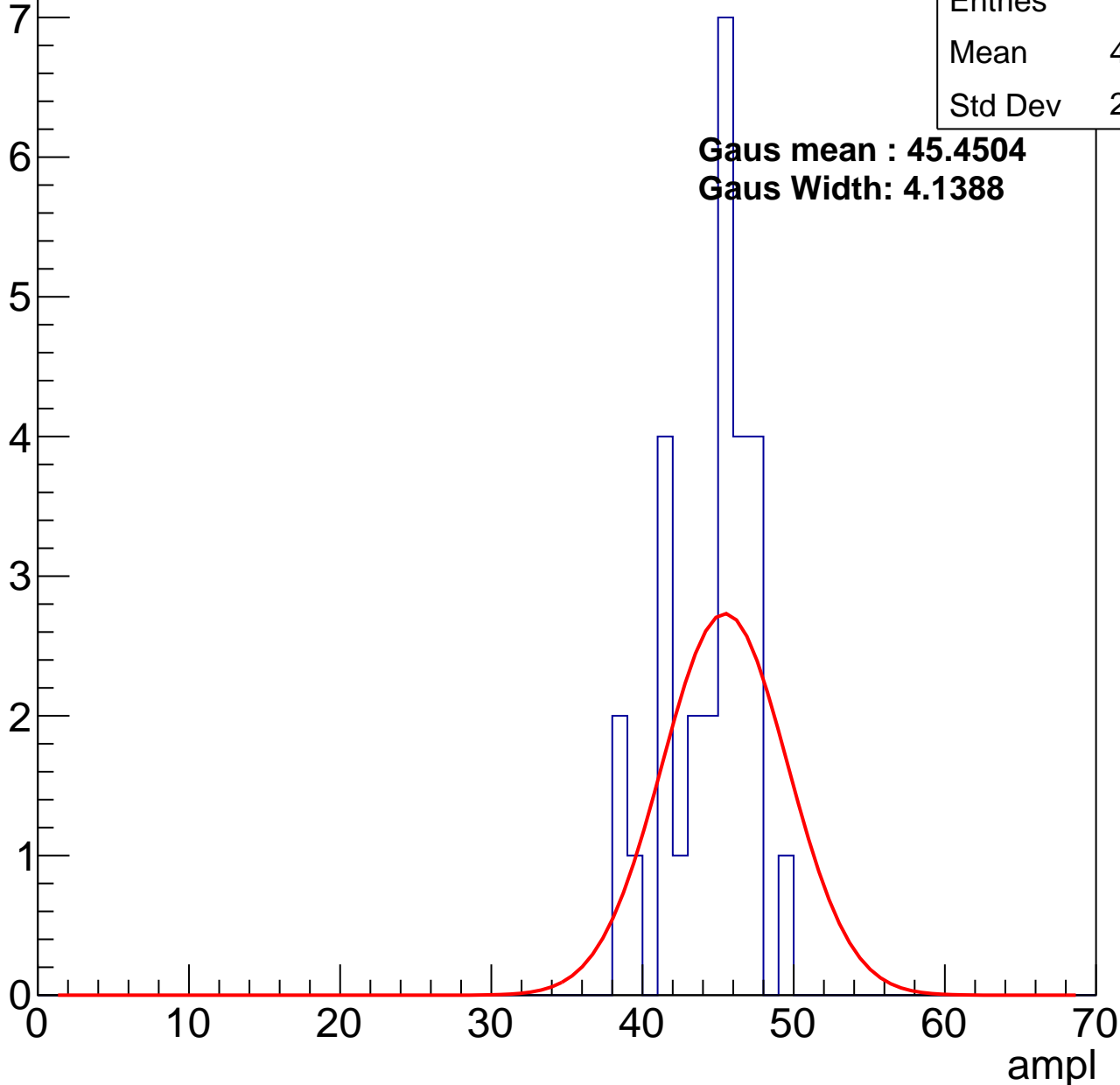
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	28
Mean	43.96
Std Dev	2.822

**Gaus mean : 45.4504**

**Gaus Width: 4.1388**

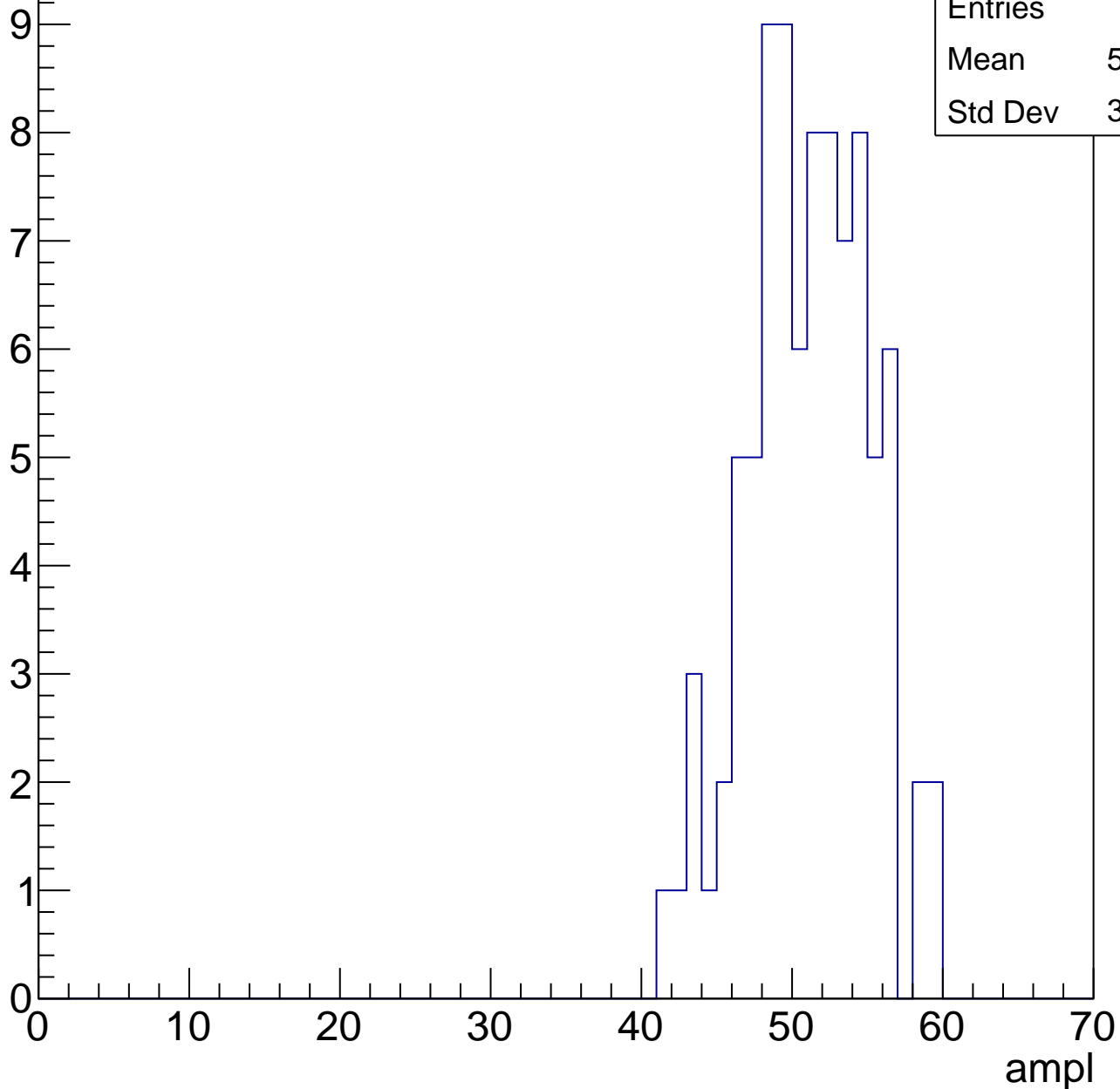


# B0L000S, U7-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	88
Mean	50.64
Std Dev	3.952

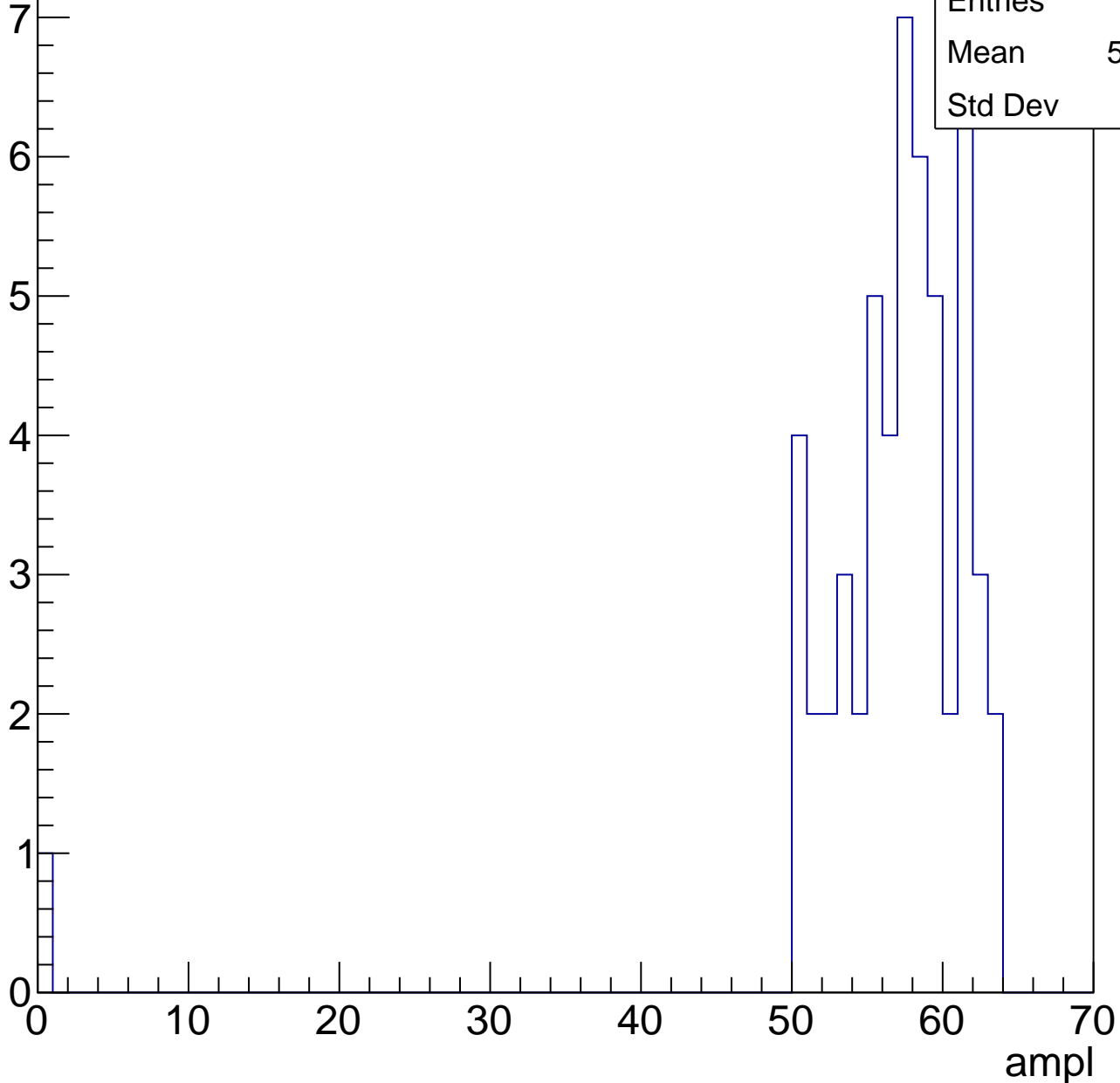


# B0L000S, U7-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

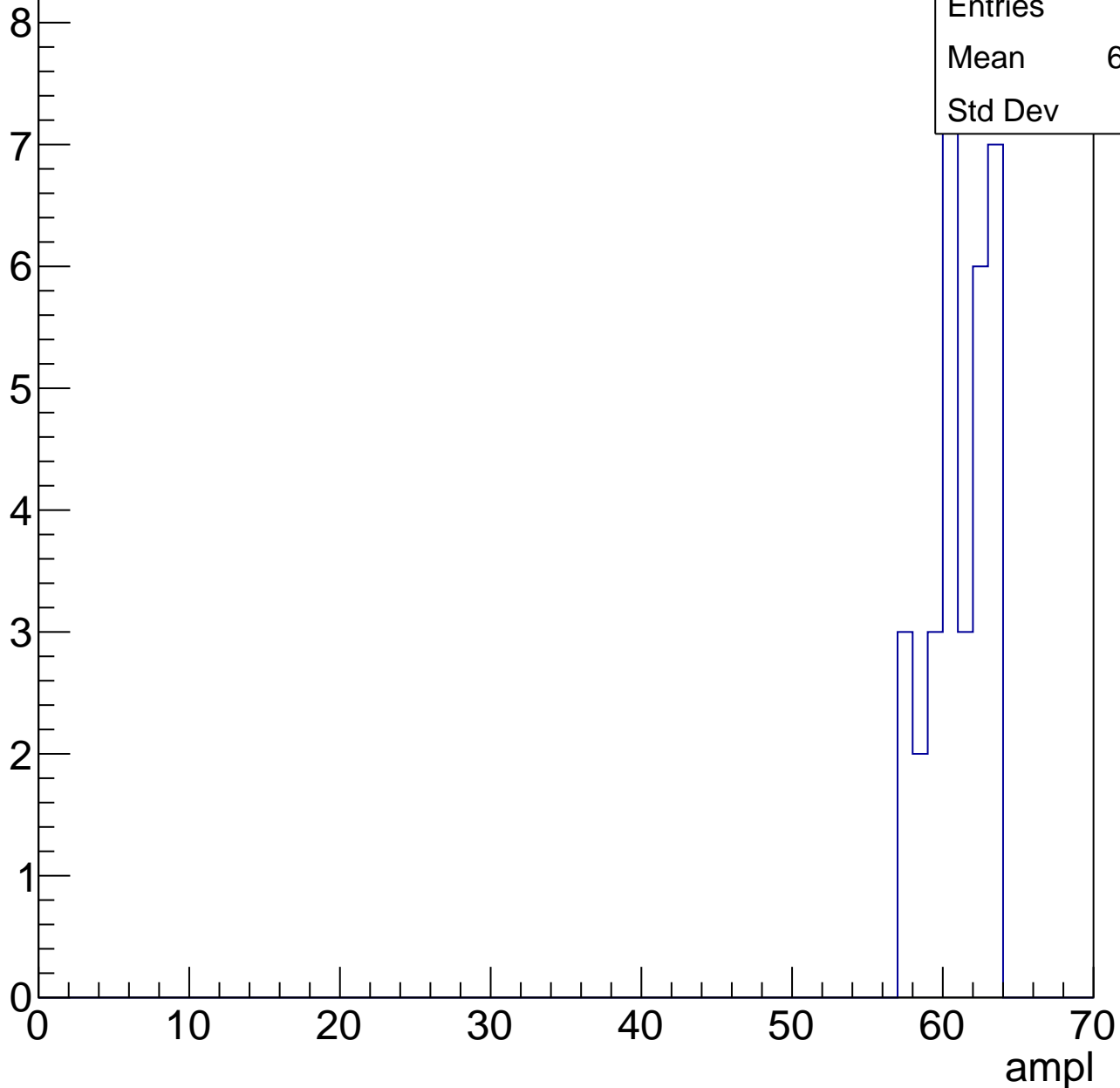
Entries	55
Mean	55.87
Std Dev	8.41



# B0L000S, U7-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	32
Mean	60.62
Std Dev	1.9

# B0L000S, U7-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch122, adc0

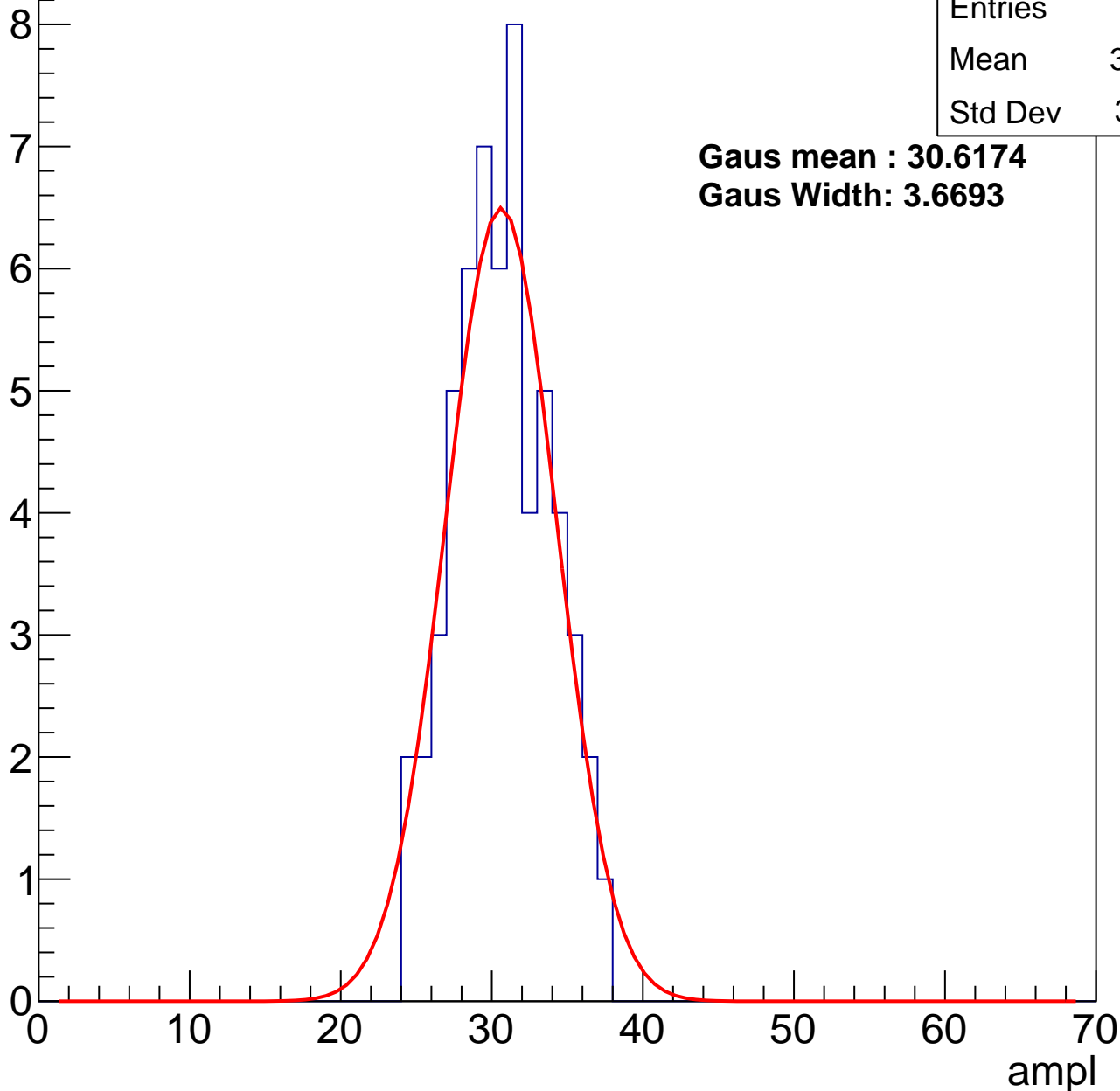
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	58
Mean	30.22
Std Dev	3.141

**Gaus mean : 30.6174**

**Gaus Width: 3.6693**



# B0L000S, U7-ch122, adc1

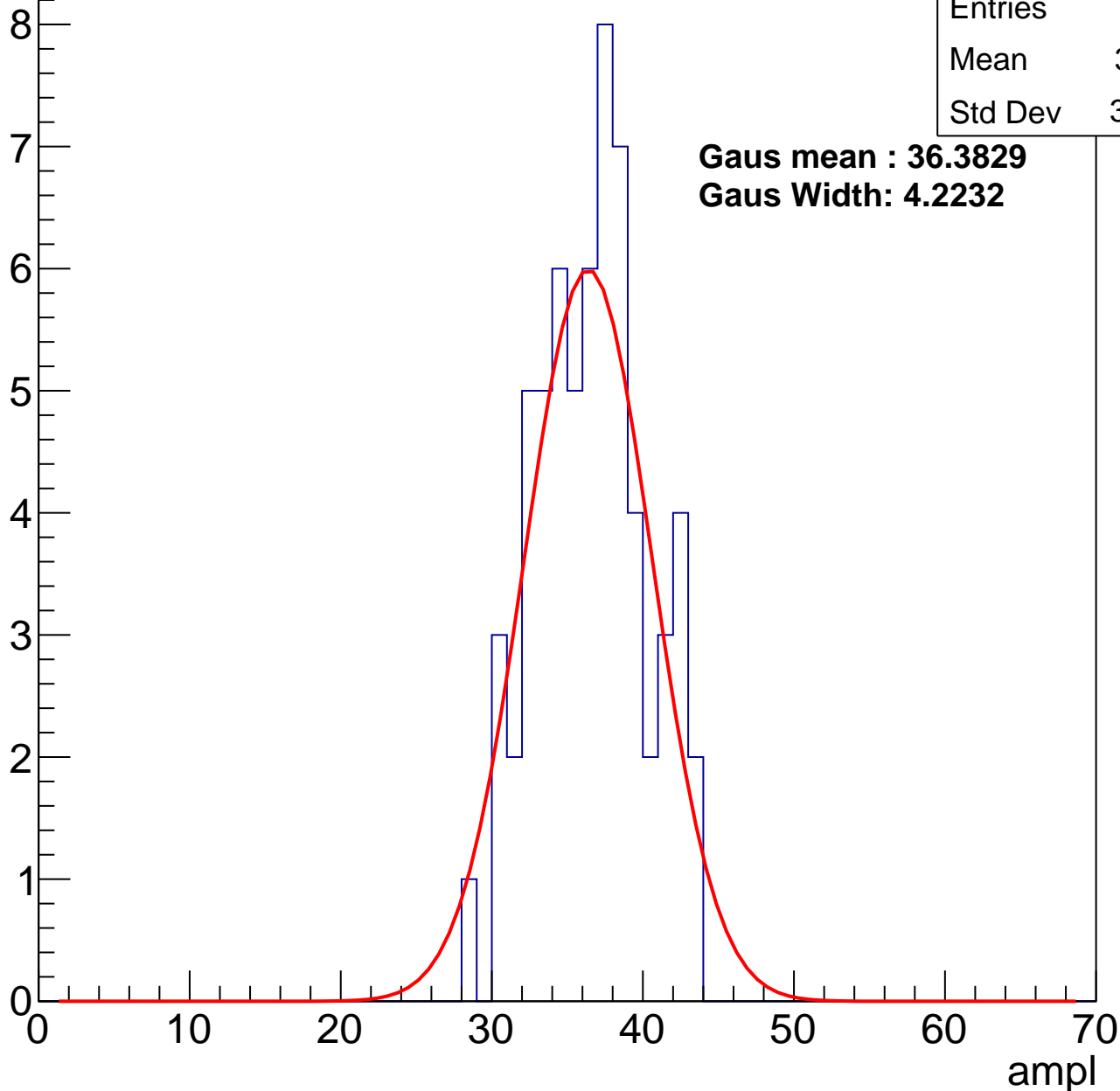
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	63
Mean	36.11
Std Dev	3.555

**Gaus mean : 36.3829**

**Gaus Width: 4.2232**



# B0L000S, U7-ch122, adc2

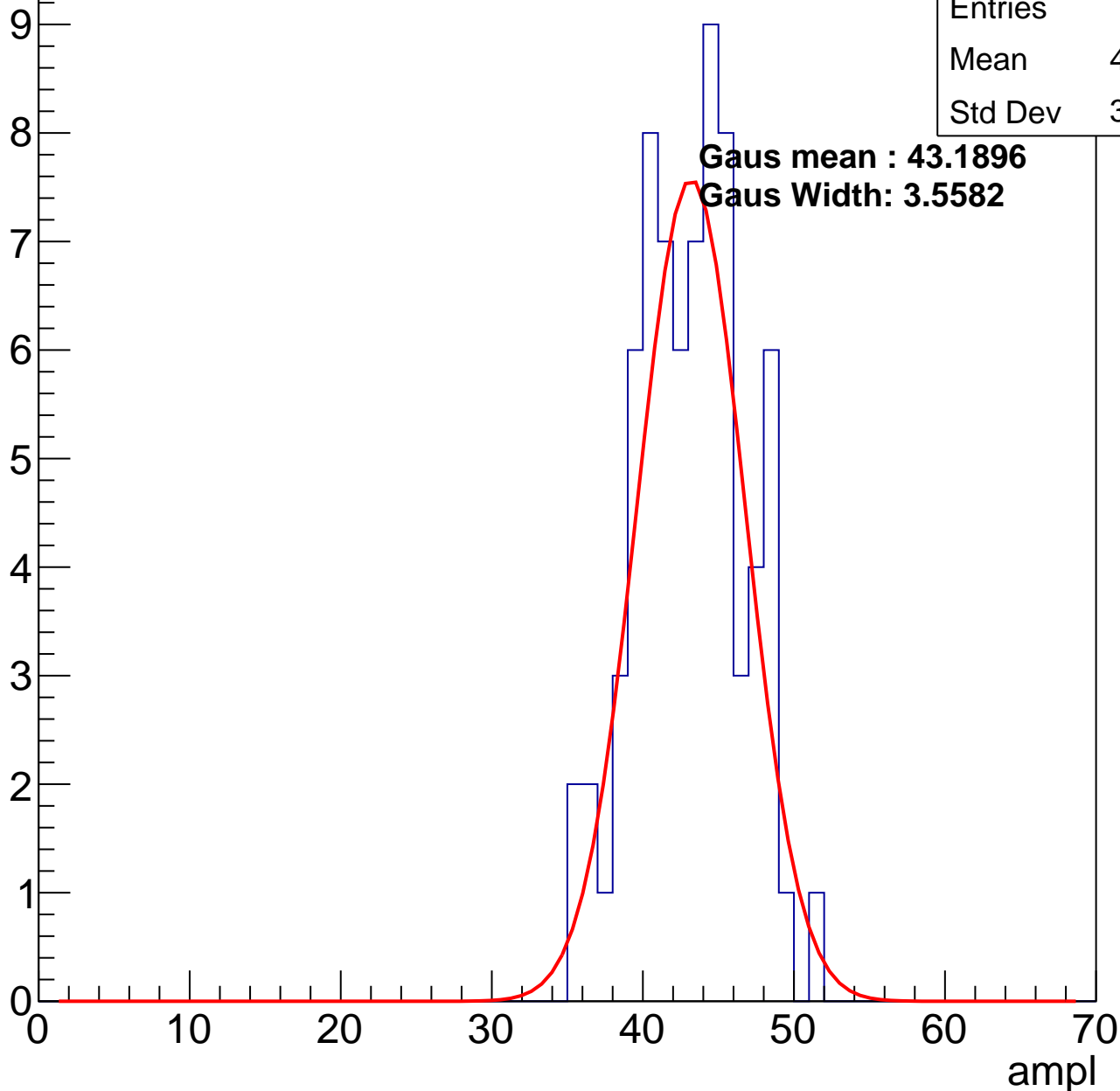
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	74
Mean	42.66
Std Dev	3.512

**Gaus mean : 43.1896**

**Gaus Width: 3.5582**



# B0L000S, U7-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

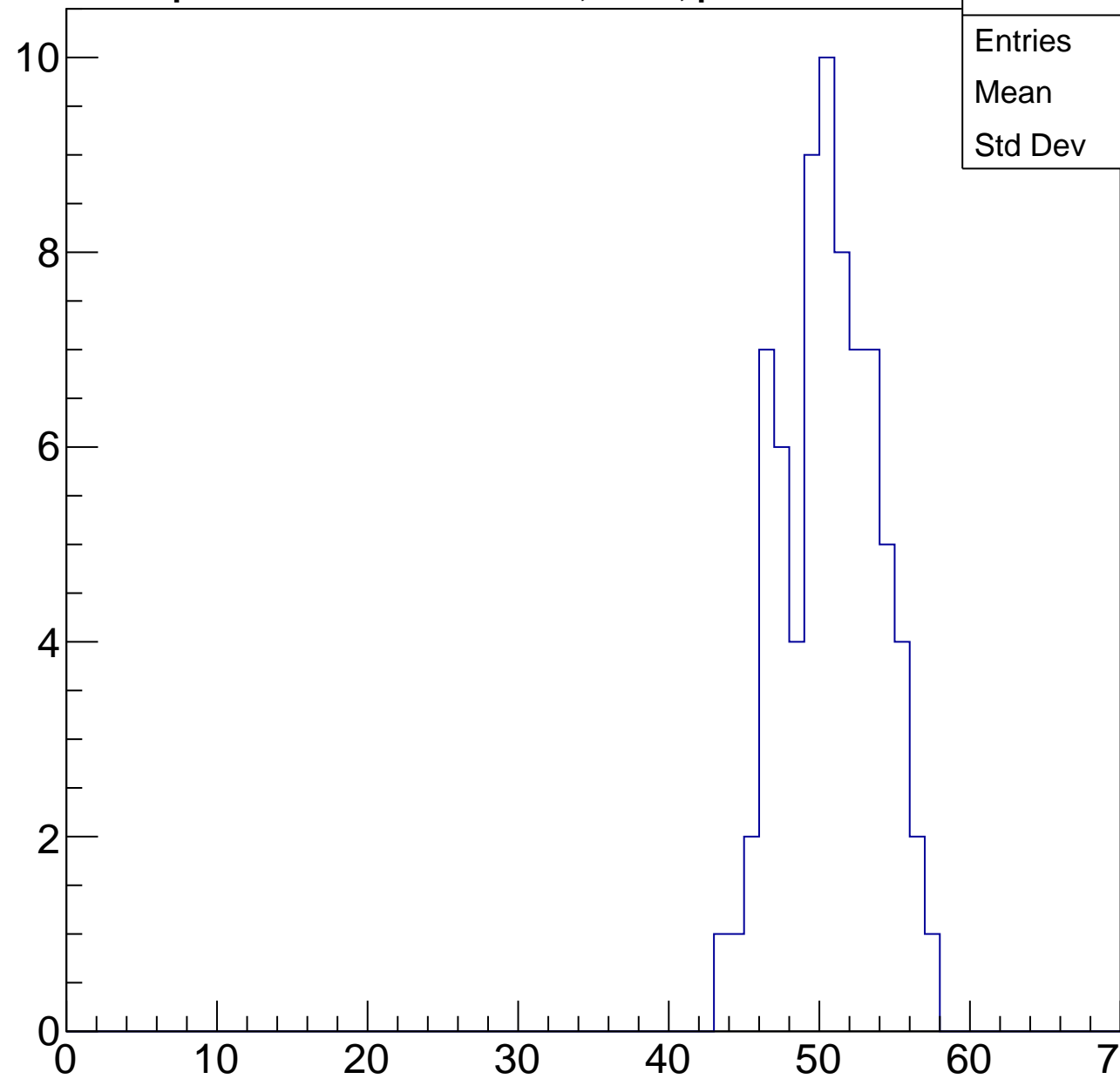
Entries	74
Mean	50.22
Std Dev	3.125

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

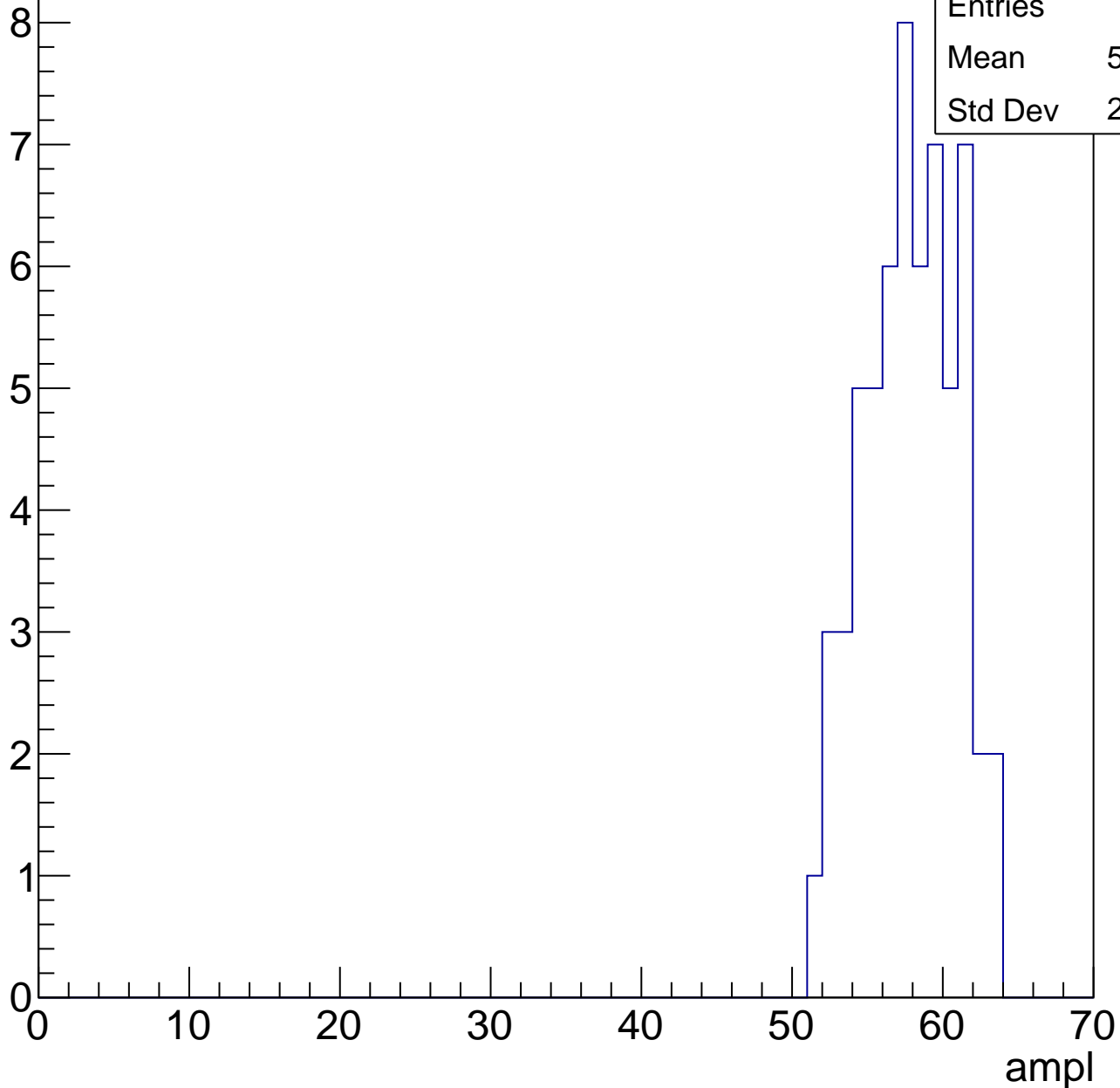
ampl



# B0L000S, U7-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



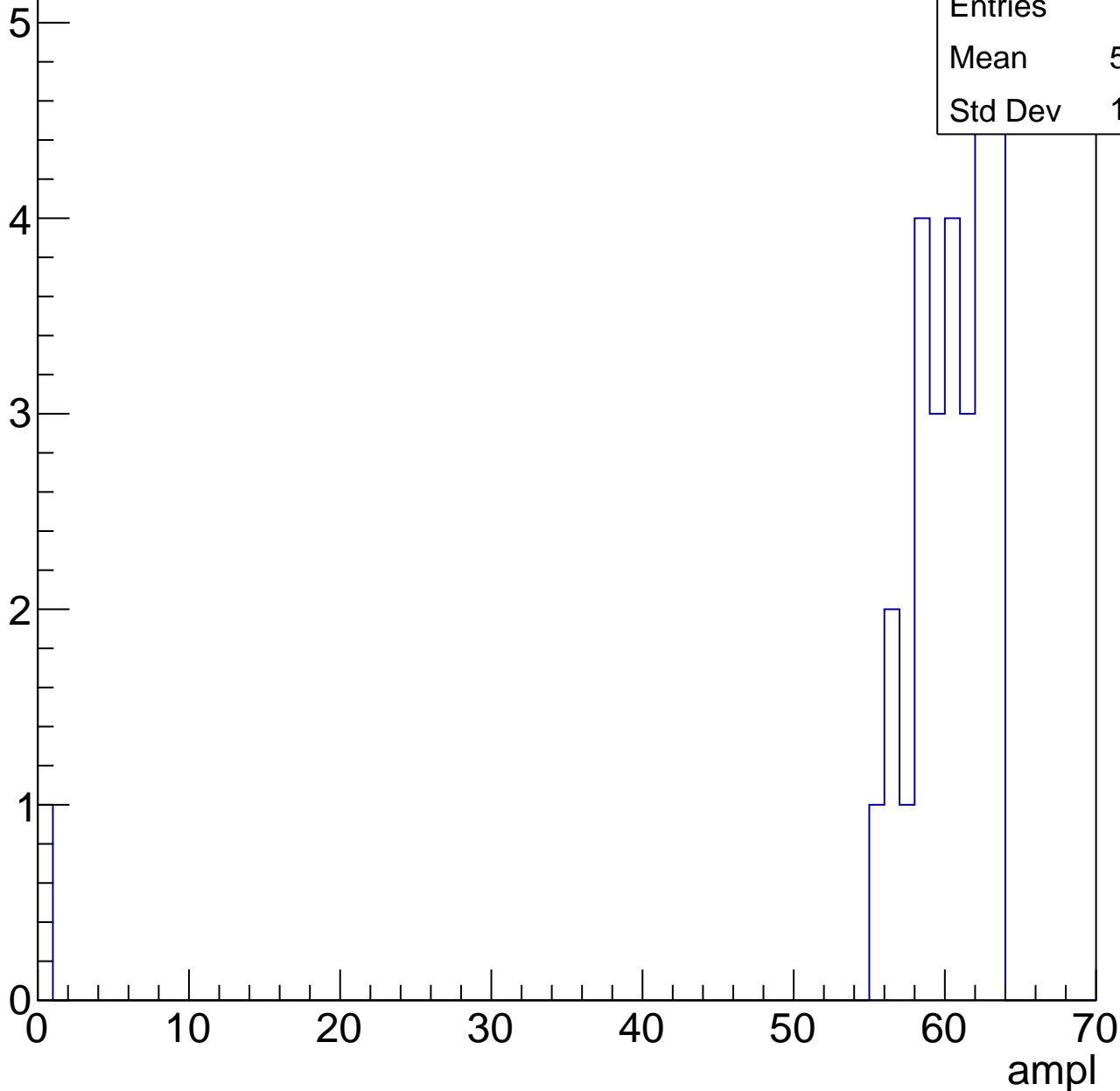
Entries	60
Mean	57.35
Std Dev	2.988

# B0L000S, U7-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	29
Mean	57.97
Std Dev	11.19



# B0L000S, U7-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L000S, U7-ch123, adc0

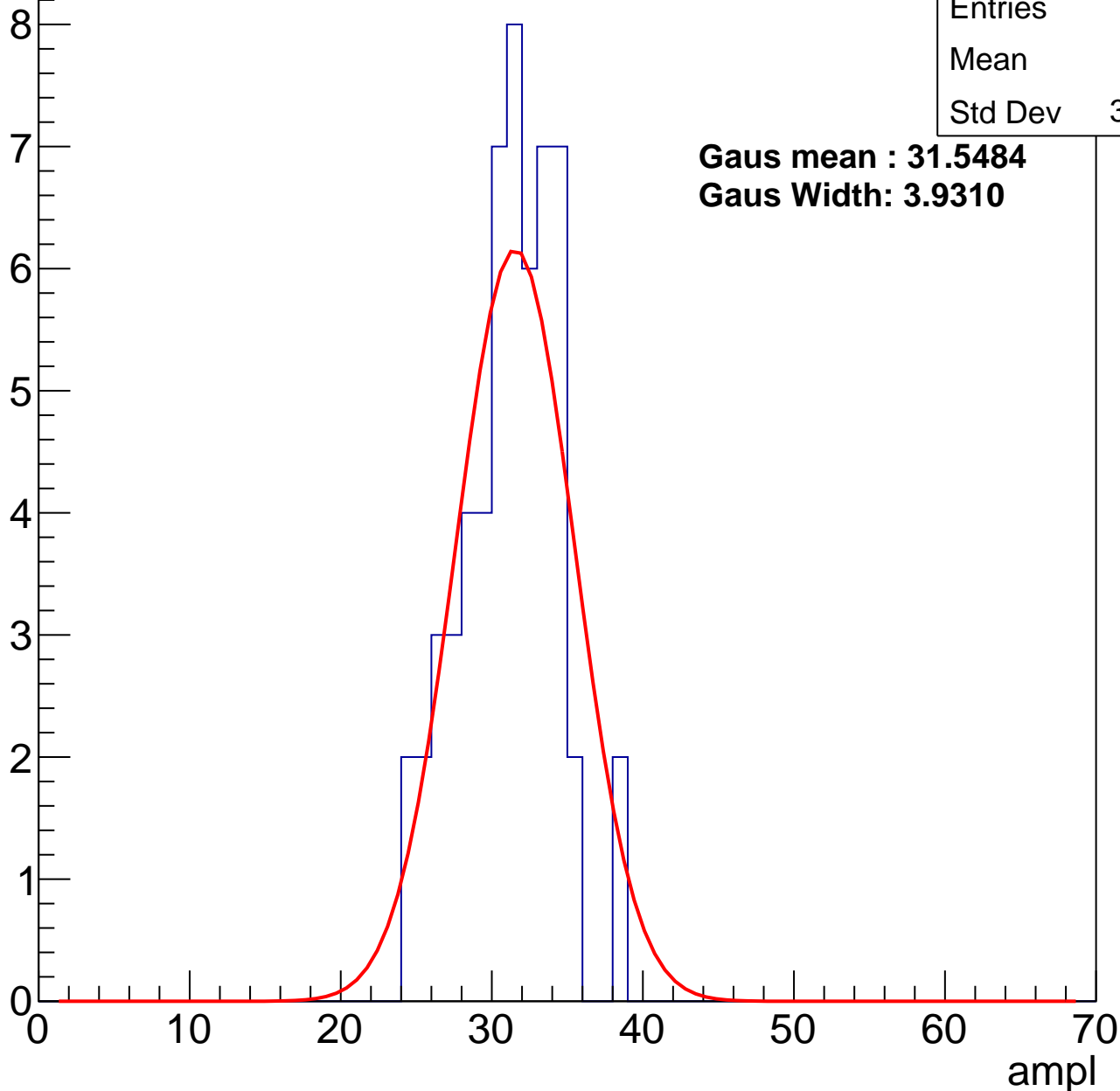
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	57
Mean	30.7
Std Dev	3.173

**Gaus mean : 31.5484**

**Gaus Width: 3.9310**



# B0L000S, U7-ch123, adc1

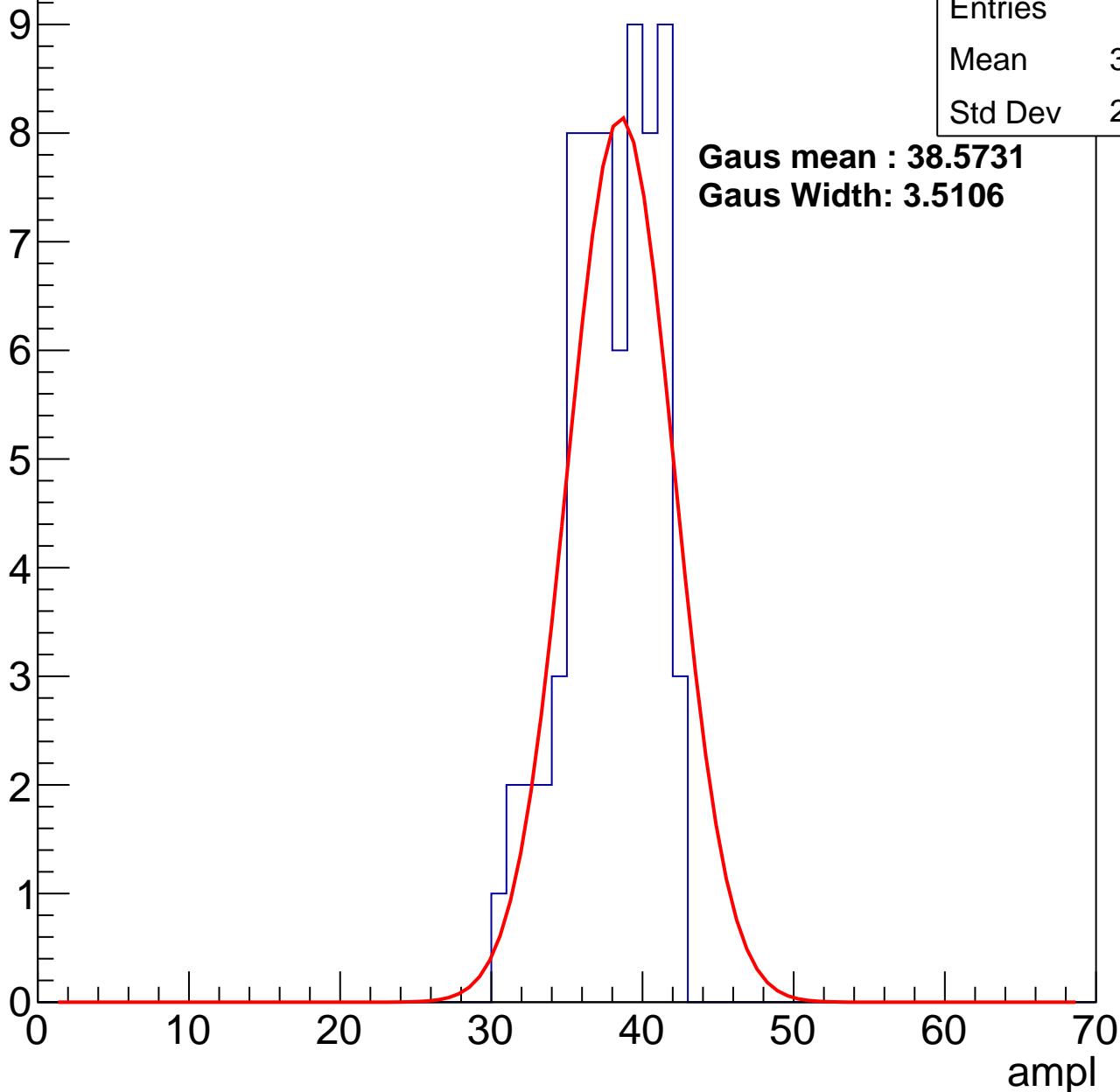
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	69
Mean	37.42
Std Dev	2.926

**Gaus mean : 38.5731**

**Gaus Width: 3.5106**



# B0L000S, U7-ch123, adc2

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	82
Mean	45.13
Std Dev	3.721

**Gaus mean : 45.8008**

**Gaus Width: 3.5149**

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

0

2

4

6

8

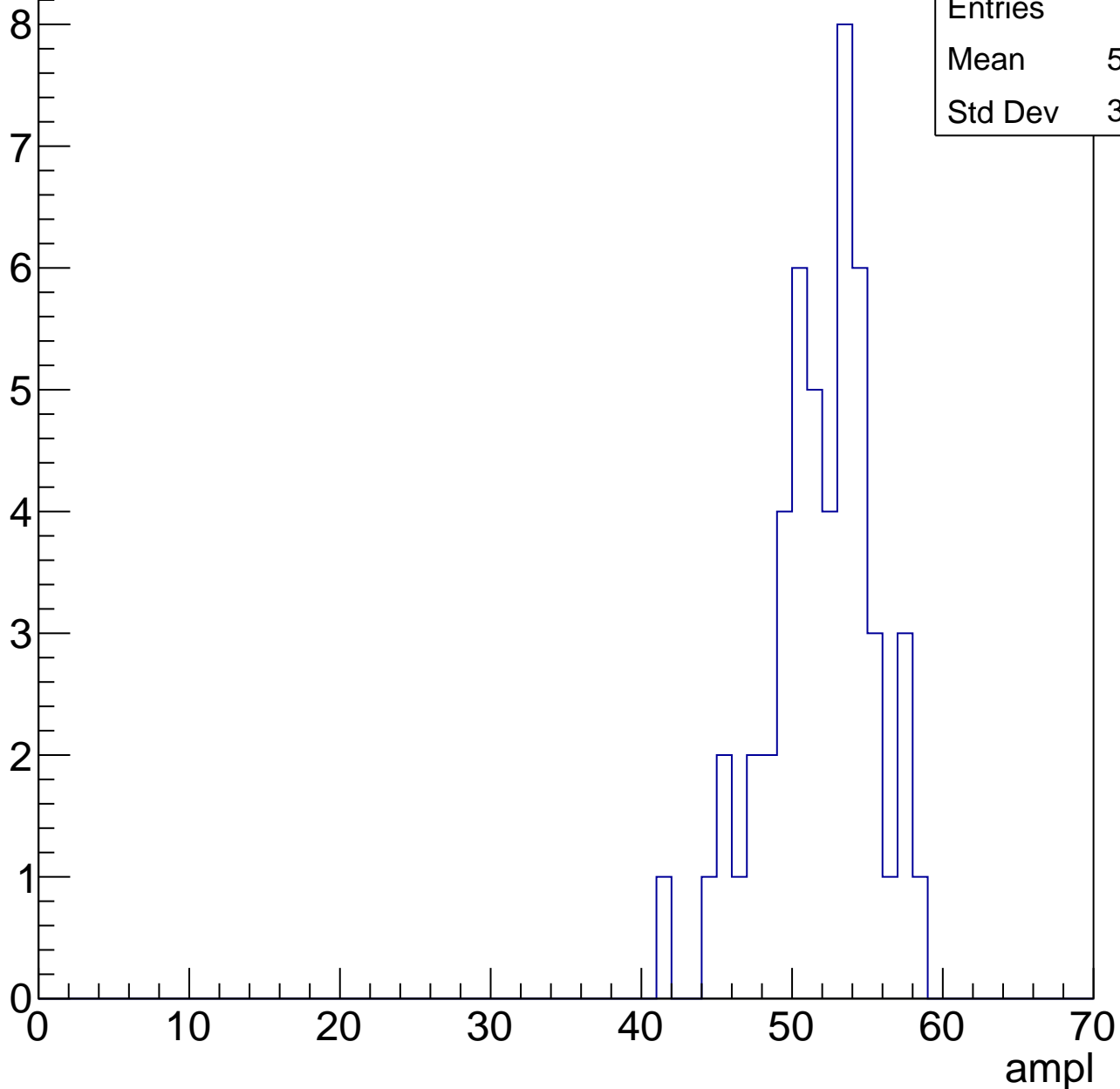
10

# B0L000S, U7-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	50
Mean	51.36
Std Dev	3.554

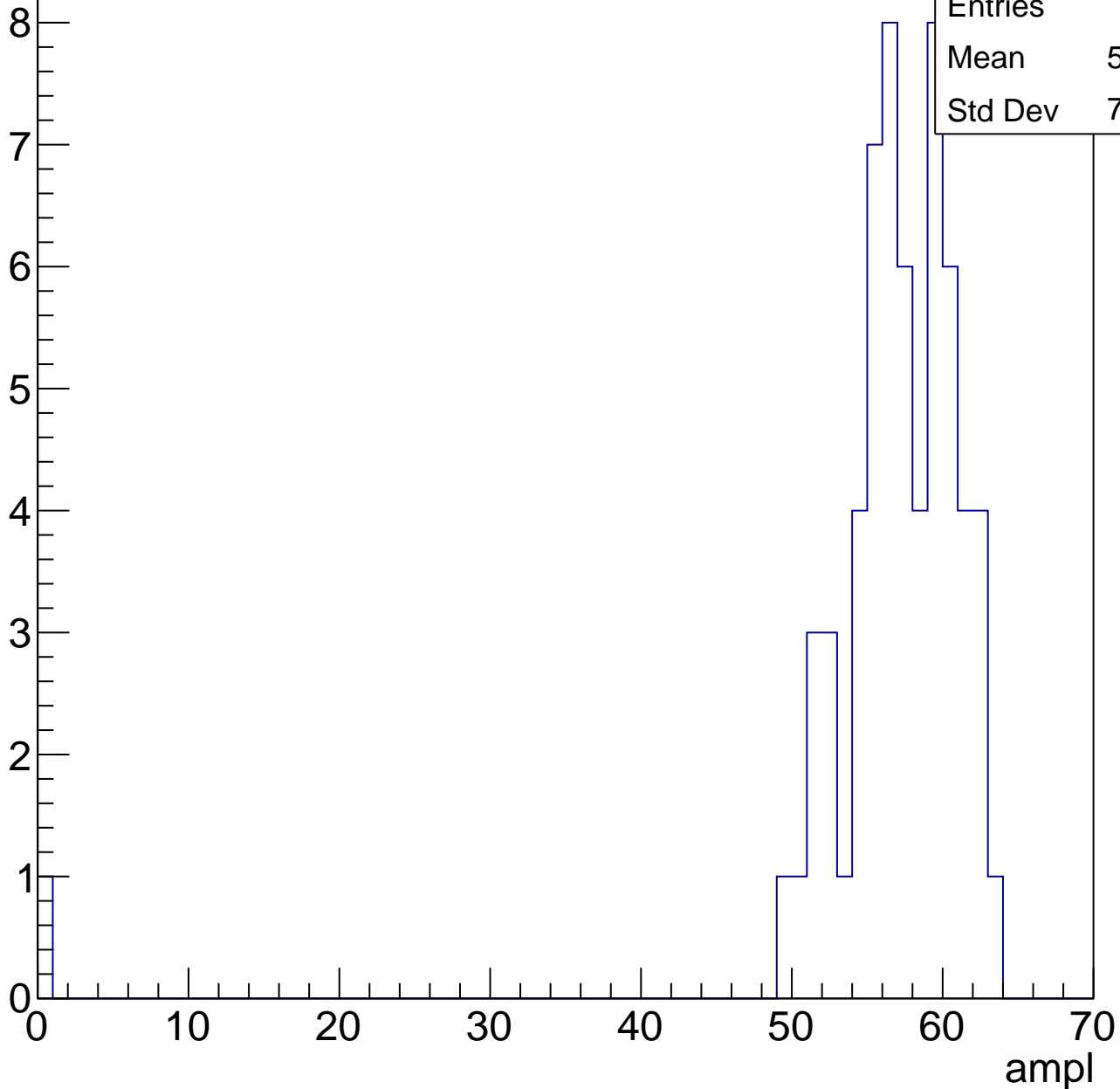


# B0L000S, U7-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	62
Mean	55.98
Std Dev	7.889

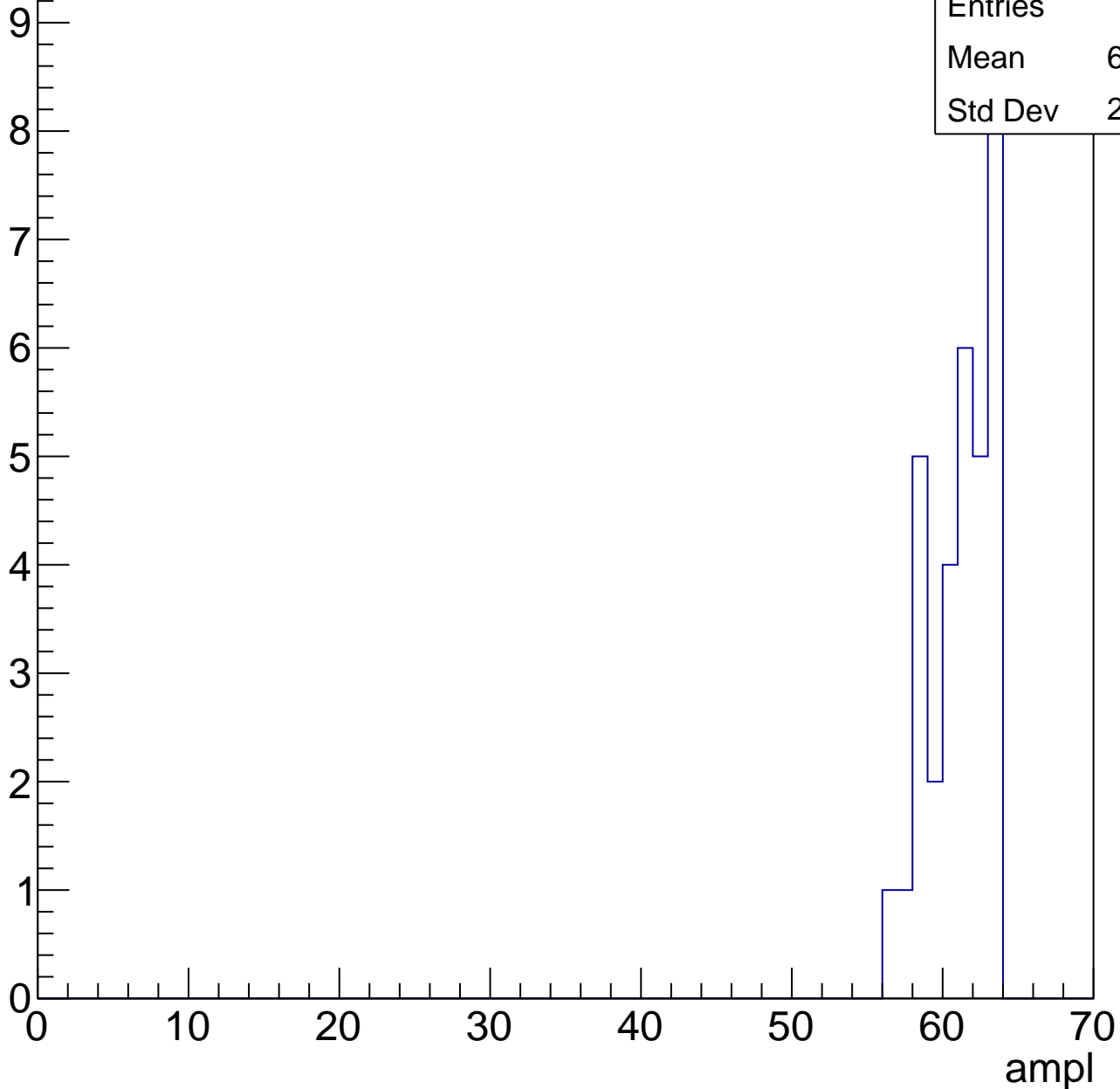


# B0L000S, U7-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	33
Mean	60.73
Std Dev	2.034



# B0L000S, U7-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	1
Mean	23
Std Dev	0

# B0L000S, U7-ch124, adc0

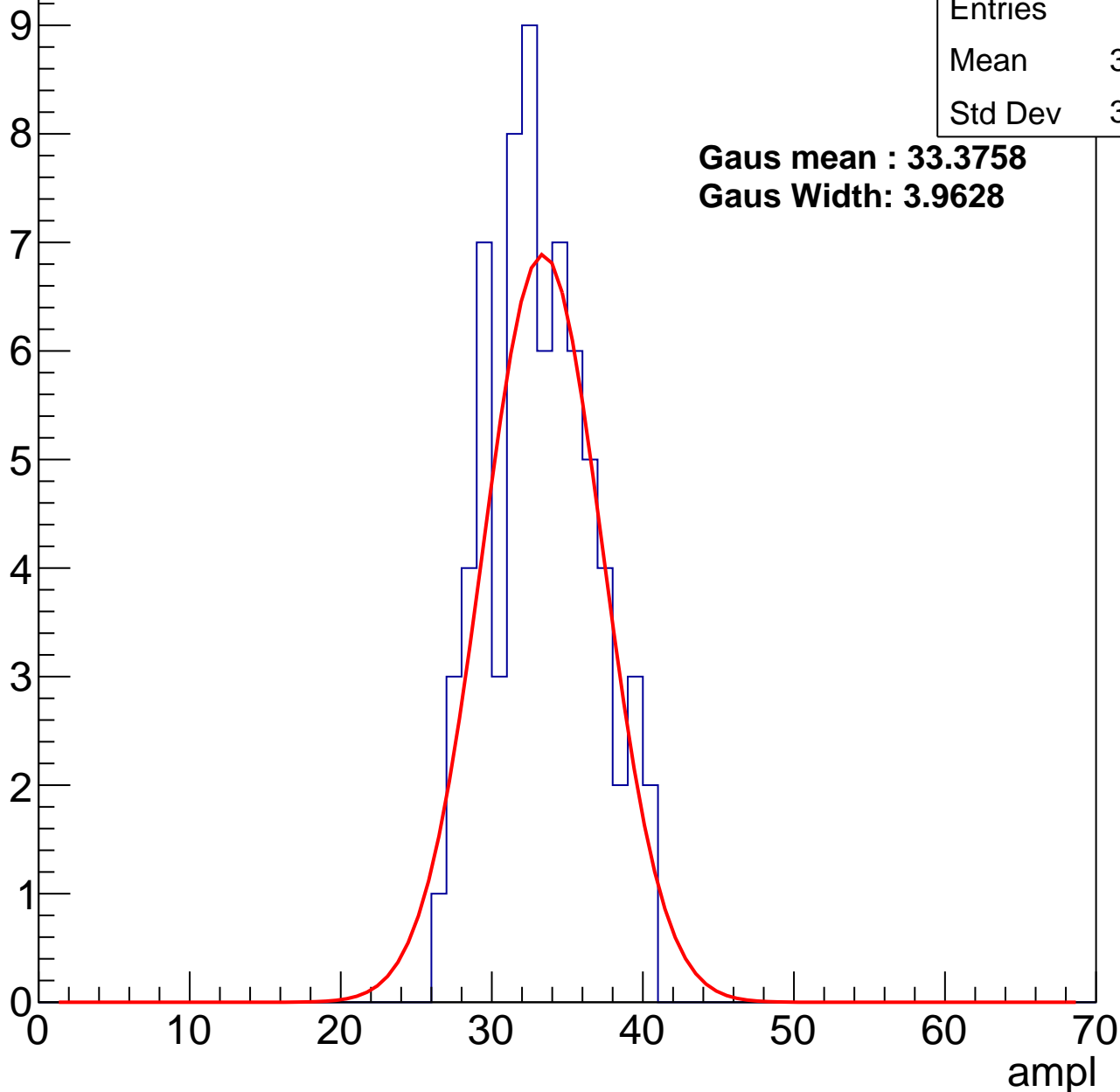
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	70
Mean	32.79
Std Dev	3.443

**Gaus mean : 33.3758**

**Gaus Width: 3.9628**



# B0L000S, U7-ch124, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	59
Mean	39.31
Std Dev	3.586

7

6

5

4

3

2

1

0

0

10

20

30

40

50

60

70

ampl

**Gaus mean : 40.0540**

**Gaus Width: 3.7999**

0

1

2

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302

303

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305

&lt;

# B0L000S, U7-ch124, adc2

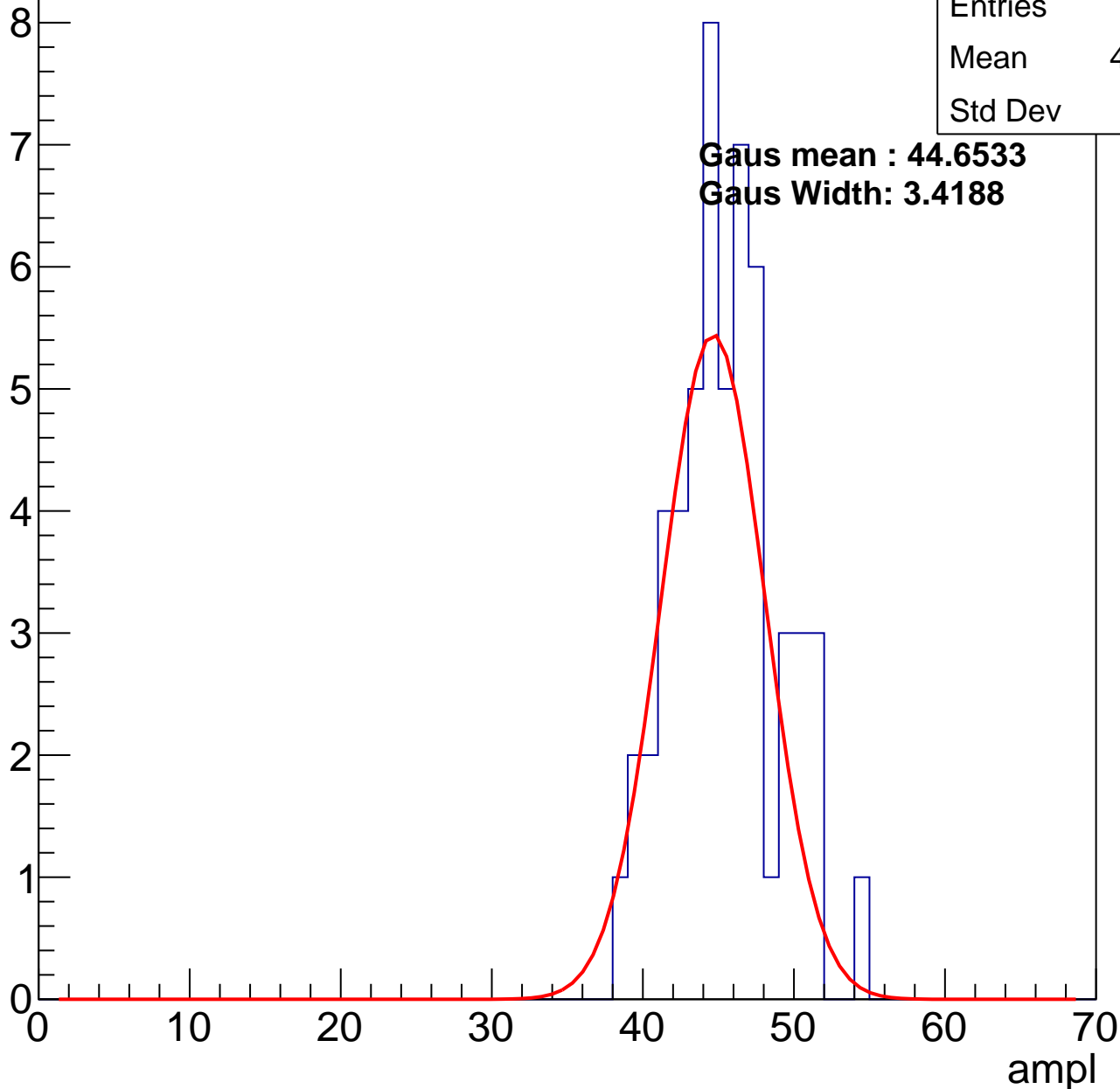
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	55
Mean	45.02
Std Dev	3.44

**Gaus mean : 44.6533**

**Gaus Width: 3.4188**

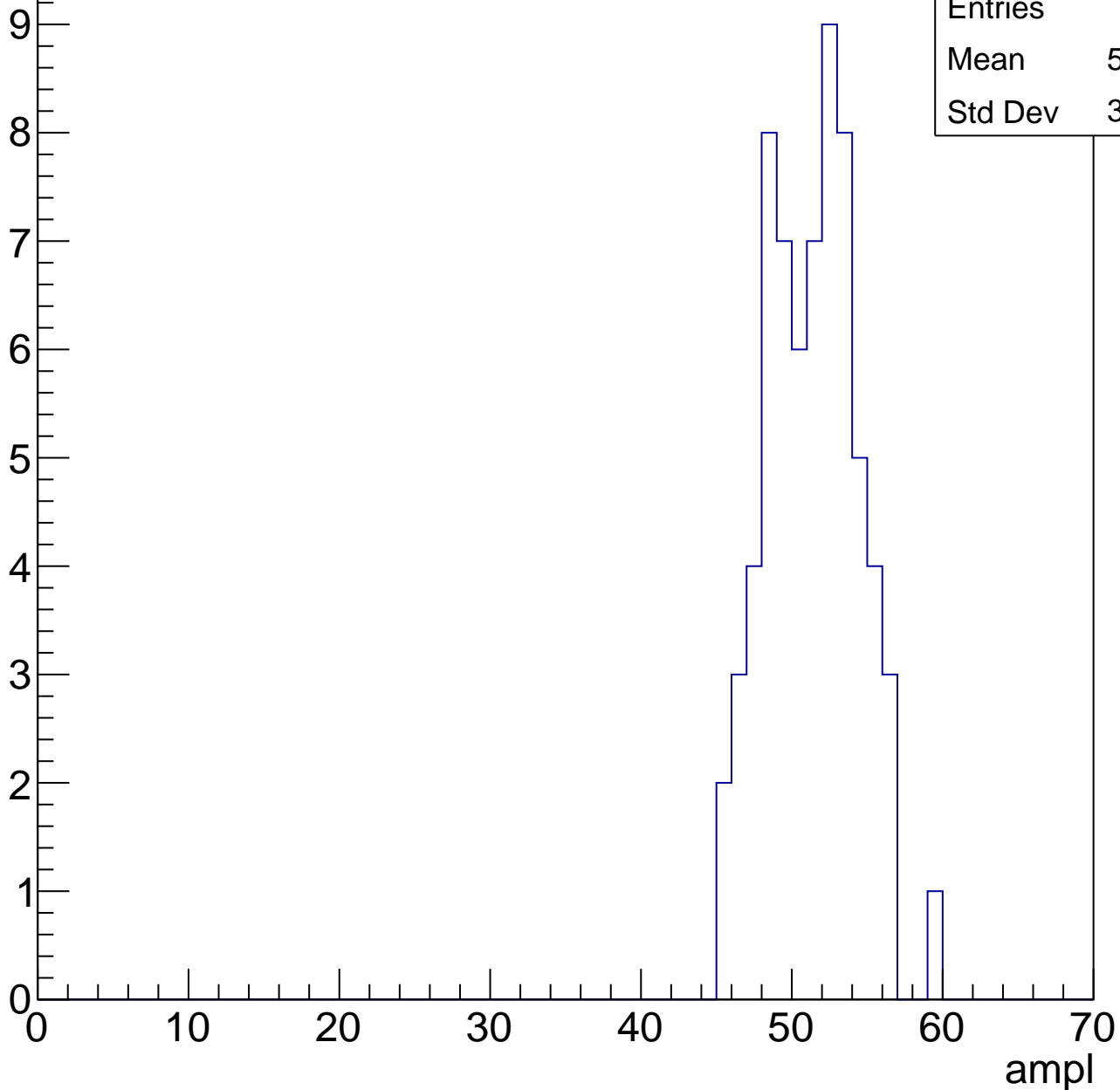


# B0L000S, U7-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	67
Mean	50.88
Std Dev	3.005

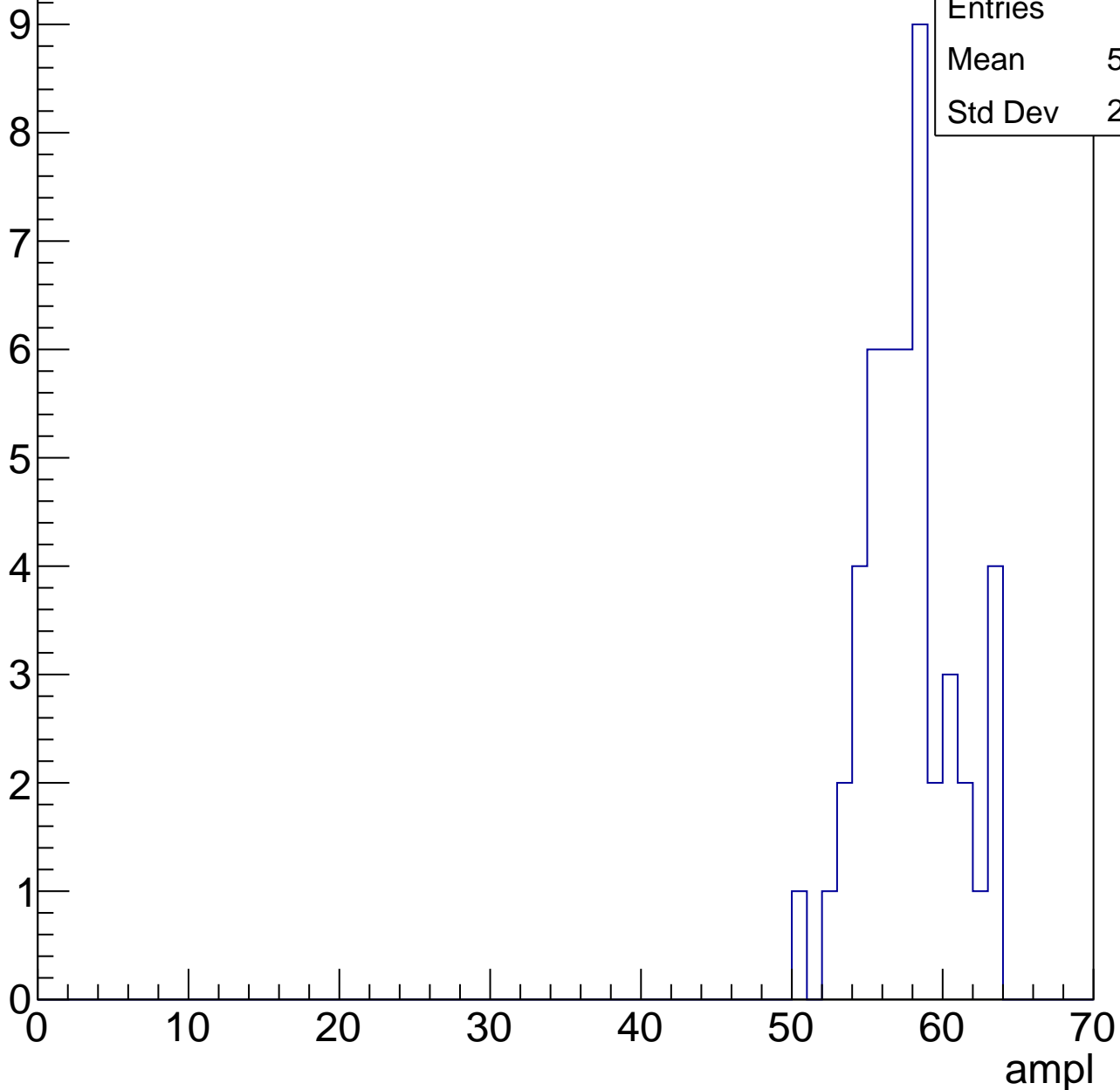


# B0L000S, U7-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	47
Mean	57.19
Std Dev	2.972

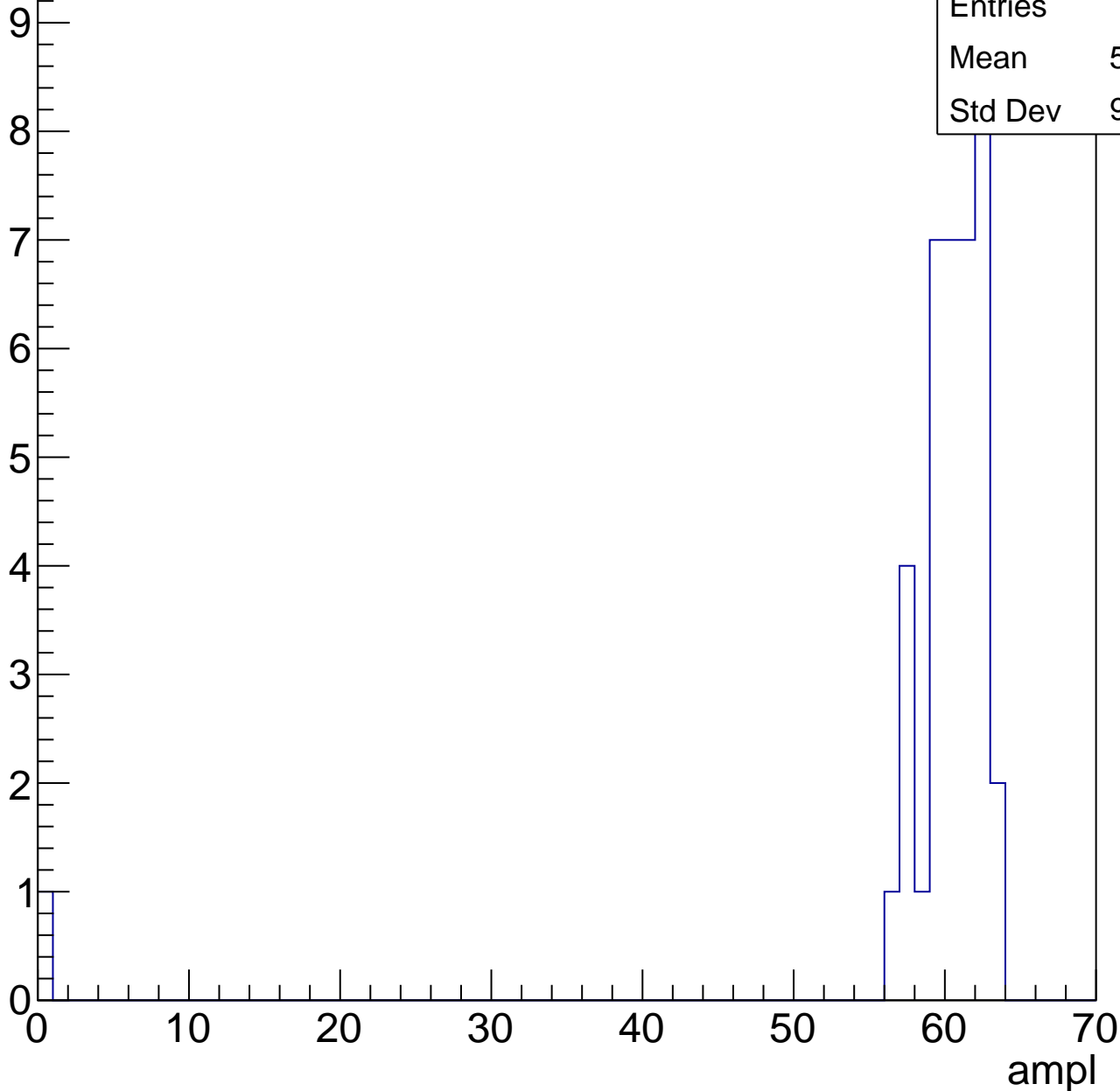


# B0L000S, U7-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

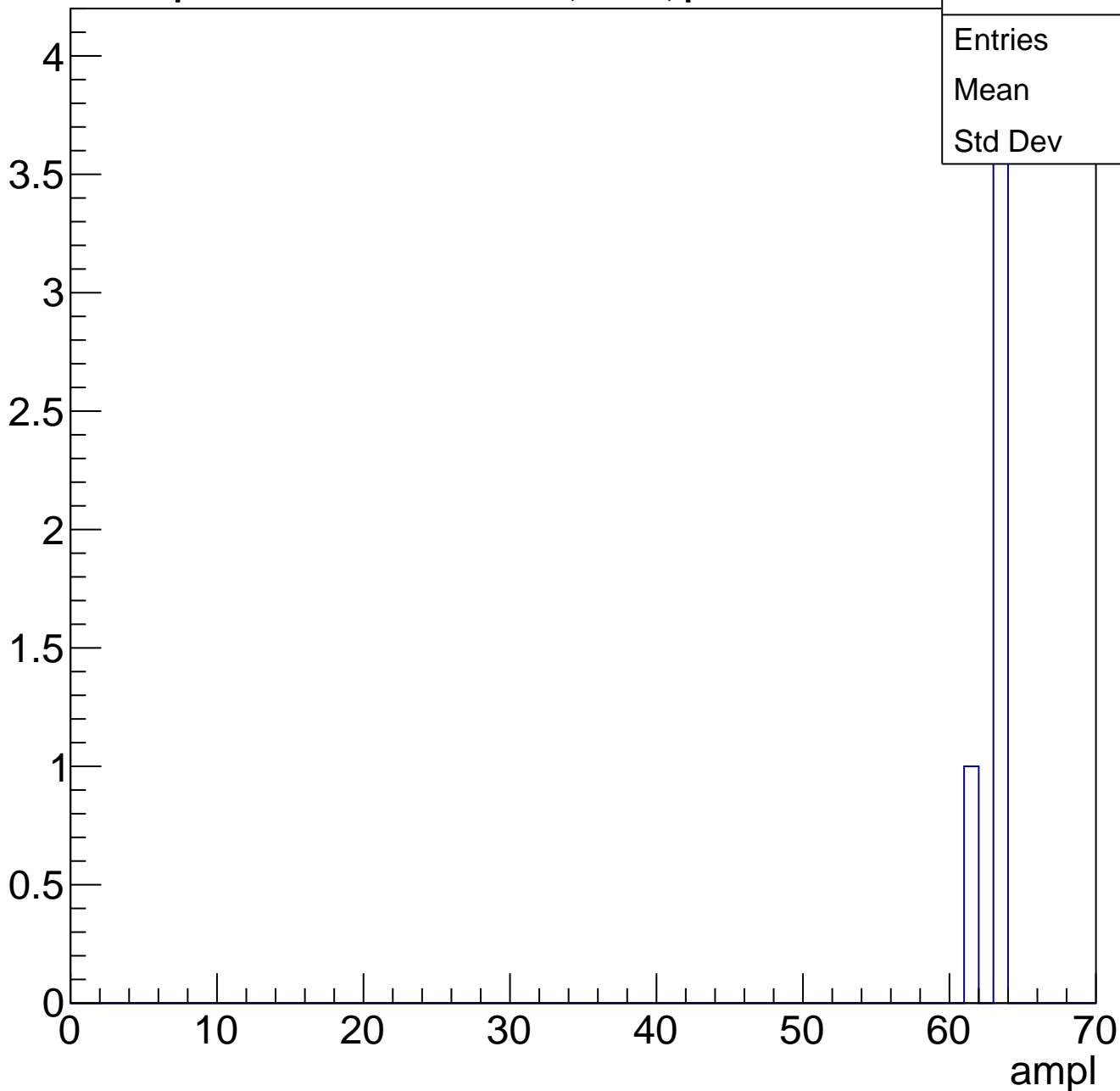
Entries	39
Mean	58.62
Std Dev	9.673



# B0L000S, U7-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L000S, U7-ch125, adc0

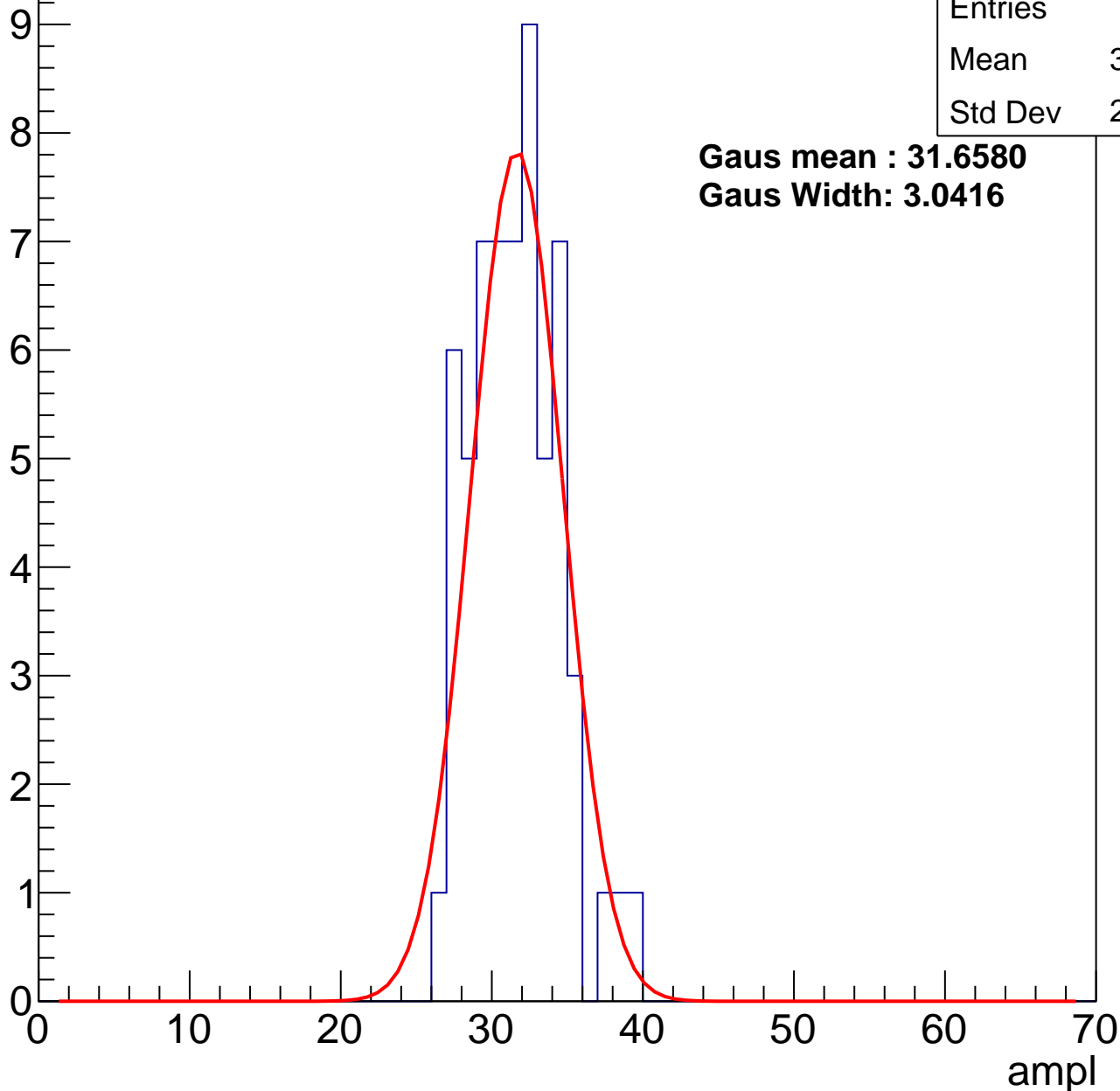
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	60
Mean	31.13
Std Dev	2.855

**Gaus mean : 31.6580**

**Gaus Width: 3.0416**

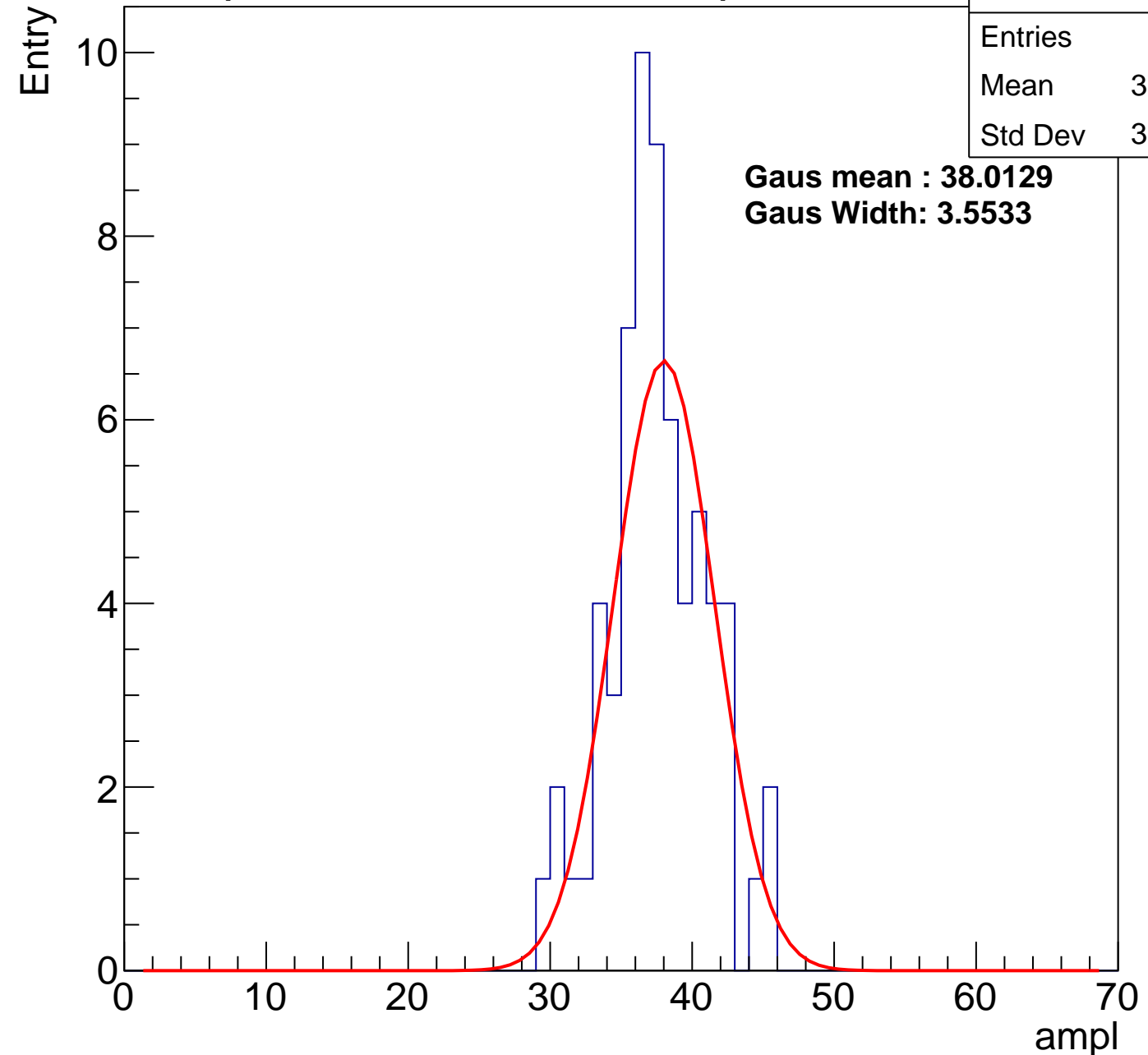


# B0L000S, U7-ch125, adc1

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	64
Mean	37.09
Std Dev	3.445

**Gaus mean : 38.0129**  
**Gaus Width: 3.5533**



# B0L000S, U7-ch125, adc2

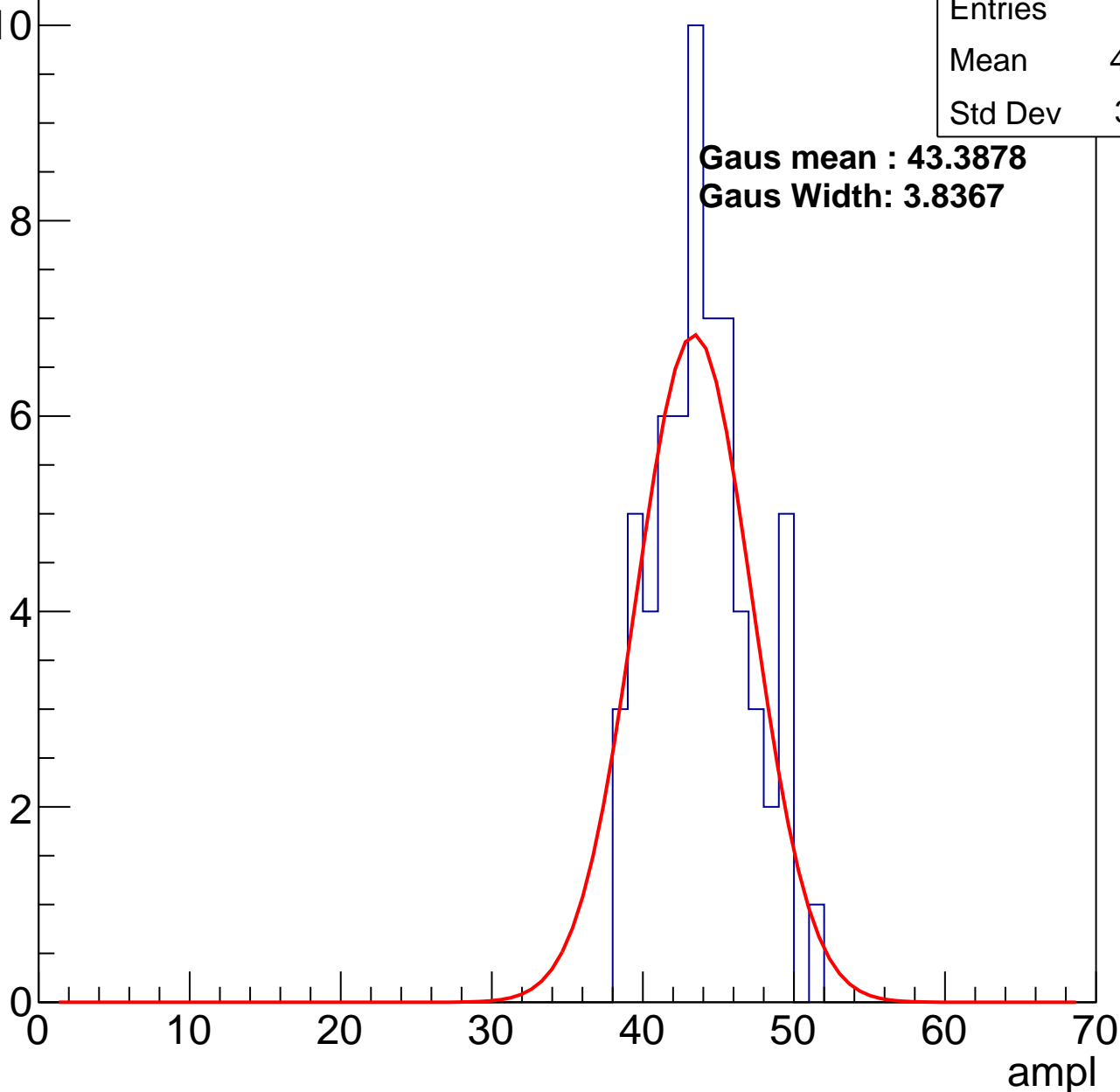
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	63
Mean	43.44
Std Dev	3.141

**Gaus mean : 43.3878**

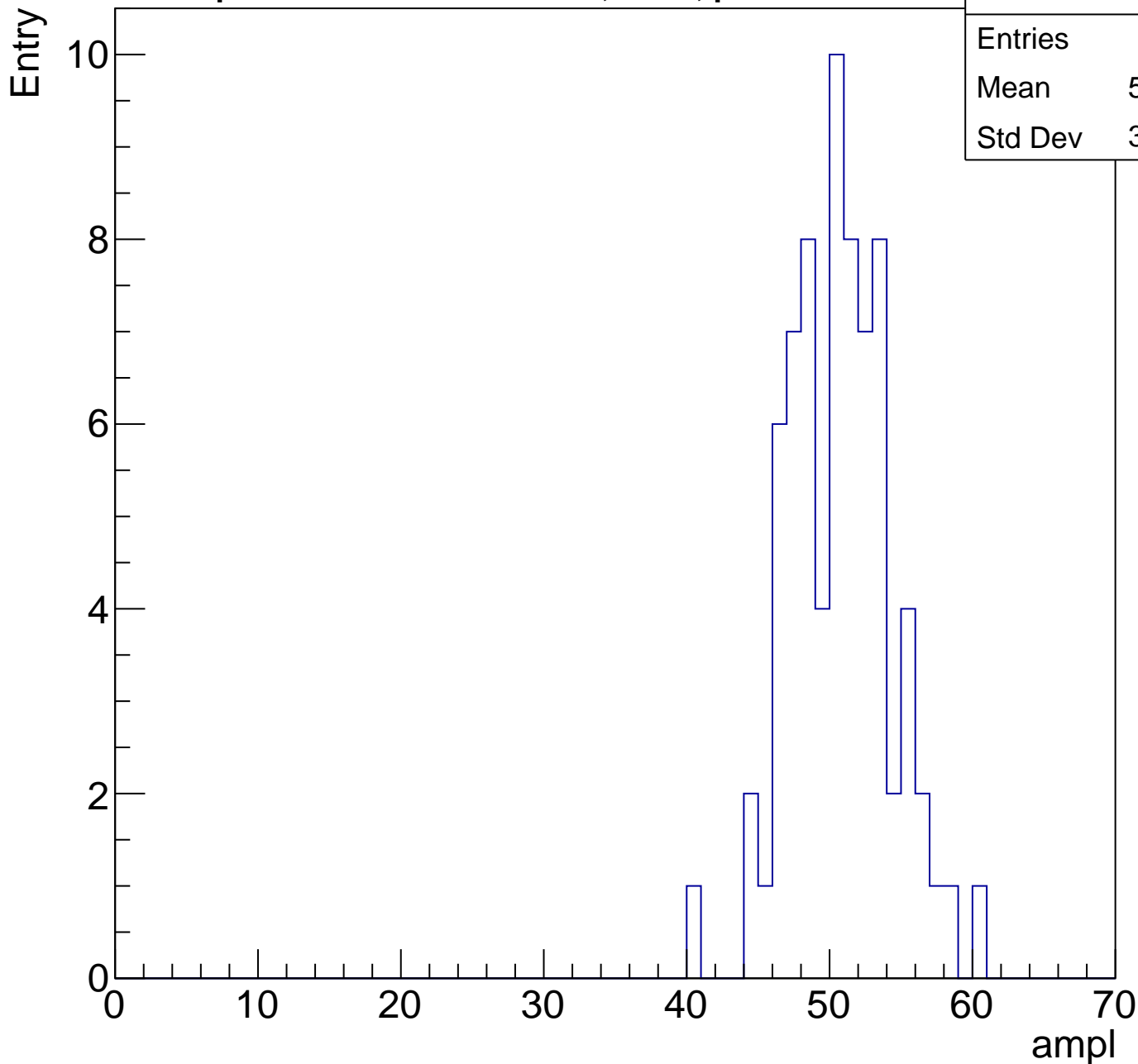
**Gaus Width: 3.8367**



# B0L000S, U7-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	73
Mean	50.26
Std Dev	3.535

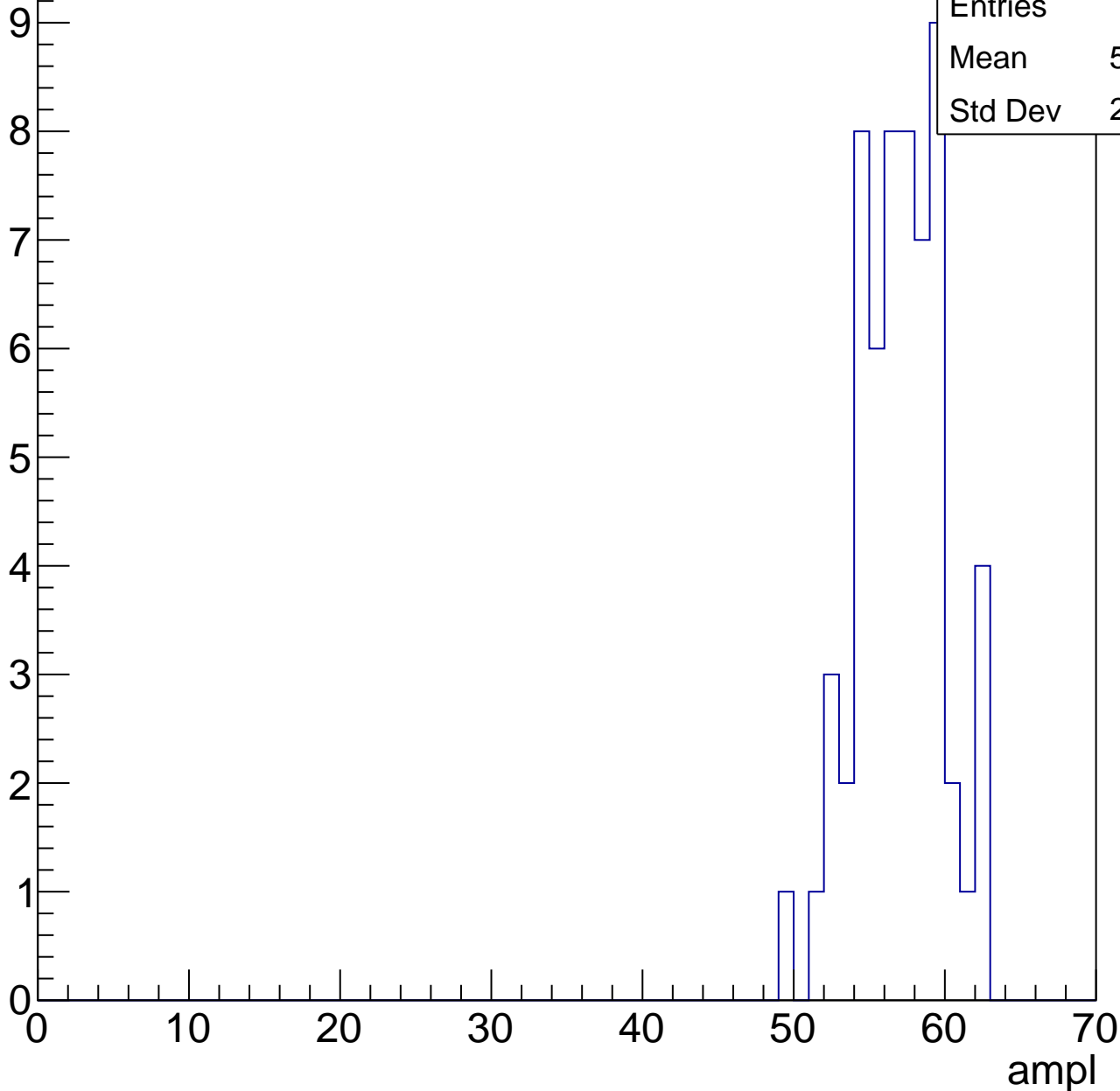


# B0L000S, U7-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	60
Mean	56.57
Std Dev	2.819

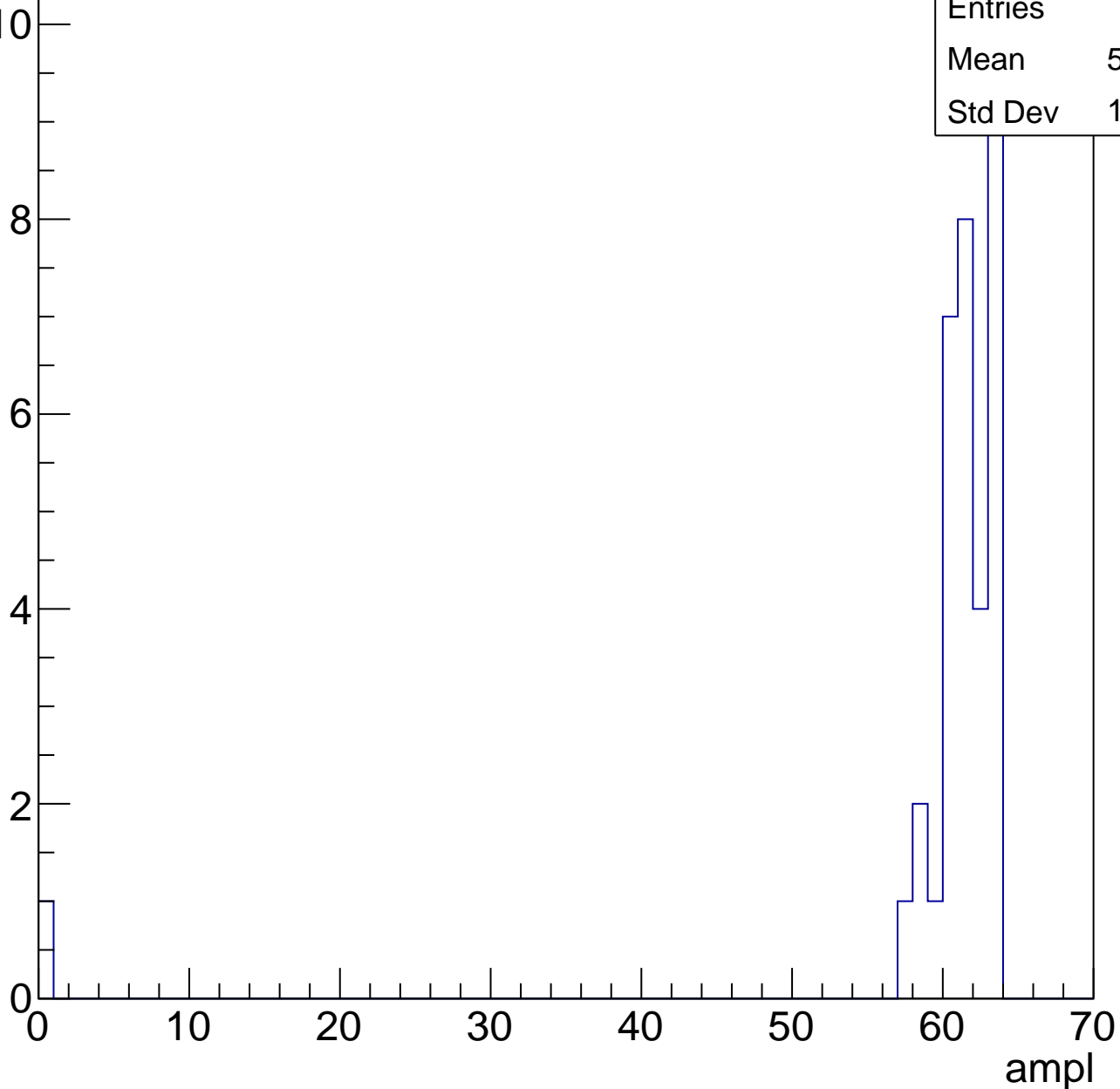


# B0L000S, U7-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	34
Mean	59.35
Std Dev	10.46



# B0L000S, U7-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

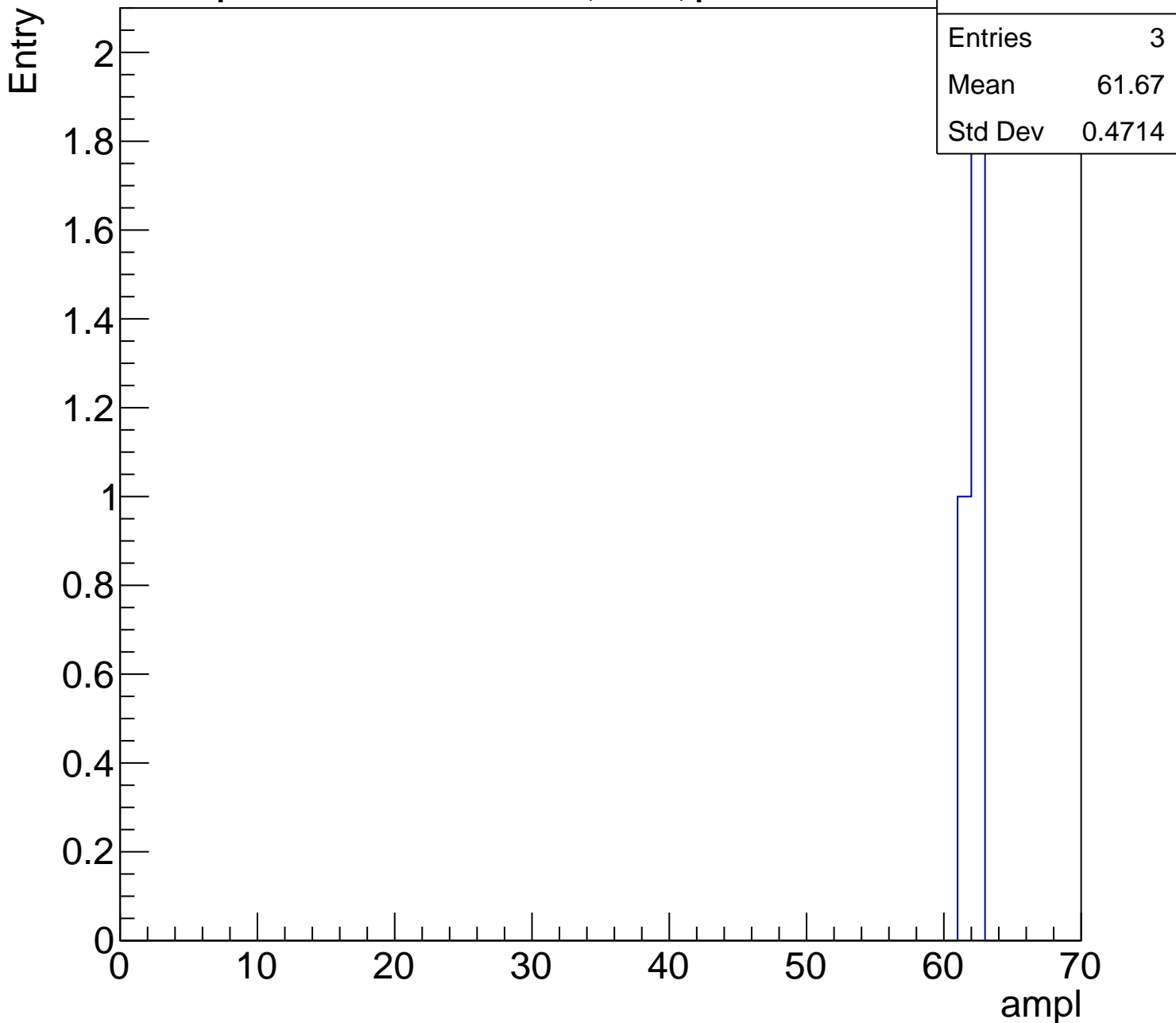
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	61.67
Std Dev	0.4714

0 10 20 30 40 50 60 70

ampl

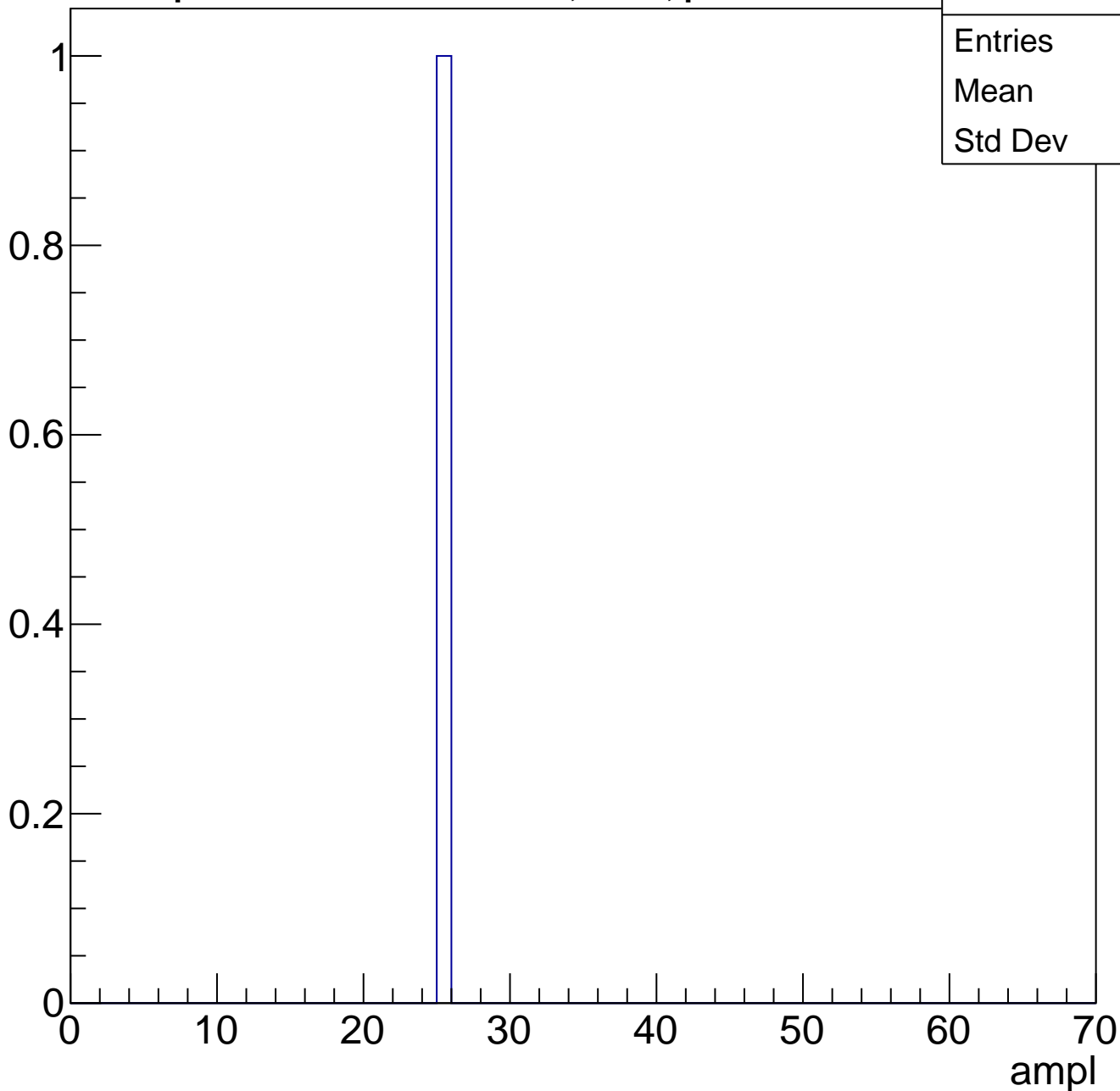




# B0L000S, U7-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



# B0L000S, U7-ch126, adc0

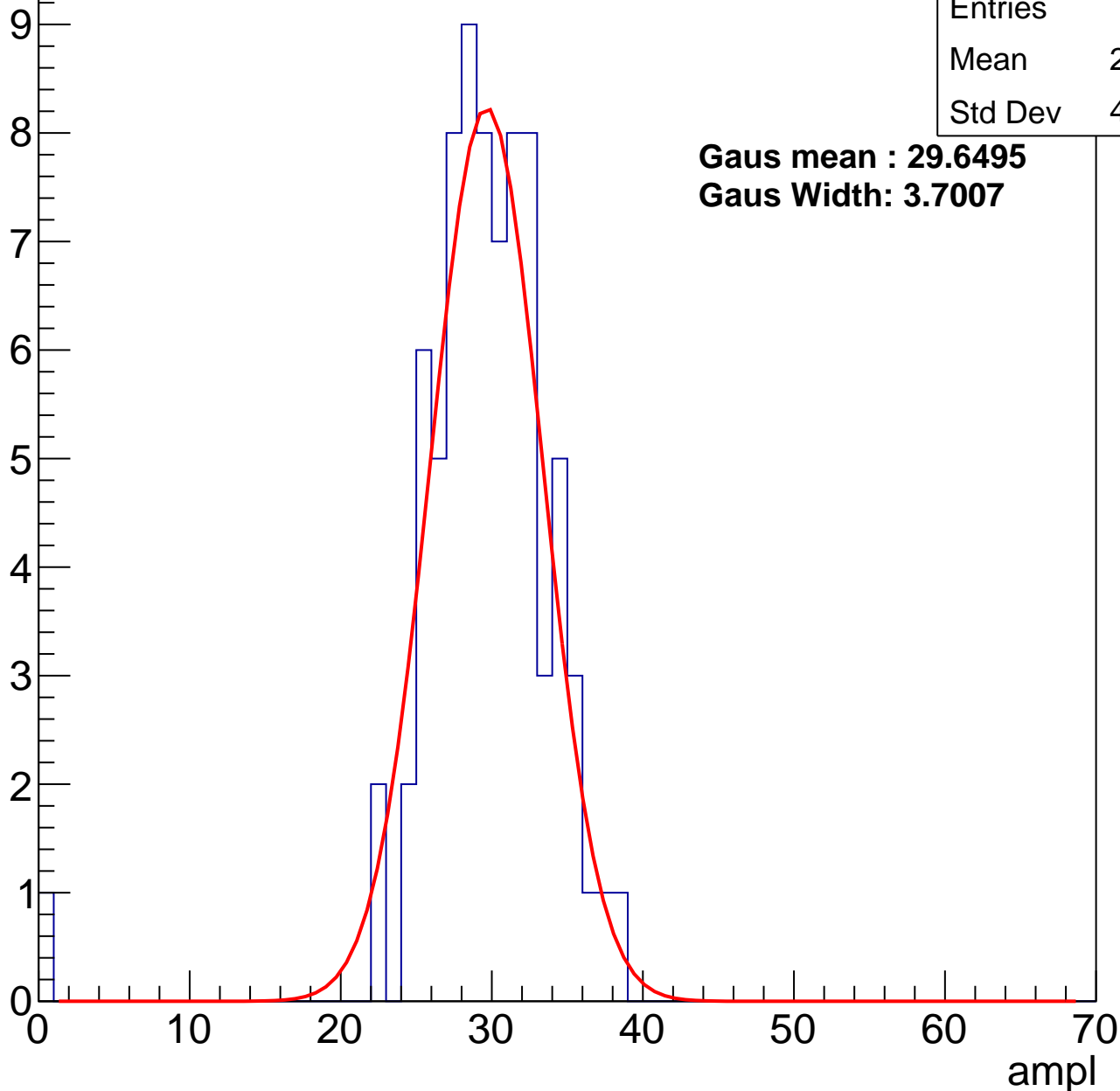
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	78
Mean	29.12
Std Dev	4.745

**Gaus mean : 29.6495**

**Gaus Width: 3.7007**



# B0L000S, U7-ch126, adc1

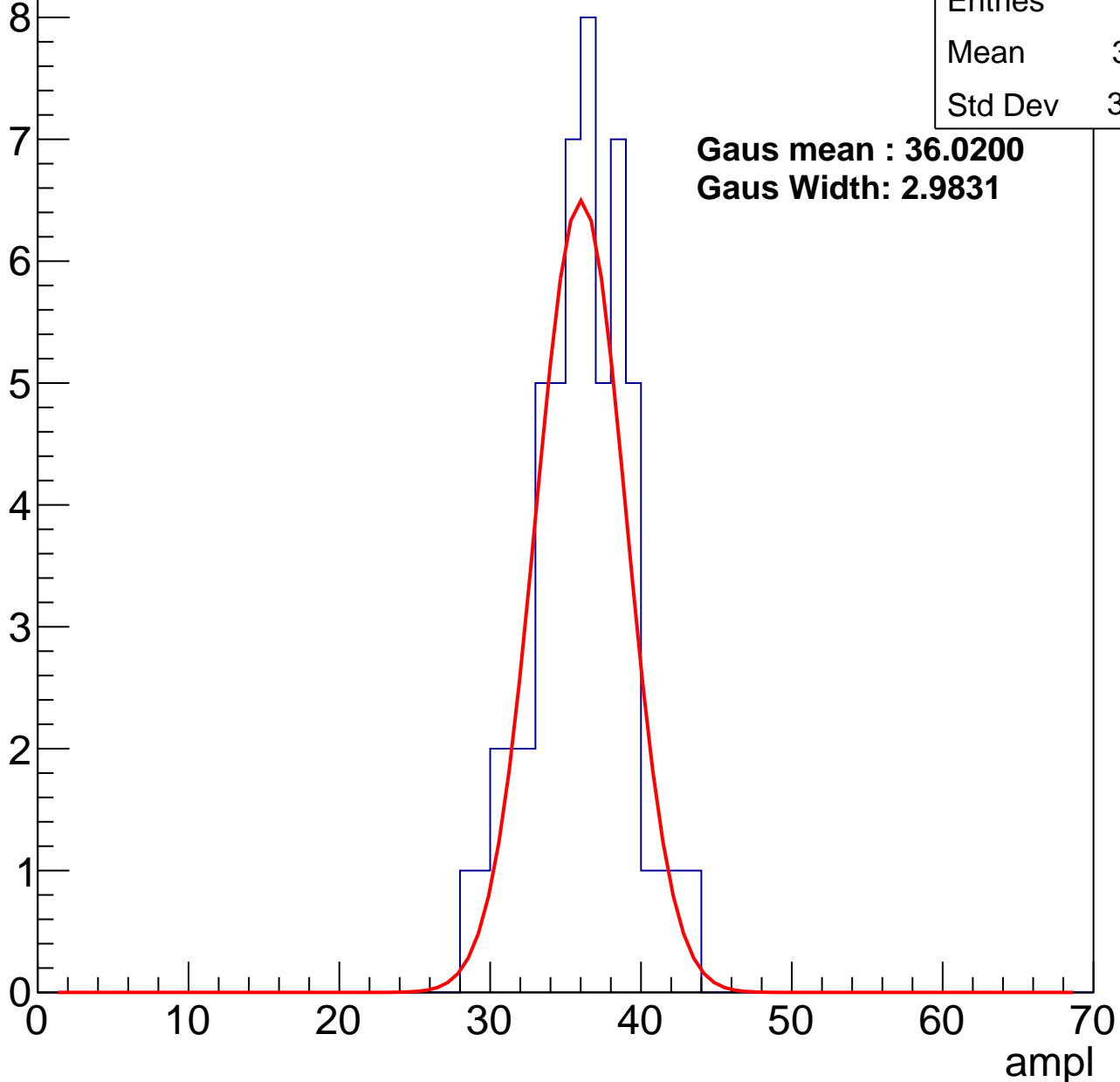
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	54
Mean	35.61
Std Dev	3.147

**Gaus mean : 36.0200**

**Gaus Width: 2.9831**



# B0L000S, U7-ch126, adc2

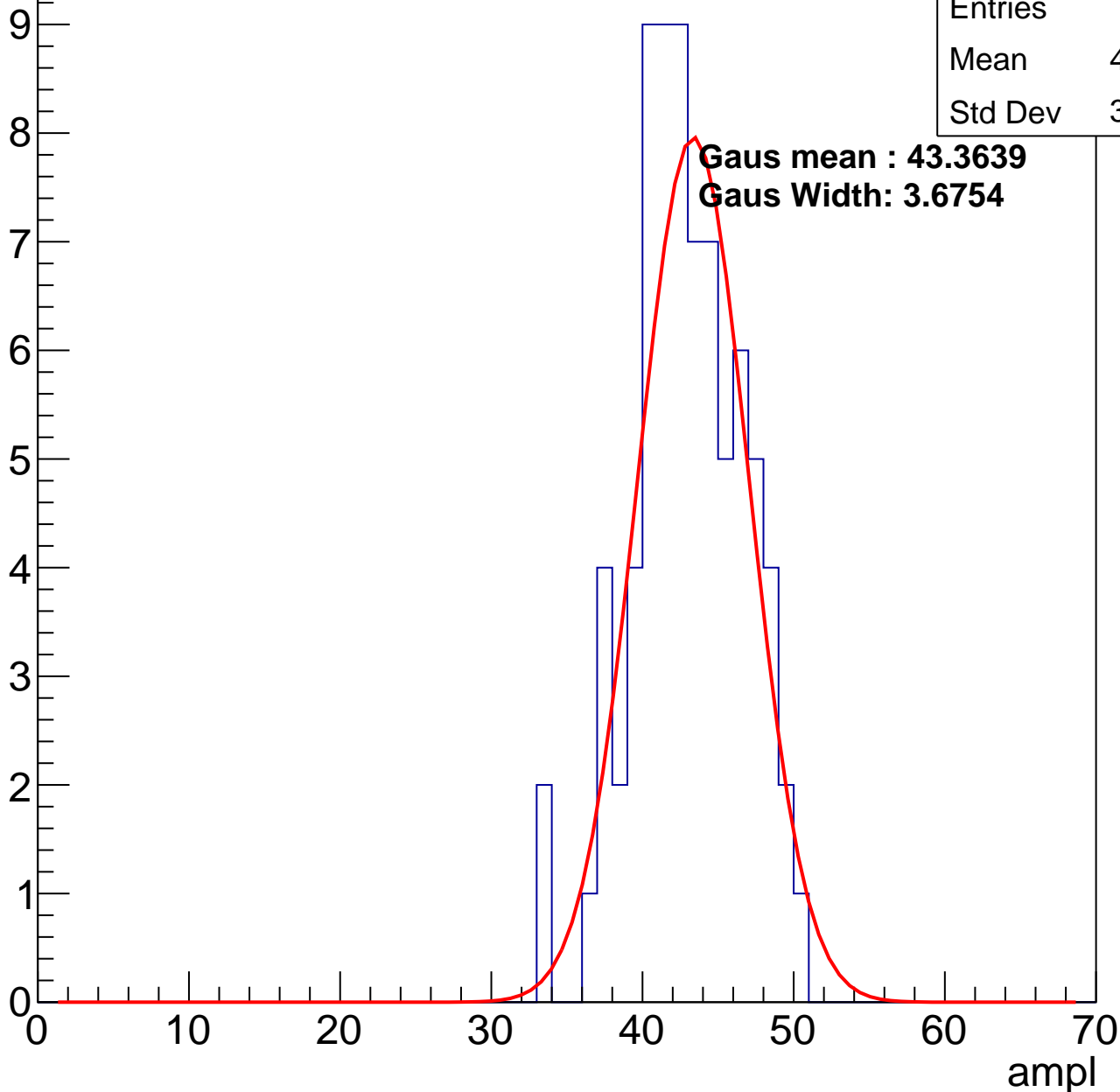
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	77
Mean	42.52
Std Dev	3.599

**Gaus mean : 43.3639**

**Gaus Width: 3.6754**

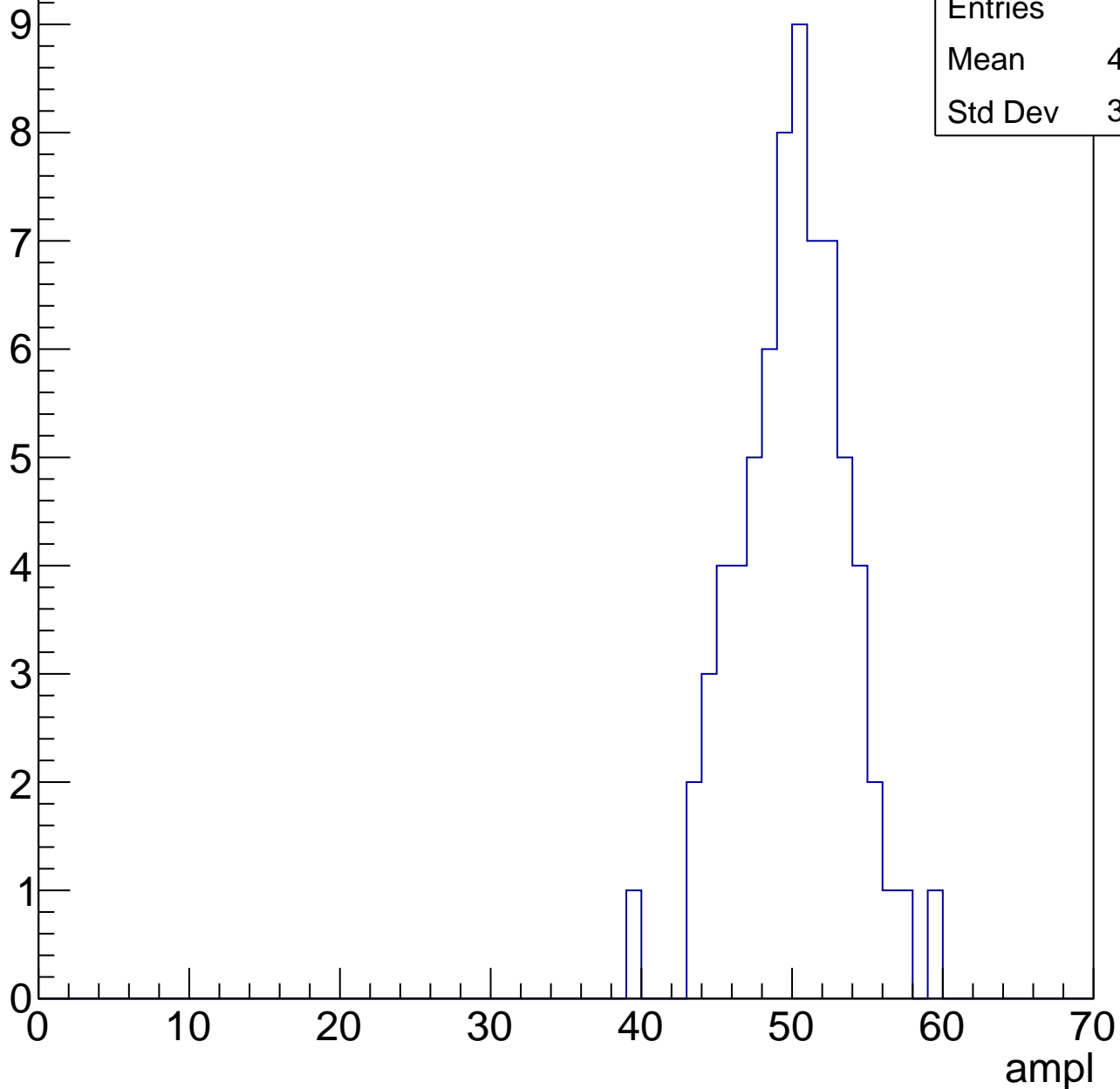


# B0L000S, U7-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	70
Mean	49.57
Std Dev	3.616

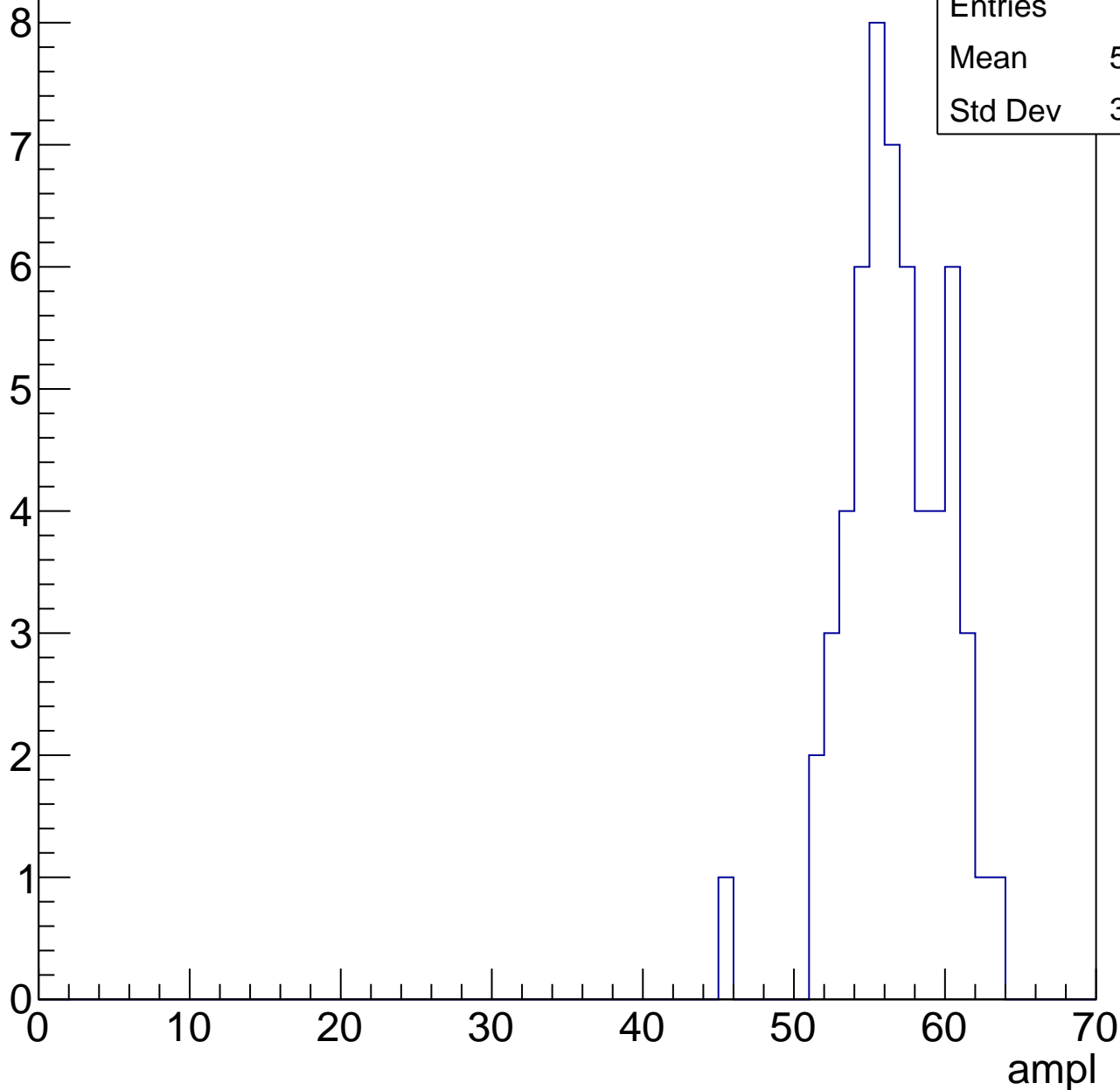


# B0L000S, U7-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	56
Mean	56.23
Std Dev	3.268

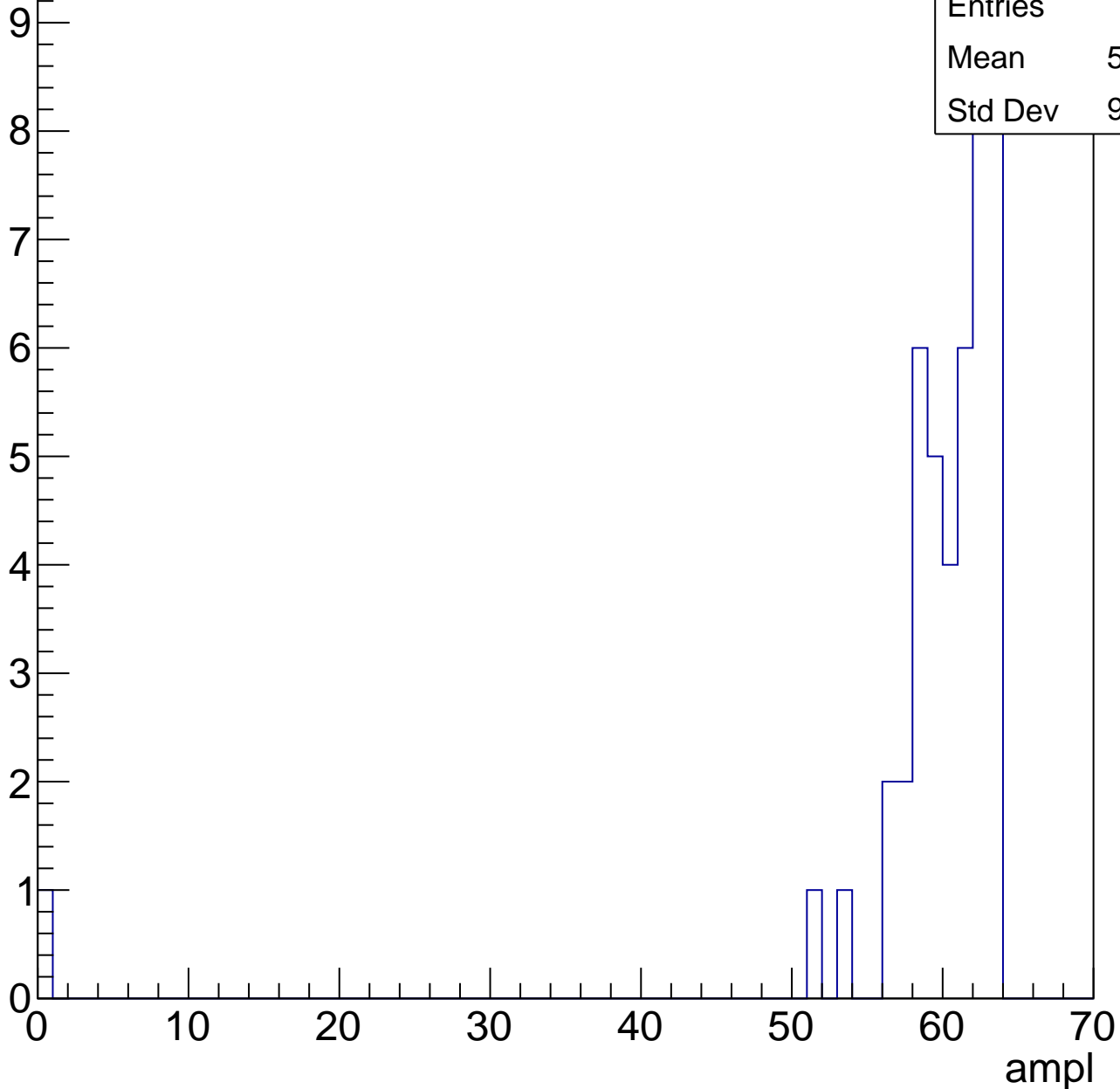


# B0L000S, U7-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

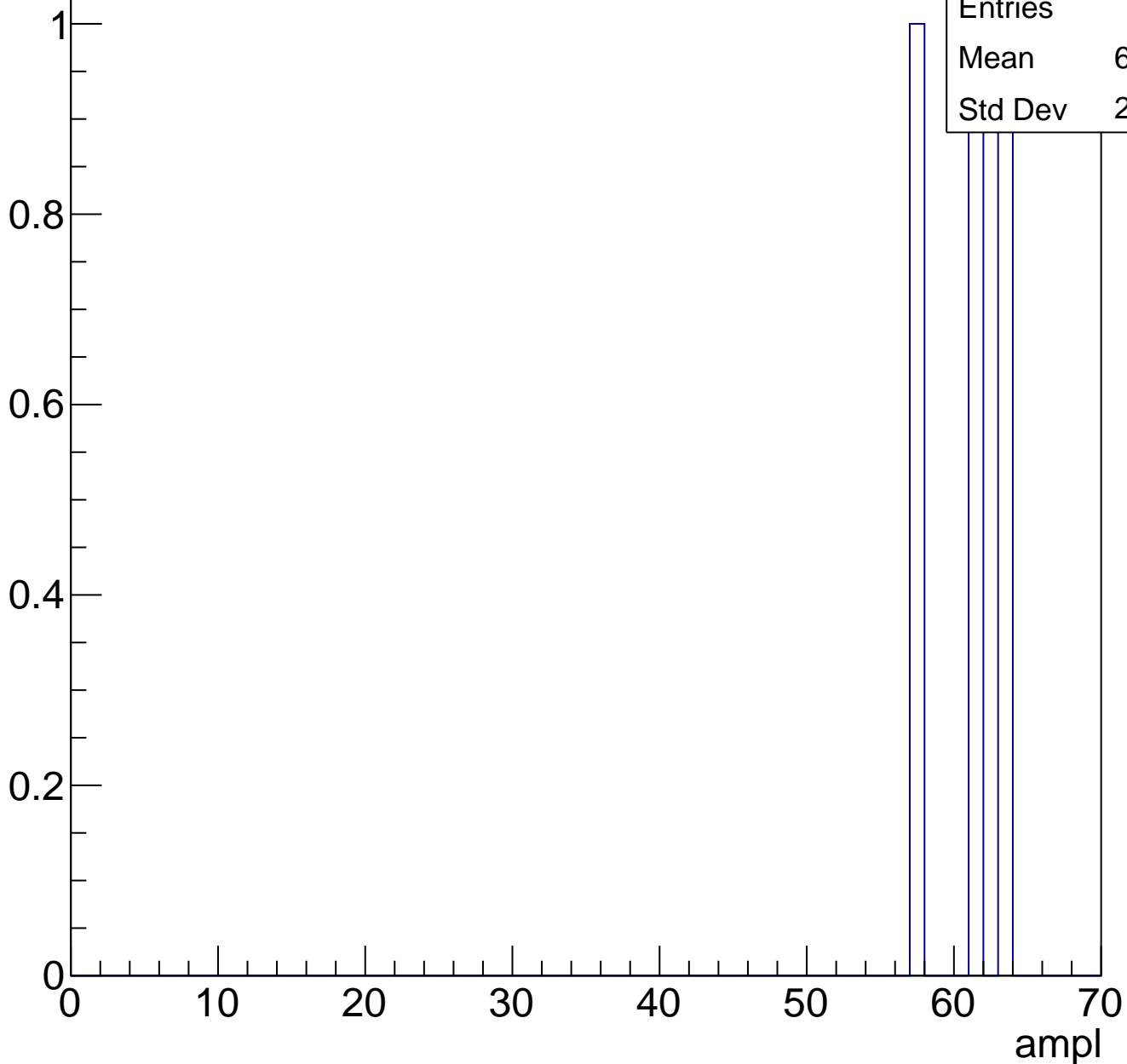
Entries	45
Mean	58.69
Std Dev	9.244



# B0L000S, U7-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry





# B0L000S, U7-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L000S, U7-ch127, adc0

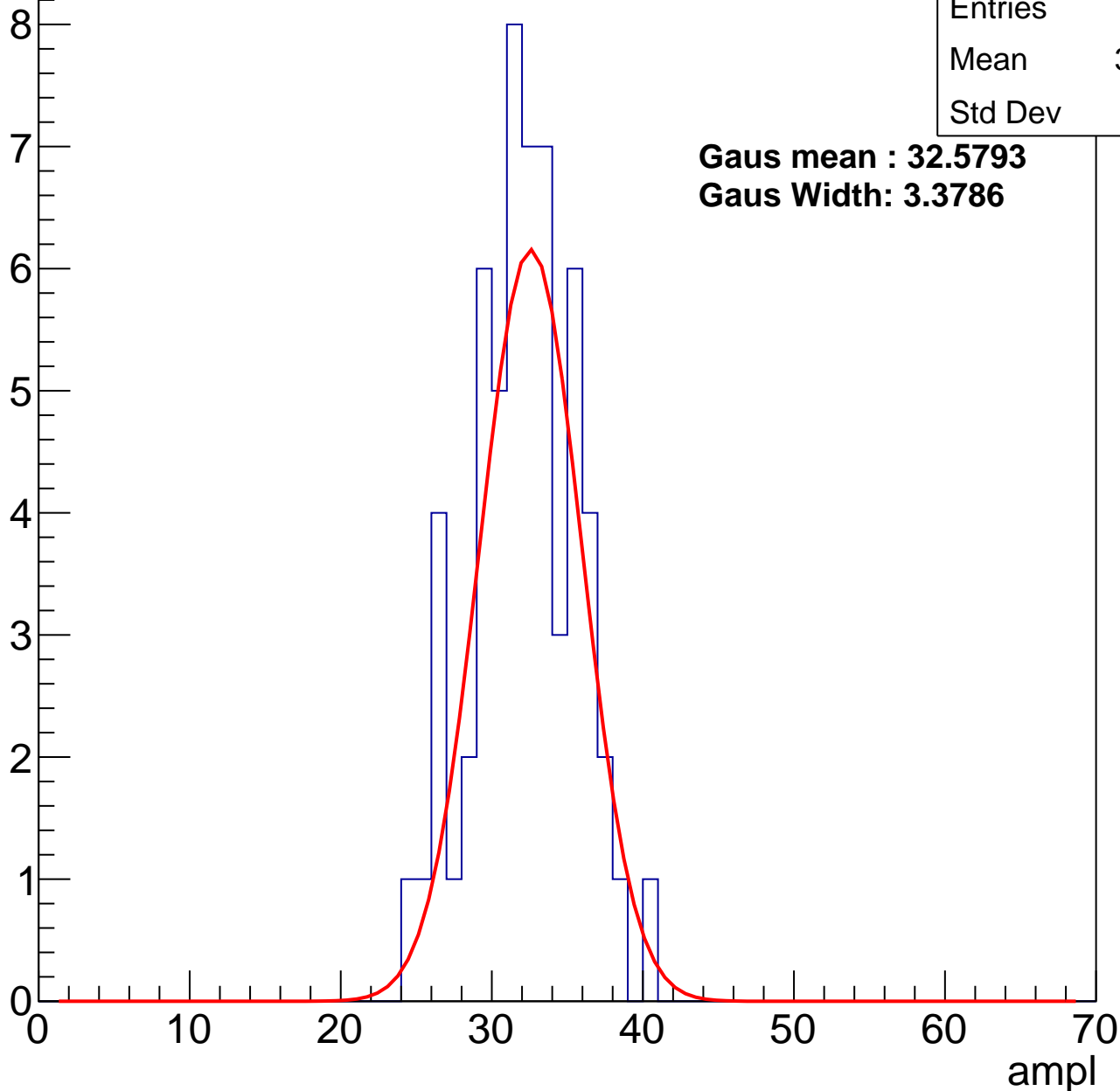
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	59
Mean	31.71
Std Dev	3.39

**Gaus mean : 32.5793**

**Gaus Width: 3.3786**



# B0L000S, U7-ch127, adc1

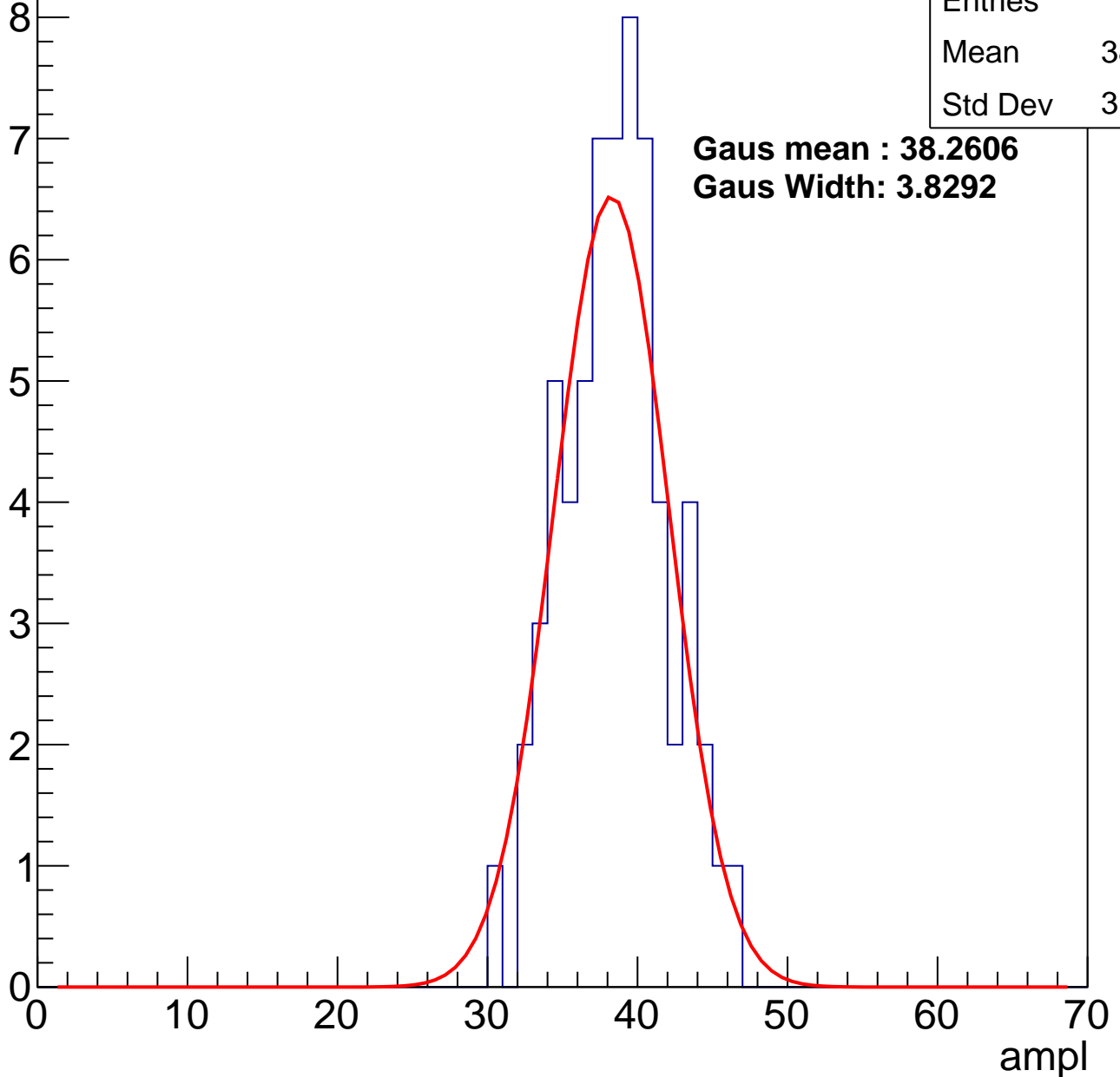
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	63
Mean	38.08
Std Dev	3.433

**Gaus mean : 38.2606**

**Gaus Width: 3.8292**



# B0L000S, U7-ch127, adc2

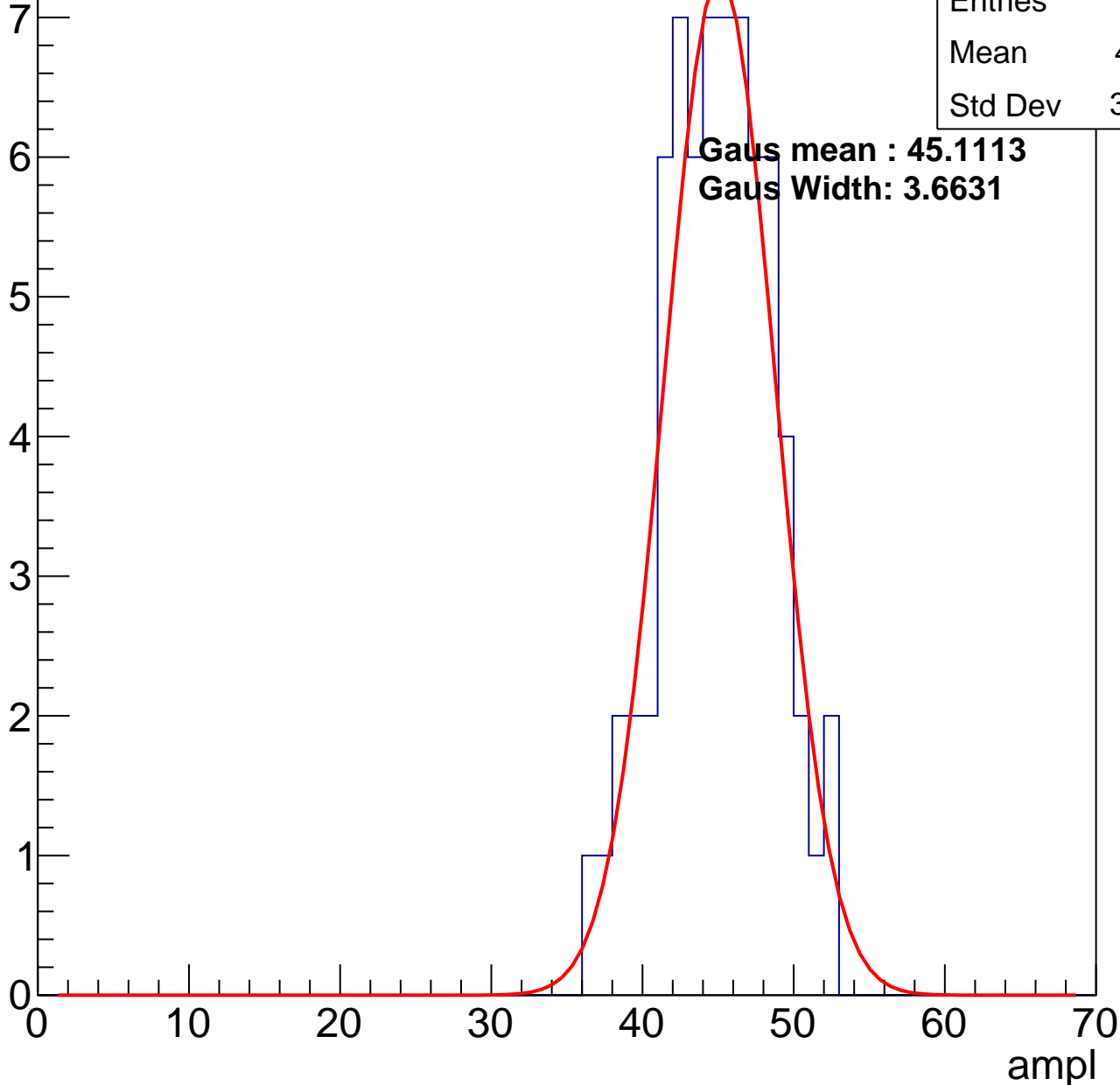
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	69
Mean	44.51
Std Dev	3.553

Gaus mean : 45.1113

Gaus Width: 3.6631

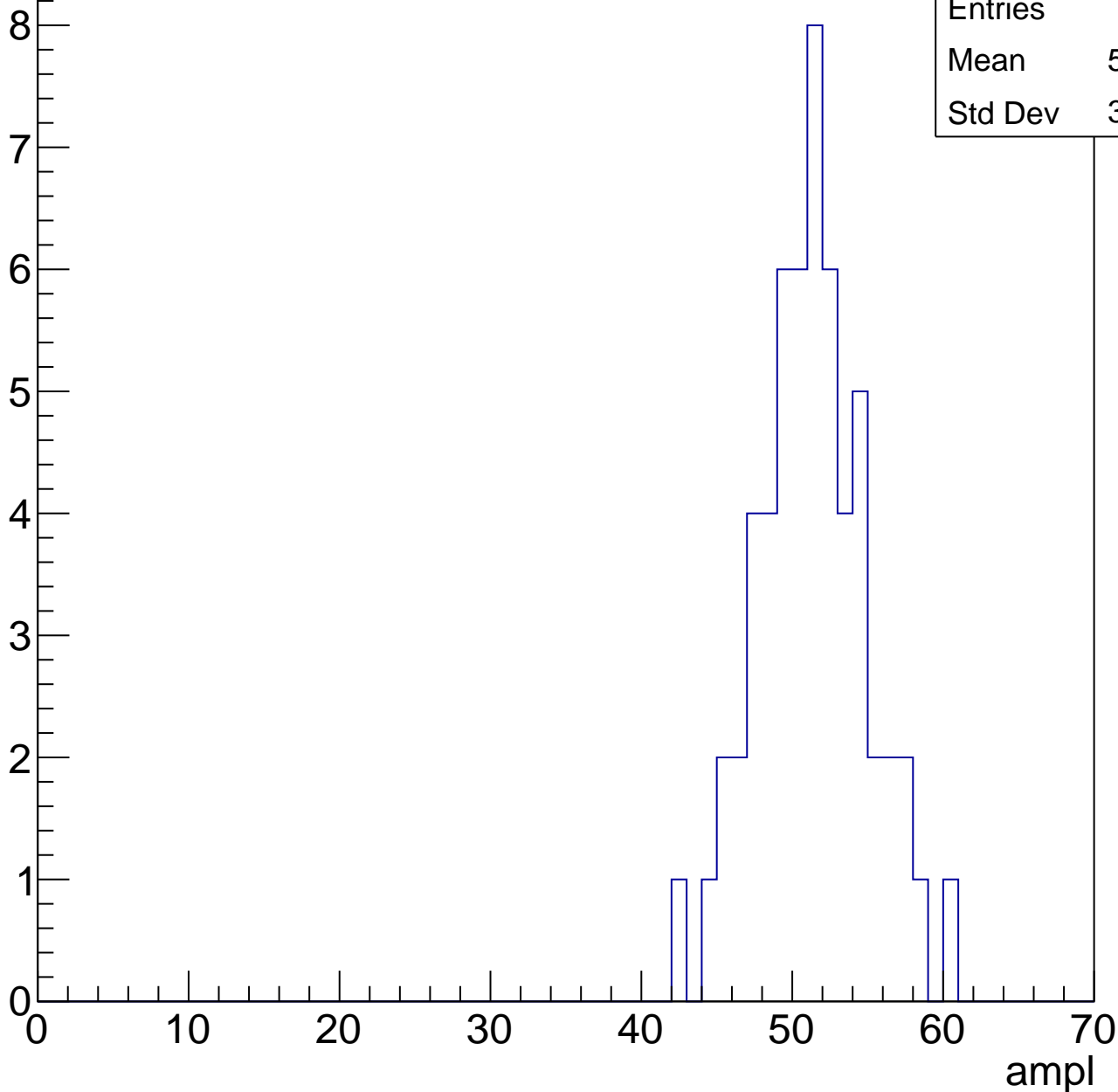


# B0L000S, U7-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	57
Mean	50.84
Std Dev	3.583

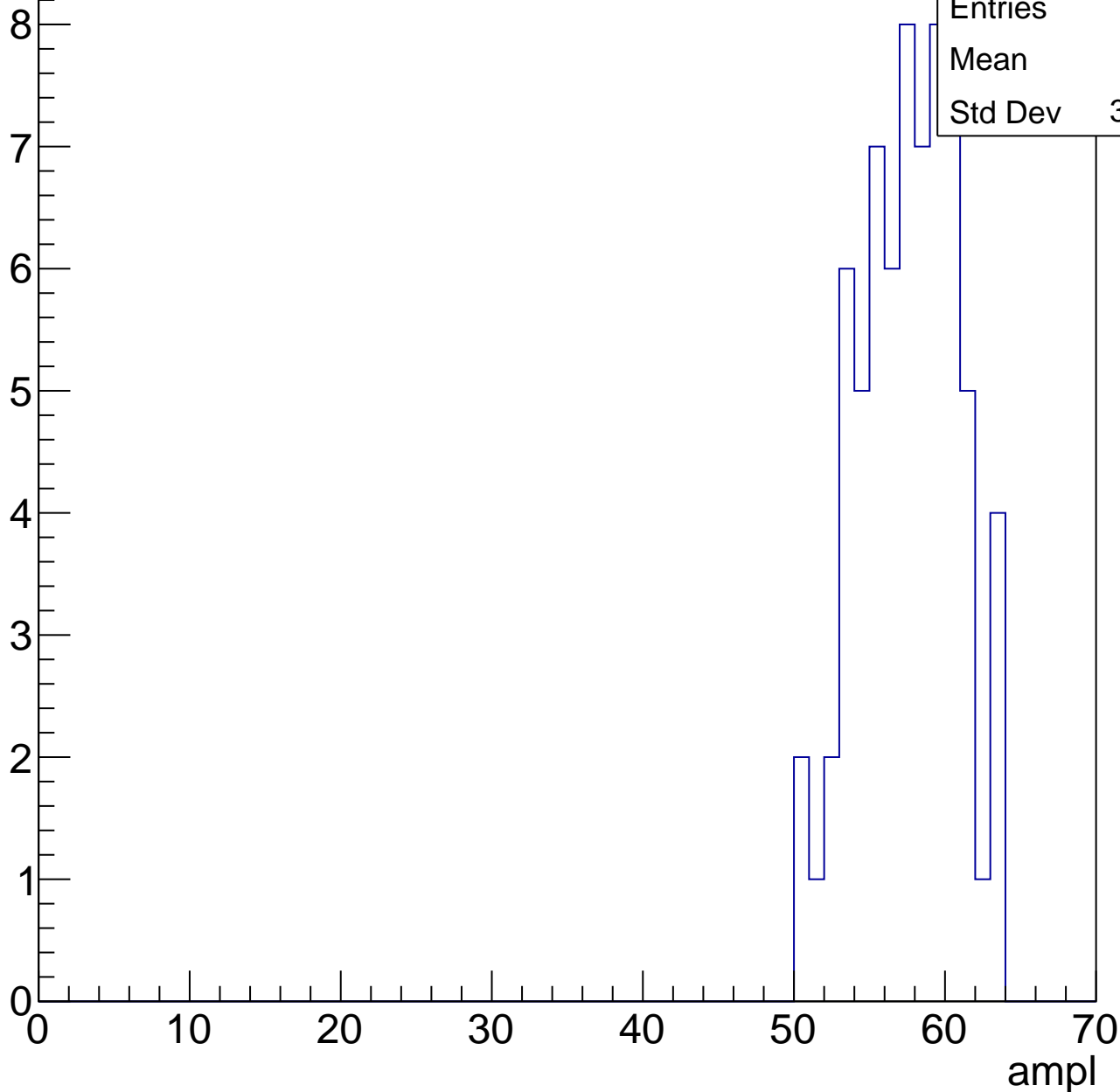


# B0L000S, U7-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	70
Mean	57.1
Std Dev	3.203

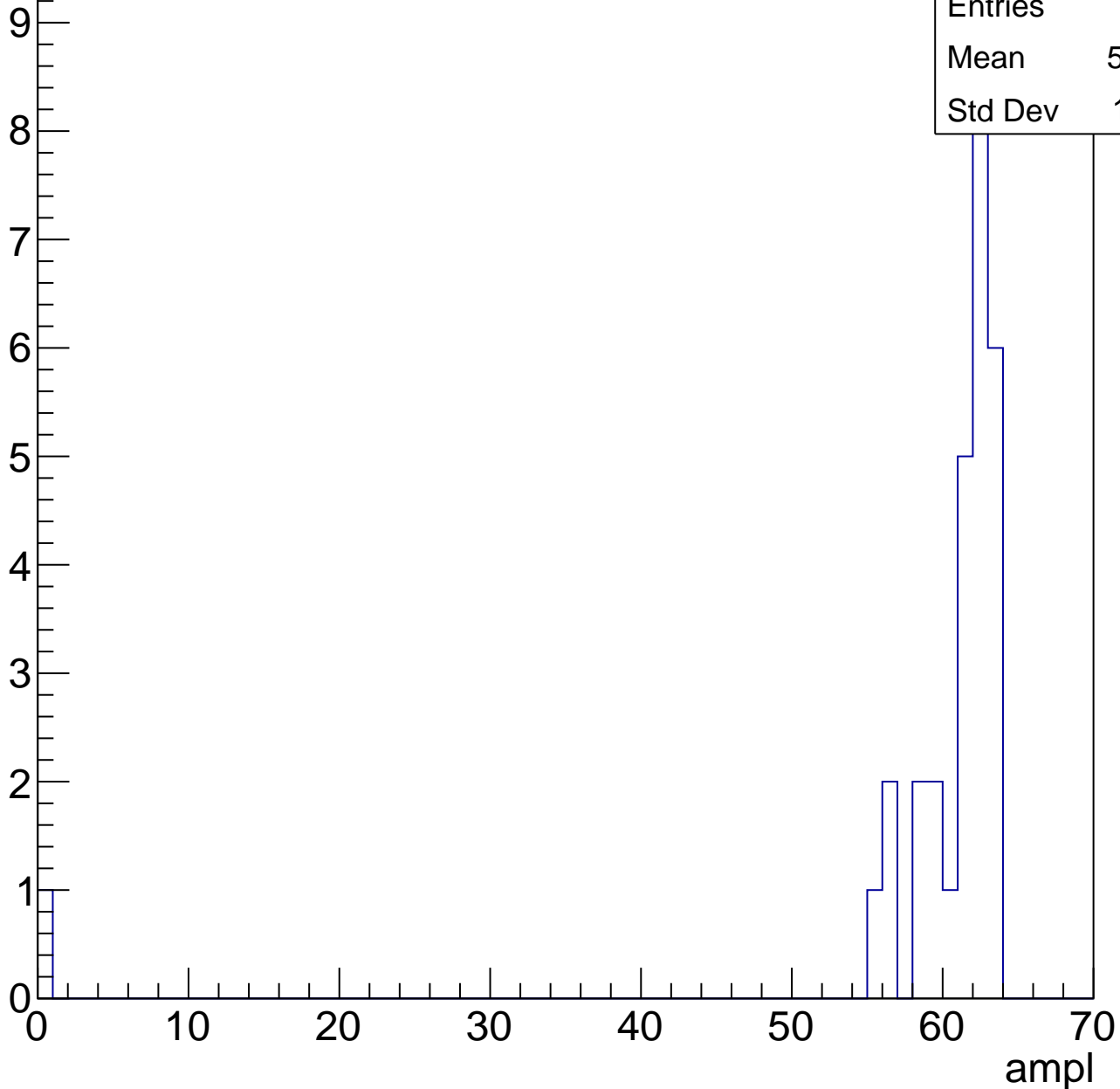


# B0L000S, U7-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	29
Mean	58.69
Std Dev	11.31



# B0L000S, U7-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L000S, U7-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

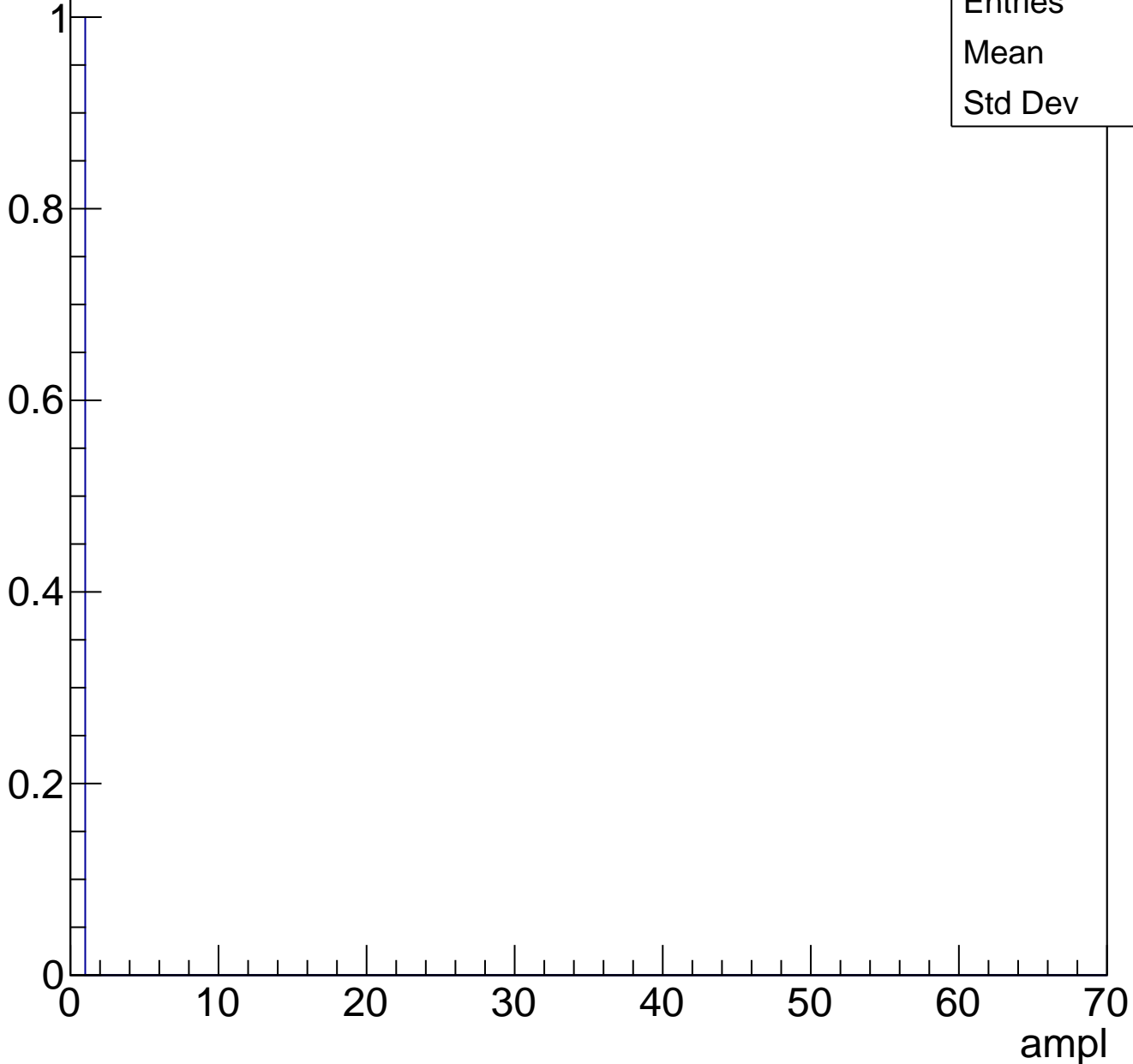


Entries	1
Mean	0
Std Dev	0

# B0L000S, U7-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry



Entries	1
Mean	0
Std Dev	0