

B0L000S, U18-ch0

calib_packv5_042523_0143.root, FC#5, port B1

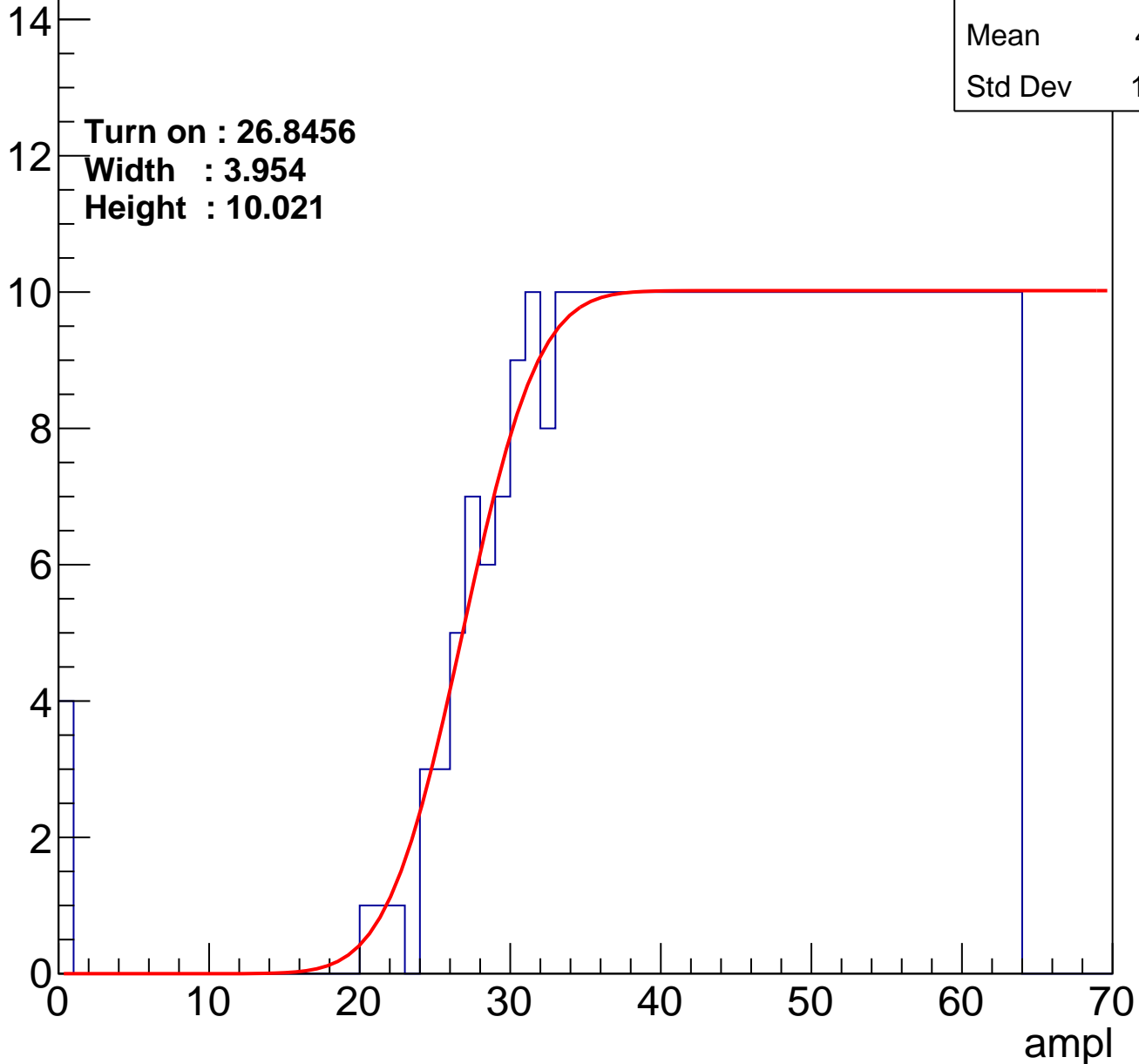
Entries	375
Mean	44.31
Std Dev	11.85

Turn on : 26.8456

Width : 3.954

Height : 10.021

Entry



B0L000S, U18-ch1

calib_packv5_042523_0143.root, FC#5, port B1

Entries	377
Mean	44.47
Std Dev	11.27

Turn on : 26.6626

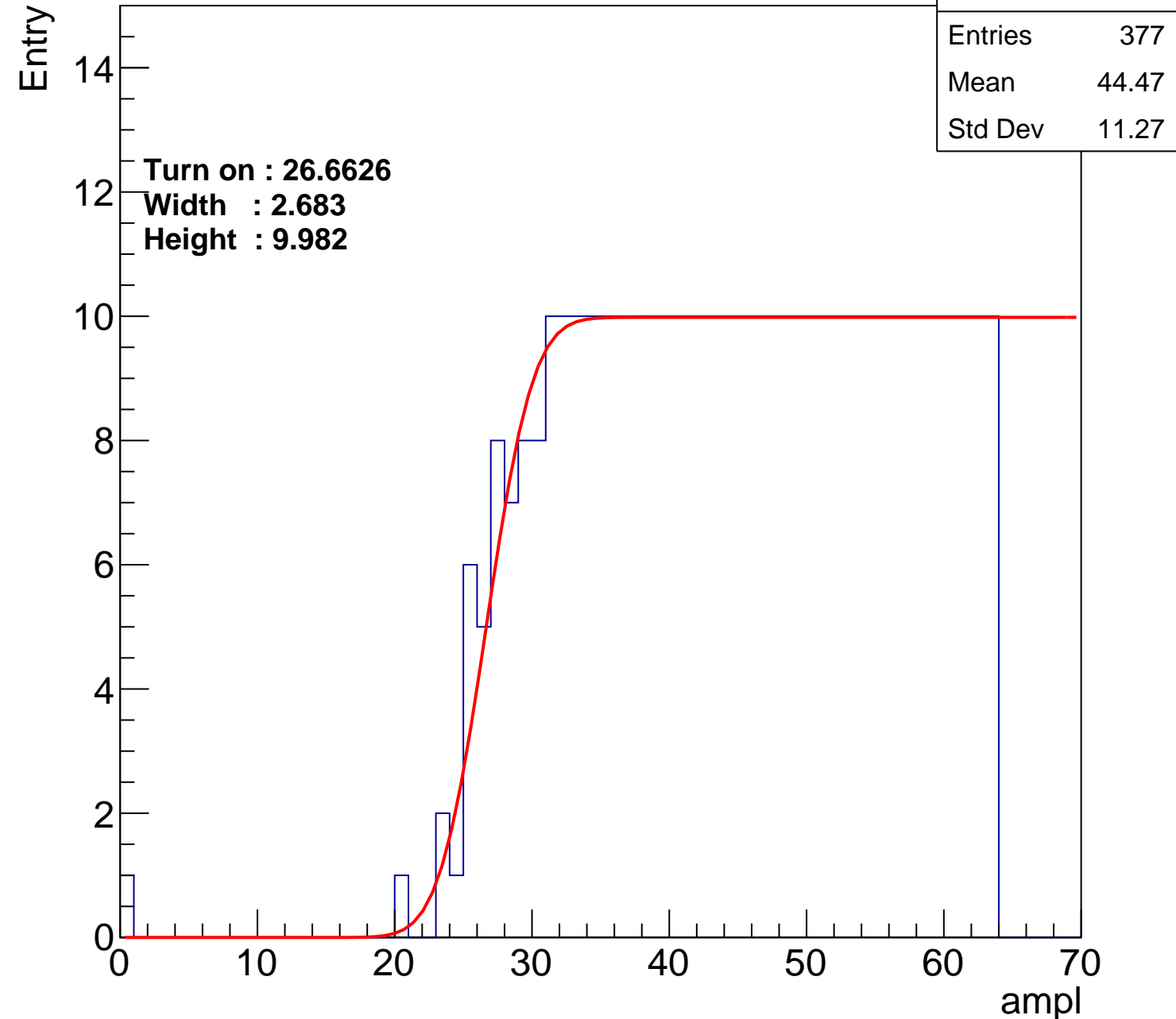
Width : 2.683

Height : 9.982

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch2

calib_packv5_042523_0143.root, FC#5, port B1

Entries	391
Mean	43.59
Std Dev	12.13

Turn on : 25.3178

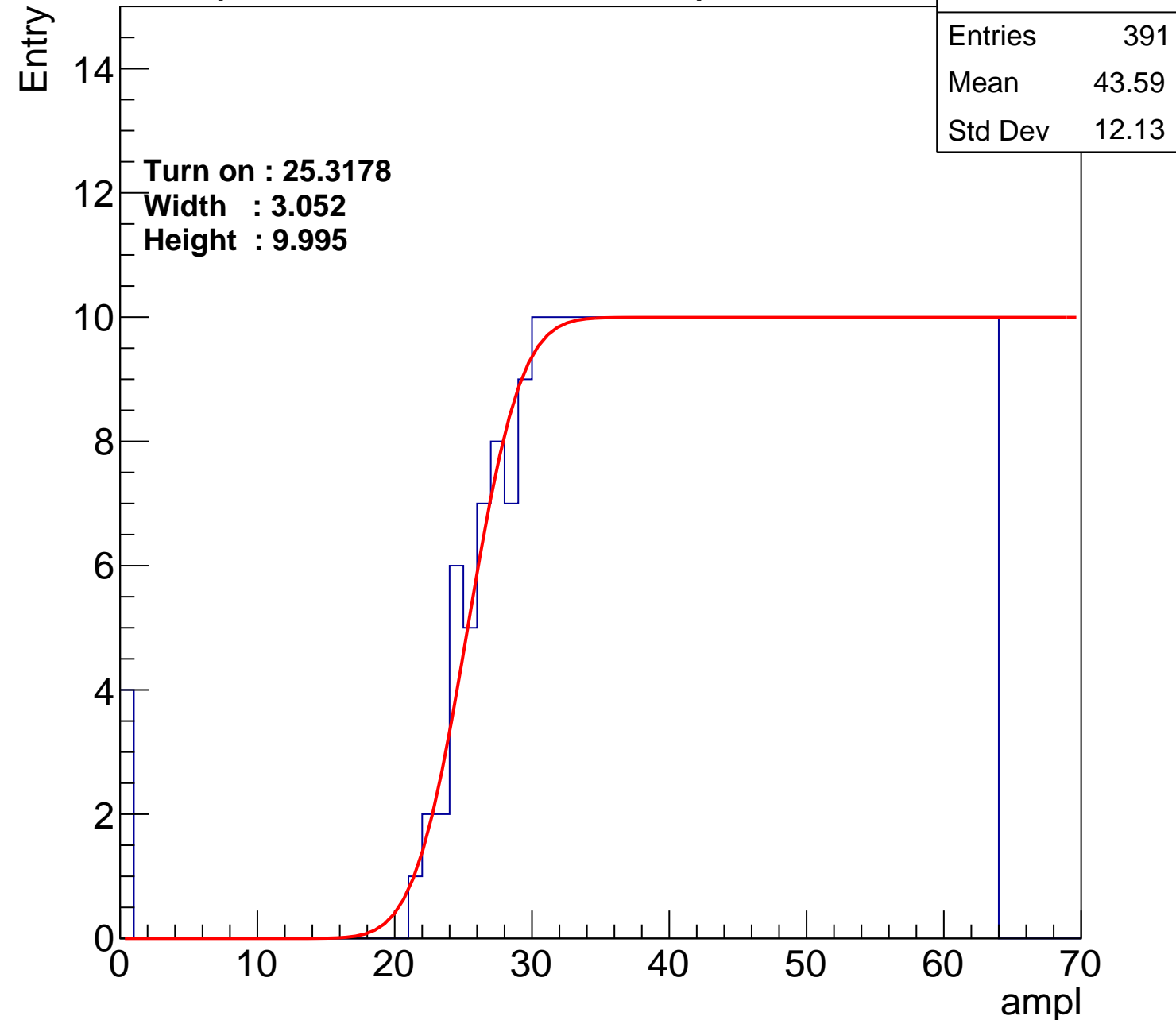
Width : 3.052

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch3

calib_packv5_042523_0143.root, FC#5, port B1

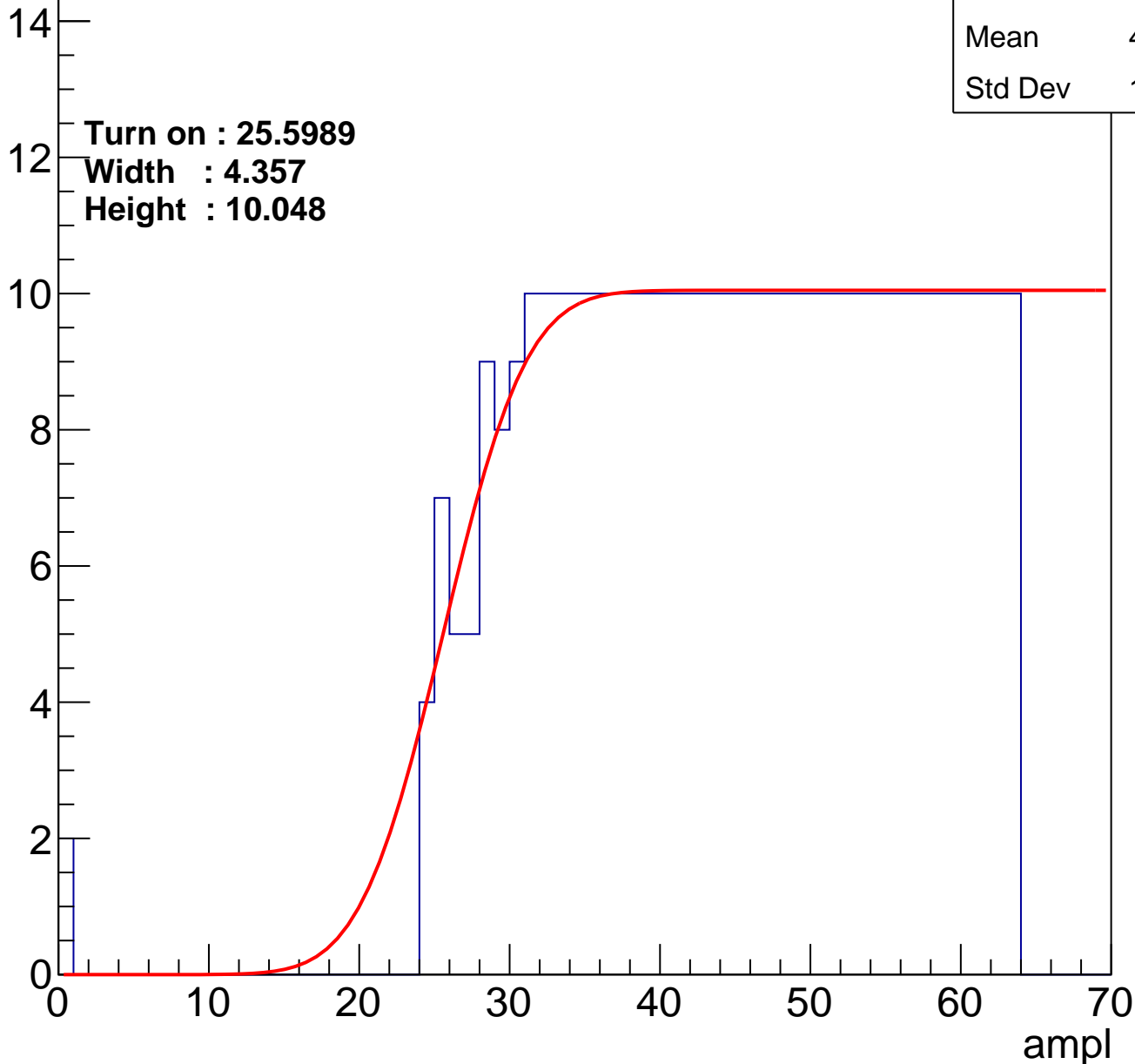
Entry

Entries	379
Mean	44.33
Std Dev	11.46

Turn on : 25.5989

Width : 4.357

Height : 10.048



B0L000S, U18-ch4

calib_packv5_042523_0143.root, FC#5, port B1

Entries	375
Mean	44.48
Std Dev	11.43

Turn on : 26.9034

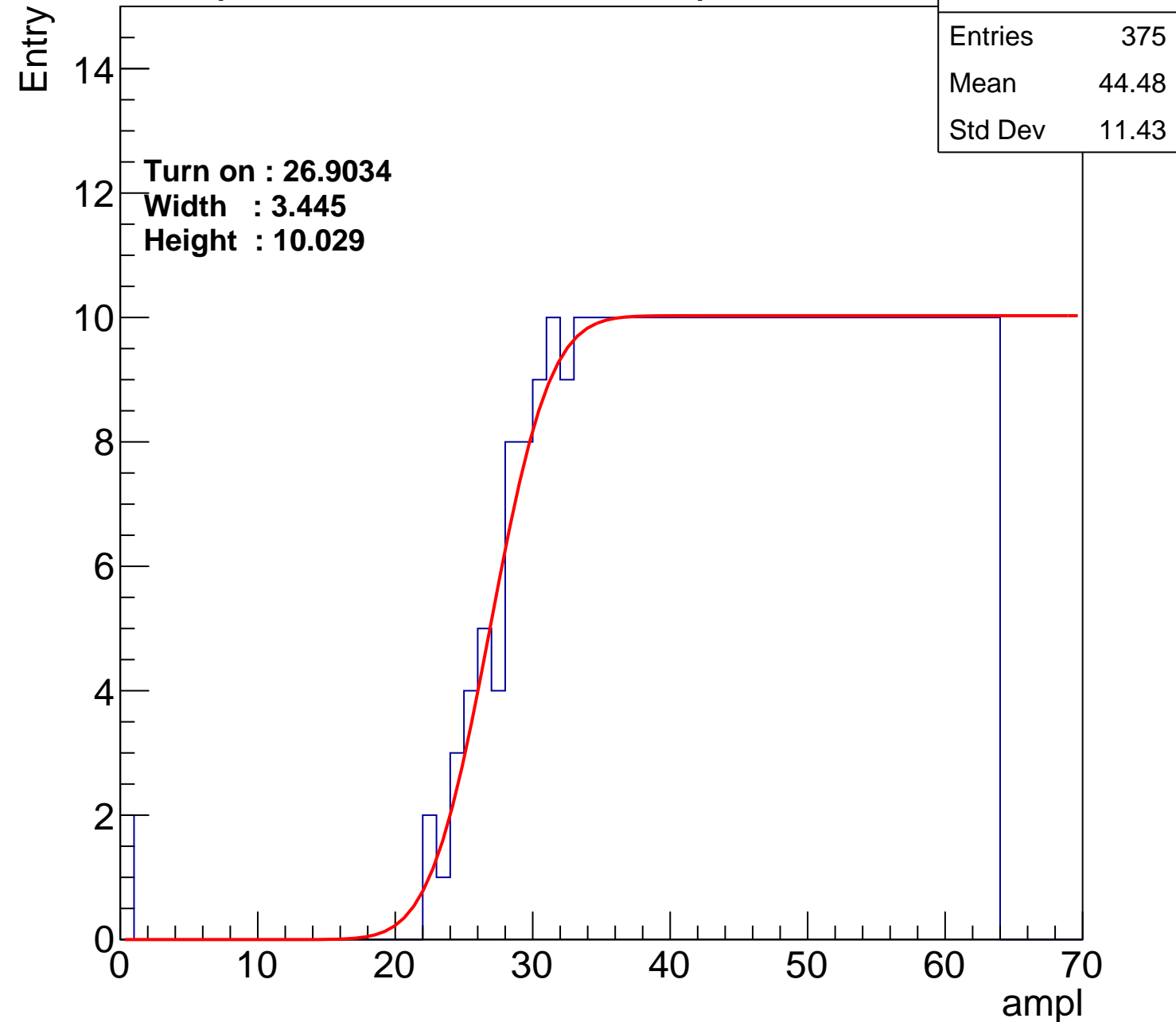
Width : 3.445

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch5

calib_packv5_042523_0143.root, FC#5, port B1

Entries	381
Mean	44.24
Std Dev	11.49

Turn on : 26.3597

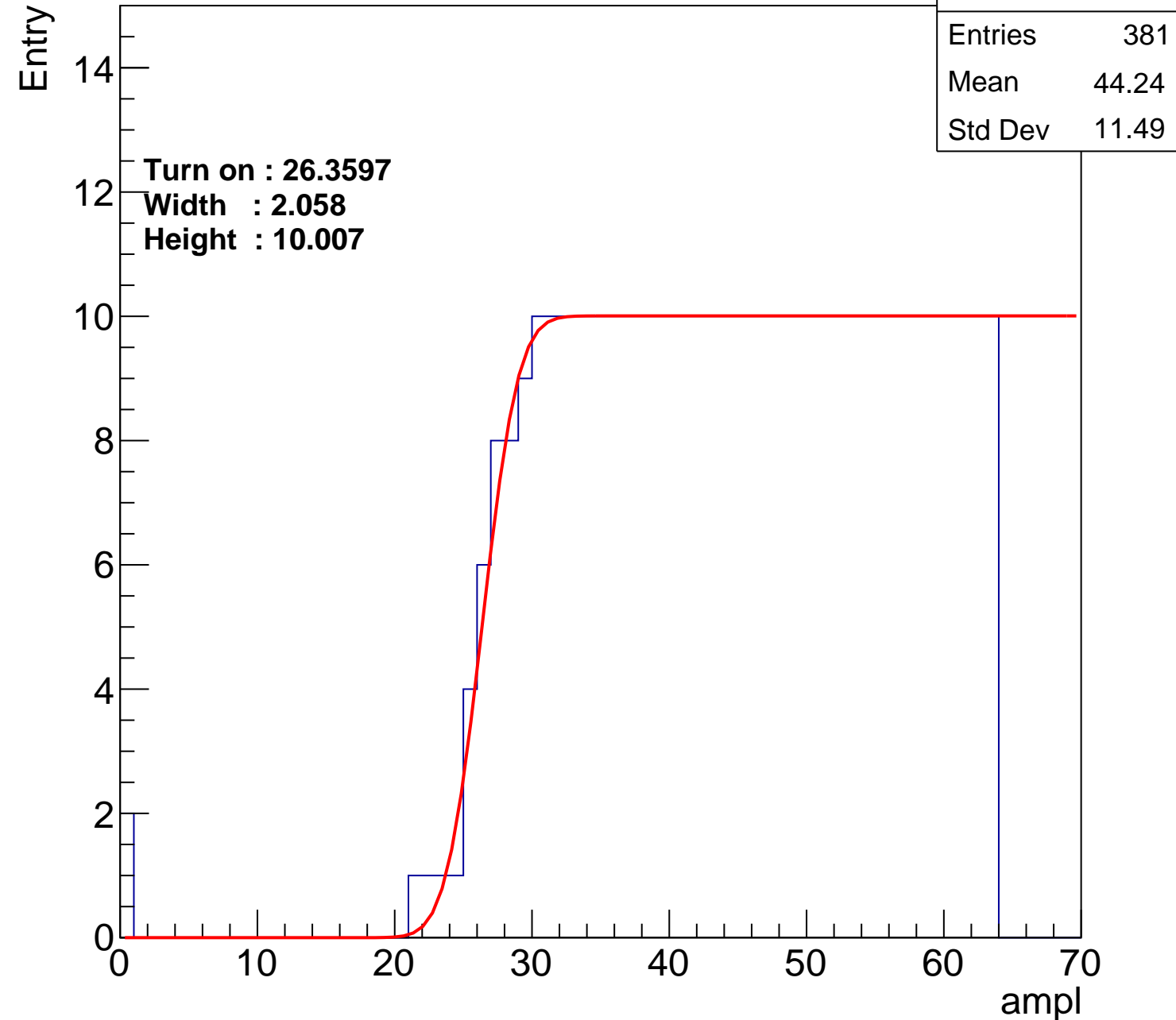
Width : 2.058

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch6

calib_packv5_042523_0143.root, FC#5, port B1

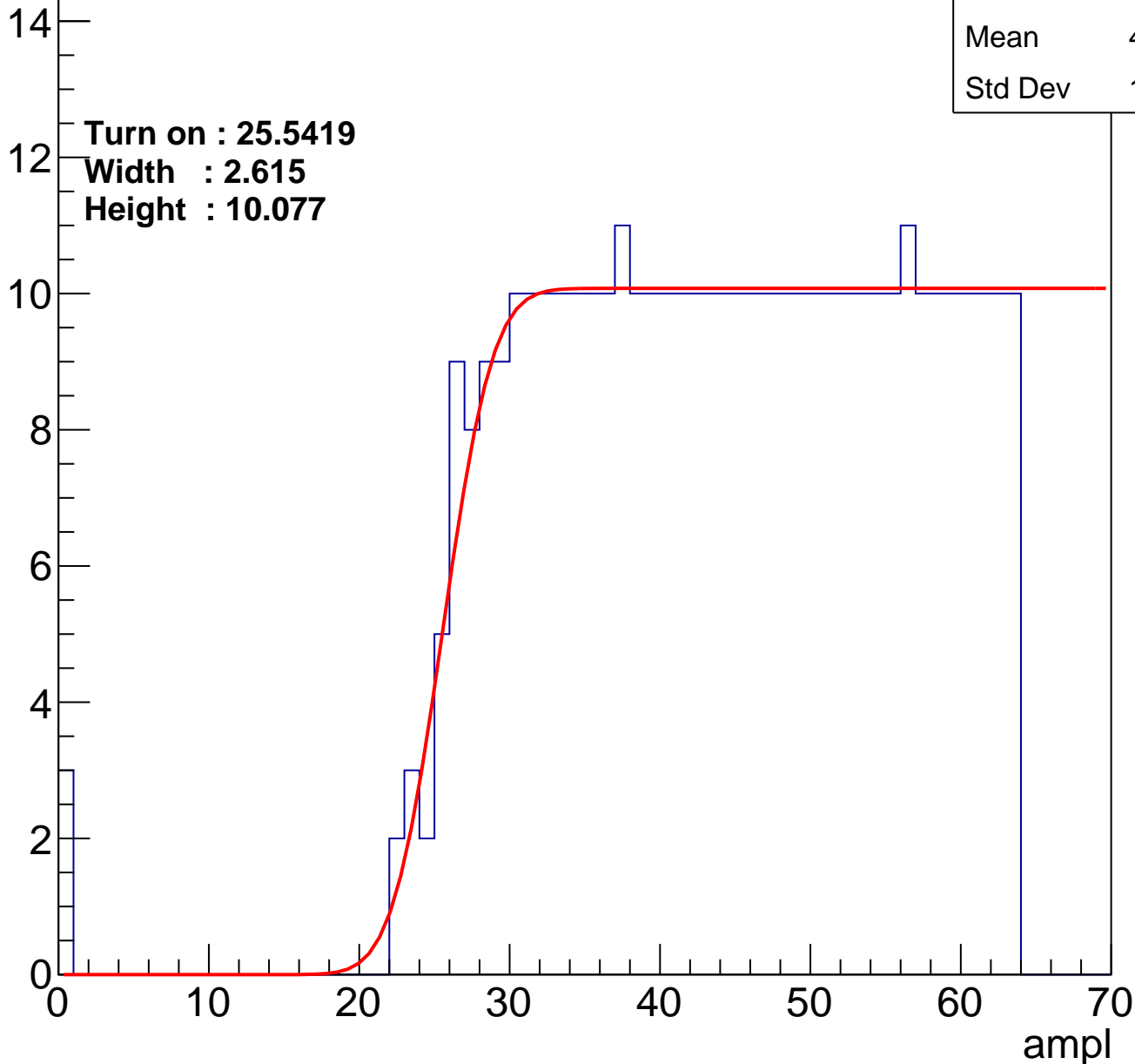
Entry

Entries	392
Mean	43.76
Std Dev	11.88

Turn on : 25.5419

Width : 2.615

Height : 10.077



B0L000S, U18-ch7

calib_packv5_042523_0143.root, FC#5, port B1

Entries	383
Mean	43.95
Std Dev	12

Turn on : 26.7912

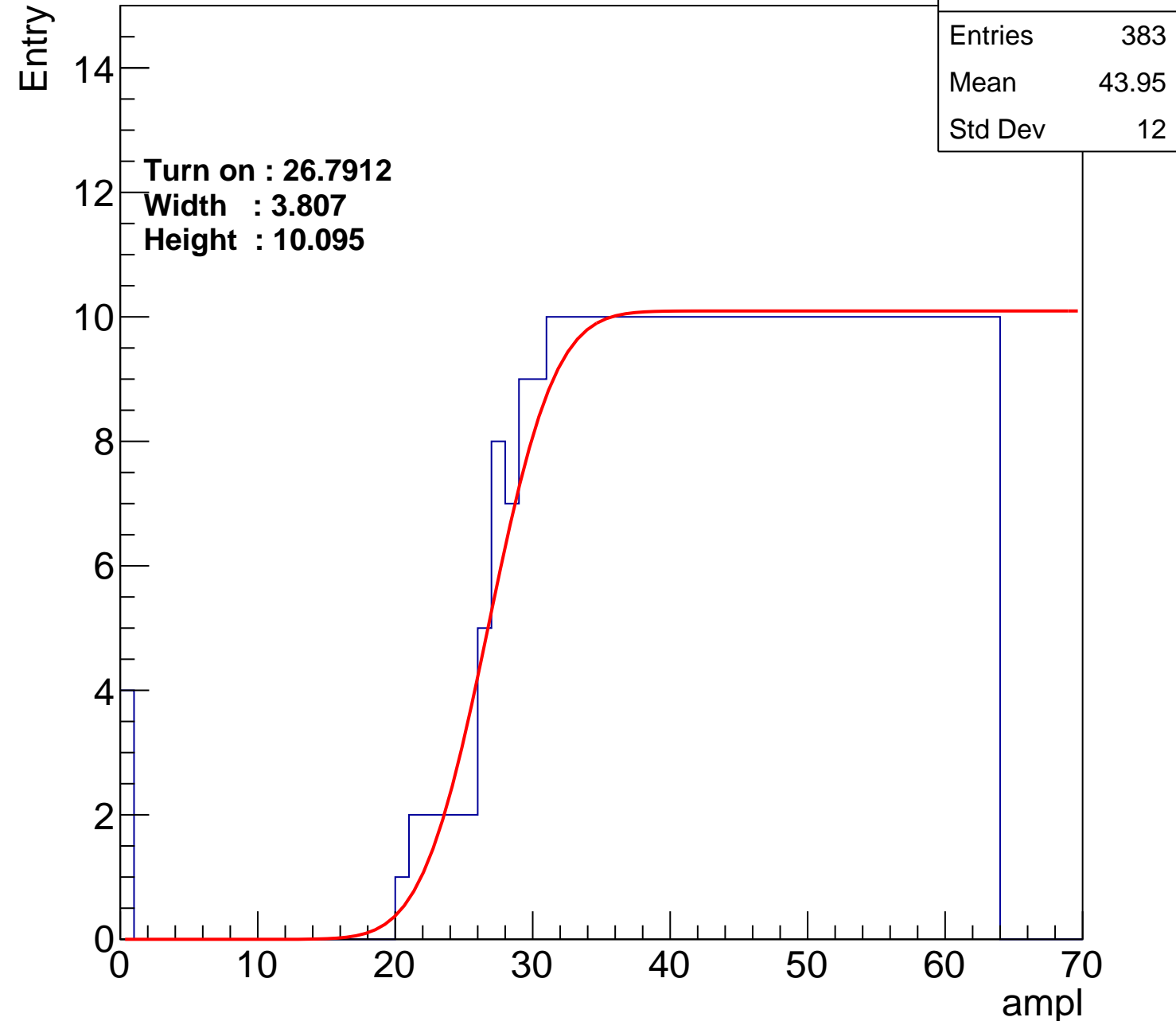
Width : 3.807

Height : 10.095

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch8

calib_packv5_042523_0143.root, FC#5, port B1

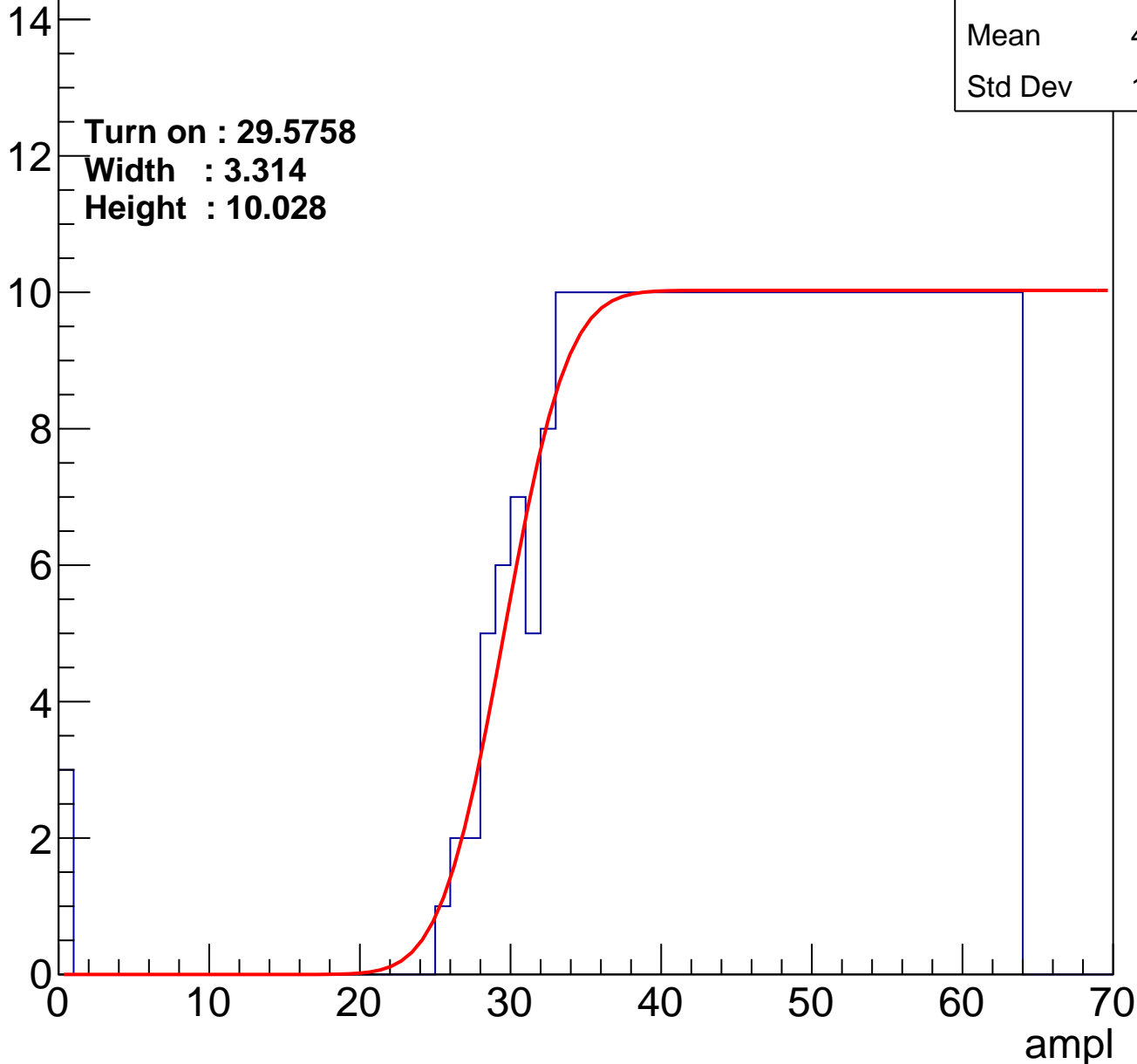
Entry

Entries	349
Mean	45.69
Std Dev	10.99

Turn on : 29.5758

Width : 3.314

Height : 10.028



B0L000S, U18-ch9

calib_packv5_042523_0143.root, FC#5, port B1

Entries	371
Mean	44.74
Std Dev	11.22

Turn on : 27.1073

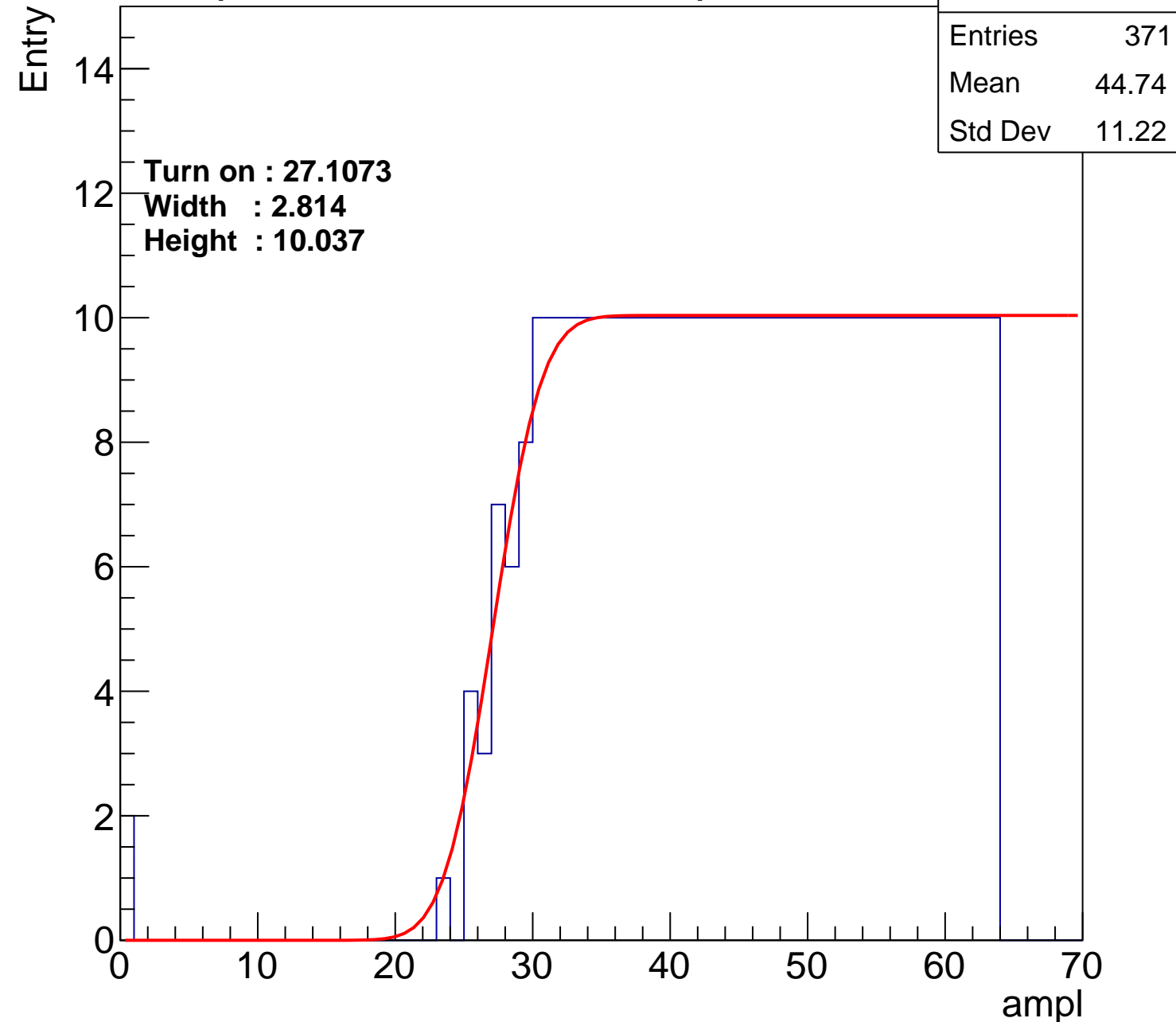
Width : 2.814

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch10

calib_packv5_042523_0143.root, FC#5, port B1

Entries	374
Mean	44.5
Std Dev	11.54

Turn on : 27.5312

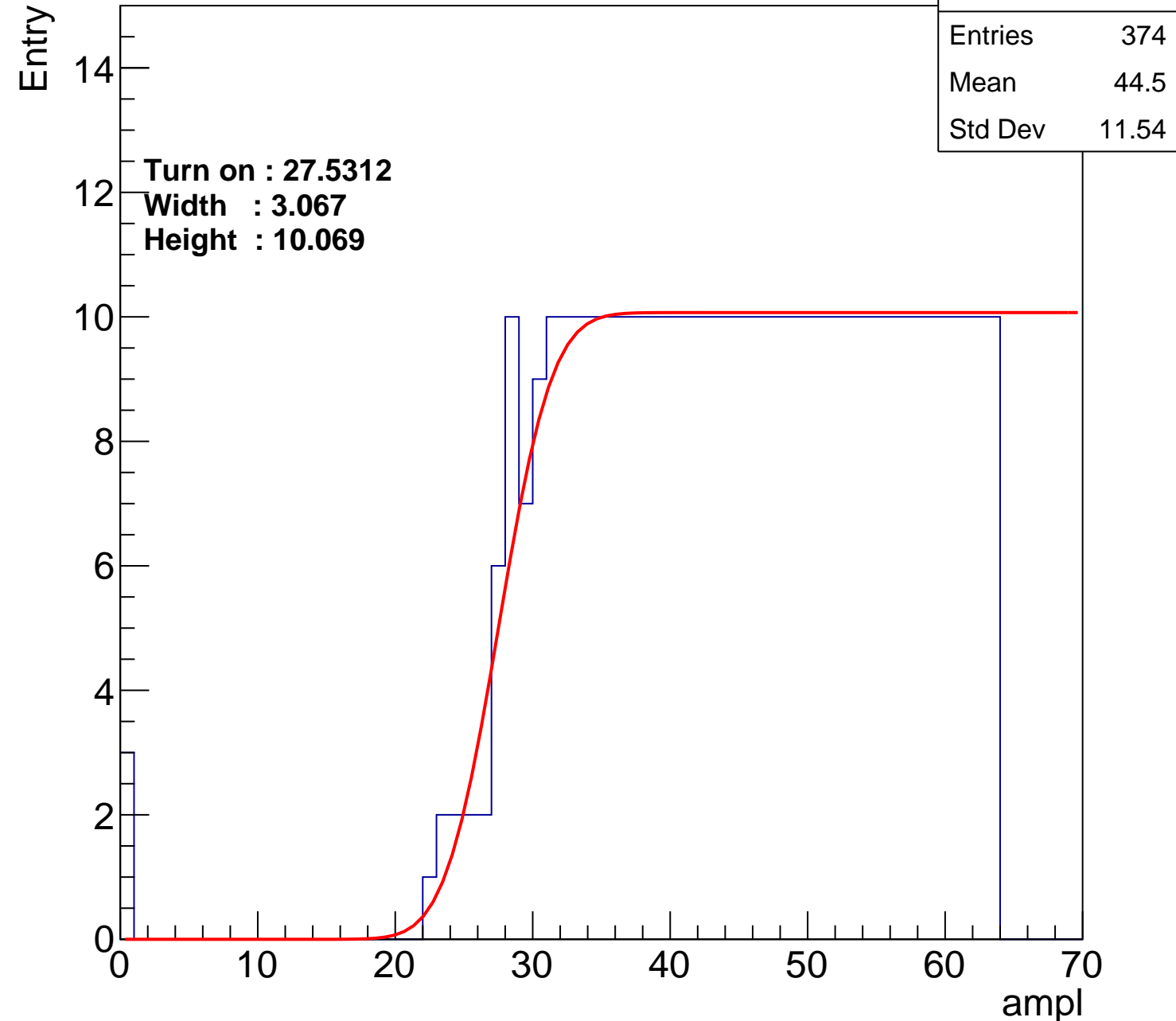
Width : 3.067

Height : 10.069

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch11

calib_packv5_042523_0143.root, FC#5, port B1

Entries	365
Mean	44.98
Std Dev	11.17

Turn on : 28.0869

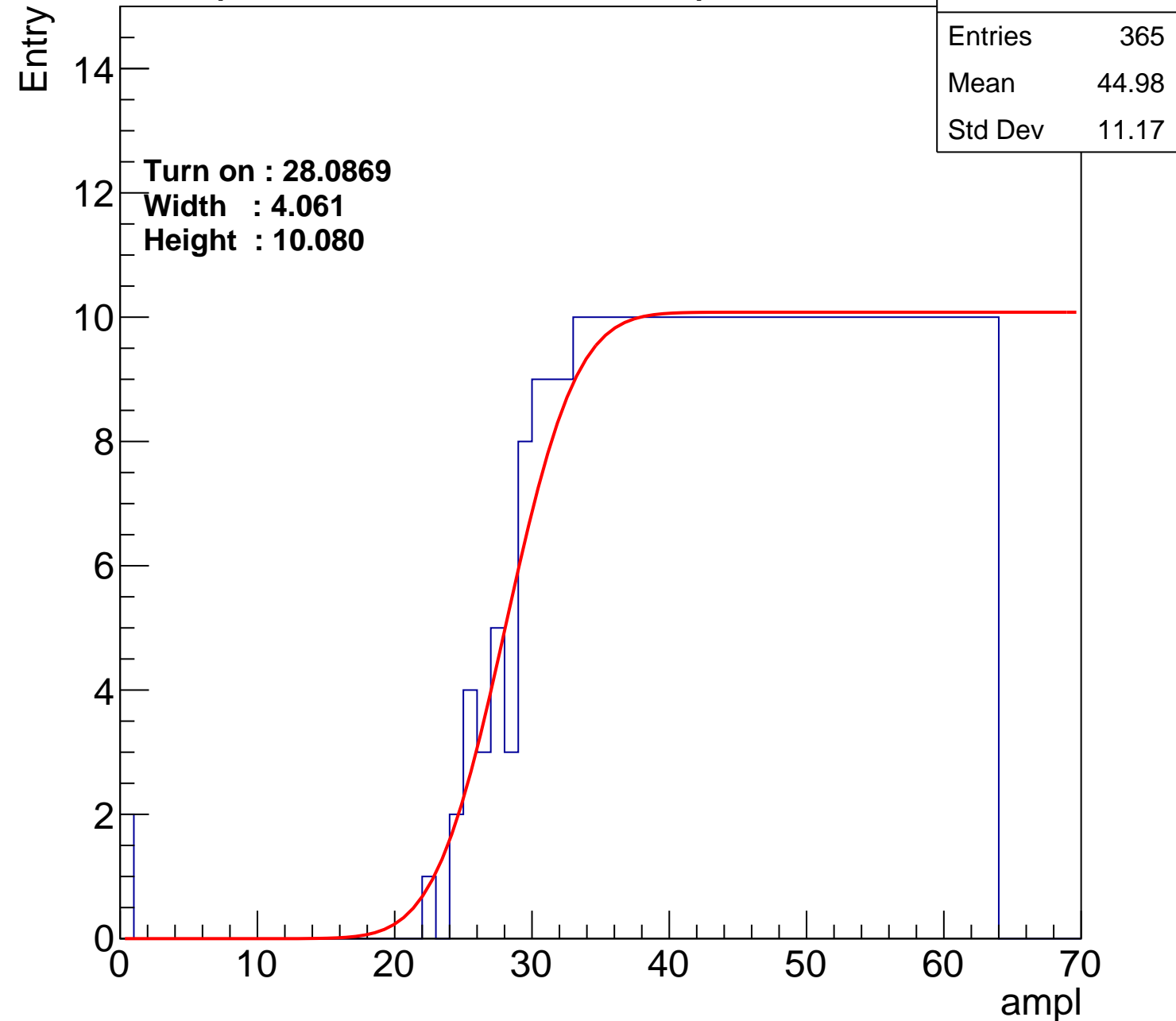
Width : 4.061

Height : 10.080

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch12

calib_packv5_042523_0143.root, FC#5, port B1

Entries	371
Mean	44.7
Std Dev	11.3

Turn on : 27.0998

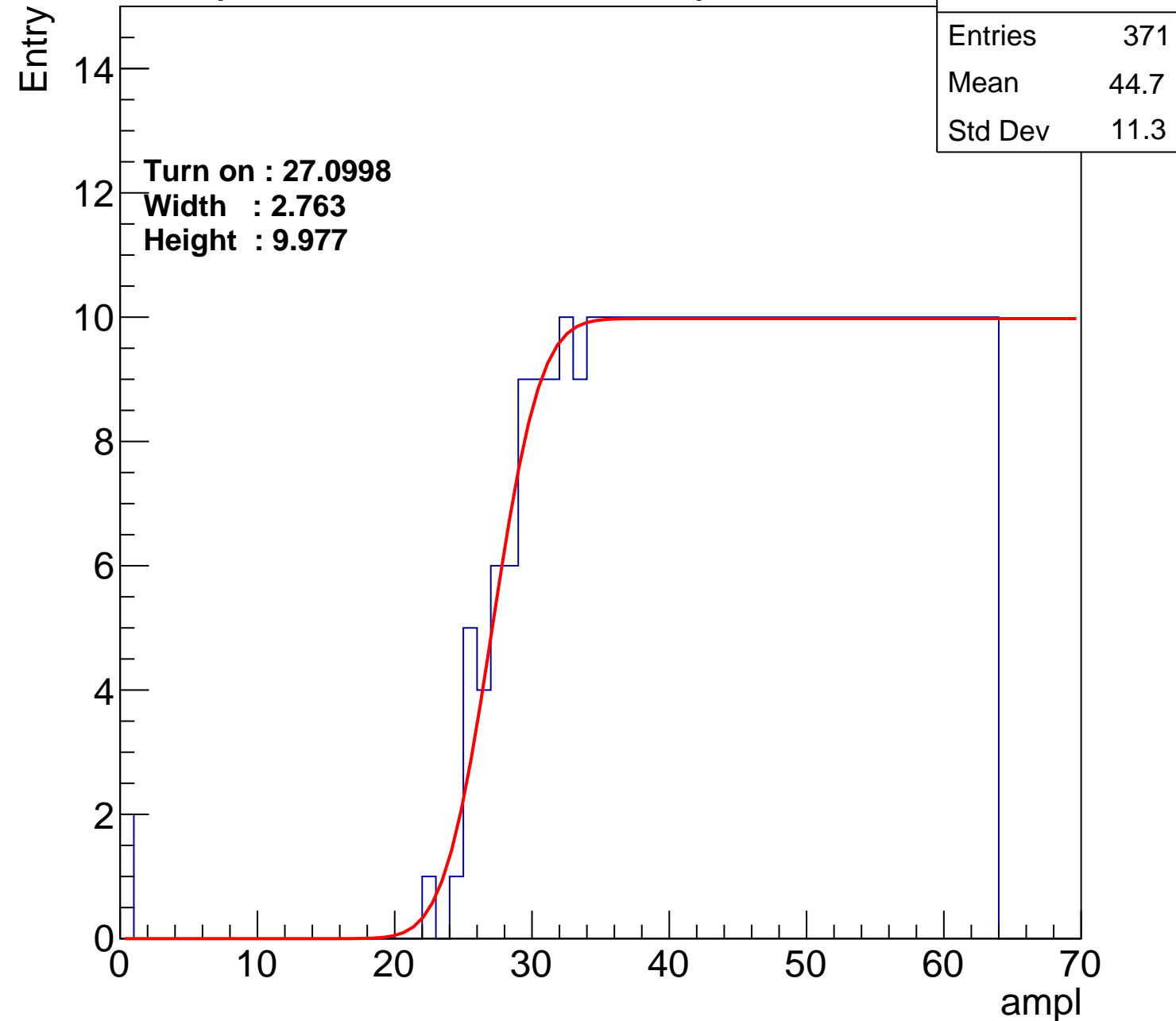
Width : 2.763

Height : 9.977

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch13

calib_packv5_042523_0143.root, FC#5, port B1

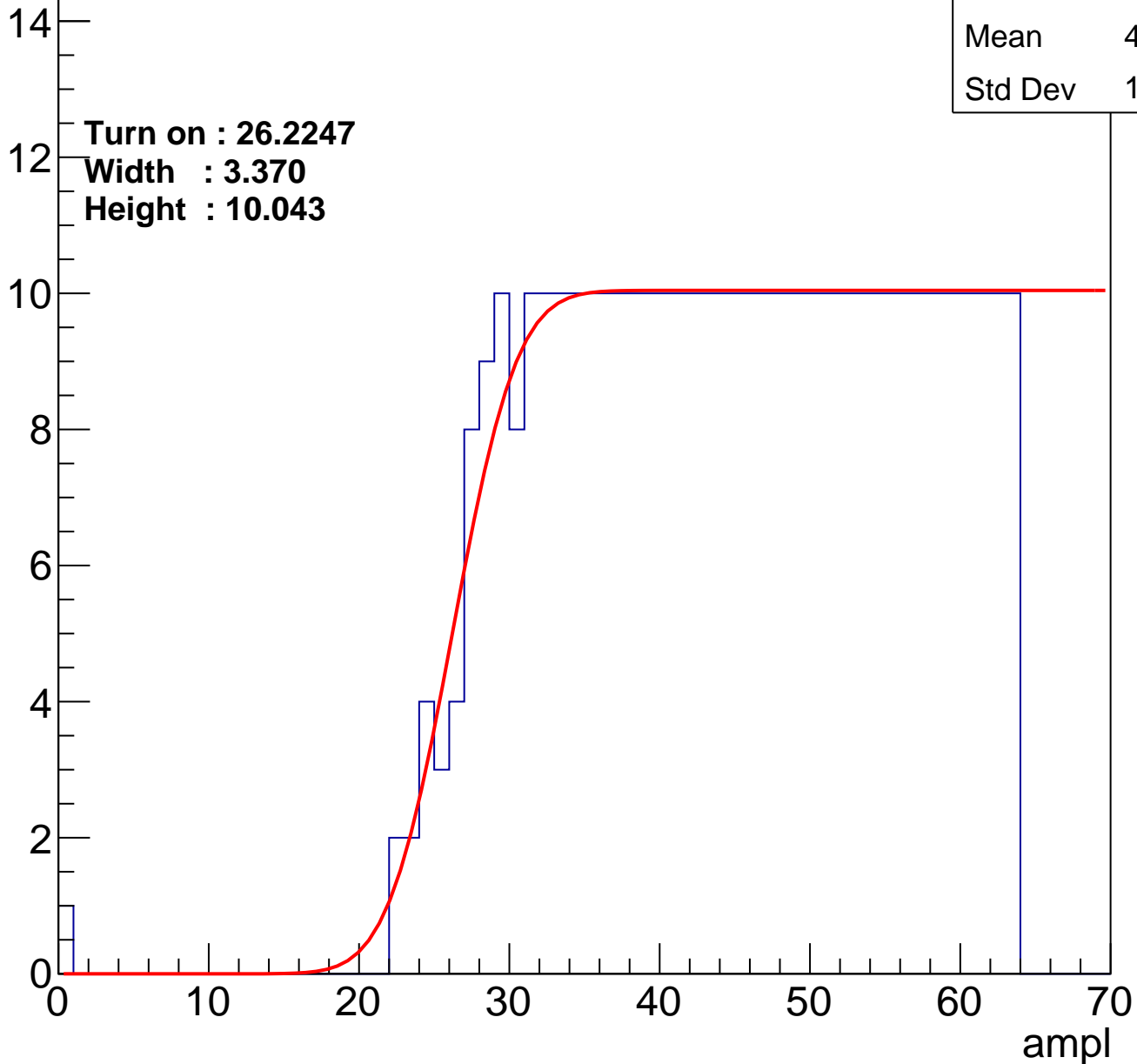
Entries	381
Mean	44.29
Std Dev	11.35

Turn on : 26.2247

Width : 3.370

Height : 10.043

Entry



B0L000S, U18-ch14

calib_packv5_042523_0143.root, FC#5, port B1

Entries	383
Mean	43.98
Std Dev	11.95

Turn on : 26.5878

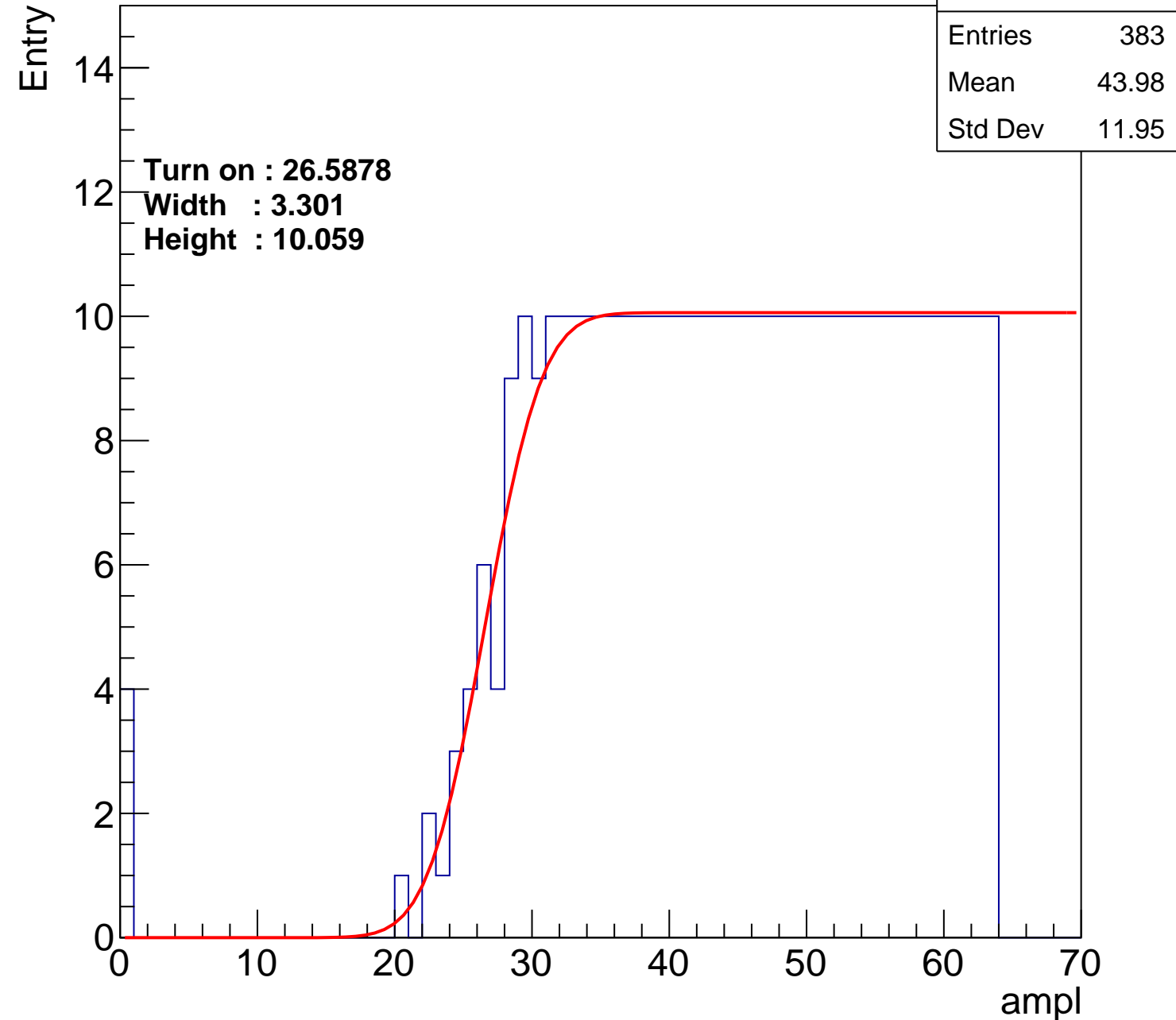
Width : 3.301

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl

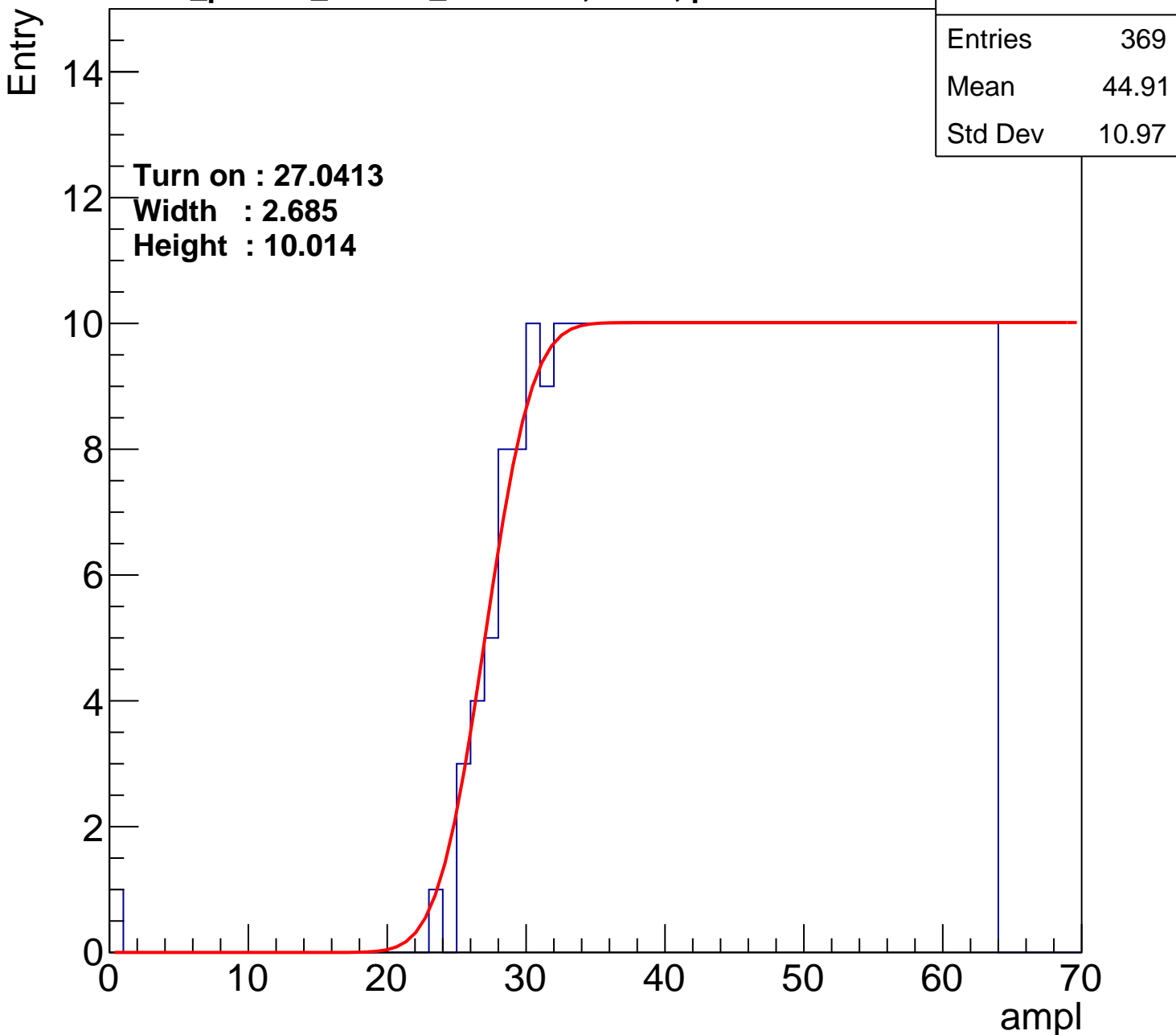


calib_packv5_042523_0143.root, FC#5, port B1

calib_packv5_042523_0143.root, FC#5, port B1

Entries	369
Mean	44.91
Std Dev	10.97

Height : 10.014



B0L000S, U18-ch16

calib_packv5_042523_0143.root, FC#5, port B1

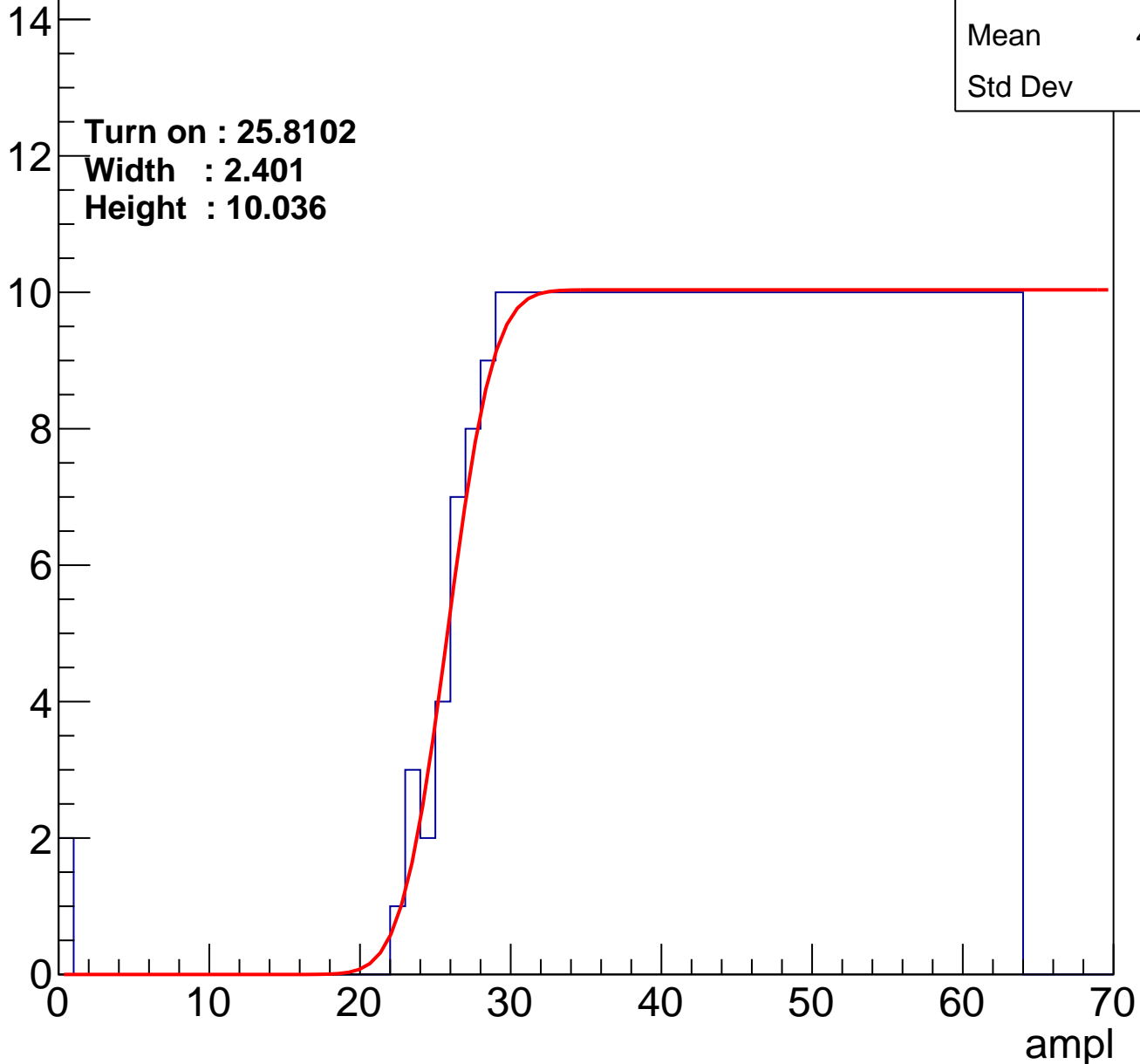
Entries	386
Mean	44.01
Std Dev	11.6

Turn on : 25.8102

Width : 2.401

Height : 10.036

Entry



B0L000S, U18-ch17

calib_packv5_042523_0143.root, FC#5, port B1

Entries	356
Mean	45.26
Std Dev	11.38

Turn on : 28.9817

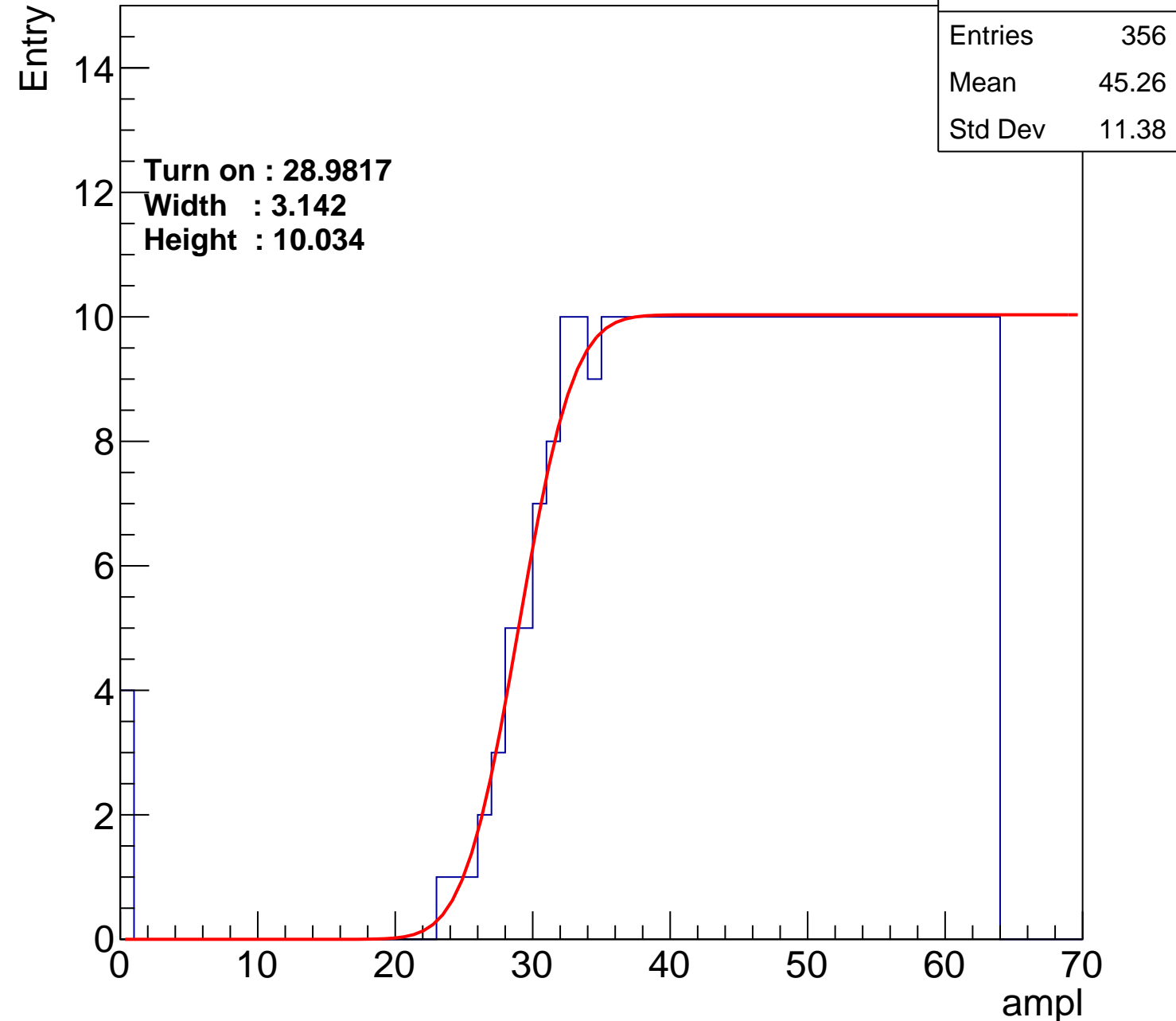
Width : 3.142

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch18

calib_packv5_042523_0143.root, FC#5, port B1

Entries	395
Mean	43.58
Std Dev	11.82

Turn on : 24.8678

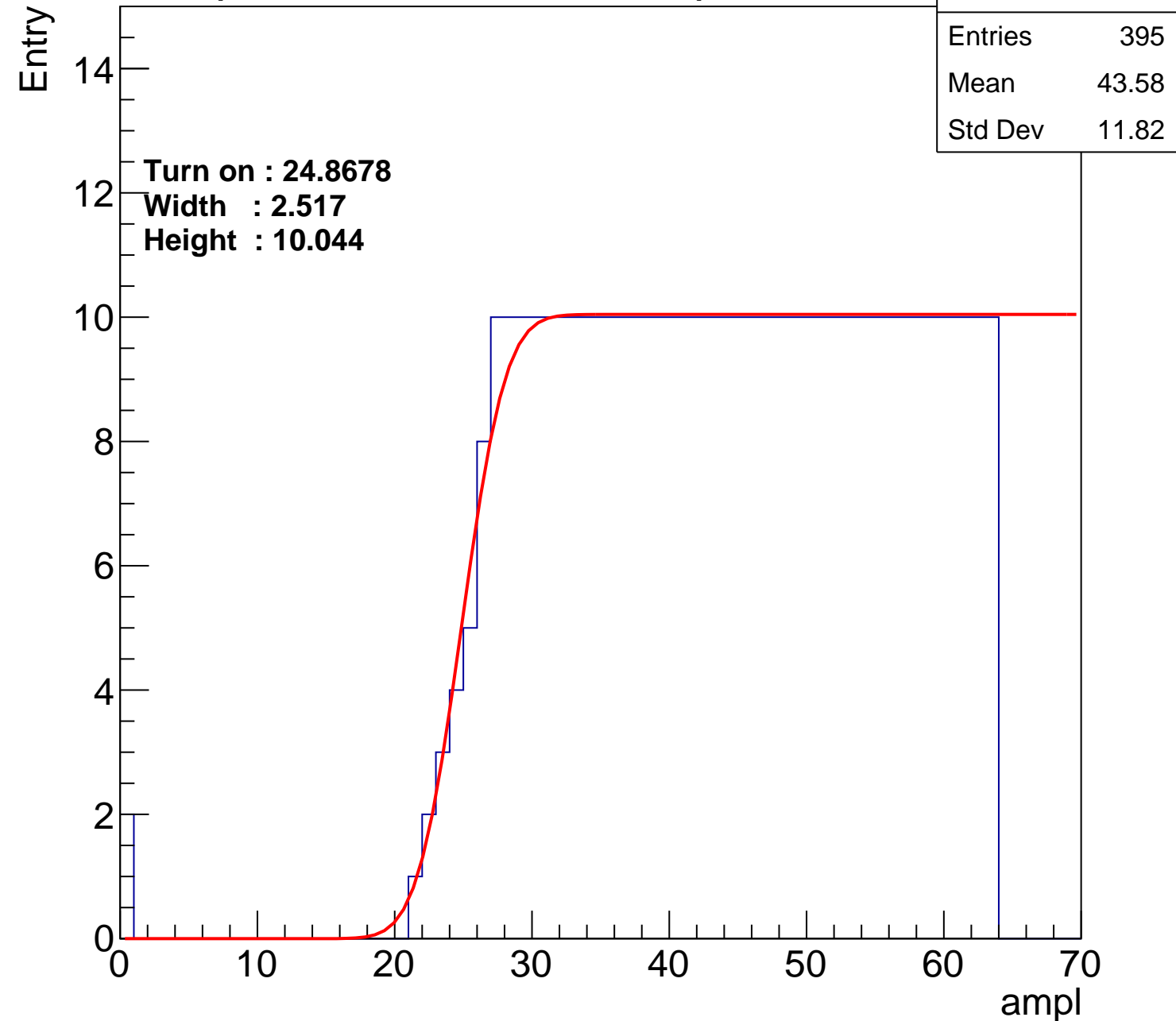
Width : 2.517

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch19

calib_packv5_042523_0143.root, FC#5, port B1

Entries	373
Mean	44.65
Std Dev	11.27

Turn on : 27.2099

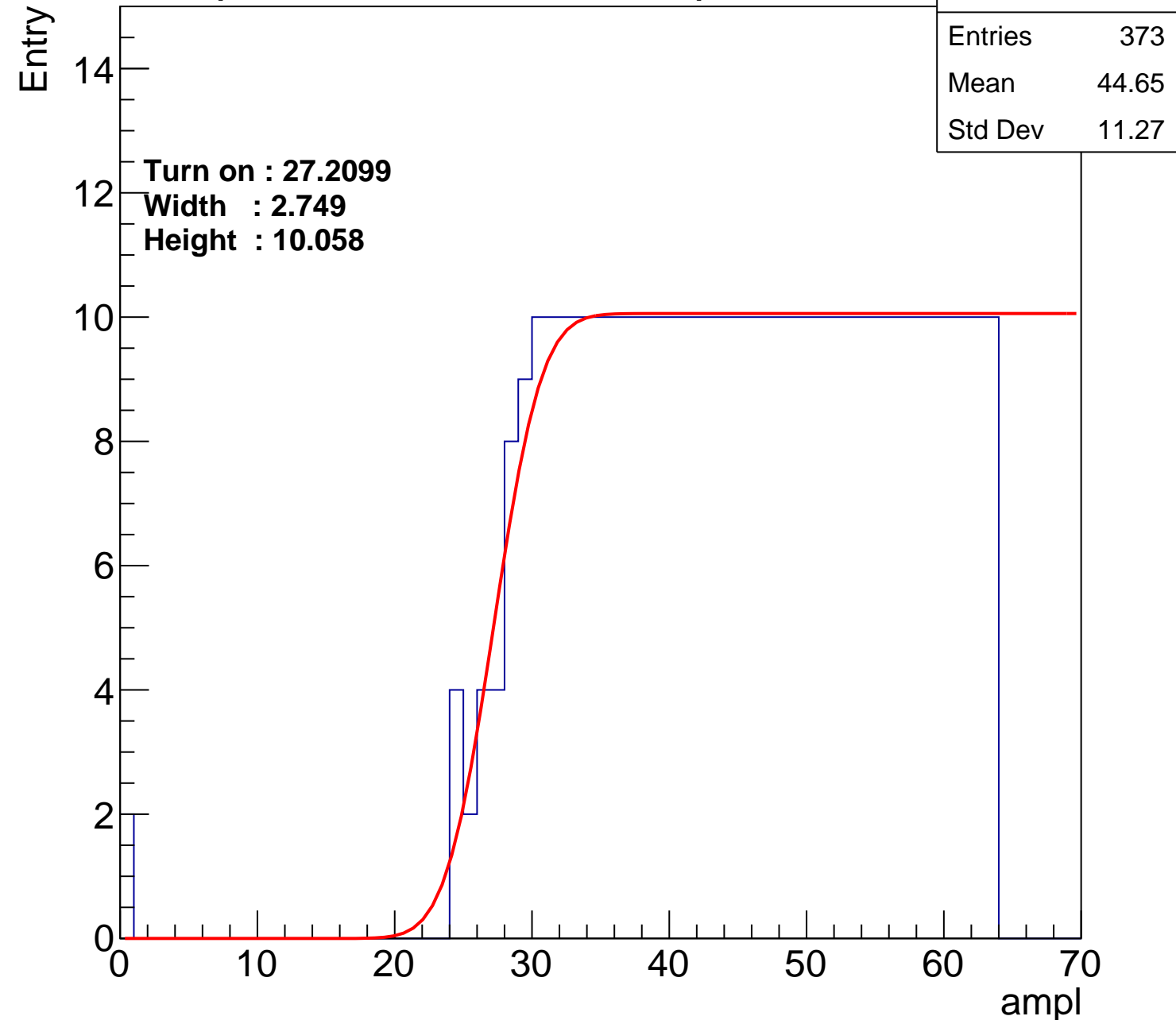
Width : 2.749

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch20

calib_packv5_042523_0143.root, FC#5, port B1

Entries	372
Mean	44.55
Std Dev	11.57

Turn on : 27.4718

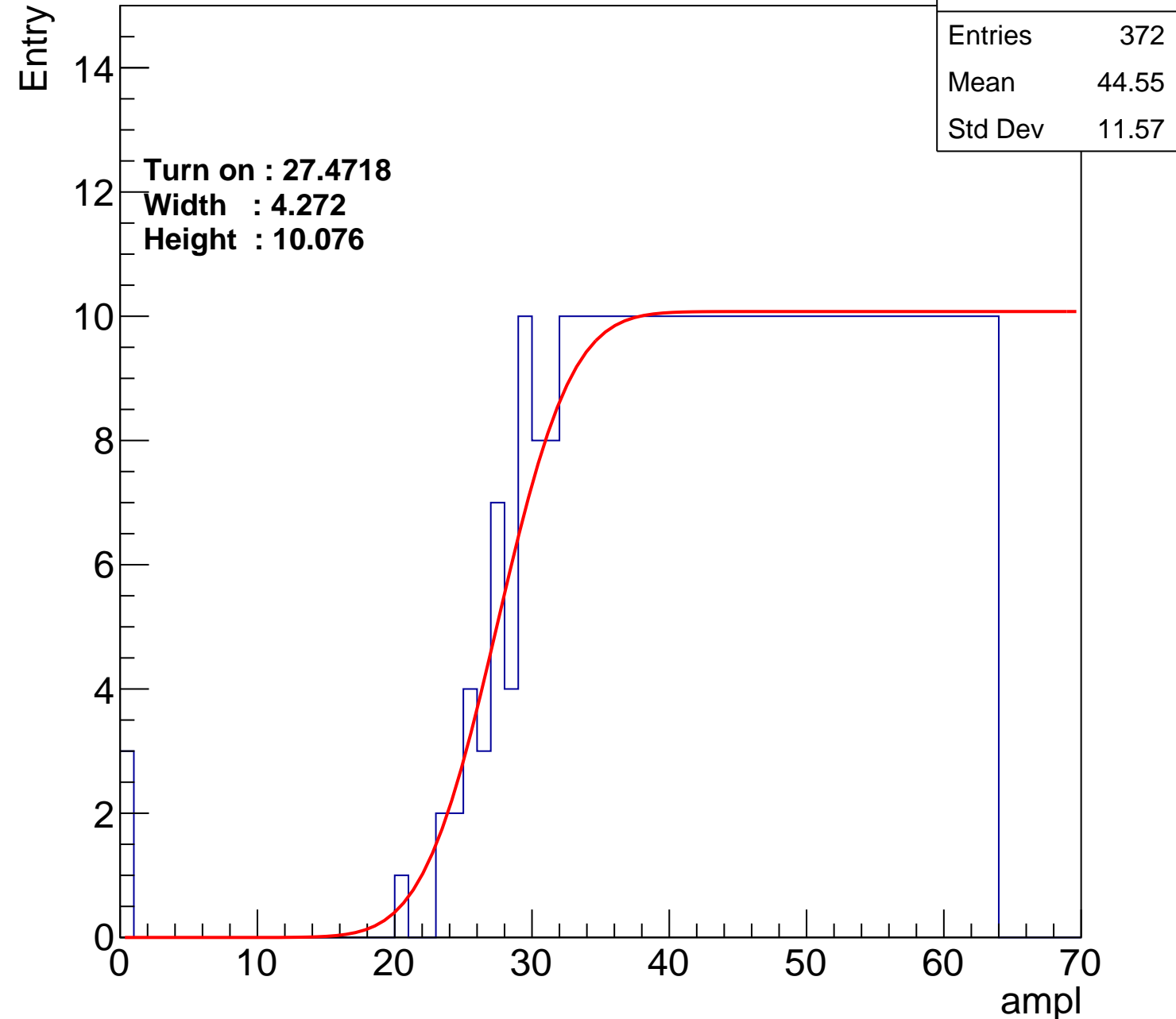
Width : 4.272

Height : 10.076

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch21

calib_packv5_042523_0143.root, FC#5, port B1

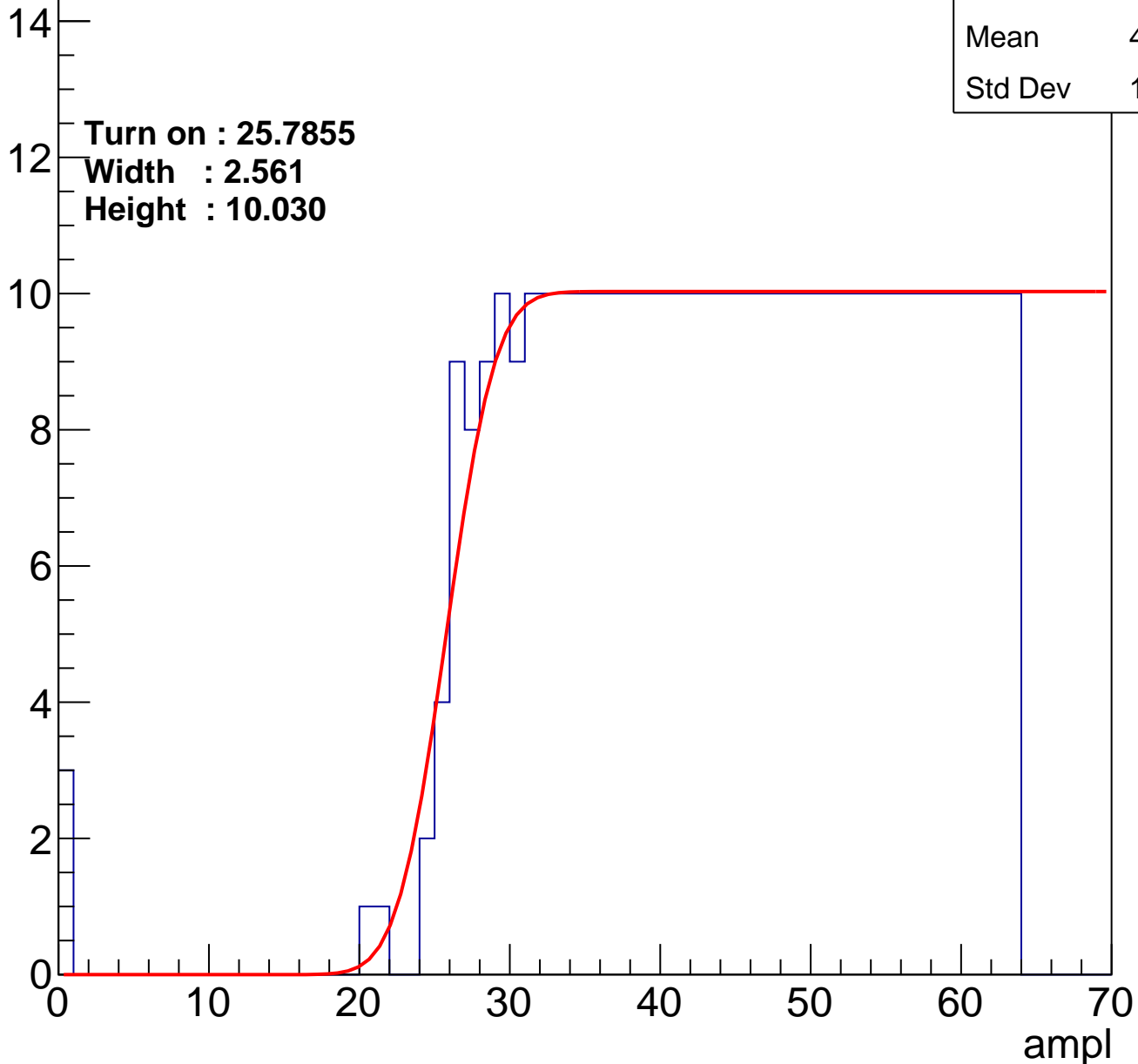
Entries	386
Mean	43.94
Std Dev	11.78

Turn on : 25.7855

Width : 2.561

Height : 10.030

Entry



B0L000S, U18-ch22

calib_packv5_042523_0143.root, FC#5, port B1

Entries	388
Mean	43.93
Std Dev	11.55

Turn on : 24.9774

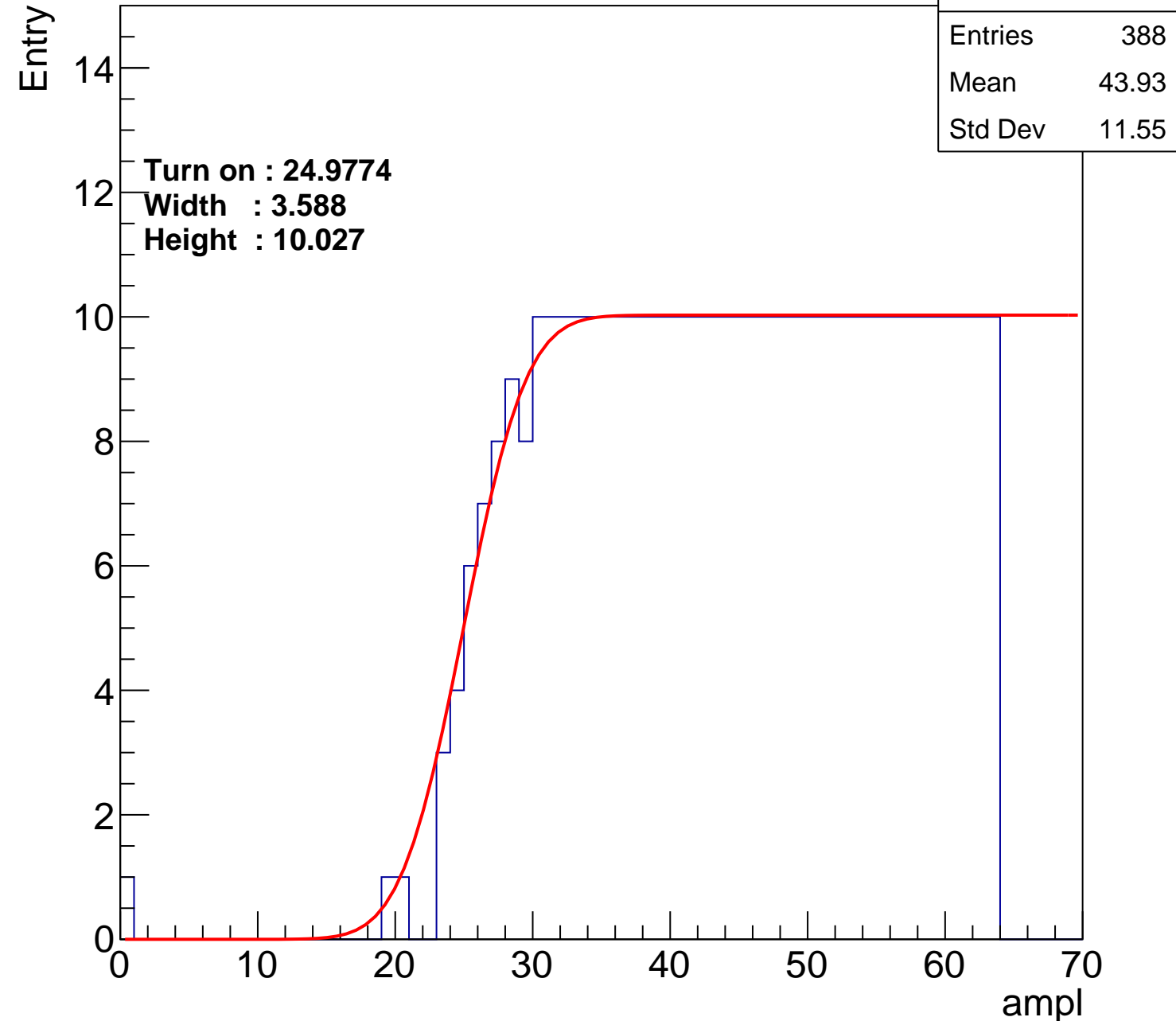
Width : 3.588

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch23

calib_packv5_042523_0143.root, FC#5, port B1

Entries	369
Mean	44.66
Std Dev	11.63

Turn on : 28.2457

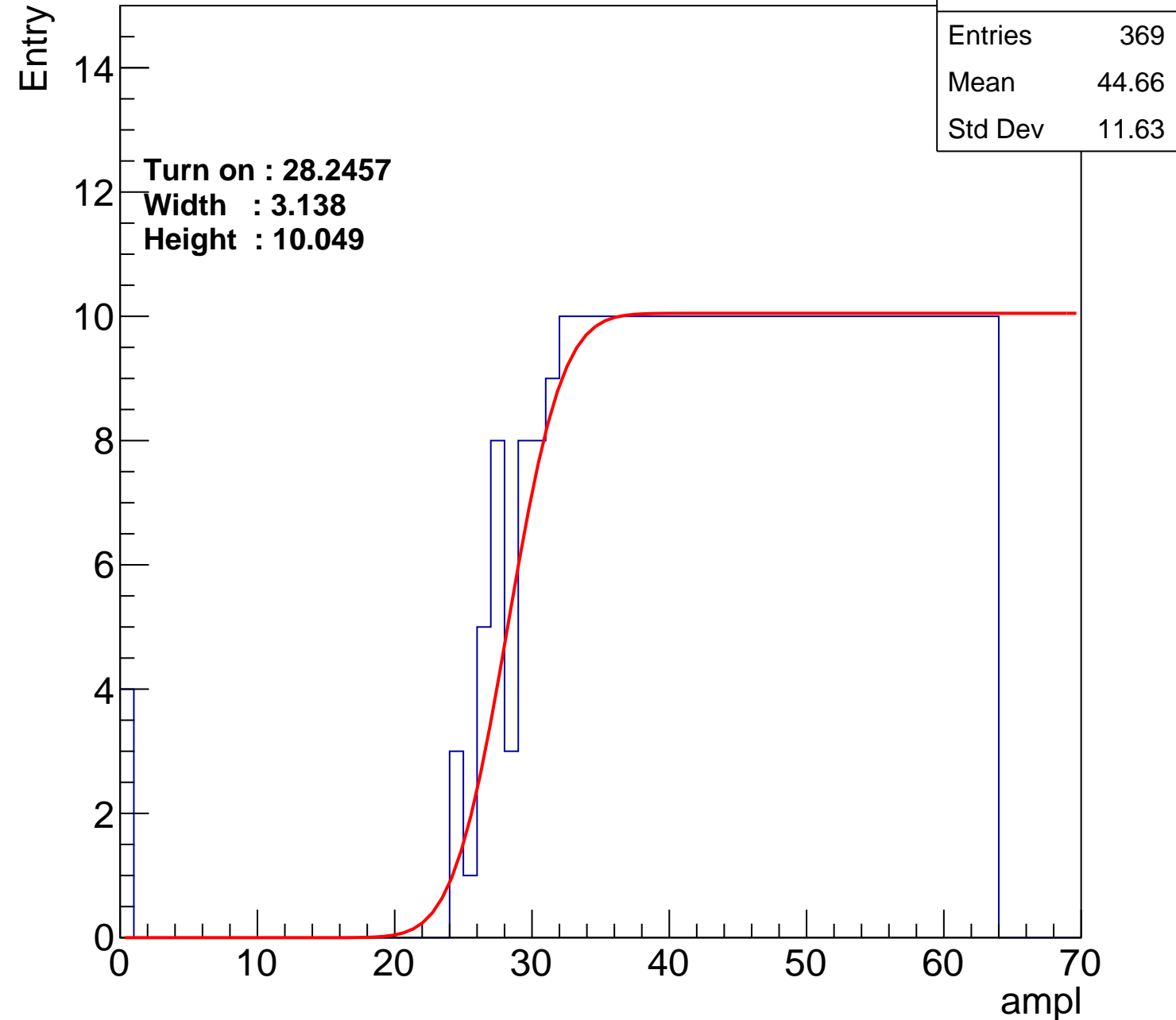
Width : 3.138

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch24

calib_packv5_042523_0143.root, FC#5, port B1

Entries	382
Mean	44.15
Std Dev	11.73

Turn on : 26.2038

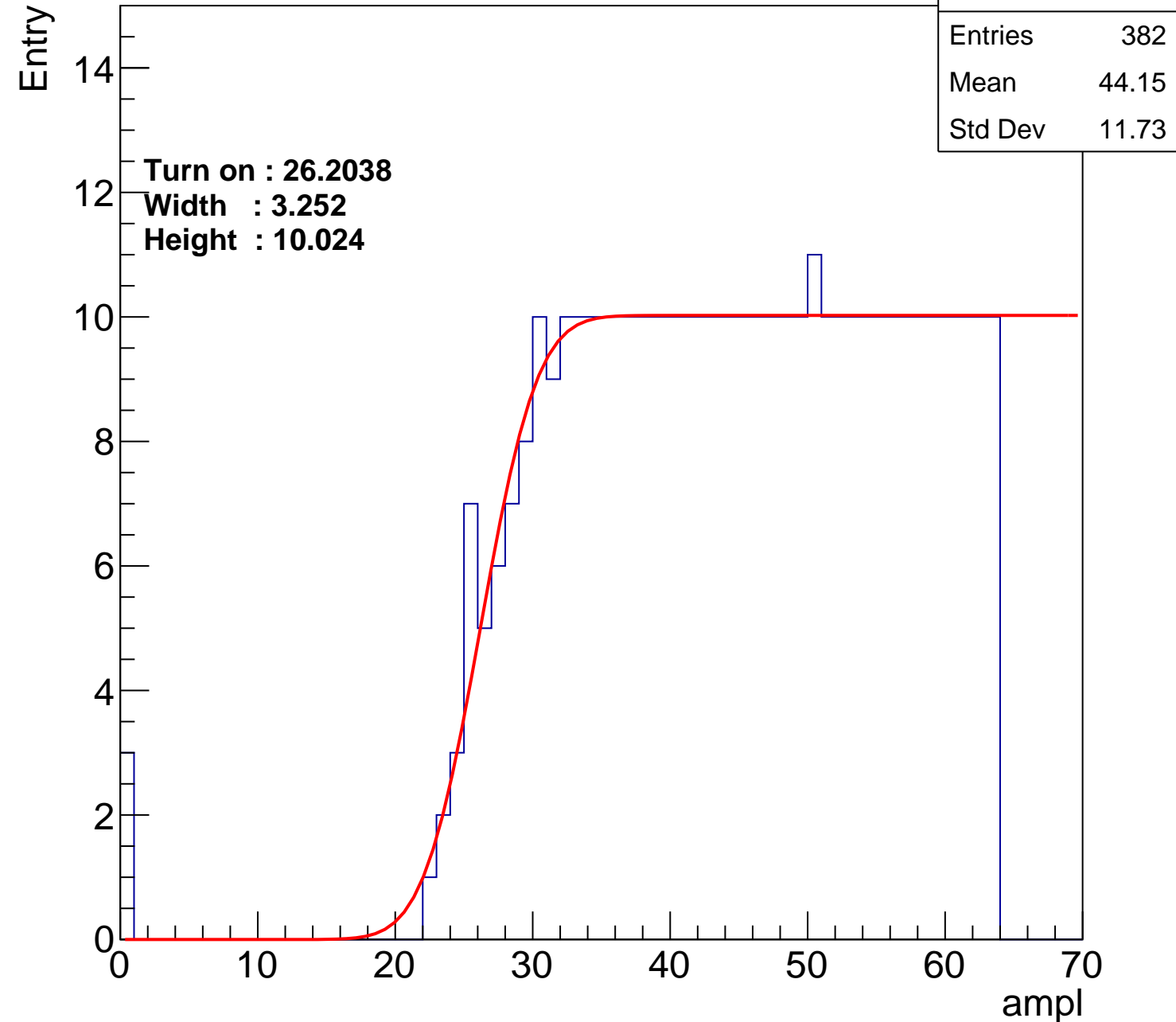
Width : 3.252

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch25

calib_packv5_042523_0143.root, FC#5, port B1

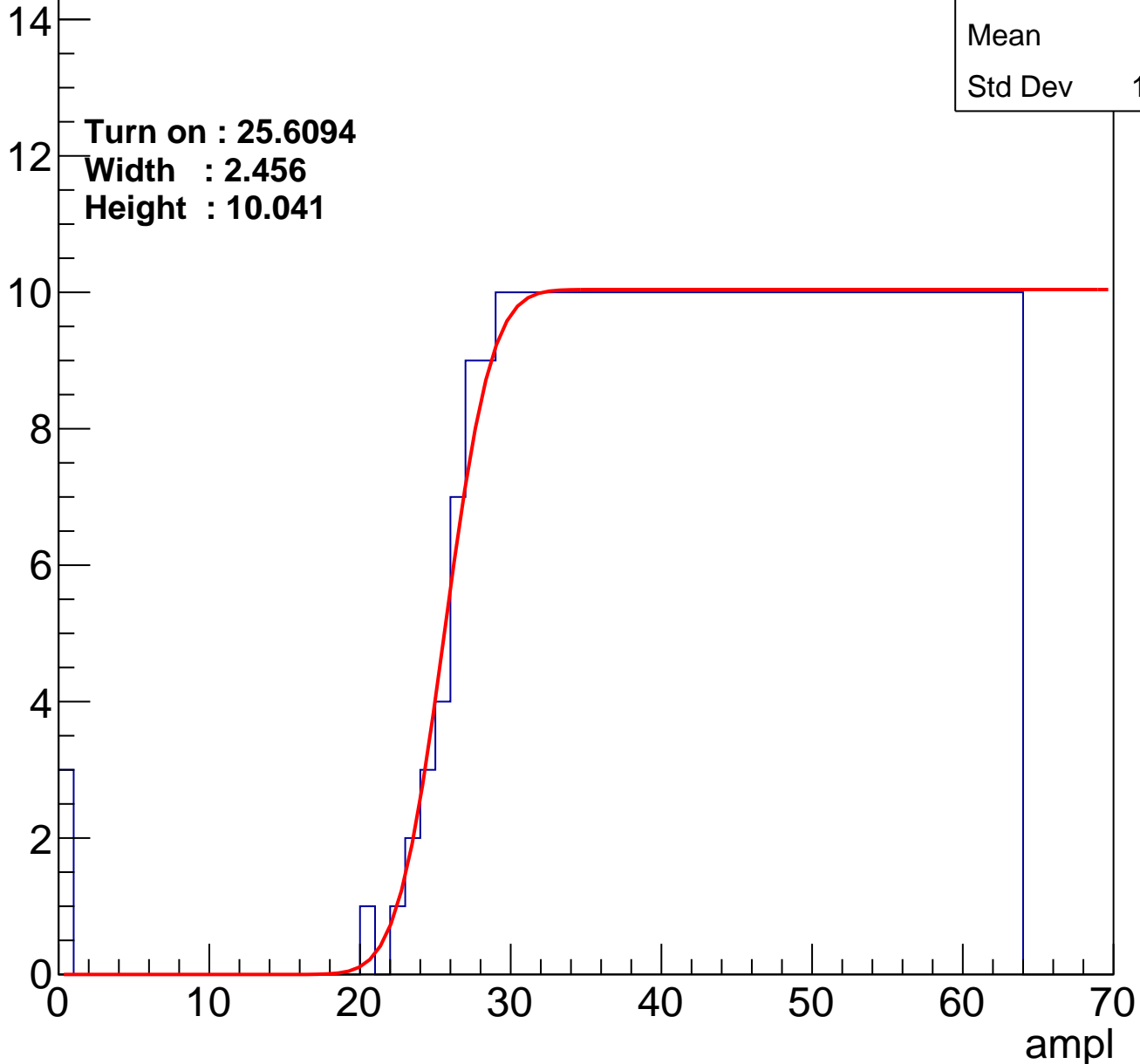
Entries	389
Mean	43.8
Std Dev	11.85

Turn on : 25.6094

Width : 2.456

Height : 10.041

Entry



B0L000S, U18-ch26

calib_packv5_042523_0143.root, FC#5, port B1

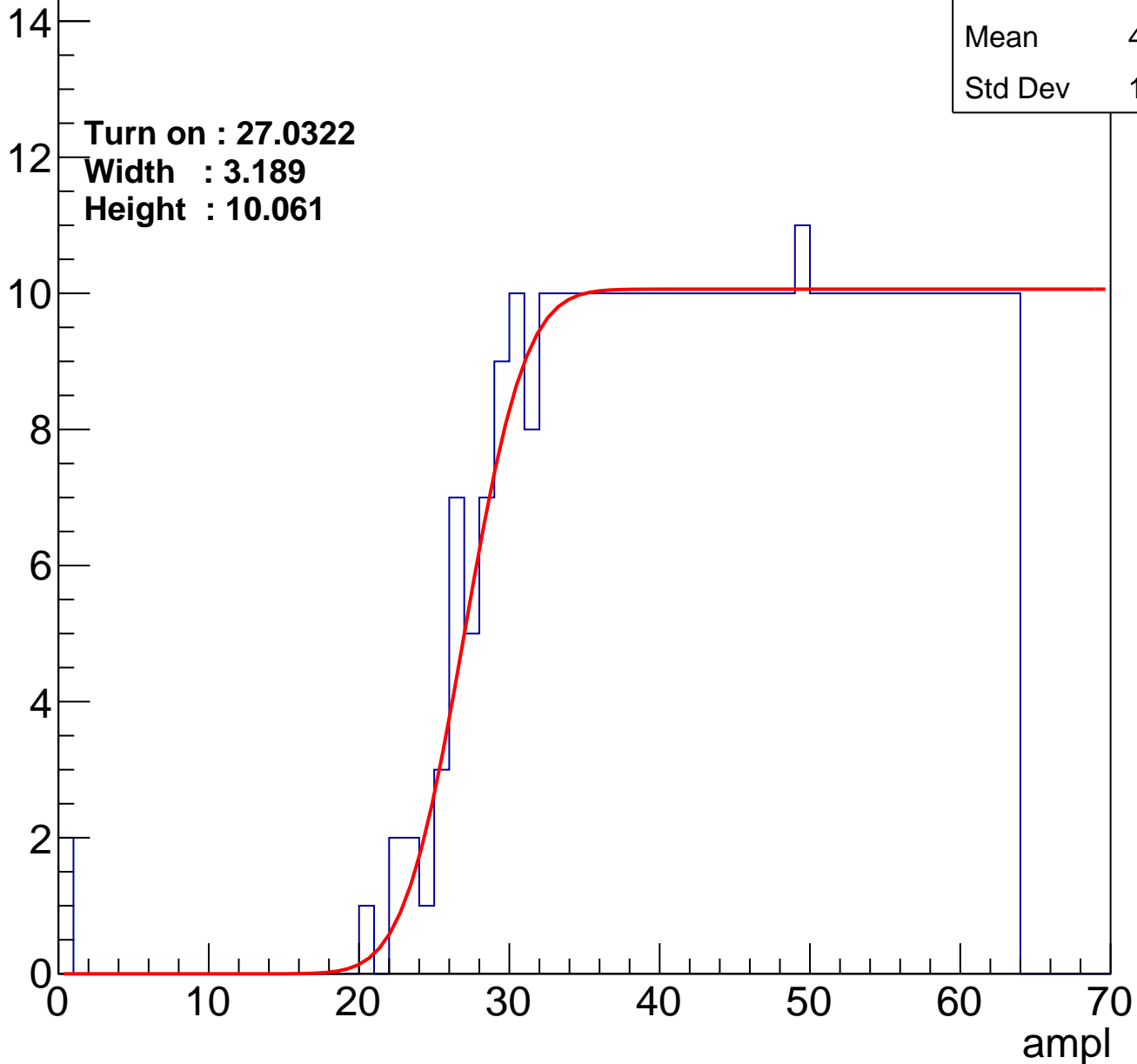
Entries	378
Mean	44.39
Std Dev	11.48

Turn on : 27.0322

Width : 3.189

Height : 10.061

Entry



B0L000S, U18-ch27

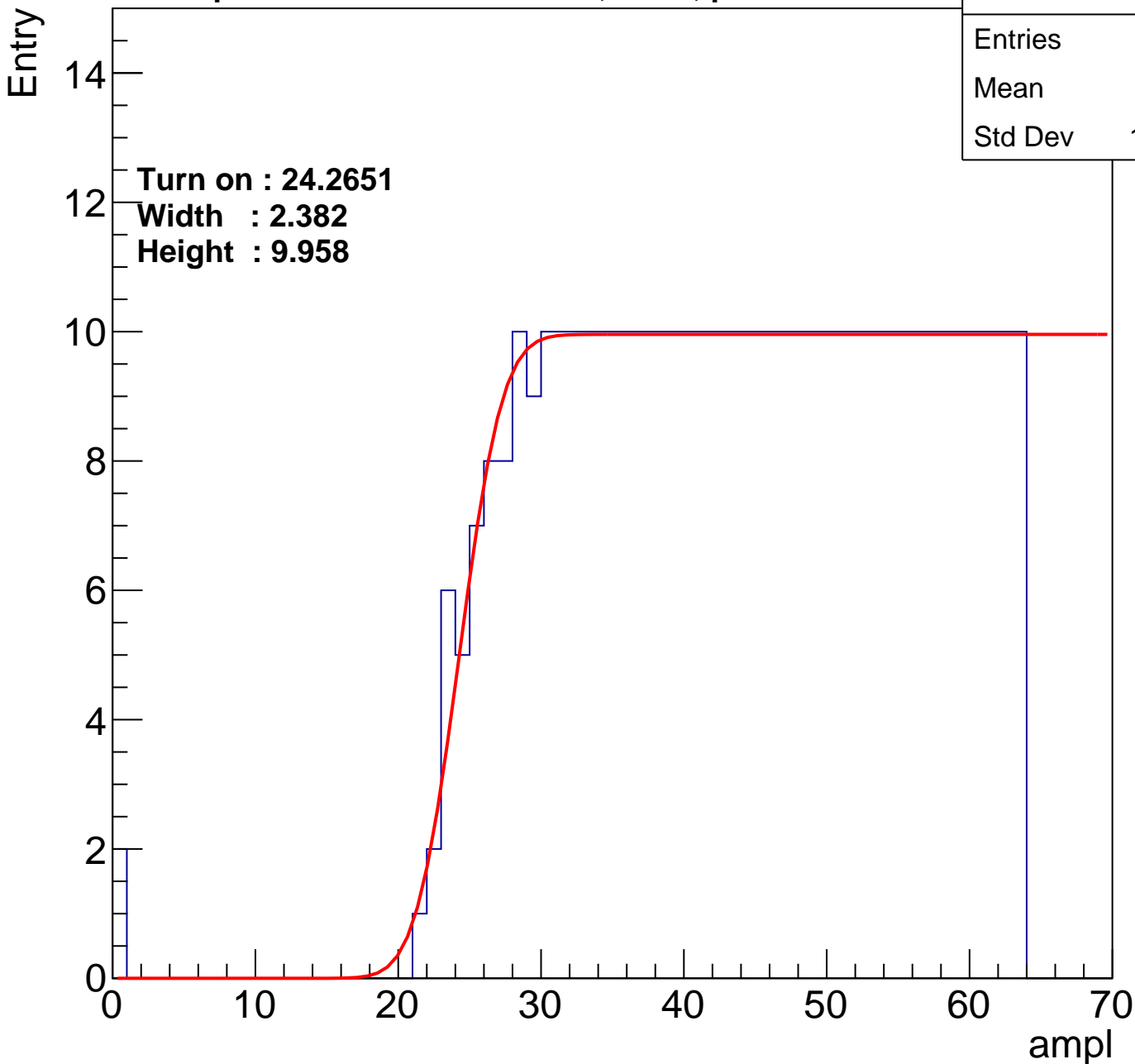
calib_packv5_042523_0143.root, FC#5, port B1

Entries	398
Mean	43.4
Std Dev	11.94

Turn on : 24.2651

Width : 2.382

Height : 9.958



B0L000S, U18-ch28

calib_packv5_042523_0143.root, FC#5, port B1

Entries	378
Mean	44.35
Std Dev	11.47

Turn on : 26.4528

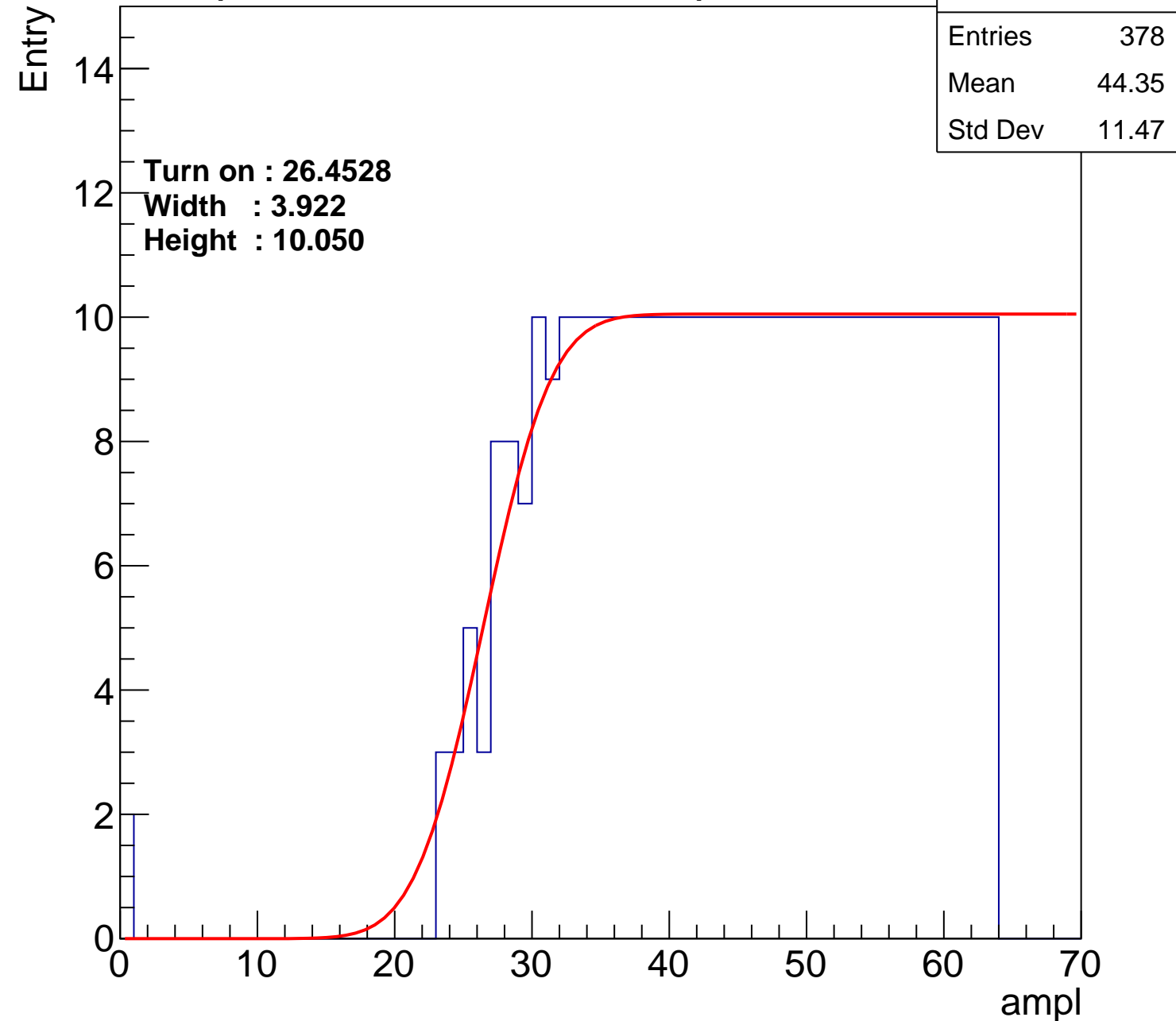
Width : 3.922

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch29

calib_packv5_042523_0143.root, FC#5, port B1

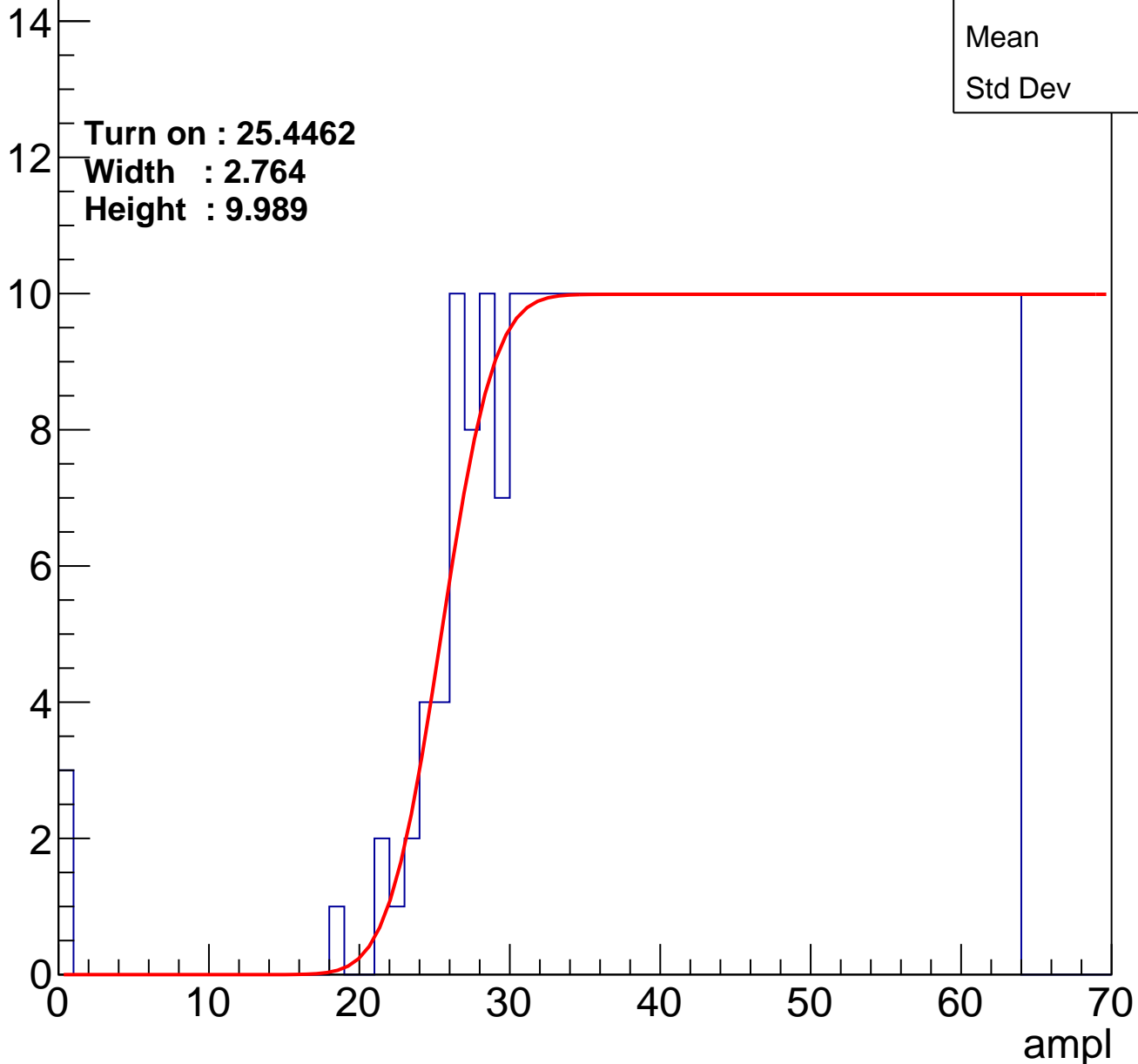
Entries	392
Mean	43.6
Std Dev	12

Turn on : 25.4462

Width : 2.764

Height : 9.989

Entry



B0L000S, U18-ch30

calib_packv5_042523_0143.root, FC#5, port B1

Entries	361
Mean	45.29
Std Dev	10.8

Turn on : 28.5717

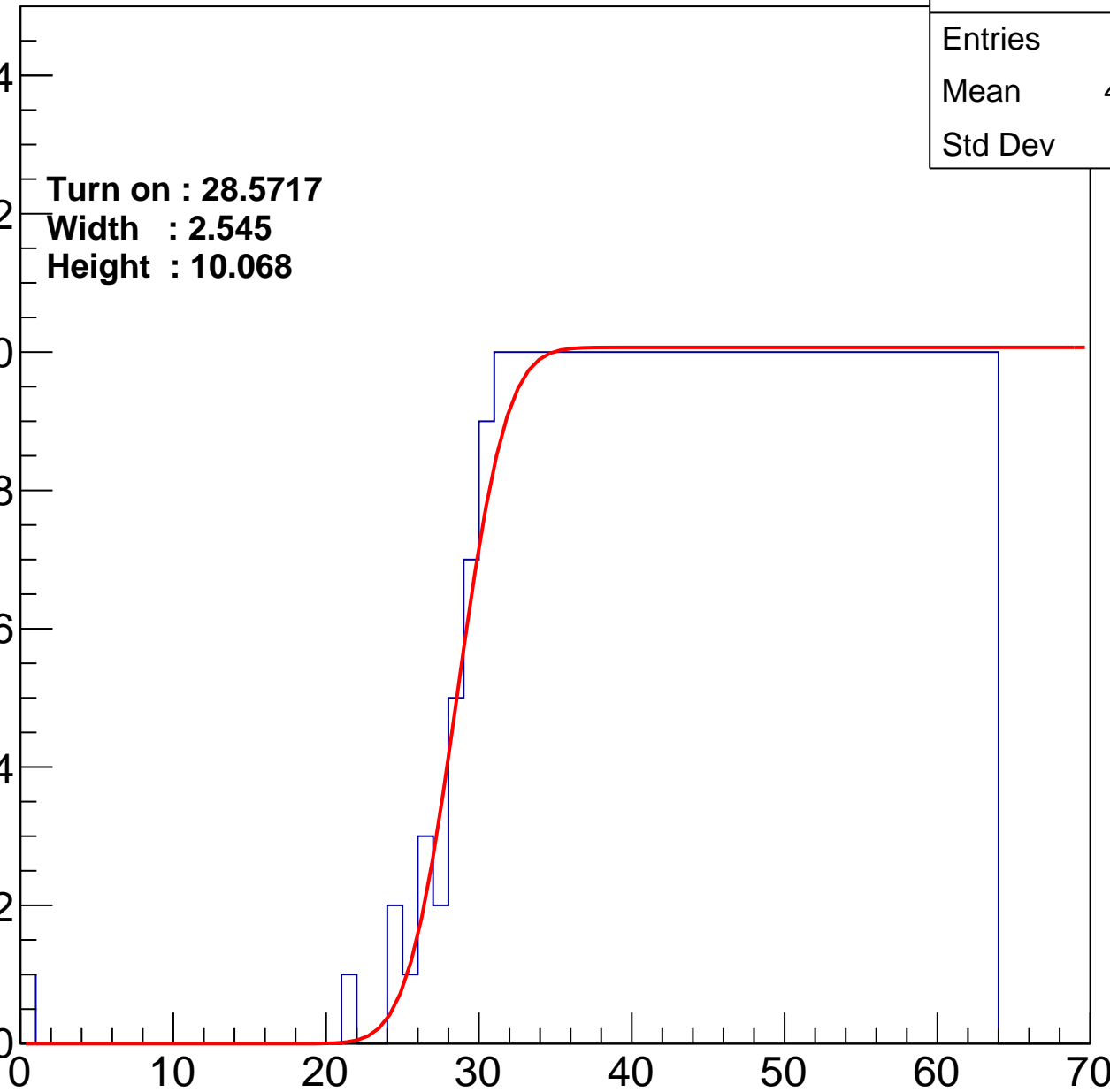
Width : 2.545

Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch31

calib_packv5_042523_0143.root, FC#5, port B1

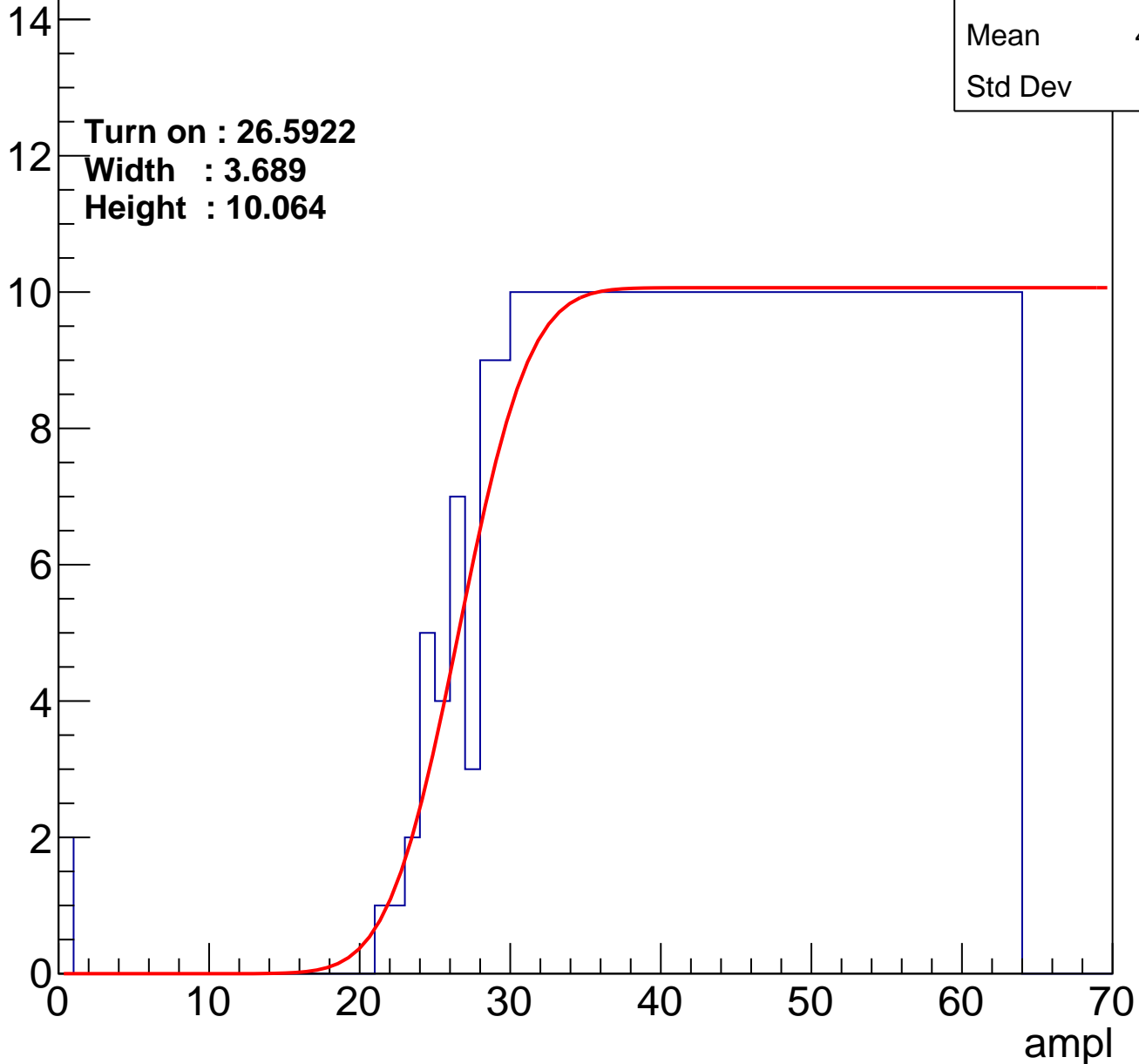
Entries	383
Mean	44.11
Std Dev	11.6

Turn on : 26.5922

Width : 3.689

Height : 10.064

Entry



B0L000S, U18-ch32

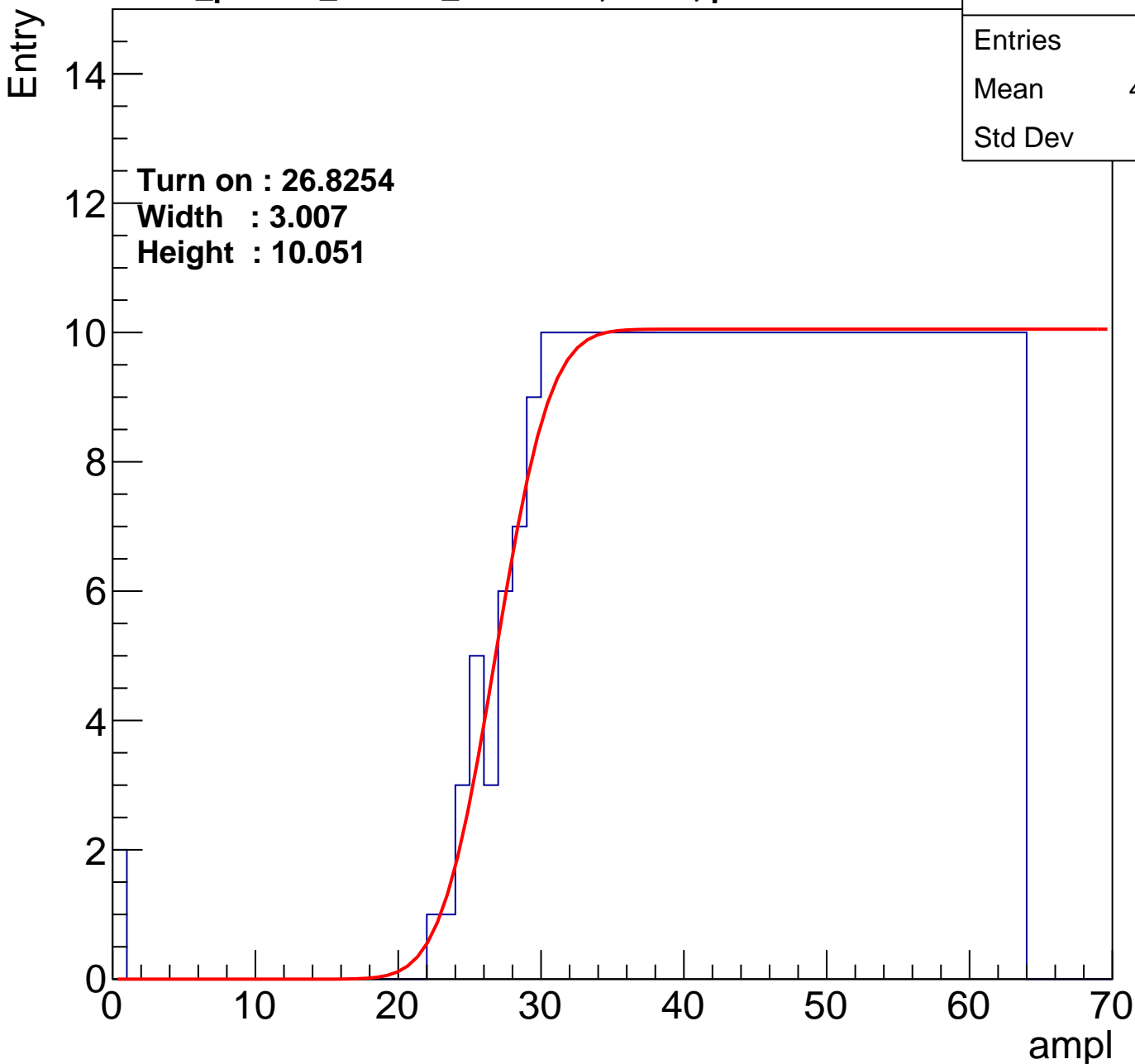
calib_packv5_042523_0143.root, FC#5, port B1

Entries	377
Mean	44.43
Std Dev	11.41

Turn on : 26.8254

Width : 3.007

Height : 10.051



B0L000S, U18-ch33

calib_packv5_042523_0143.root, FC#5, port B1

Entries	387
Mean	43.91
Std Dev	11.71

Turn on : 25.8571

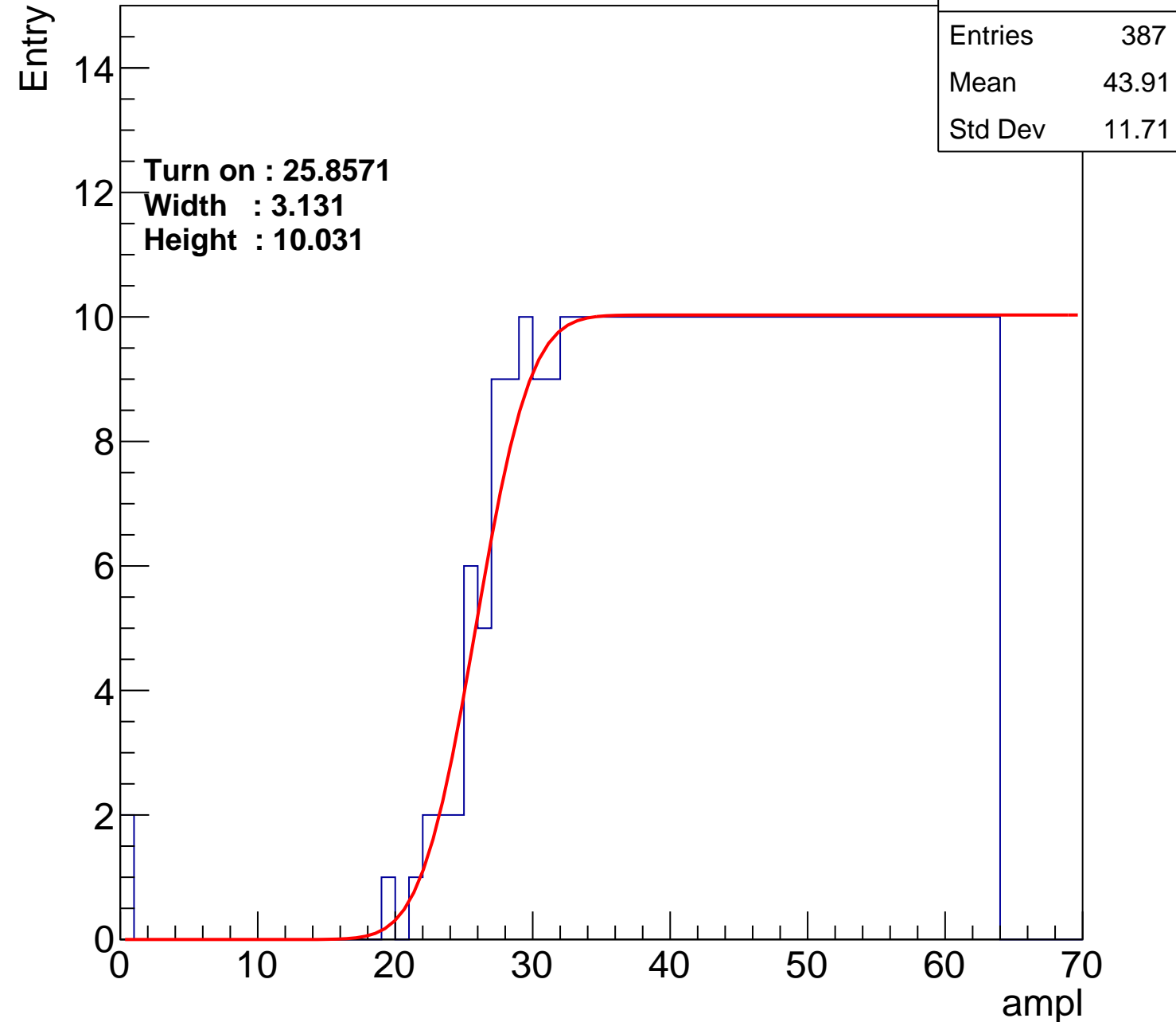
Width : 3.131

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch34

calib_packv5_042523_0143.root, FC#5, port B1

Entries	391
Mean	43.82
Std Dev	11.57

Turn on : 25.3100

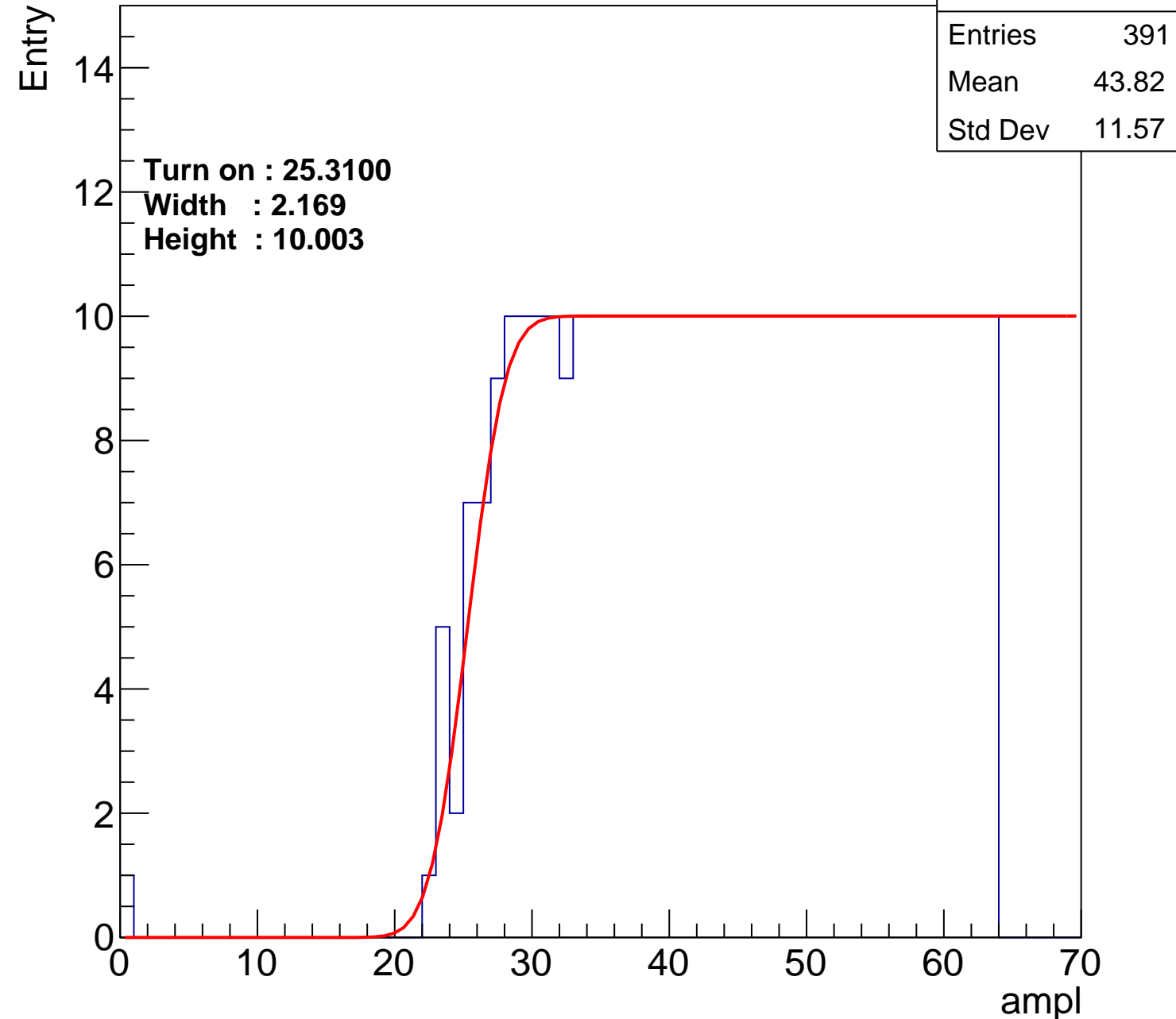
Width : 2.169

Height : 10.003

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch35

calib_packv5_042523_0143.root, FC#5, port B1

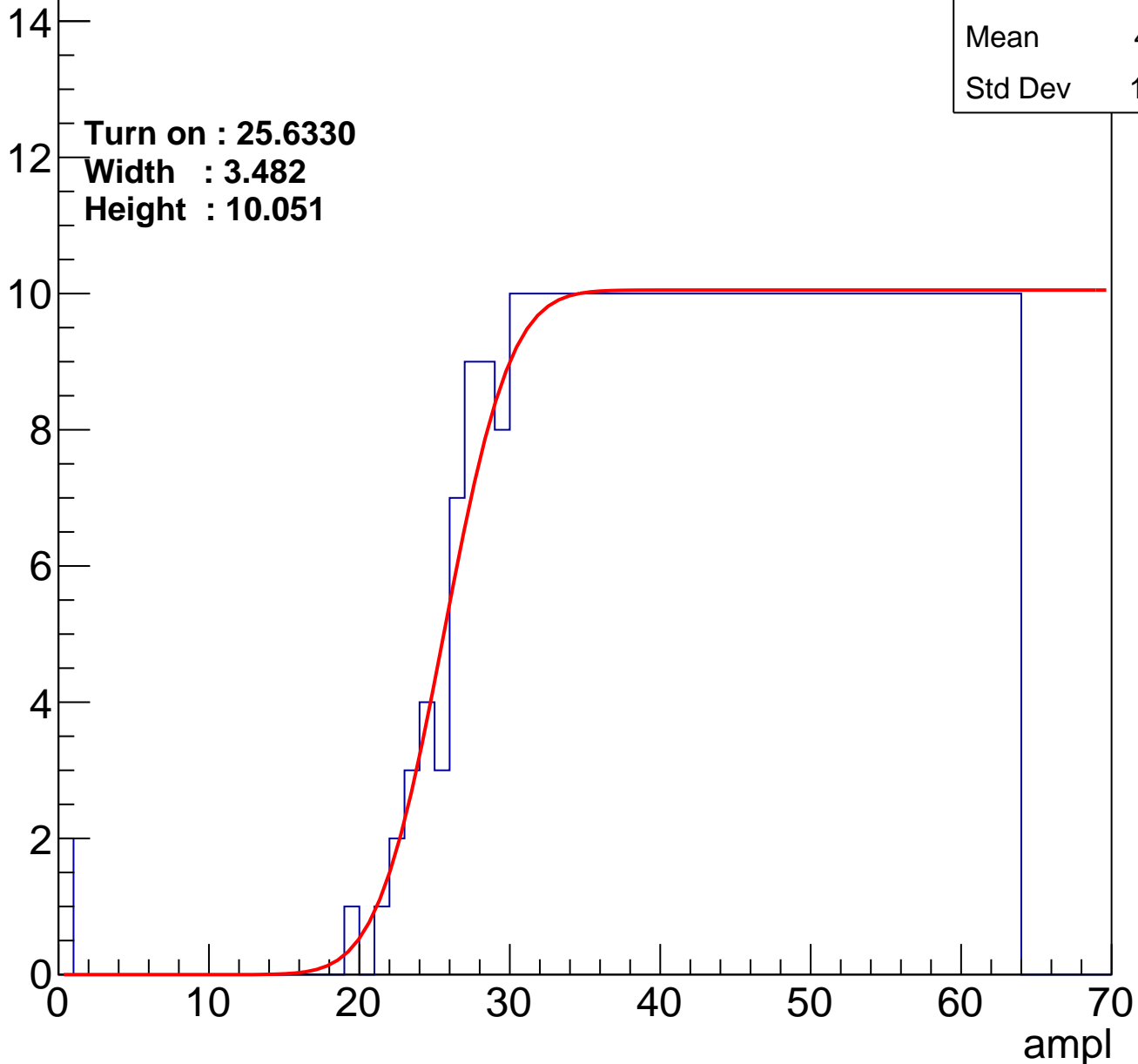
Entries	389
Mean	43.81
Std Dev	11.76

Turn on : 25.6330

Width : 3.482

Height : 10.051

Entry



B0L000S, U18-ch36

calib_packv5_042523_0143.root, FC#5, port B1

Entries	384
Mean	44.16
Std Dev	11.4

Turn on : 25.5363

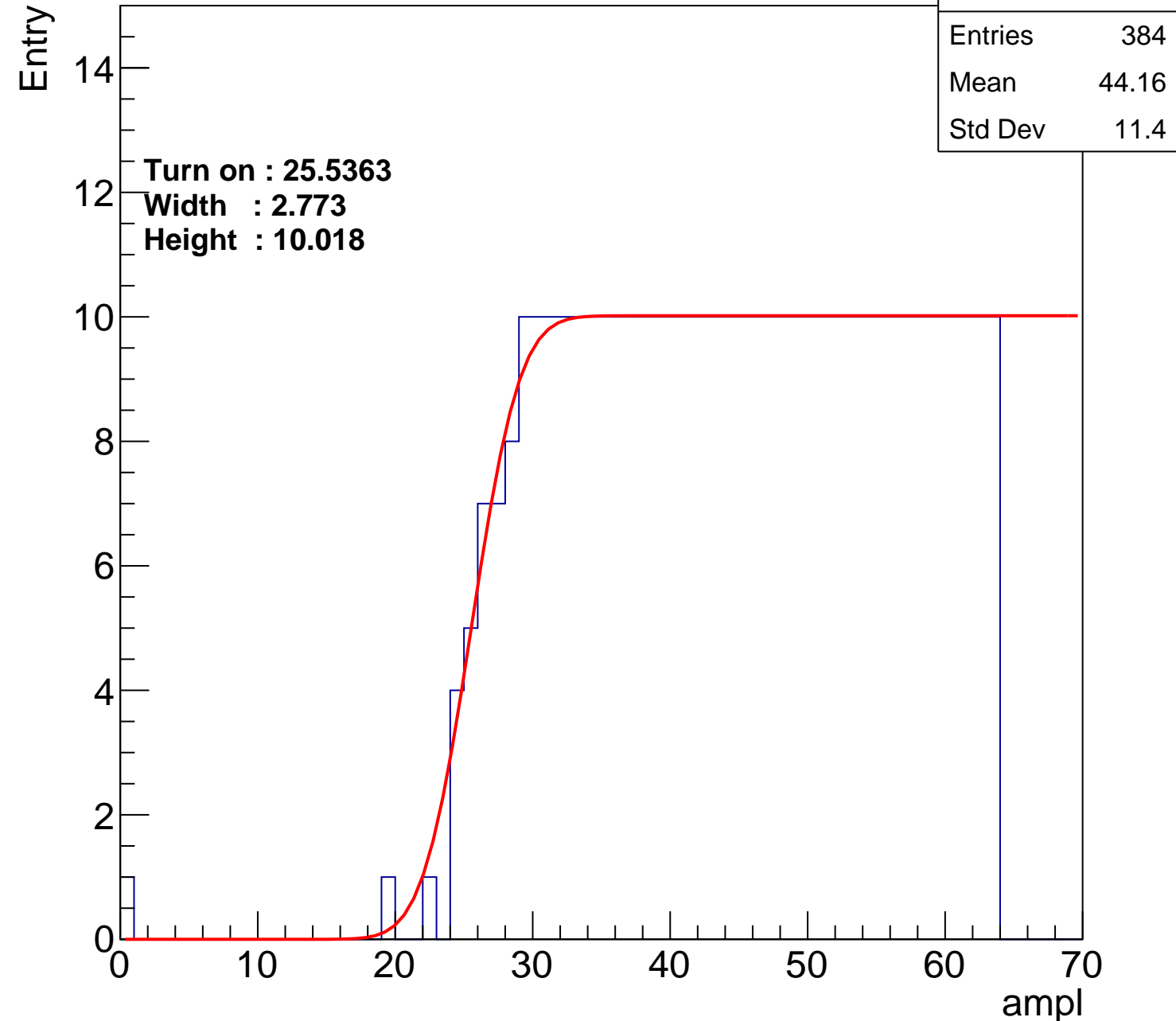
Width : 2.773

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch37

calib_packv5_042523_0143.root, FC#5, port B1

Entries	363
Mean	45.16
Std Dev	10.89

Turn on : 27.9304

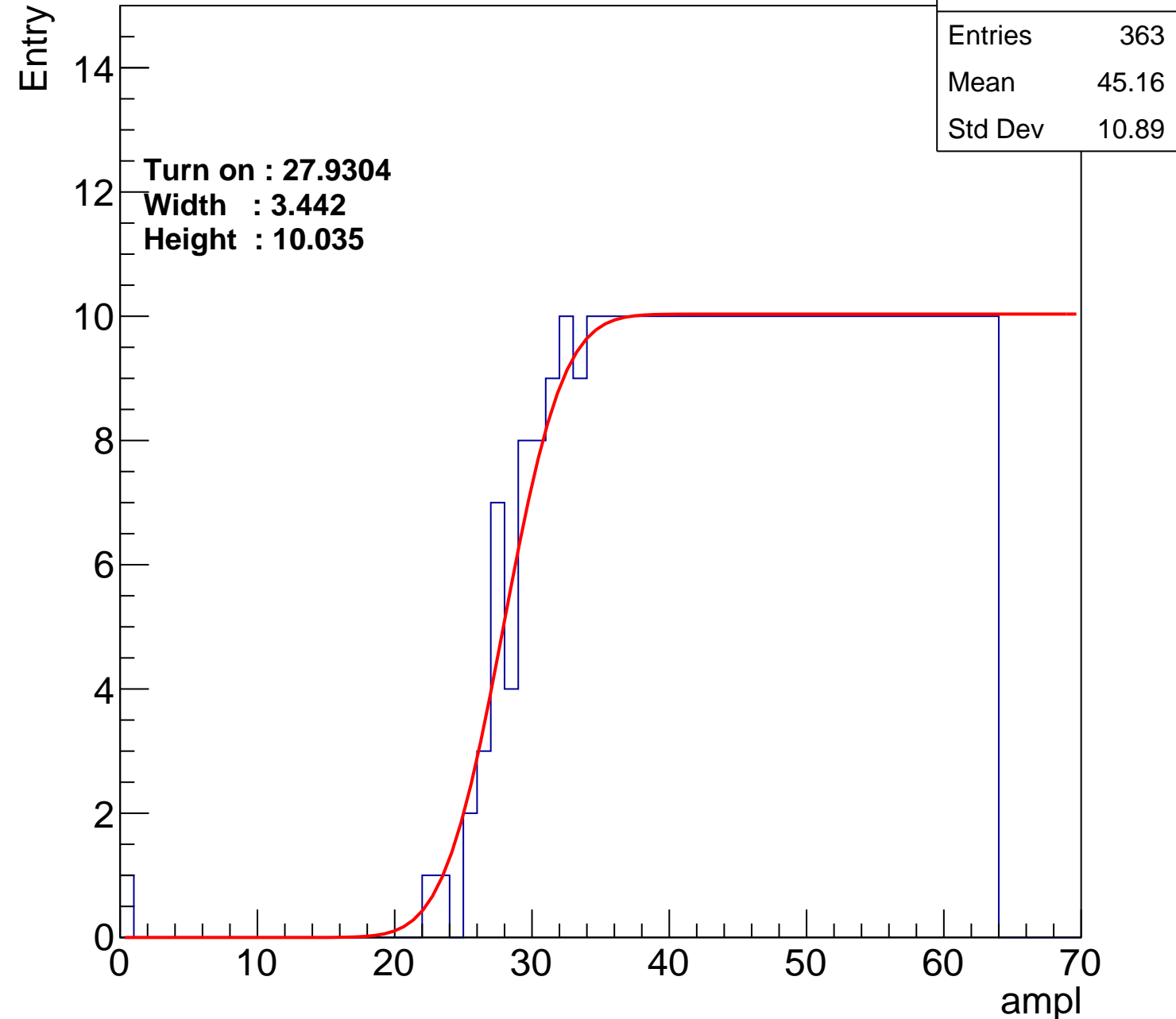
Width : 3.442

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch38

calib_packv5_042523_0143.root, FC#5, port B1

Entries	394
Mean	43.68
Std Dev	11.84

Turn on : 25.4348

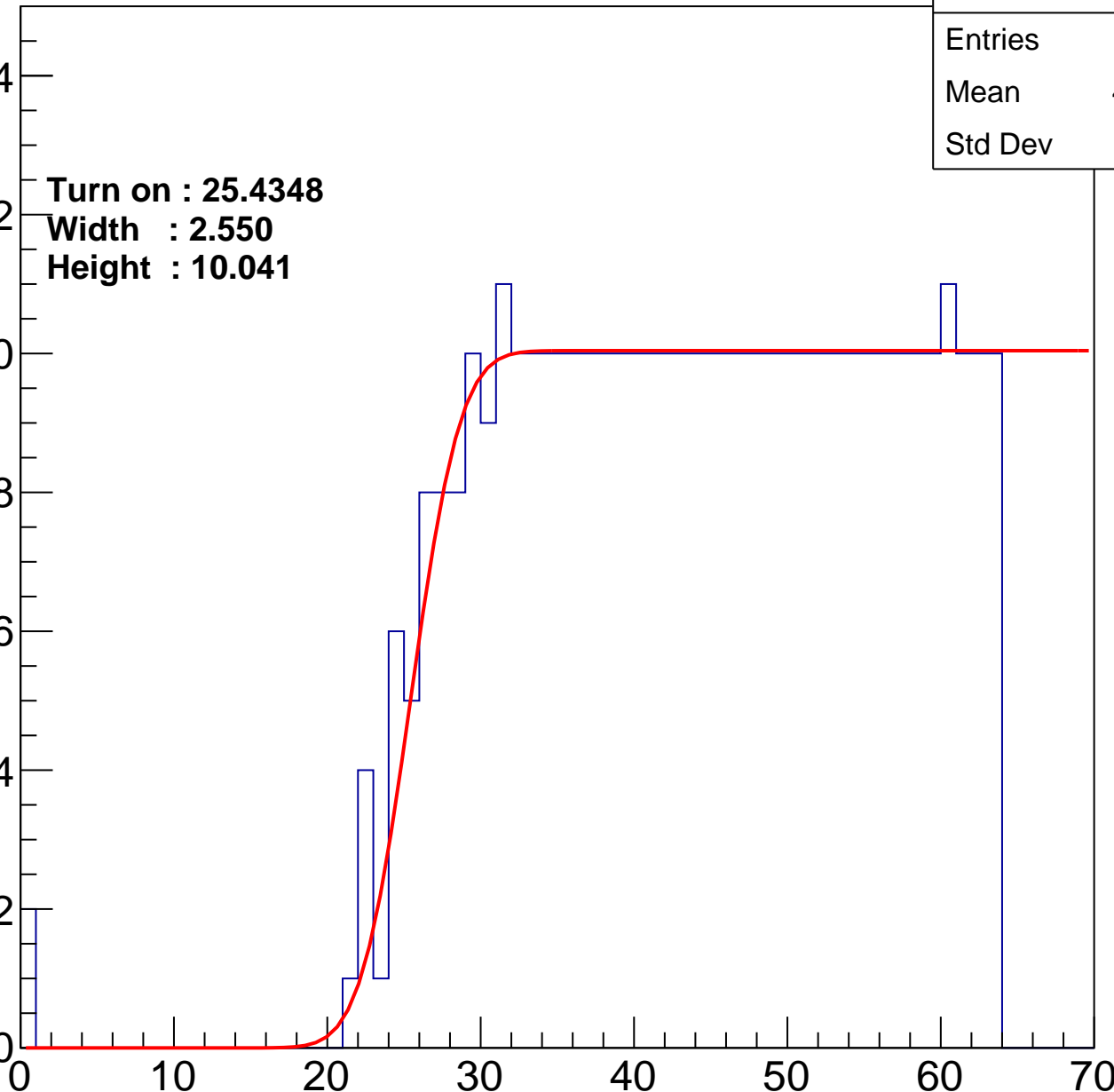
Width : 2.550

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch39

calib_packv5_042523_0143.root, FC#5, port B1

Entries	376
Mean	44.4
Std Dev	11.5

Turn on : 27.1786

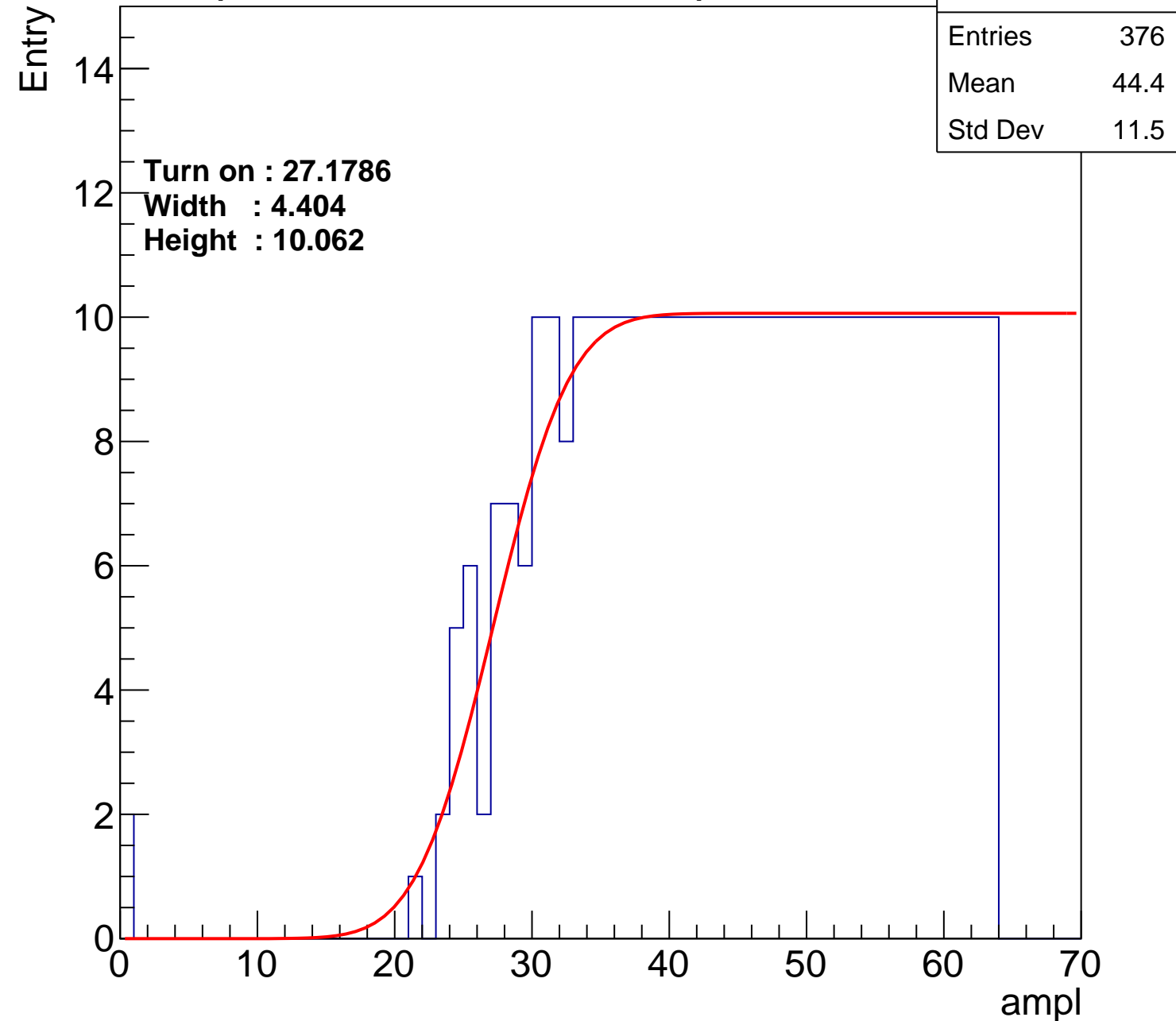
Width : 4.404

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch40

calib_packv5_042523_0143.root, FC#5, port B1

Entries	378
Mean	44.28
Std Dev	11.75

Turn on : 27.0166

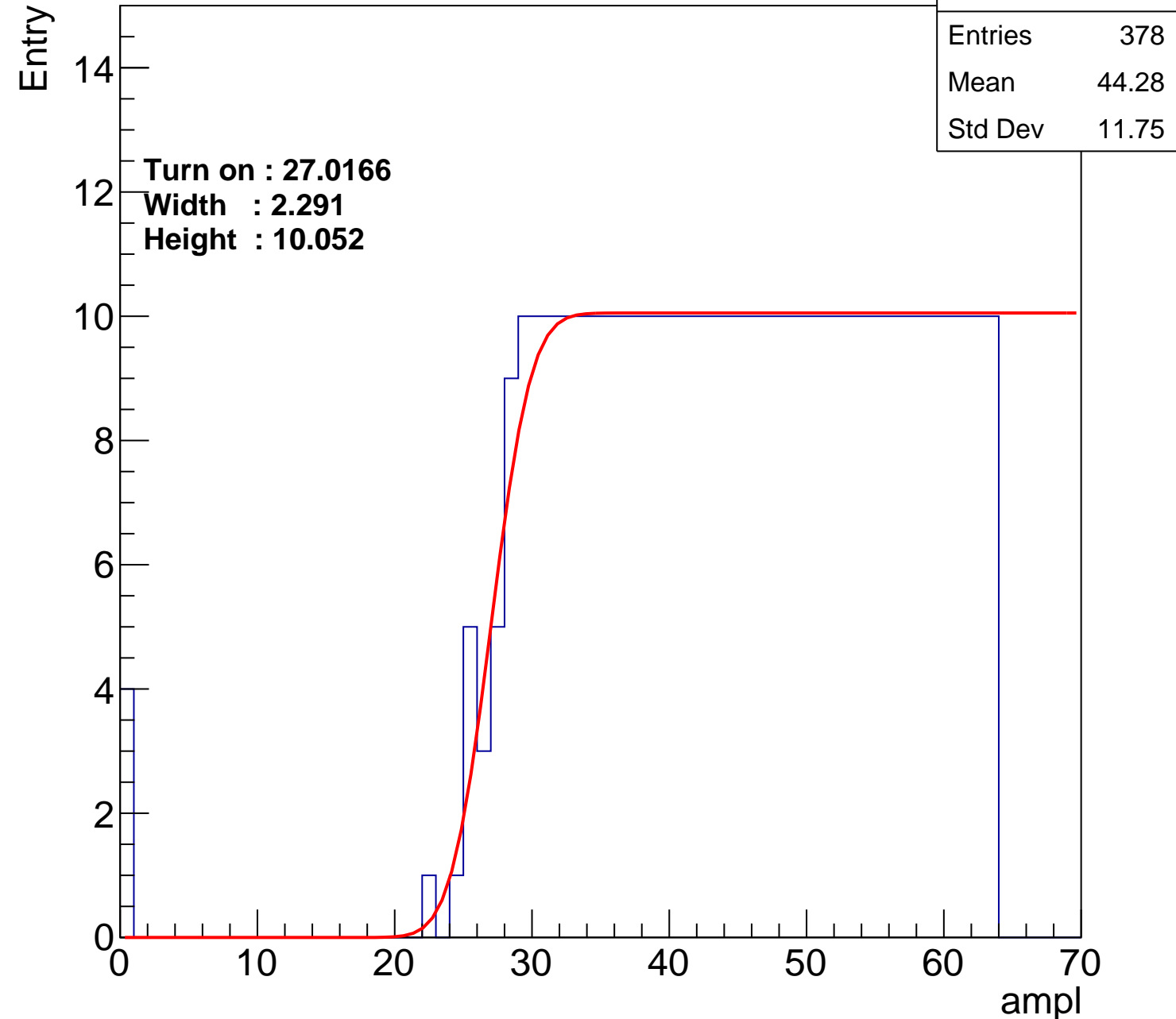
Width : 2.291

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch41

calib_packv5_042523_0143.root, FC#5, port B1

Entries	365
Mean	45.08
Std Dev	11.07

Turn on : 27.4004

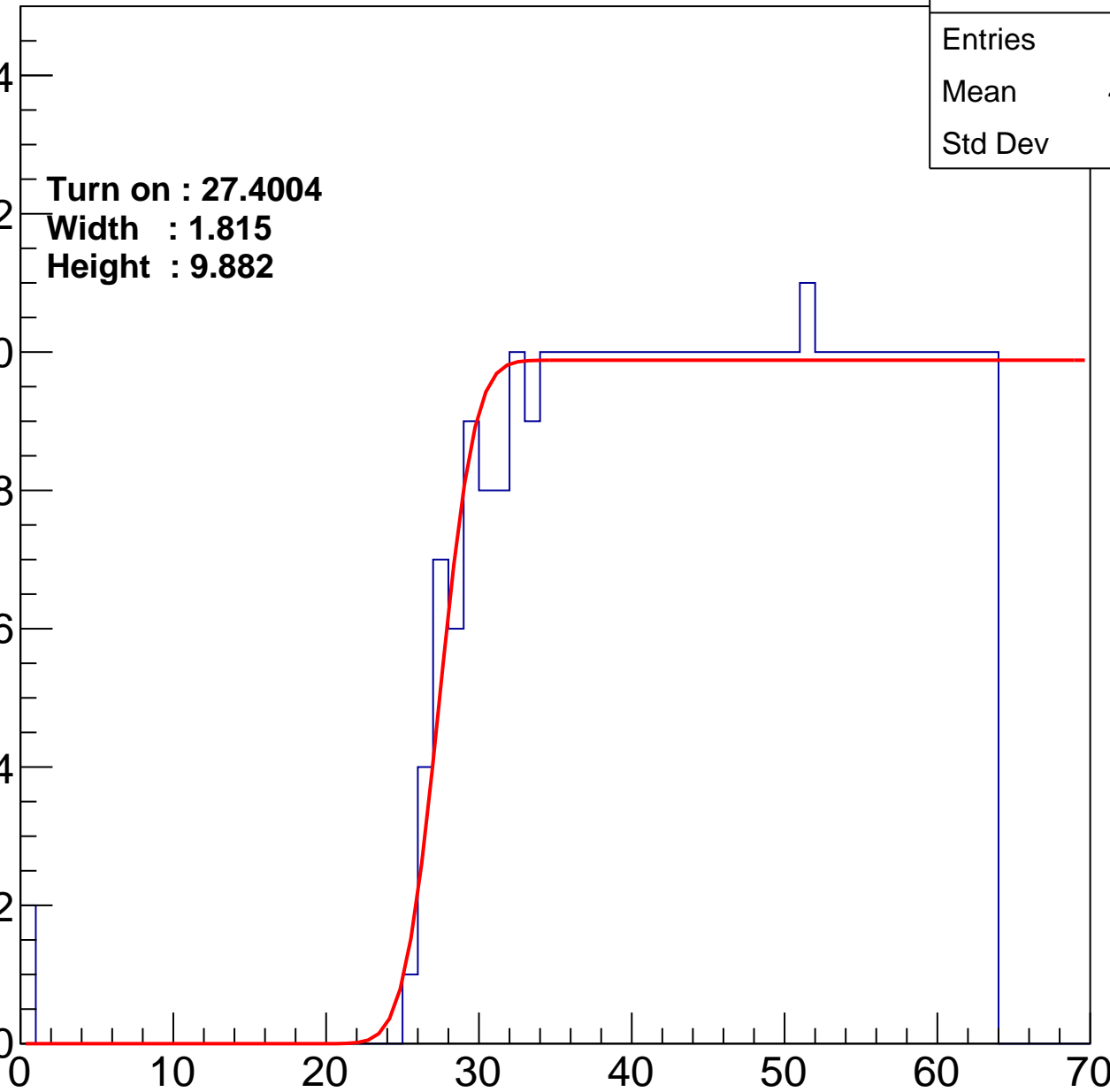
Width : 1.815

Height : 9.882

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch42

calib_packv5_042523_0143.root, FC#5, port B1

Entries	377
Mean	44.29
Std Dev	11.78

Turn on : 27.1733

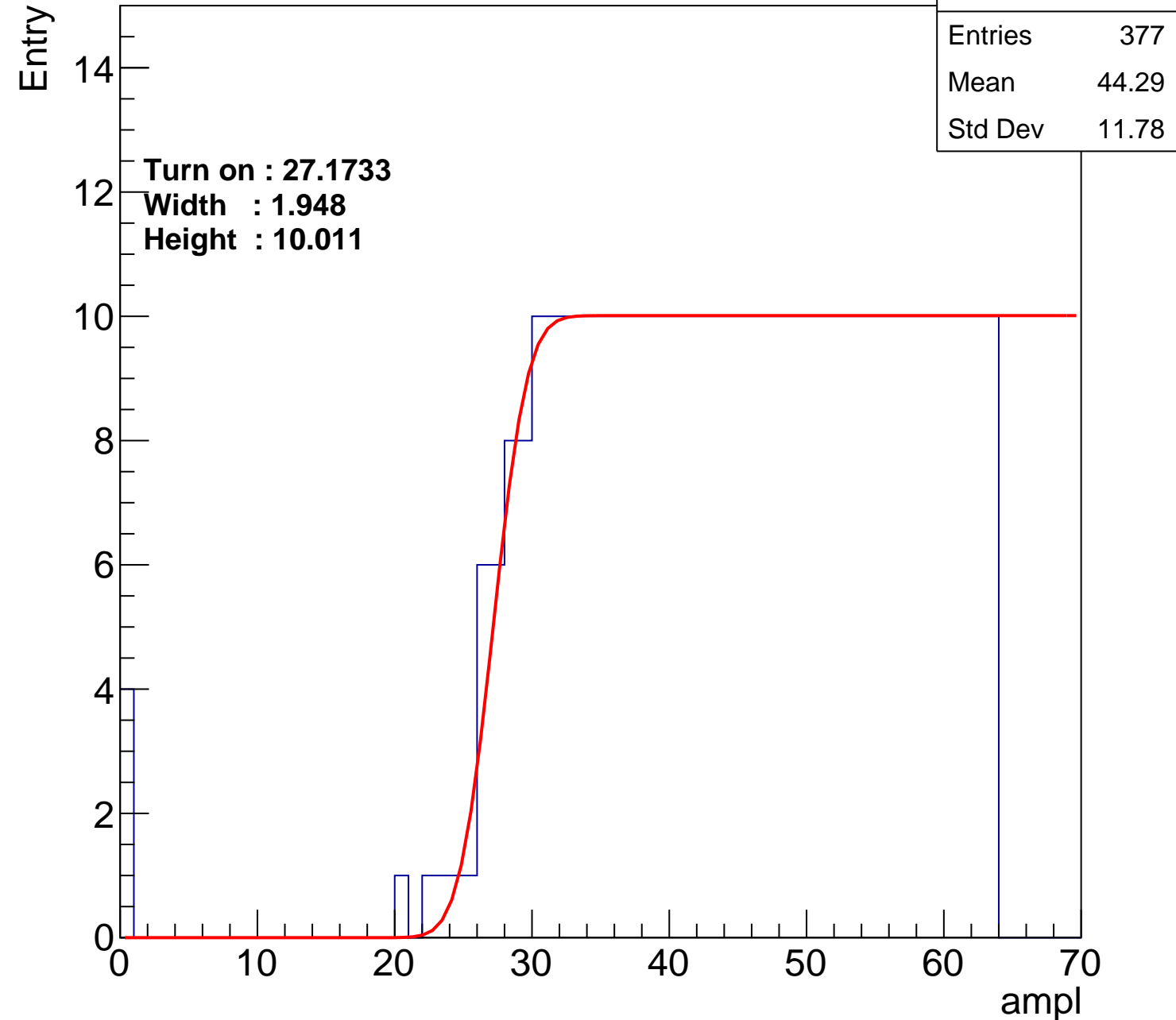
Width : 1.948

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch43

calib_packv5_042523_0143.root, FC#5, port B1

Entries	398
Mean	43.37
Std Dev	11.99

Turn on : 24.3189

Width : 3.727

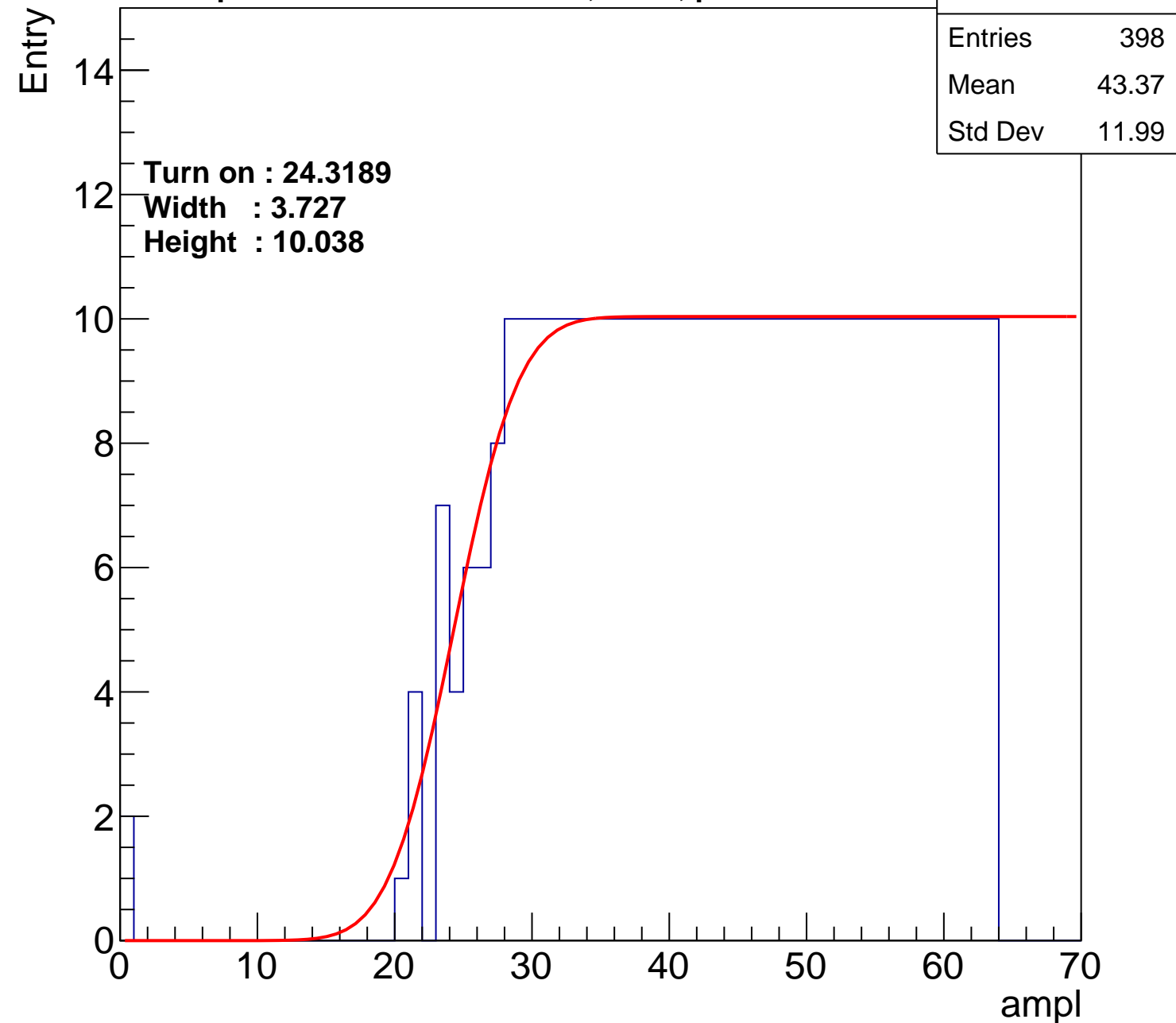
Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B0L000S, U18-ch44

calib_packv5_042523_0143.root, FC#5, port B1

Entries	365
Mean	44.99
Std Dev	11.14

Turn on : 27.6988

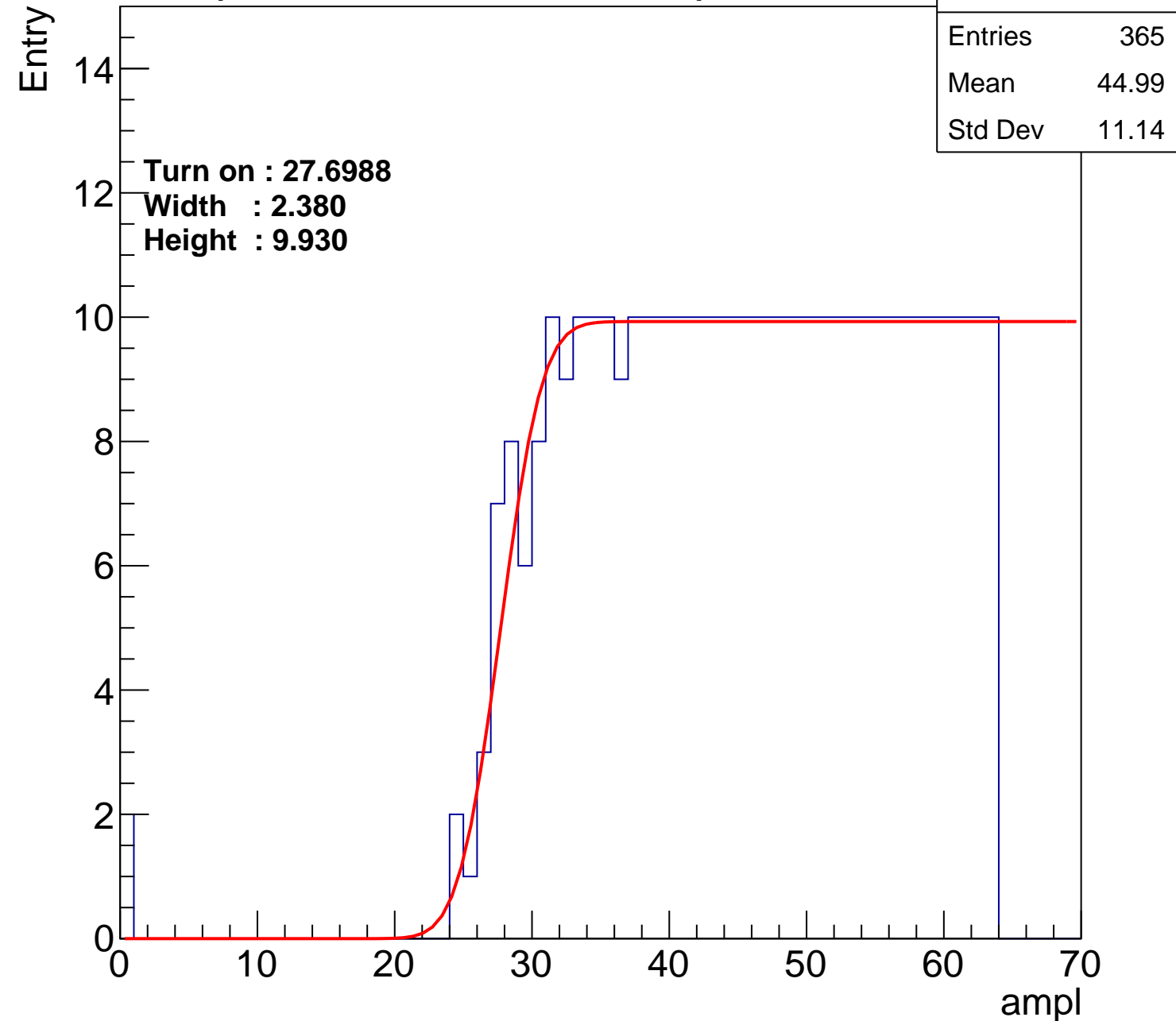
Width : 2.380

Height : 9.930

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch45

calib_packv5_042523_0143.root, FC#5, port B1

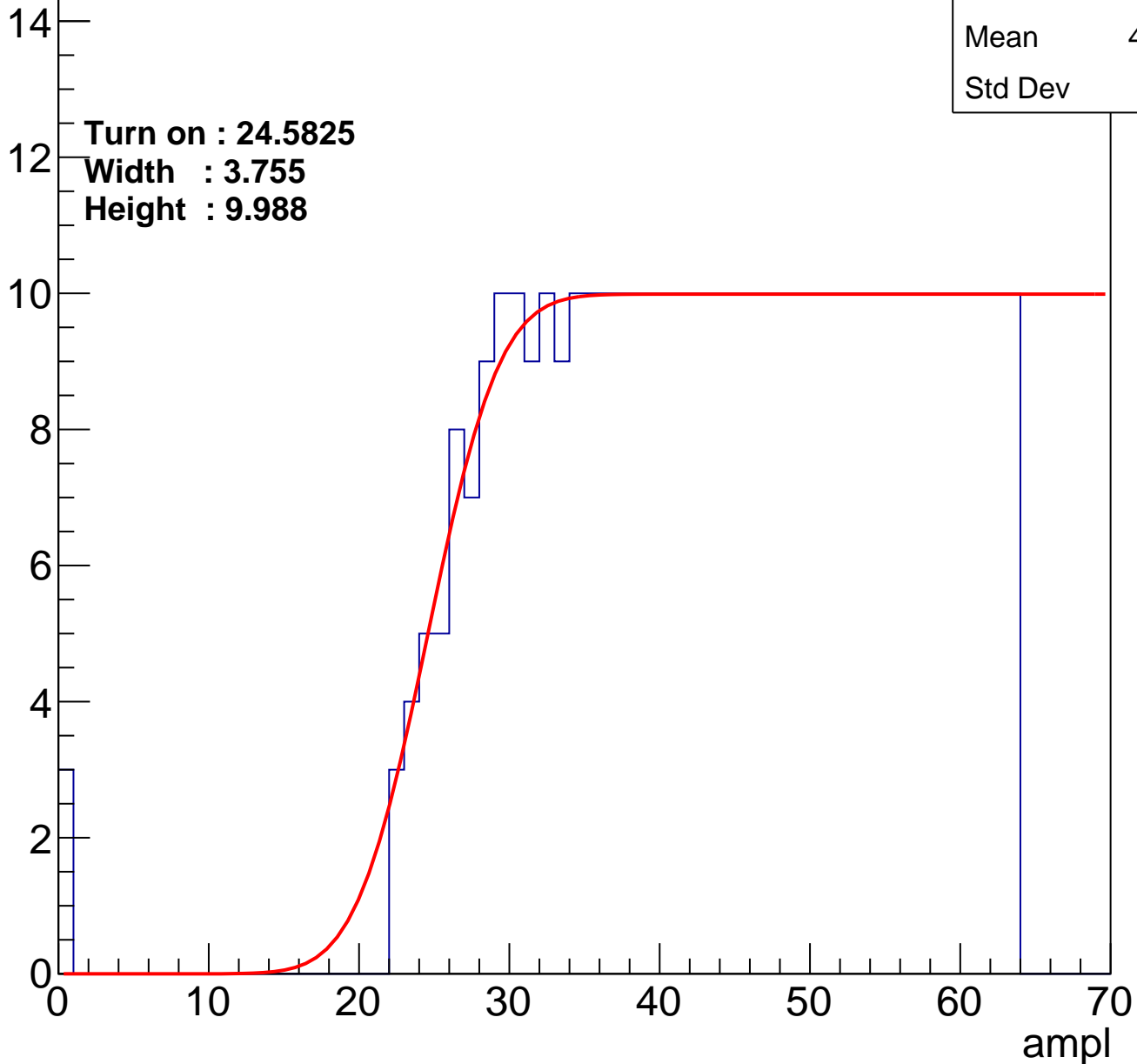
Entries	392
Mean	43.59
Std Dev	12

Turn on : 24.5825

Width : 3.755

Height : 9.988

Entry



B0L000S, U18-ch46

calib_packv5_042523_0143.root, FC#5, port B1

Entries	362
Mean	45.2
Std Dev	10.87

Turn on : 28.1664

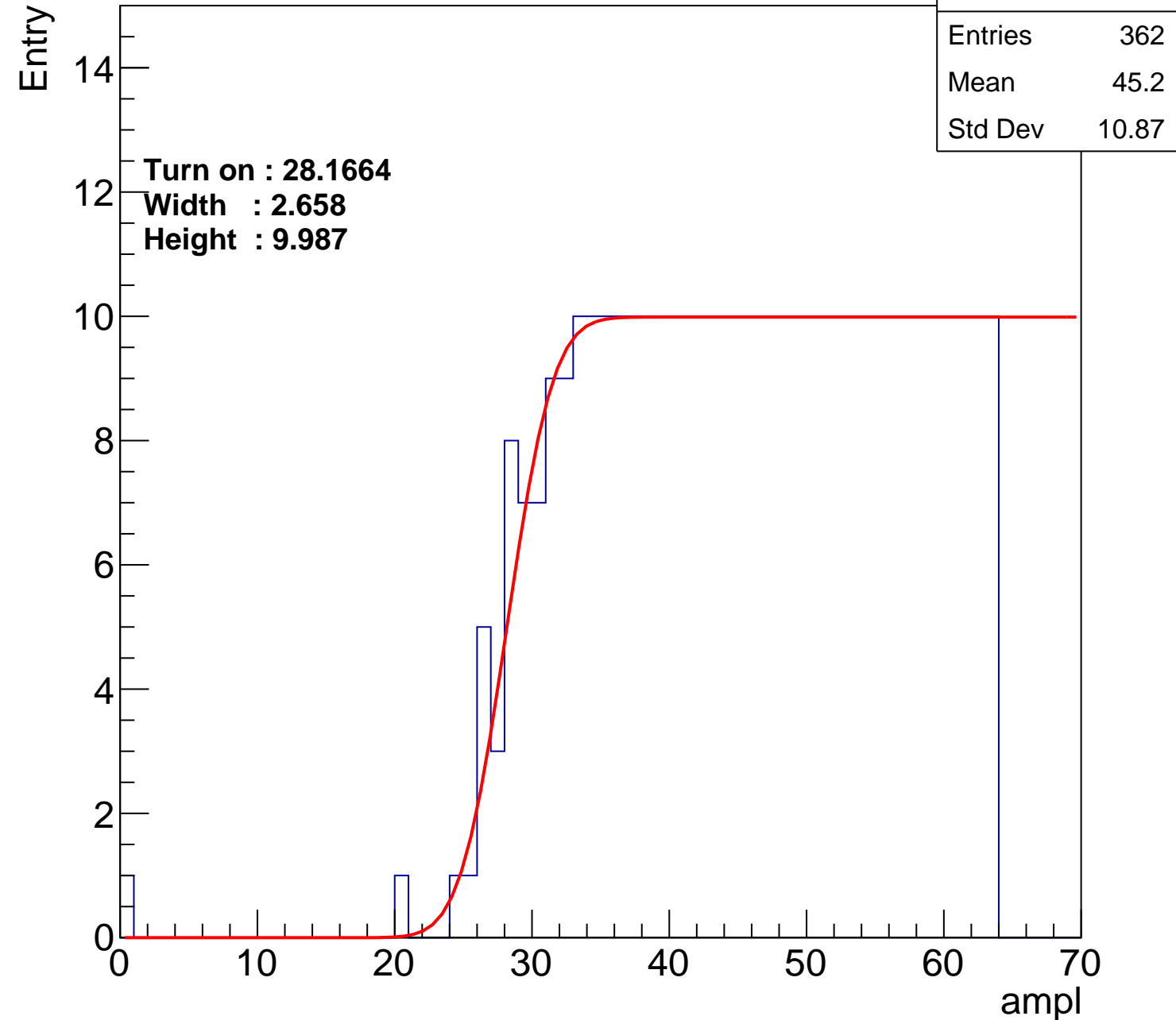
Width : 2.658

Height : 9.987

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch47

calib_packv5_042523_0143.root, FC#5, port B1

Entries	386
Mean	43.96
Std Dev	11.68

Turn on : 25.6939

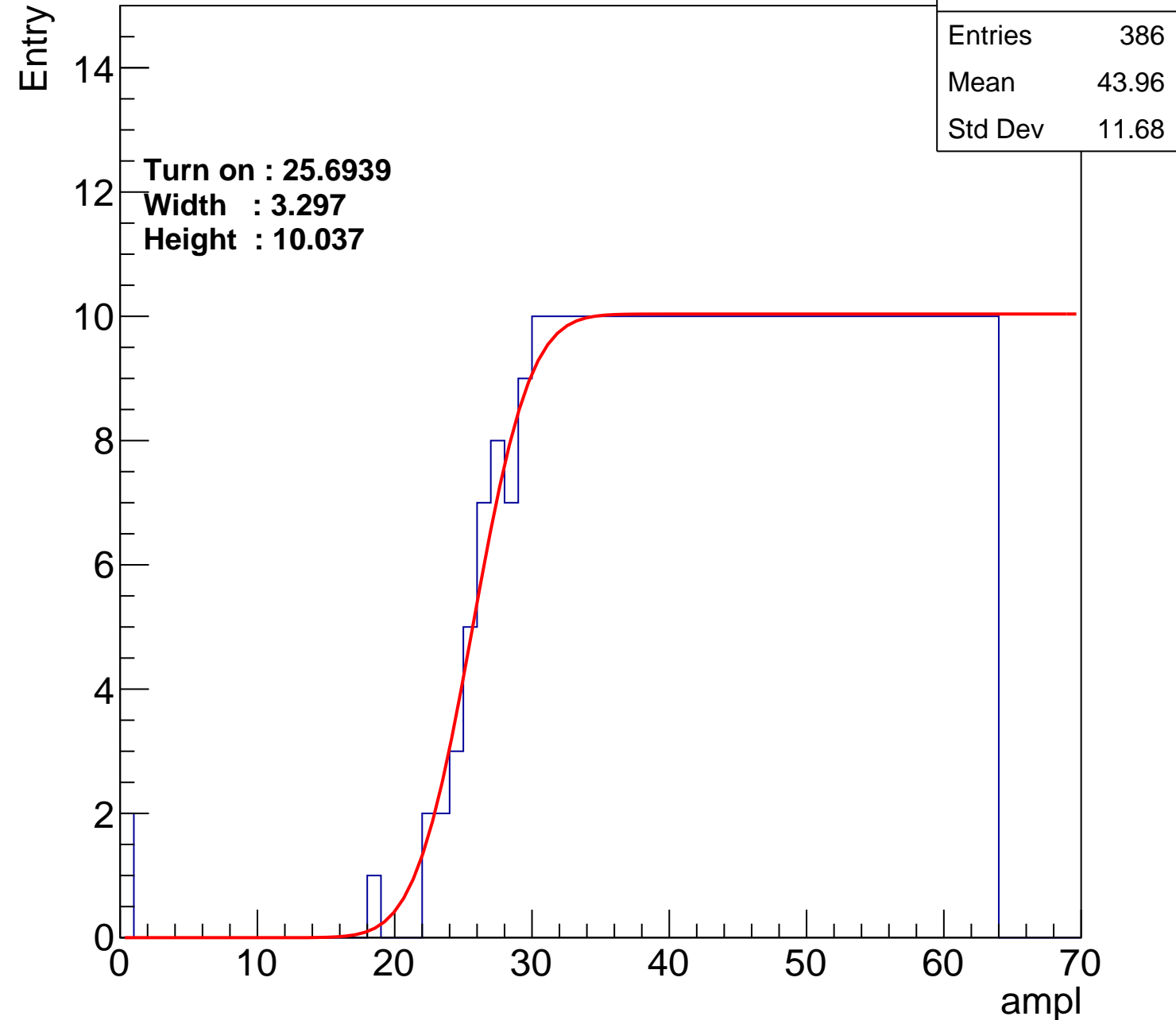
Width : 3.297

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch48

calib_packv5_042523_0143.root, FC#5, port B1

Entries	372
Mean	44.79
Std Dev	11.01

Turn on : 27.1417

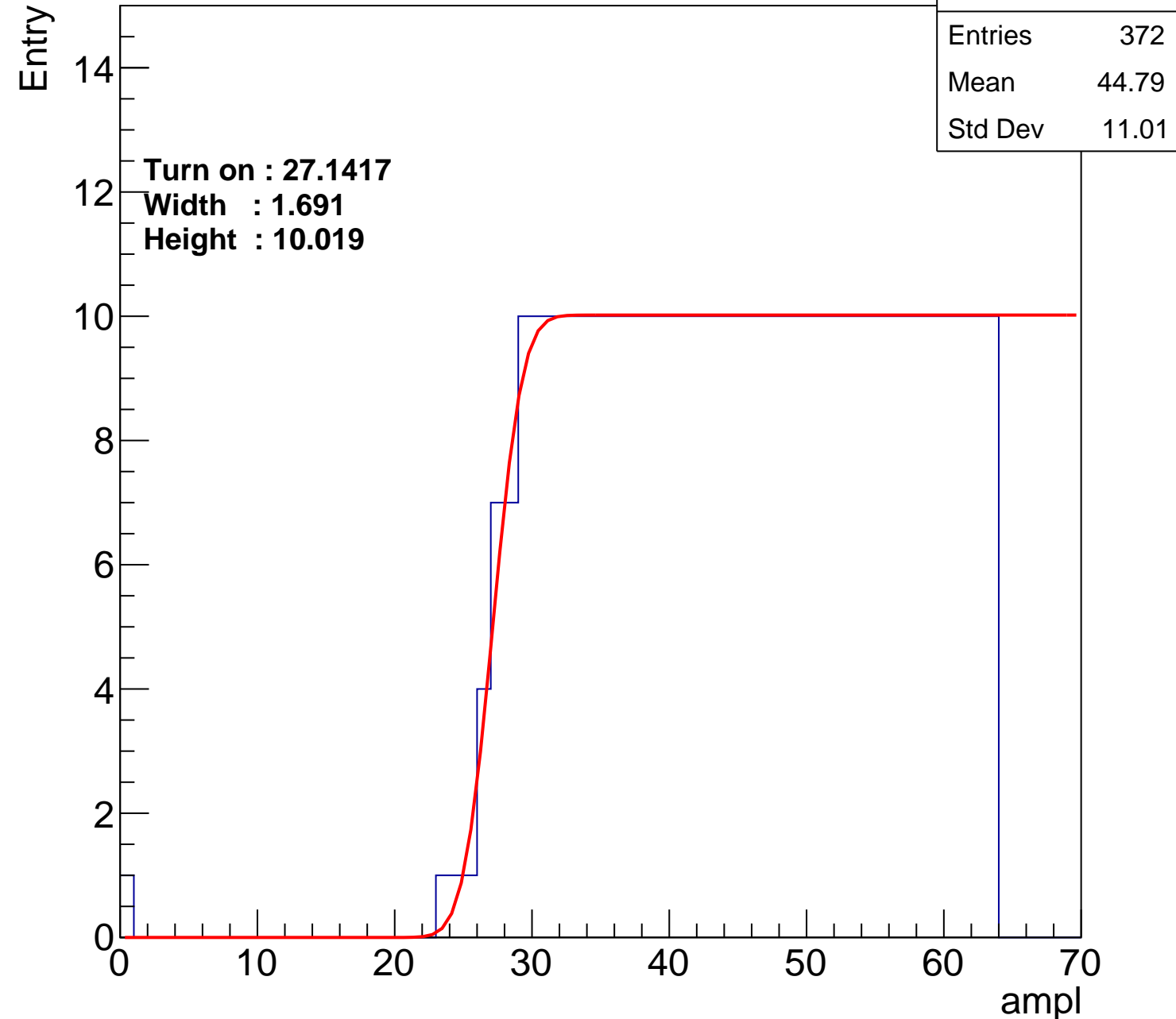
Width : 1.691

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch49

calib_packv5_042523_0143.root, FC#5, port B1

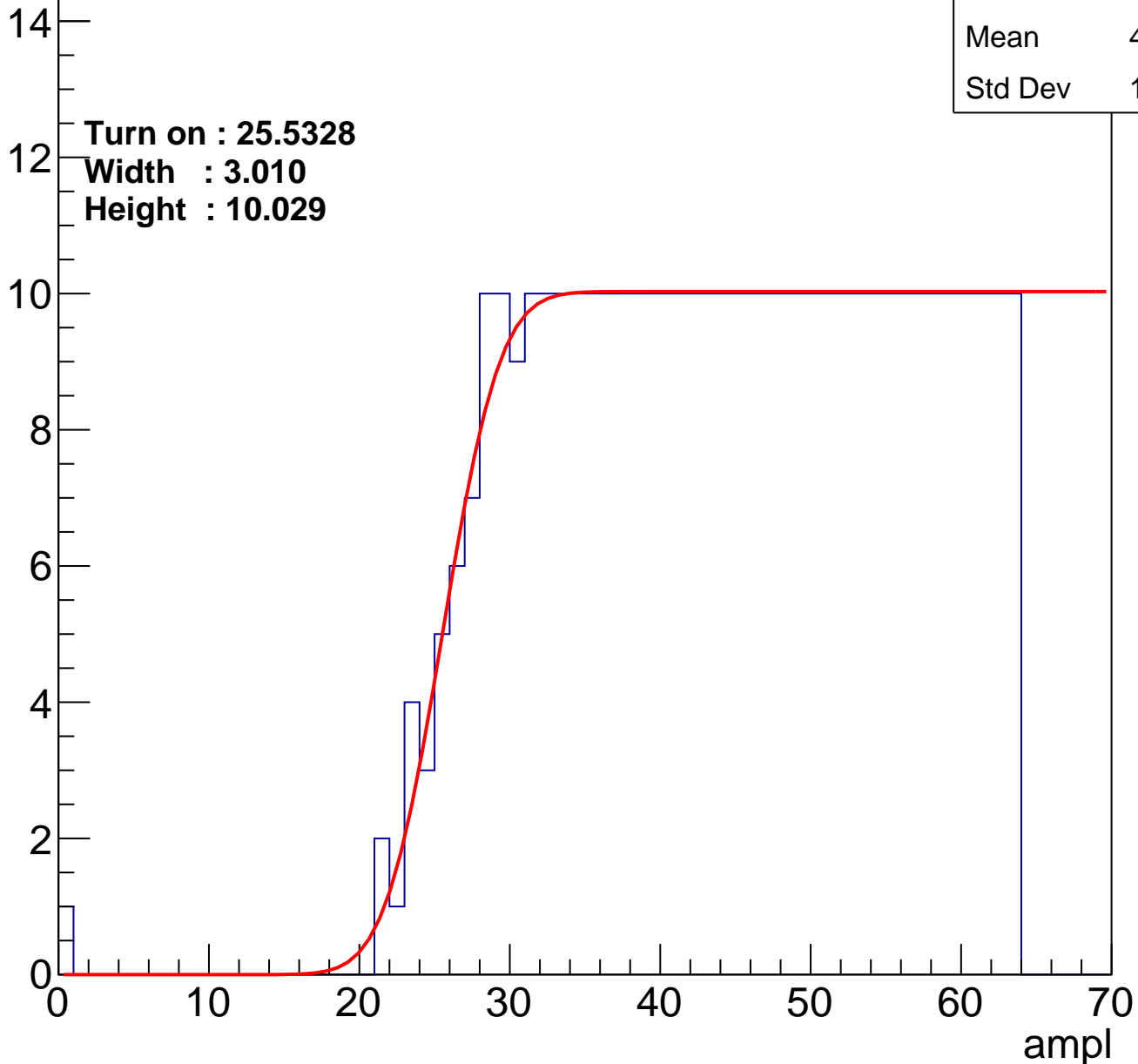
Entries	388
Mean	43.94
Std Dev	11.54

Turn on : 25.5328

Width : 3.010

Height : 10.029

Entry



B0L000S, U18-ch50

calib_packv5_042523_0143.root, FC#5, port B1

Entries	388
Mean	43.91
Std Dev	11.57

Turn on : 25.2469

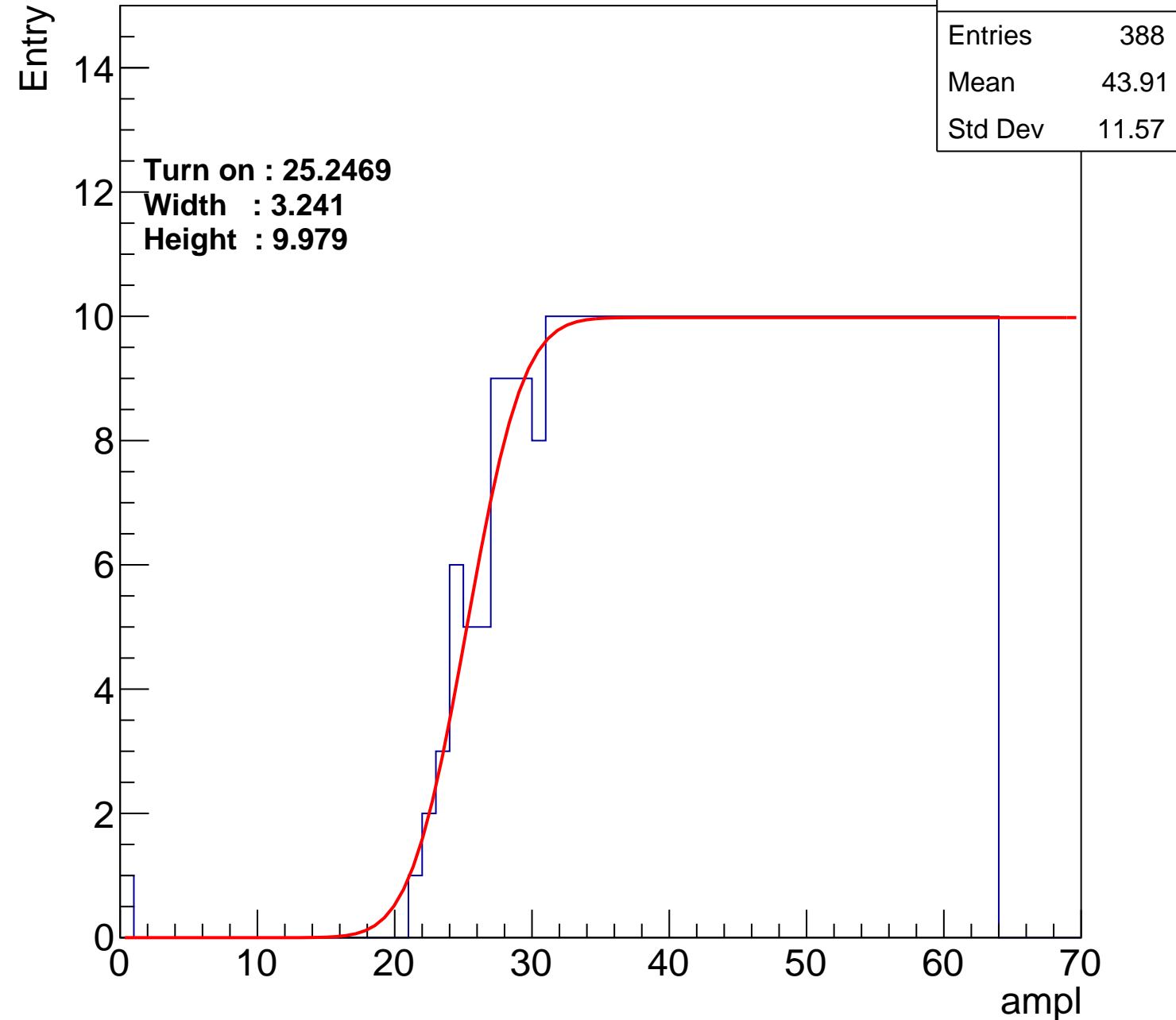
Width : 3.241

Height : 9.979

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch51

calib_packv5_042523_0143.root, FC#5, port B1

Entries	361
Mean	45.17
Std Dev	11.09

Turn on : 28.8007

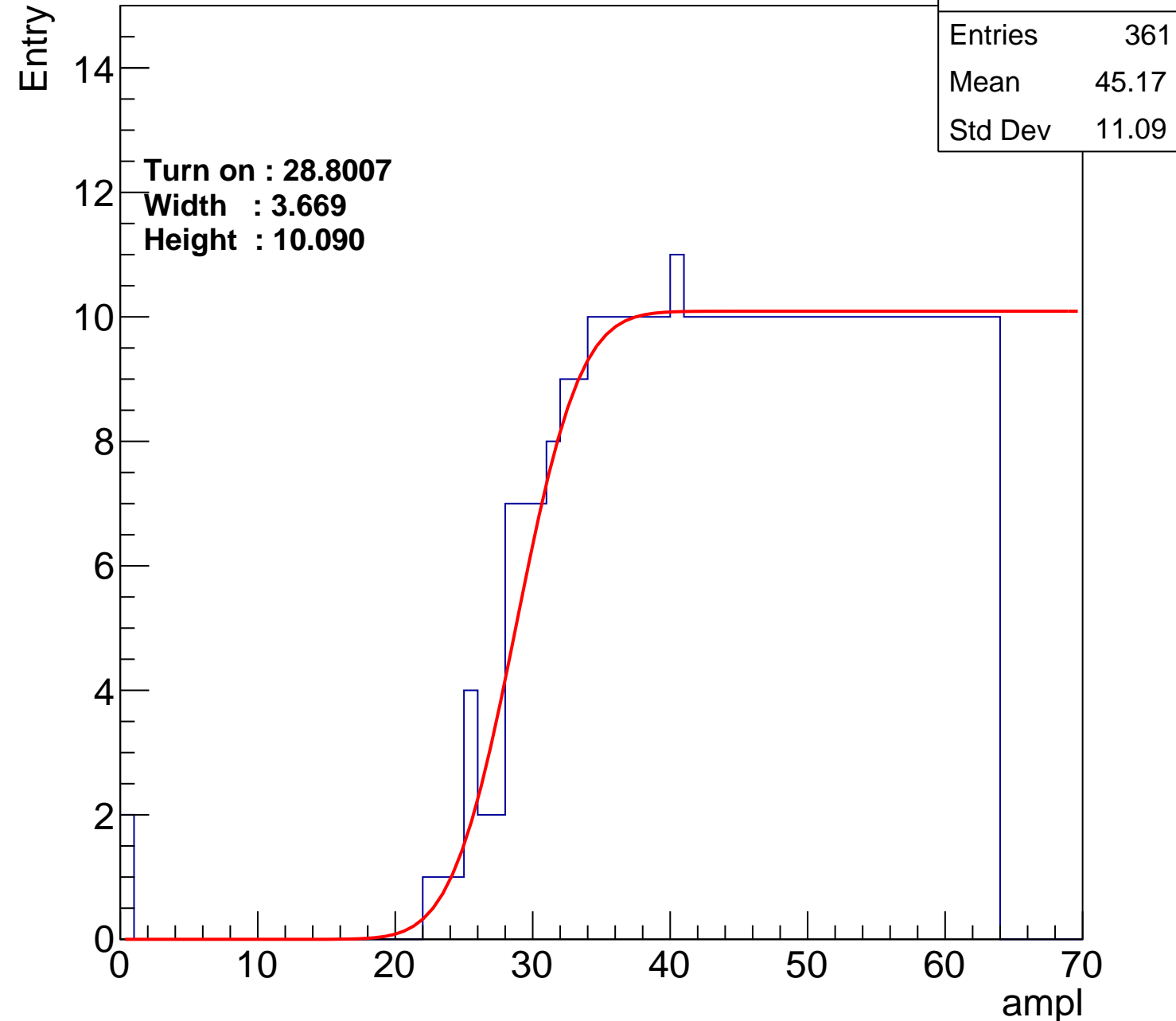
Width : 3.669

Height : 10.090

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch52

calib_packv5_042523_0143.root, FC#5, port B1

Entries	371
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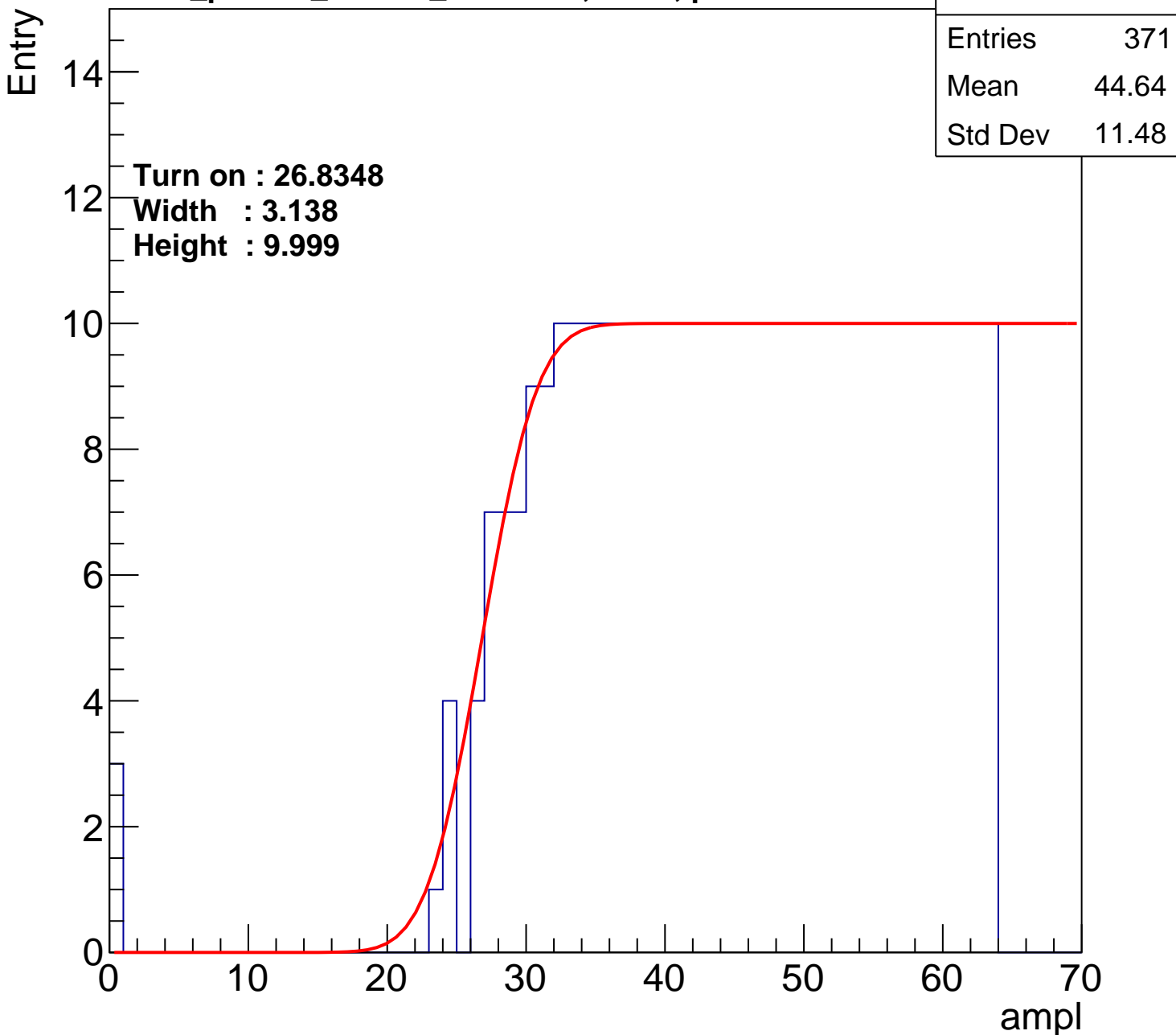
Mean	44.64
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Std Dev	11.48
---------	-------

Turn on : 26.8348

Width : 3.138

Height : 9.999



B0L000S, U18-ch53

calib_packv5_042523_0143.root, FC#5, port B1

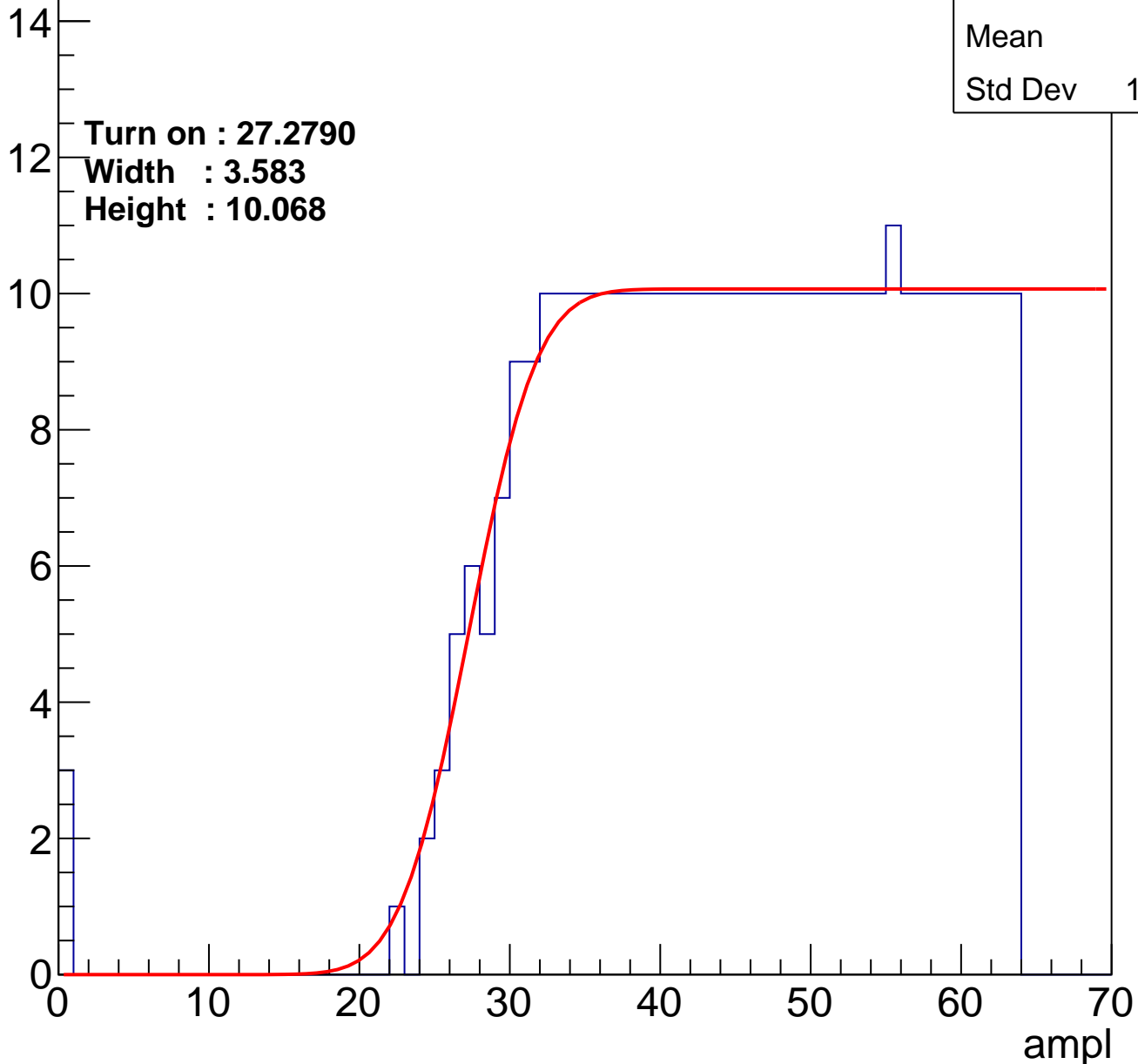
Entries	371
Mean	44.7
Std Dev	11.47

Turn on : 27.2790

Width : 3.583

Height : 10.068

Entry



B0L000S, U18-ch54

calib_packv5_042523_0143.root, FC#5, port B1

Entries	381
Mean	44.06
Std Dev	11.93

Turn on : 27.3276

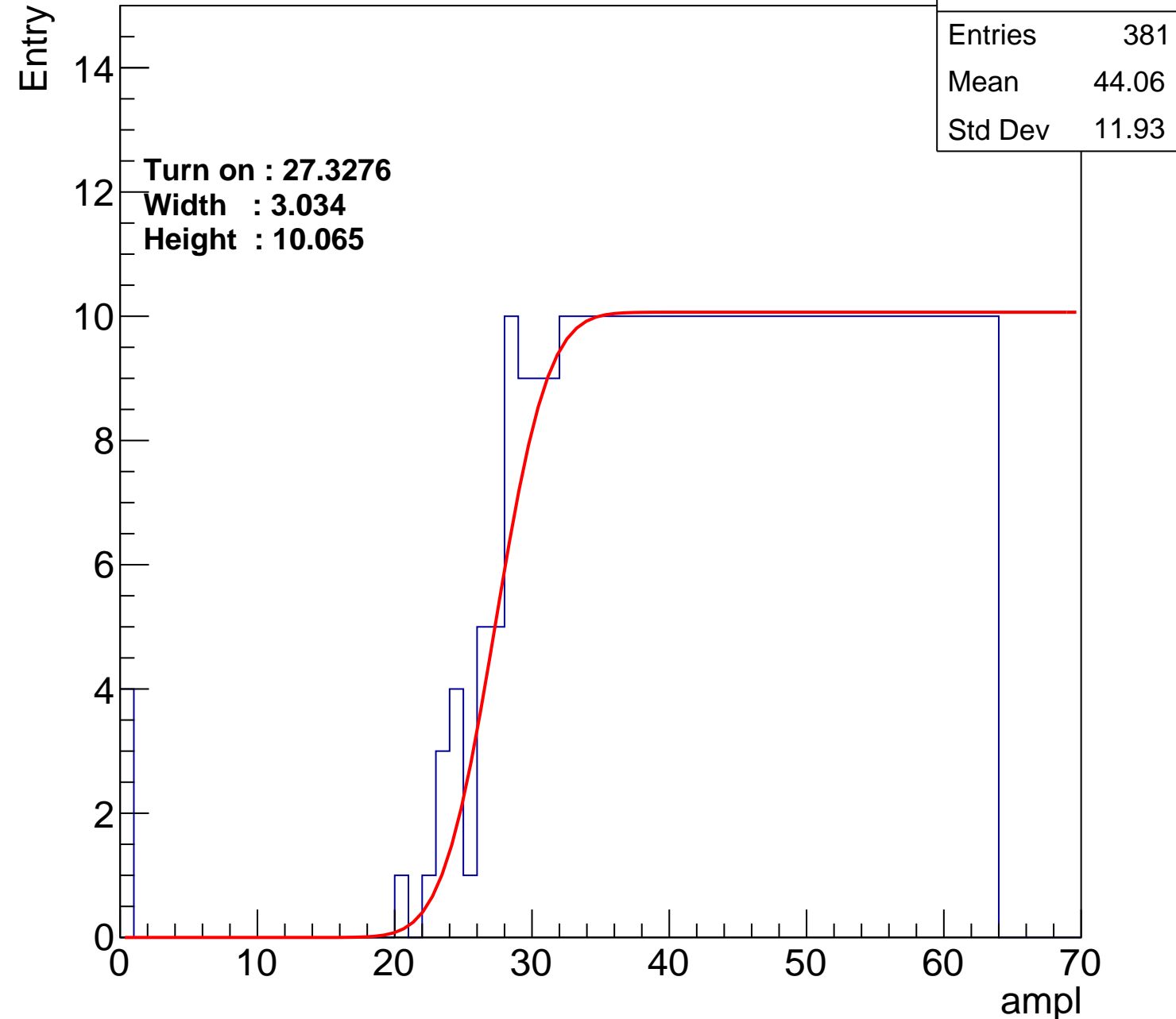
Width : 3.034

Height : 10.065

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch55

calib_packv5_042523_0143.root, FC#5, port B1

Entries	375
Mean	44.53
Std Dev	11.28

Turn on : 27.0436

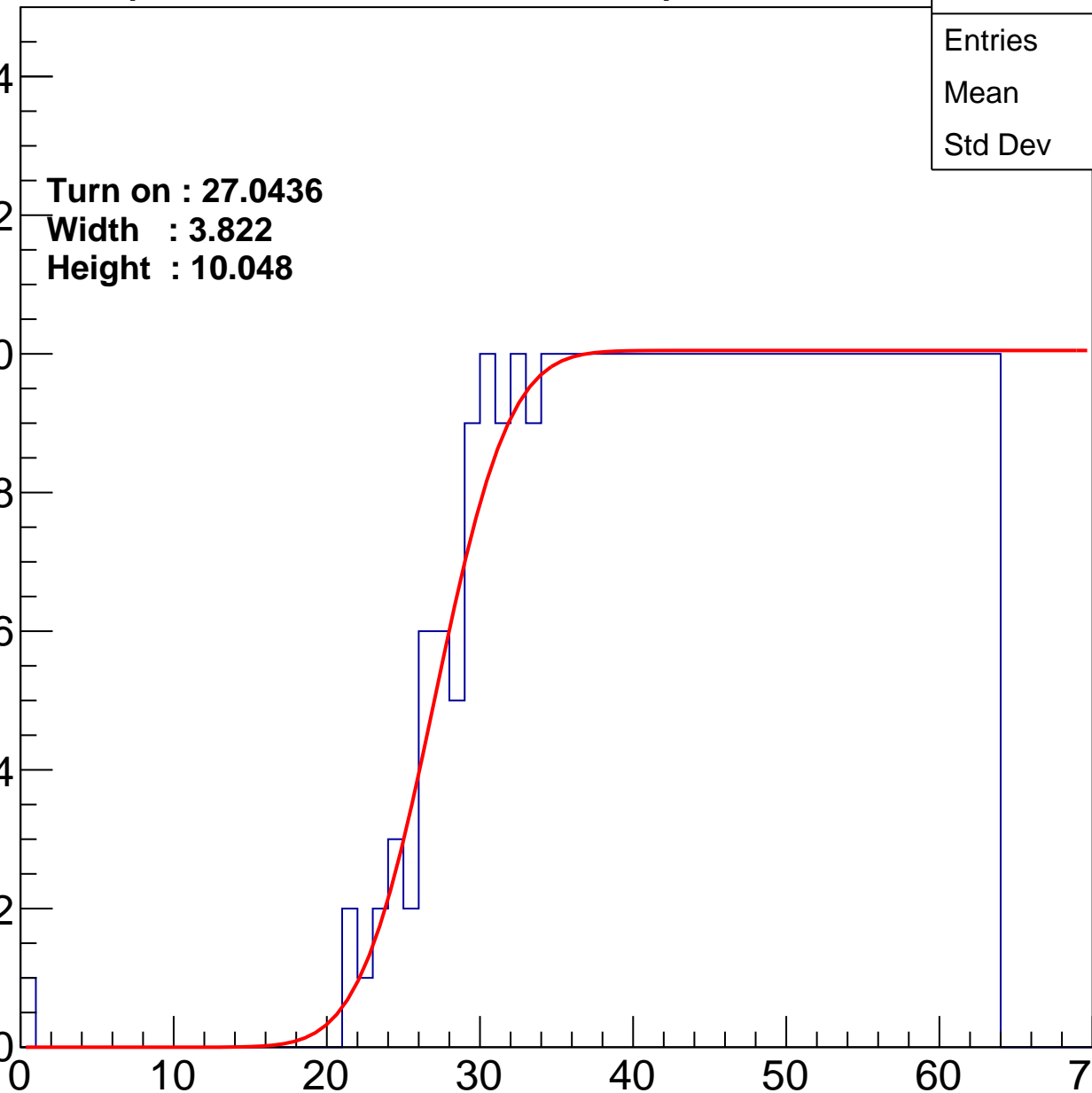
Width : 3.822

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch56

calib_packv5_042523_0143.root, FC#5, port B1

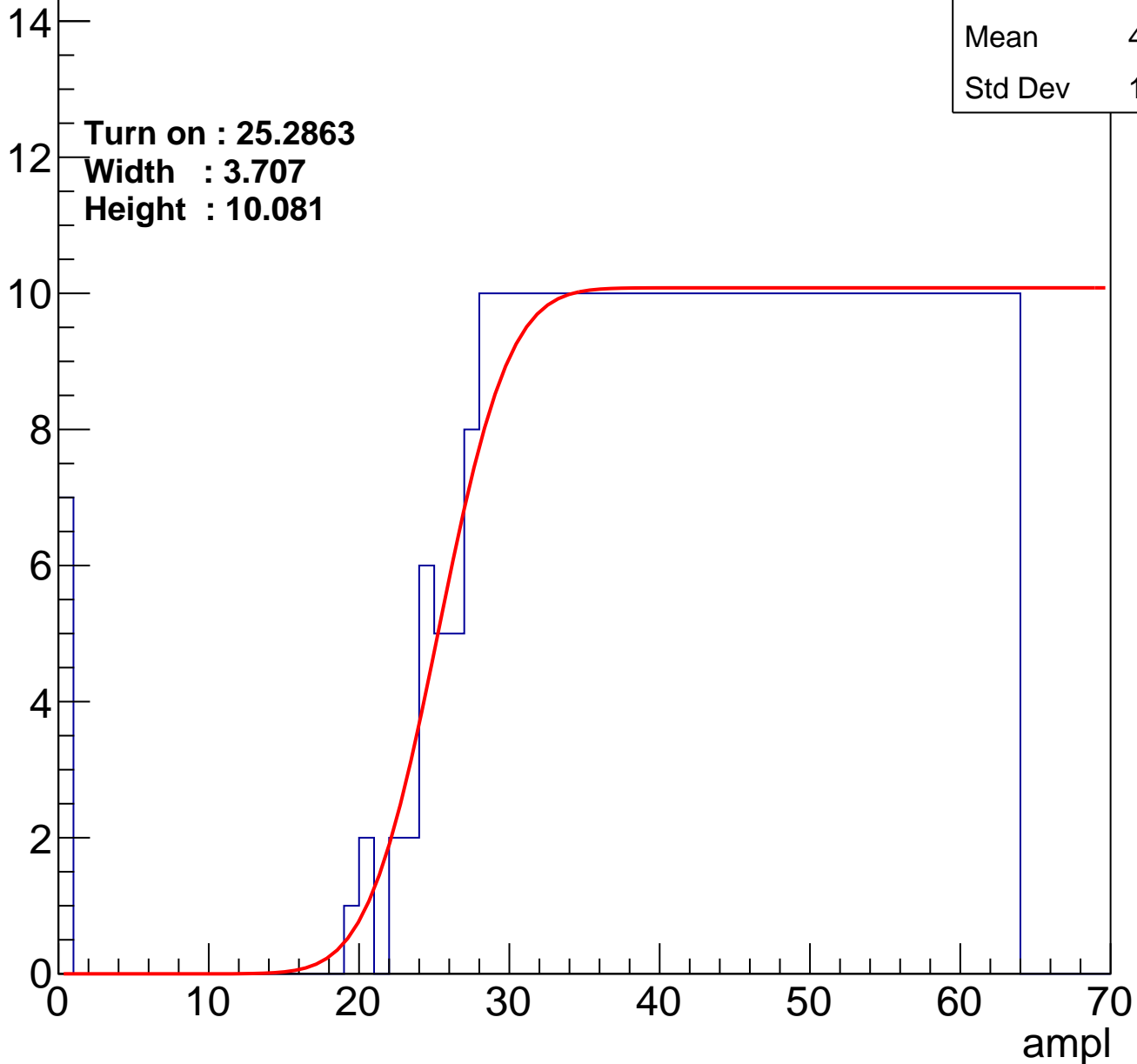
Entries	398
Mean	43.08
Std Dev	12.74

Turn on : 25.2863

Width : 3.707

Height : 10.081

Entry



B0L000S, U18-ch57

calib_packv5_042523_0143.root, FC#5, port B1

Entries	390
Mean	43.63
Std Dev	12.14

Turn on : 25.9060

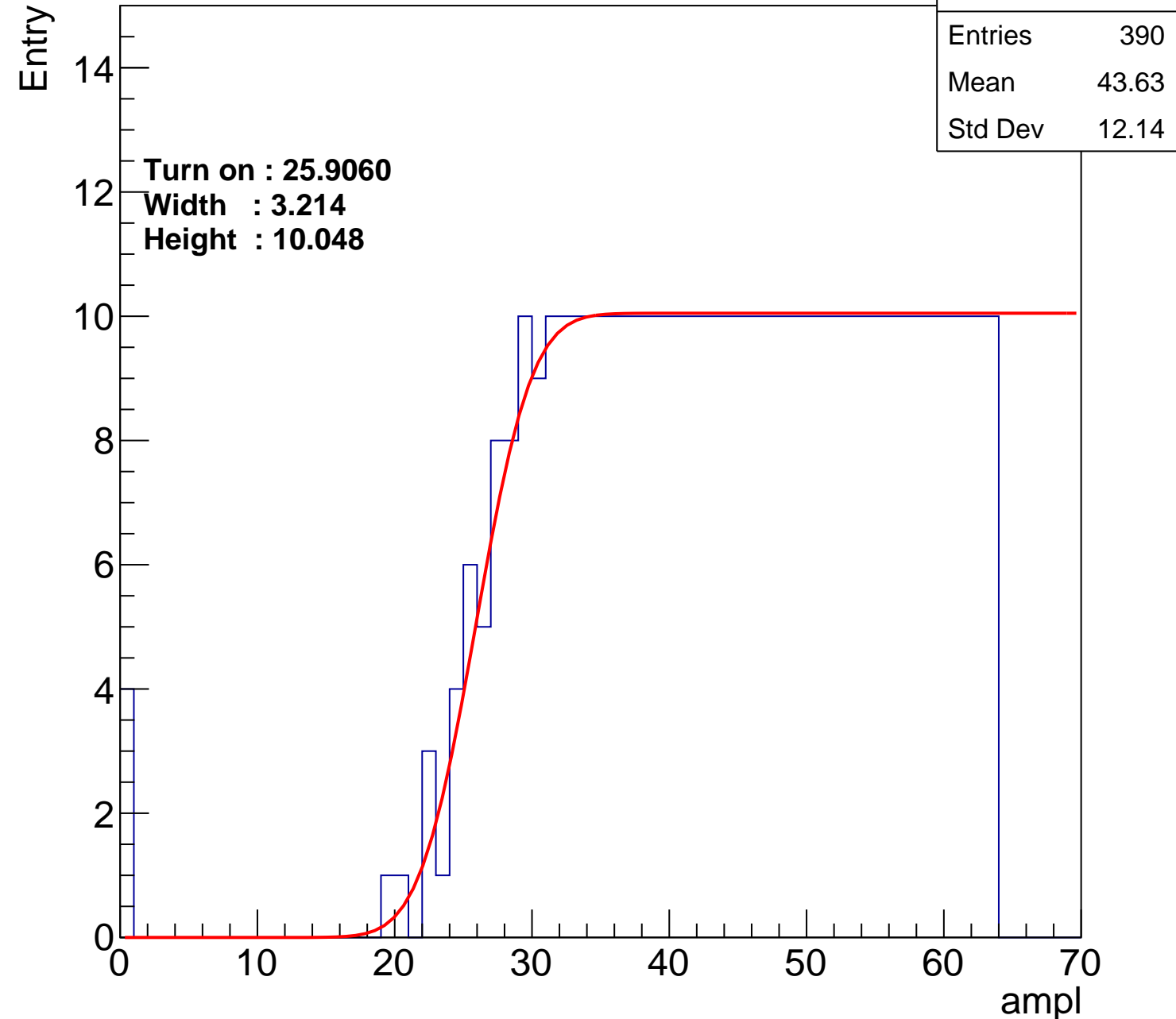
Width : 3.214

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch58

calib_packv5_042523_0143.root, FC#5, port B1

Entries	387
Mean	43.77
Std Dev	12.07

Turn on : 25.9614

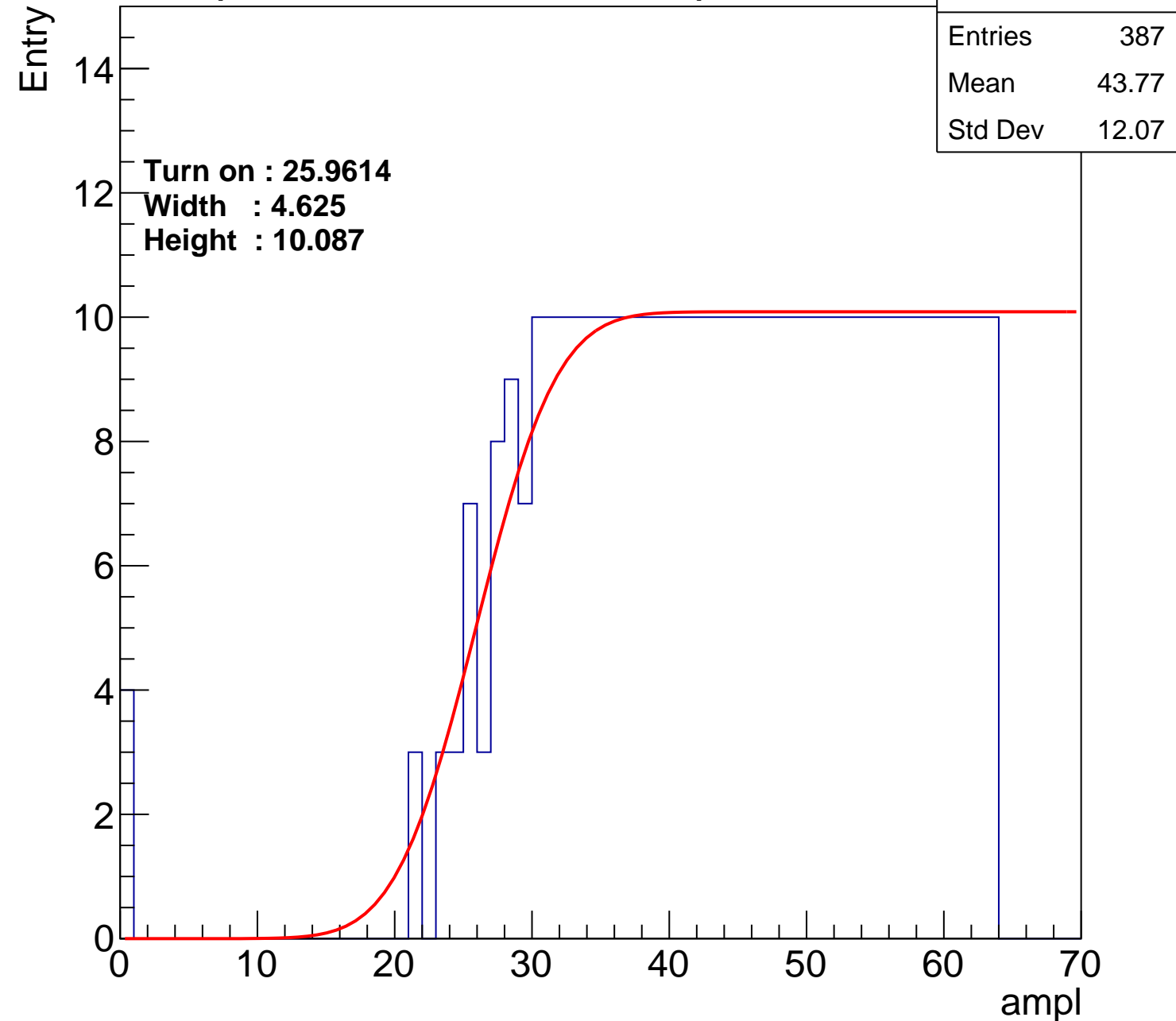
Width : 4.625

Height : 10.087

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch59

calib_packv5_042523_0143.root, FC#5, port B1

Entries	365
Mean	45.09
Std Dev	10.9

Turn on : 27.6907

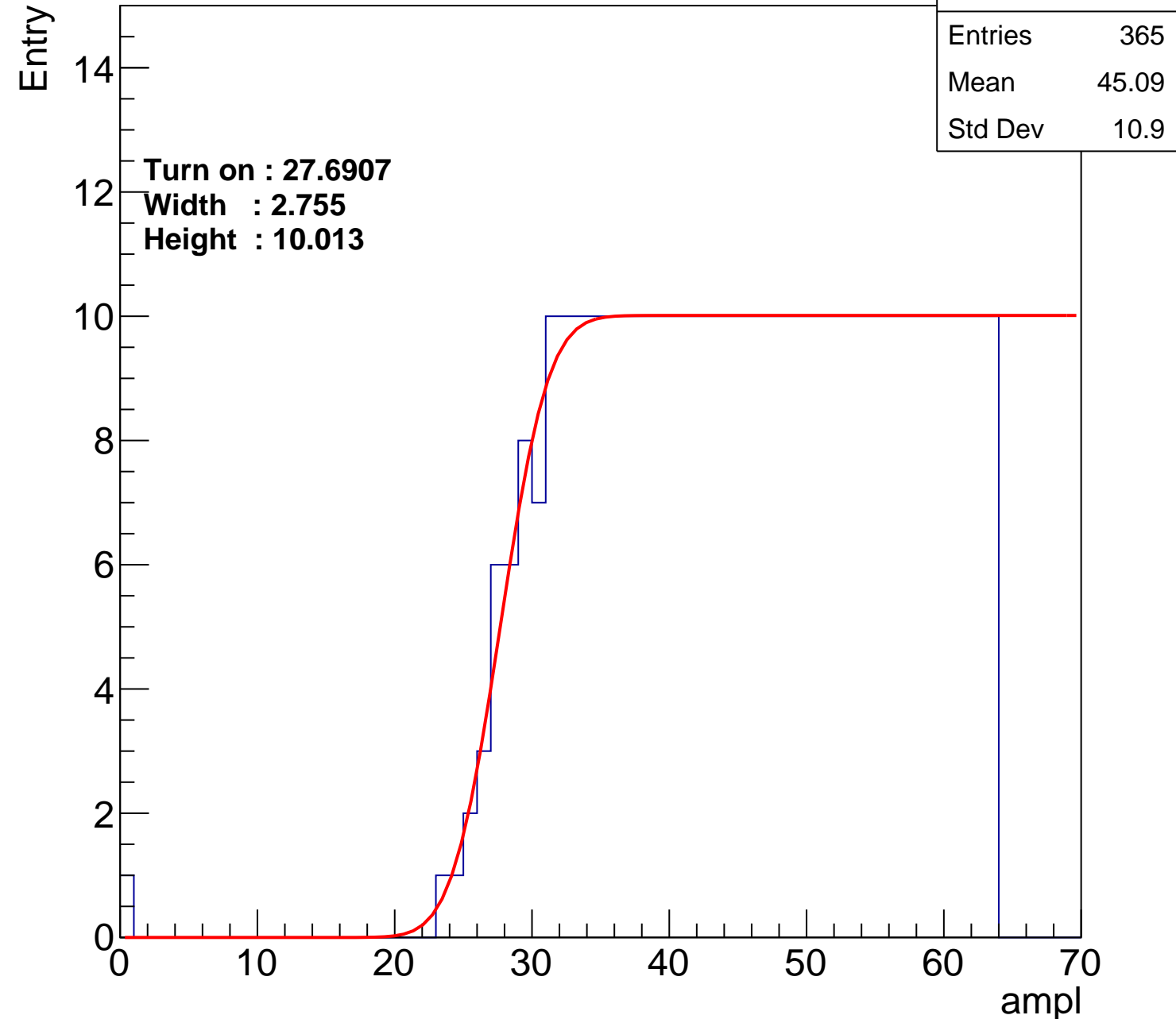
Width : 2.755

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch60

calib_packv5_042523_0143.root, FC#5, port B1

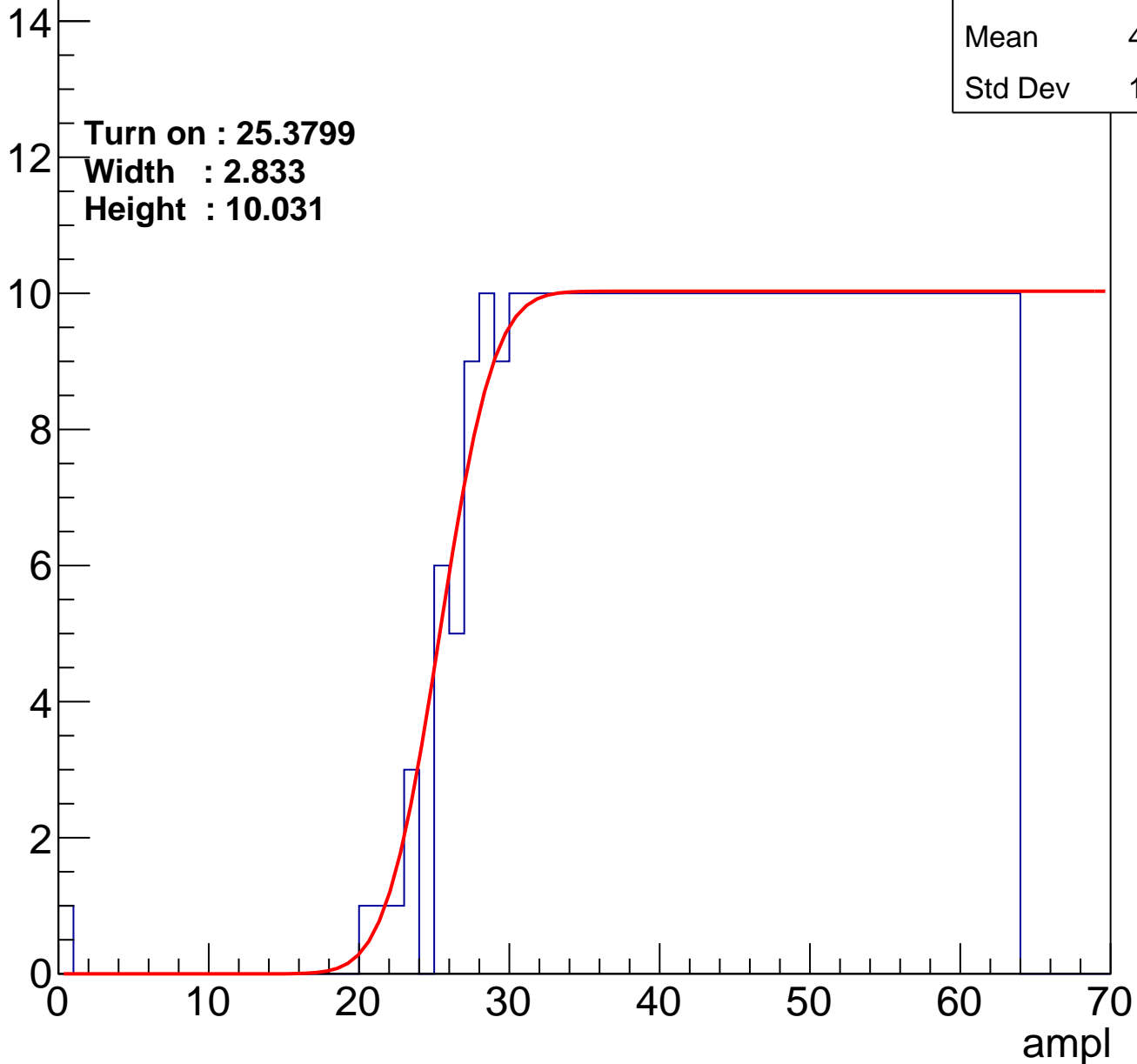
Entries	386
Mean	44.06
Std Dev	11.46

Turn on : 25.3799

Width : 2.833

Height : 10.031

Entry



B0L000S, U18-ch61

calib_packv5_042523_0143.root, FC#5, port B1

Entries	365
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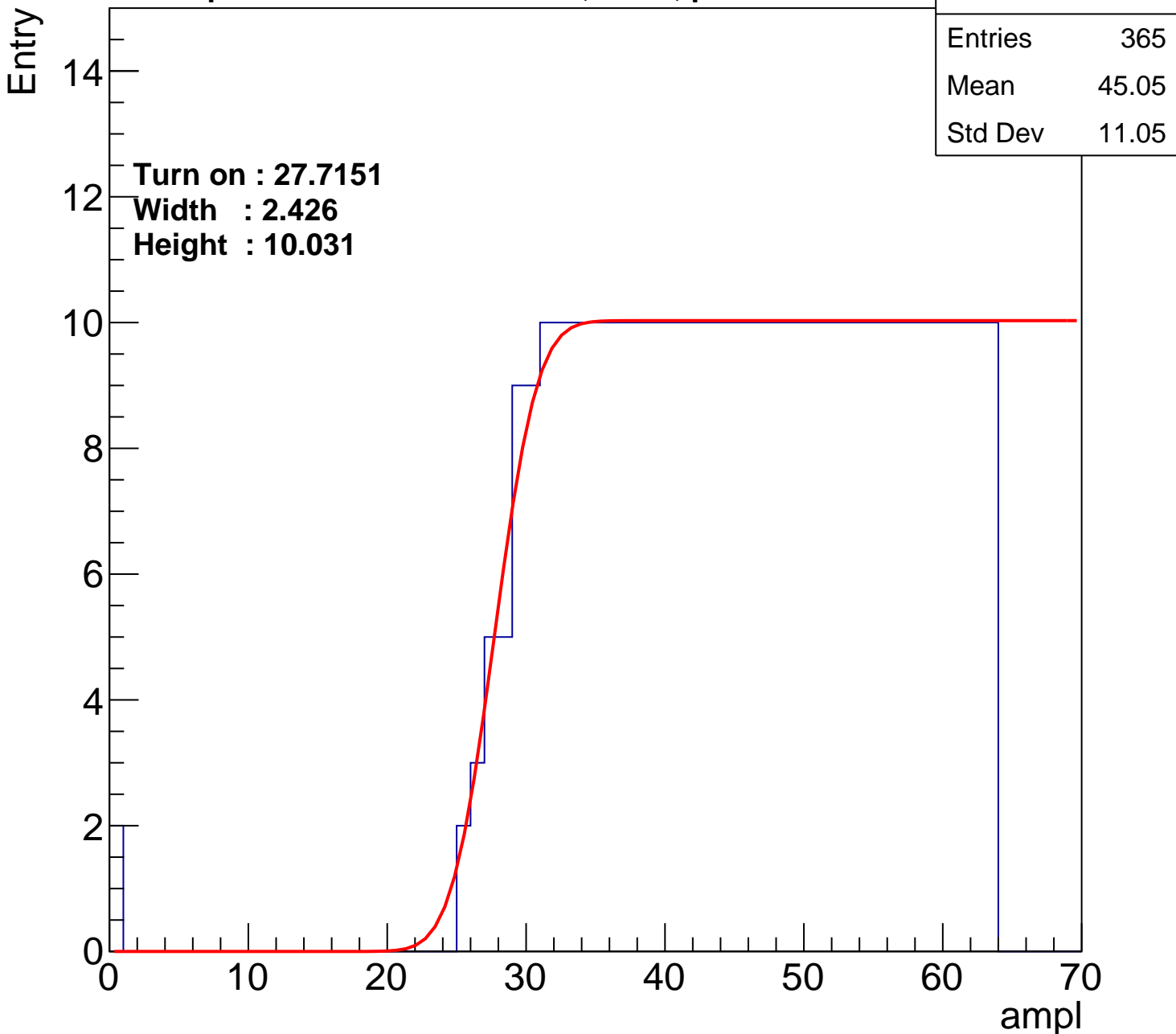
Mean	45.05
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Std Dev	11.05
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Turn on : 27.7151

Width : 2.426

Height : 10.031



B0L000S, U18-ch62

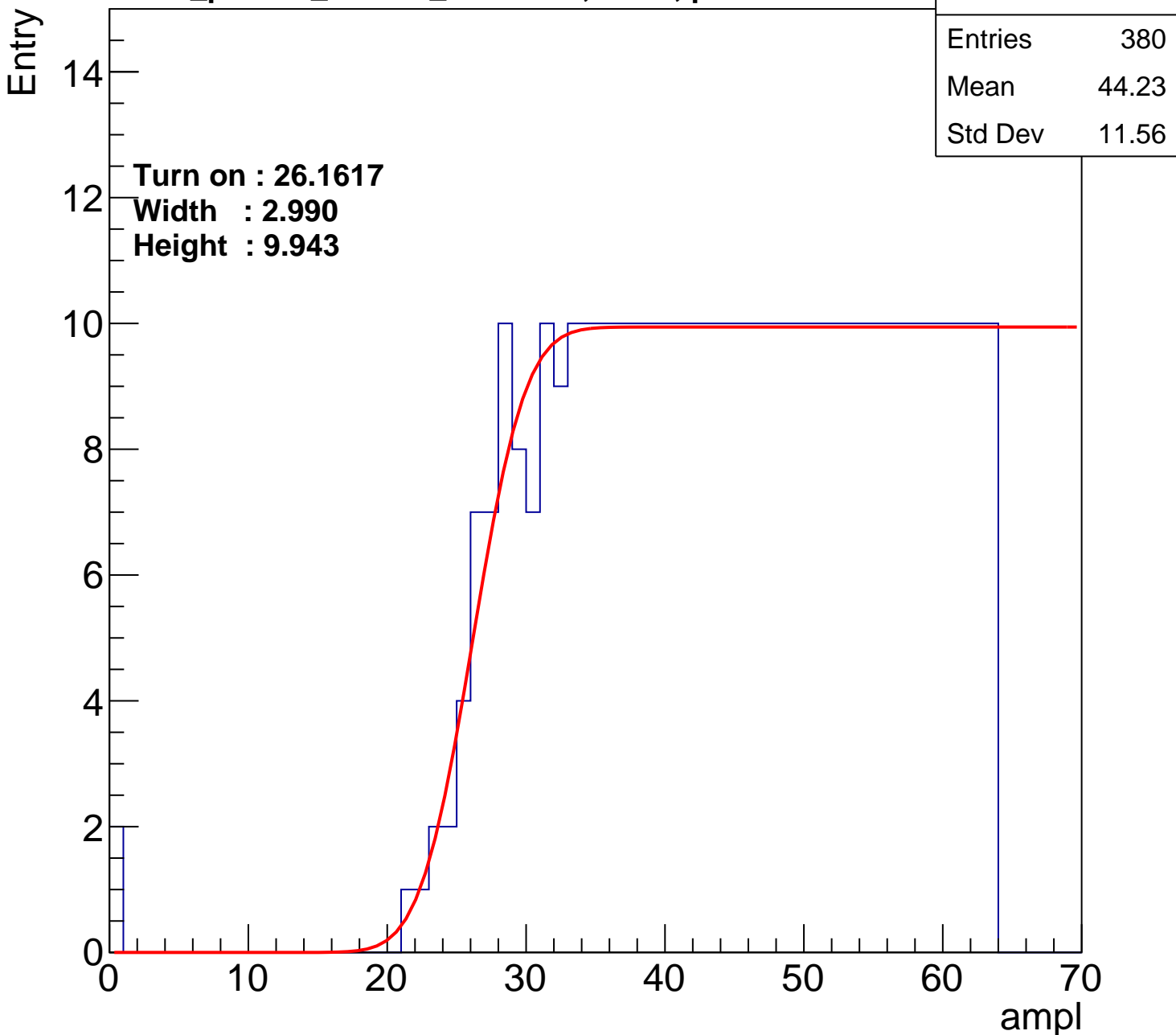
calib_packv5_042523_0143.root, FC#5, port B1

Turn on : 26.1617

Width : 2.990

Height : 9.943

Entries	380
Mean	44.23
Std Dev	11.56



B0L000S, U18-ch63

calib_packv5_042523_0143.root, FC#5, port B1

Entries	384
Mean	43.97
Std Dev	11.82

Turn on : 25.7797

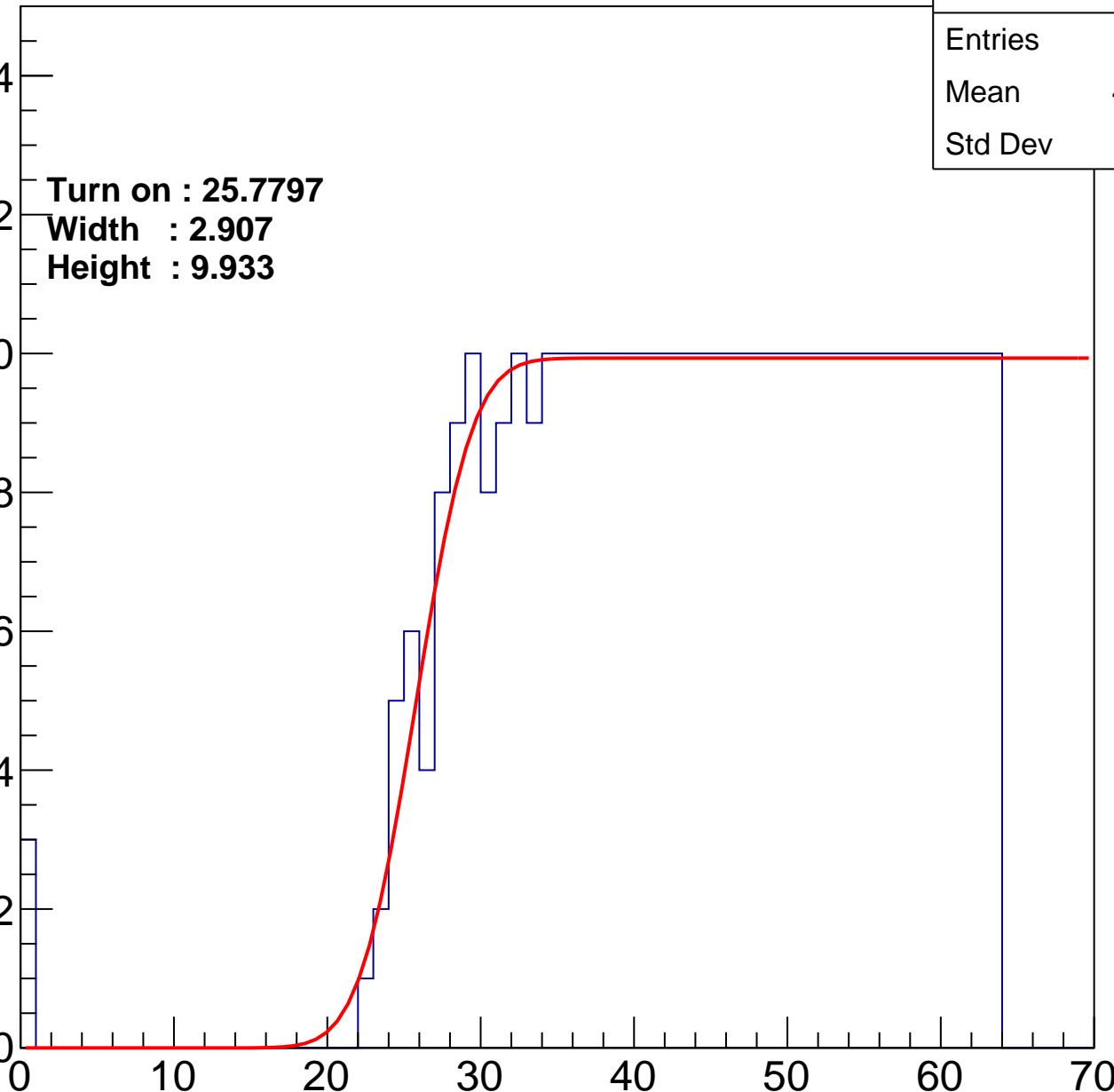
Width : 2.907

Height : 9.933

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch64

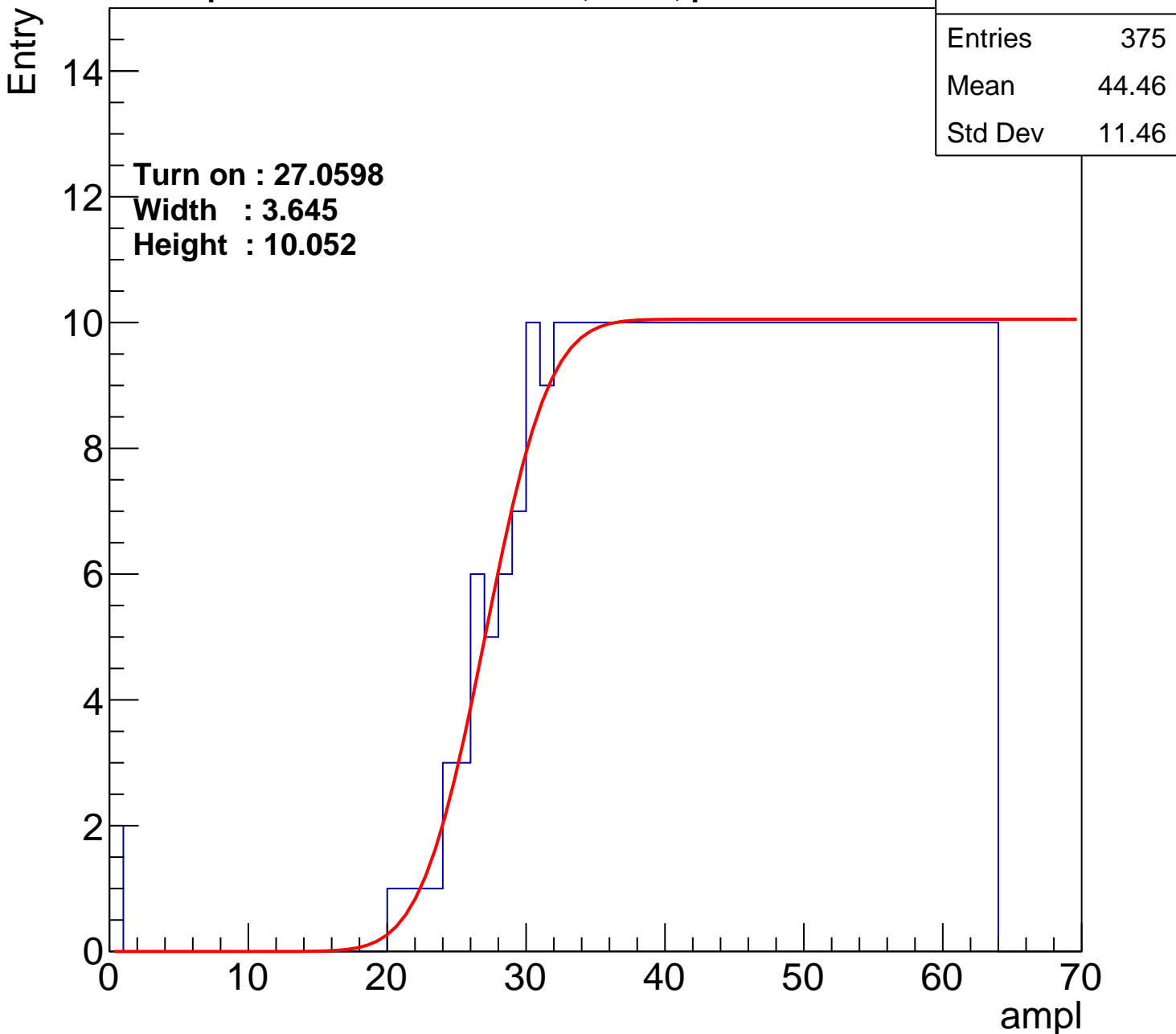
calib_packv5_042523_0143.root, FC#5, port B1

Entries	375
Mean	44.46
Std Dev	11.46

Turn on : 27.0598

Width : 3.645

Height : 10.052



B0L000S, U18-ch65

calib_packv5_042523_0143.root, FC#5, port B1

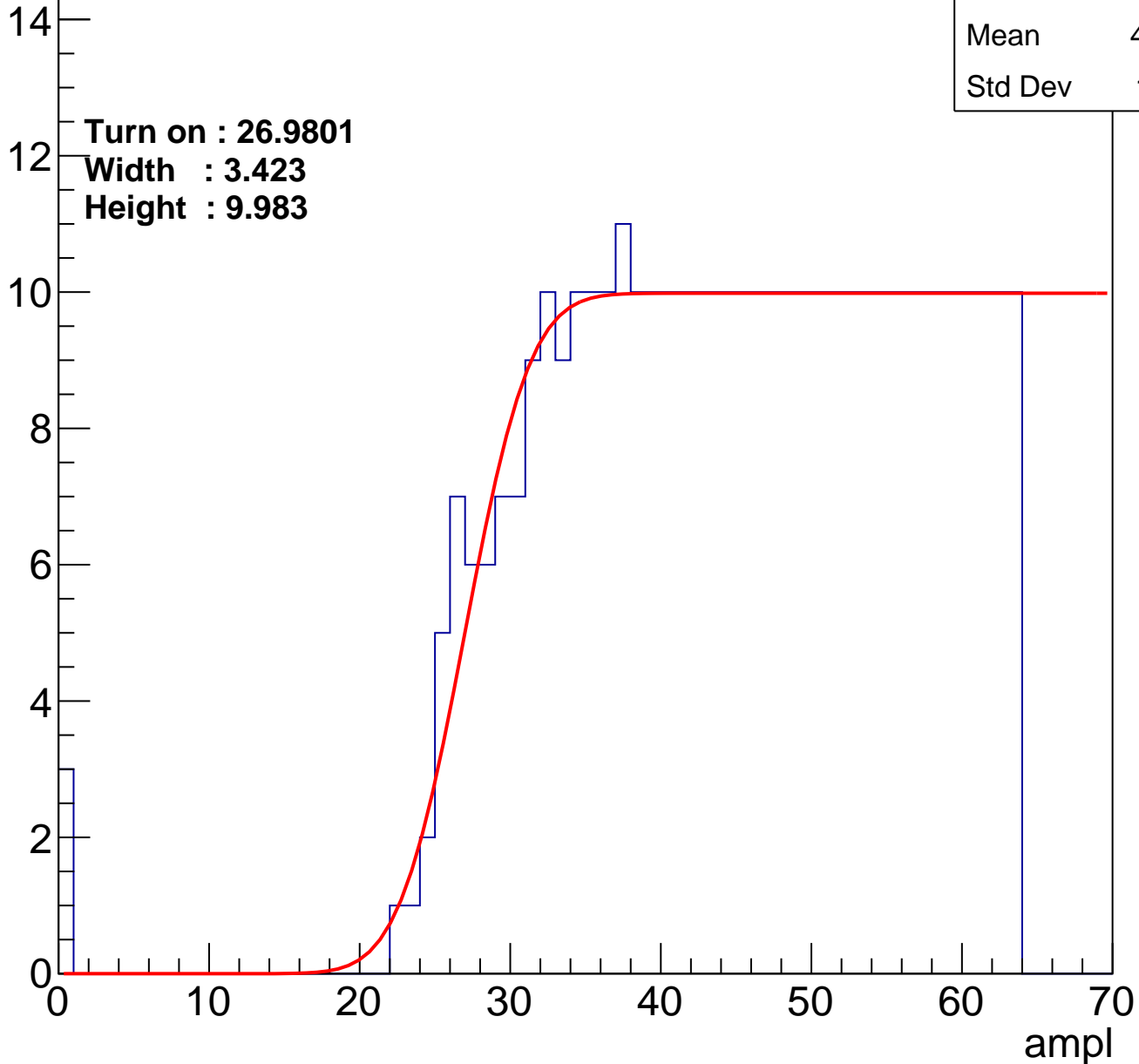
Entries	374
Mean	44.45
Std Dev	11.61

Turn on : 26.9801

Width : 3.423

Height : 9.983

Entry



B0L000S, U18-ch66

calib_packv5_042523_0143.root, FC#5, port B1

Entries	398
Mean	43.32
Std Dev	12.13

Turn on : 24.3595

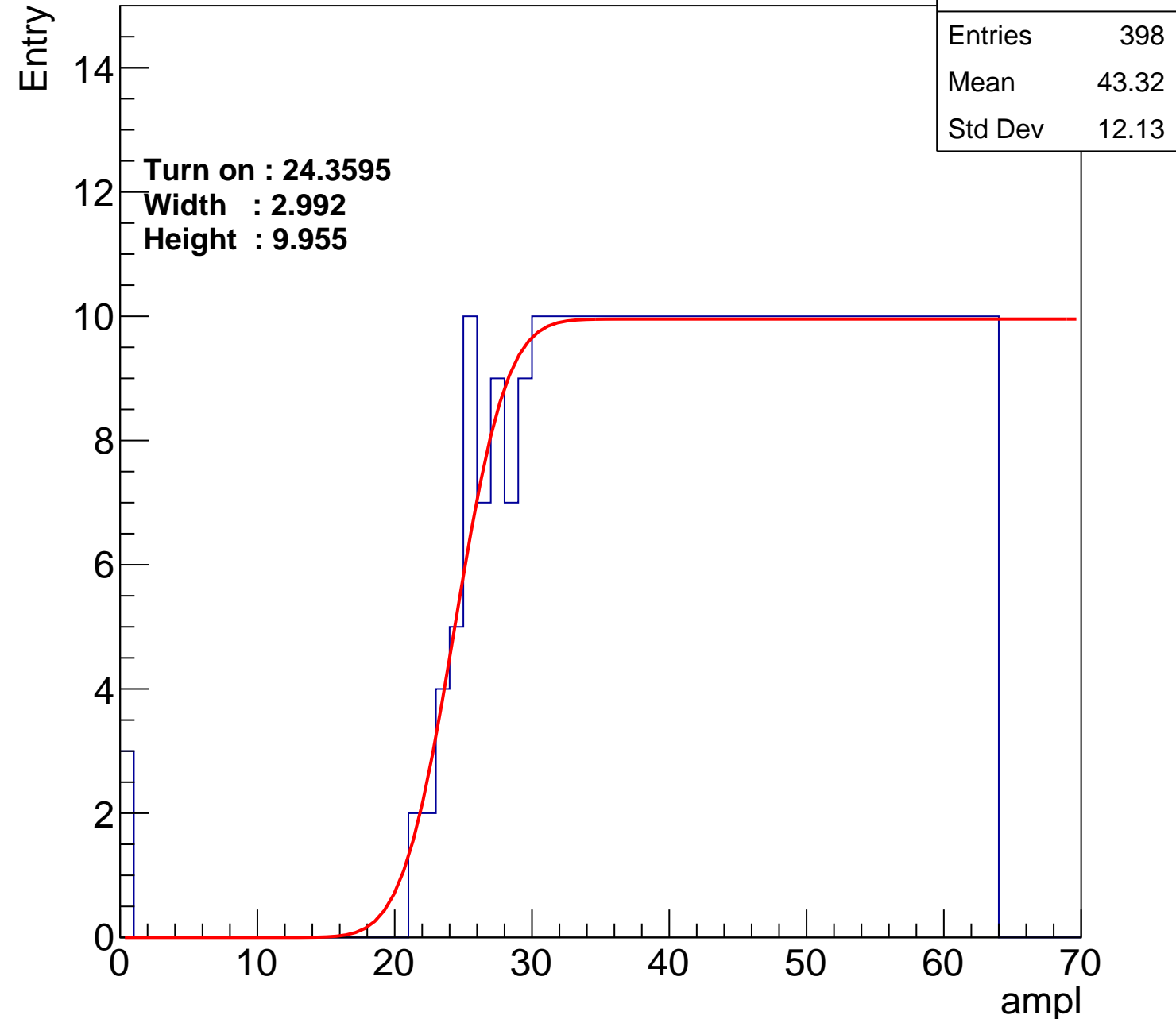
Width : 2.992

Height : 9.955

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch67

calib_packv5_042523_0143.root, FC#5, port B1

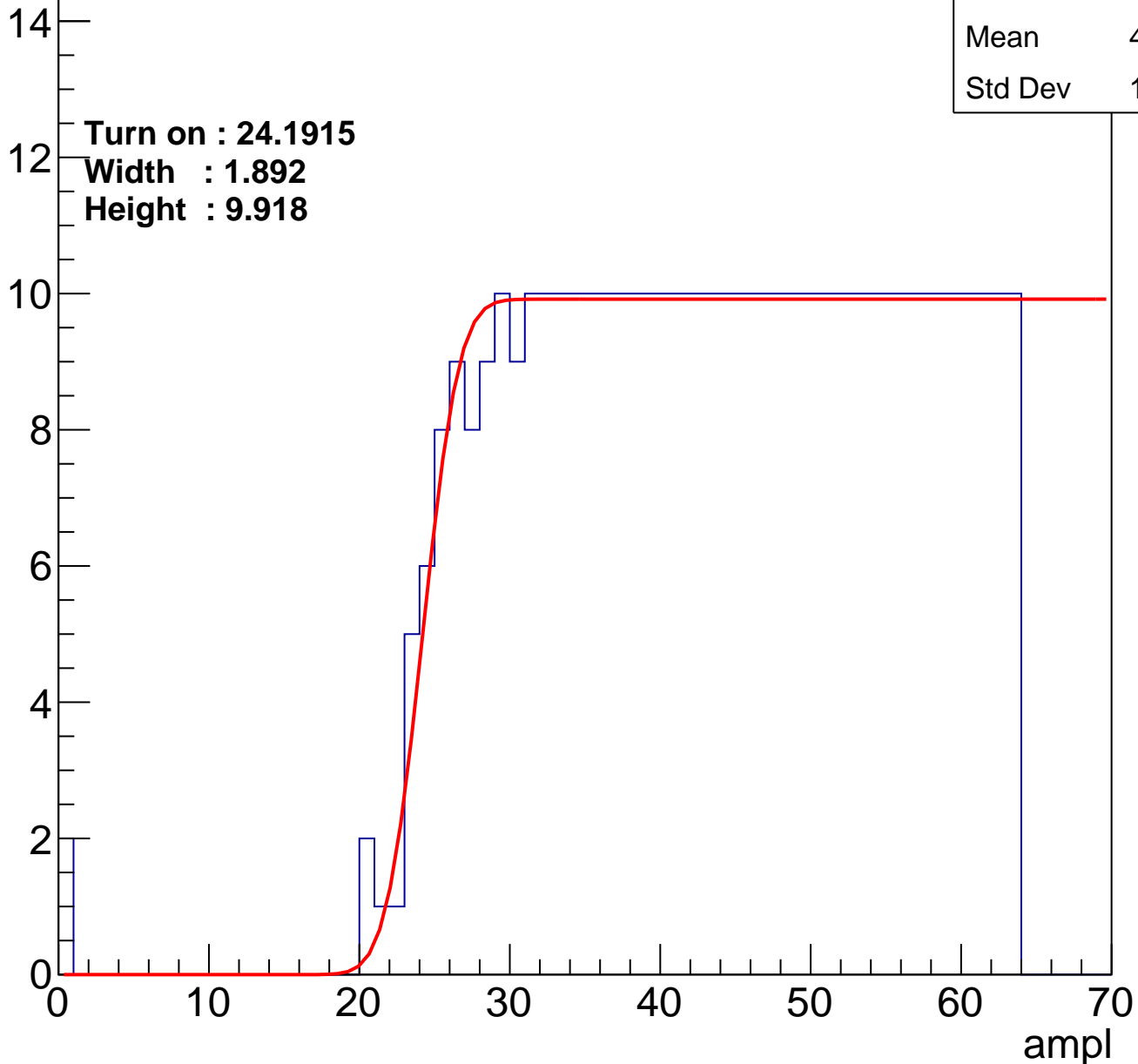
Entries	400
Mean	43.28
Std Dev	12.02

Turn on : 24.1915

Width : 1.892

Height : 9.918

Entry



B0L000S, U18-ch68

calib_packv5_042523_0143.root, FC#5, port B1

Entries	373
Mean	44.48
Std Dev	11.7

Turn on : 27.7403

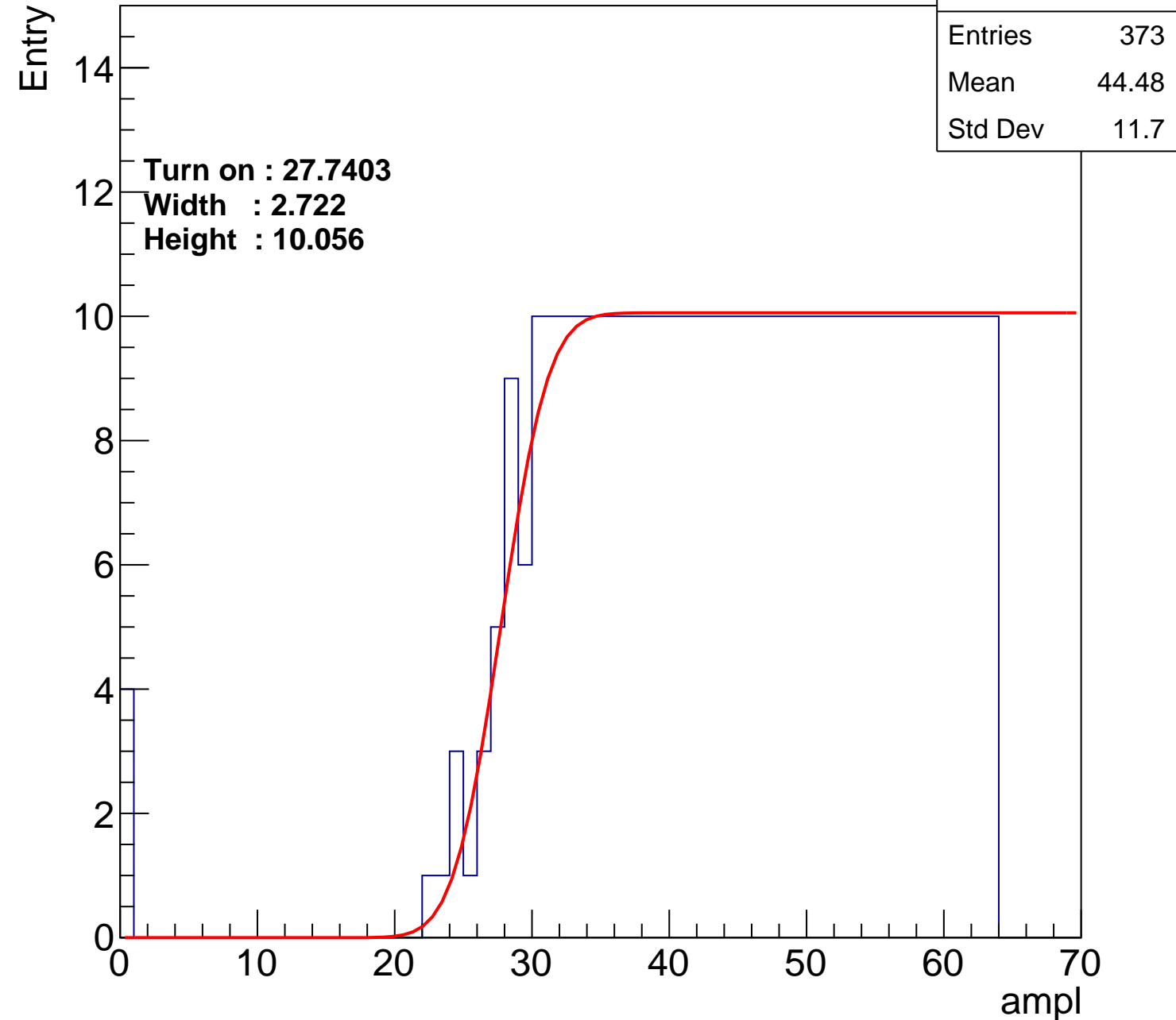
Width : 2.722

Height : 10.056

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch69

calib_packv5_042523_0143.root, FC#5, port B1

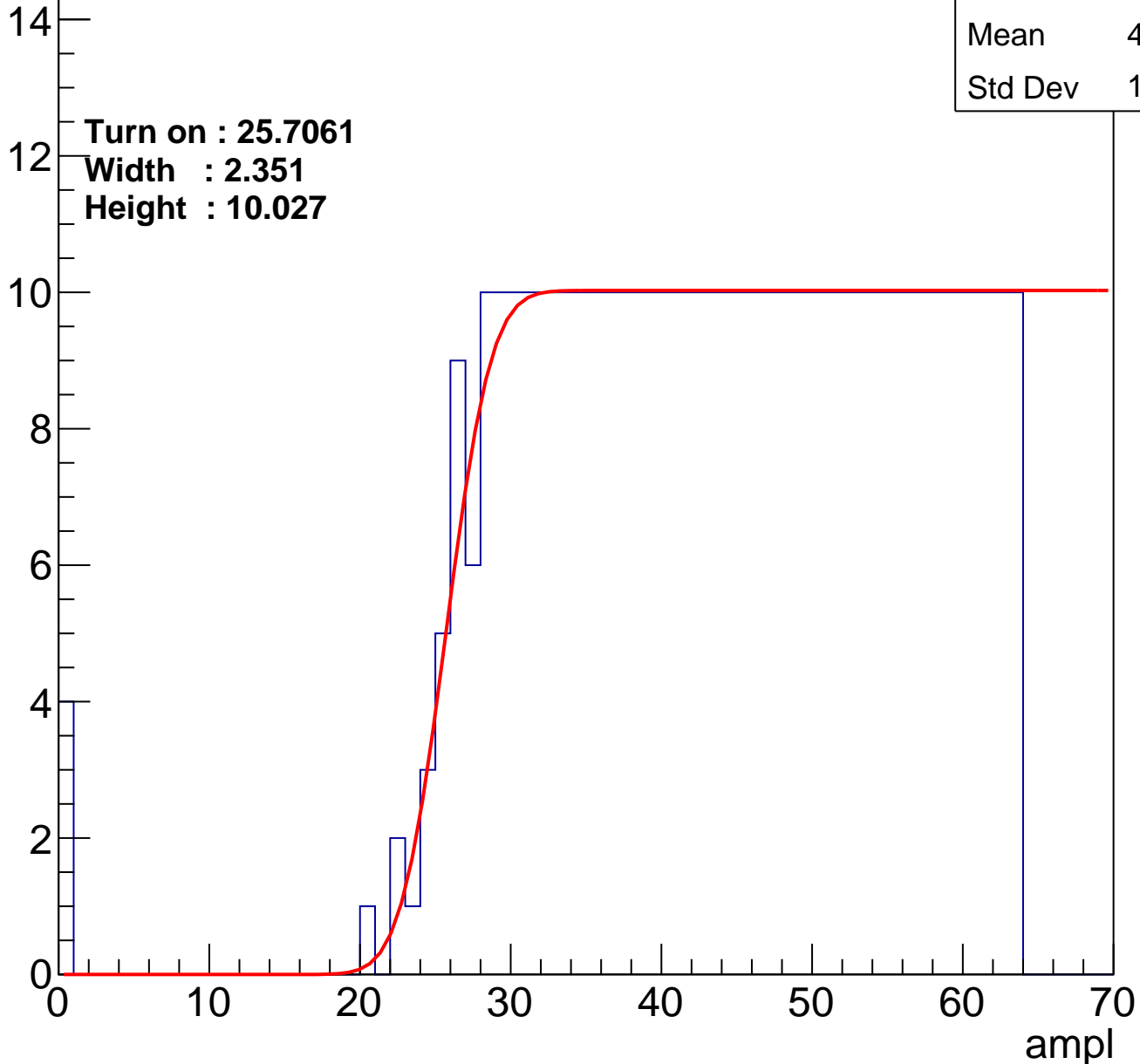
Entries	391
Mean	43.63
Std Dev	12.07

Turn on : 25.7061

Width : 2.351

Height : 10.027

Entry



B0L000S, U18-ch70

calib_packv5_042523_0143.root, FC#5, port B1

Entries	375
Mean	44.6
Std Dev	11.16

Turn on : 27.1568

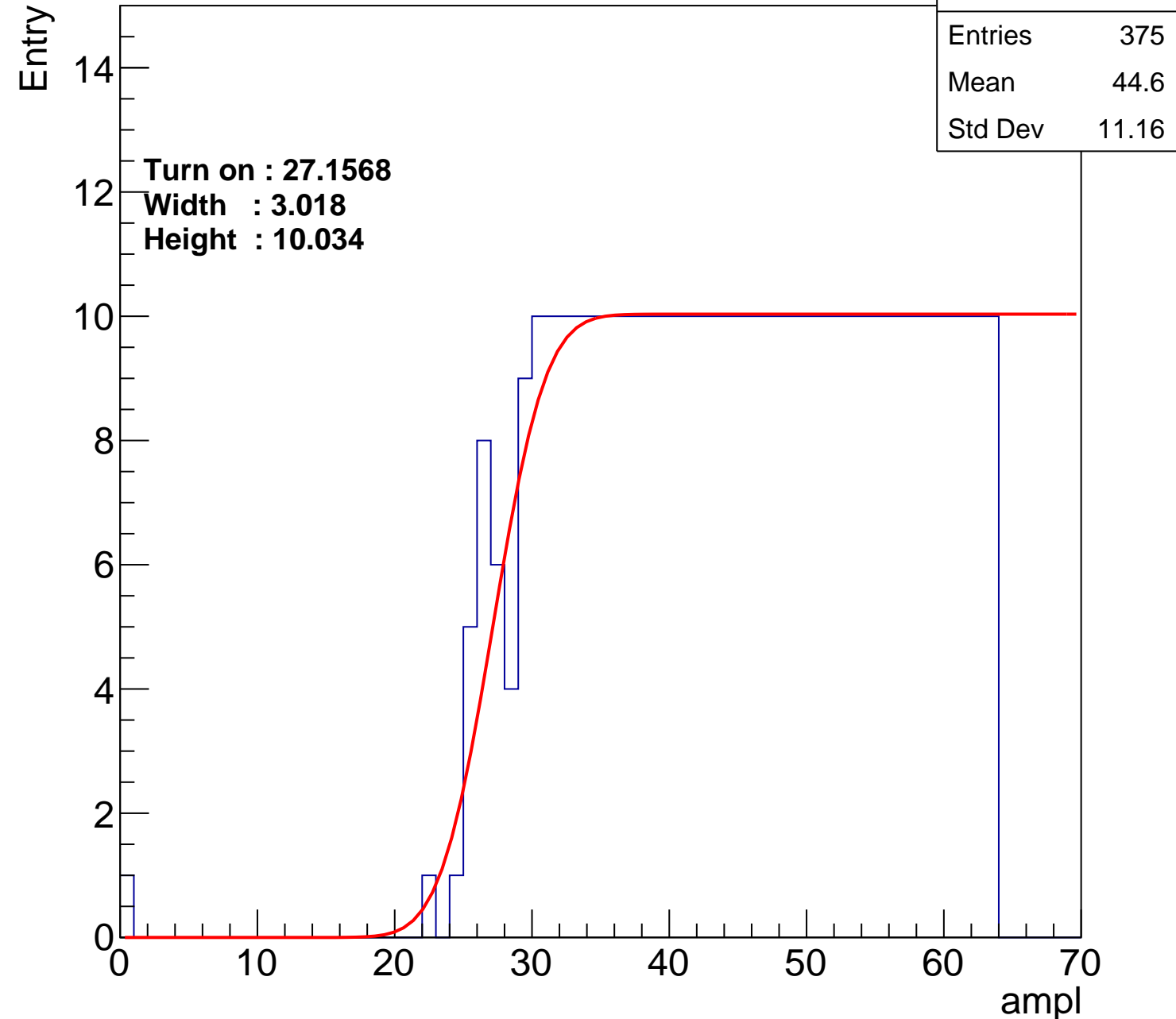
Width : 3.018

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch71

calib_packv5_042523_0143.root, FC#5, port B1

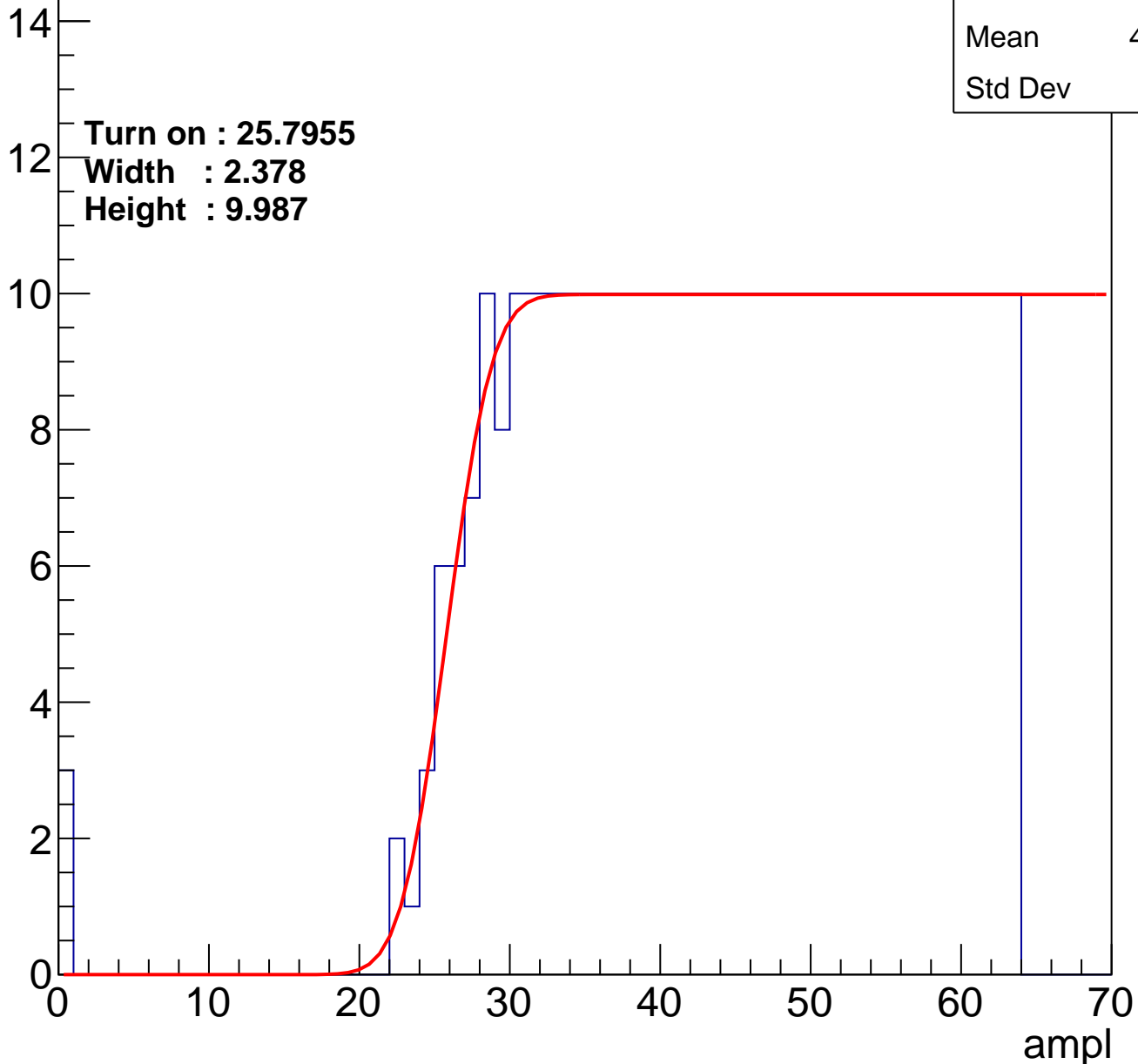
Entries	386
Mean	43.93
Std Dev	11.8

Turn on : 25.7955

Width : 2.378

Height : 9.987

Entry



B0L000S, U18-ch72

calib_packv5_042523_0143.root, FC#5, port B1

Entries	374
Mean	44.39
Std Dev	11.79

Turn on : 27.1006

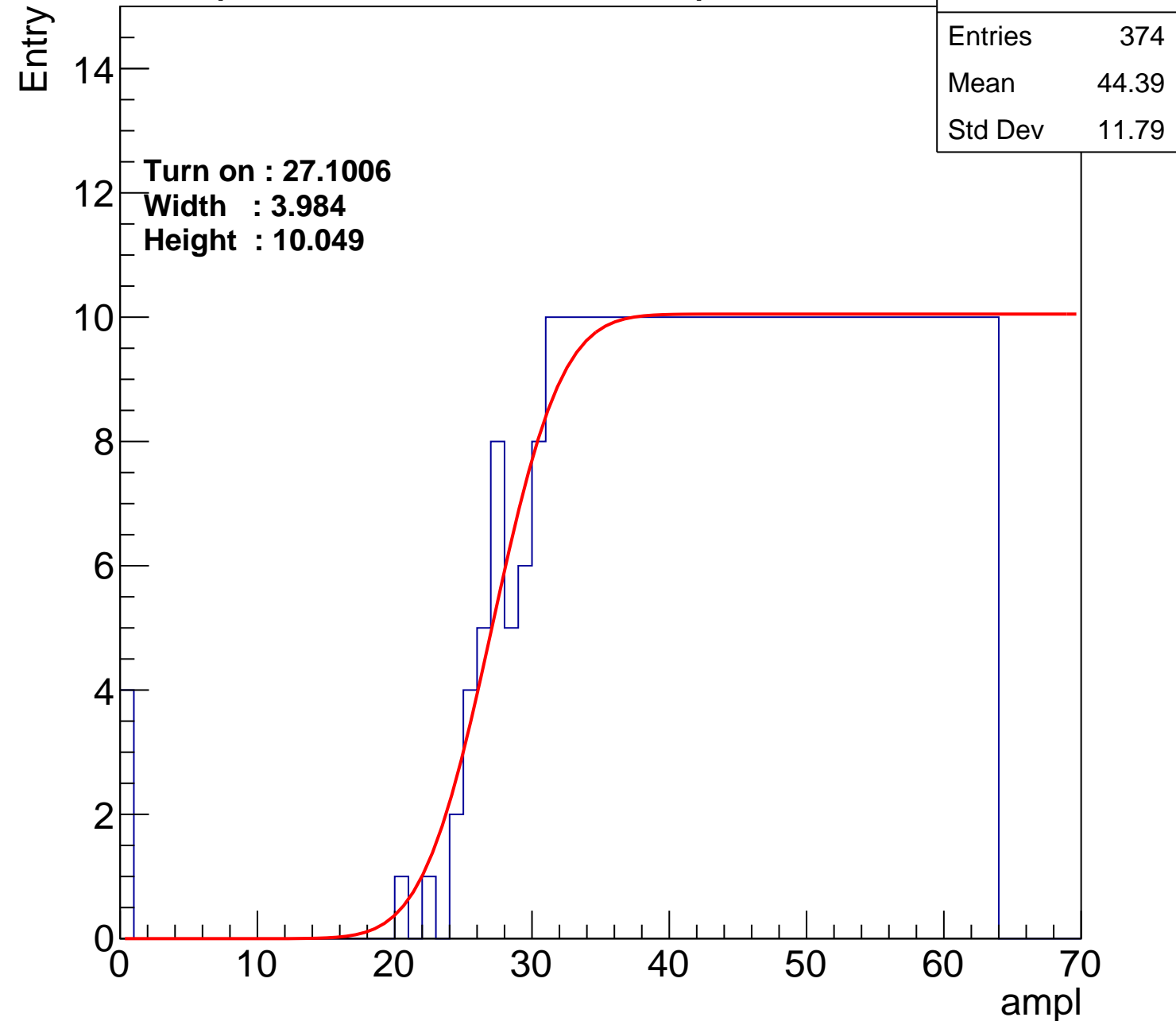
Width : 3.984

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch73

calib_packv5_042523_0143.root, FC#5, port B1

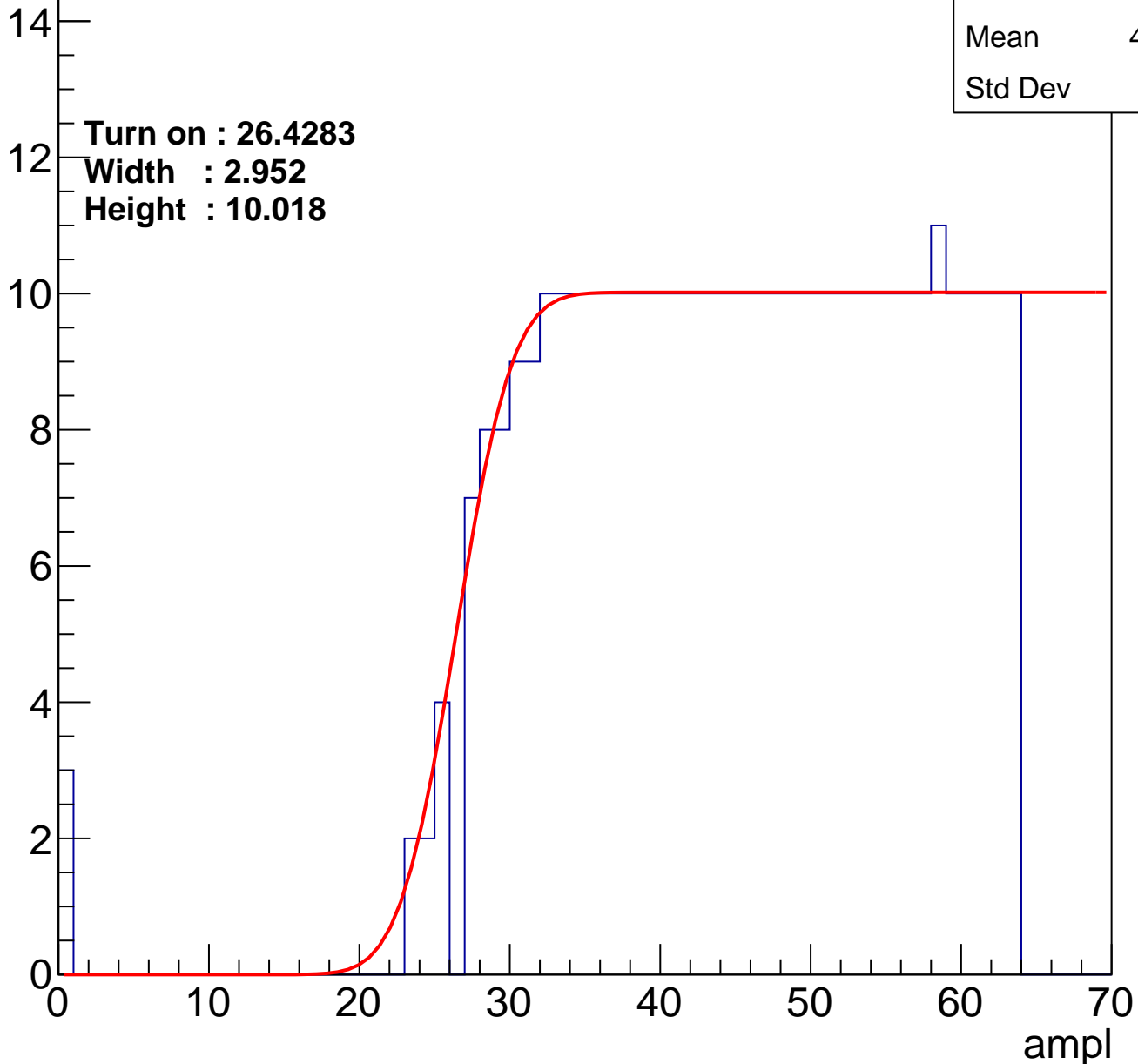
Entries	373
Mean	44.63
Std Dev	11.5

Turn on : 26.4283

Width : 2.952

Height : 10.018

Entry



B0L000S, U18-ch74

calib_packv5_042523_0143.root, FC#5, port B1

Entries	381
Mean	44.13
Std Dev	11.74

Turn on : 25.5544

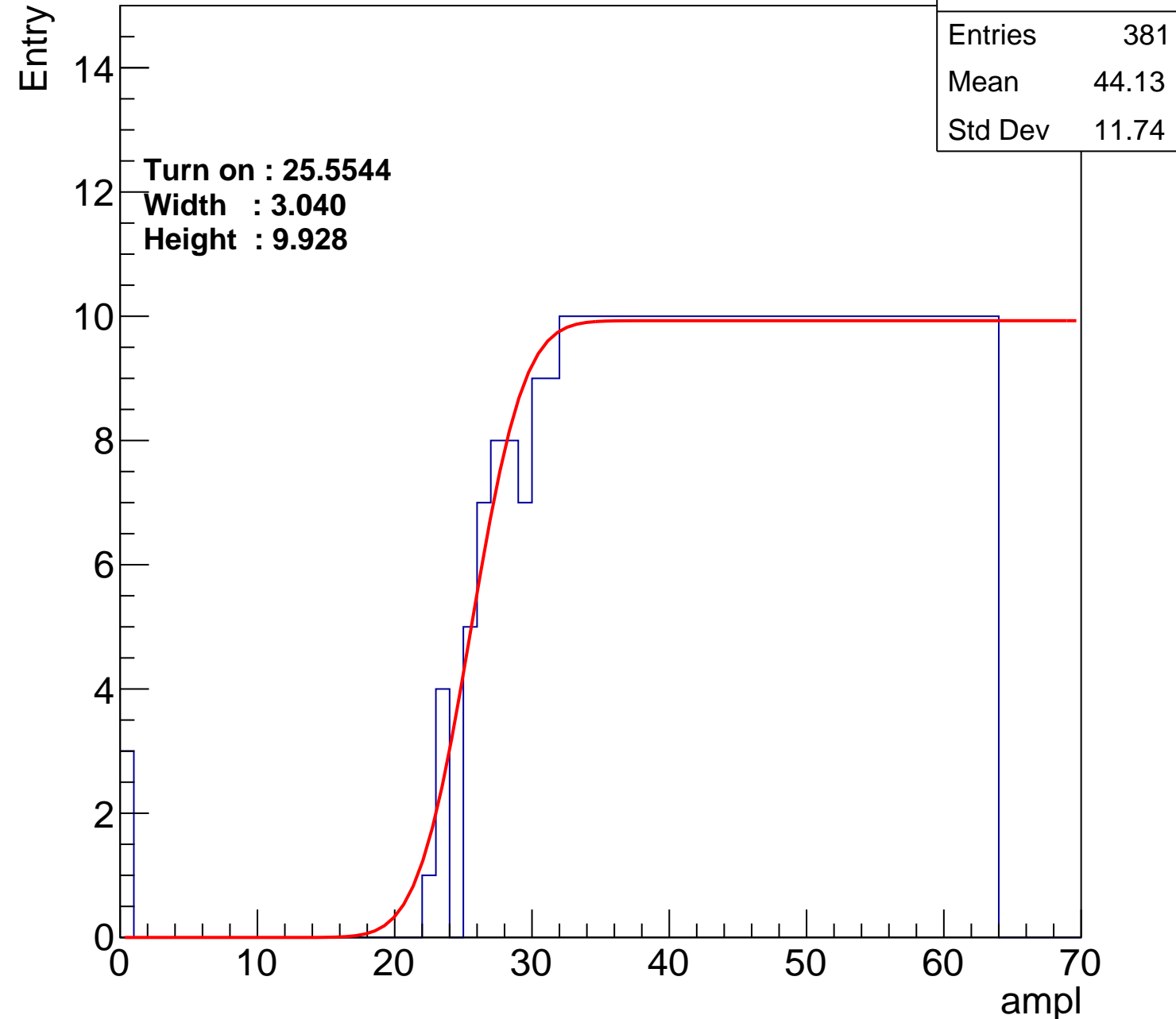
Width : 3.040

Height : 9.928

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch75

calib_packv5_042523_0143.root, FC#5, port B1

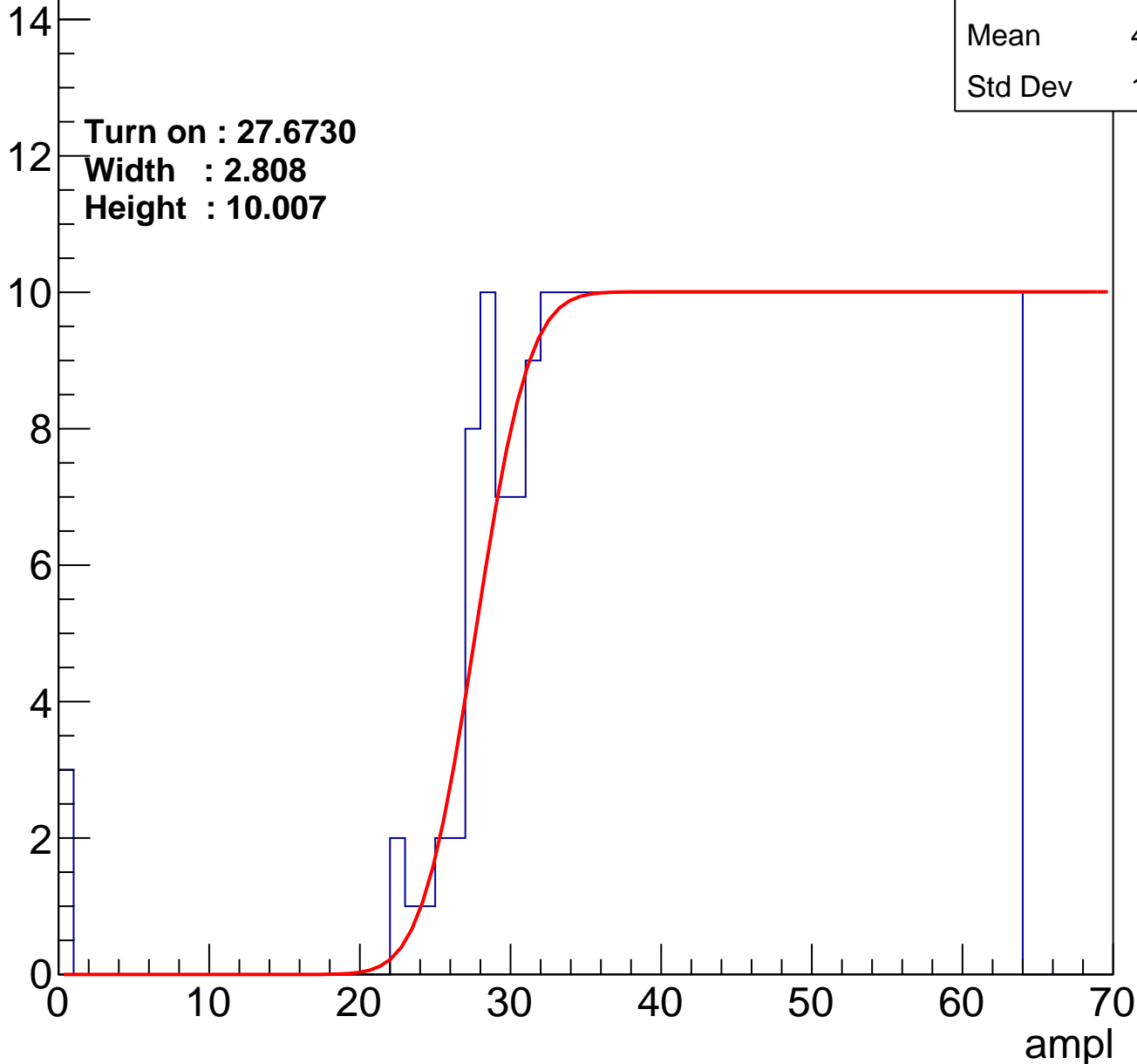
Entries	372
Mean	44.57
Std Dev	11.52

Turn on : 27.6730

Width : 2.808

Height : 10.007

Entry



B0L000S, U18-ch76

calib_packv5_042523_0143.root, FC#5, port B1

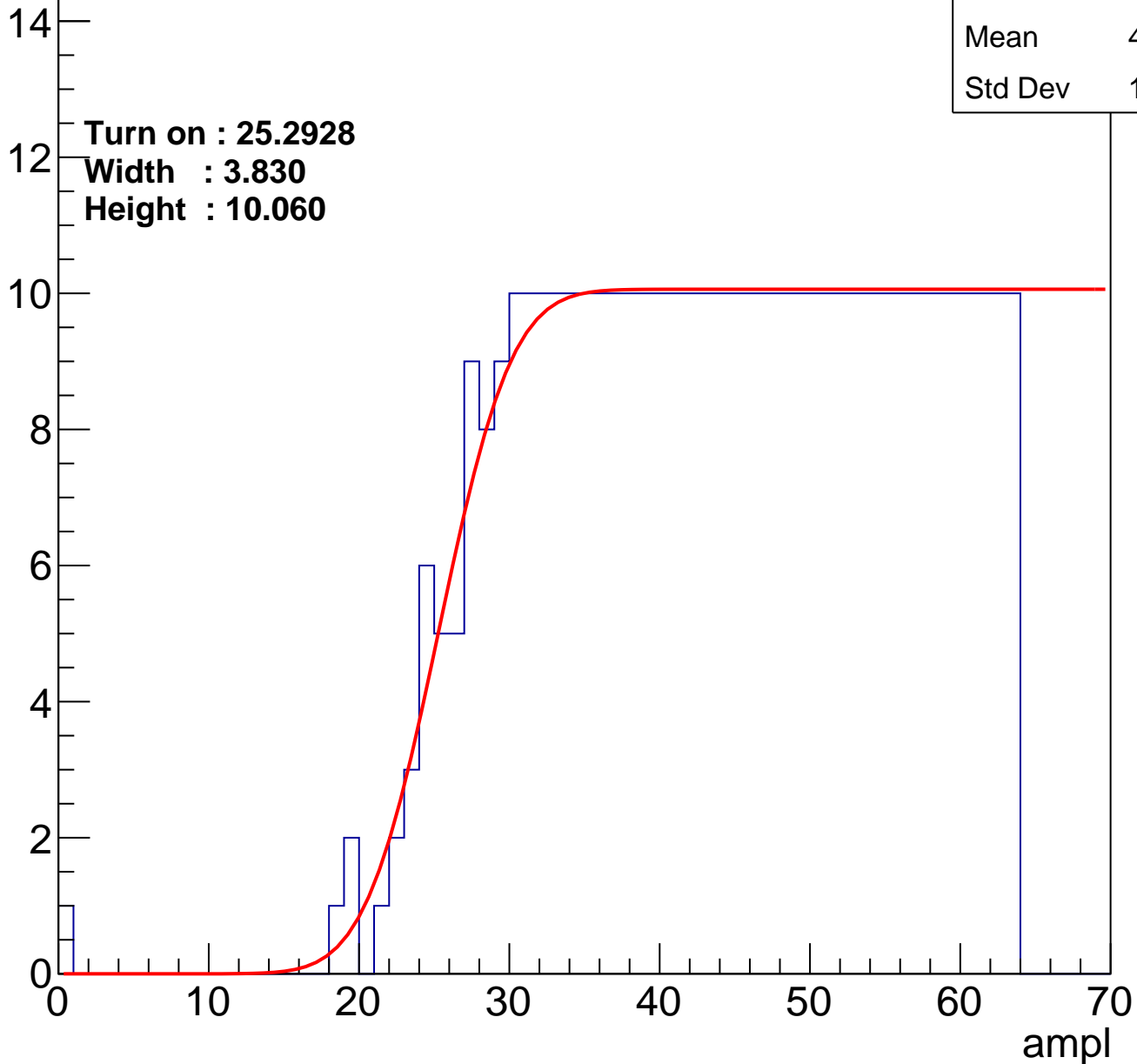
Entries	392
Mean	43.69
Std Dev	11.74

Turn on : 25.2928

Width : 3.830

Height : 10.060

Entry



B0L000S, U18-ch77

calib_packv5_042523_0143.root, FC#5, port B1

Entries	374
Mean	44.34
Std Dev	11.93

Turn on : 27.1333

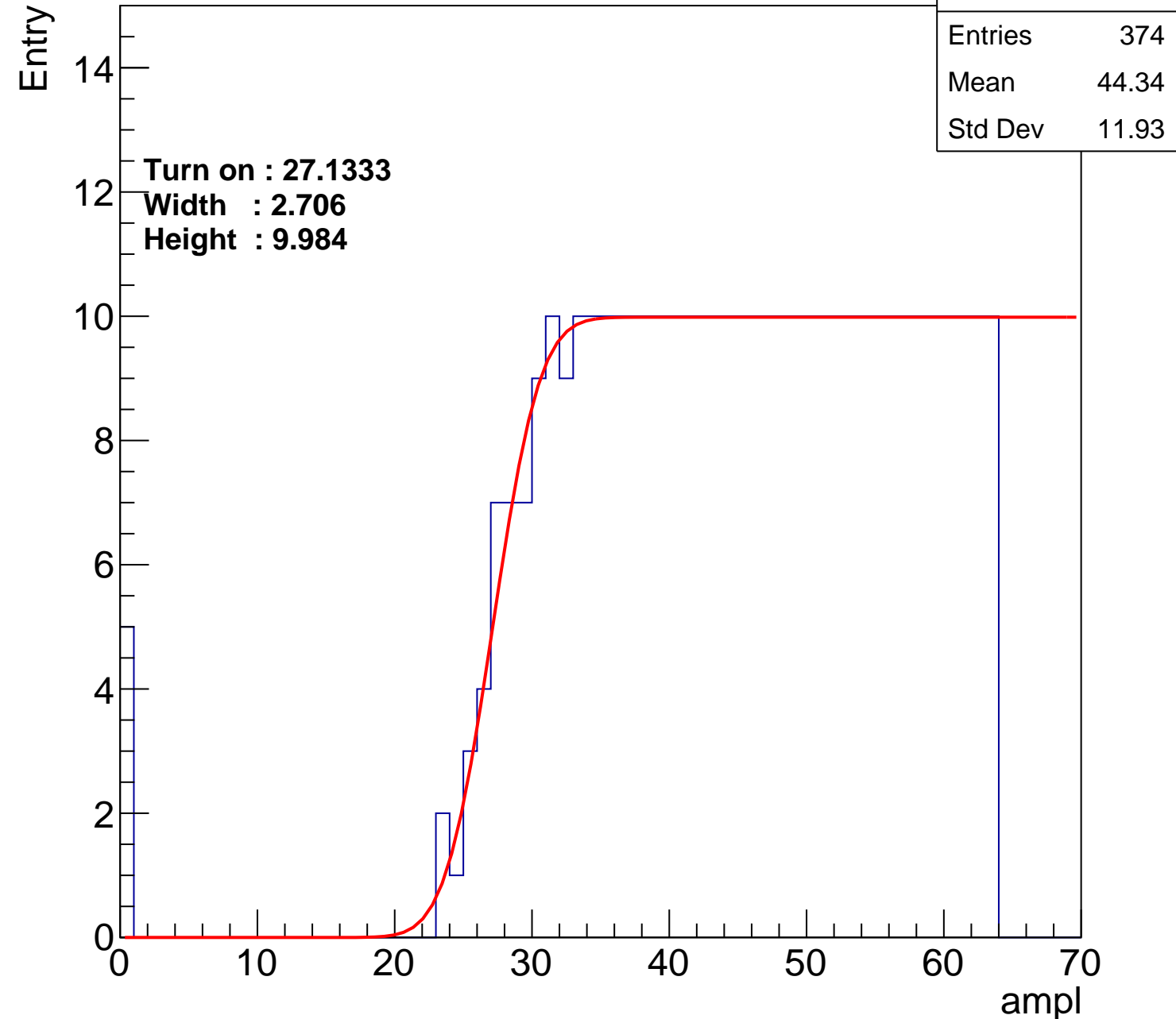
Width : 2.706

Height : 9.984

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch78

calib_packv5_042523_0143.root, FC#5, port B1

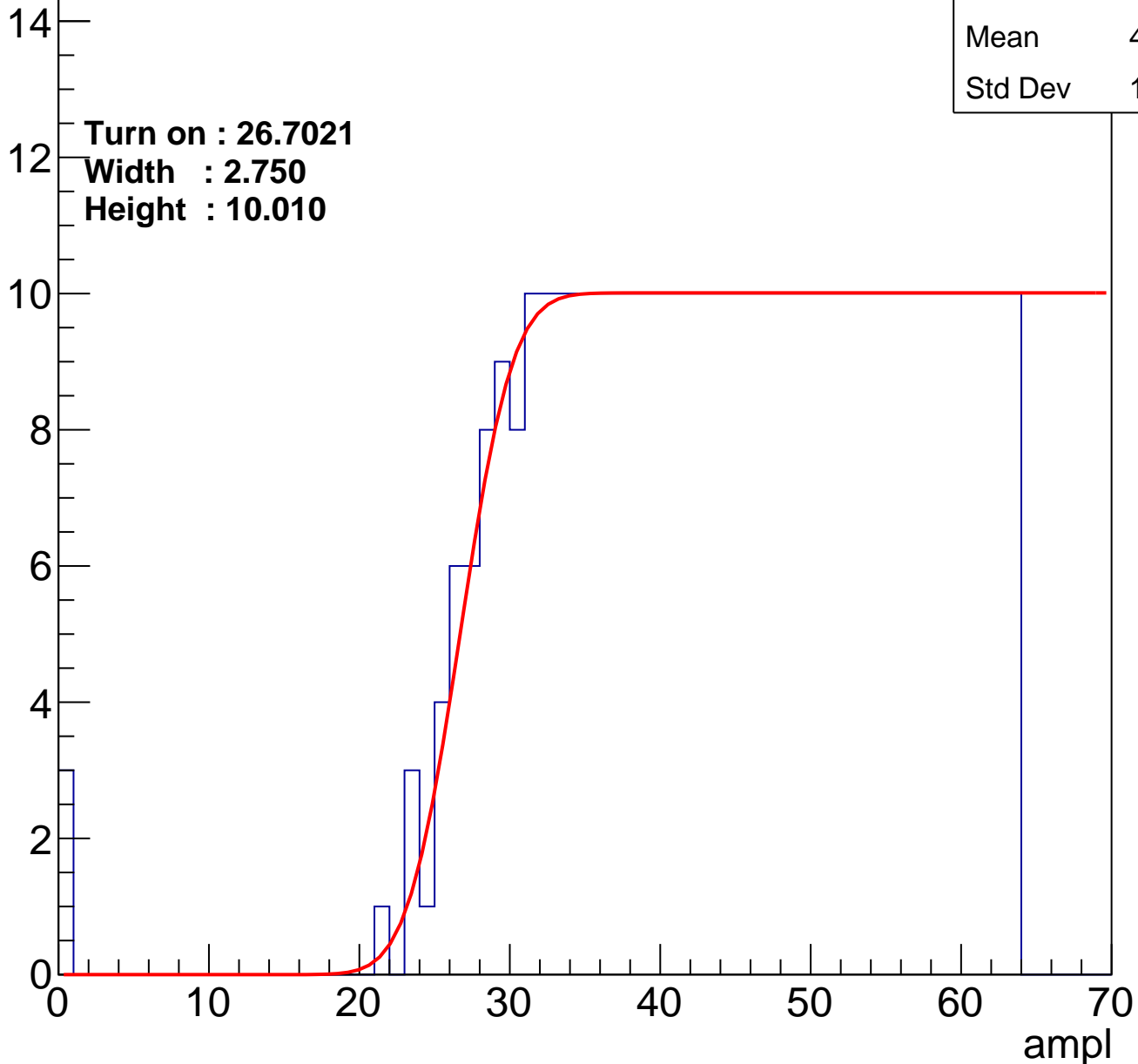
Entries	379
Mean	44.24
Std Dev	11.68

Turn on : 26.7021

Width : 2.750

Height : 10.010

Entry



calib_packv5_042523_0143.root, FC#5, port B1

calib_packv5_042523_0143.root, FC#5, port B1

Turn on : 26.7807
Width : 2.964
Height : 10.046



B0L000S, U18-ch80

calib_packv5_042523_0143.root, FC#5, port B1

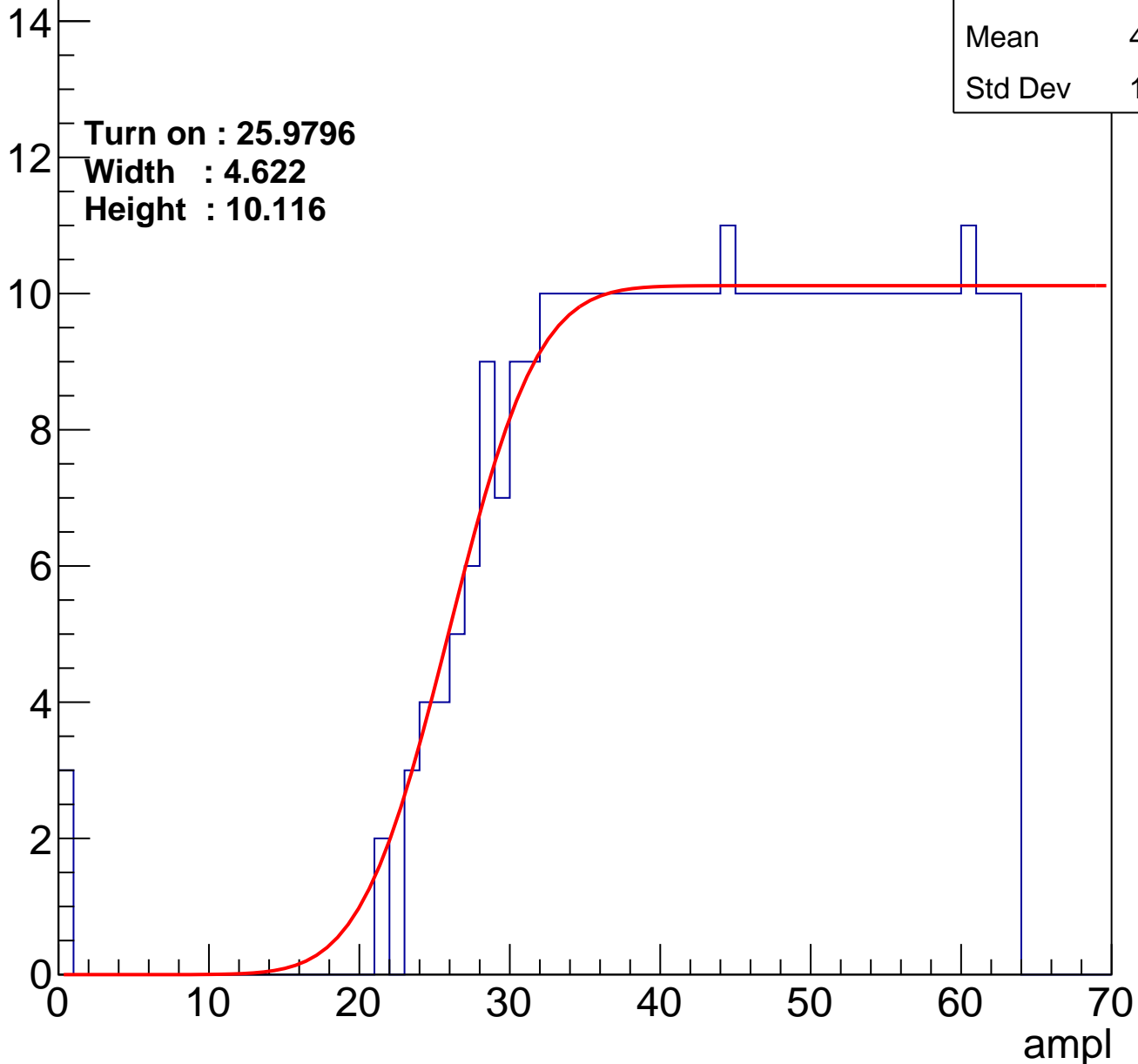
Entries	383
Mean	44.14
Std Dev	11.79

Turn on : 25.9796

Width : 4.622

Height : 10.116

Entry



B0L000S, U18-ch81

calib_packv5_042523_0143.root, FC#5, port B1

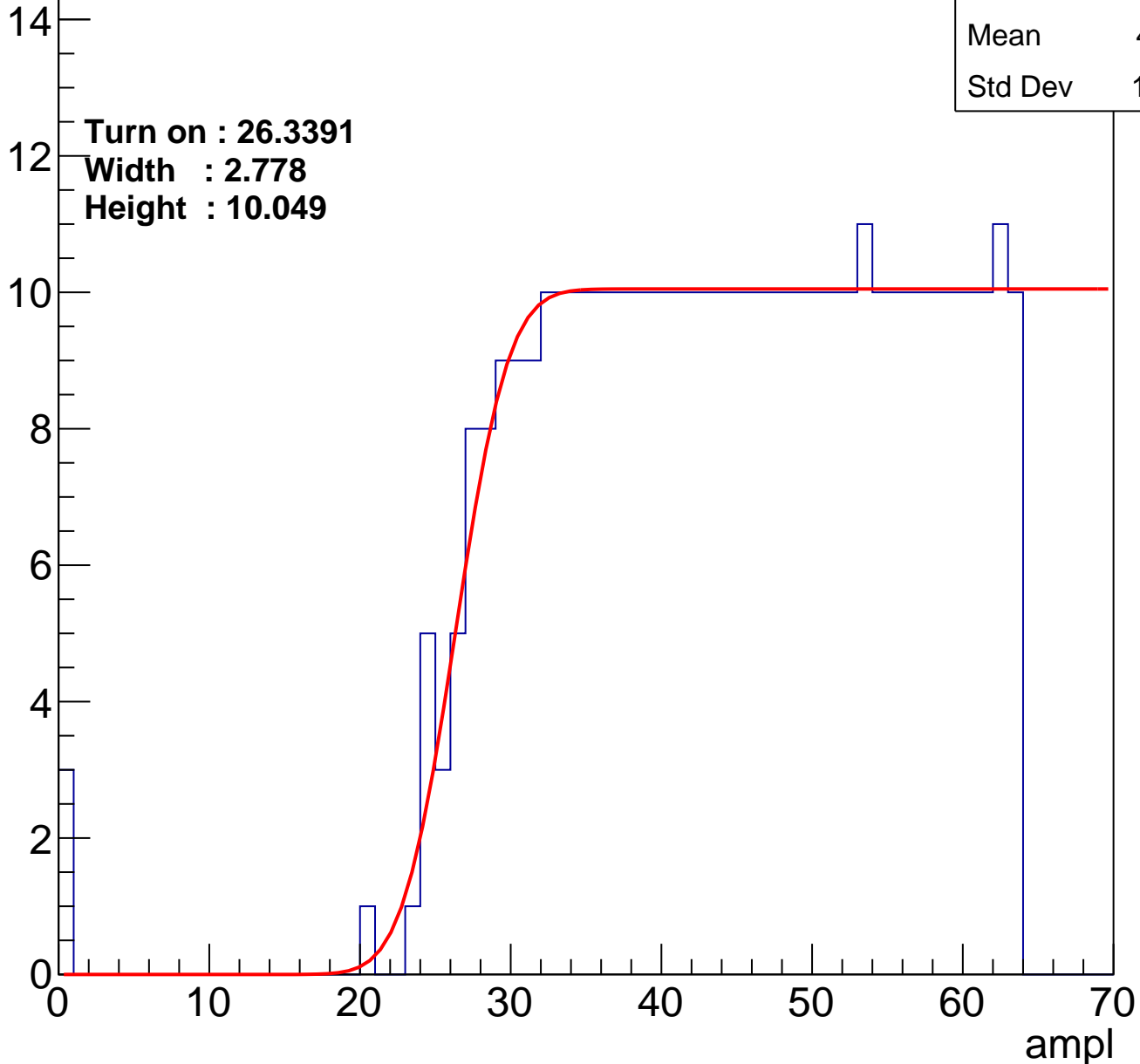
Entries	383
Mean	44.21
Std Dev	11.74

Turn on : 26.3391

Width : 2.778

Height : 10.049

Entry



B0L000S, U18-ch82

calib_packv5_042523_0143.root, FC#5, port B1

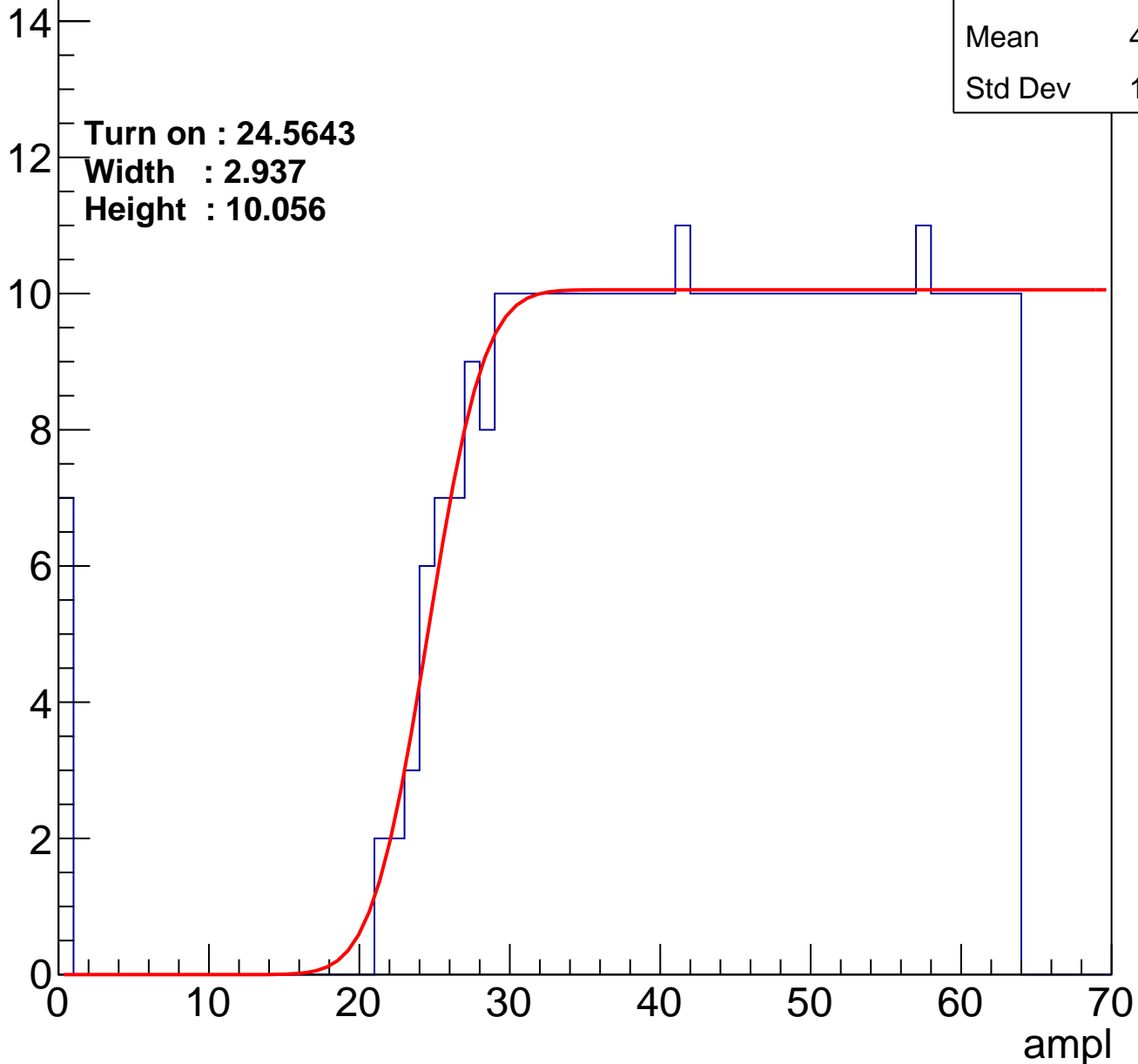
Entries	403
Mean	42.98
Std Dev	12.76

Turn on : 24.5643

Width : 2.937

Height : 10.056

Entry



B0L000S, U18-ch83

calib_packv5_042523_0143.root, FC#5, port B1

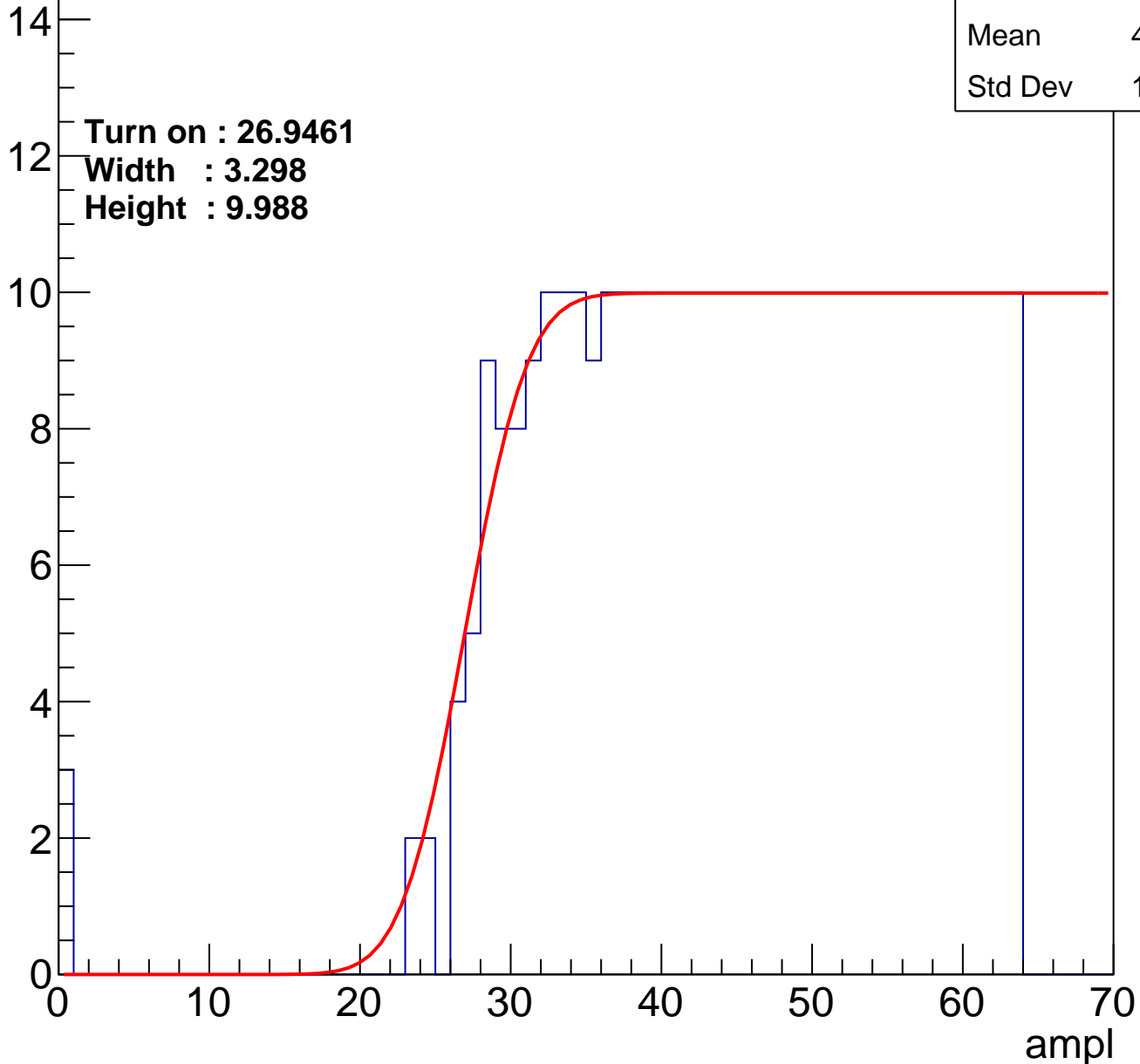
Entries	369
Mean	44.72
Std Dev	11.45

Turn on : 26.9461

Width : 3.298

Height : 9.988

Entry



B0L000S, U18-ch84

calib_packv5_042523_0143.root, FC#5, port B1

Entries	357
Mean	45.44
Std Dev	10.86

Turn on : 28.4732

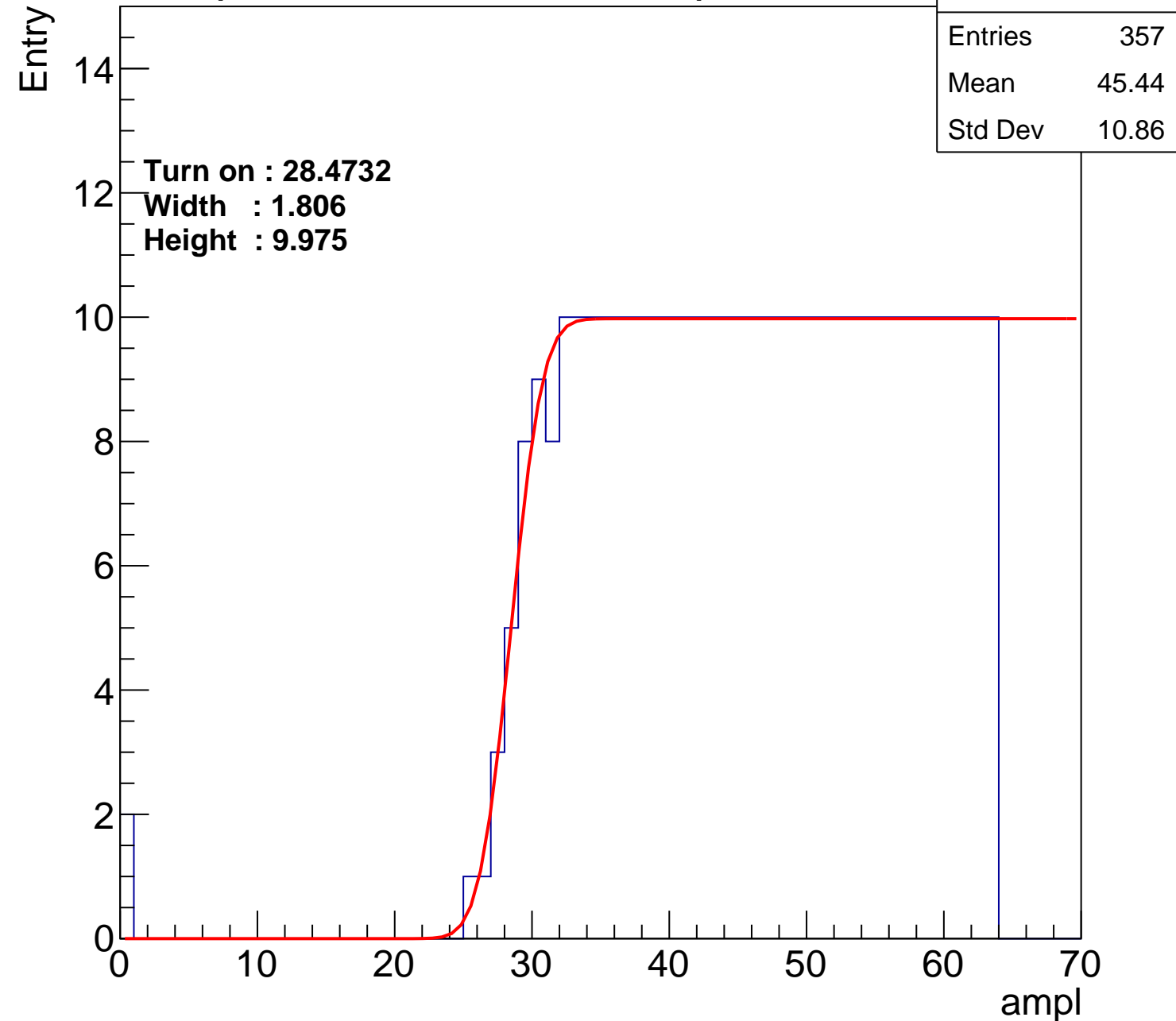
Width : 1.806

Height : 9.975

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch85

calib_packv5_042523_0143.root, FC#5, port B1

Entries	387
Mean	43.93
Std Dev	11.68

Turn on : 26.0354

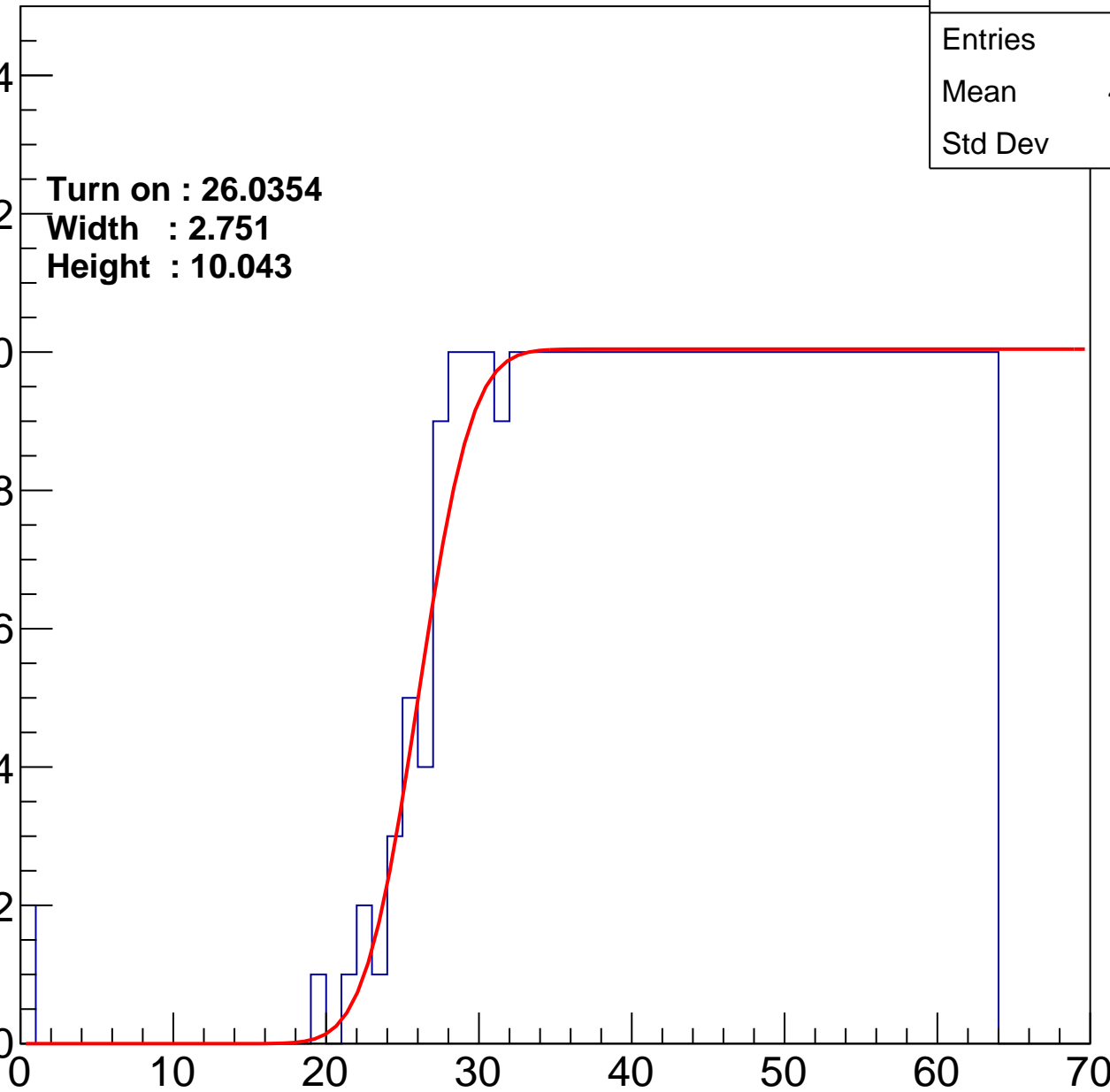
Width : 2.751

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch86

calib_packv5_042523_0143.root, FC#5, port B1

Entries	383
Mean	44.2
Std Dev	11.61

Turn on : 25.9350

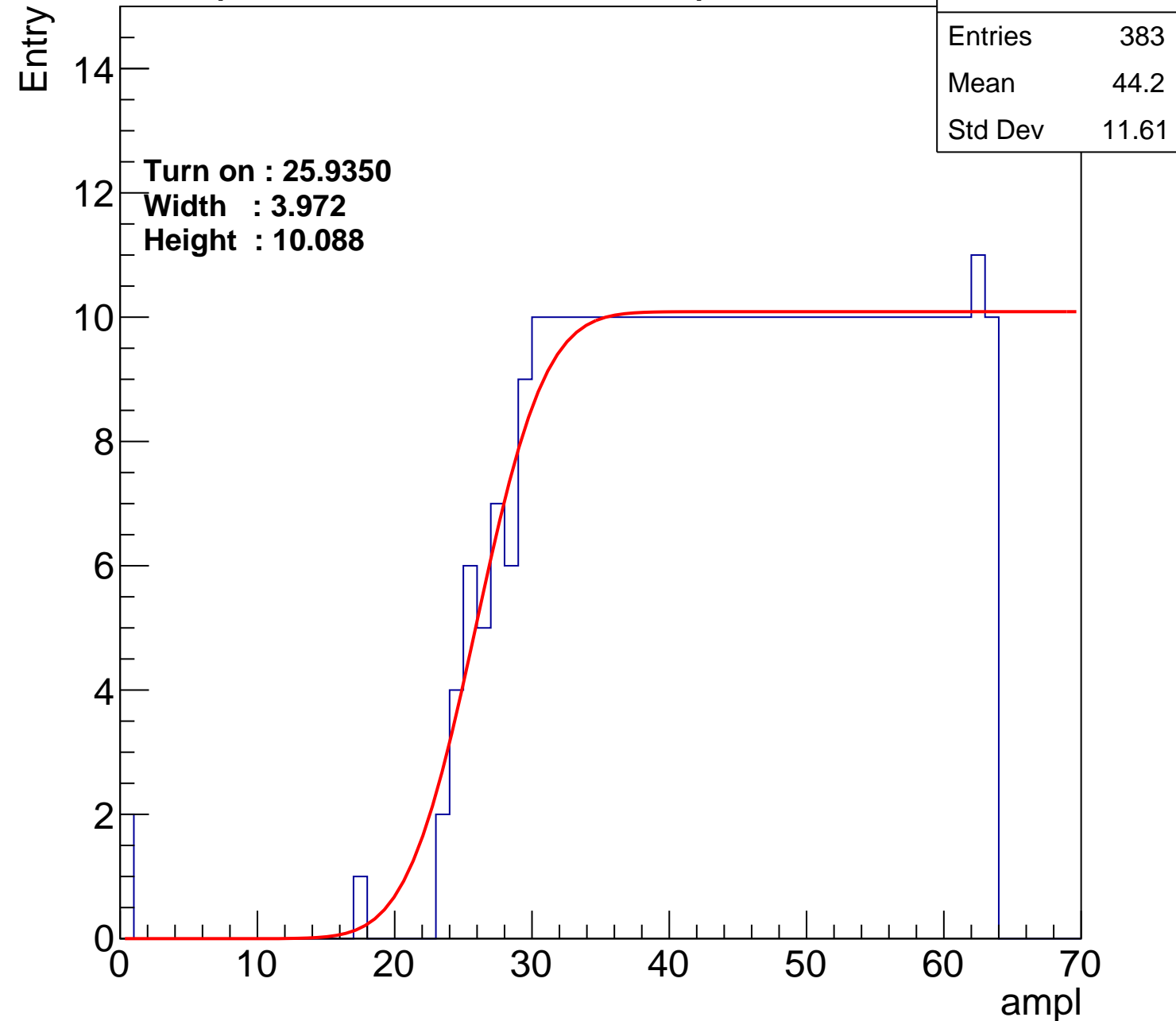
Width : 3.972

Height : 10.088

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch87

calib_packv5_042523_0143.root, FC#5, port B1

Entries	378
Mean	44.32
Std Dev	11.6

Turn on : 27.0916

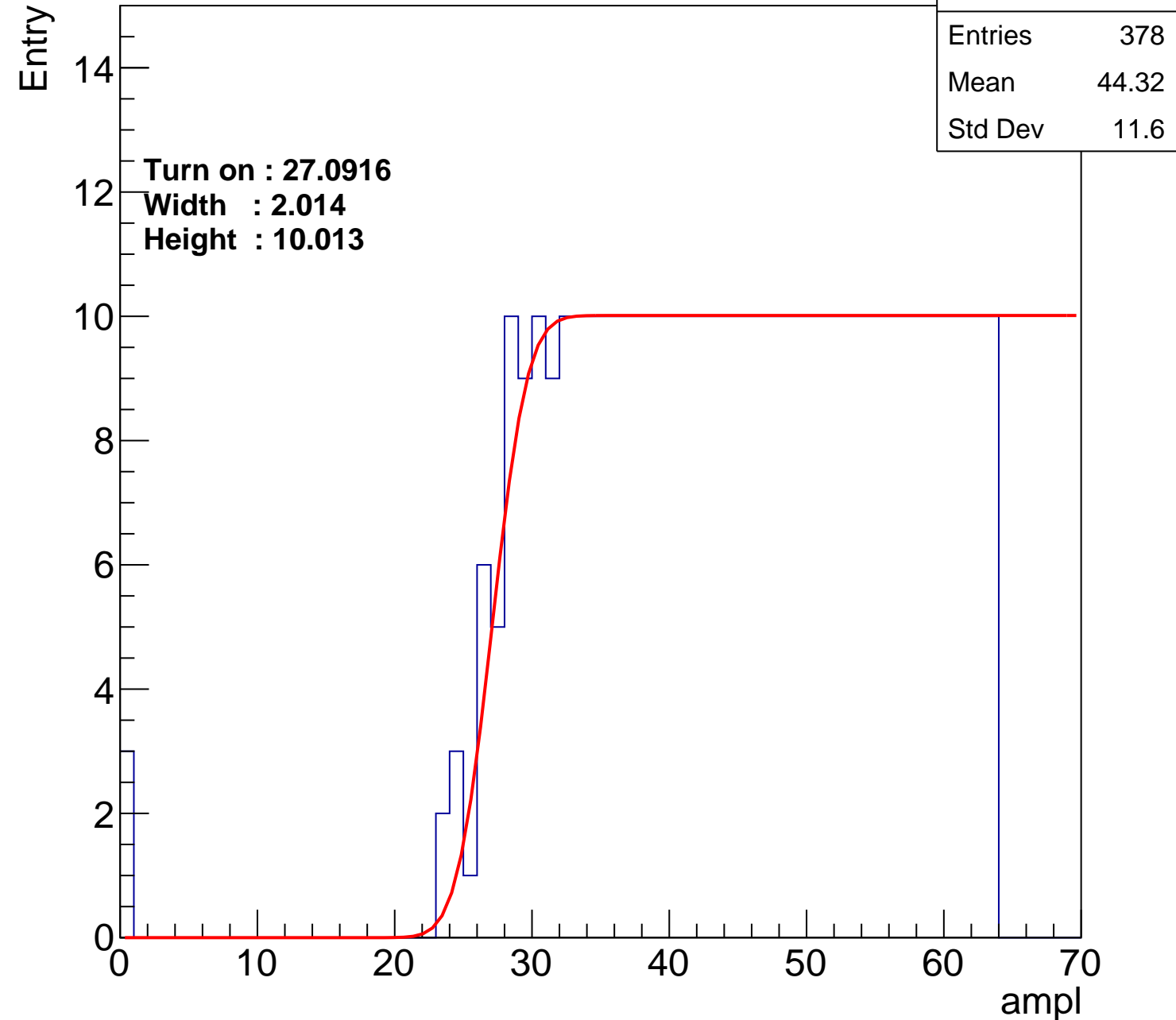
Width : 2.014

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch88

calib_packv5_042523_0143.root, FC#5, port B1

Entries	381
Mean	44.24
Std Dev	11.7

Turn on : 26.7261

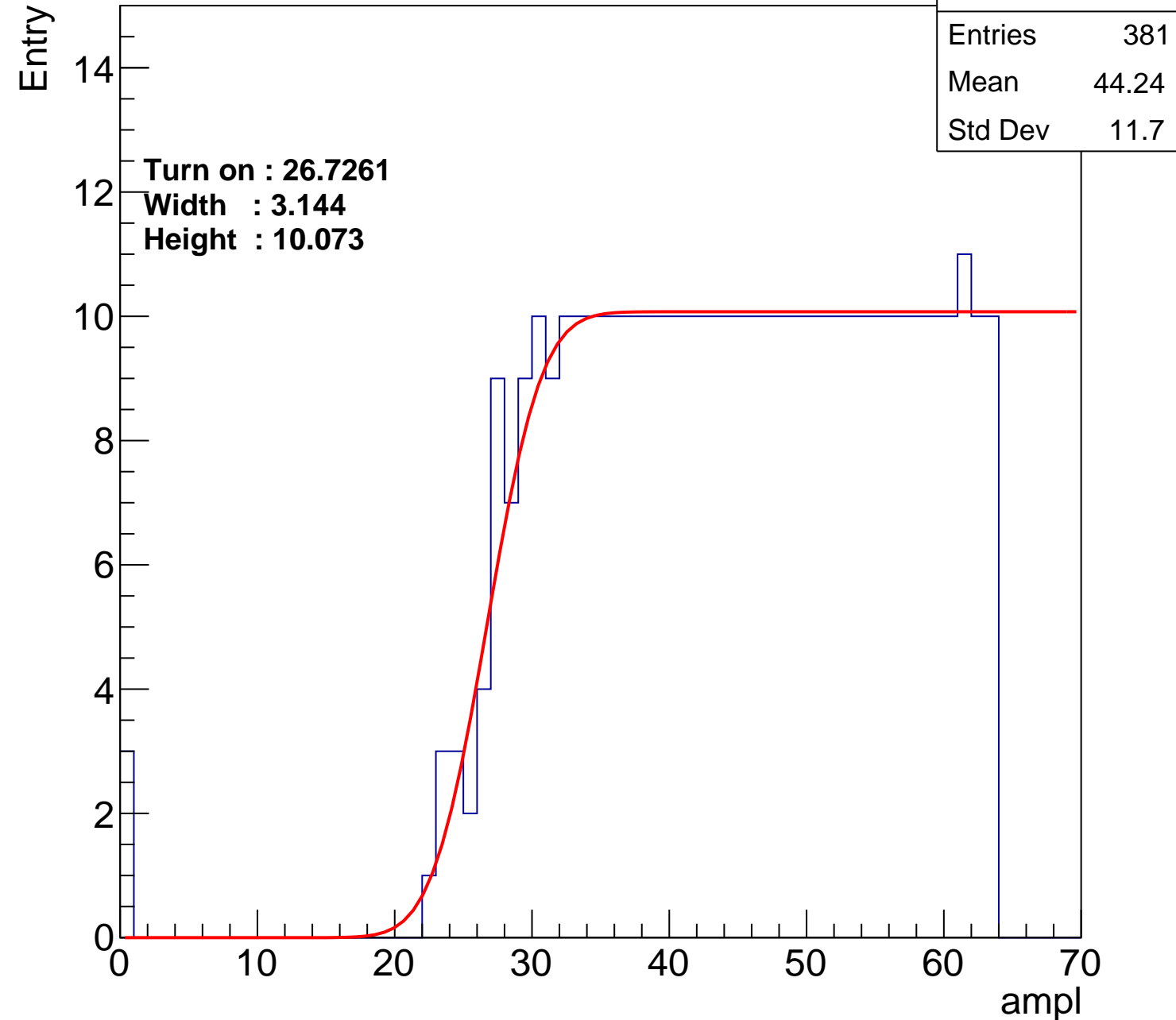
Width : 3.144

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch89

calib_packv5_042523_0143.root, FC#5, port B1

Entries	387
Mean	43.82
Std Dev	11.92

Turn on : 25.4294

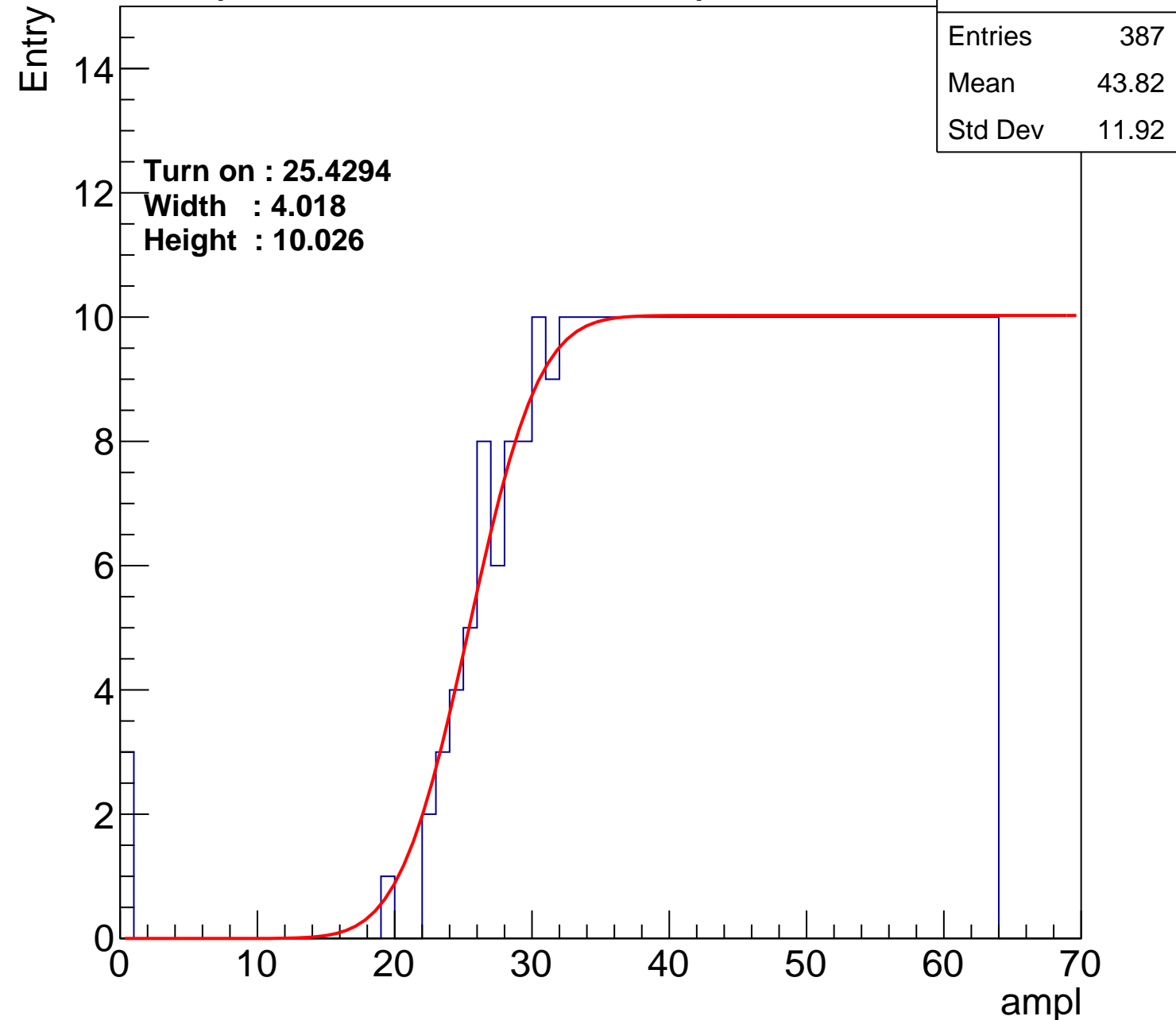
Width : 4.018

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch90

calib_packv5_042523_0143.root, FC#5, port B1

Entries	385
Mean	43.92
Std Dev	11.94

Turn on : 26.1210

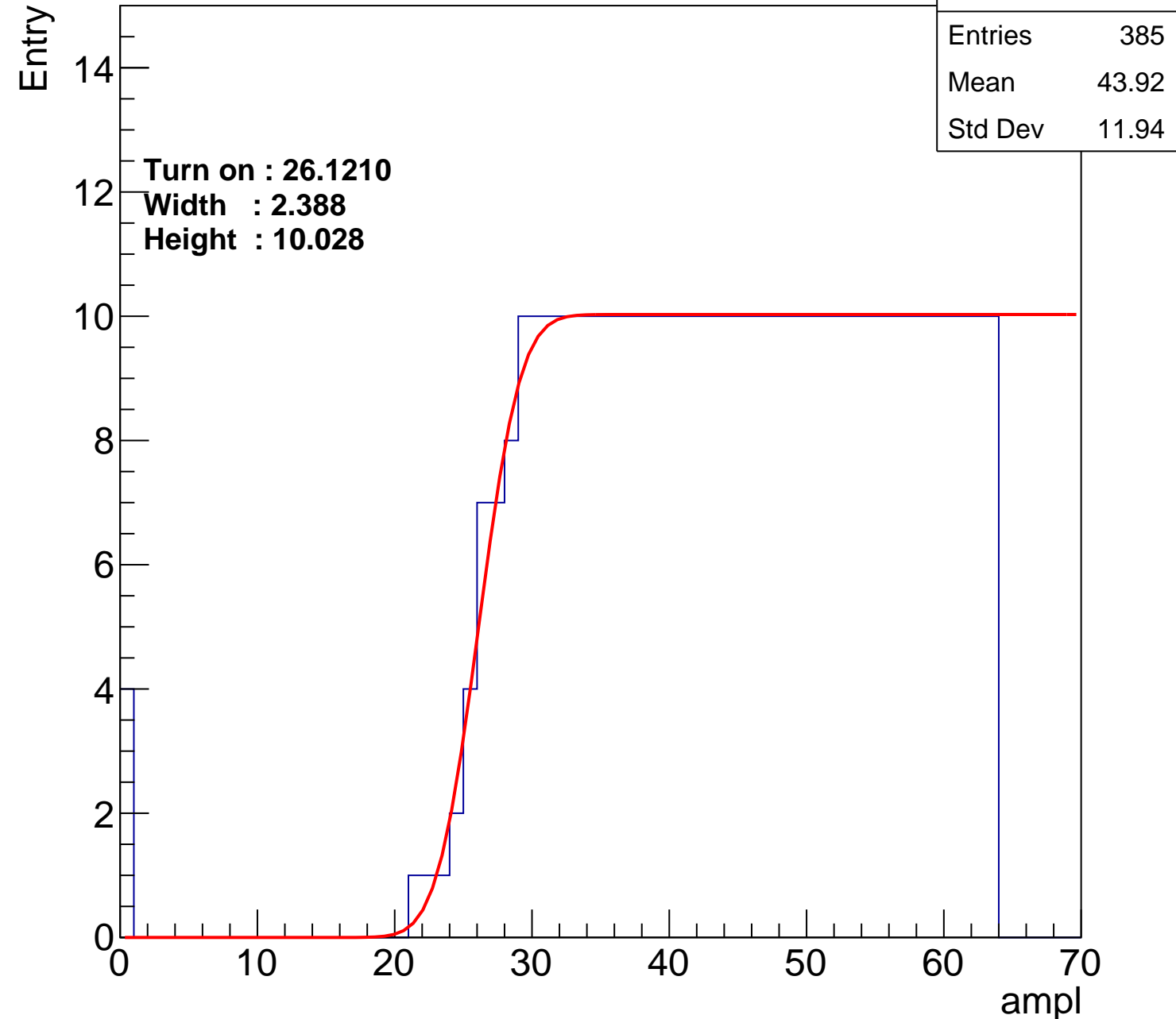
Width : 2.388

Height : 10.028

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch91

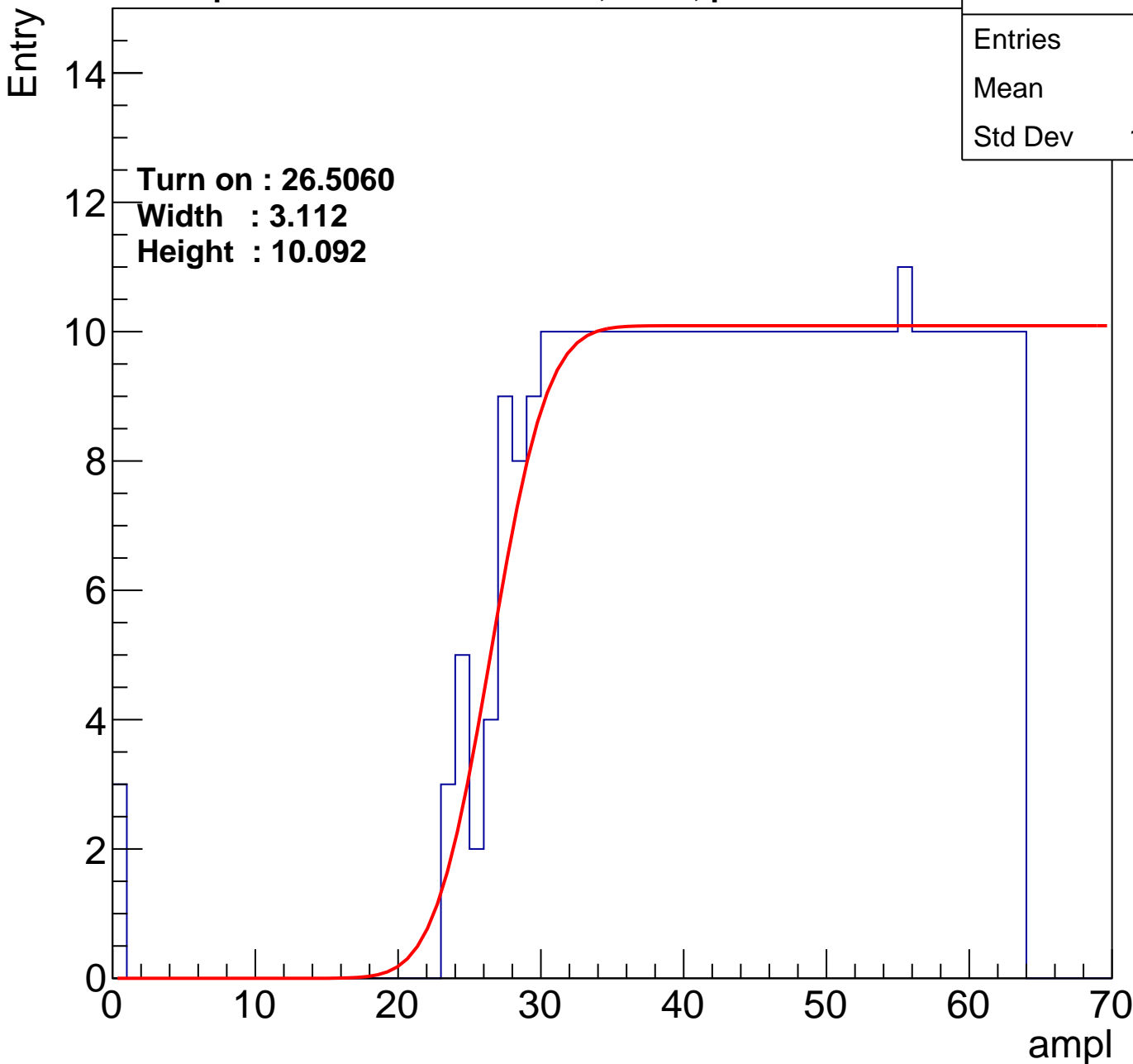
calib_packv5_042523_0143.root, FC#5, port B1

Entries	384
Mean	44.1
Std Dev	11.72

Turn on : 26.5060

Width : 3.112

Height : 10.092



B0L000S, U18-ch92

calib_packv5_042523_0143.root, FC#5, port B1

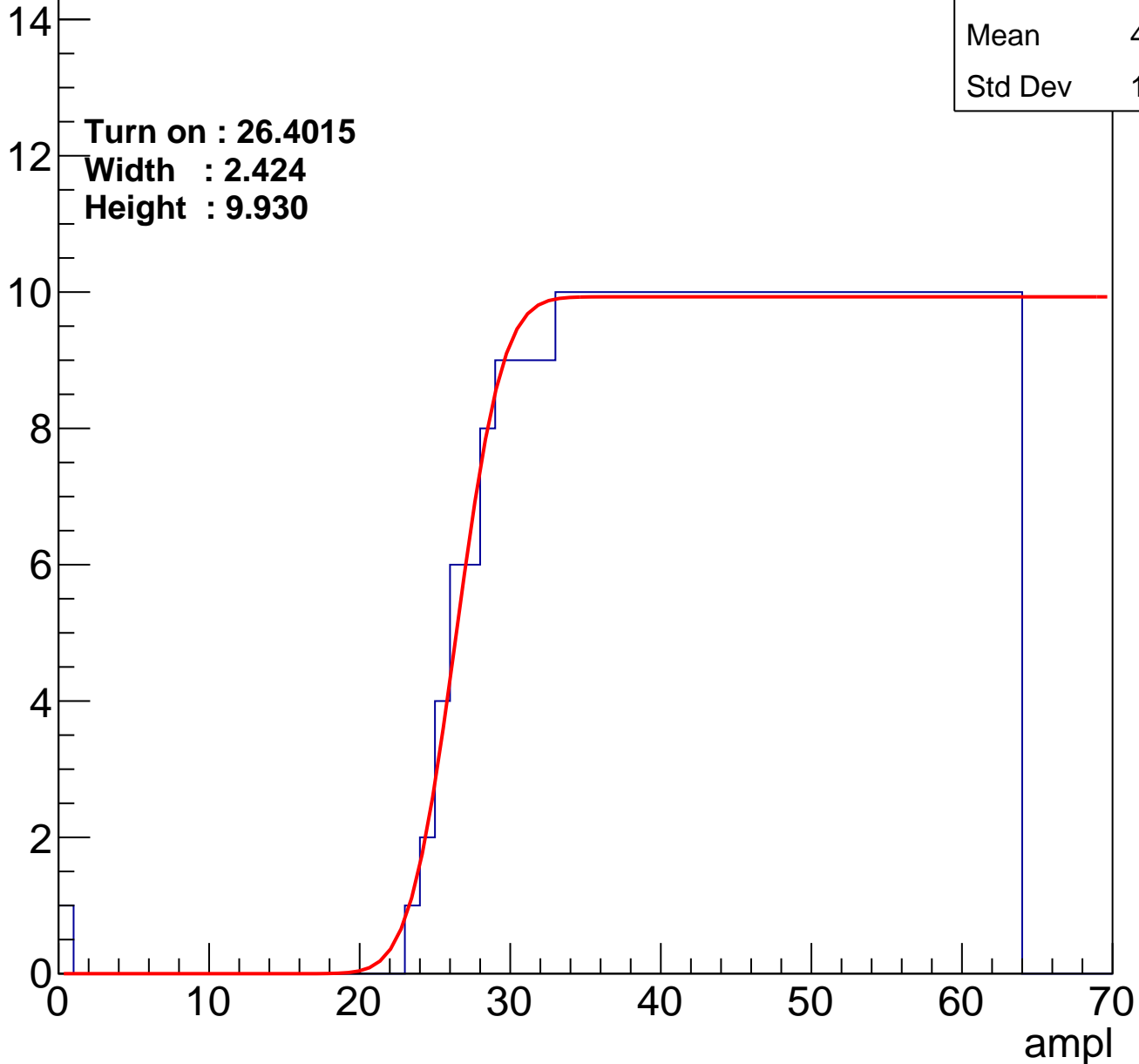
Entries	374
Mean	44.63
Std Dev	11.16

Turn on : 26.4015

Width : 2.424

Height : 9.930

Entry



B0L000S, U18-ch93

calib_packv5_042523_0143.root, FC#5, port B1

Entries	373
Mean	44.57
Std Dev	11.5

Turn on : 27.1018

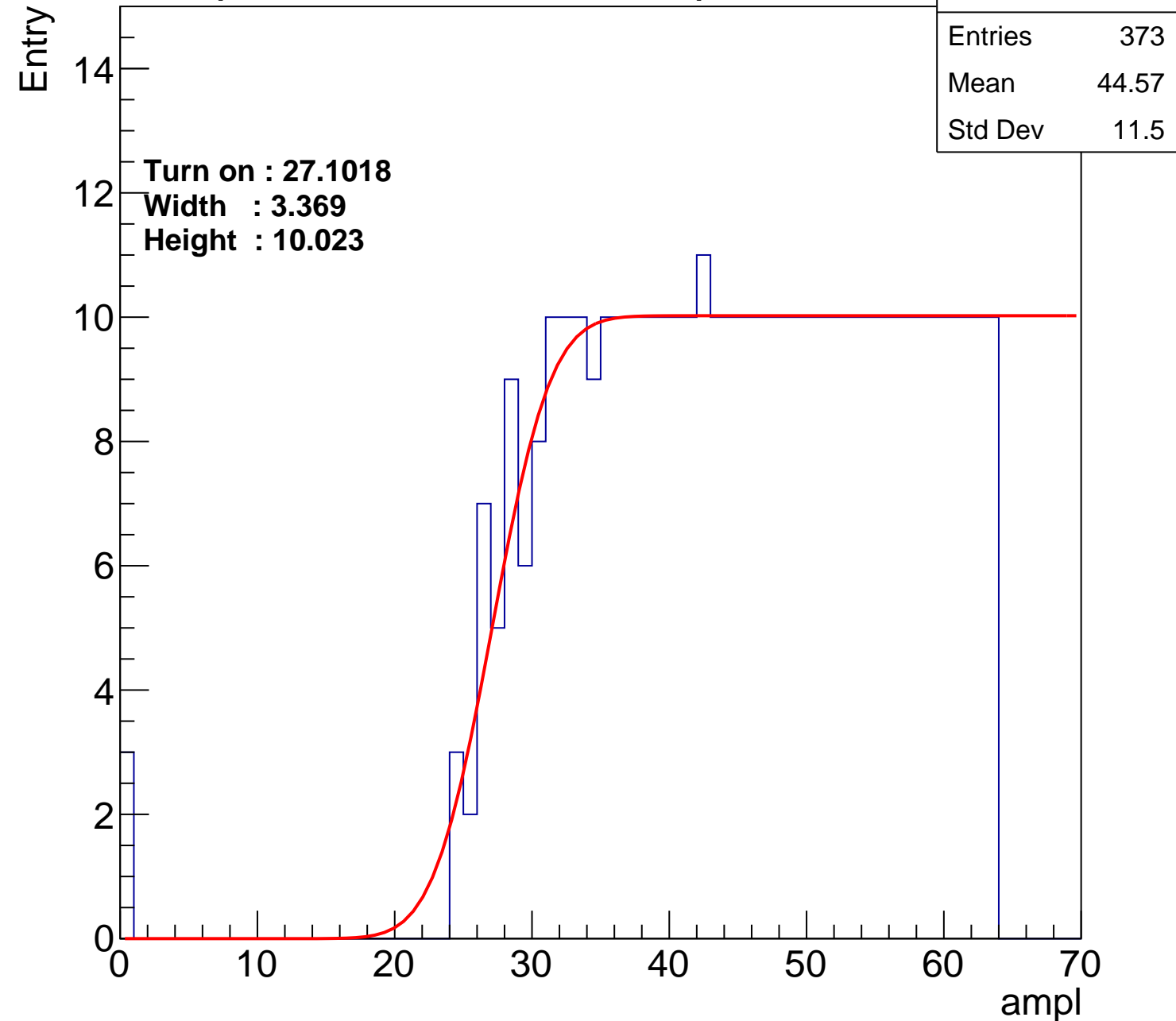
Width : 3.369

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch94

calib_packv5_042523_0143.root, FC#5, port B1

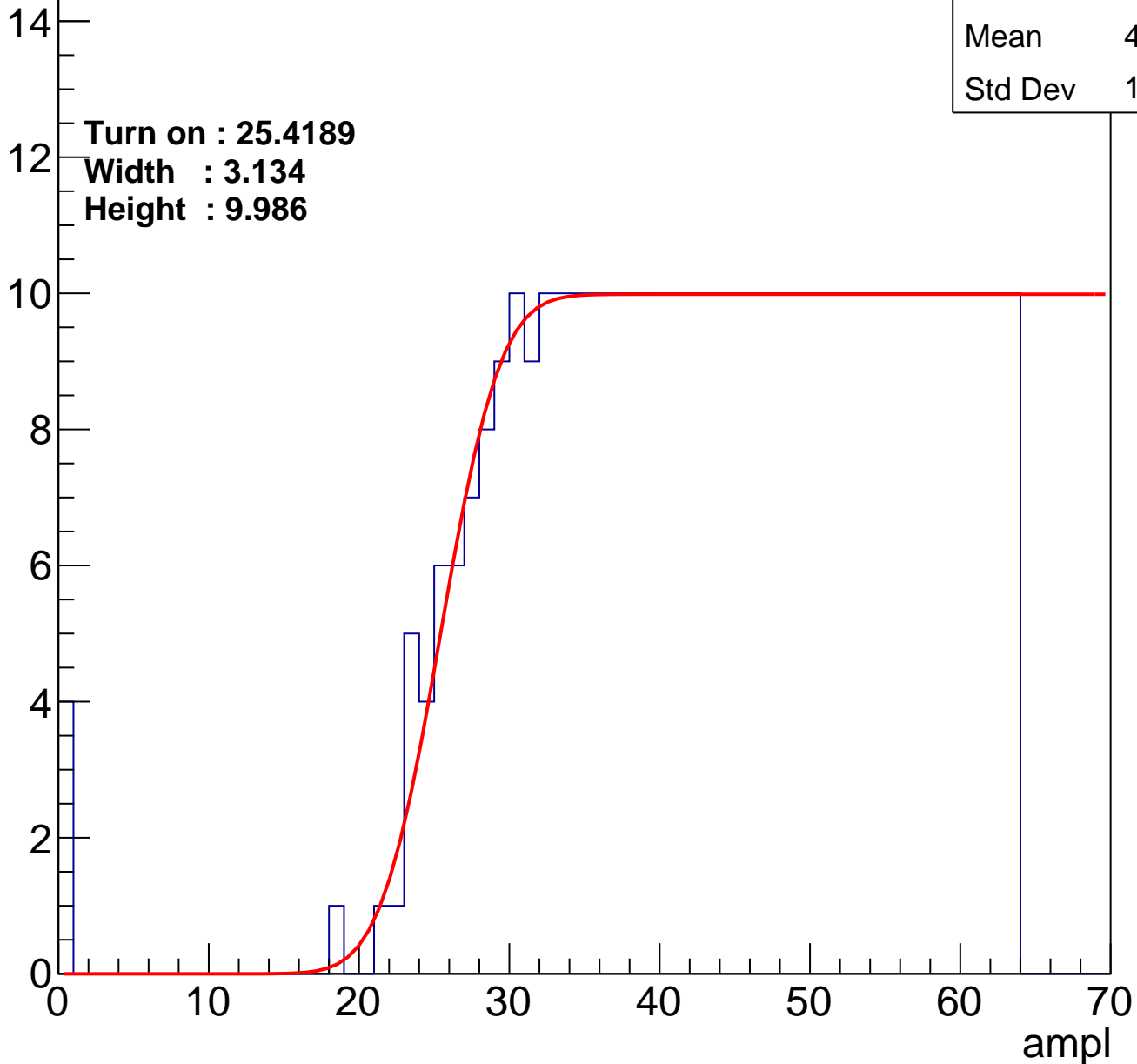
Entries	391
Mean	43.56
Std Dev	12.18

Turn on : 25.4189

Width : 3.134

Height : 9.986

Entry



B0L000S, U18-ch95

calib_packv5_042523_0143.root, FC#5, port B1

Entries	380
Mean	44.29
Std Dev	11.47

Turn on : 26.5616

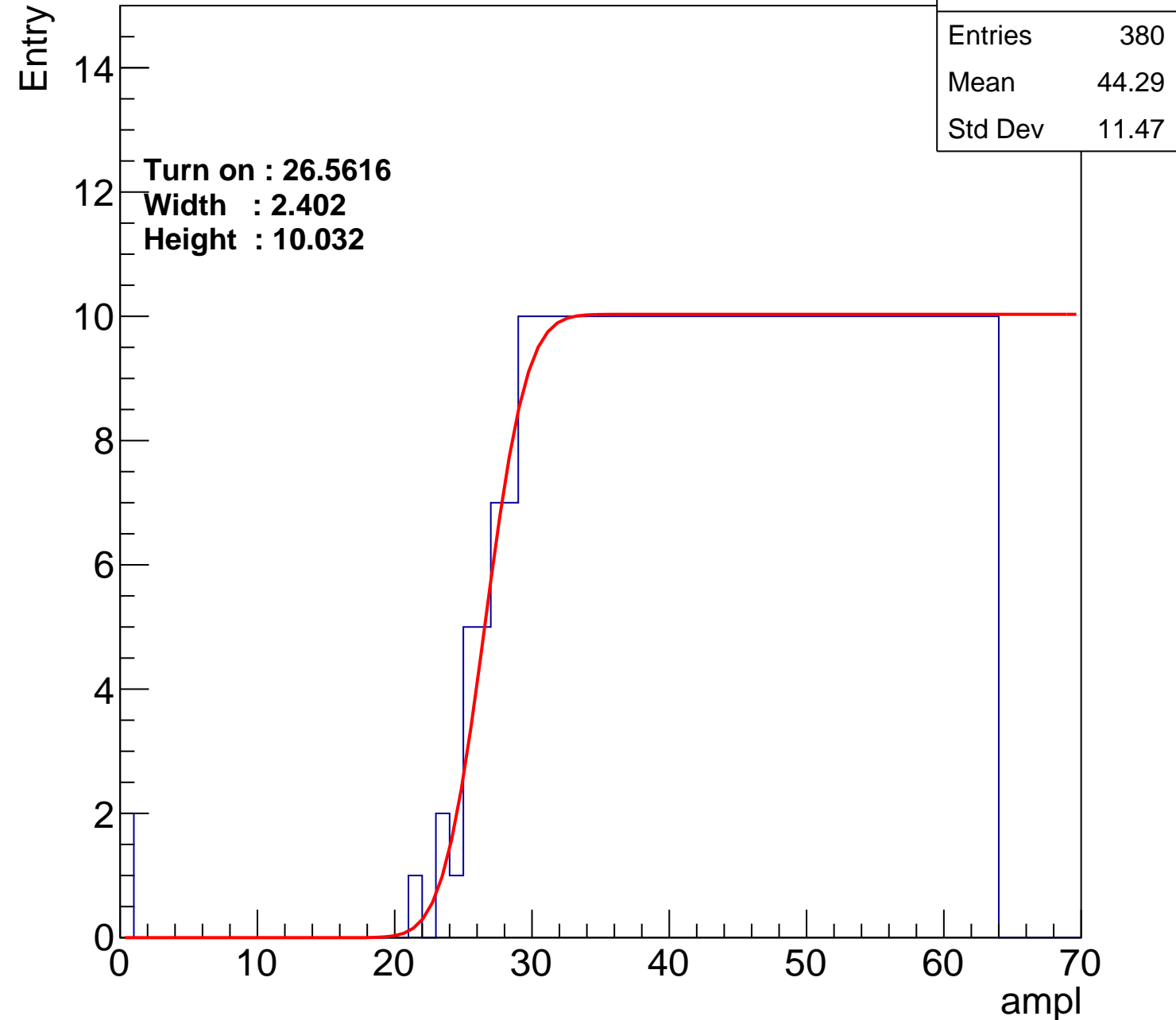
Width : 2.402

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch96

calib_packv5_042523_0143.root, FC#5, port B1

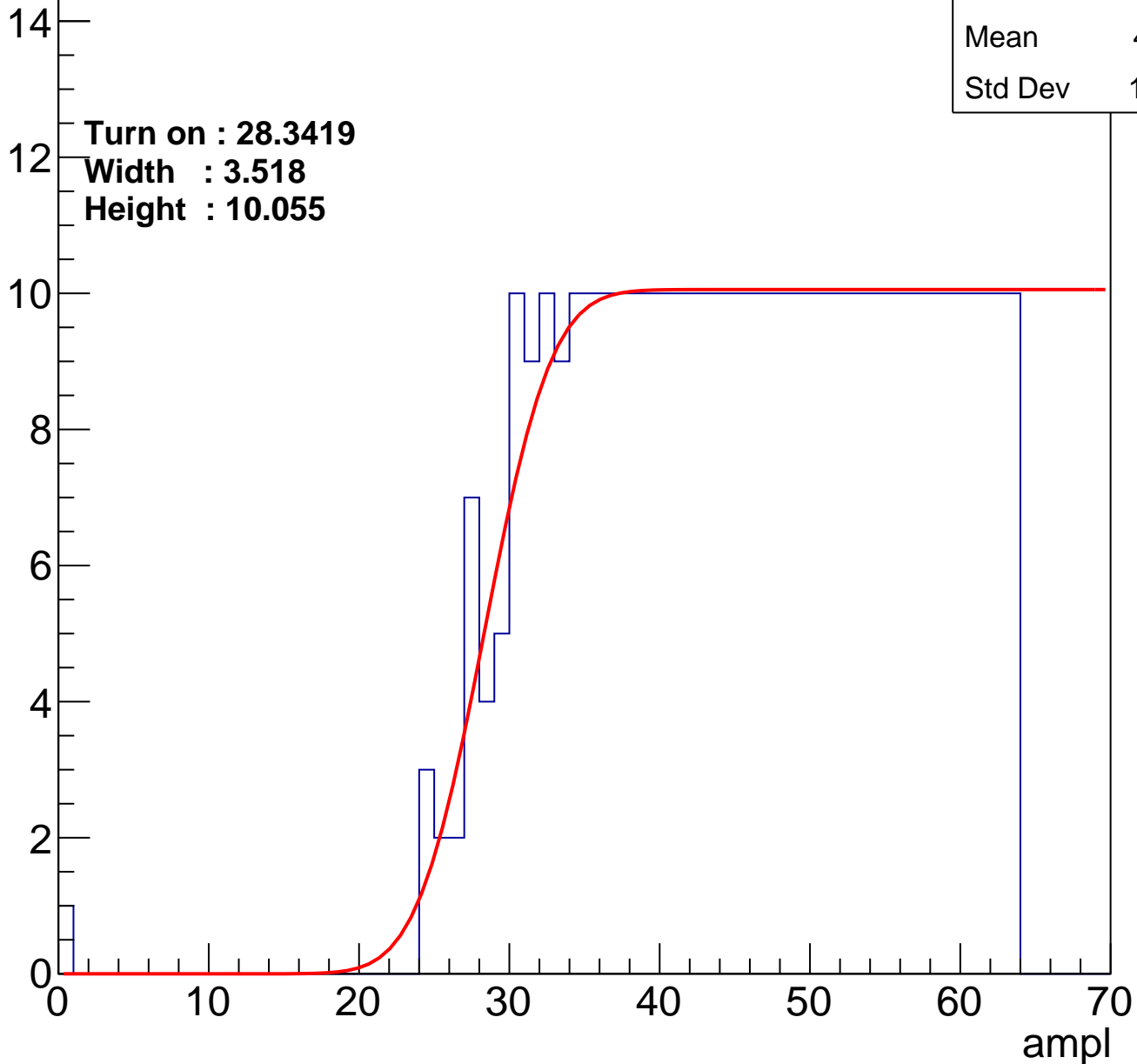
Entries	362
Mean	45.21
Std Dev	10.86

Turn on : 28.3419

Width : 3.518

Height : 10.055

Entry



B0L000S, U18-ch97

calib_packv5_042523_0143.root, FC#5, port B1

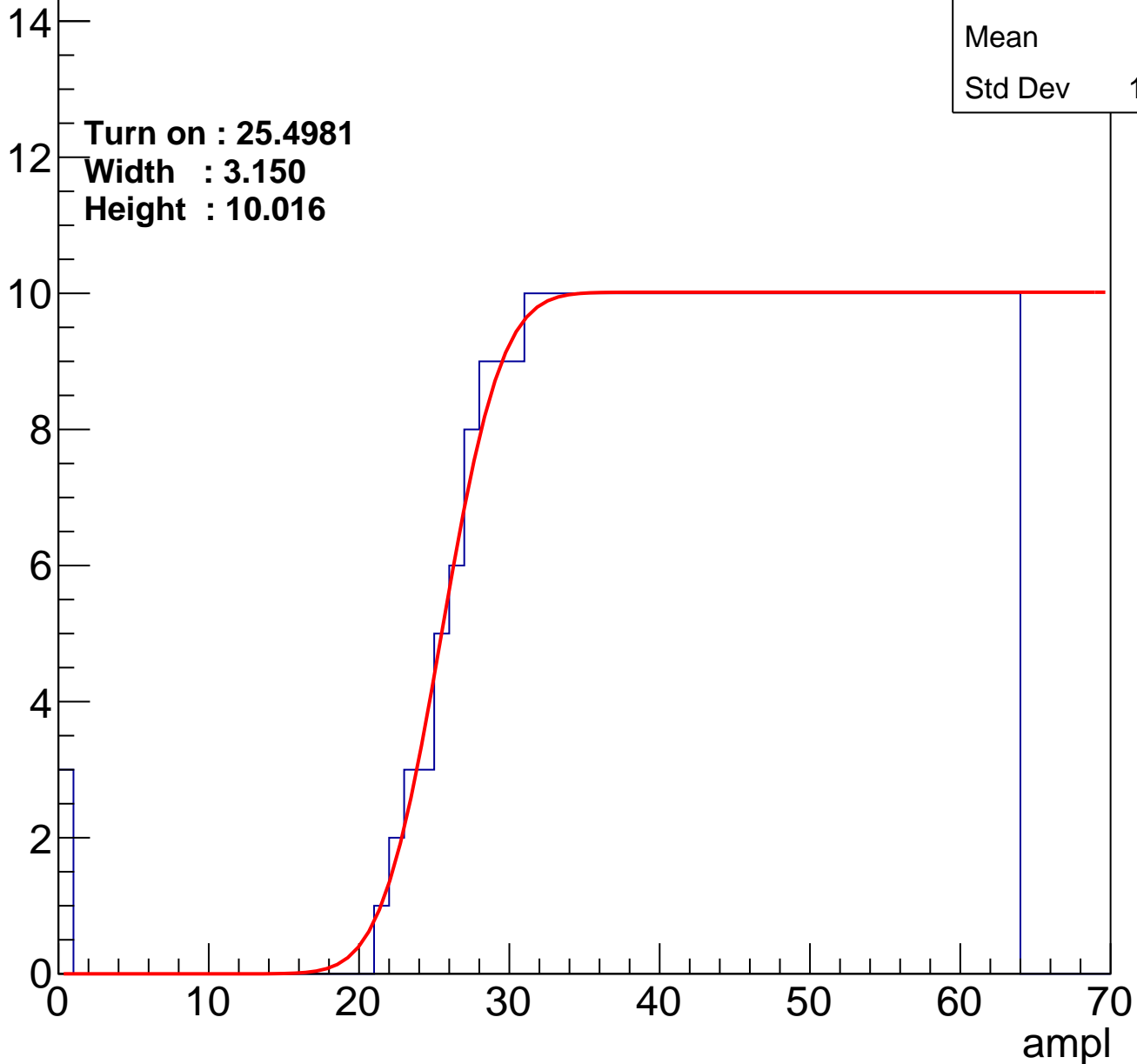
Entries	388
Mean	43.8
Std Dev	11.89

Turn on : 25.4981

Width : 3.150

Height : 10.016

Entry



B0L000S, U18-ch98

calib_packv5_042523_0143.root, FC#5, port B1

Entries	361
Mean	45.2
Std Dev	11.04

Turn on : 28.5658

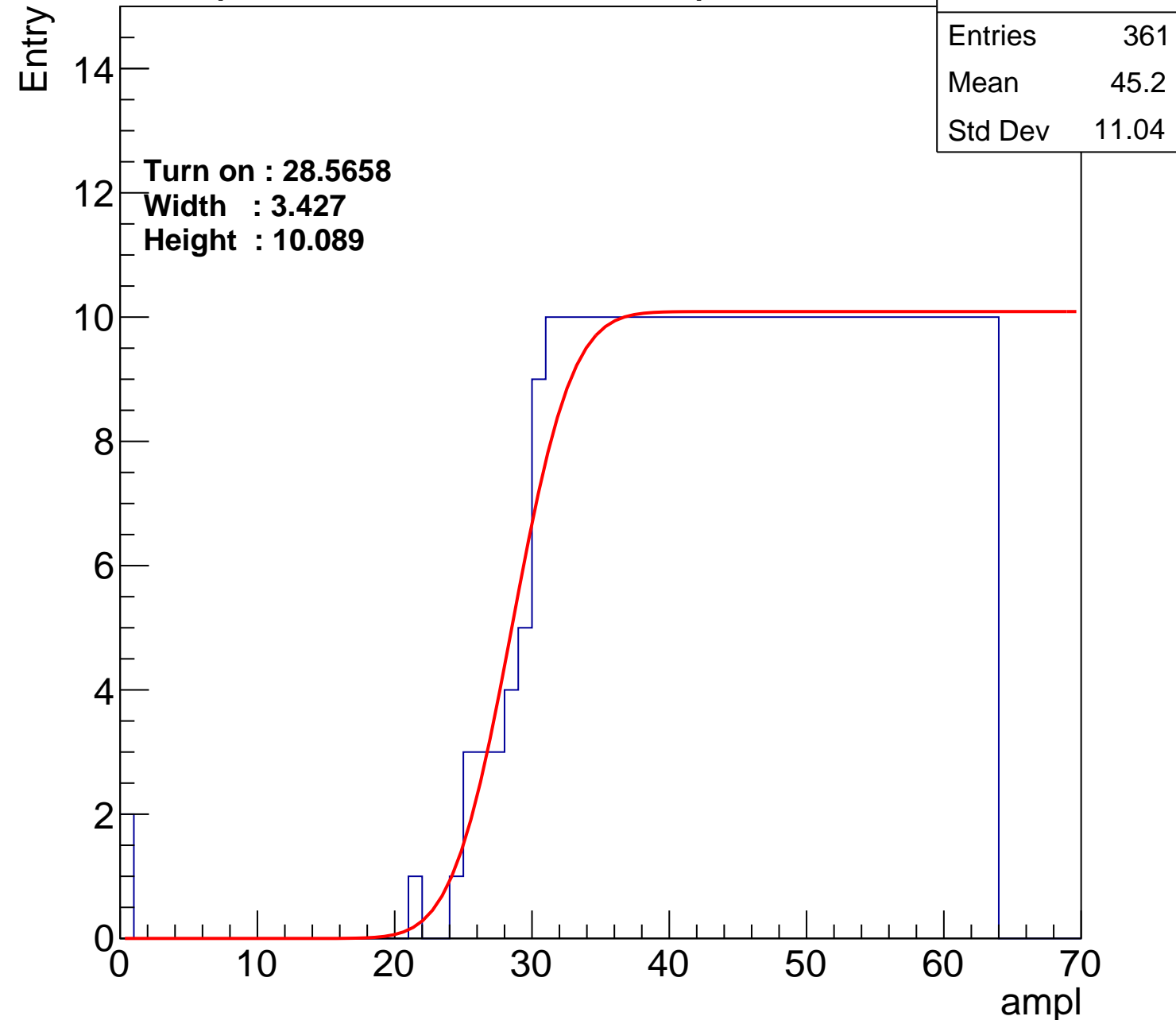
Width : 3.427

Height : 10.089

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch99

calib_packv5_042523_0143.root, FC#5, port B1

Entries	391
Mean	43.54
Std Dev	12.27

Turn on : 25.3181

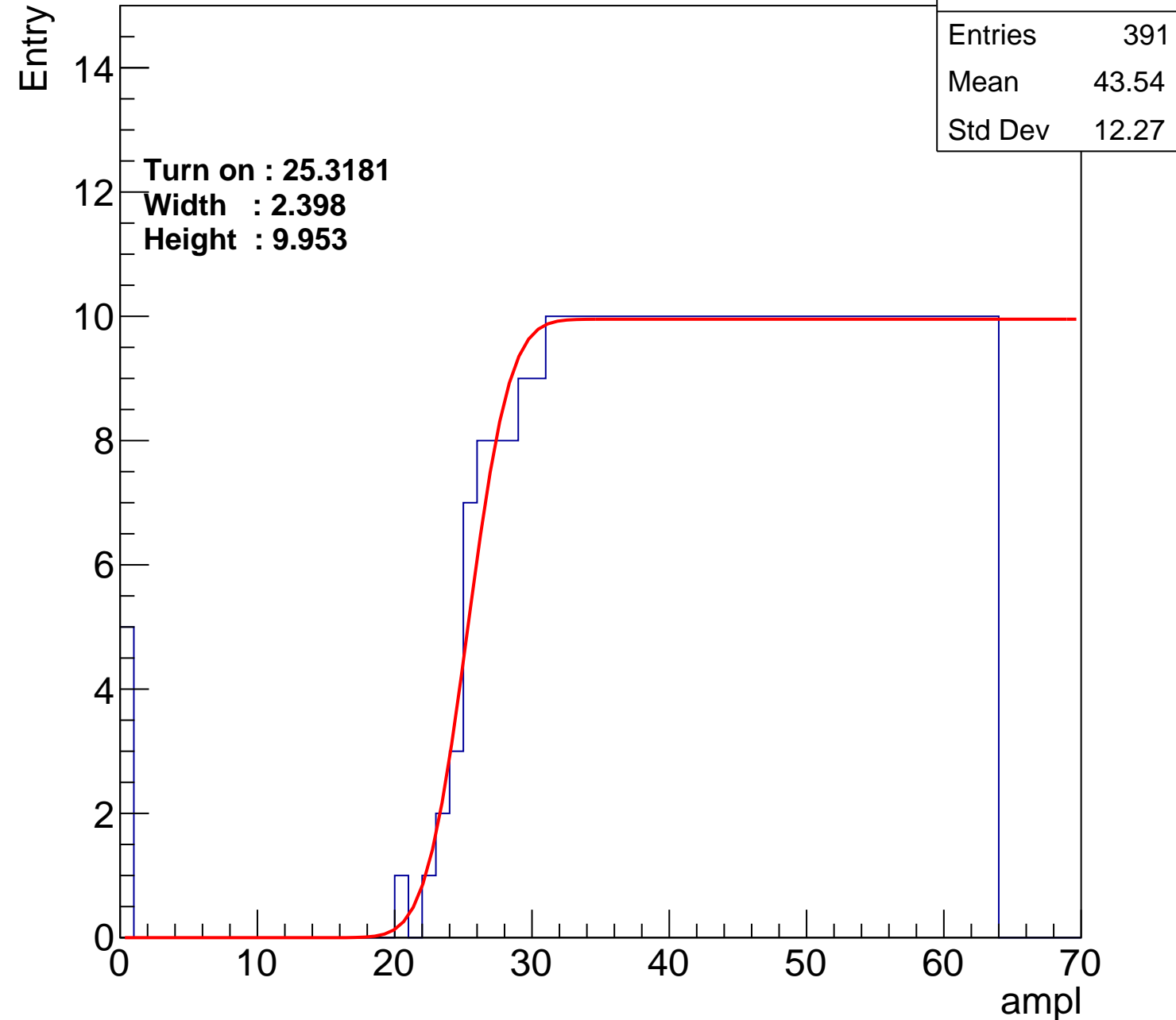
Width : 2.398

Height : 9.953

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch100

calib_packv5_042523_0143.root, FC#5, port B1

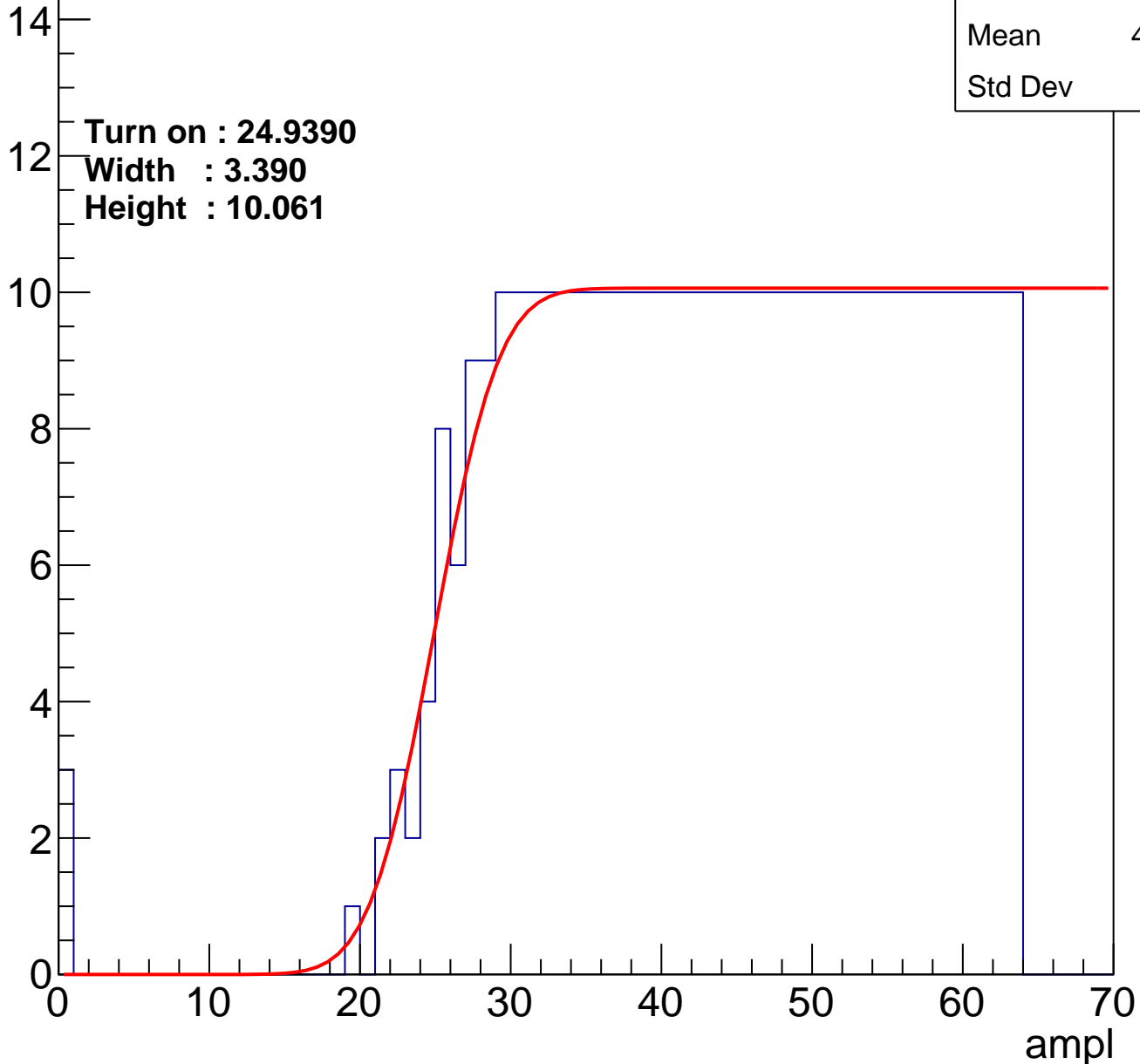
Entries	397
Mean	43.38
Std Dev	12.1

Turn on : 24.9390

Width : 3.390

Height : 10.061

Entry



B0L000S, U18-ch101

calib_packv5_042523_0143.root, FC#5, port B1

Entries	383
Mean	43.98
Std Dev	11.94

Turn on : 26.0248

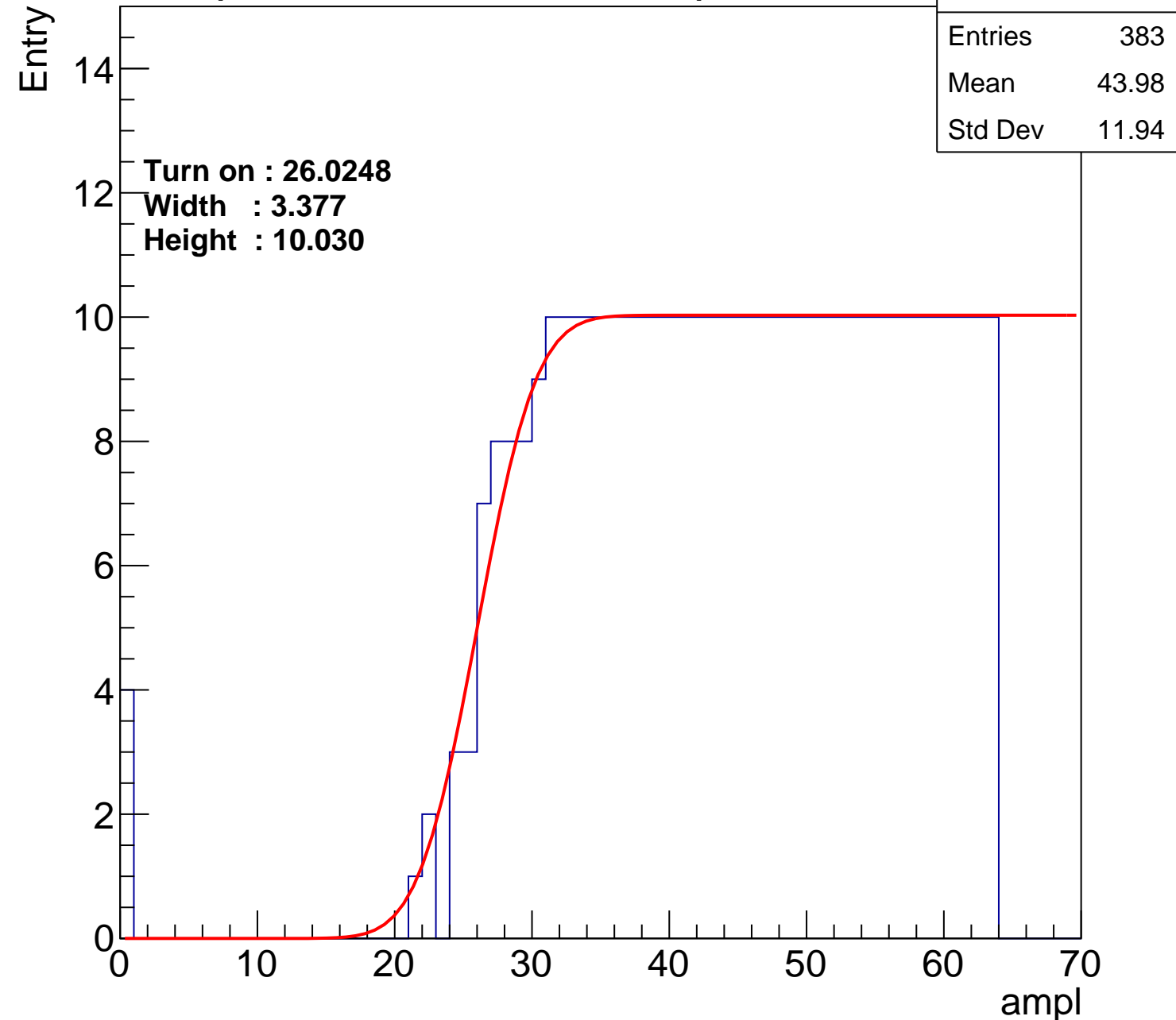
Width : 3.377

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch102

calib_packv5_042523_0143.root, FC#5, port B1

Entries	394
Mean	43.47
Std Dev	12.17

Turn on : 24.7615

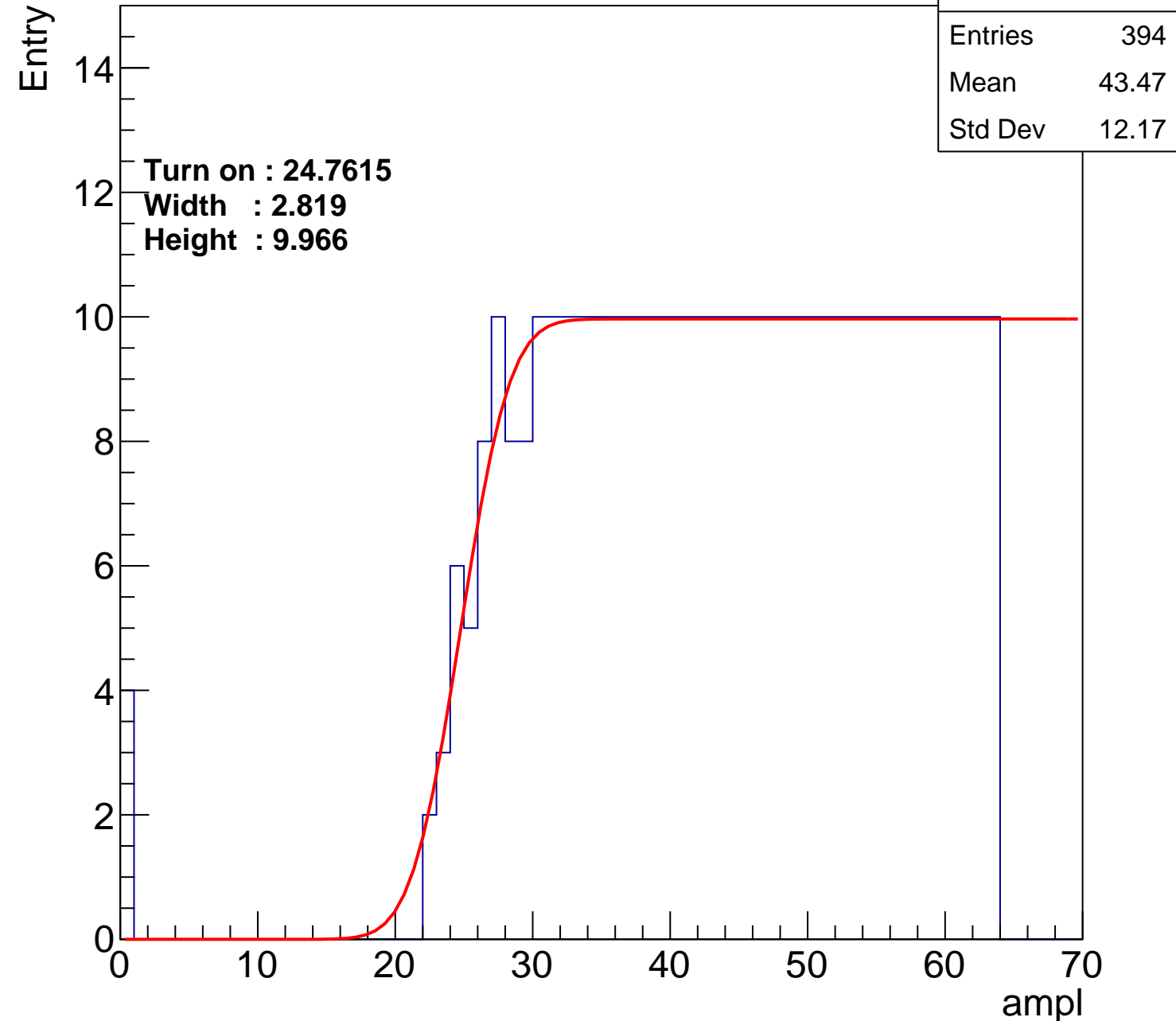
Width : 2.819

Height : 9.966

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch103

calib_packv5_042523_0143.root, FC#5, port B1

Entries	393
Mean	43.54
Std Dev	12.05

Turn on : 25.3384

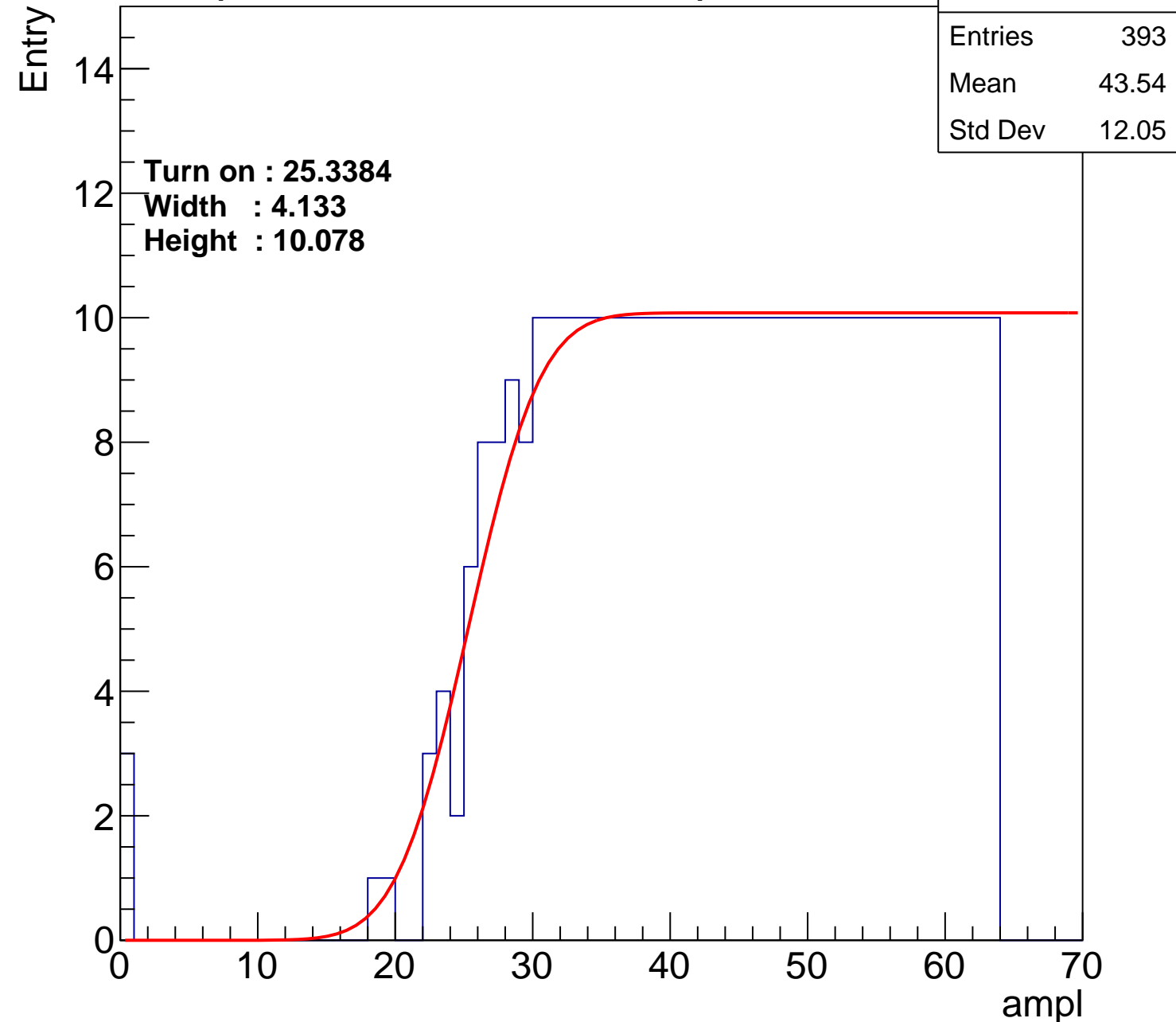
Width : 4.133

Height : 10.078

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch104

calib_packv5_042523_0143.root, FC#5, port B1

Entries	386
Mean	43.94
Std Dev	11.71

Turn on : 25.5997

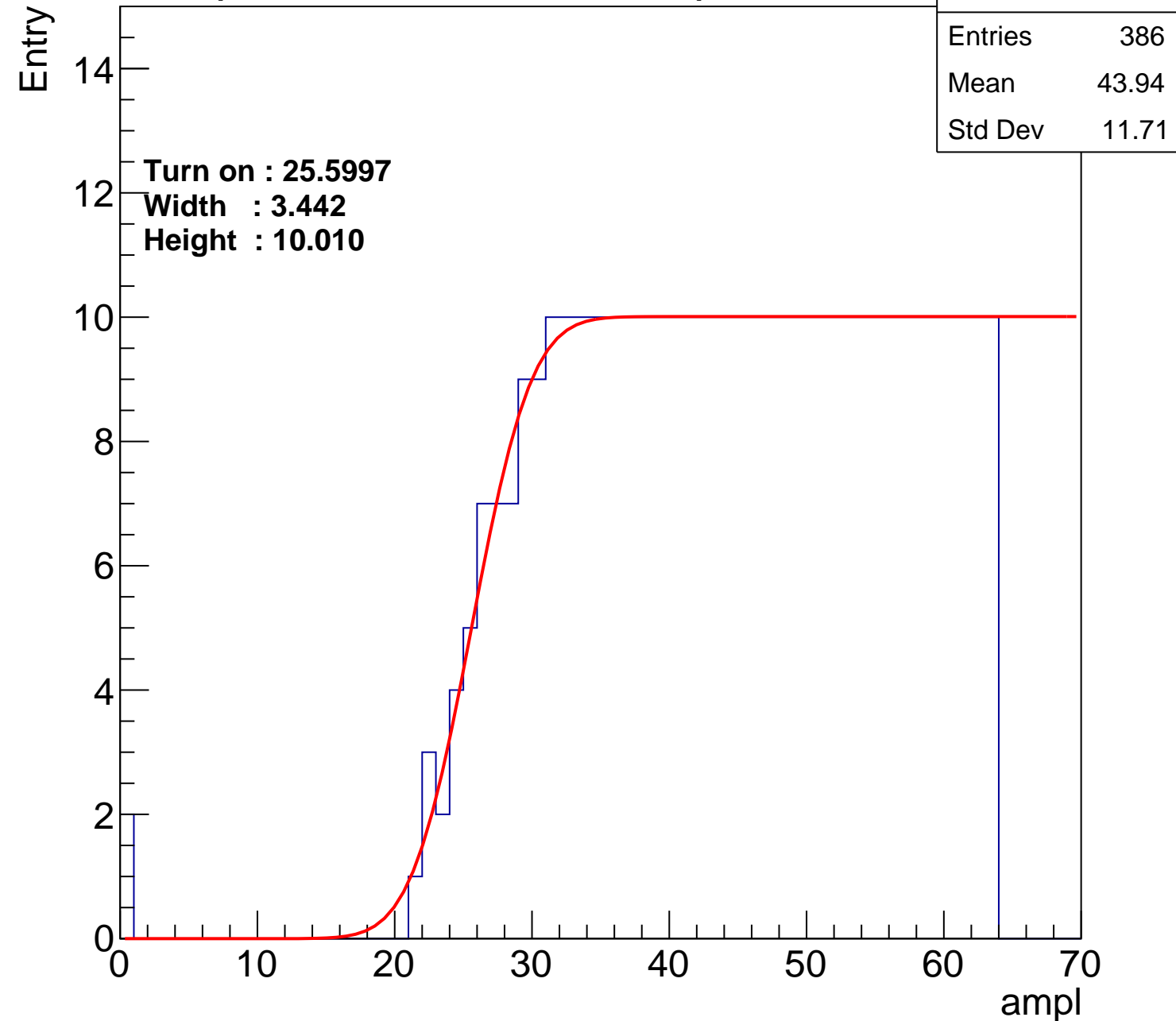
Width : 3.442

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch105

calib_packv5_042523_0143.root, FC#5, port B1

Entries	391
Mean	43.49
Std Dev	12.35

Turn on : 25.2331

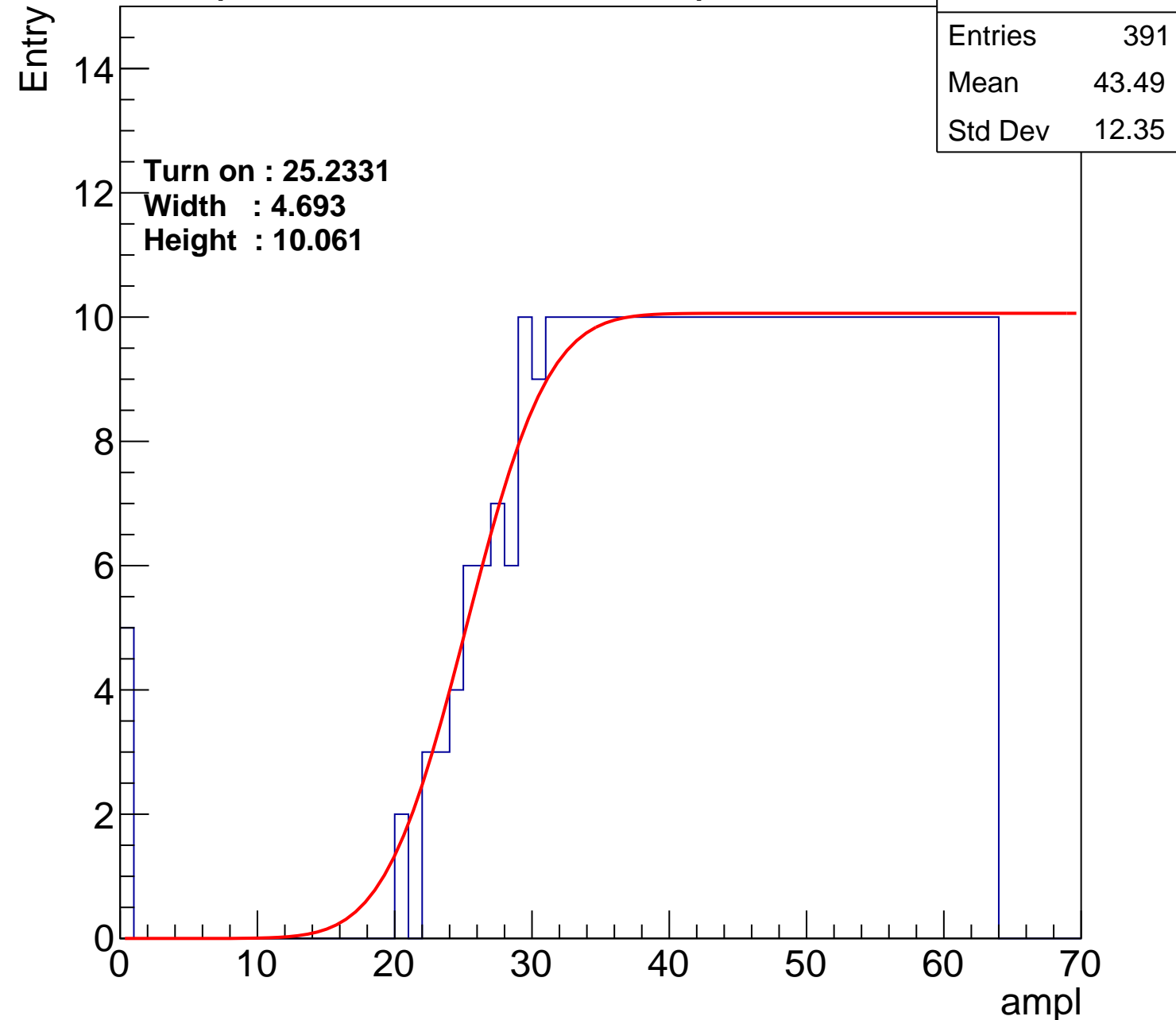
Width : 4.693

Height : 10.061

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch106

calib_packv5_042523_0143.root, FC#5, port B1

Entries	392
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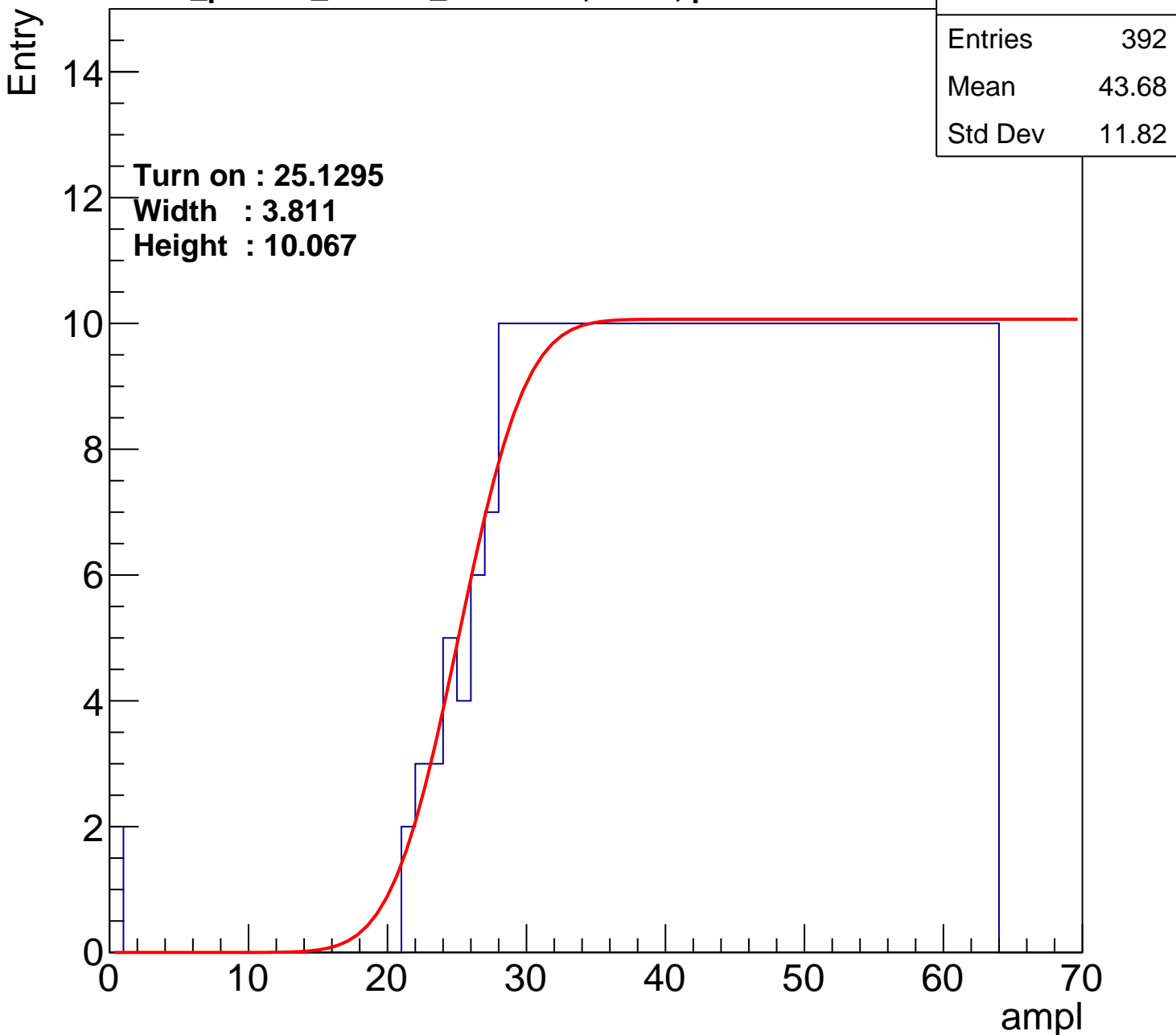
Mean	43.68
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Std Dev	11.82
---------	-------

Turn on : 25.1295

Width : 3.811

Height : 10.067



B0L000S, U18-ch107

calib_packv5_042523_0143.root, FC#5, port B1

Entries	367
Mean	44.84
Std Dev	11.37

Turn on : 27.8146

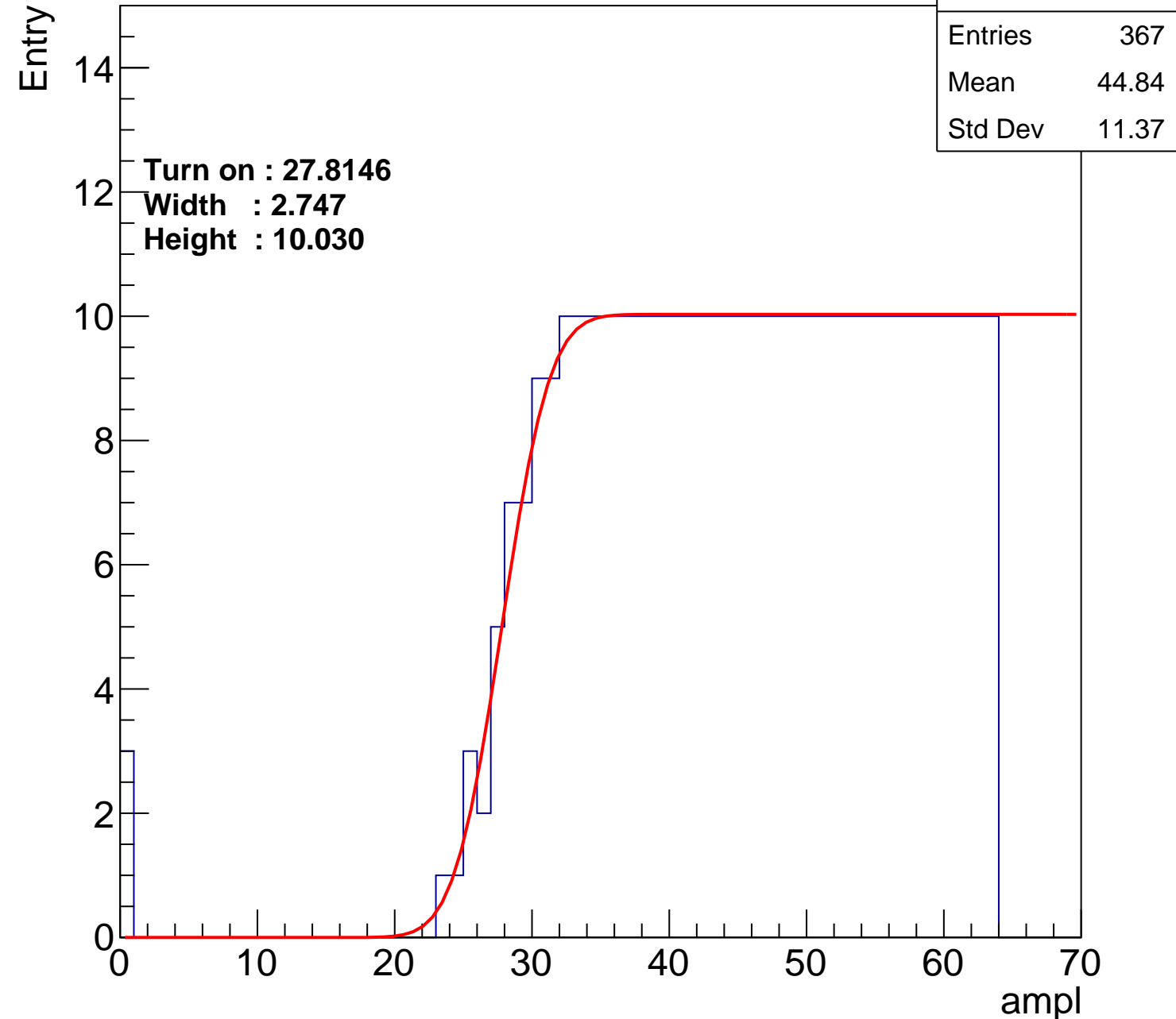
Width : 2.747

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch108

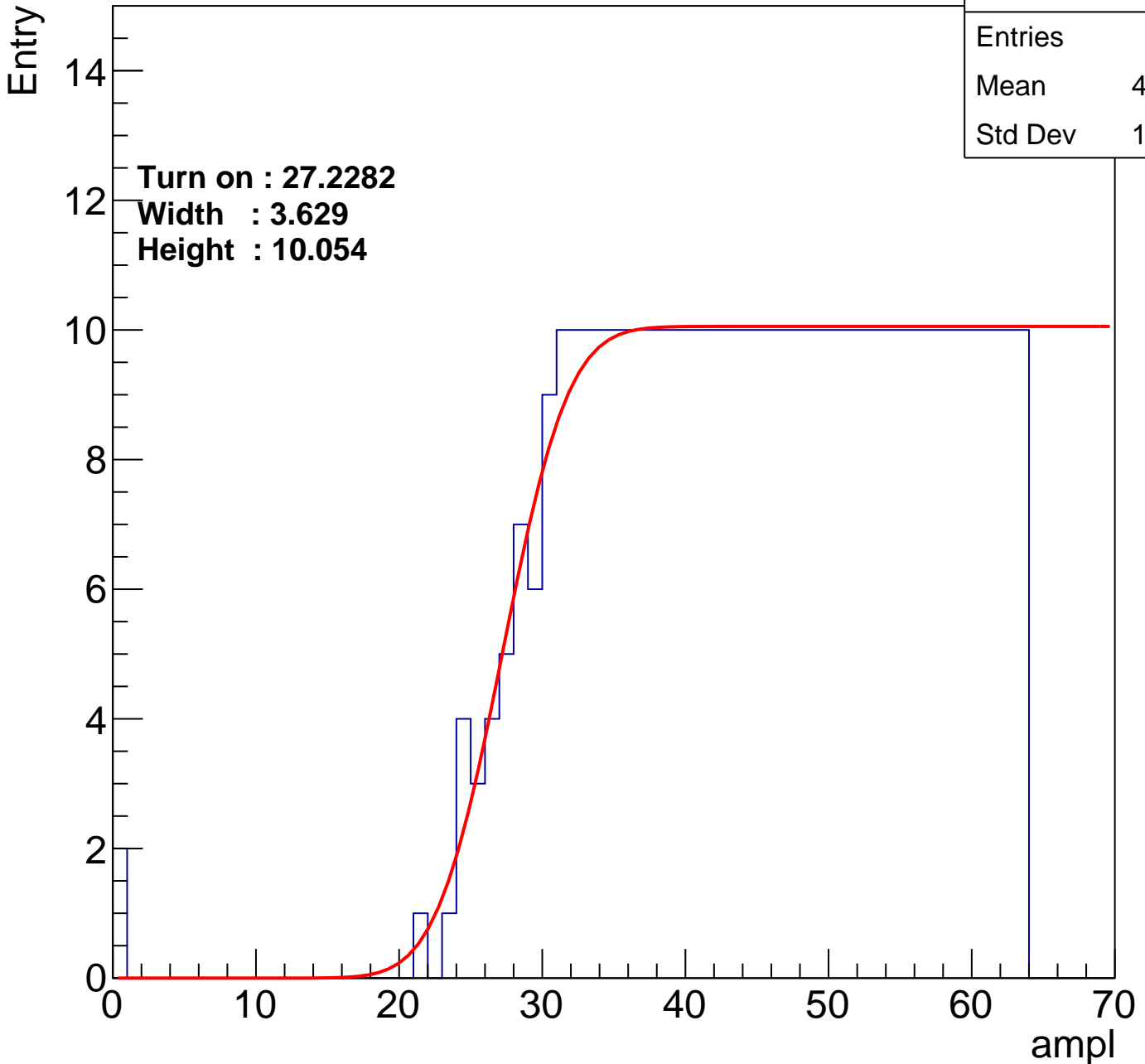
calib_packv5_042523_0143.root, FC#5, port B1

Entries	372
Mean	44.63
Std Dev	11.35

Turn on : 27.2282

Width : 3.629

Height : 10.054



B0L000S, U18-ch109

calib_packv5_042523_0143.root, FC#5, port B1

Entries	369
Mean	44.82
Std Dev	11.22

Turn on : 28.1868

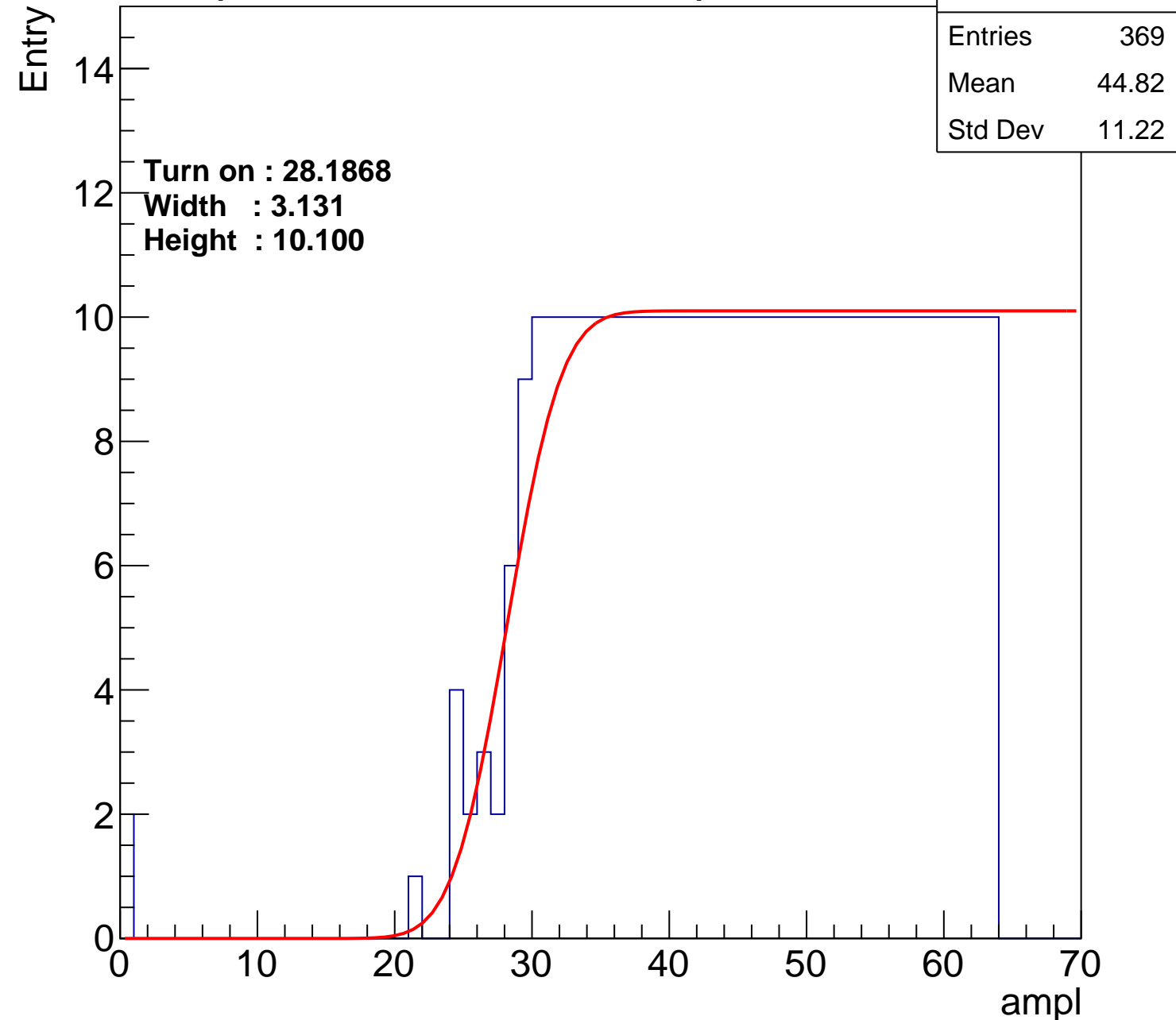
Width : 3.131

Height : 10.100

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch110

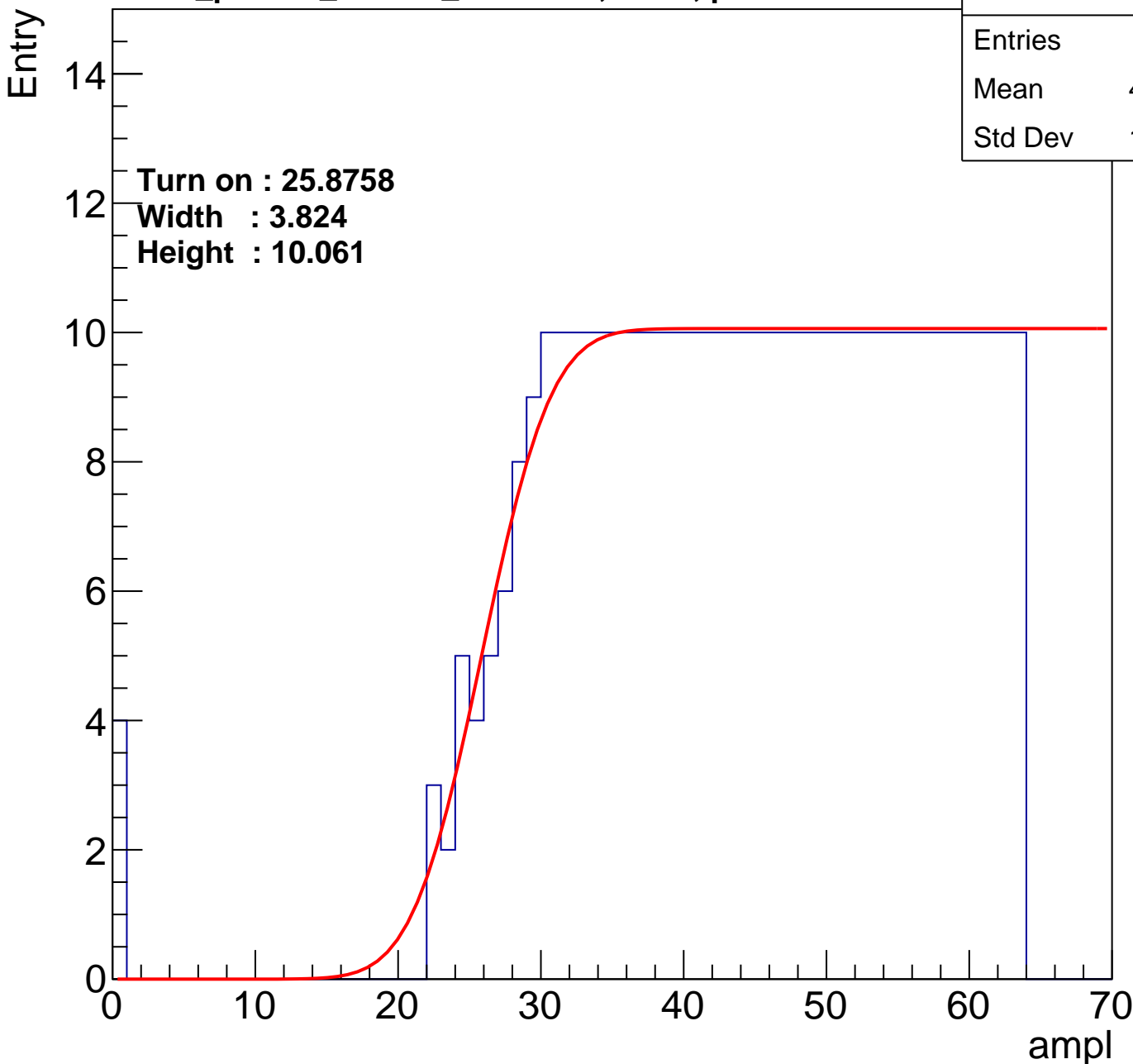
calib_packv5_042523_0143.root, FC#5, port B1

Entries	386
Mean	43.83
Std Dev	12.02

Turn on : 25.8758

Width : 3.824

Height : 10.061



B0L000S, U18-ch111

calib_packv5_042523_0143.root, FC#5, port B1

Entries	366
Mean	44.92
Std Dev	11.3

Turn on : 27.4533

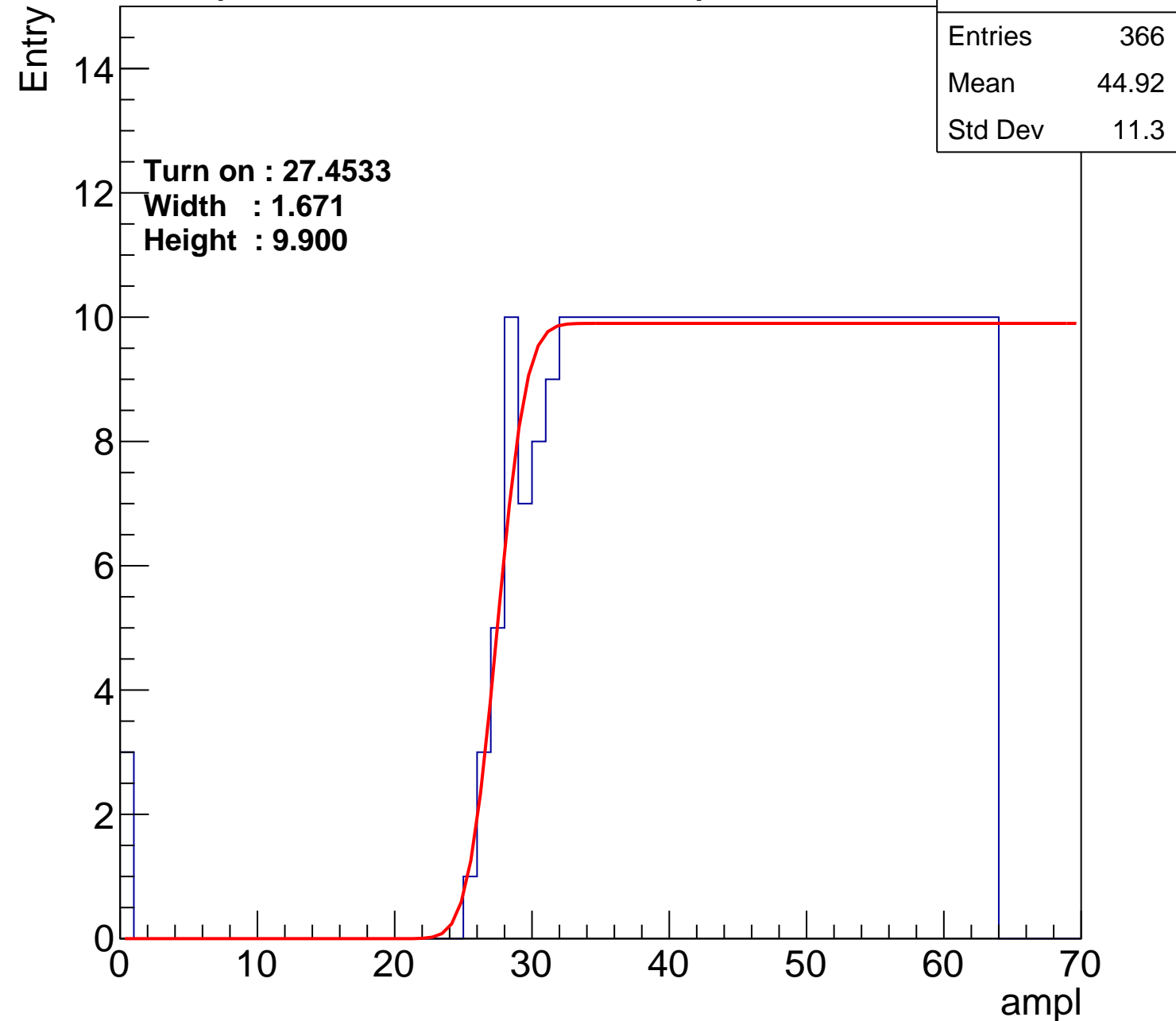
Width : 1.671

Height : 9.900

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch112

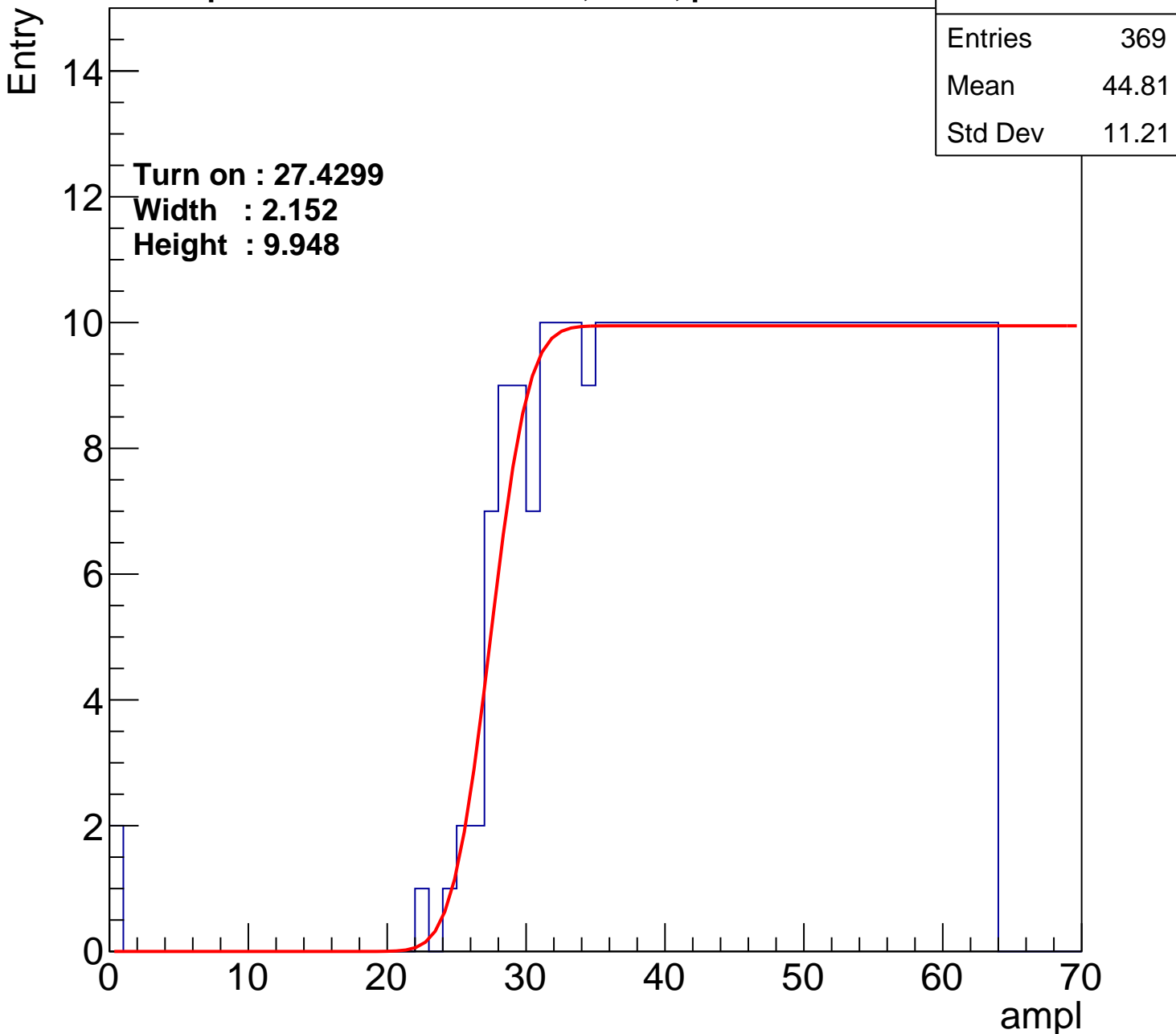
calib_packv5_042523_0143.root, FC#5, port B1

Turn on : 27.4299

Width : 2.152

Height : 9.948

Entries	369
Mean	44.81
Std Dev	11.21



B0L000S, U18-ch113

calib_packv5_042523_0143.root, FC#5, port B1

Entries	376
Mean	44.37
Std Dev	11.63

Turn on : 26.8693

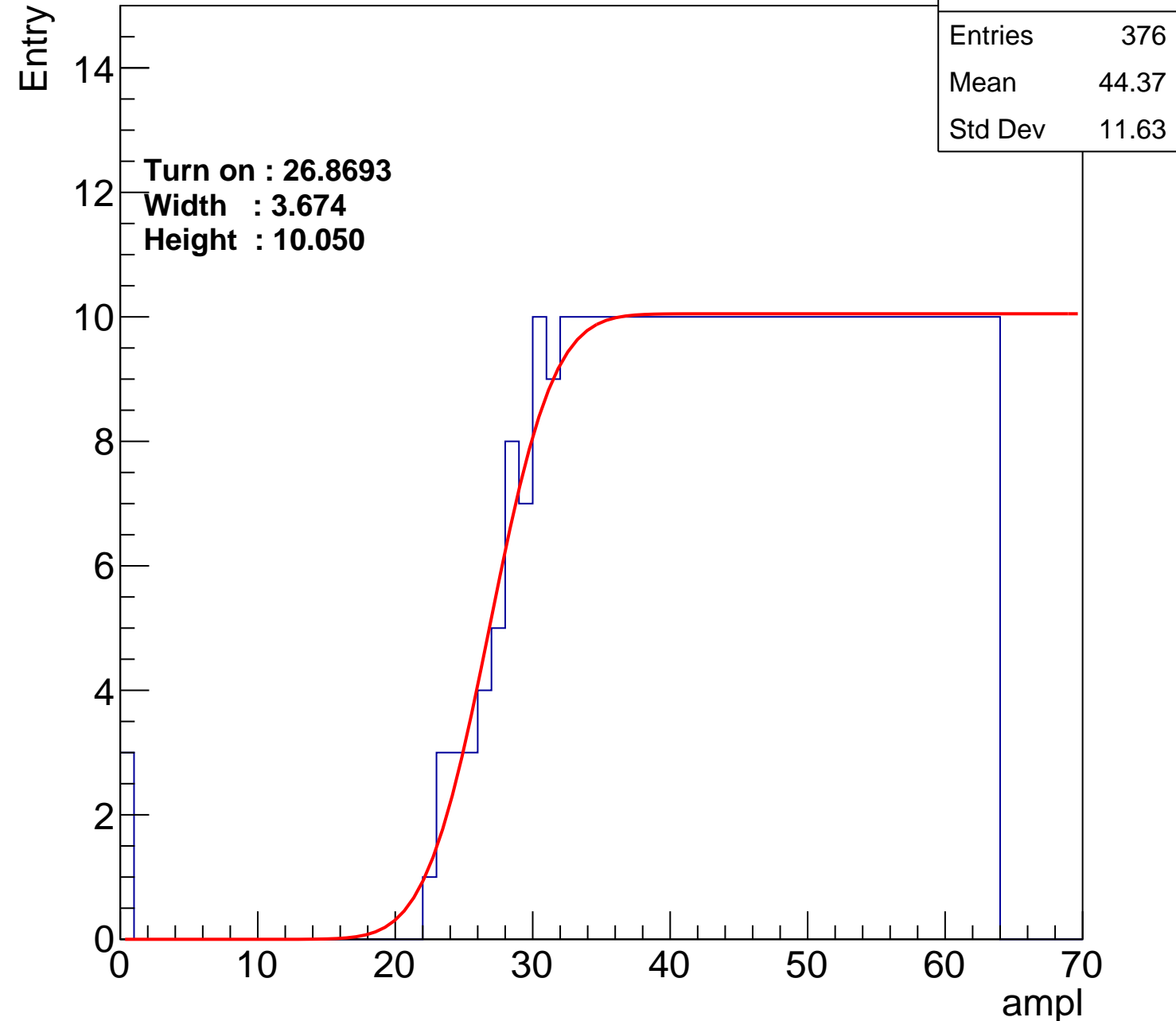
Width : 3.674

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch114

calib_packv5_042523_0143.root, FC#5, port B1

Entries	365
Mean	45.03
Std Dev	11.08

Turn on : 27.2245

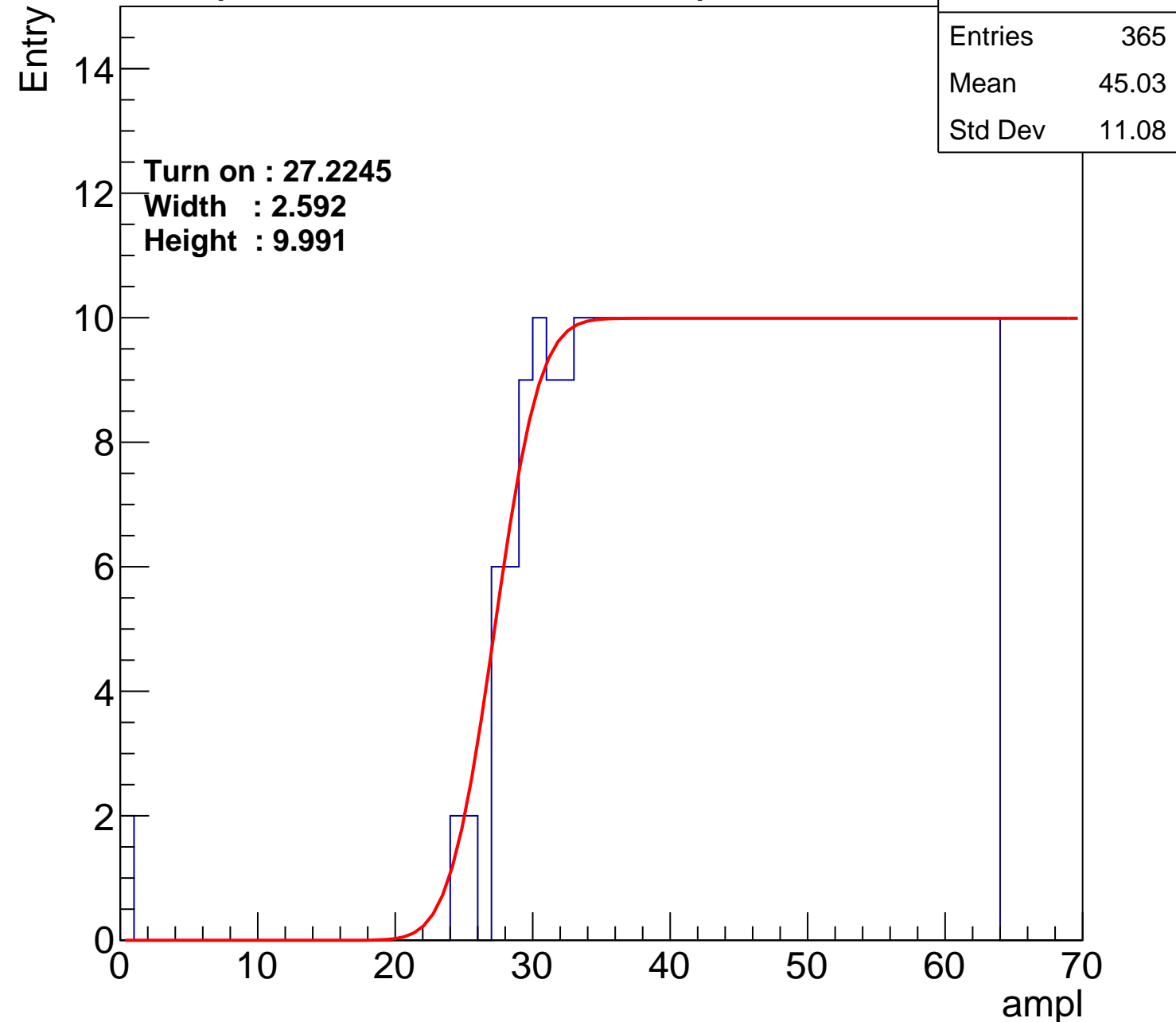
Width : 2.592

Height : 9.991

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch115

calib_packv5_042523_0143.root, FC#5, port B1

Entries	385
Mean	44.1
Std Dev	11.44

Turn on : 25.8486

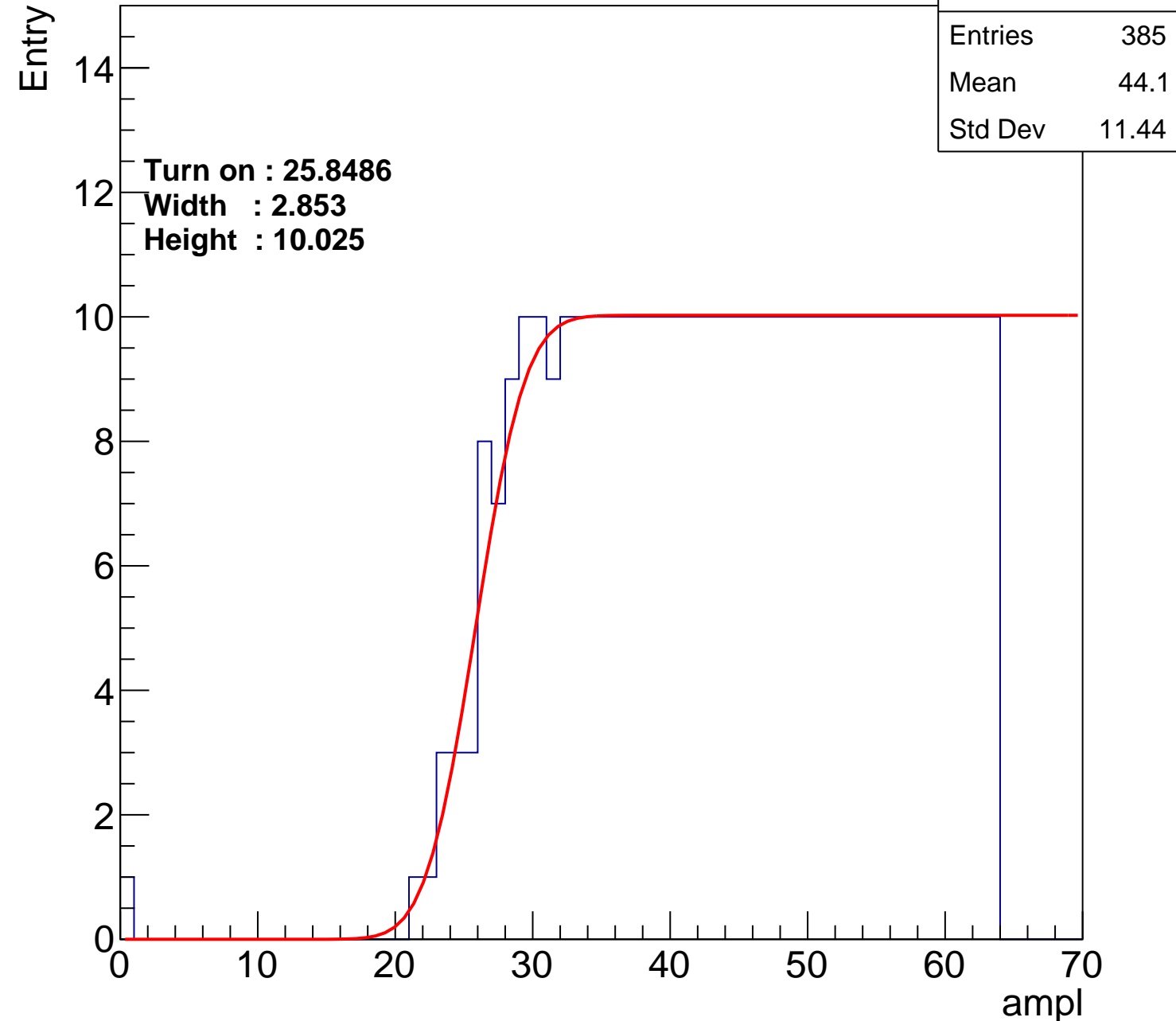
Width : 2.853

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch116

calib_packv5_042523_0143.root, FC#5, port B1

Entries	394
Mean	43.62
Std Dev	11.82

Turn on : 24.5541

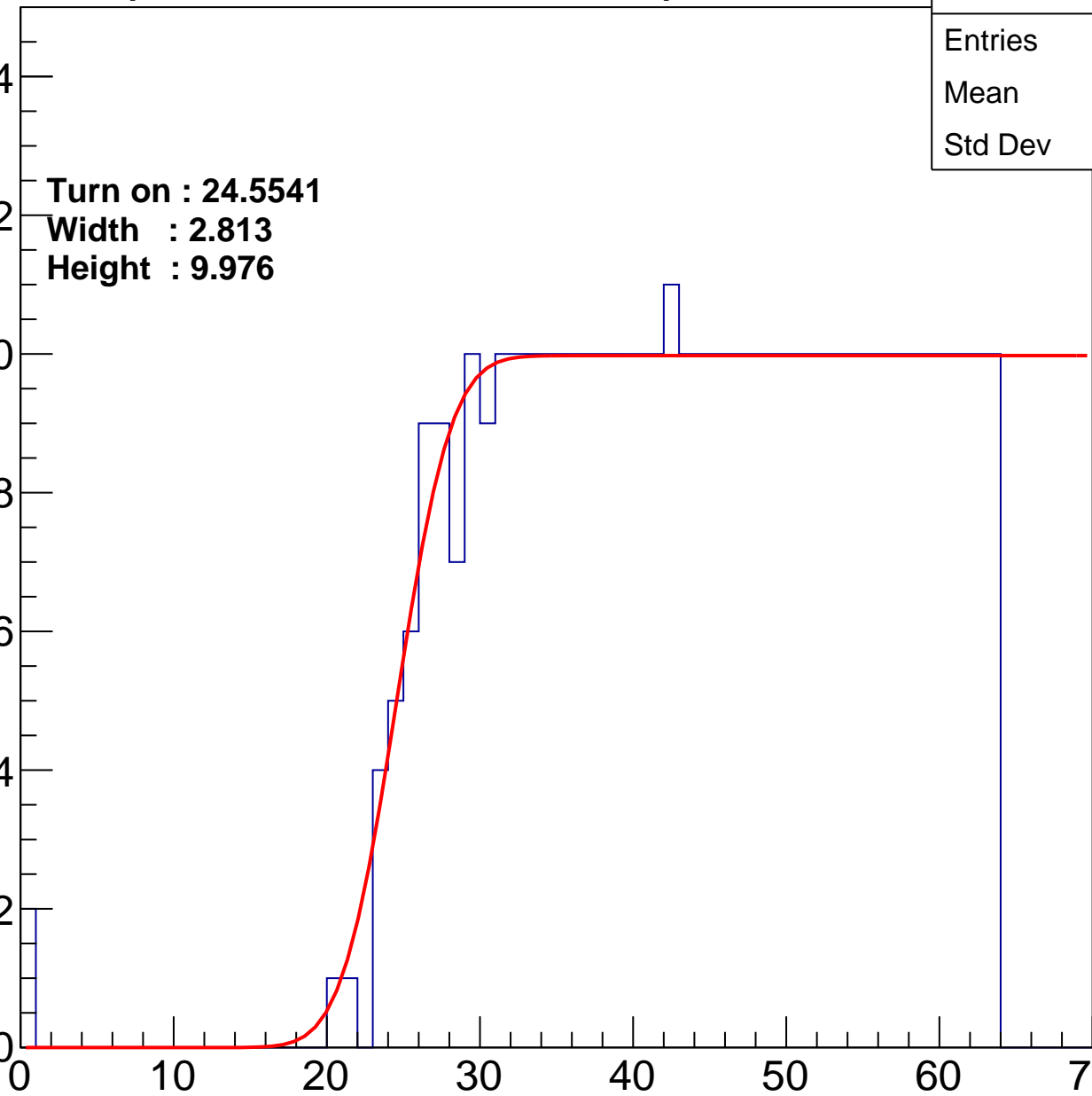
Width : 2.813

Height : 9.976

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch117

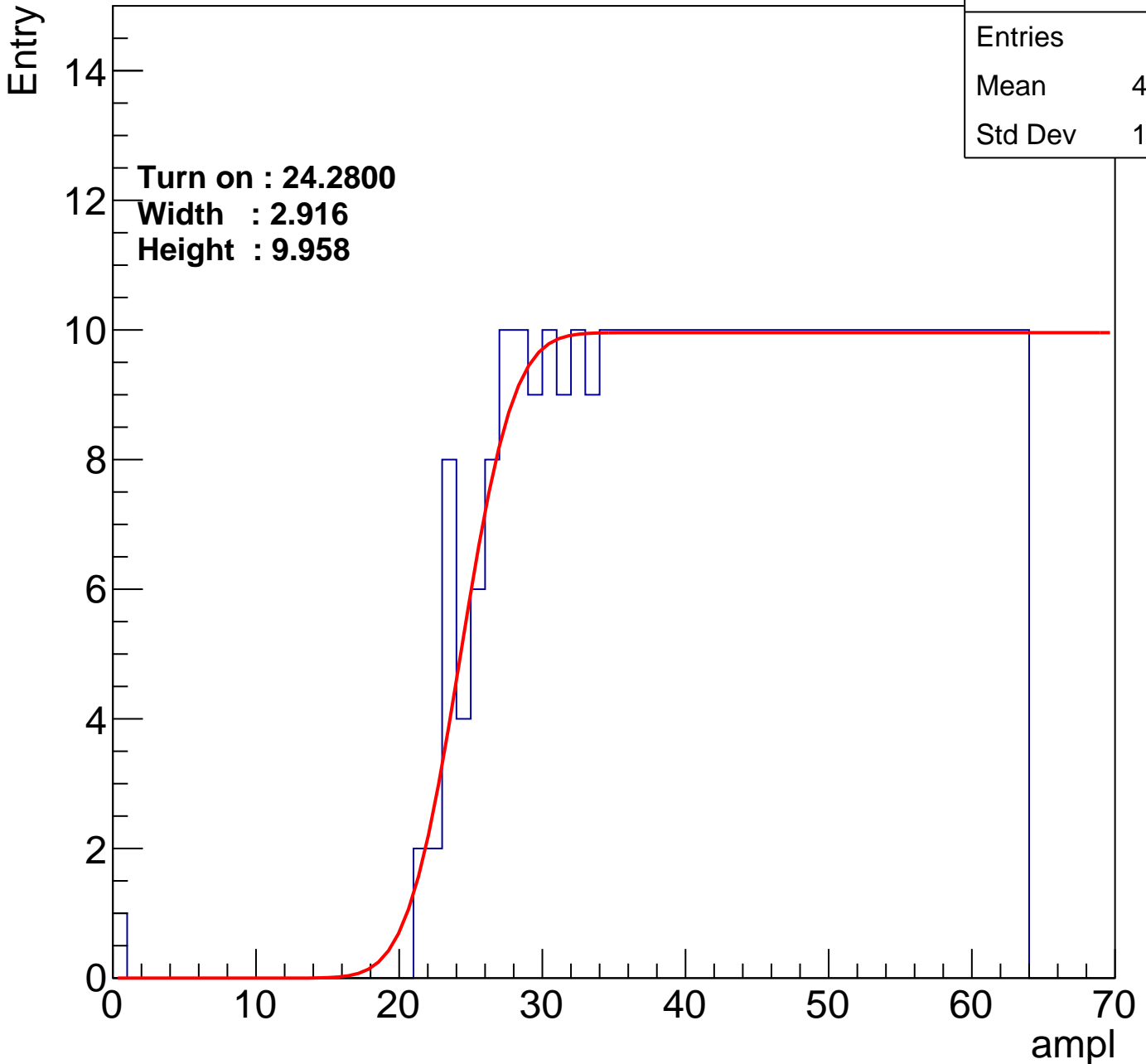
calib_packv5_042523_0143.root, FC#5, port B1

Entries	398
Mean	43.42
Std Dev	11.84

Turn on : 24.2800

Width : 2.916

Height : 9.958



B0L000S, U18-ch118

calib_packv5_042523_0143.root, FC#5, port B1

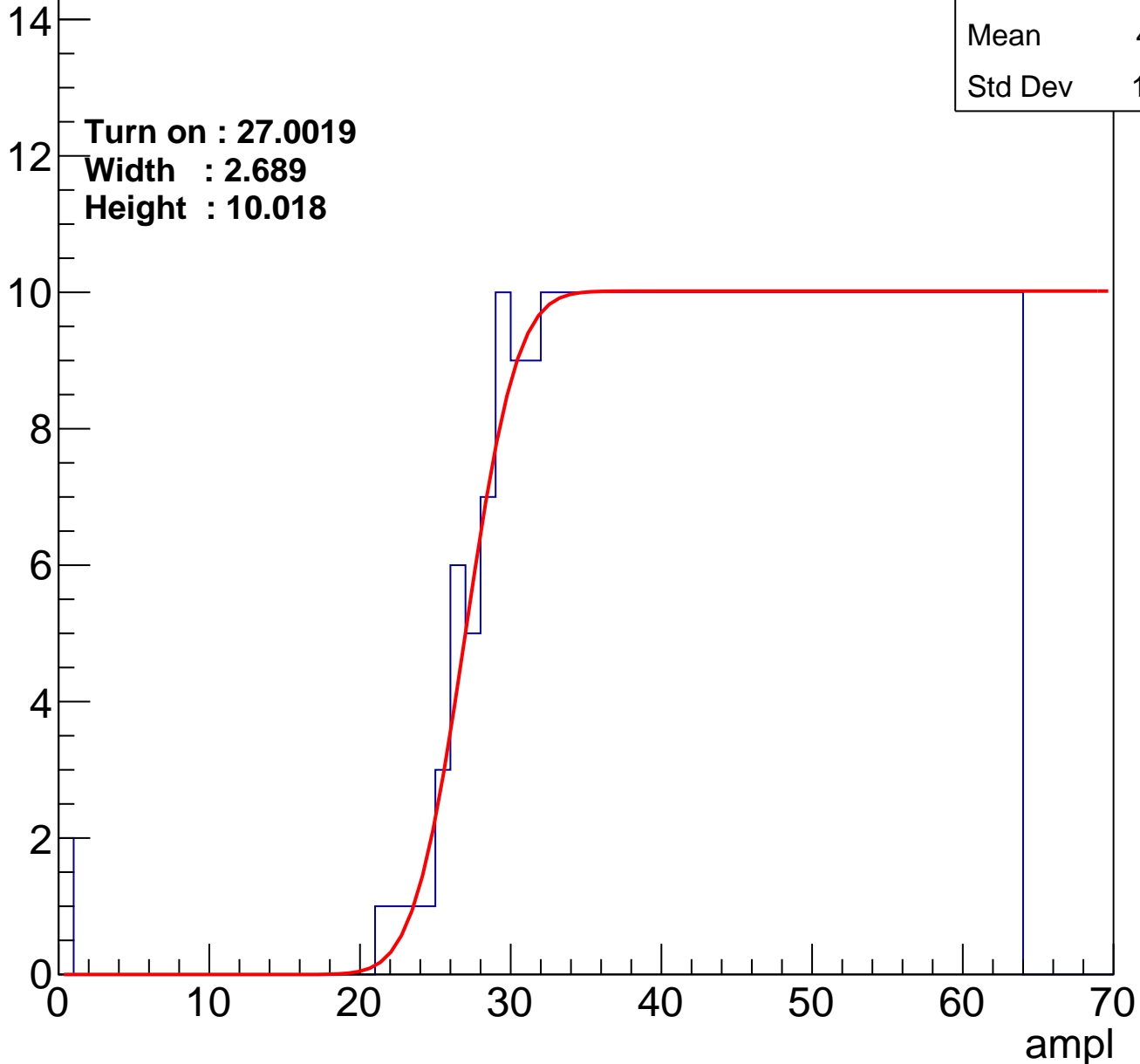
Entries	375
Mean	44.51
Std Dev	11.39

Turn on : 27.0019

Width : 2.689

Height : 10.018

Entry



B0L000S, U18-ch119

calib_packv5_042523_0143.root, FC#5, port B1

Entries	364
Mean	44.88
Std Dev	11.56

Turn on : 28.5417

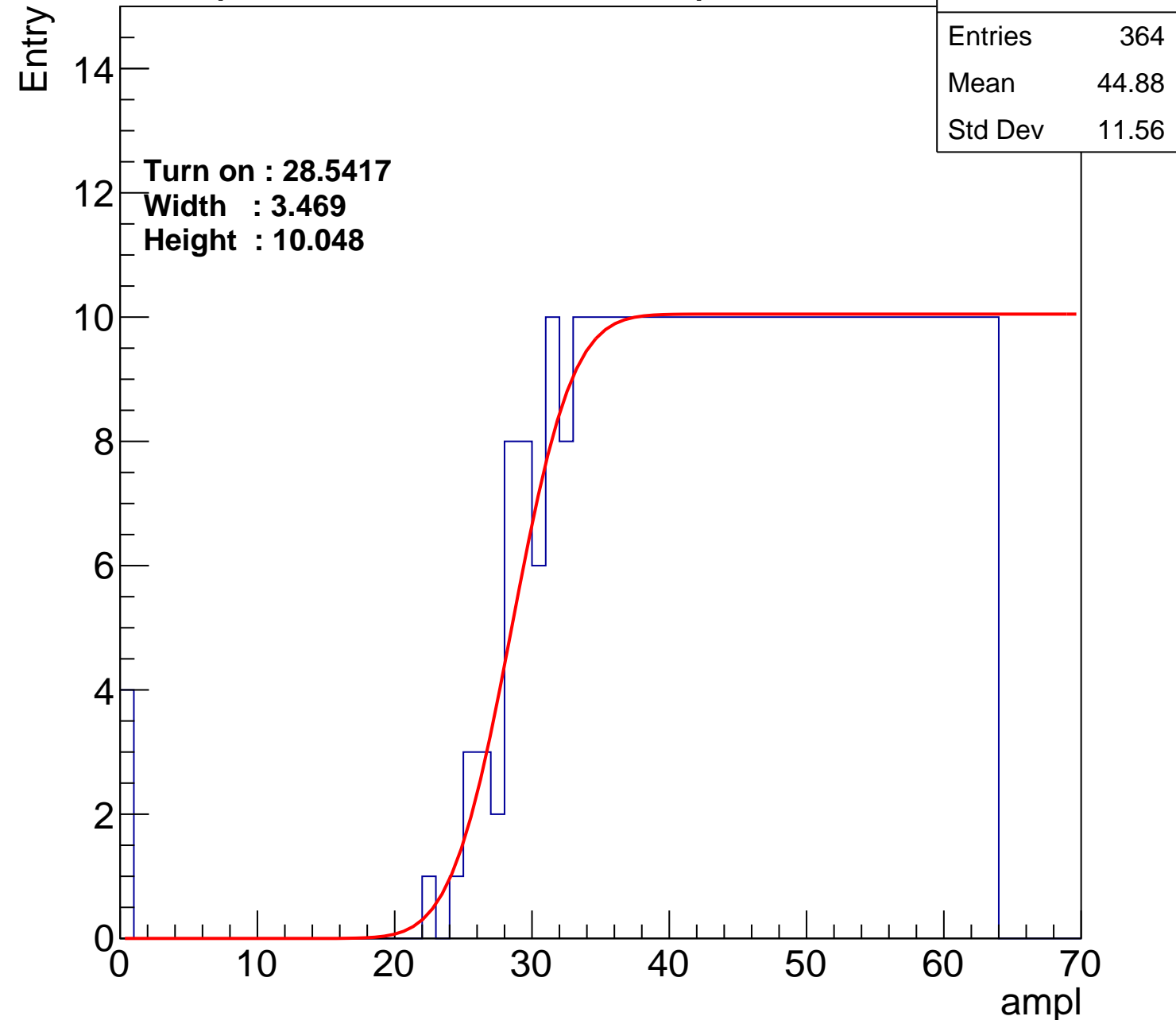
Width : 3.469

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch120

calib_packv5_042523_0143.root, FC#5, port B1

Entries	362
Mean	45.19
Std Dev	10.9

Turn on : 28.5334

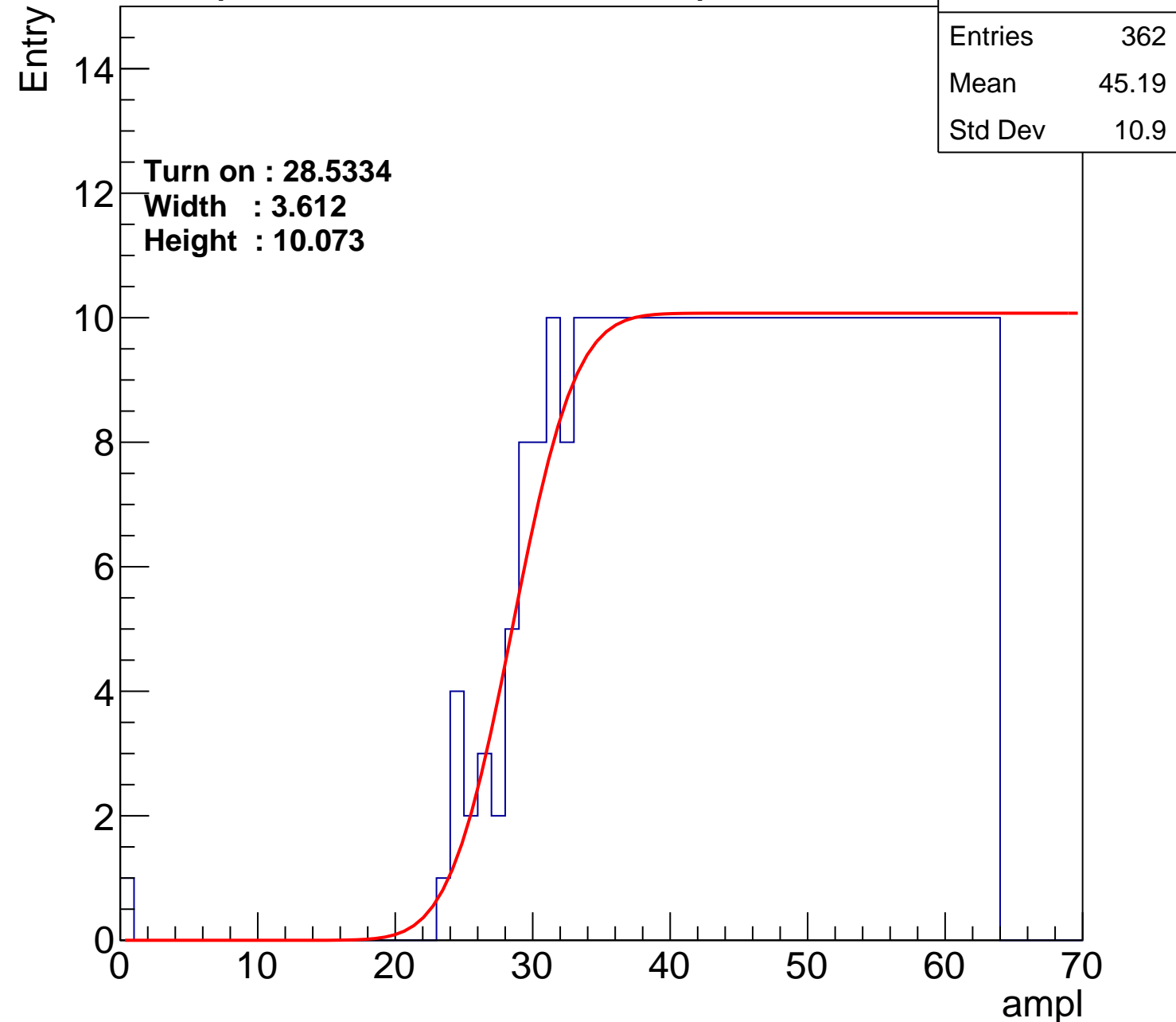
Width : 3.612

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch121

calib_packv5_042523_0143.root, FC#5, port B1

Entries	379
Mean	44.31
Std Dev	11.58

Turn on : 26.0743

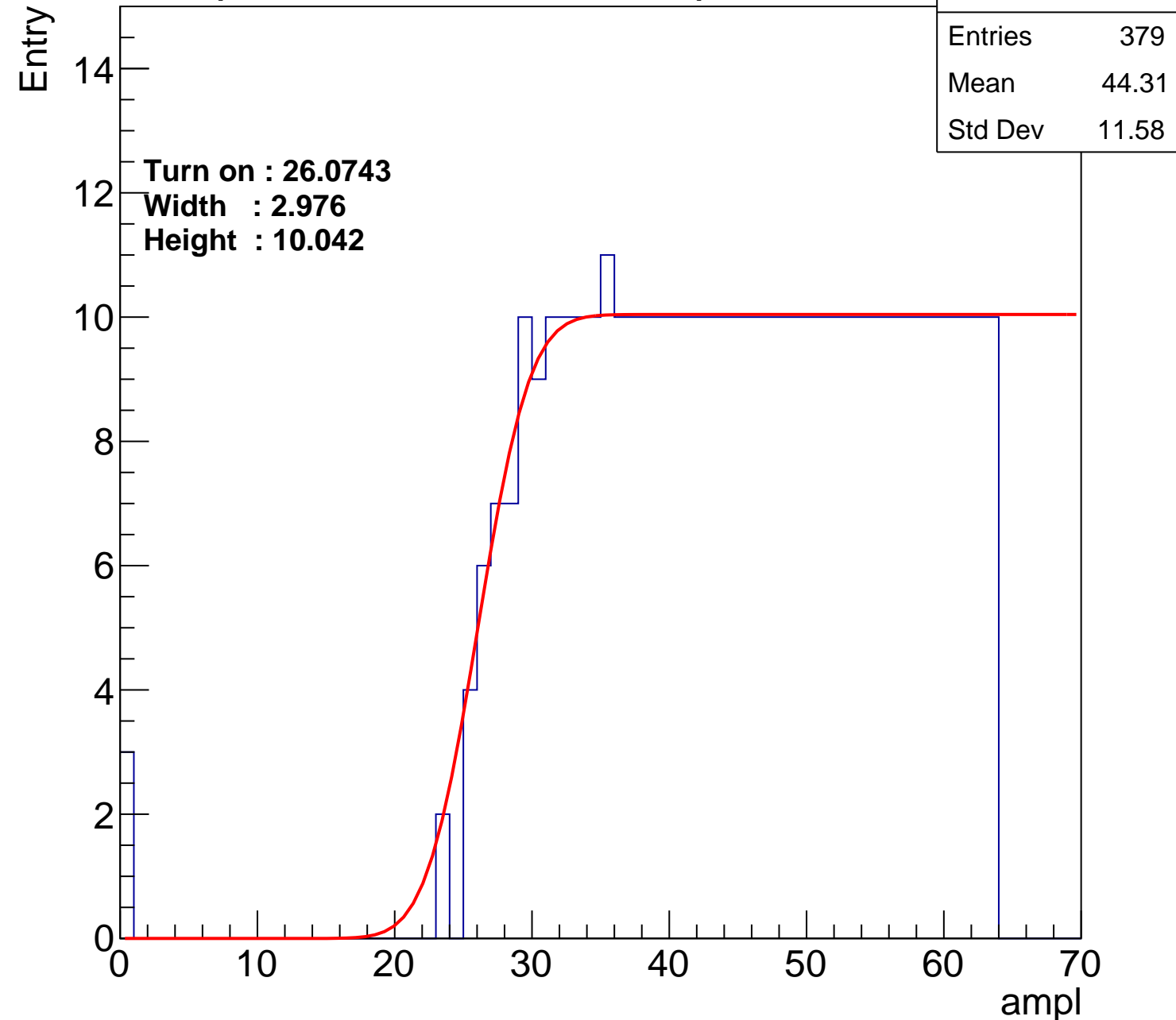
Width : 2.976

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch122

calib_packv5_042523_0143.root, FC#5, port B1

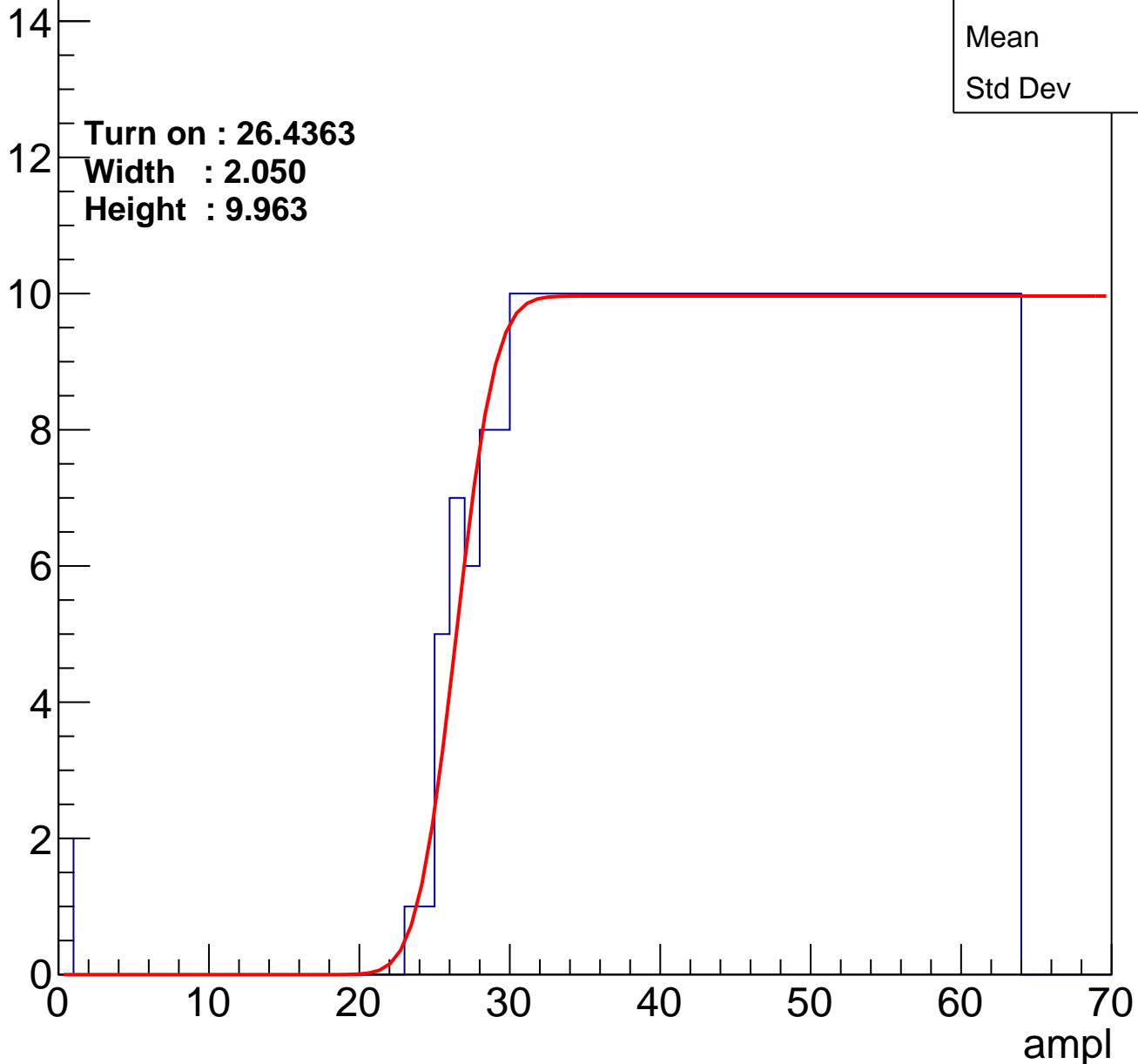
Entries	378
Mean	44.4
Std Dev	11.4

Turn on : 26.4363

Width : 2.050

Height : 9.963

Entry



B0L000S, U18-ch123

calib_packv5_042523_0143.root, FC#5, port B1

Entries	359
Mean	45.24
Std Dev	11.17

Turn on : 28.2783

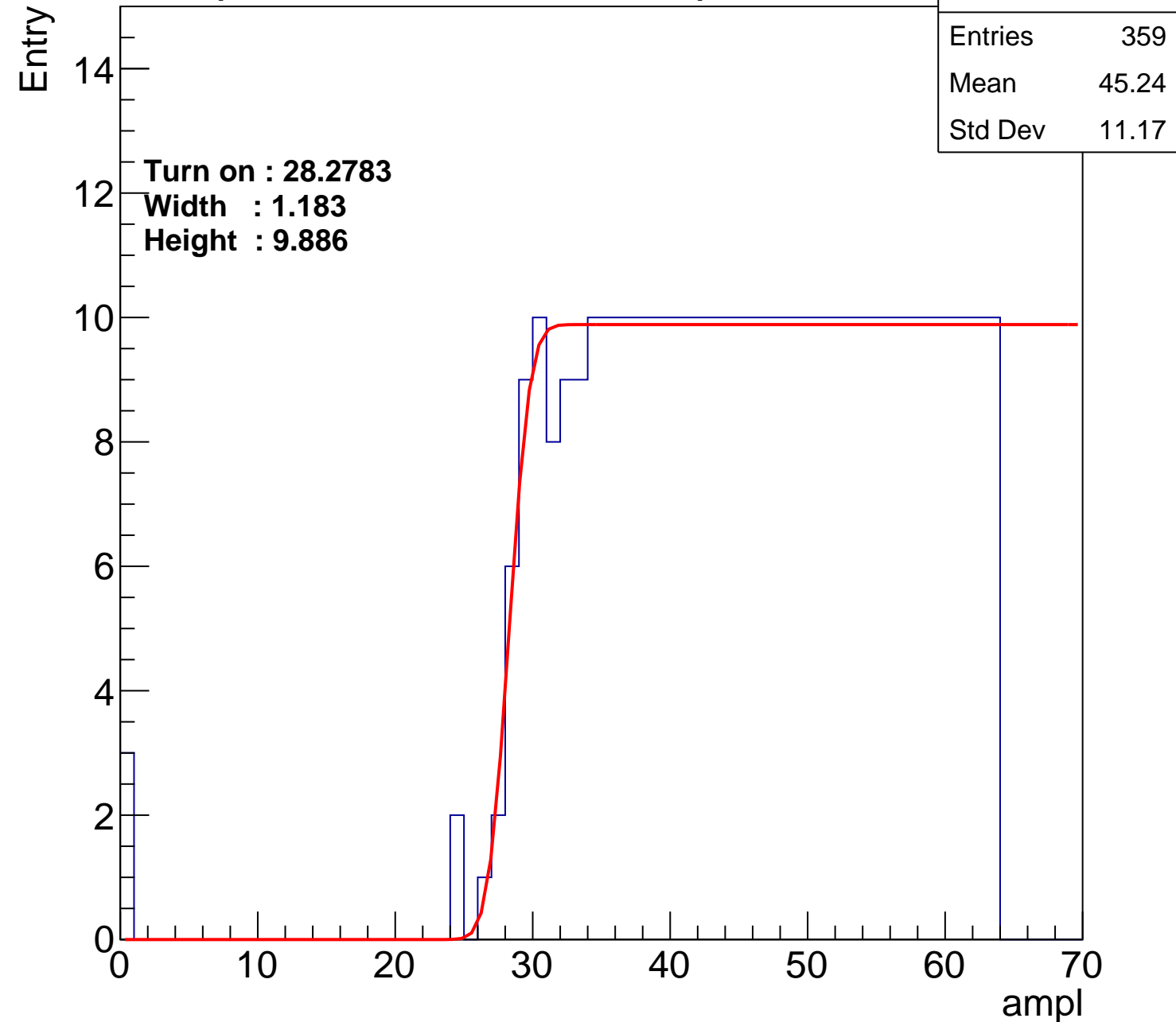
Width : 1.183

Height : 9.886

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch124

calib_packv5_042523_0143.root, FC#5, port B1

Entries	378
Mean	44.29
Std Dev	11.64

Turn on : 26.3989

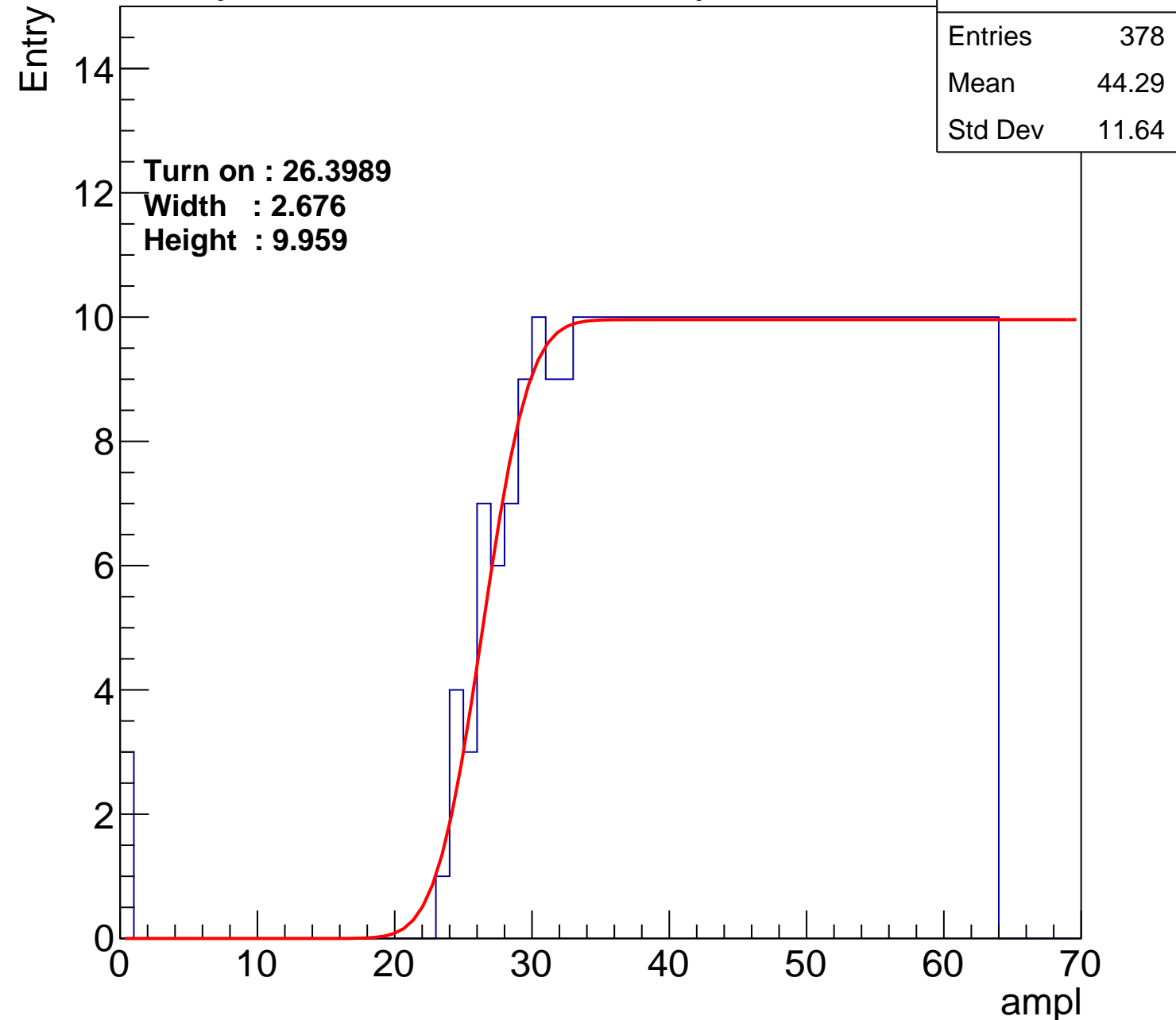
Width : 2.676

Height : 9.959

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch125

calib_packv5_042523_0143.root, FC#5, port B1

Entries	375
Mean	44.39
Std Dev	11.67

Turn on : 27.7141

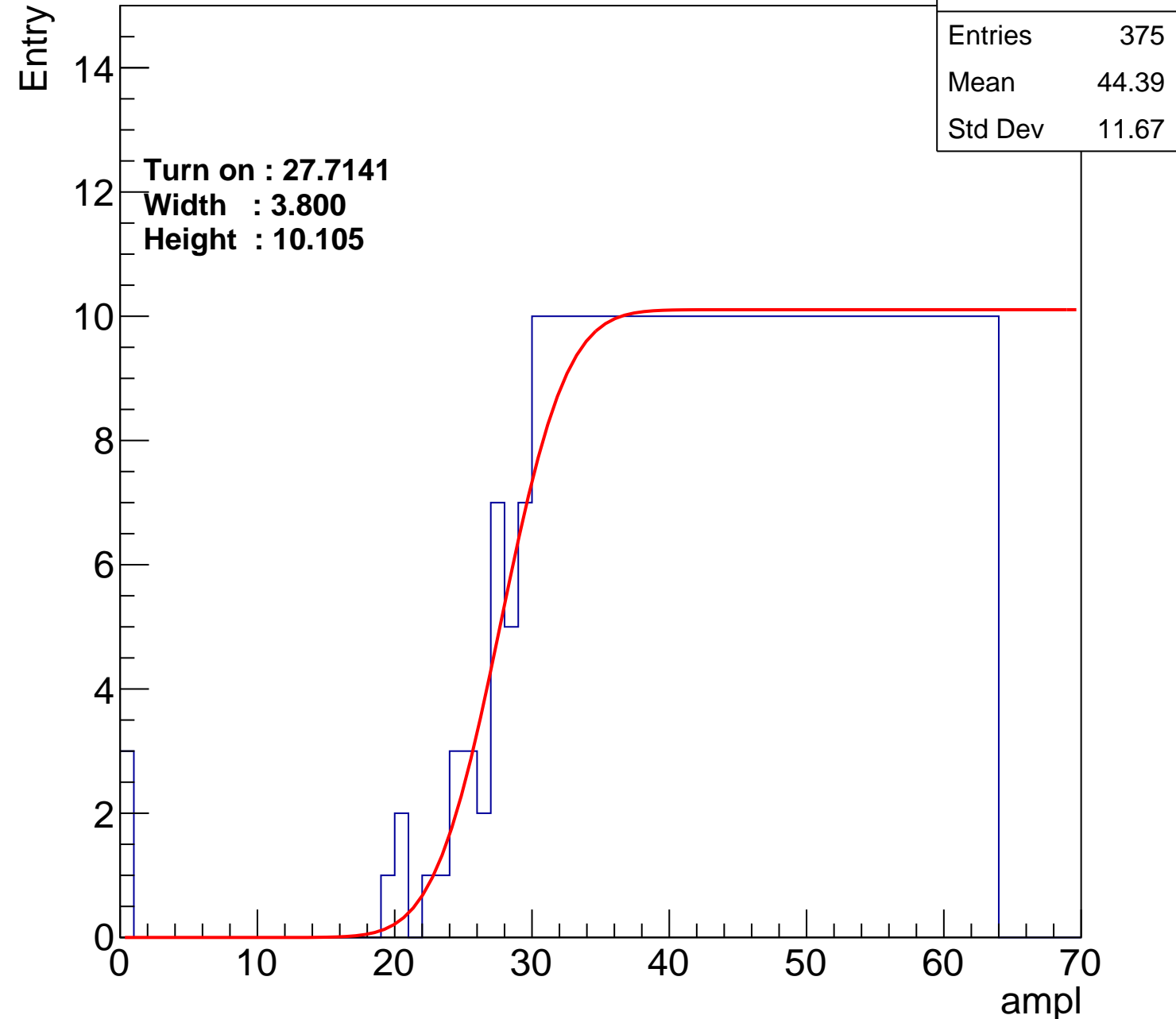
Width : 3.800

Height : 10.105

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch126

calib_packv5_042523_0143.root, FC#5, port B1

Entries	372
Mean	44.67
Std Dev	11.28

Turn on : 27.2740

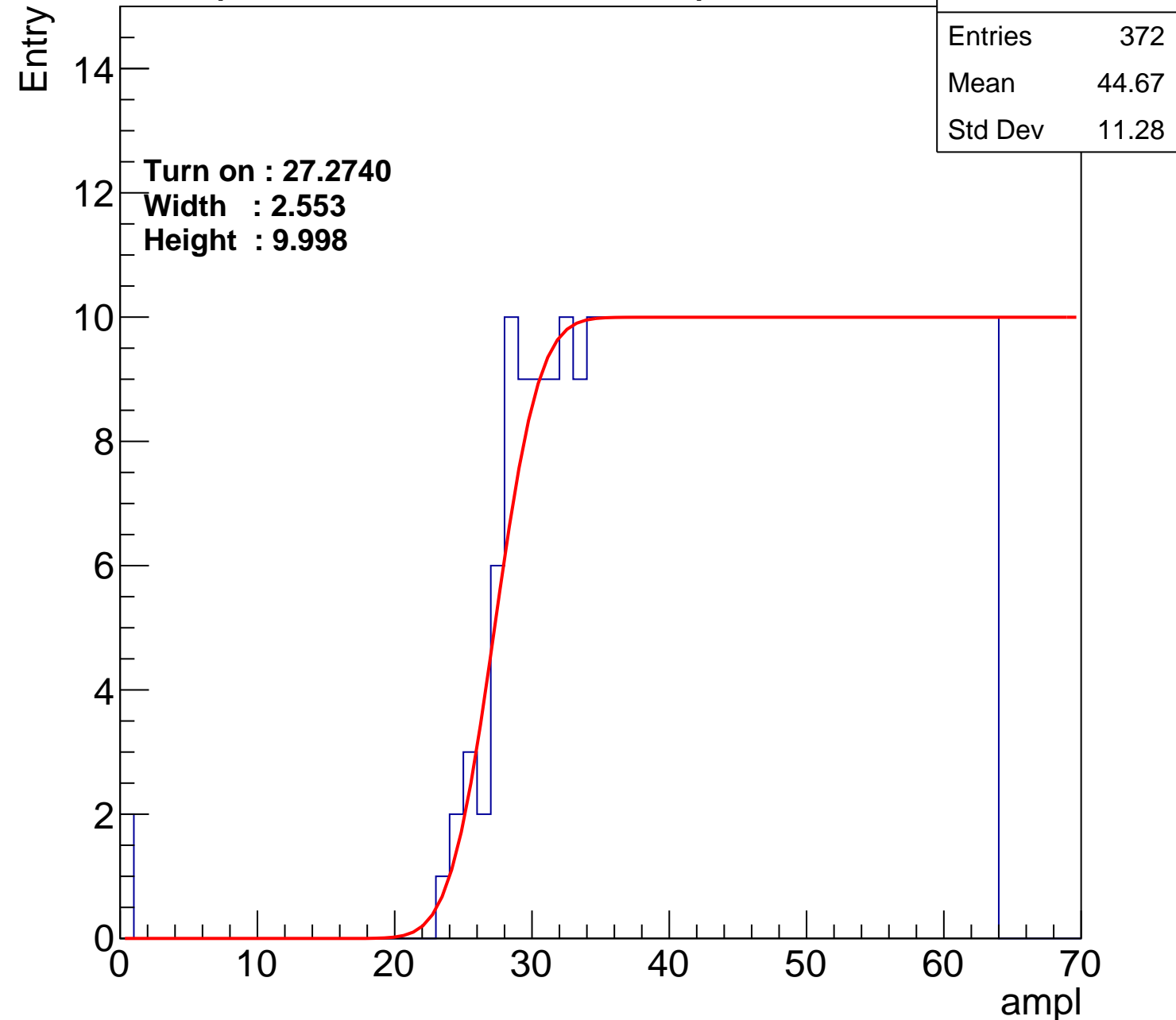
Width : 2.553

Height : 9.998

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch127

calib_packv5_042523_0143.root, FC#5, port B1

Entries	367
Mean	44.99
Std Dev	11.2

Turn on : 28.0767

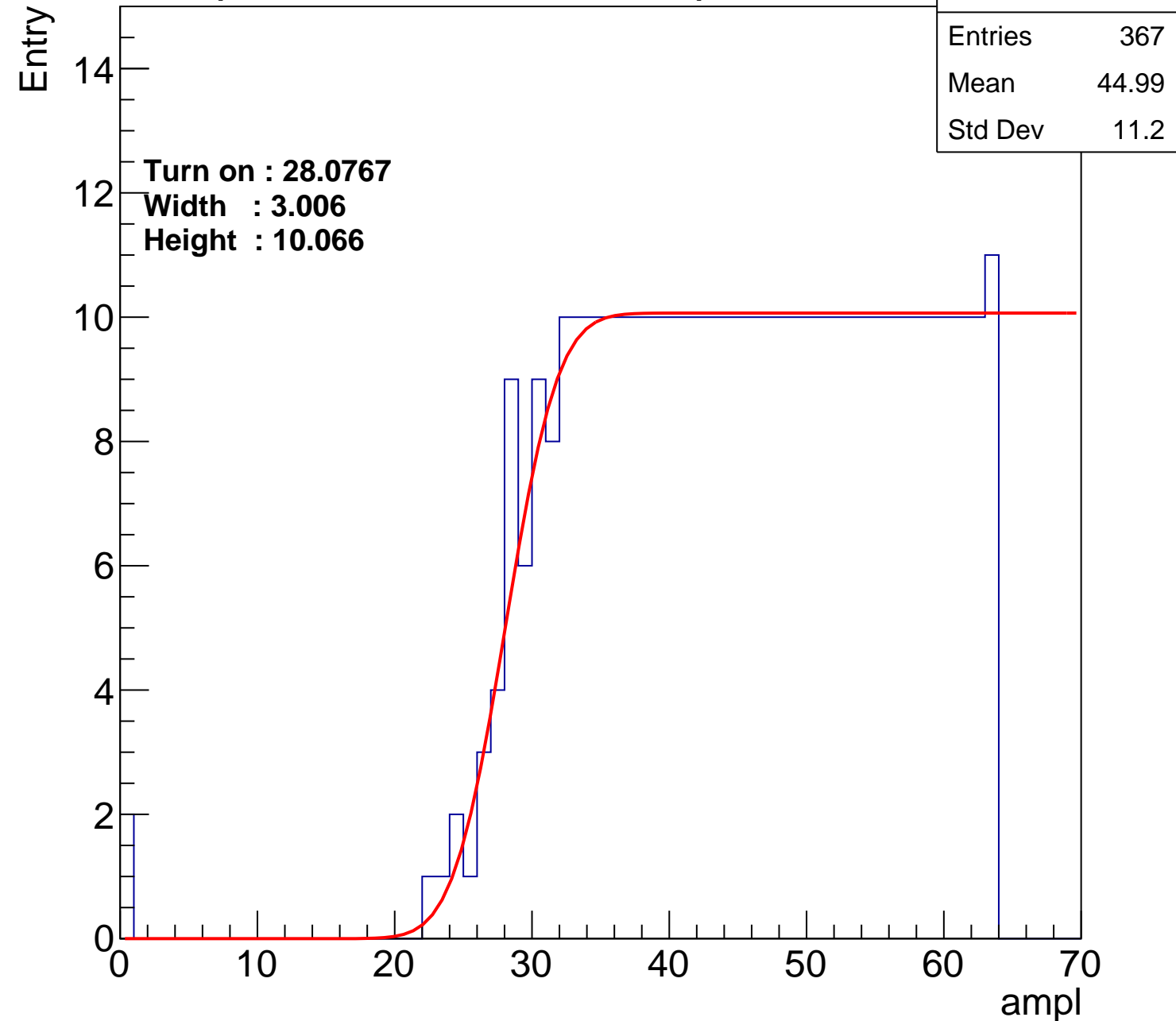
Width : 3.006

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B0L000S, U18-ch127

calib_packv5_042523_0143.root, FC#5, port B1

Entries	367
Mean	44.99
Std Dev	11.2

Turn on : 28.0767

Width : 3.006

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl

