



# B1L103S, U16-ch0, adc0

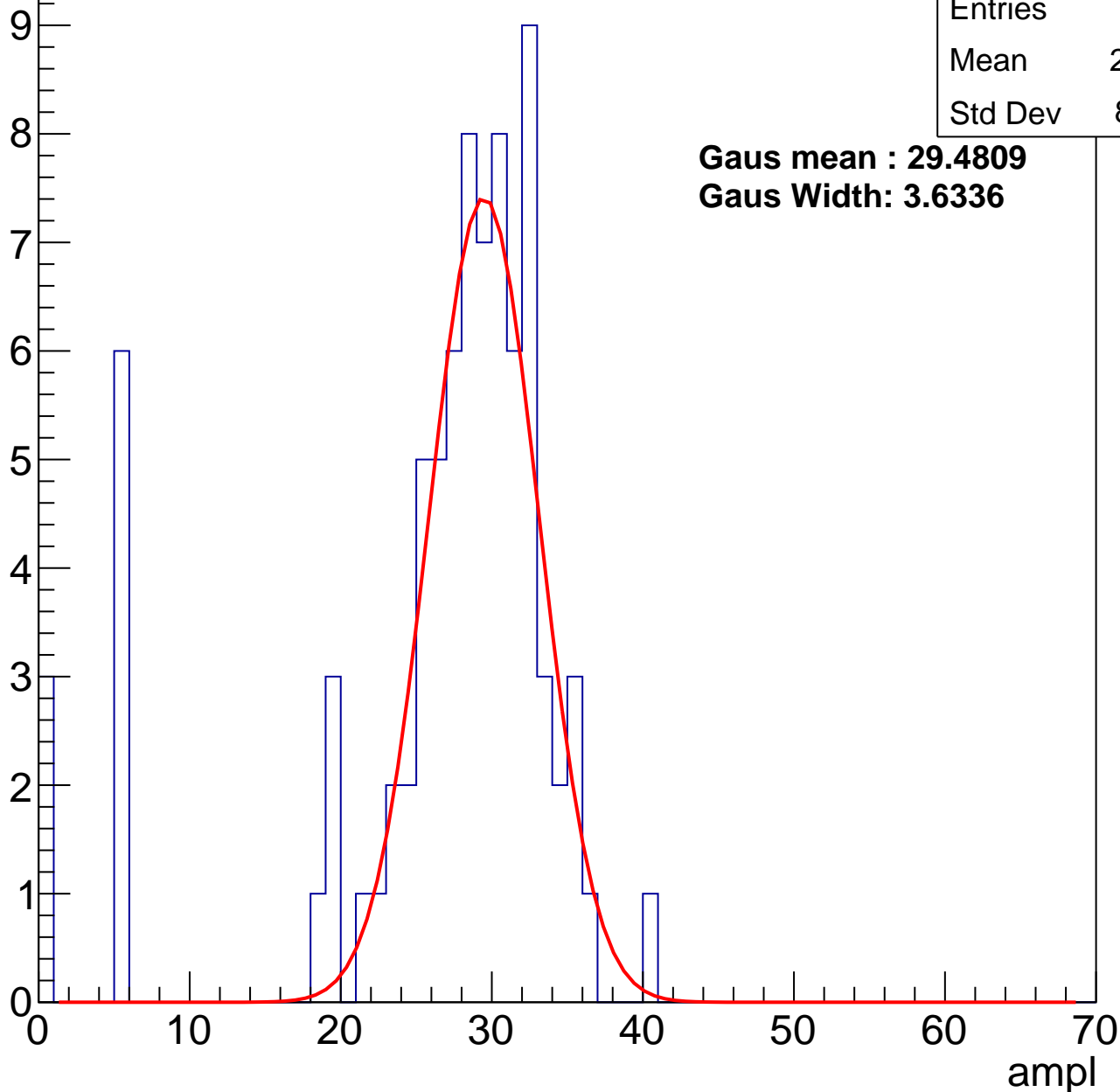
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	25.88
Std Dev	8.831

**Gaus mean : 29.4809**

**Gaus Width: 3.6336**



# B1L103S, U16-ch0, adc1

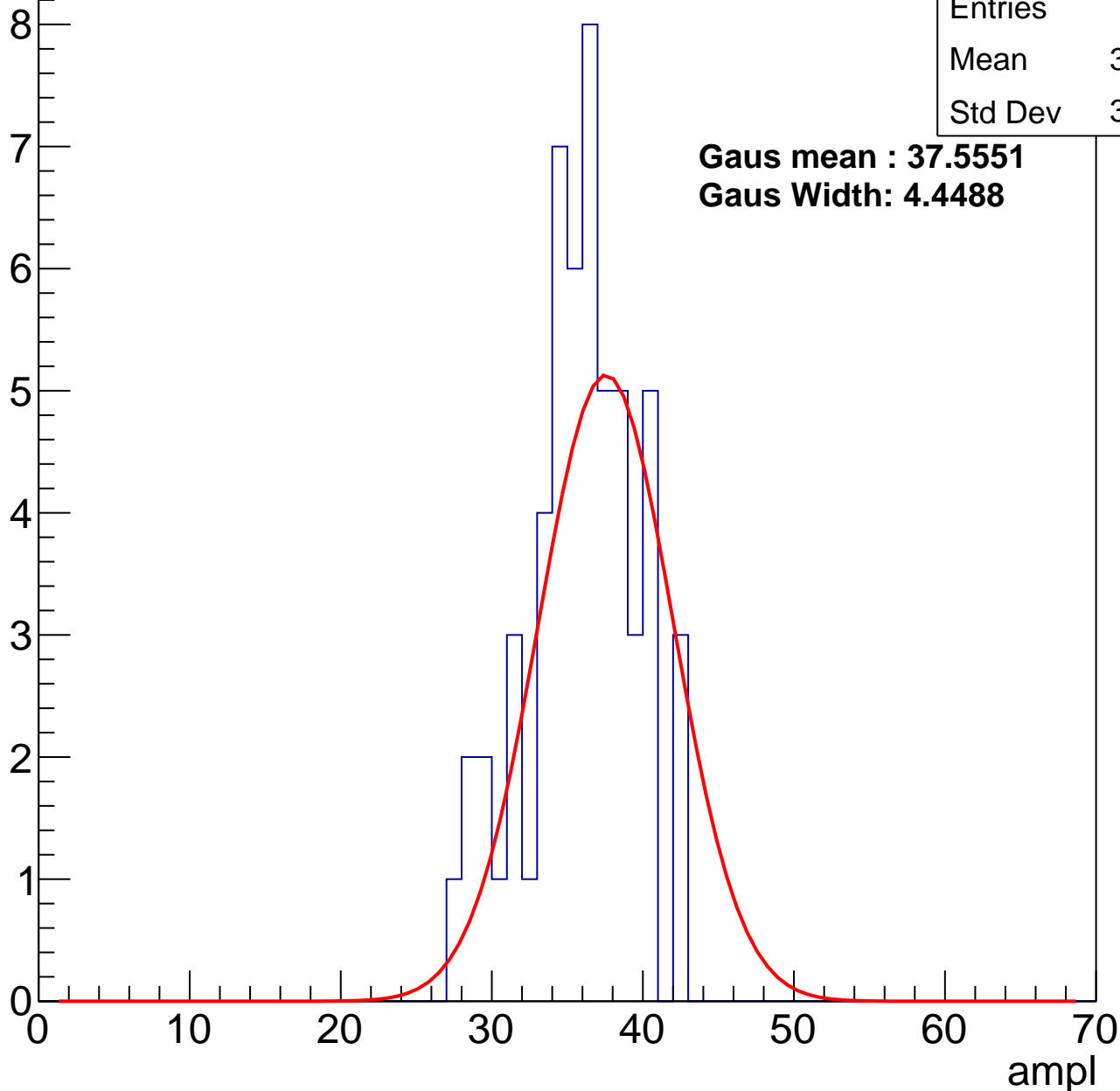
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	35.39
Std Dev	3.594

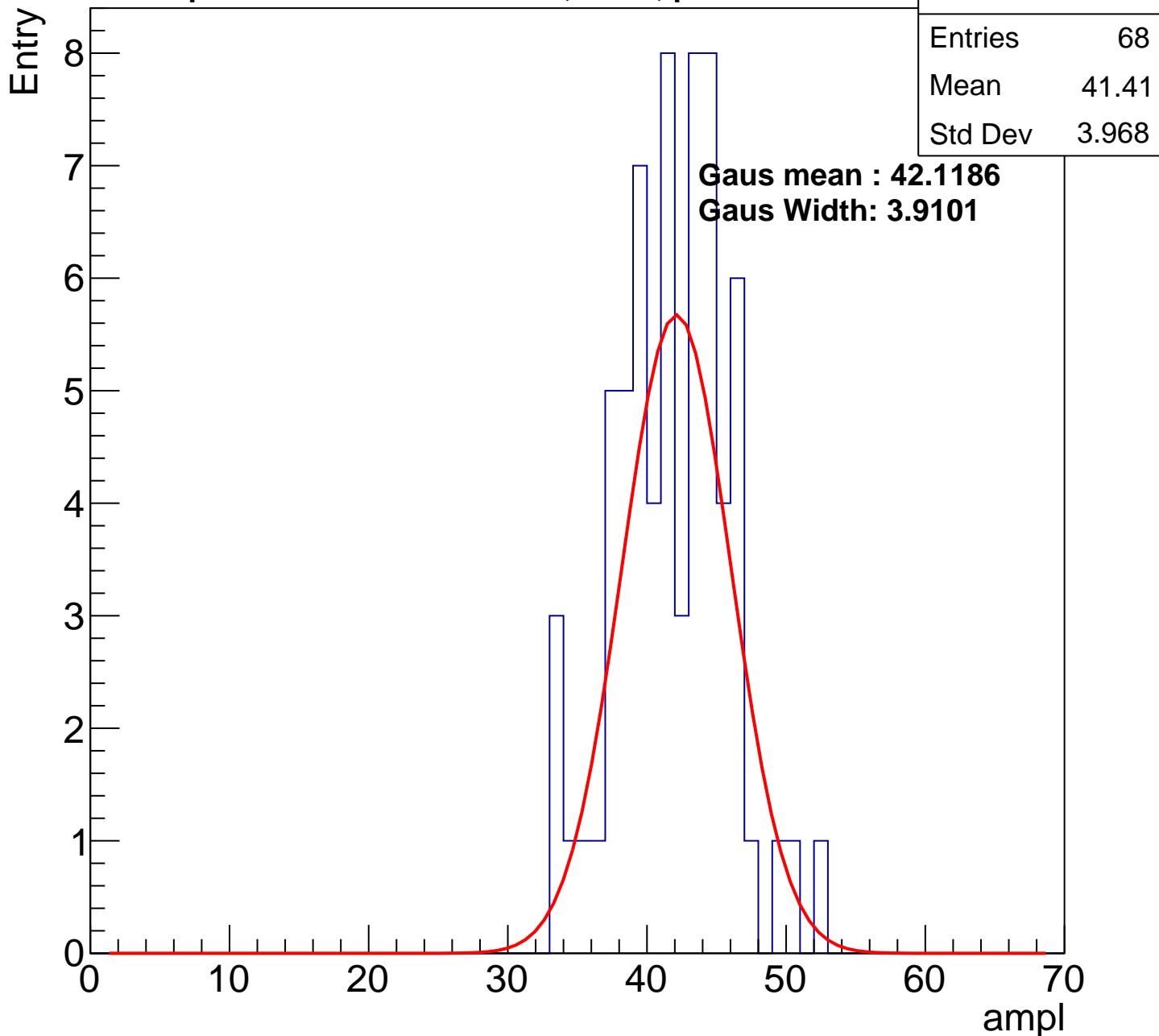
**Gaus mean : 37.5551**

**Gaus Width: 4.4488**



# B1L103S, U16-ch0, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

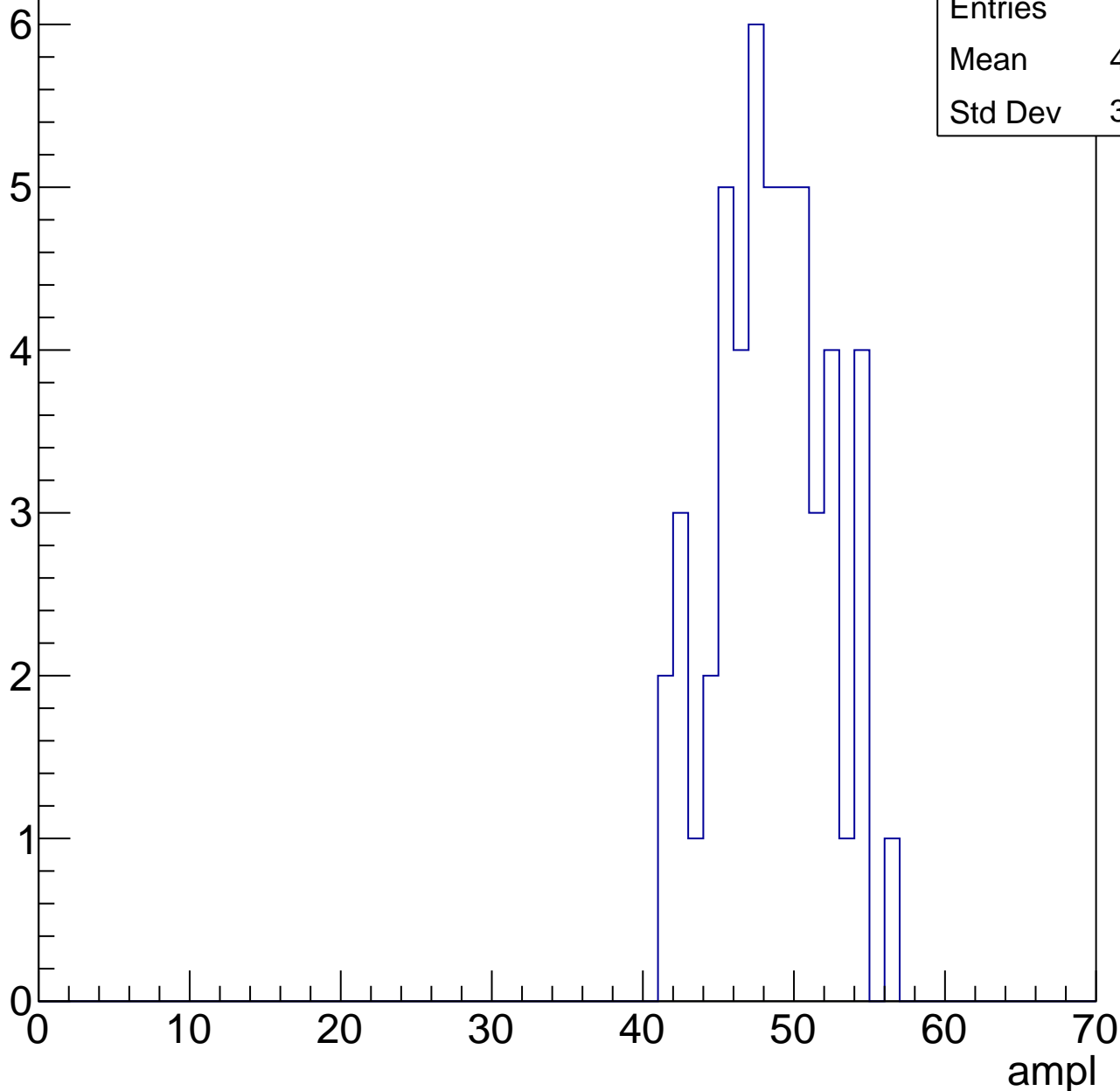


# B1L103S, U16-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	48.06
Std Dev	3.648

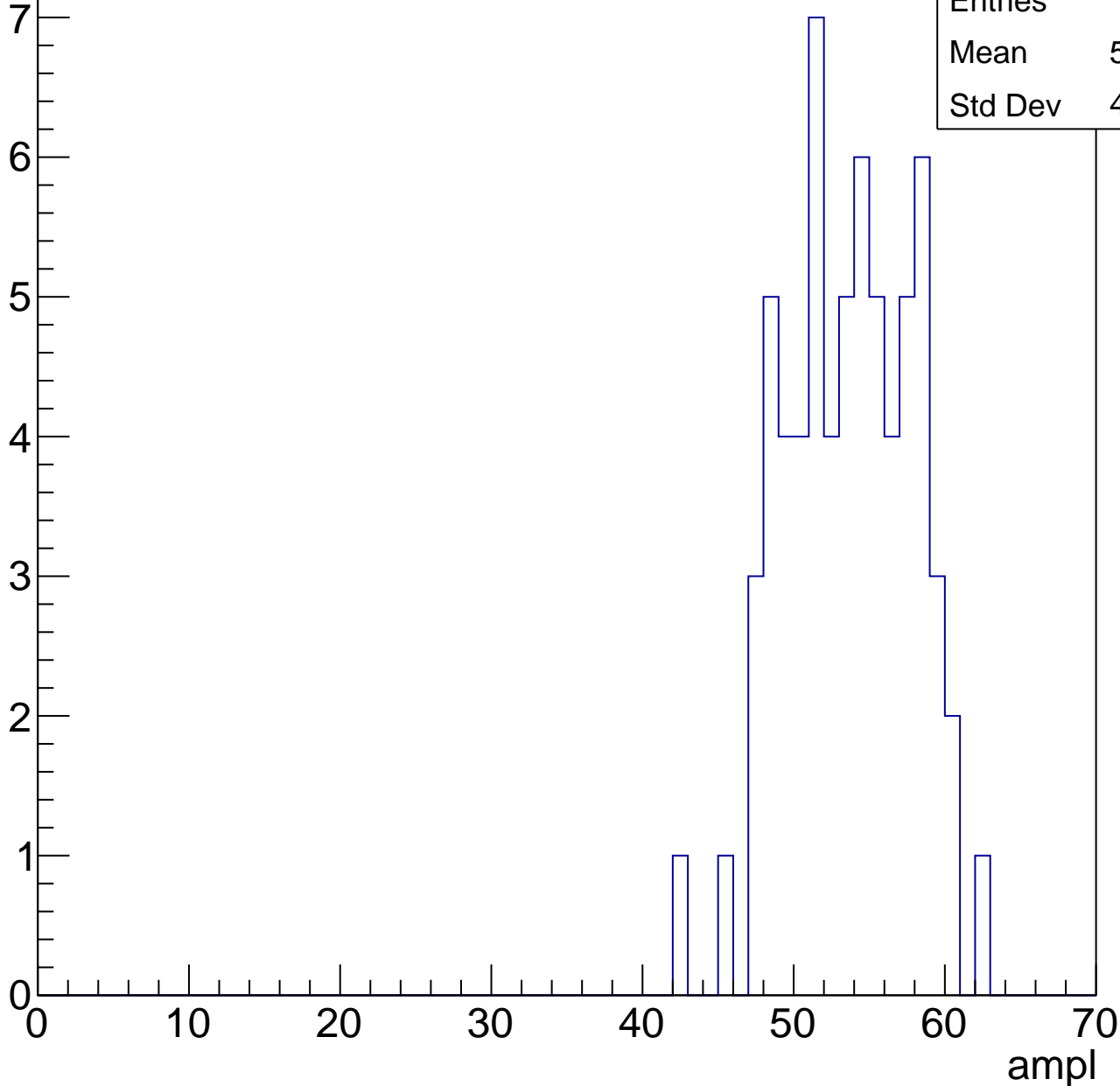


# B1L103S, U16-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	53.17
Std Dev	4.133

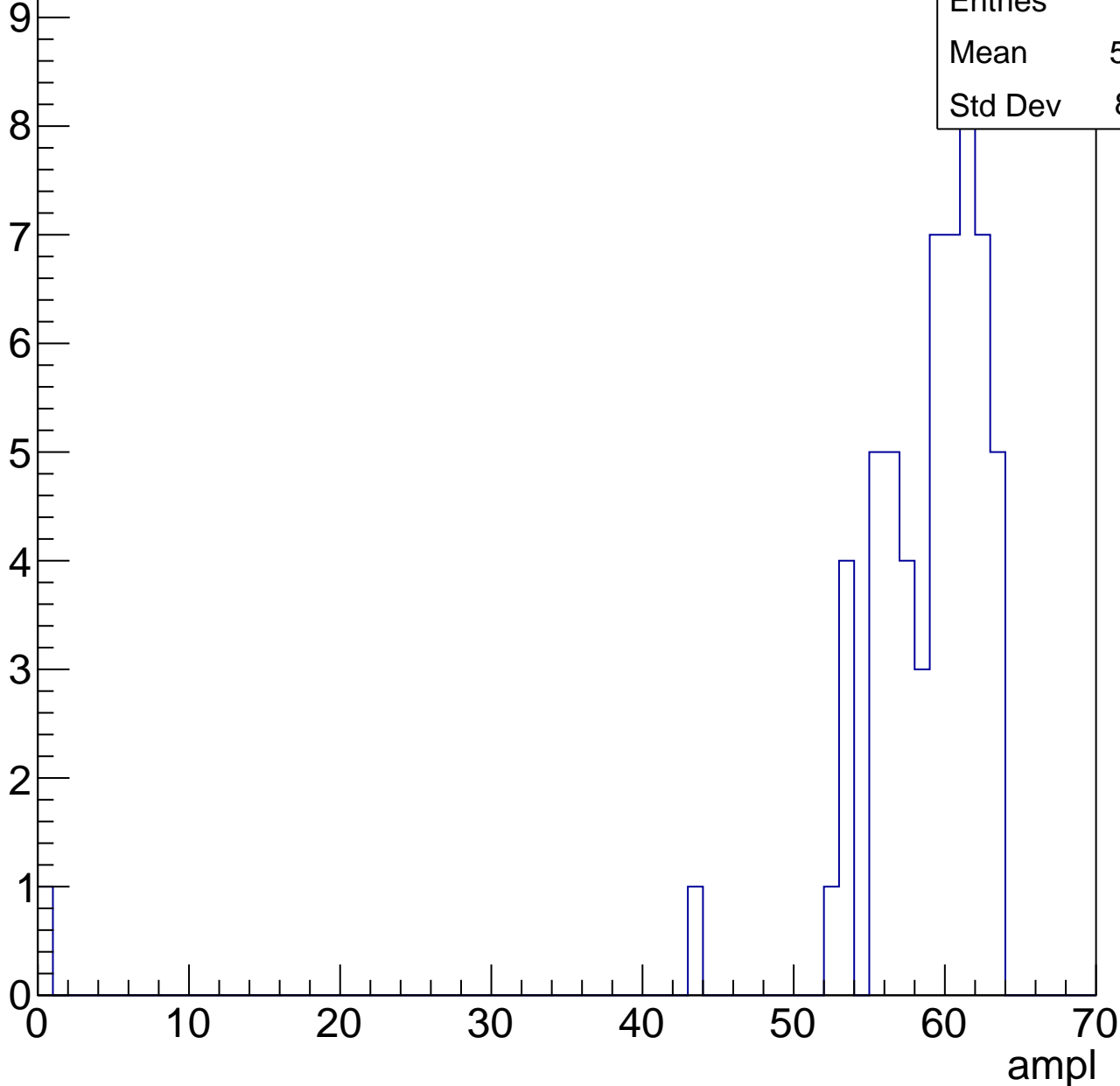


# B1L103S, U16-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	57.54
Std Dev	8.371

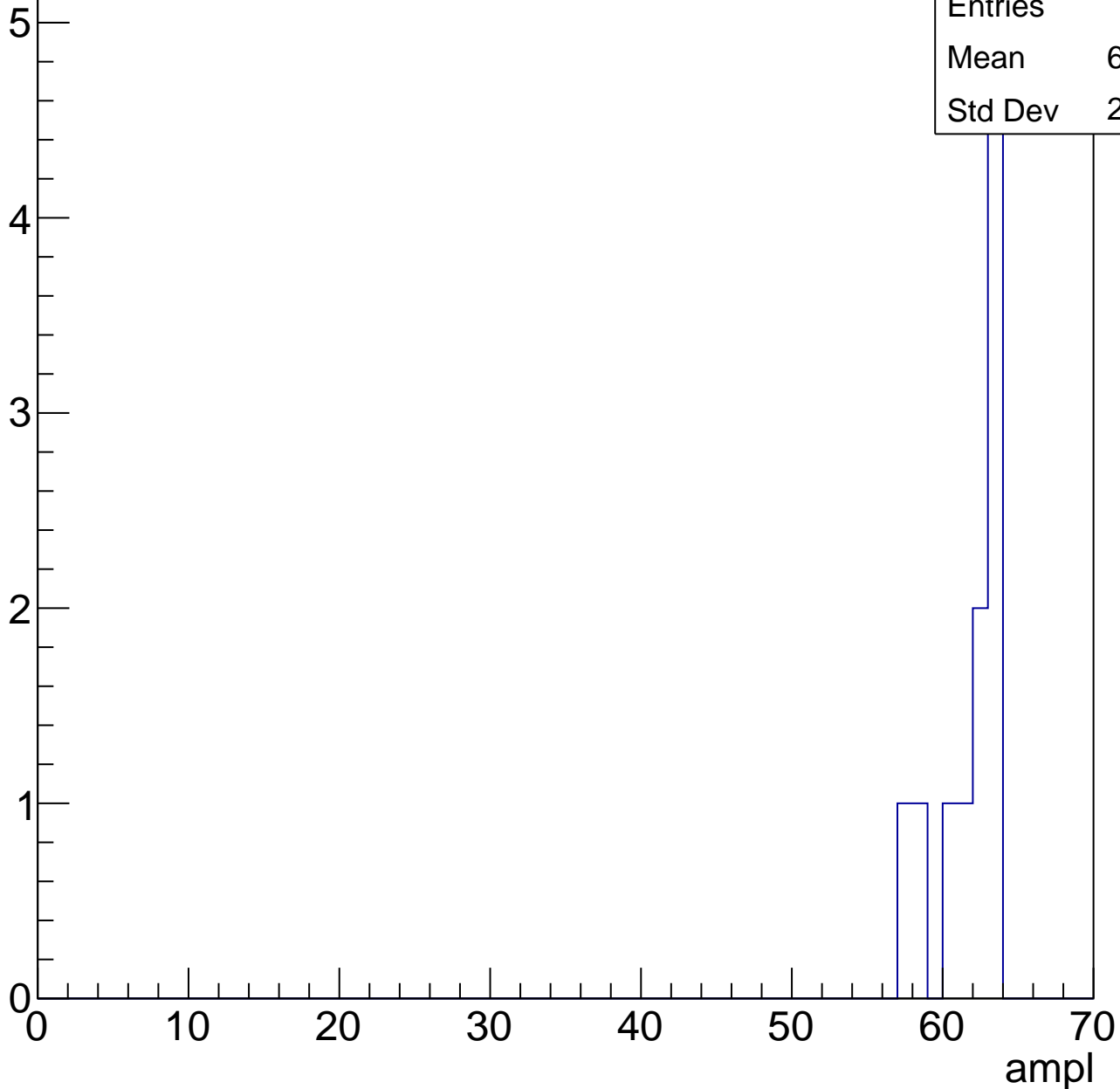


# B1L103S, U16-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	11
Mean	61.36
Std Dev	2.057





# B1L103S, U16-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

1

Mean

5

Std Dev

0

# B1L103S, U16-ch1, adc0

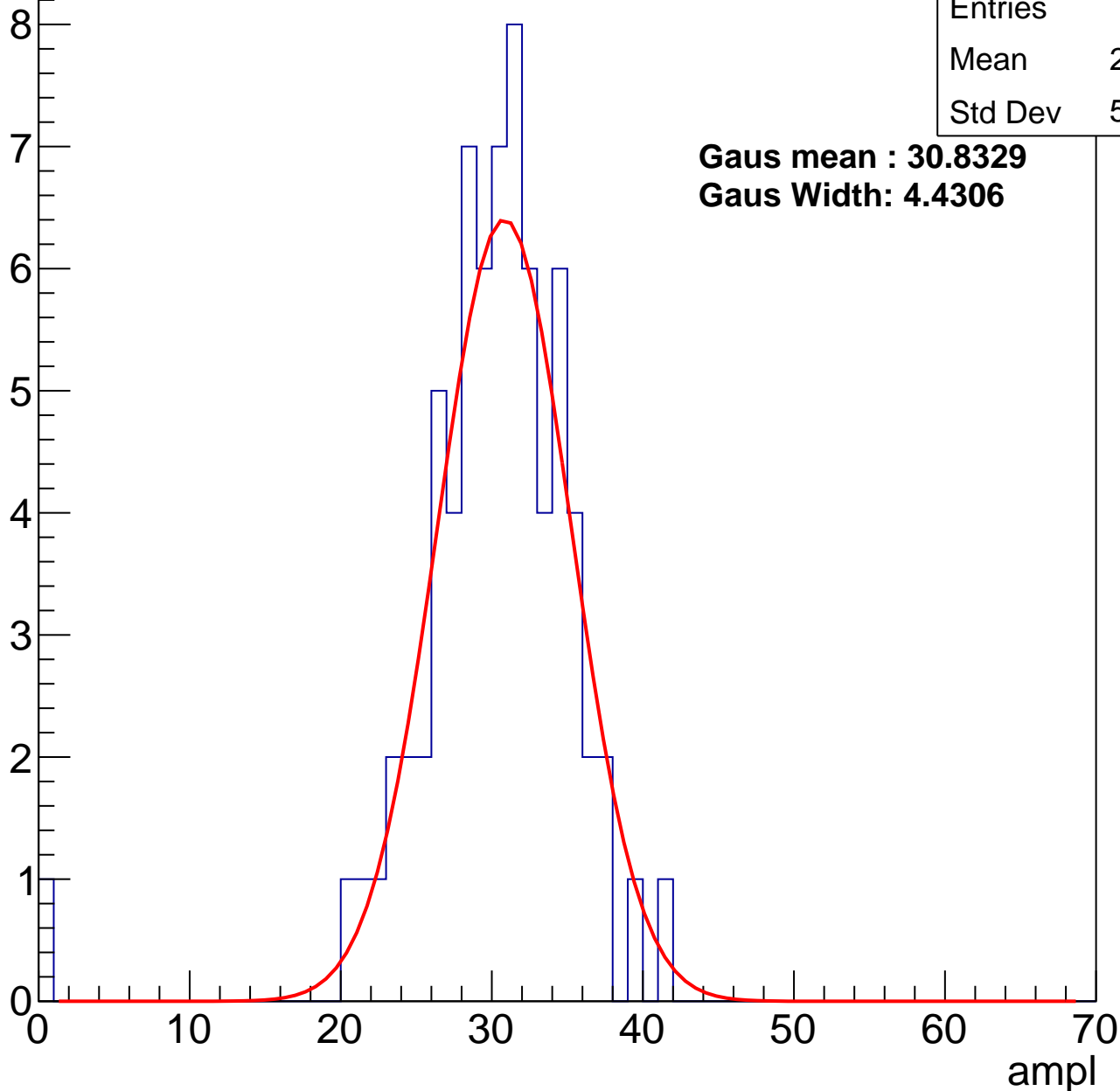
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	29.68
Std Dev	5.419

**Gaus mean : 30.8329**

**Gaus Width: 4.4306**



# B1L103S, U16-ch1, adc1

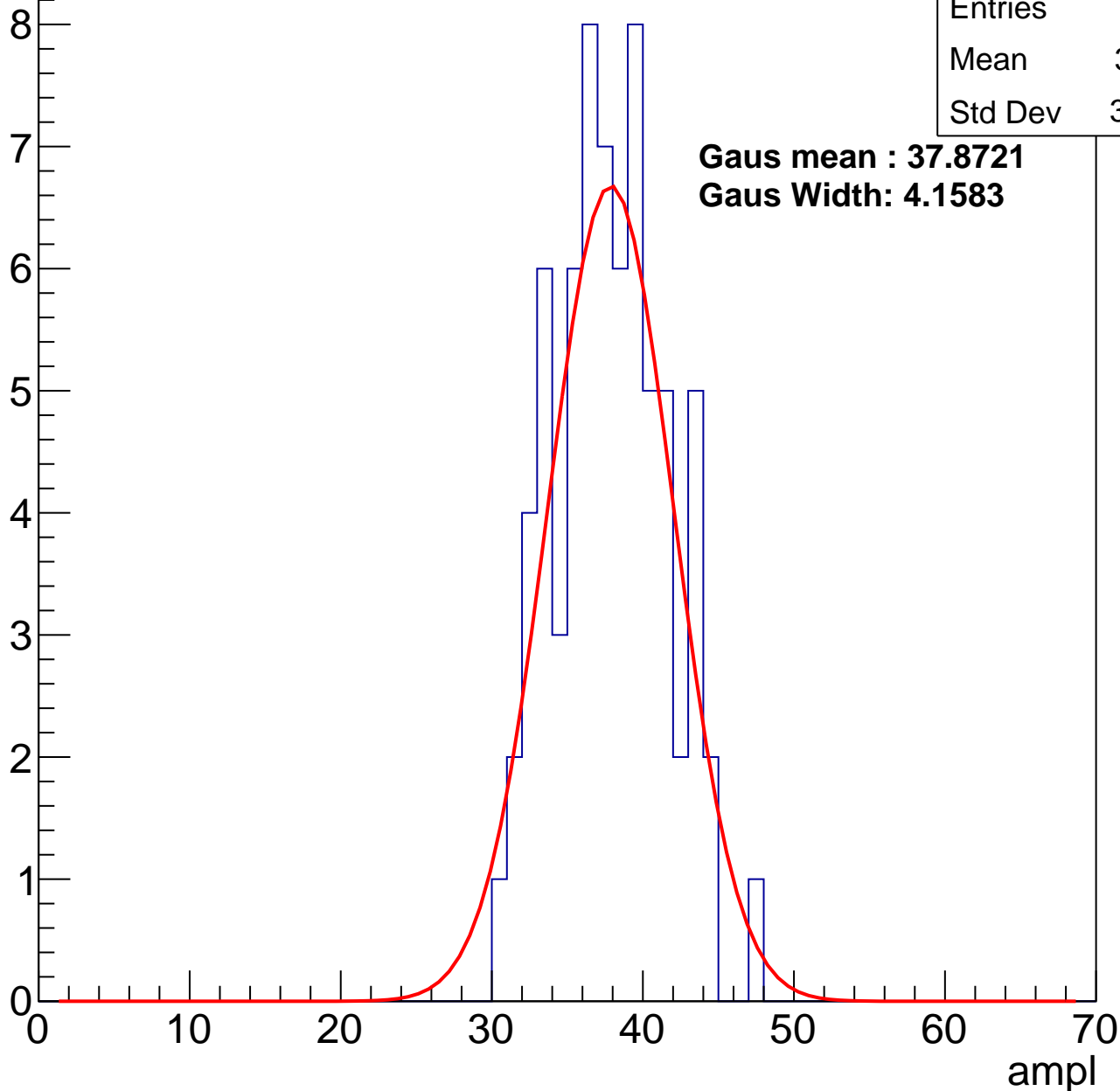
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	37.41
Std Dev	3.668

**Gaus mean : 37.8721**

**Gaus Width: 4.1583**



# B1L103S, U16-ch1, adc2

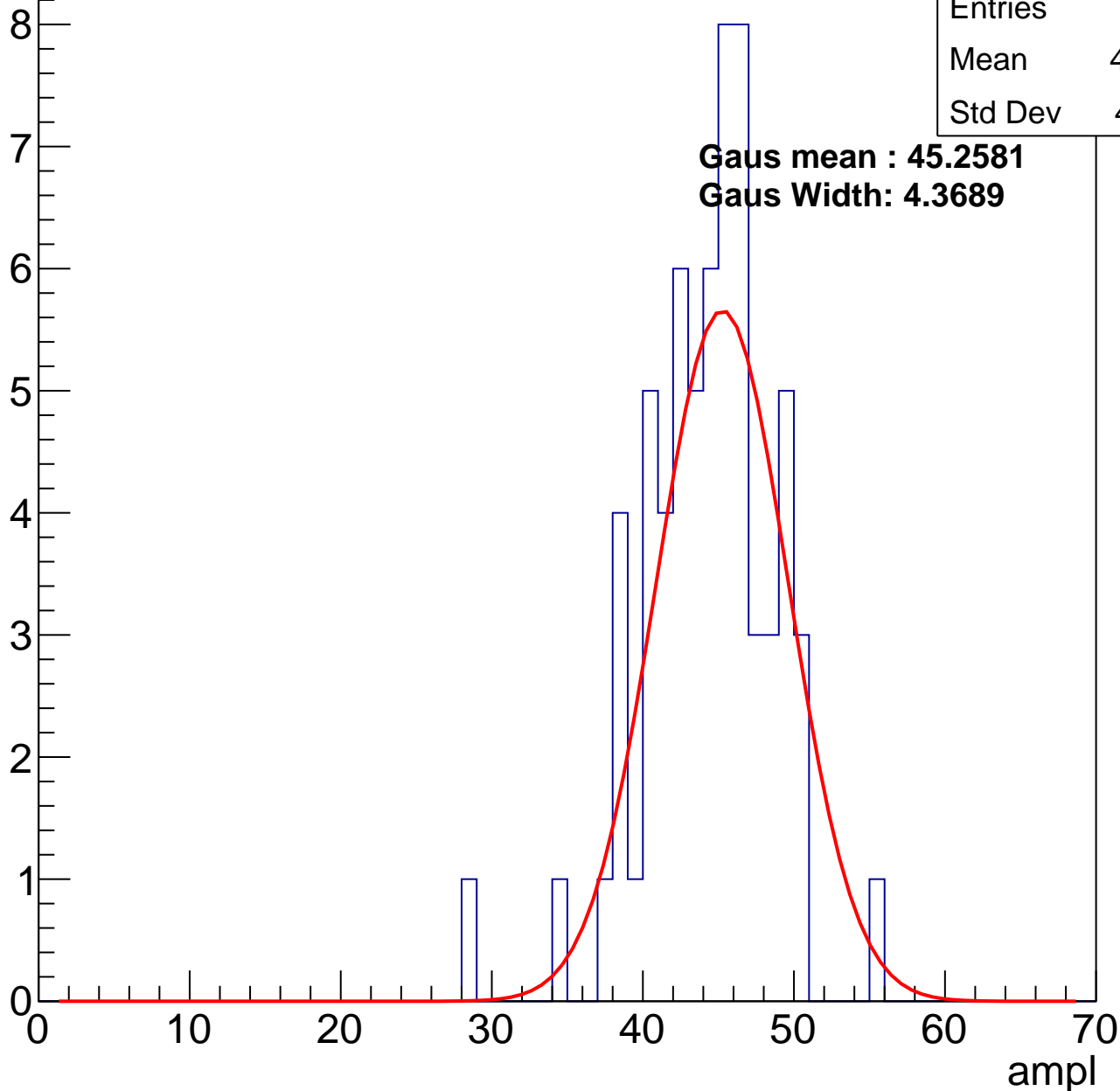
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	43.82
Std Dev	4.271

**Gaus mean : 45.2581**

**Gaus Width: 4.3689**

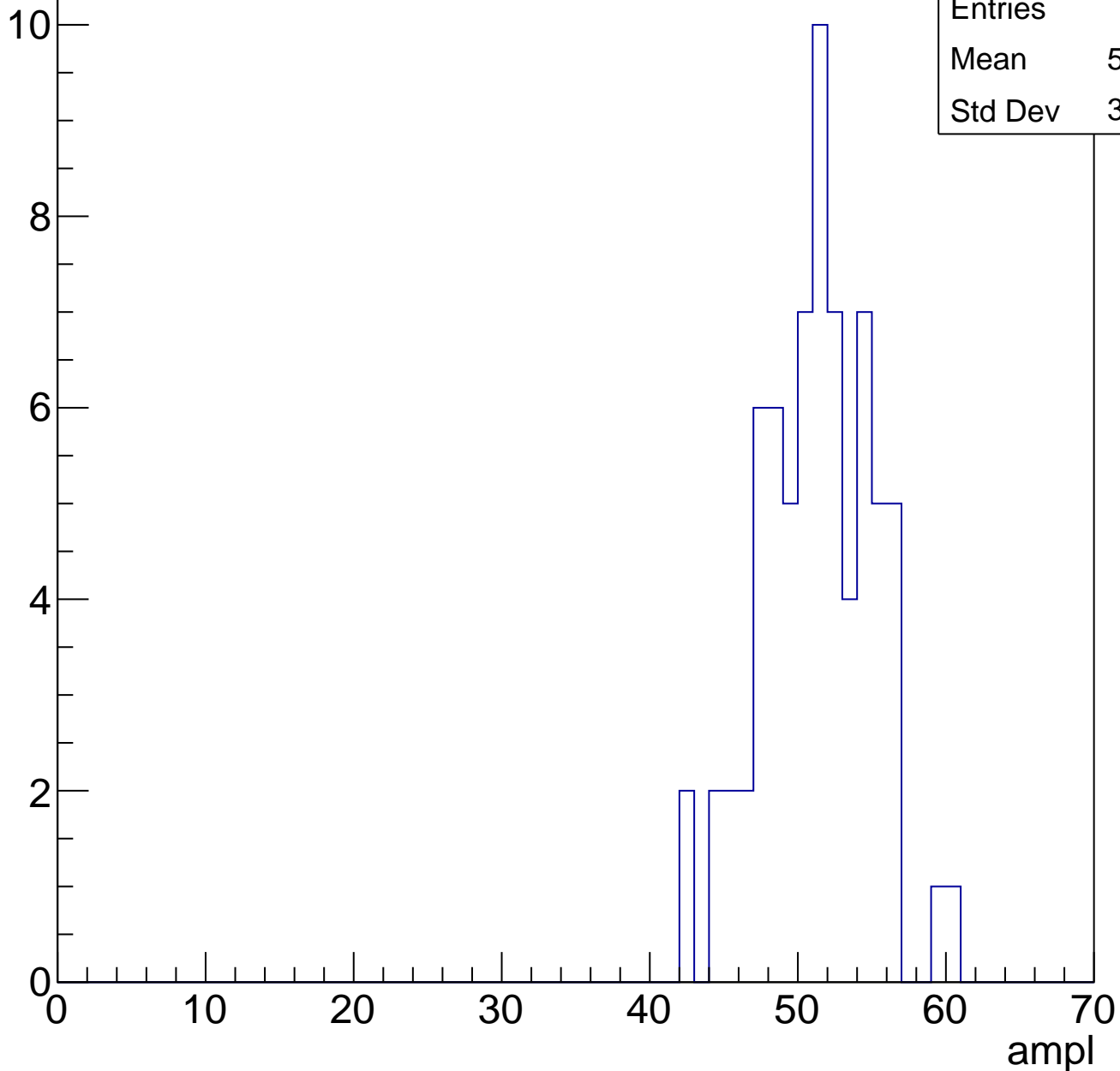


# B1L103S, U16-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	72
Mean	50.79
Std Dev	3.712

Entry

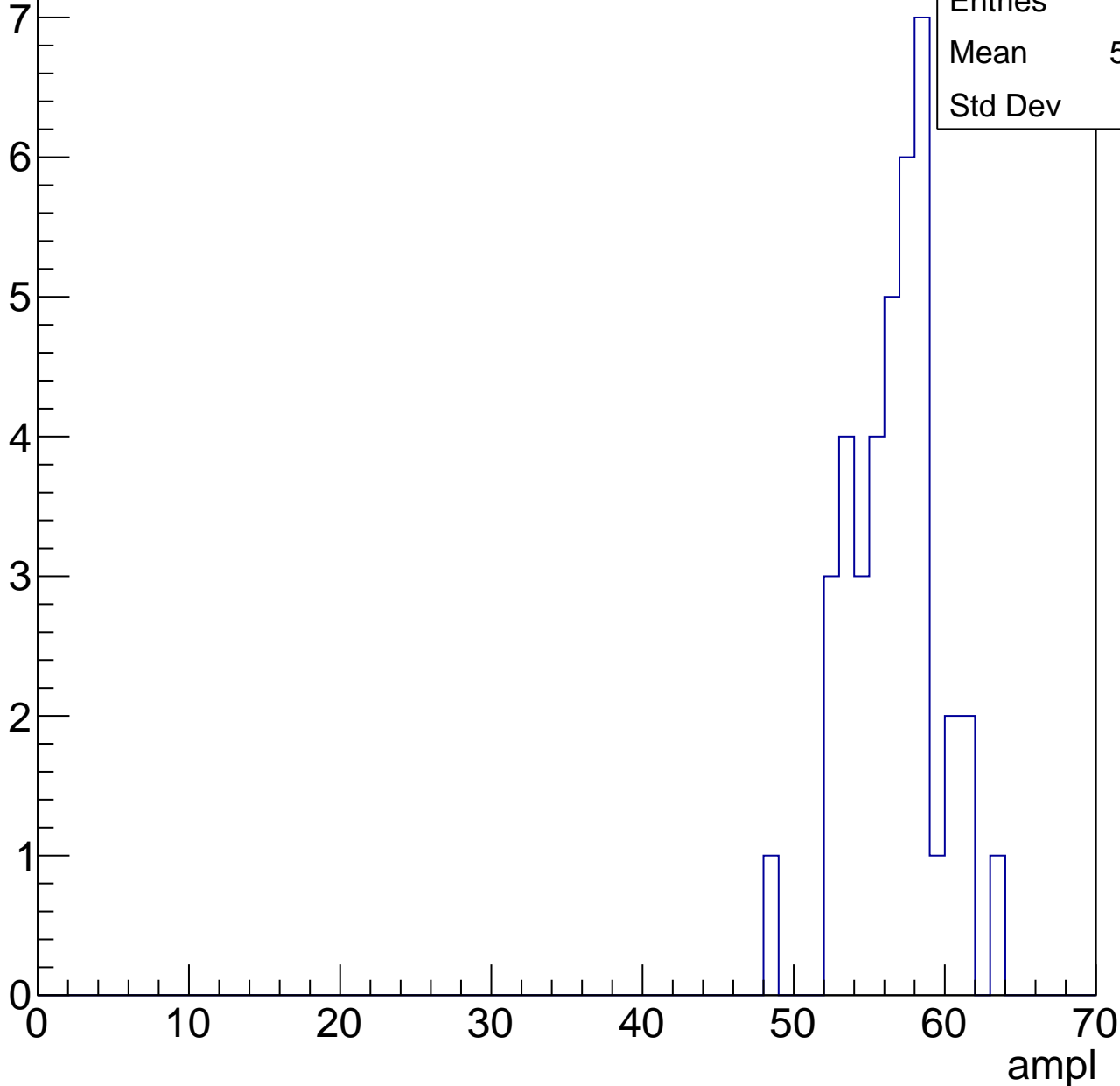


# B1L103S, U16-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

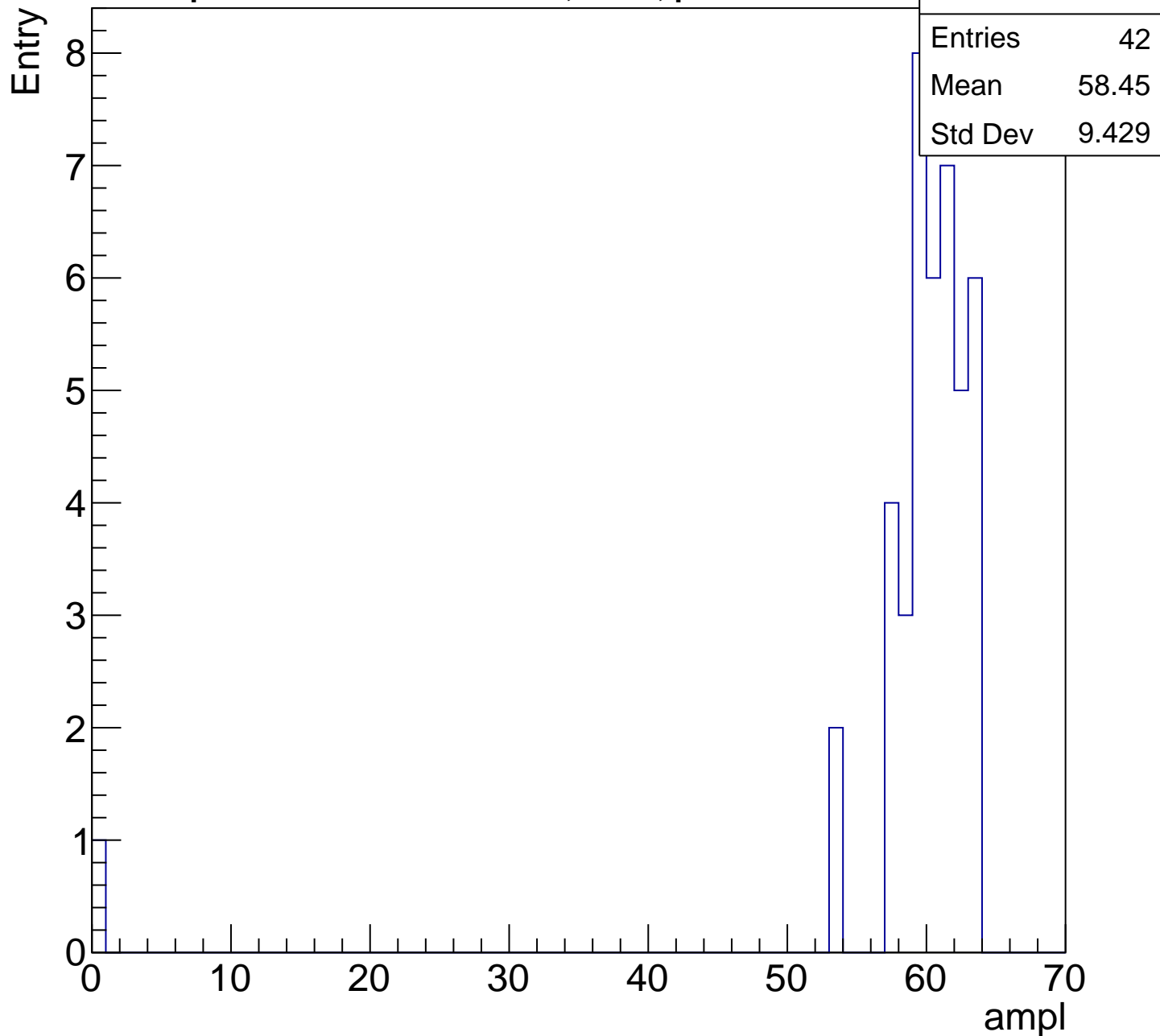
Entry

Entries	39
Mean	56.15
Std Dev	2.94



# B1L103S, U16-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

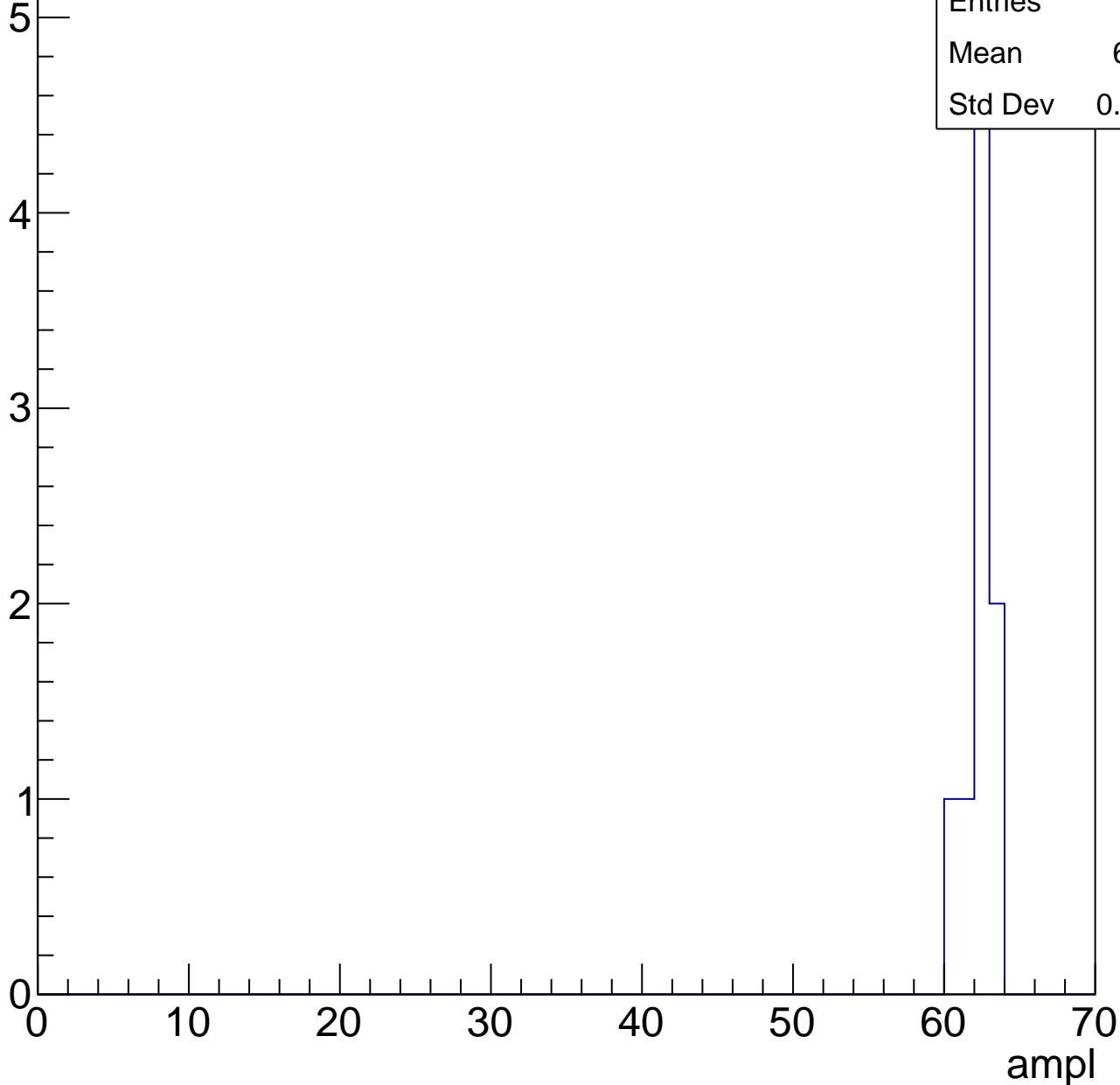


# B1L103S, U16-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	9
Mean	61.89
Std Dev	0.8749





# B1L103S, U16-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch2, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	72
Mean	29.12
Std Dev	3.979

**Gaus mean : 30.1053**

**Gaus Width: 3.9876**

Entry

10  
8  
6  
4  
2  
0

ampl

0

10

20

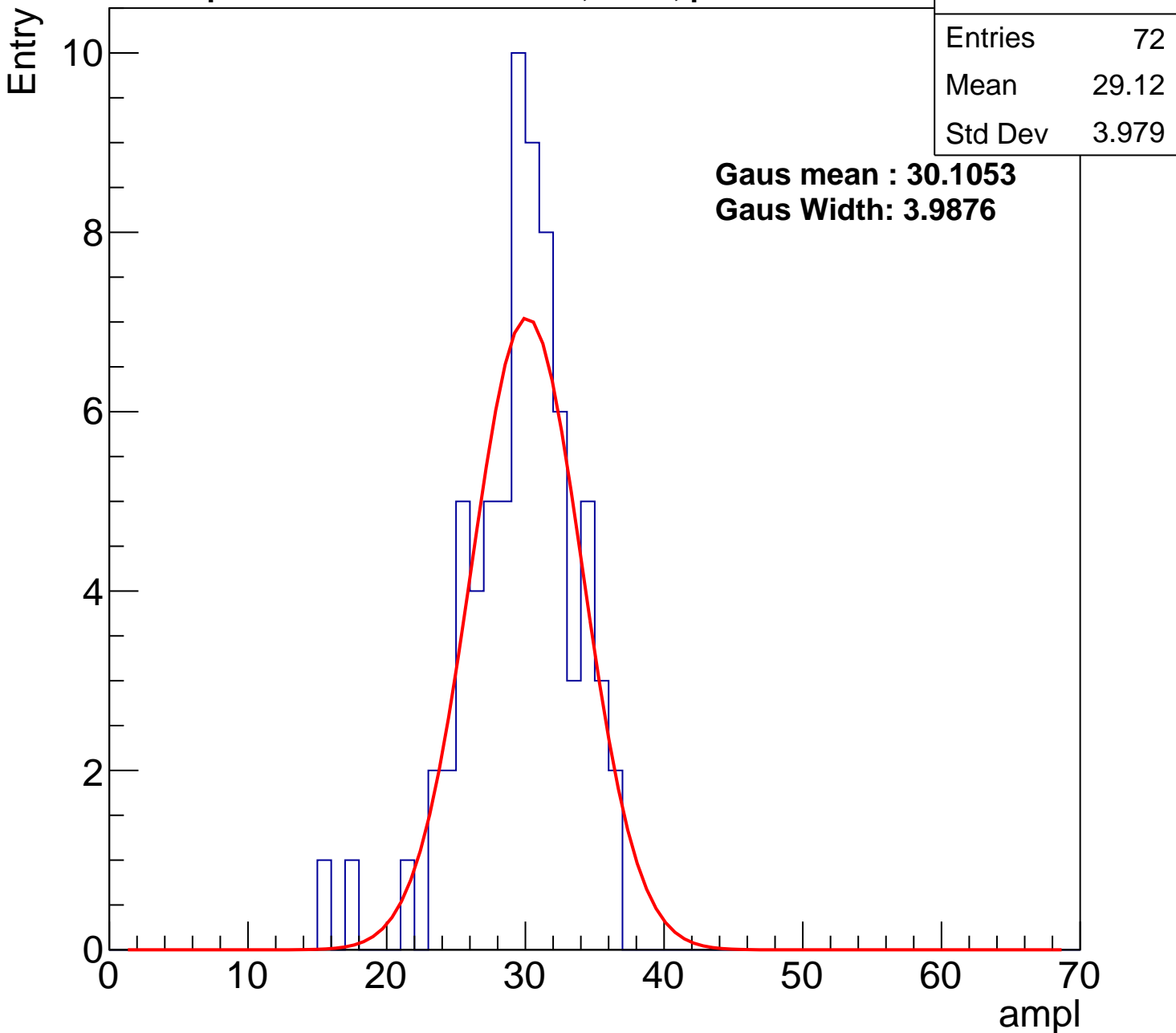
30

40

50

60

70



# B1L103S, U16-ch2, adc1

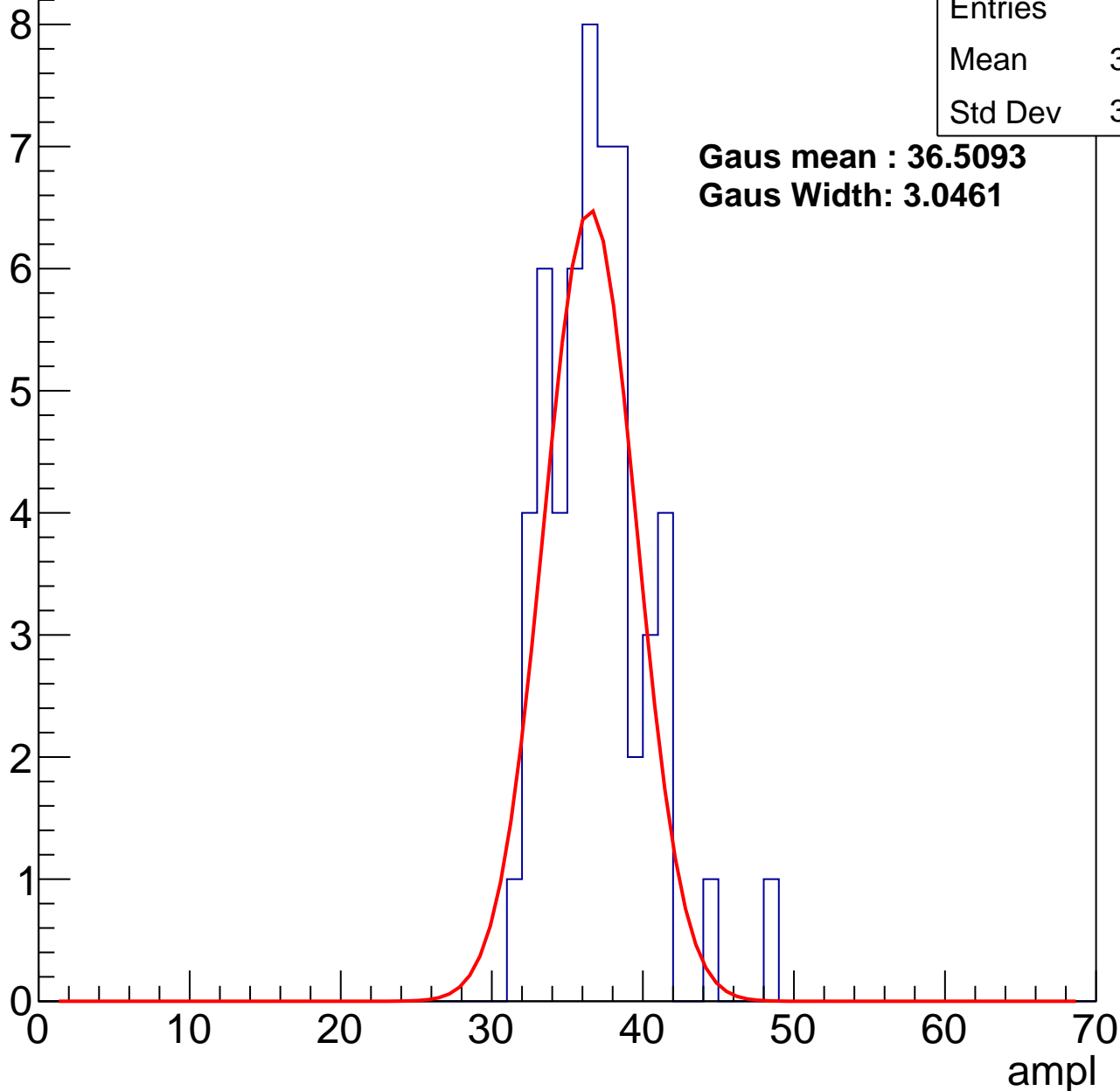
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	36.48
Std Dev	3.225

**Gaus mean : 36.5093**

**Gaus Width: 3.0461**



# B1L103S, U16-ch2, adc2

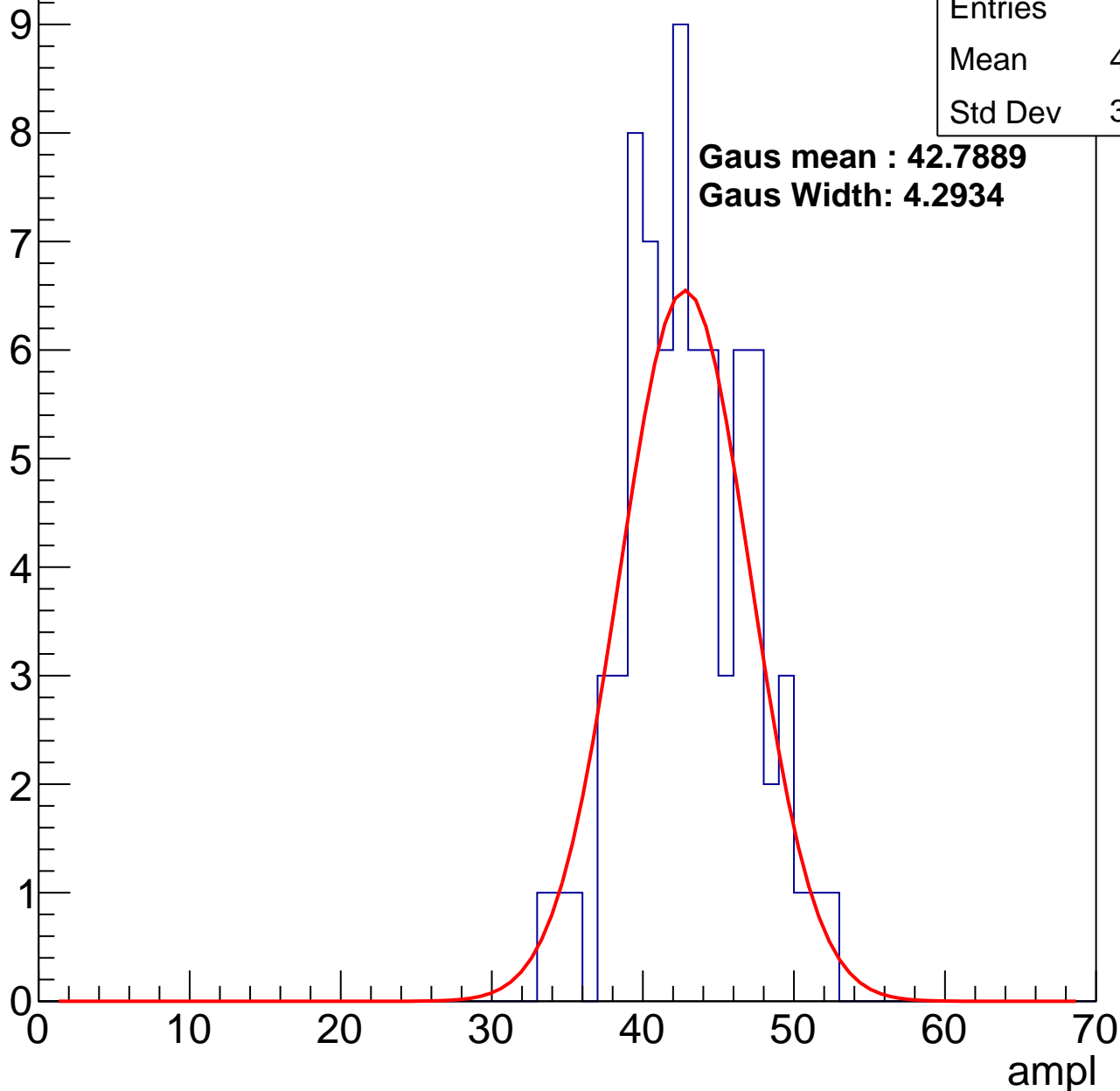
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	42.62
Std Dev	3.962

**Gaus mean : 42.7889**

**Gaus Width: 4.2934**

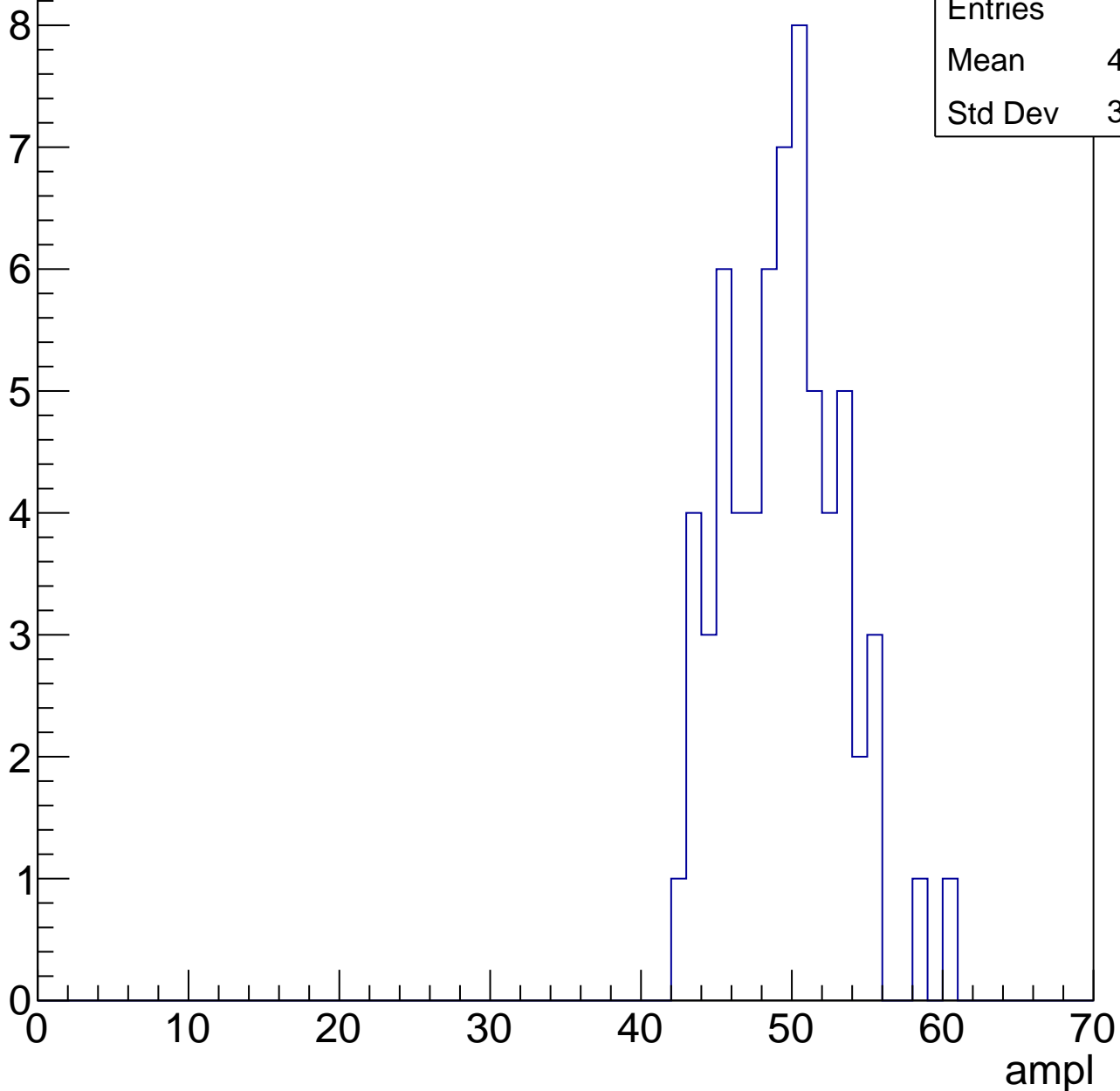


# B1L103S, U16-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	49.03
Std Dev	3.804

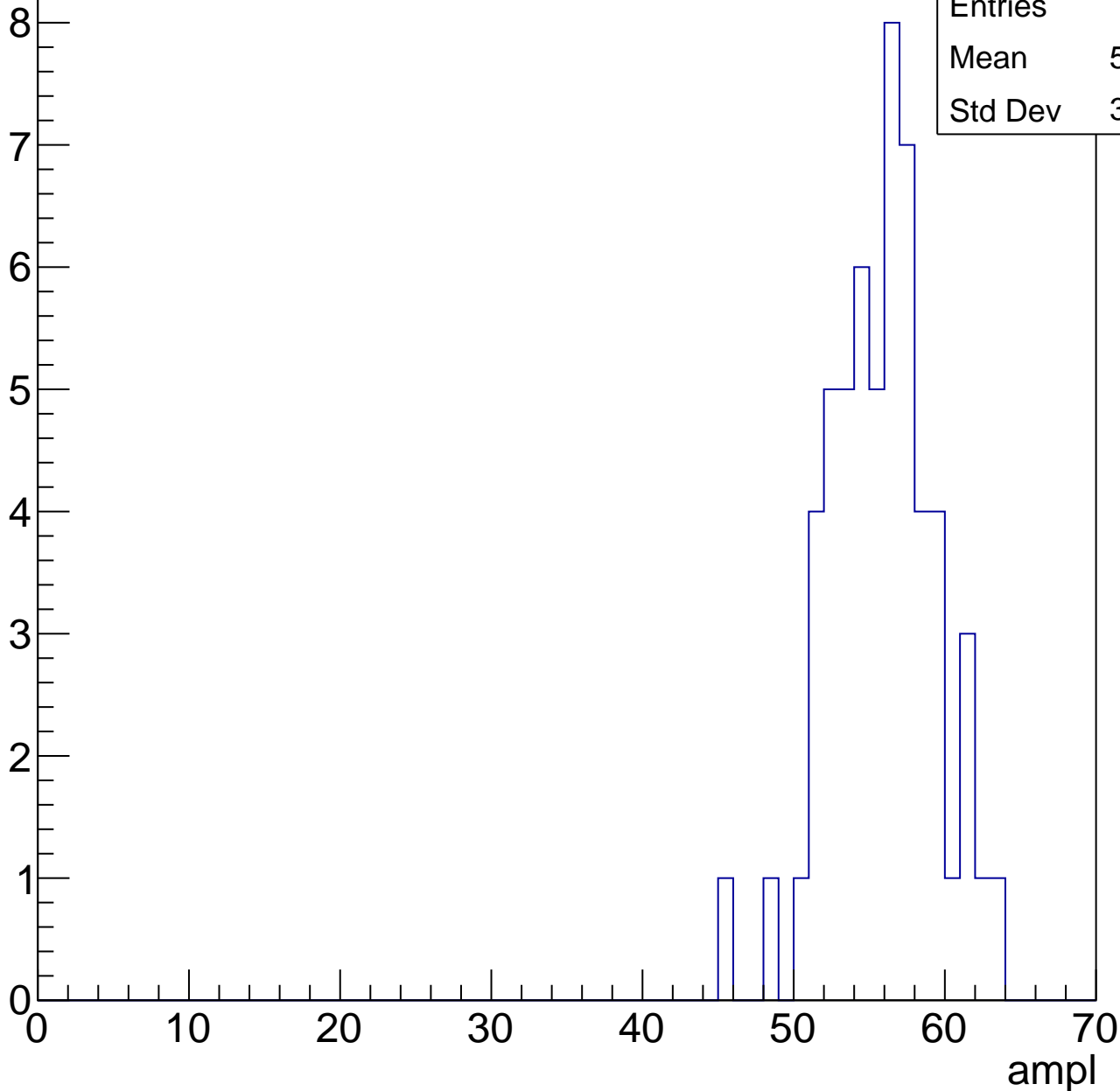


# B1L103S, U16-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

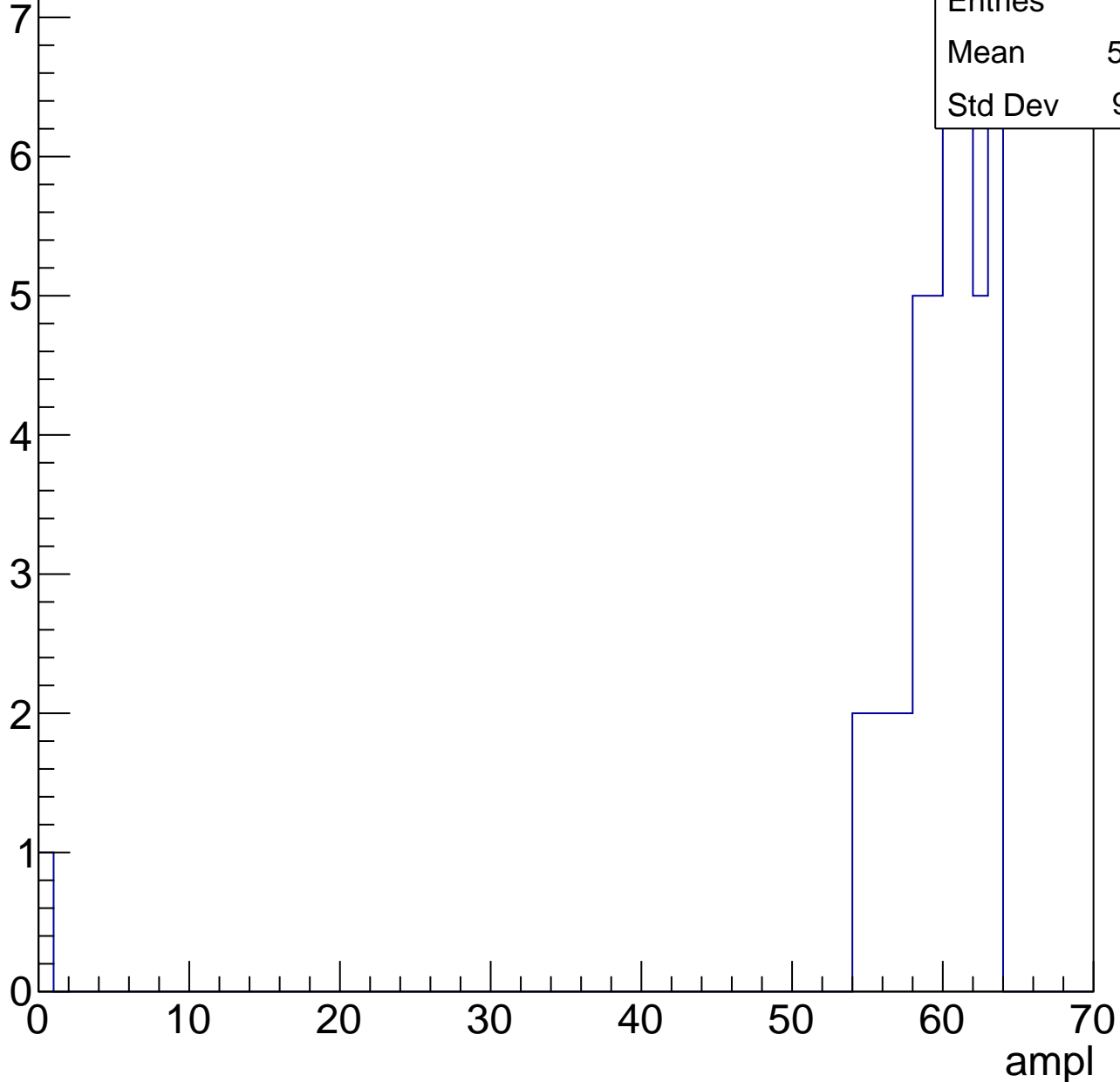
Entries	57
Mean	55.33
Std Dev	3.466



# B1L103S, U16-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

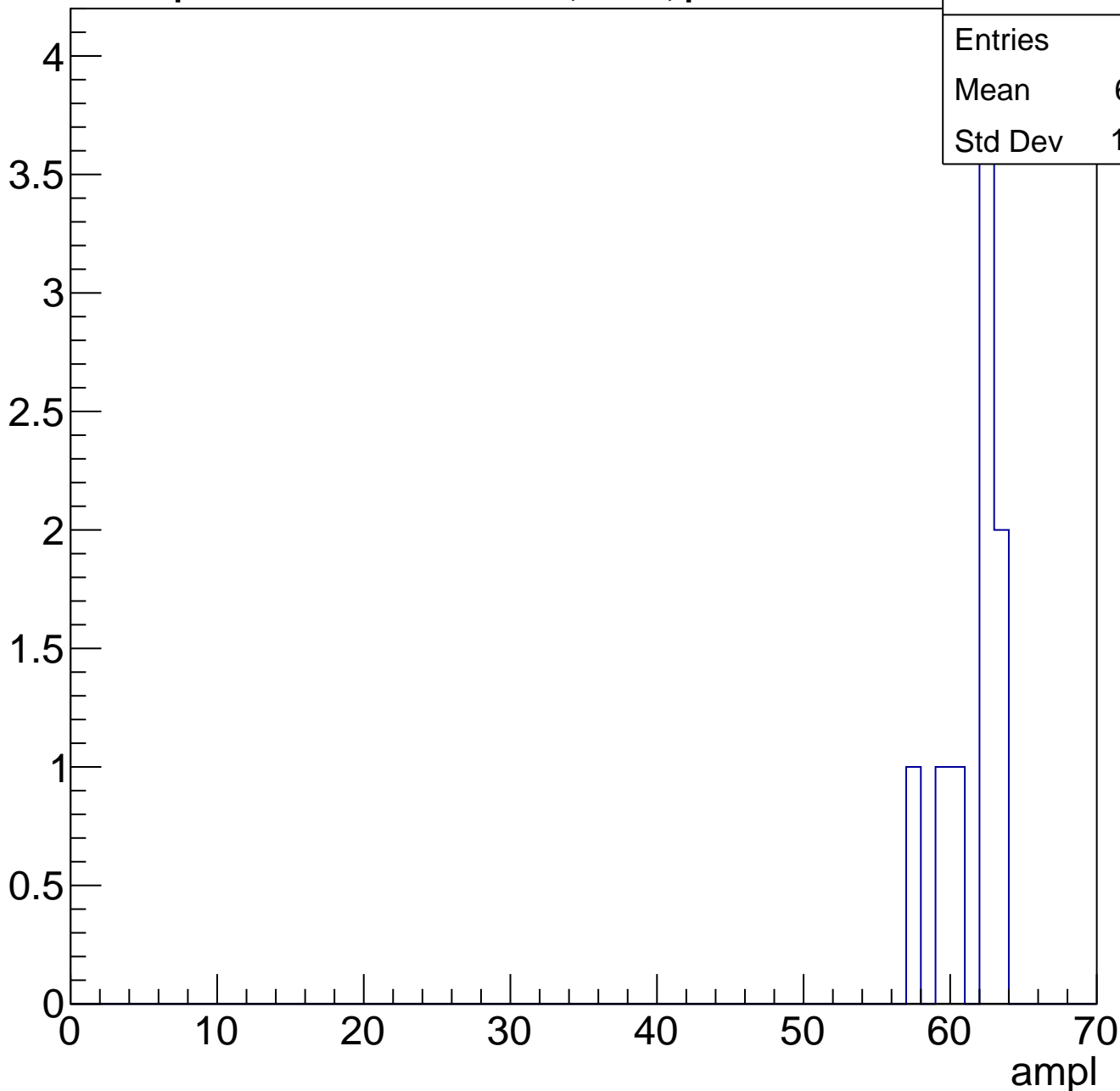
Entry



# B1L103S, U16-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U16-ch3, adc0

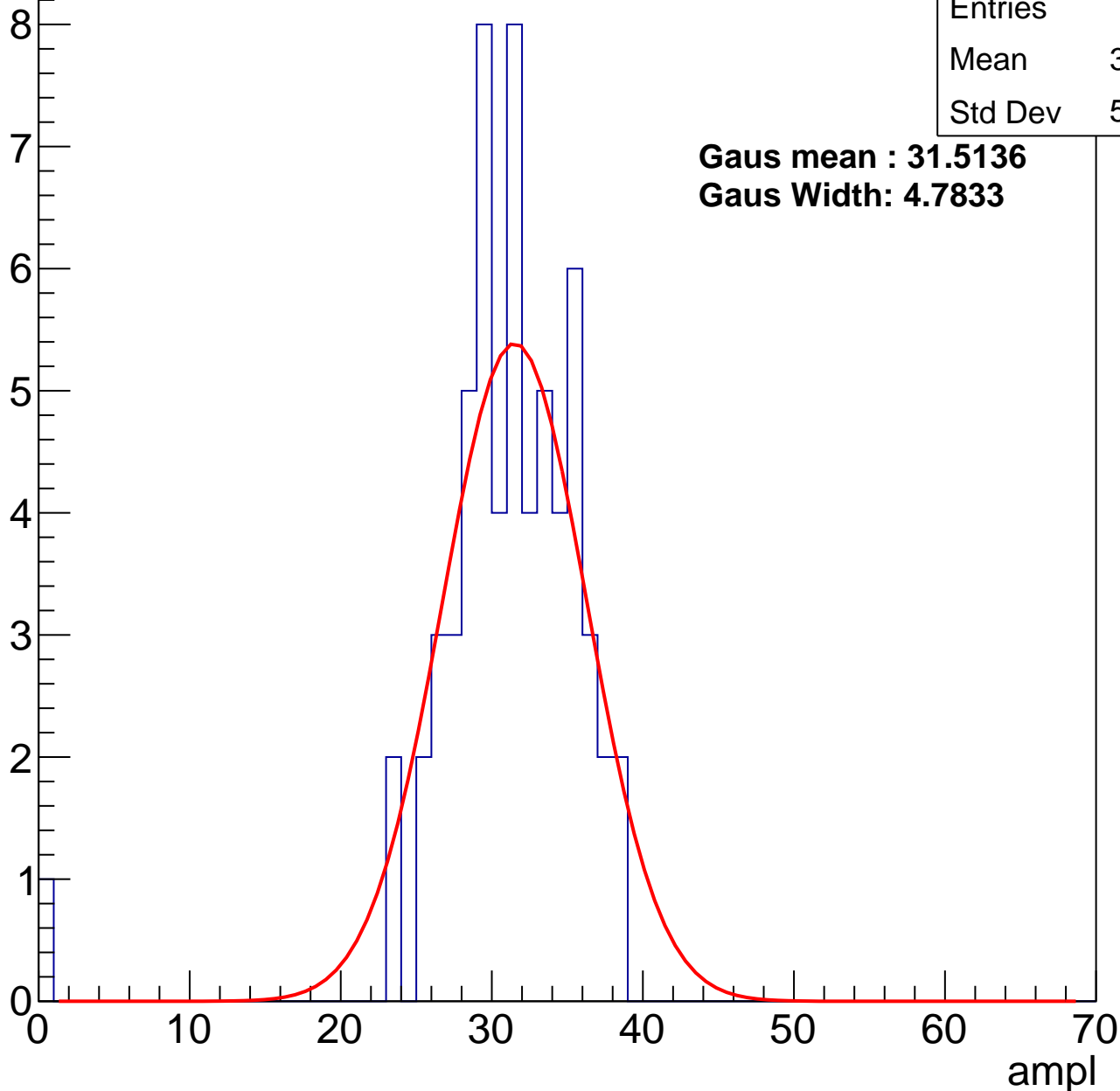
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	30.52
Std Dev	5.315

**Gaus mean : 31.5136**

**Gaus Width: 4.7833**



# B1L103S, U16-ch3, adc1

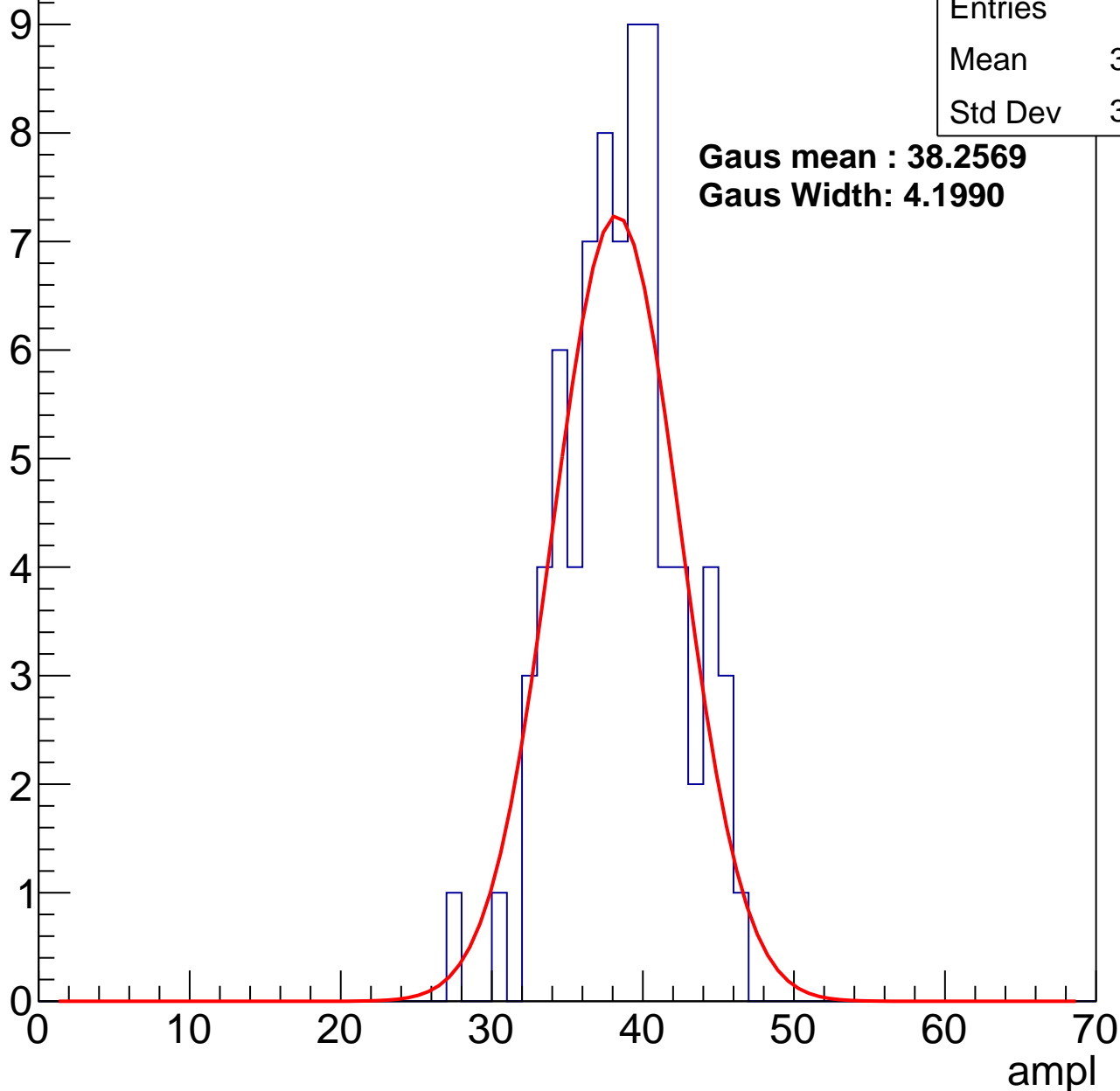
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	38.04
Std Dev	3.798

**Gaus mean : 38.2569**

**Gaus Width: 4.1990**



# B1L103S, U16-ch3, adc2

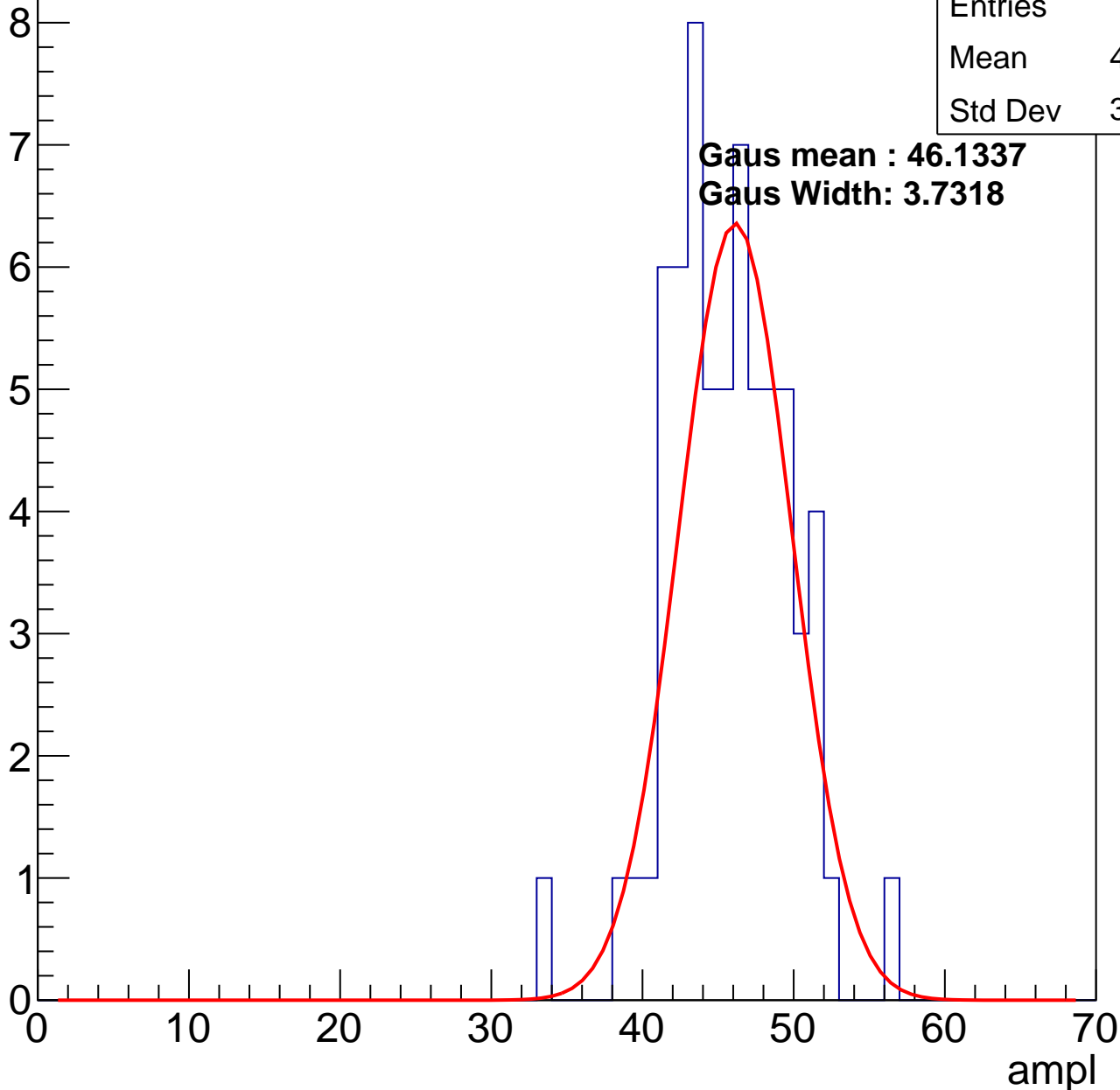
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	45.25
Std Dev	3.879

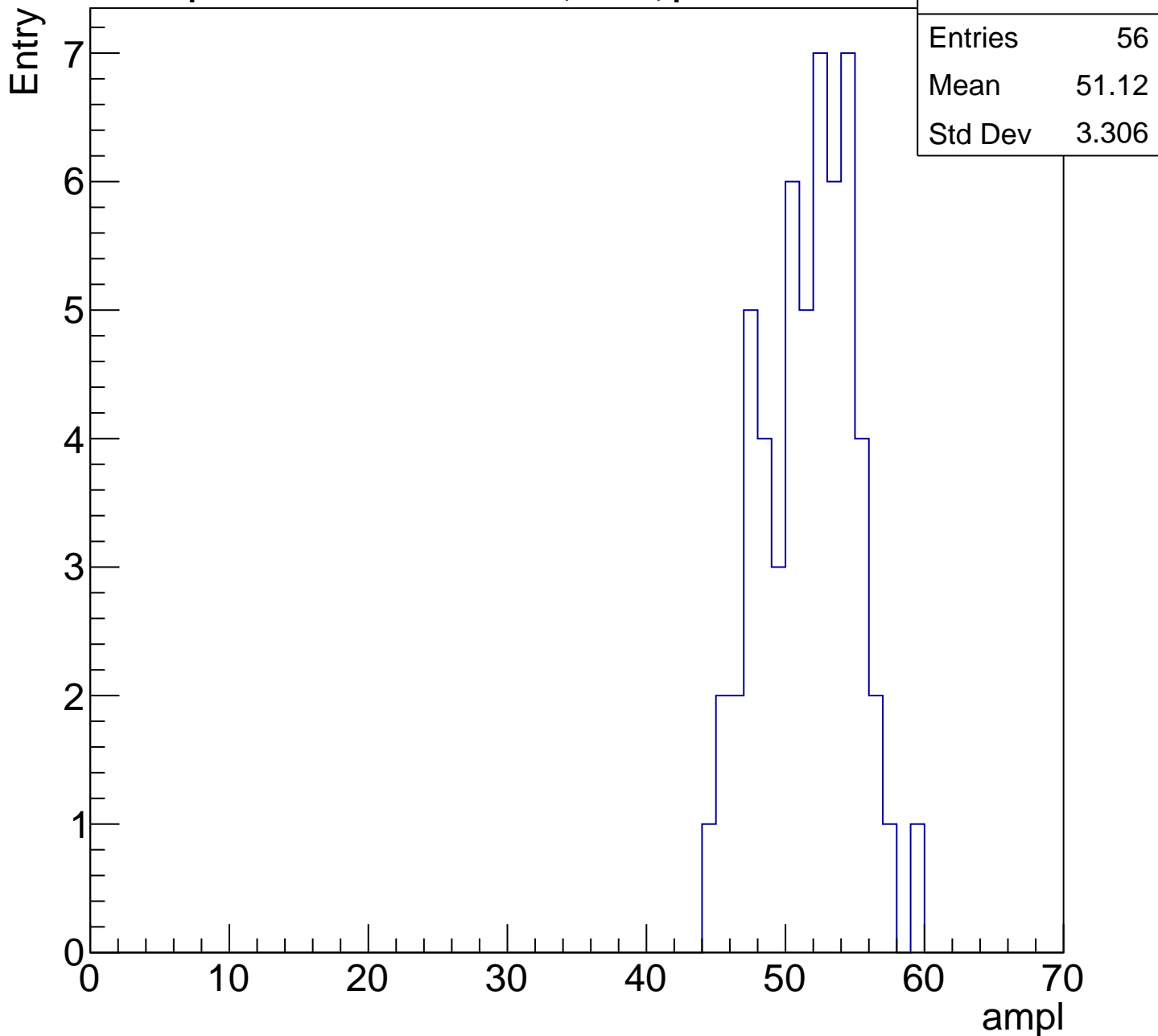
**Gaus mean : 46.1337**

**Gaus Width: 3.7318**



# B1L103S, U16-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

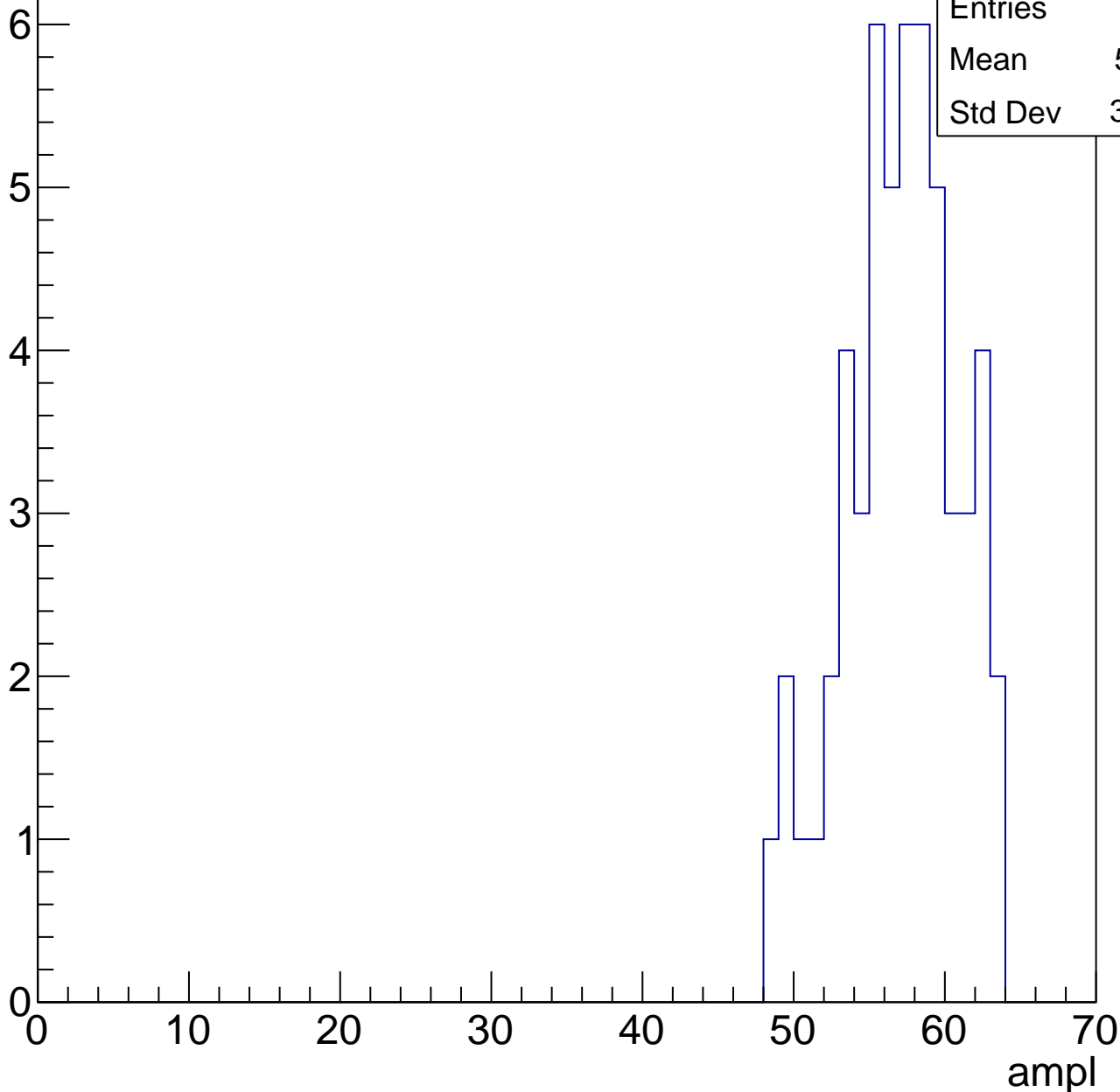


# B1L103S, U16-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	56.61
Std Dev	3.674



# B1L103S, U16-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

7

6

5

4

3

2

1

0

Entries

41

Mean

58.8

Std Dev

9.518

ampl

0

10

20

30

40

50

60

70

# B1L103S, U16-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

1

Mean

63

Std Dev

0



# B1L103S, U16-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U16-ch4, adc0

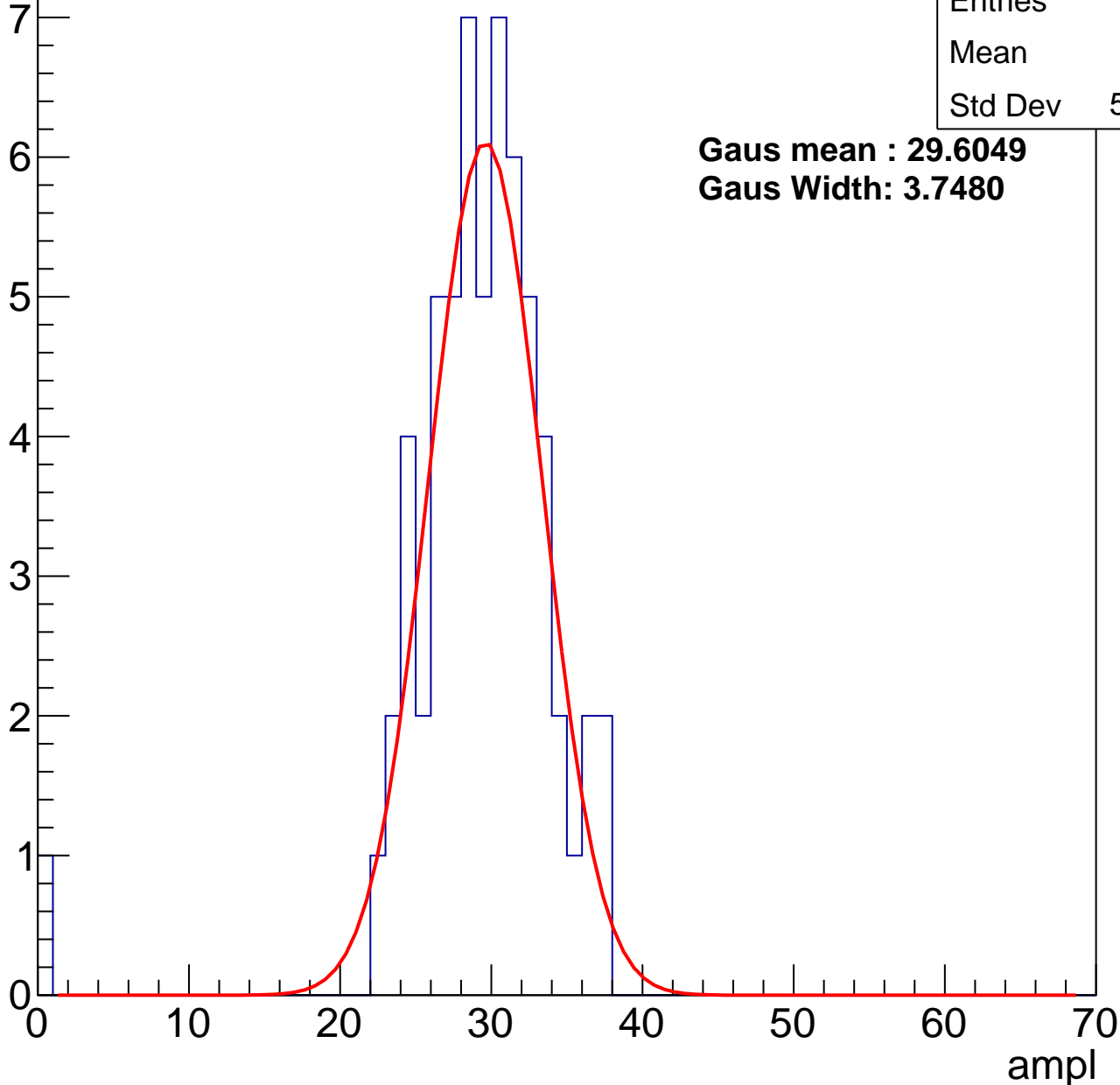
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	28.8
Std Dev	5.146

**Gaus mean : 29.6049**

**Gaus Width: 3.7480**



# B1L103S, U16-ch4, adc1

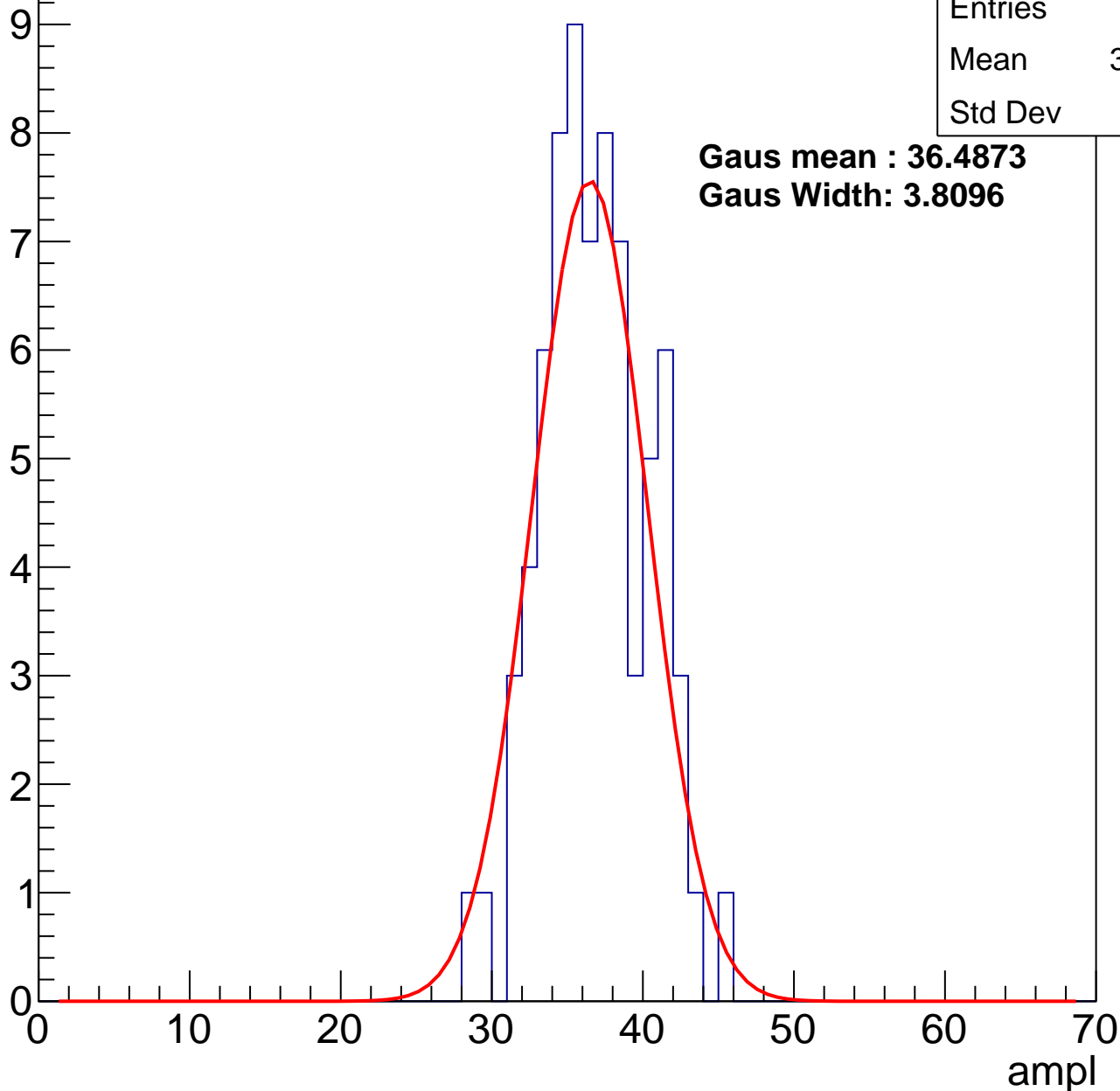
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	36.36
Std Dev	3.45

**Gaus mean : 36.4873**

**Gaus Width: 3.8096**



# B1L103S, U16-ch4, adc2

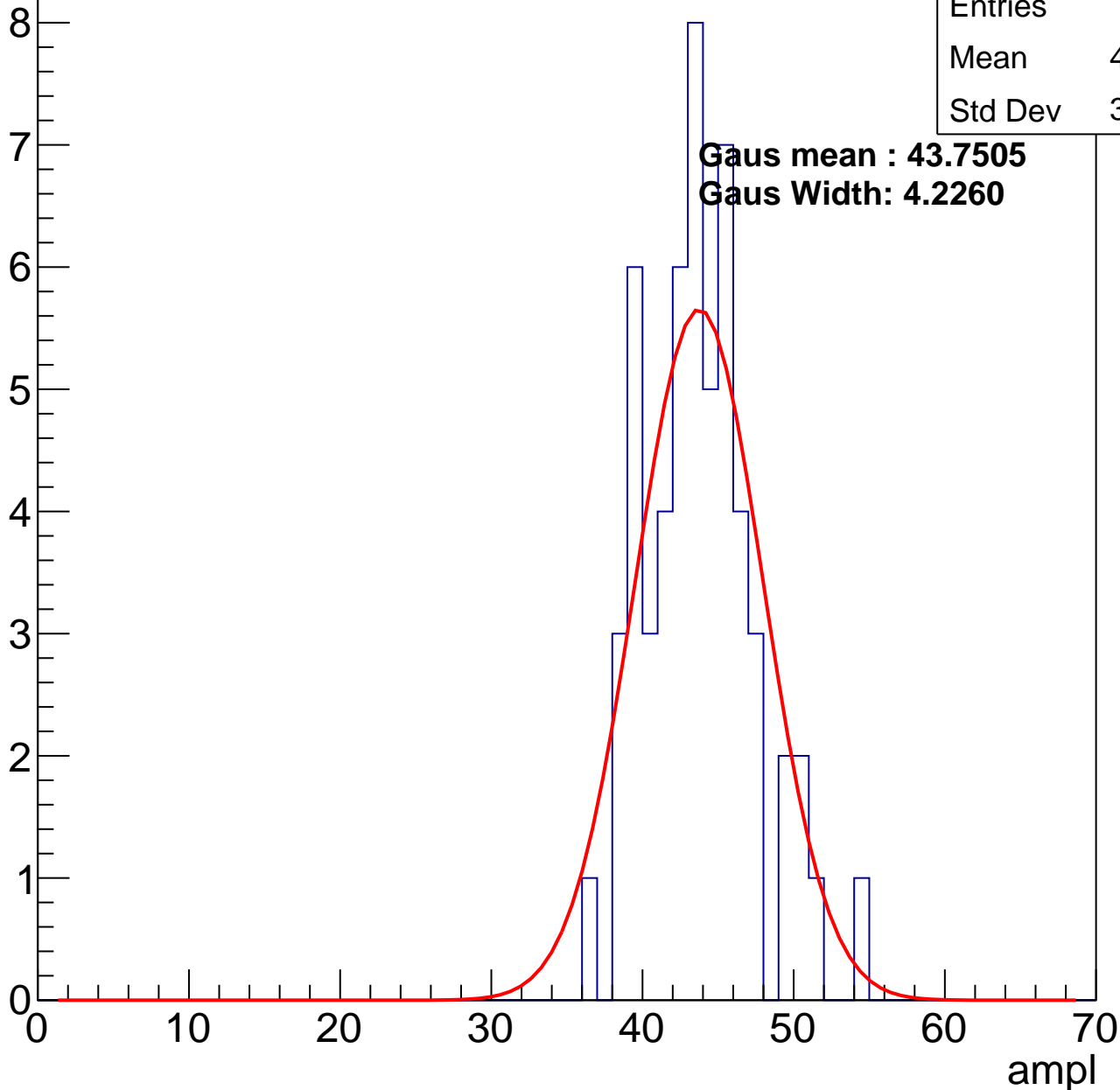
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	43.34
Std Dev	3.622

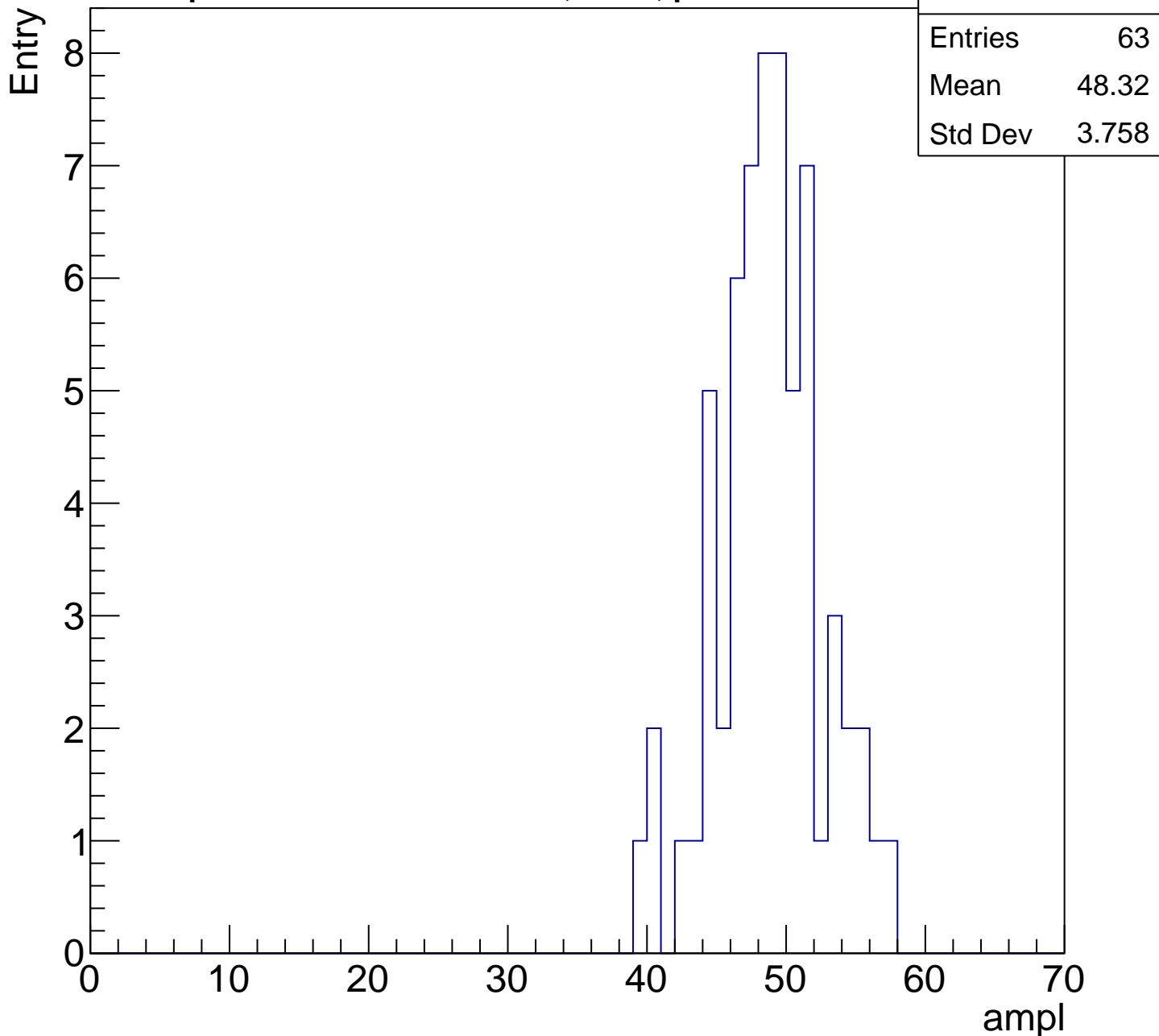
**Gaus mean : 43.7505**

**Gaus Width: 4.2260**



# B1L103S, U16-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

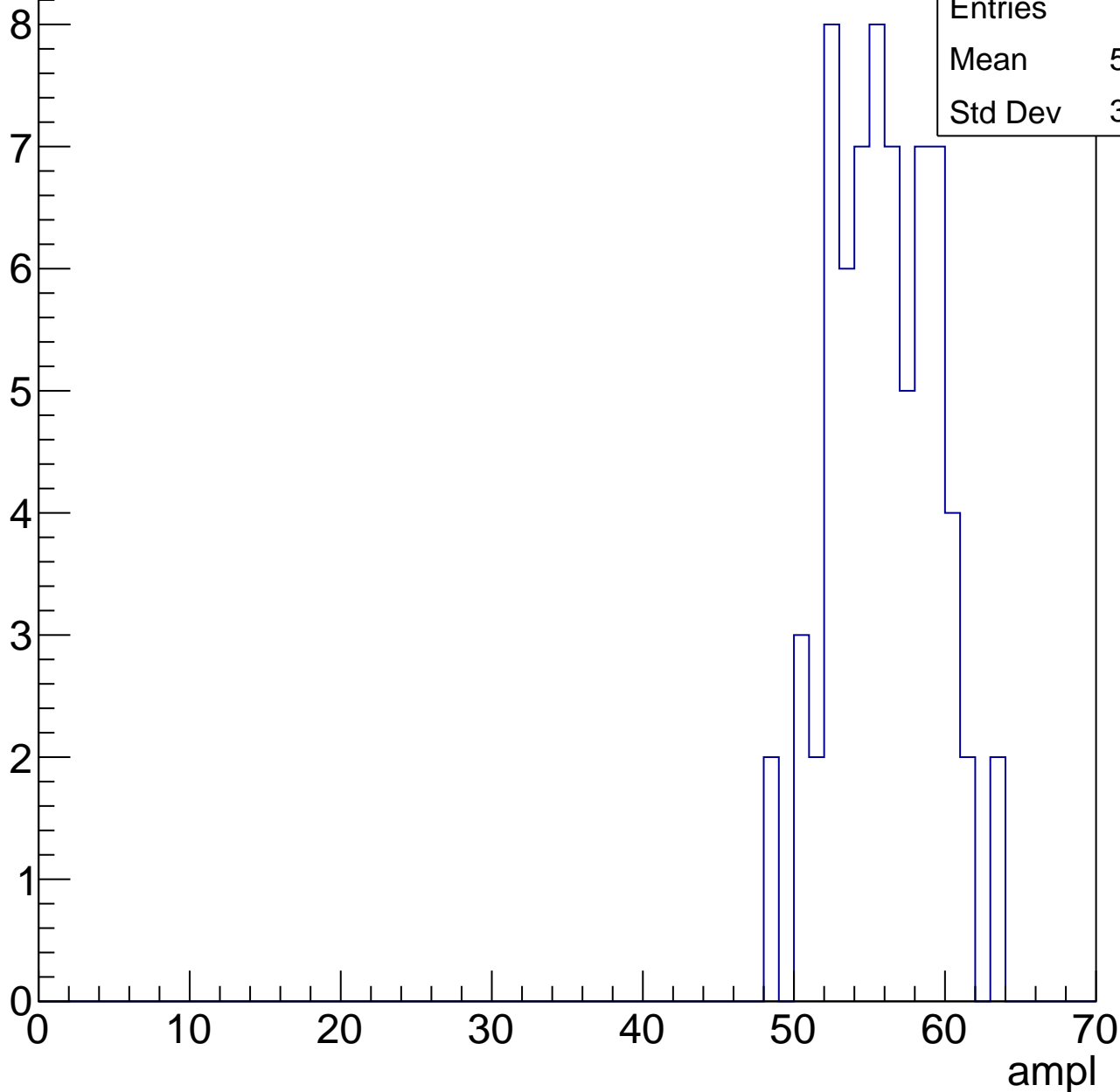


# B1L103S, U16-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	55.49
Std Dev	3.367

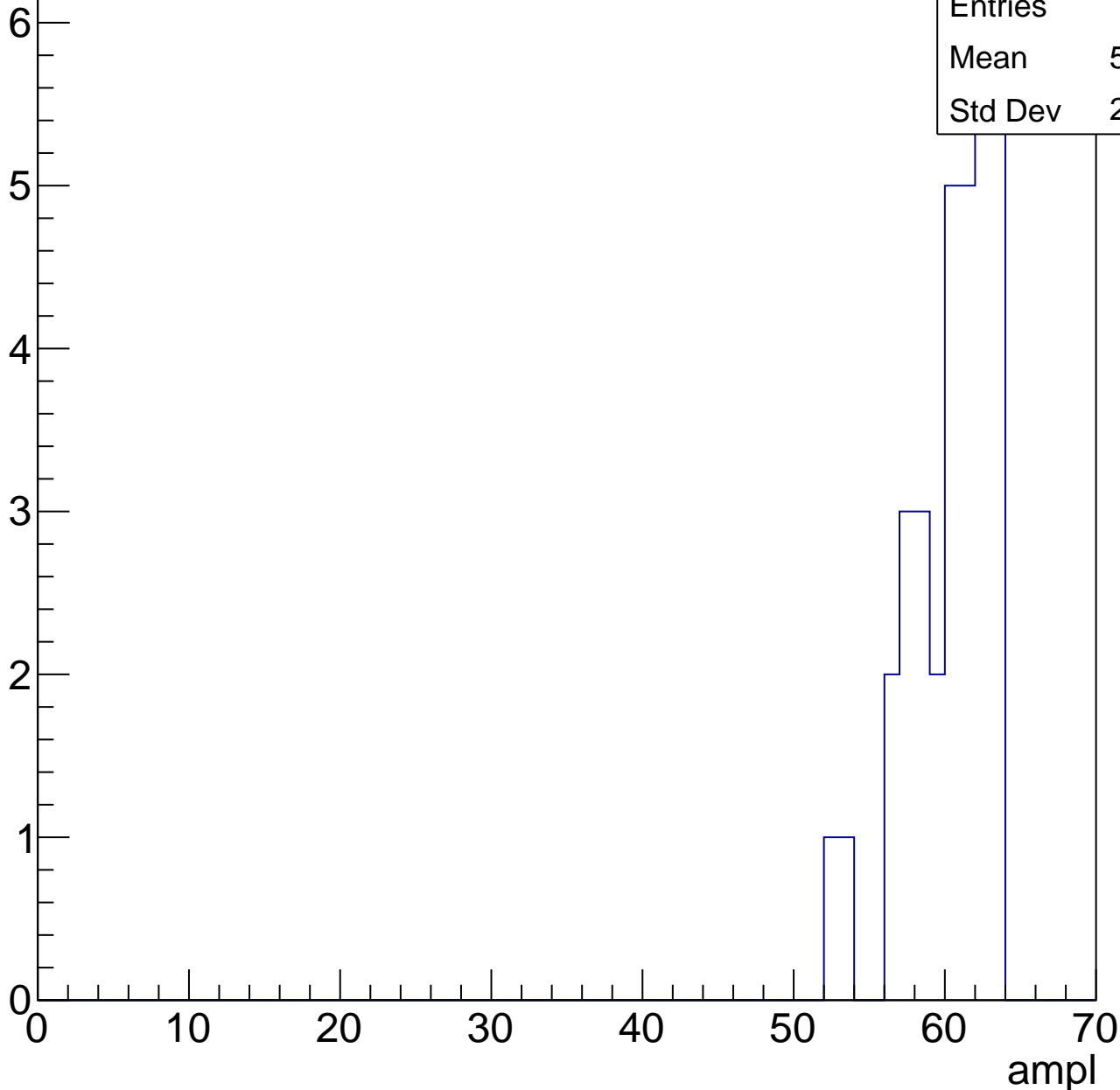


# B1L103S, U16-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

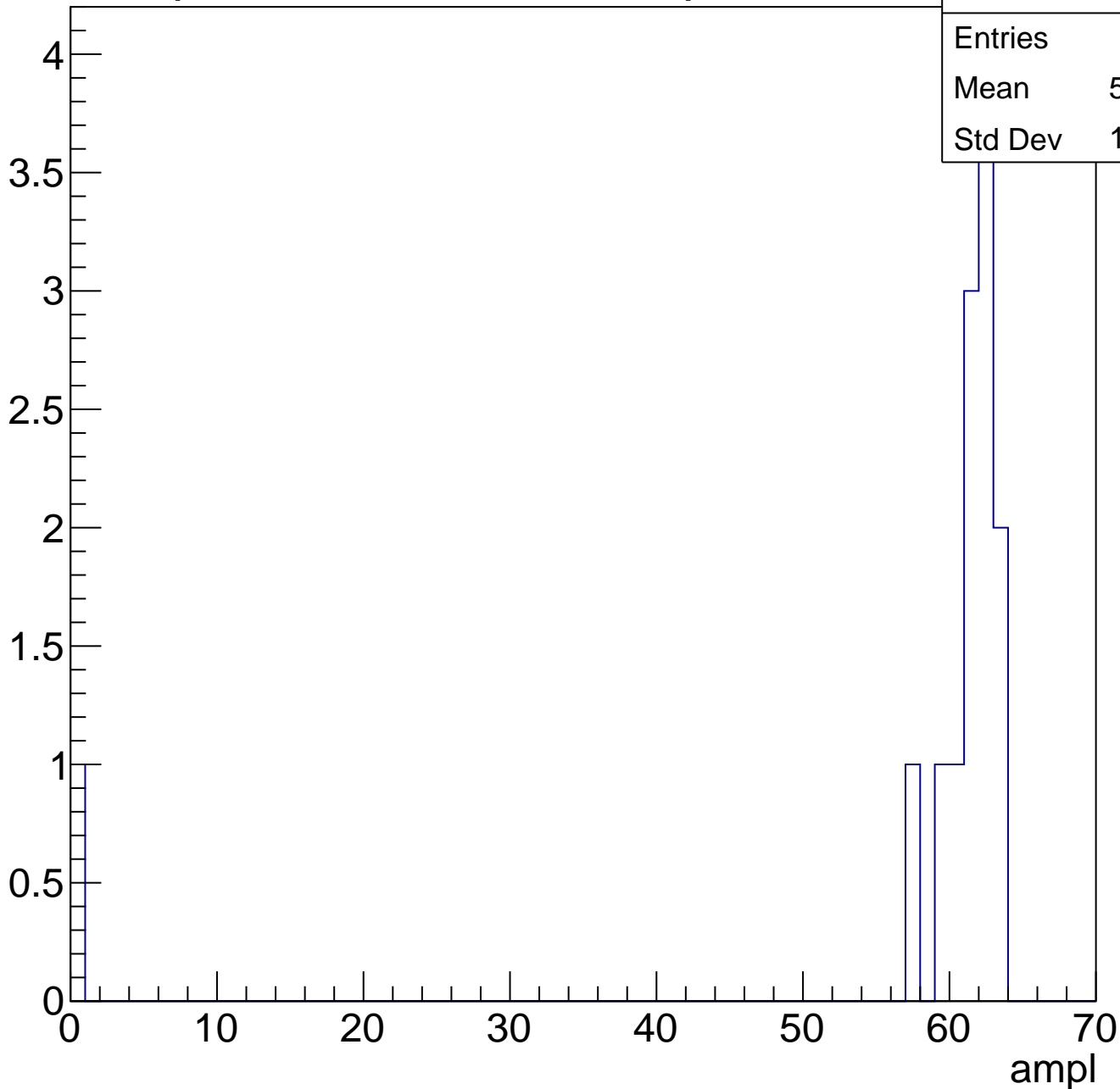
Entries	34
Mean	59.85
Std Dev	2.809



# B1L103S, U16-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	20
Std Dev	0

ampl

# B1L103S, U16-ch5, adc0

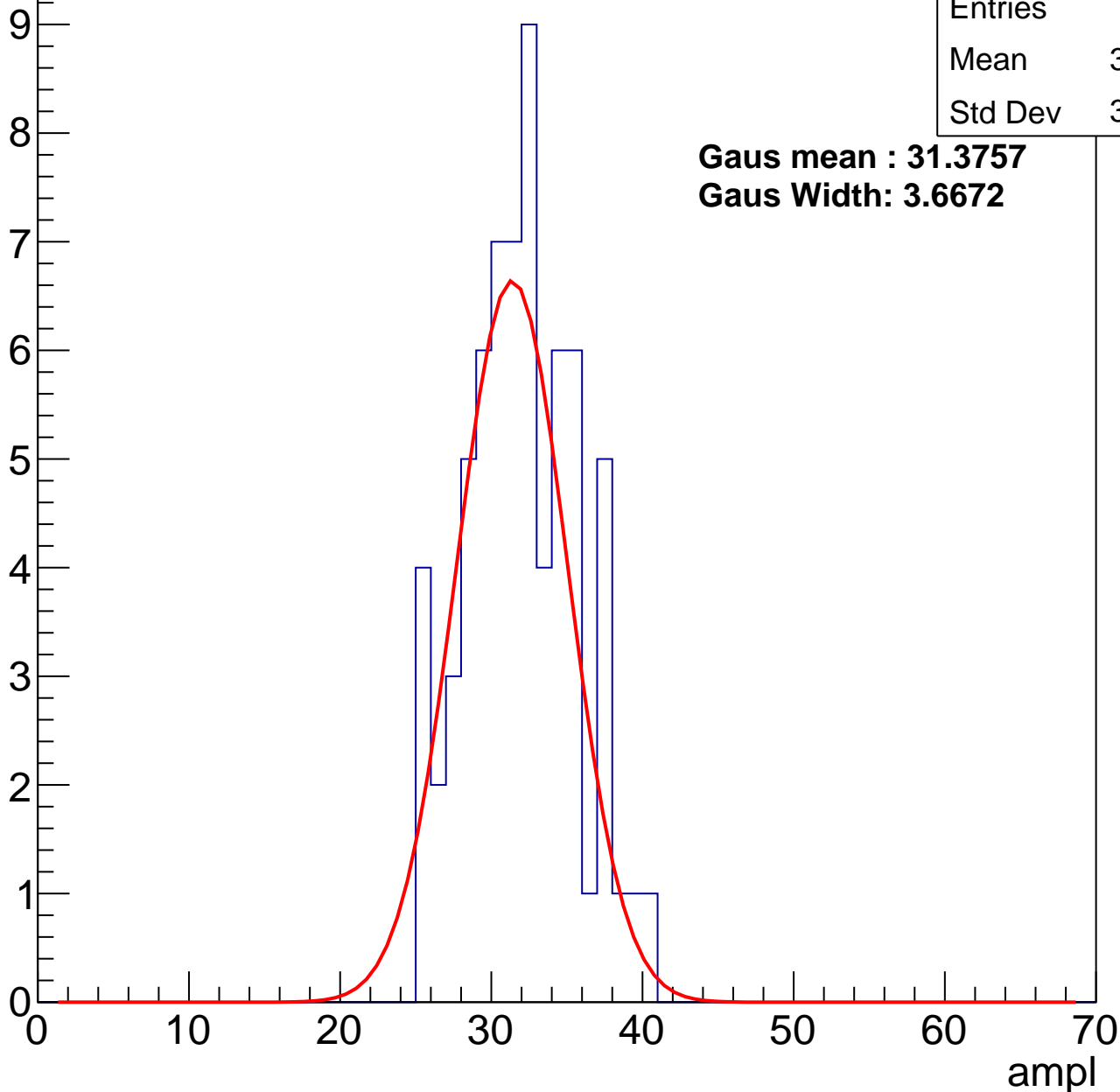
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	31.56
Std Dev	3.578

**Gaus mean : 31.3757**

**Gaus Width: 3.6672**



# B1L103S, U16-ch5, adc1

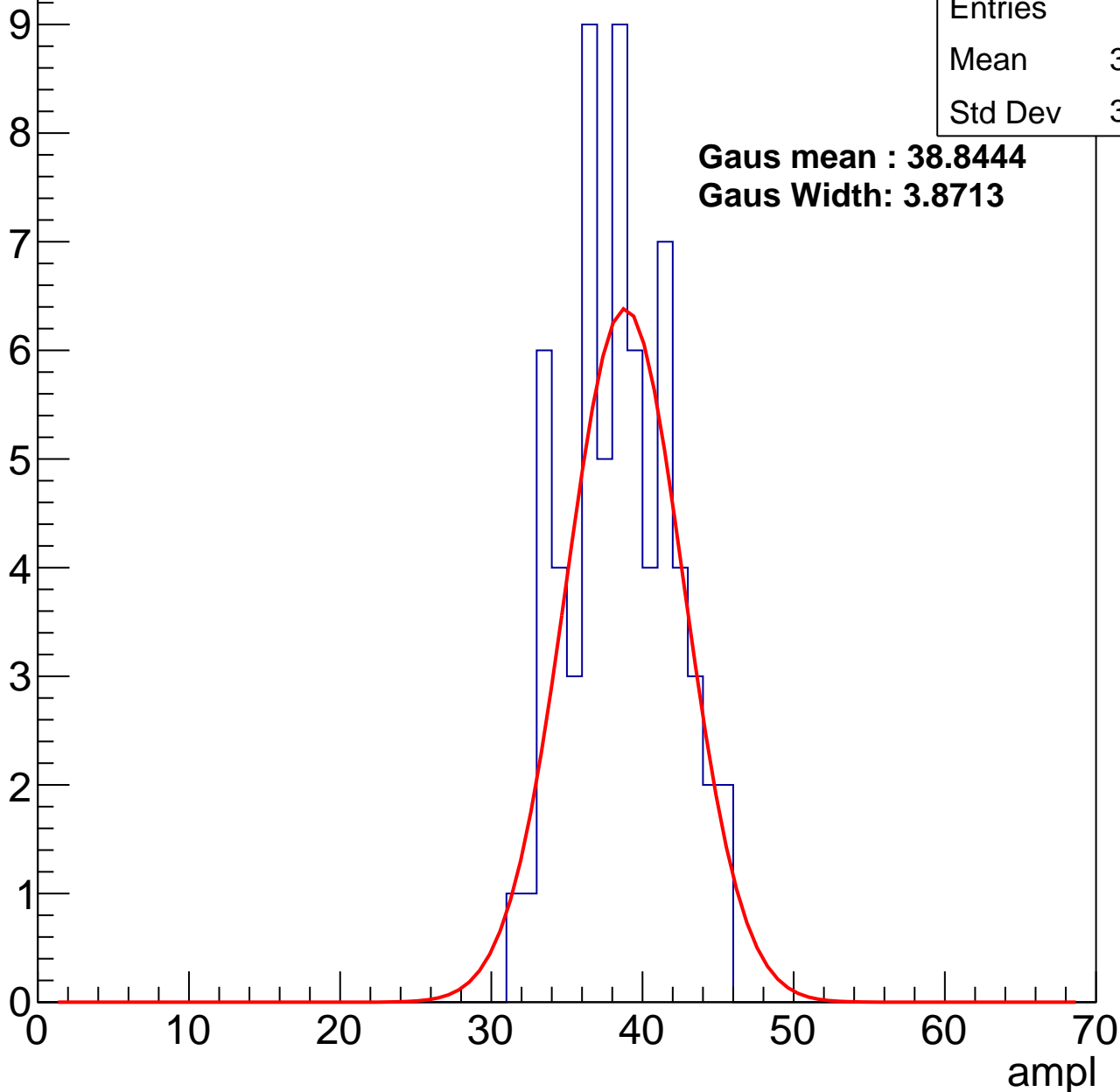
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	38.02
Std Dev	3.396

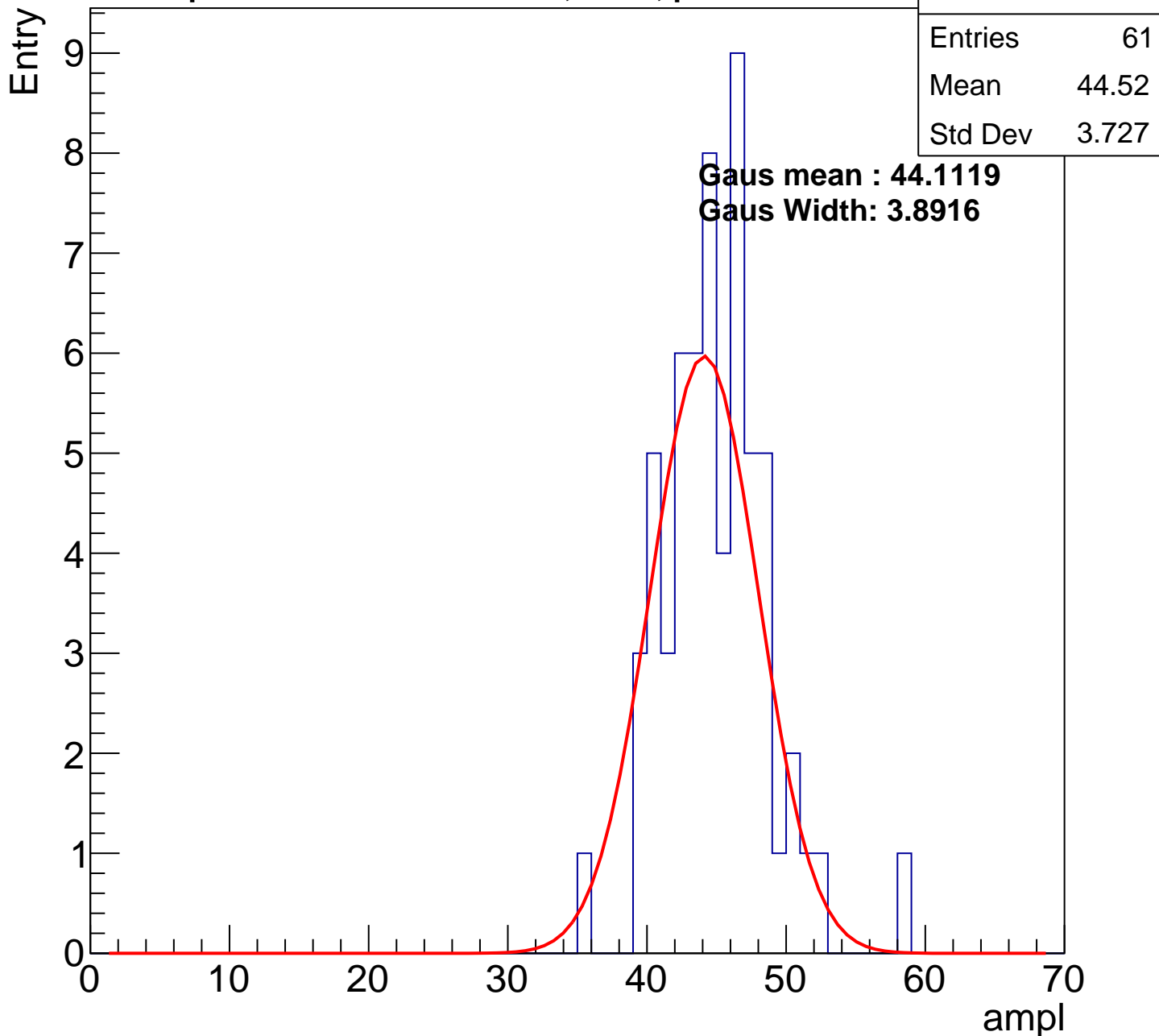
**Gaus mean : 38.8444**

**Gaus Width: 3.8713**



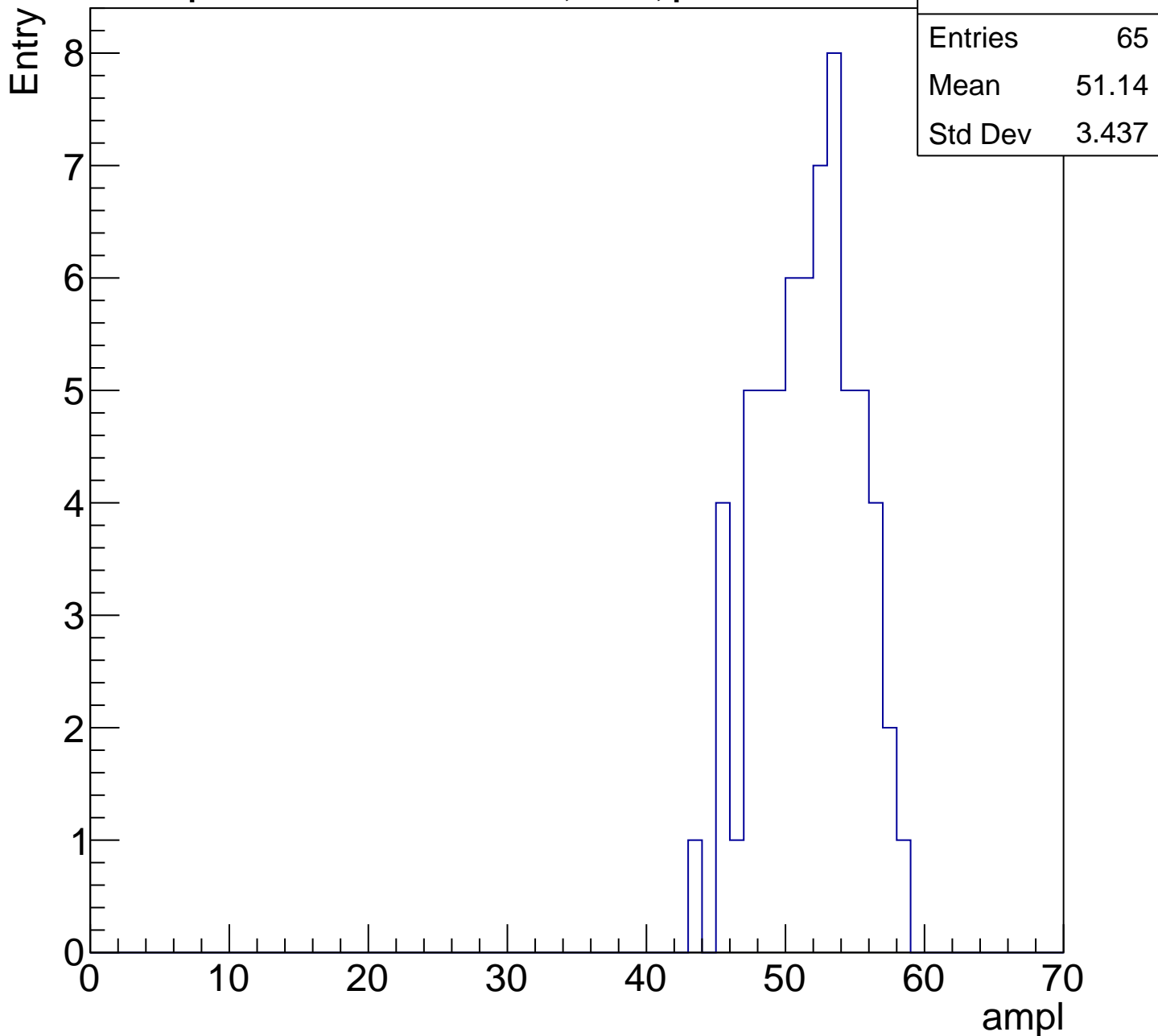
# B1L103S, U16-ch5, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U16-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

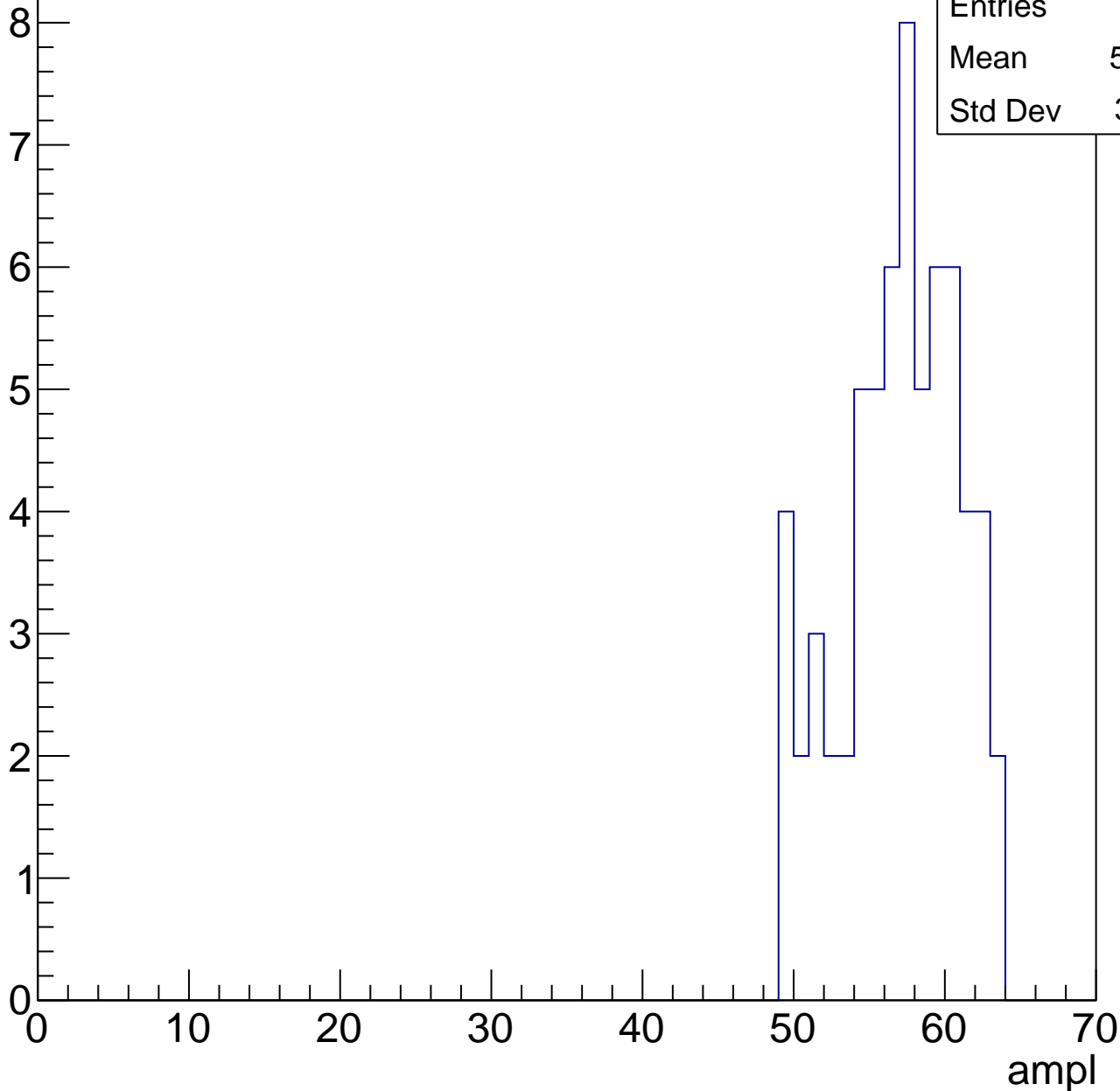


# B1L103S, U16-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	56.53
Std Dev	3.791

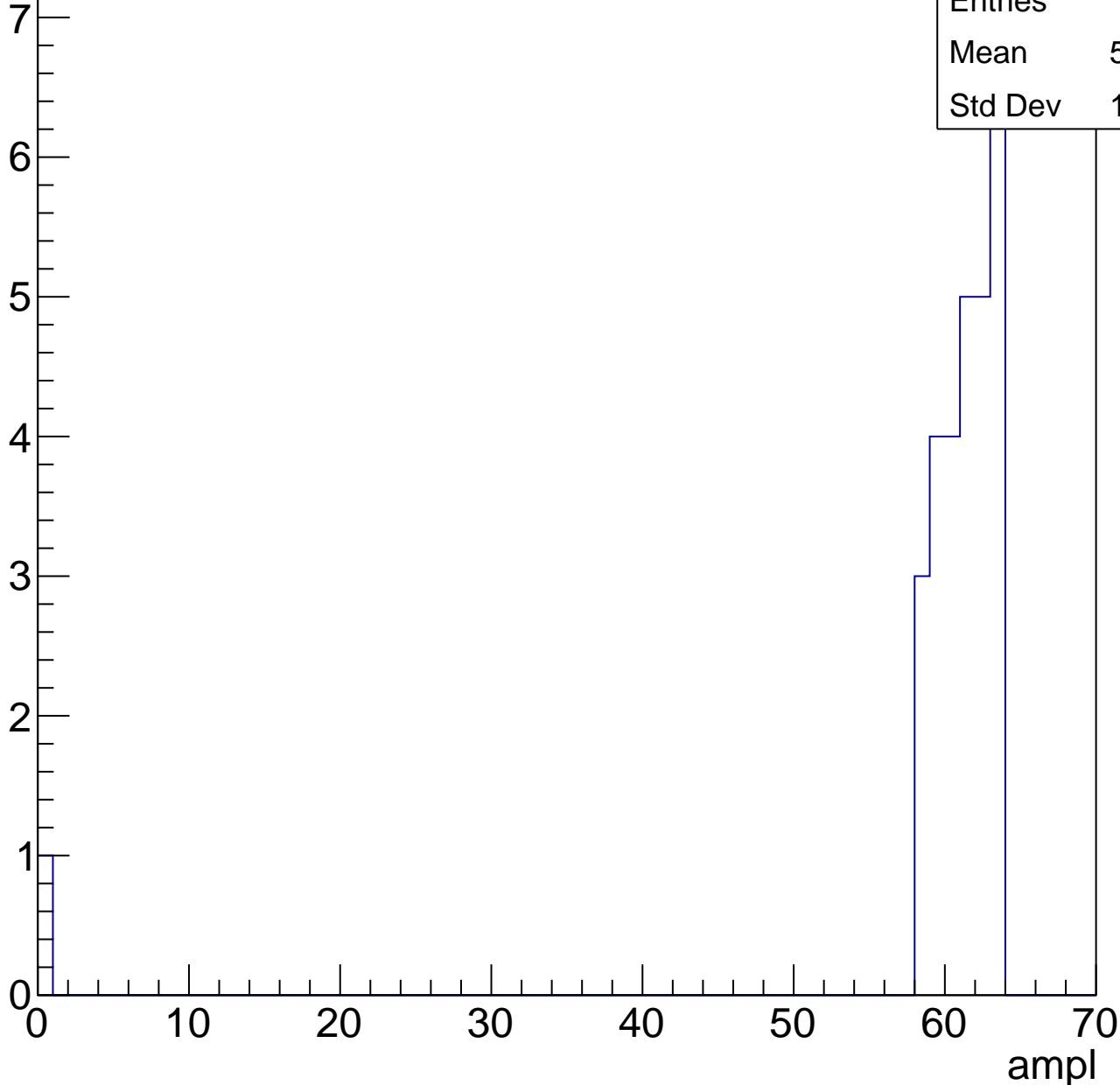


# B1L103S, U16-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

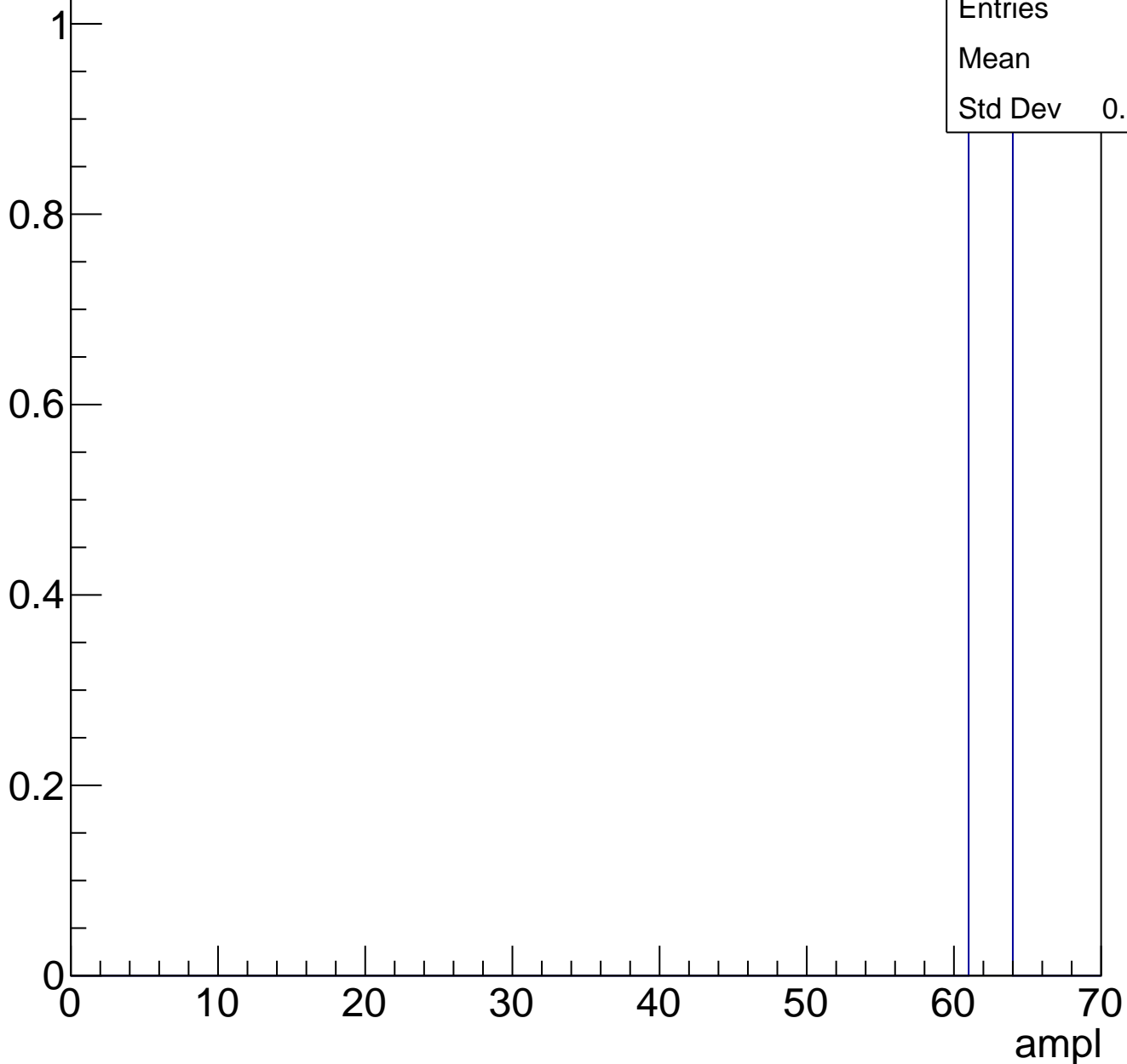
Entries	29
Mean	58.83
Std Dev	11.24



# B1L103S, U16-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U16-ch6, adc0

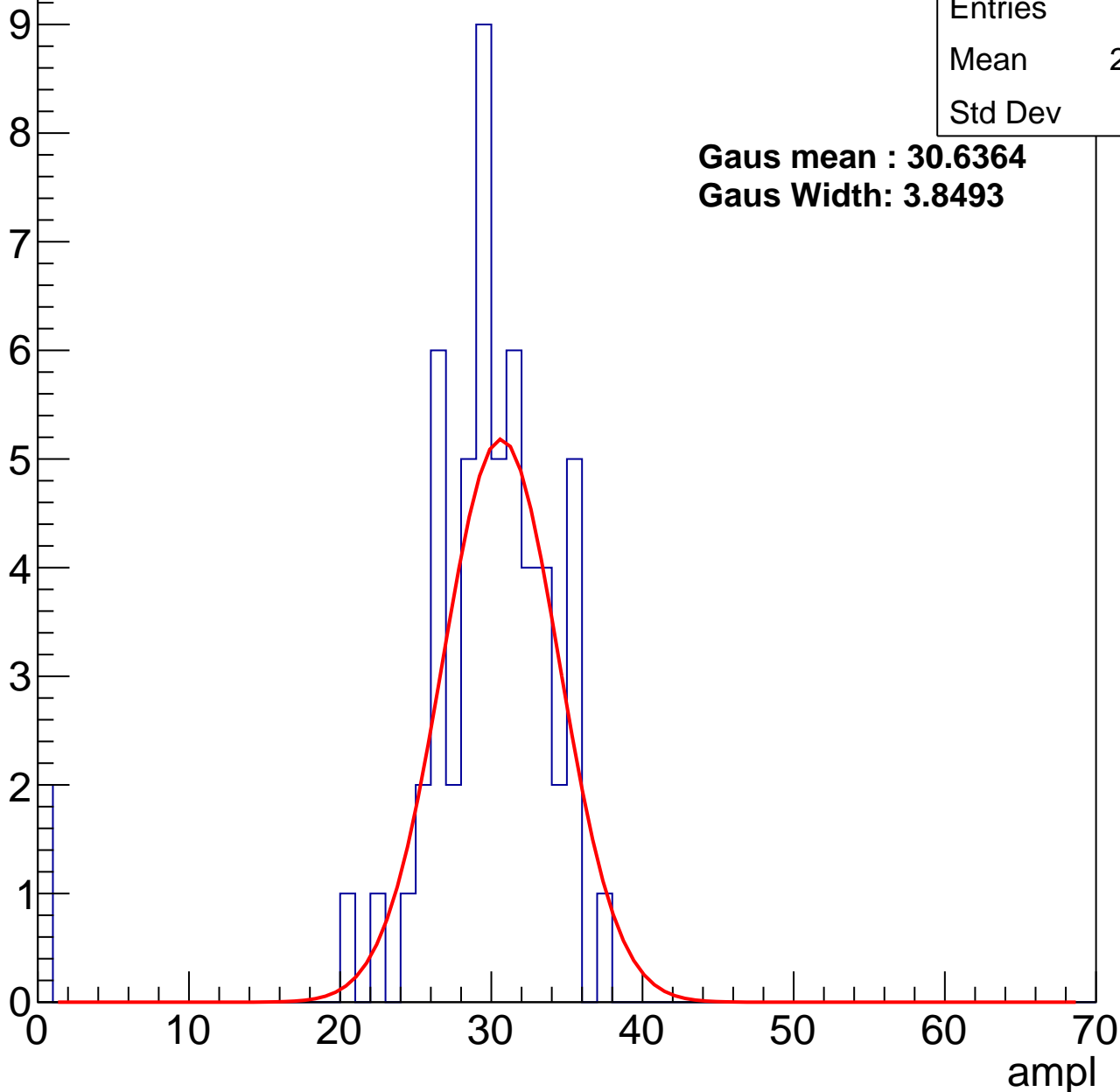
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	28.62
Std Dev	6.48

**Gaus mean : 30.6364**

**Gaus Width: 3.8493**



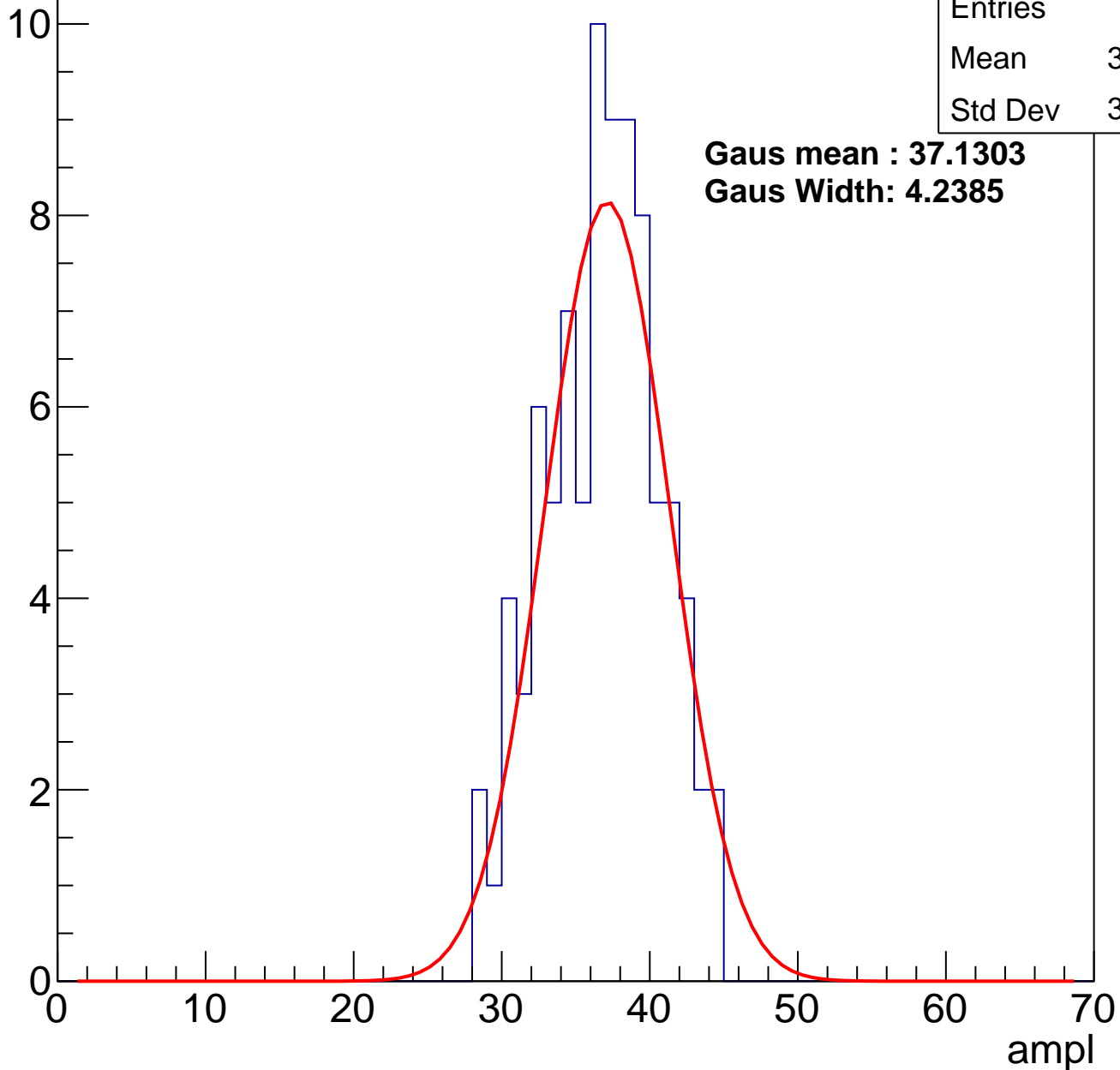
# B1L103S, U16-ch6, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	87
Mean	36.34
Std Dev	3.793

**Gaus mean : 37.1303**  
**Gaus Width: 4.2385**

Entry



# B1L103S, U16-ch6, adc2

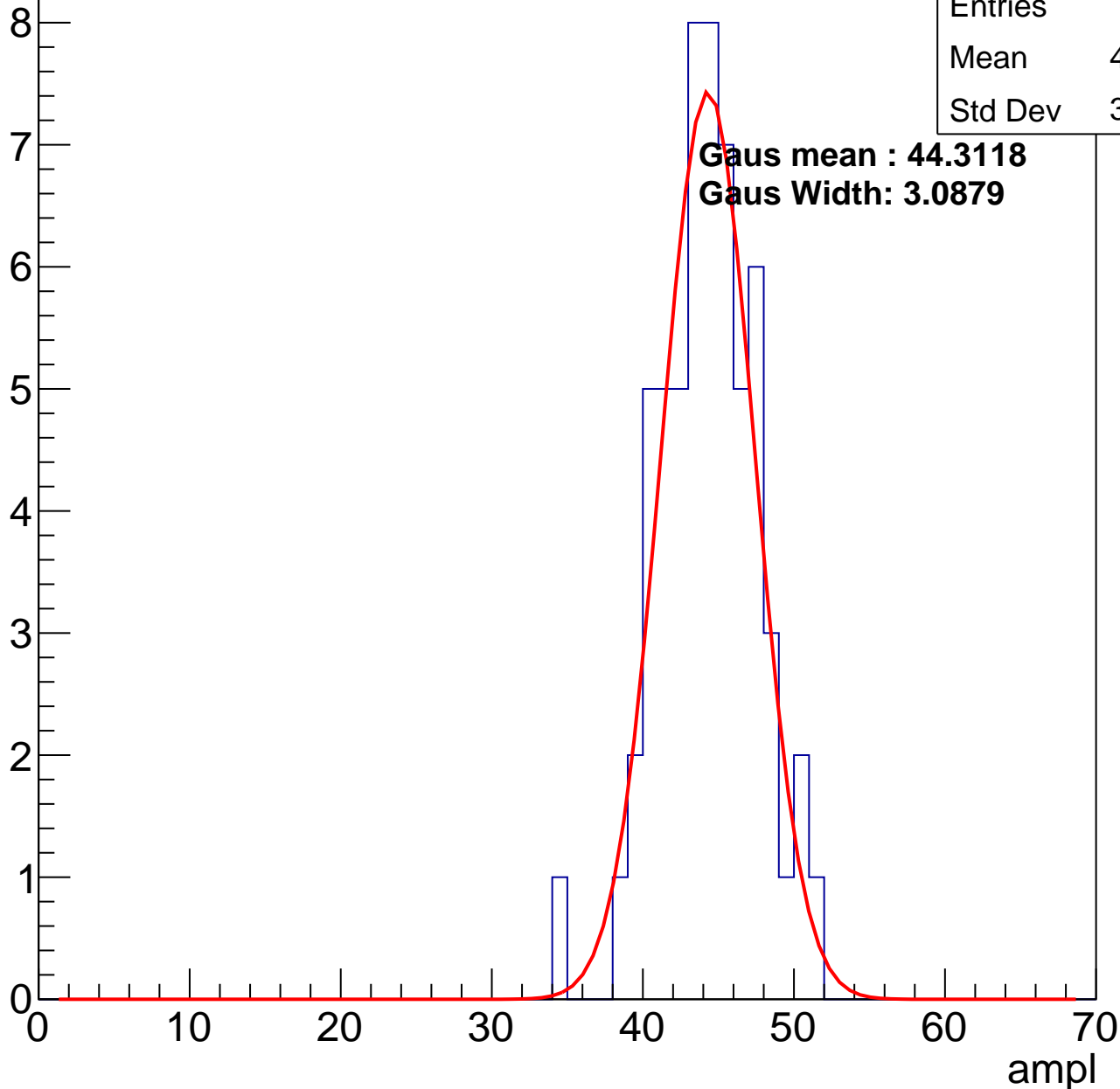
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	43.87
Std Dev	3.196

**Gaus mean : 44.3118**

**Gaus Width: 3.0879**

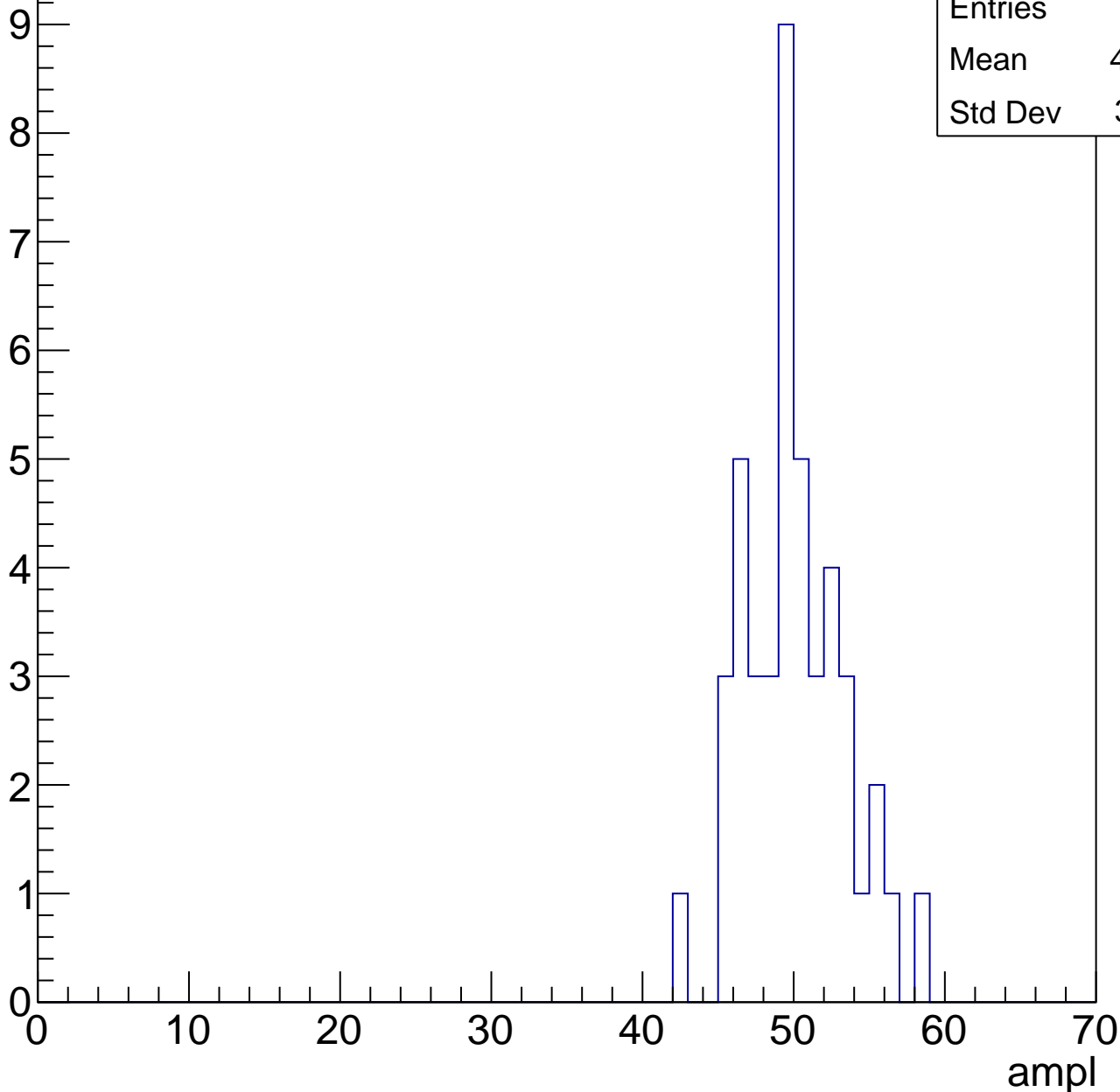


# B1L103S, U16-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	49.57
Std Dev	3.271

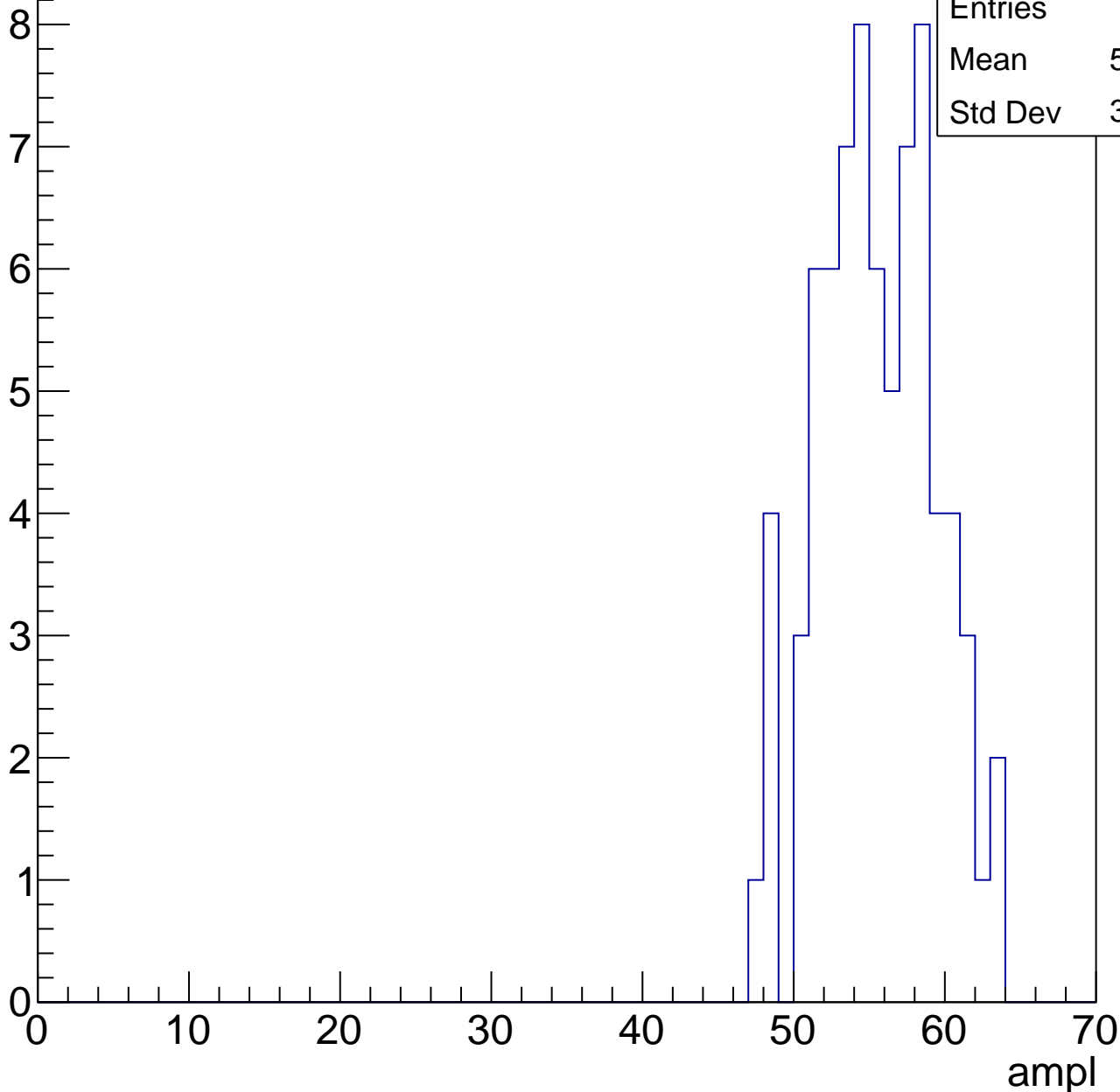


# B1L103S, U16-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	55.07
Std Dev	3.785

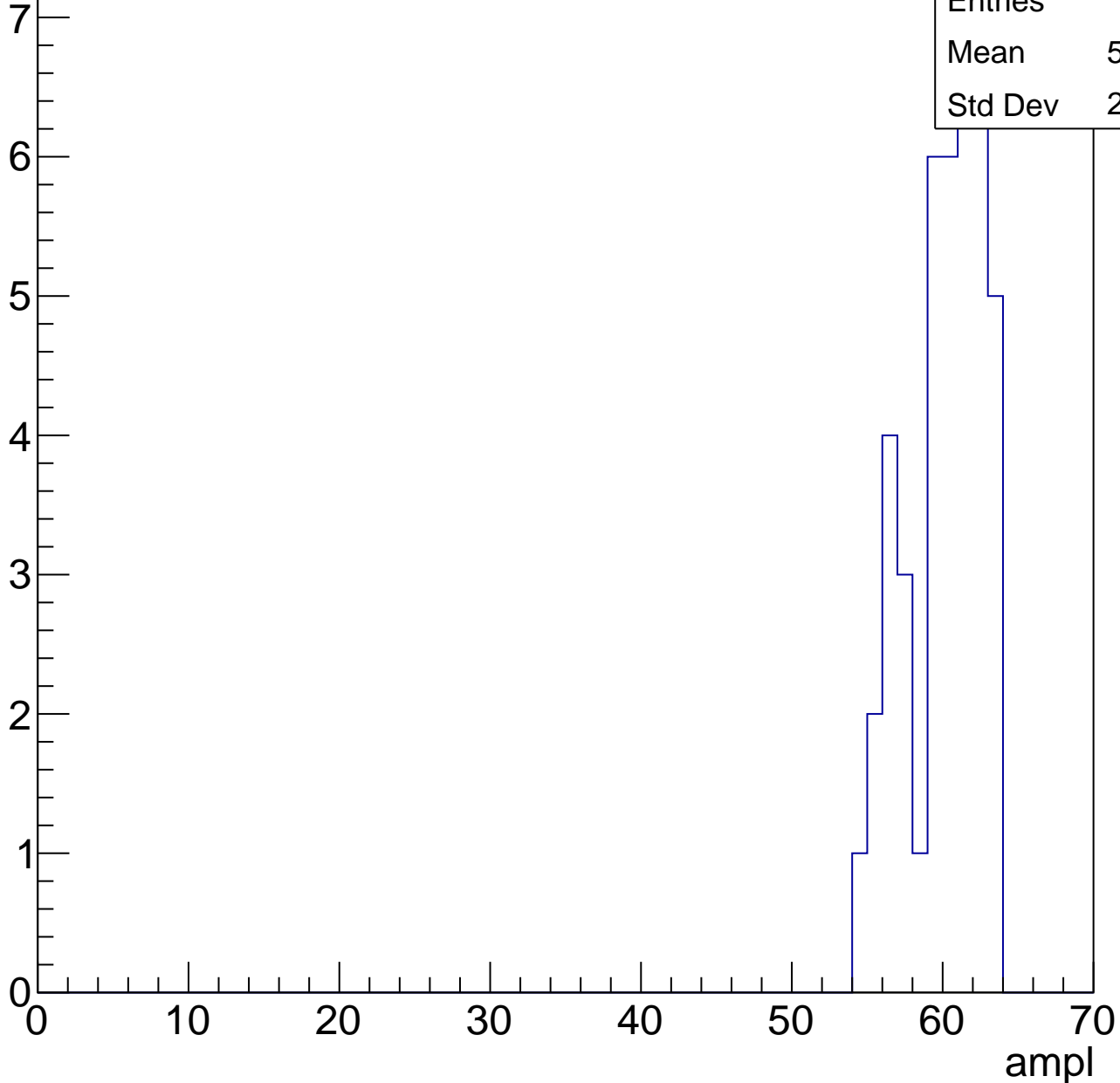


# B1L103S, U16-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	42
Mean	59.69
Std Dev	2.502



# B1L103S, U16-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

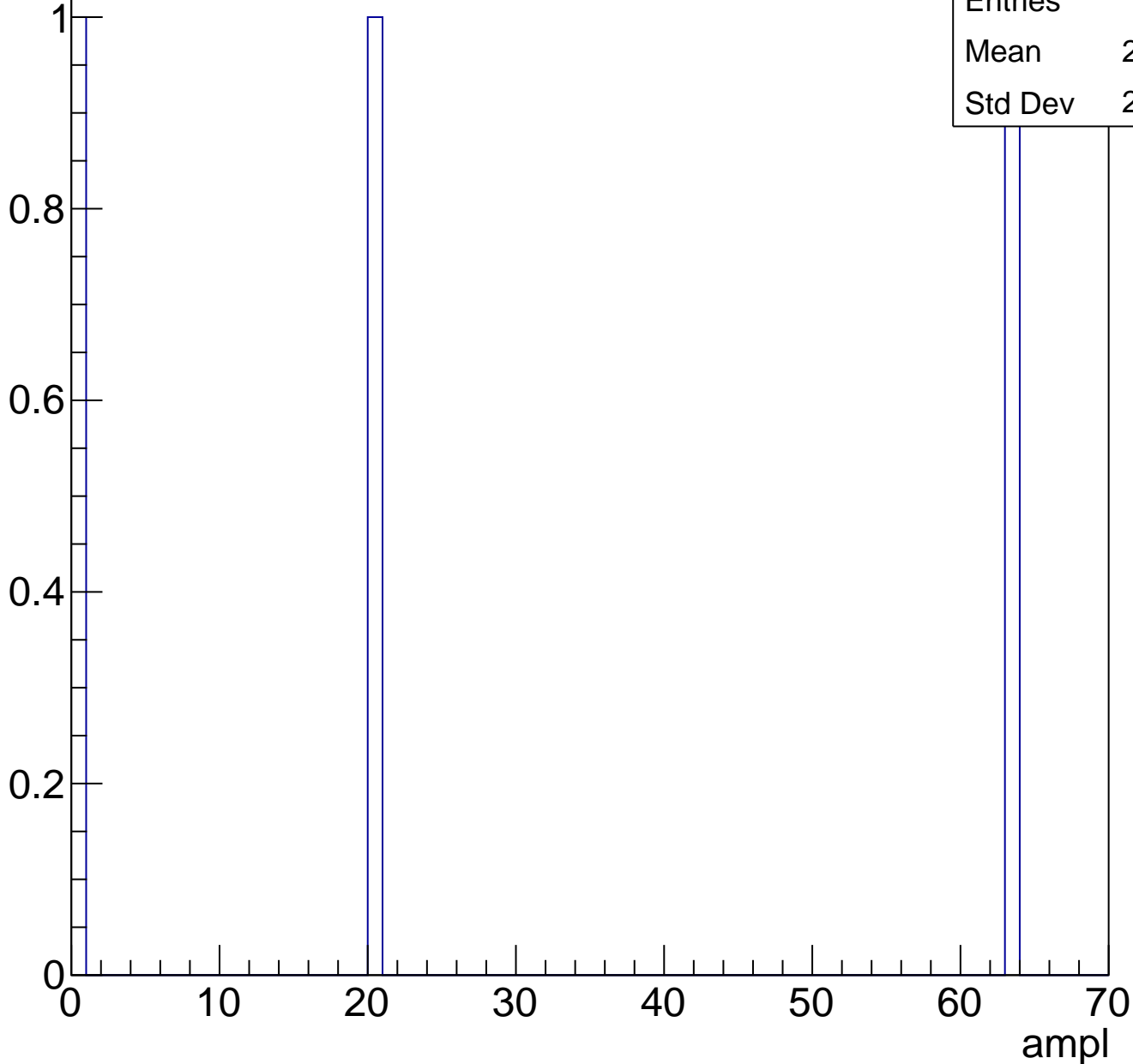




# B1L103S, U16-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch7, adc0

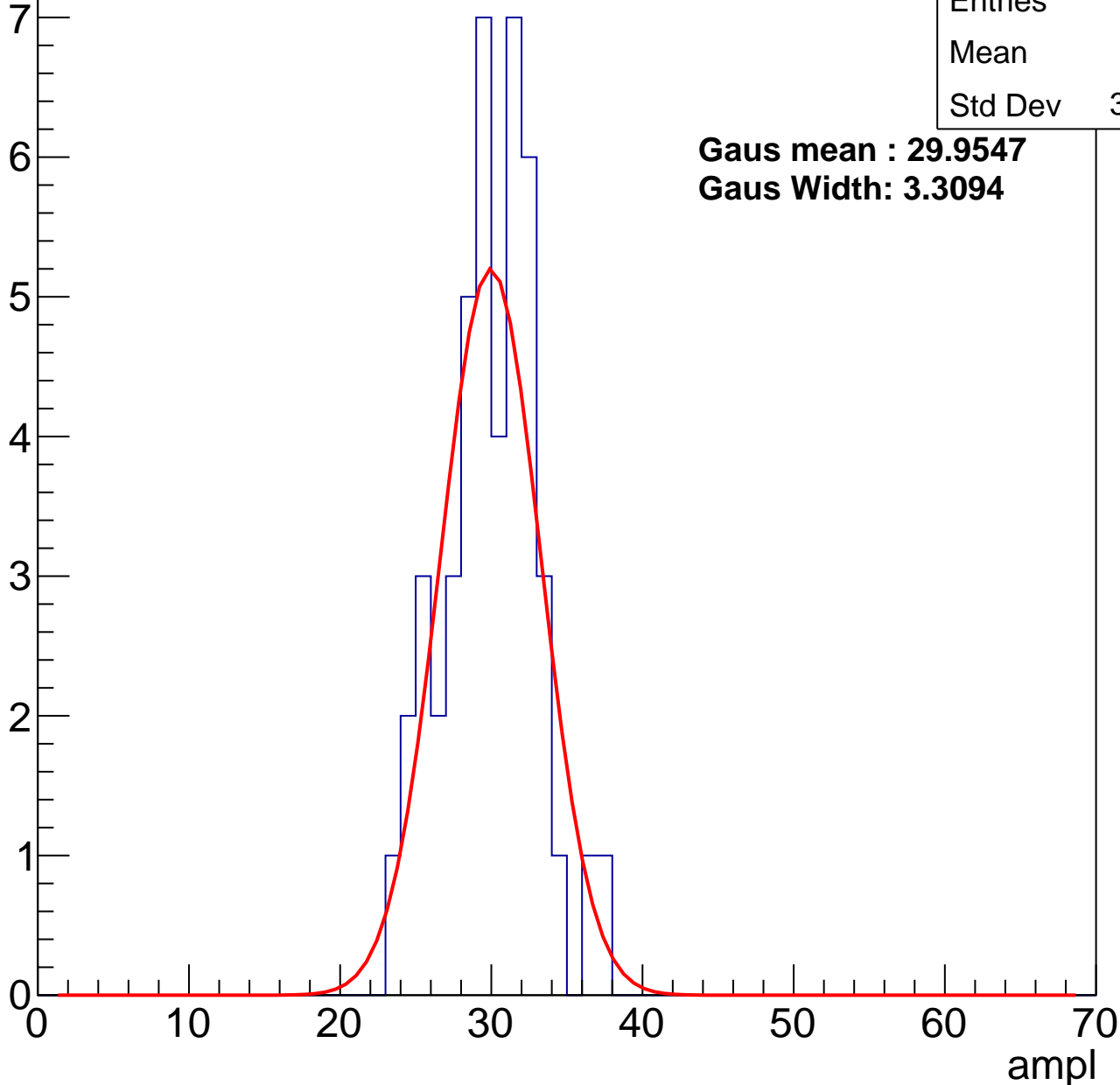
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	29.5
Std Dev	3.056

**Gaus mean : 29.9547**

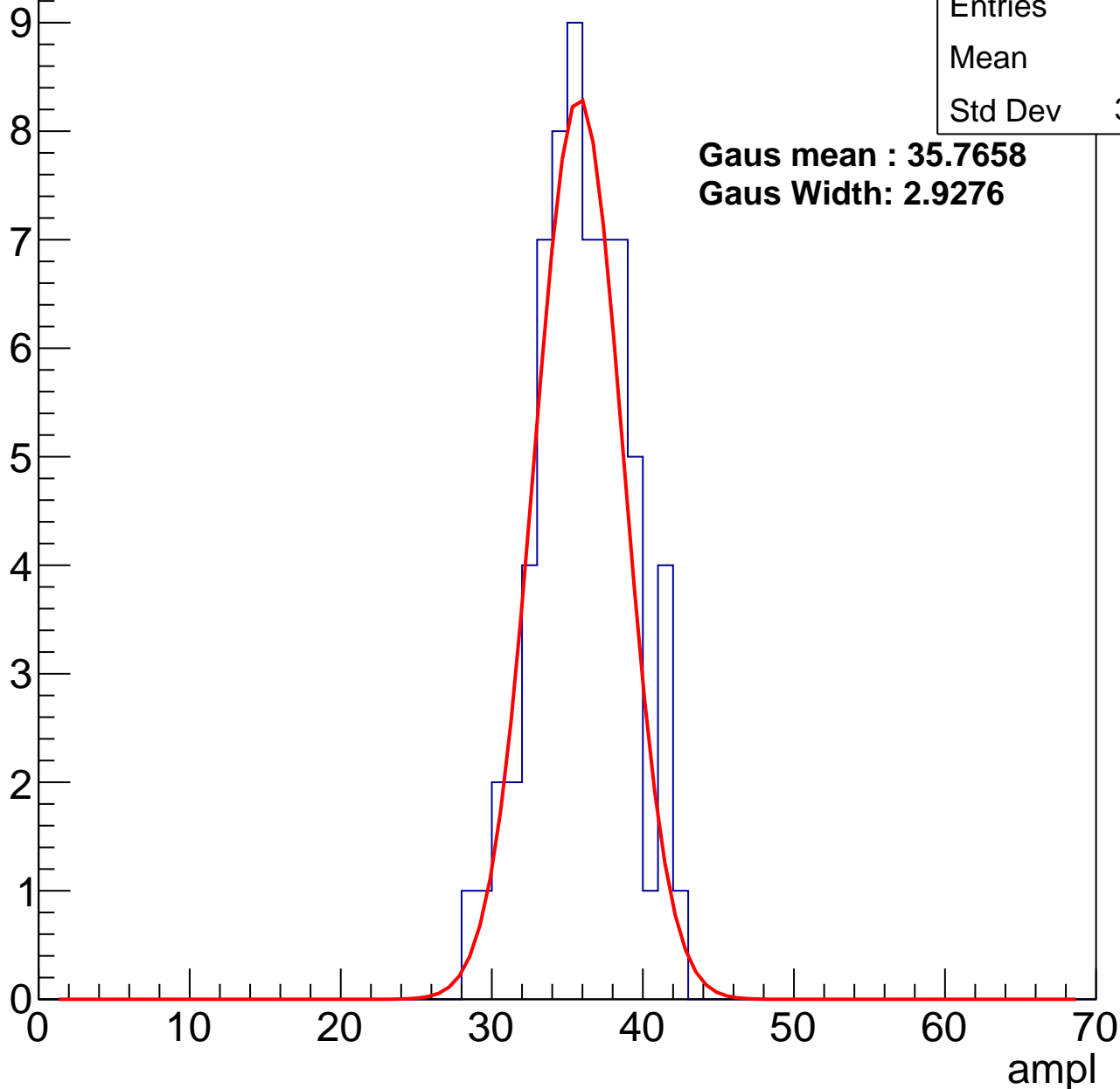
**Gaus Width: 3.3094**



# B1L103S, U16-ch7, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	66
Mean	35.5
Std Dev	3.061

# B1L103S, U16-ch7, adc2

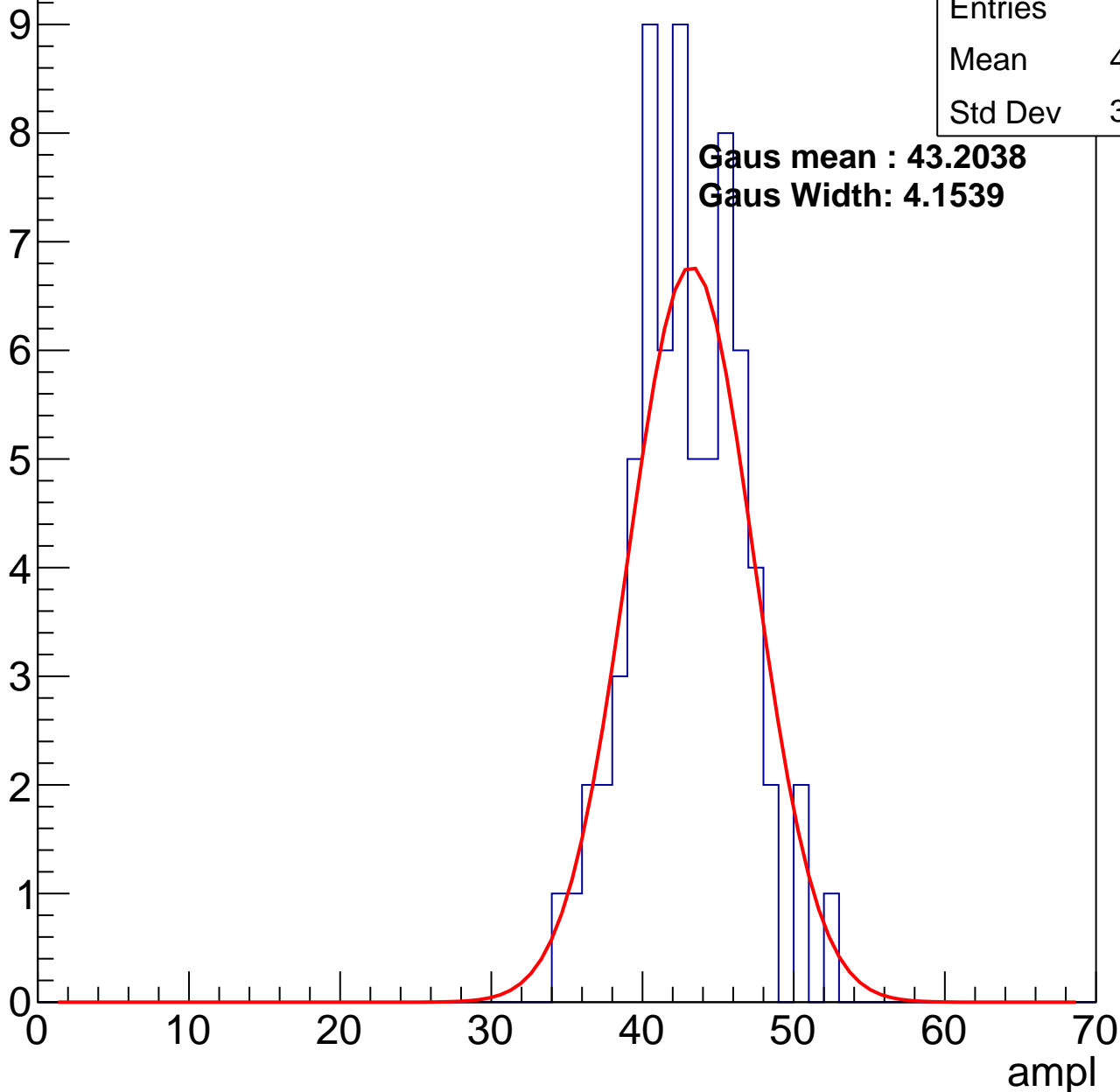
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	42.46
Std Dev	3.653

**Gaus mean : 43.2038**

**Gaus Width: 4.1539**

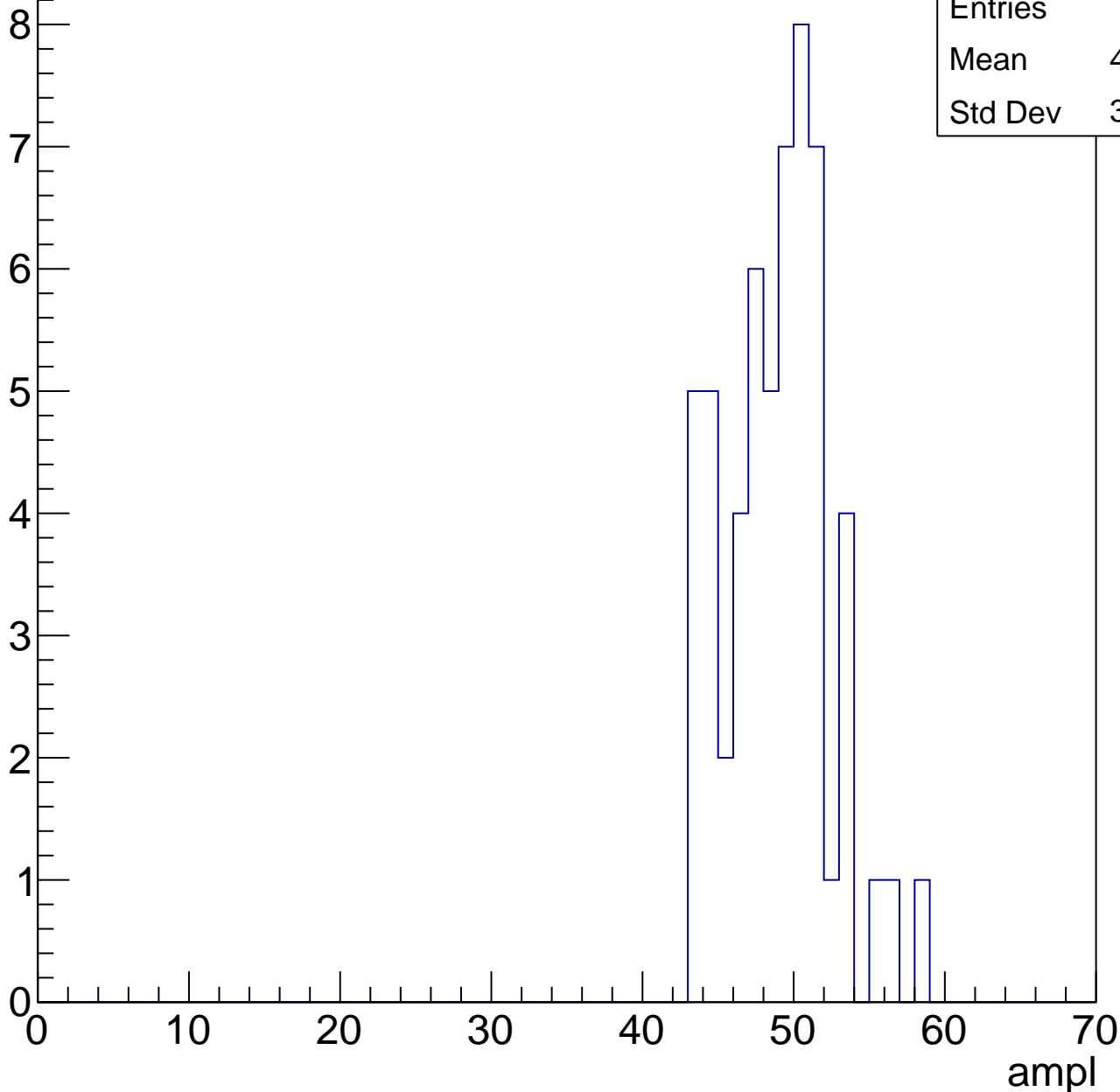


# B1L103S, U16-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	48.49
Std Dev	3.409

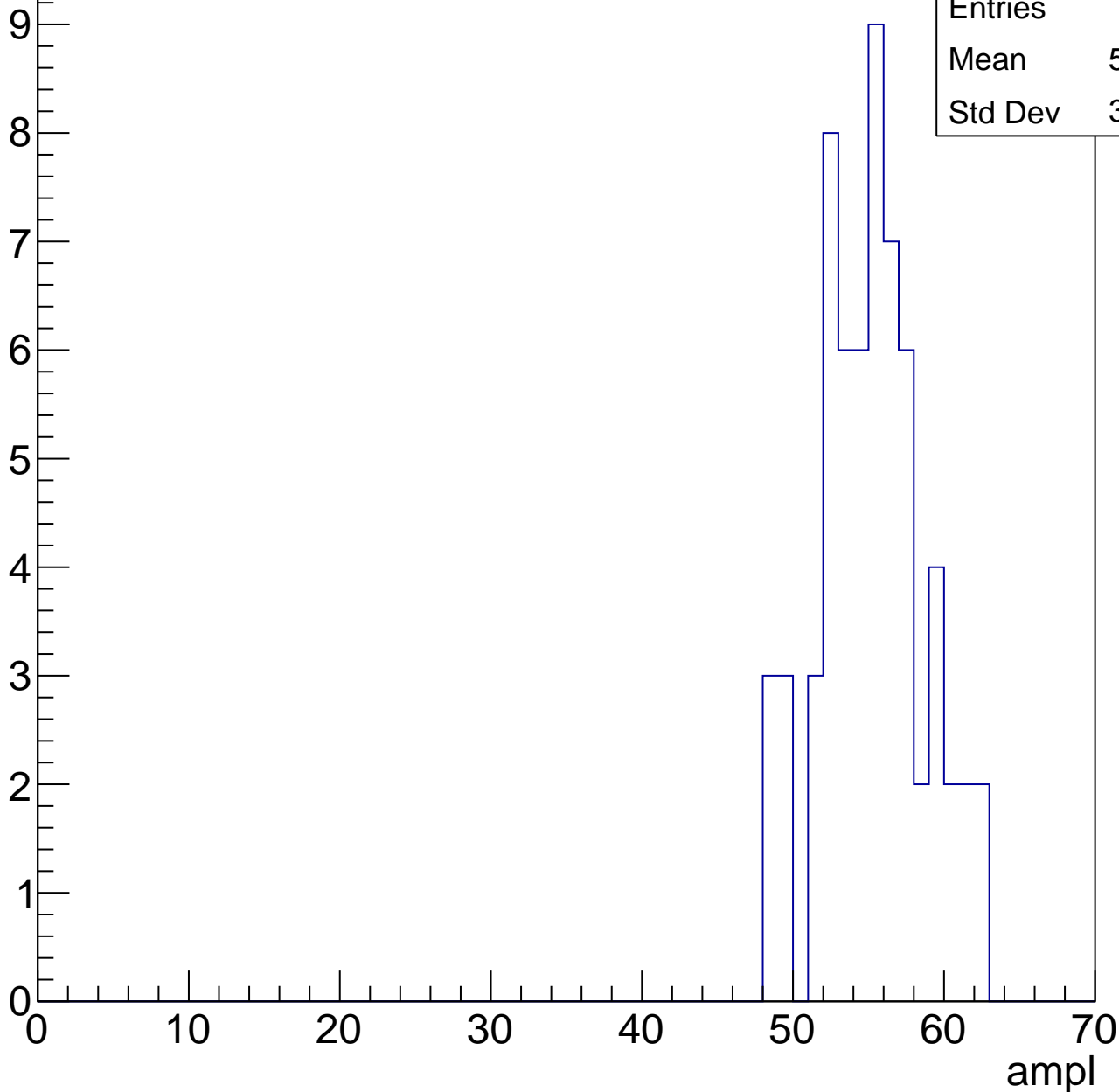


# B1L103S, U16-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	54.75
Std Dev	3.413

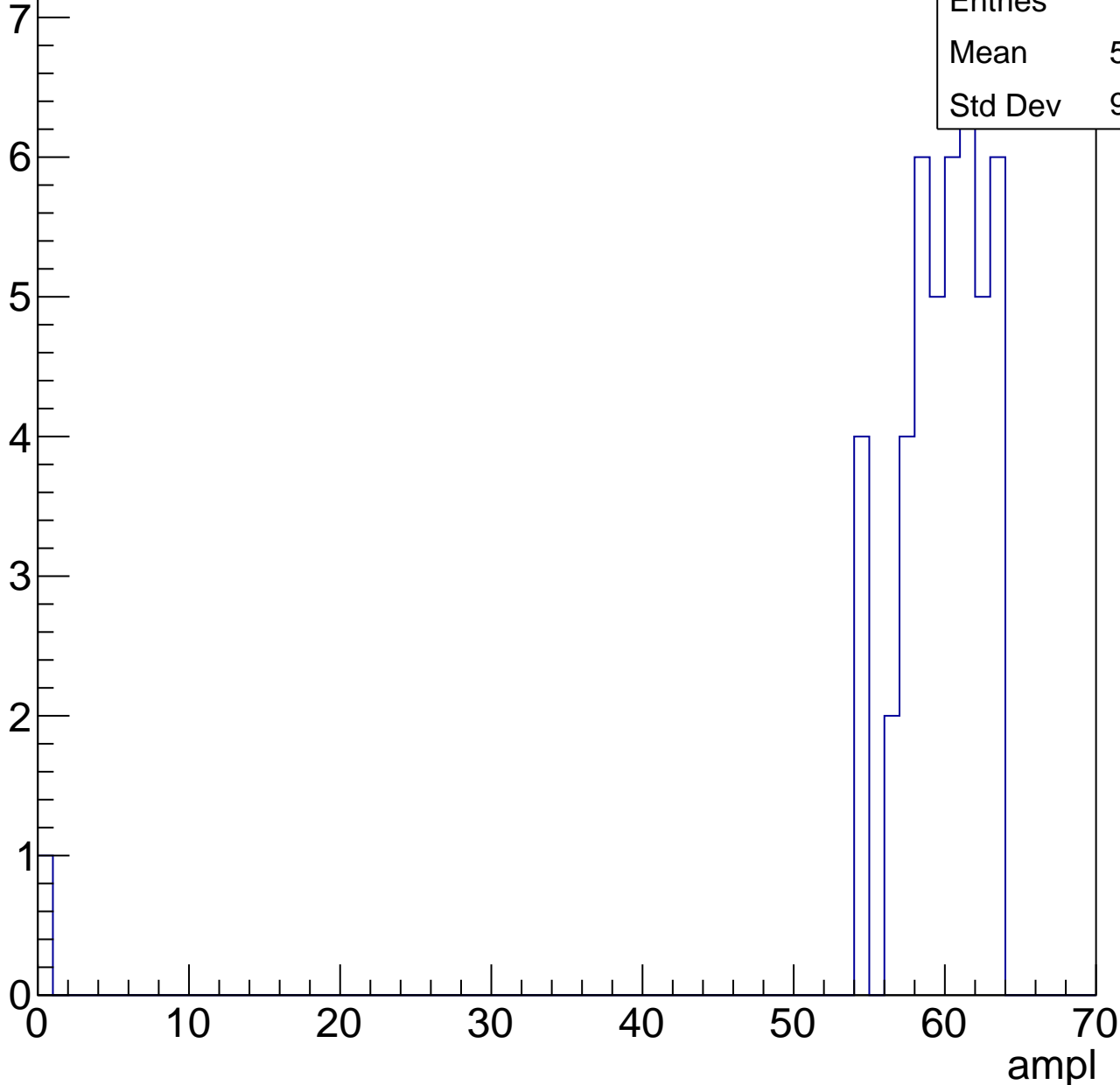


# B1L103S, U16-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

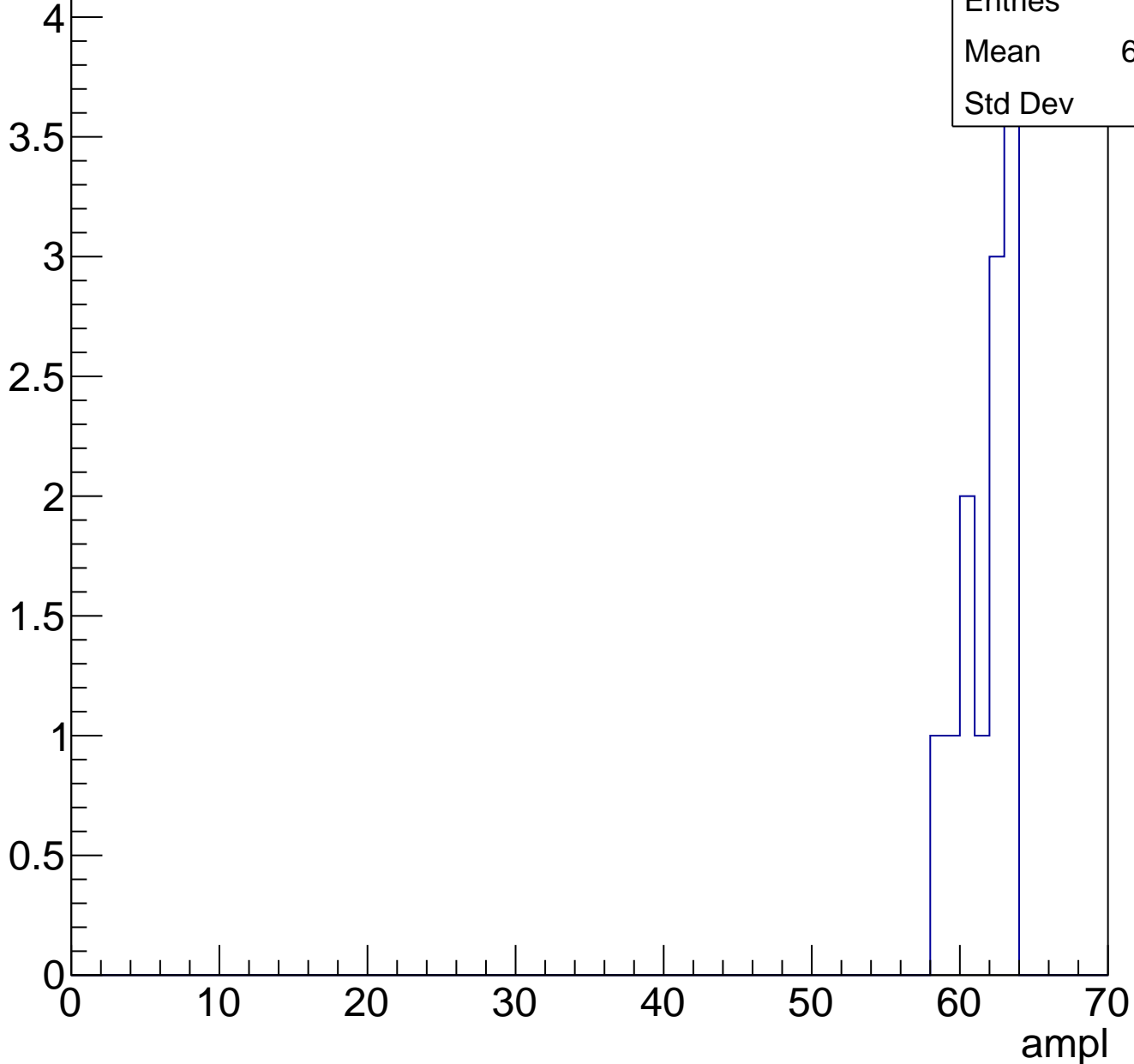
Entries	46
Mean	58.13
Std Dev	9.042



# B1L103S, U16-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch8, adc0

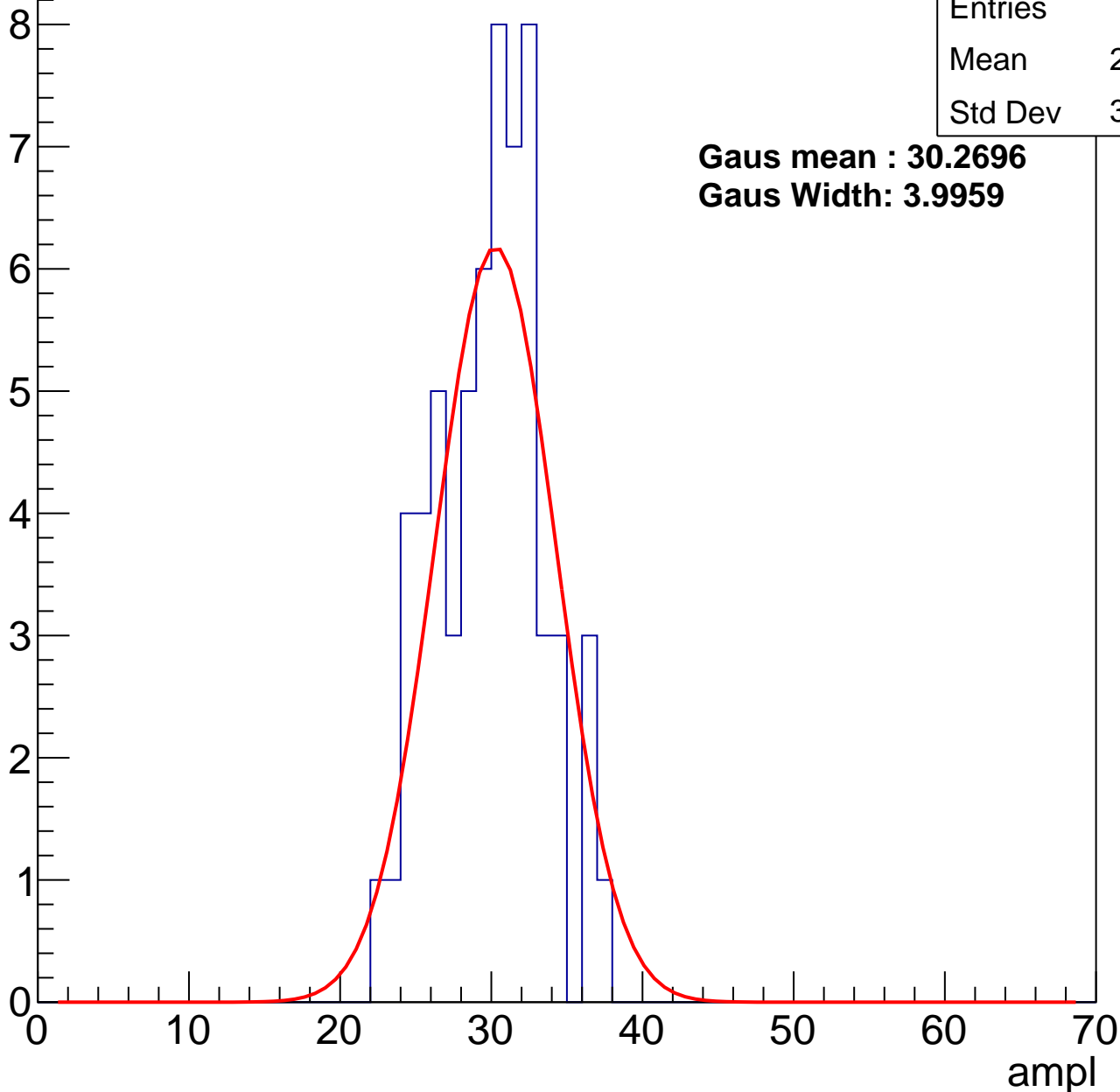
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	29.44
Std Dev	3.458

**Gaus mean : 30.2696**

**Gaus Width: 3.9959**



# B1L103S, U16-ch8, adc1

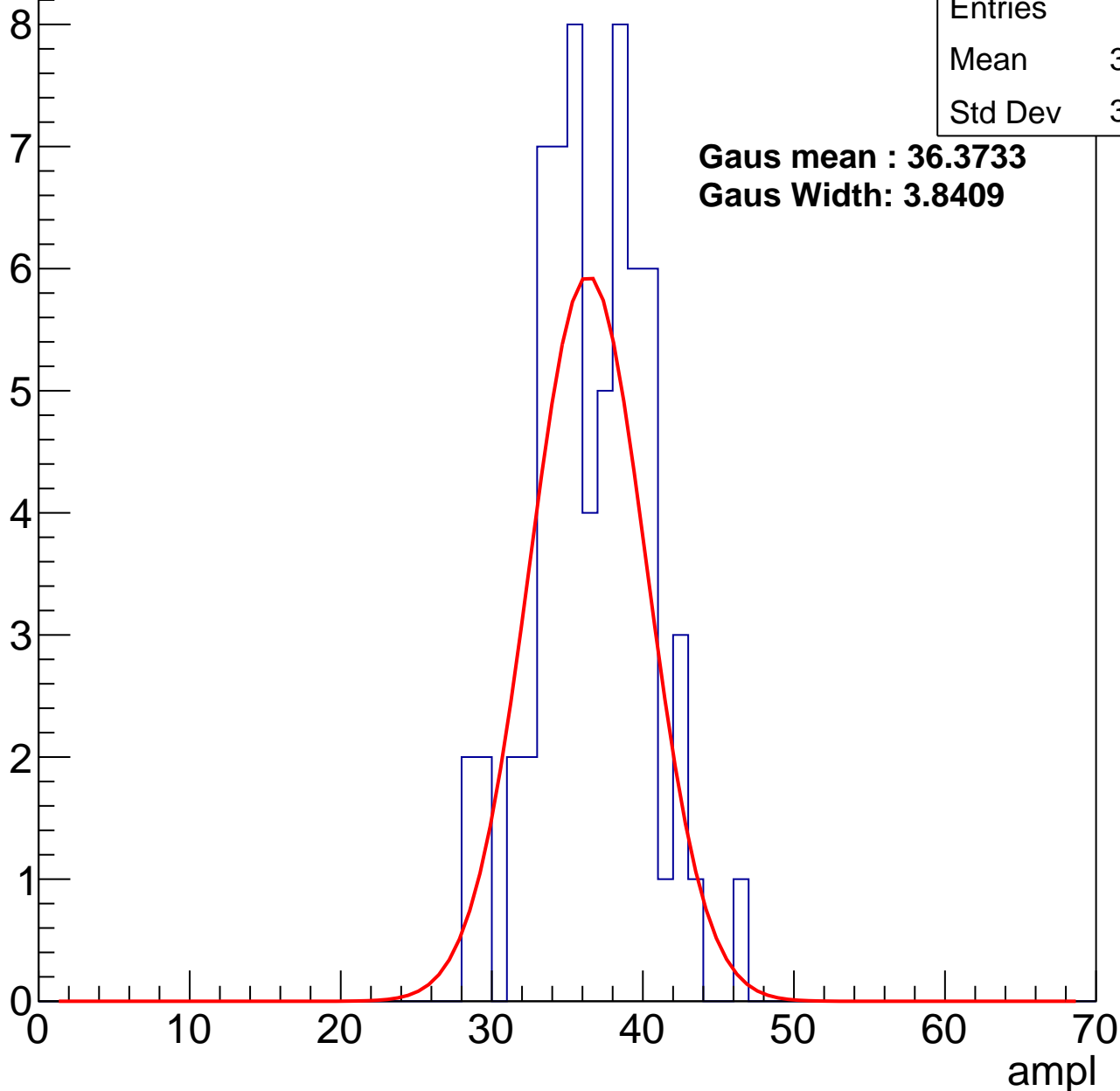
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	36.18
Std Dev	3.666

**Gaus mean : 36.3733**

**Gaus Width: 3.8409**



# B1L103S, U16-ch8, adc2

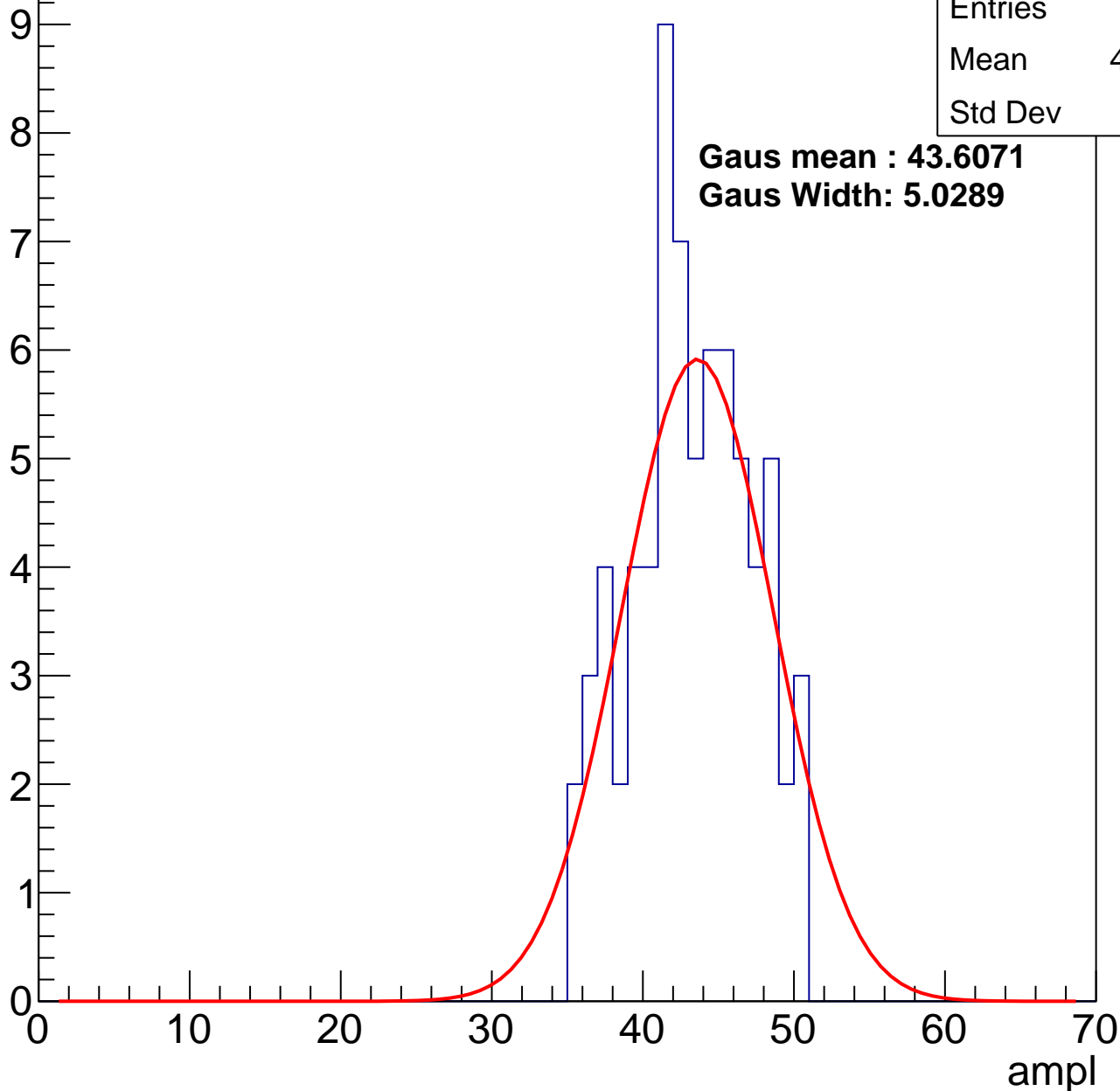
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	42.76
Std Dev	3.92

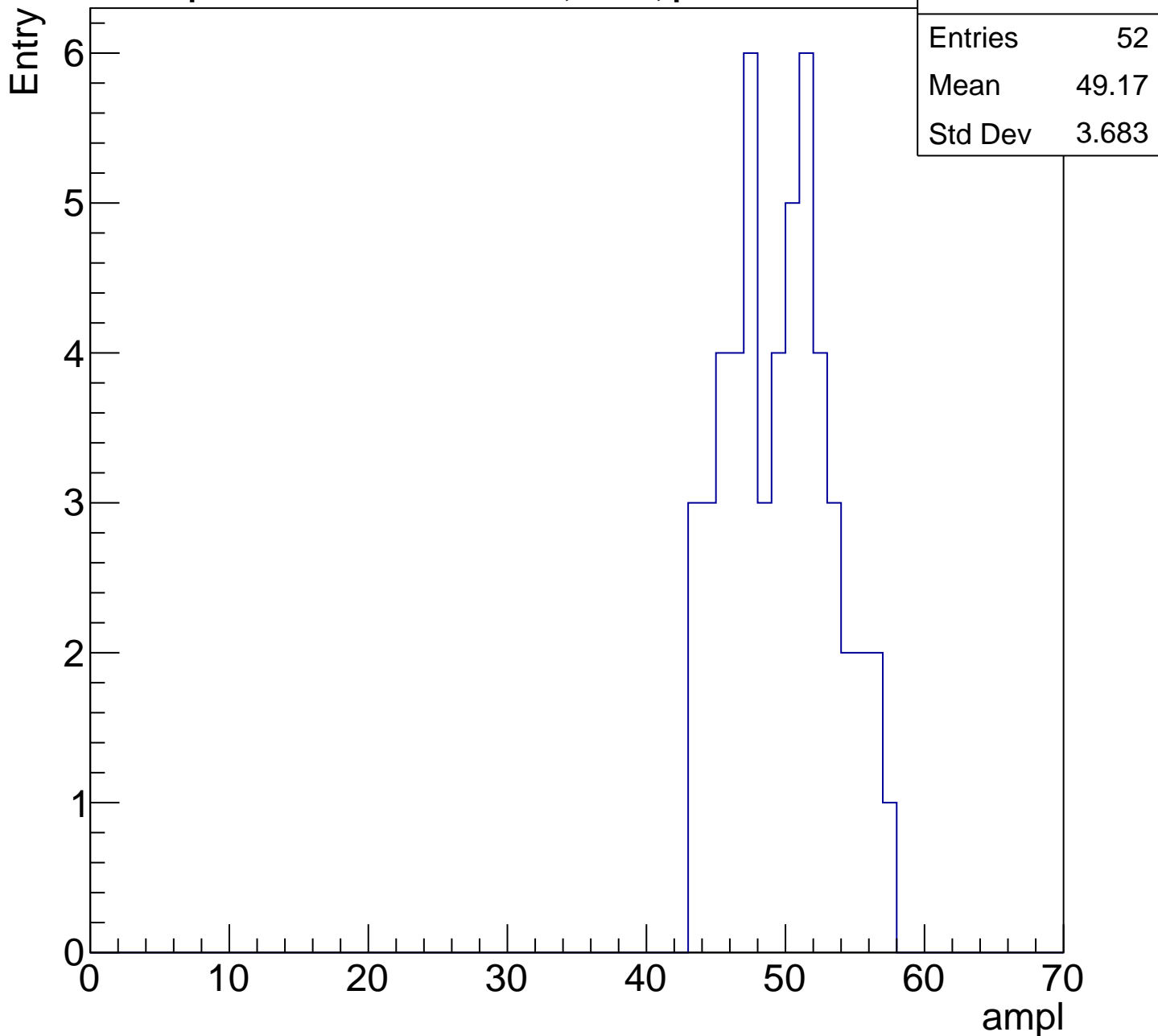
**Gaus mean : 43.6071**

**Gaus Width: 5.0289**



# B1L103S, U16-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

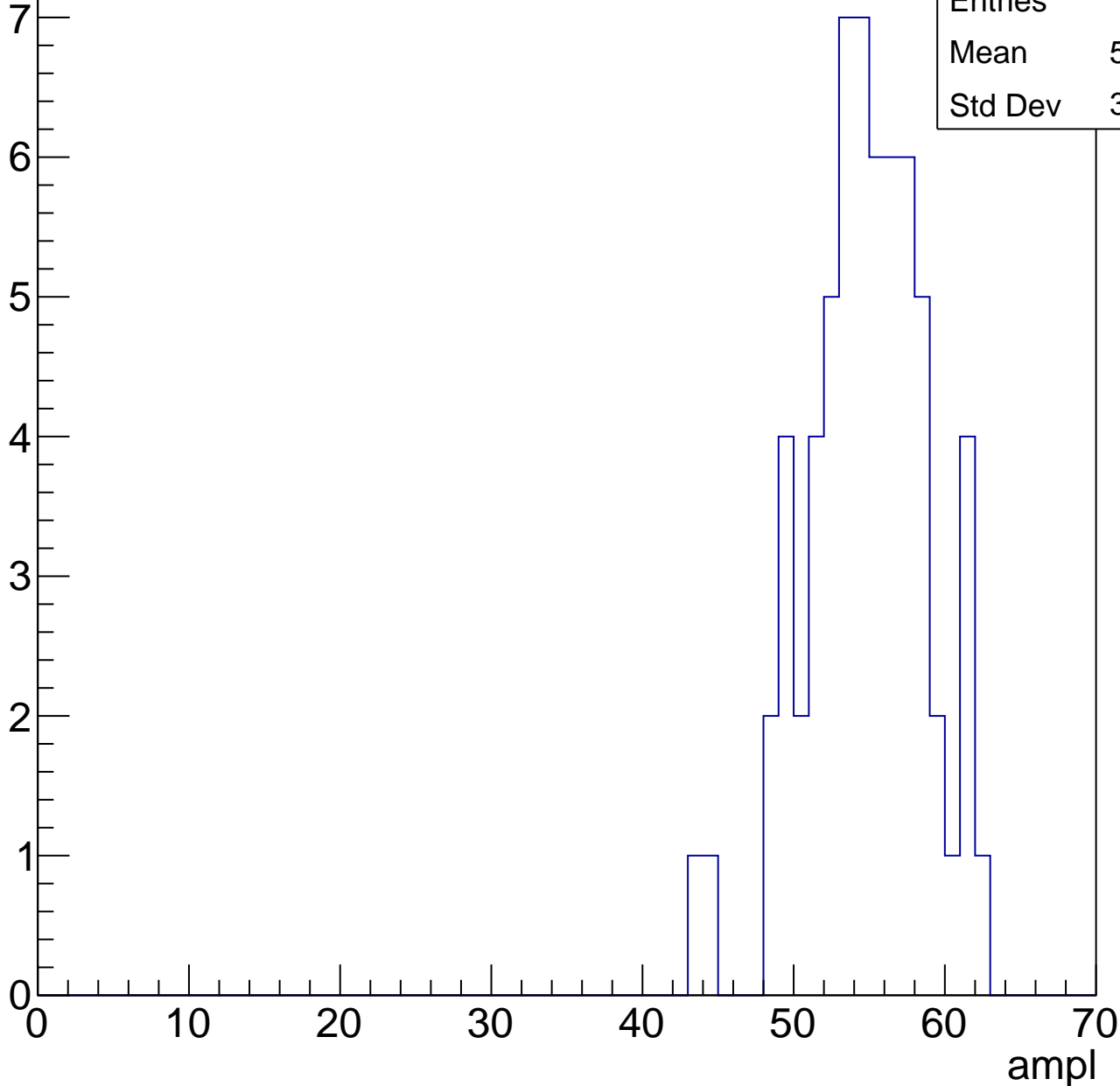


# B1L103S, U16-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

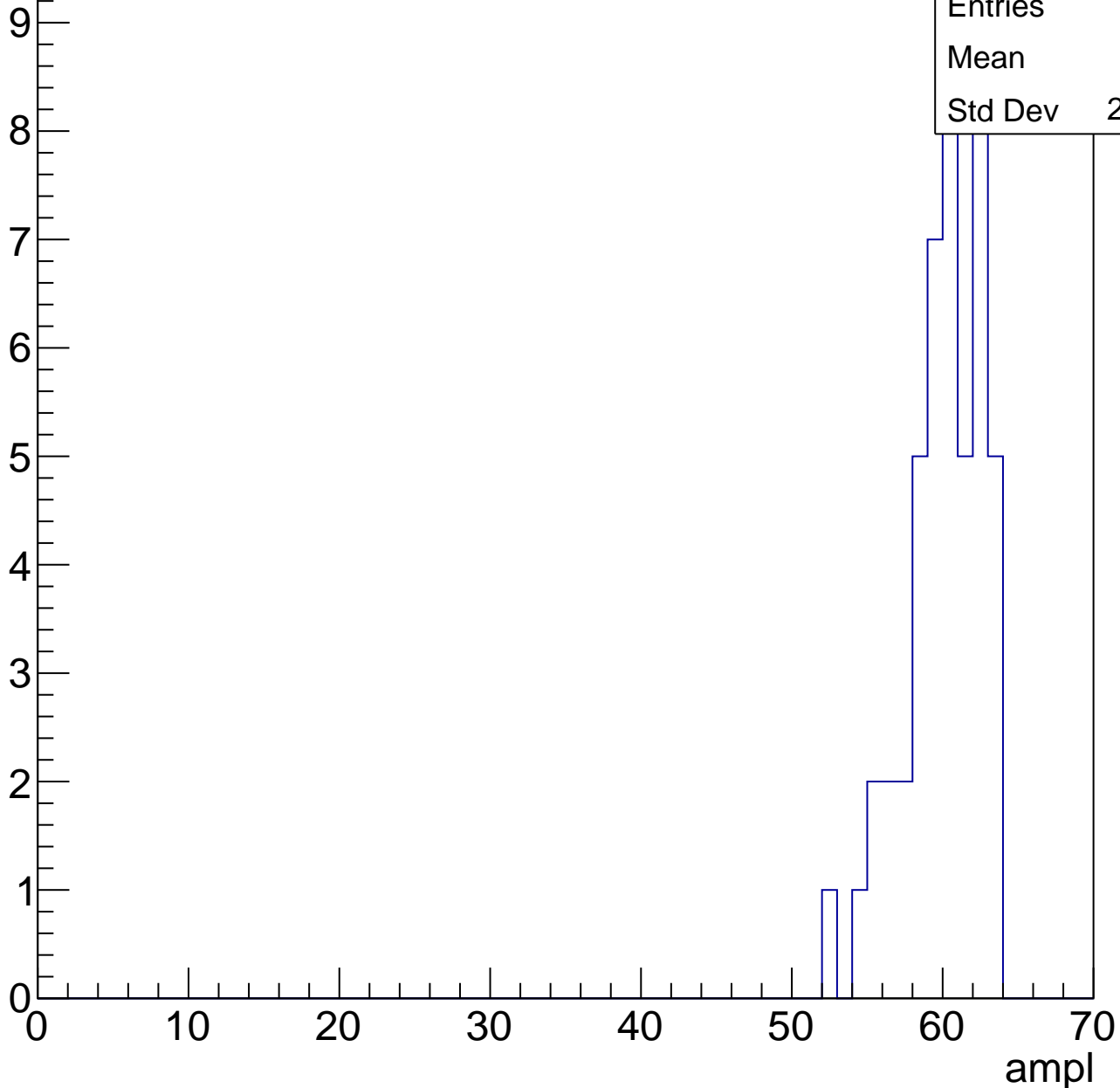
Entries	64
Mean	54.28
Std Dev	3.939



# B1L103S, U16-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

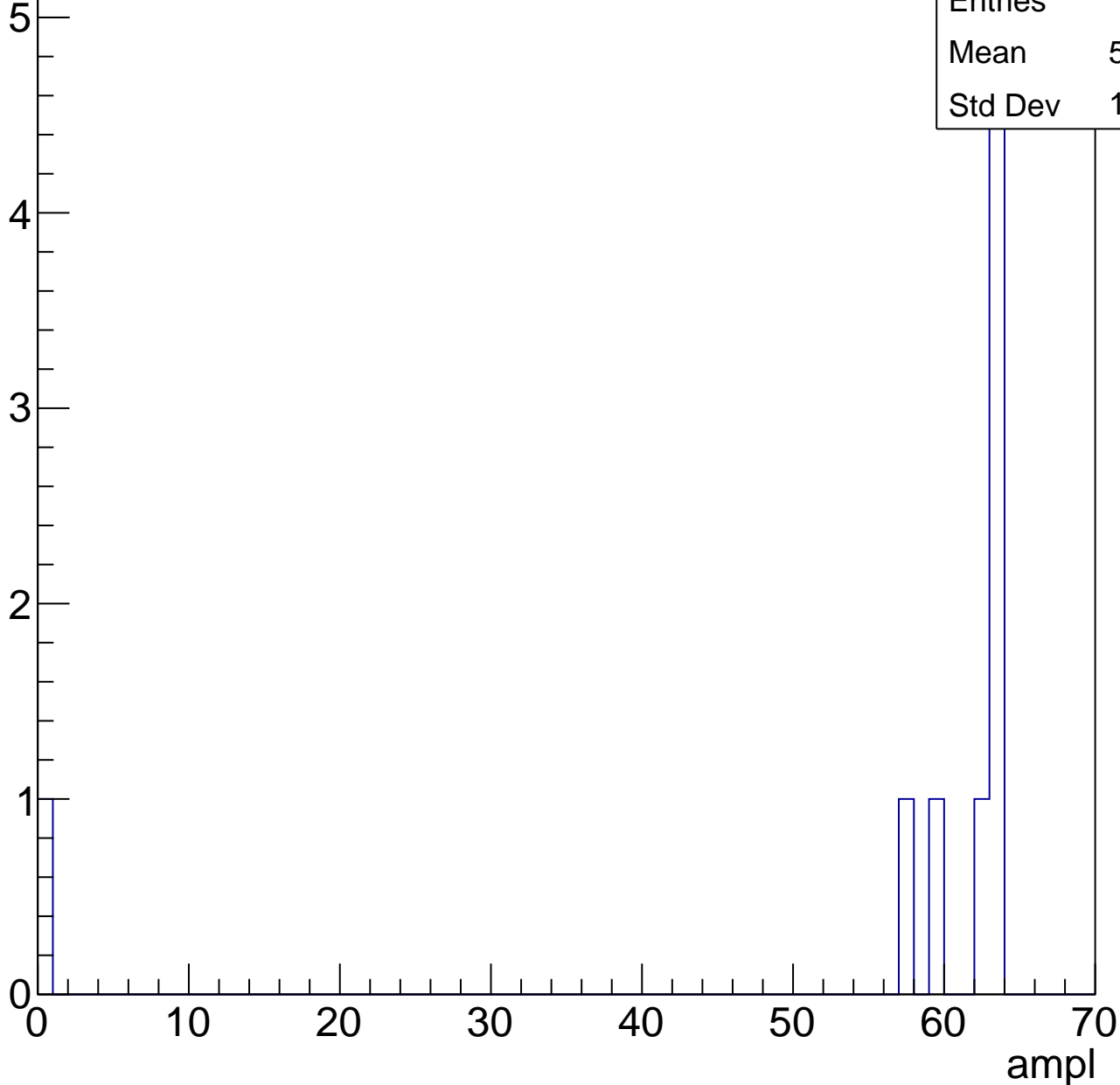


# B1L103S, U16-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	9
Mean	54.78
Std Dev	19.48

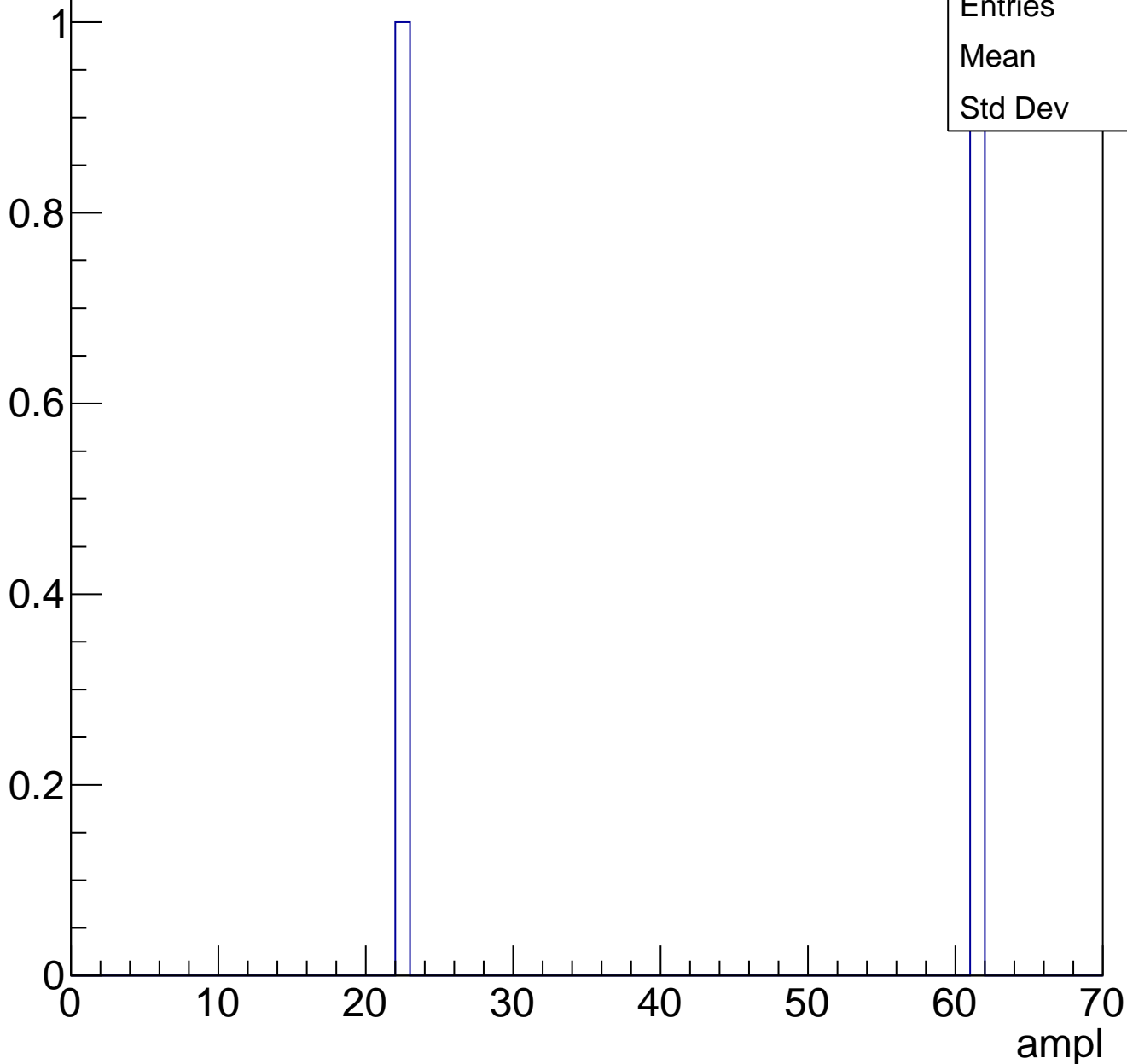




# B1L103S, U16-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch9, adc0

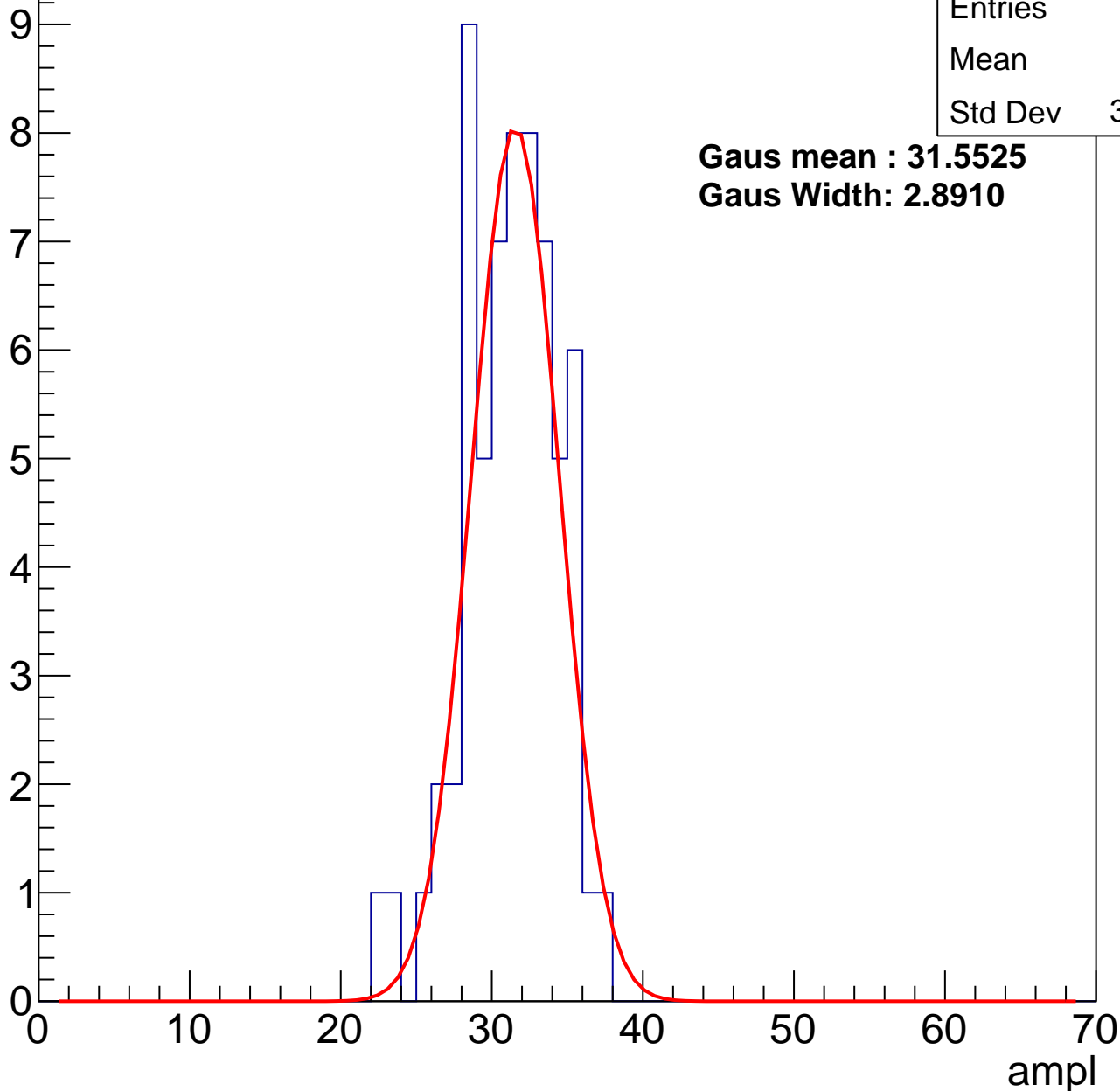
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	30.8
Std Dev	3.078

**Gaus mean : 31.5525**

**Gaus Width: 2.8910**



# B1L103S, U16-ch9, adc1

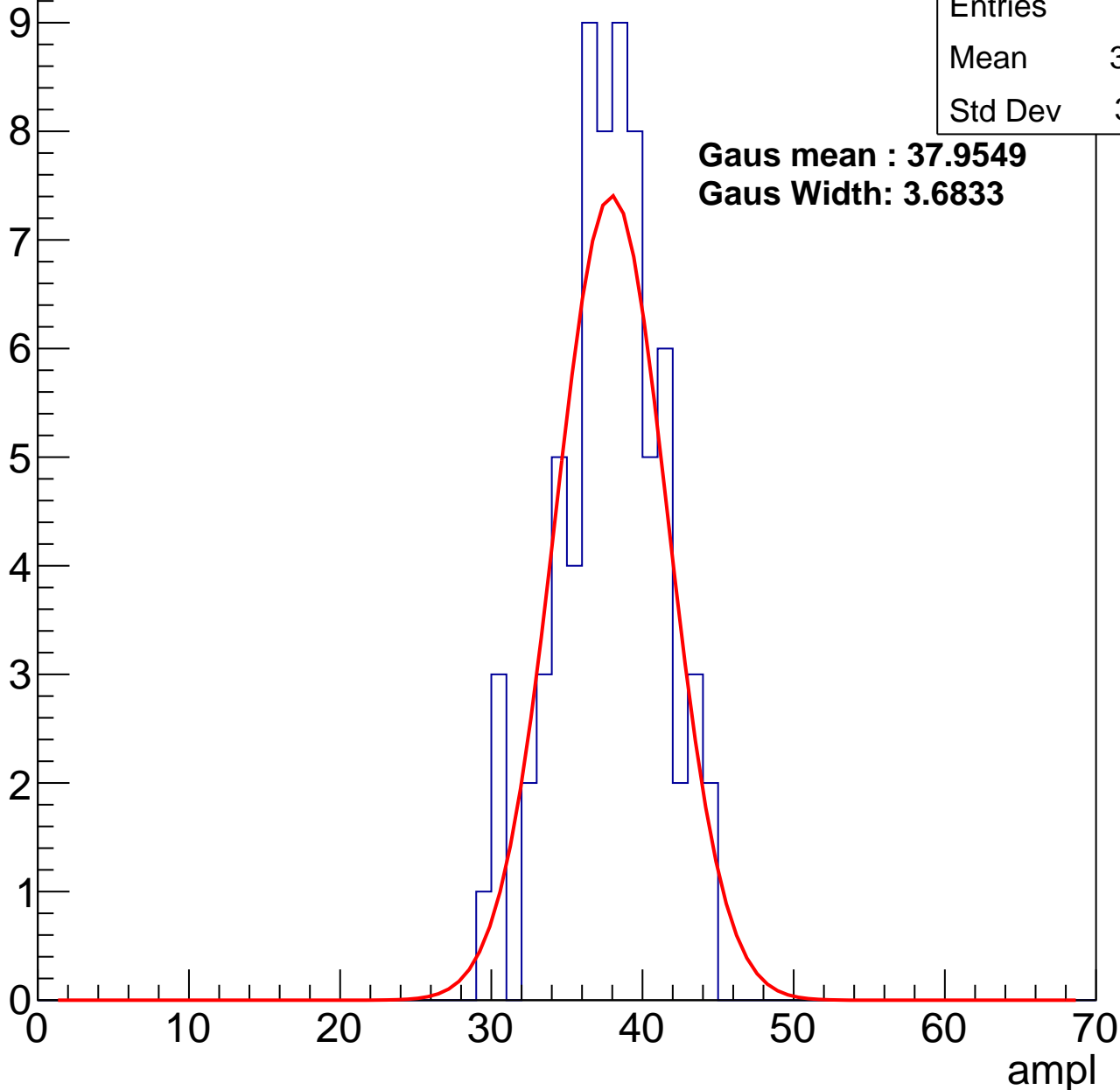
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	37.33
Std Dev	3.401

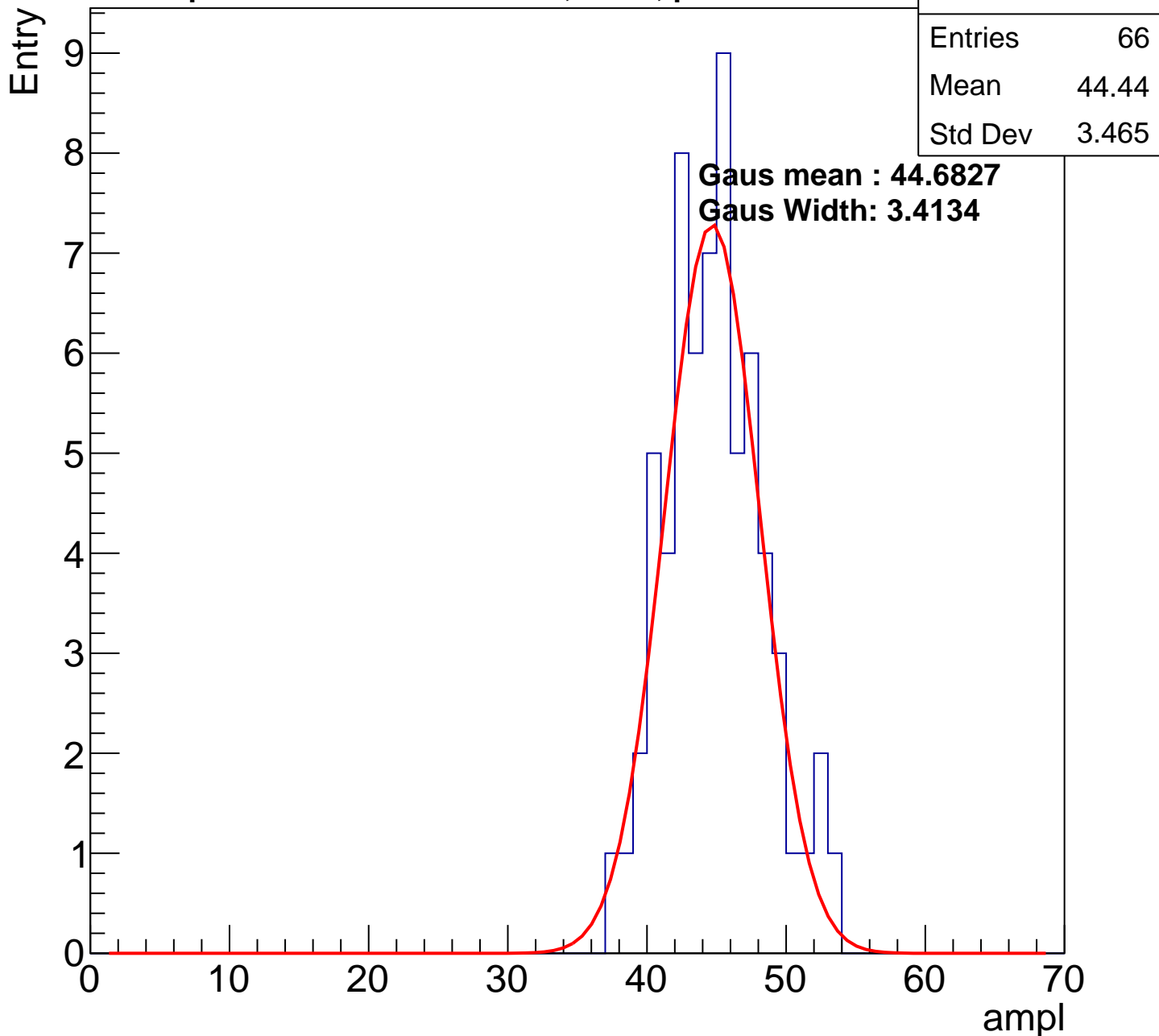
**Gaus mean : 37.9549**

**Gaus Width: 3.6833**



# B1L103S, U16-ch9, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

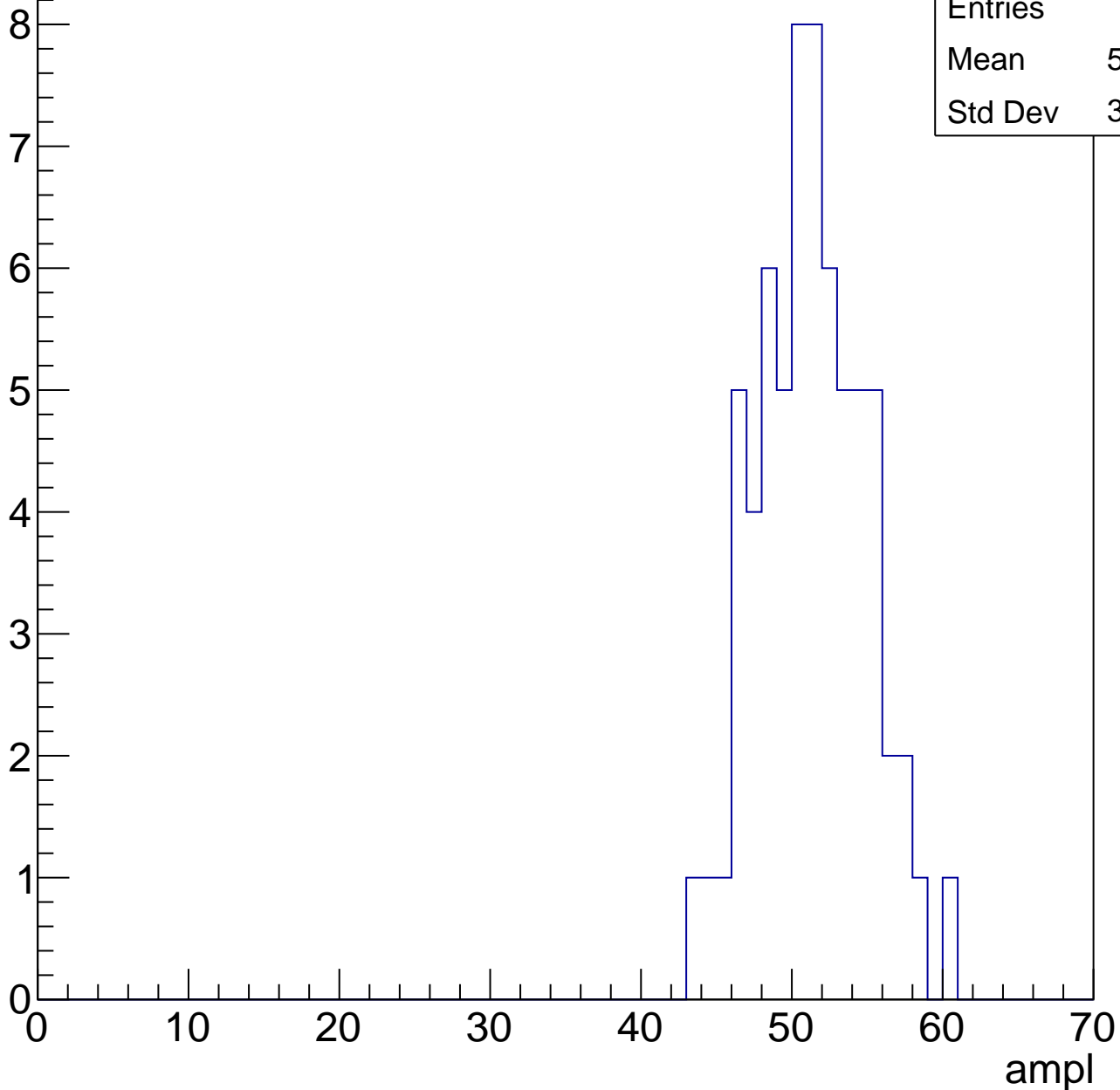


# B1L103S, U16-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	50.86
Std Dev	3.529

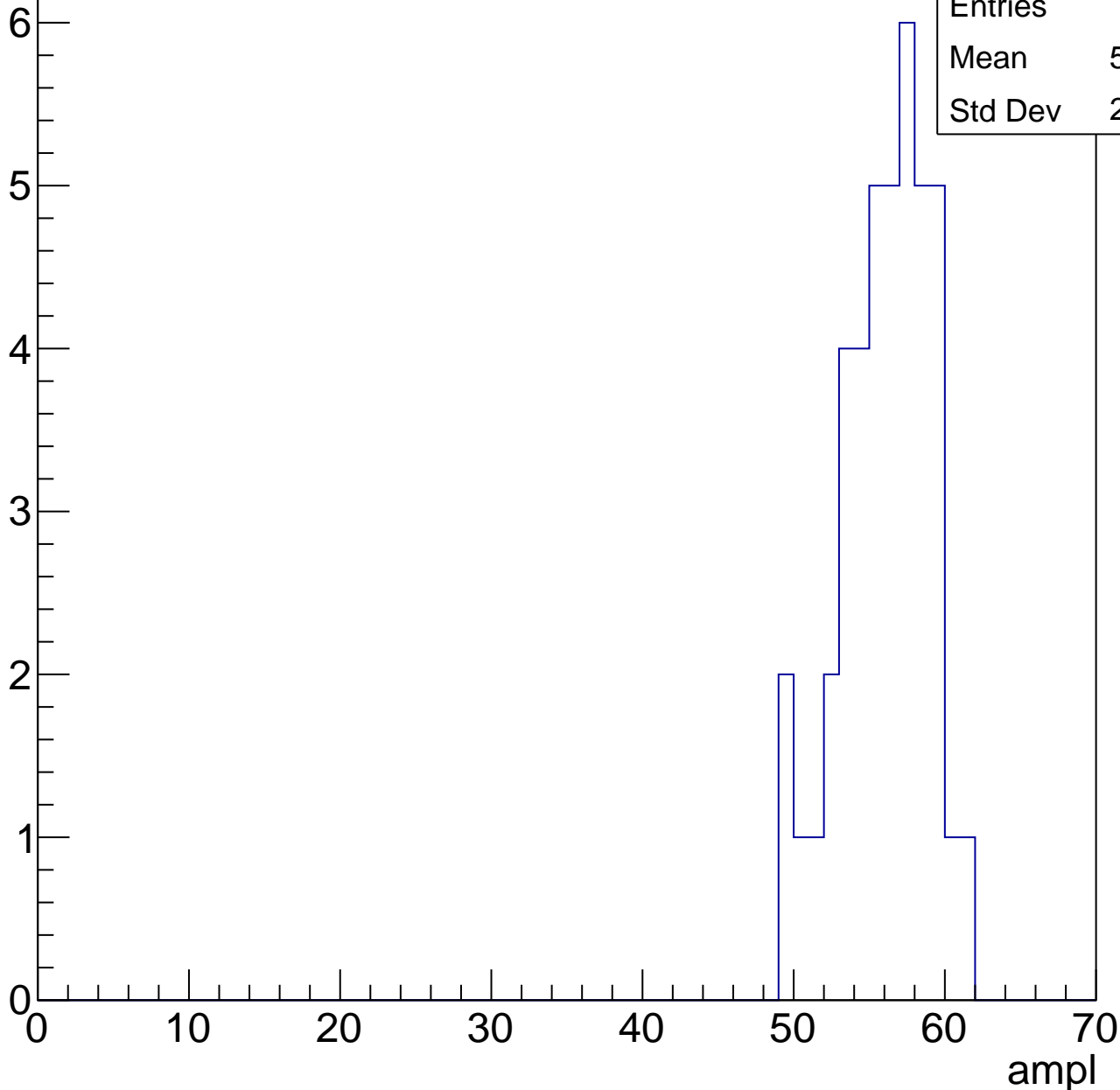


# B1L103S, U16-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	42
Mean	55.57
Std Dev	2.896

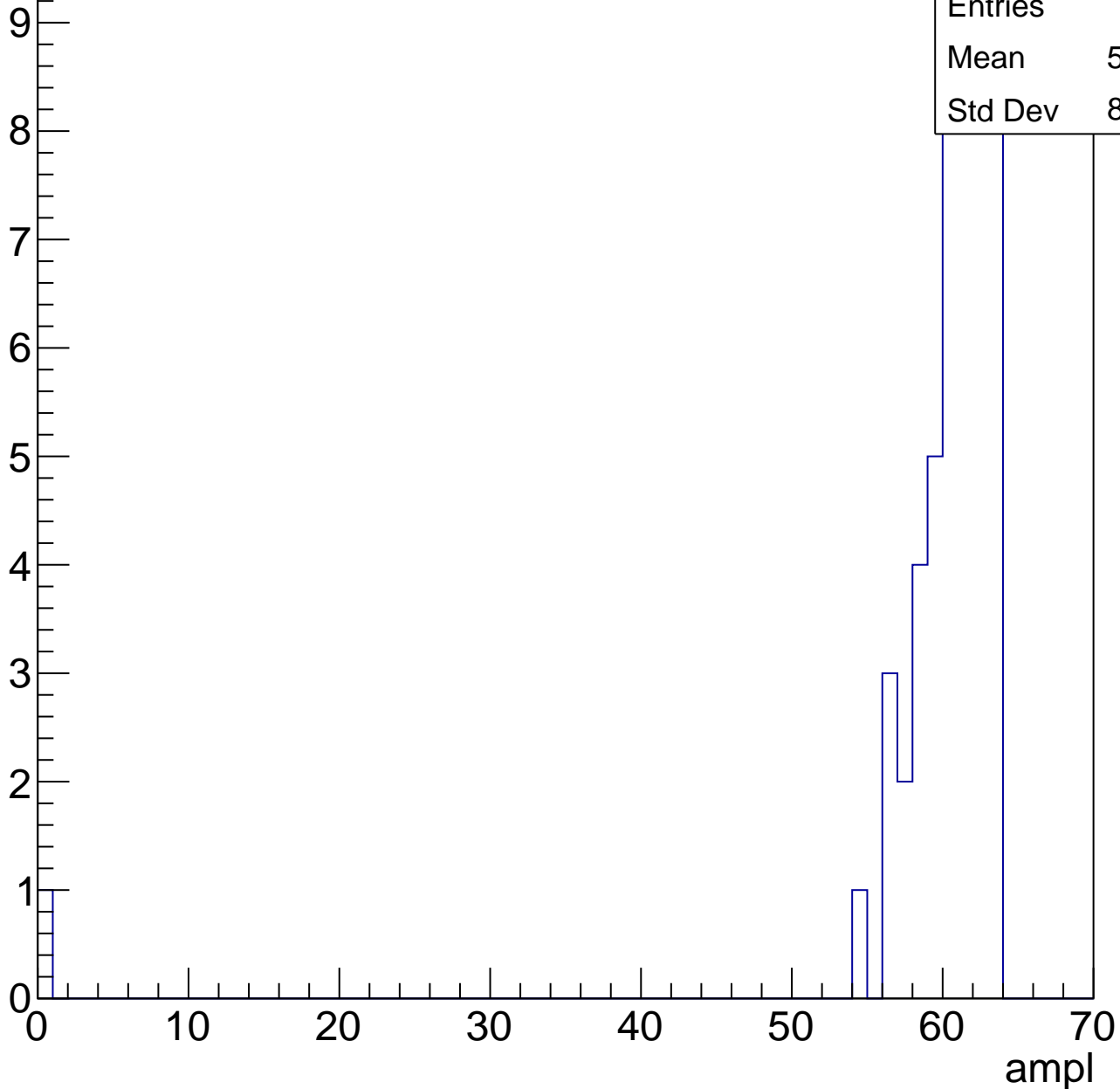


# B1L103S, U16-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	59.08
Std Dev	8.715



# B1L103S, U16-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B1L103S, U16-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U16-ch10, adc0

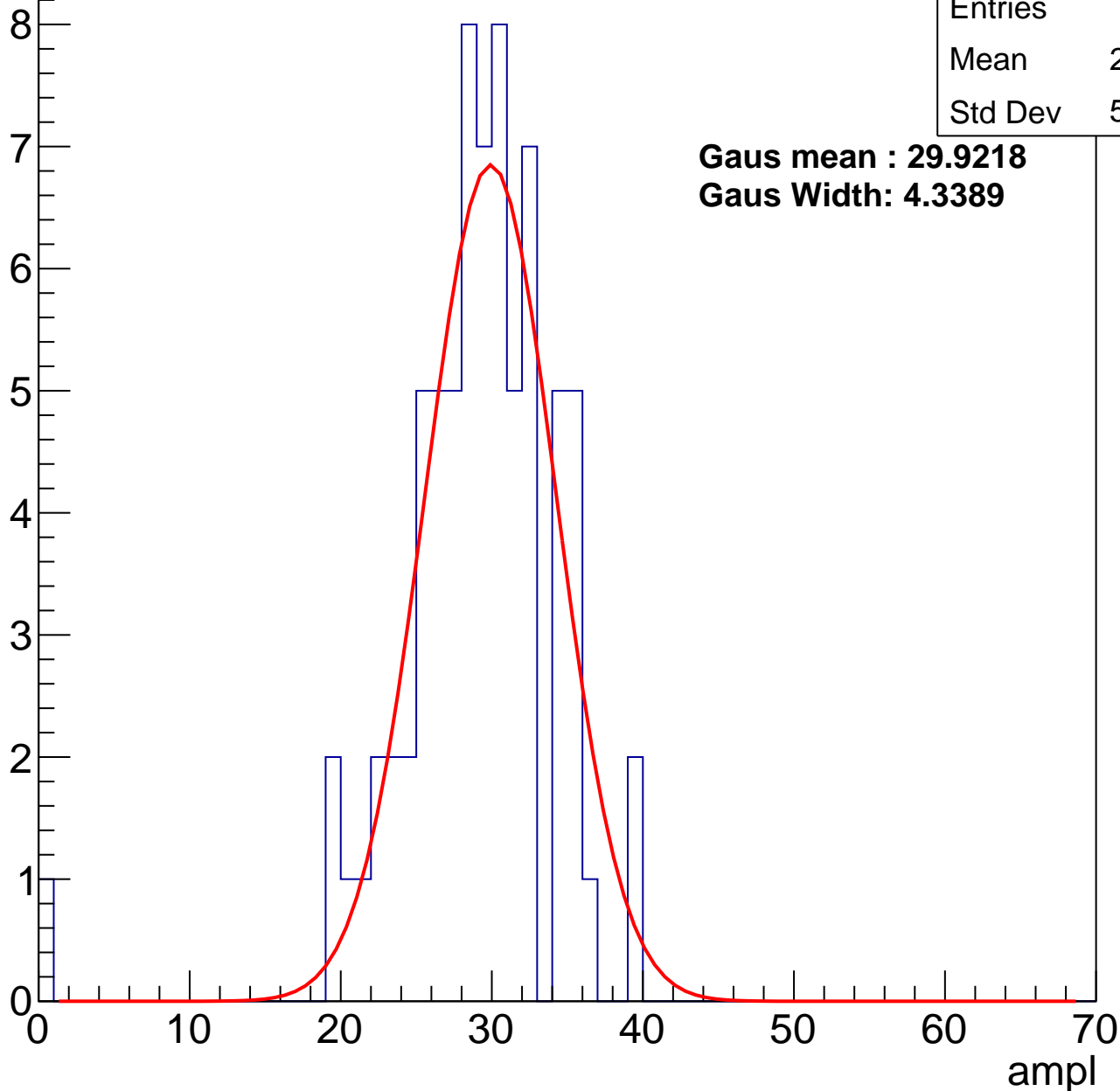
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	28.54
Std Dev	5.438

**Gaus mean : 29.9218**

**Gaus Width: 4.3389**



# B1L103S, U16-ch10, adc1

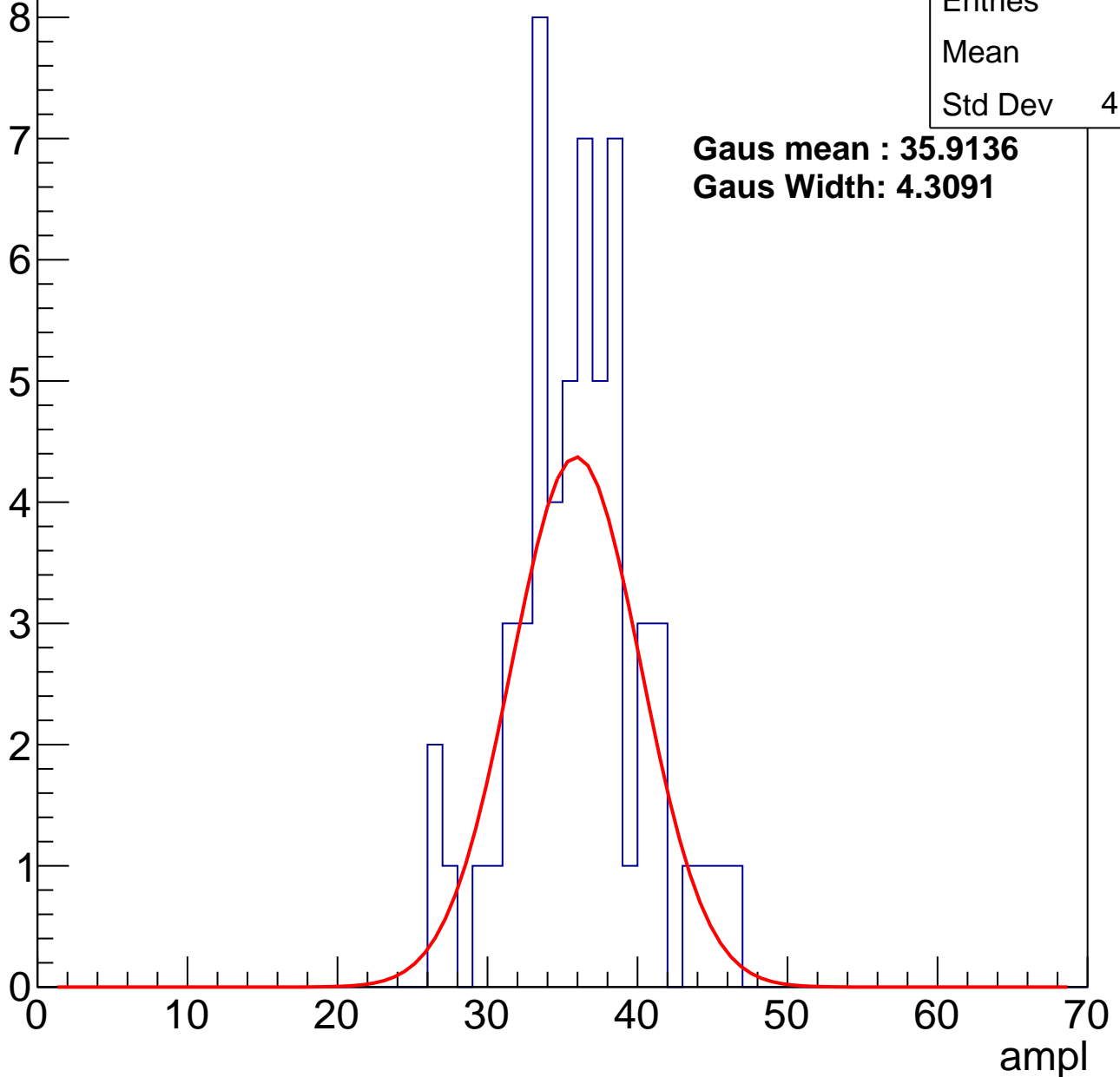
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	35.6
Std Dev	4.218

**Gaus mean : 35.9136**

**Gaus Width: 4.3091**



# B1L103S, U16-ch10, adc2

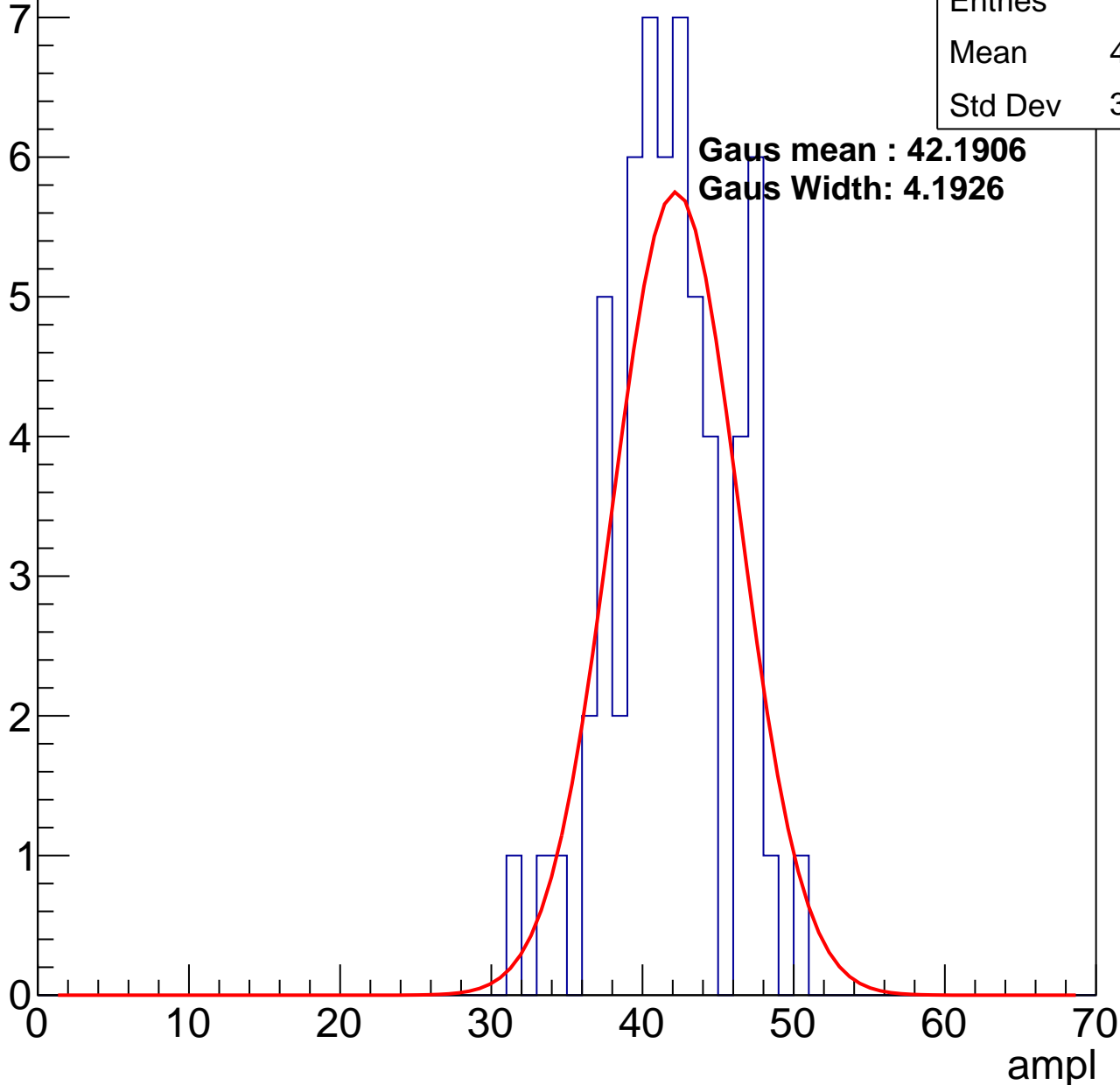
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	41.36
Std Dev	3.892

**Gaus mean : 42.1906**

**Gaus Width: 4.1926**

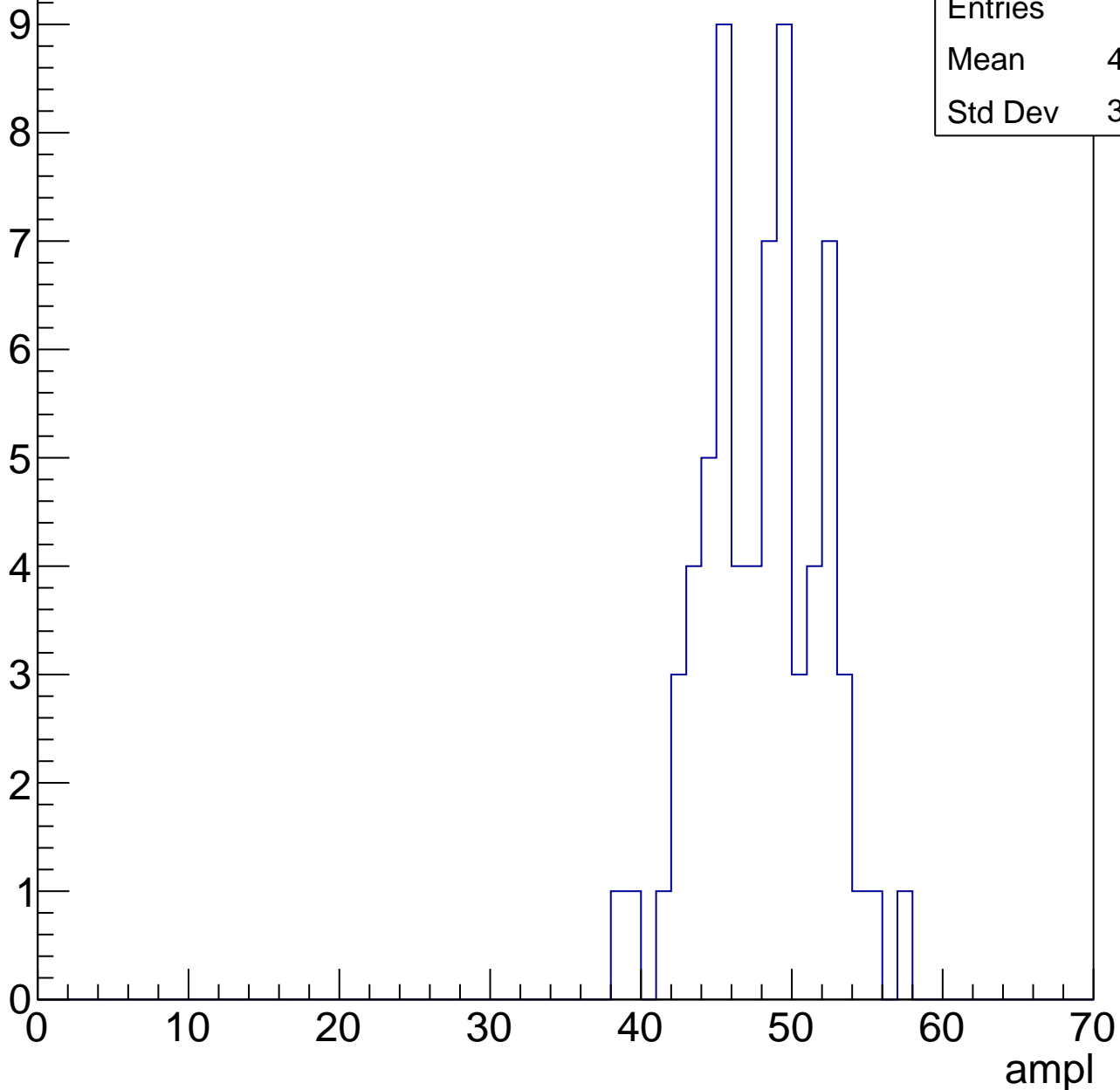


# B1L103S, U16-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	47.54
Std Dev	3.863

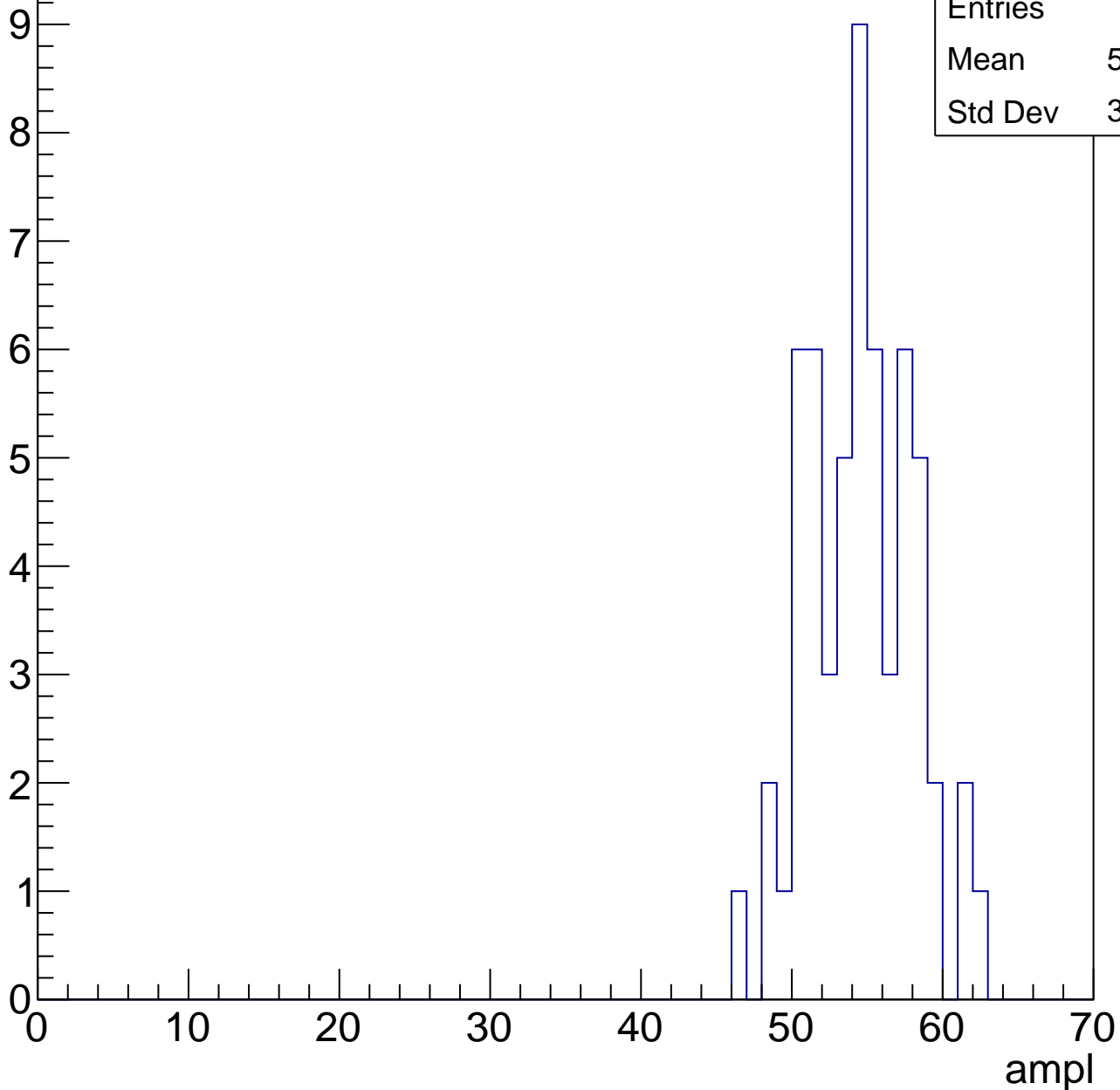


# B1L103S, U16-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

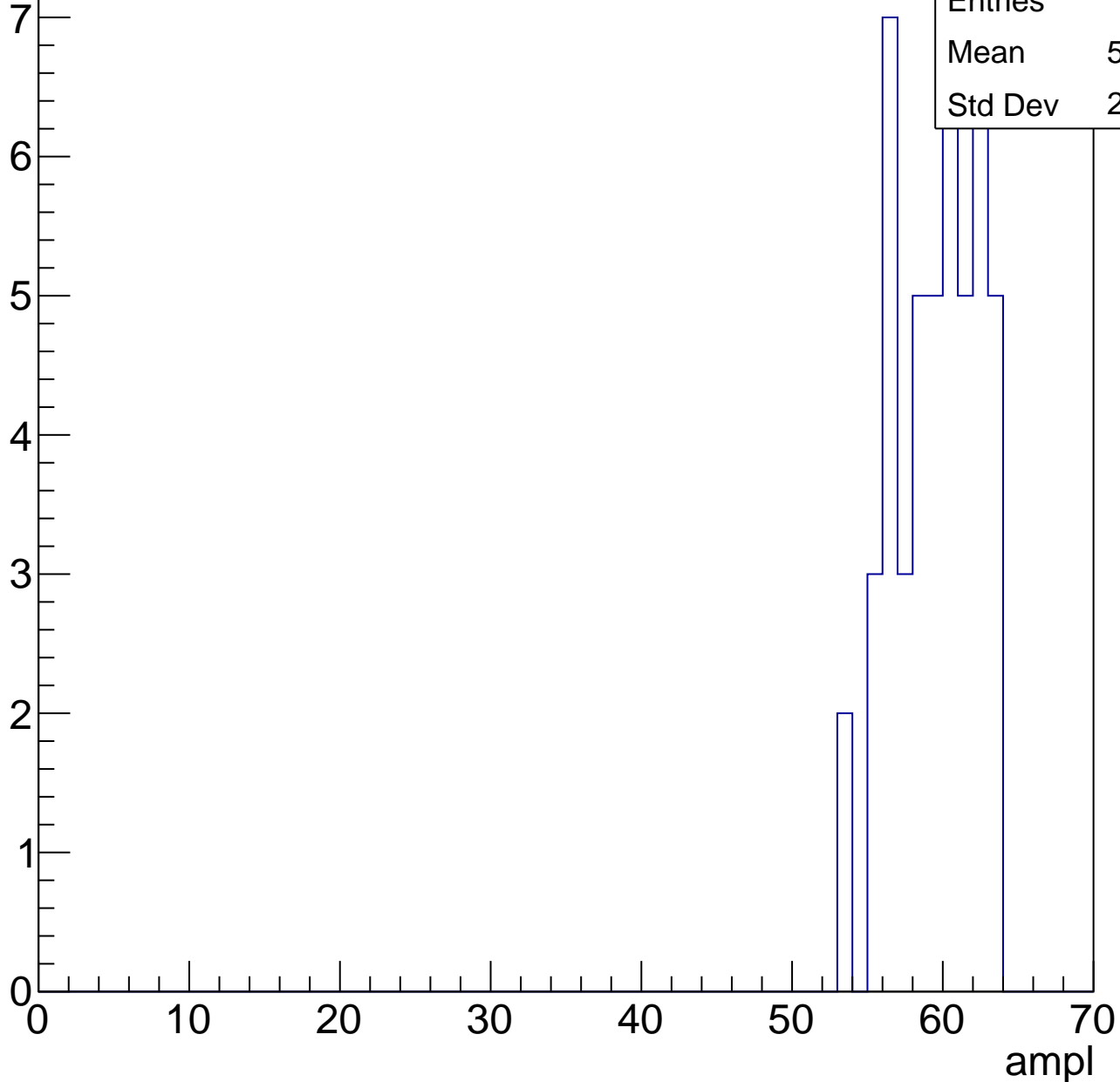
Entries	58
Mean	54.07
Std Dev	3.453



# B1L103S, U16-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

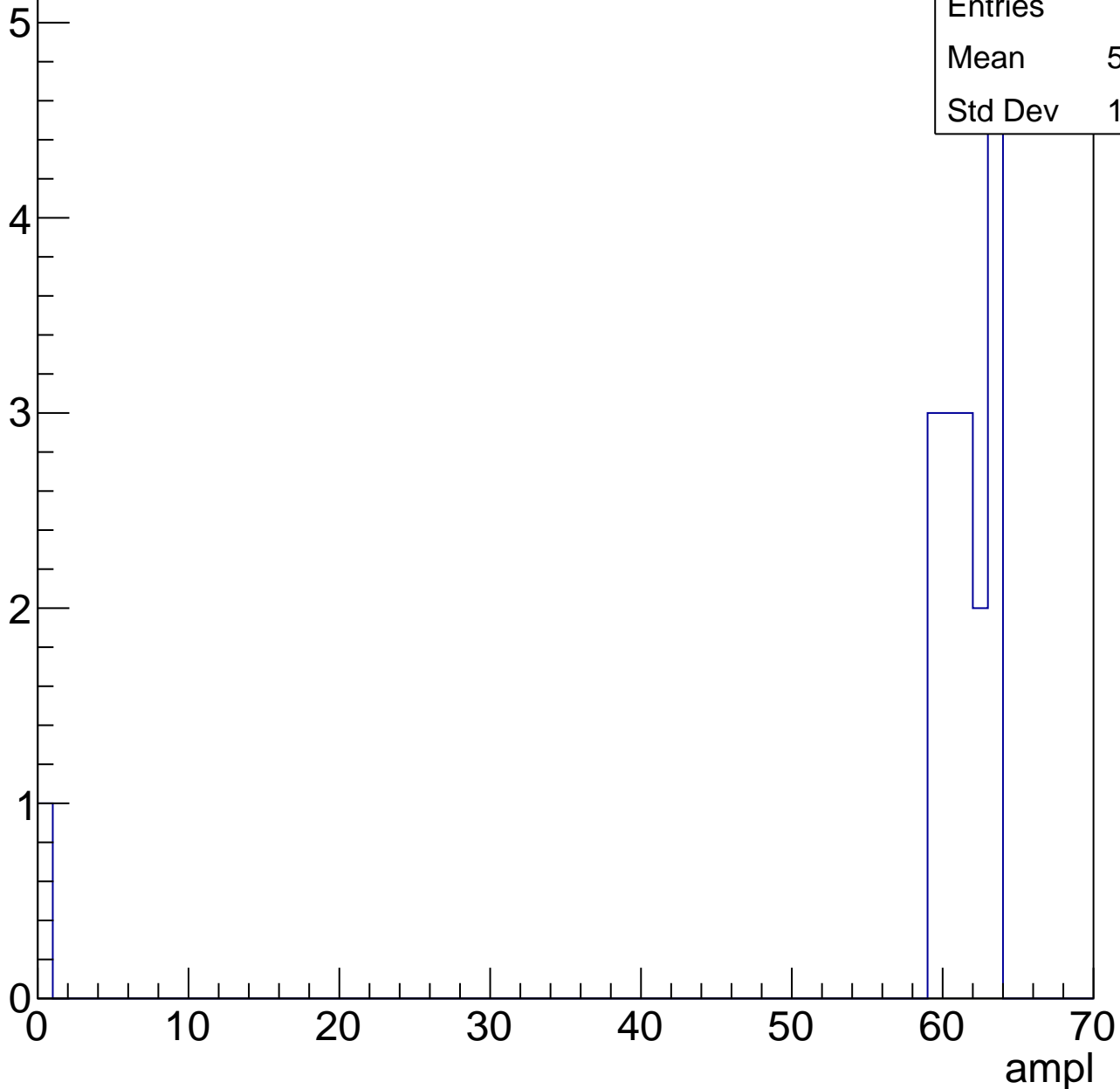


# B1L103S, U16-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	17
Mean	57.59
Std Dev	14.47





# B1L103S, U16-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U16-ch11, adc0

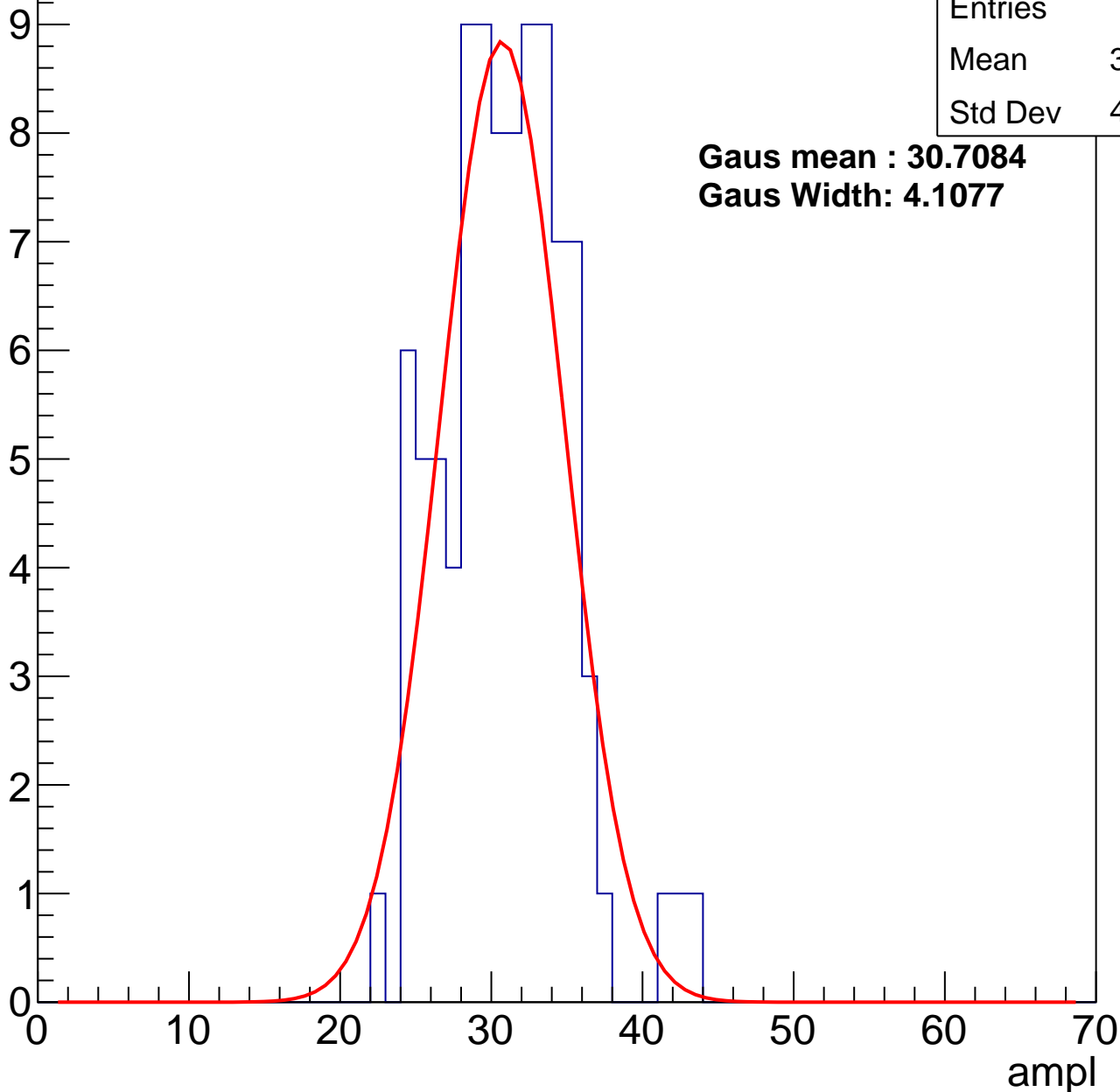
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	94
Mean	30.52
Std Dev	4.052

**Gaus mean : 30.7084**

**Gaus Width: 4.1077**



# B1L103S, U16-ch11, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	64
Mean	37.98
Std Dev	3.11

**Gaus mean : 38.9843**

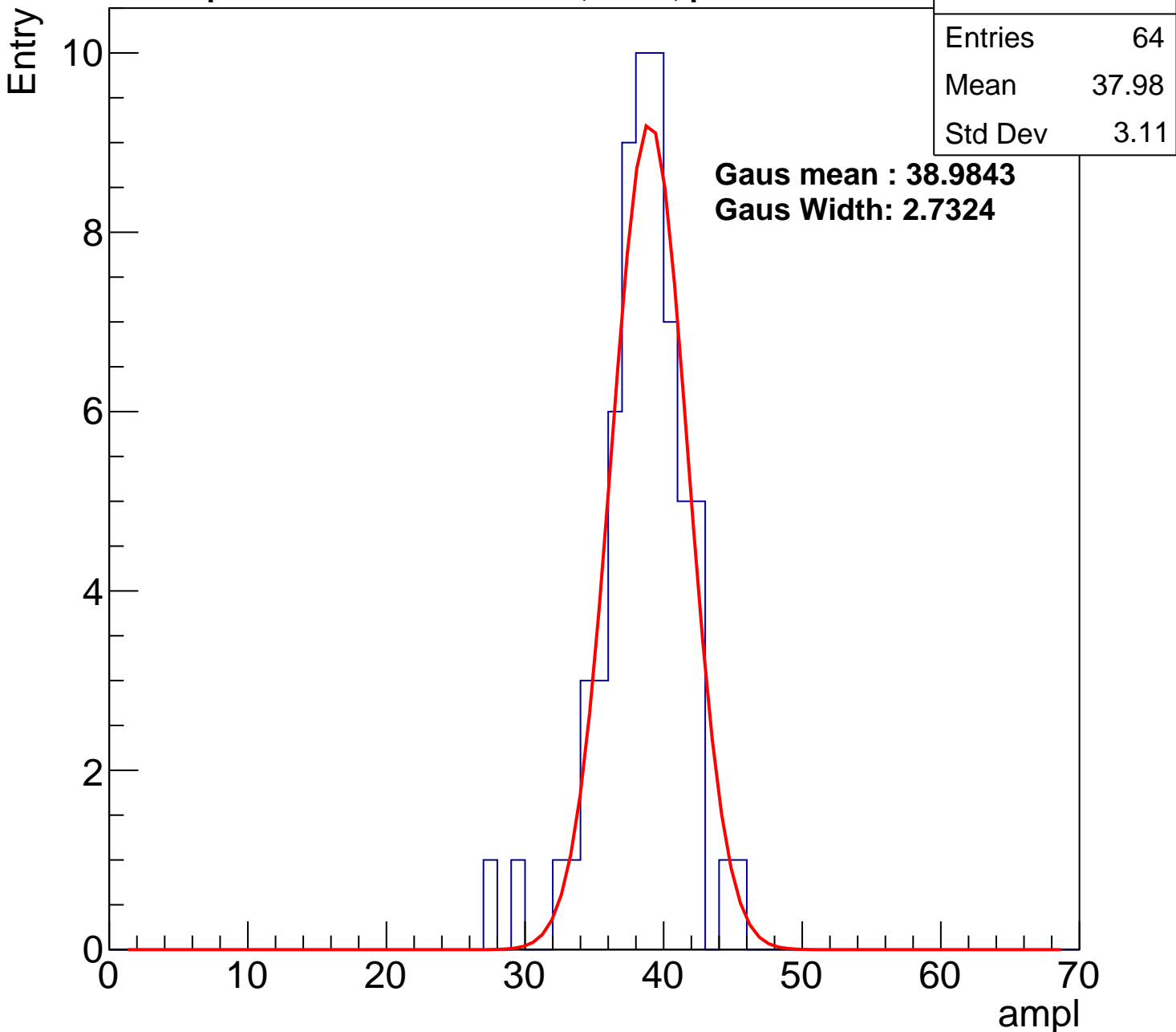
**Gaus Width: 2.7324**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U16-ch11, adc2

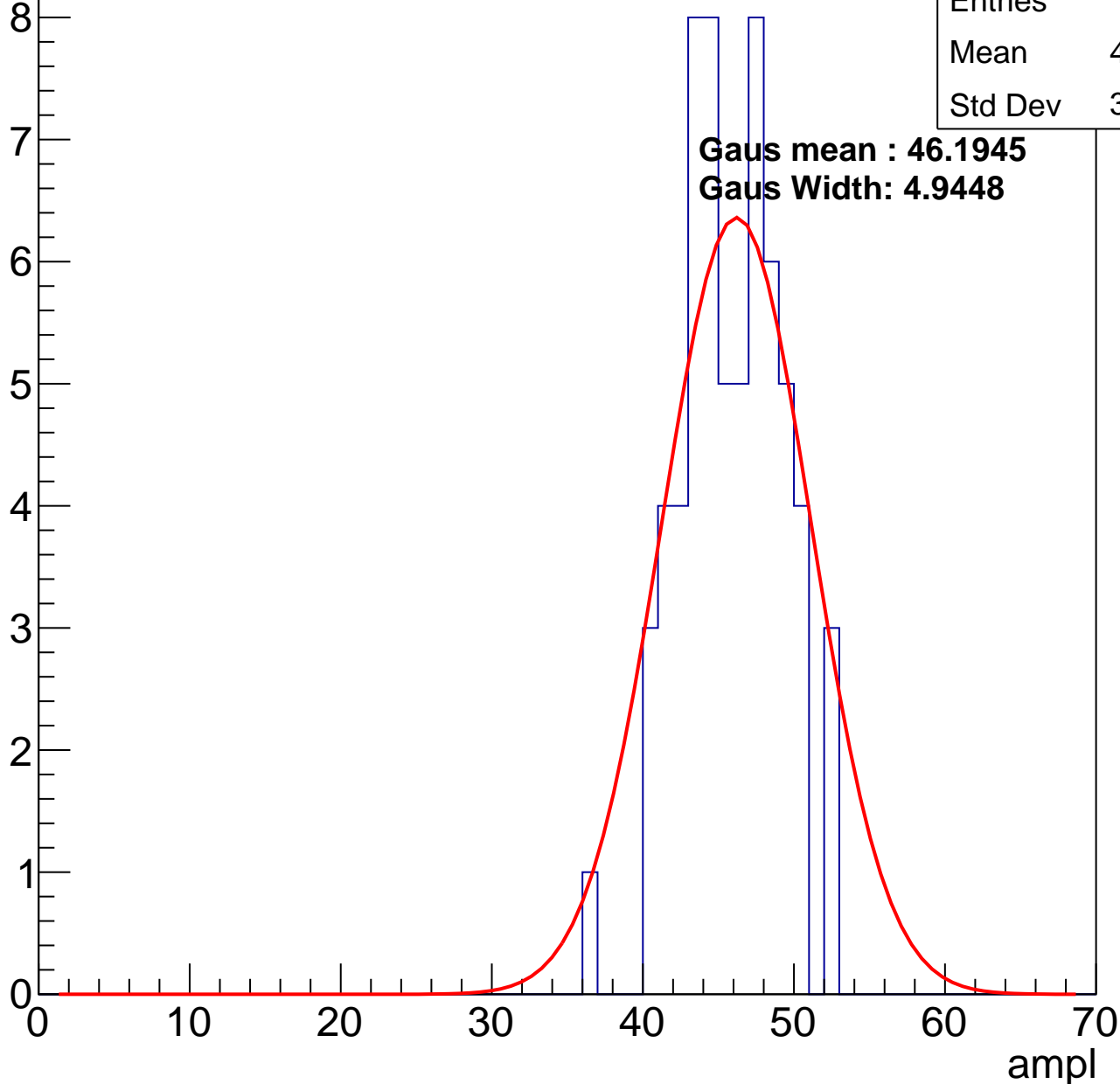
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	45.38
Std Dev	3.319

**Gaus mean : 46.1945**

**Gaus Width: 4.9448**

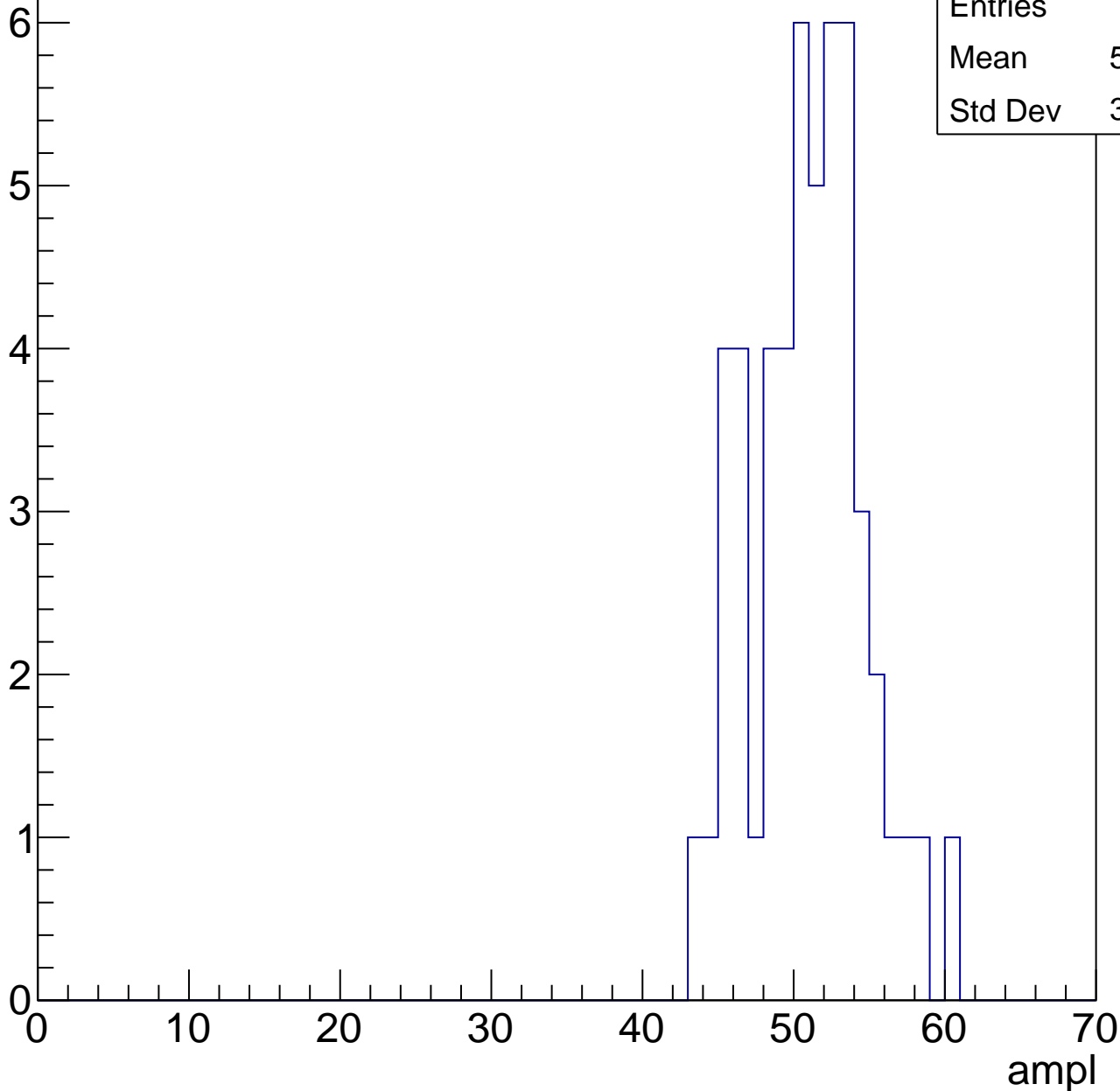


# B1L103S, U16-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	50.47
Std Dev	3.696

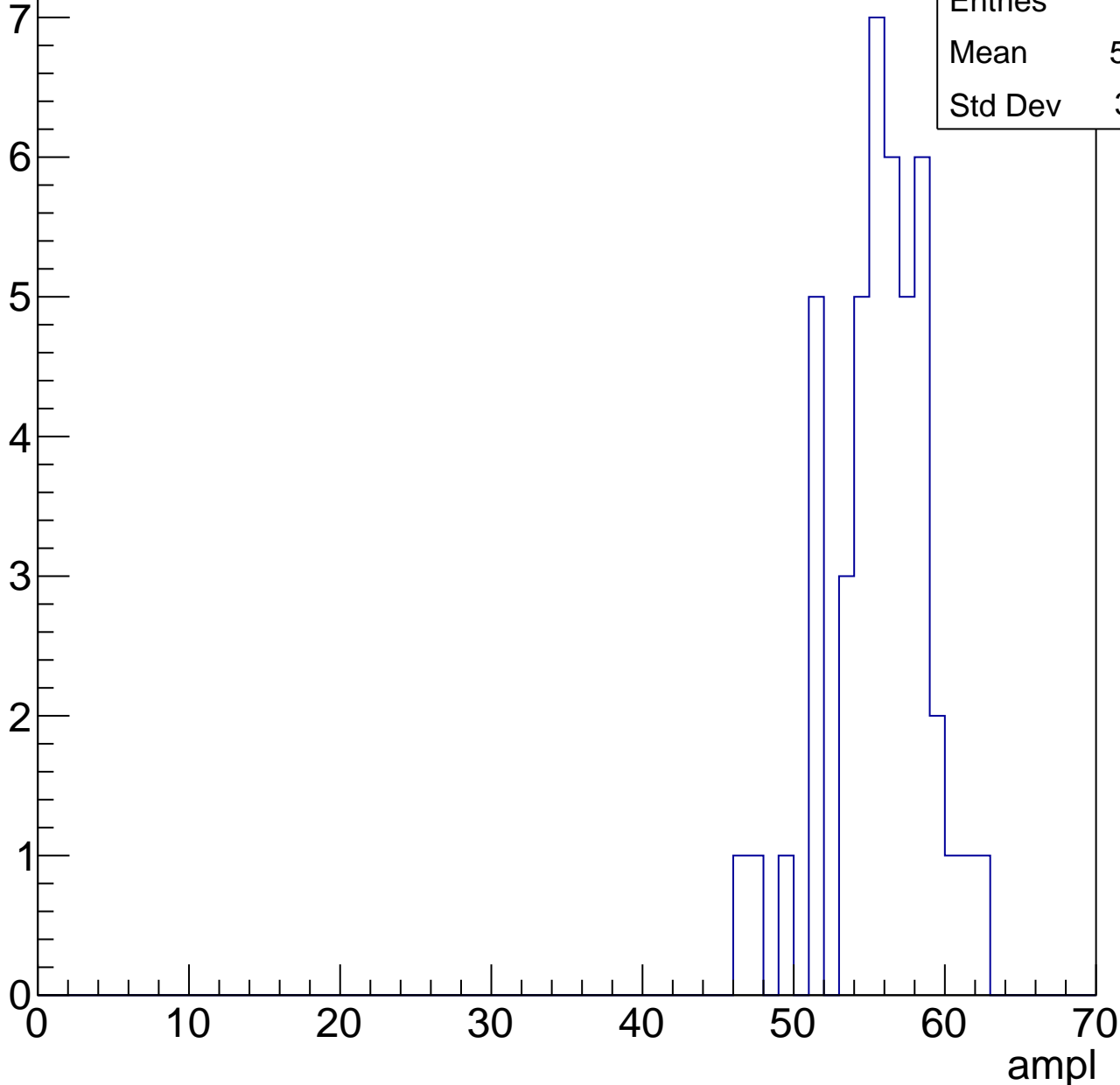


# B1L103S, U16-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

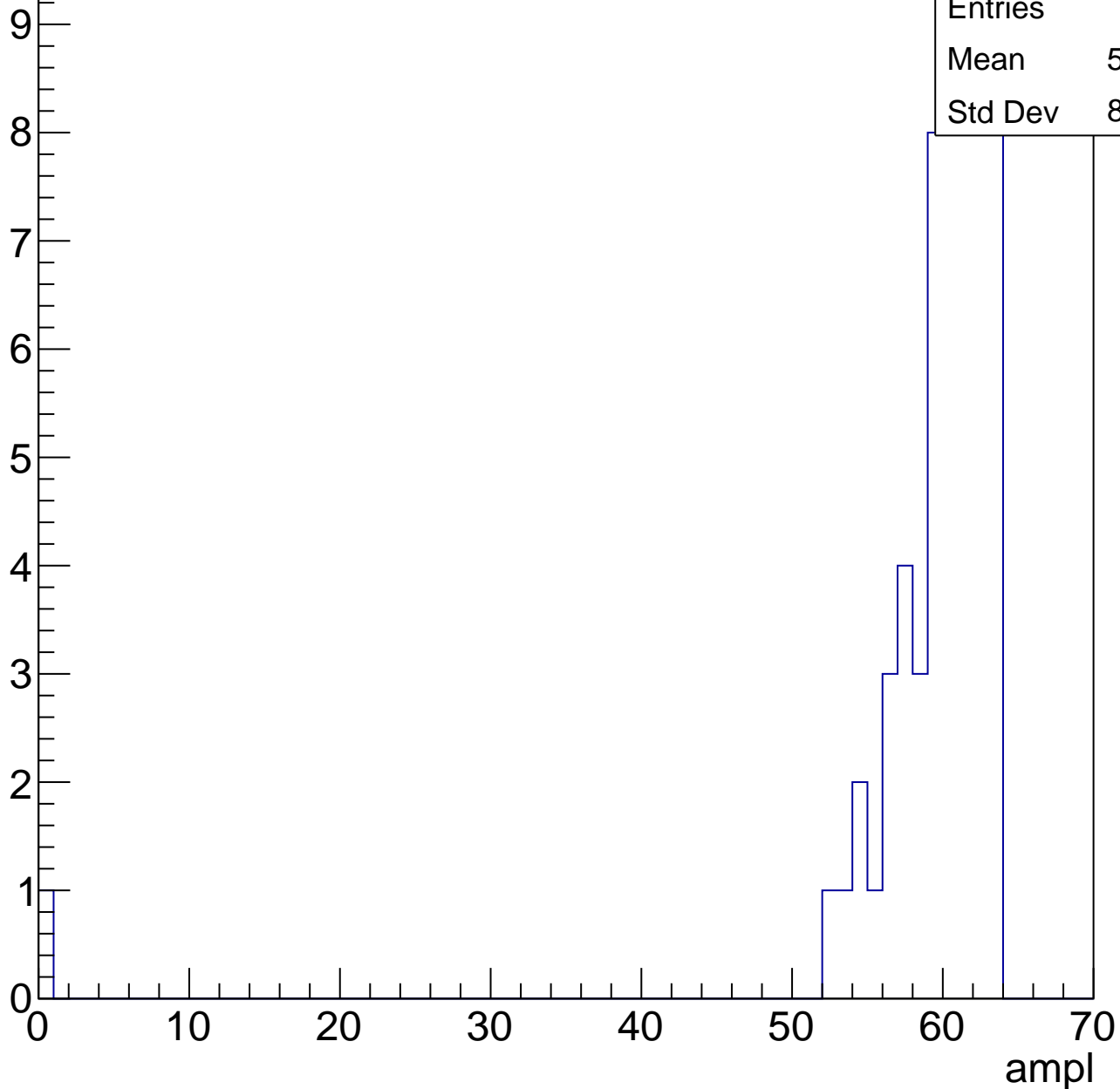
Entries	45
Mean	55.13
Std Dev	3.331



# B1L103S, U16-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U16-ch12, adc0

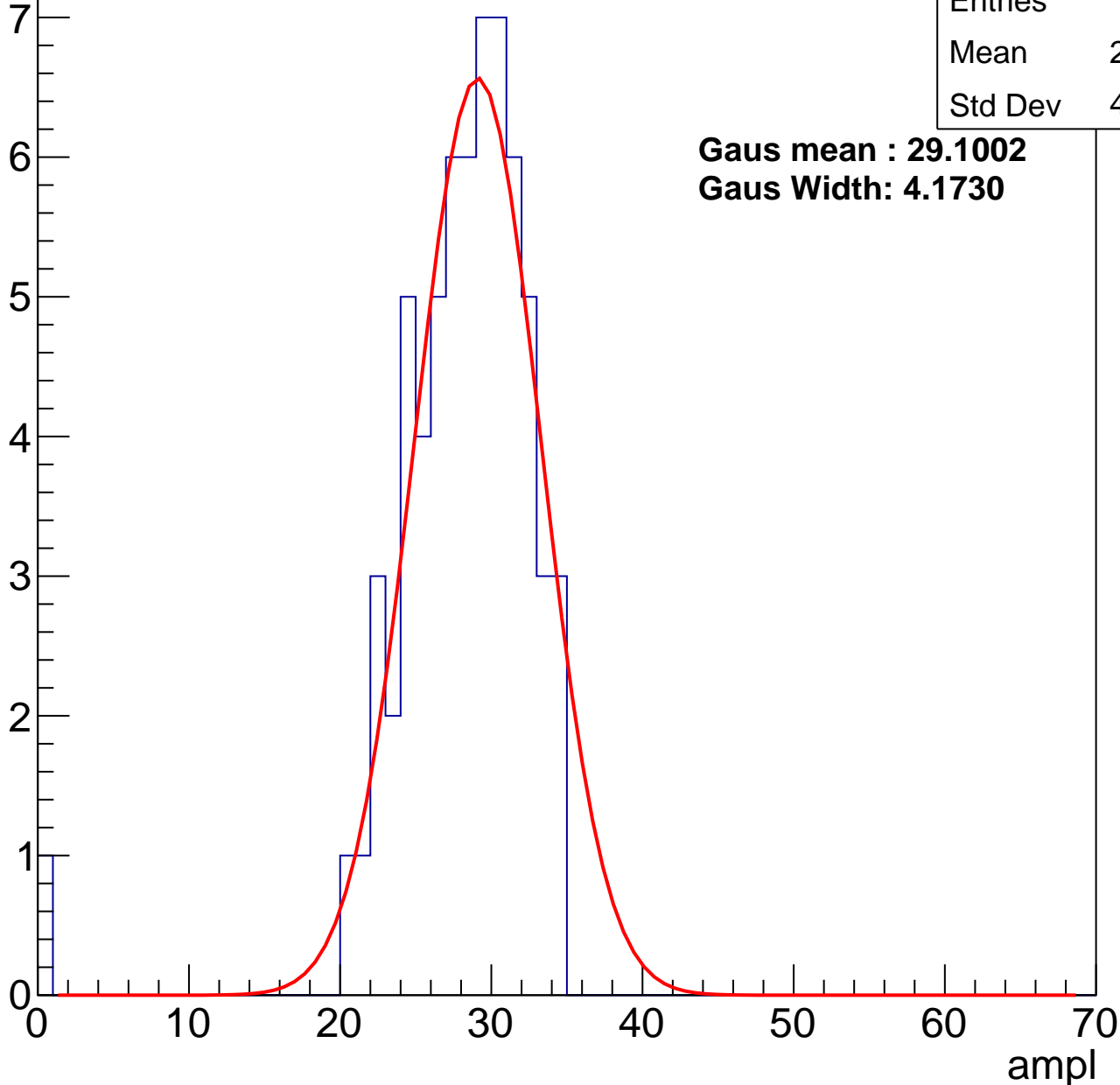
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	27.58
Std Dev	4.864

**Gaus mean : 29.1002**

**Gaus Width: 4.1730**



# B1L103S, U16-ch12, adc1

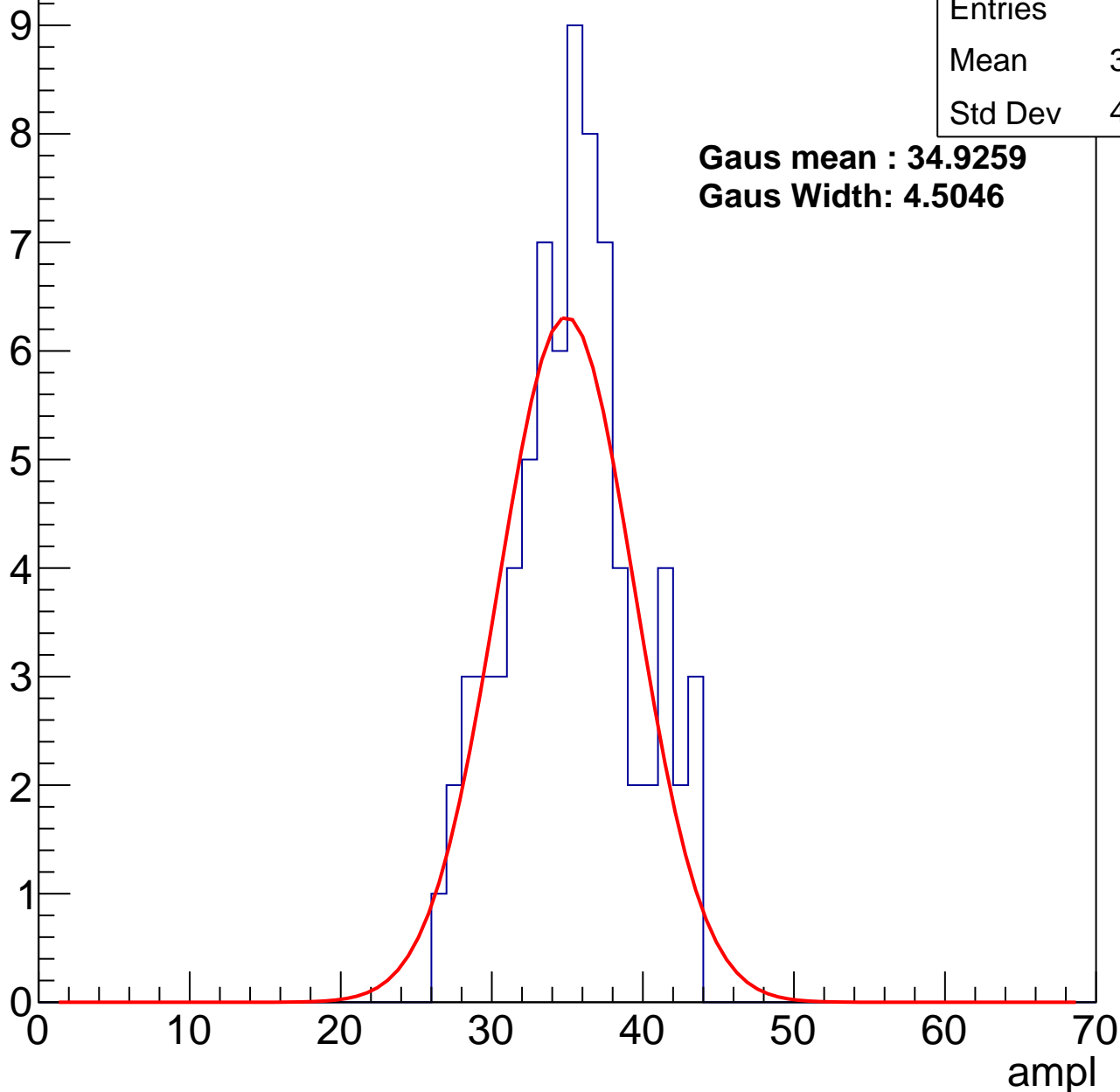
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	34.79
Std Dev	4.109

**Gaus mean : 34.9259**

**Gaus Width: 4.5046**



# B1L103S, U16-ch12, adc2

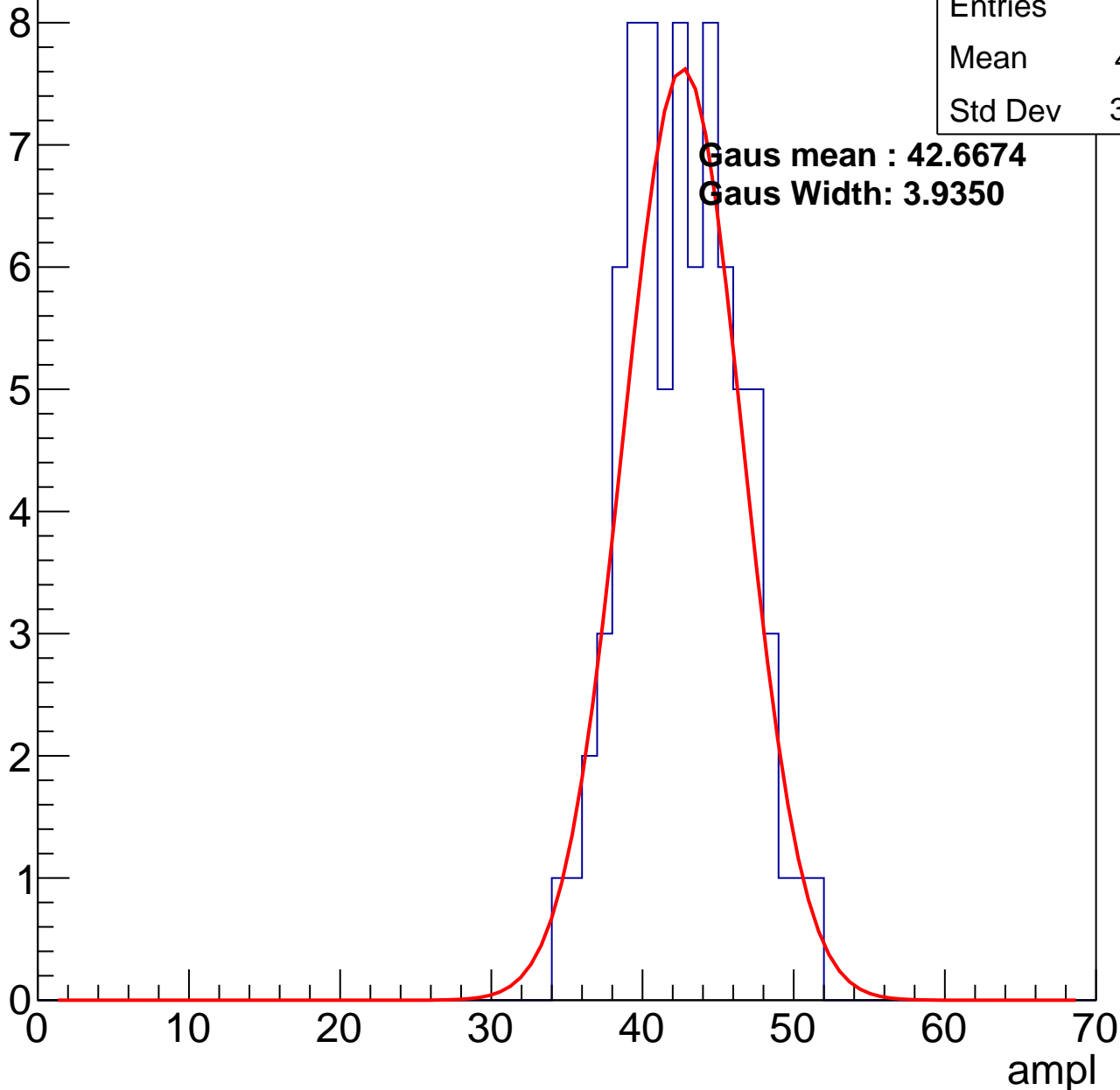
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	42.21
Std Dev	3.688

**Gaus mean : 42.6674**

**Gaus Width: 3.9350**

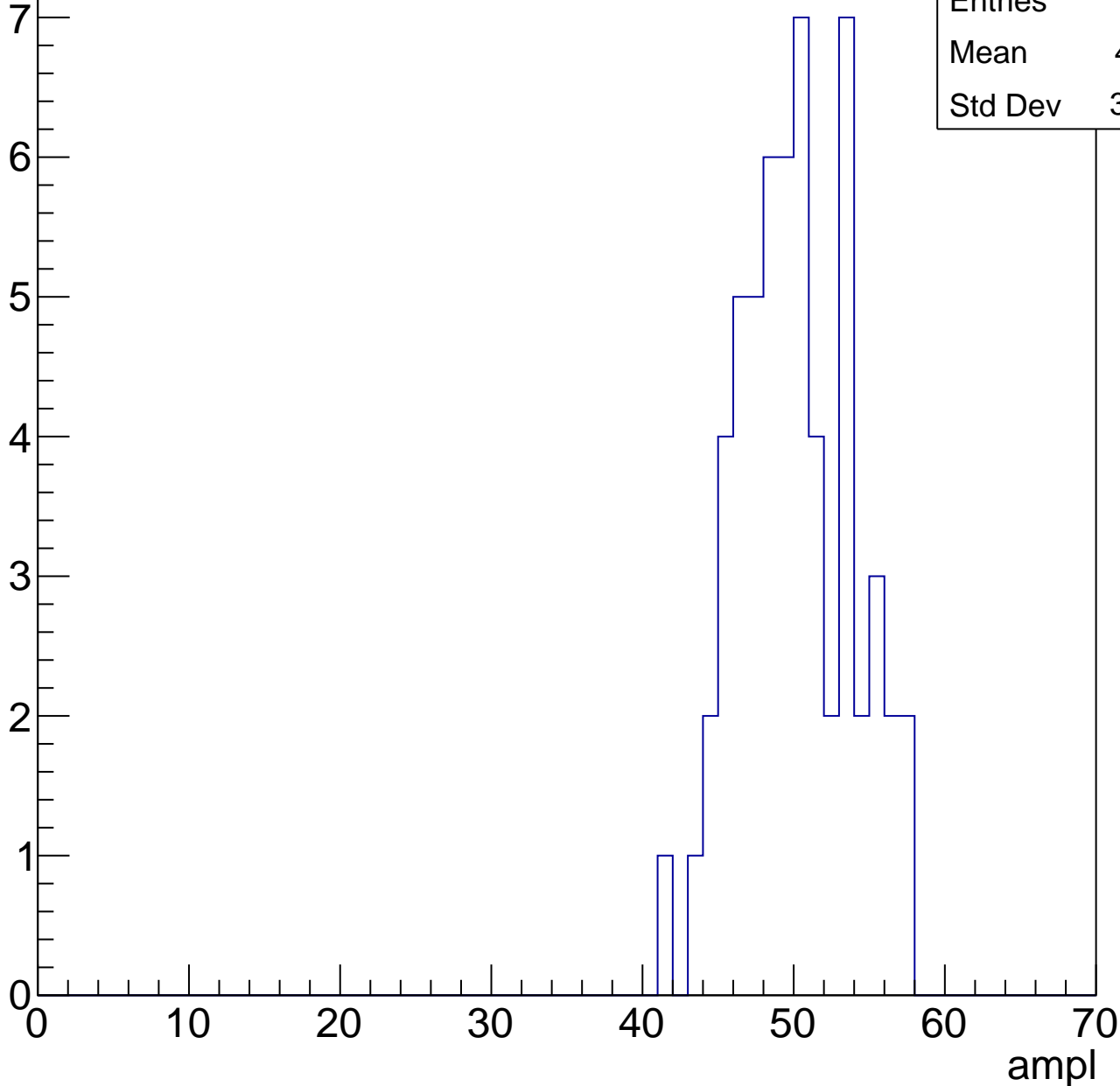


# B1L103S, U16-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	49.61
Std Dev	3.682

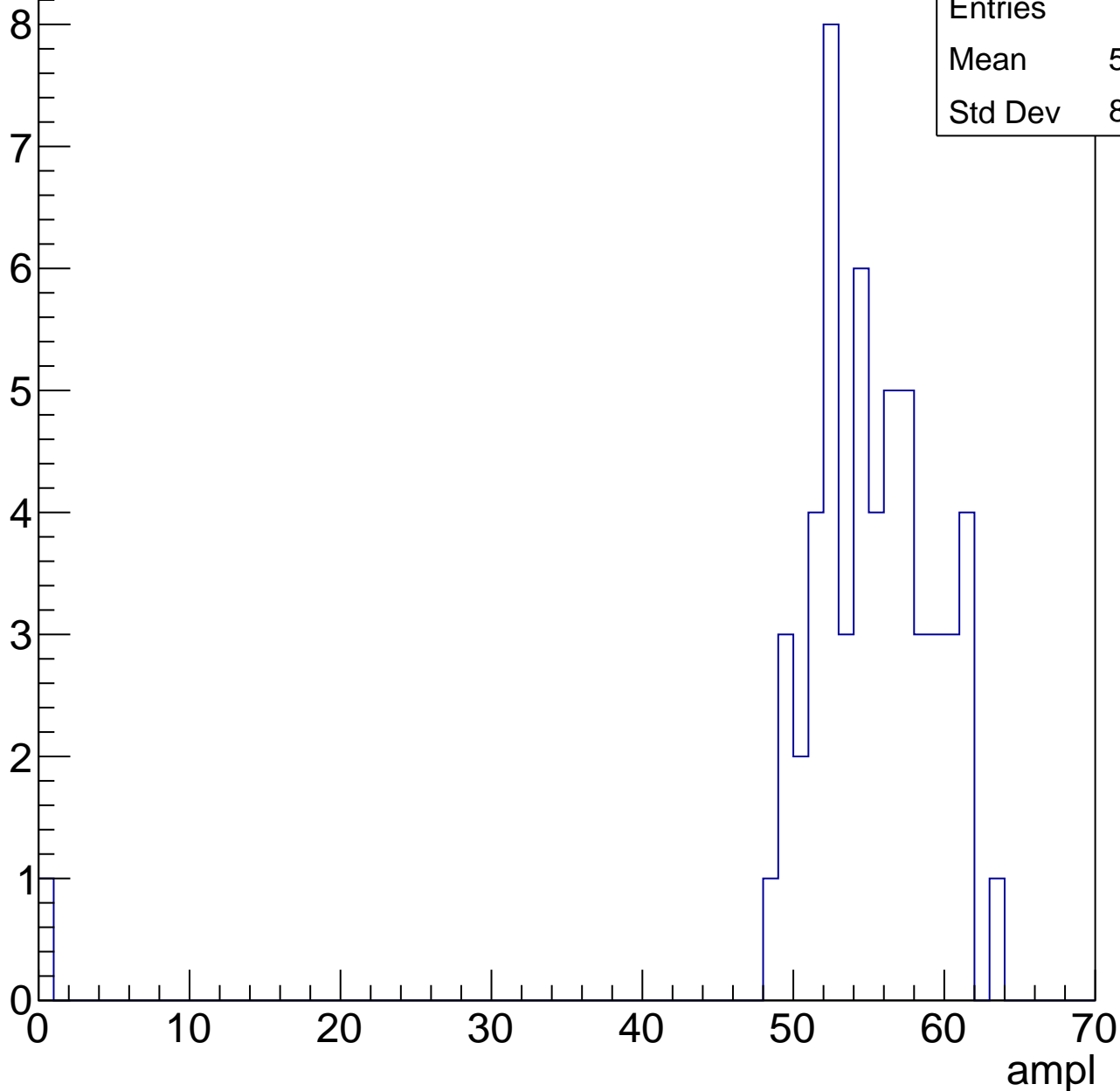


# B1L103S, U16-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	53.95
Std Dev	8.136



# B1L103S, U16-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

7

6

5

4

3

2

1

0

Entries

48

Mean

59.15

Std Dev

2.821

0

10

20

30

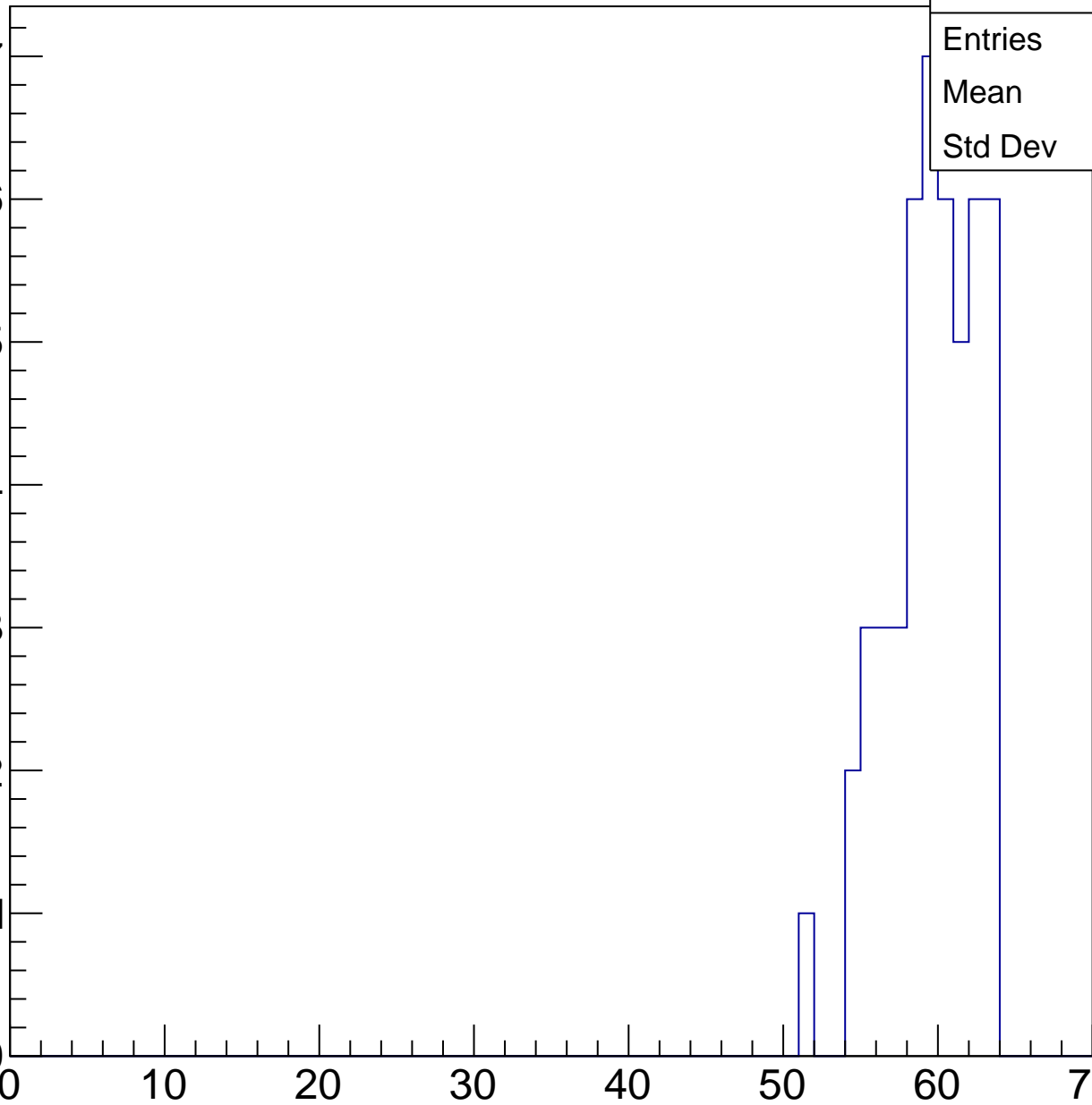
40

50

60

70

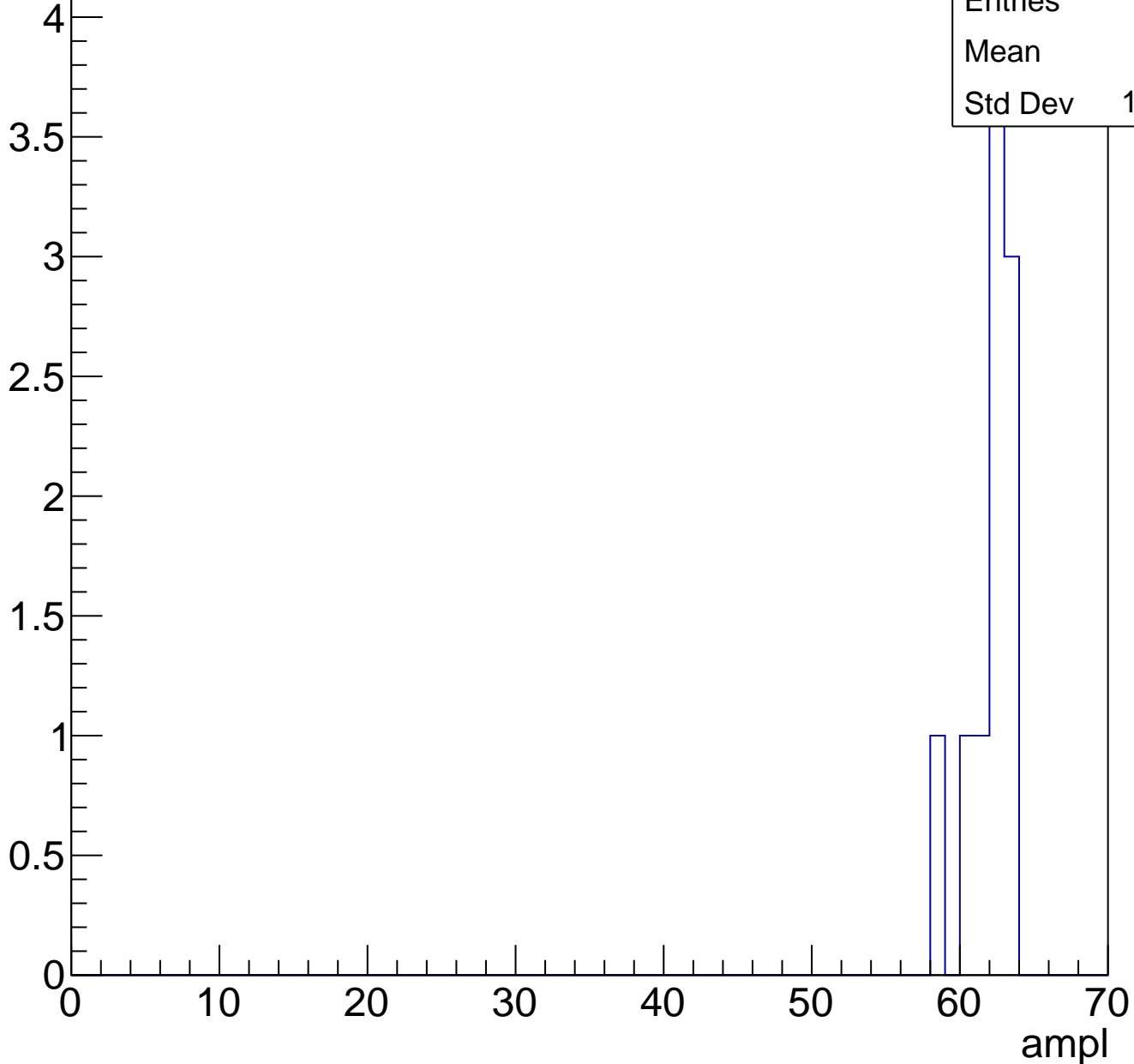
ampl



# B1L103S, U16-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	10
Mean	61.6
Std Dev	1.497



# B1L103S, U16-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U16-ch13, adc0

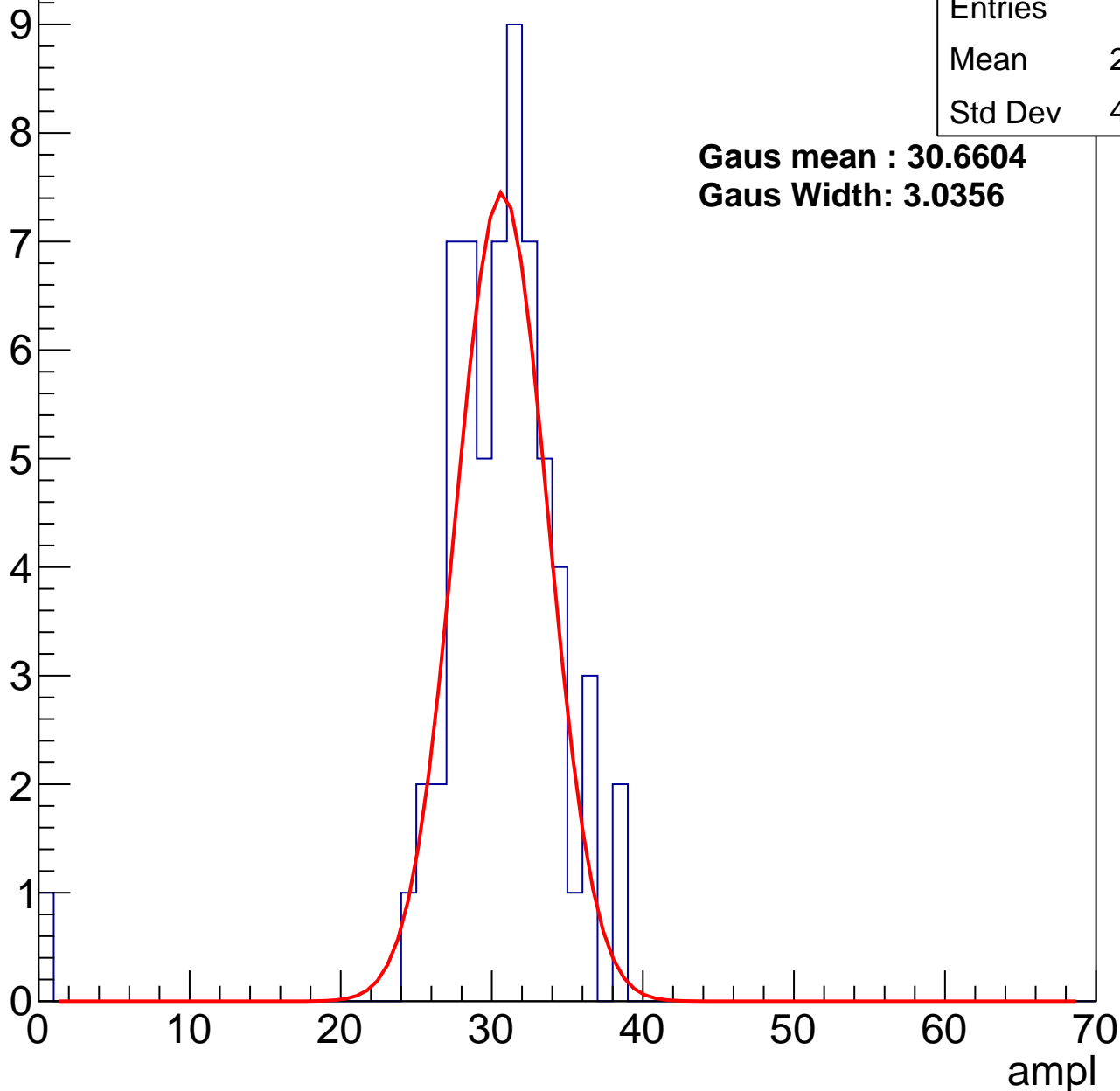
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	29.98
Std Dev	4.914

**Gaus mean : 30.6604**

**Gaus Width: 3.0356**



# B1L103S, U16-ch13, adc1

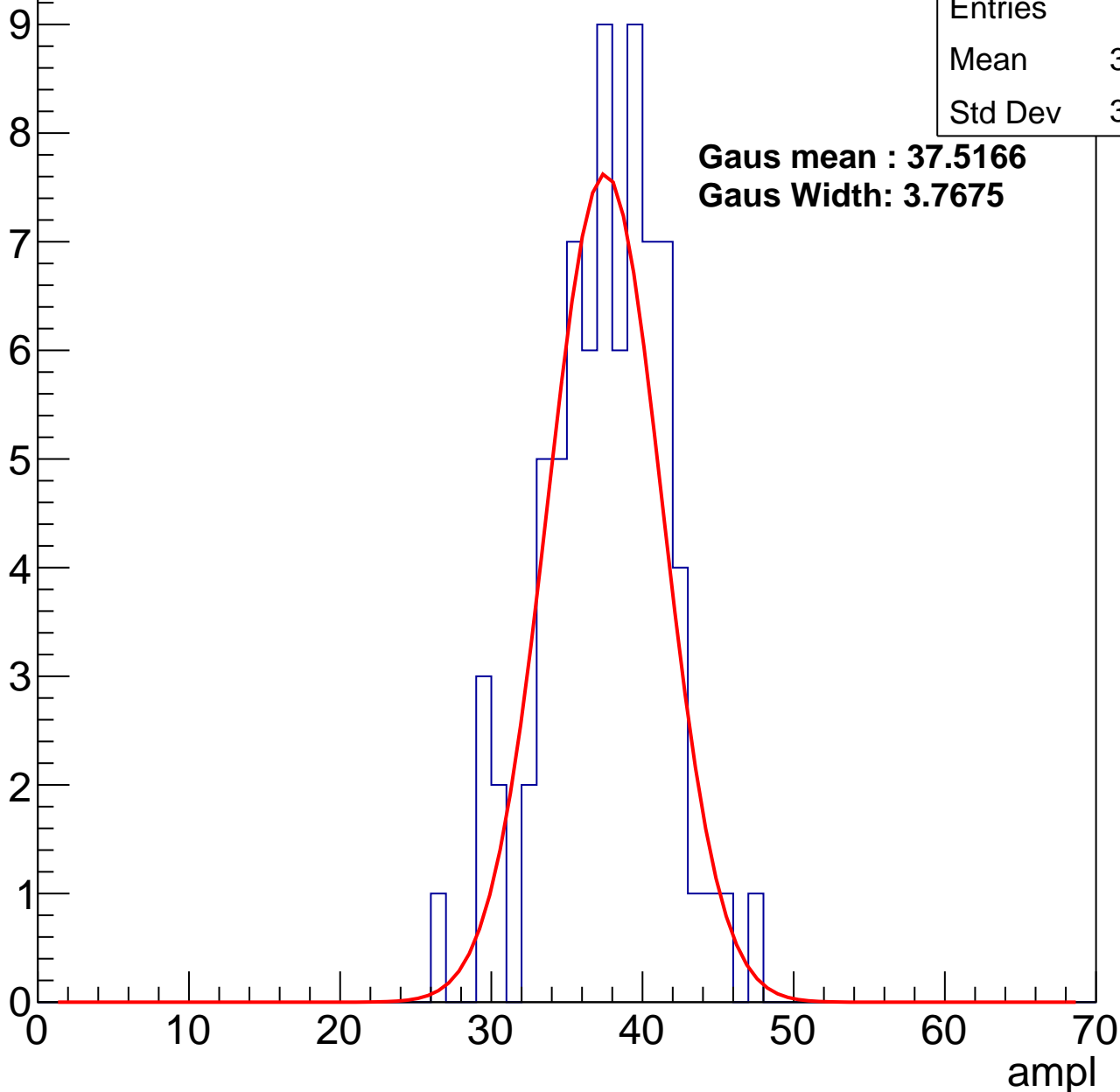
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	37.13
Std Dev	3.922

**Gaus mean : 37.5166**

**Gaus Width: 3.7675**



# B1L103S, U16-ch13, adc2

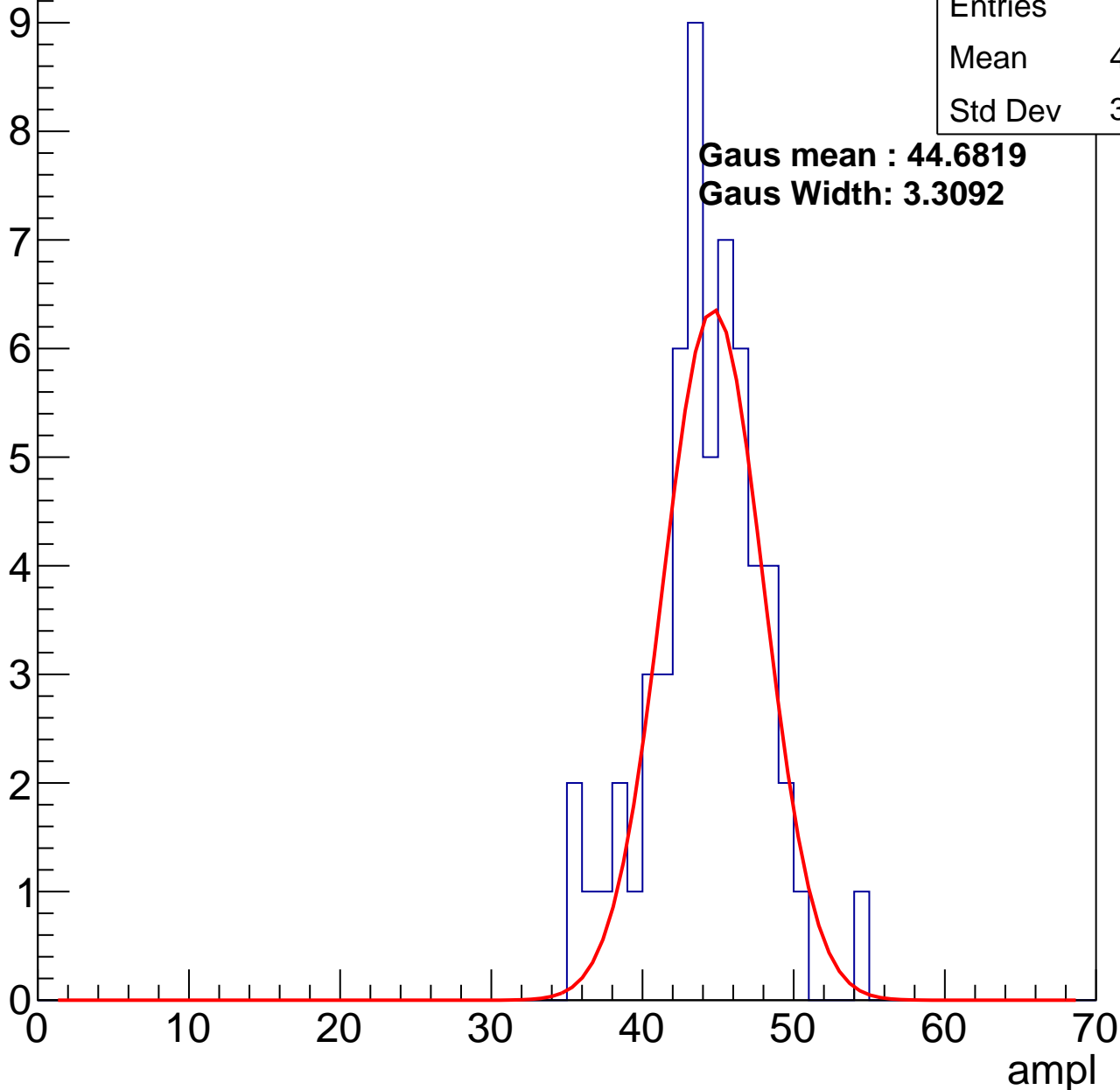
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	43.67
Std Dev	3.692

**Gaus mean : 44.6819**

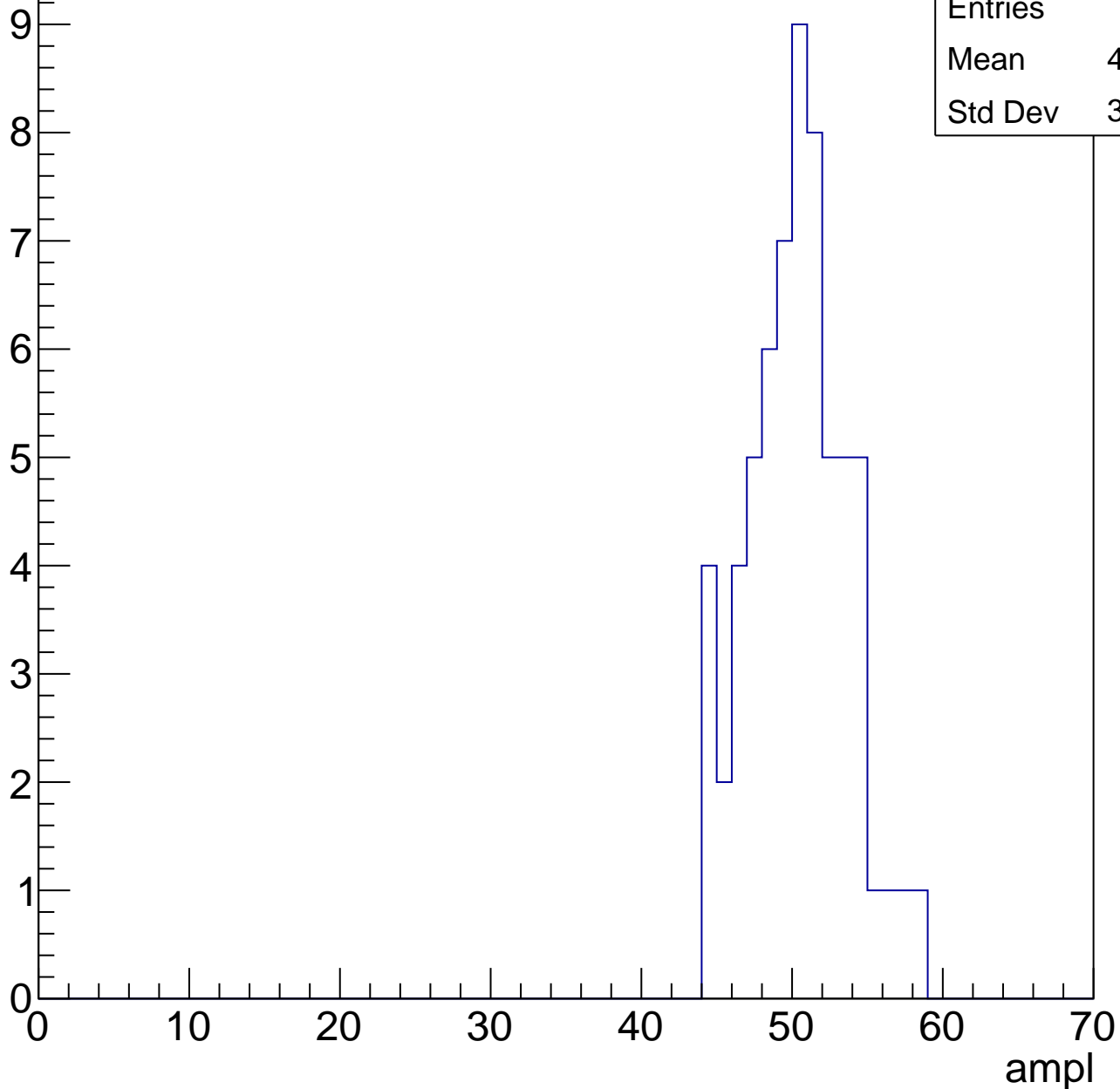
**Gaus Width: 3.3092**



# B1L103S, U16-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



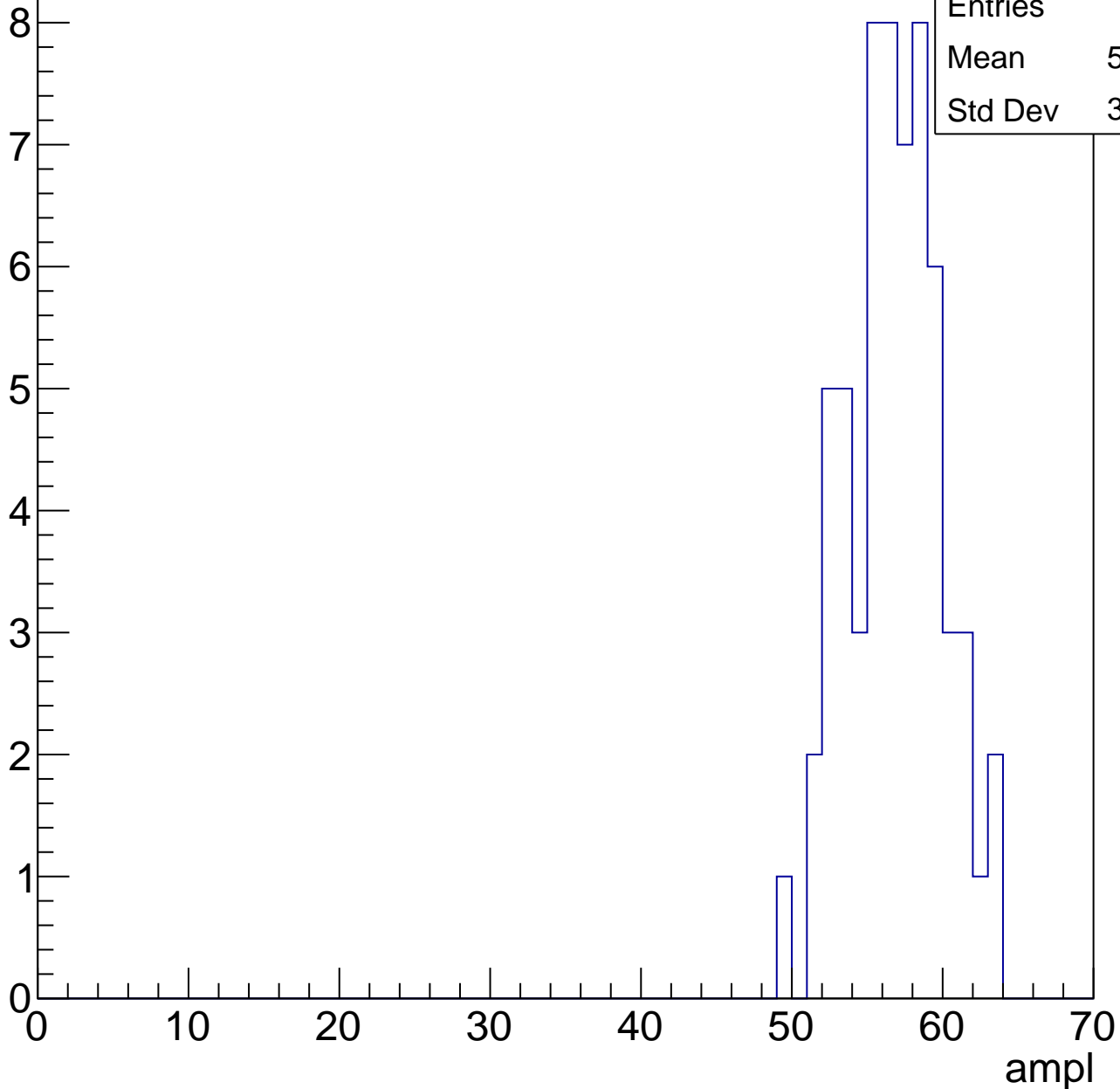
Entries	64
Mean	49.92
Std Dev	3.213

# B1L103S, U16-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	56.35
Std Dev	3.075

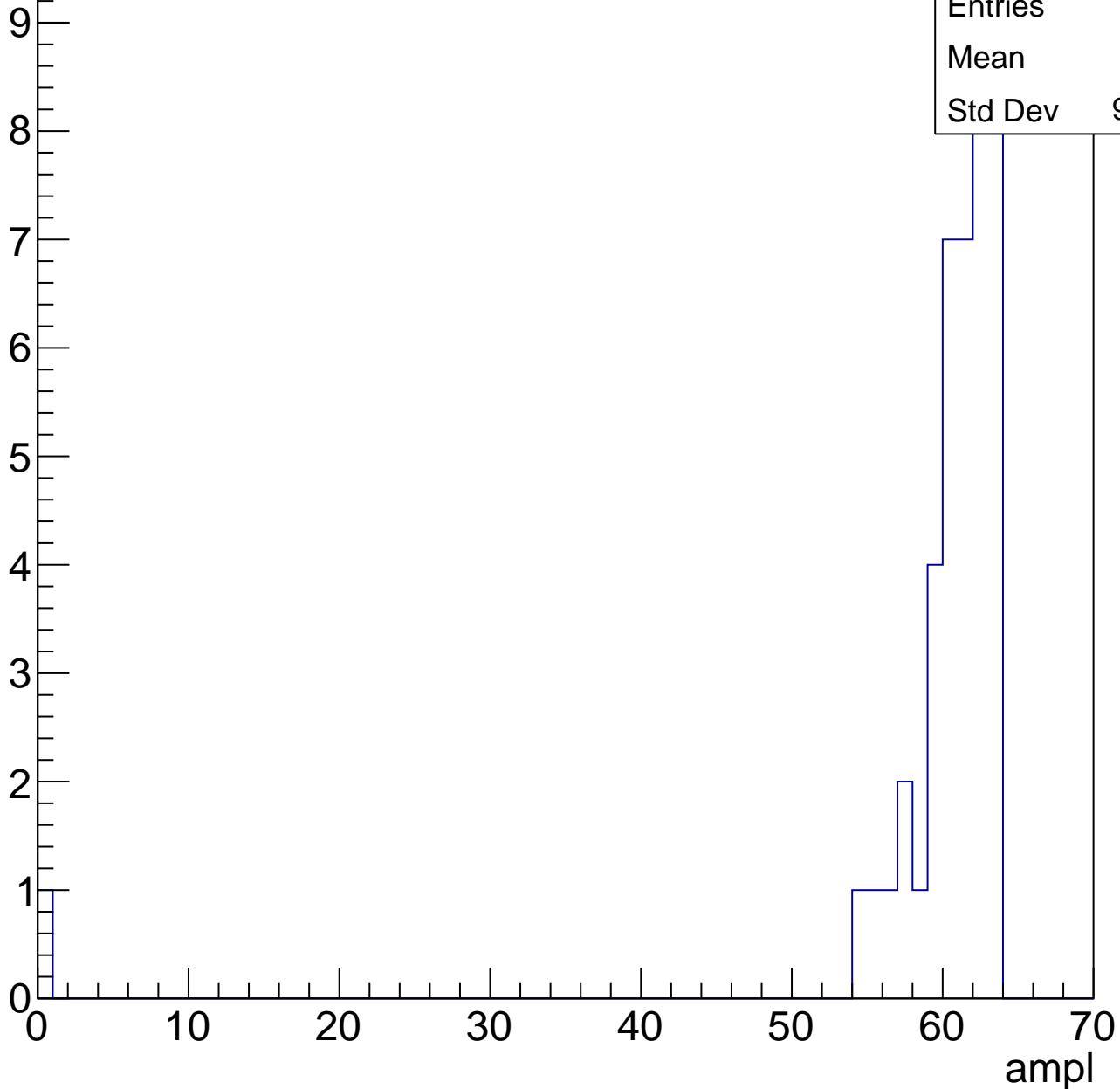


# B1L103S, U16-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	42
Mean	59.1
Std Dev	9.491



# B1L103S, U16-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L103S, U16-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U16-ch14, adc0

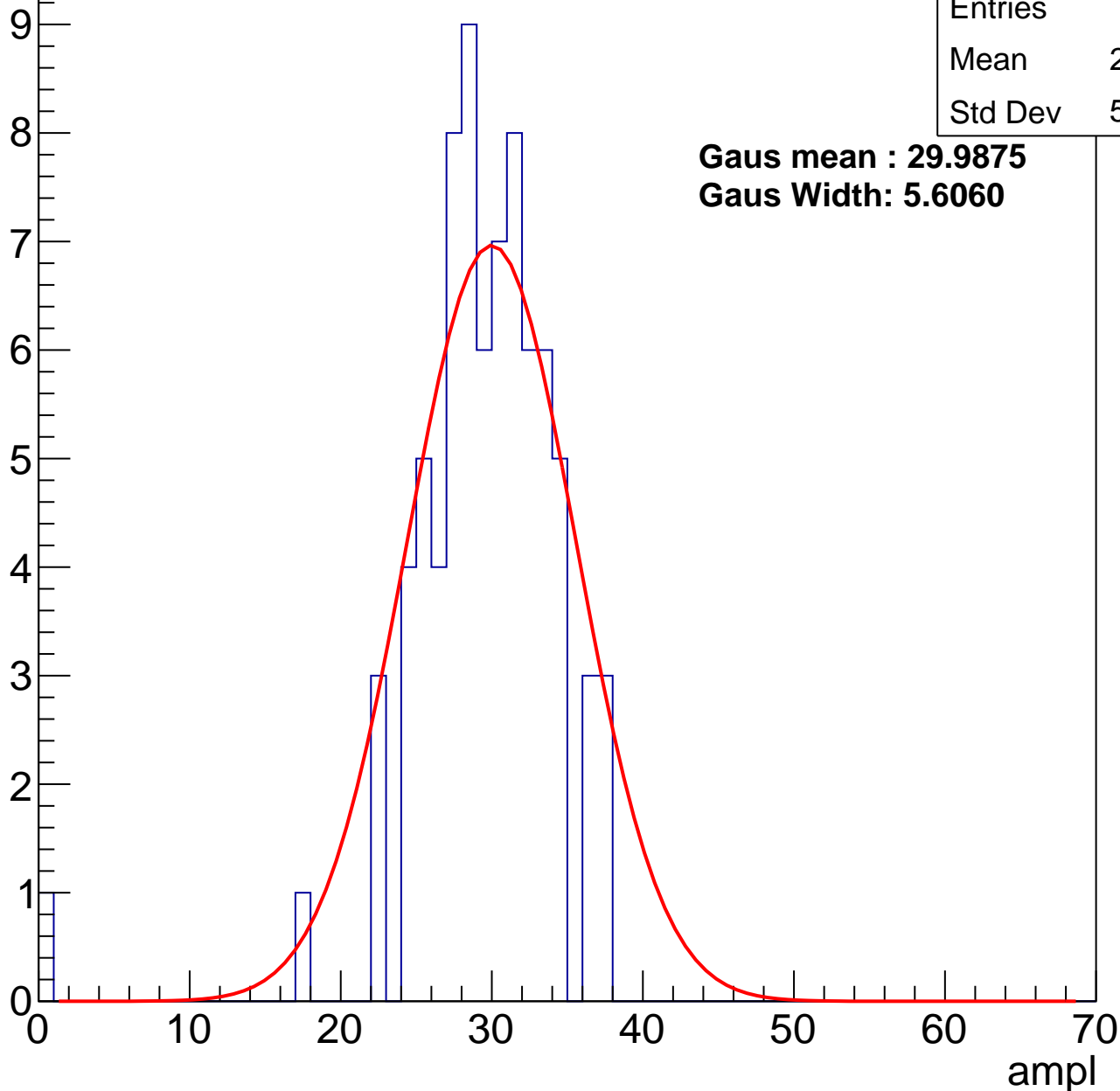
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	28.95
Std Dev	5.084

**Gaus mean : 29.9875**

**Gaus Width: 5.6060**



# B1L103S, U16-ch14, adc1

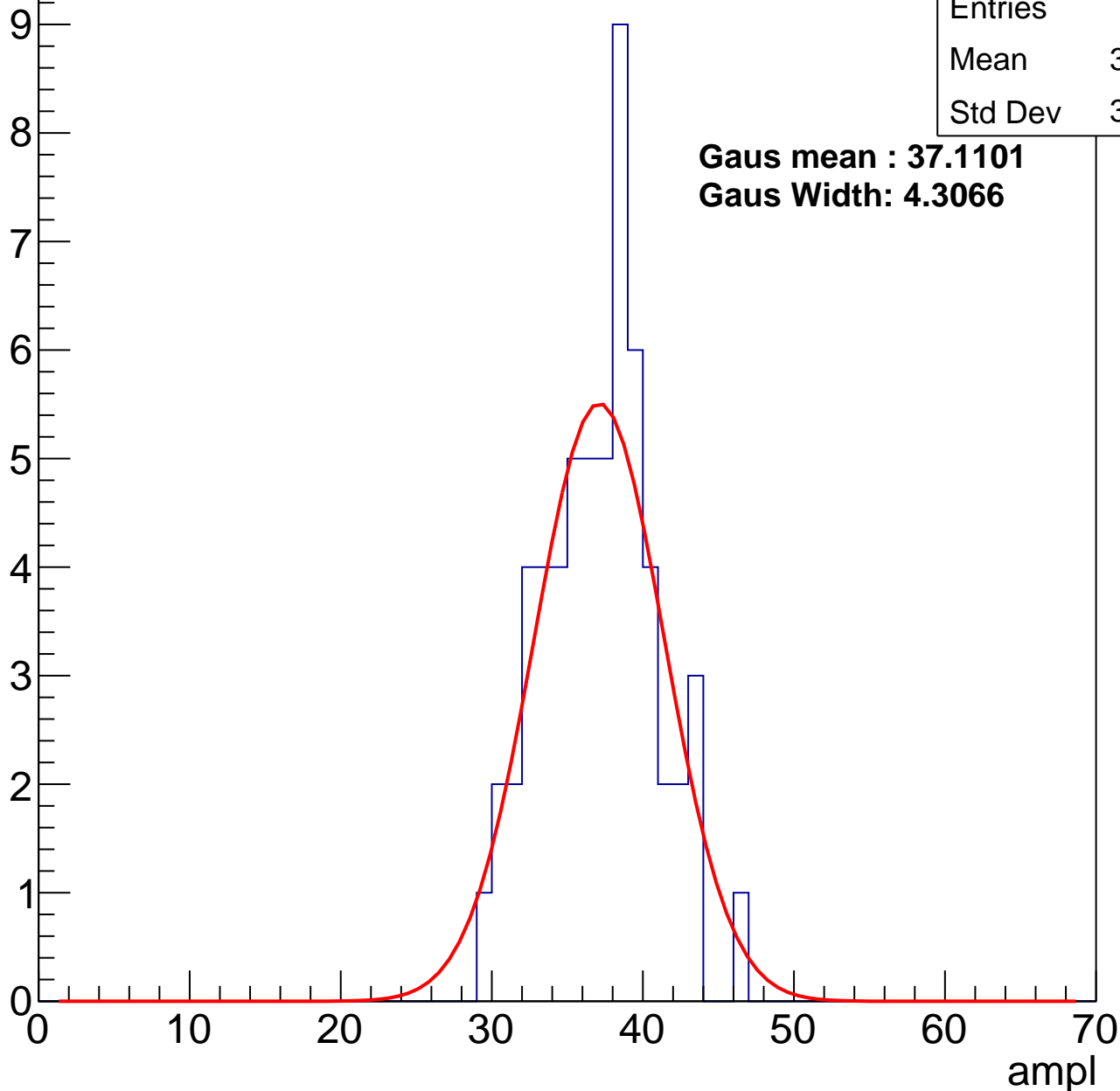
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	36.68
Std Dev	3.666

**Gaus mean : 37.1101**

**Gaus Width: 4.3066**



# B1L103S, U16-ch14, adc2

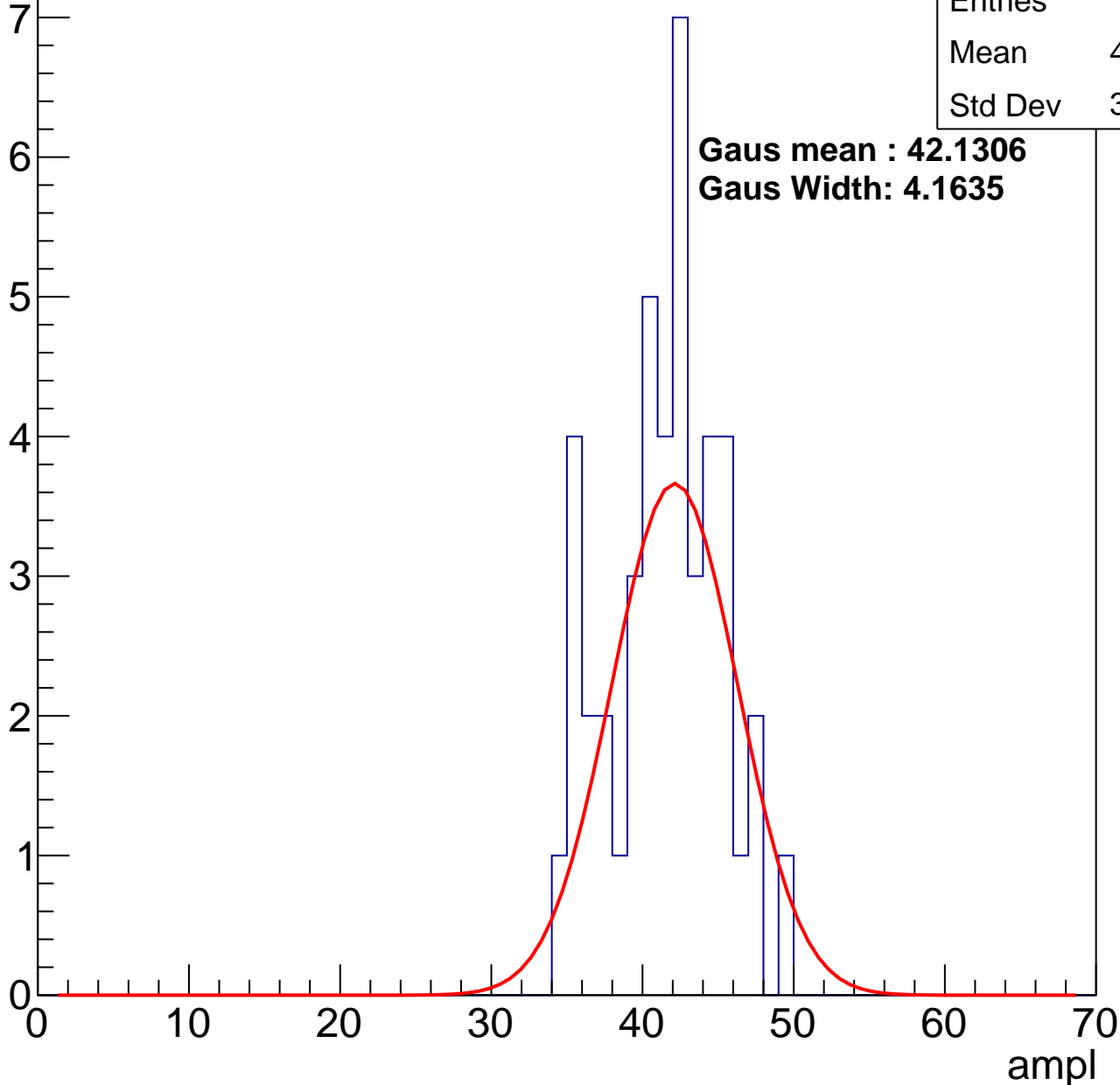
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	41.07
Std Dev	3.633

**Gaus mean : 42.1306**

**Gaus Width: 4.1635**



# B1L103S, U16-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	107
Mean	48.86
Std Dev	4.513

Entry

10

8

6

4

2

0

0

10

20

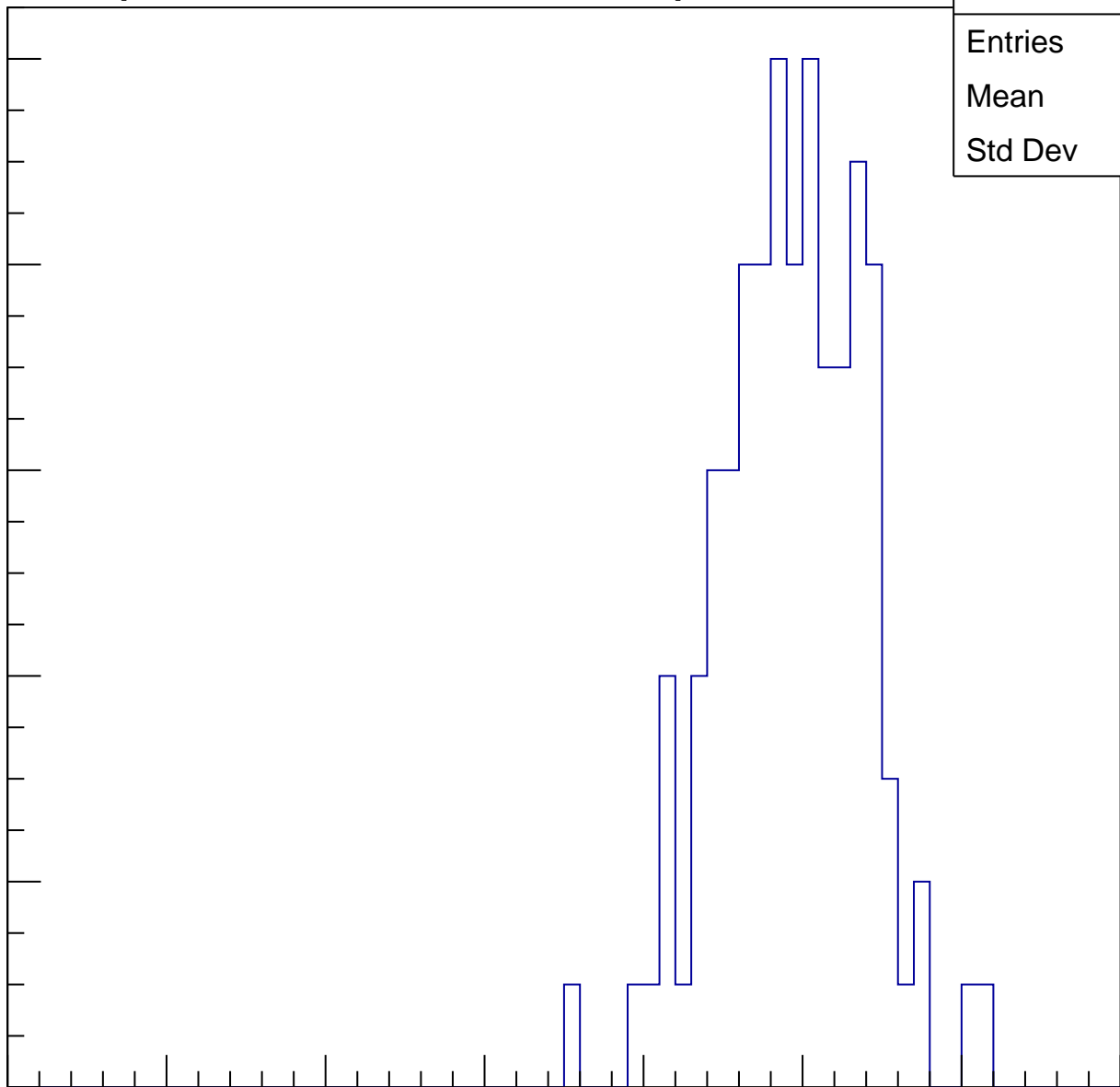
30

40

50

60

ampl

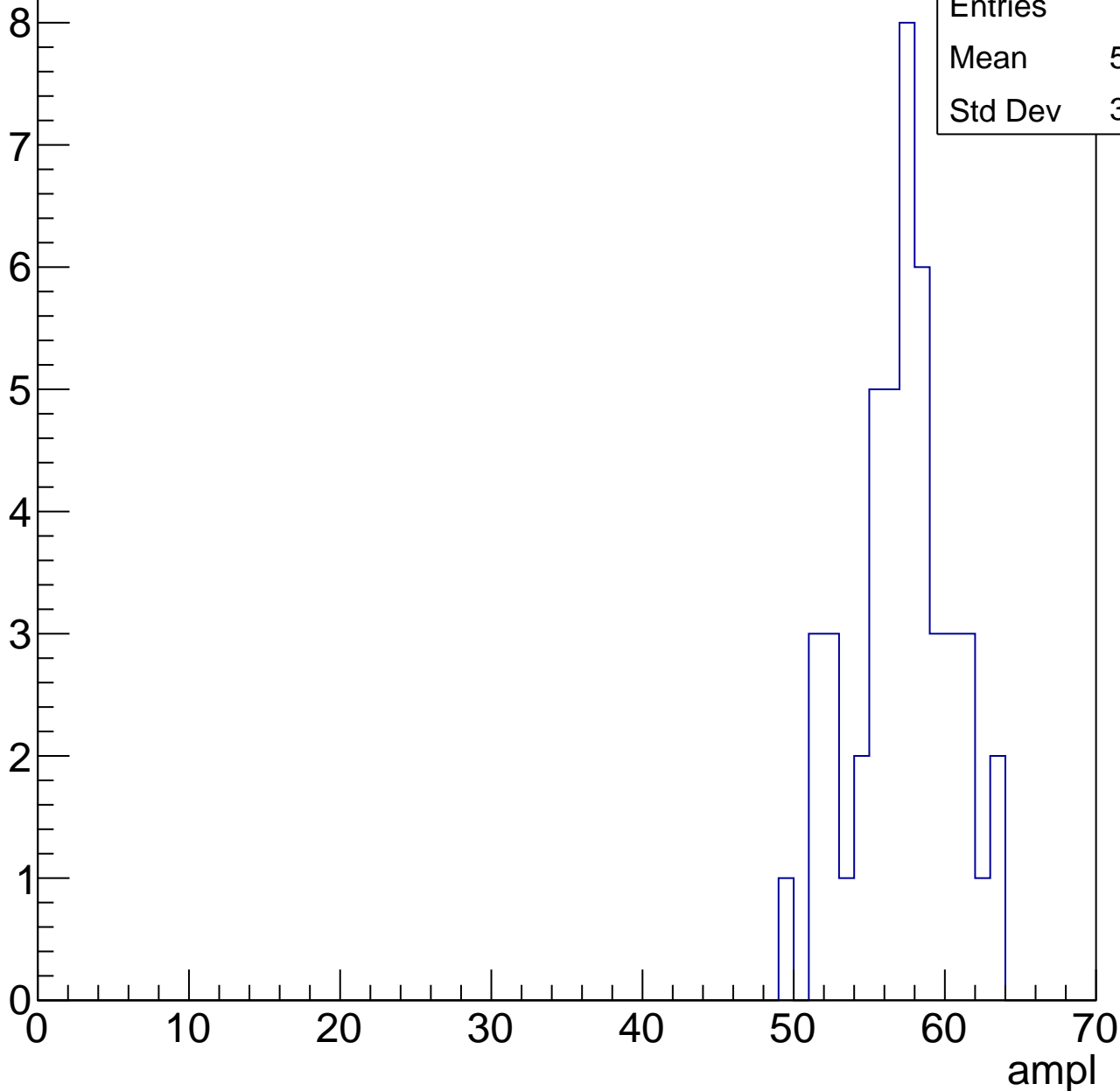


# B1L103S, U16-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	56.65
Std Dev	3.265

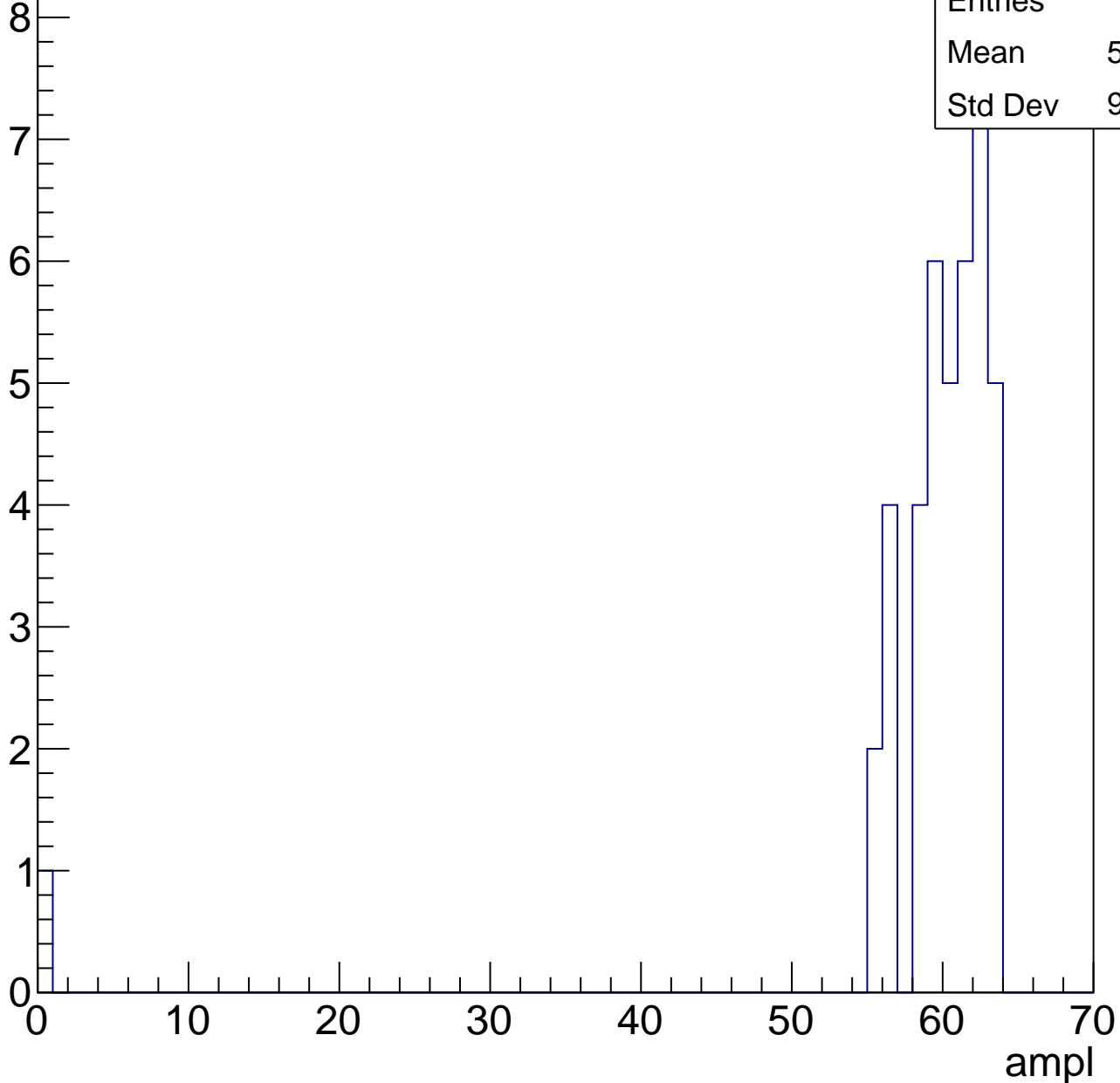


# B1L103S, U16-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

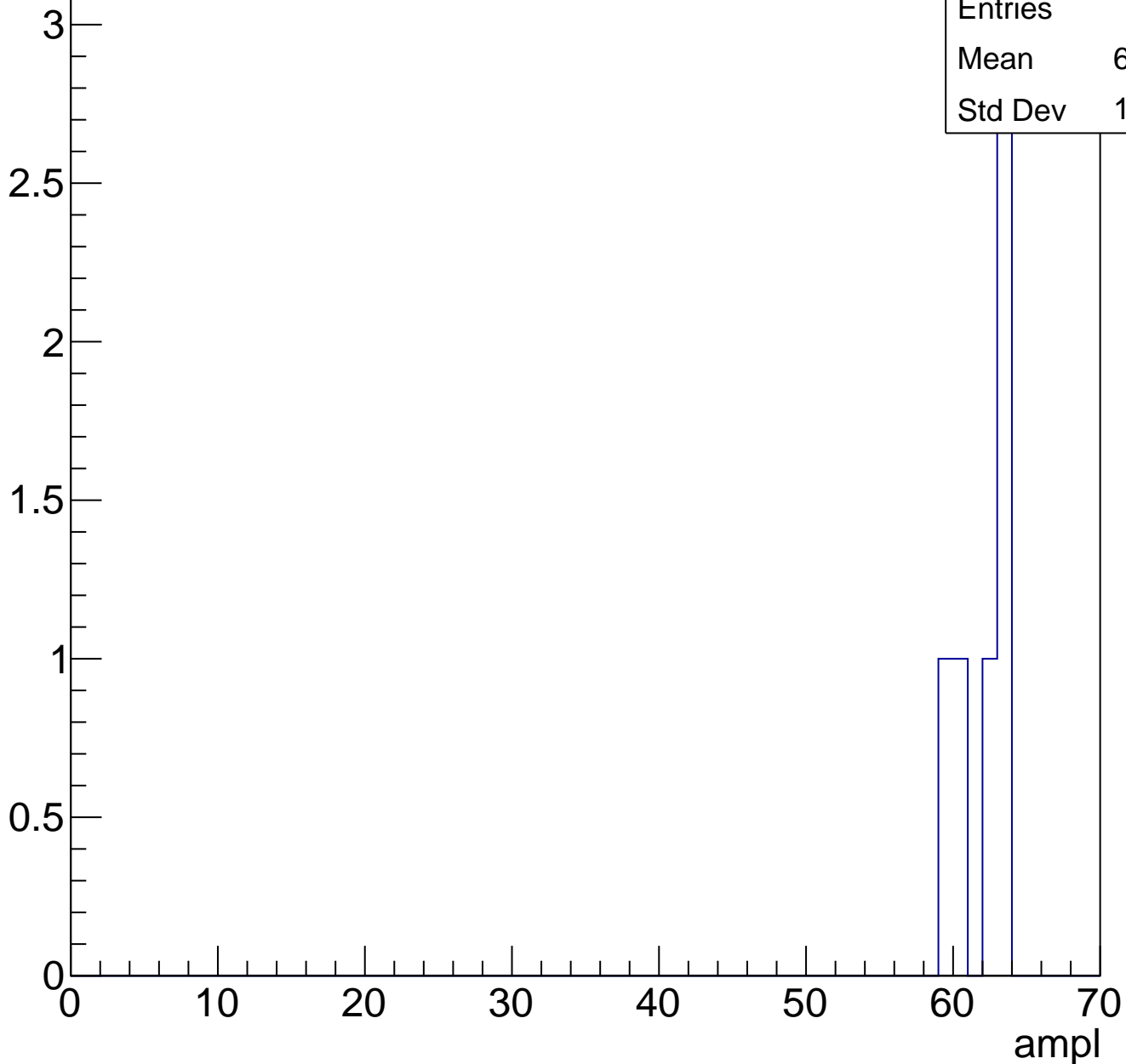
Entries	41
Mean	58.46
Std Dev	9.528



# B1L103S, U16-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U16-ch15, adc0

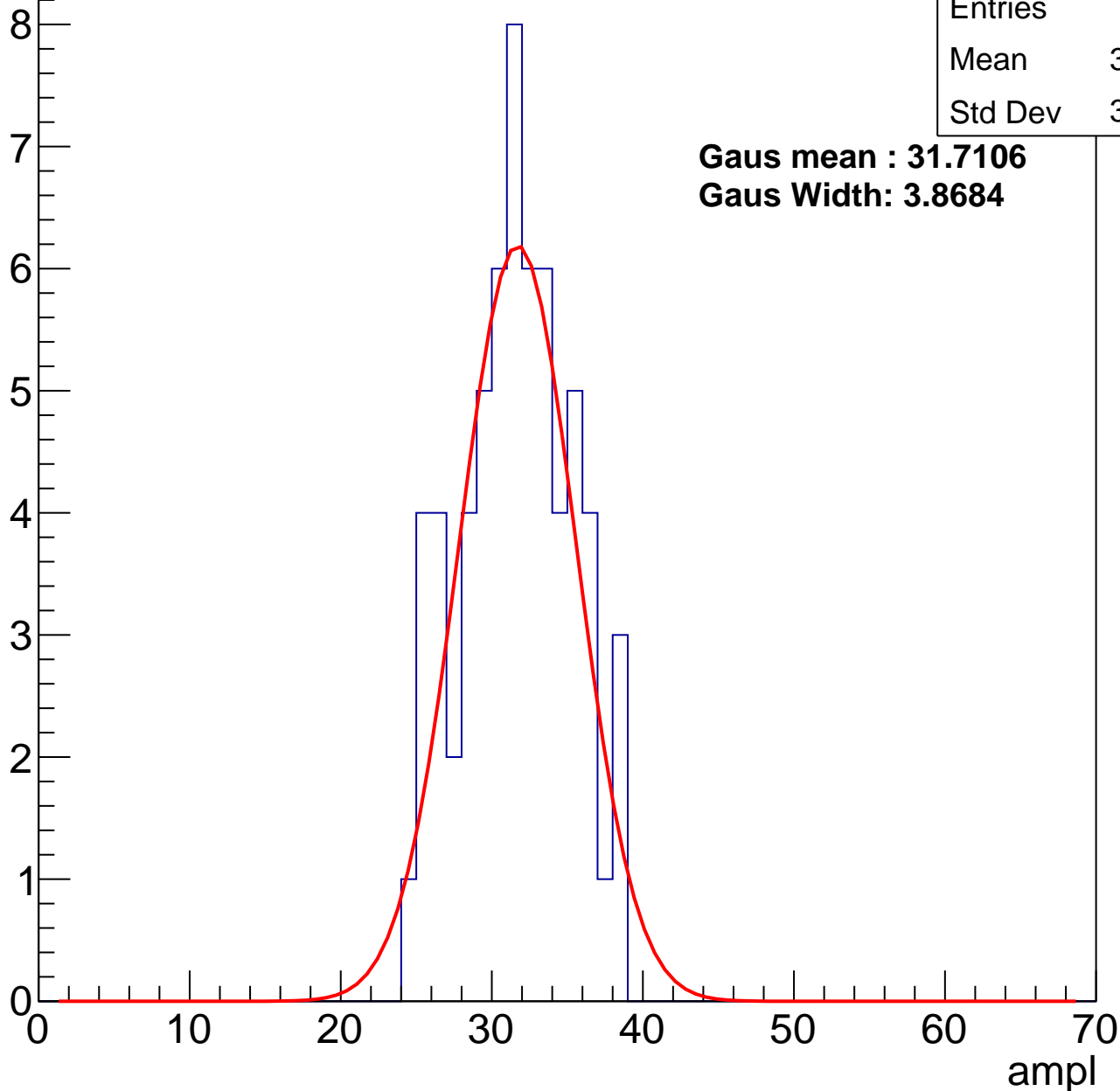
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	31.16
Std Dev	3.595

**Gaus mean : 31.7106**

**Gaus Width: 3.8684**



# B1L103S, U16-ch15, adc1

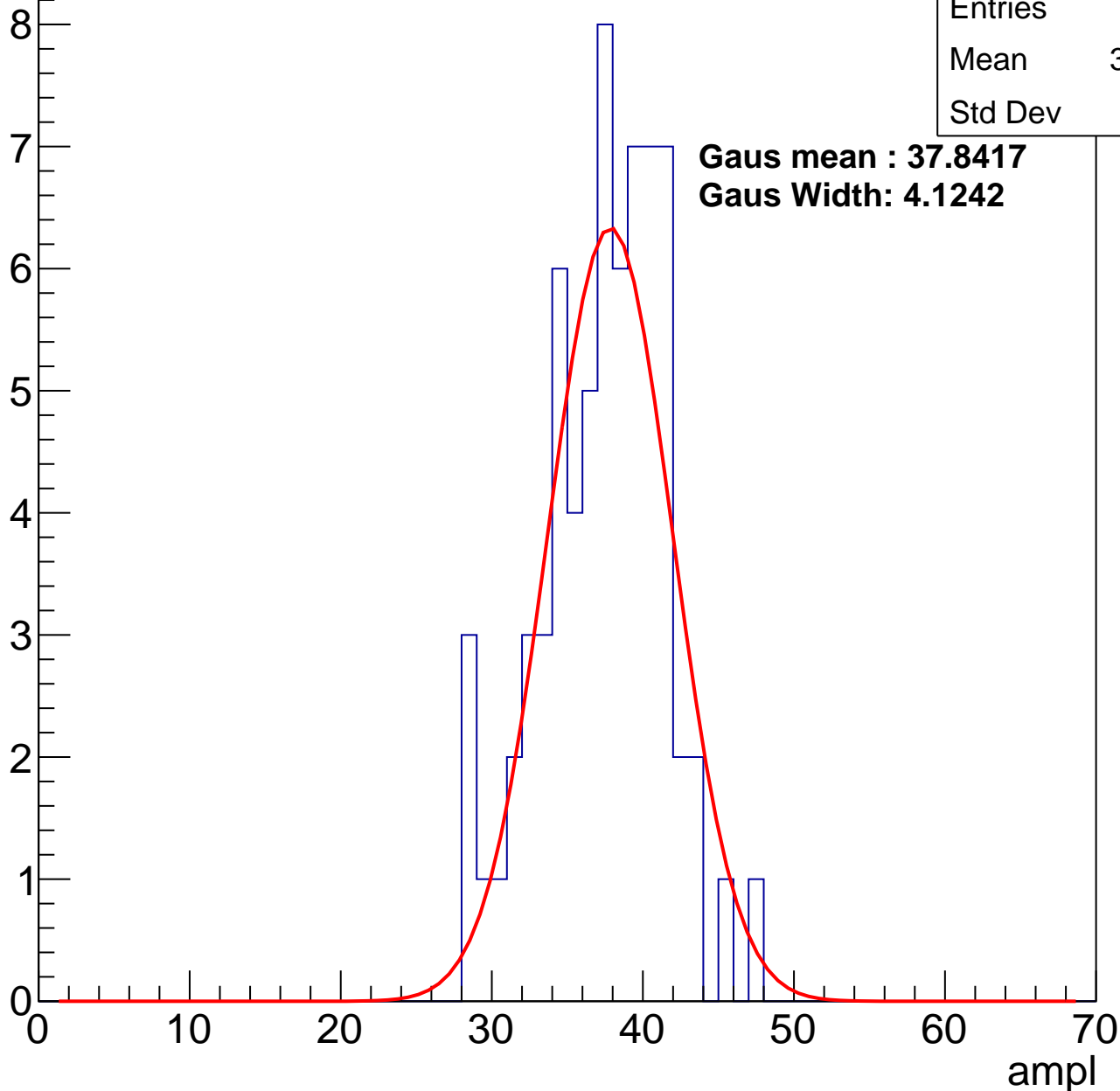
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	36.96
Std Dev	4.03

**Gaus mean : 37.8417**

**Gaus Width: 4.1242**



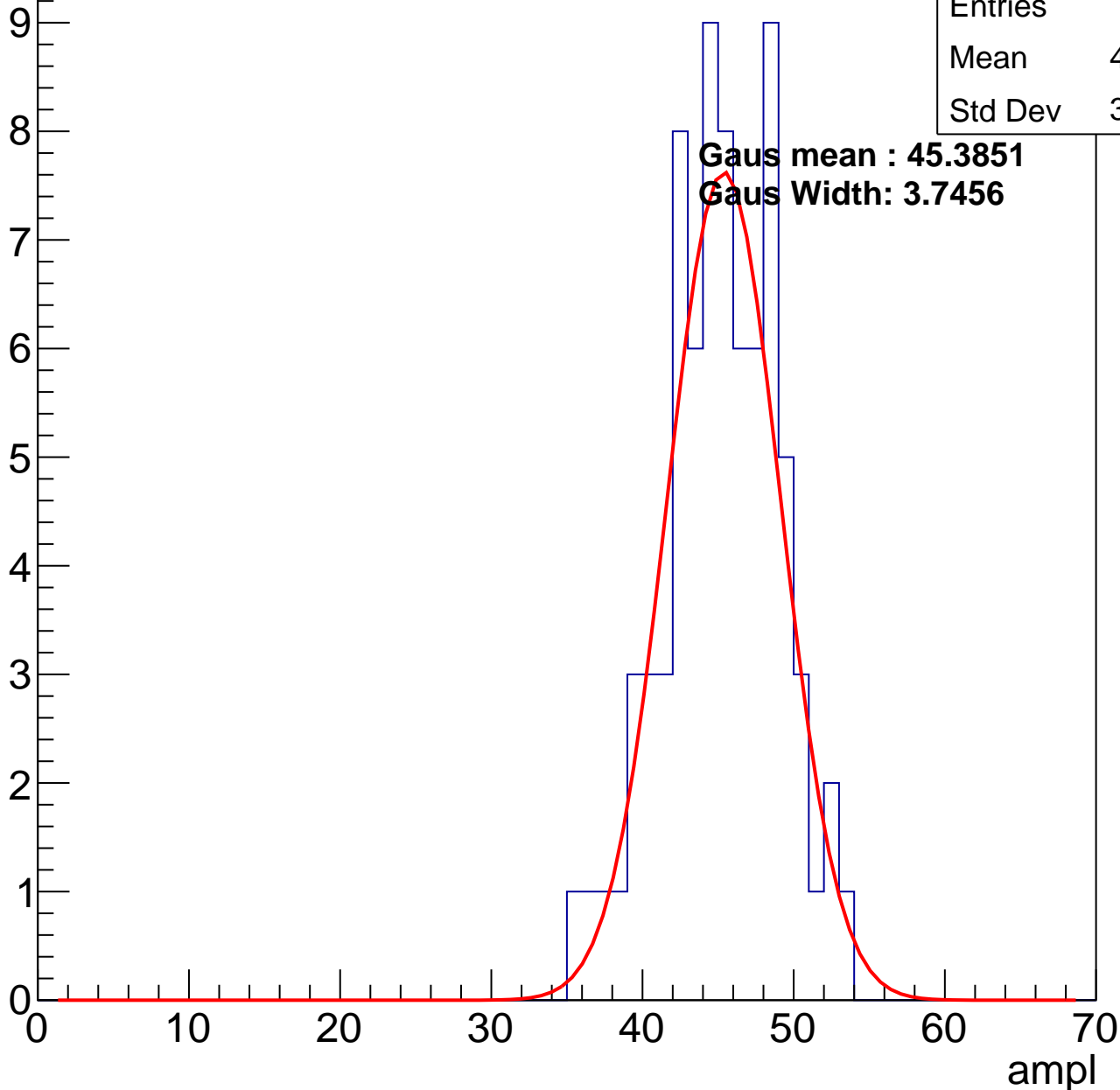
# B1L103S, U16-ch15, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	44.79
Std Dev	3.764

**Gaus mean : 45.3851**  
**Gaus Width: 3.7456**

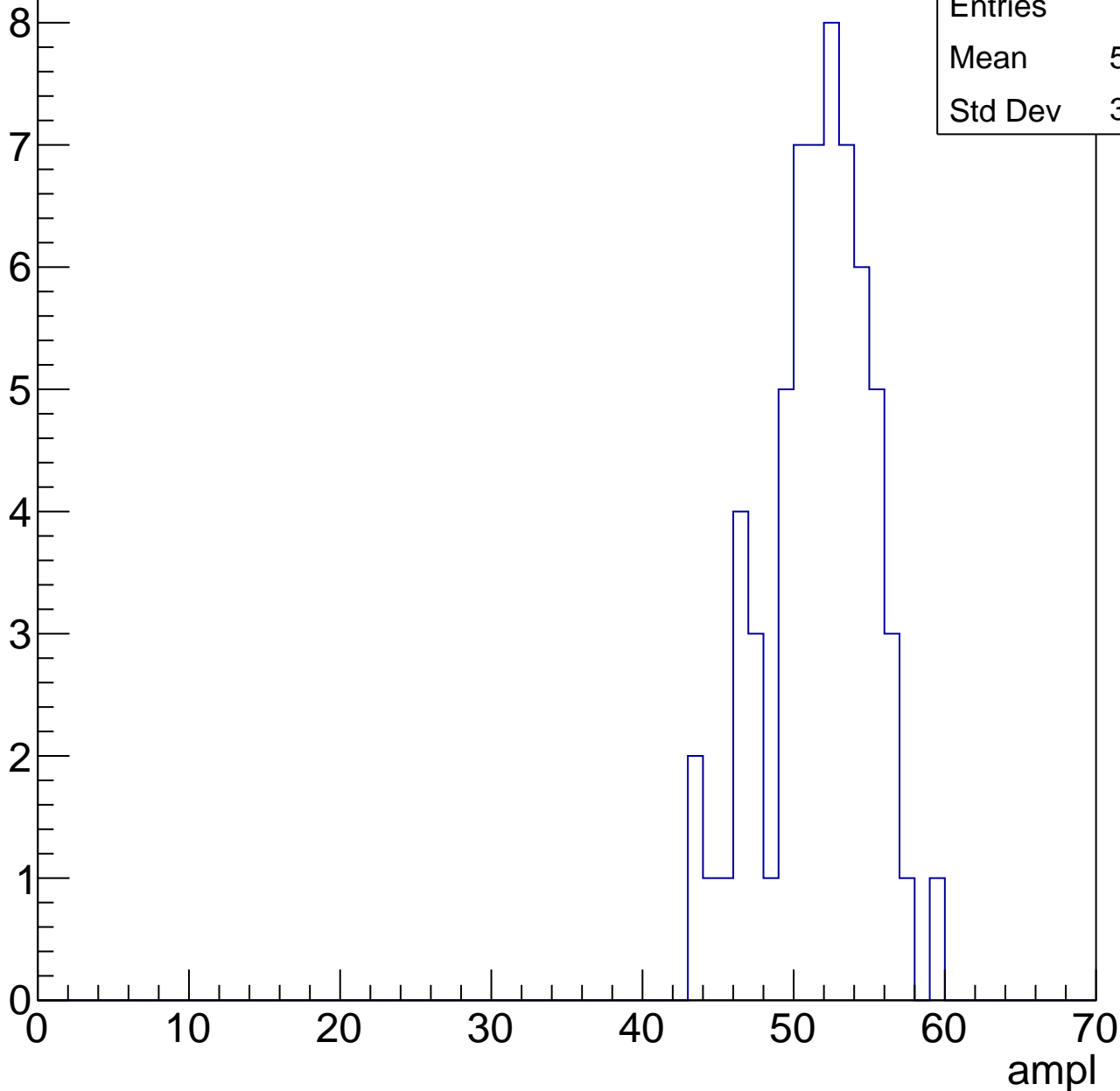


# B1L103S, U16-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	51.13
Std Dev	3.457

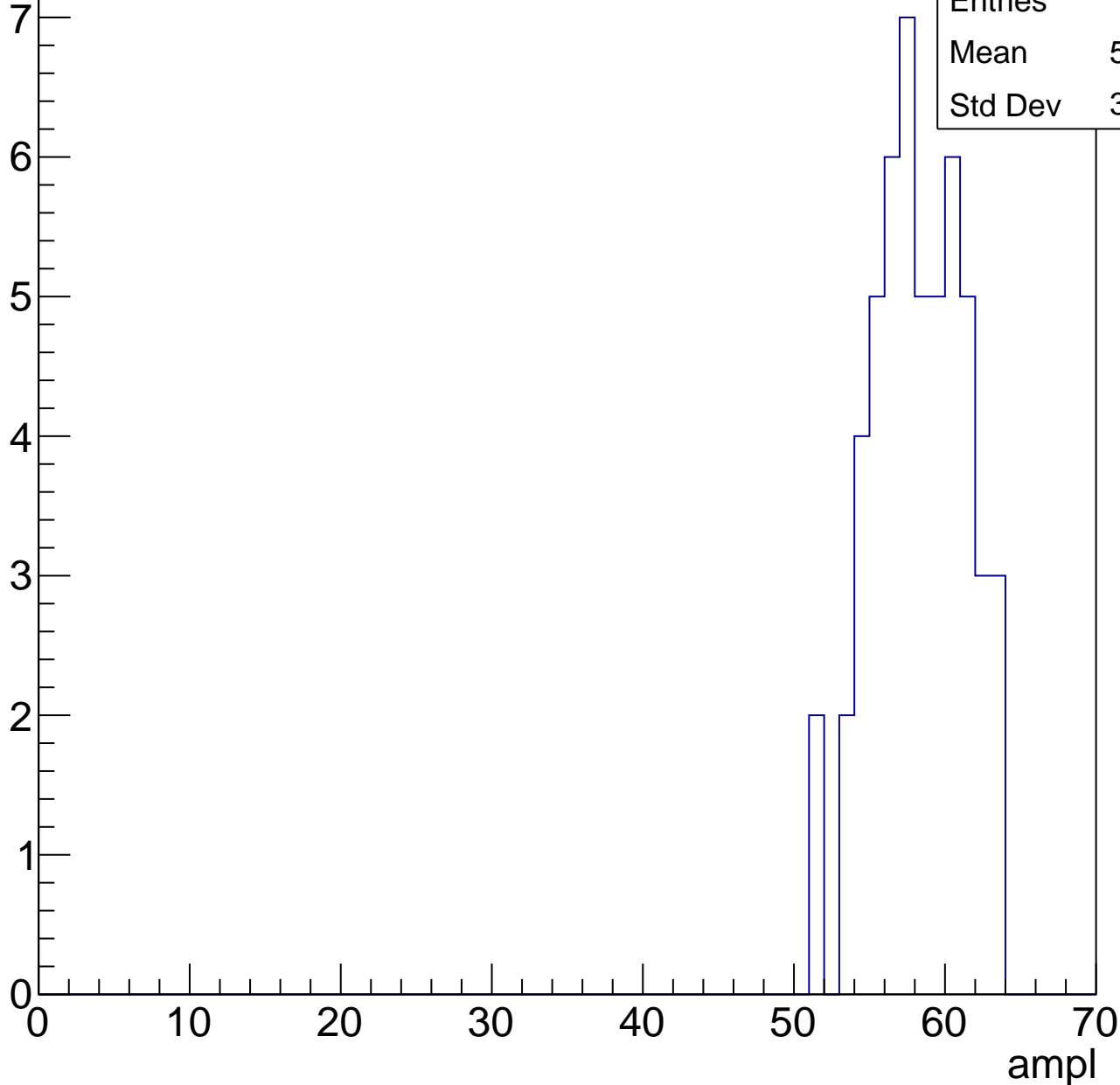


# B1L103S, U16-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	57.72
Std Dev	3.012

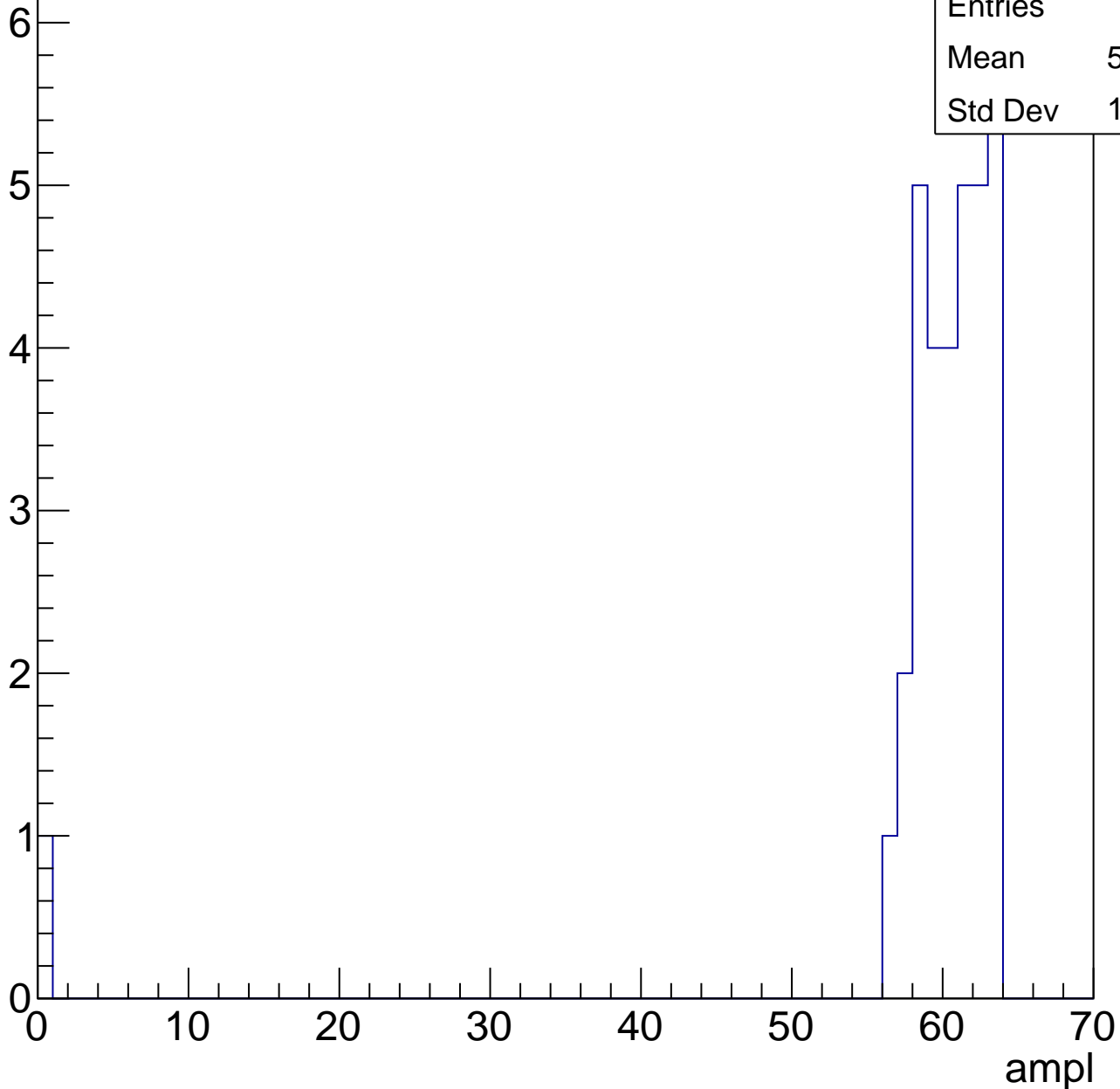


# B1L103S, U16-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	33
Mean	58.45
Std Dev	10.53



# B1L103S, U16-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	62.33
Std Dev	0.4714



# B1L103S, U16-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U16-ch16, adc0

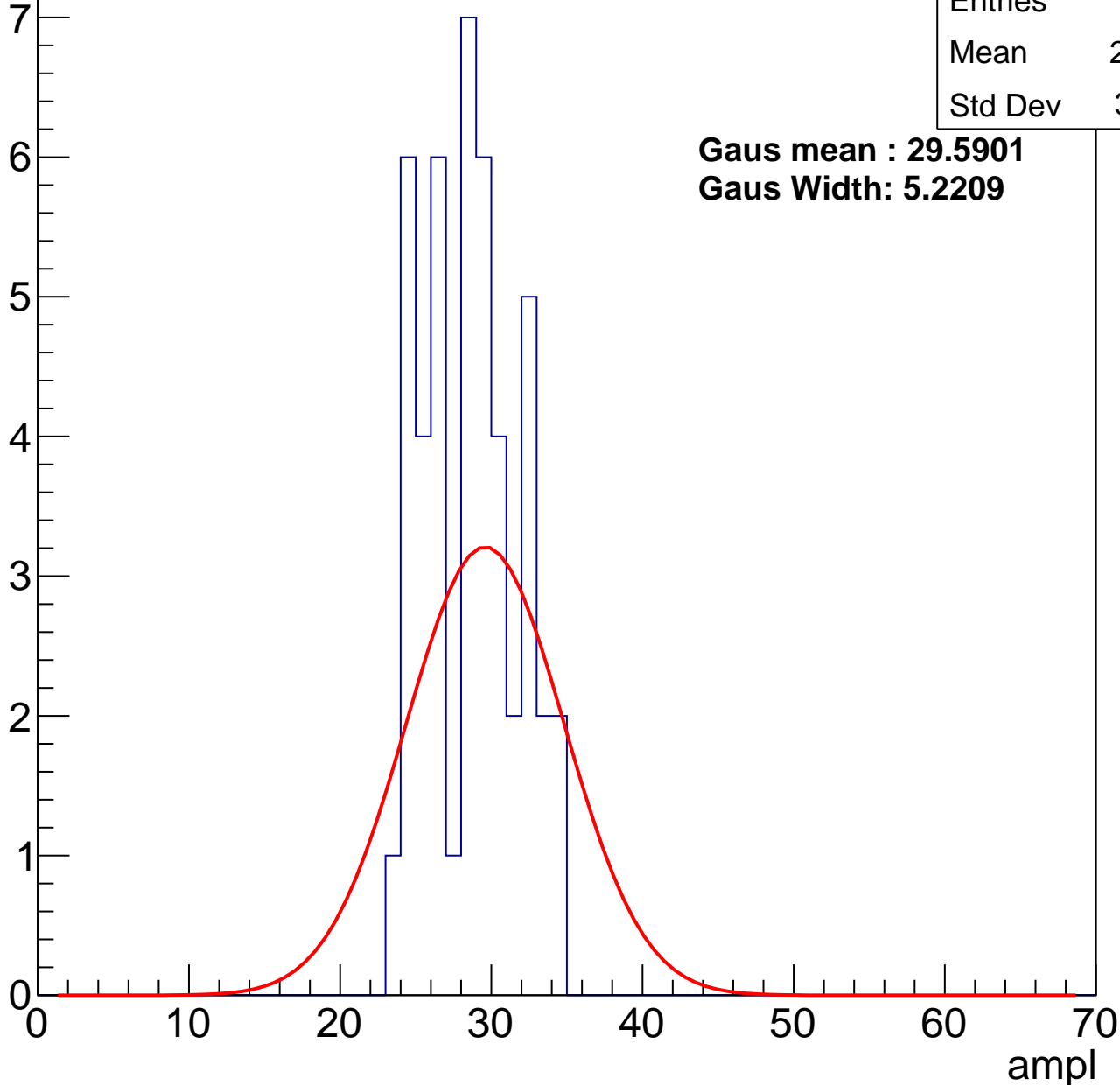
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	28.17
Std Dev	3.031

**Gaus mean : 29.5901**

**Gaus Width: 5.2209**

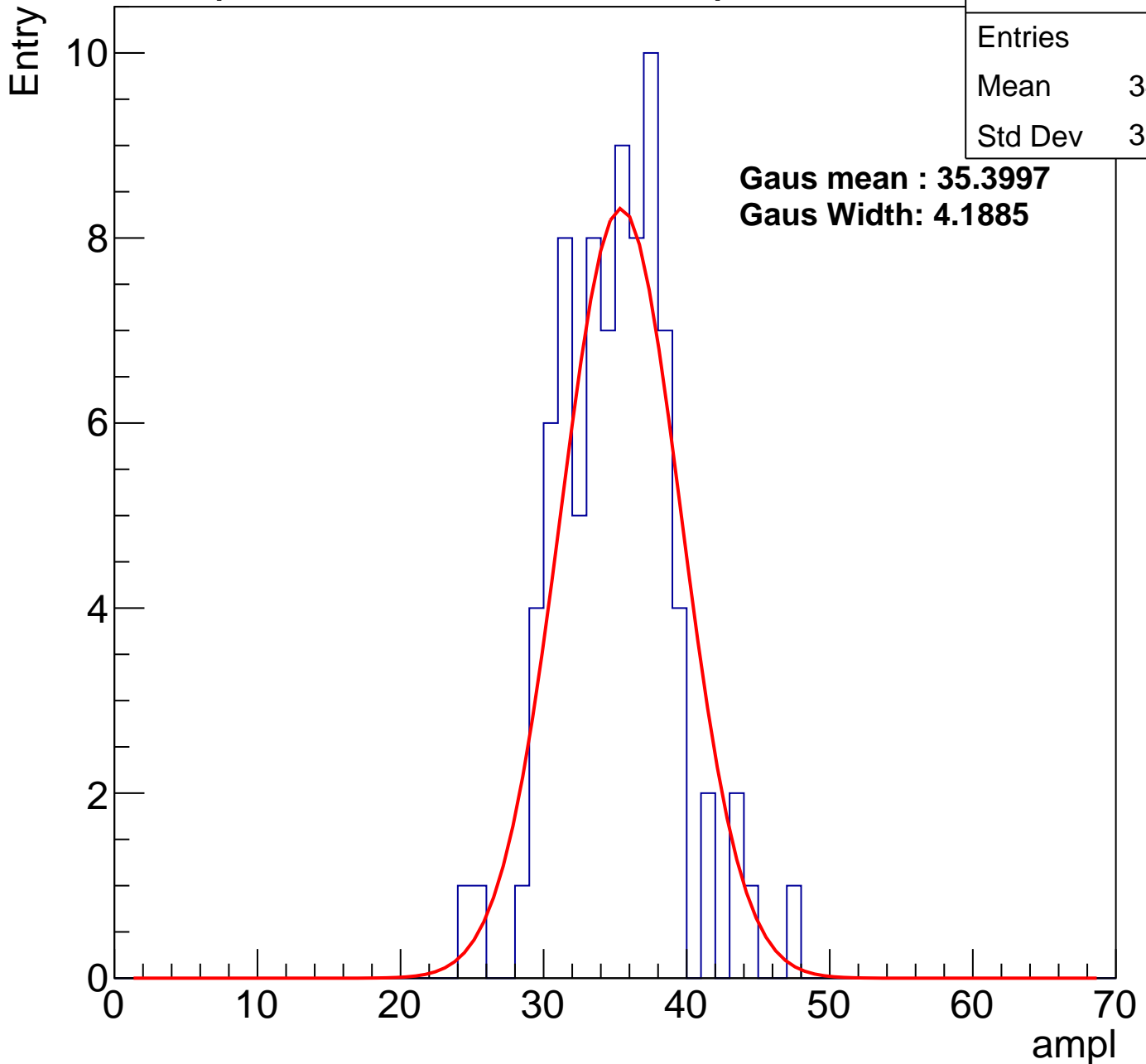


# B1L103S, U16-ch16, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	85
Mean	34.55
Std Dev	3.999

**Gaus mean : 35.3997**  
**Gaus Width: 4.1885**



# B1L103S, U16-ch16, adc2

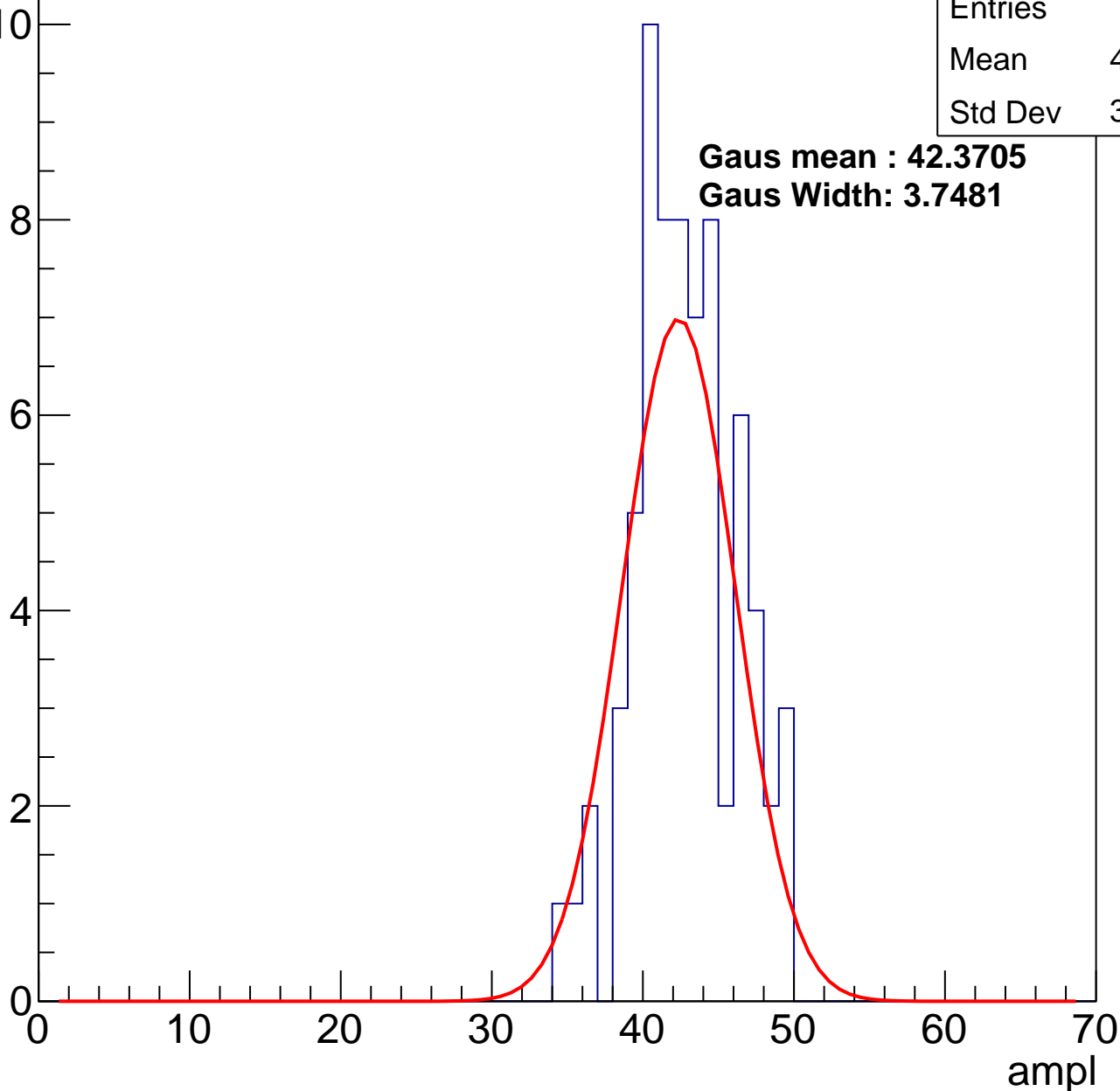
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	42.34
Std Dev	3.359

**Gaus mean : 42.3705**

**Gaus Width: 3.7481**

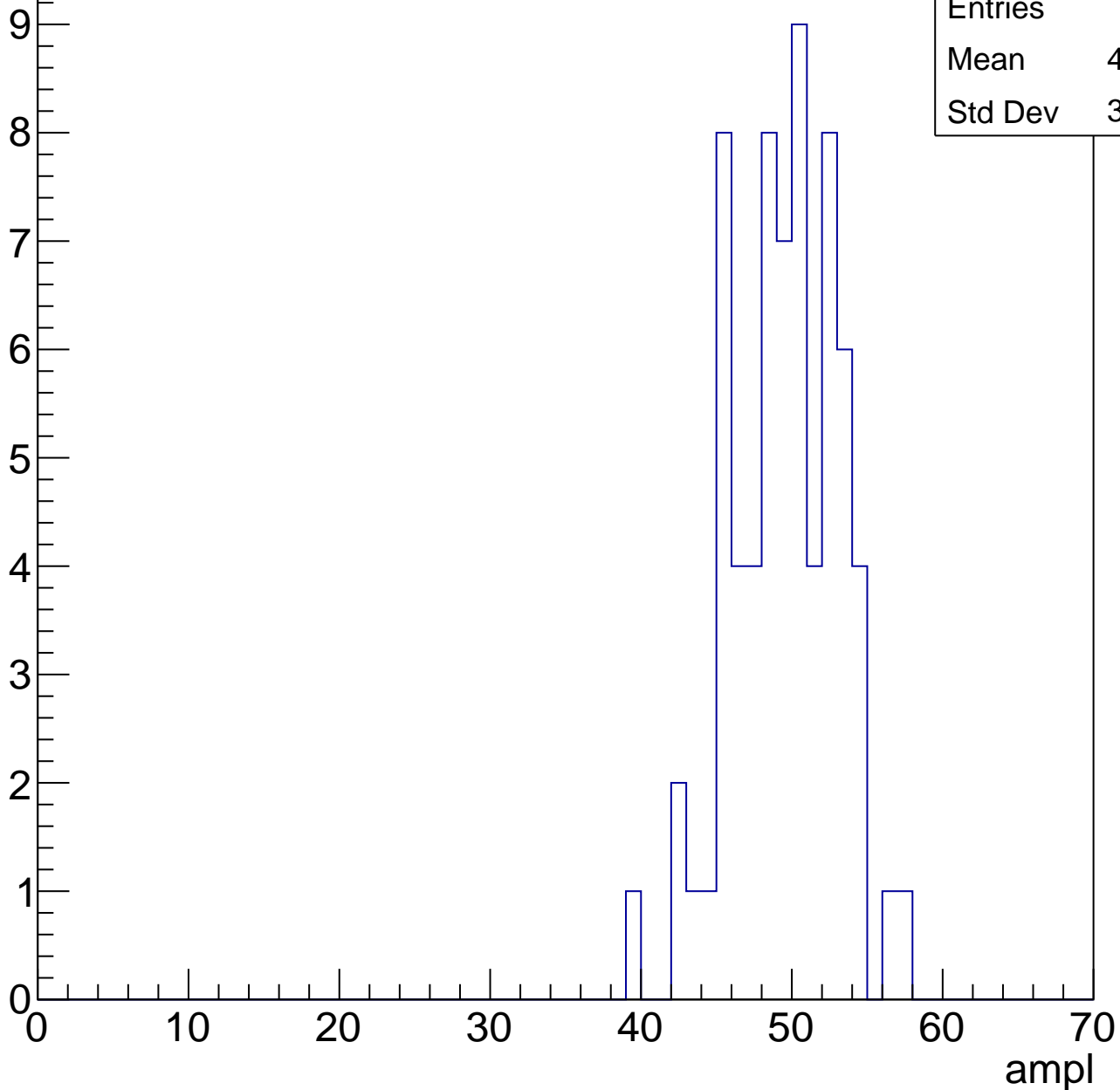


# B1L103S, U16-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	49.07
Std Dev	3.515

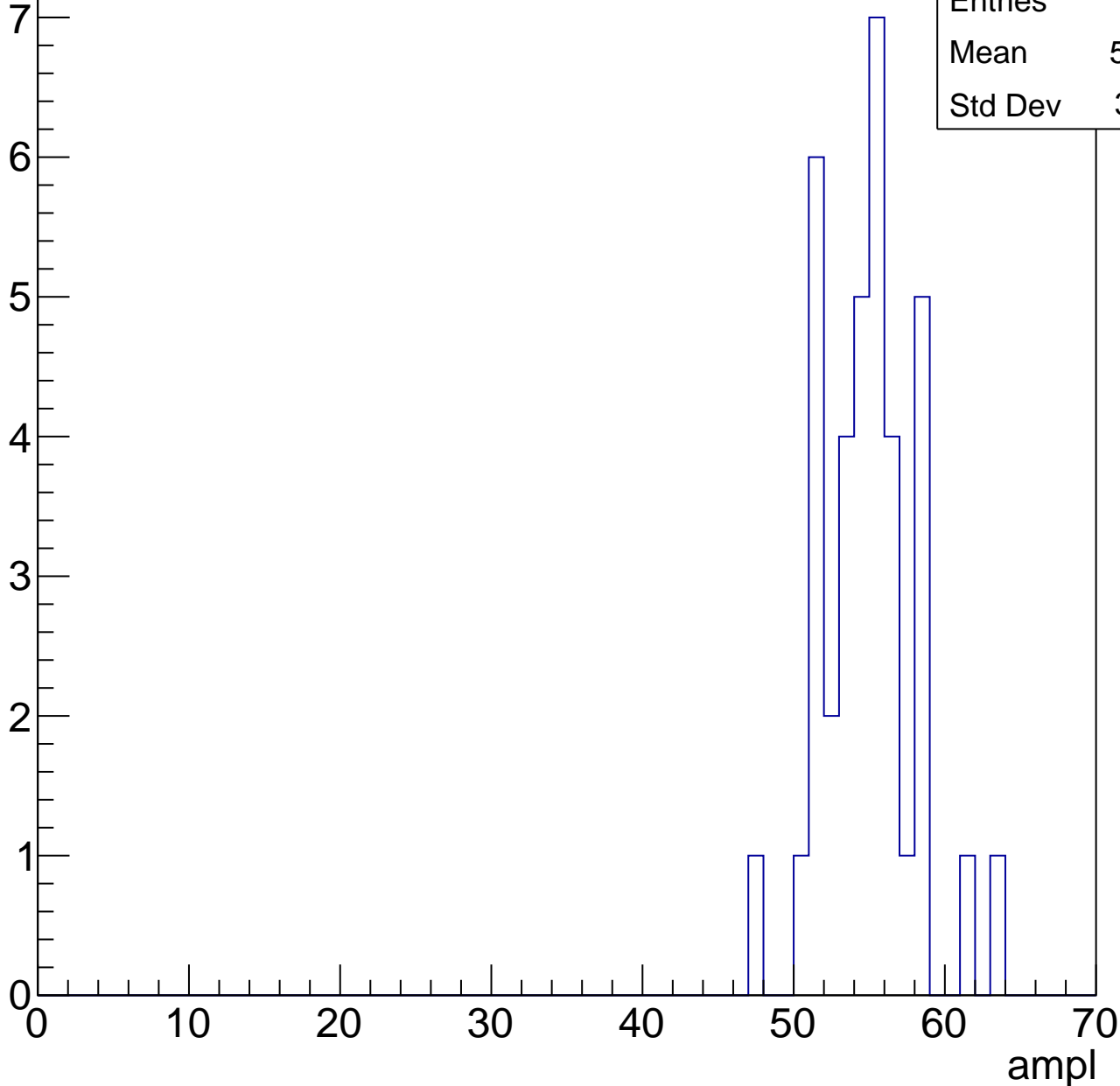


# B1L103S, U16-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	38
Mean	54.45
Std Dev	3.101

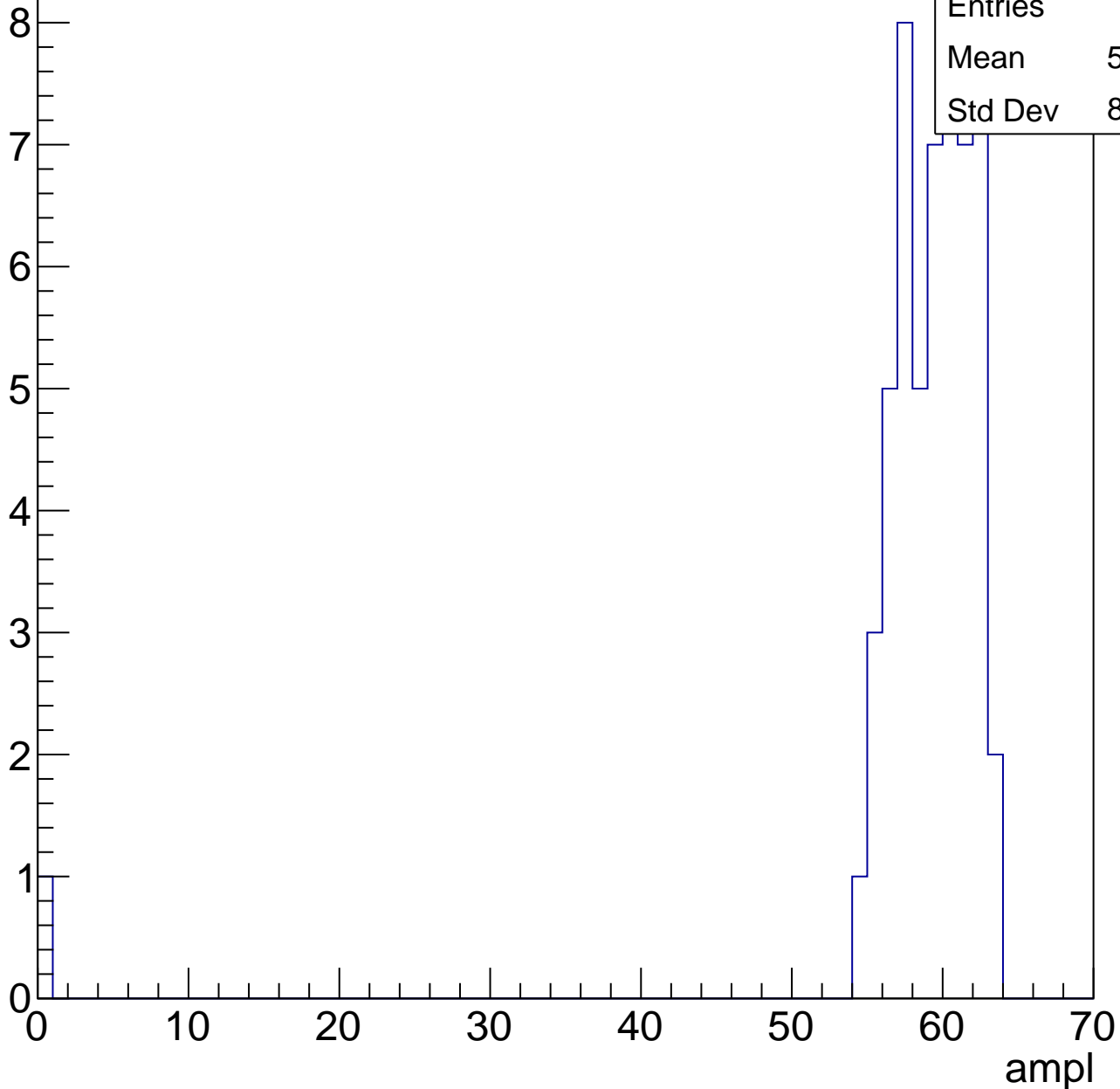


# B1L103S, U16-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	57.95
Std Dev	8.218

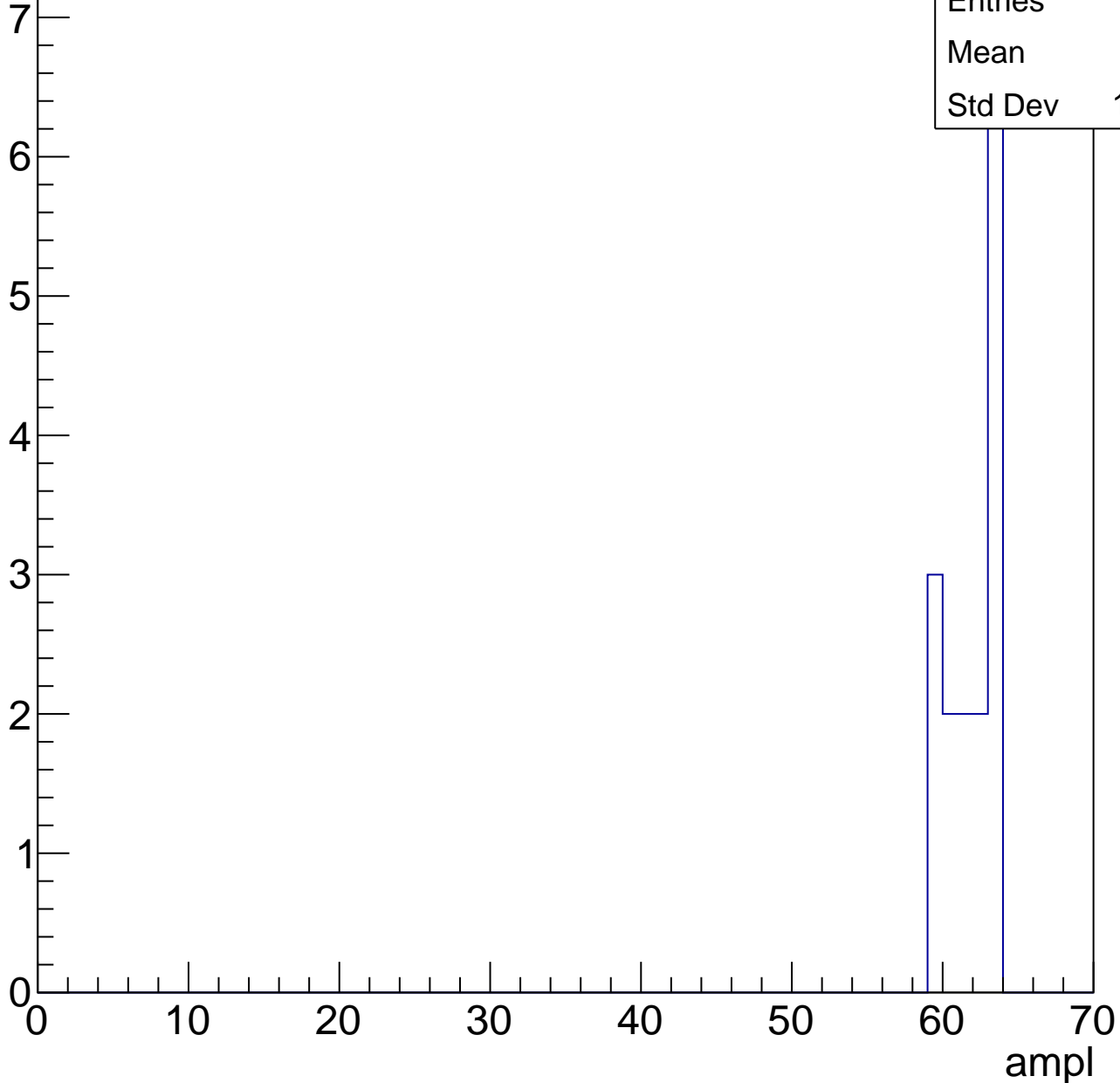


# B1L103S, U16-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	16
Mean	61.5
Std Dev	1.581





# B1L103S, U16-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch17, adc0

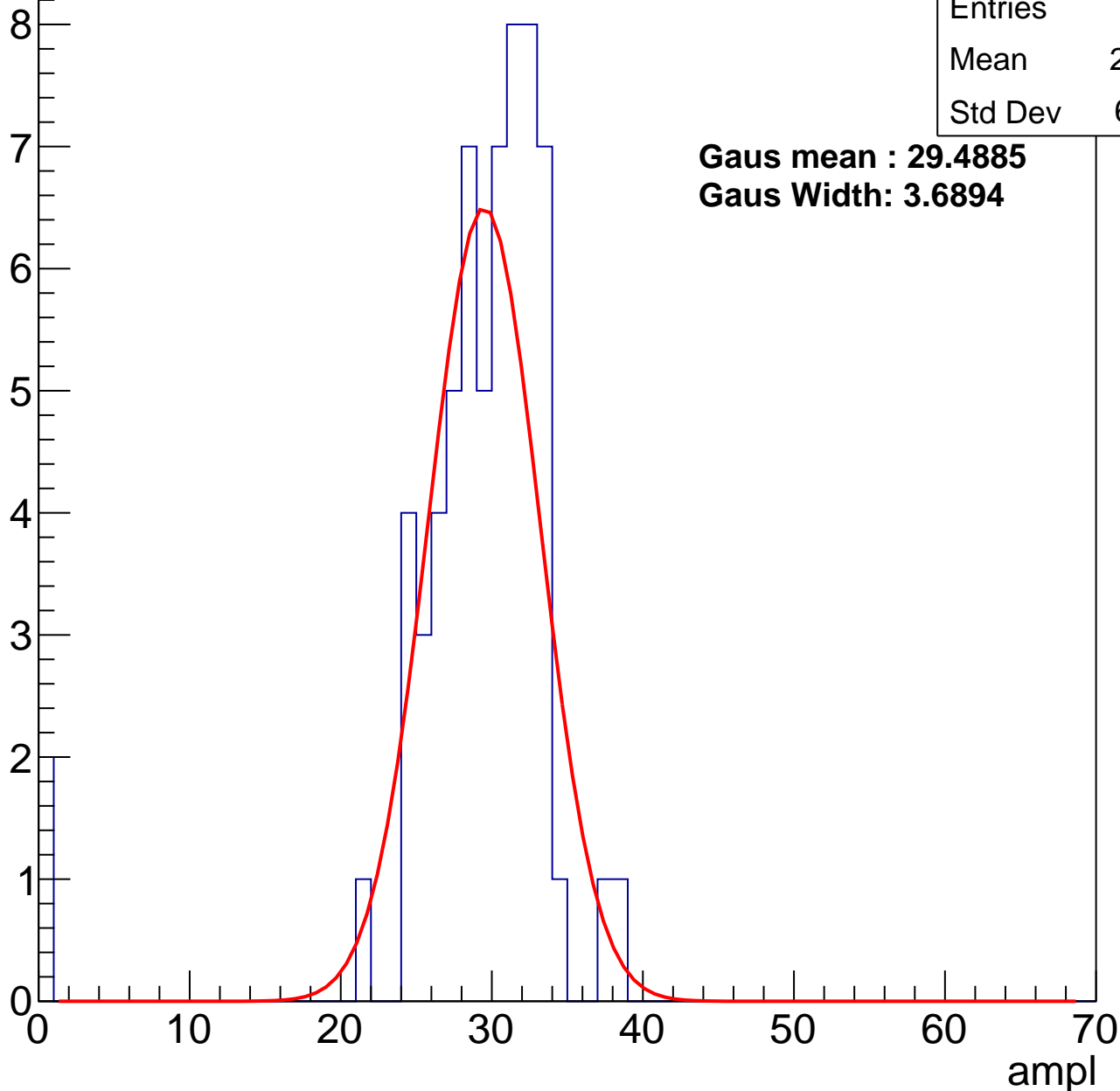
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	28.53
Std Dev	6.041

**Gaus mean : 29.4885**

**Gaus Width: 3.6894**



# B1L103S, U16-ch17, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	77
Mean	36.47
Std Dev	3.723

**Gaus mean : 37.0333**

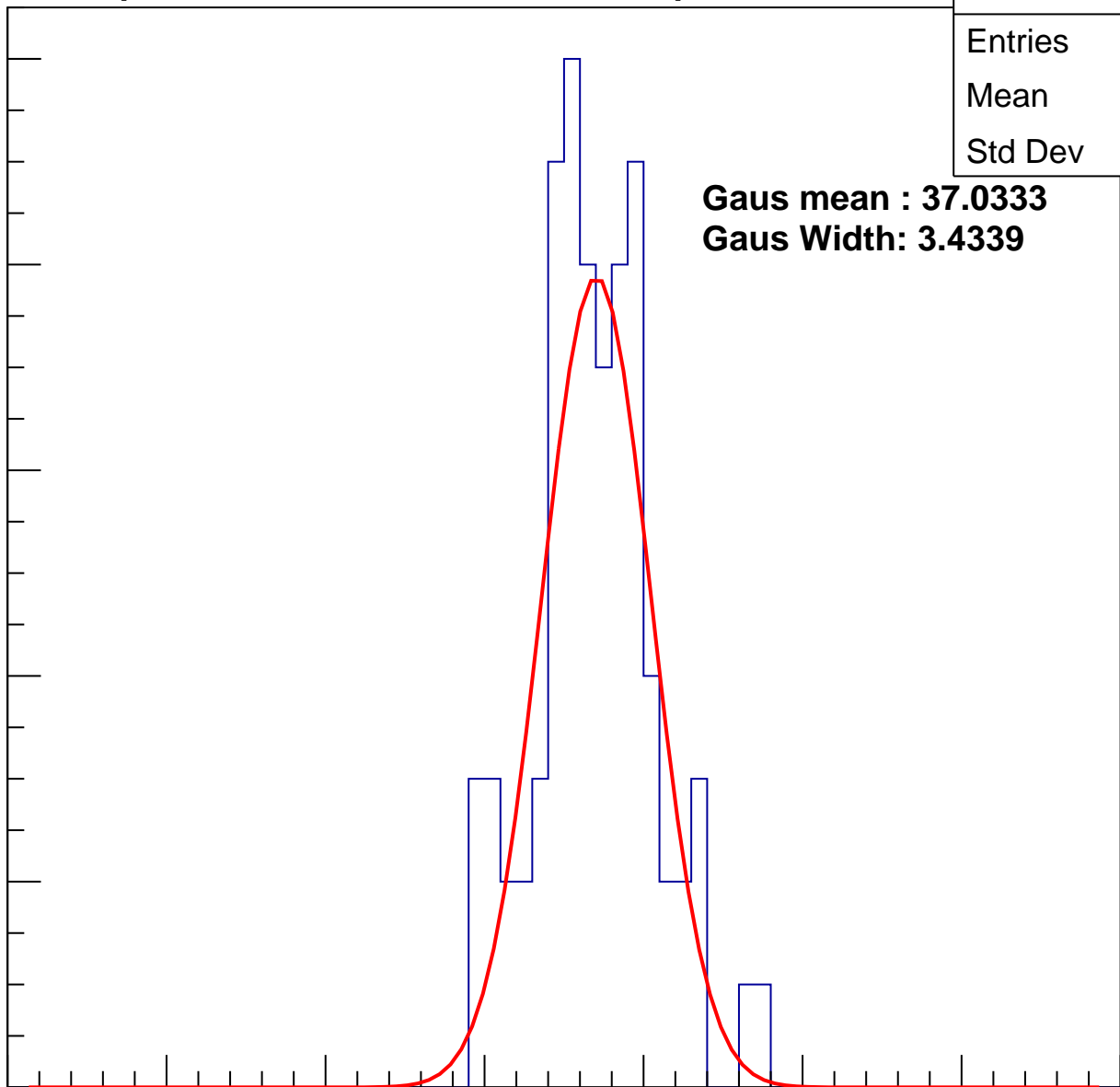
**Gaus Width: 3.4339**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U16-ch17, adc2

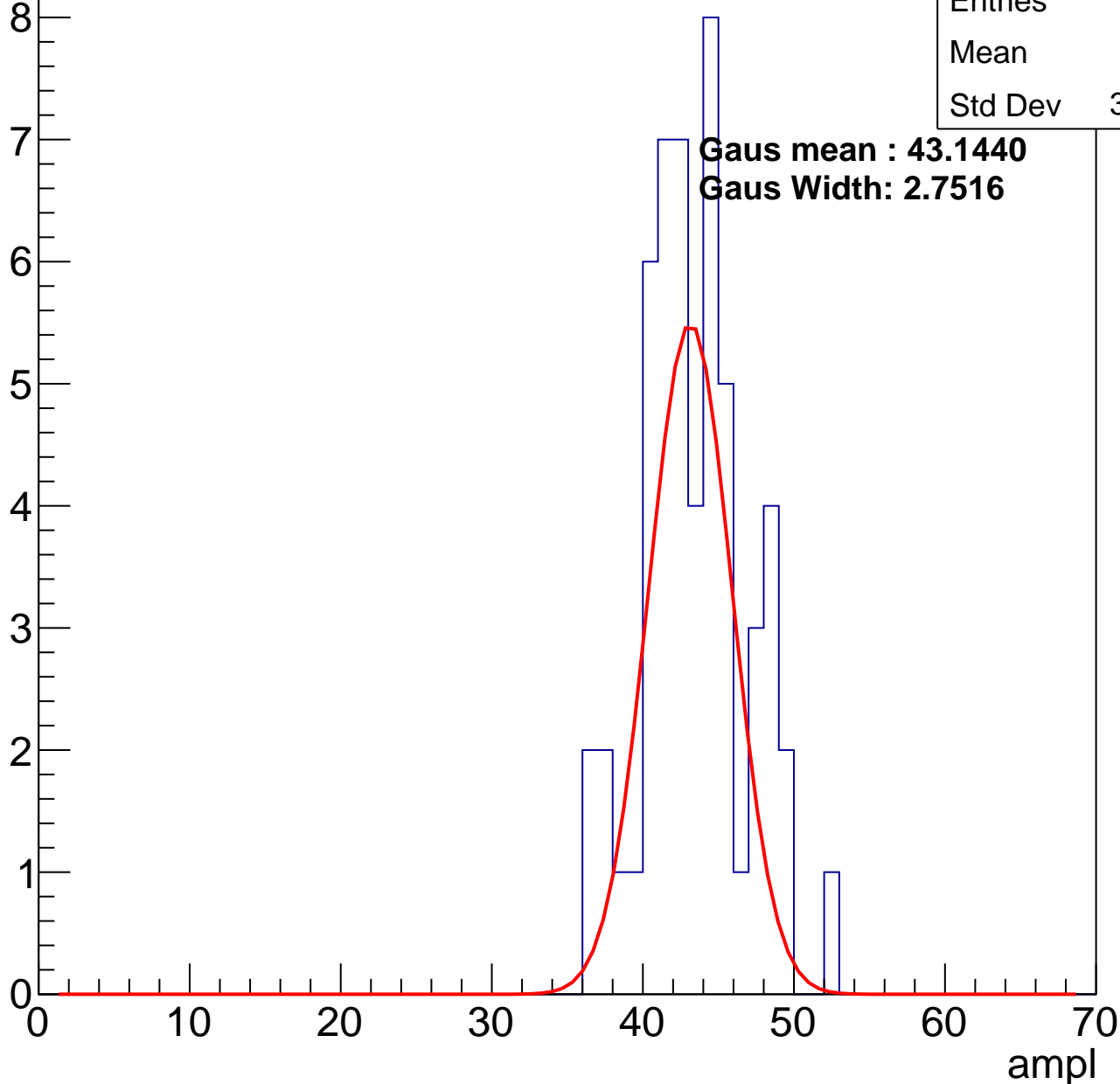
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	43
Std Dev	3.437

**Gaus mean : 43.1440**

**Gaus Width: 2.7516**

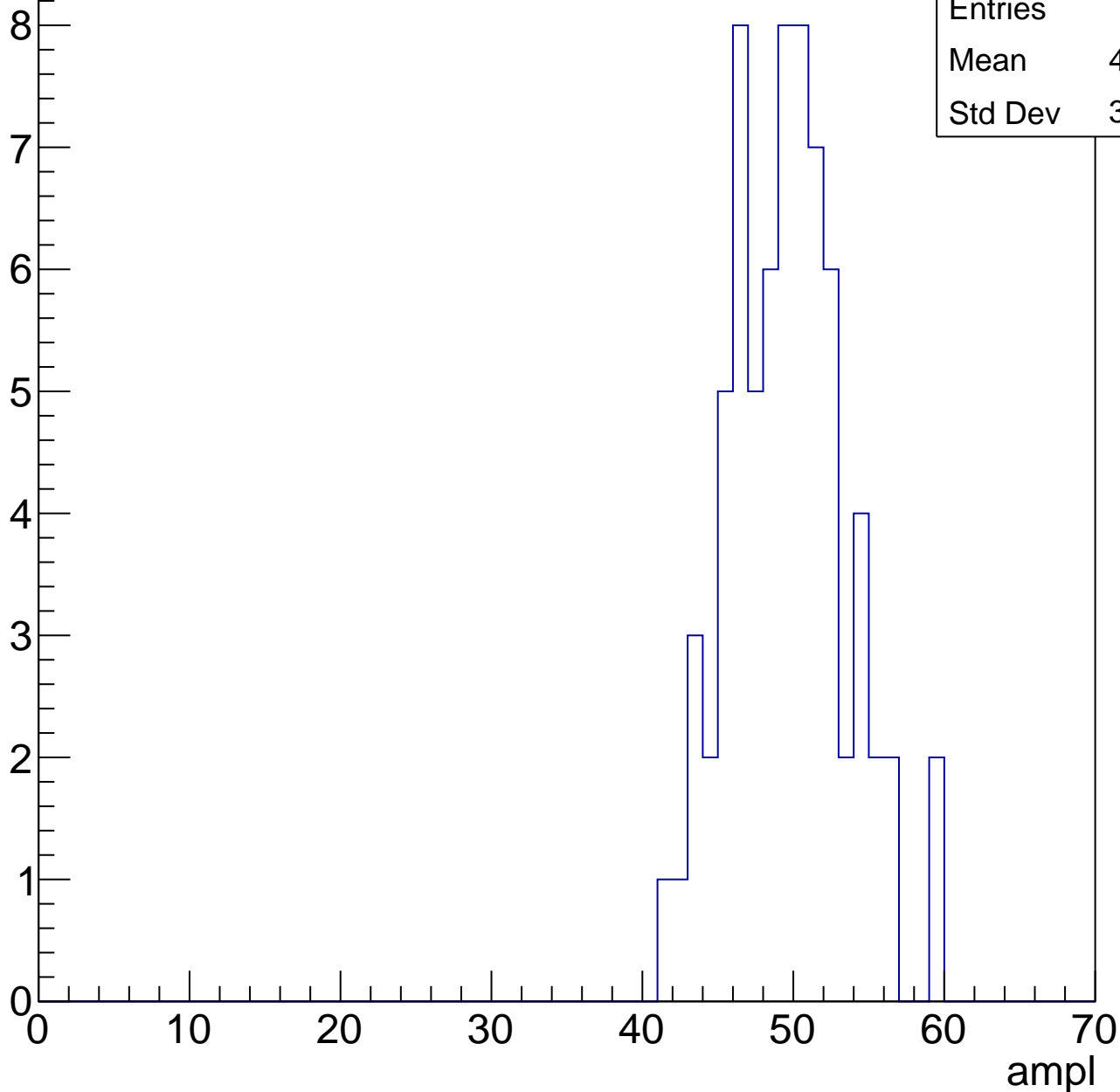


# B1L103S, U16-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

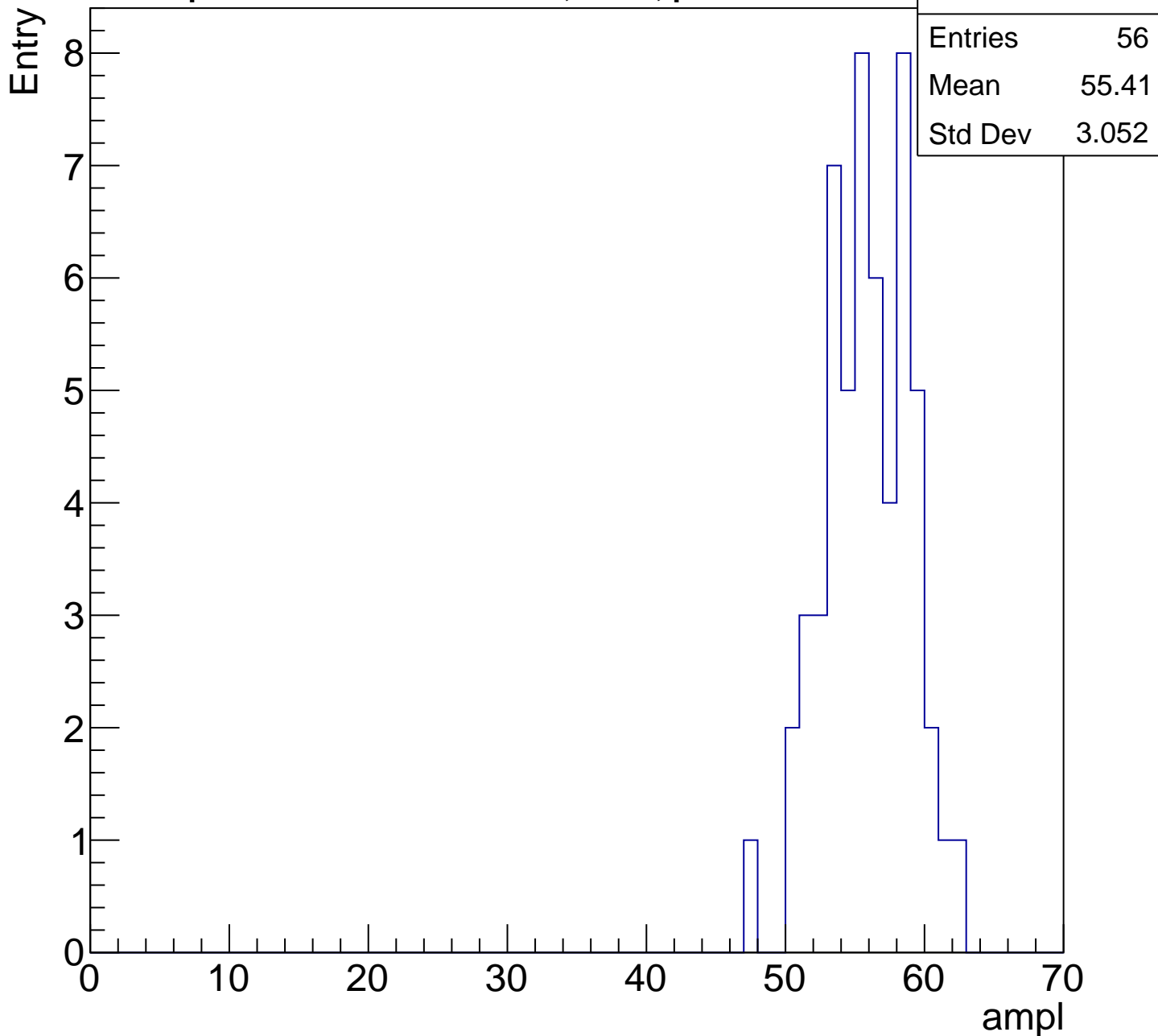
Entry

Entries	72
Mean	49.15
Std Dev	3.799



# B1L103S, U16-ch17, adc4

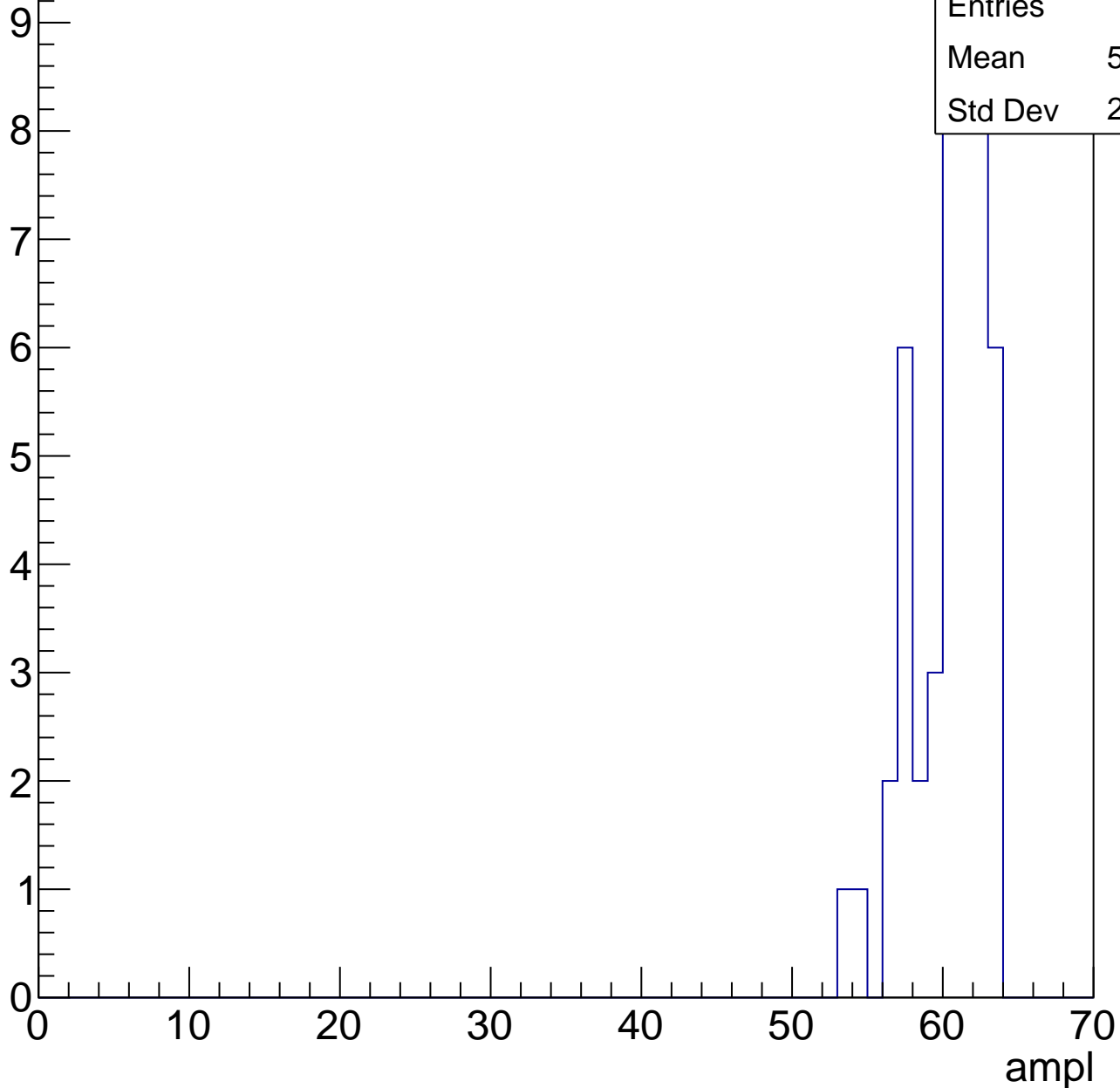
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U16-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

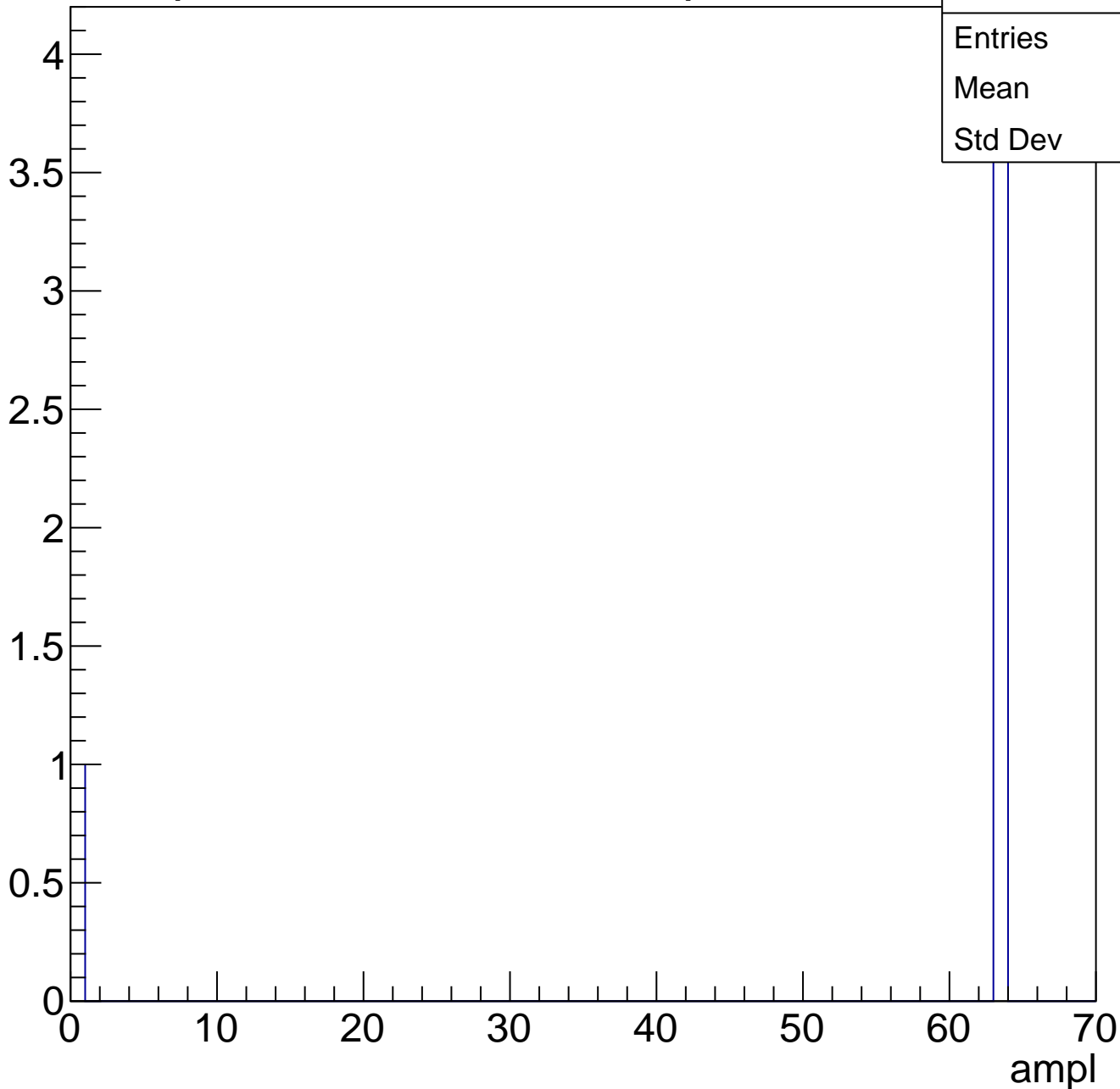


Entries	47
Mean	59.98
Std Dev	2.445

# B1L103S, U16-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch18, adc0

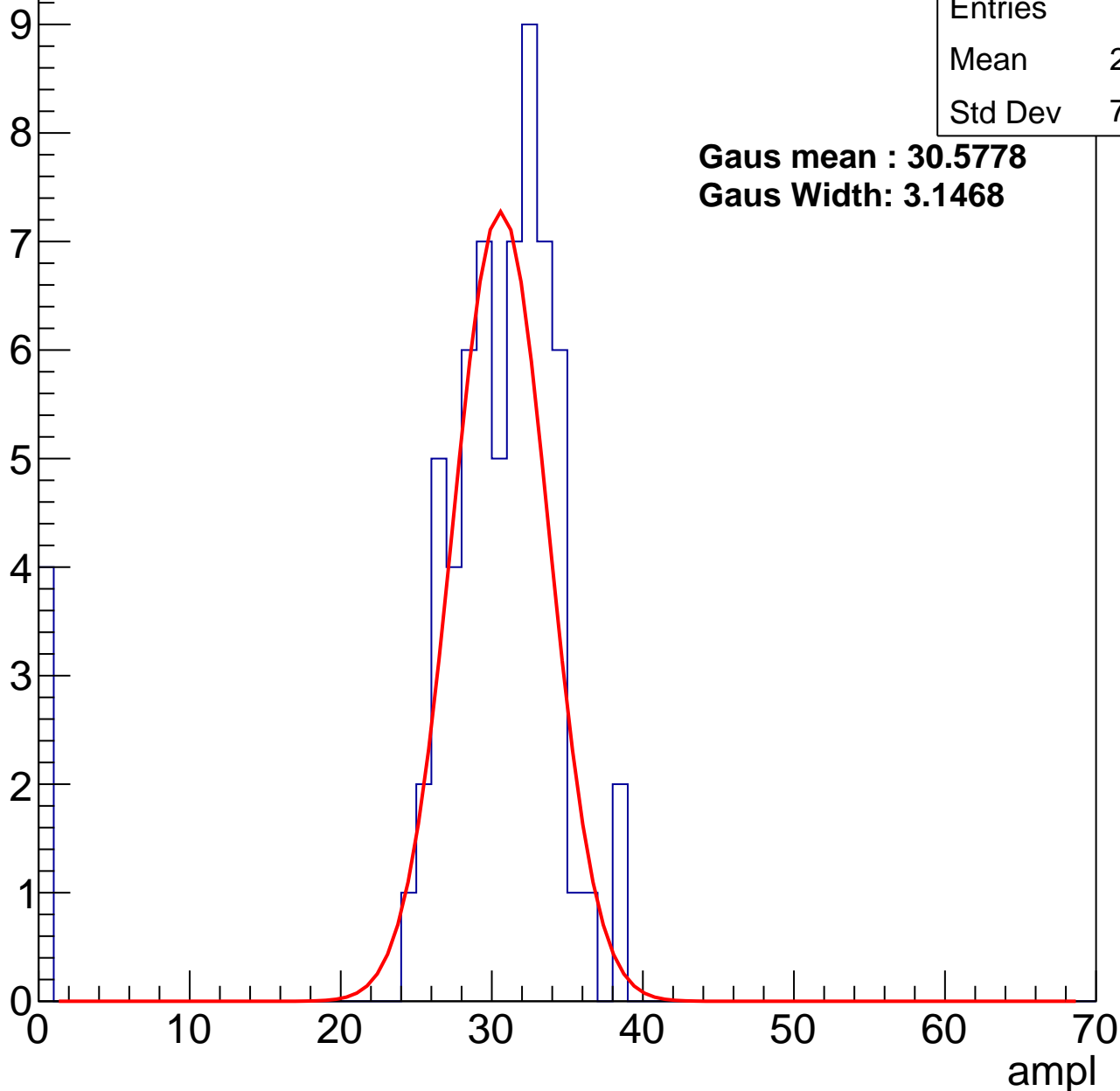
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	28.66
Std Dev	7.826

**Gaus mean : 30.5778**

**Gaus Width: 3.1468**



# B1L103S, U16-ch18, adc1

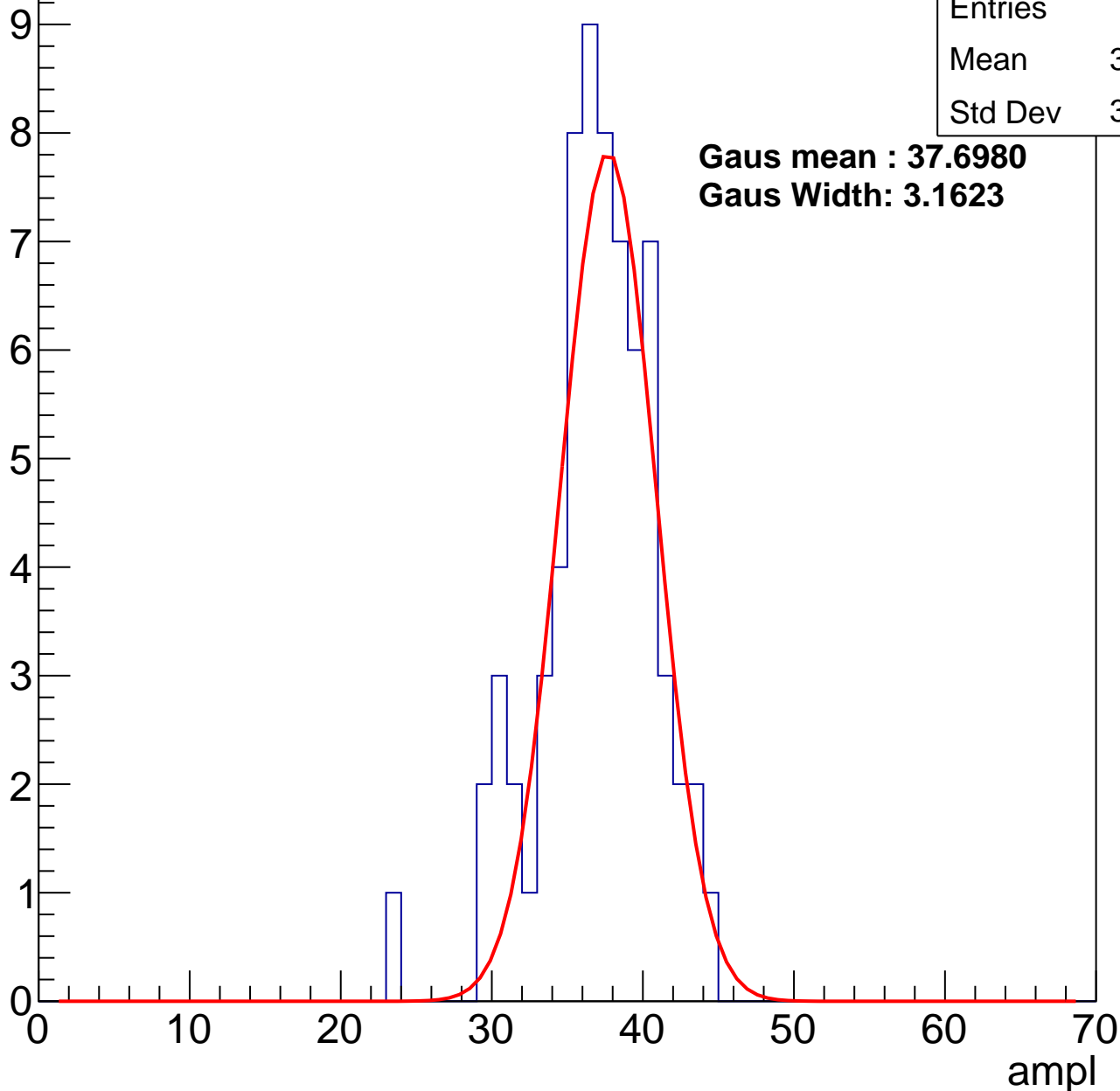
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	36.48
Std Dev	3.783

**Gaus mean : 37.6980**

**Gaus Width: 3.1623**



# B1L103S, U16-ch18, adc2

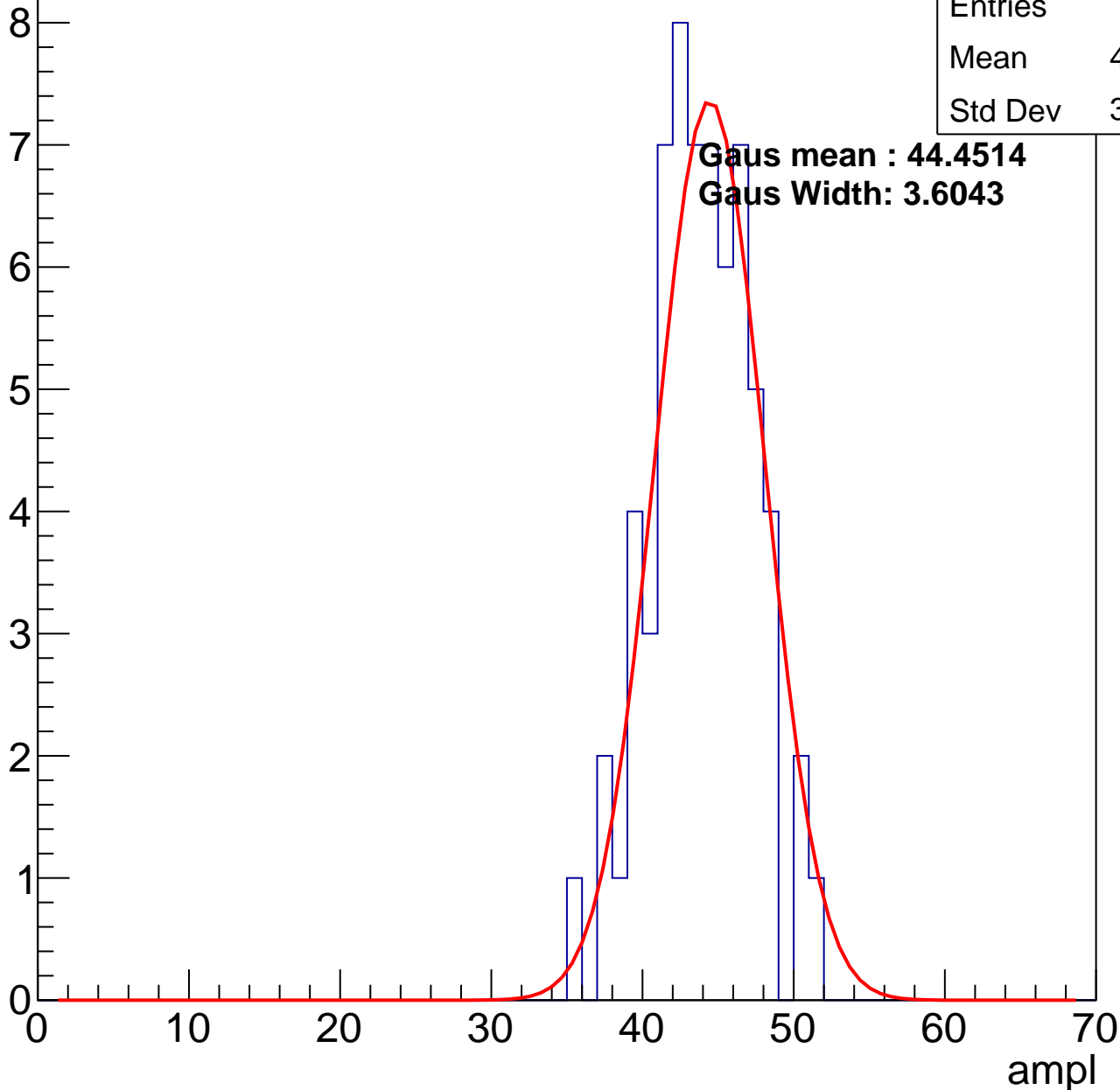
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	43.46
Std Dev	3.305

**Gaus mean : 44.4514**

**Gaus Width: 3.6043**



# B1L103S, U16-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

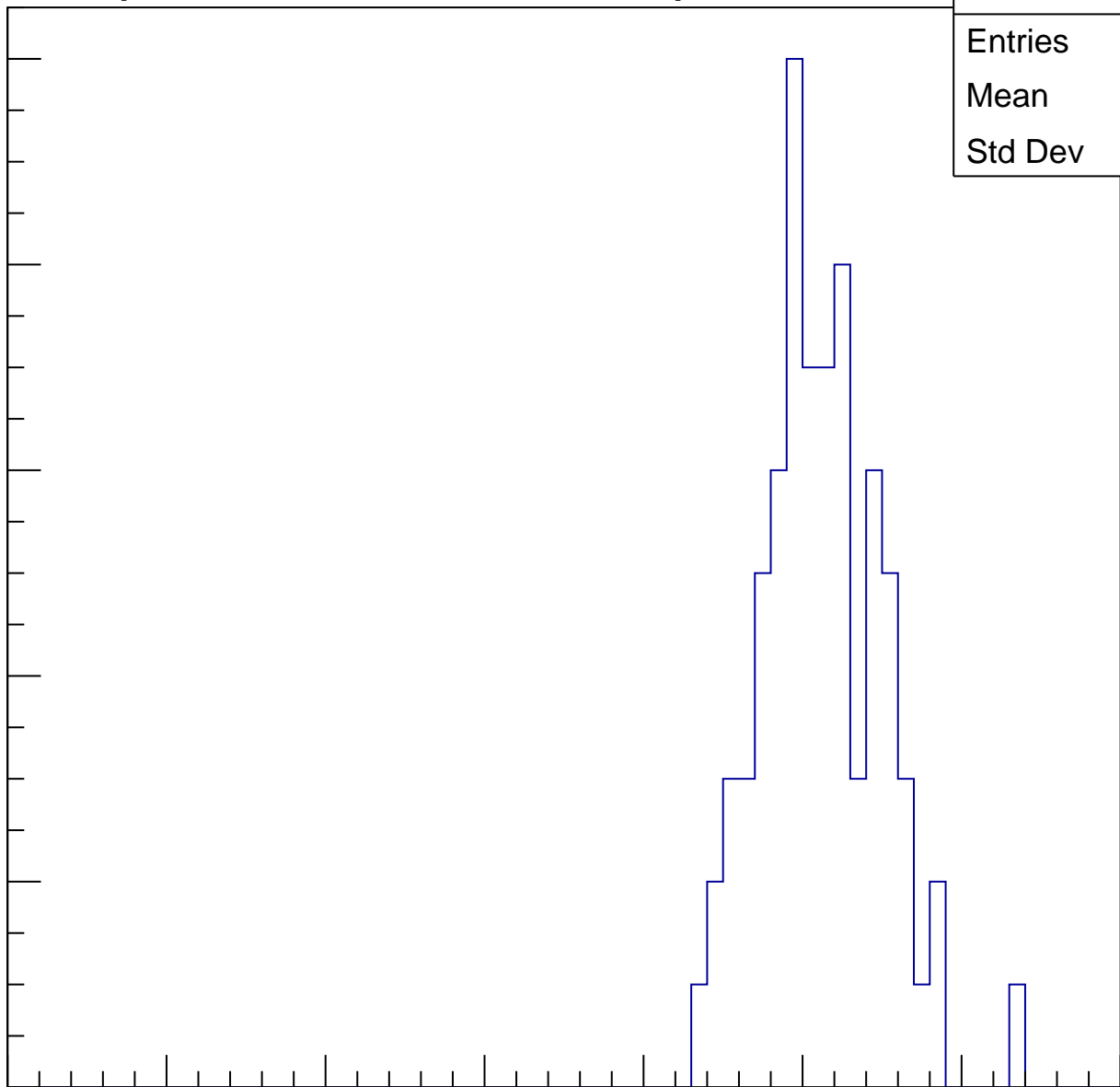
Entries	73
Mean	50.71
Std Dev	3.751

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

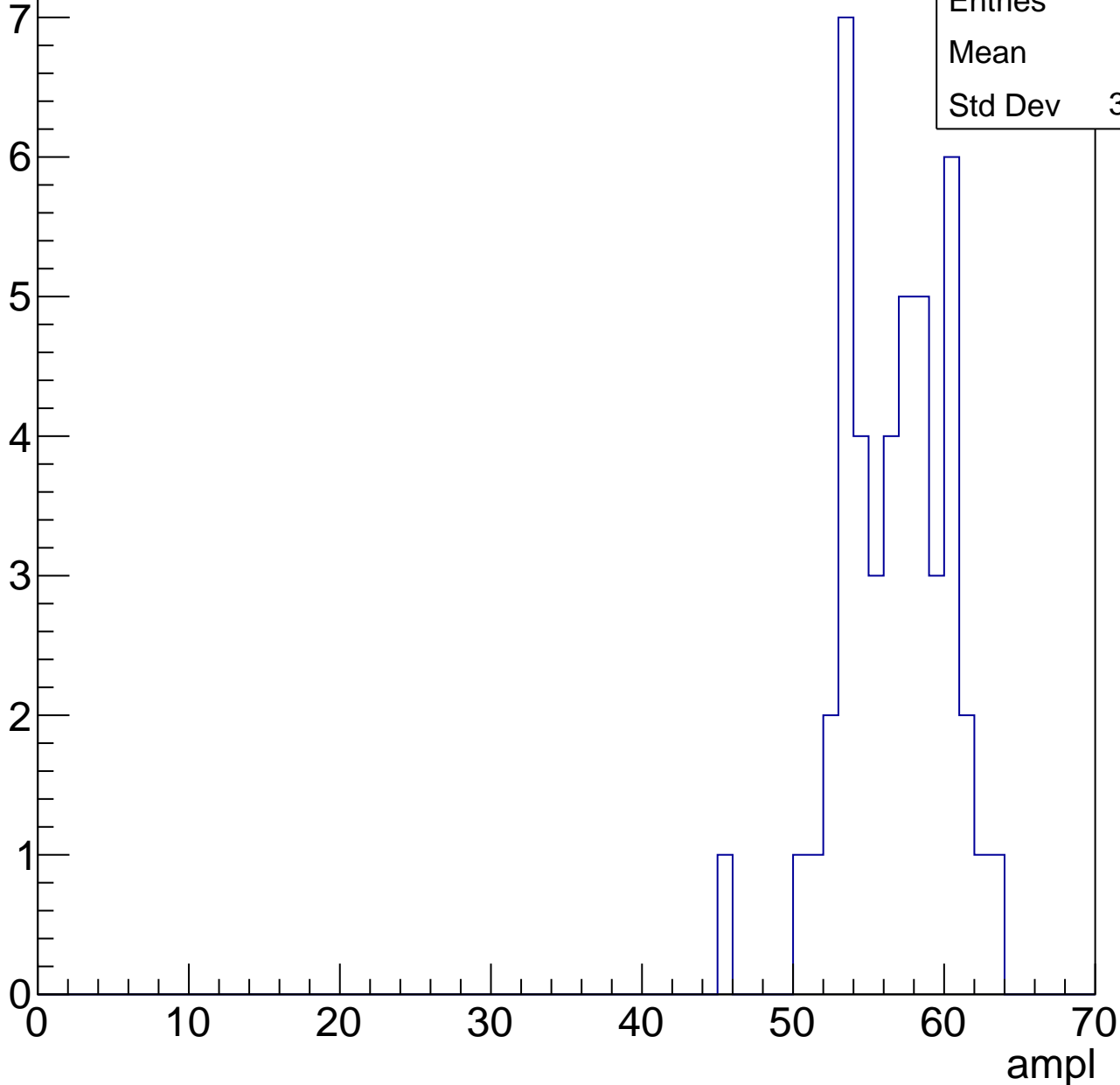


# B1L103S, U16-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	56.2
Std Dev	3.542

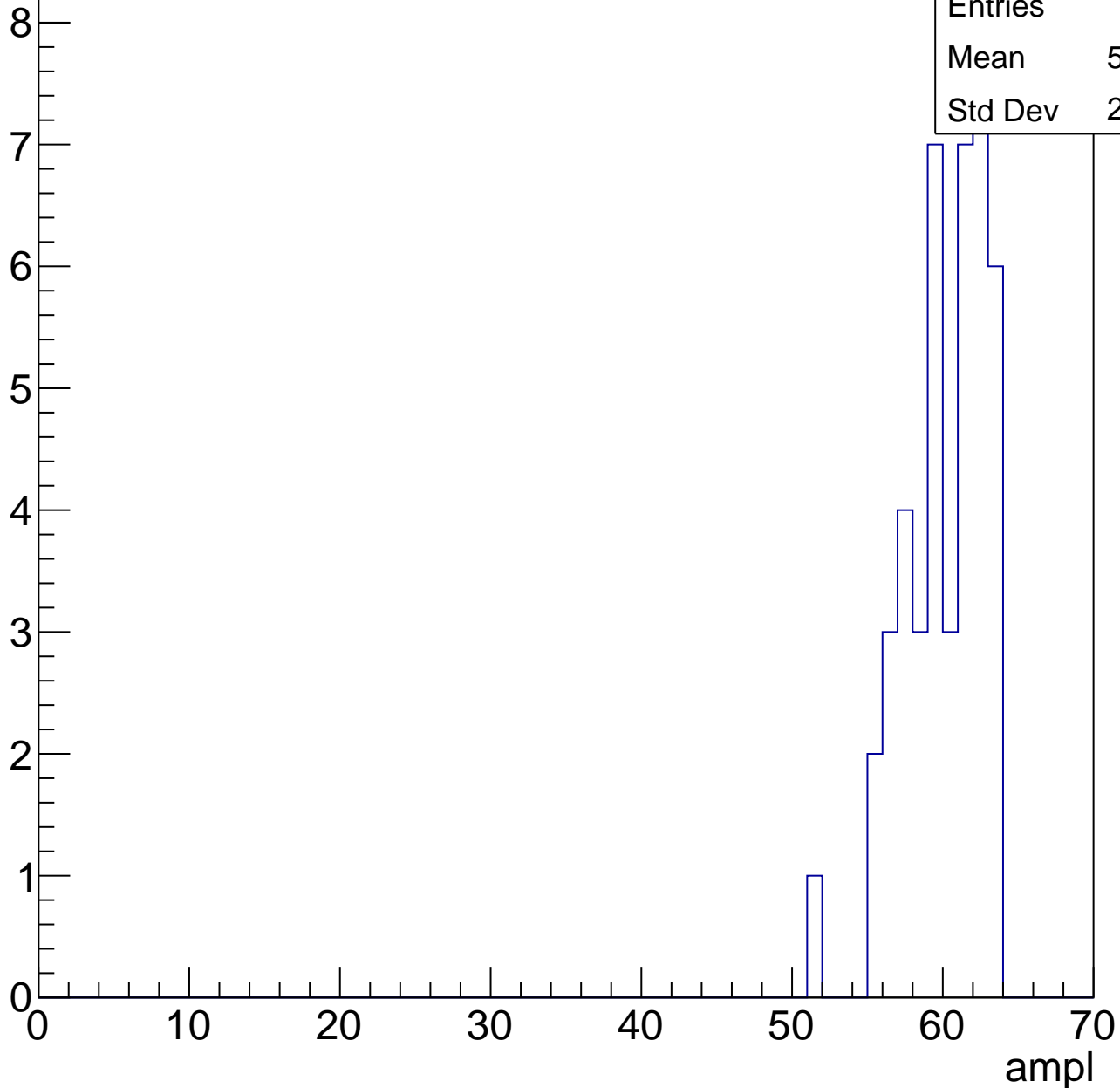


# B1L103S, U16-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

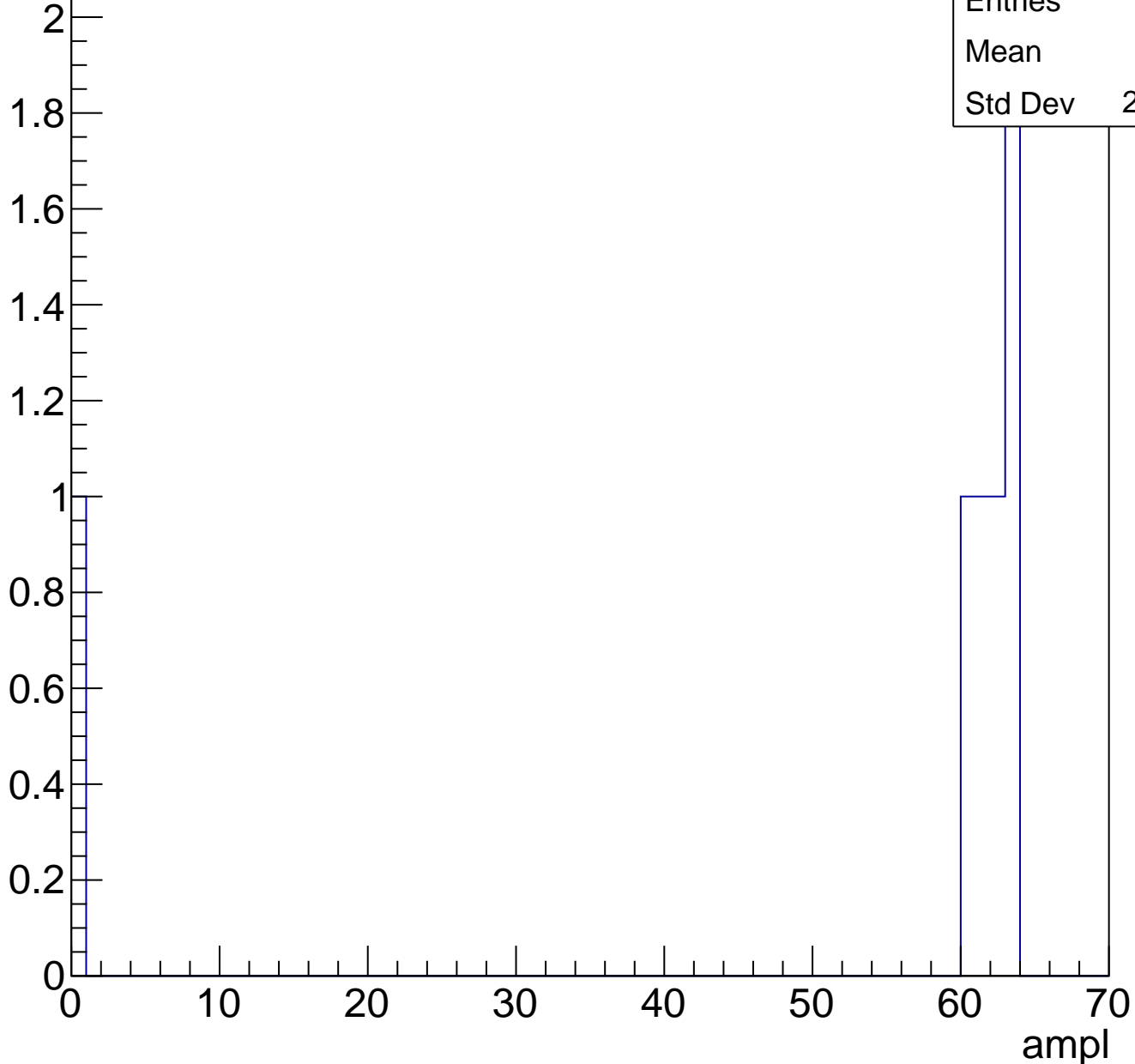
Entries	44
Mean	59.66
Std Dev	2.705



# B1L103S, U16-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U16-ch19, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	78
Mean	29.77
Std Dev	3.826

**Gaus mean : 30.1132**

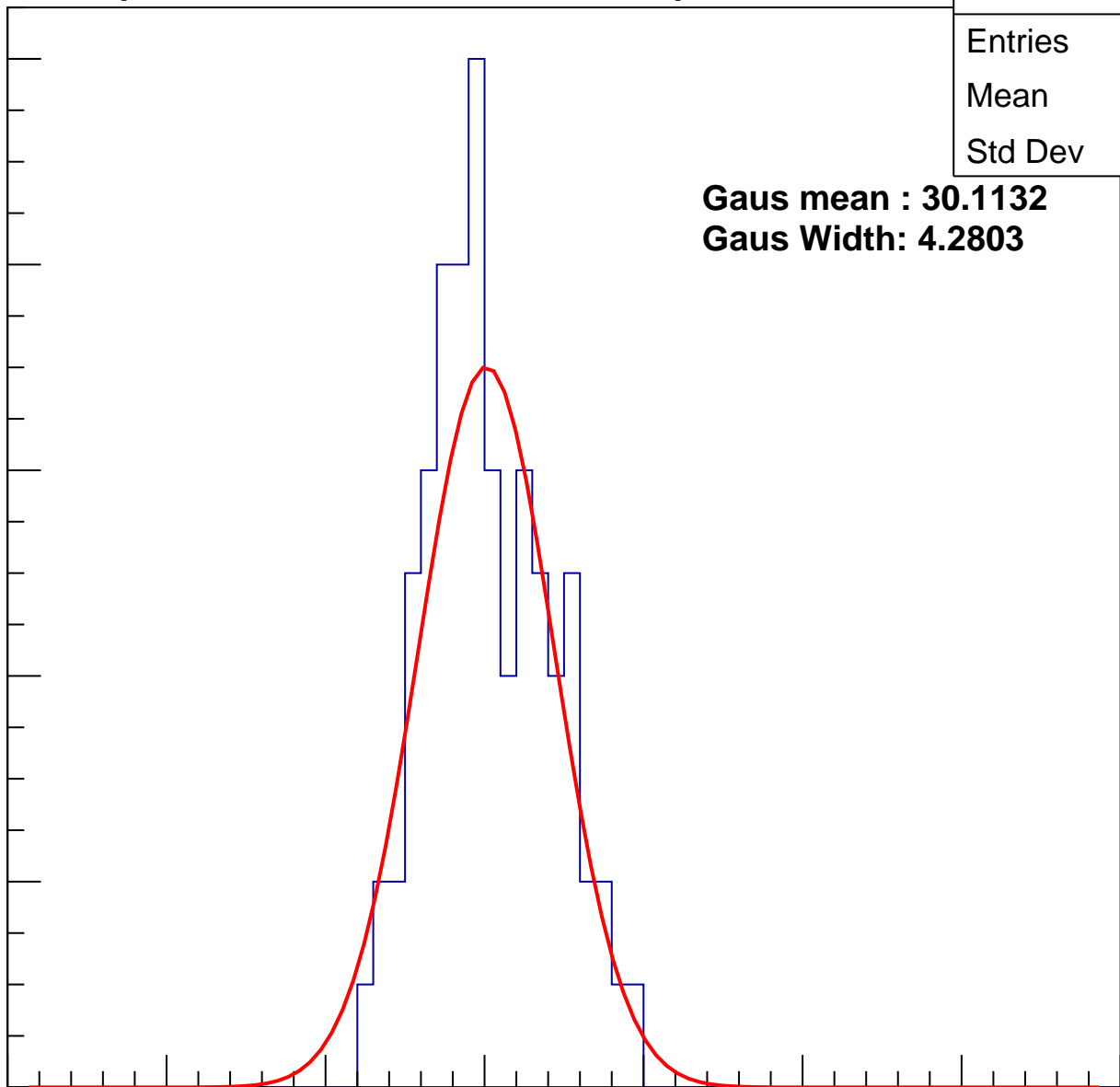
**Gaus Width: 4.2803**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U16-ch19, adc1

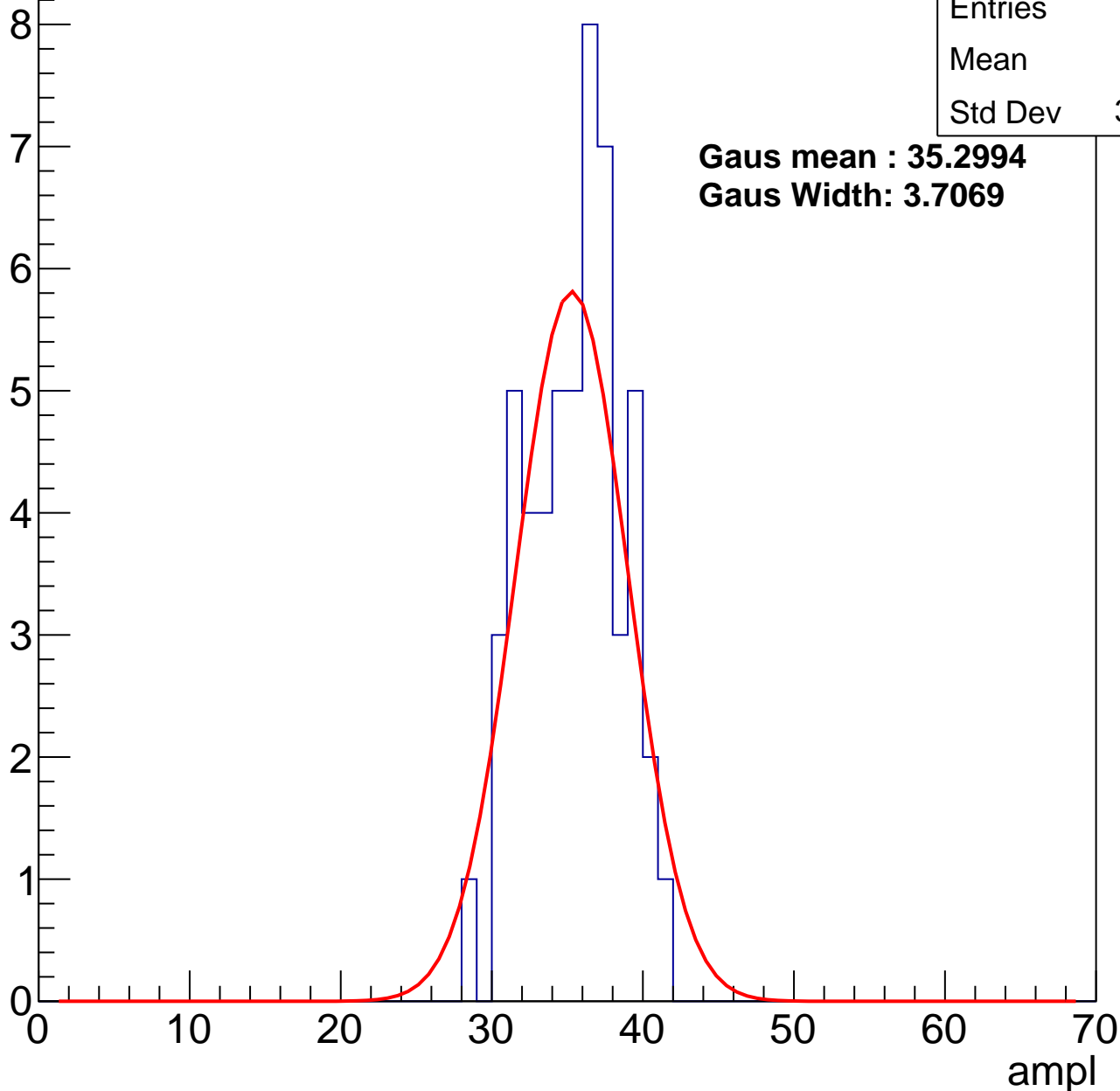
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	35
Std Dev	3.041

**Gaus mean : 35.2994**

**Gaus Width: 3.7069**



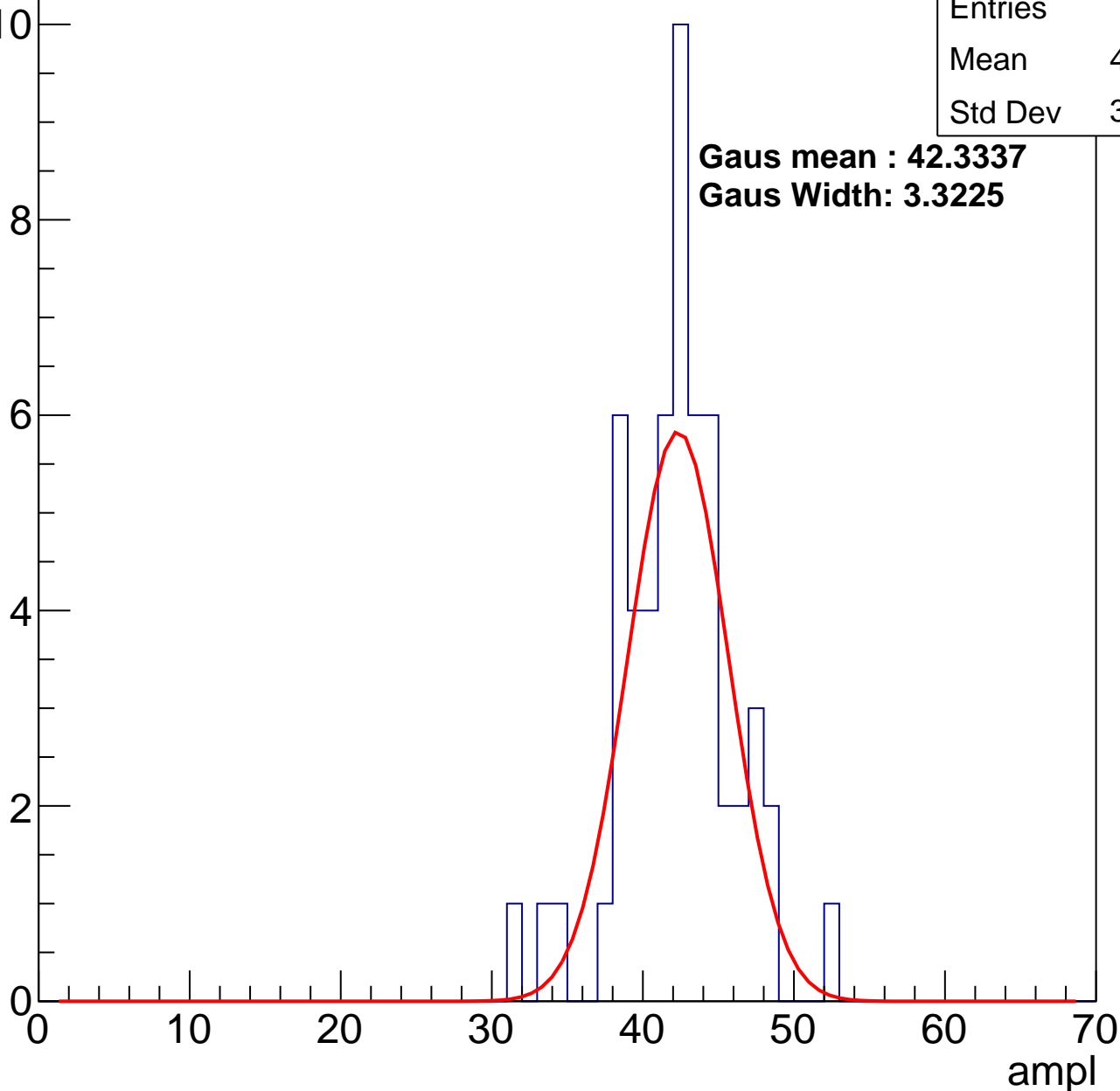
# B1L103S, U16-ch19, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	41.75
Std Dev	3.704

**Gaus mean : 42.3337**  
**Gaus Width: 3.3225**

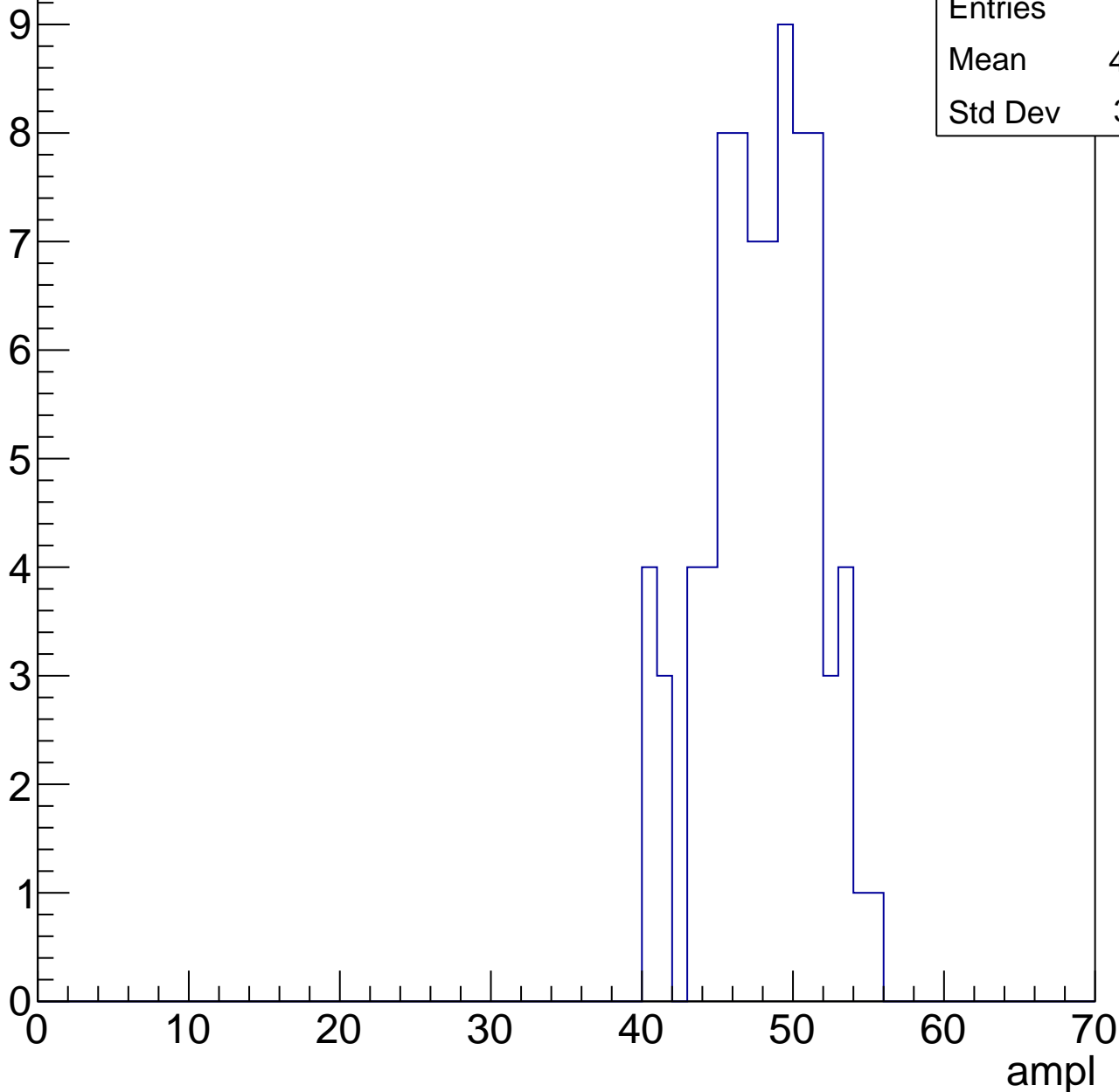


# B1L103S, U16-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

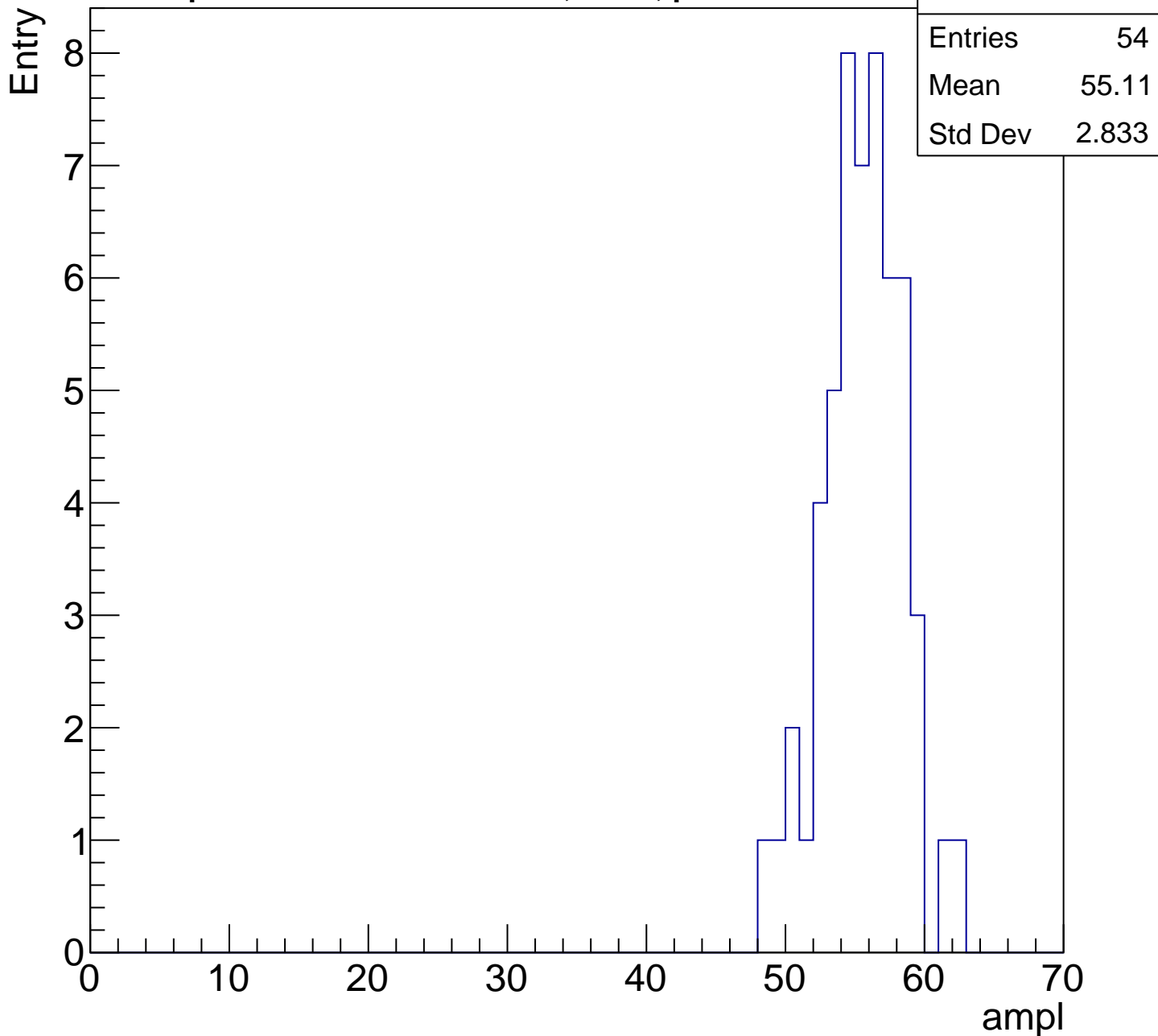
Entry

Entries	79
Mean	47.47
Std Dev	3.561



# B1L103S, U16-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

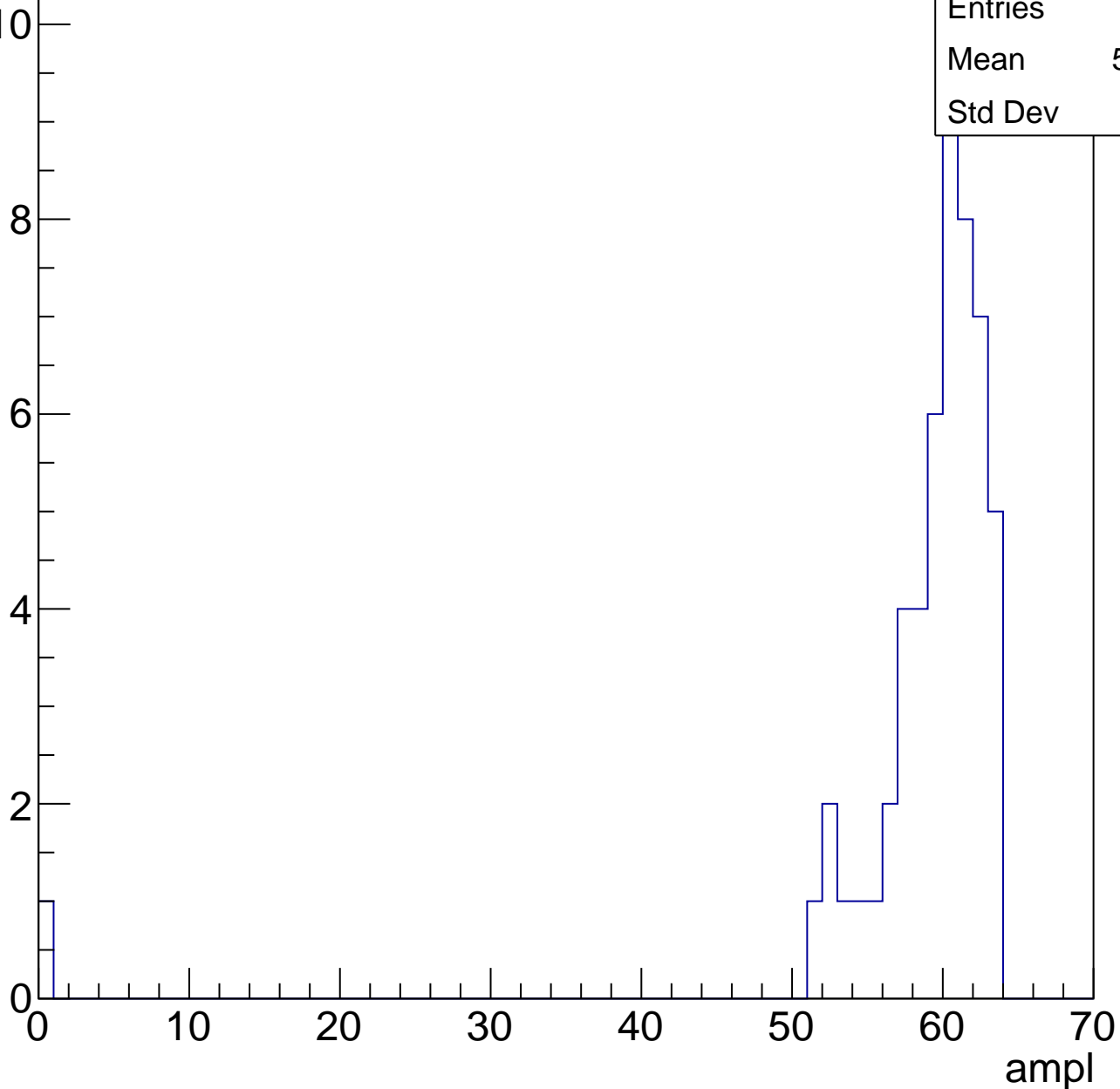


# B1L103S, U16-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	58.11
Std Dev	8.58



# B1L103S, U16-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

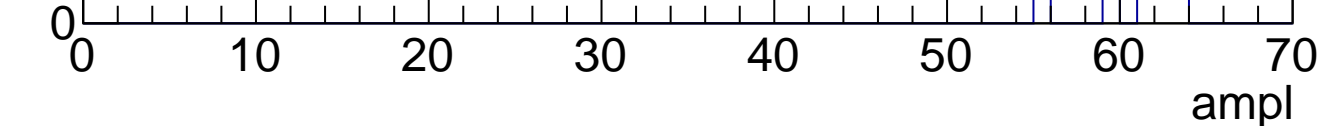
8

Mean

61

Std Dev

2.598





# B1L103S, U16-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch20, adc0

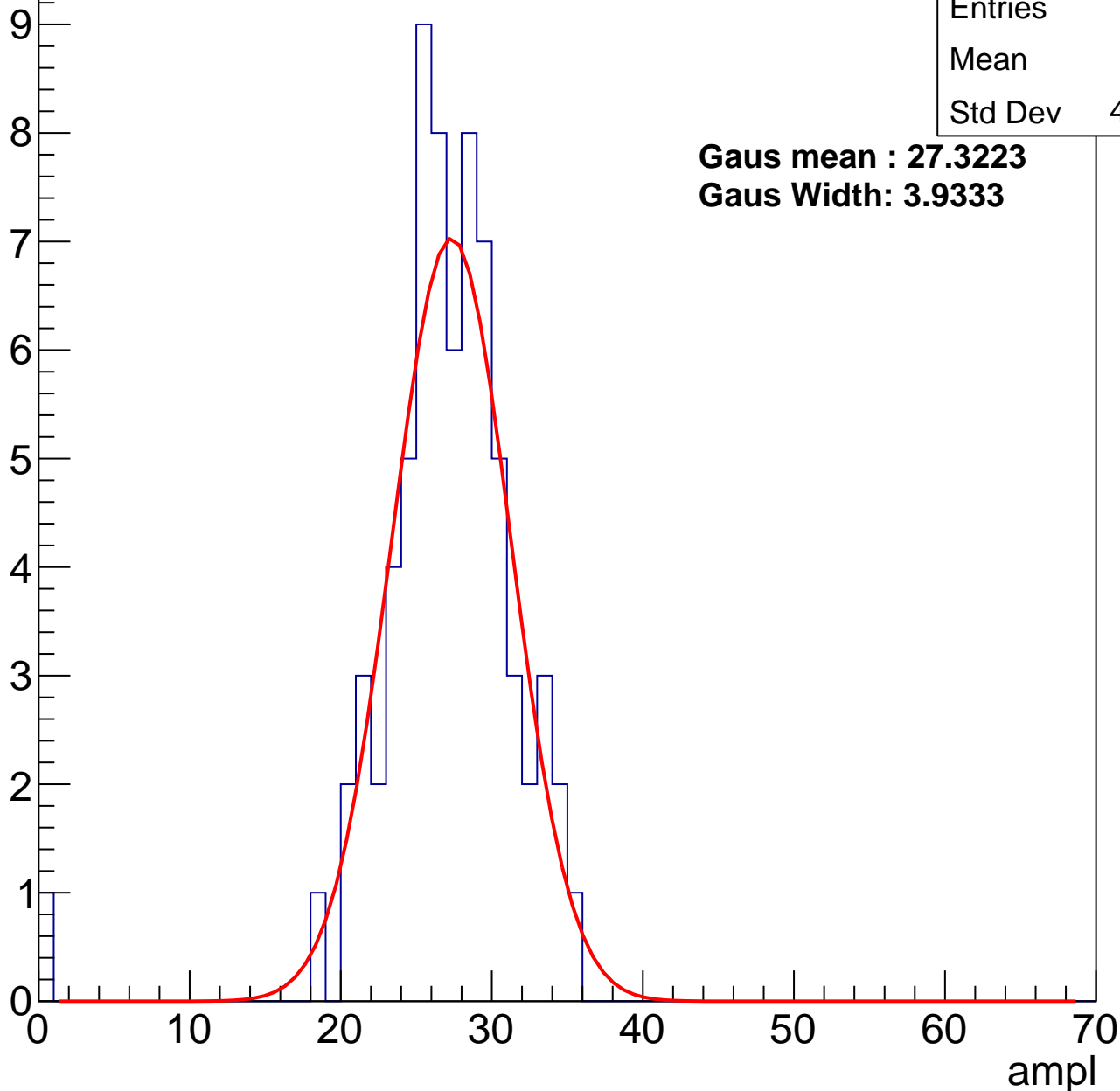
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	26.5
Std Dev	4.787

**Gaus mean : 27.3223**

**Gaus Width: 3.9333**



# B1L103S, U16-ch20, adc1

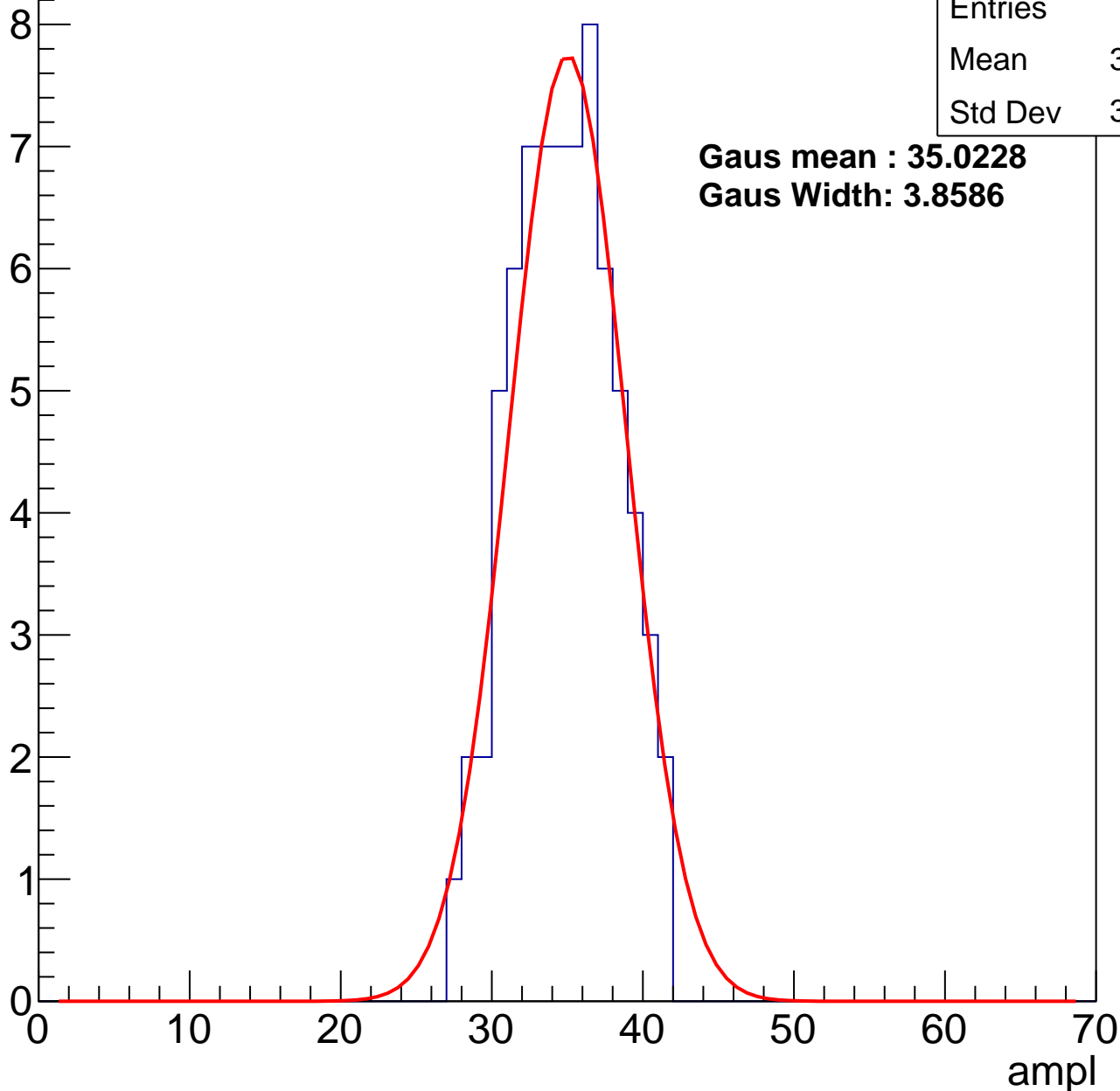
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	34.35
Std Dev	3.355

**Gaus mean : 35.0228**

**Gaus Width: 3.8586**

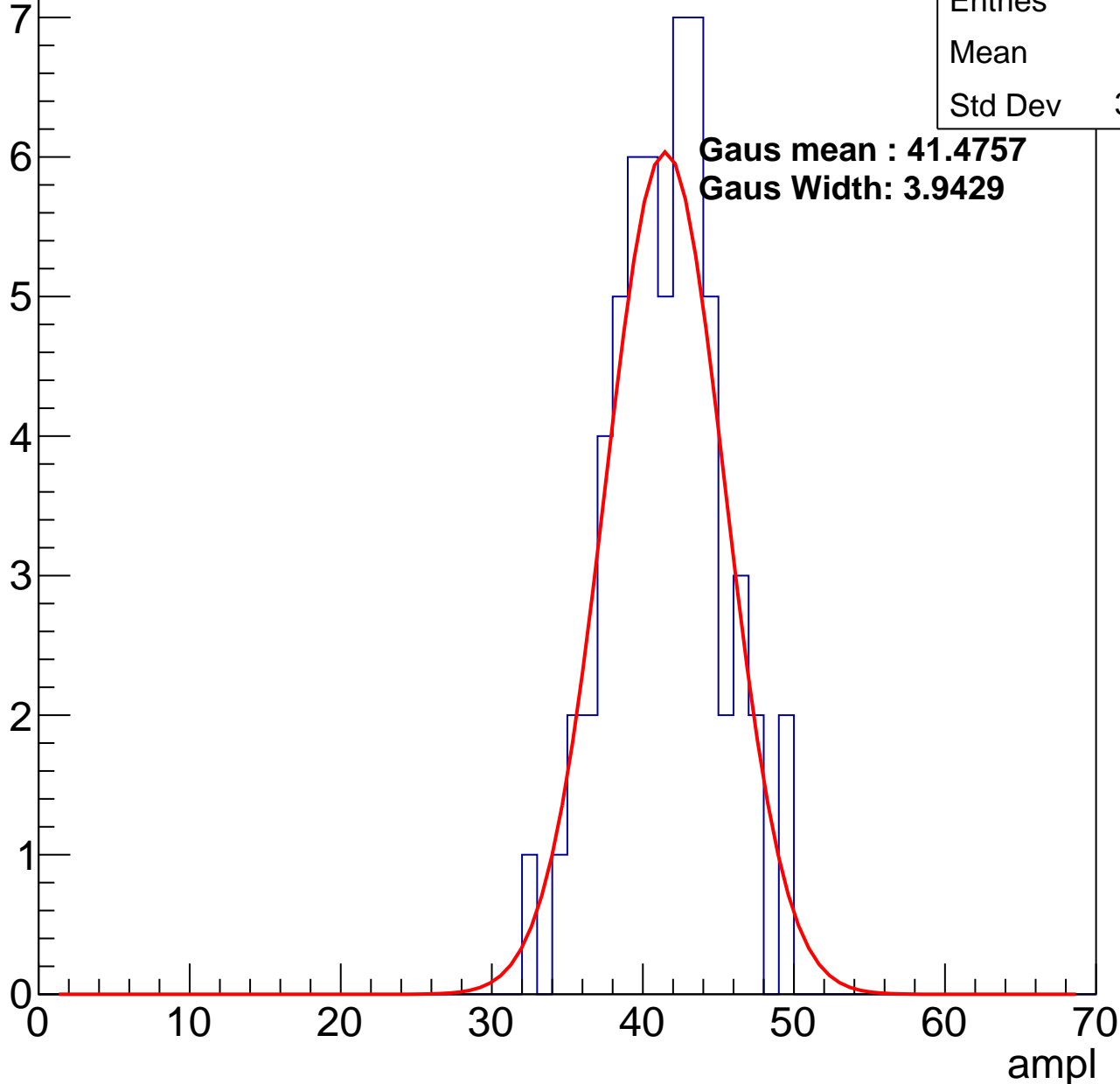


# B1L103S, U16-ch20, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	41
Std Dev	3.601

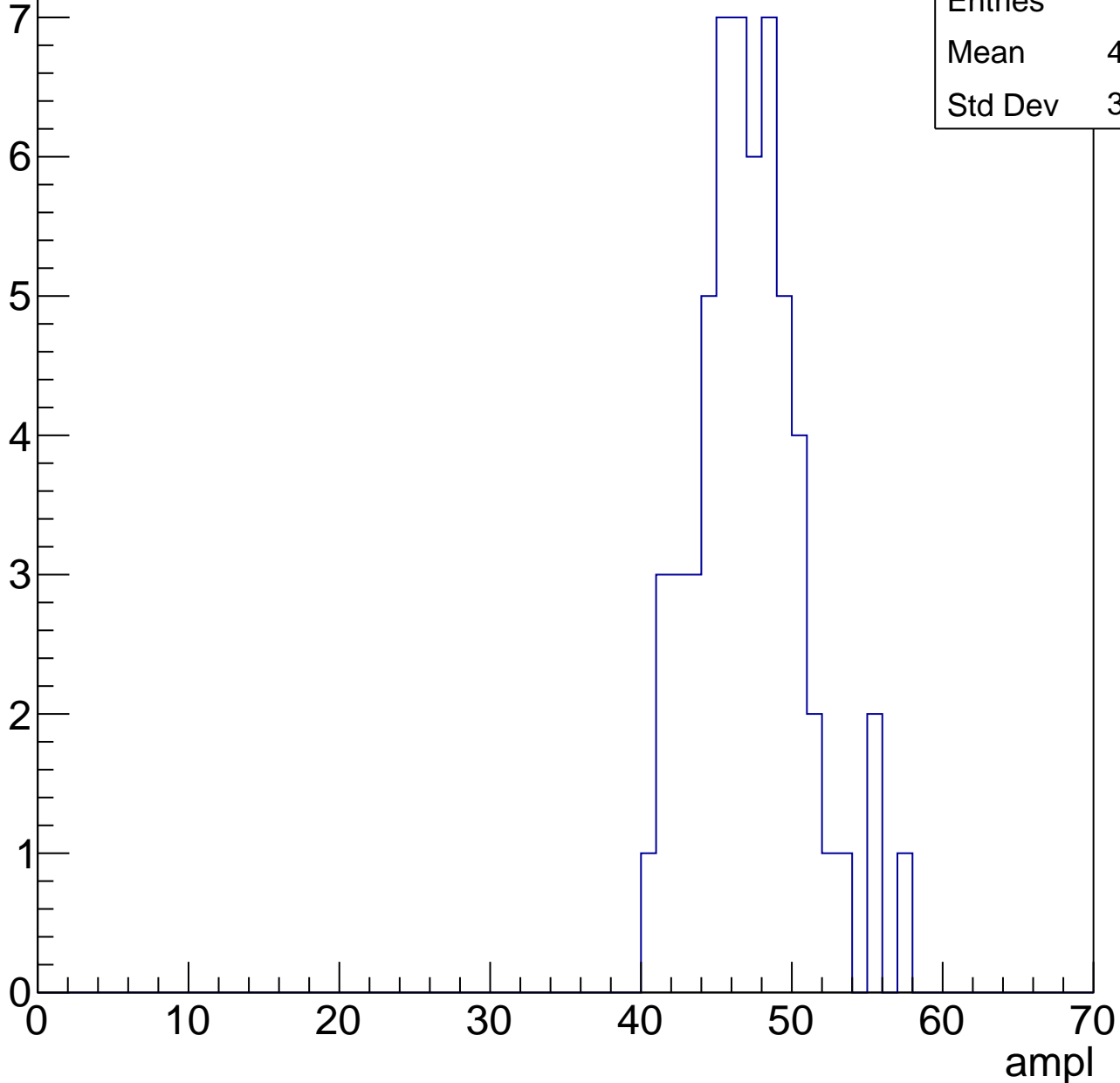


# B1L103S, U16-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

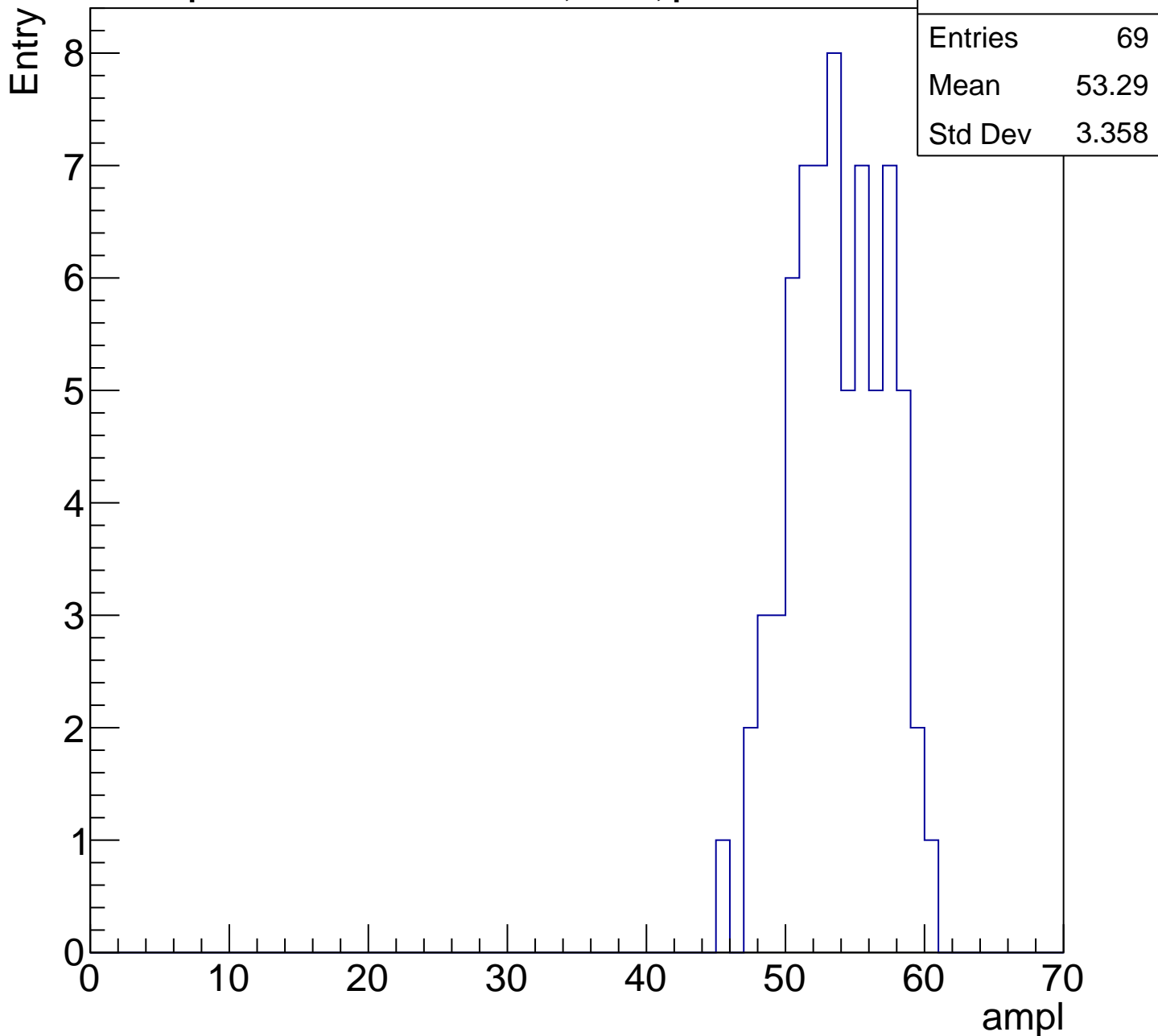
Entry

Entries	58
Mean	46.76
Std Dev	3.573



# B1L103S, U16-ch20, adc4

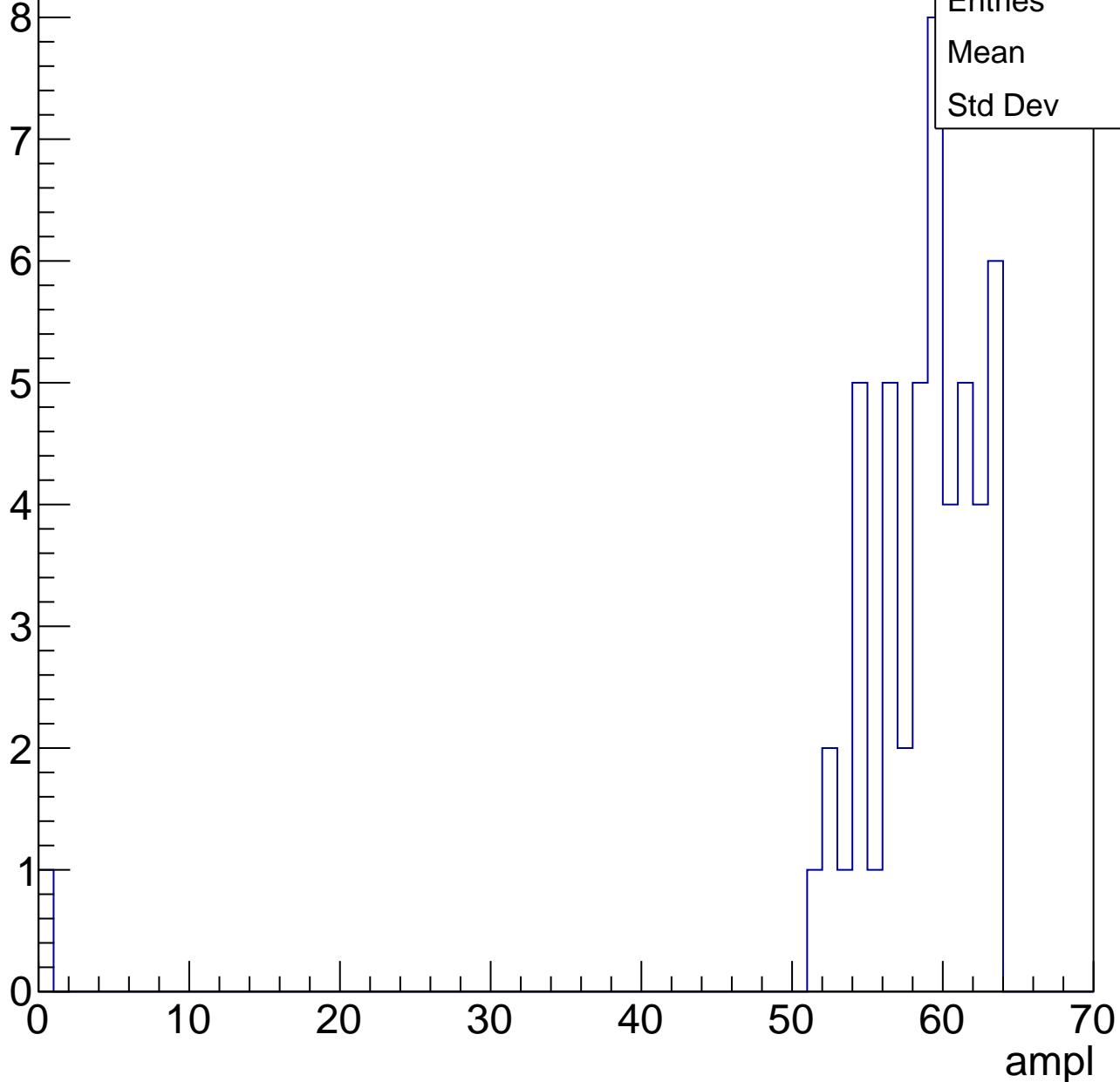
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U16-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



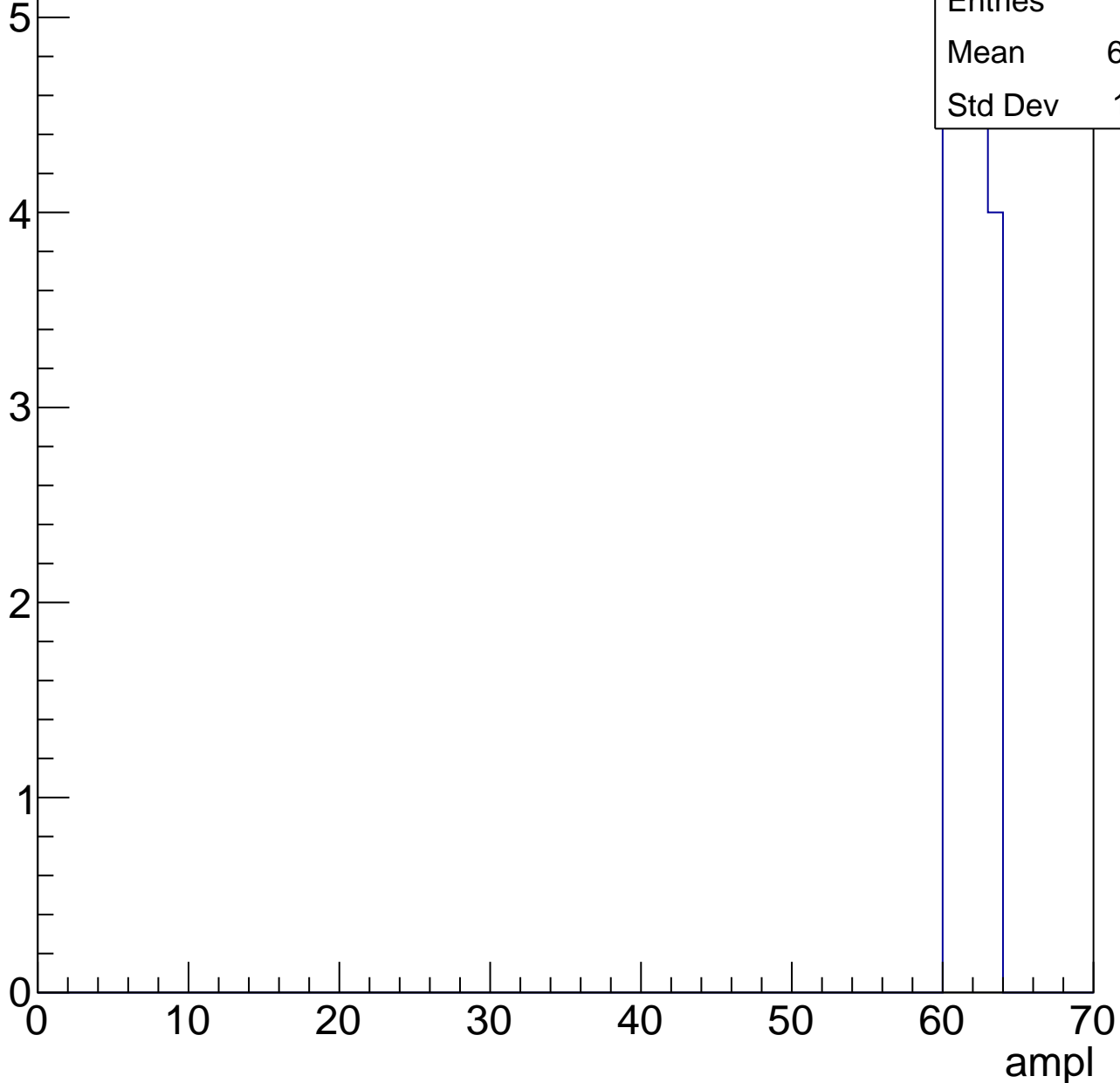
Entries	50
Mean	57.2
Std Dev	8.8

# B1L103S, U16-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	19
Mean	61.42
Std Dev	1.091





# B1L103S, U16-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch21, adc0

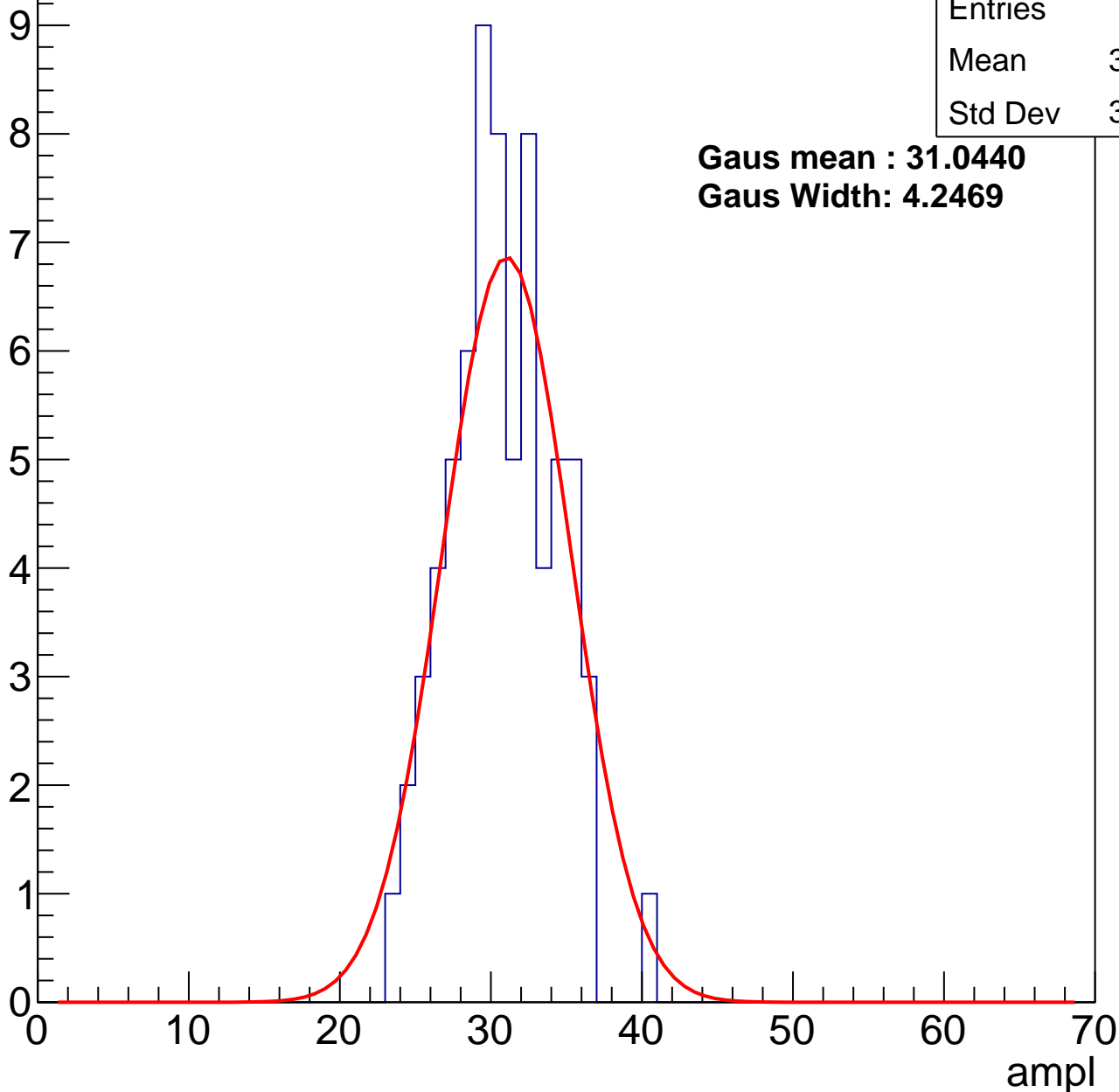
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	30.29
Std Dev	3.444

**Gaus mean : 31.0440**

**Gaus Width: 4.2469**



# B1L103S, U16-ch21, adc1

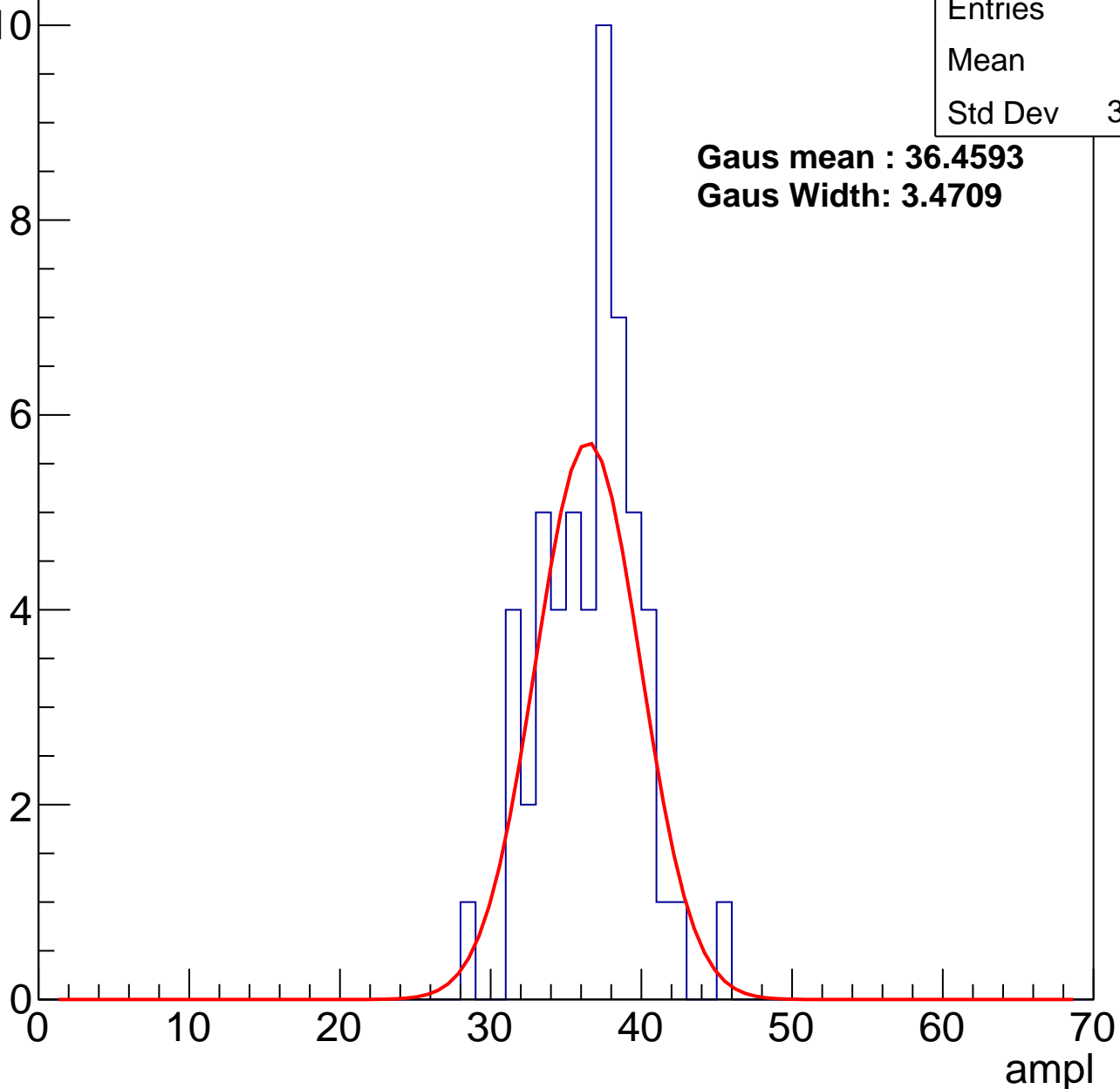
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	36.2
Std Dev	3.188

**Gaus mean : 36.4593**

**Gaus Width: 3.4709**



# B1L103S, U16-ch21, adc2

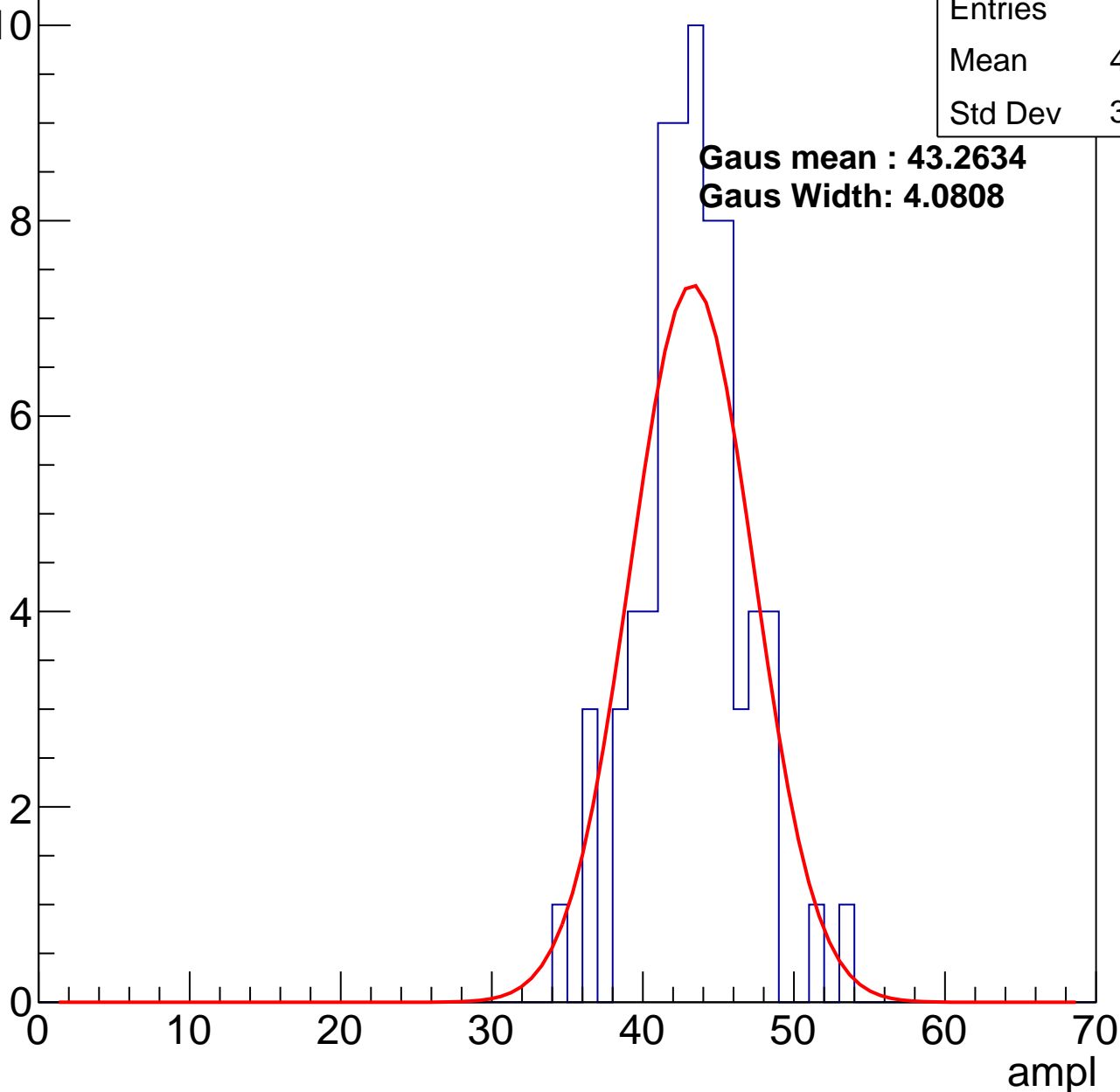
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	42.82
Std Dev	3.417

**Gaus mean : 43.2634**

**Gaus Width: 4.0808**



# B1L103S, U16-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

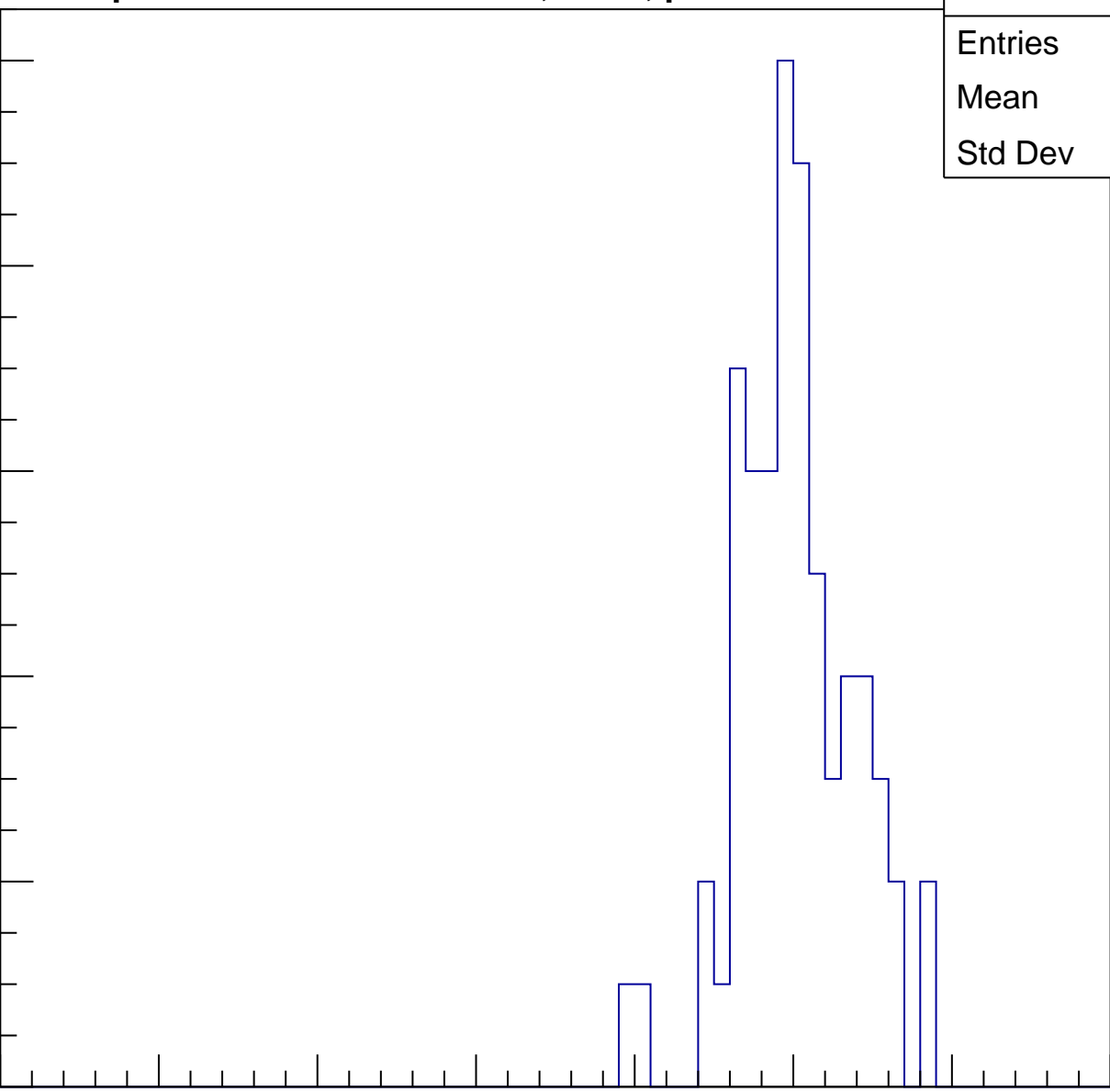
Entries	66
Mean	49.64
Std Dev	3.695

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

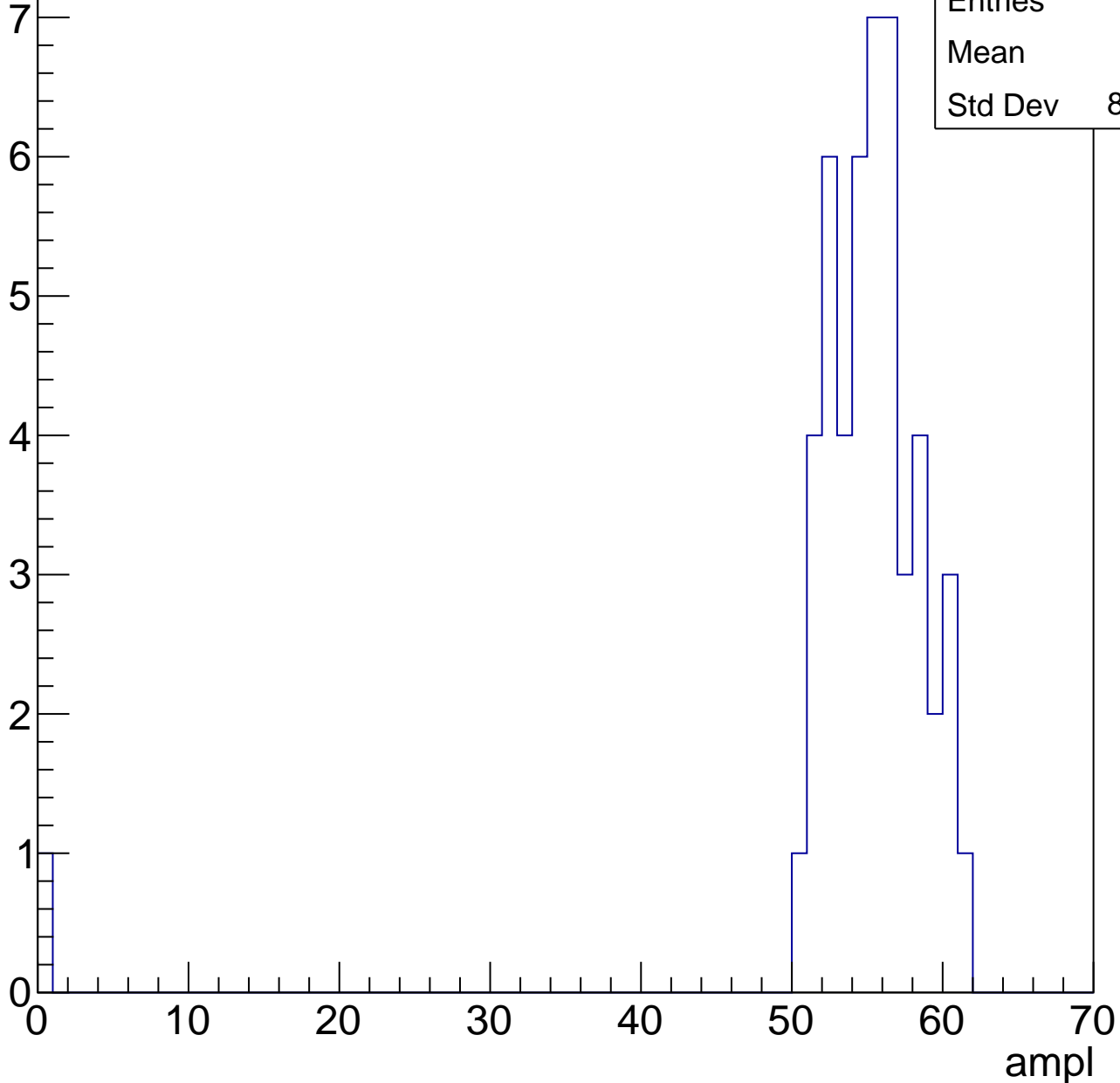


# B1L103S, U16-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	53.9
Std Dev	8.242

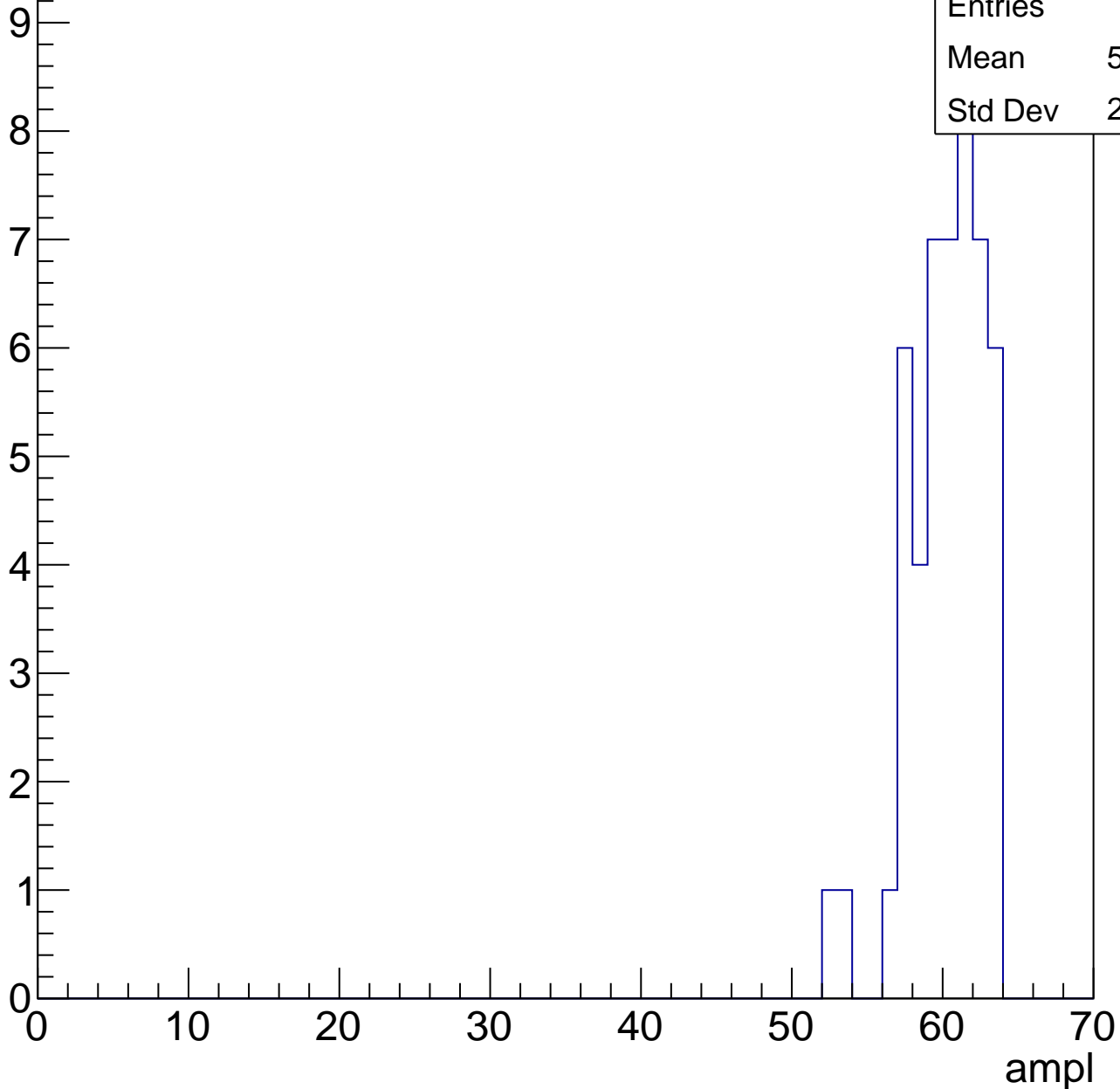


# B1L103S, U16-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

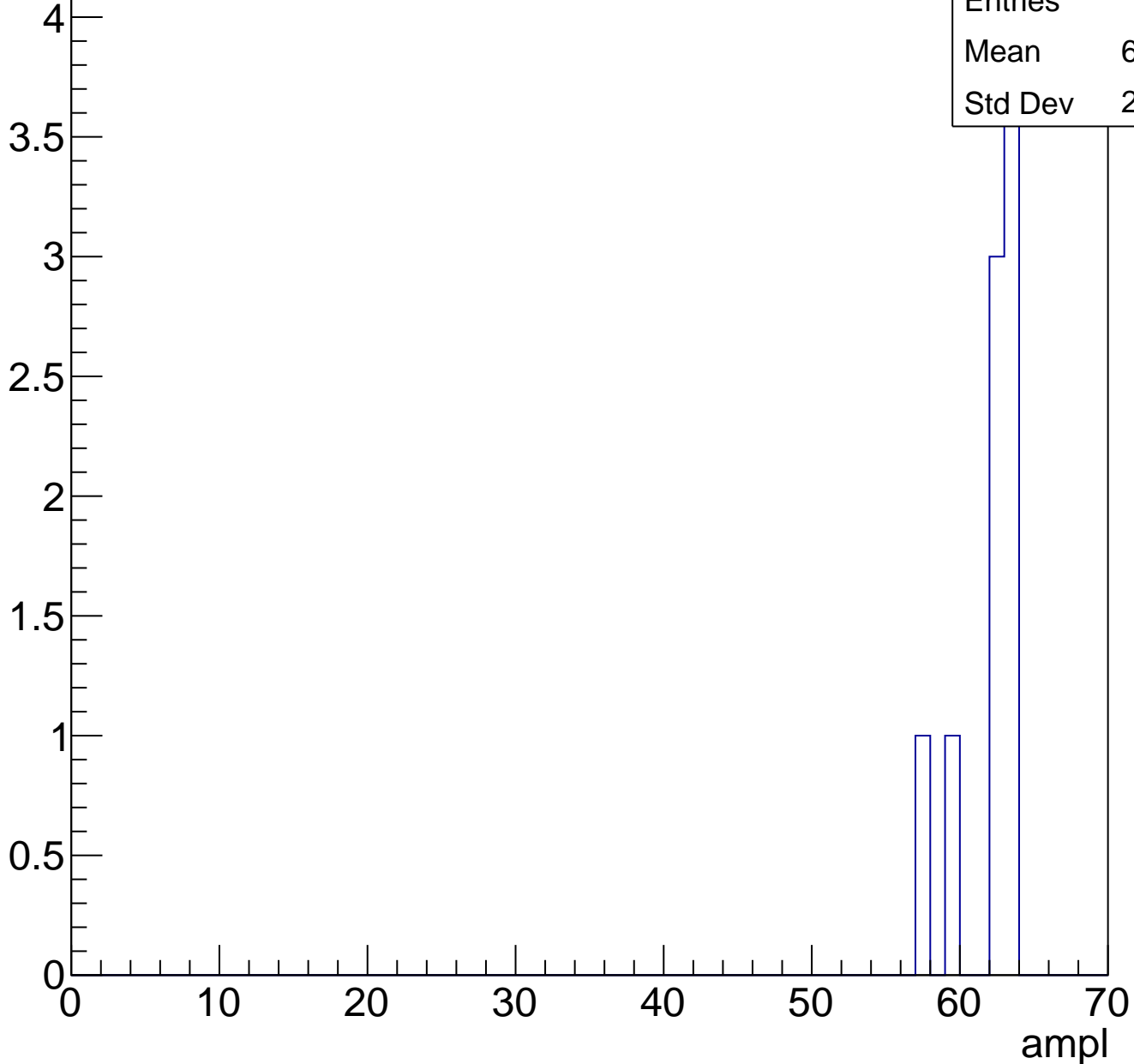
Entries	49
Mean	59.78
Std Dev	2.452



# B1L103S, U16-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	9
Mean	61.56
Std Dev	2.006



# B1L103S, U16-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U16-ch22, adc0

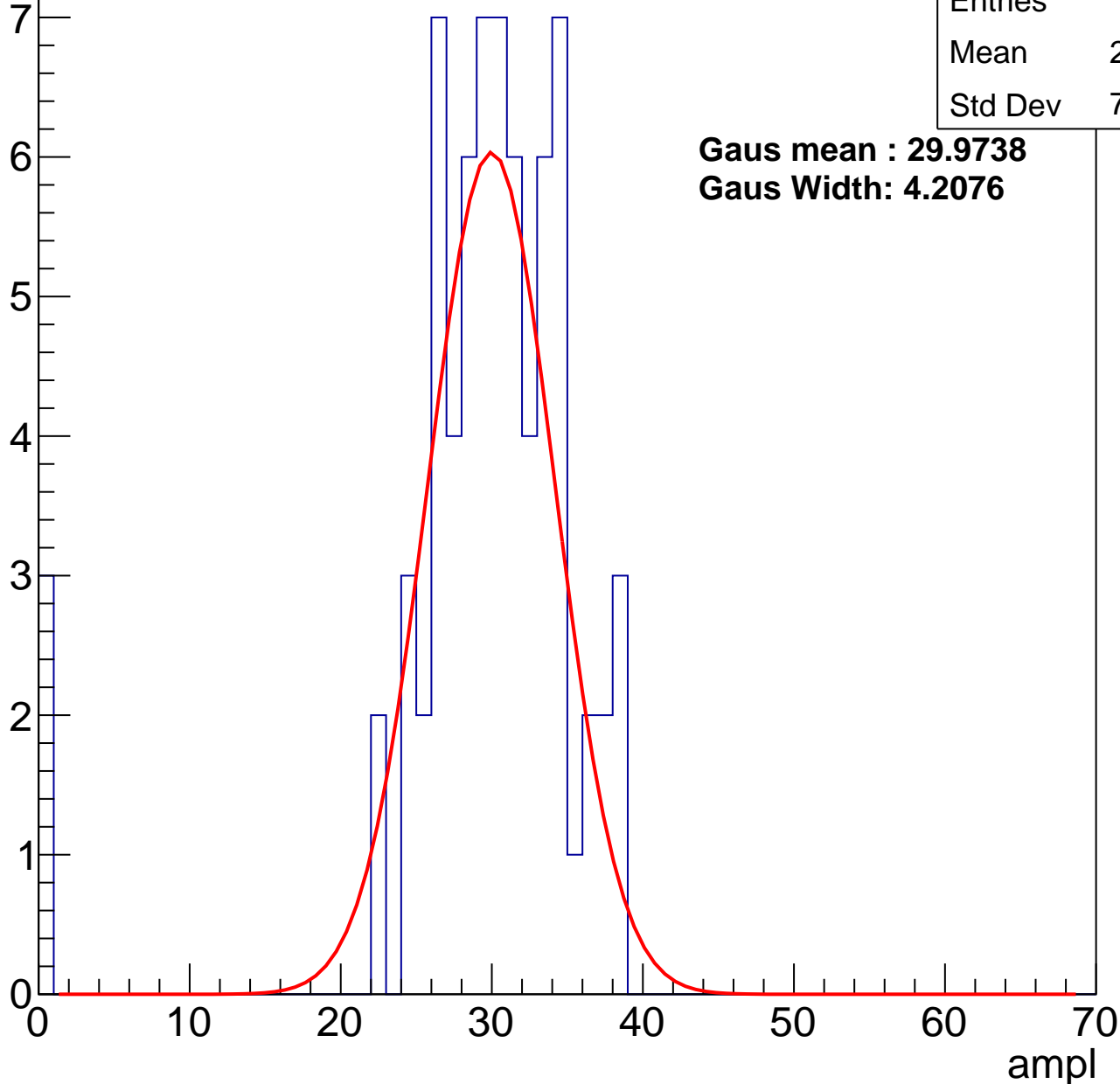
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	28.92
Std Dev	7.125

**Gaus mean : 29.9738**

**Gaus Width: 4.2076**



# B1L103S, U16-ch22, adc1

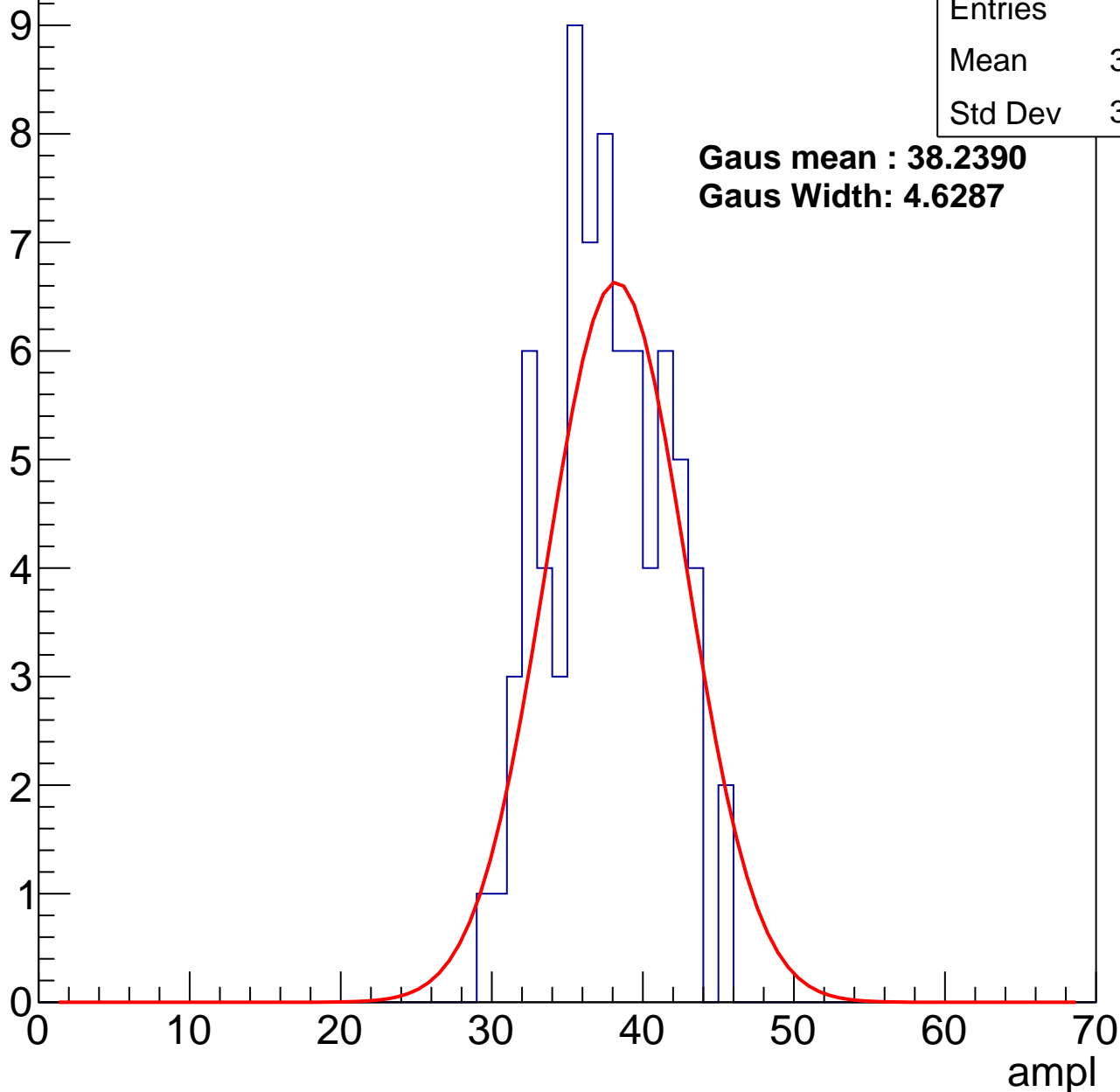
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	37.08
Std Dev	3.766

**Gaus mean : 38.2390**

**Gaus Width: 4.6287**



# B1L103S, U16-ch22, adc2

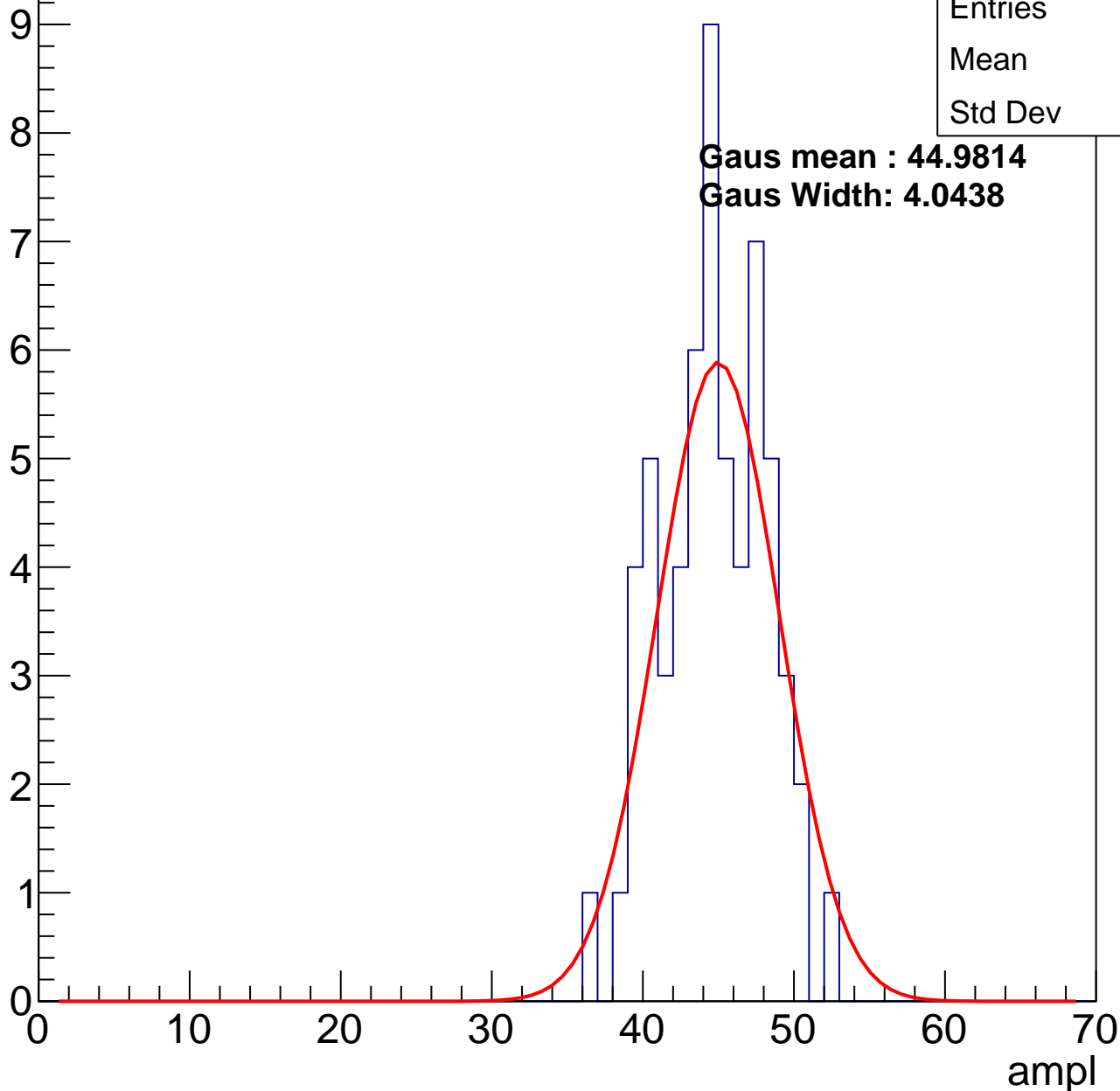
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	44.2
Std Dev	3.42

**Gaus mean : 44.9814**

**Gaus Width: 4.0438**



# B1L103S, U16-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	71
Mean	50.65
Std Dev	4.273

Entry

10

8

6

4

2

0

0

10

20

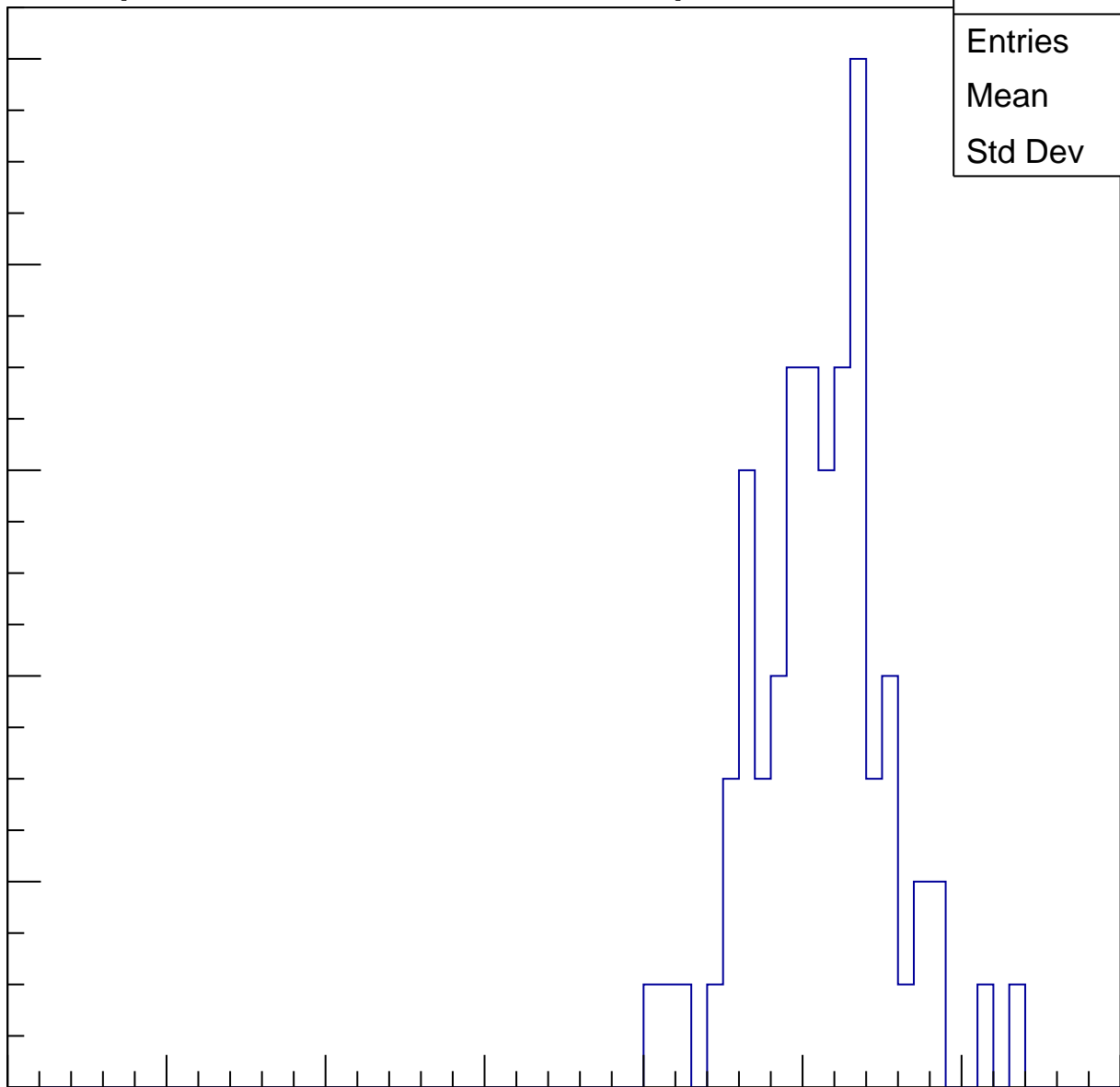
30

40

50

60

ampl

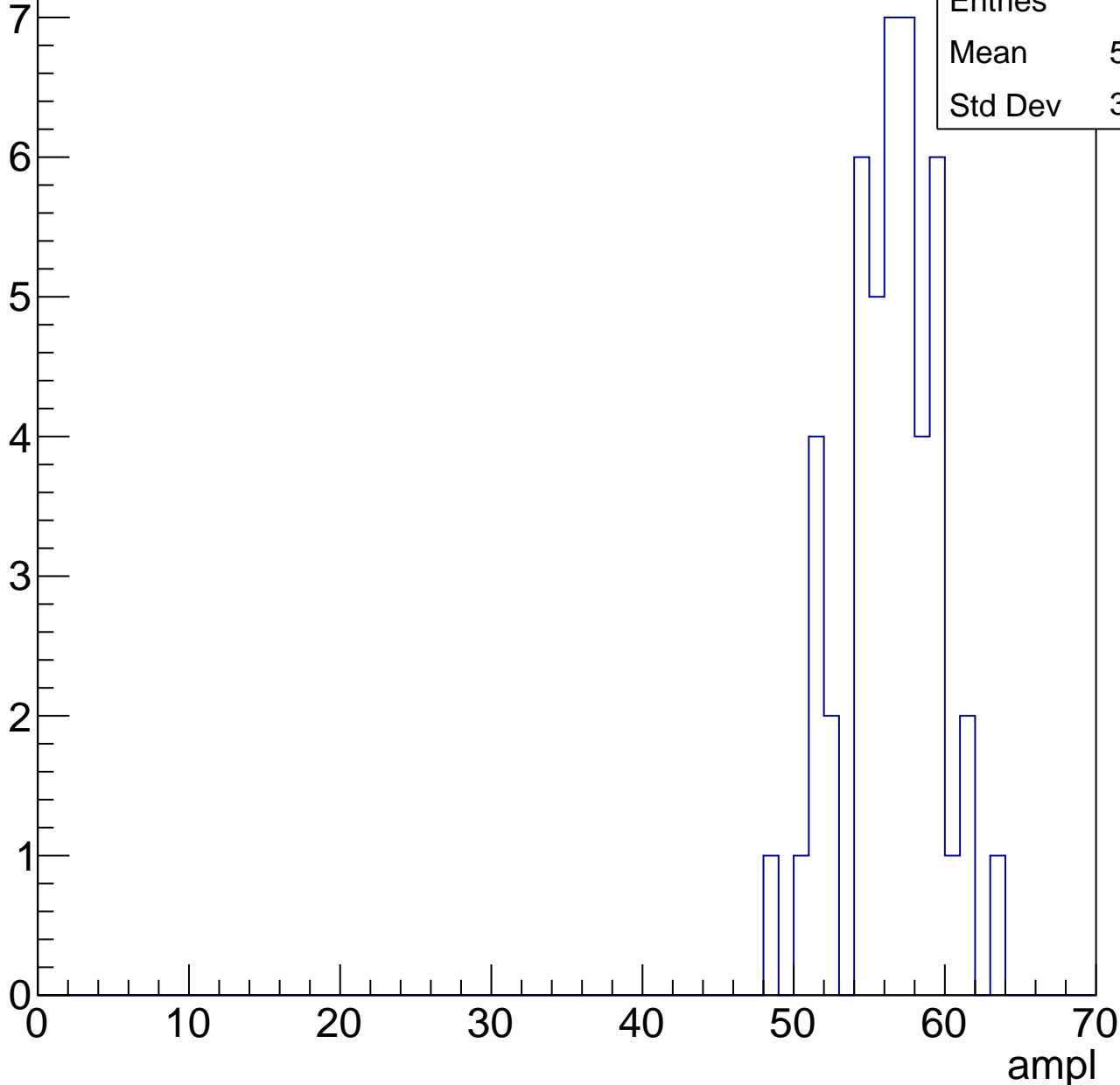


# B1L103S, U16-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

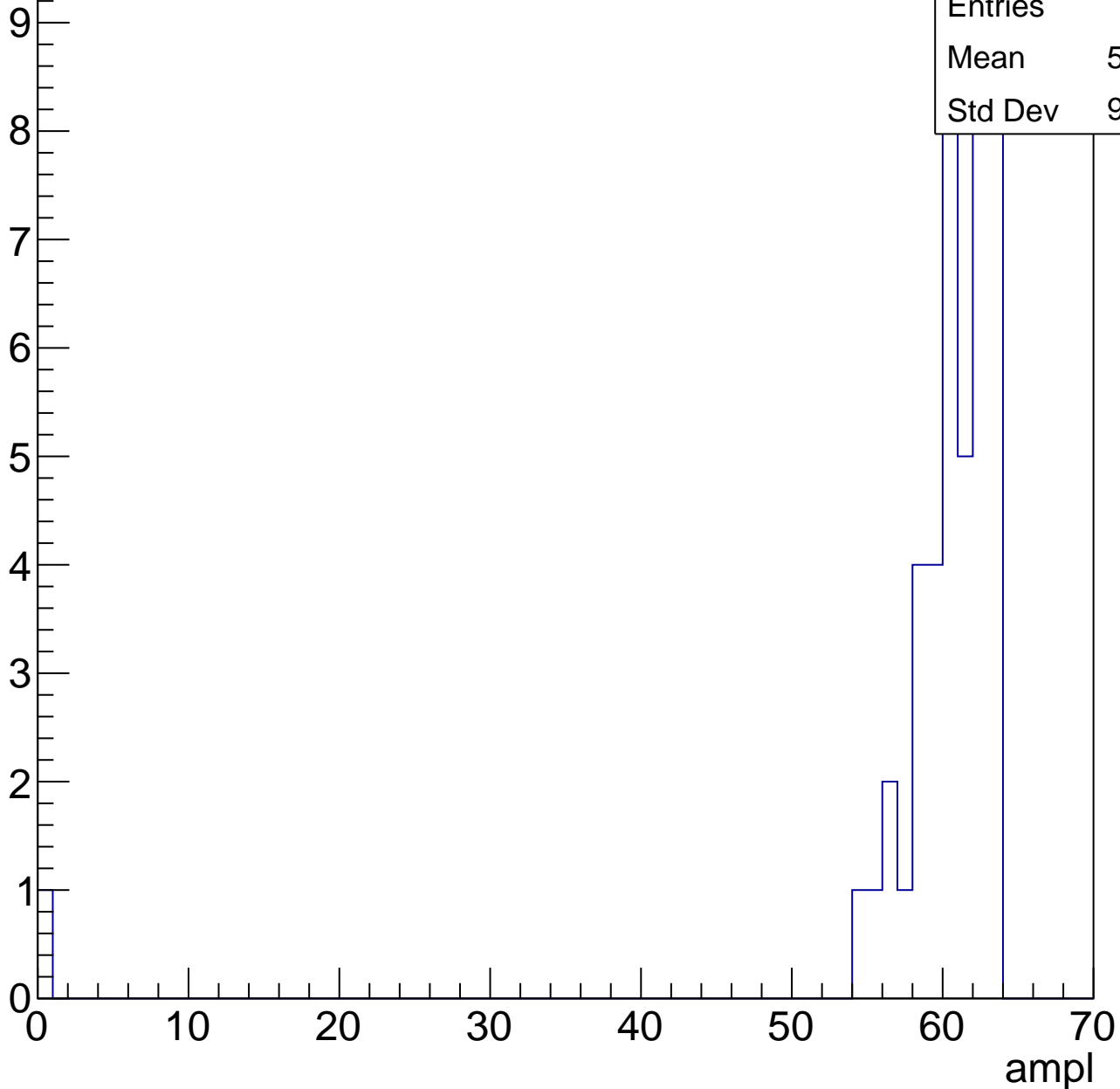
Entries	47
Mean	55.89
Std Dev	3.103



# B1L103S, U16-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	61.33
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B1L103S, U16-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U16-ch23, adc0

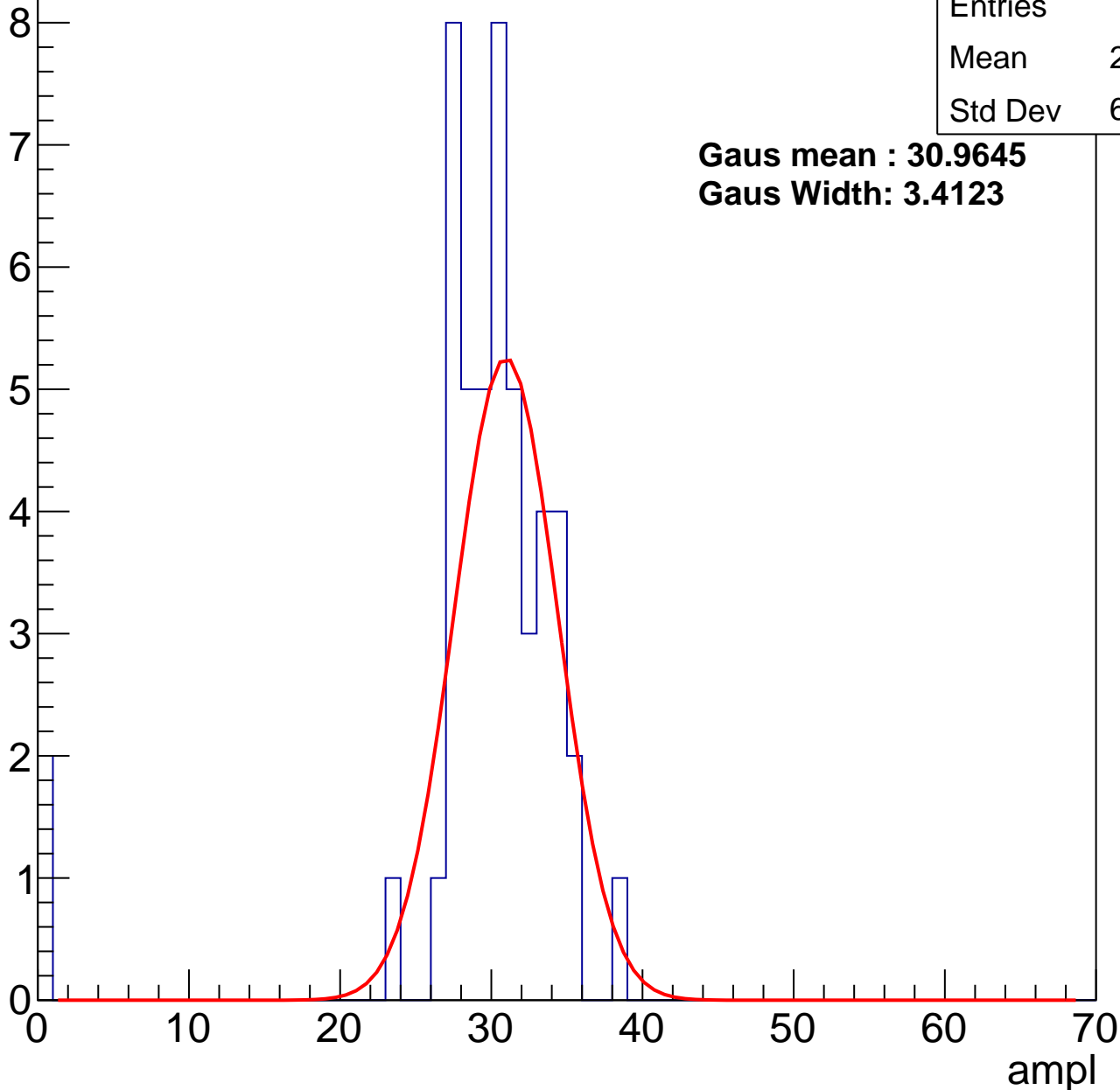
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	28.92
Std Dev	6.602

**Gaus mean : 30.9645**

**Gaus Width: 3.4123**



# B1L103S, U16-ch23, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	88
Mean	37.39
Std Dev	3.722

**Gaus mean : 37.7091**

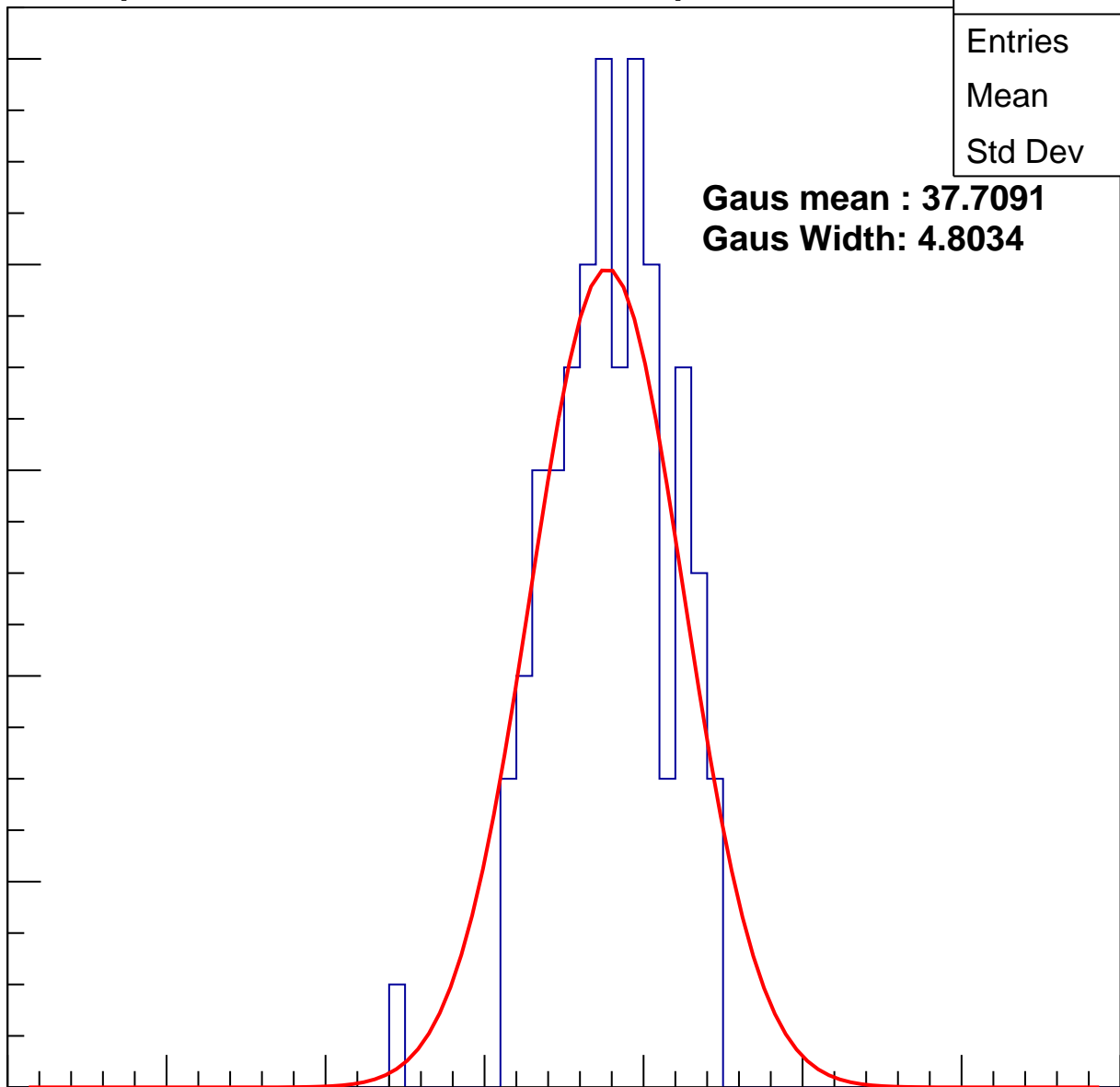
**Gaus Width: 4.8034**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U16-ch23, adc2

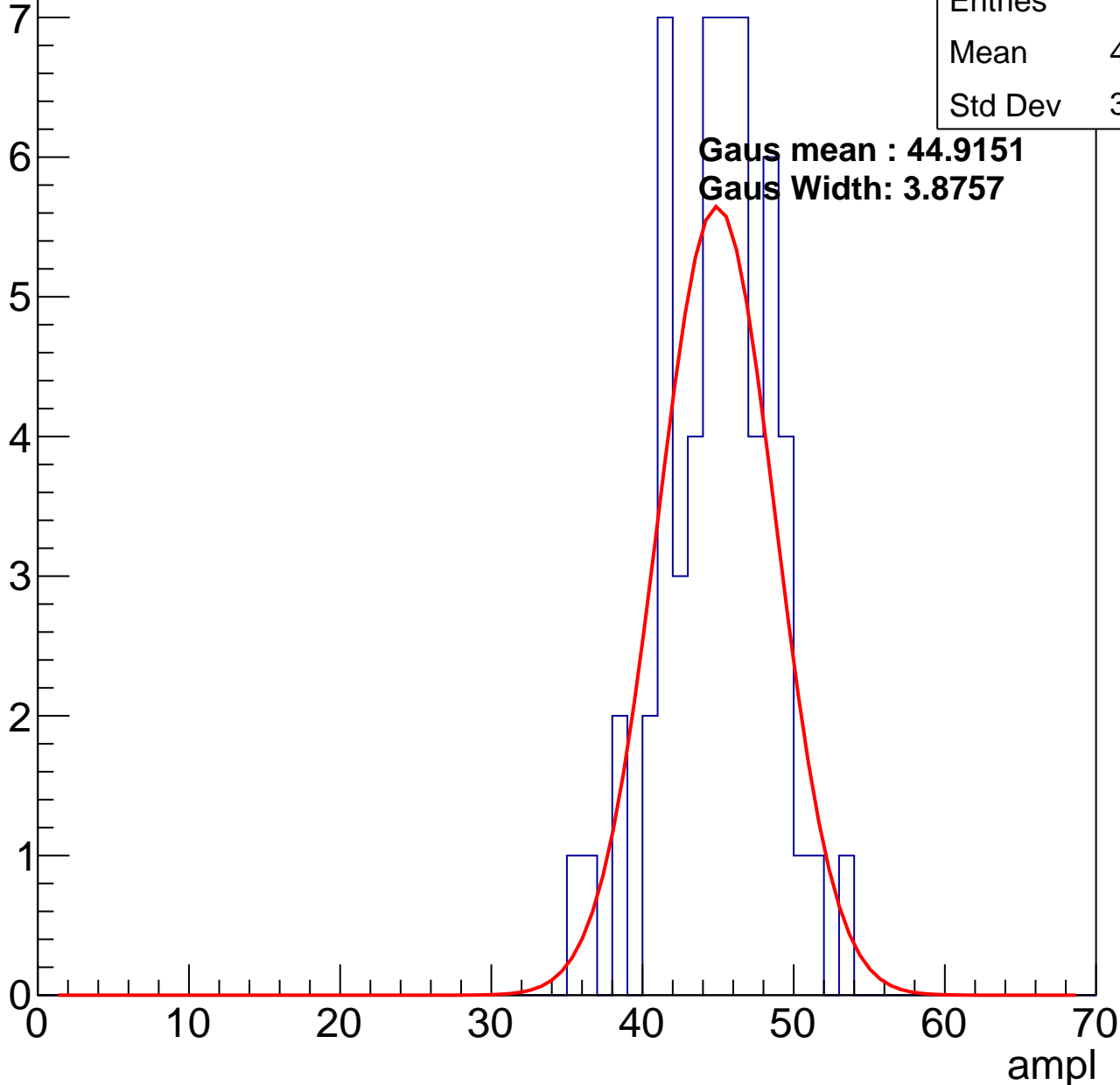
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	44.53
Std Dev	3.583

**Gaus mean : 44.9151**

**Gaus Width: 3.8757**

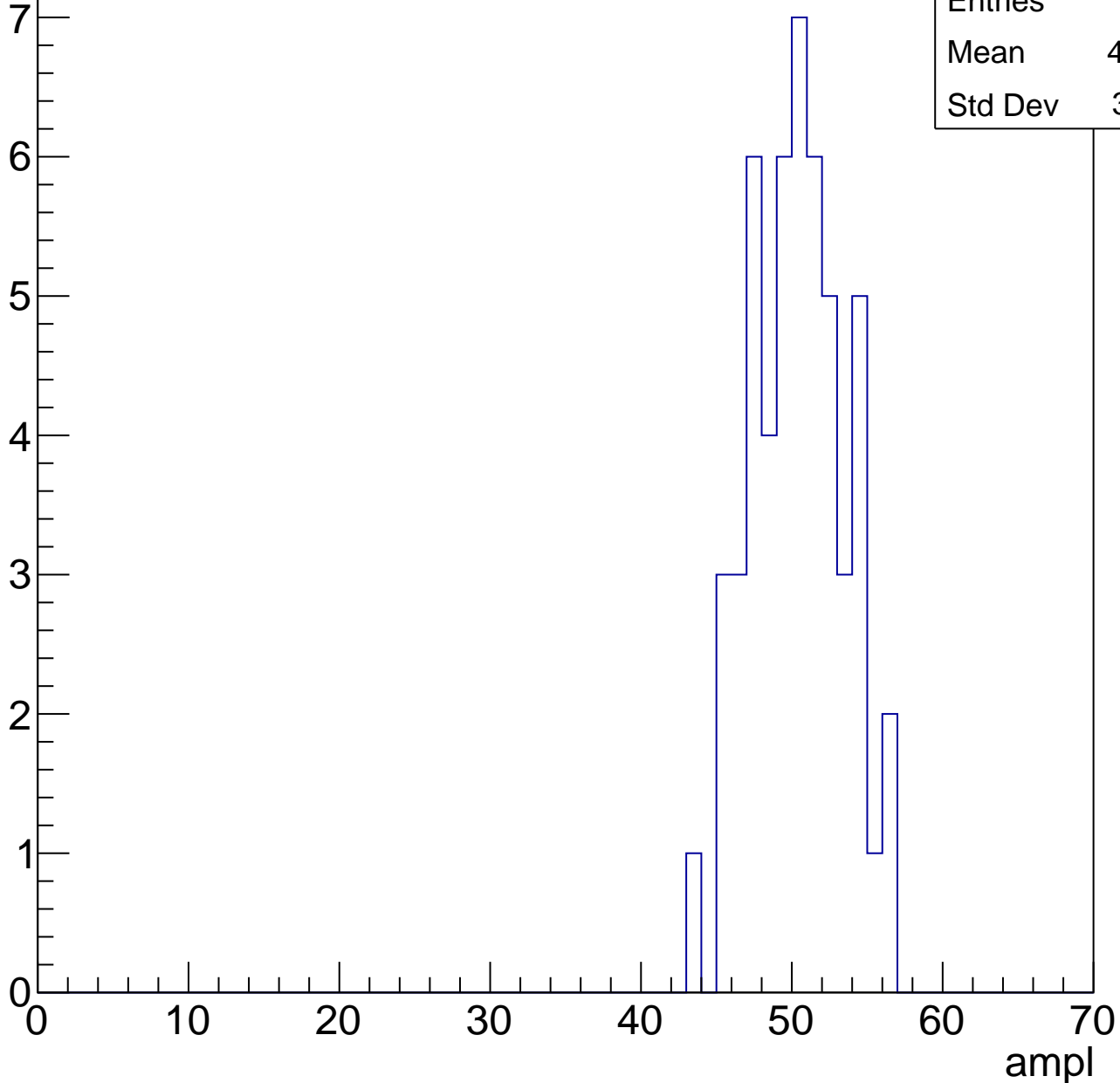


# B1L103S, U16-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

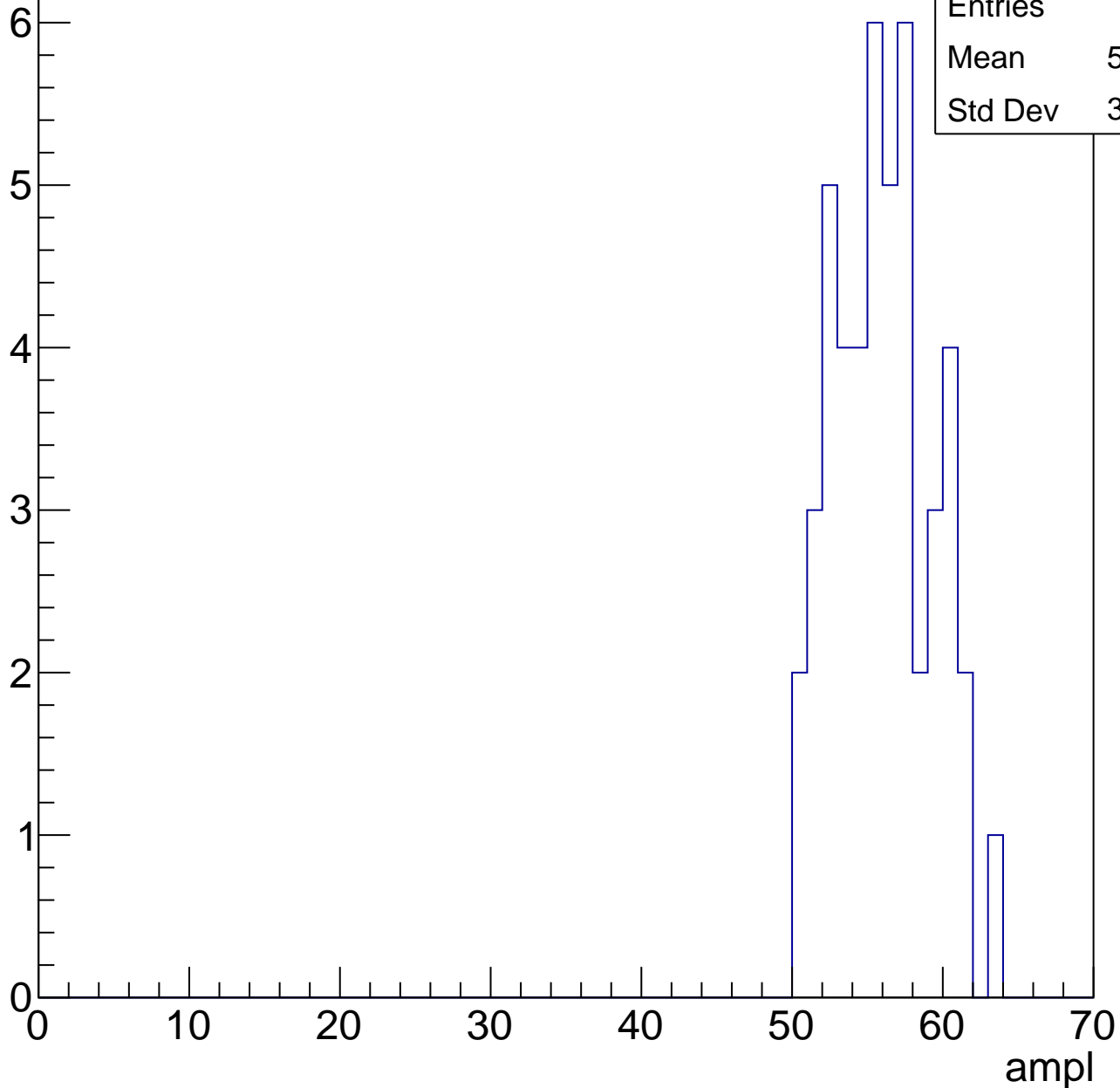
Entries	52
Mean	49.92
Std Dev	3.031



# B1L103S, U16-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

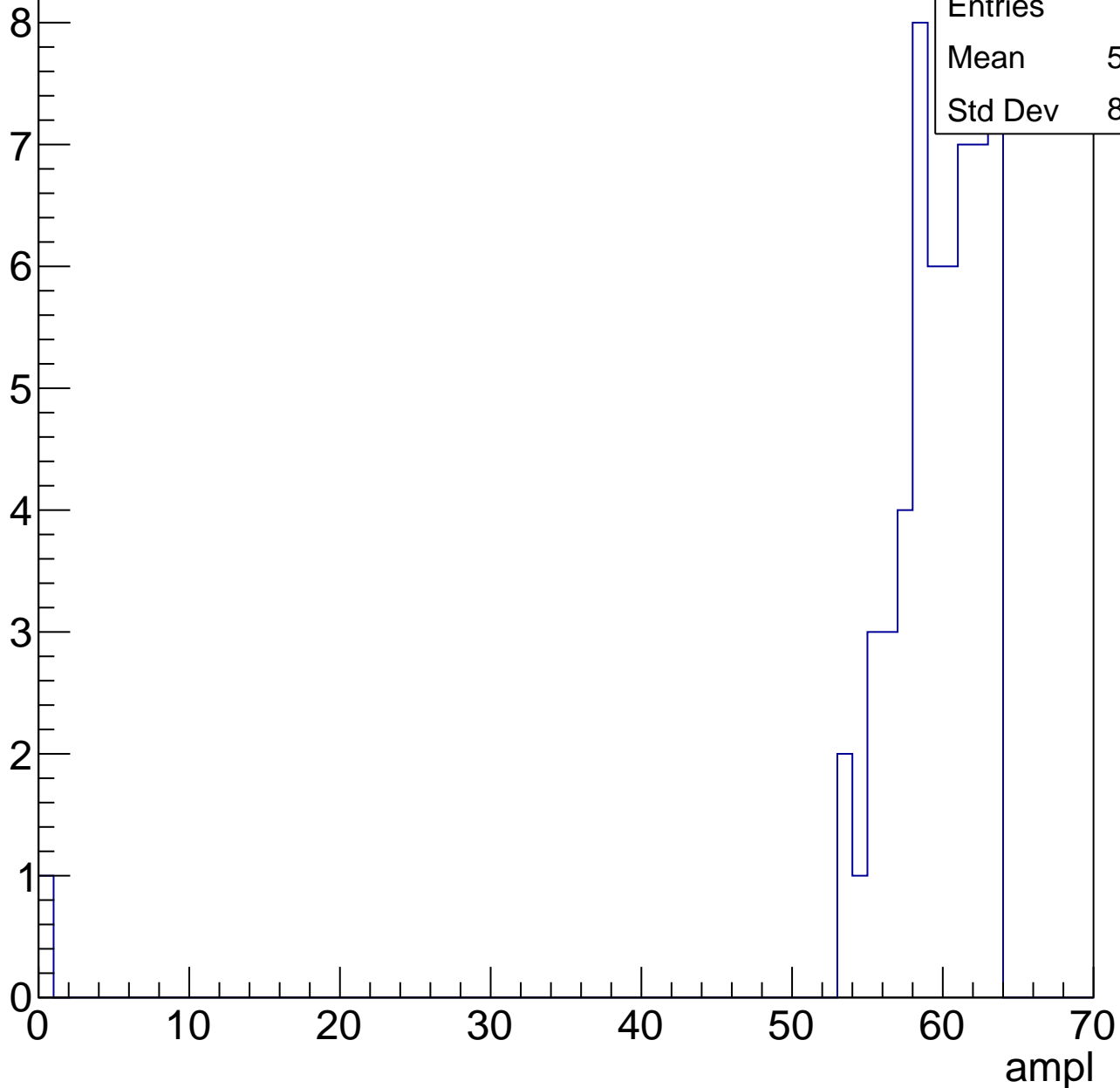


Entries	47
Mean	55.55
Std Dev	3.194

# B1L103S, U16-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

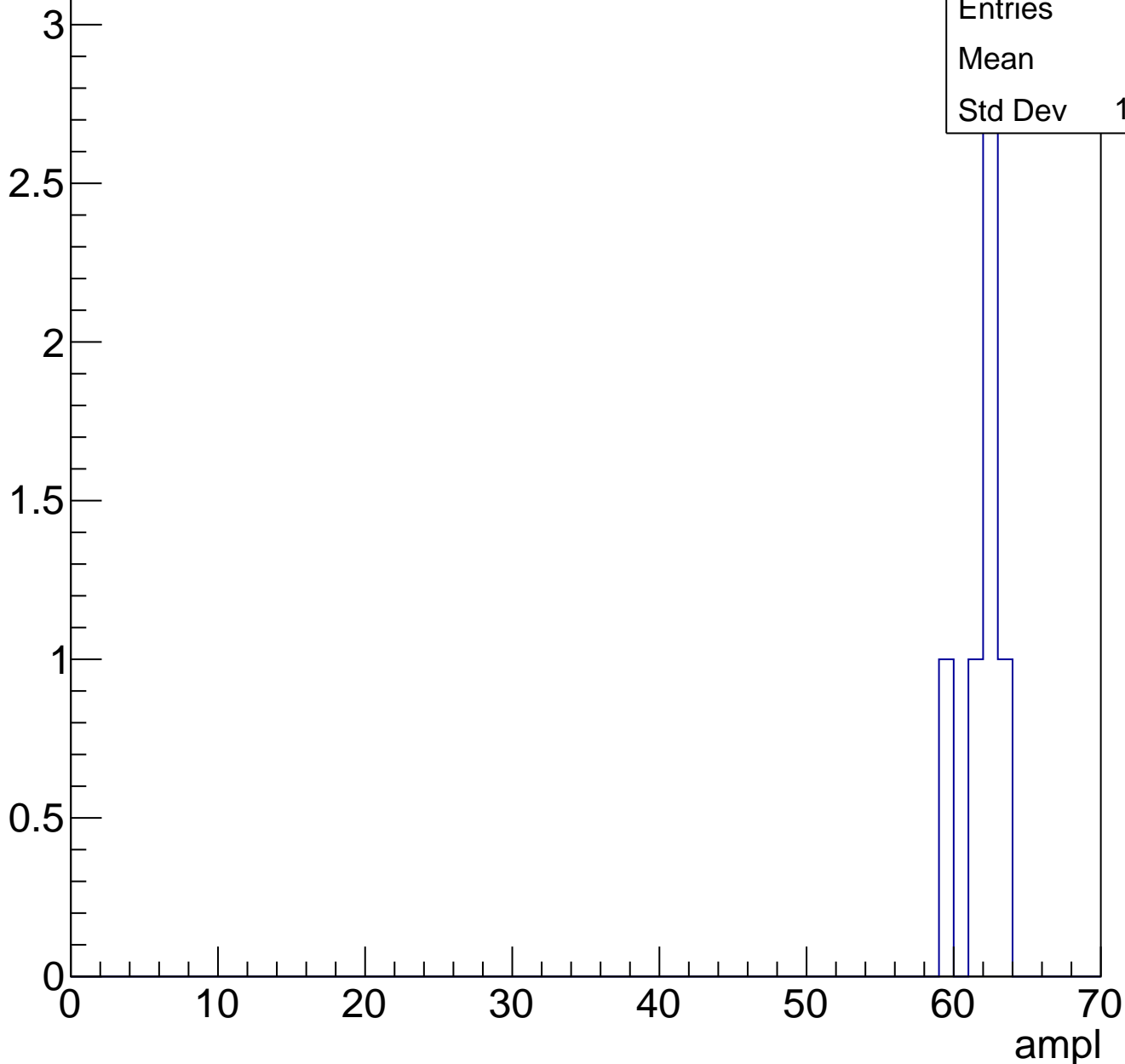
Entry



# B1L103S, U16-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch24, adc0

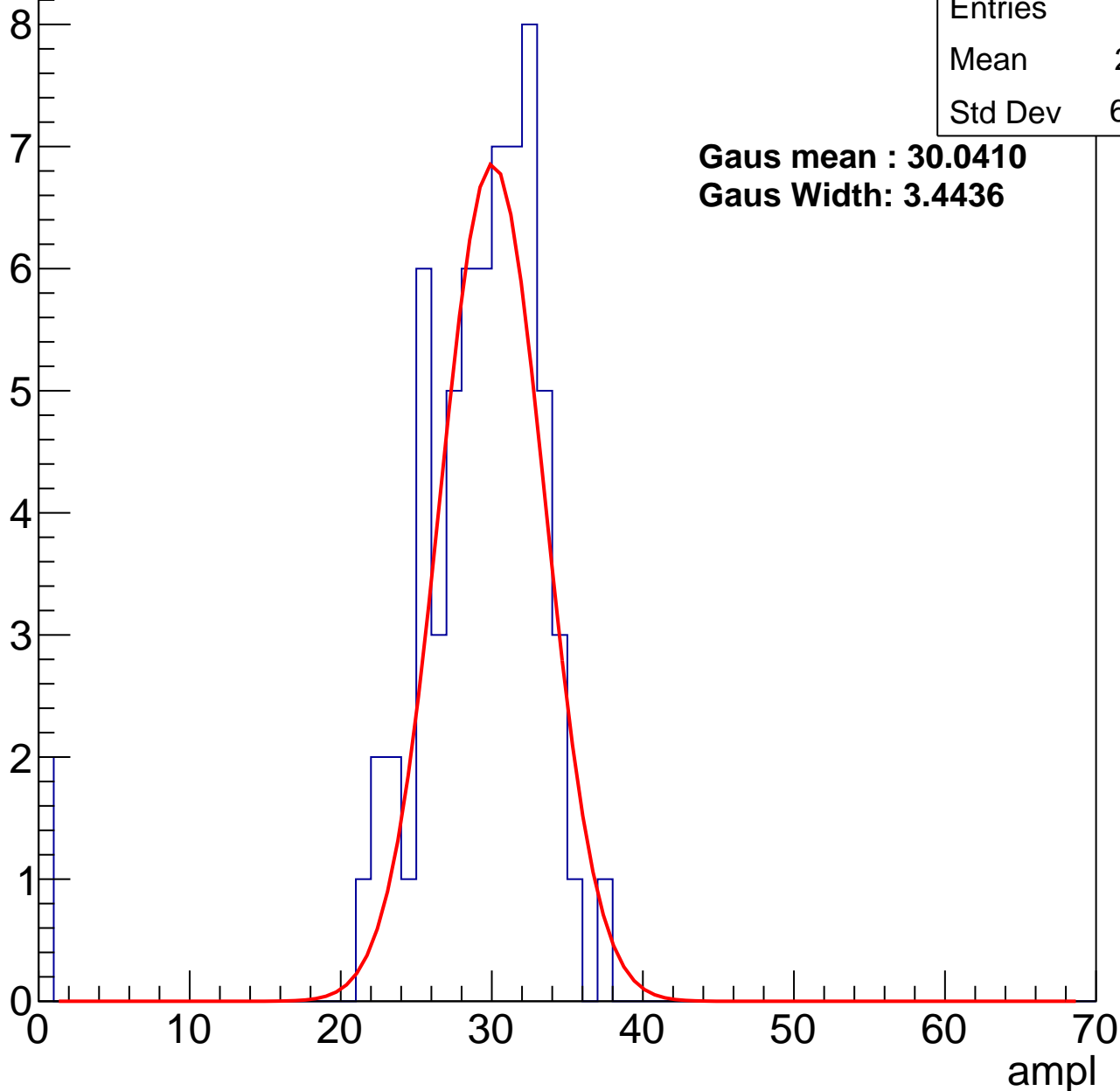
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	28.21
Std Dev	6.044

**Gaus mean : 30.0410**

**Gaus Width: 3.4436**



# B1L103S, U16-ch24, adc1

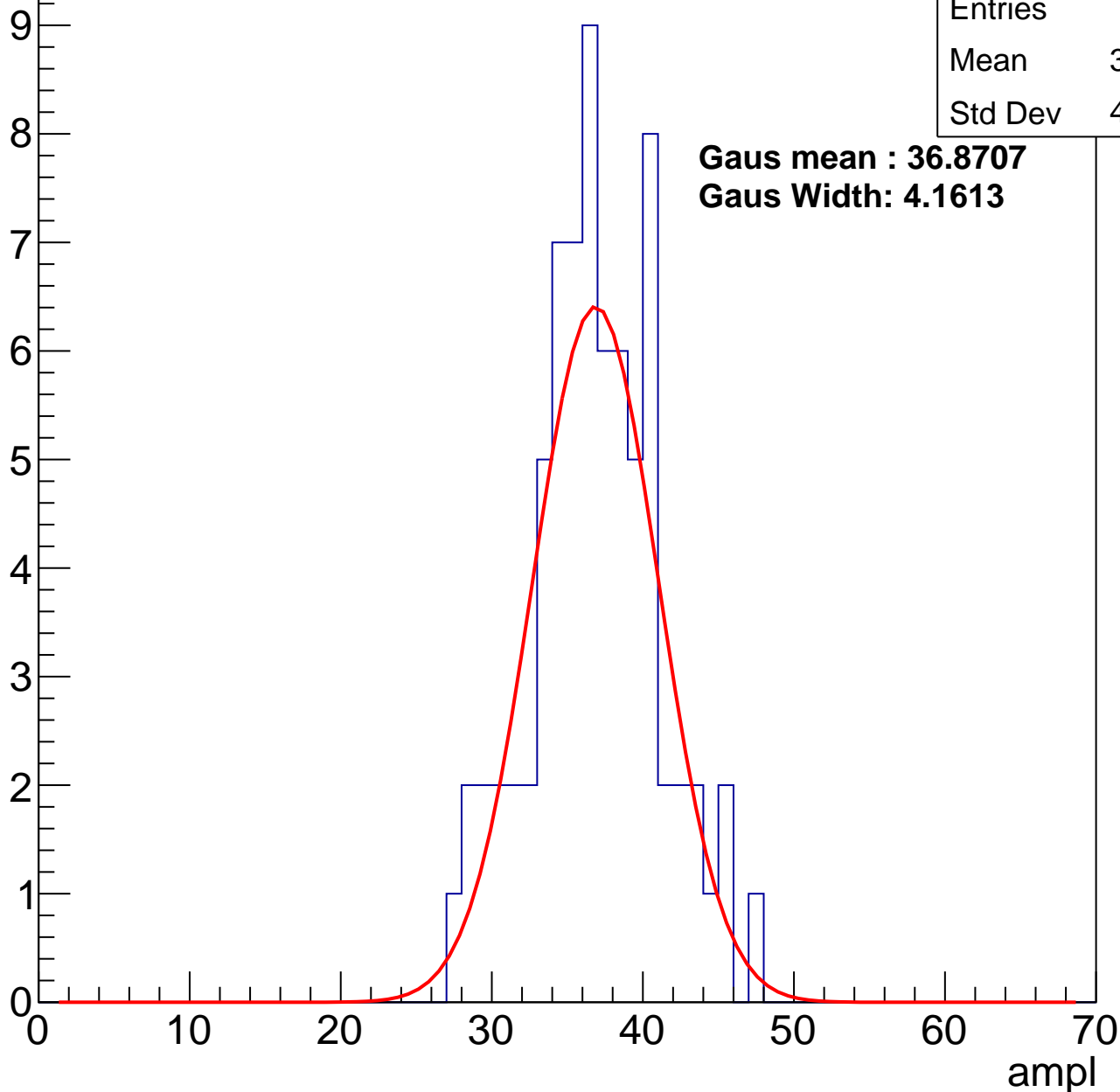
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	36.45
Std Dev	4.185

**Gaus mean : 36.8707**

**Gaus Width: 4.1613**



# B1L103S, U16-ch24, adc2

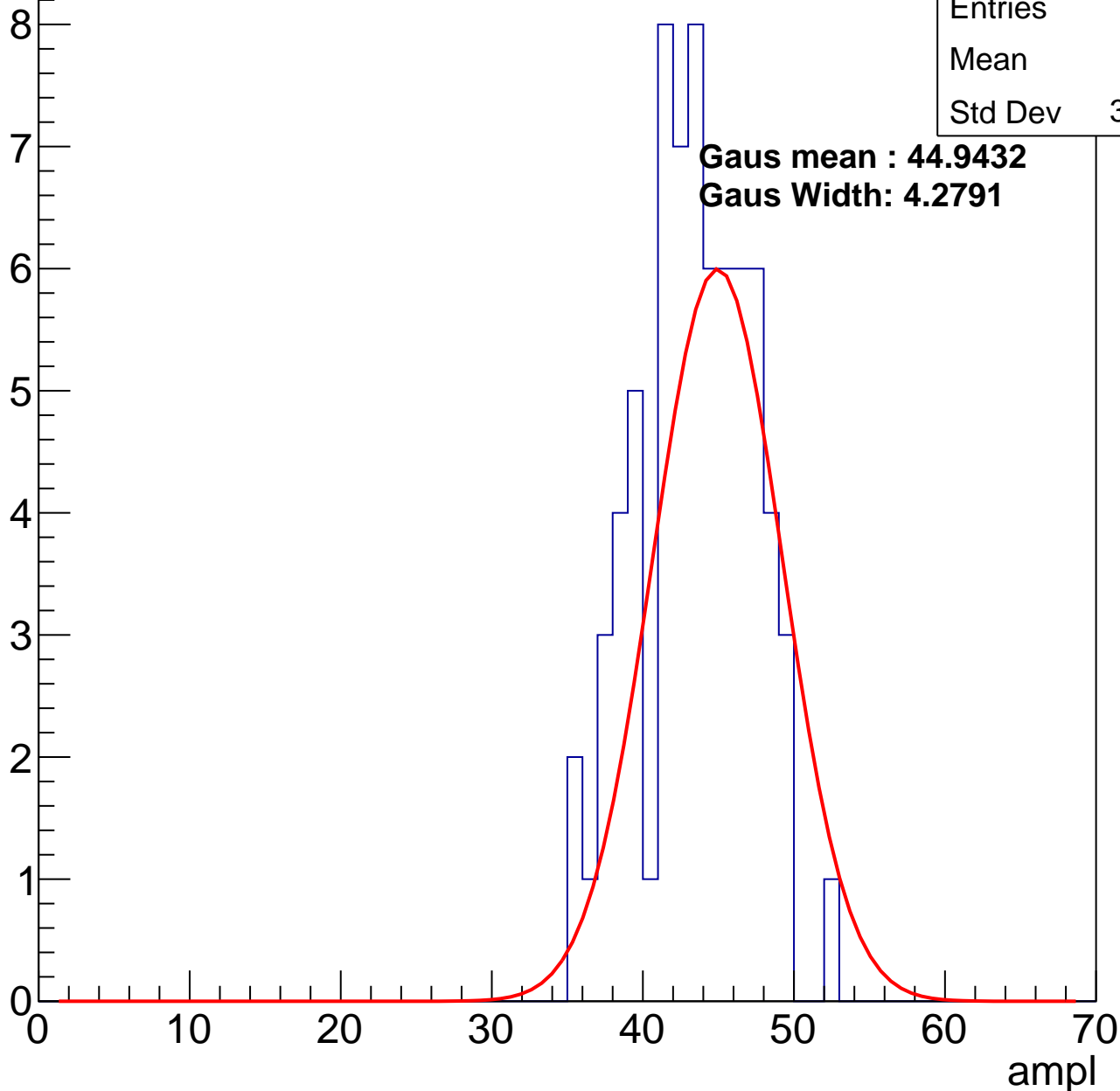
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	43
Std Dev	3.719

**Gaus mean : 44.9432**

**Gaus Width: 4.2791**

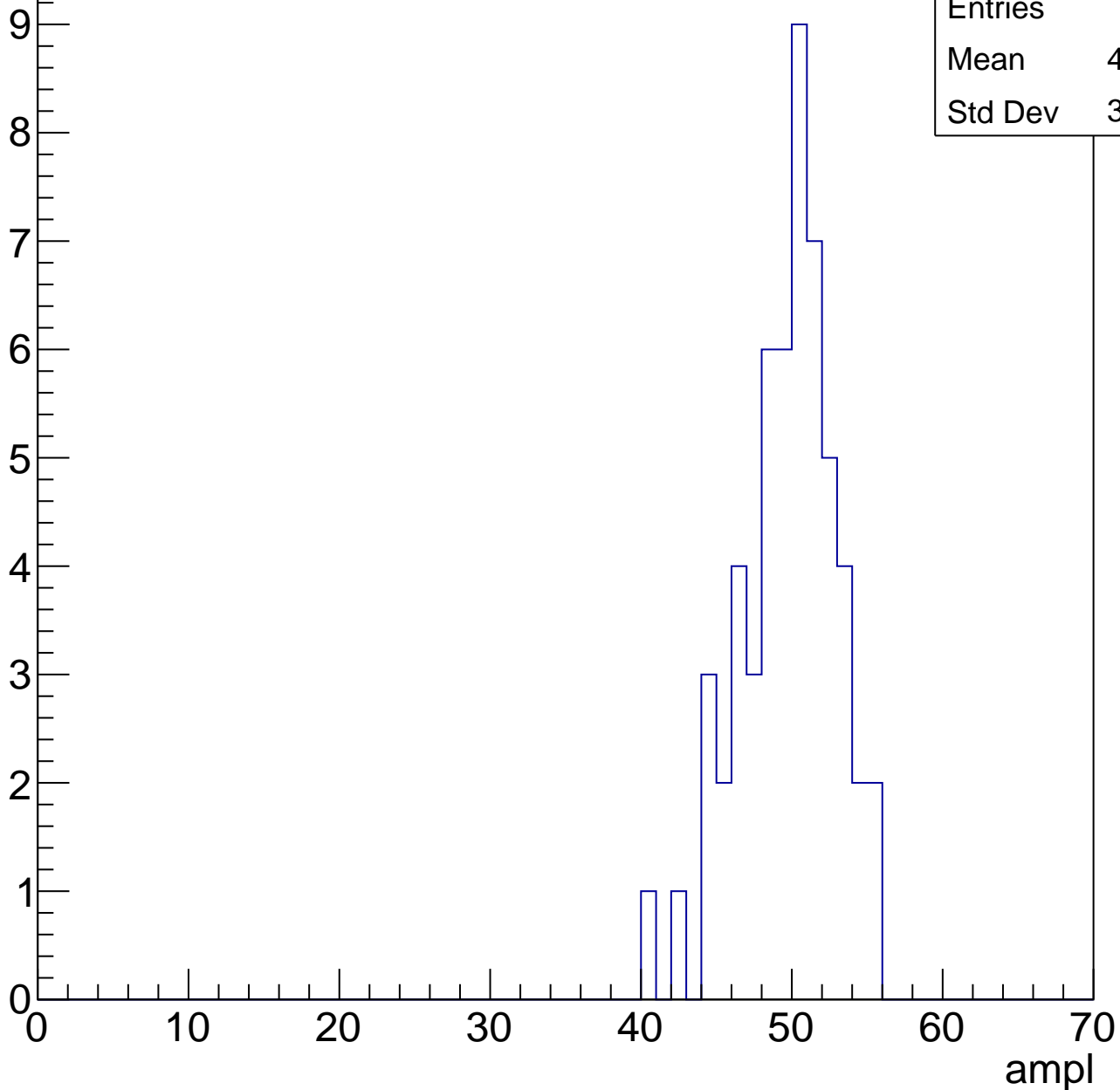


# B1L103S, U16-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	49.24
Std Dev	3.179

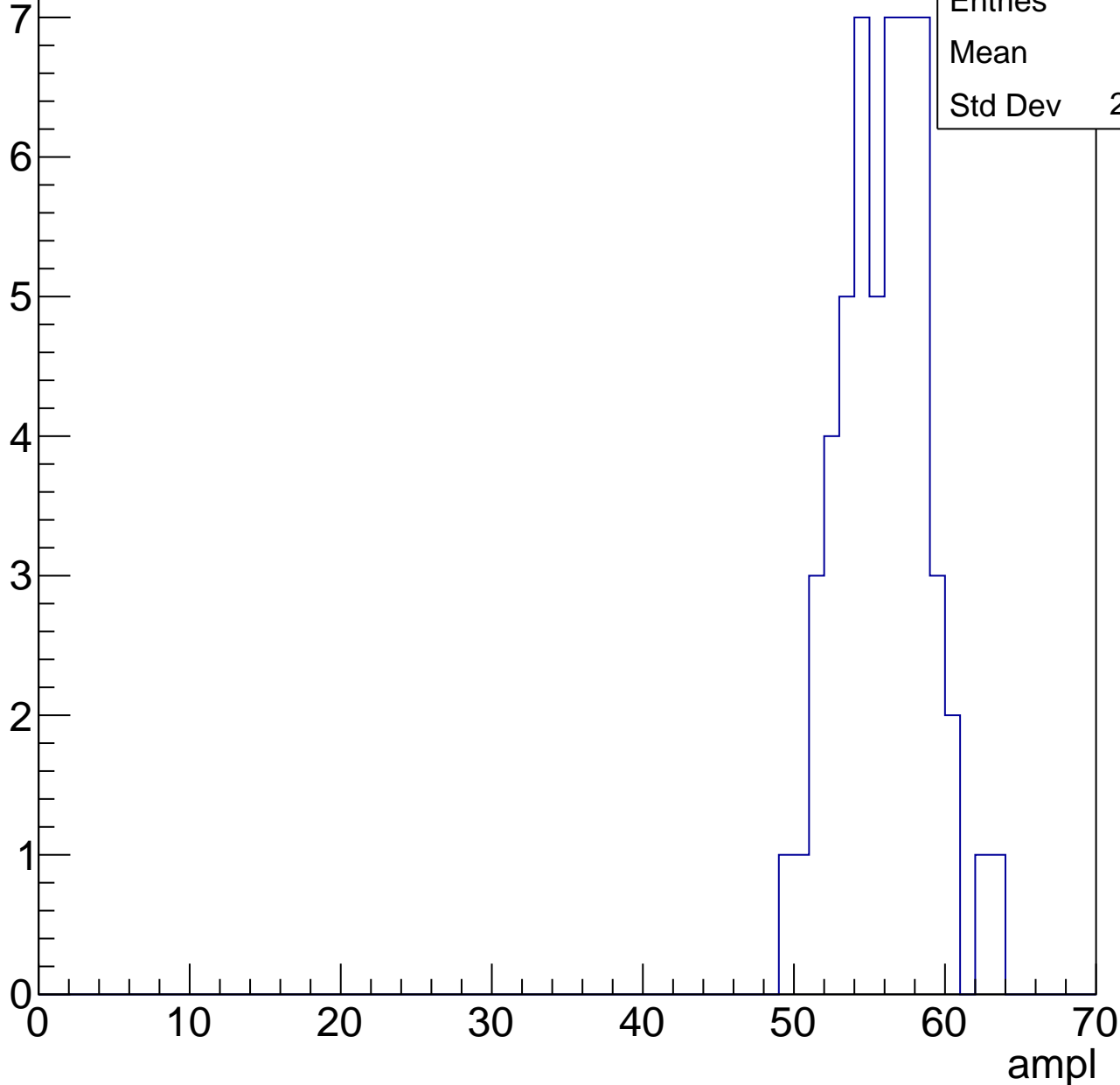


# B1L103S, U16-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	55.5
Std Dev	2.942

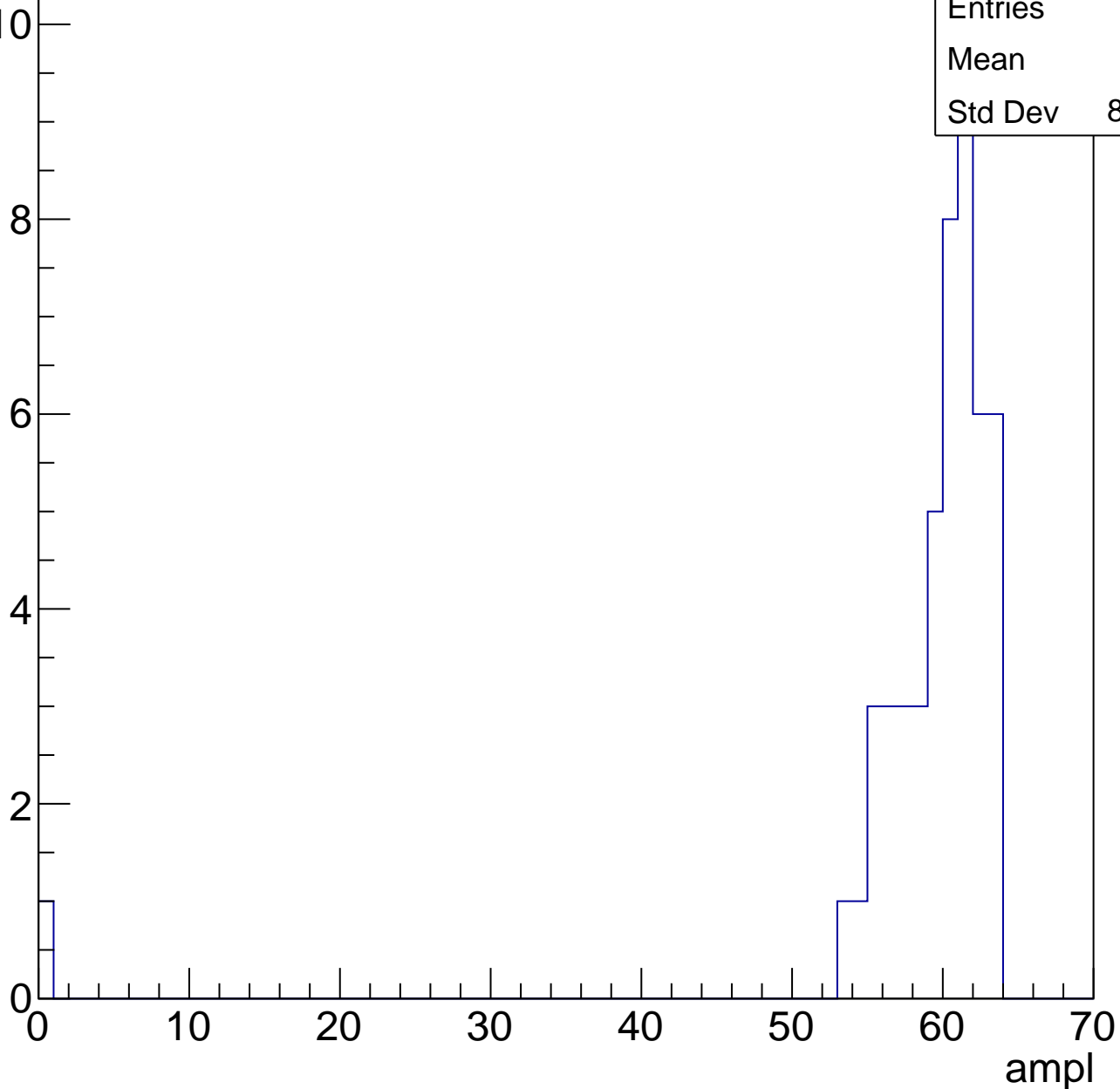


# B1L103S, U16-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

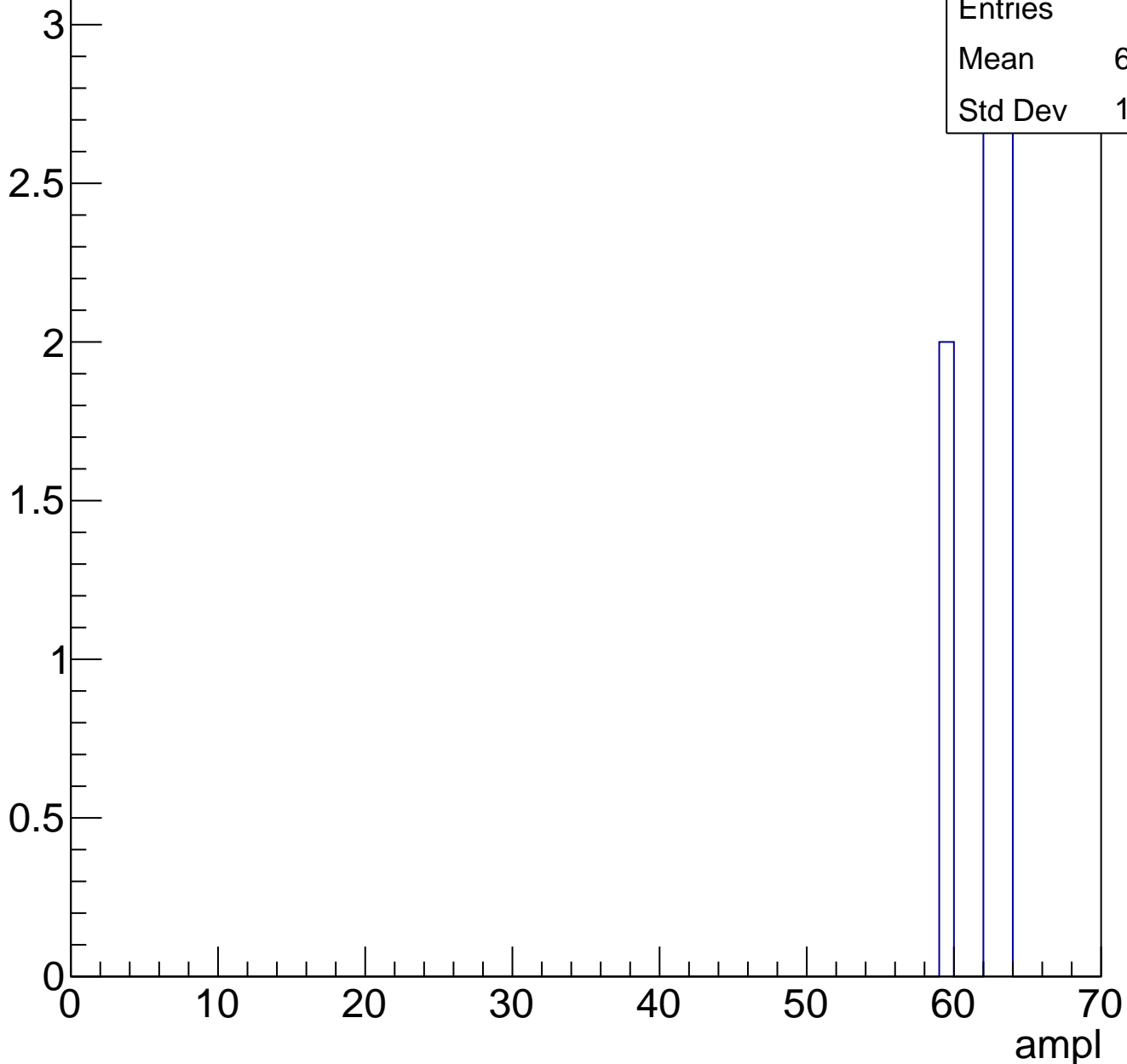
Entries	50
Mean	58.4
Std Dev	8.732



# B1L103S, U16-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

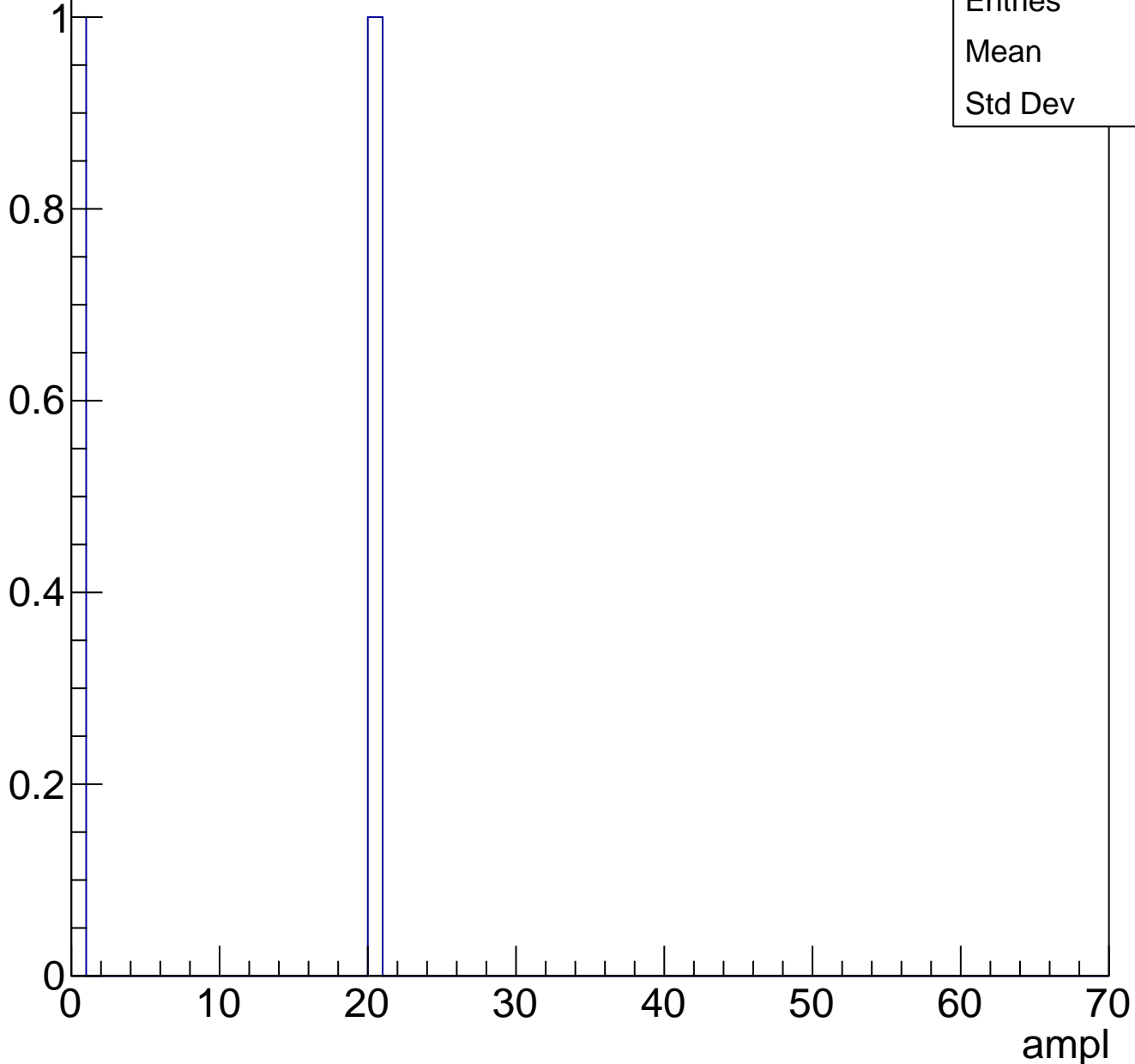




# B1L103S, U16-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	10
Std Dev	10

# B1L103S, U16-ch25, adc0

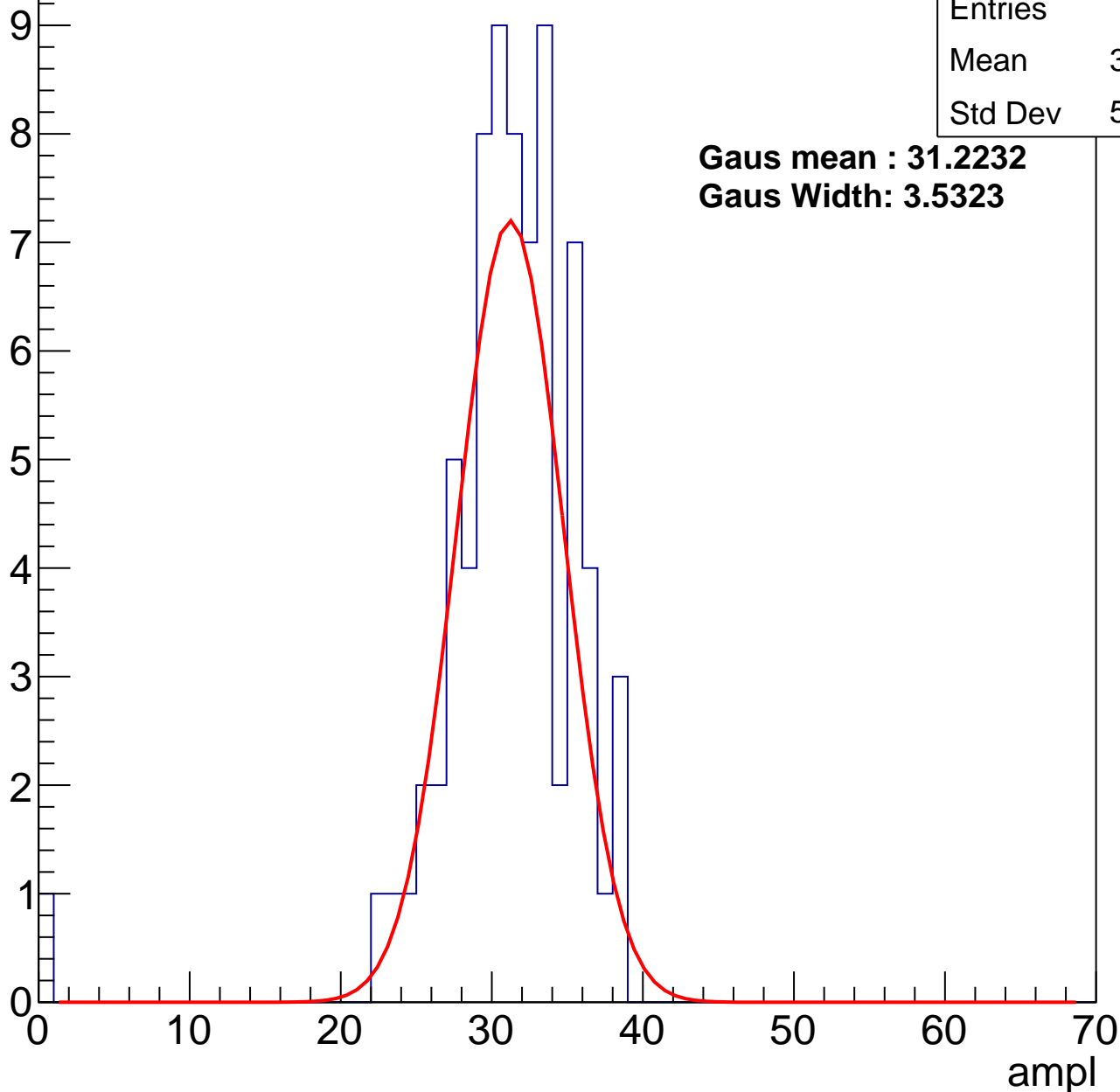
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	30.63
Std Dev	5.006

**Gaus mean : 31.2232**

**Gaus Width: 3.5323**



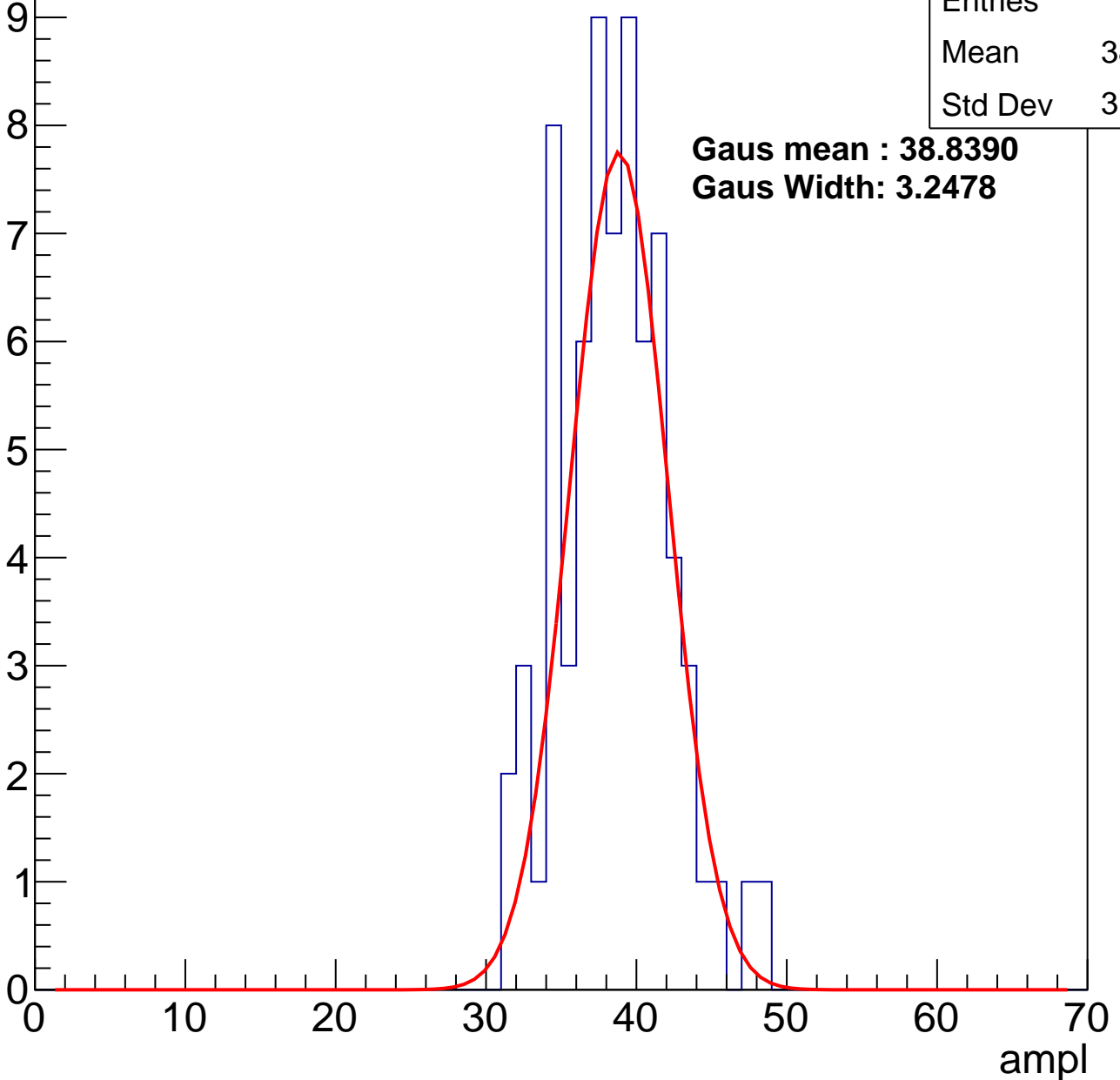
# B1L103S, U16-ch25, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

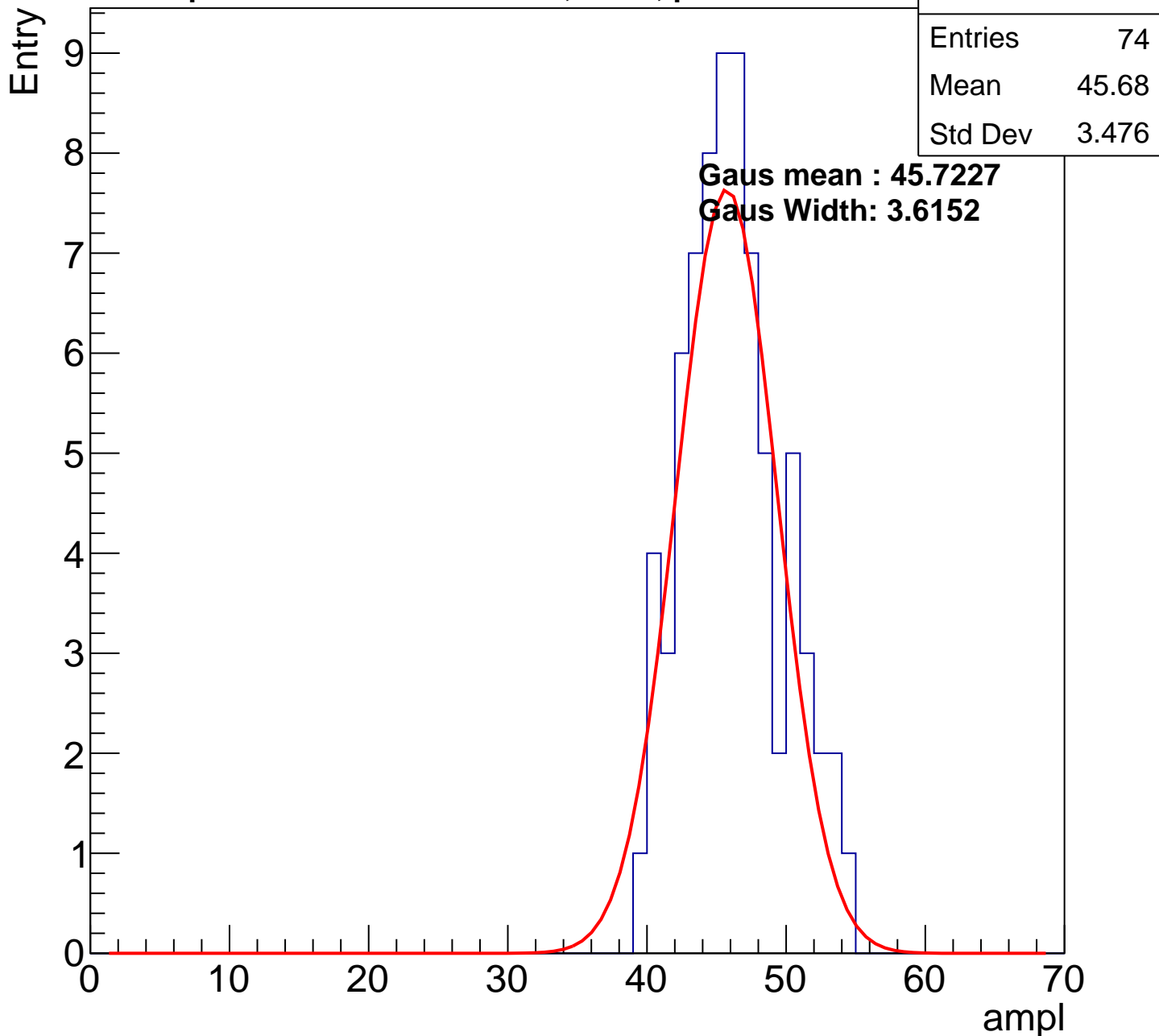
Entries	72
Mean	38.08
Std Dev	3.574

**Gaus mean : 38.8390**  
**Gaus Width: 3.2478**



# B1L103S, U16-ch25, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

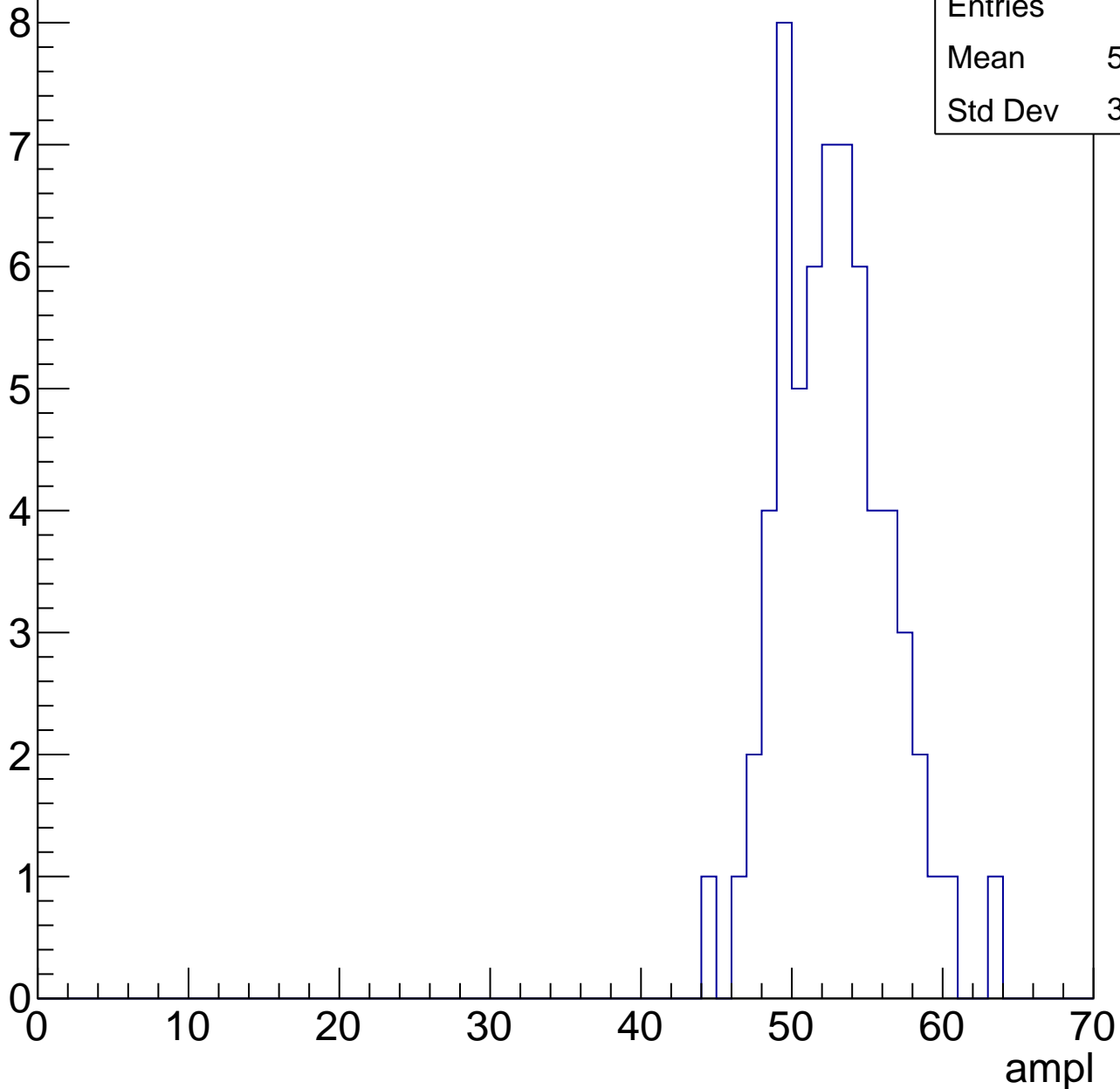


# B1L103S, U16-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	52.32
Std Dev	3.603

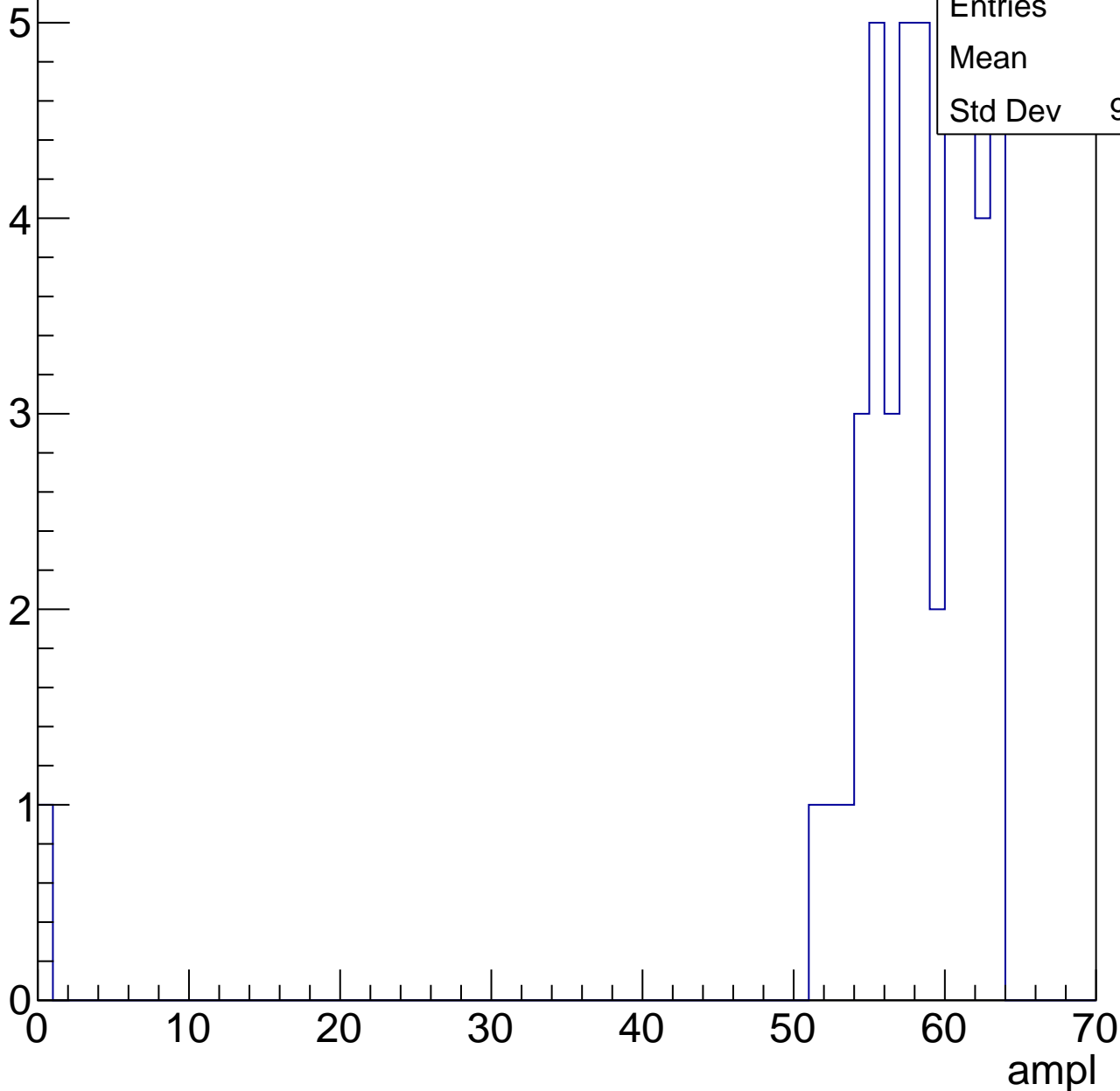


# B1L103S, U16-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	57
Std Dev	9.082



# B1L103S, U16-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

7

6

5

4

3

2

1

0

Entries

34

Mean

59.71

Std Dev

2.19

0

ampl

0

10

20

30

40

50

60

70

# B1L103S, U16-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U16-ch26, adc0

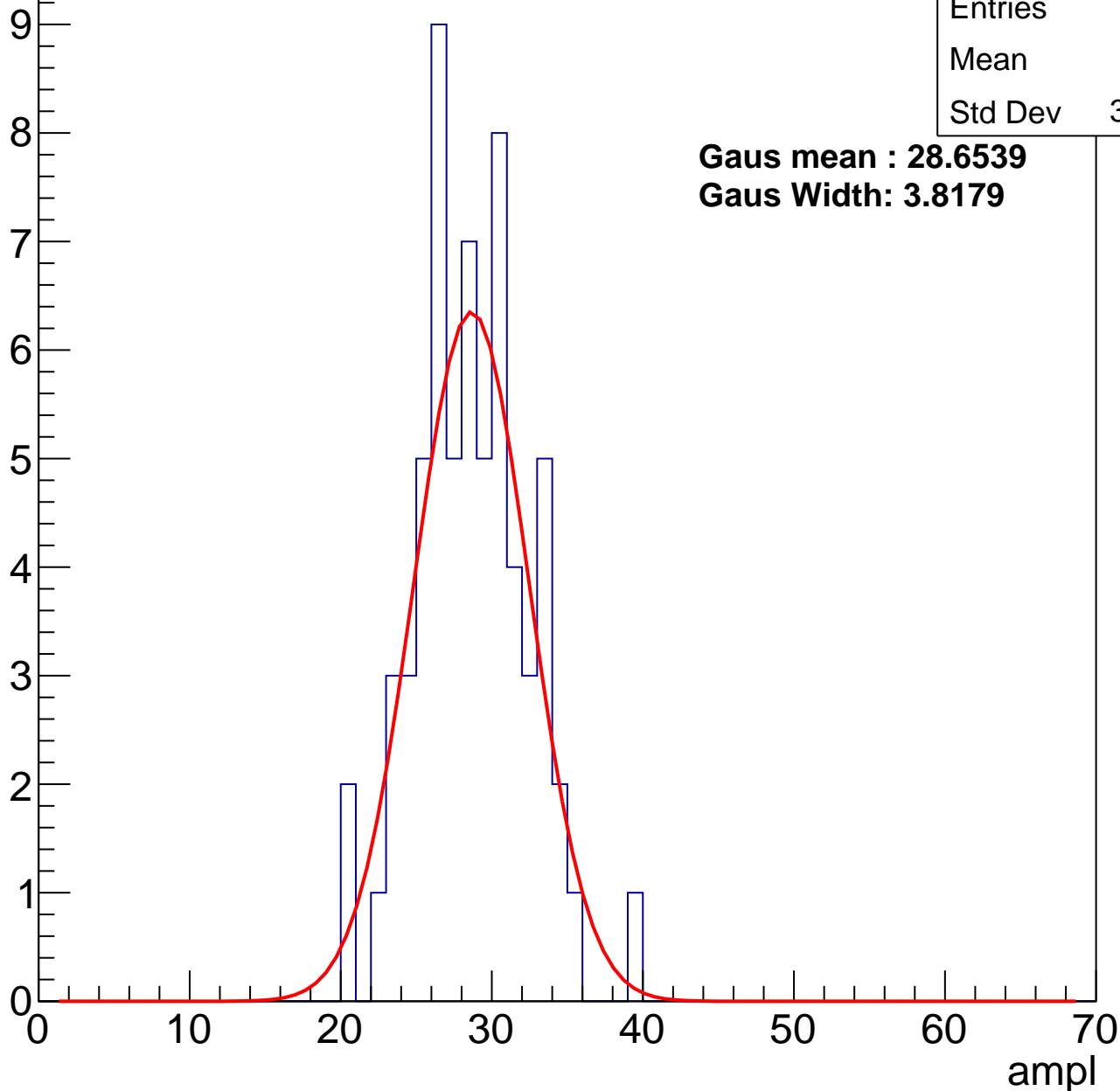
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	28.2
Std Dev	3.662

**Gaus mean : 28.6539**

**Gaus Width: 3.8179**



# B1L103S, U16-ch26, adc1

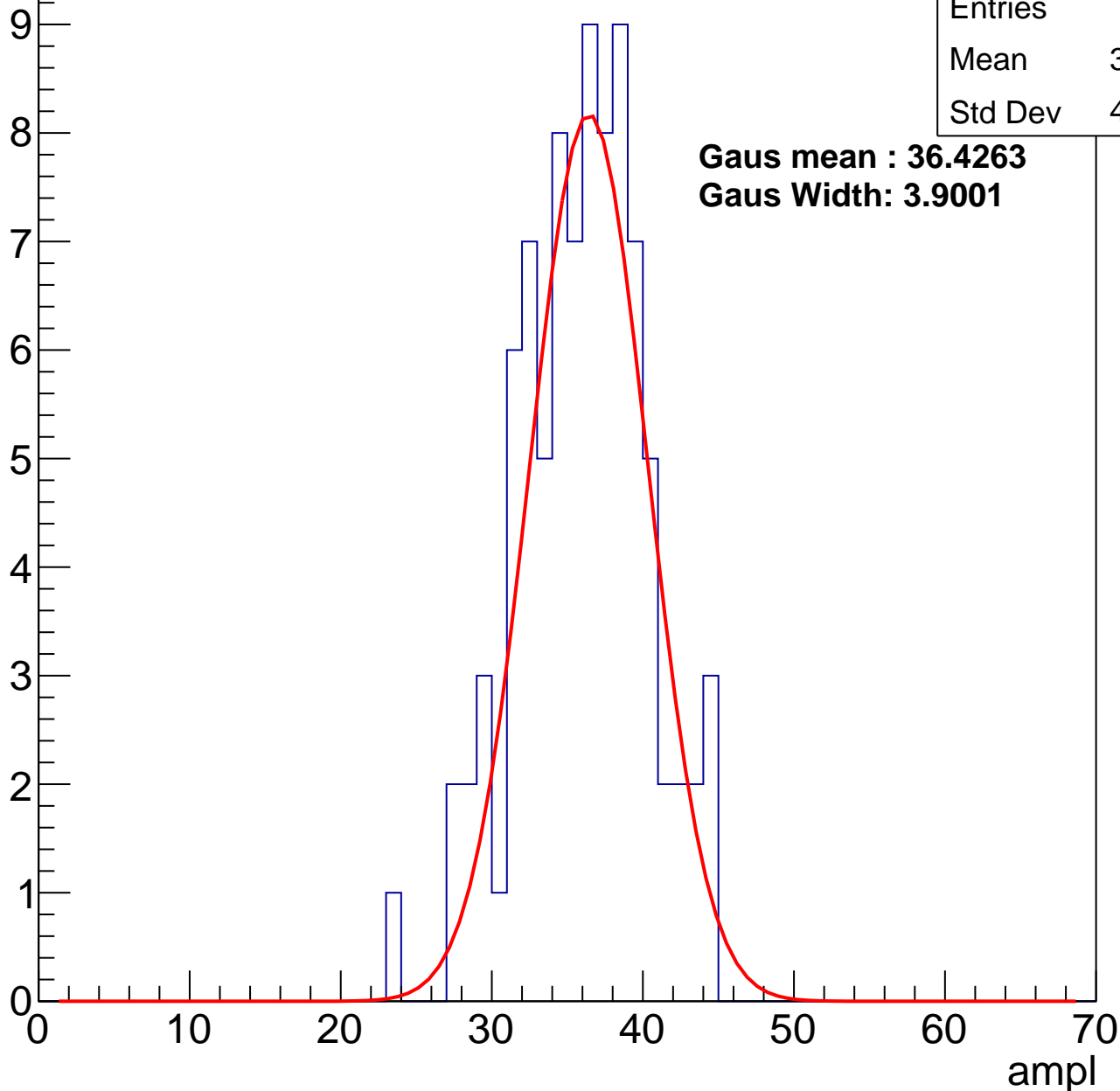
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	89
Mean	35.52
Std Dev	4.195

**Gaus mean : 36.4263**

**Gaus Width: 3.9001**



# B1L103S, U16-ch26, adc2

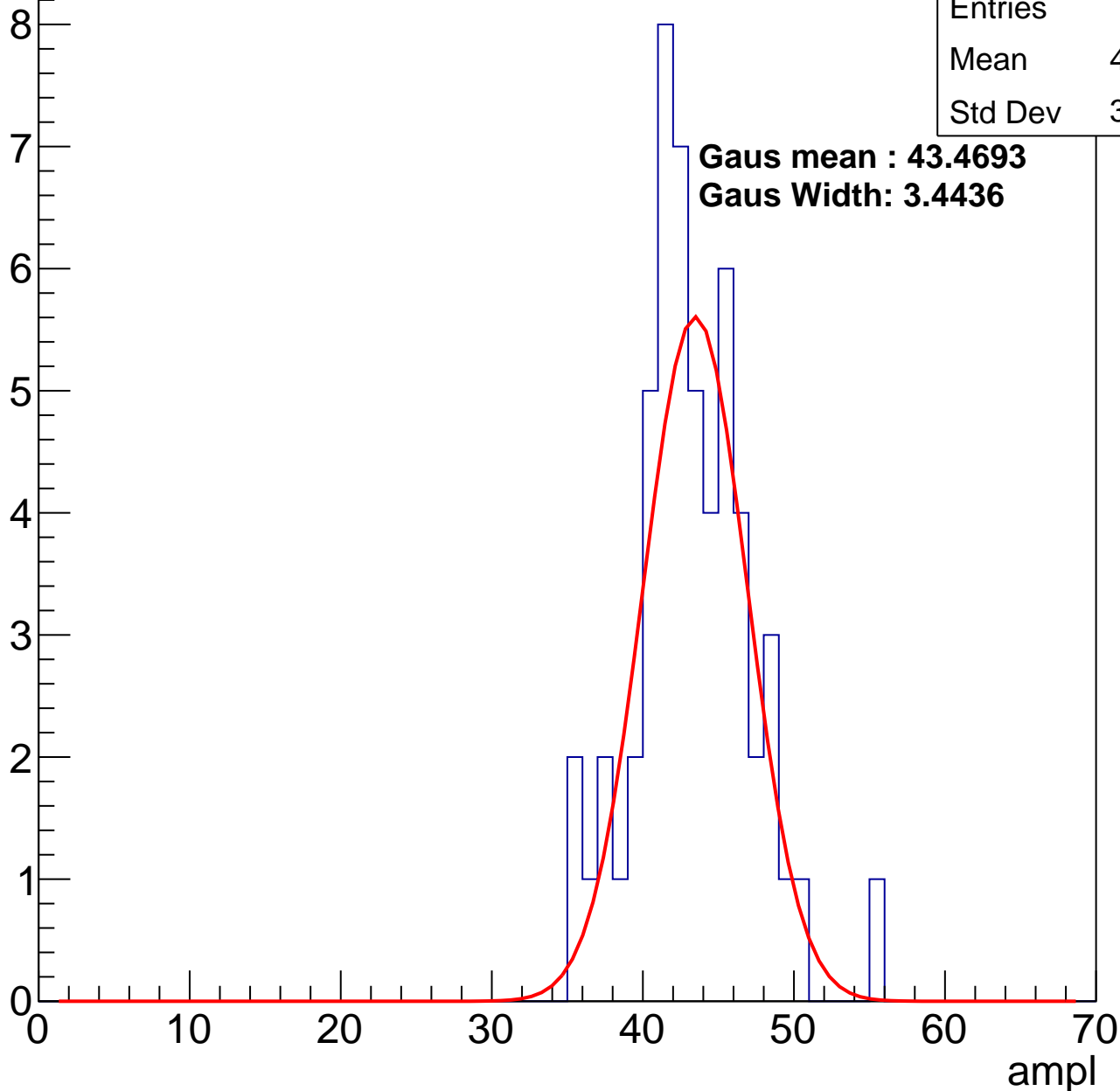
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	42.82
Std Dev	3.786

**Gaus mean : 43.4693**

**Gaus Width: 3.4436**

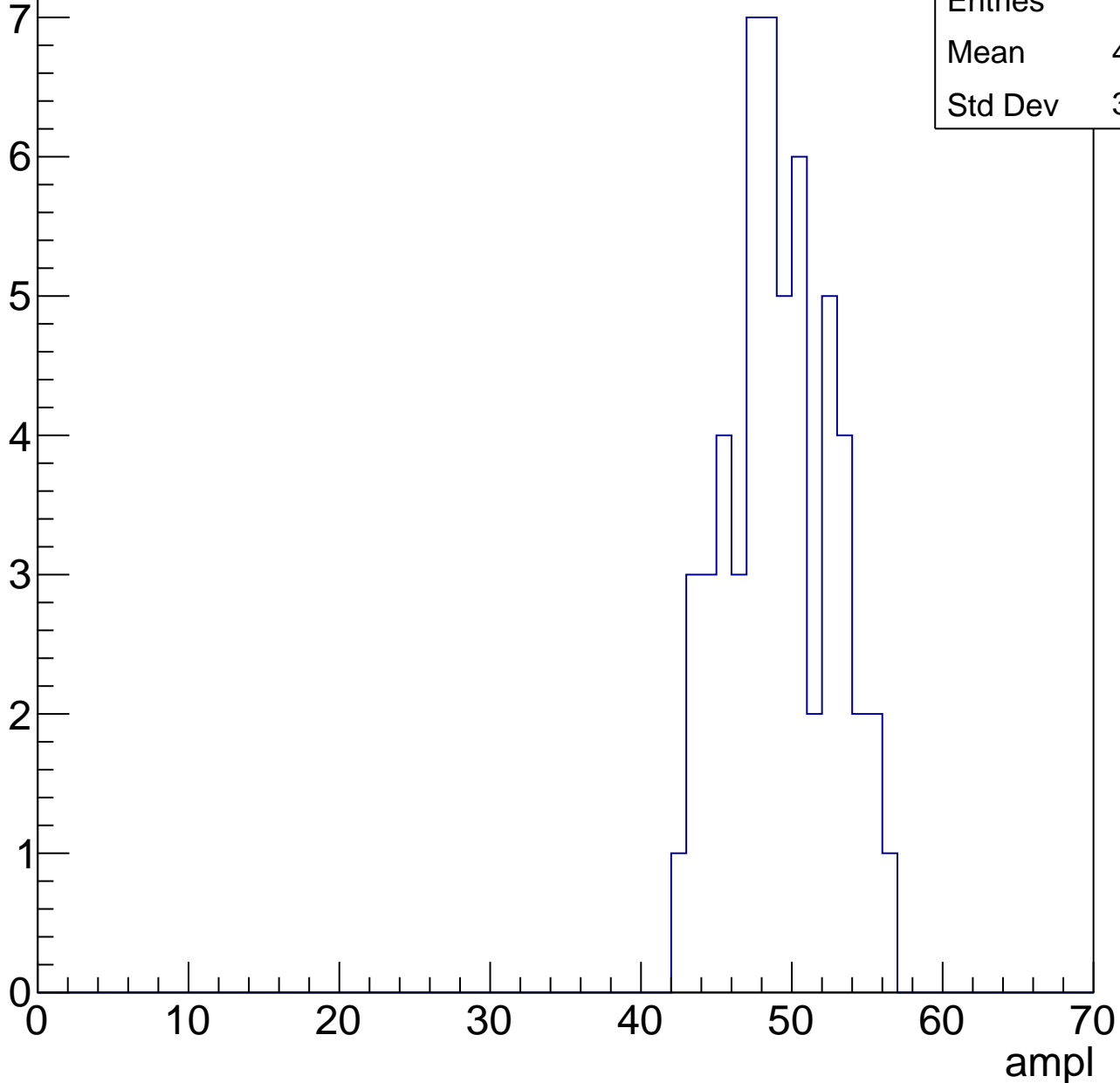


# B1L103S, U16-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	48.71
Std Dev	3.431

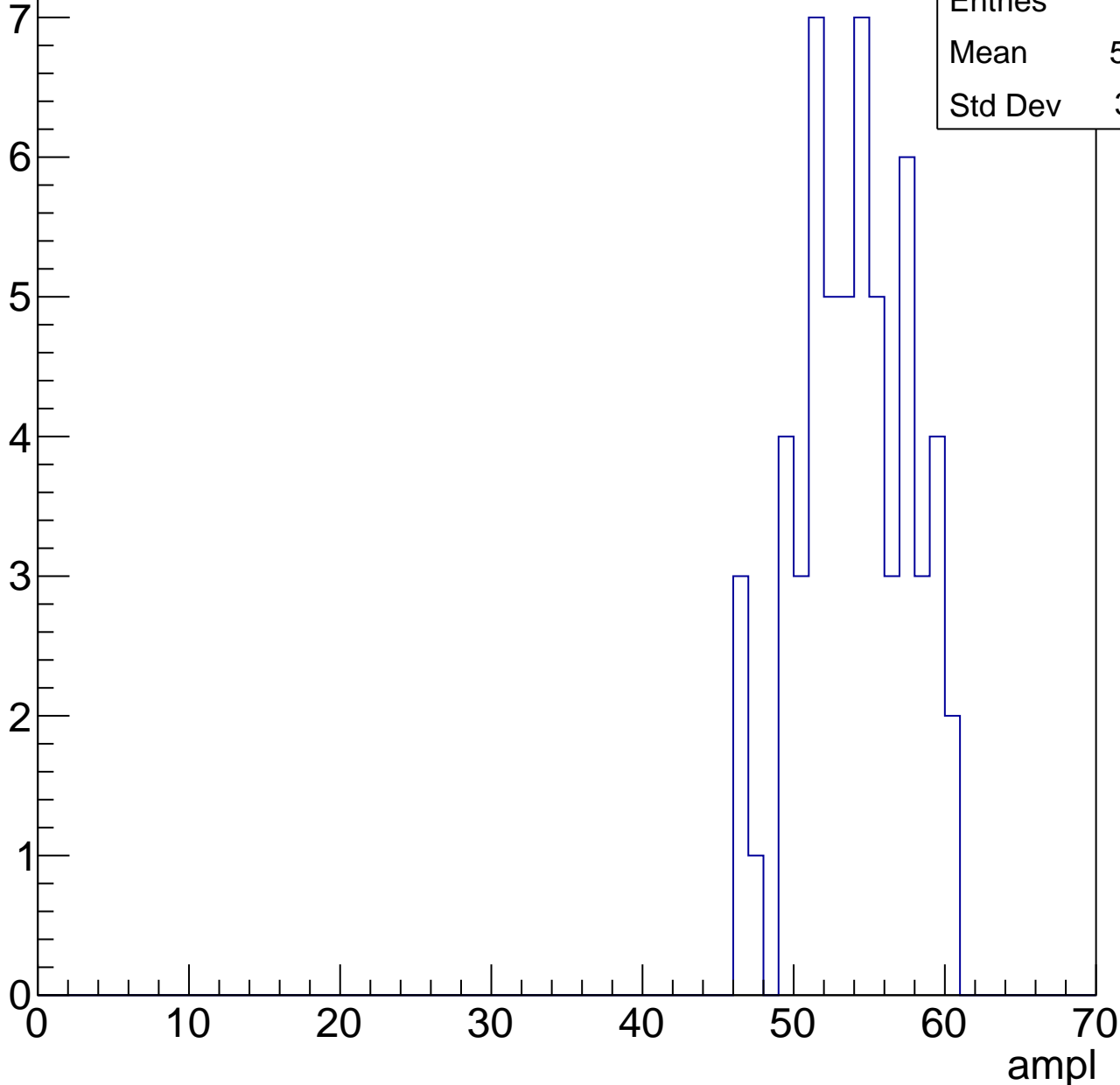


# B1L103S, U16-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	53.55
Std Dev	3.611

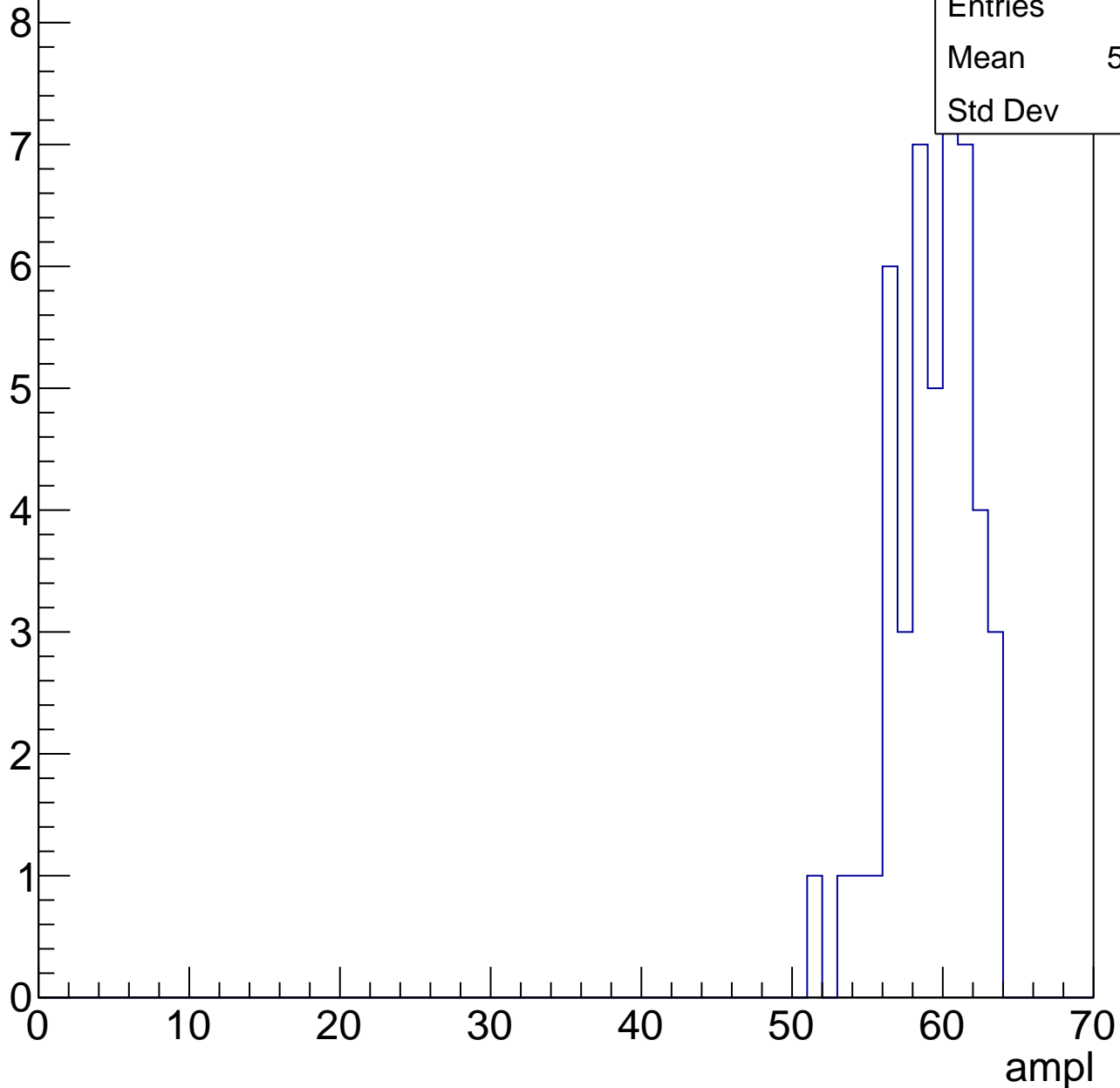


# B1L103S, U16-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	58.83
Std Dev	2.66

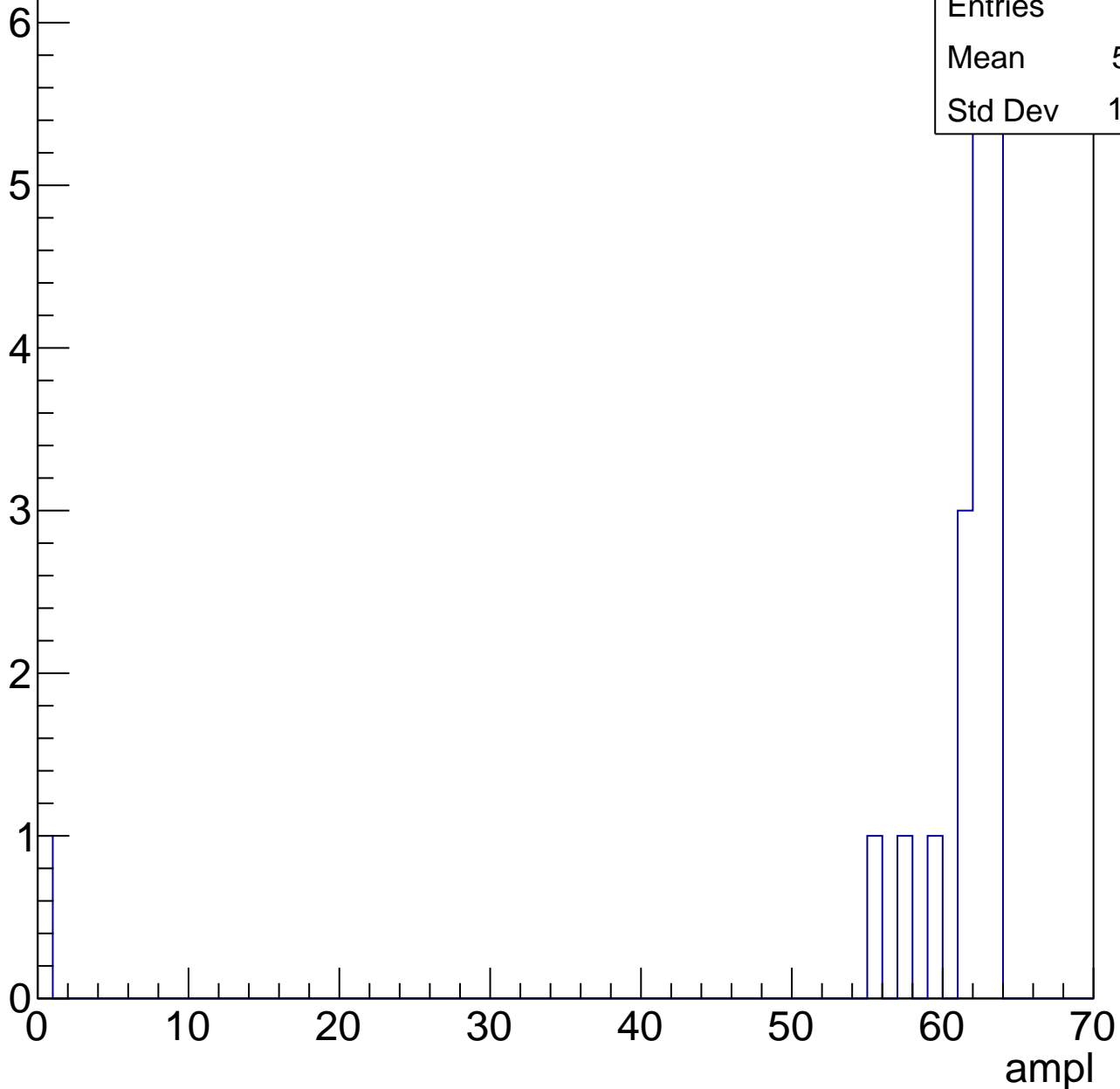


# B1L103S, U16-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	19
Mean	58.11
Std Dev	13.86





# B1L103S, U16-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	63
Std Dev	0

# B1L103S, U16-ch27, adc0

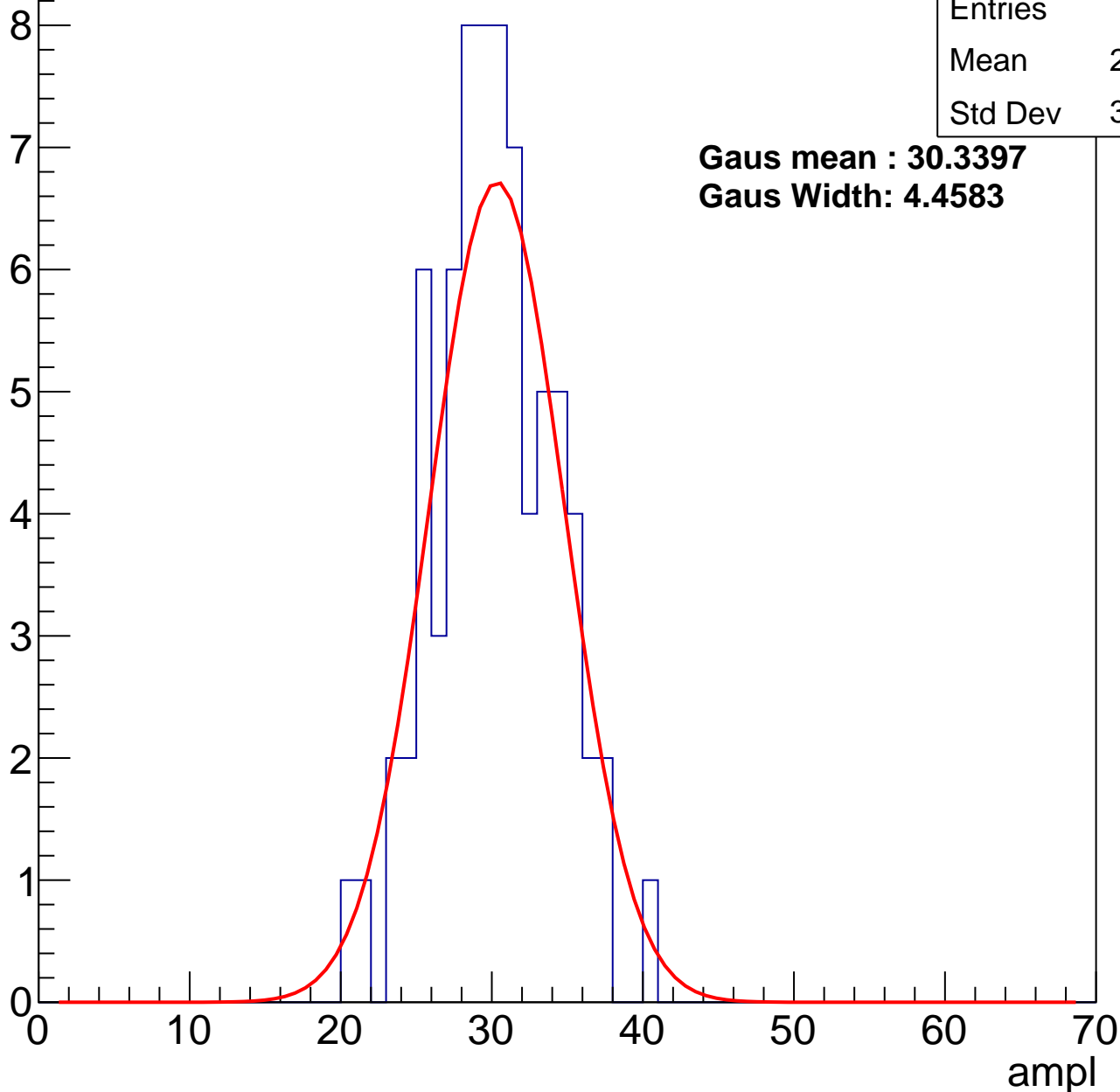
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	29.69
Std Dev	3.922

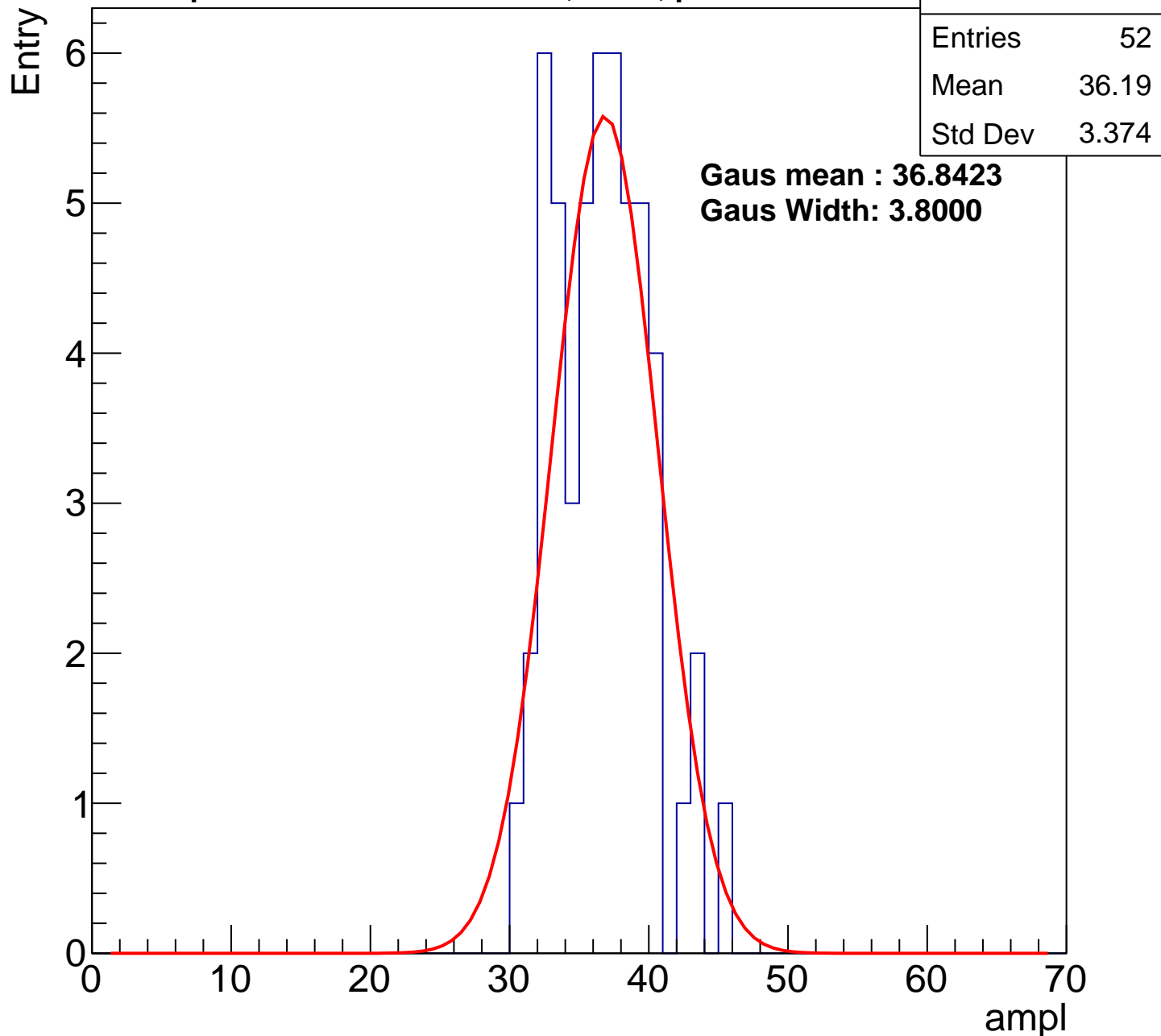
**Gaus mean : 30.3397**

**Gaus Width: 4.4583**



# B1L103S, U16-ch27, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U16-ch27, adc2

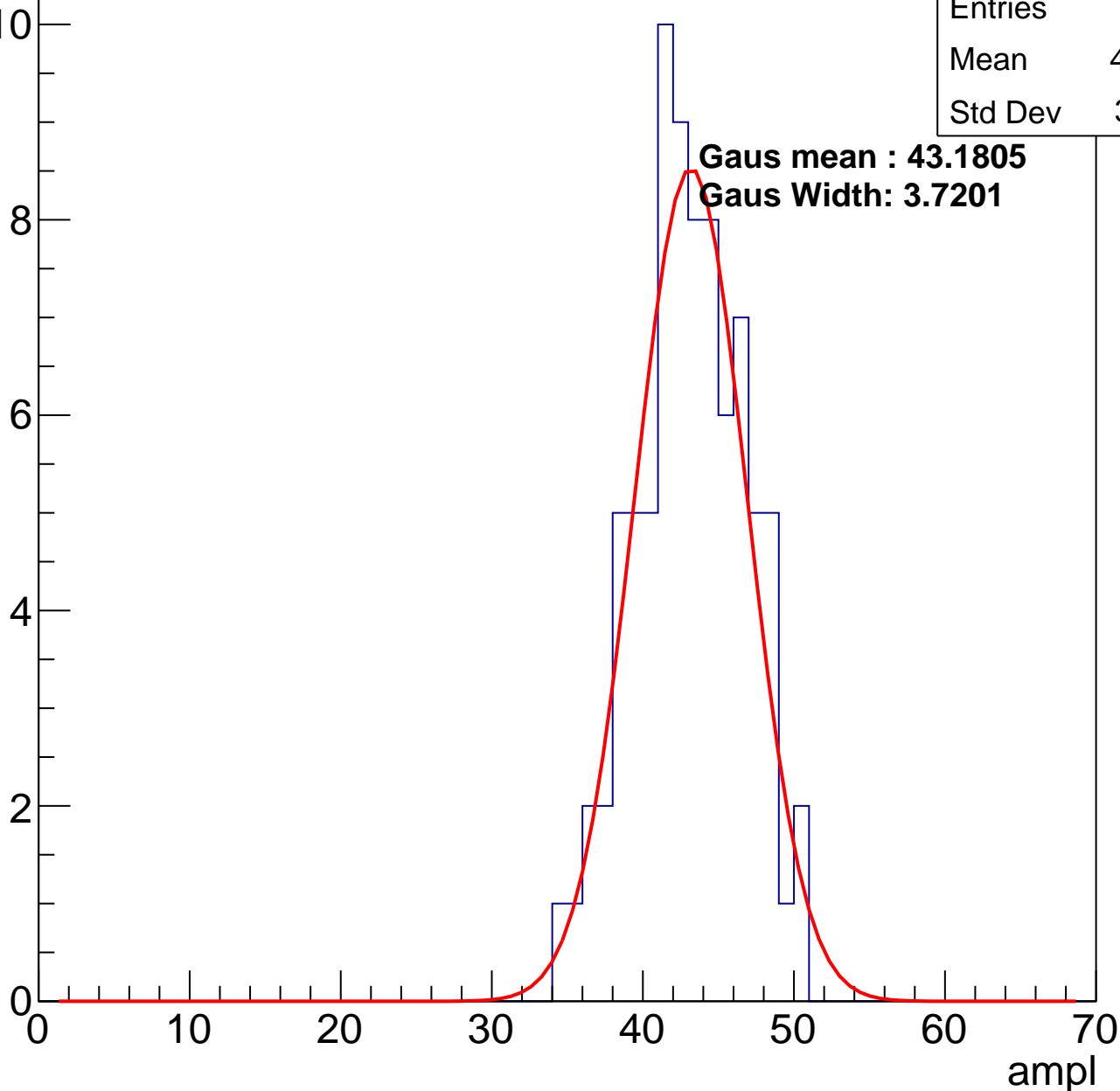
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	82
Mean	42.68
Std Dev	3.561

**Gaus mean : 43.1805**

**Gaus Width: 3.7201**

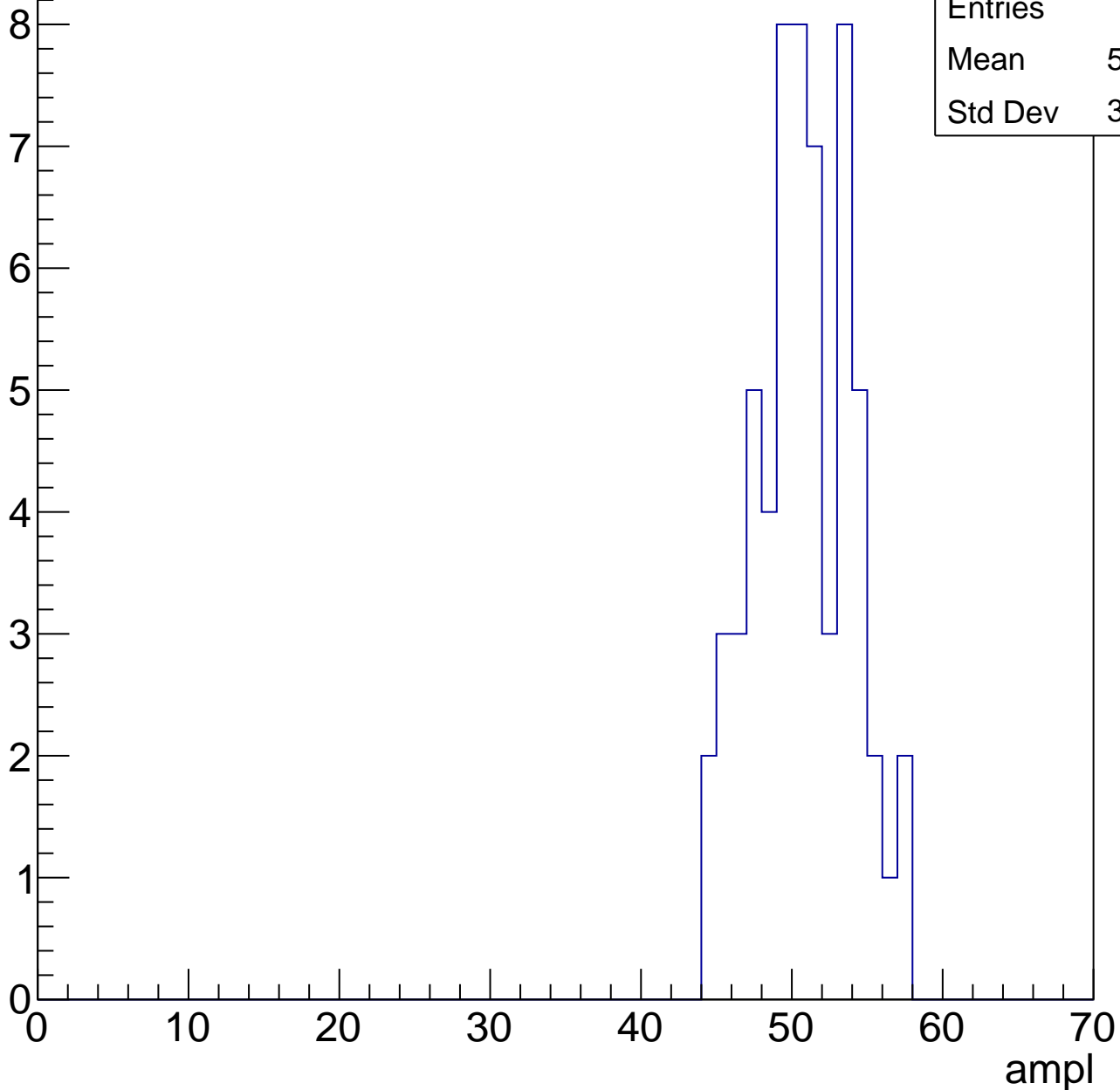


# B1L103S, U16-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	50.28
Std Dev	3.173

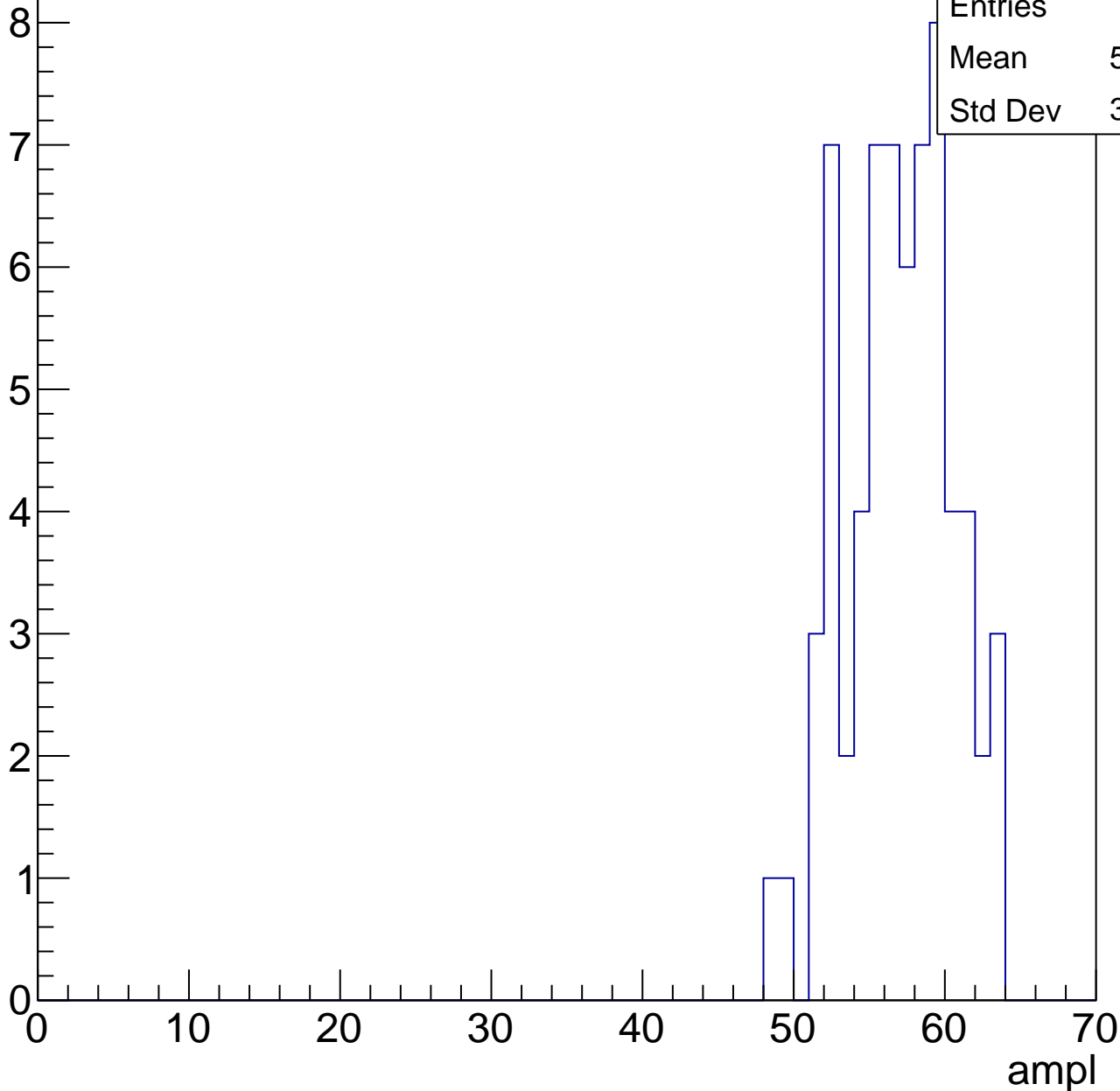


# B1L103S, U16-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	56.52
Std Dev	3.509

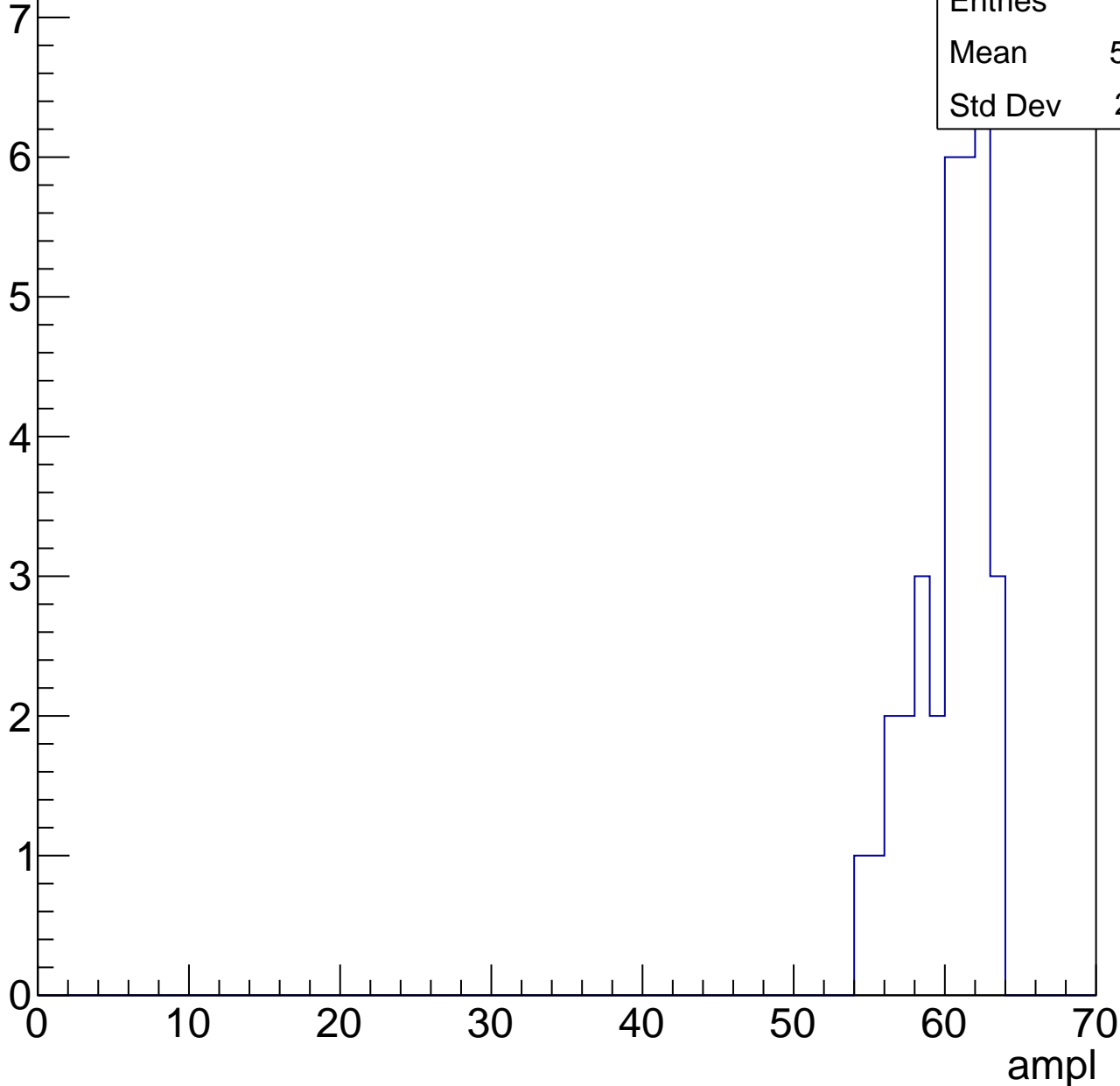


# B1L103S, U16-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

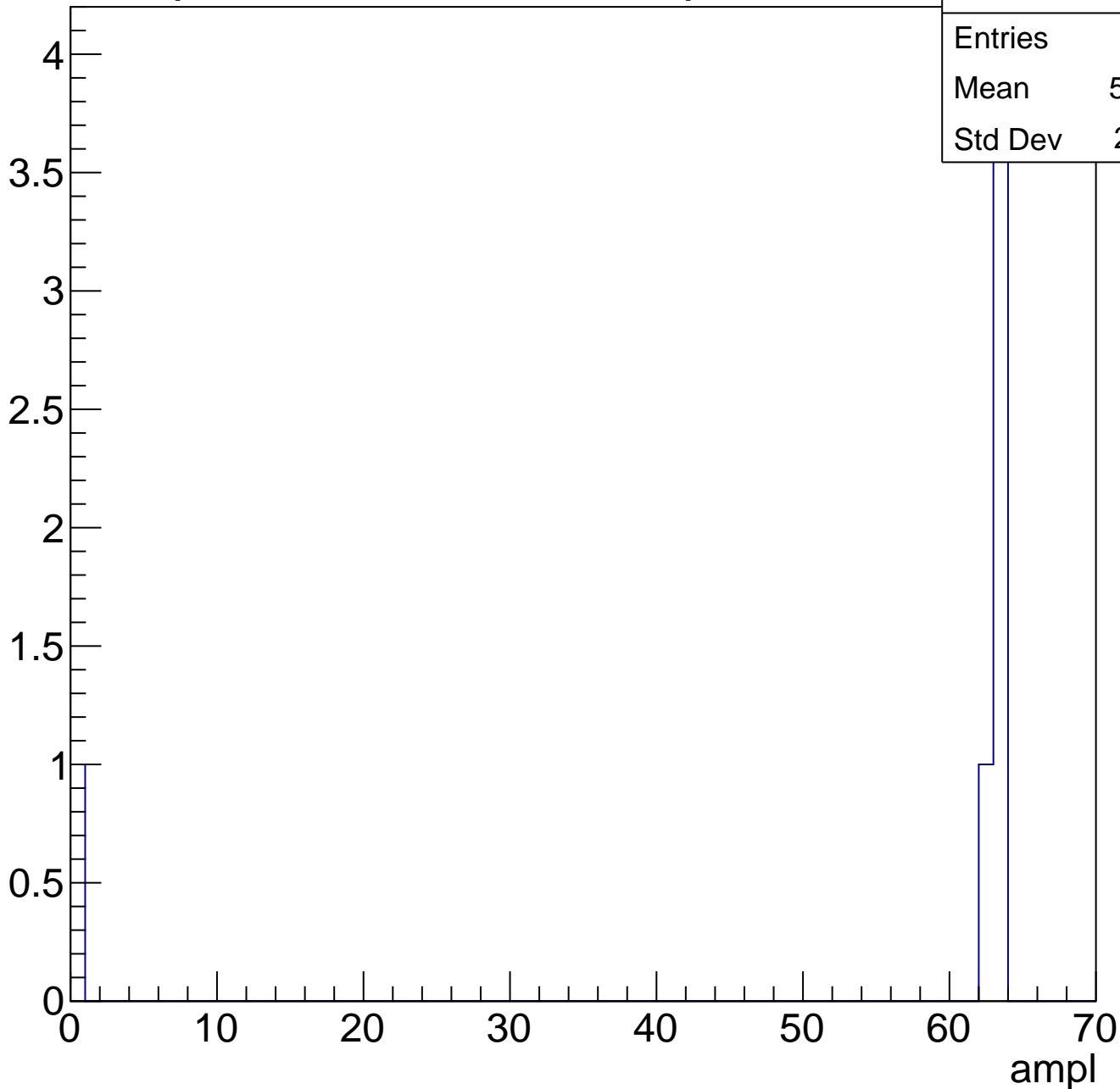
Entries	33
Mean	59.88
Std Dev	2.371



# B1L103S, U16-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U16-ch28, adc0

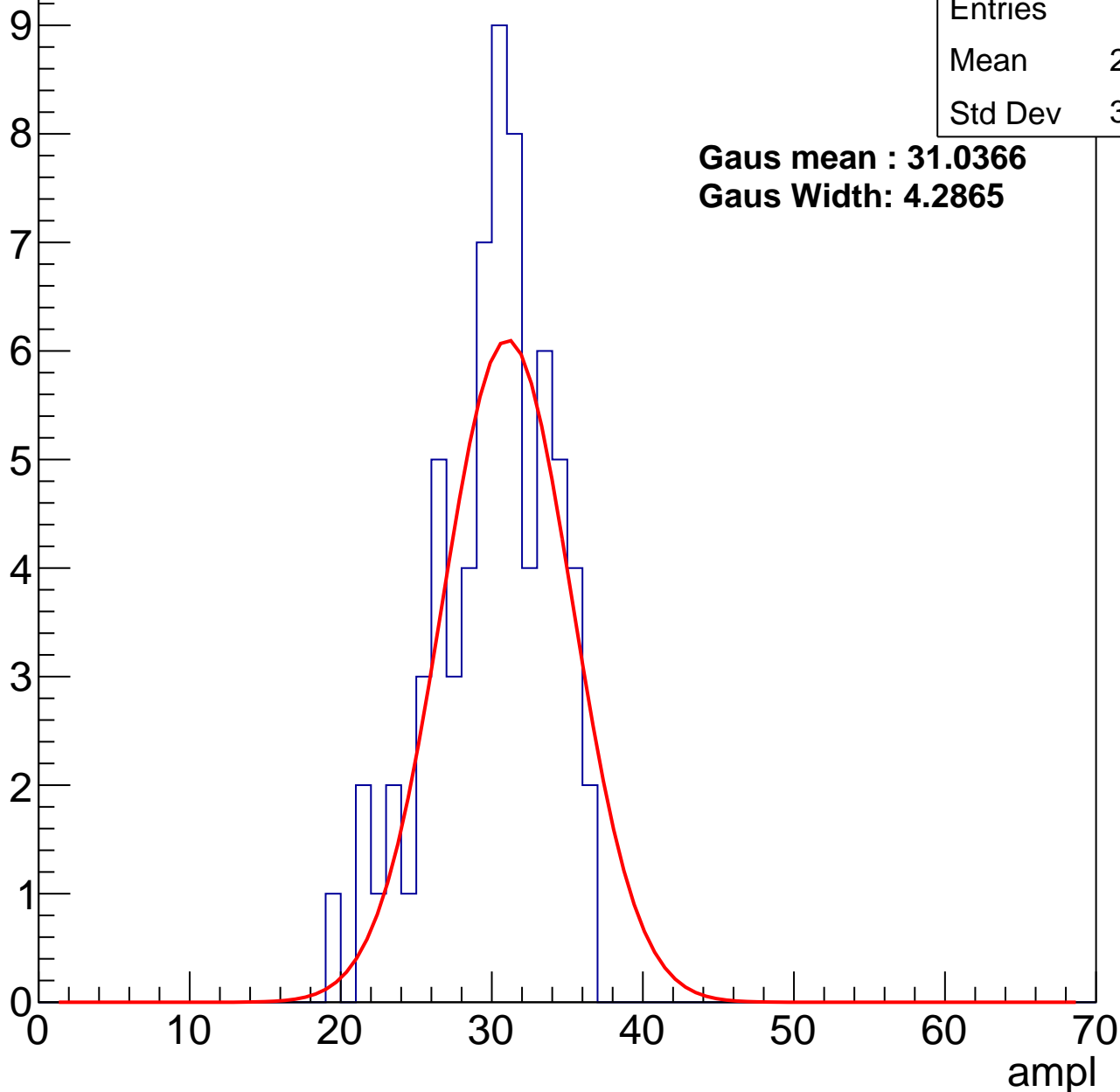
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	29.55
Std Dev	3.868

**Gaus mean : 31.0366**

**Gaus Width: 4.2865**



# B1L103S, U16-ch28, adc1

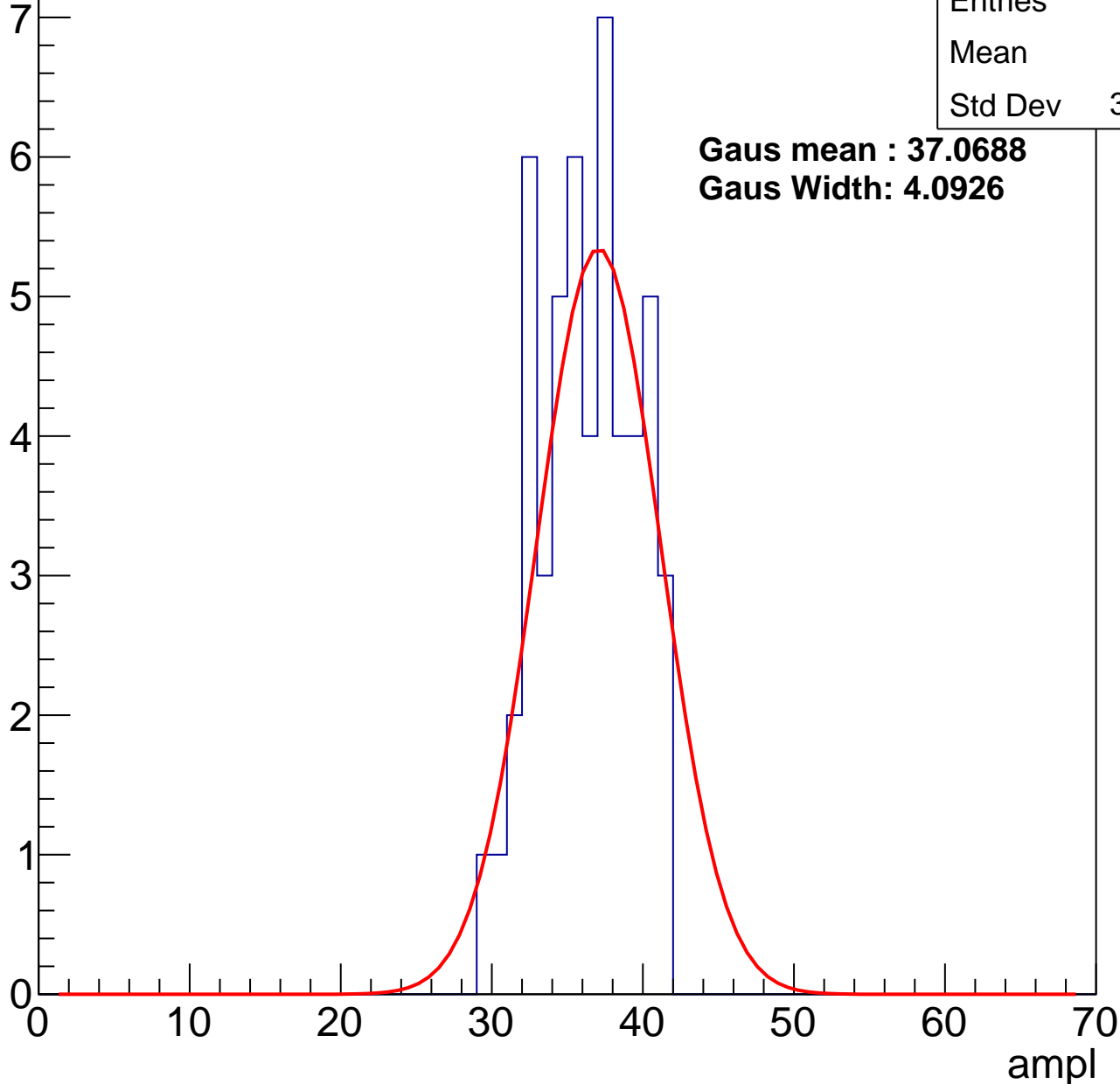
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	35.8
Std Dev	3.119

**Gaus mean : 37.0688**

**Gaus Width: 4.0926**



# B1L103S, U16-ch28, adc2

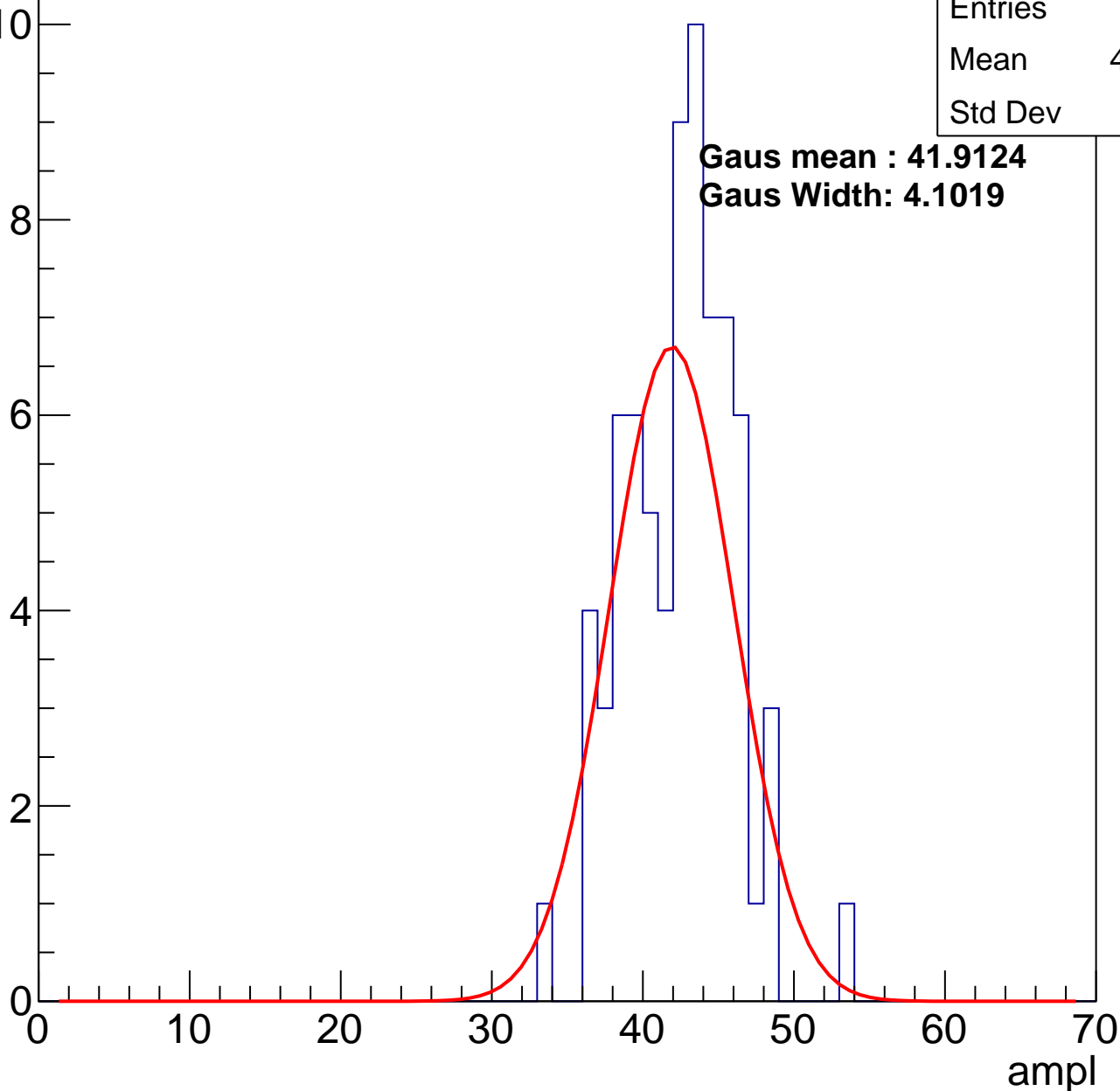
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	41.99
Std Dev	3.56

**Gaus mean : 41.9124**

**Gaus Width: 4.1019**

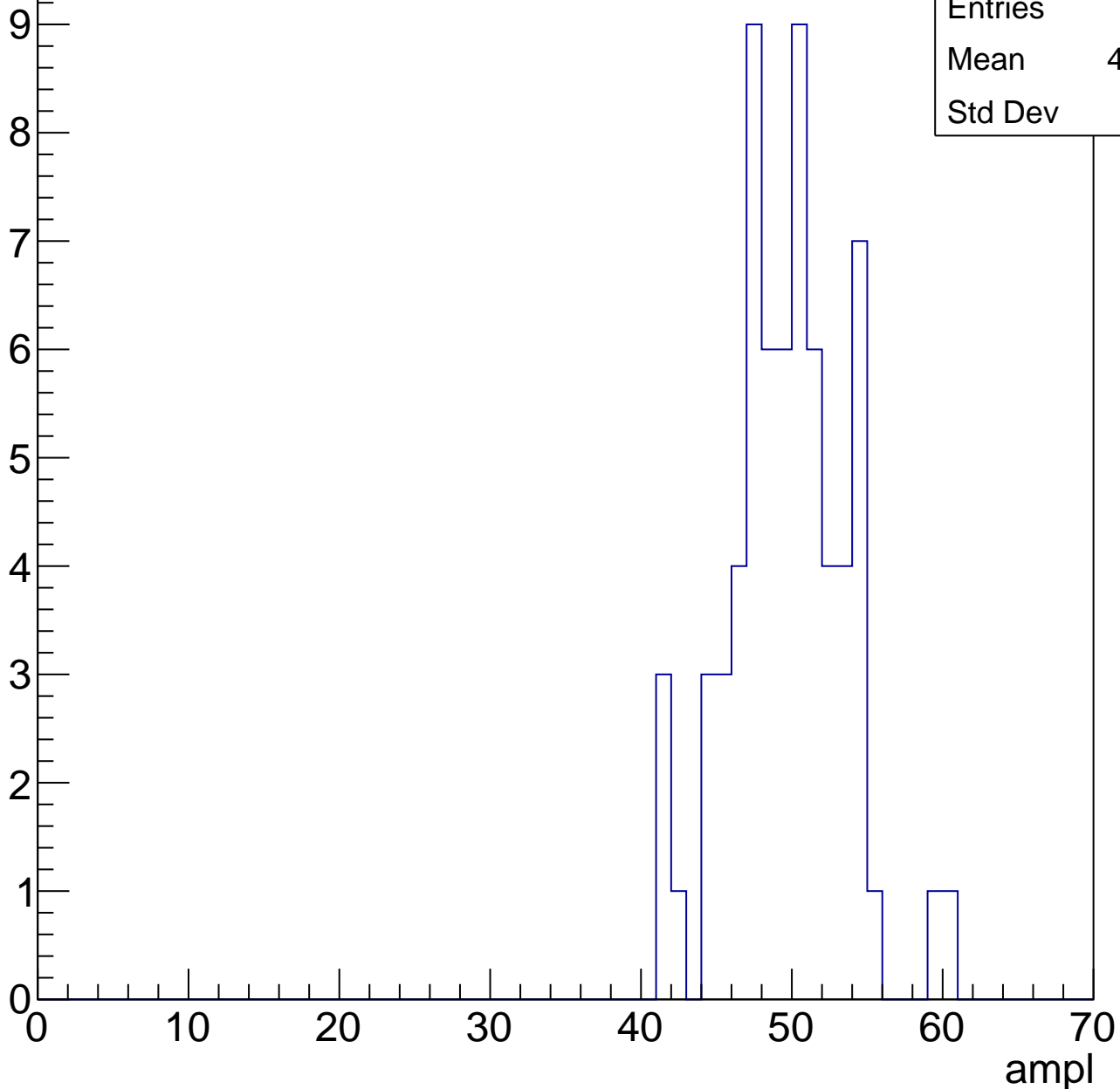


# B1L103S, U16-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	49.25
Std Dev	3.84

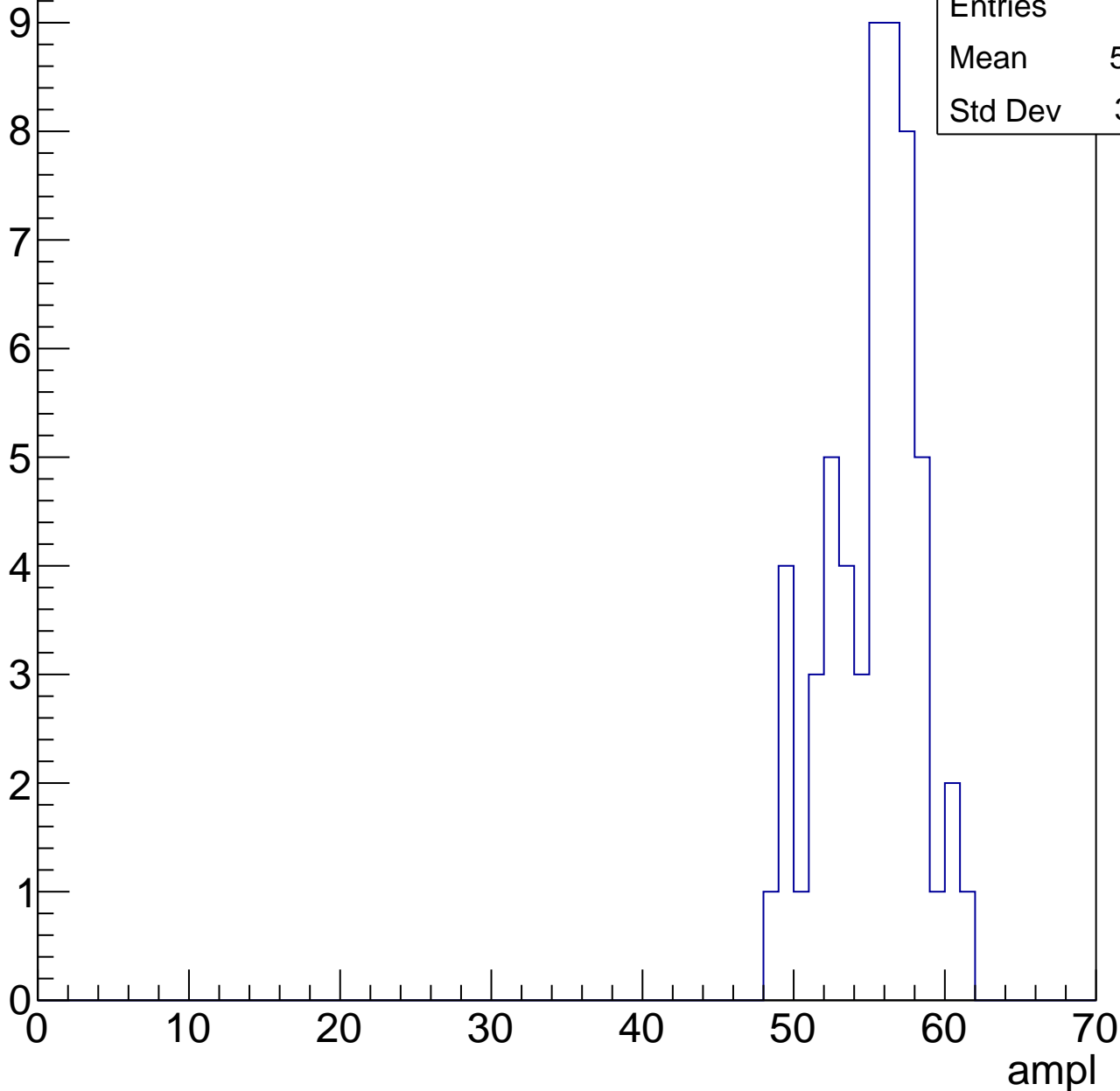


# B1L103S, U16-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

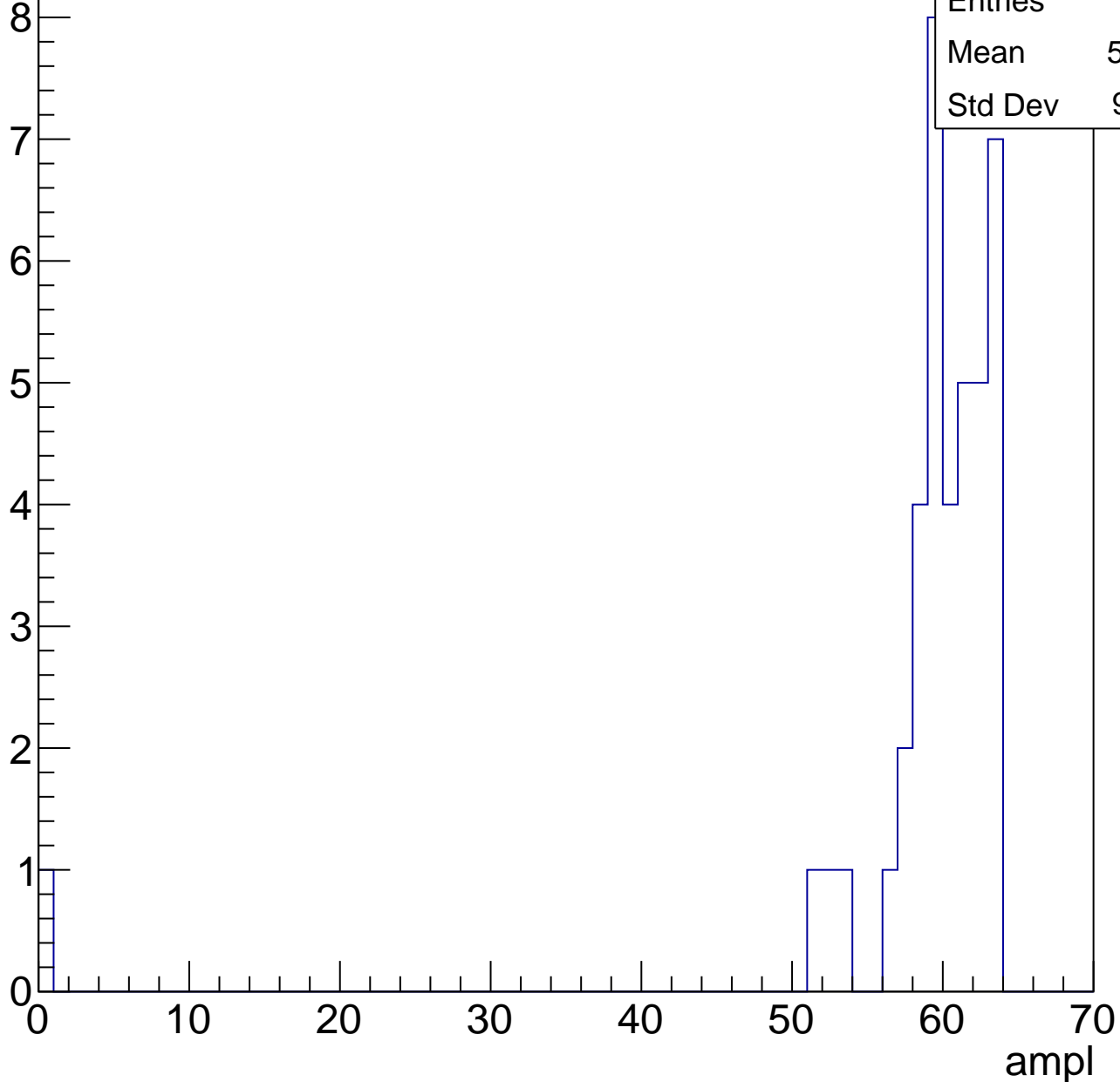
Entries	56
Mean	54.75
Std Dev	3.031



# B1L103S, U16-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

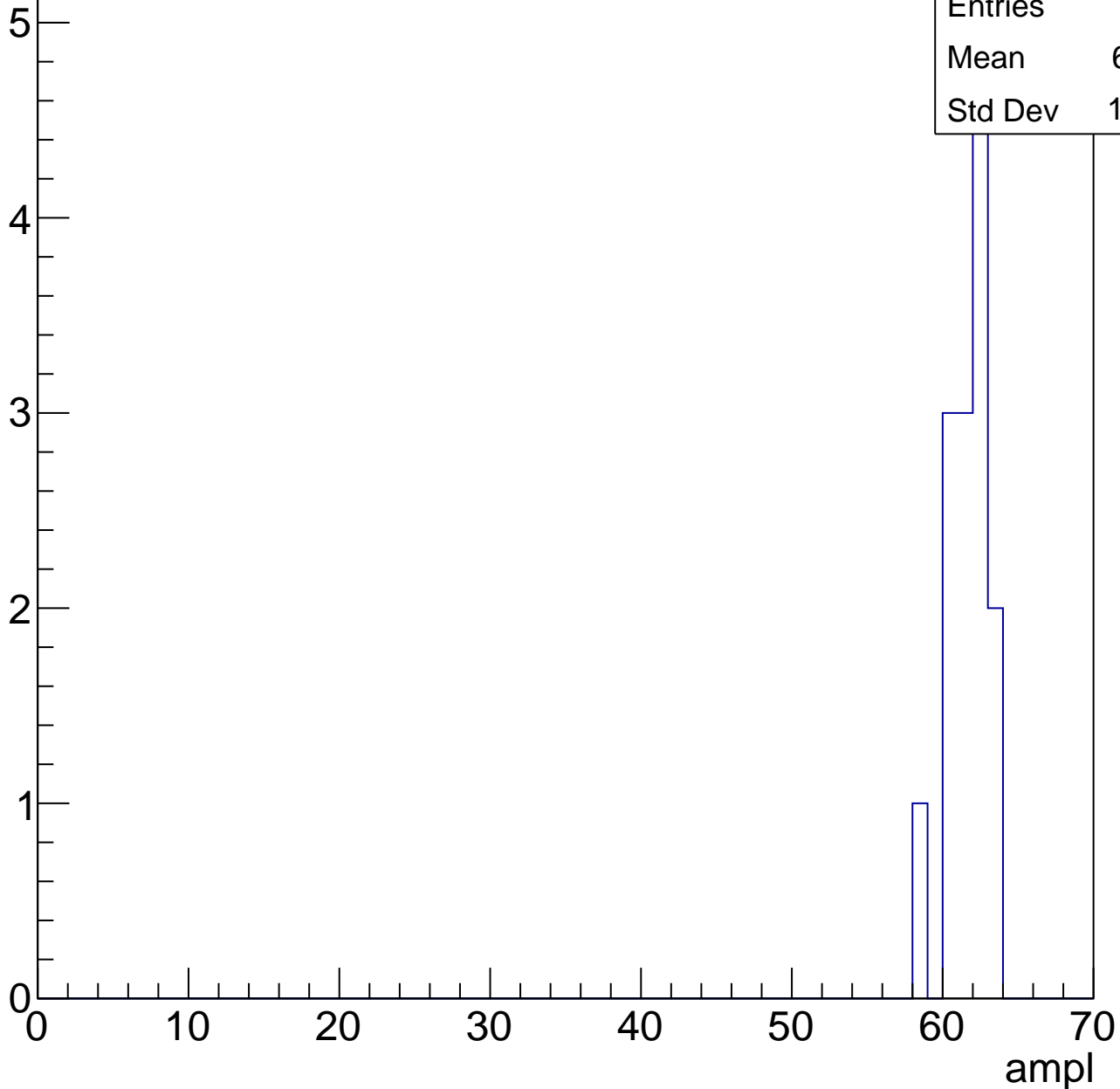


# B1L103S, U16-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	14
Mean	61.21
Std Dev	1.319





# B1L103S, U16-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch29, adc0

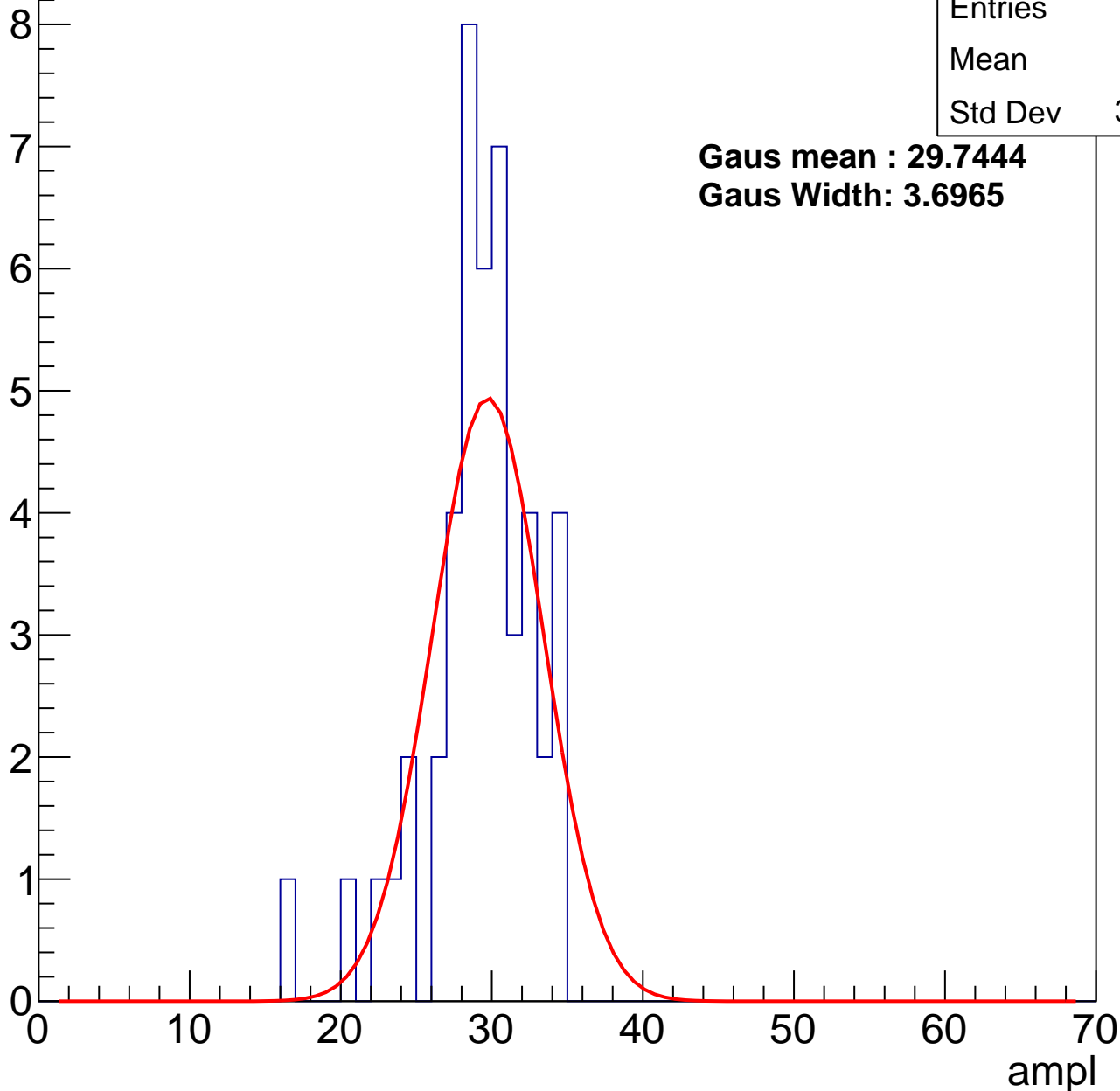
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	28.7
Std Dev	3.641

**Gaus mean : 29.7444**

**Gaus Width: 3.6965**



# B1L103S, U16-ch29, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	83
Mean	35.48
Std Dev	3.638

**Gaus mean : 35.8429**

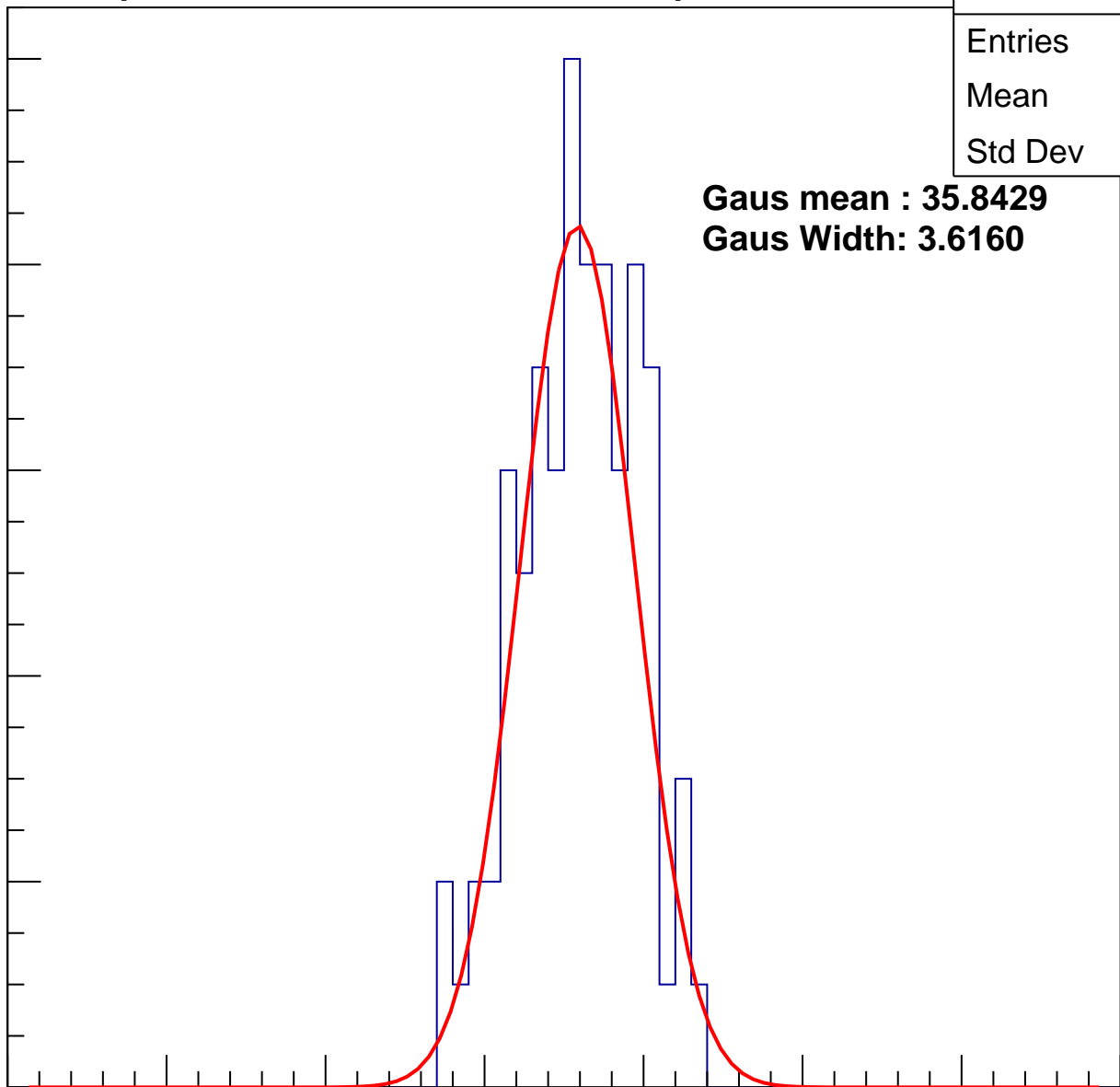
**Gaus Width: 3.6160**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U16-ch29, adc2

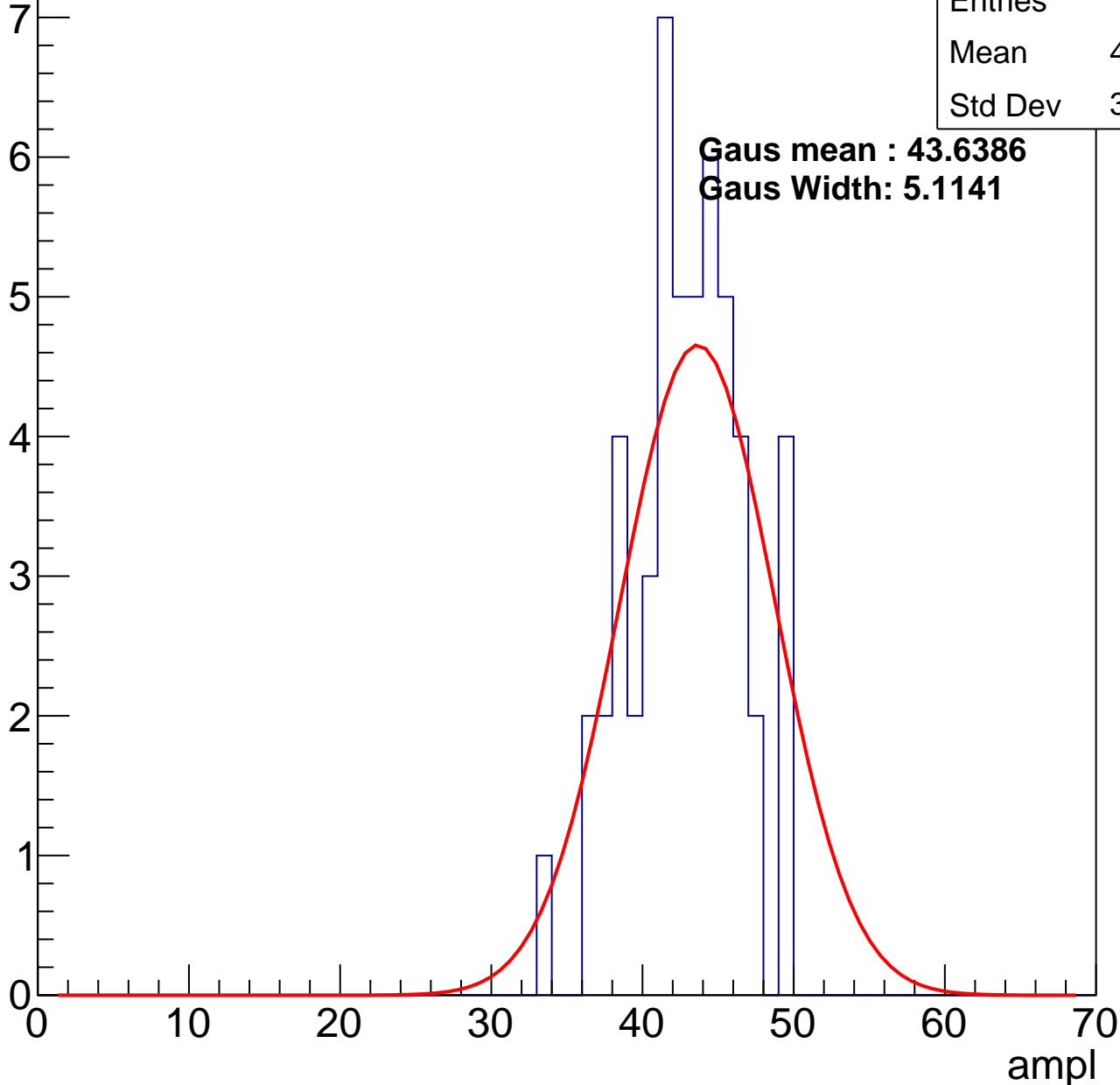
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	42.38
Std Dev	3.617

**Gaus mean : 43.6386**

**Gaus Width: 5.1141**



# B1L103S, U16-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	81
Mean	48.62
Std Dev	3.68

Entry

10

8

6

4

2

0

0

10

20

30

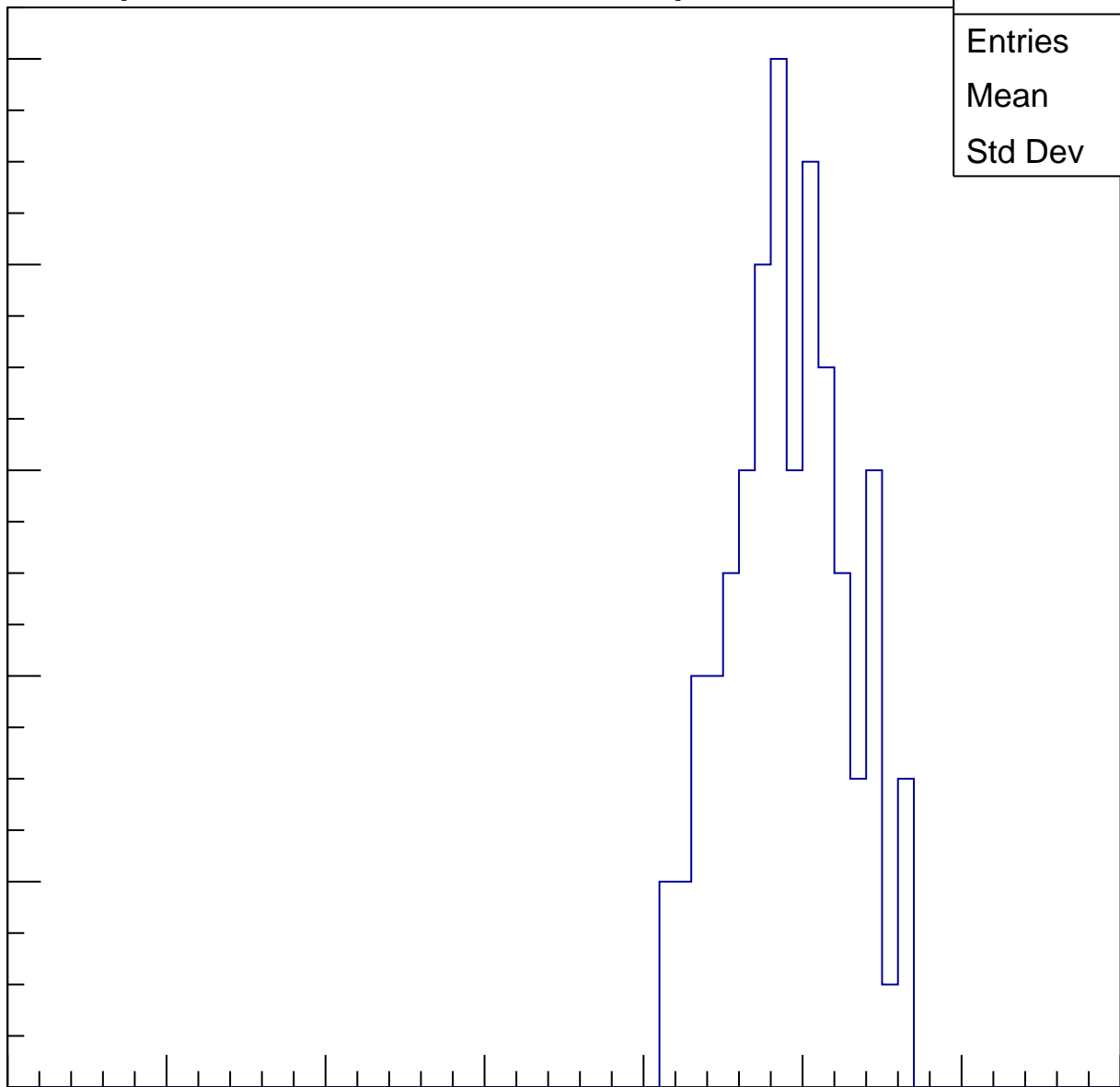
40

50

60

70

ampl

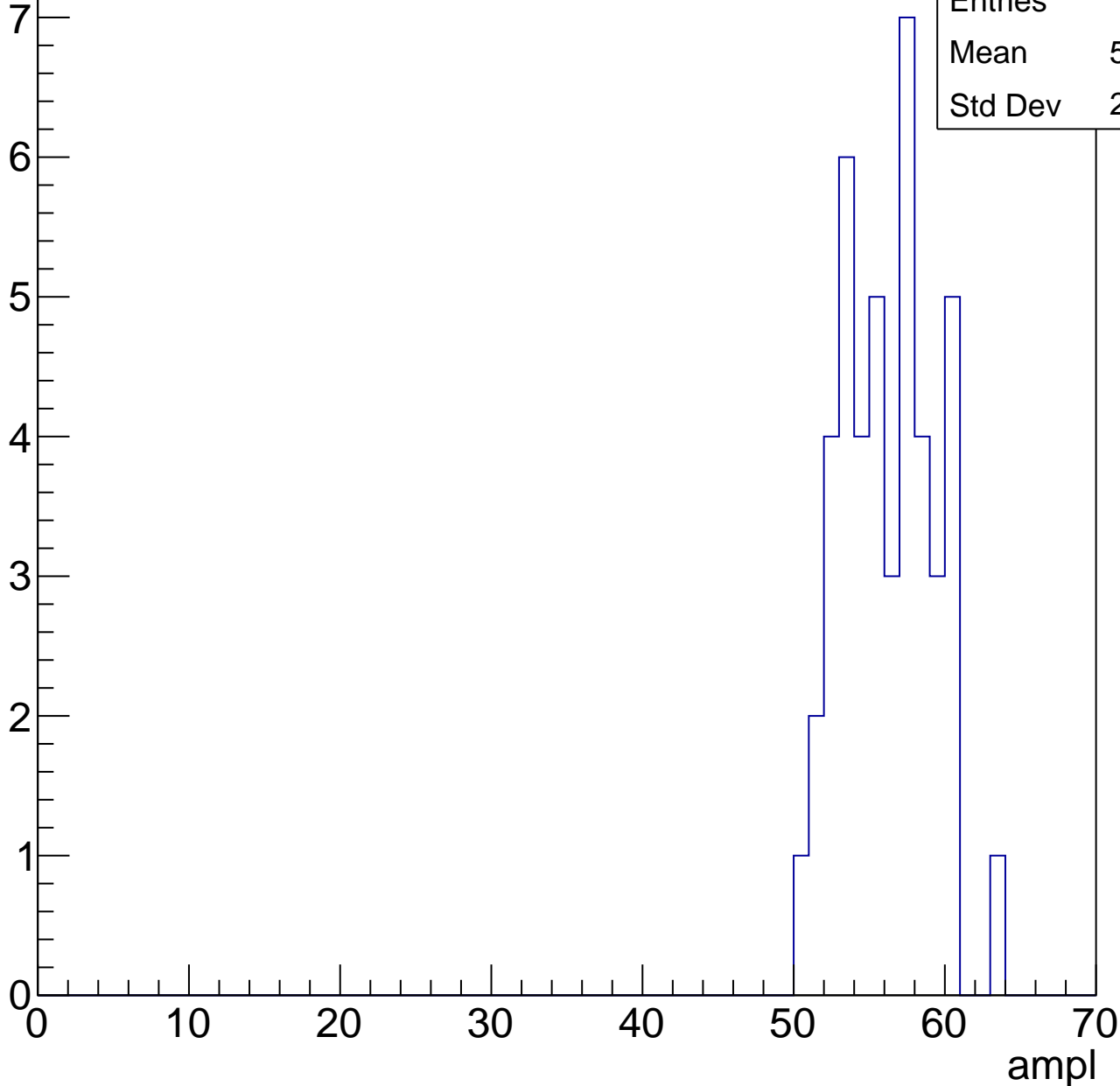


# B1L103S, U16-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	55.73
Std Dev	2.984

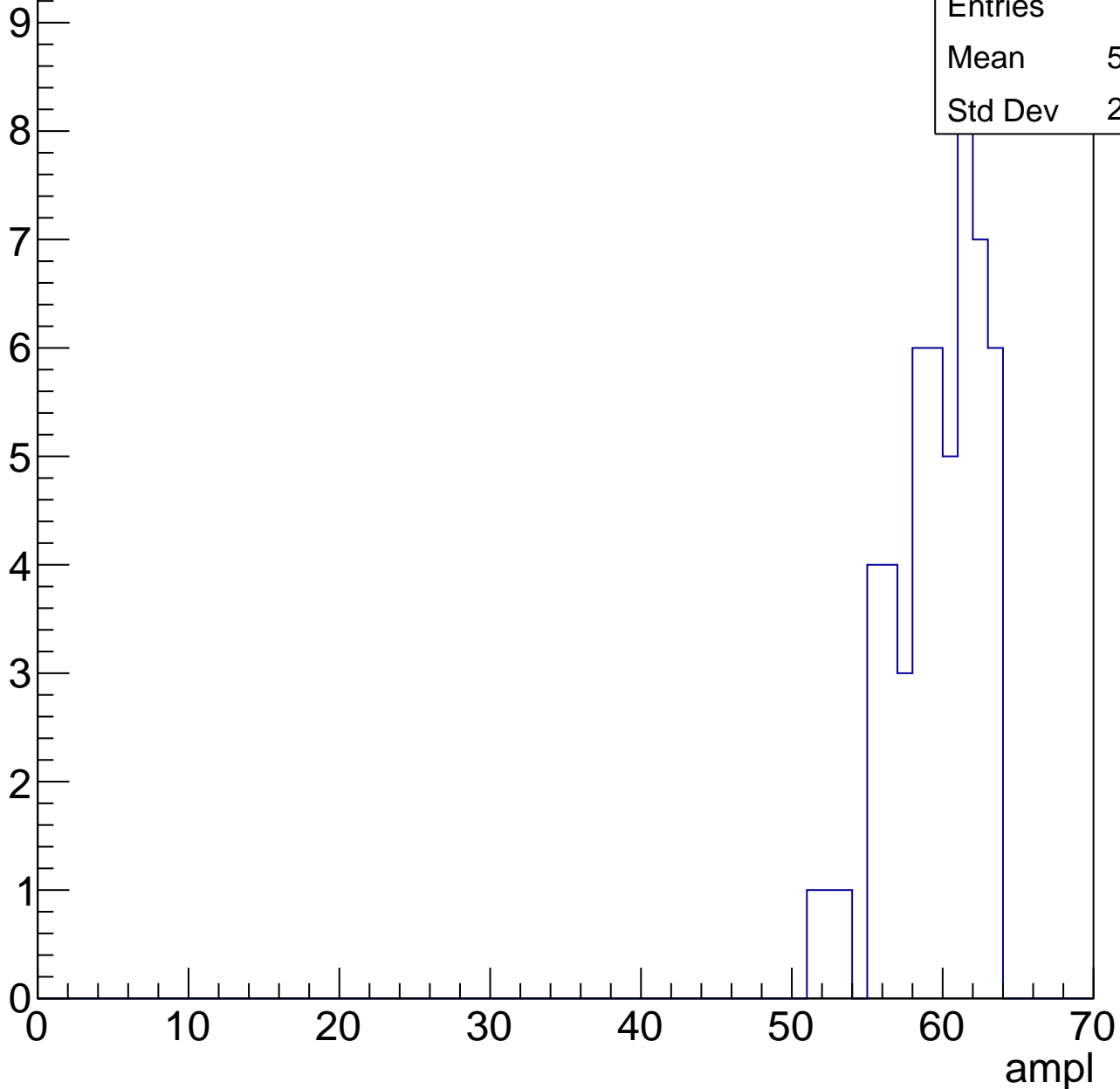


# B1L103S, U16-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

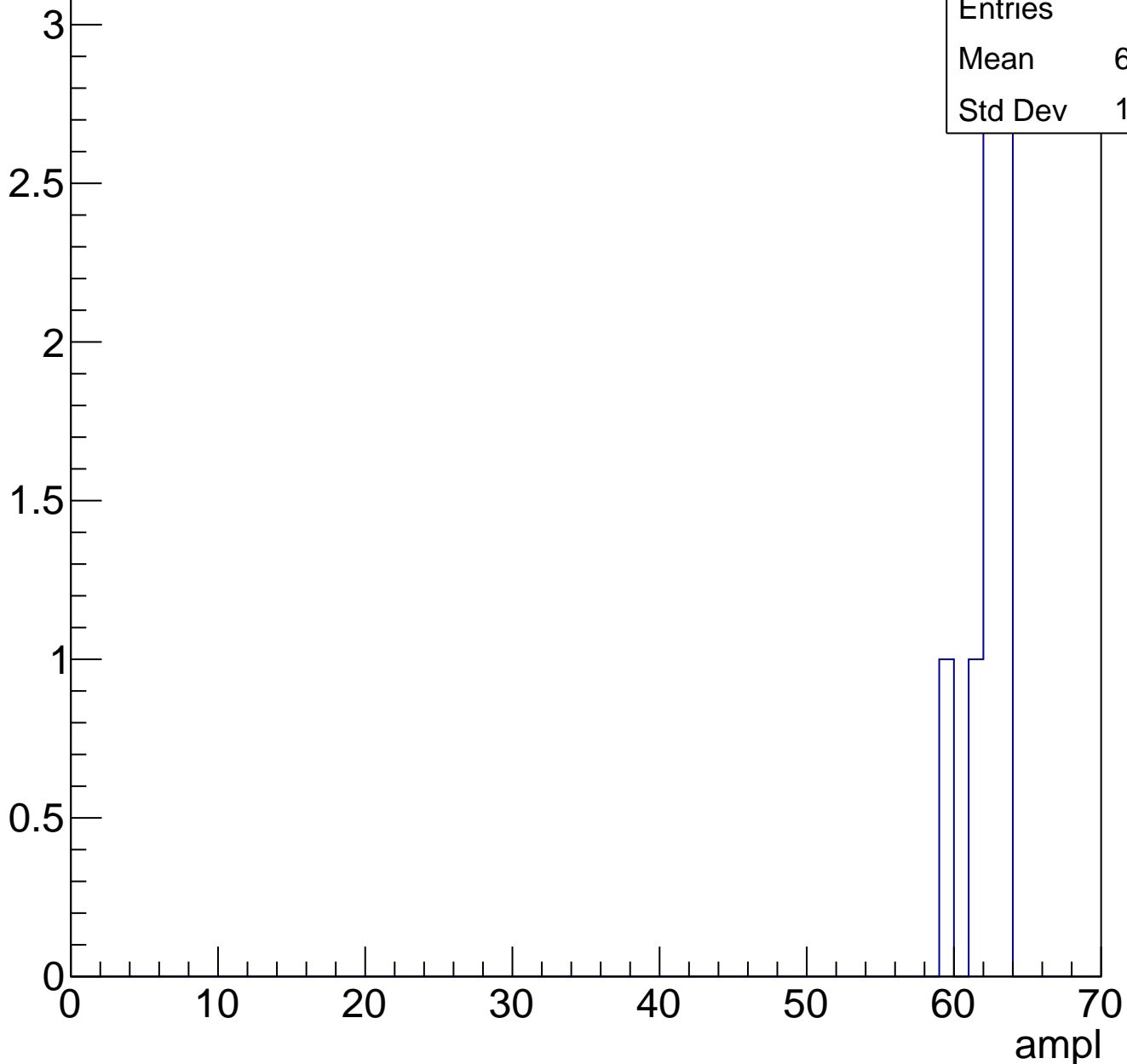
Entries	53
Mean	59.13
Std Dev	2.965



# B1L103S, U16-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

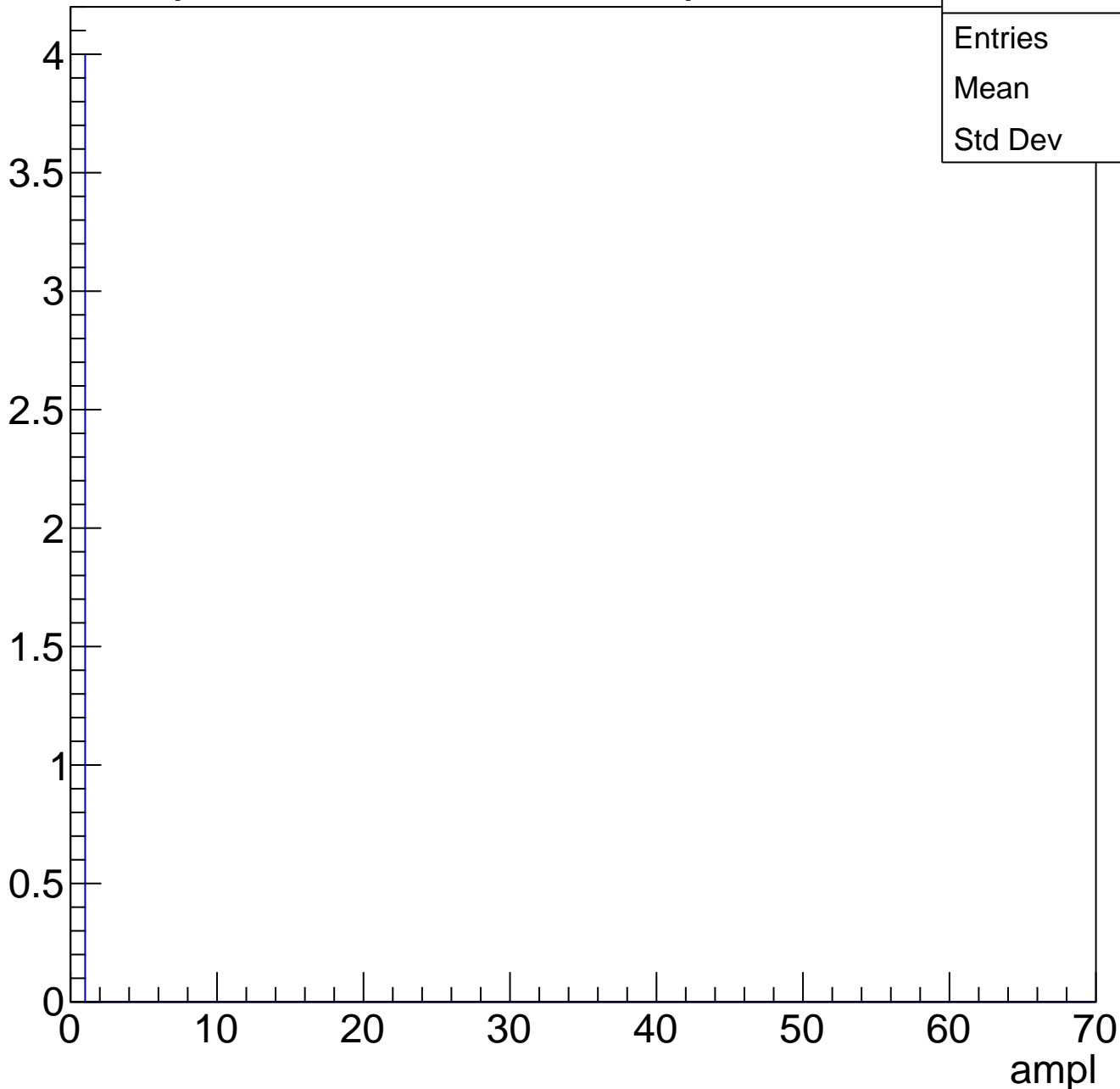




# B1L103S, U16-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	4
Mean	0
Std Dev	0

# B1L103S, U16-ch30, adc0

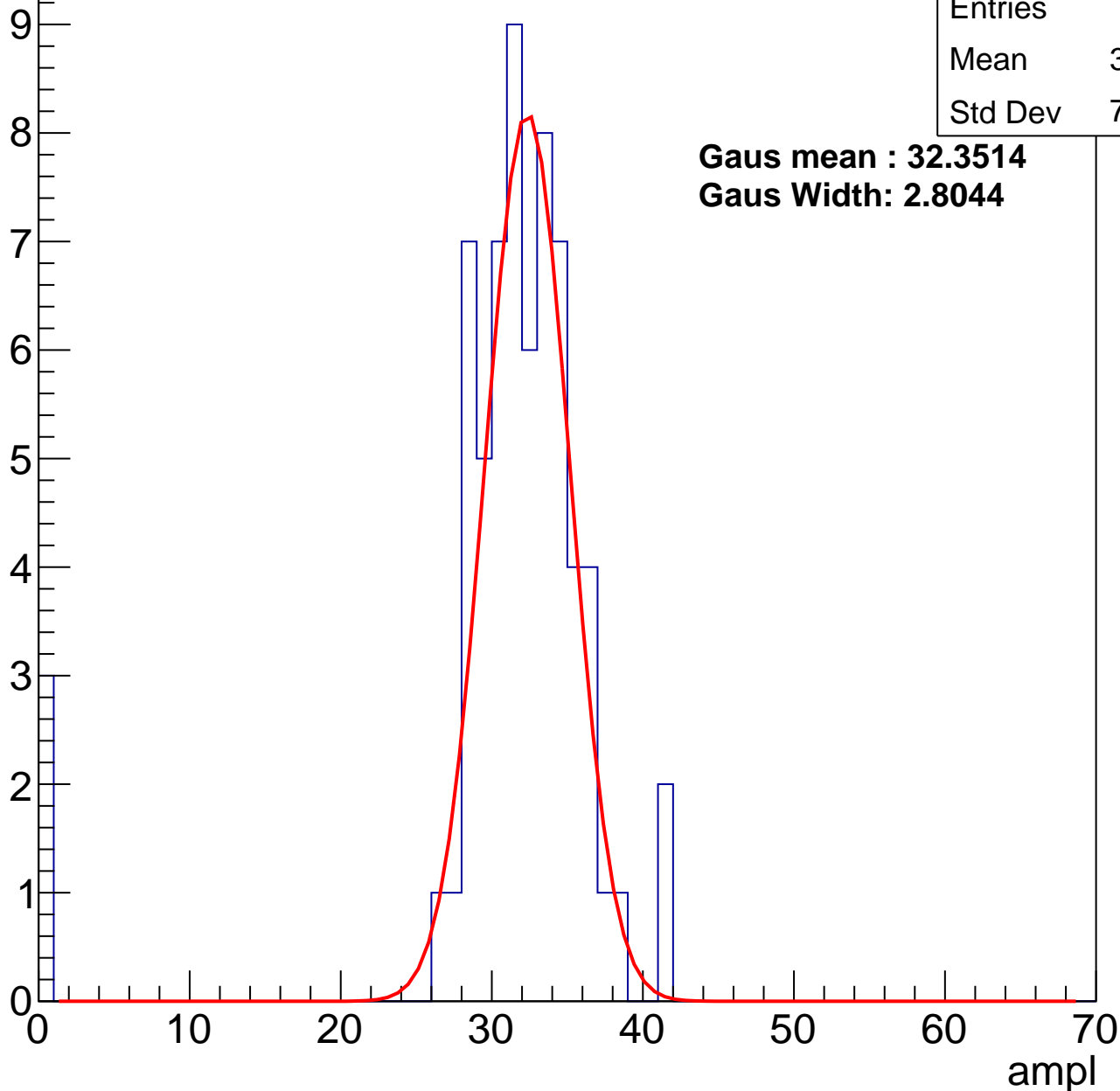
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	30.58
Std Dev	7.336

**Gaus mean : 32.3514**

**Gaus Width: 2.8044**



# B1L103S, U16-ch30, adc1

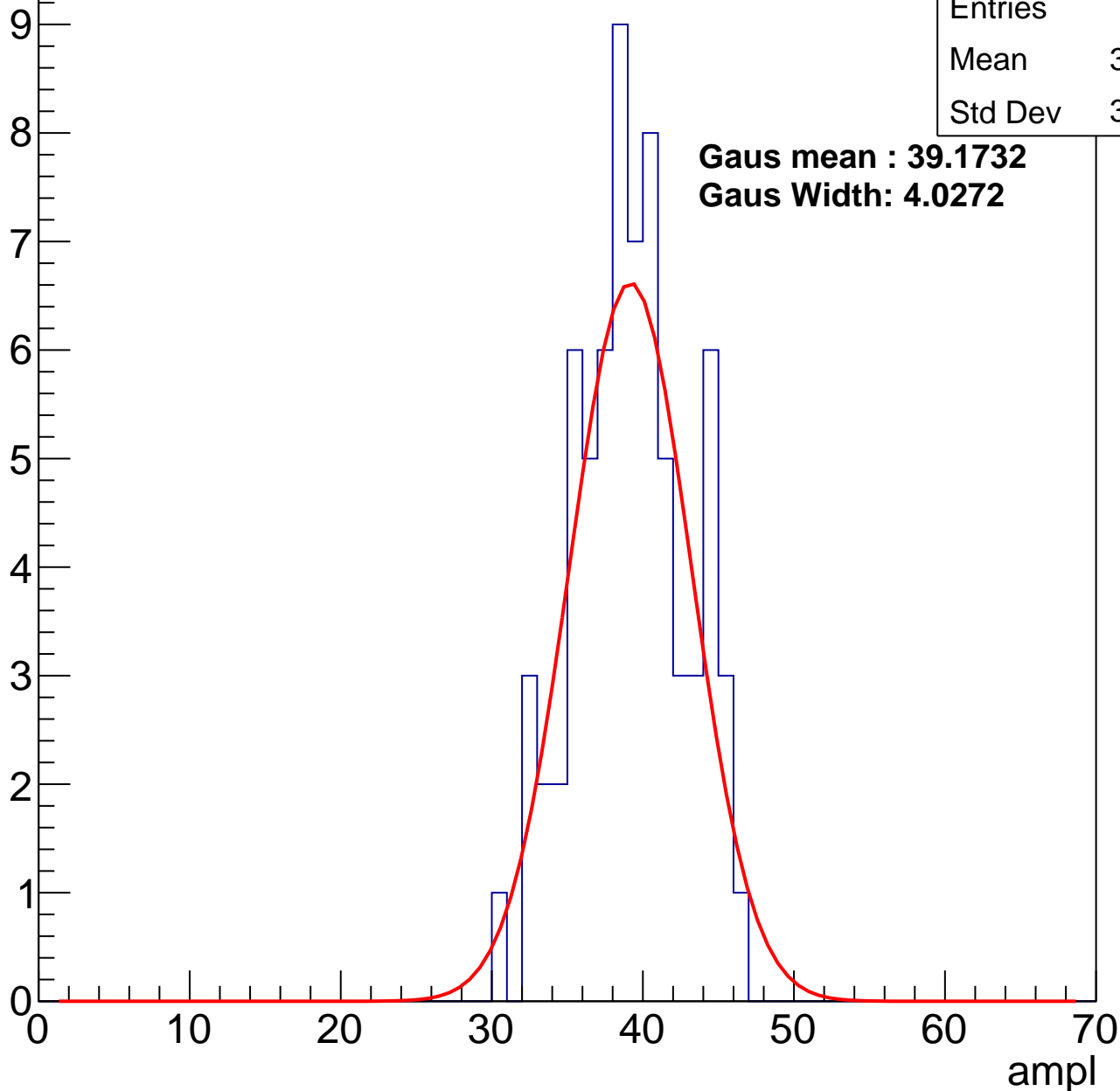
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	38.74
Std Dev	3.644

**Gaus mean : 39.1732**

**Gaus Width: 4.0272**



# B1L103S, U16-ch30, adc2

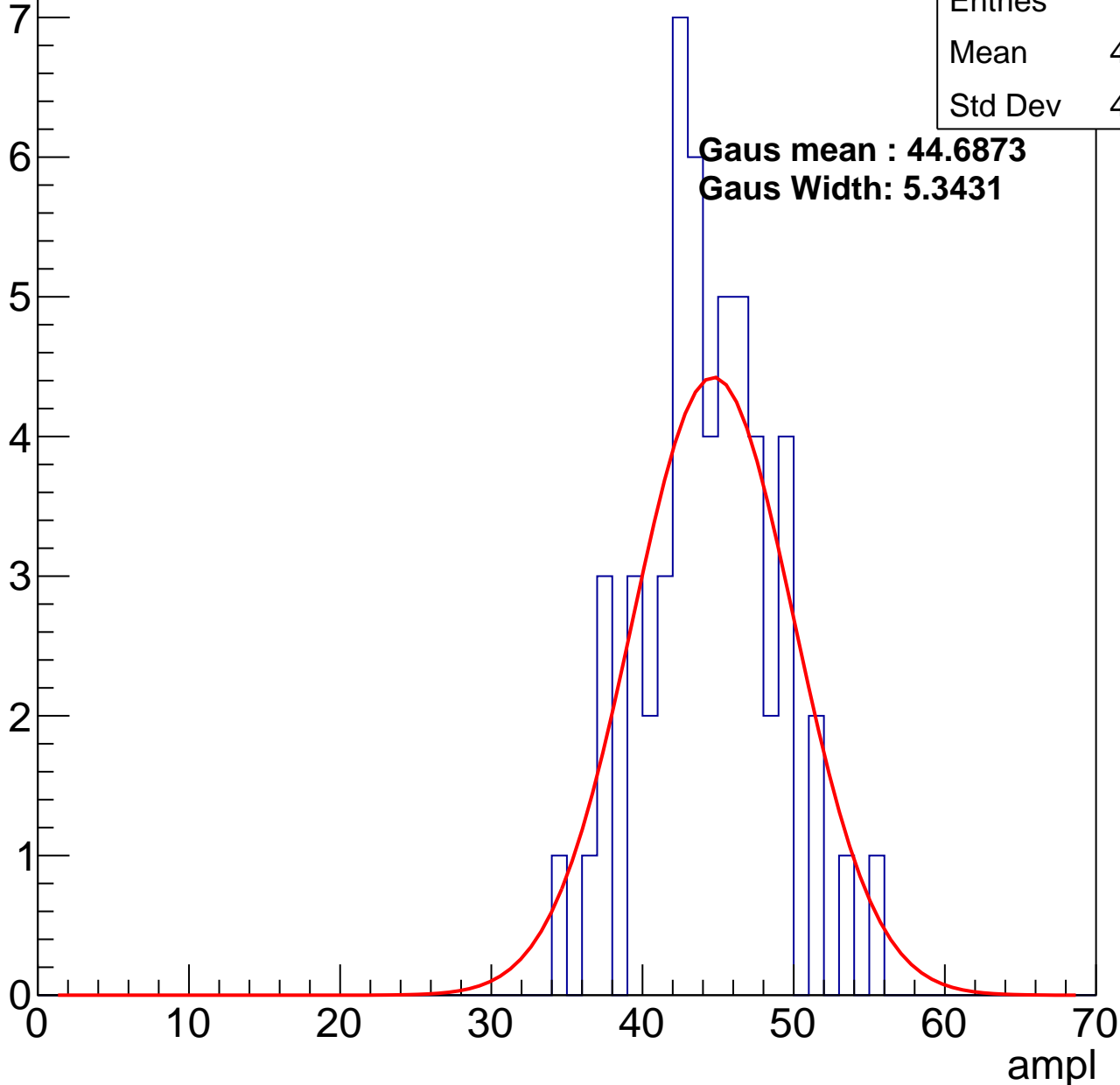
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	43.96
Std Dev	4.242

**Gaus mean : 44.6873**

**Gaus Width: 5.3431**

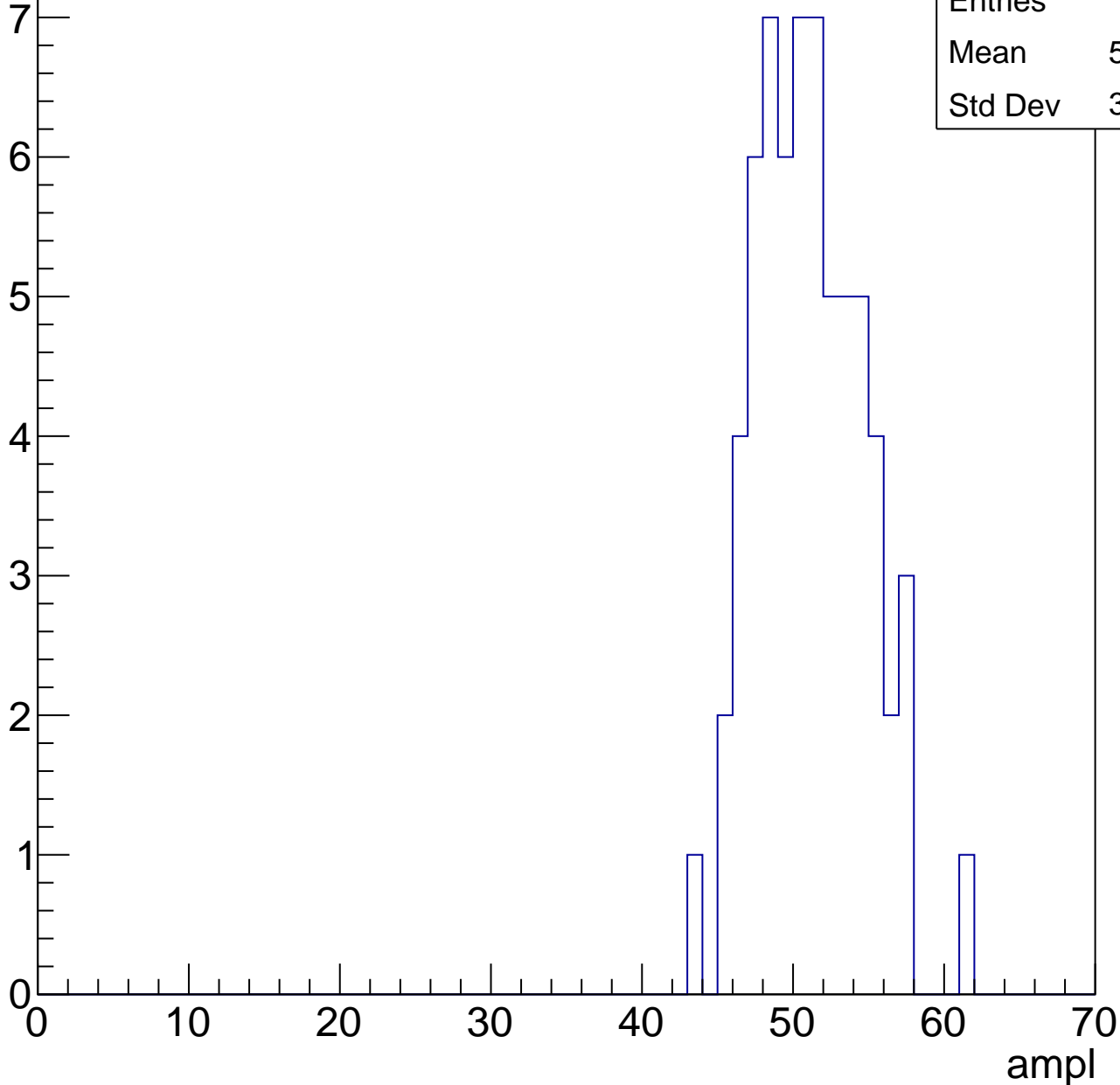


# B1L103S, U16-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

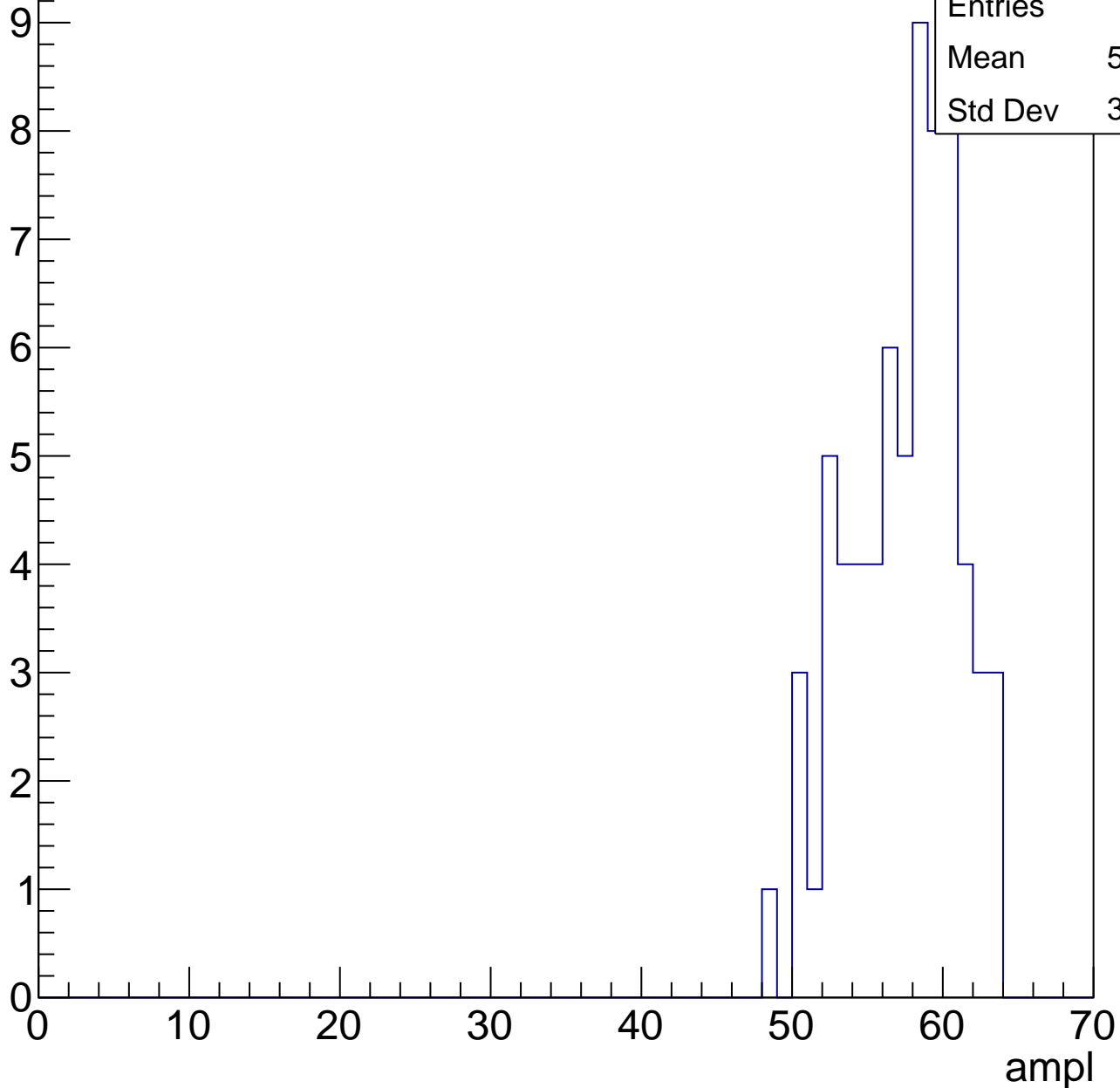
Entries	65
Mean	50.69
Std Dev	3.534



# B1L103S, U16-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

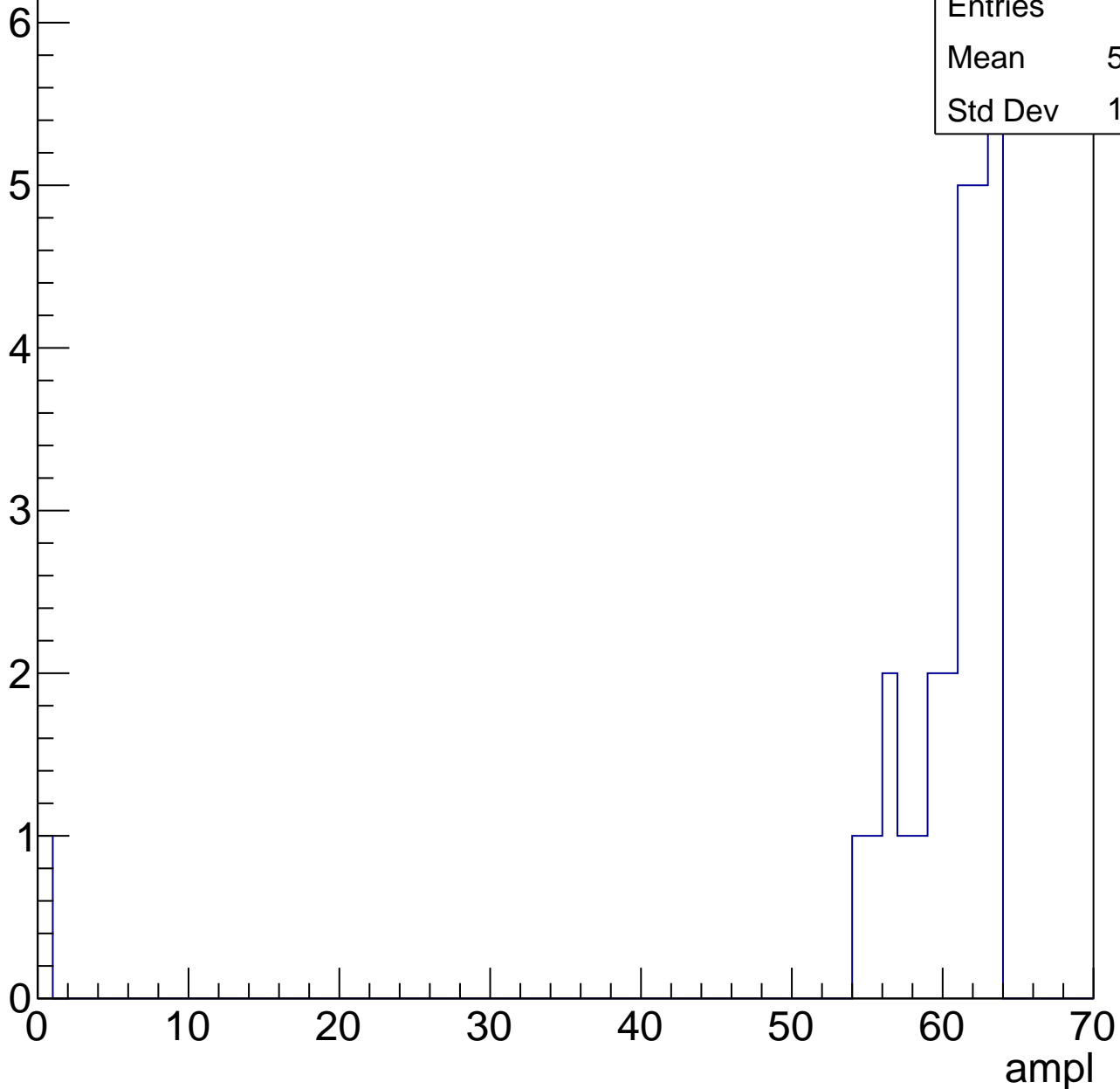


# B1L103S, U16-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

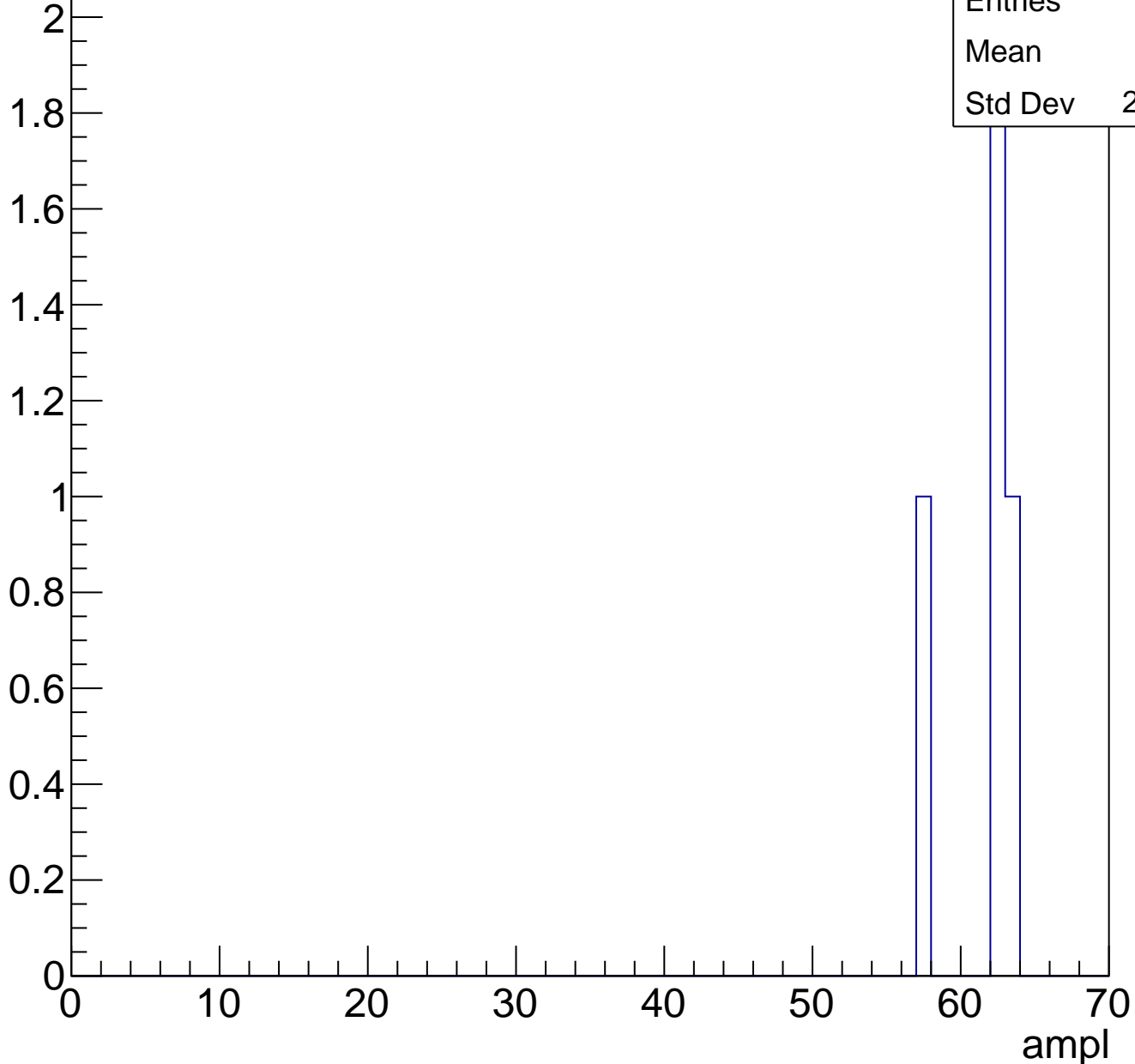
Entries	27
Mean	58.04
Std Dev	11.68



# B1L103S, U16-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	25
Std Dev	0

ampl

0 10 20 30 40 50 60 70

# B1L103S, U16-ch31, adc0

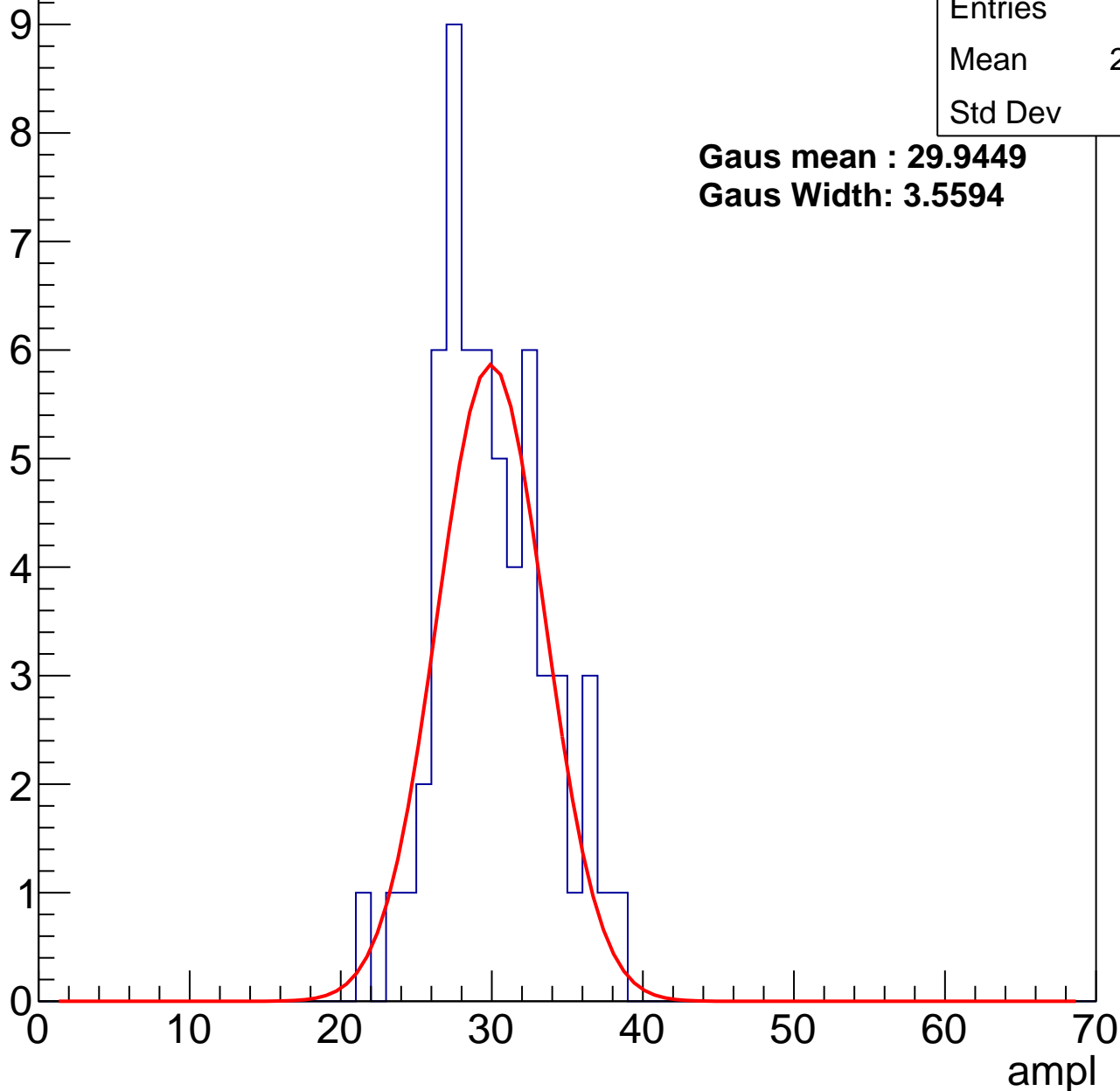
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	29.56
Std Dev	3.59

**Gaus mean : 29.9449**

**Gaus Width: 3.5594**



# B1L103S, U16-ch31, adc1

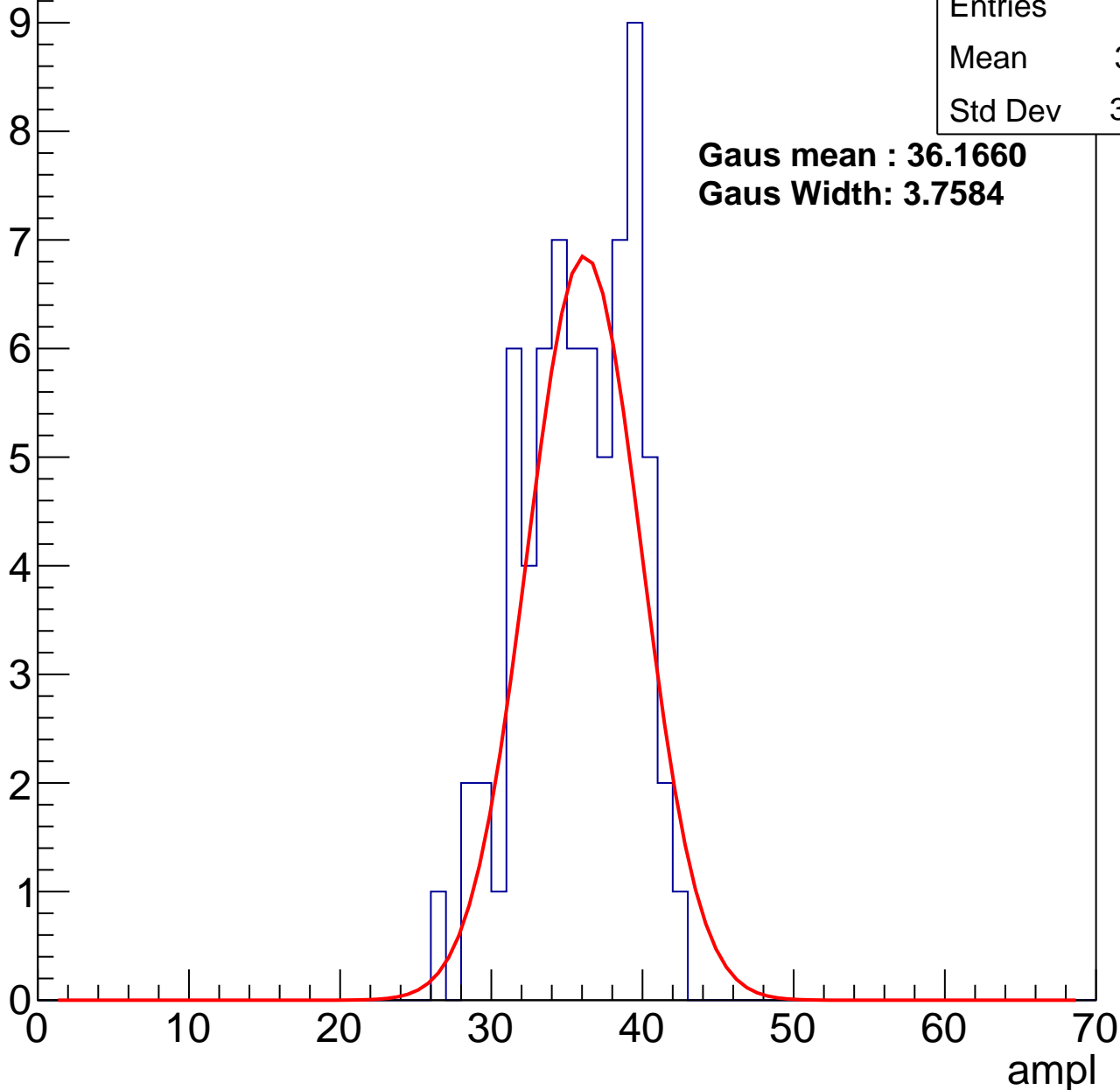
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	35.31
Std Dev	3.608

**Gaus mean : 36.1660**

**Gaus Width: 3.7584**



# B1L103S, U16-ch31, adc2

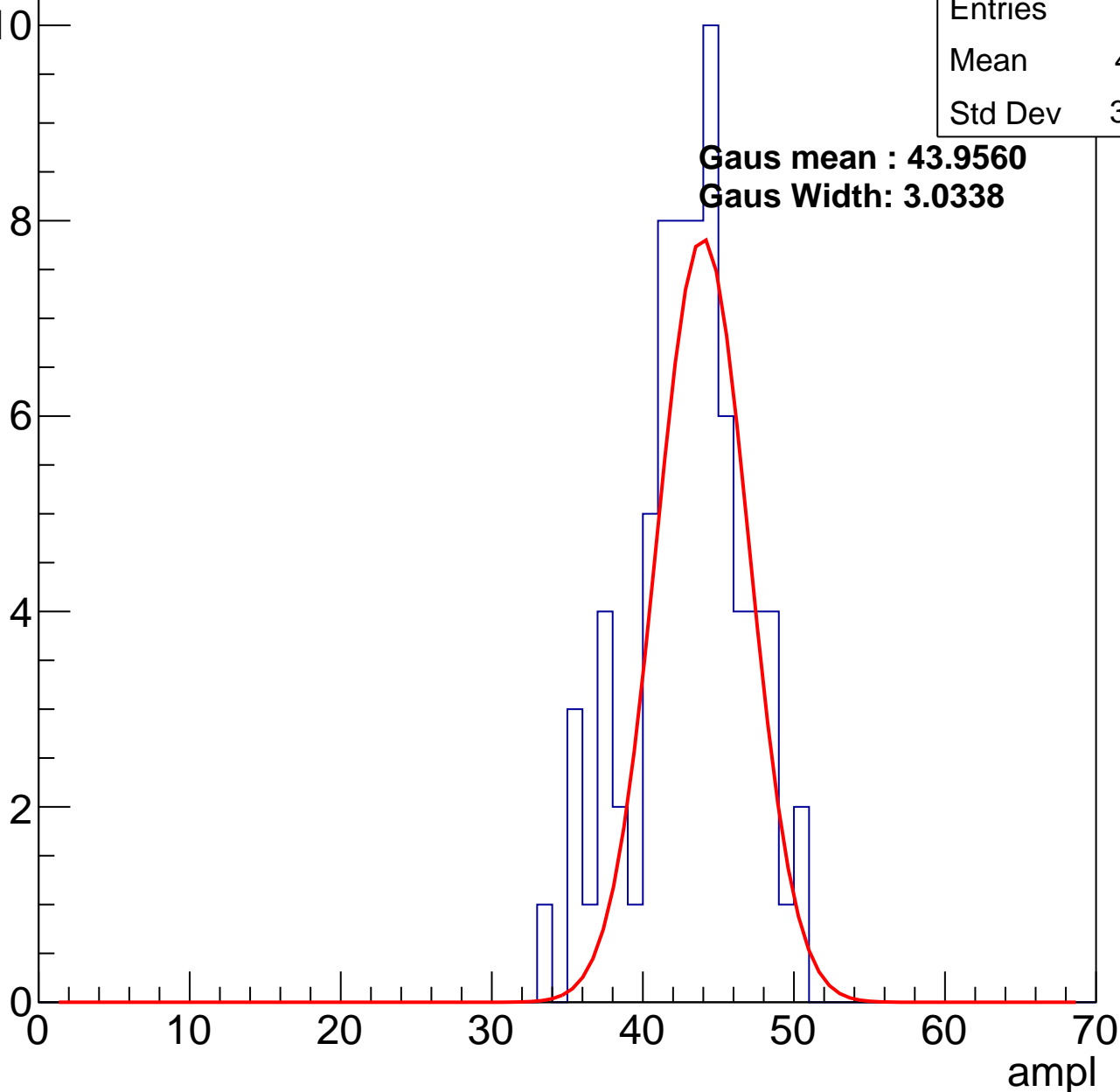
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	42.61
Std Dev	3.714

**Gaus mean : 43.9560**

**Gaus Width: 3.0338**

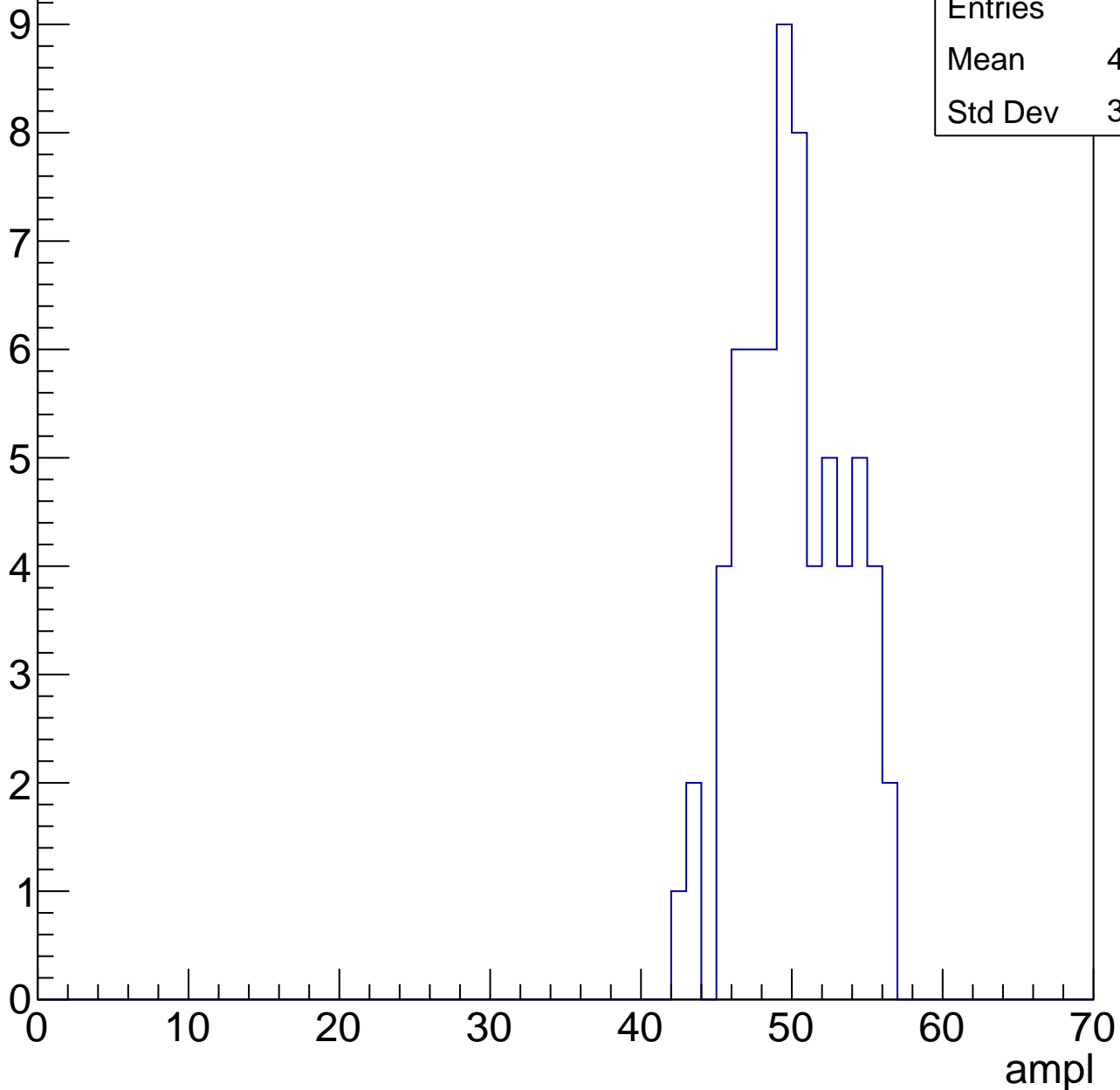


# B1L103S, U16-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

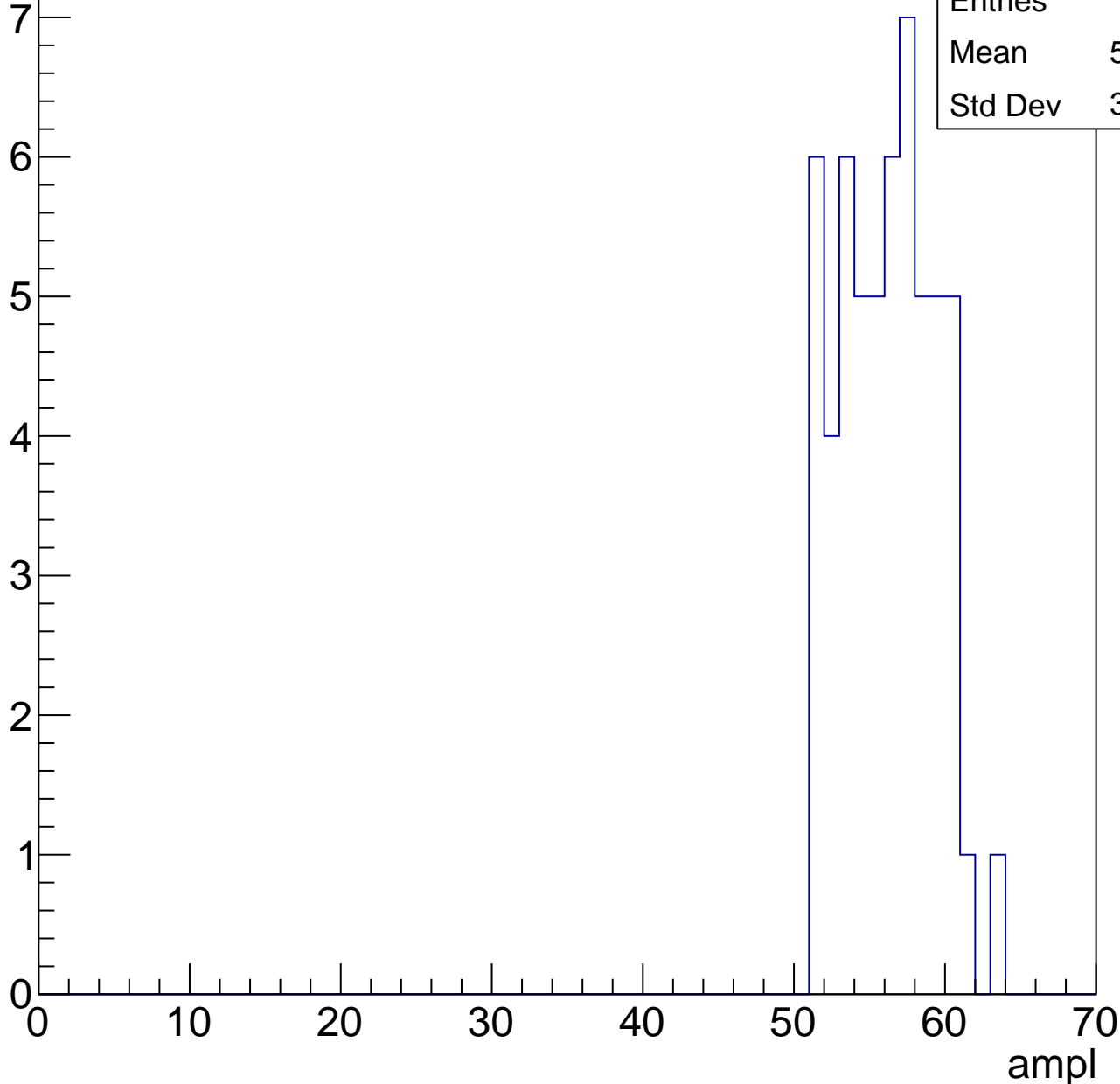
Entries	66
Mean	49.59
Std Dev	3.362



# B1L103S, U16-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



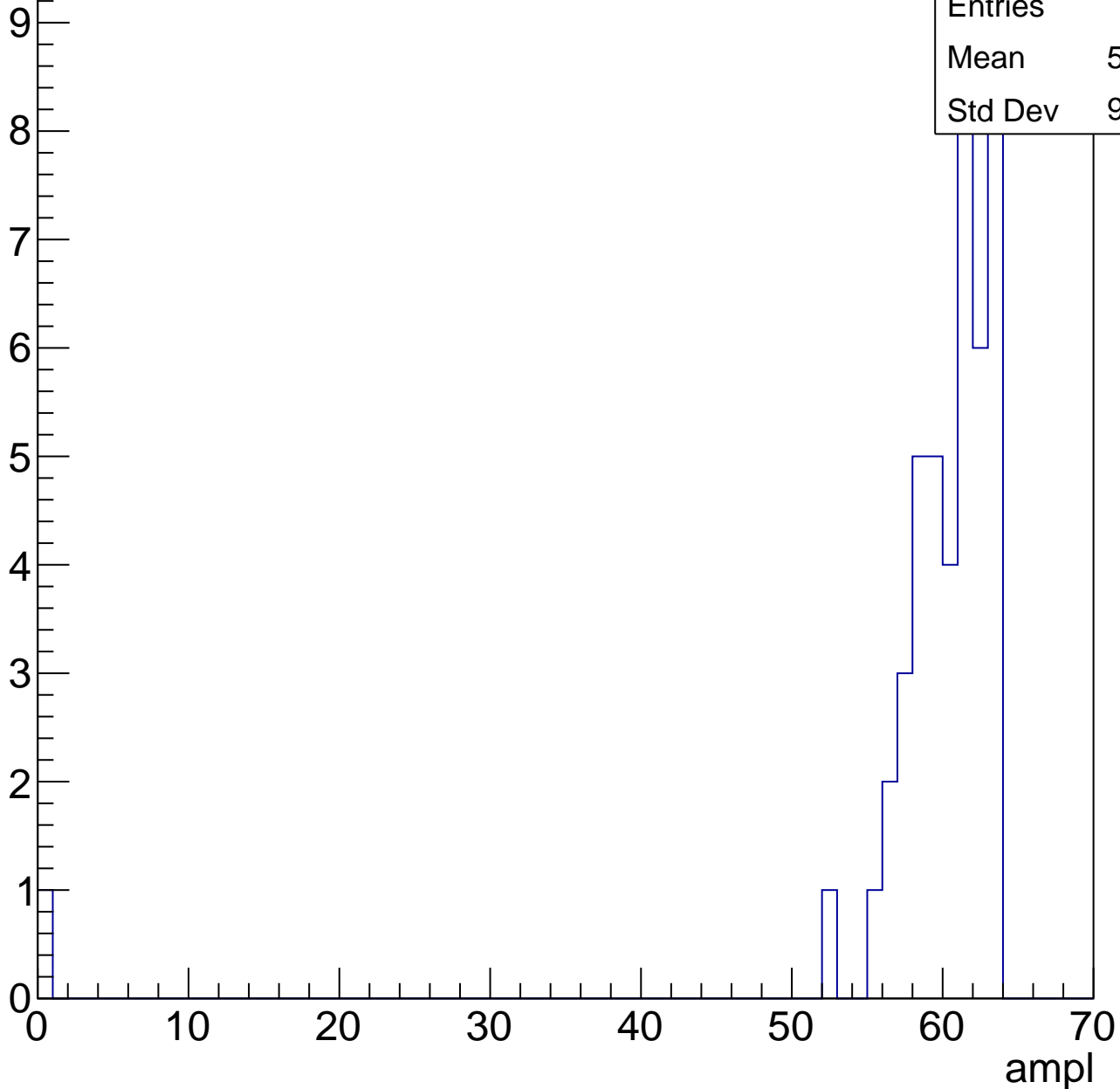
Entries	56
Mean	55.73
Std Dev	3.033

# B1L103S, U16-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

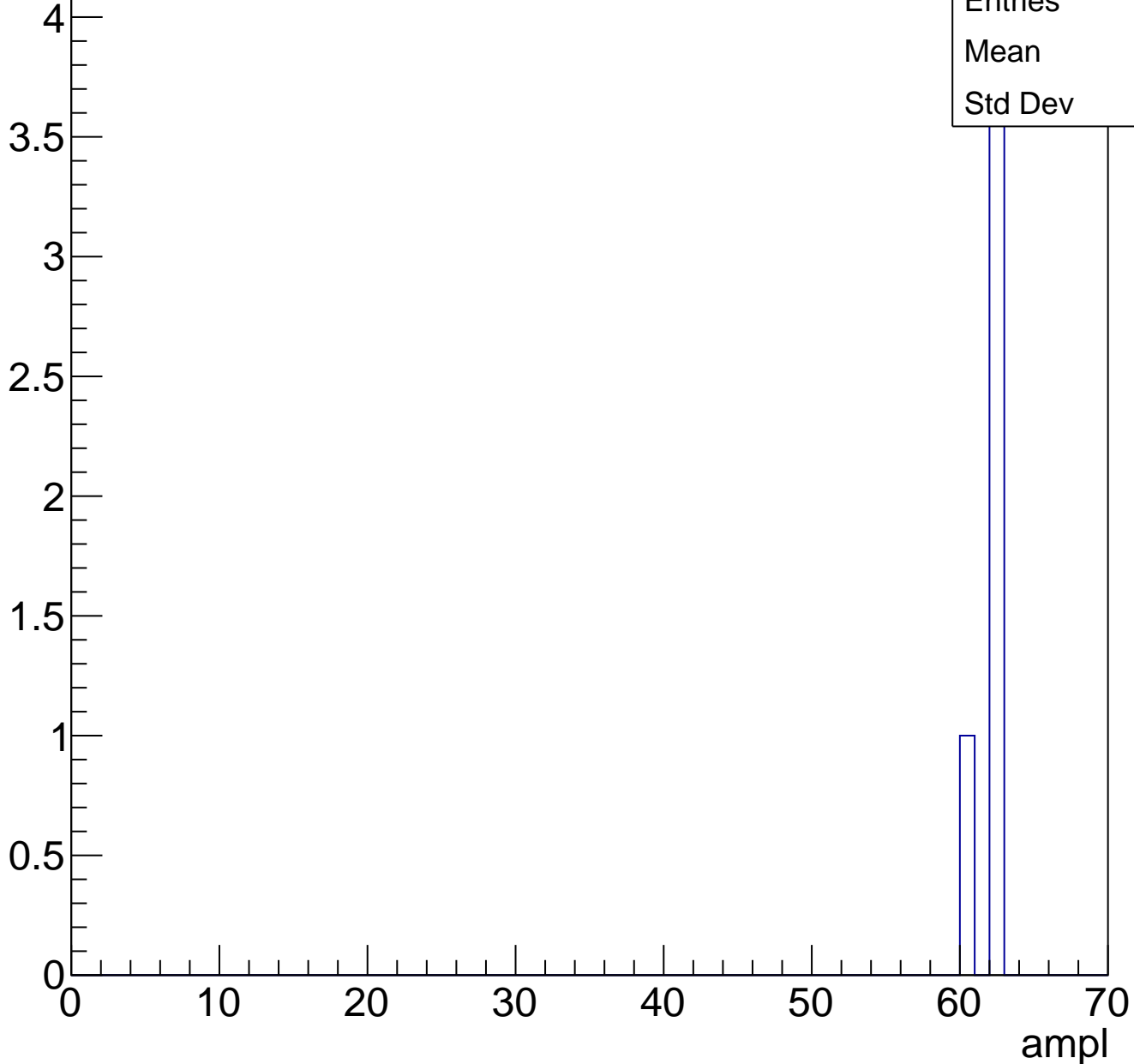
Entries	46
Mean	58.76
Std Dev	9.108



# B1L103S, U16-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U16-ch32, adc0

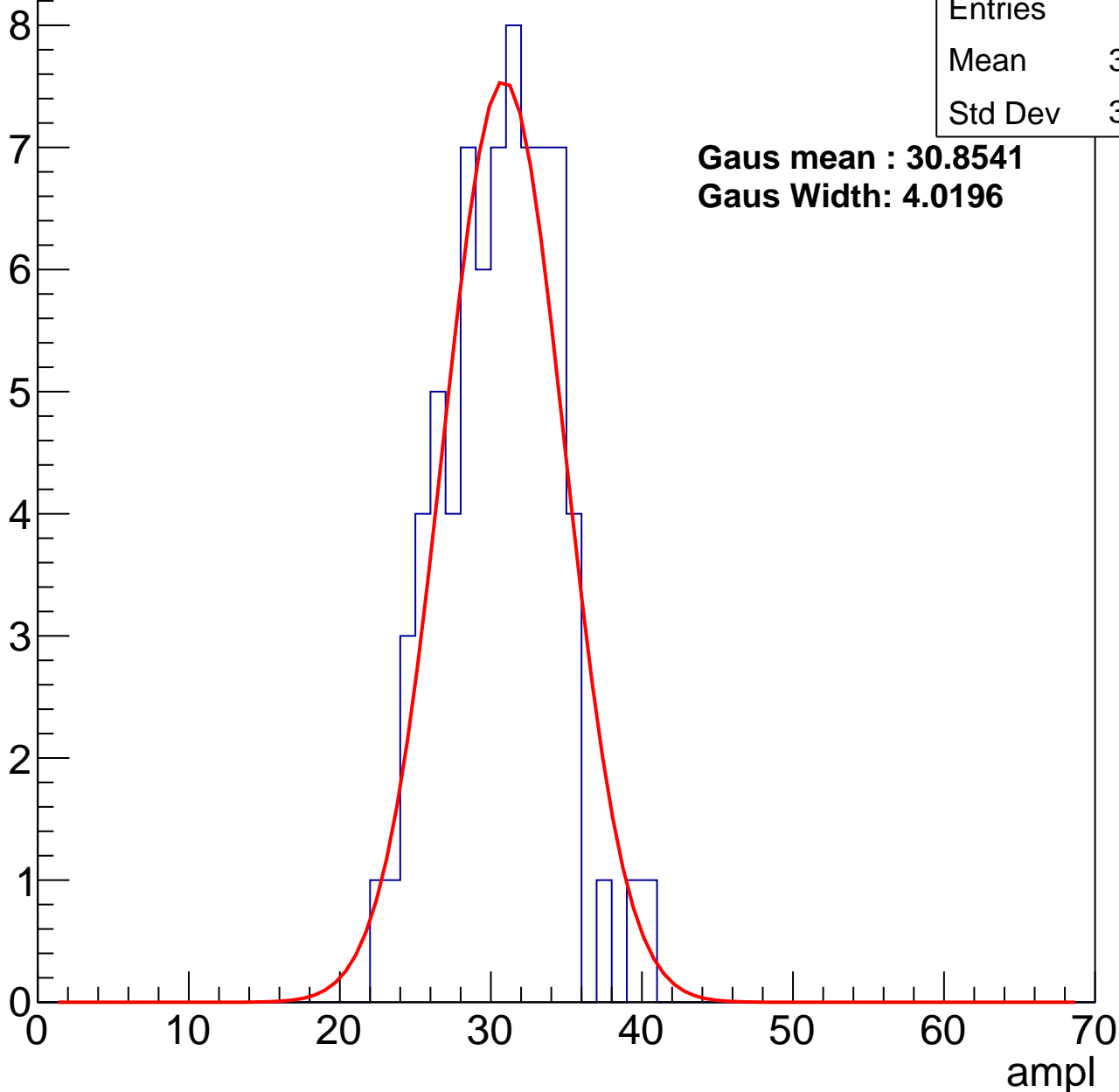
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	30.16
Std Dev	3.695

**Gaus mean : 30.8541**

**Gaus Width: 4.0196**



# B1L103S, U16-ch32, adc1

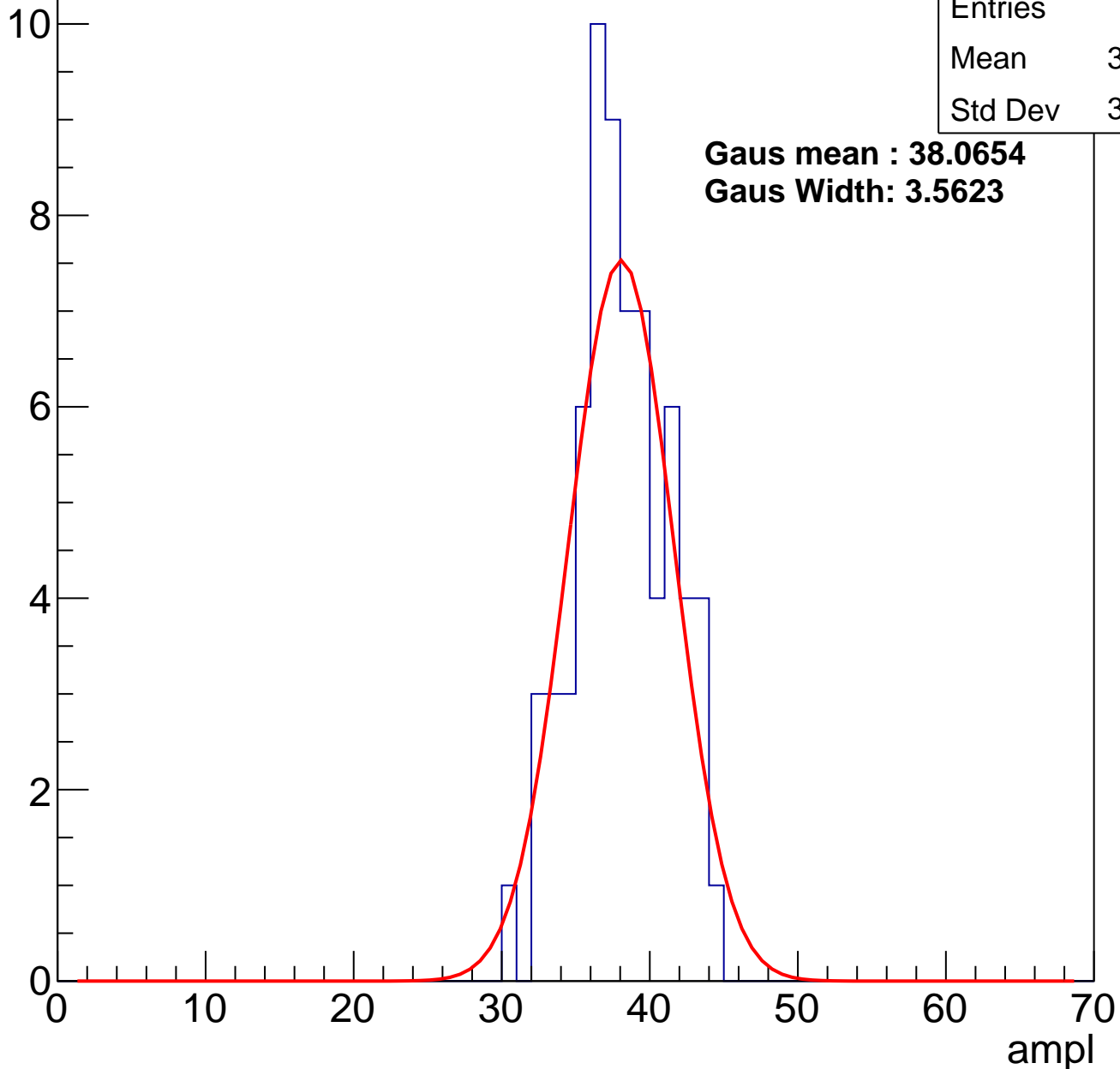
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	68
Mean	37.63
Std Dev	3.129

**Gaus mean : 38.0654**

**Gaus Width: 3.5623**

Entry



# B1L103S, U16-ch32, adc2

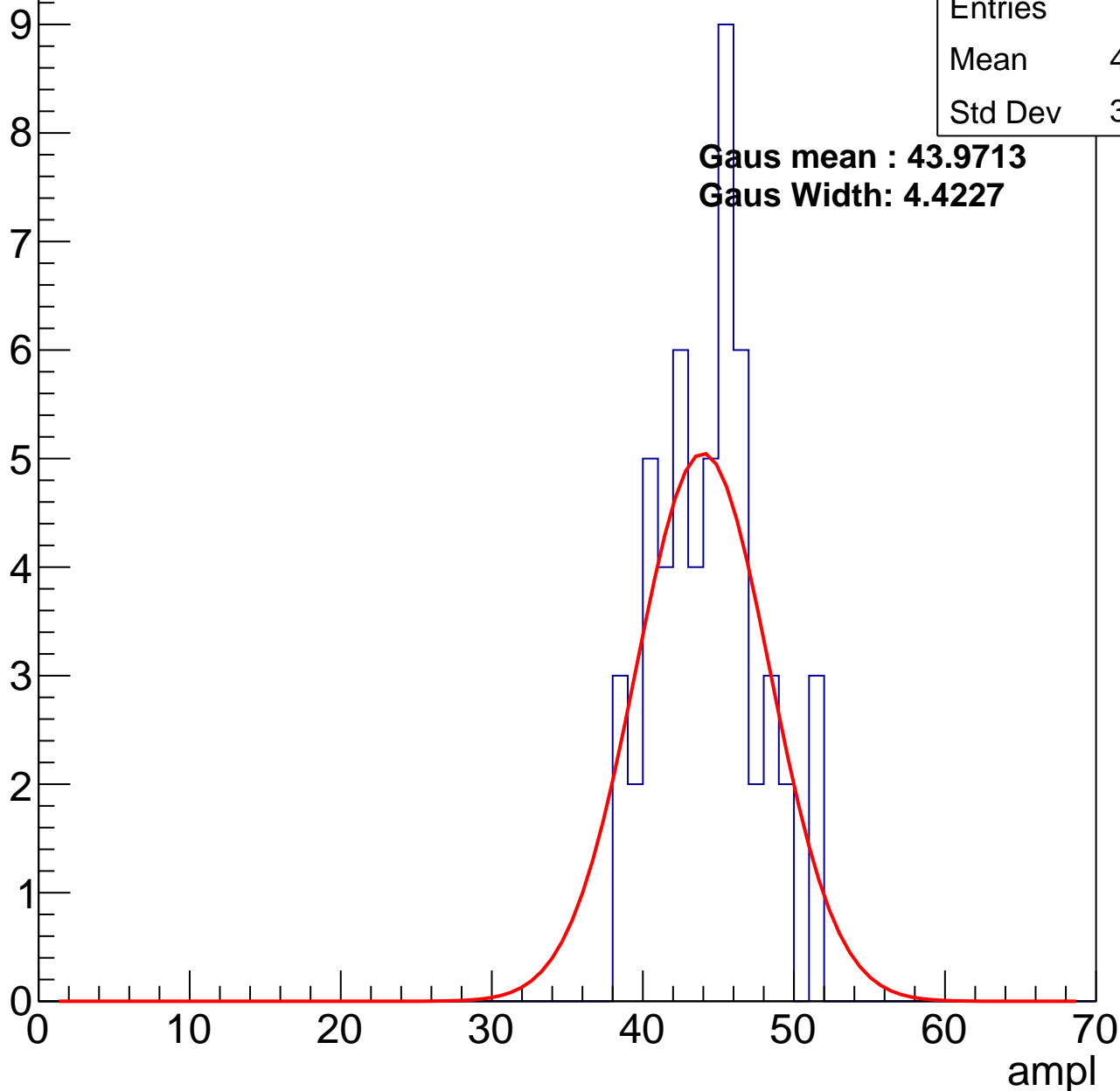
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	43.89
Std Dev	3.326

**Gaus mean : 43.9713**

**Gaus Width: 4.4227**

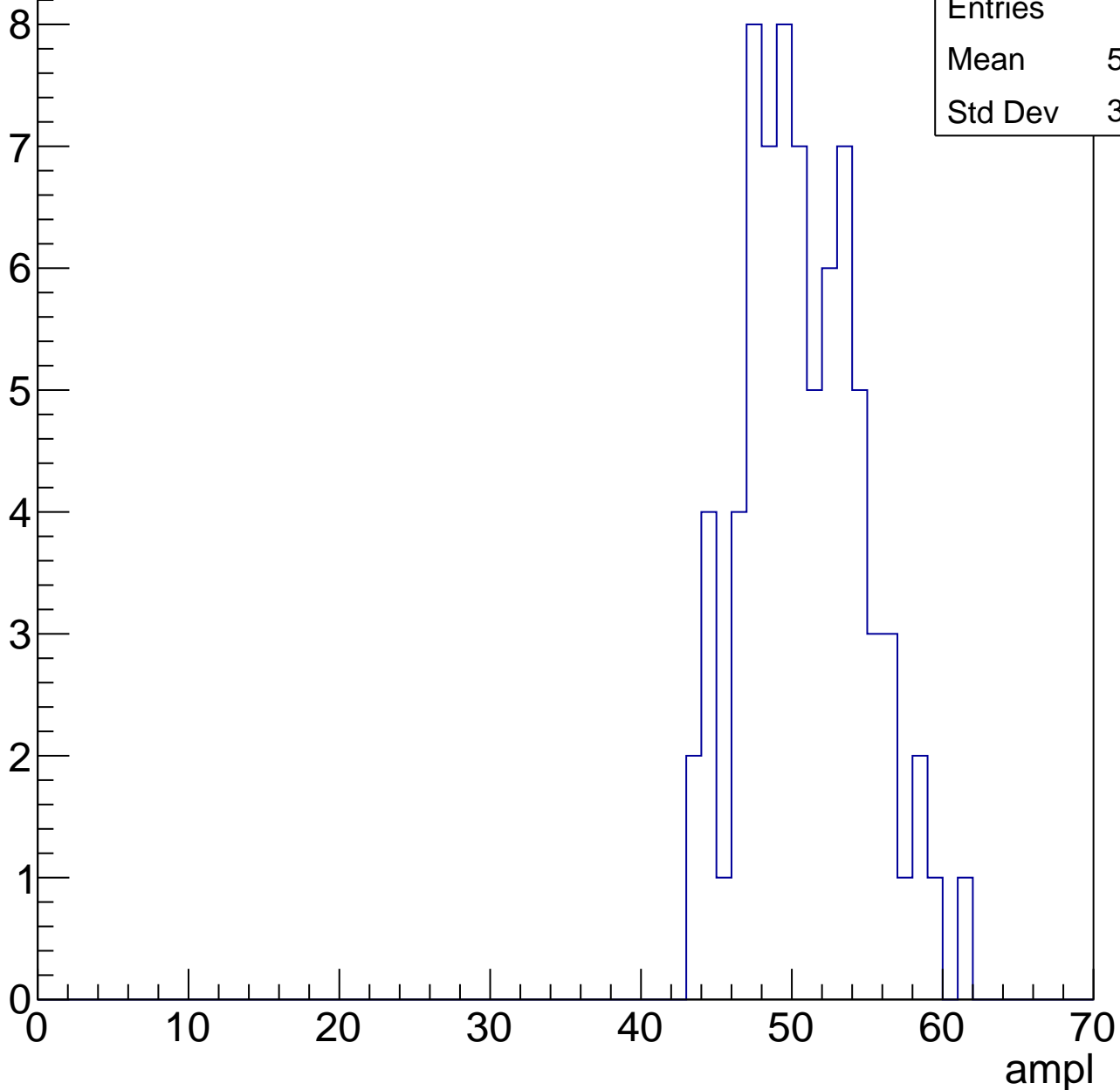


# B1L103S, U16-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

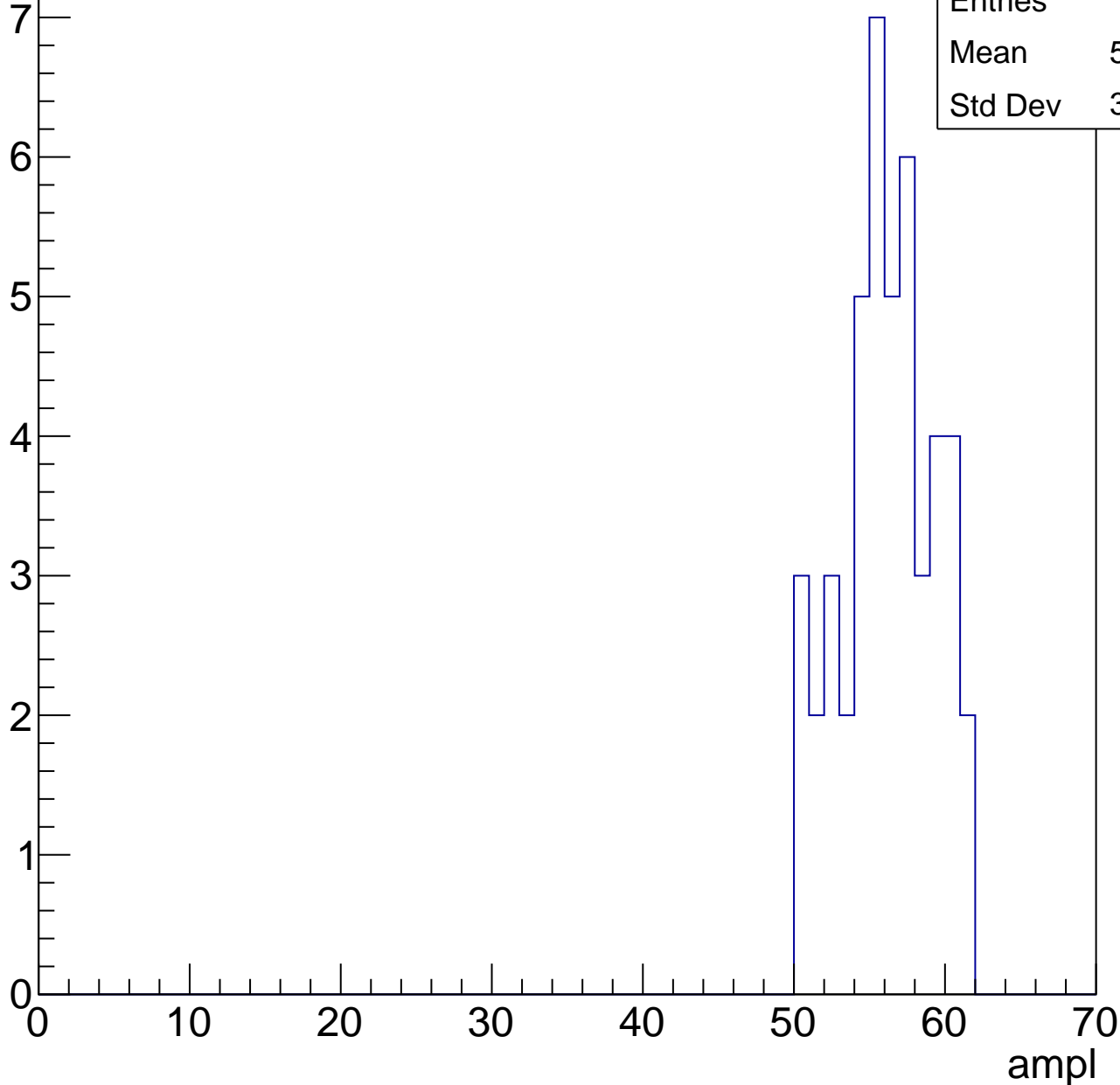
Entries	75
Mean	50.39
Std Dev	3.936



# B1L103S, U16-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

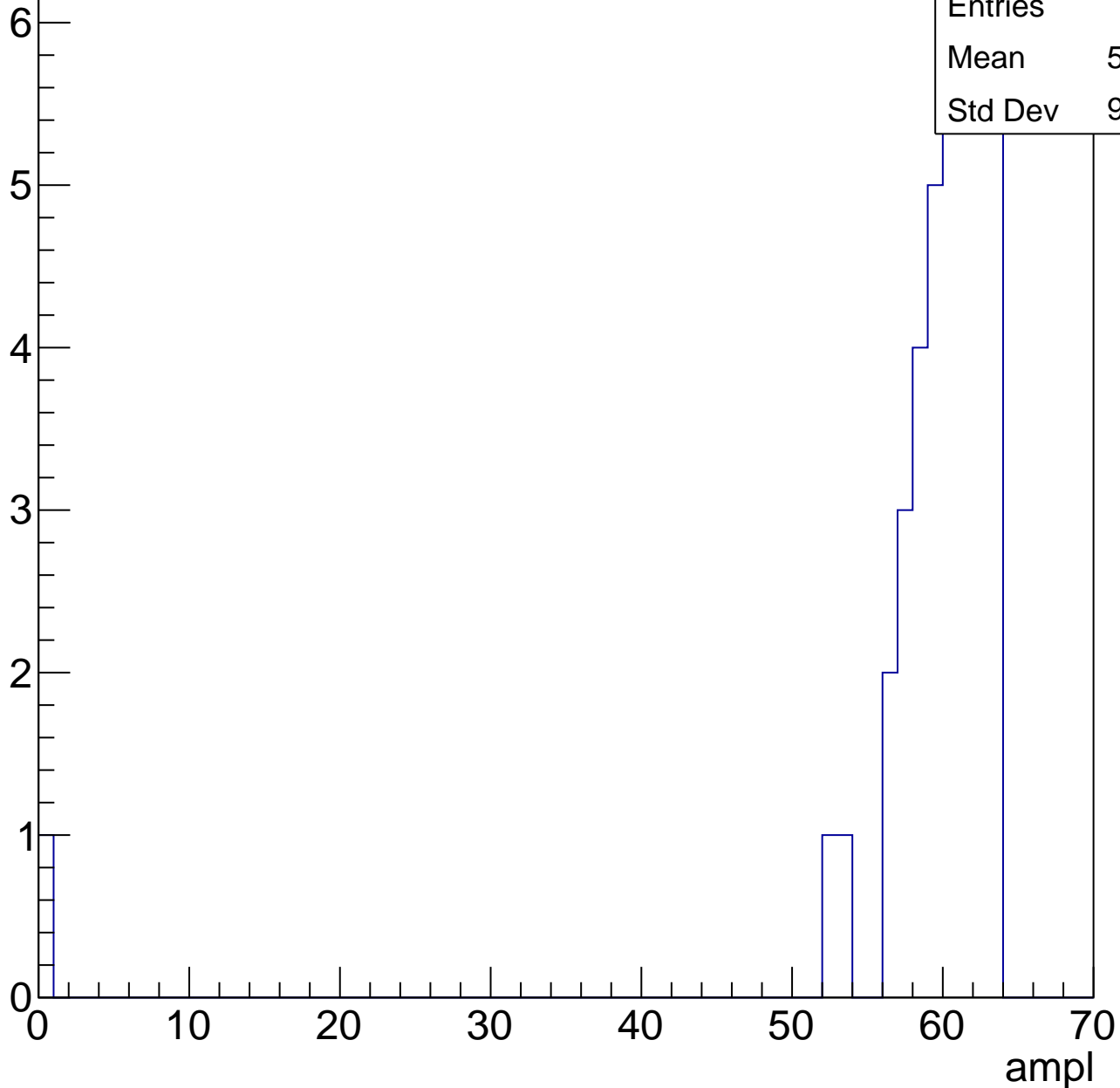


Entries	46
Mean	55.72
Std Dev	3.005

# B1L103S, U16-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

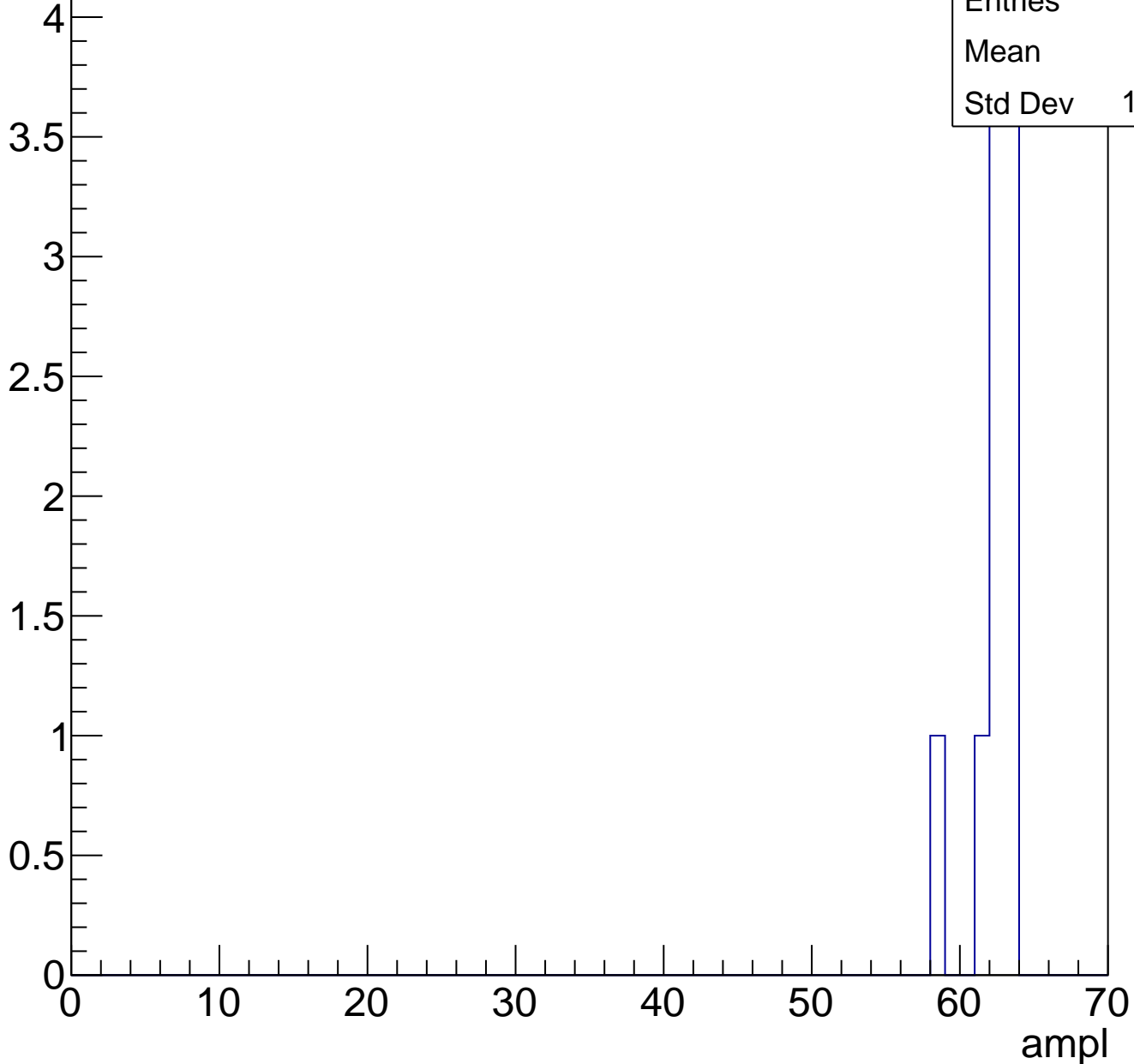
Entry



# B1L103S, U16-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U16-ch33, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	75
Mean	29
Std Dev	5.2

**Gaus mean : 29.8683**

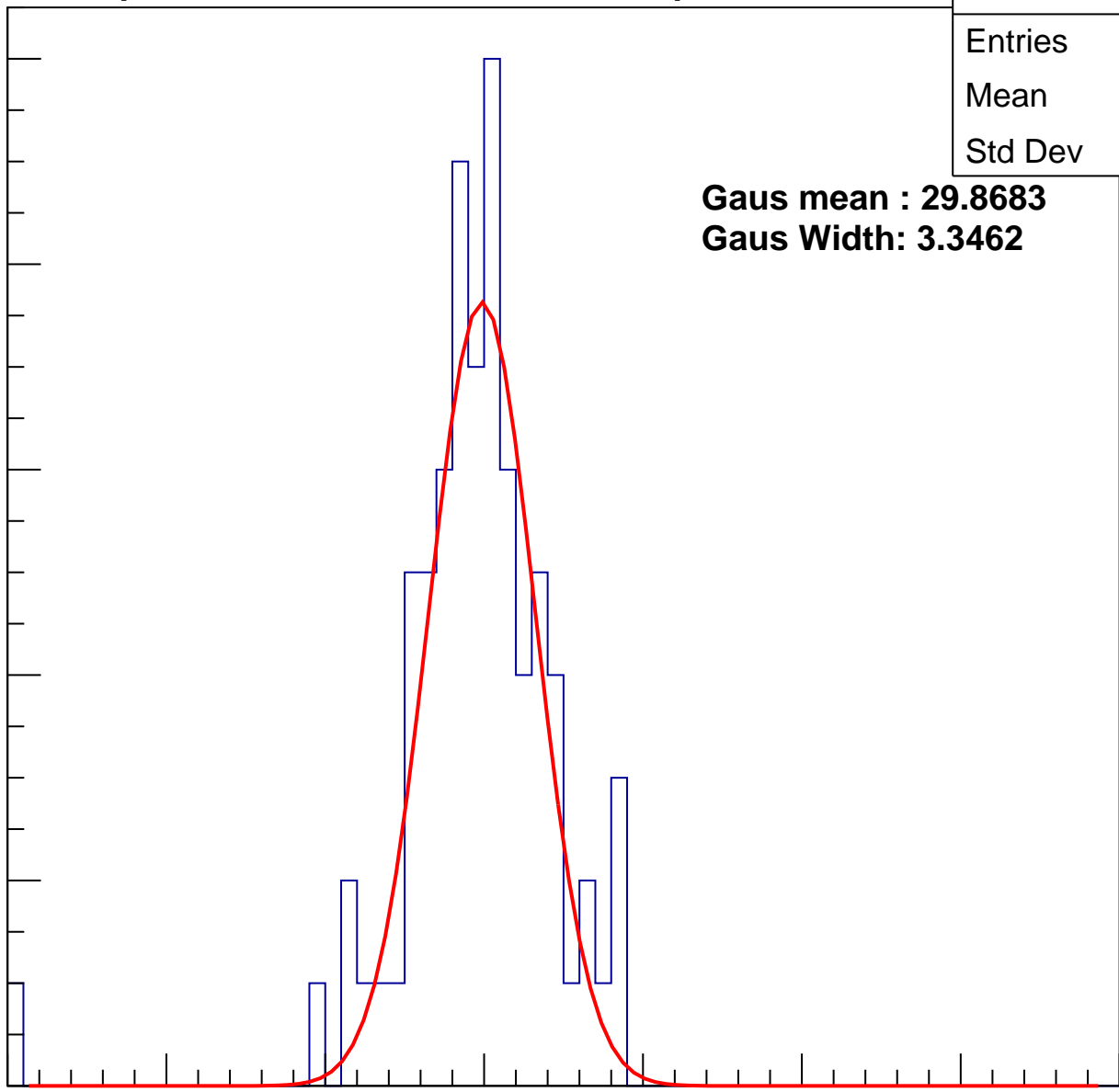
**Gaus Width: 3.3462**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U16-ch33, adc1

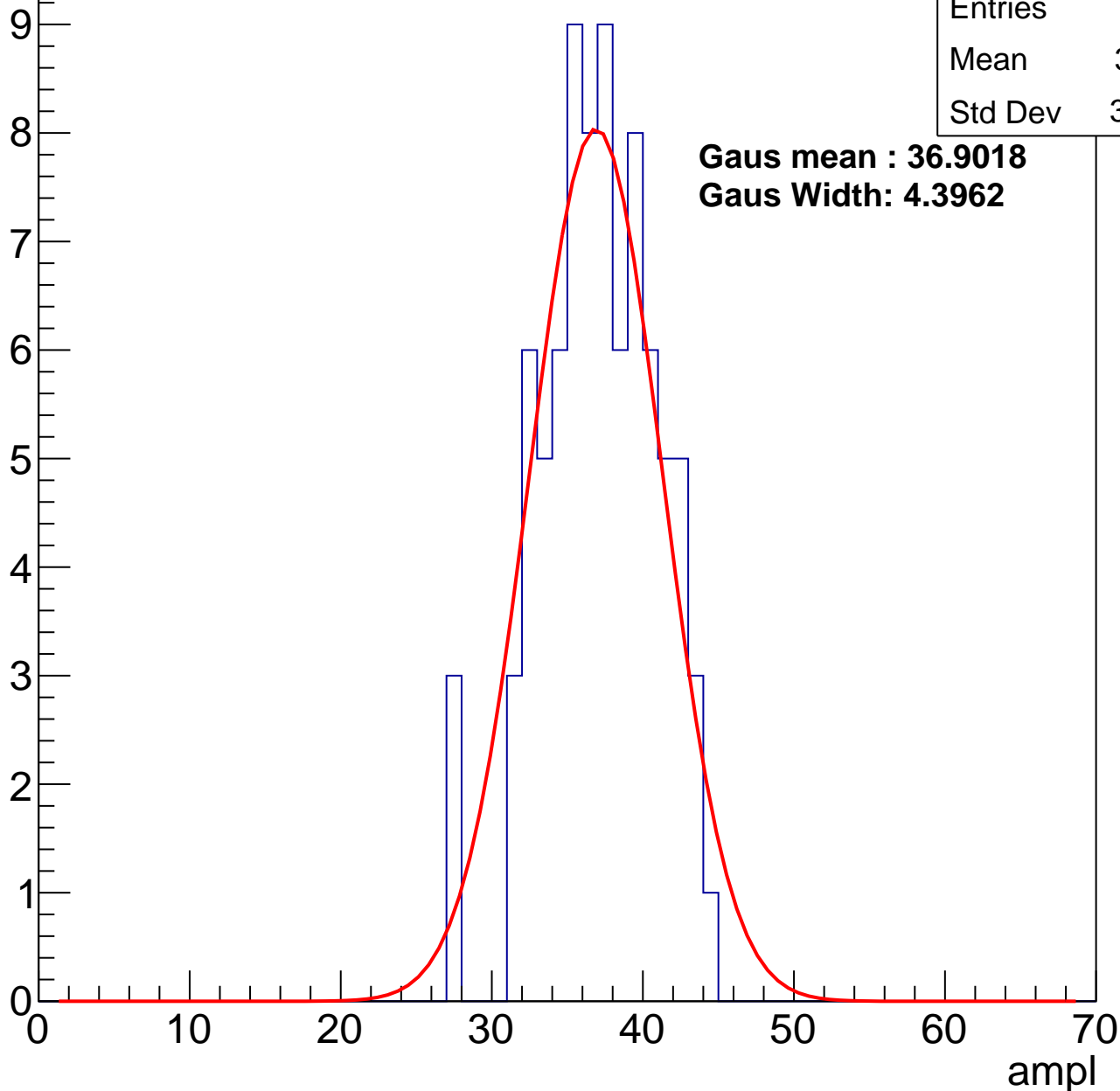
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	36.61
Std Dev	3.767

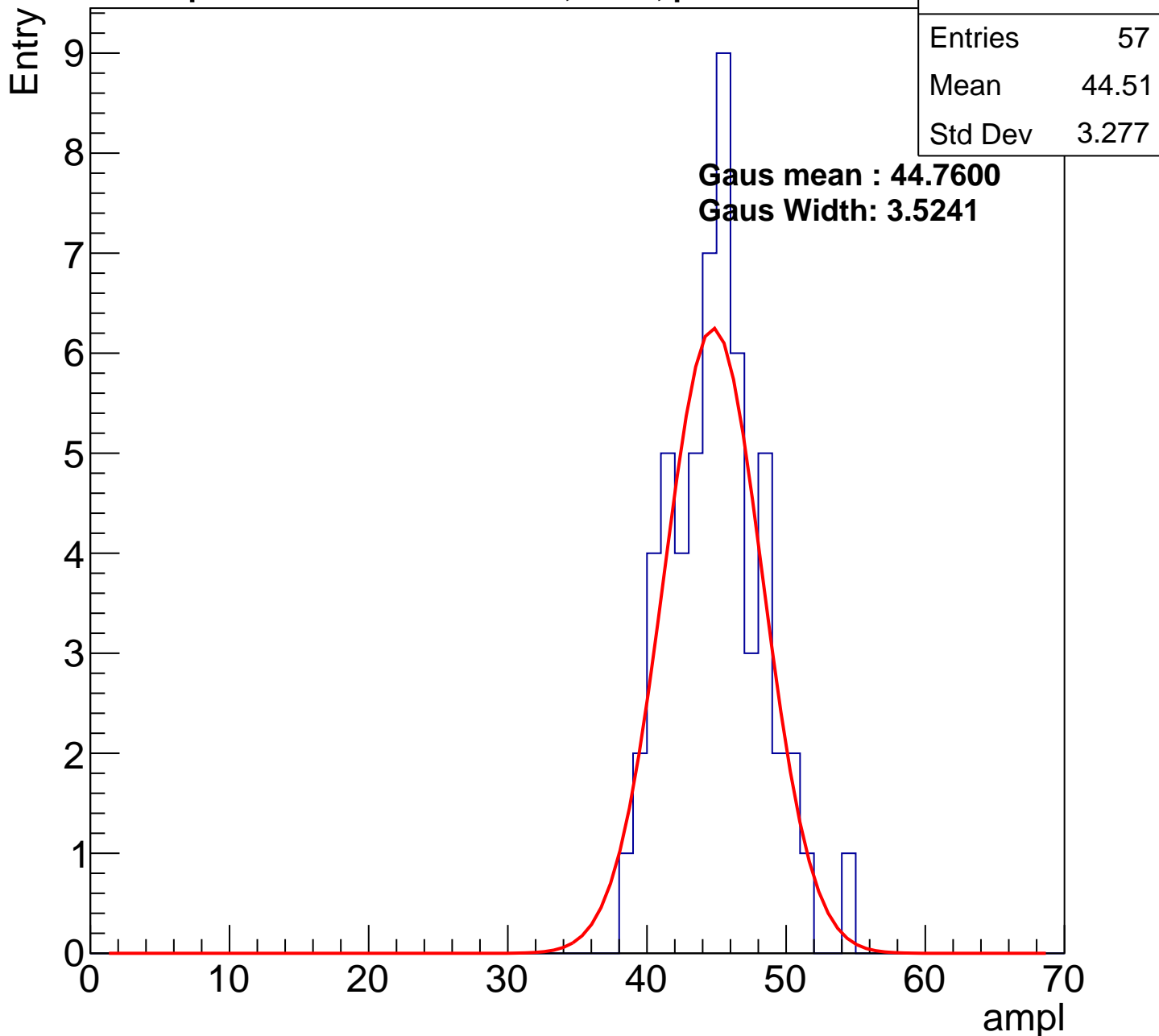
**Gaus mean : 36.9018**

**Gaus Width: 4.3962**



# B1L103S, U16-ch33, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

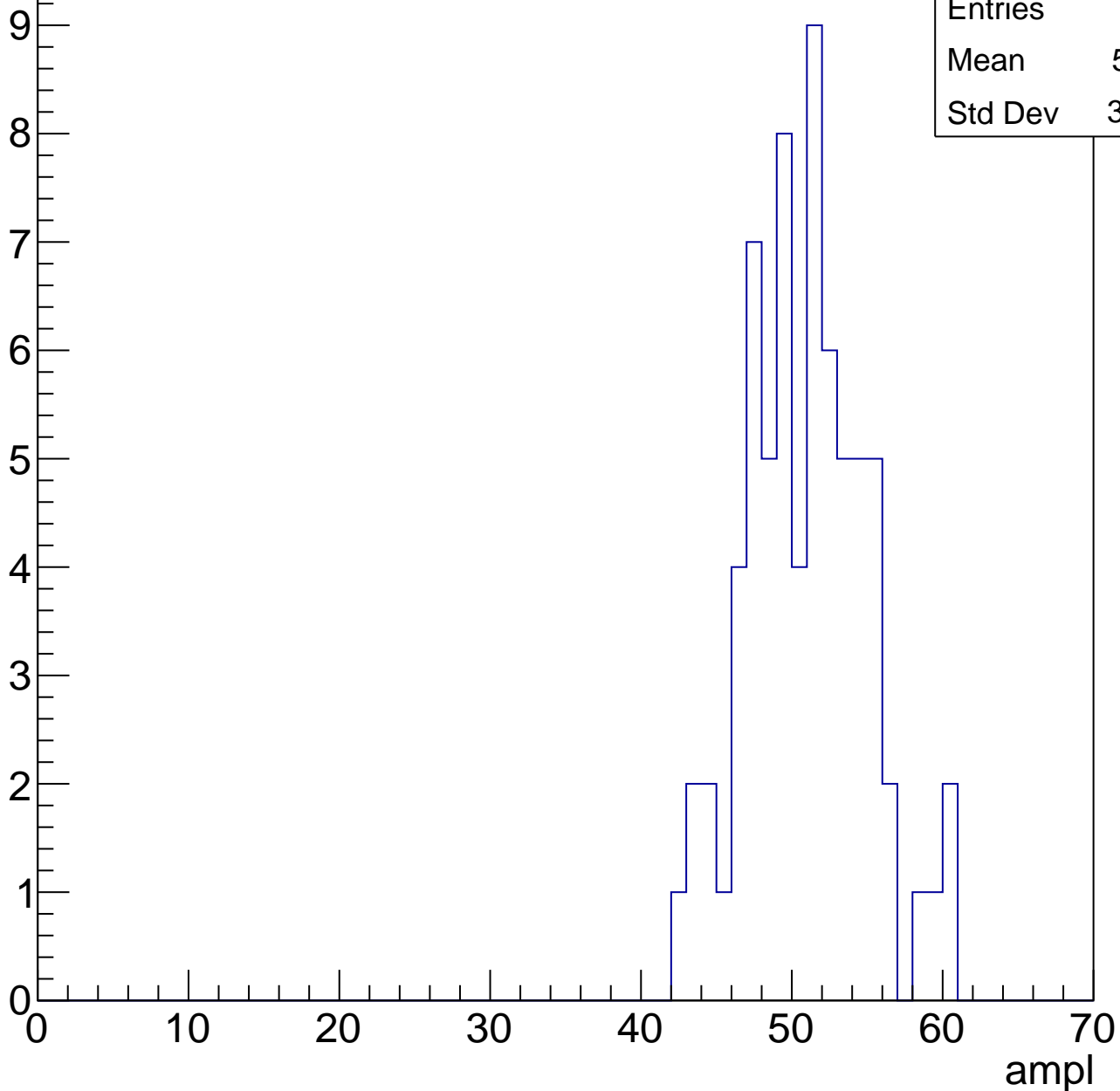


# B1L103S, U16-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

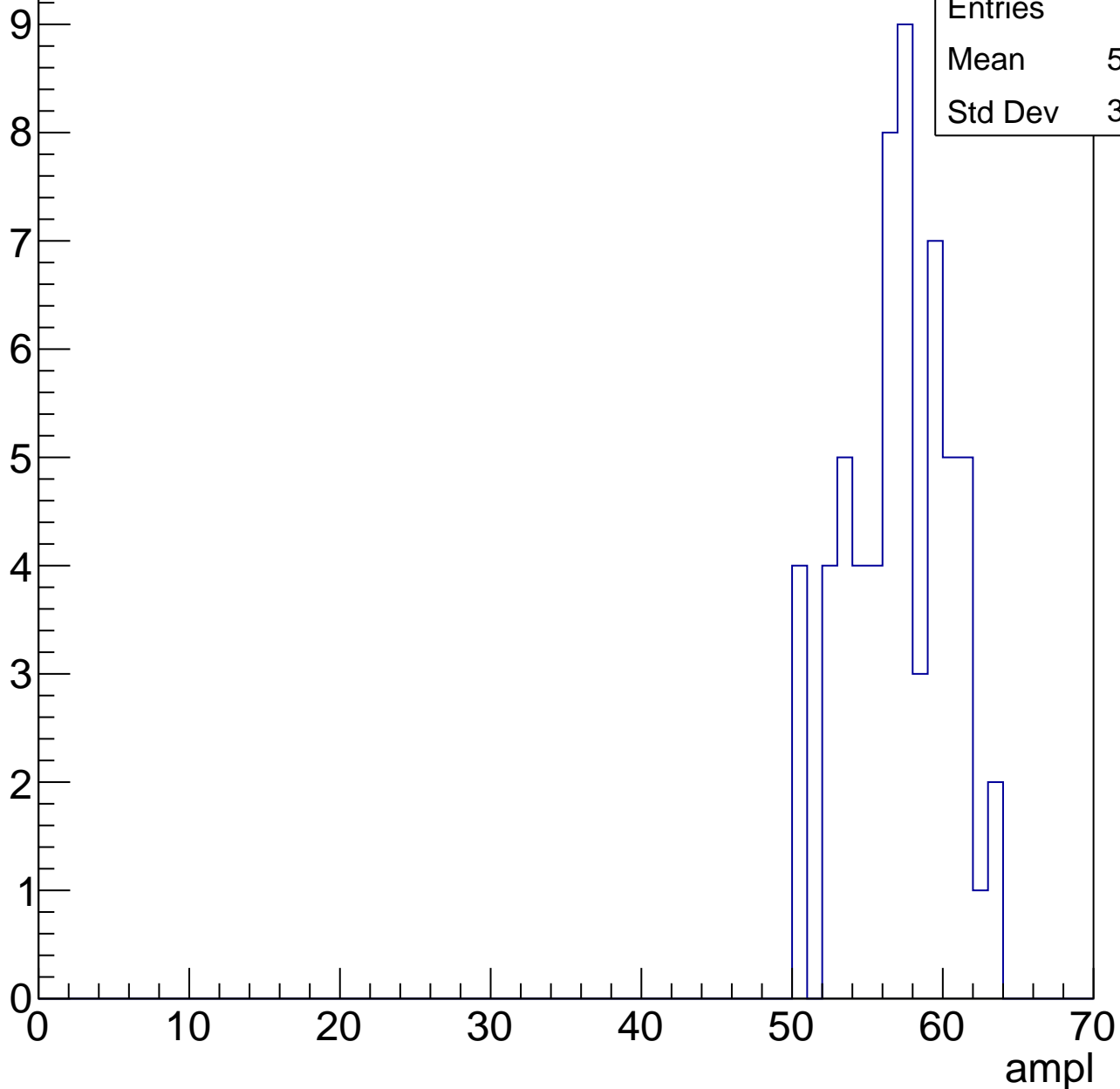
Entries	70
Mean	50.51
Std Dev	3.956



# B1L103S, U16-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

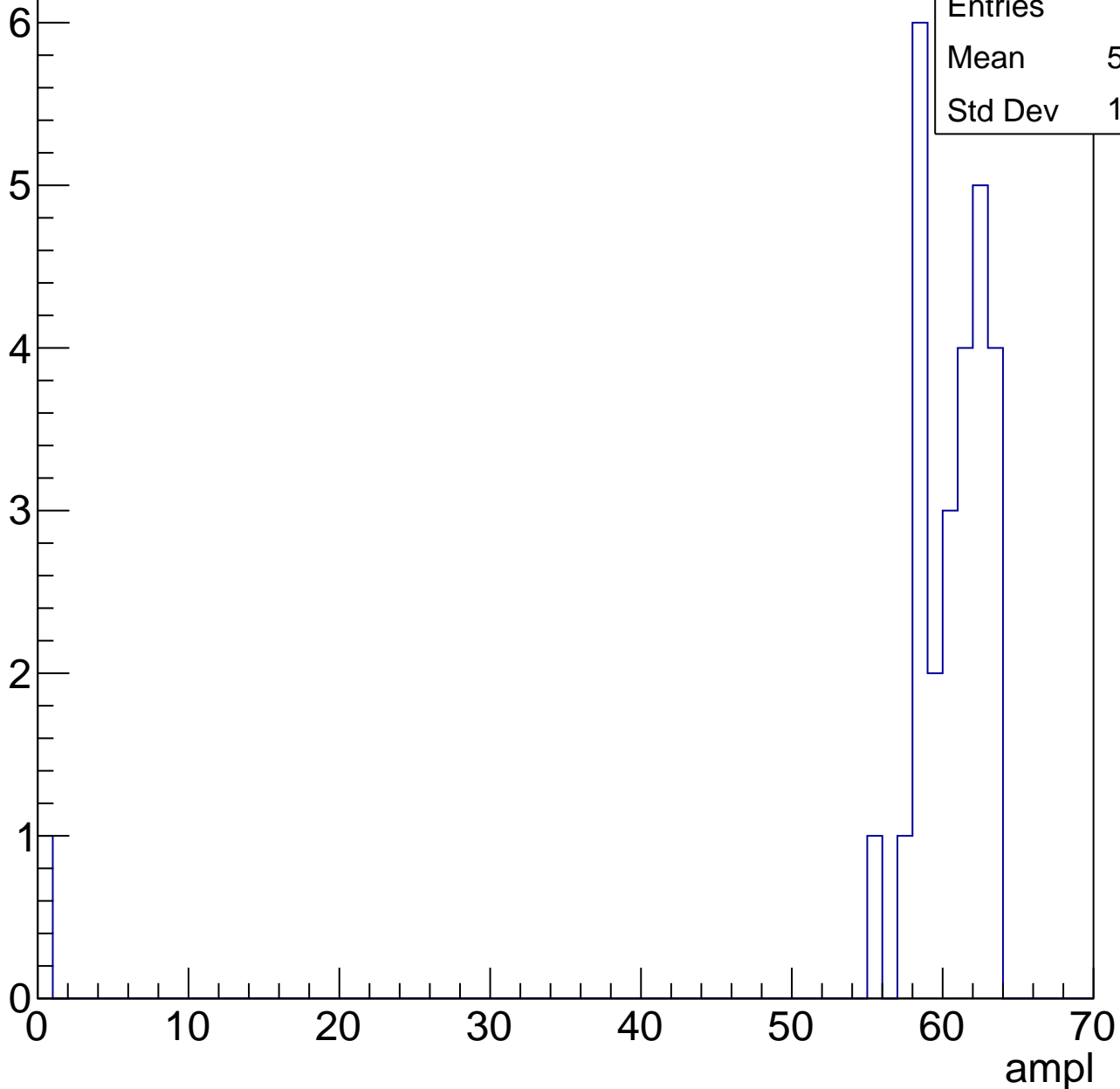


# B1L103S, U16-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

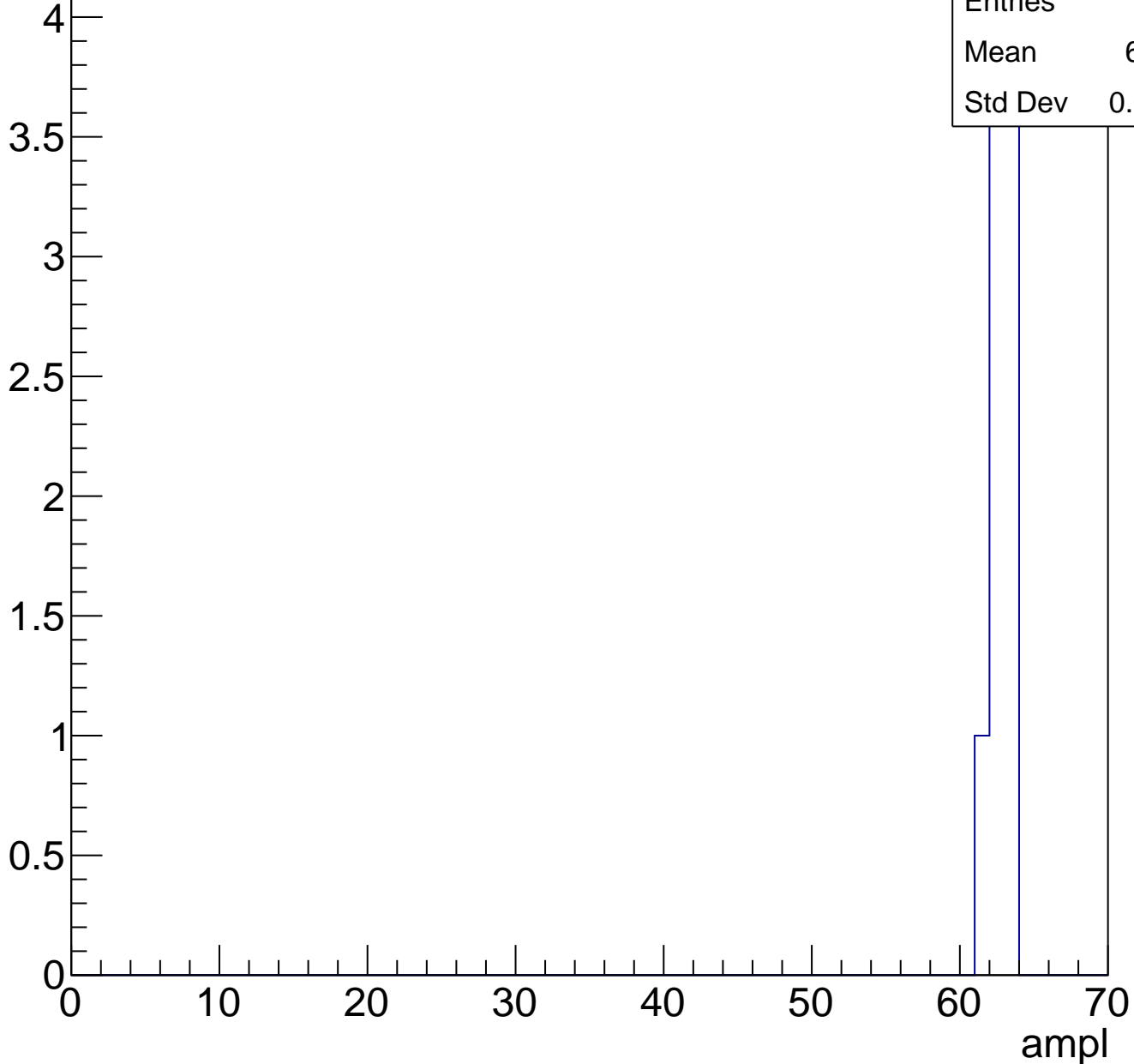
Entries	27
Mean	57.93
Std Dev	11.55



# B1L103S, U16-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U16-ch34, adc0

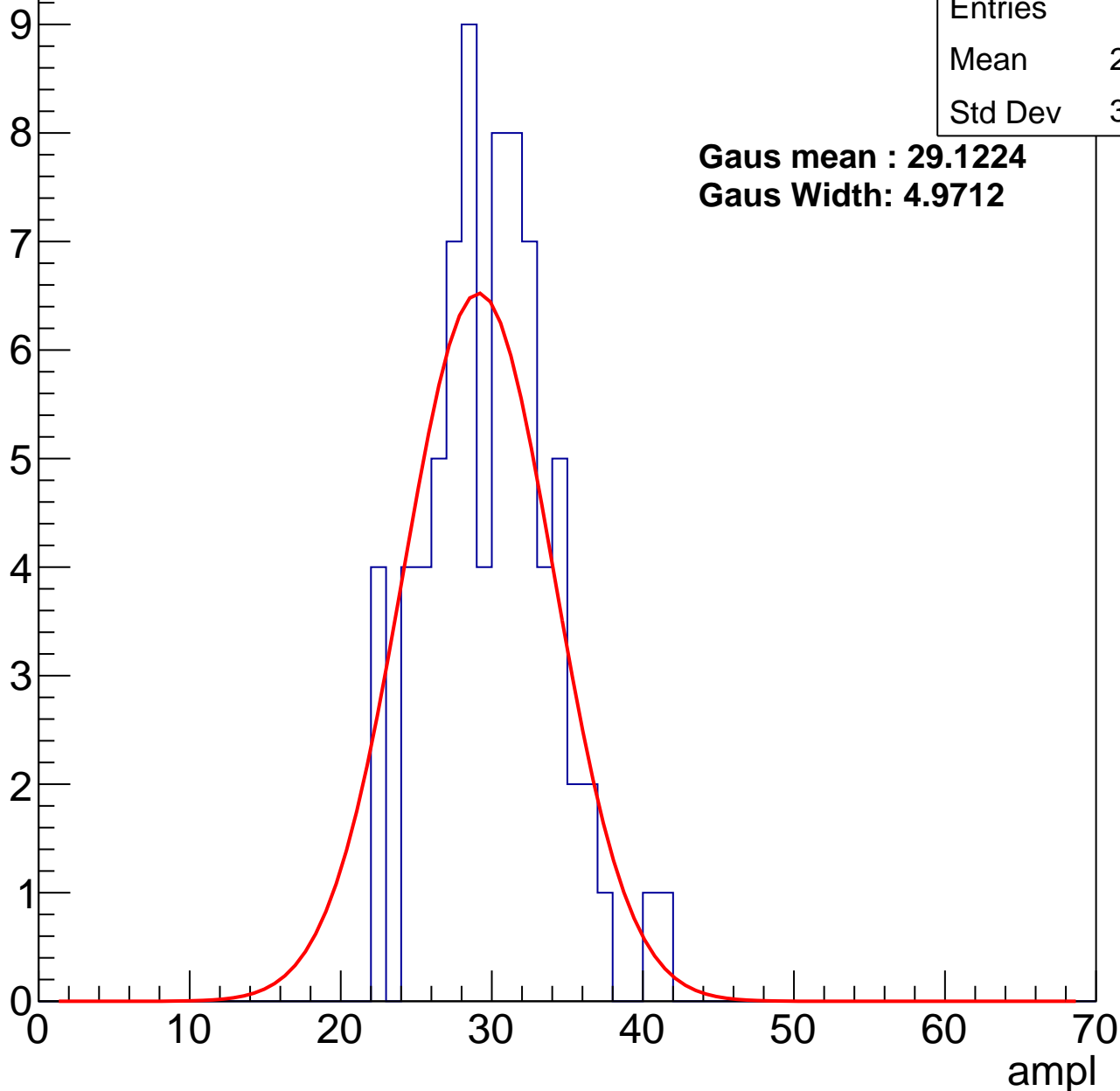
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	29.54
Std Dev	3.992

**Gaus mean : 29.1224**

**Gaus Width: 4.9712**



# B1L103S, U16-ch34, adc1

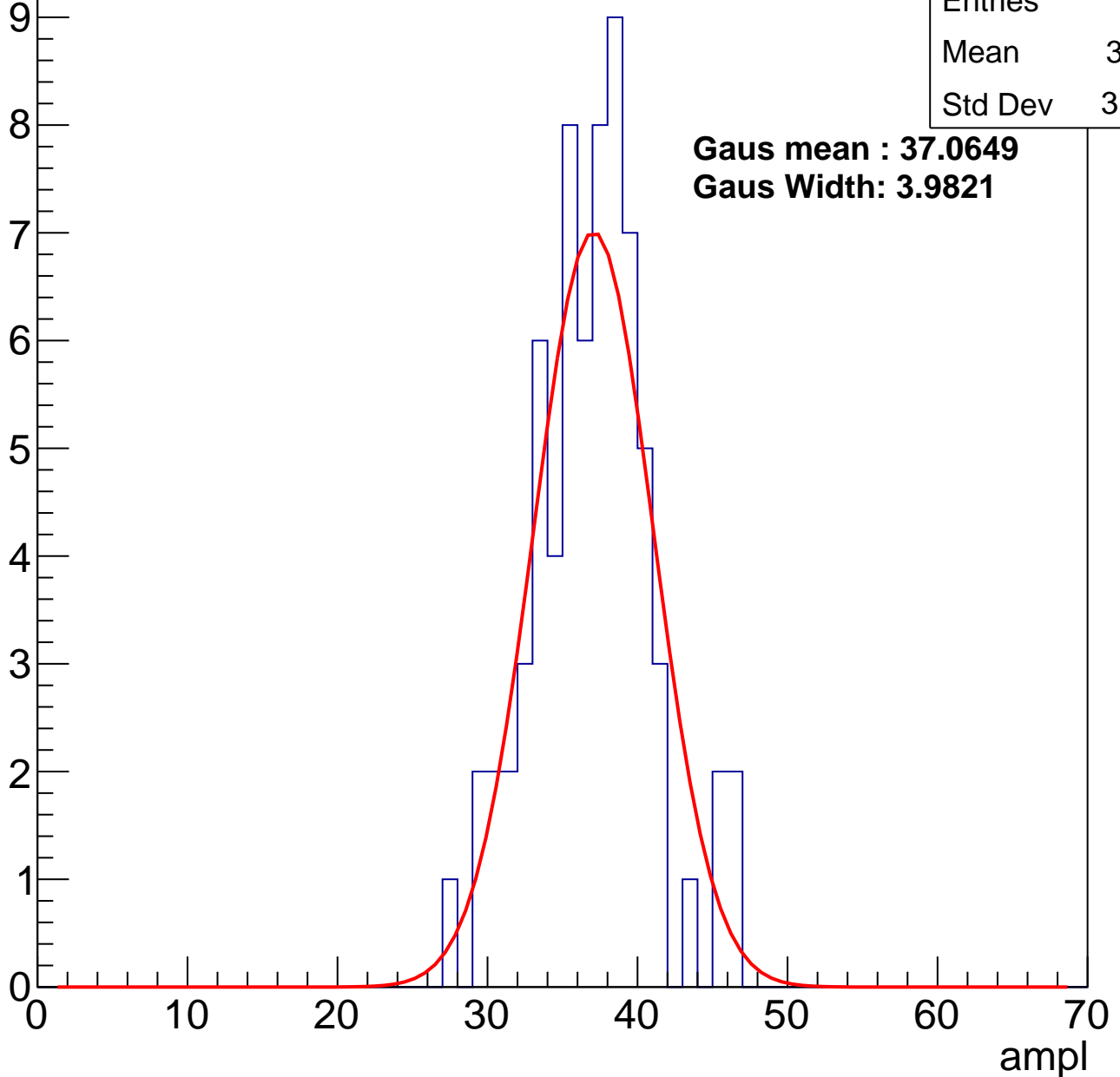
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	36.51
Std Dev	3.903

**Gaus mean : 37.0649**

**Gaus Width: 3.9821**



# B1L103S, U16-ch34, adc2

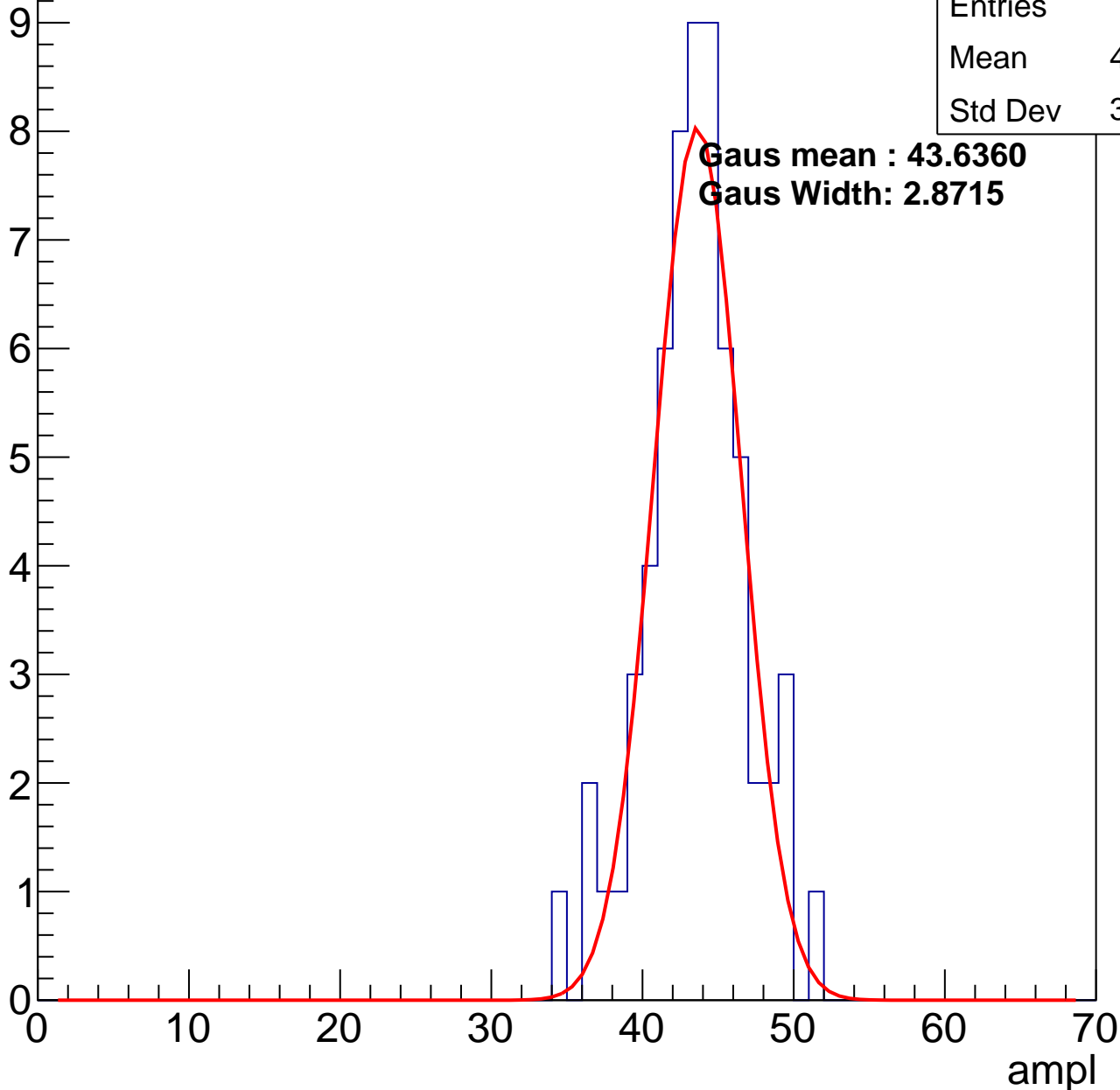
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	43.03
Std Dev	3.304

**Gaus mean : 43.6360**

**Gaus Width: 2.8715**

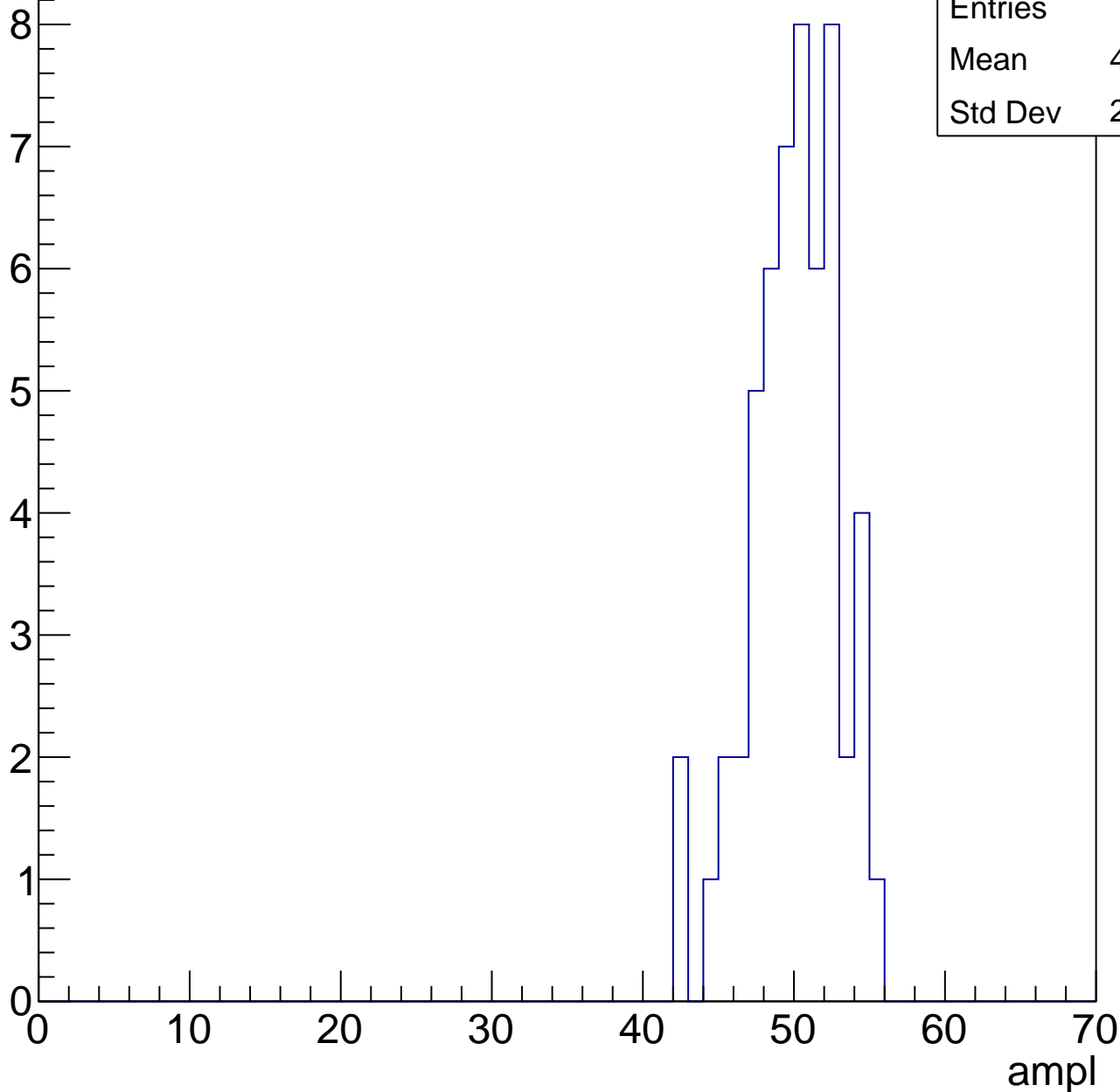


# B1L103S, U16-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	49.54
Std Dev	2.904

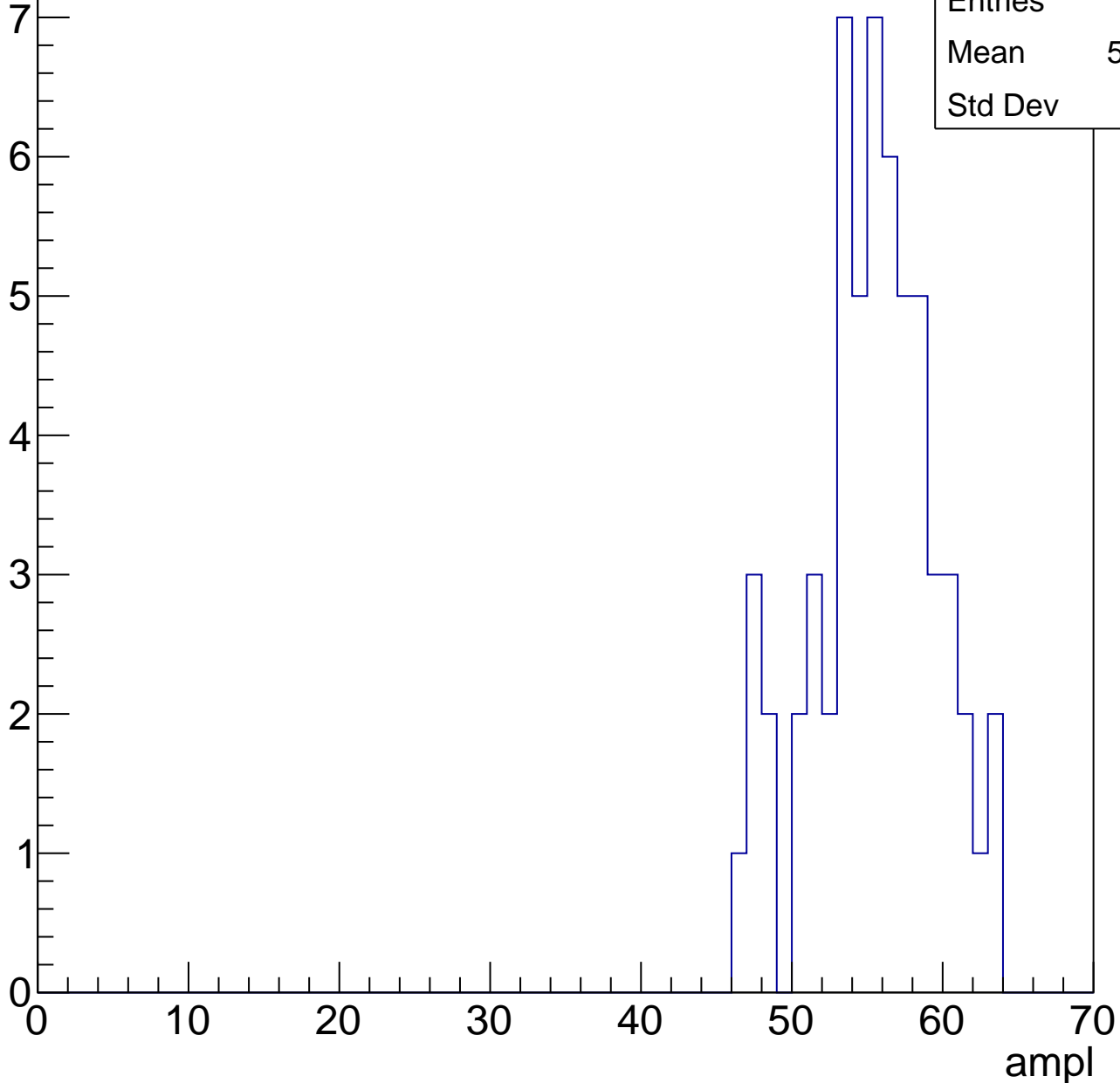


# B1L103S, U16-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	54.98
Std Dev	4.04

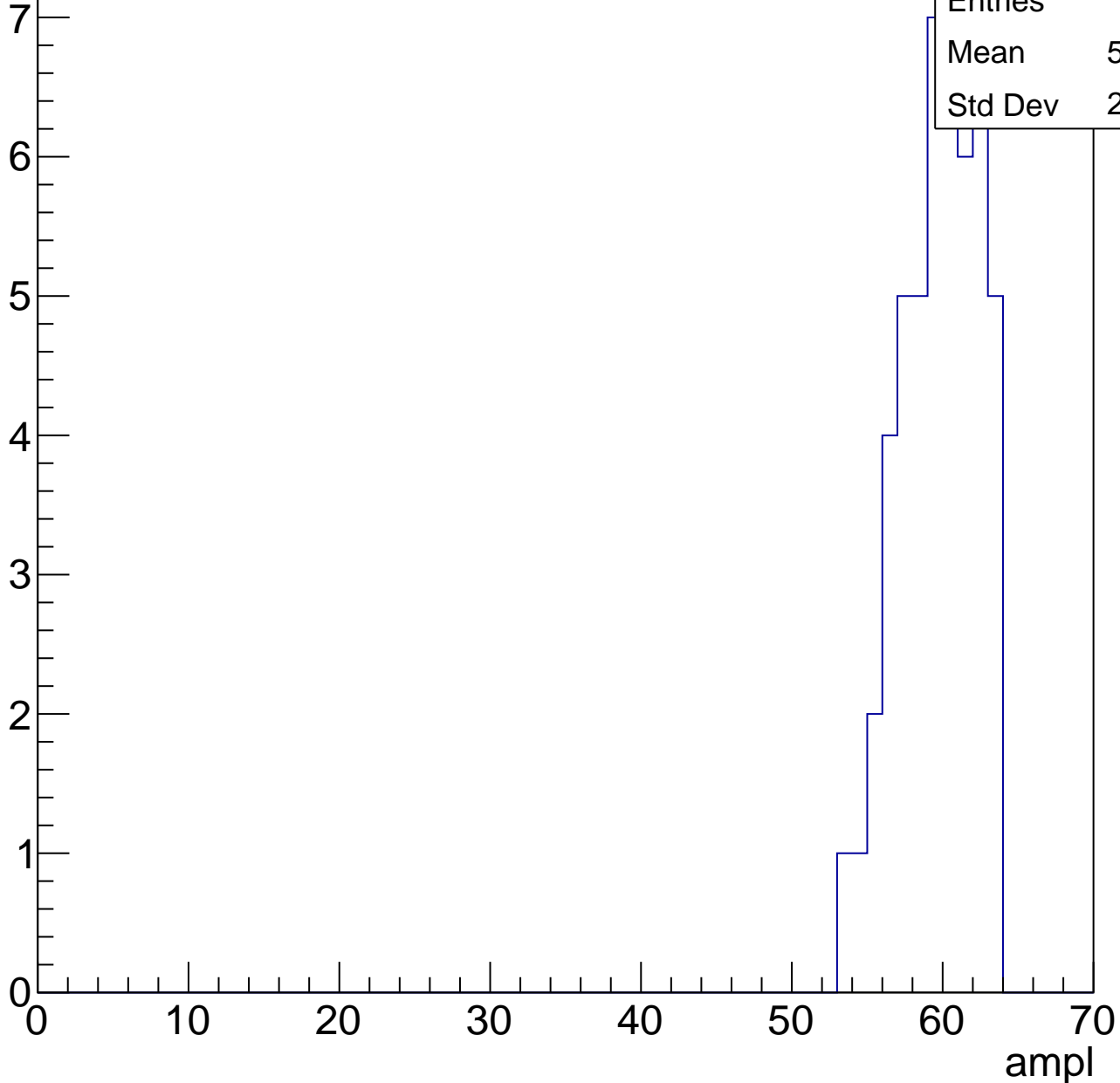


# B1L103S, U16-ch34, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

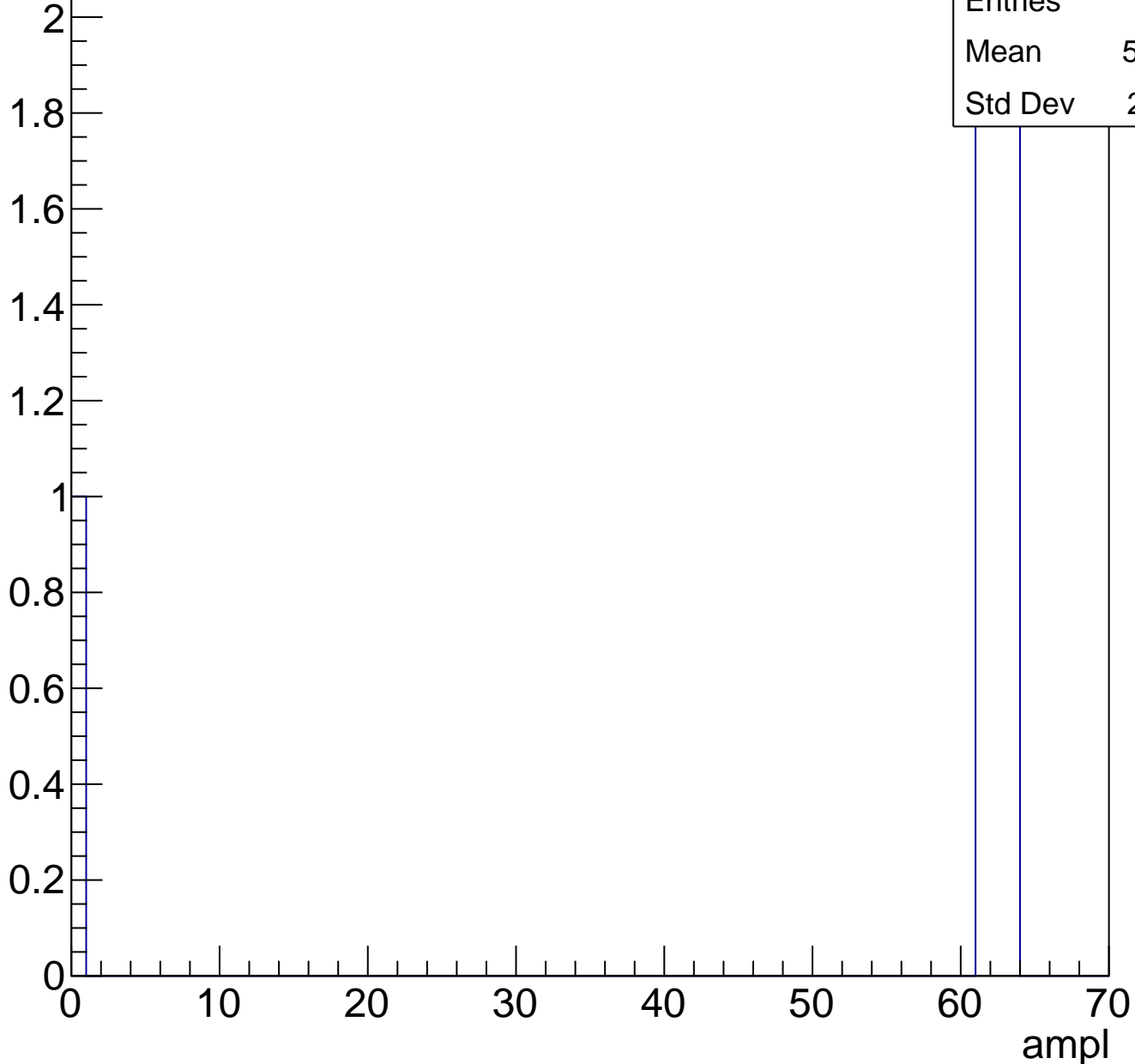
Entries	50
Mean	59.28
Std Dev	2.546



# B1L103S, U16-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	42.5
Std Dev	20.5

ampl

# B1L103S, U16-ch35, adc0

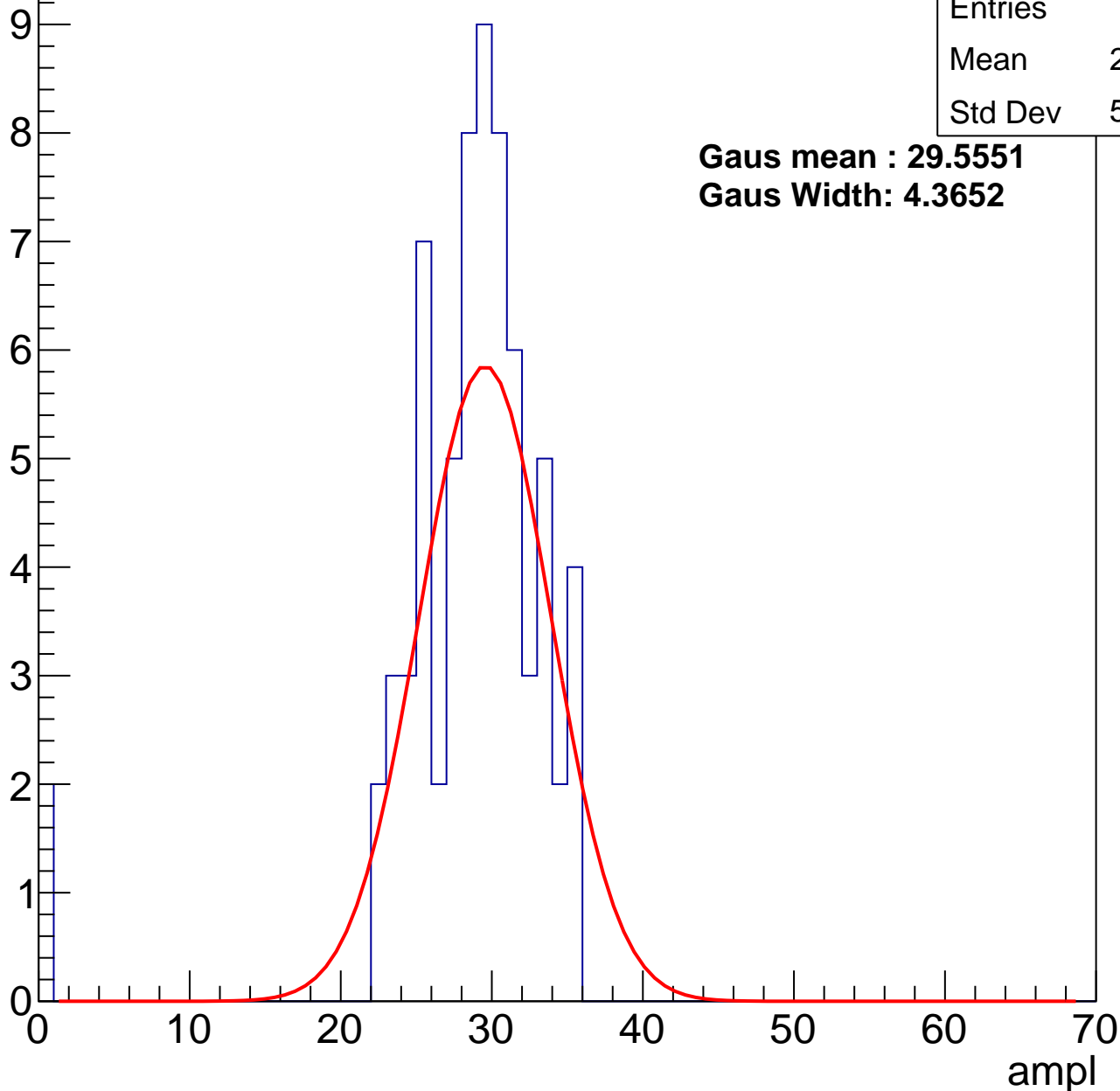
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	27.93
Std Dev	5.866

**Gaus mean : 29.5551**

**Gaus Width: 4.3652**



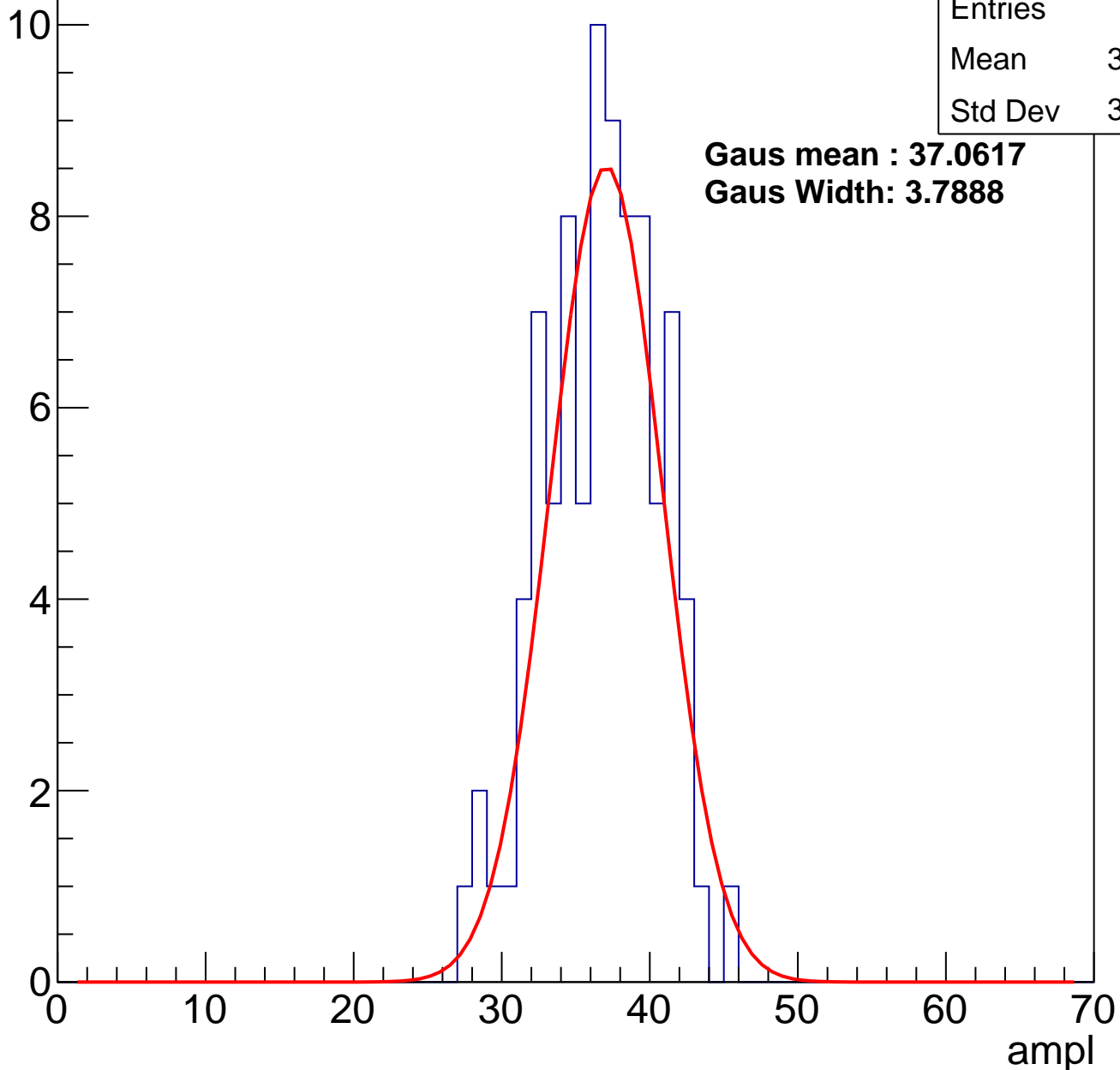
# B1L103S, U16-ch35, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	87
Mean	36.25
Std Dev	3.752

**Gaus mean : 37.0617**  
**Gaus Width: 3.7888**

Entry



# B1L103S, U16-ch35, adc2

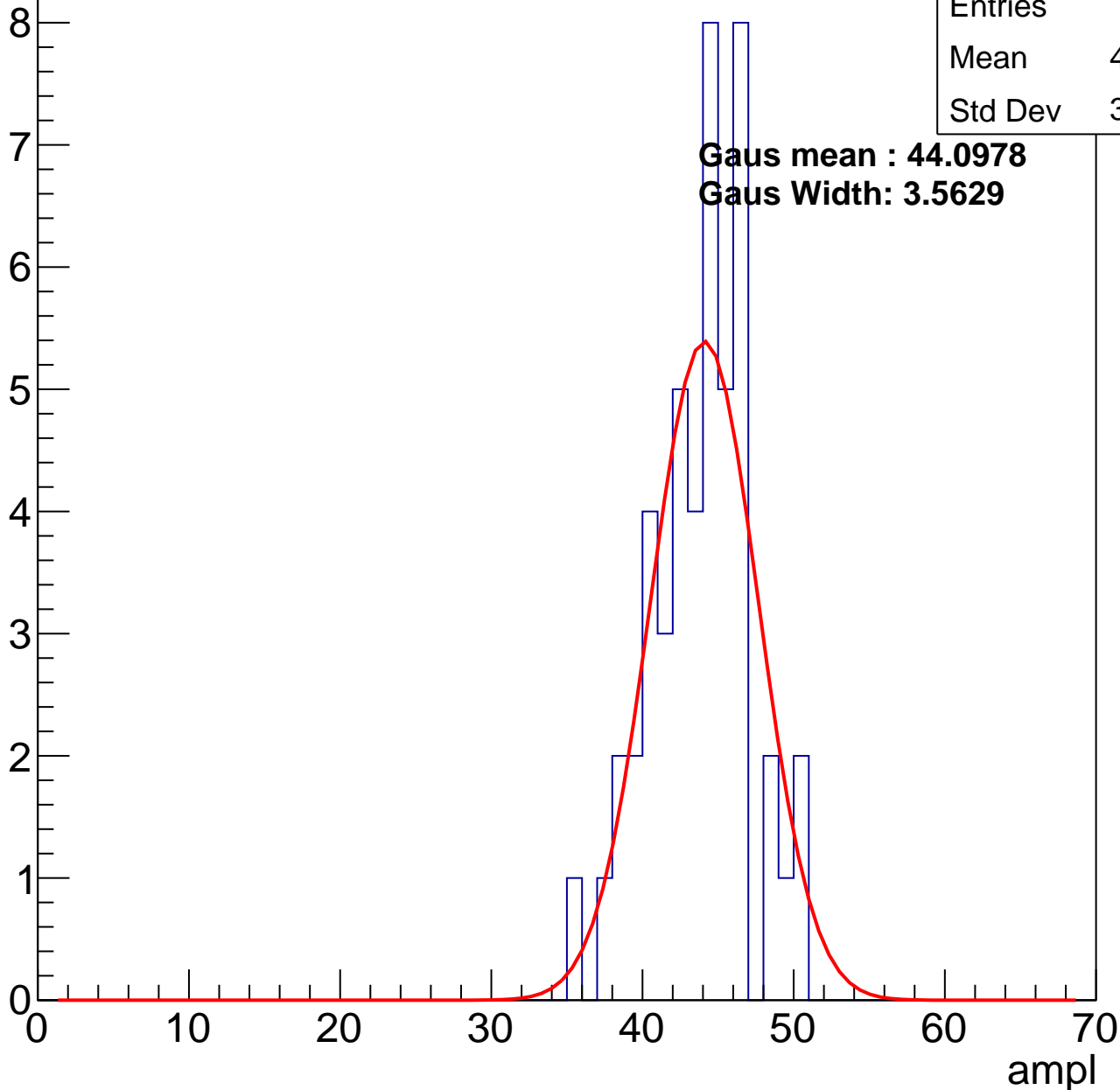
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	43.35
Std Dev	3.269

**Gaus mean : 44.0978**

**Gaus Width: 3.5629**



# B1L103S, U16-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

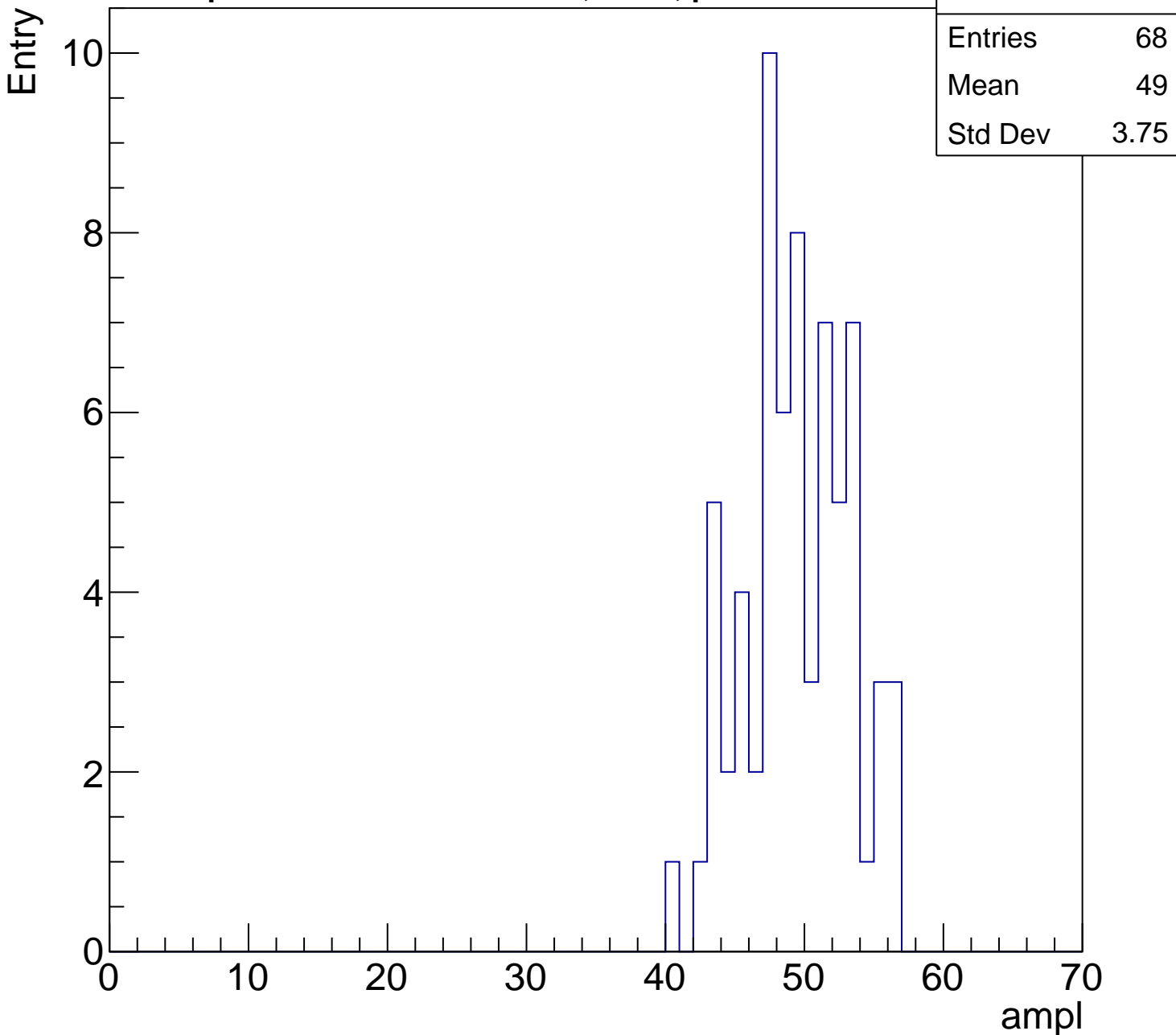
Entries	68
Mean	49
Std Dev	3.75

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

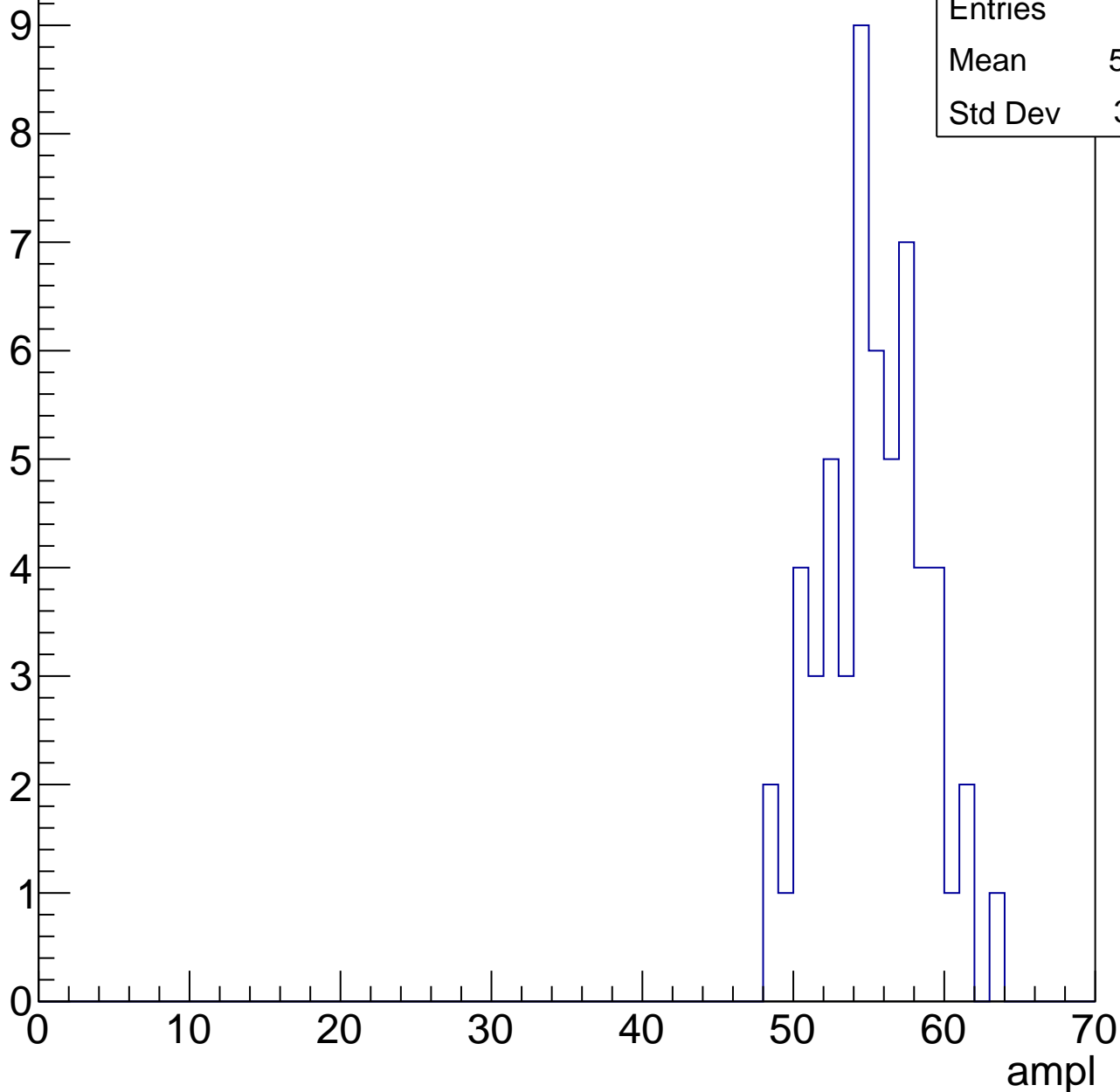


# B1L103S, U16-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	54.82
Std Dev	3.351

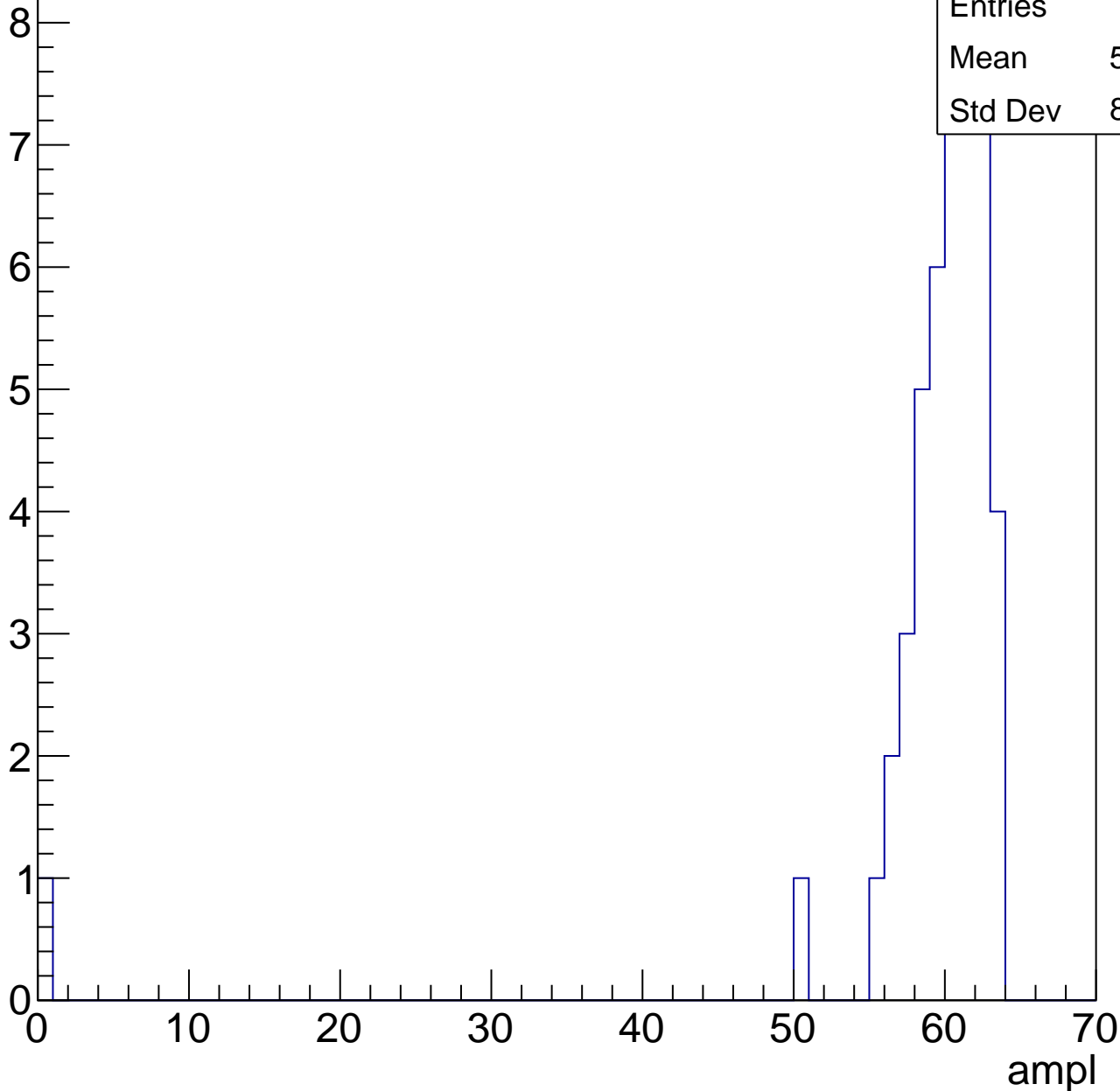


# B1L103S, U16-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	58.47
Std Dev	8.963

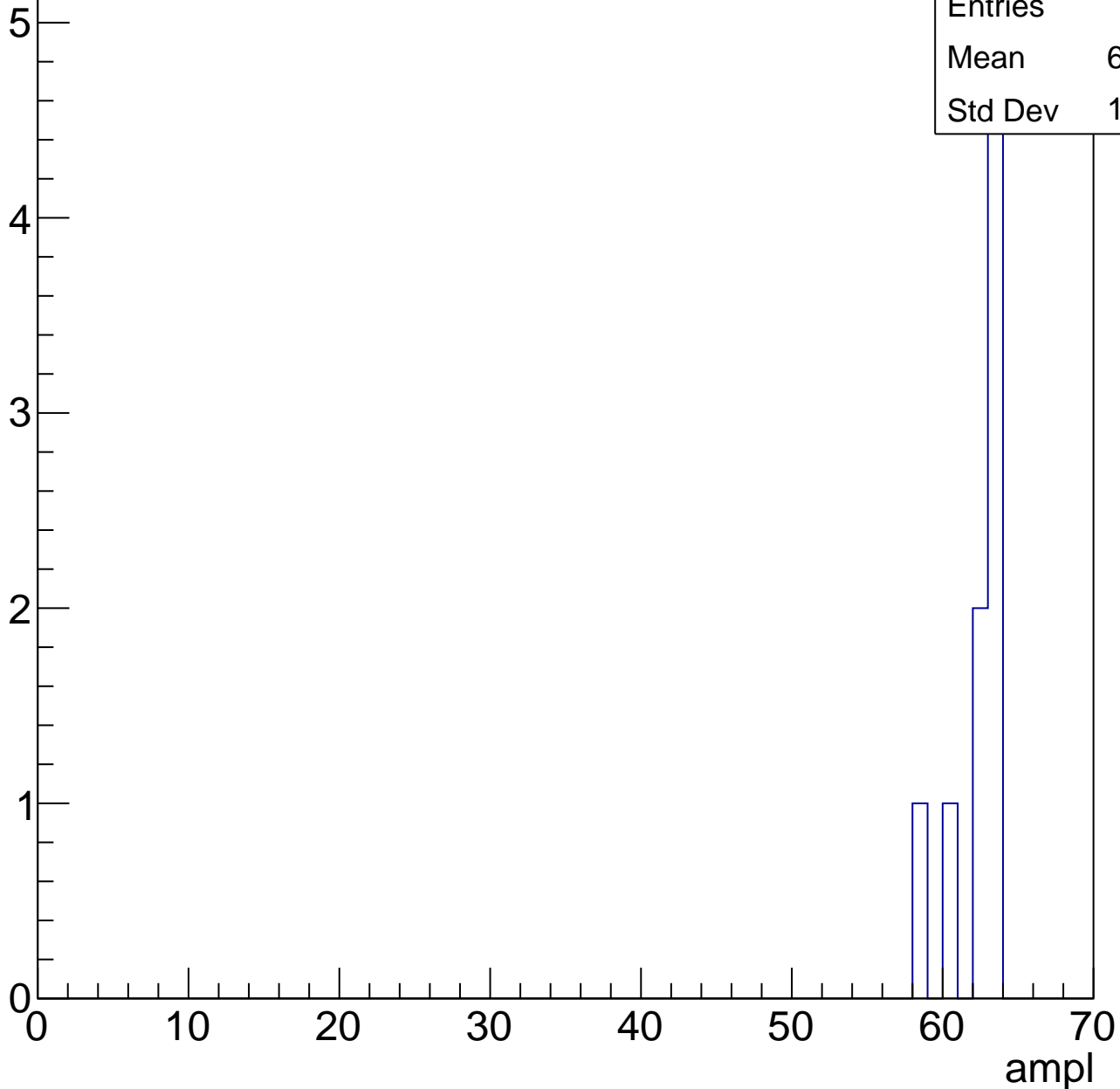


# B1L103S, U16-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	9
Mean	61.89
Std Dev	1.663





# B1L103S, U16-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U16-ch36, adc0

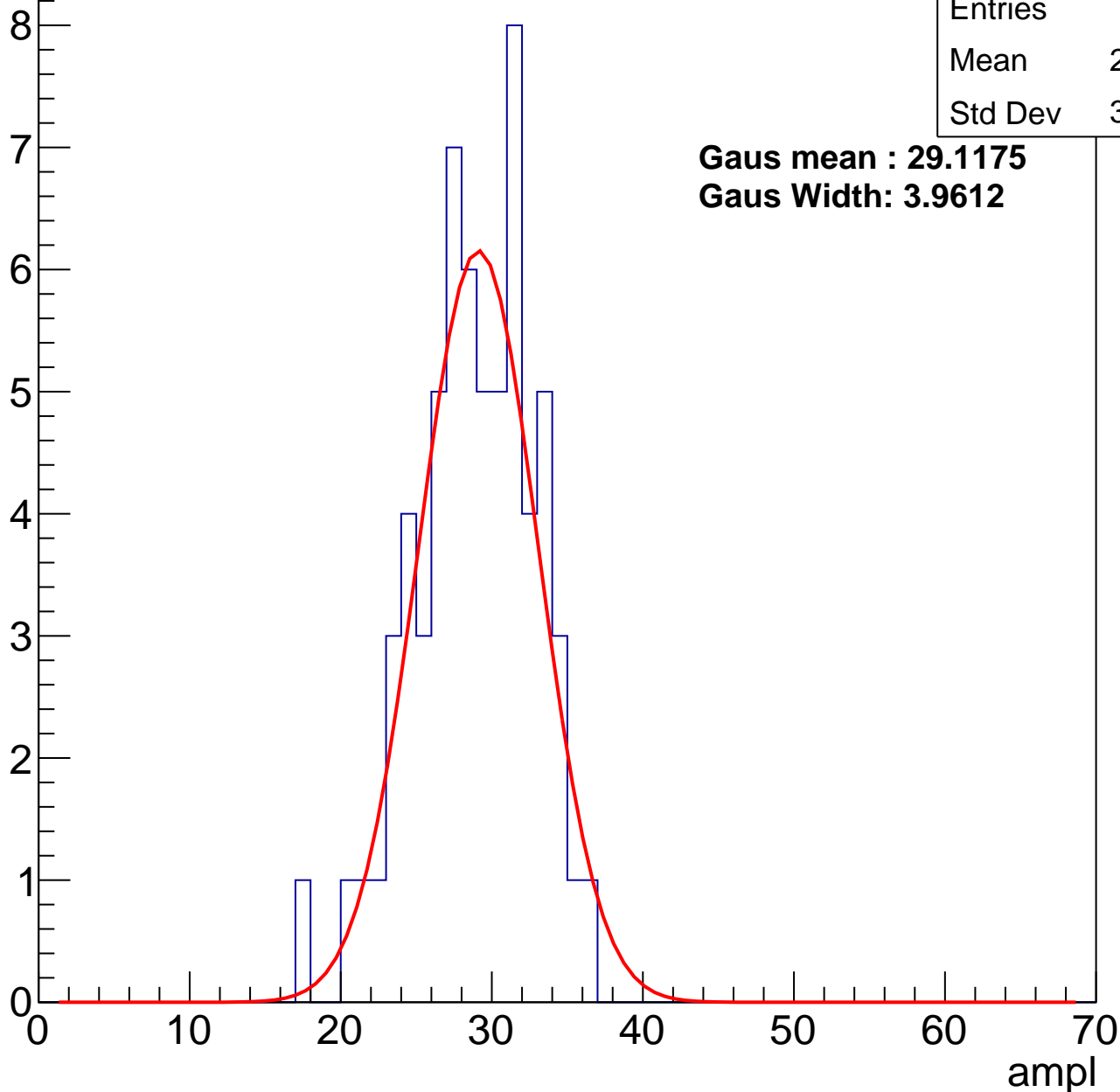
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	28.38
Std Dev	3.875

**Gaus mean : 29.1175**

**Gaus Width: 3.9612**



# B1L103S, U16-ch36, adc1

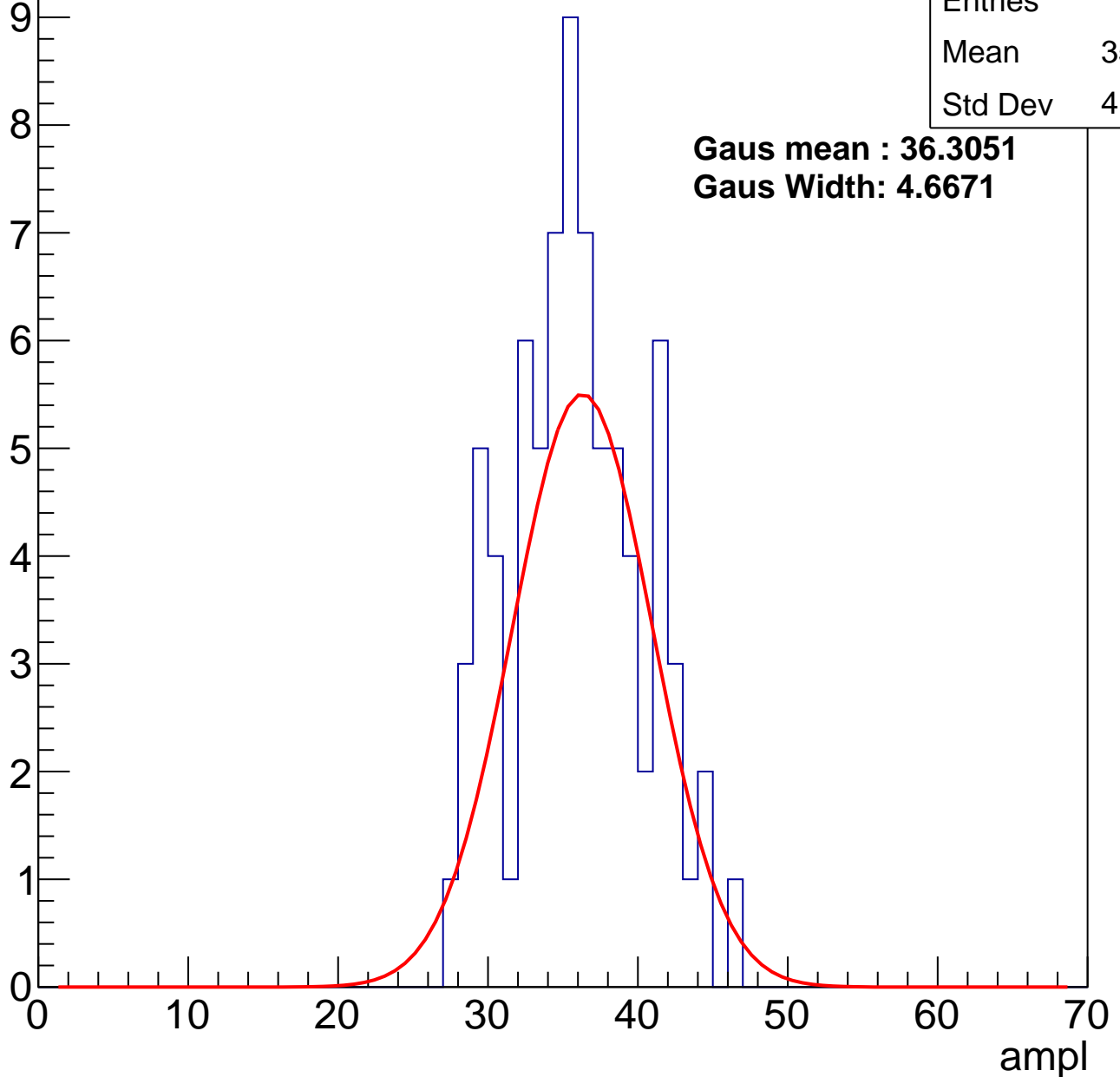
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	35.44
Std Dev	4.368

**Gaus mean : 36.3051**

**Gaus Width: 4.6671**



# B1L103S, U16-ch36, adc2

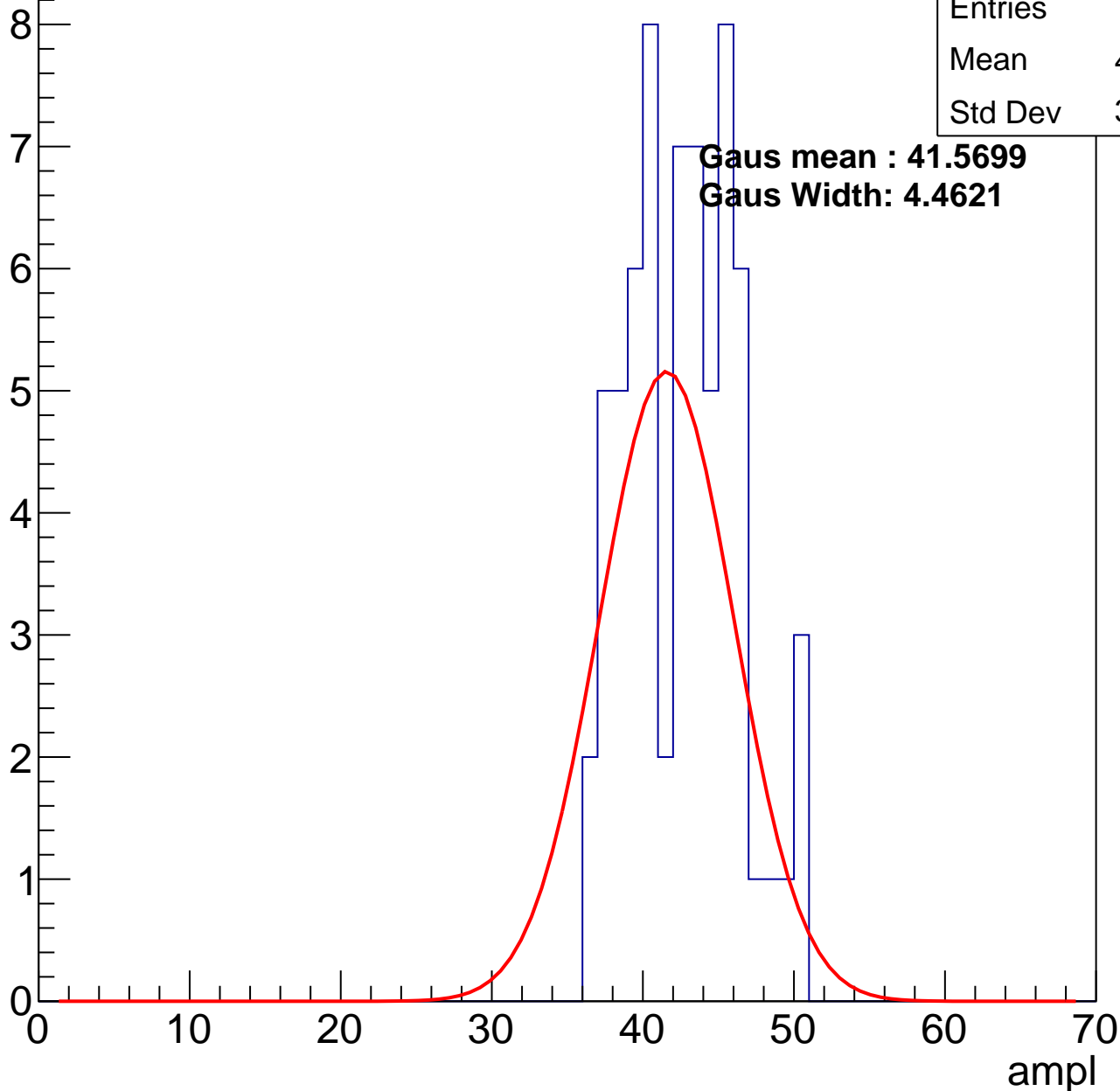
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	42.21
Std Dev	3.581

**Gaus mean : 41.5699**

**Gaus Width: 4.4621**

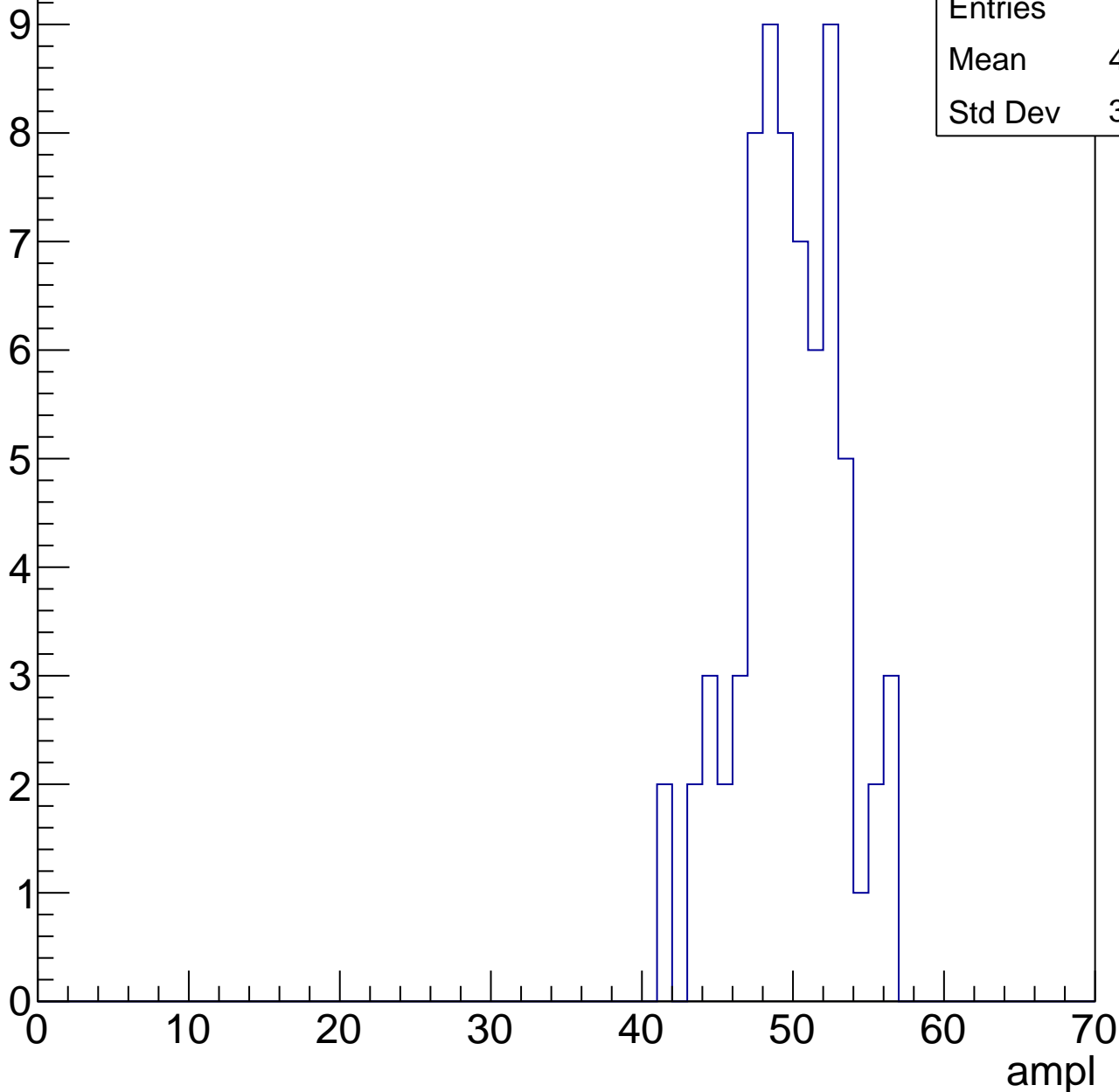


# B1L103S, U16-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	49.27
Std Dev	3.393

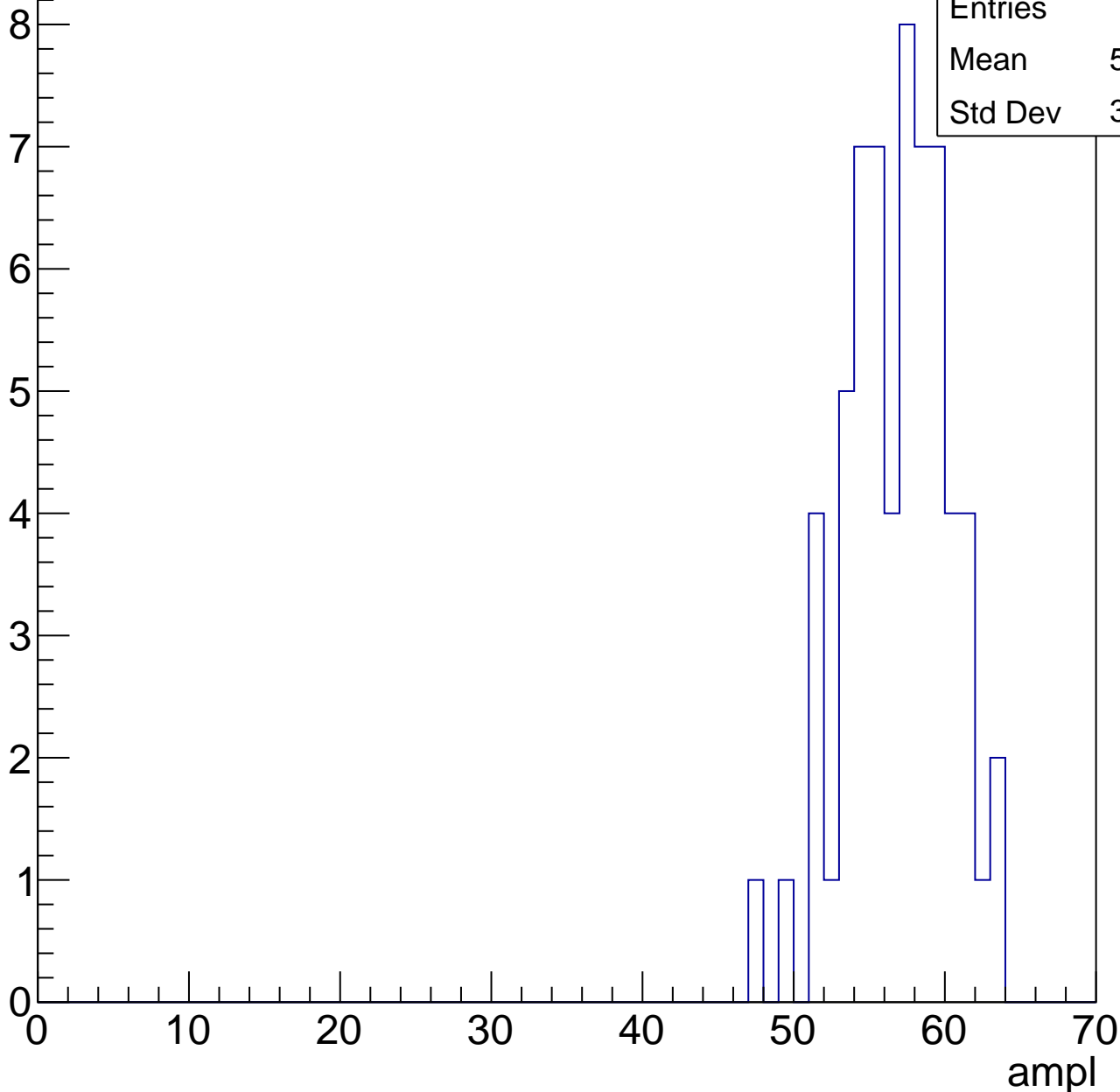


# B1L103S, U16-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	56.37
Std Dev	3.368

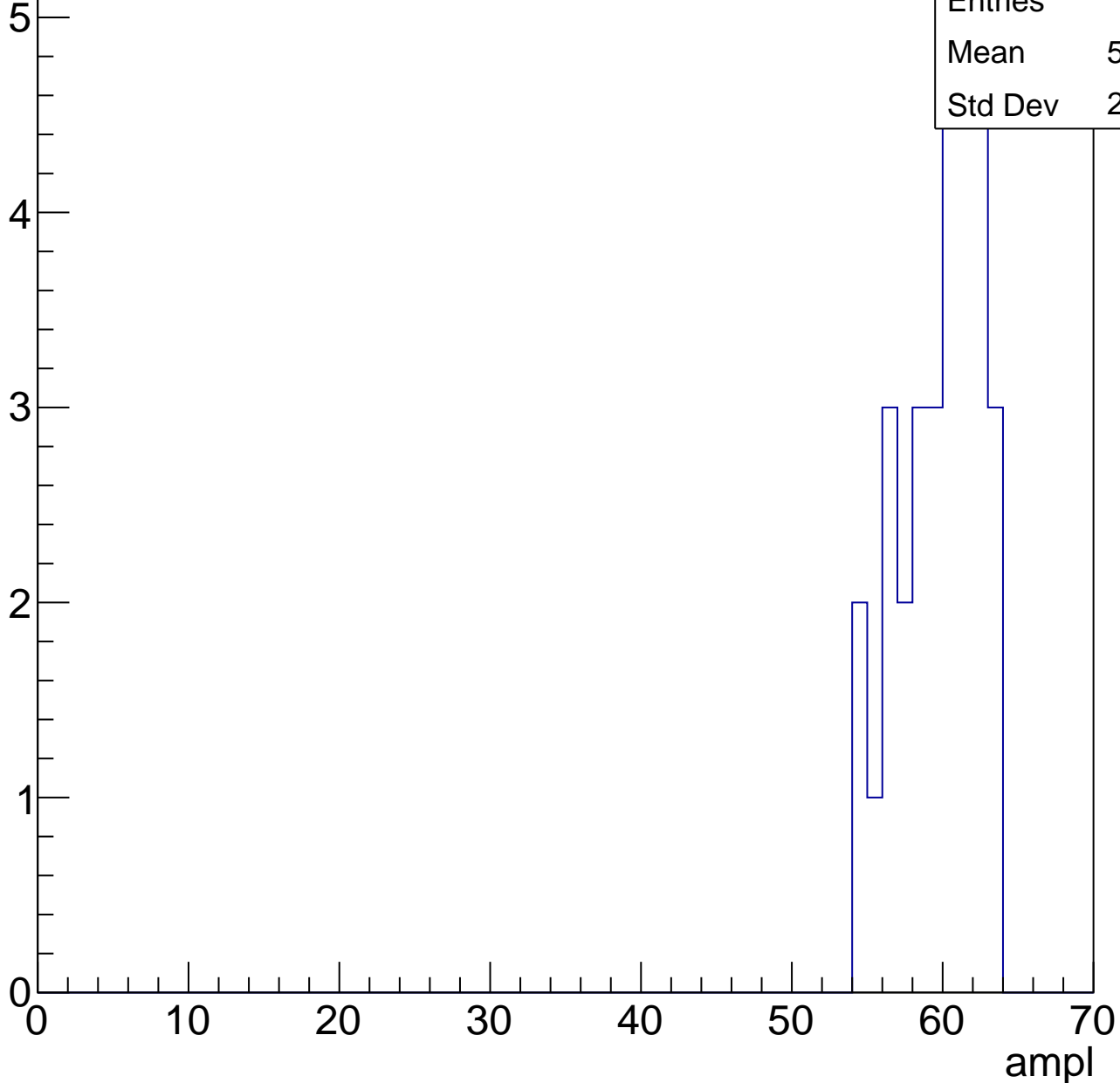


# B1L103S, U16-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	32
Mean	59.38
Std Dev	2.607

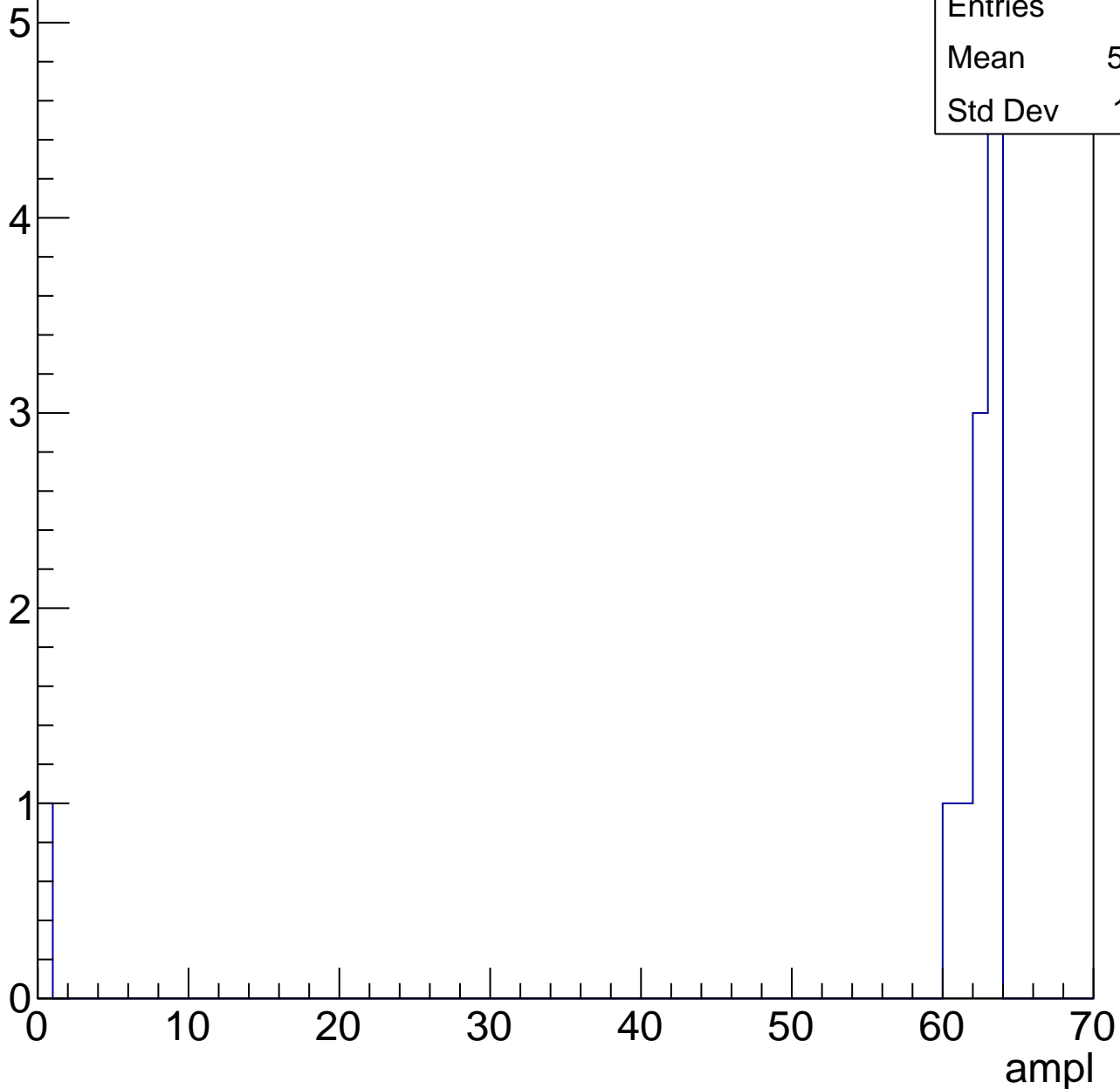


# B1L103S, U16-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	11
Mean	56.55
Std Dev	17.91





# B1L103S, U16-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch37, adc0

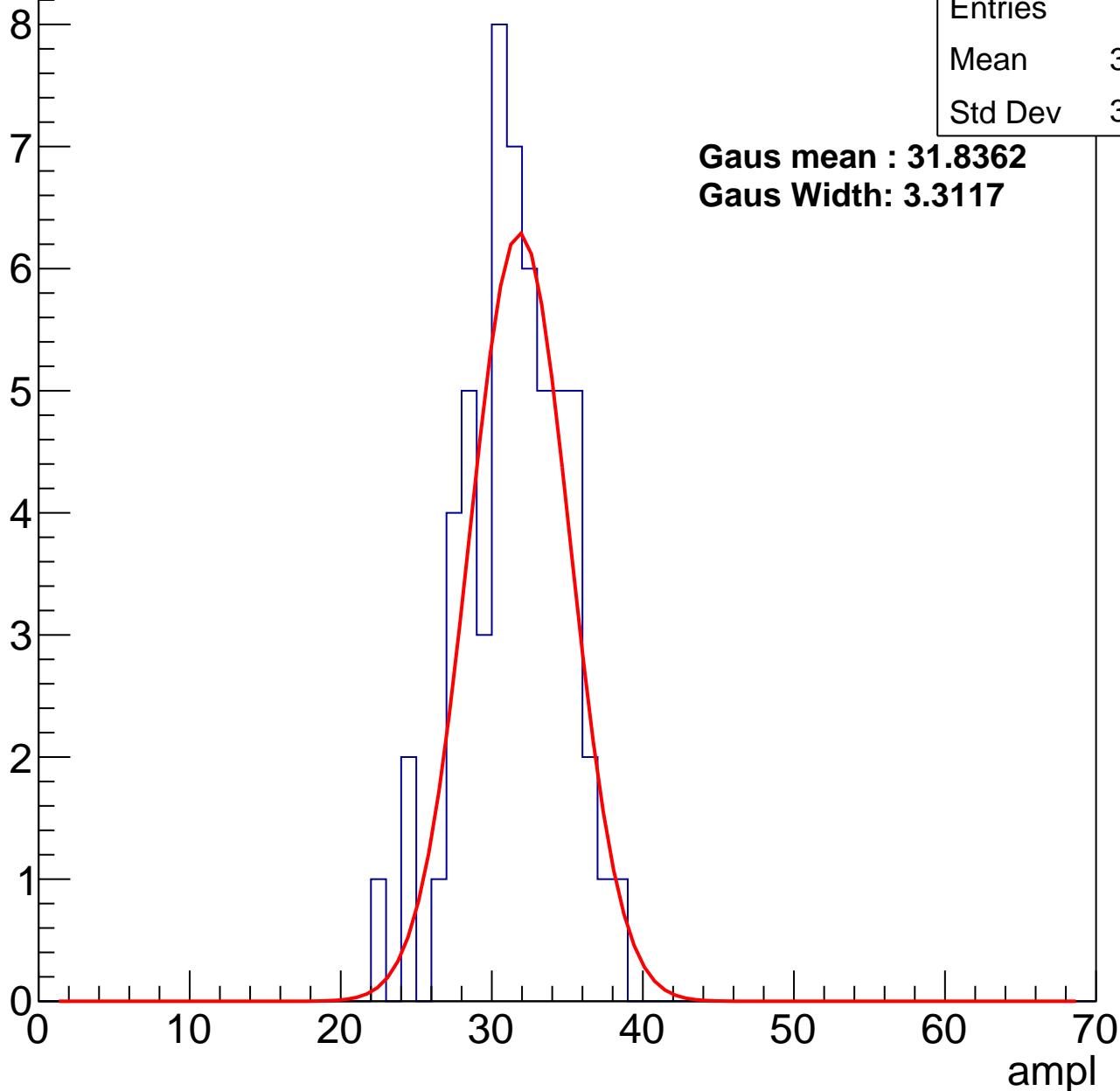
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	31.02
Std Dev	3.325

**Gaus mean : 31.8362**

**Gaus Width: 3.3117**



# B1L103S, U16-ch37, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

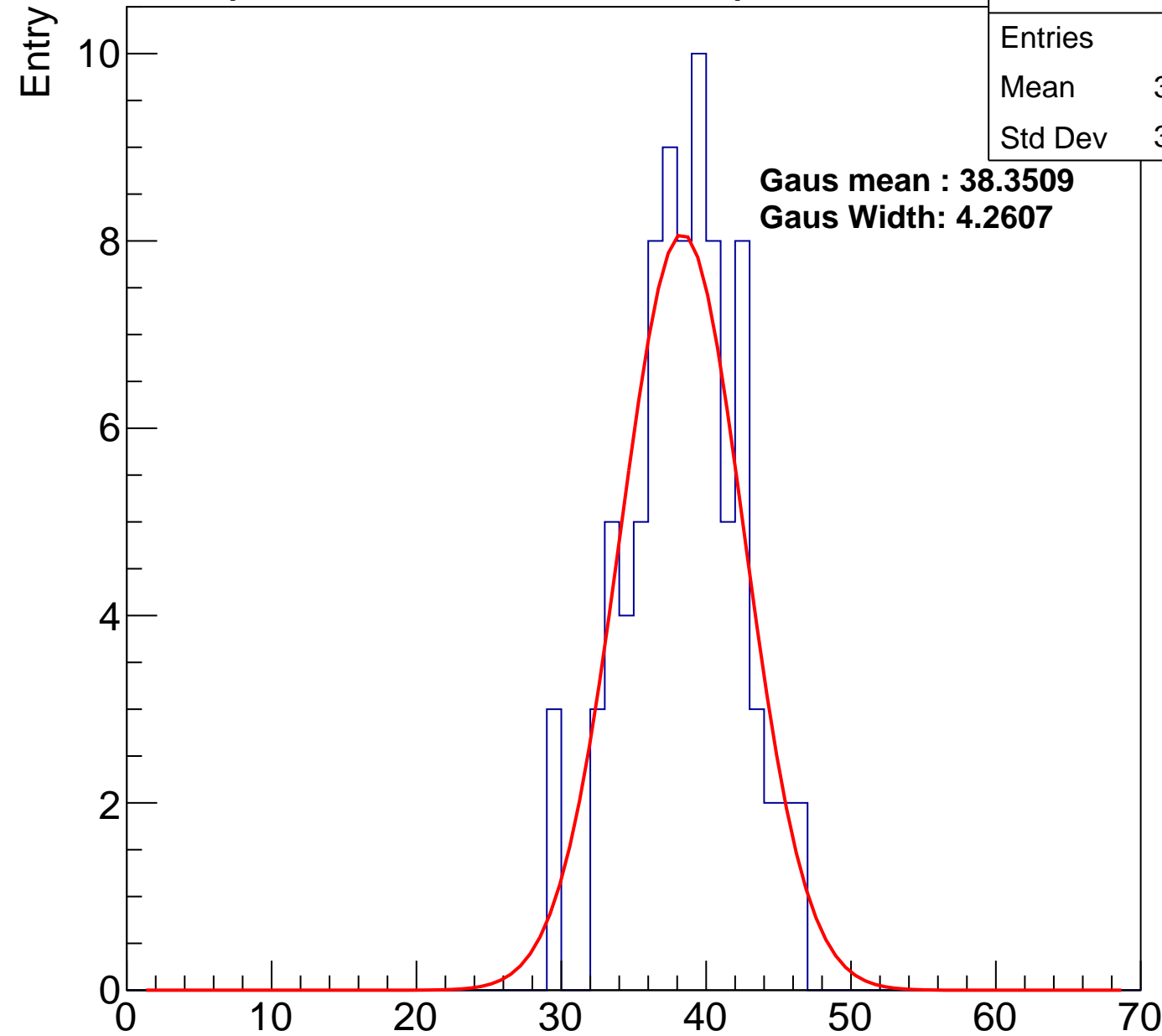
Entries	85
Mean	38.05
Std Dev	3.779

**Gaus mean : 38.3509**

**Gaus Width: 4.2607**

10  
8  
6  
4  
2  
0

ampl



# B1L103S, U16-ch37, adc2

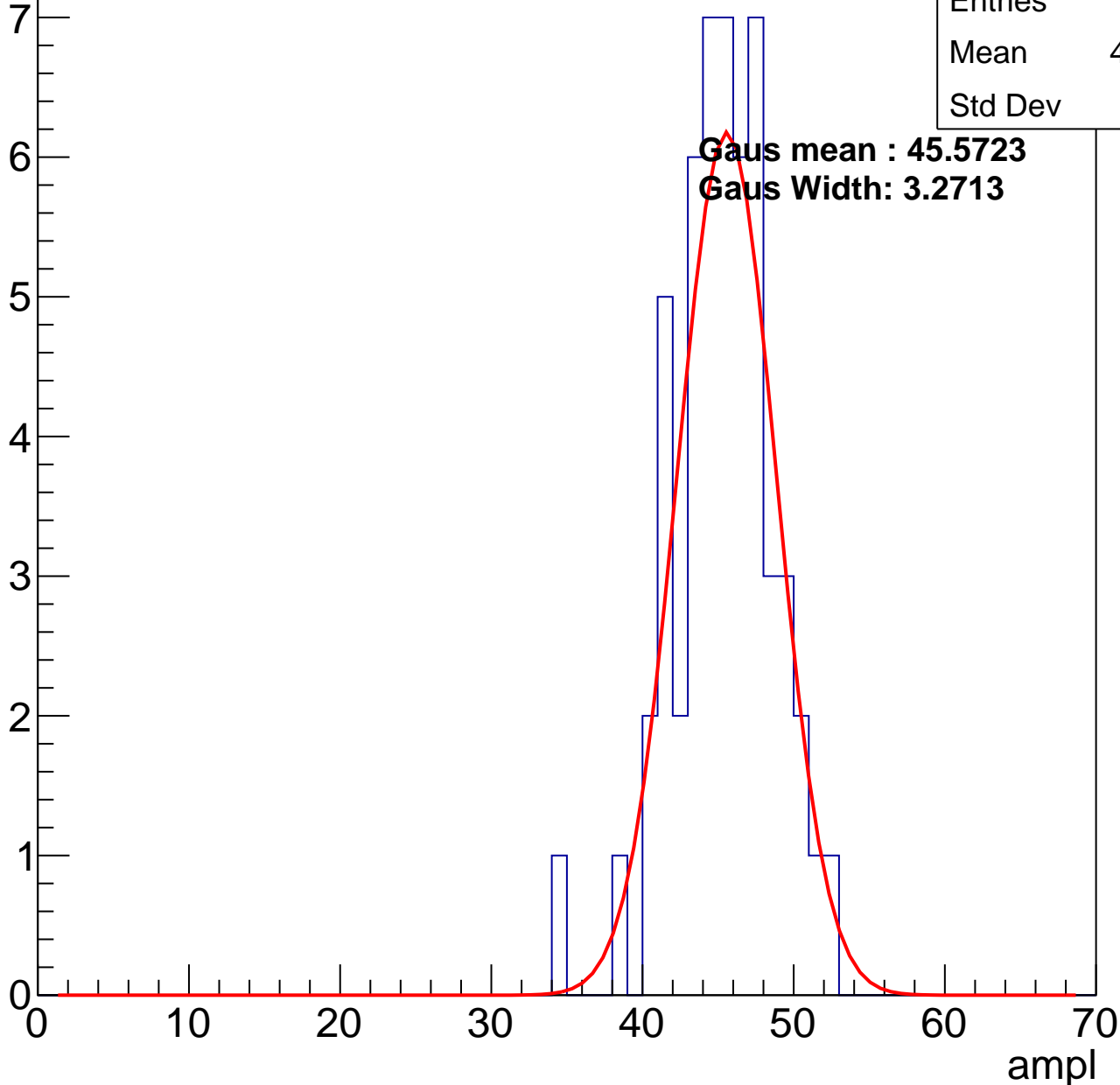
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	44.83
Std Dev	3.31

Gaus mean : 45.5723

Gaus Width: 3.2713

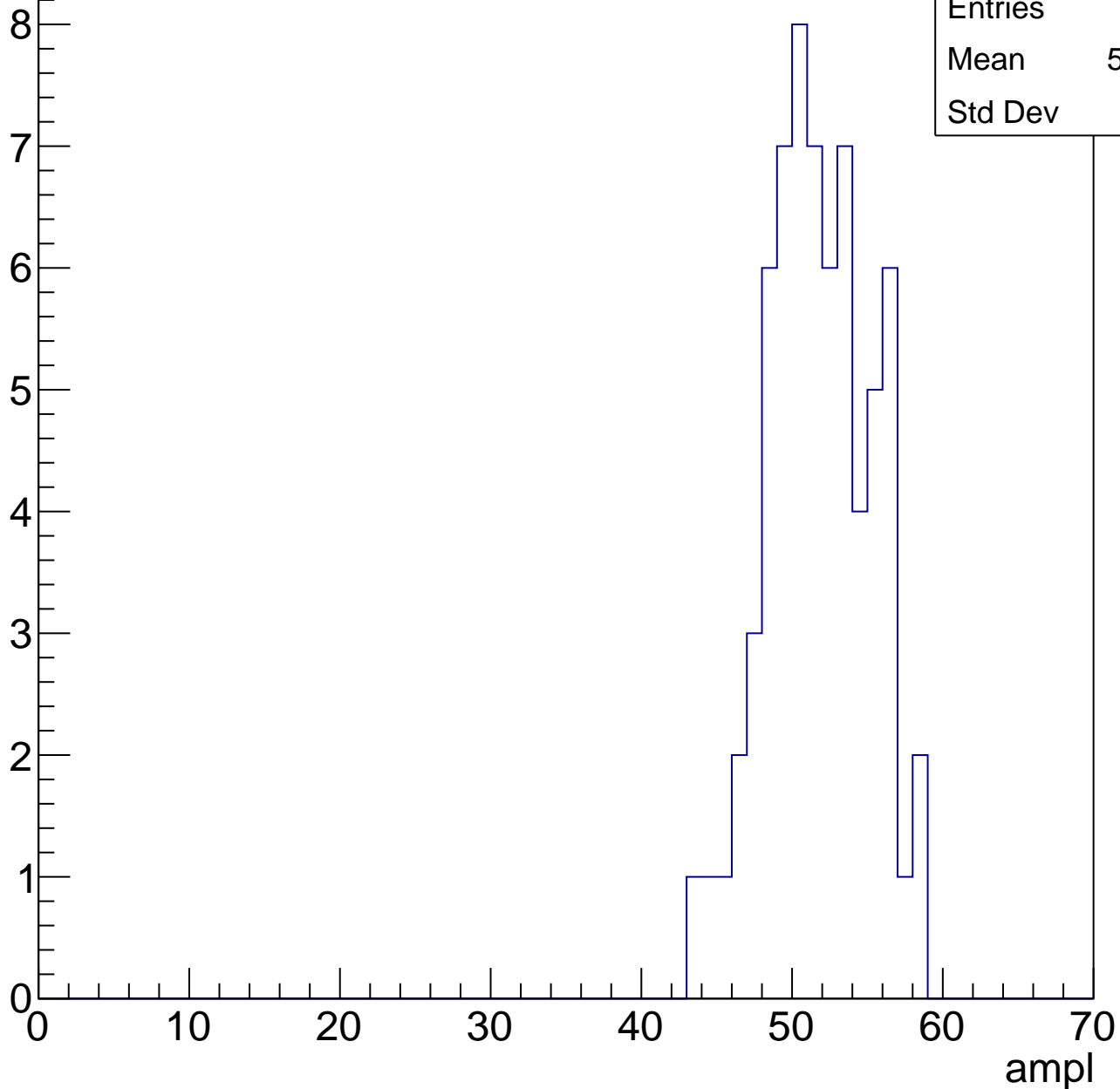


# B1L103S, U16-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

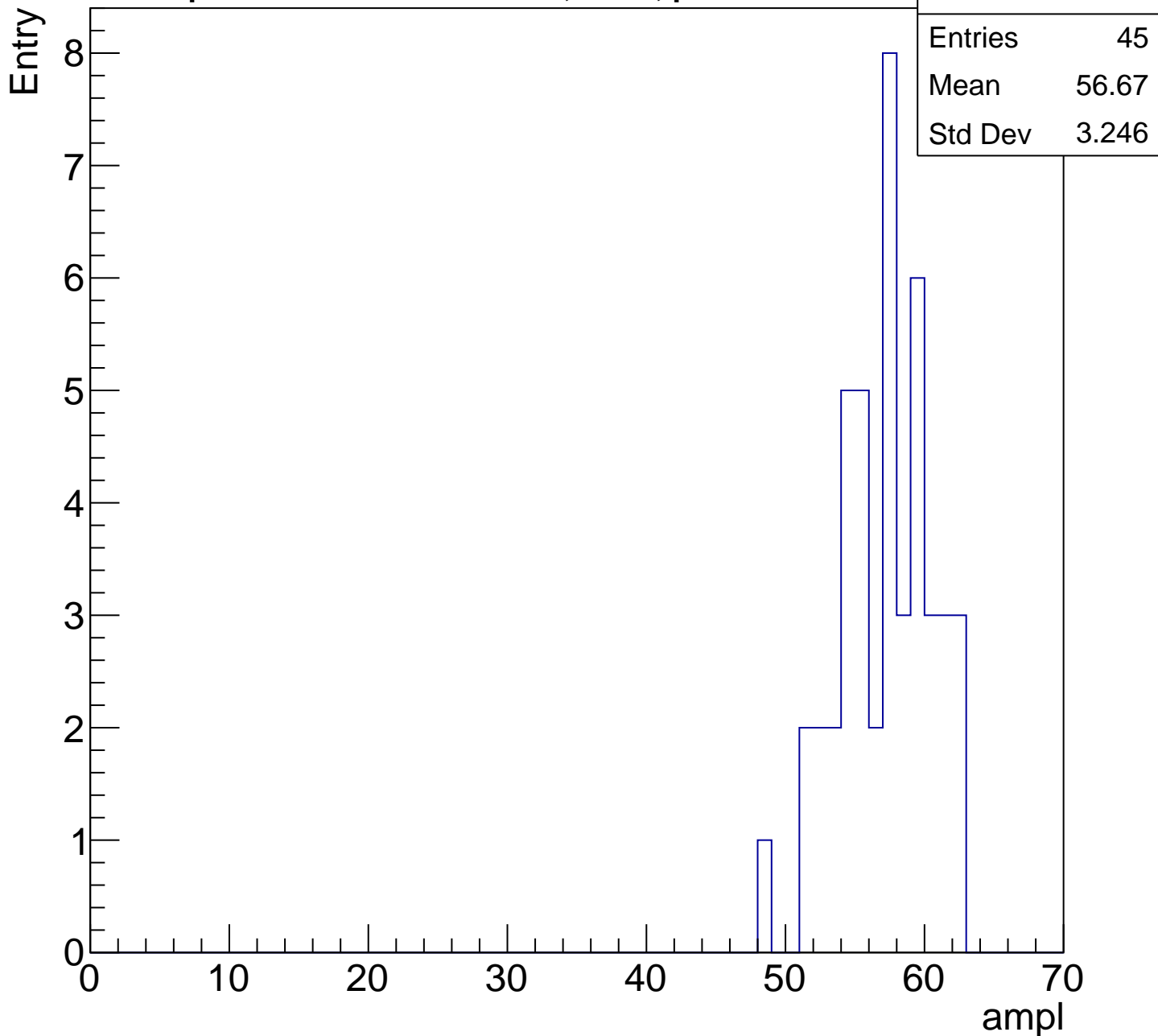
Entry

Entries	67
Mean	51.28
Std Dev	3.38



# B1L103S, U16-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

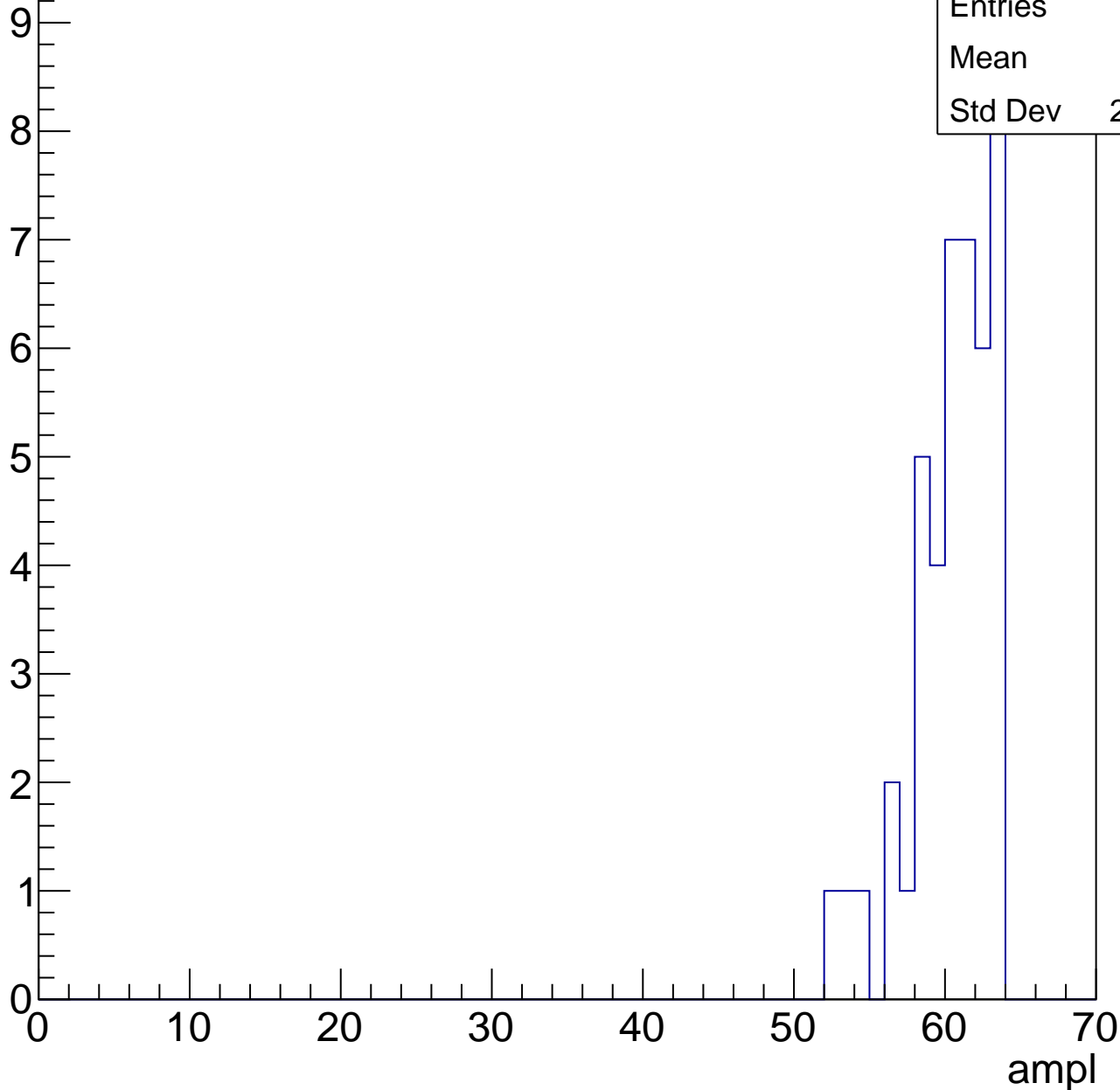


# B1L103S, U16-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

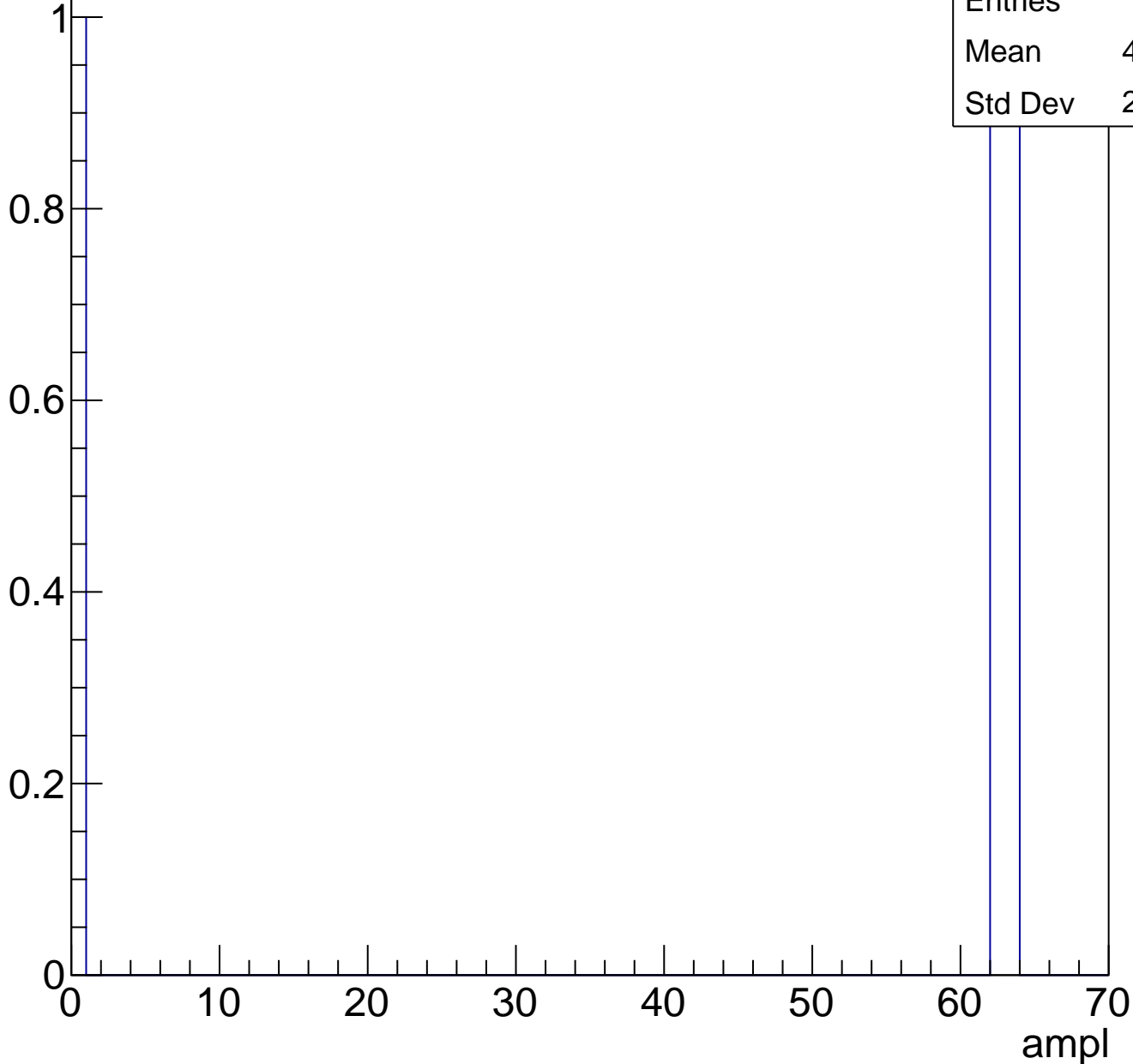
Entries	44
Mean	60
Std Dev	2.722



# B1L103S, U16-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch38, adc0

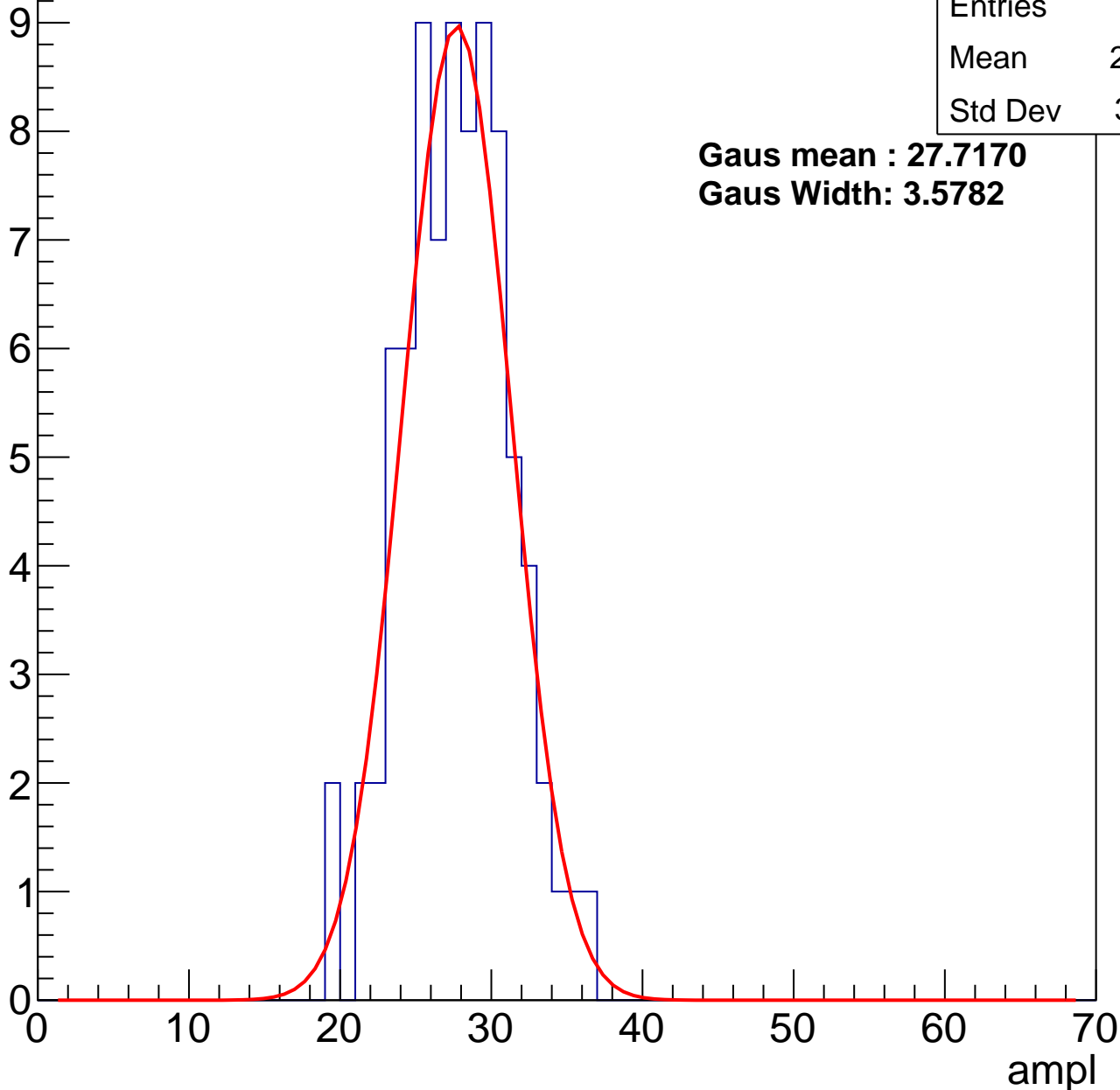
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	82
Mean	27.26
Std Dev	3.491

**Gaus mean : 27.7170**

**Gaus Width: 3.5782**



# B1L103S, U16-ch38, adc1

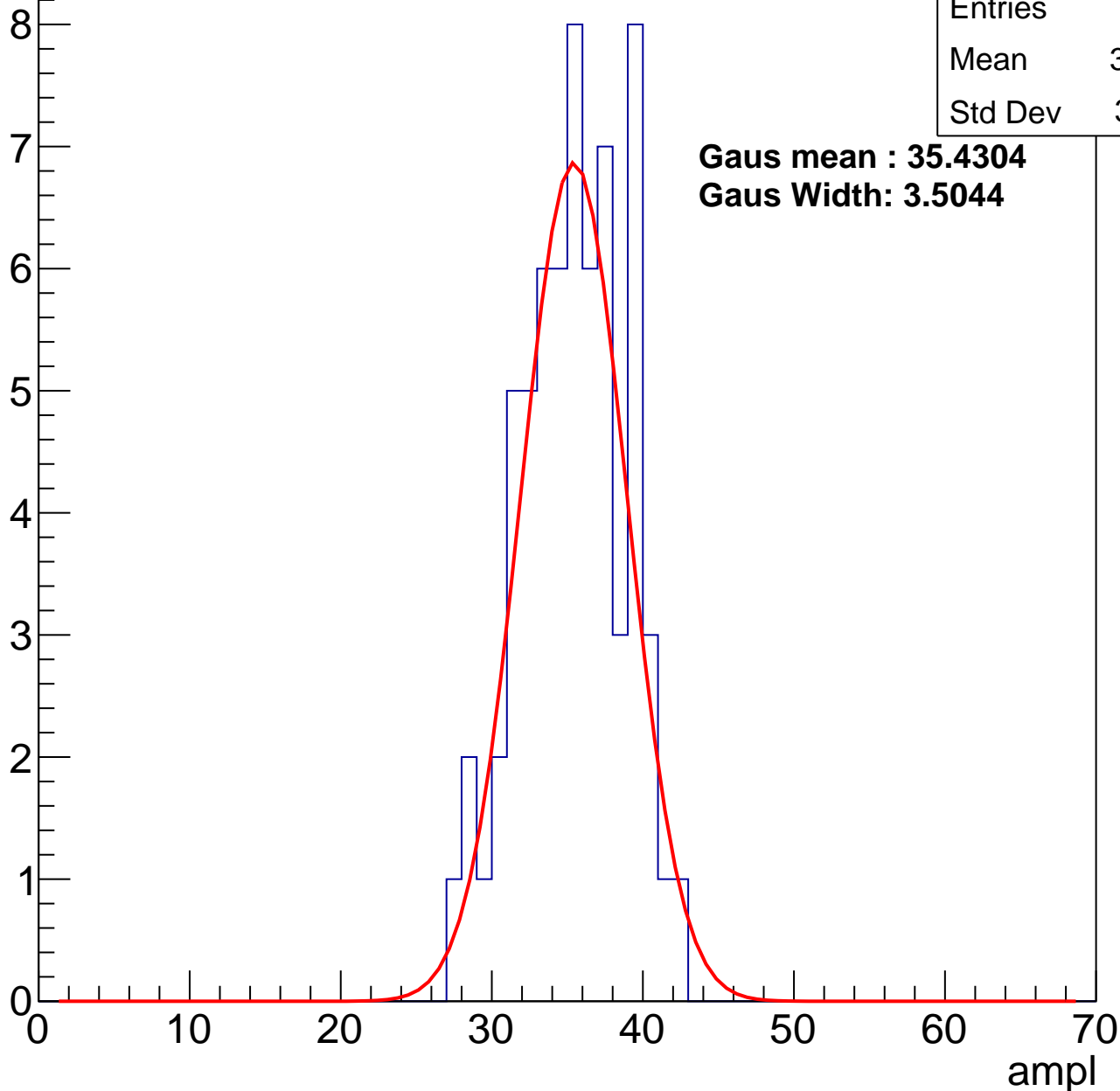
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	34.97
Std Dev	3.401

**Gaus mean : 35.4304**

**Gaus Width: 3.5044**



# B1L103S, U16-ch38, adc2

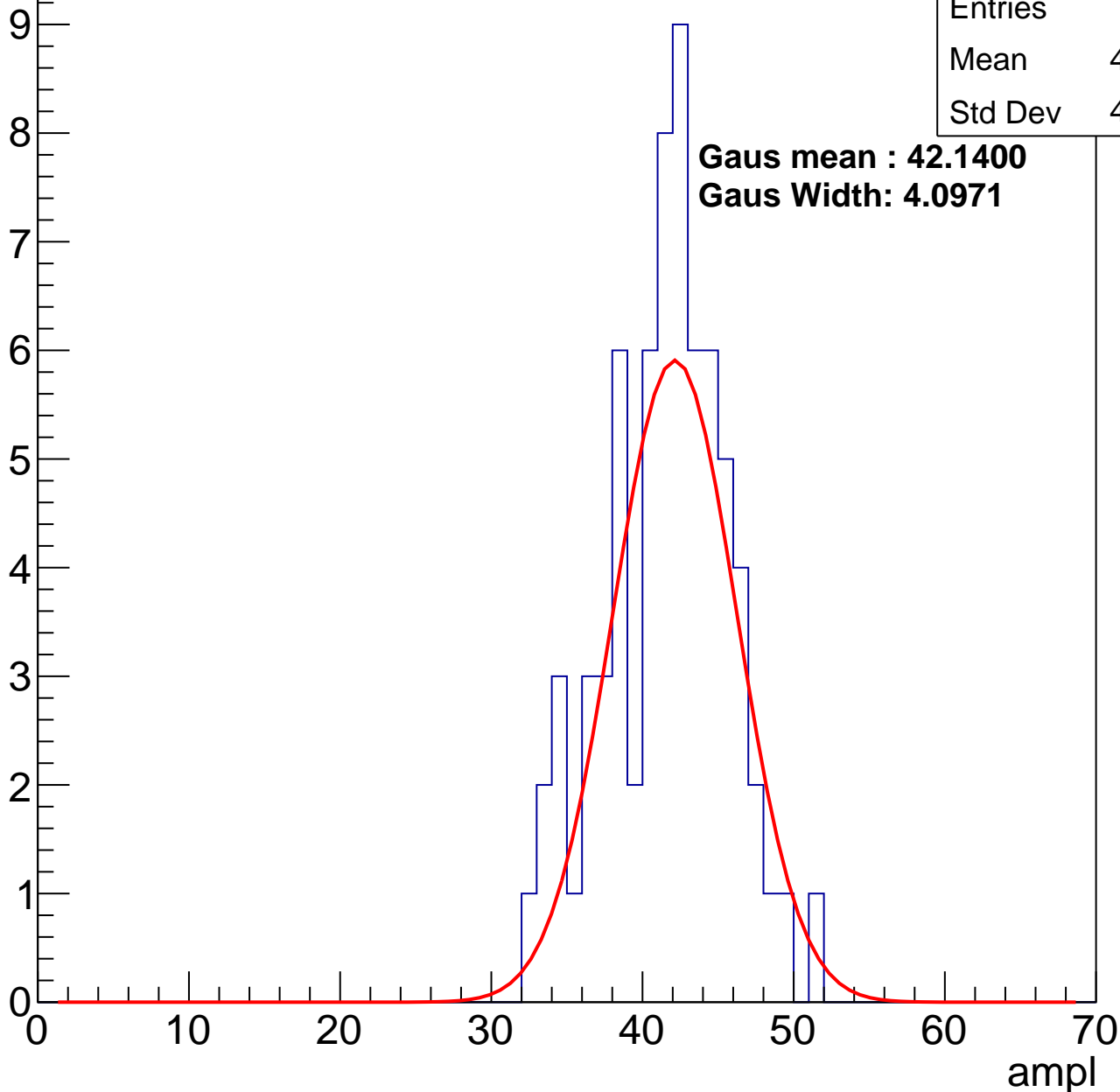
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	41.13
Std Dev	4.025

**Gaus mean : 42.1400**

**Gaus Width: 4.0971**

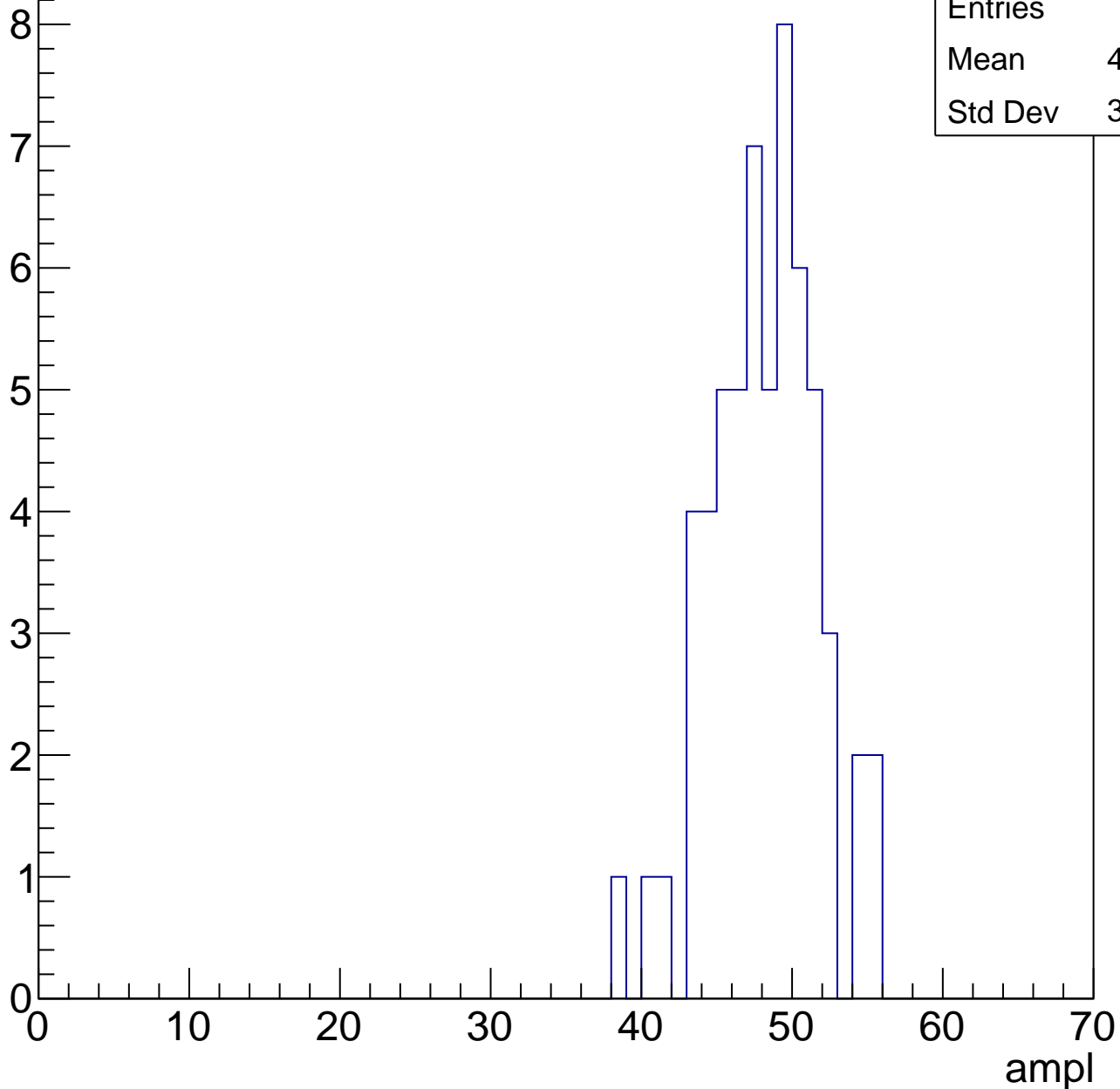


# B1L103S, U16-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	47.66
Std Dev	3.535

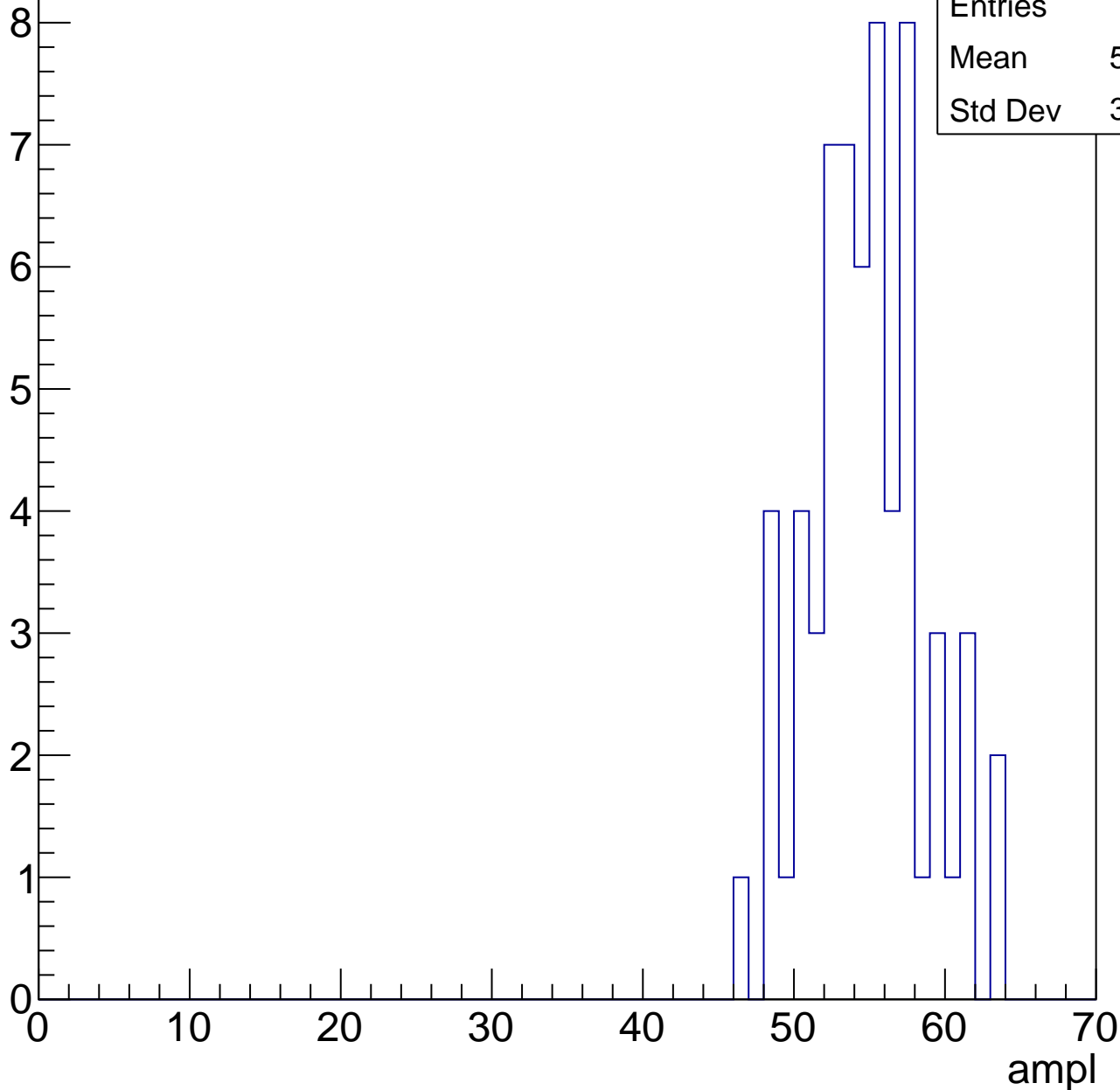


# B1L103S, U16-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	54.33
Std Dev	3.746

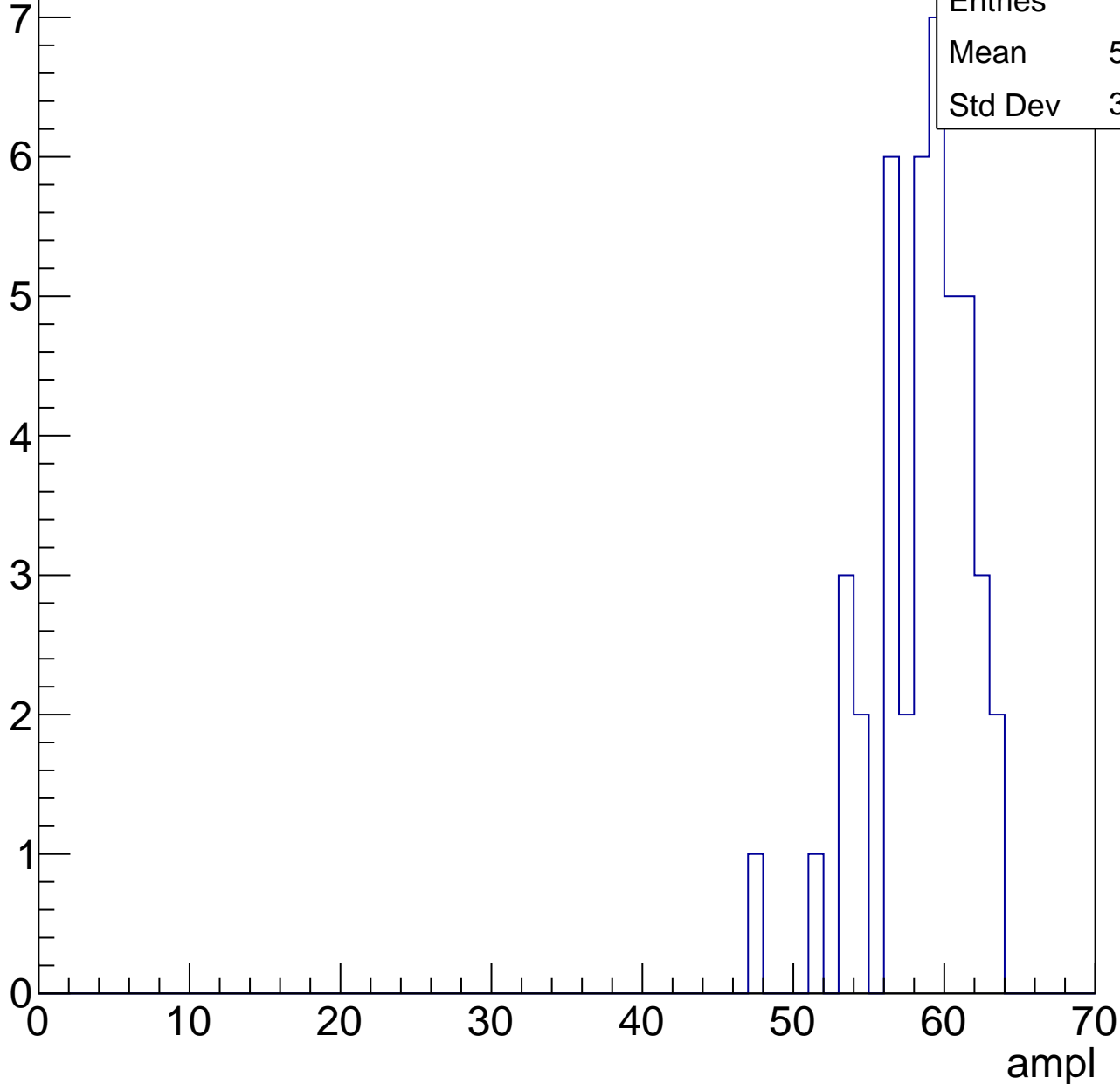


# B1L103S, U16-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	43
Mean	57.98
Std Dev	3.317

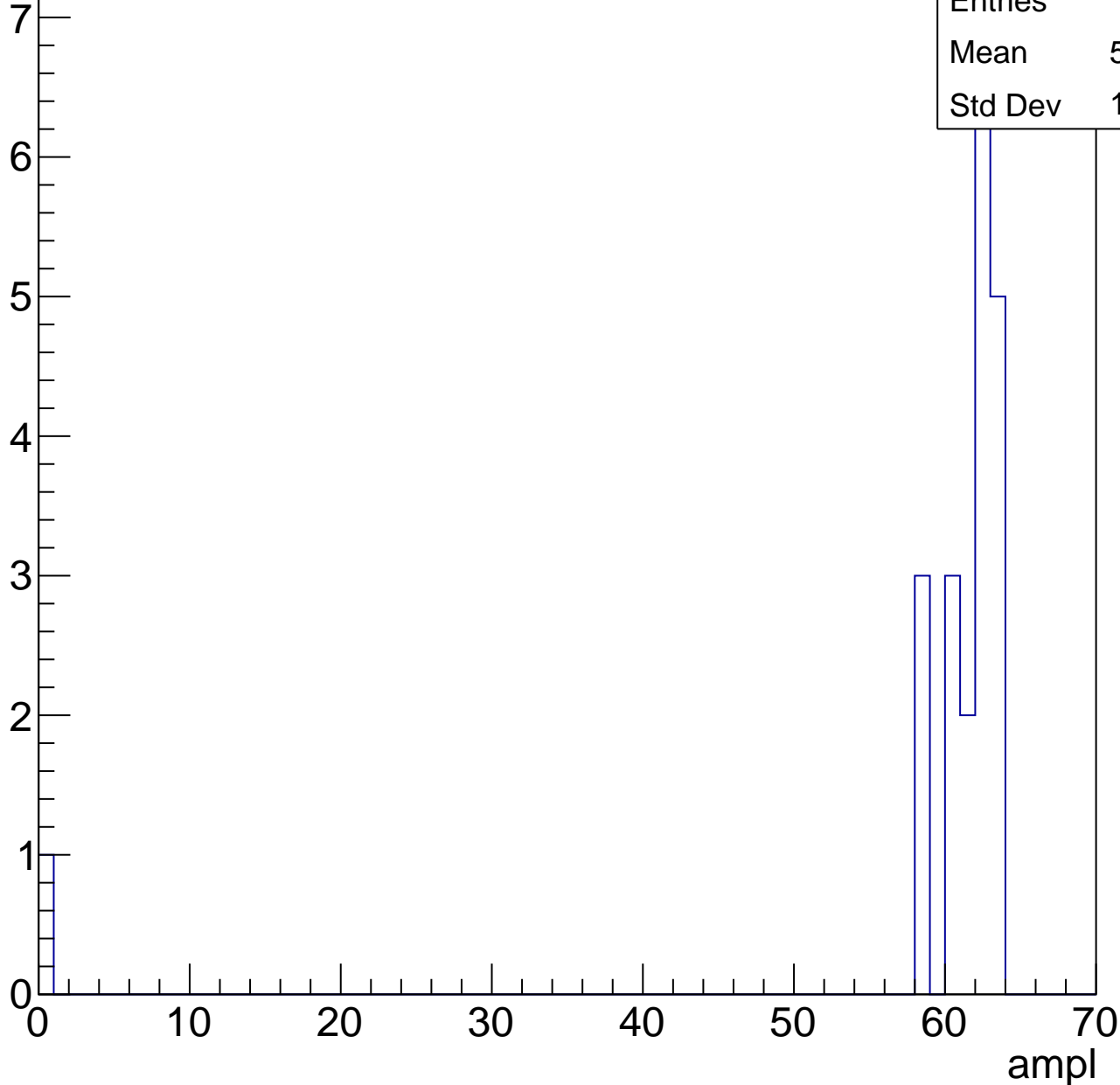


# B1L103S, U16-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	21
Mean	58.33
Std Dev	13.15





# B1L103S, U16-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch39, adc0

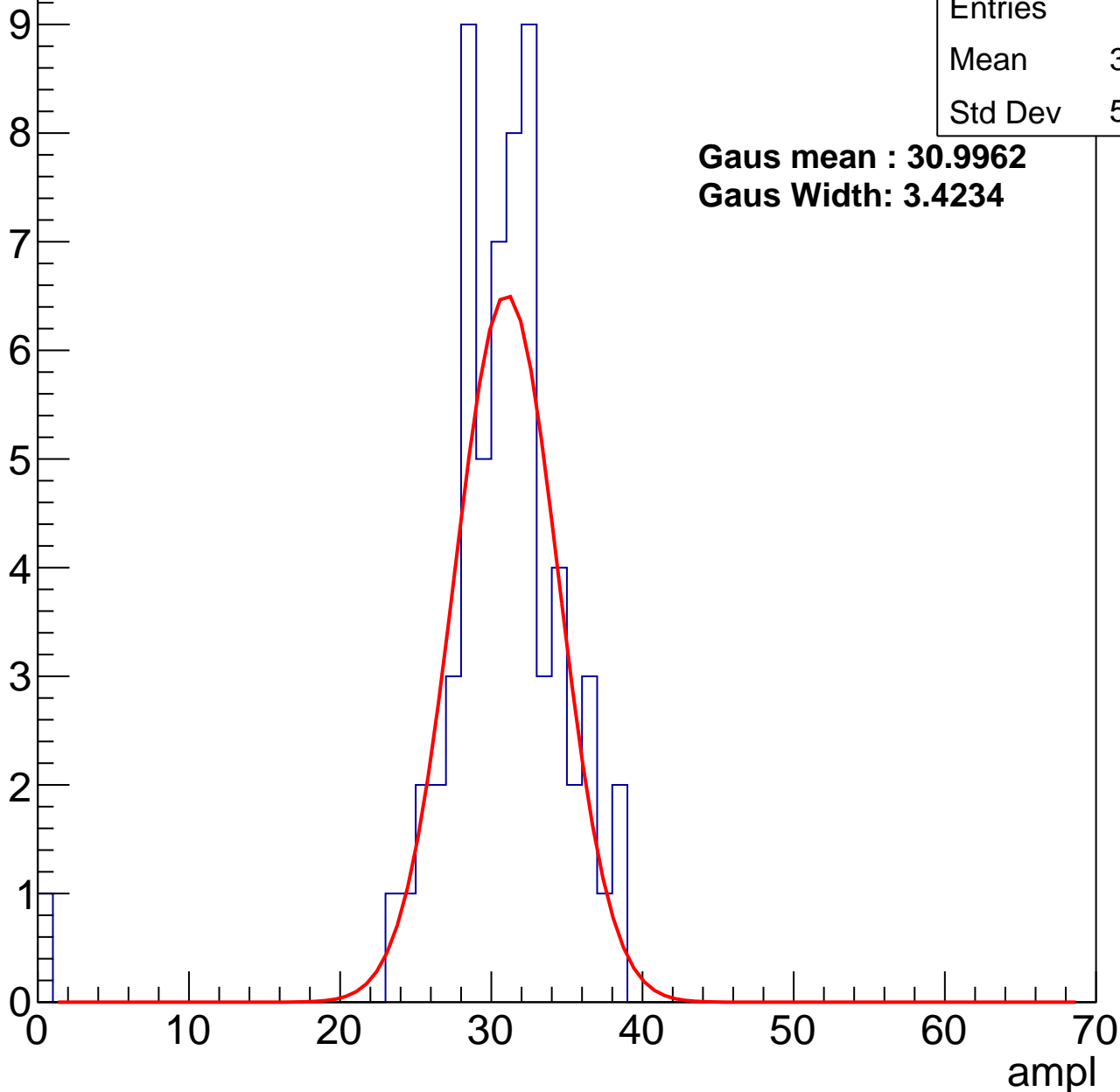
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	30.14
Std Dev	5.045

**Gaus mean : 30.9962**

**Gaus Width: 3.4234**



# B1L103S, U16-ch39, adc1

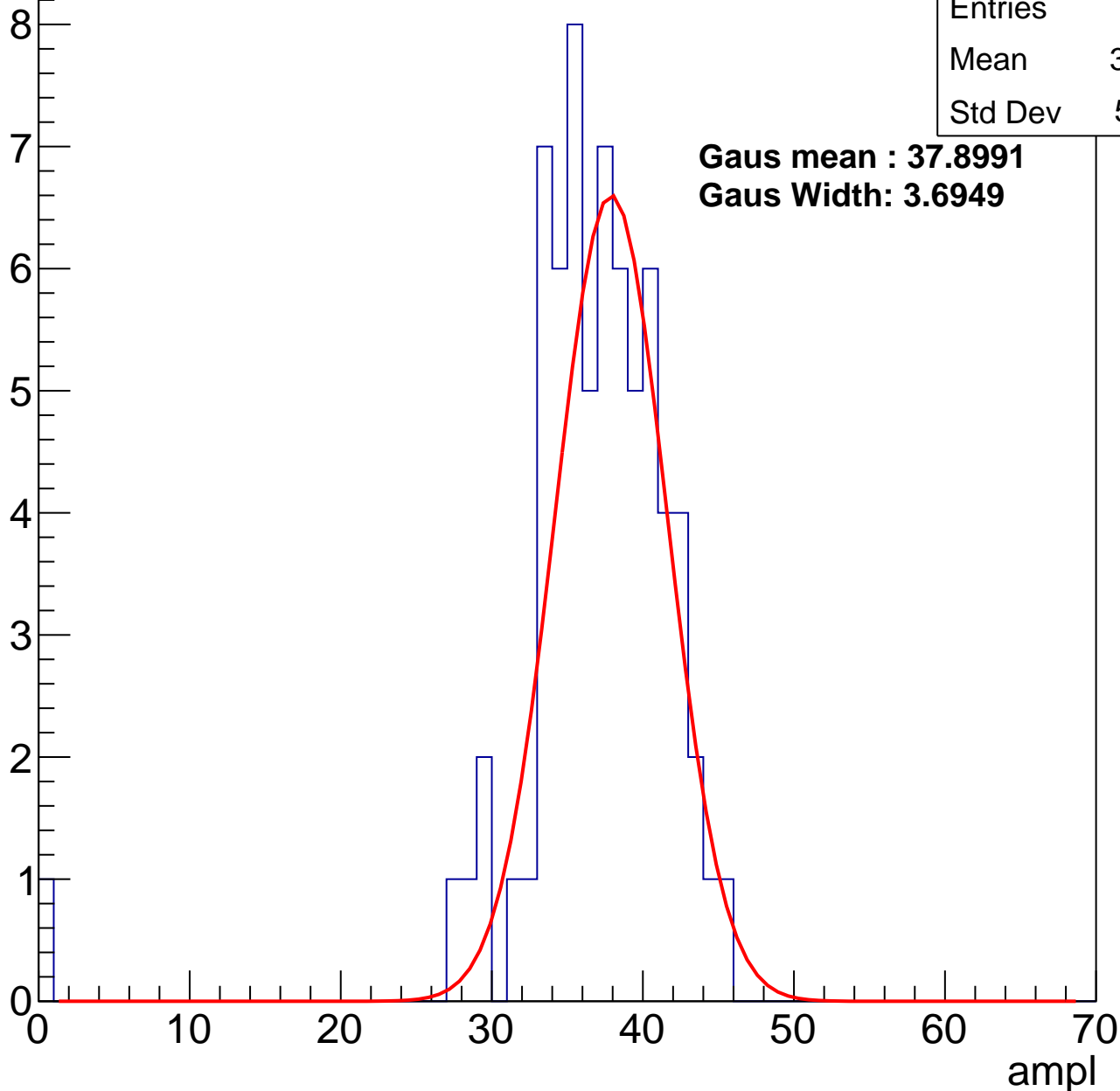
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	36.23
Std Dev	5.811

**Gaus mean : 37.8991**

**Gaus Width: 3.6949**



# B1L103S, U16-ch39, adc2

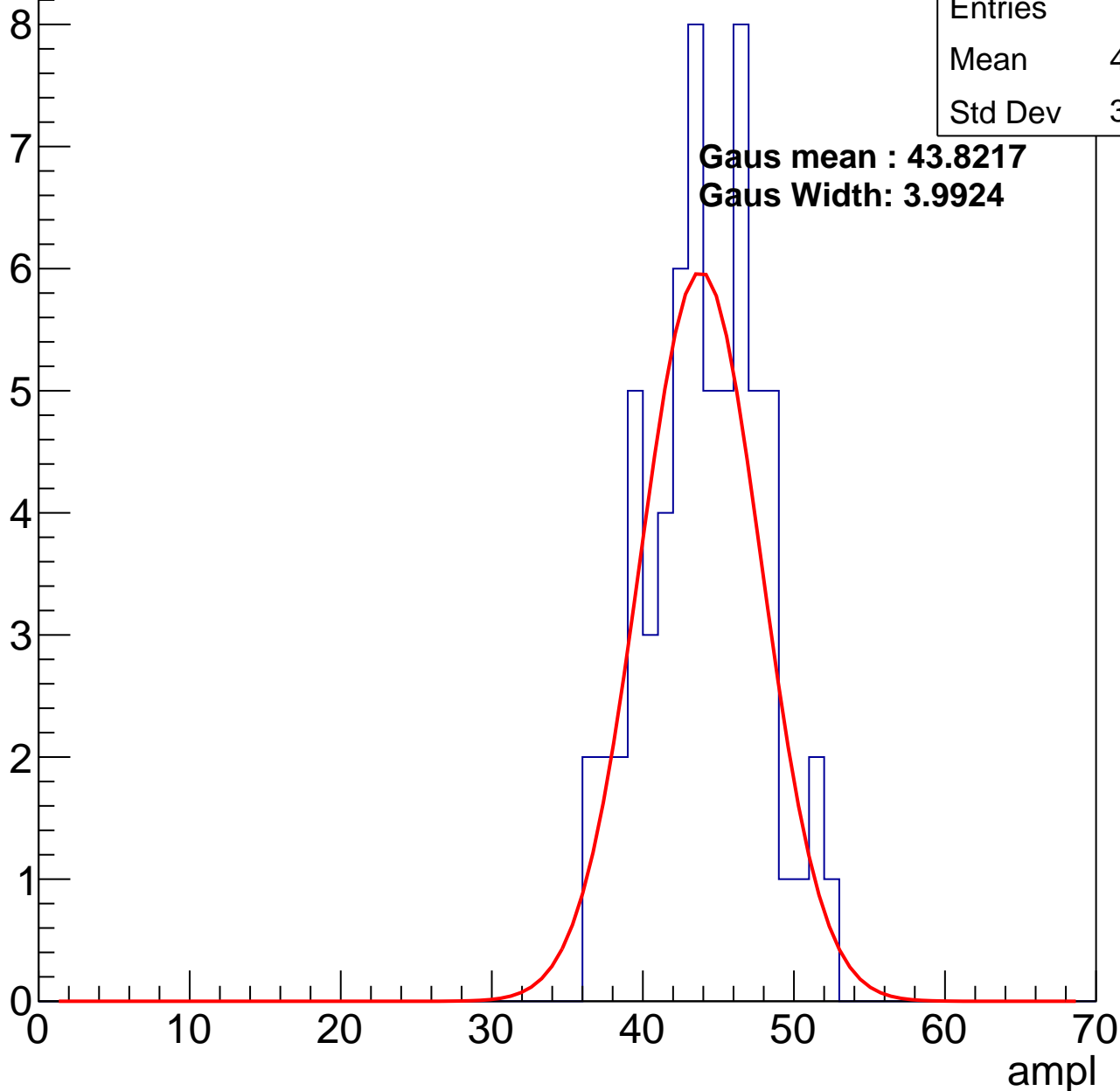
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	43.66
Std Dev	3.755

**Gaus mean : 43.8217**

**Gaus Width: 3.9924**

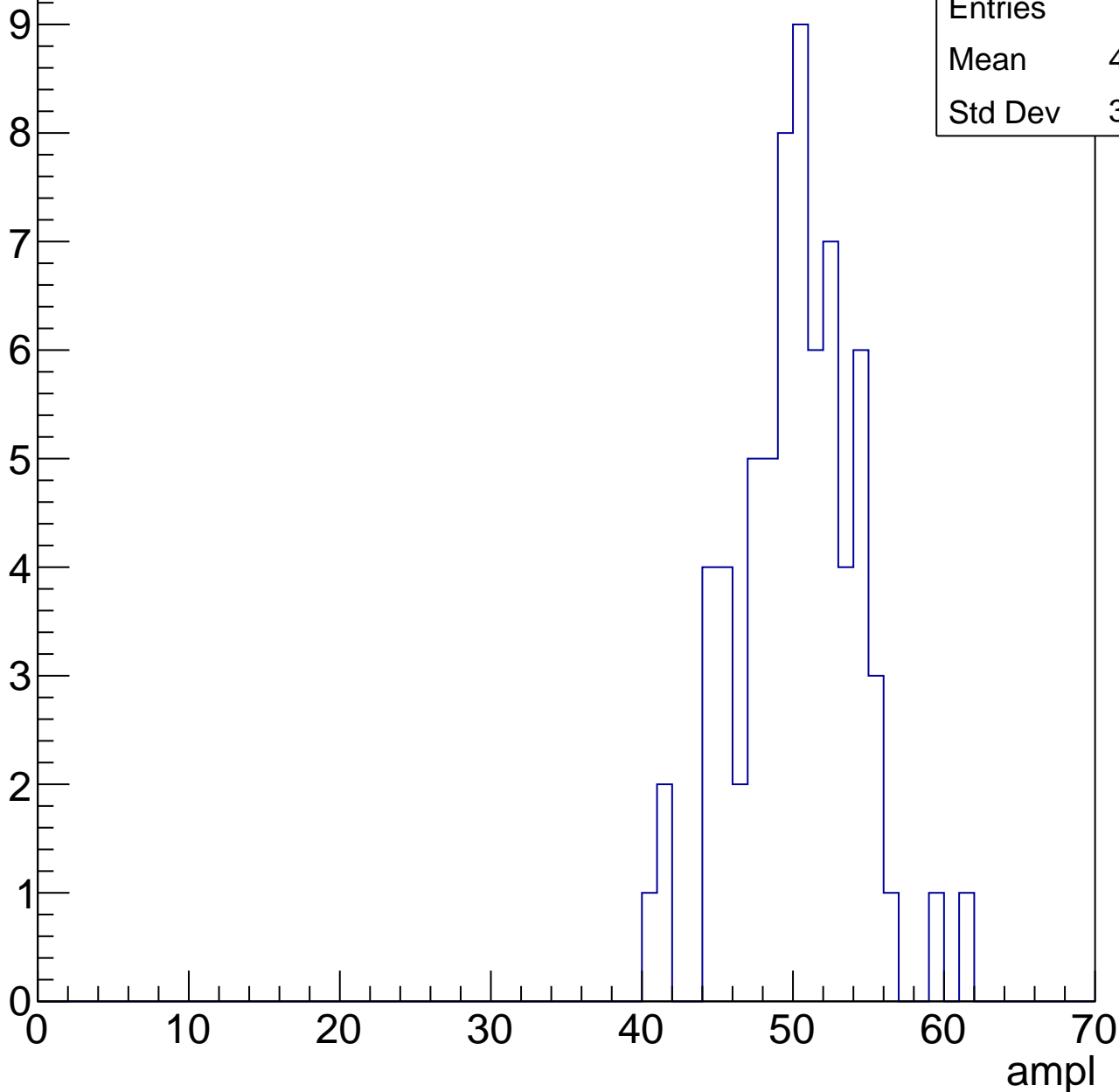


# B1L103S, U16-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

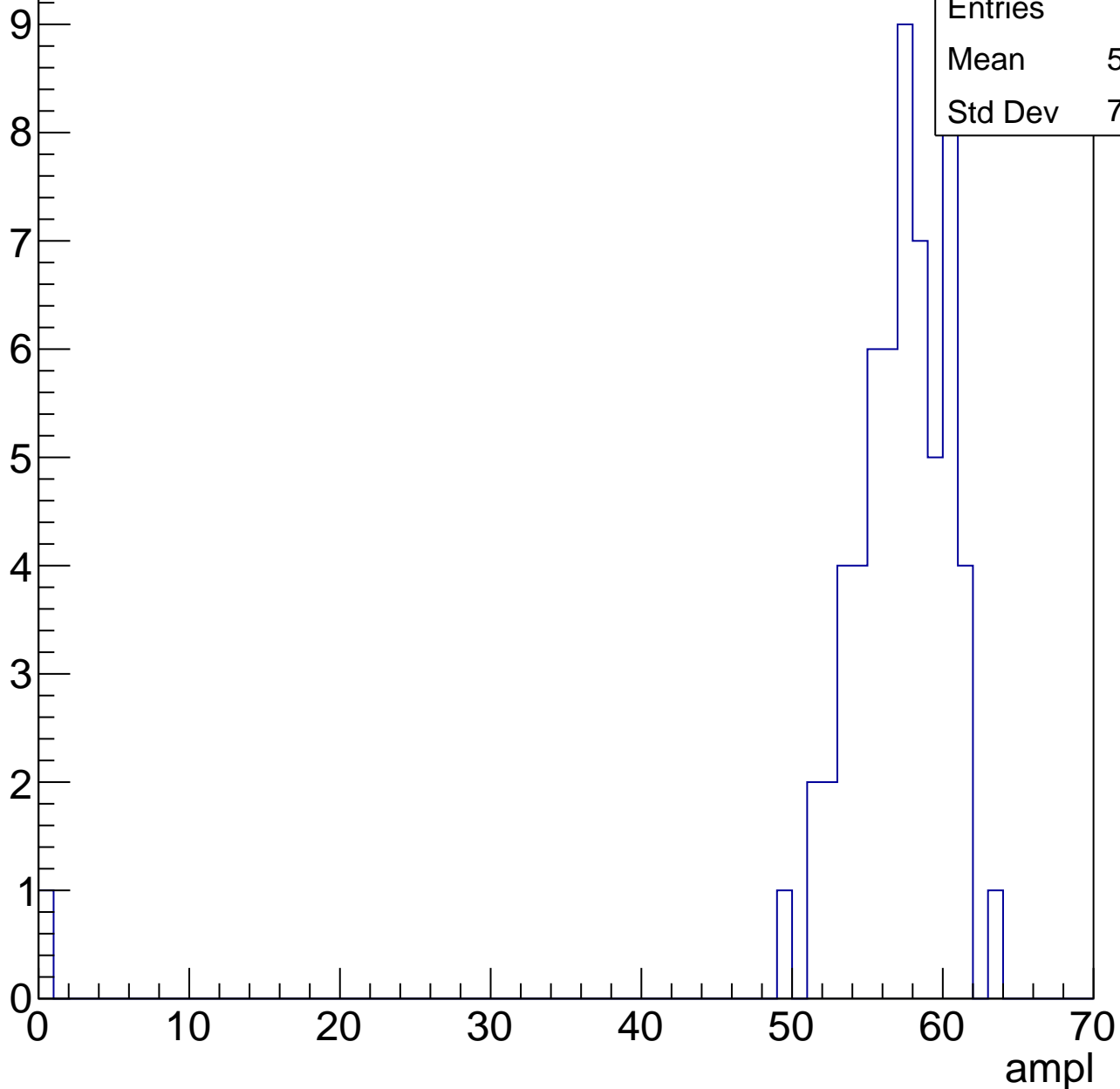
Entries	69
Mean	49.77
Std Dev	3.968



# B1L103S, U16-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

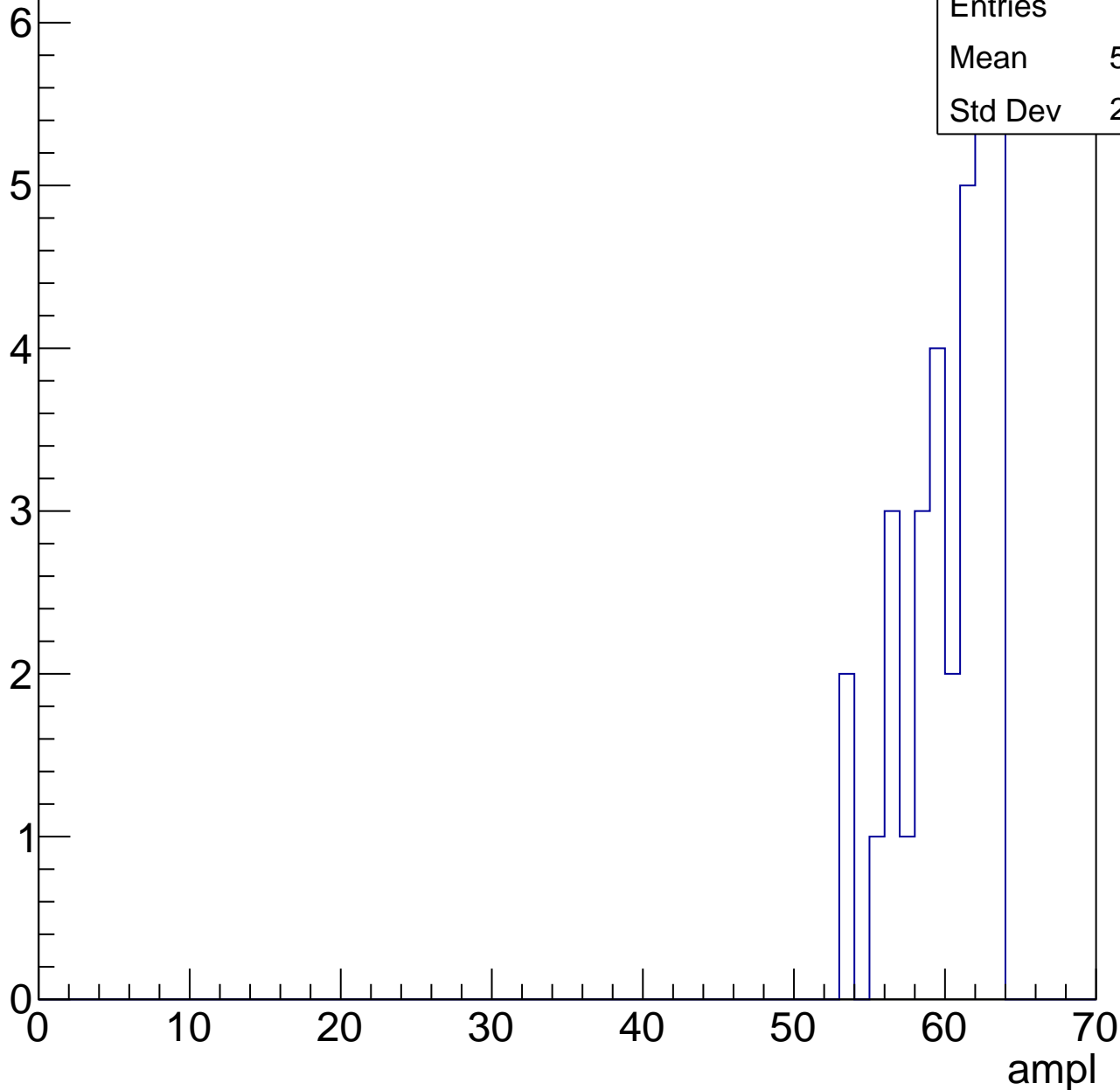


# B1L103S, U16-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

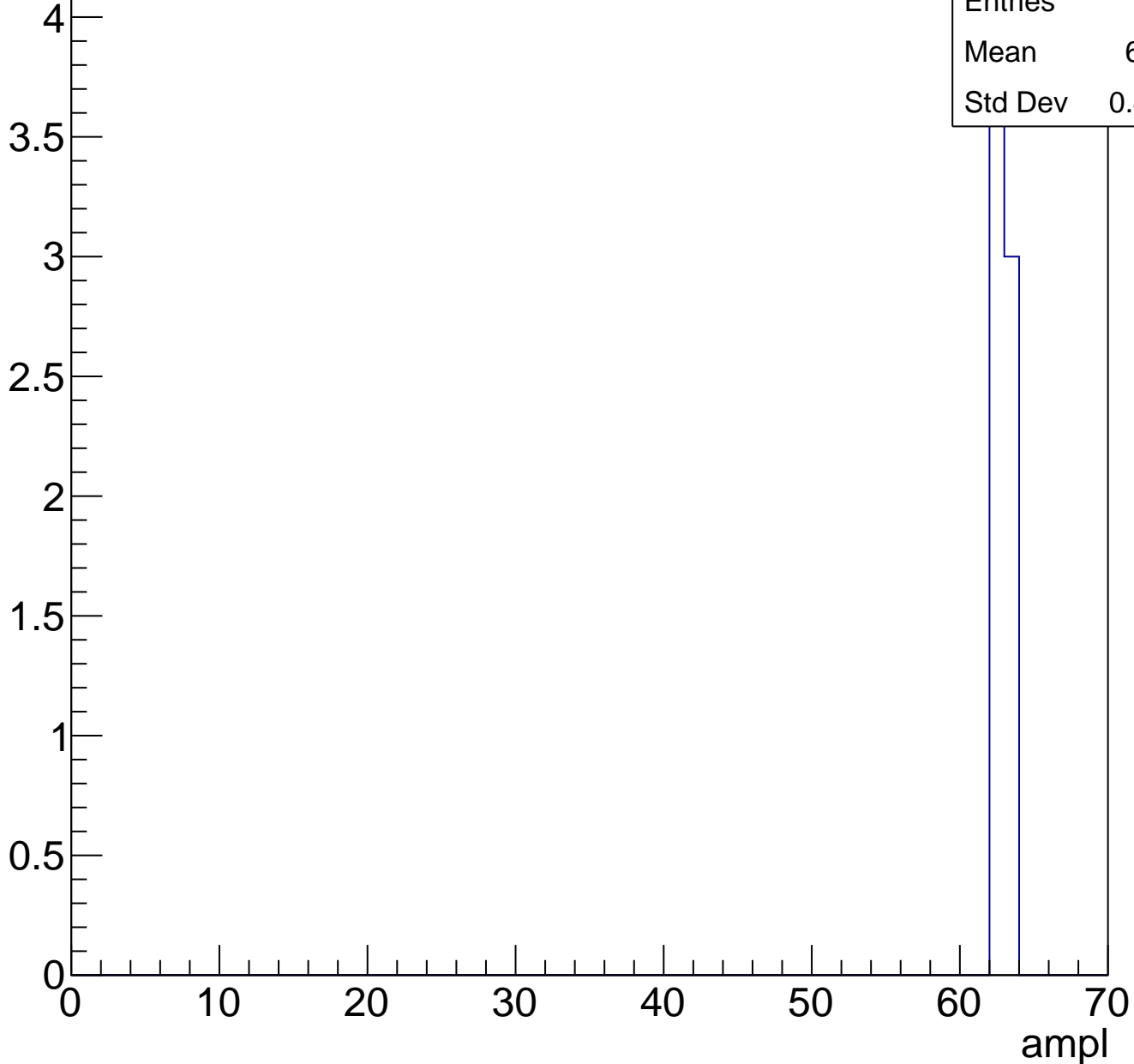
Entries	33
Mean	59.73
Std Dev	2.895



# B1L103S, U16-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch40, adc0

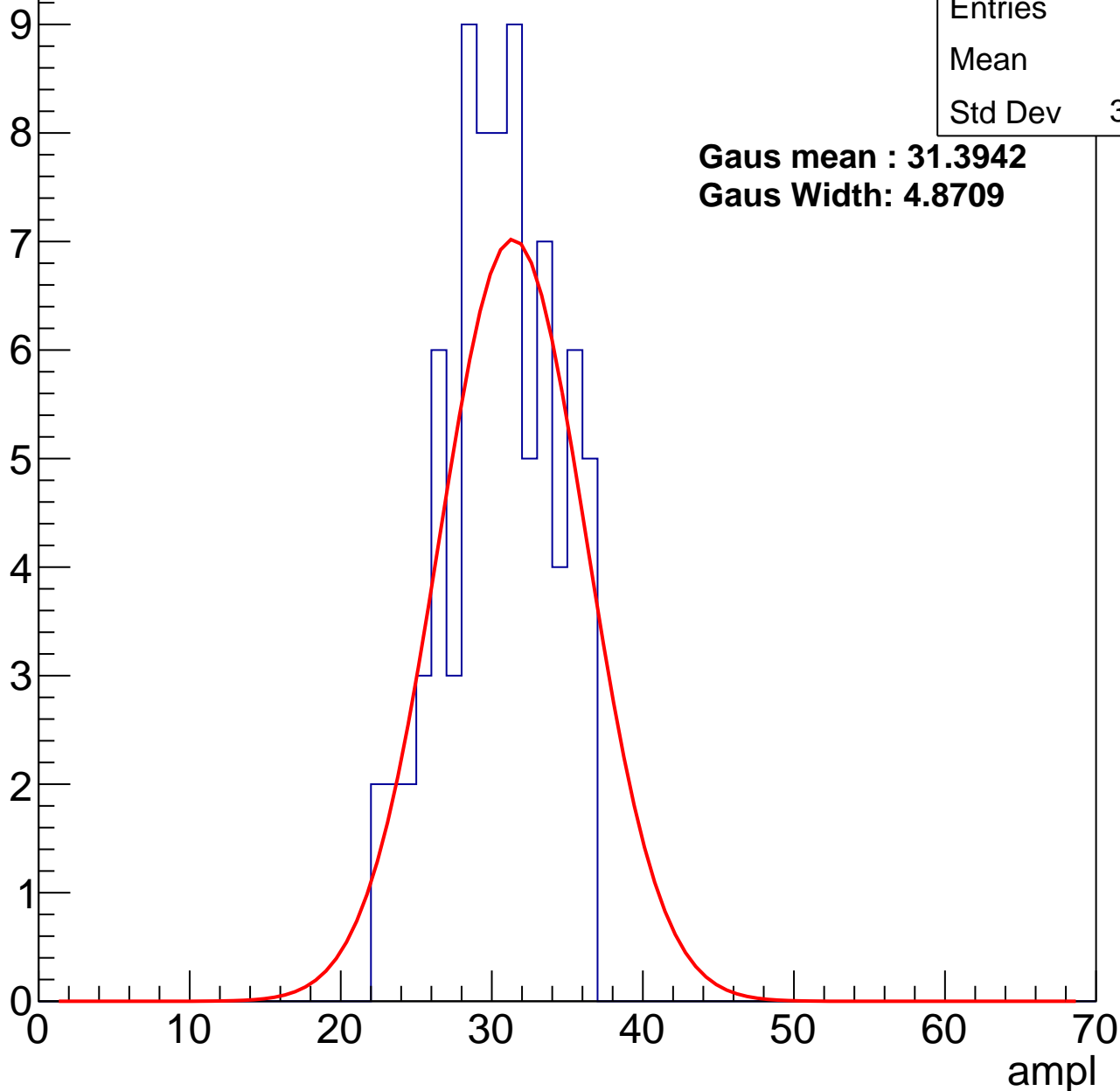
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	30
Std Dev	3.604

**Gaus mean : 31.3942**

**Gaus Width: 4.8709**



# B1L103S, U16-ch40, adc1

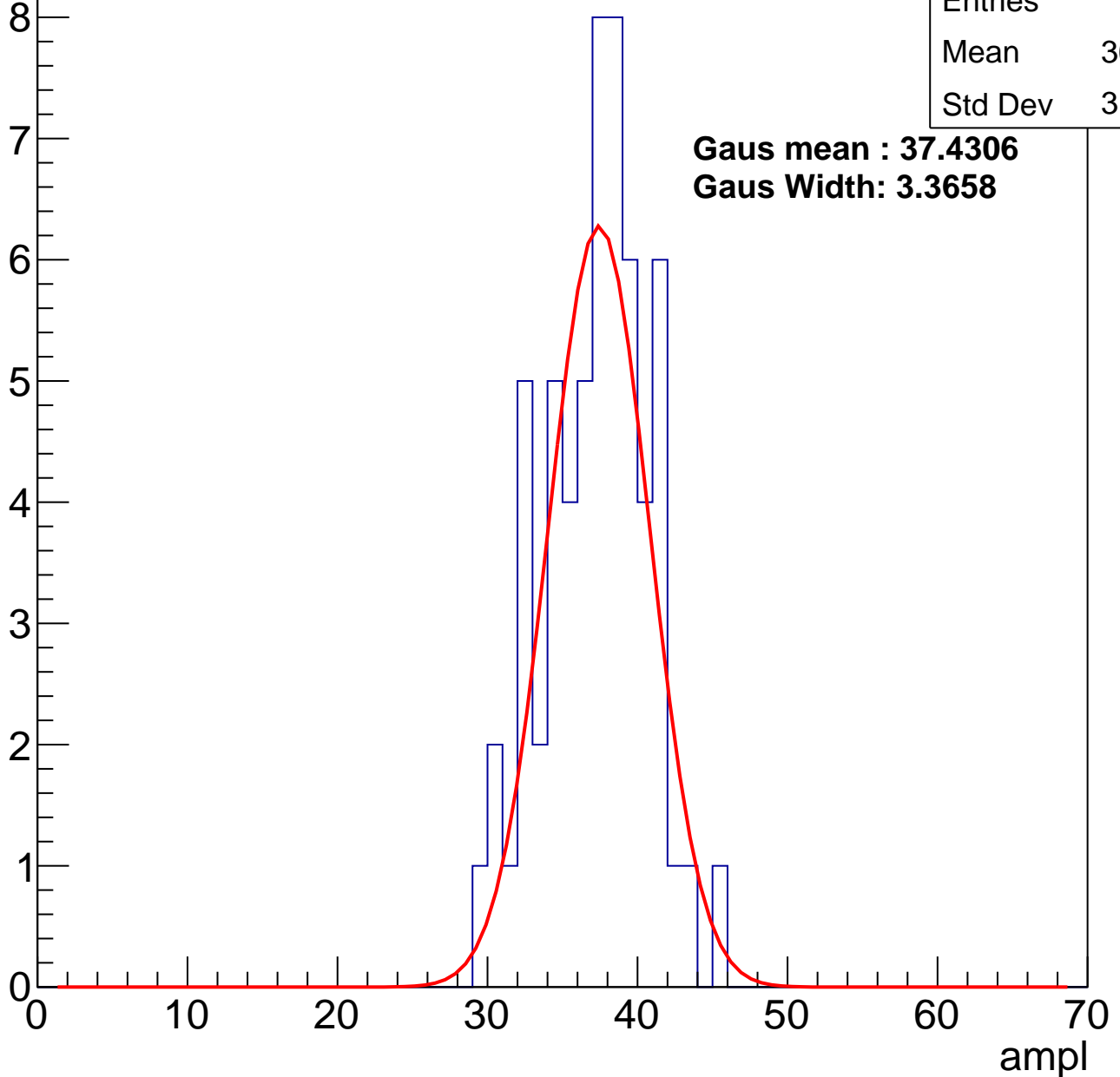
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	36.77
Std Dev	3.432

**Gaus mean : 37.4306**

**Gaus Width: 3.3658**



# B1L103S, U16-ch40, adc2

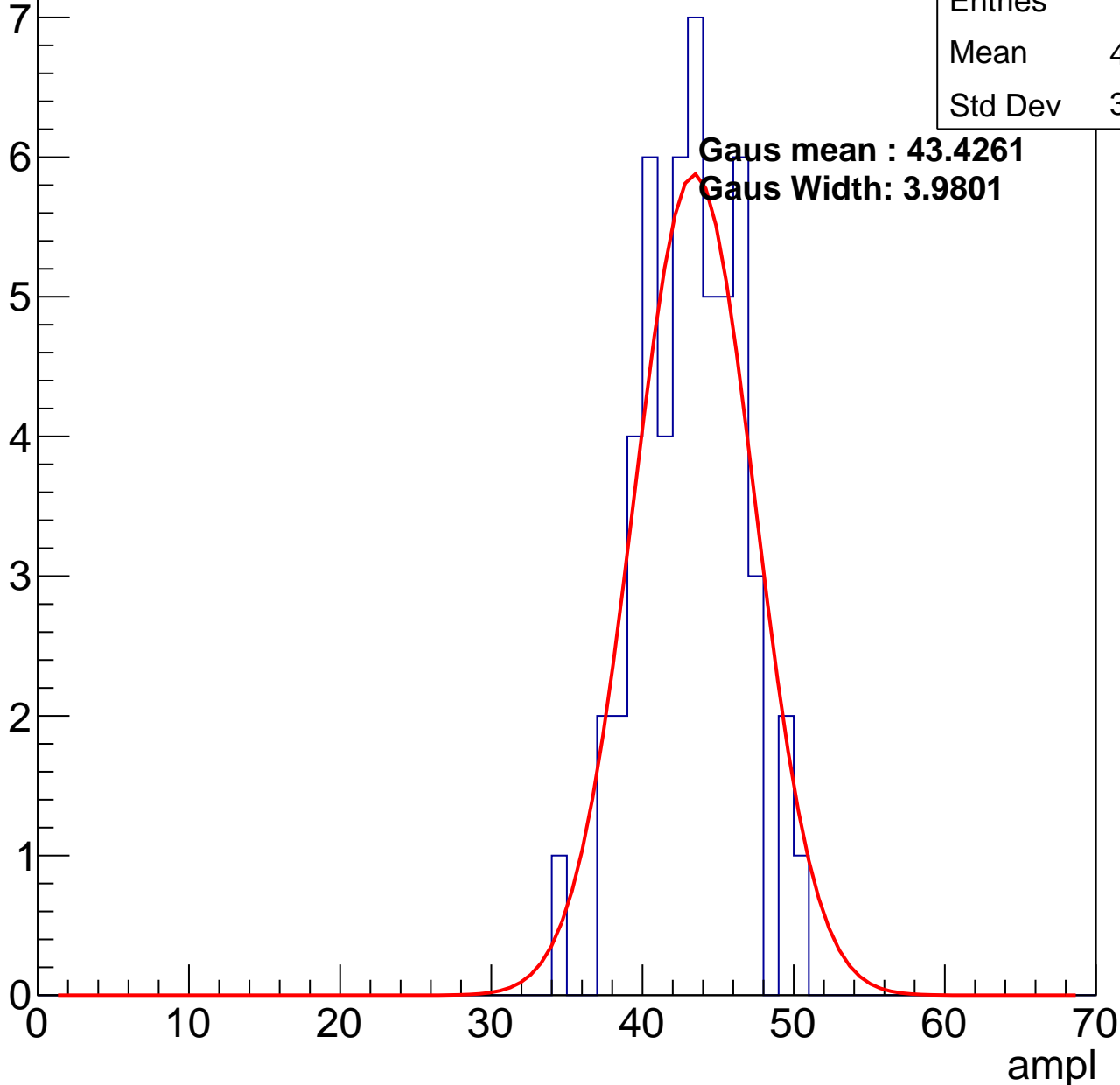
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	42.72
Std Dev	3.297

**Gaus mean : 43.4261**

**Gaus Width: 3.9801**

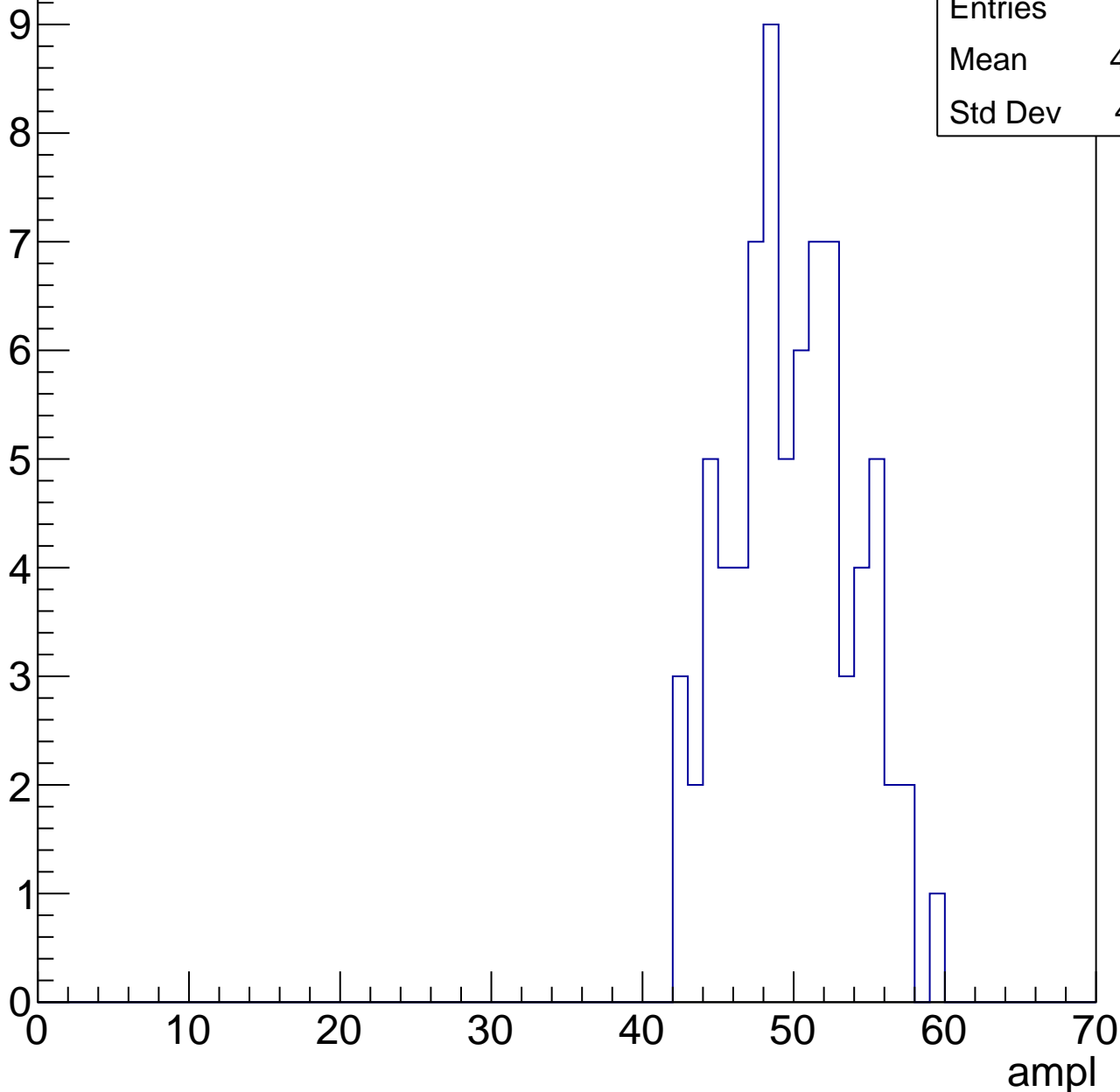


# B1L103S, U16-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	49.45
Std Dev	4.001

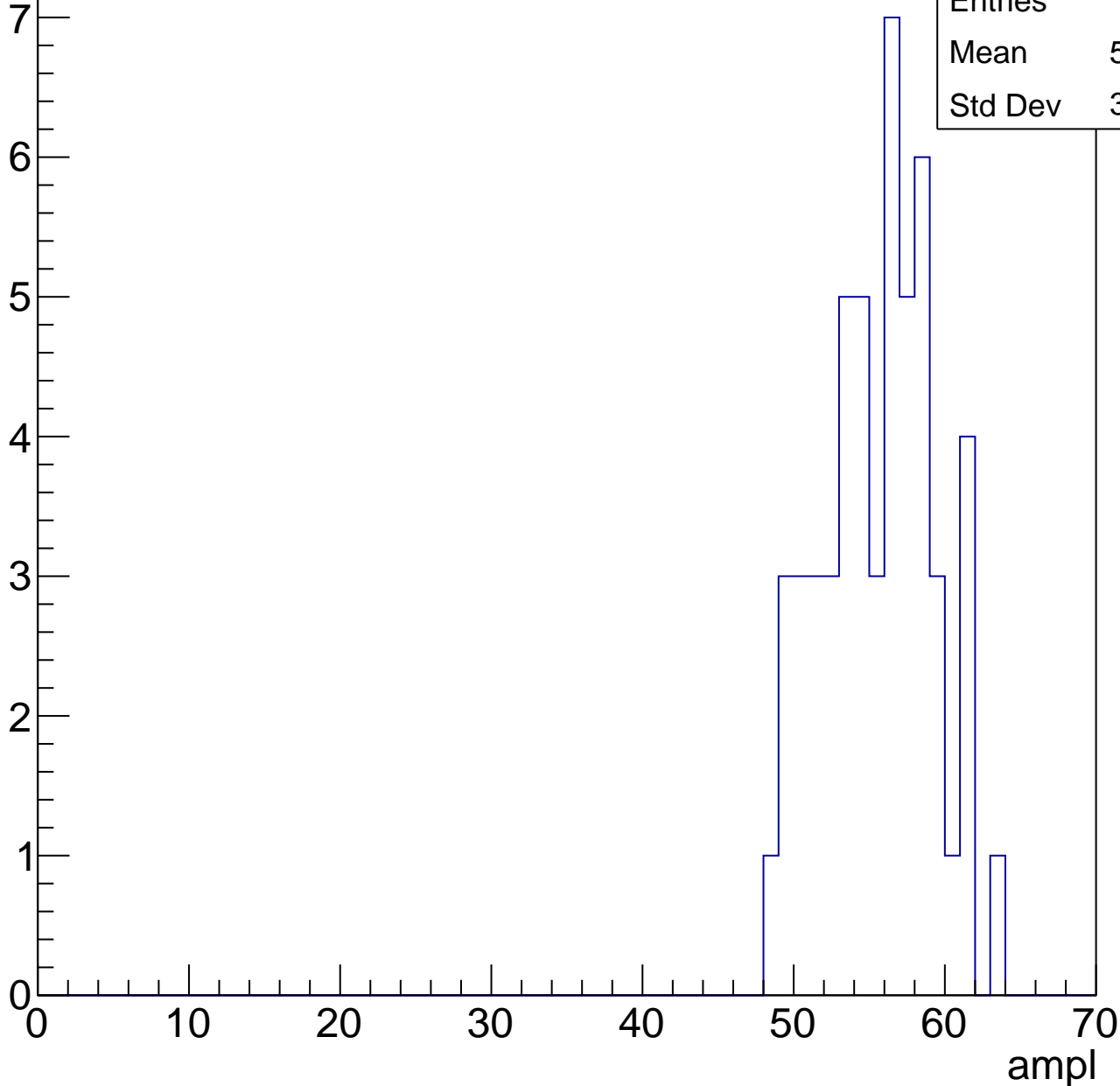


# B1L103S, U16-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

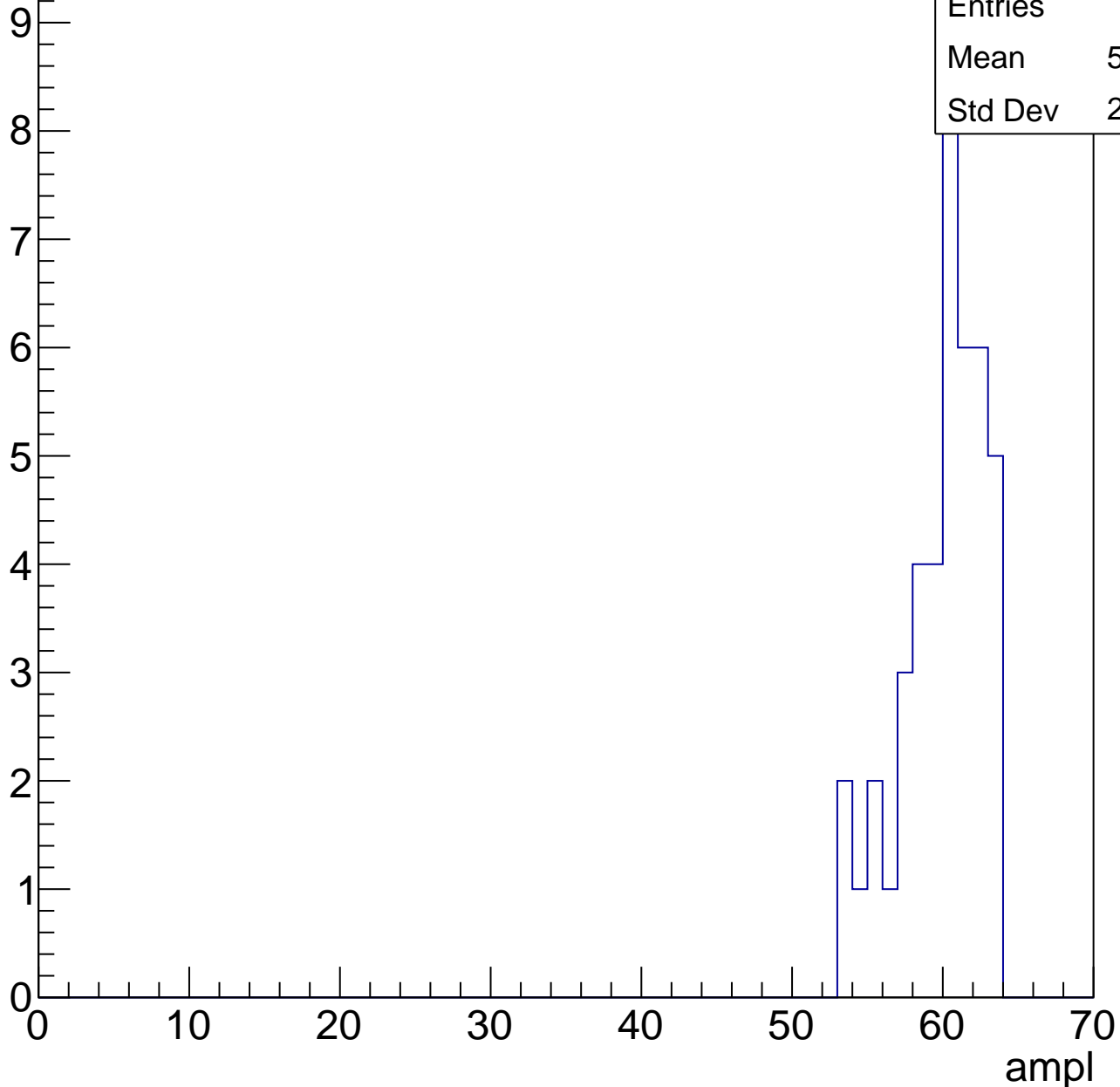
Entries	53
Mean	55.15
Std Dev	3.615



# B1L103S, U16-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

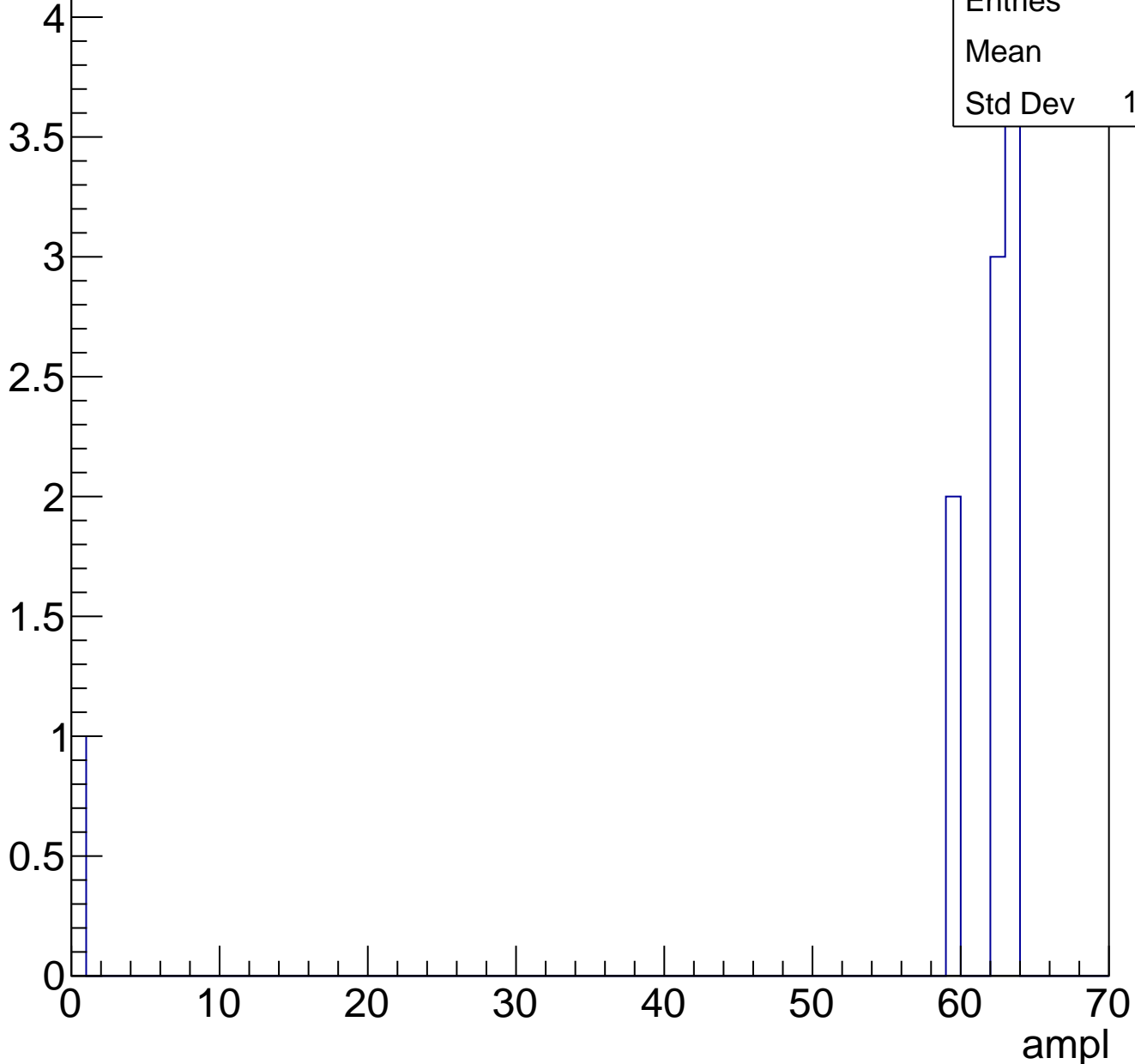
Entry



# B1L103S, U16-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

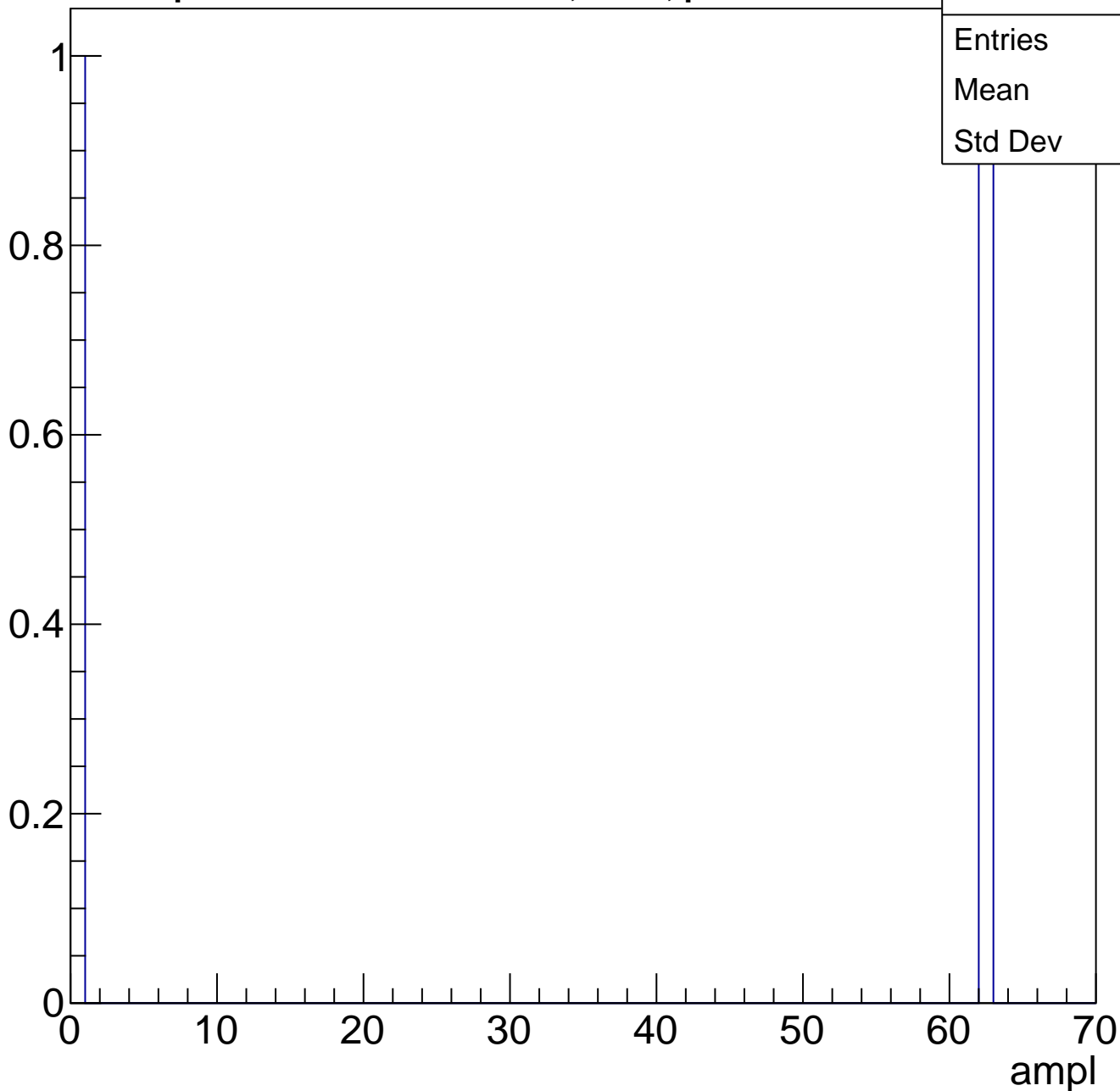




# B1L103S, U16-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch41, adc0

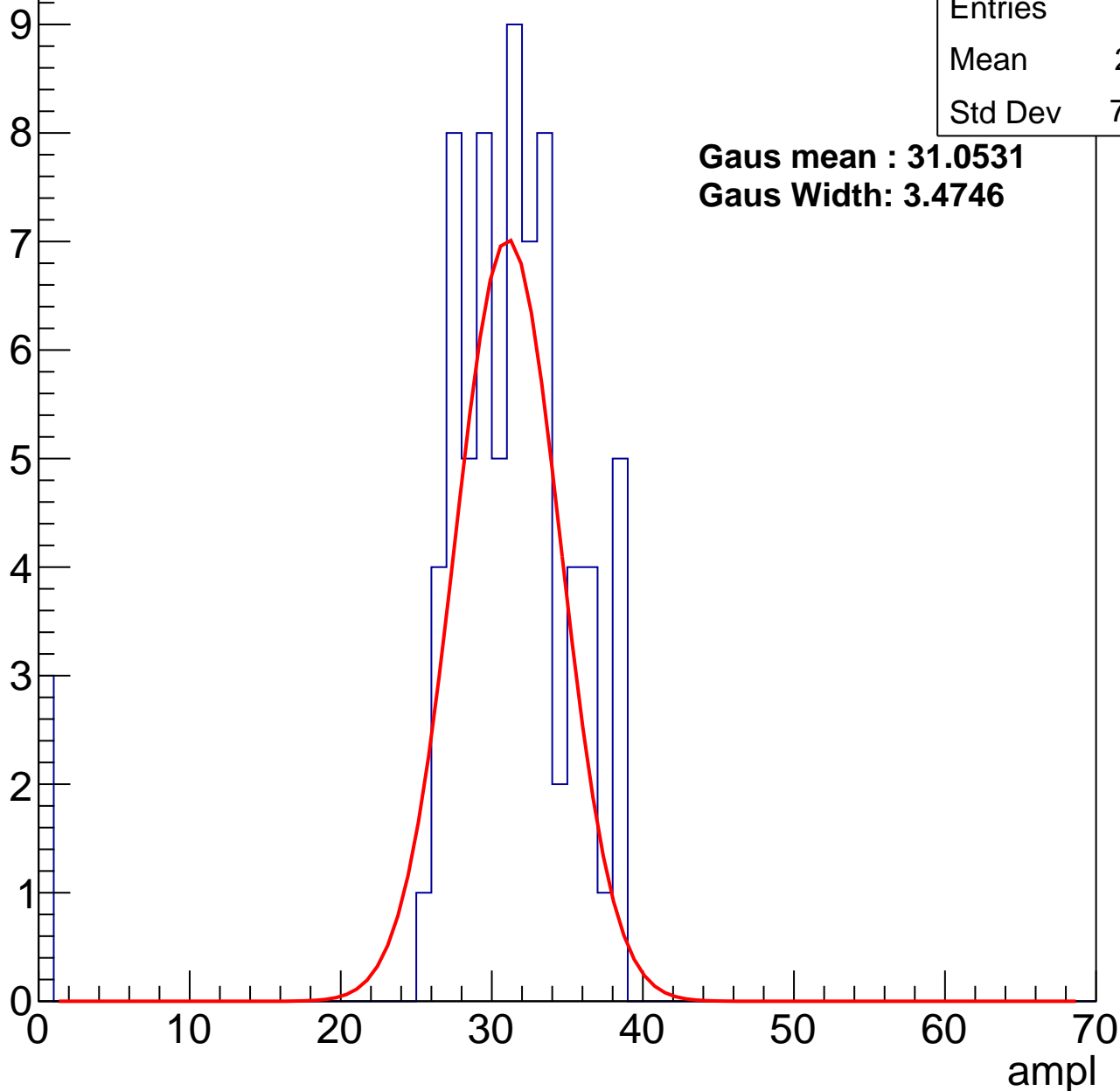
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	29.91
Std Dev	7.016

**Gaus mean : 31.0531**

**Gaus Width: 3.4746**



# B1L103S, U16-ch41, adc1

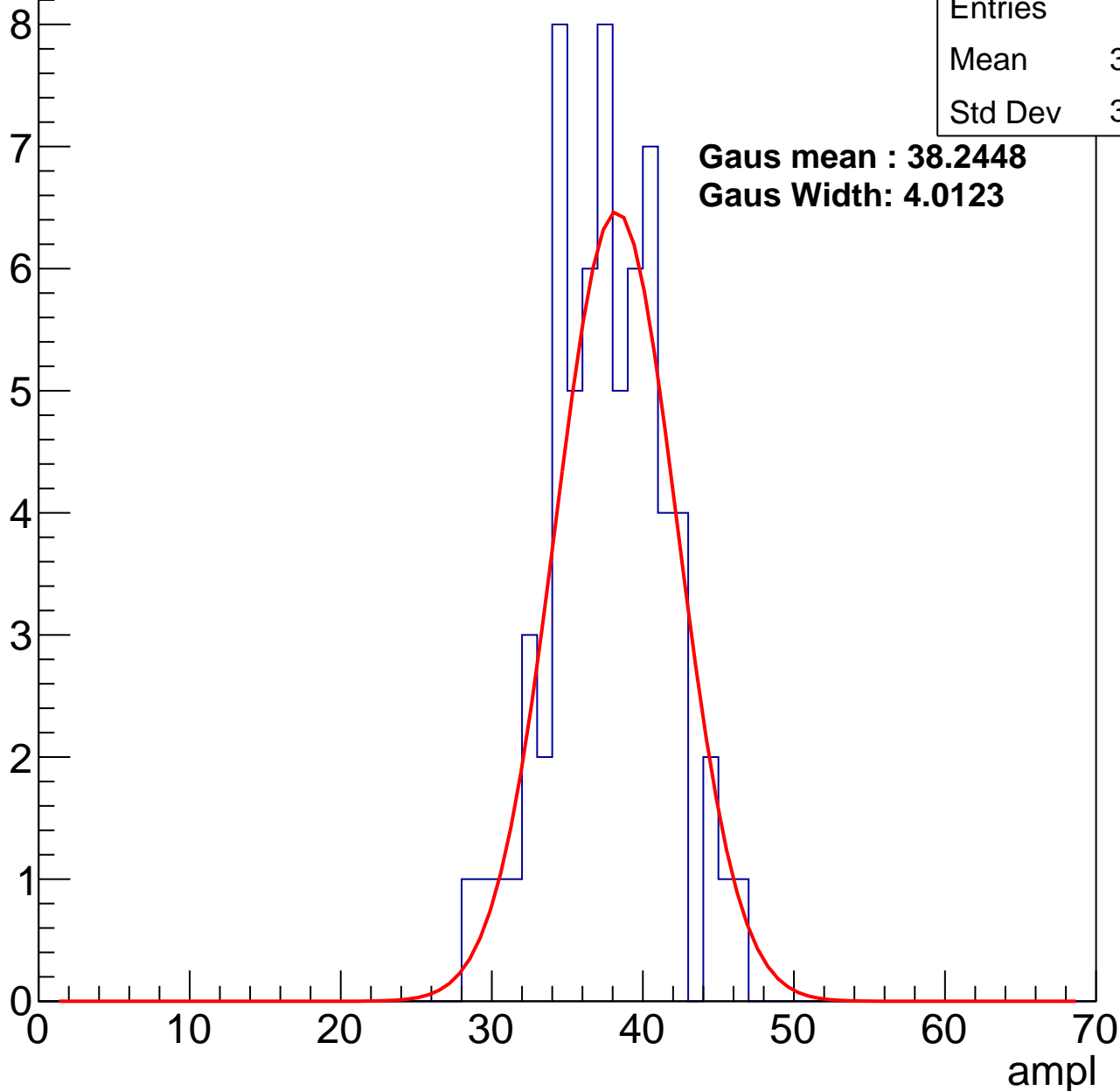
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	37.18
Std Dev	3.757

**Gaus mean : 38.2448**

**Gaus Width: 4.0123**



# B1L103S, U16-ch41, adc2

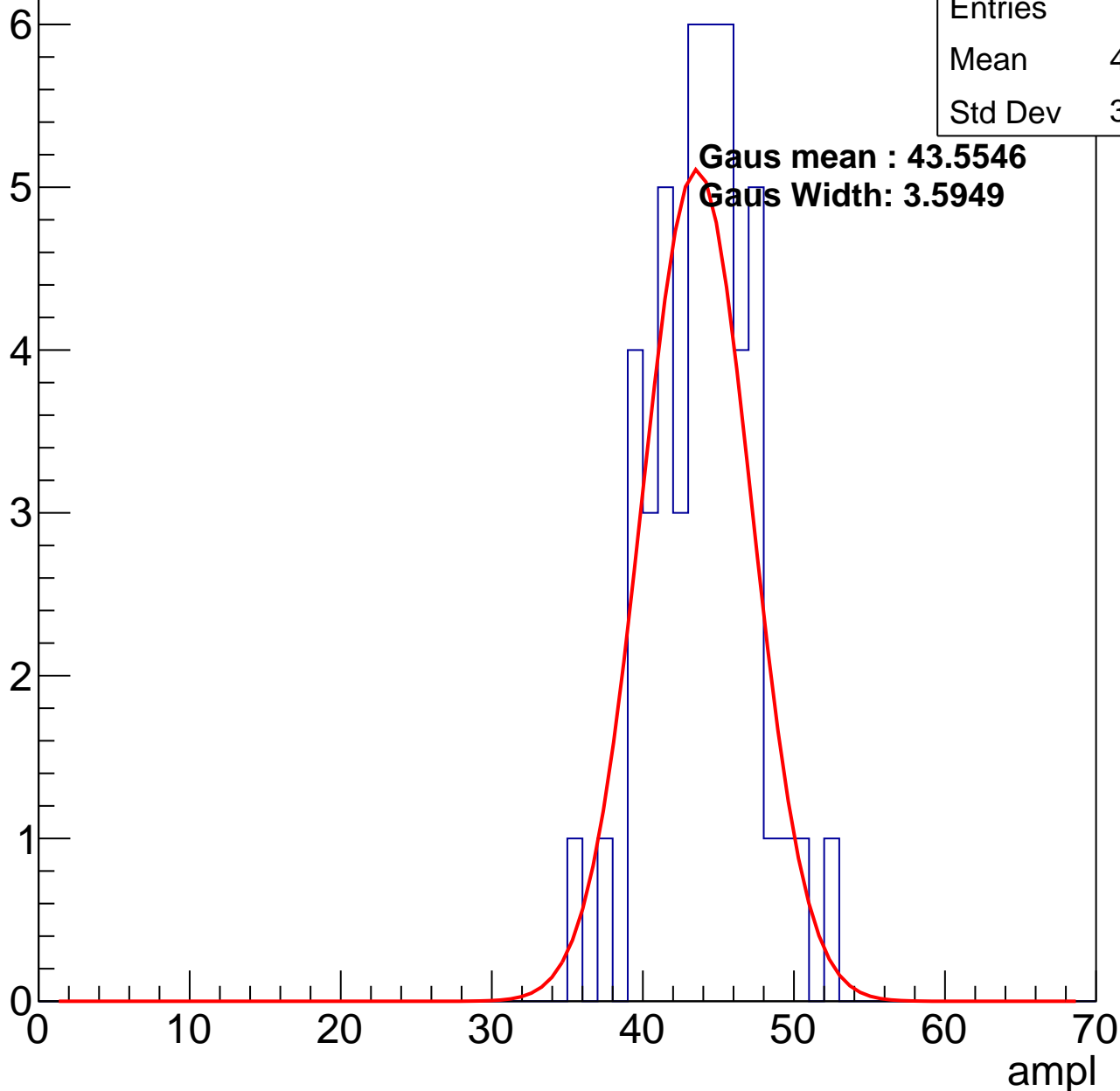
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	43.52
Std Dev	3.348

**Gaus mean : 43.5546**

**Gaus Width: 3.5949**

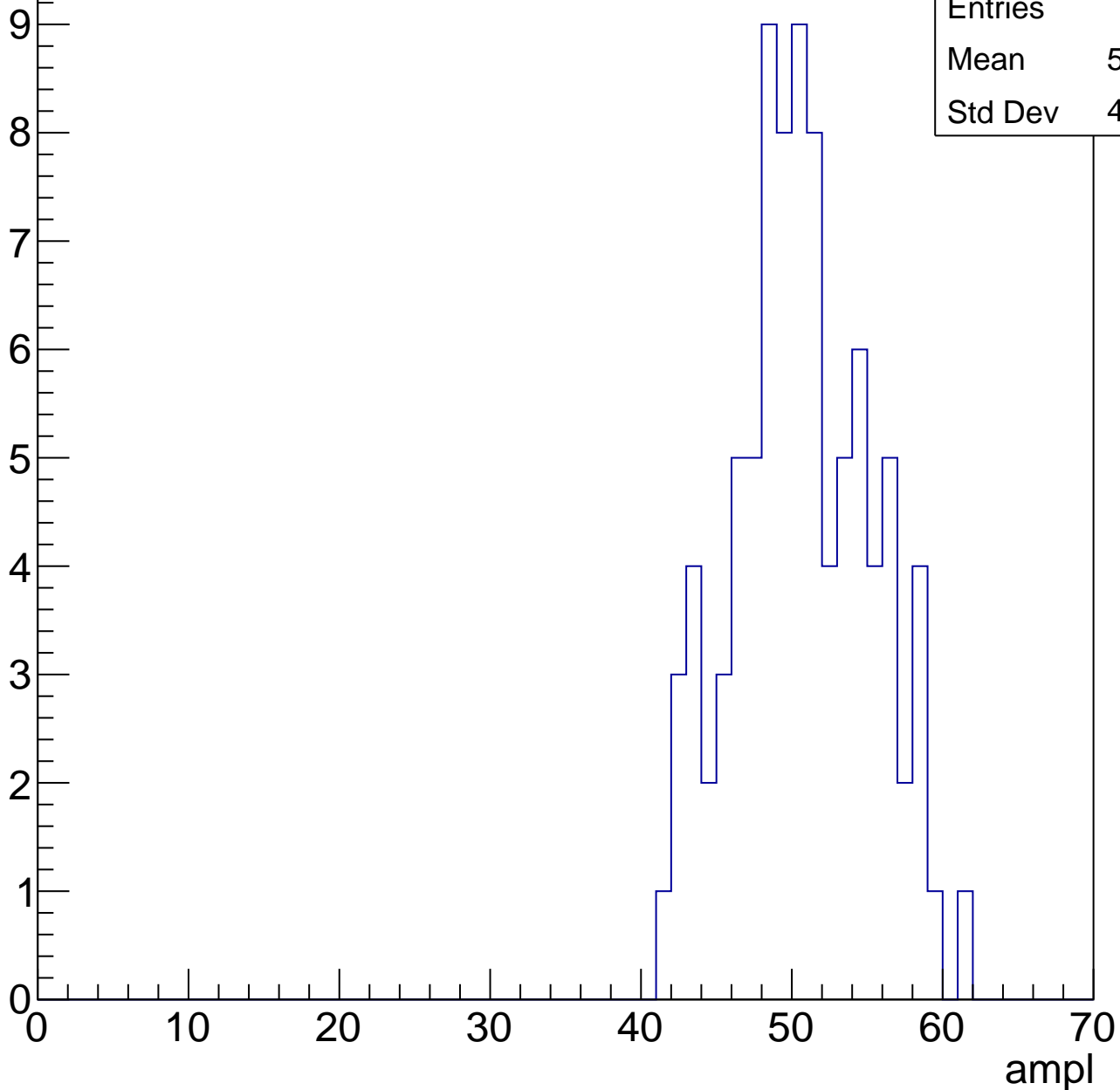


# B1L103S, U16-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	89
Mean	50.25
Std Dev	4.473

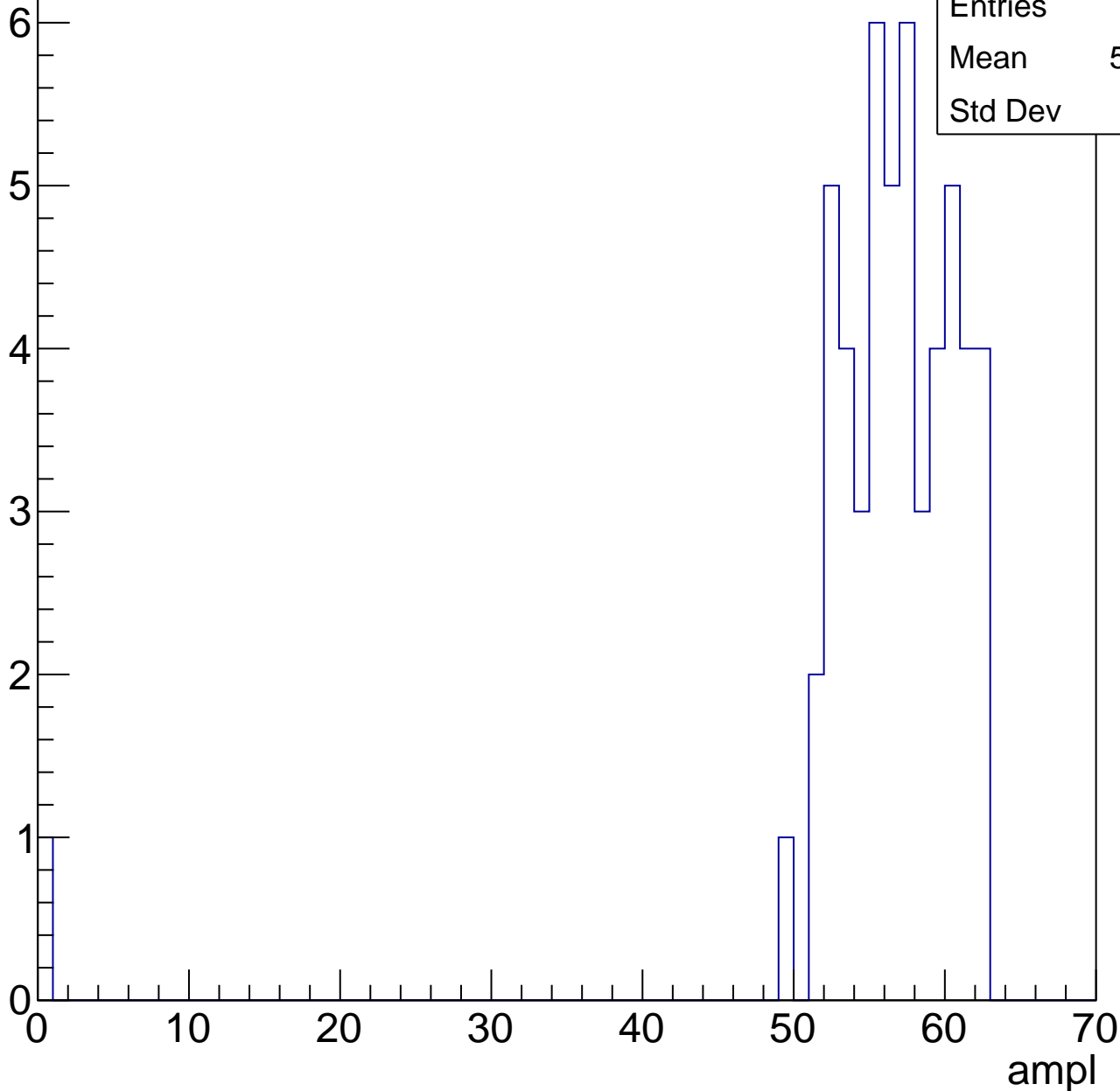


# B1L103S, U16-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	55.45
Std Dev	8.39

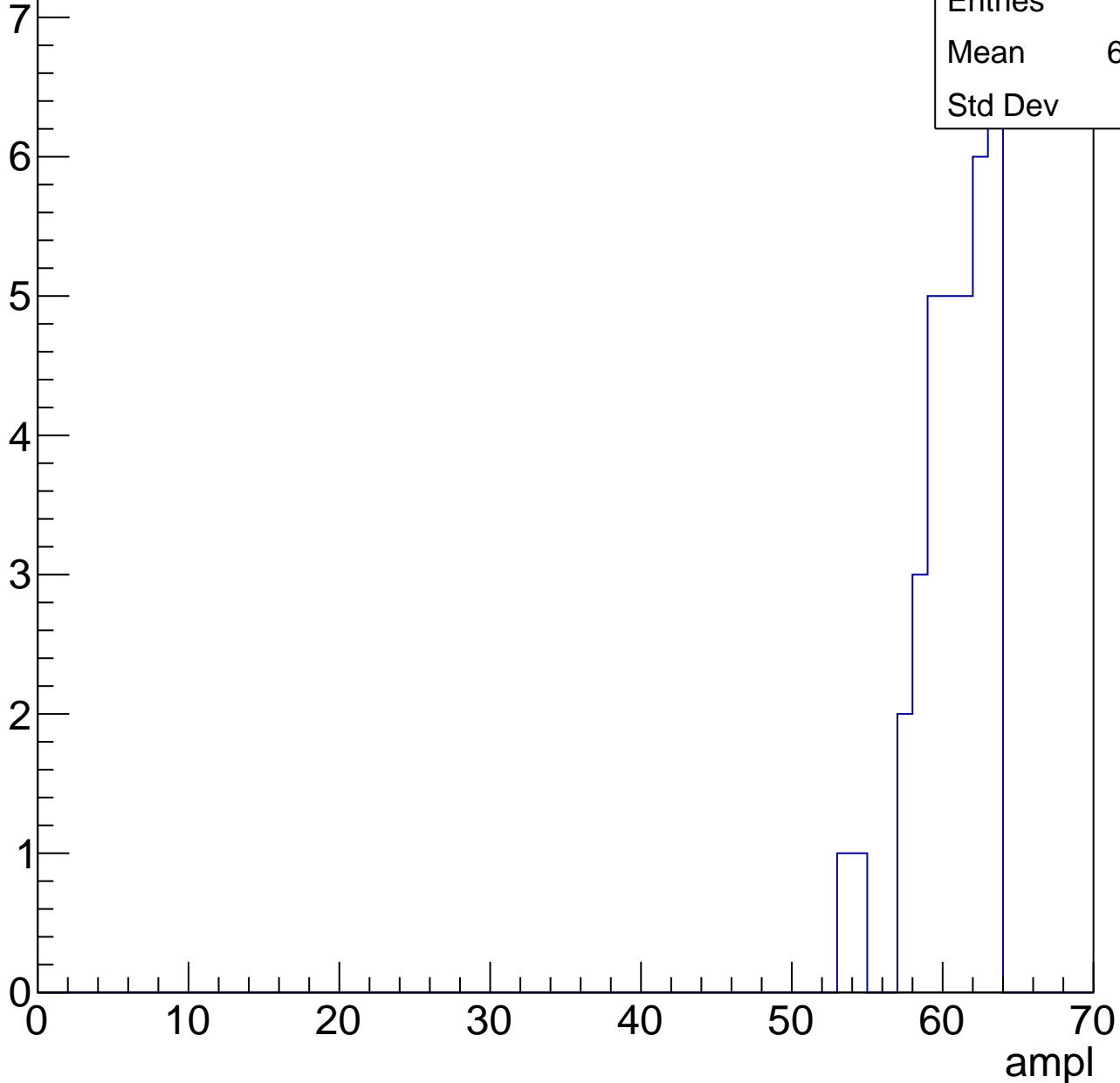


# B1L103S, U16-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	35
Mean	60.23
Std Dev	2.45



# B1L103S, U16-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U16-ch42, adc0

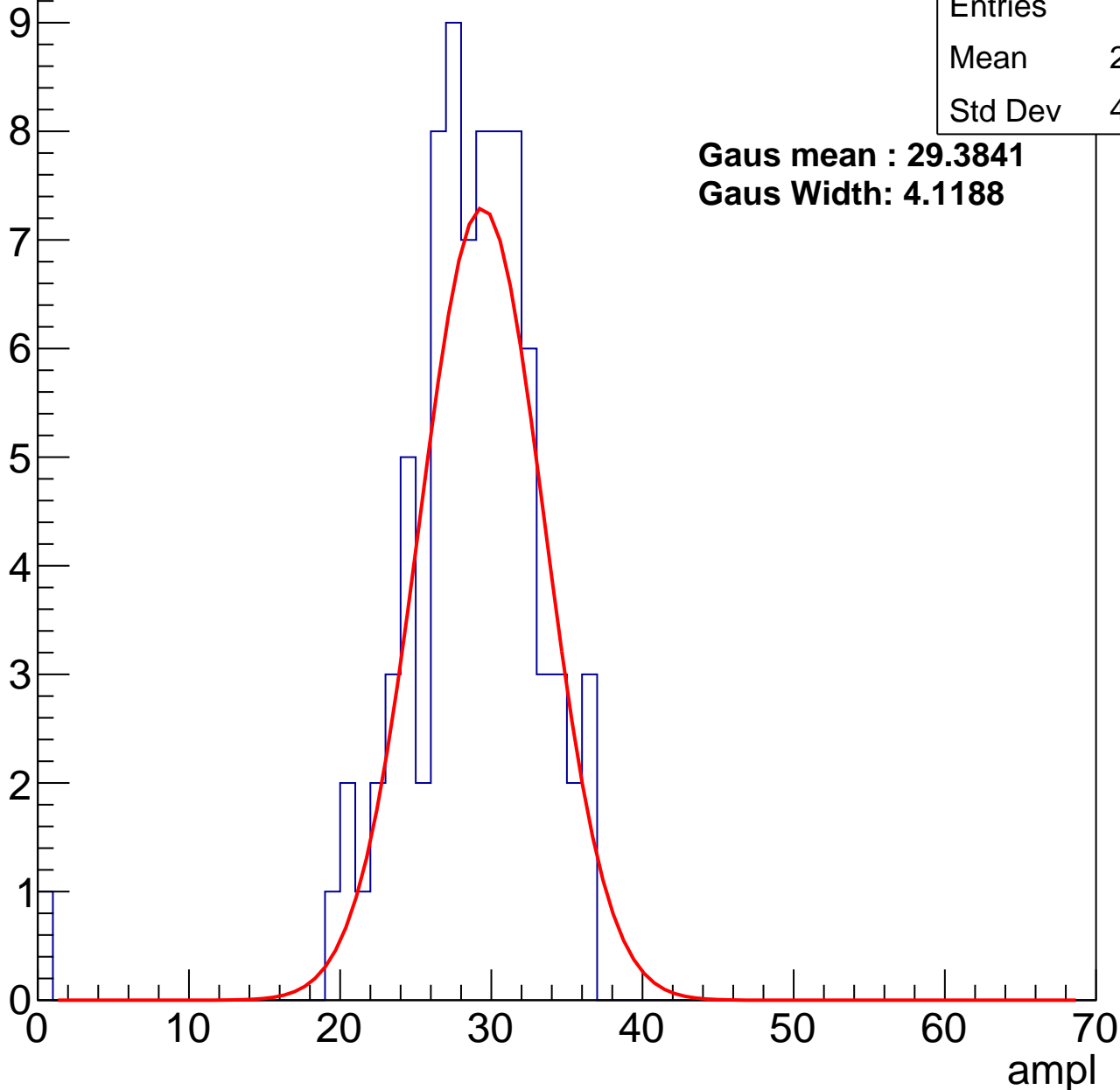
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	82
Mean	28.06
Std Dev	4.949

**Gaus mean : 29.3841**

**Gaus Width: 4.1188**



# B1L103S, U16-ch42, adc1

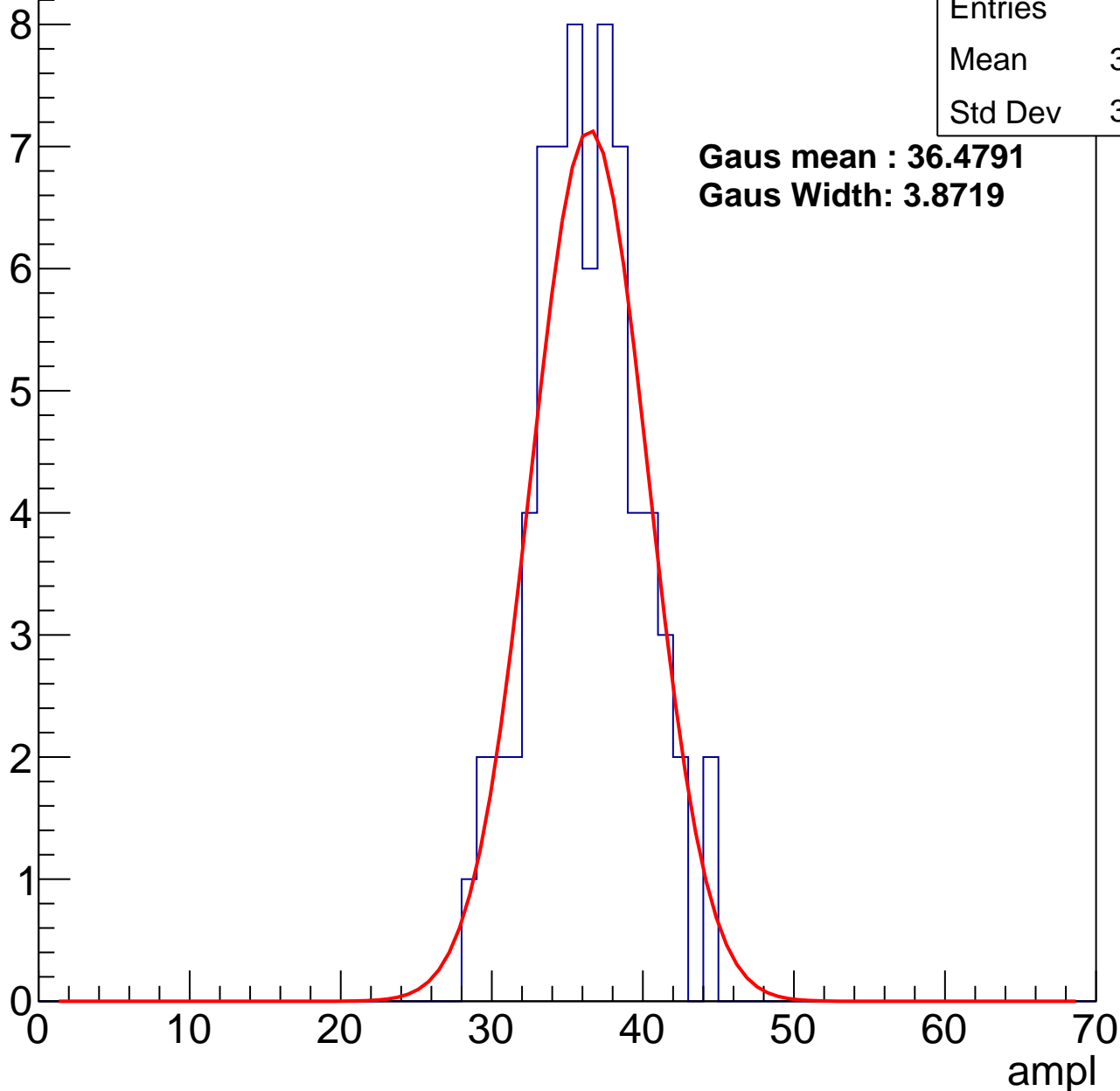
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	35.86
Std Dev	3.523

**Gaus mean : 36.4791**

**Gaus Width: 3.8719**



# B1L103S, U16-ch42, adc2

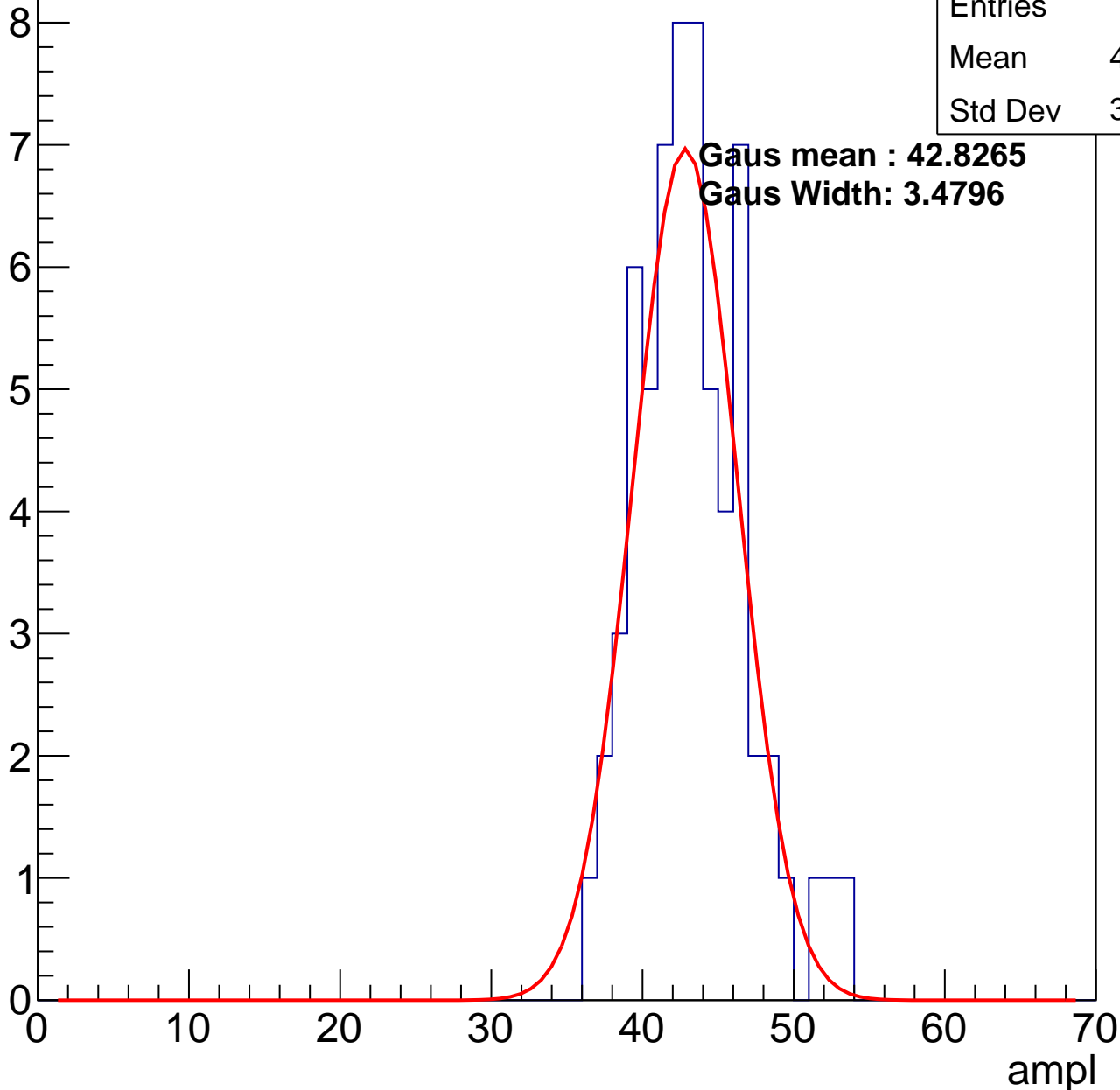
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	42.84
Std Dev	3.576

**Gaus mean : 42.8265**

**Gaus Width: 3.4796**

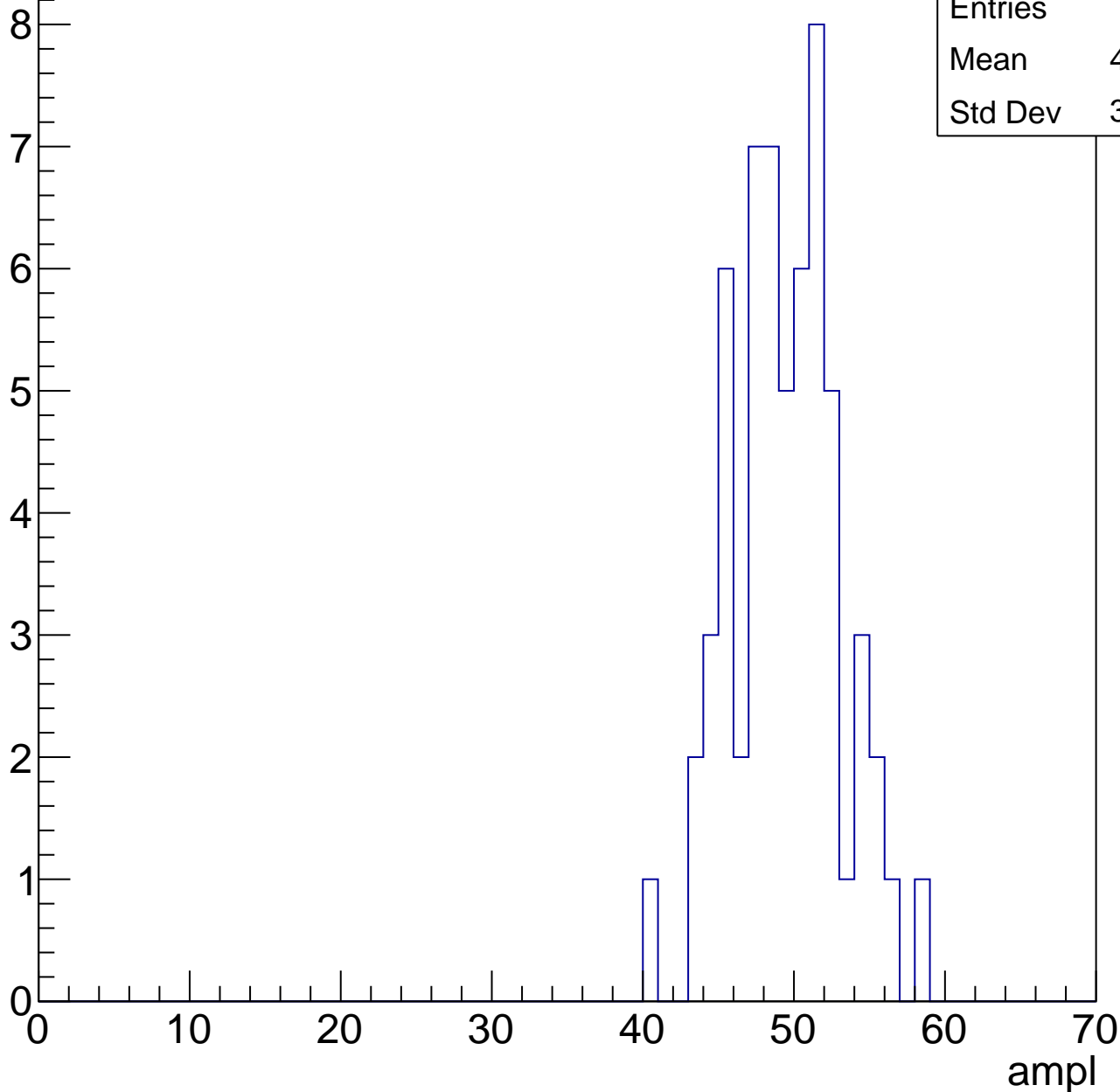


# B1L103S, U16-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	48.95
Std Dev	3.542



# B1L103S, U16-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

7

6

5

4

3

2

1

0

Entries 49

Mean 53.86

Std Dev 3.54

ampl

0

10

20

30

40

50

60

70

0

1

2

3

4

5

6

7

# B1L103S, U16-ch42, adc5

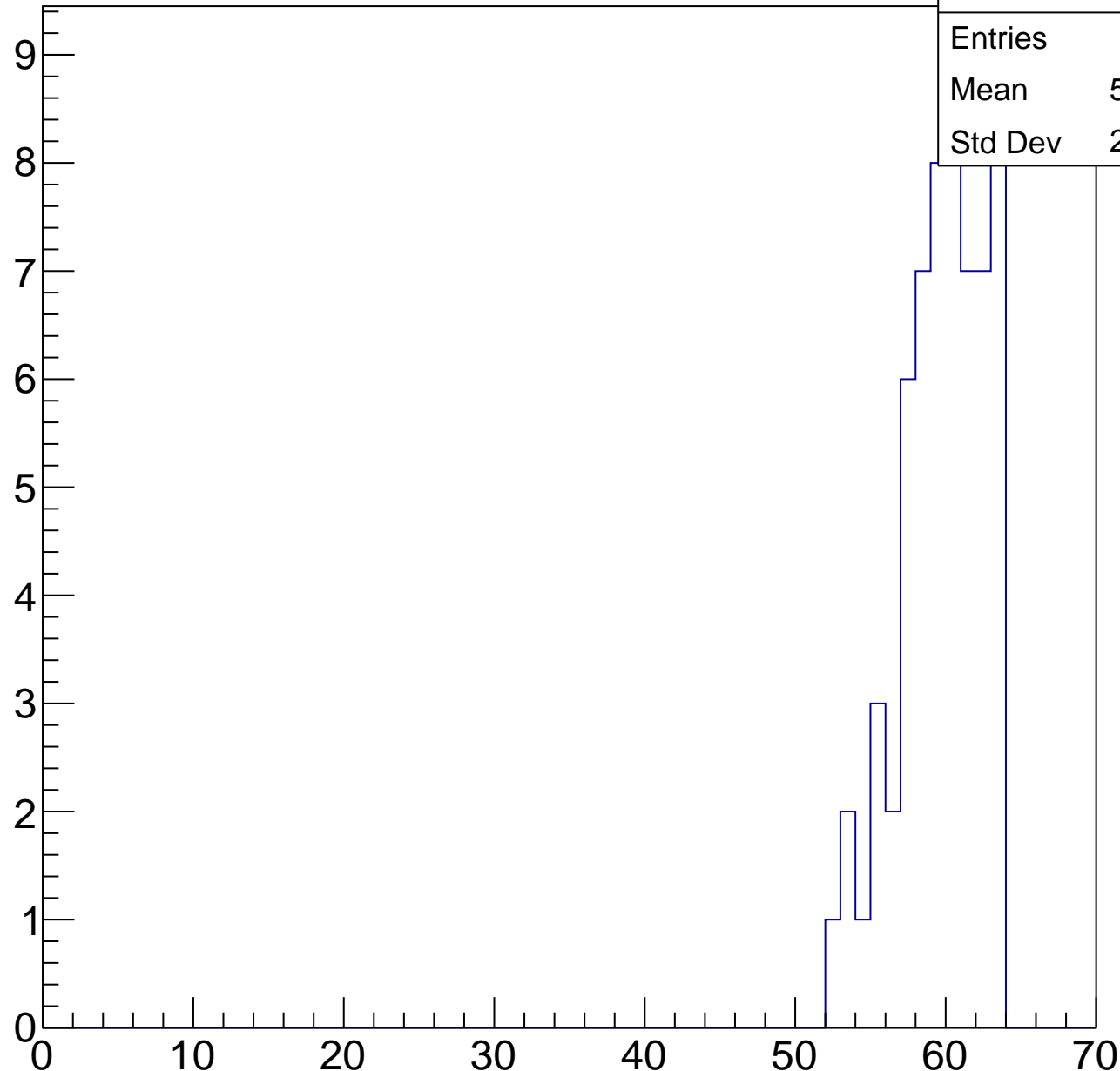
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	61
Mean	59.25
Std Dev	2.768

ampl



# B1L103S, U16-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

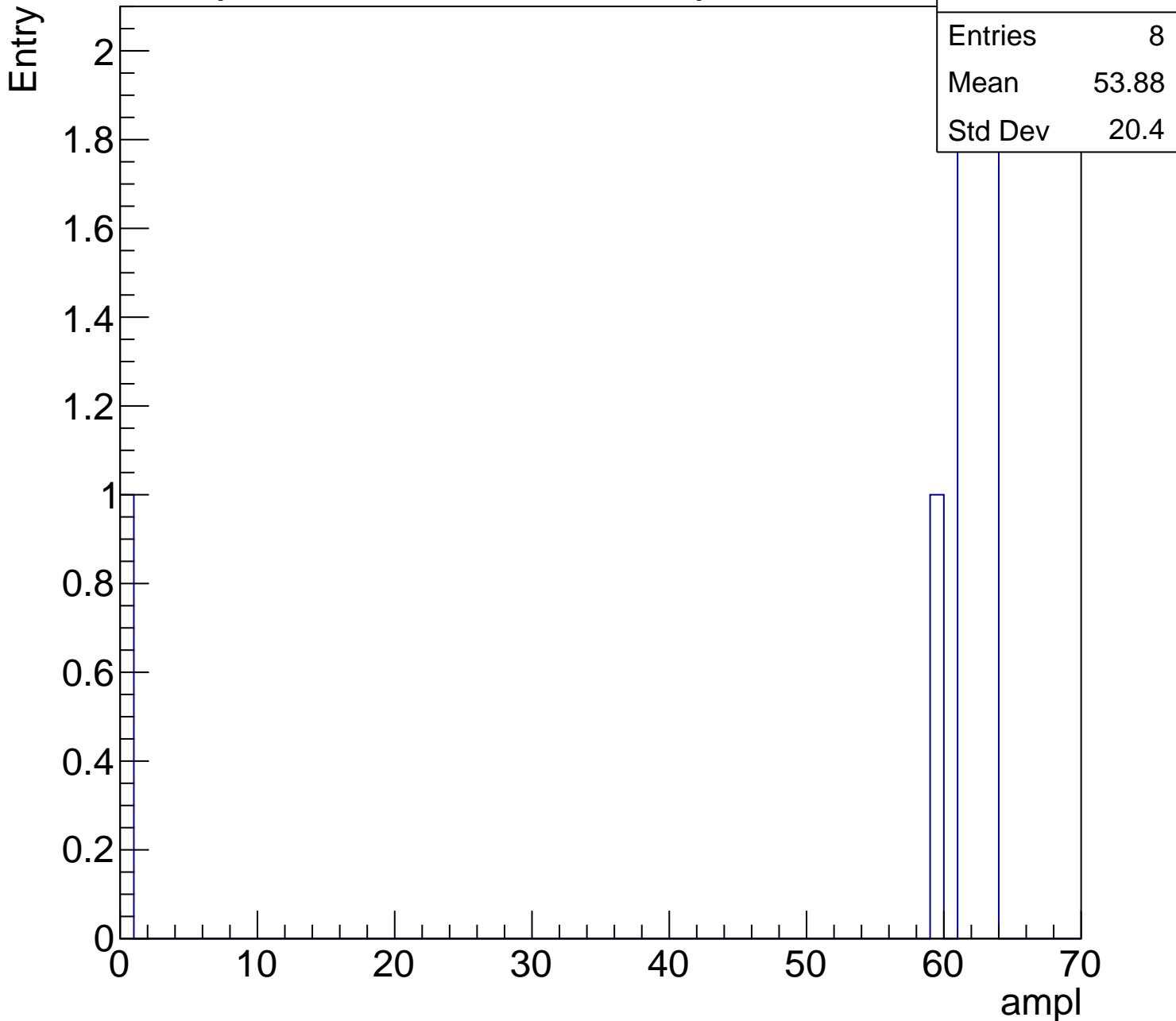
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	8
Mean	53.88
Std Dev	20.4

0 10 20 30 40 50 60 70

ampl





# B1L103S, U16-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L103S, U16-ch43, adc0

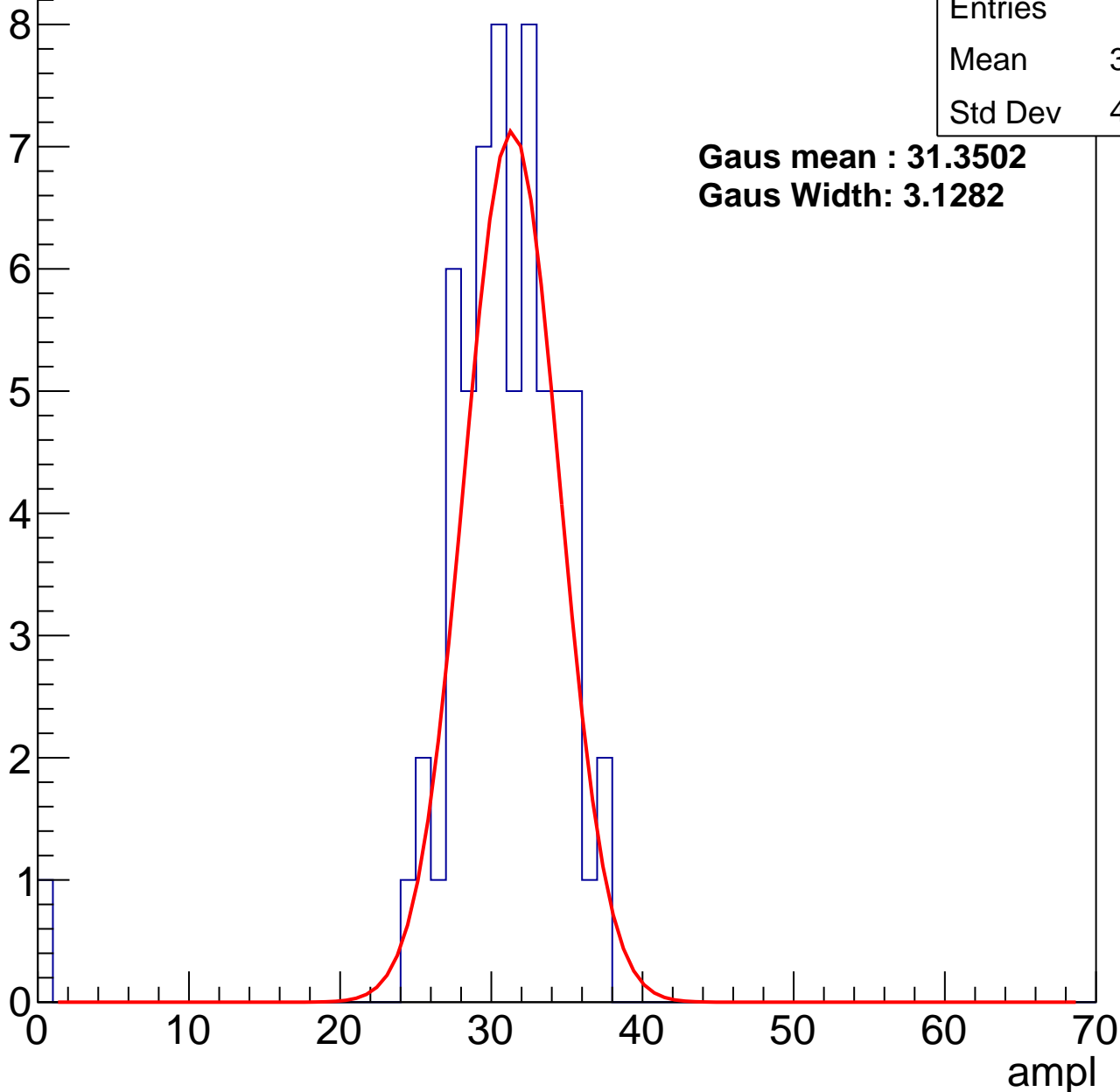
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	30.26
Std Dev	4.918

**Gaus mean : 31.3502**

**Gaus Width: 3.1282**



# B1L103S, U16-ch43, adc1

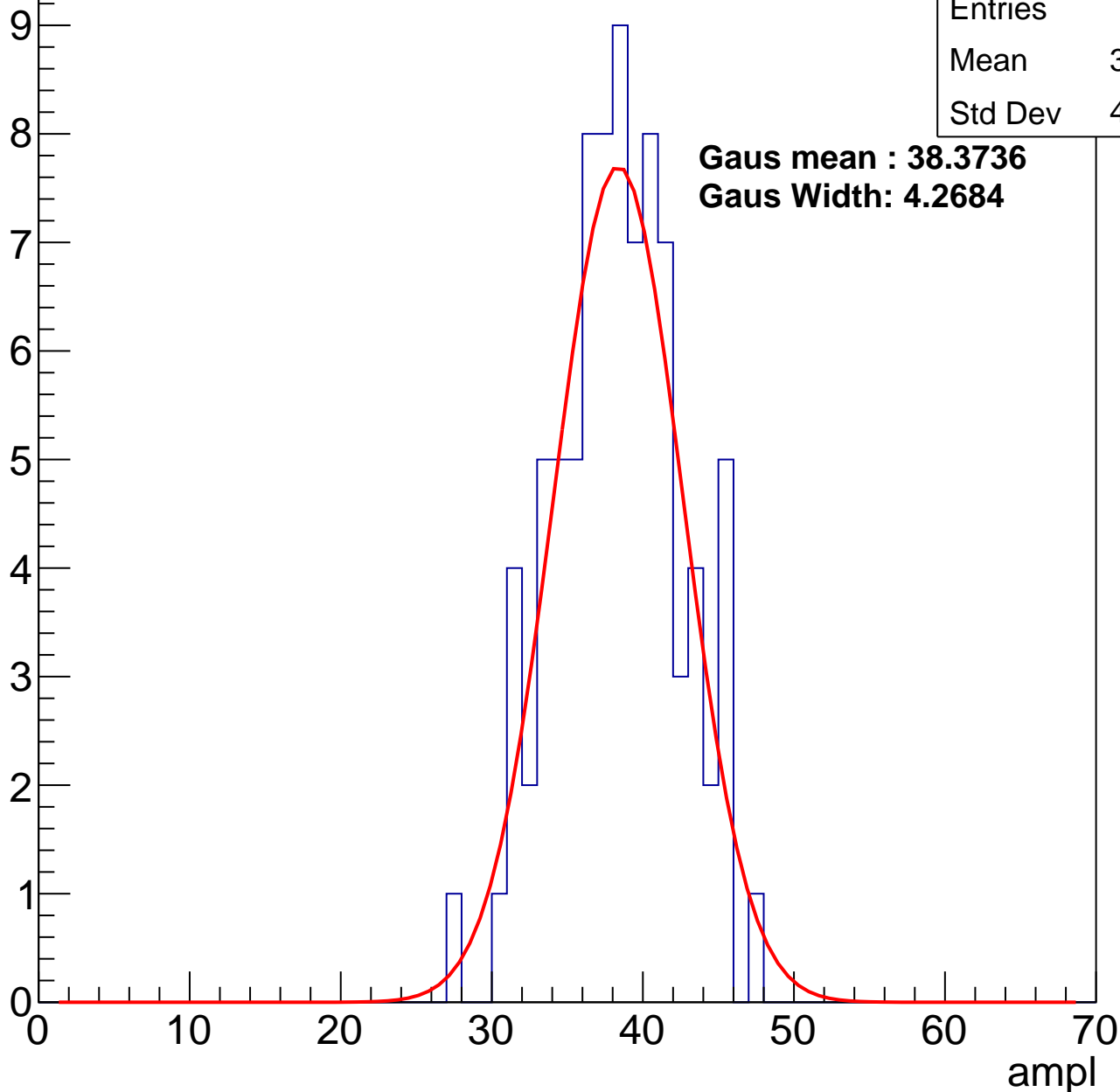
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	85
Mean	37.87
Std Dev	4.043

**Gaus mean : 38.3736**

**Gaus Width: 4.2684**



# B1L103S, U16-ch43, adc2

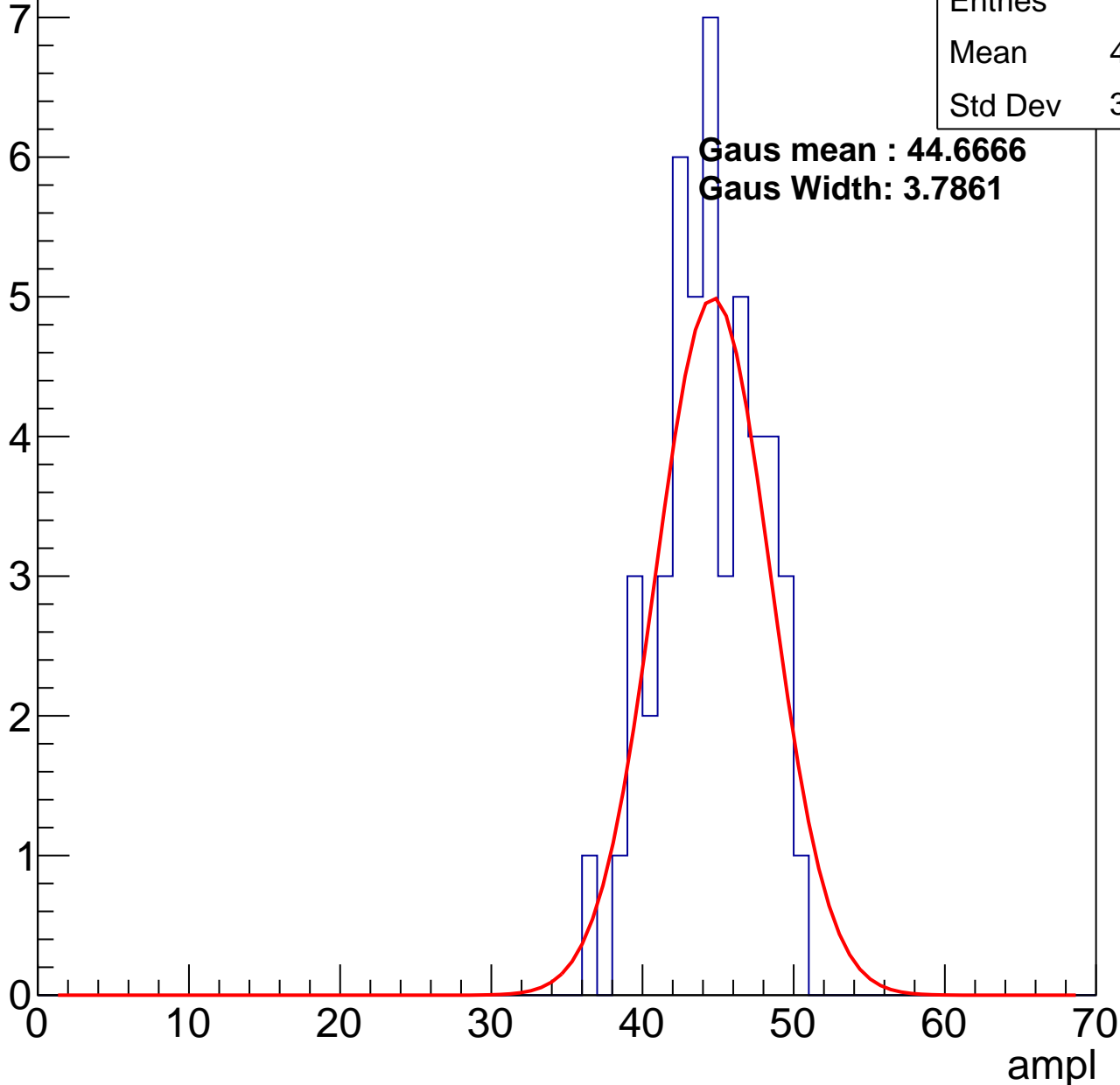
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	43.98
Std Dev	3.218

**Gaus mean : 44.6666**

**Gaus Width: 3.7861**

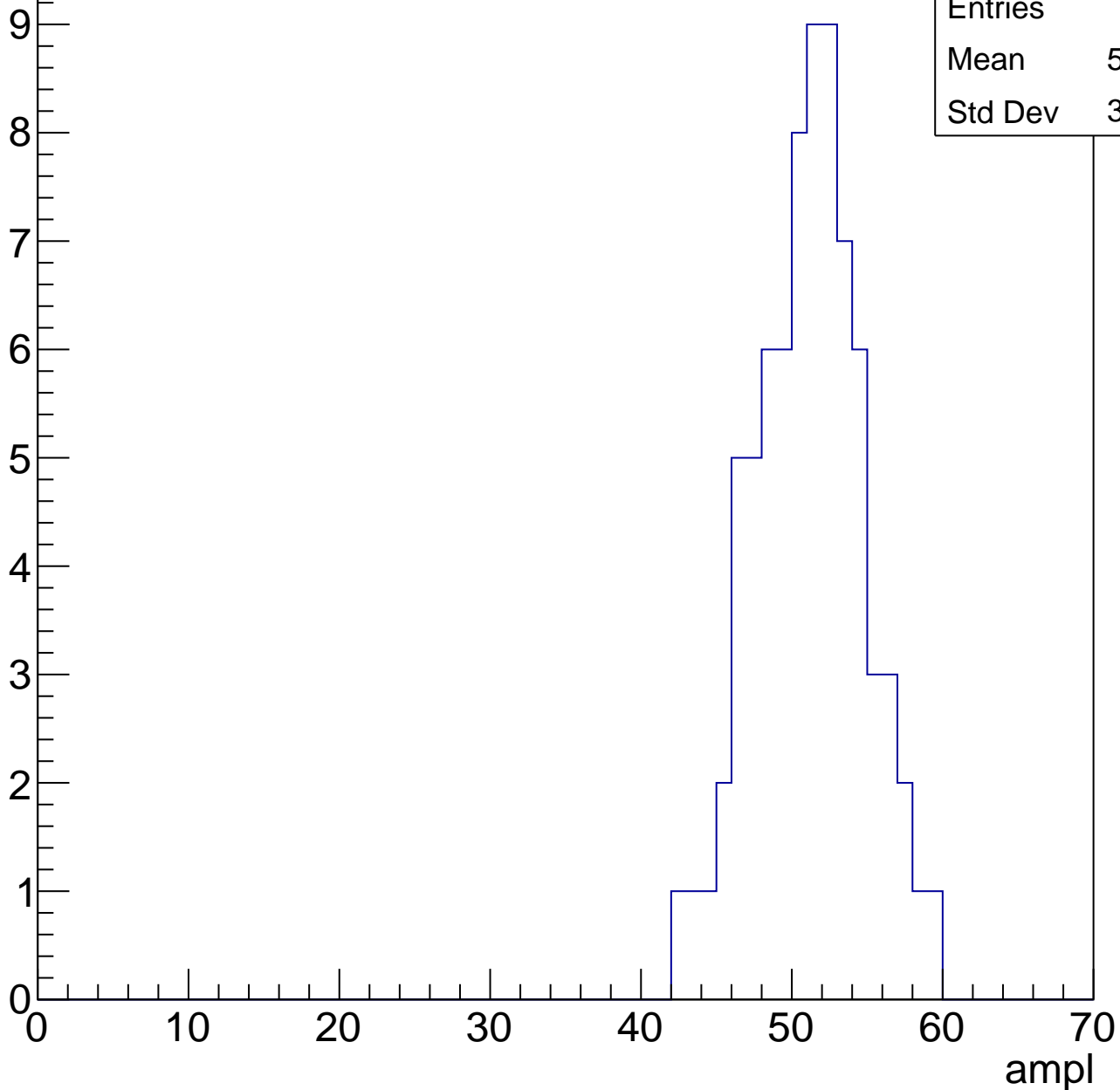


# B1L103S, U16-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	50.68
Std Dev	3.533

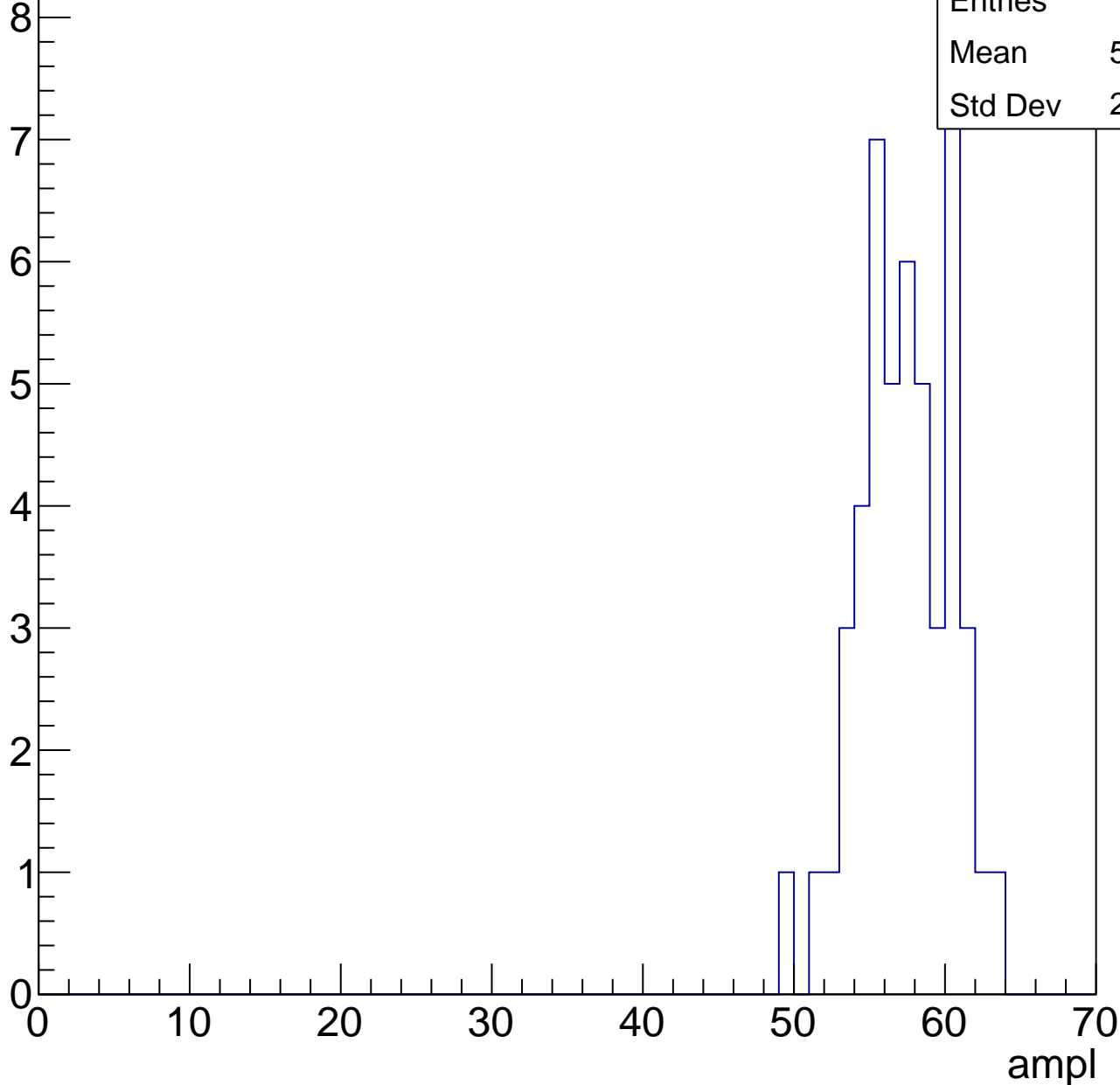


# B1L103S, U16-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	56.92
Std Dev	2.995

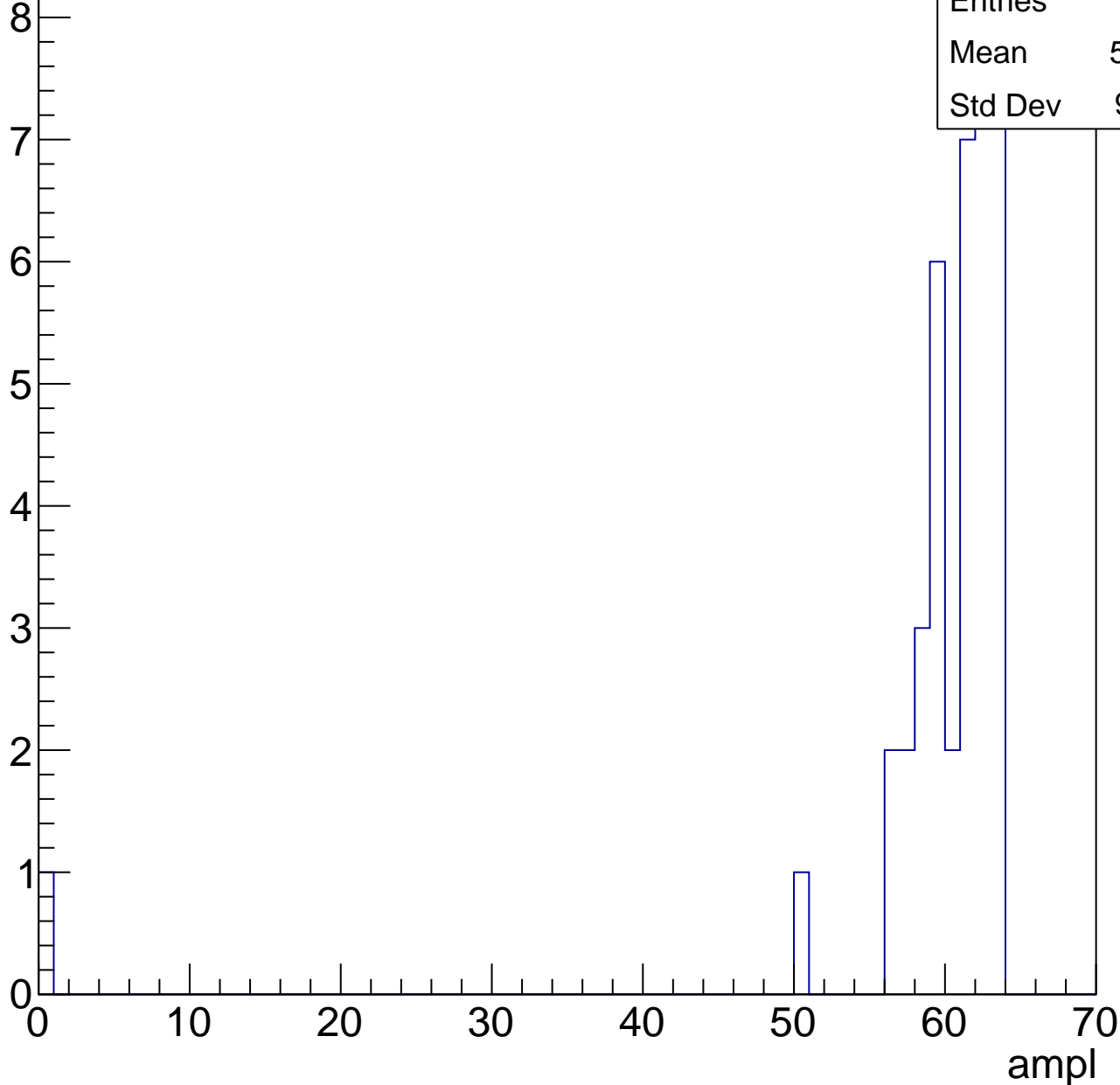


# B1L103S, U16-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

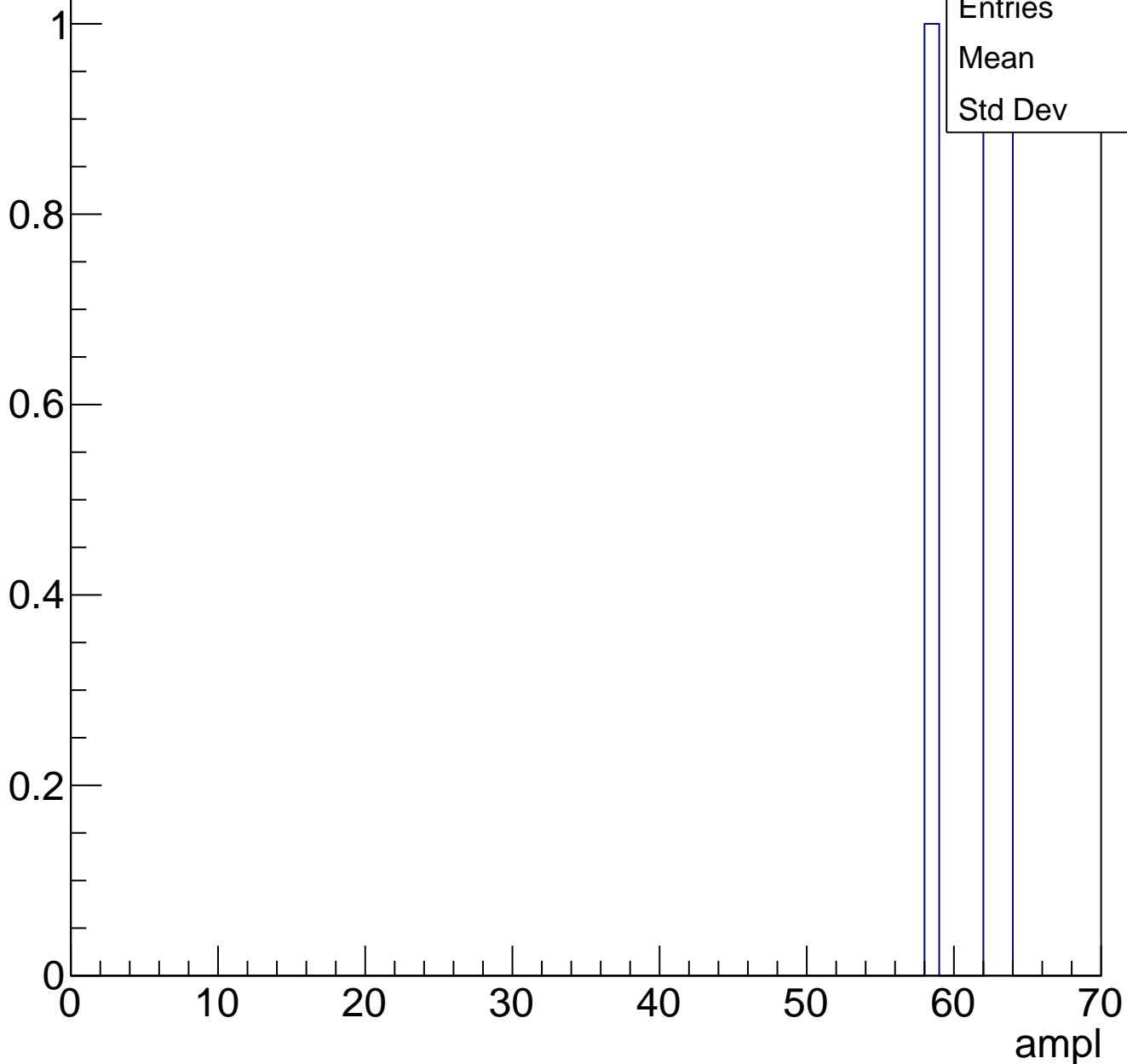
Entries	40
Mean	58.77
Std Dev	9.771



# B1L103S, U16-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch44, adc0

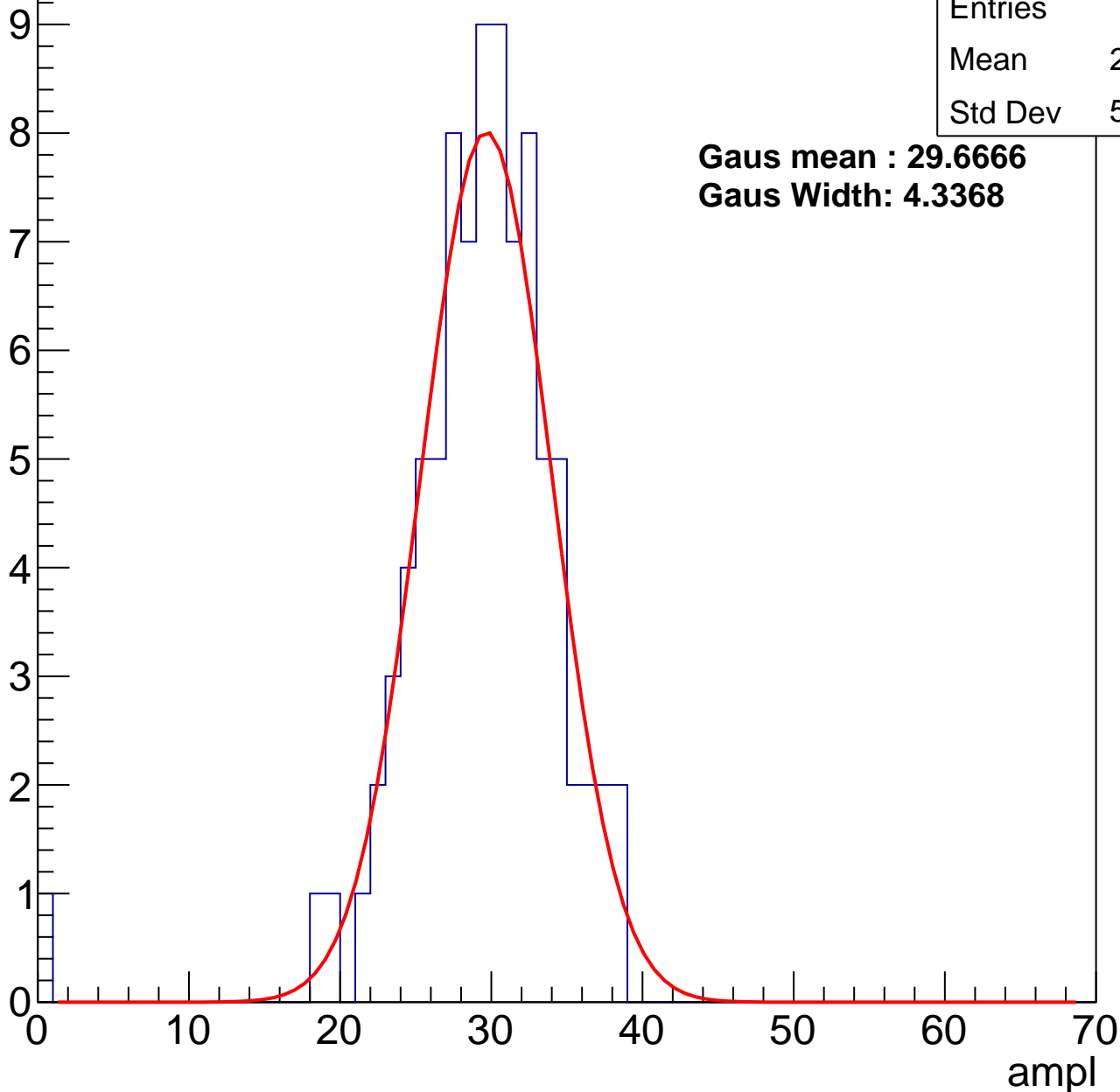
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	89
Mean	28.82
Std Dev	5.157

**Gaus mean : 29.6666**

**Gaus Width: 4.3368**



# B1L103S, U16-ch44, adc1

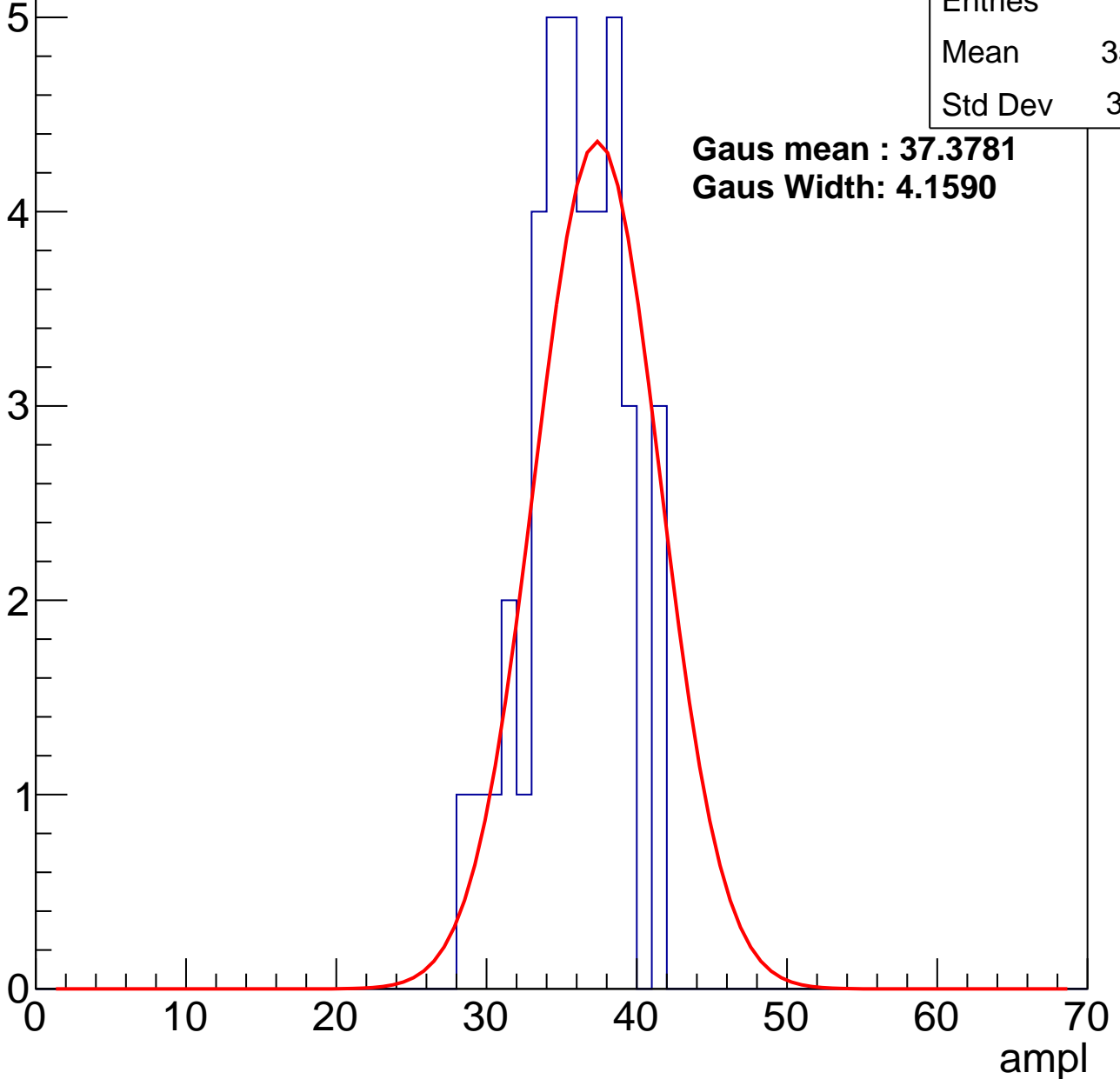
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	39
Mean	35.38
Std Dev	3.151

**Gaus mean : 37.3781**

**Gaus Width: 4.1590**



# B1L103S, U16-ch44, adc2

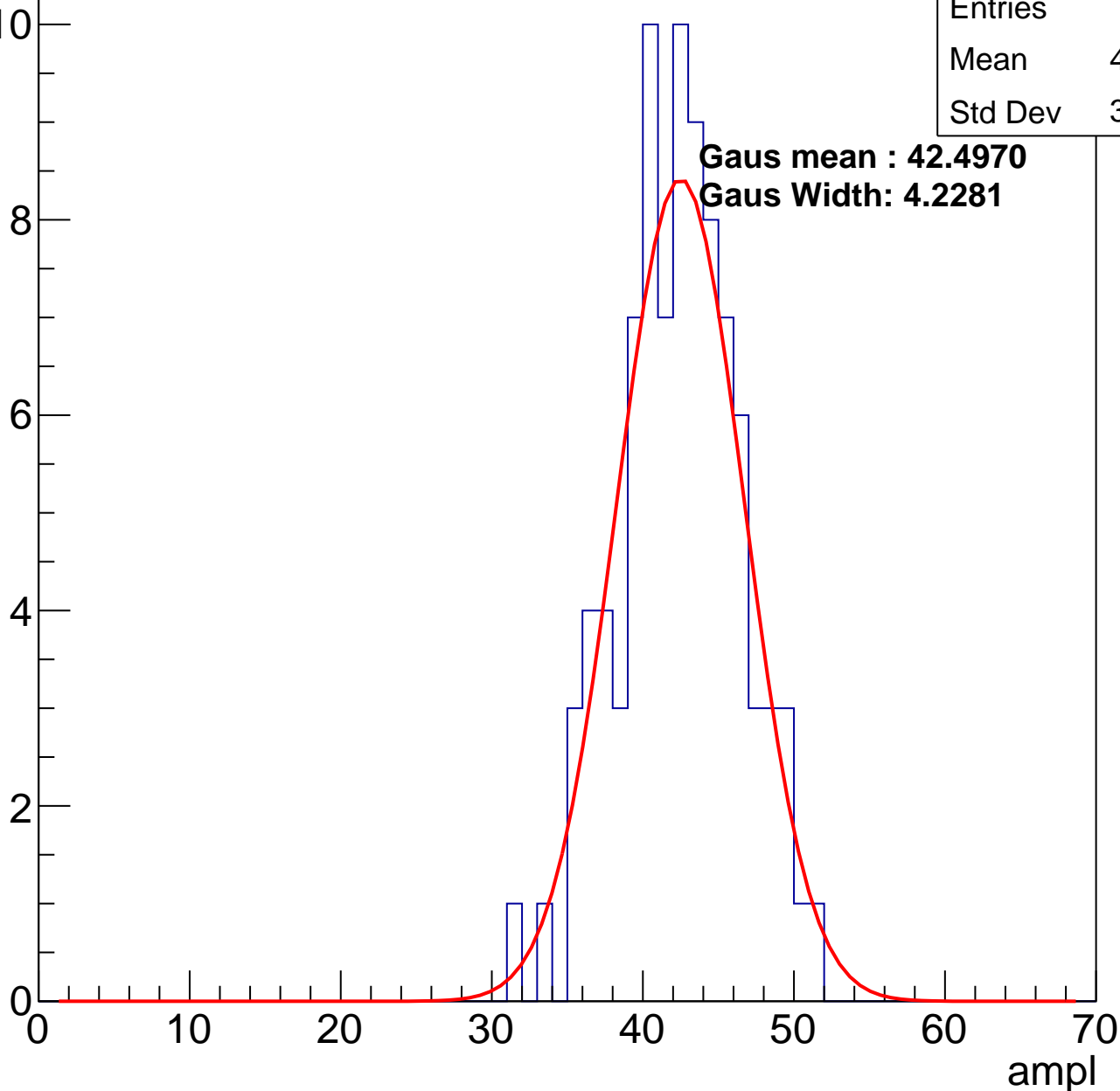
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	91
Mean	41.96
Std Dev	3.958

**Gaus mean : 42.4970**

**Gaus Width: 4.2281**

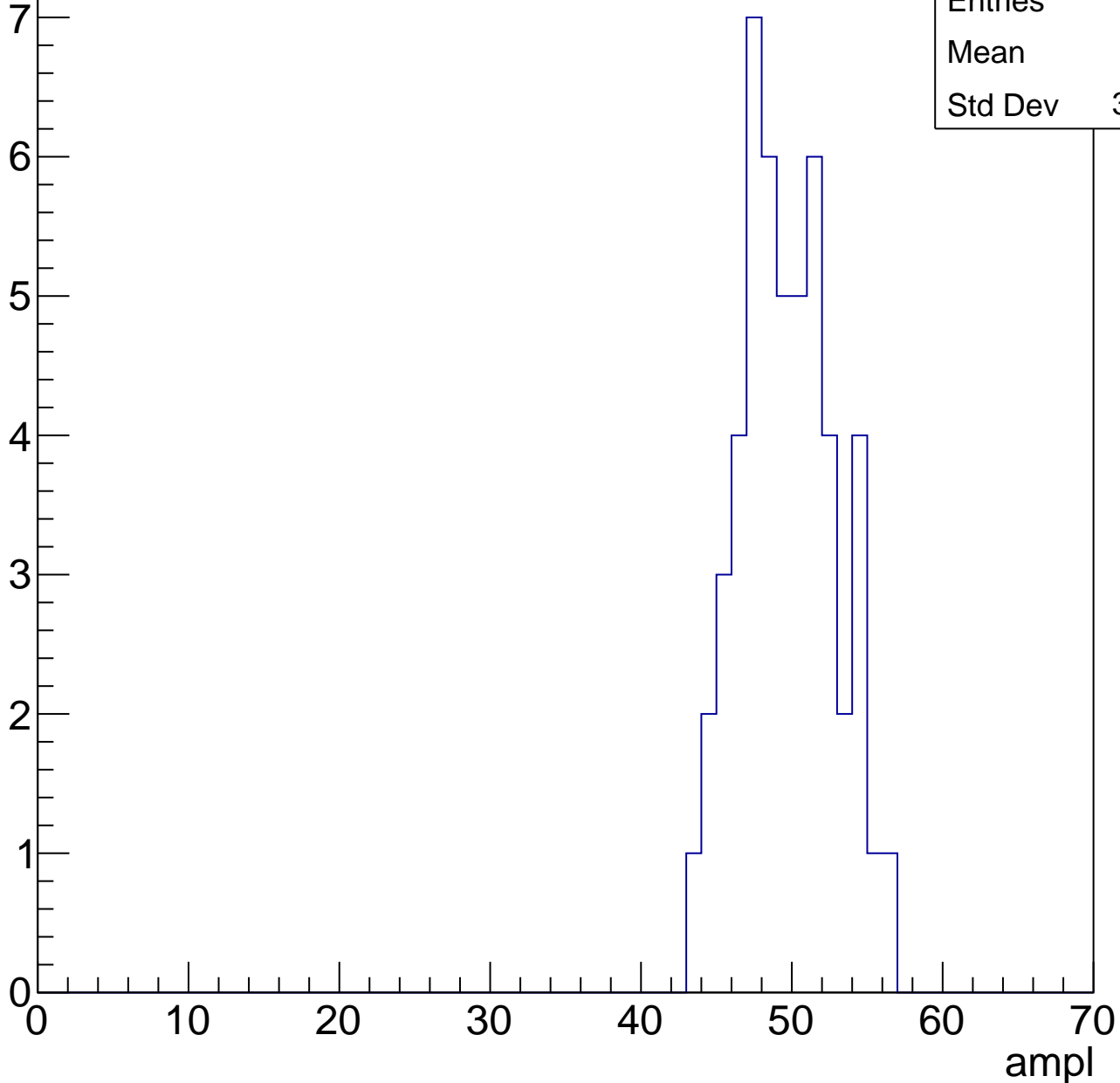


# B1L103S, U16-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	49.2
Std Dev	3.081



# B1L103S, U16-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

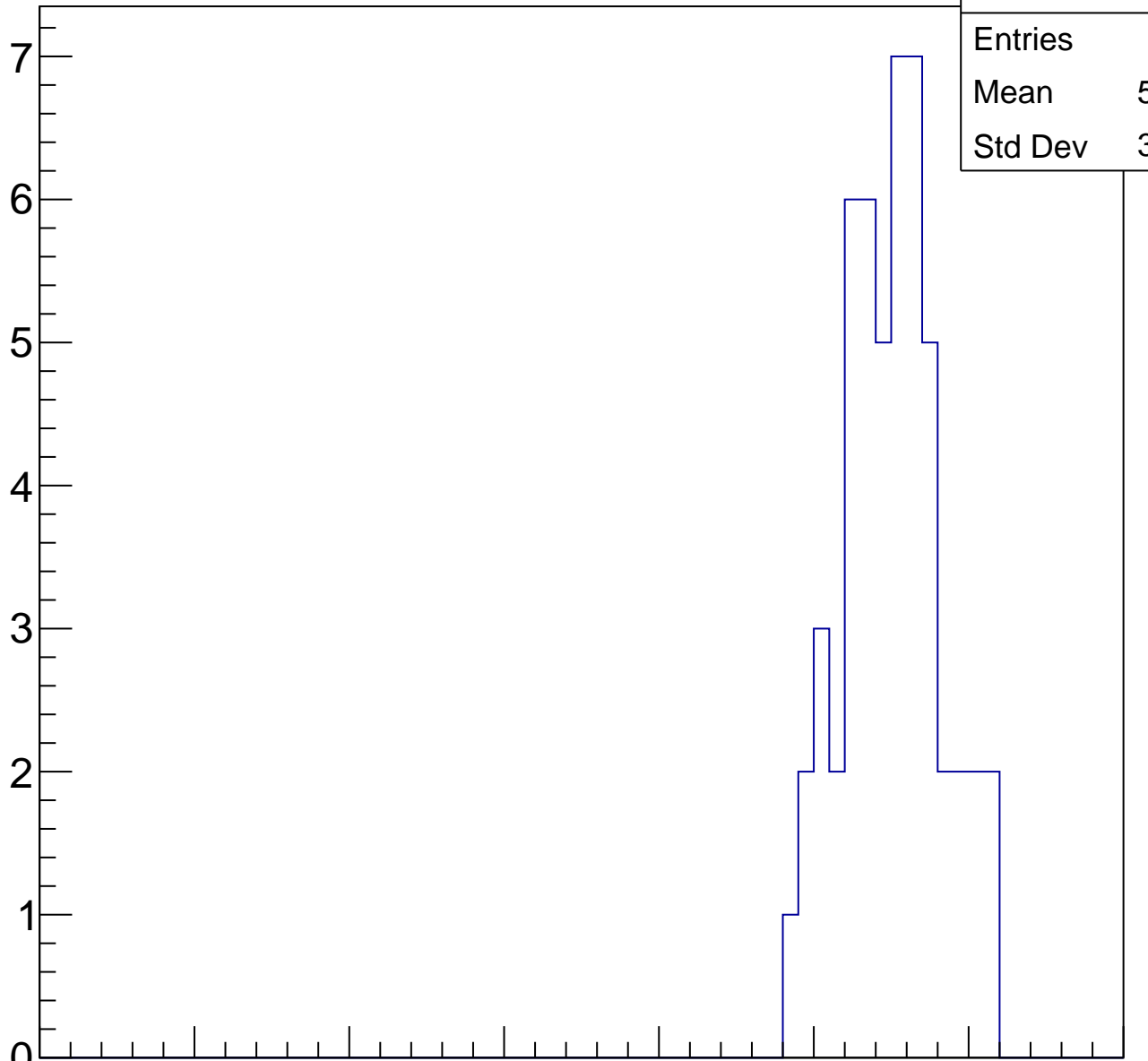
Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	52
Mean	54.54
Std Dev	3.098

ampl

0 10 20 30 40 50 60 70

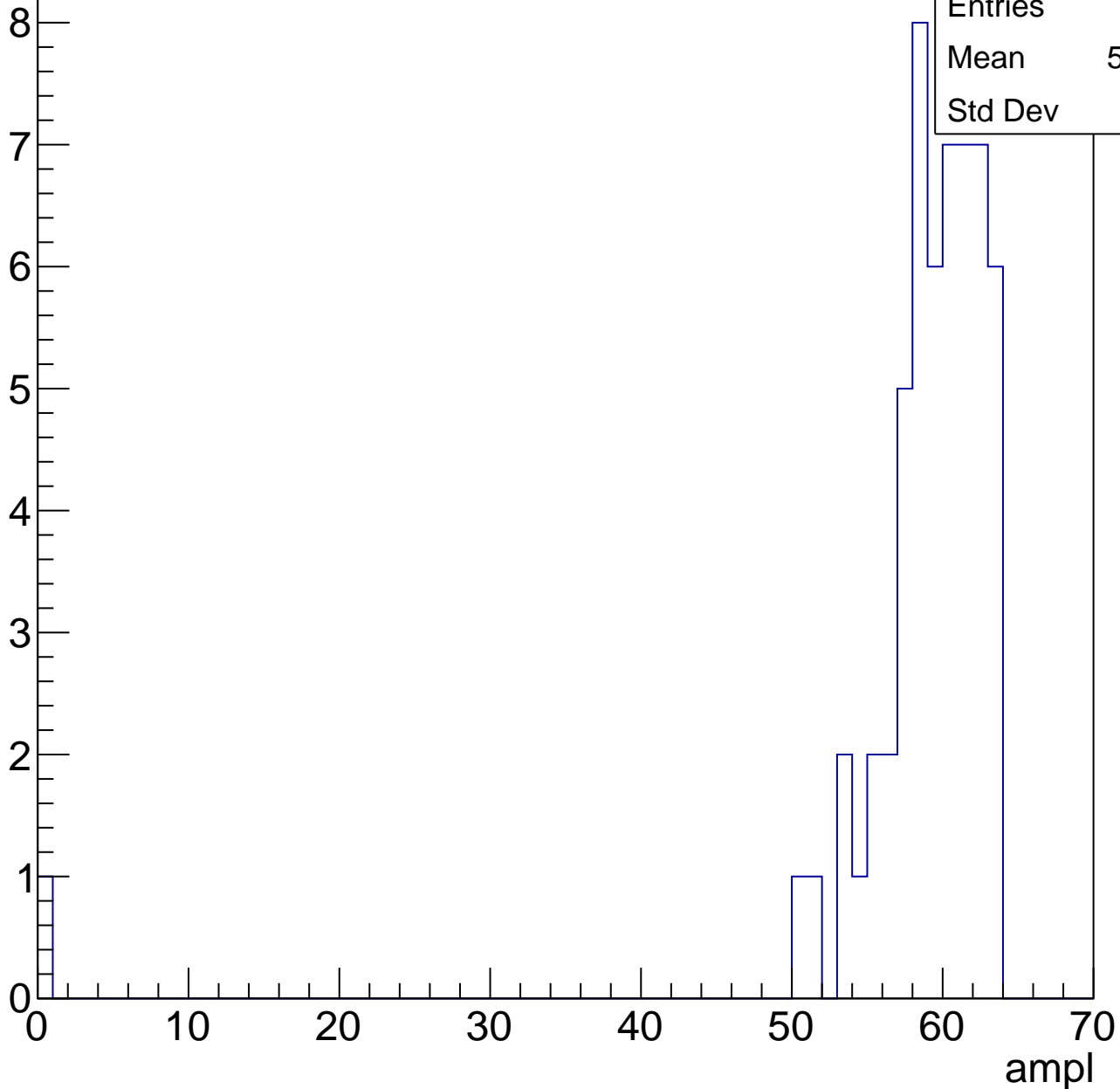


# B1L103S, U16-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	57.95
Std Dev	8.38



# B1L103S, U16-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

3

2.5

2

1.5

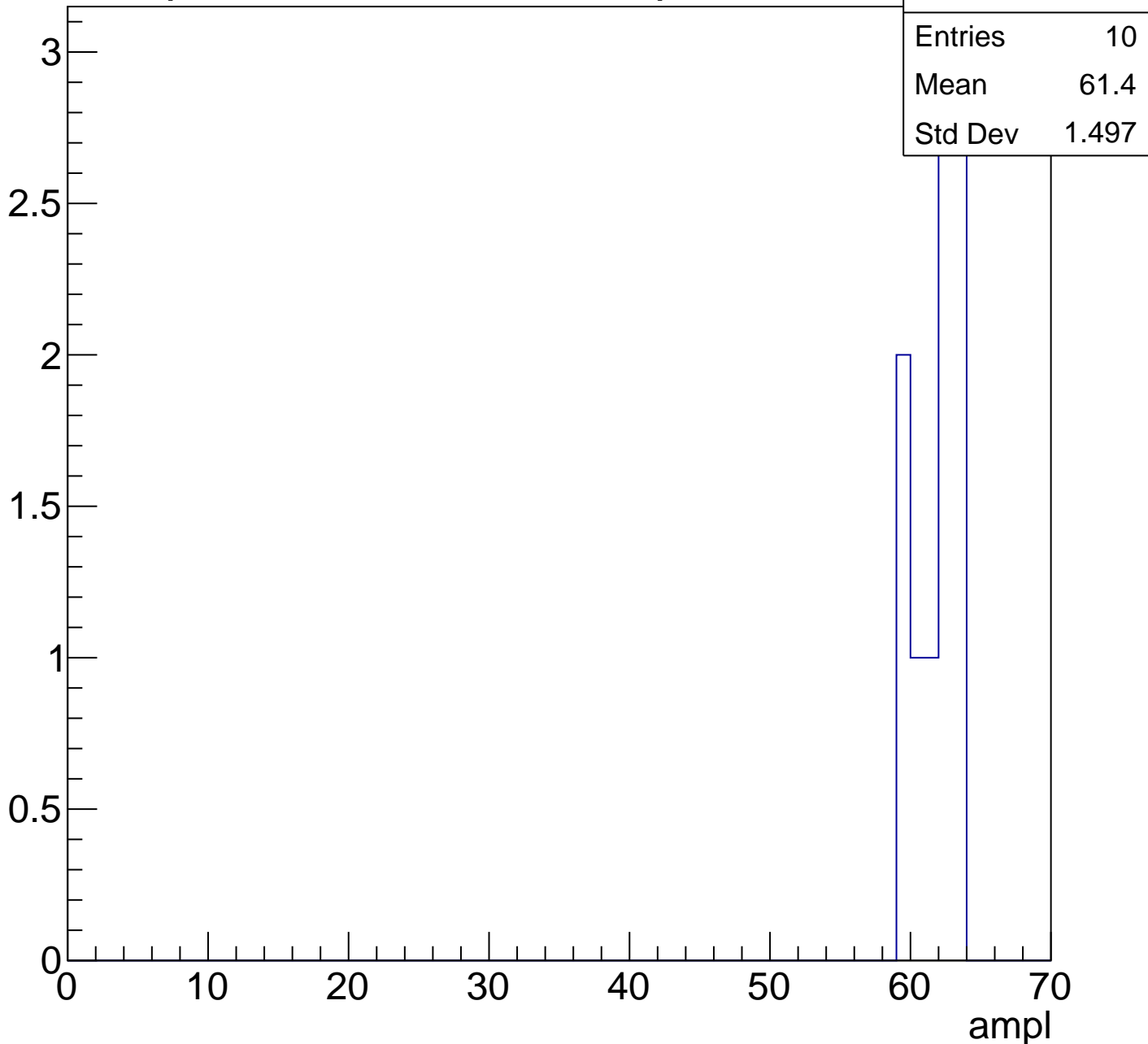
1

0.5

0

Entries	10
Mean	61.4
Std Dev	1.497

ampl





# B1L103S, U16-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	63
Std Dev	0

# B1L103S, U16-ch45, adc0

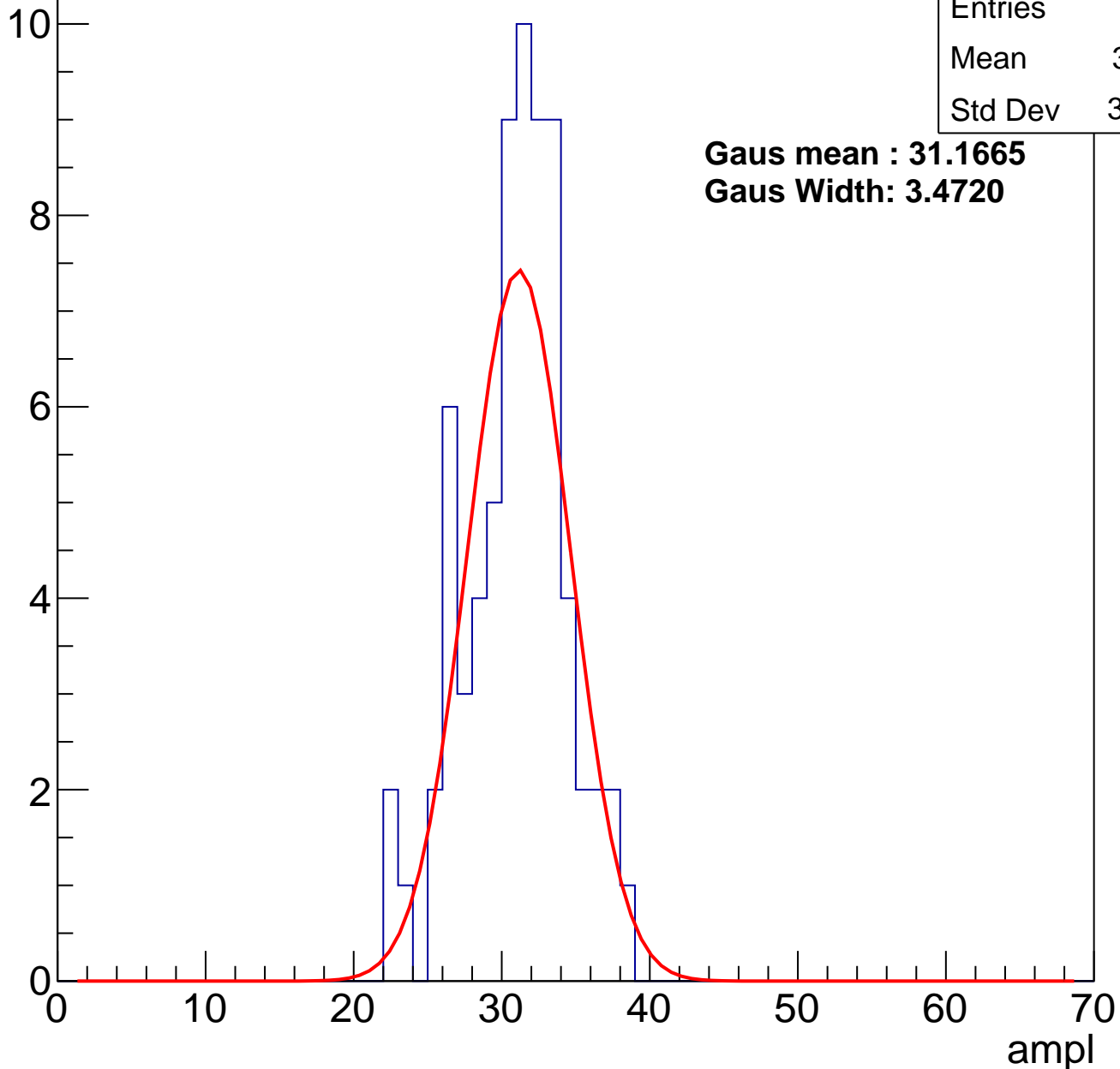
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	71
Mean	30.51
Std Dev	3.414

**Gaus mean : 31.1665**

**Gaus Width: 3.4720**

Entry



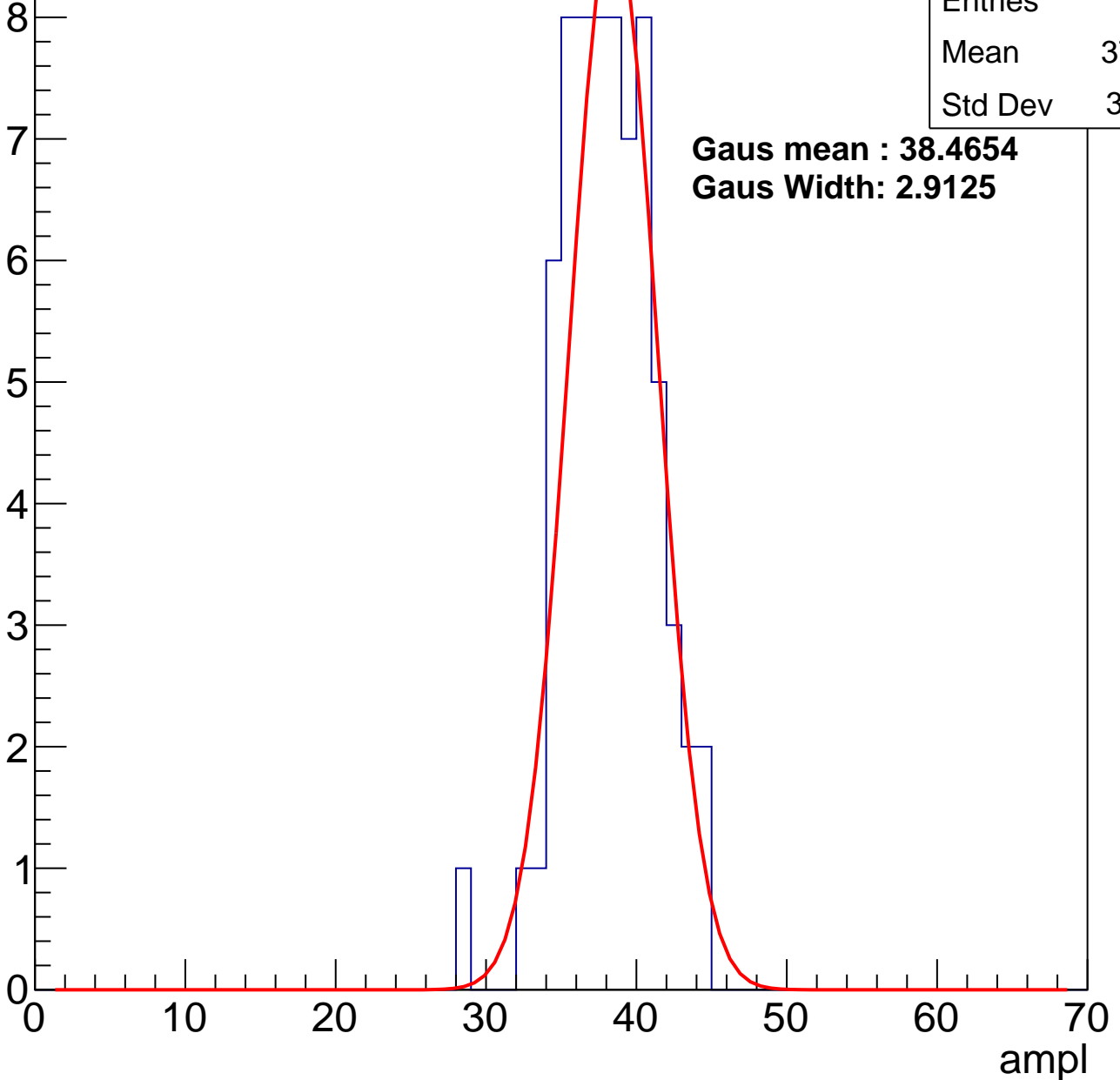
# B1L103S, U16-ch45, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	37.69
Std Dev	3.011

**Gaus mean : 38.4654**  
**Gaus Width: 2.9125**



# B1L103S, U16-ch45, adc2

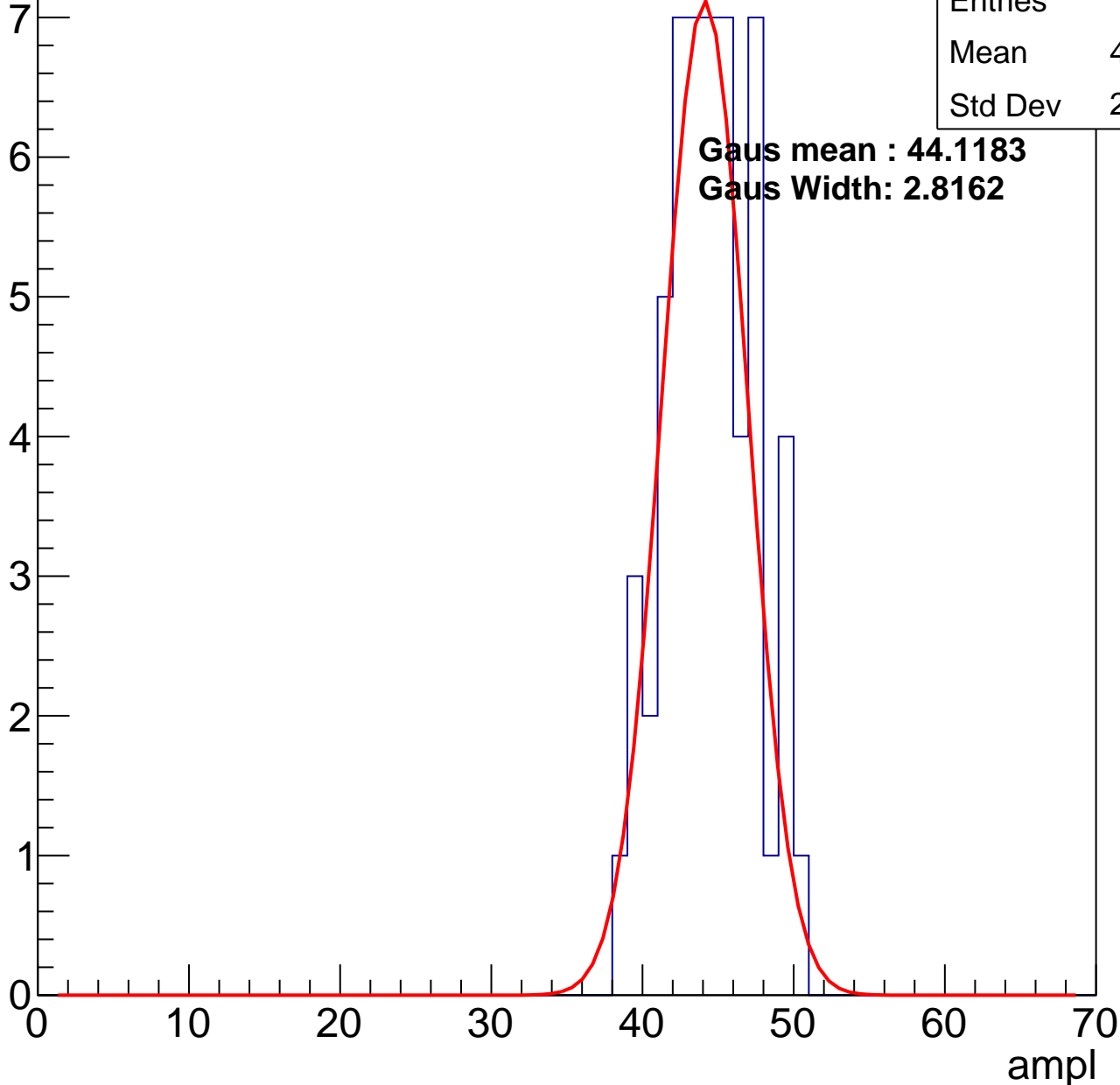
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	44.02
Std Dev	2.869

**Gaus mean : 44.1183**

**Gaus Width: 2.8162**

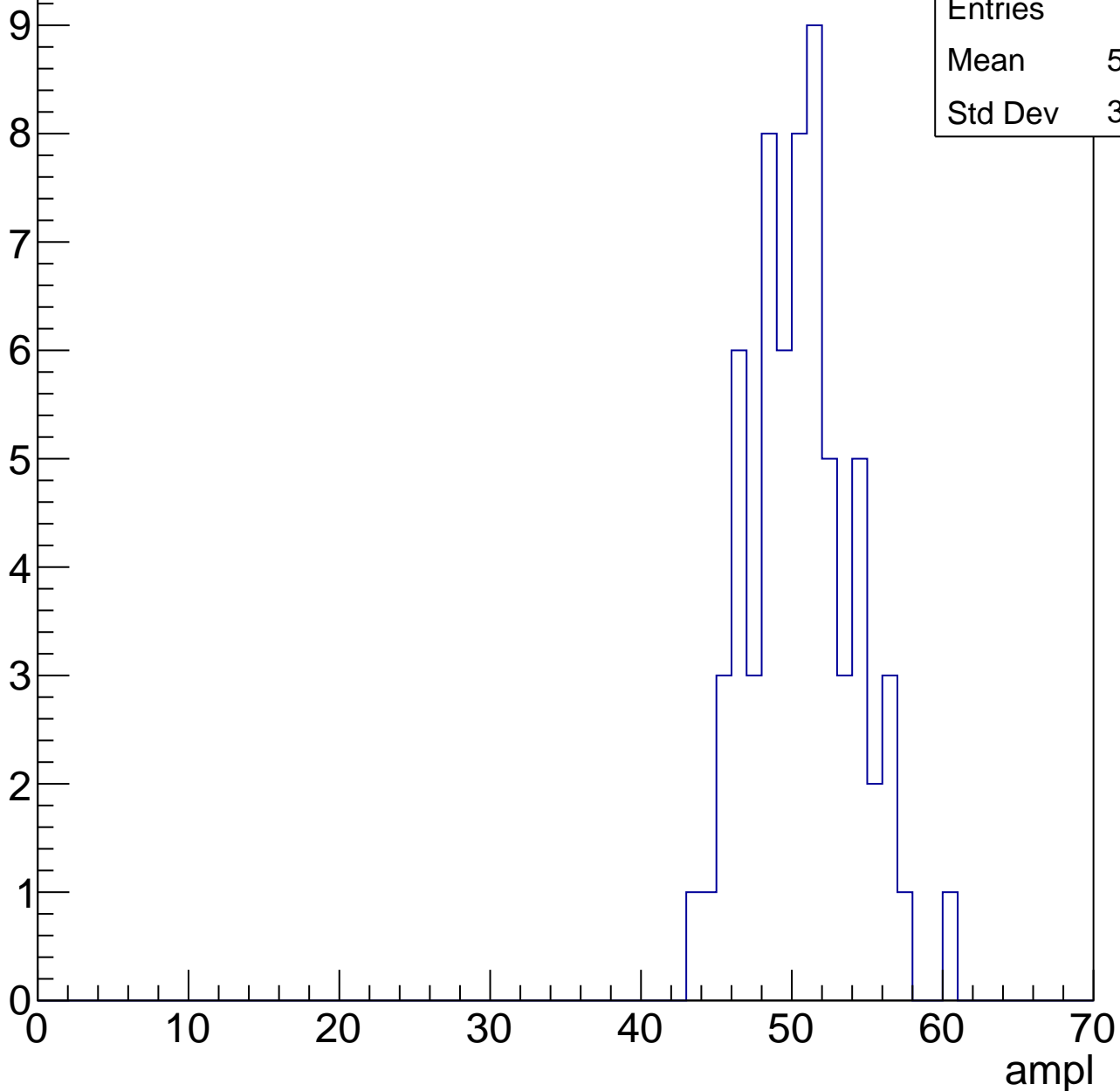


# B1L103S, U16-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	50.15
Std Dev	3.425

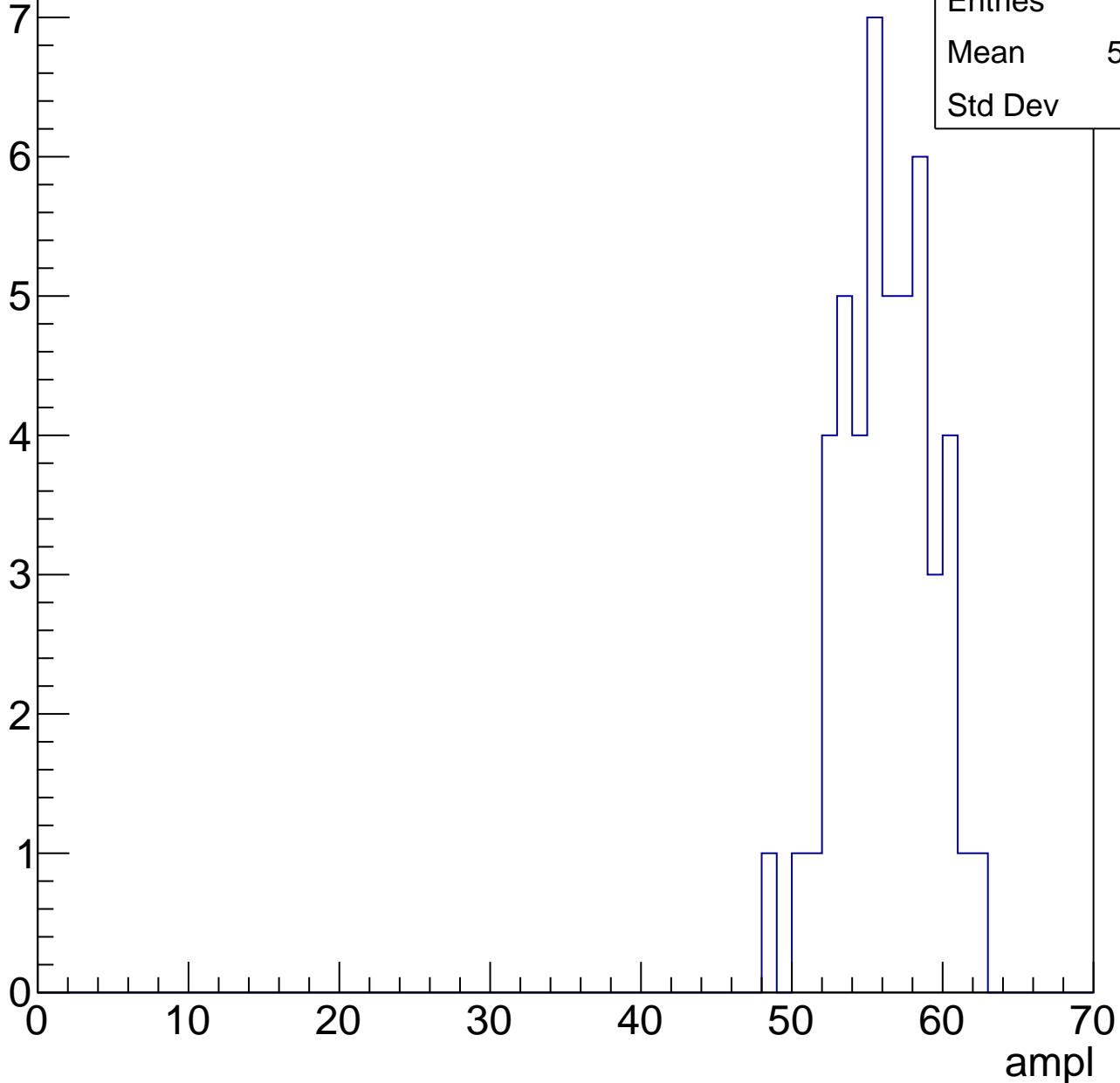


# B1L103S, U16-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	55.75
Std Dev	3.01

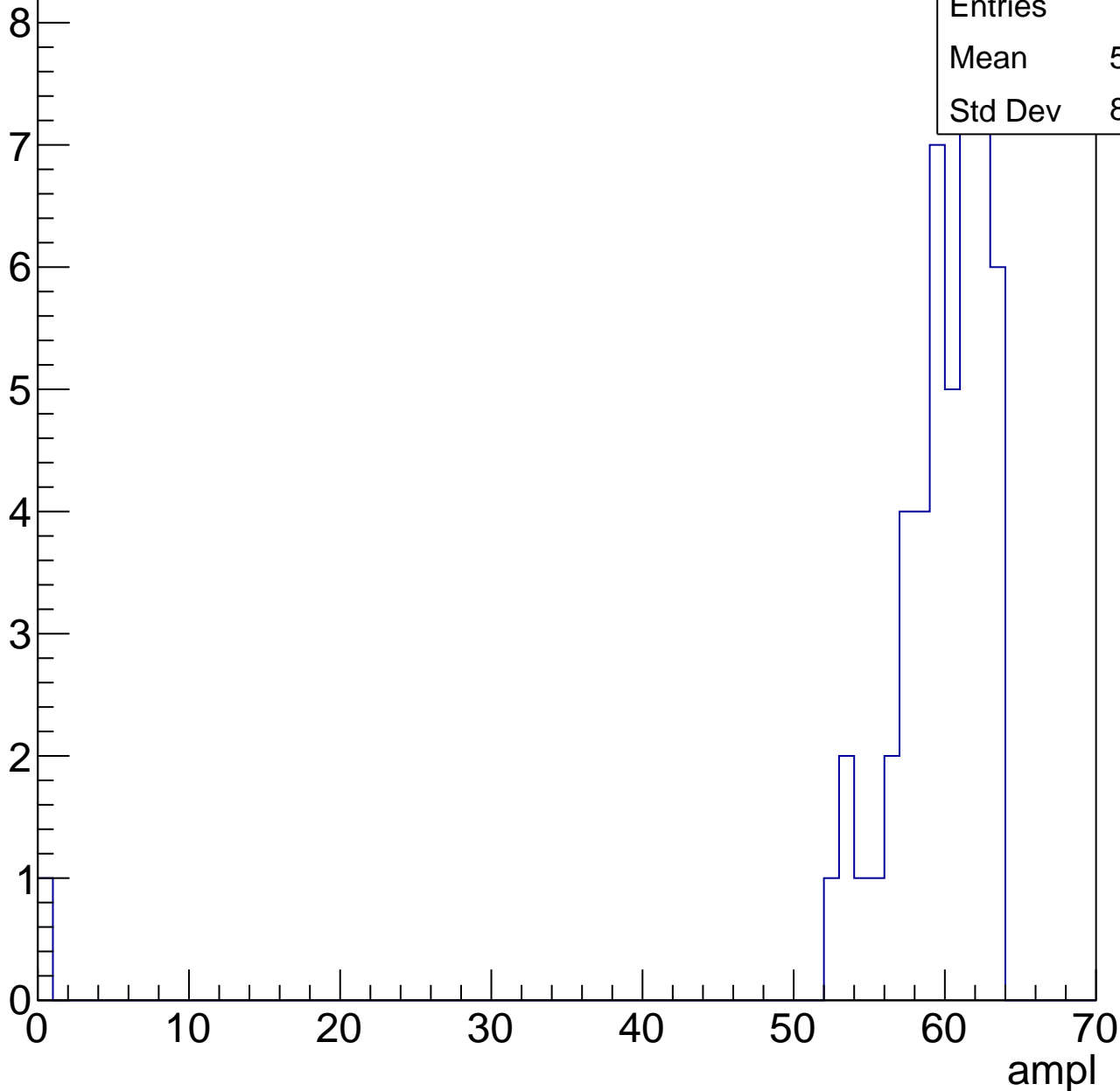


# B1L103S, U16-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	58.28
Std Dev	8.786



# B1L103S, U16-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch46, adc0

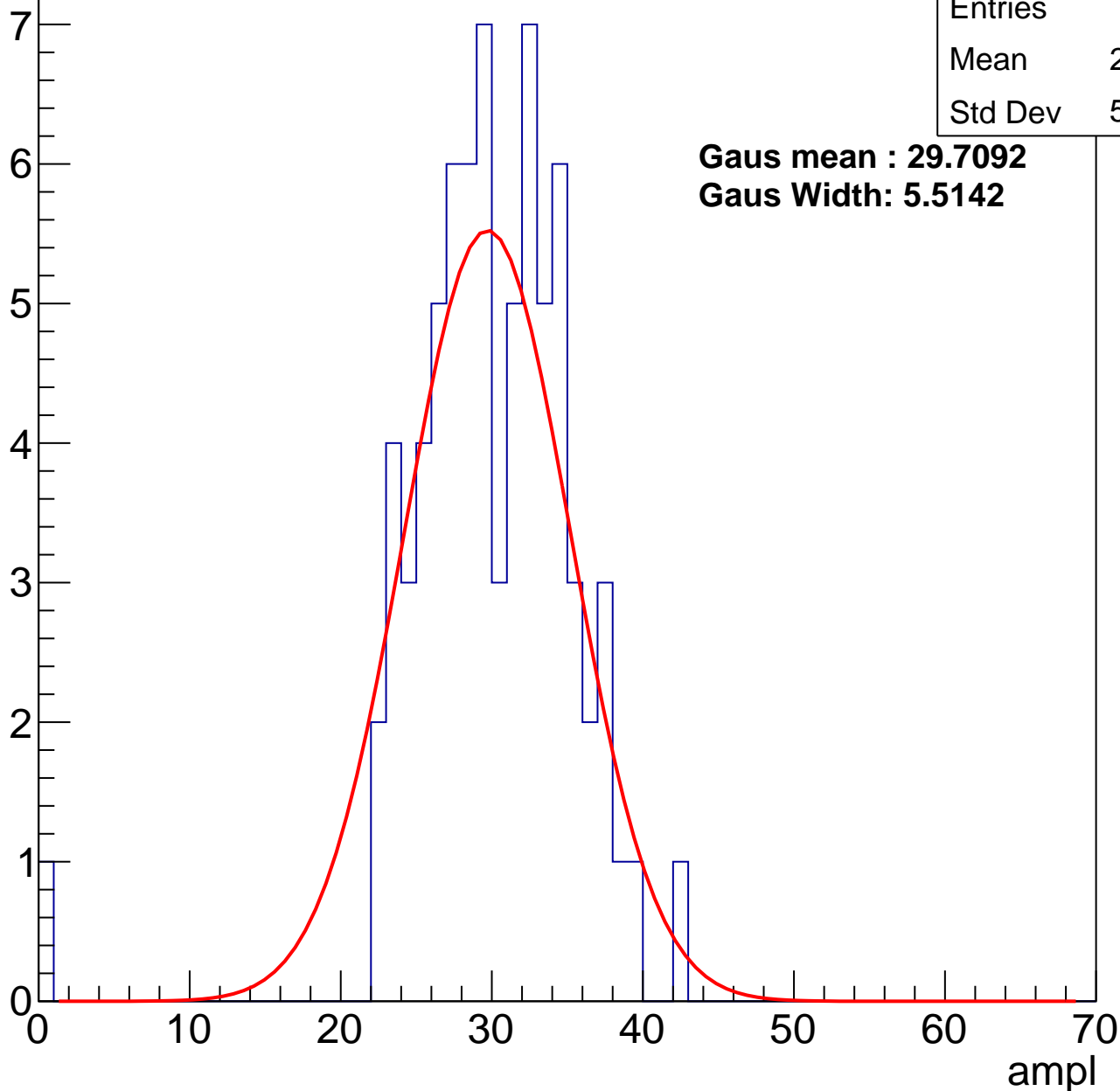
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	29.55
Std Dev	5.584

**Gaus mean : 29.7092**

**Gaus Width: 5.5142**



# B1L103S, U16-ch46, adc1

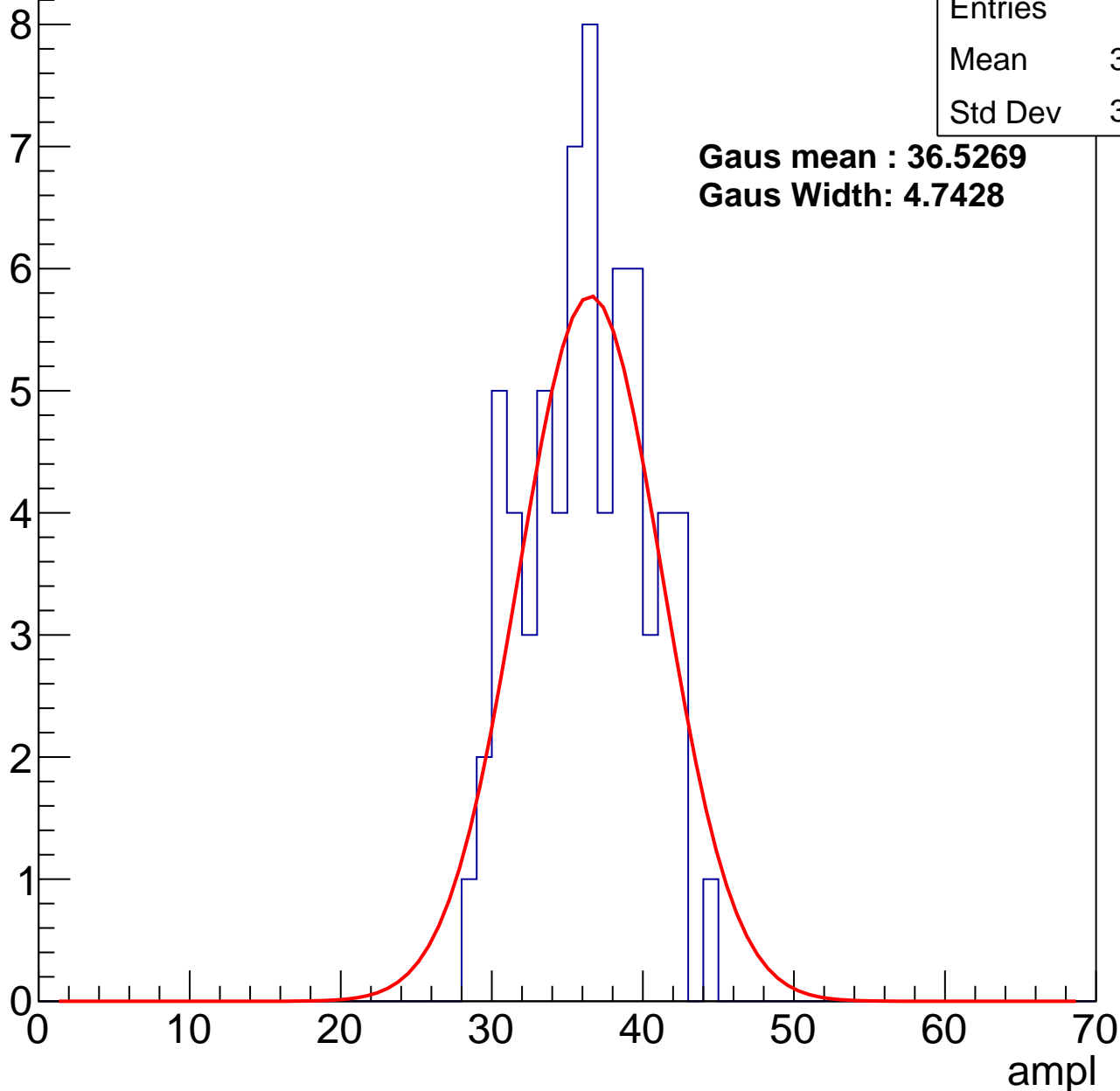
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	35.76
Std Dev	3.848

**Gaus mean : 36.5269**

**Gaus Width: 4.7428**



# B1L103S, U16-ch46, adc2

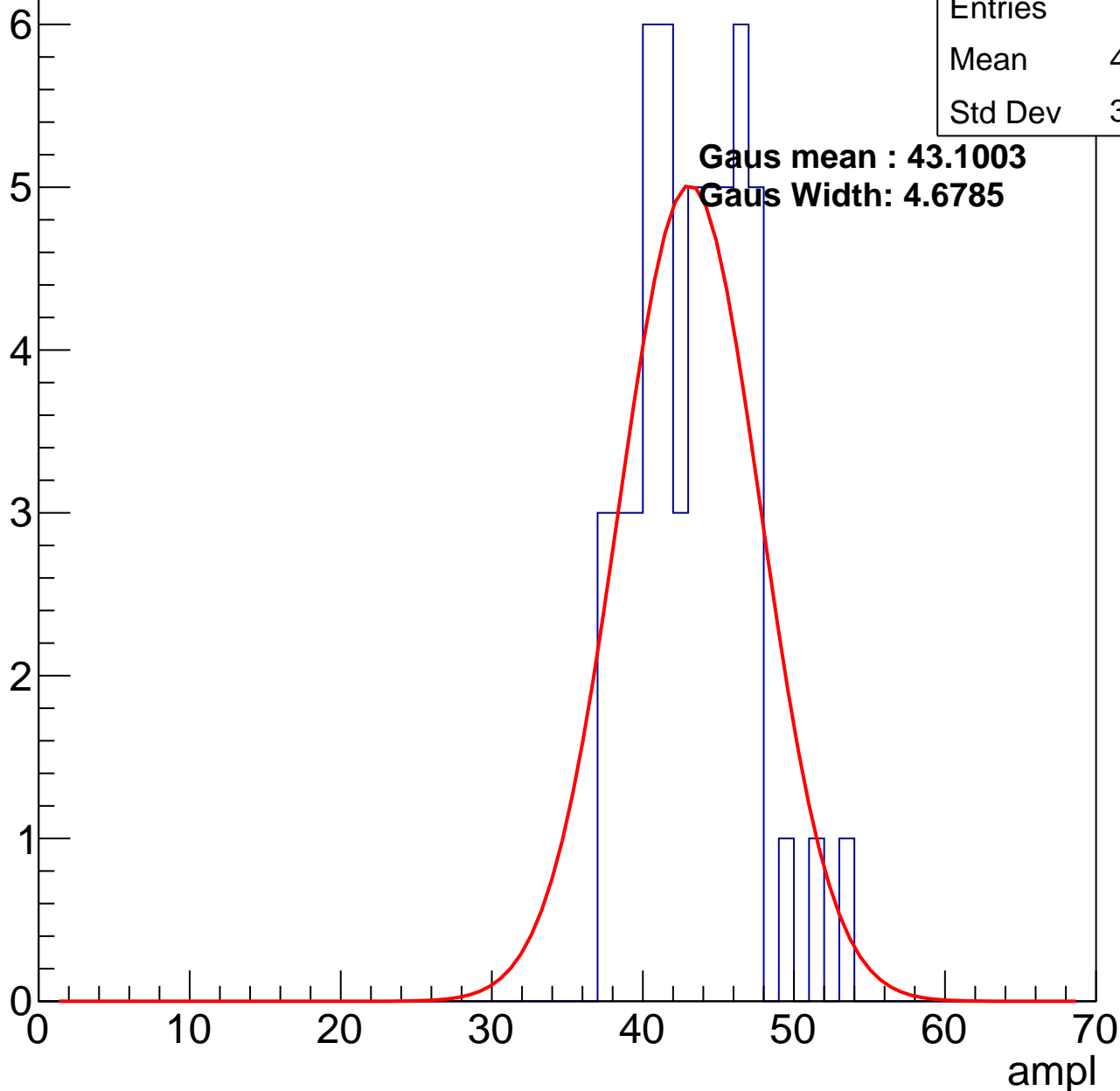
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	42.98
Std Dev	3.558

**Gaus mean : 43.1003**

**Gaus Width: 4.6785**

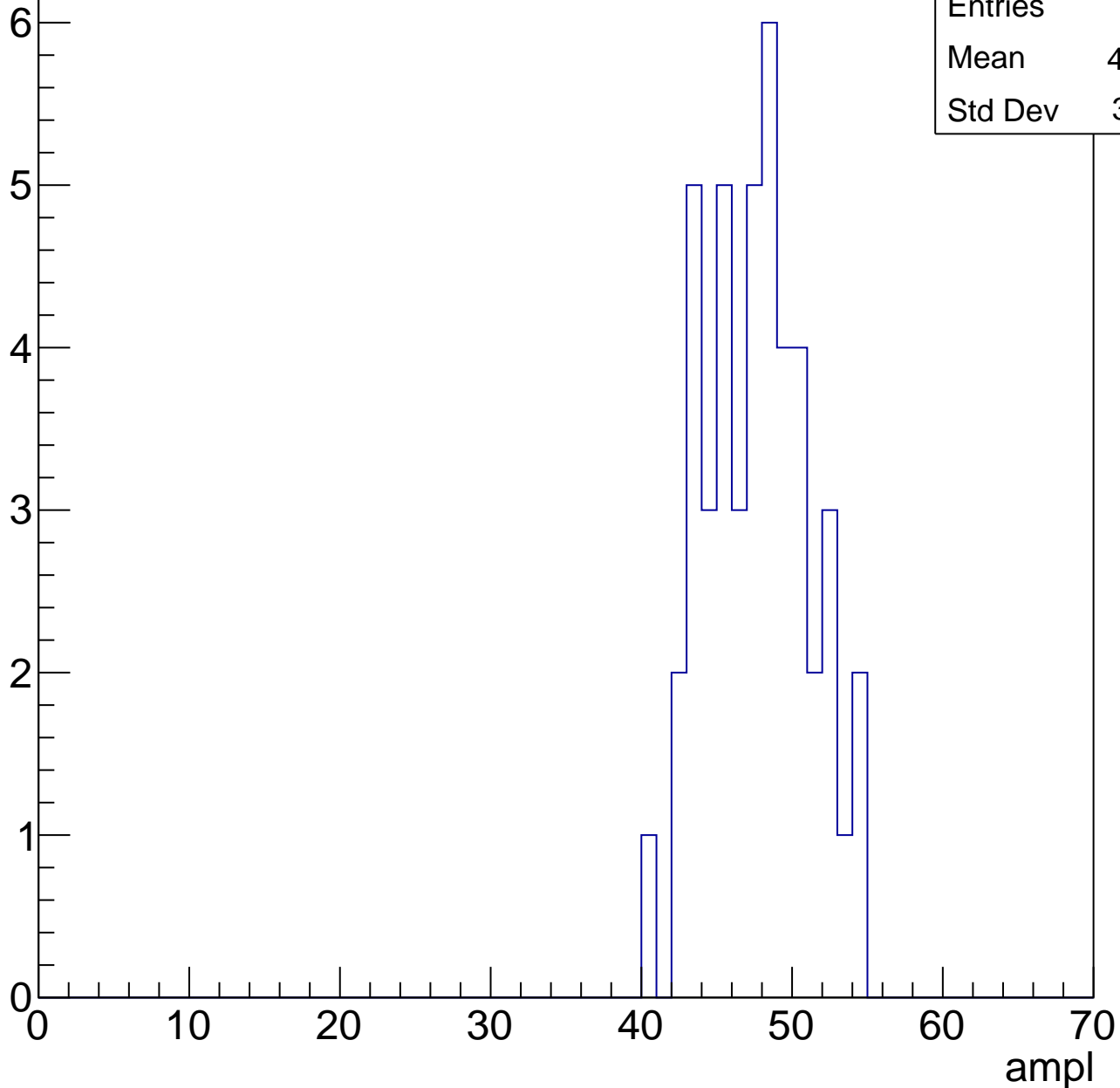


# B1L103S, U16-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	47.22
Std Dev	3.381

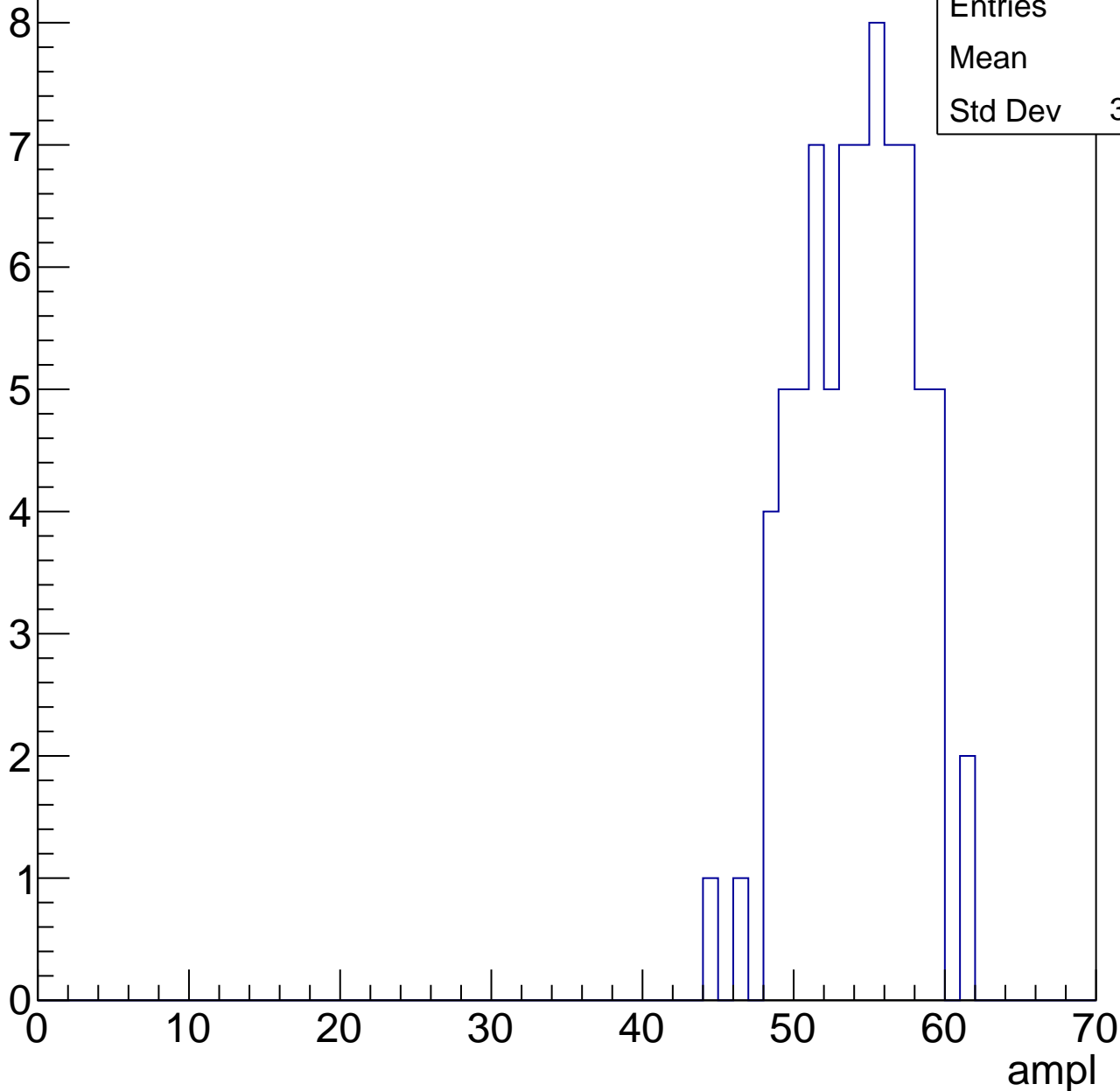


# B1L103S, U16-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	53.7
Std Dev	3.624

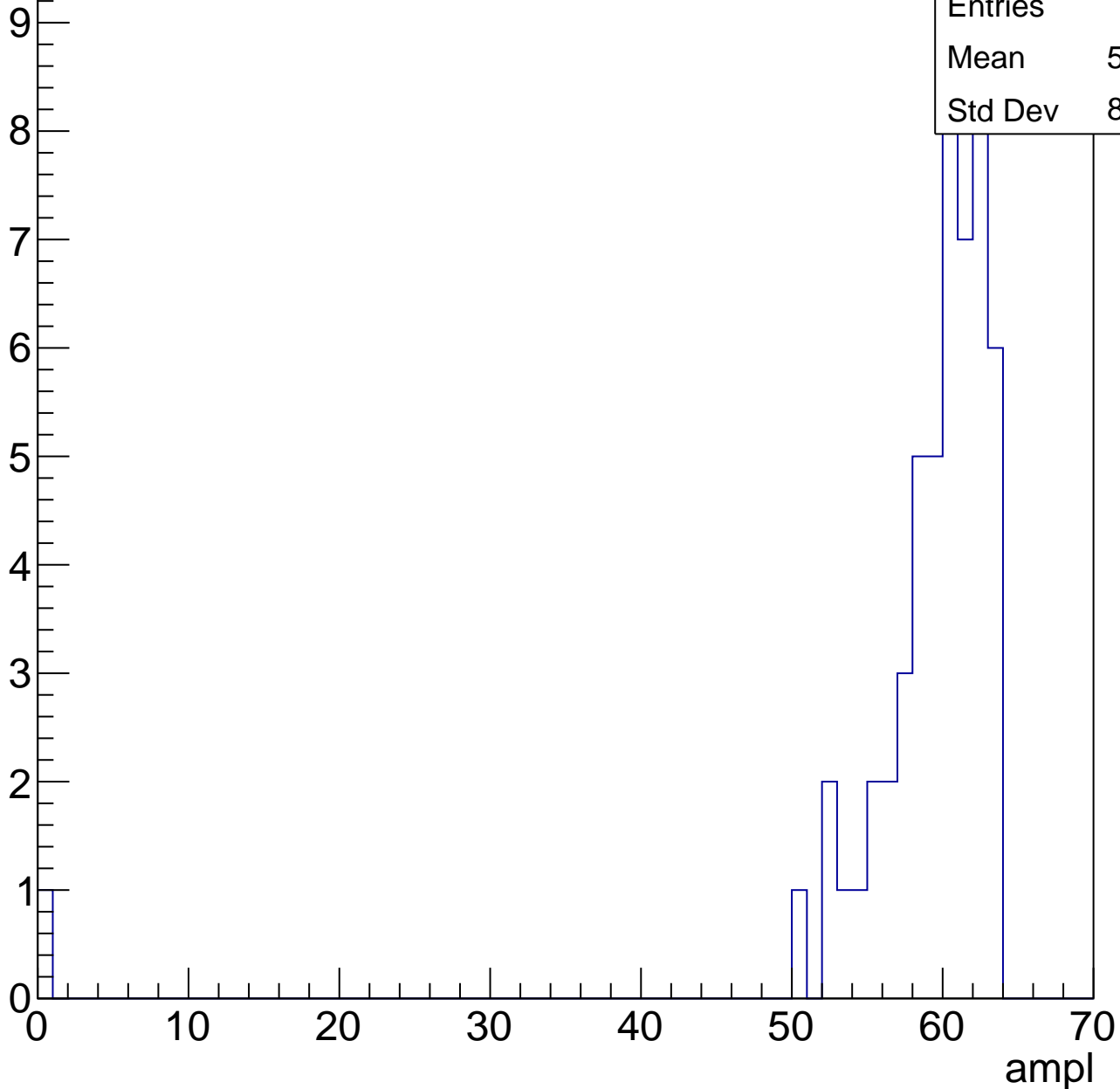


# B1L103S, U16-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

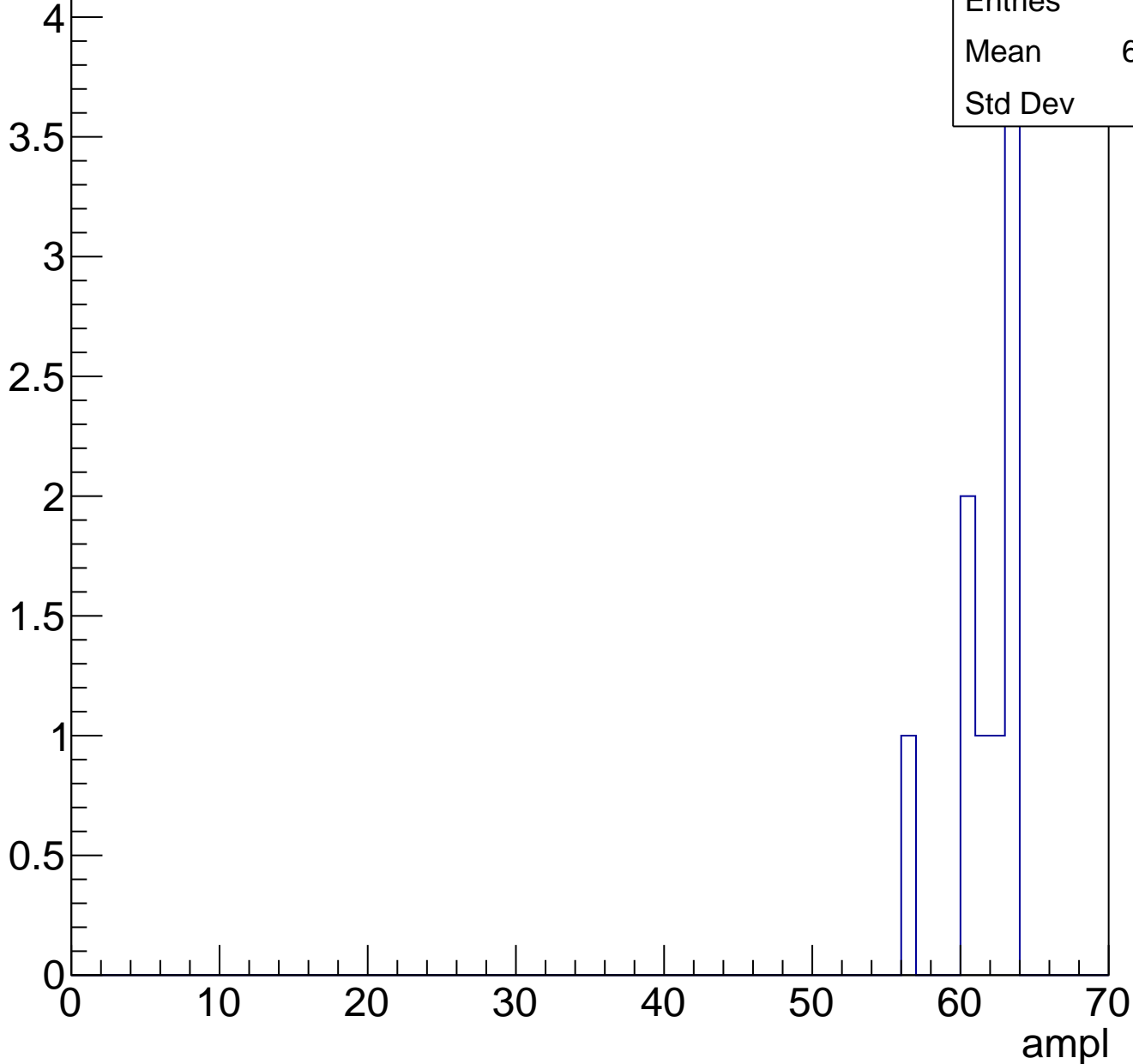
Entries	53
Mean	58.15
Std Dev	8.647



# B1L103S, U16-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch47, adc0

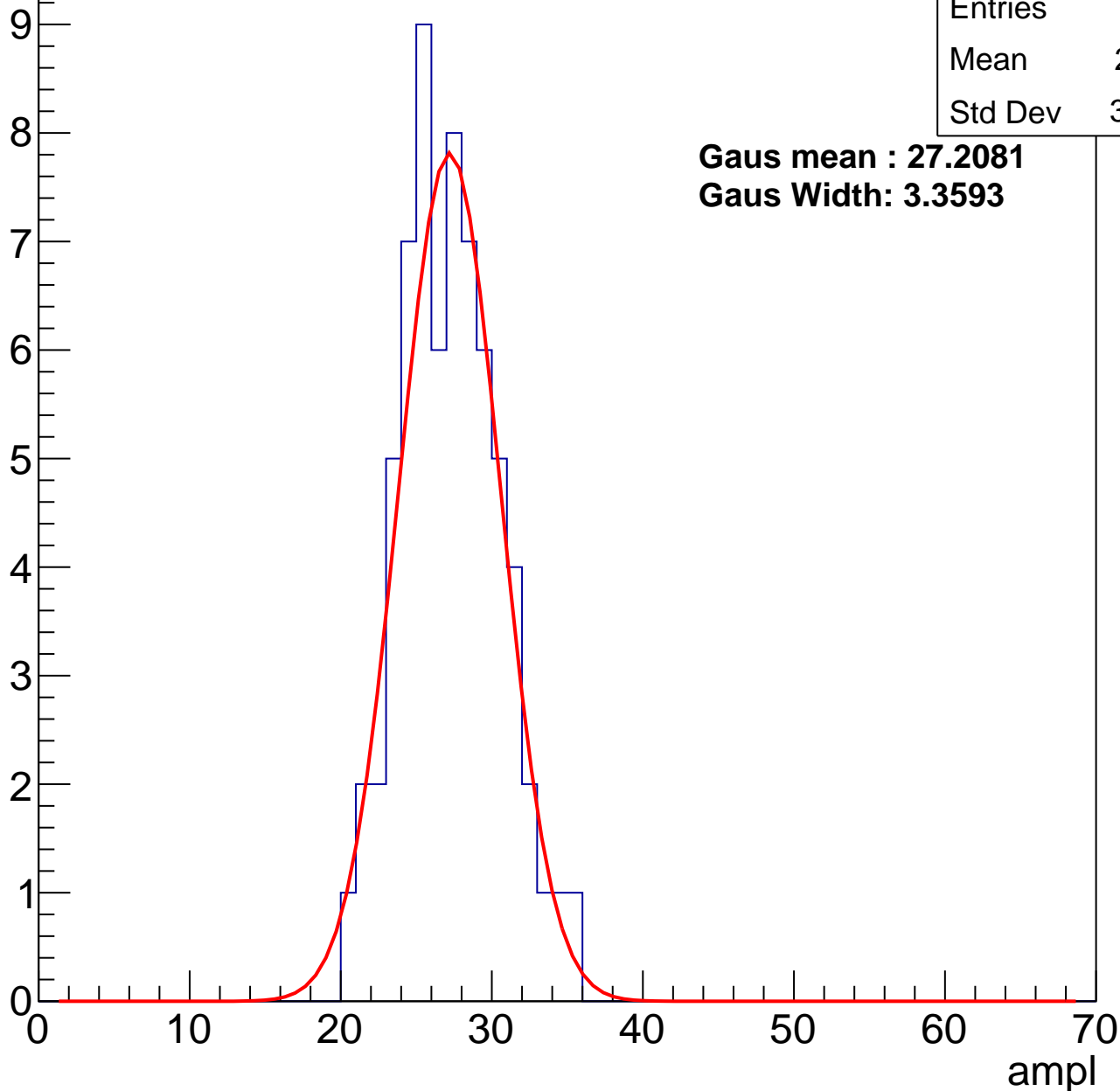
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	26.81
Std Dev	3.215

**Gaus mean : 27.2081**

**Gaus Width: 3.3593**



# B1L103S, U16-ch47, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	92
Mean	34.54
Std Dev	3.658

**Gaus mean : 34.8077**

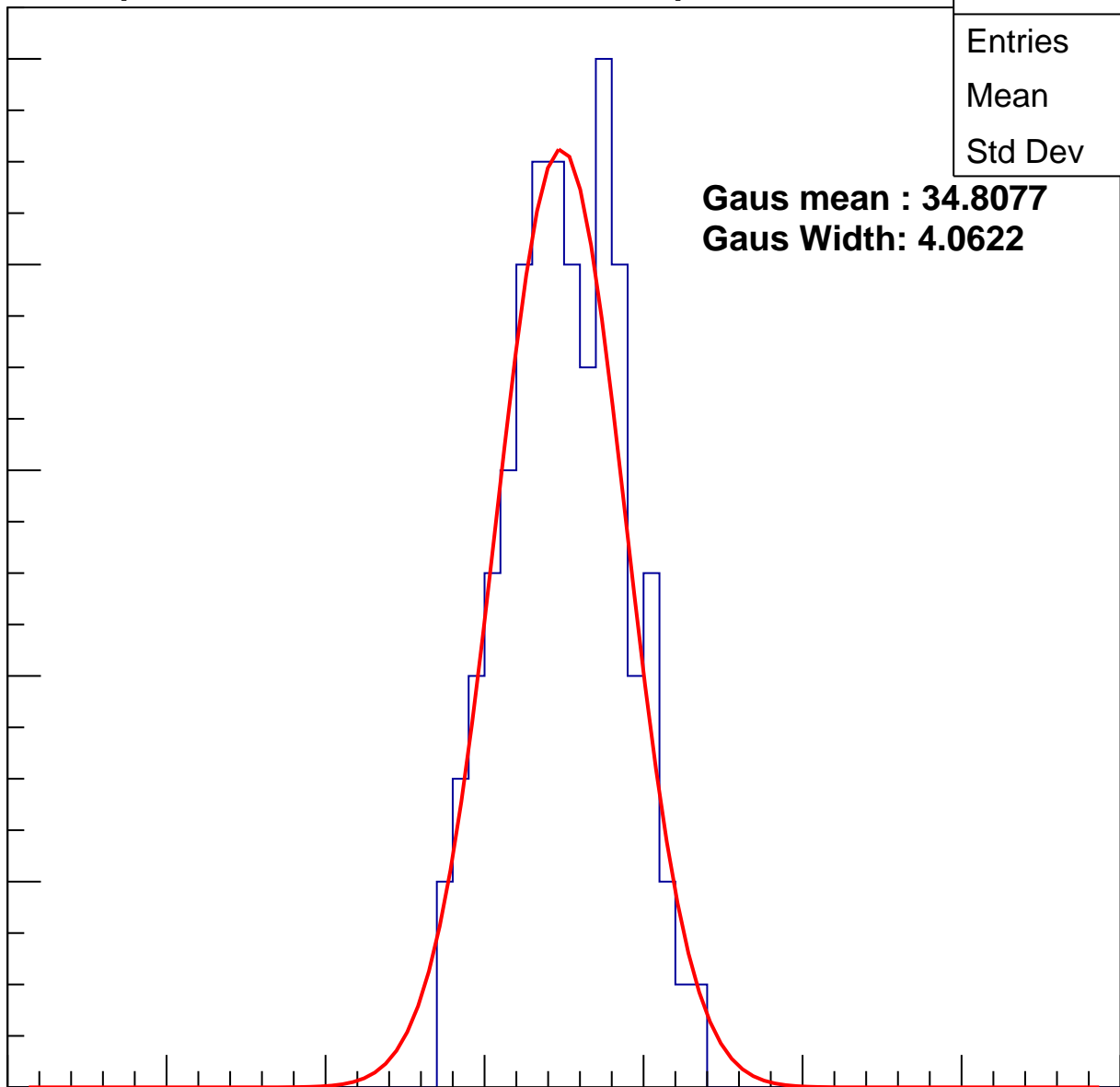
**Gaus Width: 4.0622**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U16-ch47, adc2

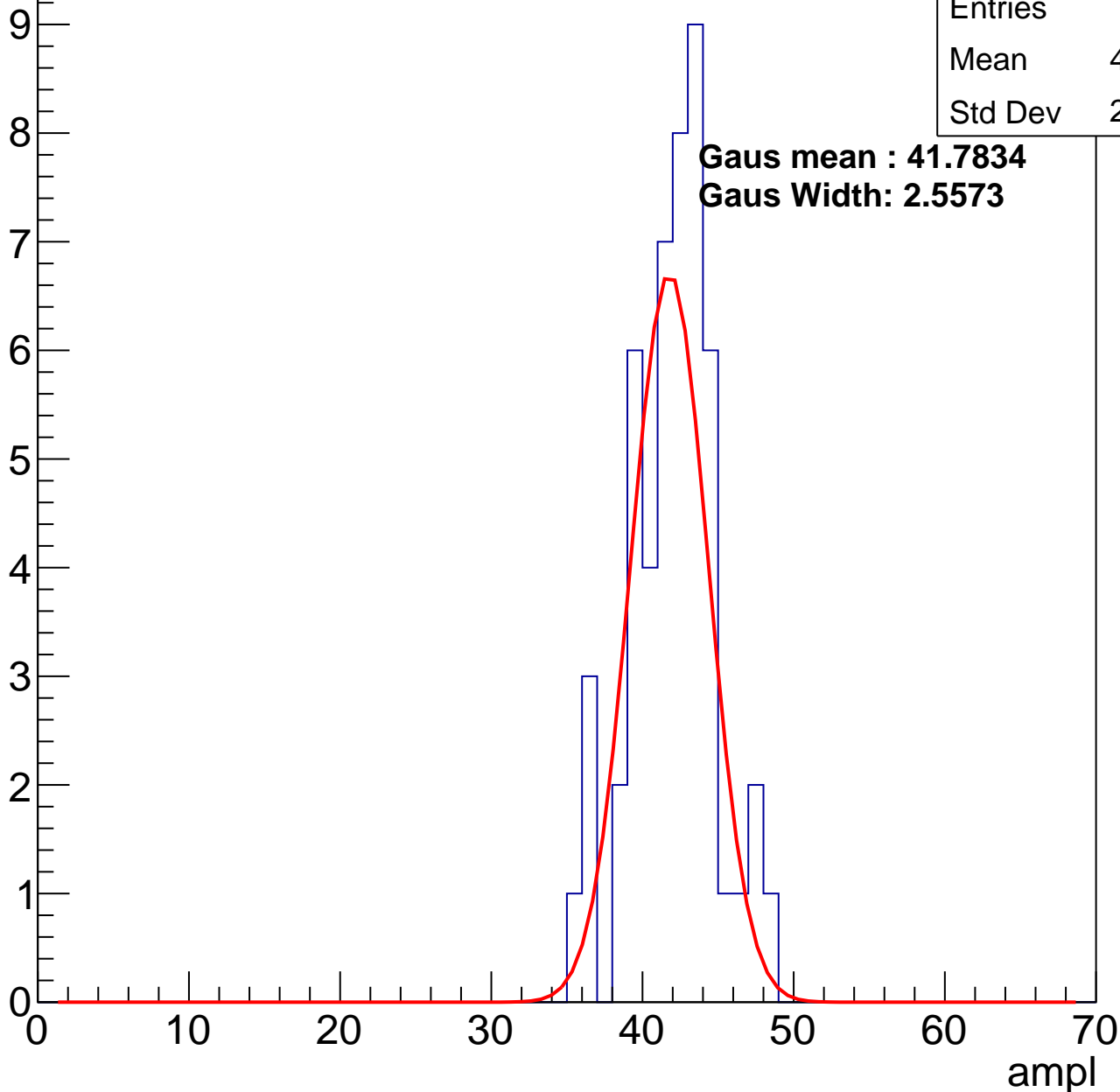
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	41.57
Std Dev	2.802

**Gaus mean : 41.7834**

**Gaus Width: 2.5573**



# B1L103S, U16-ch47, adc3

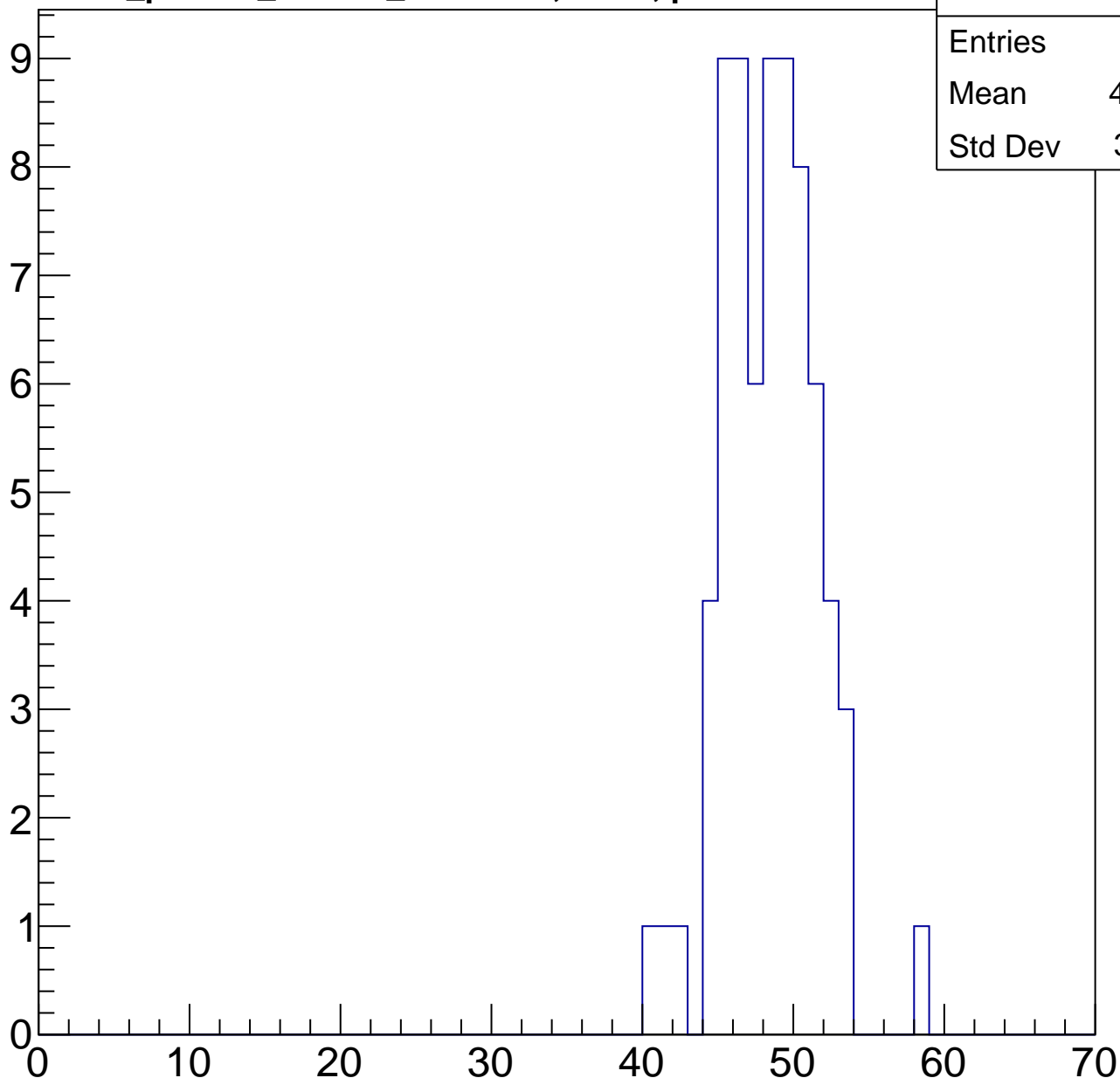
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	71
Mean	47.94
Std Dev	3.071

ampl

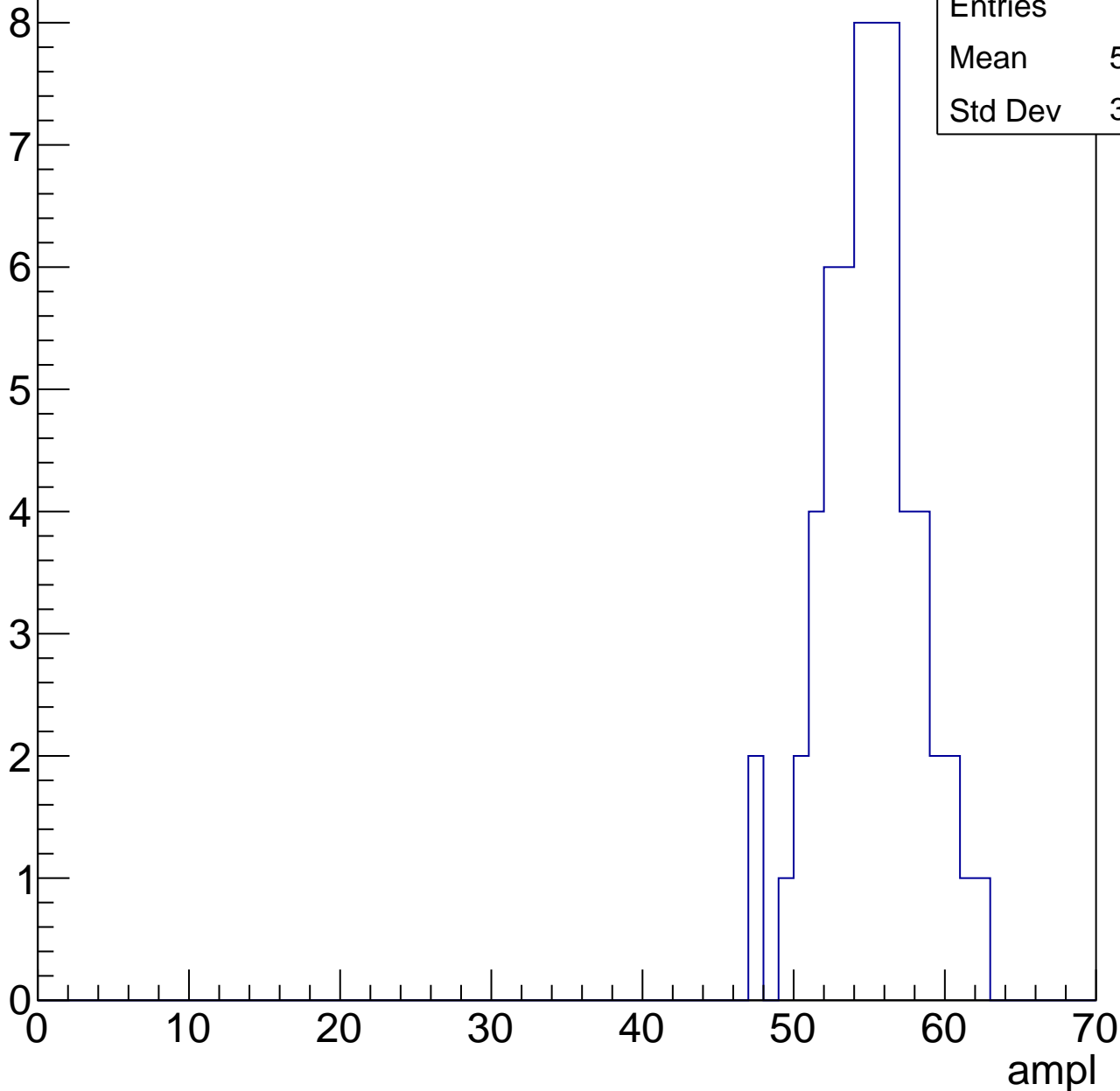


# B1L103S, U16-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

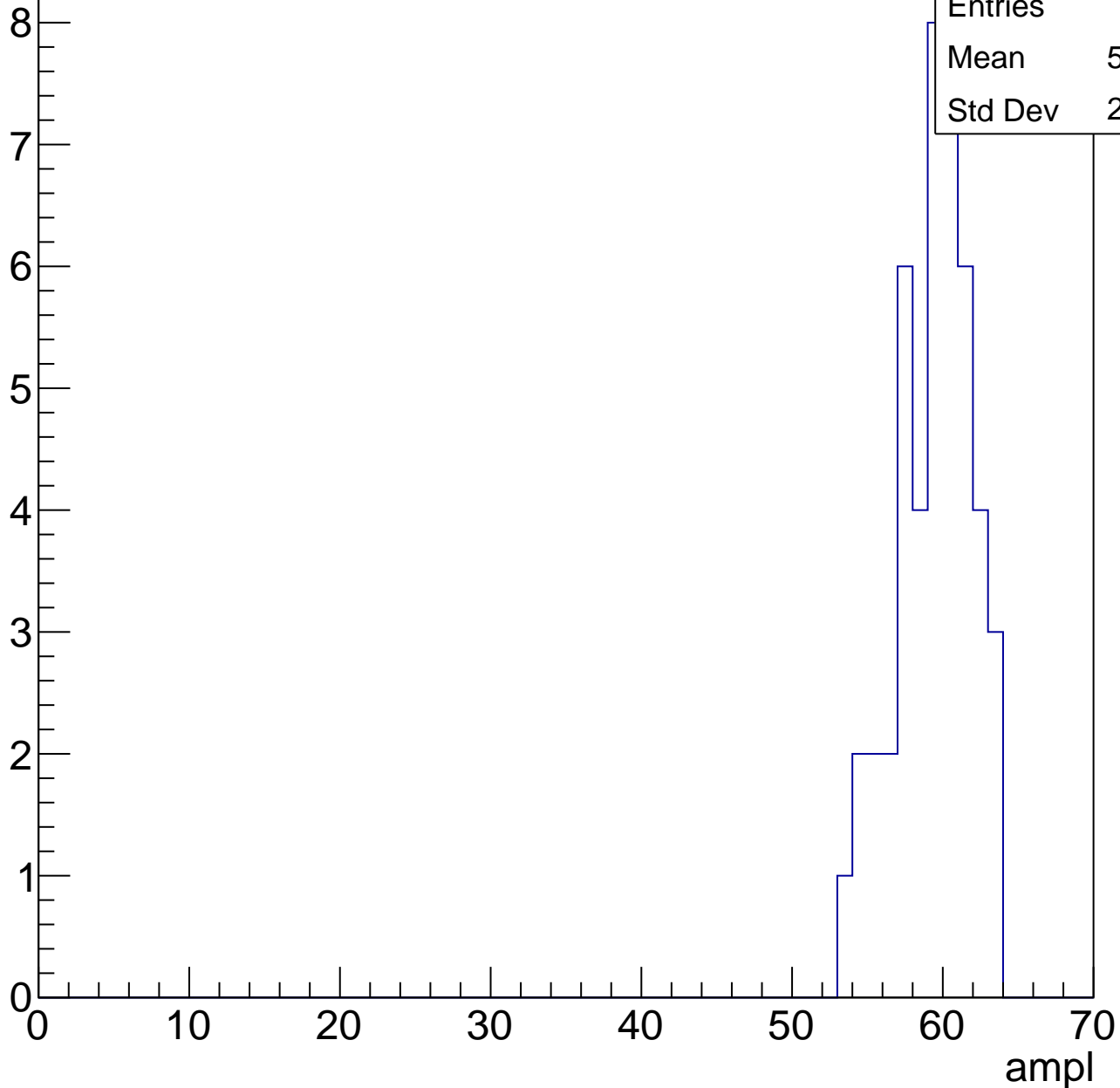
Entries	59
Mean	54.54
Std Dev	3.132



# B1L103S, U16-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

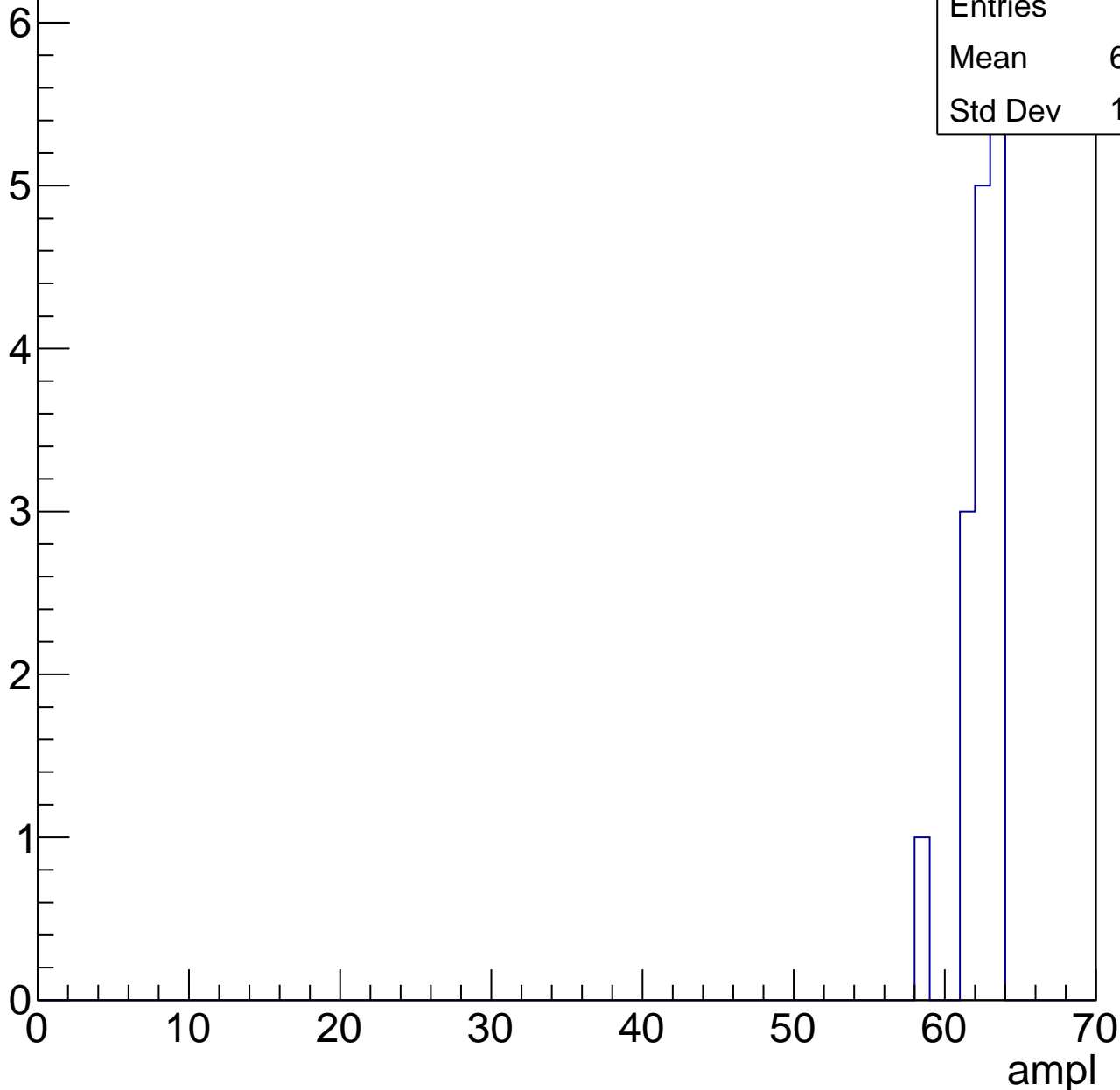


# B1L103S, U16-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	15
Mean	61.93
Std Dev	1.289

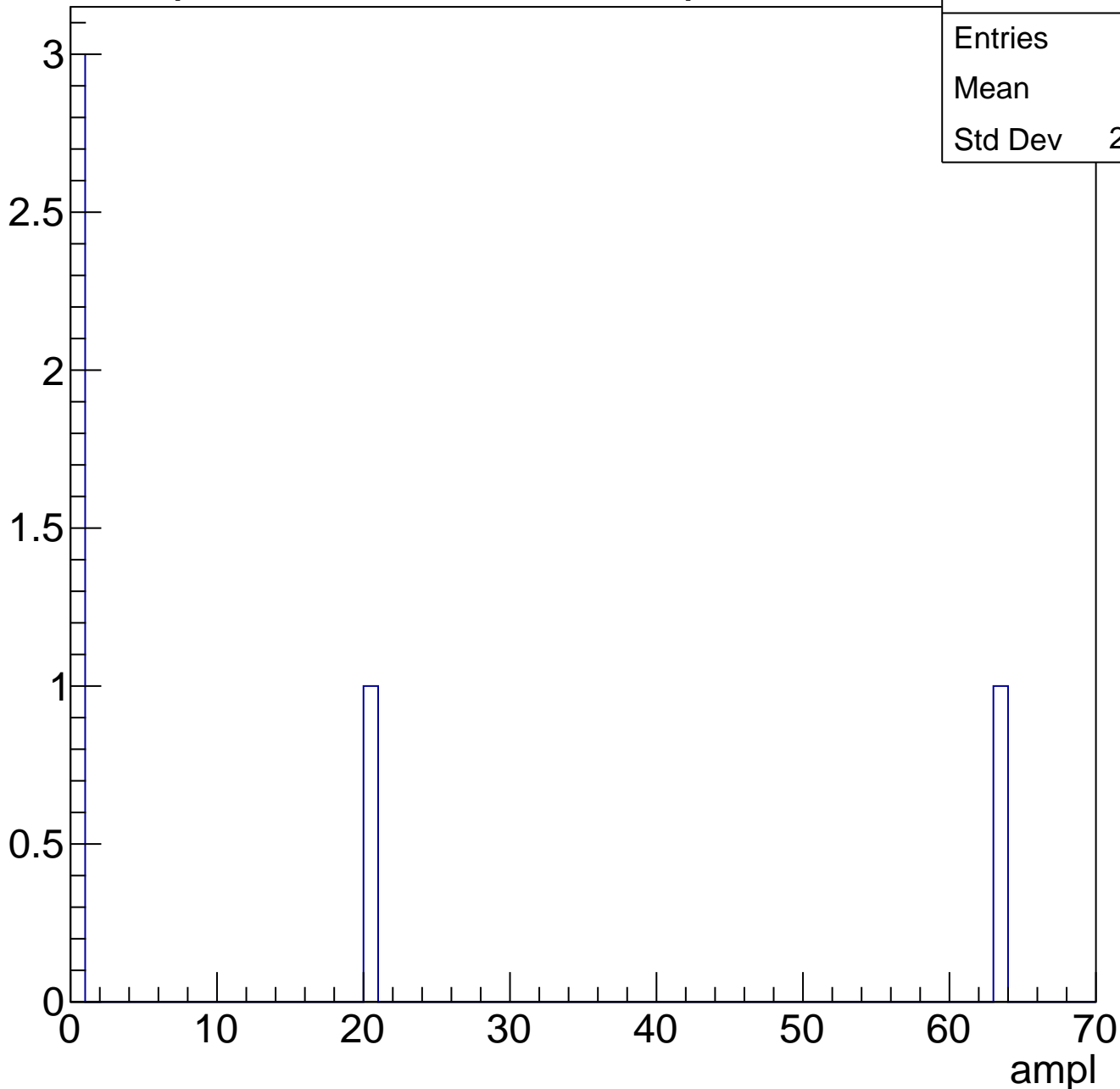




# B1L103S, U16-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	5
Mean	16.6
Std Dev	24.46

# B1L103S, U16-ch48, adc0

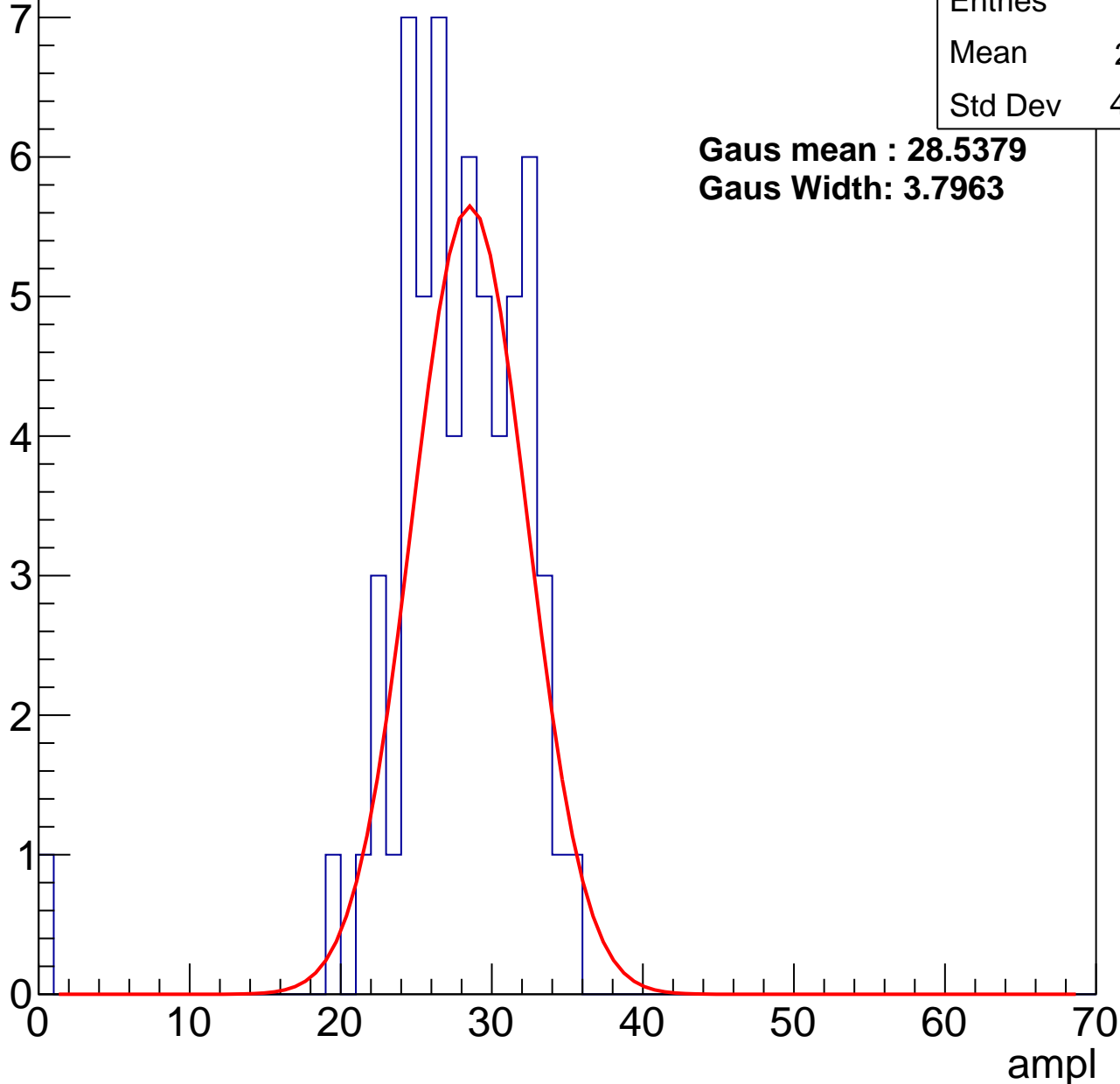
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	27.21
Std Dev	4.992

**Gaus mean : 28.5379**

**Gaus Width: 3.7963**



# B1L103S, U16-ch48, adc1

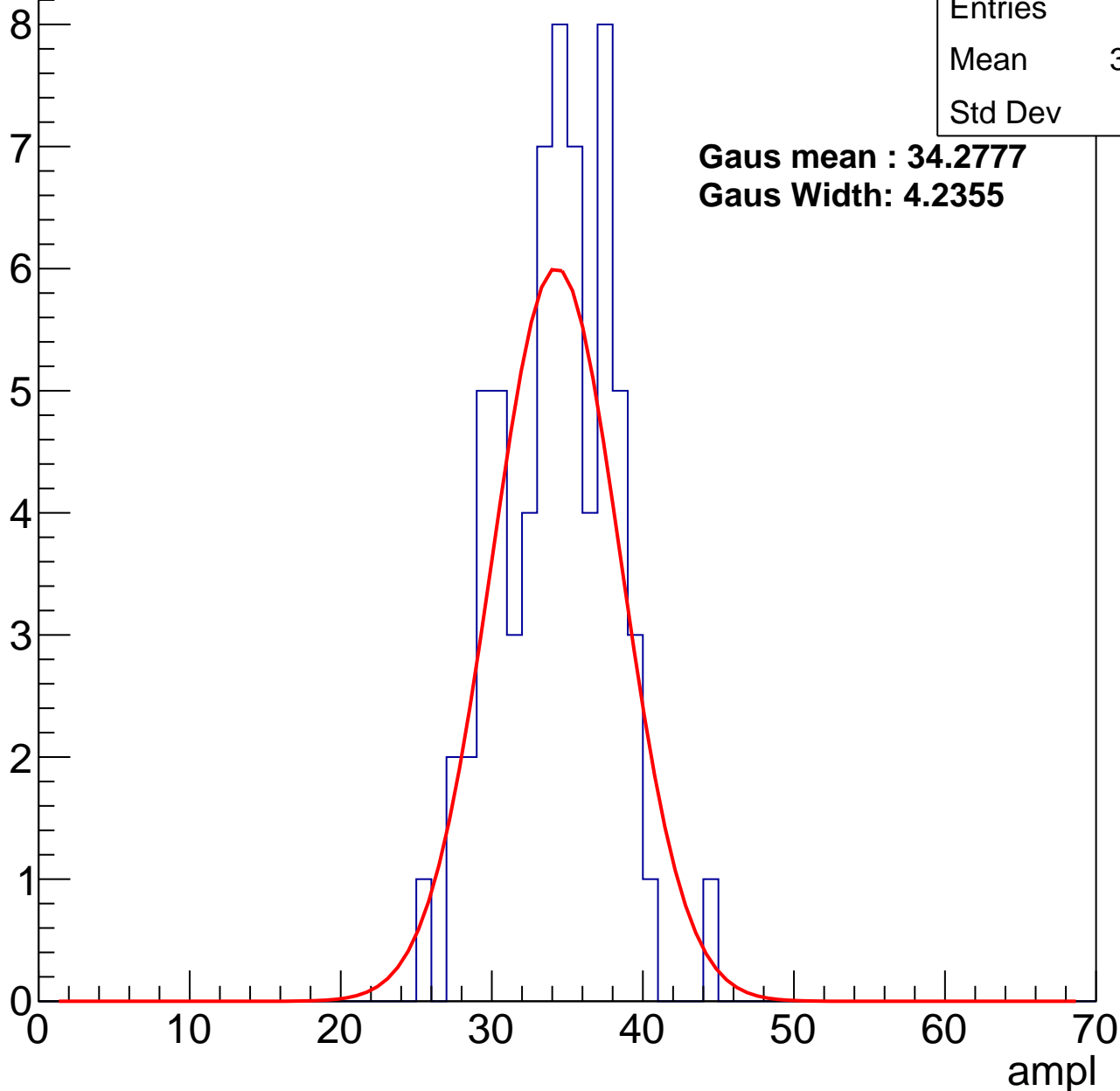
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	33.79
Std Dev	3.67

**Gaus mean : 34.2777**

**Gaus Width: 4.2355**



# B1L103S, U16-ch48, adc2

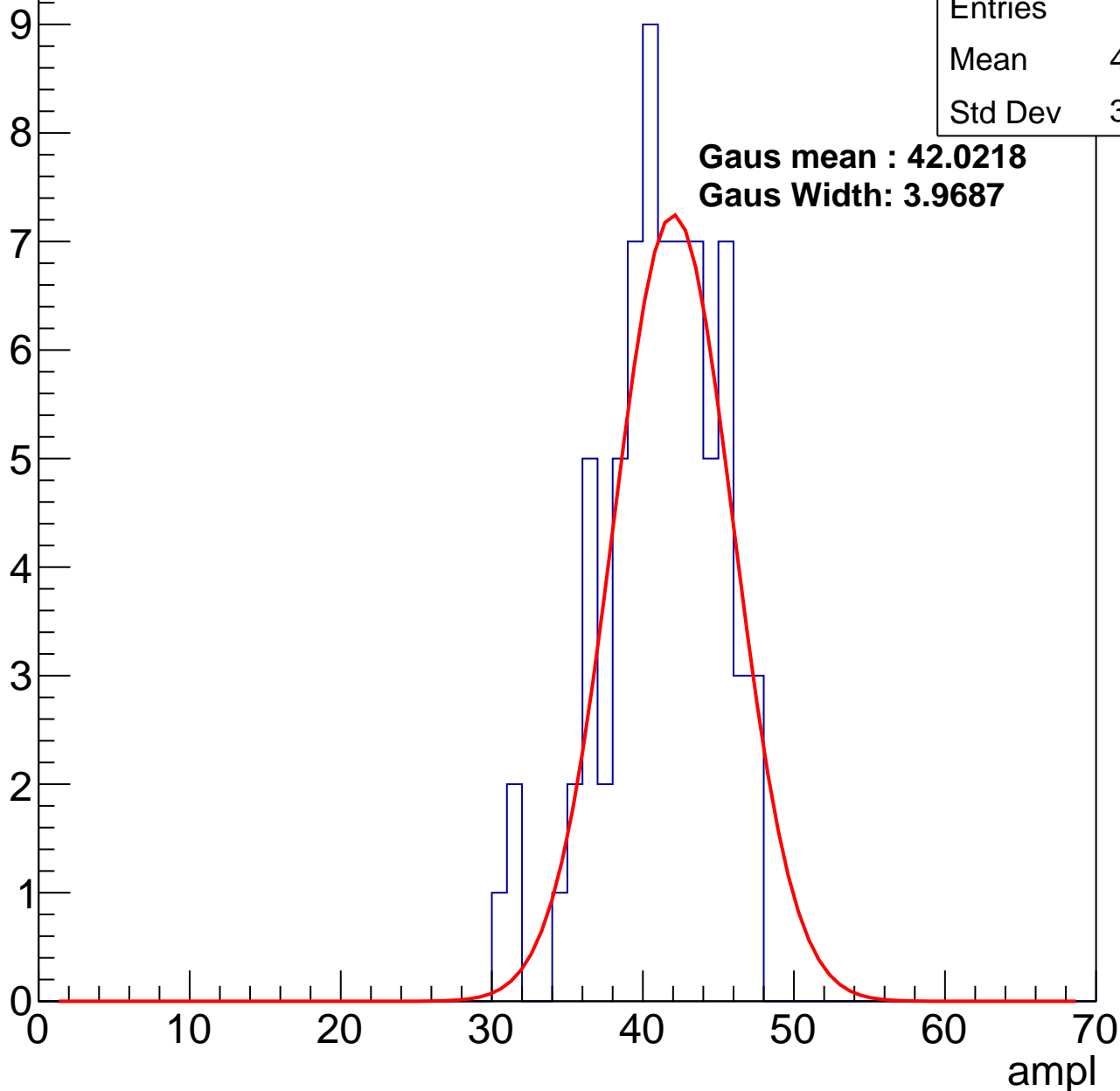
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	40.67
Std Dev	3.789

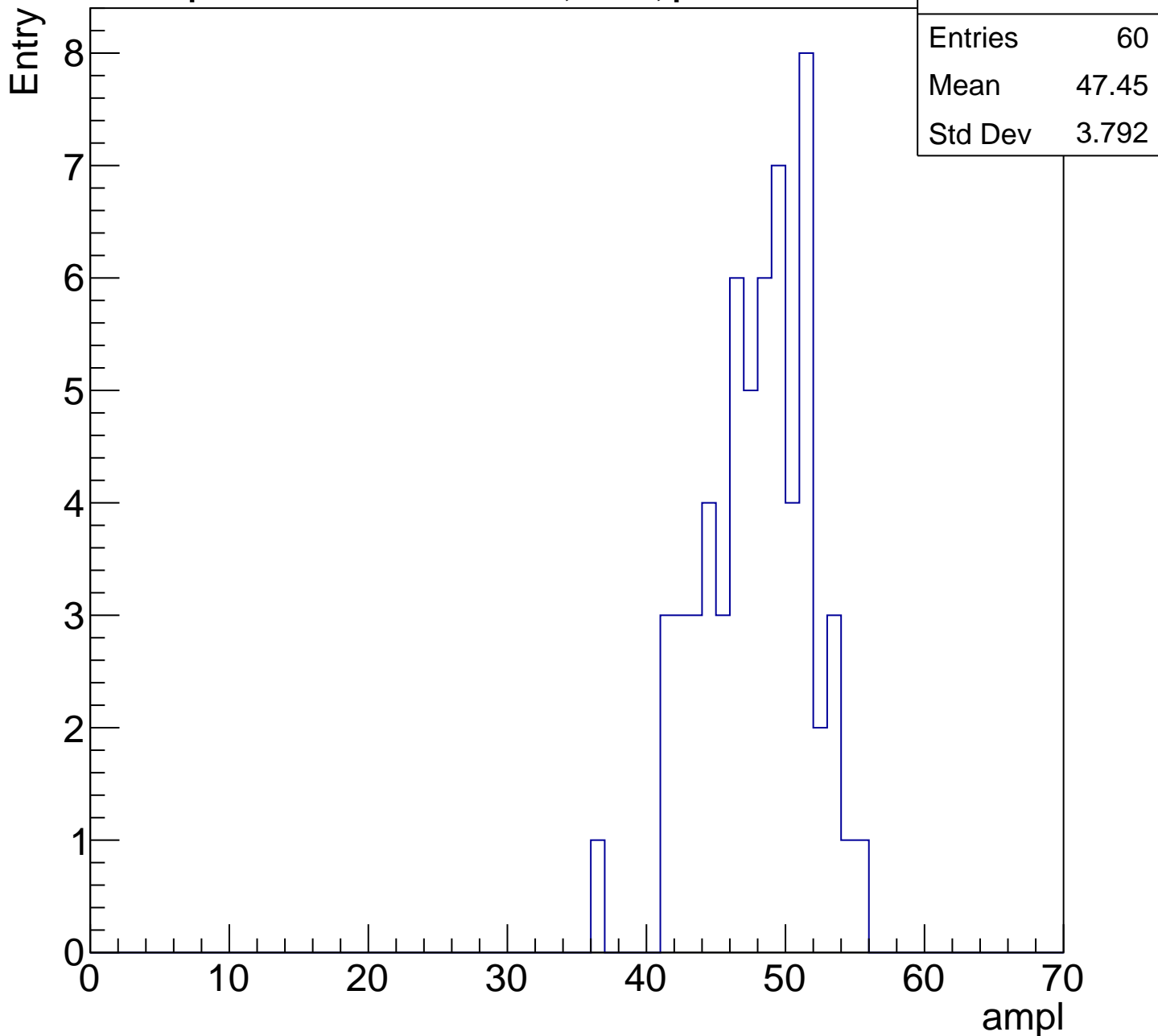
**Gaus mean : 42.0218**

**Gaus Width: 3.9687**



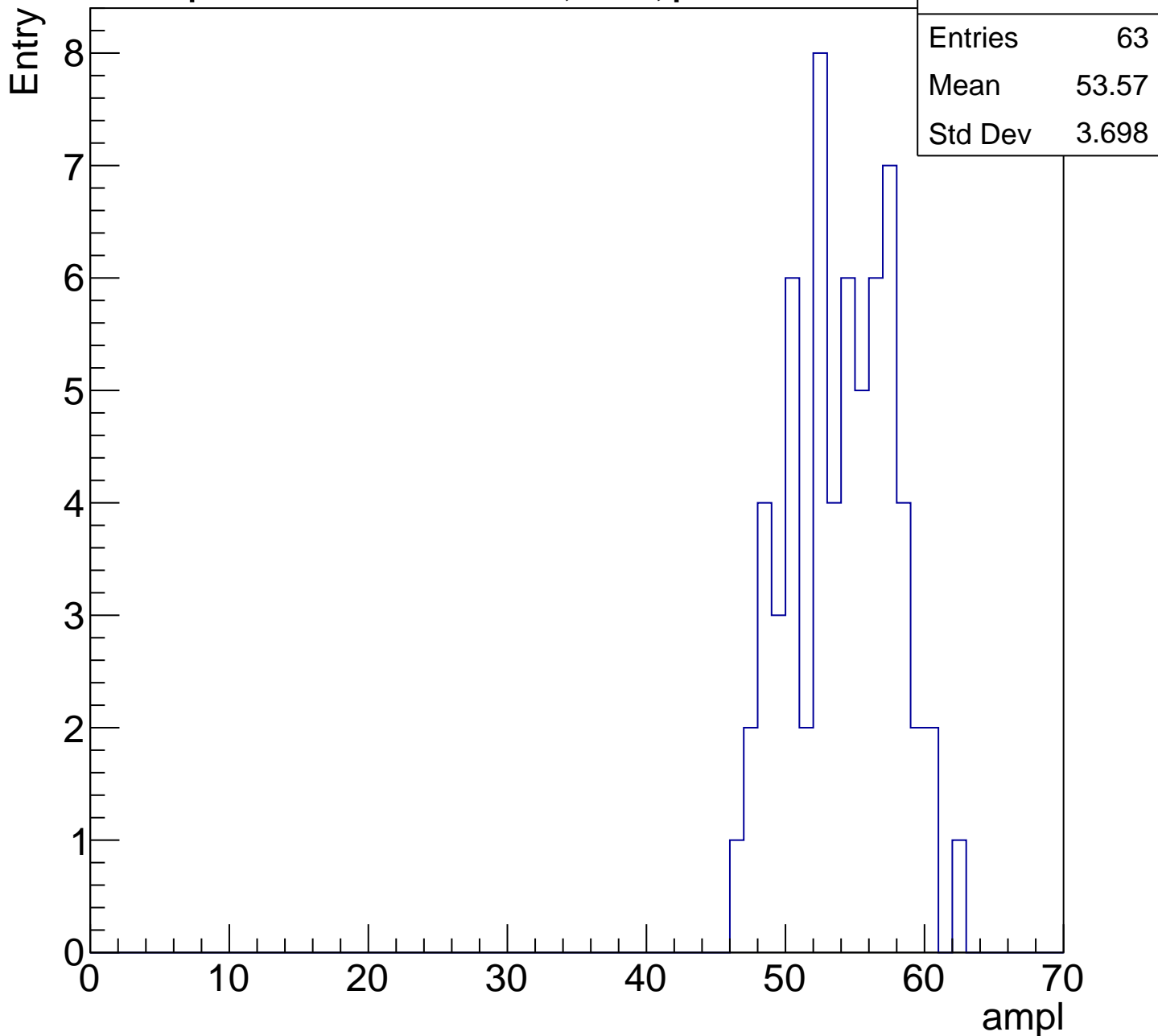
# B1L103S, U16-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U16-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

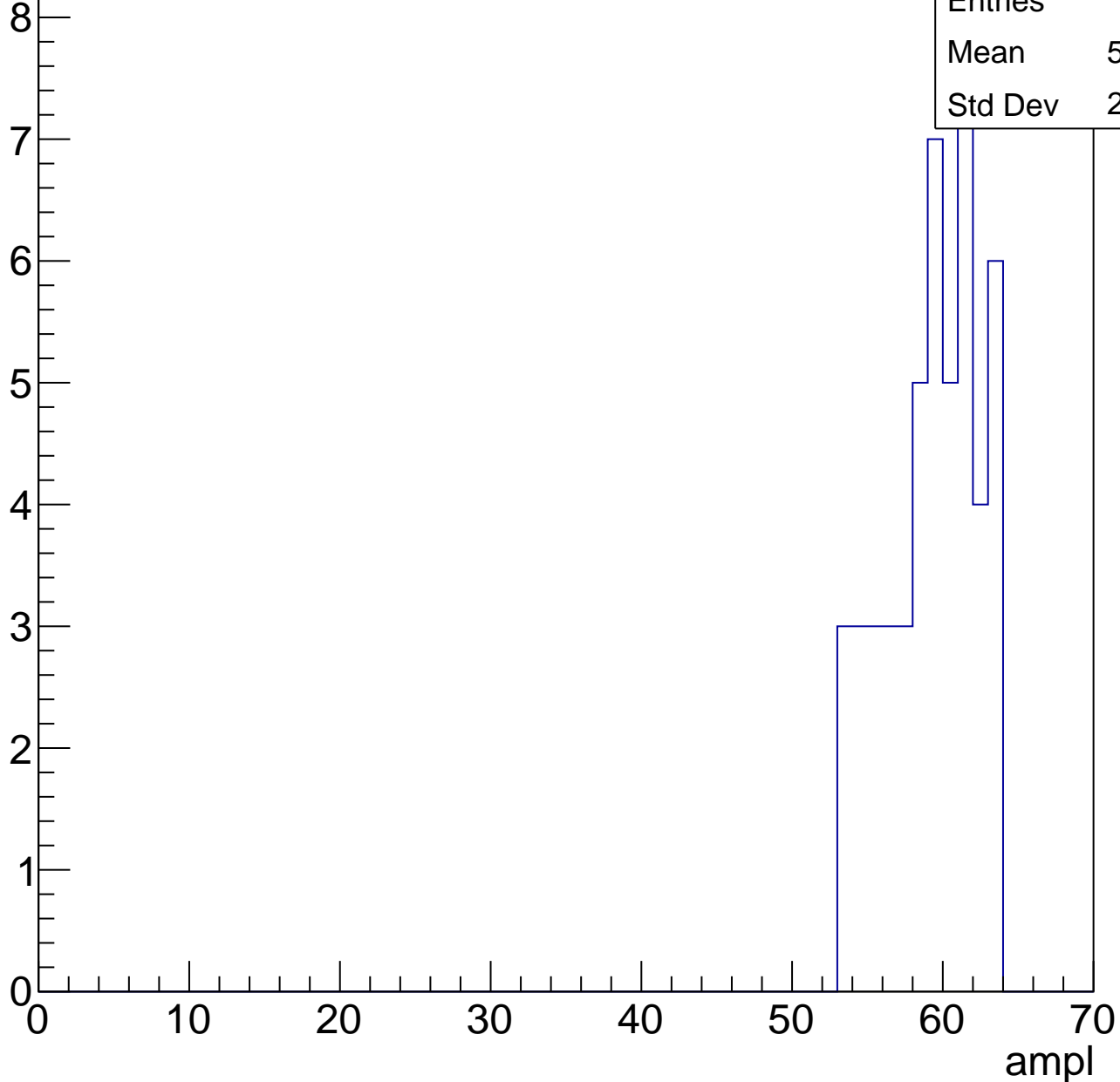


# B1L103S, U16-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	58.84
Std Dev	2.976

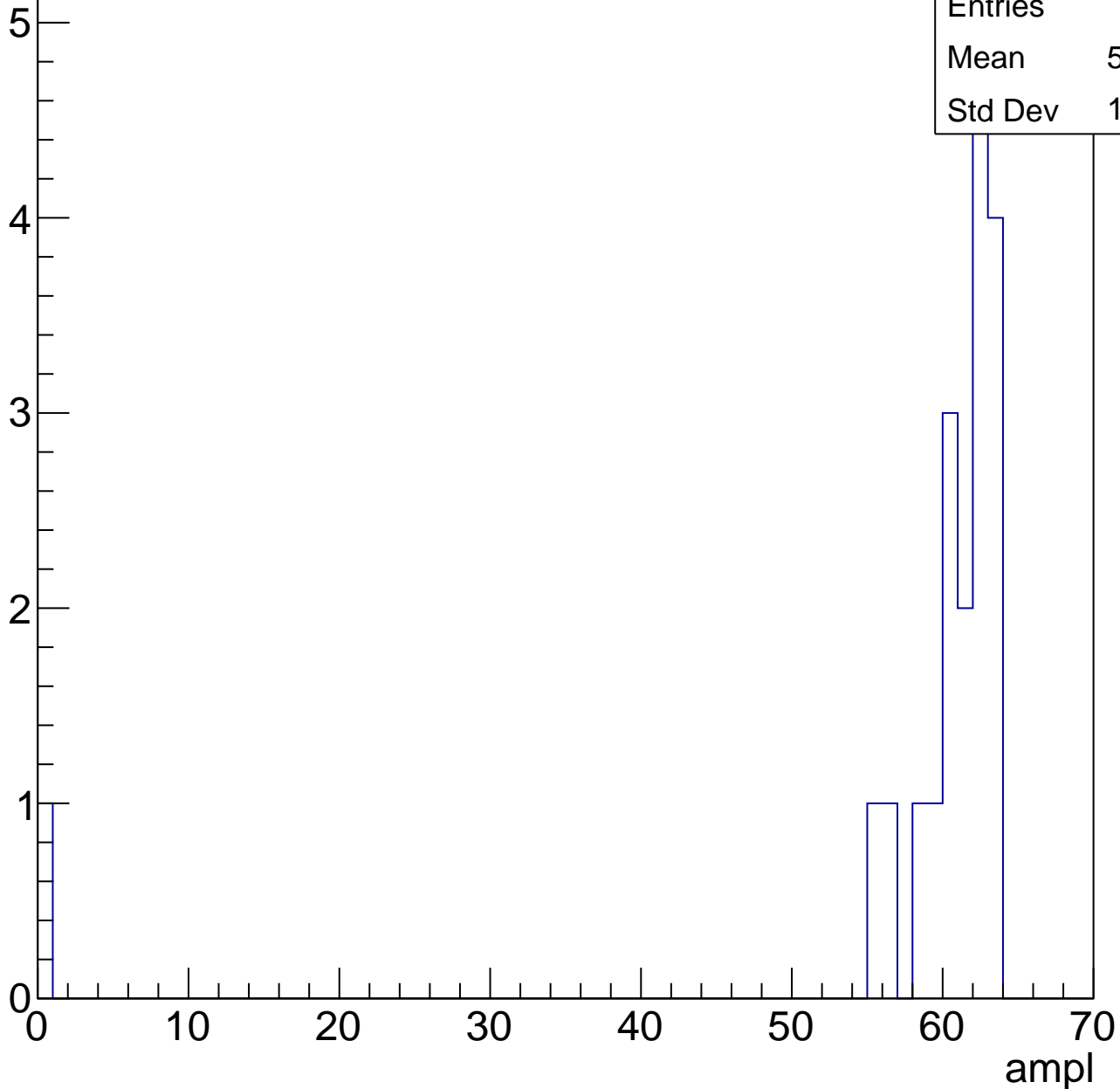


# B1L103S, U16-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	19
Mean	57.47
Std Dev	13.73





# B1L103S, U16-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U16-ch49, adc0

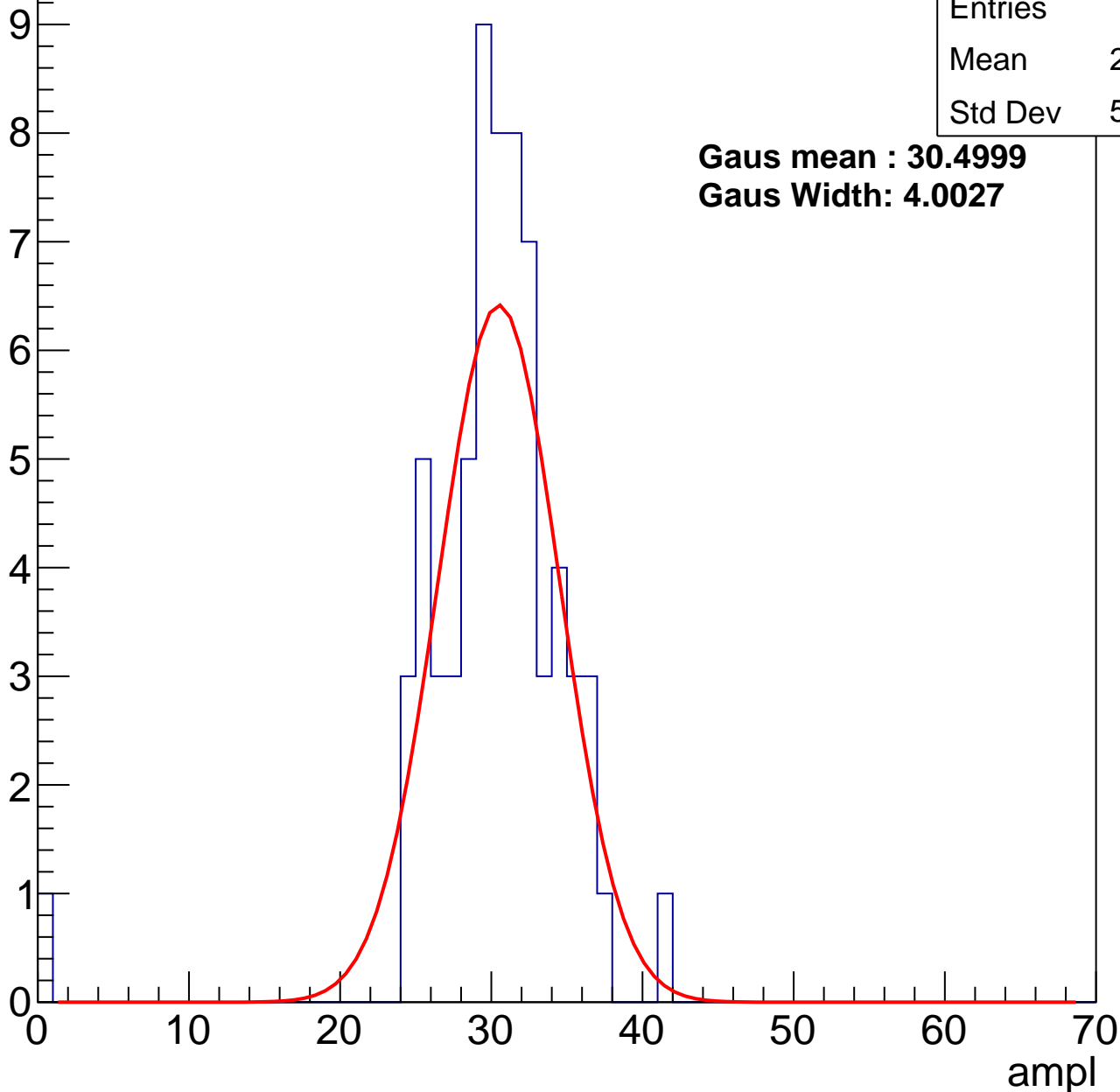
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	29.78
Std Dev	5.057

**Gaus mean : 30.4999**

**Gaus Width: 4.0027**



# B1L103S, U16-ch49, adc1

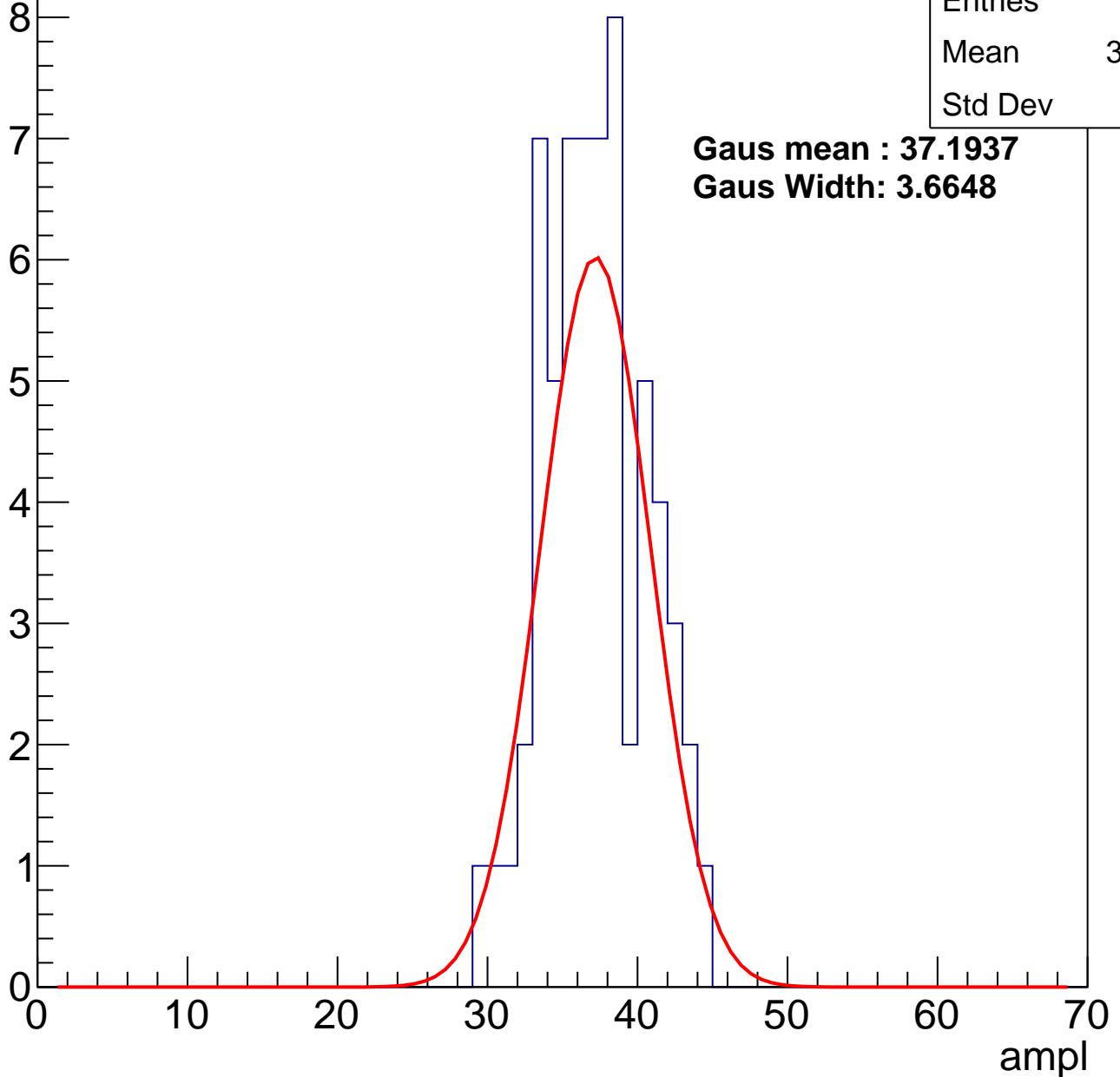
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	36.71
Std Dev	3.35

**Gaus mean : 37.1937**

**Gaus Width: 3.6648**



# B1L103S, U16-ch49, adc2

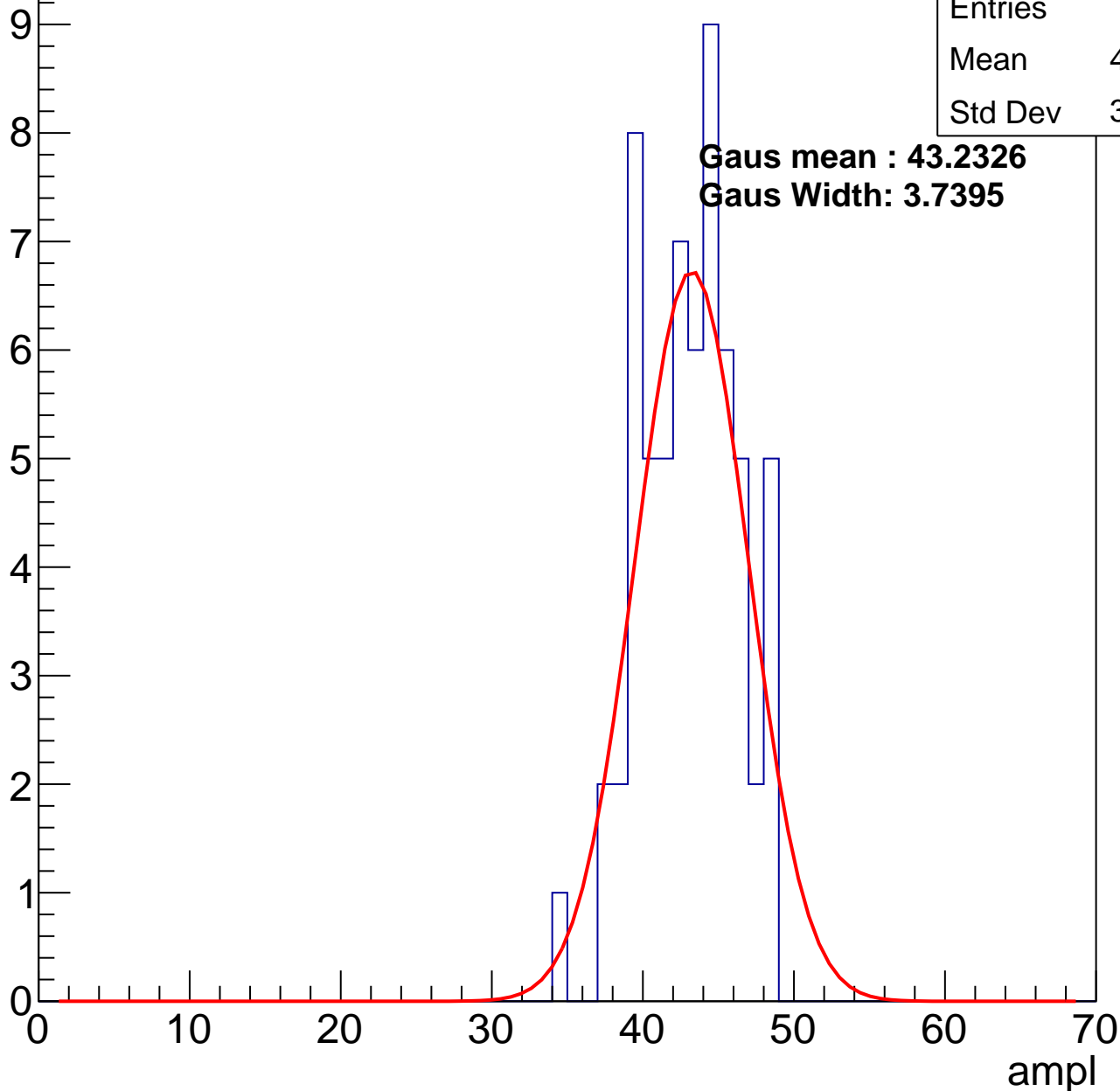
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	42.59
Std Dev	3.155

**Gaus mean : 43.2326**

**Gaus Width: 3.7395**

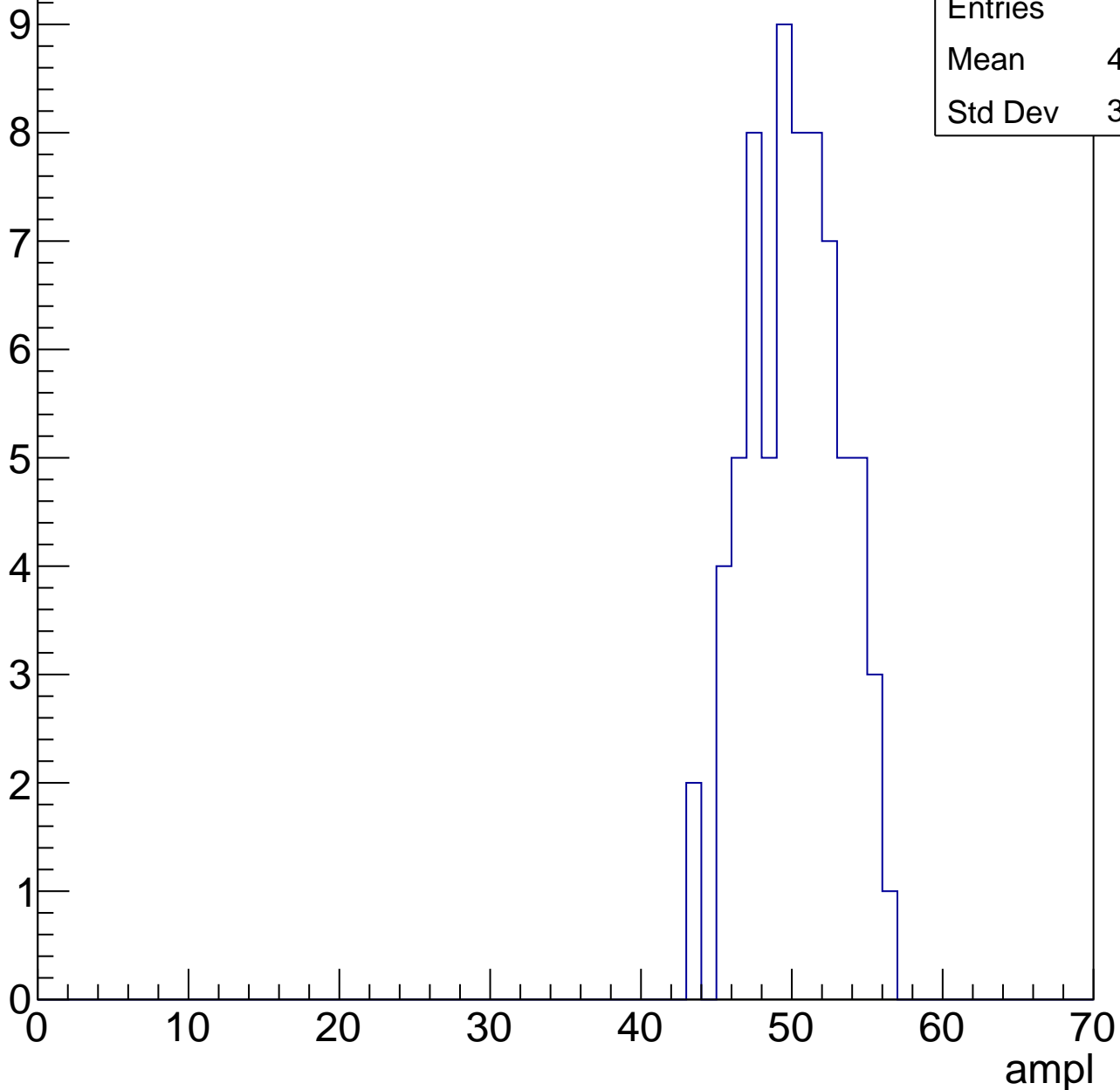


# B1L103S, U16-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	49.73
Std Dev	3.037

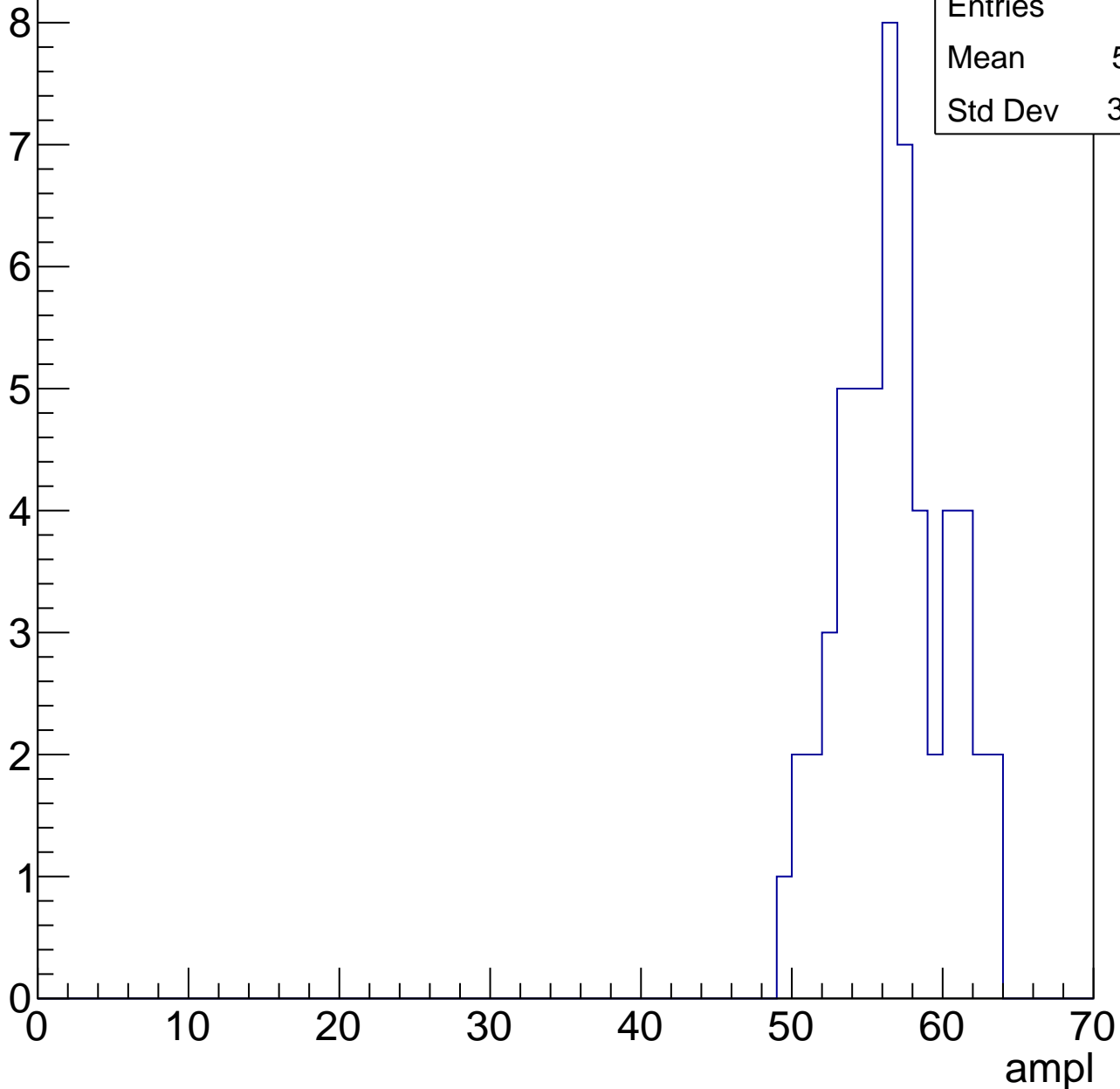


# B1L103S, U16-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	56.21
Std Dev	3.437



# B1L103S, U16-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	58.77
Std Dev	8.849

ampl

0

10

20

30

40

50

60

70

# B1L103S, U16-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch50, adc0

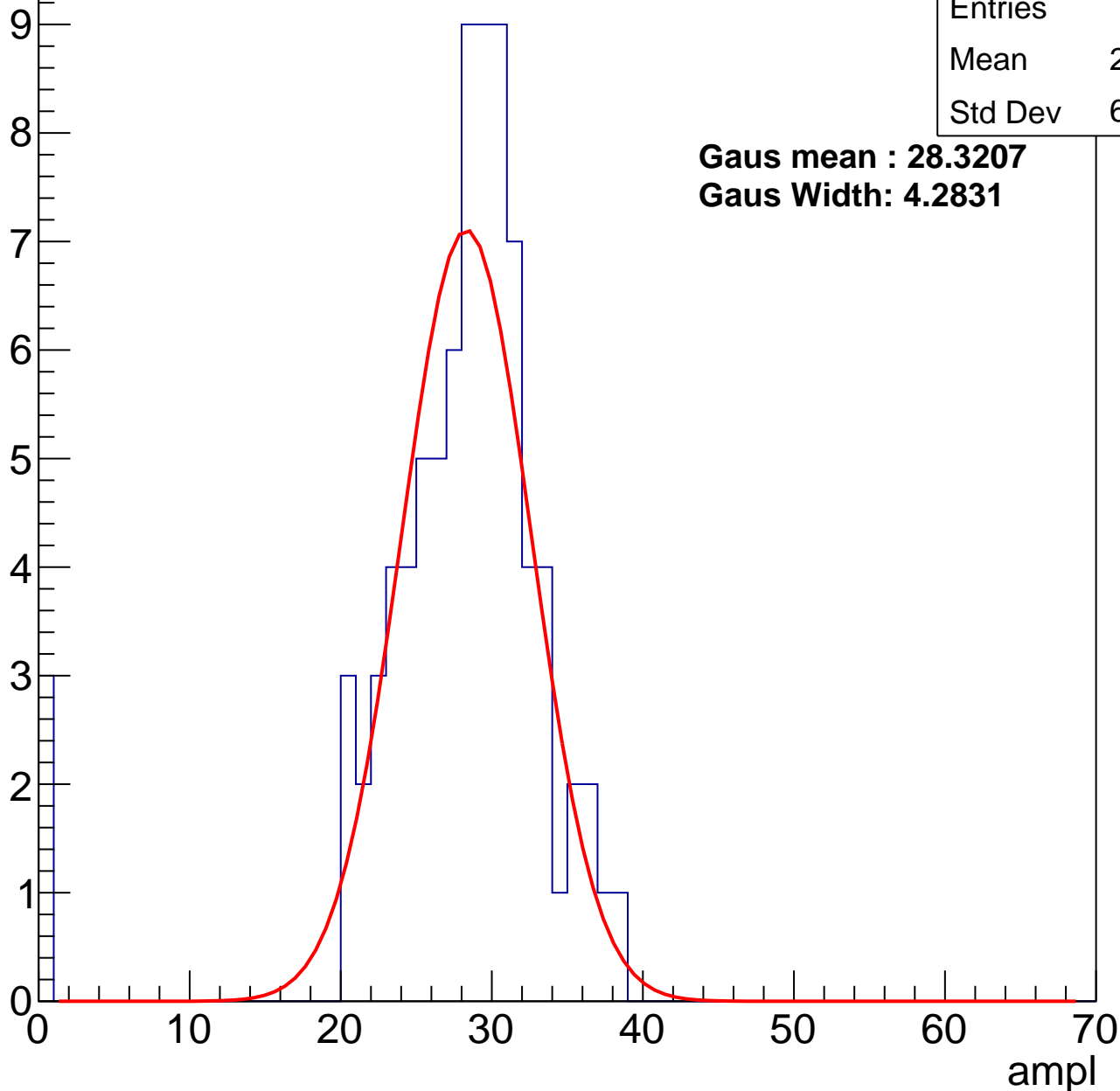
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	84
Mean	27.19
Std Dev	6.587

**Gaus mean : 28.3207**

**Gaus Width: 4.2831**



# B1L103S, U16-ch50, adc1

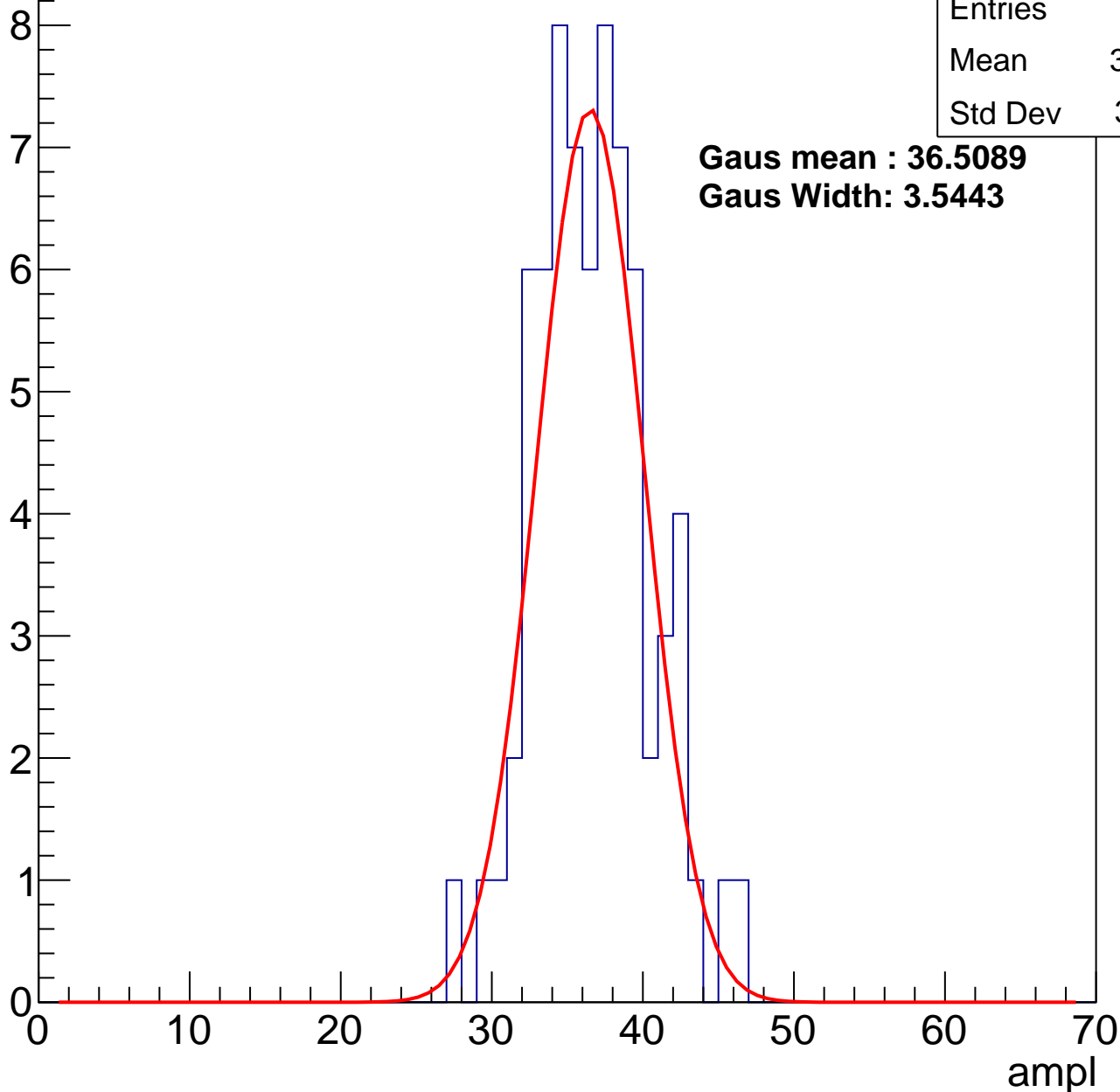
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	36.23
Std Dev	3.701

**Gaus mean : 36.5089**

**Gaus Width: 3.5443**



# B1L103S, U16-ch50, adc2

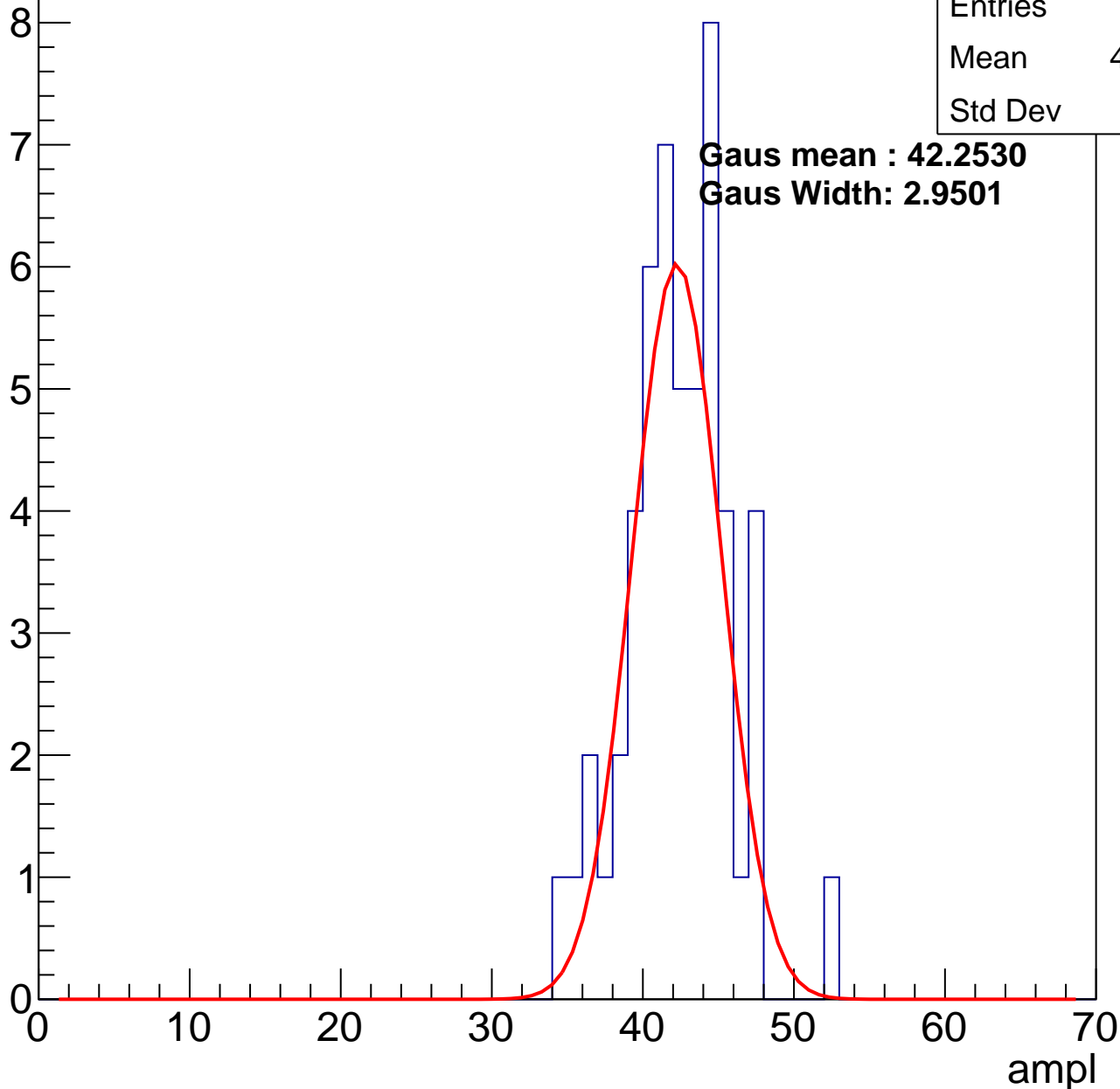
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	41.92
Std Dev	3.39

**Gaus mean : 42.2530**

**Gaus Width: 2.9501**



# B1L103S, U16-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	76
Mean	48.88
Std Dev	3.738

Entry

10

8

6

4

2

0

0

10

20

30

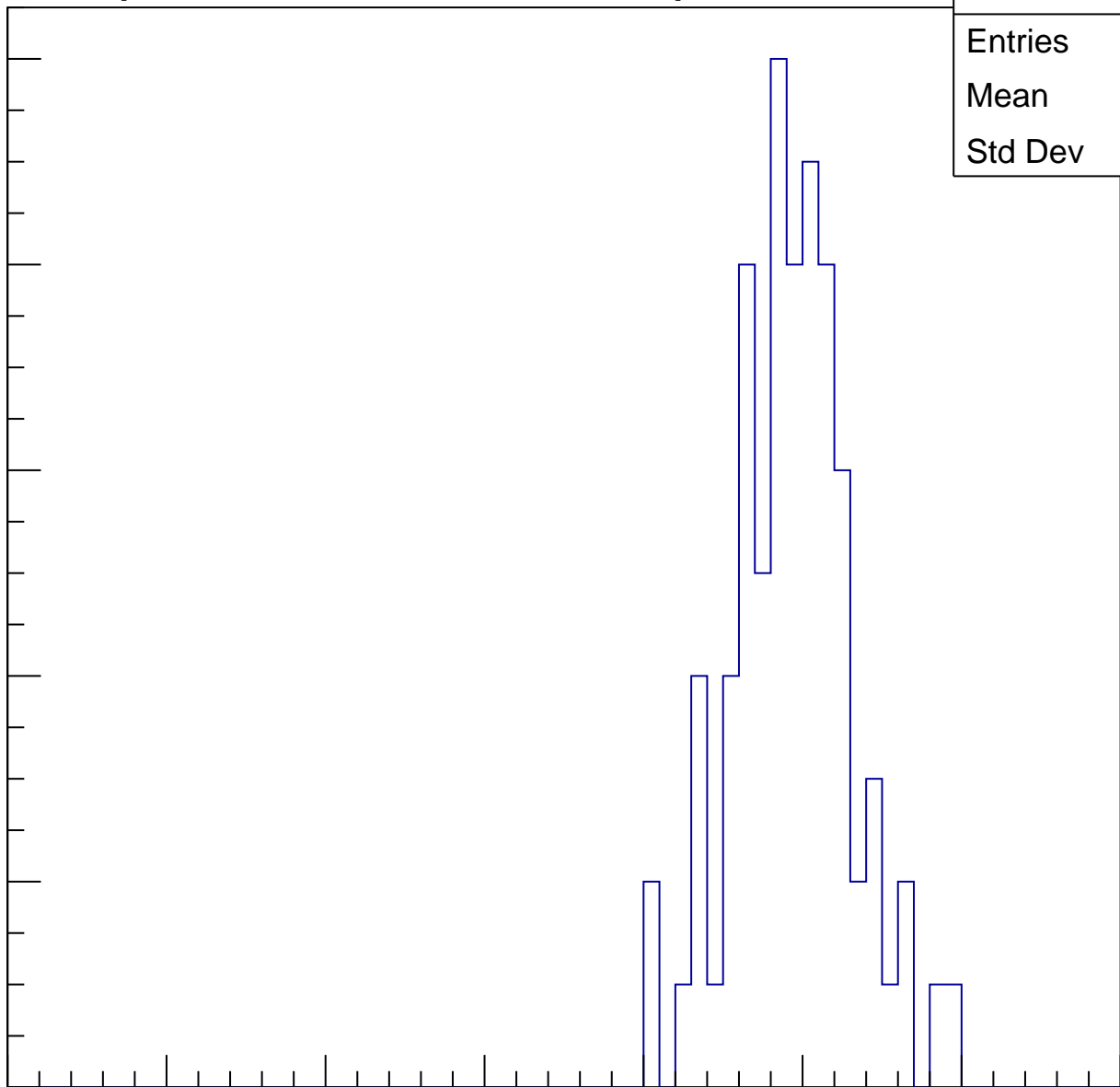
40

50

60

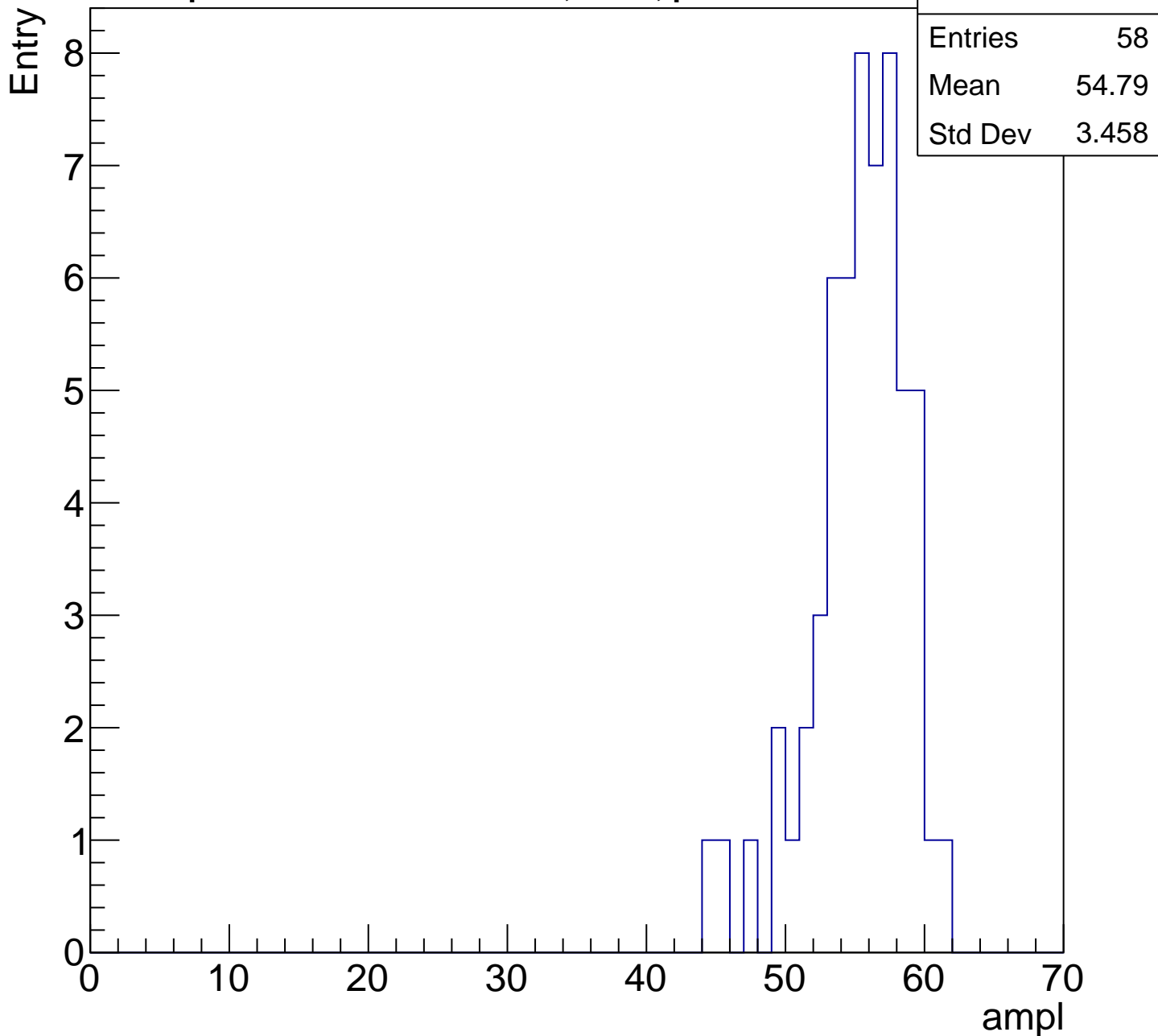
70

ampl



# B1L103S, U16-ch50, adc4

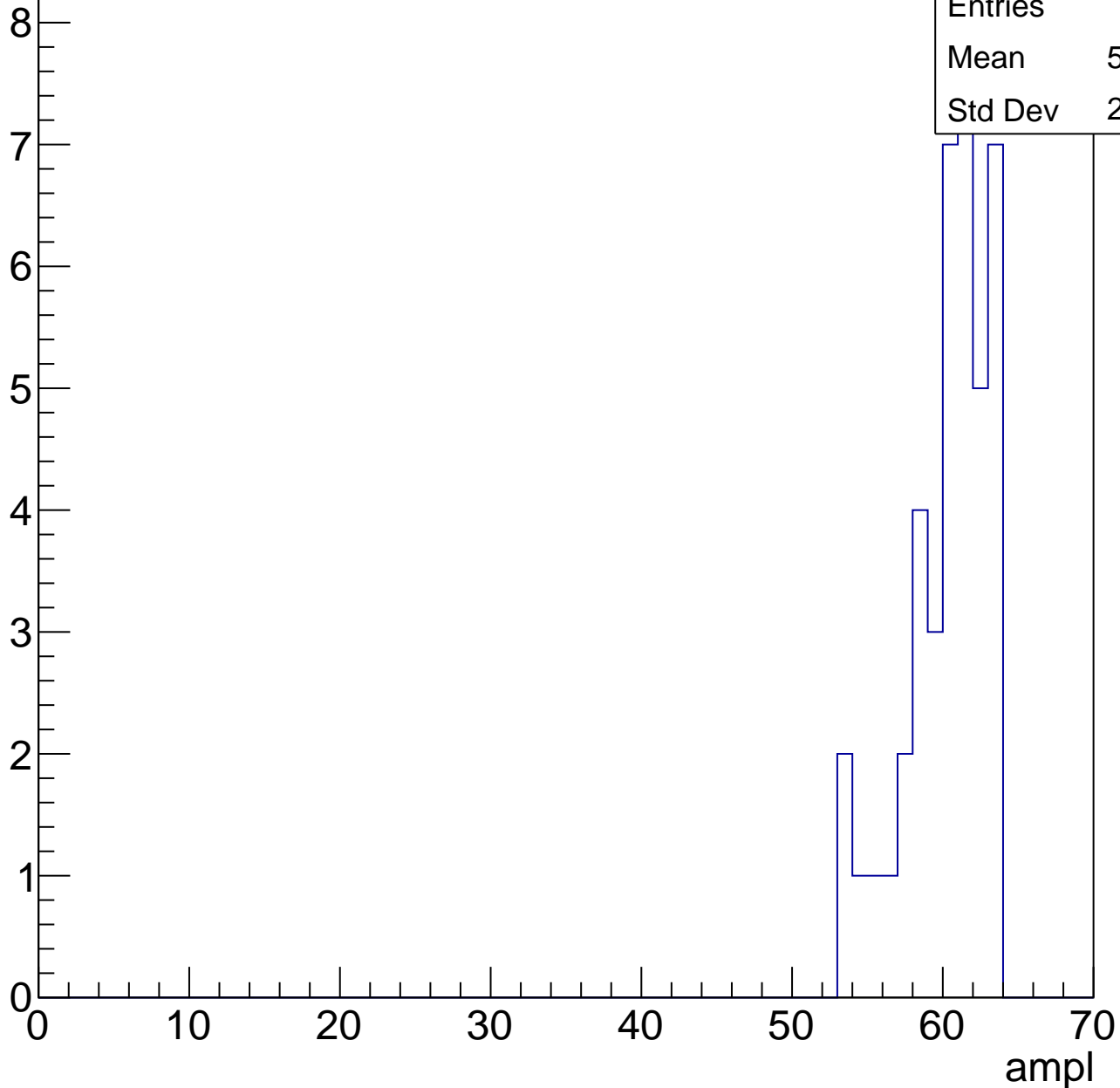
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U16-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



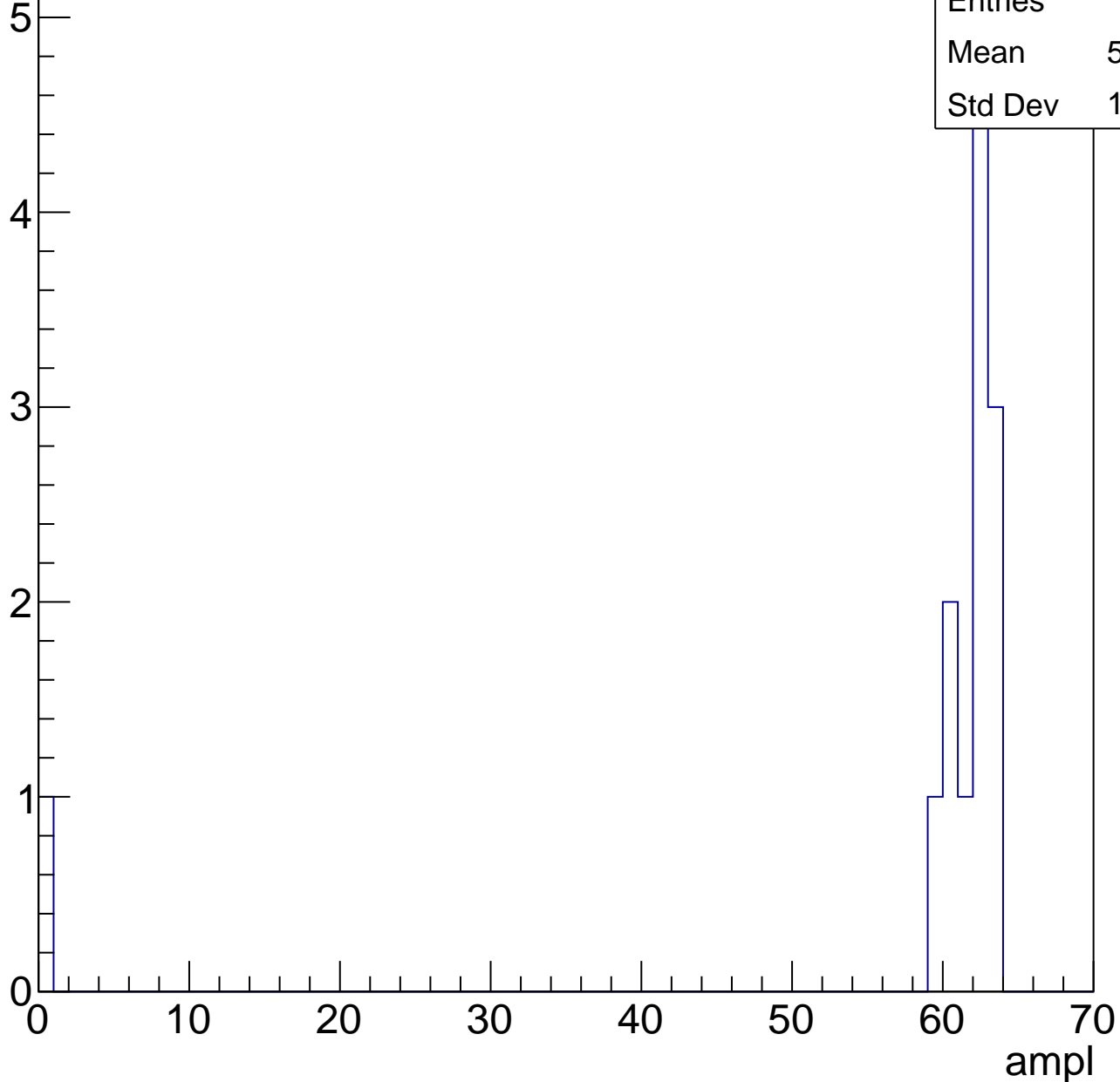
Entries	41
Mean	59.83
Std Dev	2.713

# B1L103S, U16-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	13
Mean	56.85
Std Dev	16.45





# B1L103S, U16-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U16-ch51, adc0

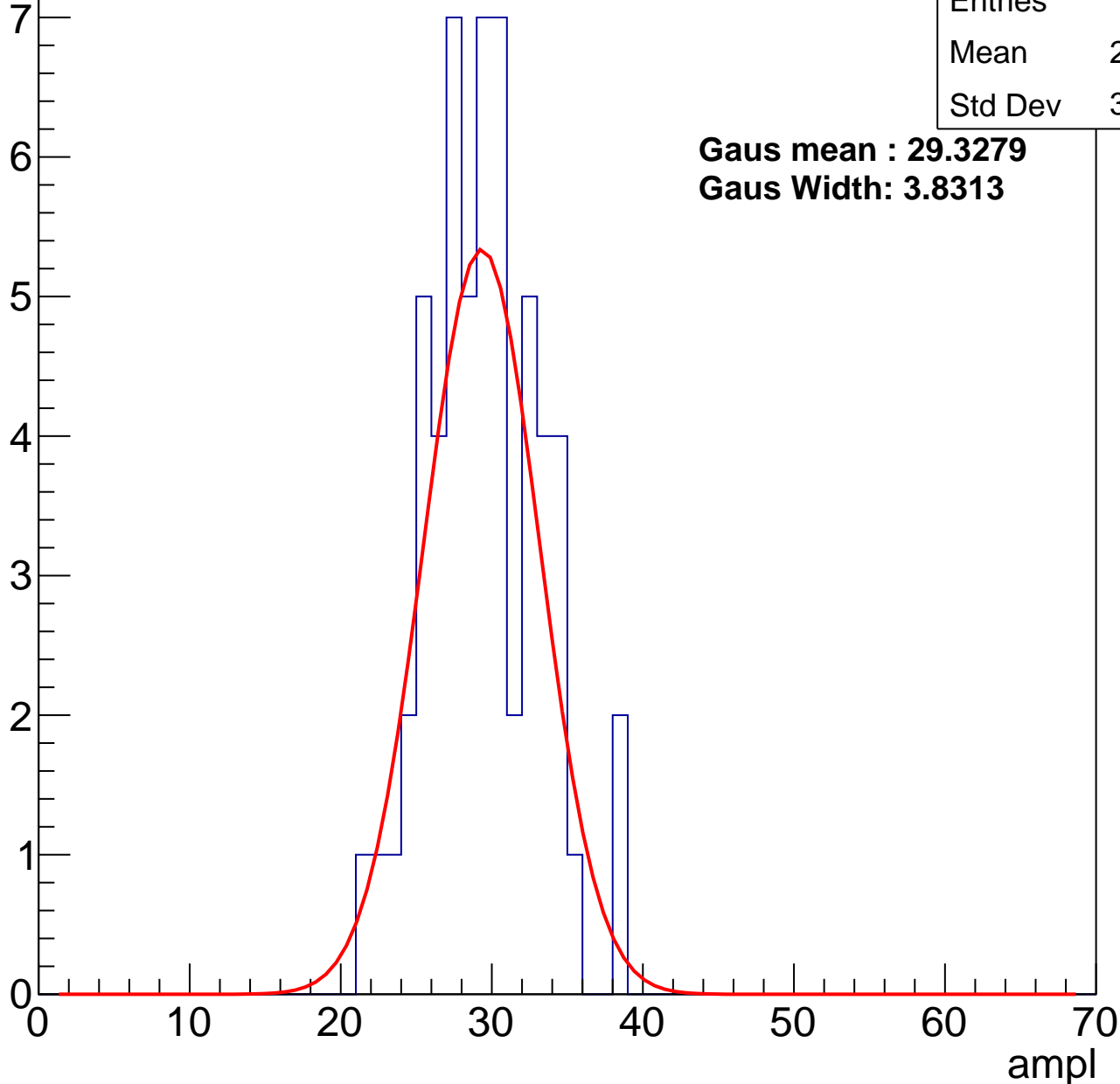
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	29.07
Std Dev	3.643

**Gaus mean : 29.3279**

**Gaus Width: 3.8313**



# B1L103S, U16-ch51, adc1

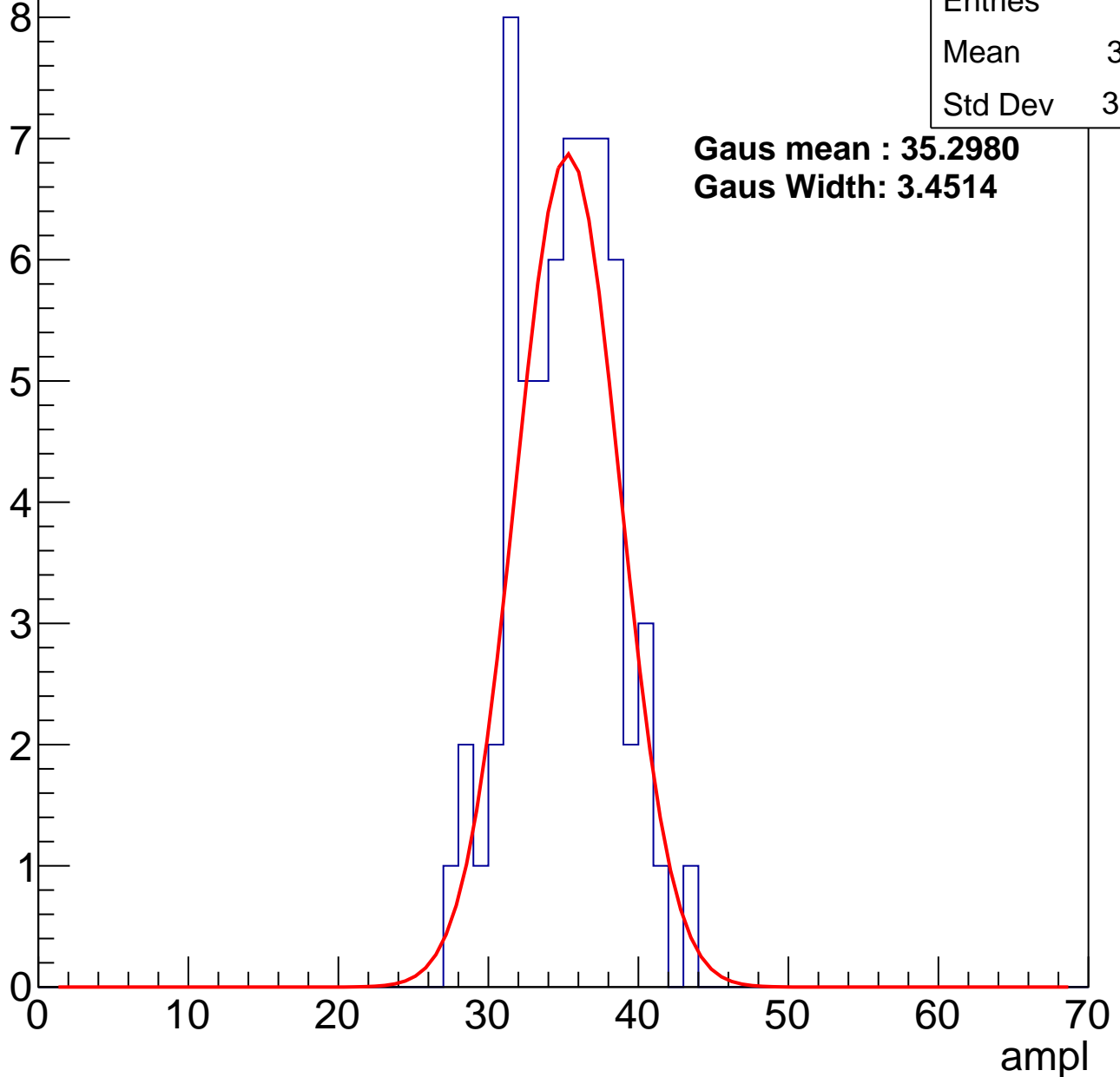
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	34.61
Std Dev	3.385

**Gaus mean : 35.2980**

**Gaus Width: 3.4514**



# B1L103S, U16-ch51, adc2

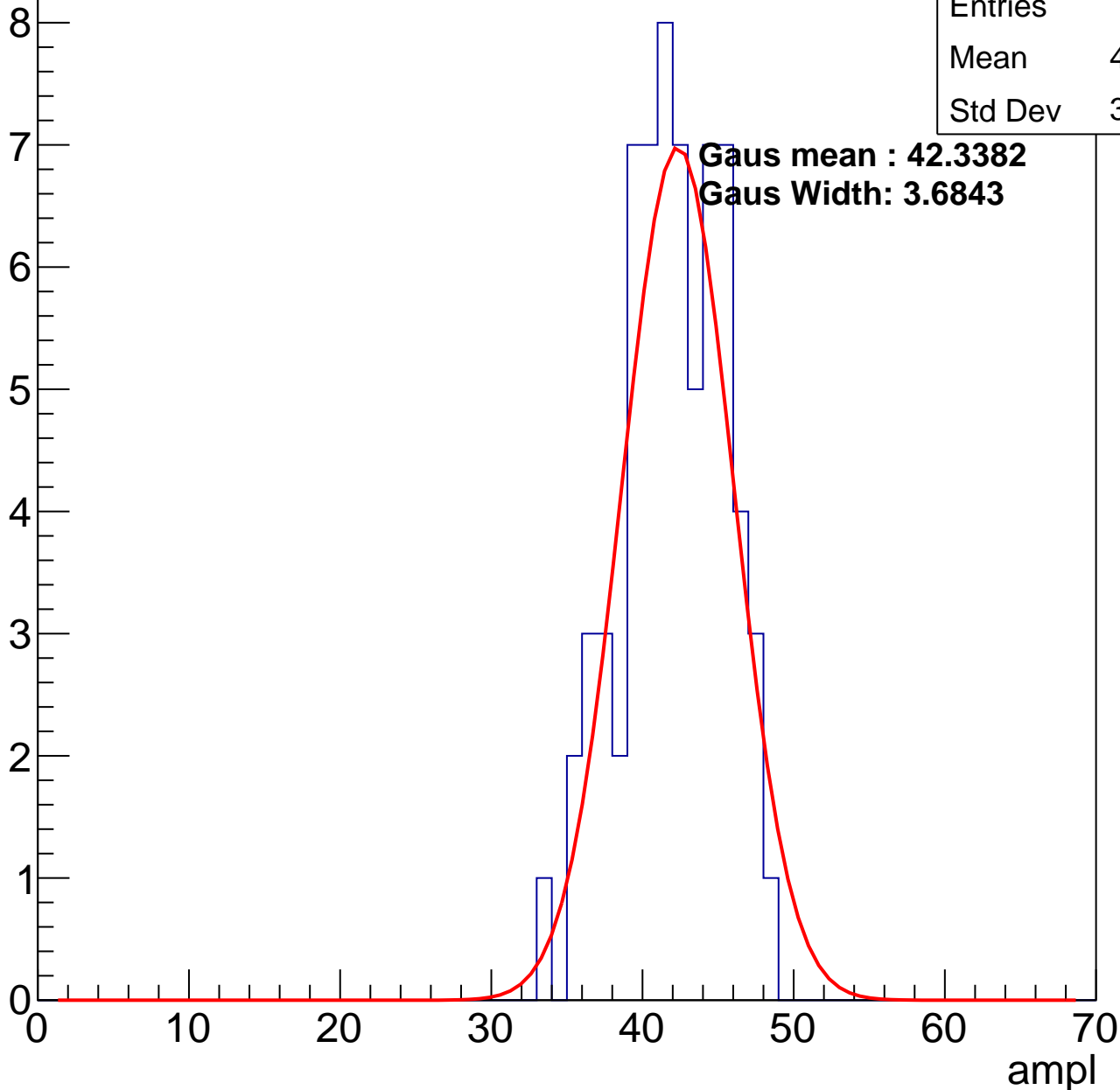
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	41.55
Std Dev	3.347

**Gaus mean : 42.3382**

**Gaus Width: 3.6843**



# B1L103S, U16-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	83
Mean	48.77
Std Dev	3.638

Entry

10

8

6

4

2

0

0

10

20

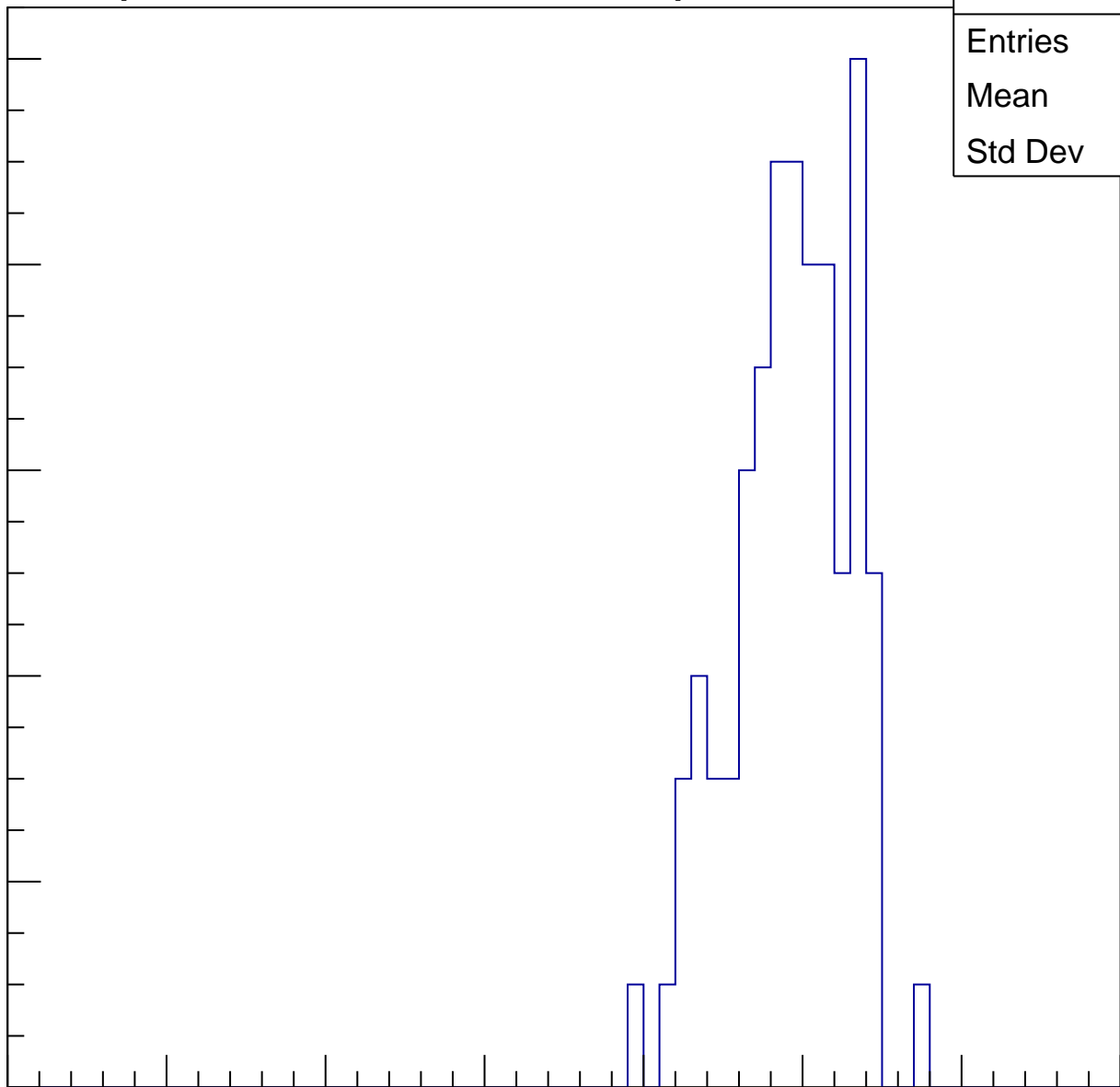
30

40

50

60

ampl

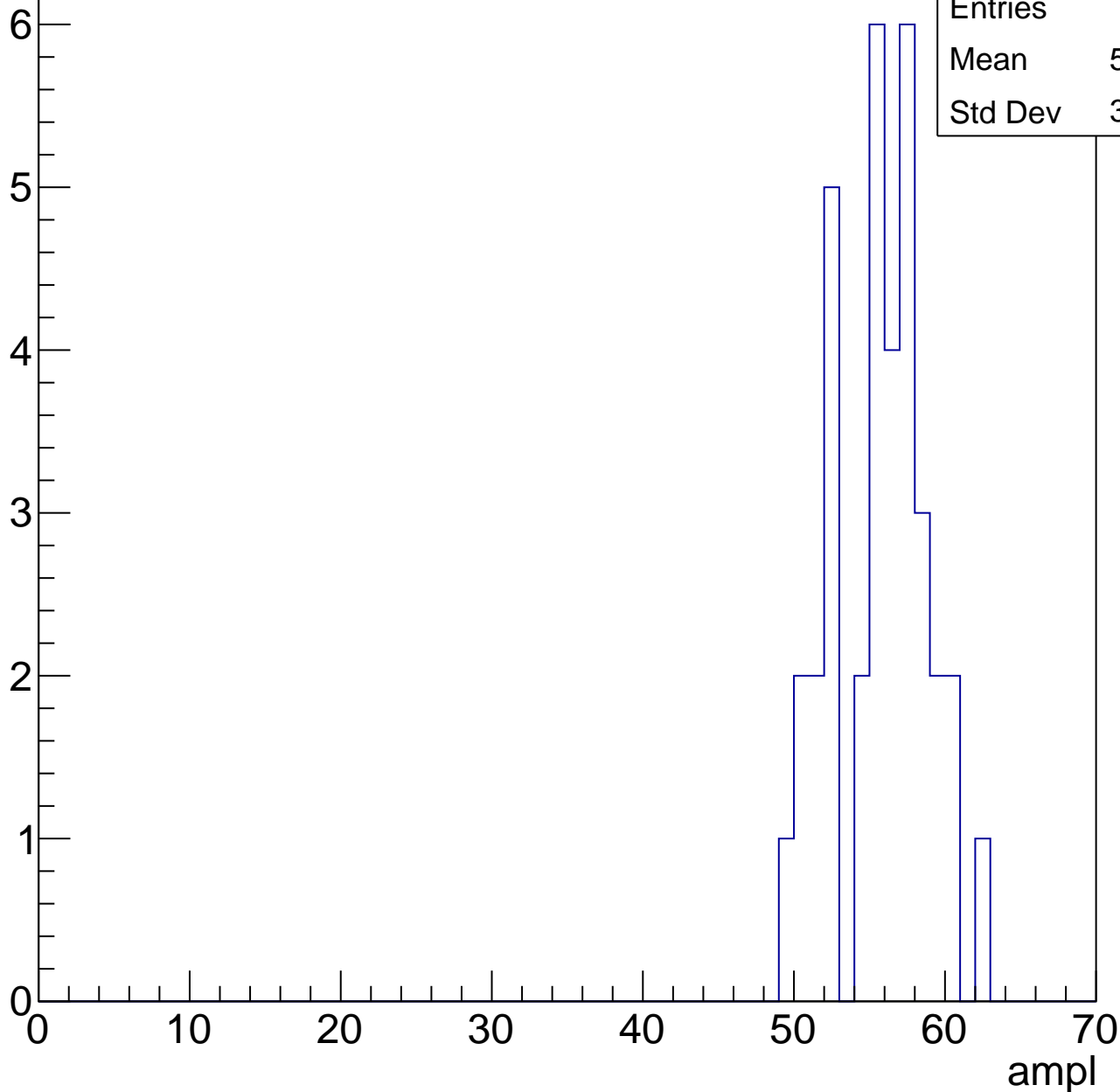


# B1L103S, U16-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	36
Mean	55.25
Std Dev	3.112



# B1L103S, U16-ch51, adc5

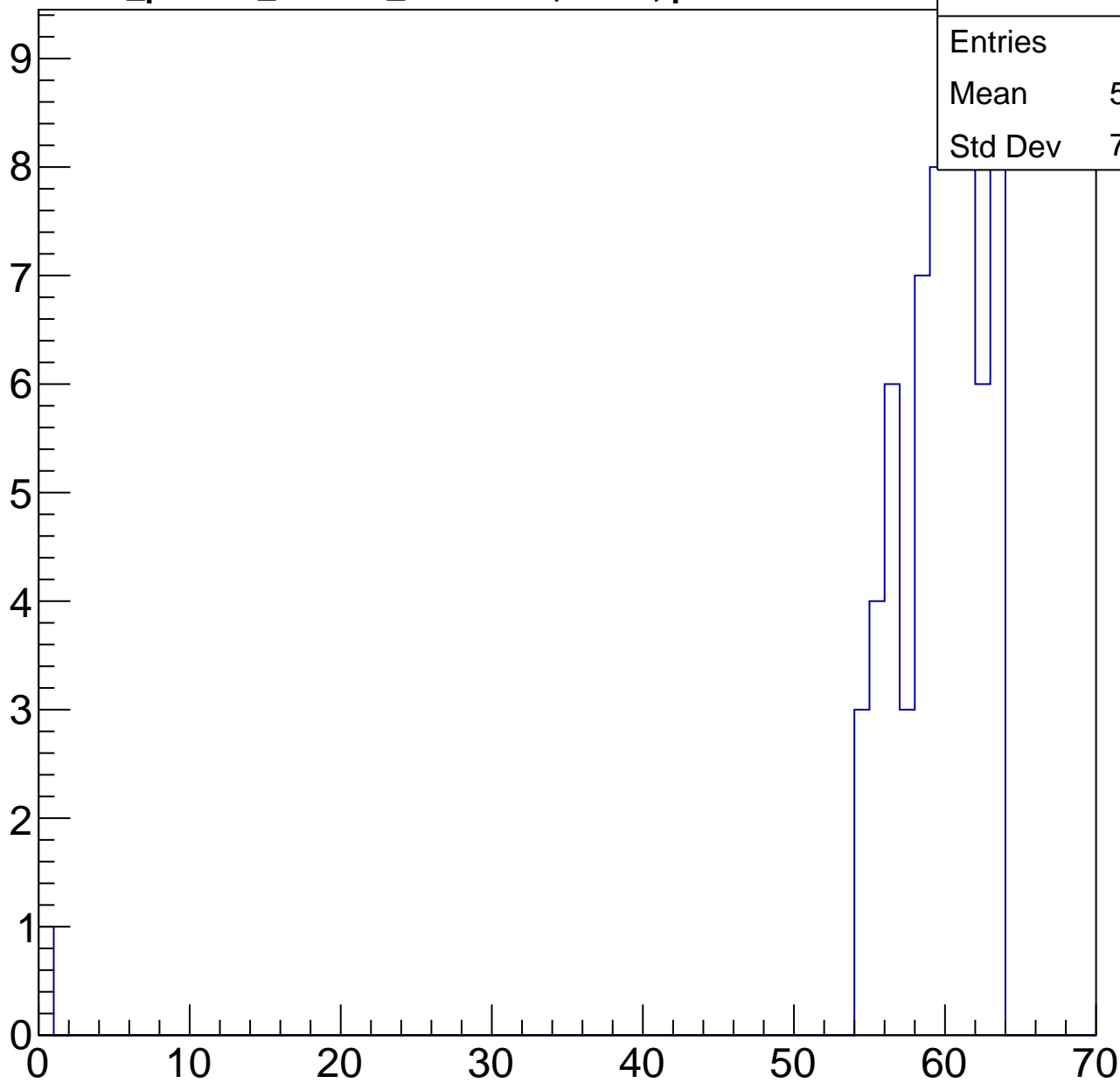
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	64
Mean	58.36
Std Dev	7.815

ampl



# B1L103S, U16-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	10.5
Std Dev	10.5

# B1L103S, U16-ch52, adc0

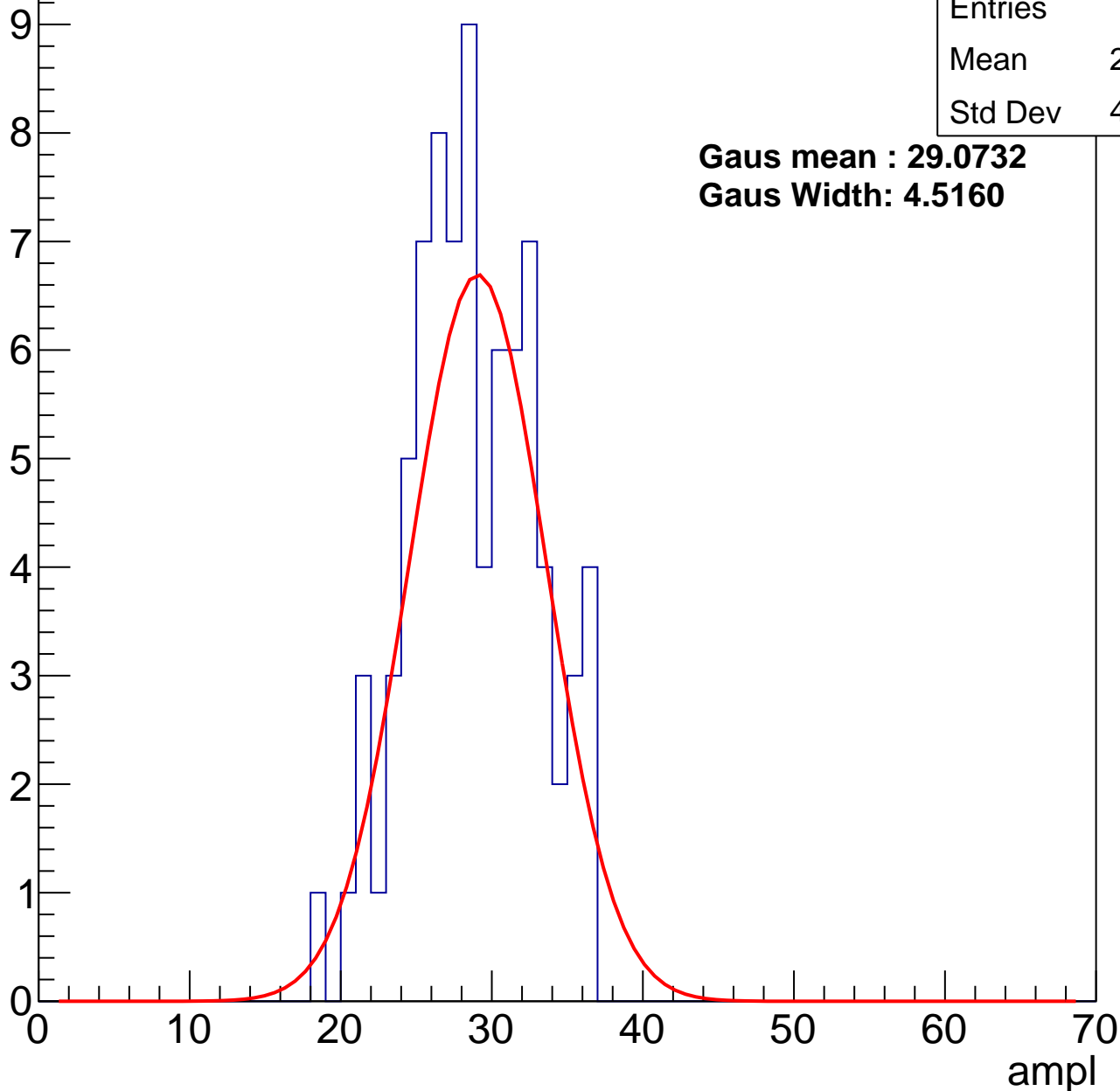
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	81
Mean	28.28
Std Dev	4.107

**Gaus mean : 29.0732**

**Gaus Width: 4.5160**



# B1L103S, U16-ch52, adc1

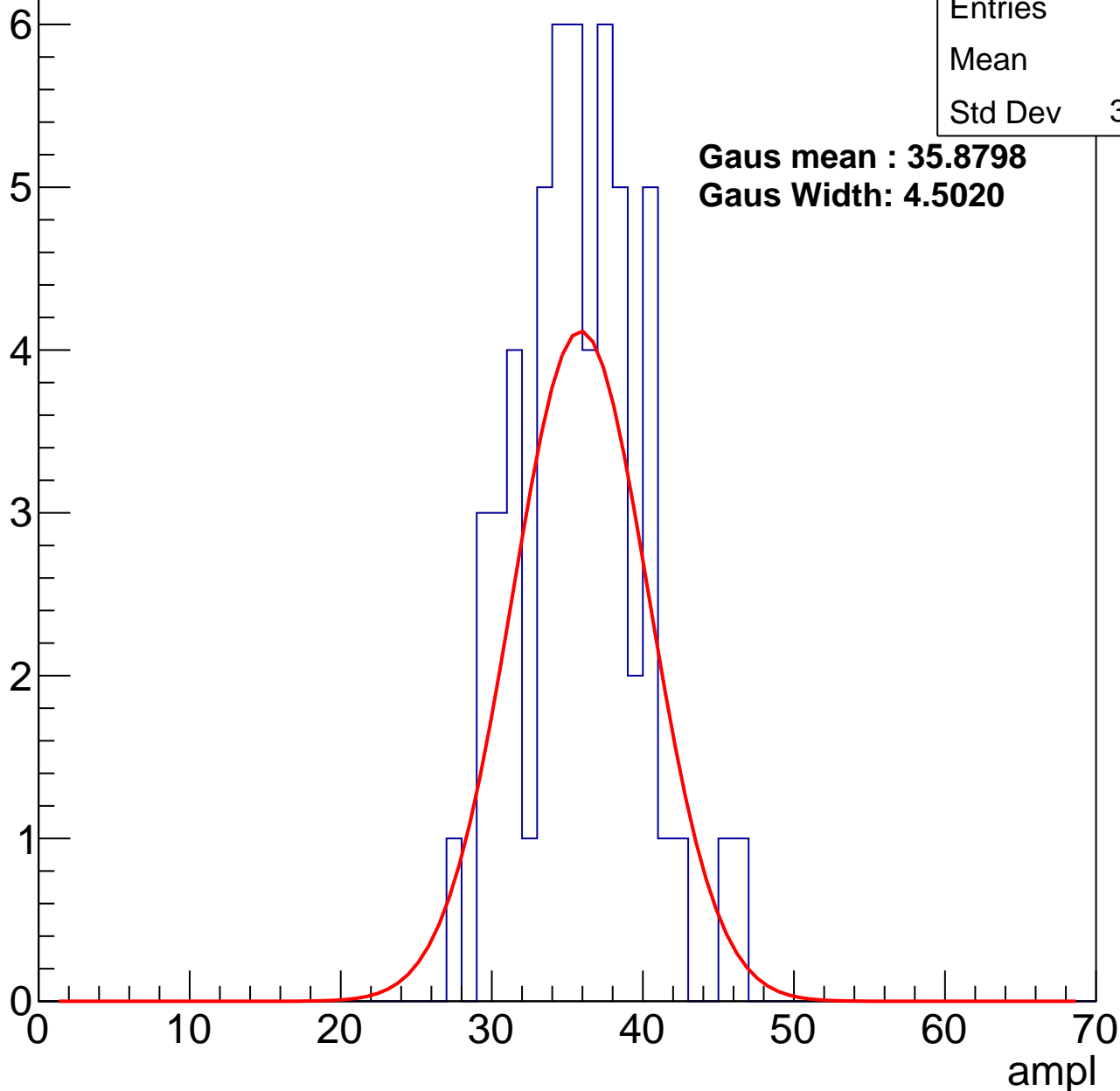
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	35.4
Std Dev	3.985

**Gaus mean : 35.8798**

**Gaus Width: 4.5020**



# B1L103S, U16-ch52, adc2

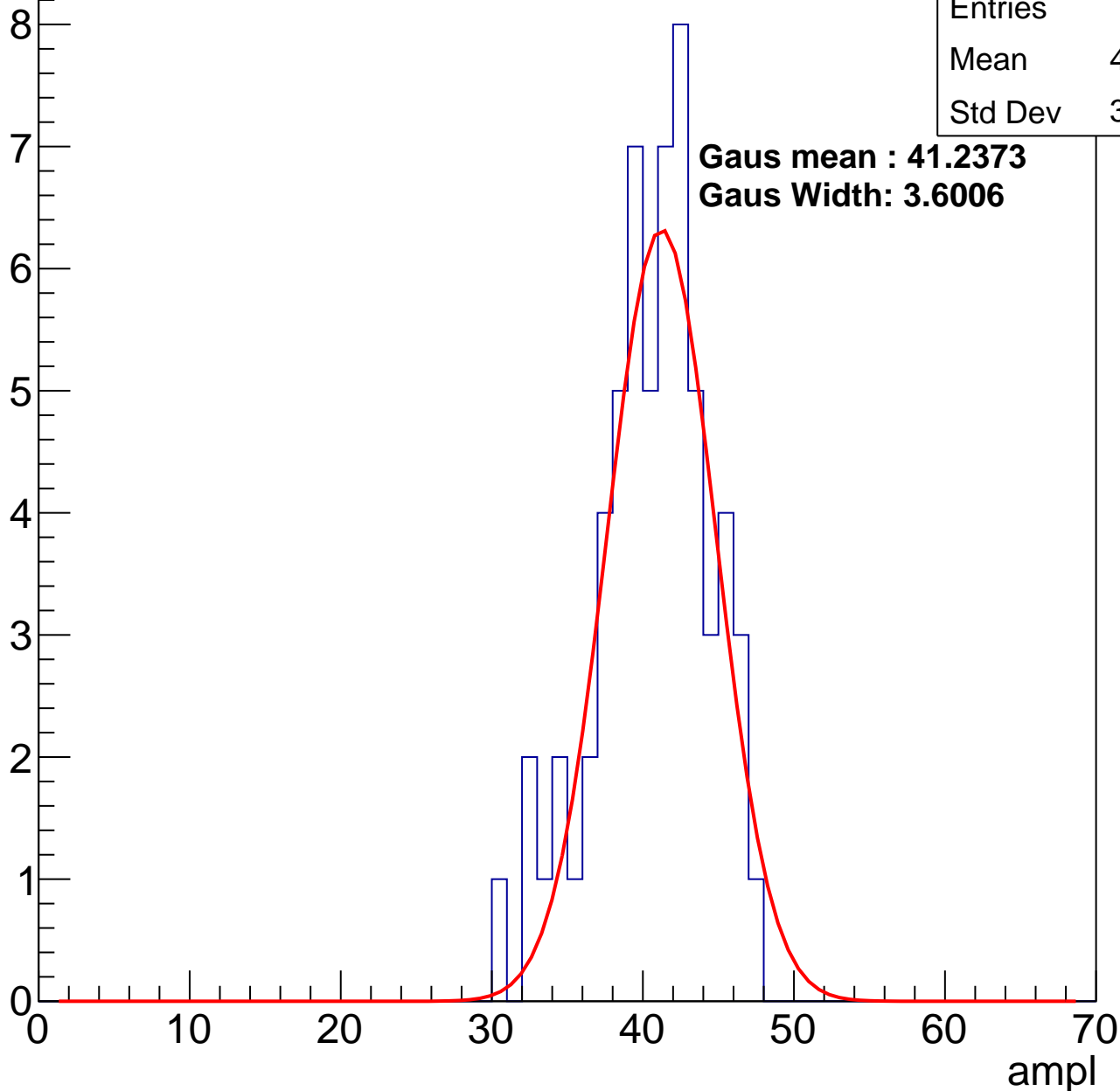
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	40.13
Std Dev	3.748

**Gaus mean : 41.2373**

**Gaus Width: 3.6006**



# B1L103S, U16-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

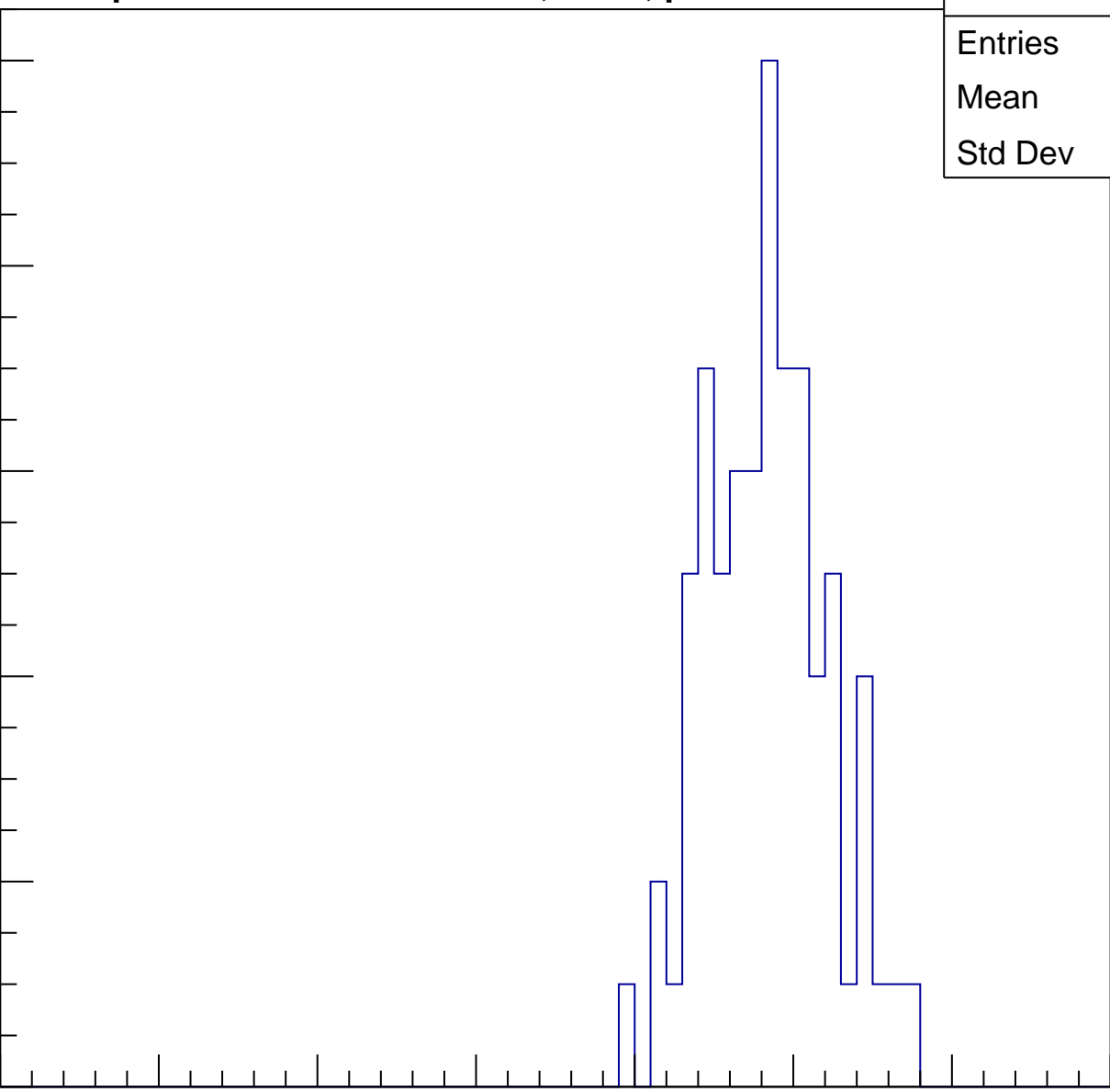
Entries	74
Mean	47.88
Std Dev	3.749

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

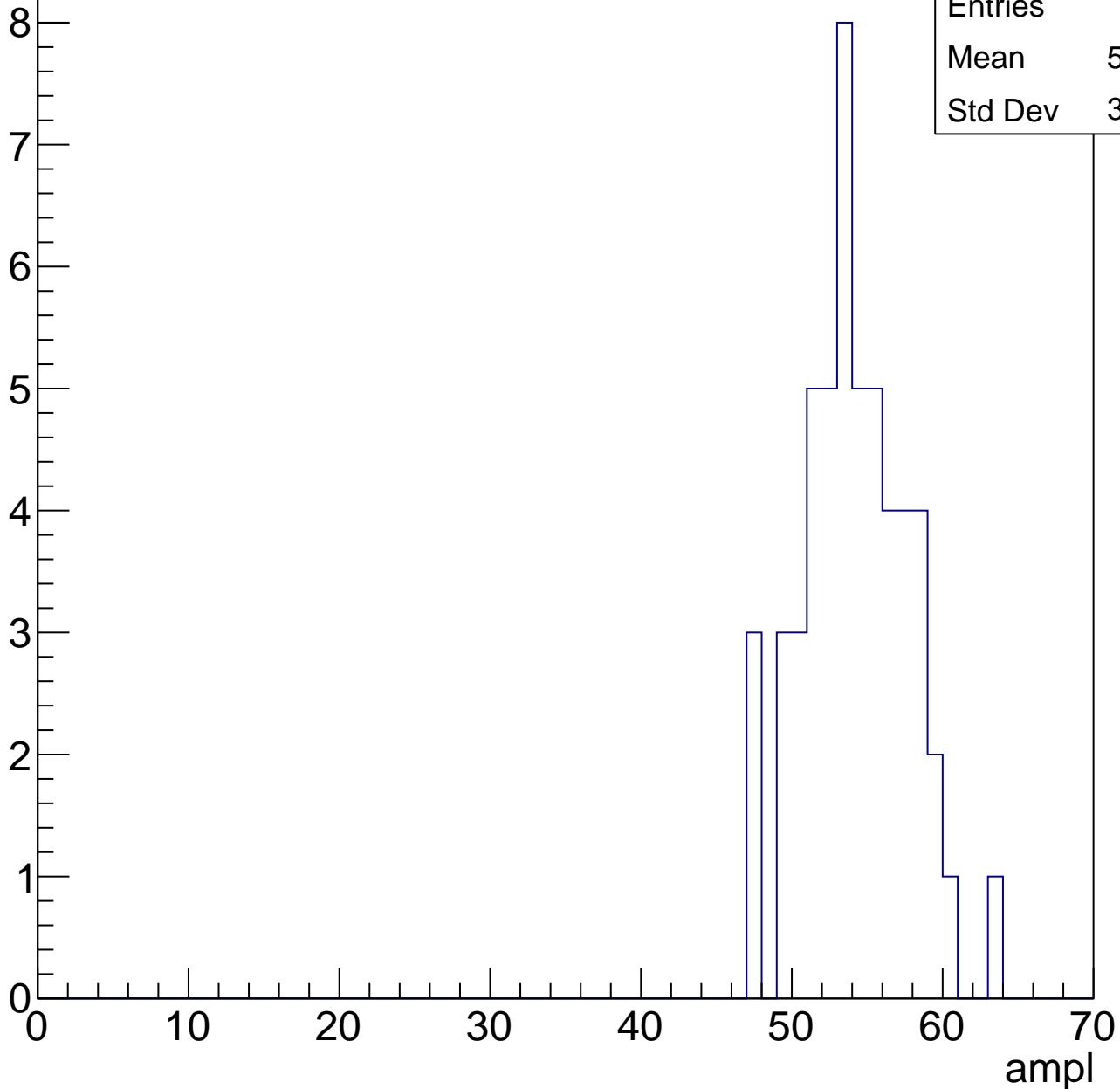


# B1L103S, U16-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

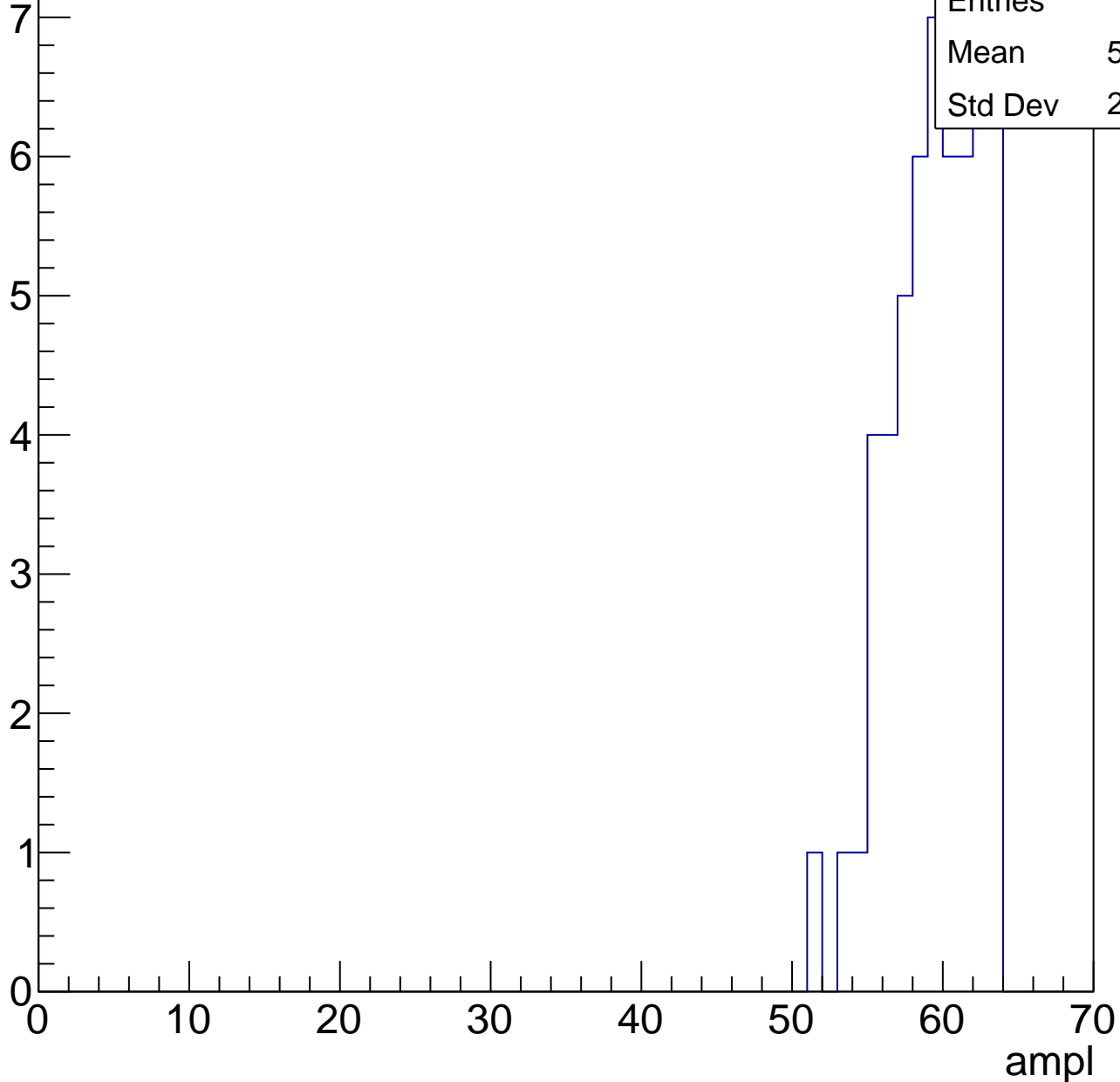
Entries	53
Mean	53.72
Std Dev	3.439



# B1L103S, U16-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

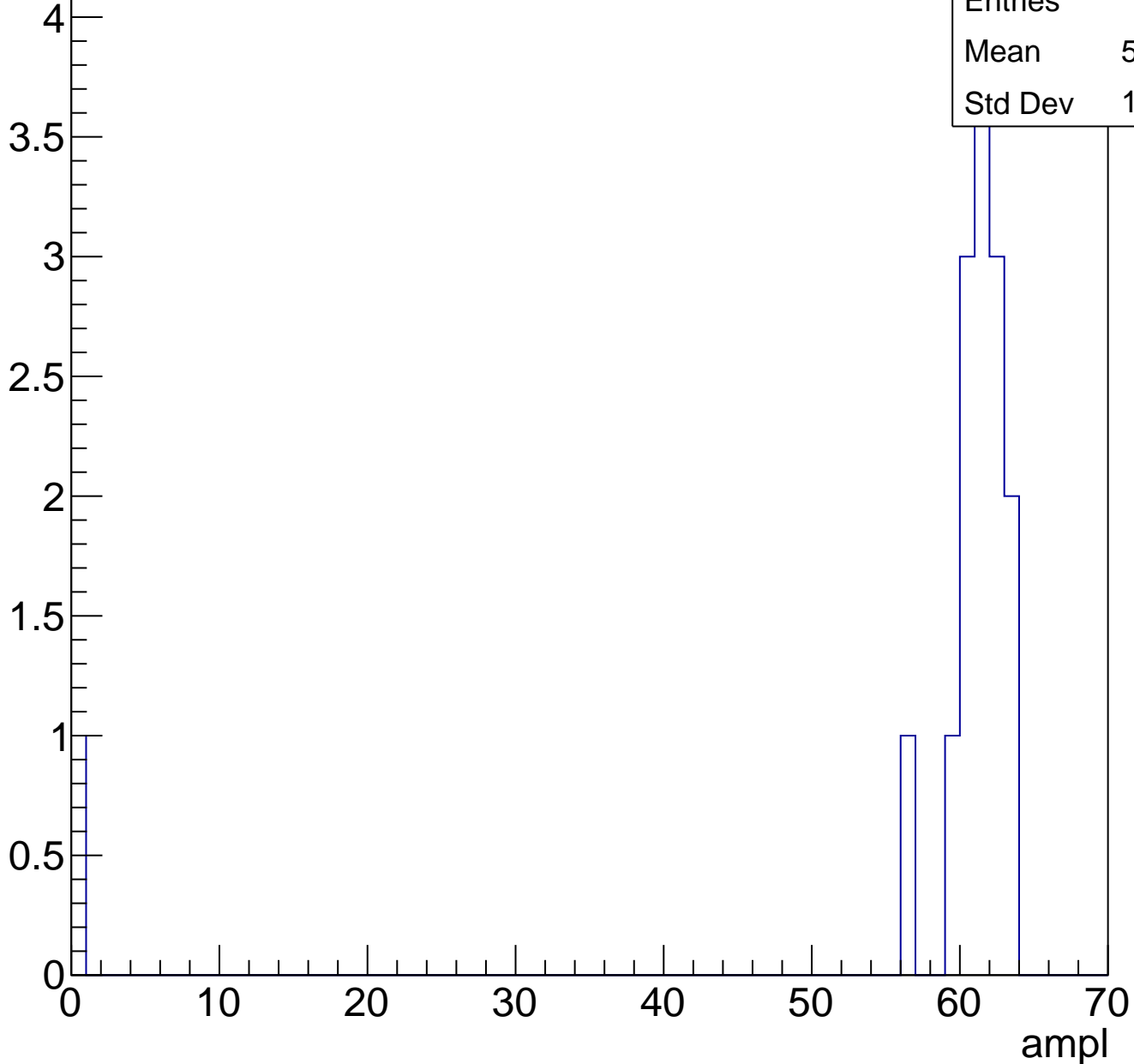
Entry



# B1L103S, U16-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U16-ch53, adc0

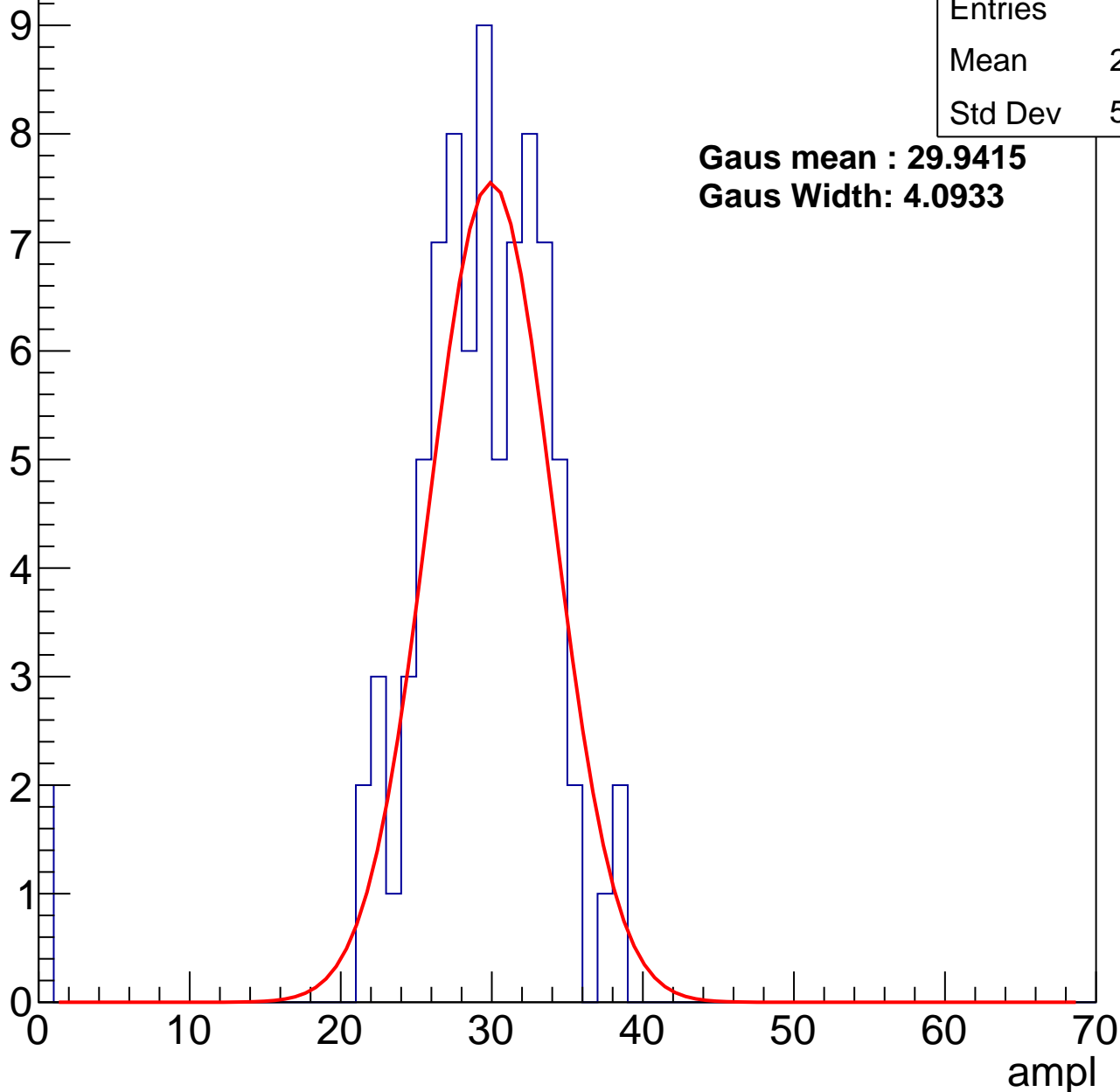
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	28.46
Std Dev	5.875

**Gaus mean : 29.9415**

**Gaus Width: 4.0933**



# B1L103S, U16-ch53, adc1

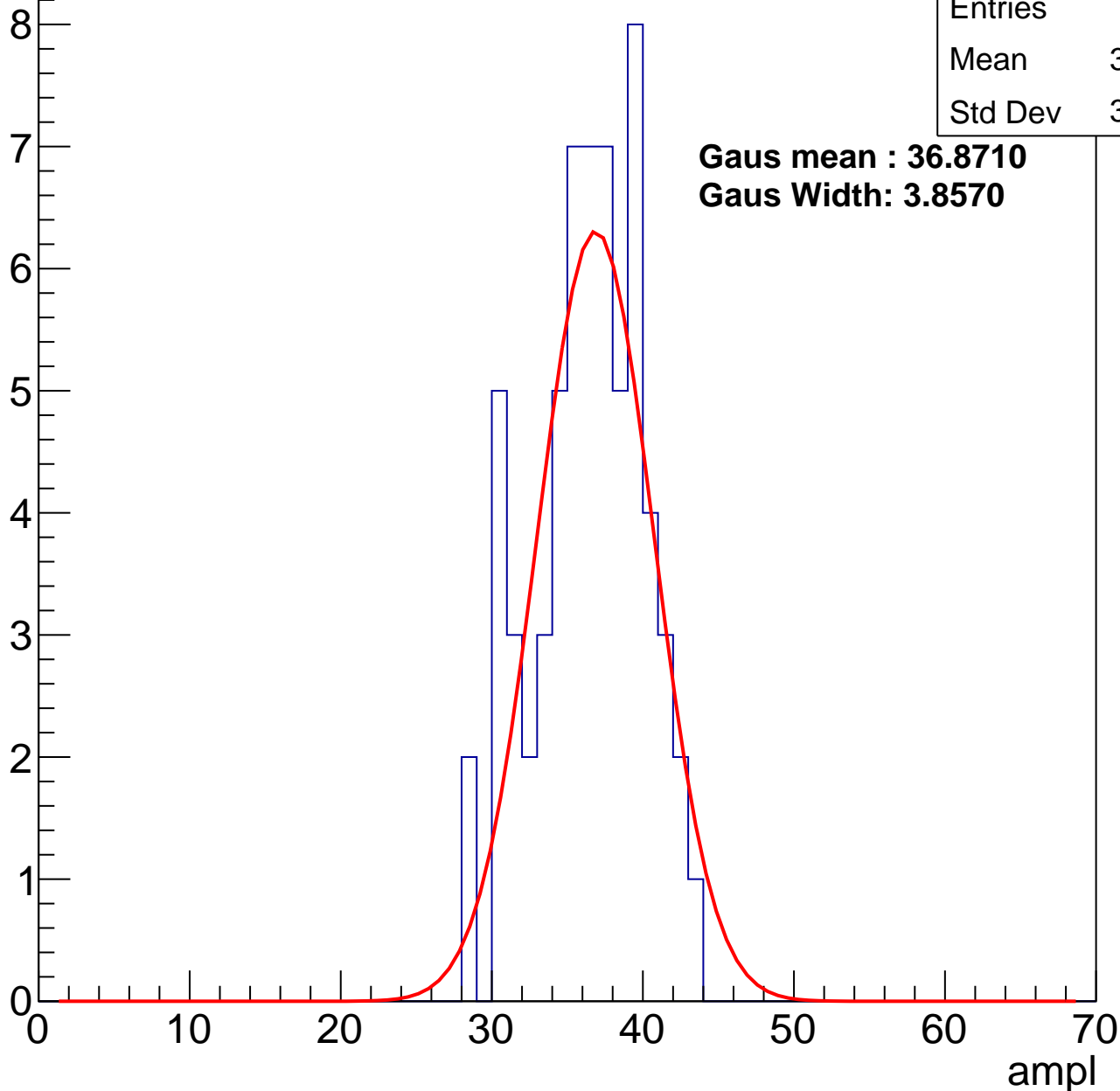
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	35.94
Std Dev	3.596

**Gaus mean : 36.8710**

**Gaus Width: 3.8570**



# B1L103S, U16-ch53, adc2

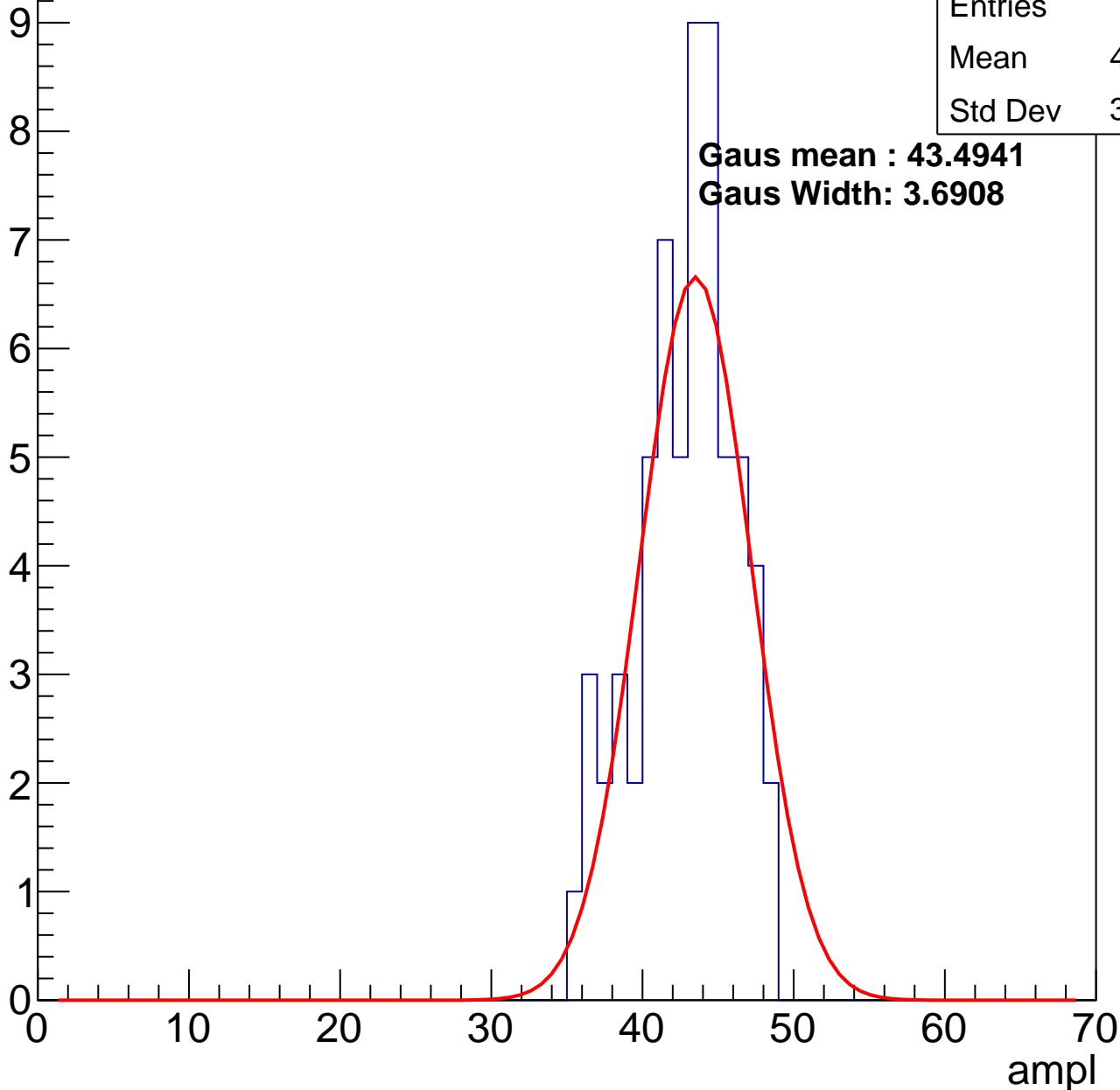
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	42.39
Std Dev	3.195

**Gaus mean : 43.4941**

**Gaus Width: 3.6908**

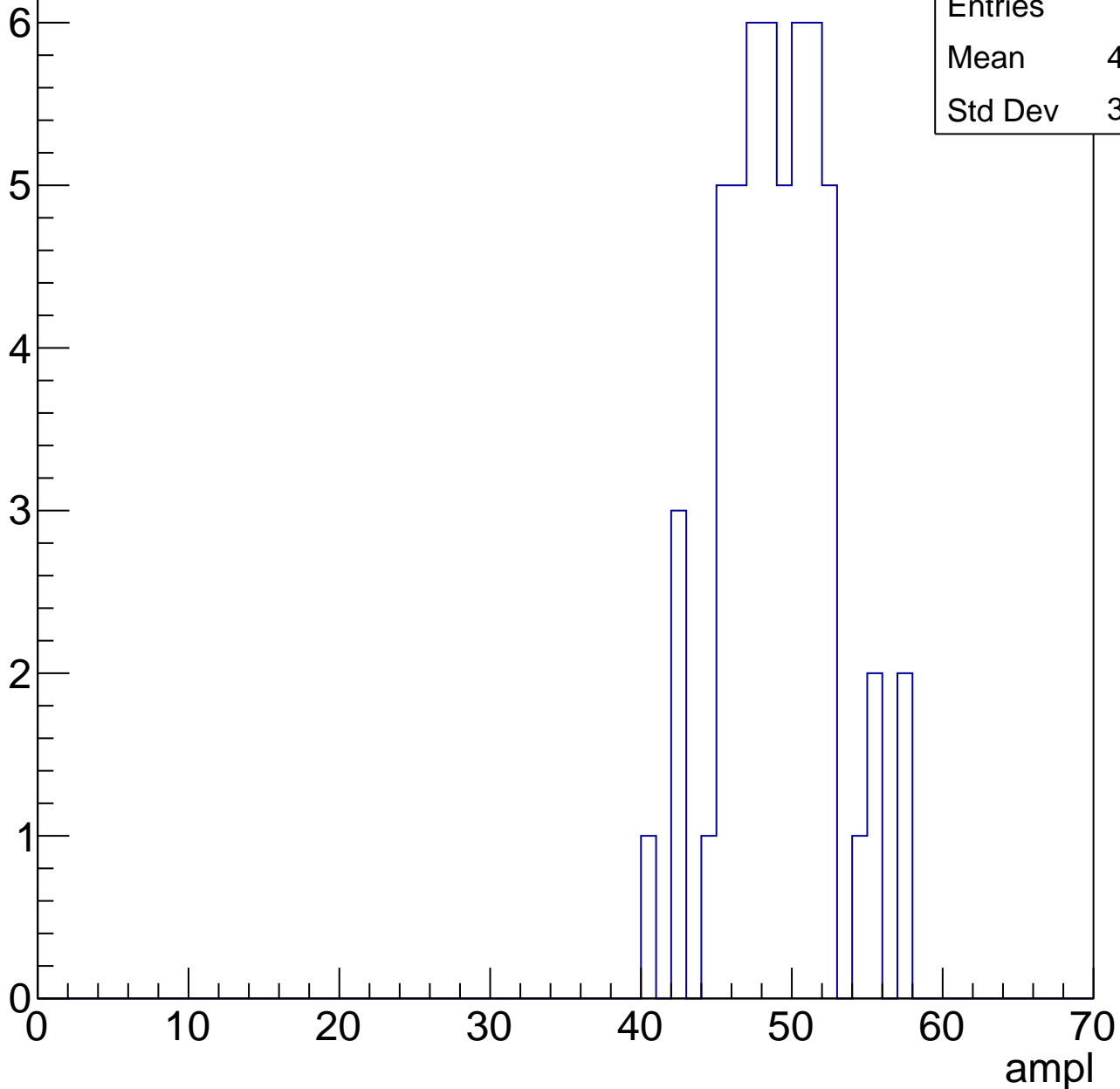


# B1L103S, U16-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	48.59
Std Dev	3.598

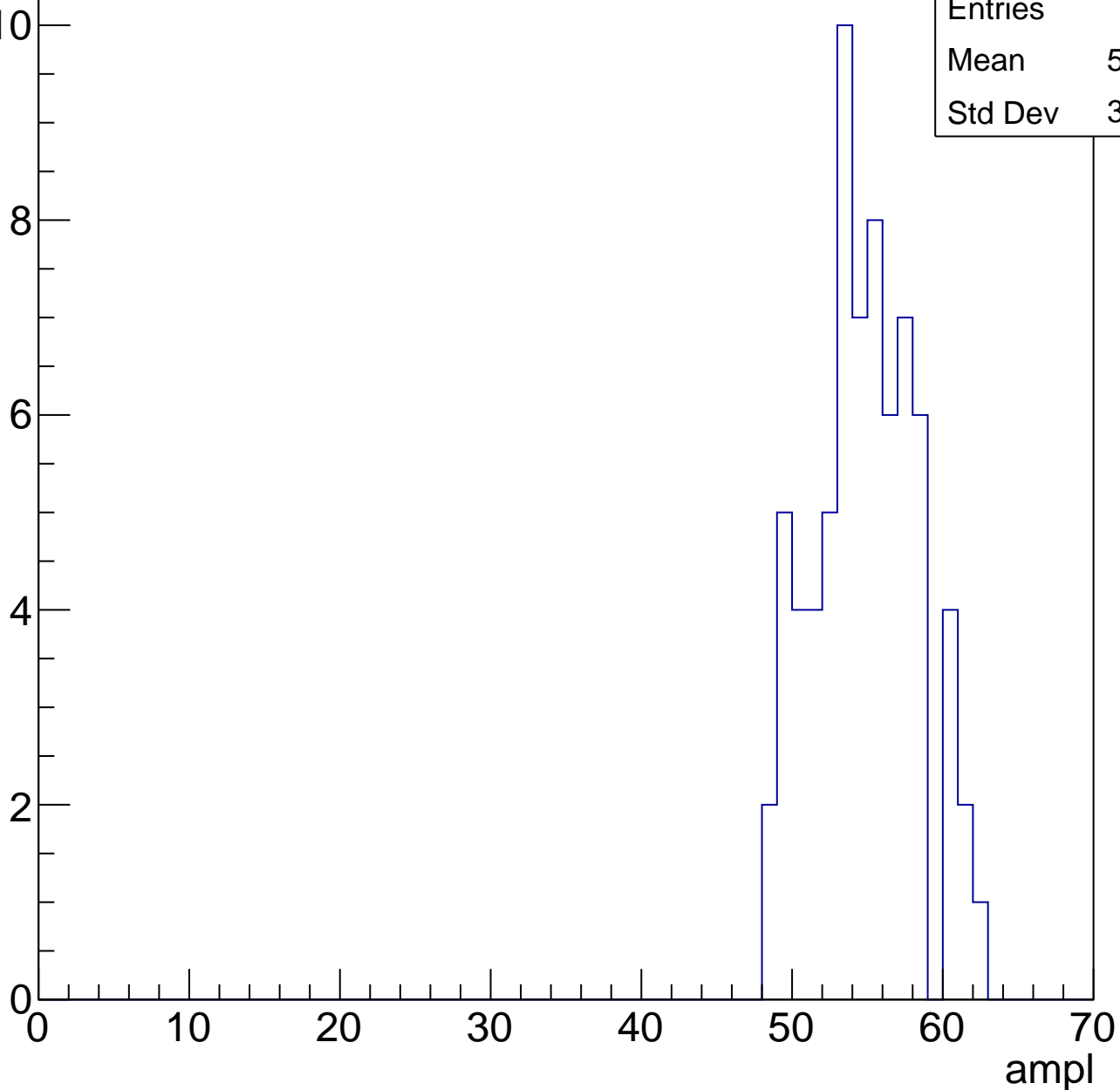


# B1L103S, U16-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	54.37
Std Dev	3.387

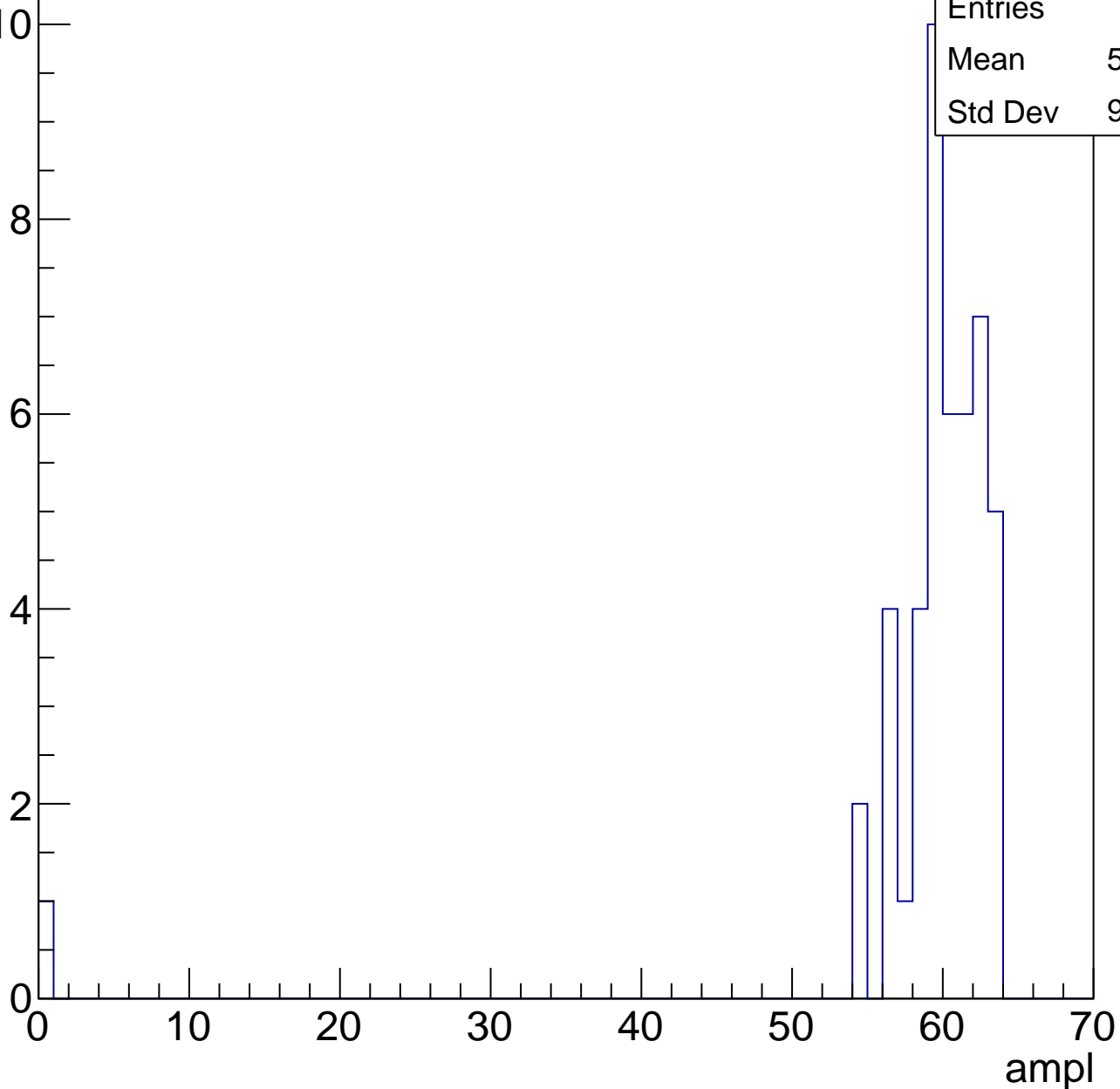


# B1L103S, U16-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	58.39
Std Dev	9.006

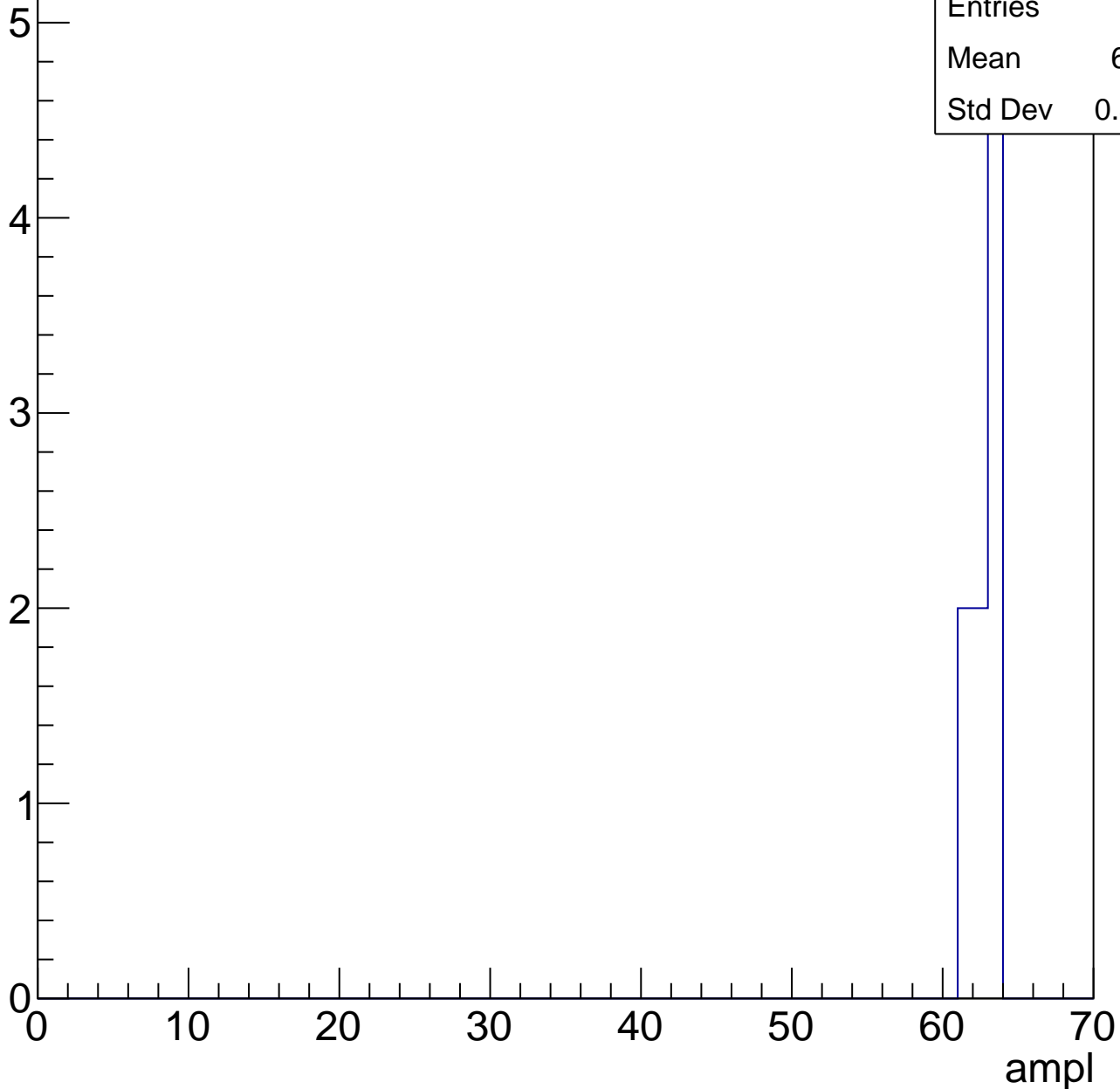


# B1L103S, U16-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	9
Mean	62.33
Std Dev	0.8165





# B1L103S, U16-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U16-ch54, adc0

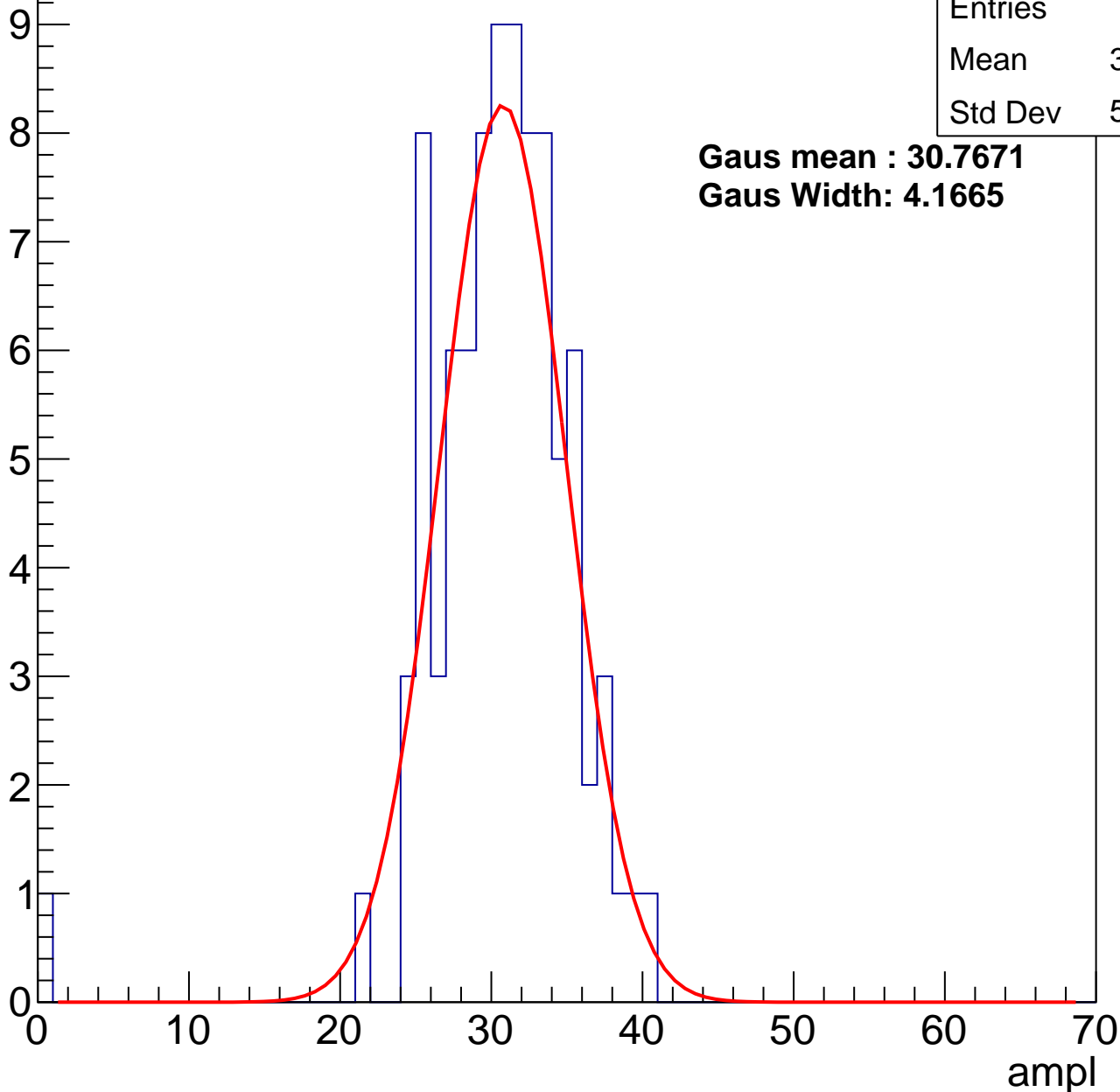
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	89
Mean	30.13
Std Dev	5.004

**Gaus mean : 30.7671**

**Gaus Width: 4.1665**



# B1L103S, U16-ch54, adc1

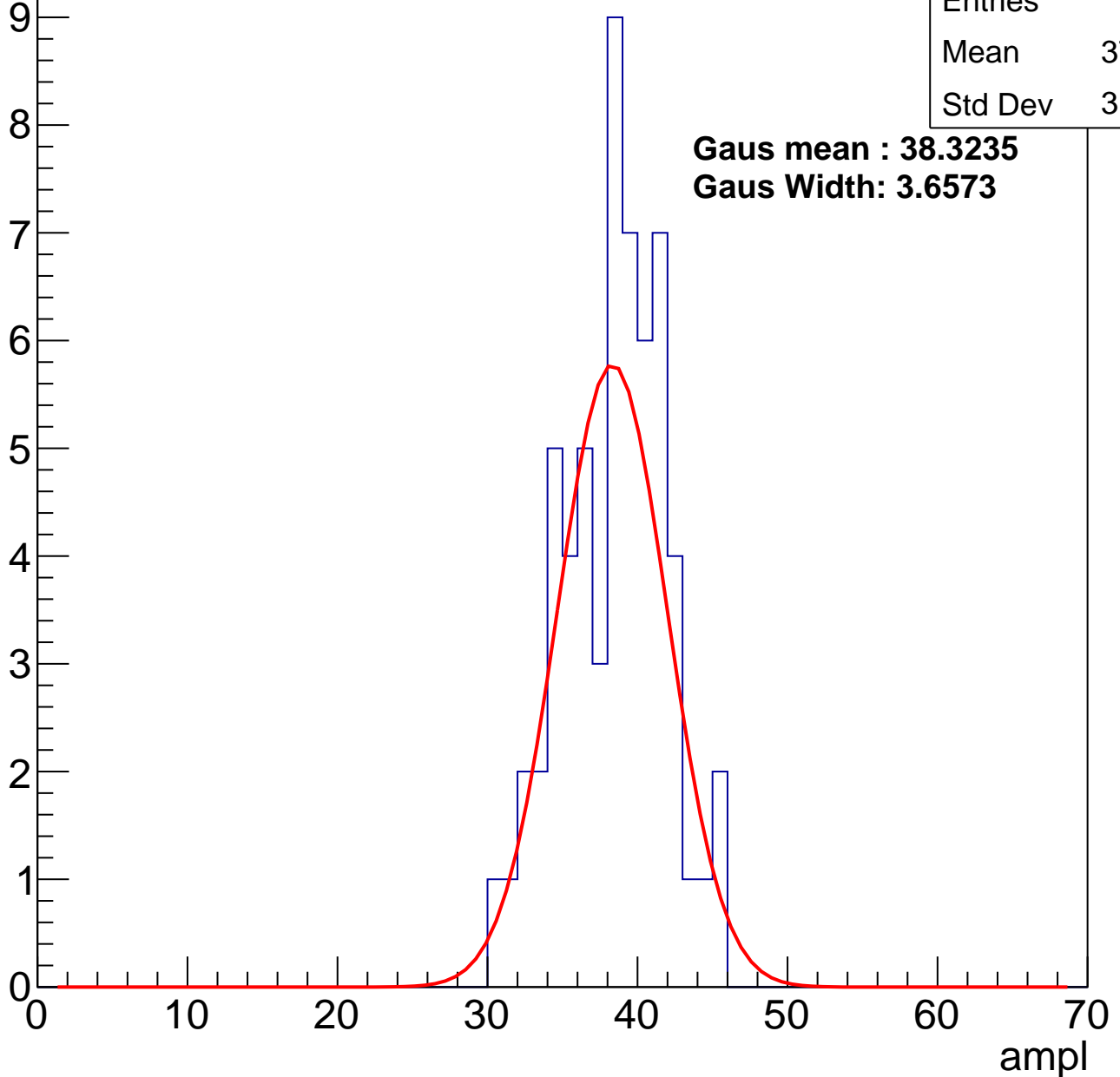
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	37.98
Std Dev	3.394

**Gaus mean : 38.3235**

**Gaus Width: 3.6573**



# B1L103S, U16-ch54, adc2

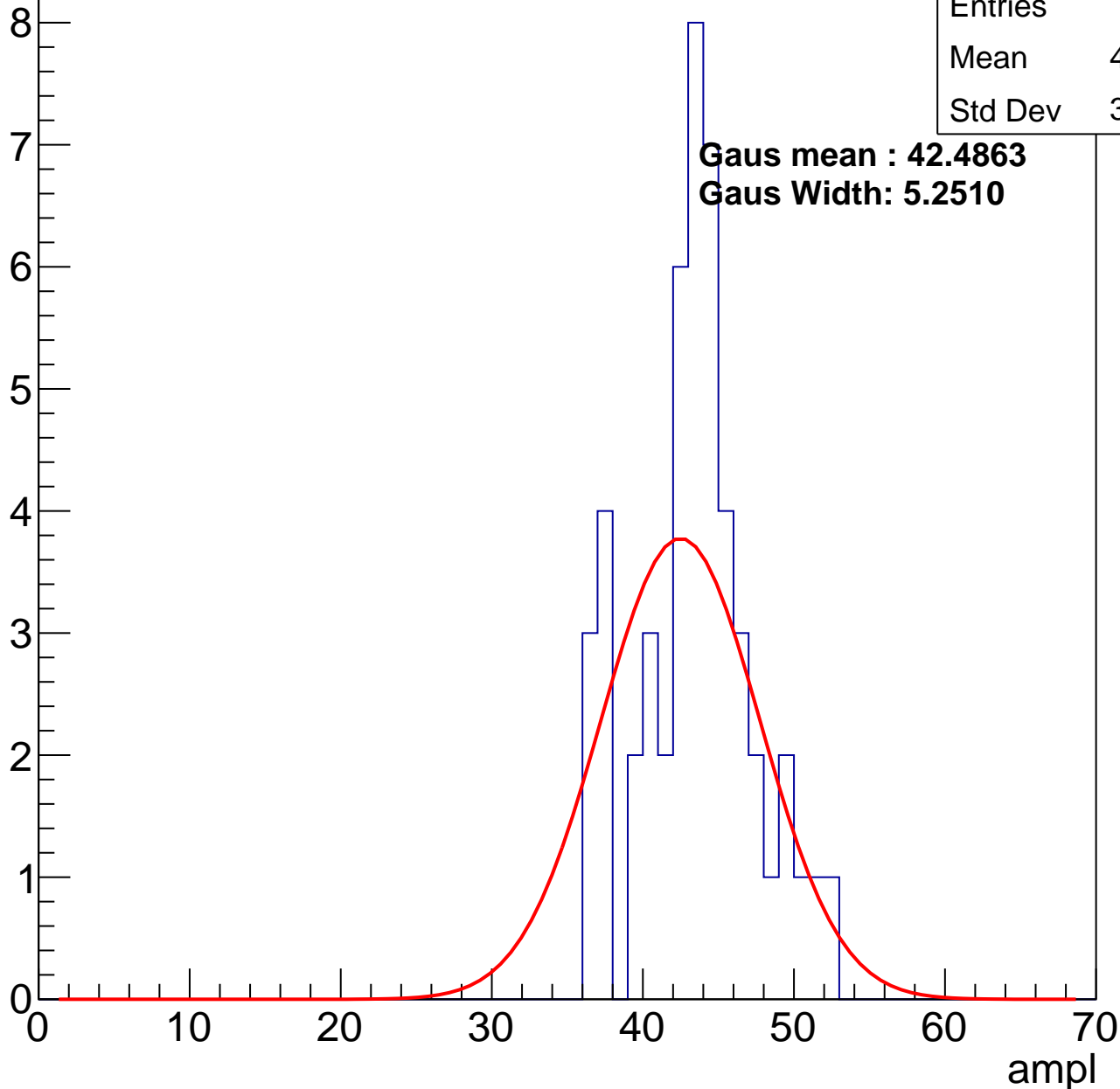
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	43.02
Std Dev	3.839

**Gaus mean : 42.4863**

**Gaus Width: 5.2510**

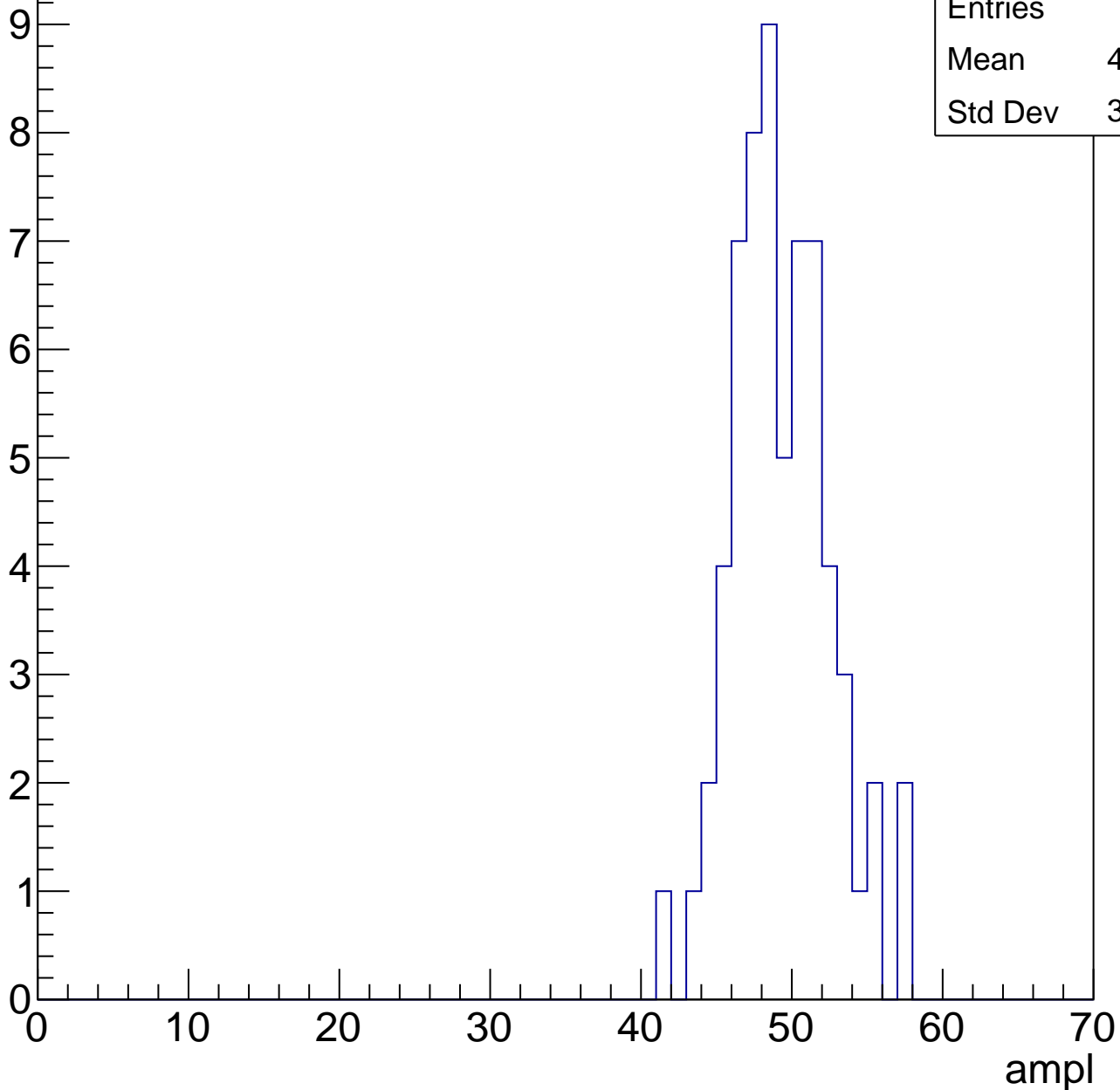


# B1L103S, U16-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	48.87
Std Dev	3.239

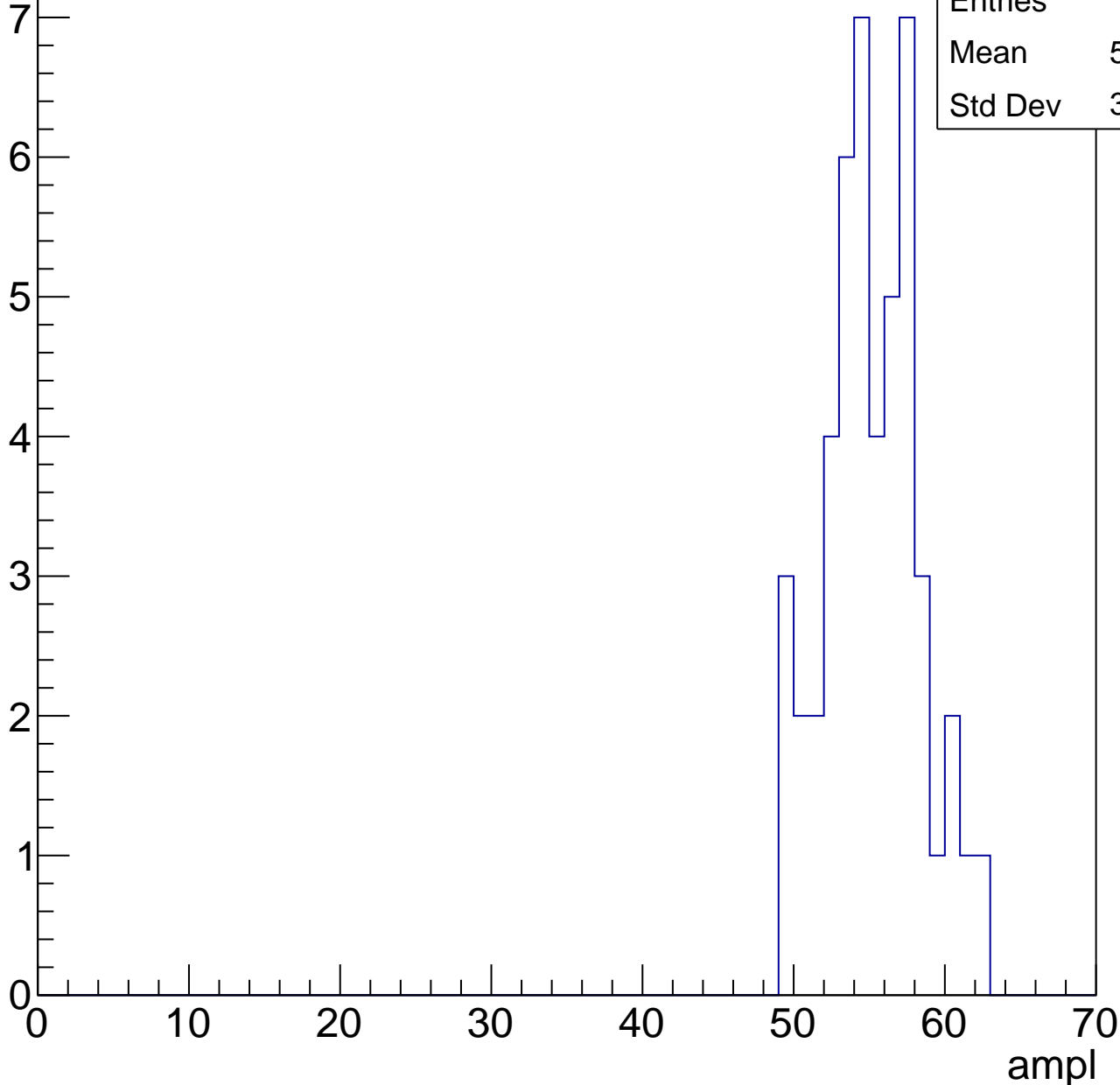


# B1L103S, U16-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

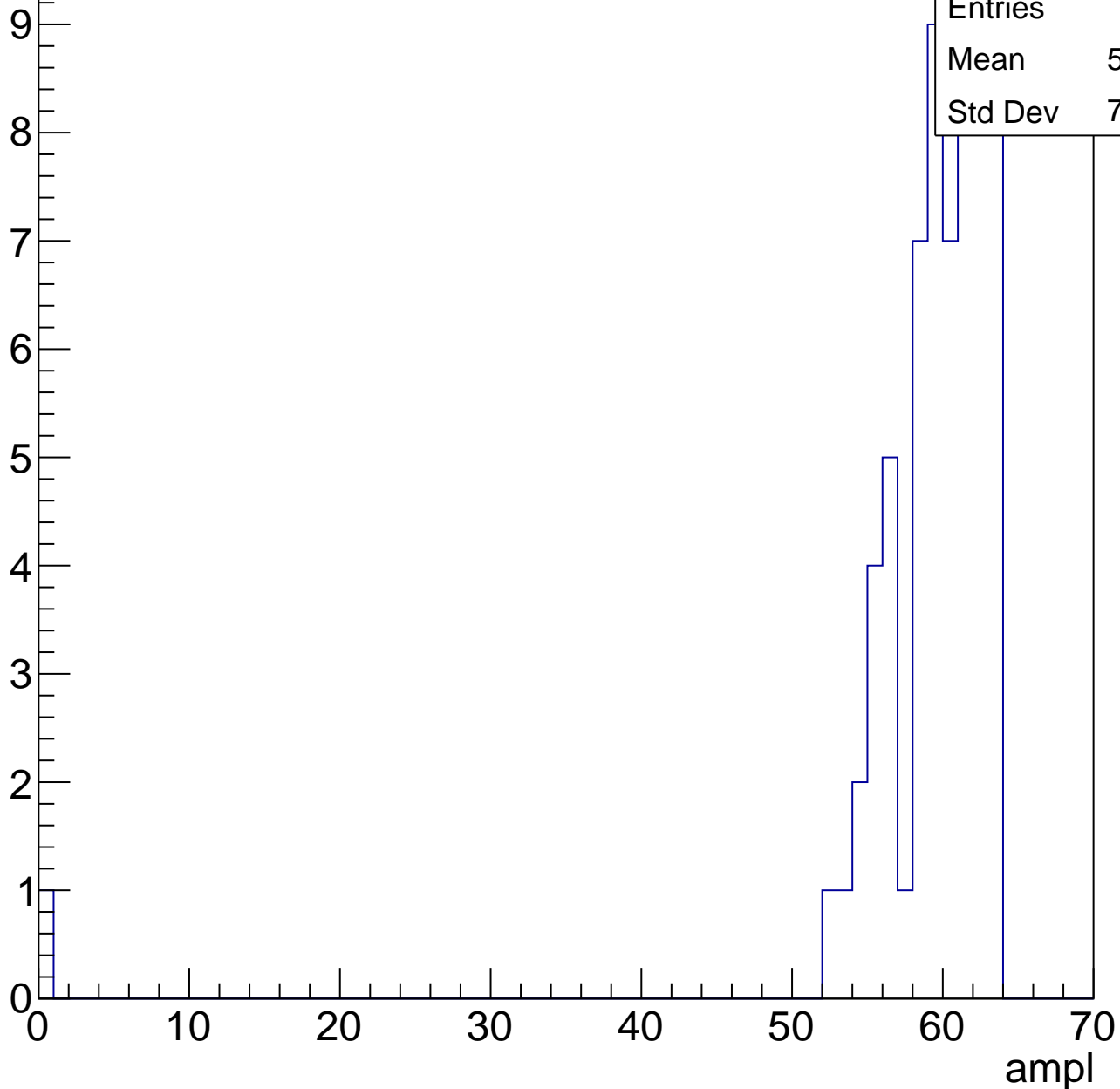
Entries	48
Mean	54.75
Std Dev	3.112



# B1L103S, U16-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch55, adc0

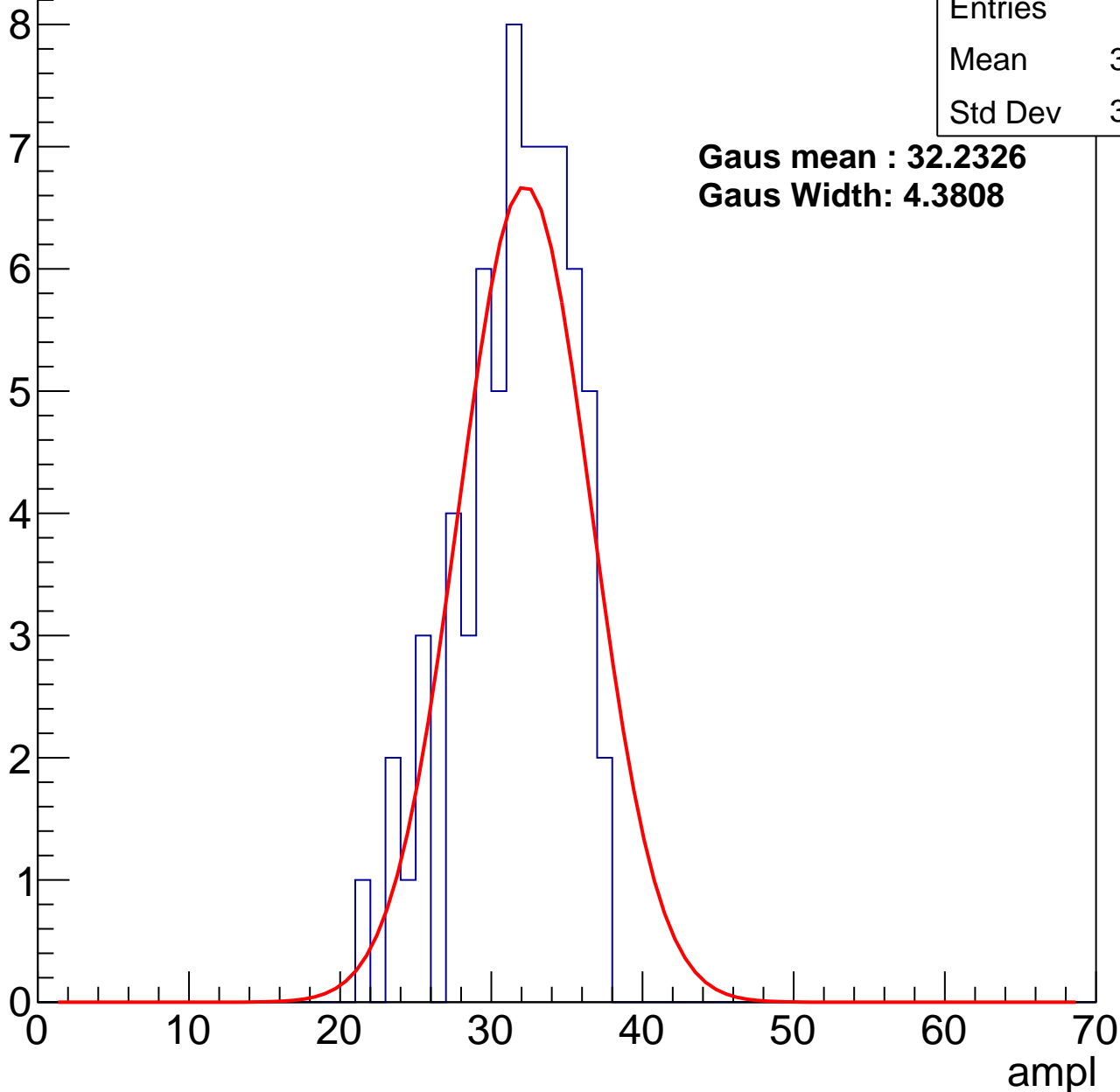
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	31.15
Std Dev	3.654

**Gaus mean : 32.2326**

**Gaus Width: 4.3808**



# B1L103S, U16-ch55, adc1

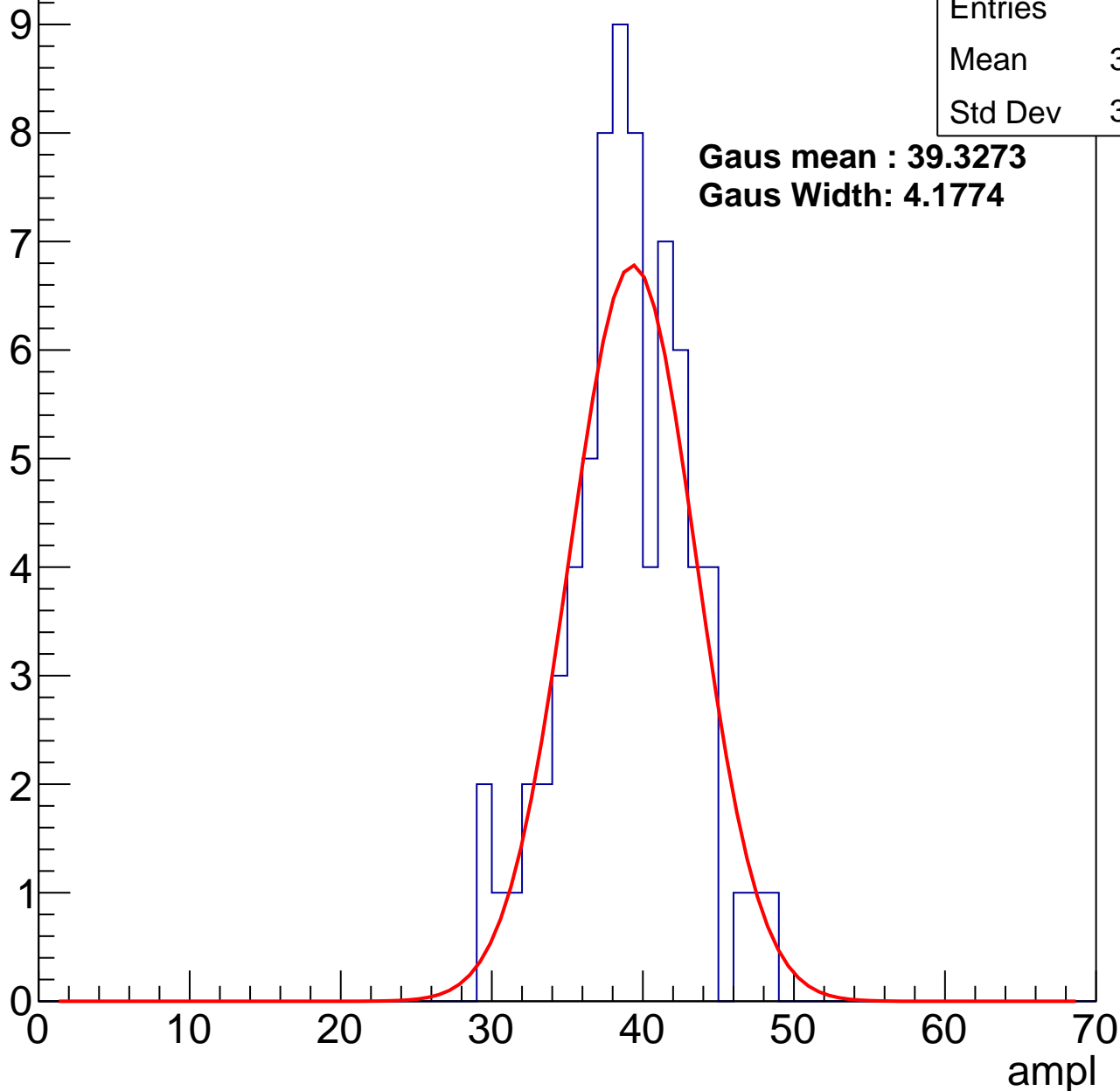
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	38.48
Std Dev	3.994

**Gaus mean : 39.3273**

**Gaus Width: 4.1774**



# B1L103S, U16-ch55, adc2

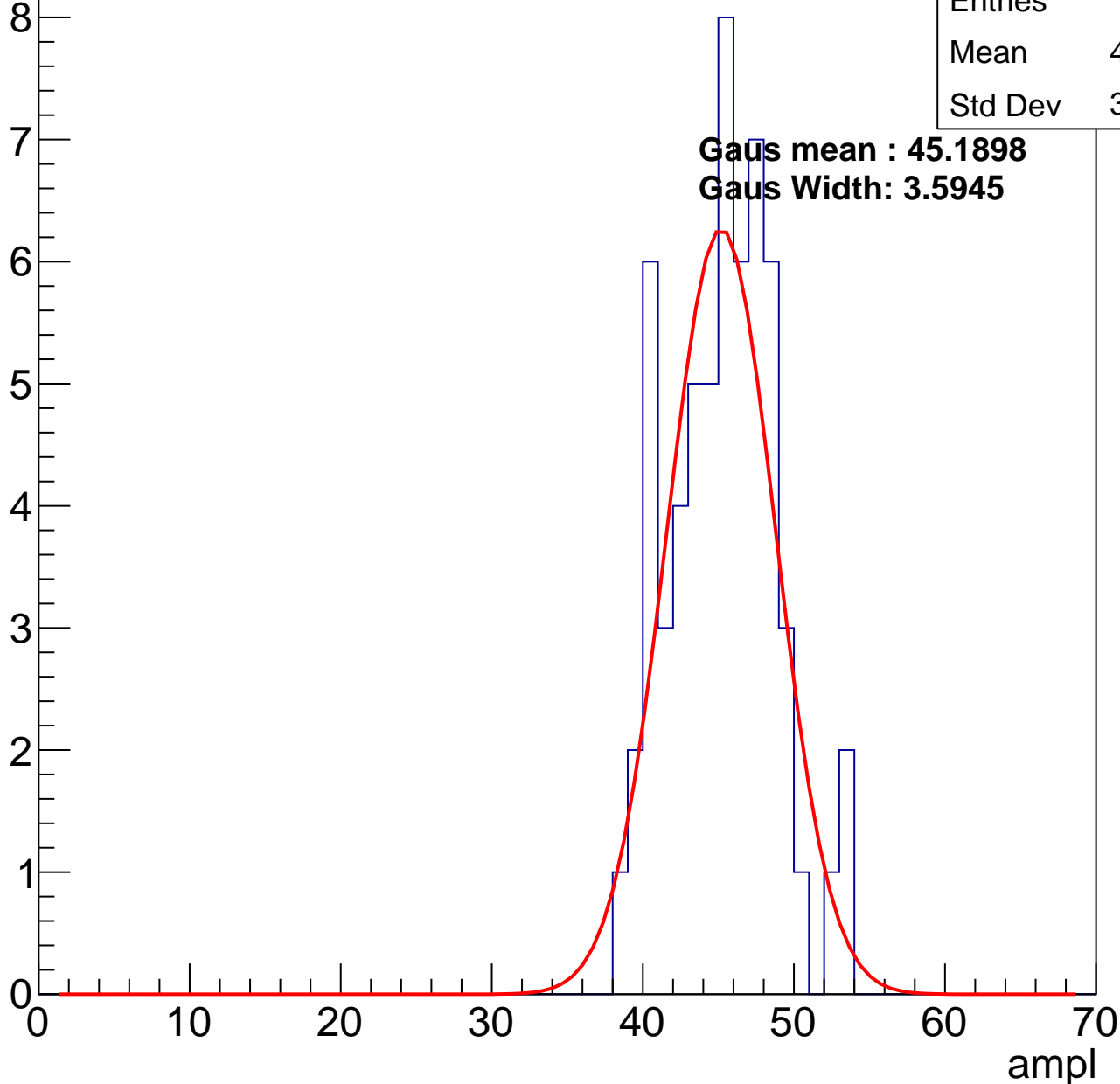
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	44.83
Std Dev	3.455

**Gaus mean : 45.1898**

**Gaus Width: 3.5945**

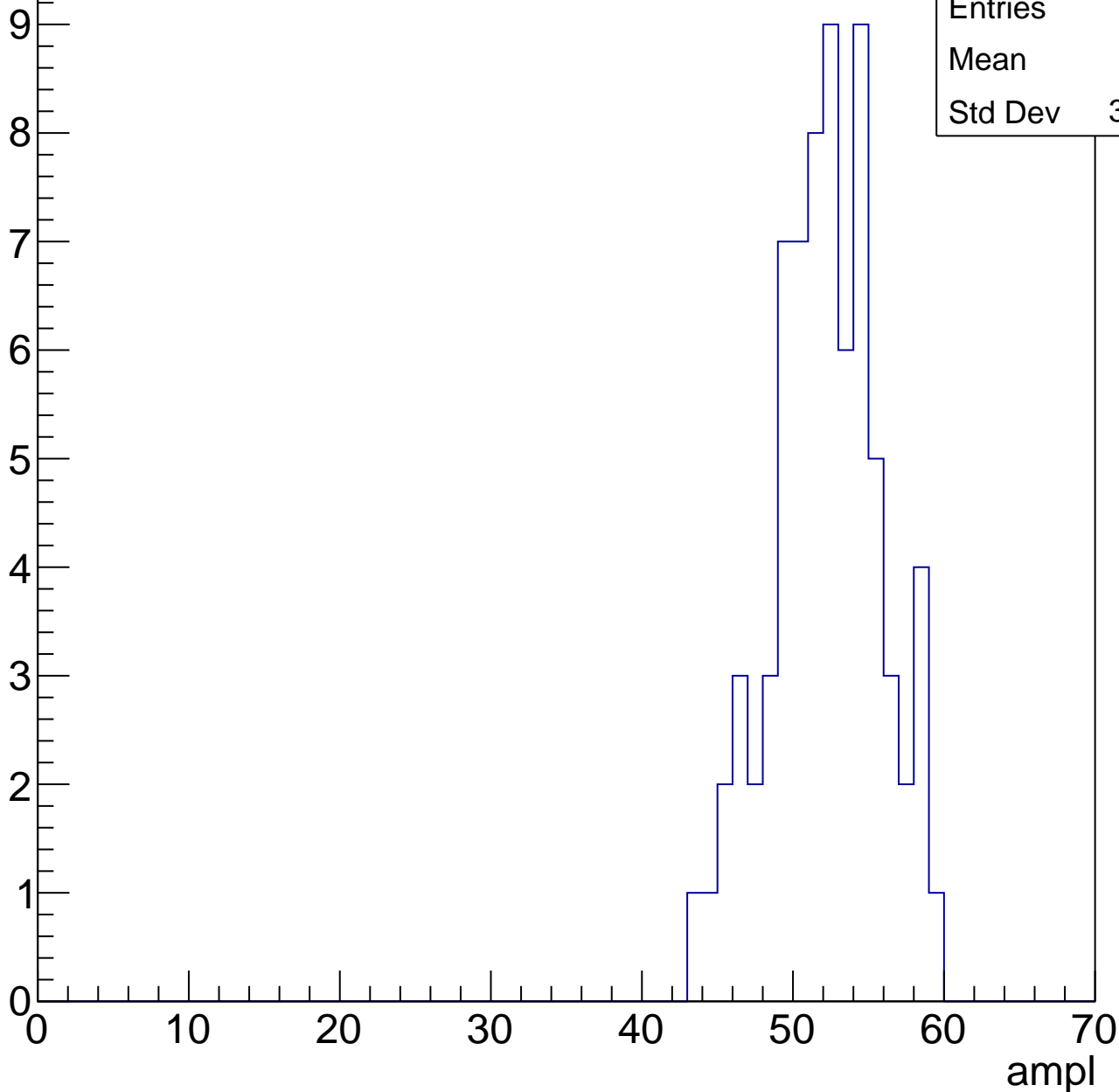


# B1L103S, U16-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	51.7
Std Dev	3.549

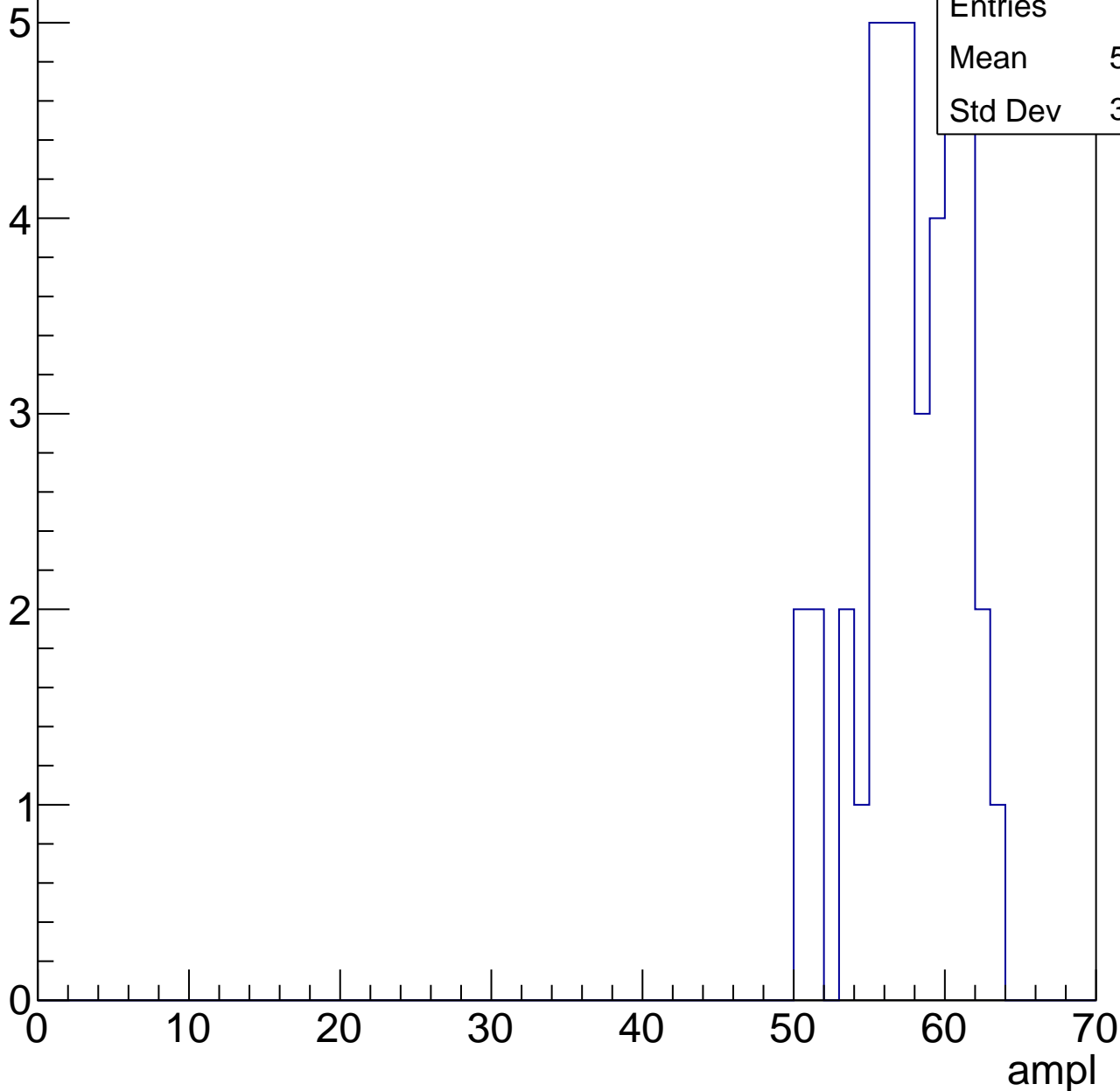


# B1L103S, U16-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	42
Mean	57.24
Std Dev	3.322

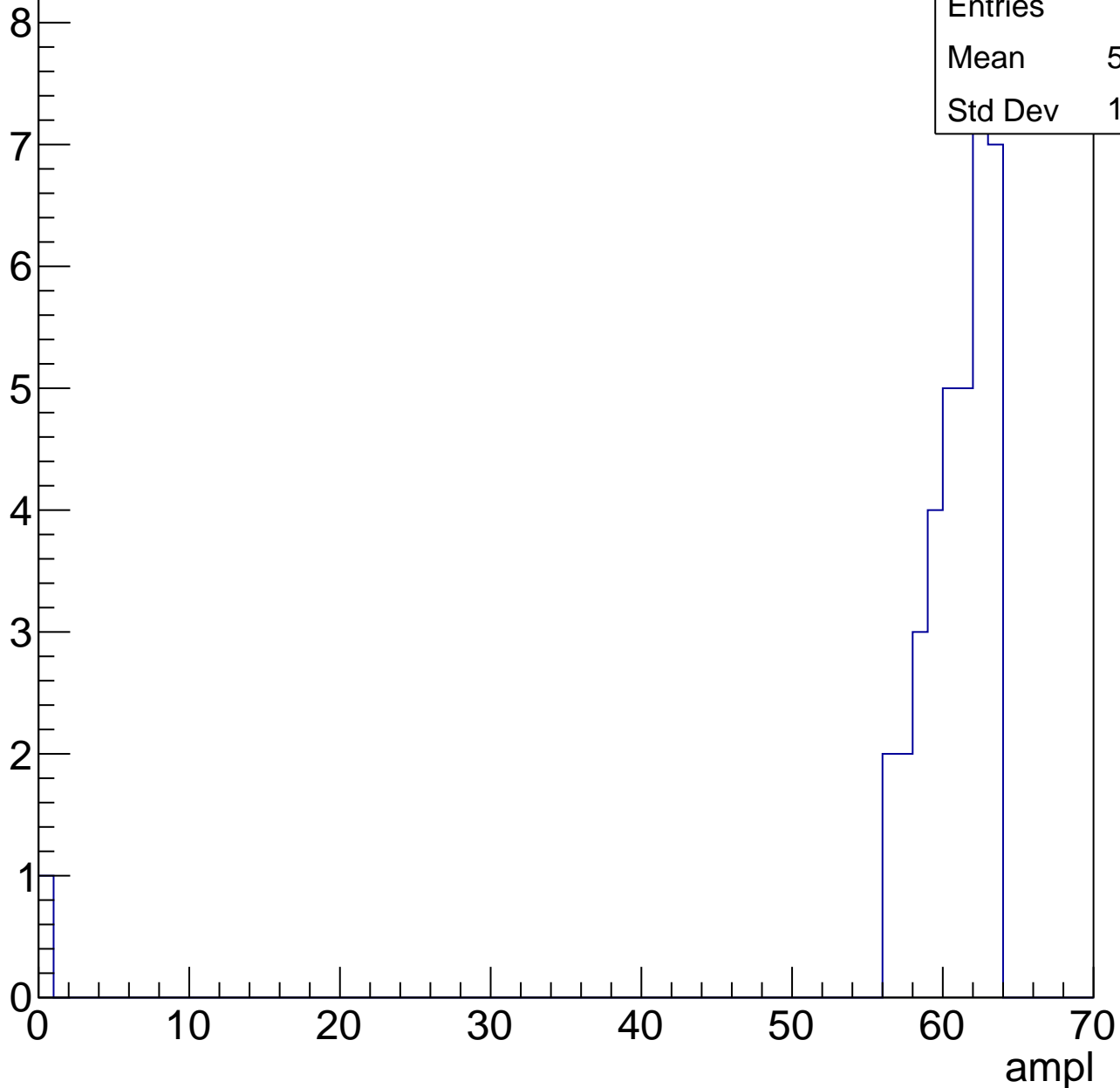


# B1L103S, U16-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

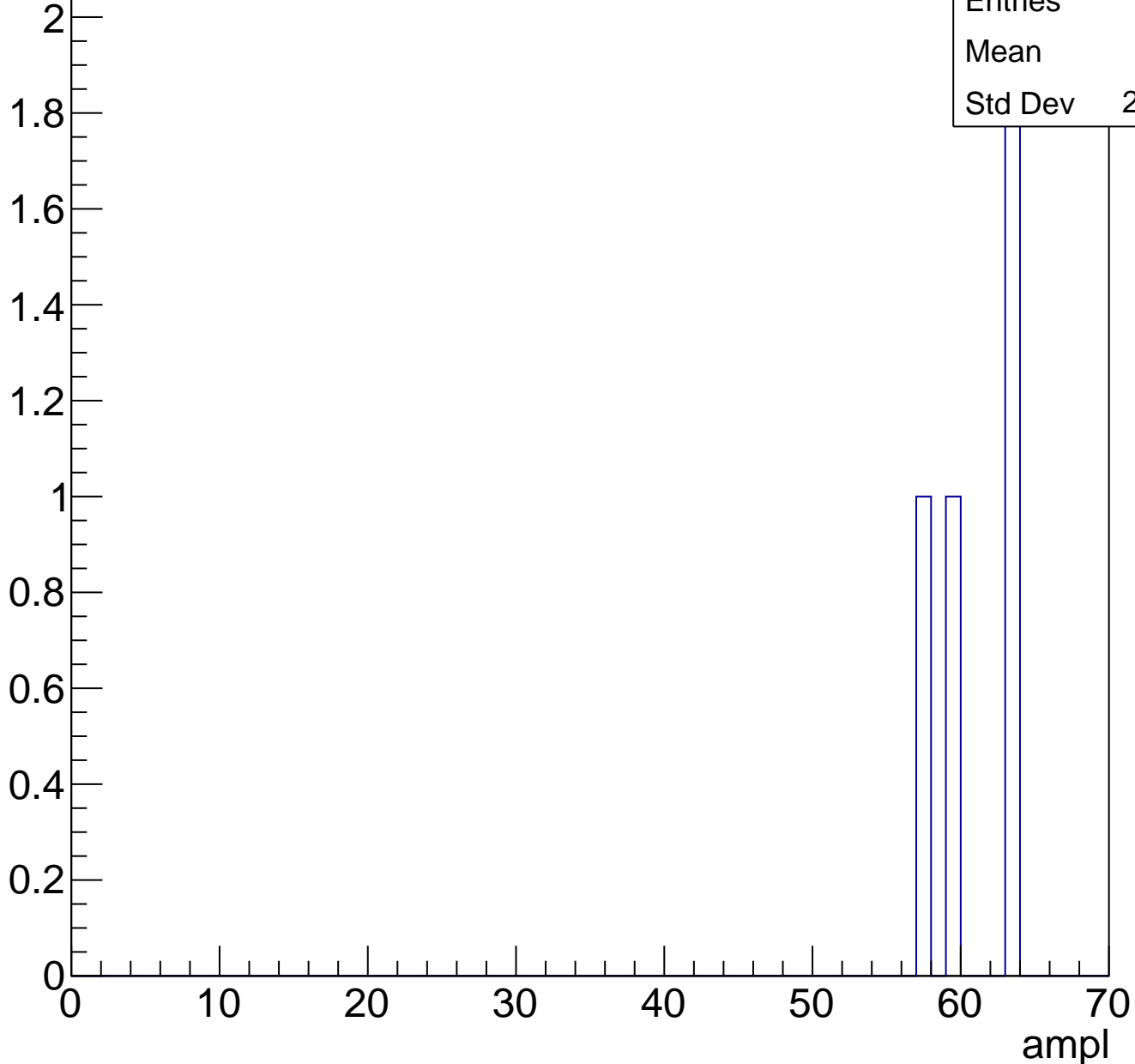
Entries	37
Mean	58.86
Std Dev	10.02



# B1L103S, U16-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	4
Mean	60.5
Std Dev	2.598



# B1L103S, U16-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch56, adc0

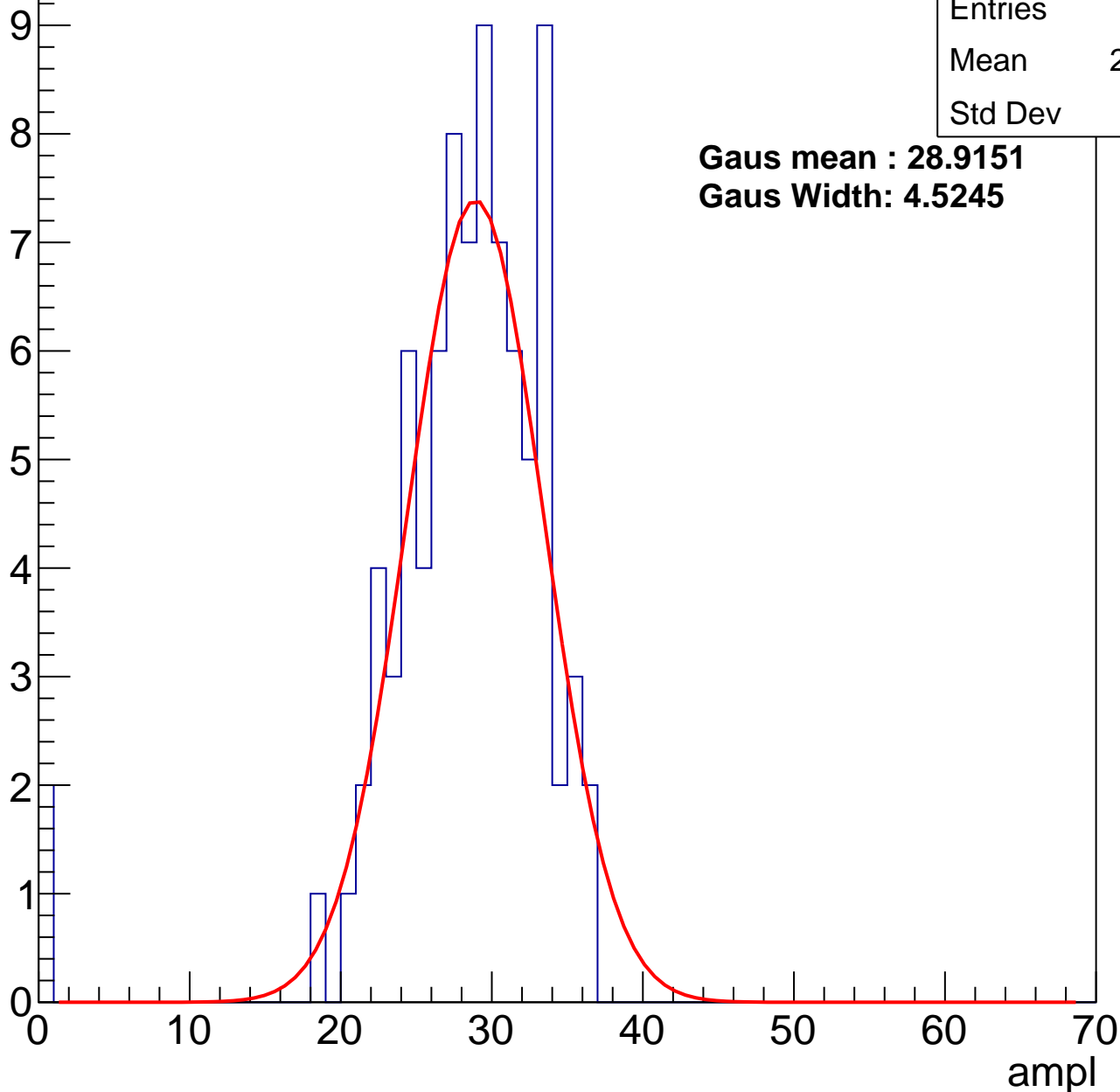
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	87
Mean	27.68
Std Dev	5.82

**Gaus mean : 28.9151**

**Gaus Width: 4.5245**



# B1L103S, U16-ch56, adc1

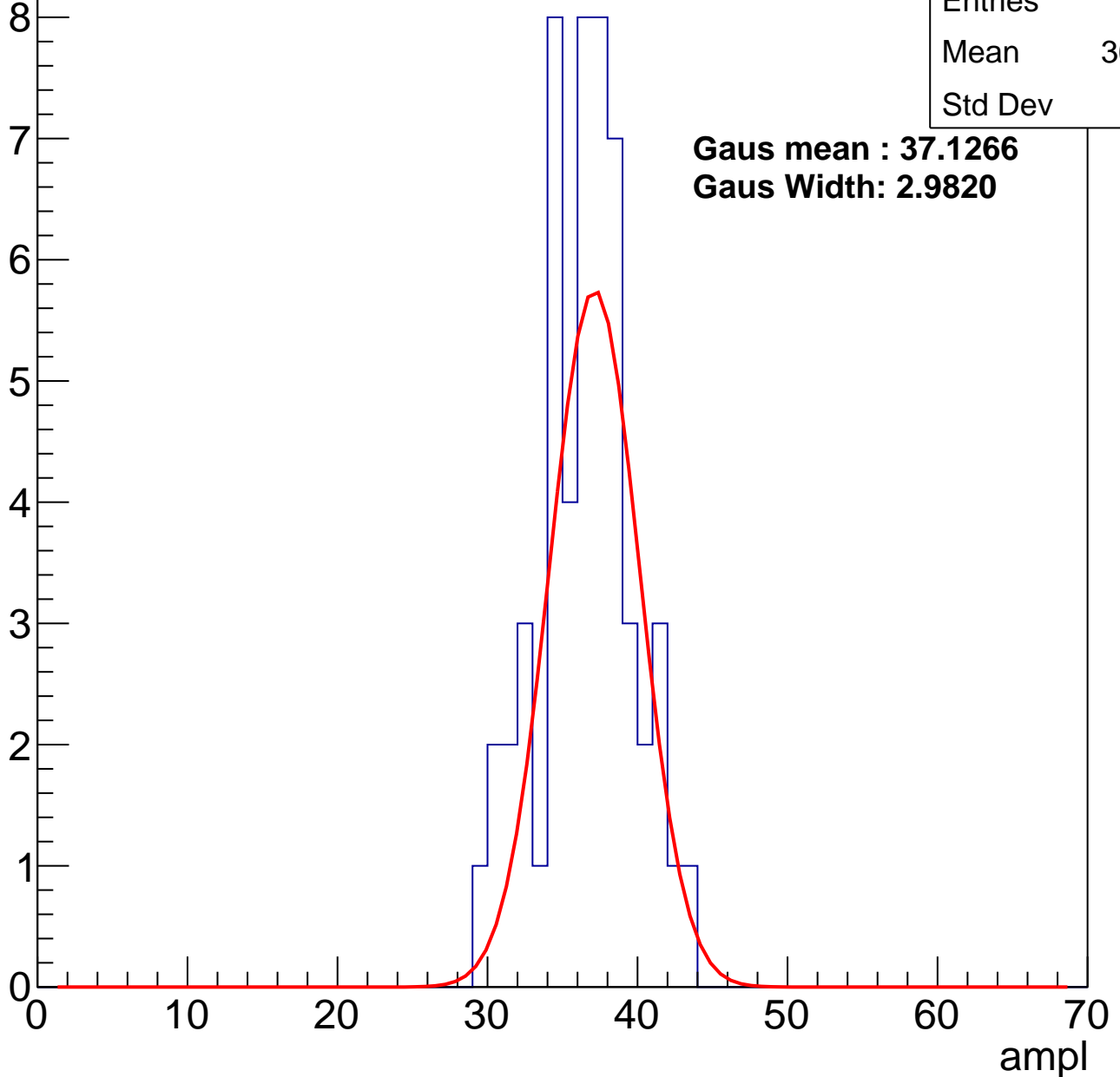
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	36.06
Std Dev	3.1

**Gaus mean : 37.1266**

**Gaus Width: 2.9820**



# B1L103S, U16-ch56, adc2

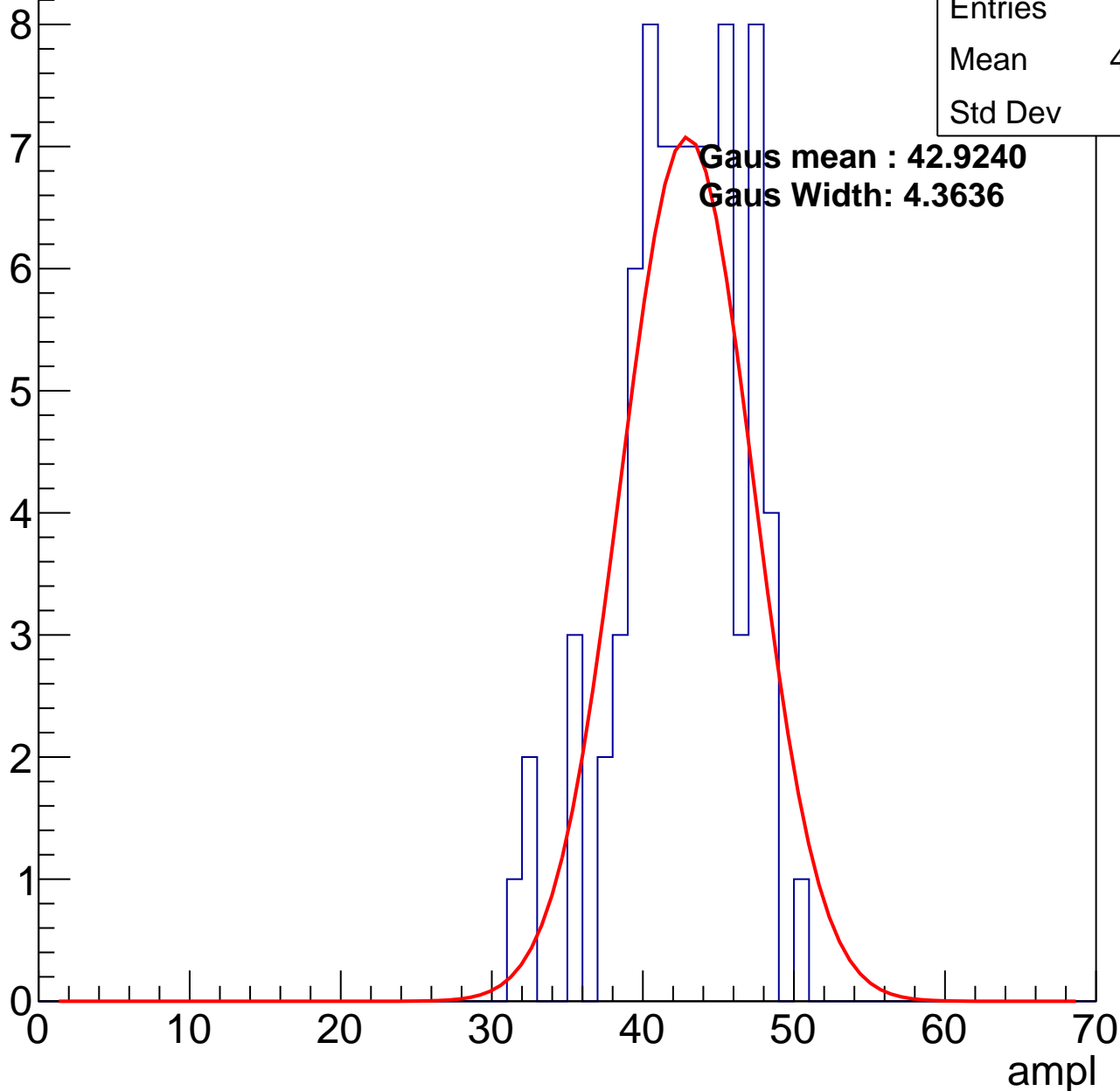
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	42.18
Std Dev	3.98

**Gaus mean : 42.9240**

**Gaus Width: 4.3636**

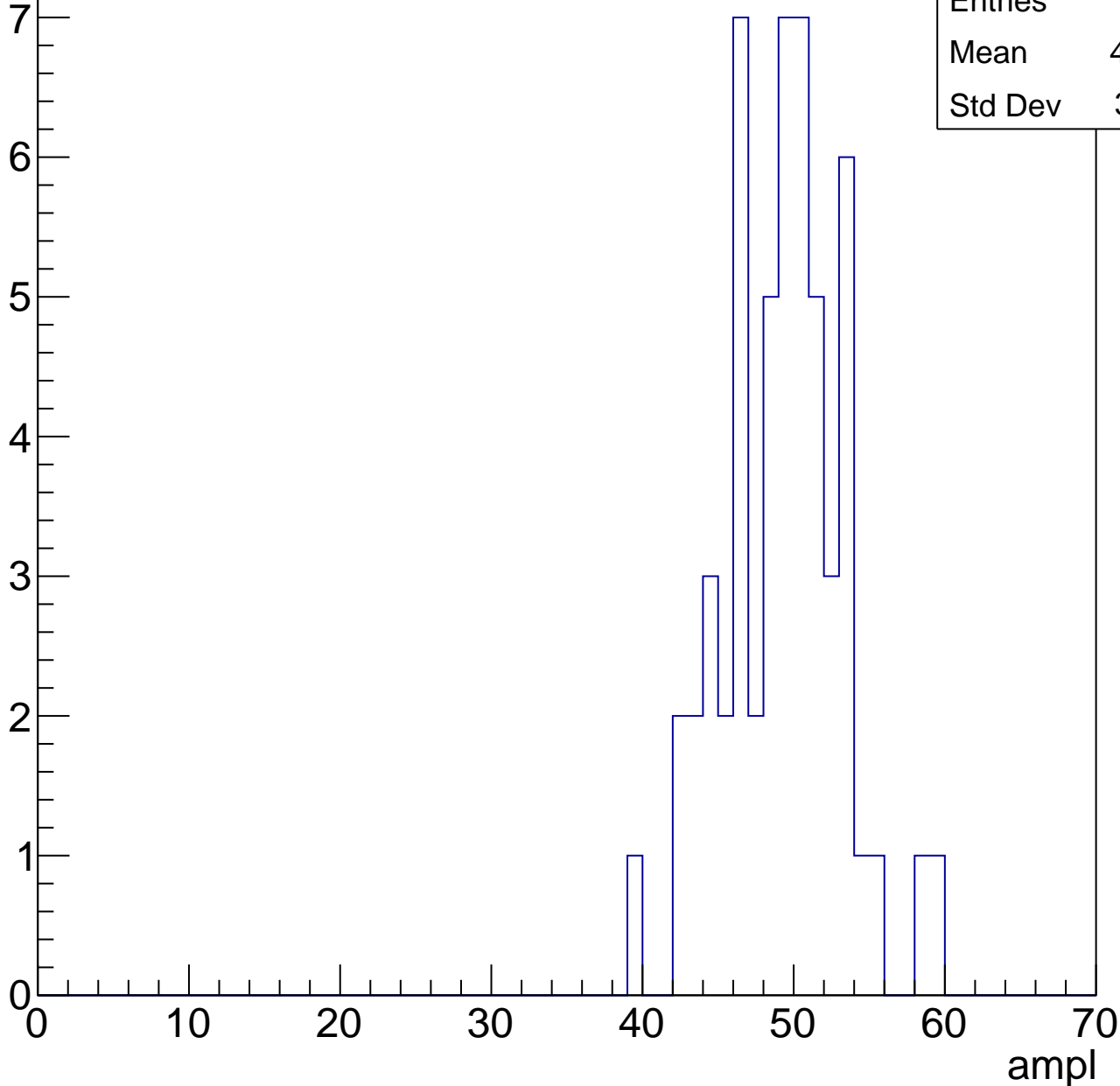


# B1L103S, U16-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	48.84
Std Dev	3.881

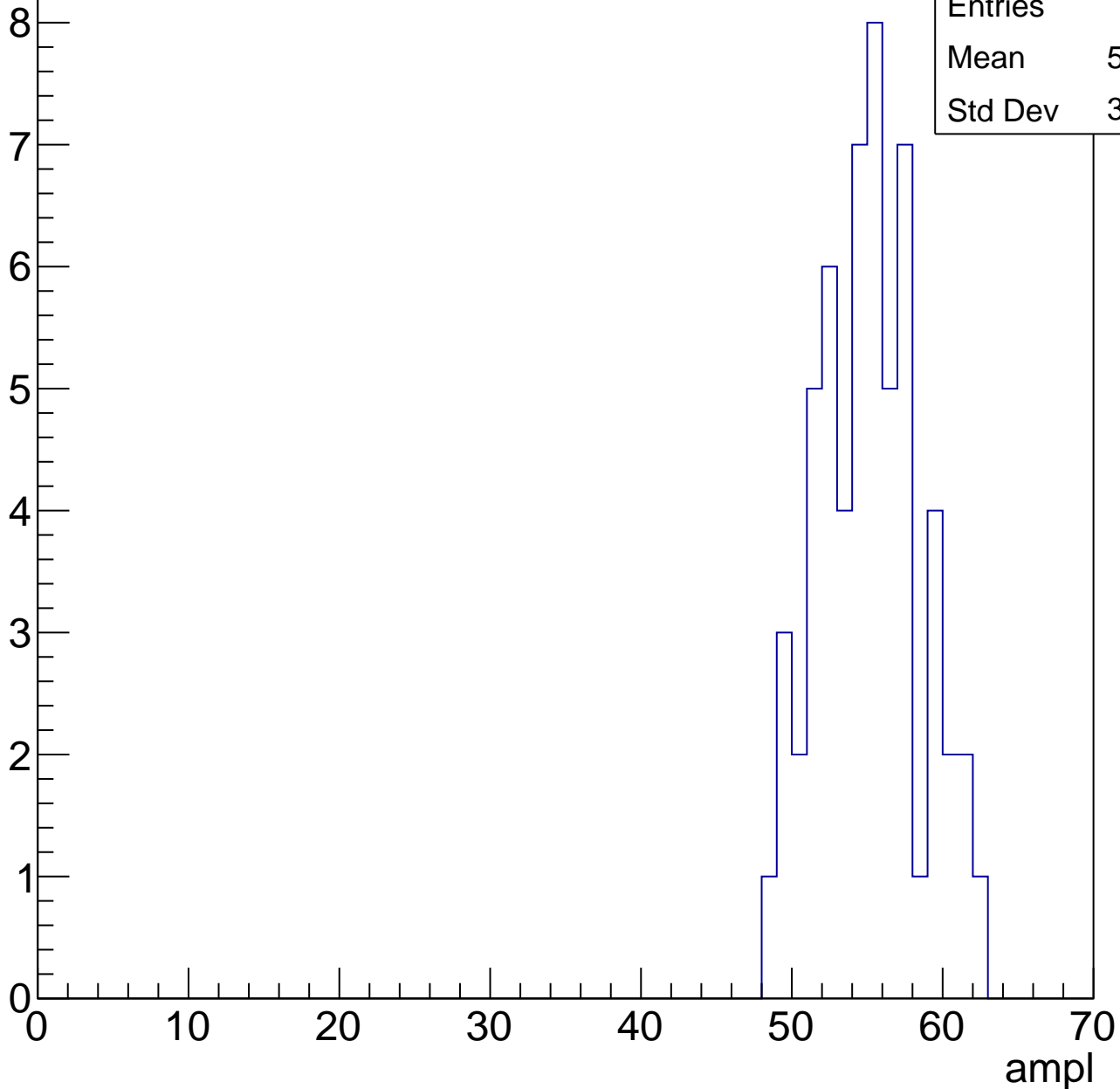


# B1L103S, U16-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

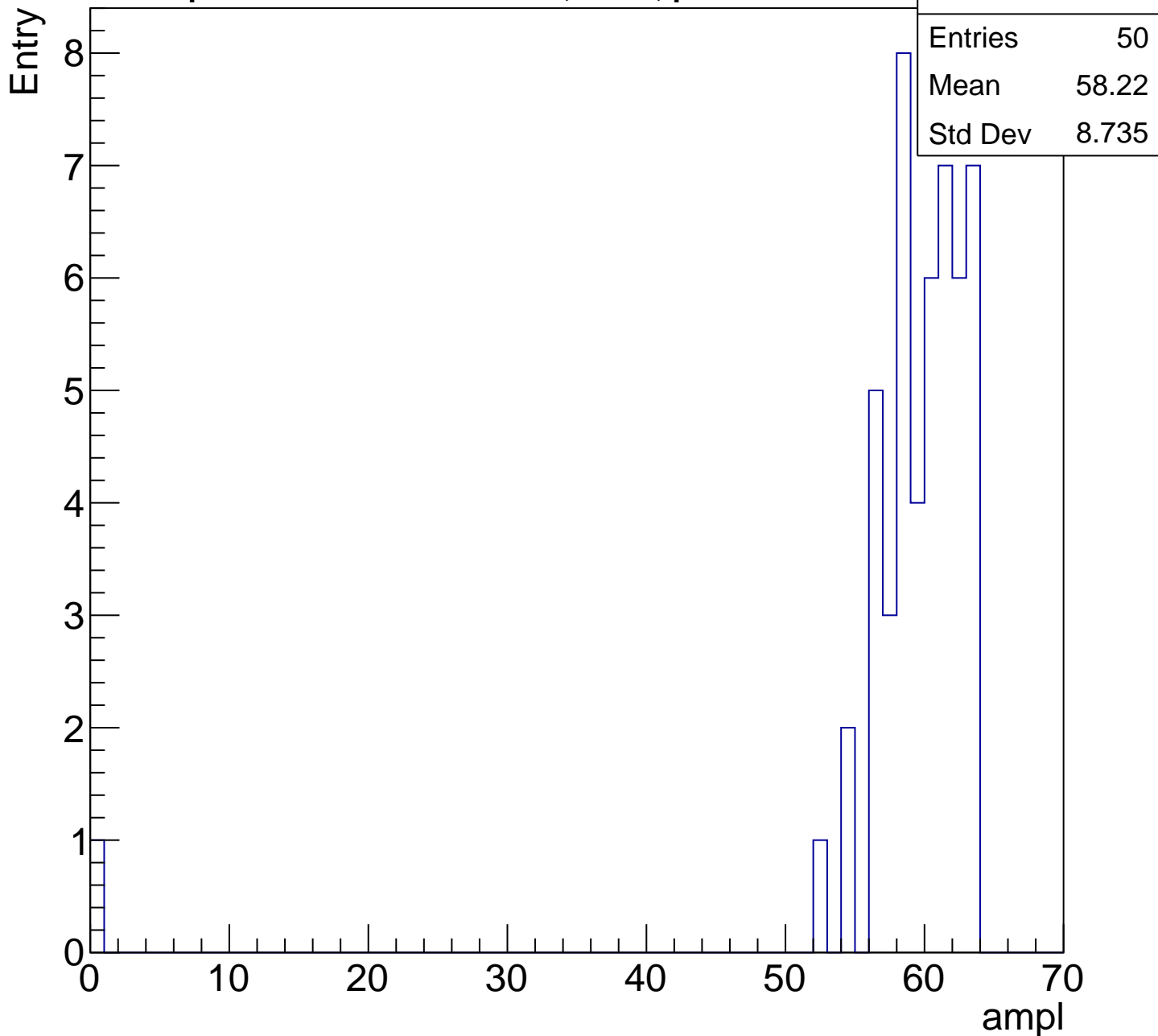
Entry

Entries	58
Mean	54.64
Std Dev	3.305



# B1L103S, U16-ch56, adc5

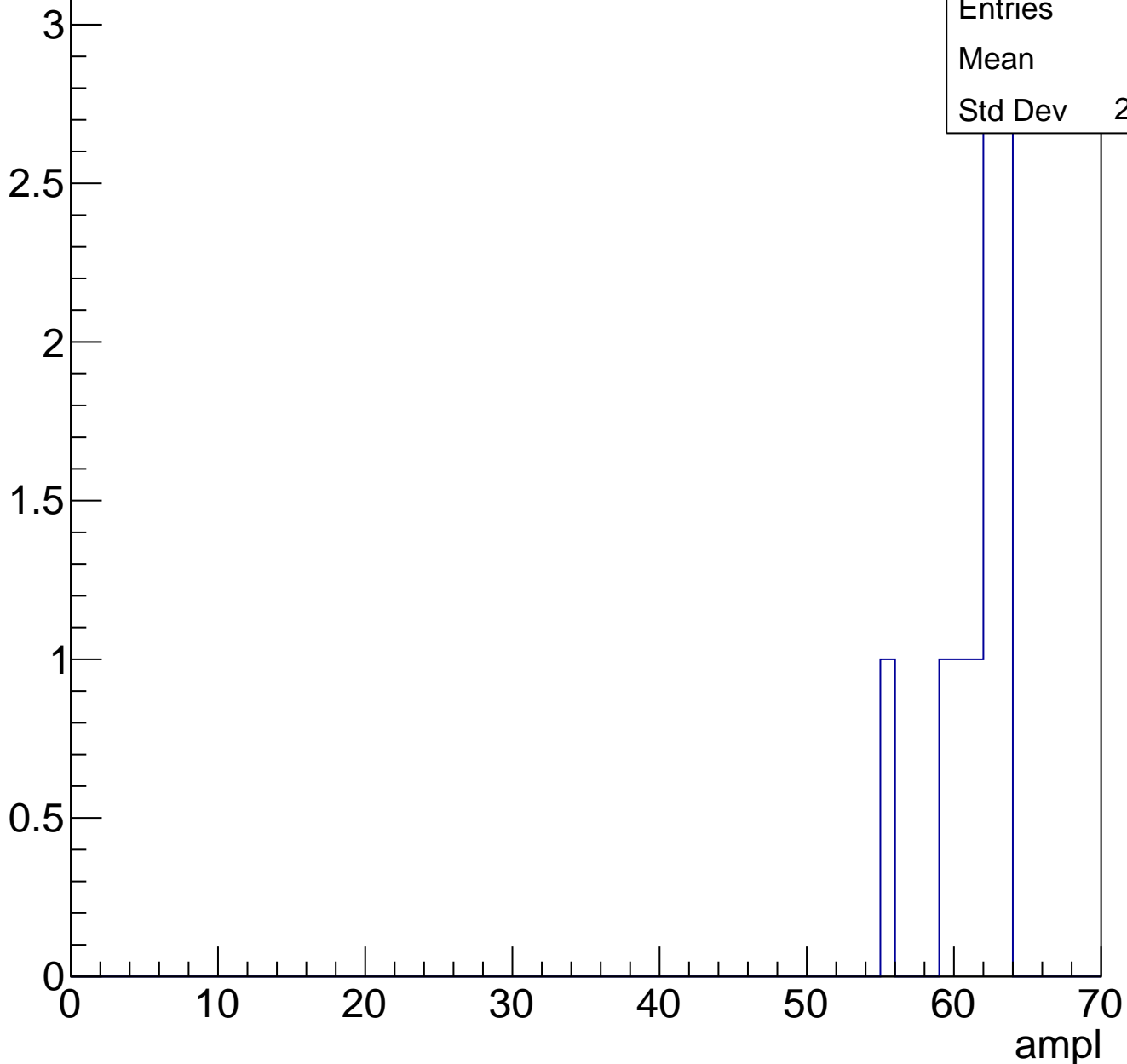
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U16-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

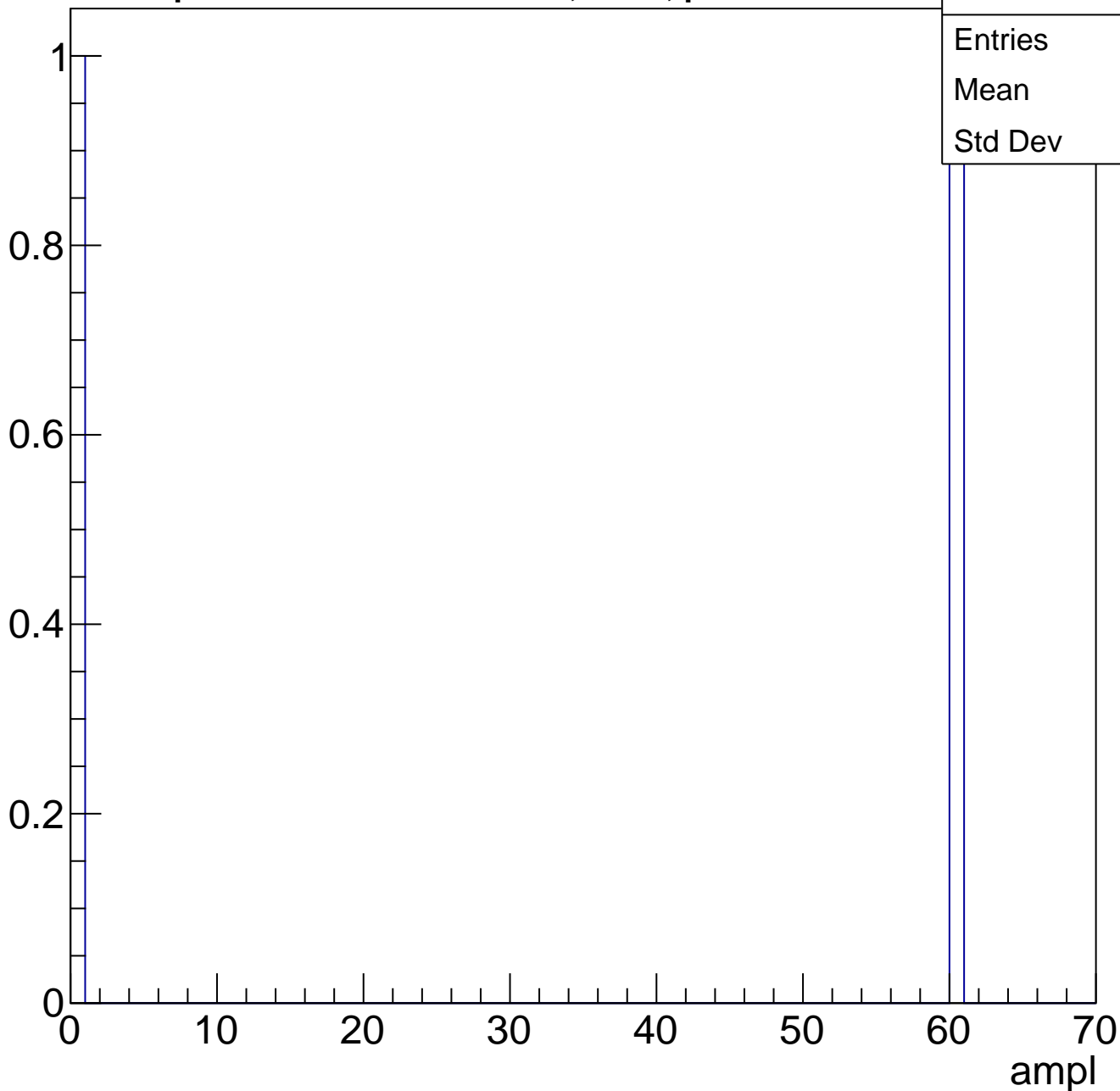




# B1L103S, U16-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch57, adc0

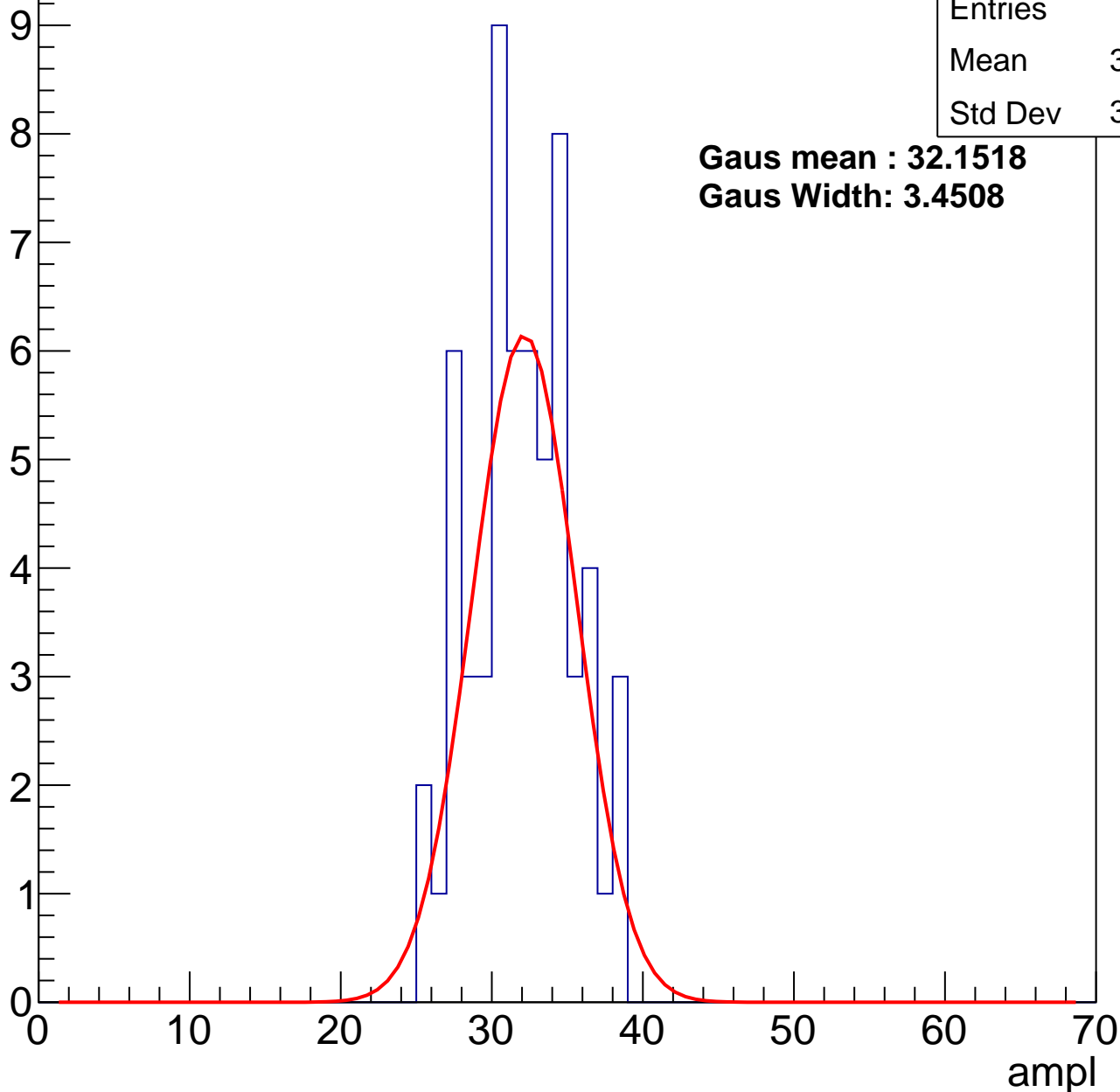
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	31.57
Std Dev	3.293

**Gaus mean : 32.1518**

**Gaus Width: 3.4508**



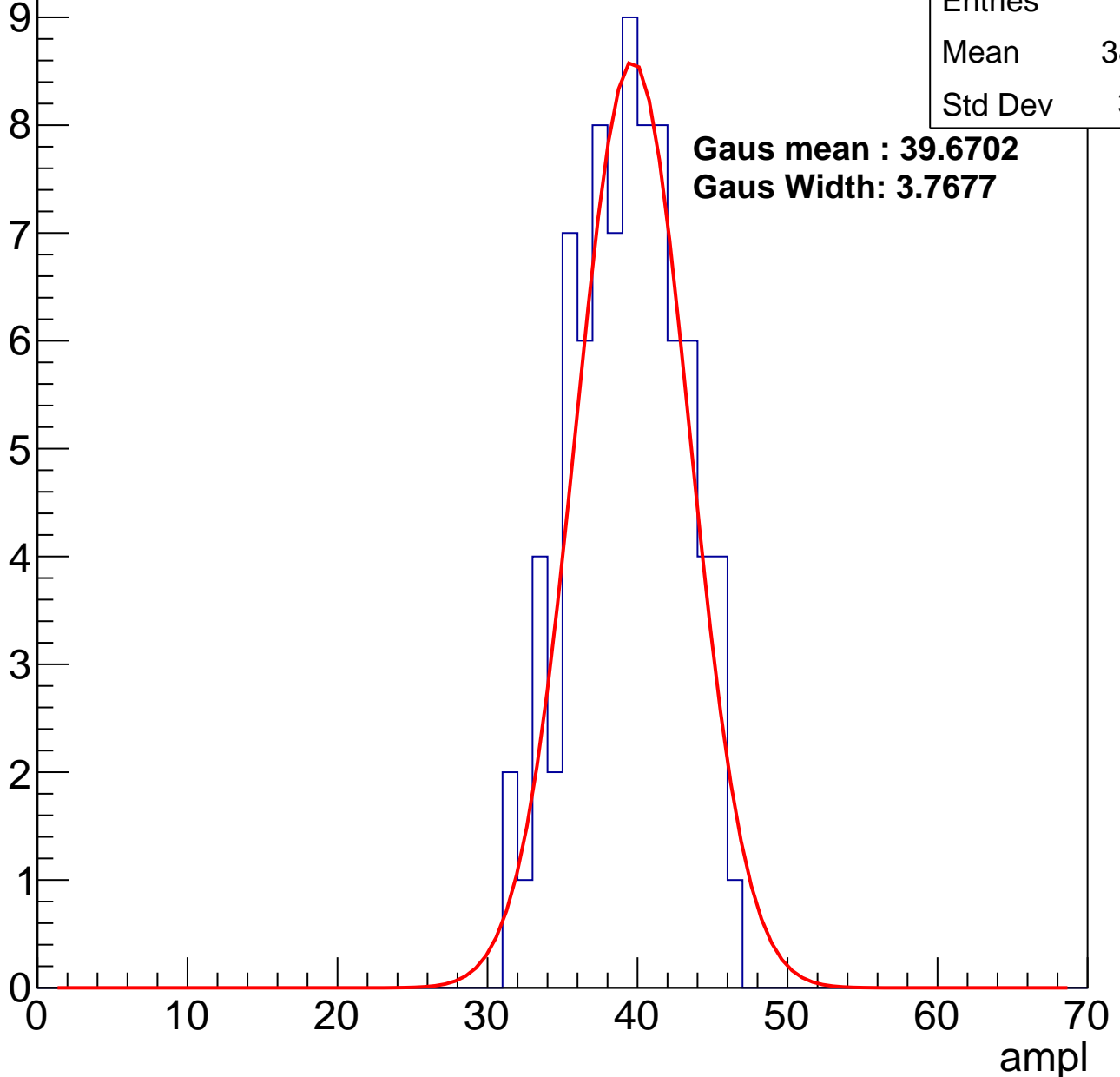
# B1L103S, U16-ch57, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	38.89
Std Dev	3.57

**Gaus mean : 39.6702**  
**Gaus Width: 3.7677**



# B1L103S, U16-ch57, adc2

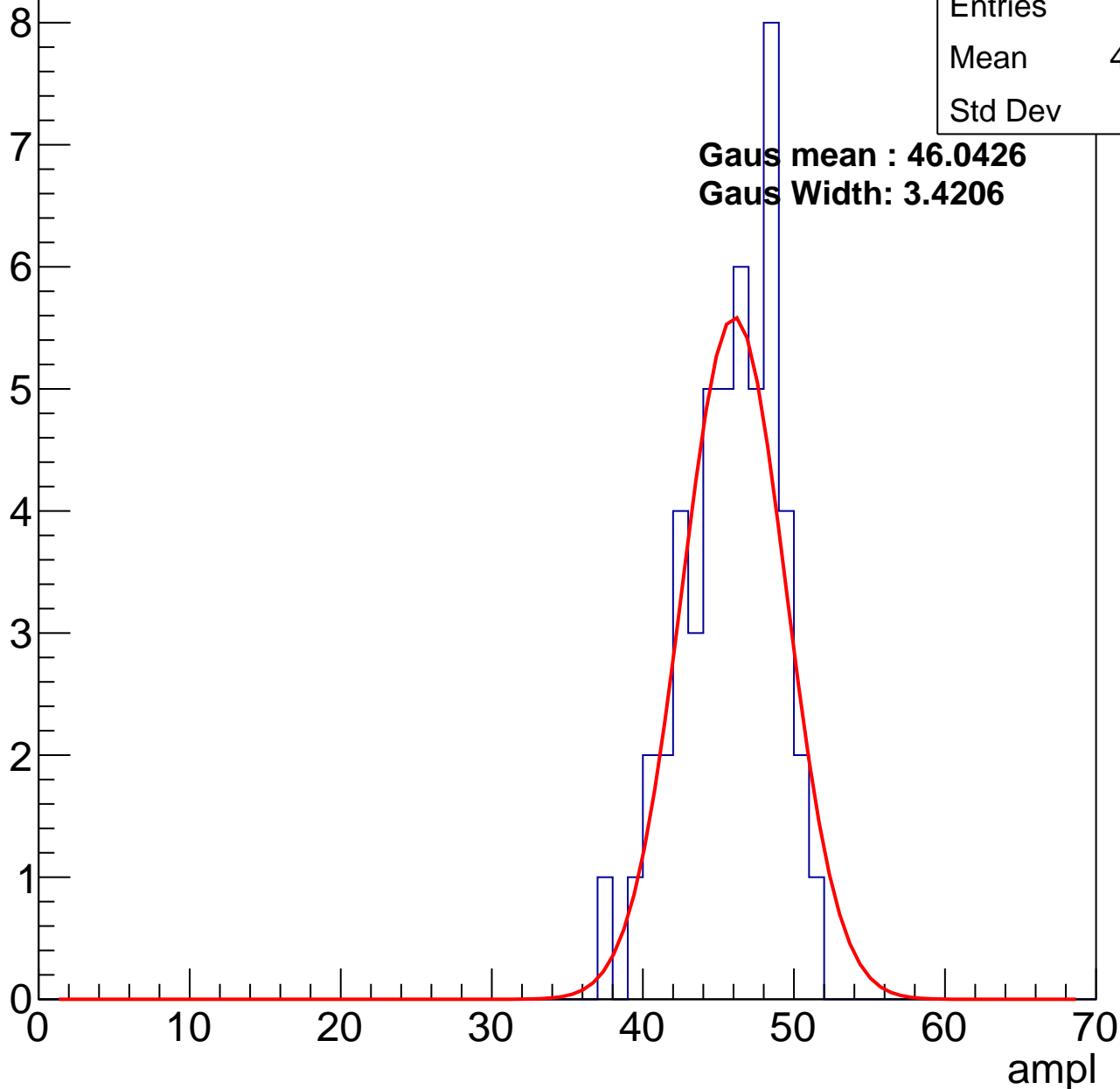
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	45.35
Std Dev	3.12

**Gaus mean : 46.0426**

**Gaus Width: 3.4206**

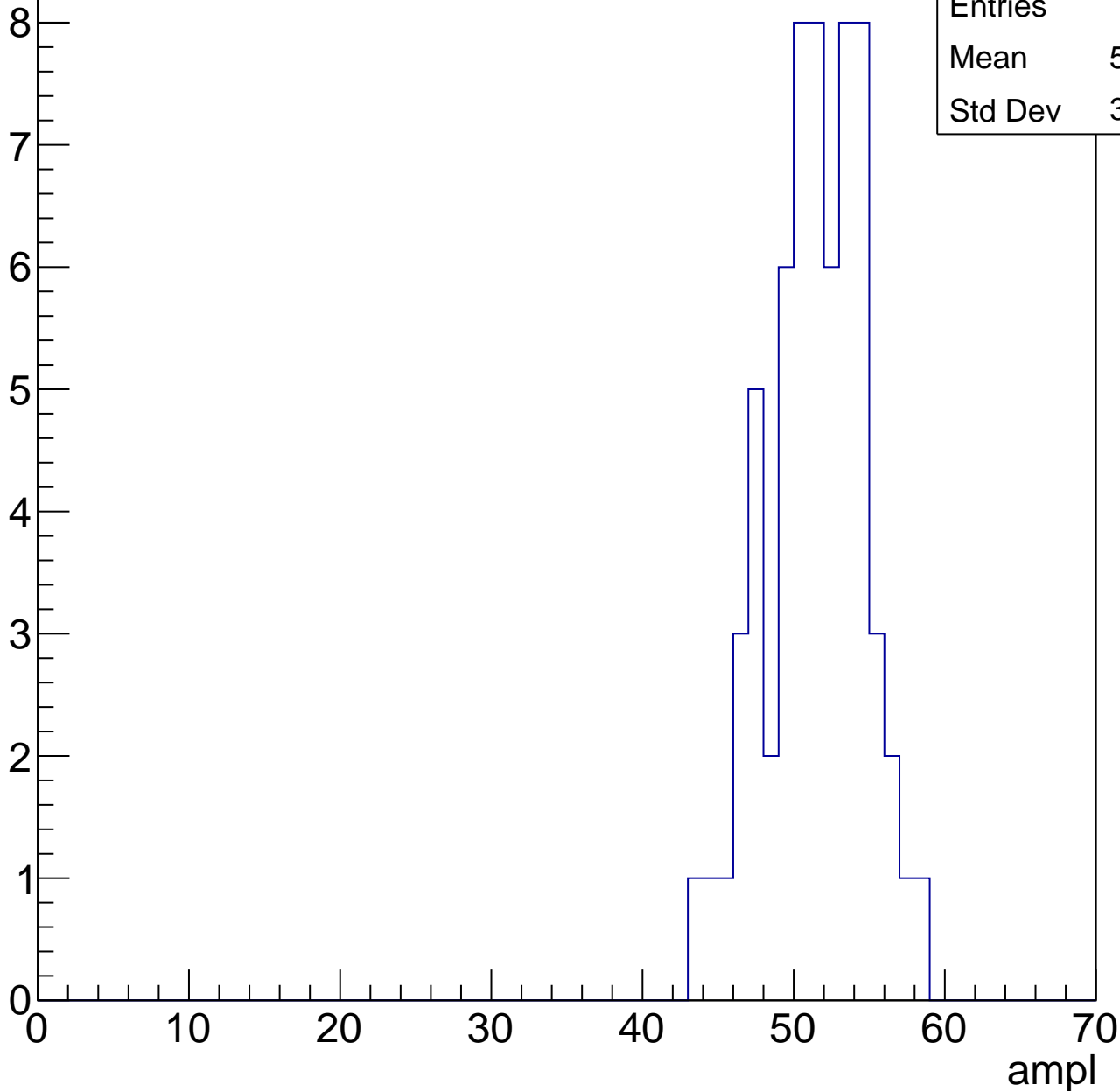


# B1L103S, U16-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

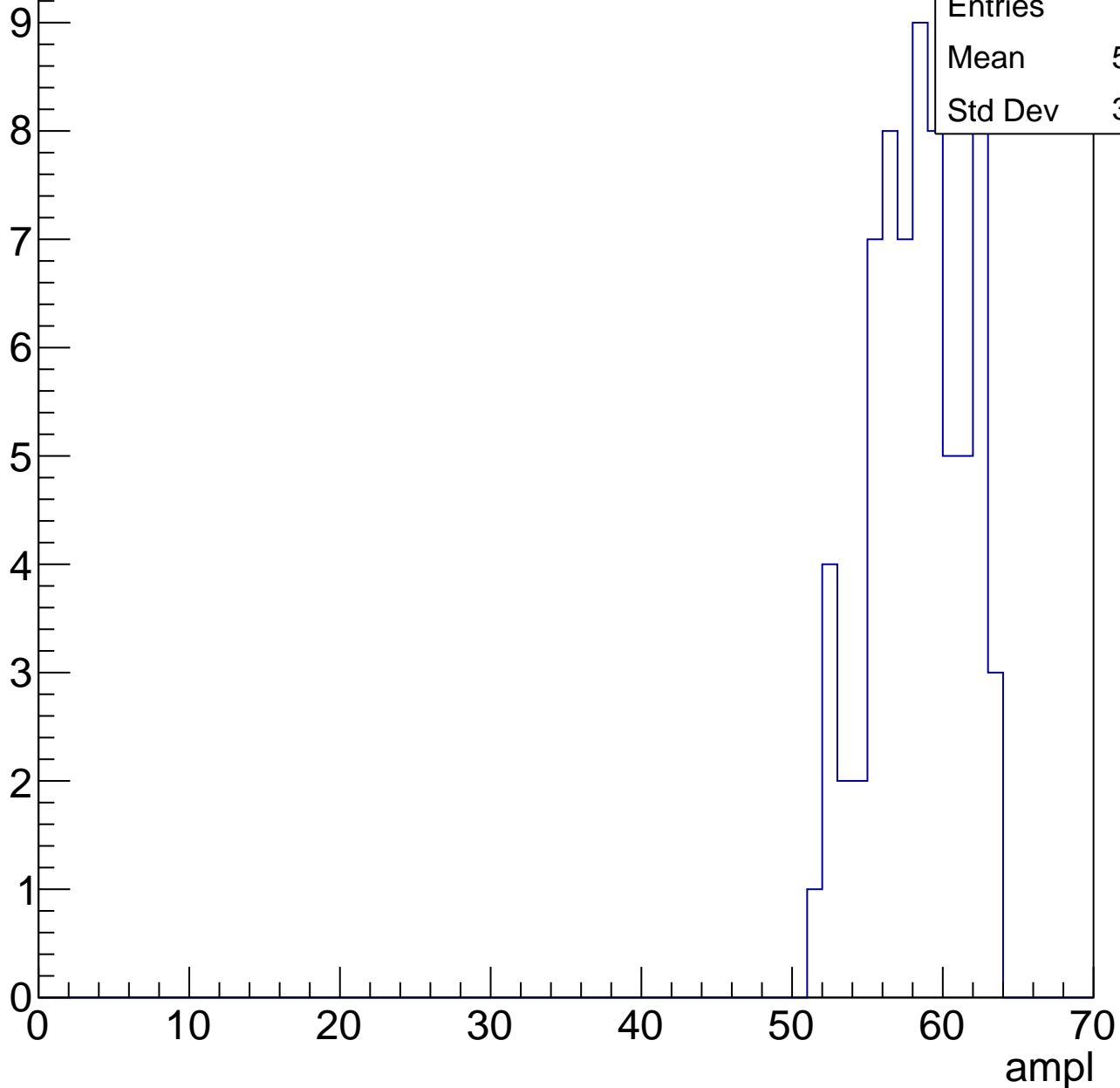
Entries	64
Mean	50.98
Std Dev	3.179



# B1L103S, U16-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

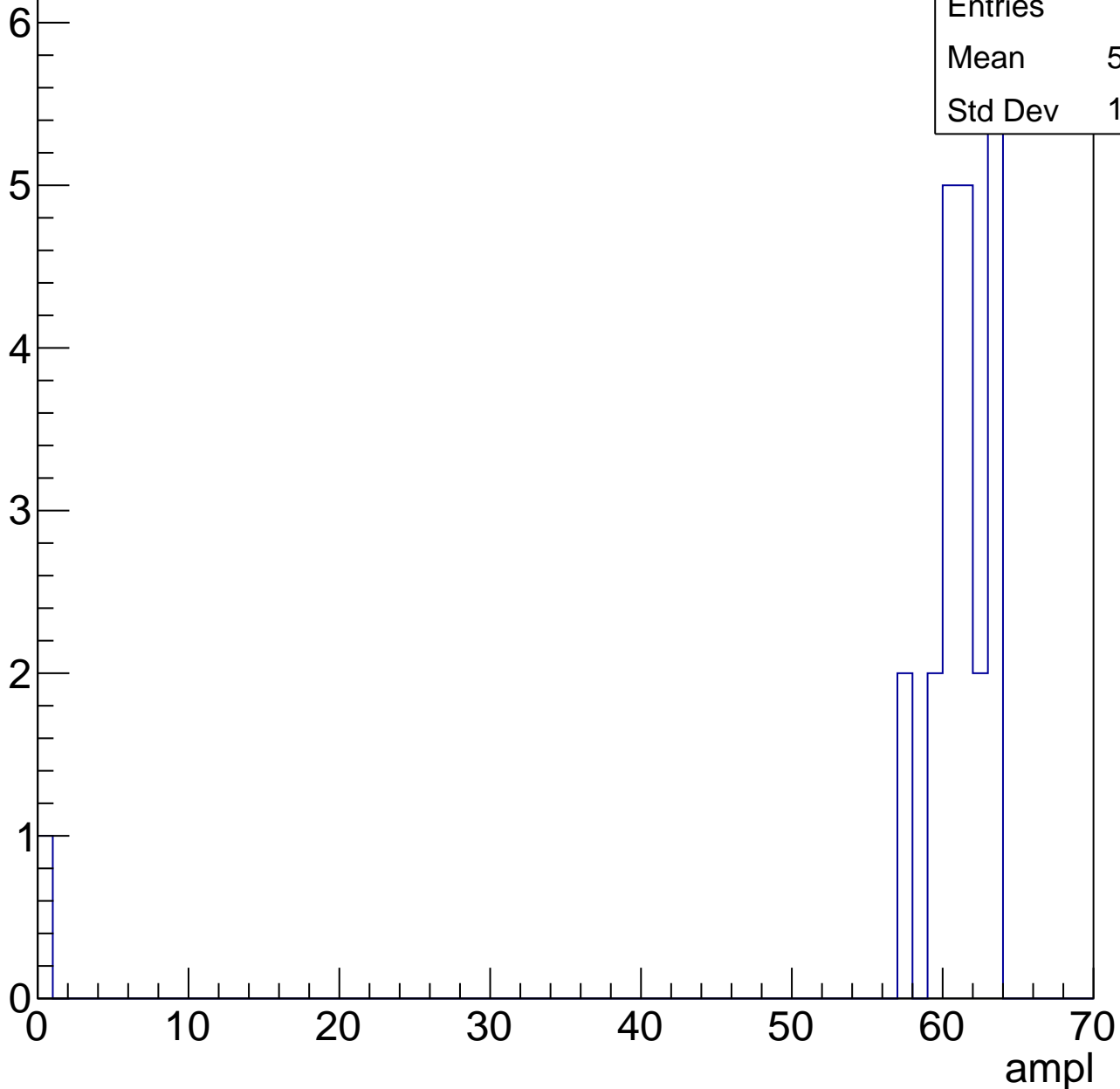


# B1L103S, U16-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	23
Mean	58.22
Std Dev	12.54



# B1L103S, U16-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	63
Std Dev	0



# B1L103S, U16-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U16-ch58, adc0

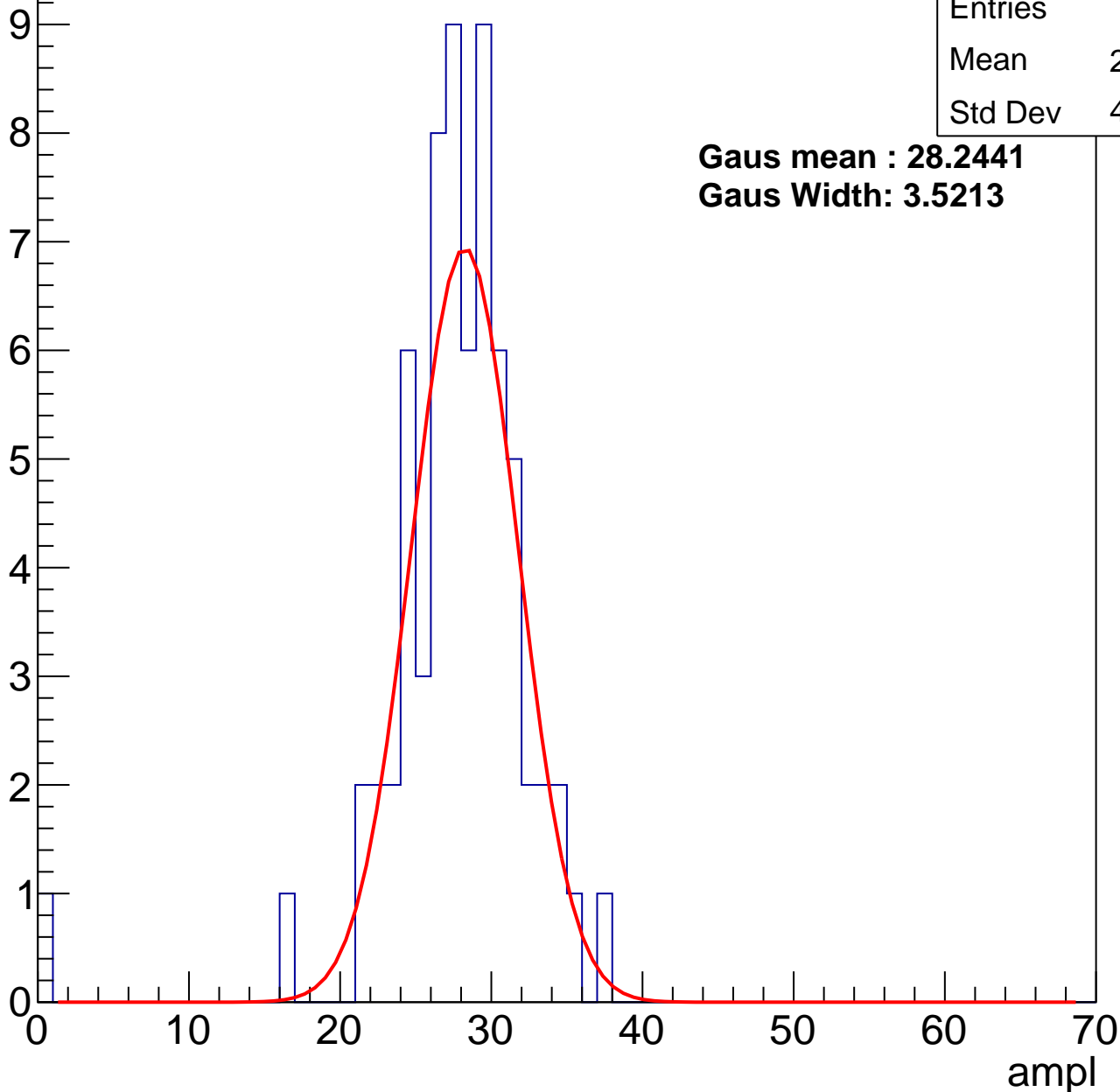
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	27.24
Std Dev	4.902

**Gaus mean : 28.2441**

**Gaus Width: 3.5213**



# B1L103S, U16-ch58, adc1

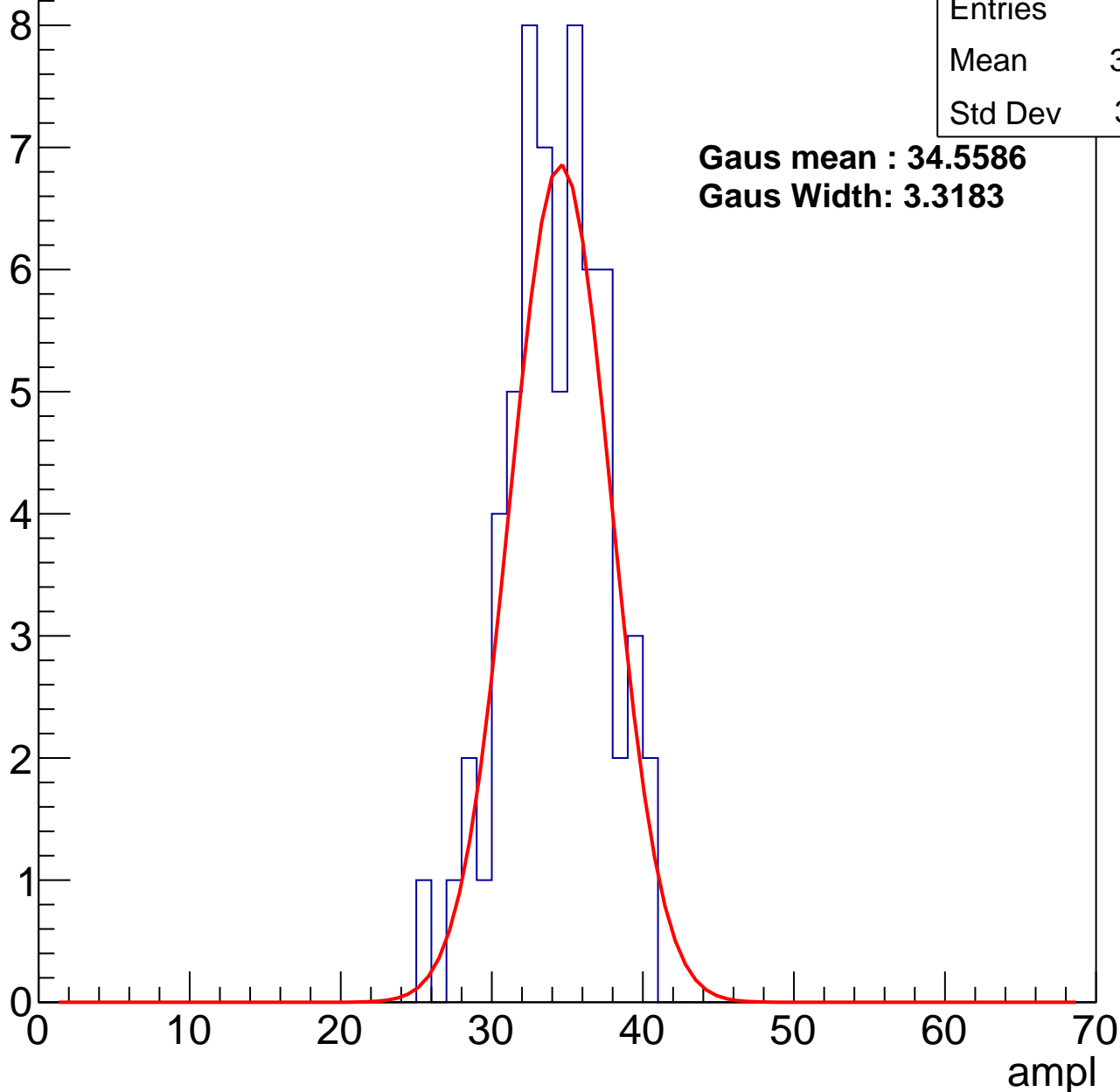
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	33.77
Std Dev	3.231

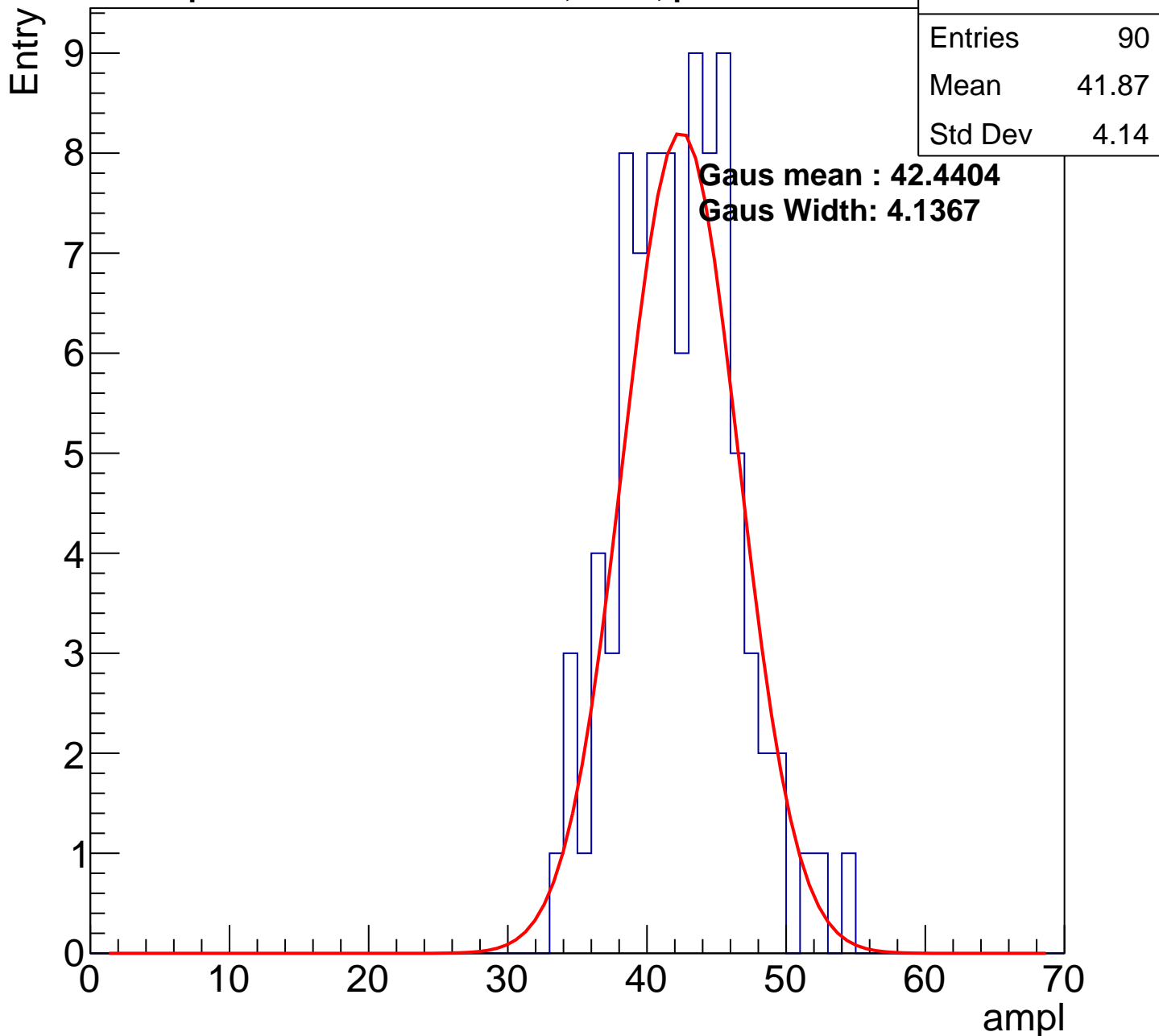
**Gaus mean : 34.5586**

**Gaus Width: 3.3183**



# B1L103S, U16-ch58, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

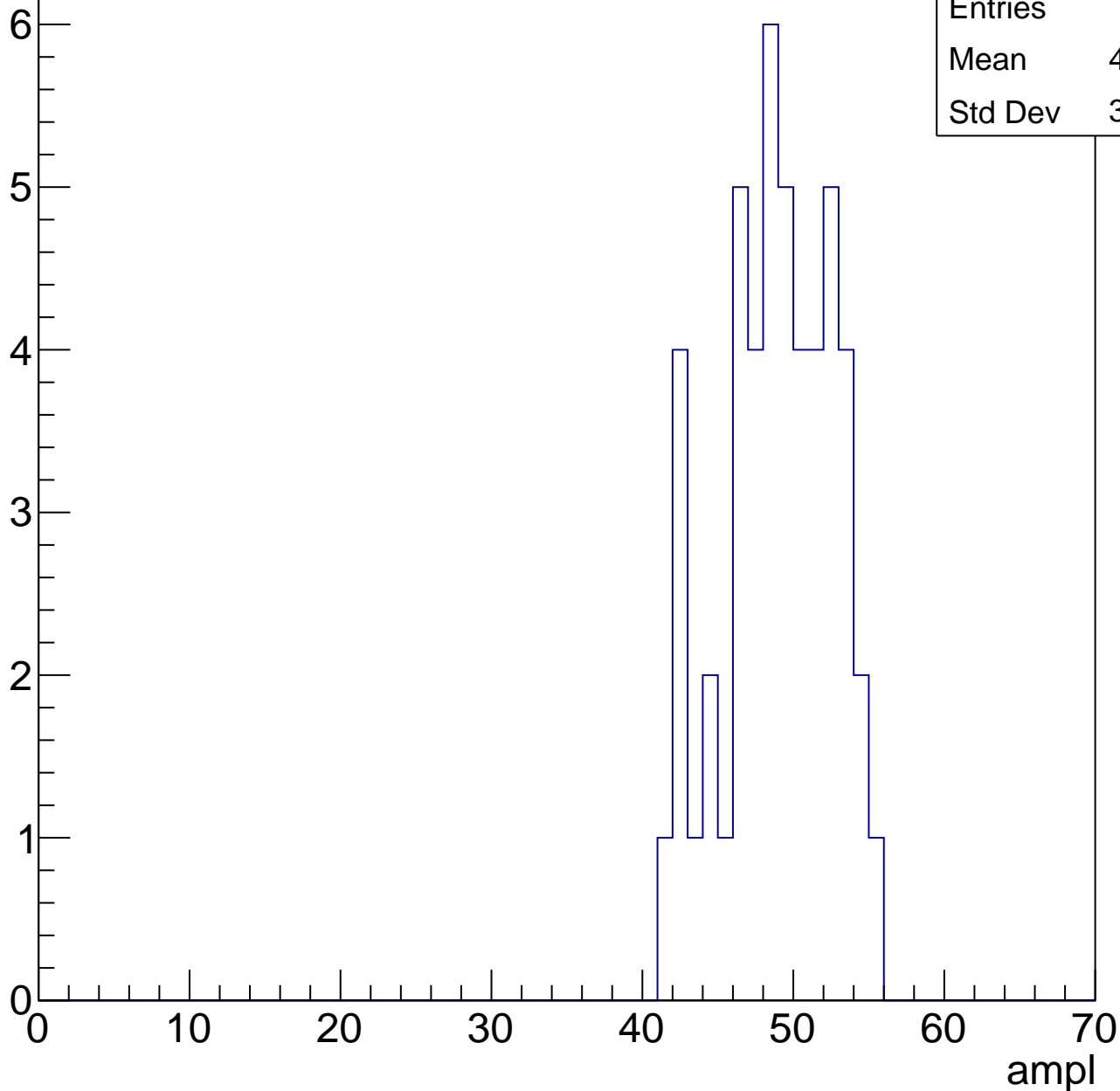


# B1L103S, U16-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	48.47
Std Dev	3.586

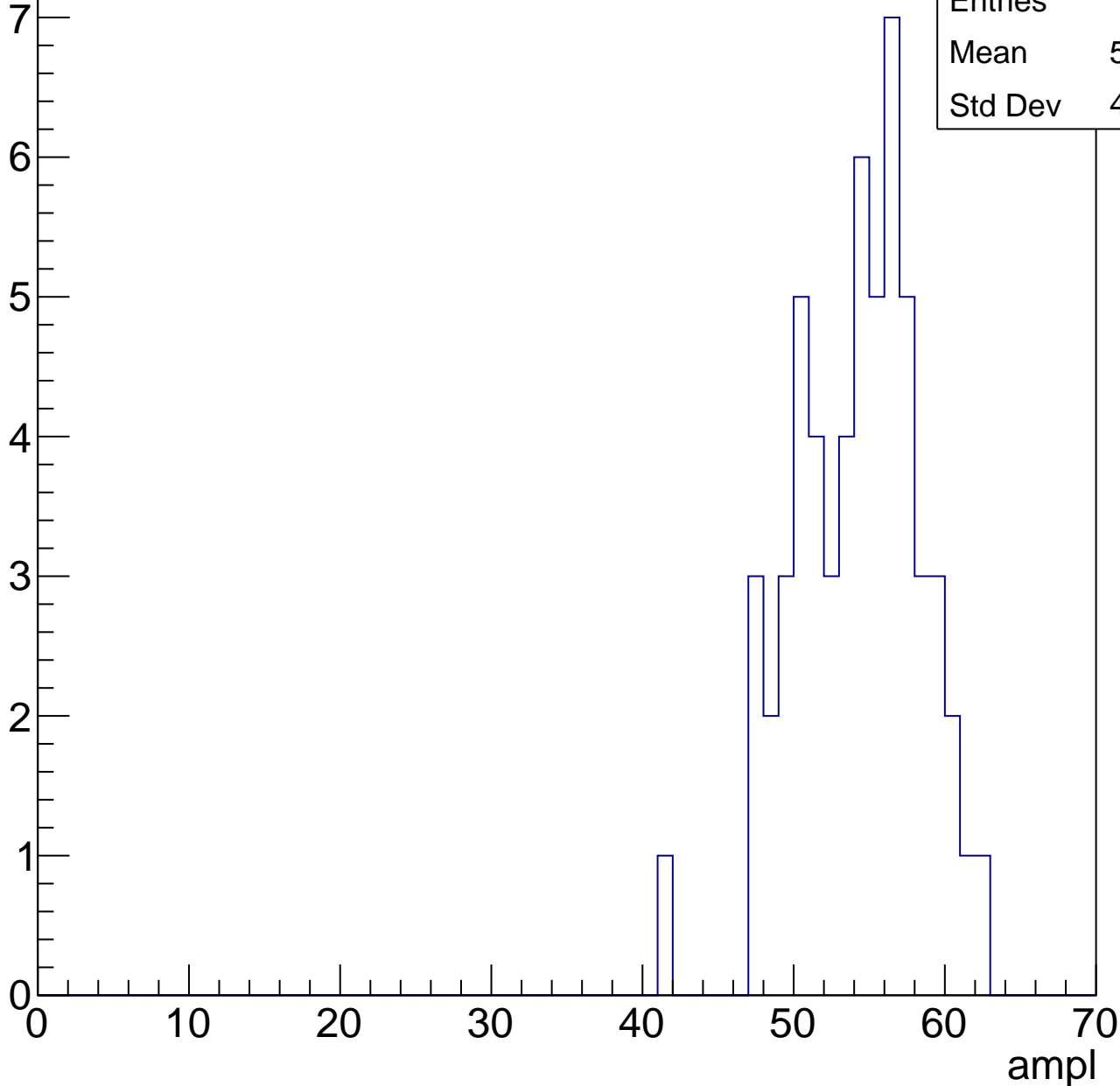


# B1L103S, U16-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	53.74
Std Dev	4.104

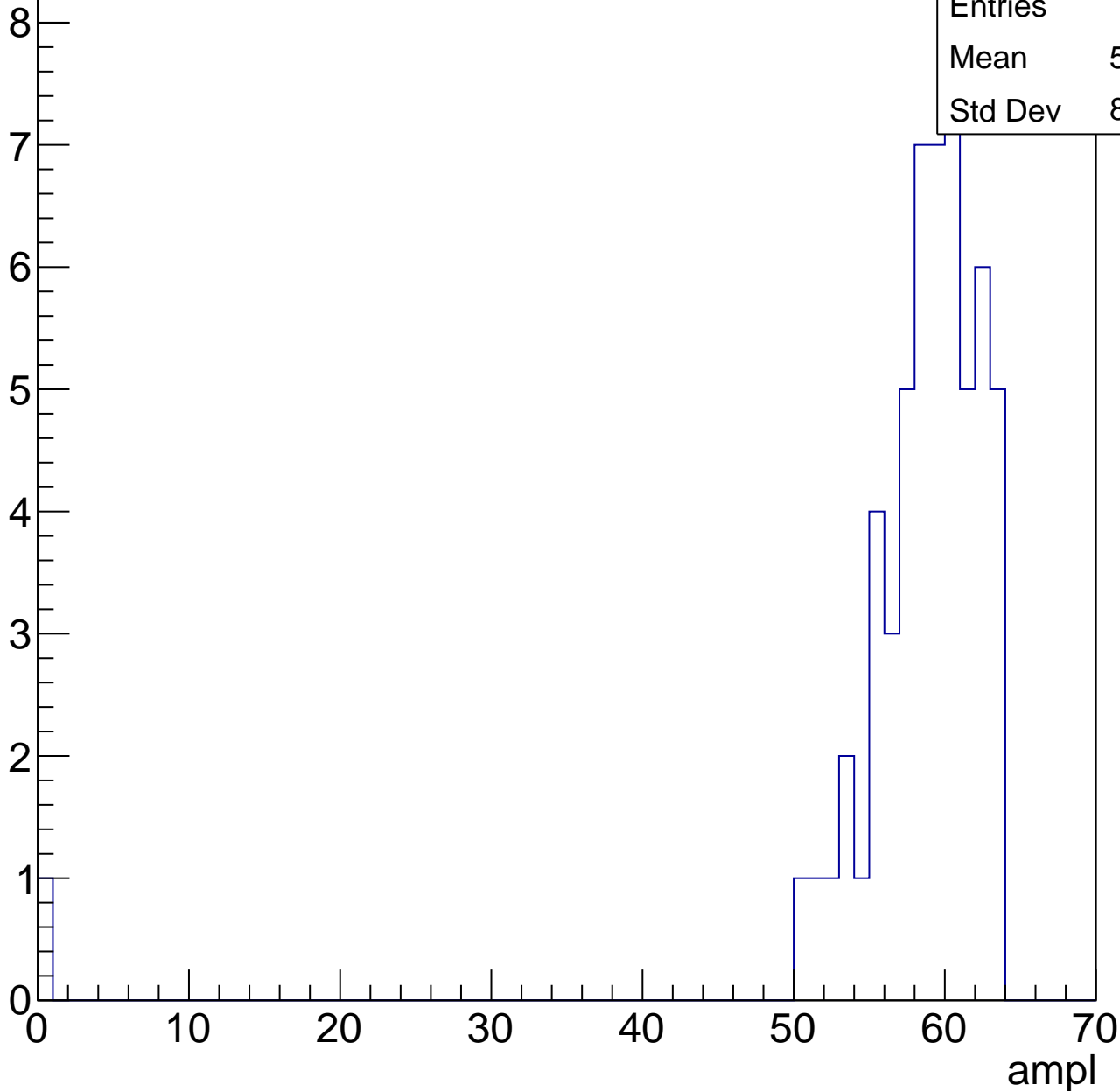


# B1L103S, U16-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	57.49
Std Dev	8.295

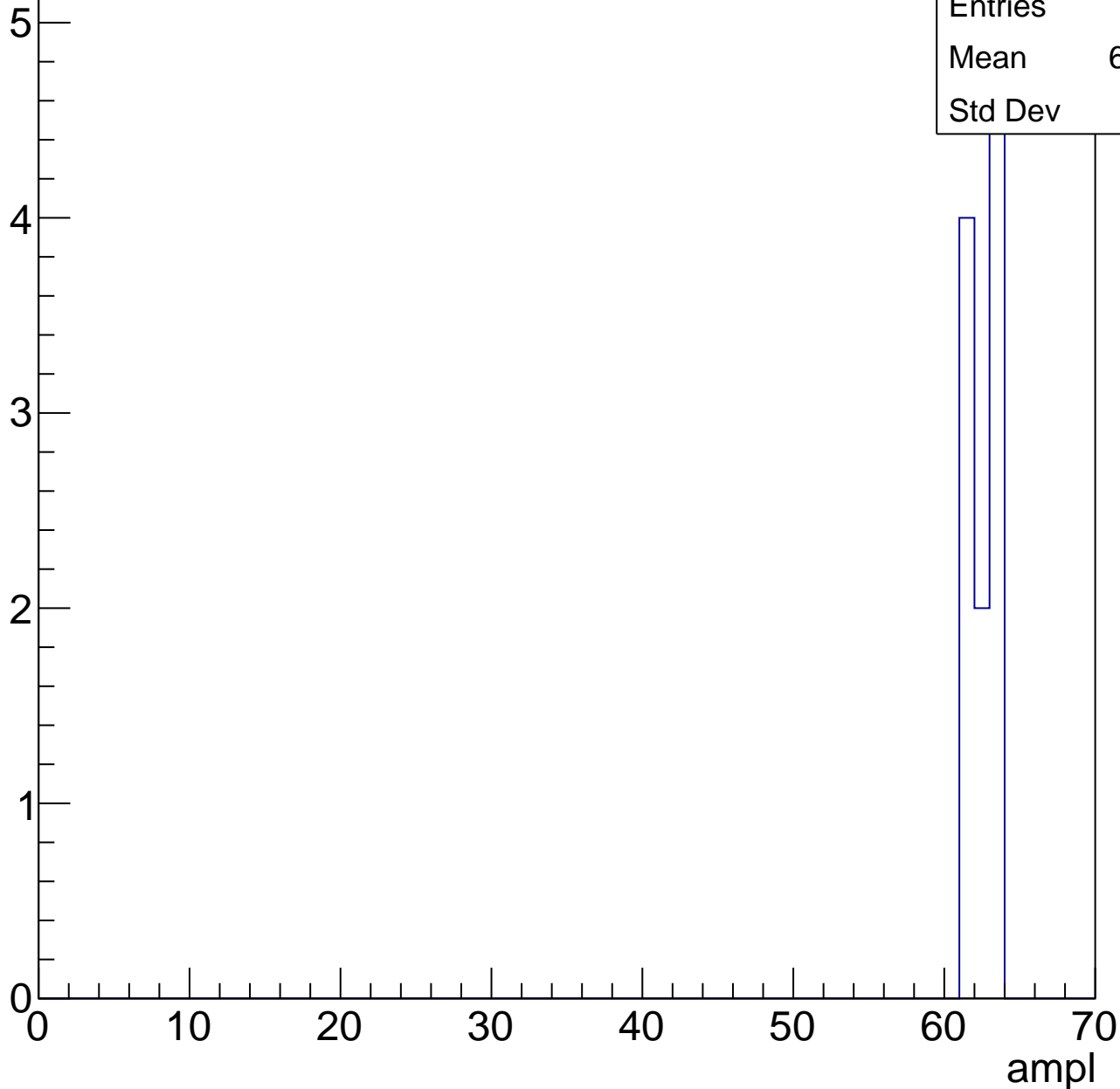


# B1L103S, U16-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	11
Mean	62.09
Std Dev	0.9





# B1L103S, U16-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch59, adc0

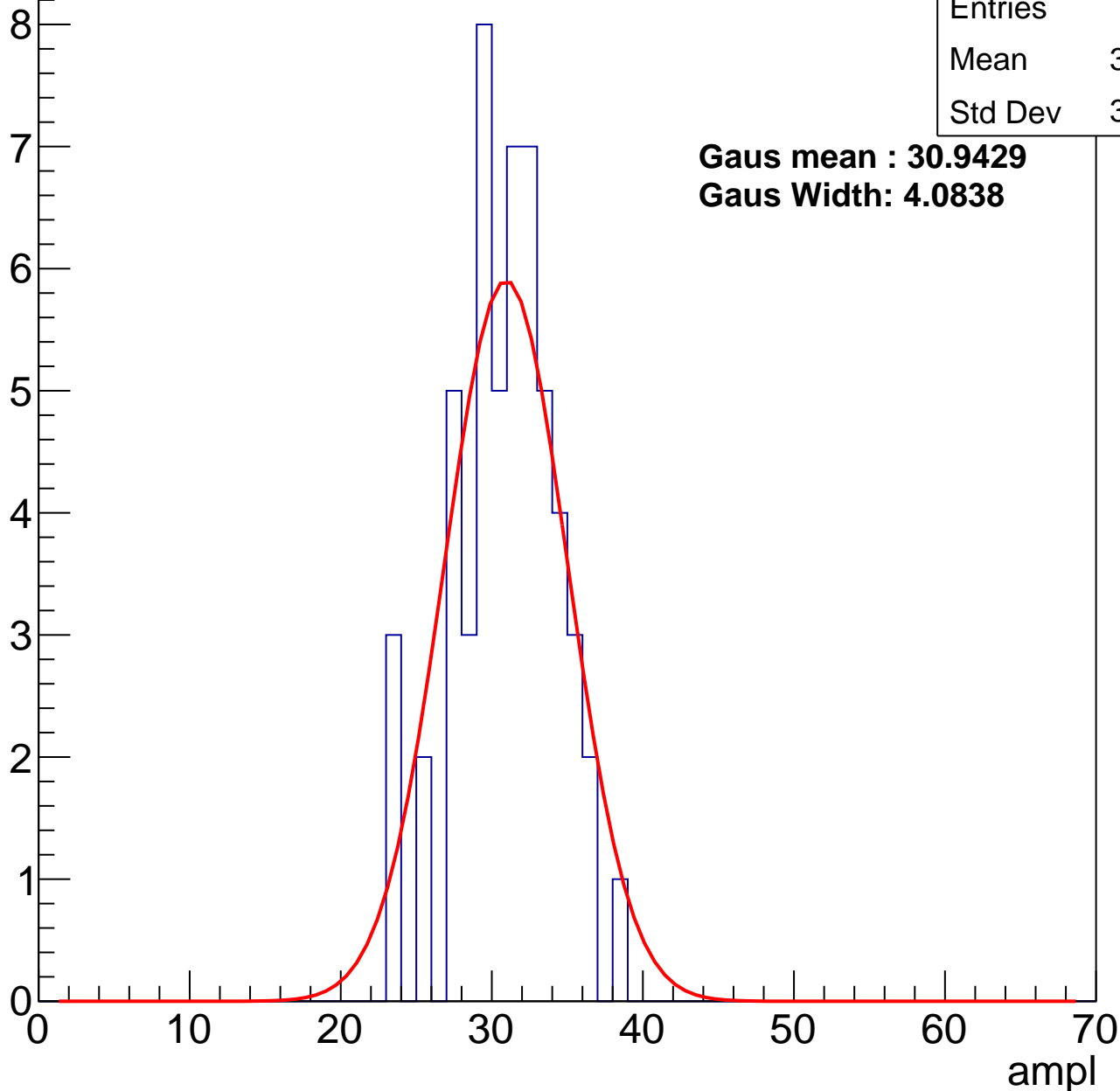
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	30.49
Std Dev	3.313

**Gaus mean : 30.9429**

**Gaus Width: 4.0838**



# B1L103S, U16-ch59, adc1

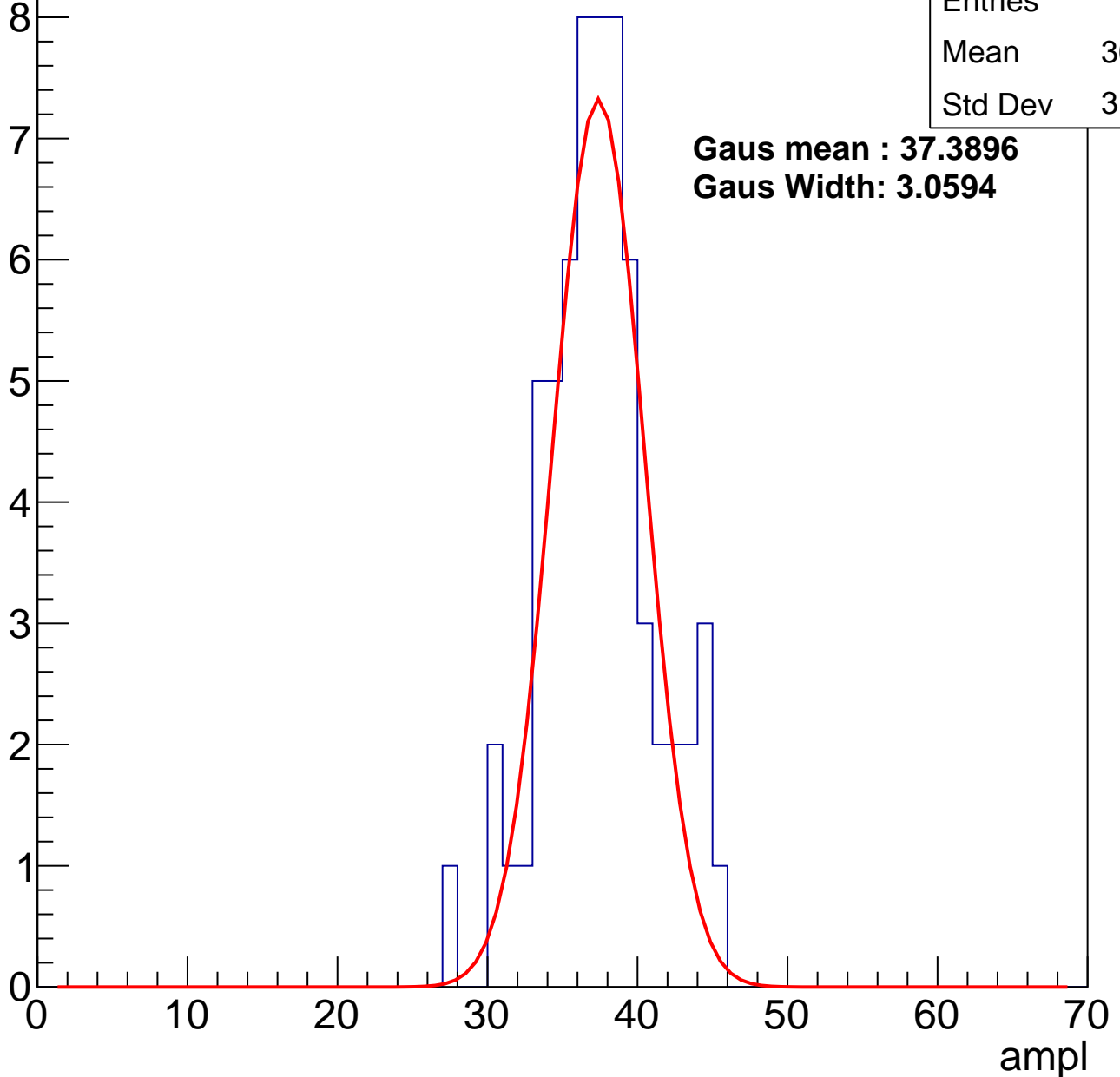
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	36.97
Std Dev	3.623

**Gaus mean : 37.3896**

**Gaus Width: 3.0594**



# B1L103S, U16-ch59, adc2

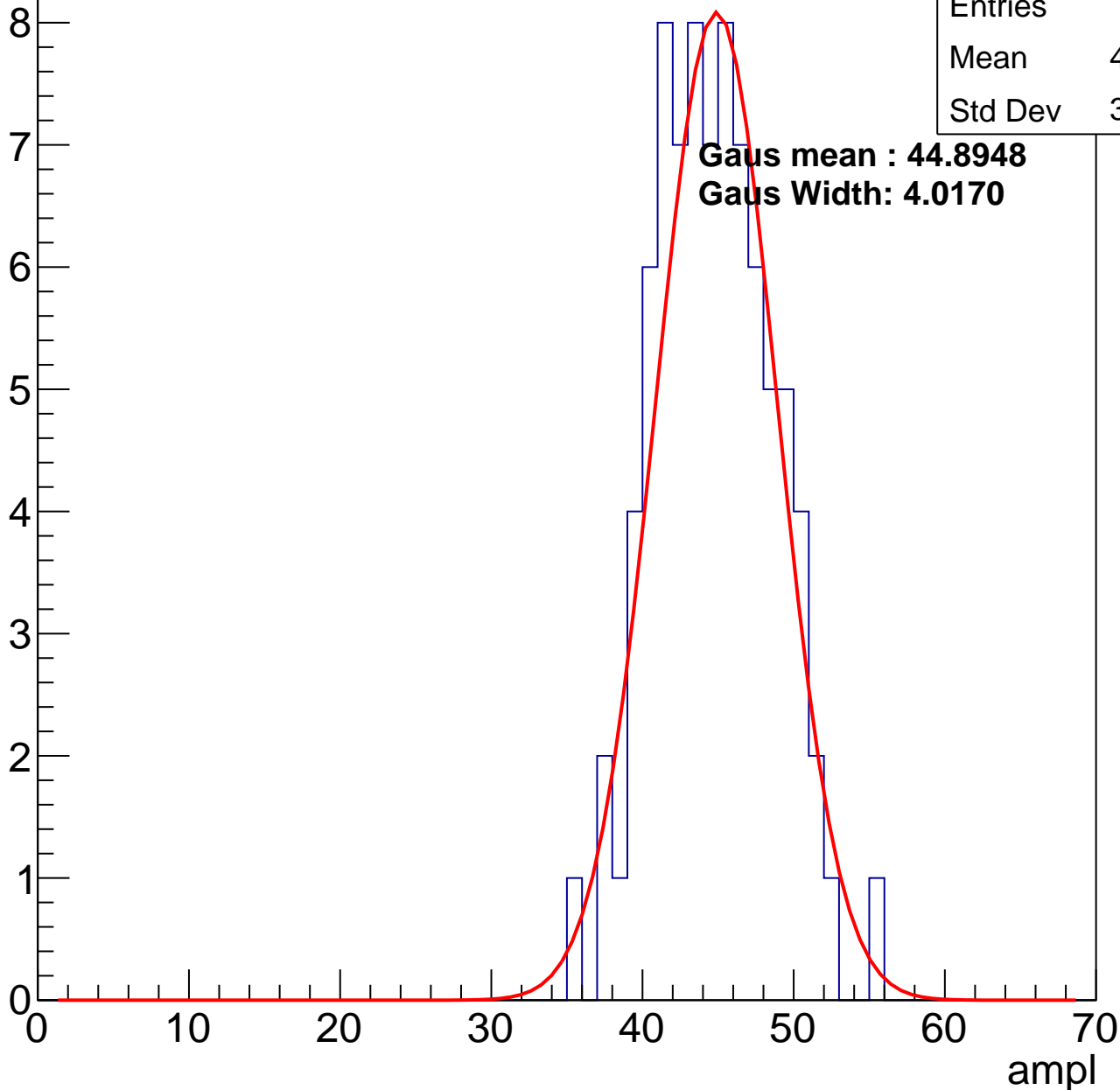
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	44.28
Std Dev	3.857

**Gaus mean : 44.8948**

**Gaus Width: 4.0170**

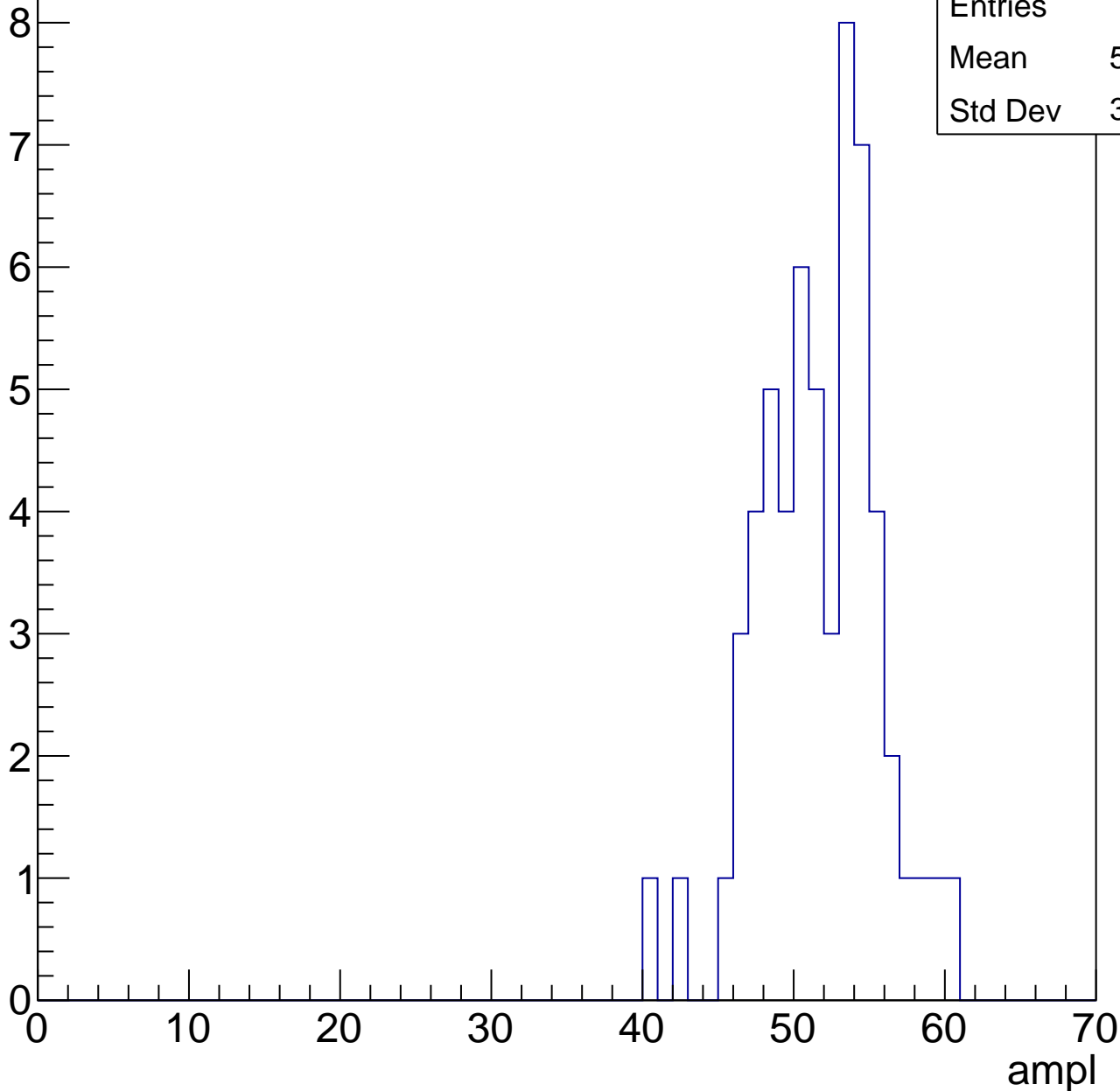


# B1L103S, U16-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	51.17
Std Dev	3.905

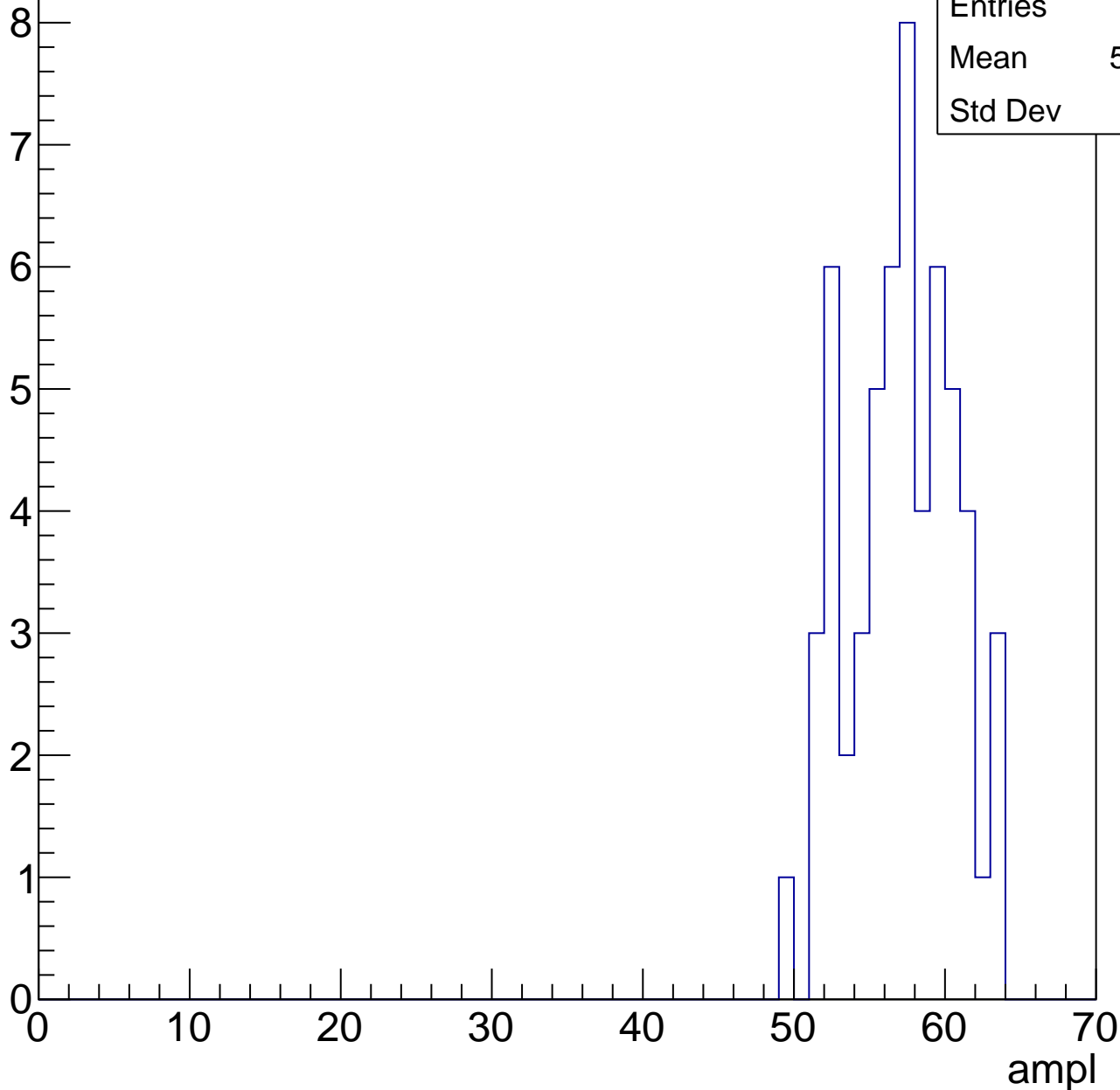


# B1L103S, U16-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	56.67
Std Dev	3.43

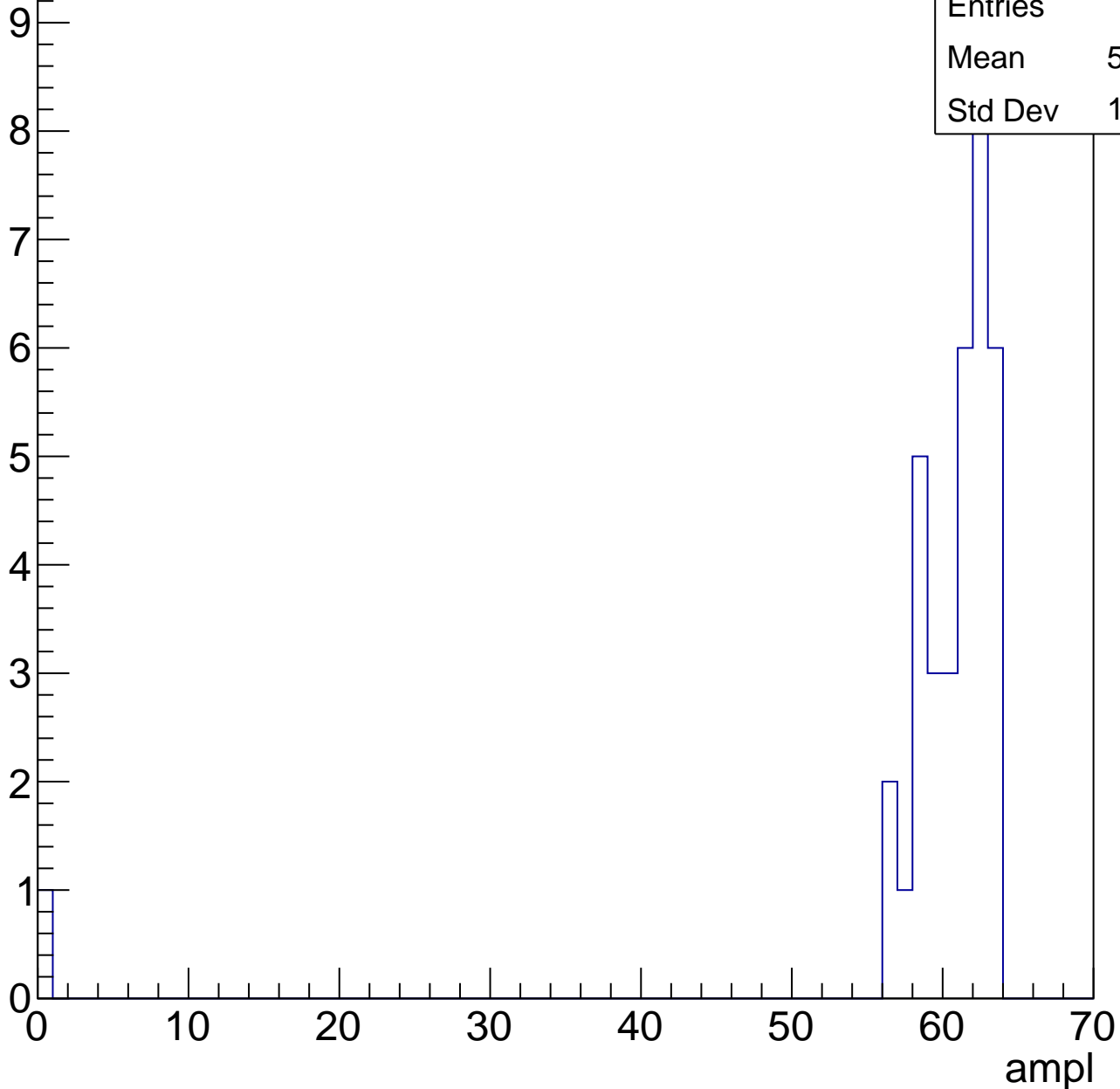


# B1L103S, U16-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	36
Mean	58.83
Std Dev	10.15



# B1L103S, U16-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L103S, U16-ch60, adc0

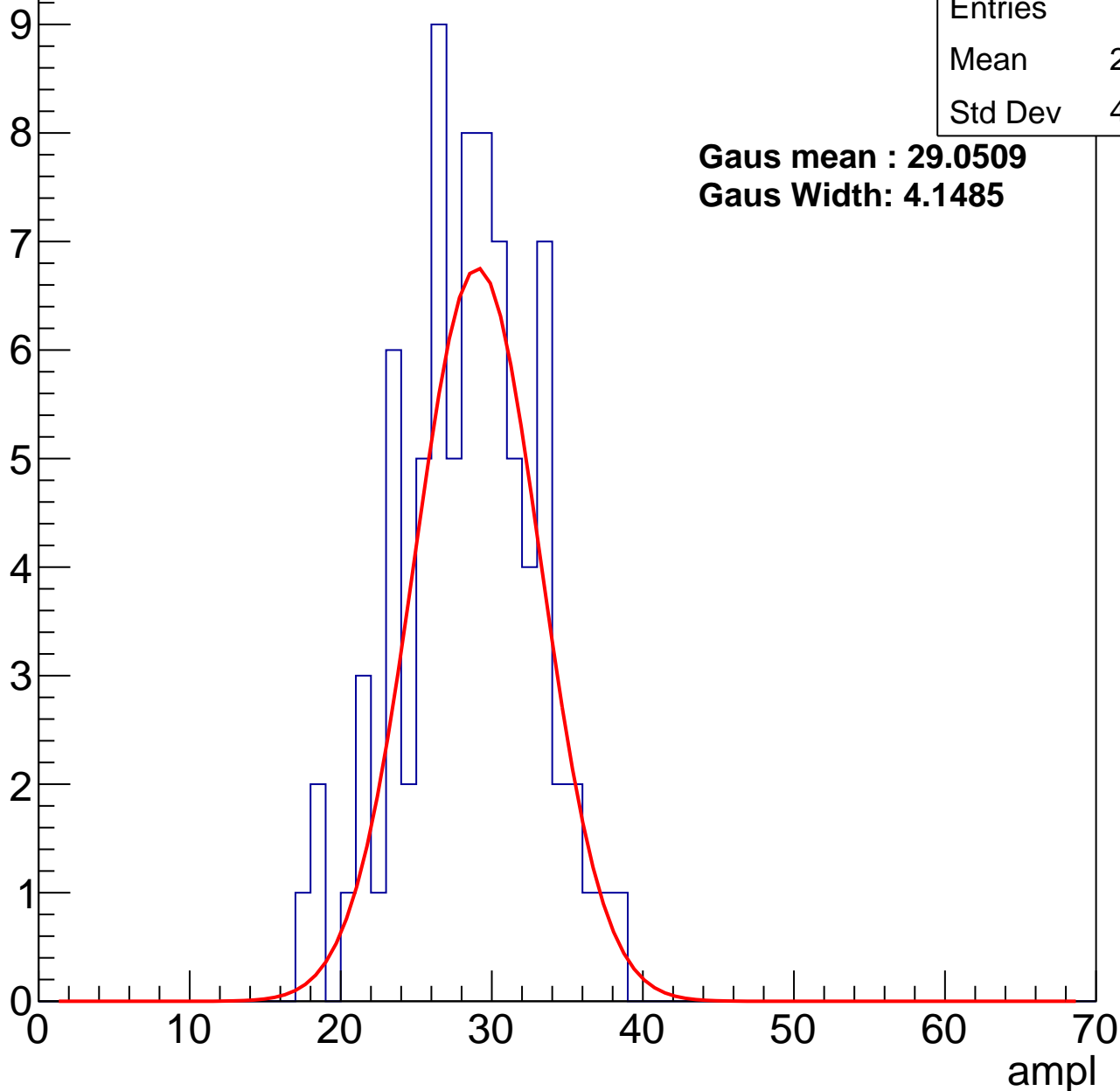
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	81
Mean	27.99
Std Dev	4.404

**Gaus mean : 29.0509**

**Gaus Width: 4.1485**



# B1L103S, U16-ch60, adc1

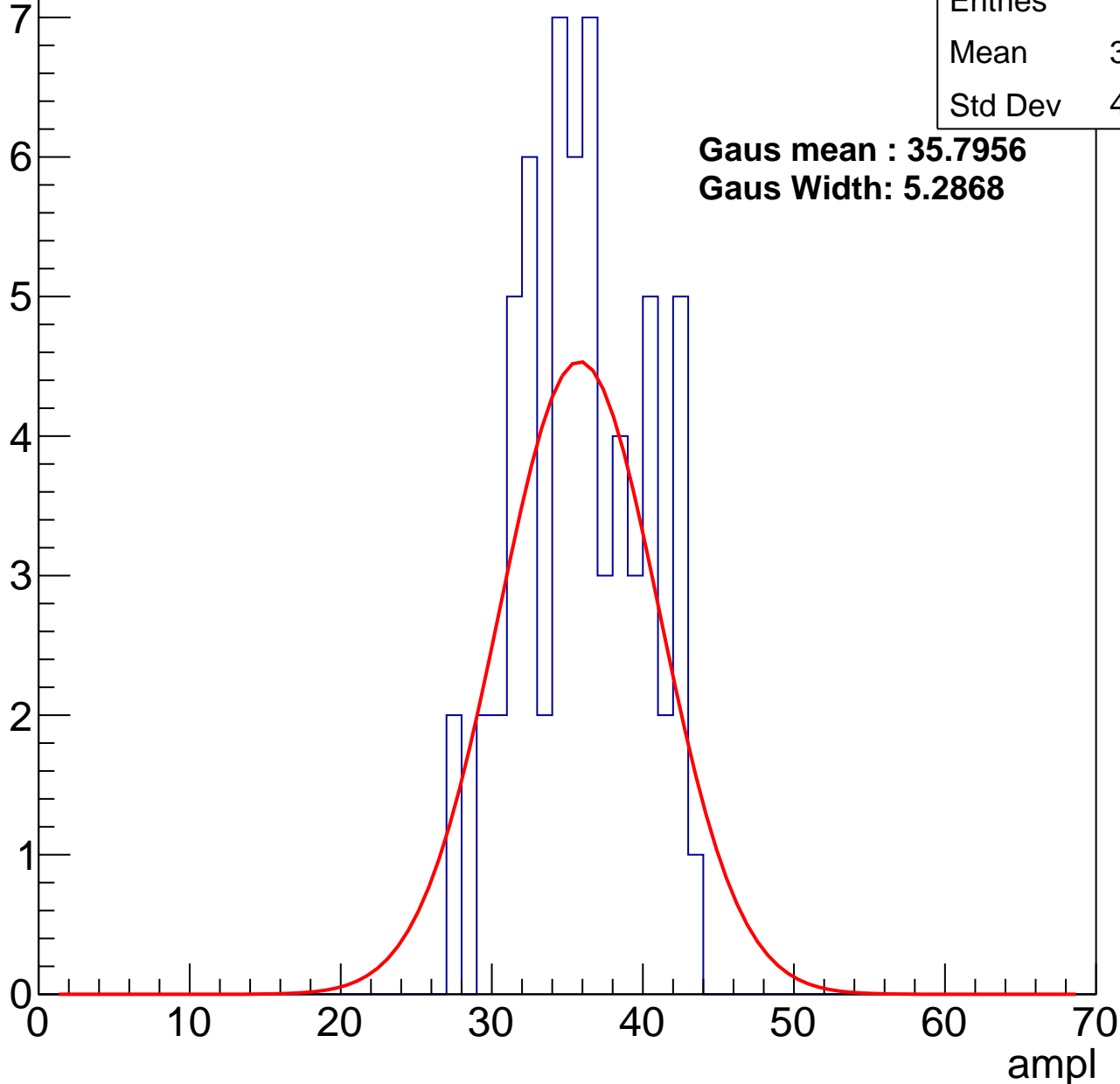
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	35.48
Std Dev	4.003

**Gaus mean : 35.7956**

**Gaus Width: 5.2868**



# B1L103S, U16-ch60, adc2

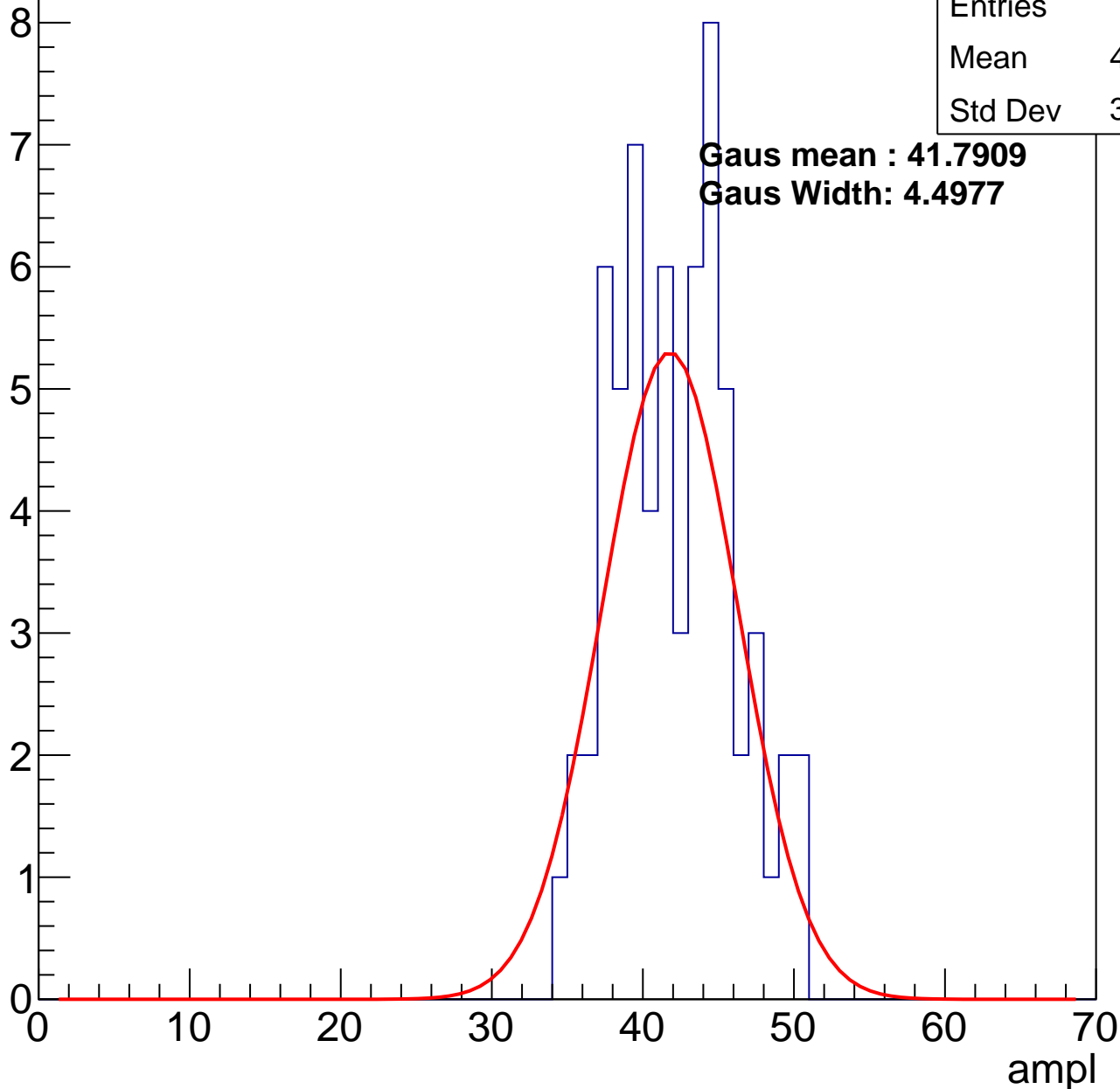
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	41.65
Std Dev	3.908

**Gaus mean : 41.7909**

**Gaus Width: 4.4977**

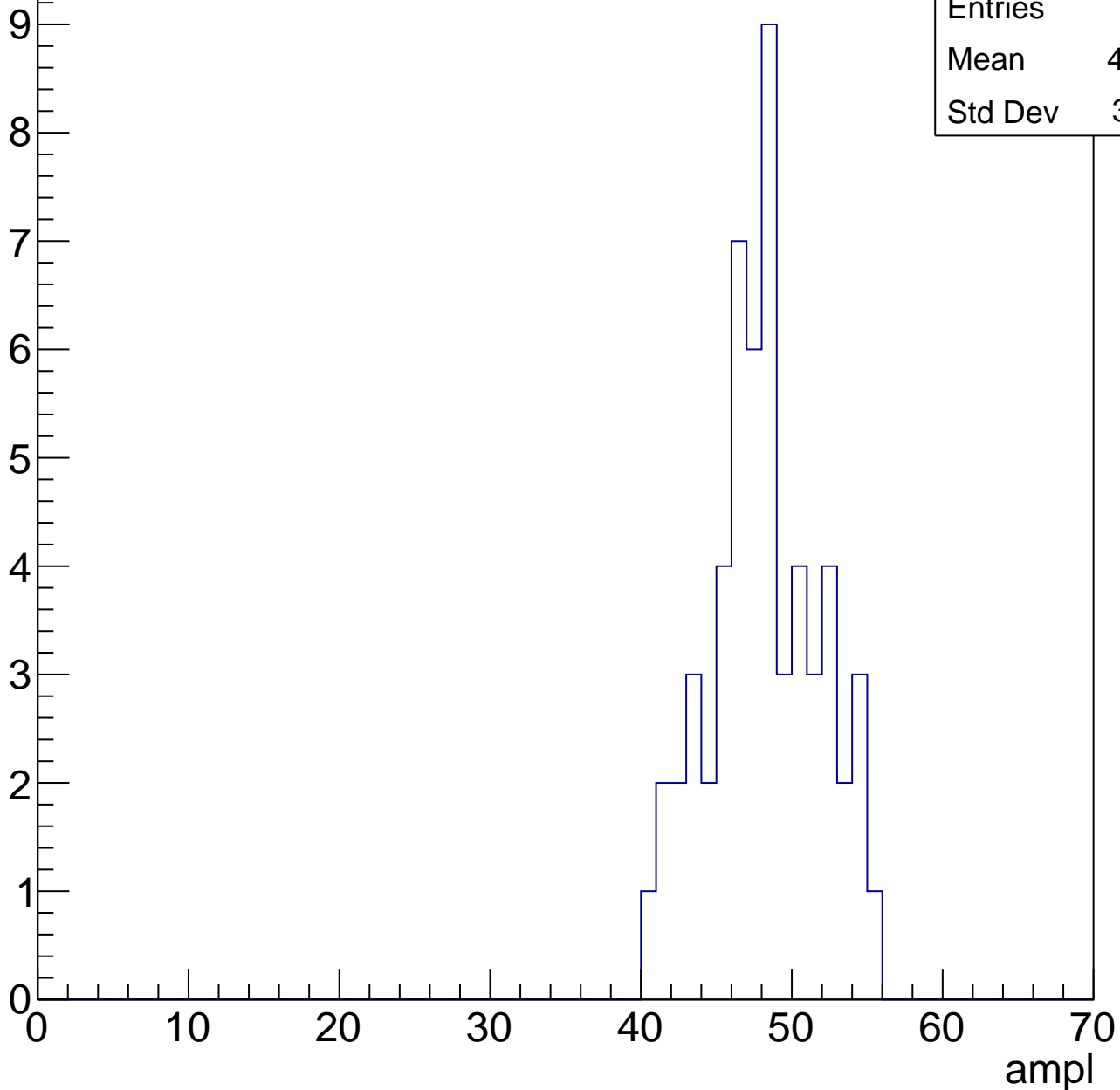


# B1L103S, U16-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	47.68
Std Dev	3.591

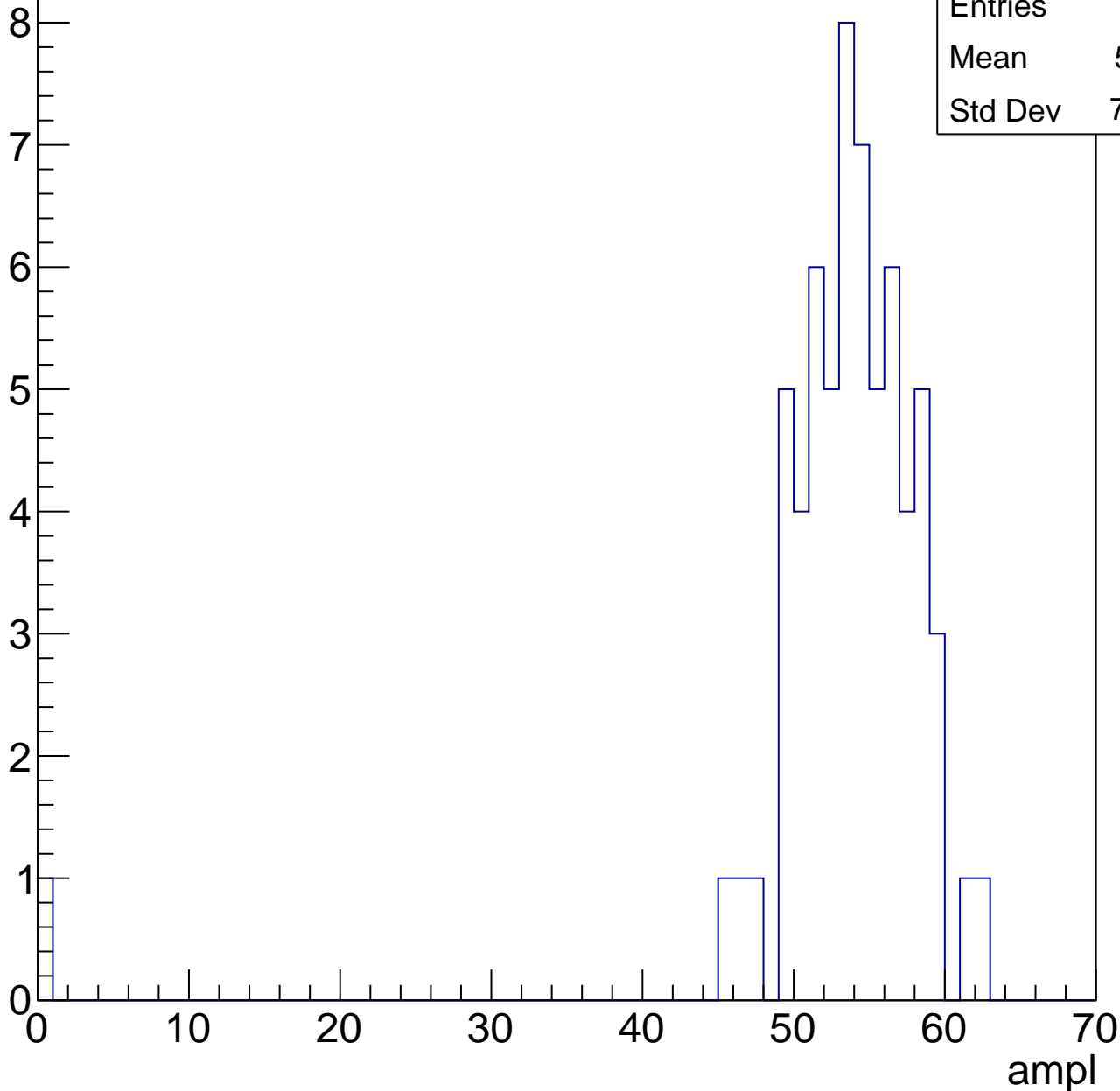


# B1L103S, U16-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	52.81
Std Dev	7.525

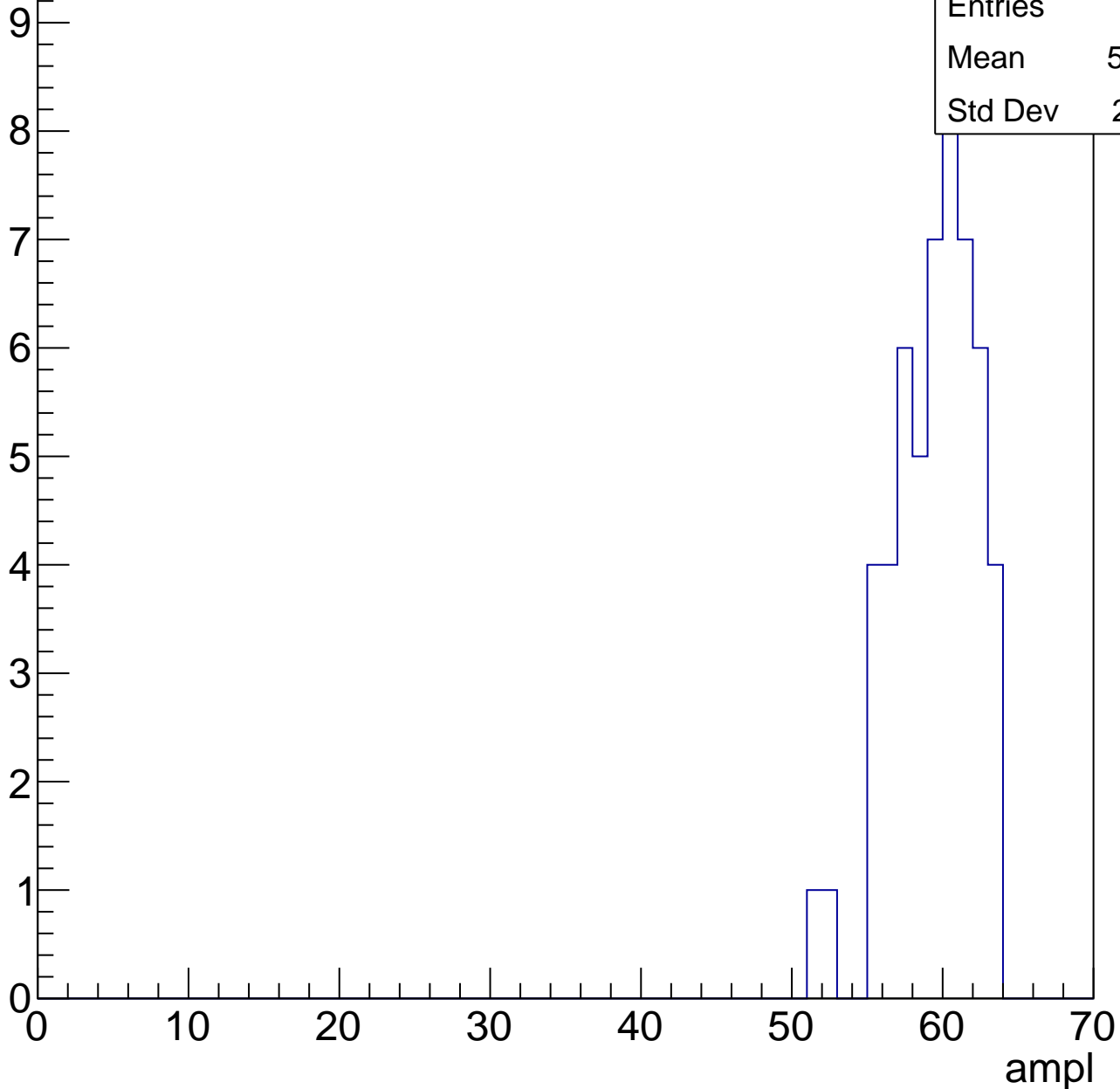


# B1L103S, U16-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	58.94
Std Dev	2.711

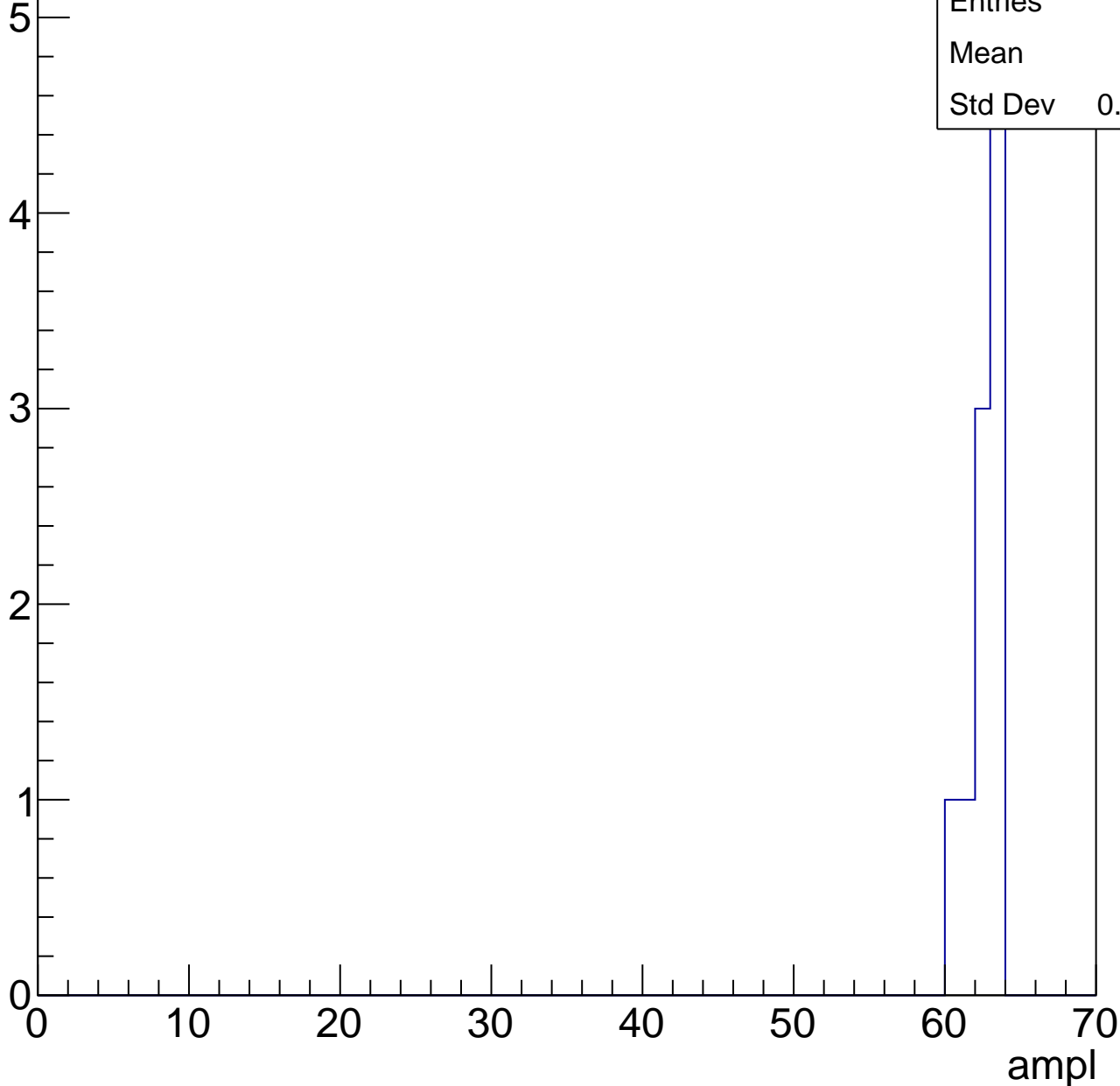


# B1L103S, U16-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	10
Mean	62.2
Std Dev	0.9798

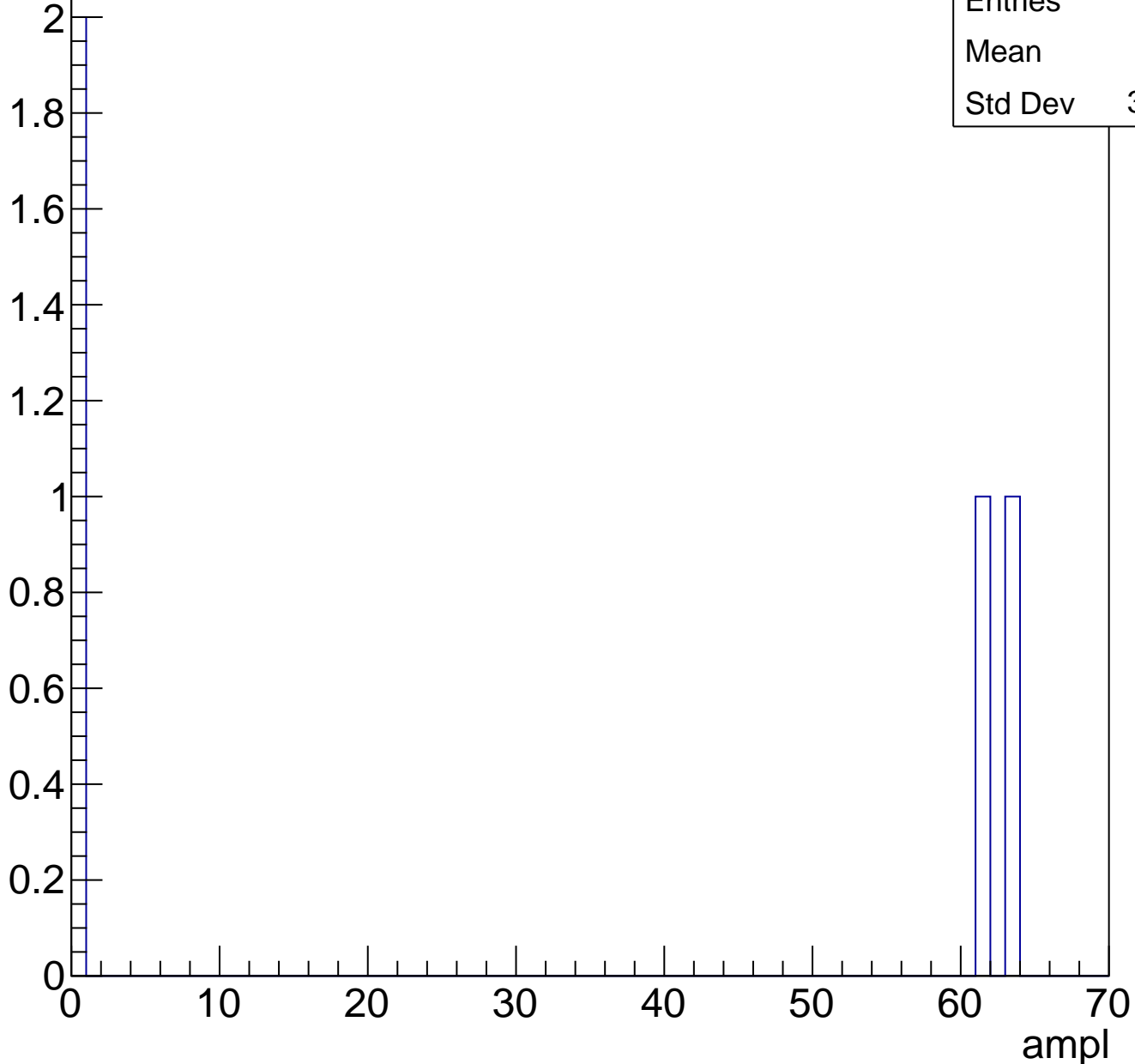




# B1L103S, U16-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	4
Mean	31
Std Dev	31.01

# B1L103S, U16-ch61, adc0

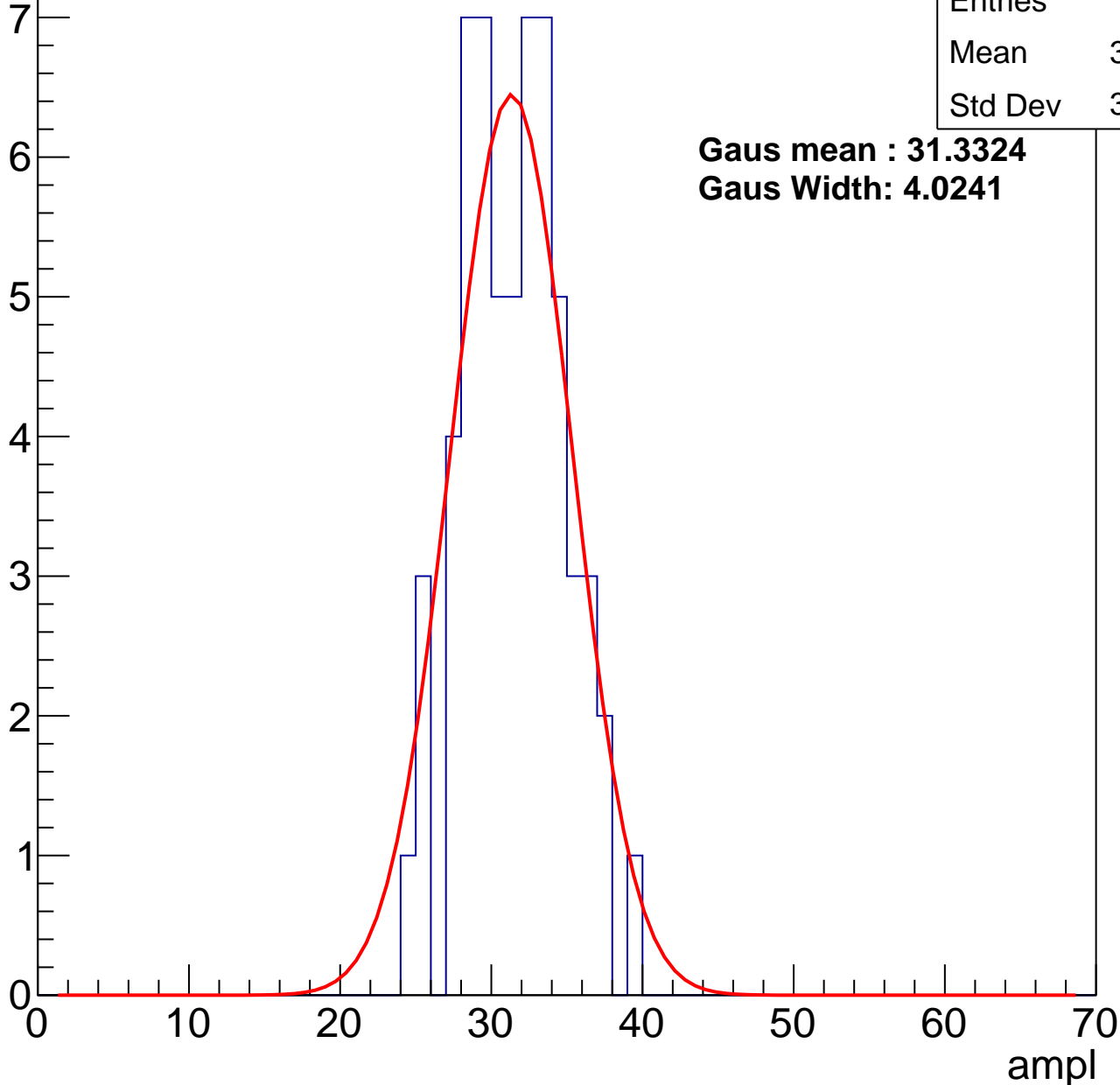
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	31.03
Std Dev	3.306

**Gaus mean : 31.3324**

**Gaus Width: 4.0241**



# B1L103S, U16-ch61, adc1

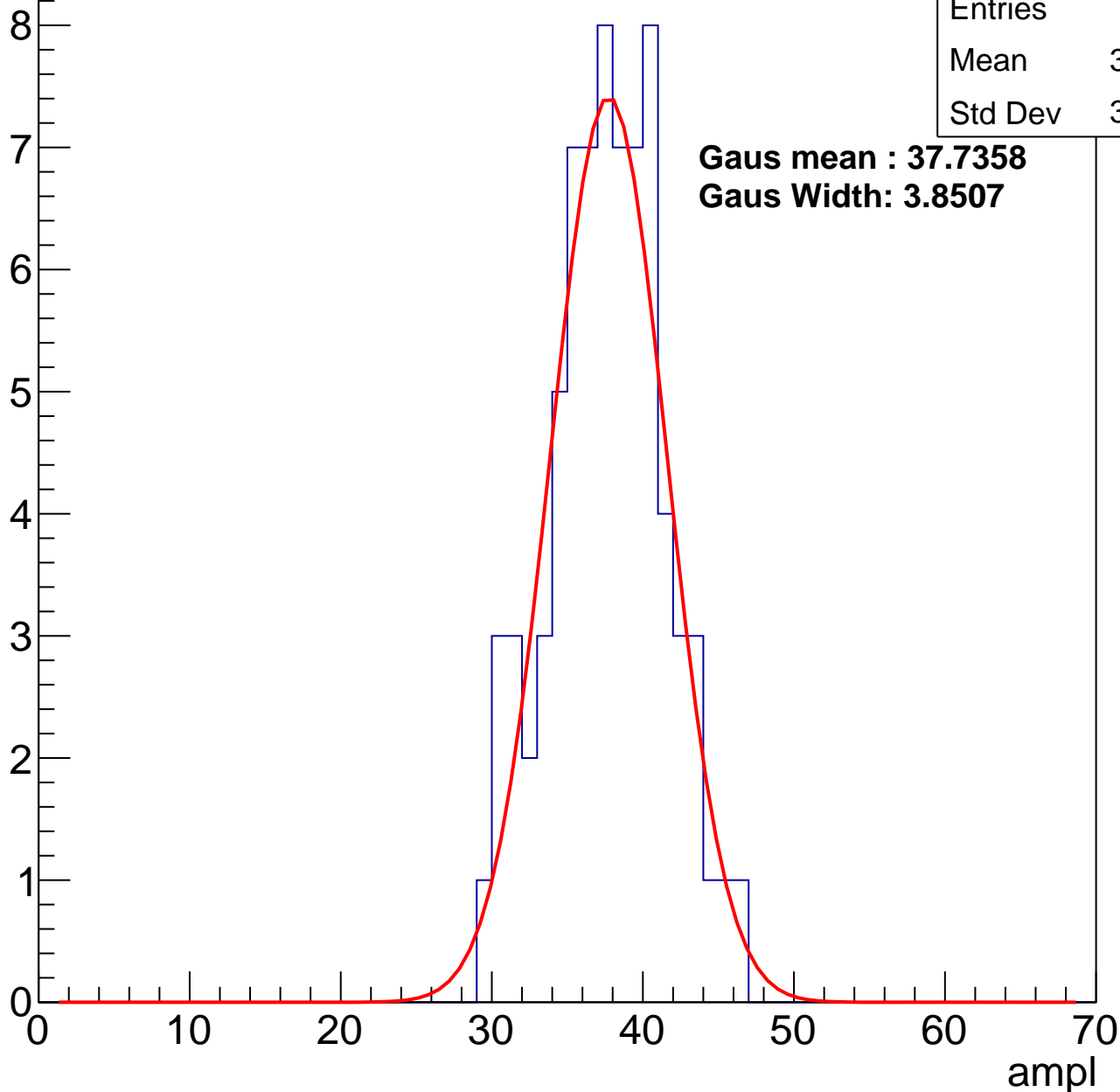
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	37.18
Std Dev	3.754

**Gaus mean : 37.7358**

**Gaus Width: 3.8507**



# B1L103S, U16-ch61, adc2

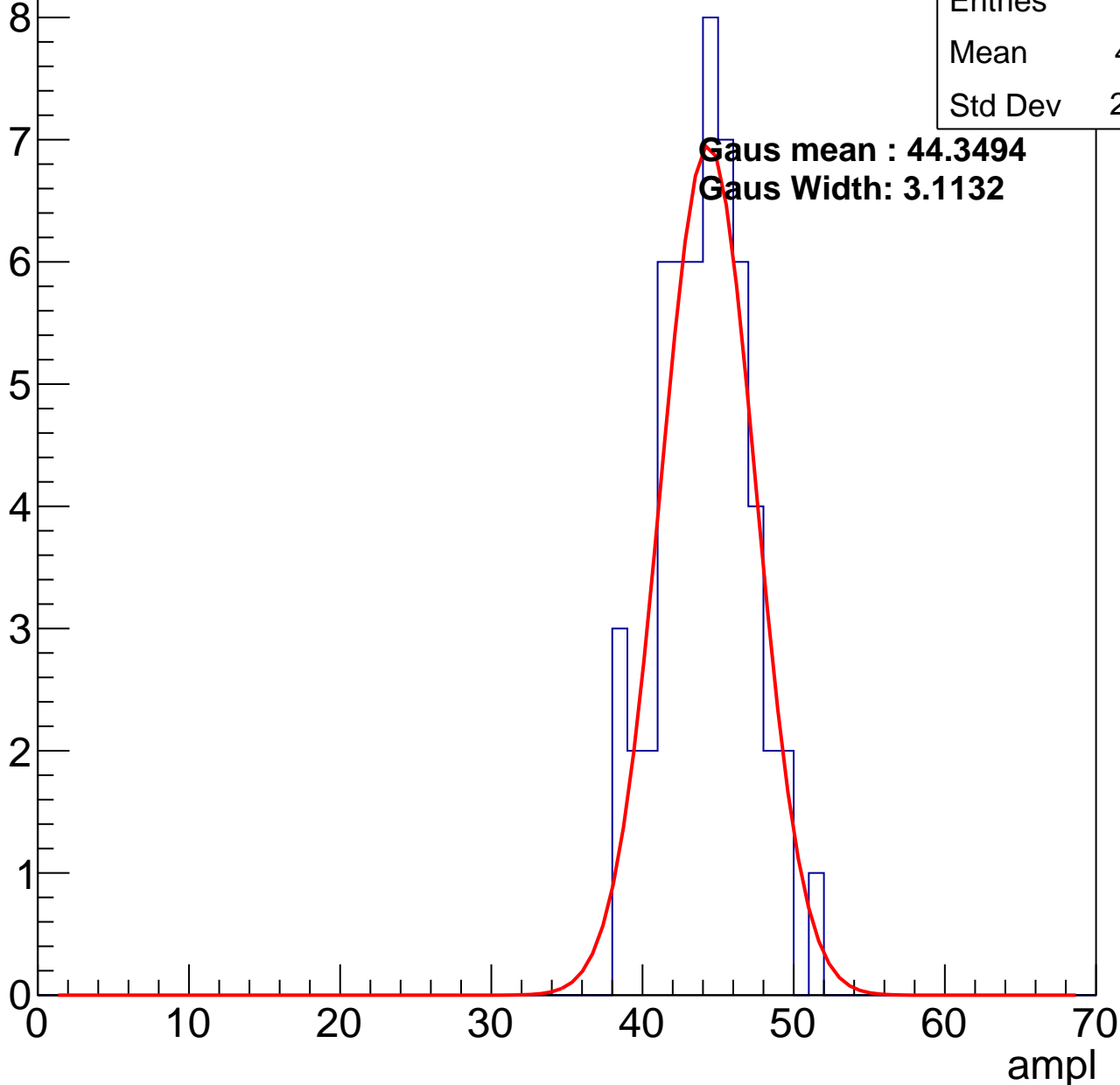
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	43.71
Std Dev	2.915

**Gaus mean : 44.3494**

**Gaus Width: 3.1132**



# B1L103S, U16-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	72
Mean	50.4
Std Dev	3.386

Entry

10

8

6

4

2

0

0

10

20

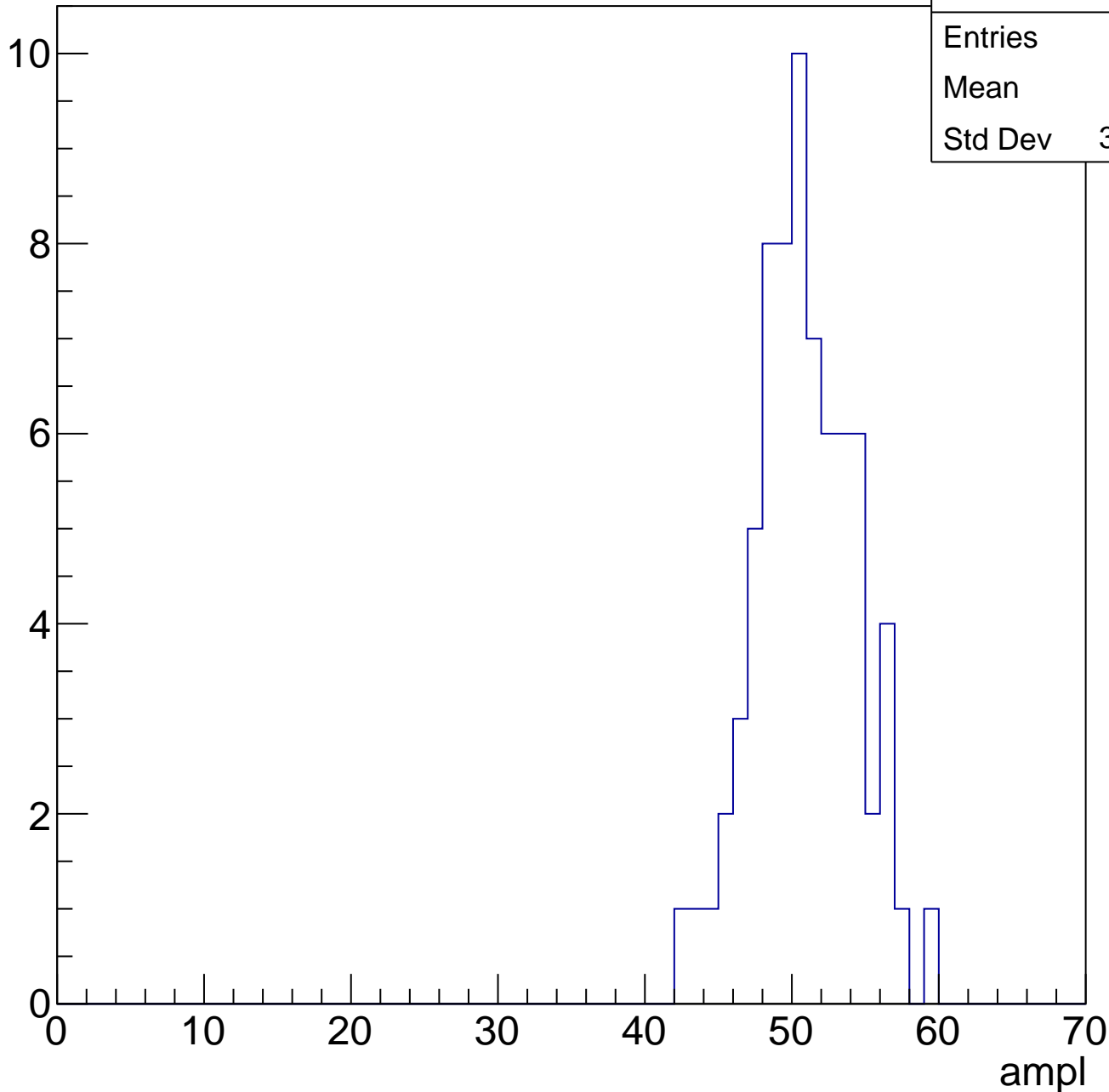
30

40

50

60

ampl

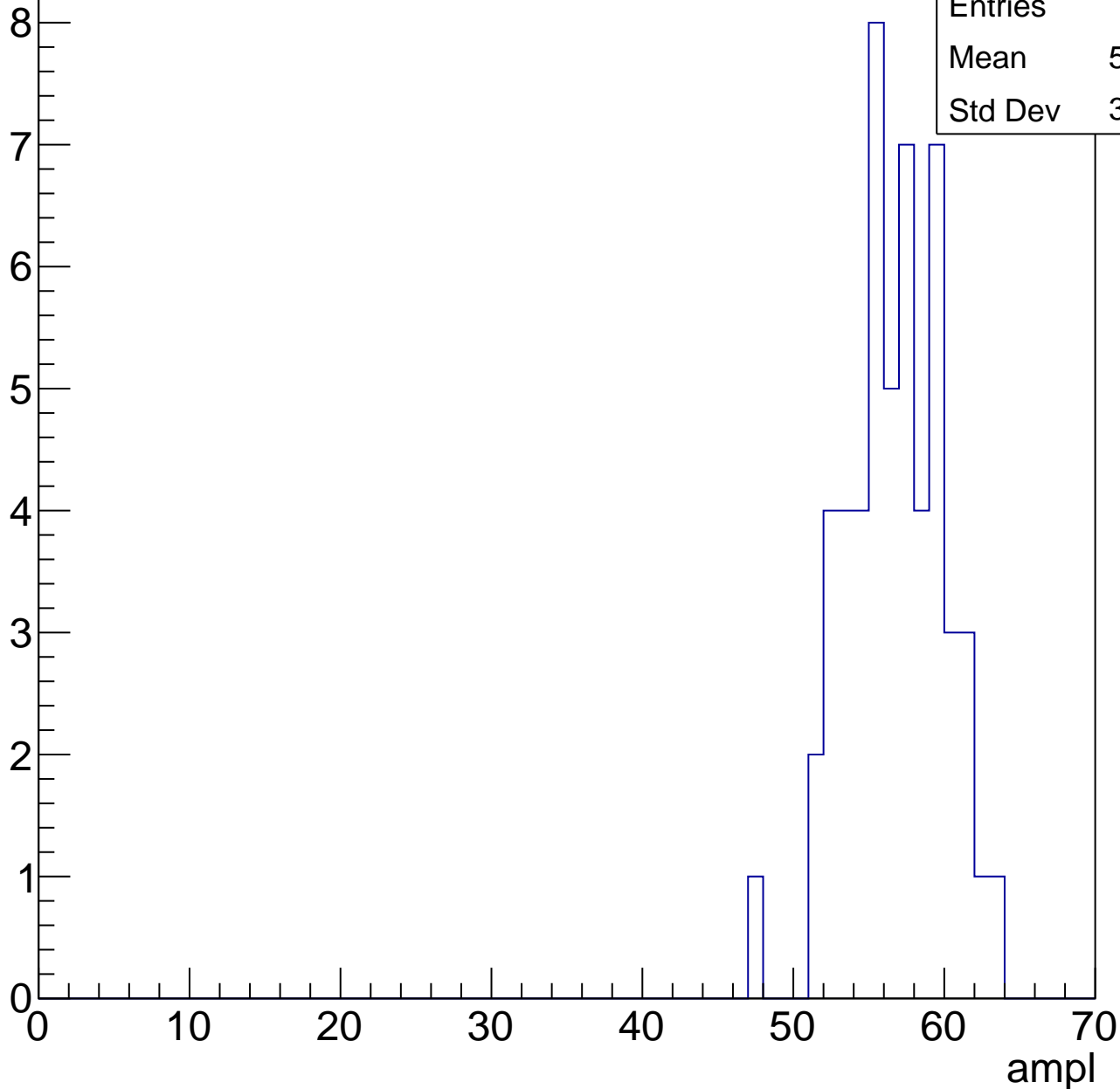


# B1L103S, U16-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	56.24
Std Dev	3.179

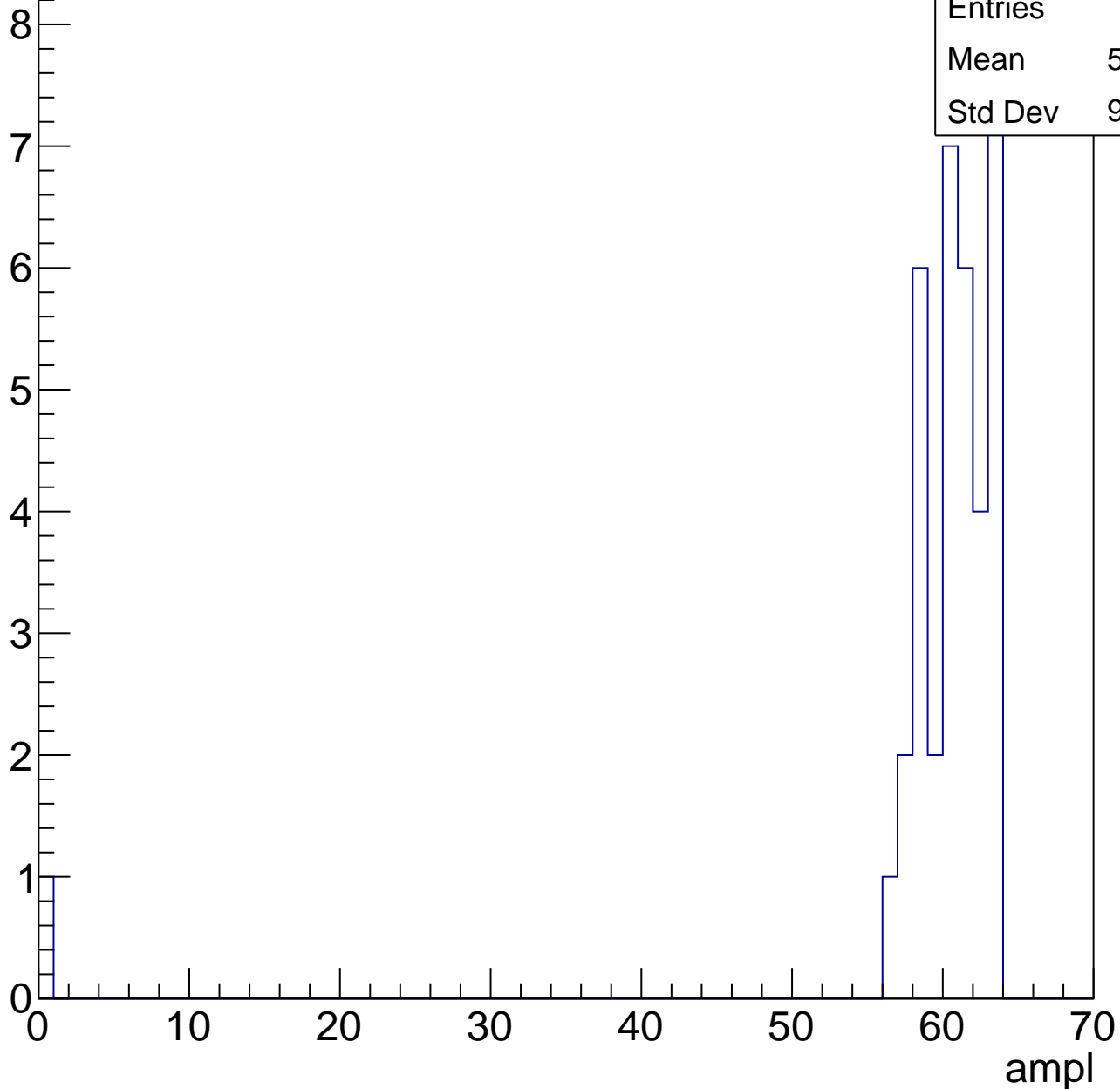


# B1L103S, U16-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	37
Mean	58.76
Std Dev	9.996

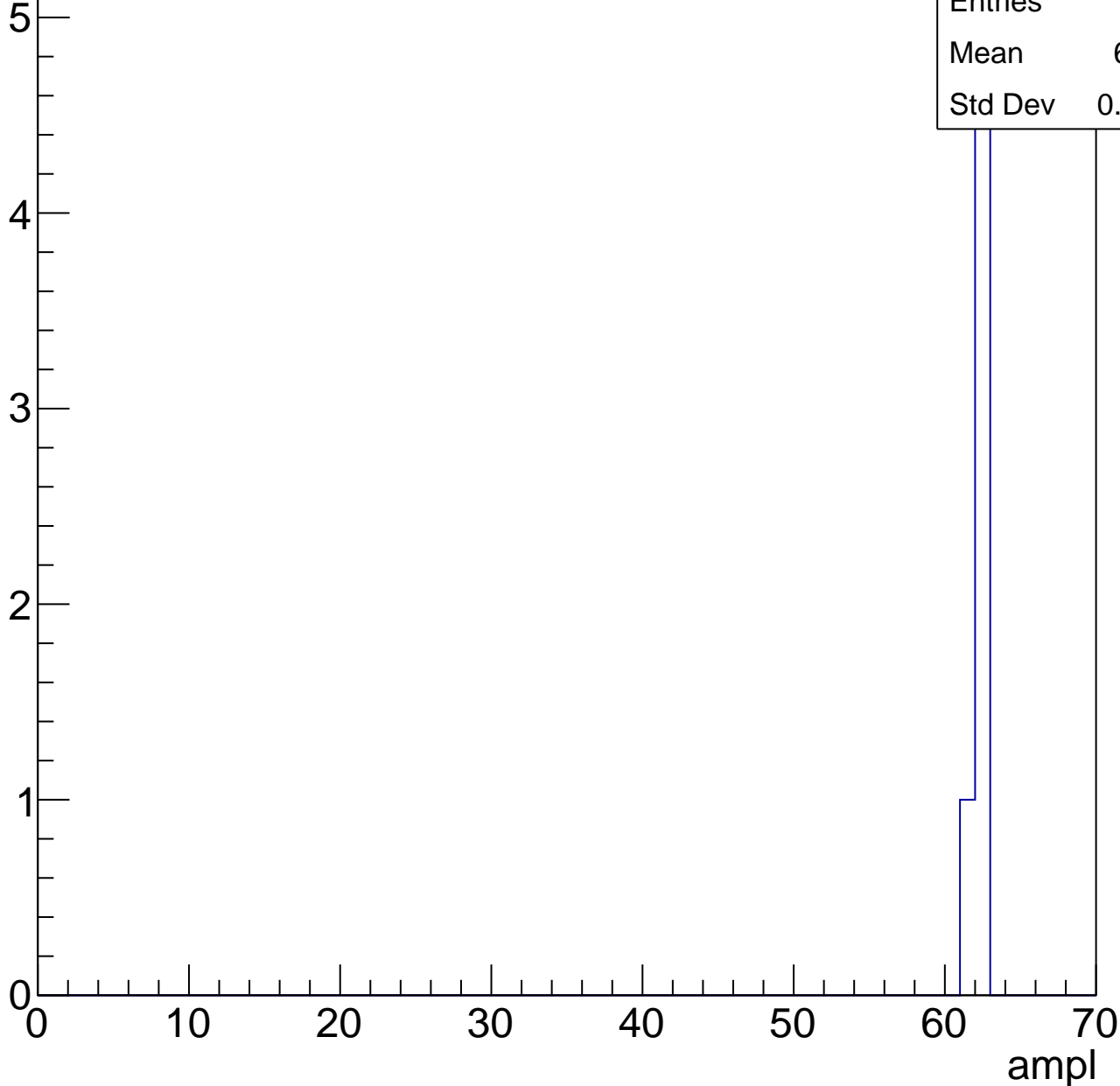


# B1L103S, U16-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	6
Mean	61.83
Std Dev	0.3727

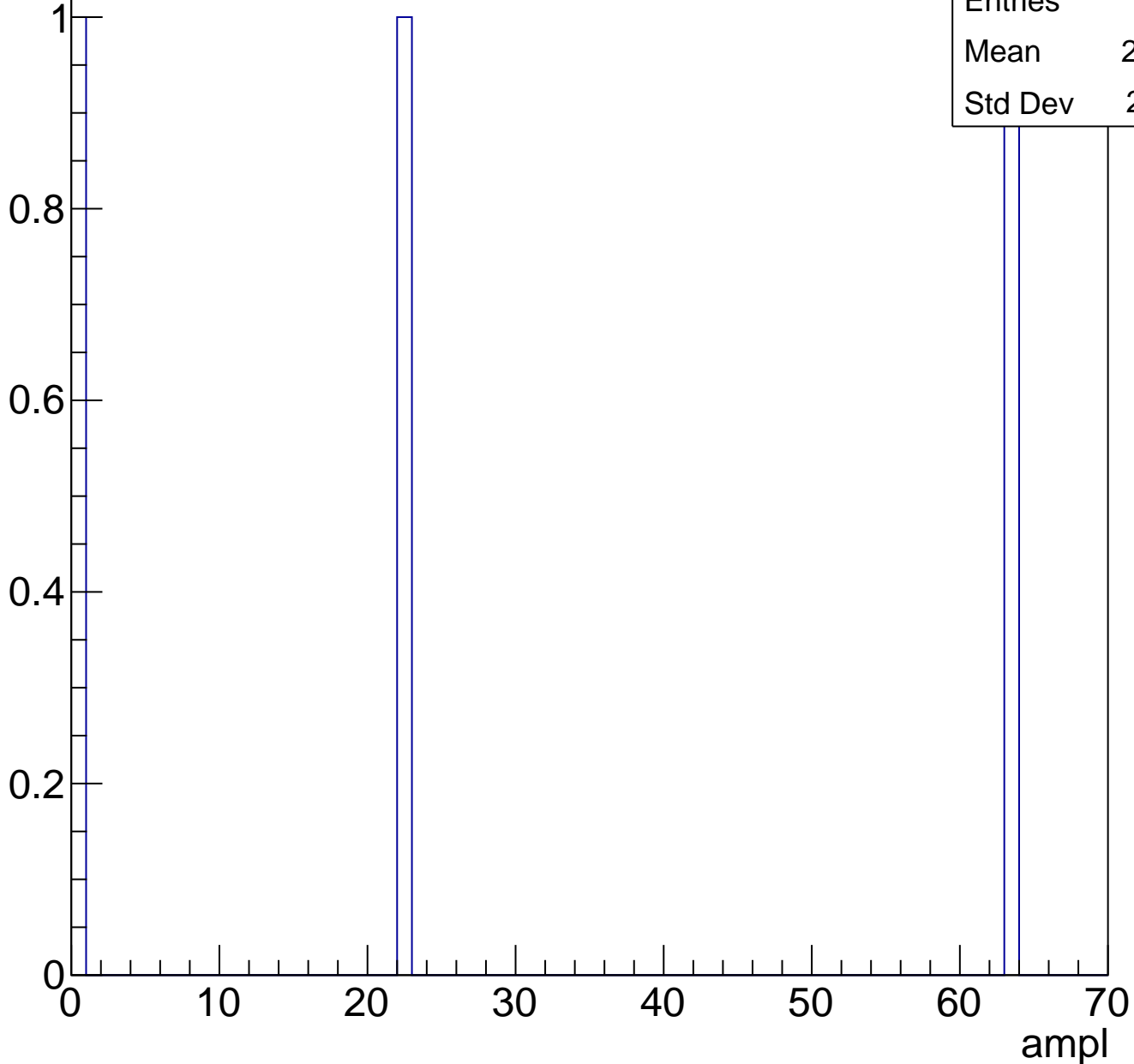




# B1L103S, U16-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	28.33
Std Dev	26.11

# B1L103S, U16-ch62, adc0

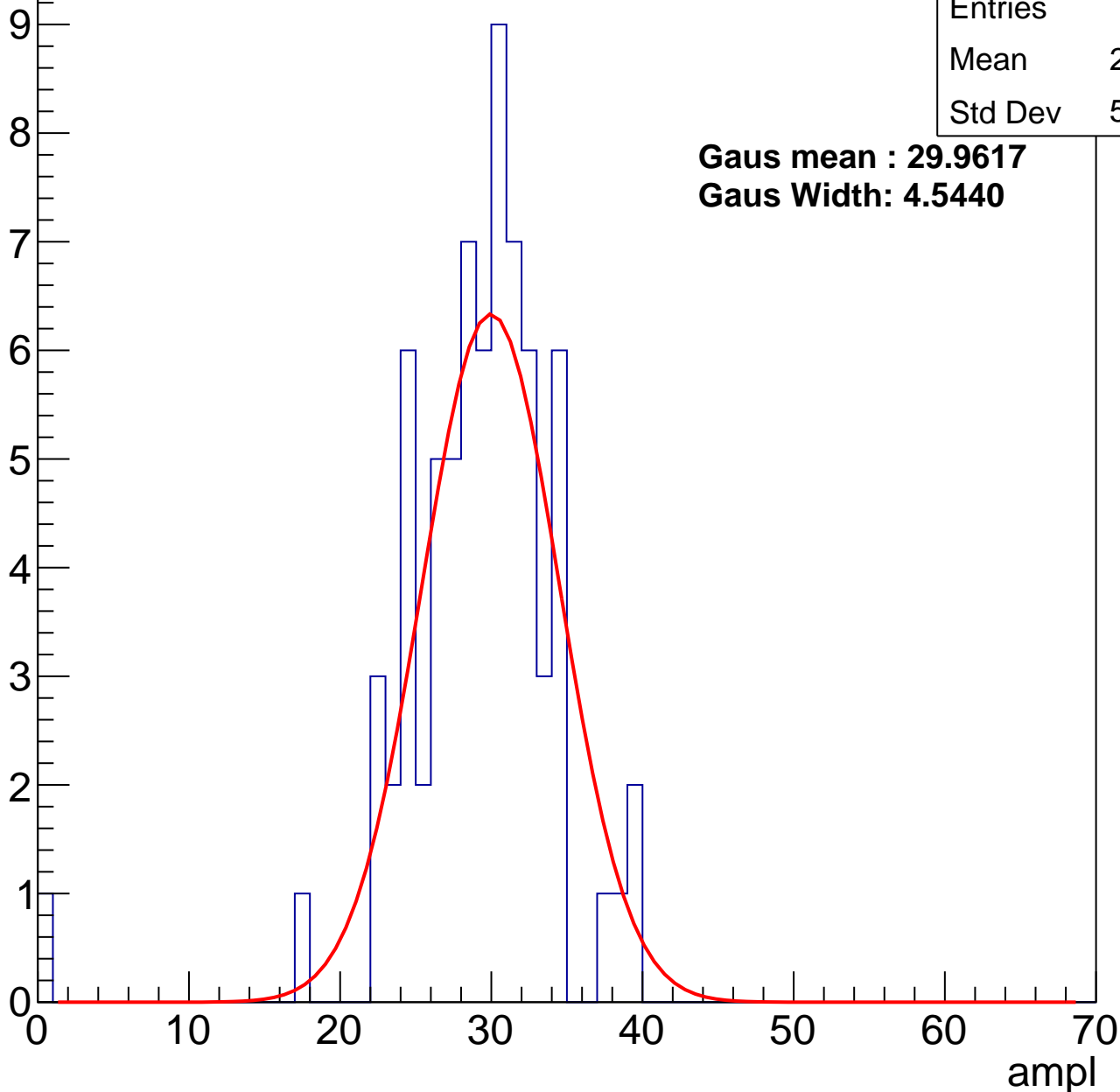
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	28.67
Std Dev	5.343

**Gaus mean : 29.9617**

**Gaus Width: 4.5440**



# B1L103S, U16-ch62, adc1

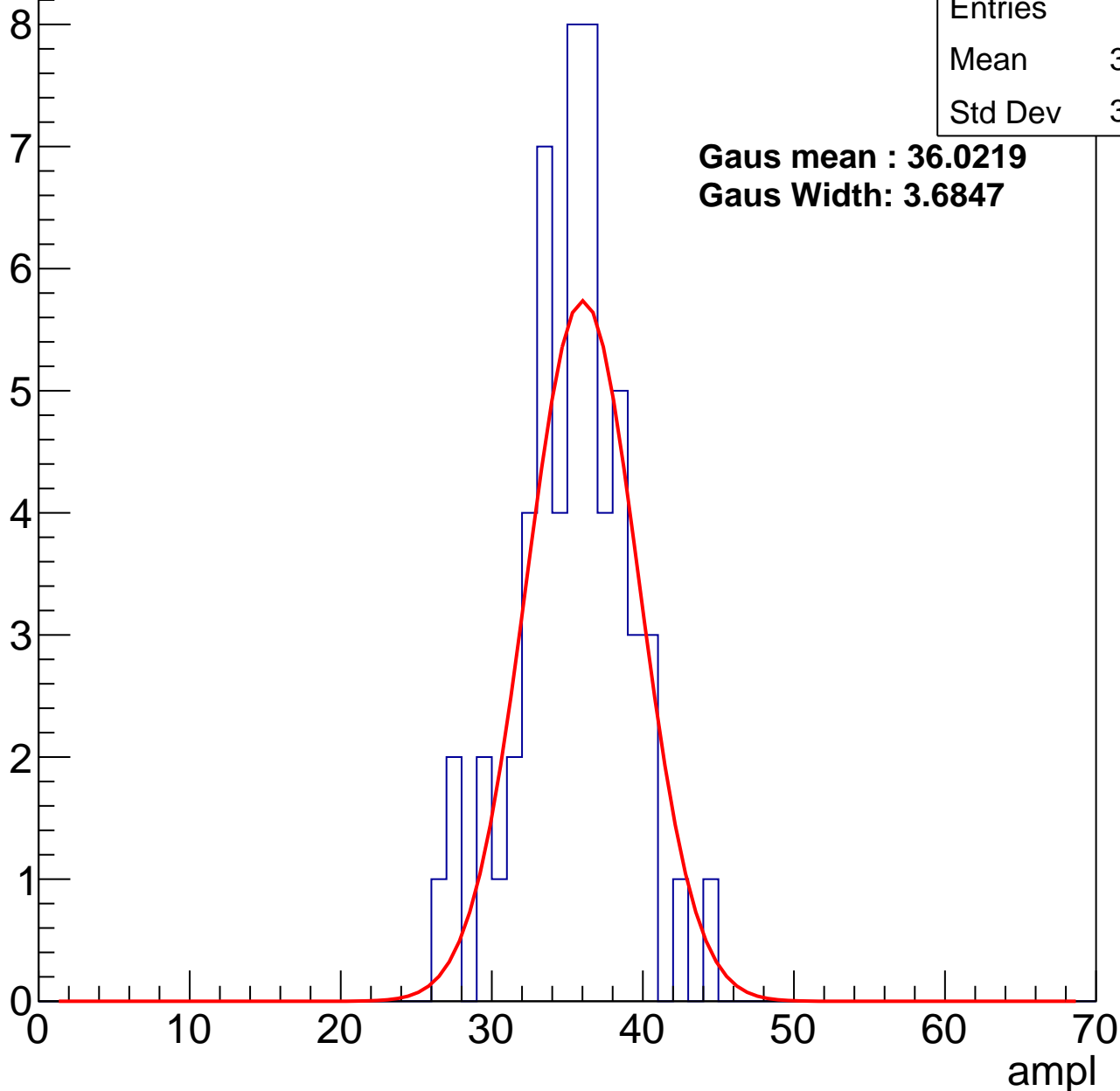
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	34.89
Std Dev	3.604

**Gaus mean : 36.0219**

**Gaus Width: 3.6847**



# B1L103S, U16-ch62, adc2

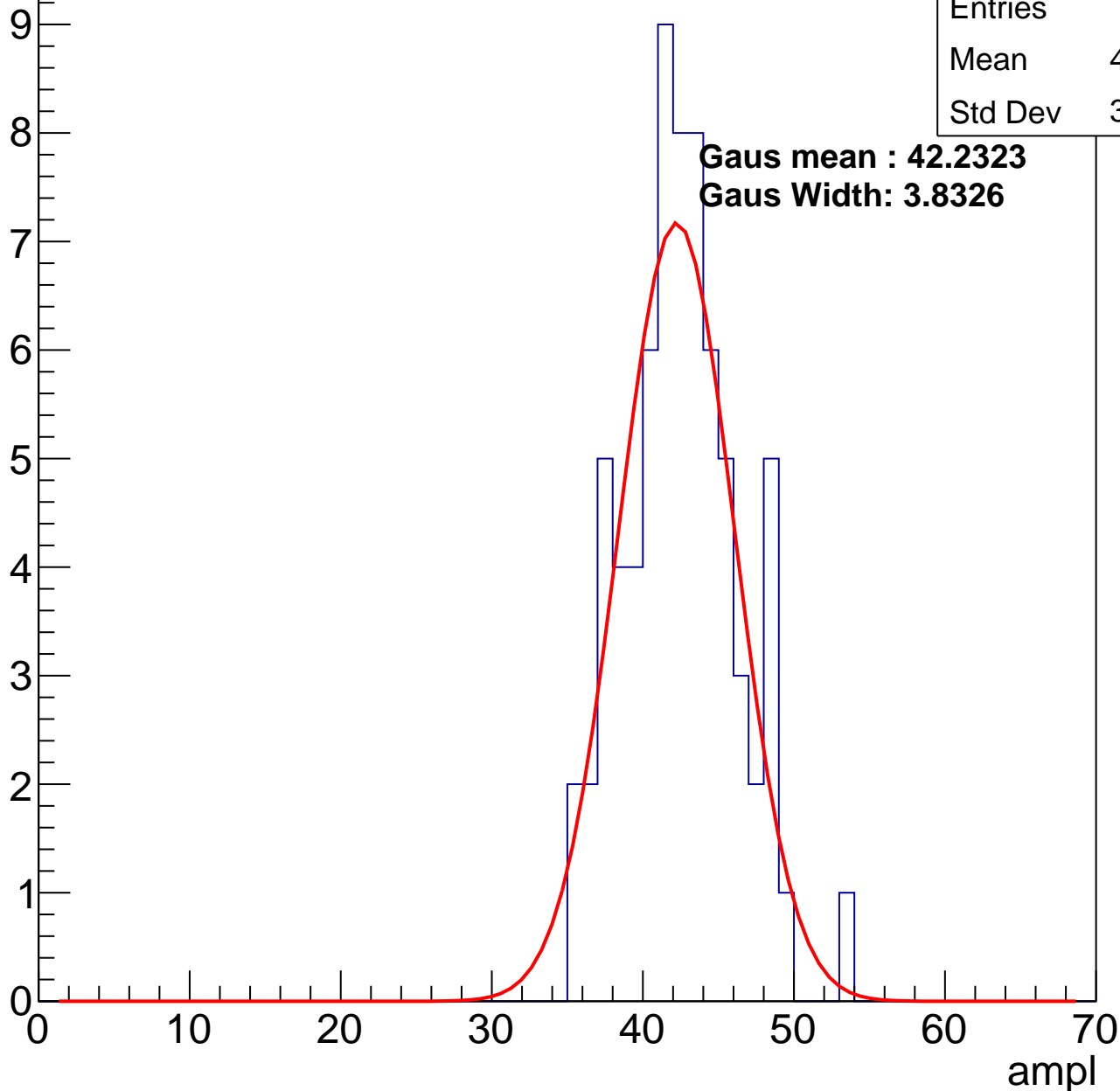
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	42.07
Std Dev	3.663

**Gaus mean : 42.2323**

**Gaus Width: 3.8326**

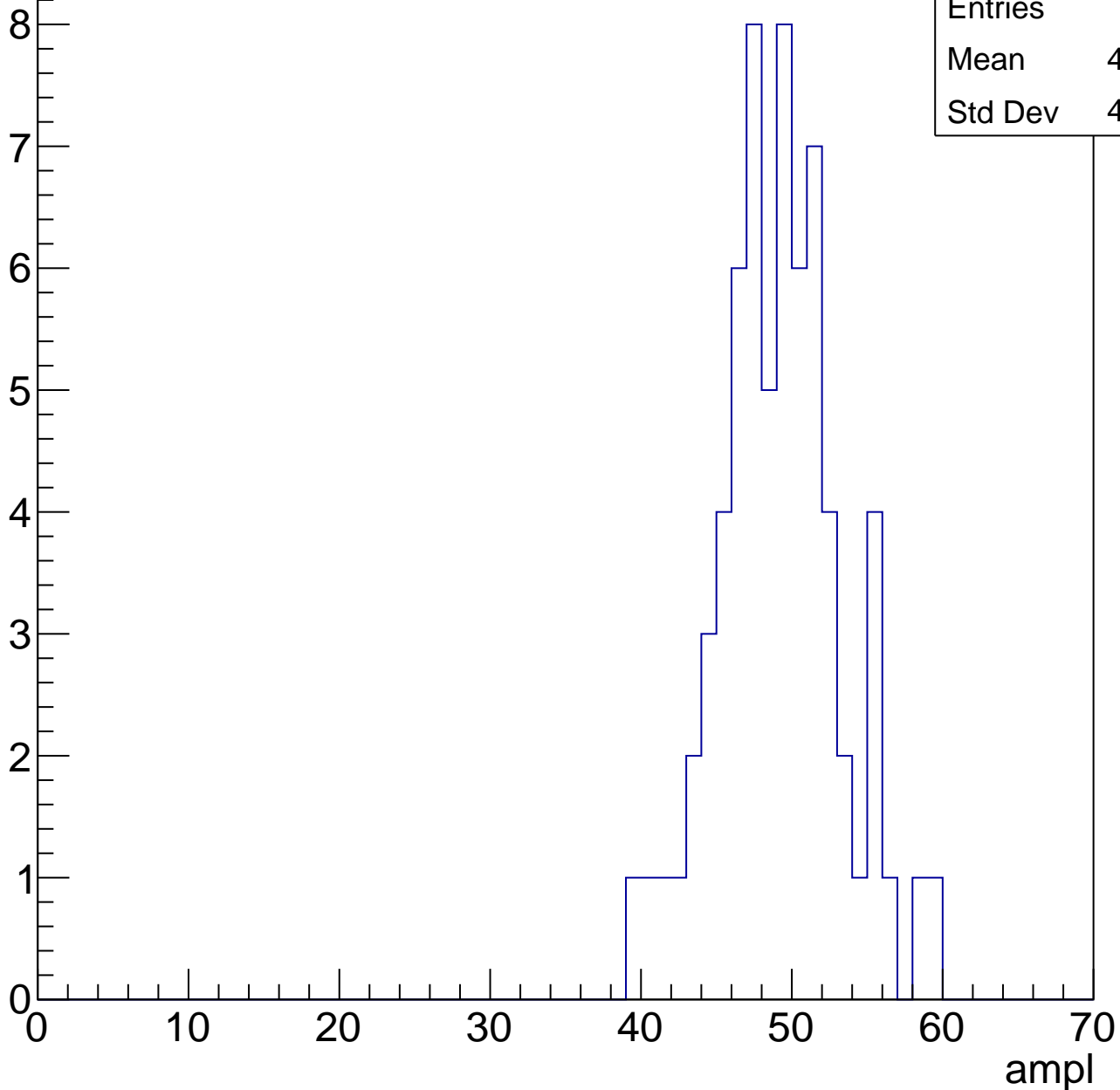


# B1L103S, U16-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	48.69
Std Dev	4.034

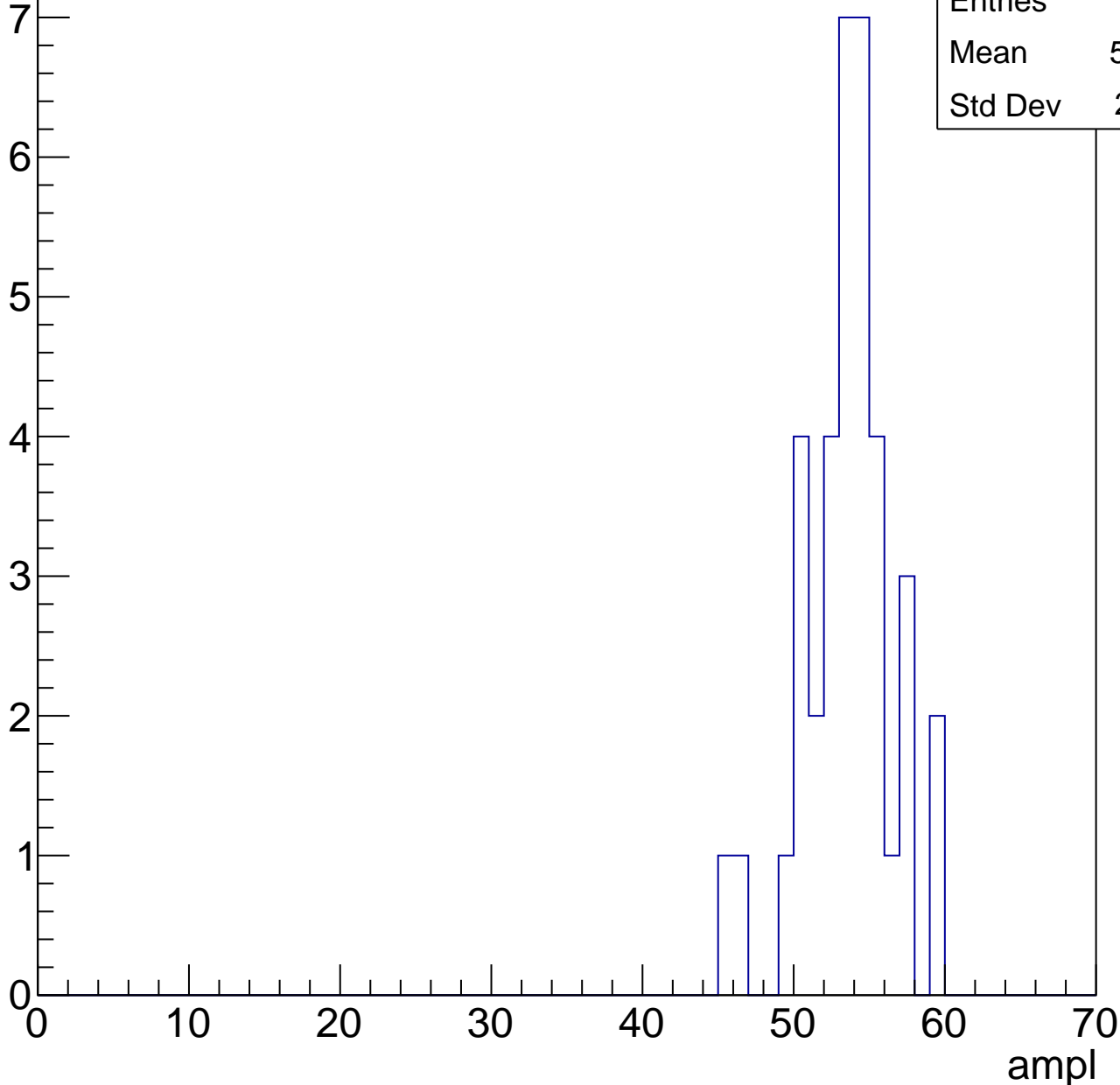


# B1L103S, U16-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	37
Mean	53.08
Std Dev	2.981

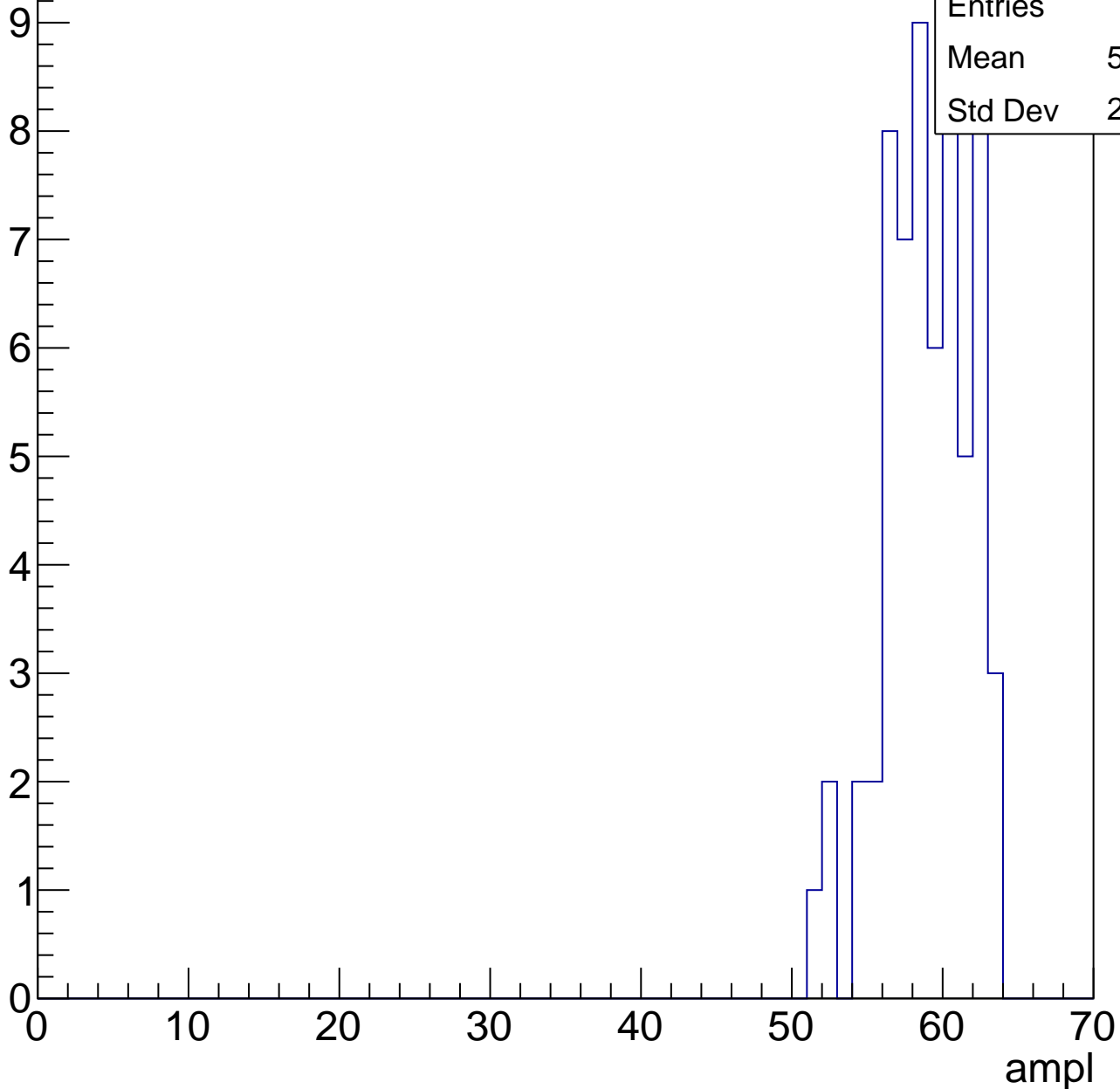


# B1L103S, U16-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	58.46
Std Dev	2.814

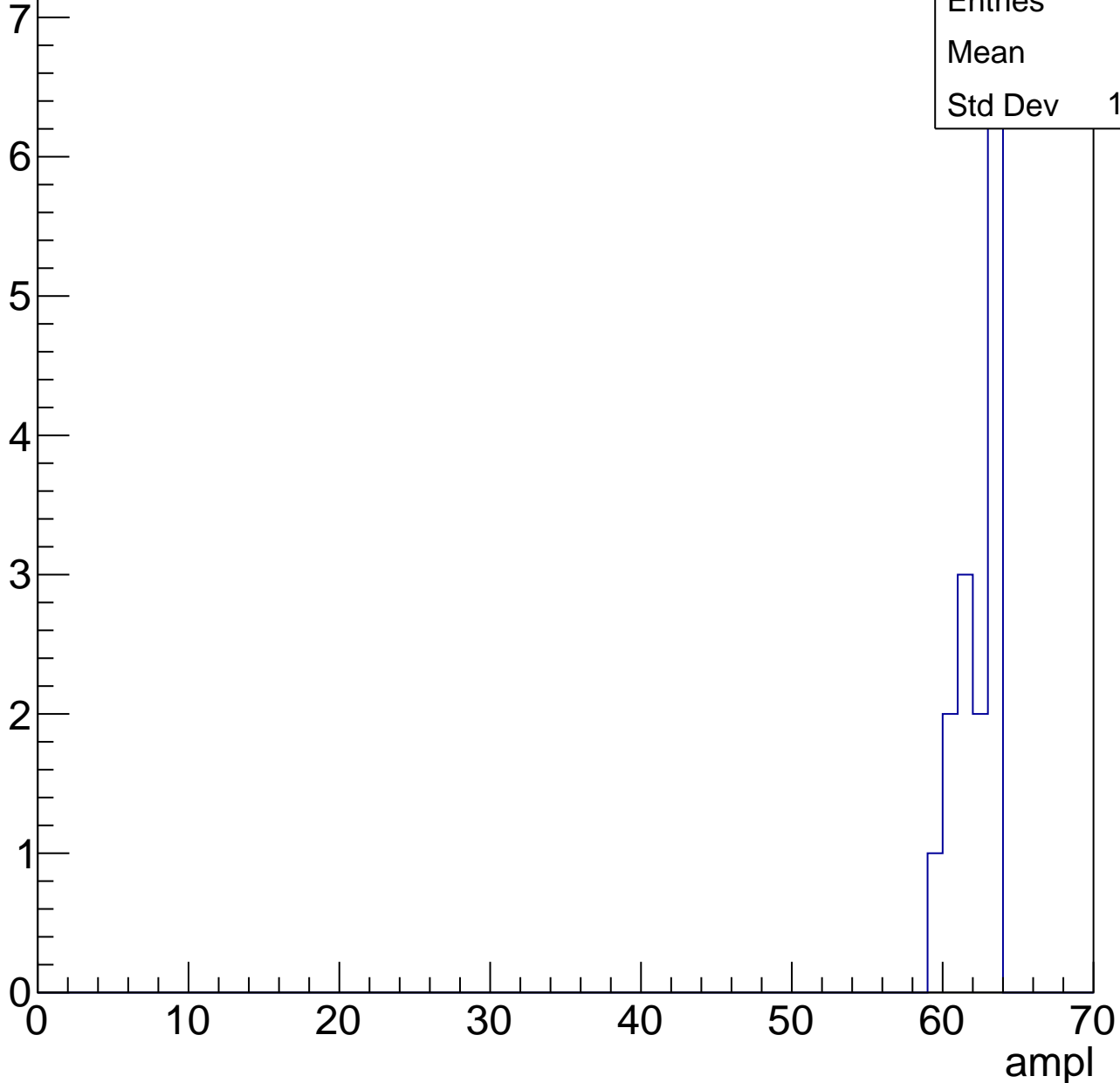


# B1L103S, U16-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	15
Mean	61.8
Std Dev	1.327

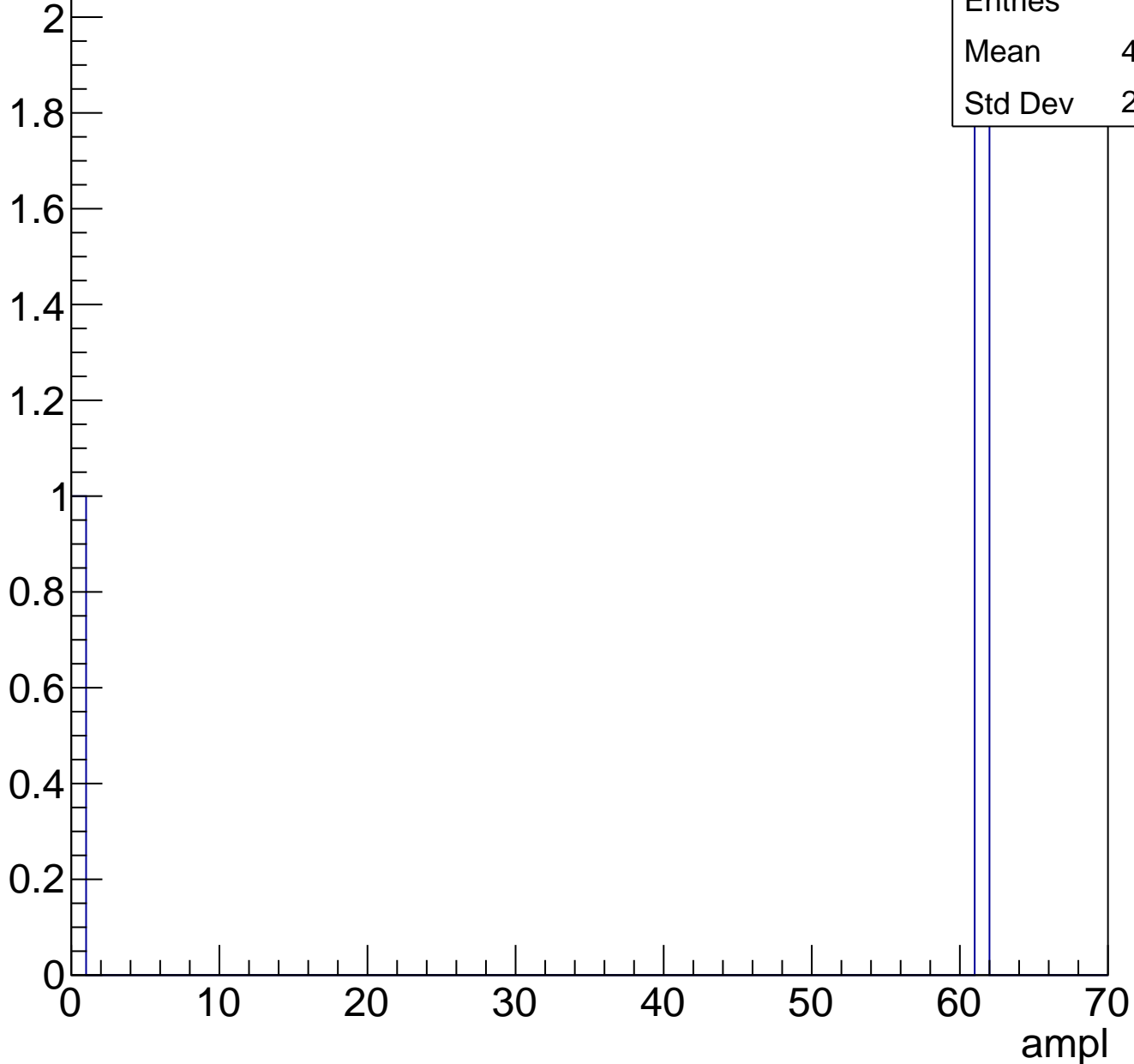




# B1L103S, U16-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch63, adc0

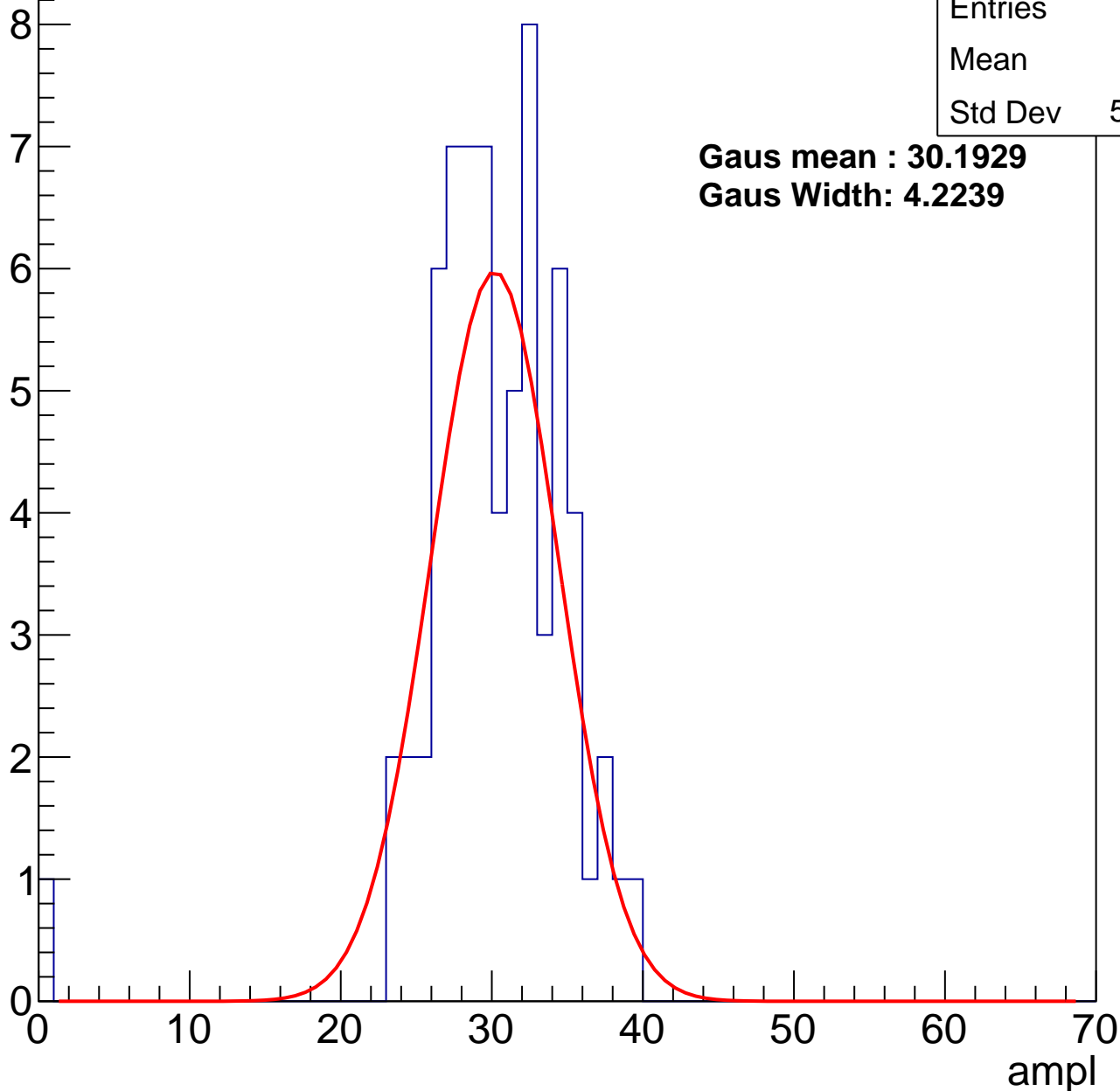
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	29.7
Std Dev	5.173

**Gaus mean : 30.1929**

**Gaus Width: 4.2239**



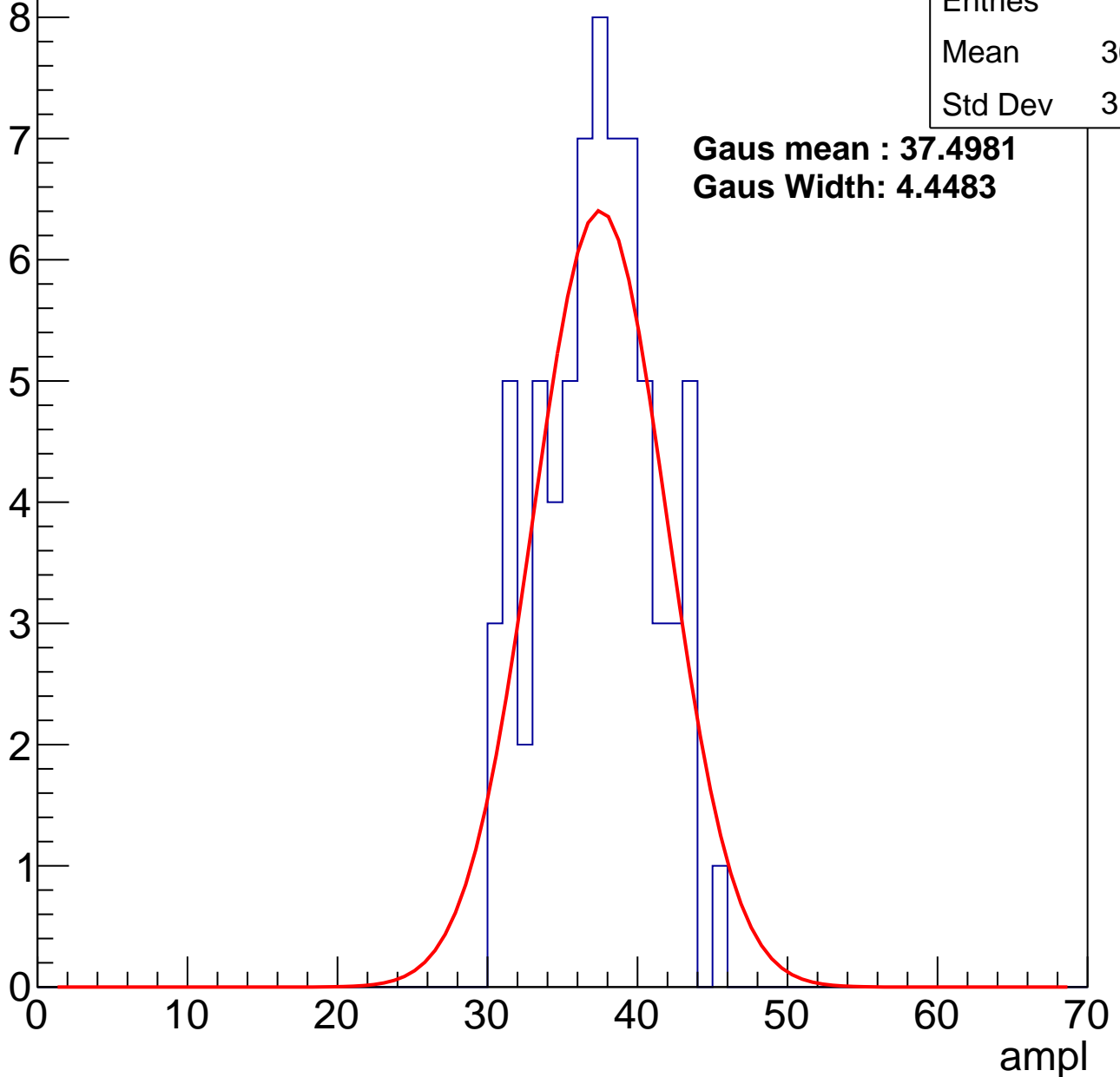
# B1L103S, U16-ch63, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	36.87
Std Dev	3.715

**Gaus mean : 37.4981**  
**Gaus Width: 4.4483**



# B1L103S, U16-ch63, adc2

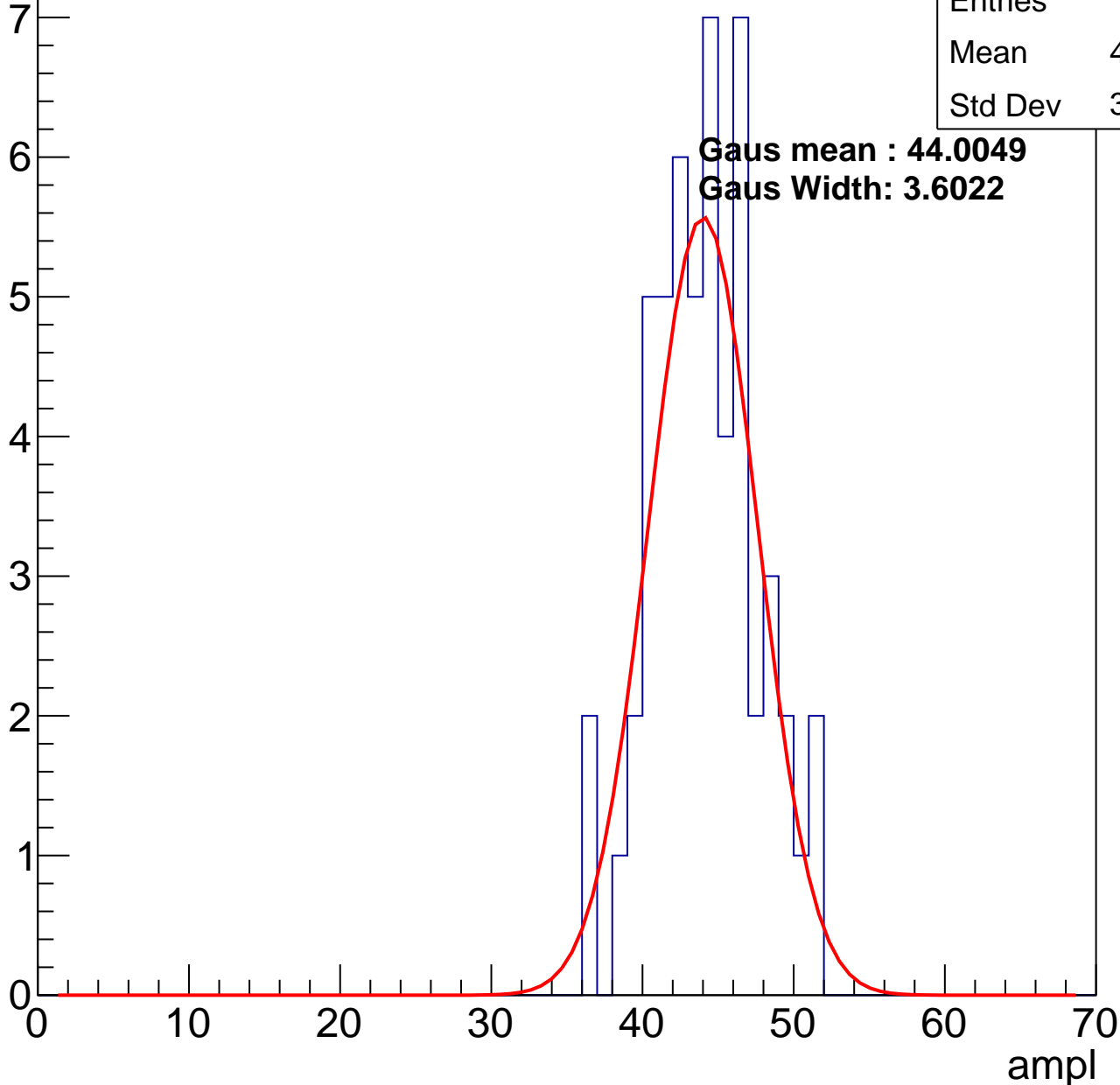
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	43.67
Std Dev	3.453

**Gaus mean : 44.0049**

**Gaus Width: 3.6022**

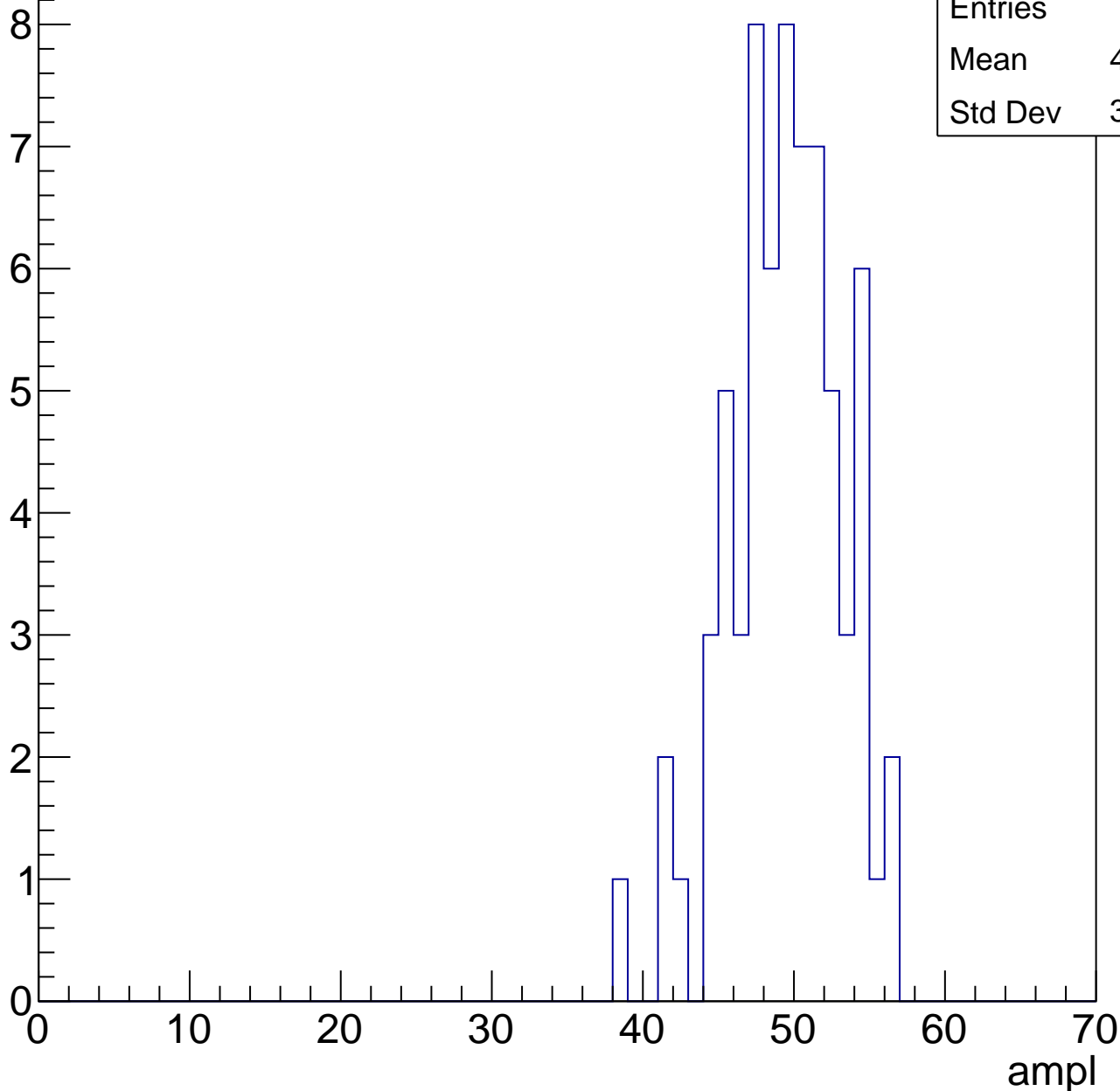


# B1L103S, U16-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

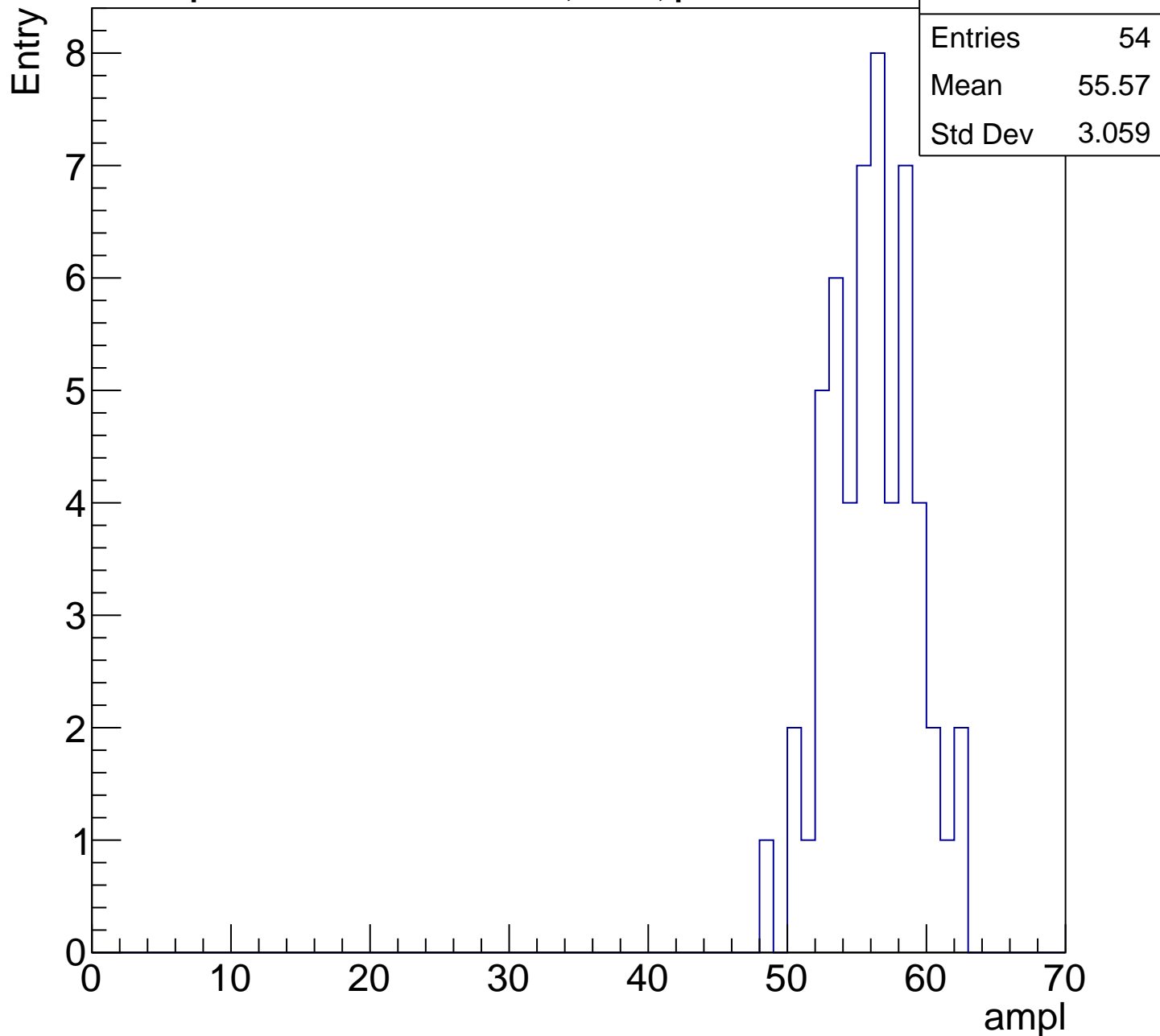
Entry

Entries	68
Mean	48.97
Std Dev	3.698



# B1L103S, U16-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

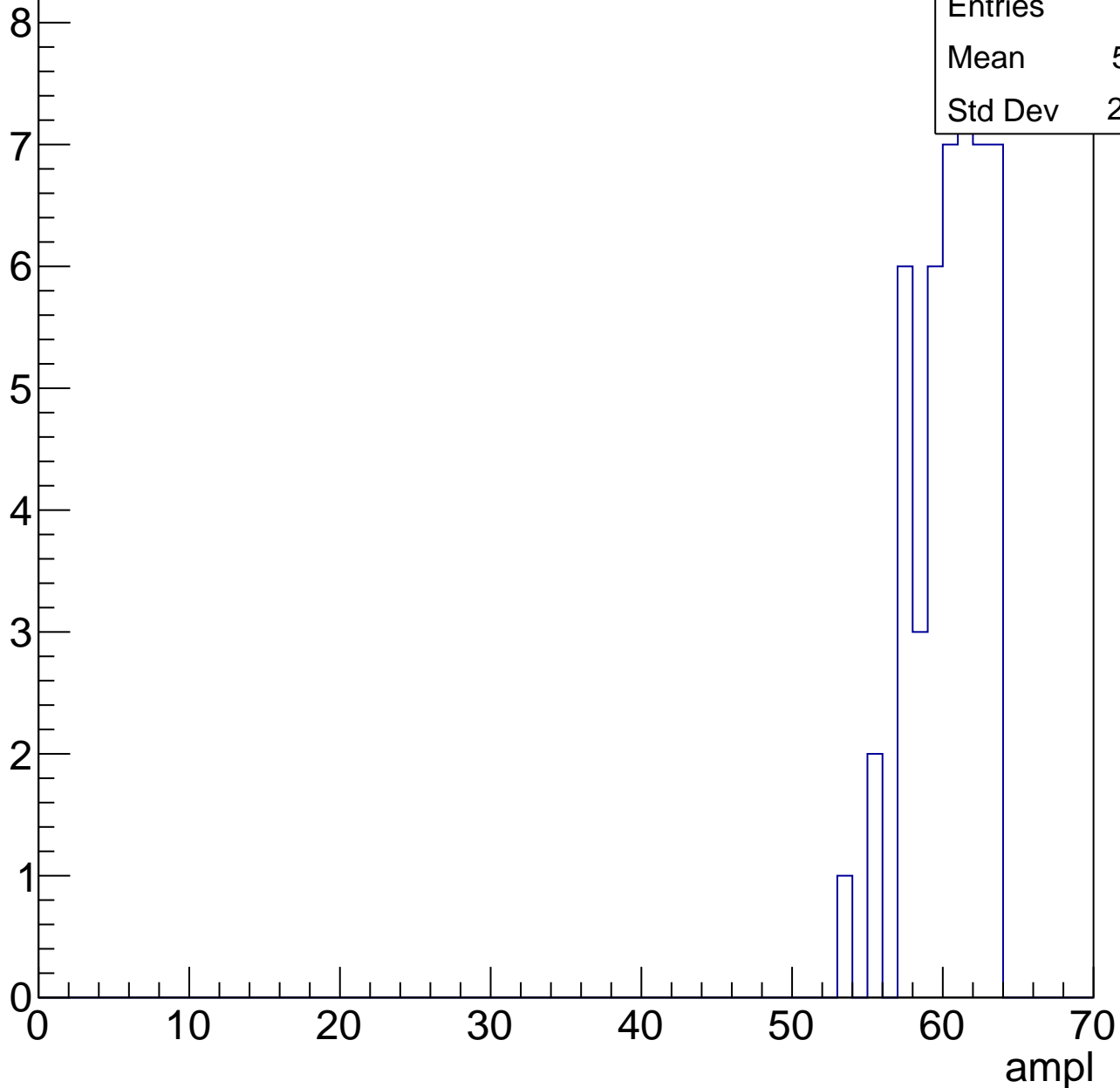


# B1L103S, U16-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

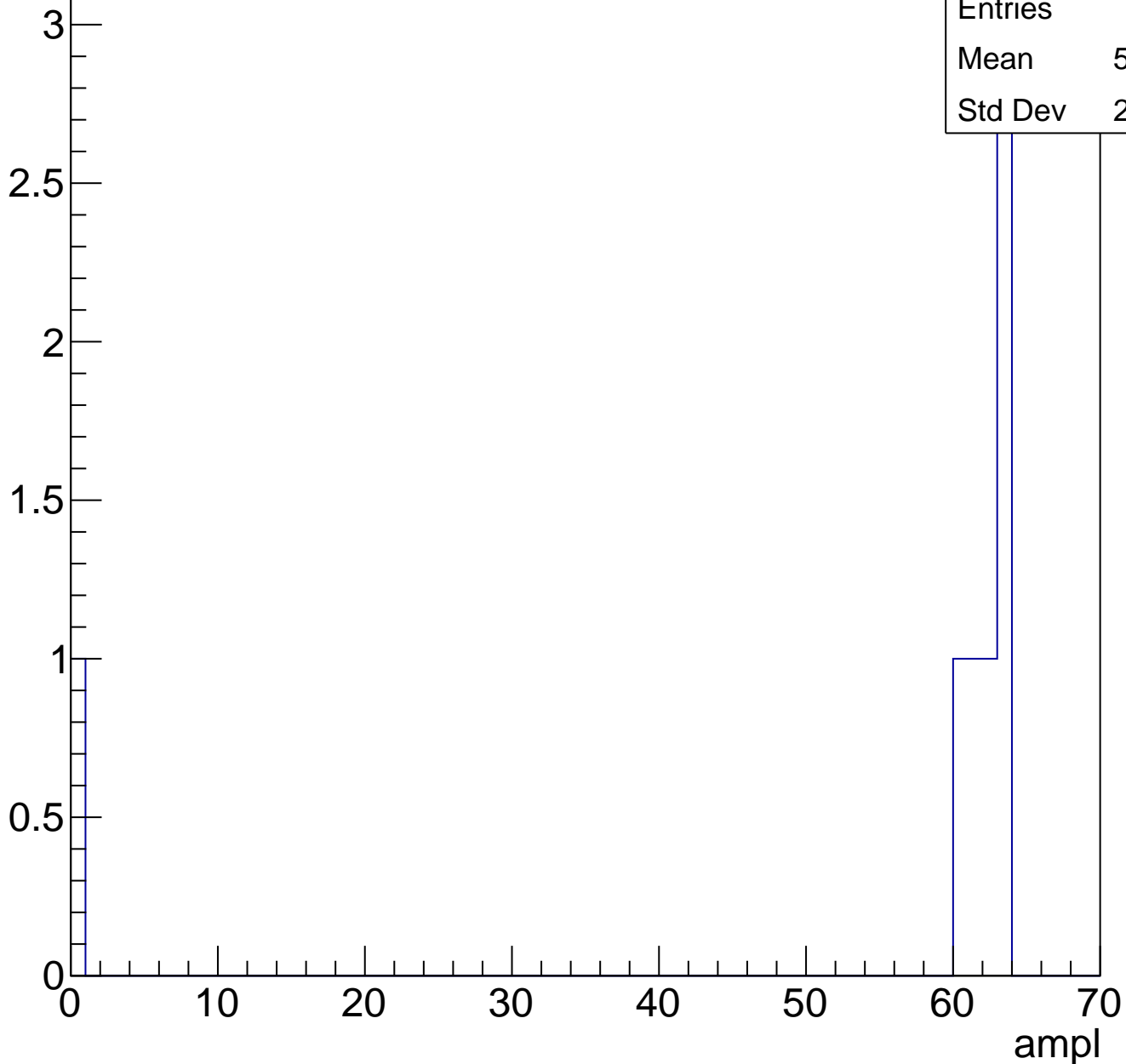
Entries	47
Mean	59.91
Std Dev	2.395



# B1L103S, U16-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U16-ch64, adc0

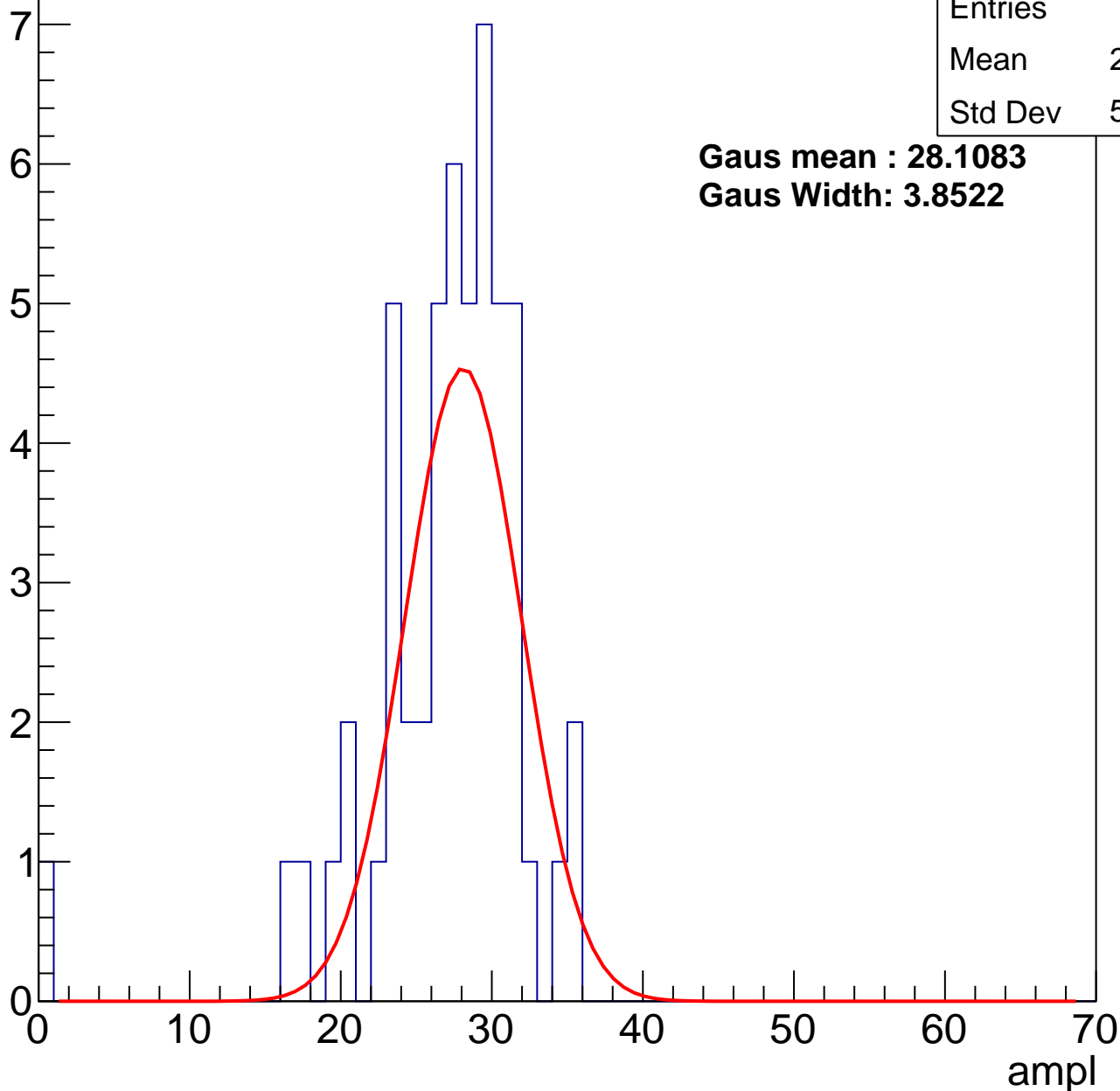
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	26.47
Std Dev	5.483

**Gaus mean : 28.1083**

**Gaus Width: 3.8522**



# B1L103S, U16-ch64, adc1

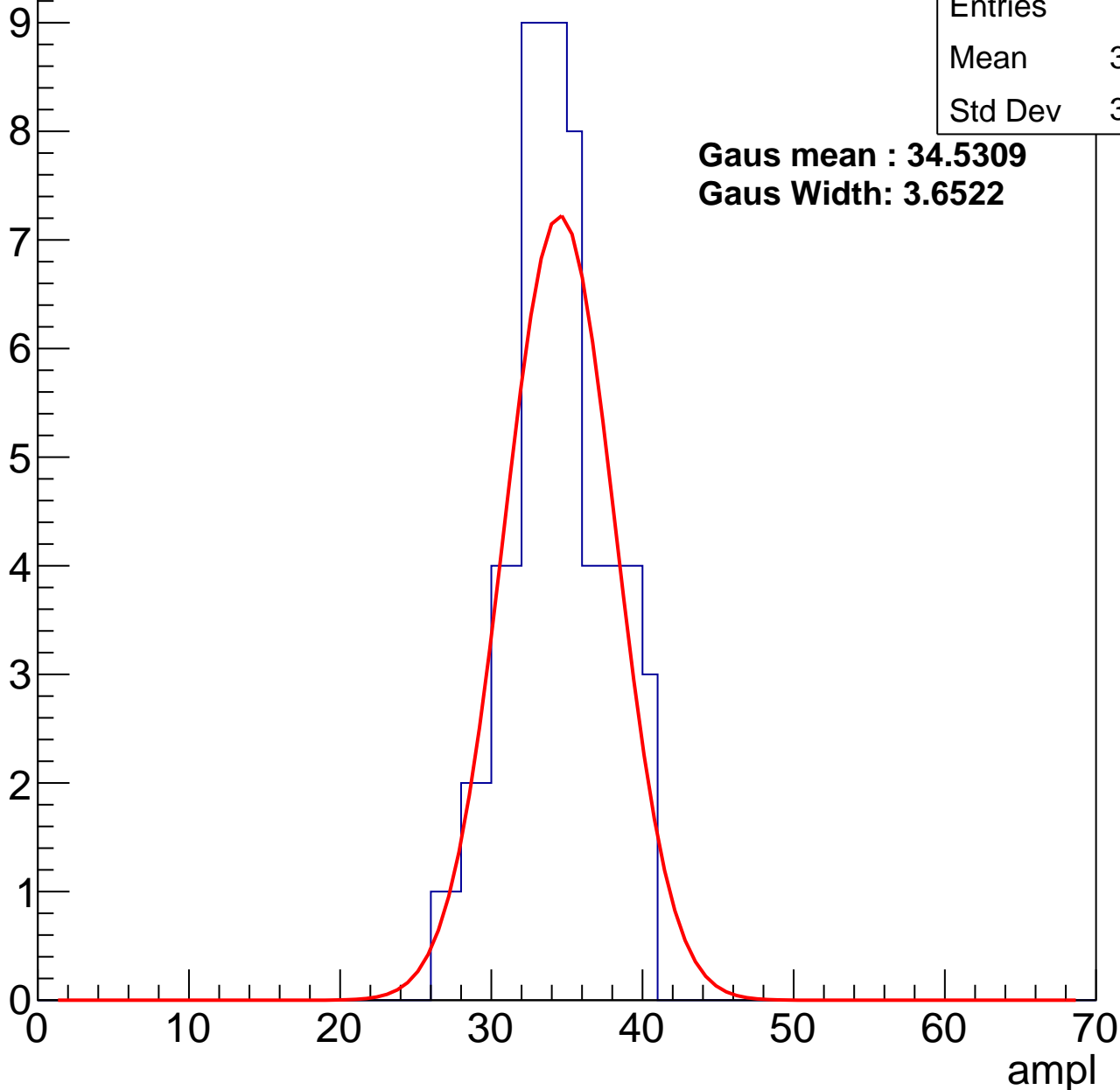
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	33.85
Std Dev	3.232

**Gaus mean : 34.5309**

**Gaus Width: 3.6522**



# B1L103S, U16-ch64, adc2

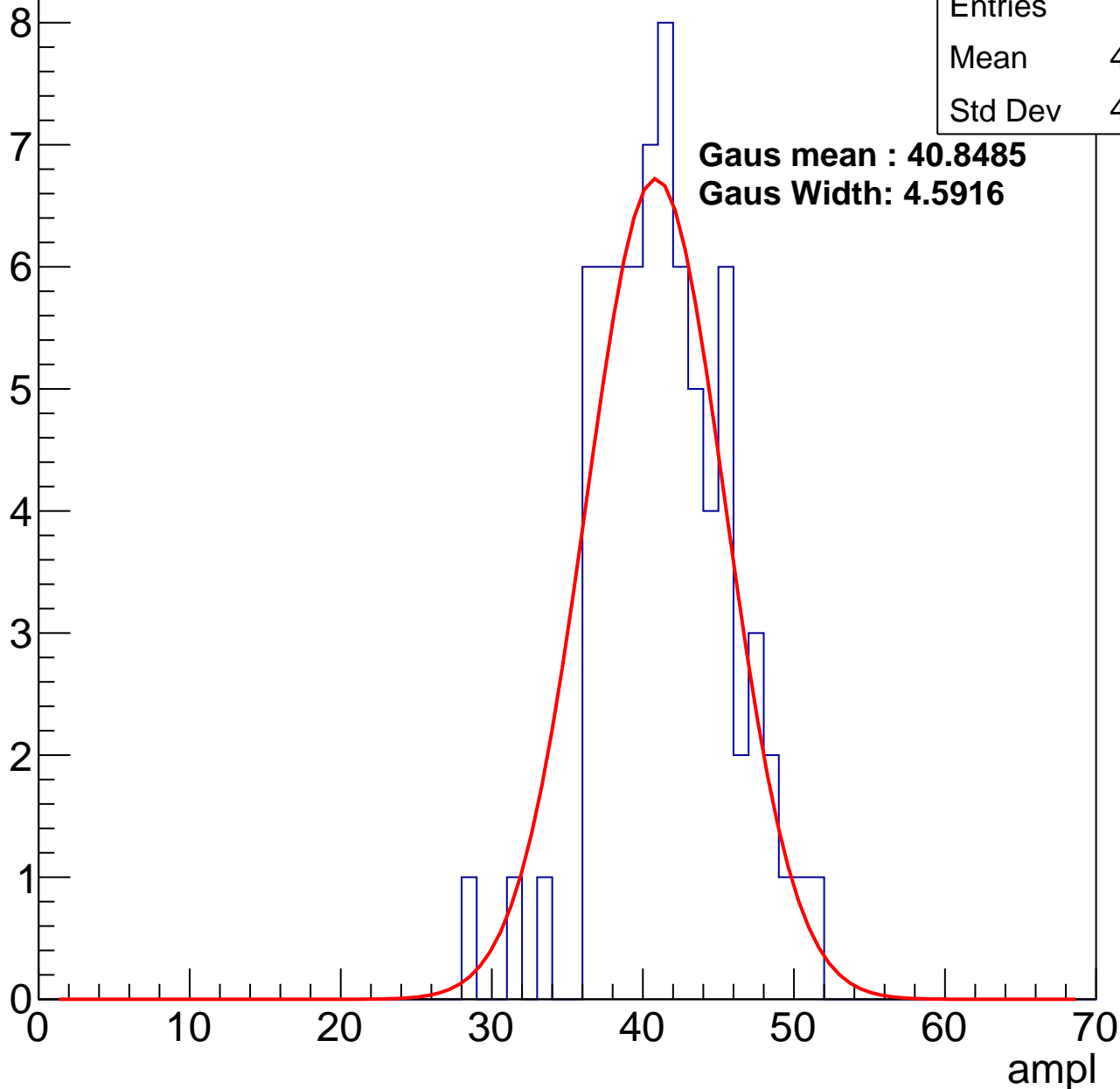
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	40.99
Std Dev	4.257

**Gaus mean : 40.8485**

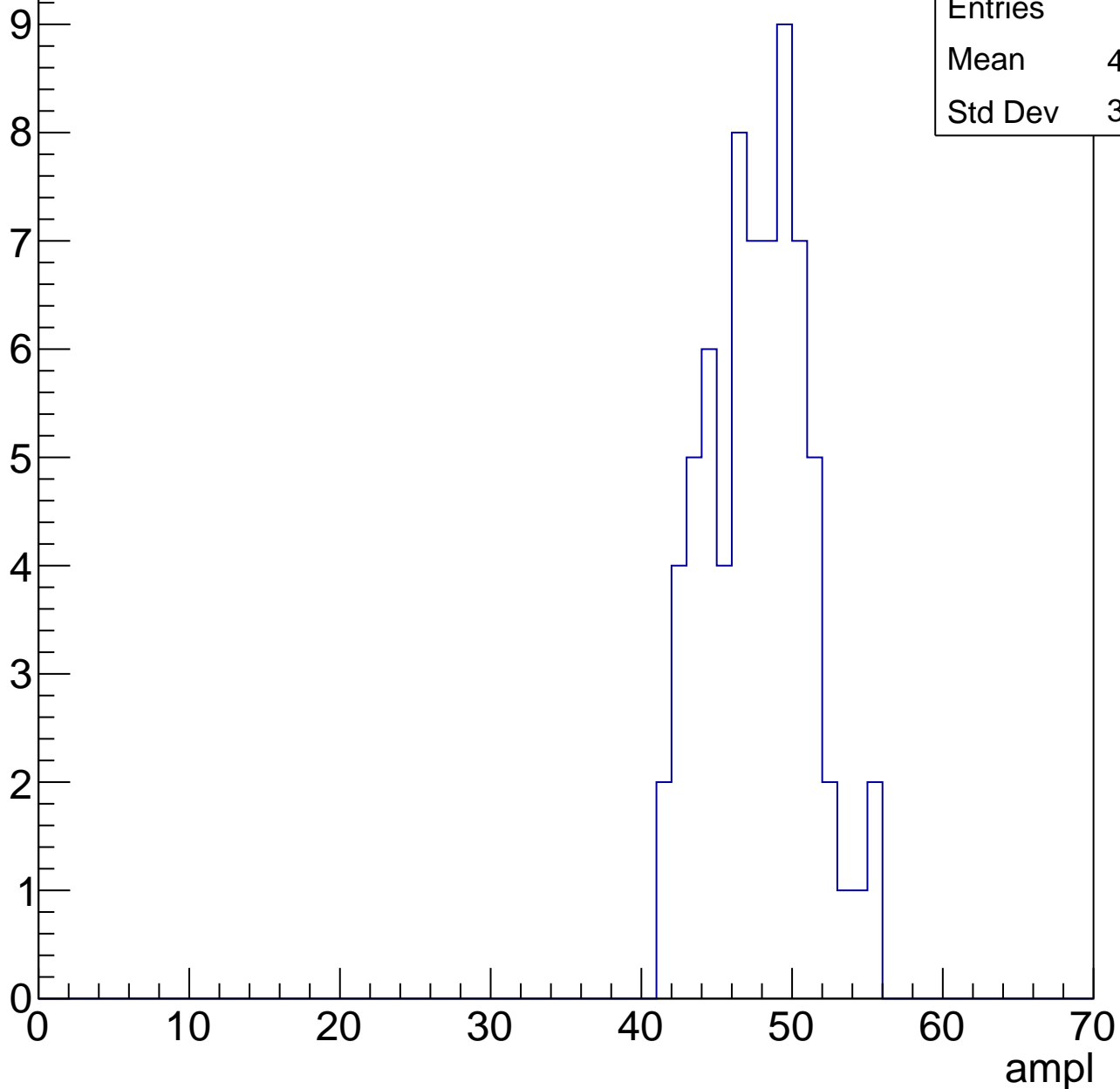
**Gaus Width: 4.5916**



# B1L103S, U16-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



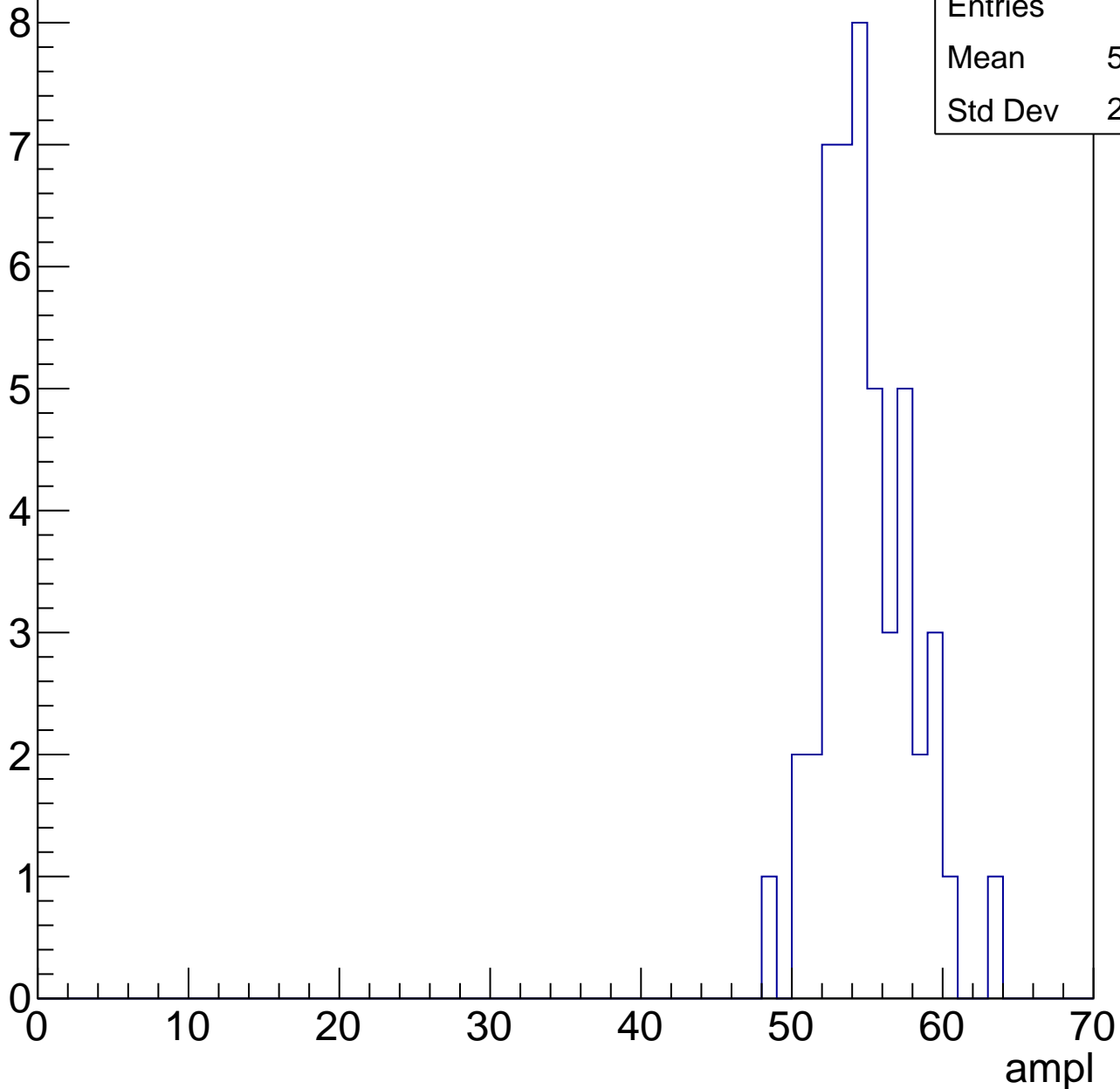
Entries	70
Mean	47.27
Std Dev	3.325

# B1L103S, U16-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	54.49
Std Dev	2.902

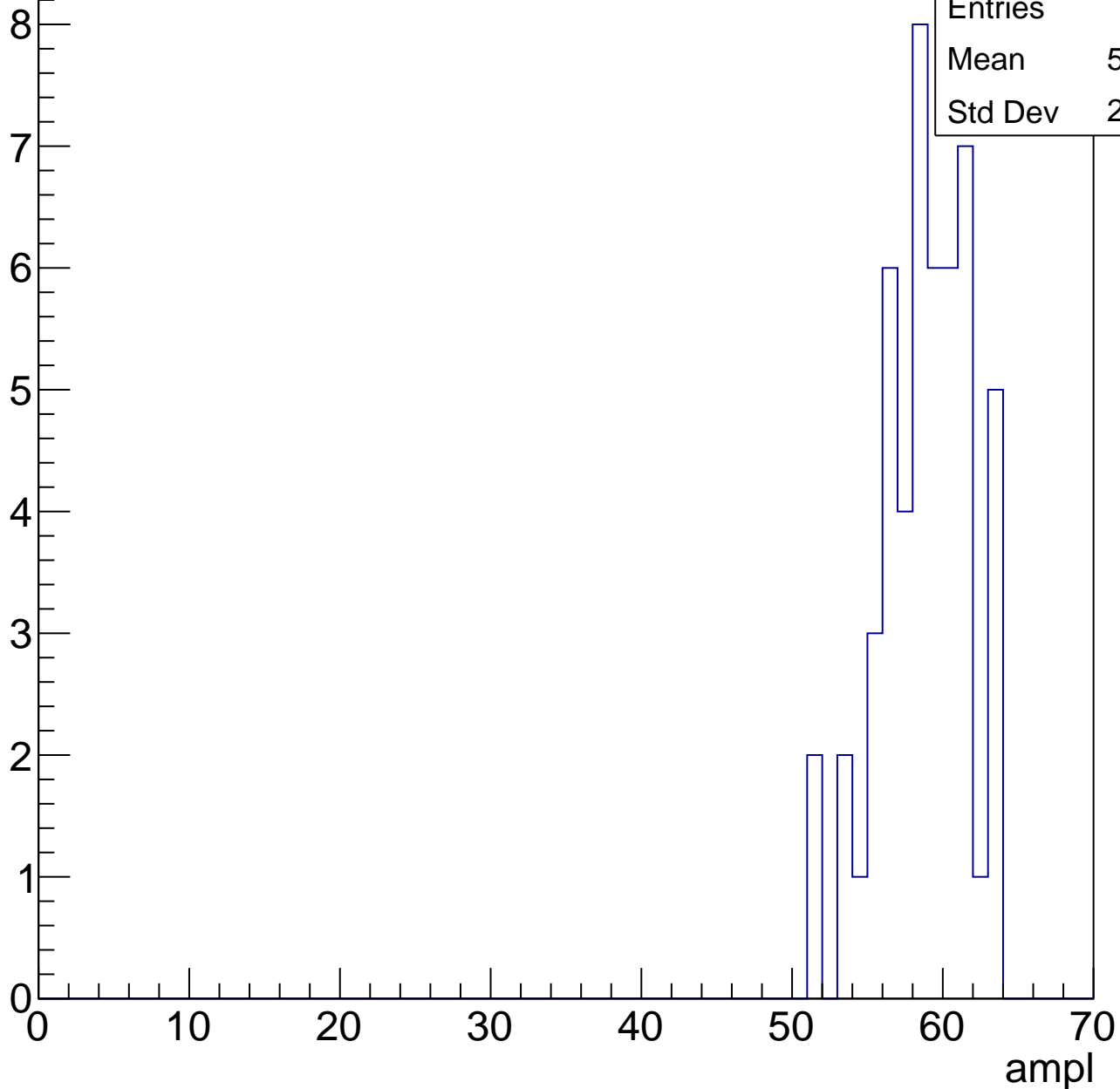


# B1L103S, U16-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	58.29
Std Dev	2.966

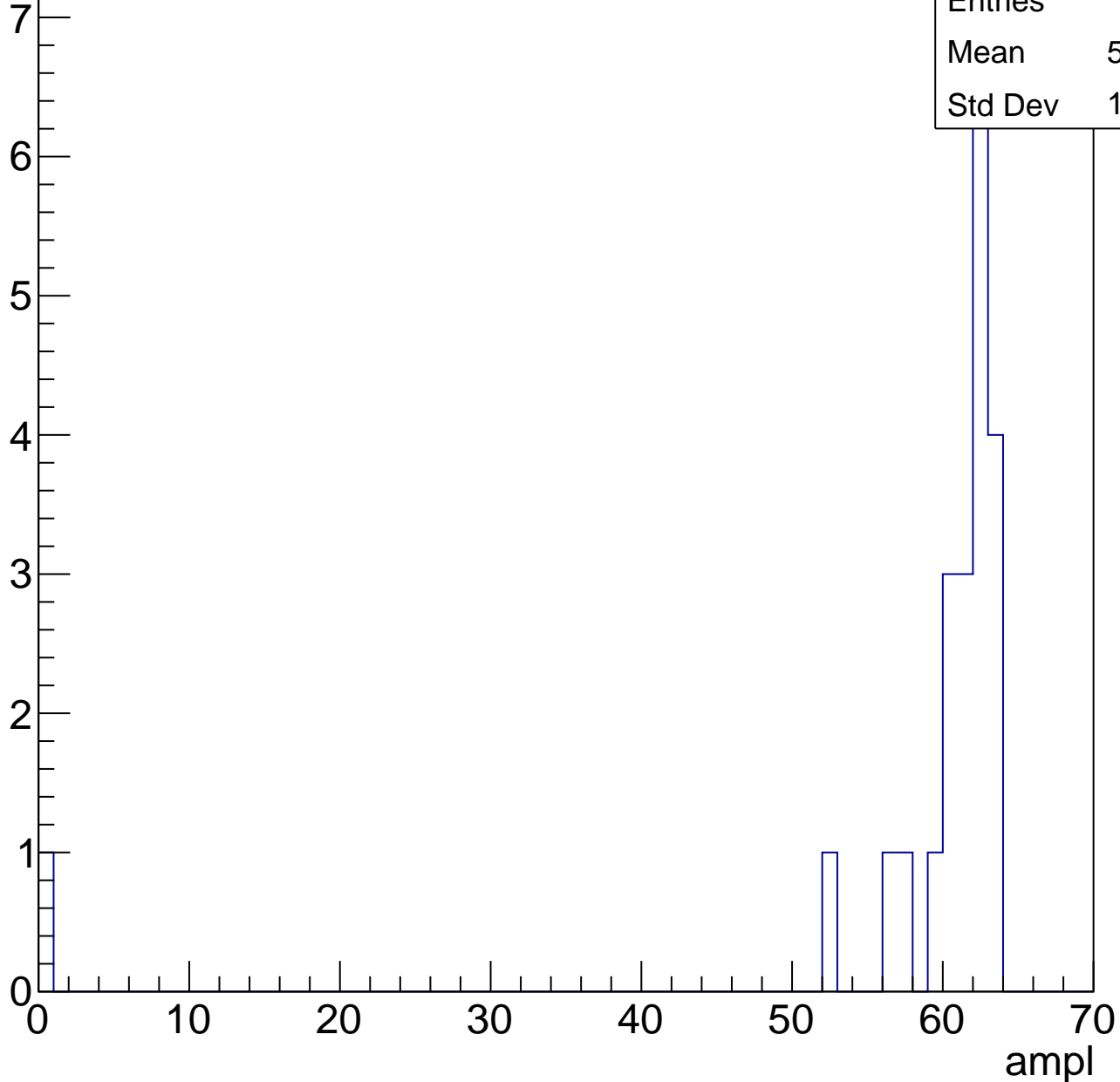


# B1L103S, U16-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	22
Mean	57.86
Std Dev	12.89

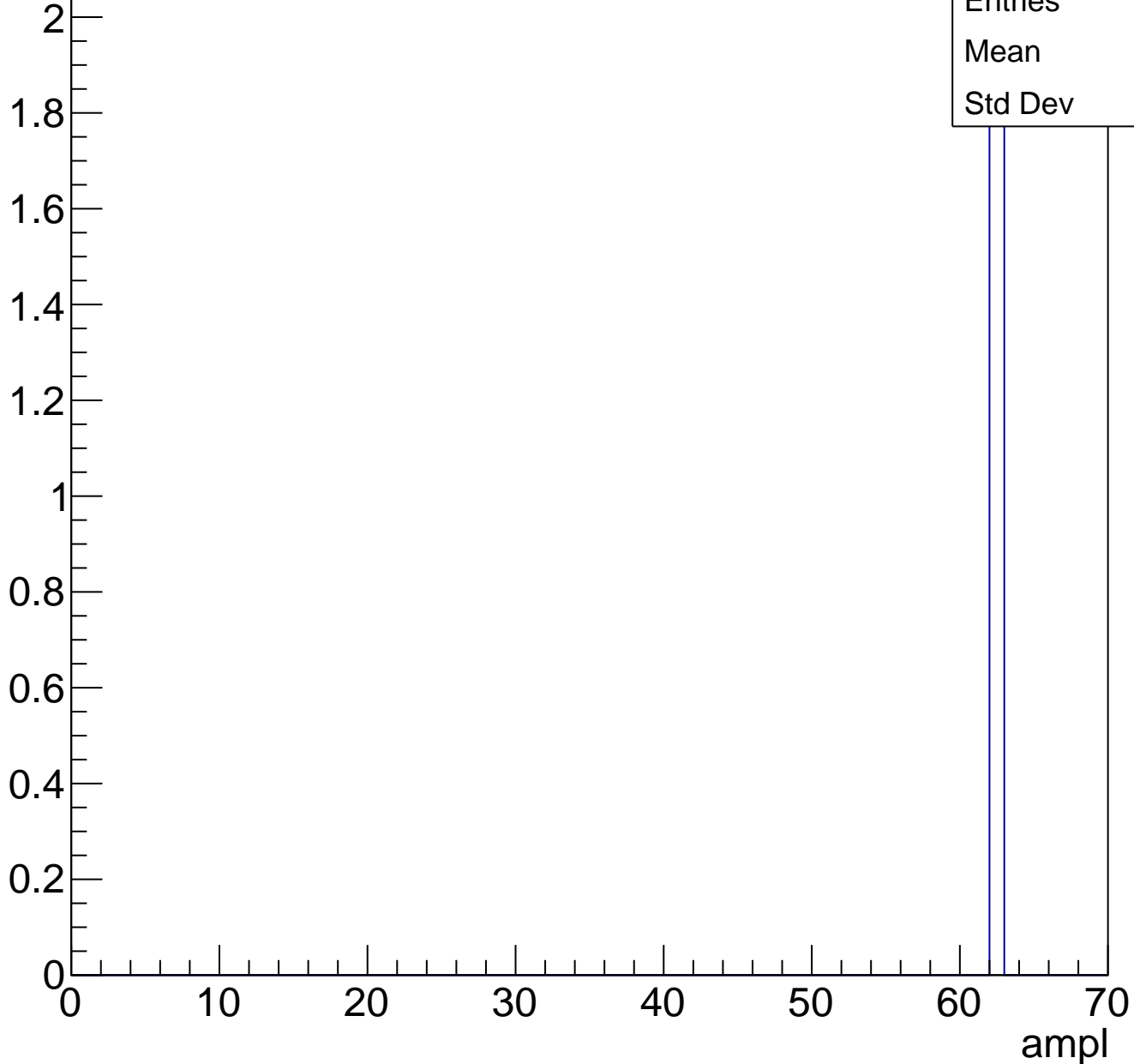




# B1L103S, U16-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch65, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	70
Mean	28.17
Std Dev	3.676

**Gaus mean : 28.8235**

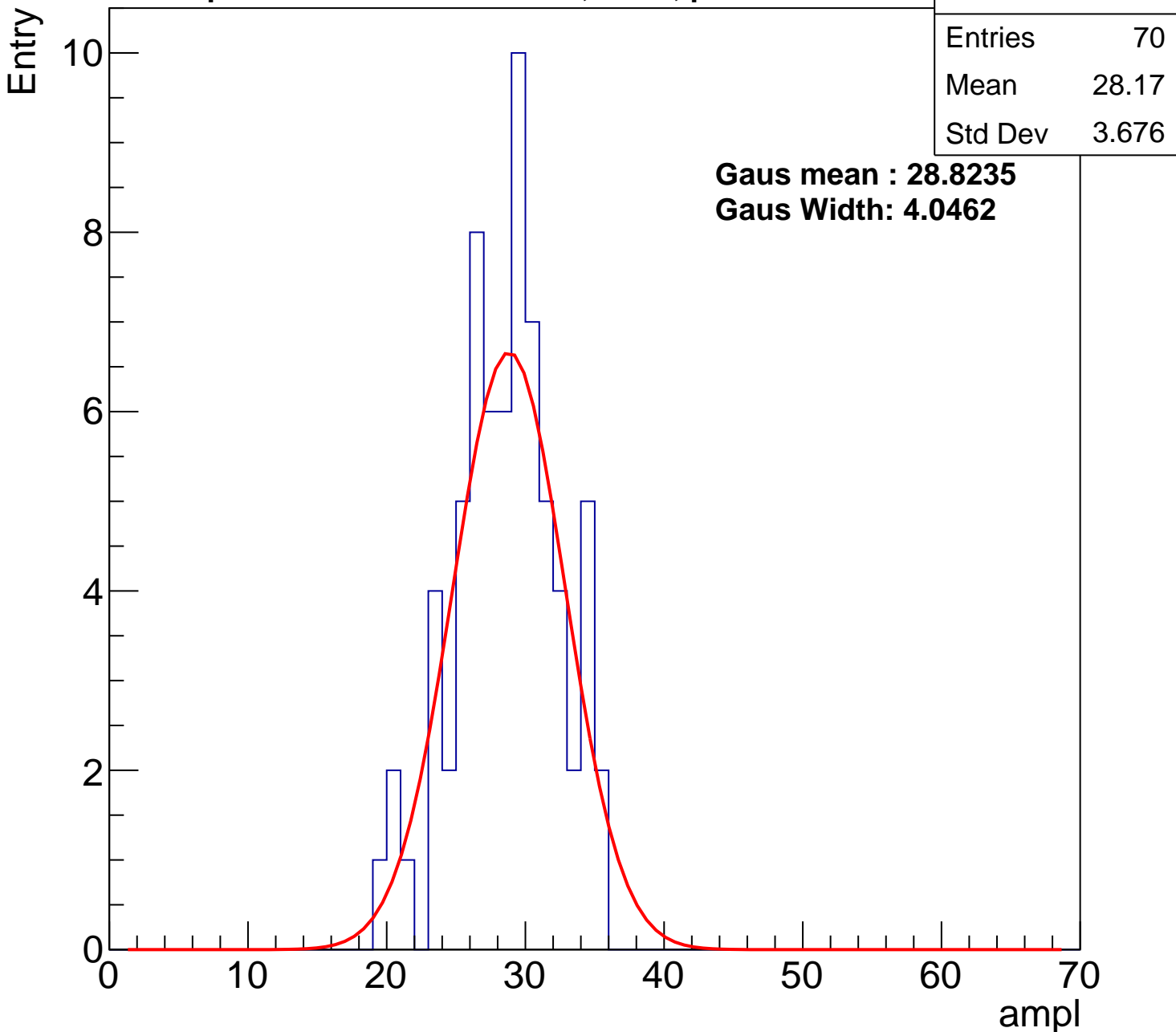
**Gaus Width: 4.0462**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U16-ch65, adc1

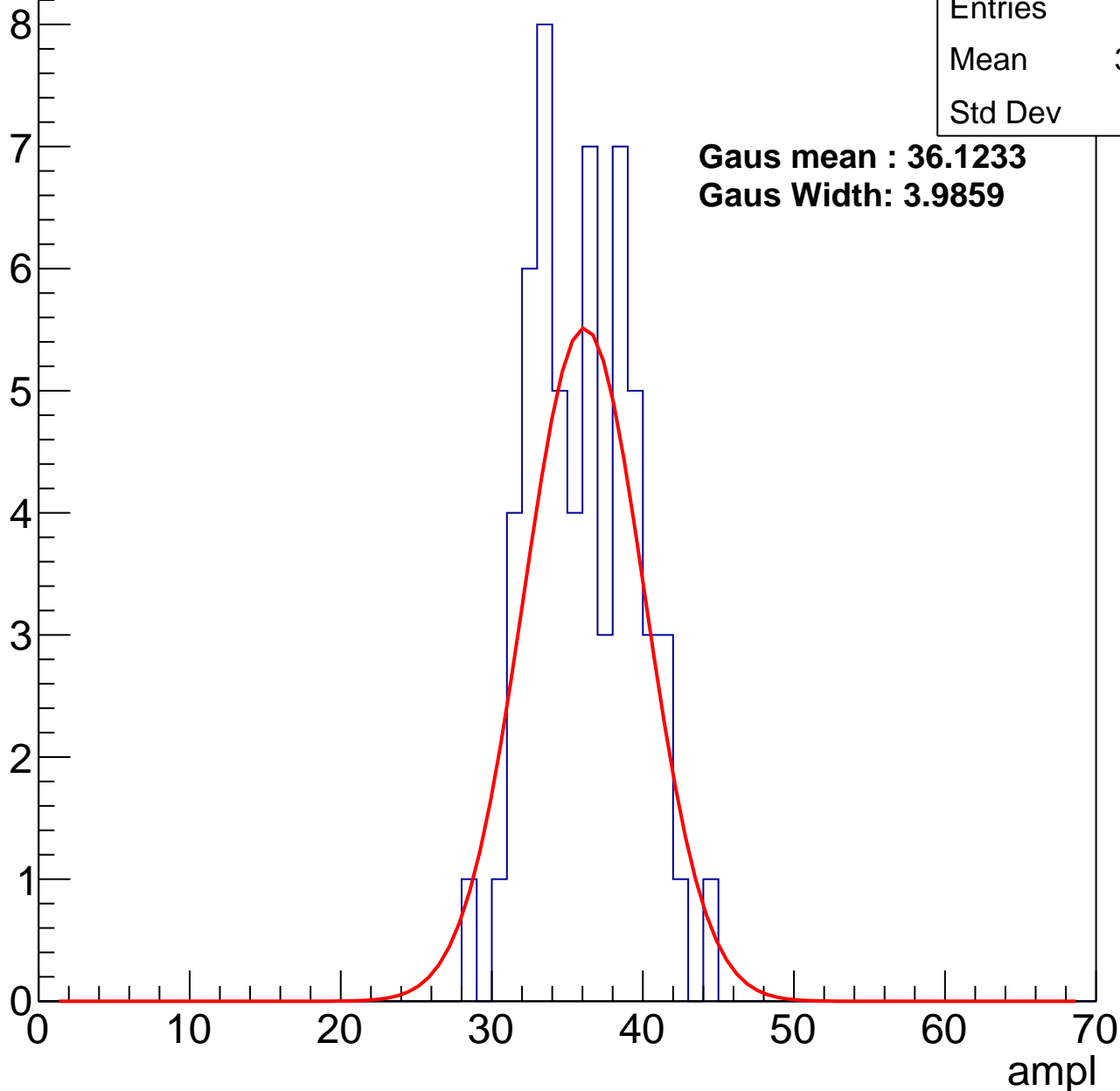
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	35.61
Std Dev	3.4

**Gaus mean : 36.1233**

**Gaus Width: 3.9859**

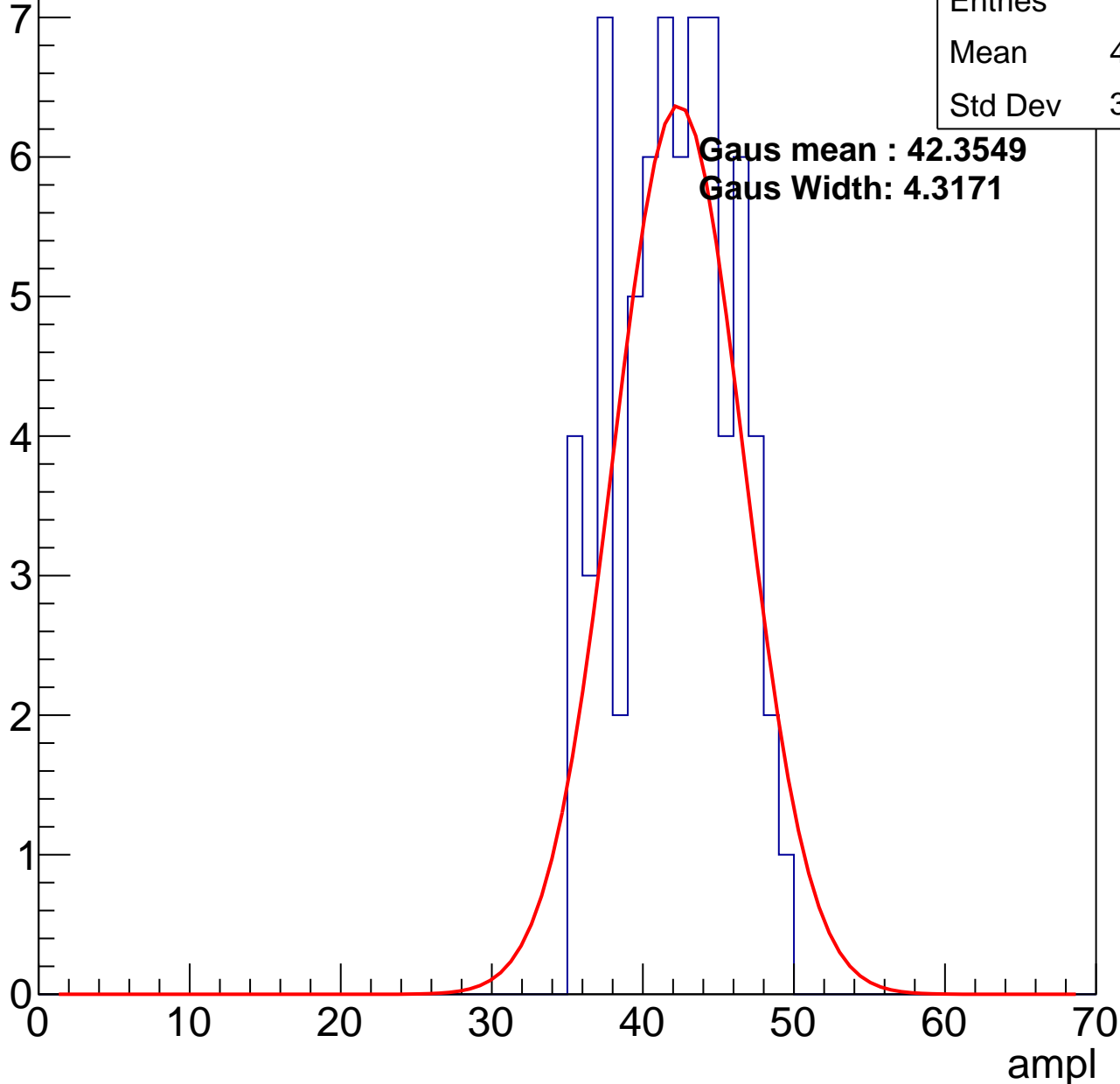


# B1L103S, U16-ch65, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	41.62
Std Dev	3.686

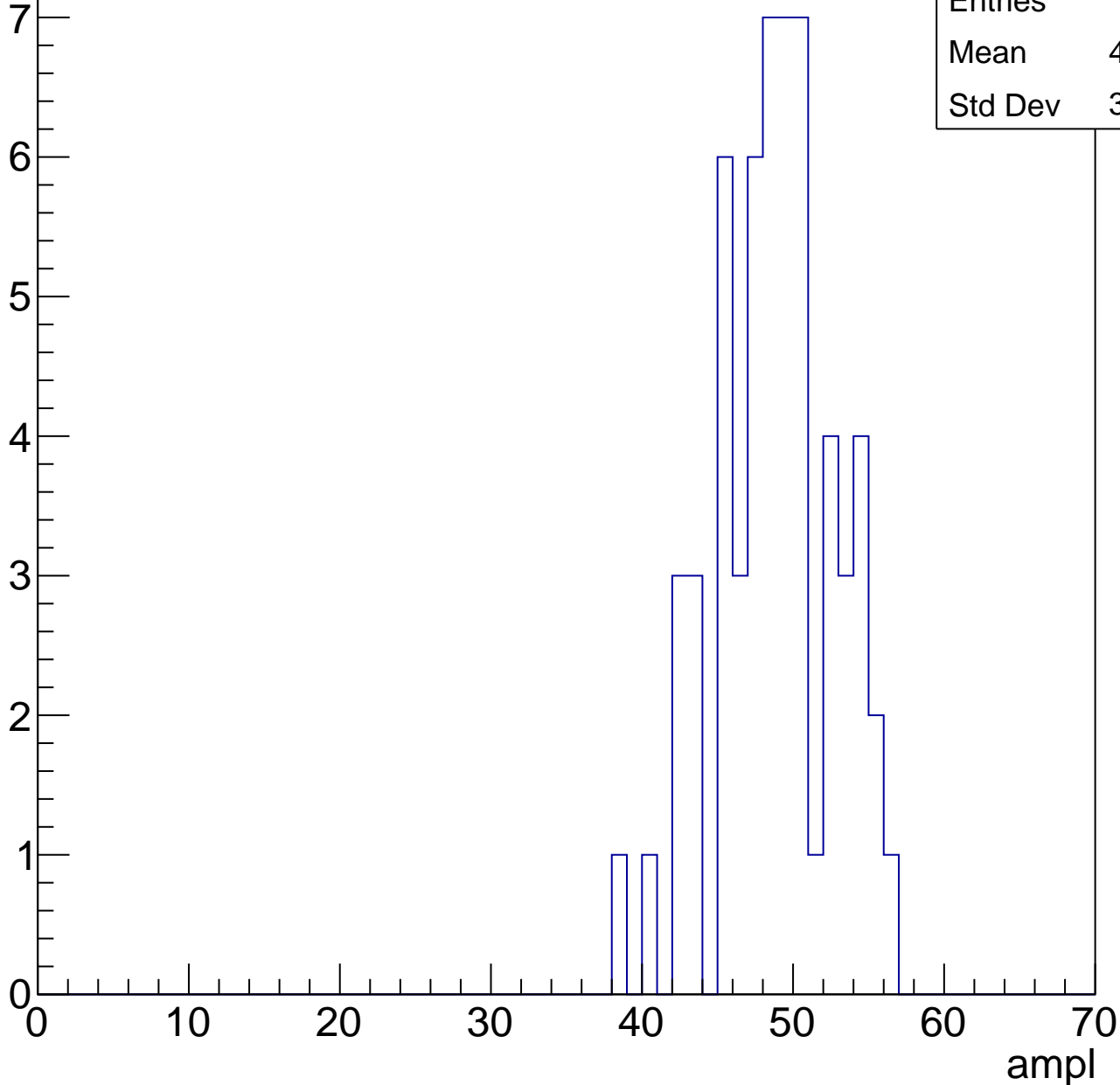


# B1L103S, U16-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	48.34
Std Dev	3.908

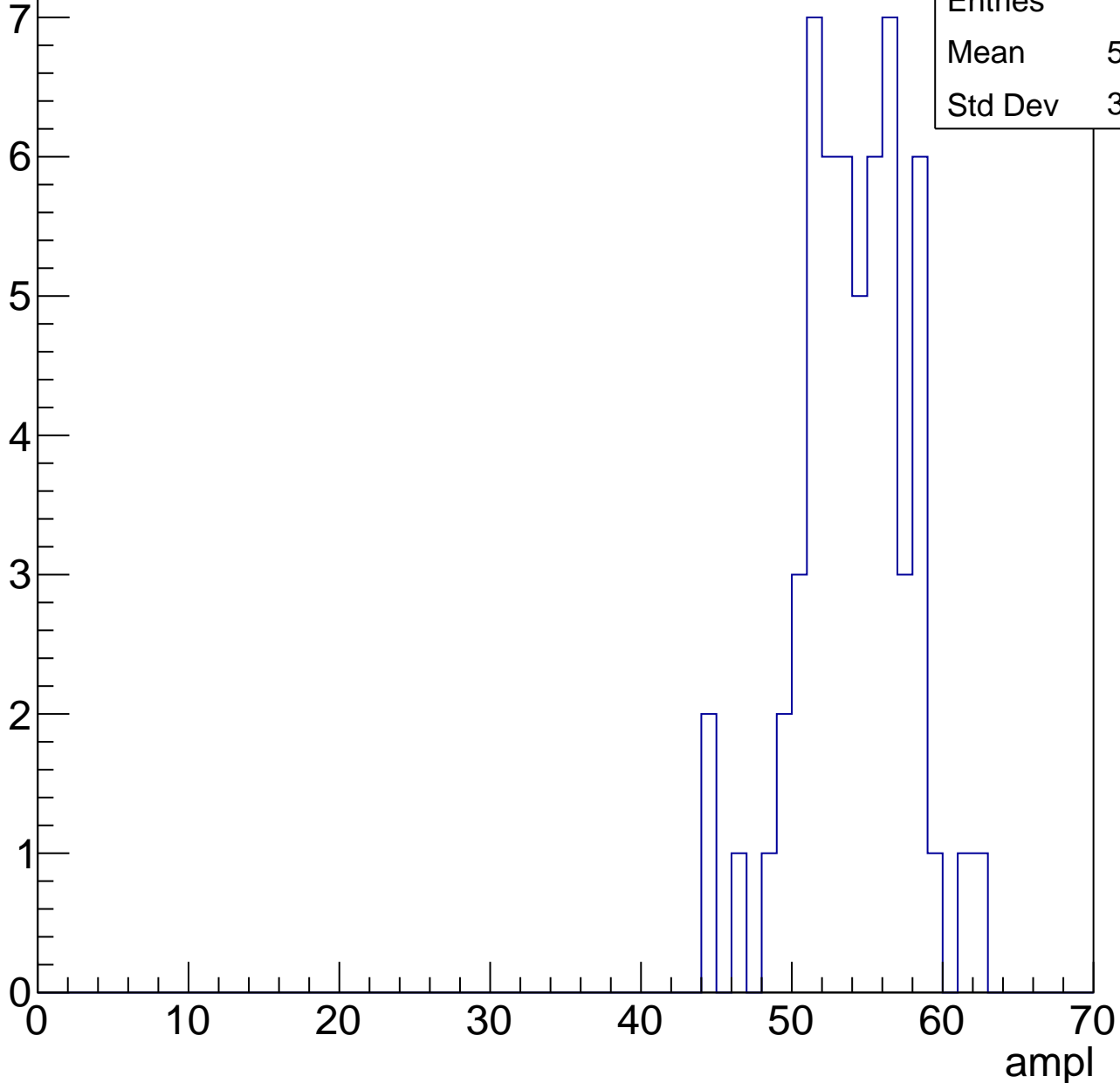


# B1L103S, U16-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	53.62
Std Dev	3.662

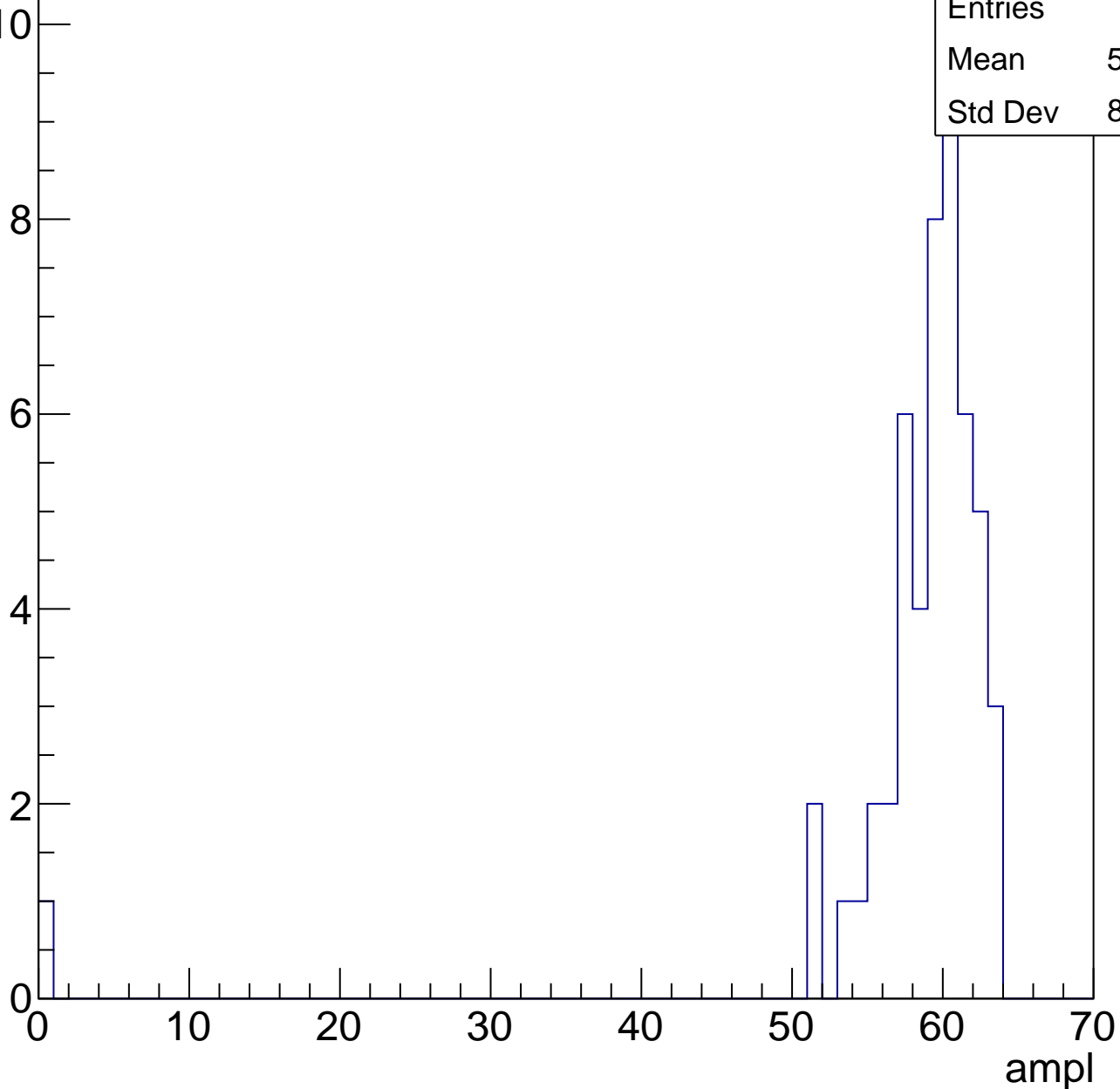


# B1L103S, U16-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	57.69
Std Dev	8.617

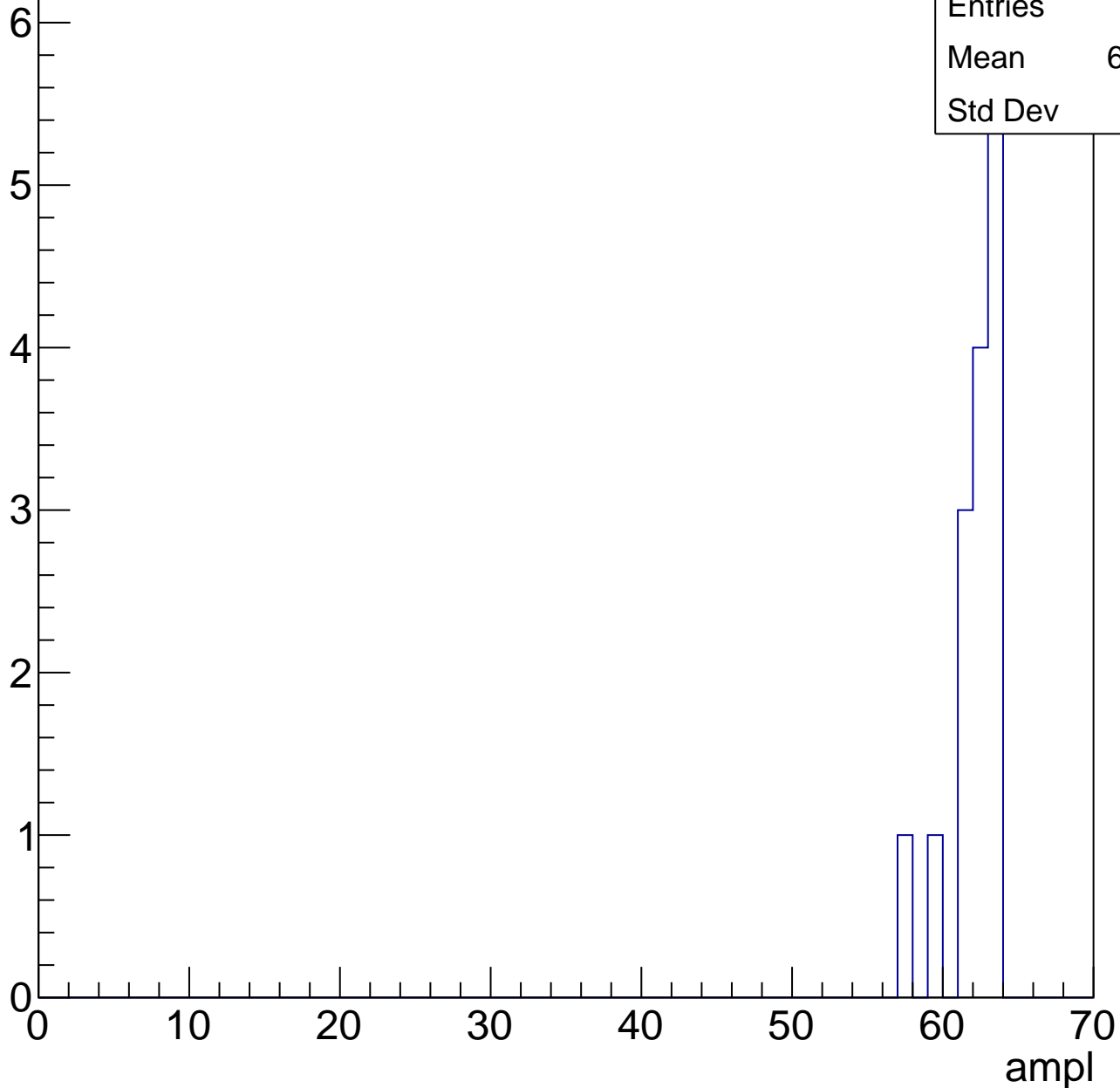


# B1L103S, U16-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	15
Mean	61.67
Std Dev	1.66





# B1L103S, U16-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch66, adc0

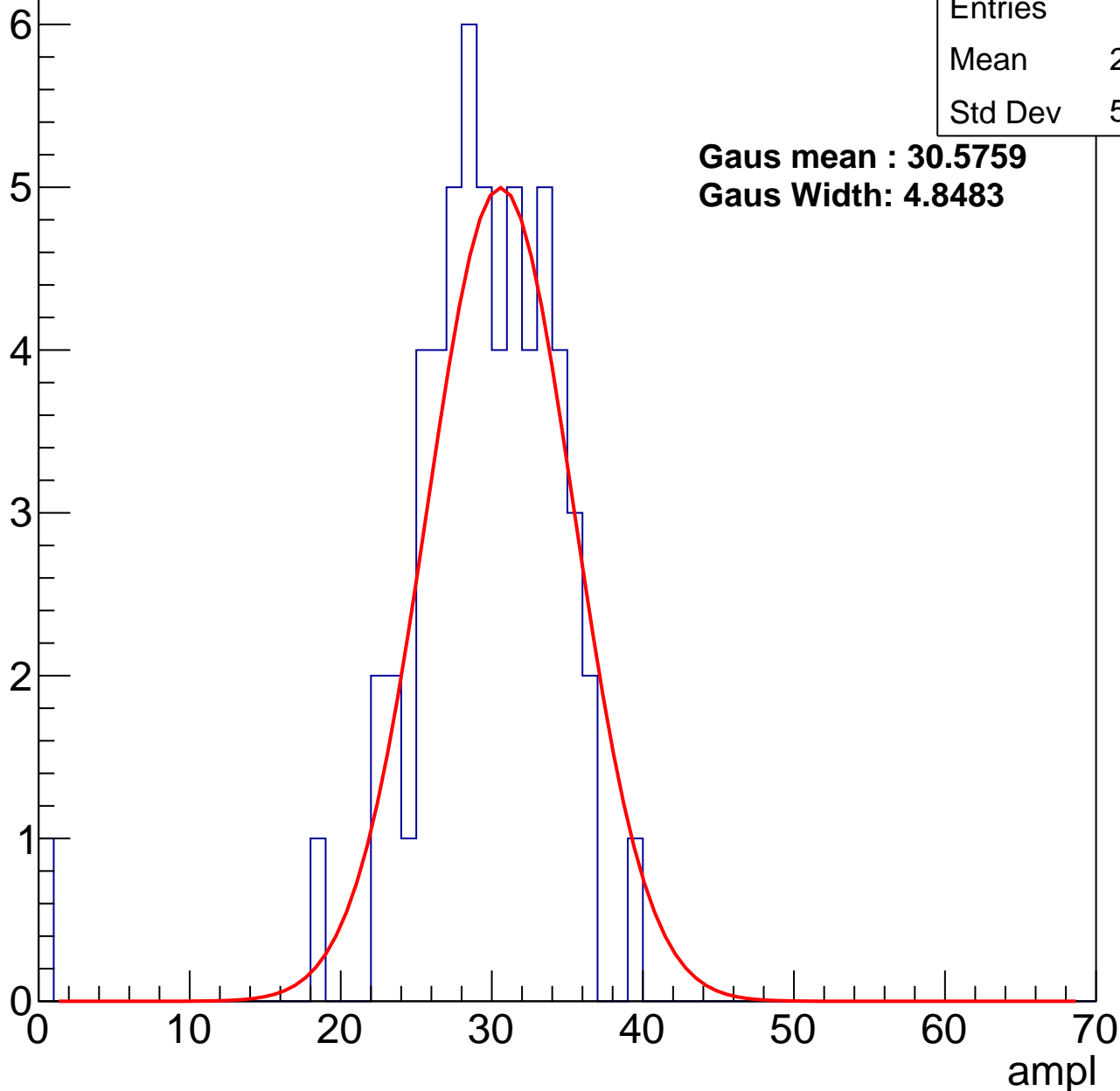
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	28.88
Std Dev	5.567

**Gaus mean : 30.5759**

**Gaus Width: 4.8483**



# B1L103S, U16-ch66, adc1

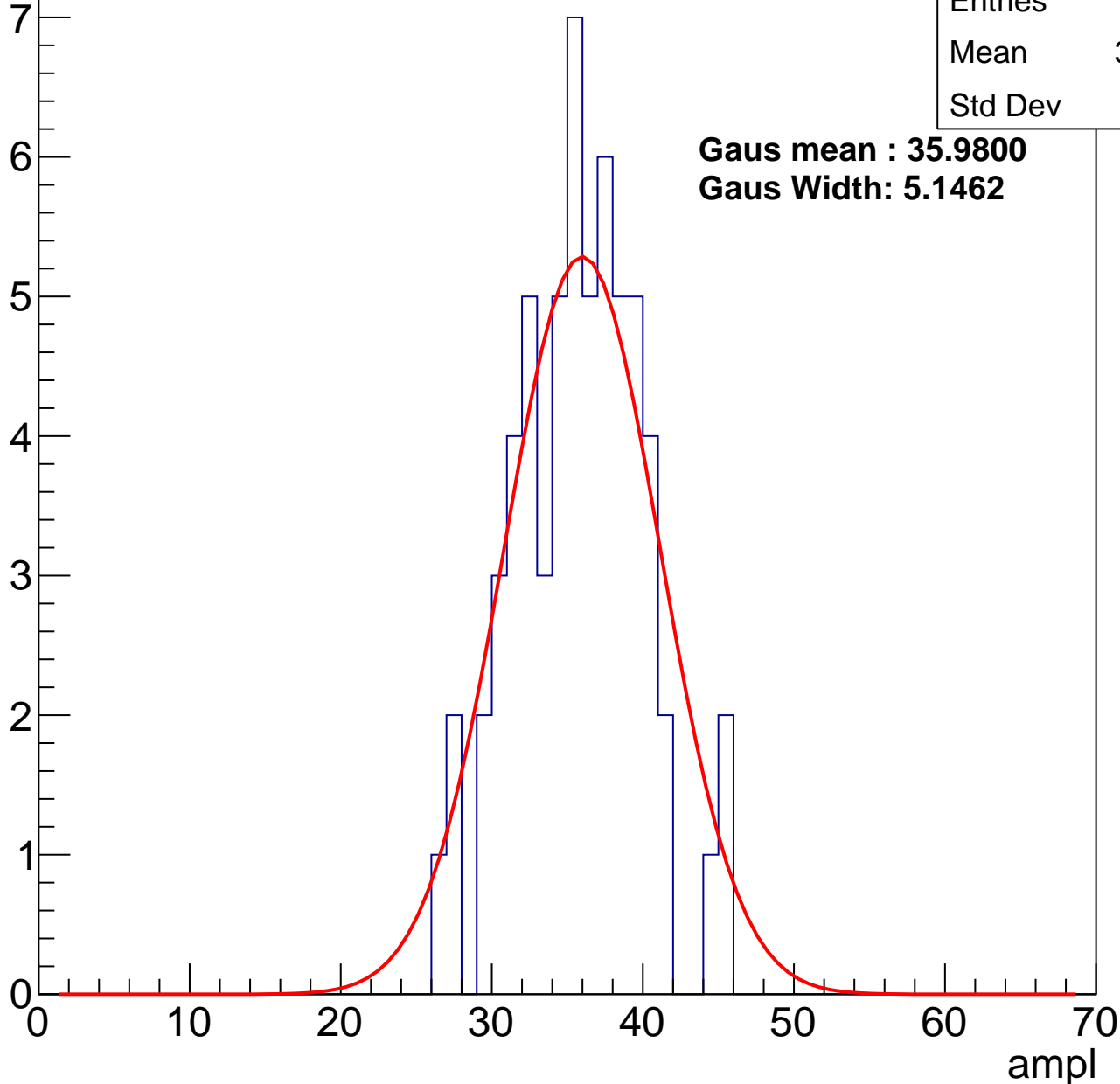
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	35.31
Std Dev	4.18

**Gaus mean : 35.9800**

**Gaus Width: 5.1462**



# B1L103S, U16-ch66, adc2

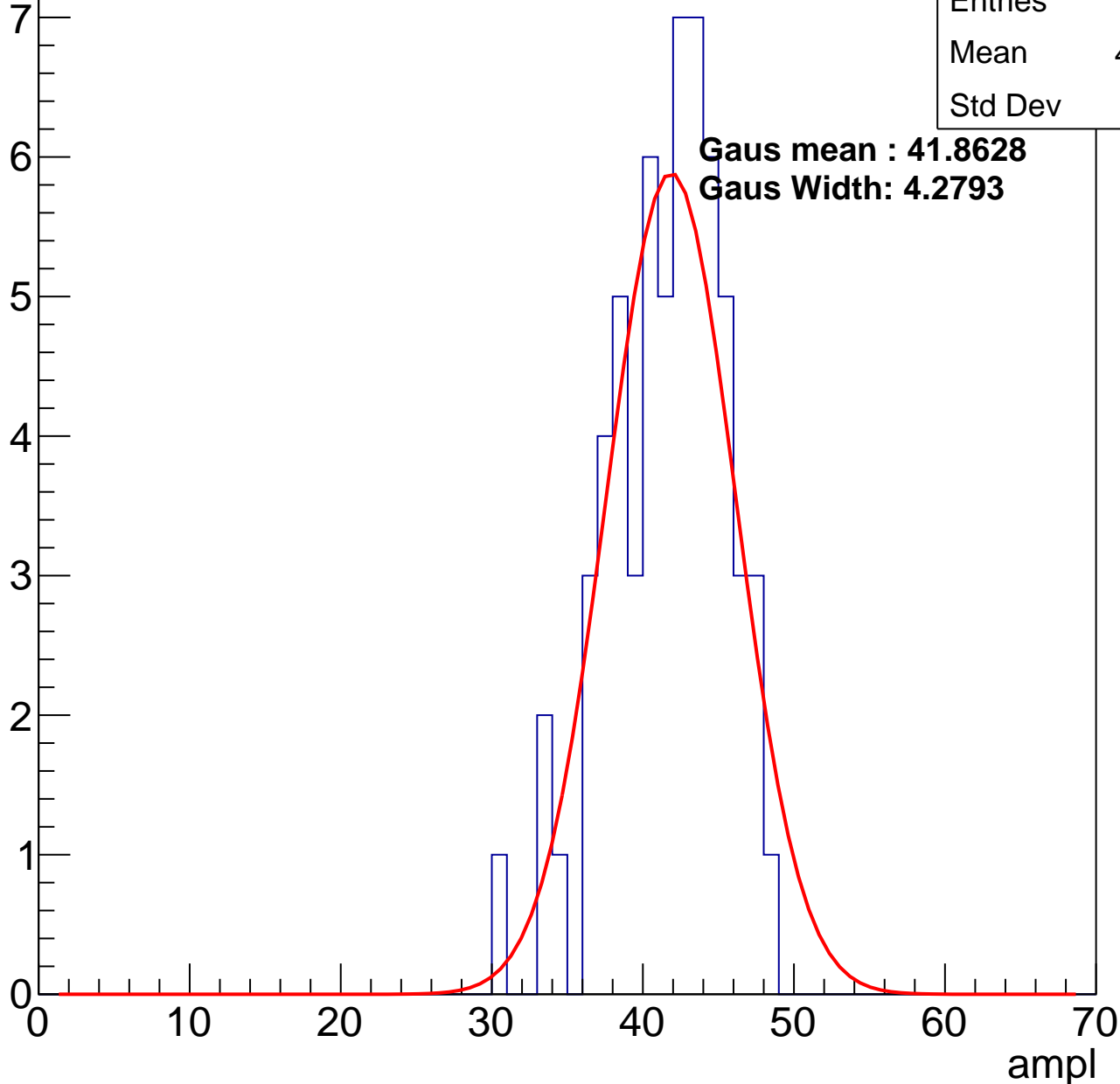
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	41.11
Std Dev	3.81

**Gaus mean : 41.8628**

**Gaus Width: 4.2793**

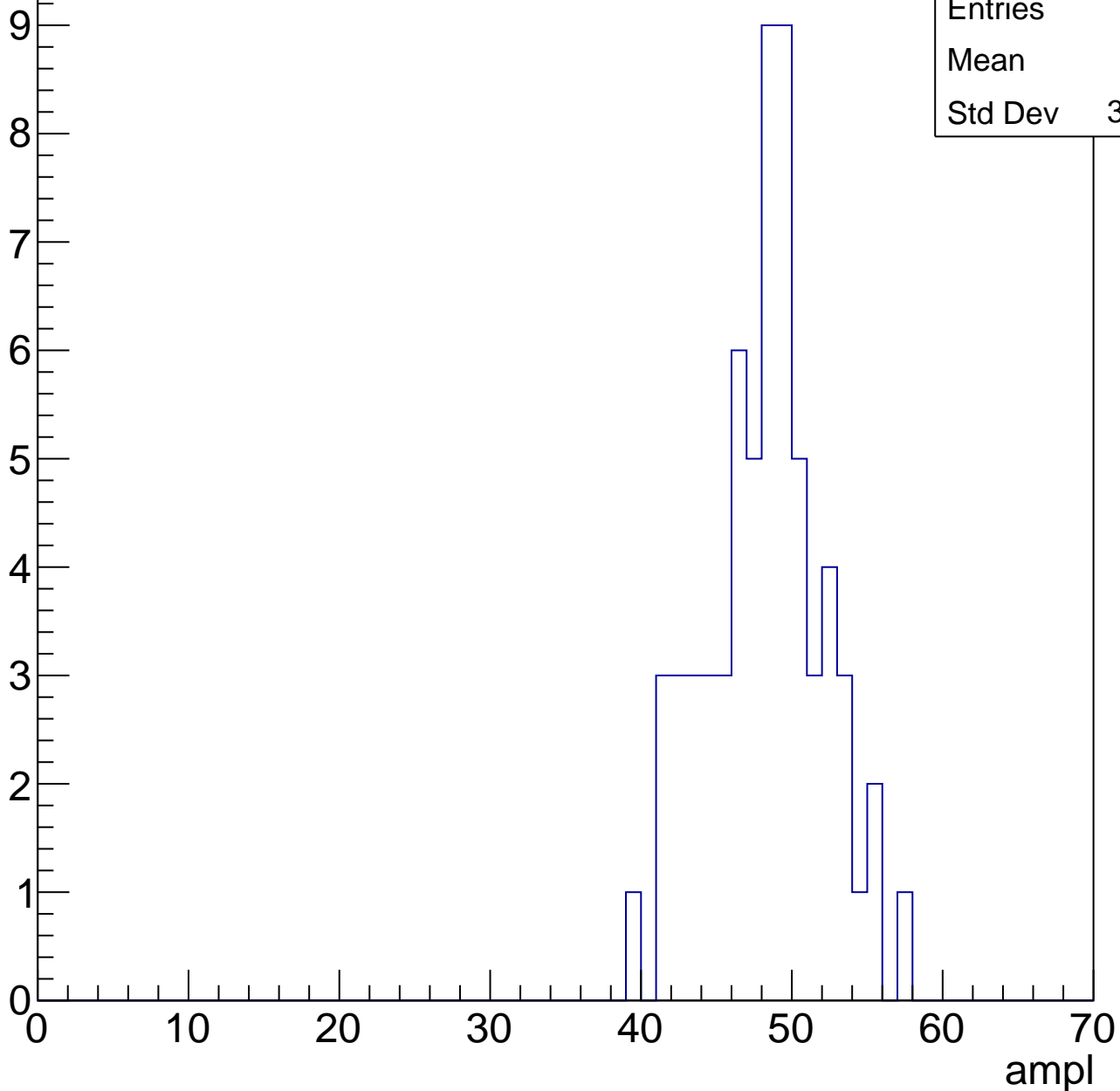


# B1L103S, U16-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

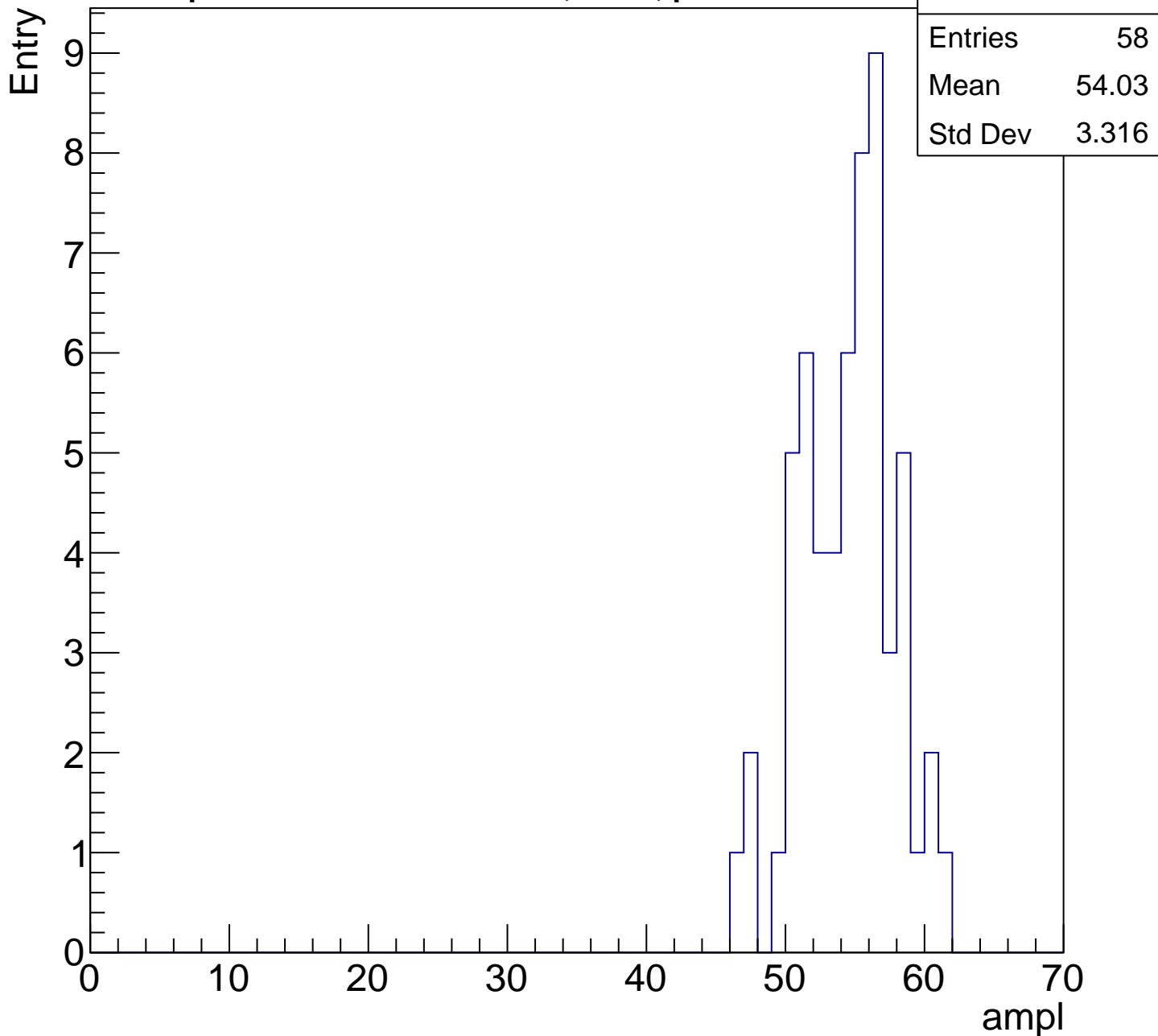
Entry

Entries	64
Mean	47.8
Std Dev	3.796



# B1L103S, U16-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

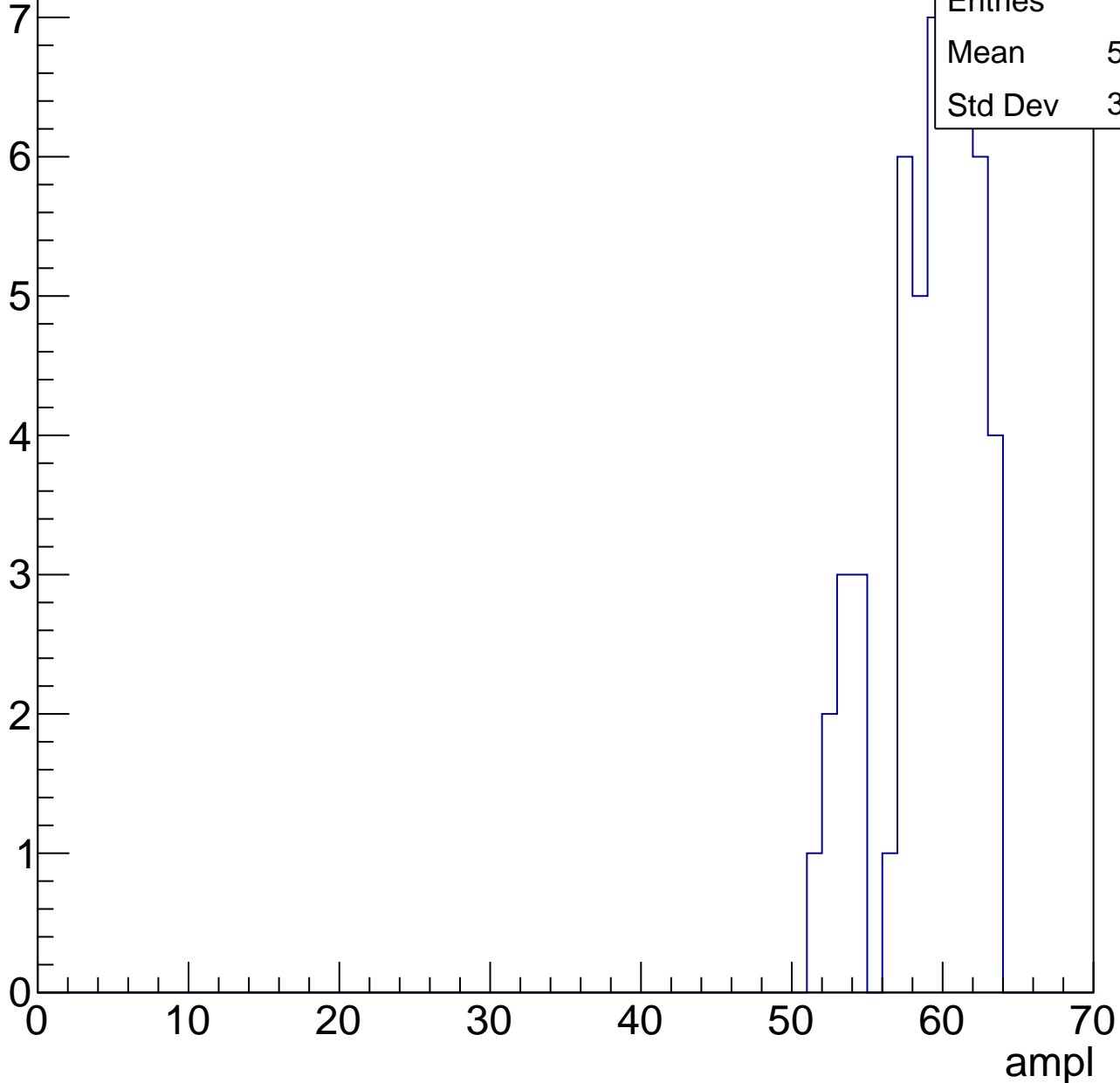


# B1L103S, U16-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	58.62
Std Dev	3.187

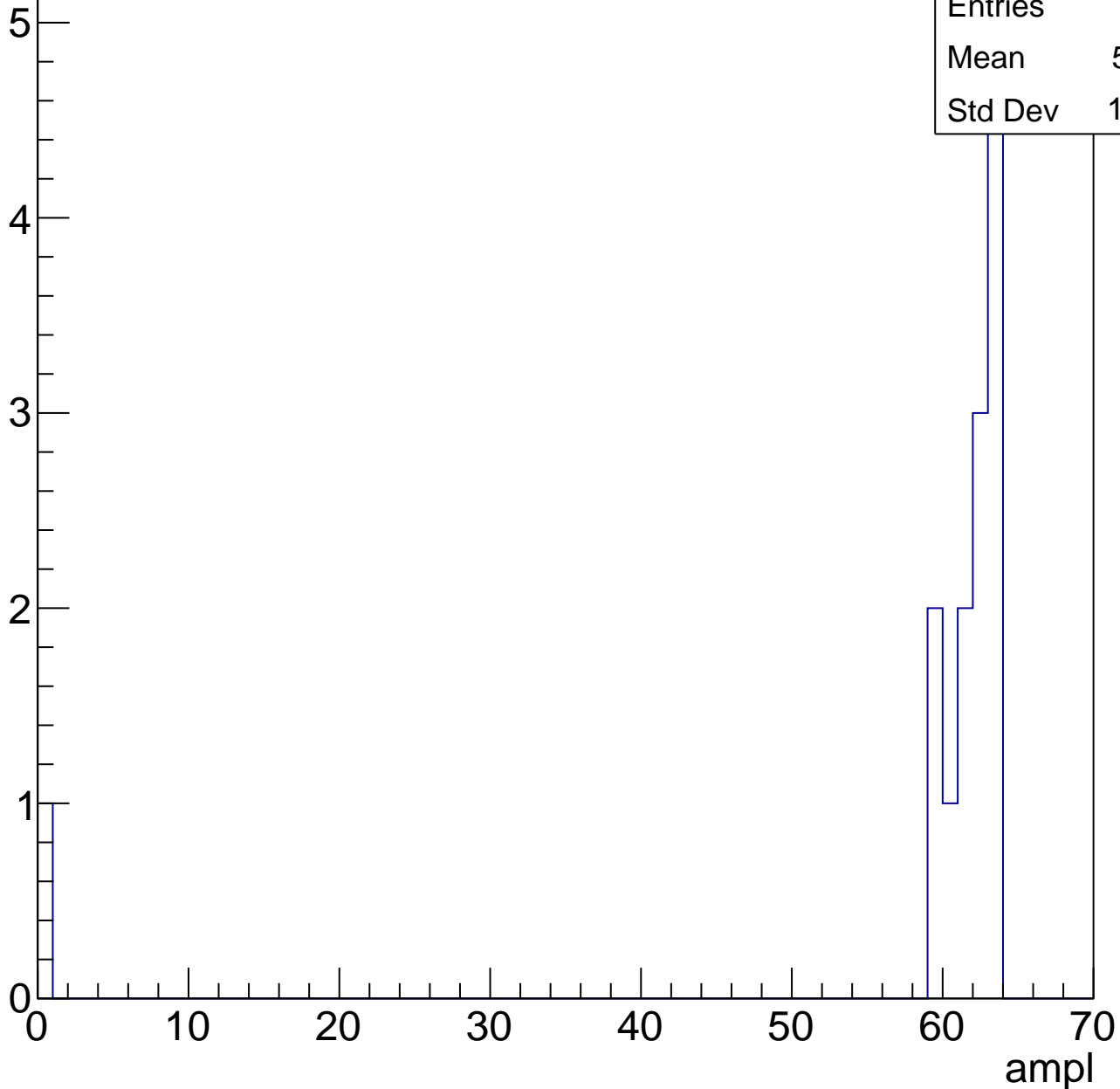


# B1L103S, U16-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	14
Mean	57.21
Std Dev	15.93

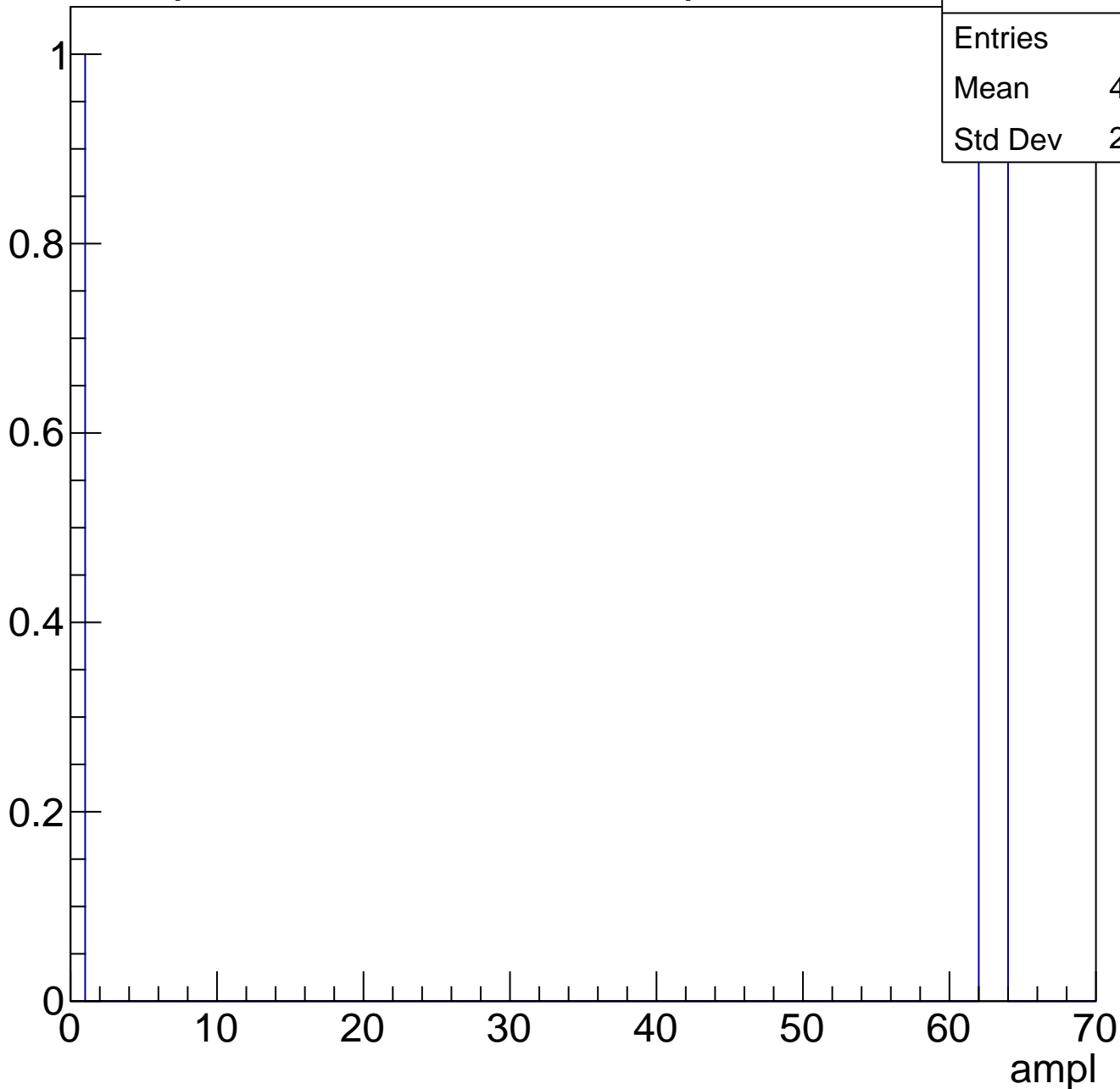




# B1L103S, U16-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch67, adc0

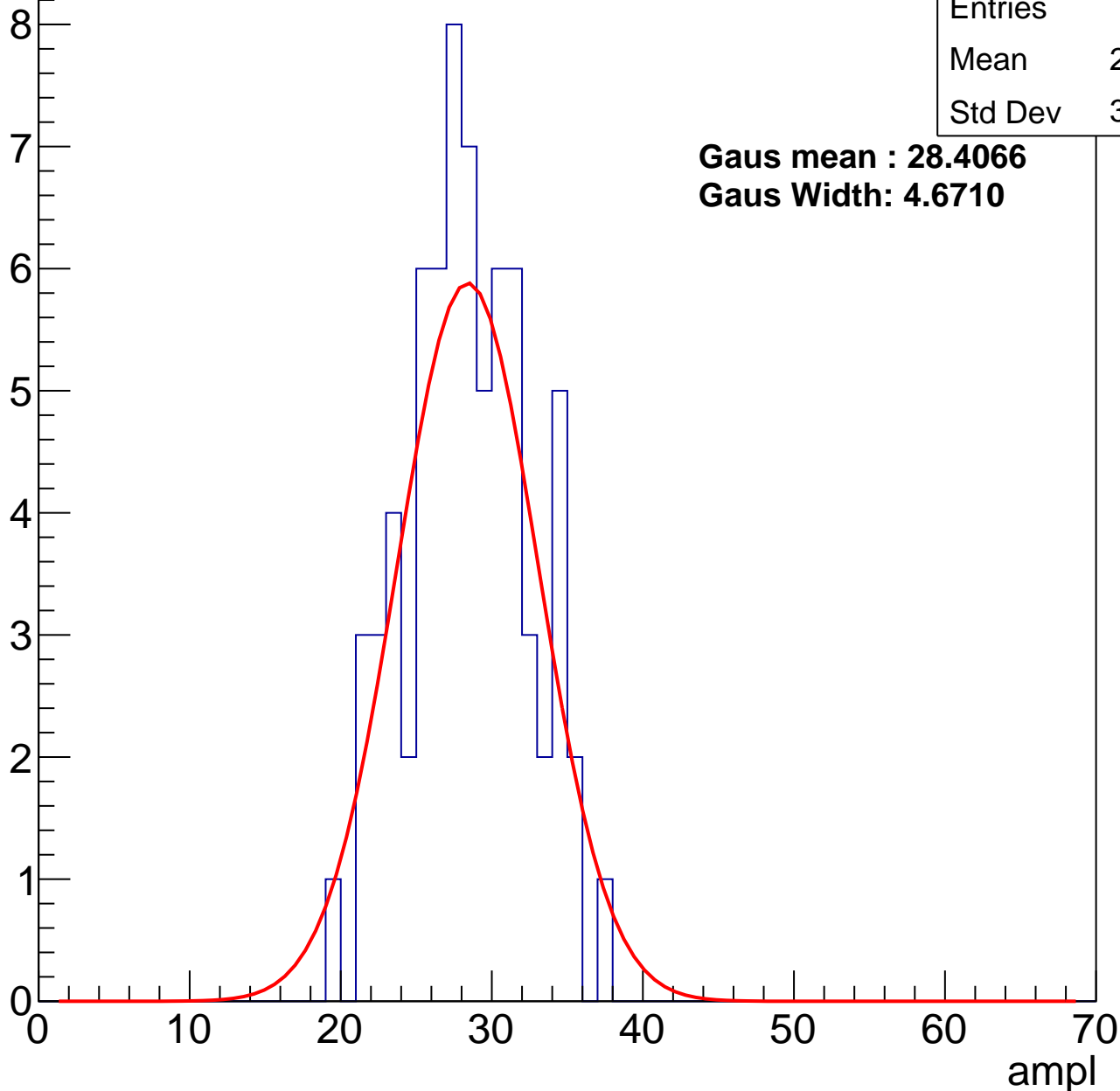
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	27.94
Std Dev	3.953

**Gaus mean : 28.4066**

**Gaus Width: 4.6710**



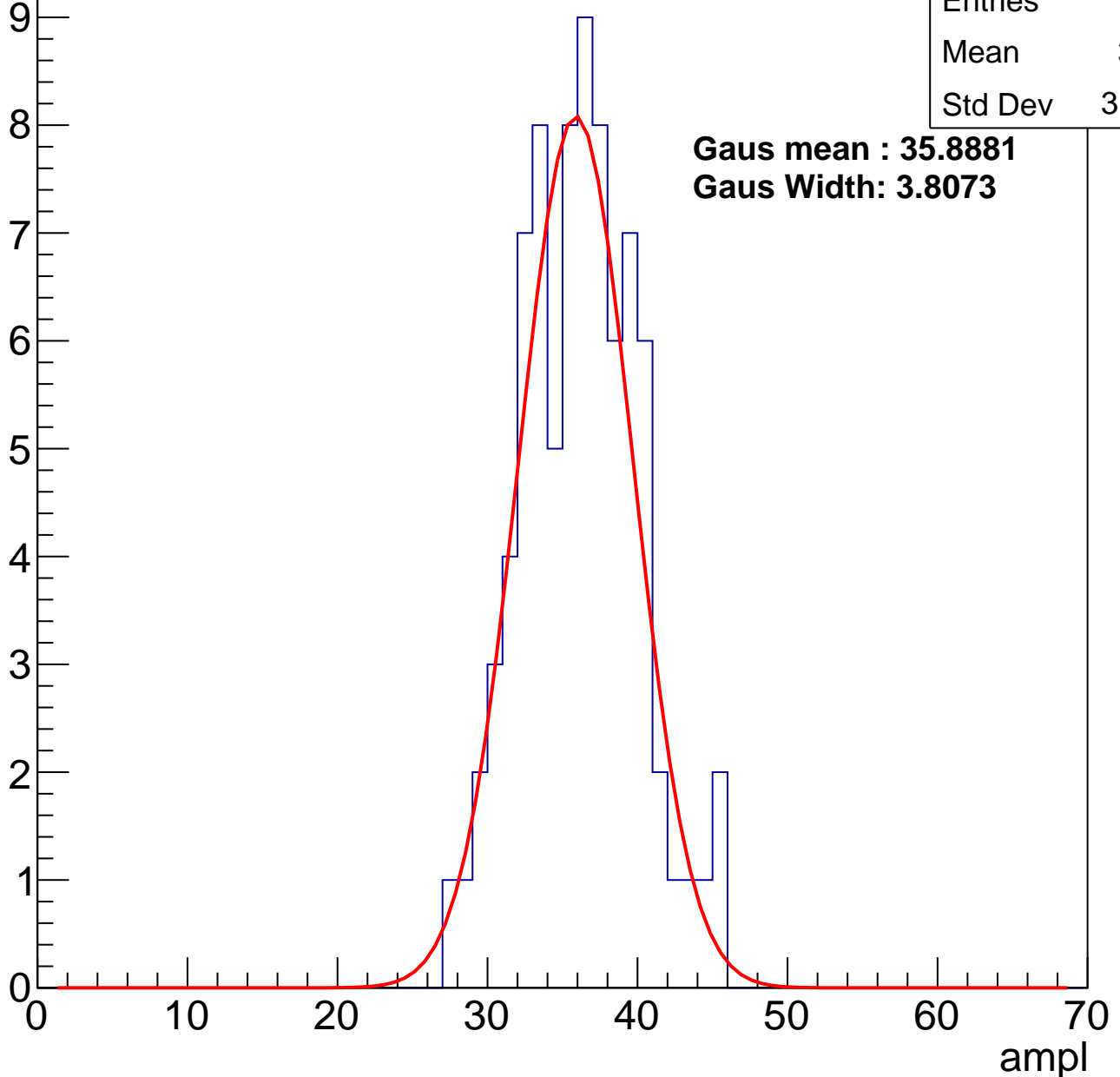
# B1L103S, U16-ch67, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	82
Mean	35.7
Std Dev	3.837

**Gaus mean : 35.8881**  
**Gaus Width: 3.8073**



# B1L103S, U16-ch67, adc2

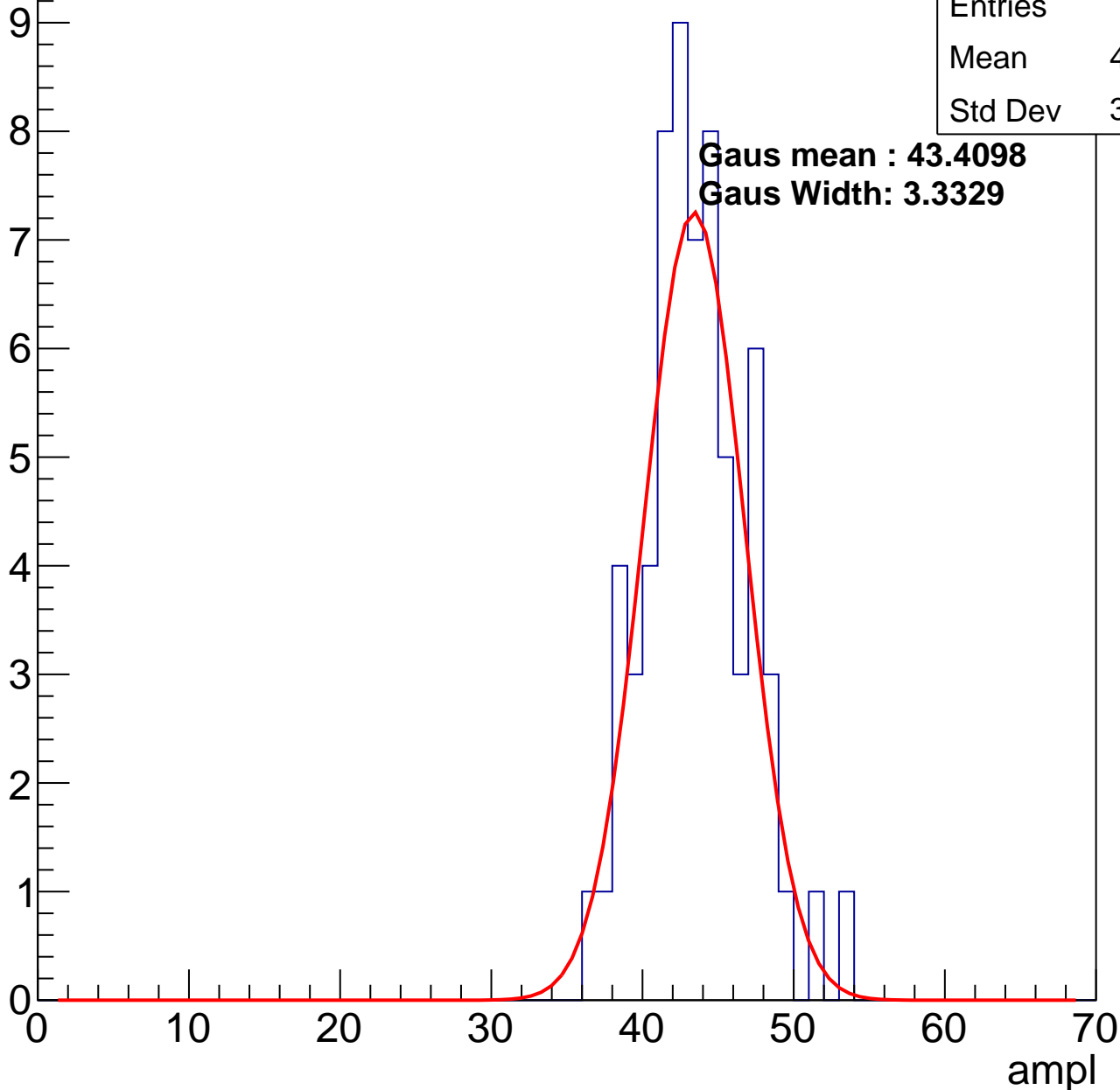
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	43.12
Std Dev	3.363

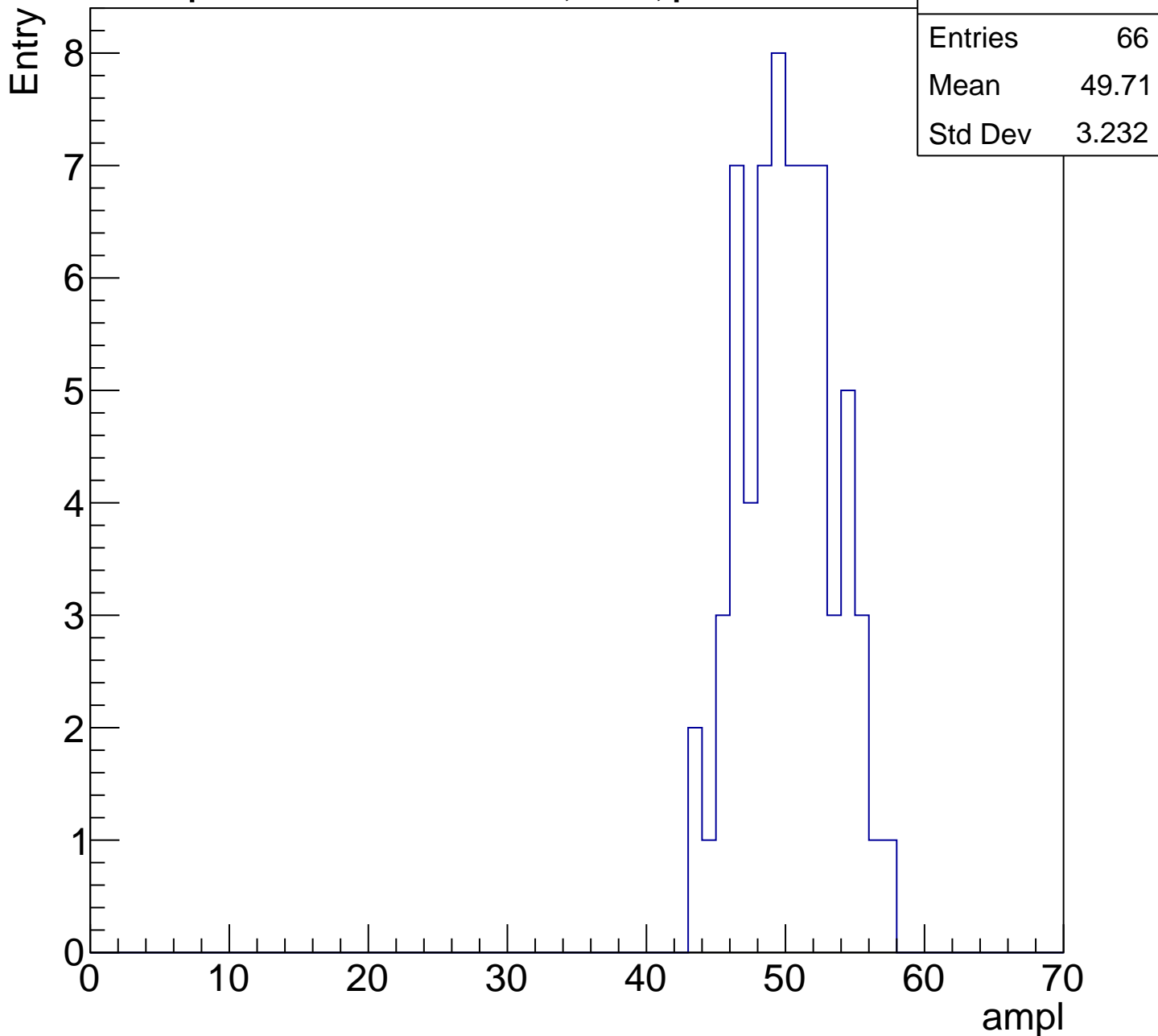
**Gaus mean : 43.4098**

**Gaus Width: 3.3329**



# B1L103S, U16-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

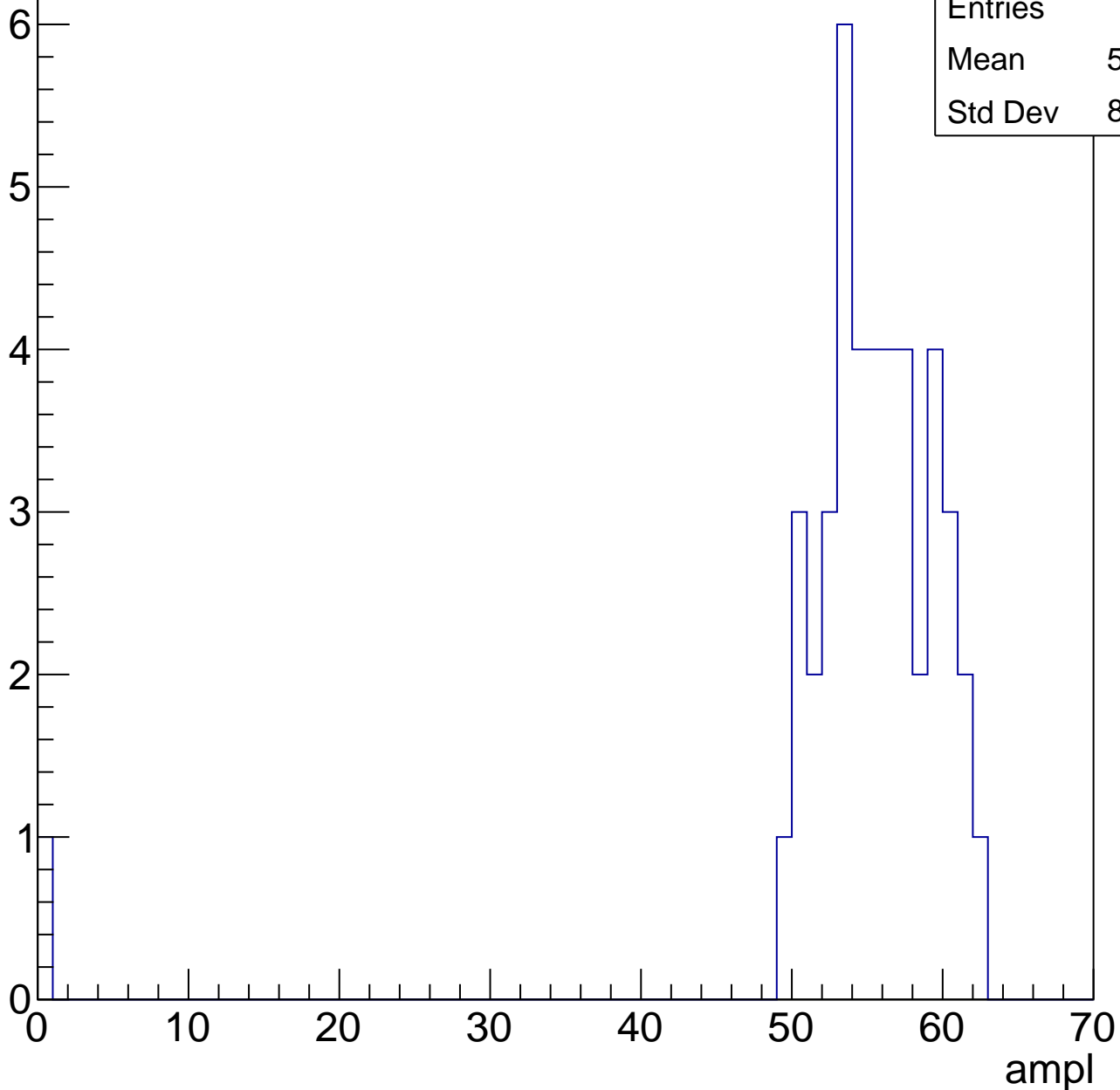


# B1L103S, U16-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

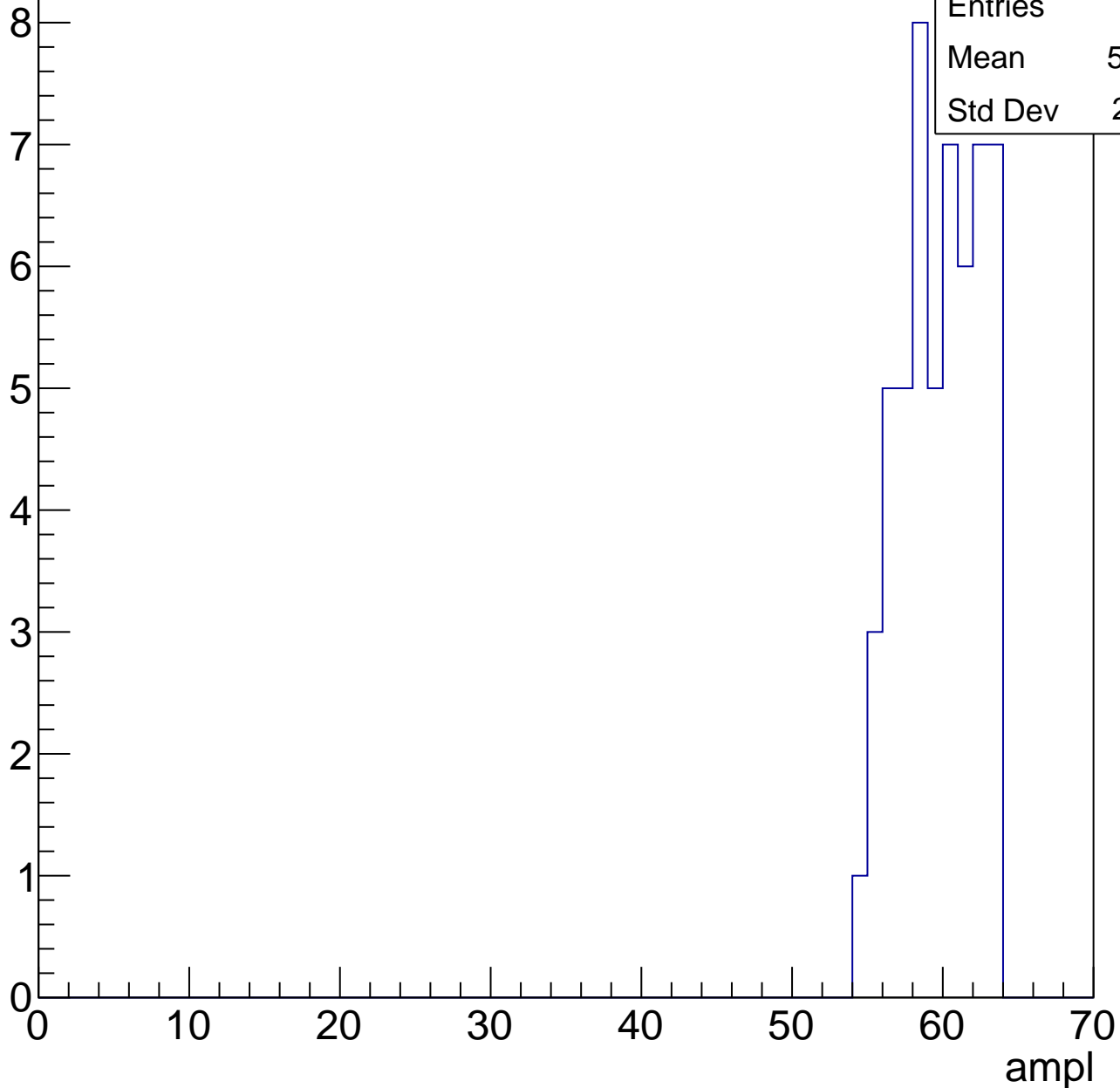
Entries	44
Mean	54.07
Std Dev	8.897



# B1L103S, U16-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

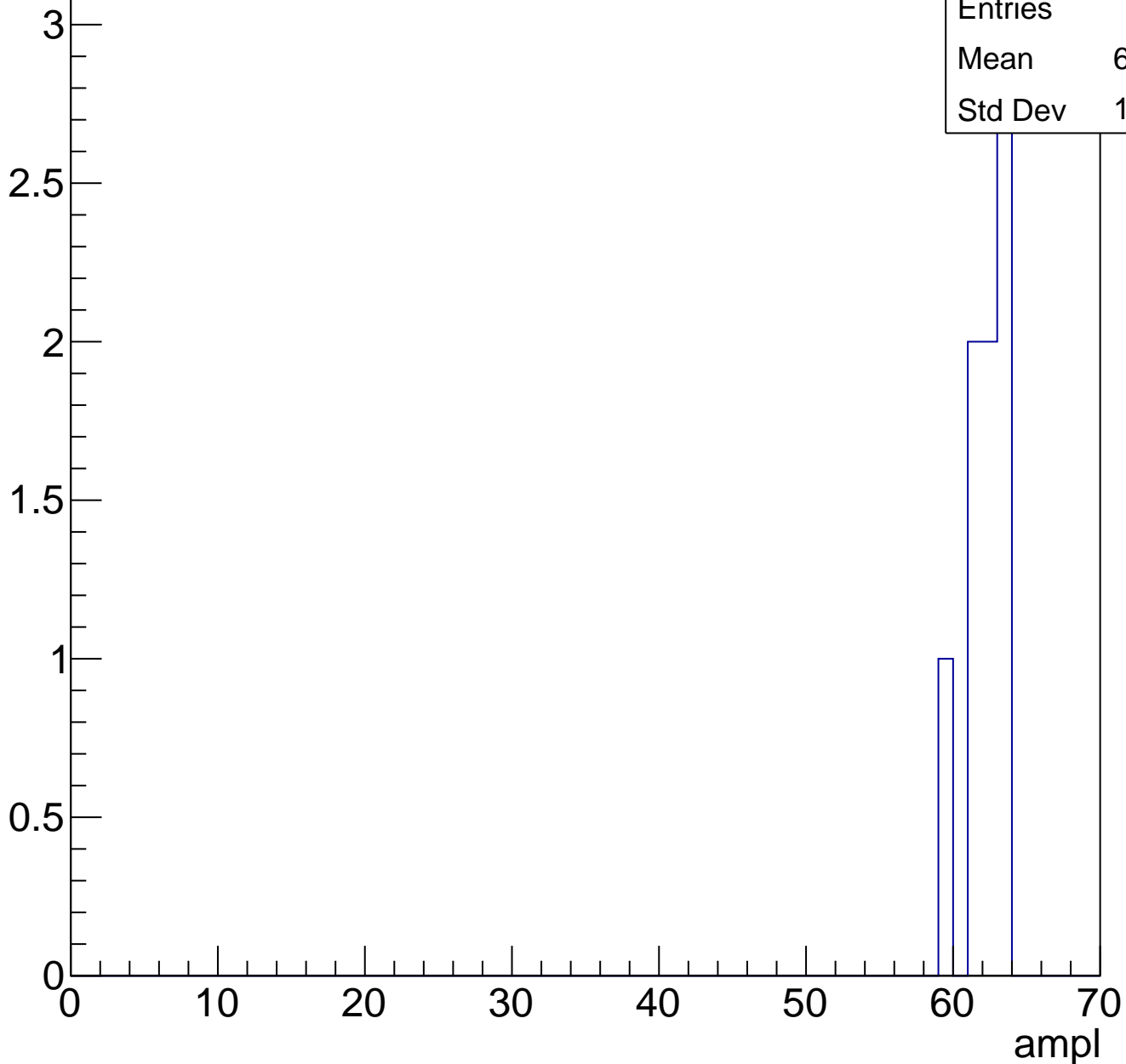


Entries	54
Mean	59.33
Std Dev	2.531

# B1L103S, U16-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U16-ch68, adc0

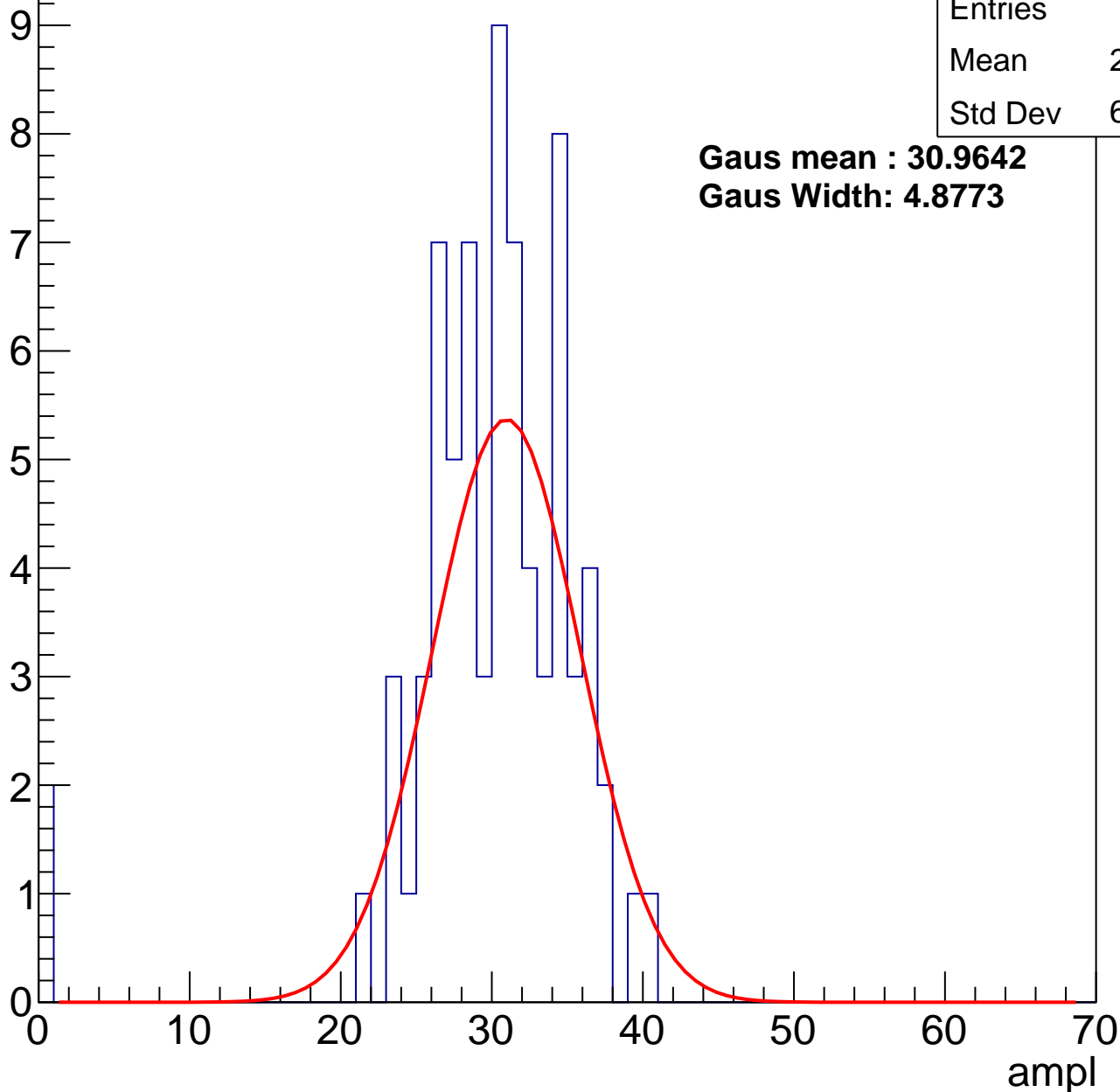
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	29.42
Std Dev	6.344

**Gaus mean : 30.9642**

**Gaus Width: 4.8773**



# B1L103S, U16-ch68, adc1

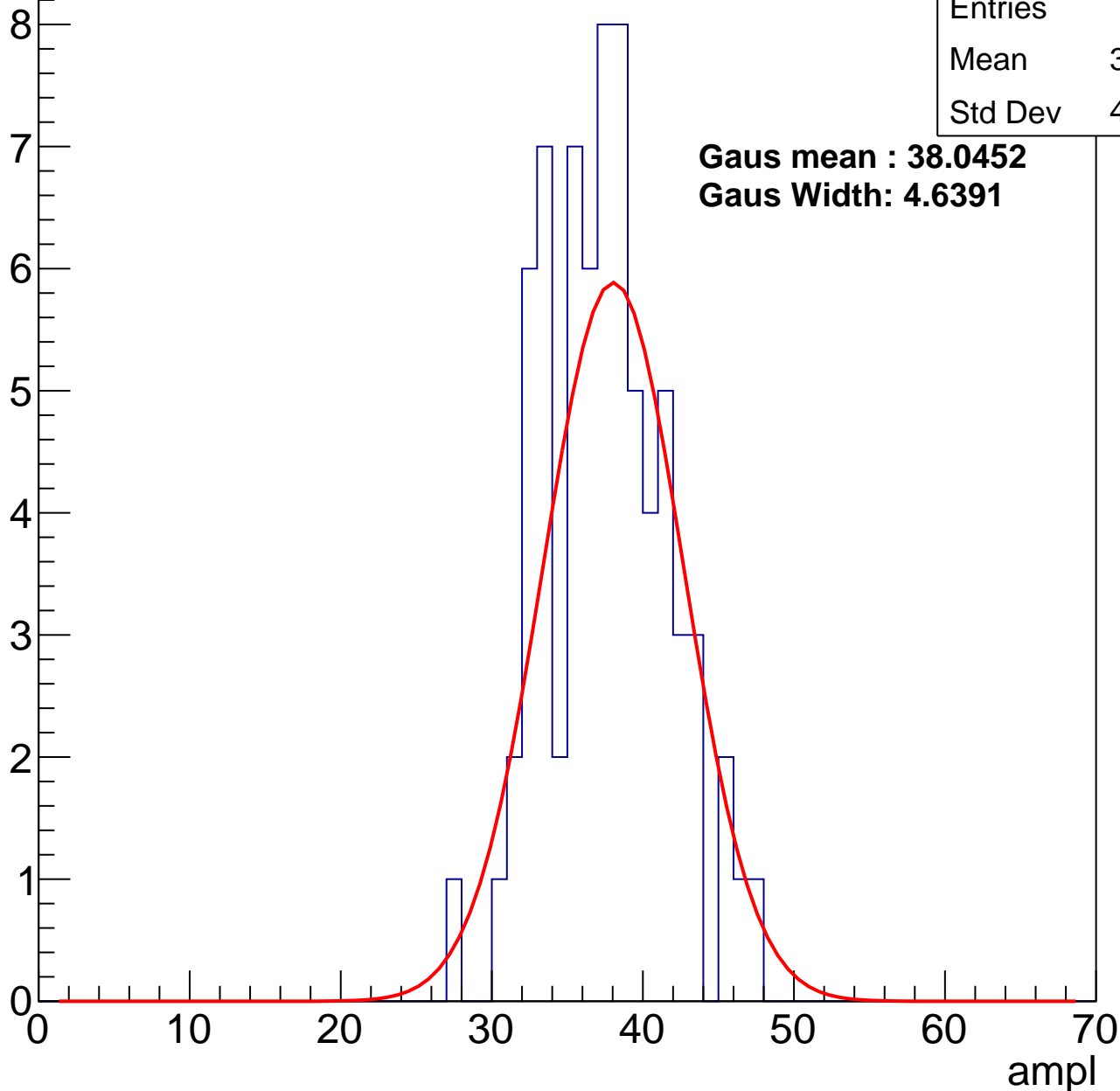
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	37.07
Std Dev	4.032

**Gaus mean : 38.0452**

**Gaus Width: 4.6391**



# B1L103S, U16-ch68, adc2

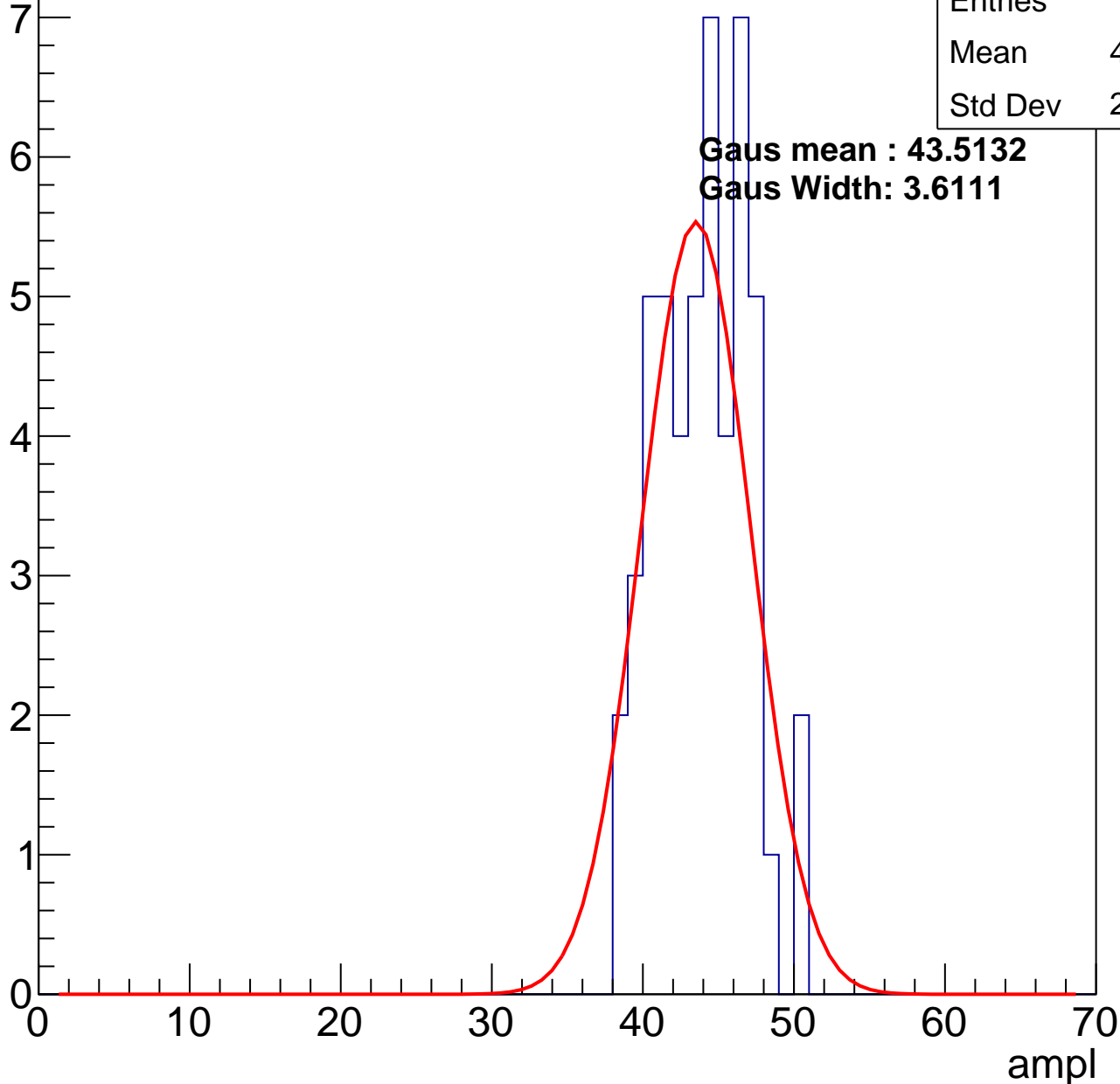
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	43.48
Std Dev	2.982

**Gaus mean : 43.5132**

**Gaus Width: 3.6111**



# B1L103S, U16-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

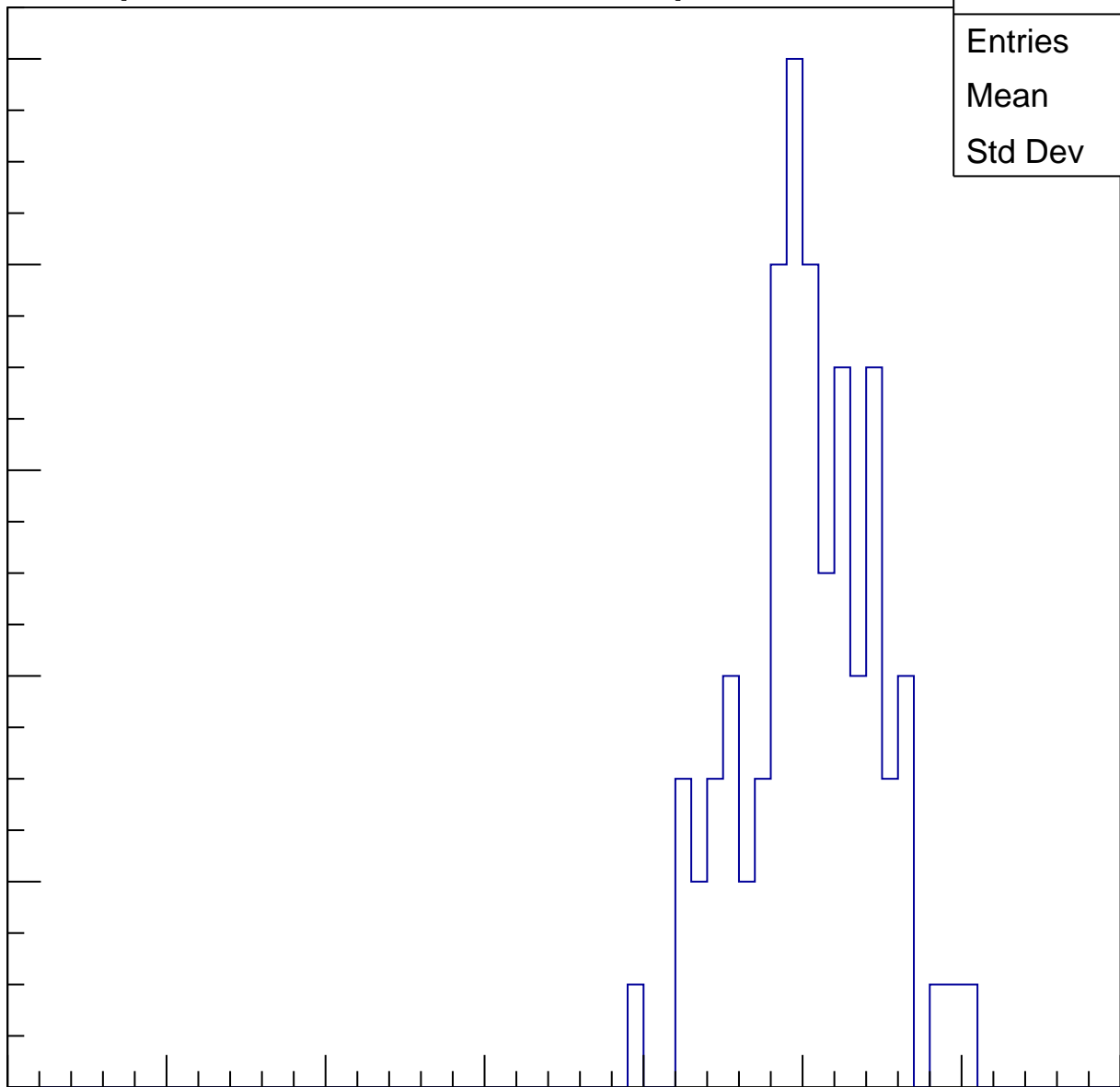
Entries	77
Mean	49.94
Std Dev	4.21

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

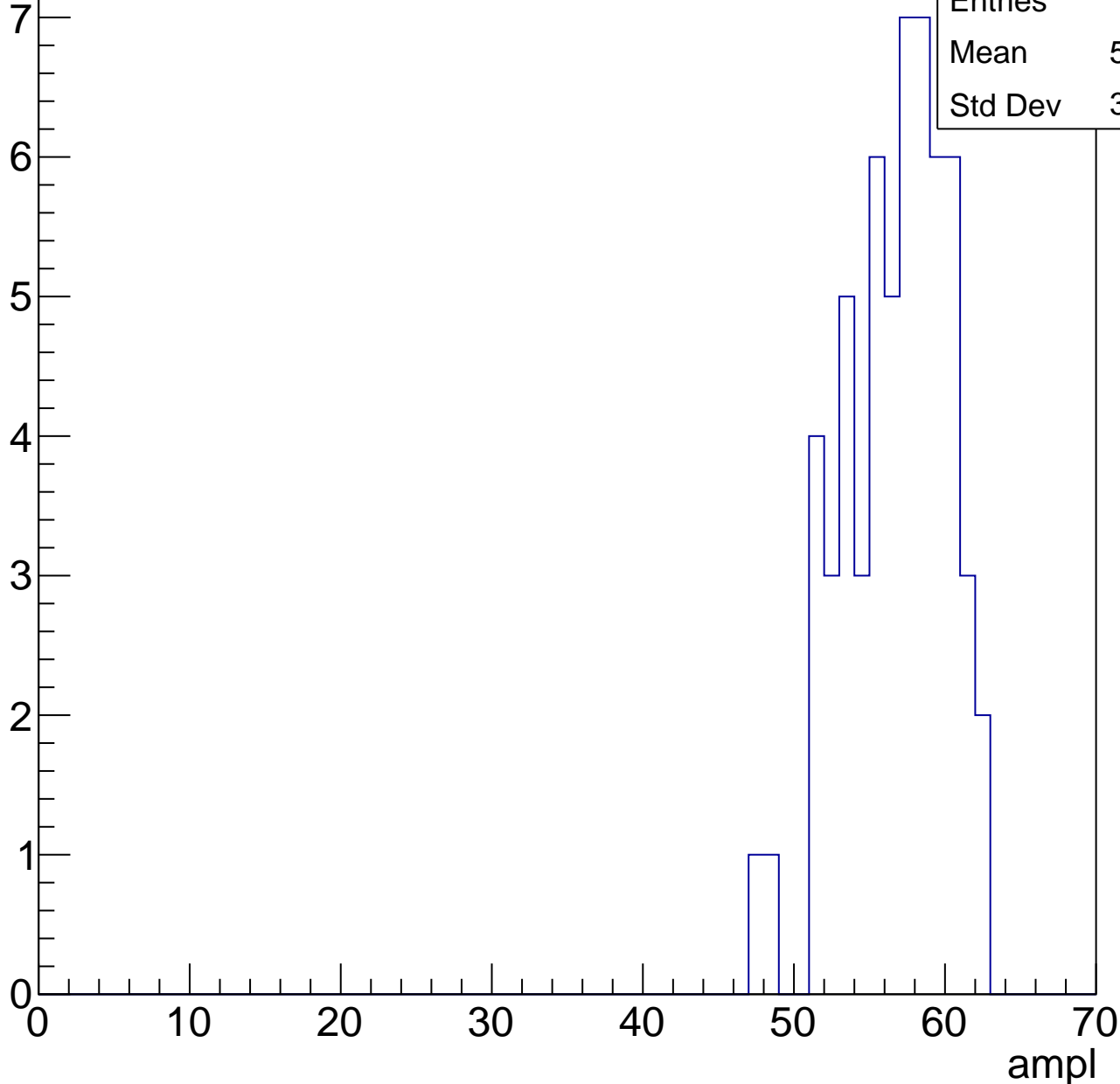


# B1L103S, U16-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	56.24
Std Dev	3.407

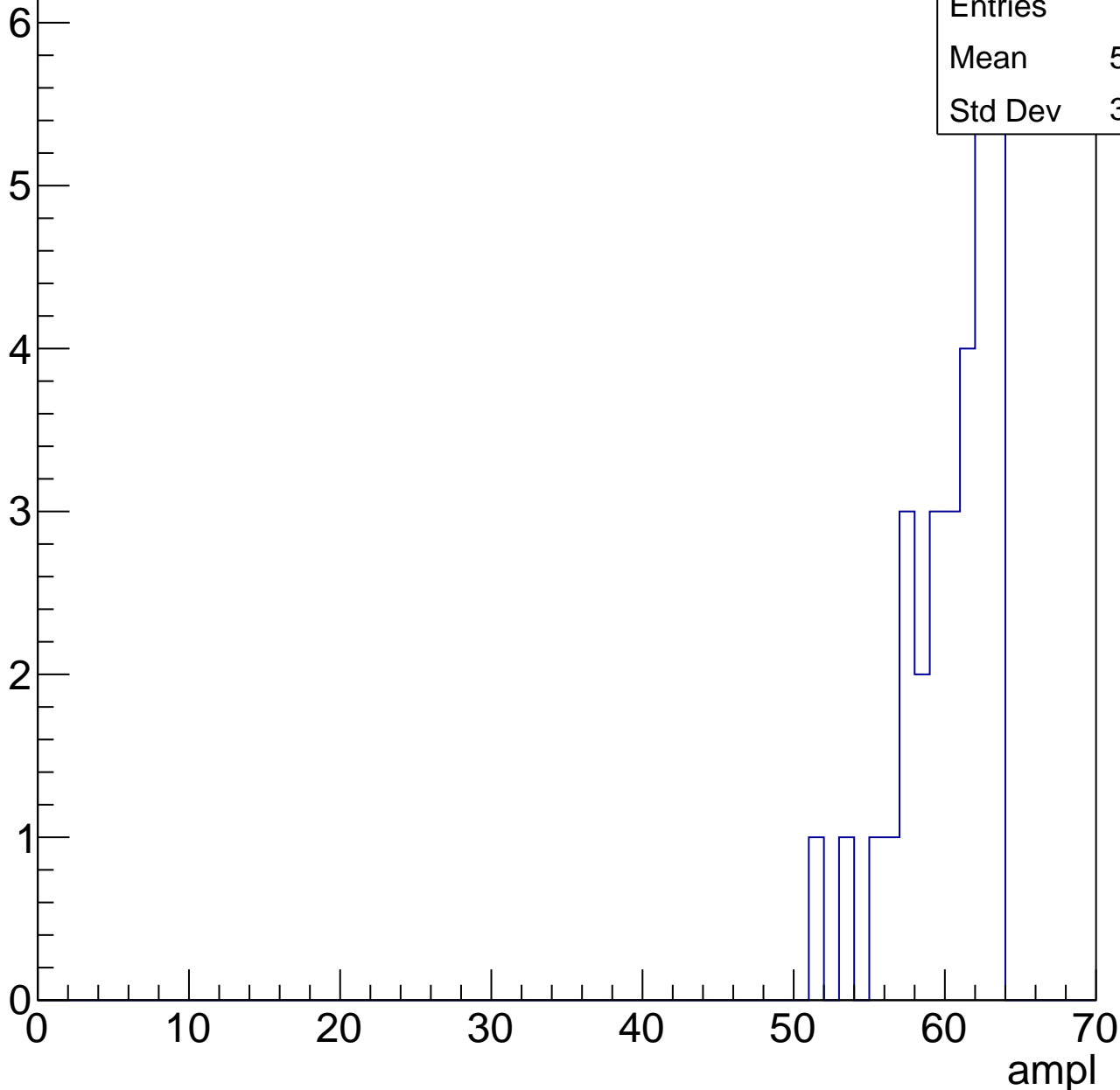


# B1L103S, U16-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

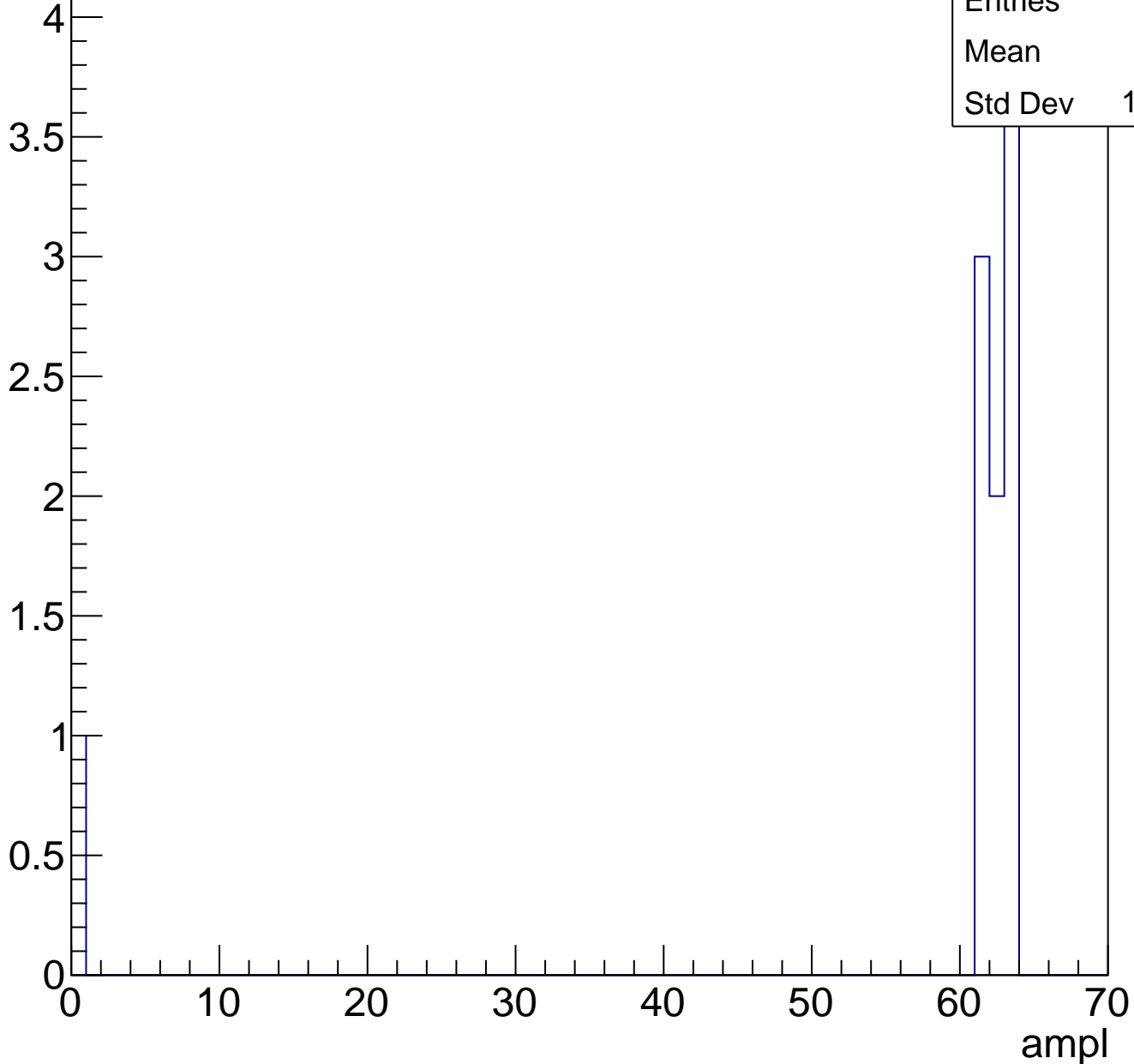
Entries	31
Mean	59.77
Std Dev	3.056



# B1L103S, U16-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch69, adc0

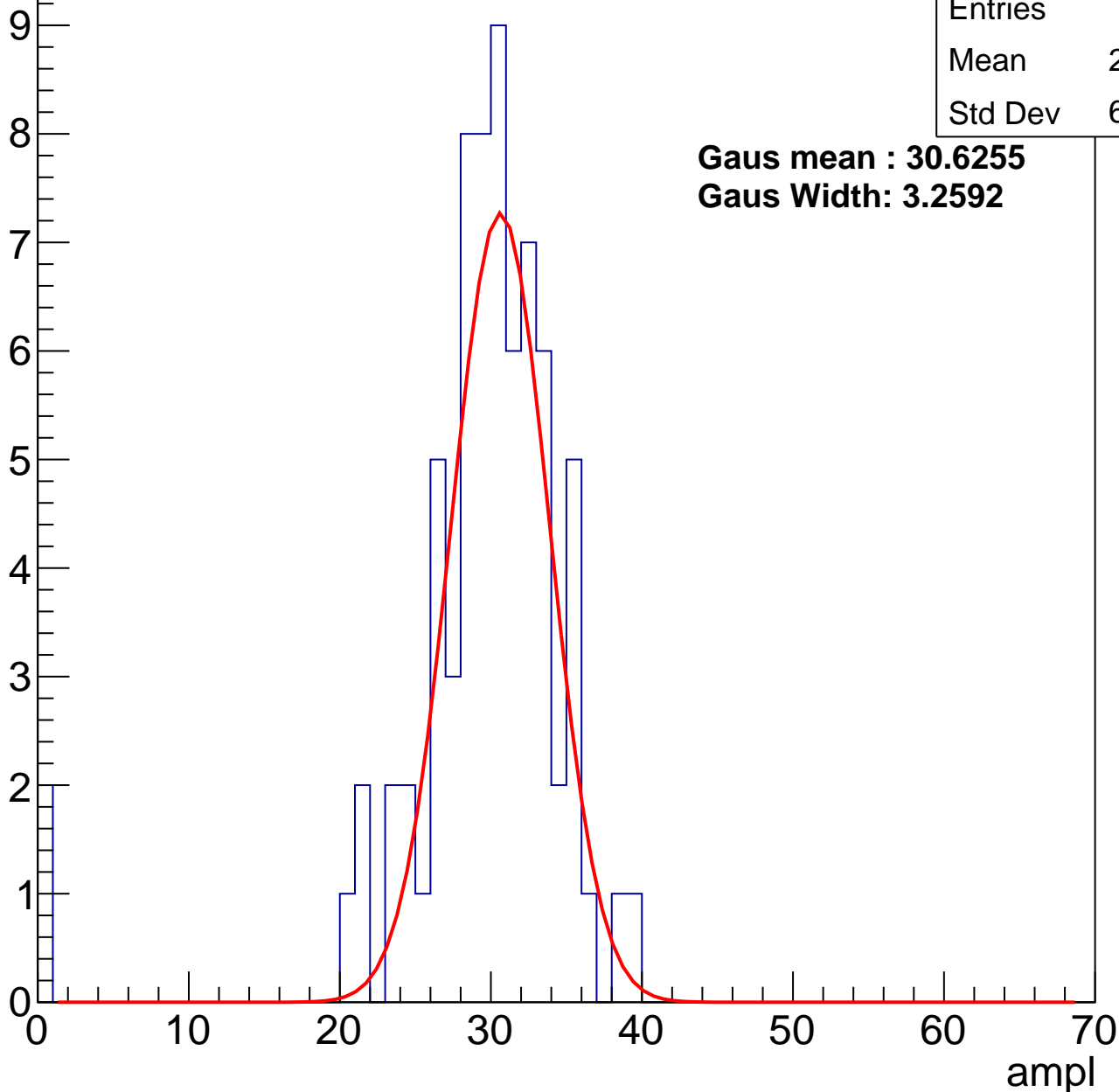
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	28.92
Std Dev	6.175

**Gaus mean : 30.6255**

**Gaus Width: 3.2592**



# B1L103S, U16-ch69, adc1

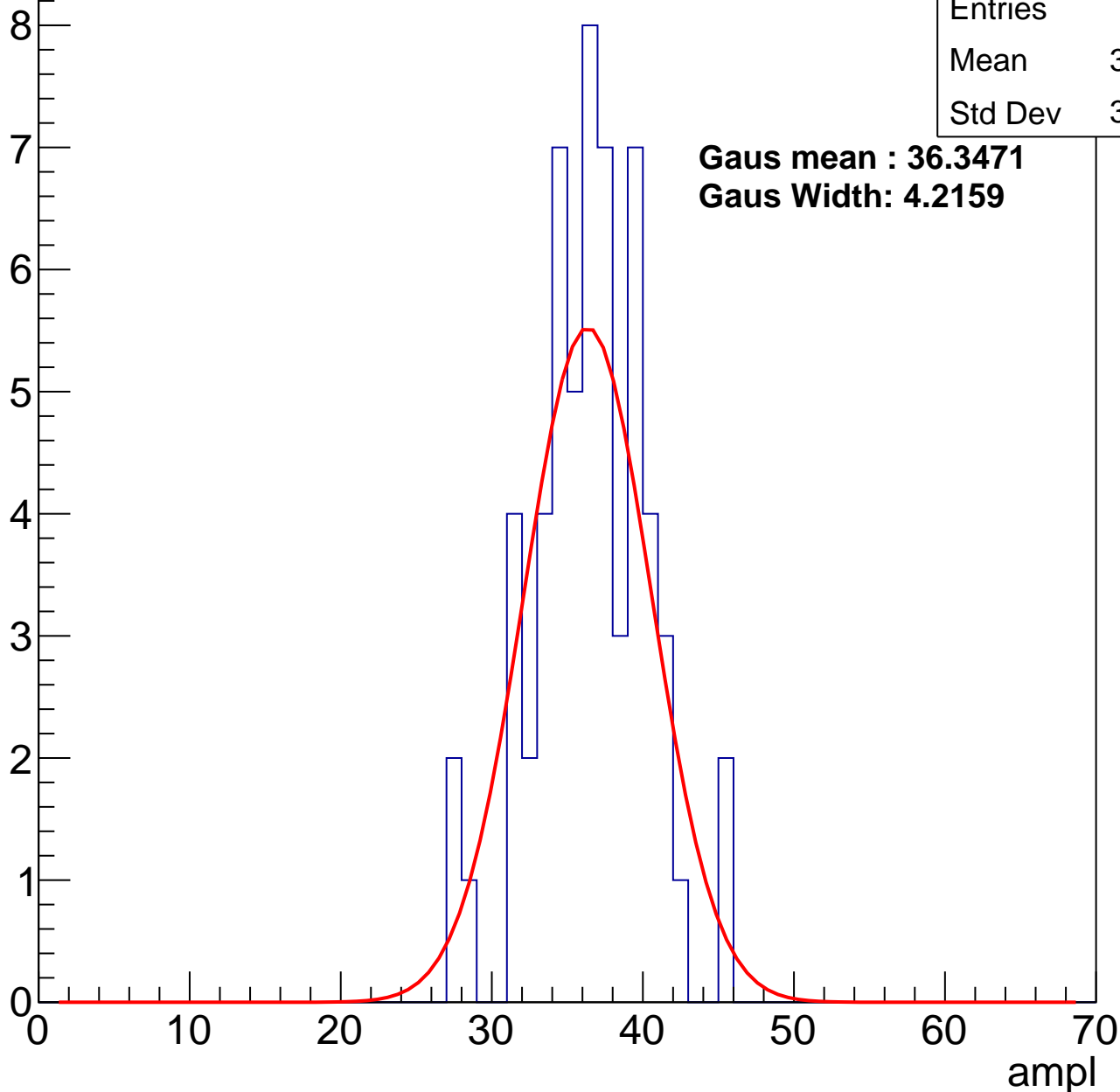
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	36.07
Std Dev	3.754

**Gaus mean : 36.3471**

**Gaus Width: 4.2159**



# B1L103S, U16-ch69, adc2

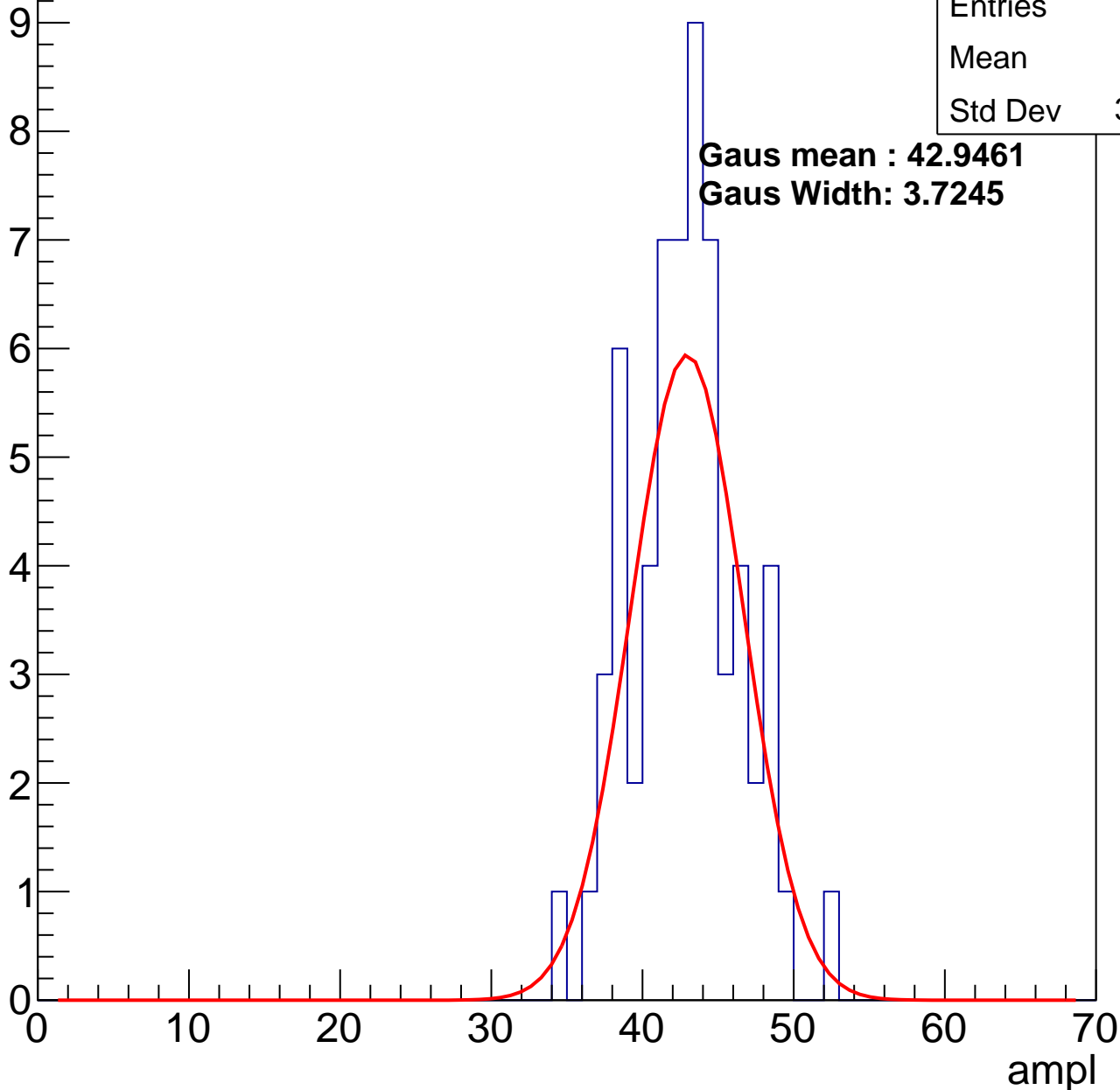
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	42.4
Std Dev	3.531

**Gaus mean : 42.9461**

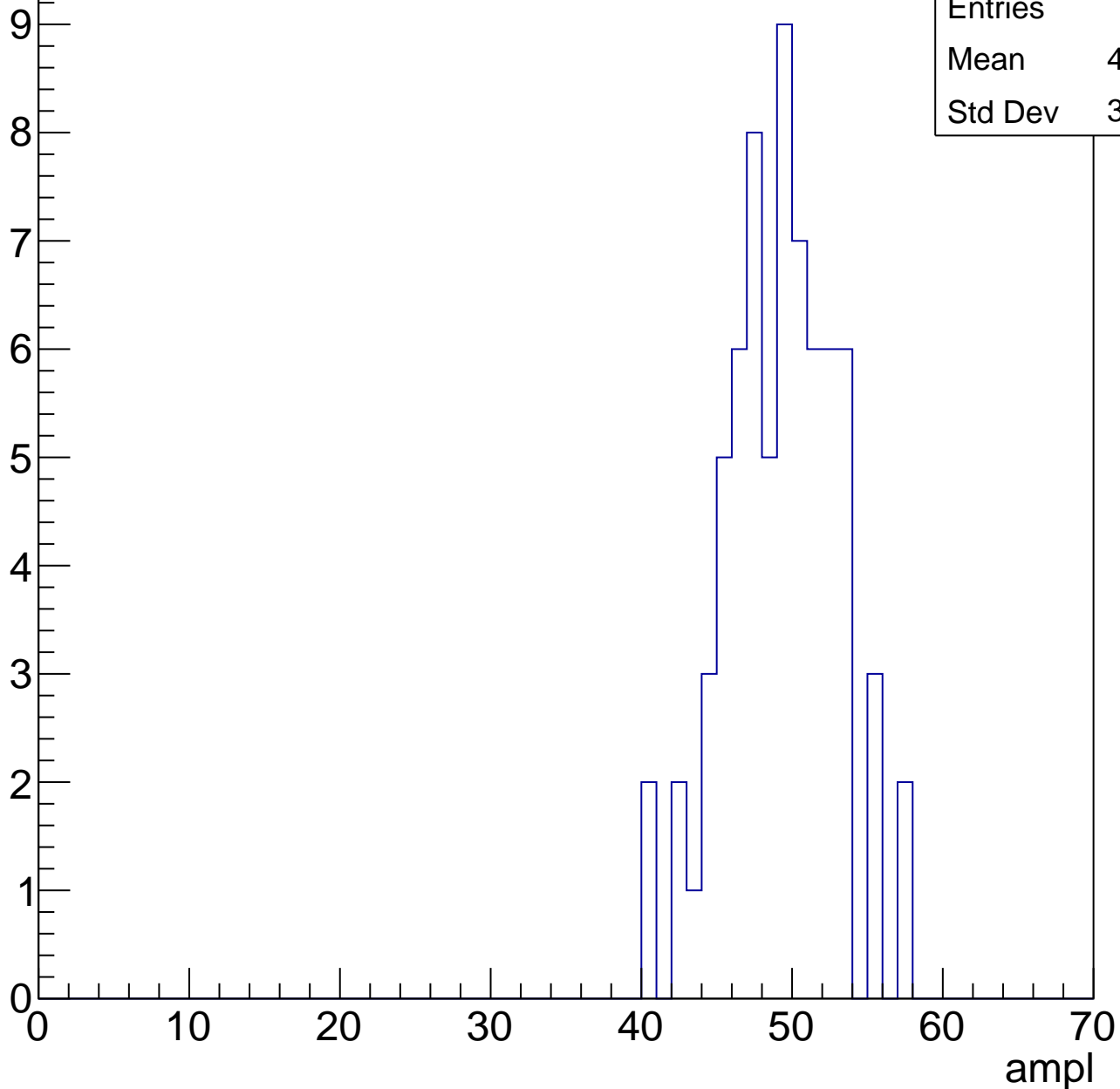
**Gaus Width: 3.7245**



# B1L103S, U16-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

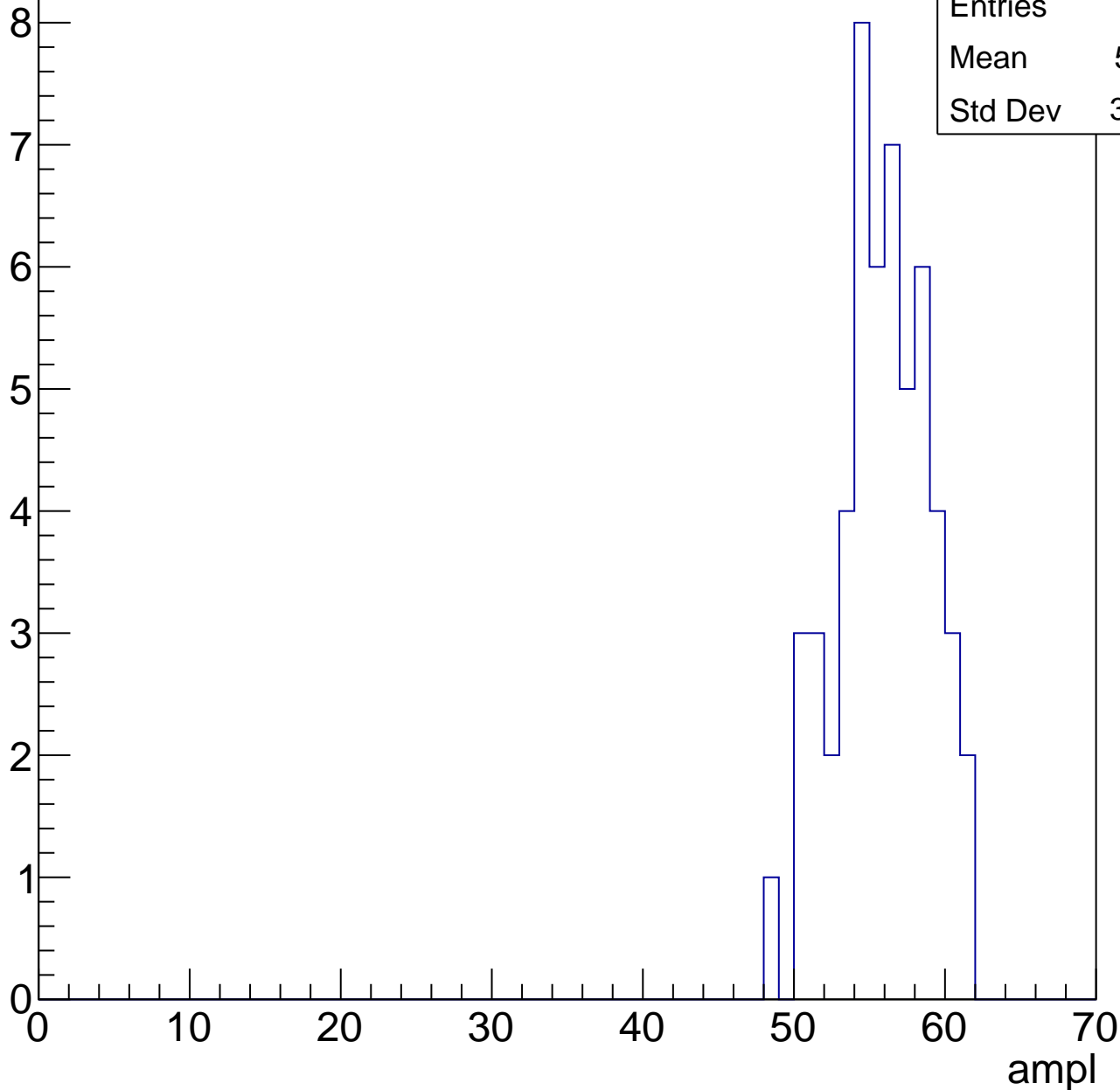


# B1L103S, U16-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	55.41
Std Dev	3.034



# B1L103S, U16-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

7

6

5

4

3

2

1

0

Entries 41

Mean 57.83

Std Dev 9.637

ampl

0

10

20

30

40

50

60

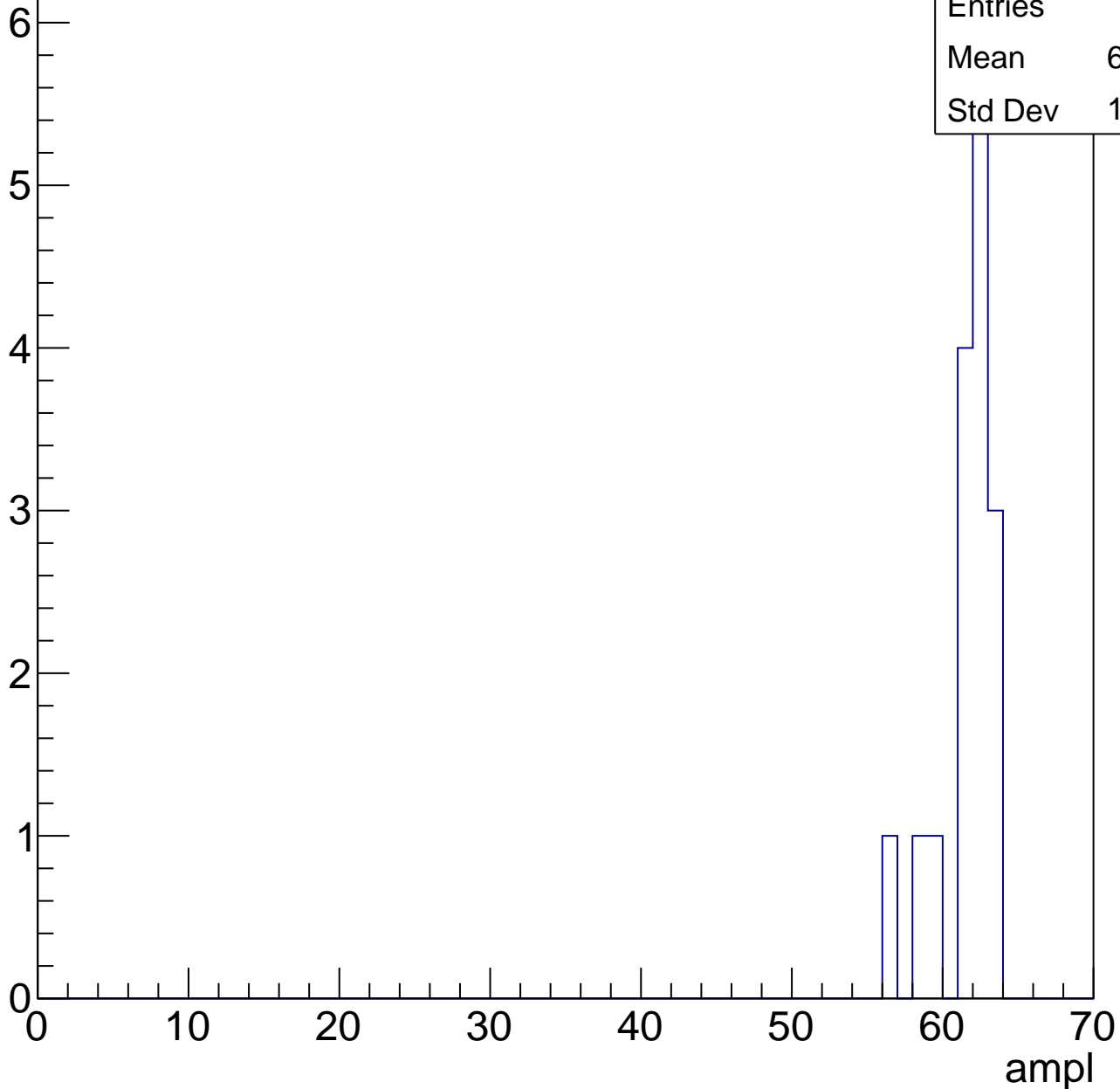
70

# B1L103S, U16-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	16
Mean	61.12
Std Dev	1.867





# B1L103S, U16-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch70, adc0

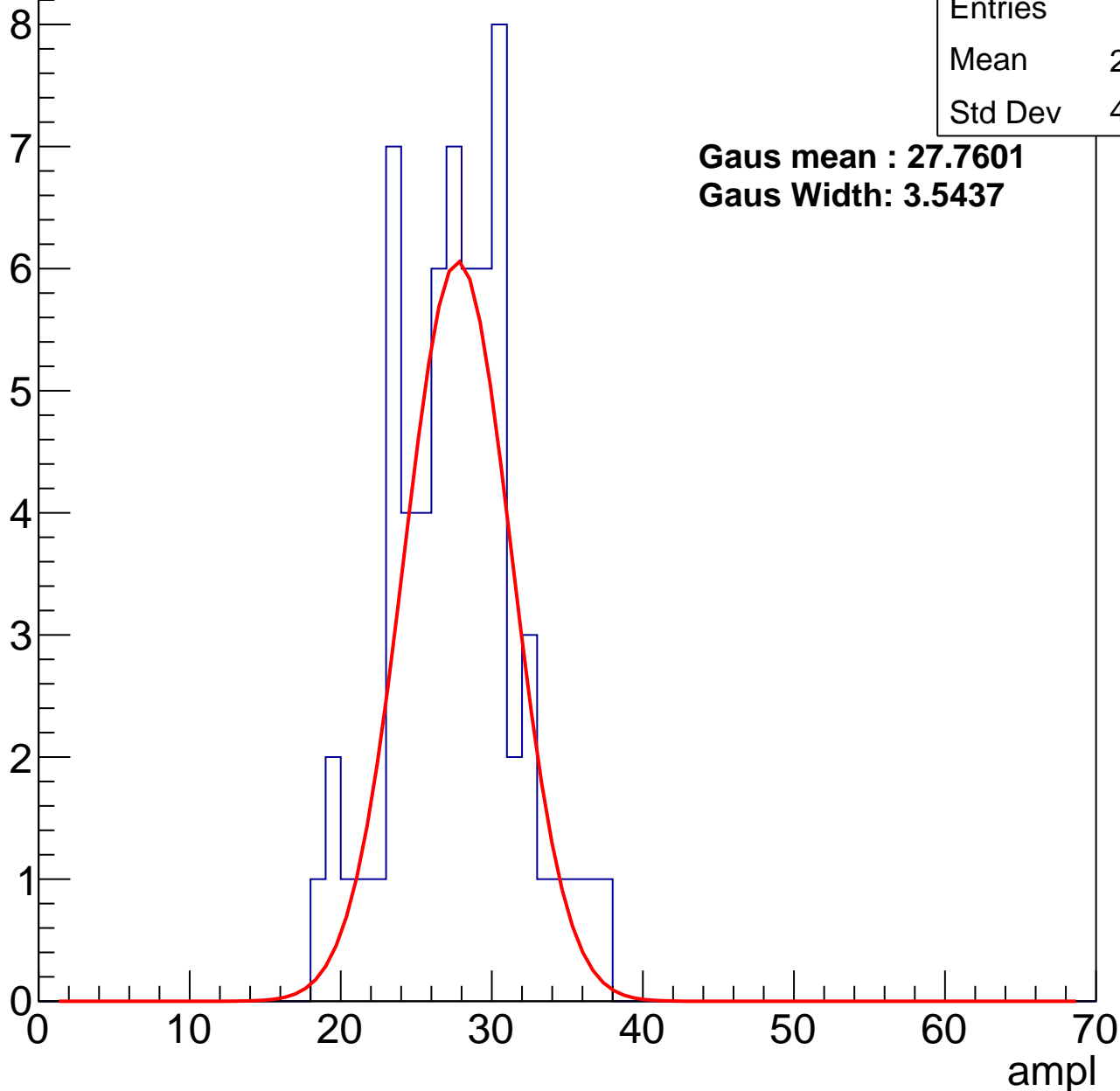
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	27.12
Std Dev	4.006

**Gaus mean : 27.7601**

**Gaus Width: 3.5437**



# B1L103S, U16-ch70, adc1

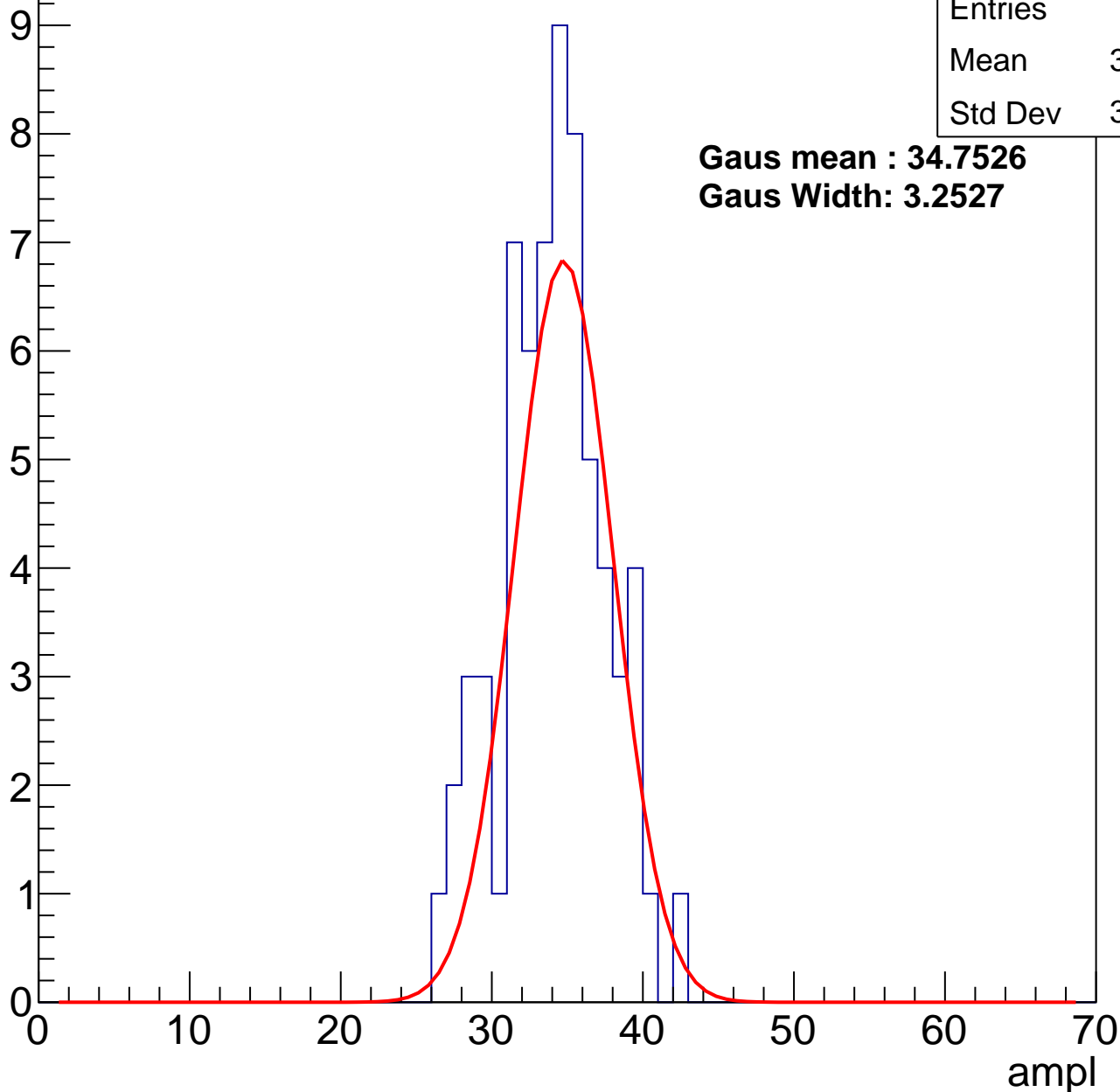
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	33.65
Std Dev	3.417

**Gaus mean : 34.7526**

**Gaus Width: 3.2527**



# B1L103S, U16-ch70, adc2

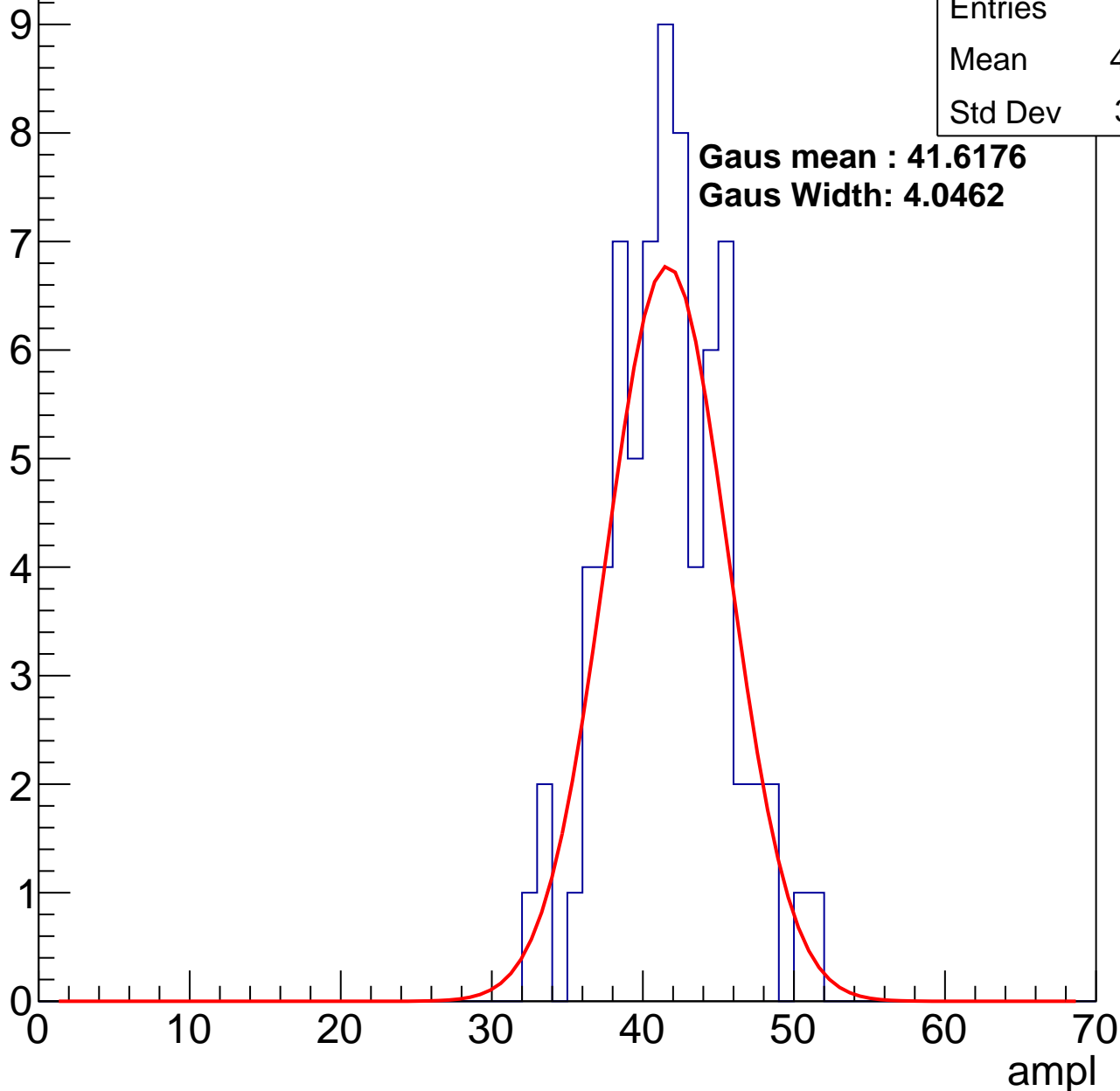
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	41.16
Std Dev	3.861

**Gaus mean : 41.6176**

**Gaus Width: 4.0462**

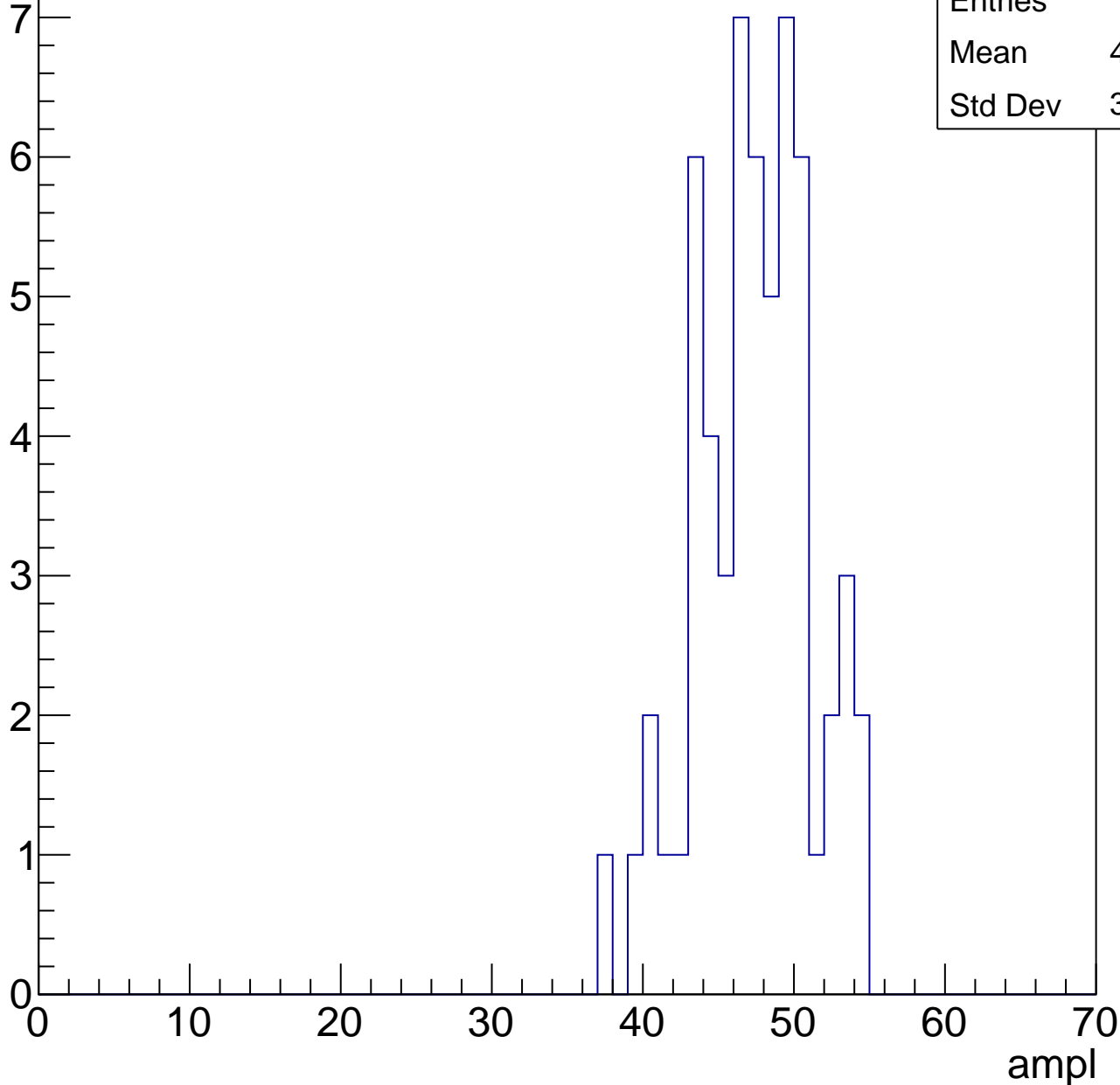


# B1L103S, U16-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	46.84
Std Dev	3.787

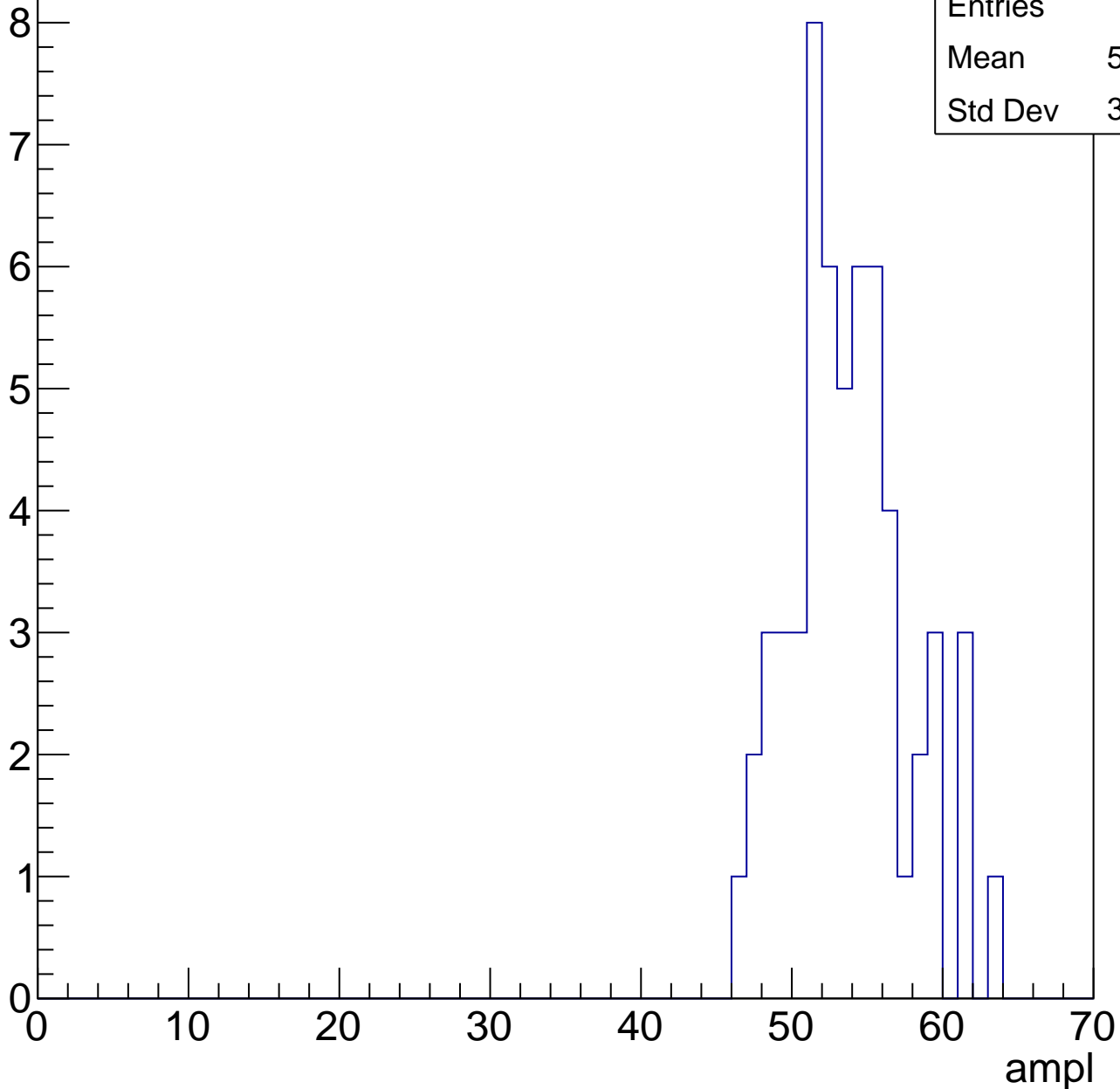


# B1L103S, U16-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

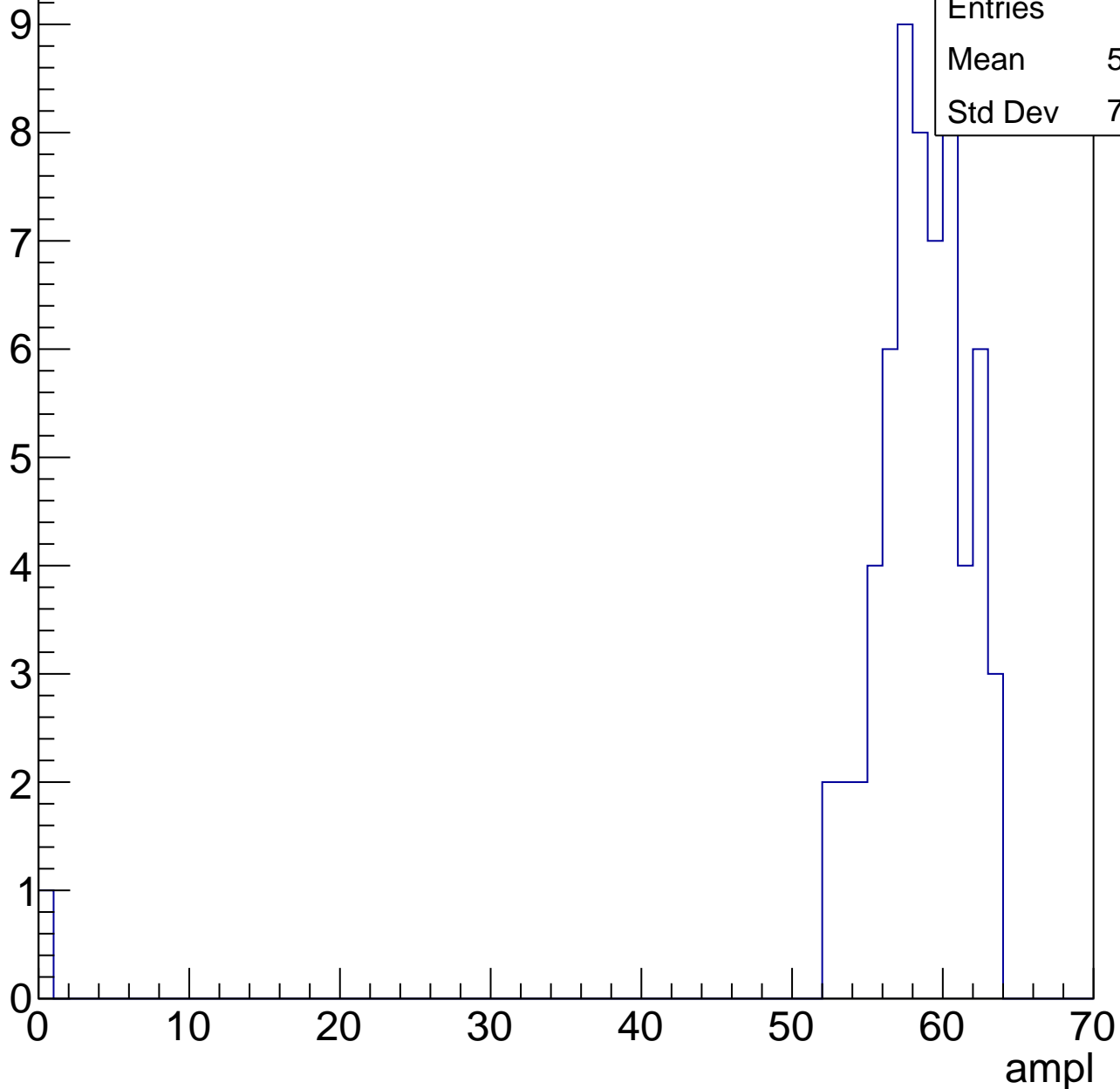
Entries	57
Mean	53.33
Std Dev	3.827



# B1L103S, U16-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

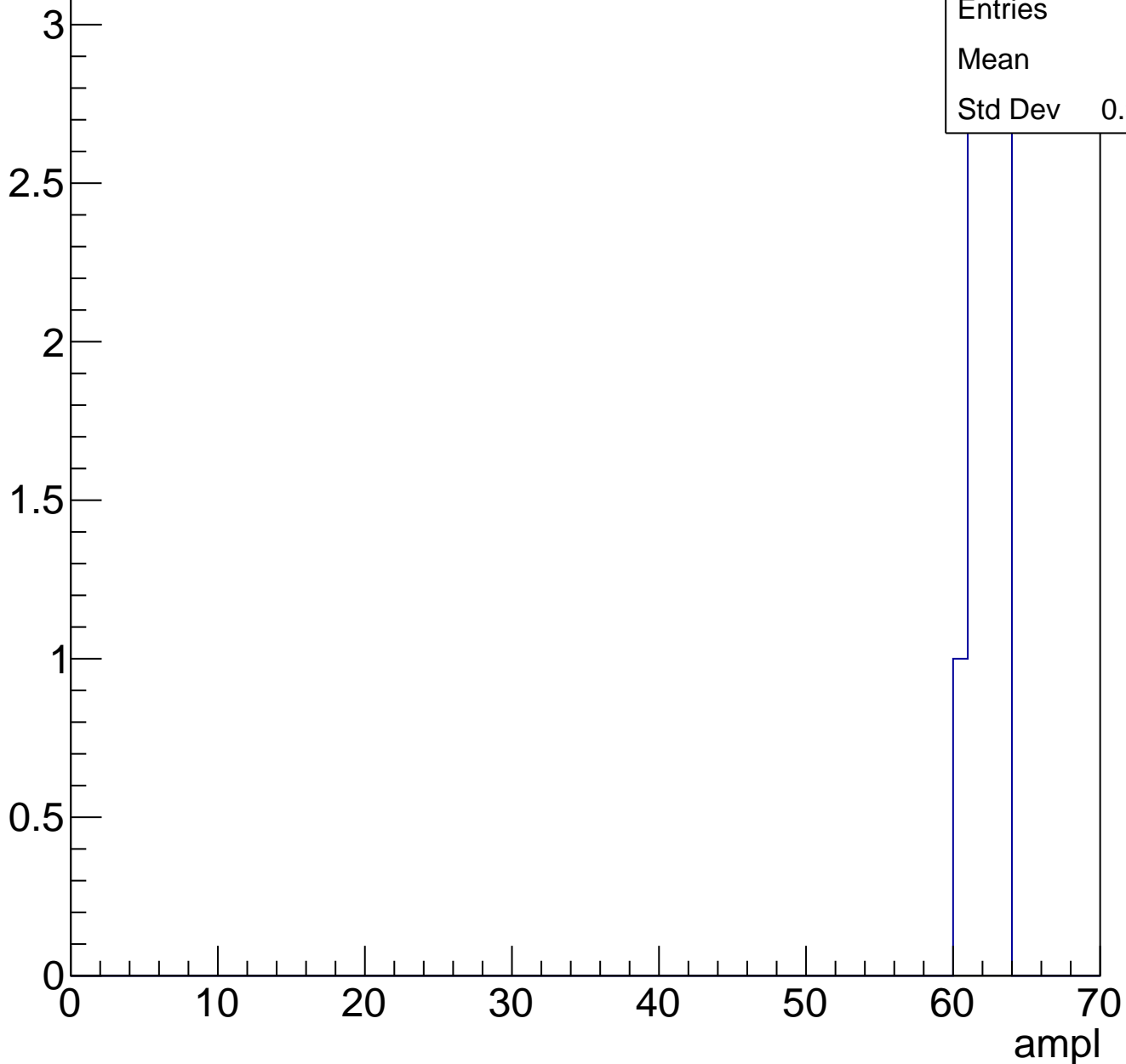


Entries	62
Mean	57.24
Std Dev	7.826

# B1L103S, U16-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

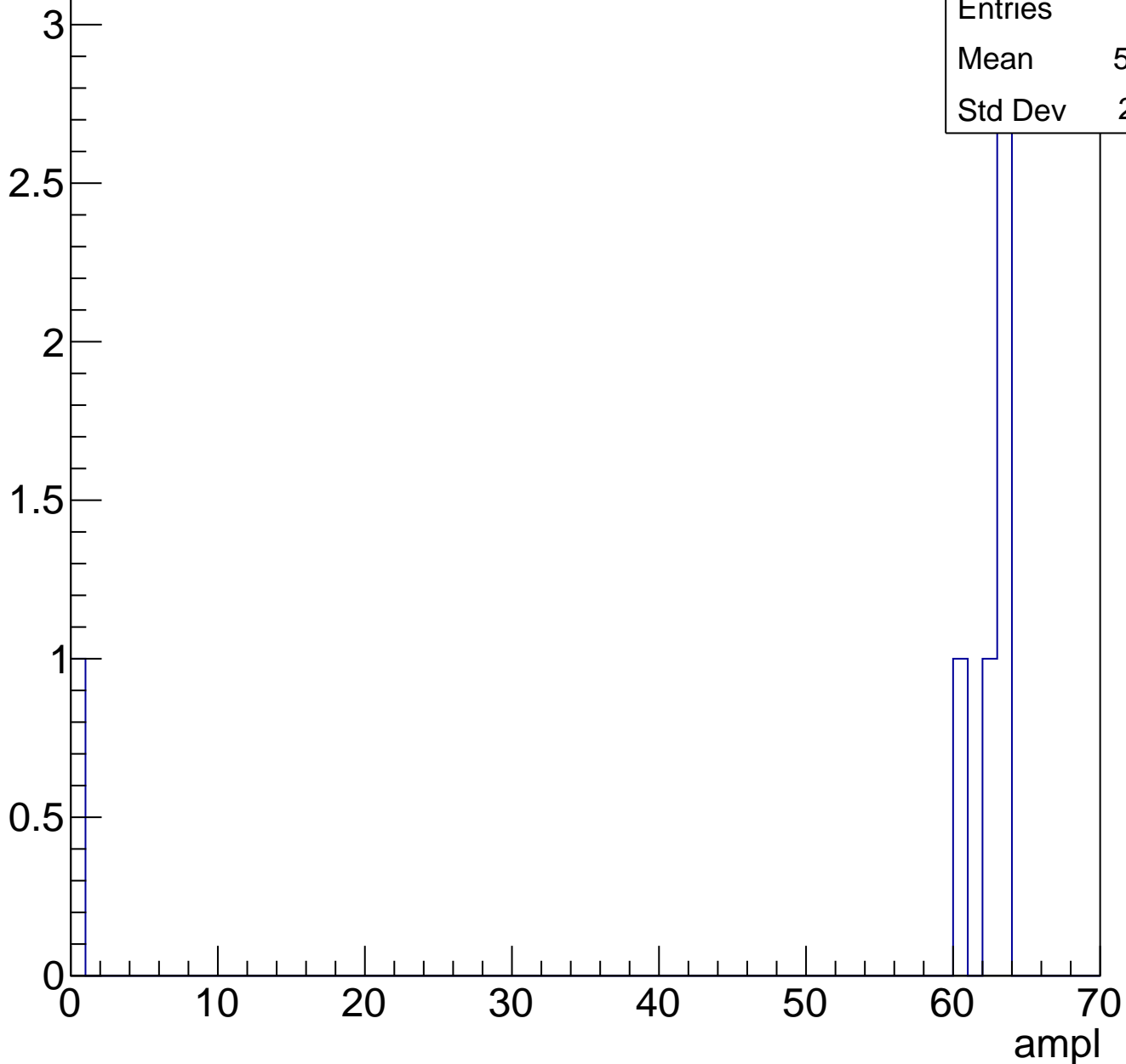




# B1L103S, U16-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch71, adc0

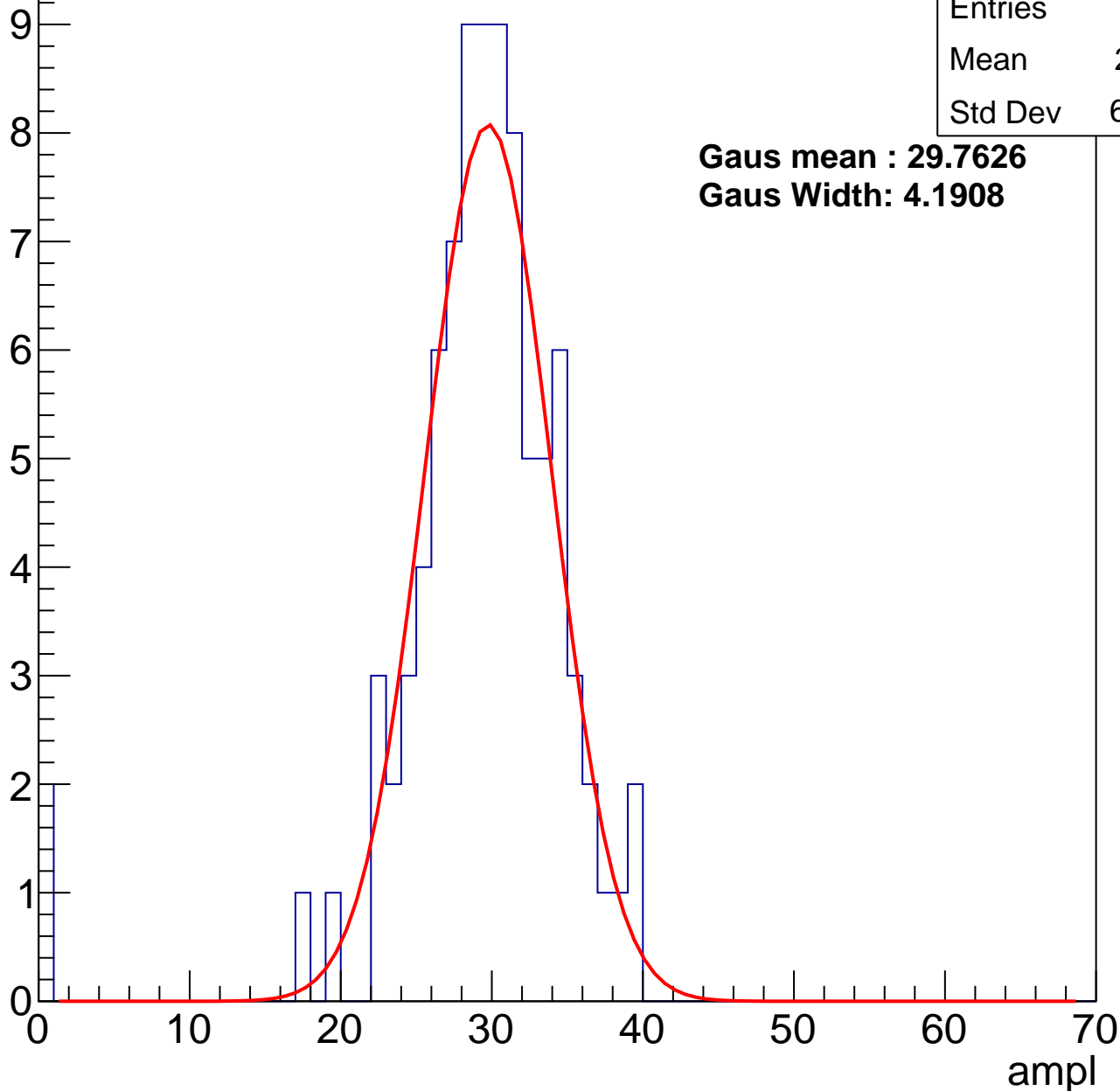
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	89
Mean	28.71
Std Dev	6.028

**Gaus mean : 29.7626**

**Gaus Width: 4.1908**



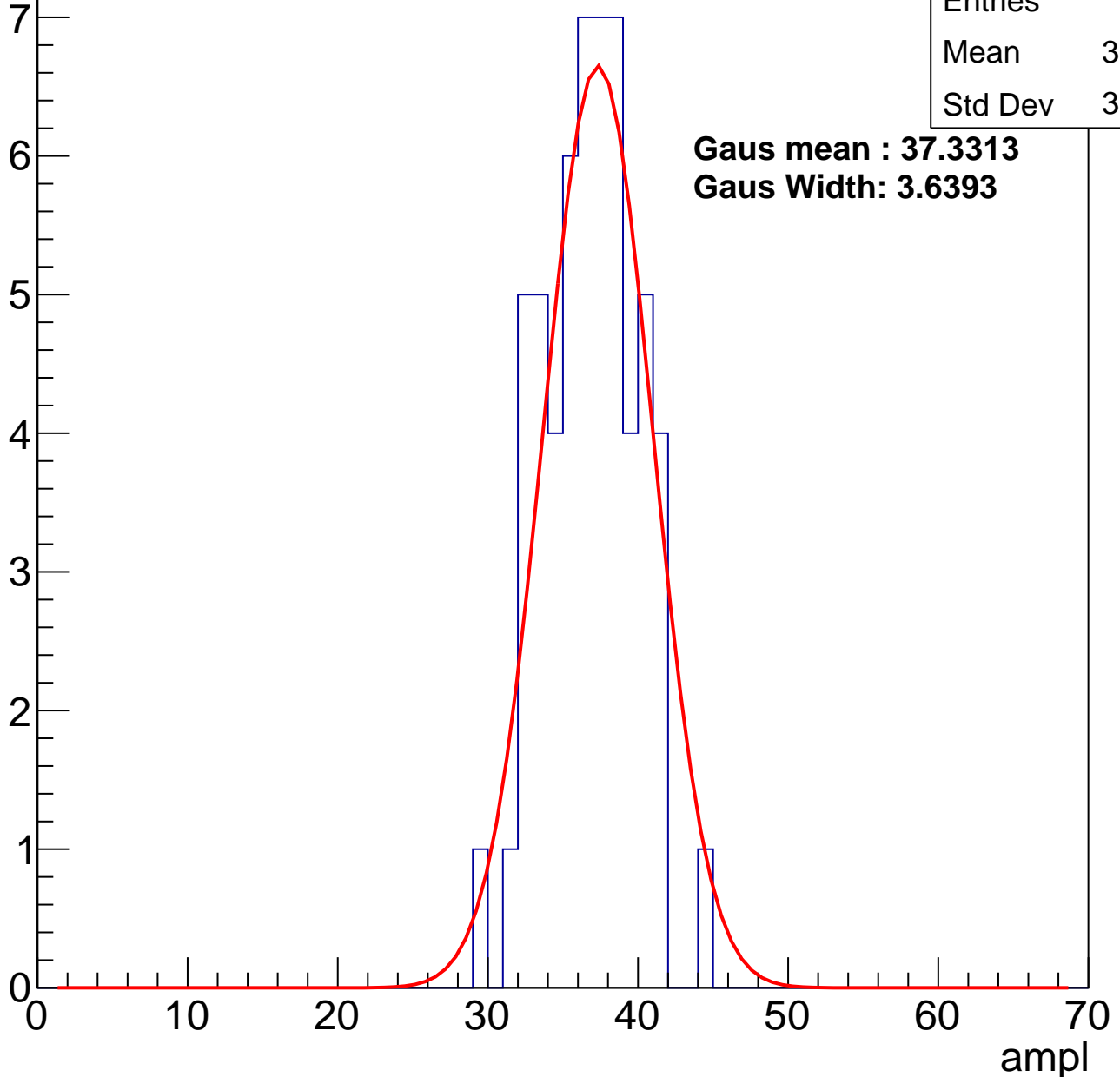
# B1L103S, U16-ch71, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	36.35
Std Dev	3.046

**Gaus mean : 37.3313**  
**Gaus Width: 3.6393**



# B1L103S, U16-ch71, adc2

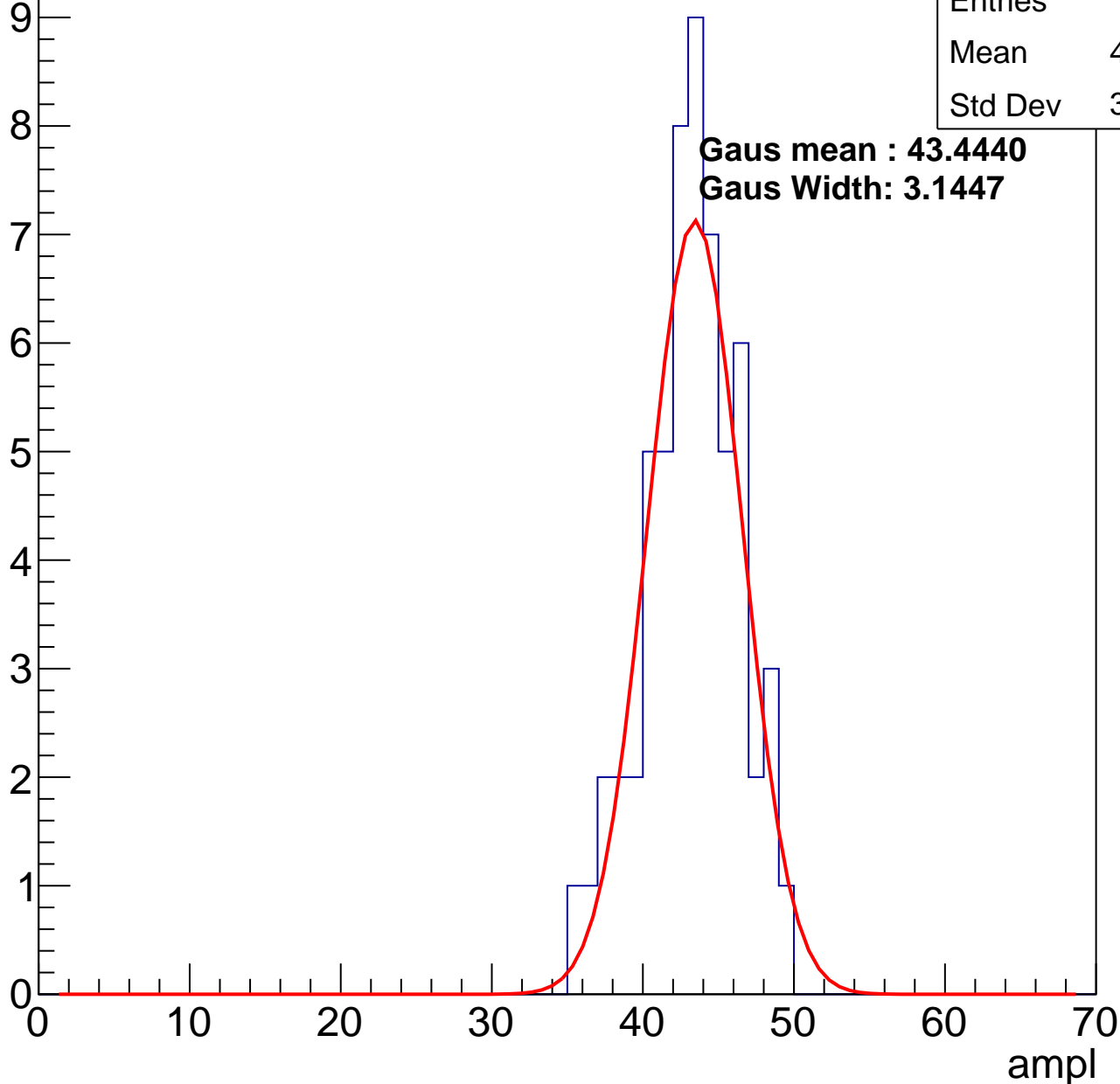
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	42.76
Std Dev	3.083

**Gaus mean : 43.4440**

**Gaus Width: 3.1447**

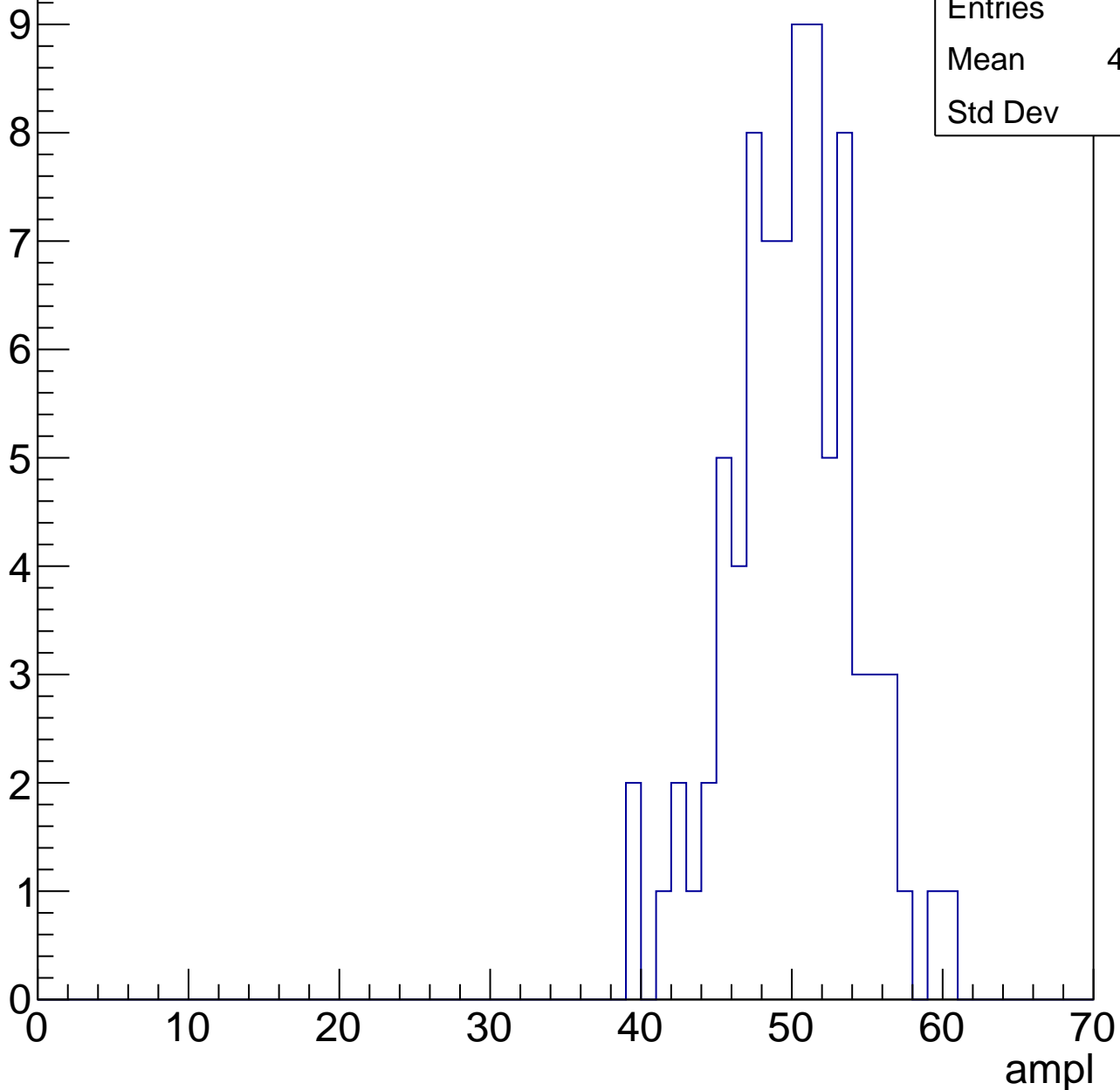


# B1L103S, U16-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	82
Mean	49.54
Std Dev	4.15

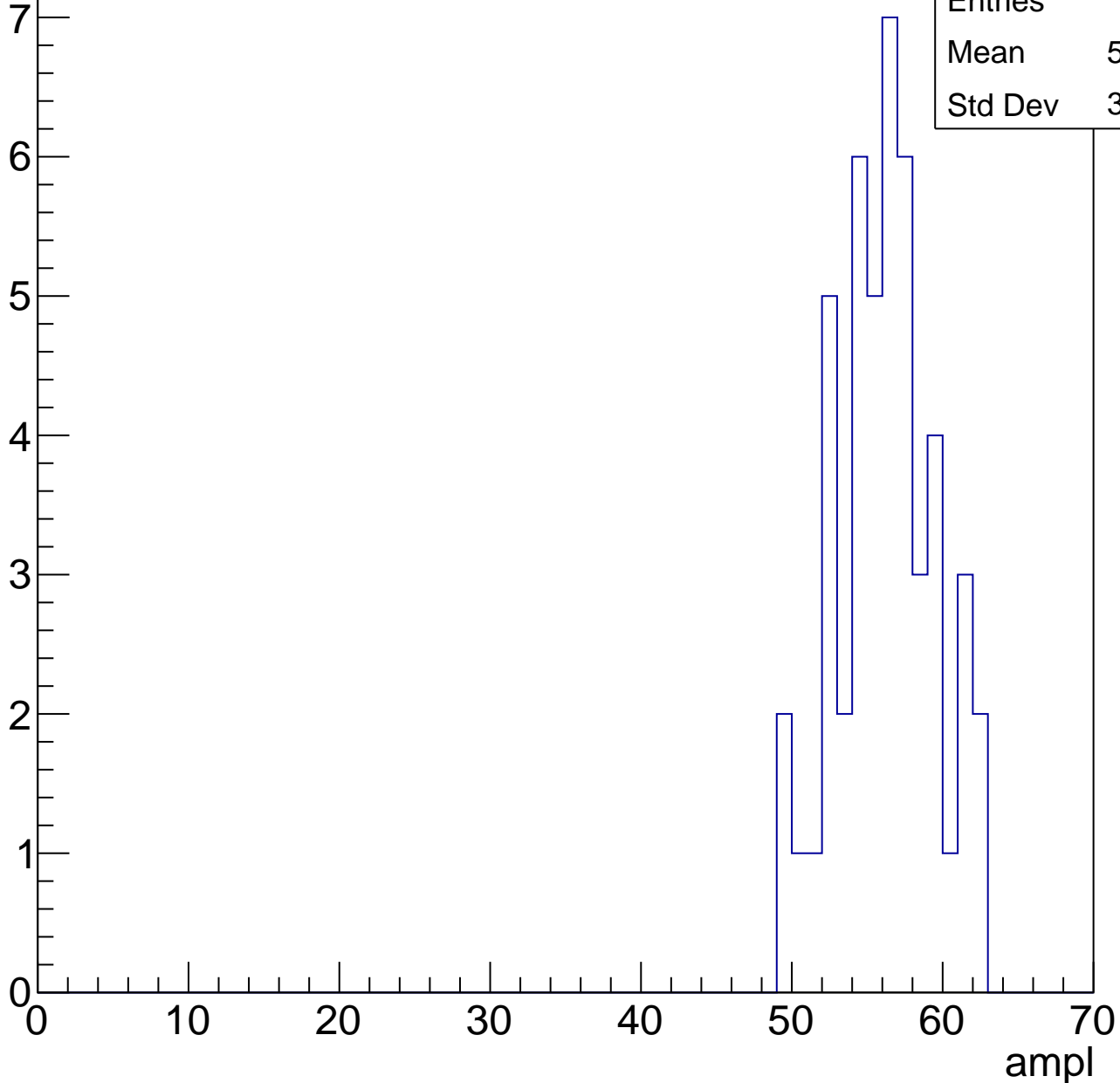


# B1L103S, U16-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	55.73
Std Dev	3.226

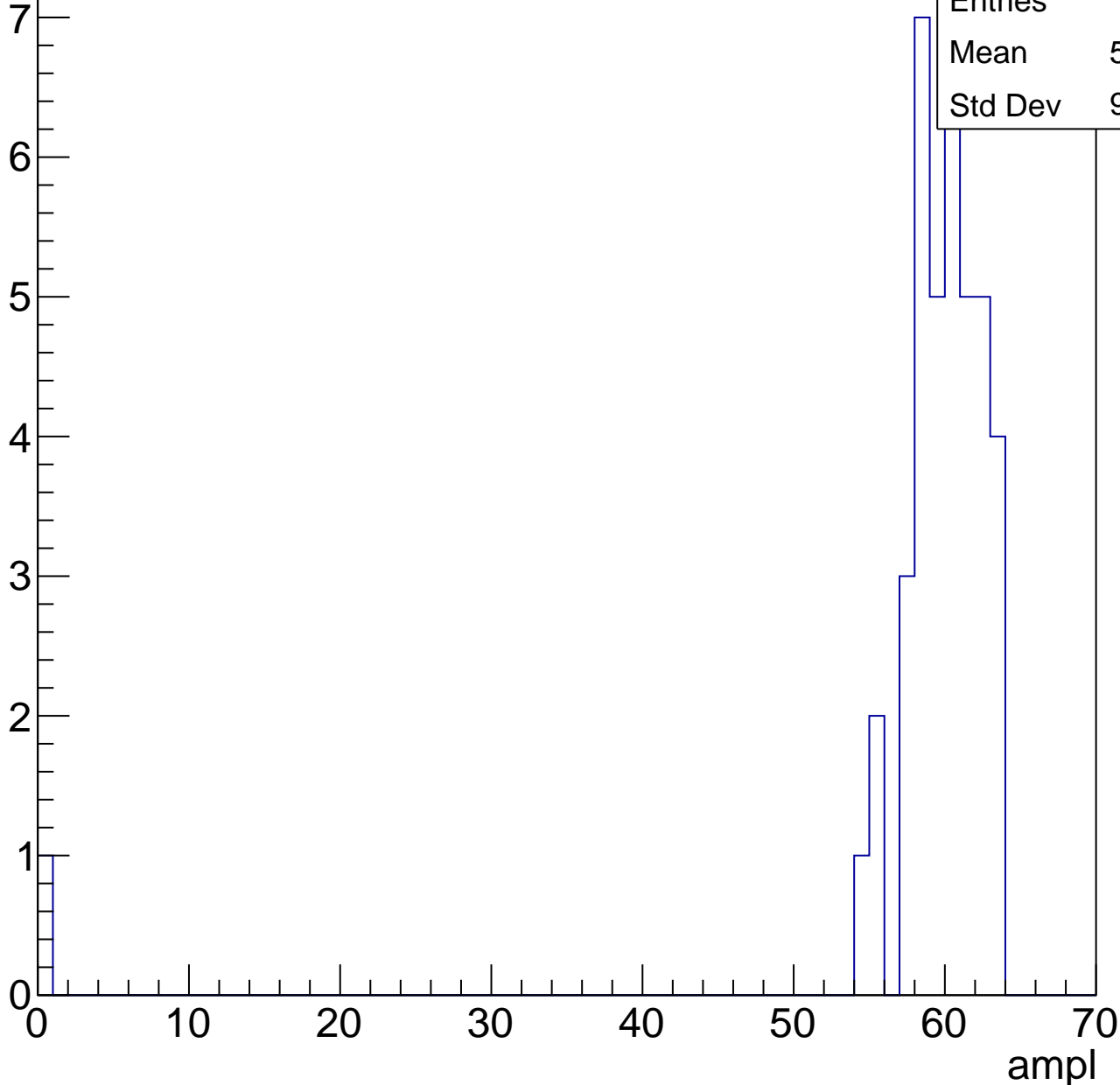


# B1L103S, U16-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	40
Mean	58.08
Std Dev	9.564

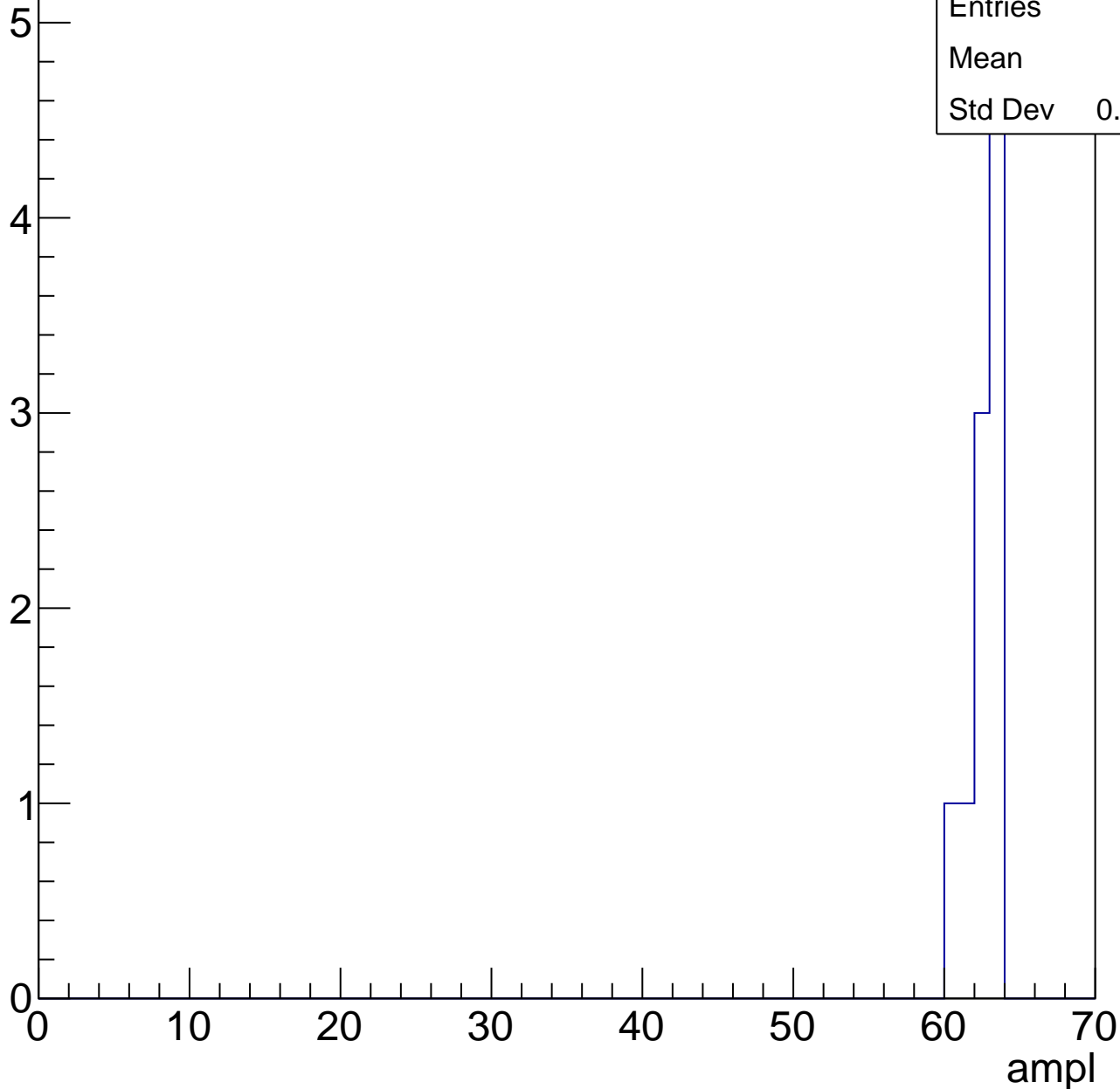


# B1L103S, U16-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	10
Mean	62.2
Std Dev	0.9798





# B1L103S, U16-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch72, adc0

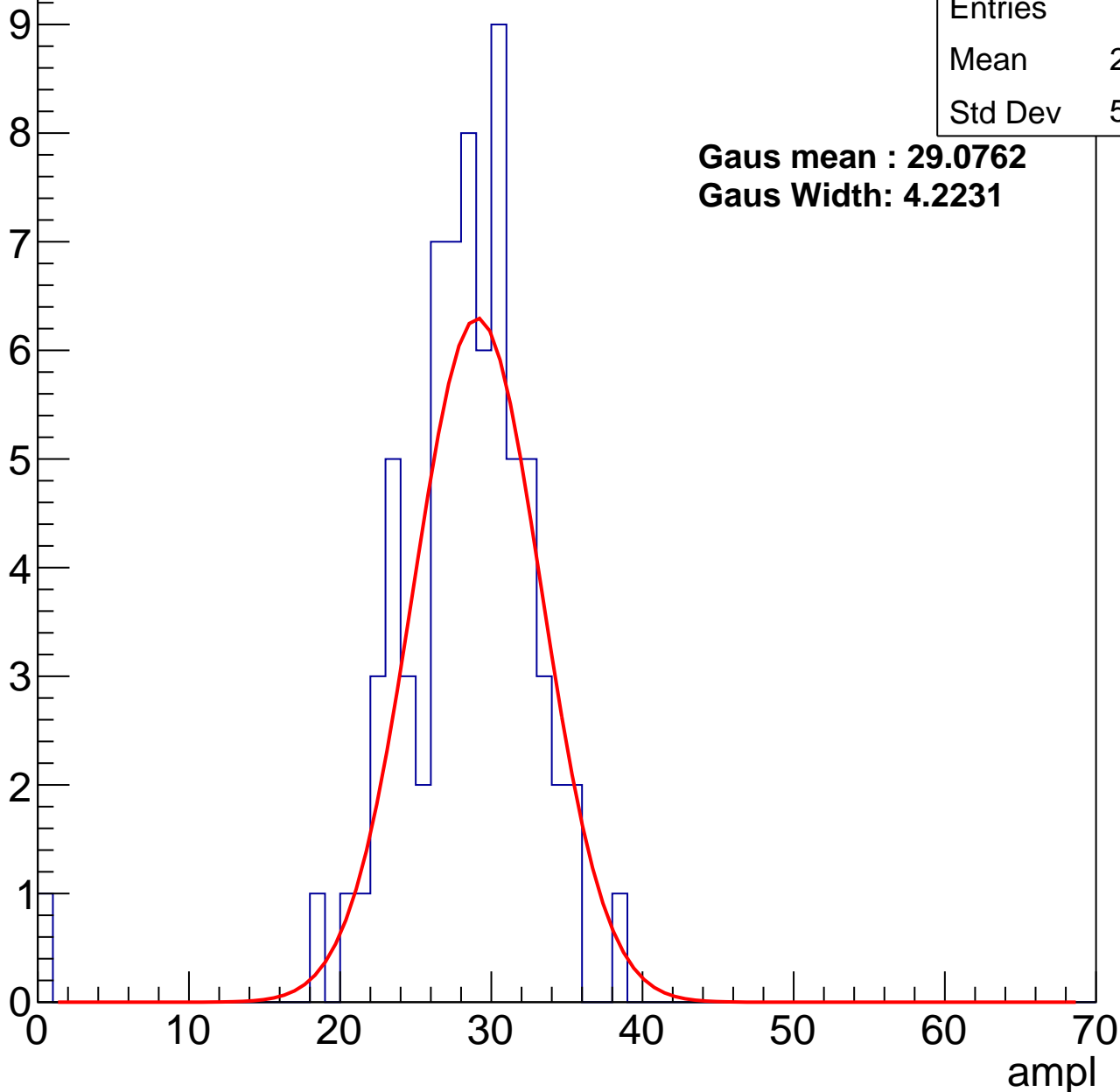
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	27.65
Std Dev	5.047

**Gaus mean : 29.0762**

**Gaus Width: 4.2231**



# B1L103S, U16-ch72, adc1

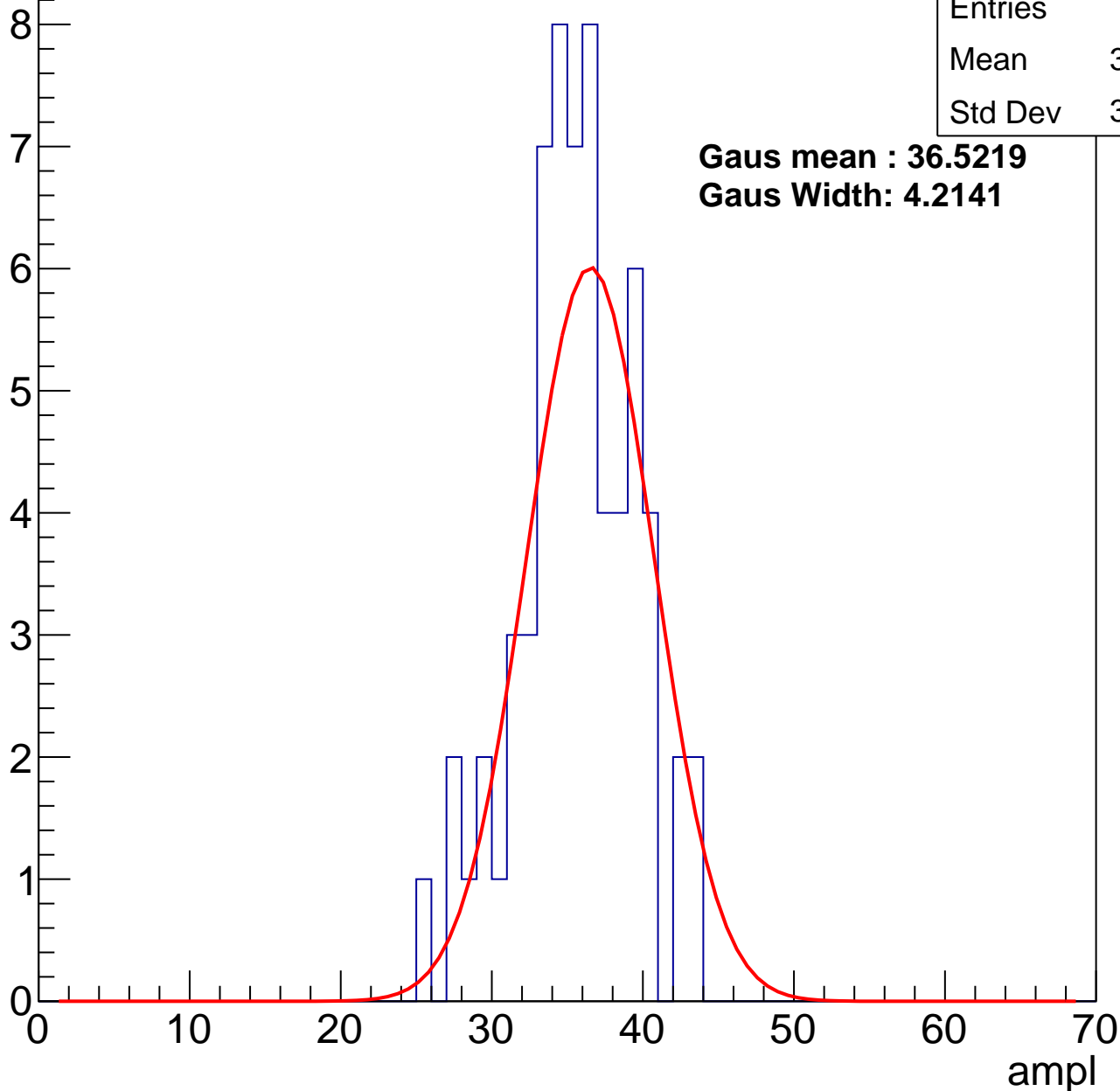
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	35.14
Std Dev	3.855

**Gaus mean : 36.5219**

**Gaus Width: 4.2141**



# B1L103S, U16-ch72, adc2

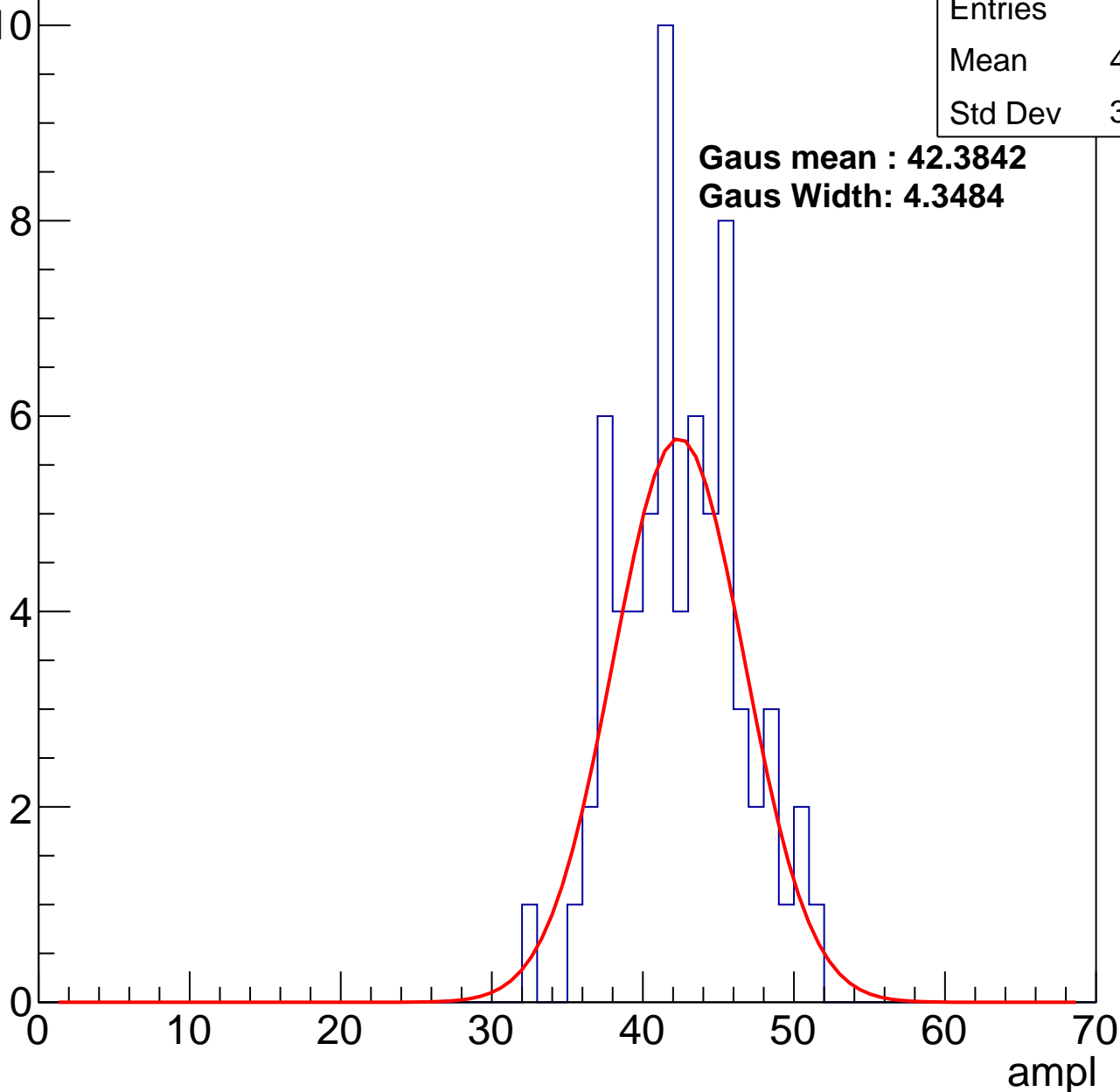
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	42.07
Std Dev	3.953

**Gaus mean : 42.3842**

**Gaus Width: 4.3484**

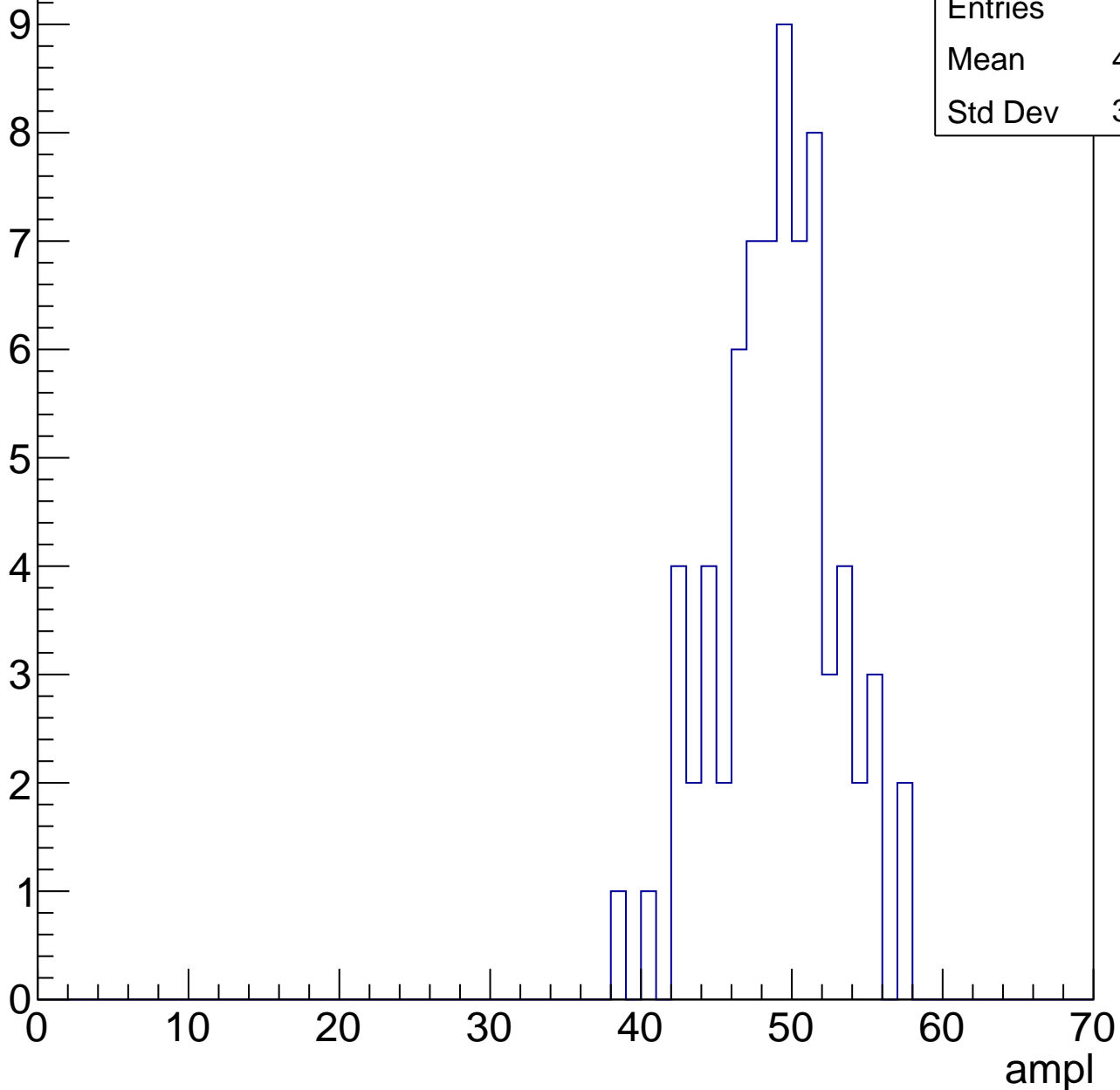


# B1L103S, U16-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	48.51
Std Dev	3.891

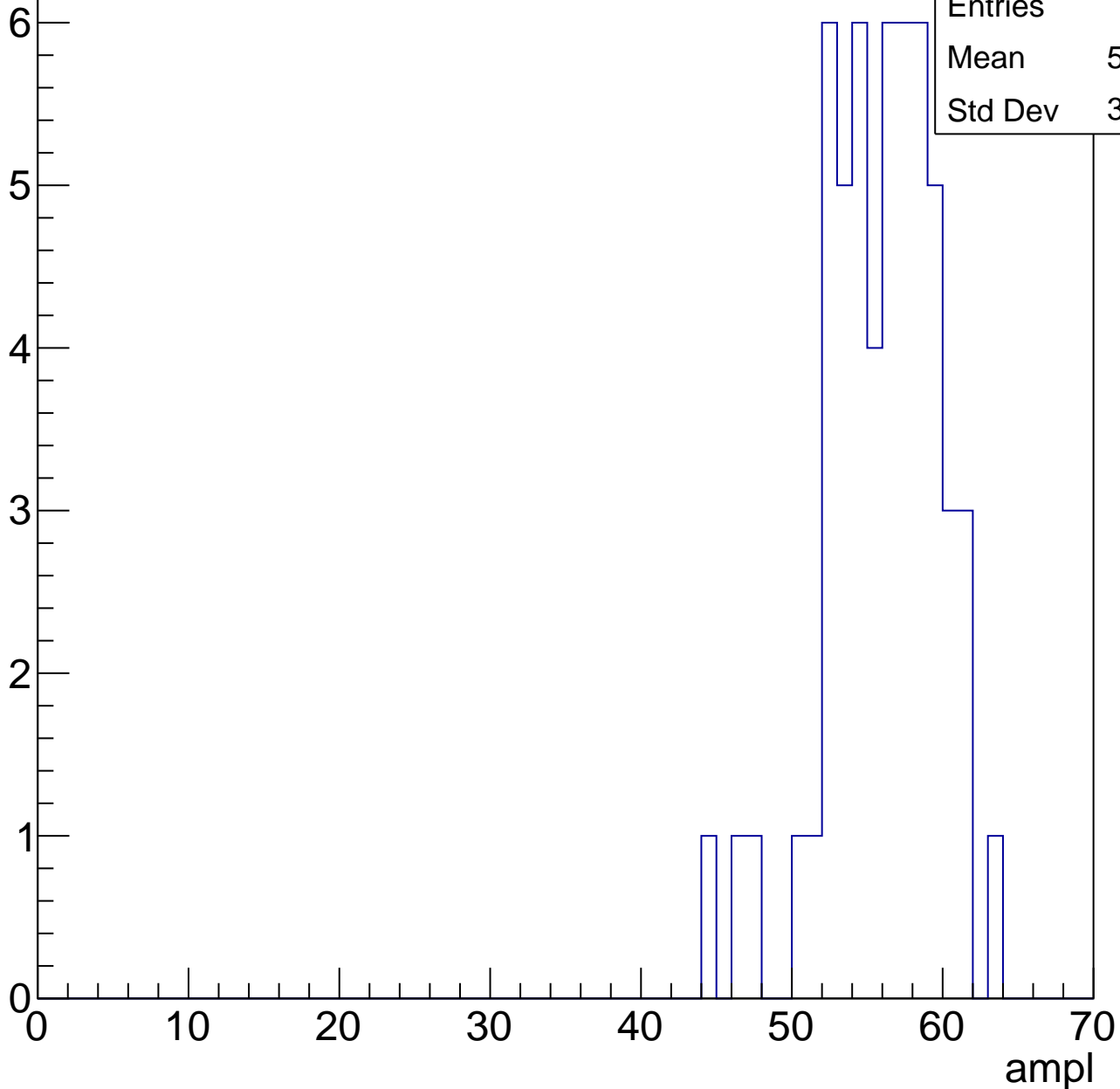


# B1L103S, U16-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	55.46
Std Dev	3.746

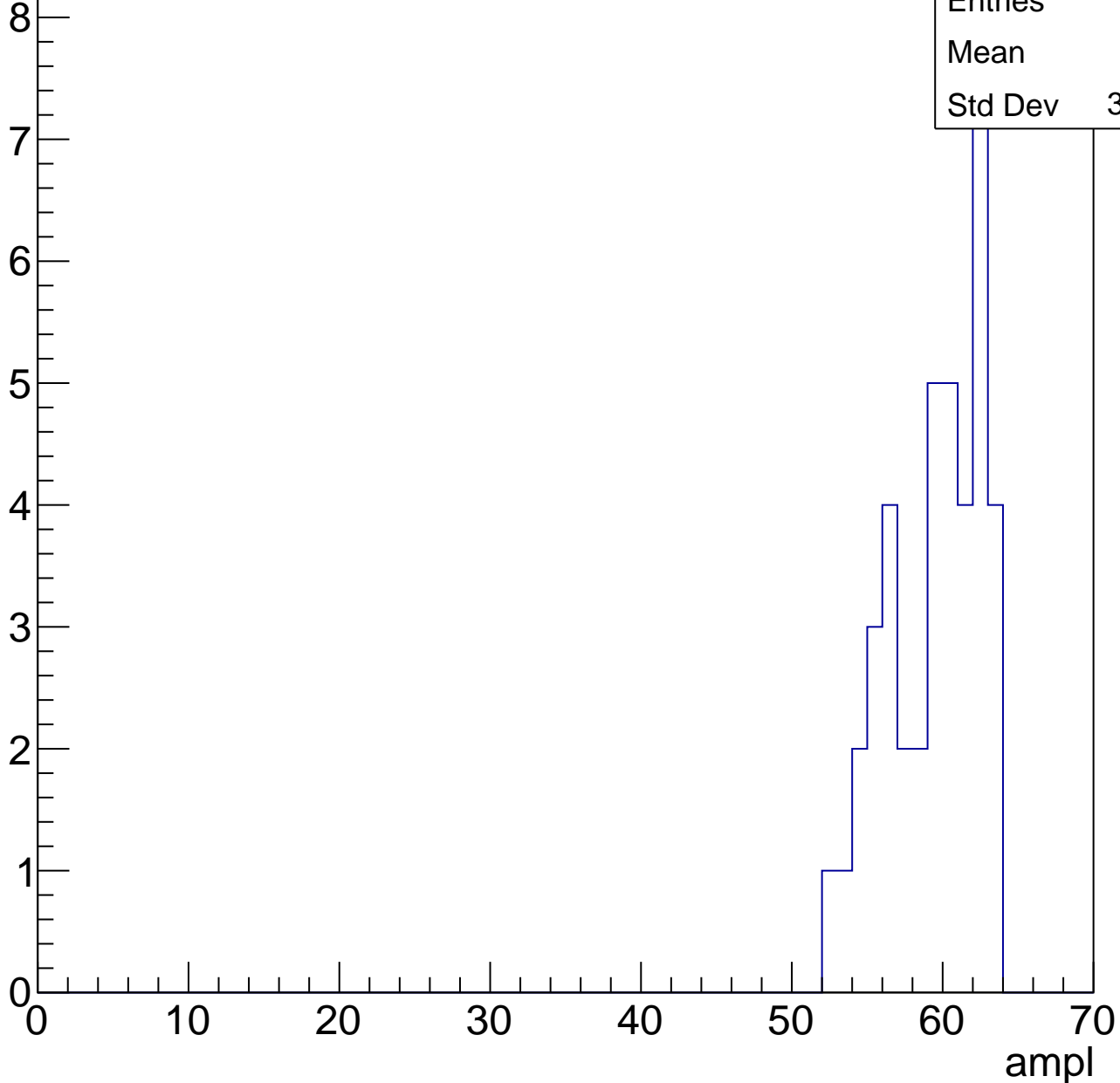


# B1L103S, U16-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	41
Mean	59
Std Dev	3.068

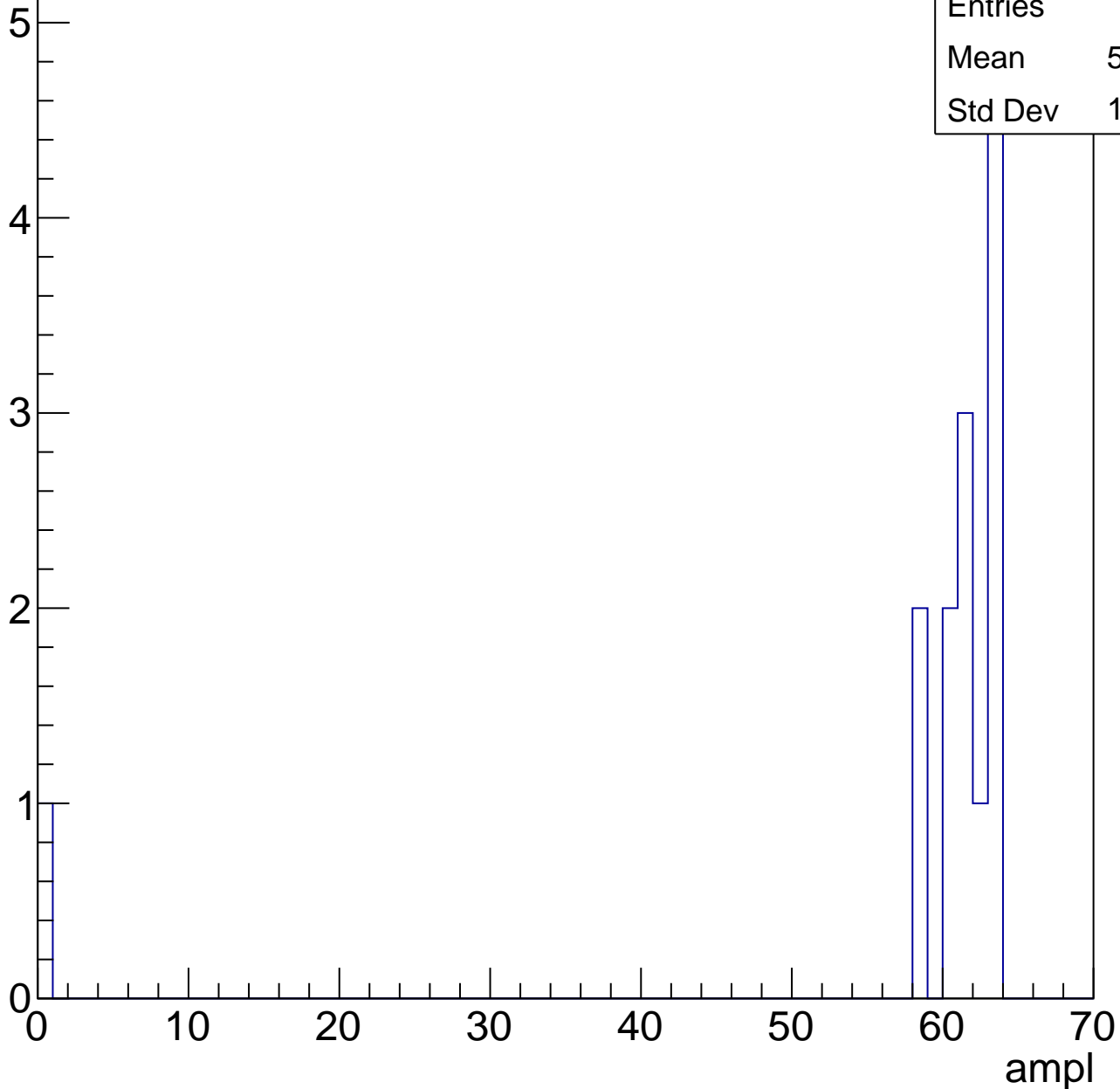


# B1L103S, U16-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	14
Mean	56.86
Std Dev	15.86





# B1L103S, U16-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch73, adc0

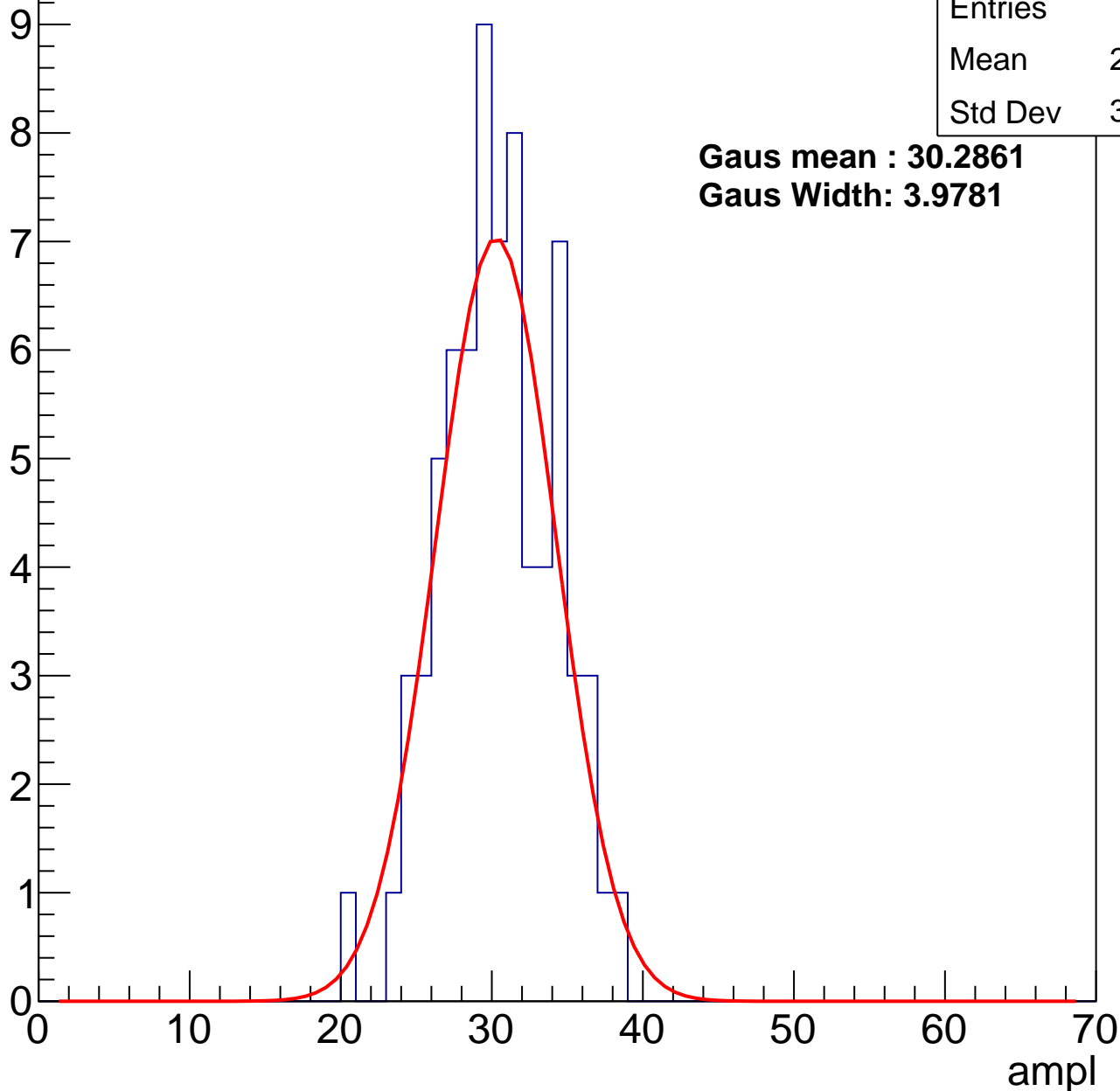
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	29.93
Std Dev	3.664

**Gaus mean : 30.2861**

**Gaus Width: 3.9781**



# B1L103S, U16-ch73, adc1

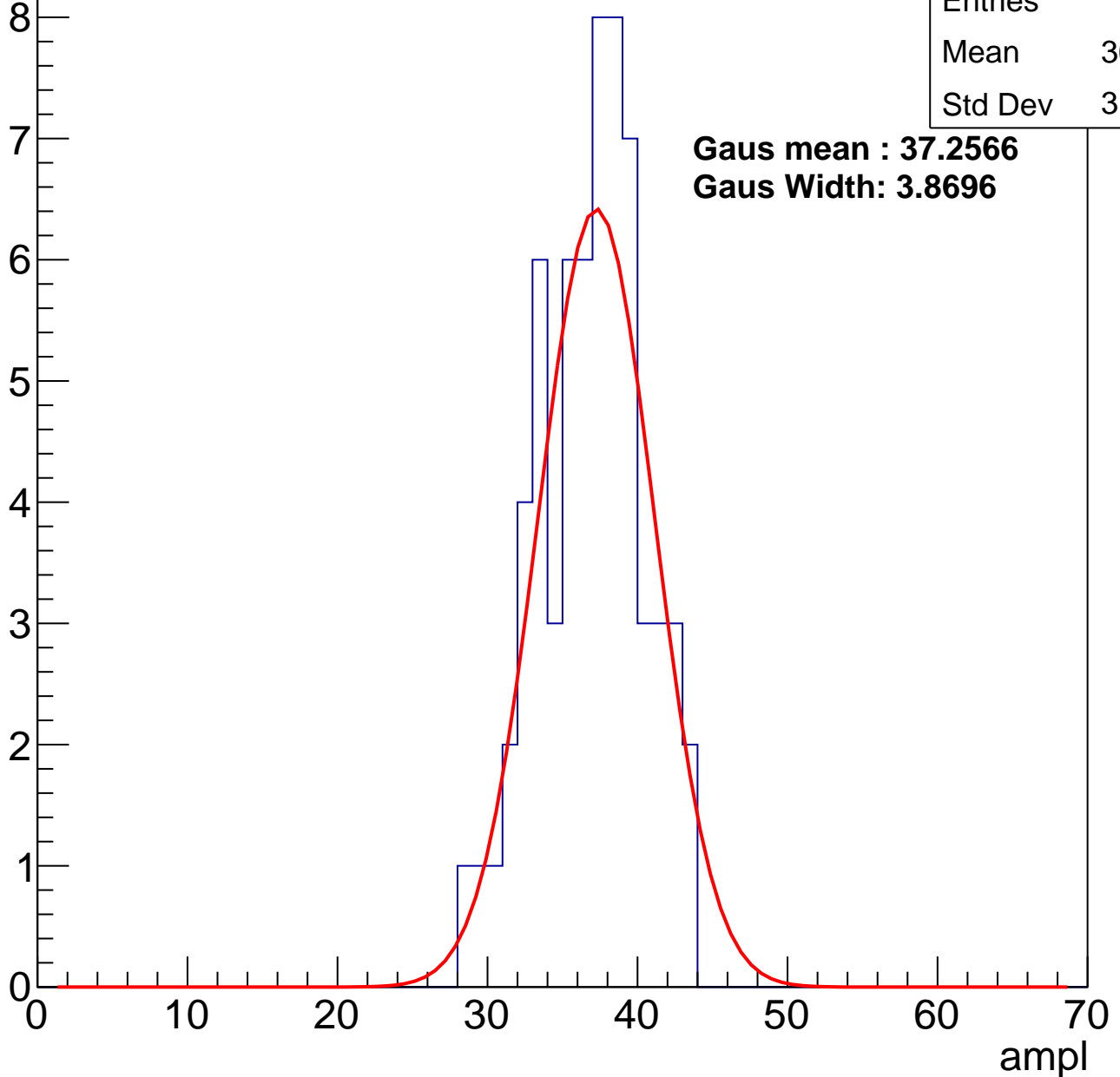
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	36.42
Std Dev	3.436

**Gaus mean : 37.2566**

**Gaus Width: 3.8696**

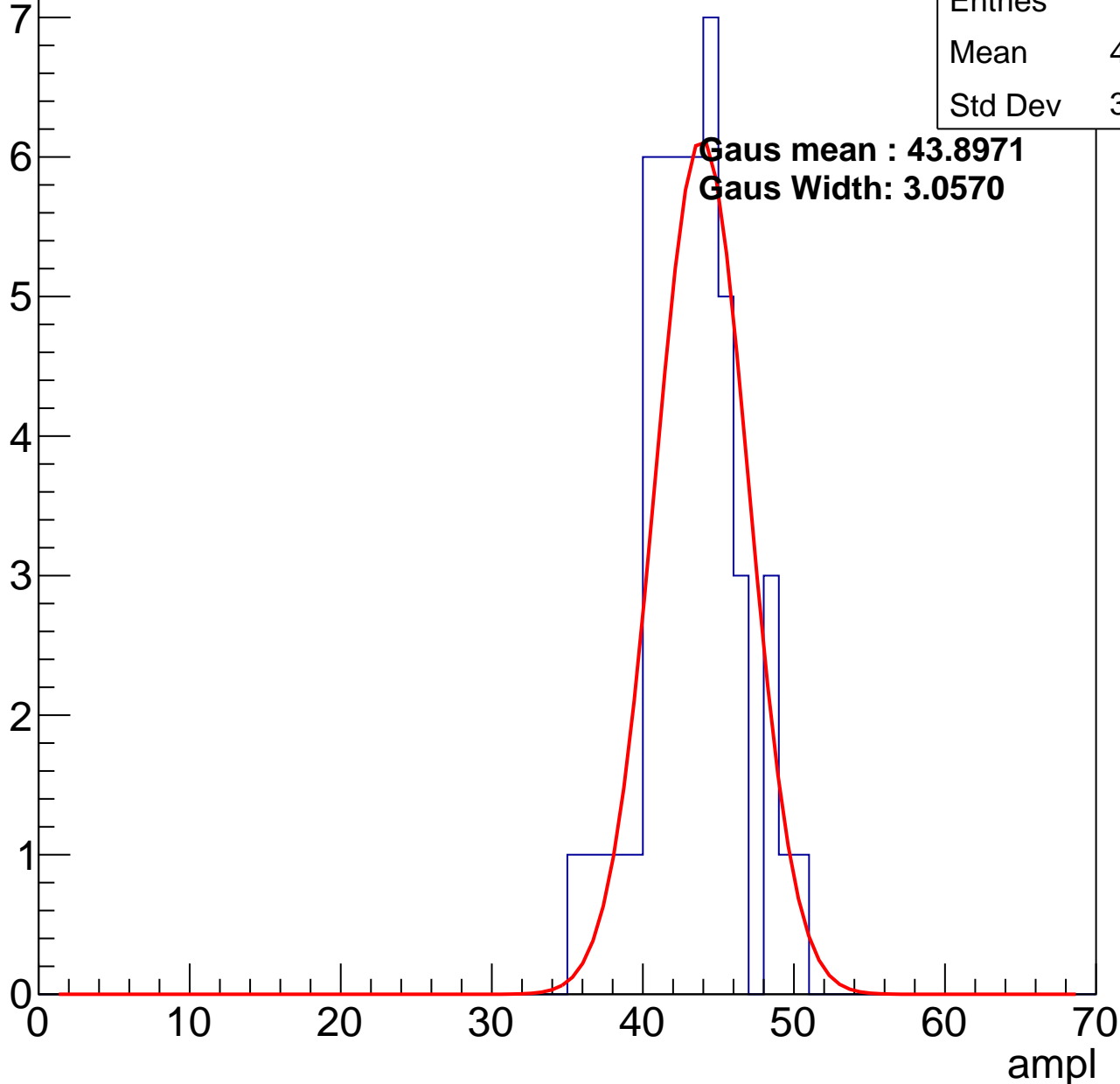


# B1L103S, U16-ch73, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	42.76
Std Dev	3.146

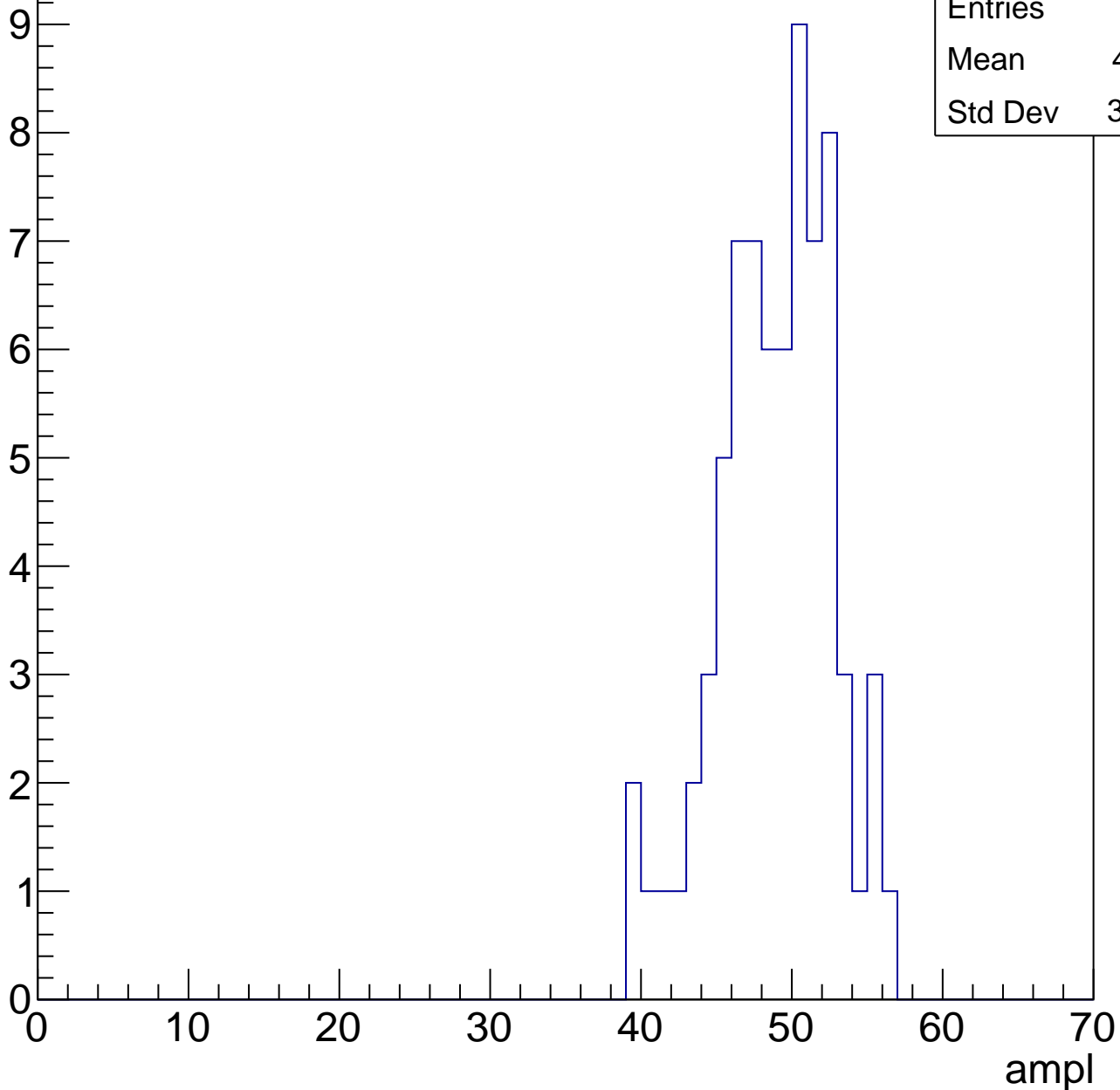


# B1L103S, U16-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	48.41
Std Dev	3.759

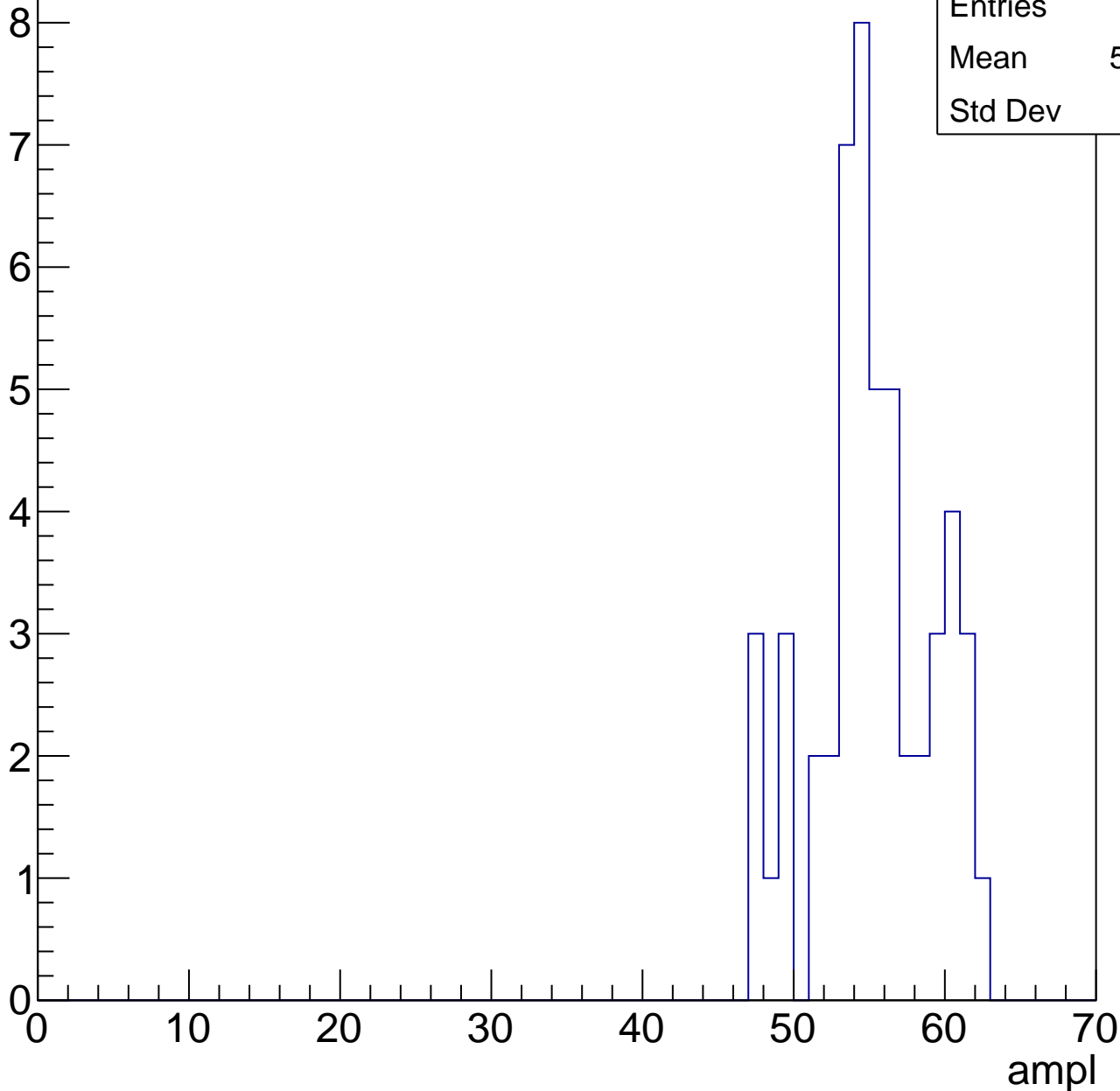


# B1L103S, U16-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	54.75
Std Dev	3.88

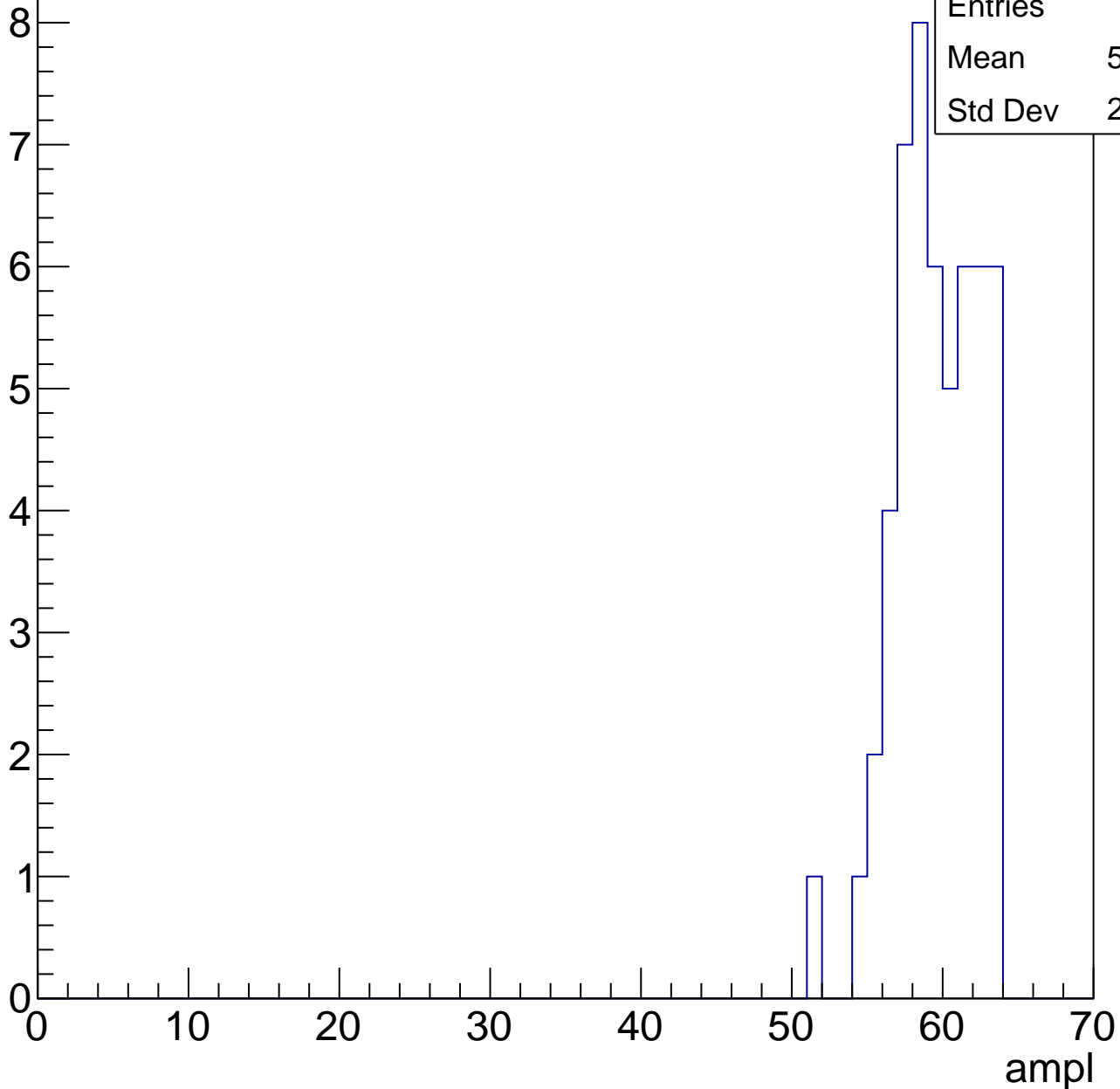


# B1L103S, U16-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

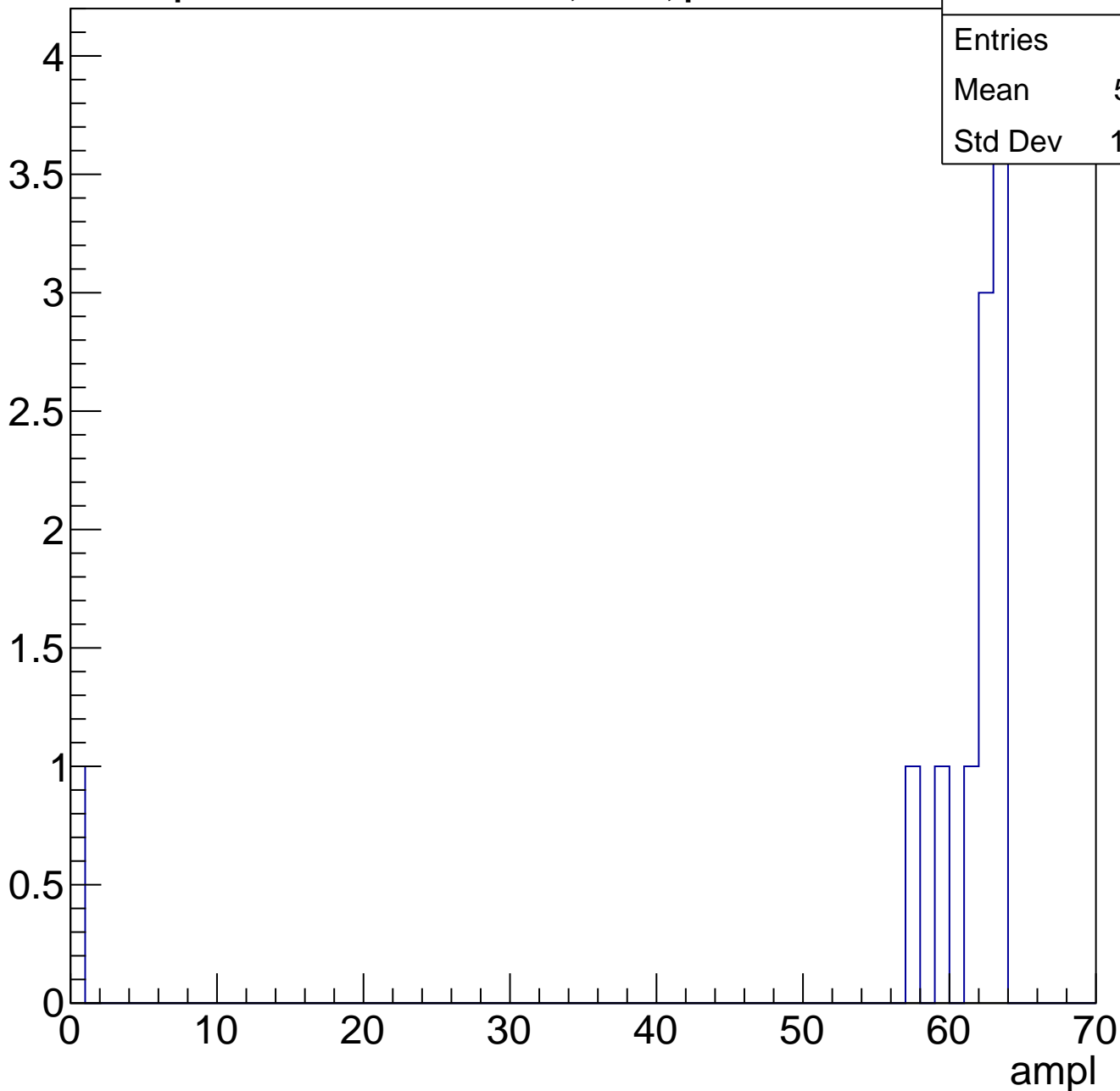
Entries	52
Mean	59.08
Std Dev	2.674



# B1L103S, U16-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



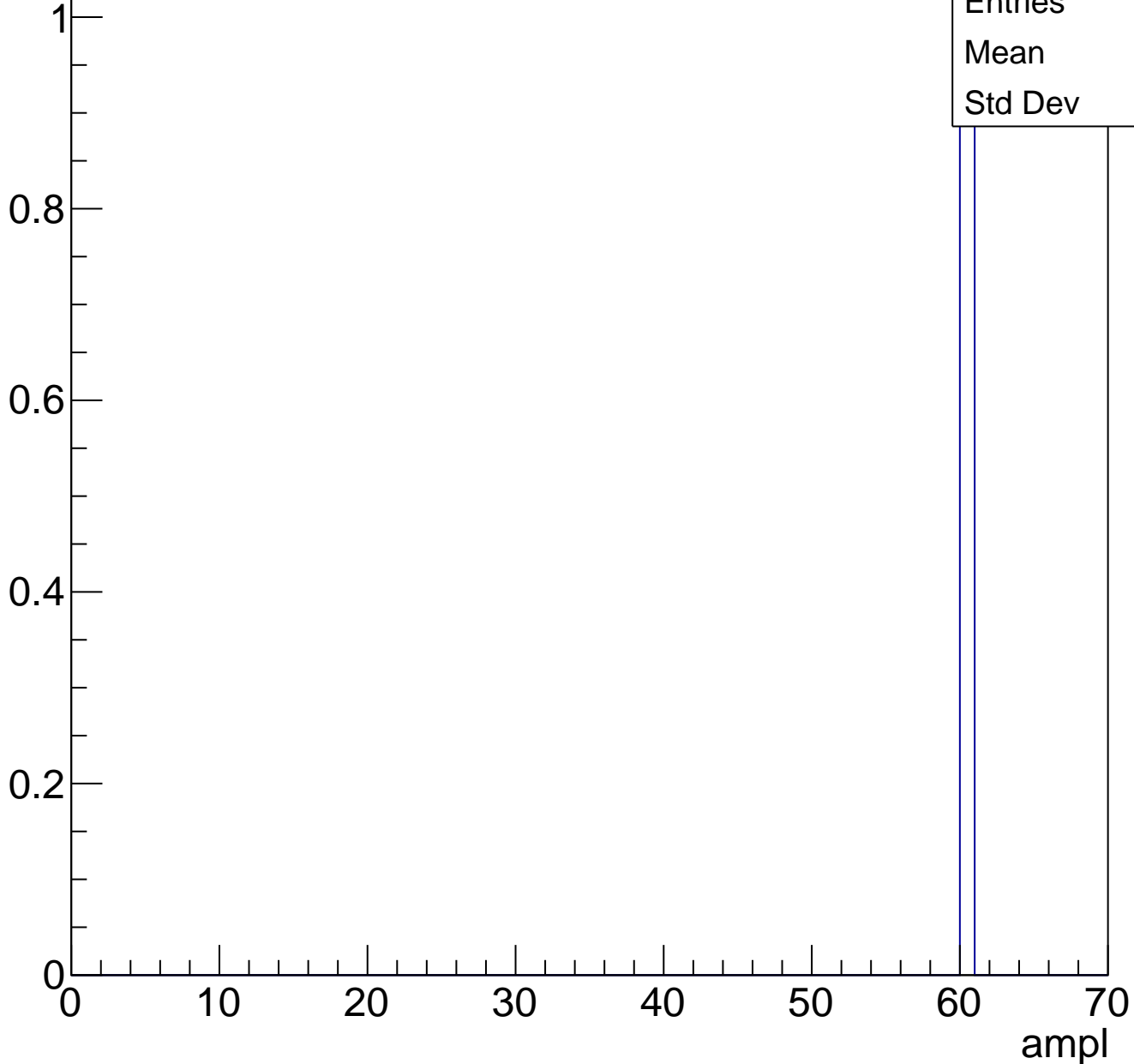
Entries	11
Mean	55.91
Std Dev	17.77



# B1L103S, U16-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch74, adc0

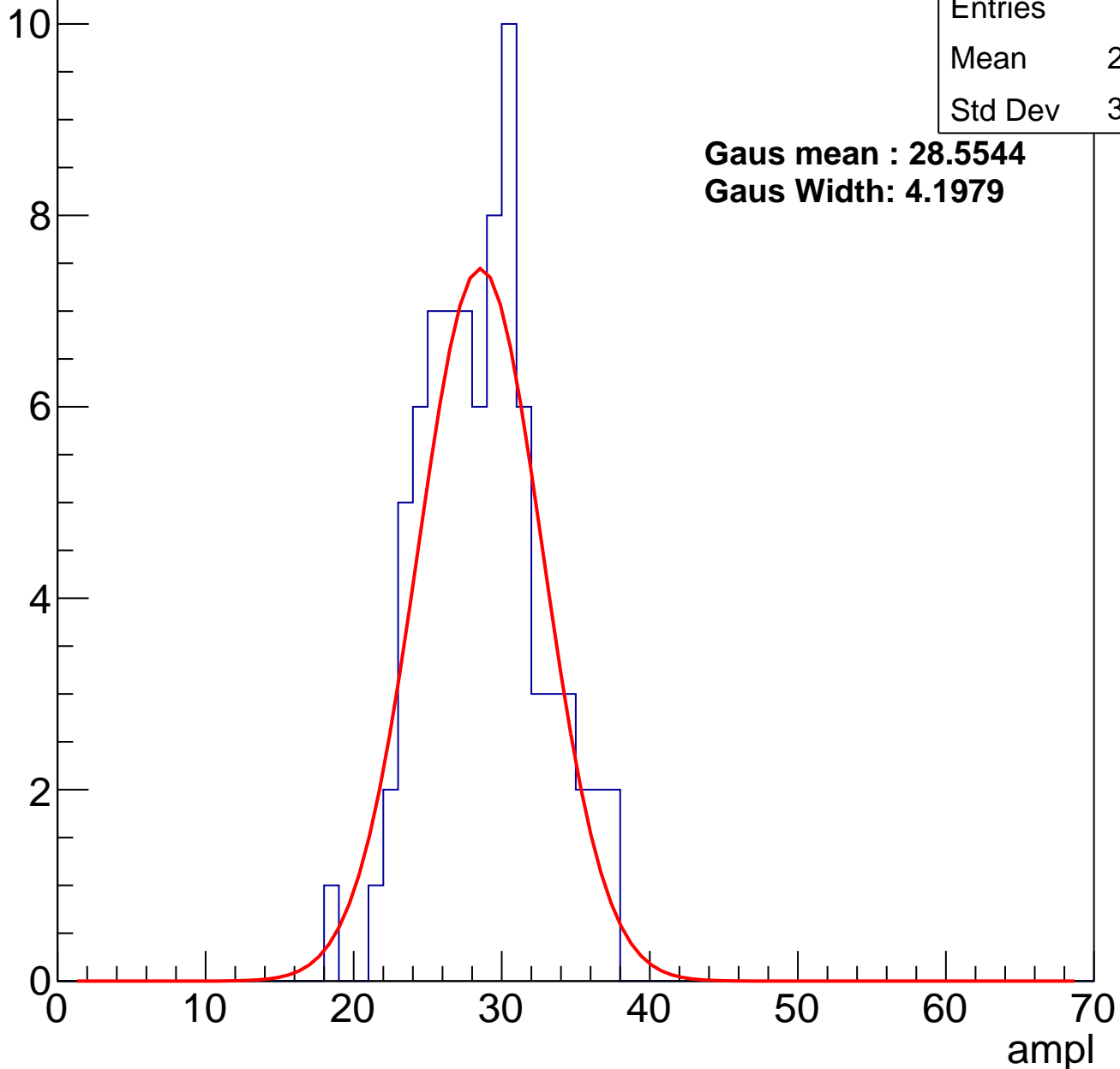
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	81
Mean	28.23
Std Dev	3.939

**Gaus mean : 28.5544**

**Gaus Width: 4.1979**

Entry



# B1L103S, U16-ch74, adc1

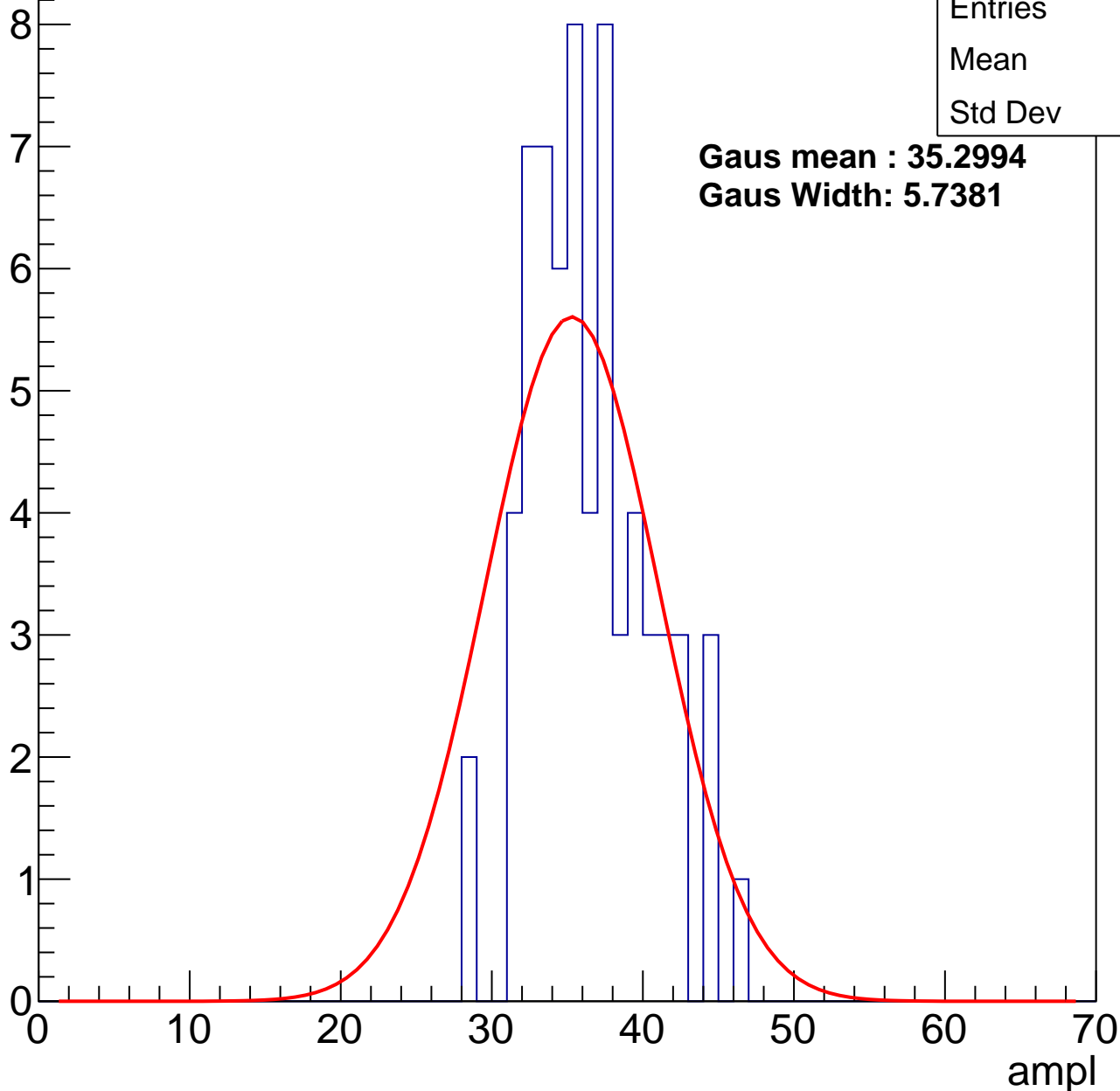
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	36
Std Dev	3.92

**Gaus mean : 35.2994**

**Gaus Width: 5.7381**

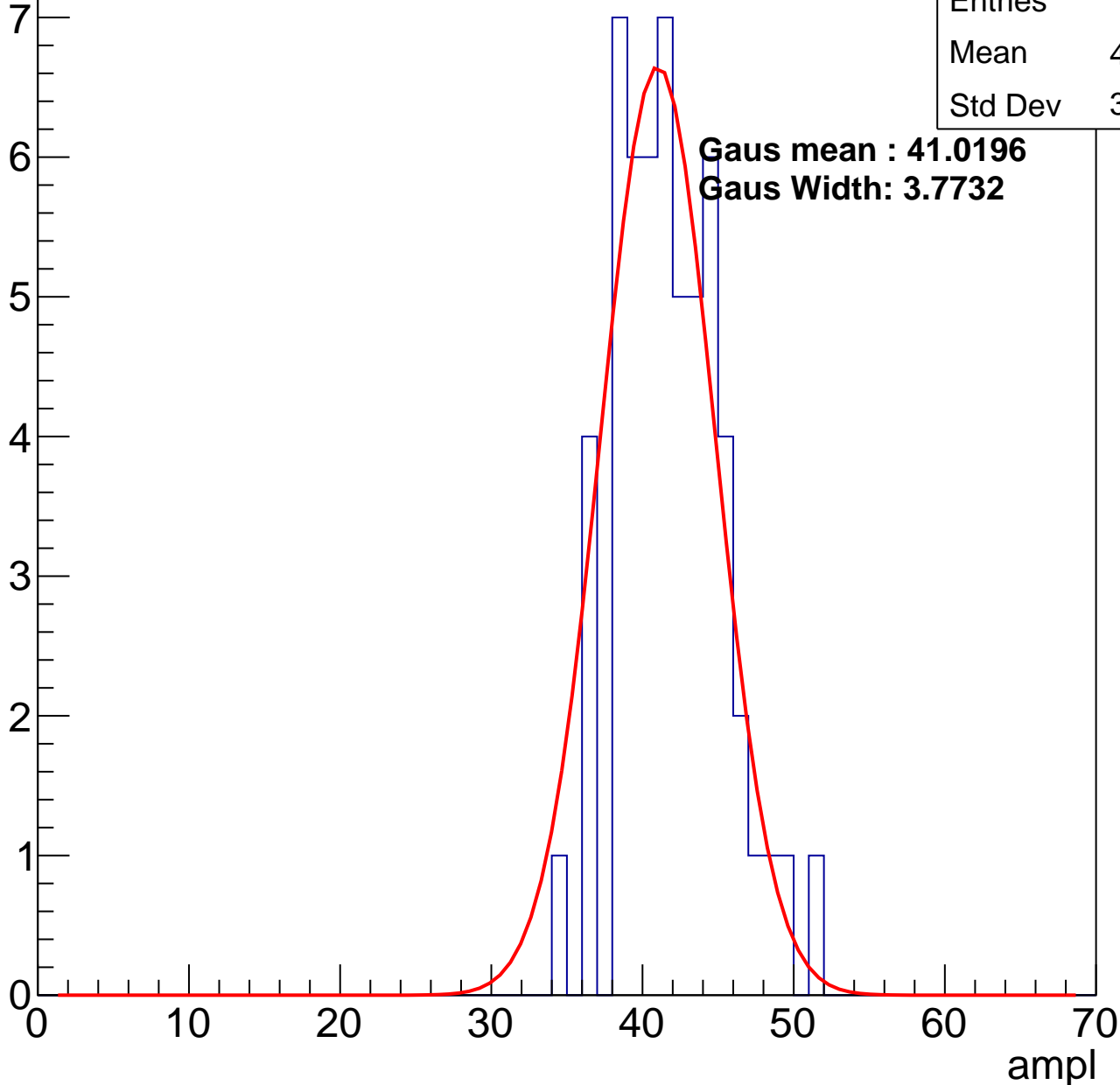


# B1L103S, U16-ch74, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	41.42
Std Dev	3.438

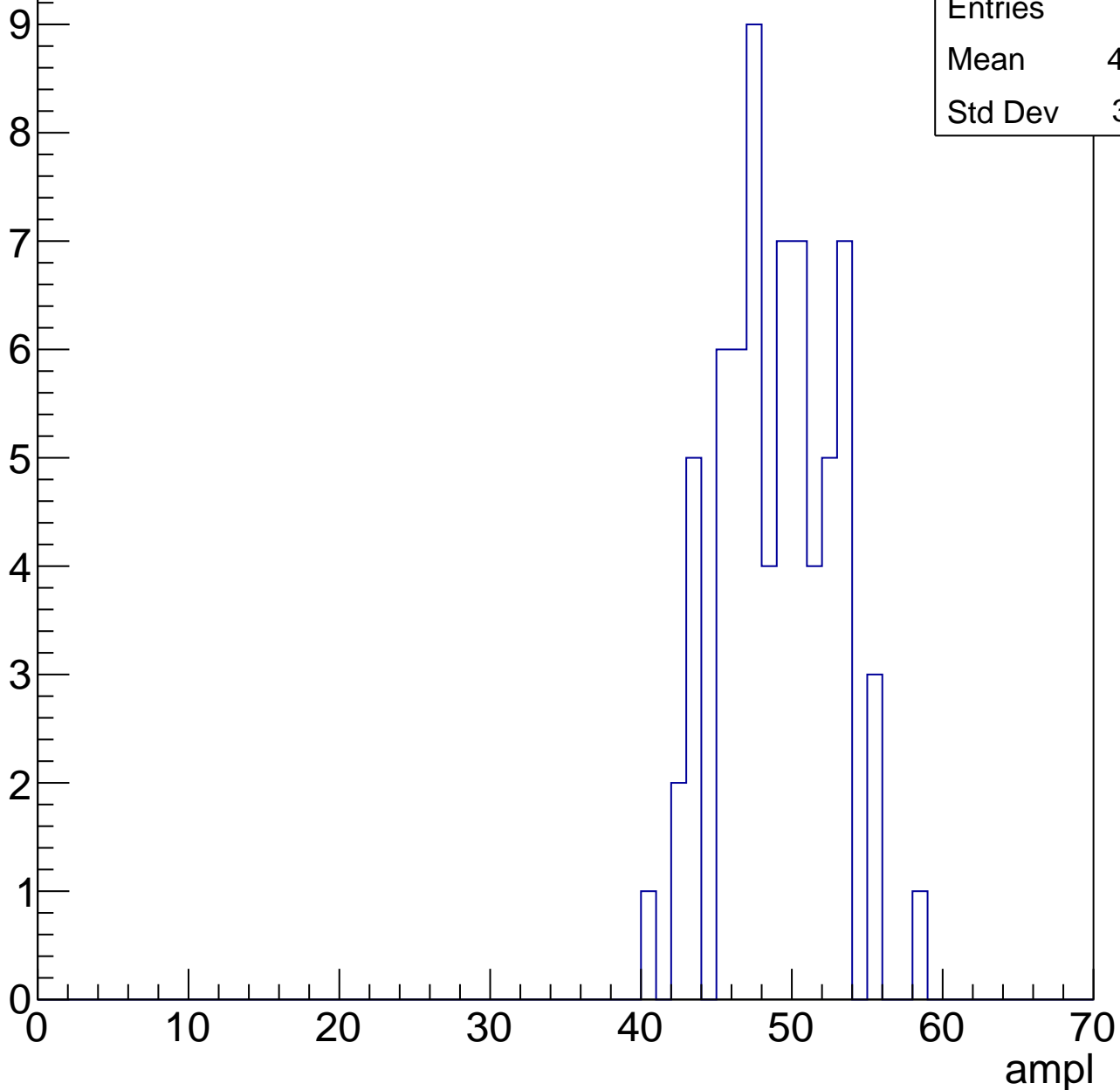


# B1L103S, U16-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	48.52
Std Dev	3.671

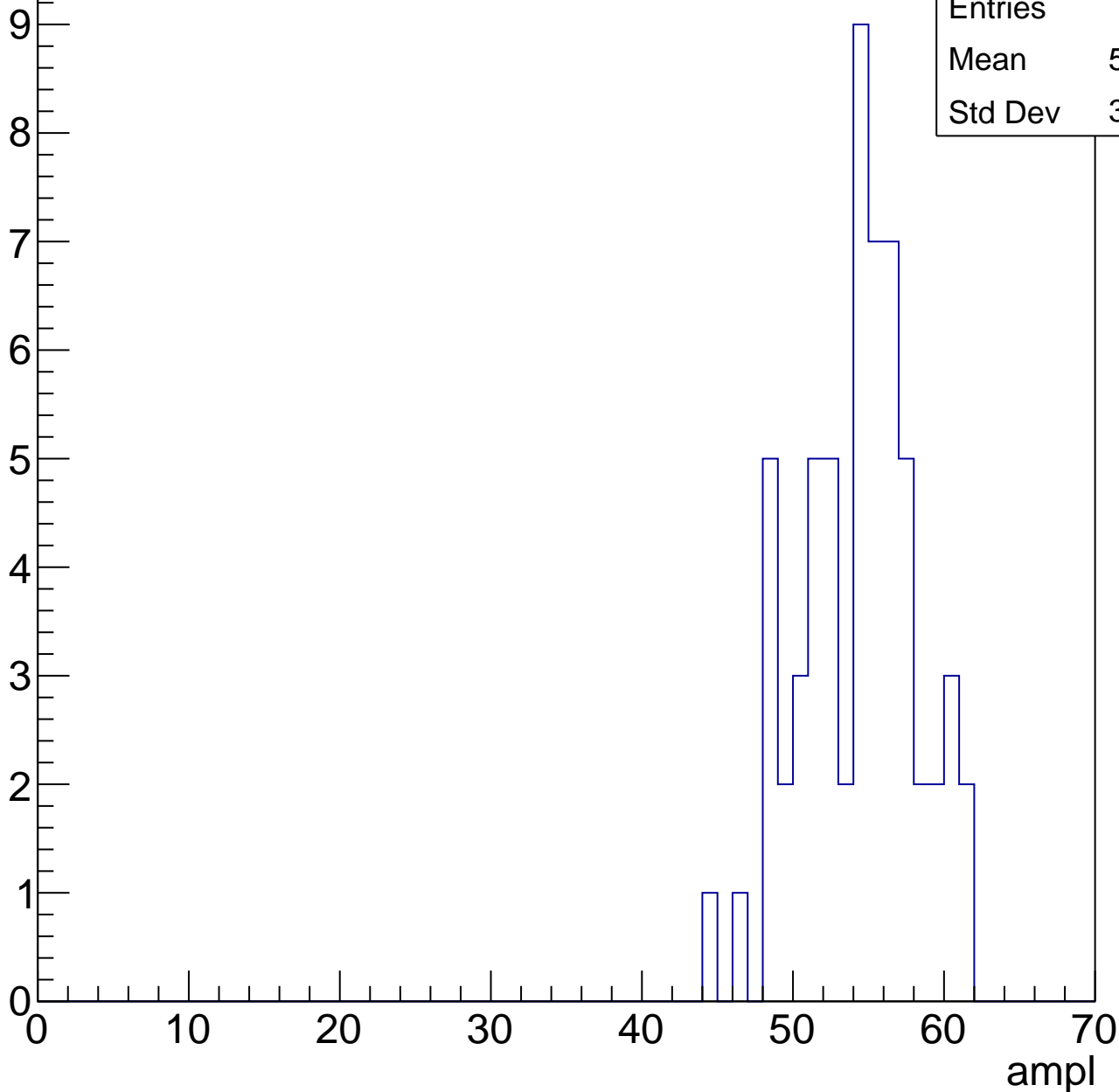


# B1L103S, U16-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	53.82
Std Dev	3.787



# B1L103S, U16-ch74, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

7

6

5

4

3

2

1

0

Entries

44

Mean

57.91

Std Dev

9.155

0

0

10

20

30

40

50

60

ampl

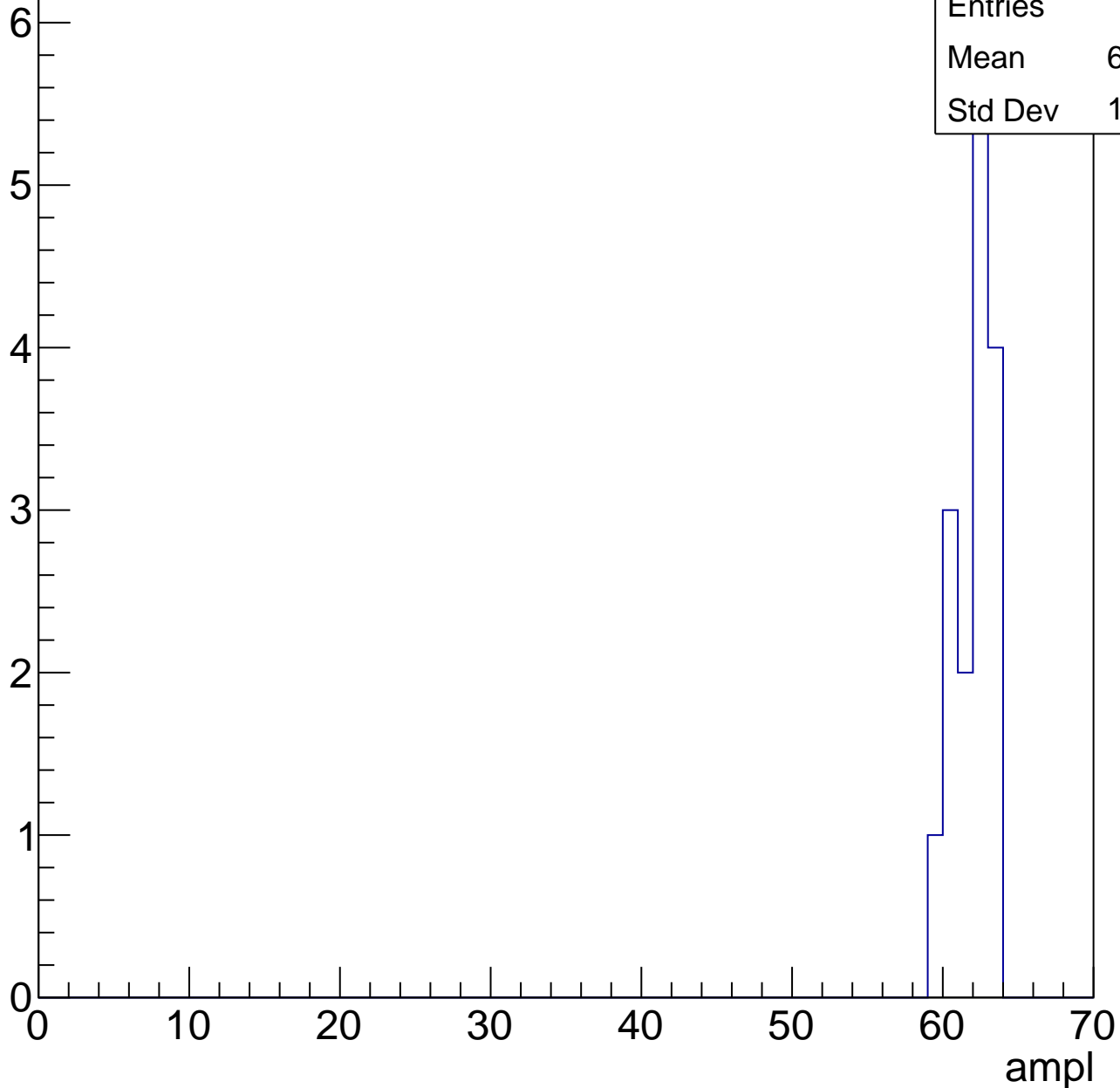
70

# B1L103S, U16-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	16
Mean	61.56
Std Dev	1.223

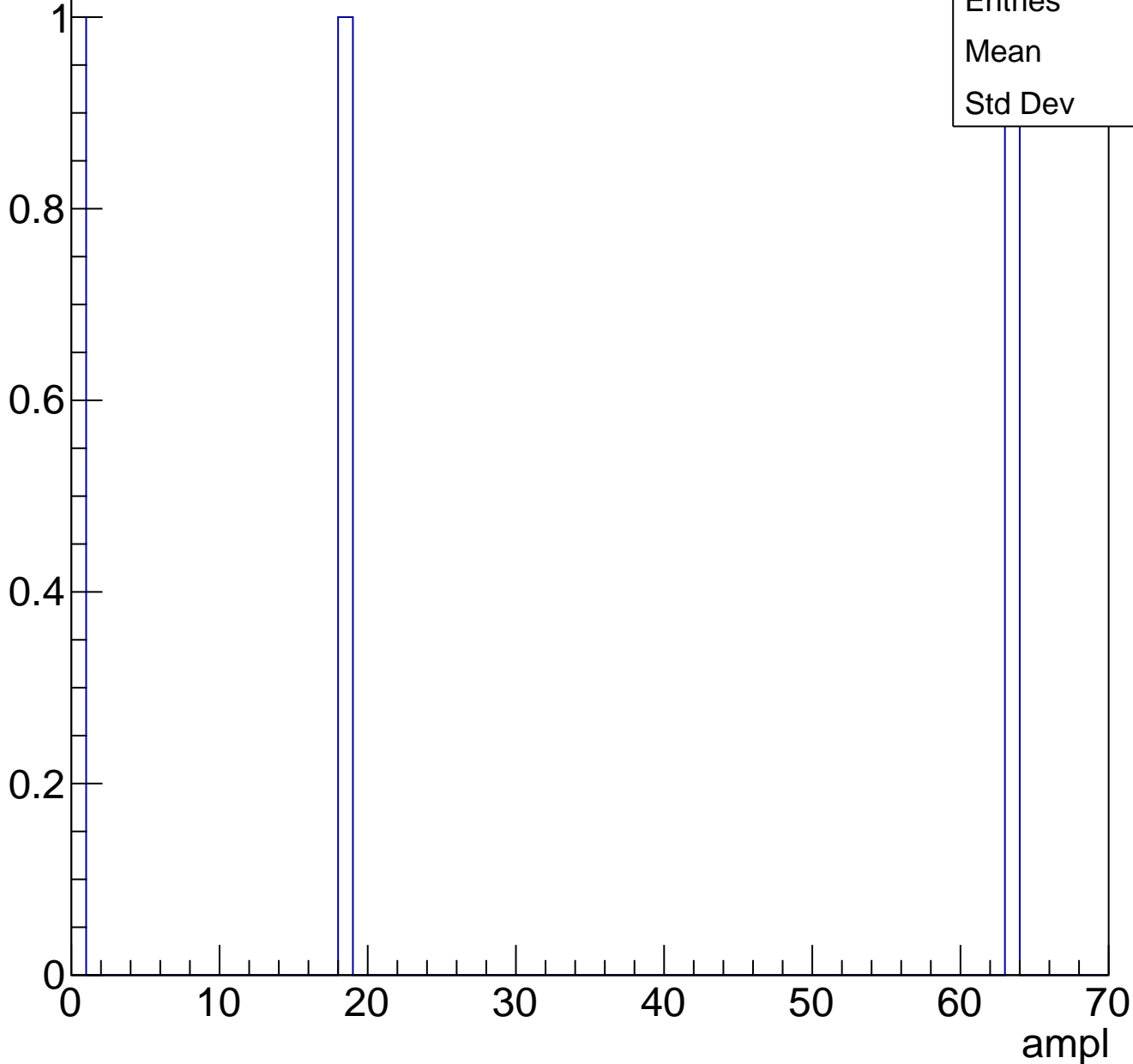




# B1L103S, U16-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch75, adc0

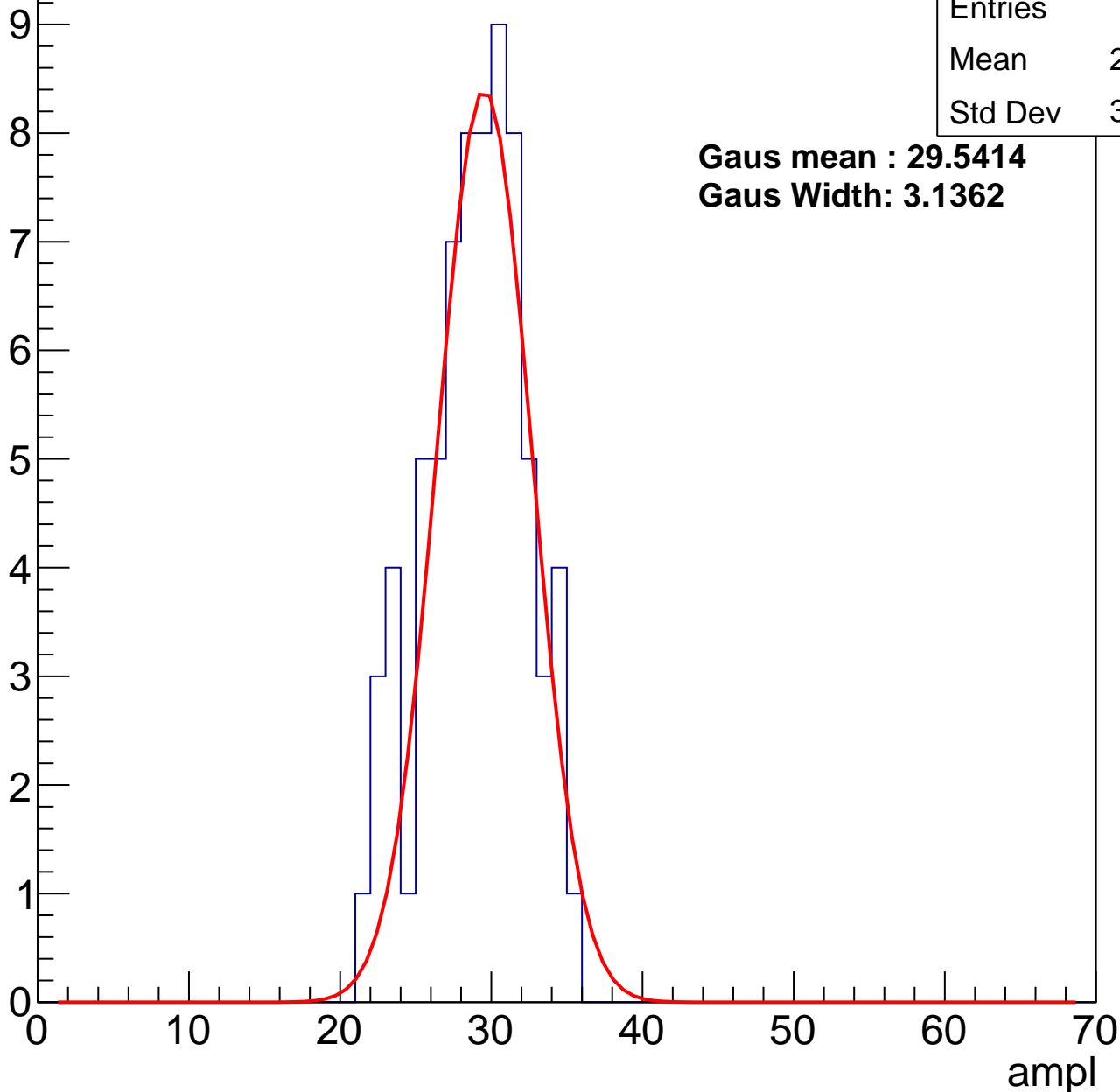
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	28.49
Std Dev	3.317

**Gaus mean : 29.5414**

**Gaus Width: 3.1362**



# B1L103S, U16-ch75, adc1

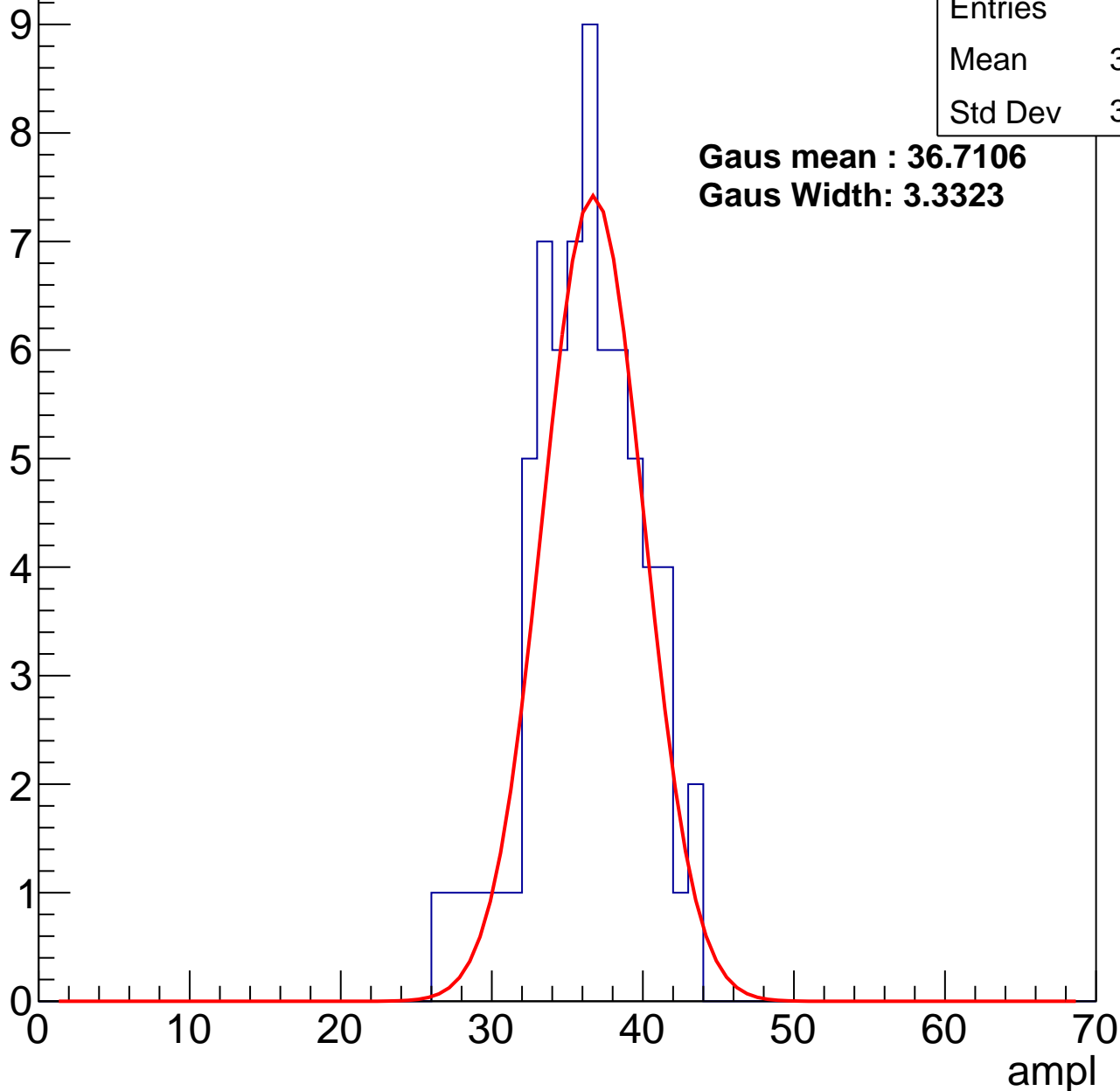
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	35.76
Std Dev	3.634

**Gaus mean : 36.7106**

**Gaus Width: 3.3323**



# B1L103S, U16-ch75, adc2

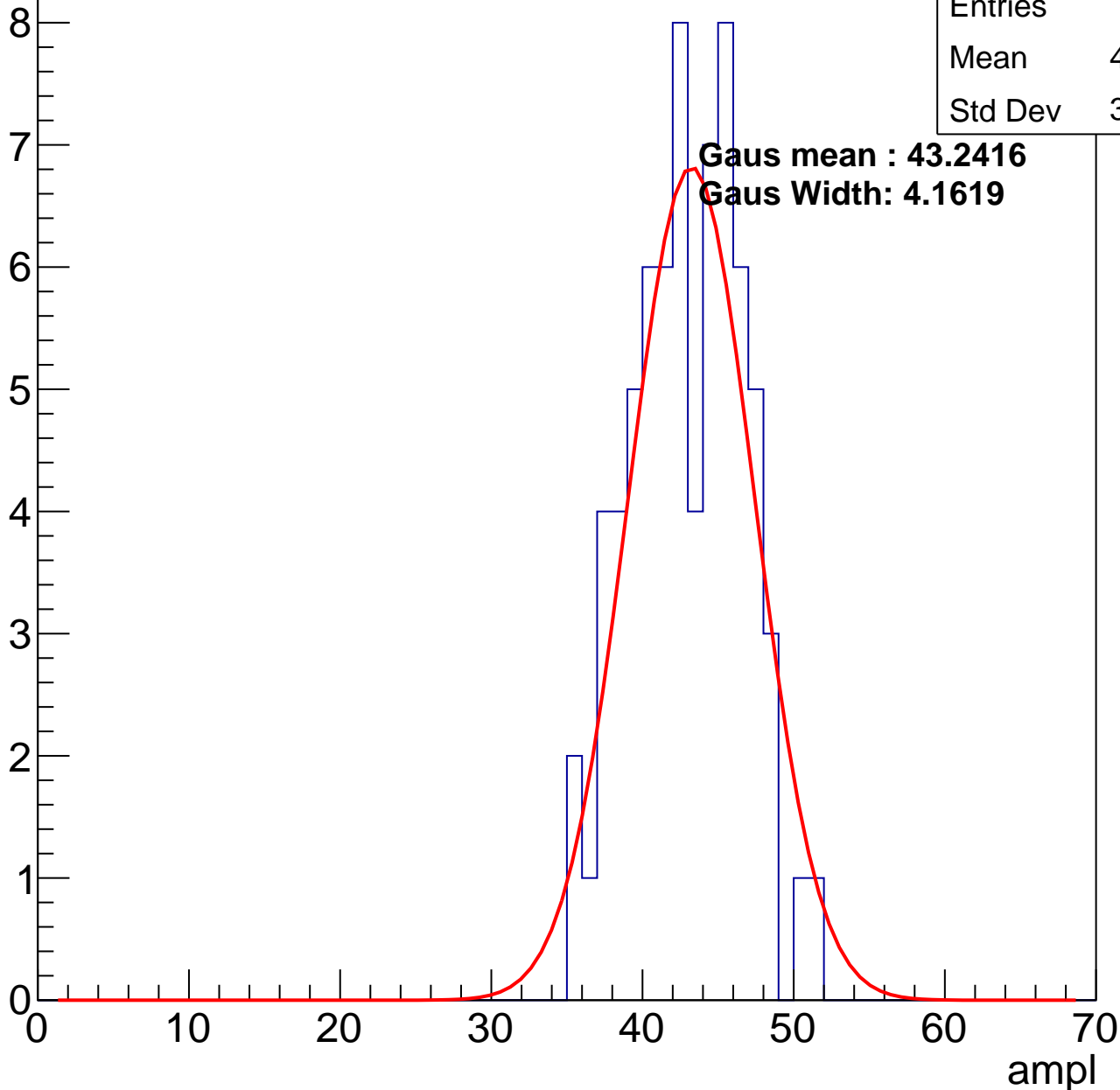
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	42.52
Std Dev	3.623

**Gaus mean : 43.2416**

**Gaus Width: 4.1619**

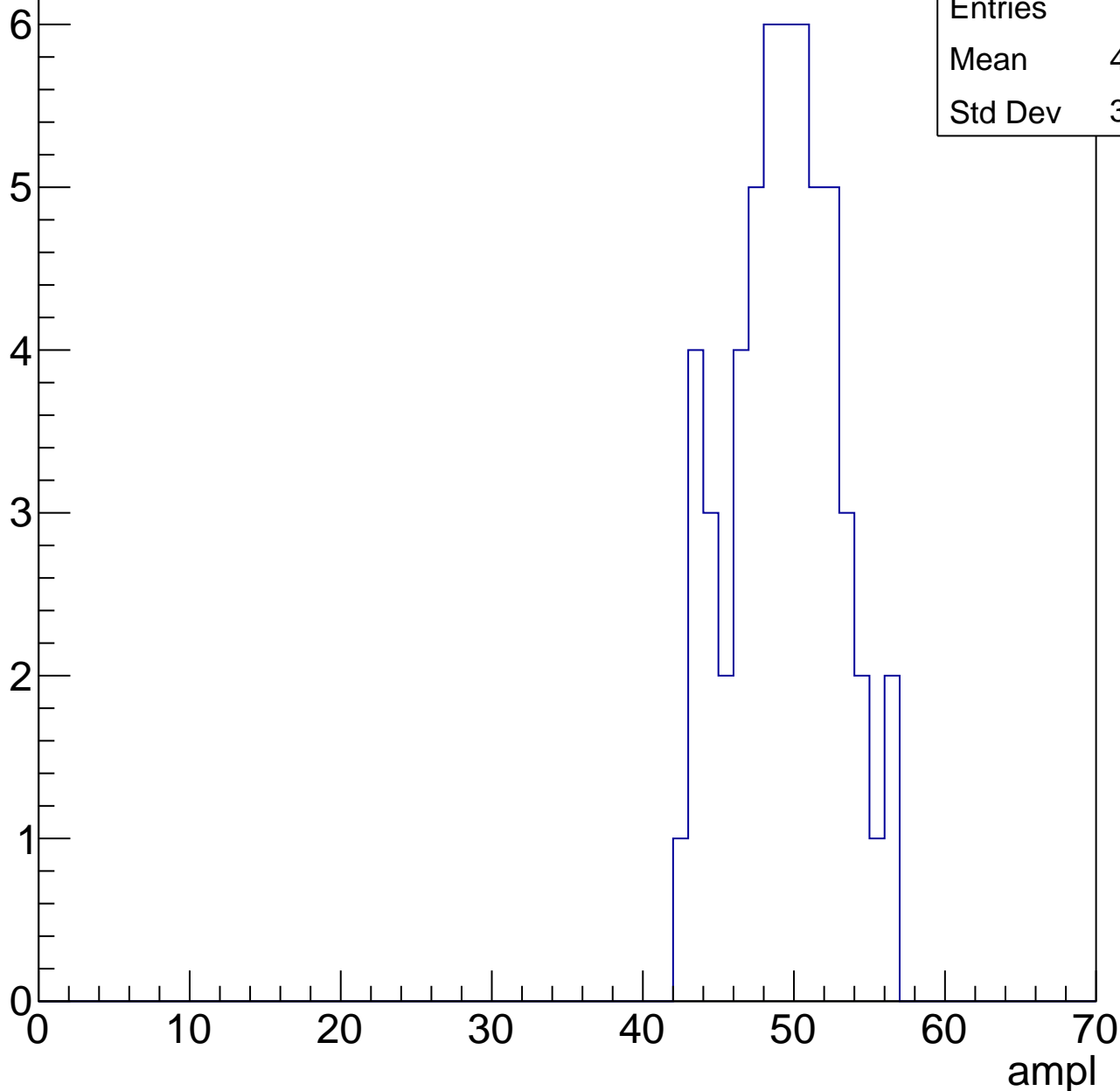


# B1L103S, U16-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	48.84
Std Dev	3.473



# B1L103S, U16-ch75, adc4

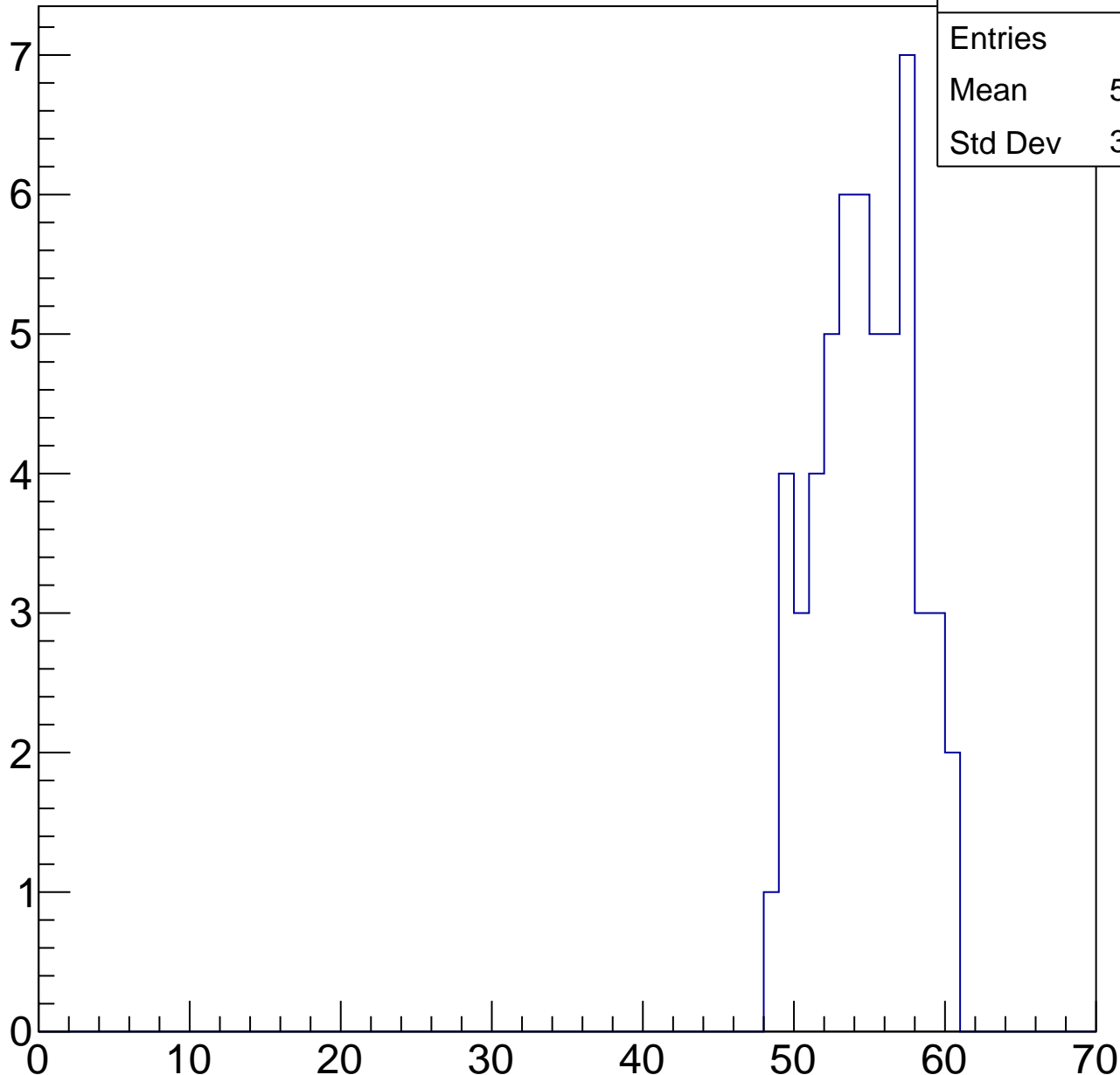
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	54
Mean	54.17
Std Dev	3.125

ampl



# B1L103S, U16-ch75, adc5

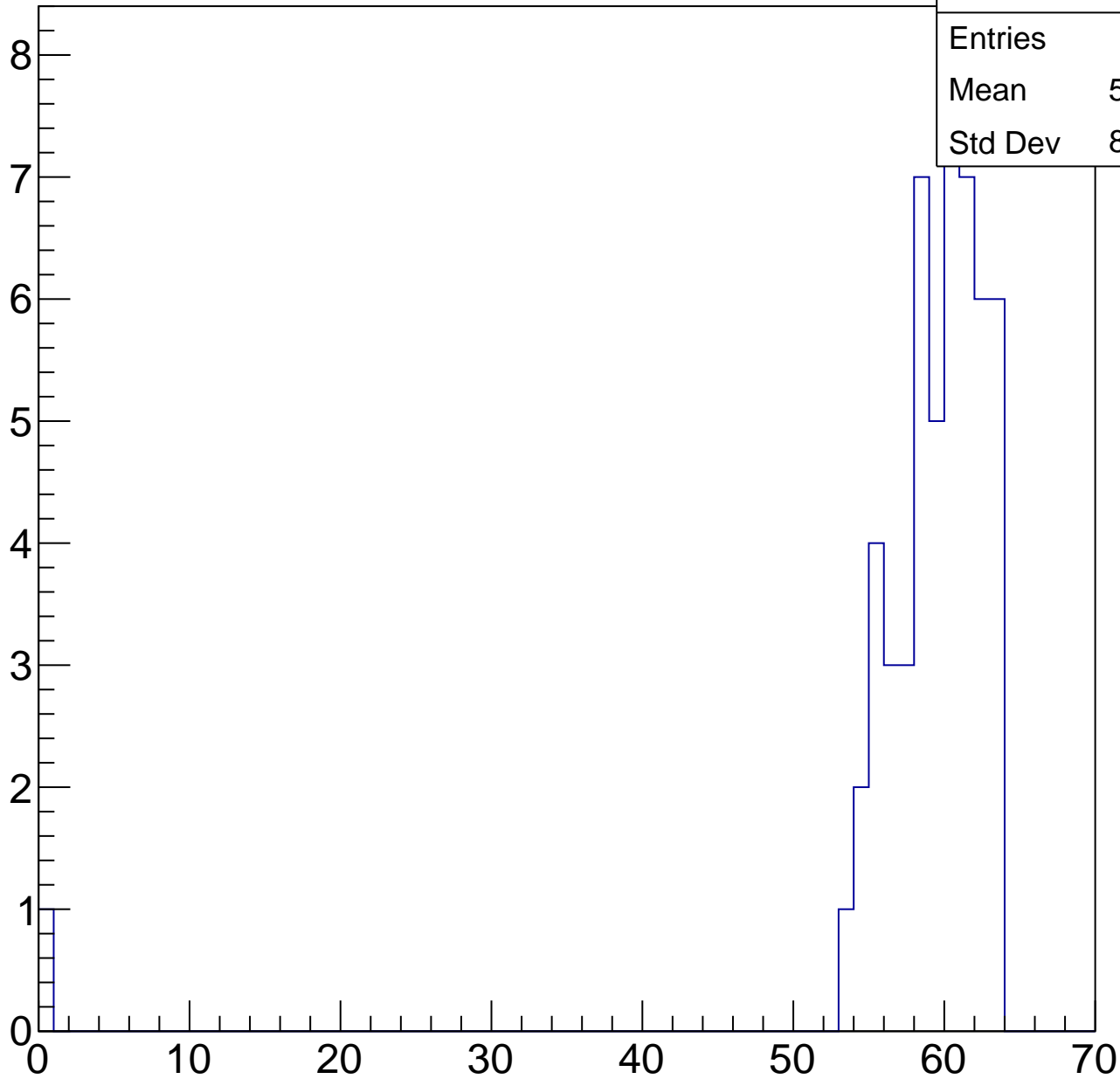
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	53
Mean	58.08
Std Dev	8.487

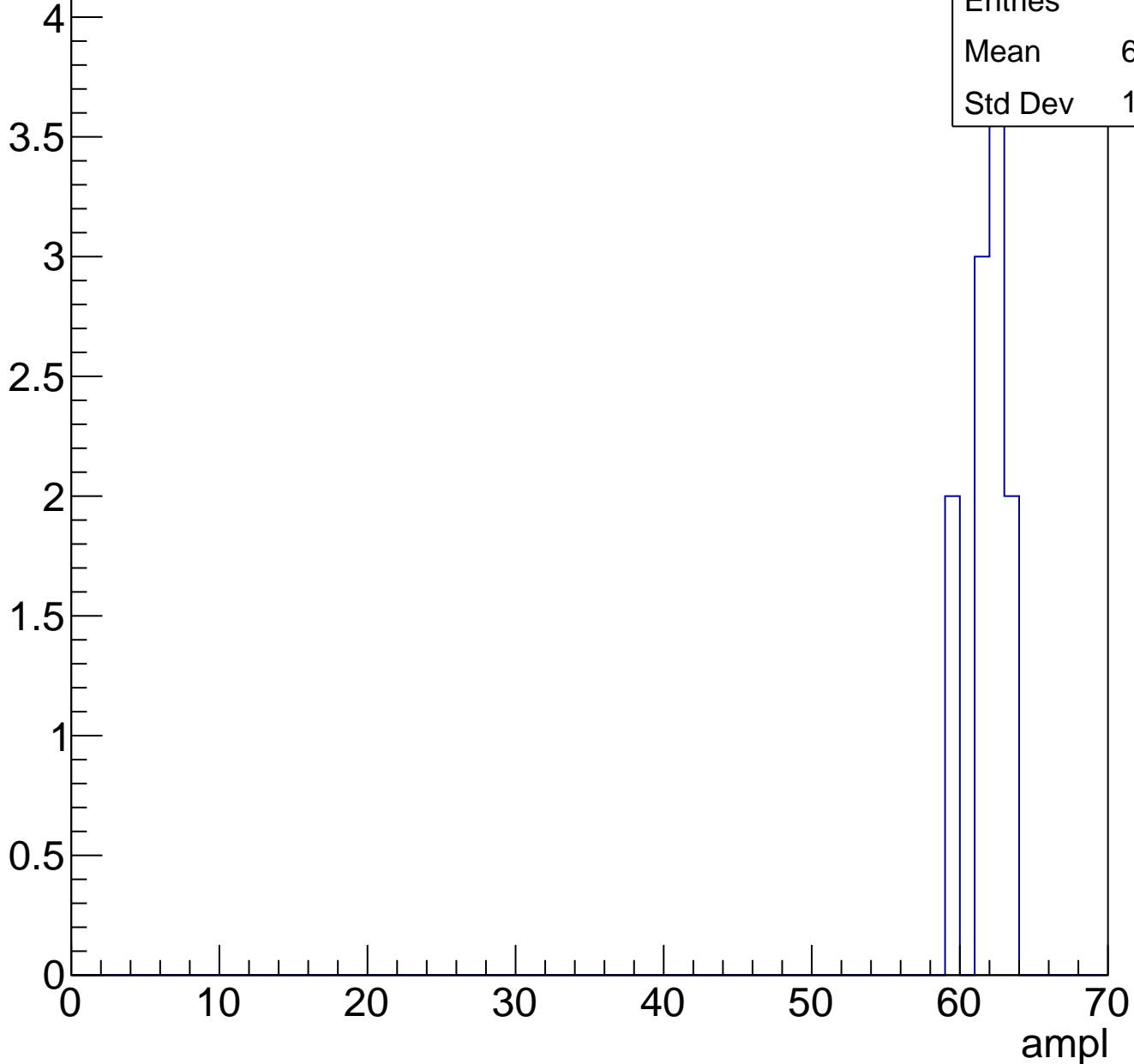
ampl



# B1L103S, U16-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch76, adc0

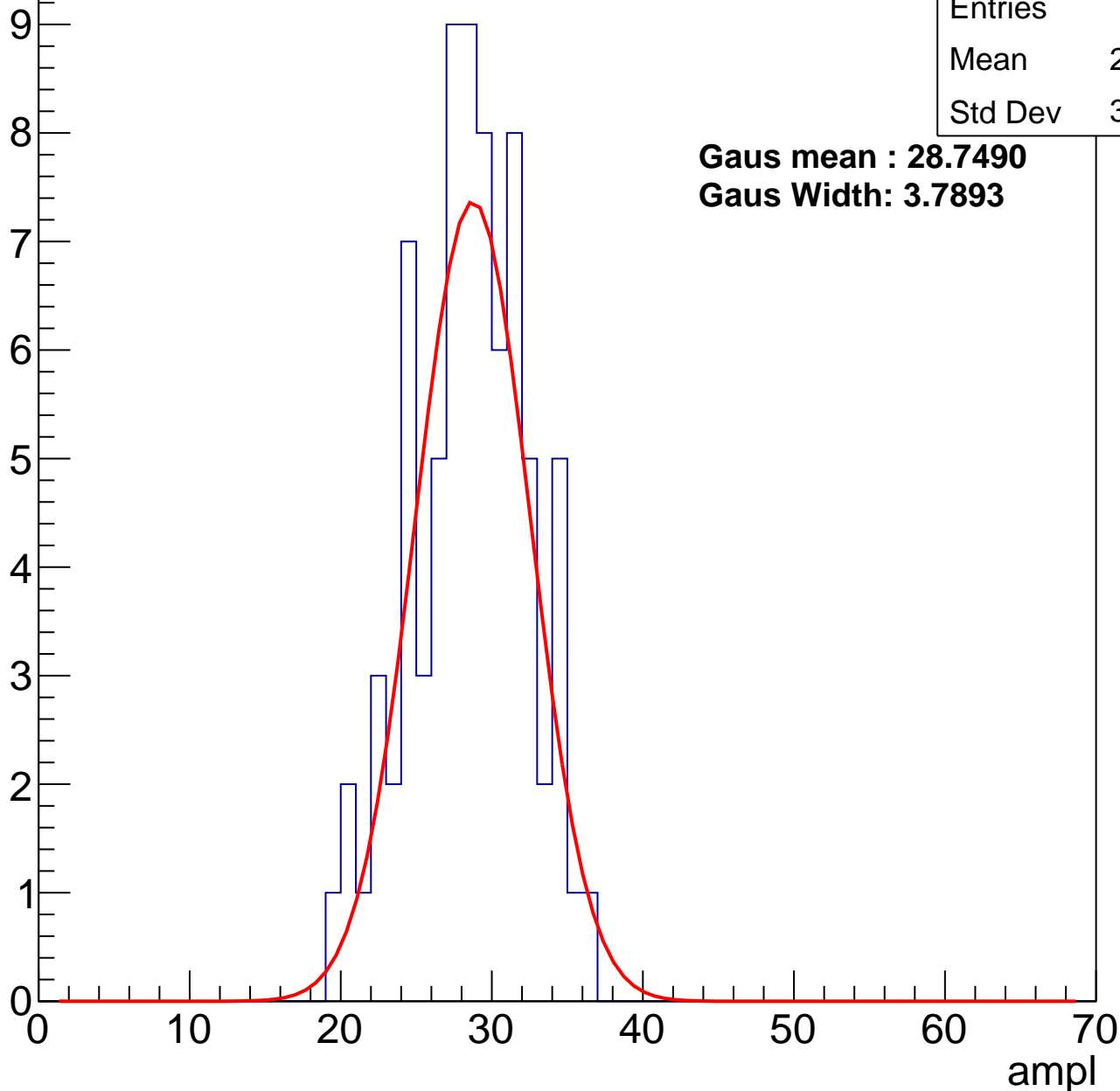
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	28.04
Std Dev	3.774

**Gaus mean : 28.7490**

**Gaus Width: 3.7893**



# B1L103S, U16-ch76, adc1

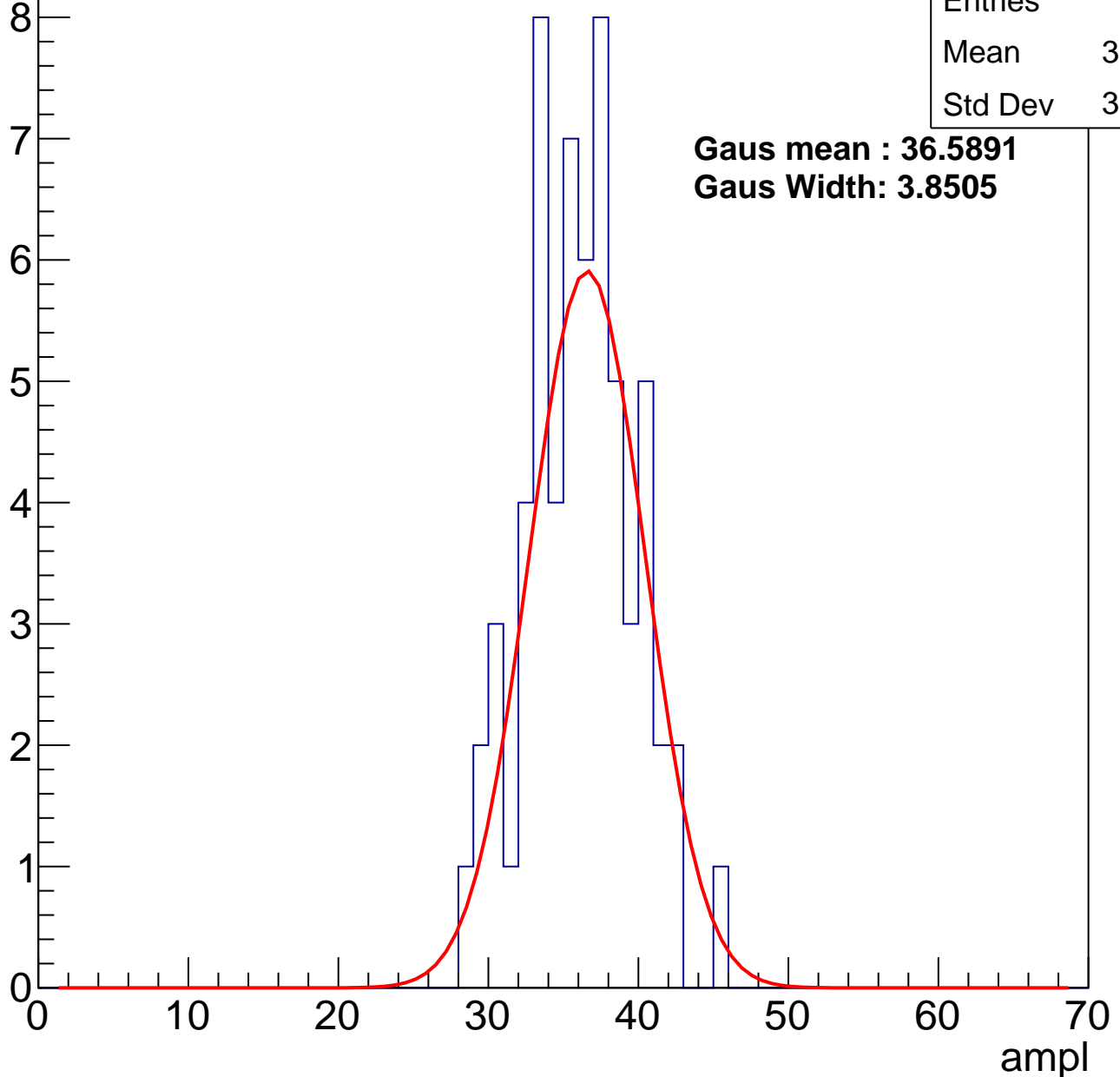
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	35.65
Std Dev	3.556

**Gaus mean : 36.5891**

**Gaus Width: 3.8505**



# B1L103S, U16-ch76, adc2

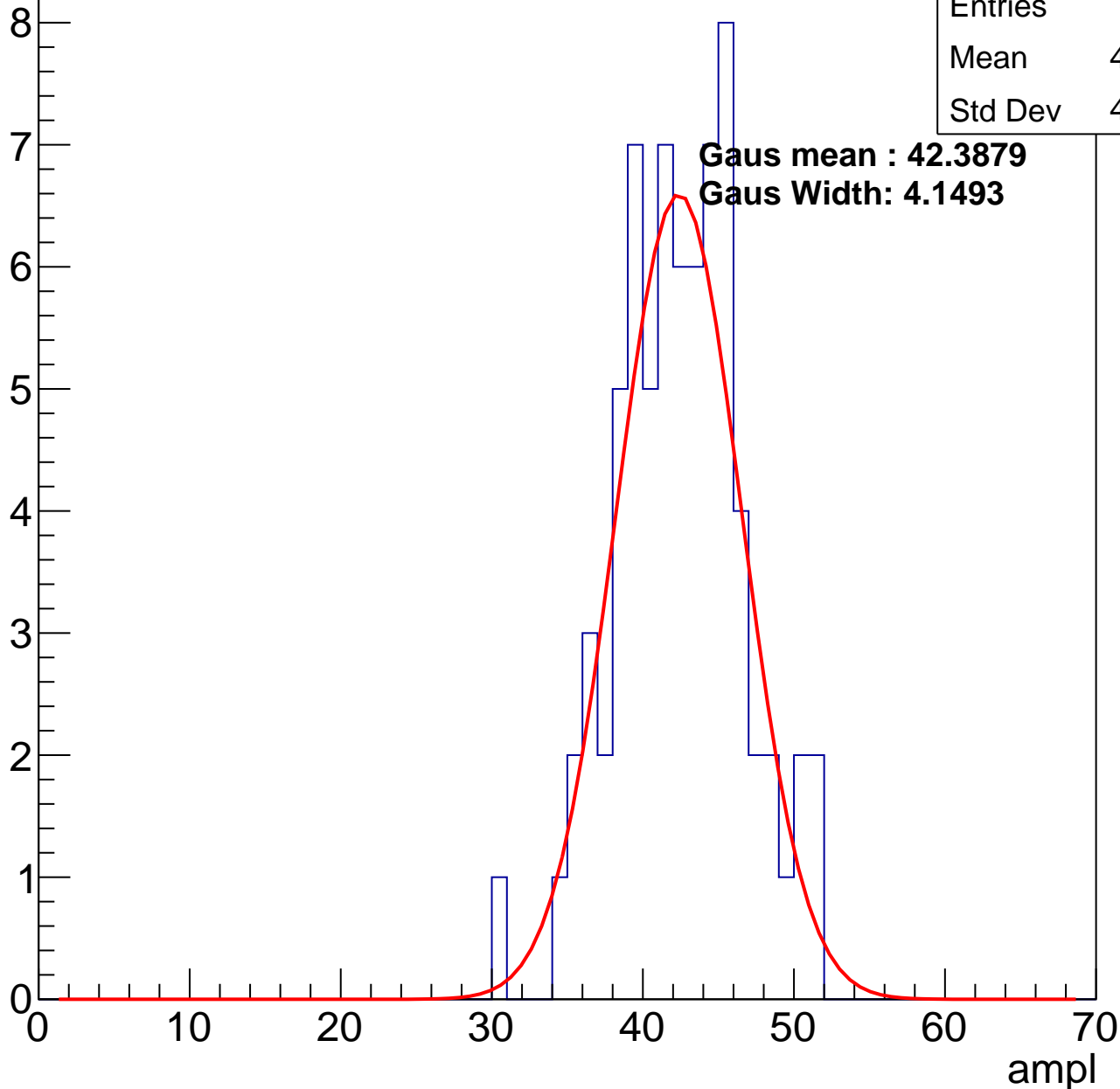
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	42.04
Std Dev	4.163

**Gaus mean : 42.3879**

**Gaus Width: 4.1493**

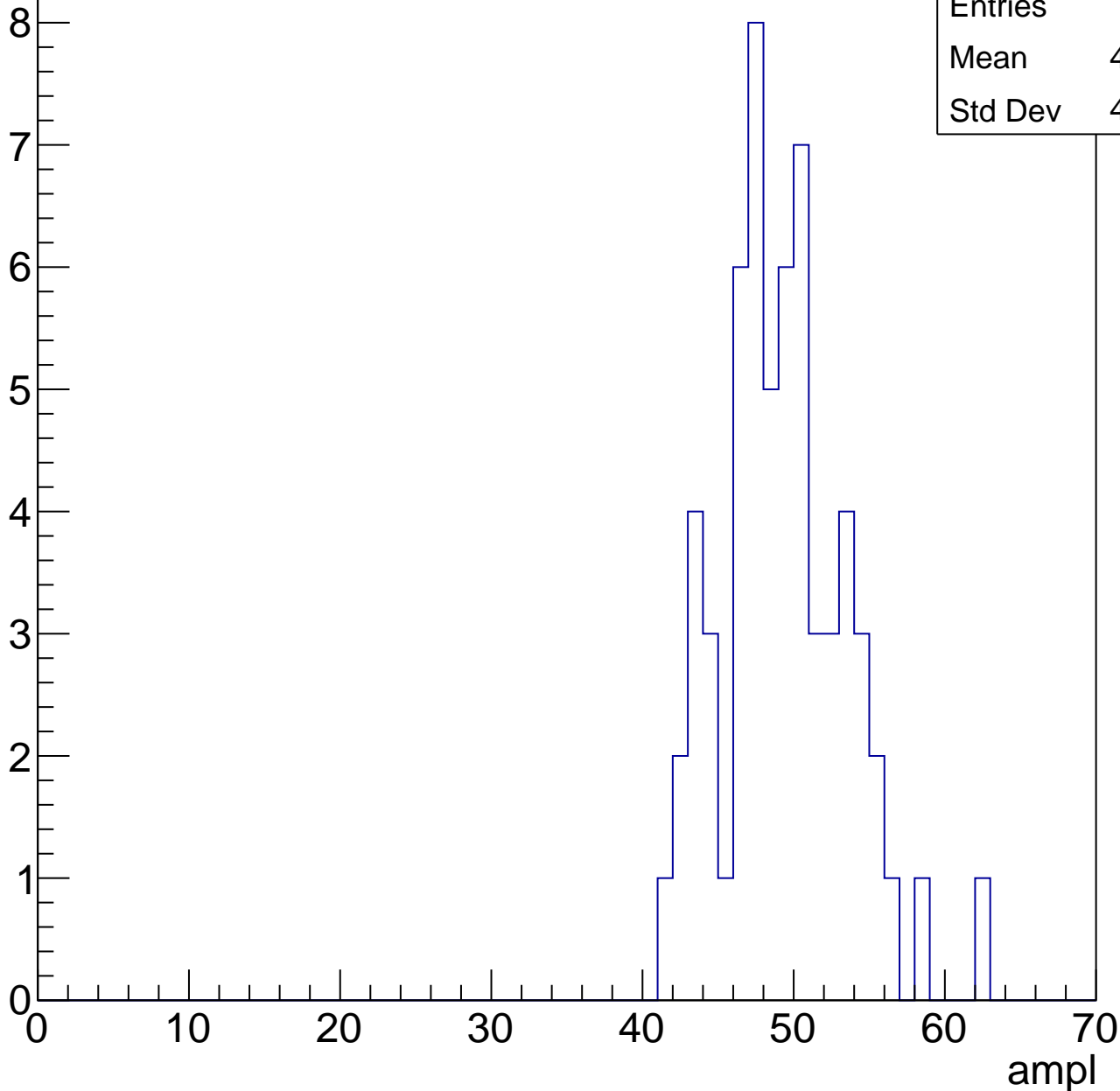


# B1L103S, U16-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	48.84
Std Dev	4.134

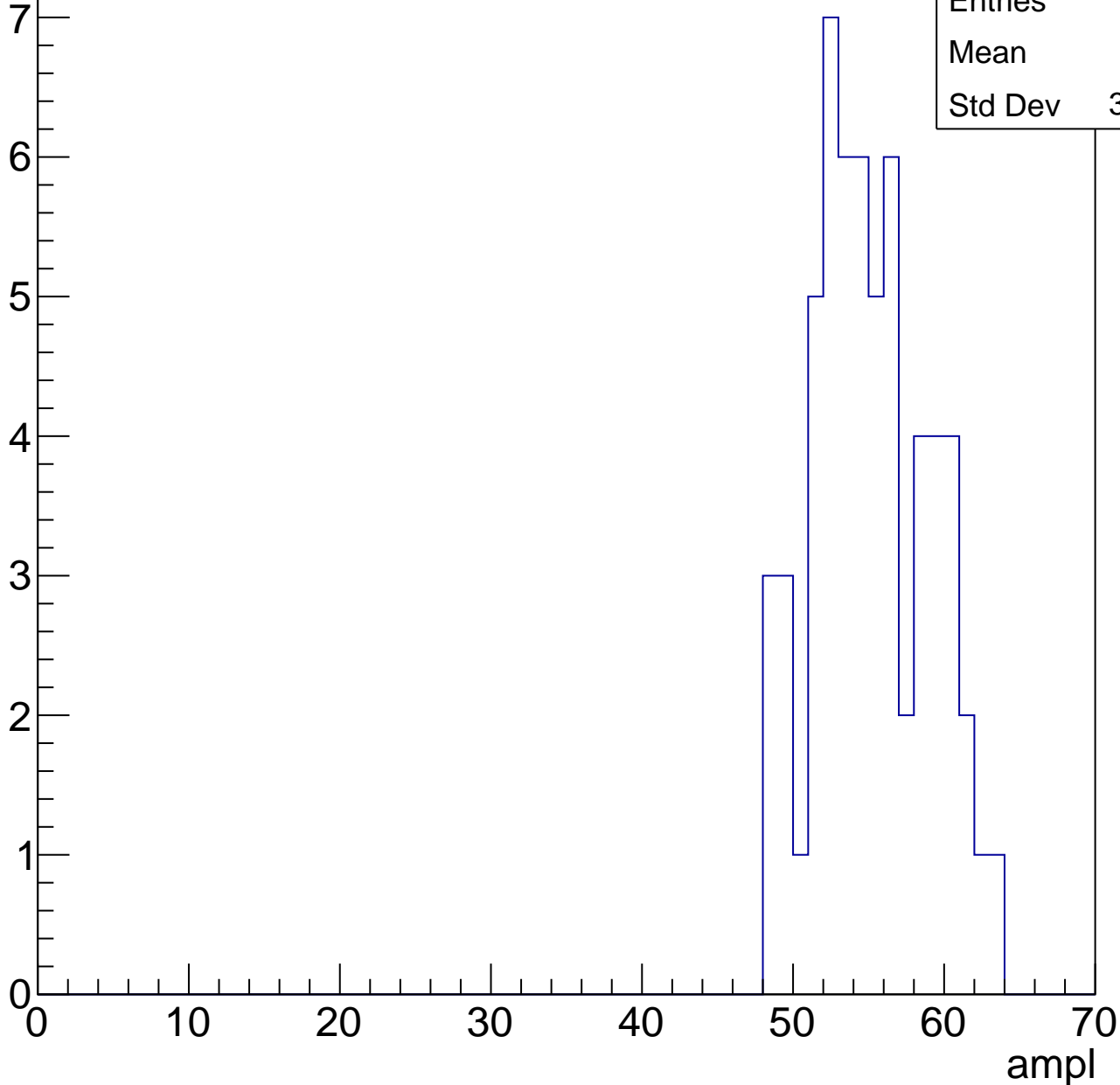


# B1L103S, U16-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

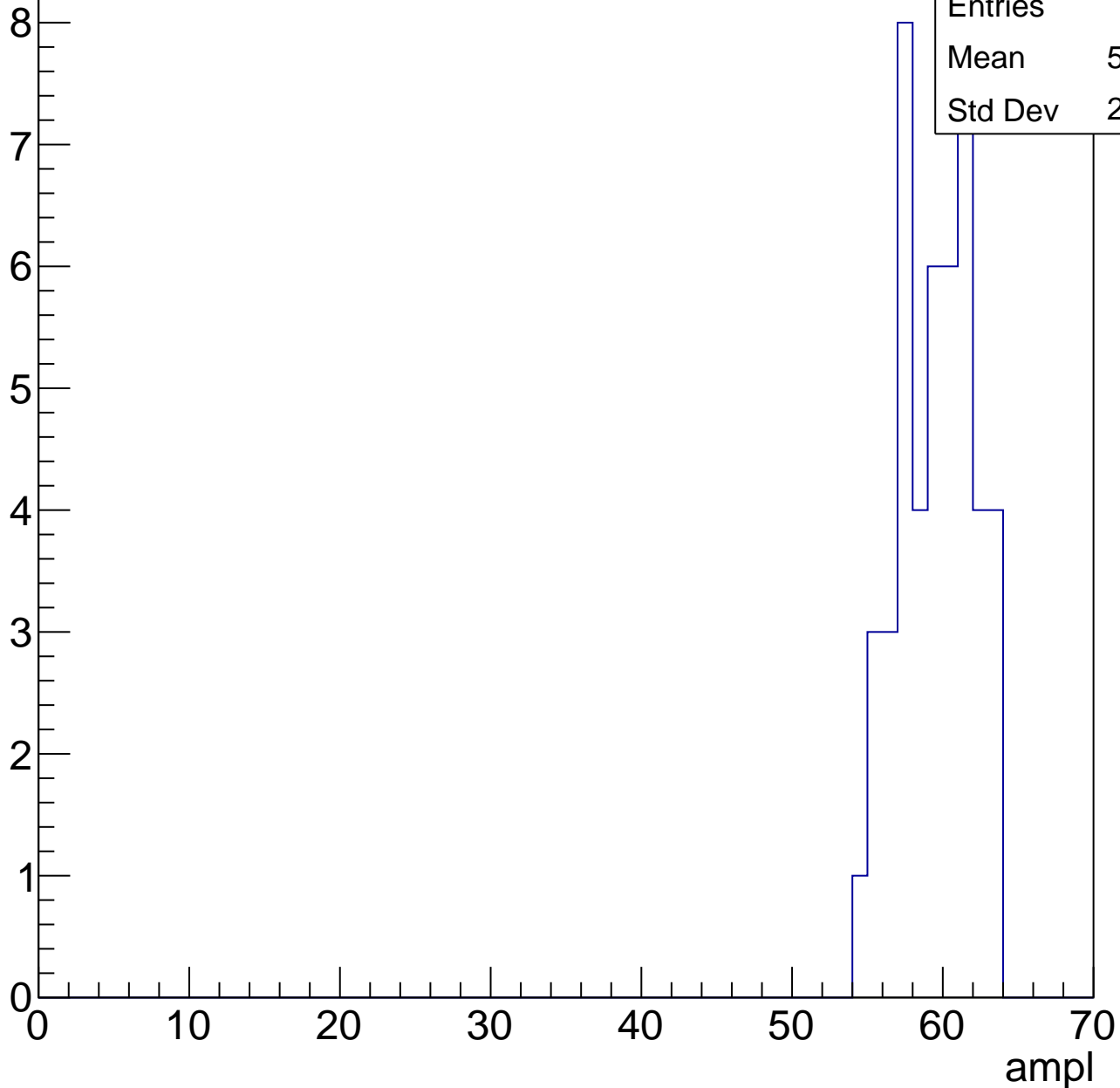
Entries	60
Mean	54.7
Std Dev	3.756



# B1L103S, U16-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

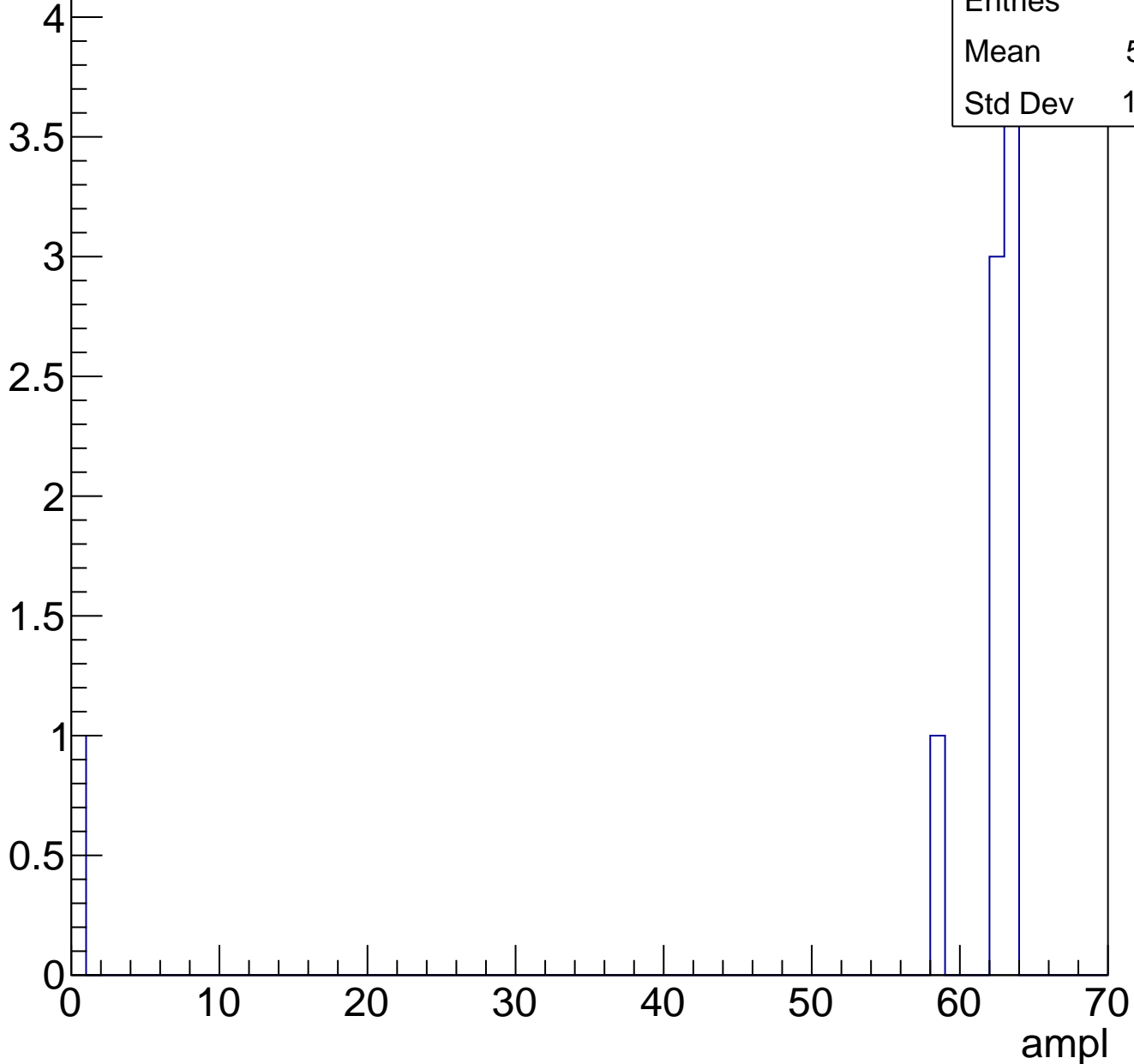


Entries	47
Mean	59.09
Std Dev	2.413

# B1L103S, U16-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

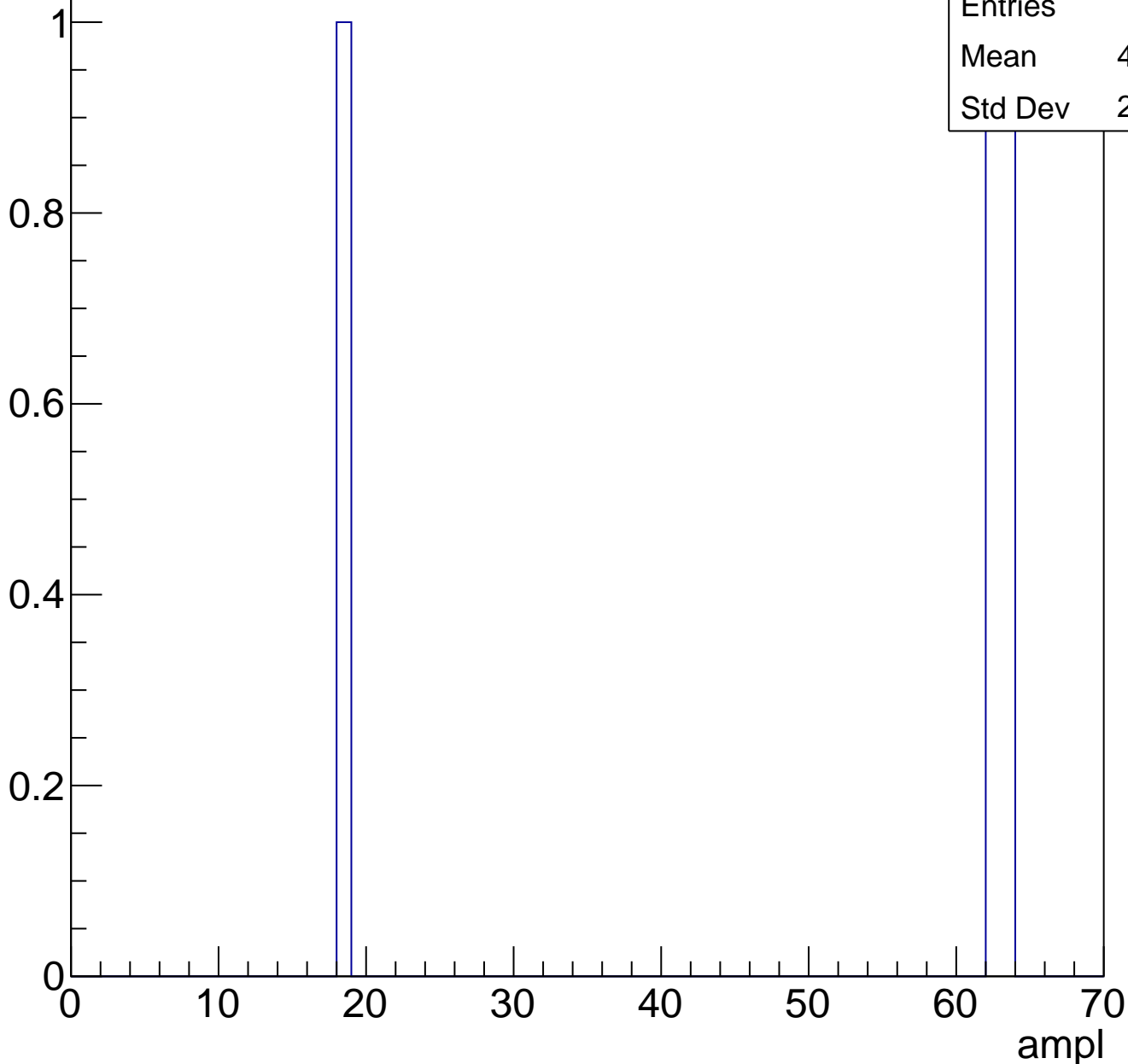




# B1L103S, U16-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch77, adc0

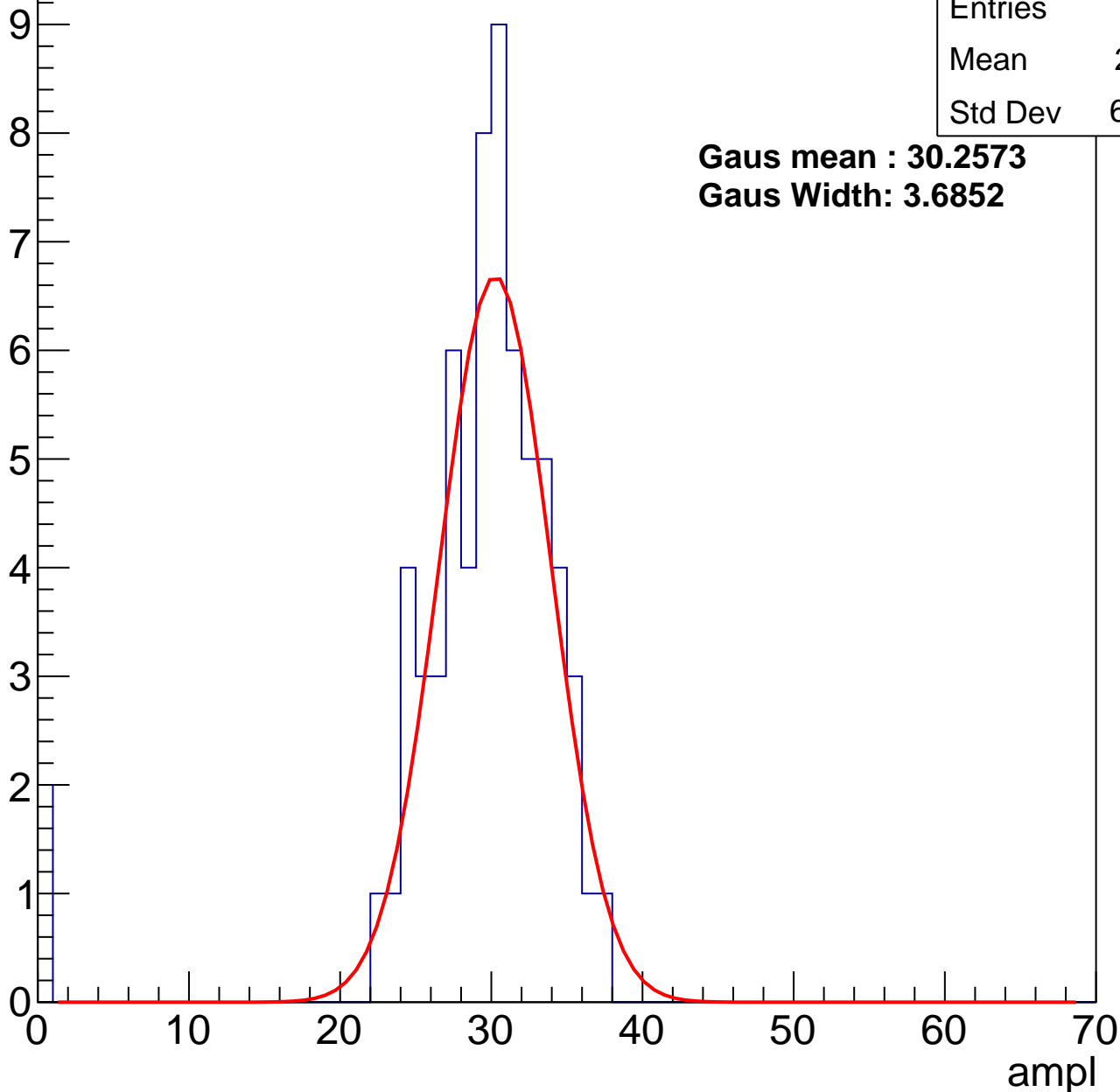
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	28.71
Std Dev	6.085

**Gaus mean : 30.2573**

**Gaus Width: 3.6852**



# B1L103S, U16-ch77, adc1

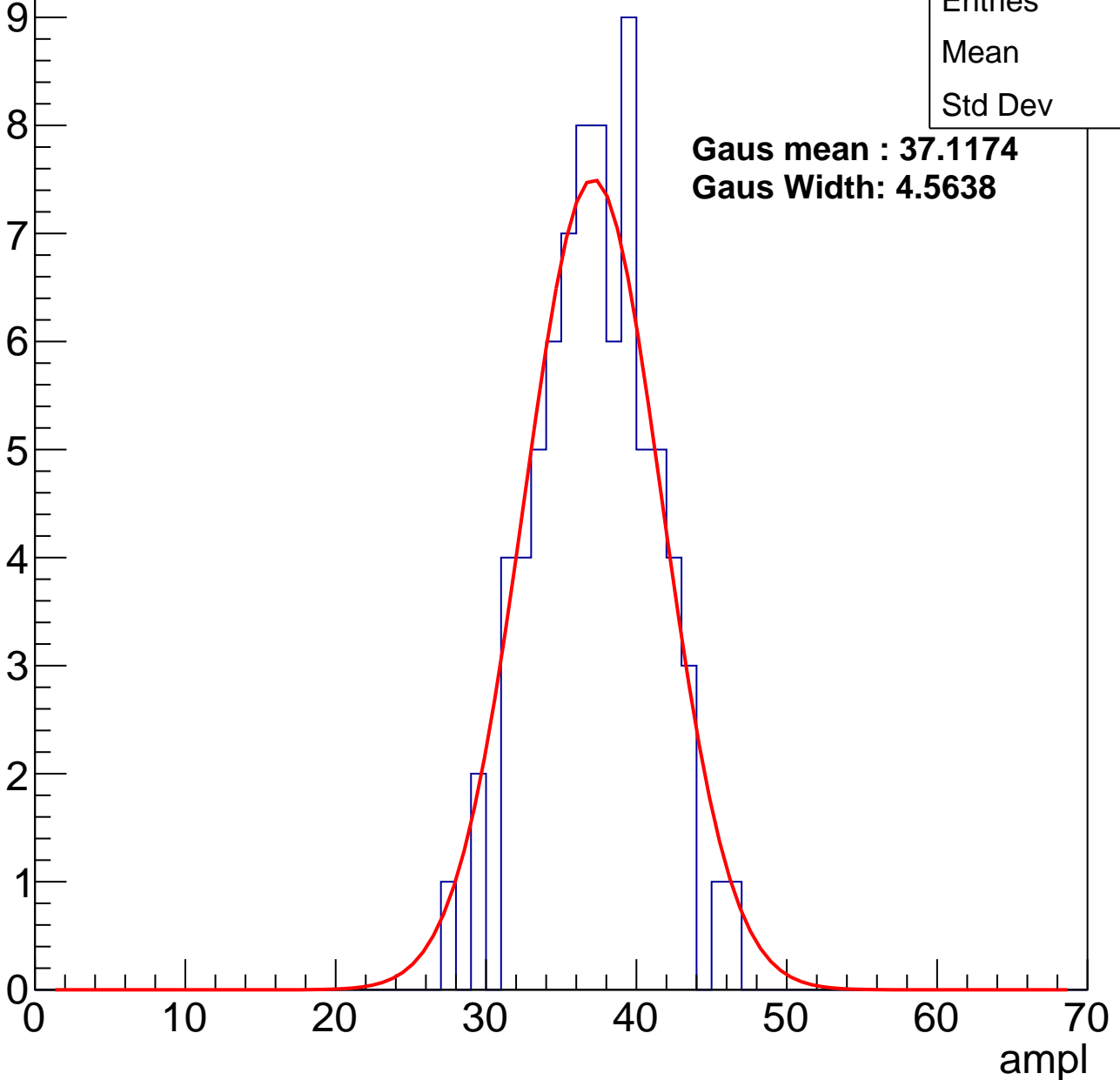
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	36.8
Std Dev	3.83

**Gaus mean : 37.1174**

**Gaus Width: 4.5638**



# B1L103S, U16-ch77, adc2

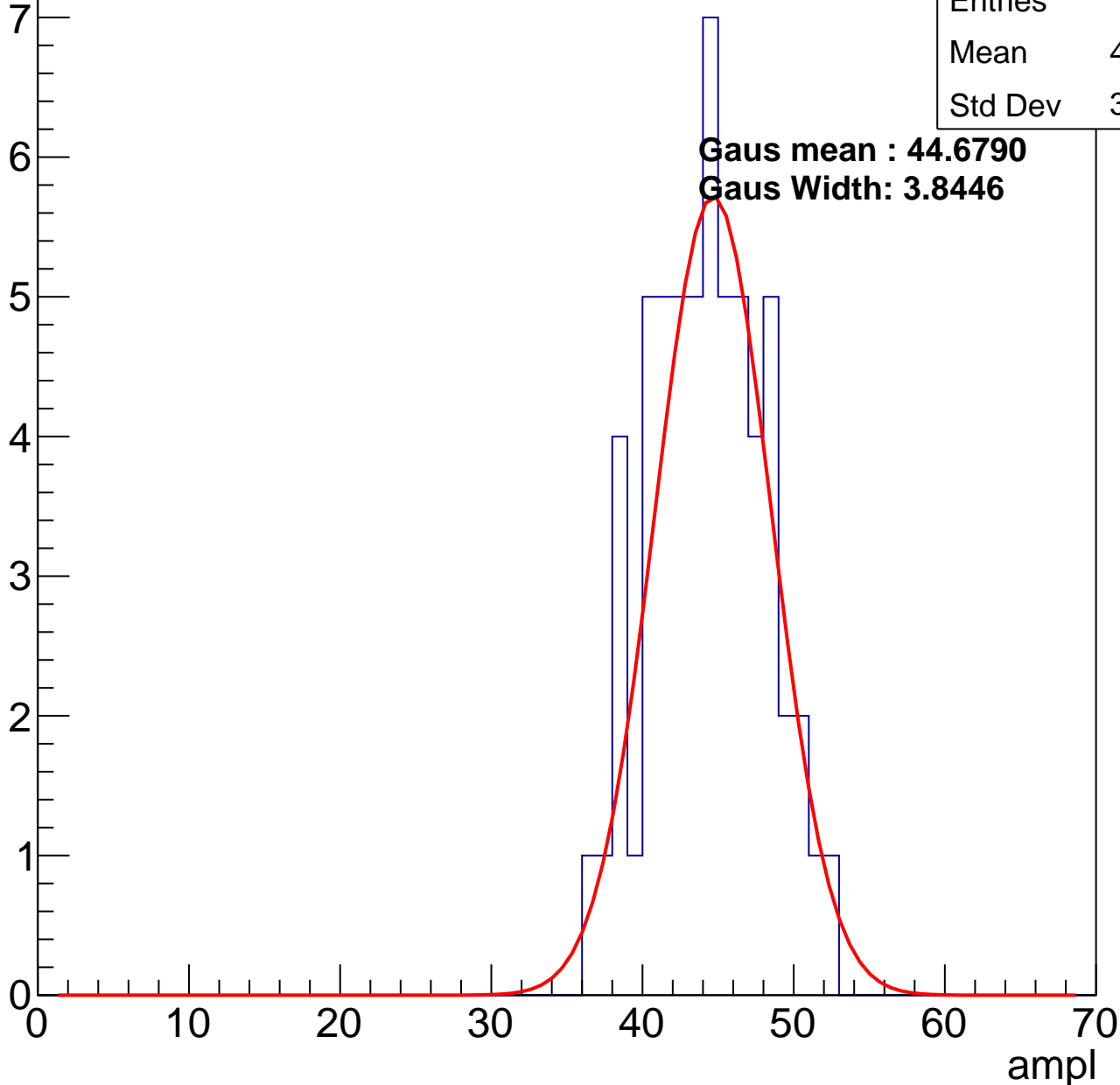
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	43.83
Std Dev	3.697

**Gaus mean : 44.6790**

**Gaus Width: 3.8446**

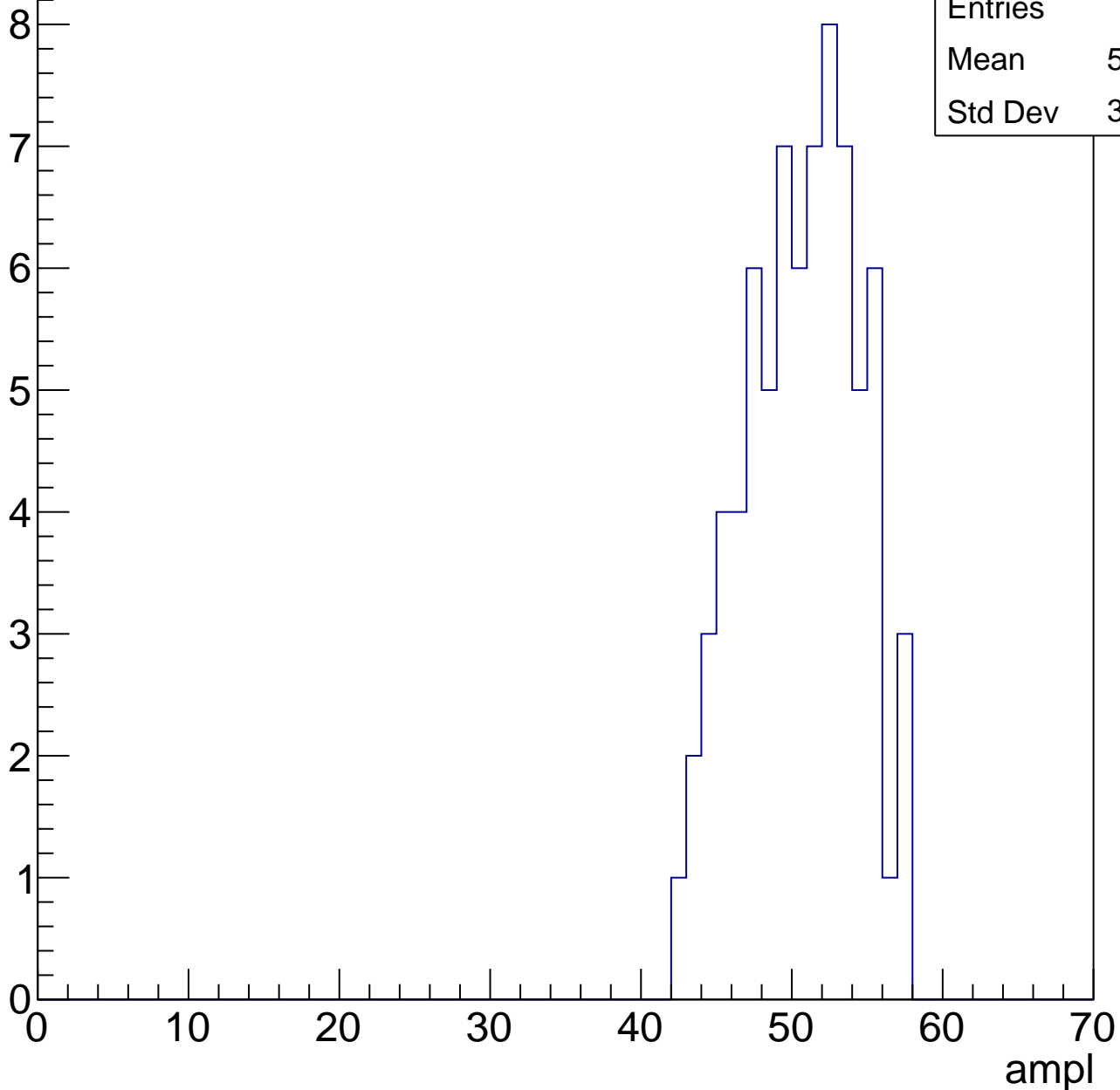


# B1L103S, U16-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	50.13
Std Dev	3.703

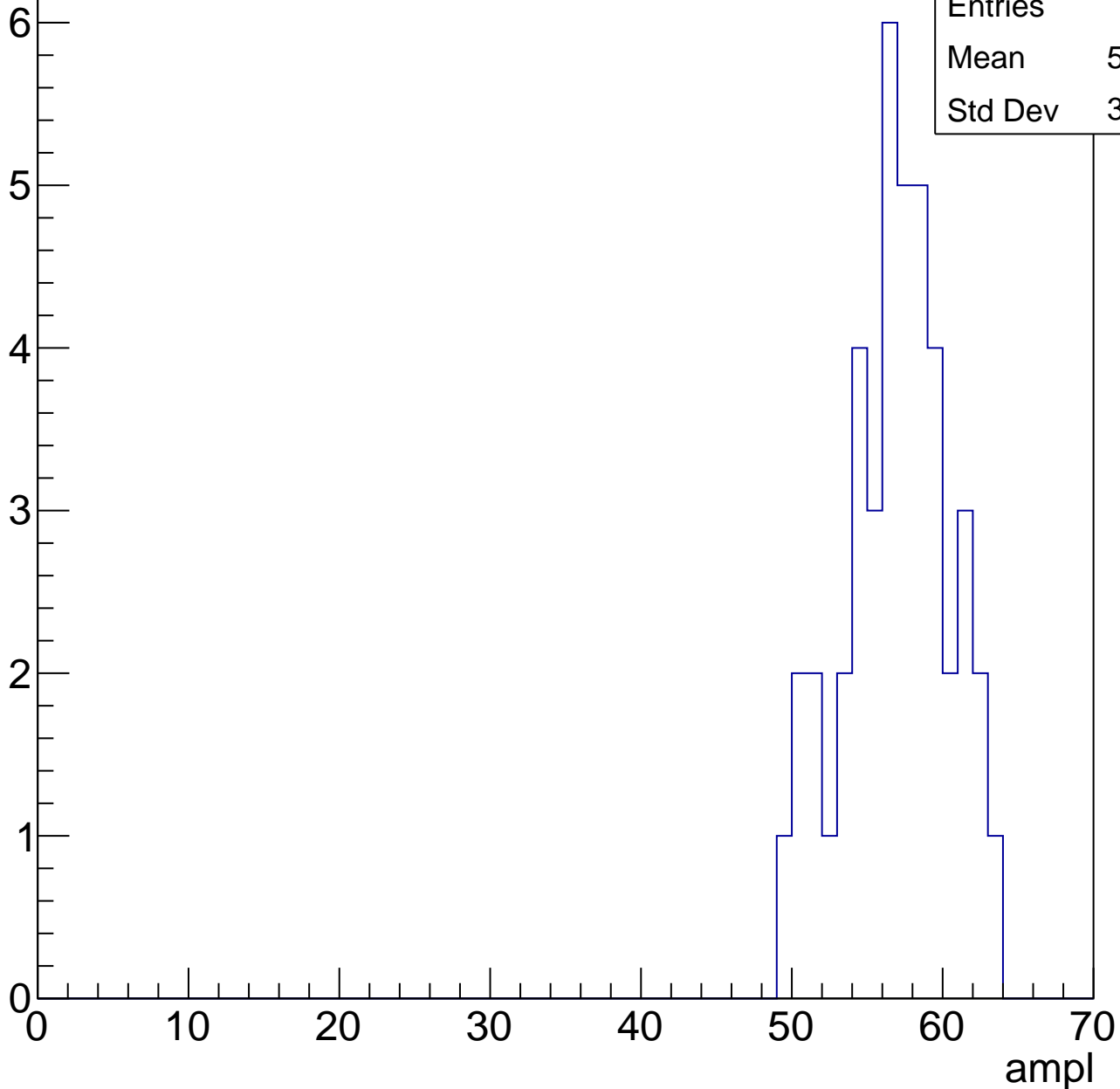


# B1L103S, U16-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	43
Mean	56.44
Std Dev	3.426



# B1L103S, U16-ch77, adc5

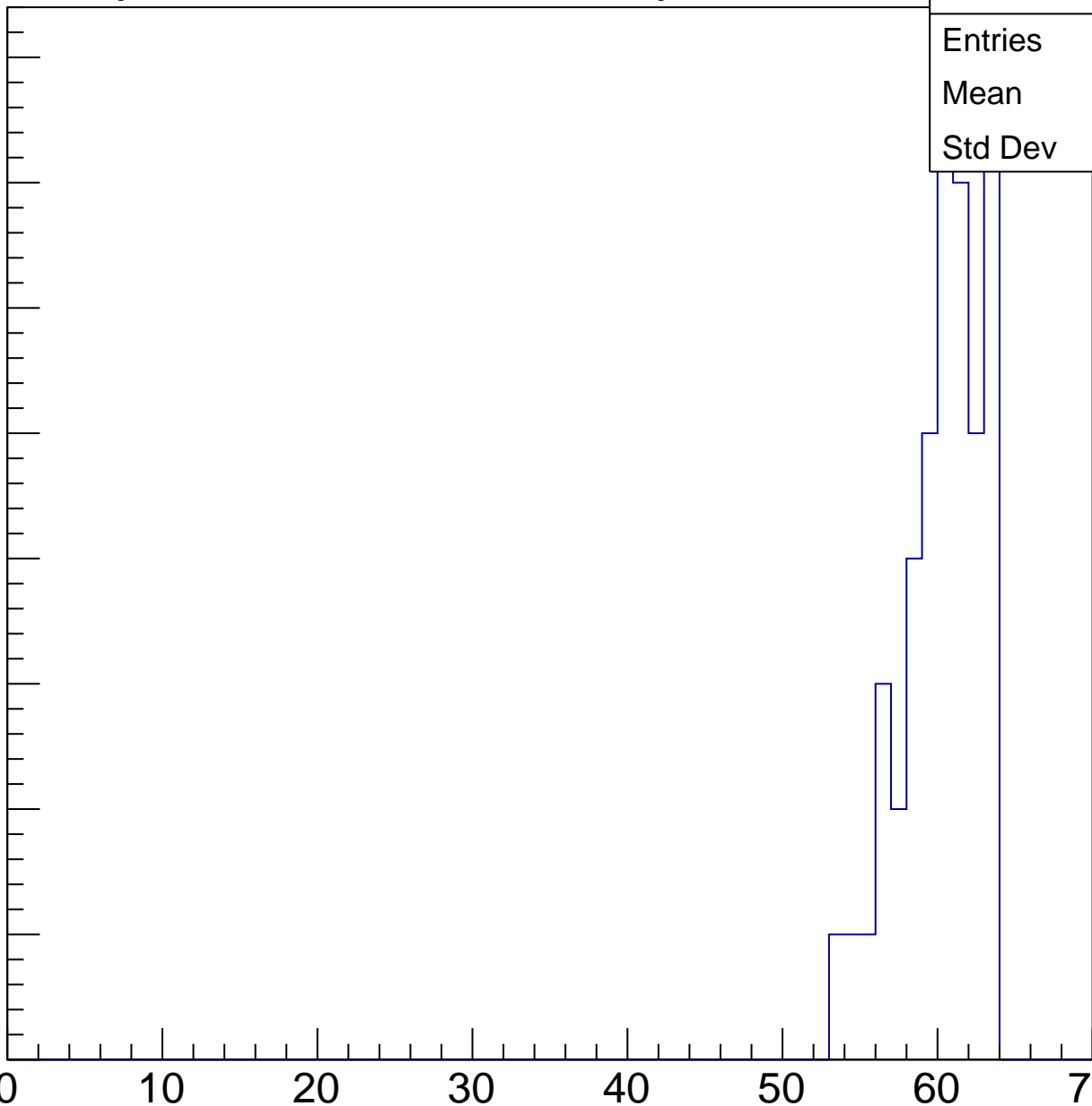
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	45
Mean	59.82
Std Dev	2.559

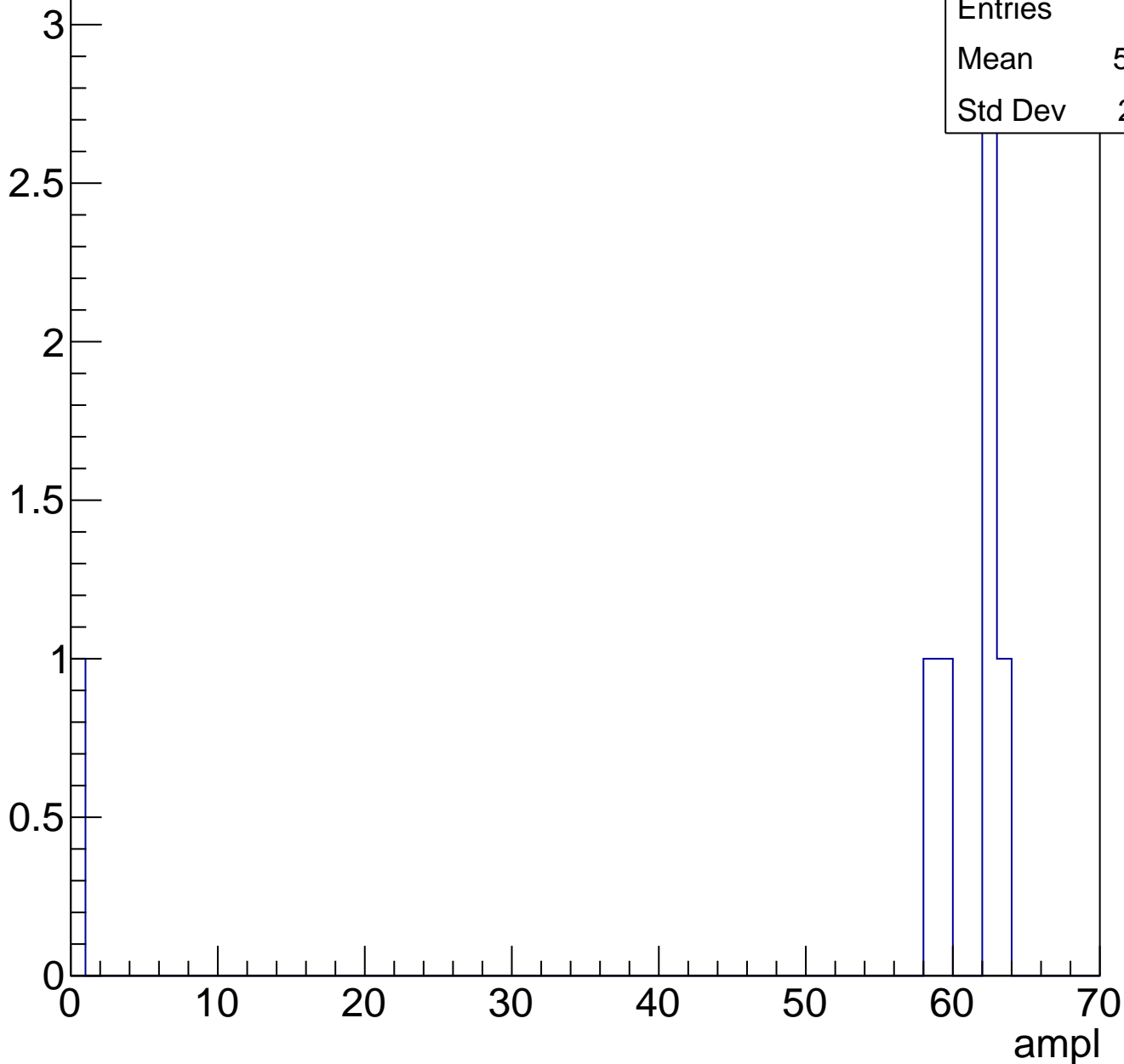
ampl



# B1L103S, U16-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U16-ch78, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	71
Mean	27.93
Std Dev	4.604

**Gaus mean : 28.6930**

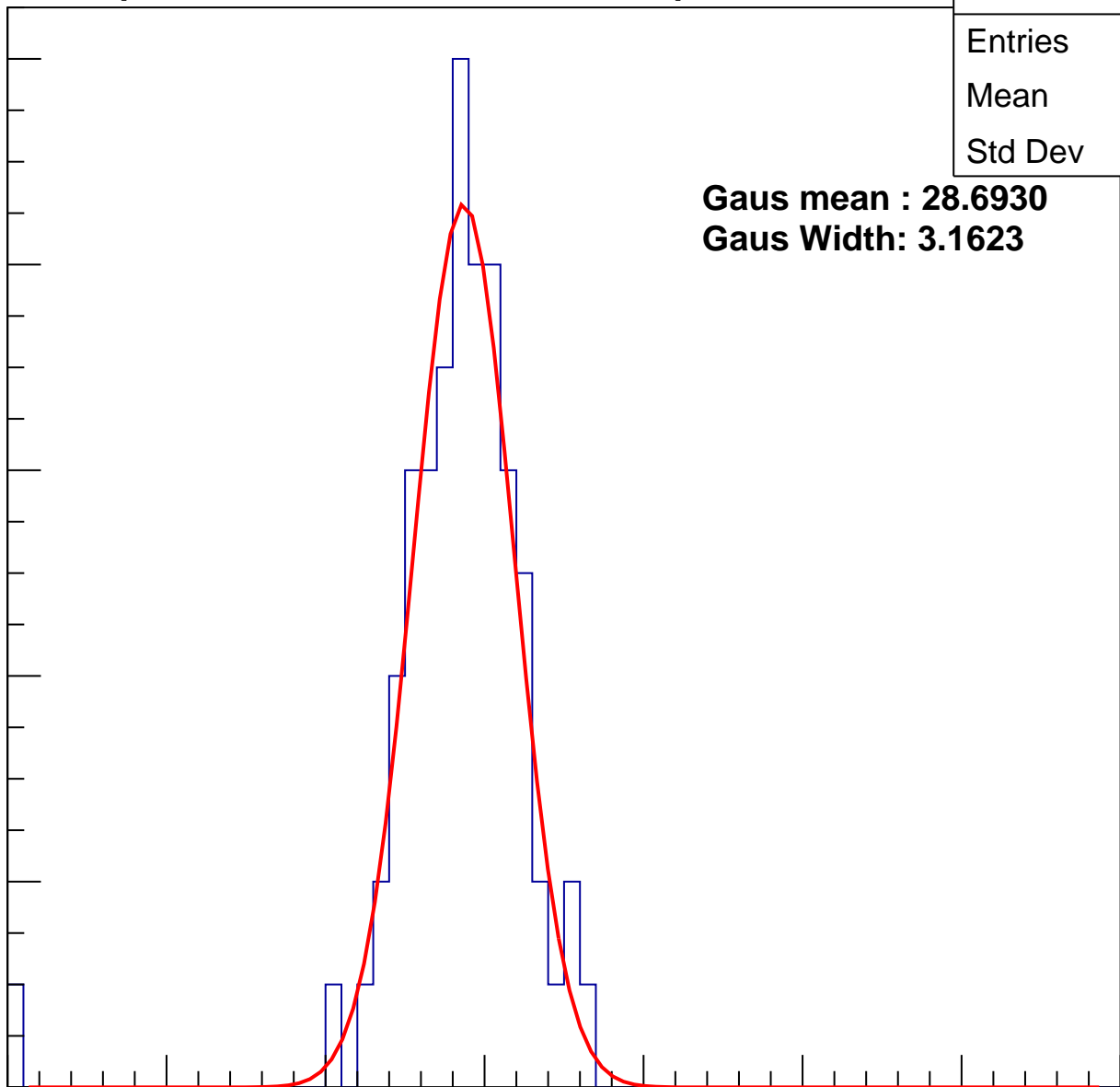
**Gaus Width: 3.1623**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U16-ch78, adc1

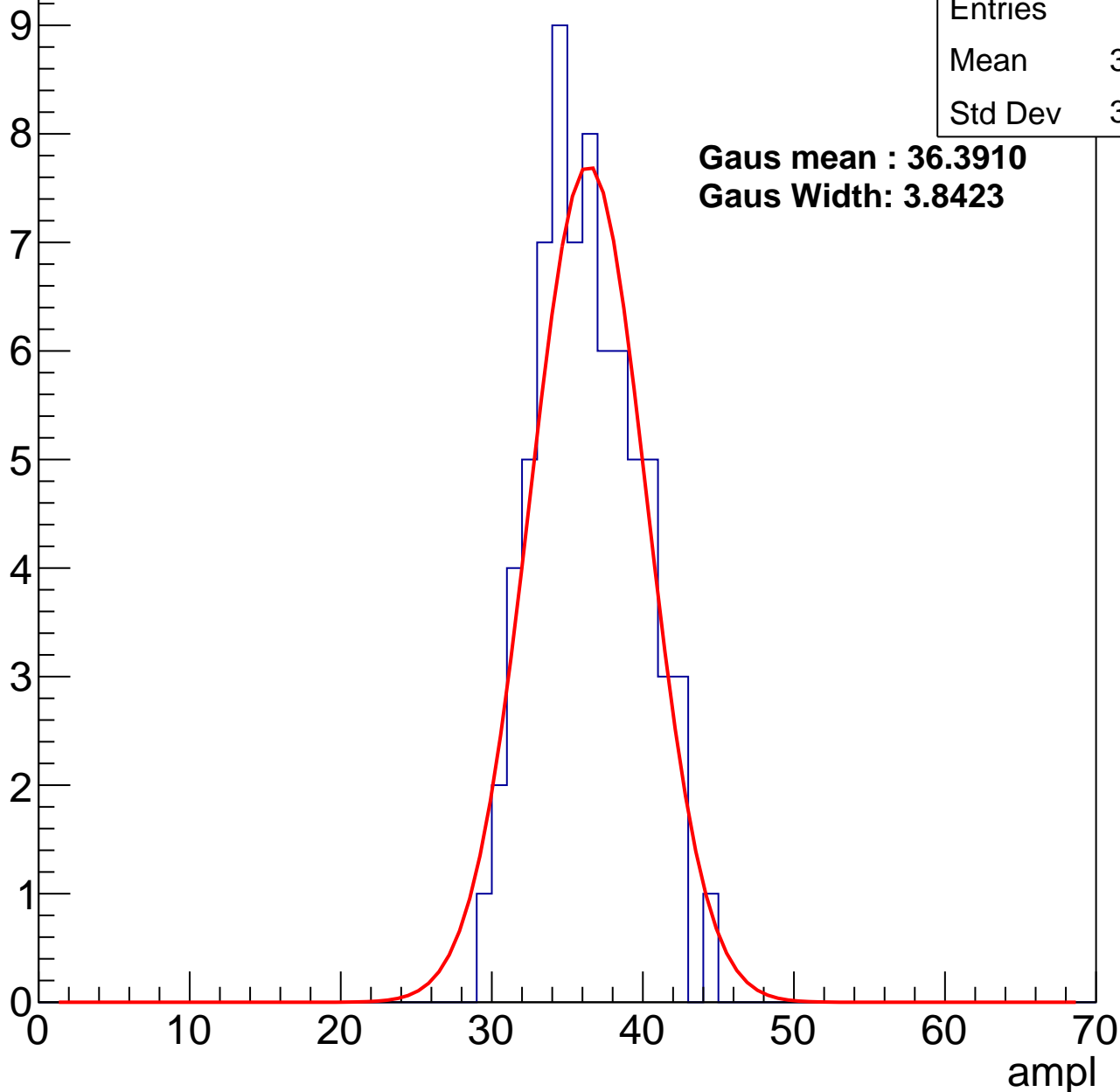
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	35.85
Std Dev	3.349

**Gaus mean : 36.3910**

**Gaus Width: 3.8423**



# B1L103S, U16-ch78, adc2

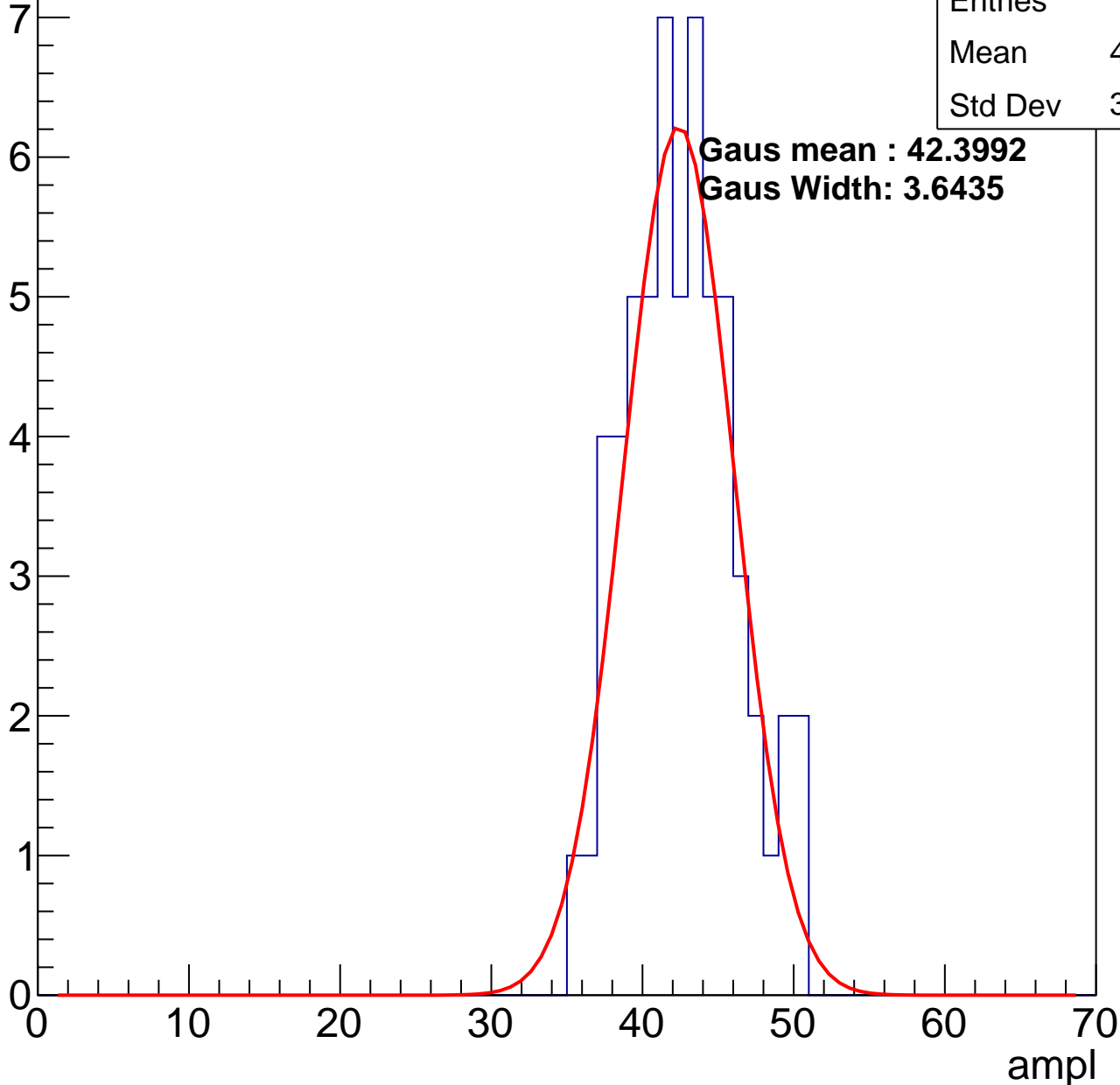
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	42.15
Std Dev	3.569

**Gaus mean : 42.3992**

**Gaus Width: 3.6435**

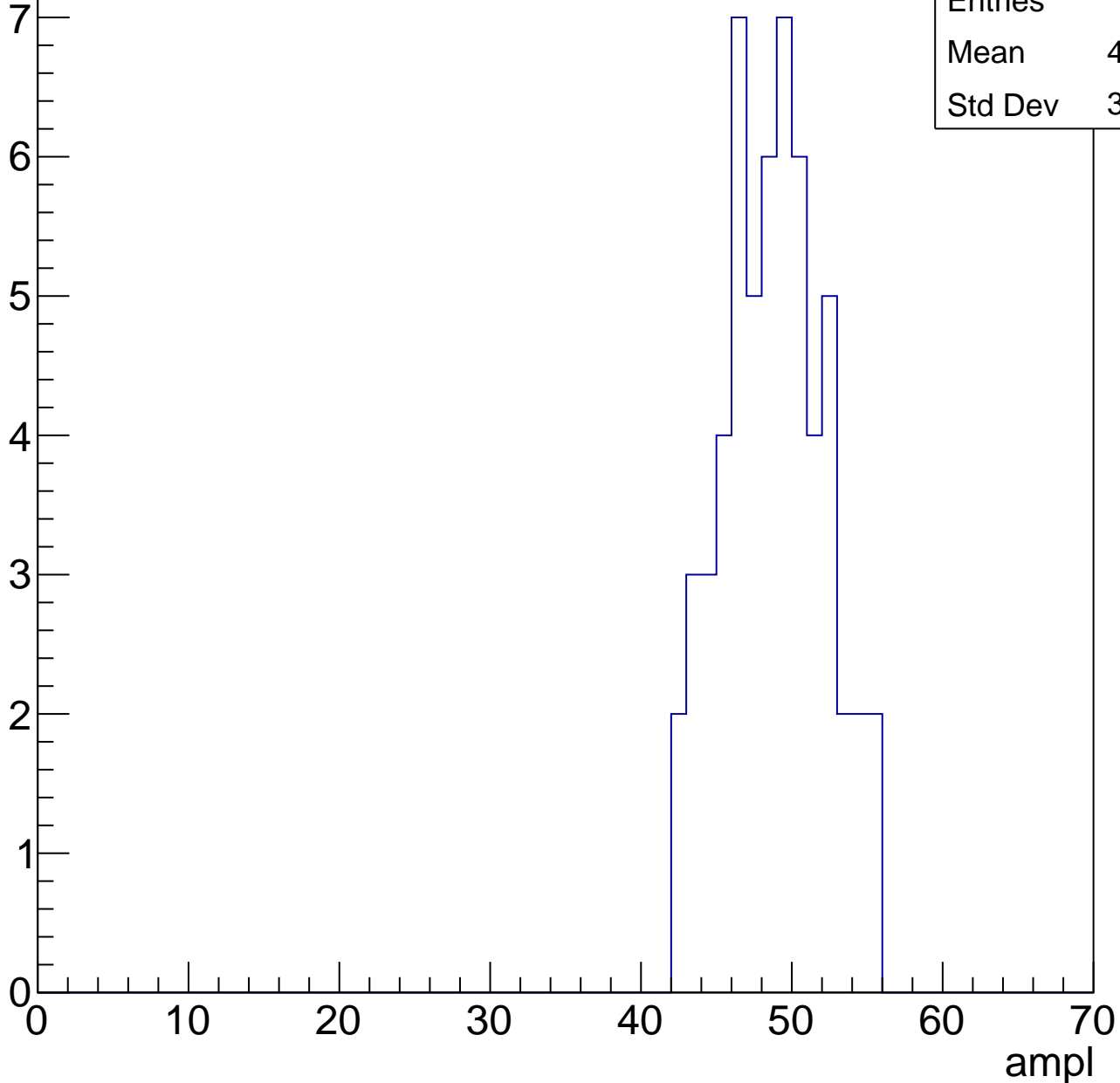


# B1L103S, U16-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	48.29
Std Dev	3.285

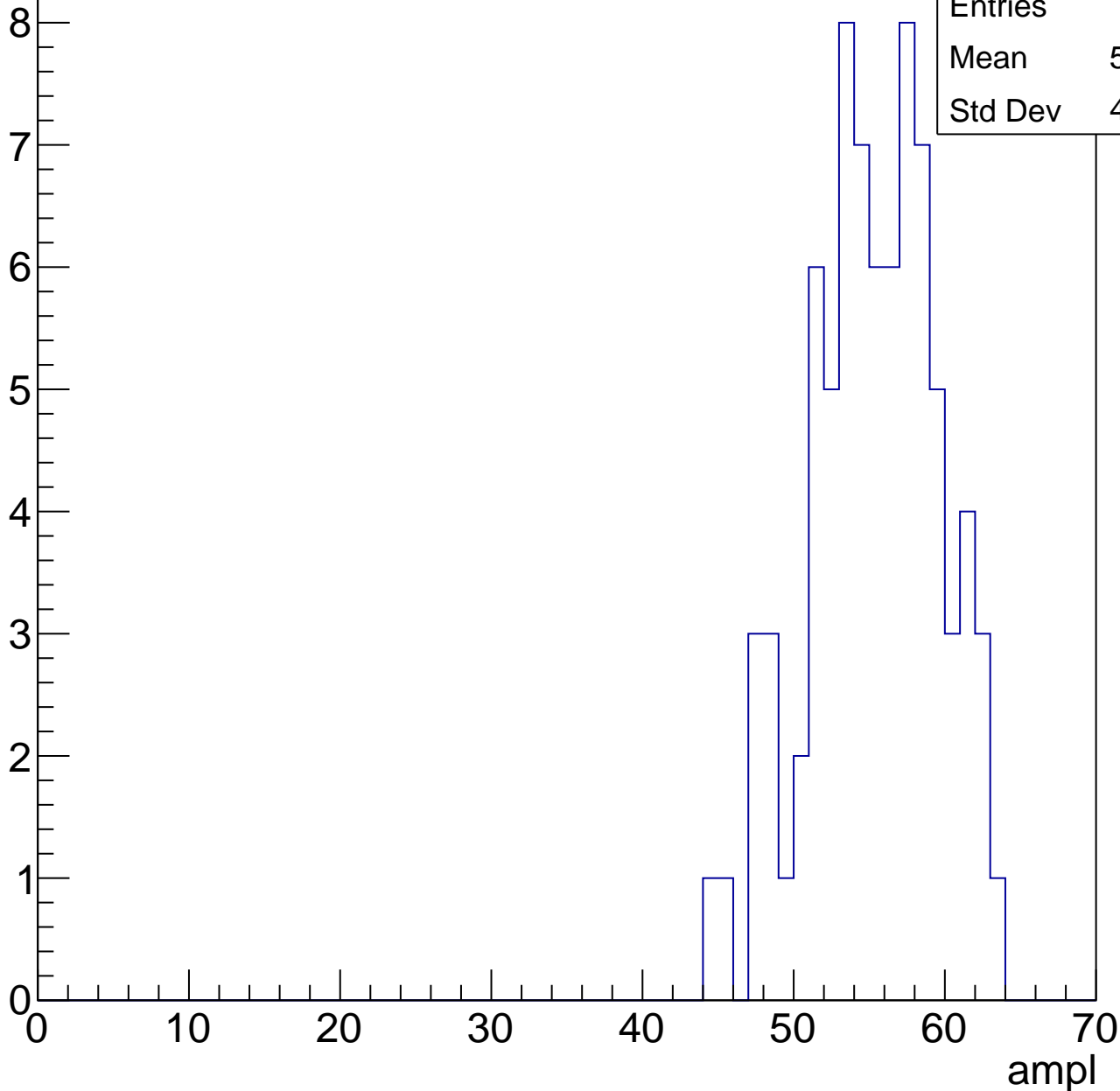


# B1L103S, U16-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

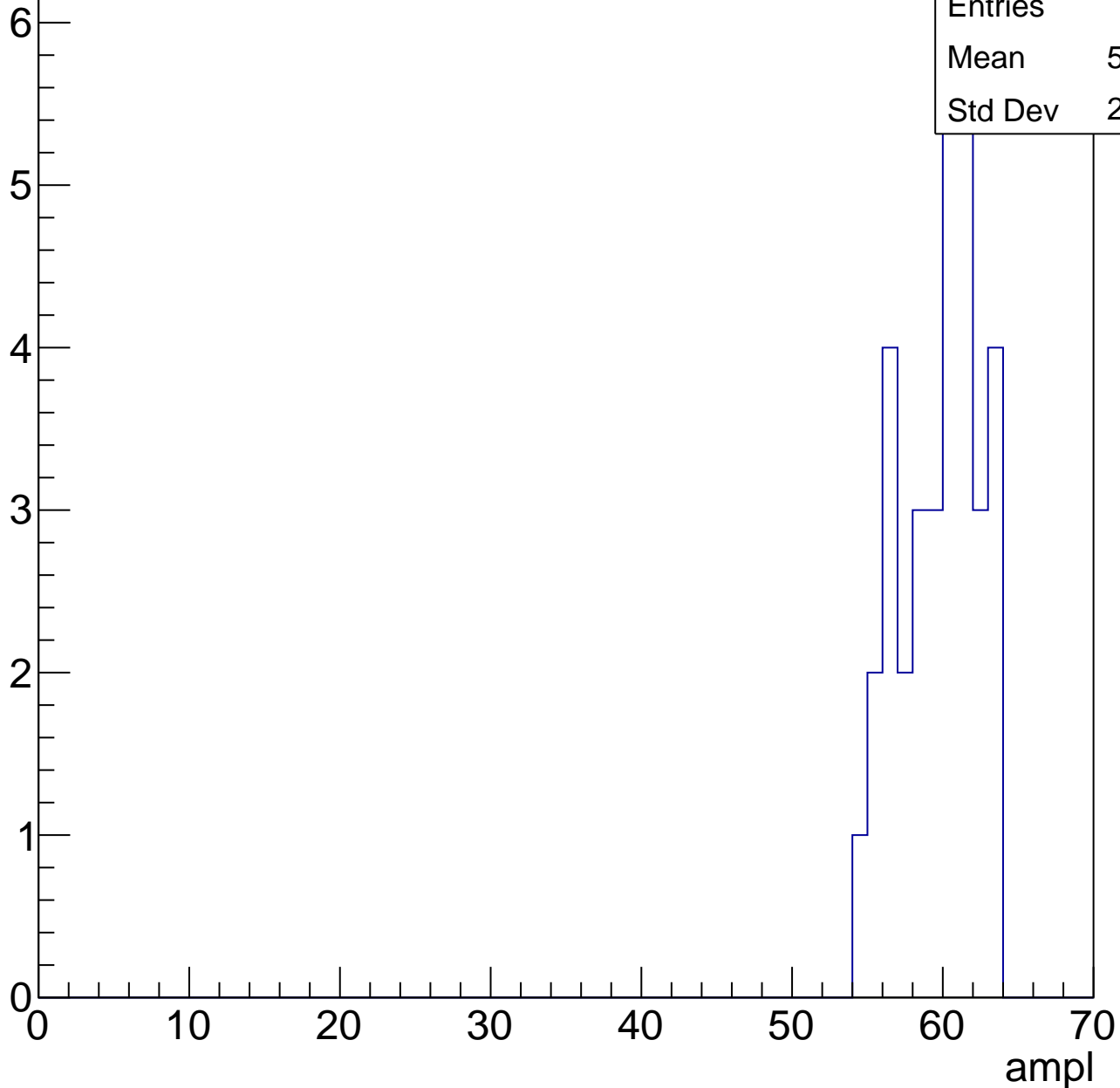
Entries	80
Mean	54.84
Std Dev	4.235



# B1L103S, U16-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

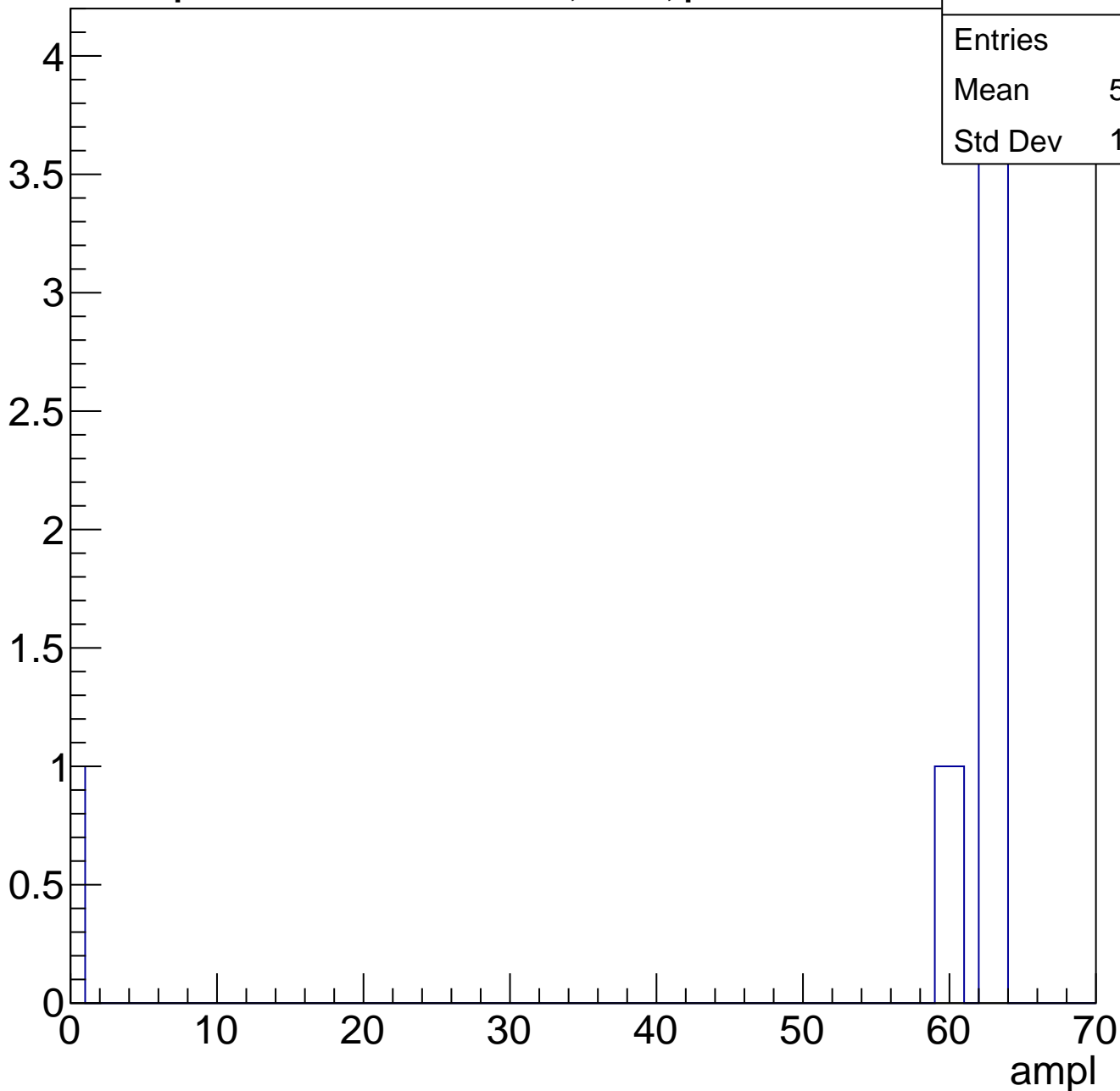
Entry



# B1L103S, U16-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

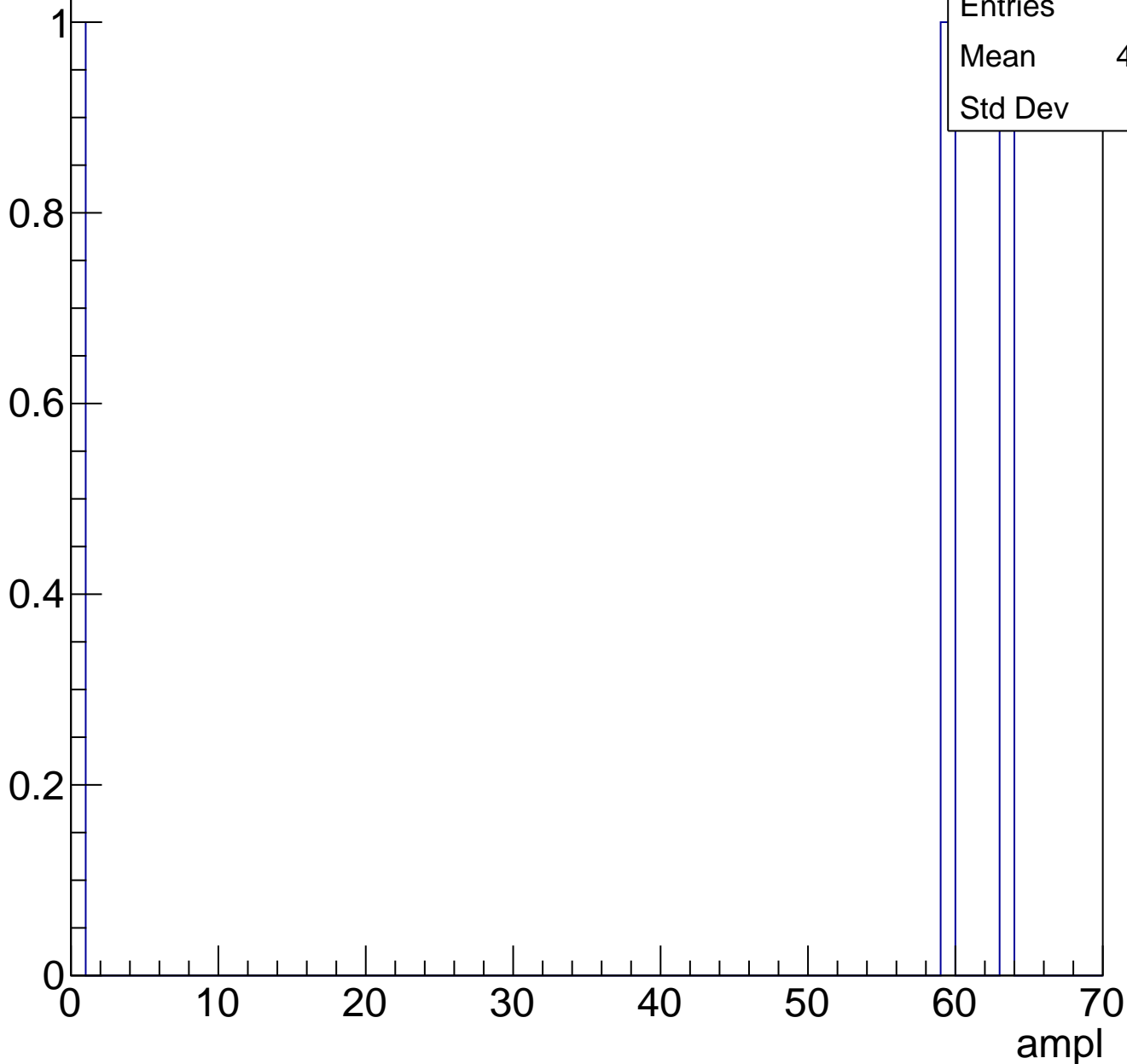




# B1L103S, U16-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch79, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	96
Mean	28.45
Std Dev	6.06

**Gaus mean : 29.3773**

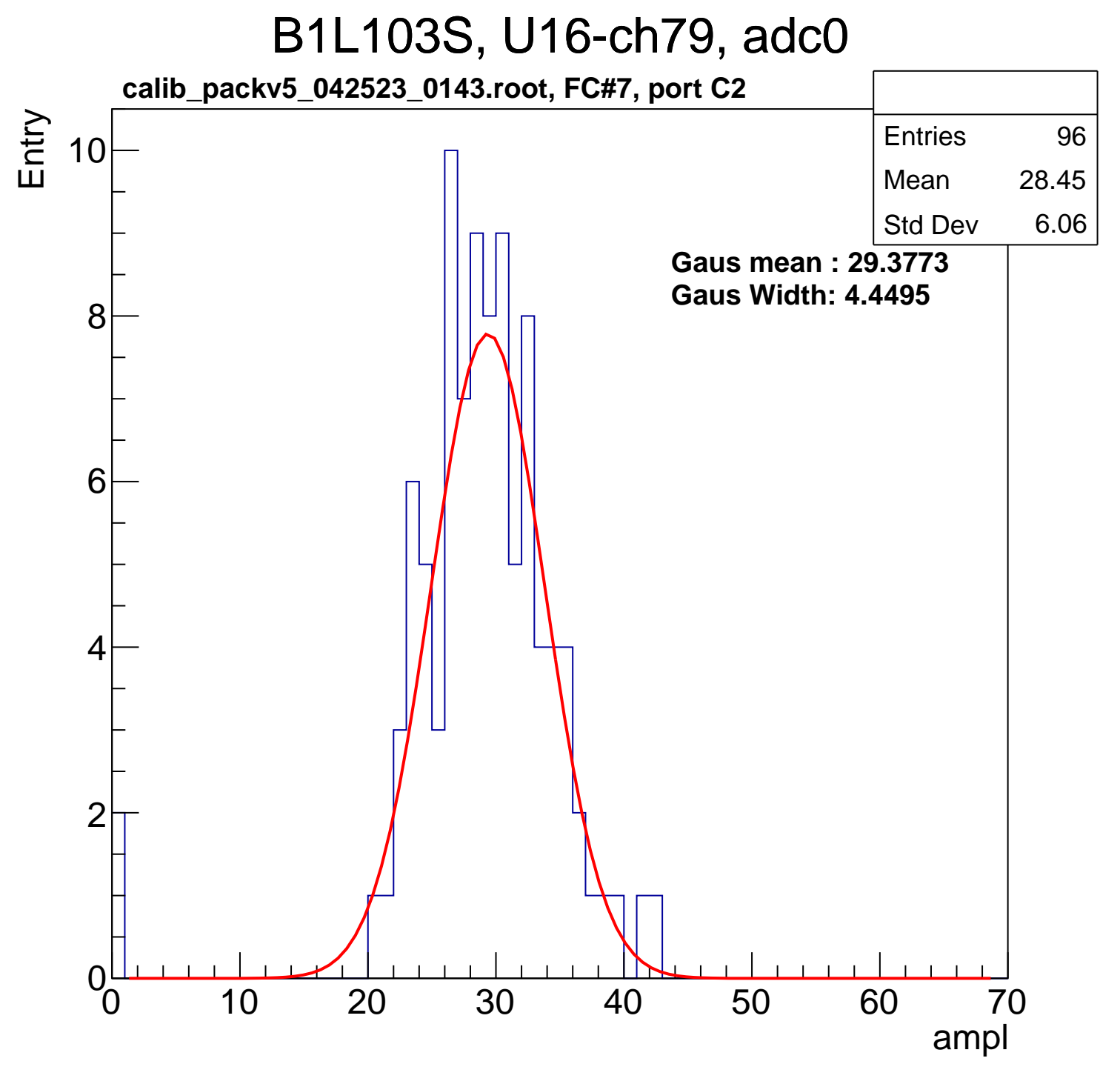
**Gaus Width: 4.4495**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U16-ch79, adc1

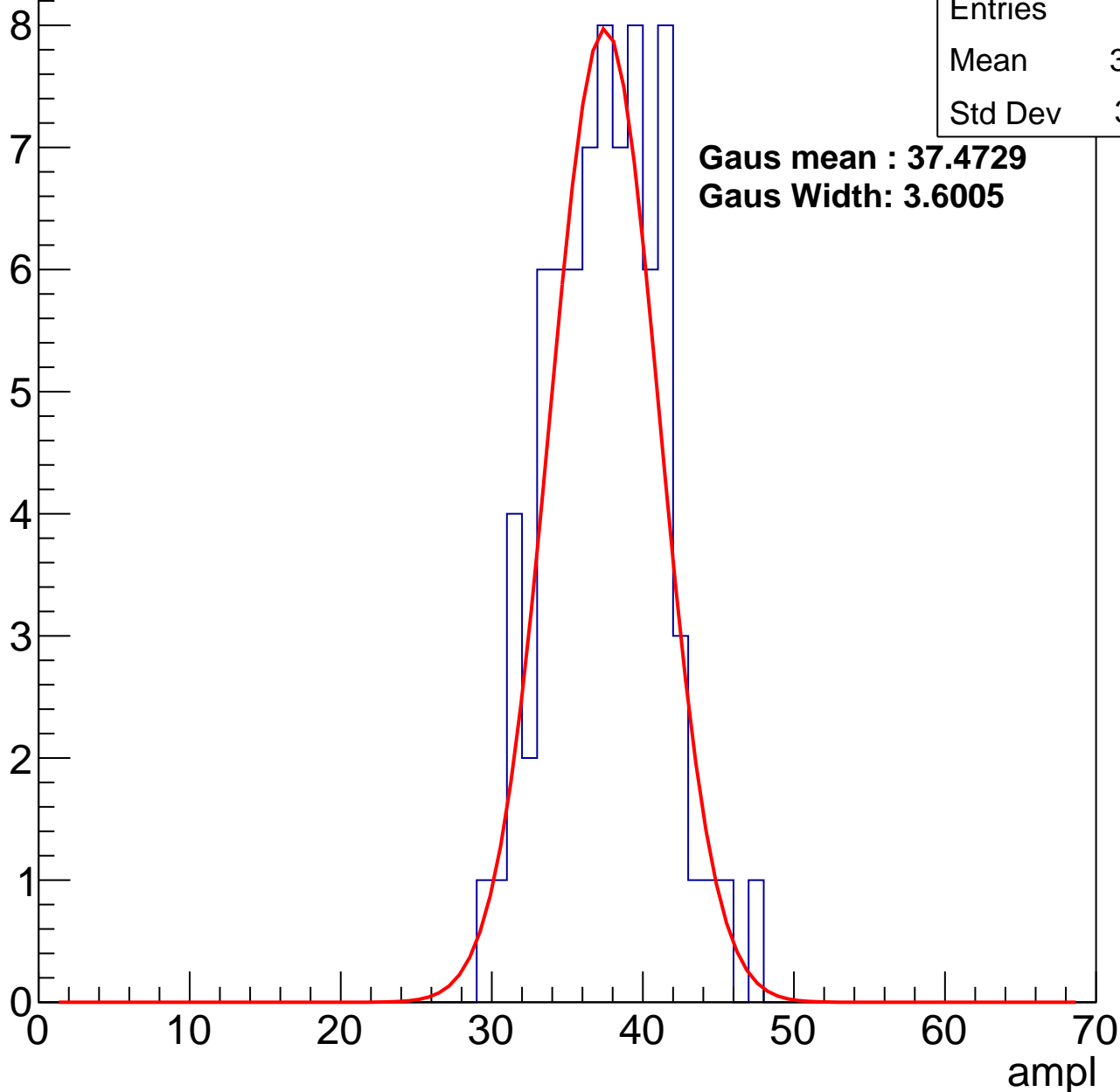
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	37.12
Std Dev	3.661

**Gaus mean : 37.4729**

**Gaus Width: 3.6005**



# B1L103S, U16-ch79, adc2

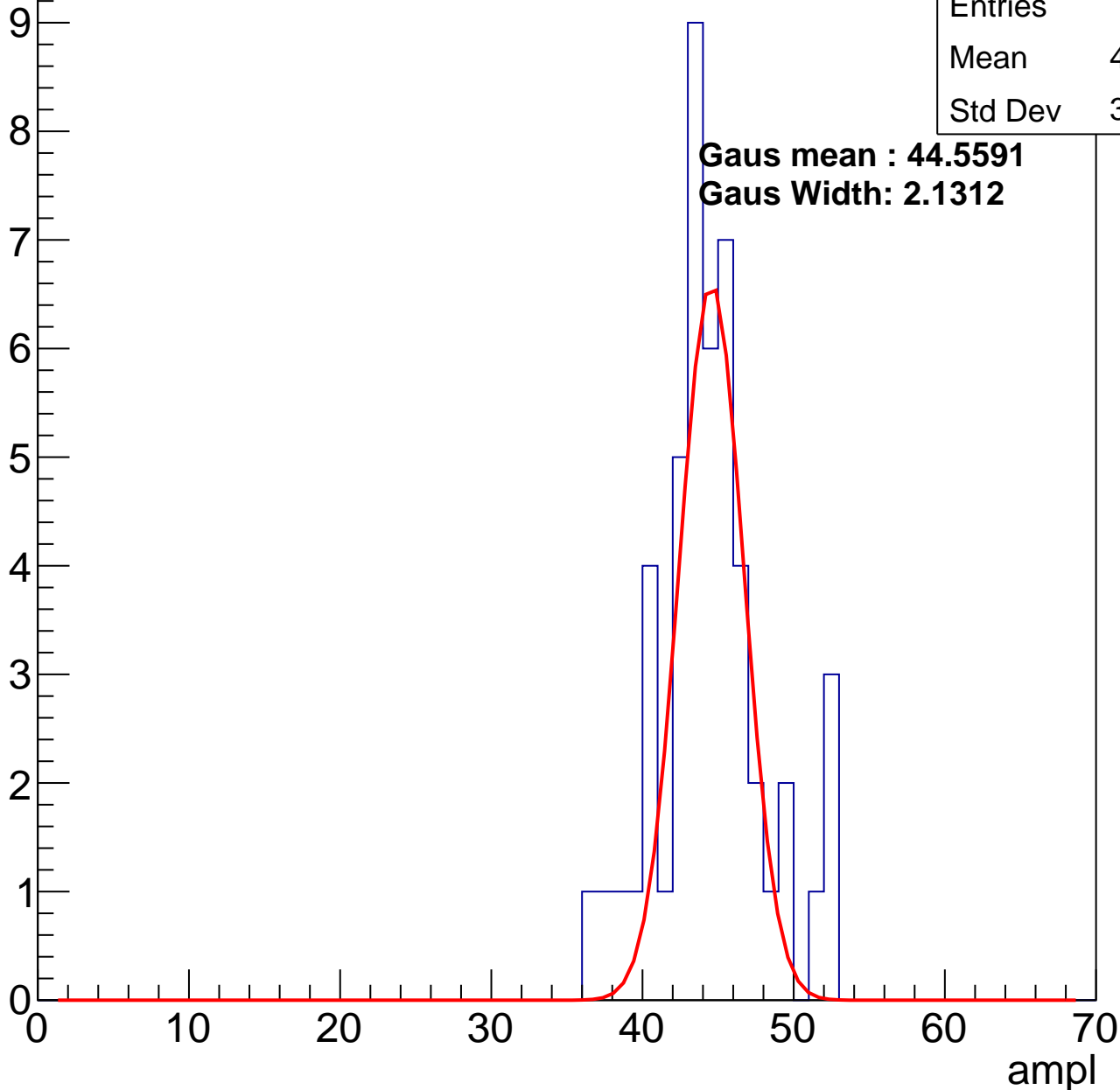
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	44.04
Std Dev	3.568

**Gaus mean : 44.5591**

**Gaus Width: 2.1312**

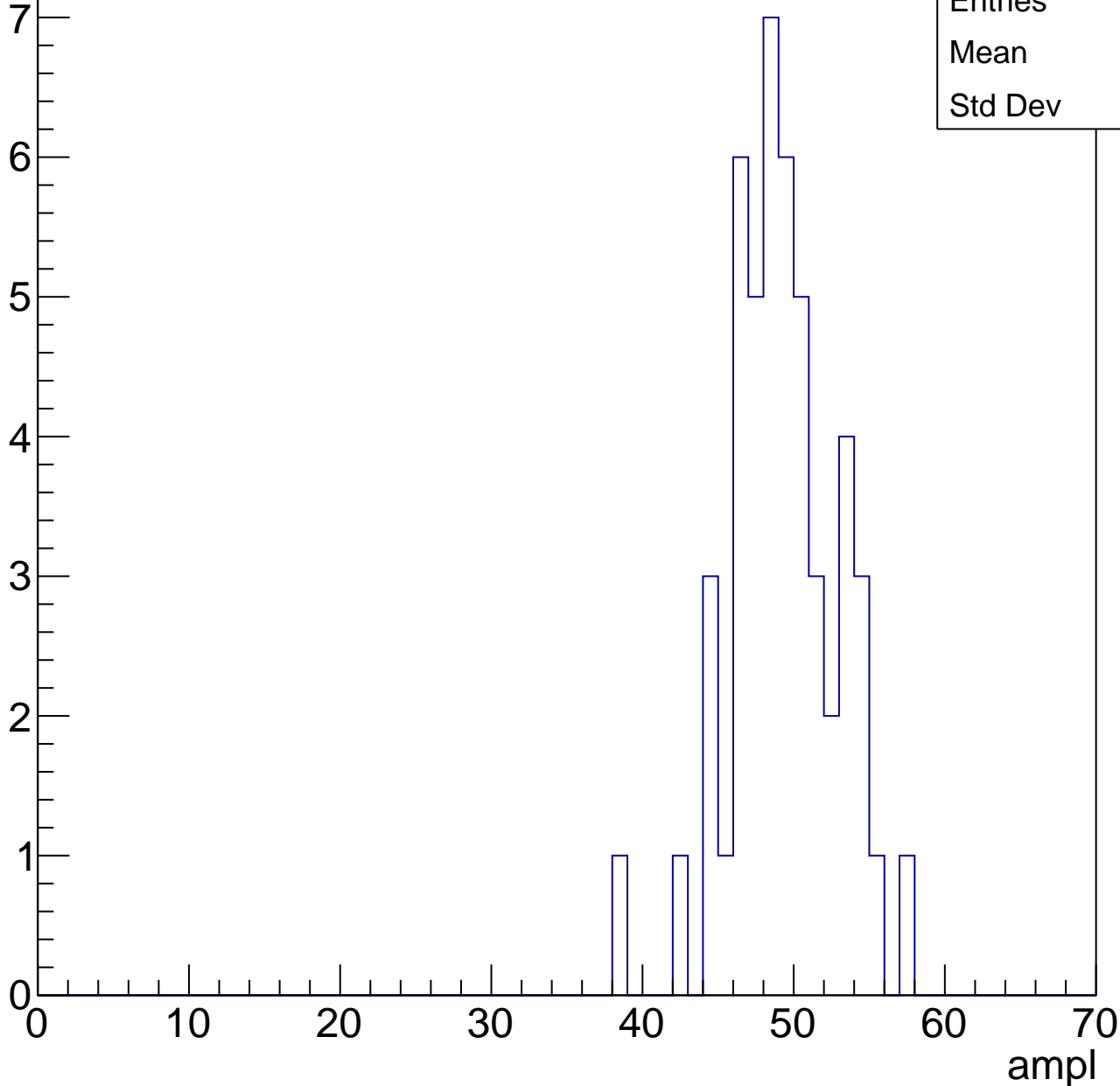


# B1L103S, U16-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	48.8
Std Dev	3.54

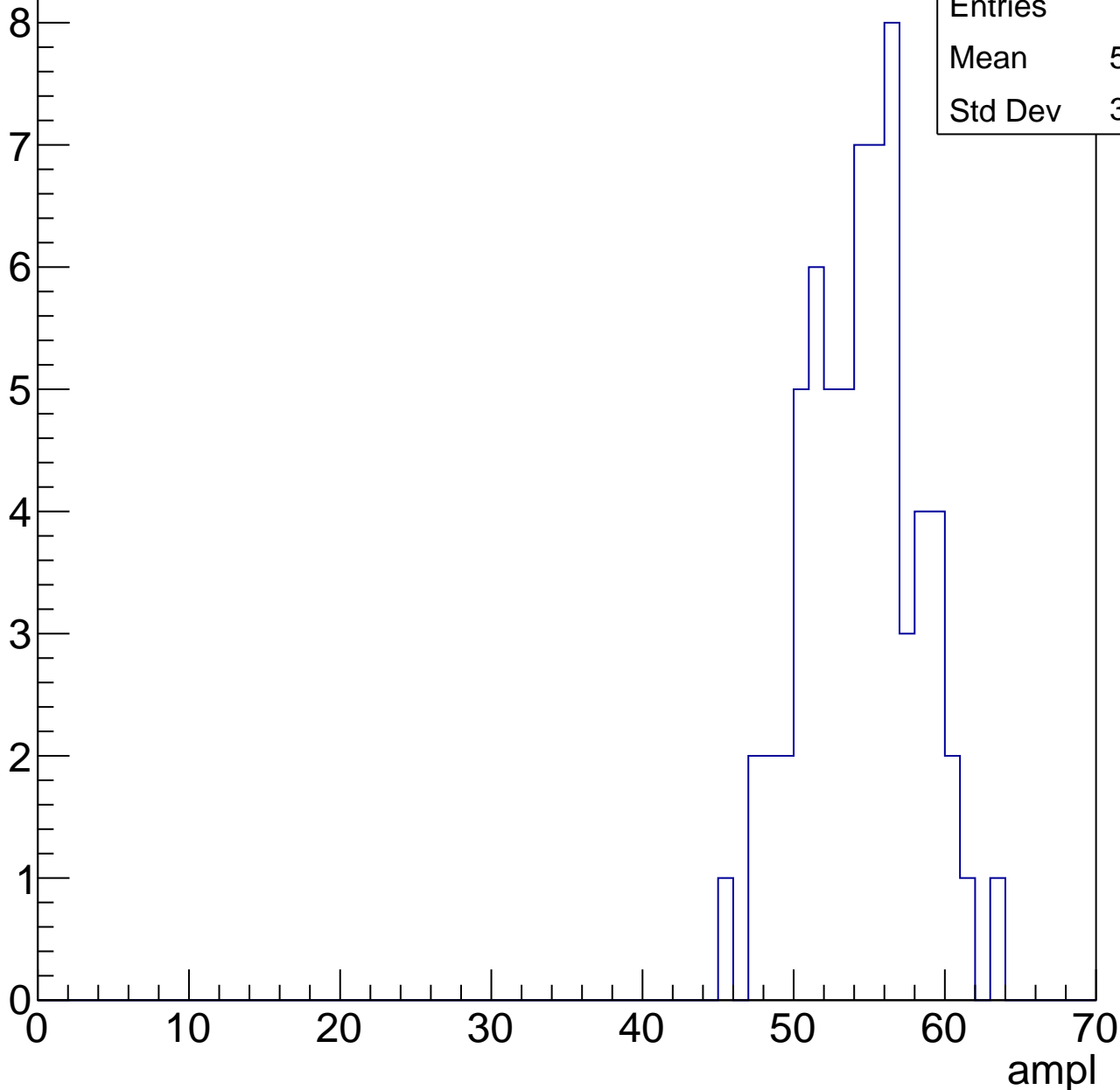


# B1L103S, U16-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

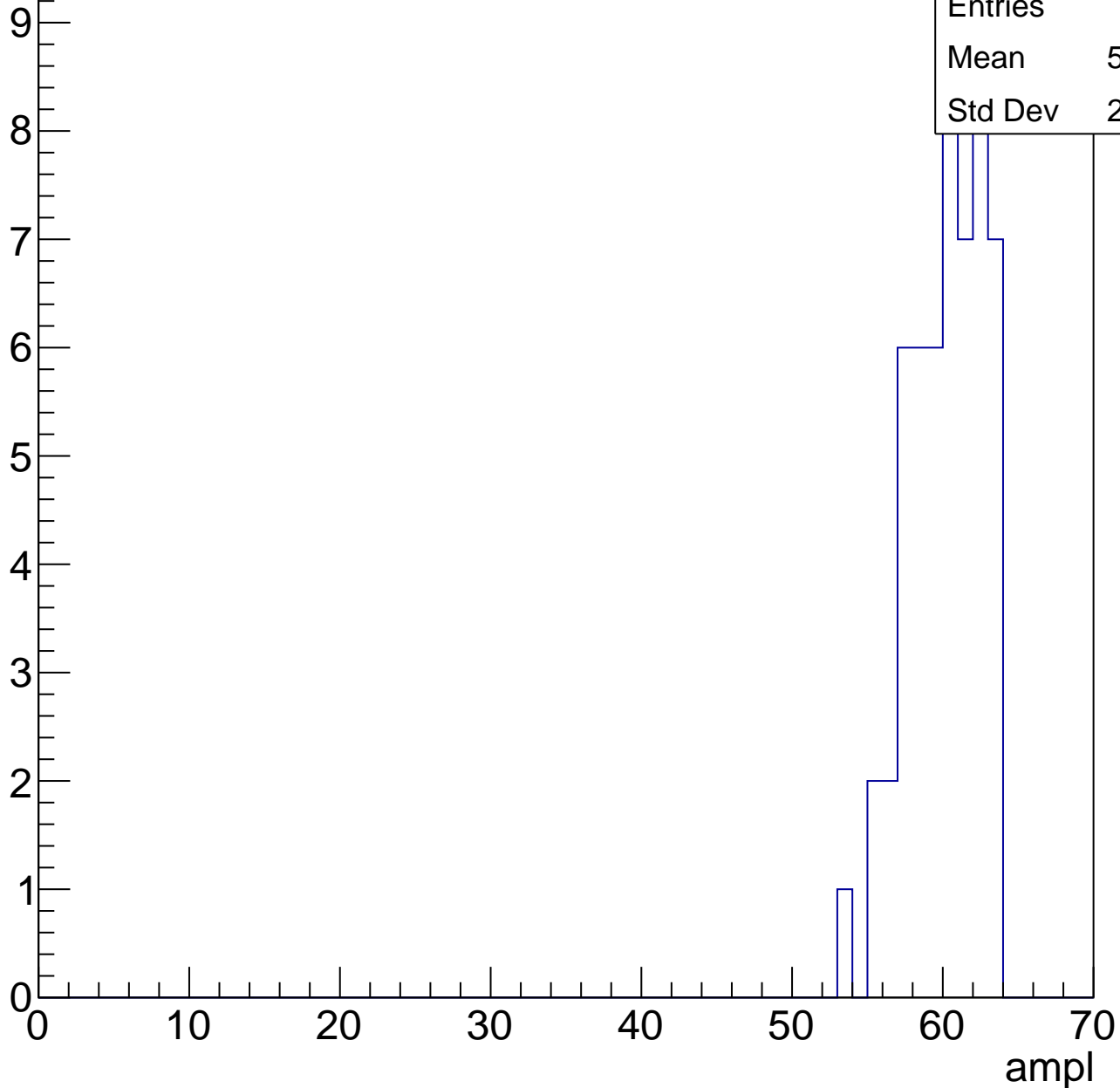
Entries	65
Mean	53.97
Std Dev	3.704



# B1L103S, U16-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

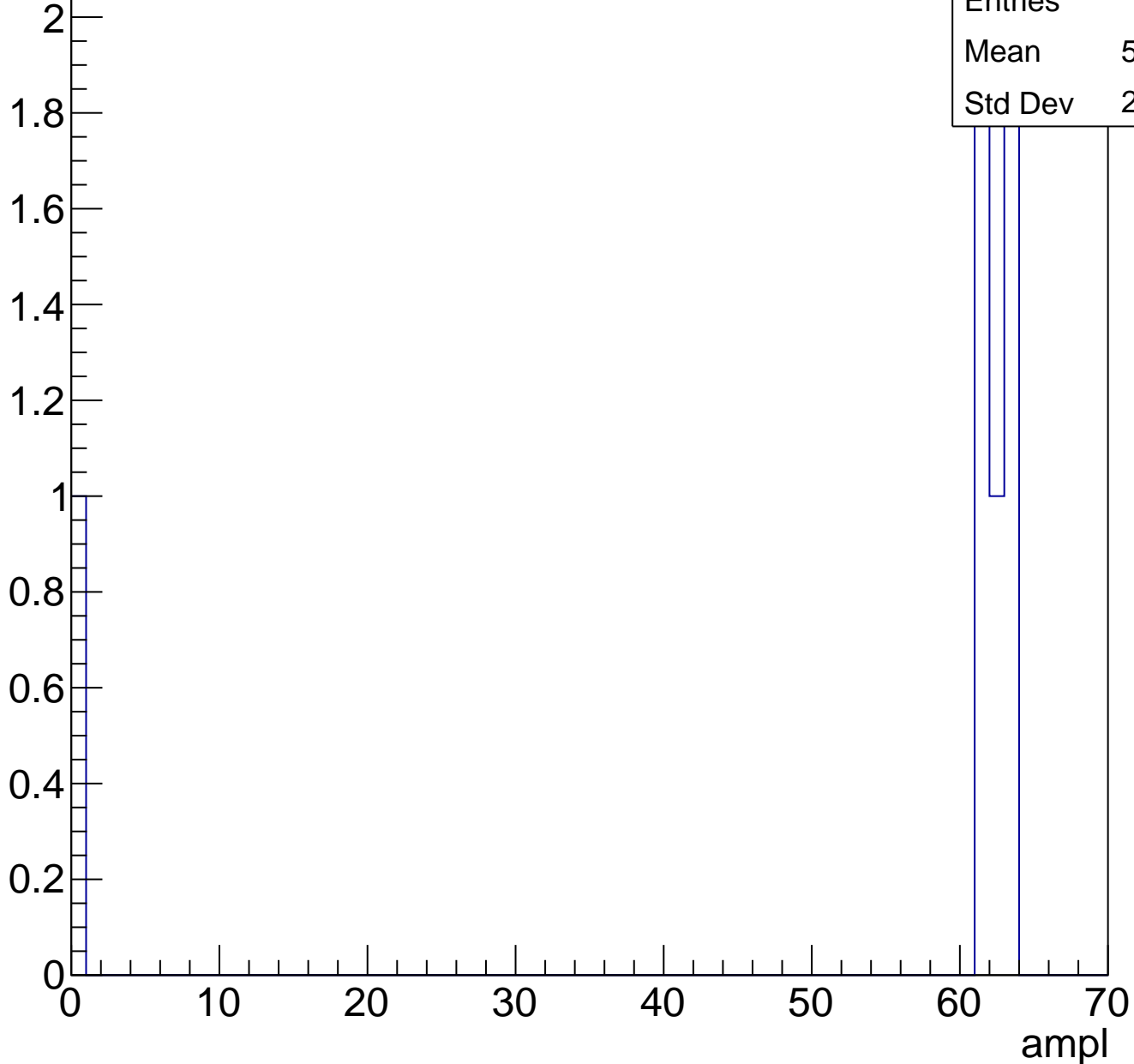
Entry



# B1L103S, U16-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch80, adc0

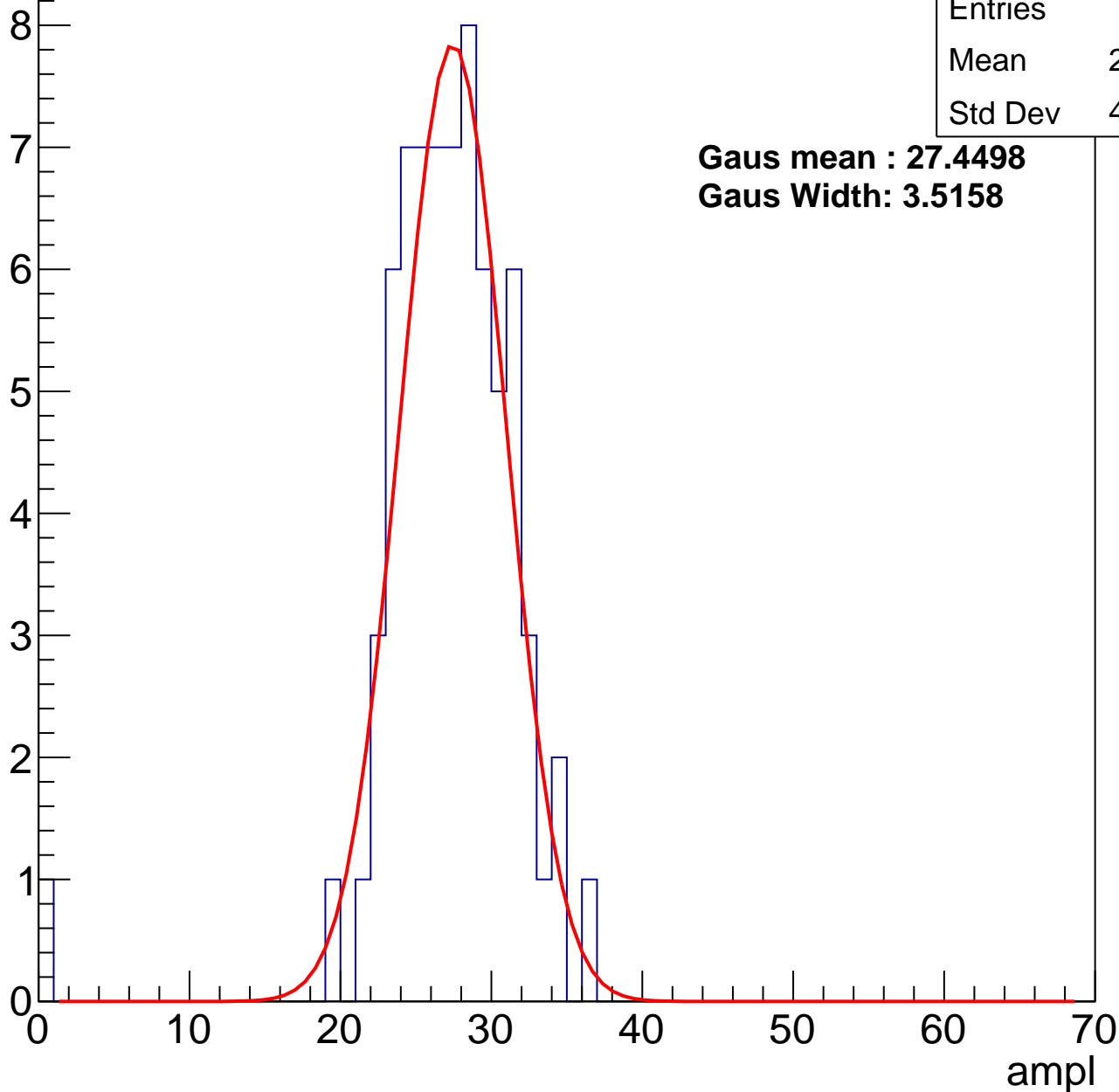
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	26.74
Std Dev	4.649

**Gaus mean : 27.4498**

**Gaus Width: 3.5158**



# B1L103S, U16-ch80, adc1

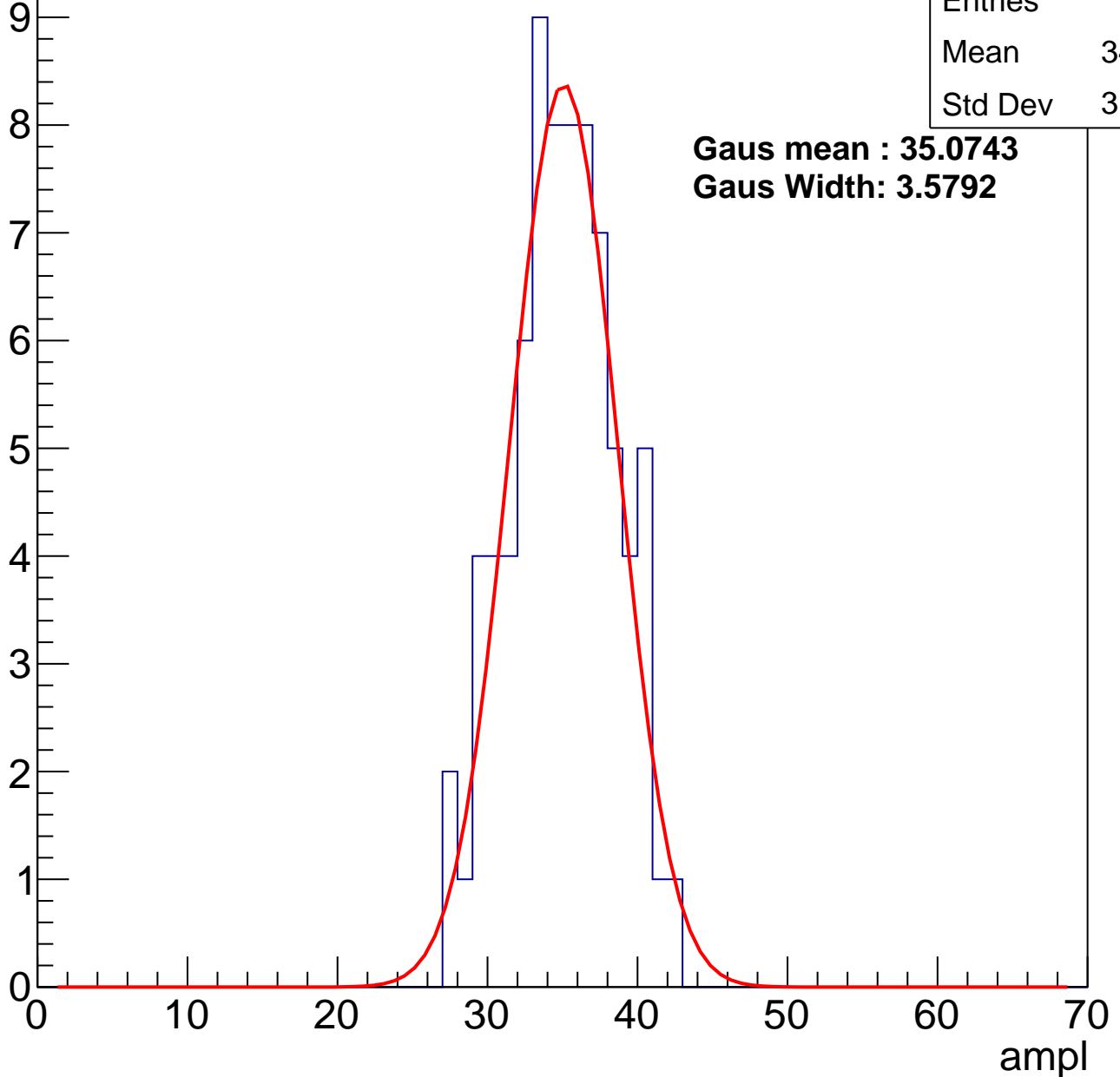
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	34.53
Std Dev	3.459

**Gaus mean : 35.0743**

**Gaus Width: 3.5792**

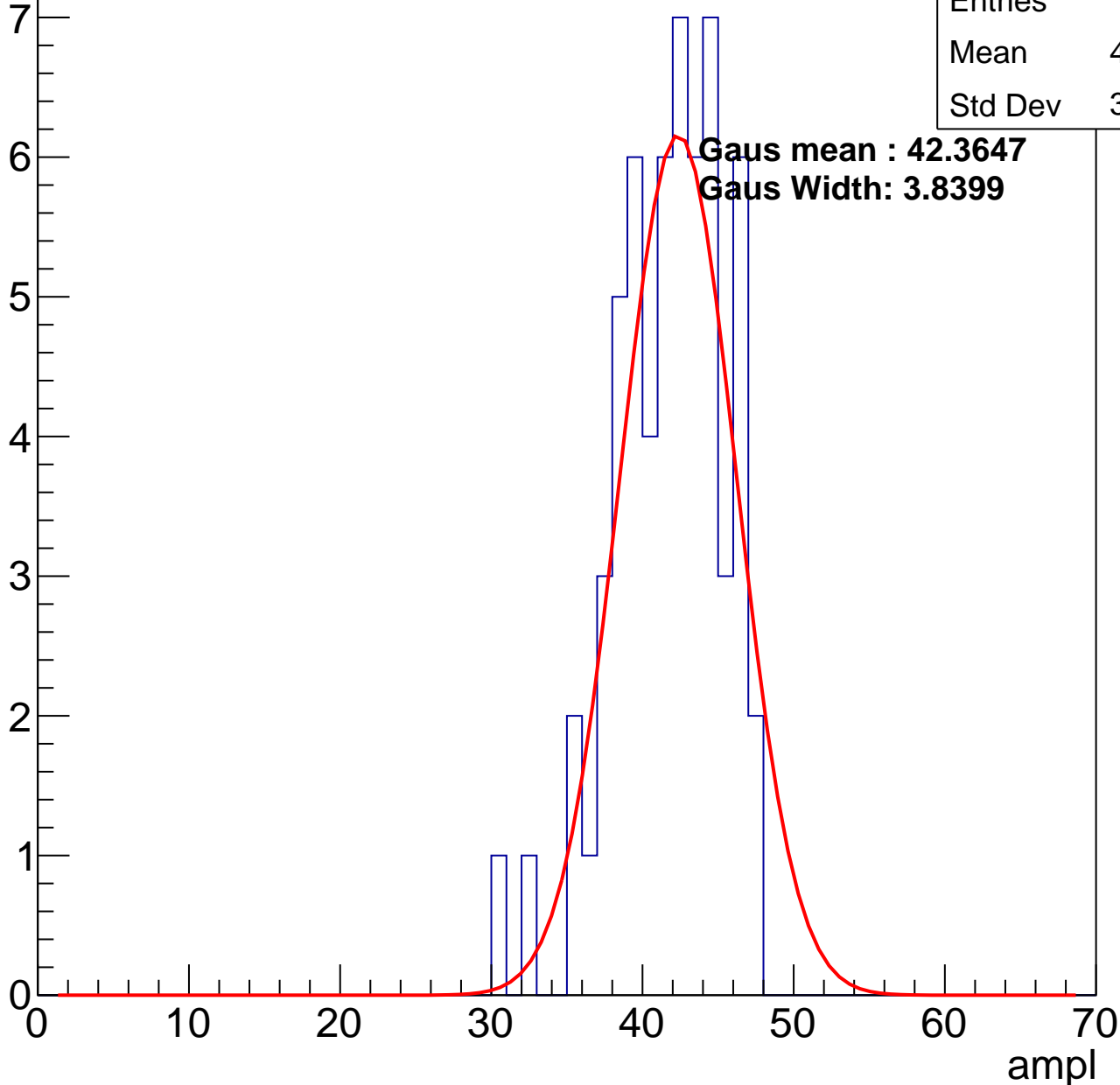


# B1L103S, U16-ch80, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	41.23
Std Dev	3.607

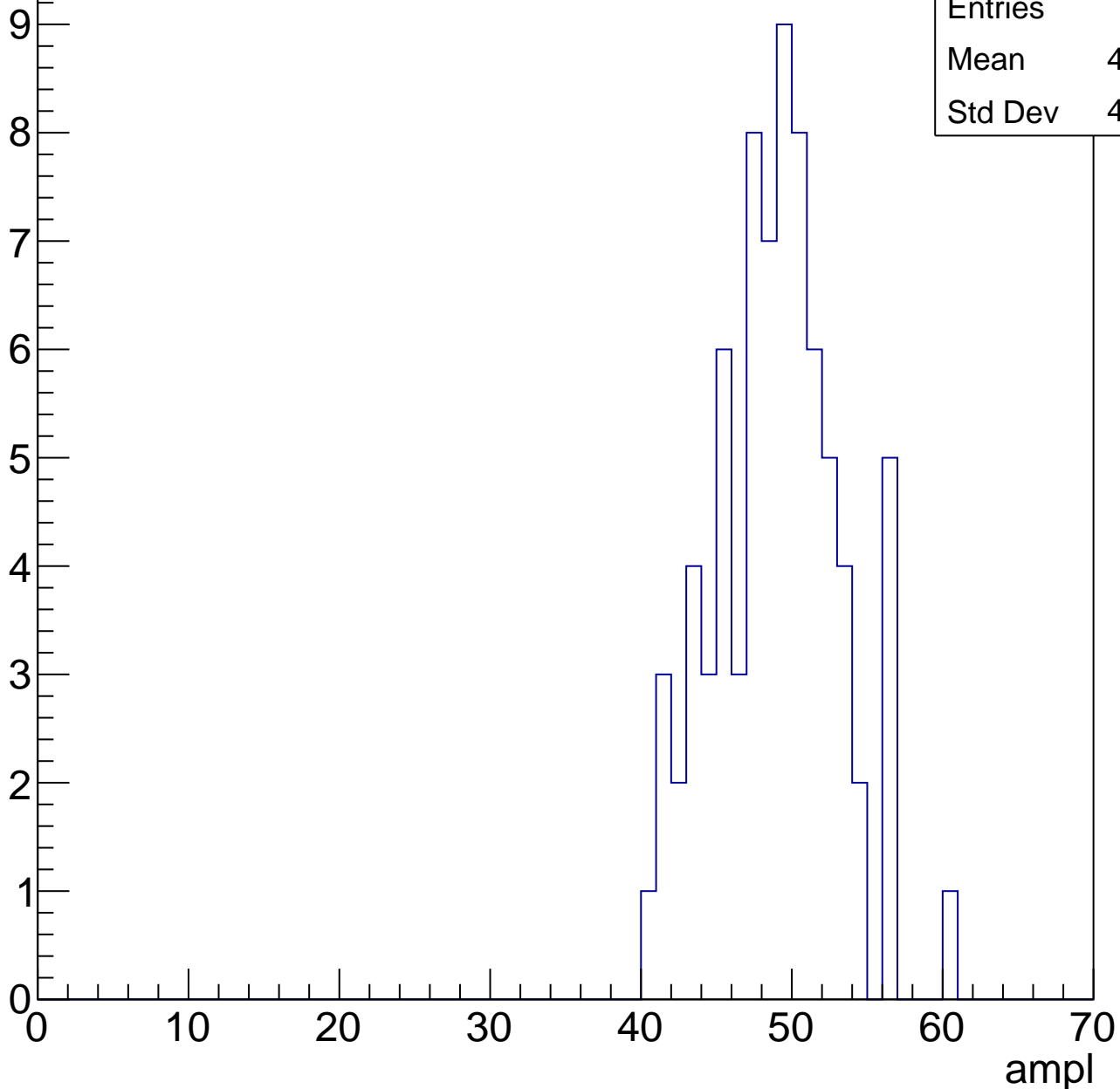


# B1L103S, U16-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	48.55
Std Dev	4.098

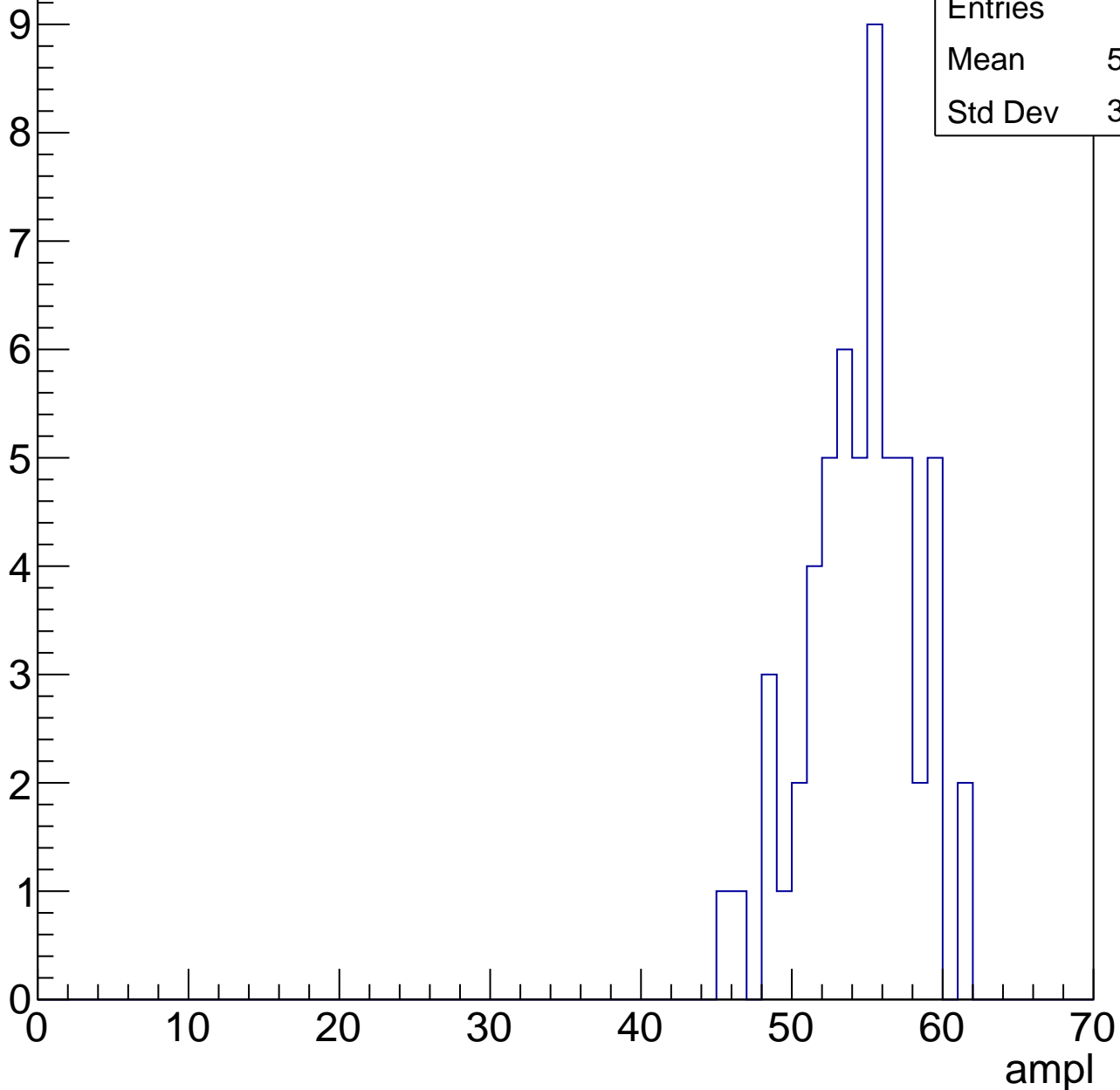


# B1L103S, U16-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	54.09
Std Dev	3.537

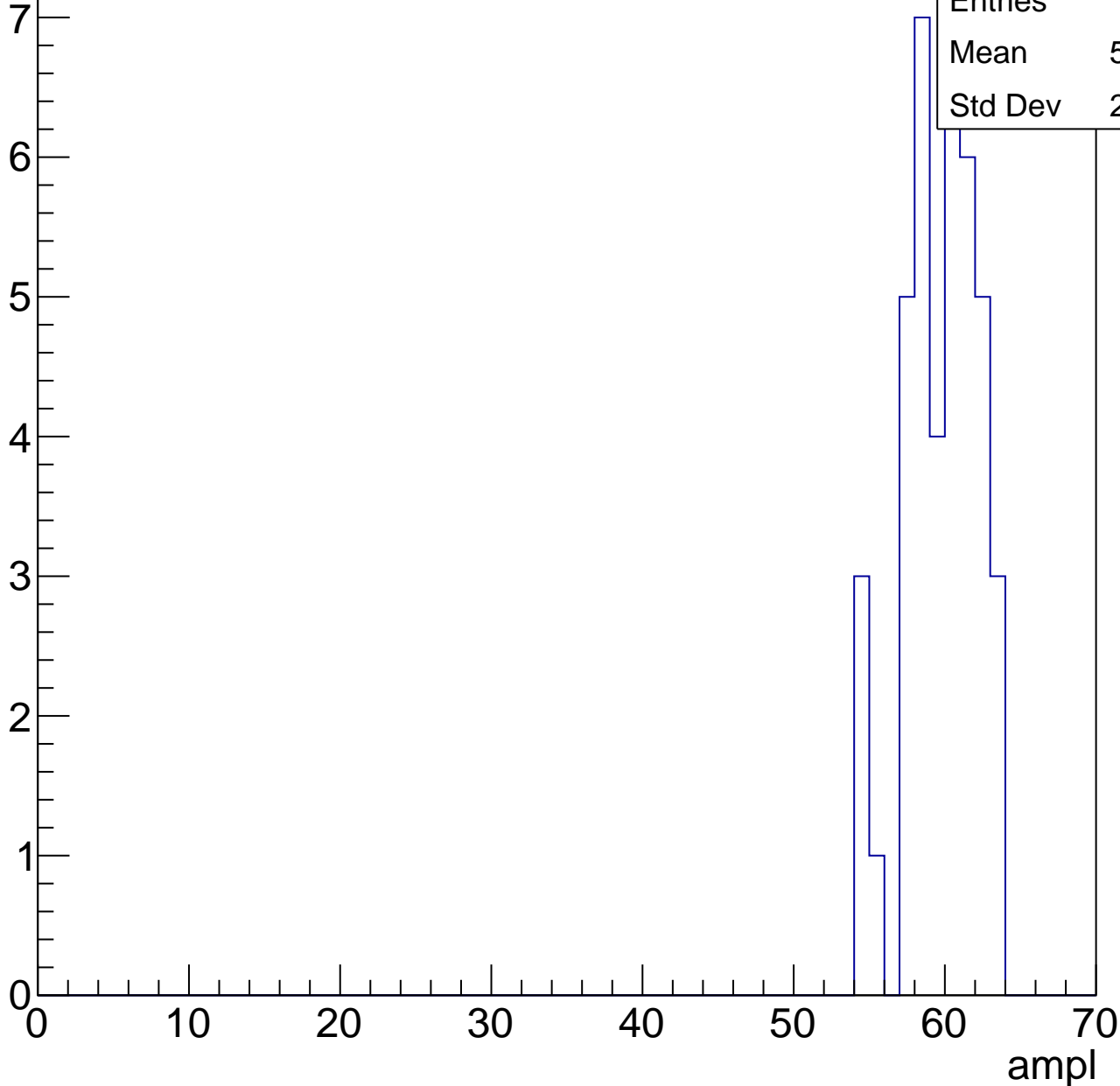


# B1L103S, U16-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	41
Mean	59.24
Std Dev	2.417

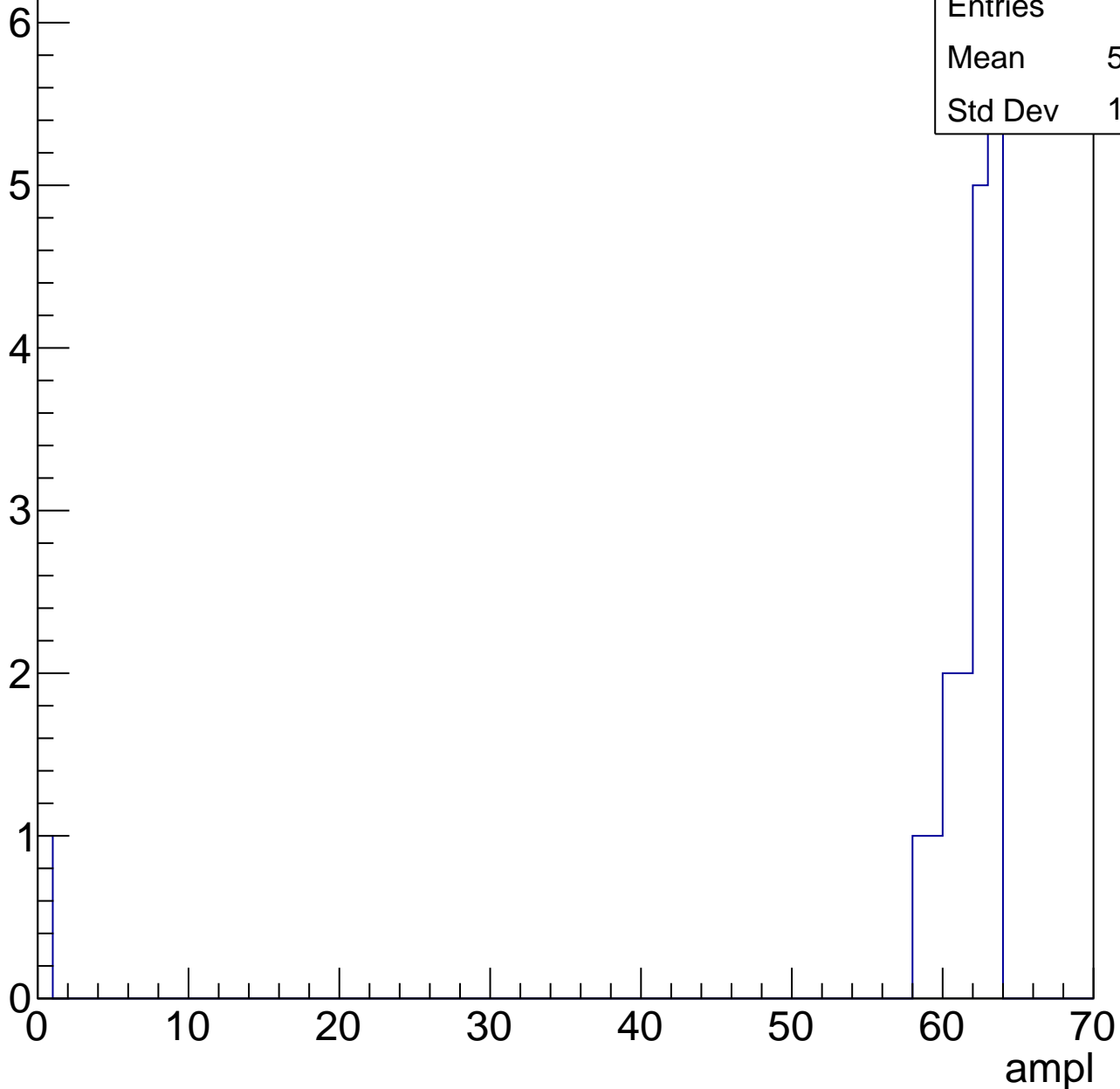


# B1L103S, U16-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	18
Mean	58.17
Std Dev	14.18





# B1L103S, U16-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	63
Std Dev	0

# B1L103S, U16-ch81, adc0

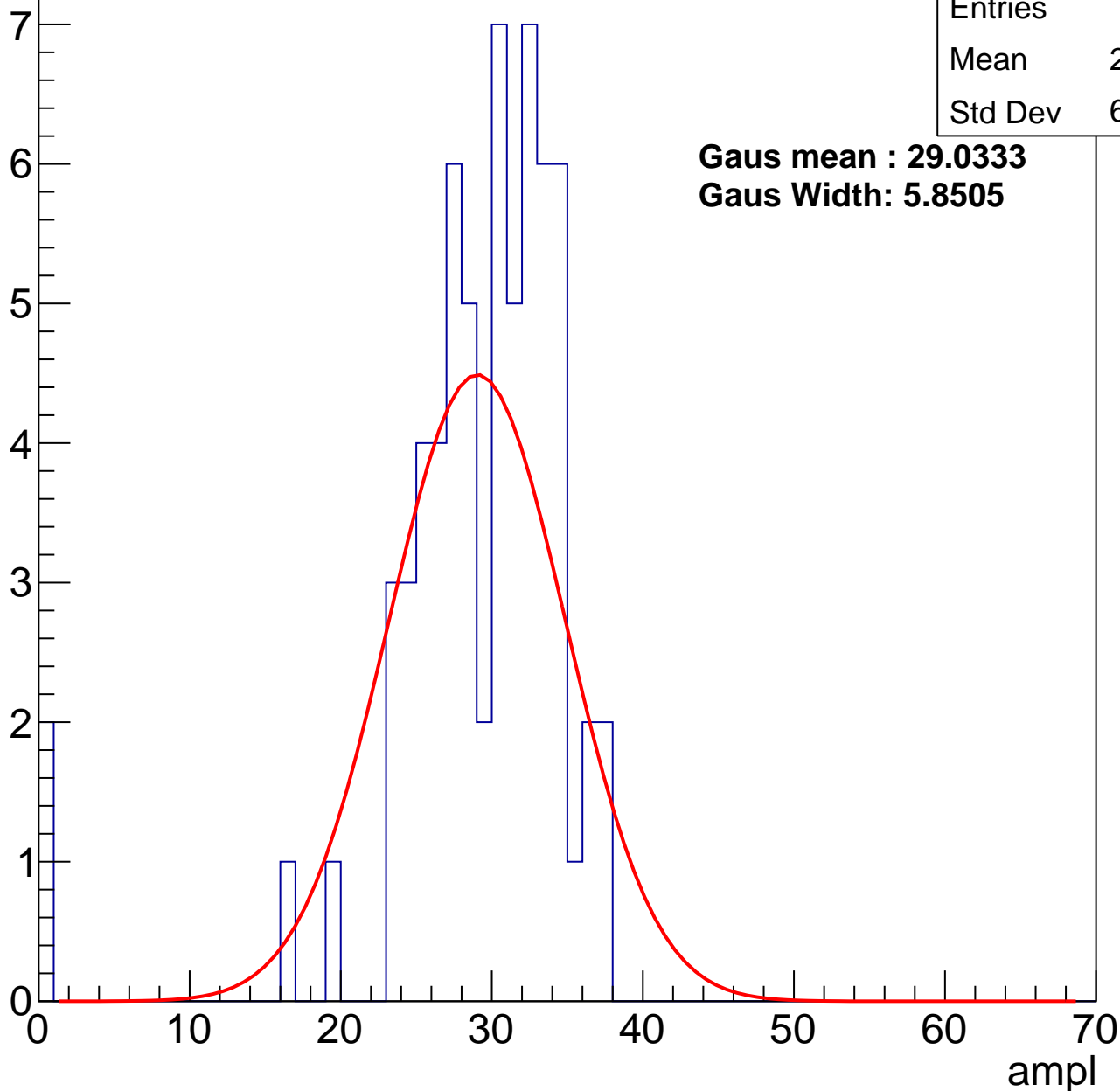
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	28.54
Std Dev	6.518

**Gaus mean : 29.0333**

**Gaus Width: 5.8505**



# B1L103S, U16-ch81, adc1

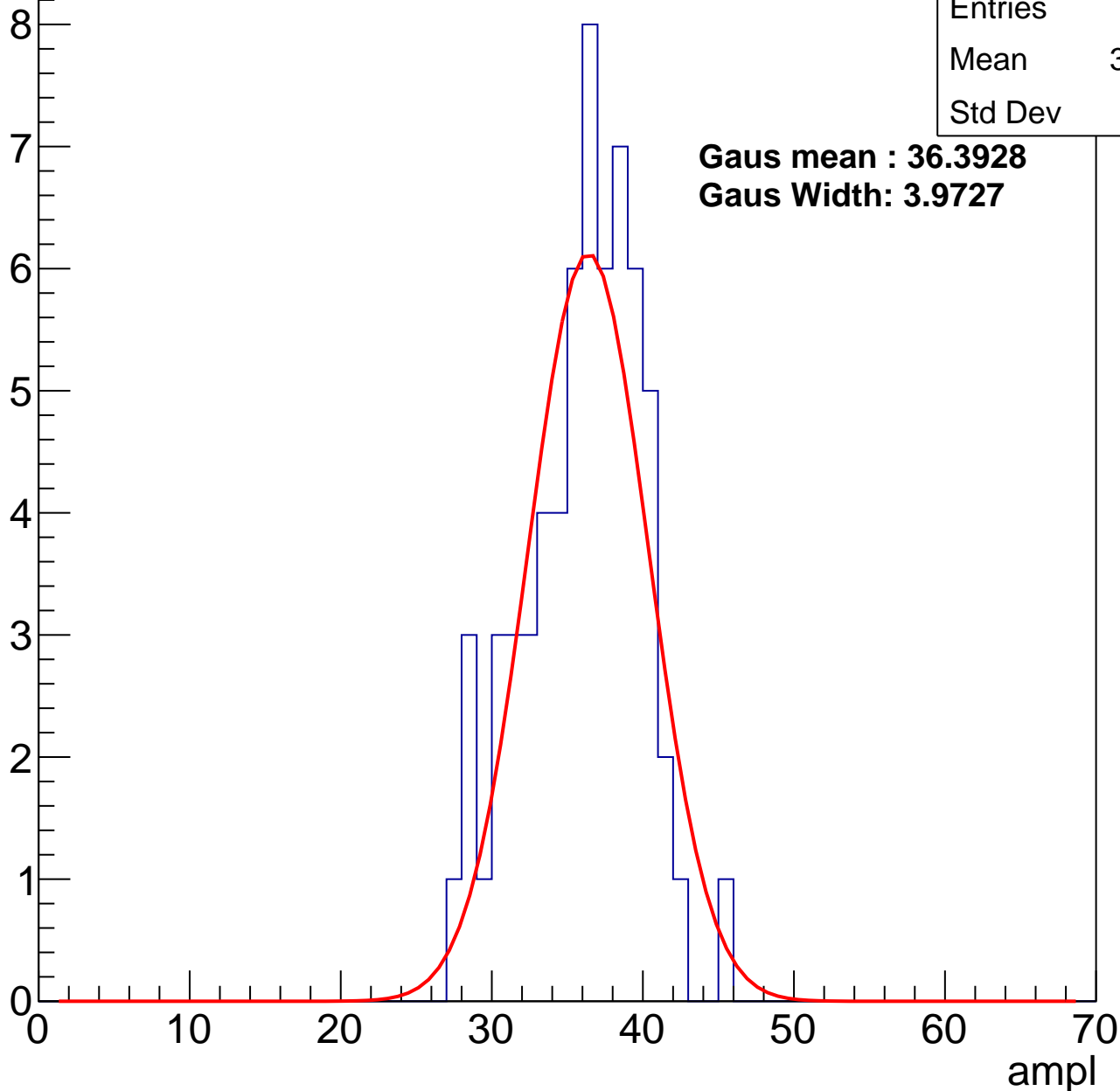
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	35.56
Std Dev	3.82

**Gaus mean : 36.3928**

**Gaus Width: 3.9727**



# B1L103S, U16-ch81, adc2

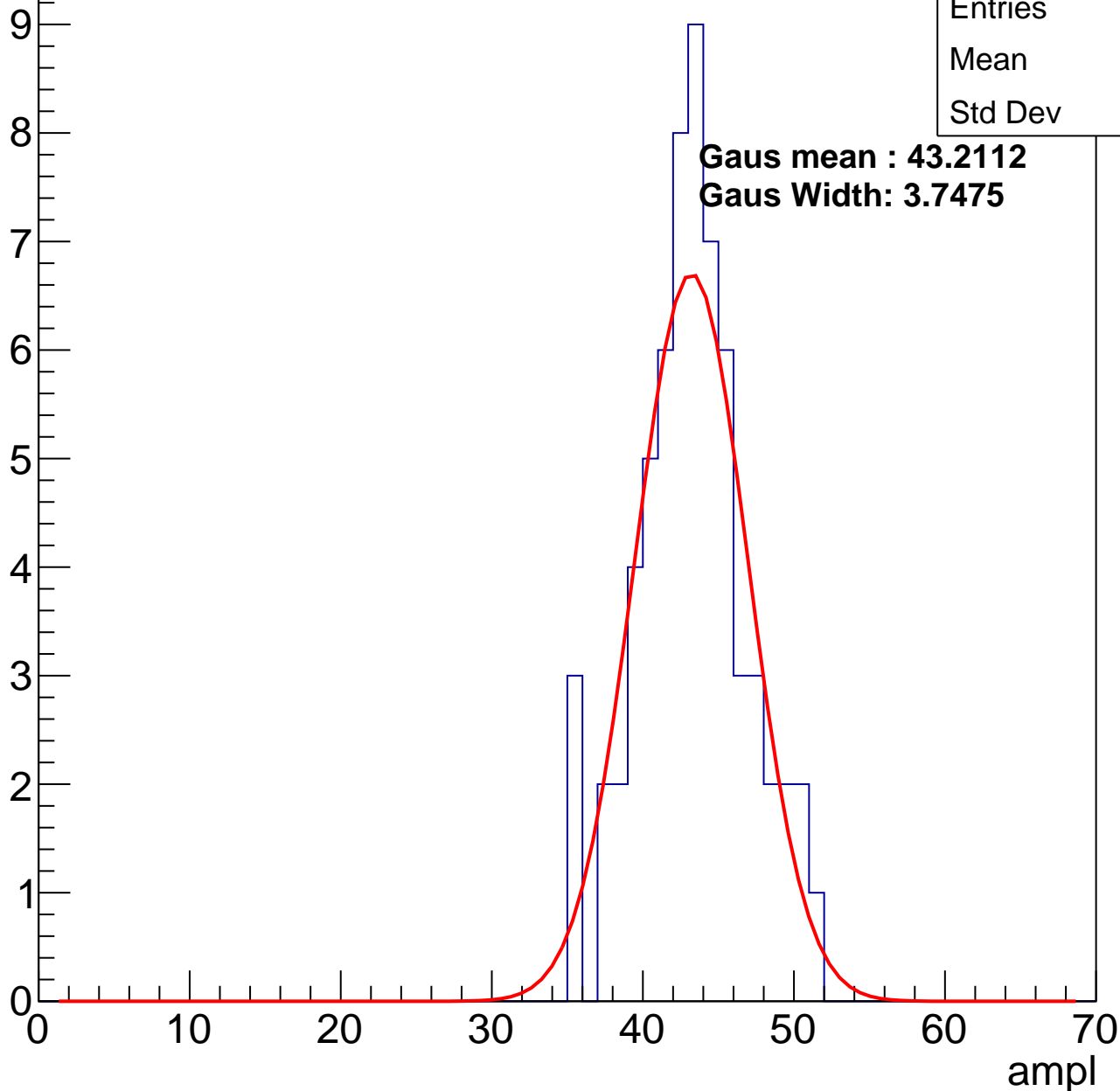
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	42.8
Std Dev	3.6

**Gaus mean : 43.2112**

**Gaus Width: 3.7475**

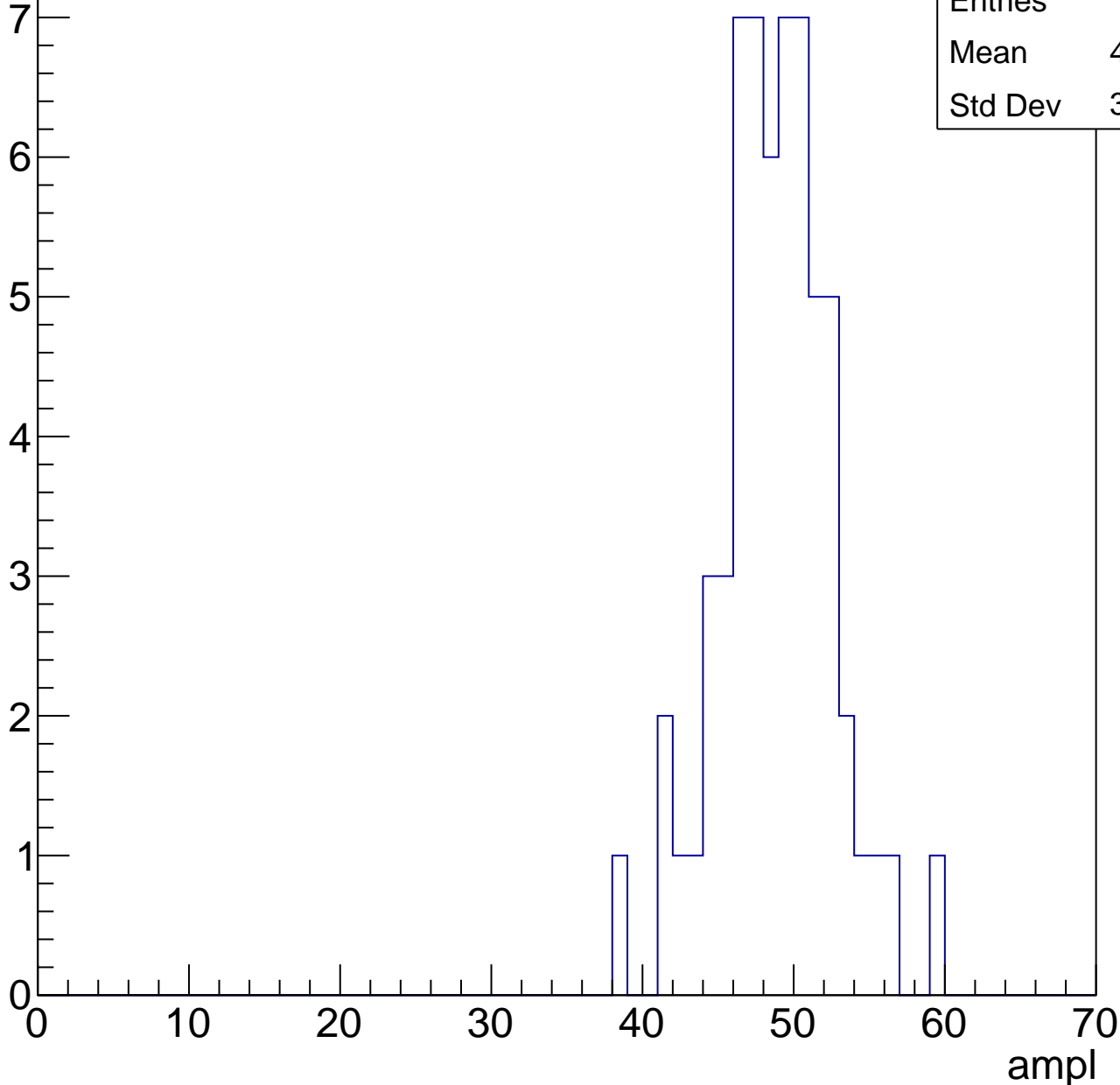


# B1L103S, U16-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	48.34
Std Dev	3.715

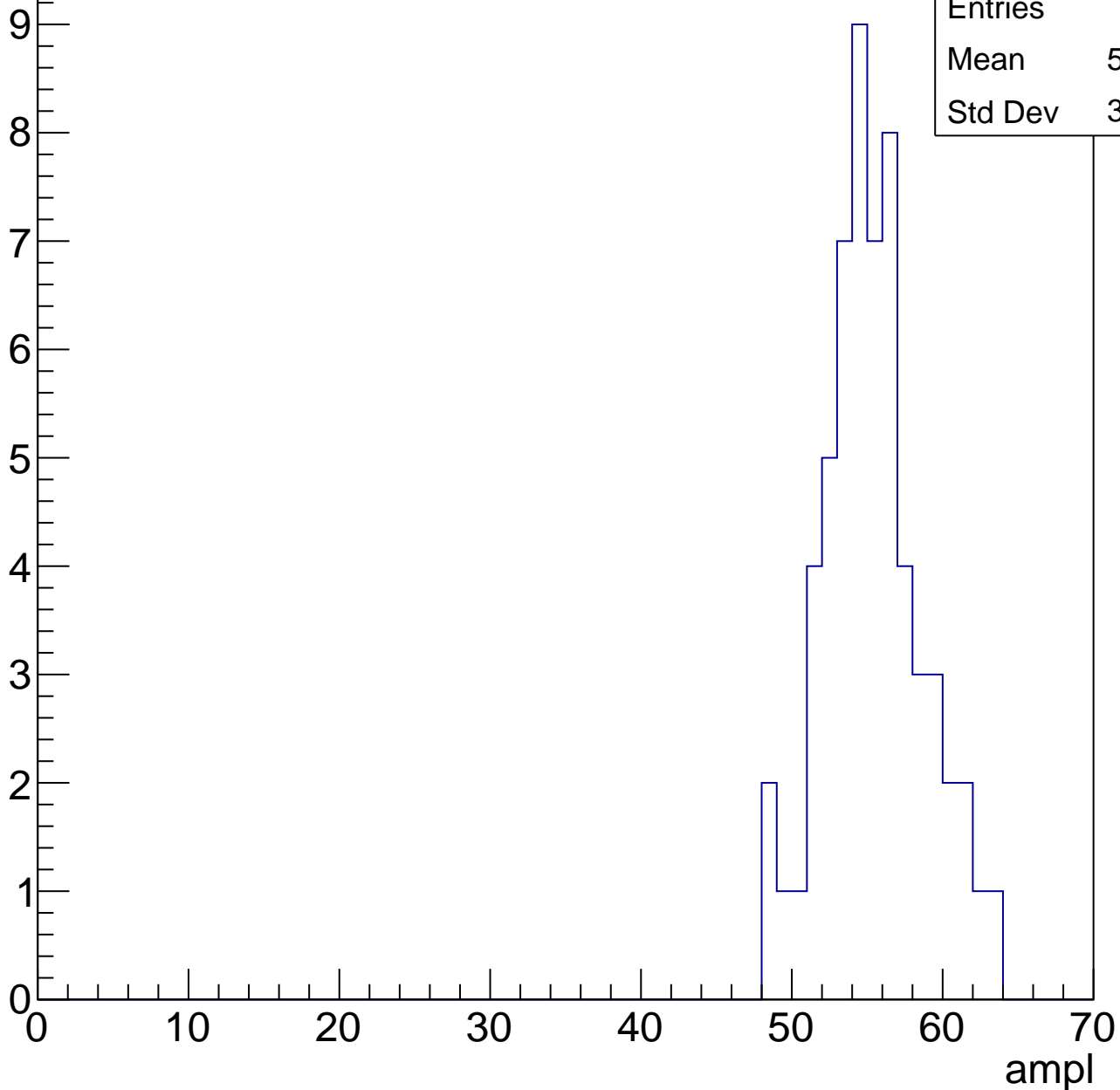


# B1L103S, U16-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

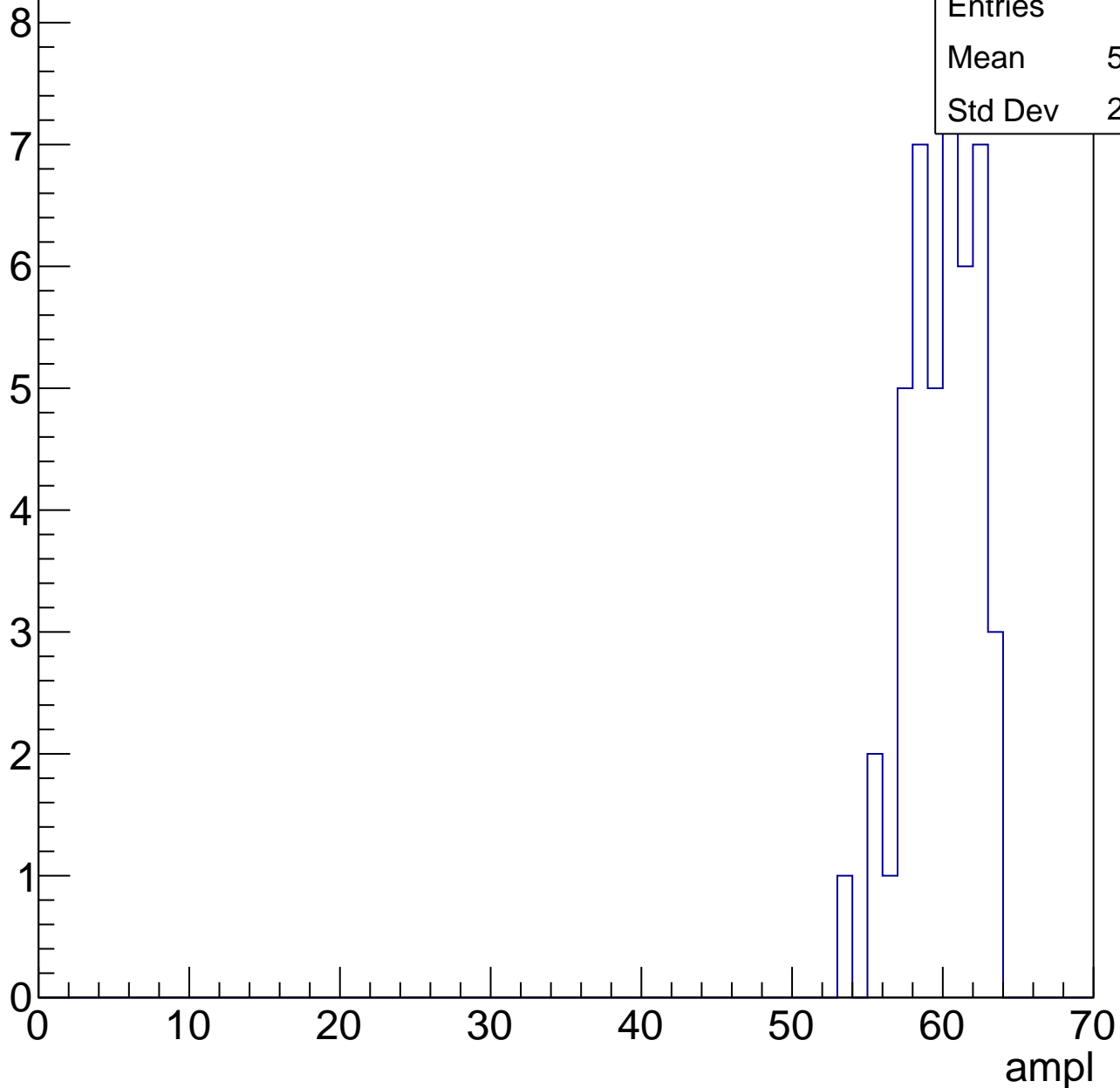
Entries	60
Mean	54.92
Std Dev	3.262



# B1L103S, U16-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



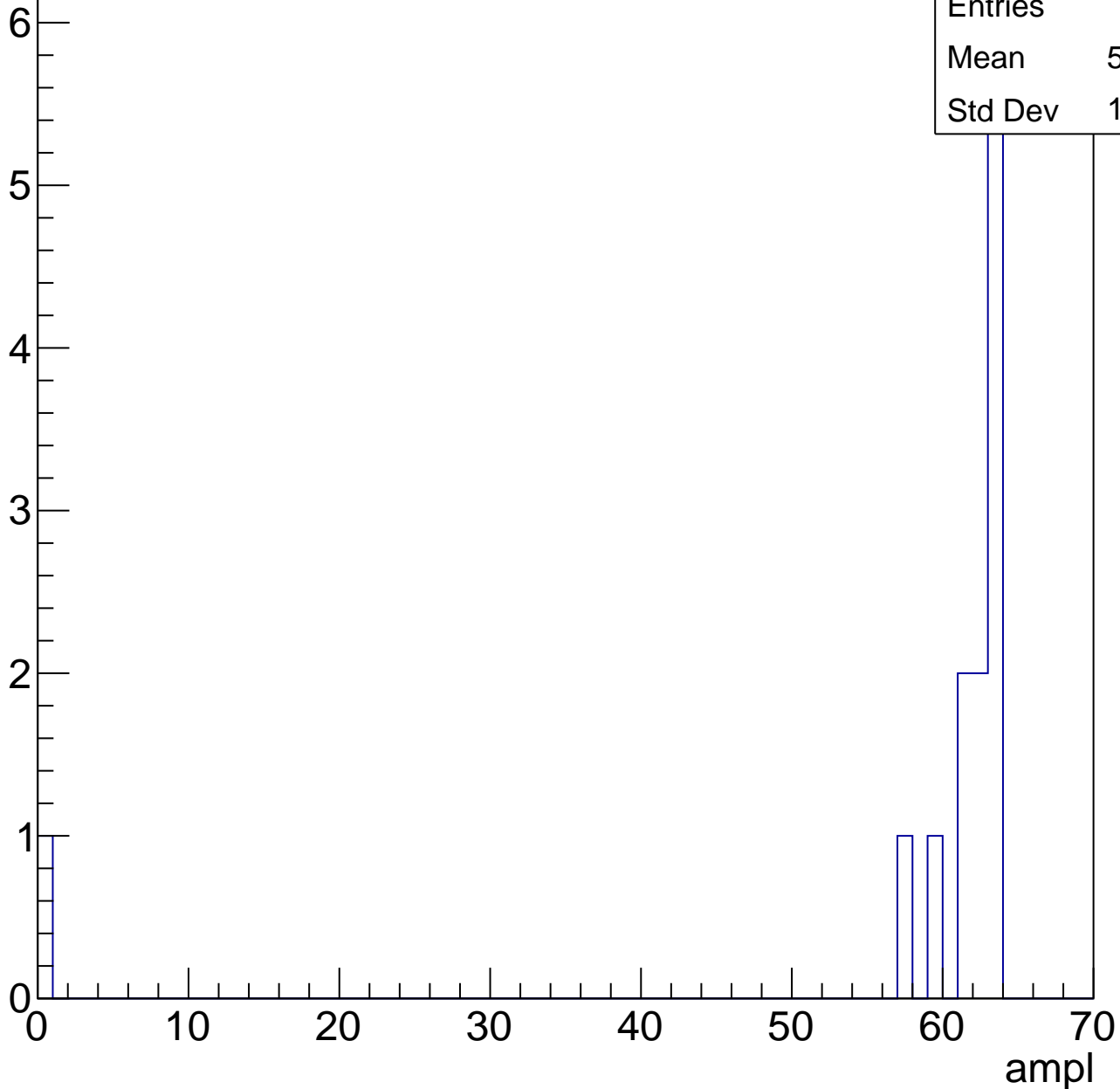
Entries	45
Mean	59.42
Std Dev	2.304

# B1L103S, U16-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	13
Mean	56.92
Std Dev	16.53





# B1L103S, U16-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U16-ch82, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	88
Mean	28.41
Std Dev	5.965

**Gaus mean : 31.0729**

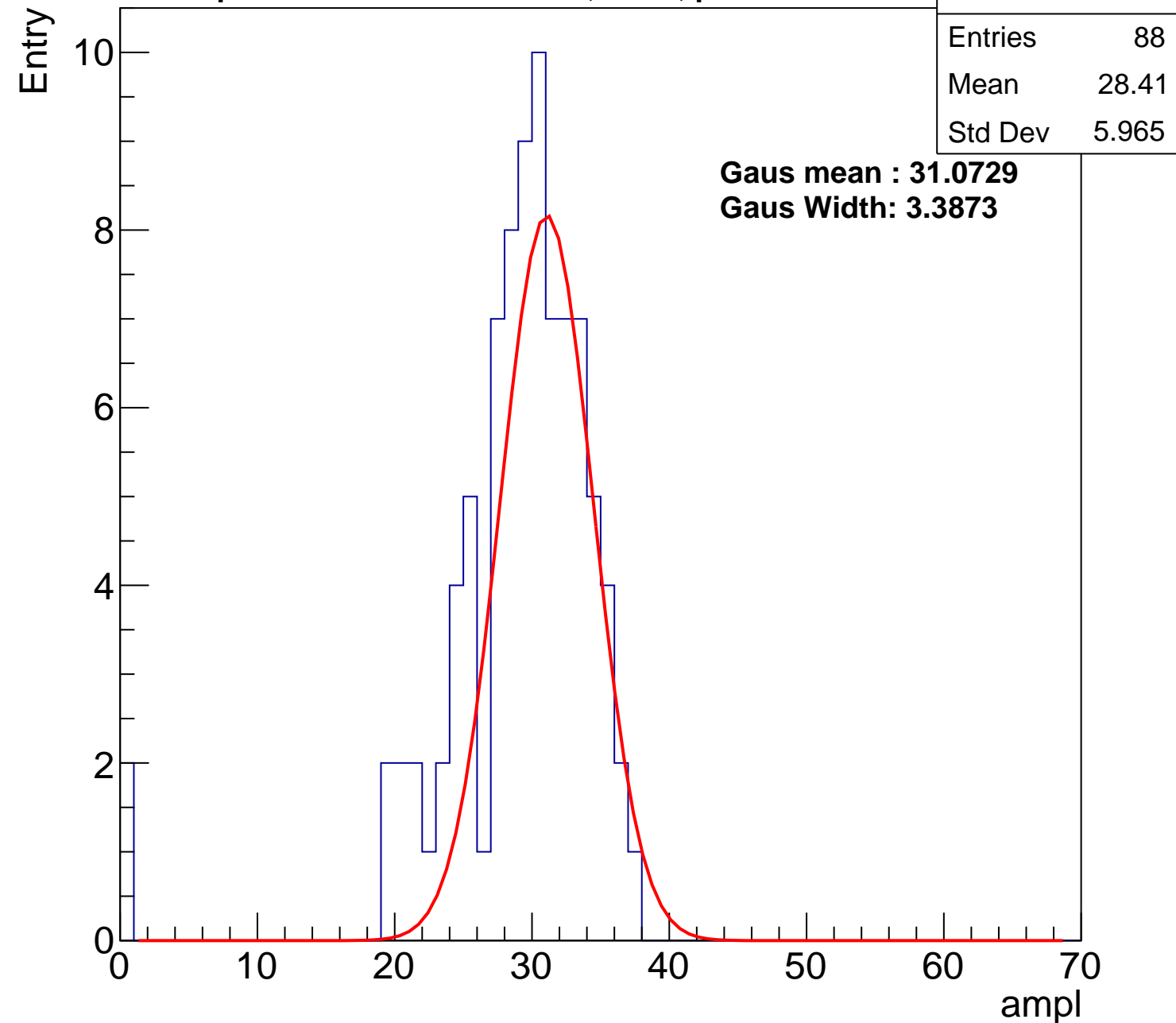
**Gaus Width: 3.3873**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U16-ch82, adc1

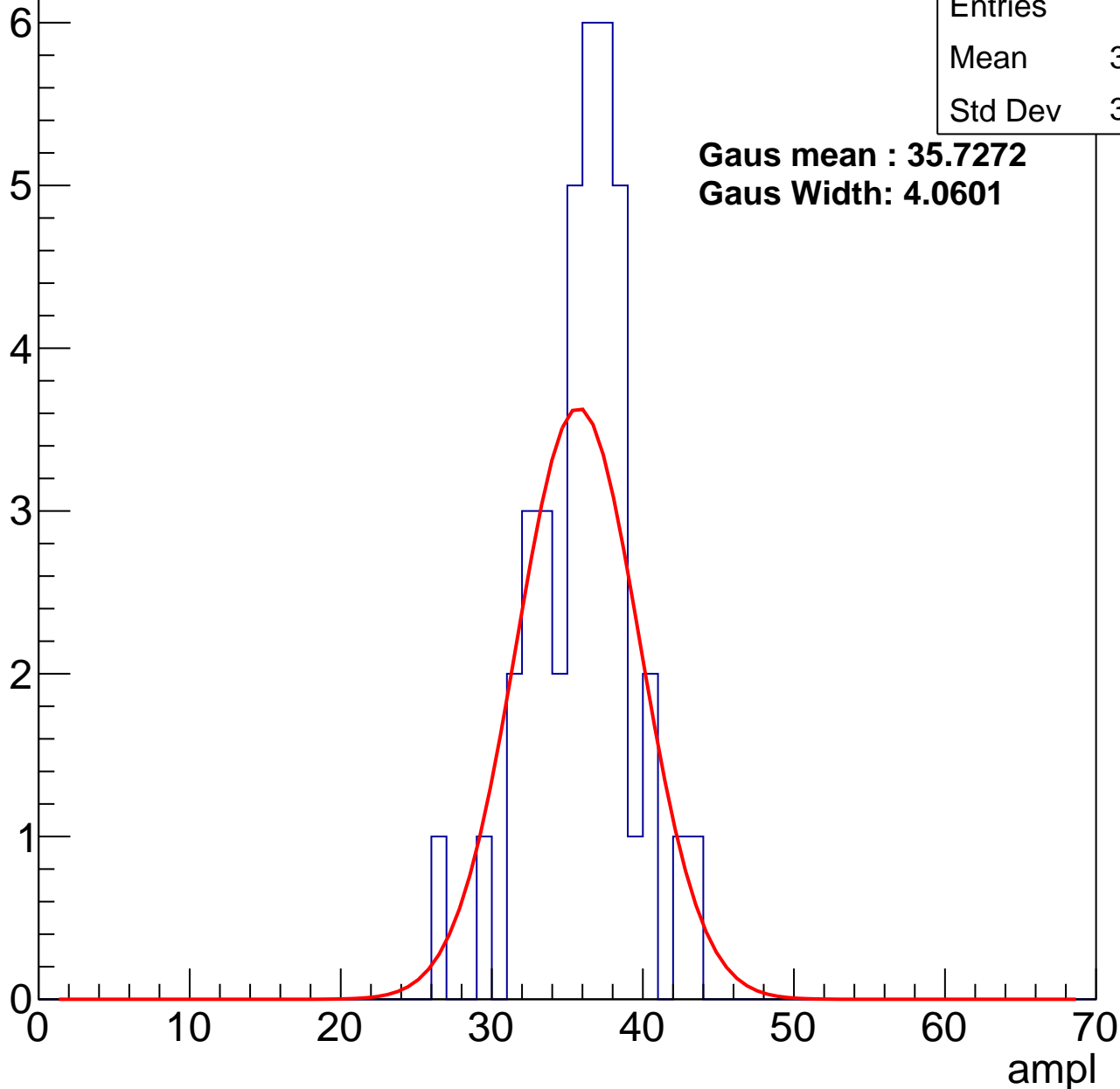
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	39
Mean	35.56
Std Dev	3.327

**Gaus mean : 35.7272**

**Gaus Width: 4.0601**



# B1L103S, U16-ch82, adc2

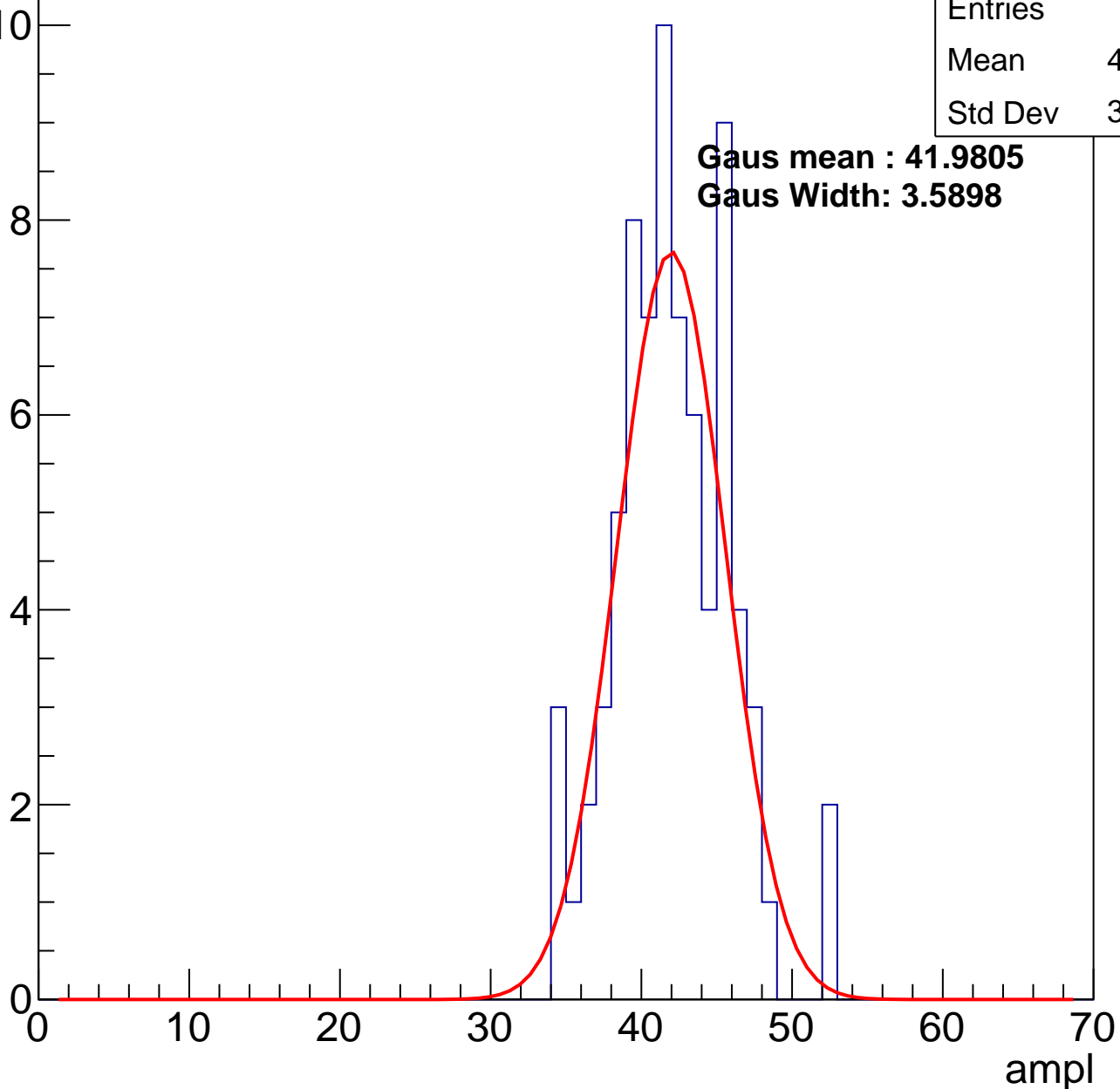
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	41.63
Std Dev	3.734

**Gaus mean : 41.9805**

**Gaus Width: 3.5898**

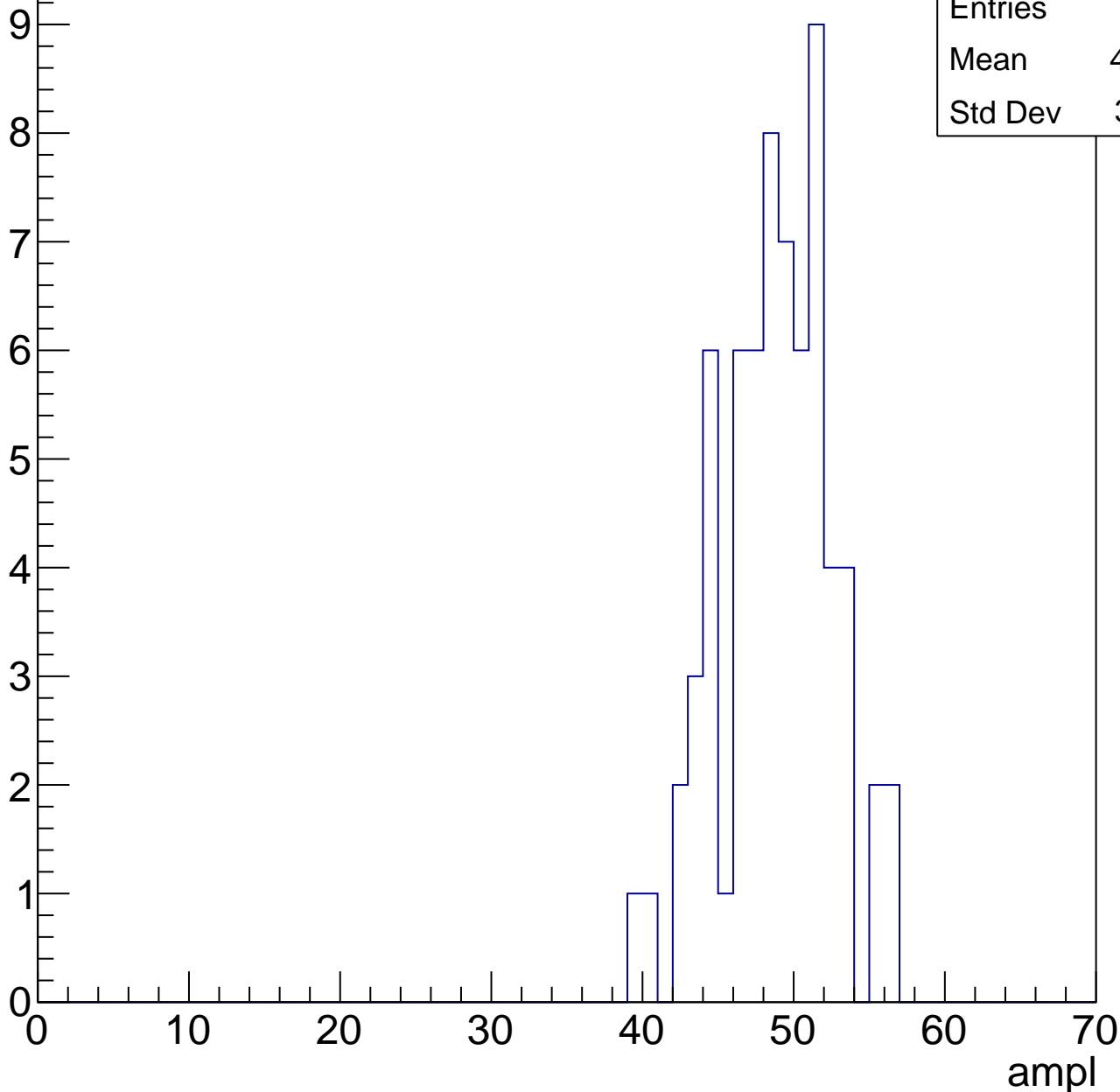


# B1L103S, U16-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	48.34
Std Dev	3.681

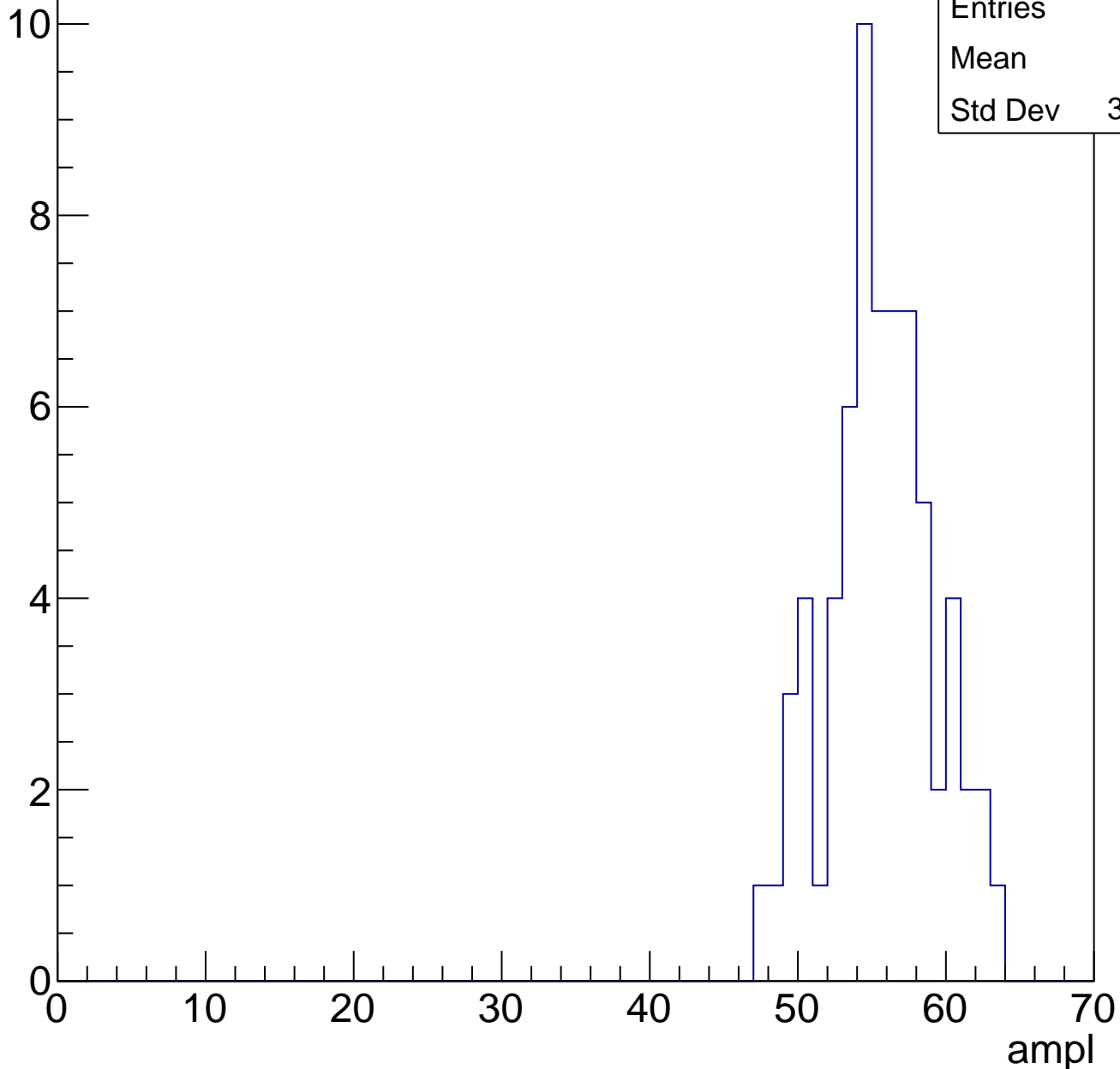


# B1L103S, U16-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	67
Mean	55.1
Std Dev	3.567

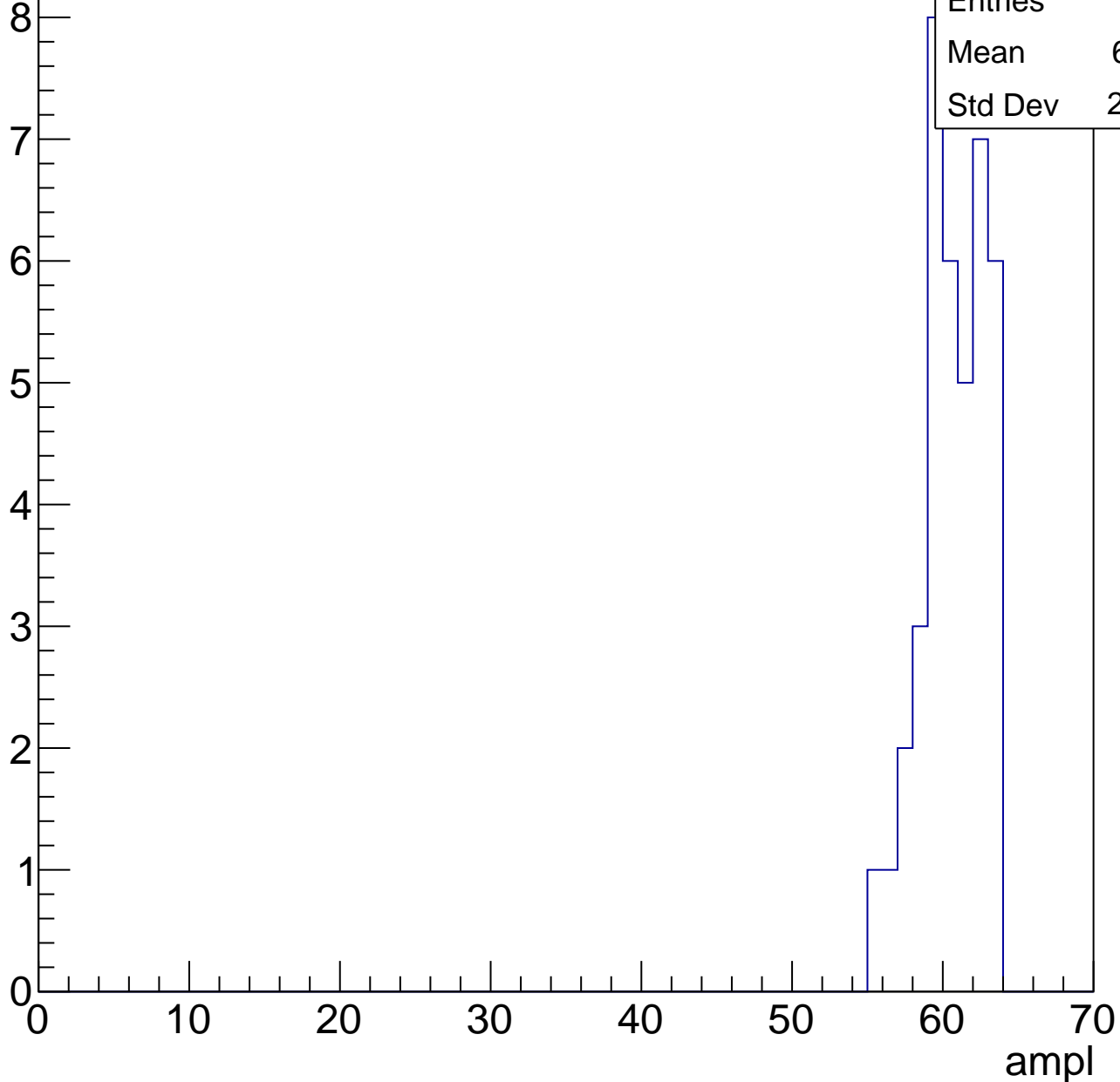
Entry



# B1L103S, U16-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

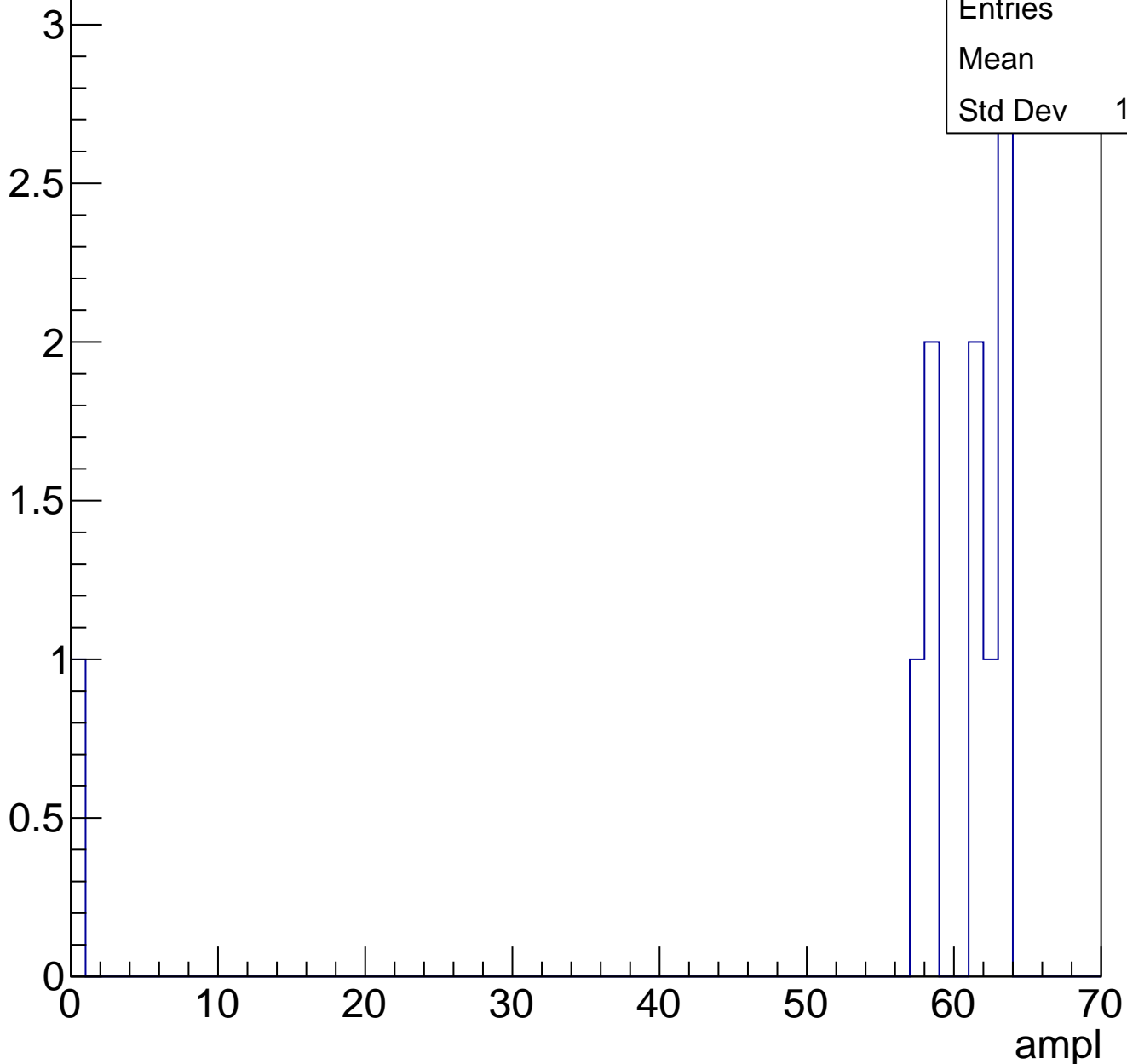
Entry



# B1L103S, U16-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

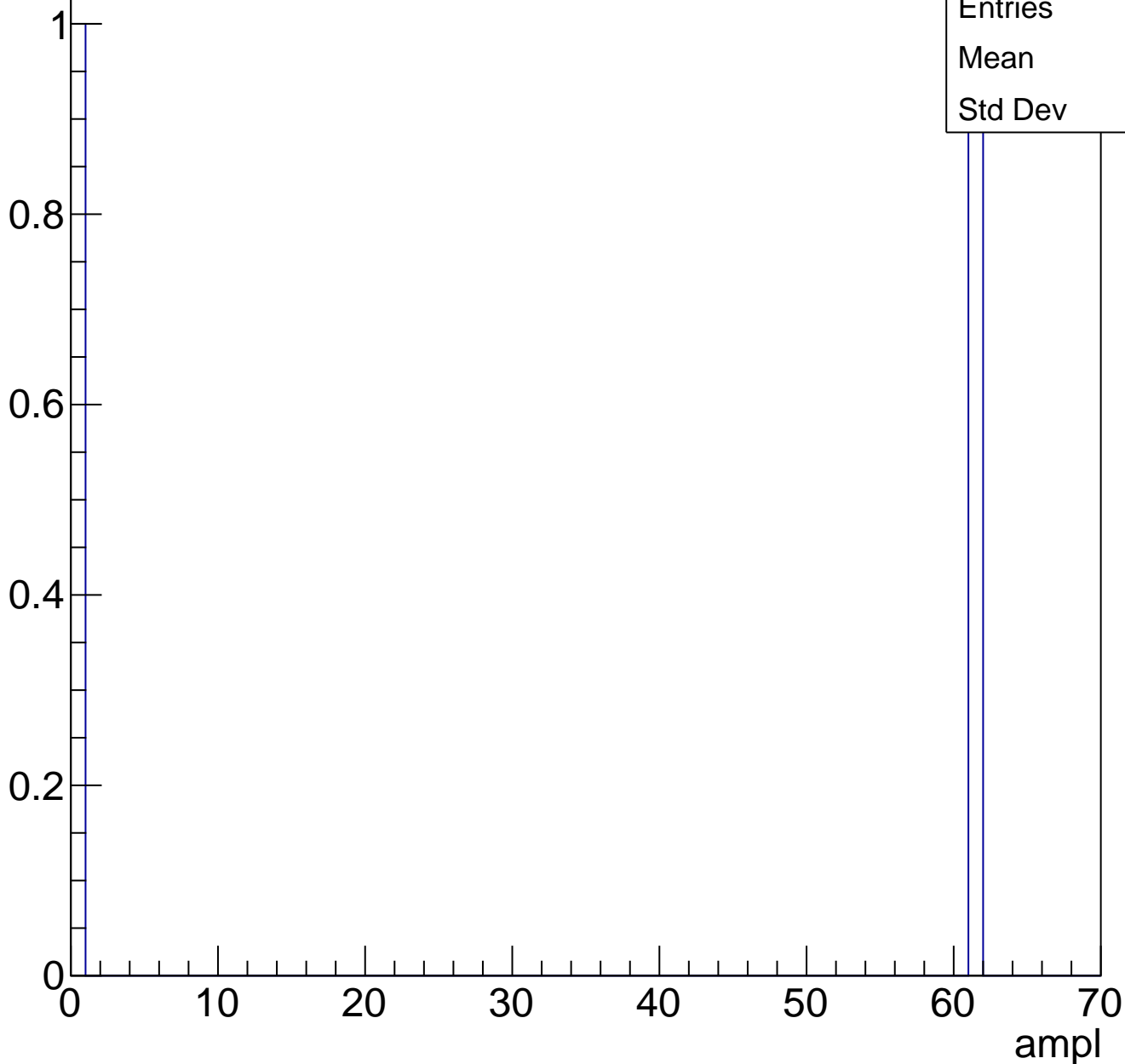




# B1L103S, U16-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch83, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	73
Mean	30.25
Std Dev	5.332

**Gaus mean : 31.1962**

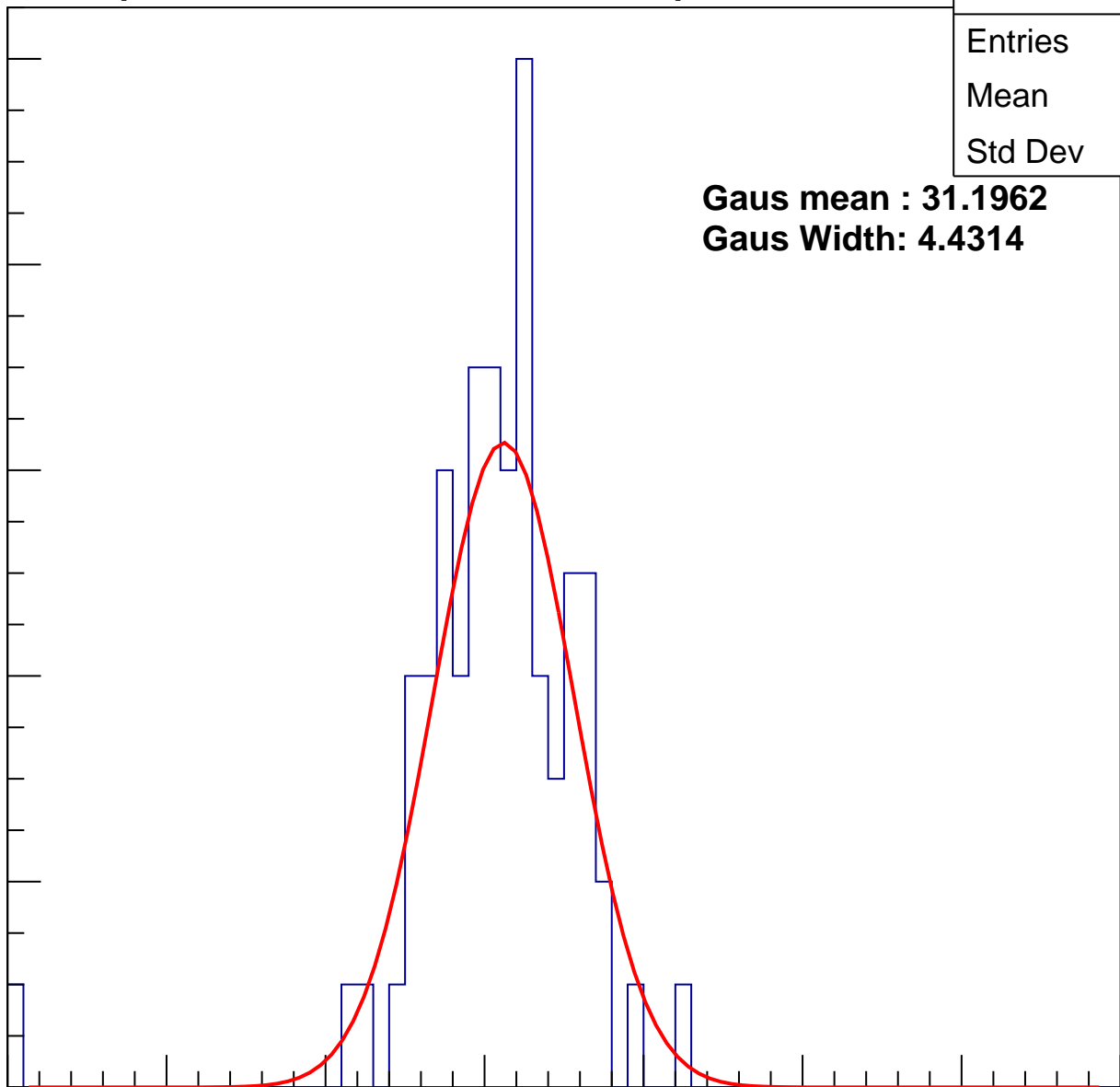
**Gaus Width: 4.4314**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U16-ch83, adc1

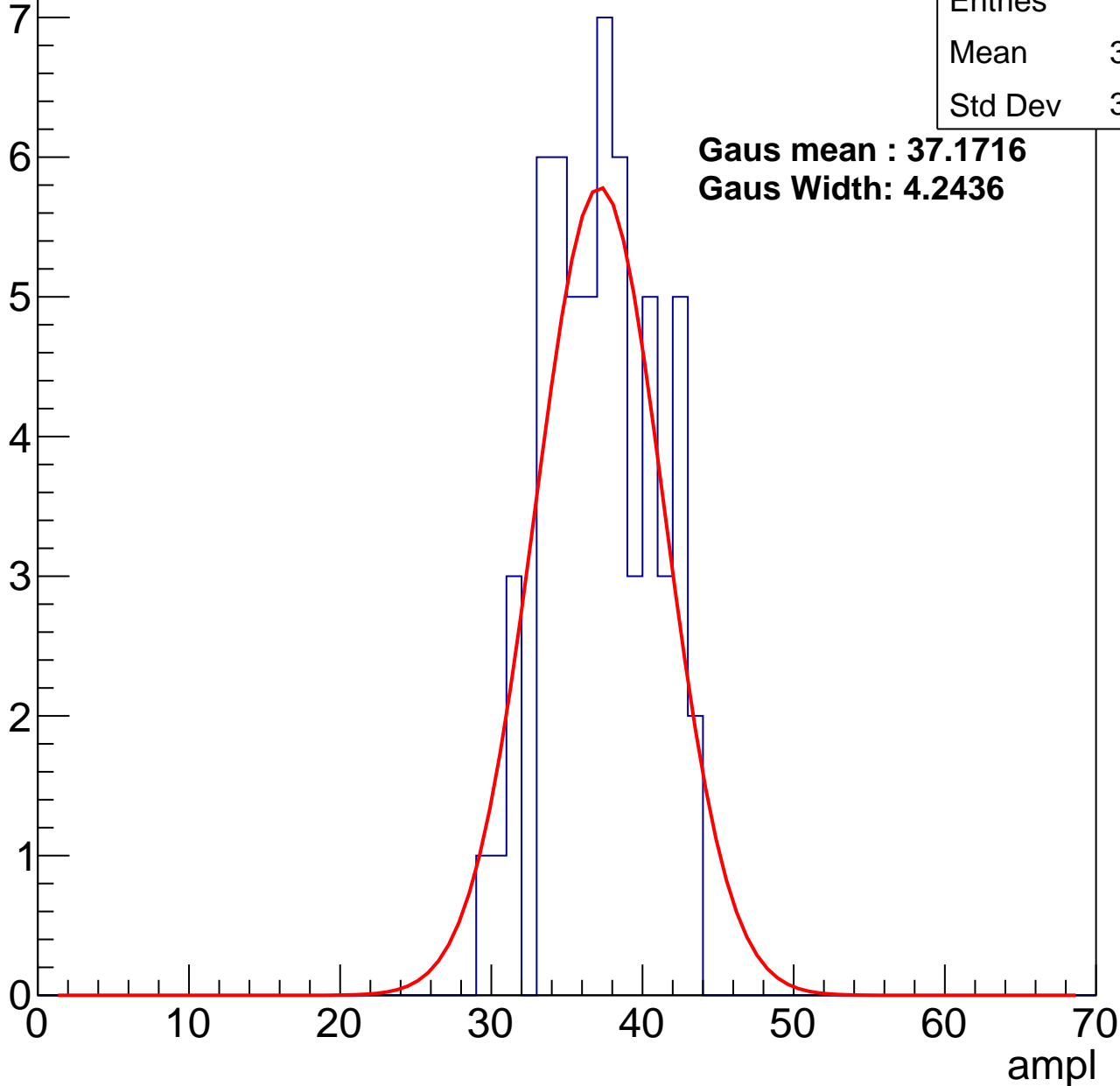
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	36.76
Std Dev	3.476

**Gaus mean : 37.1716**

**Gaus Width: 4.2436**



# B1L103S, U16-ch83, adc2

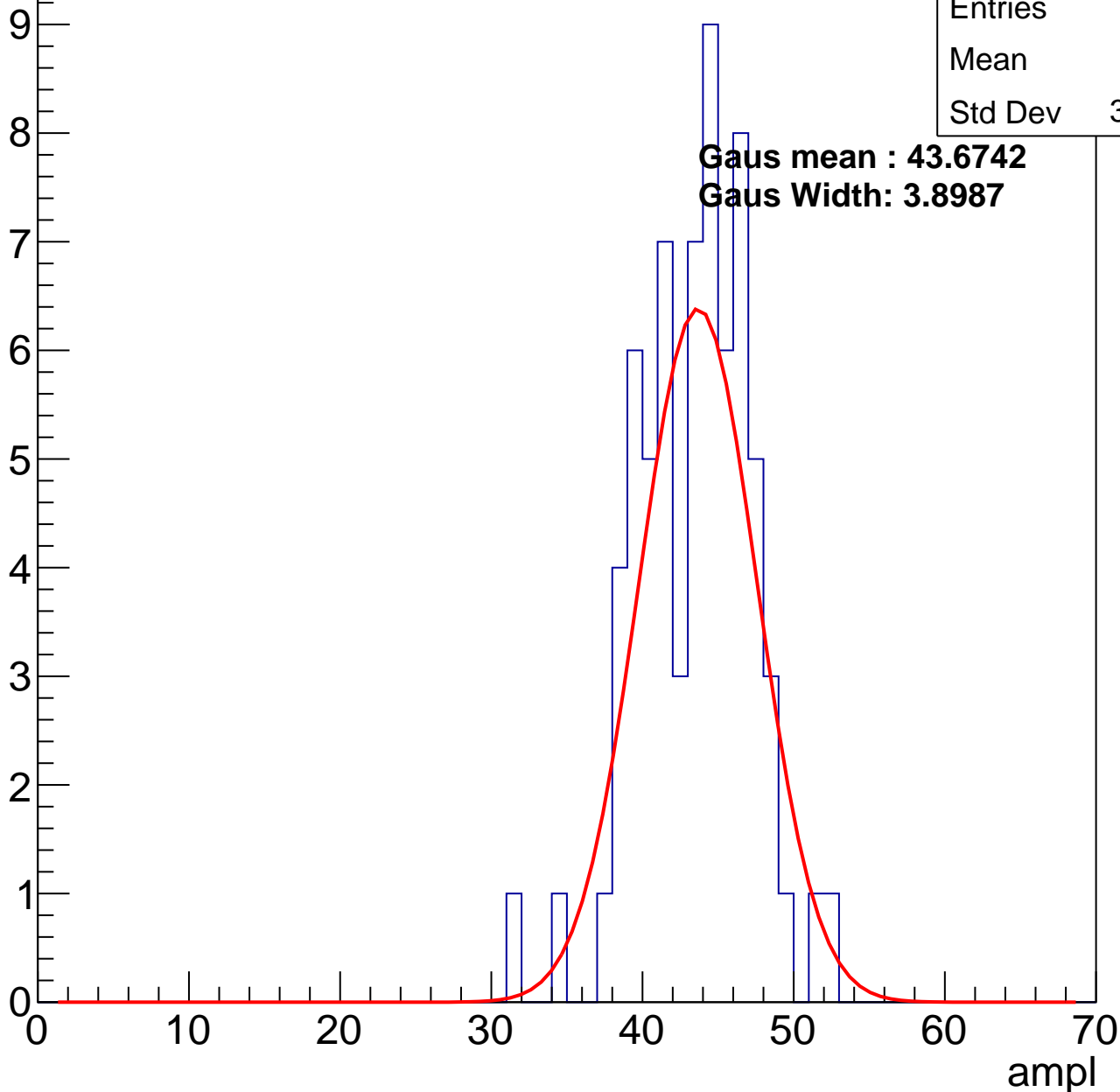
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	43
Std Dev	3.757

**Gaus mean : 43.6742**

**Gaus Width: 3.8987**

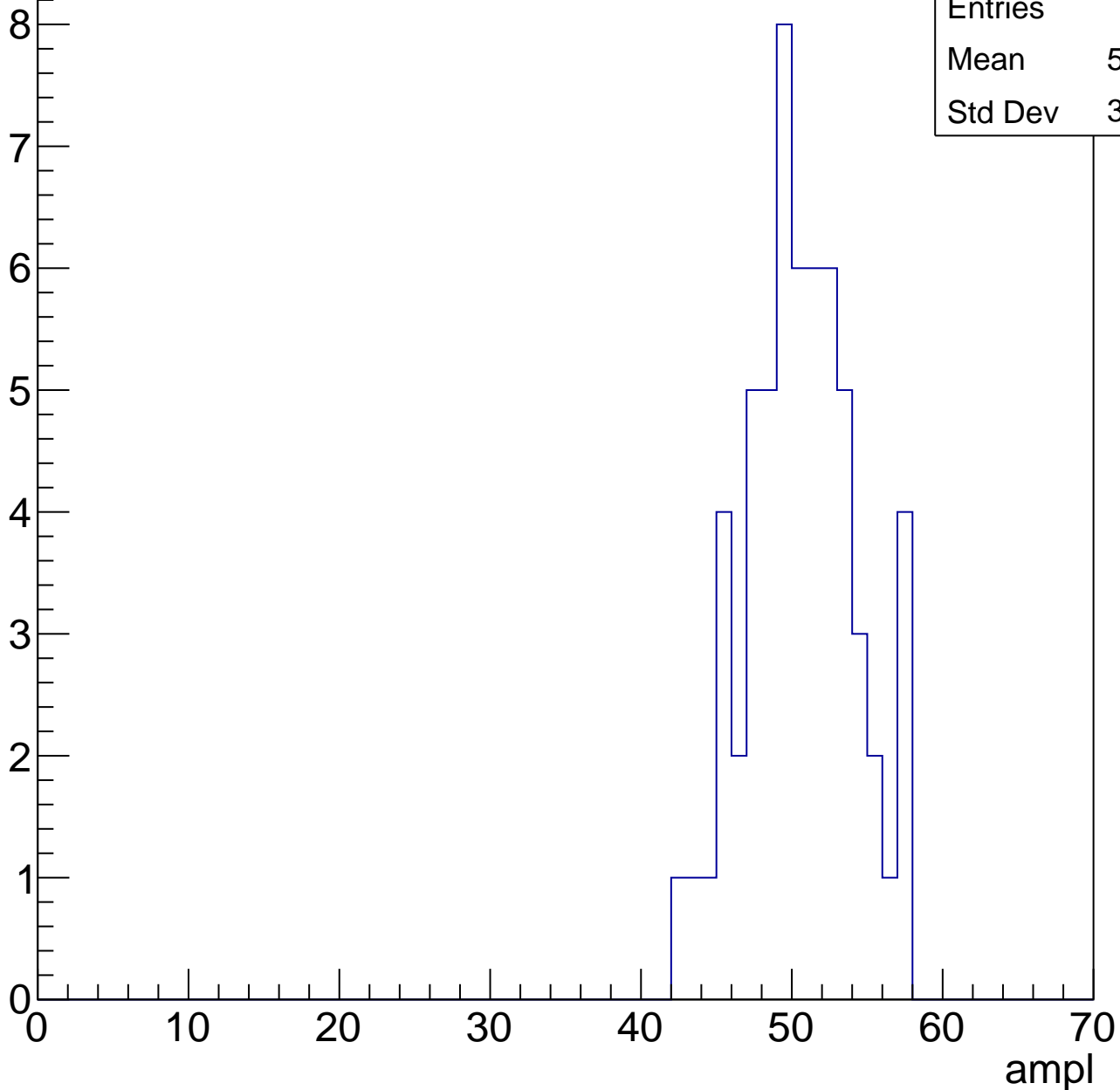


# B1L103S, U16-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	50.12
Std Dev	3.555

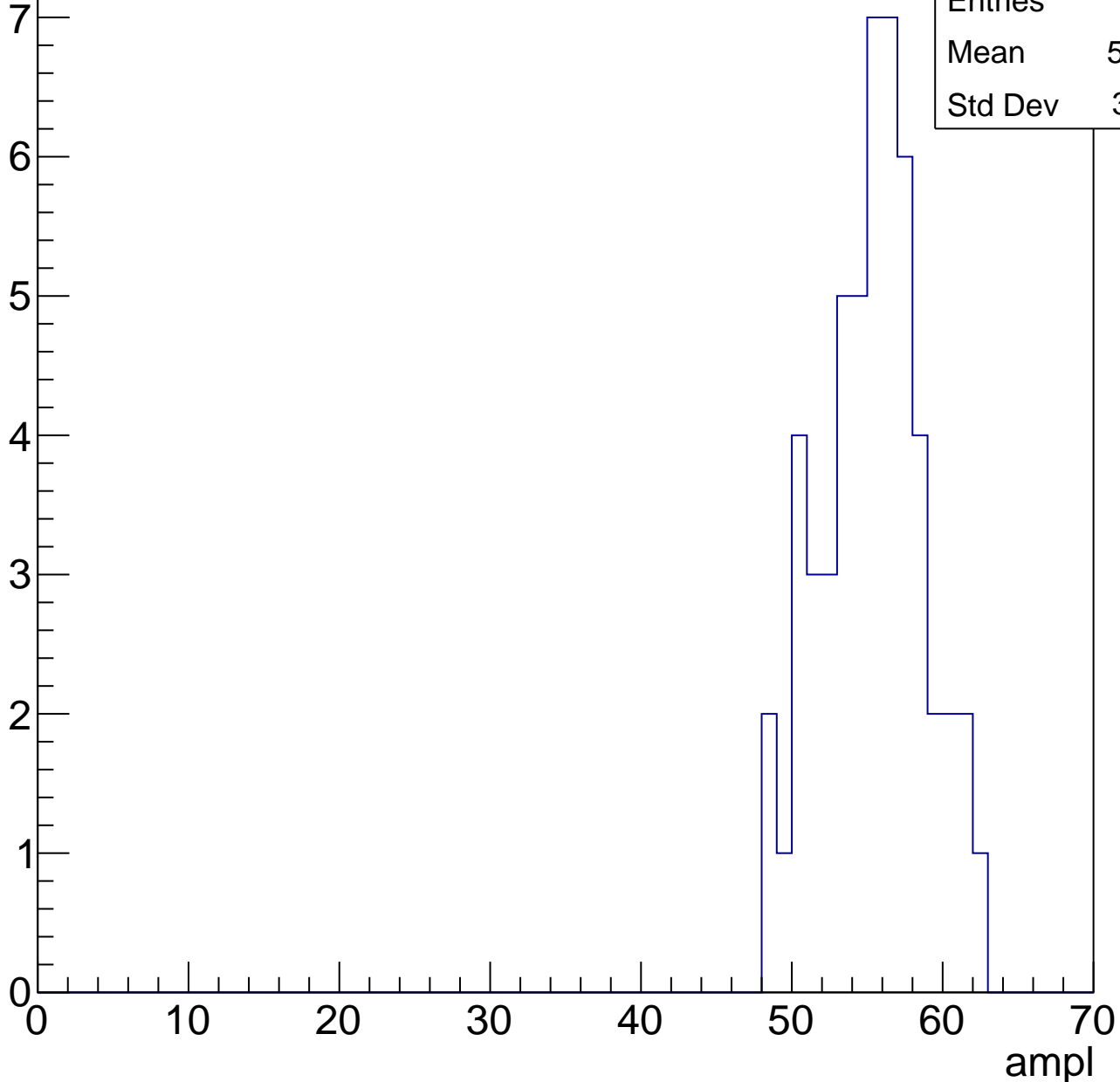


# B1L103S, U16-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

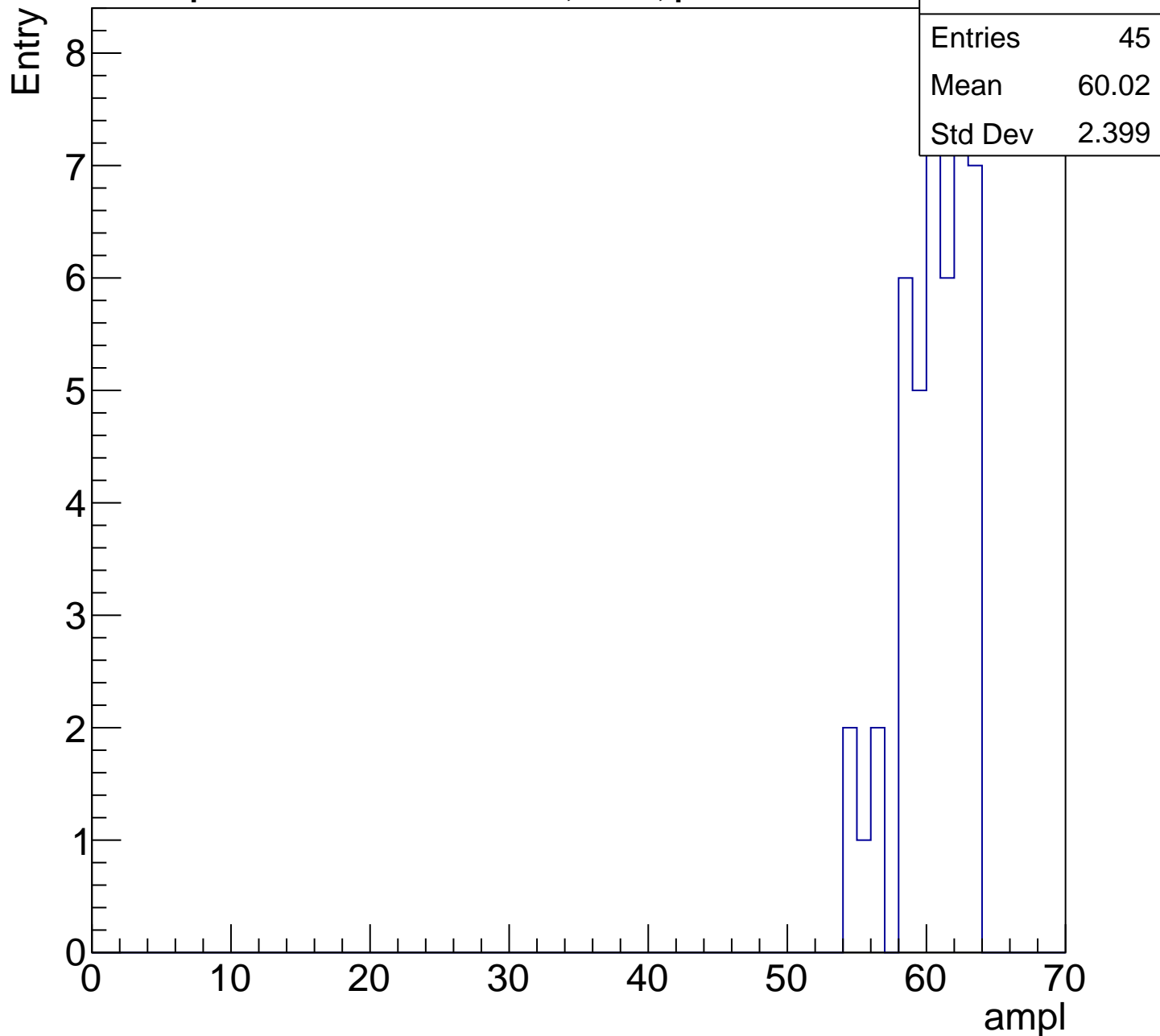
Entry

Entries	54
Mean	54.85
Std Dev	3.341



# B1L103S, U16-ch83, adc5

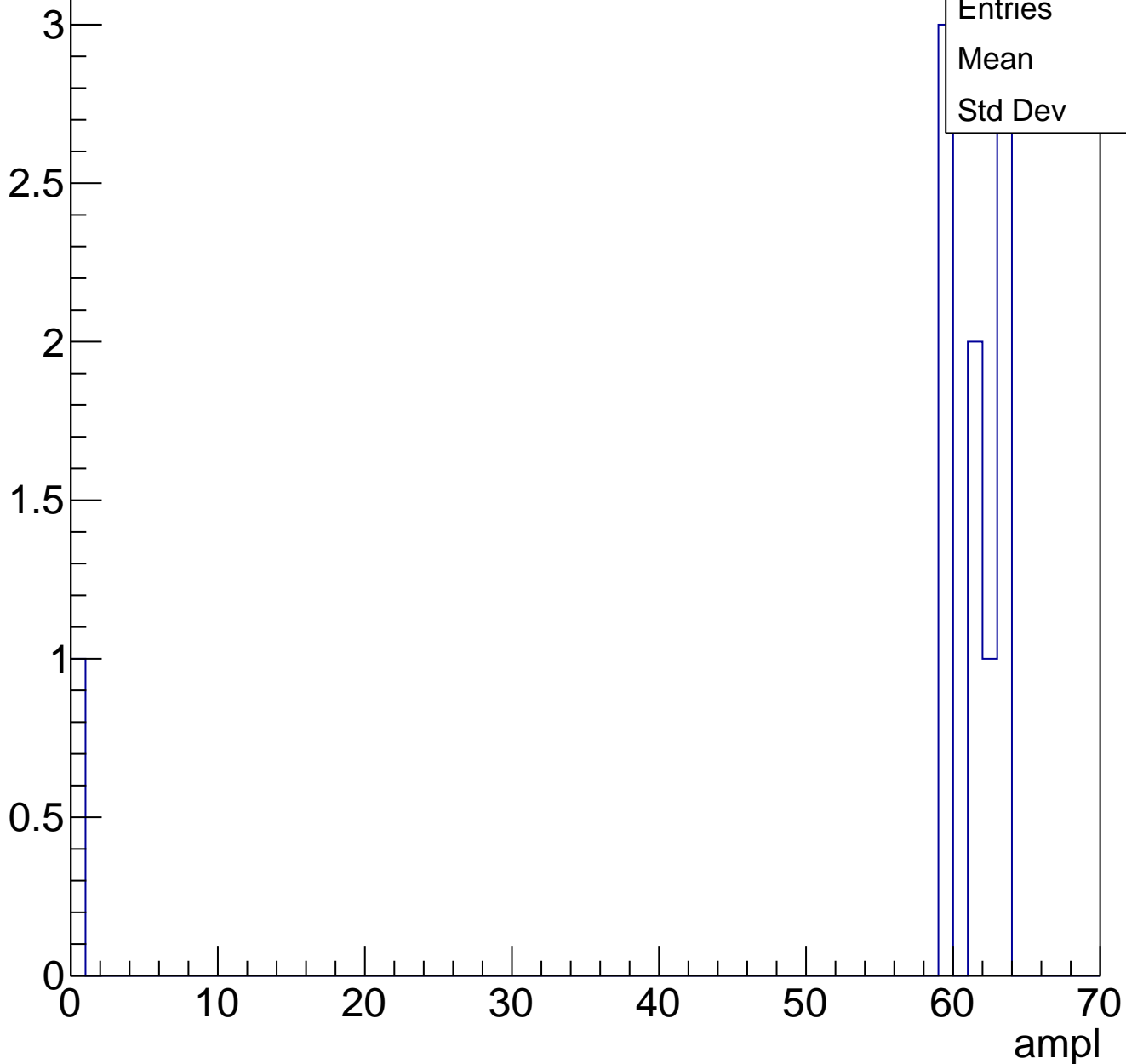
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U16-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U16-ch84, adc0

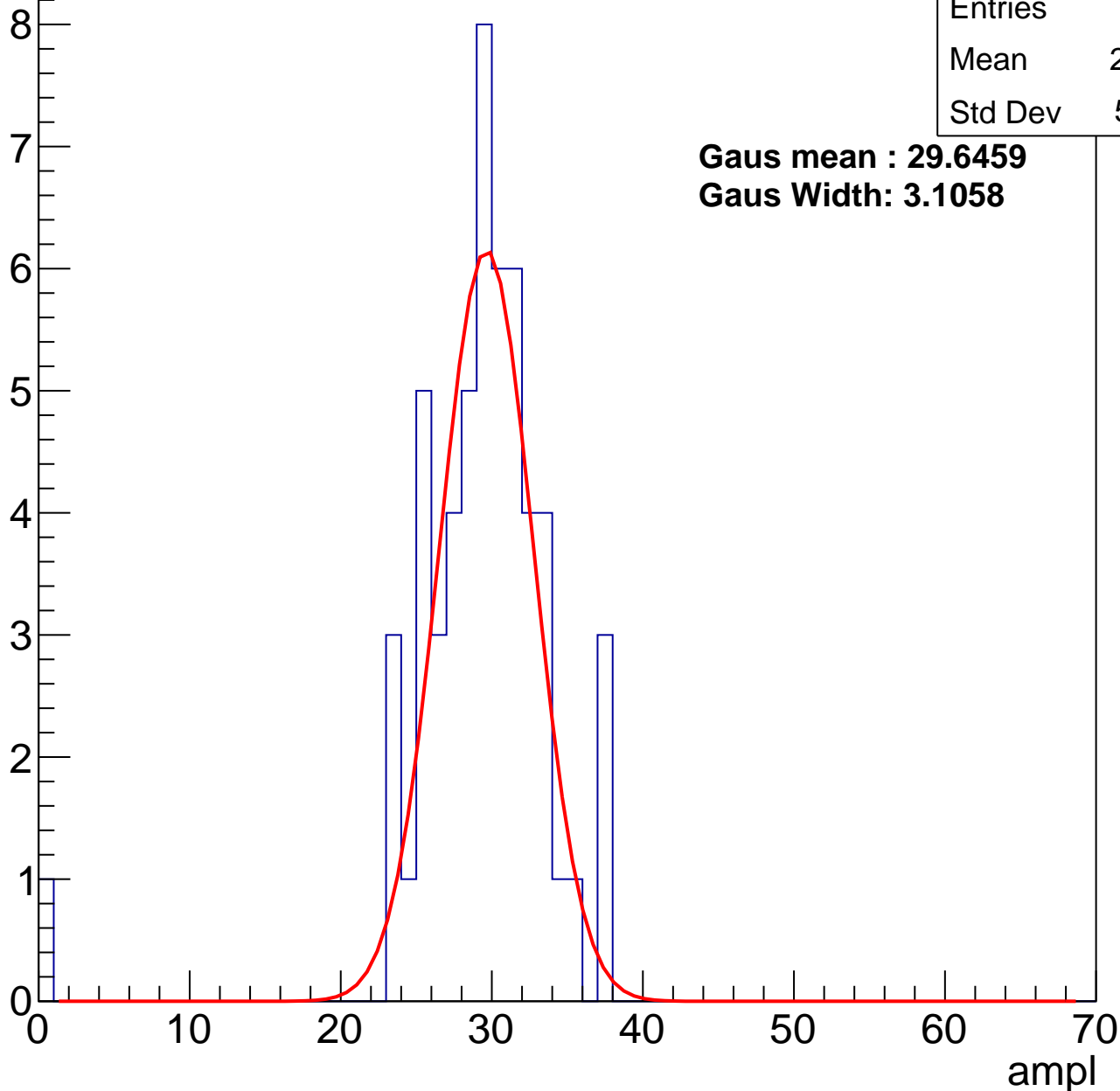
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	28.76
Std Dev	5.191

**Gaus mean : 29.6459**

**Gaus Width: 3.1058**



# B1L103S, U16-ch84, adc1

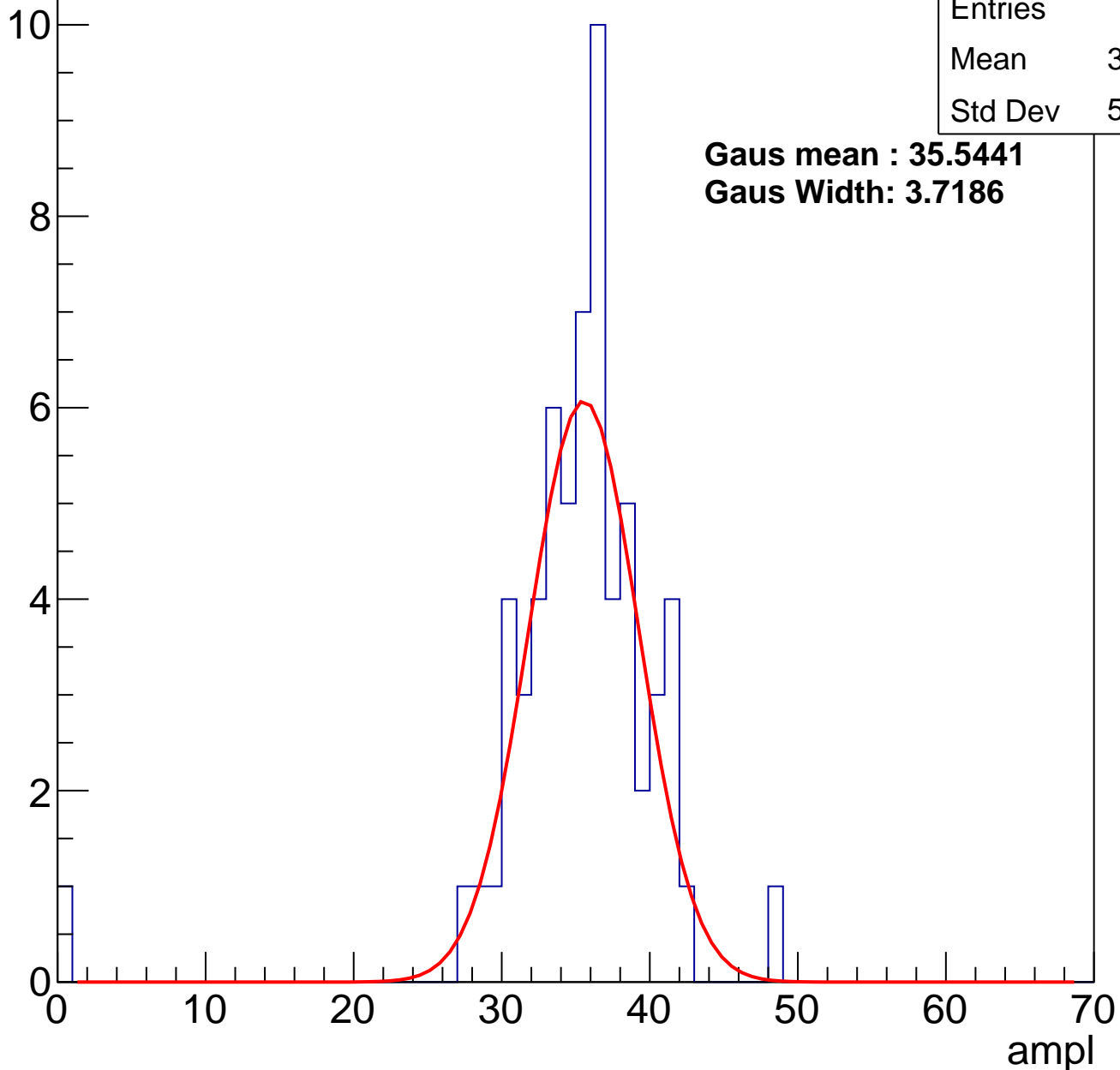
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	63
Mean	34.73
Std Dev	5.804

**Gaus mean : 35.5441**

**Gaus Width: 3.7186**

Entry



# B1L103S, U16-ch84, adc2

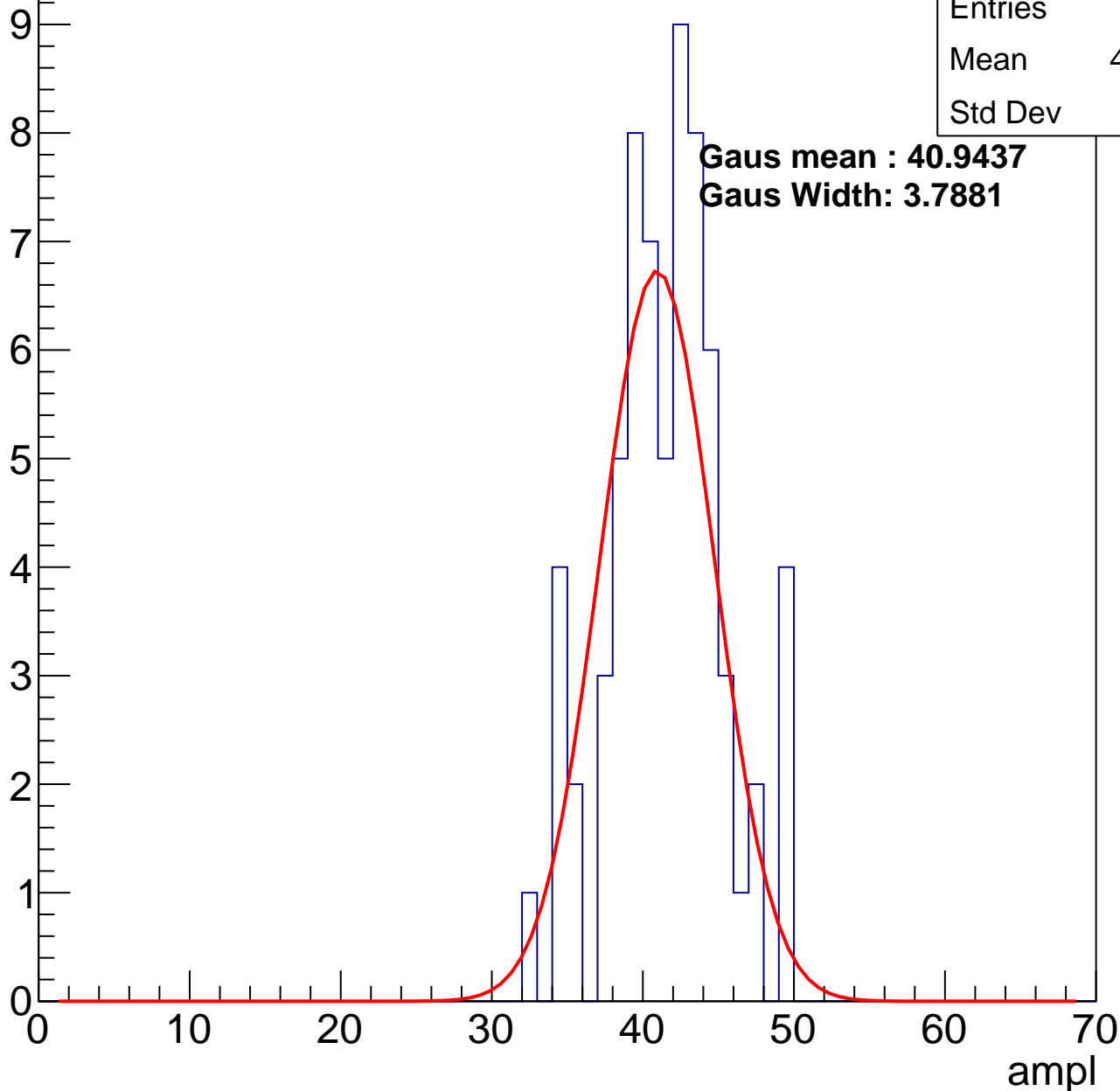
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	41.07
Std Dev	3.79

**Gaus mean : 40.9437**

**Gaus Width: 3.7881**

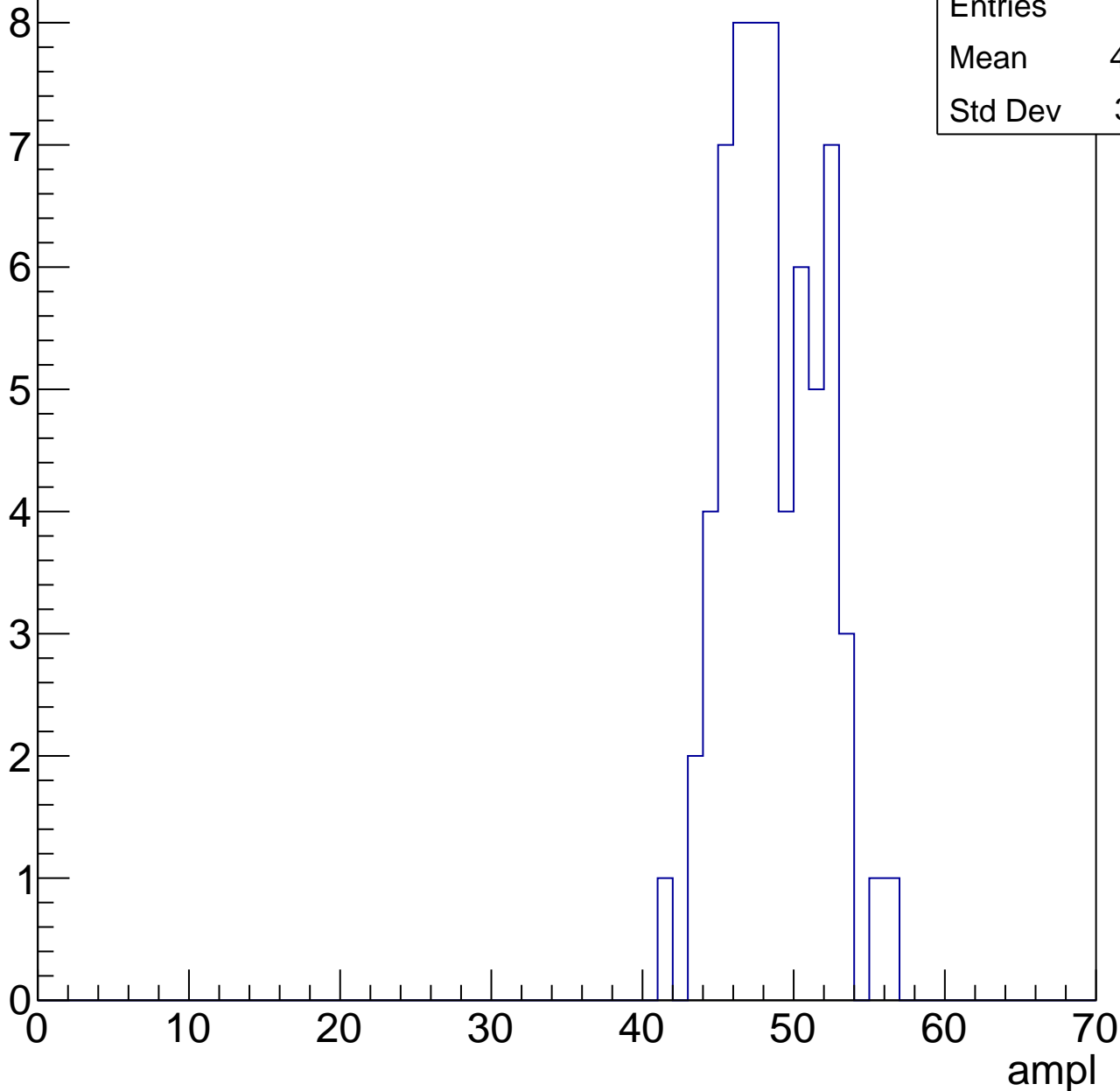


# B1L103S, U16-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

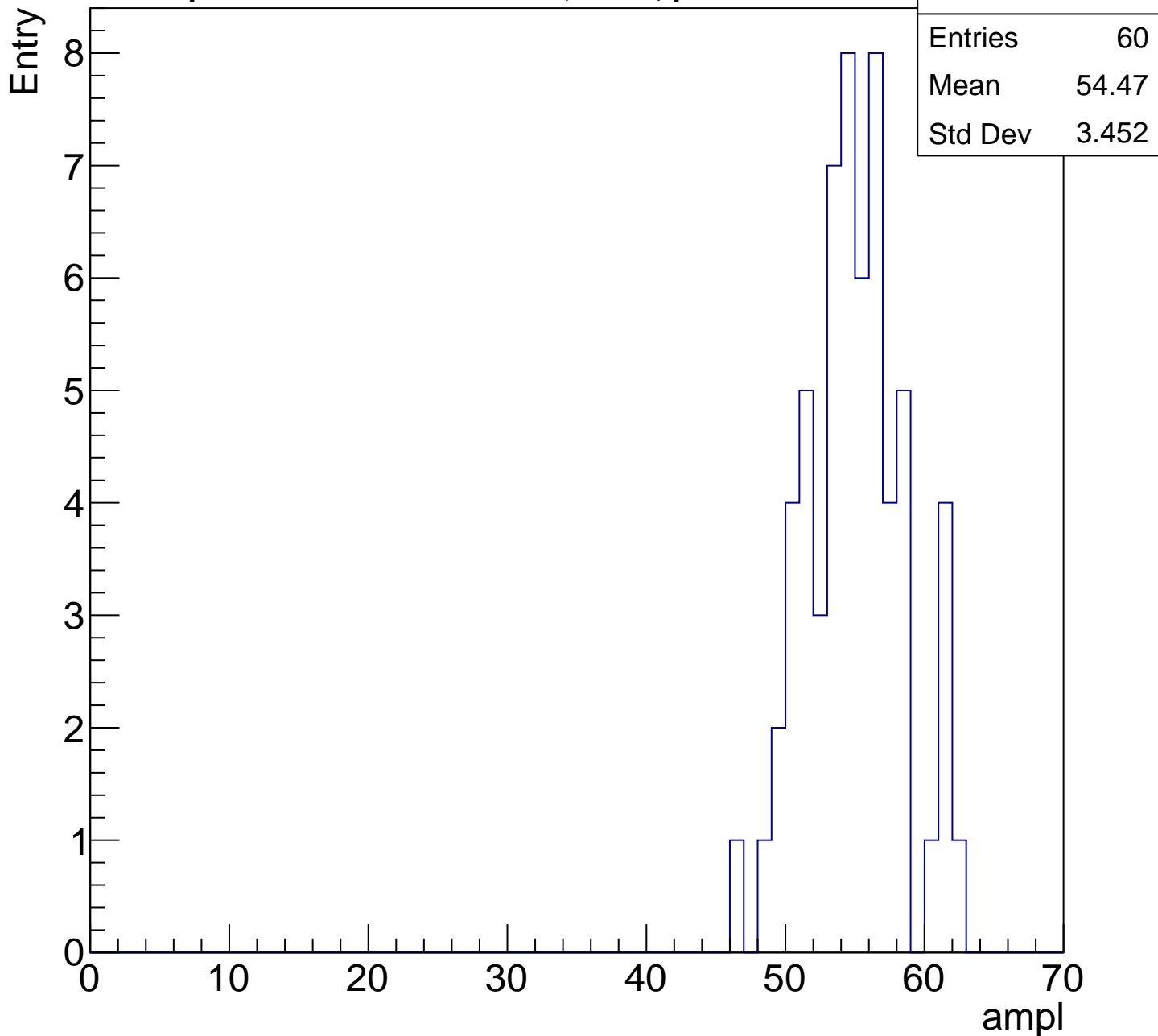
Entry

Entries	65
Mean	48.17
Std Dev	3.131



# B1L103S, U16-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

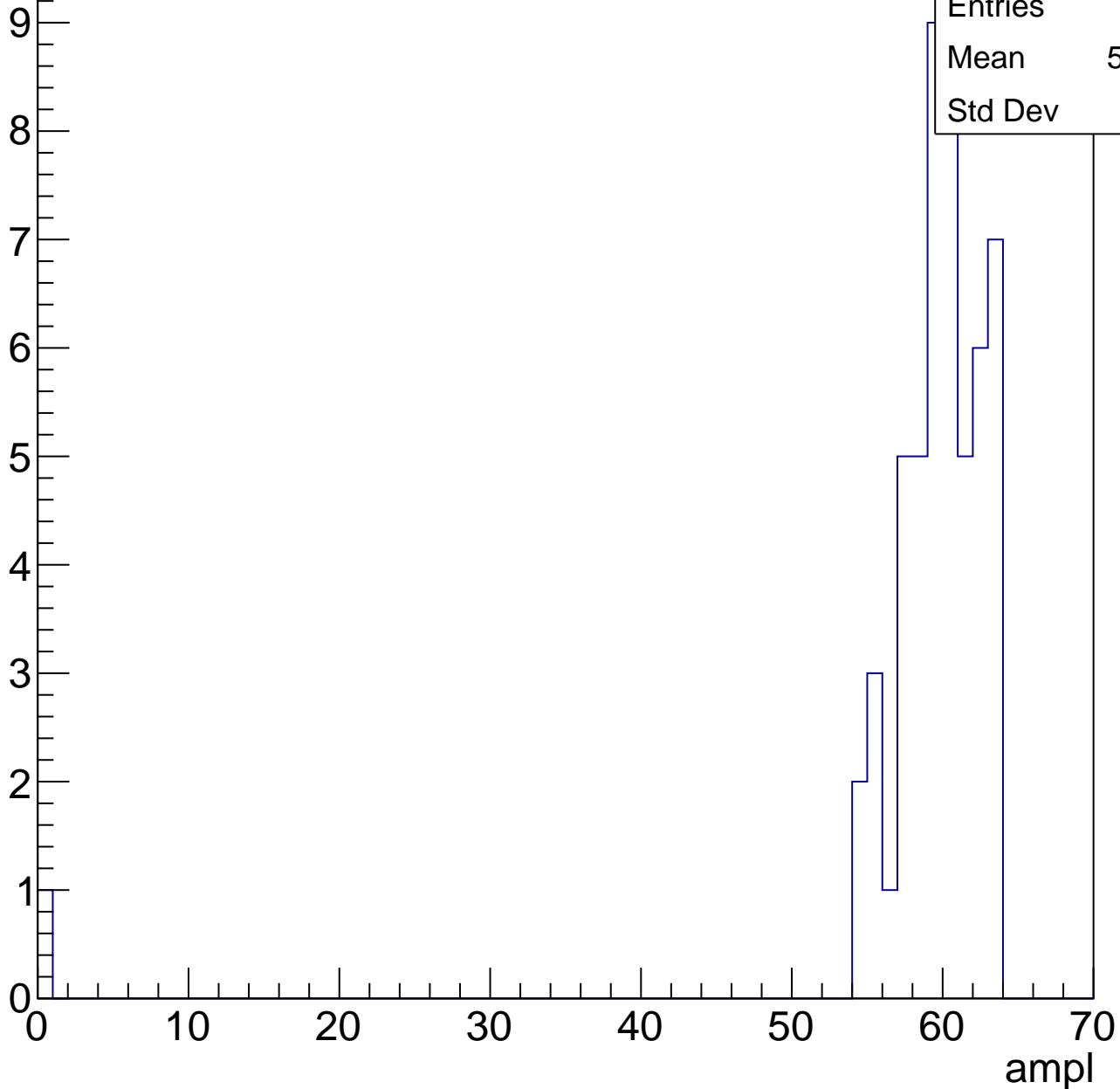


# B1L103S, U16-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

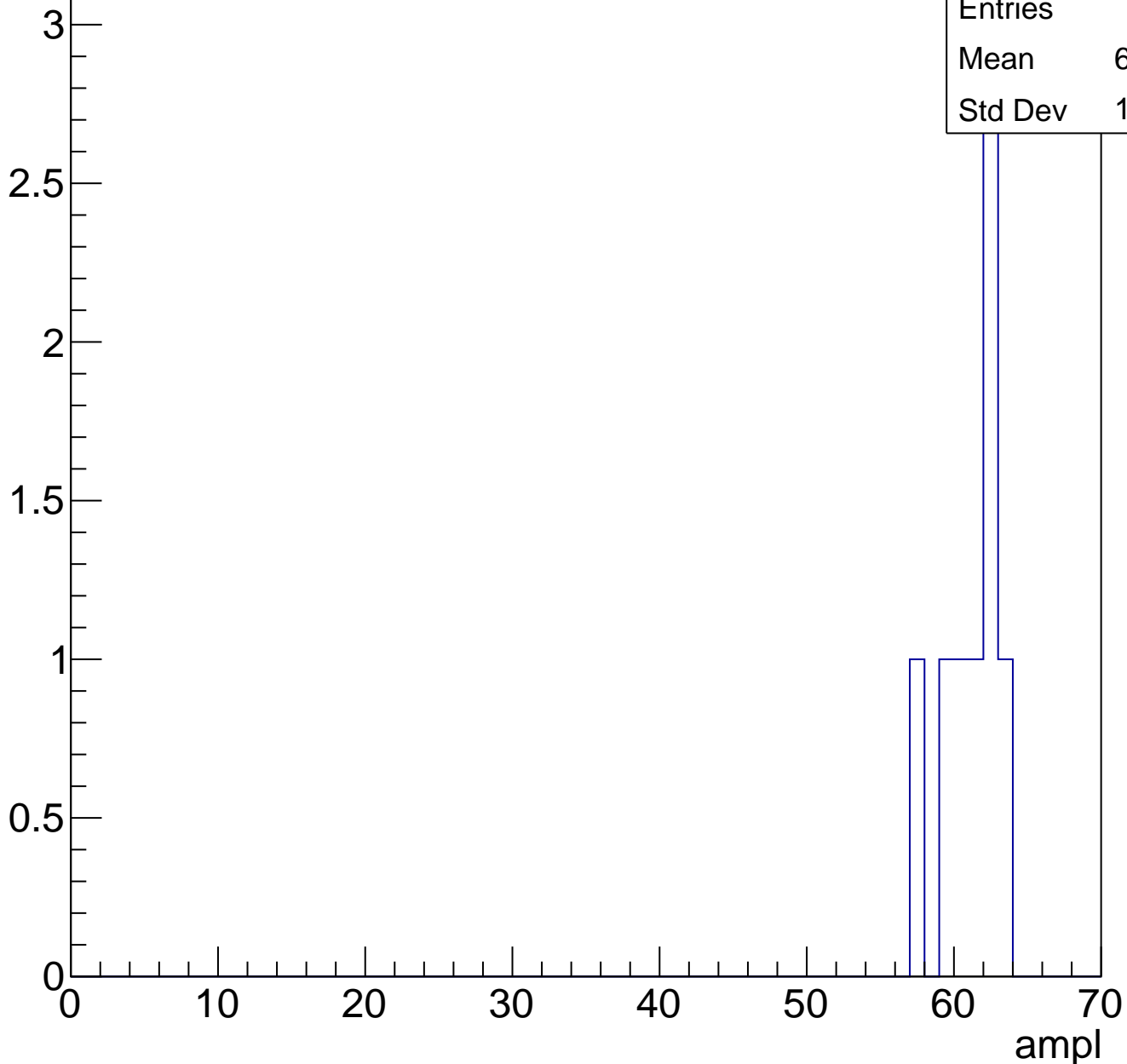
Entries	52
Mean	58.33
Std Dev	8.53



# B1L103S, U16-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch85, adc0

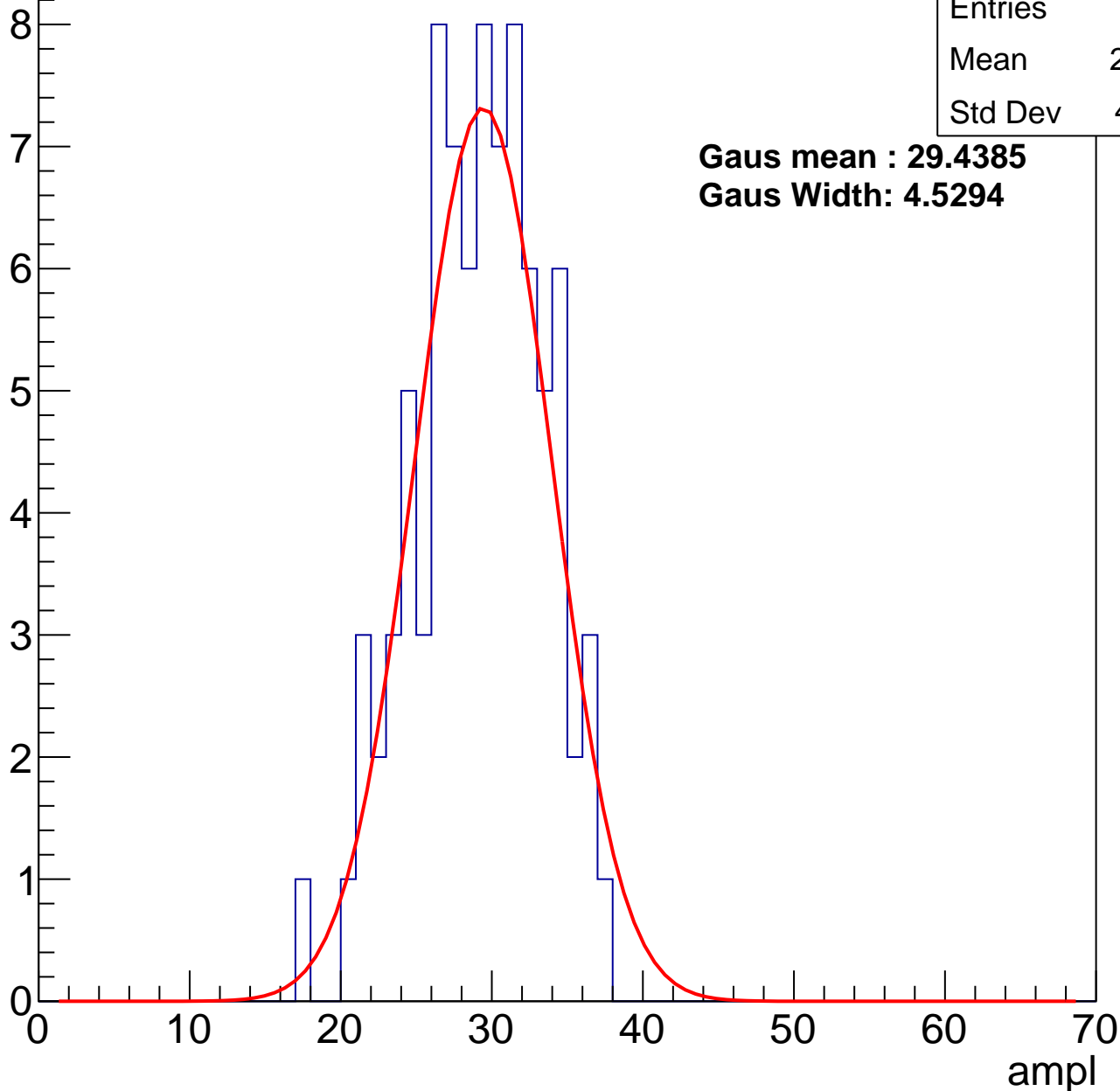
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	85
Mean	28.69
Std Dev	4.201

**Gaus mean : 29.4385**

**Gaus Width: 4.5294**



# B1L103S, U16-ch85, adc1

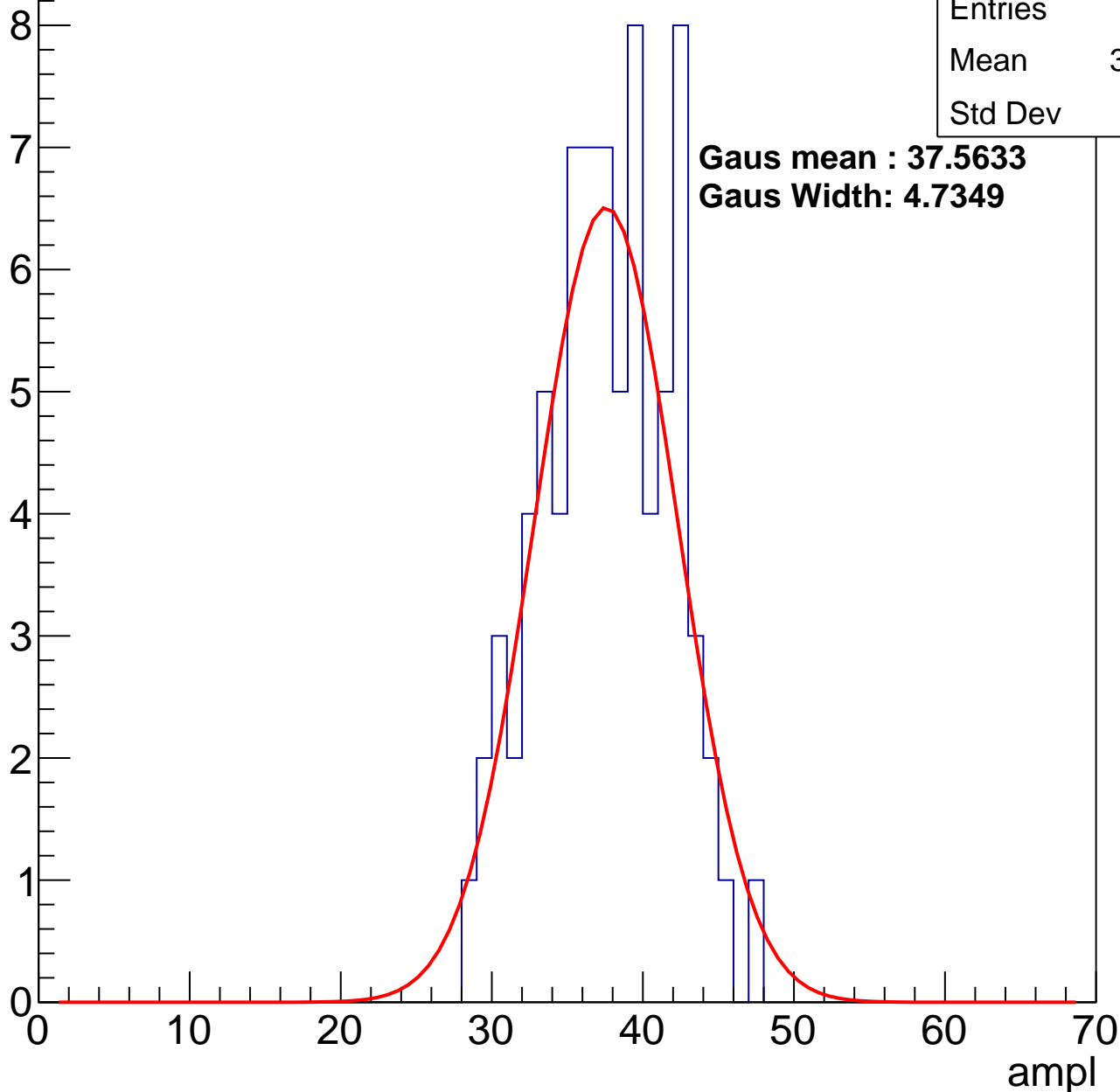
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	37.15
Std Dev	4.21

**Gaus mean : 37.5633**

**Gaus Width: 4.7349**



# B1L103S, U16-ch85, adc2

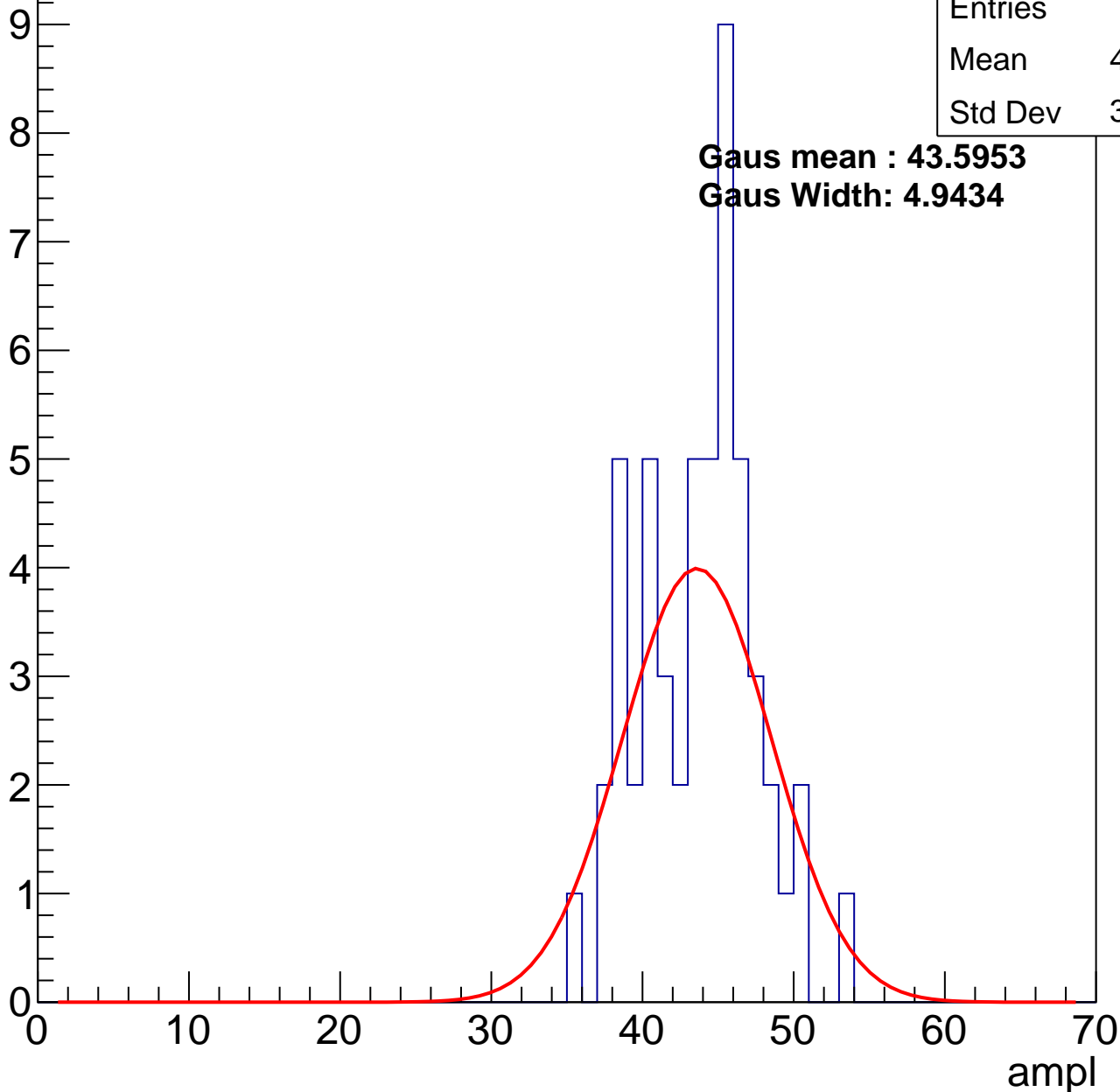
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	43.26
Std Dev	3.802

**Gaus mean : 43.5953**

**Gaus Width: 4.9434**

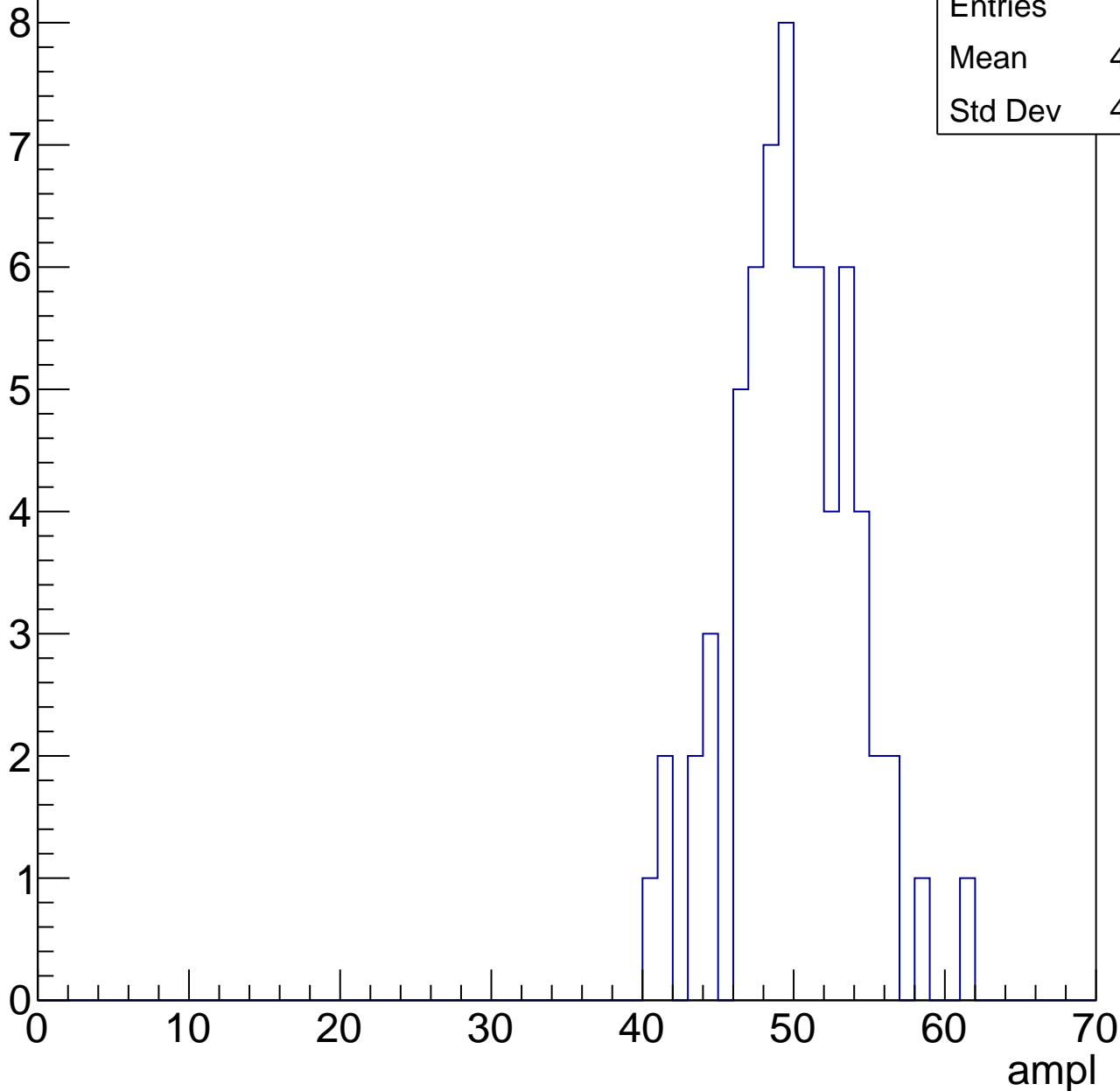


# B1L103S, U16-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	49.53
Std Dev	4.027

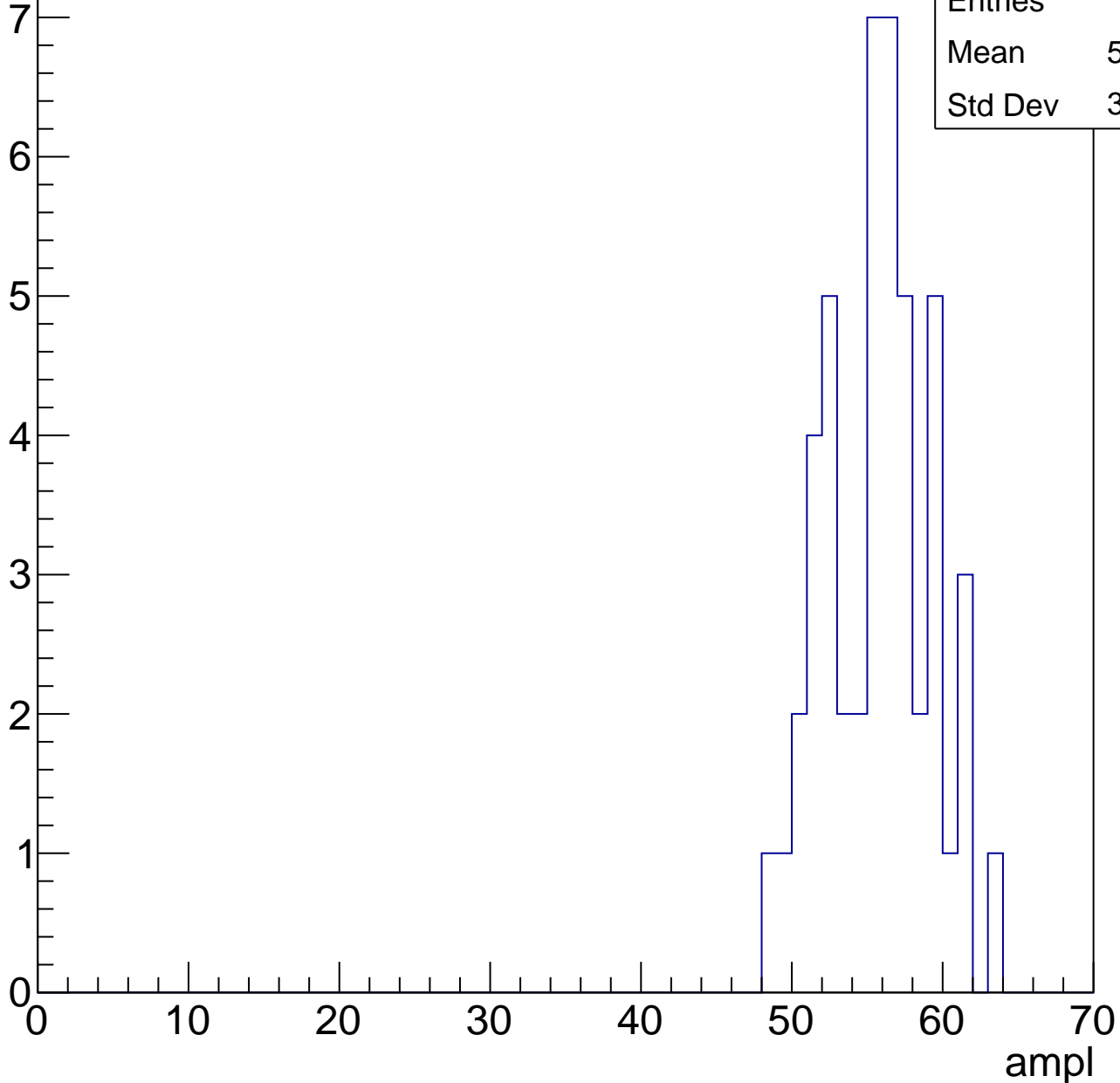


# B1L103S, U16-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	55.29
Std Dev	3.452

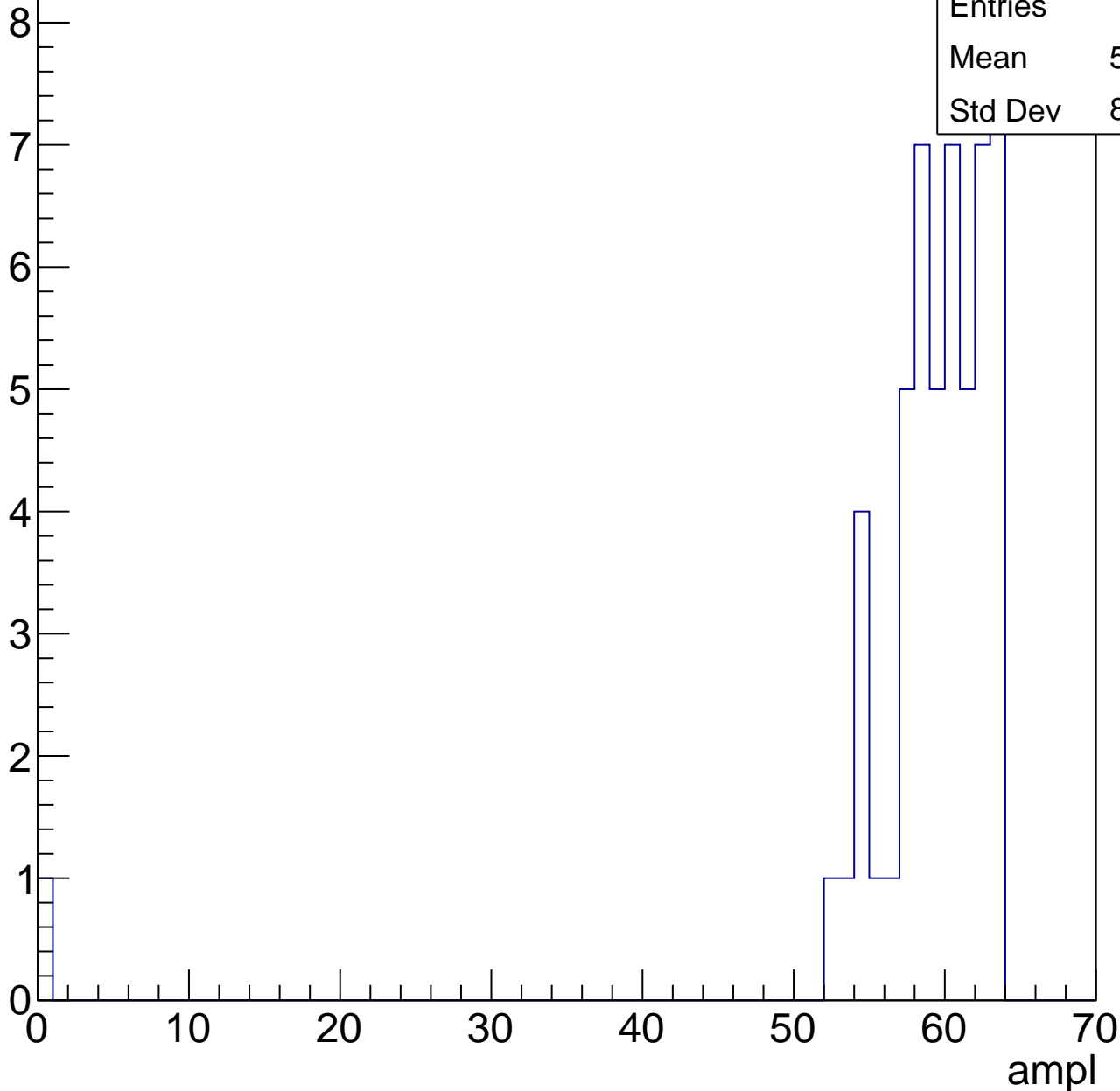


# B1L103S, U16-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

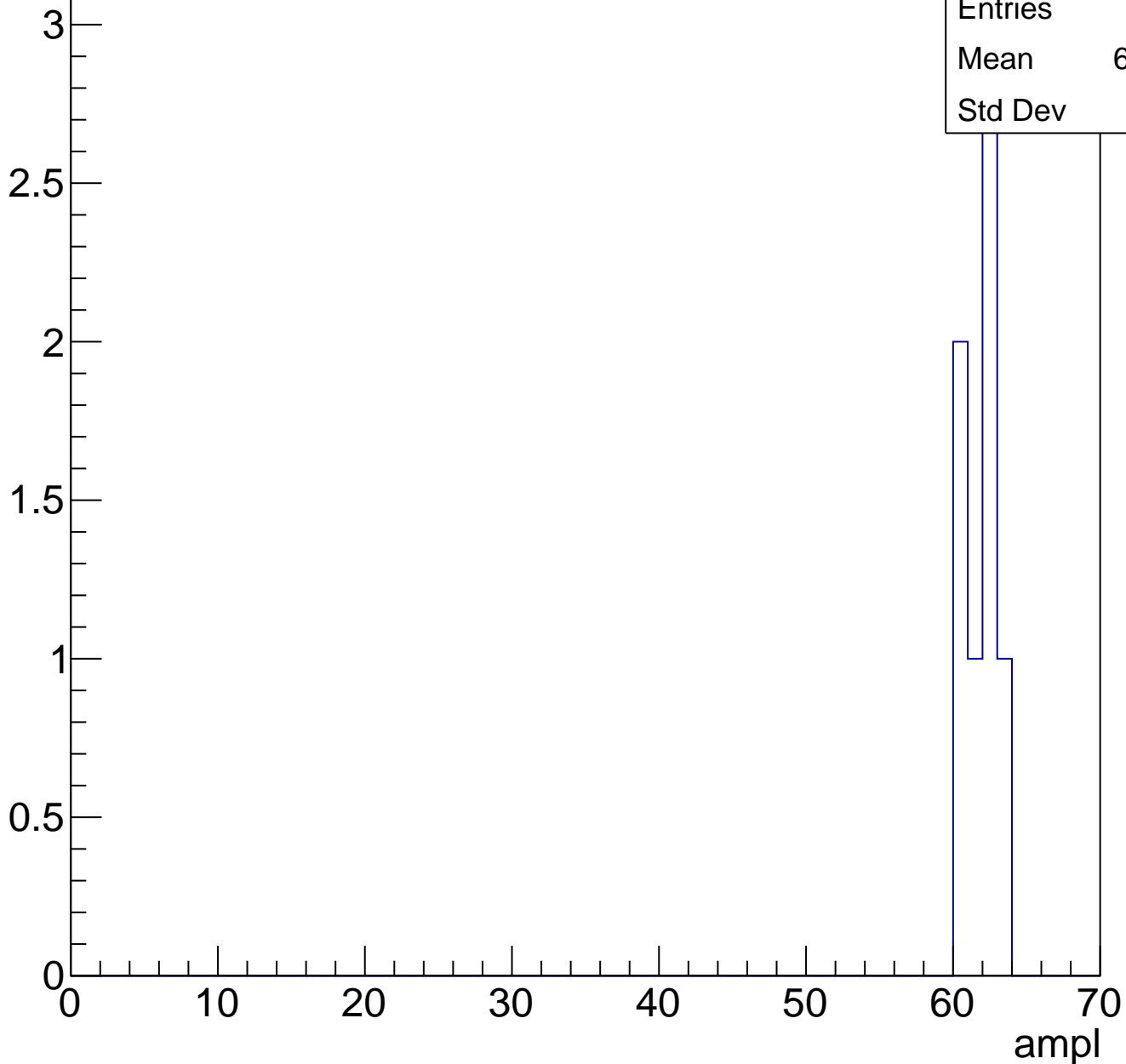
Entries	53
Mean	58.13
Std Dev	8.574



# B1L103S, U16-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L103S, U16-ch86, adc0

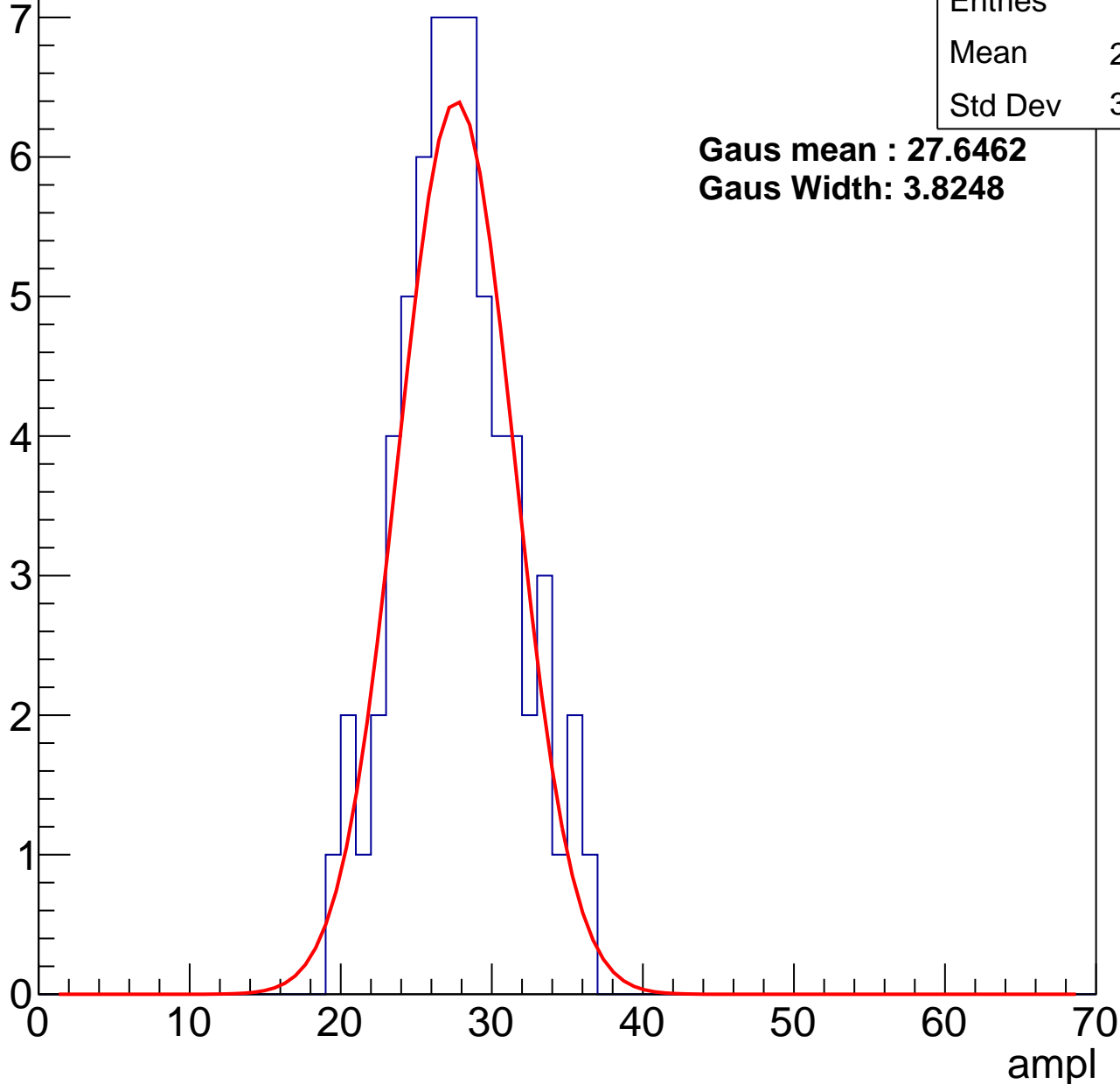
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	27.27
Std Dev	3.805

**Gaus mean : 27.6462**

**Gaus Width: 3.8248**



# B1L103S, U16-ch86, adc1

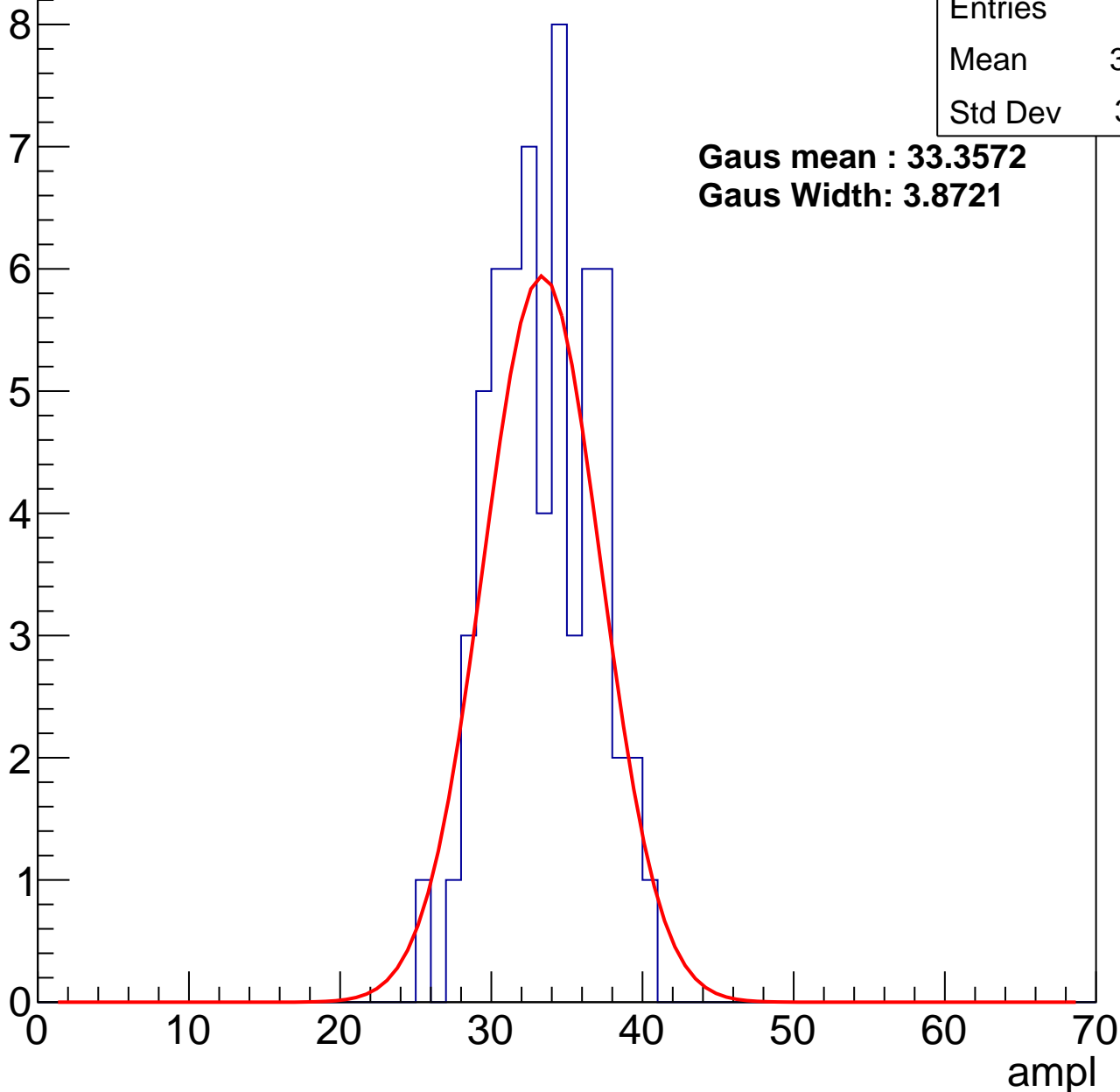
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	32.98
Std Dev	3.341

**Gaus mean : 33.3572**

**Gaus Width: 3.8721**



# B1L103S, U16-ch86, adc2

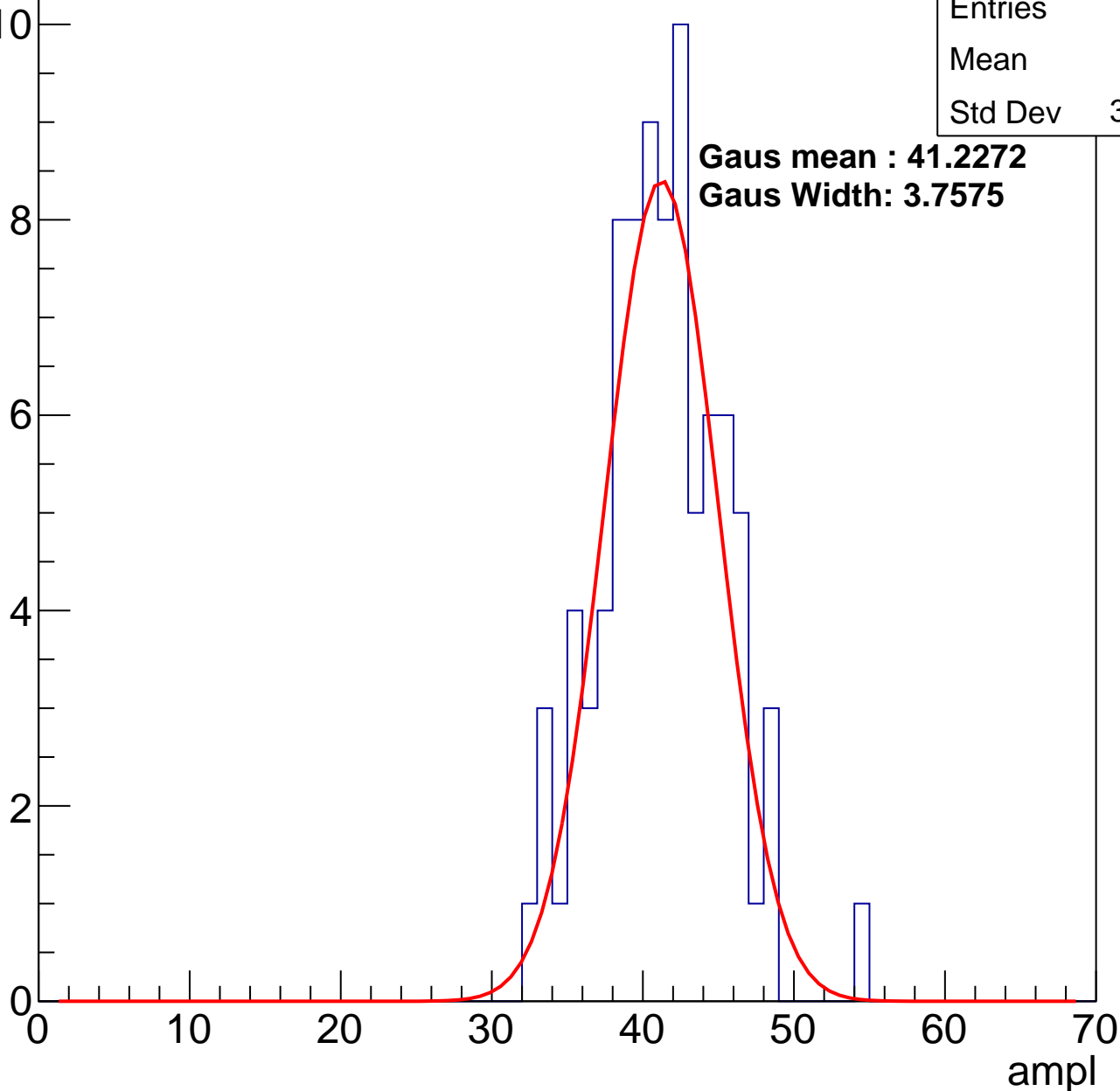
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	86
Mean	40.8
Std Dev	3.994

**Gaus mean : 41.2272**

**Gaus Width: 3.7575**

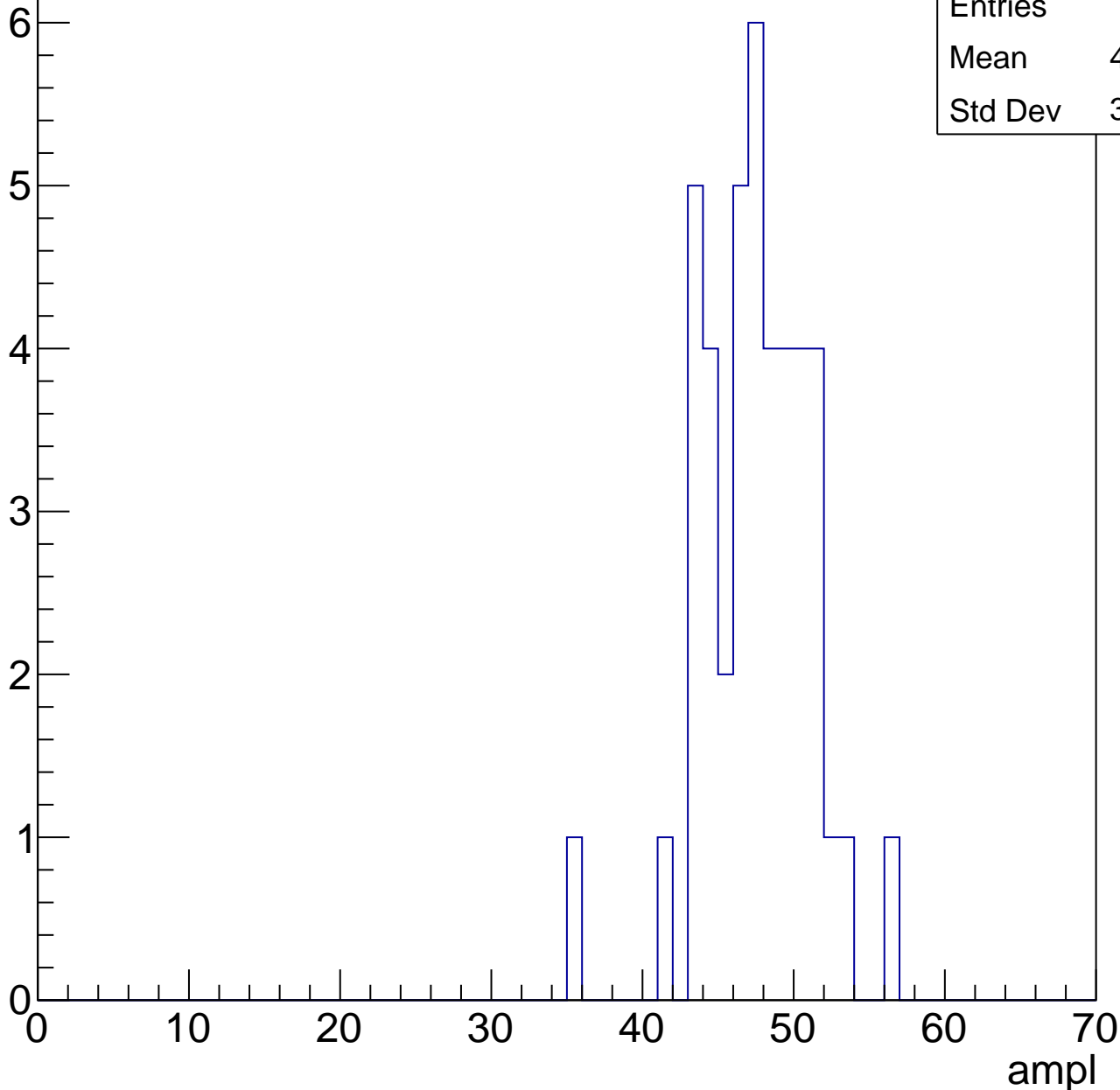


# B1L103S, U16-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	43
Mean	47.02
Std Dev	3.644

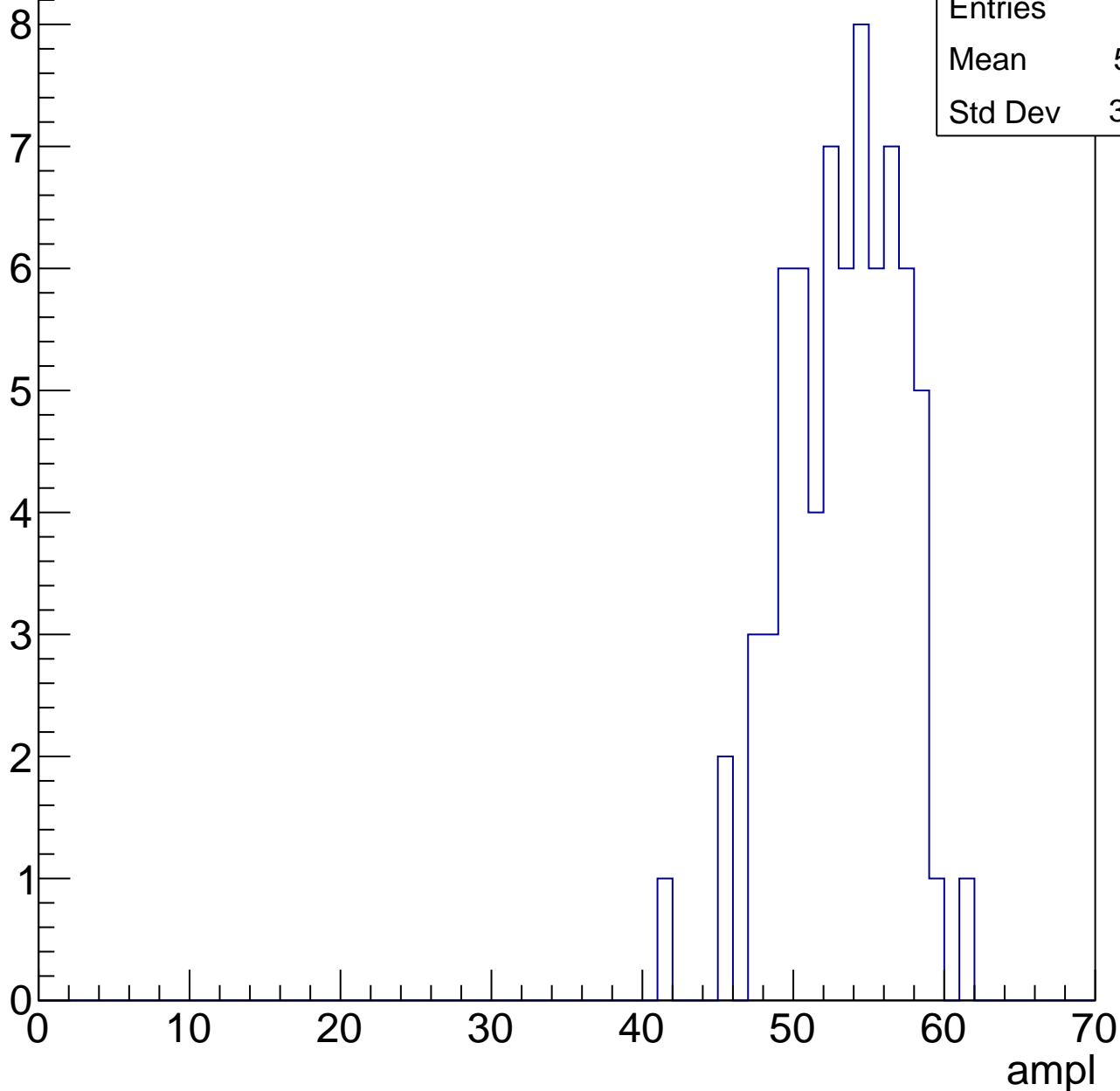


# B1L103S, U16-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	52.81
Std Dev	3.803

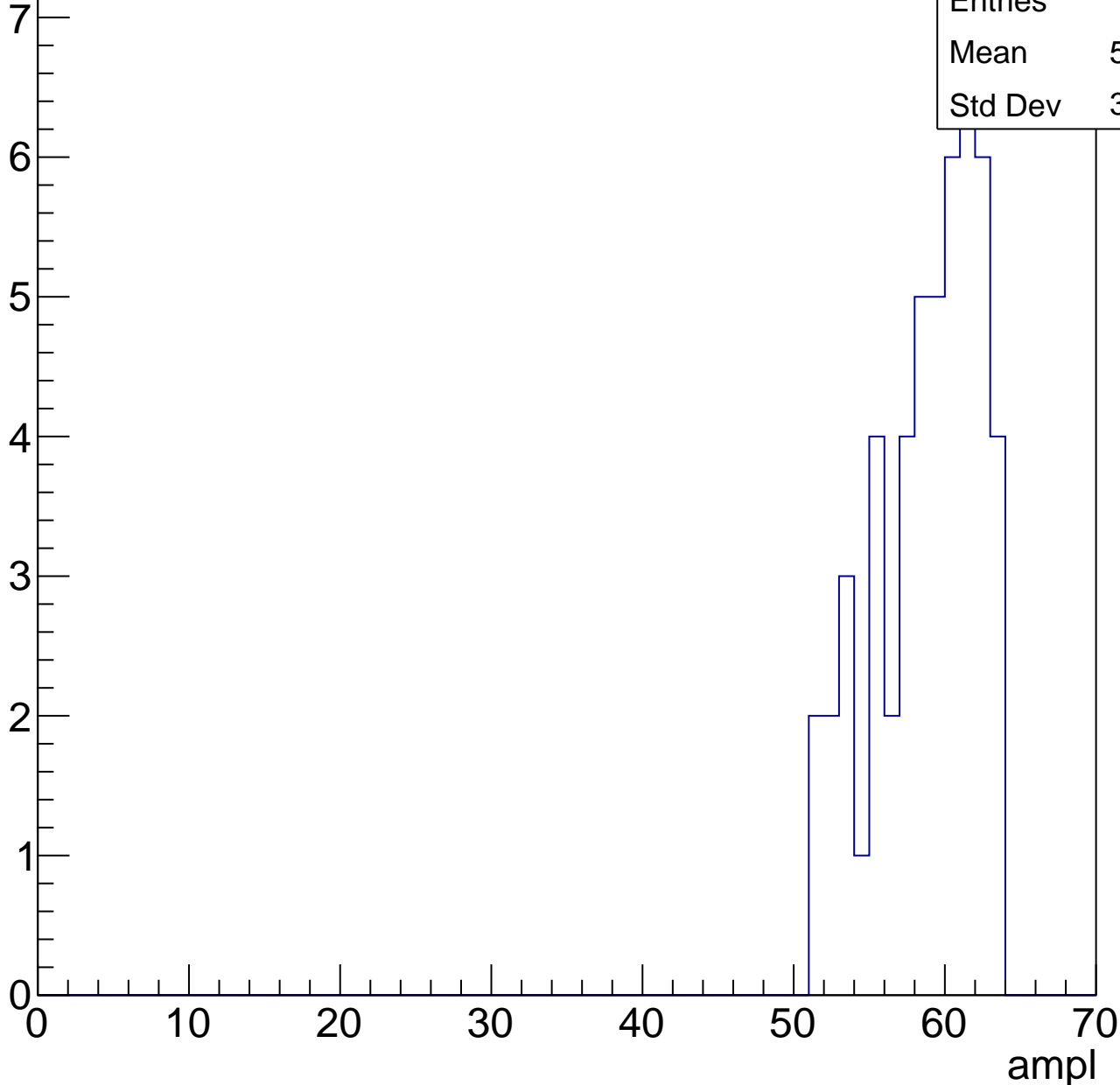


# B1L103S, U16-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	58.33
Std Dev	3.405

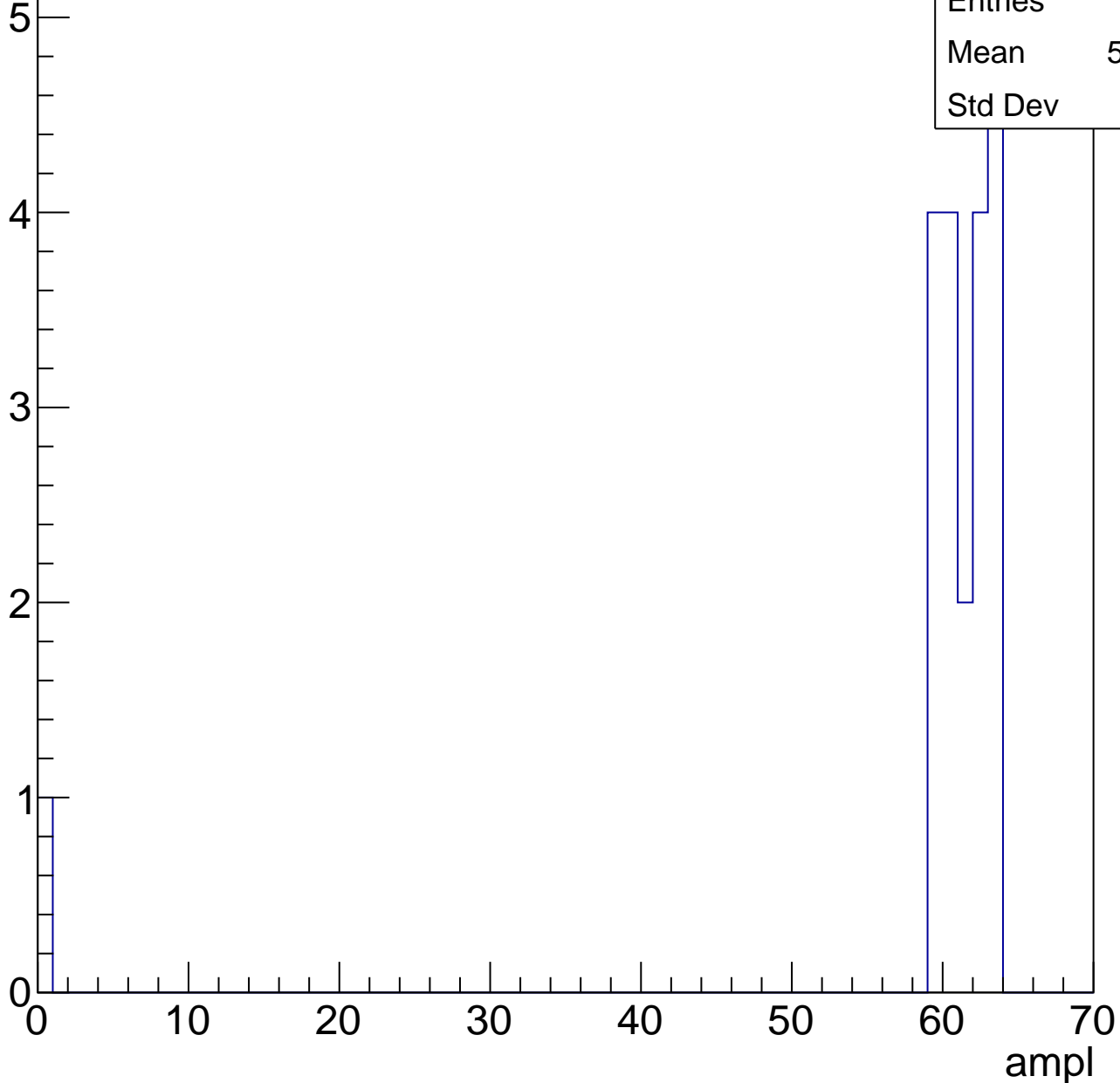


# B1L103S, U16-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	20
Mean	58.05
Std Dev	13.4

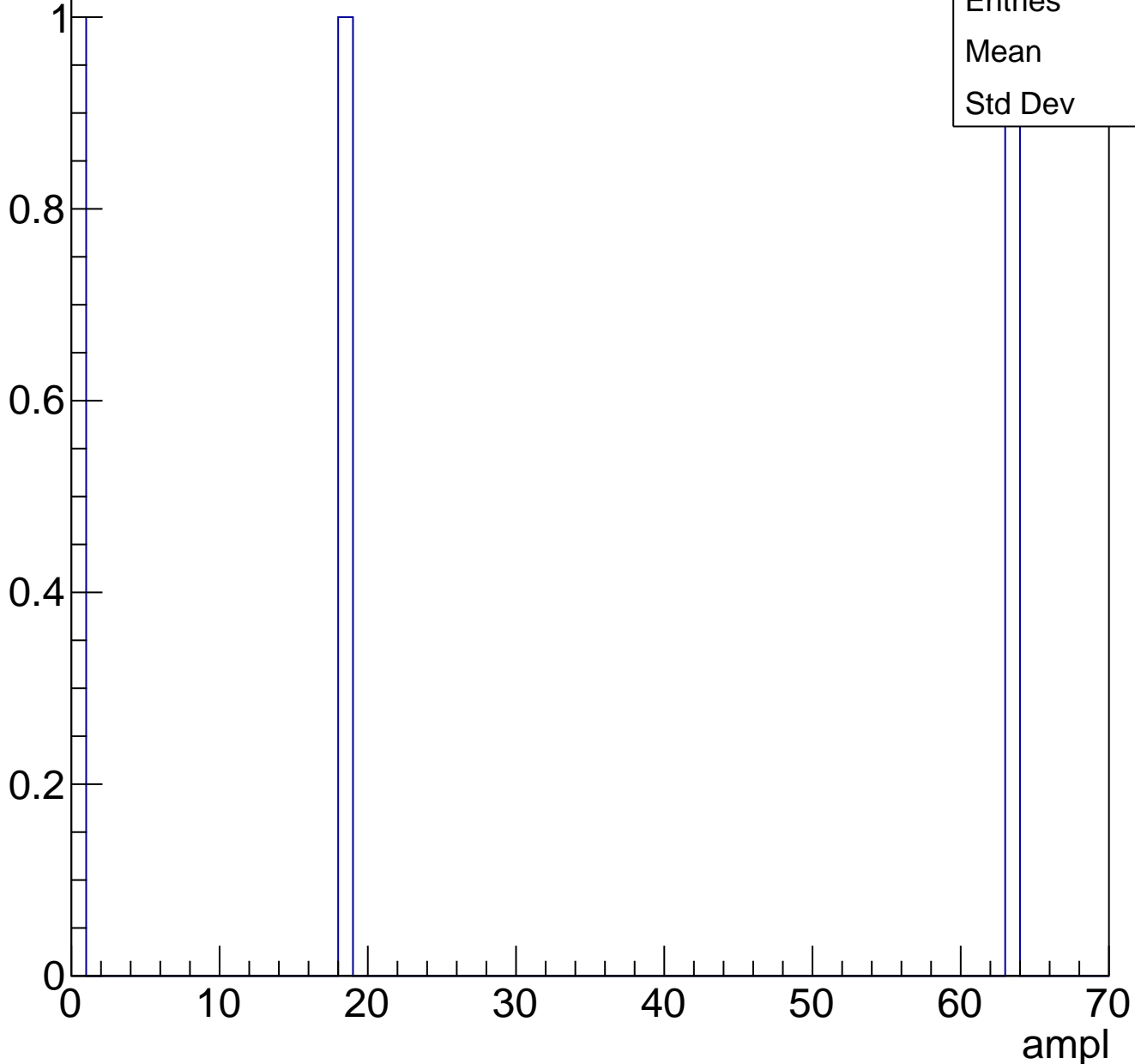




# B1L103S, U16-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch87, adc0

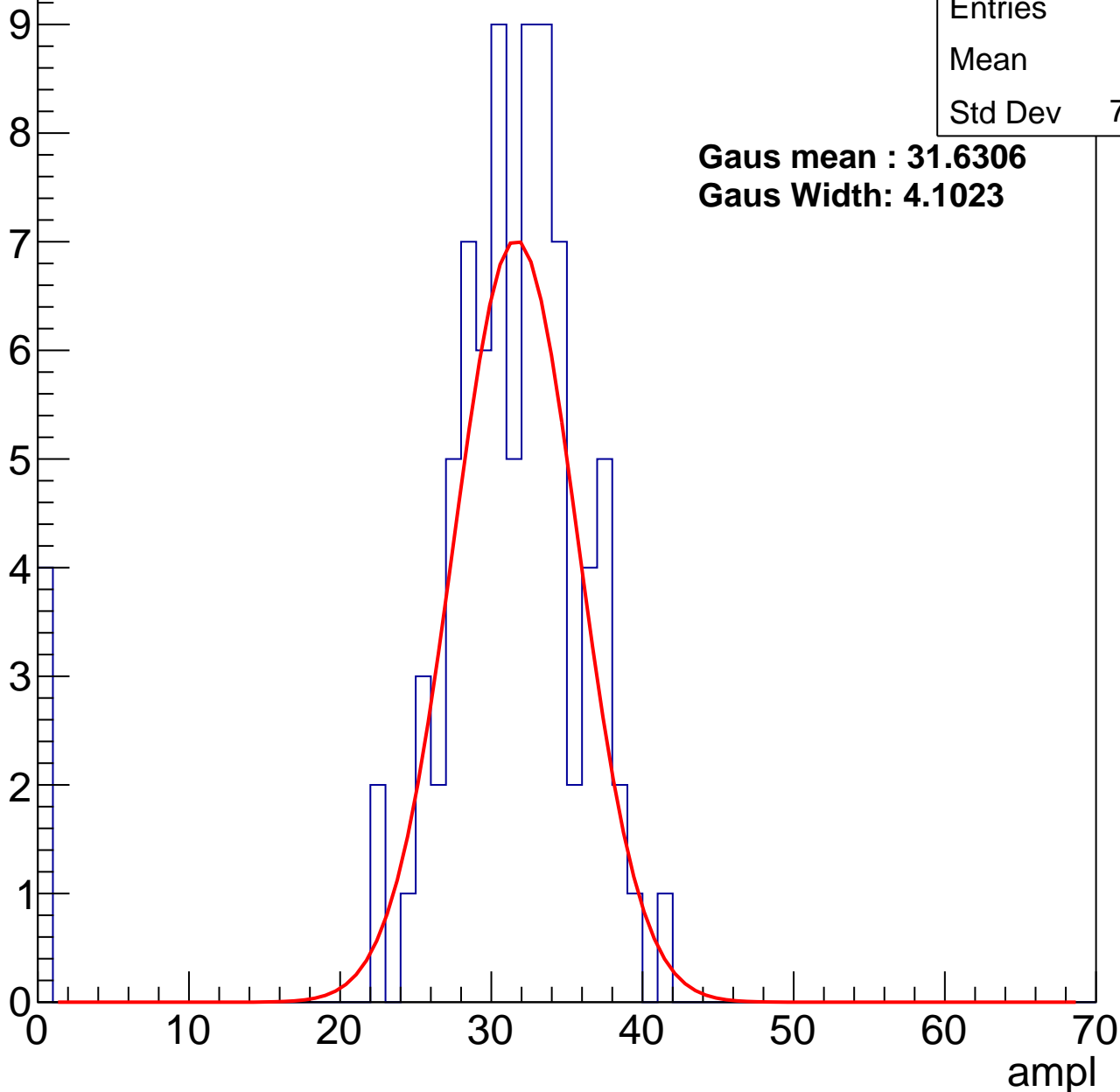
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	84
Mean	29.8
Std Dev	7.676

**Gaus mean : 31.6306**

**Gaus Width: 4.1023**



# B1L103S, U16-ch87, adc1

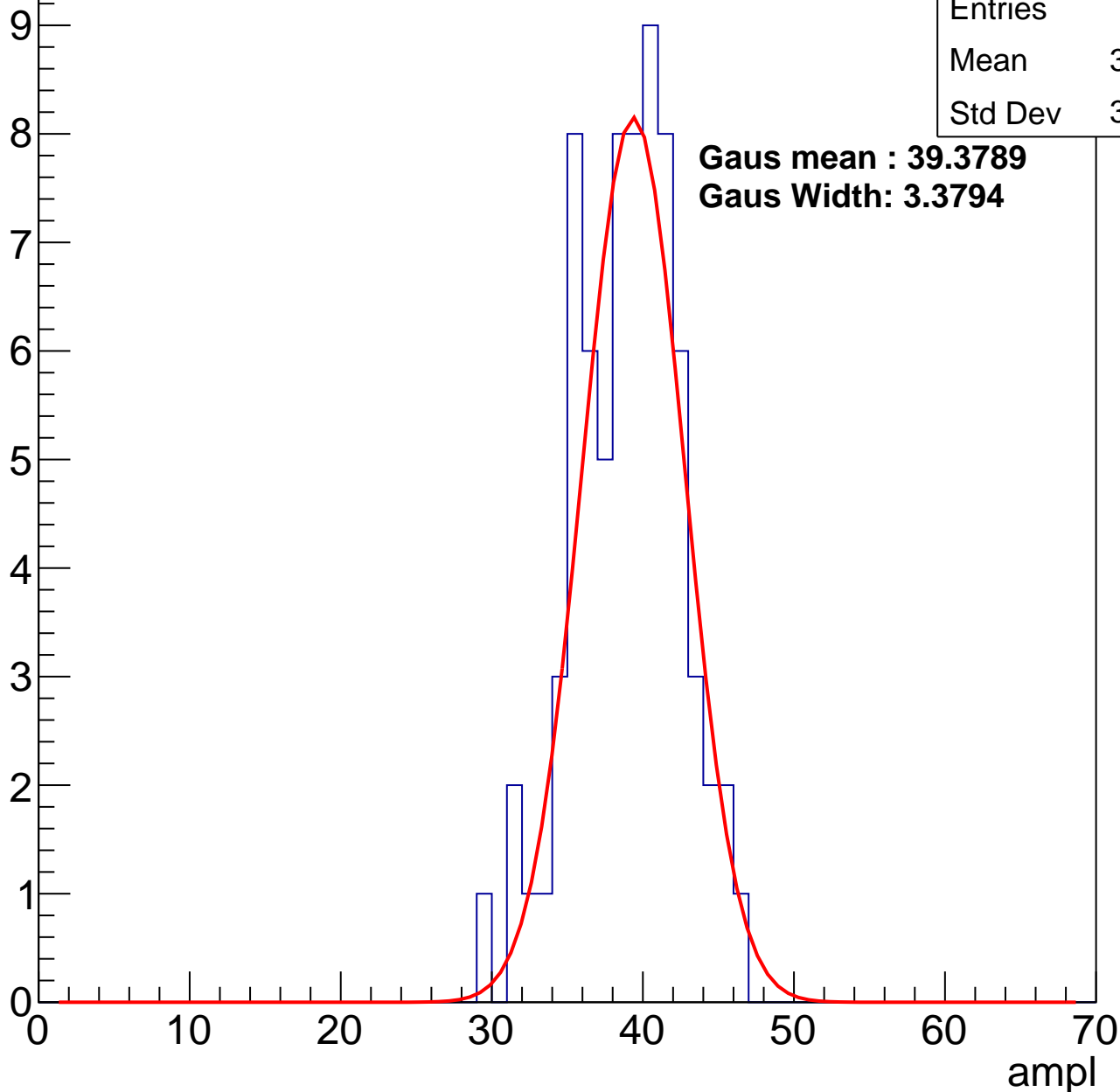
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	38.49
Std Dev	3.473

**Gaus mean : 39.3789**

**Gaus Width: 3.3794**



# B1L103S, U16-ch87, adc2

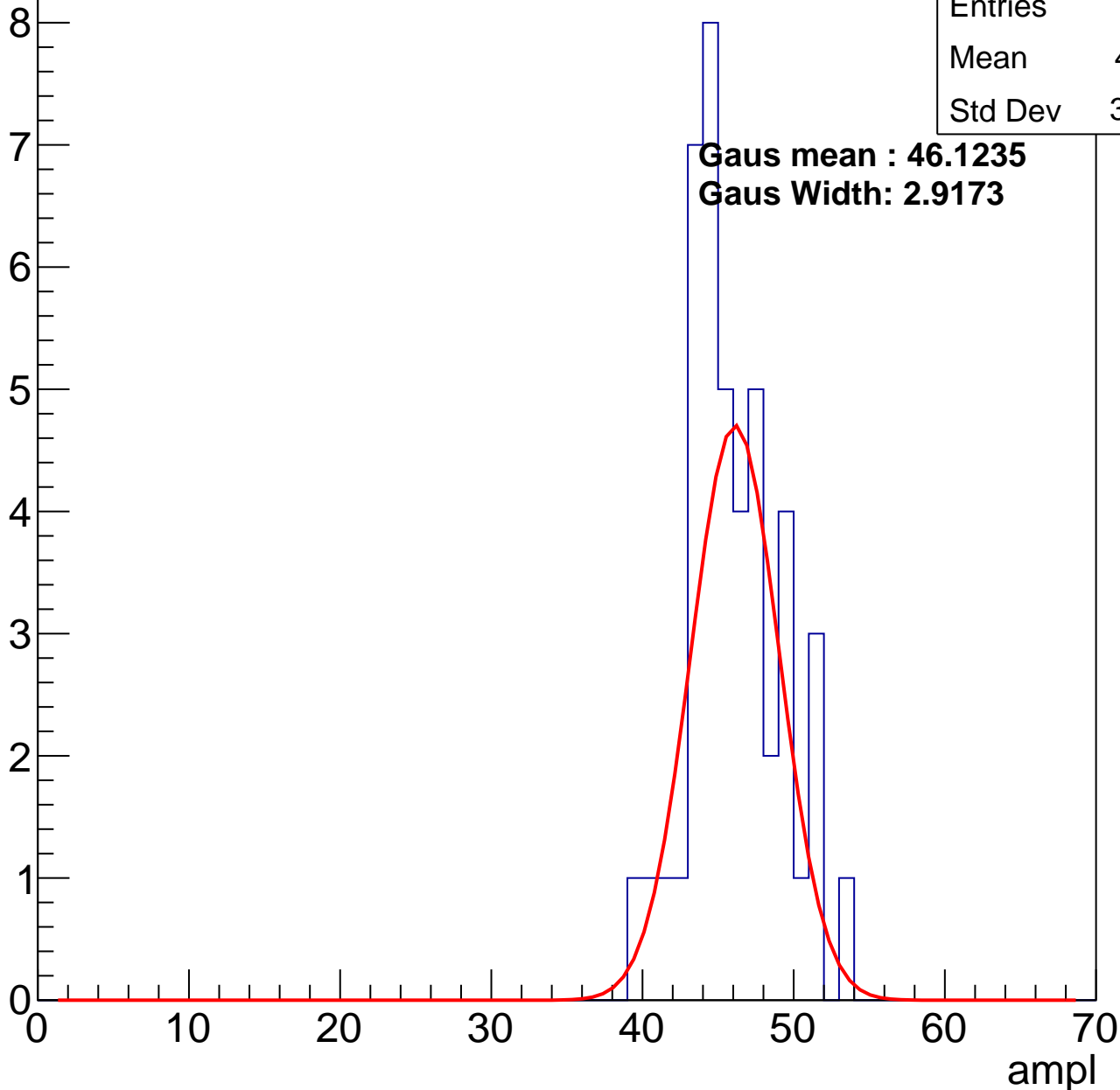
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	45.61
Std Dev	3.047

**Gaus mean : 46.1235**

**Gaus Width: 2.9173**

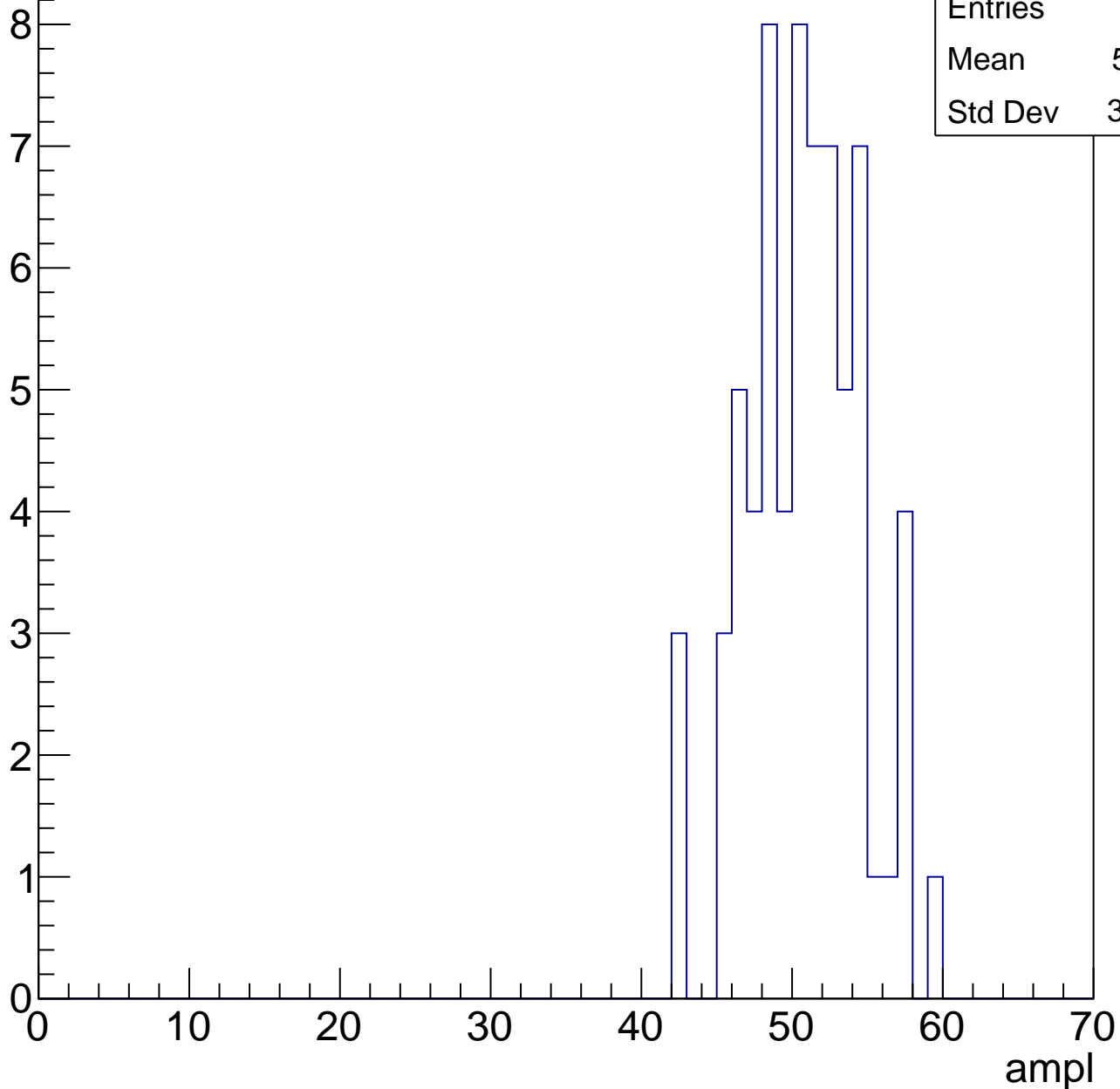


# B1L103S, U16-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	50.31
Std Dev	3.723

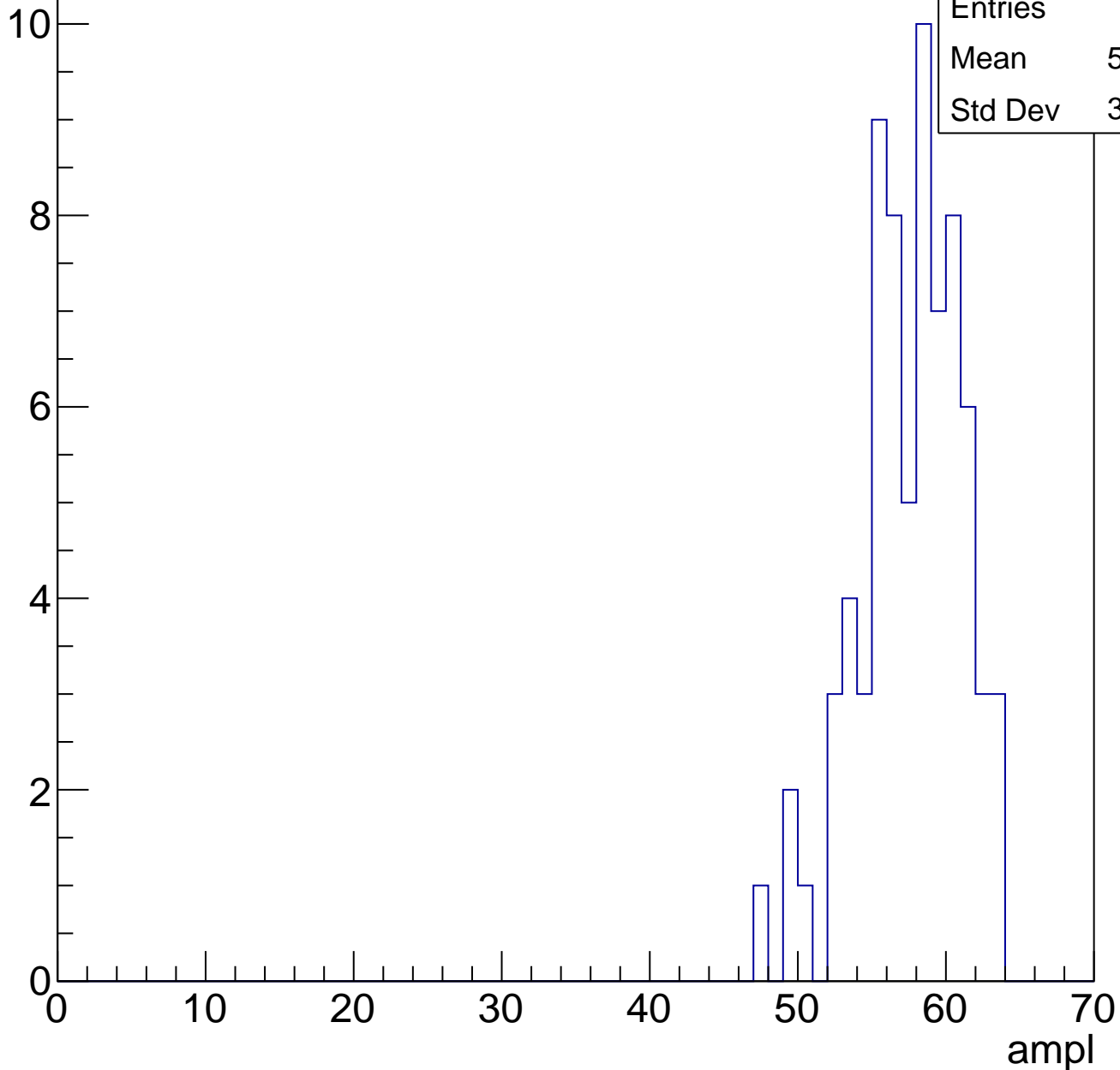


# B1L103S, U16-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	73
Mean	57.08
Std Dev	3.463

Entry

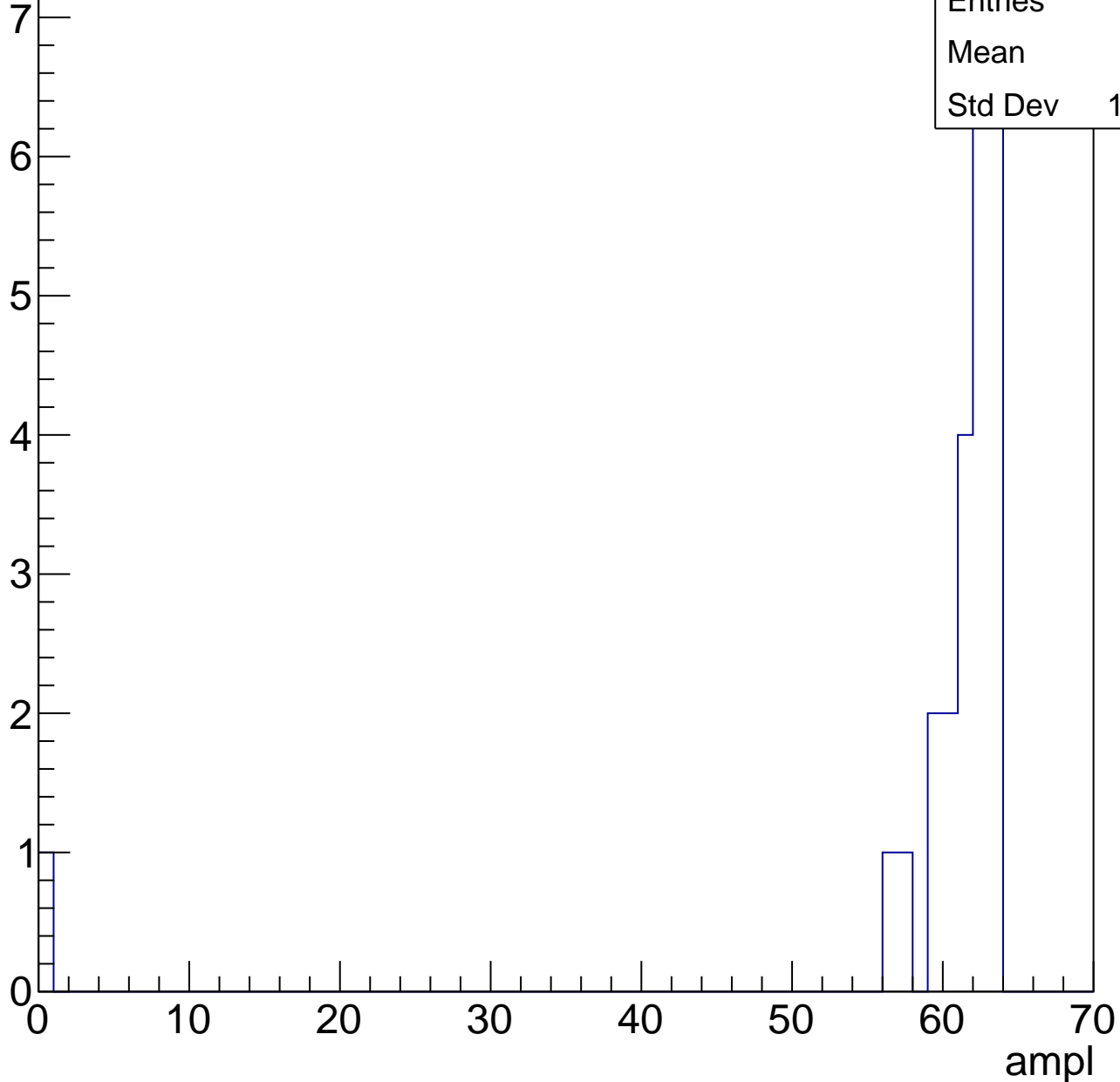


# B1L103S, U16-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	25
Mean	58.8
Std Dev	12.14



# B1L103S, U16-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L103S, U16-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch88, adc0

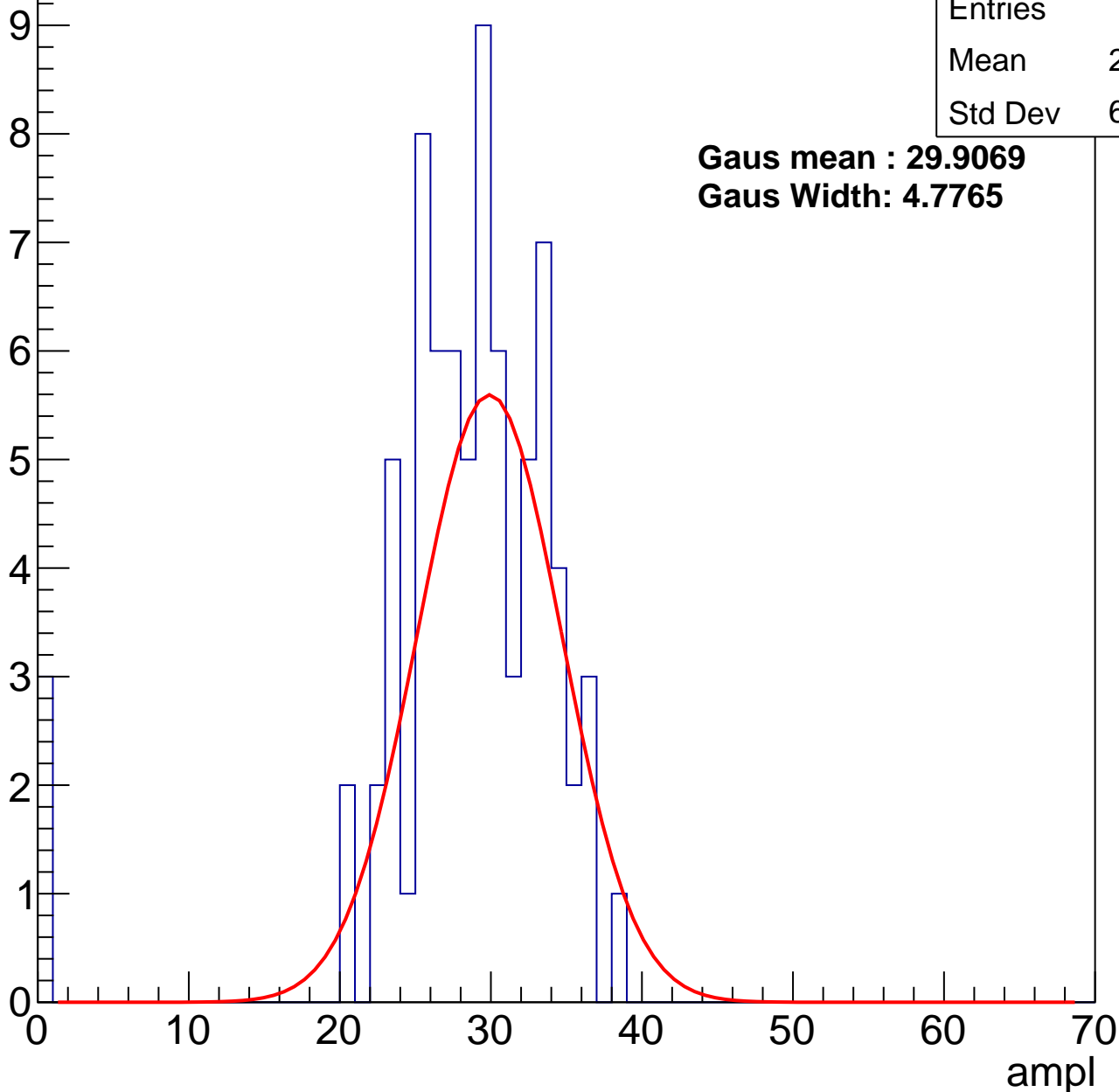
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	27.67
Std Dev	6.827

**Gaus mean : 29.9069**

**Gaus Width: 4.7765**



# B1L103S, U16-ch88, adc1

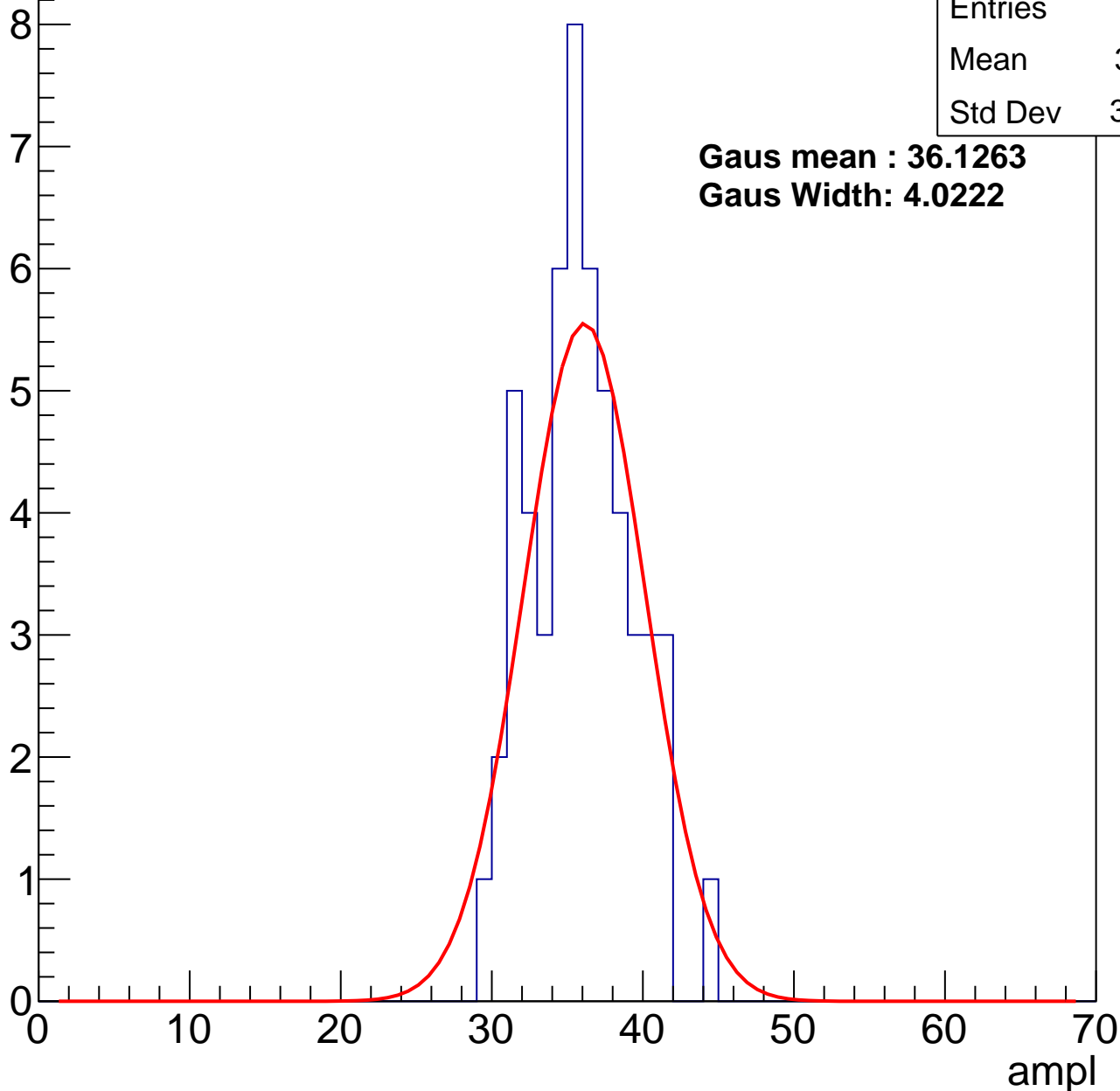
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	35.41
Std Dev	3.292

**Gaus mean : 36.1263**

**Gaus Width: 4.0222**



# B1L103S, U16-ch88, adc2

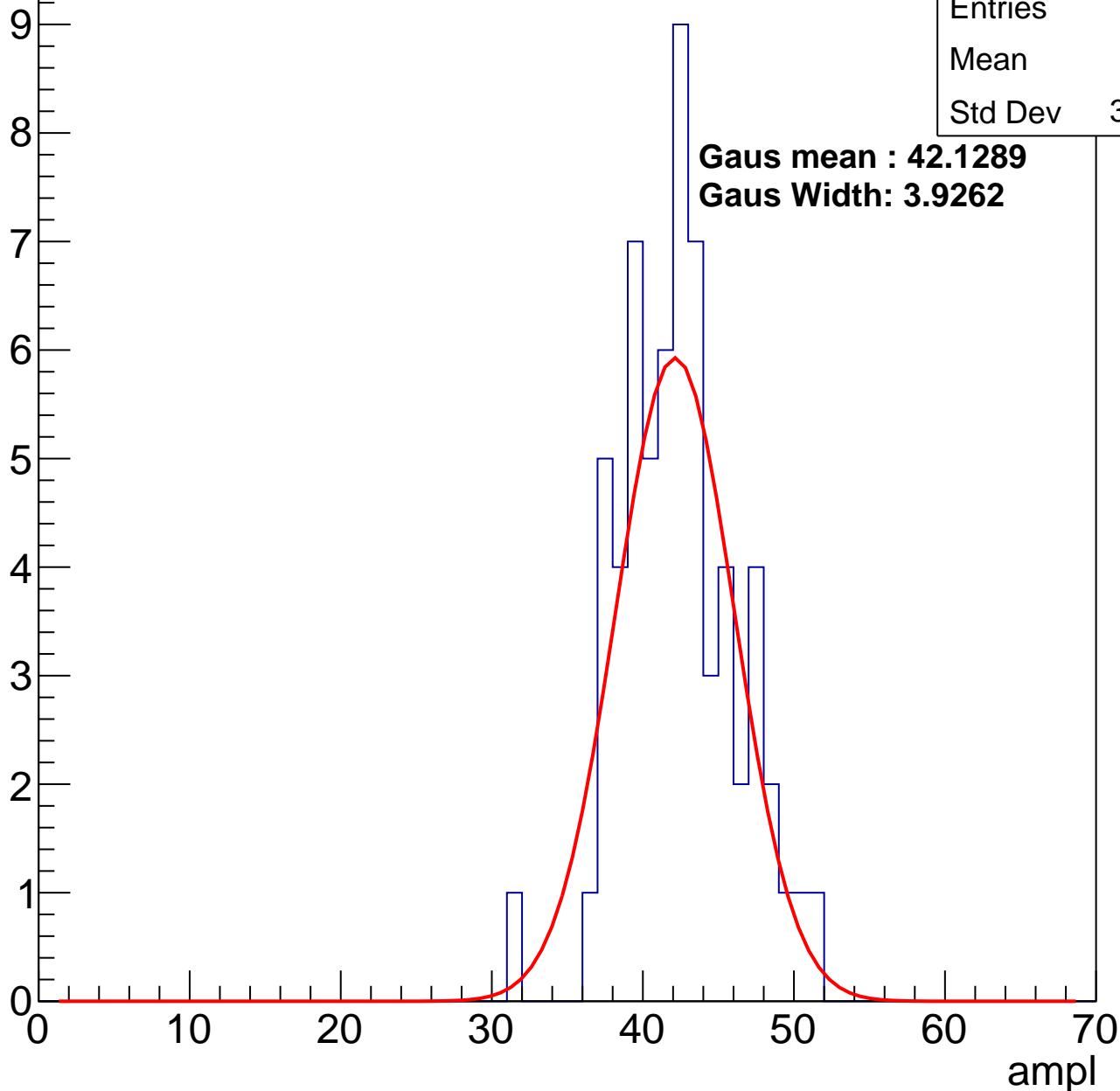
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	41.9
Std Dev	3.753

**Gaus mean : 42.1289**

**Gaus Width: 3.9262**

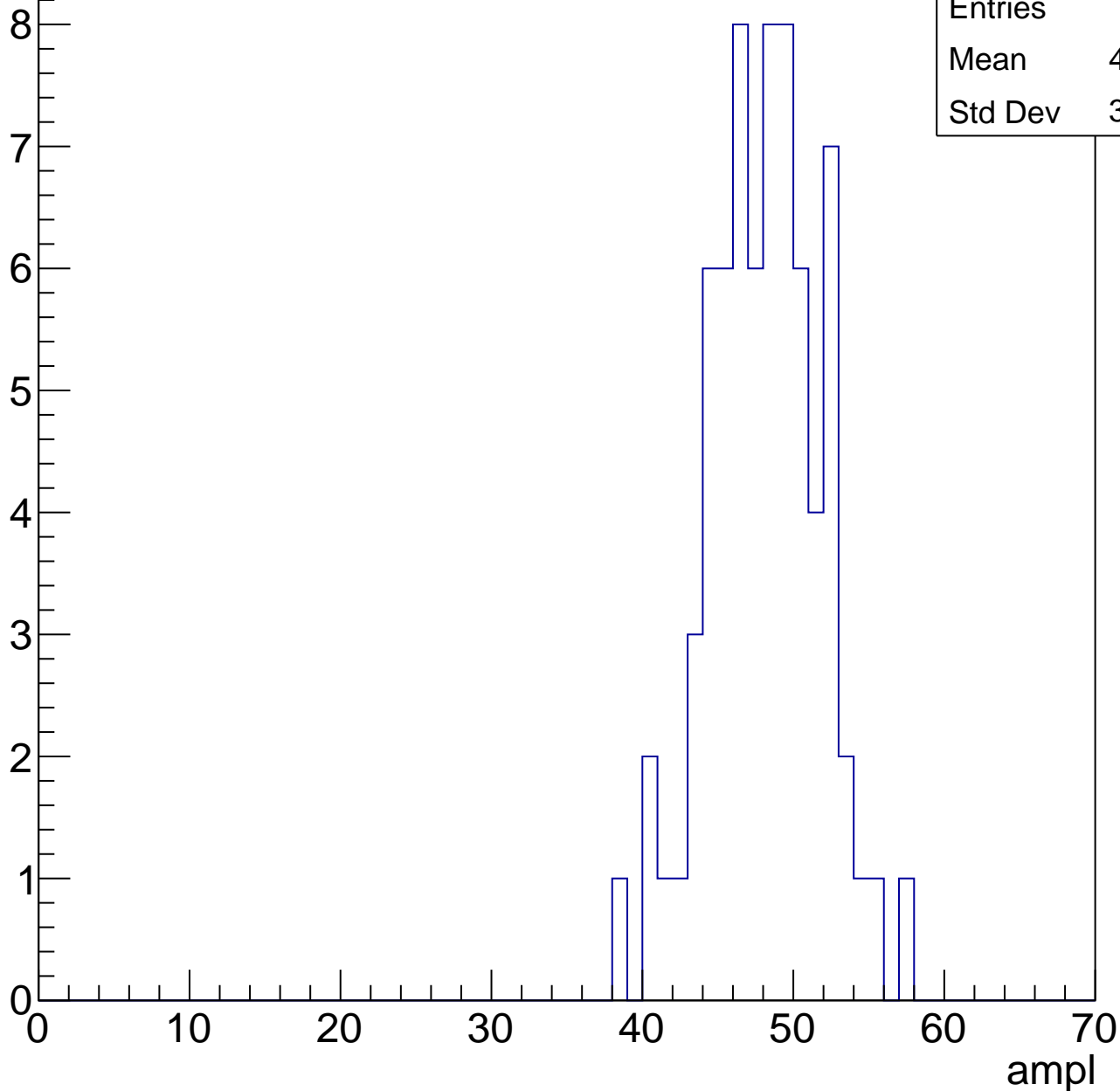


# B1L103S, U16-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	47.64
Std Dev	3.656

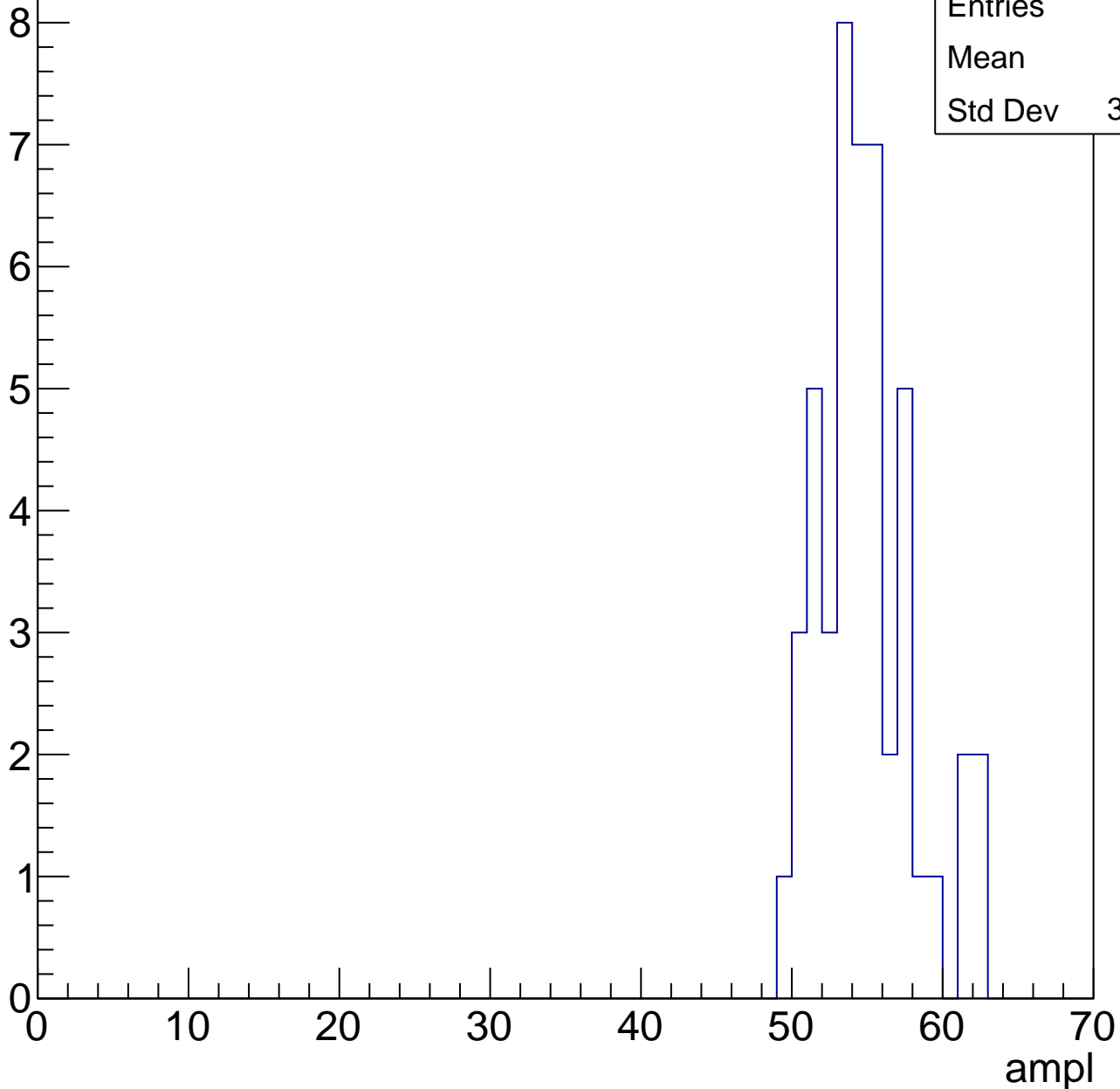


# B1L103S, U16-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

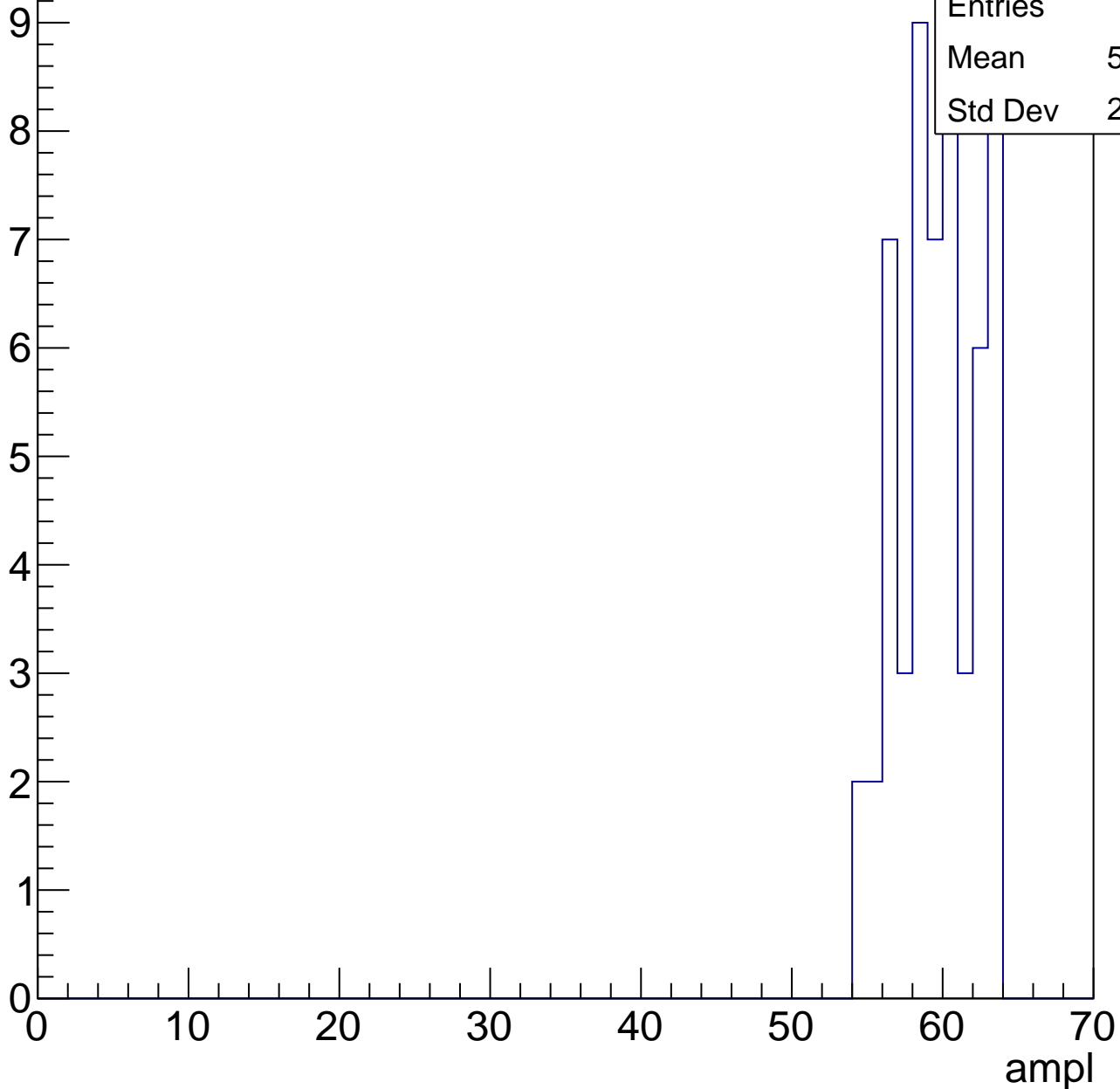
Entries	47
Mean	54.4
Std Dev	3.119



# B1L103S, U16-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

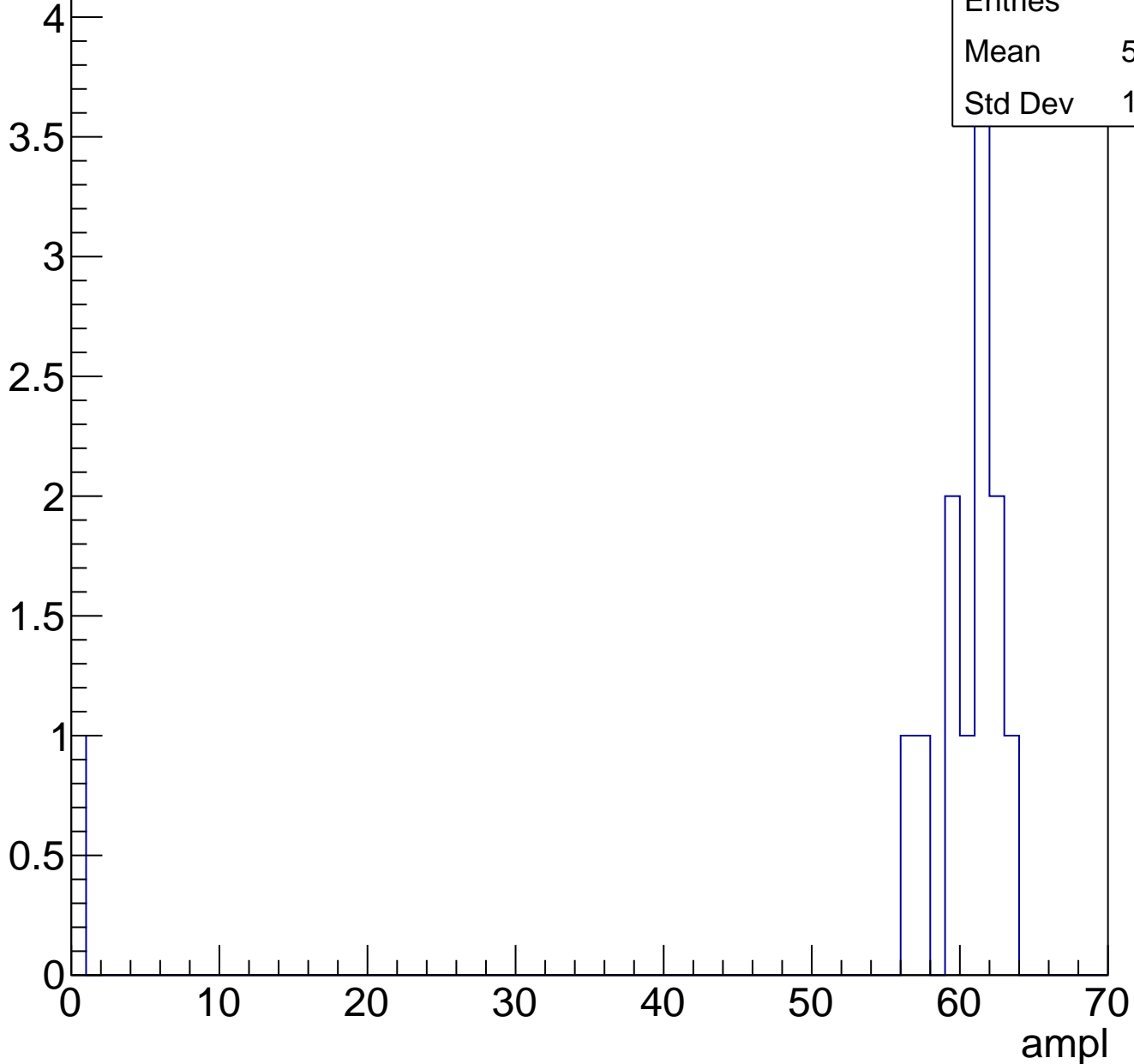


Entries	57
Mean	59.26
Std Dev	2.586

# B1L103S, U16-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

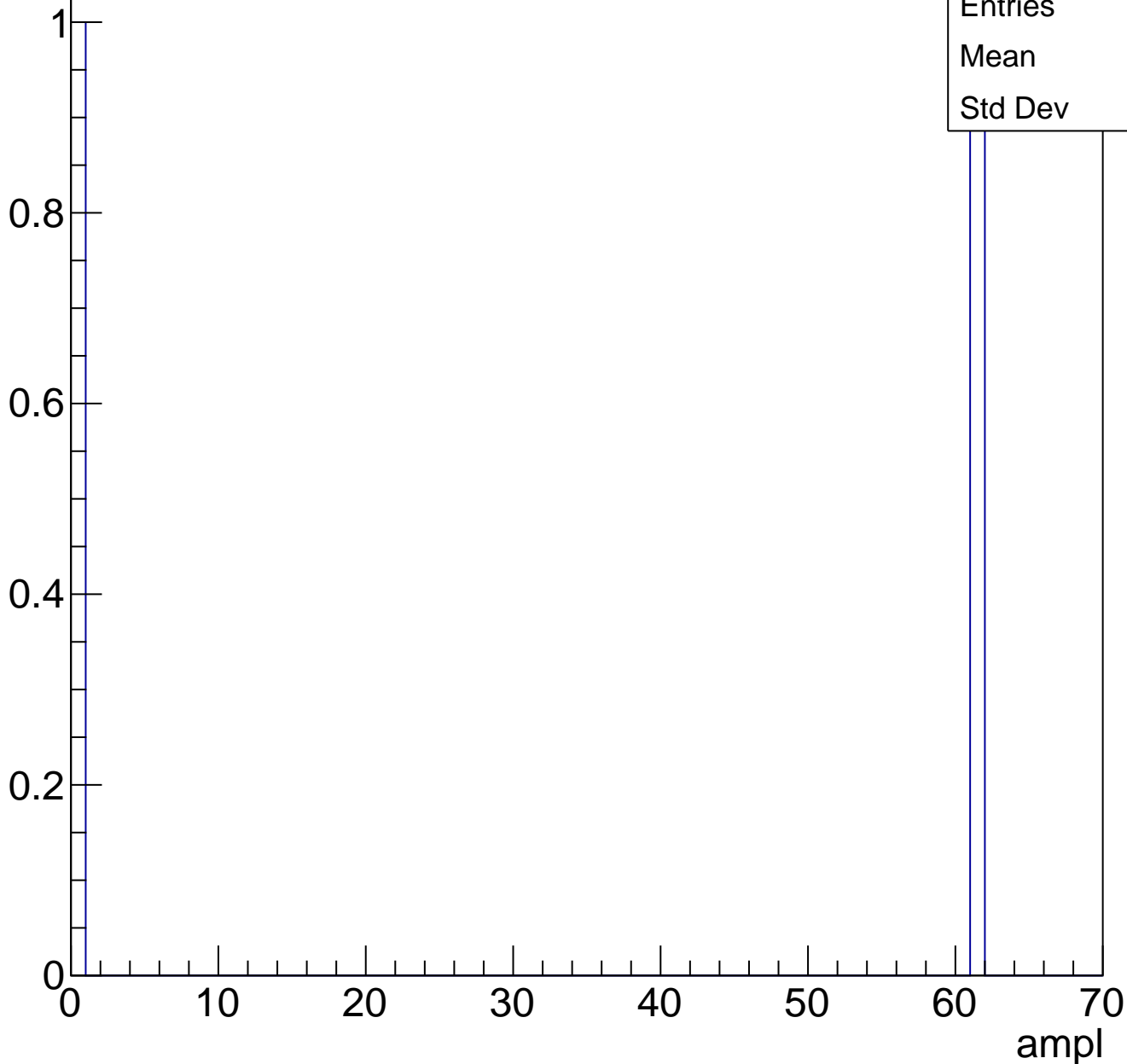




# B1L103S, U16-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch89, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	95
Mean	30.71
Std Dev	4.157

**Gaus mean : 31.4779**

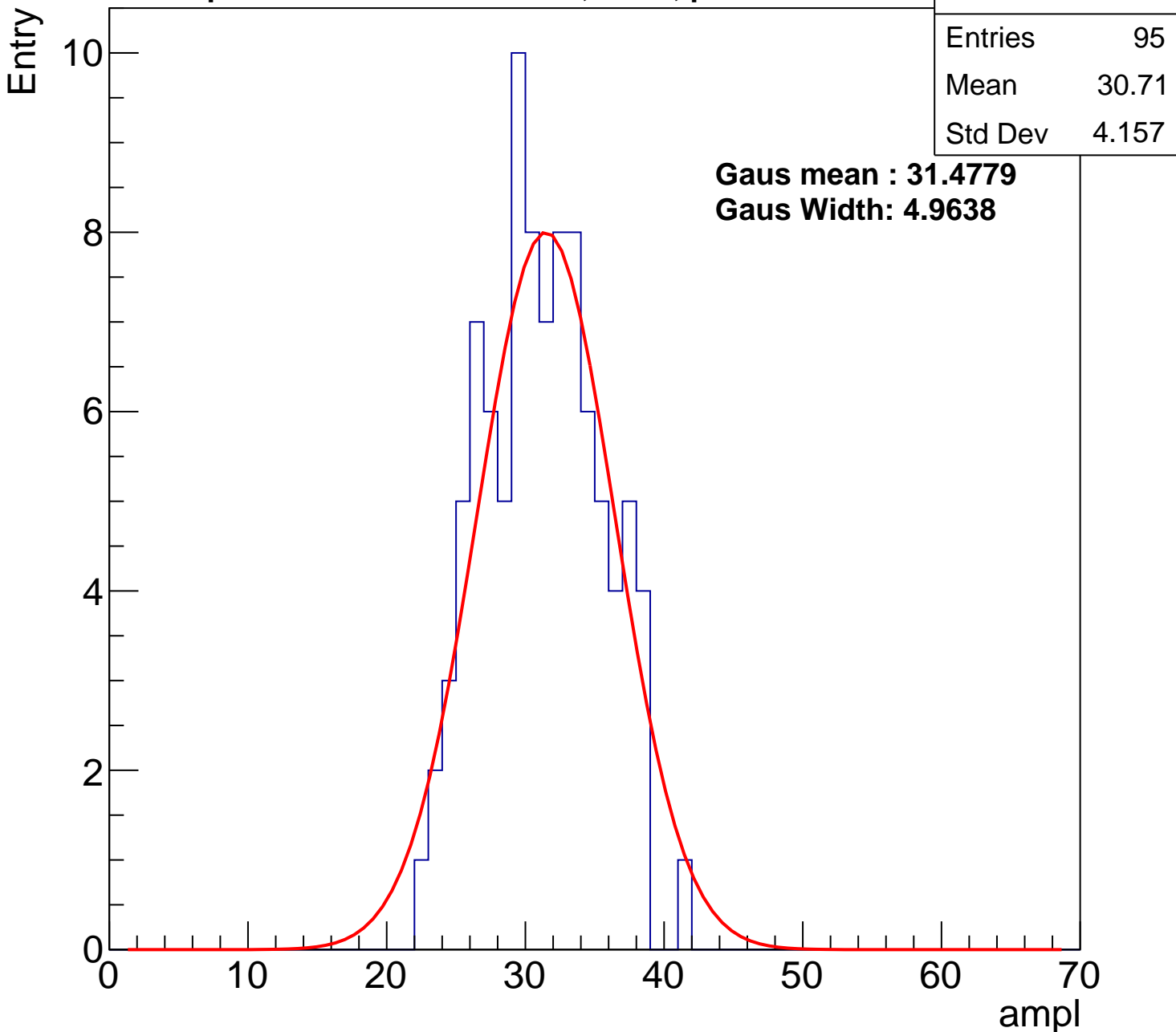
**Gaus Width: 4.9638**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U16-ch89, adc1

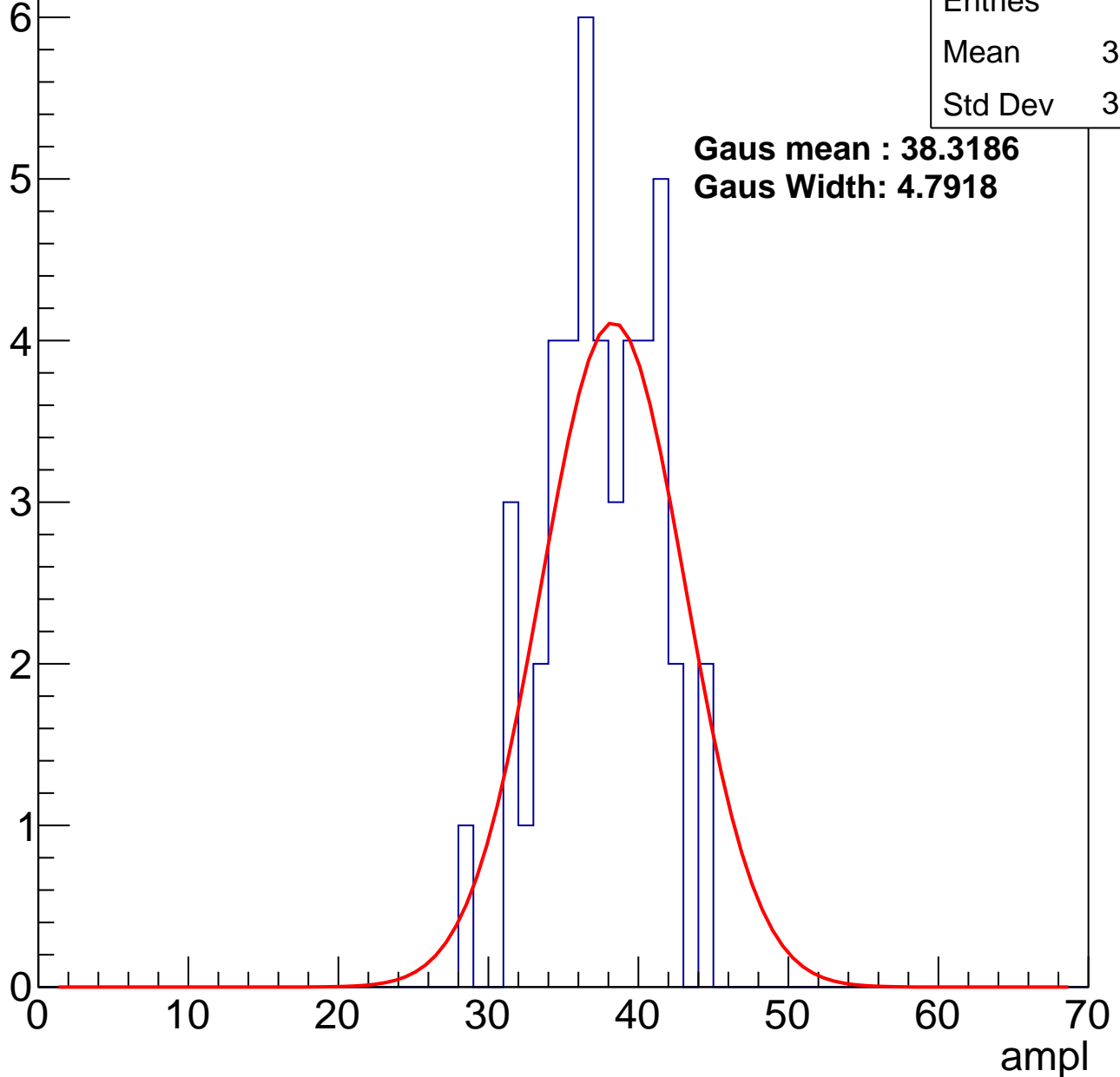
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	37.02
Std Dev	3.612

**Gaus mean : 38.3186**

**Gaus Width: 4.7918**



# B1L103S, U16-ch89, adc2

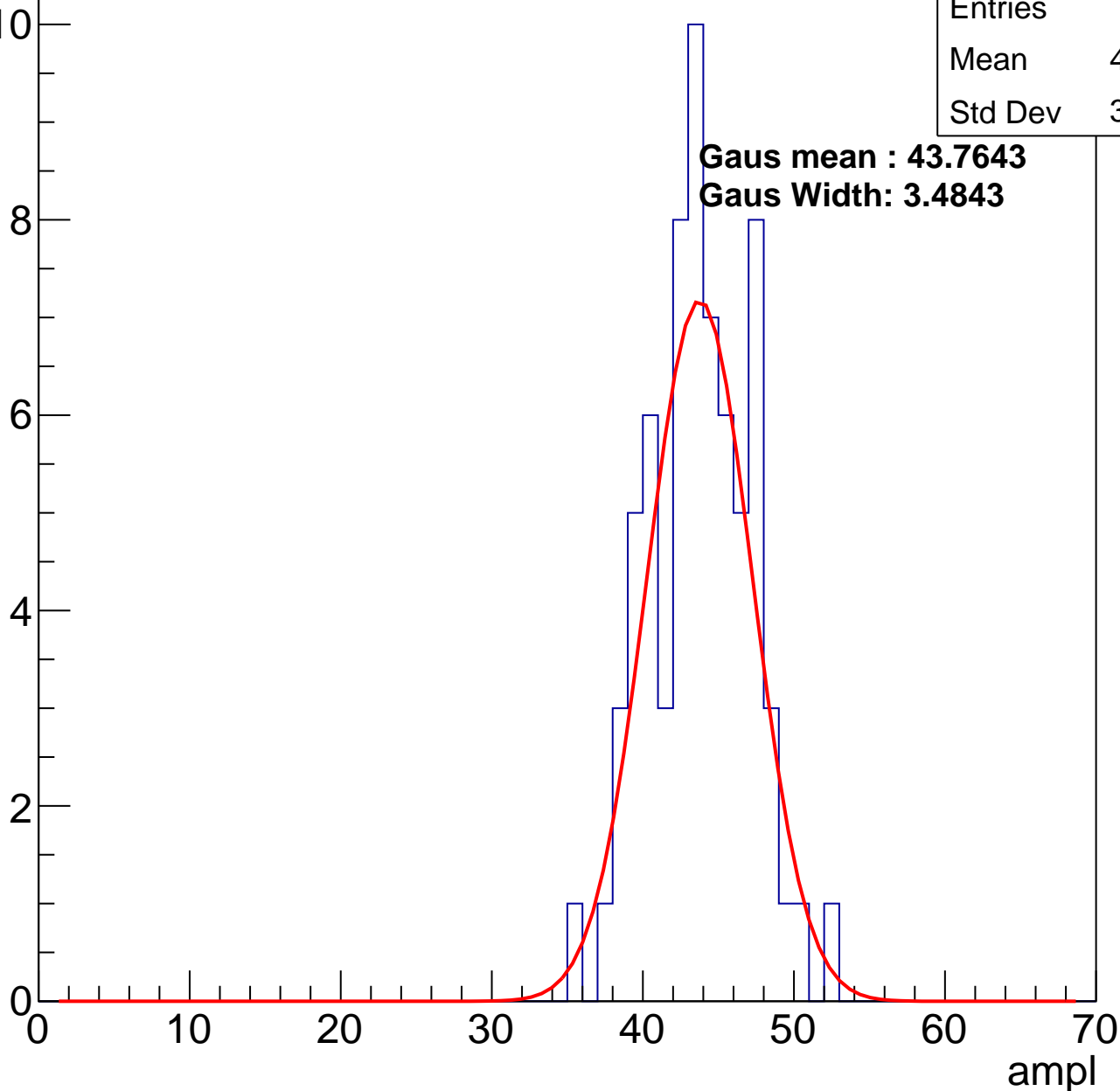
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	43.32
Std Dev	3.334

**Gaus mean : 43.7643**

**Gaus Width: 3.4843**

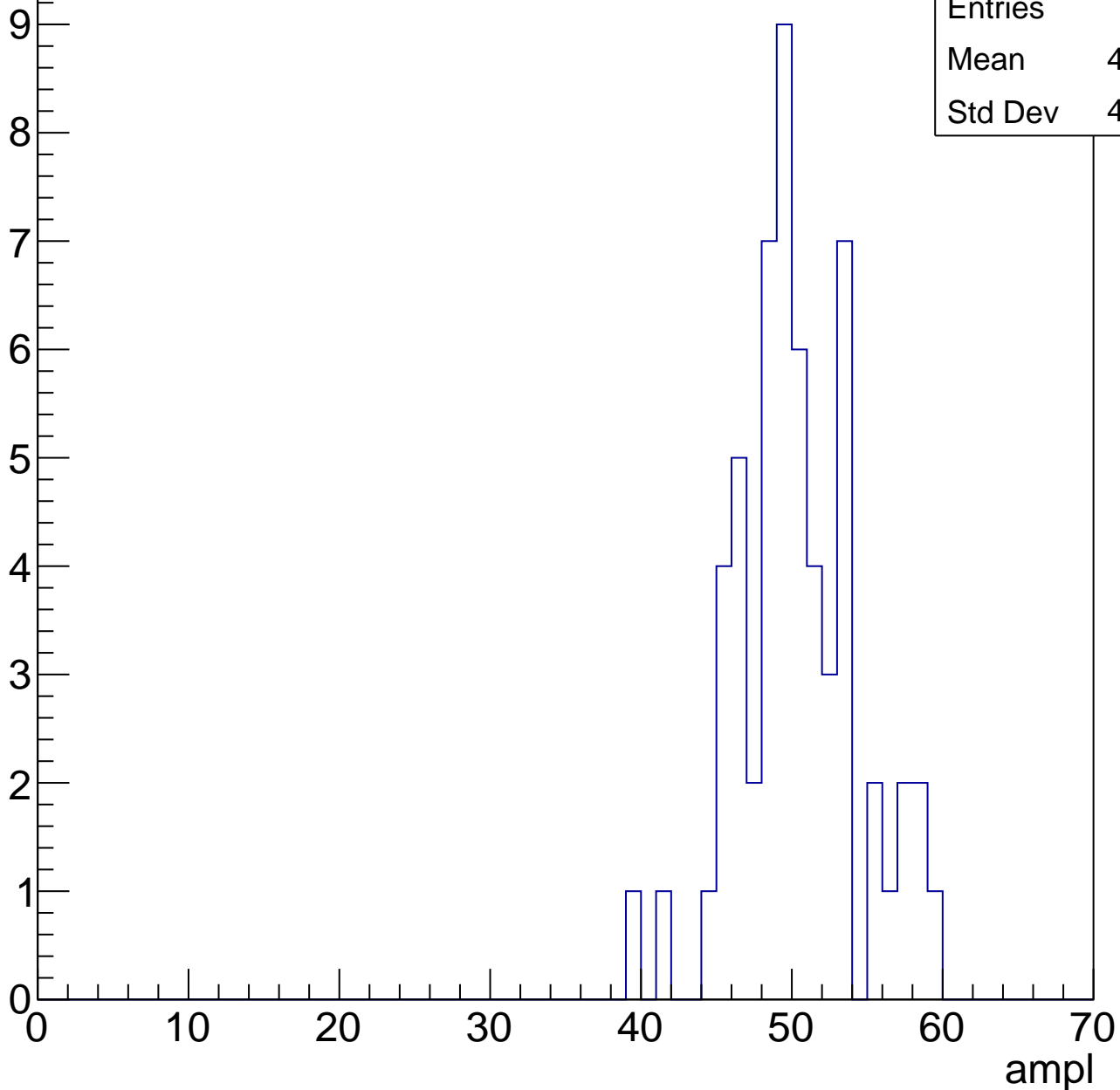


# B1L103S, U16-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	49.84
Std Dev	4.033

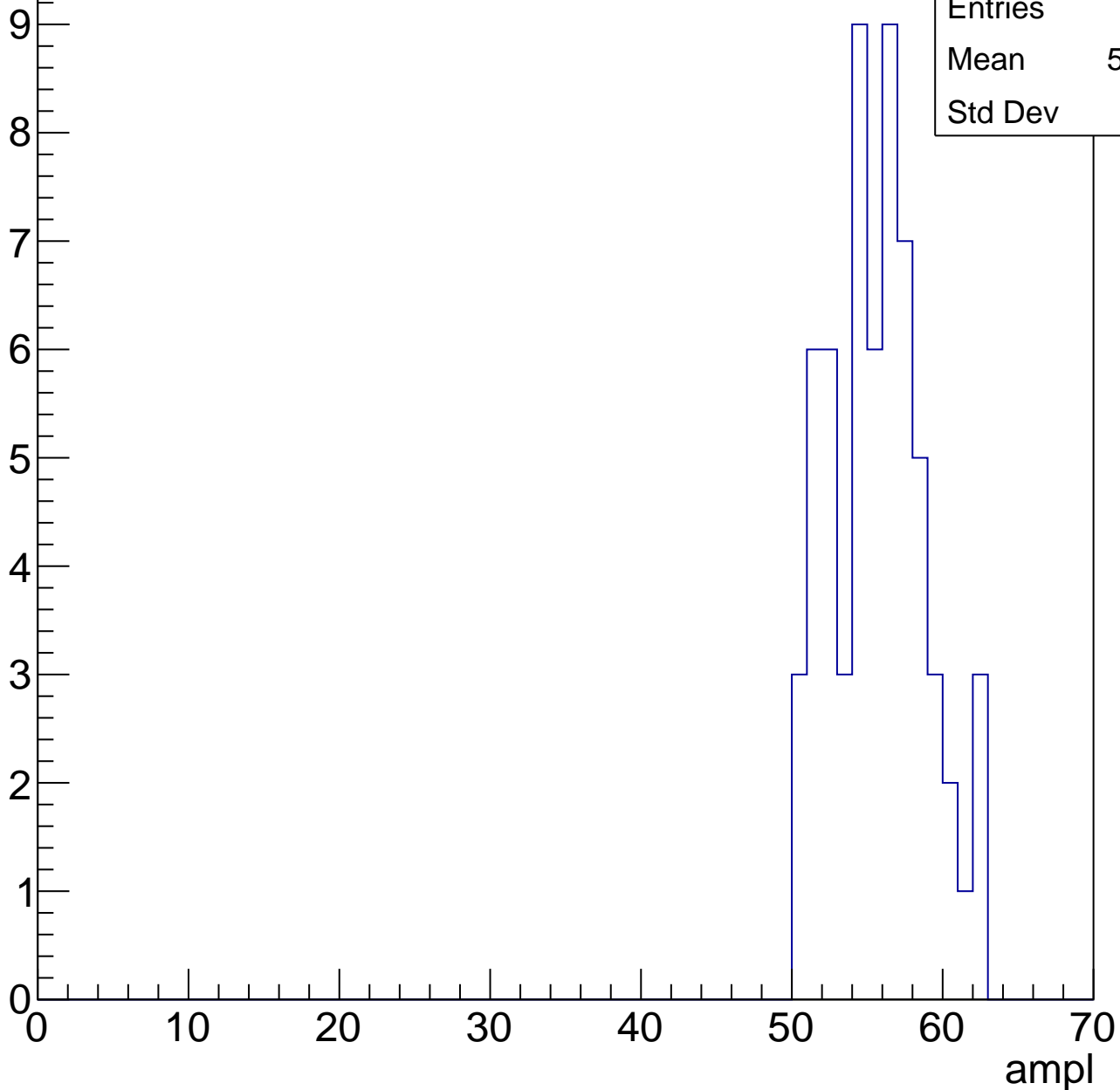


# B1L103S, U16-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	55.24
Std Dev	3.1

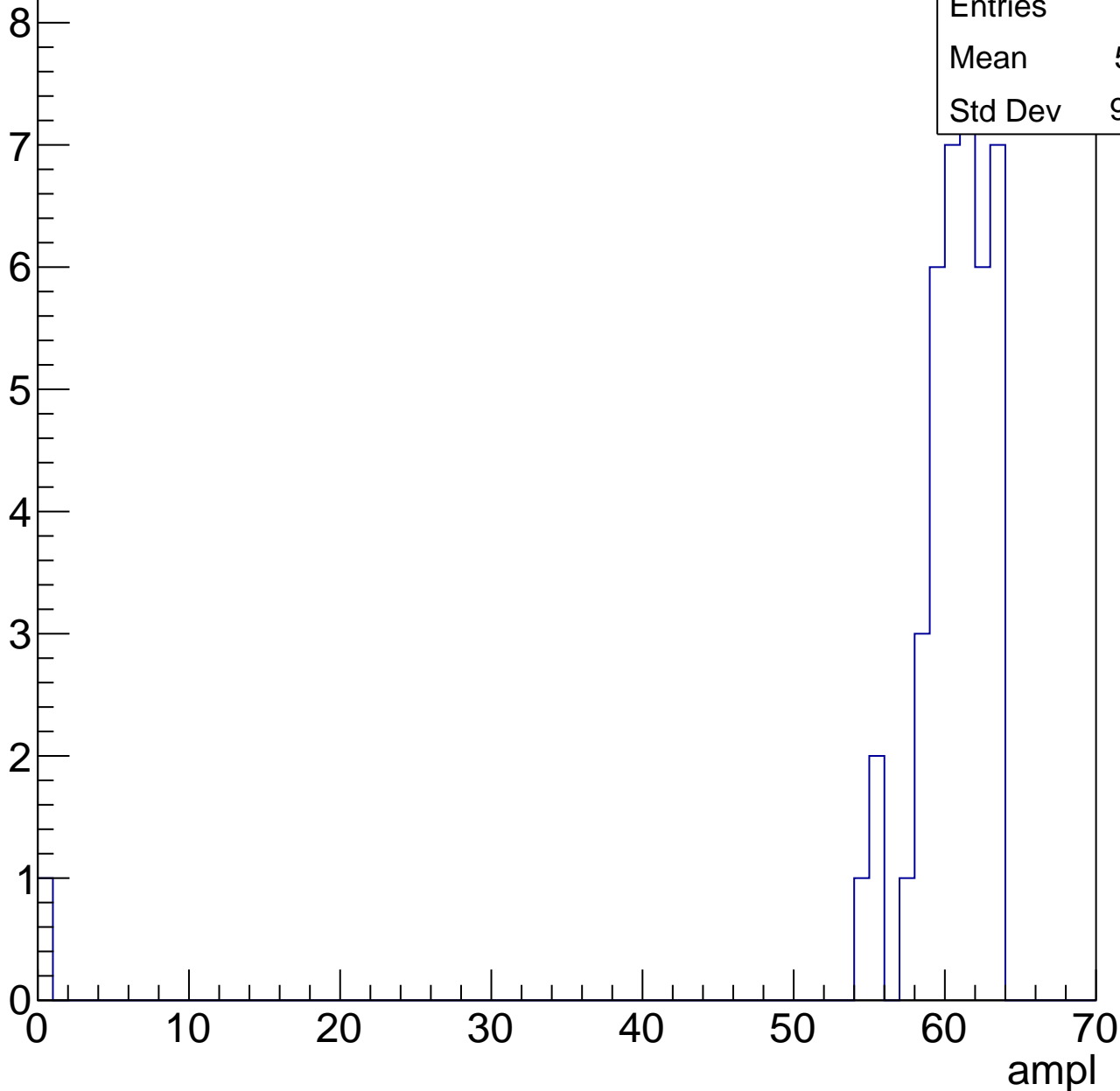


# B1L103S, U16-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	42
Mean	58.81
Std Dev	9.447



# B1L103S, U16-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	63
Std Dev	0

# B1L103S, U16-ch90, adc0

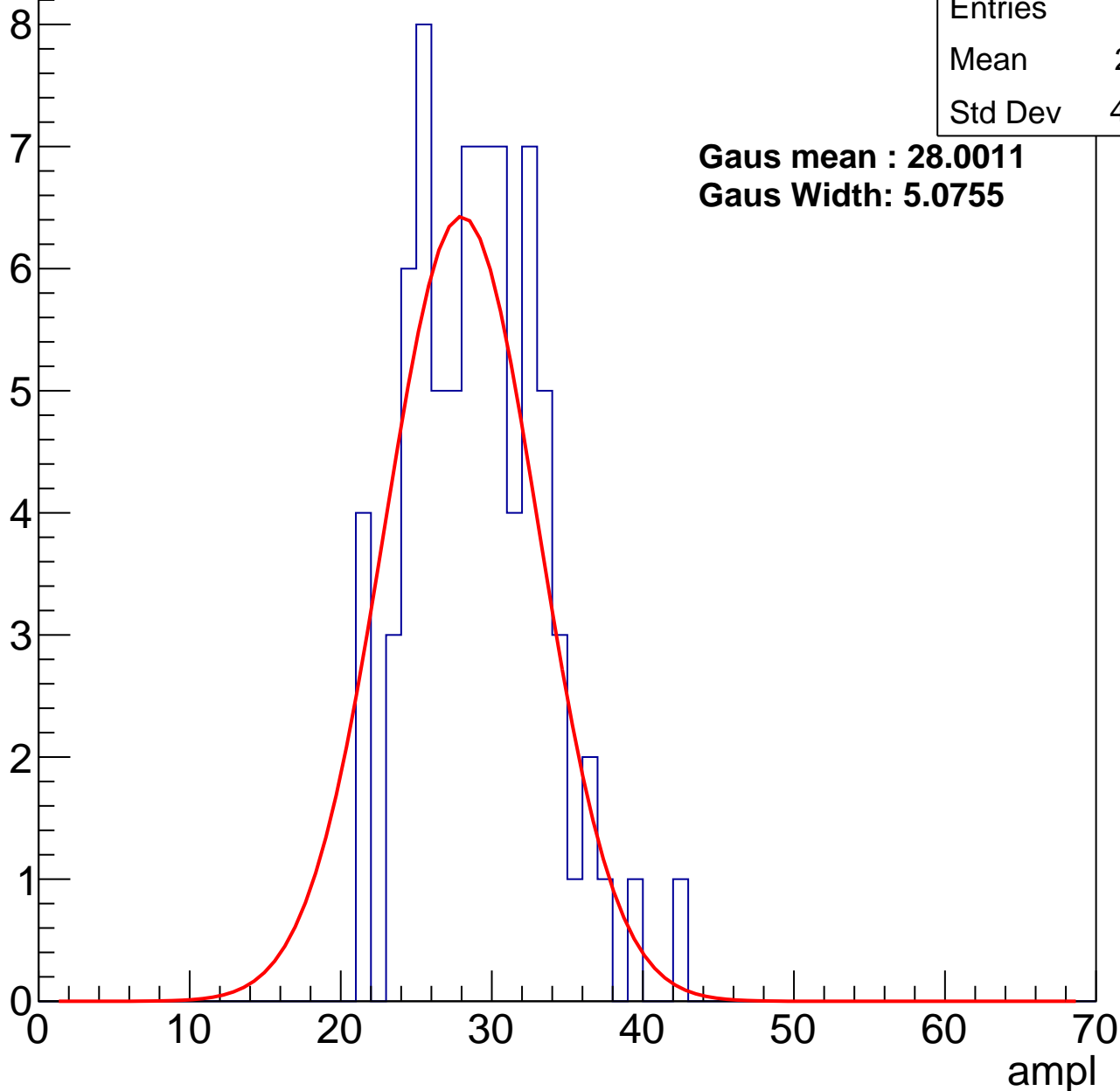
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	28.71
Std Dev	4.288

**Gaus mean : 28.0011**

**Gaus Width: 5.0755**



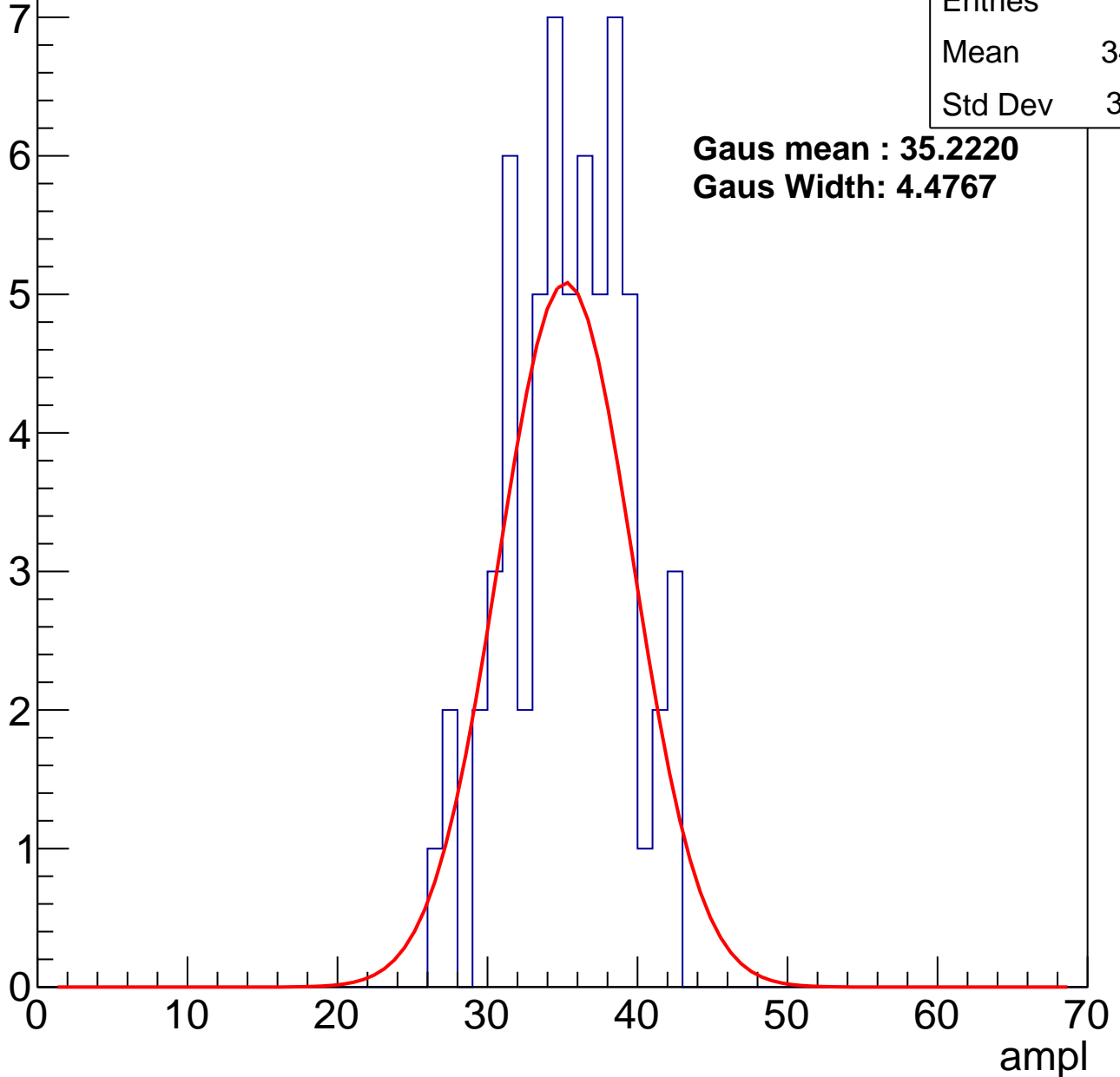
# B1L103S, U16-ch90, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	34.94
Std Dev	3.831

**Gaus mean : 35.2220**  
**Gaus Width: 4.4767**



# B1L103S, U16-ch90, adc2

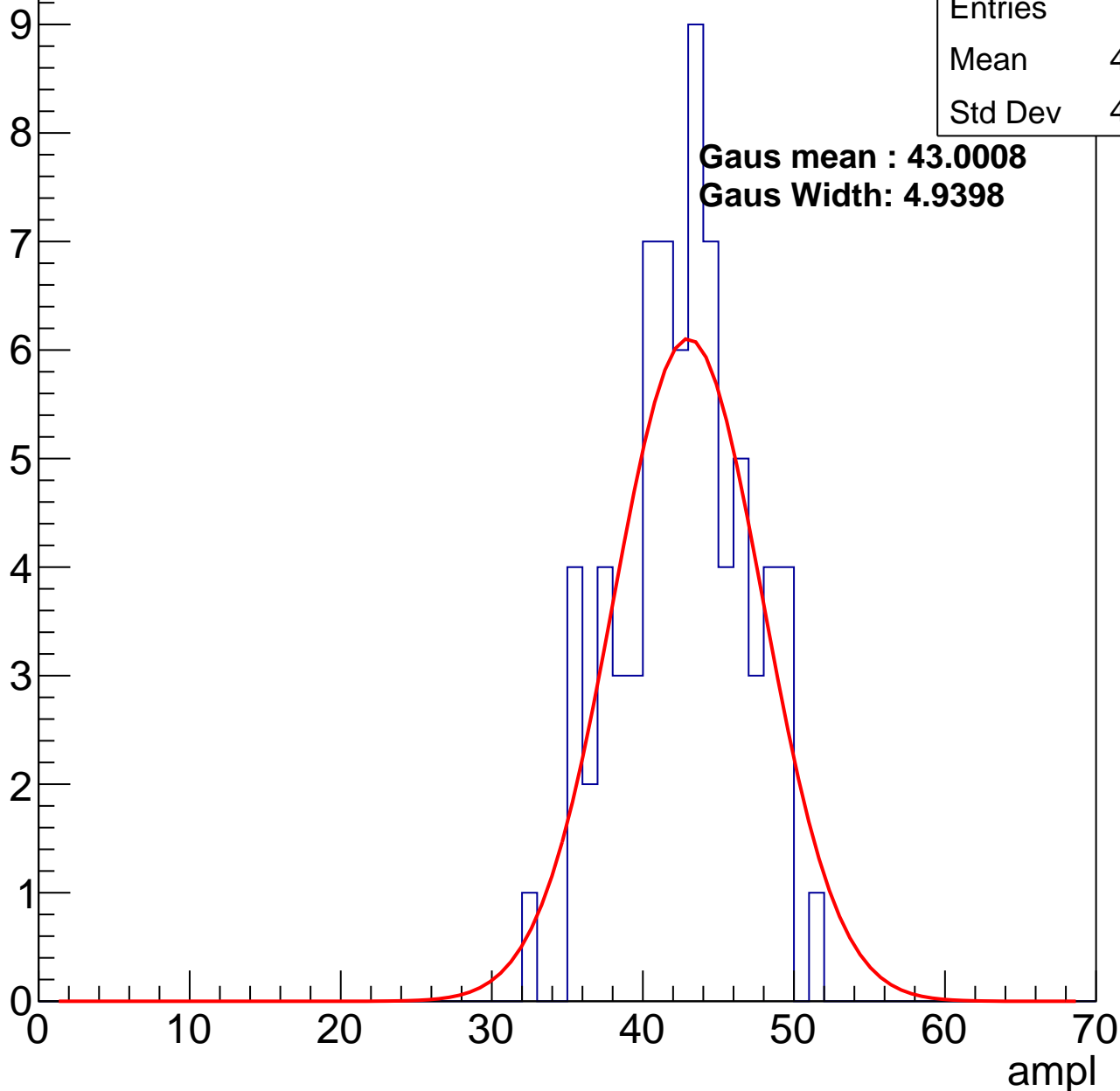
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	42.26
Std Dev	4.064

**Gaus mean : 43.0008**

**Gaus Width: 4.9398**

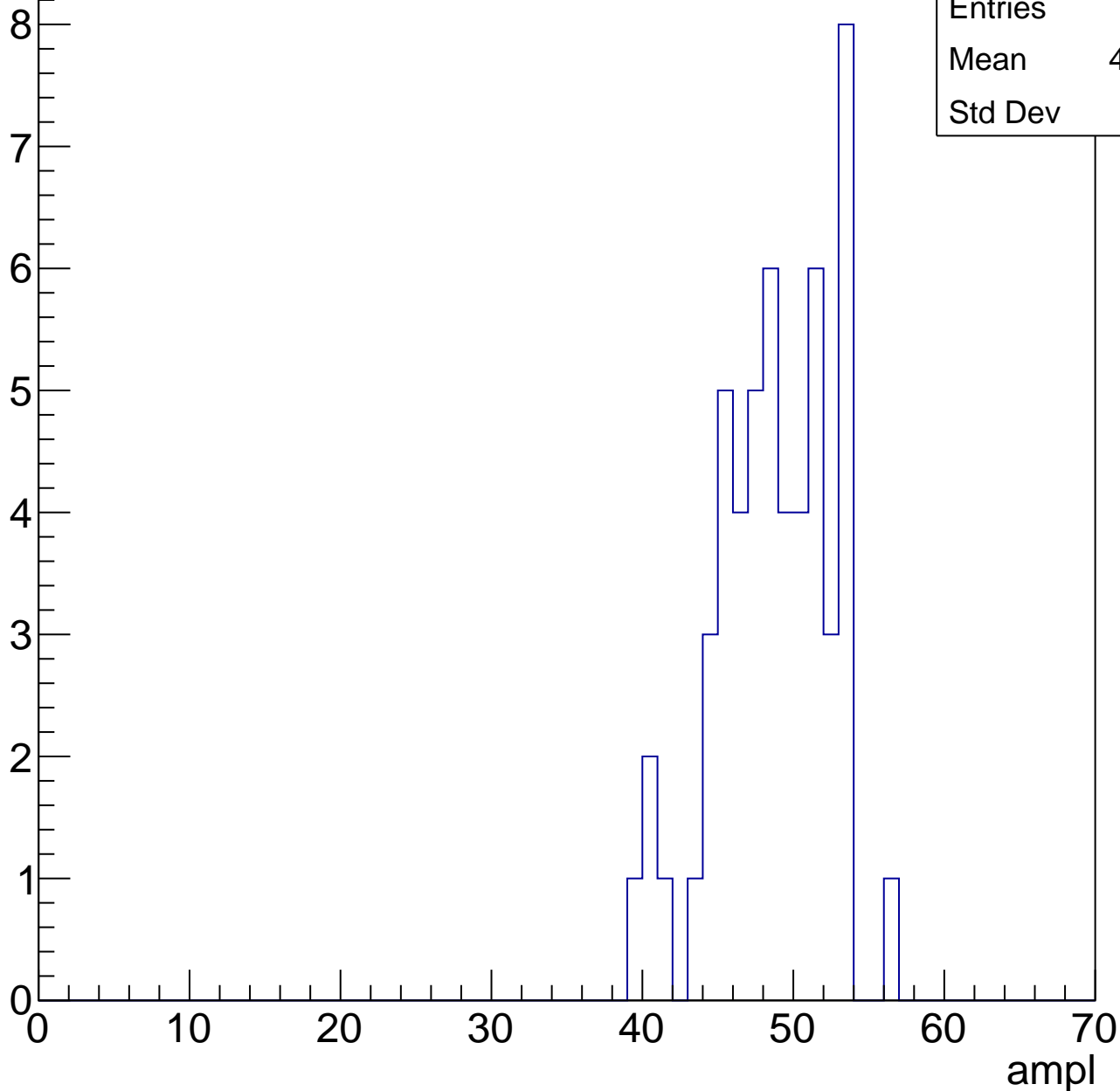


# B1L103S, U16-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	48.24
Std Dev	3.8

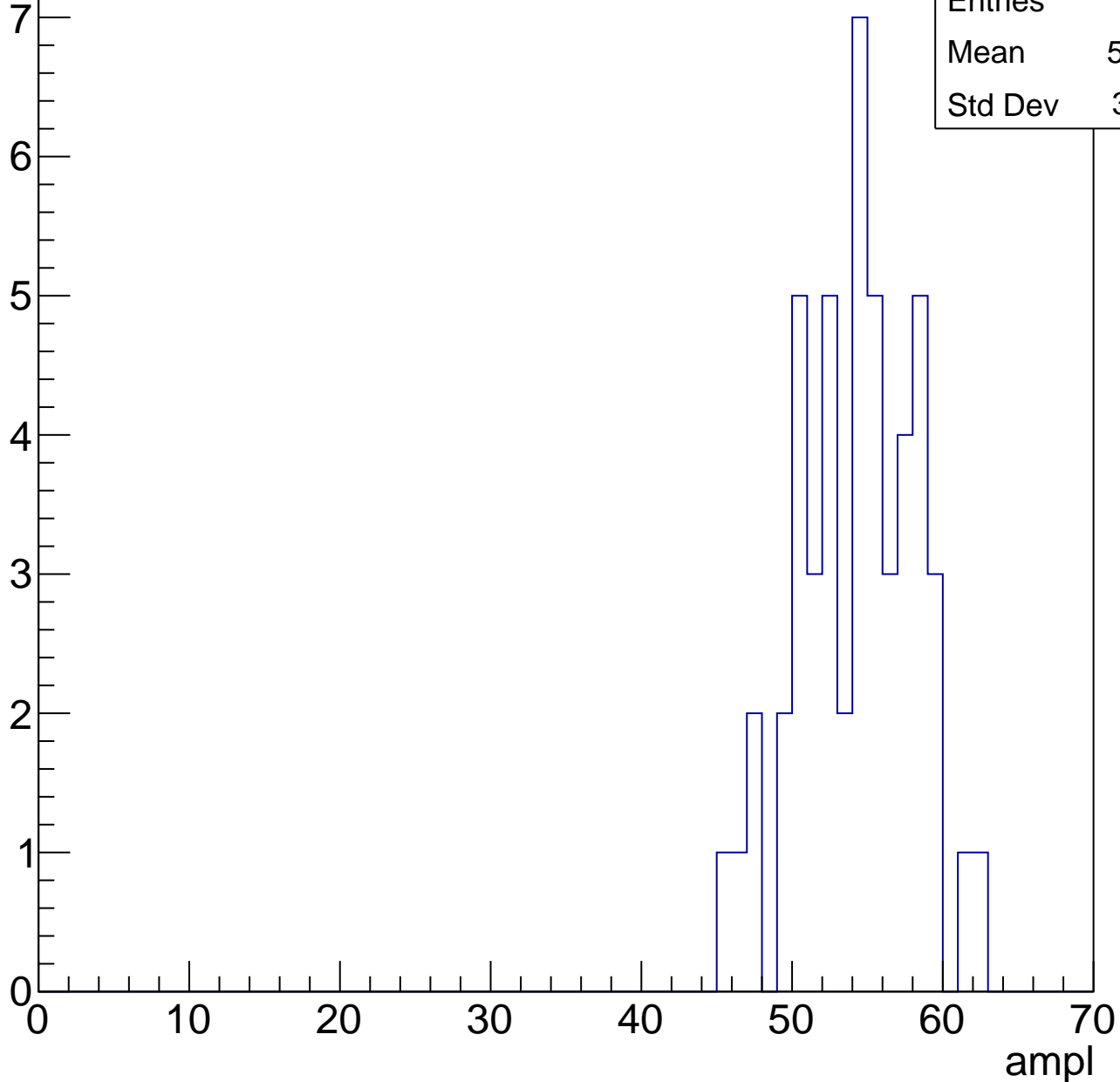


# B1L103S, U16-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

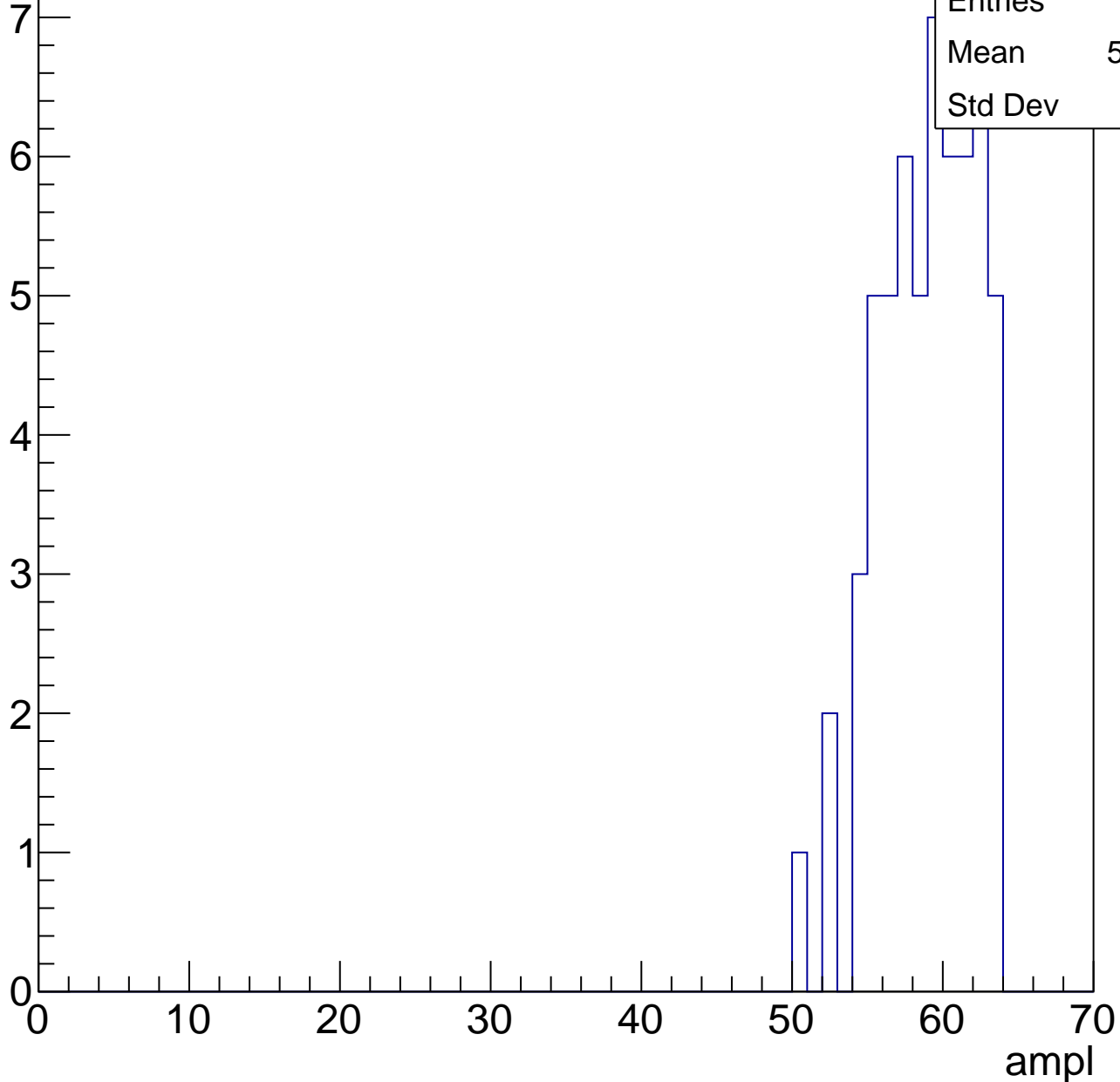
Entries	50
Mean	53.82
Std Dev	3.851



# B1L103S, U16-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

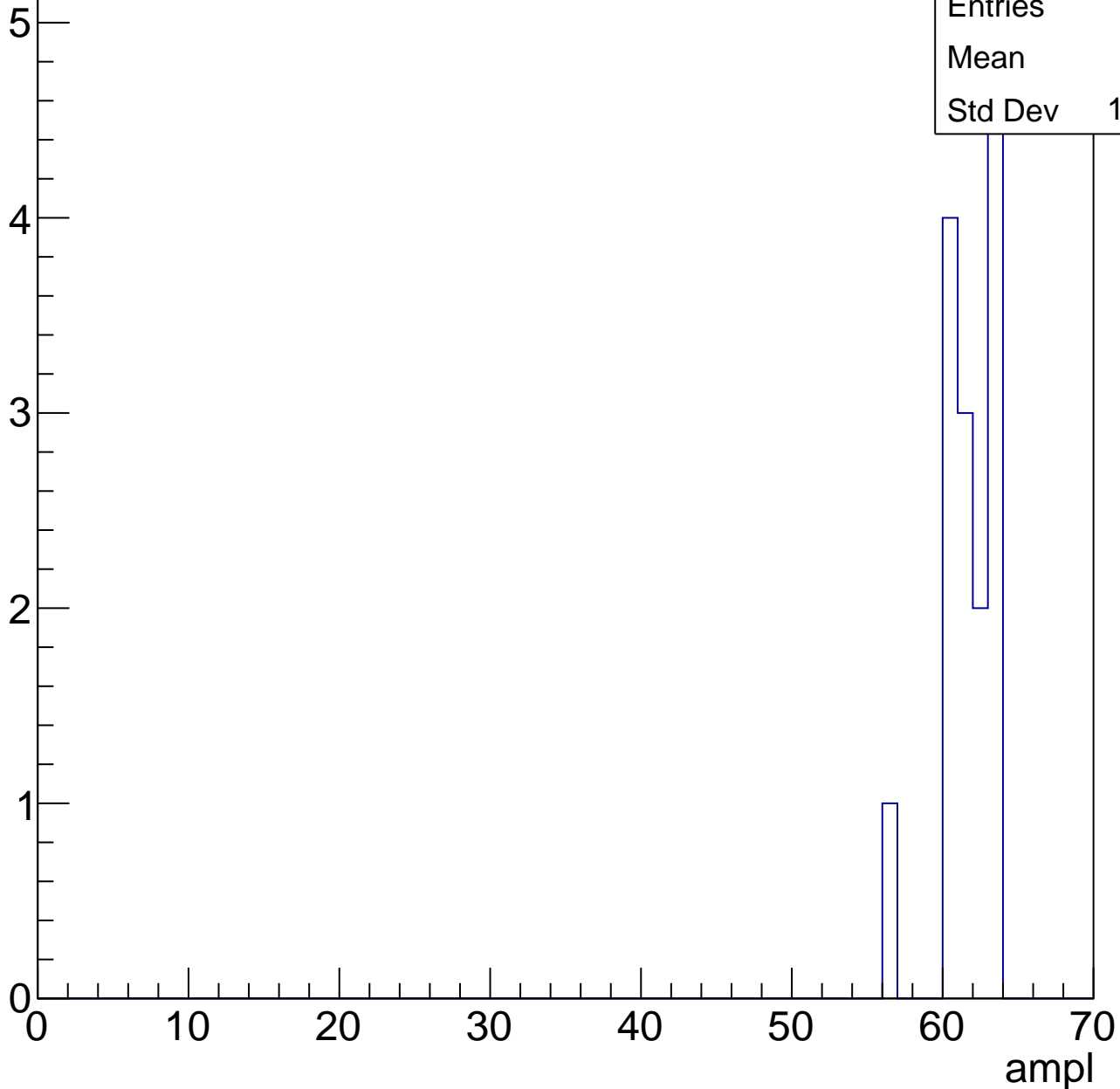


# B1L103S, U16-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	15
Mean	61.2
Std Dev	1.833





# B1L103S, U16-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U16-ch91, adc0

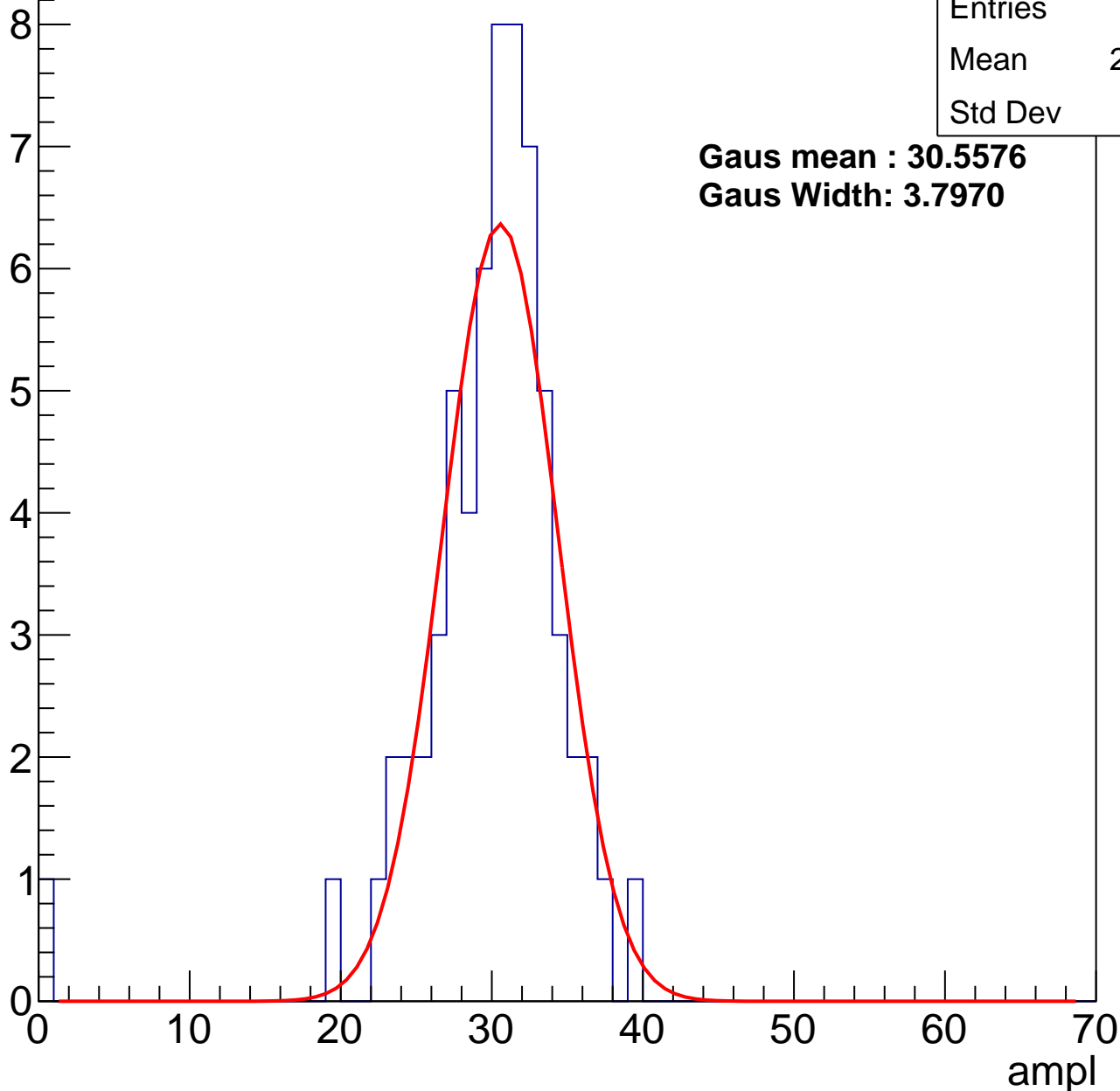
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	29.39
Std Dev	5.27

**Gaus mean : 30.5576**

**Gaus Width: 3.7970**



# B1L103S, U16-ch91, adc1

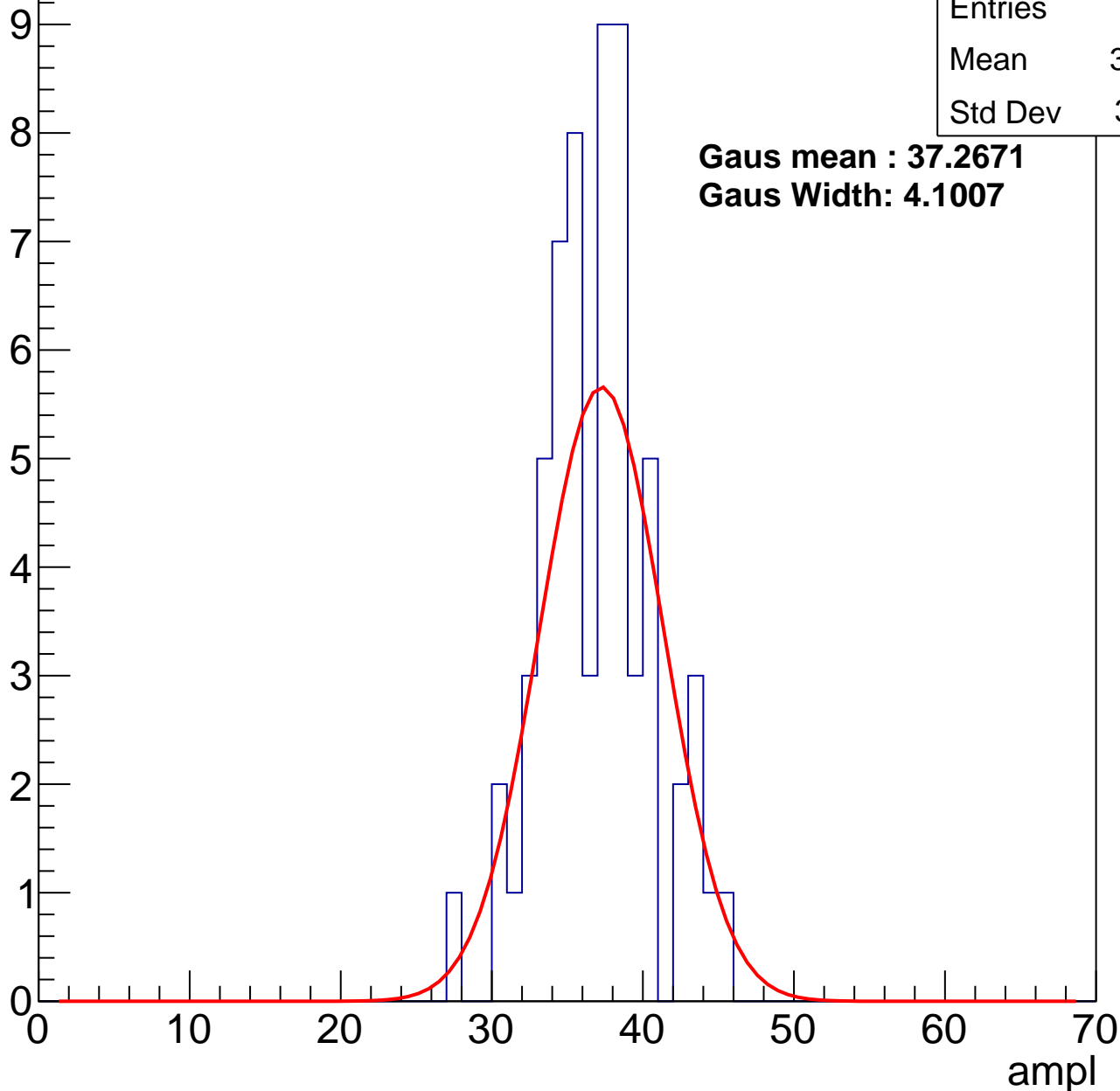
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	36.49
Std Dev	3.581

**Gaus mean : 37.2671**

**Gaus Width: 4.1007**



# B1L103S, U16-ch91, adc2

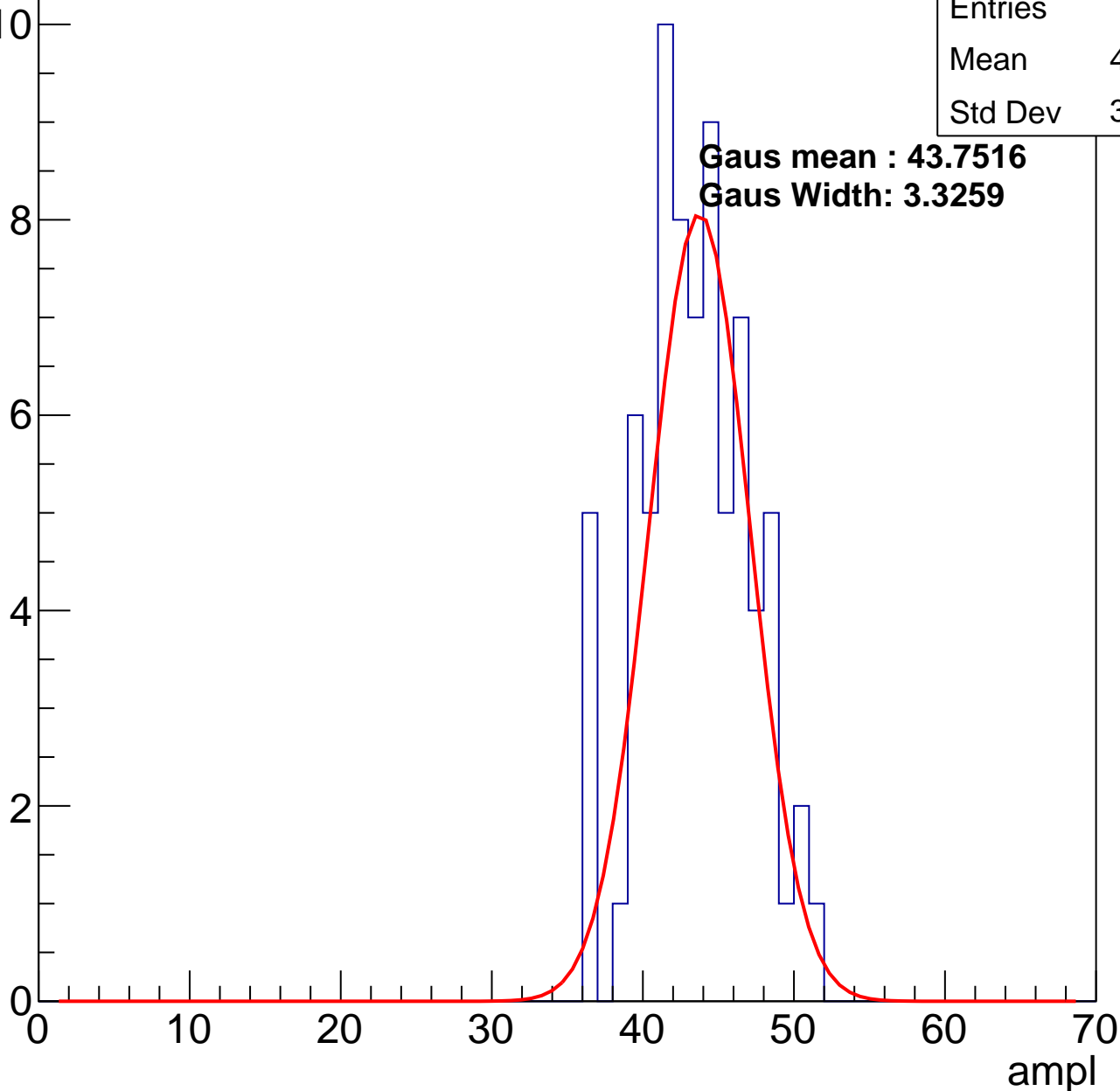
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	43.03
Std Dev	3.513

**Gaus mean : 43.7516**

**Gaus Width: 3.3259**

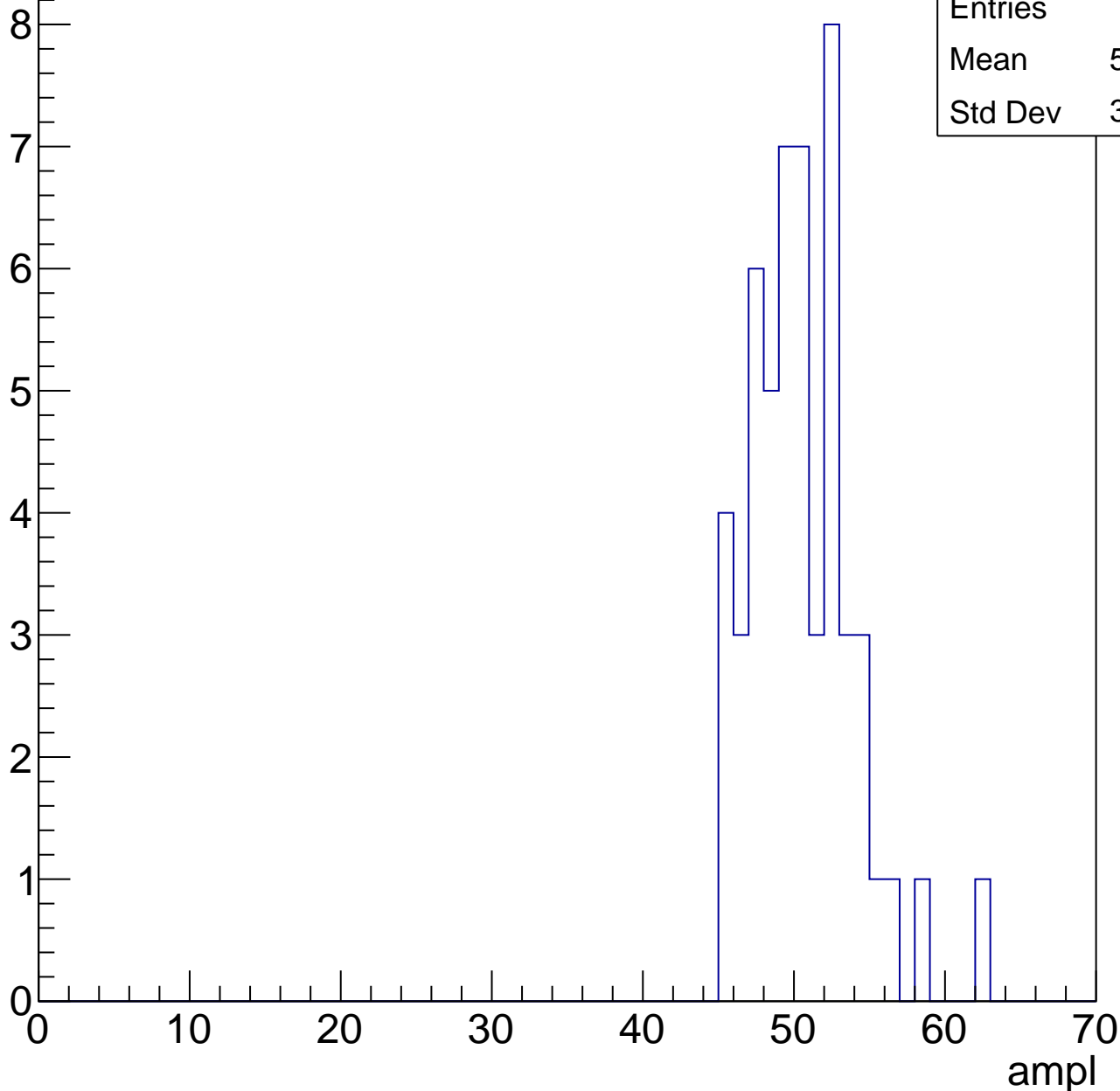


# B1L103S, U16-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

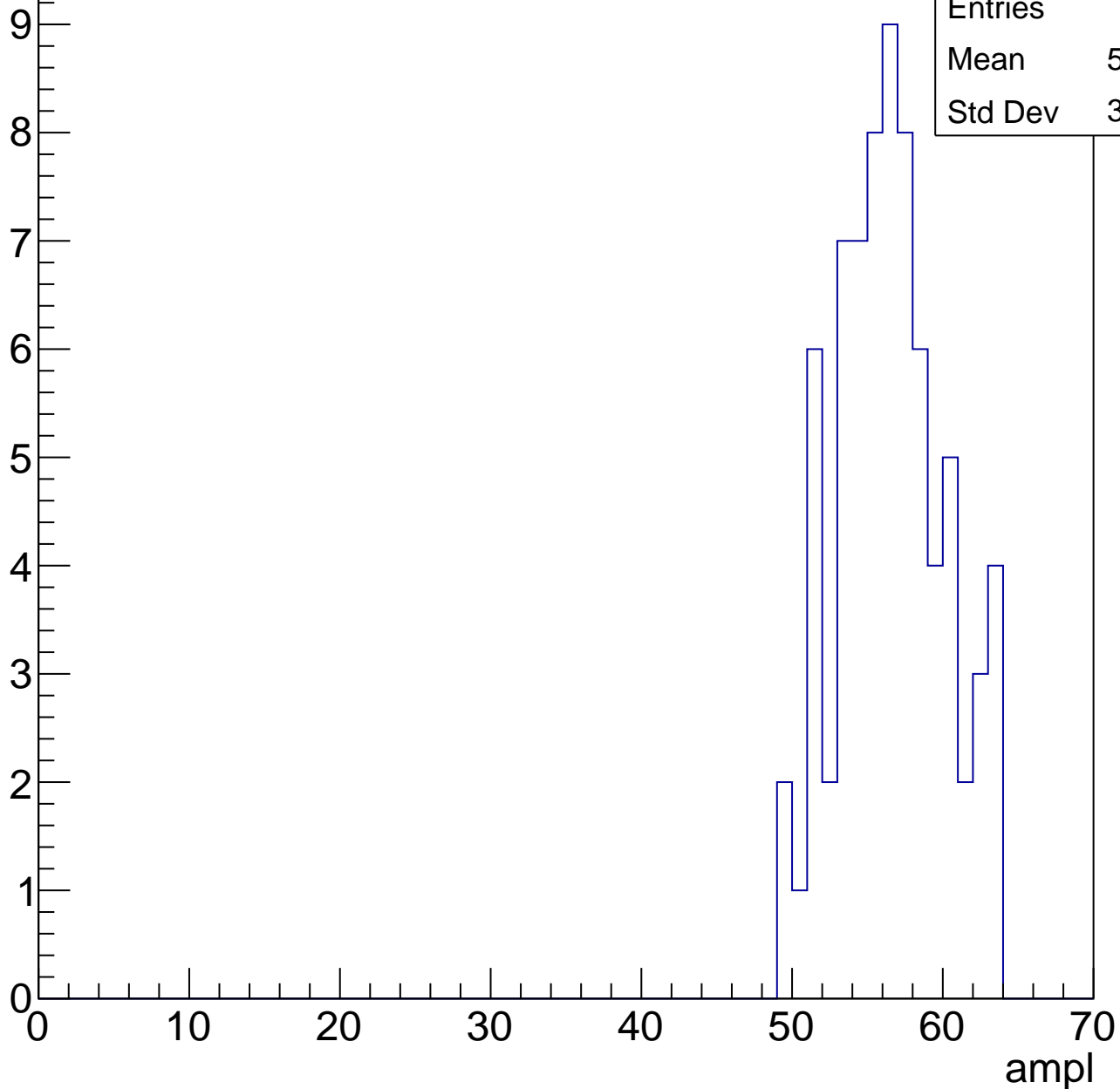
Entries	53
Mean	50.08
Std Dev	3.386



# B1L103S, U16-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



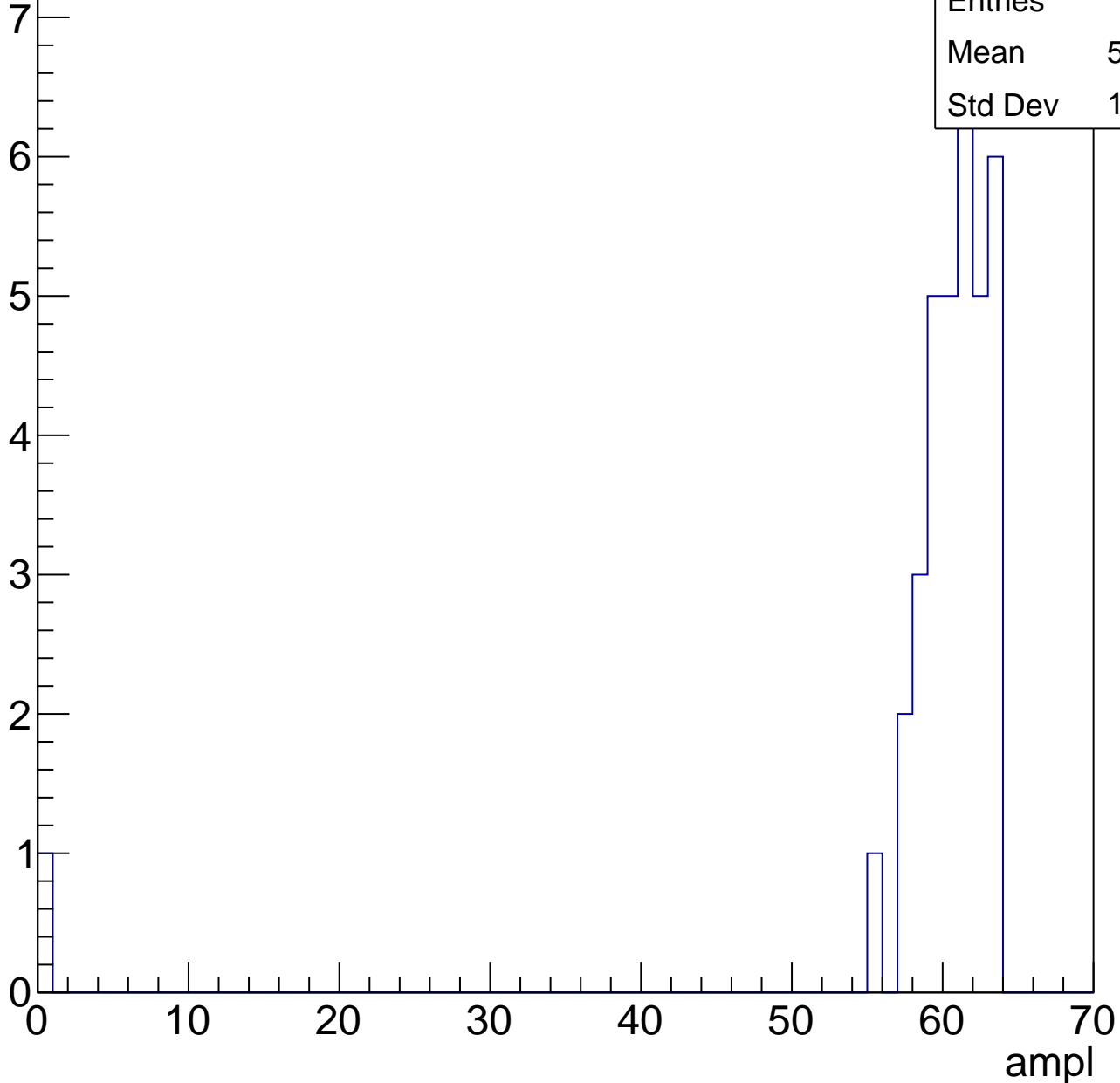
Entries	74
Mean	56.09
Std Dev	3.519

# B1L103S, U16-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

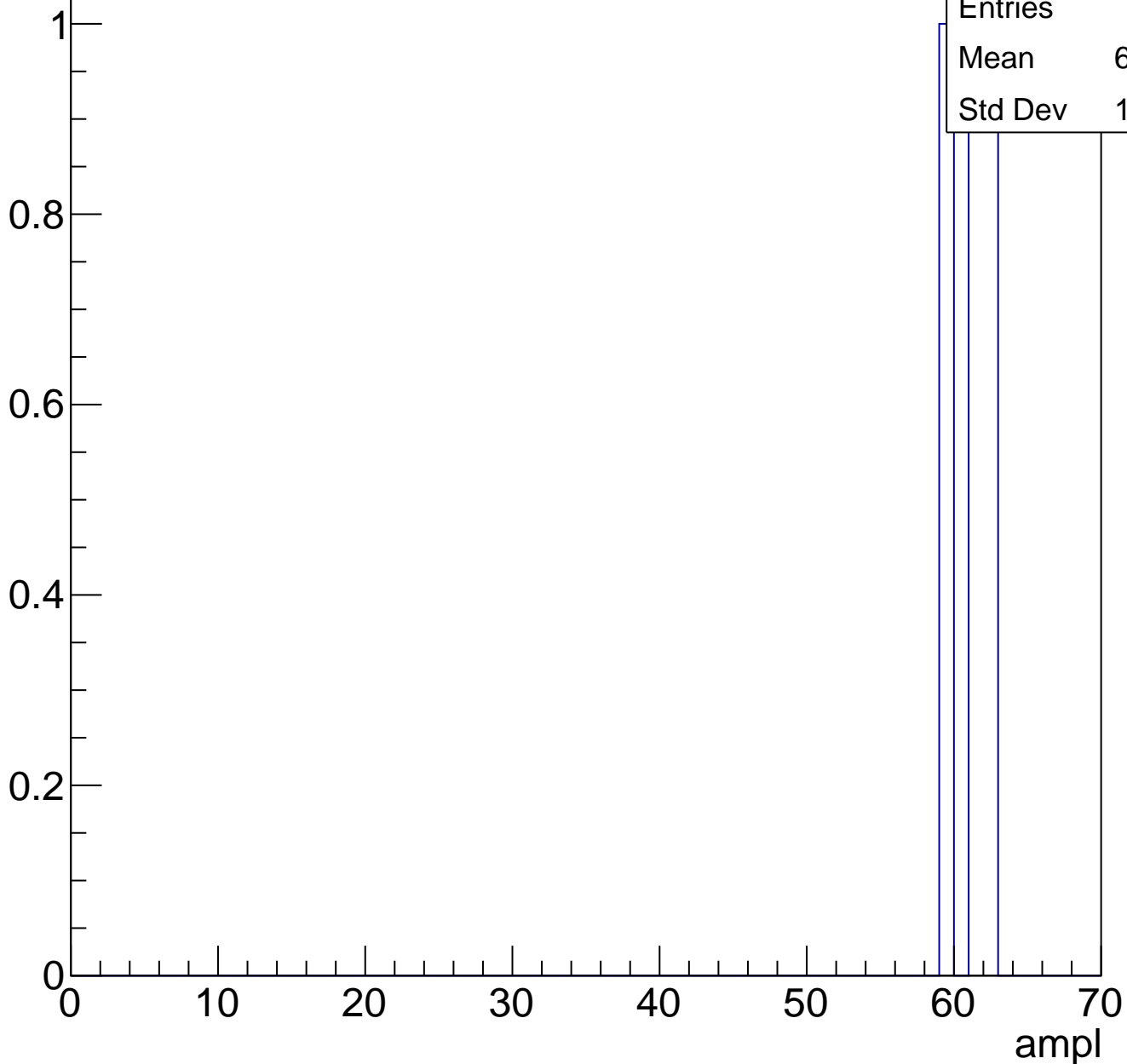
Entries	35
Mean	58.66
Std Dev	10.25



# B1L103S, U16-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U16-ch92, adc0

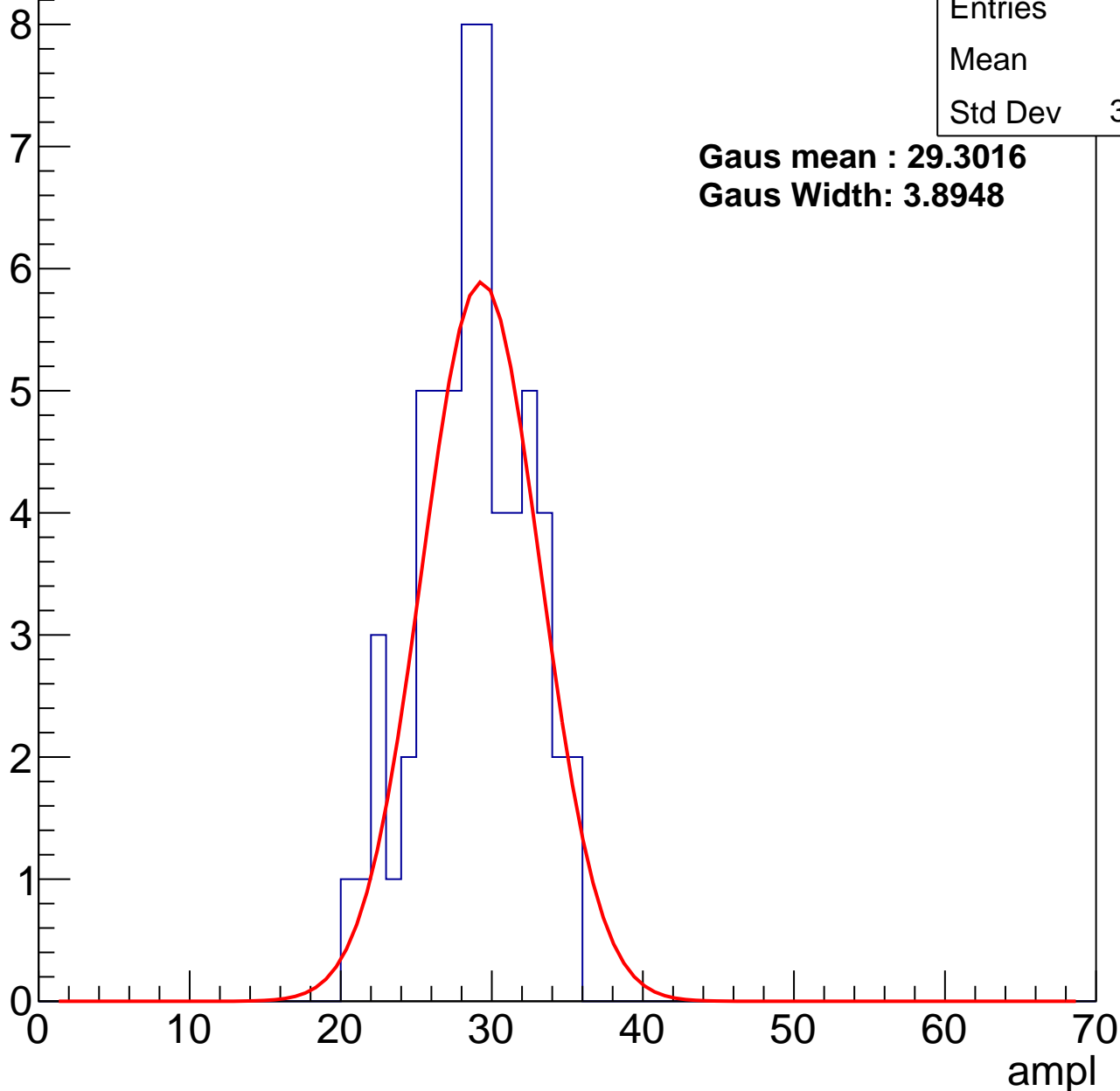
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	28.3
Std Dev	3.542

**Gaus mean : 29.3016**

**Gaus Width: 3.8948**



# B1L103S, U16-ch92, adc1

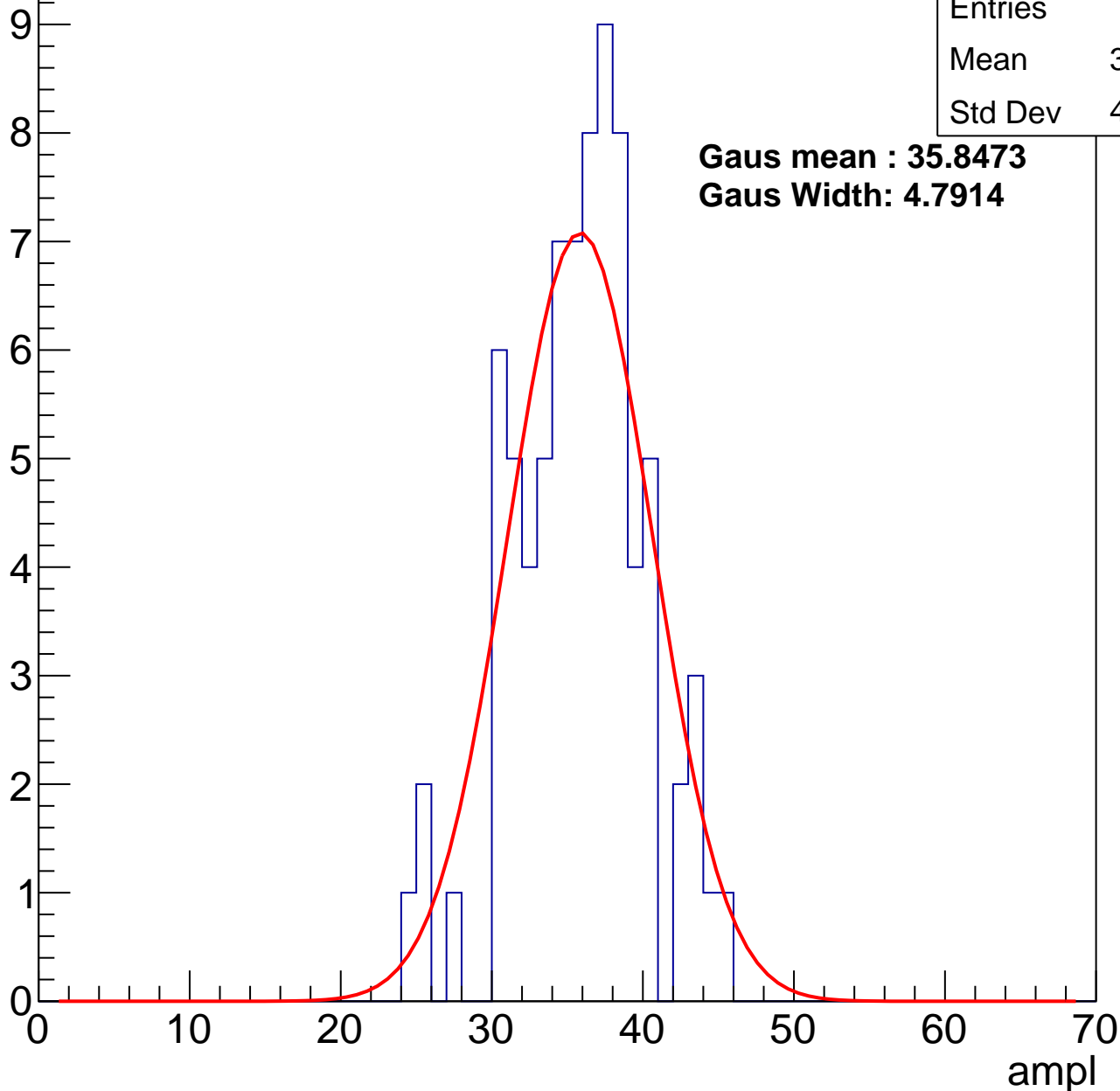
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	35.38
Std Dev	4.273

**Gaus mean : 35.8473**

**Gaus Width: 4.7914**



# B1L103S, U16-ch92, adc2

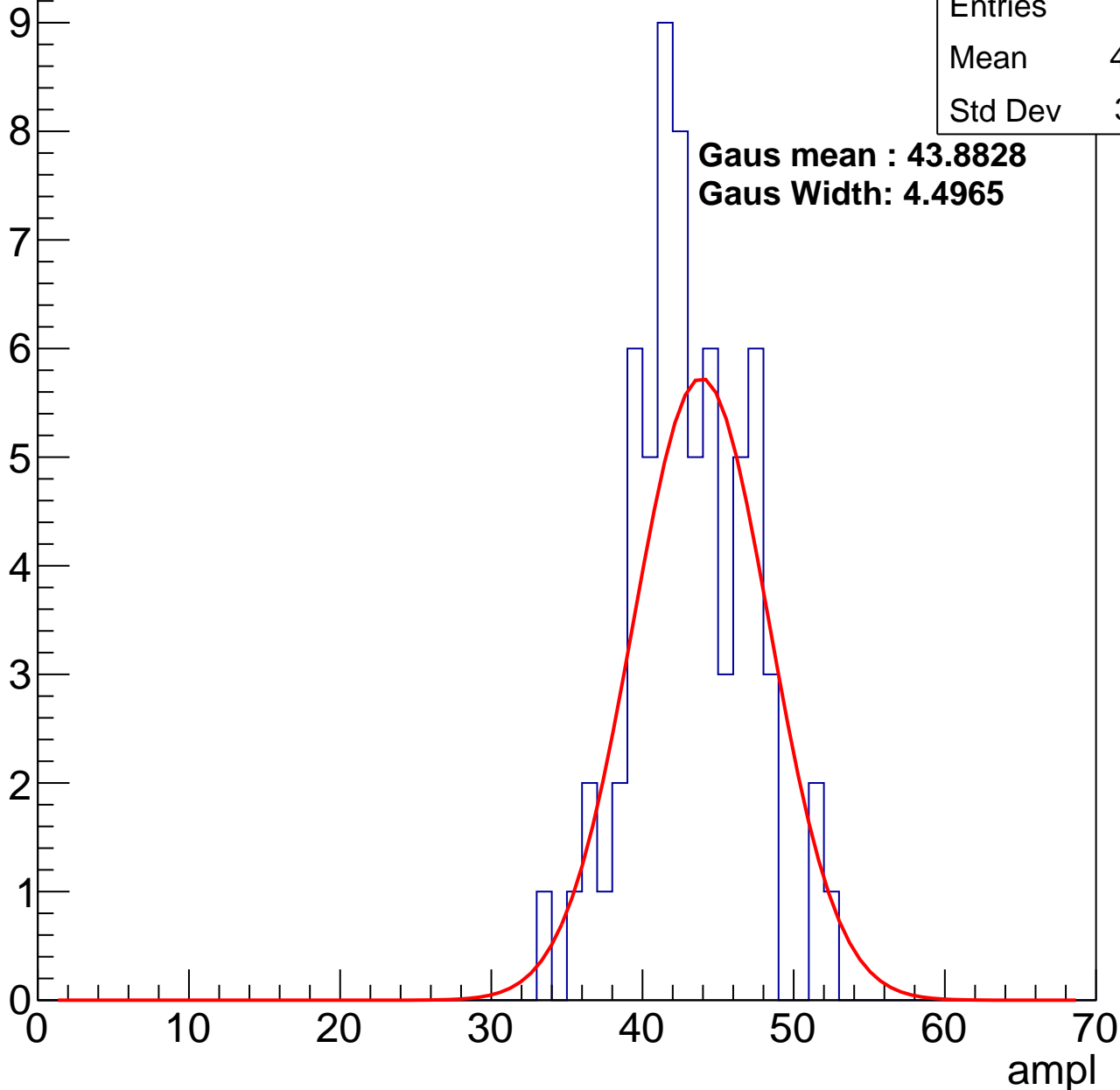
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	42.67
Std Dev	3.831

**Gaus mean : 43.8828**

**Gaus Width: 4.4965**

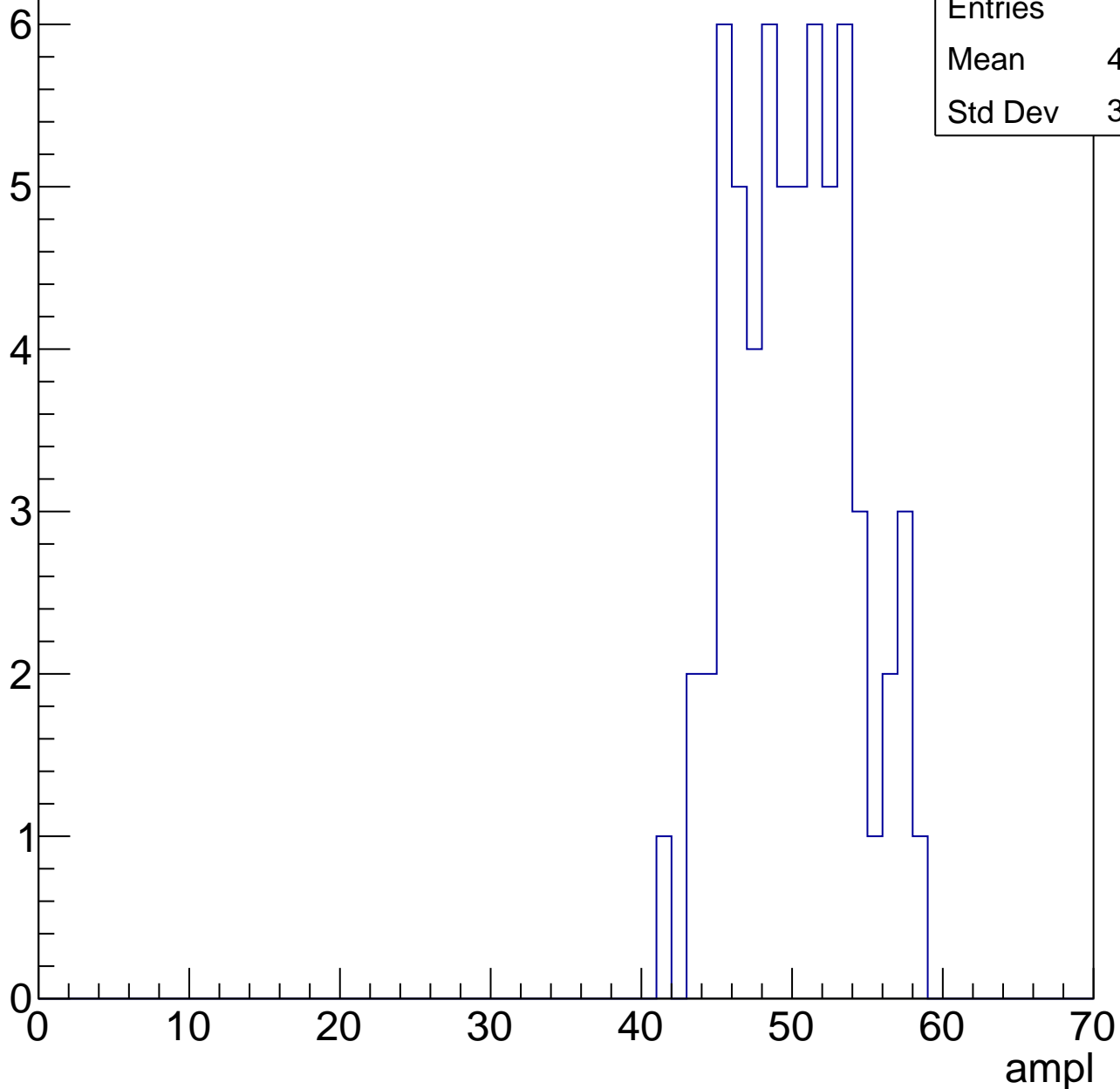


# B1L103S, U16-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	49.65
Std Dev	3.933

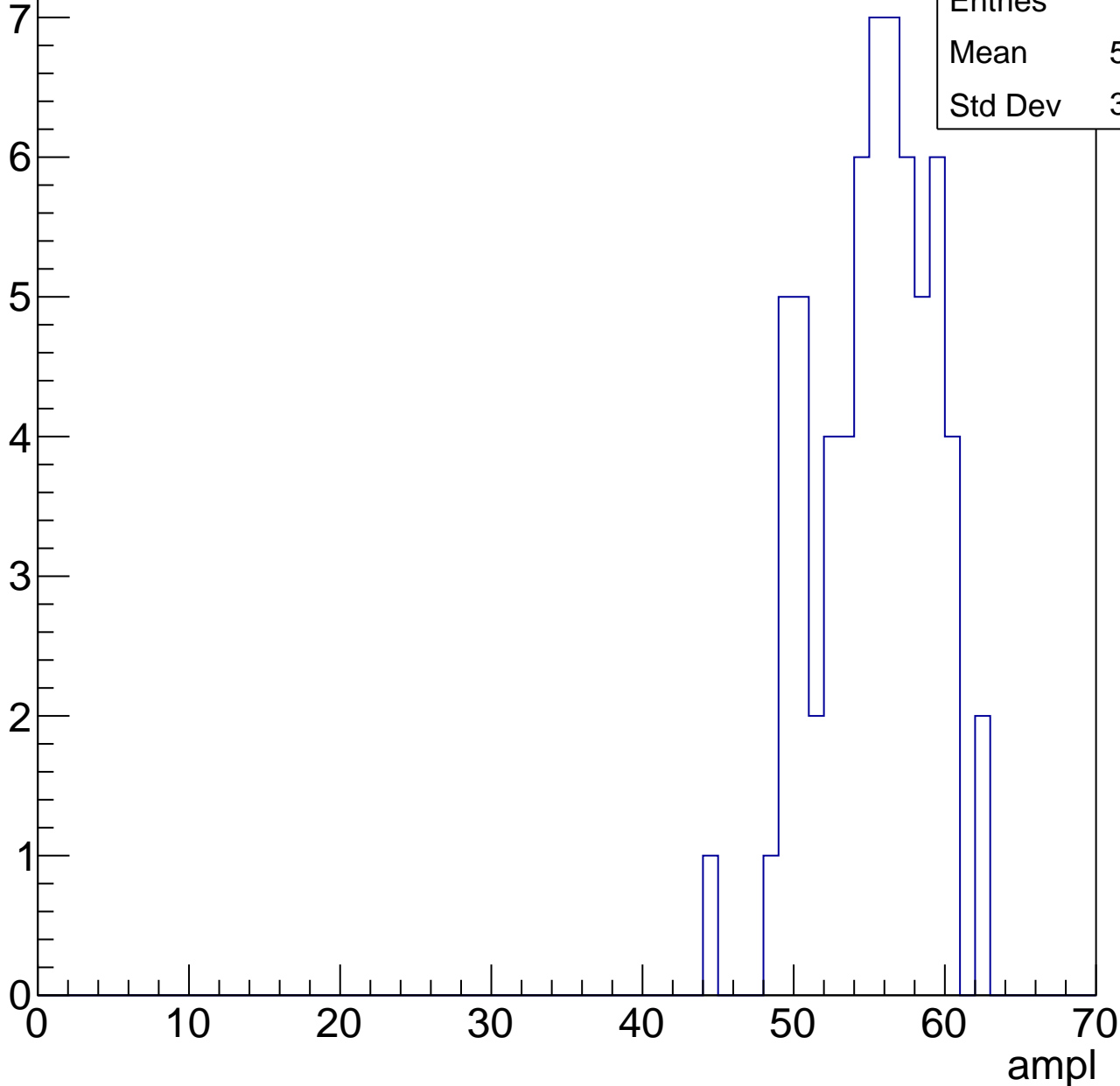


# B1L103S, U16-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	54.77
Std Dev	3.786

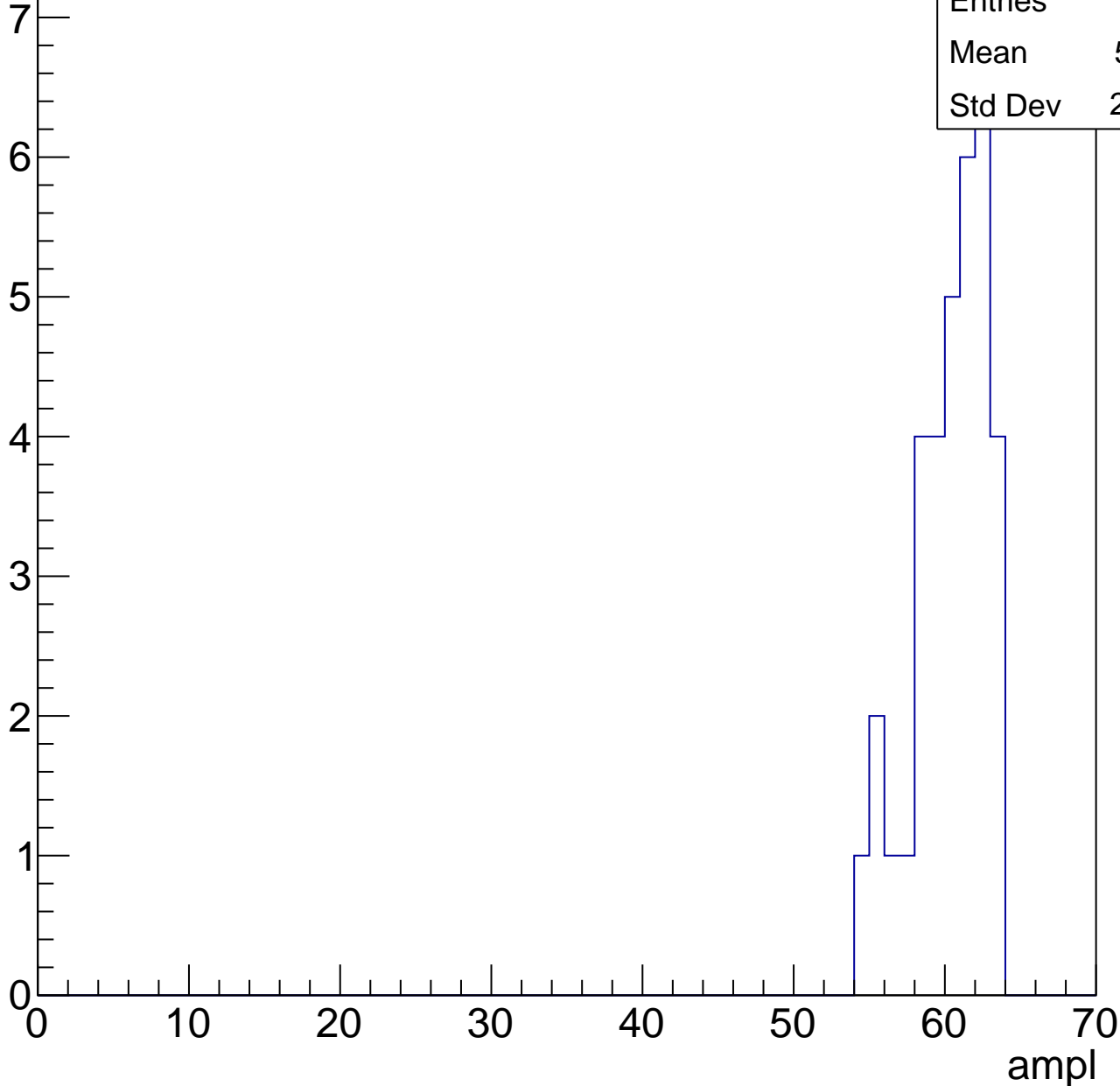


# B1L103S, U16-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	35
Mean	59.91
Std Dev	2.395

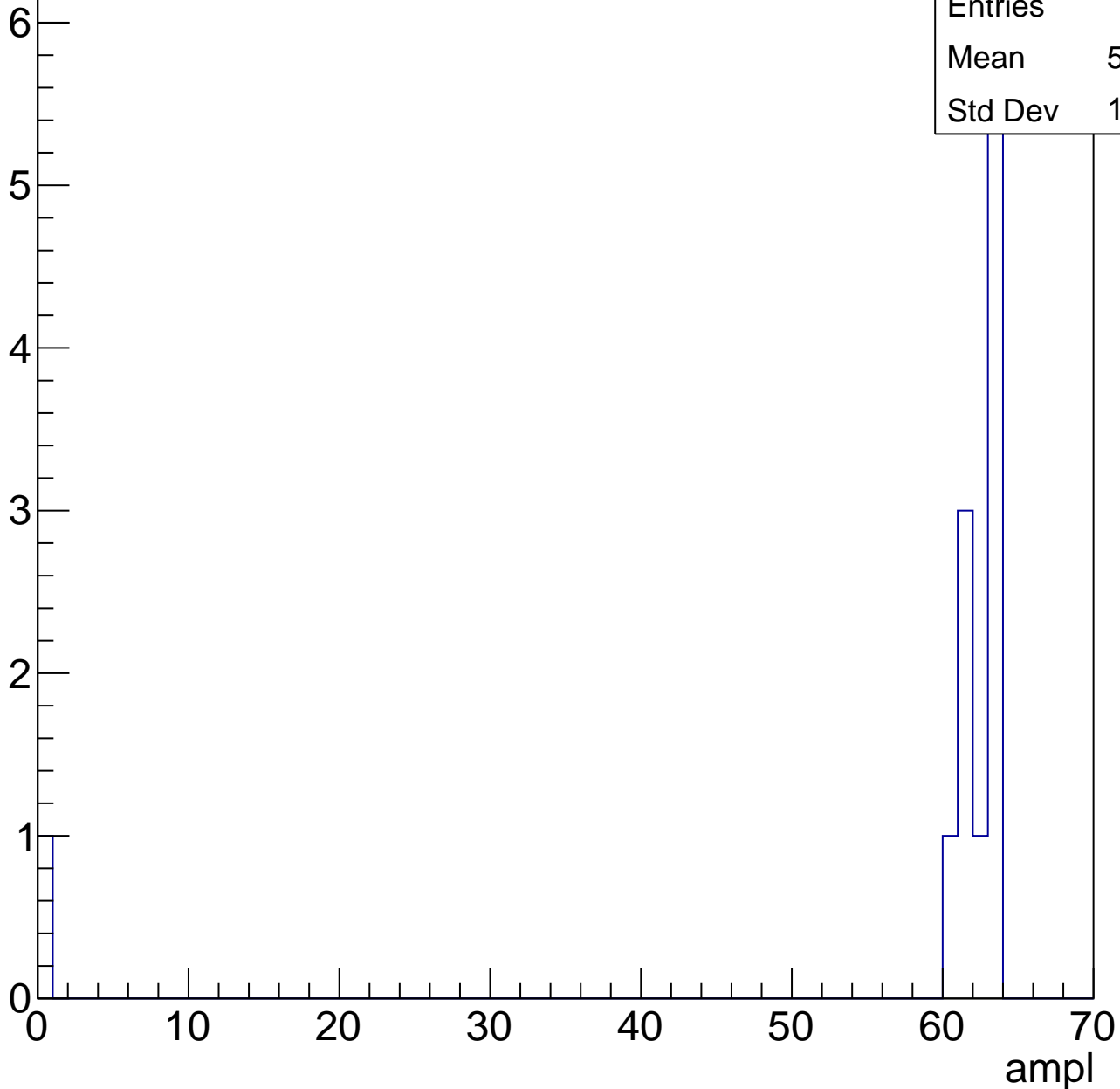


# B1L103S, U16-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	12
Mean	56.92
Std Dev	17.19

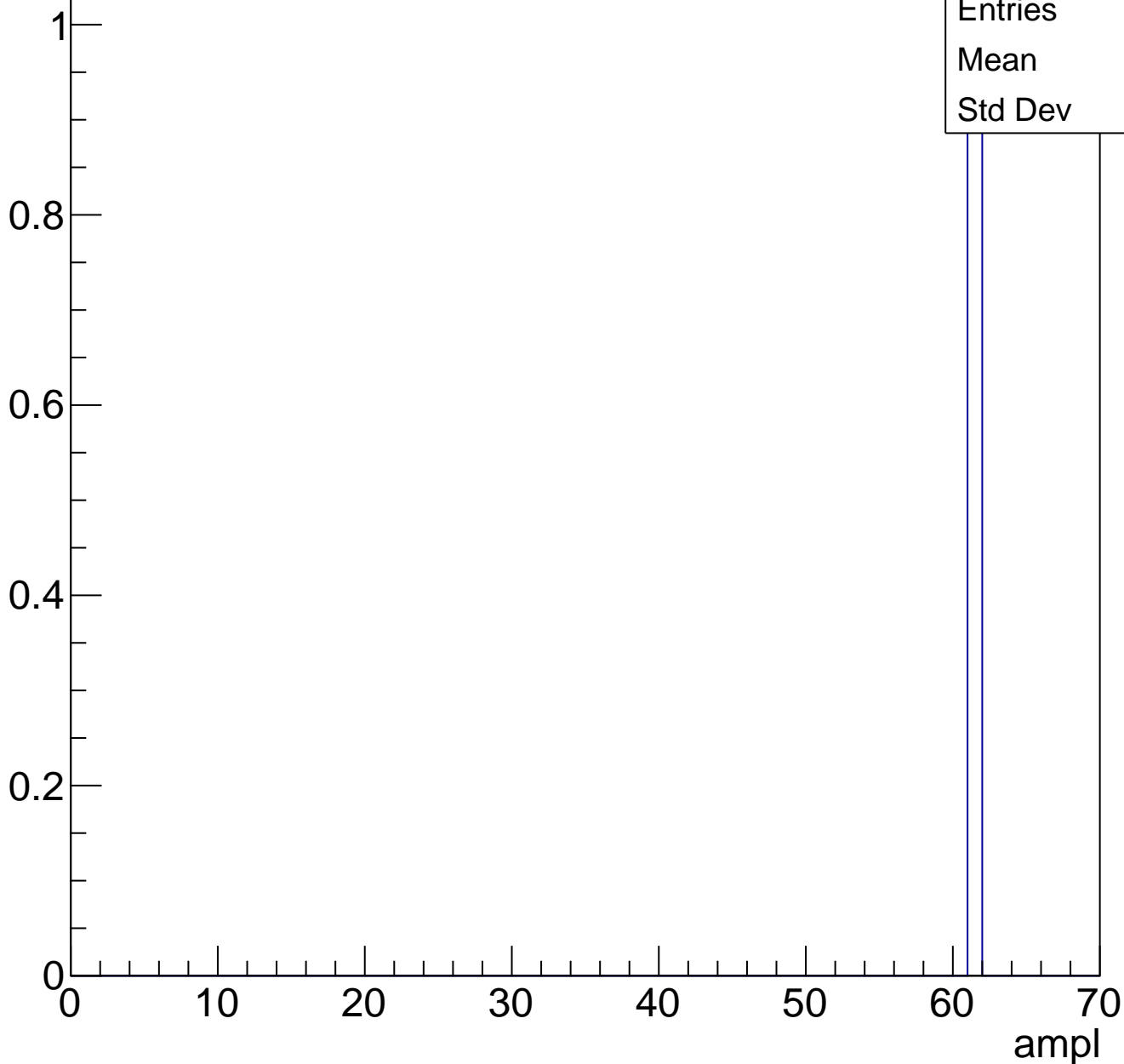




# B1L103S, U16-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch93, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	68
Mean	28.19
Std Dev	4.806

**Gaus mean : 29.5280**

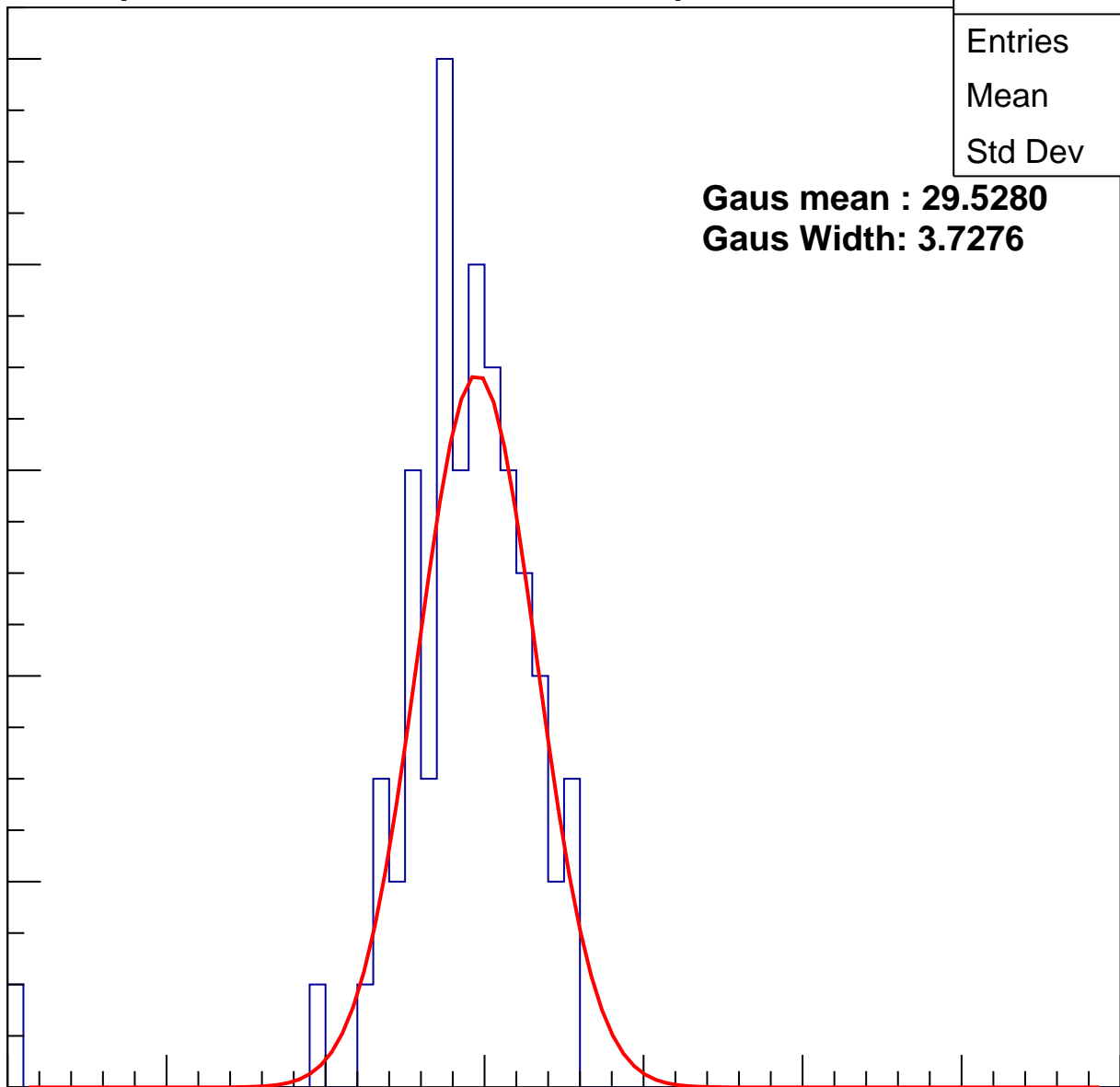
**Gaus Width: 3.7276**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U16-ch93, adc1

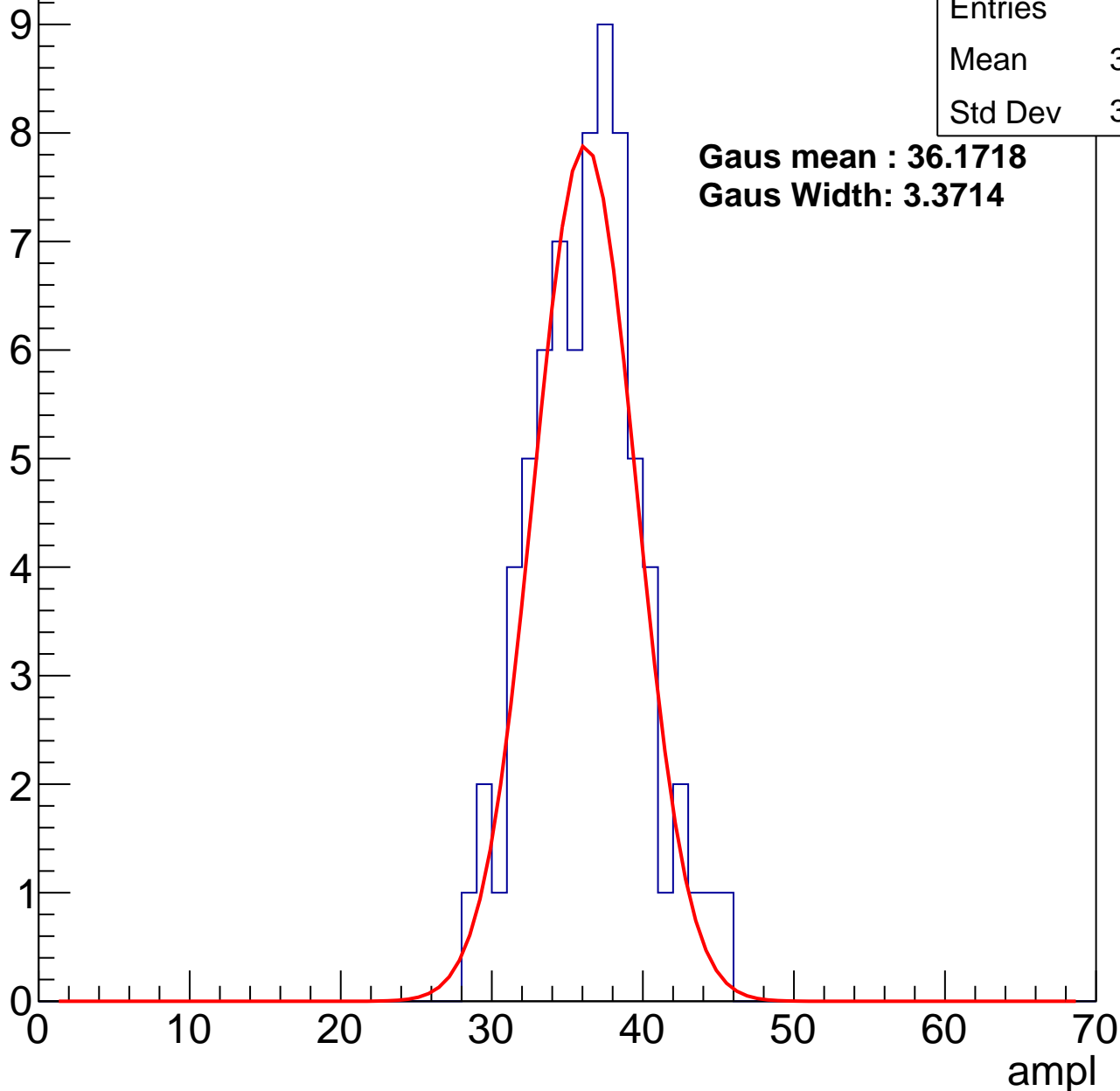
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	35.88
Std Dev	3.547

**Gaus mean : 36.1718**

**Gaus Width: 3.3714**



# B1L103S, U16-ch93, adc2

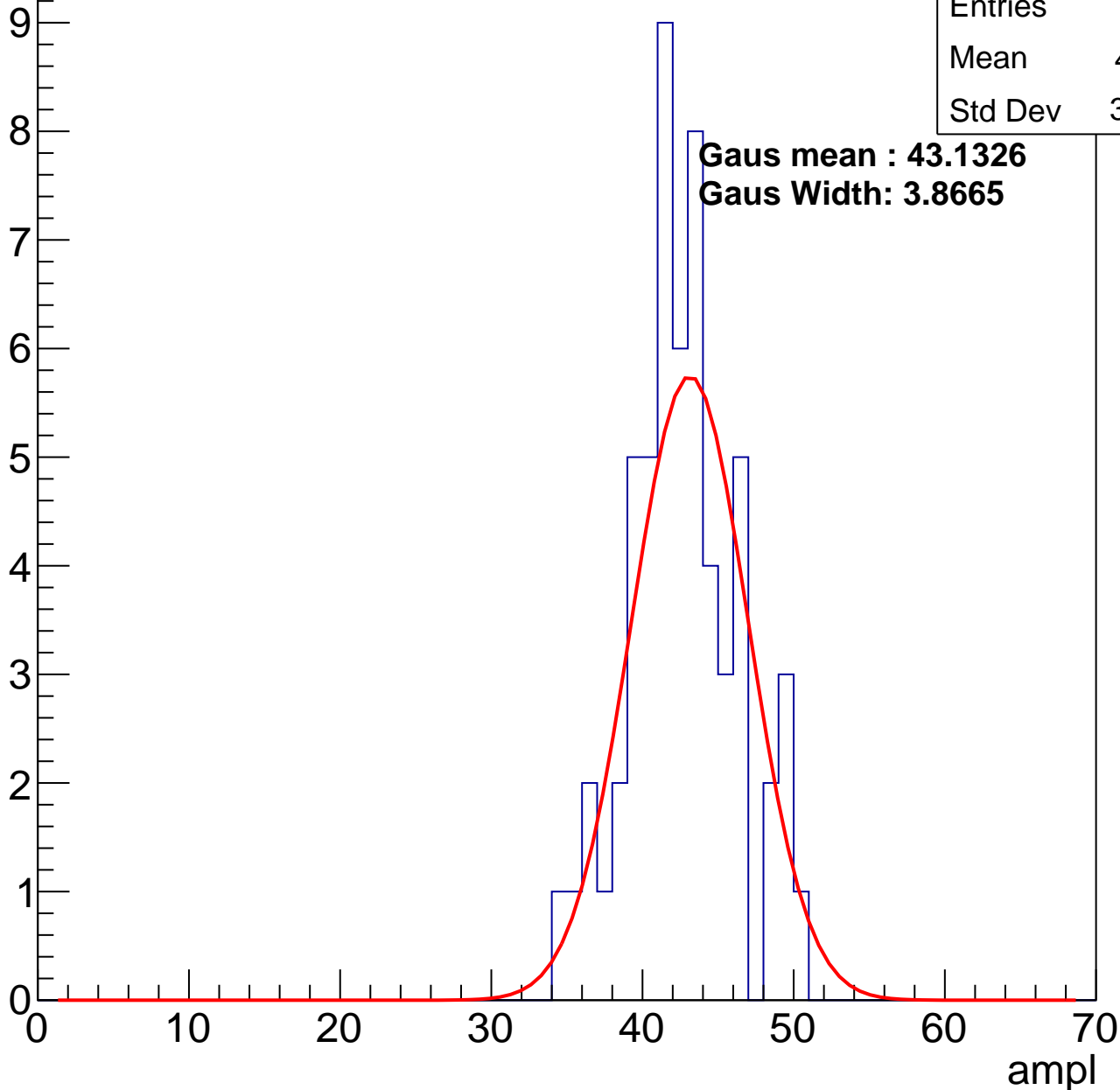
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	42.21
Std Dev	3.542

**Gaus mean : 43.1326**

**Gaus Width: 3.8665**



# B1L103S, U16-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	73
Mean	48.62
Std Dev	3.399

Entry

10

8

6

4

2

0

0

10

20

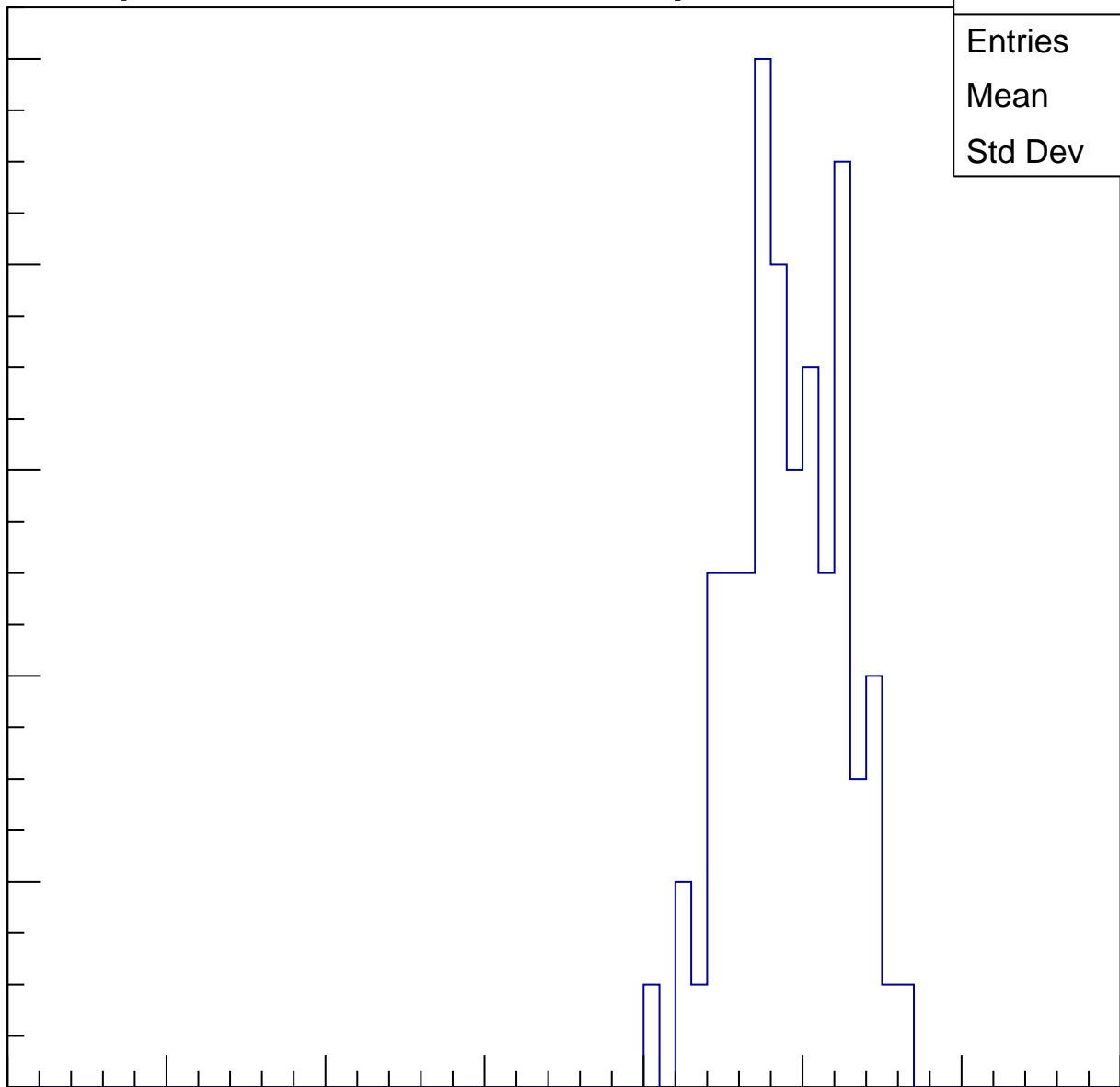
30

40

50

60

ampl

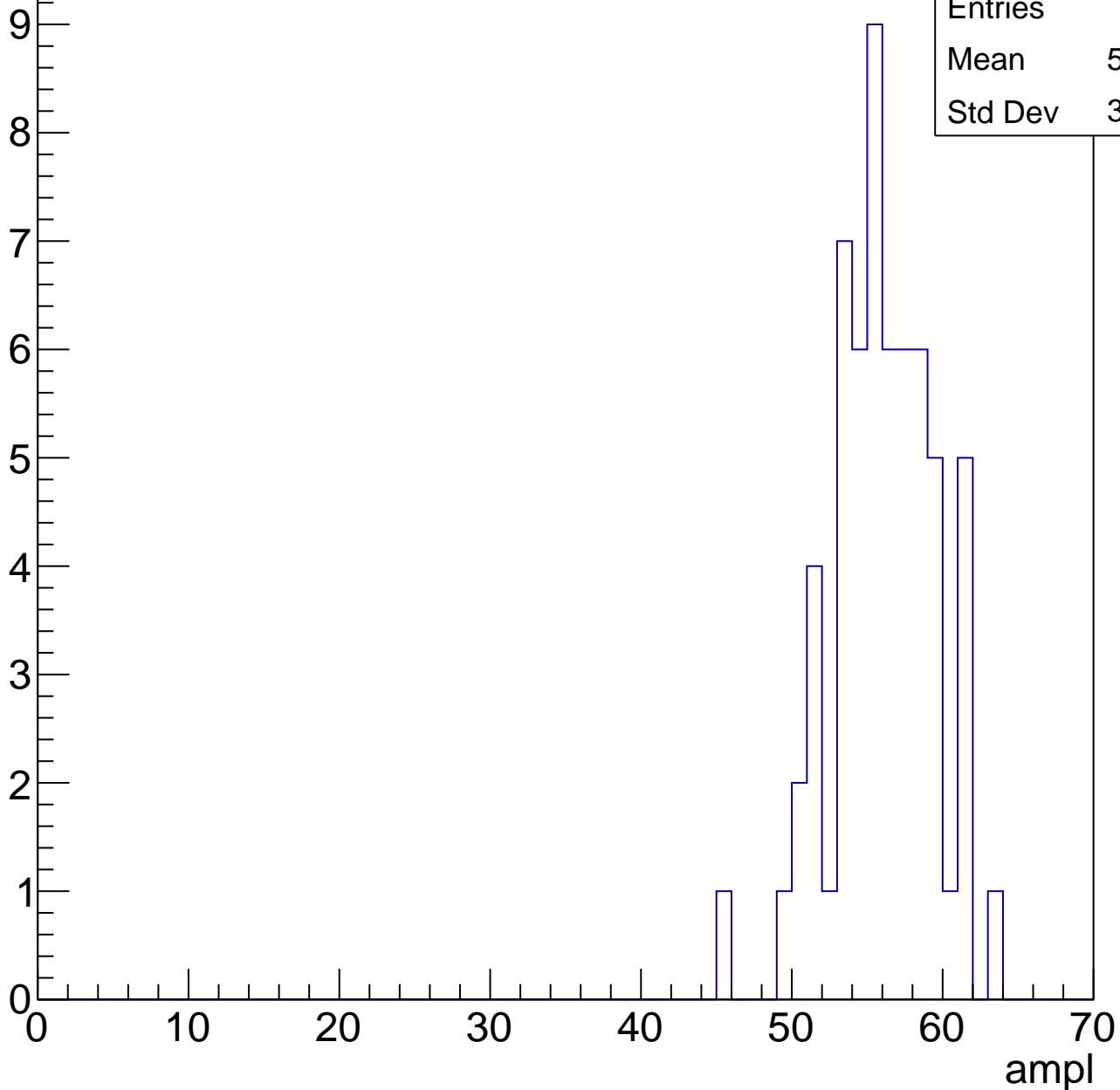


# B1L103S, U16-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	55.56
Std Dev	3.405

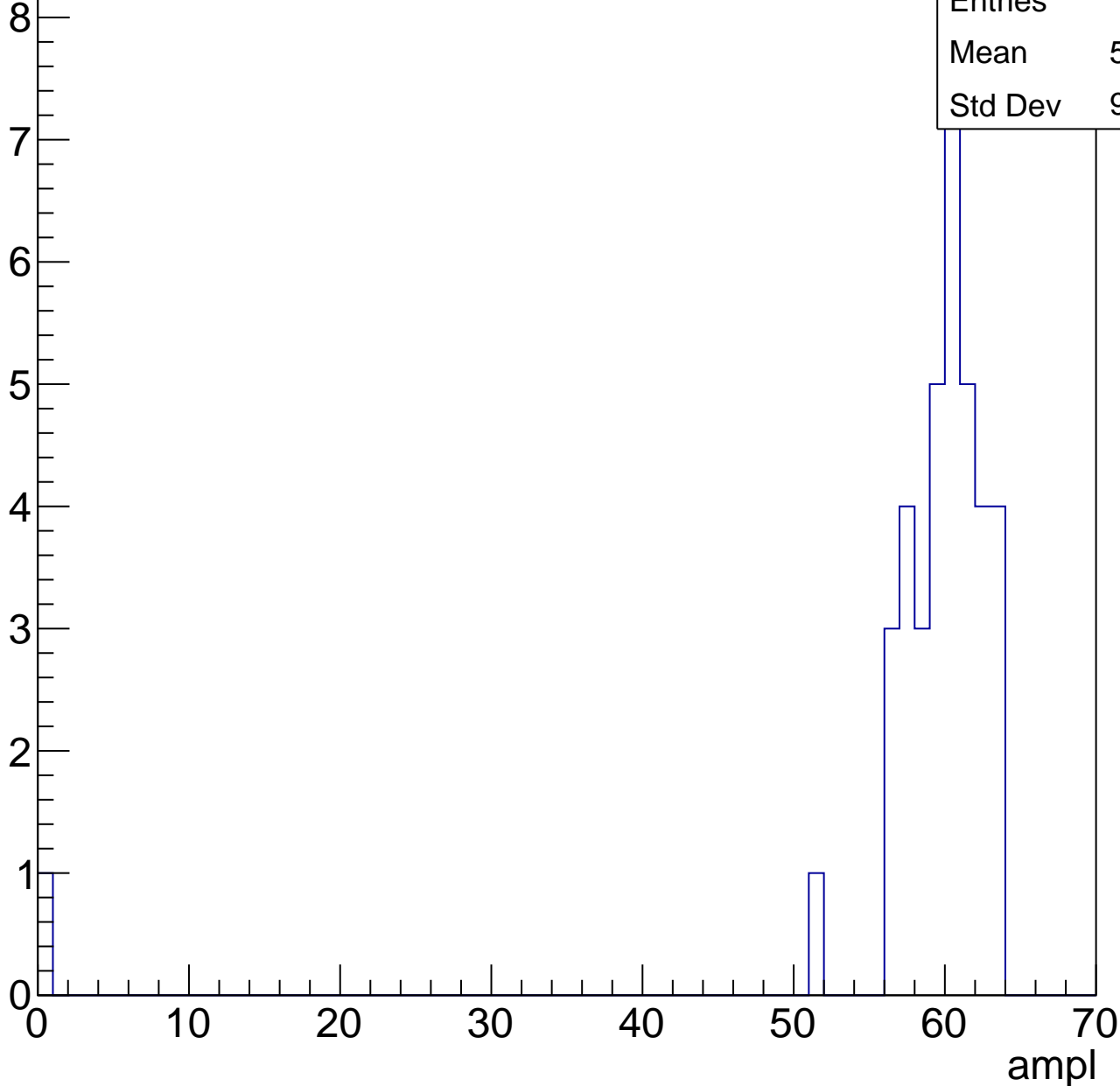


# B1L103S, U16-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	38
Mean	57.92
Std Dev	9.834

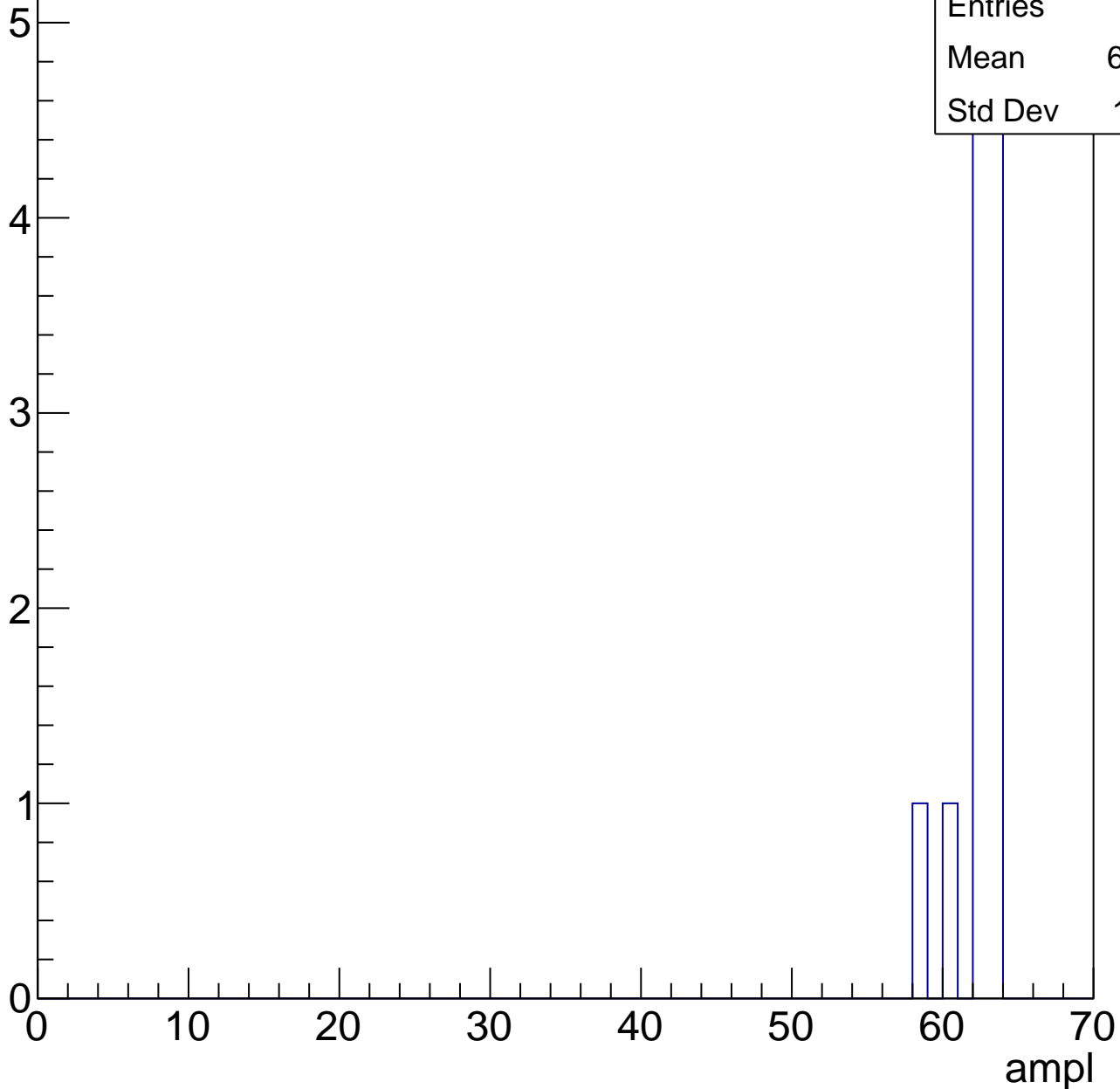


# B1L103S, U16-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	12
Mean	61.92
Std Dev	1.441





# B1L103S, U16-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch94, adc0

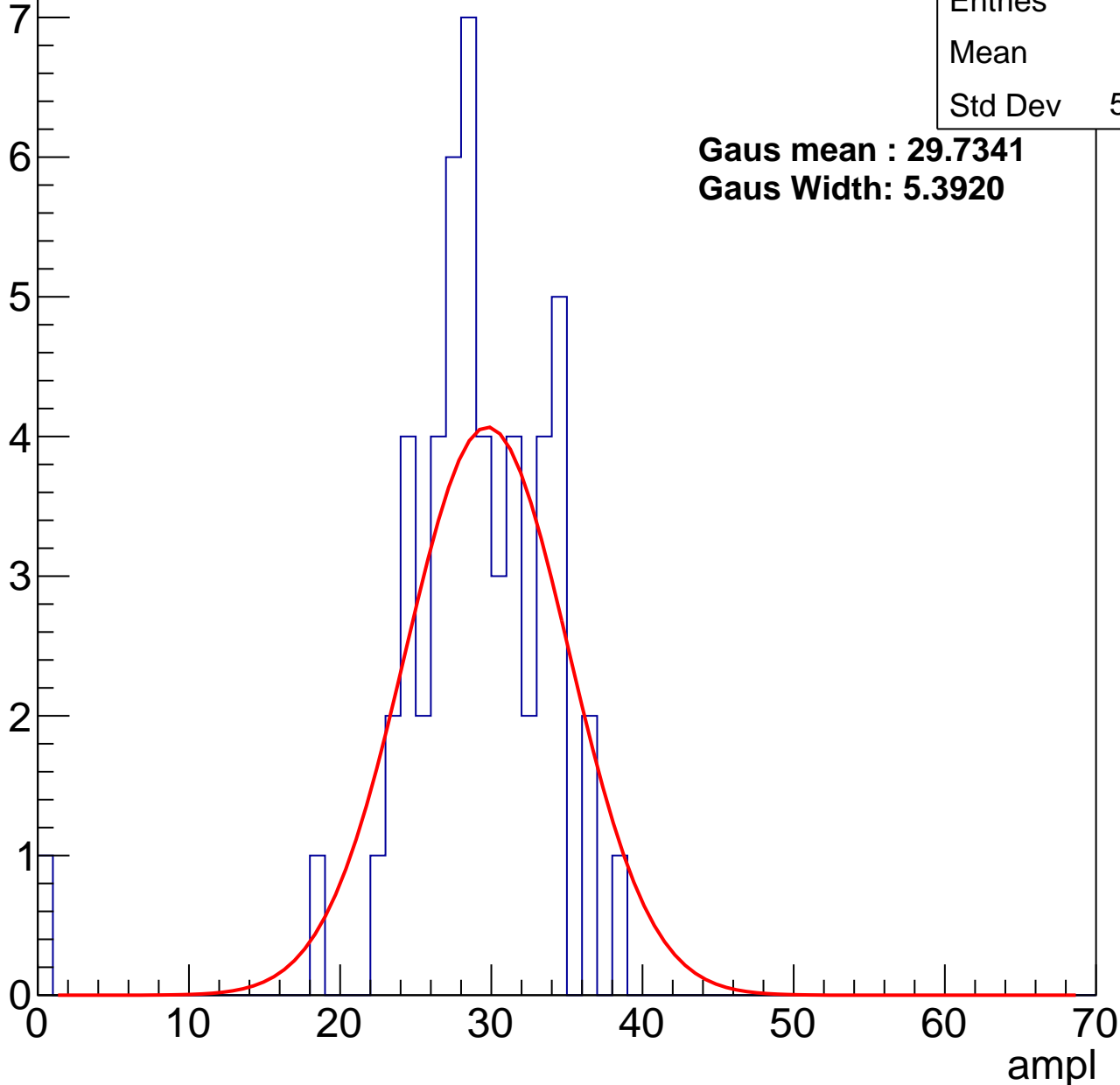
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	28.3
Std Dev	5.598

**Gaus mean : 29.7341**

**Gaus Width: 5.3920**



# B1L103S, U16-ch94, adc1

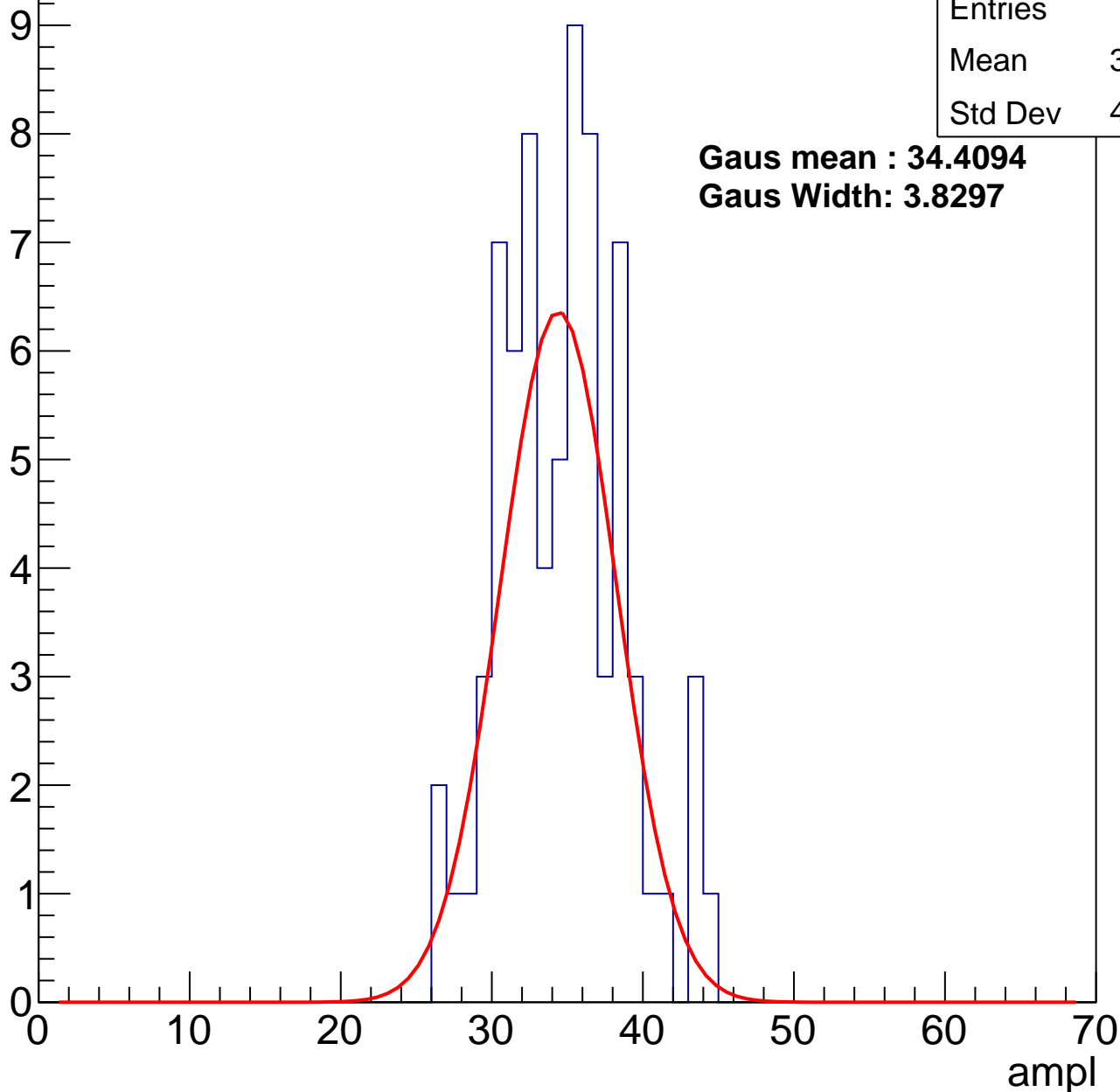
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	34.23
Std Dev	4.002

**Gaus mean : 34.4094**

**Gaus Width: 3.8297**



# B1L103S, U16-ch94, adc2

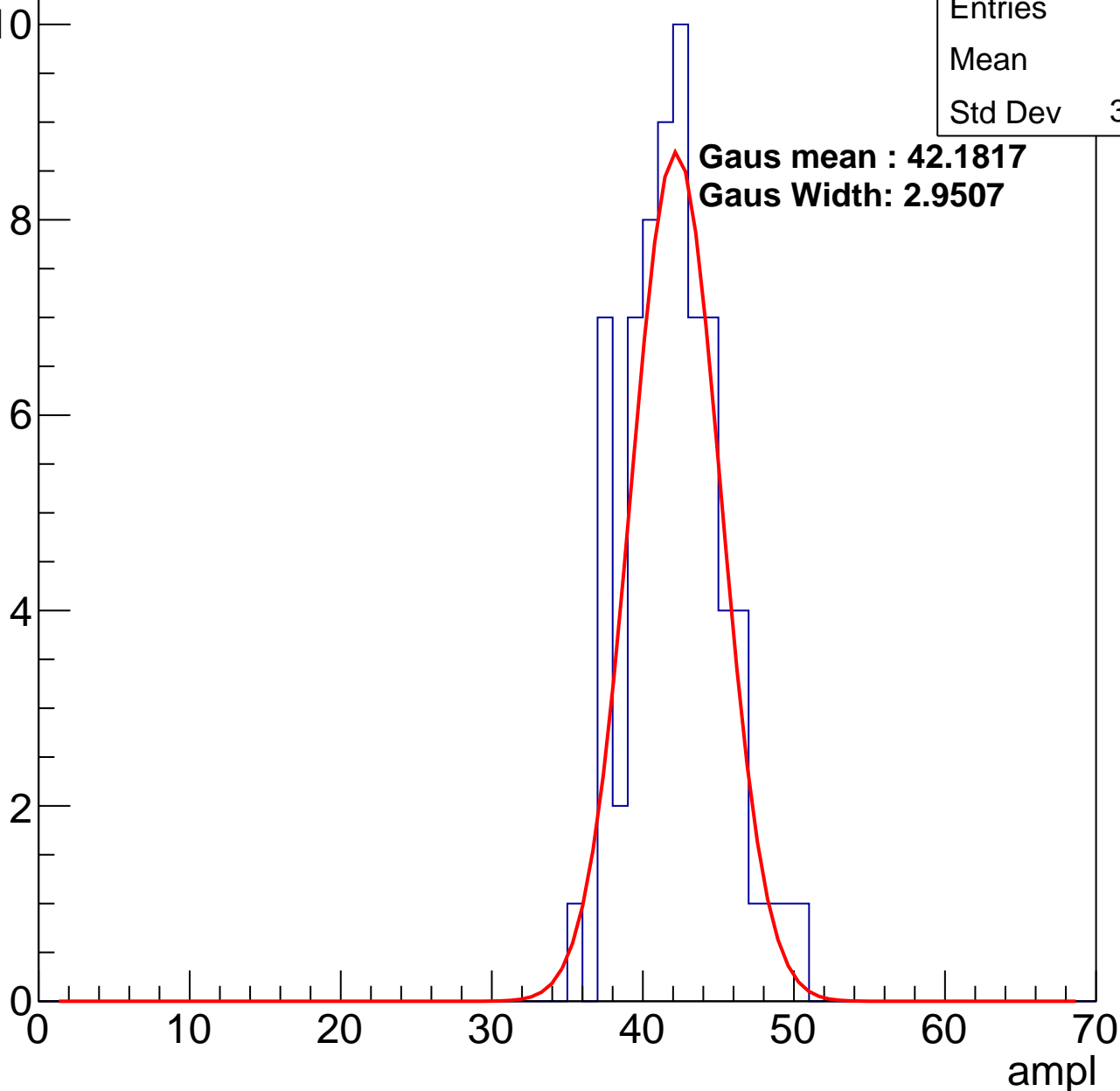
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	41.7
Std Dev	3.077

**Gaus mean : 42.1817**

**Gaus Width: 2.9507**

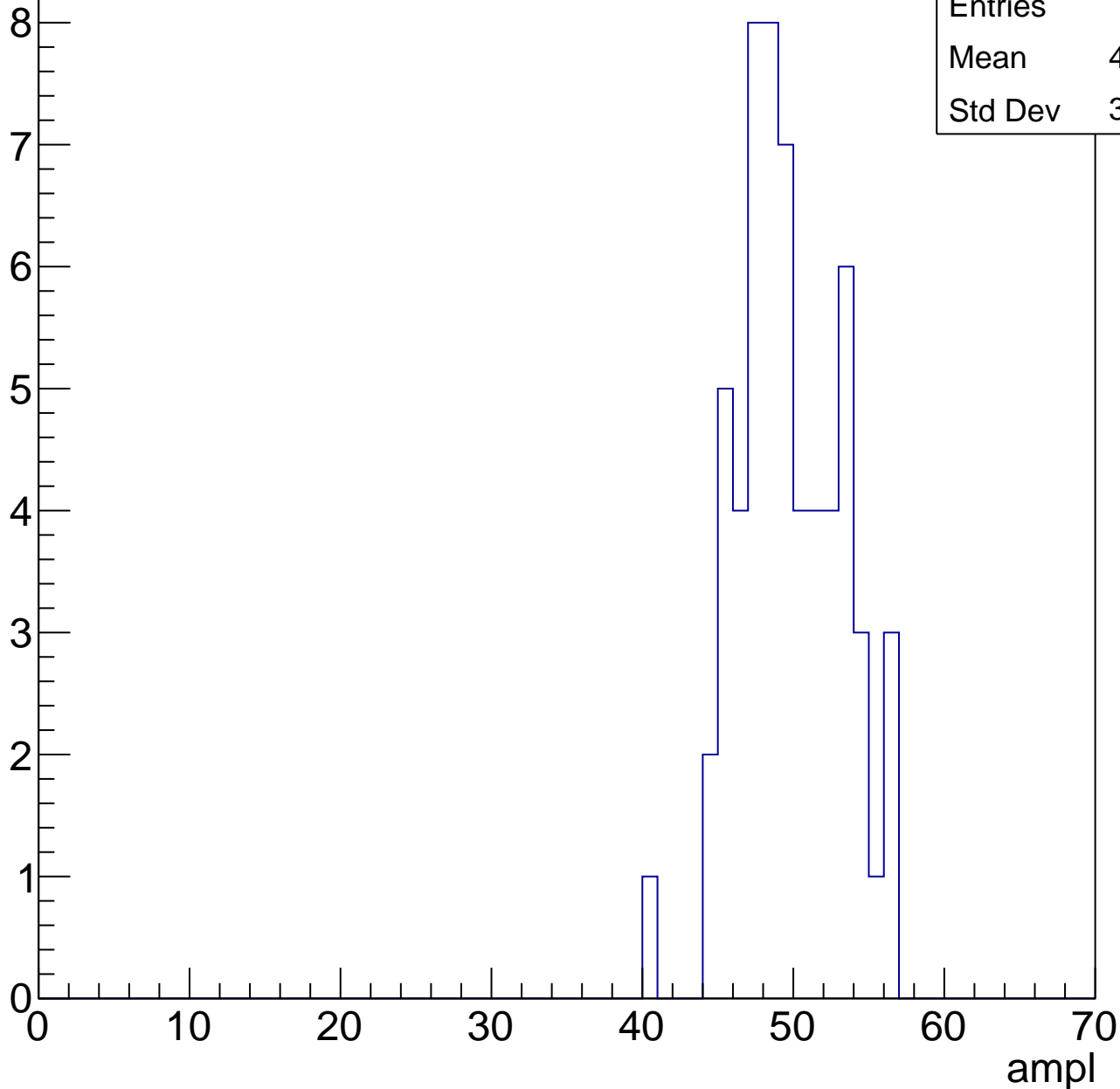


# B1L103S, U16-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	49.25
Std Dev	3.399

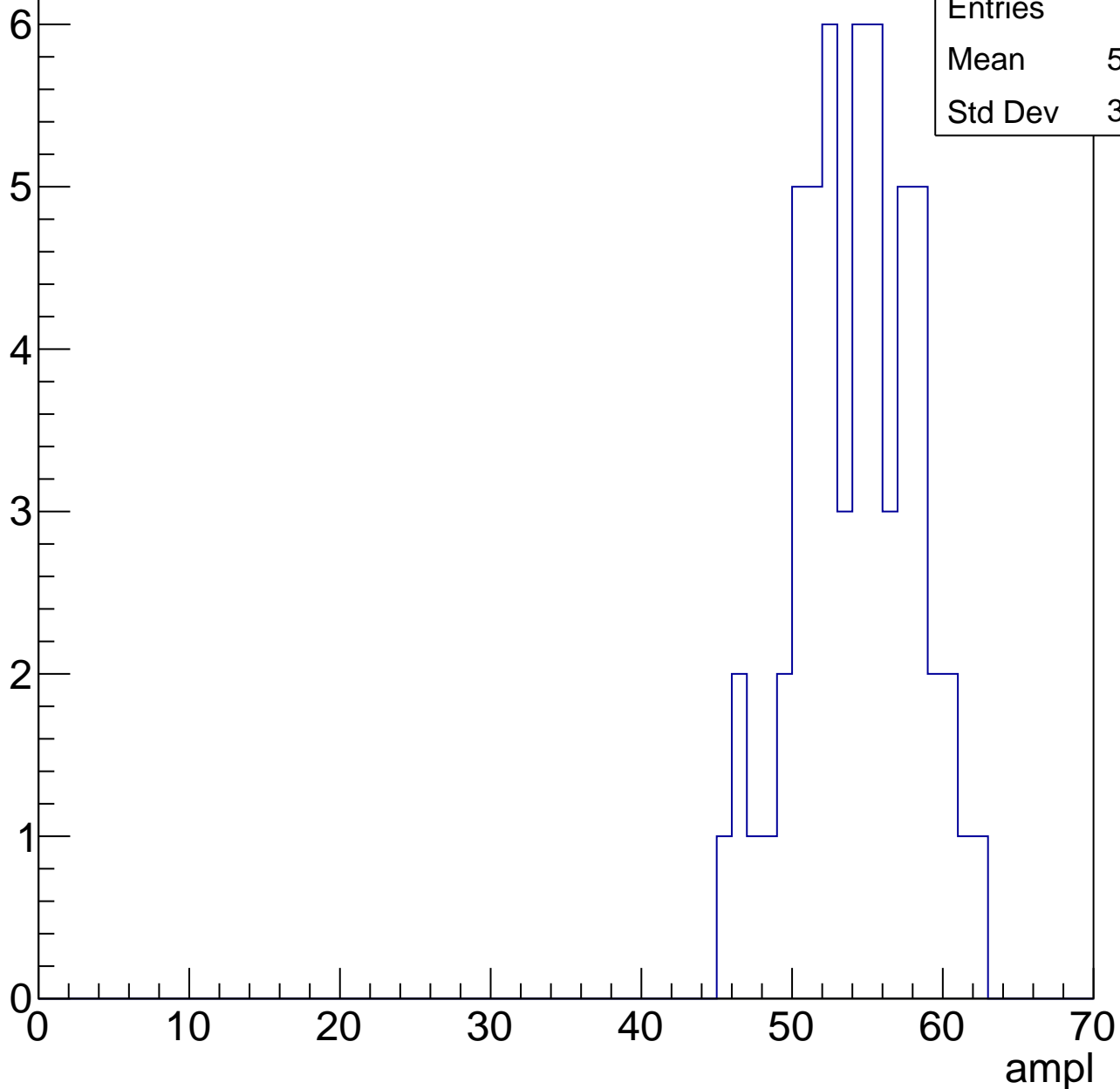


# B1L103S, U16-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	53.75
Std Dev	3.908

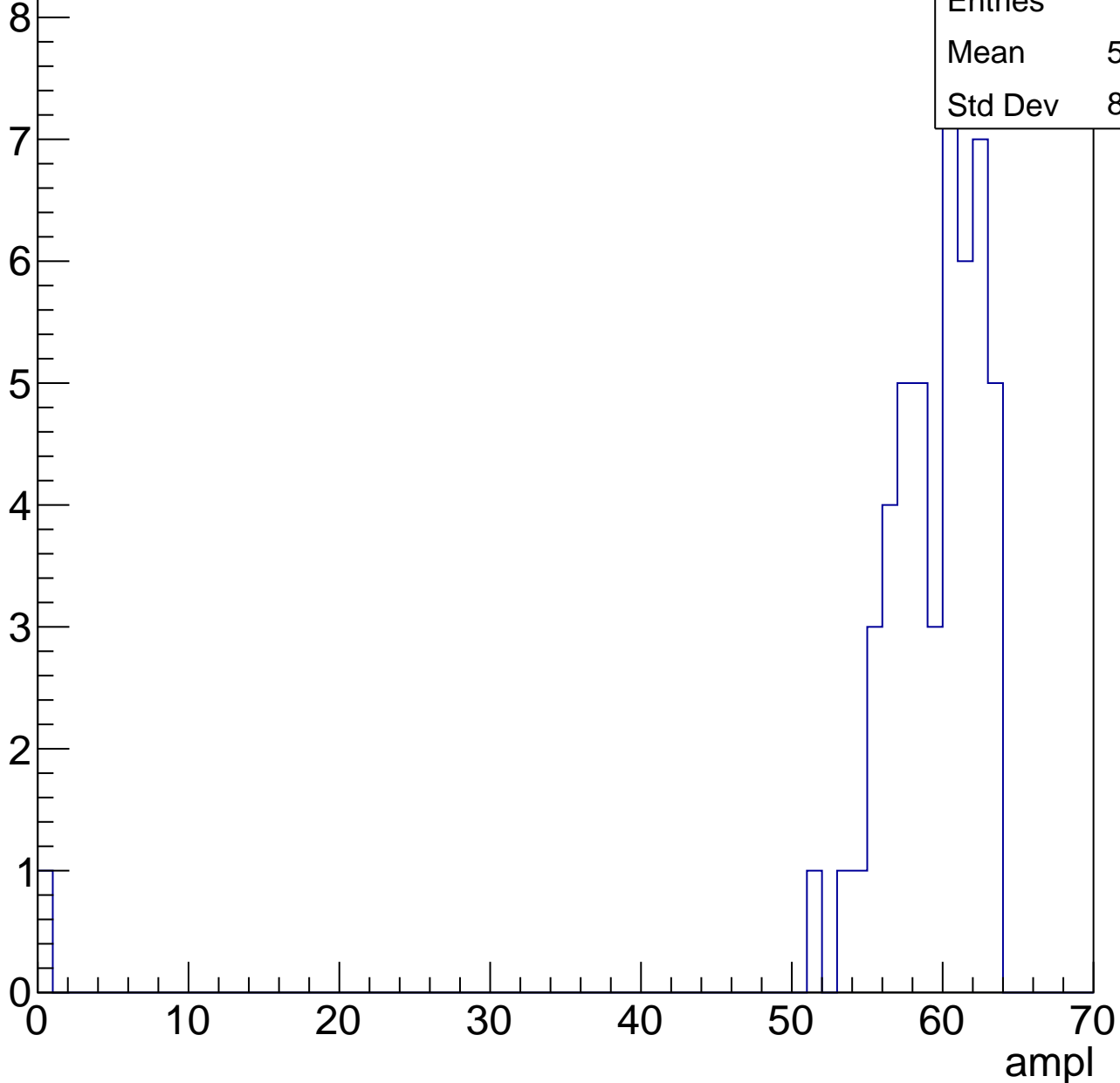


# B1L103S, U16-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	57.88
Std Dev	8.749



# B1L103S, U16-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

5

4

3

2

1

0

0

10

20

30

40

50

60

70

ampl

Entries

14

Mean

61

Std Dev

1.648

5  
4  
3  
2  
1  
0

0

10

20

30

40

50

60

70

ampl

Entries

14

Mean

61

Std Dev

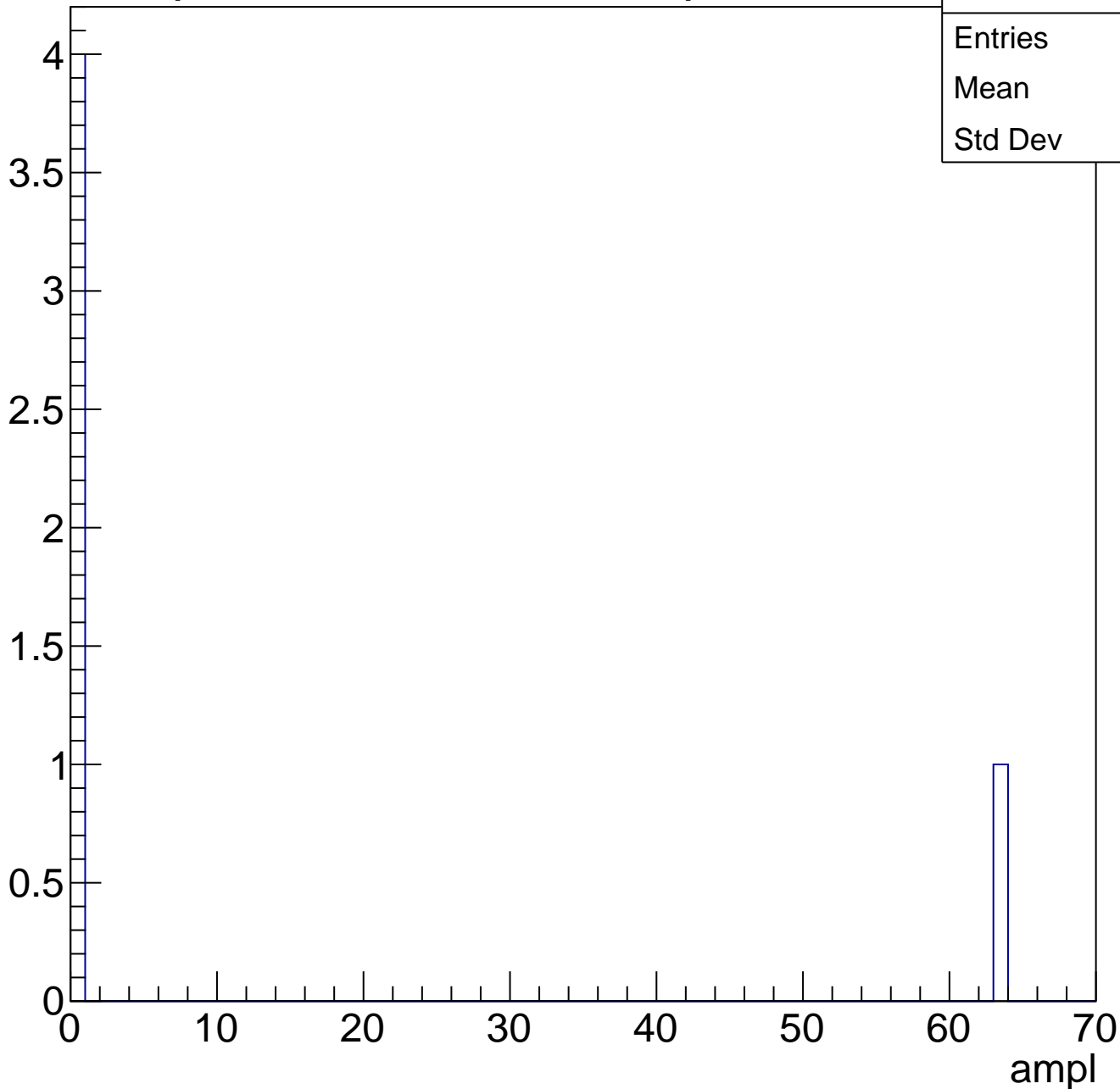
1.648



# B1L103S, U16-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch95, adc0

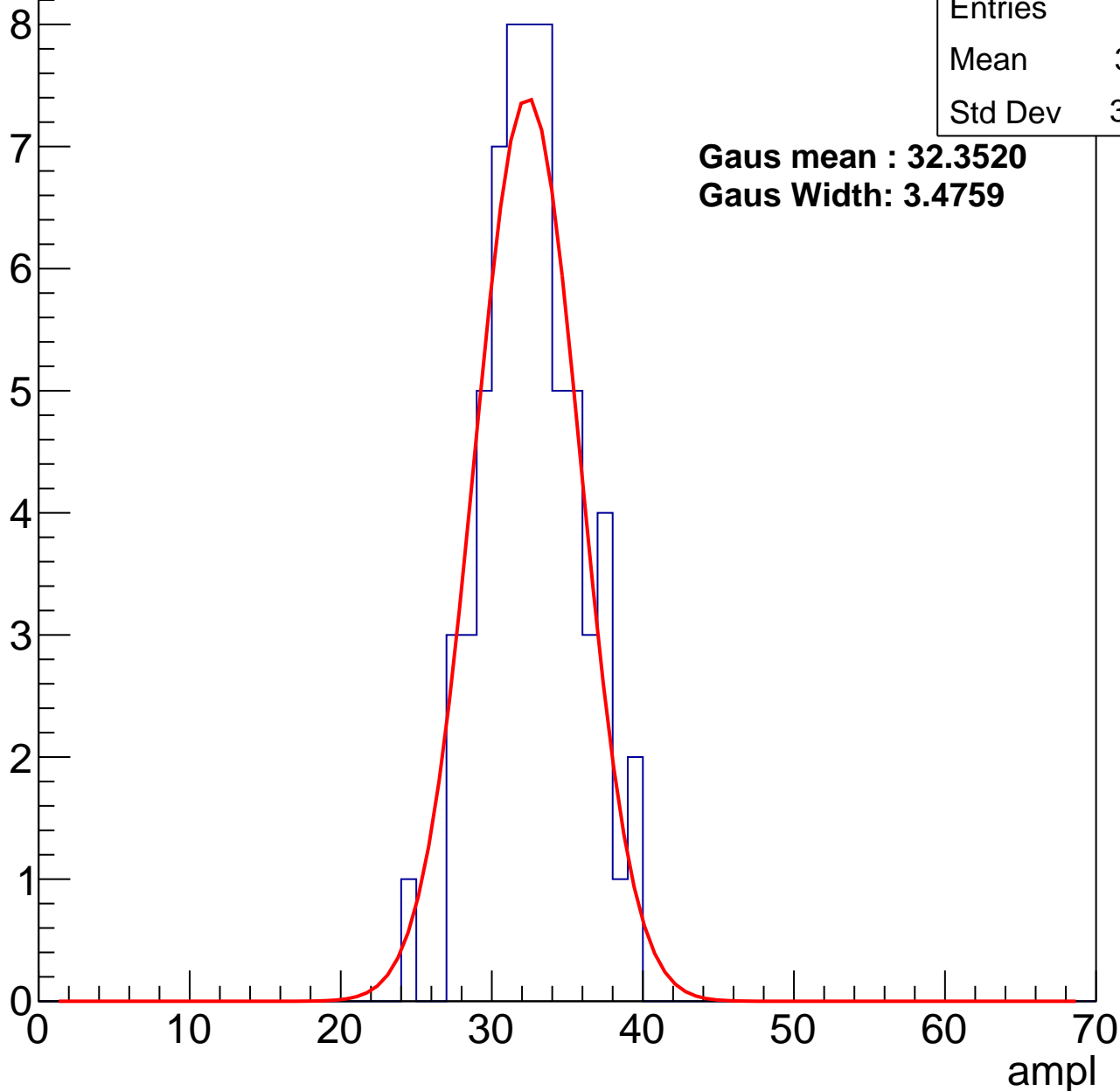
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	32.21
Std Dev	3.138

**Gaus mean : 32.3520**

**Gaus Width: 3.4759**



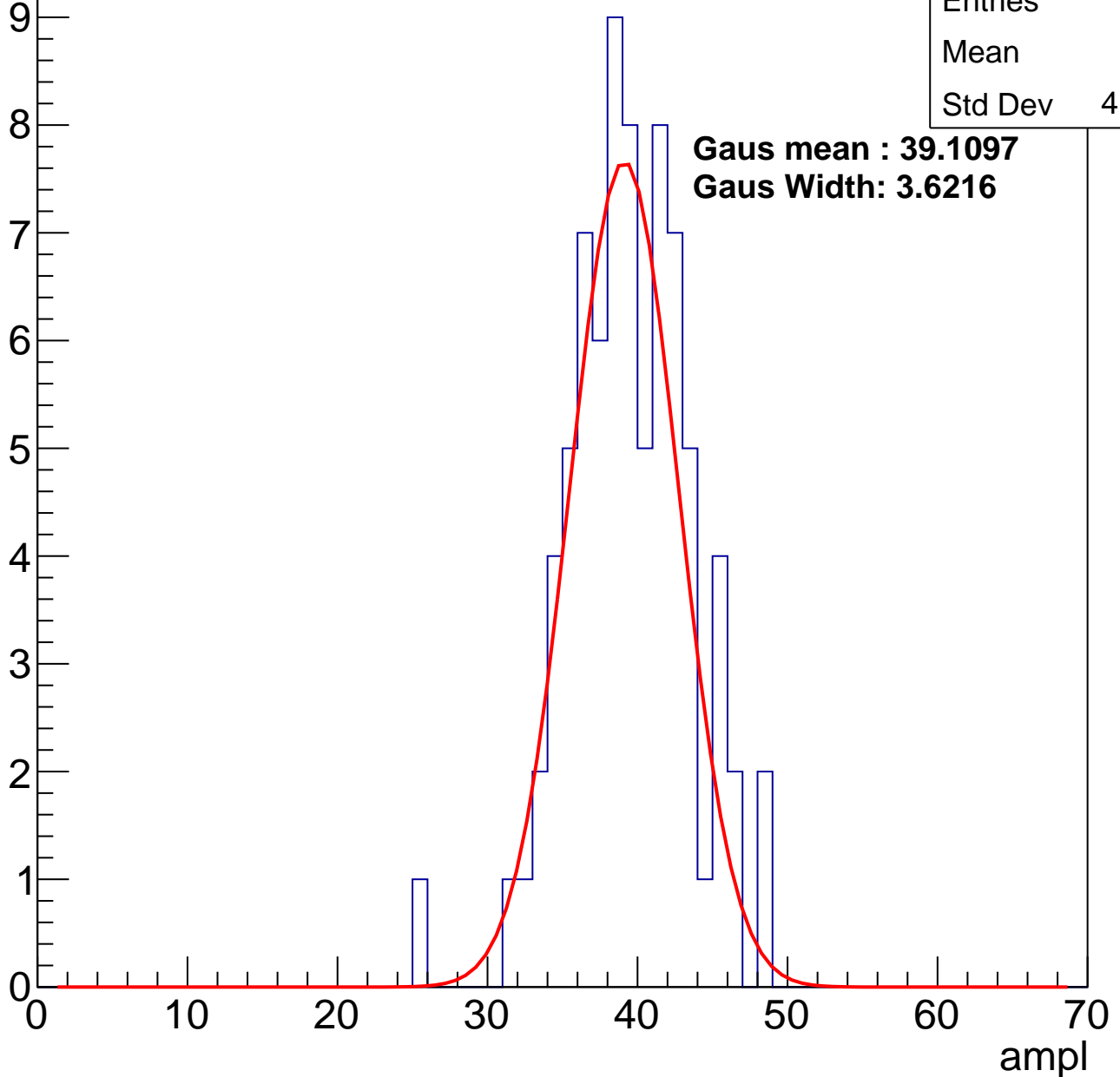
# B1L103S, U16-ch95, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	39
Std Dev	4.029

**Gaus mean : 39.1097**  
**Gaus Width: 3.6216**



# B1L103S, U16-ch95, adc2

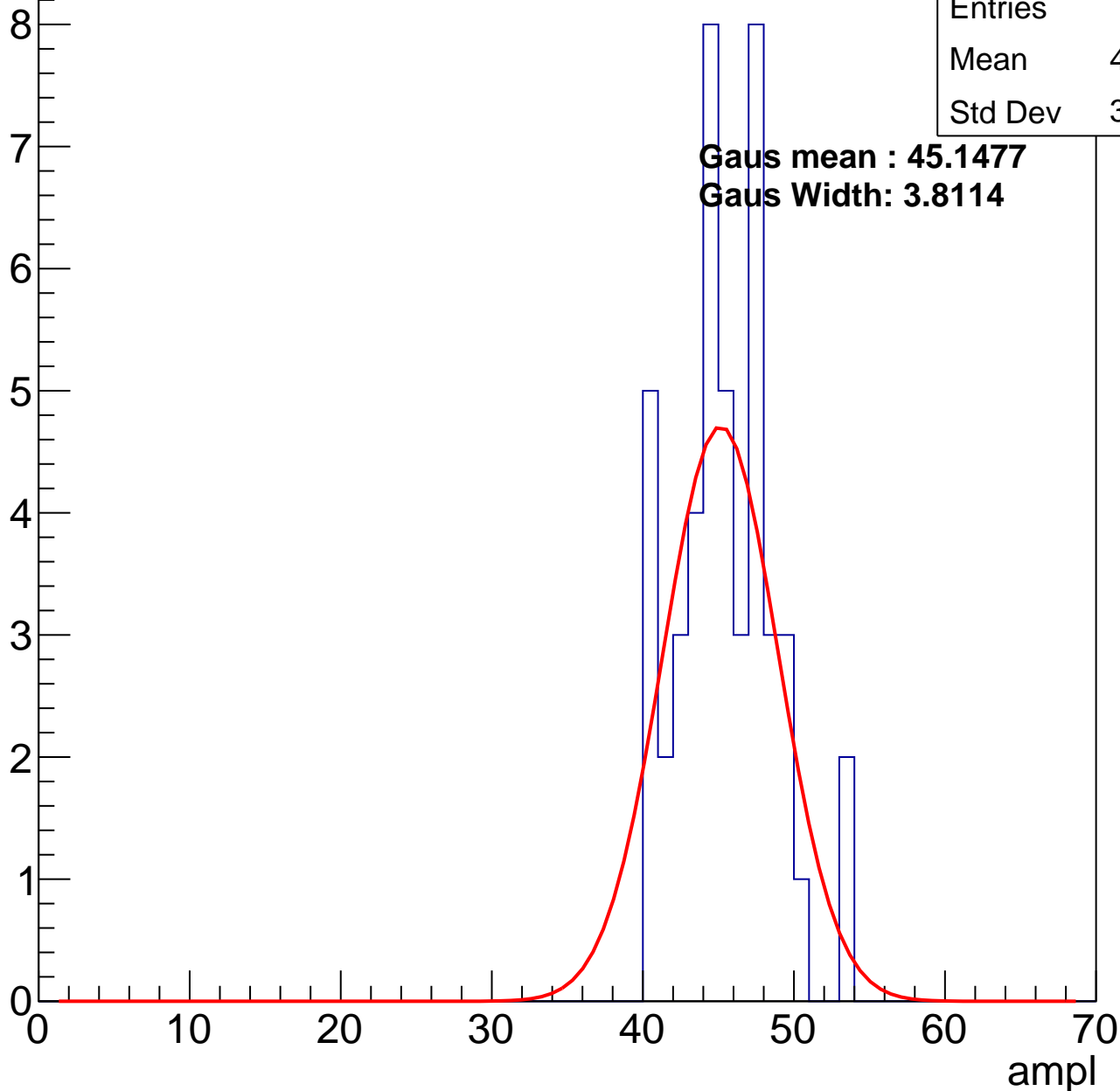
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	45.06
Std Dev	3.165

**Gaus mean : 45.1477**

**Gaus Width: 3.8114**

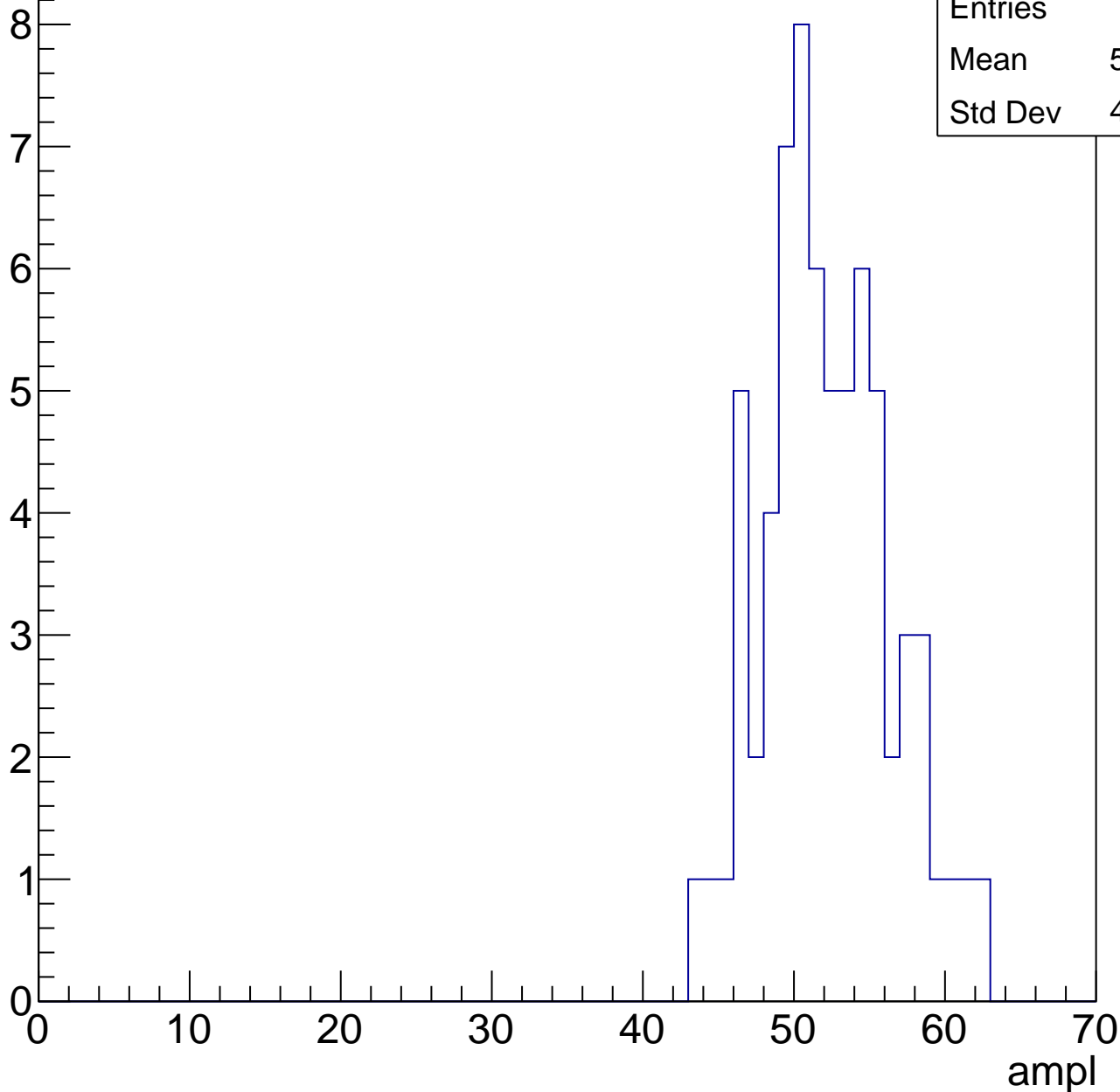


# B1L103S, U16-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	51.76
Std Dev	4.145

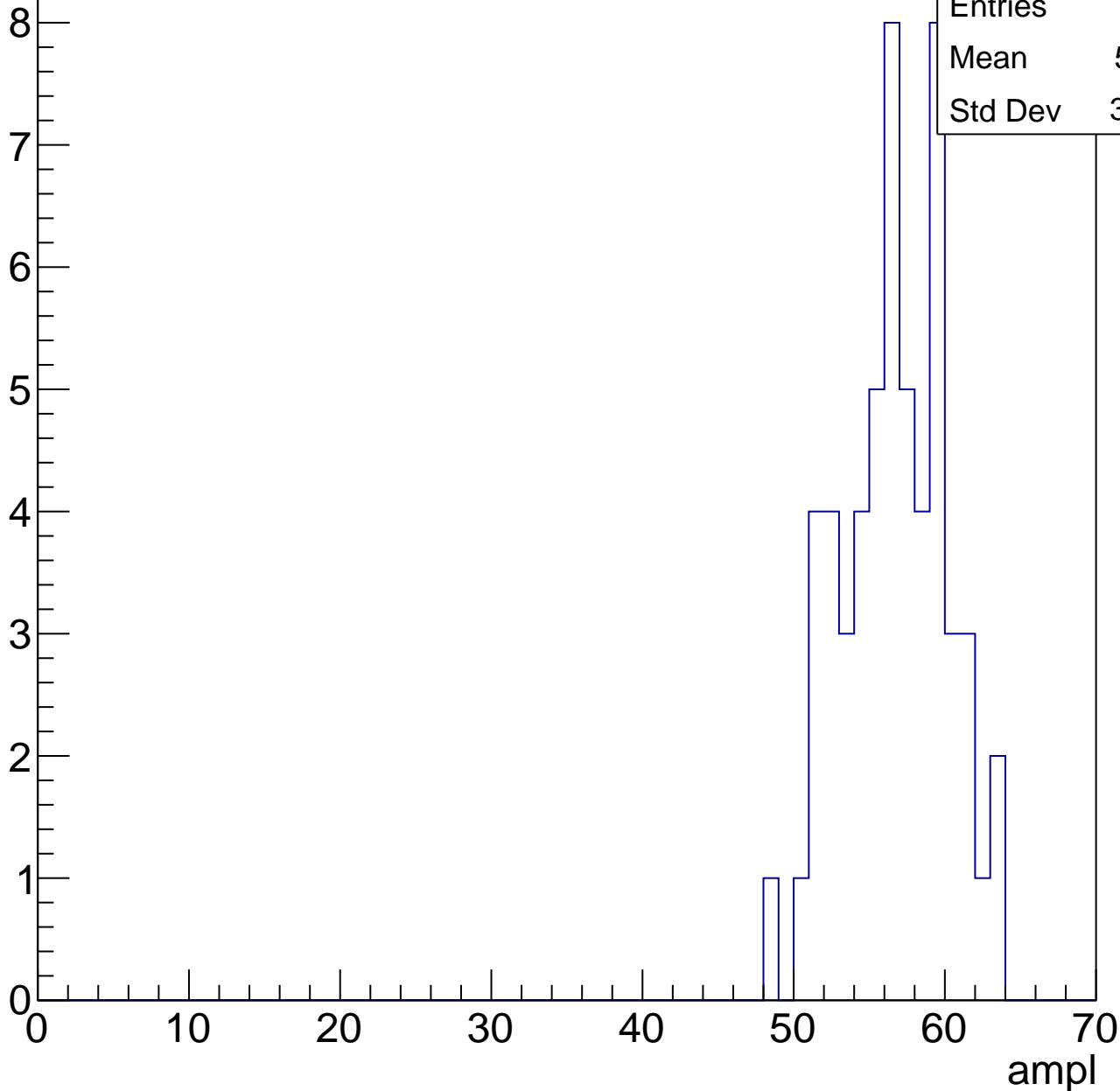


# B1L103S, U16-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	56.21
Std Dev	3.432

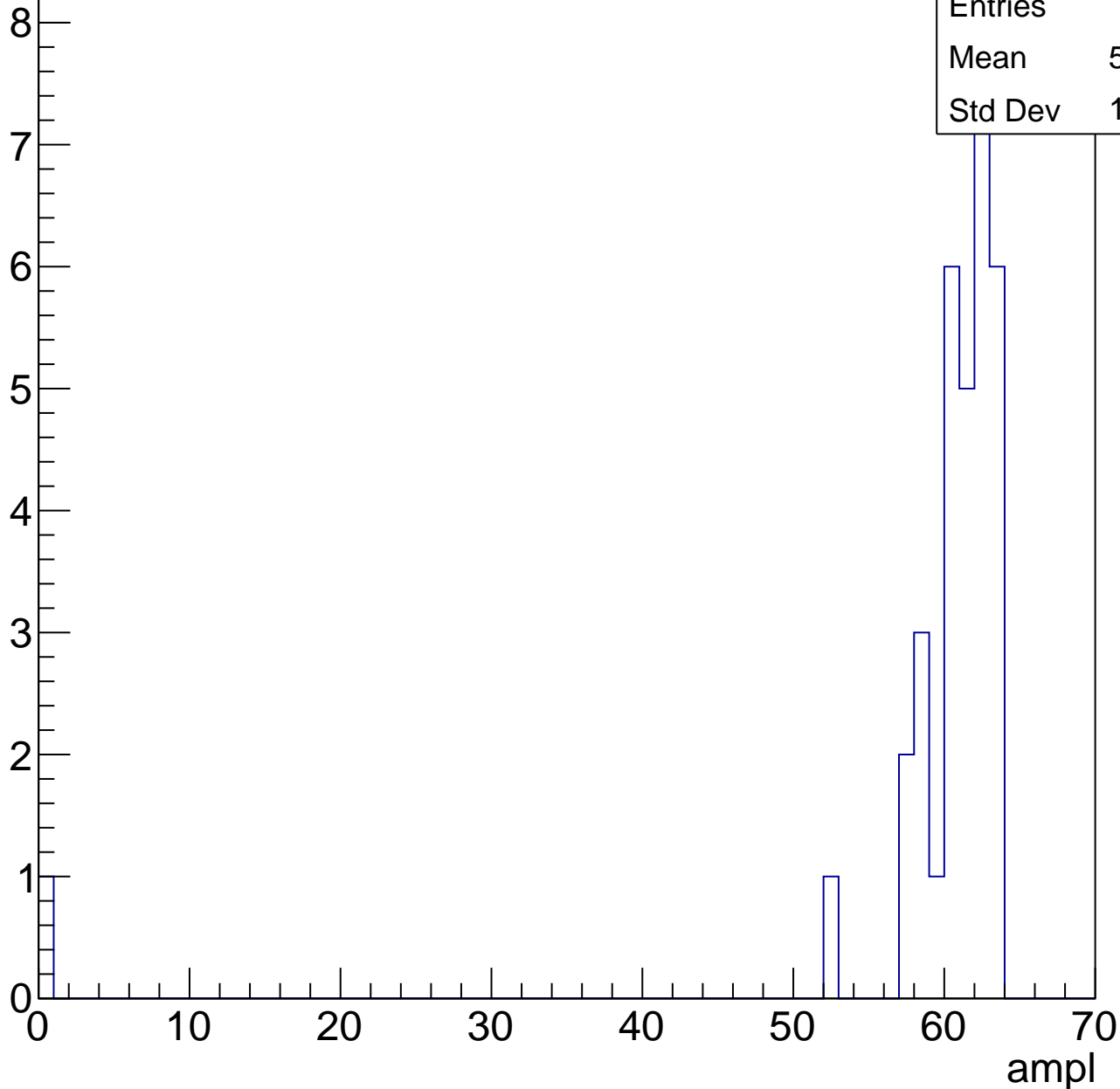


# B1L103S, U16-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	33
Mean	58.73
Std Dev	10.64



# B1L103S, U16-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

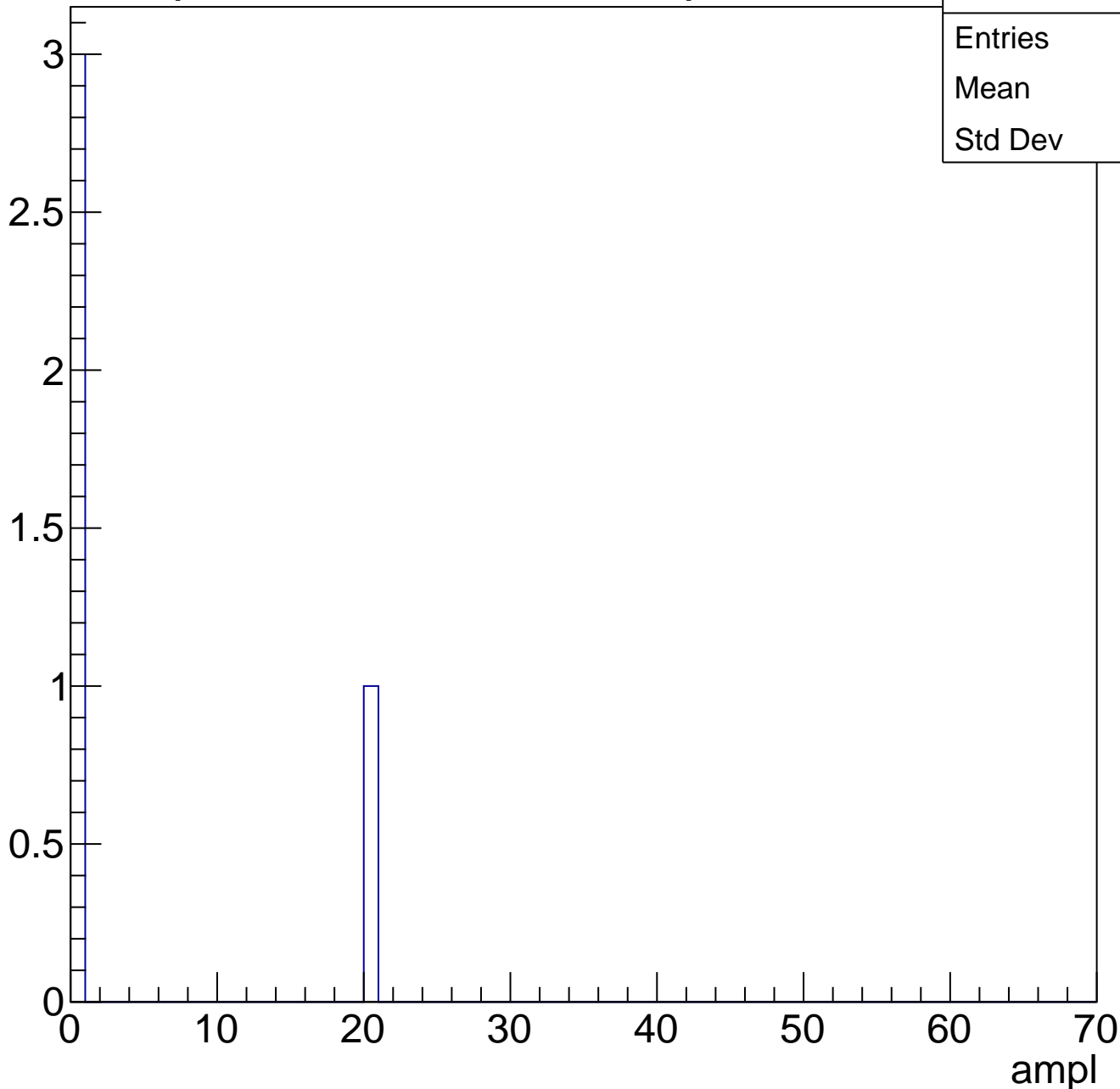




# B1L103S, U16-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	4
Mean	5
Std Dev	8.66

# B1L103S, U16-ch96, adc0

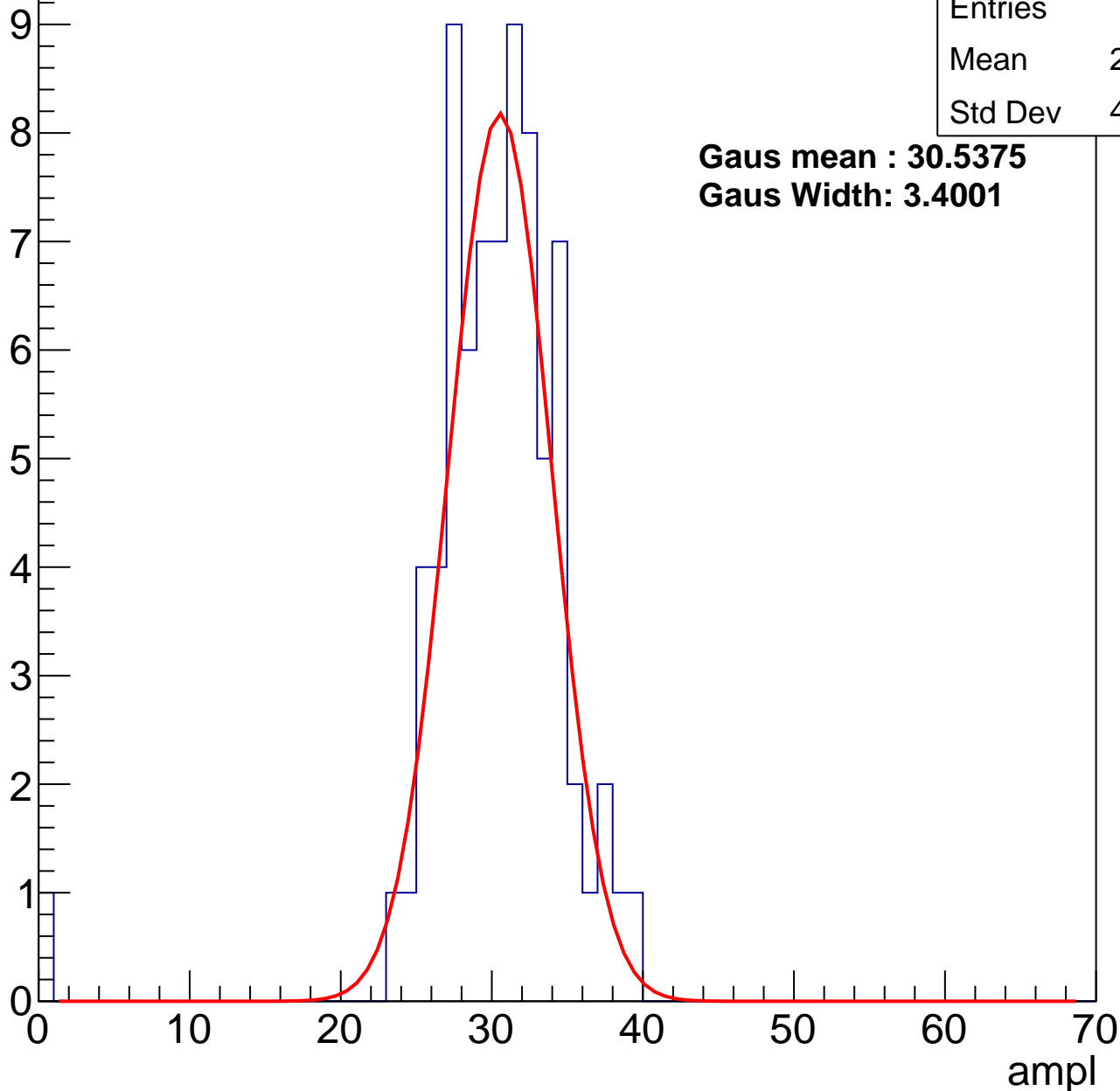
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	29.87
Std Dev	4.849

**Gaus mean : 30.5375**

**Gaus Width: 3.4001**



# B1L103S, U16-ch96, adc1

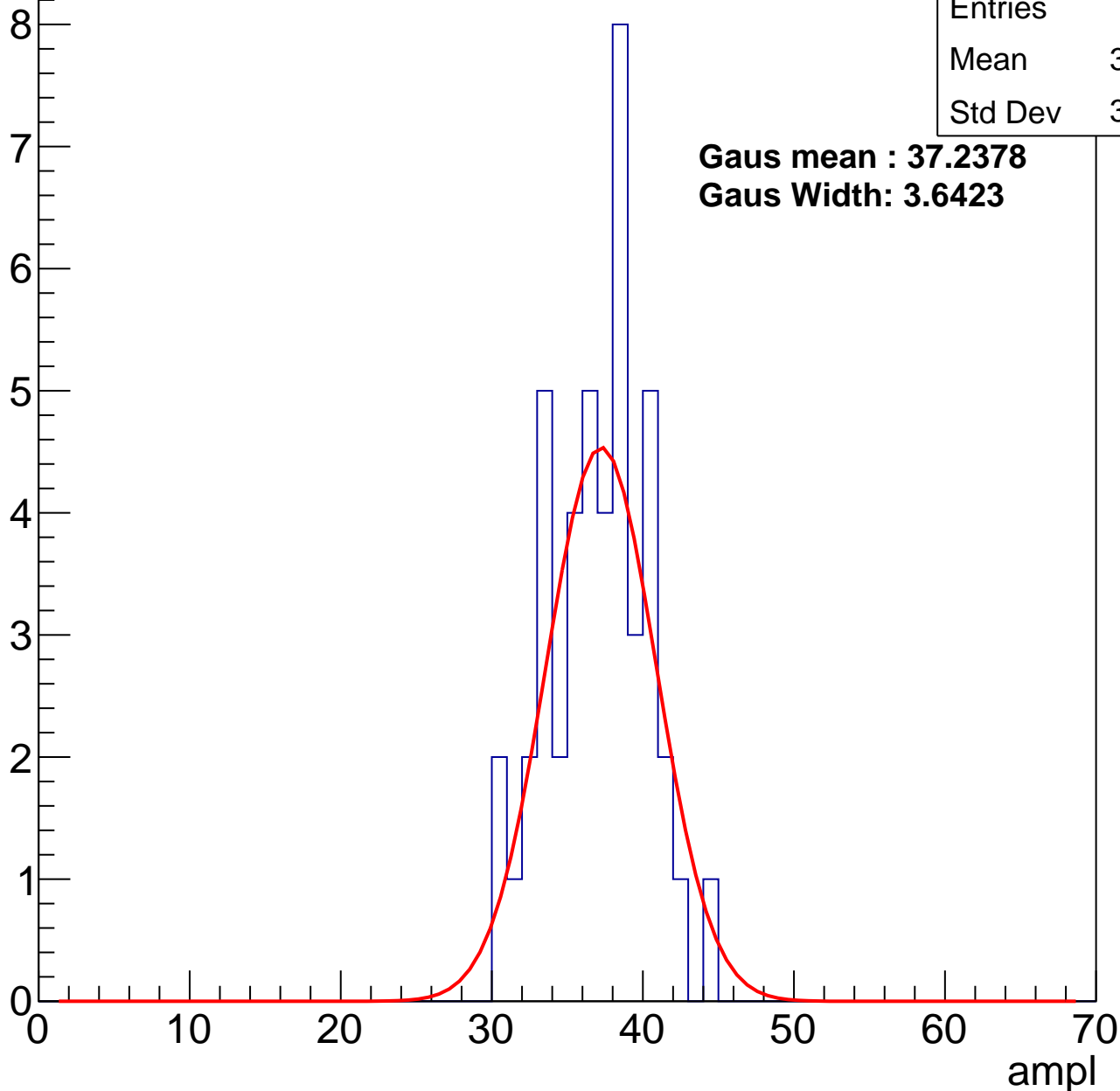
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	36.56
Std Dev	3.215

**Gaus mean : 37.2378**

**Gaus Width: 3.6423**



# B1L103S, U16-ch96, adc2

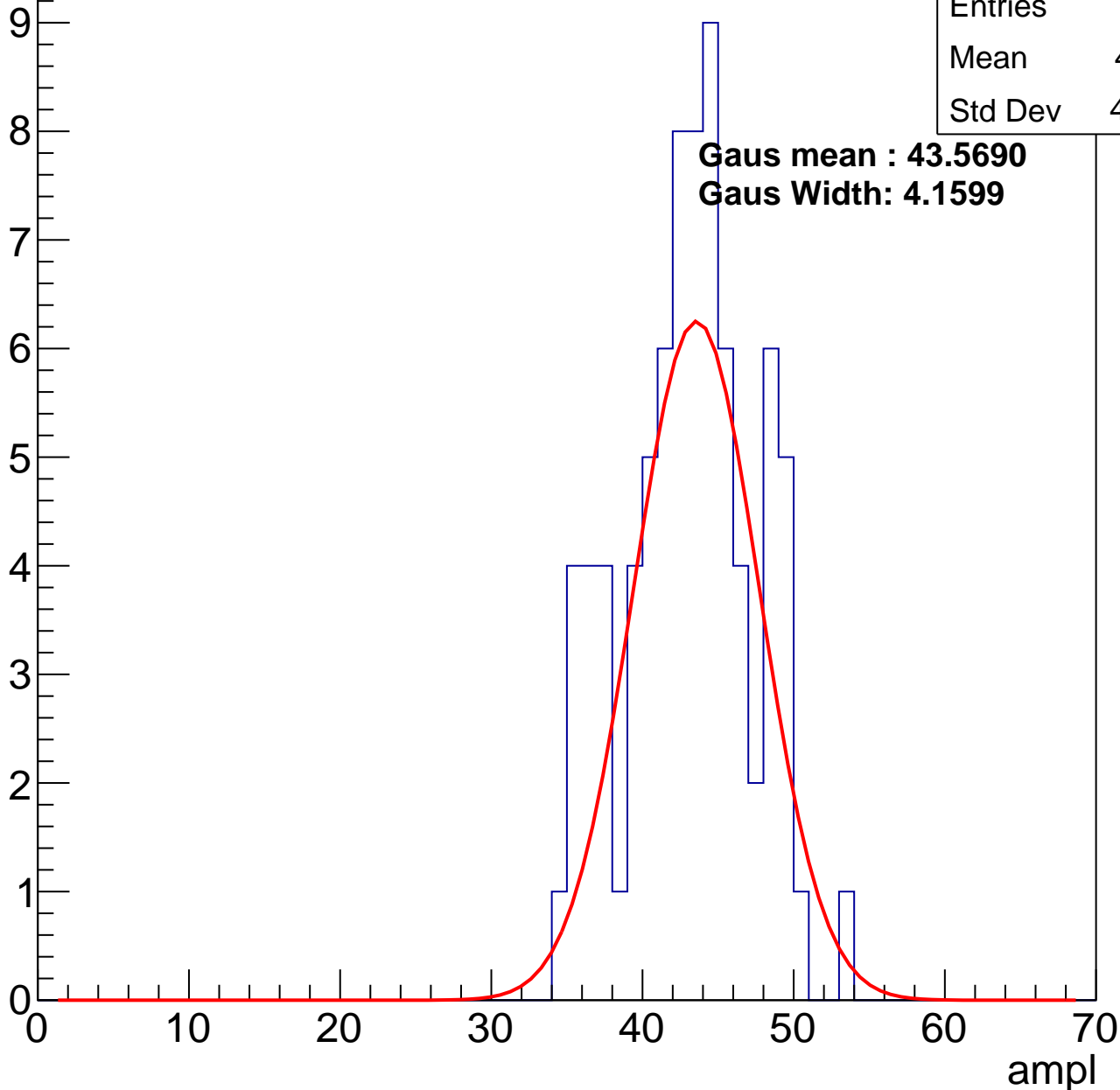
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	42.61
Std Dev	4.226

**Gaus mean : 43.5690**

**Gaus Width: 4.1599**

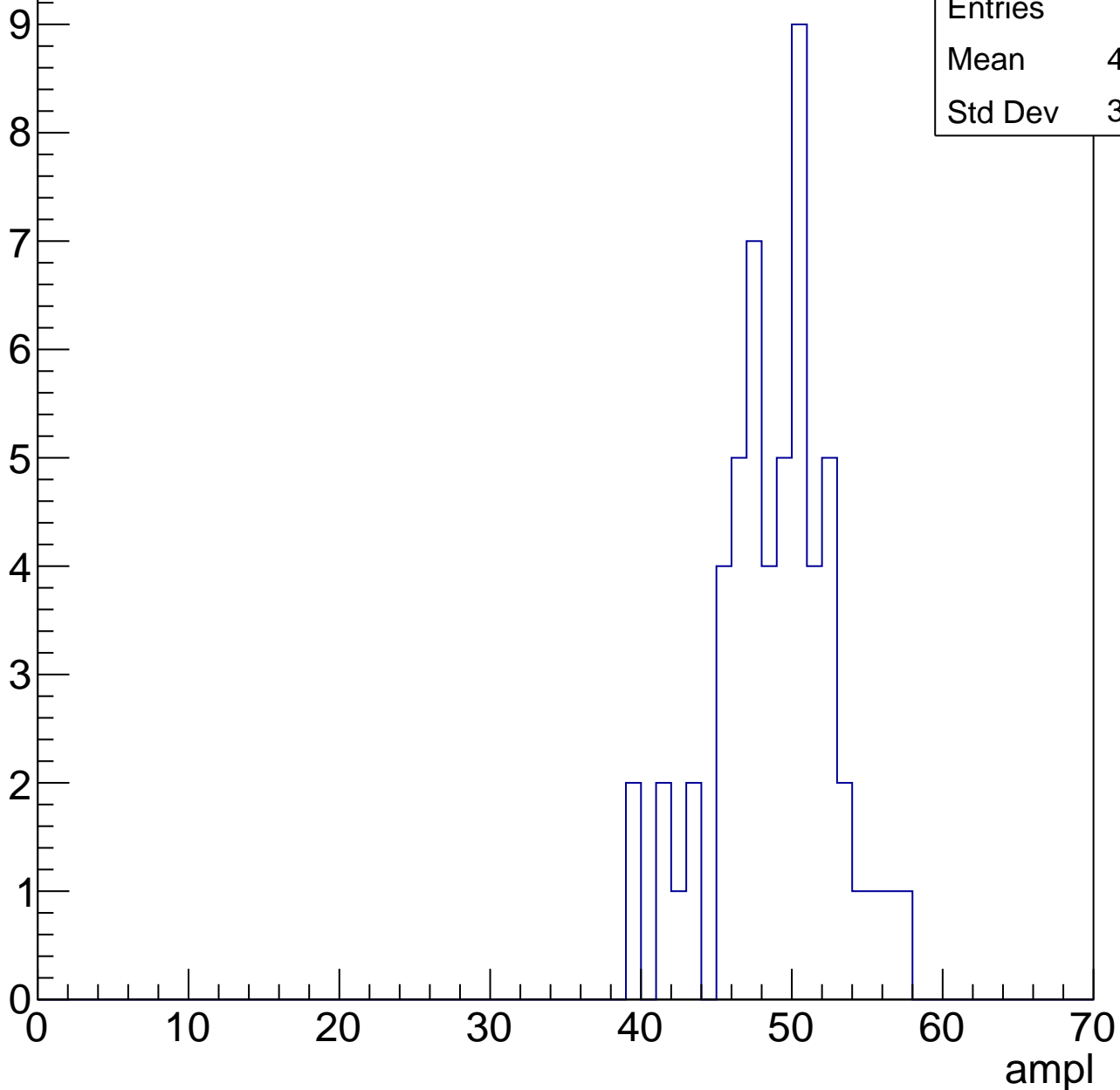


# B1L103S, U16-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	48.32
Std Dev	3.873

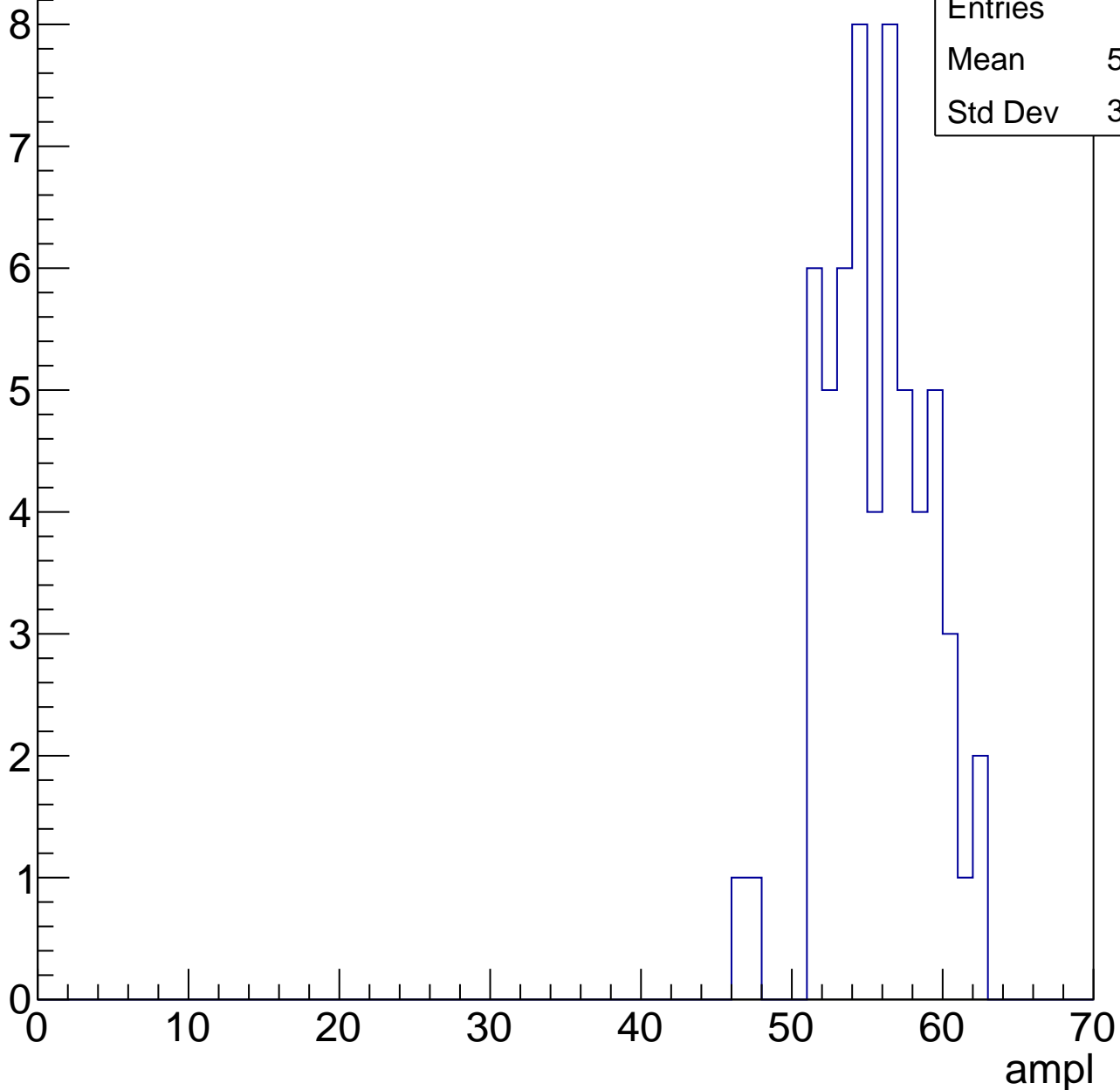


# B1L103S, U16-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	55.15
Std Dev	3.369

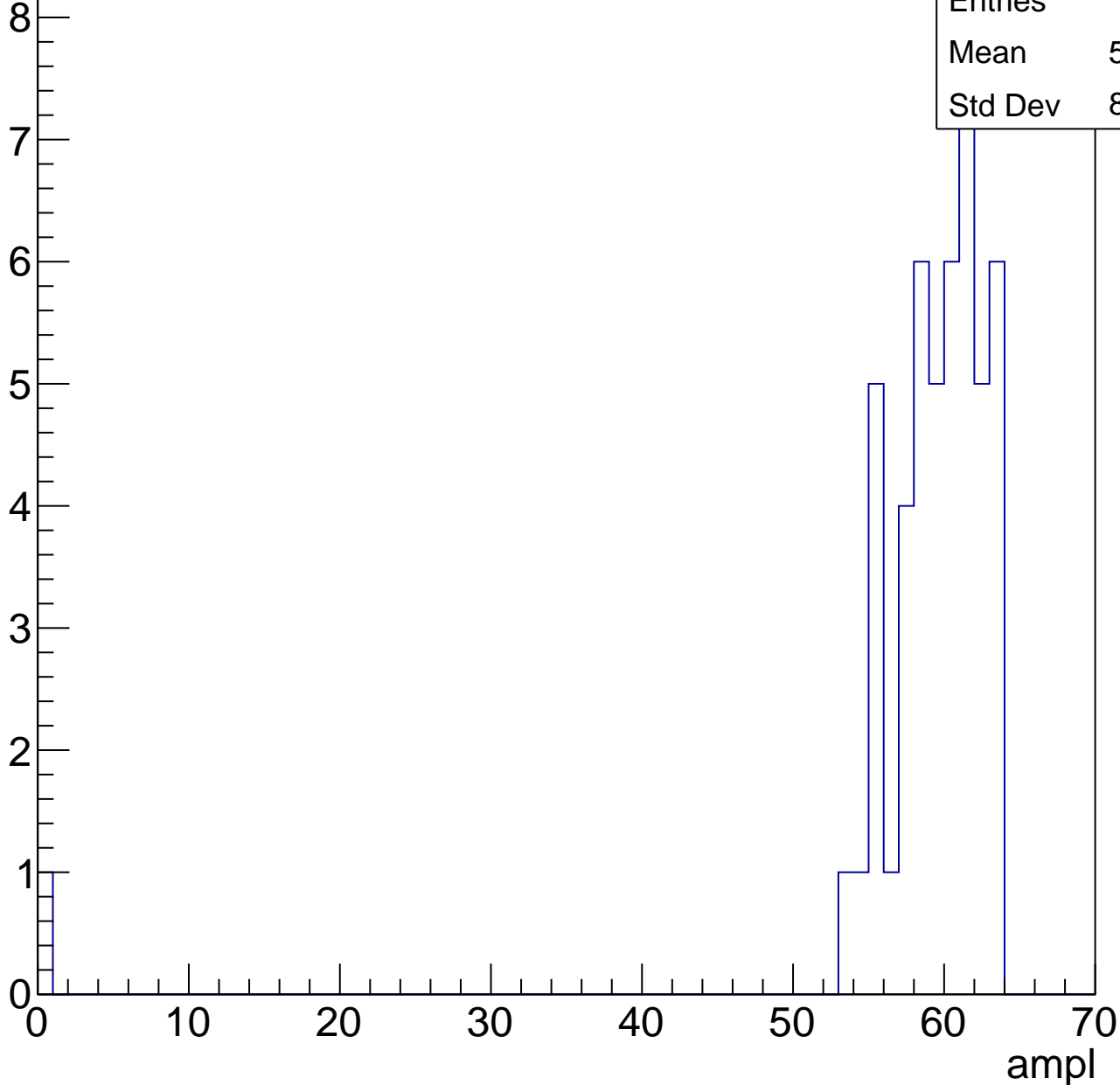


# B1L103S, U16-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	58.06
Std Dev	8.793



# B1L103S, U16-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	7
Std Dev	9.899

# B1L103S, U16-ch97, adc0

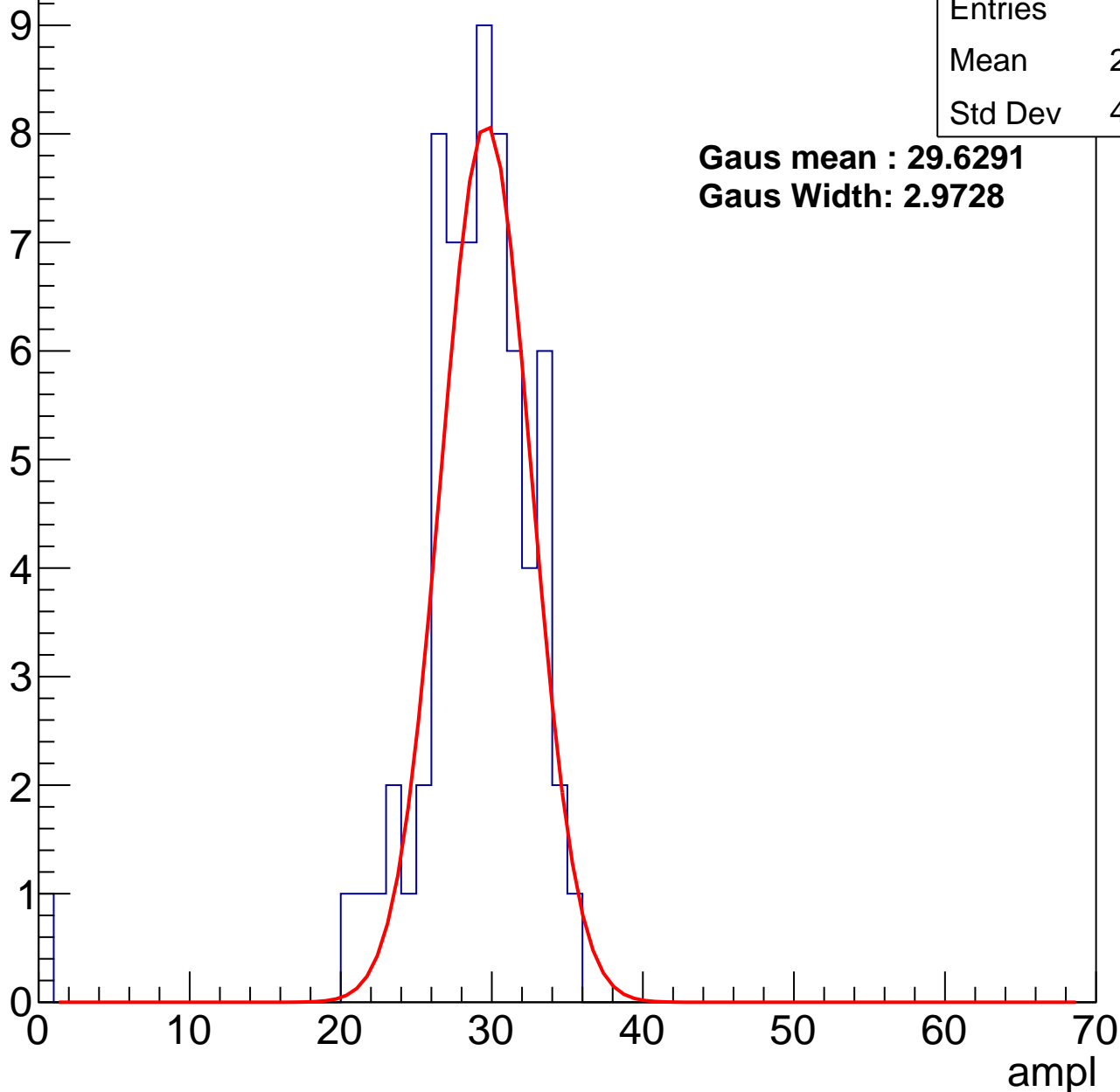
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	28.24
Std Dev	4.703

**Gaus mean : 29.6291**

**Gaus Width: 2.9728**



# B1L103S, U16-ch97, adc1

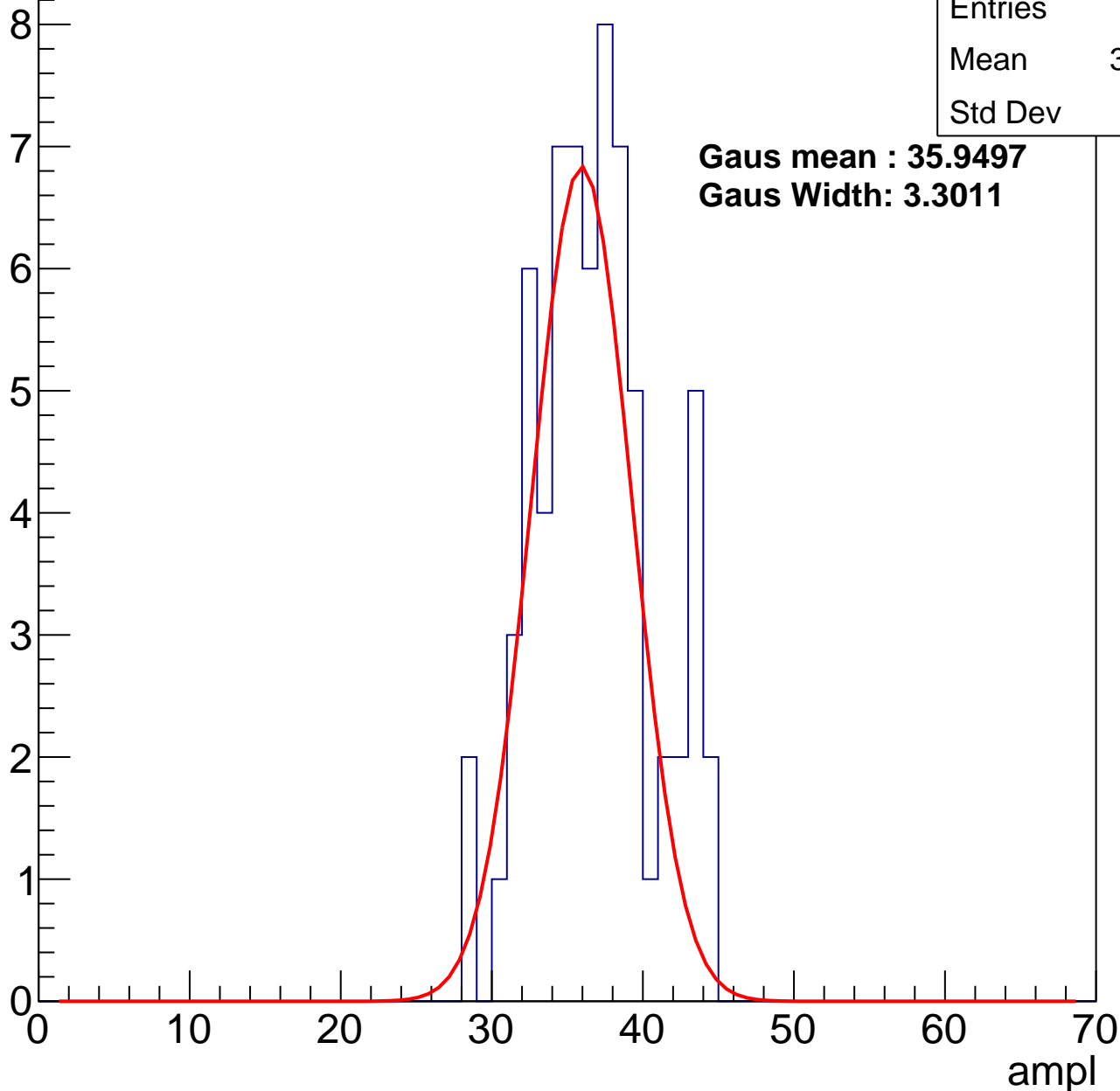
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	36.29
Std Dev	3.82

**Gaus mean : 35.9497**

**Gaus Width: 3.3011**



# B1L103S, U16-ch97, adc2

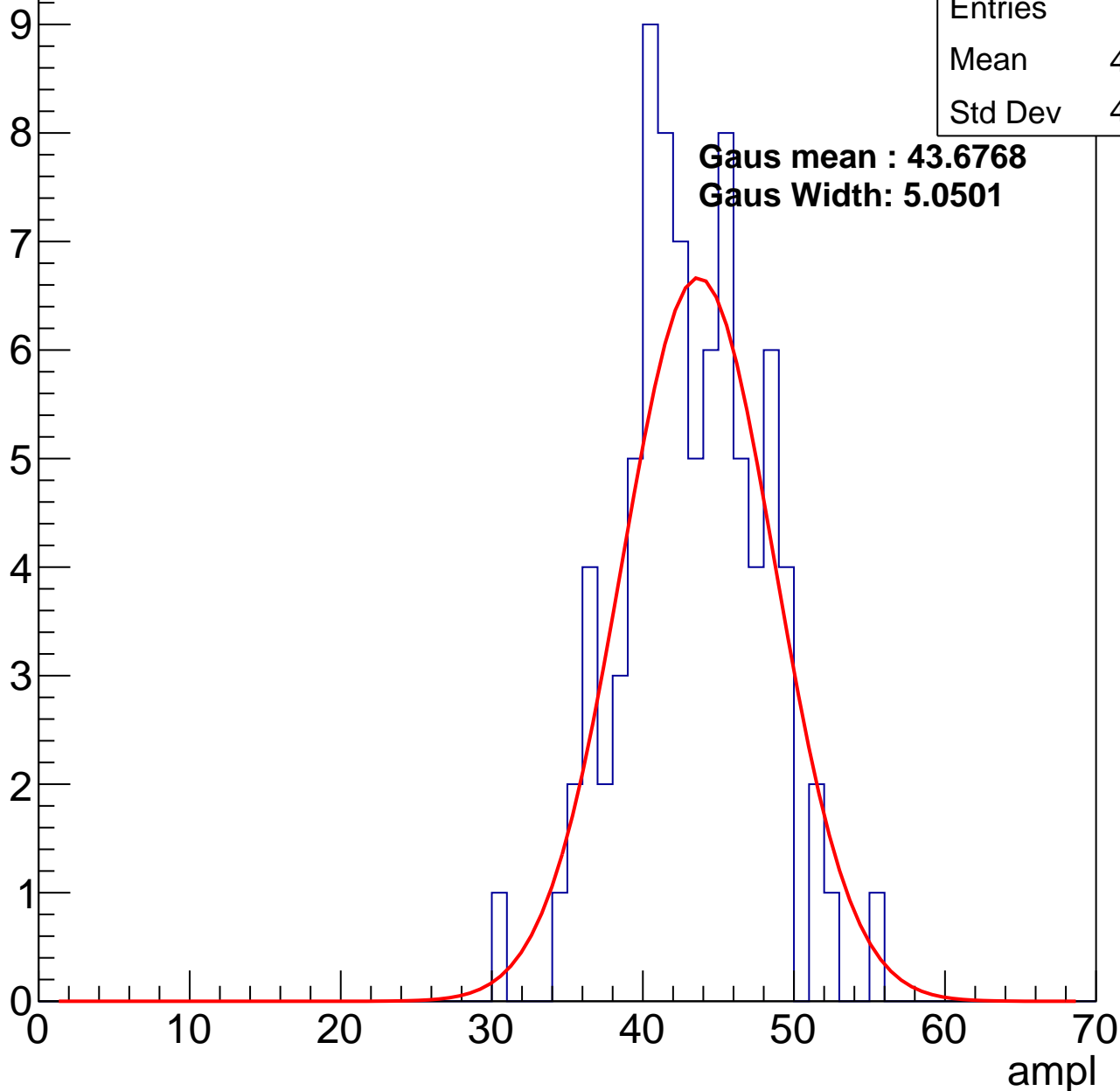
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	84
Mean	42.77
Std Dev	4.513

**Gaus mean : 43.6768**

**Gaus Width: 5.0501**

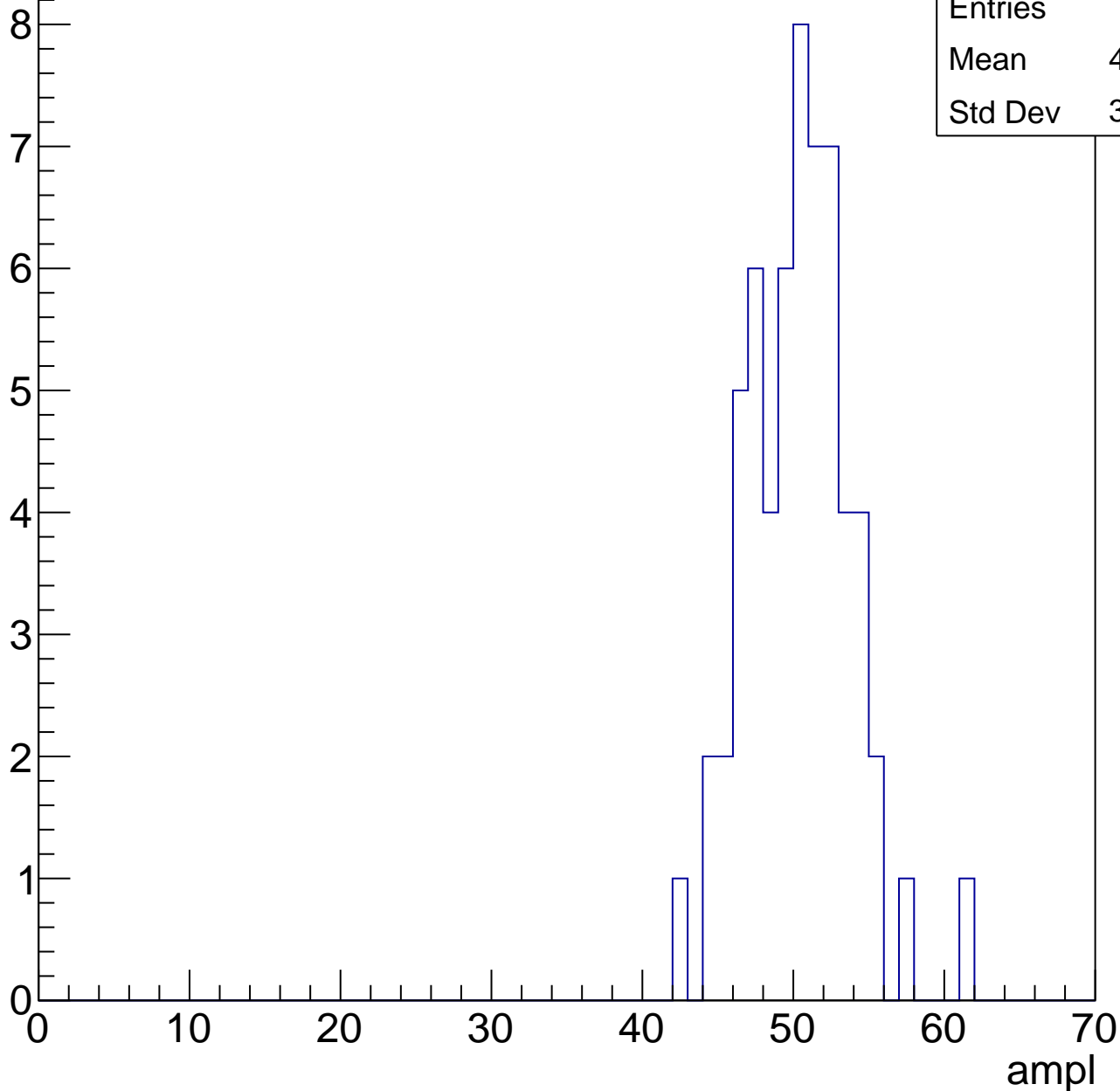


# B1L103S, U16-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	49.92
Std Dev	3.407

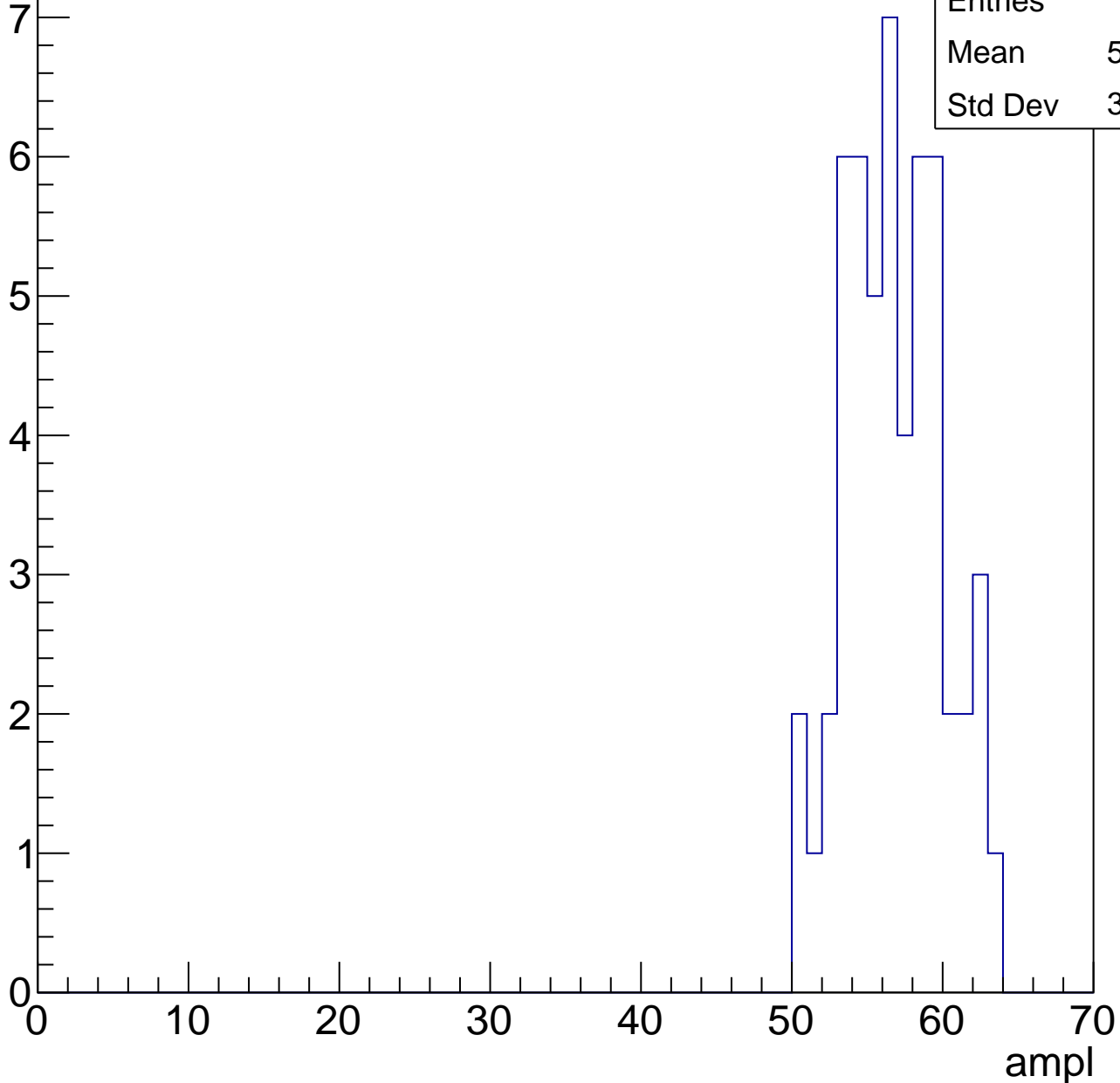


# B1L103S, U16-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	56.32
Std Dev	3.155

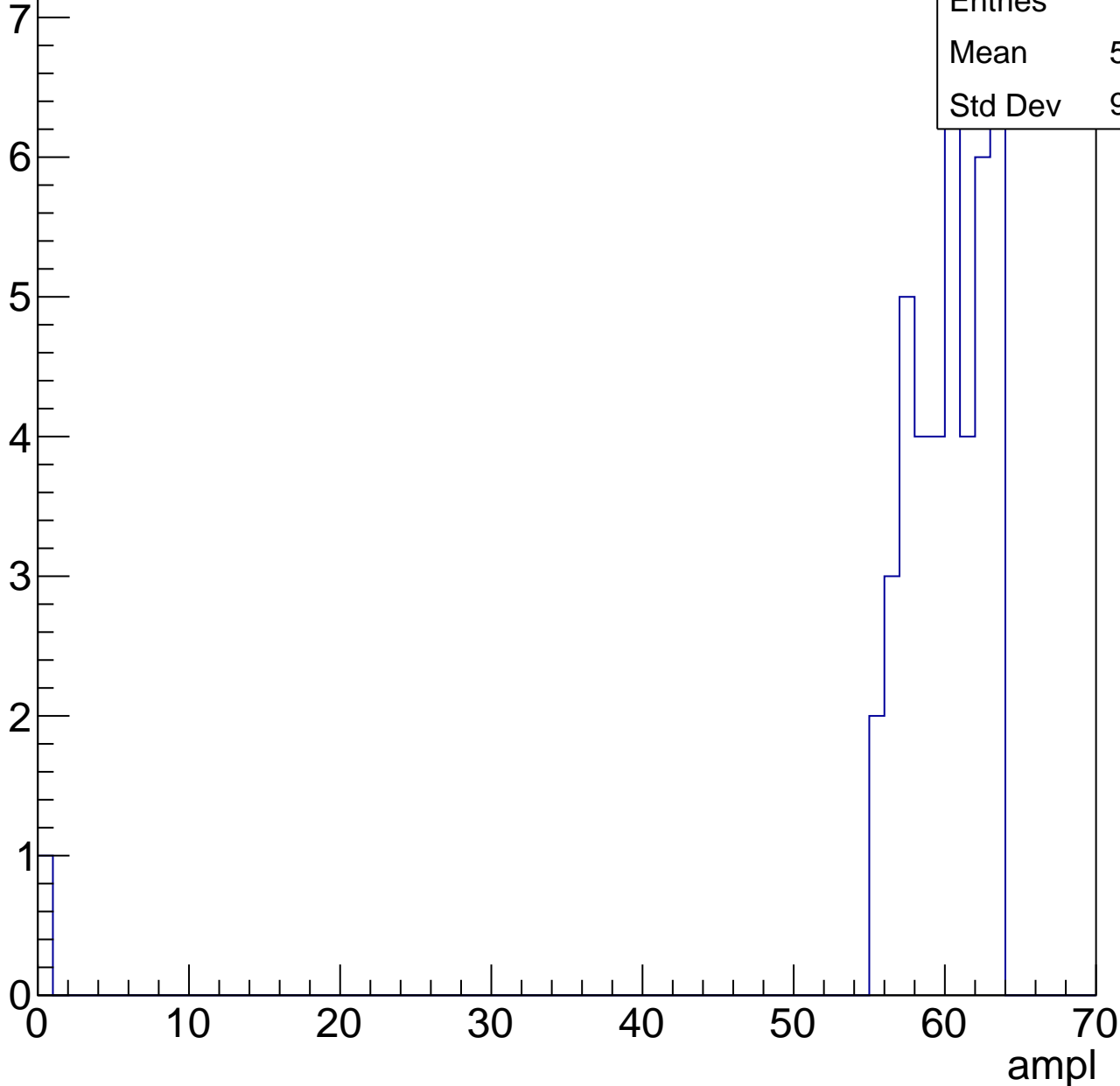


# B1L103S, U16-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	43
Mean	58.33
Std Dev	9.318



# B1L103S, U16-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

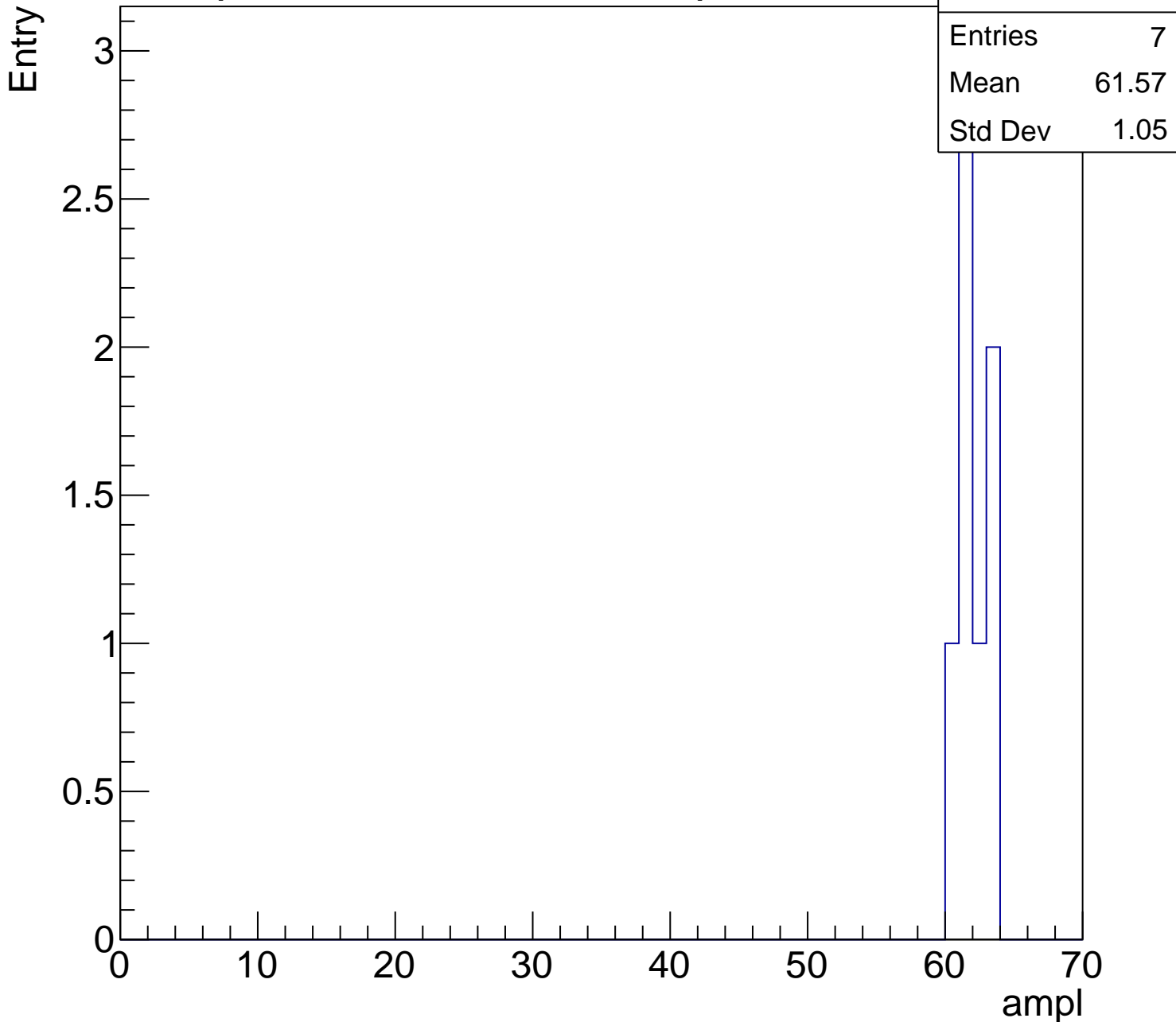
7

Mean

61.57

Std Dev

1.05





# B1L103S, U16-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U16-ch98, adc0

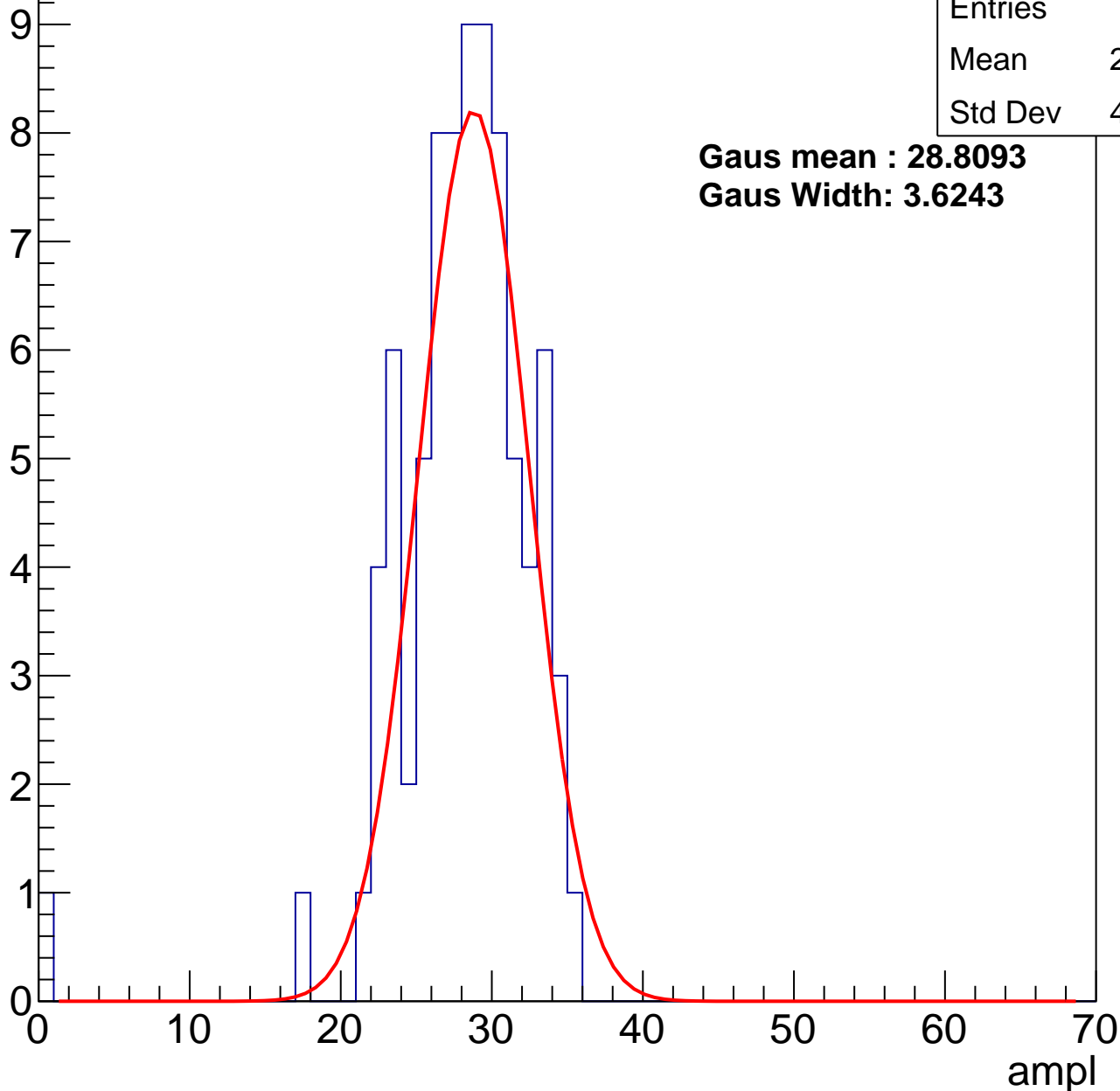
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	81
Mean	27.56
Std Dev	4.722

**Gaus mean : 28.8093**

**Gaus Width: 3.6243**



# B1L103S, U16-ch98, adc1

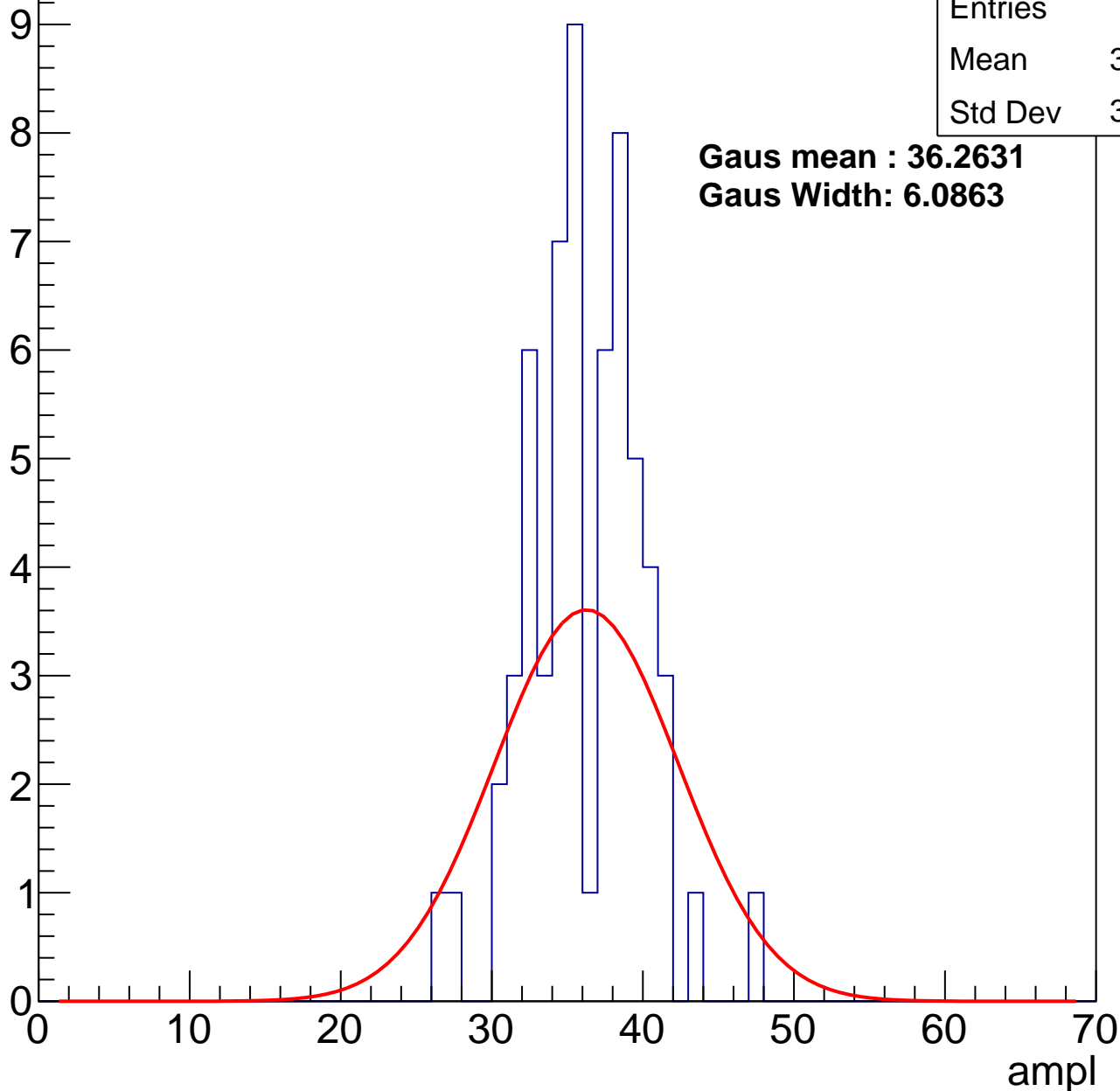
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	35.74
Std Dev	3.789

**Gaus mean : 36.2631**

**Gaus Width: 6.0863**



# B1L103S, U16-ch98, adc2

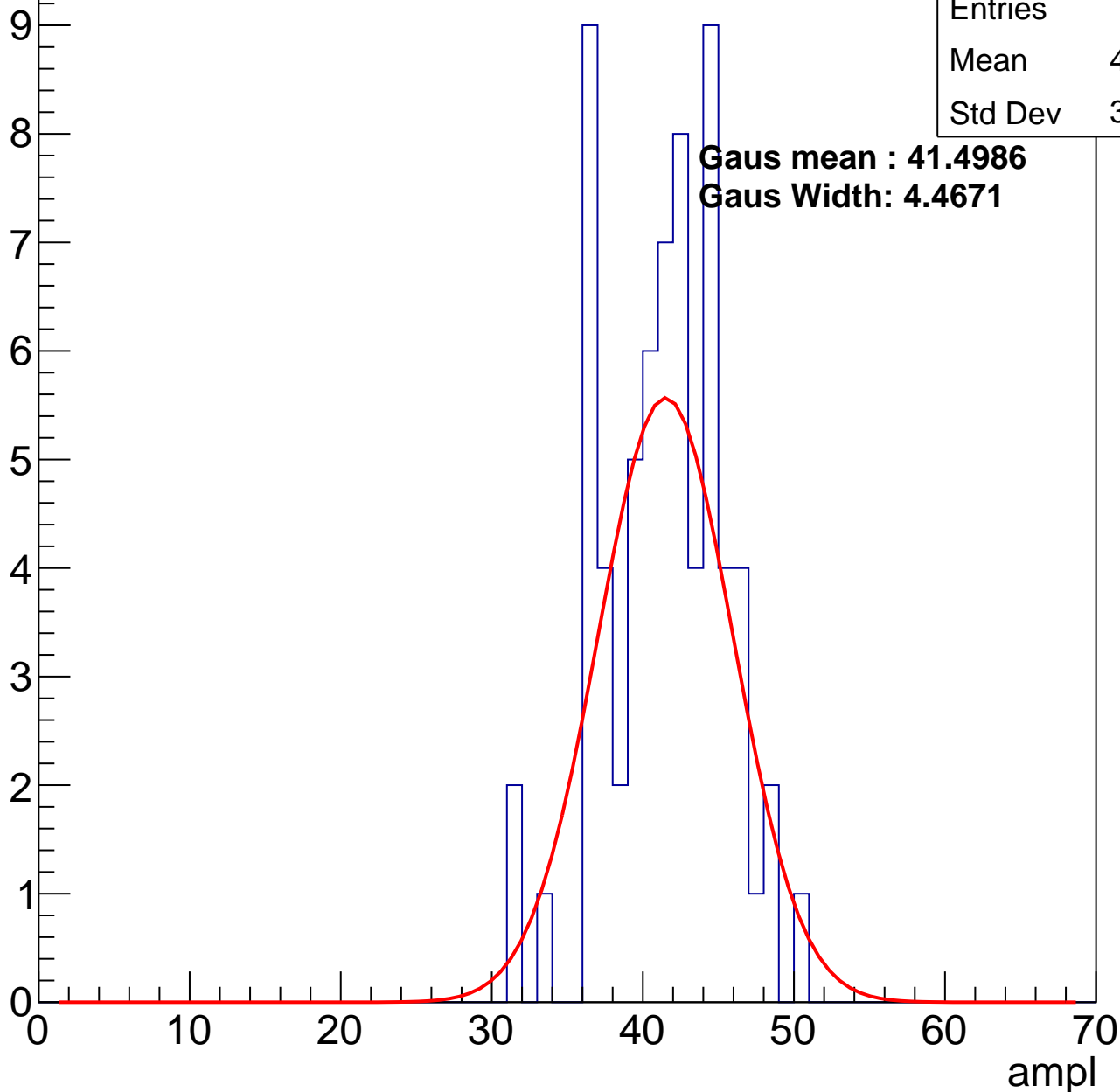
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	40.96
Std Dev	3.958

**Gaus mean : 41.4986**

**Gaus Width: 4.4671**

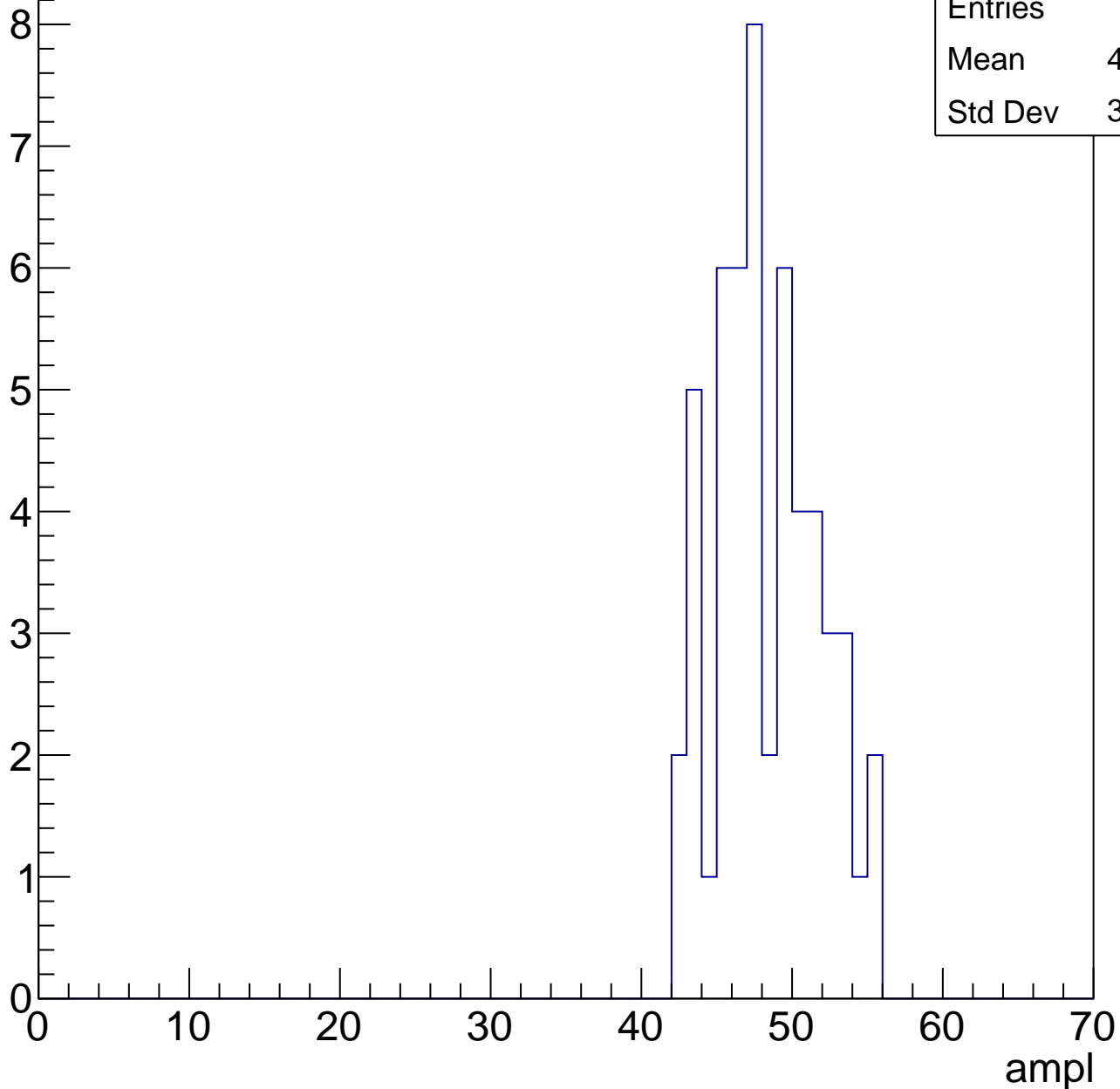


# B1L103S, U16-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	47.89
Std Dev	3.402

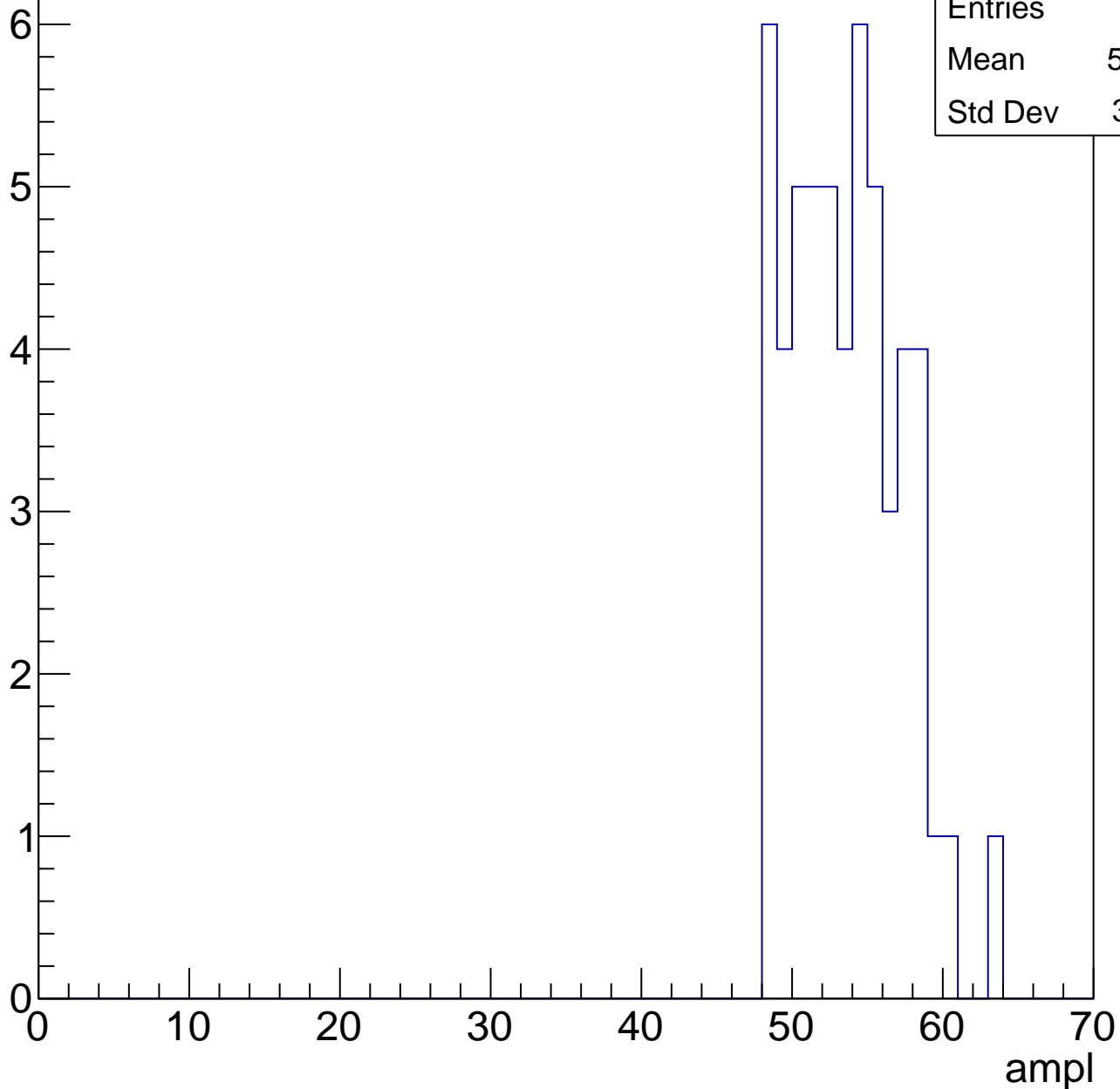


# B1L103S, U16-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	53.15
Std Dev	3.561

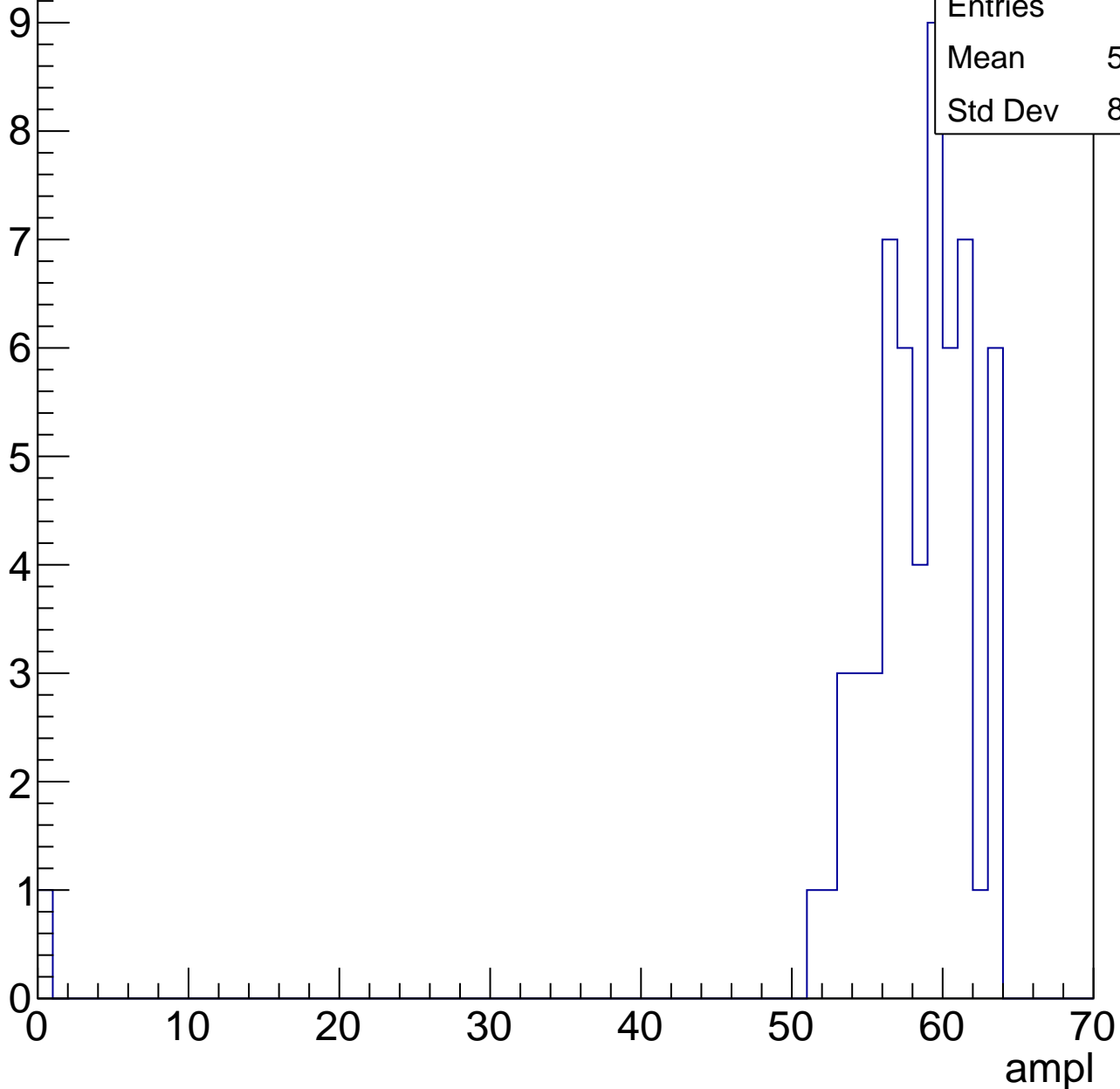


# B1L103S, U16-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	57.12
Std Dev	8.148

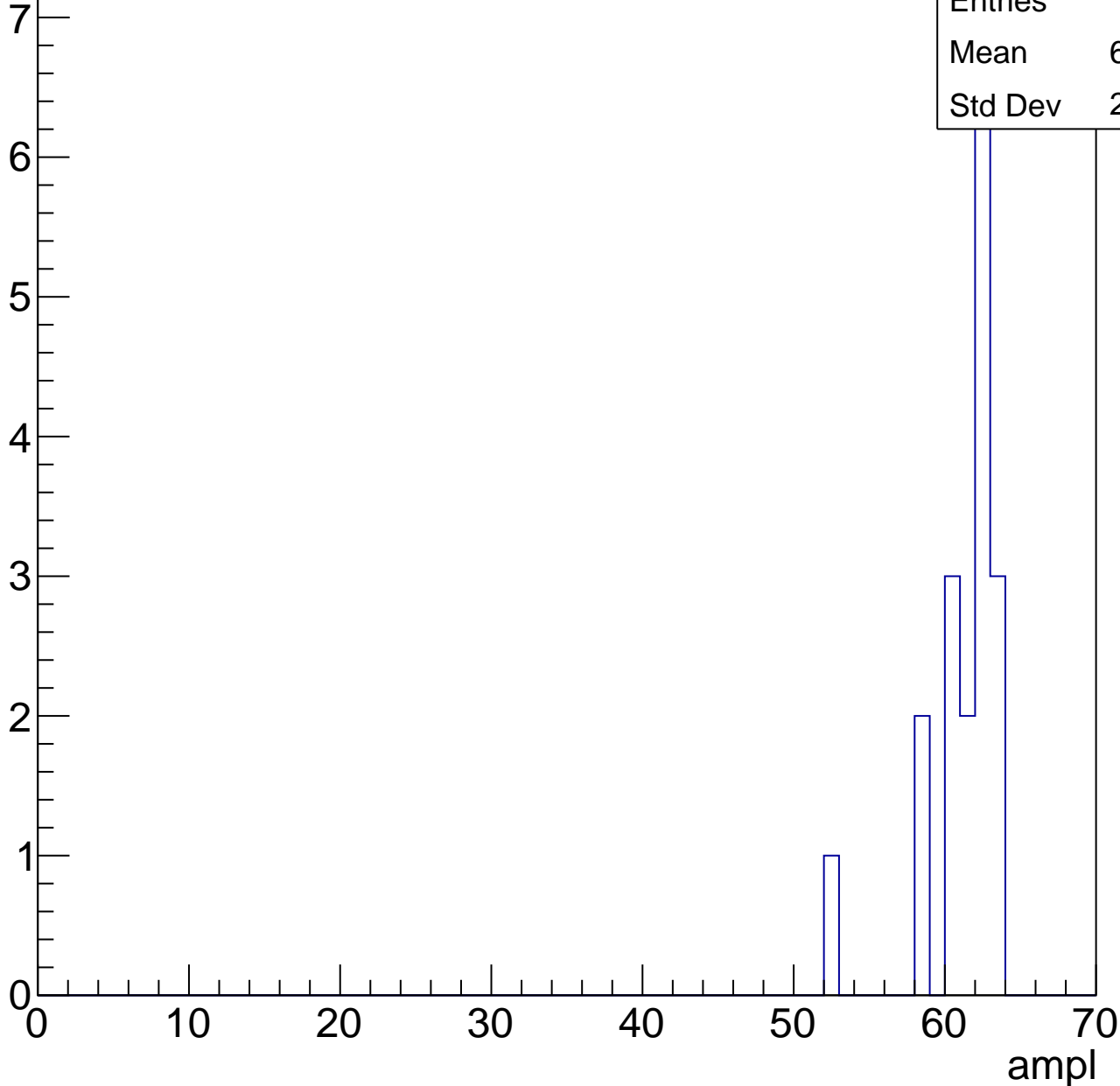


# B1L103S, U16-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	18
Mean	60.72
Std Dev	2.578





# B1L103S, U16-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	61.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70

# B1L103S, U16-ch99, adc0

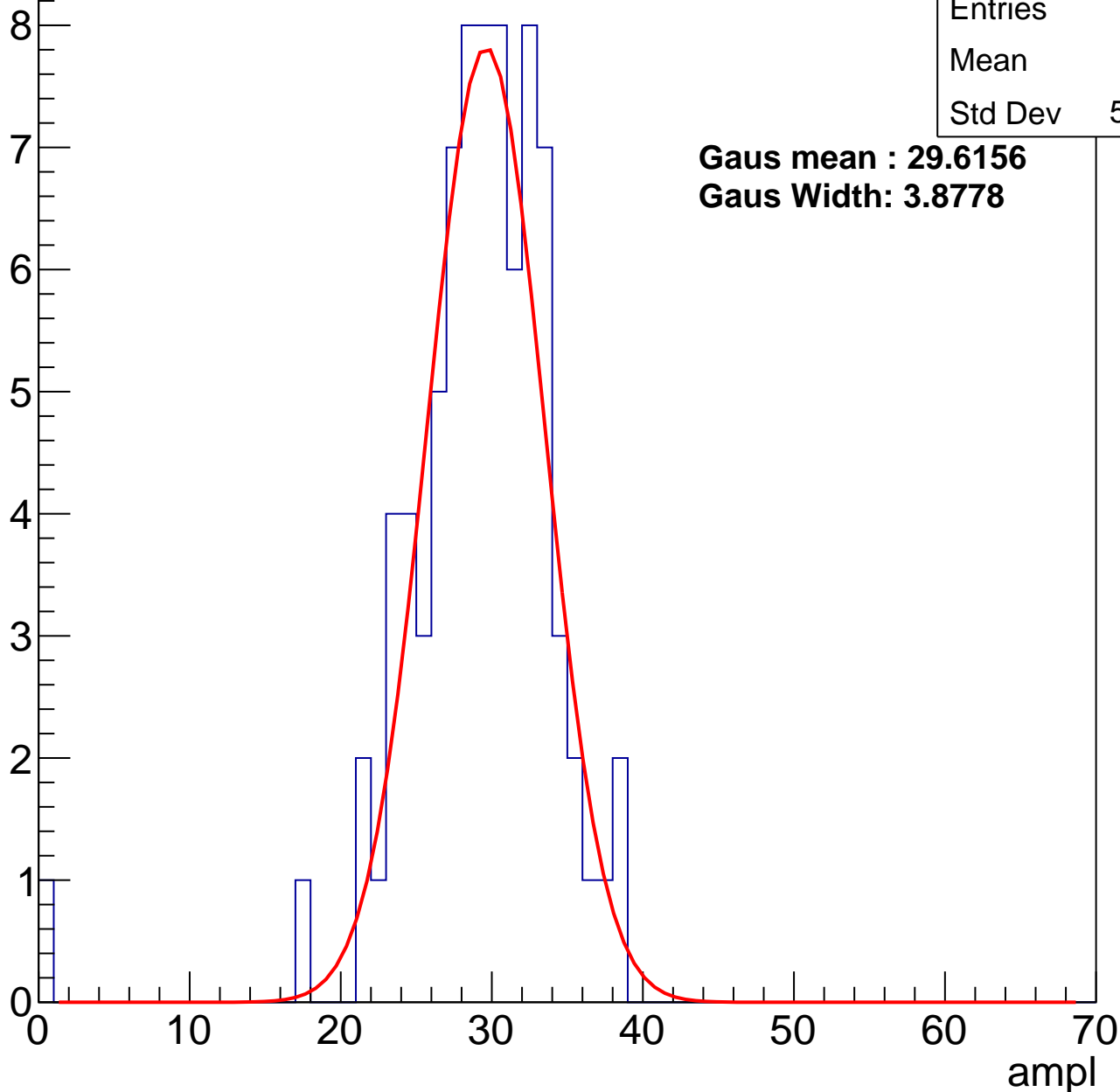
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	82
Mean	28.7
Std Dev	5.139

**Gaus mean : 29.6156**

**Gaus Width: 3.8778**



# B1L103S, U16-ch99, adc1

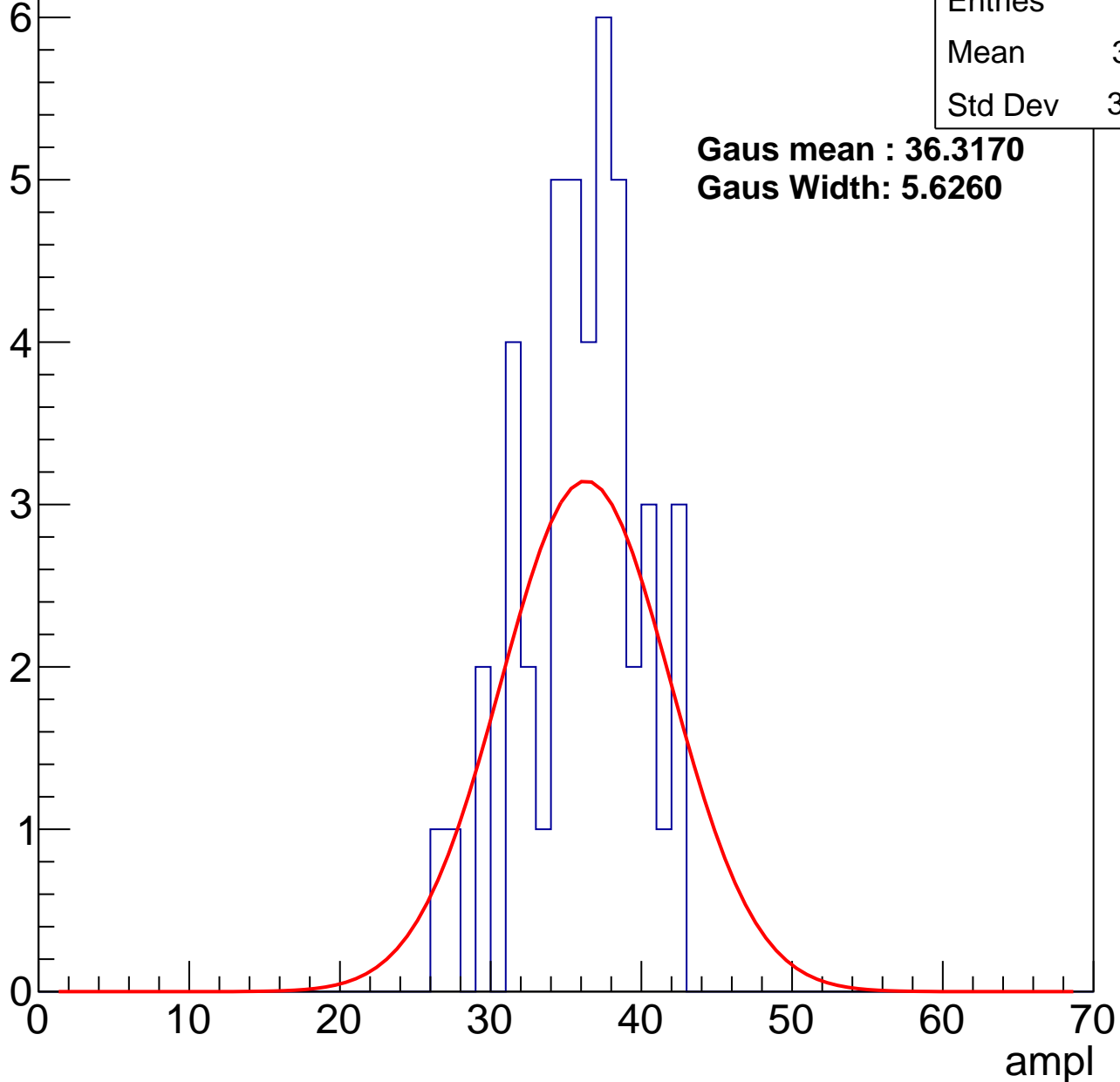
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	35.51
Std Dev	3.828

**Gaus mean : 36.3170**

**Gaus Width: 5.6260**



# B1L103S, U16-ch99, adc2

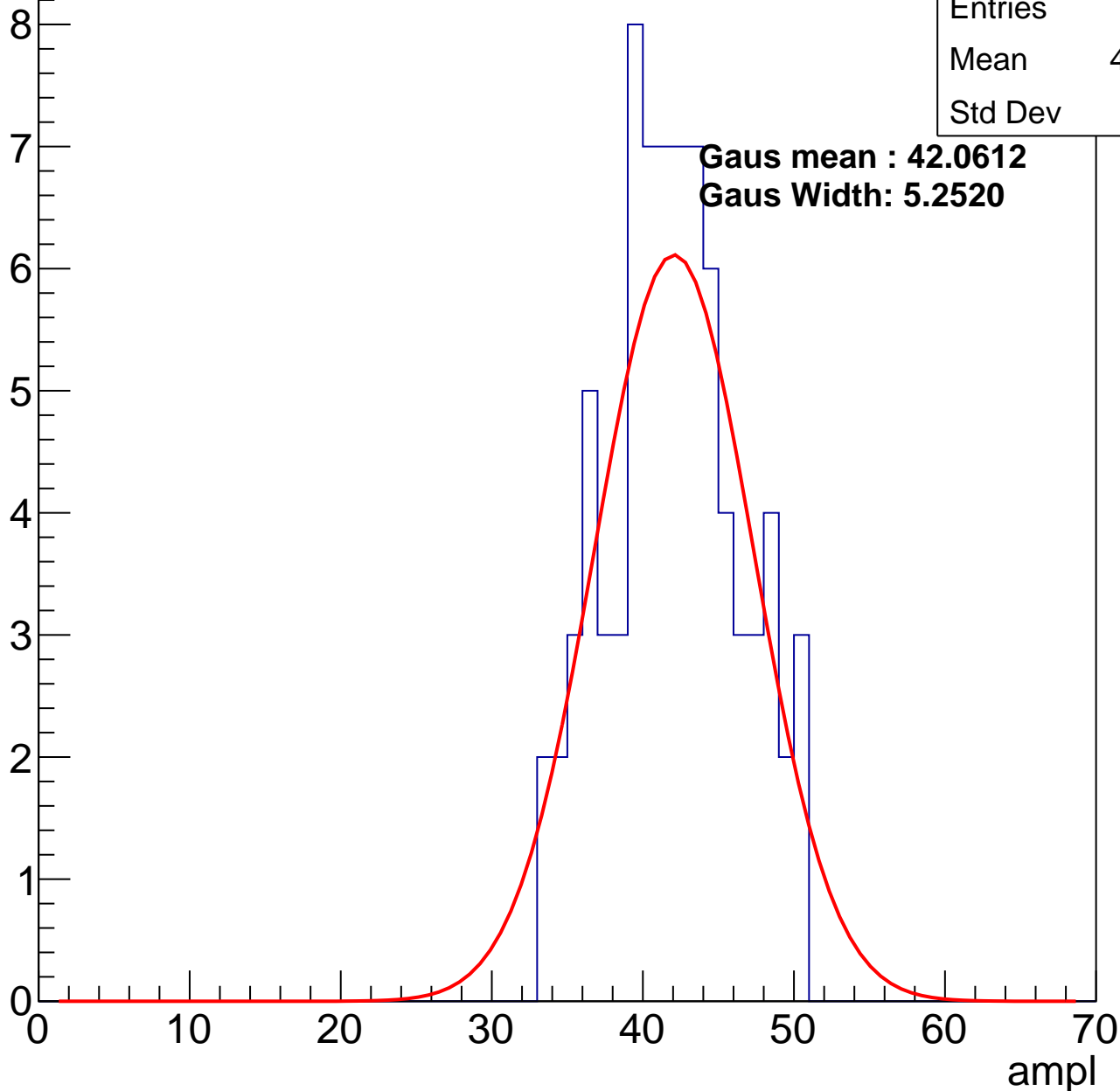
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	41.53
Std Dev	4.29

**Gaus mean : 42.0612**

**Gaus Width: 5.2520**

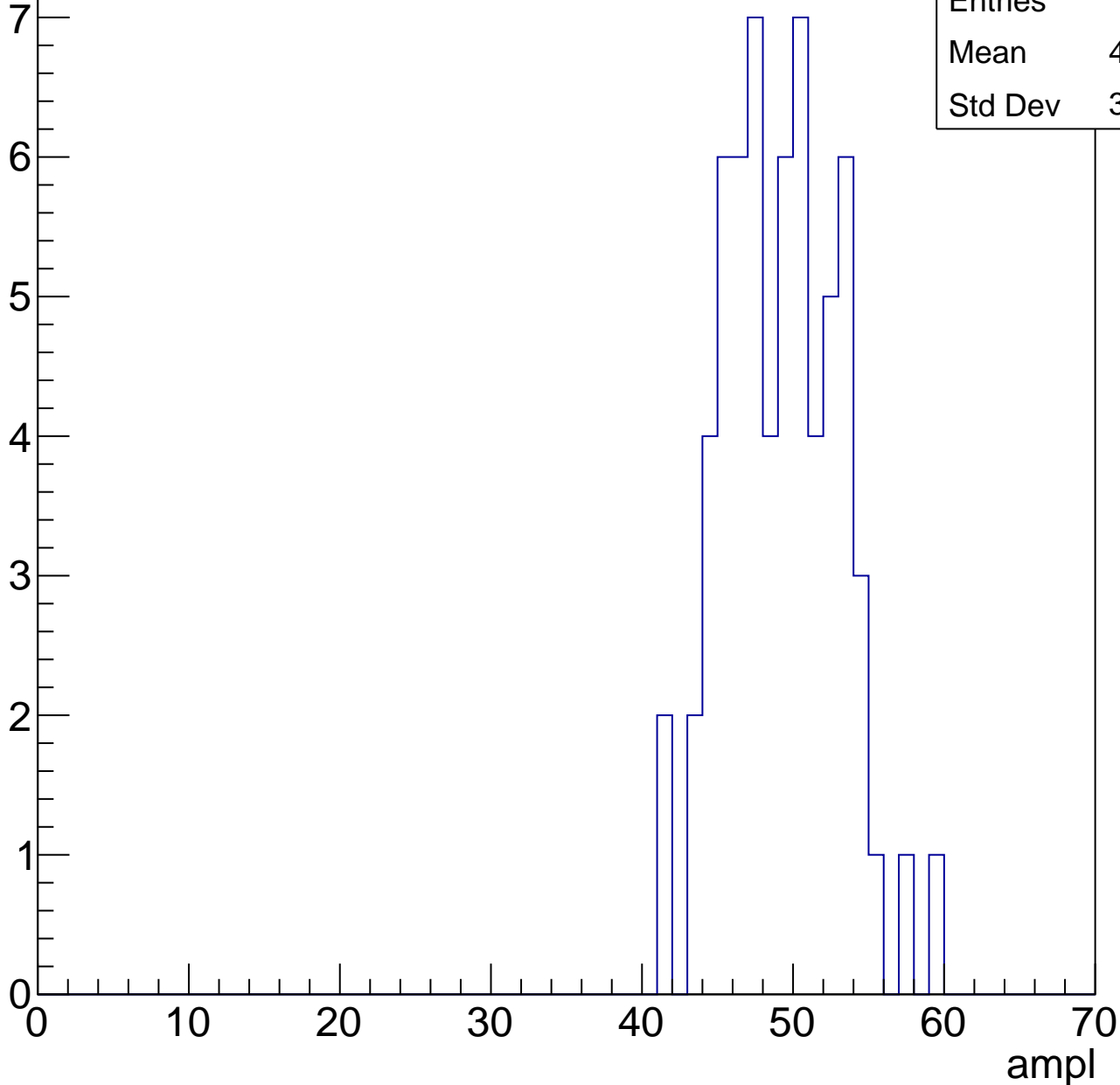


# B1L103S, U16-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	48.77
Std Dev	3.757



# B1L103S, U16-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	68
Mean	55.46
Std Dev	4.027

Entry

10

8

6

4

2

0

0

10

20

30

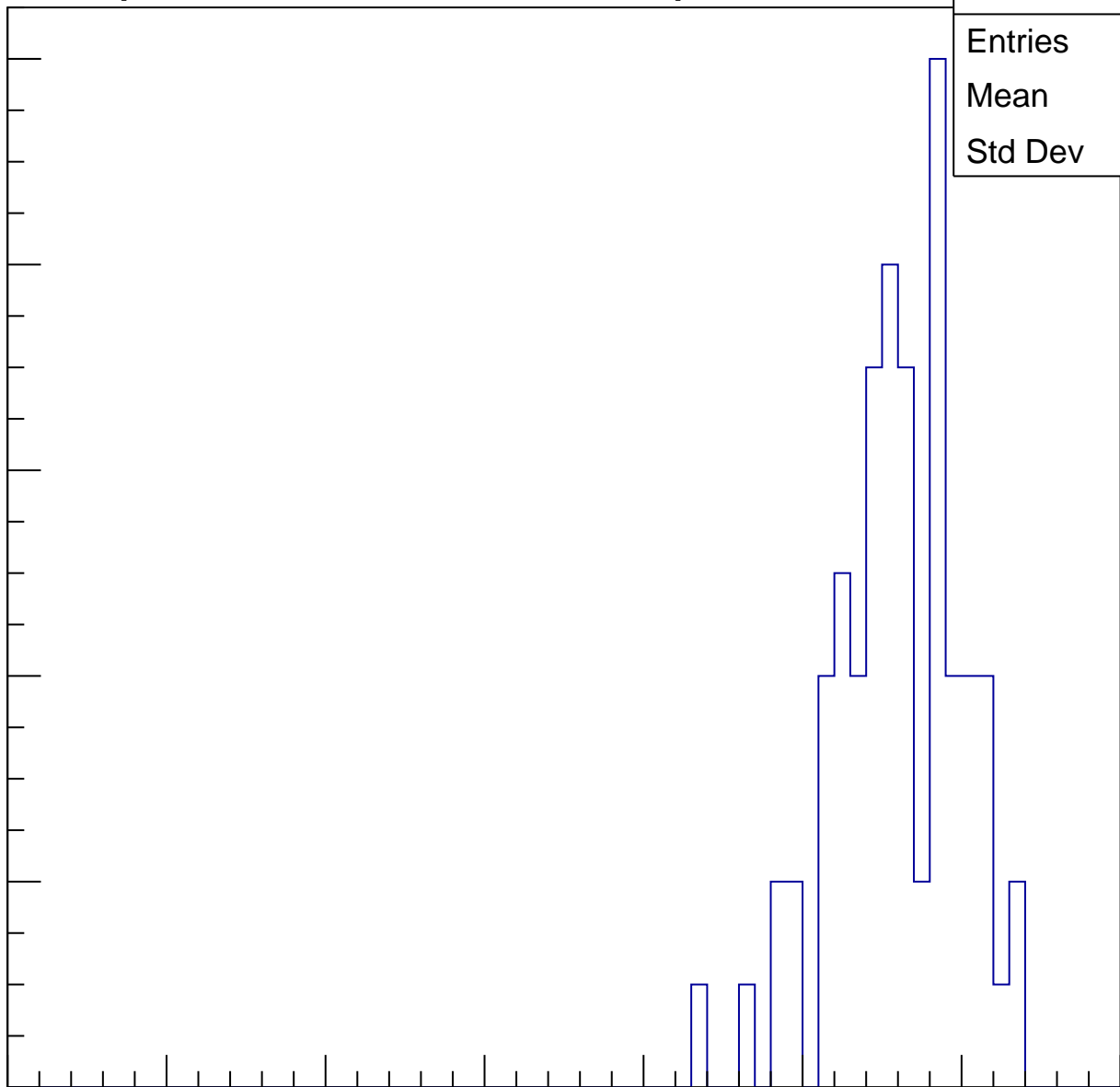
40

50

60

70

ampl



# B1L103S, U16-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

7

6

5

4

3

2

1

0

Entries 42

Mean 57.93

Std Dev 9.513

0

10

20

30

40

50

60

70

ampl

0

1

2

3

4

5

6

7

8

9

10

11

12

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14

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311

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314

315

316

317

318

319

320

321

322

323

# B1L103S, U16-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	6
Mean	62.33
Std Dev	0.7454



# B1L103S, U16-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U16-ch100, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	81
Mean	25.81
Std Dev	6.665

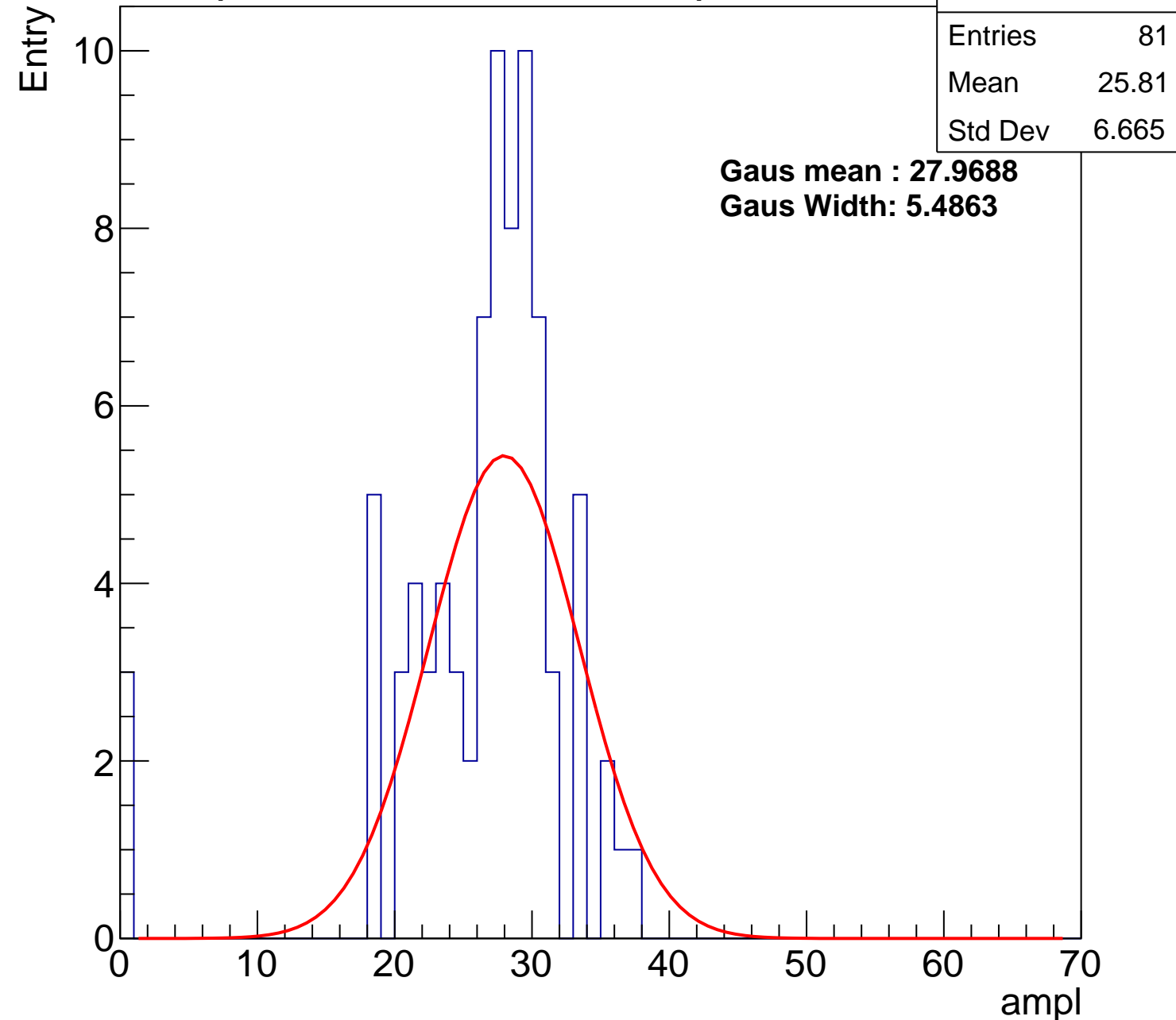
**Gaus mean : 27.9688**

**Gaus Width: 5.4863**

Entry

10  
8  
6  
4  
2  
0

ampl



# B1L103S, U16-ch100, adc1

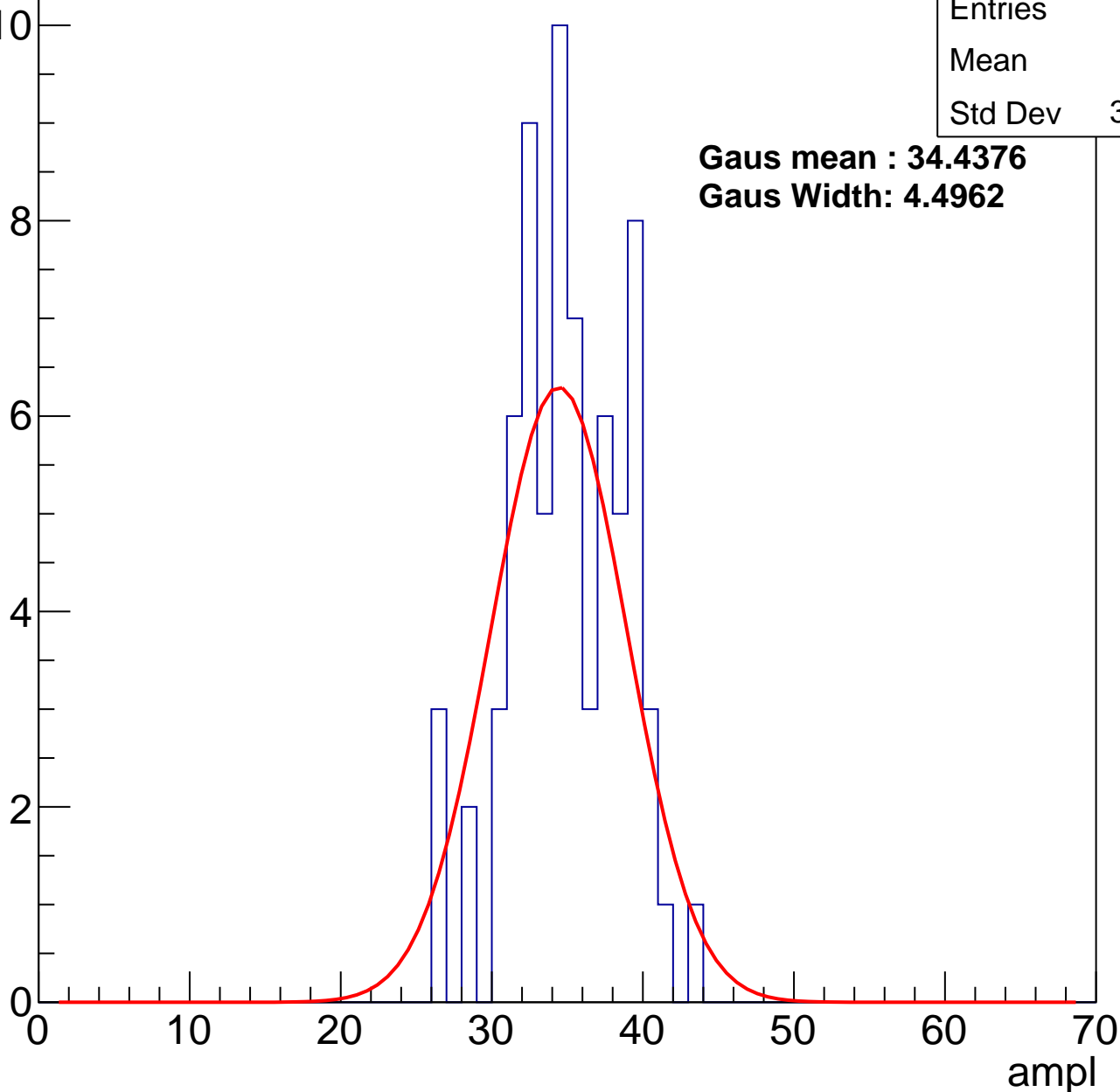
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	34.5
Std Dev	3.689

**Gaus mean : 34.4376**

**Gaus Width: 4.4962**



# B1L103S, U16-ch100, adc2

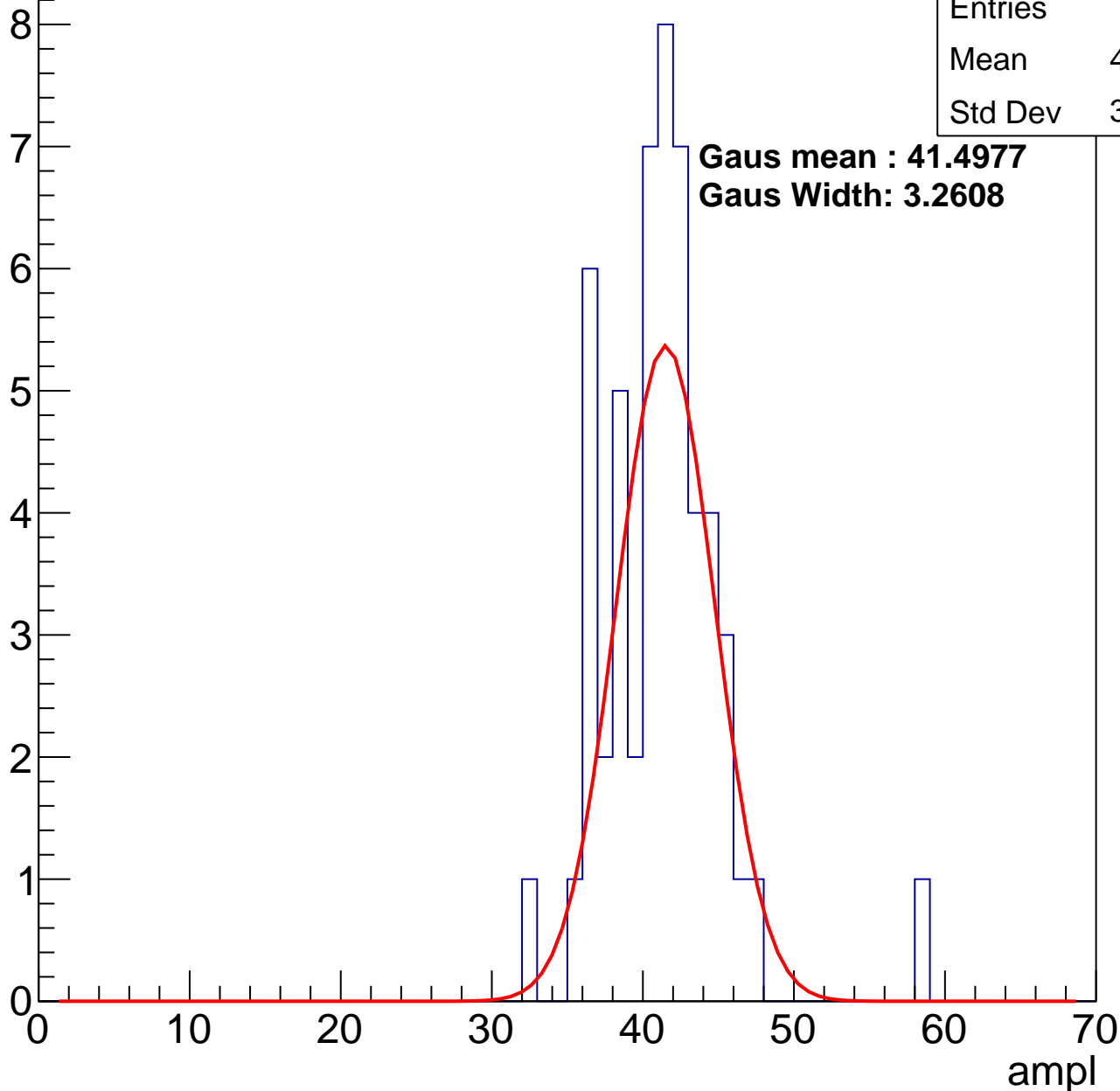
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	40.77
Std Dev	3.917

**Gaus mean : 41.4977**

**Gaus Width: 3.2608**

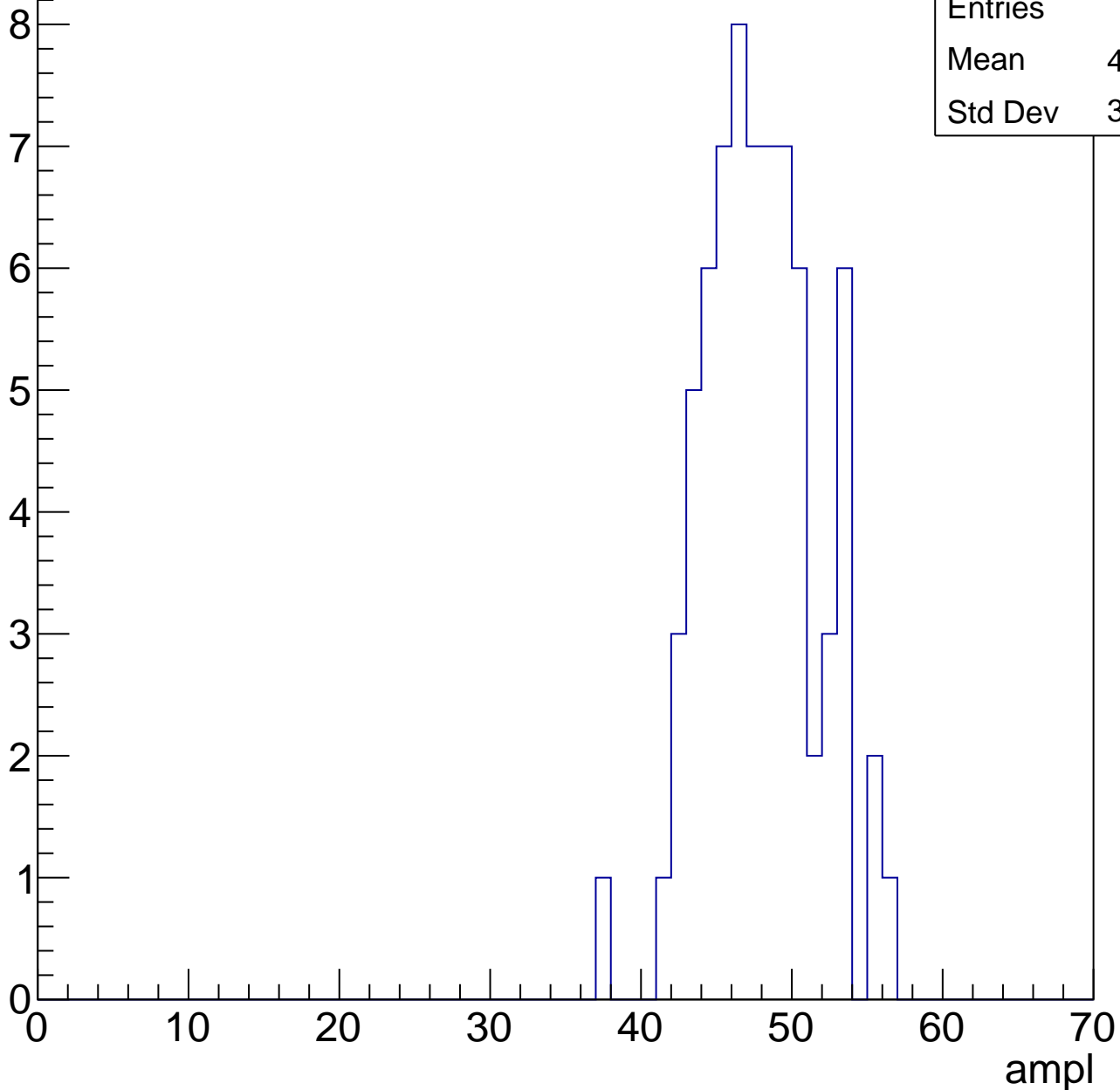


# B1L103S, U16-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	47.44
Std Dev	3.704

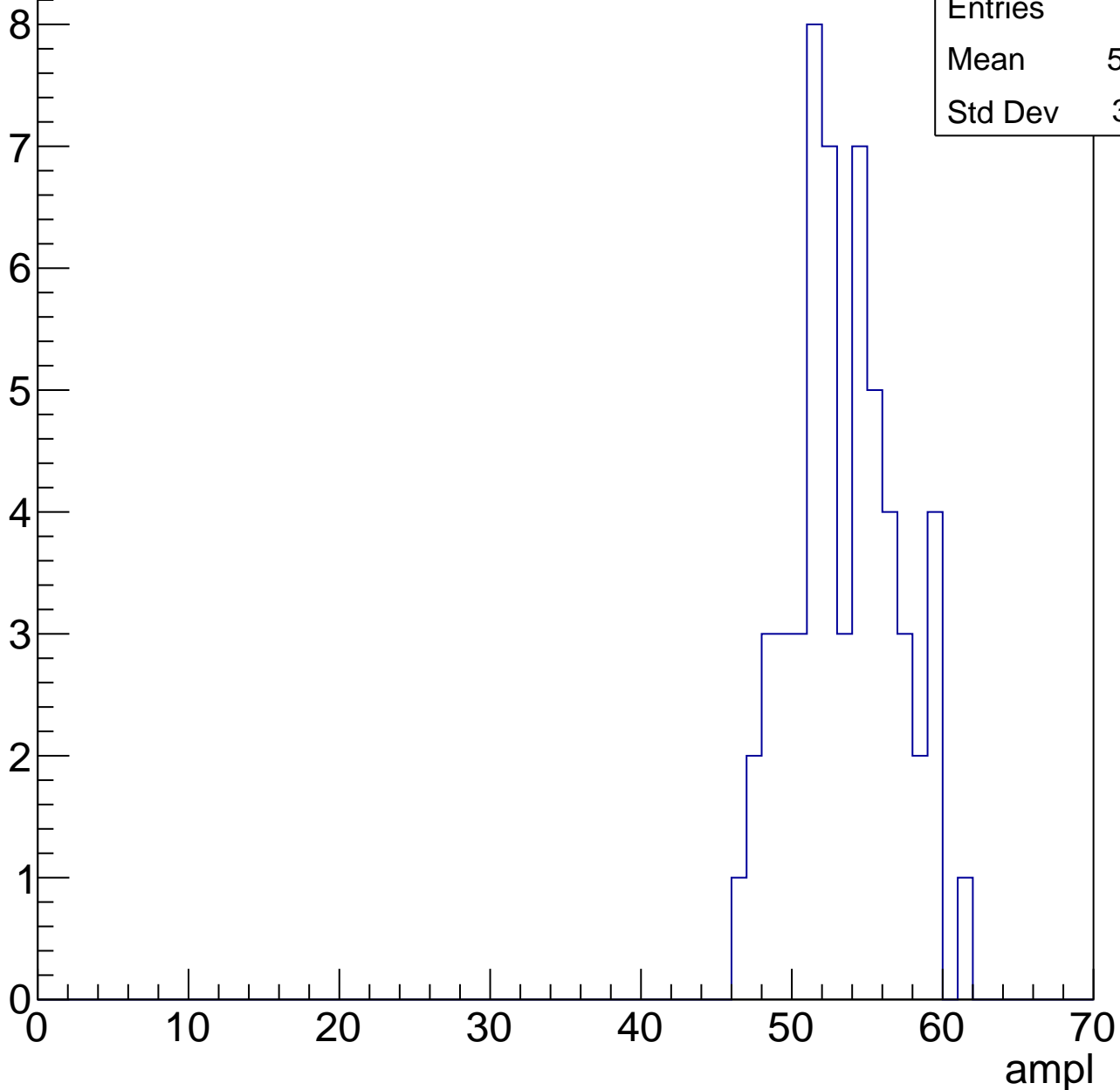


# B1L103S, U16-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

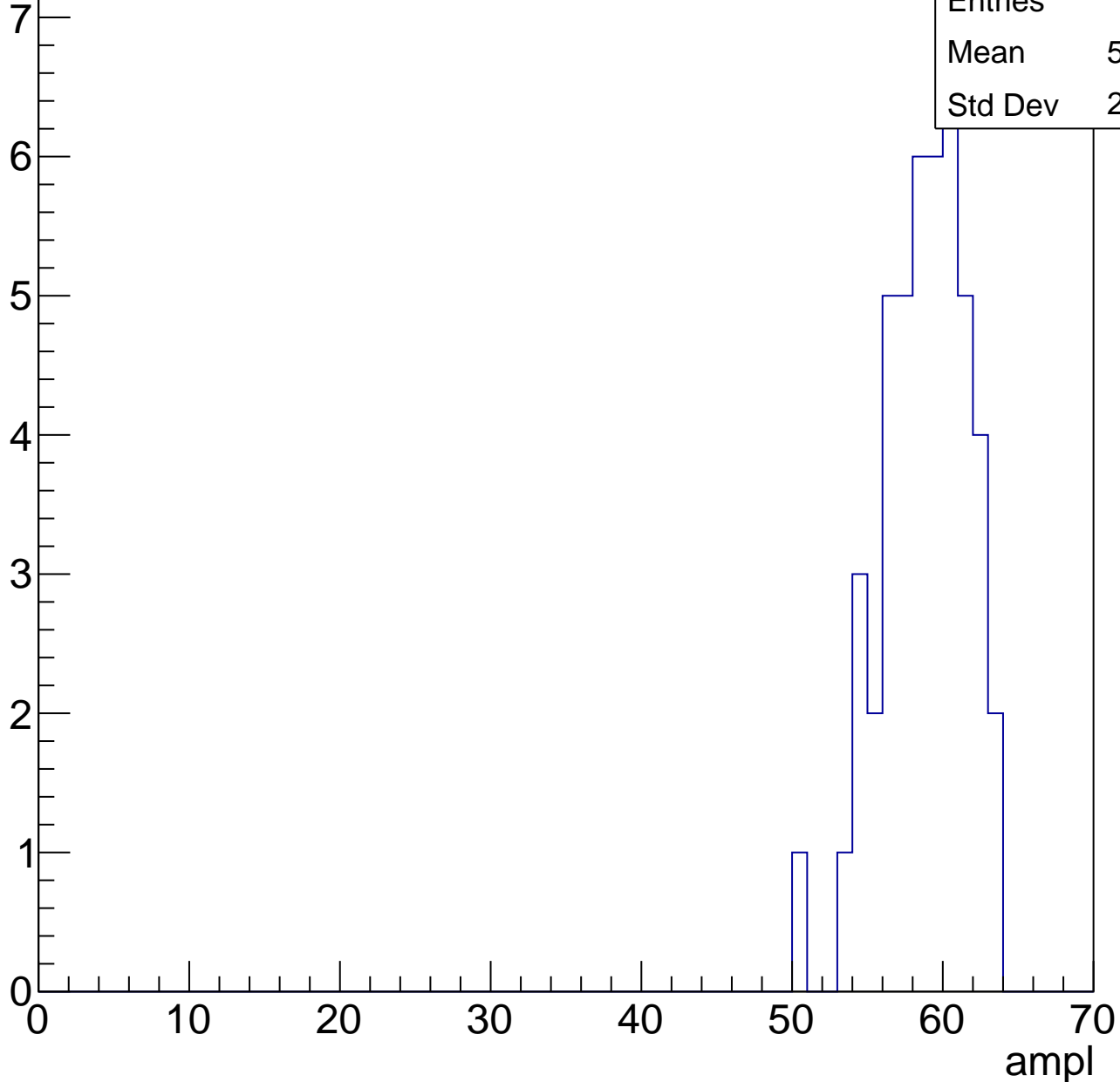
Entries	56
Mean	53.09
Std Dev	3.481



# B1L103S, U16-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

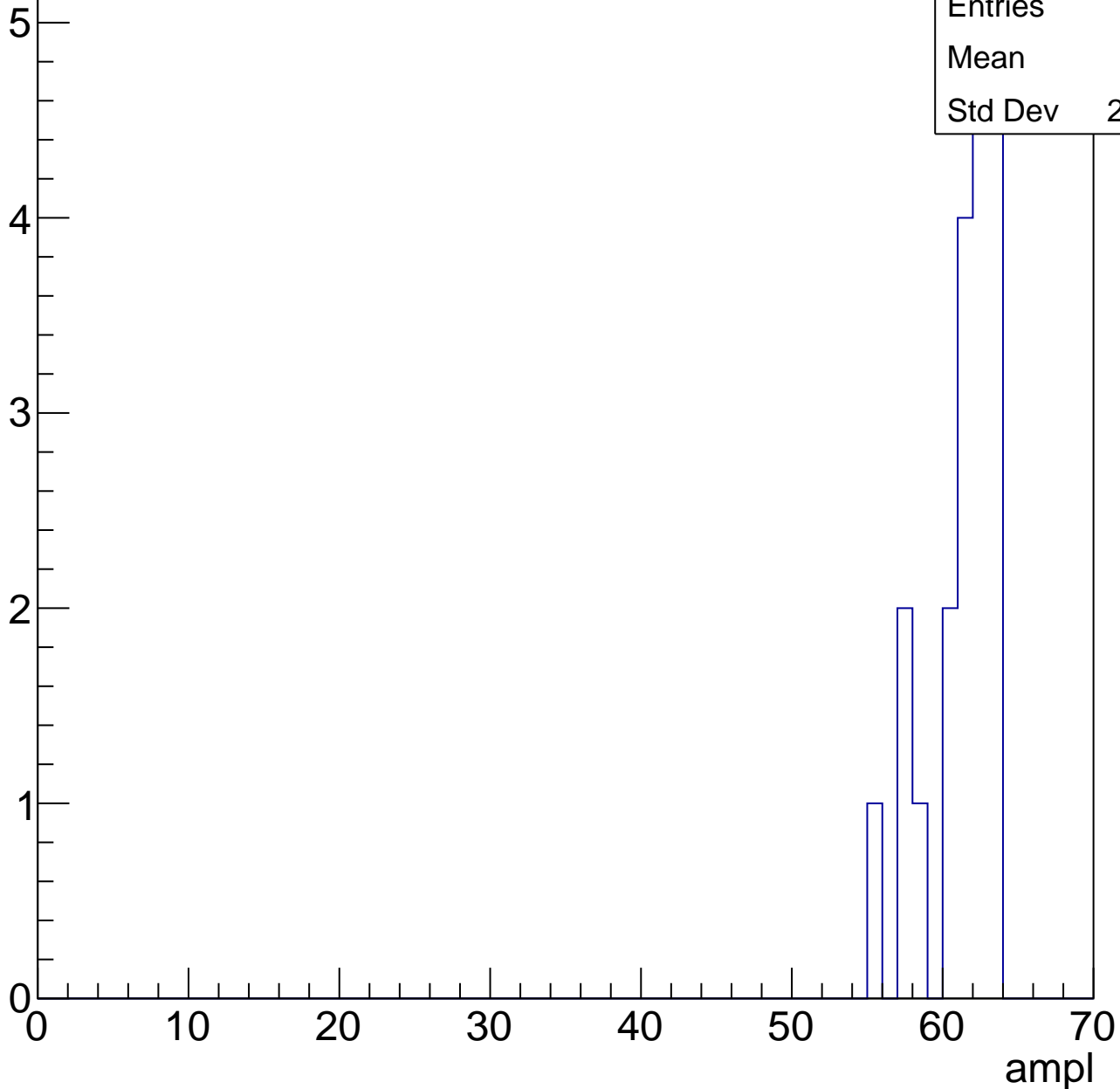


# B1L103S, U16-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	20
Mean	60.8
Std Dev	2.272

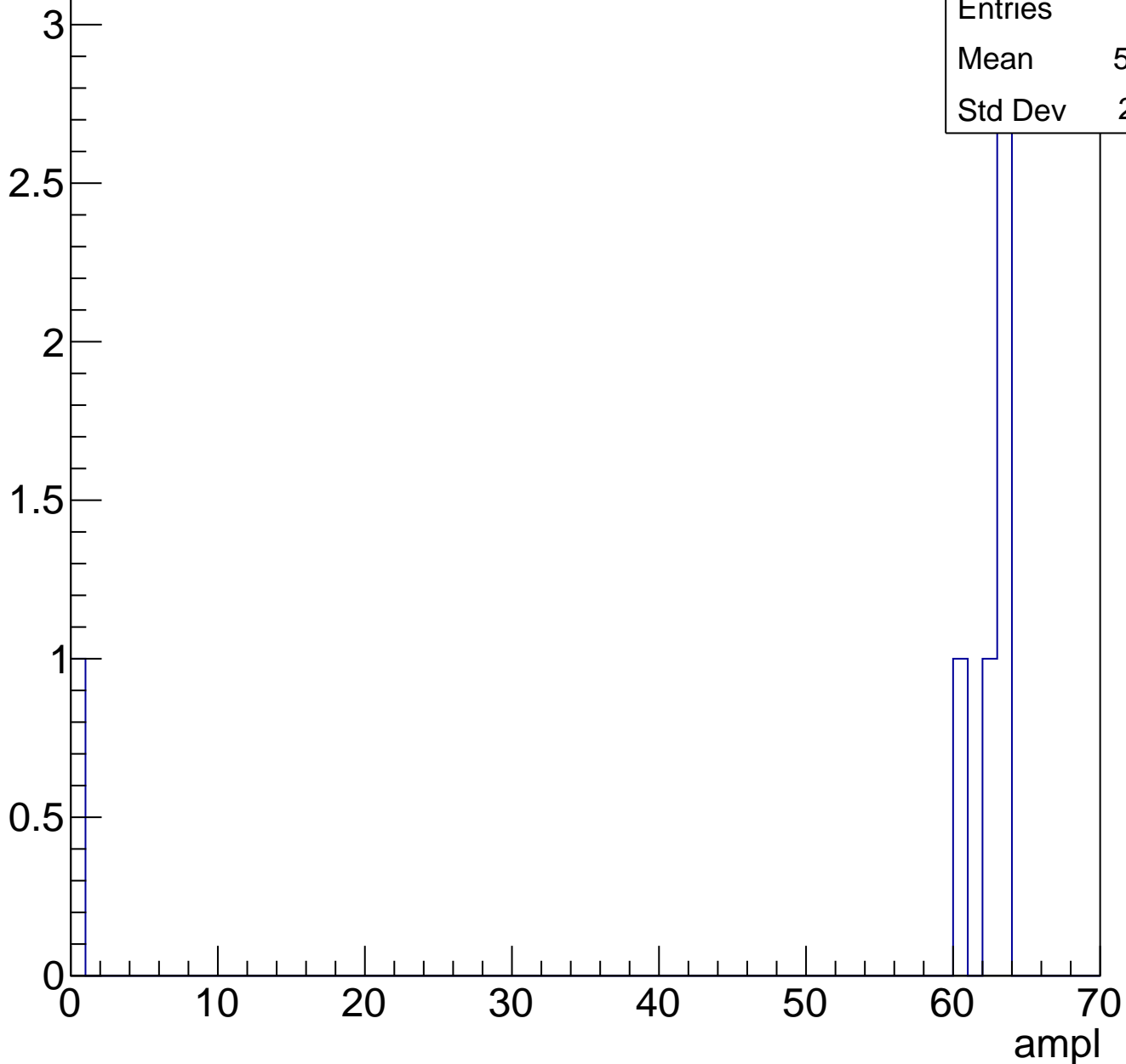




# B1L103S, U16-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch101, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	66
Mean	28.02
Std Dev	7.145

**Gaus mean : 30.5111**

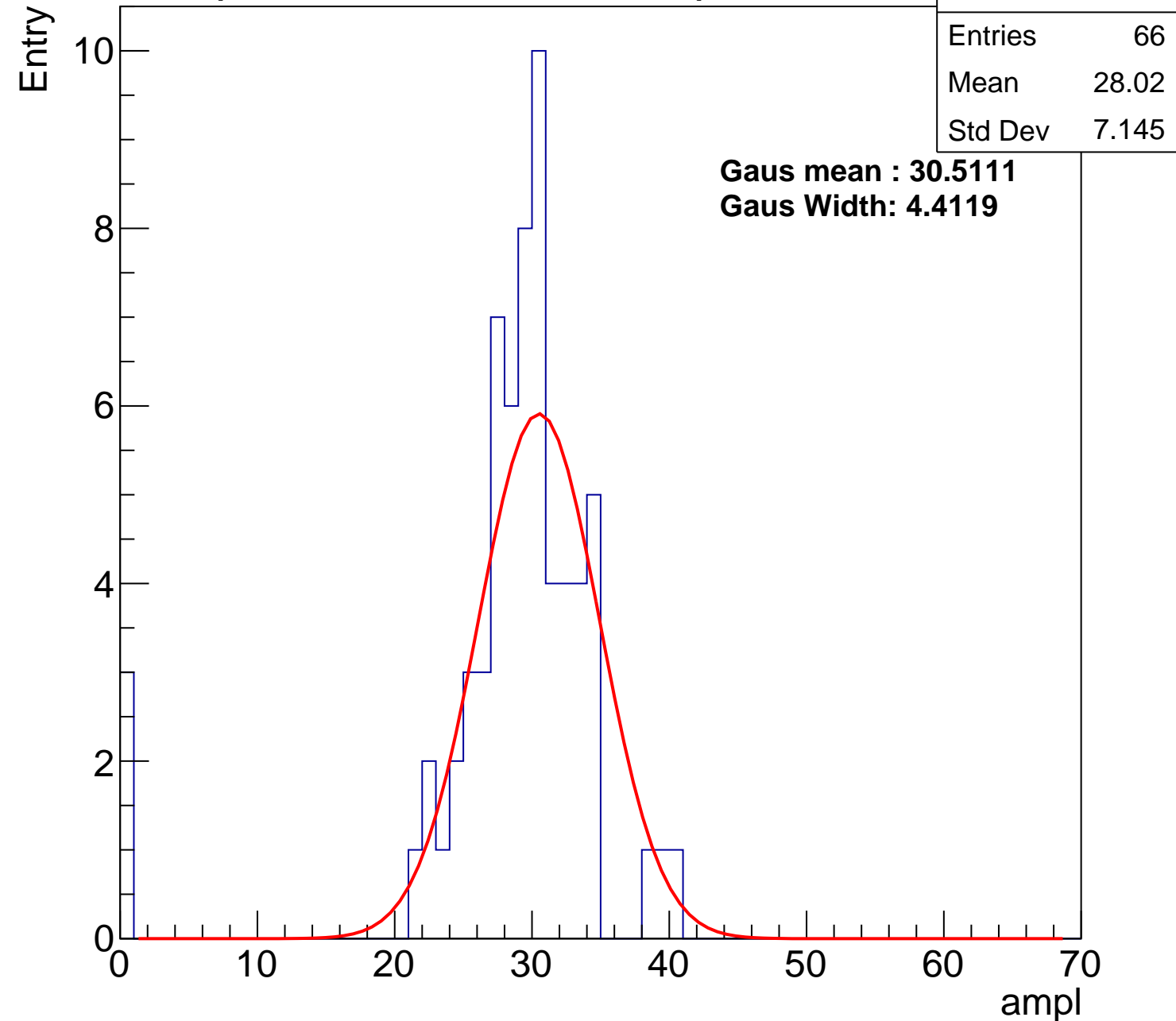
**Gaus Width: 4.4119**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U16-ch101, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	77
Mean	36.55
Std Dev	3.309

**Gaus mean : 36.3197**

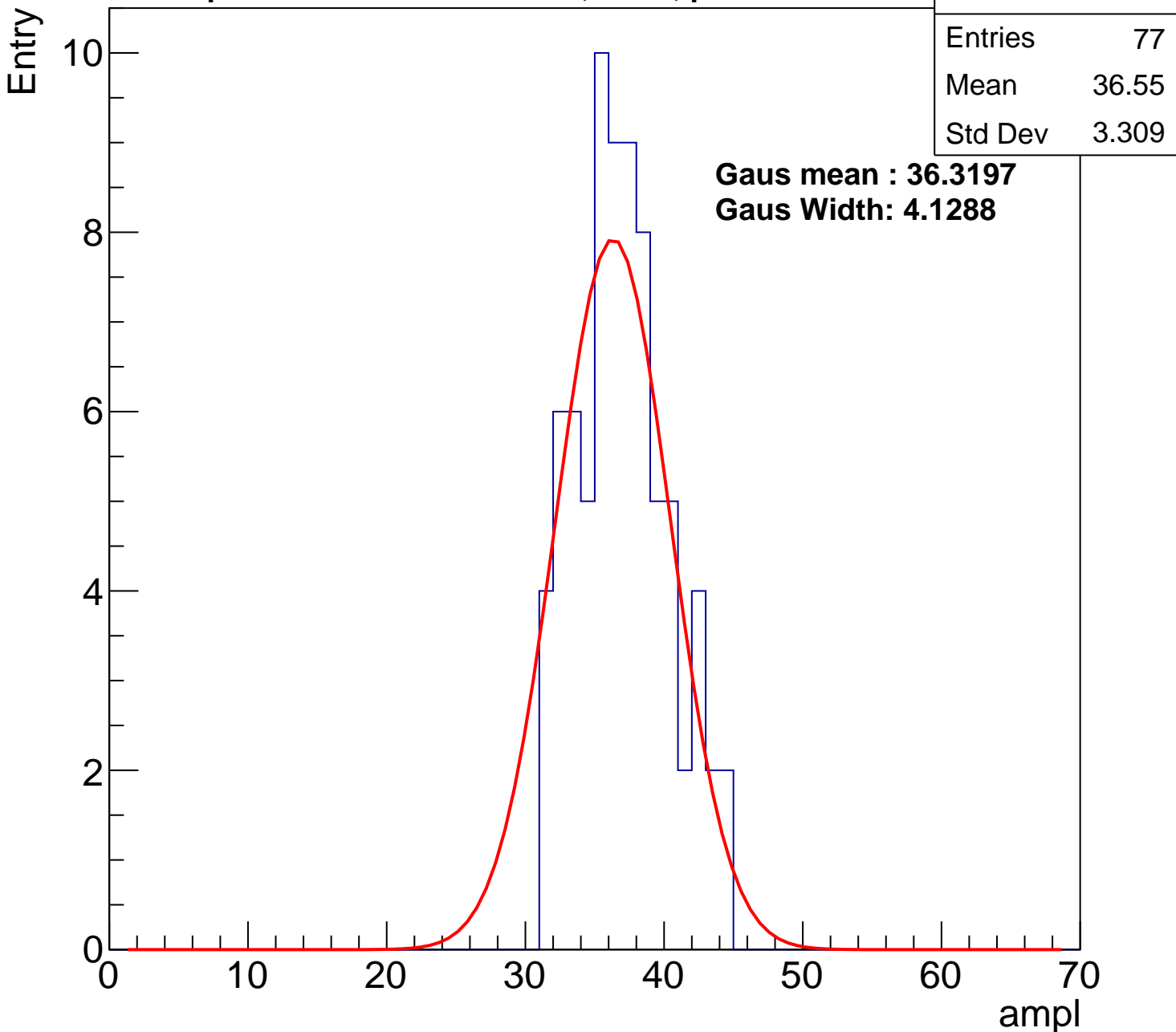
**Gaus Width: 4.1288**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U16-ch101, adc2

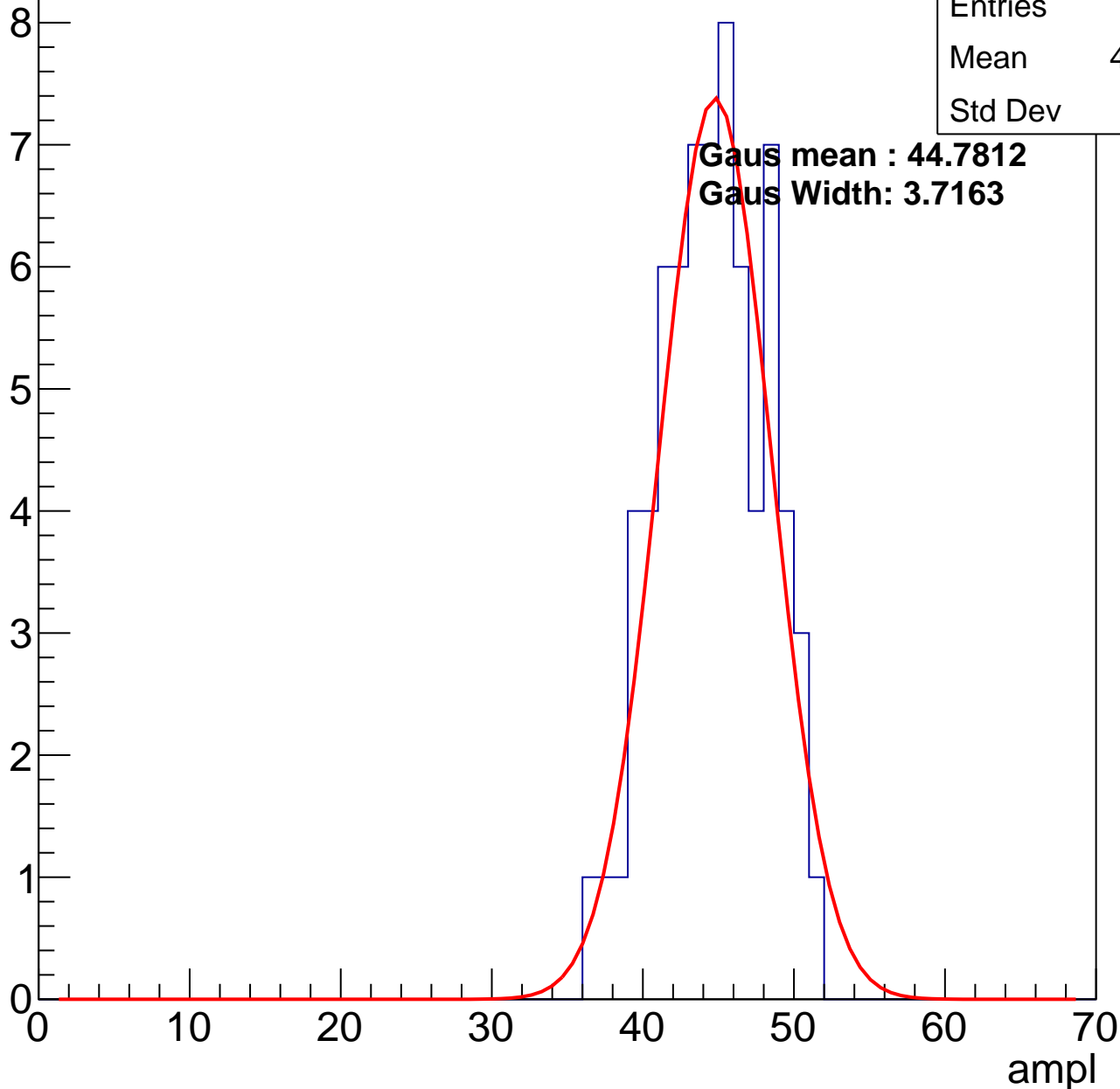
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	44.16
Std Dev	3.45

**Gaus mean : 44.7812**

**Gaus Width: 3.7163**

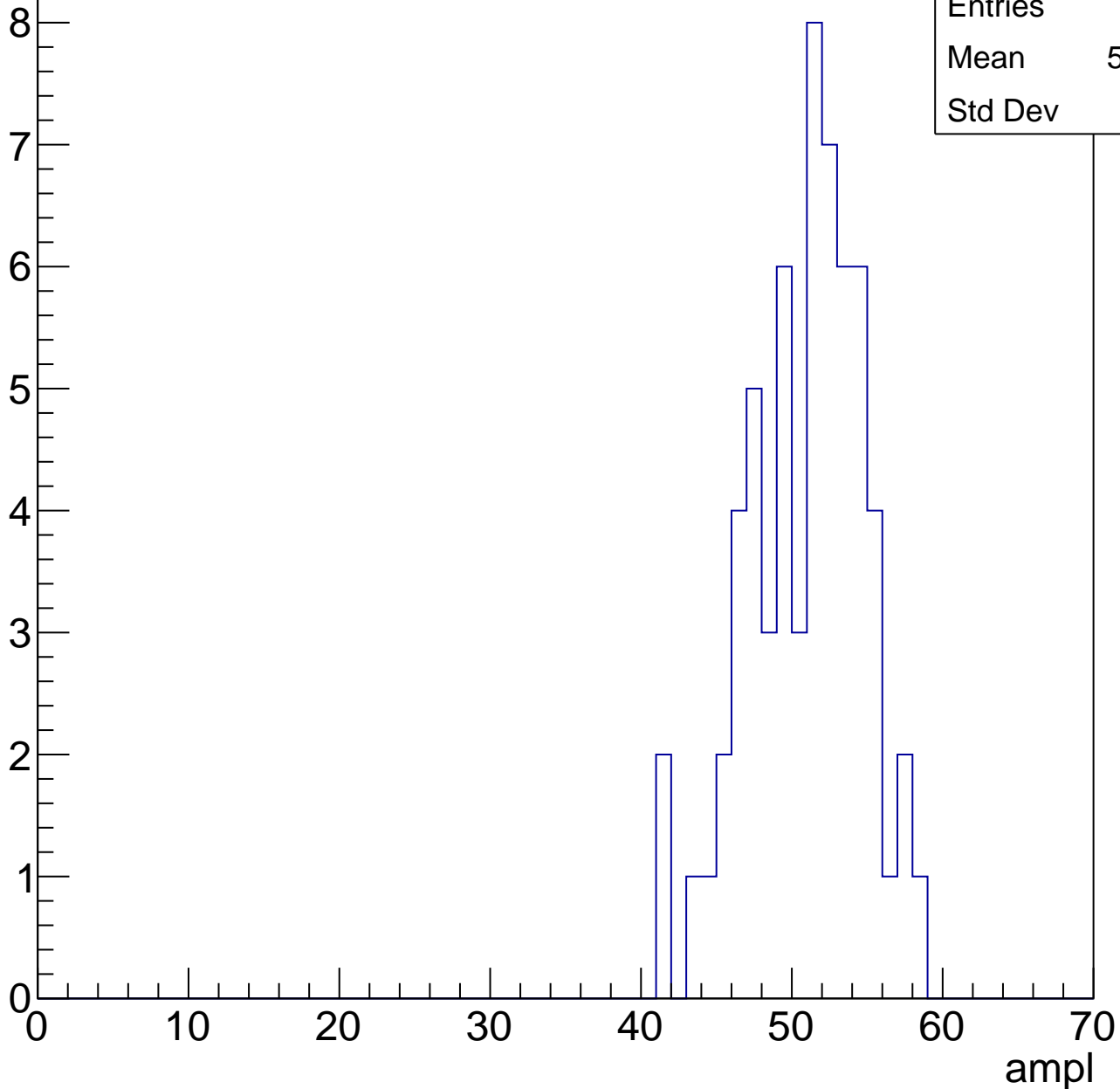


# B1L103S, U16-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	50.45
Std Dev	3.8

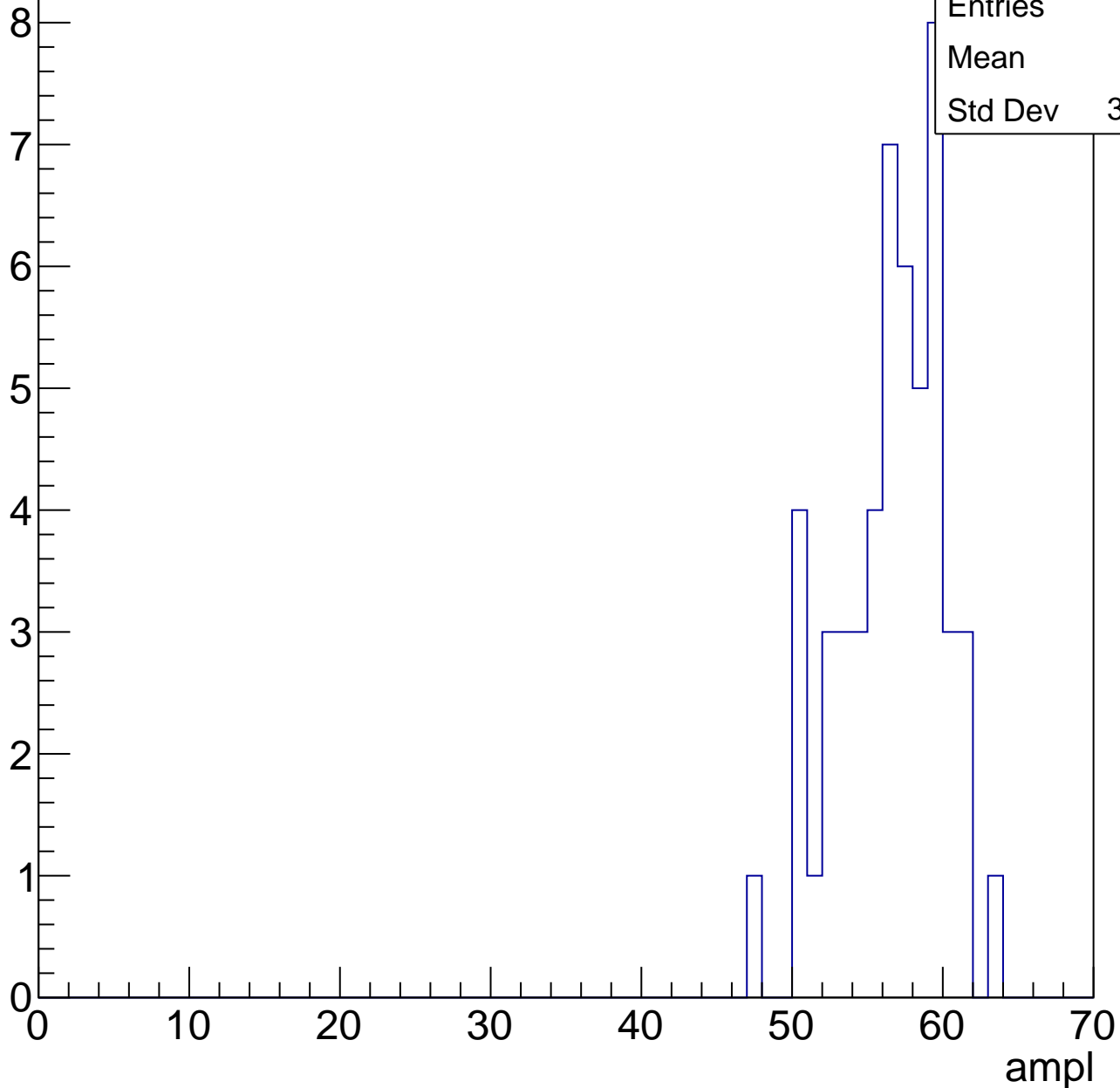


# B1L103S, U16-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	56.1
Std Dev	3.426

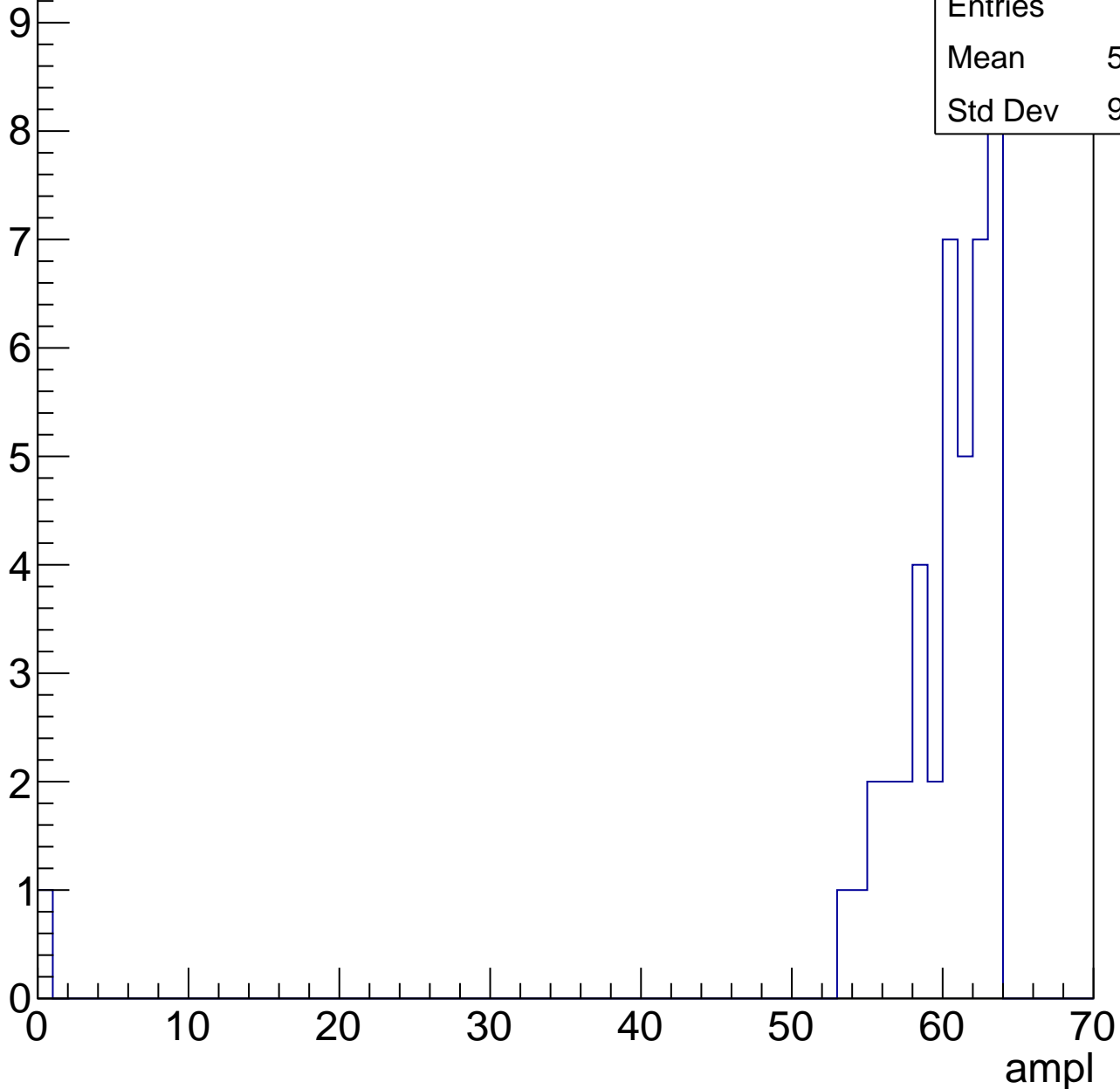


# B1L103S, U16-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

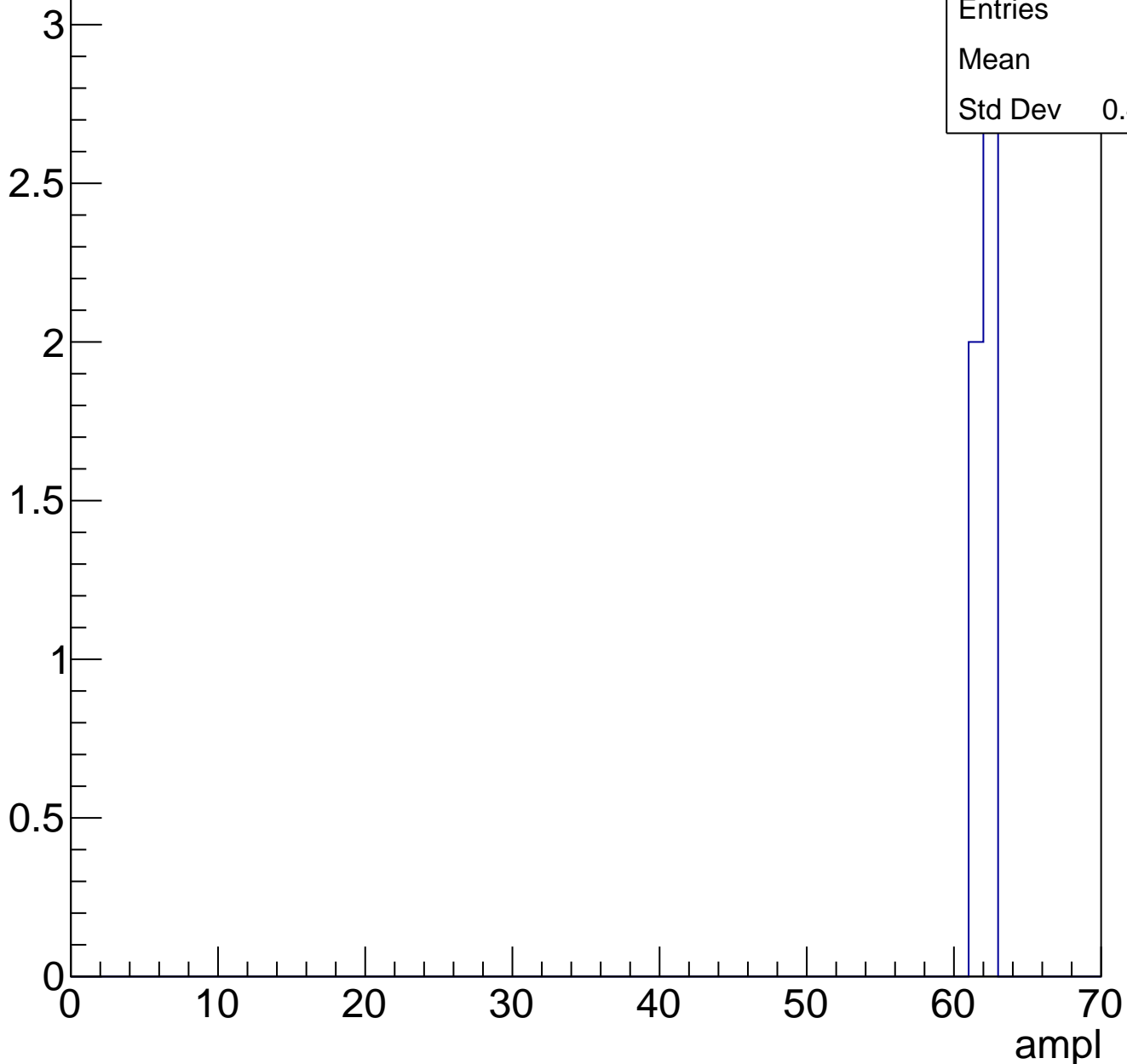
Entries	43
Mean	58.58
Std Dev	9.438



# B1L103S, U16-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U16-ch102, adc0

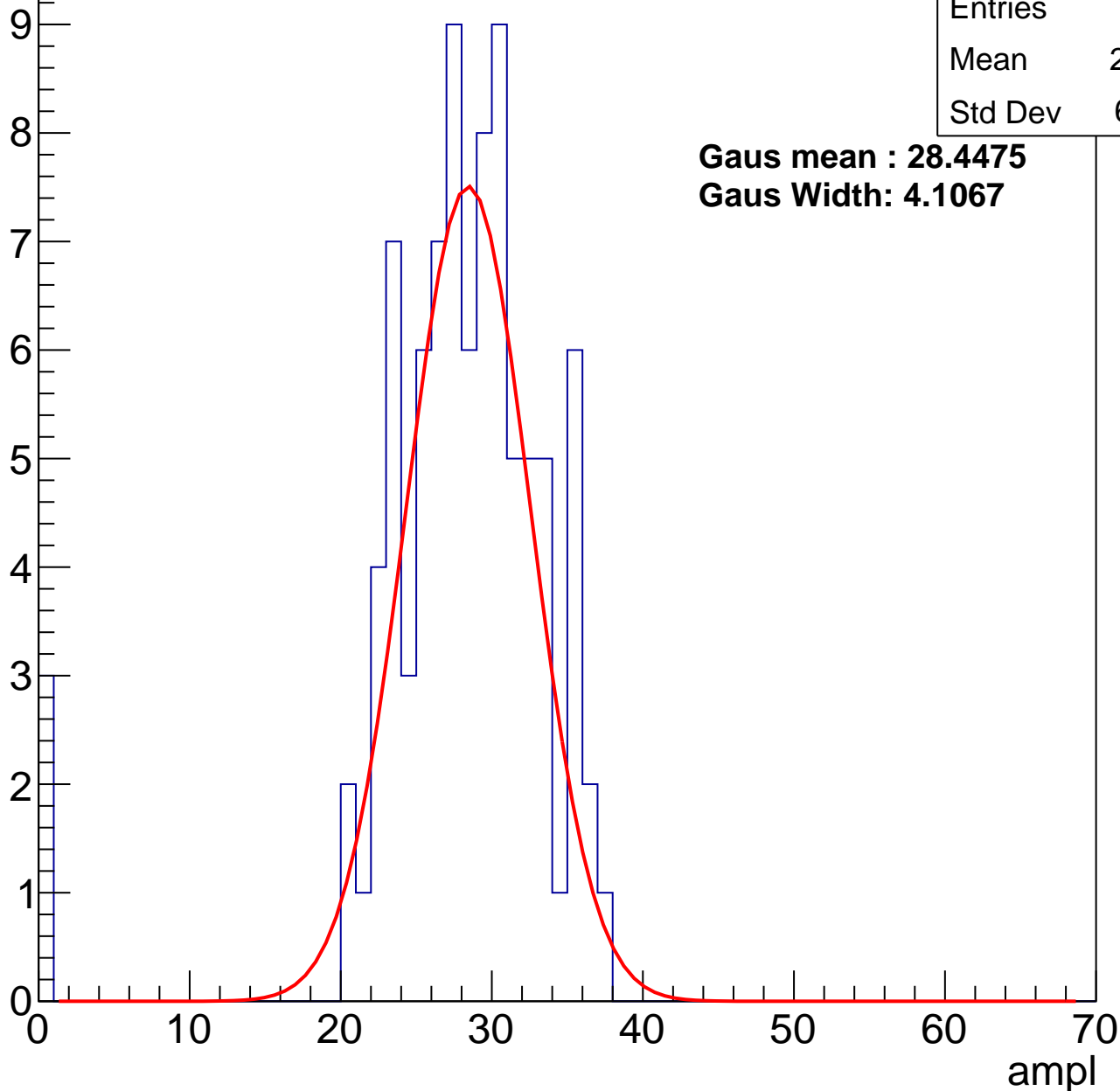
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	90
Mean	27.33
Std Dev	6.481

**Gaus mean : 28.4475**

**Gaus Width: 4.1067**



# B1L103S, U16-ch102, adc1

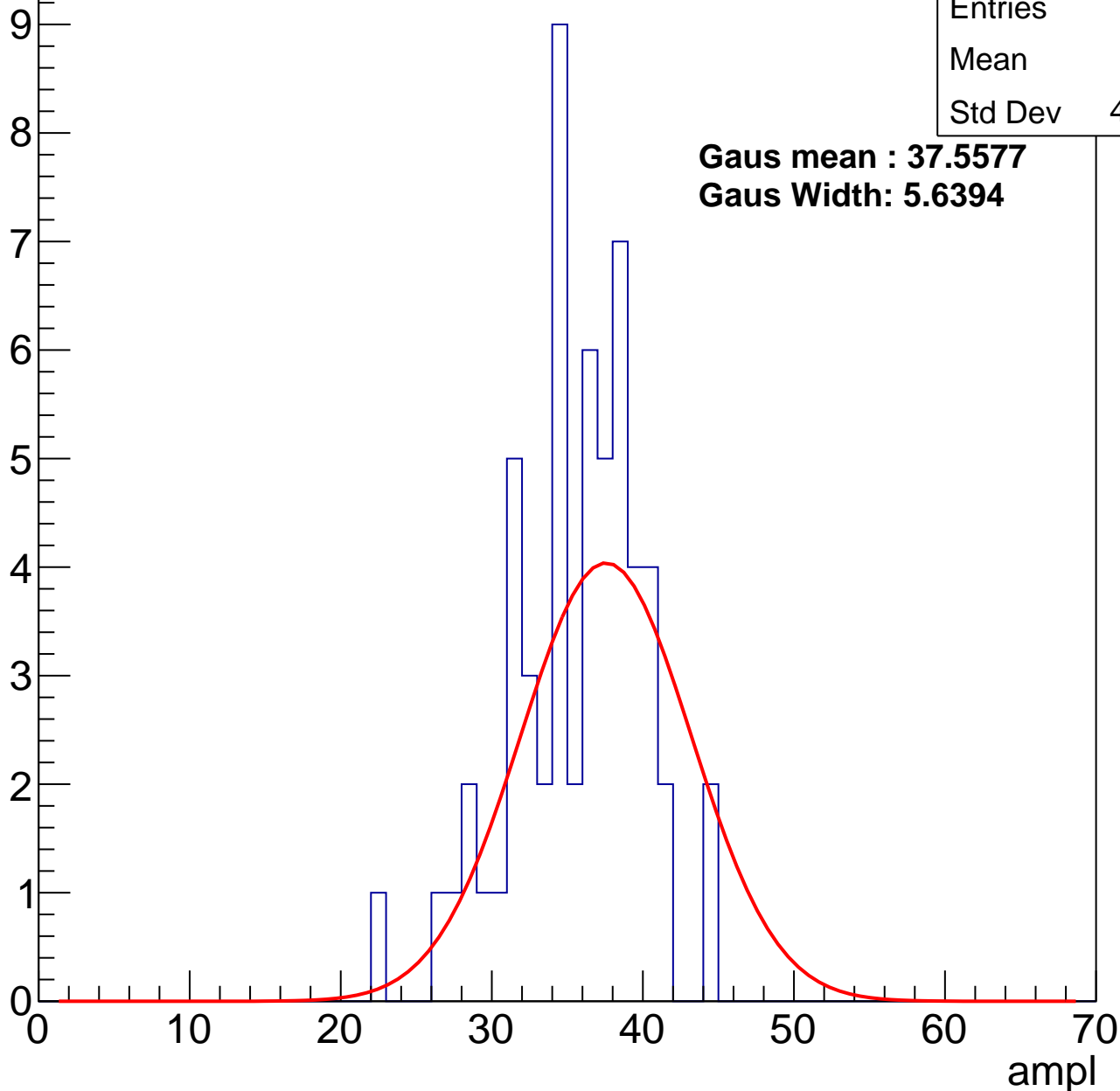
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	35.1
Std Dev	4.322

**Gaus mean : 37.5577**

**Gaus Width: 5.6394**



# B1L103S, U16-ch102, adc2

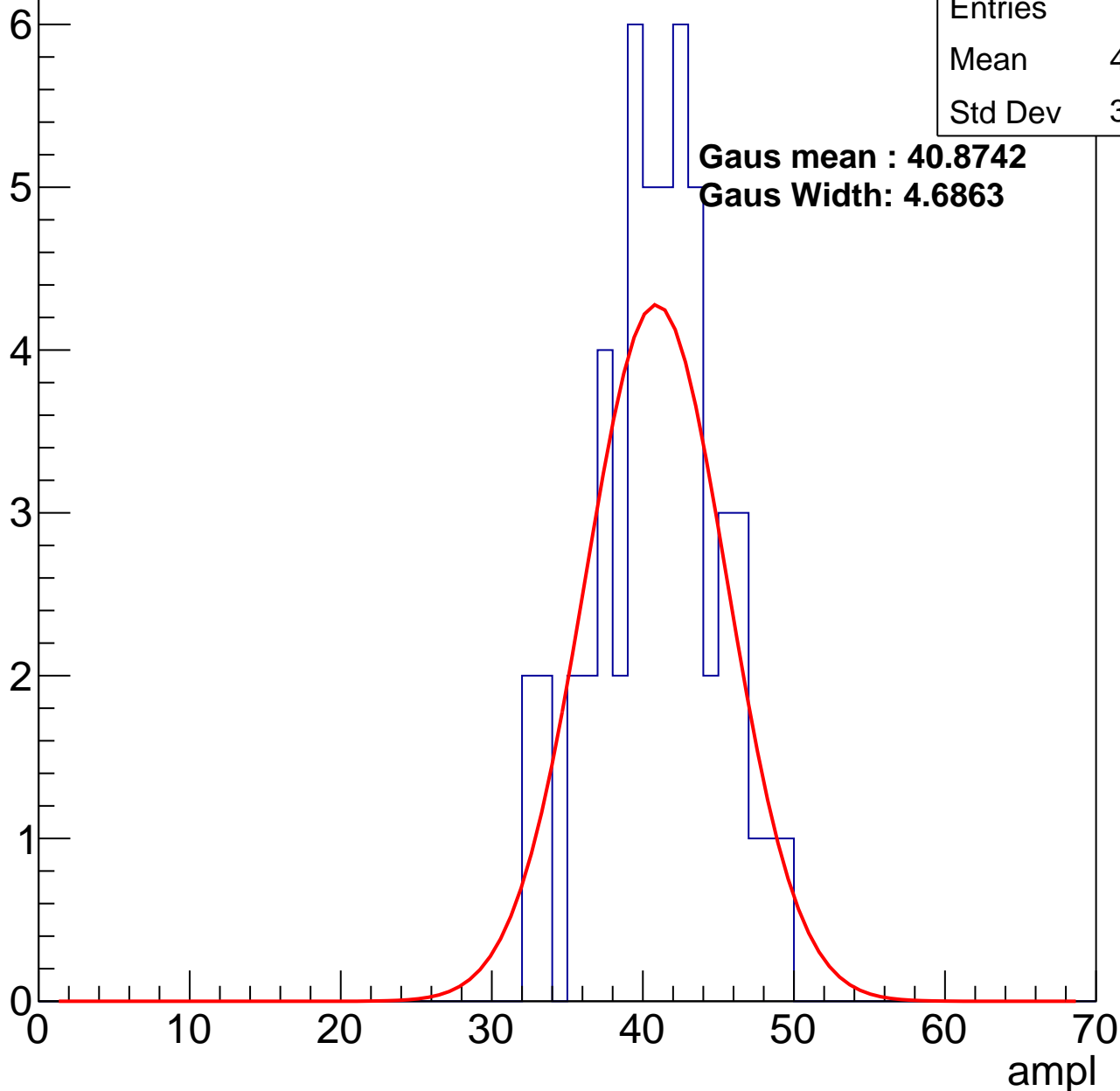
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	40.52
Std Dev	3.988

**Gaus mean : 40.8742**

**Gaus Width: 4.6863**

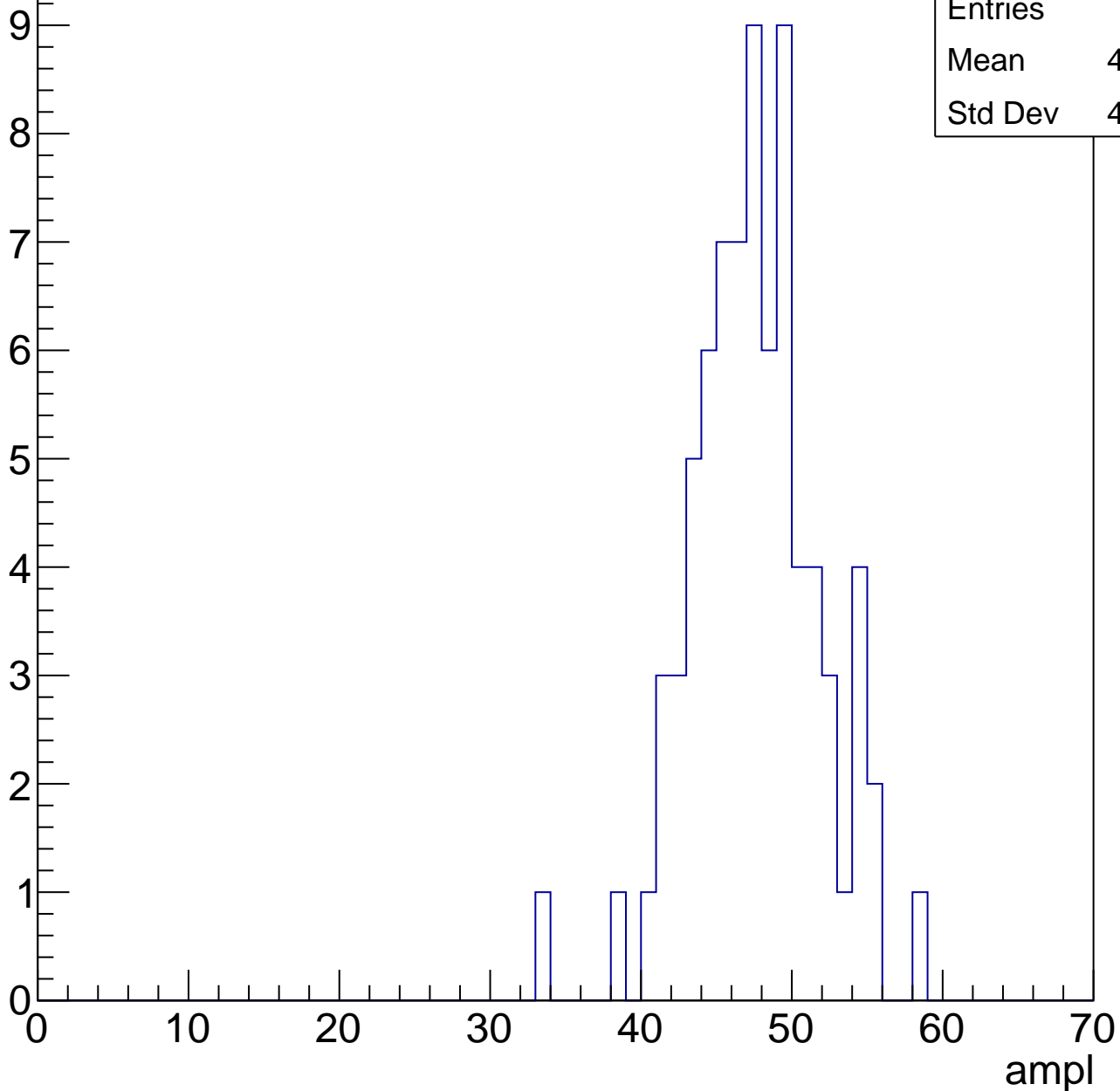


# B1L103S, U16-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	47.08
Std Dev	4.227

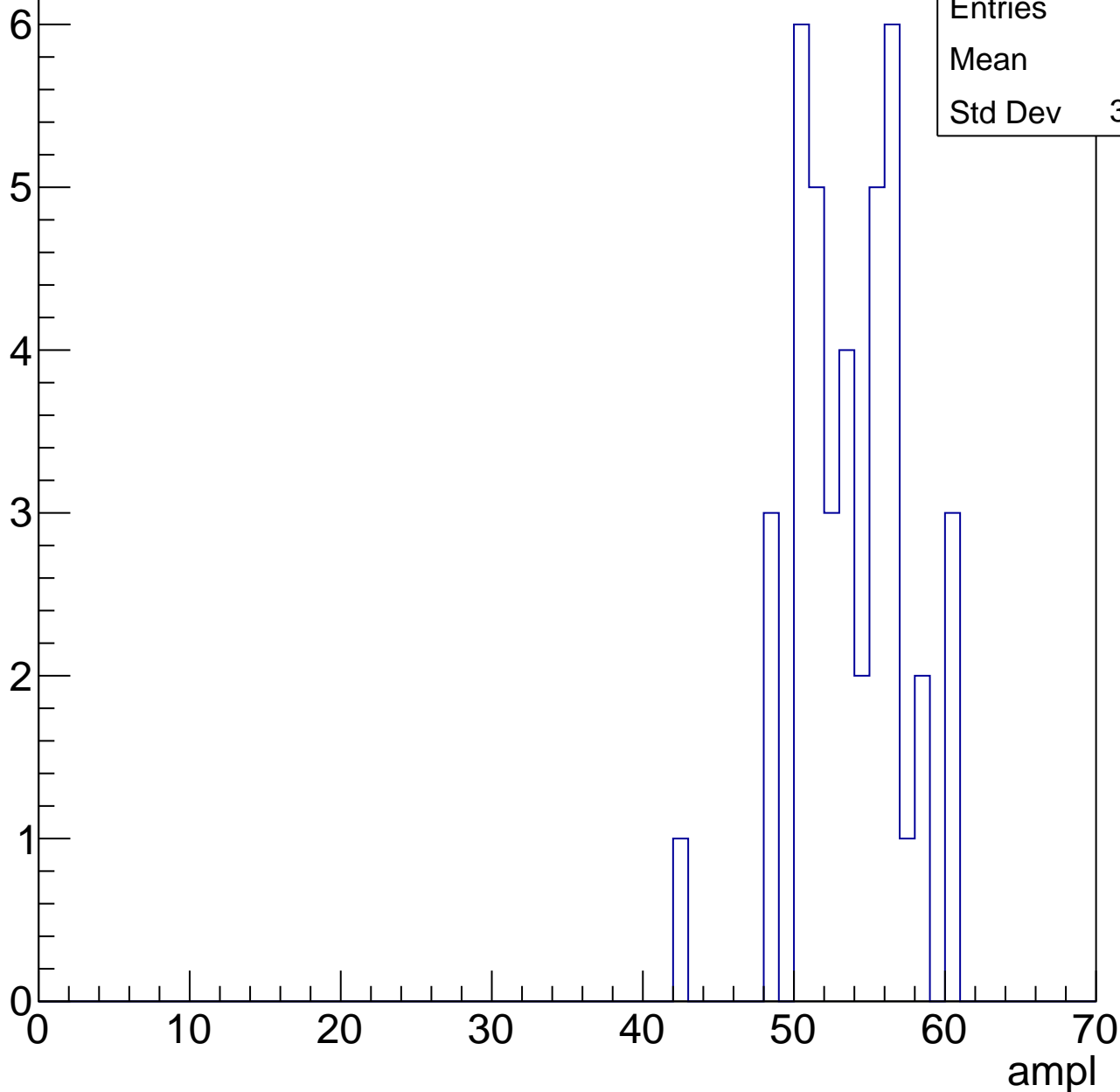


# B1L103S, U16-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	41
Mean	53.2
Std Dev	3.697



# B1L103S, U16-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	57
Mean	57.04
Std Dev	2.932

Entry

10

8

6

4

2

0

0

10

20

30

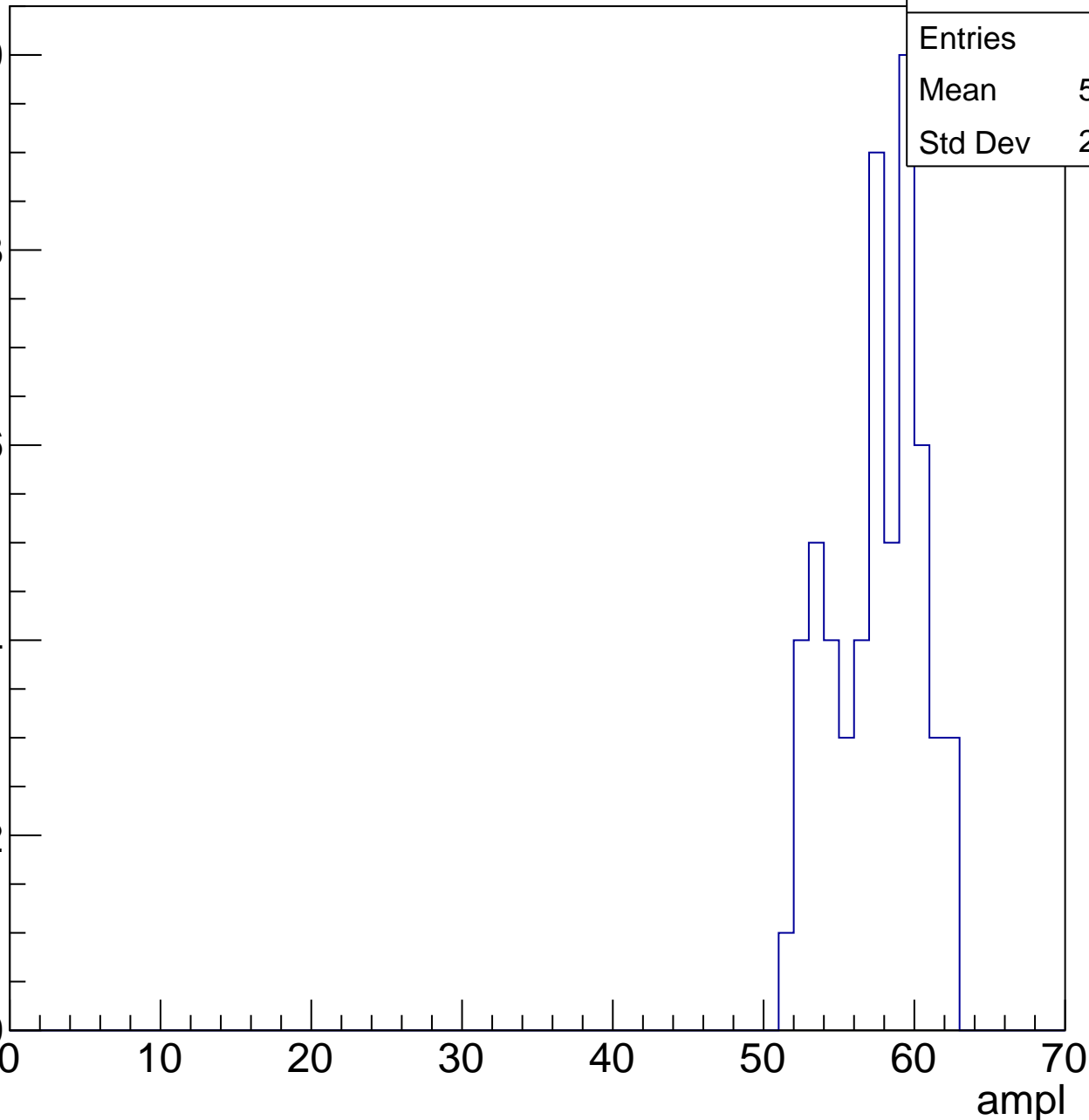
40

50

60

70

ampl

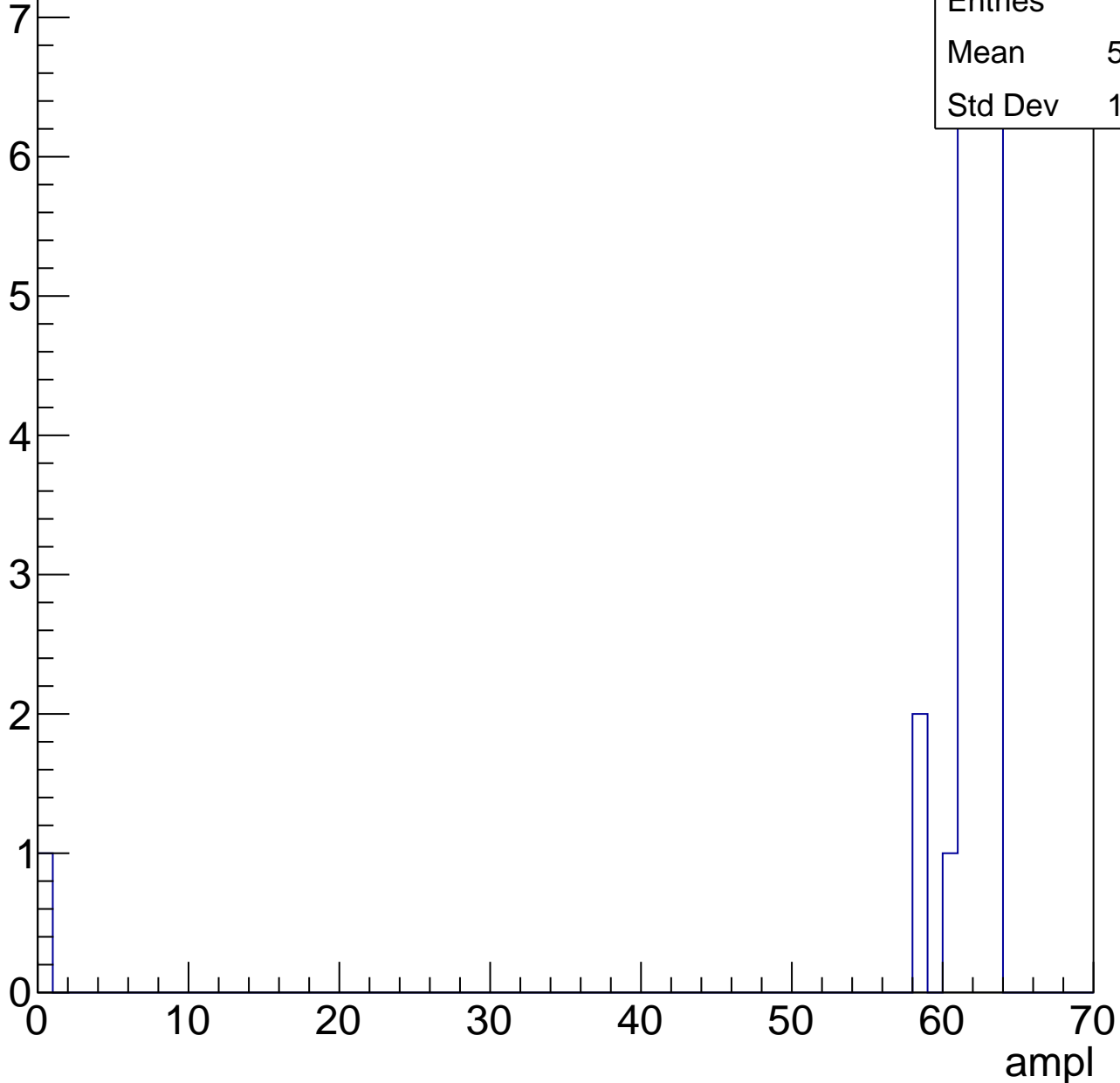


# B1L103S, U16-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	25
Mean	59.12
Std Dev	12.14





# B1L103S, U16-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch103, adc0

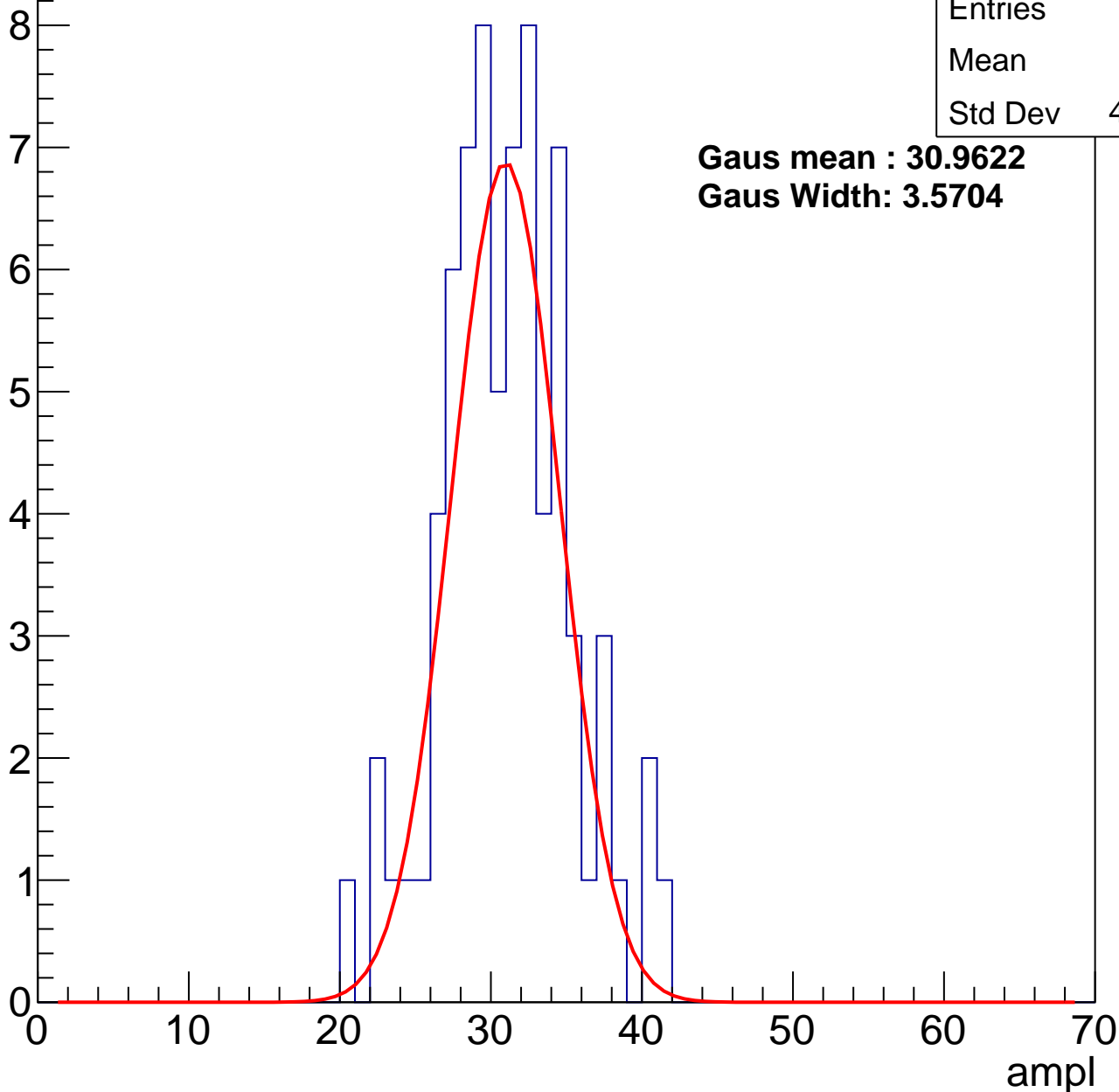
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	30.6
Std Dev	4.213

**Gaus mean : 30.9622**

**Gaus Width: 3.5704**



# B1L103S, U16-ch103, adc1

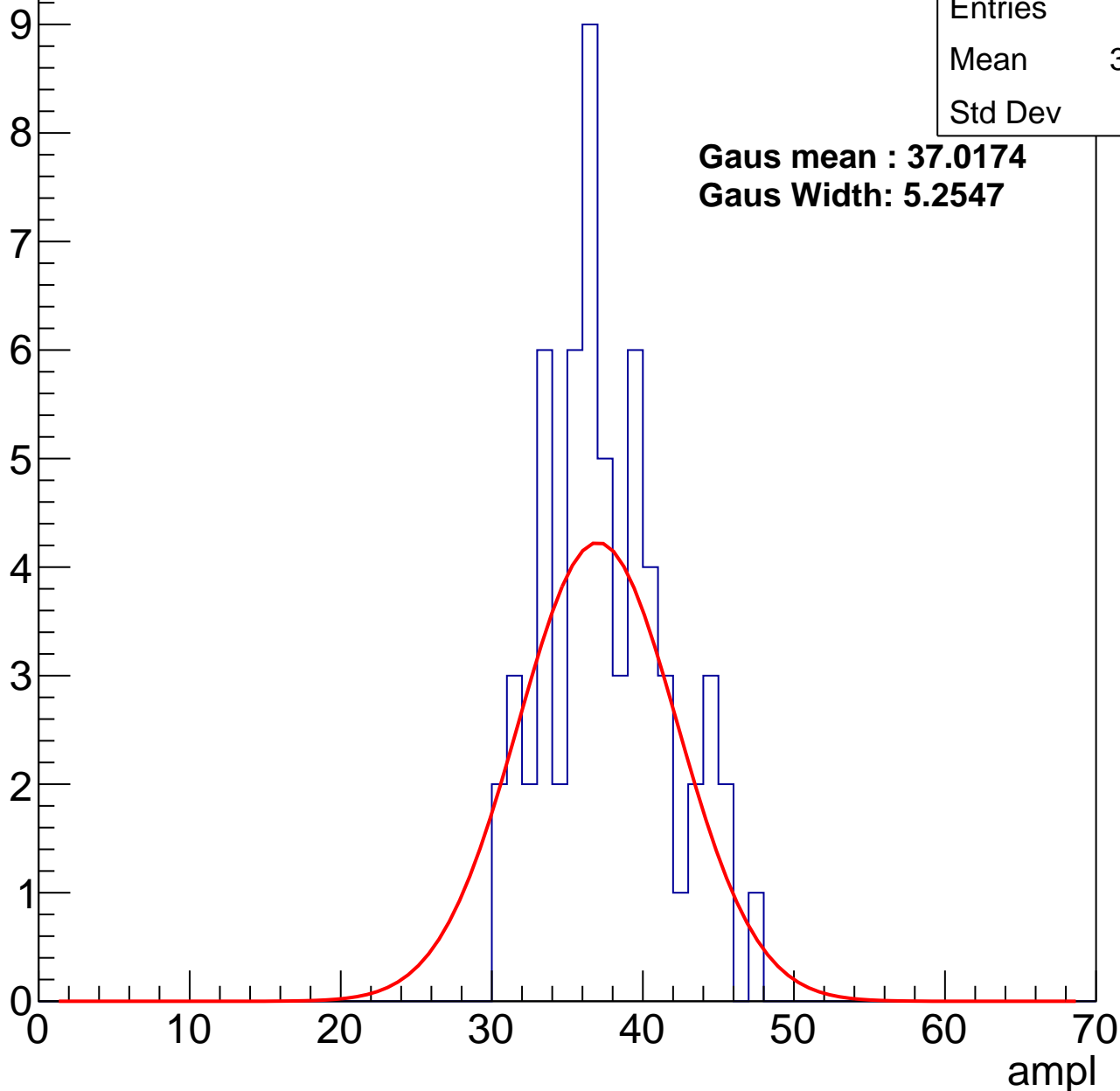
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	37.17
Std Dev	4.05

**Gaus mean : 37.0174**

**Gaus Width: 5.2547**



# B1L103S, U16-ch103, adc2

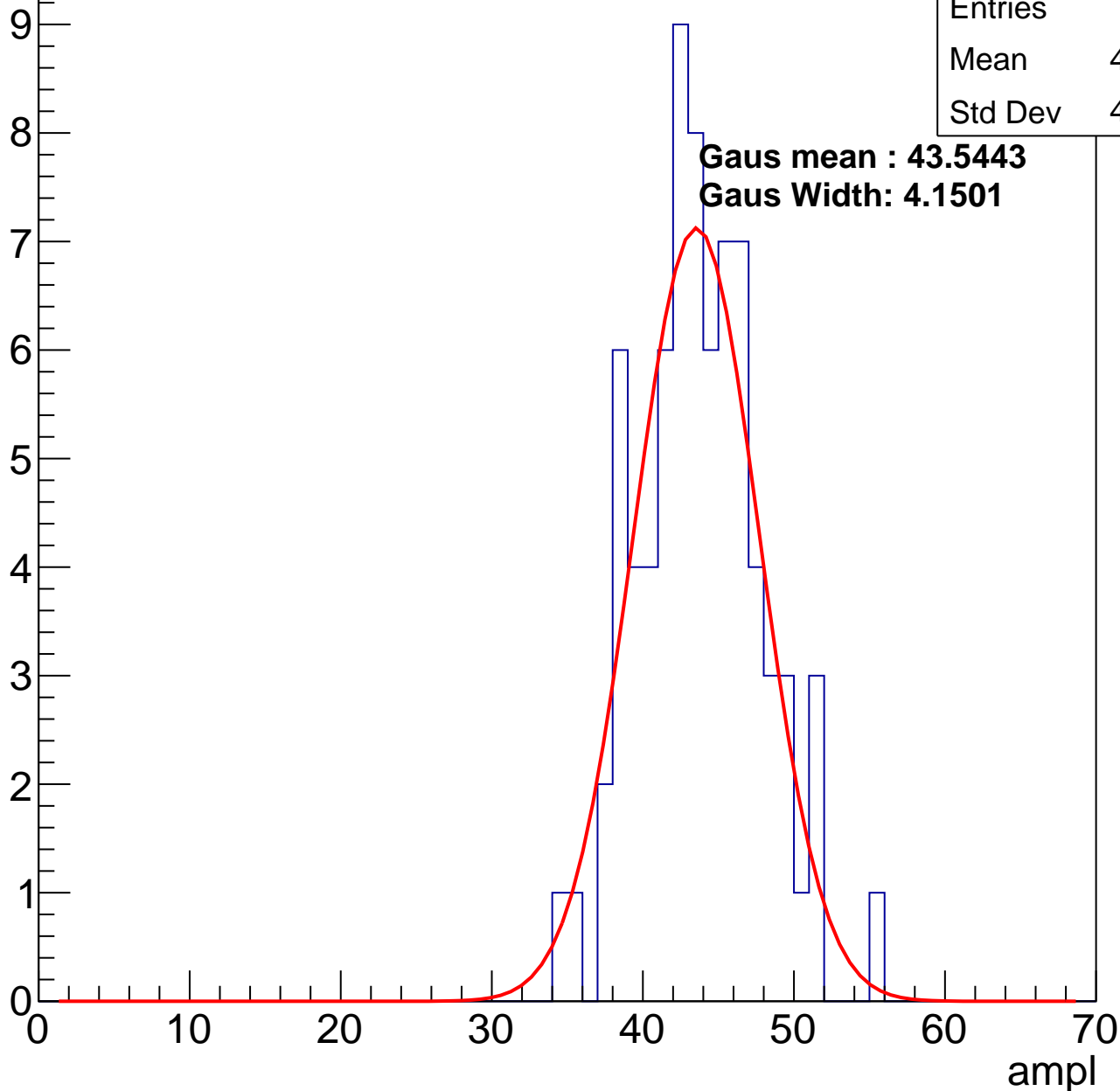
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	43.33
Std Dev	4.008

**Gaus mean : 43.5443**

**Gaus Width: 4.1501**

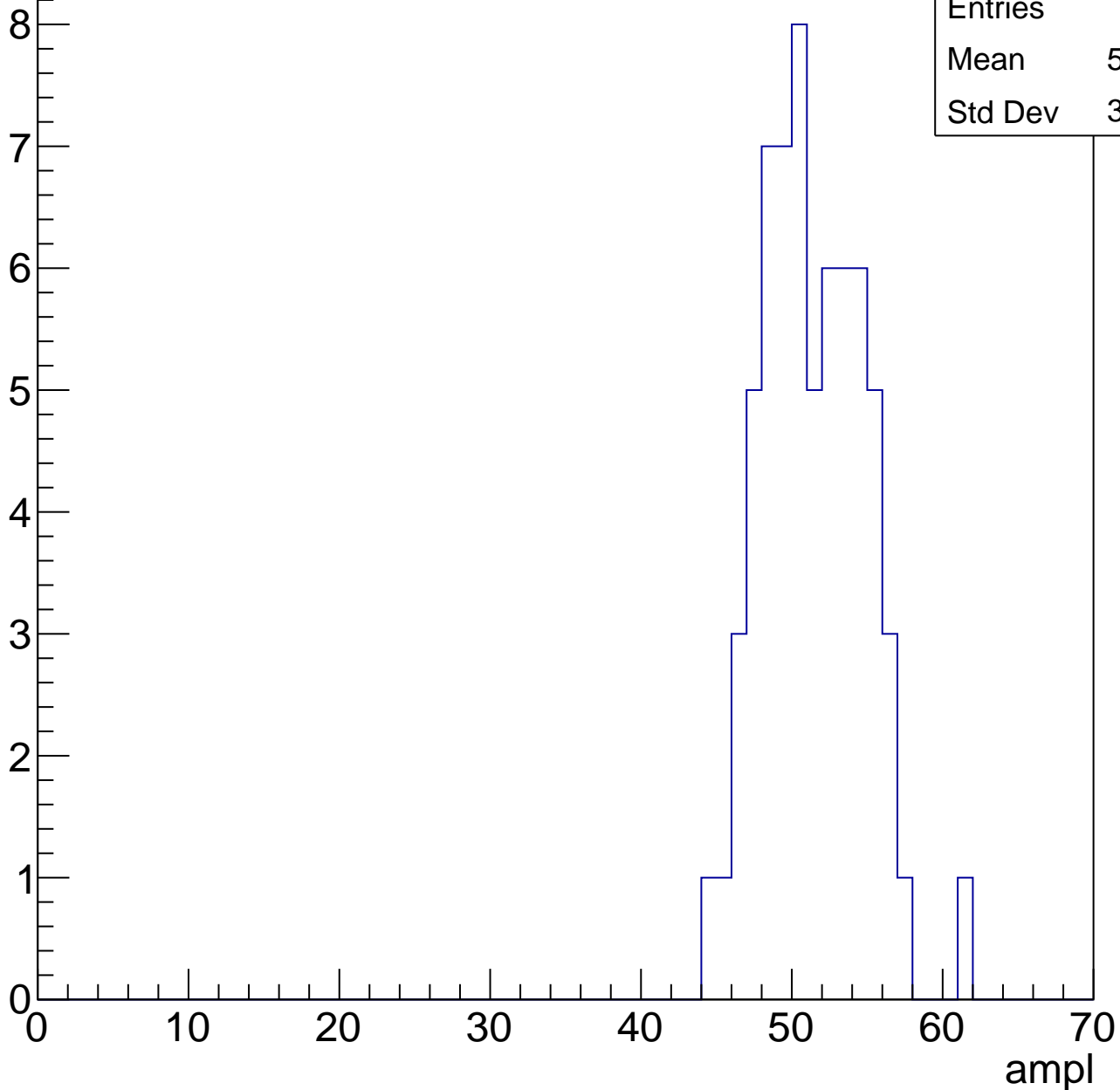


# B1L103S, U16-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	50.94
Std Dev	3.314

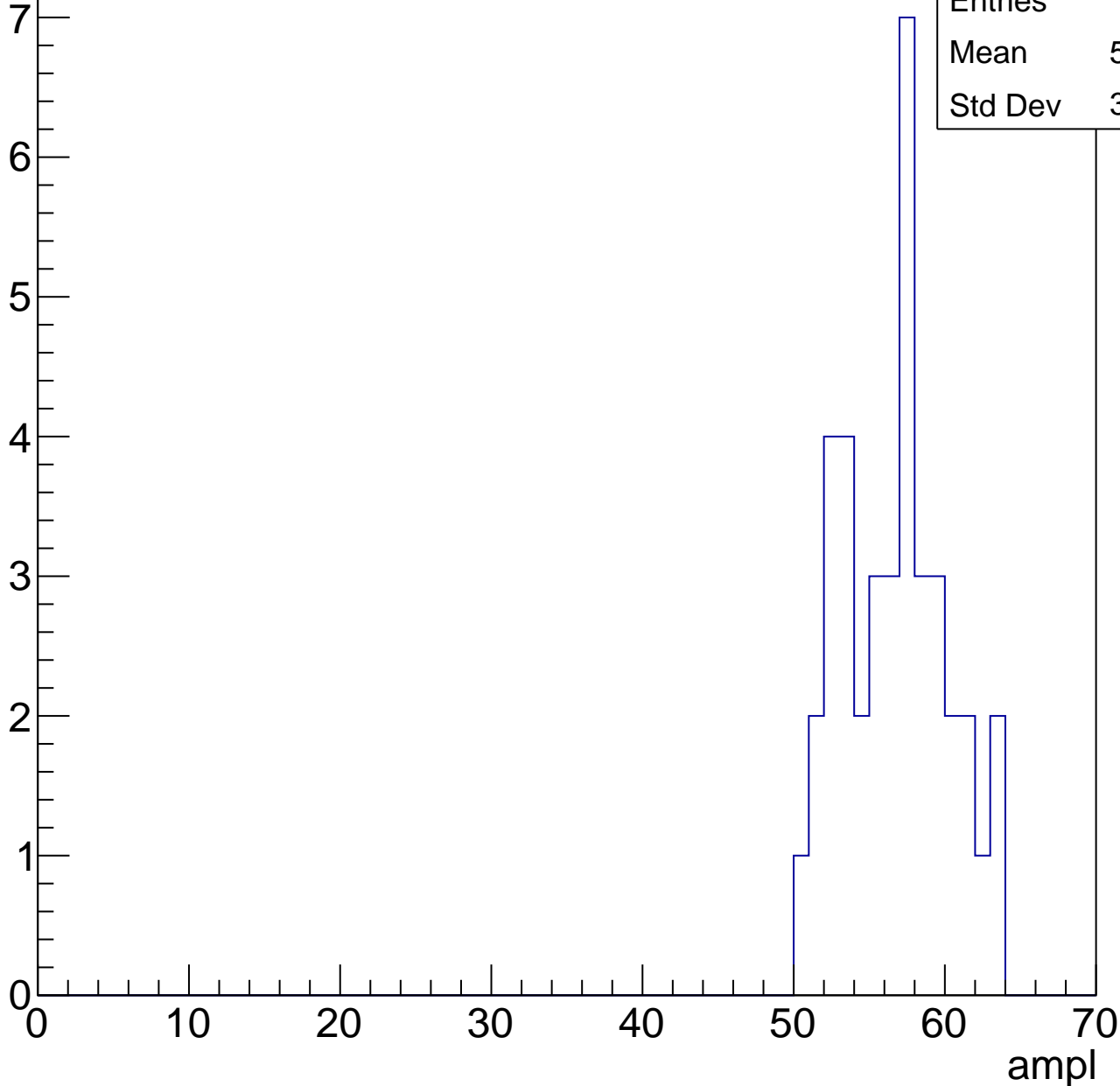


# B1L103S, U16-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	39
Mean	56.23
Std Dev	3.423



# B1L103S, U16-ch103, adc5

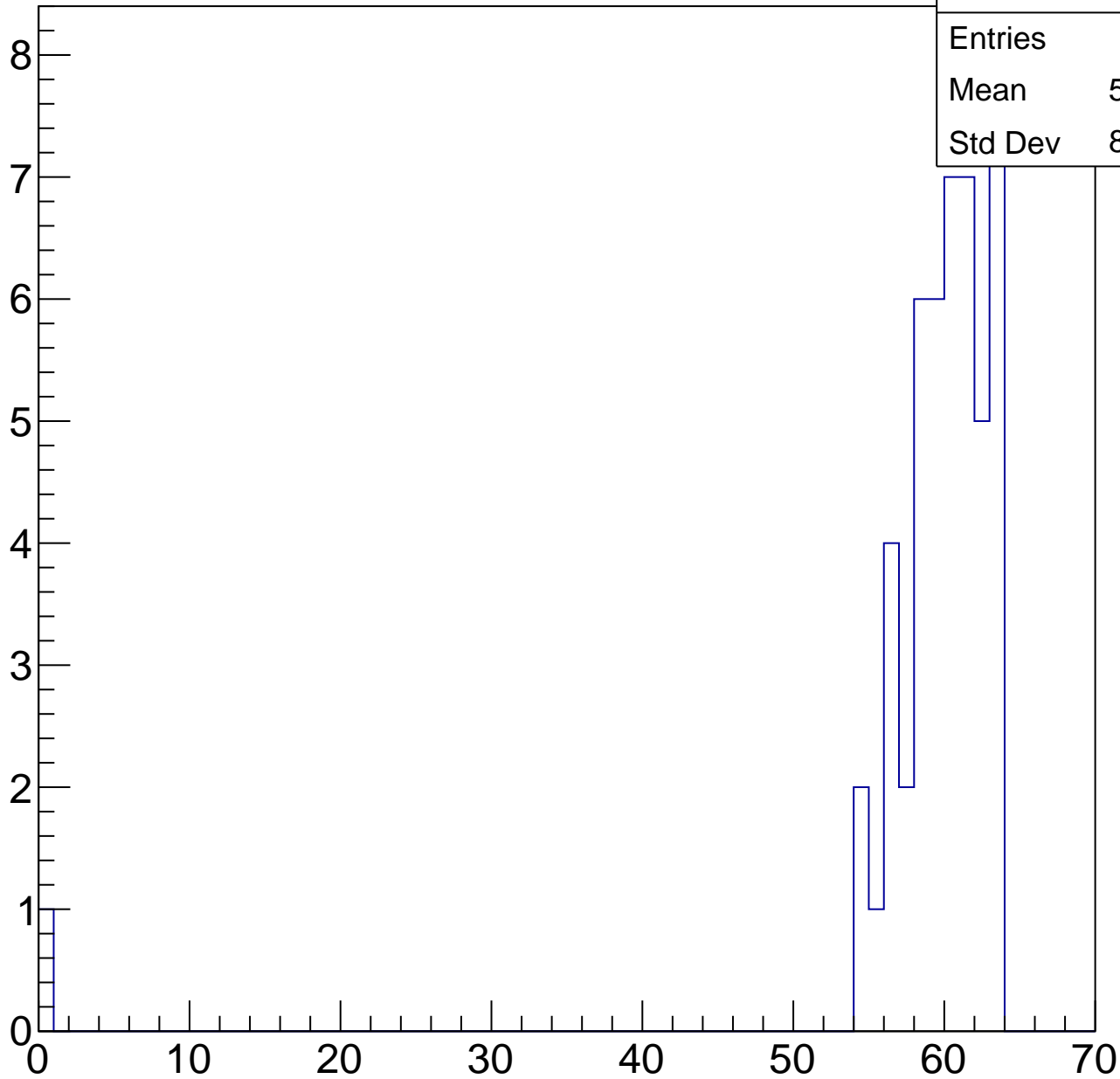
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	58.45
Std Dev	8.795

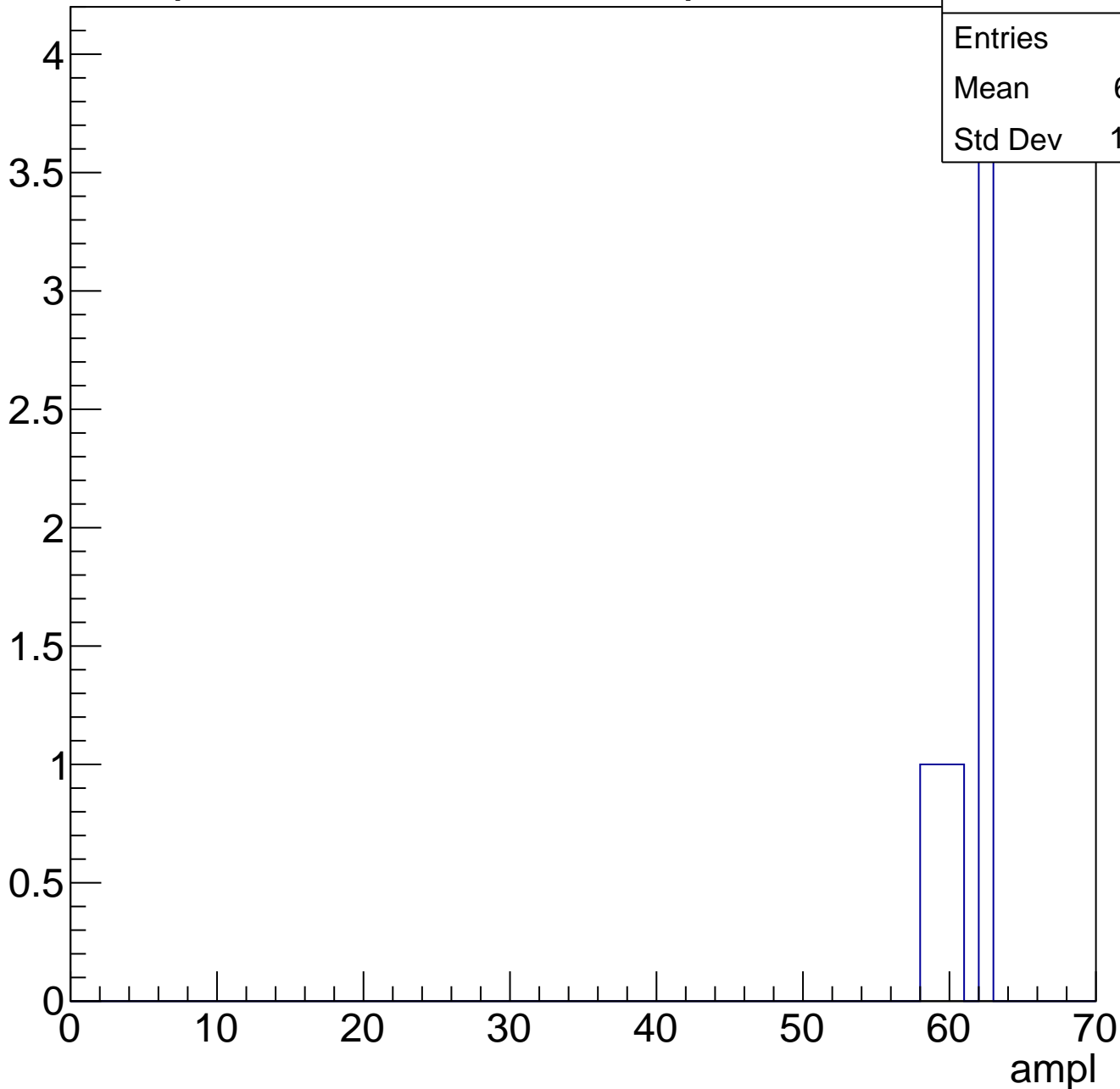
ampl



# B1L103S, U16-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U16-ch104, adc0

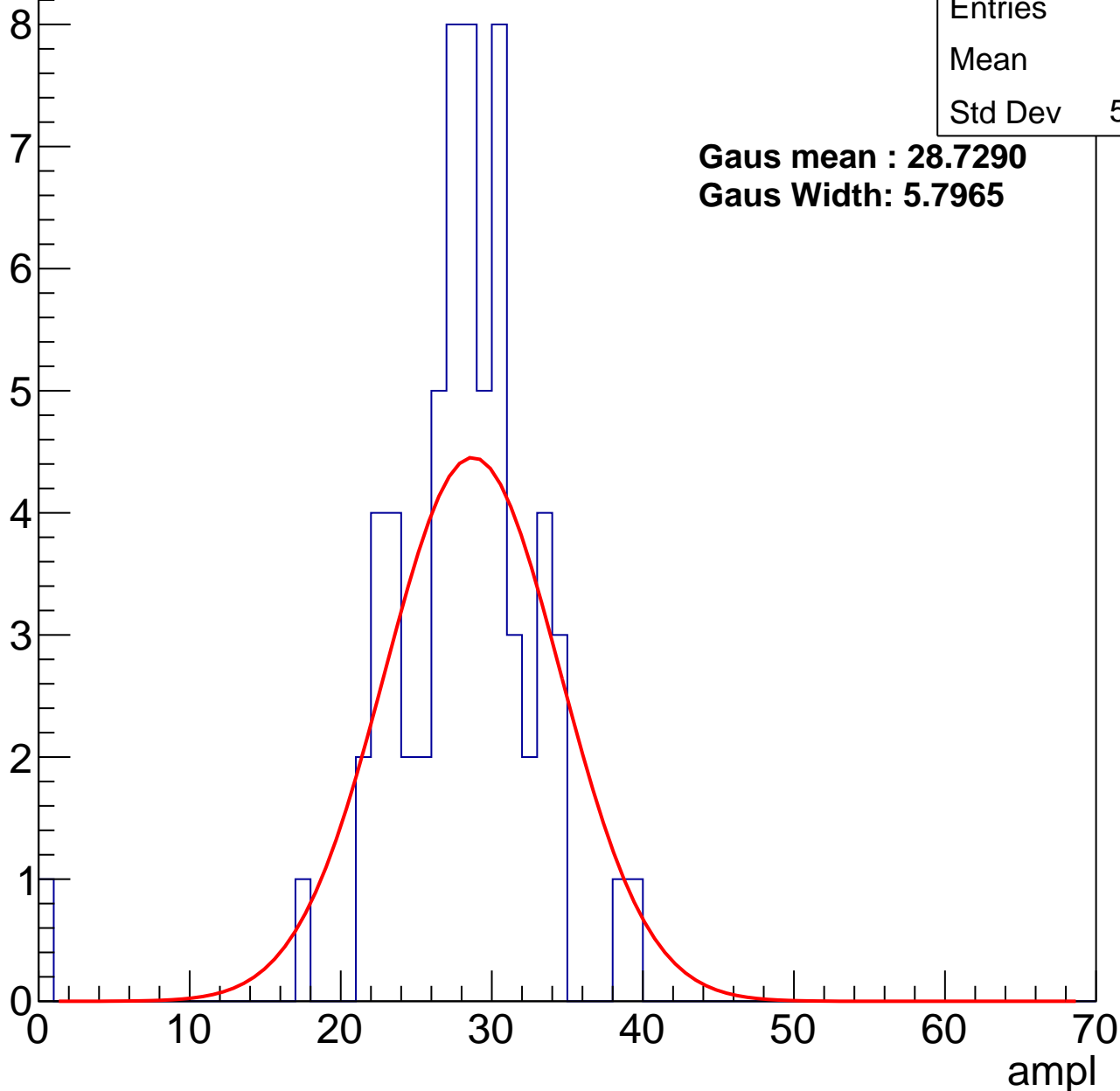
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	27.5
Std Dev	5.353

**Gaus mean : 28.7290**

**Gaus Width: 5.7965**



# B1L103S, U16-ch104, adc1

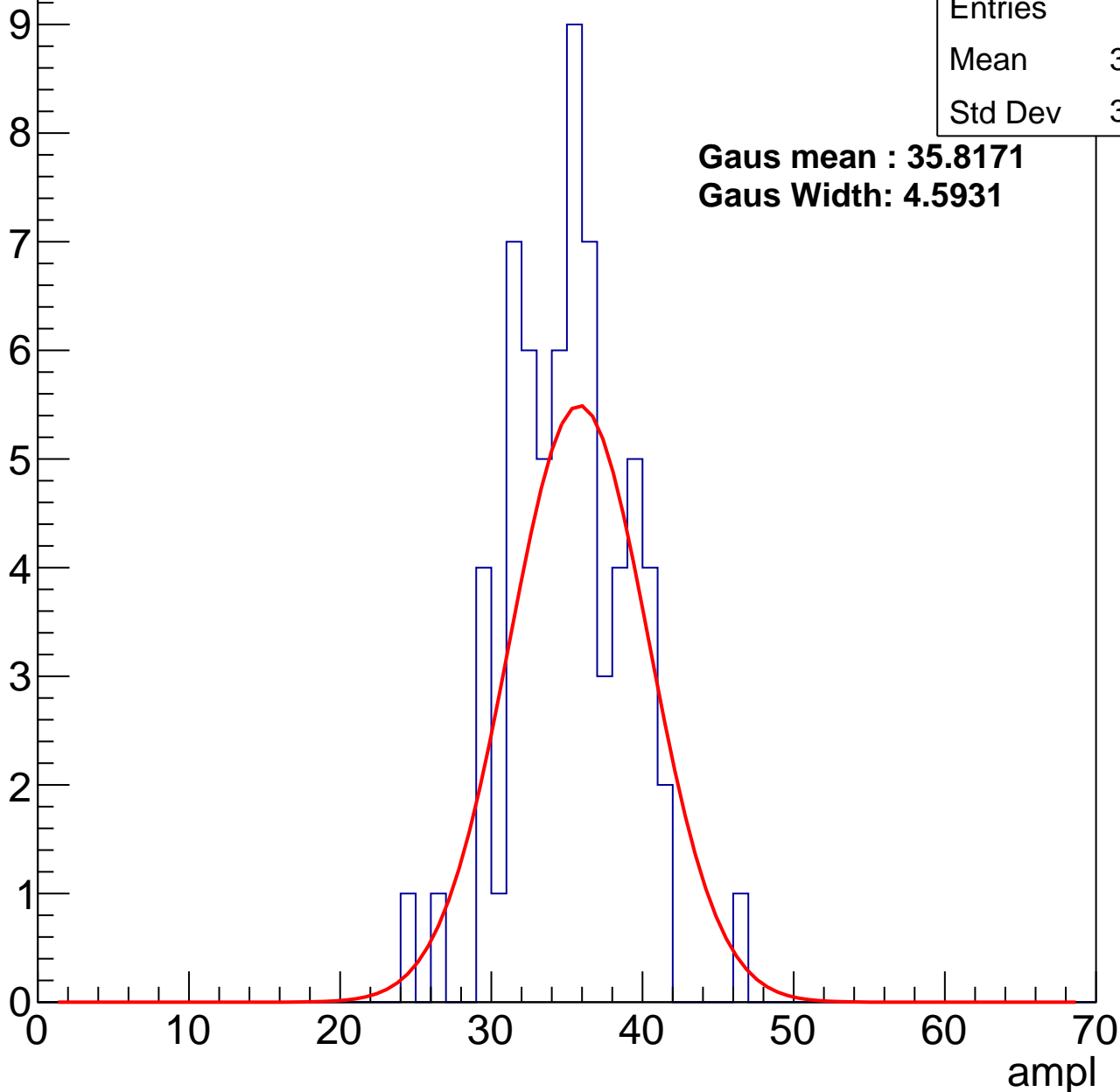
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	34.65
Std Dev	3.859

**Gaus mean : 35.8171**

**Gaus Width: 4.5931**



# B1L103S, U16-ch104, adc2

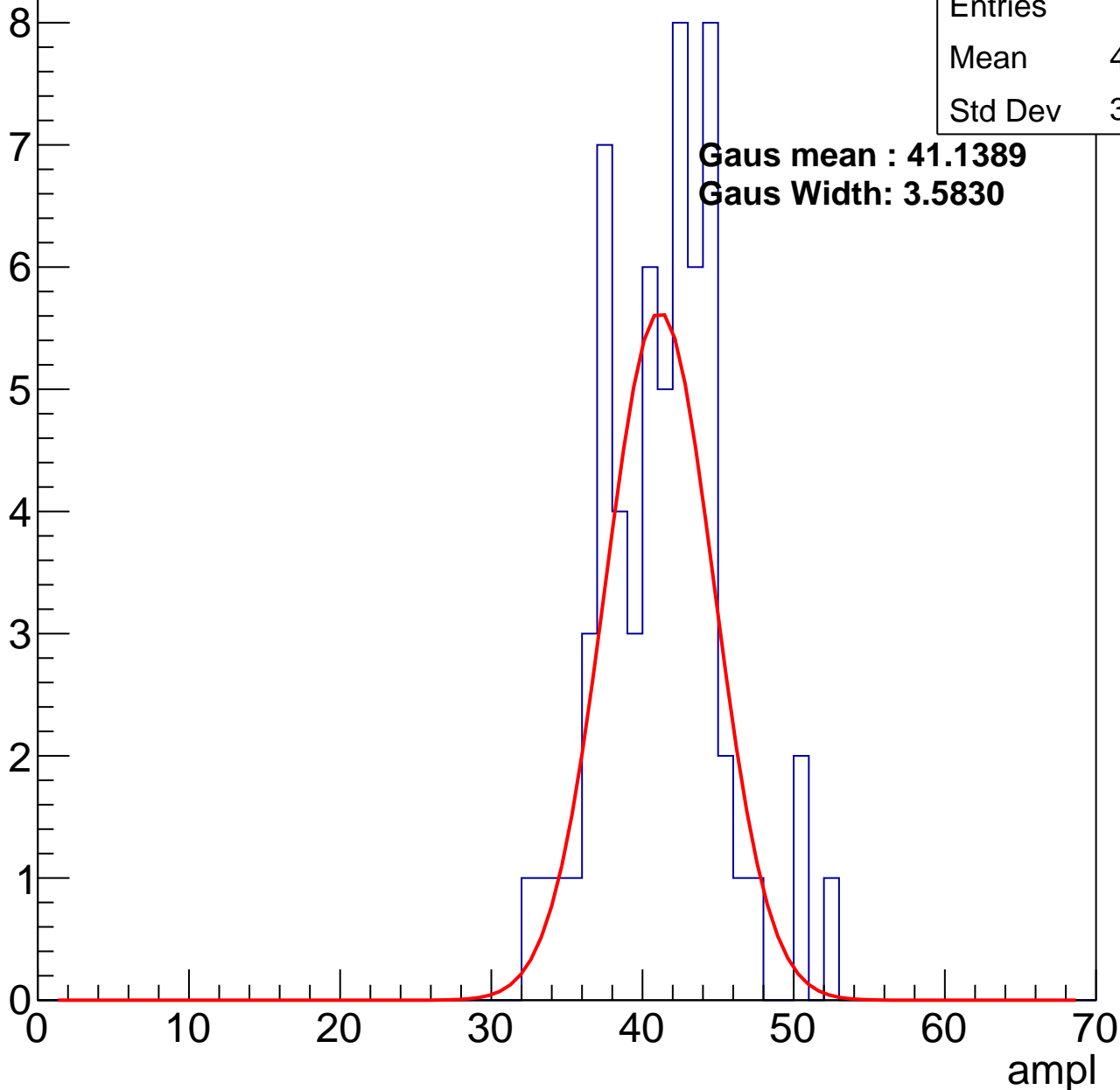
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	40.92
Std Dev	3.948

**Gaus mean : 41.1389**

**Gaus Width: 3.5830**

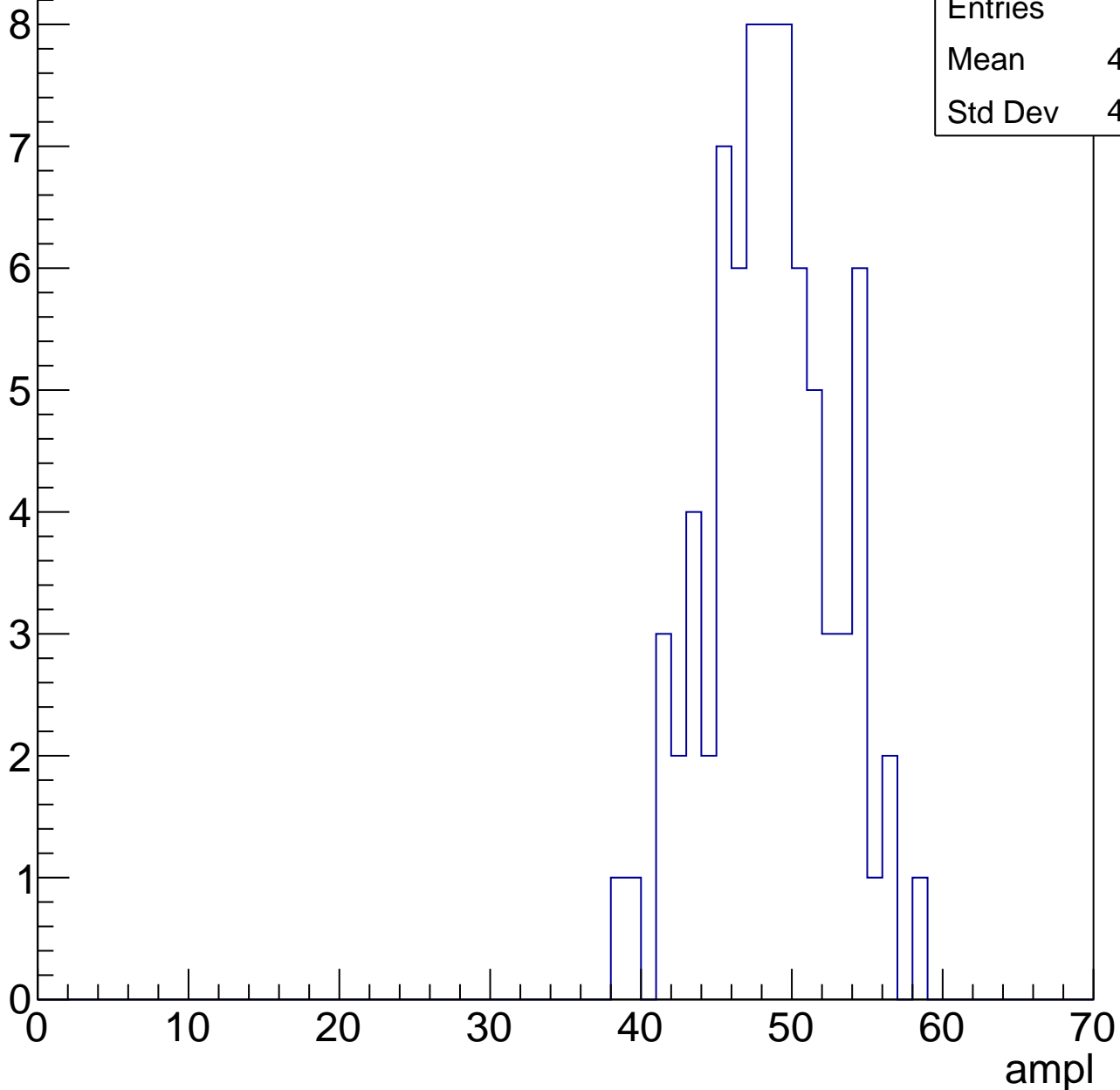


# B1L103S, U16-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	48.13
Std Dev	4.138

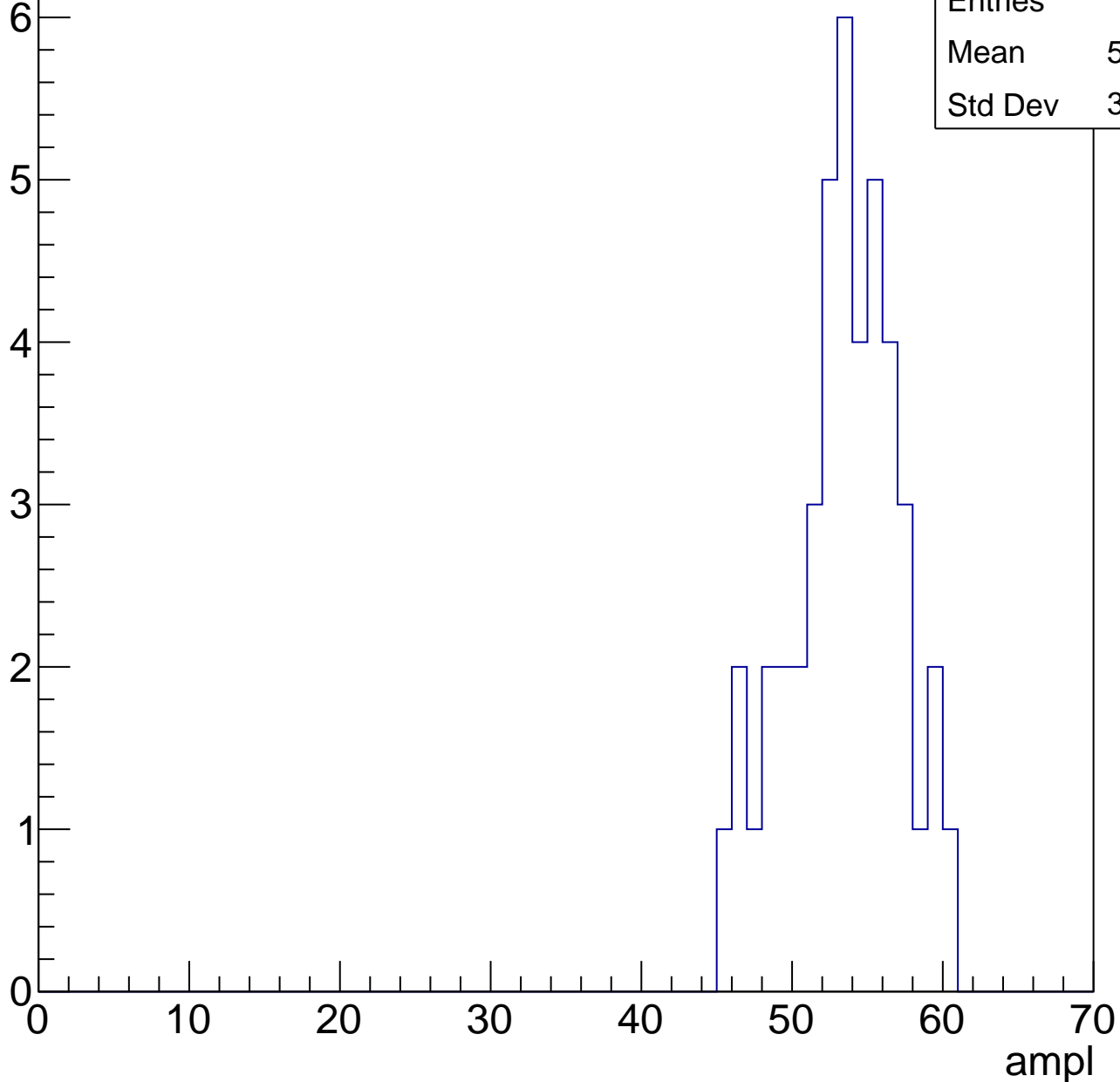


# B1L103S, U16-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	52.98
Std Dev	3.596

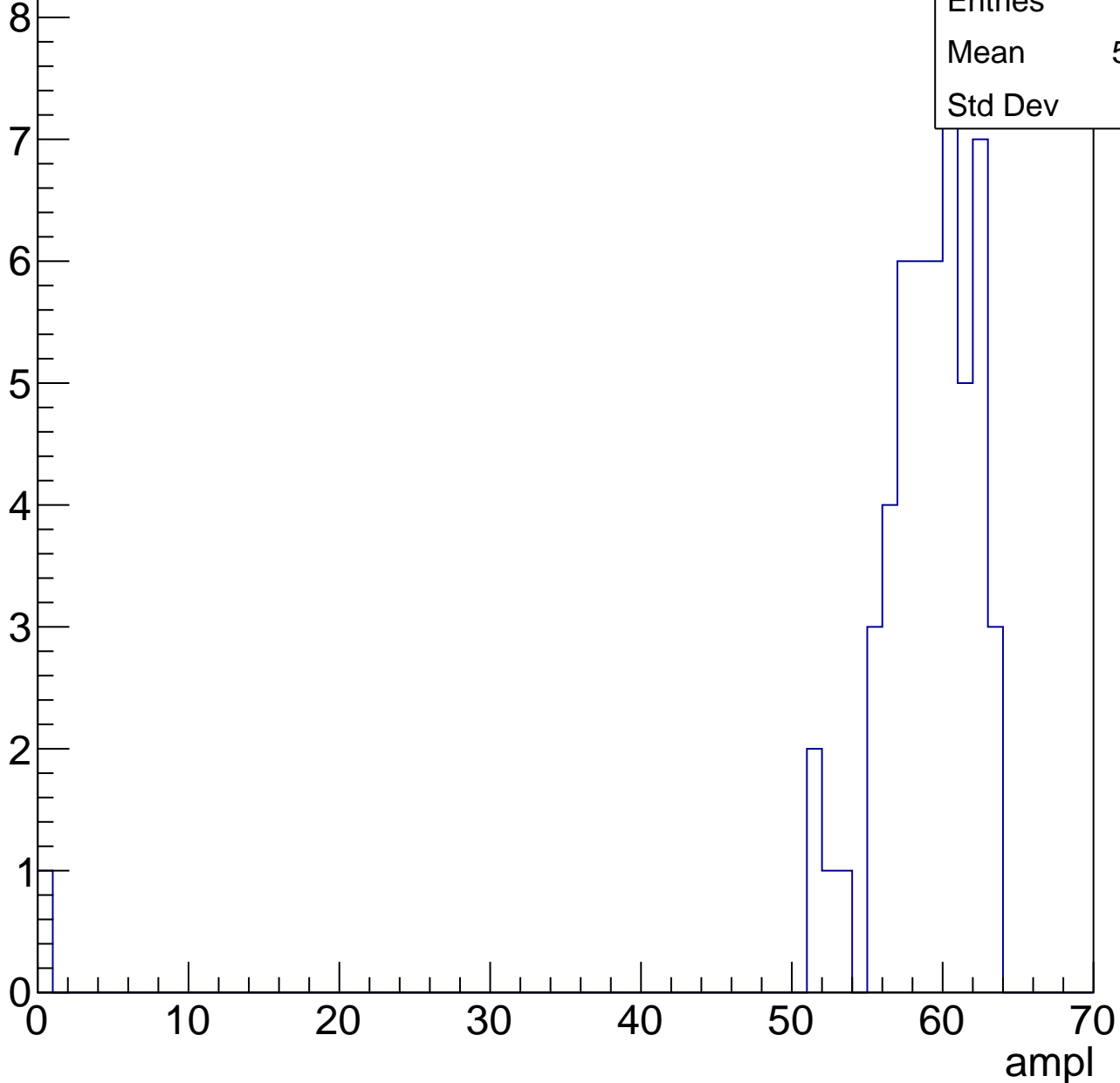


# B1L103S, U16-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	57.51
Std Dev	8.5

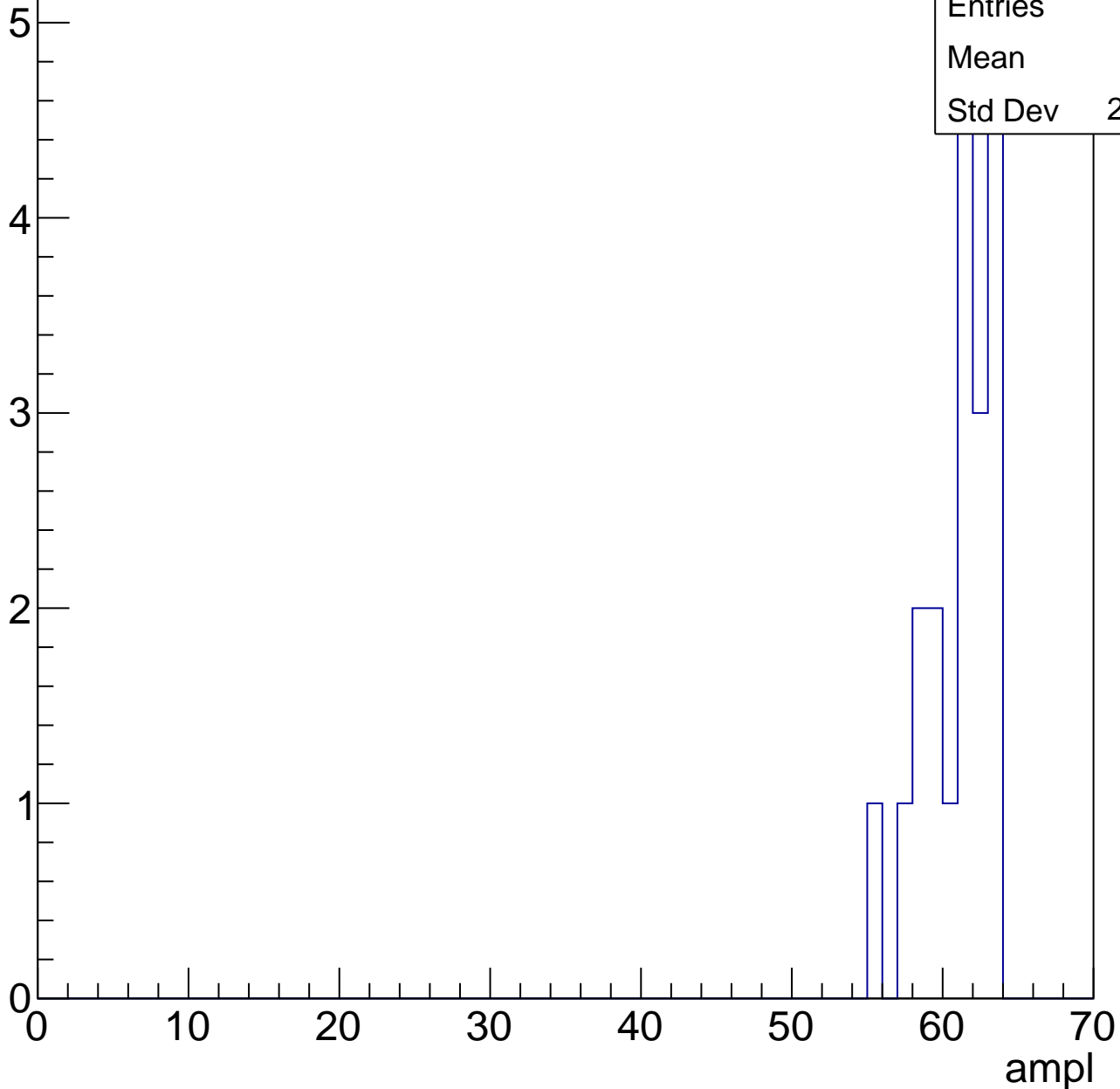


# B1L103S, U16-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	20
Mean	60.6
Std Dev	2.223





# B1L103S, U16-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch105, adc0

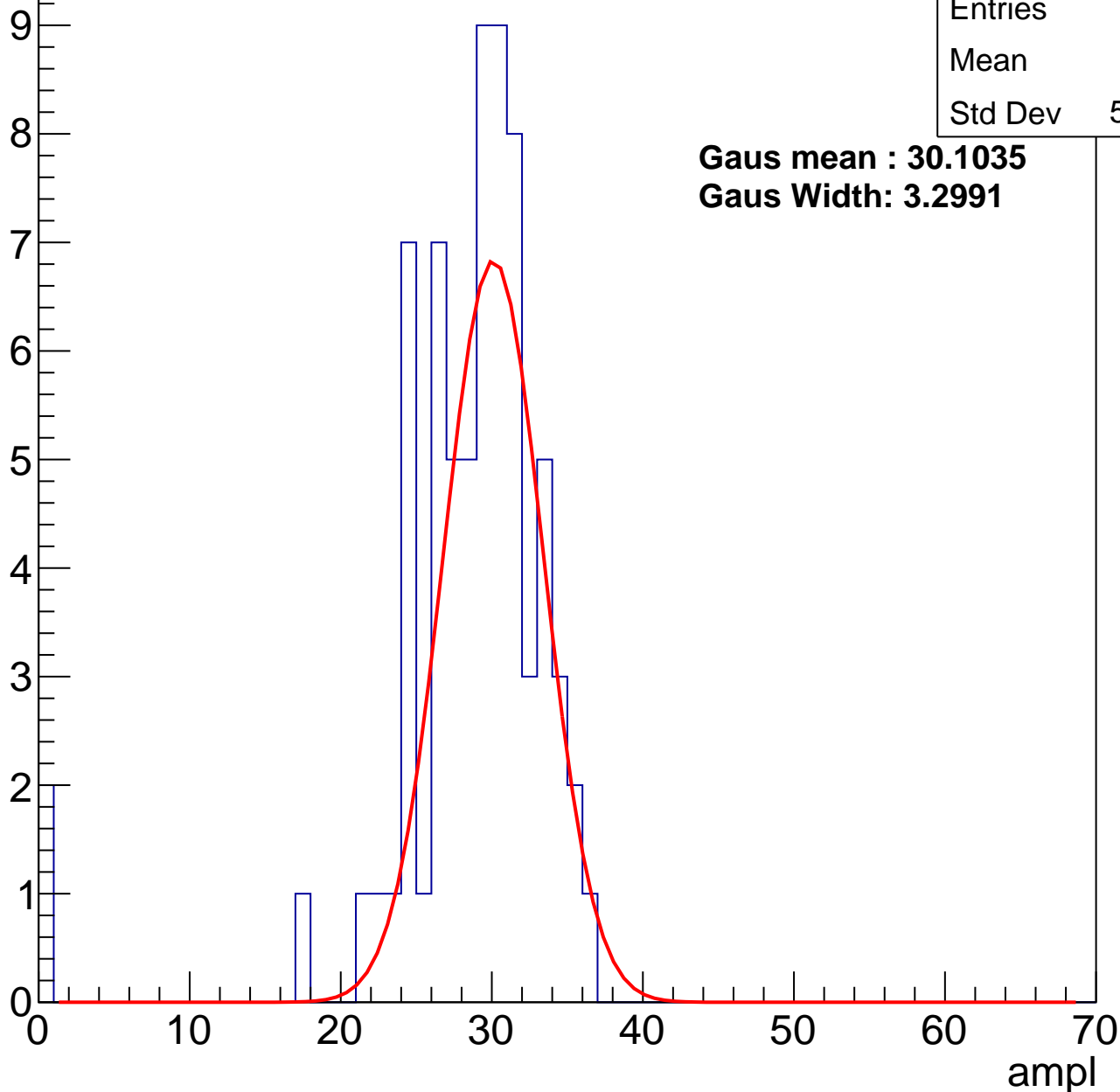
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	27.9
Std Dev	5.948

**Gaus mean : 30.1035**

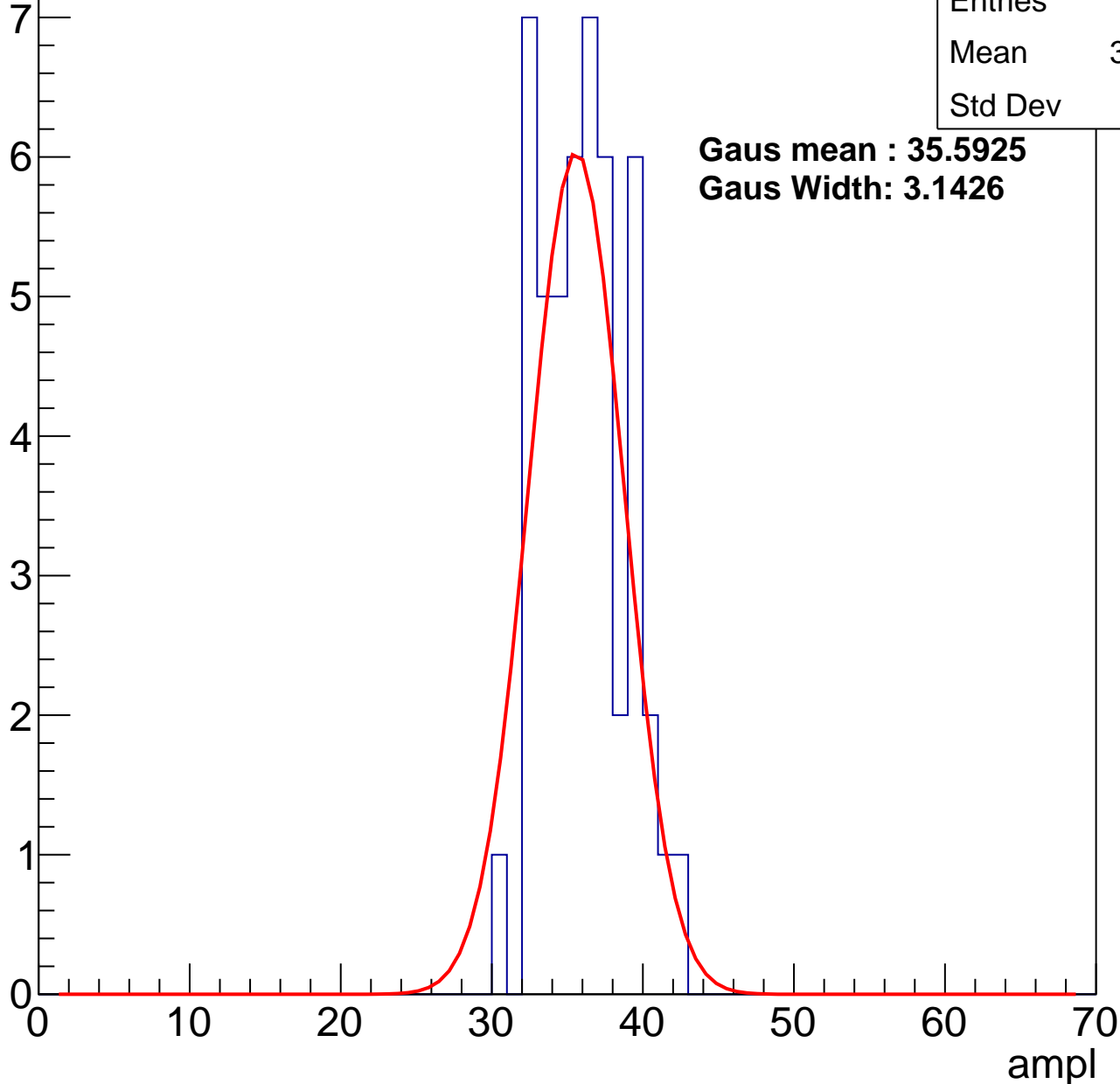
**Gaus Width: 3.2991**



# B1L103S, U16-ch105, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch105, adc2

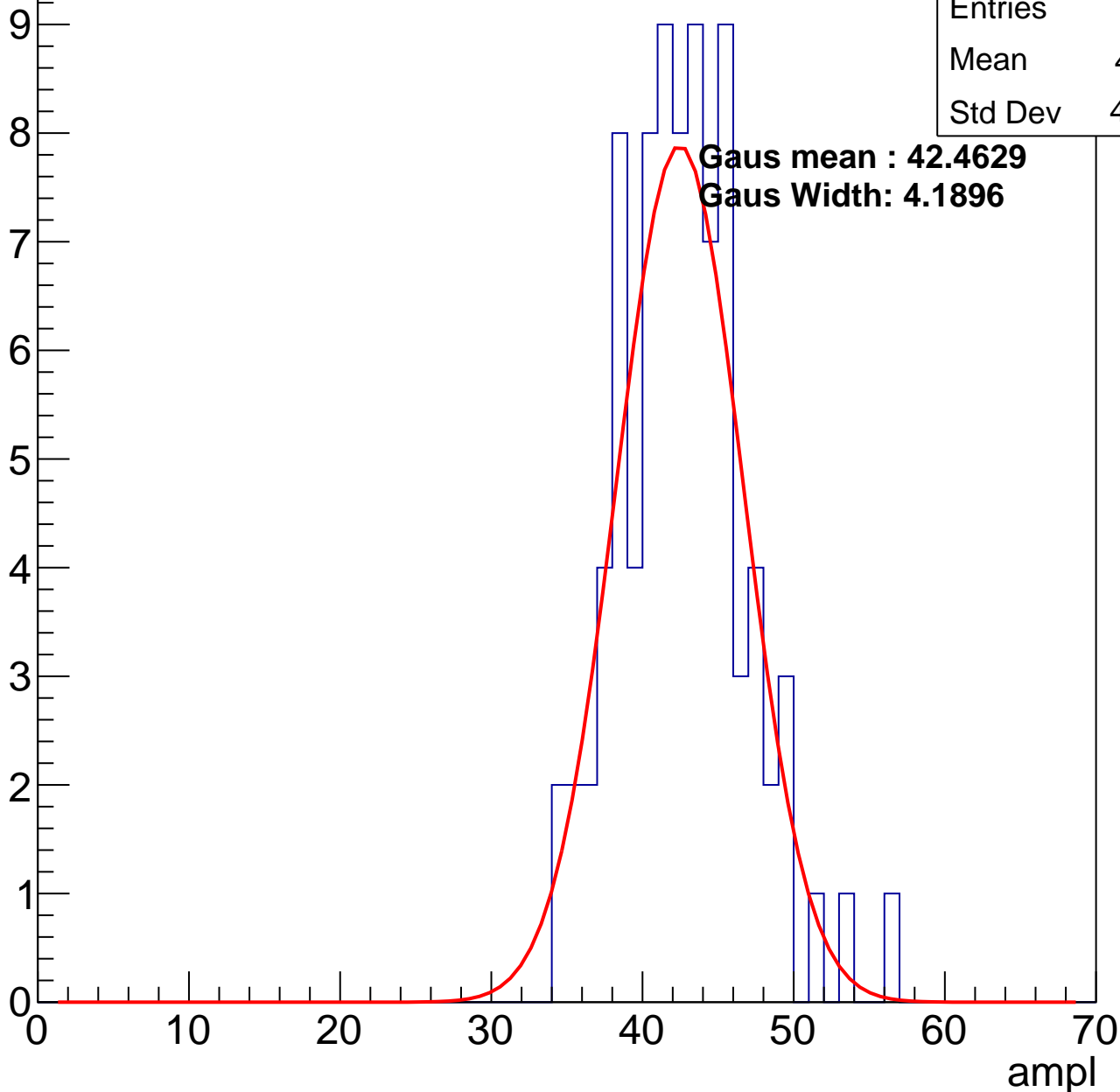
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	87
Mean	42.21
Std Dev	4.128

**Gaus mean : 42.4629**

**Gaus Width: 4.1896**

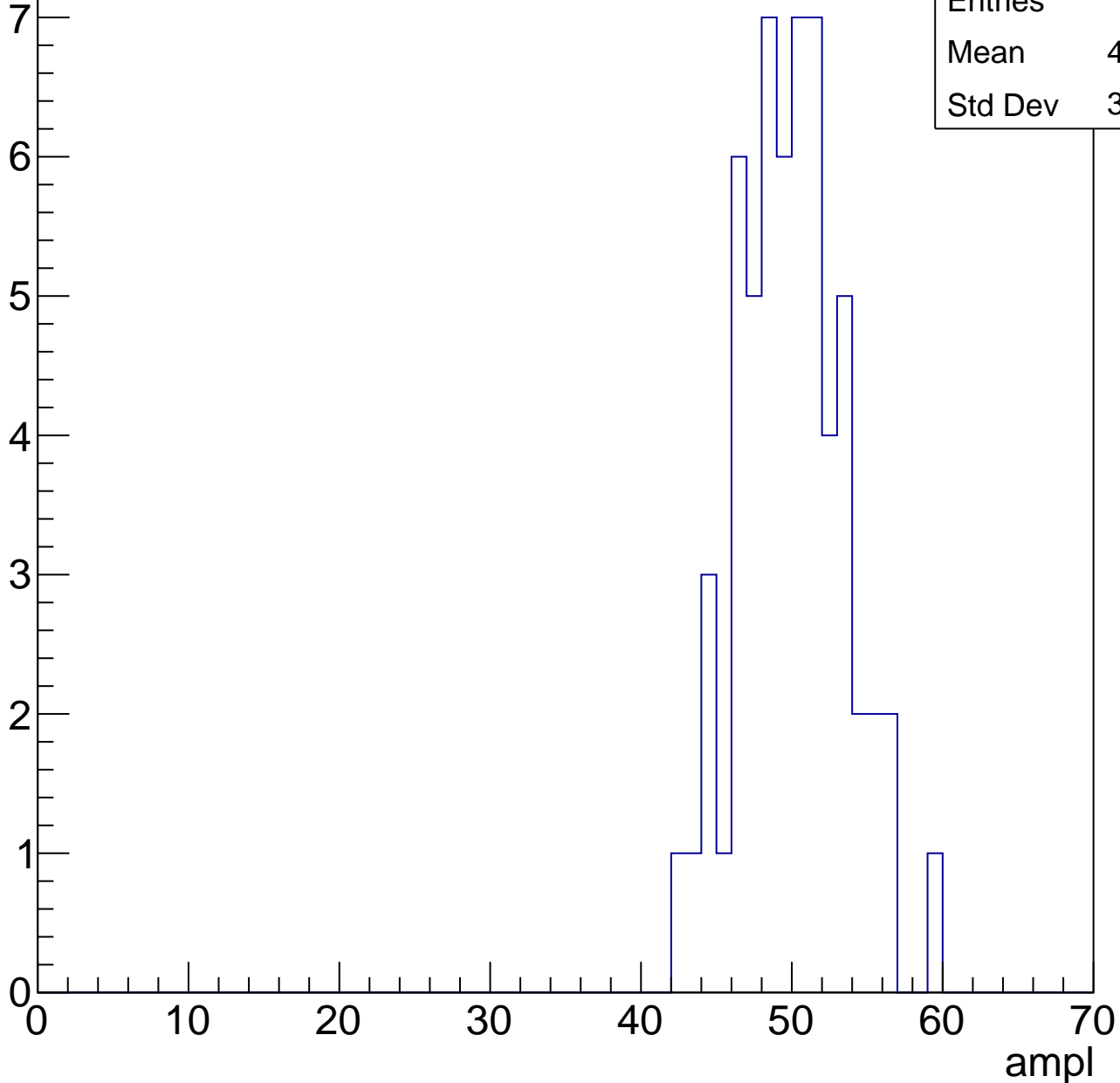


# B1L103S, U16-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	49.53
Std Dev	3.442

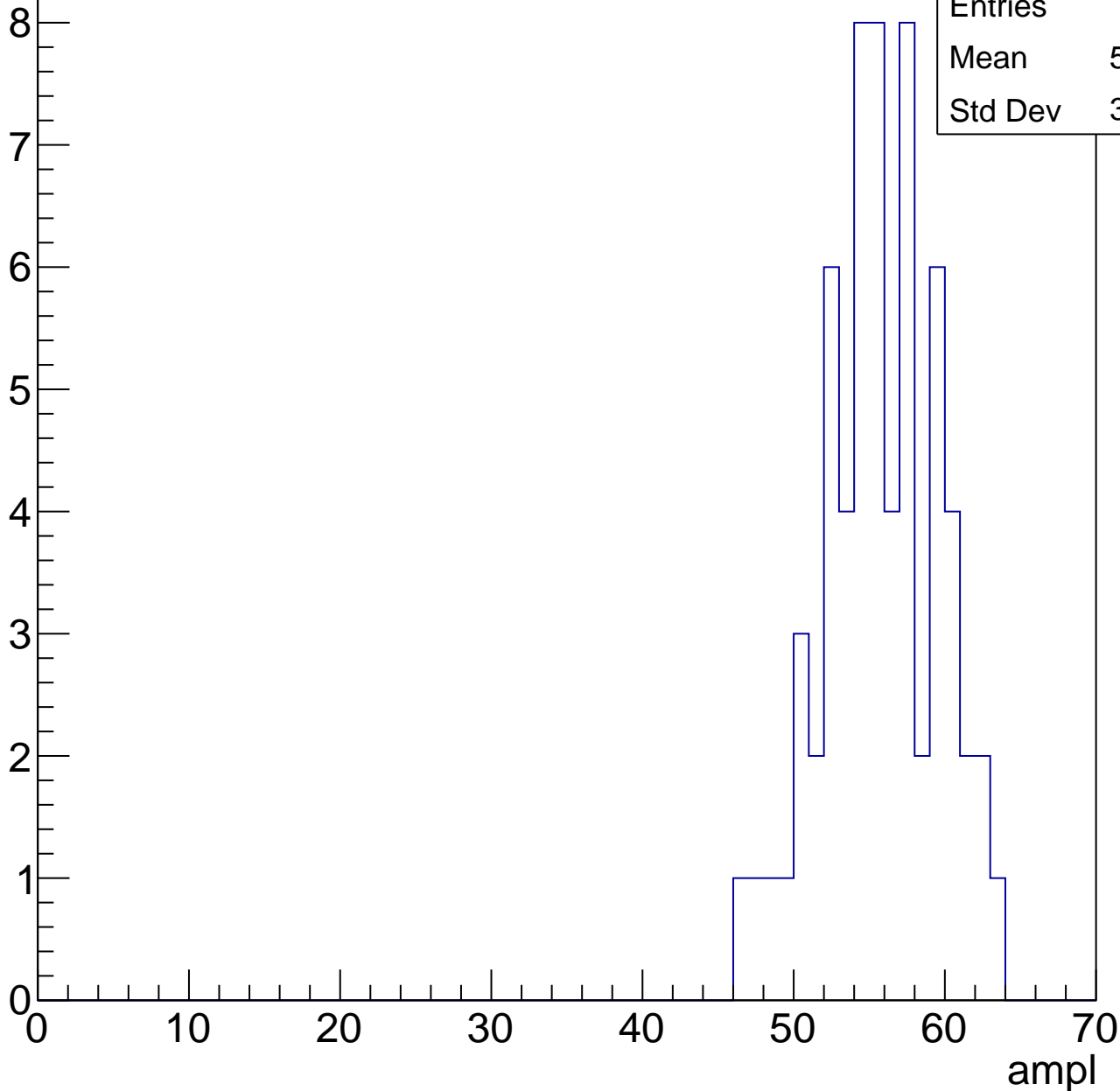


# B1L103S, U16-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	55.27
Std Dev	3.738



# B1L103S, U16-ch105, adc5

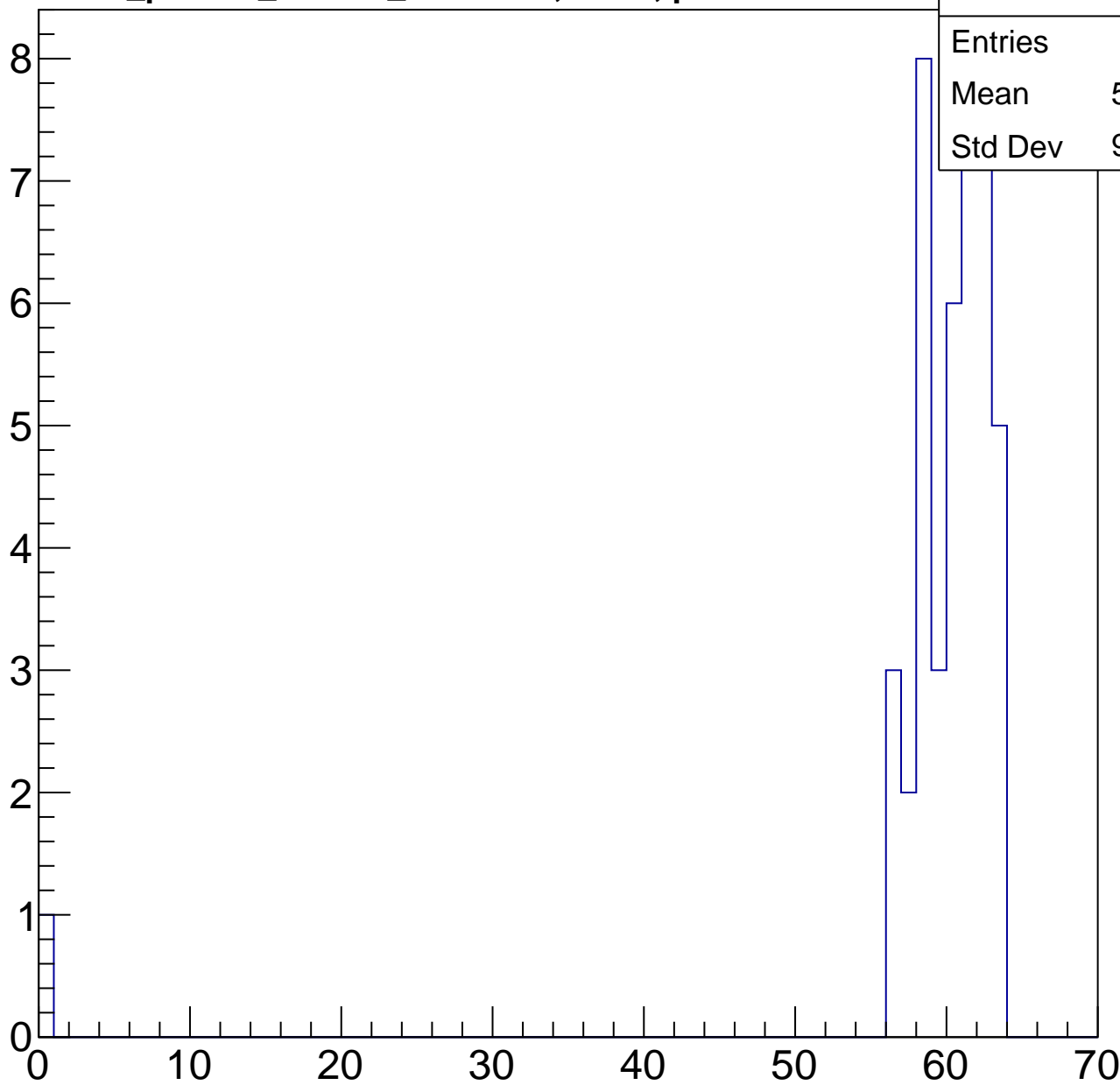
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	44
Mean	58.68
Std Dev	9.182

ampl



# B1L103S, U16-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch106, adc0

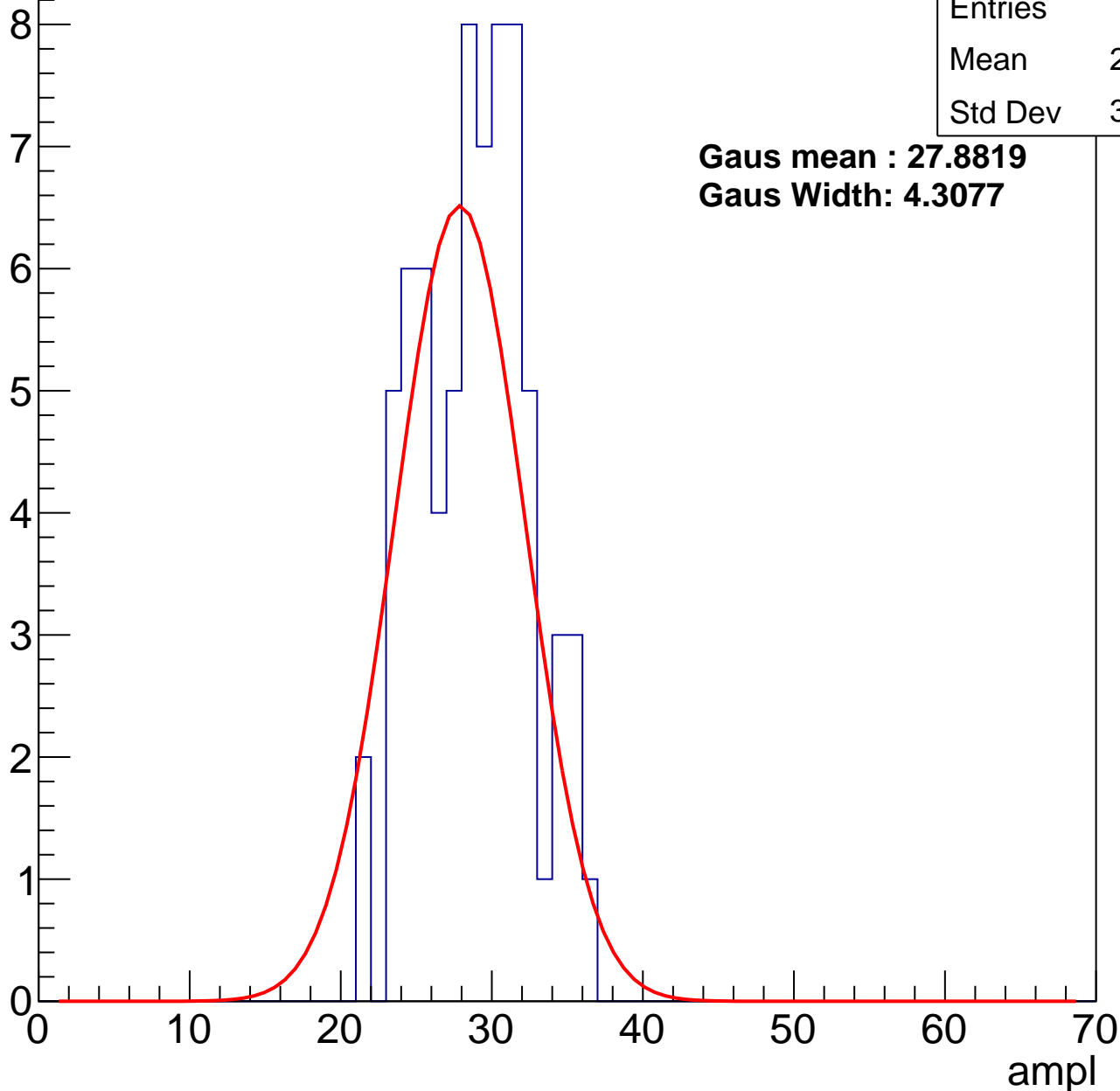
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	28.35
Std Dev	3.575

**Gaus mean : 27.8819**

**Gaus Width: 4.3077**



# B1L103S, U16-ch106, adc1

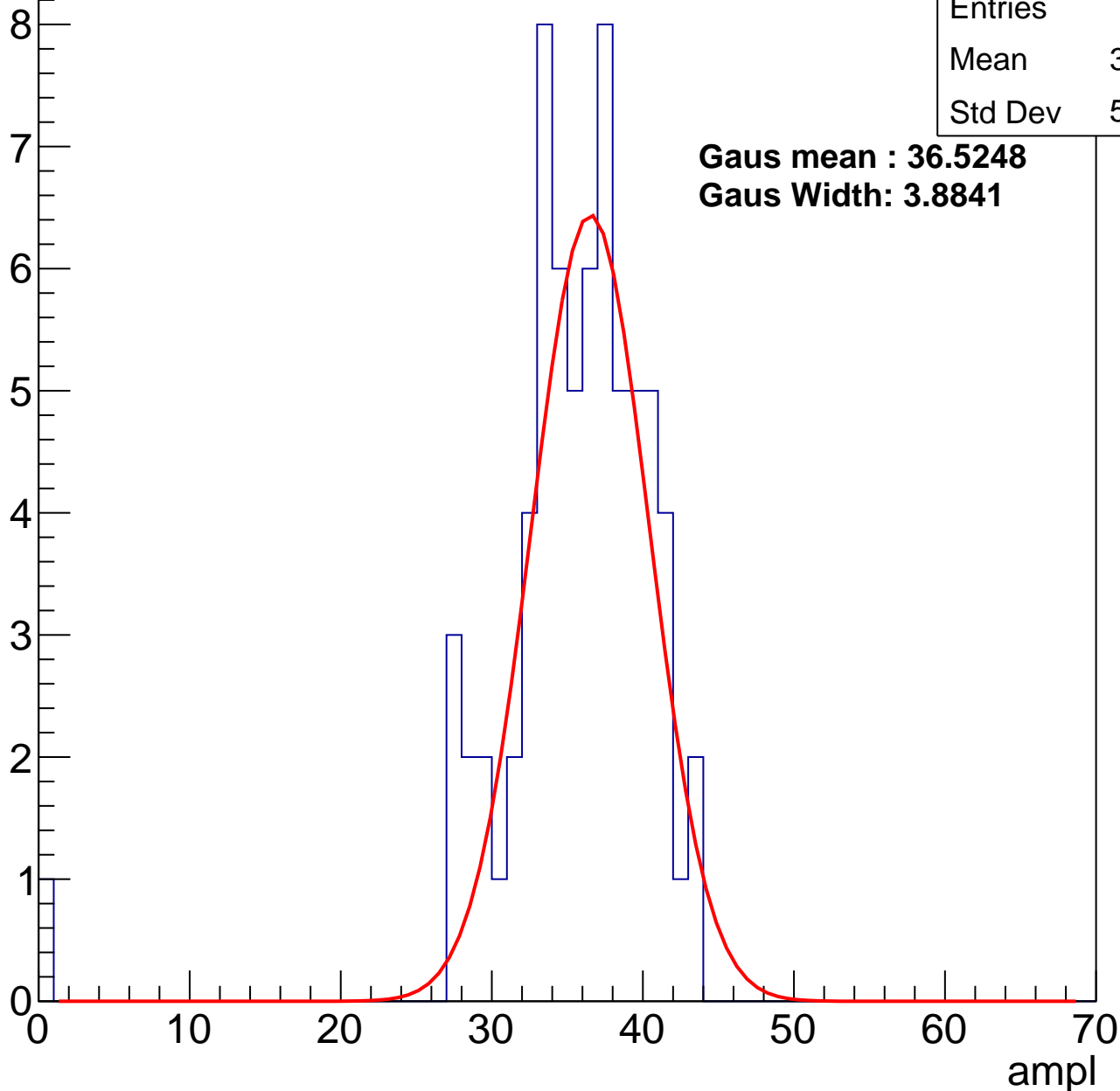
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	34.96
Std Dev	5.766

**Gaus mean : 36.5248**

**Gaus Width: 3.8841**



# B1L103S, U16-ch106, adc2

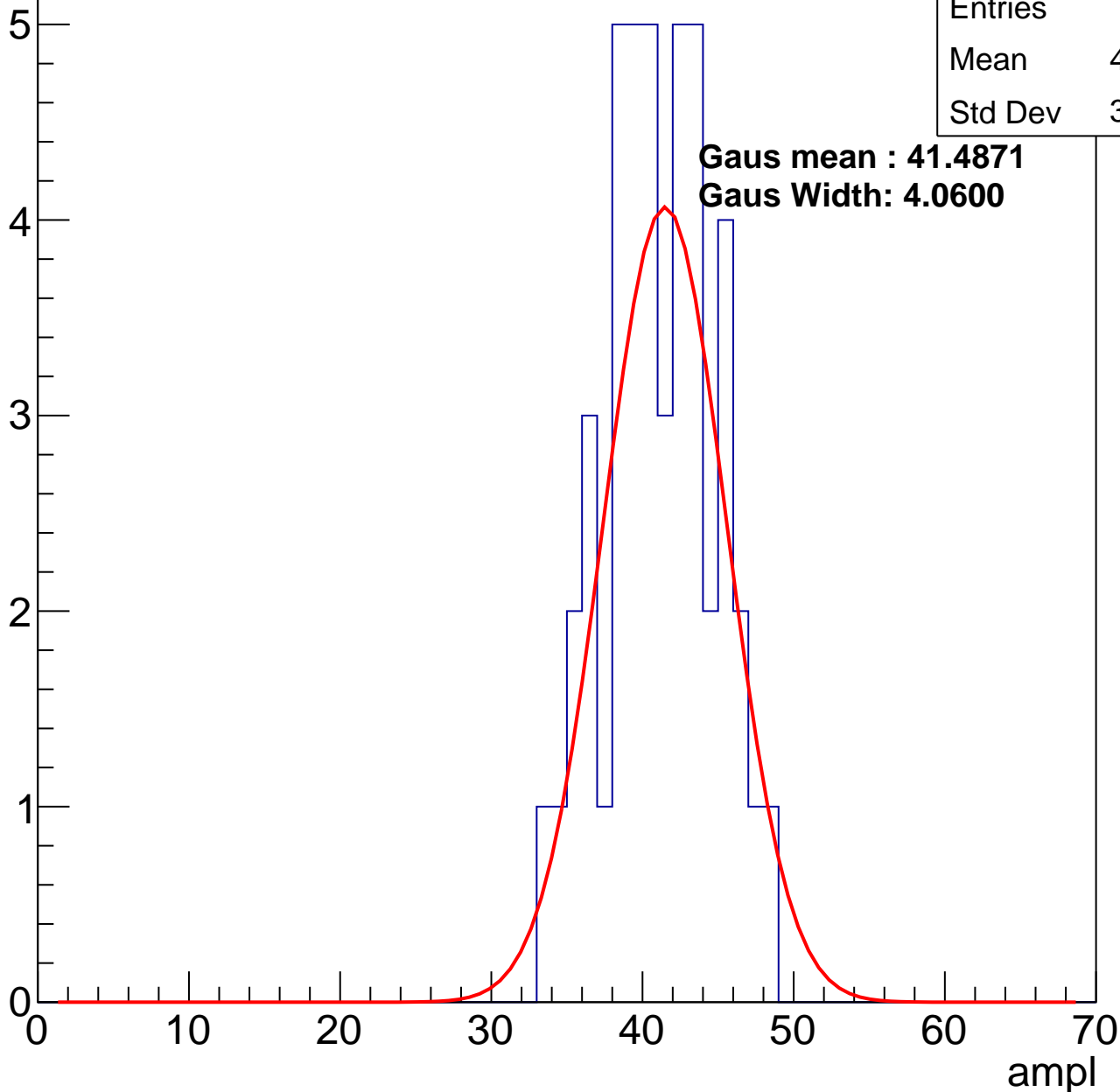
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	40.65
Std Dev	3.558

**Gaus mean : 41.4871**

**Gaus Width: 4.0600**

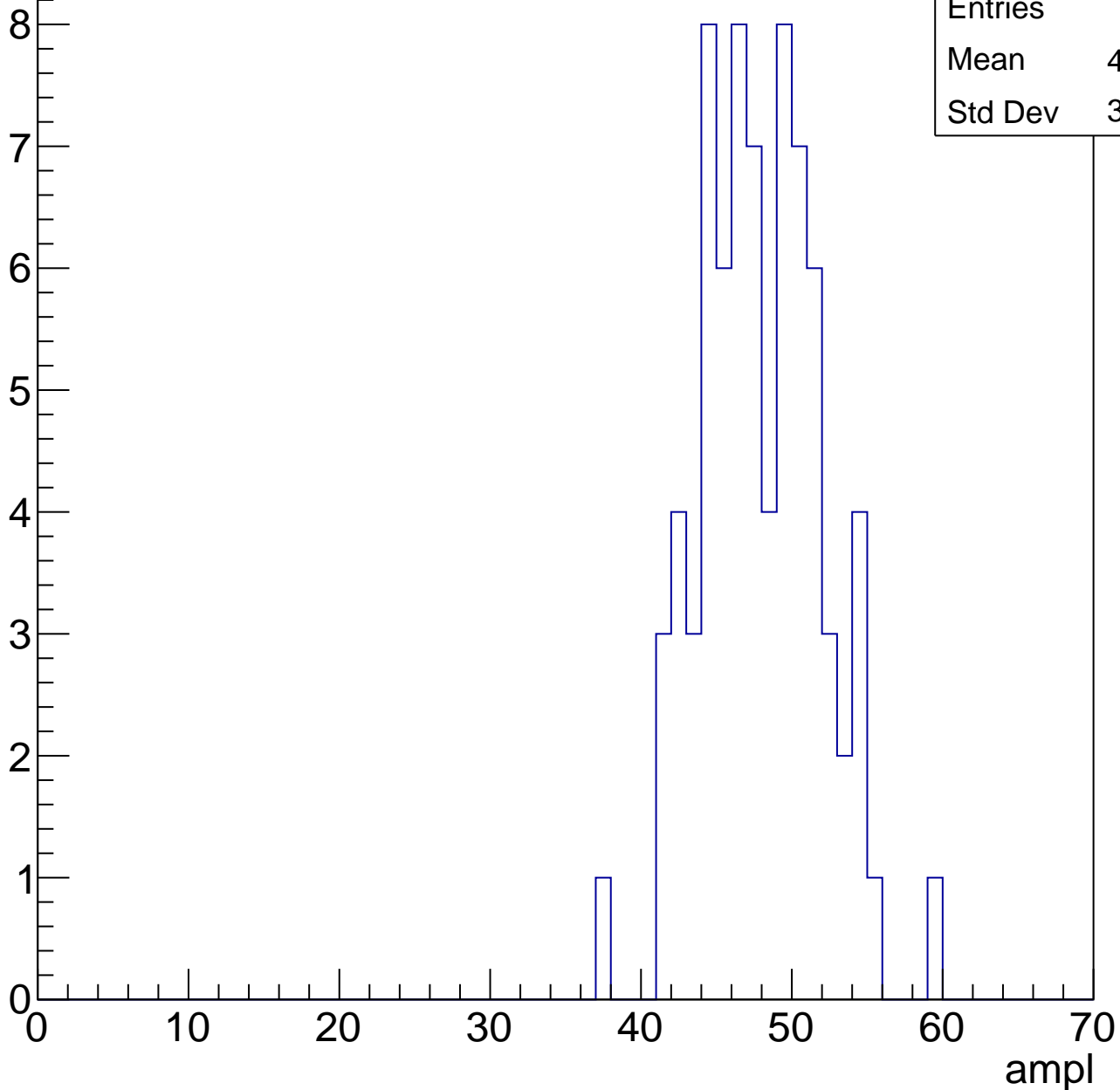


# B1L103S, U16-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	47.47
Std Dev	3.955

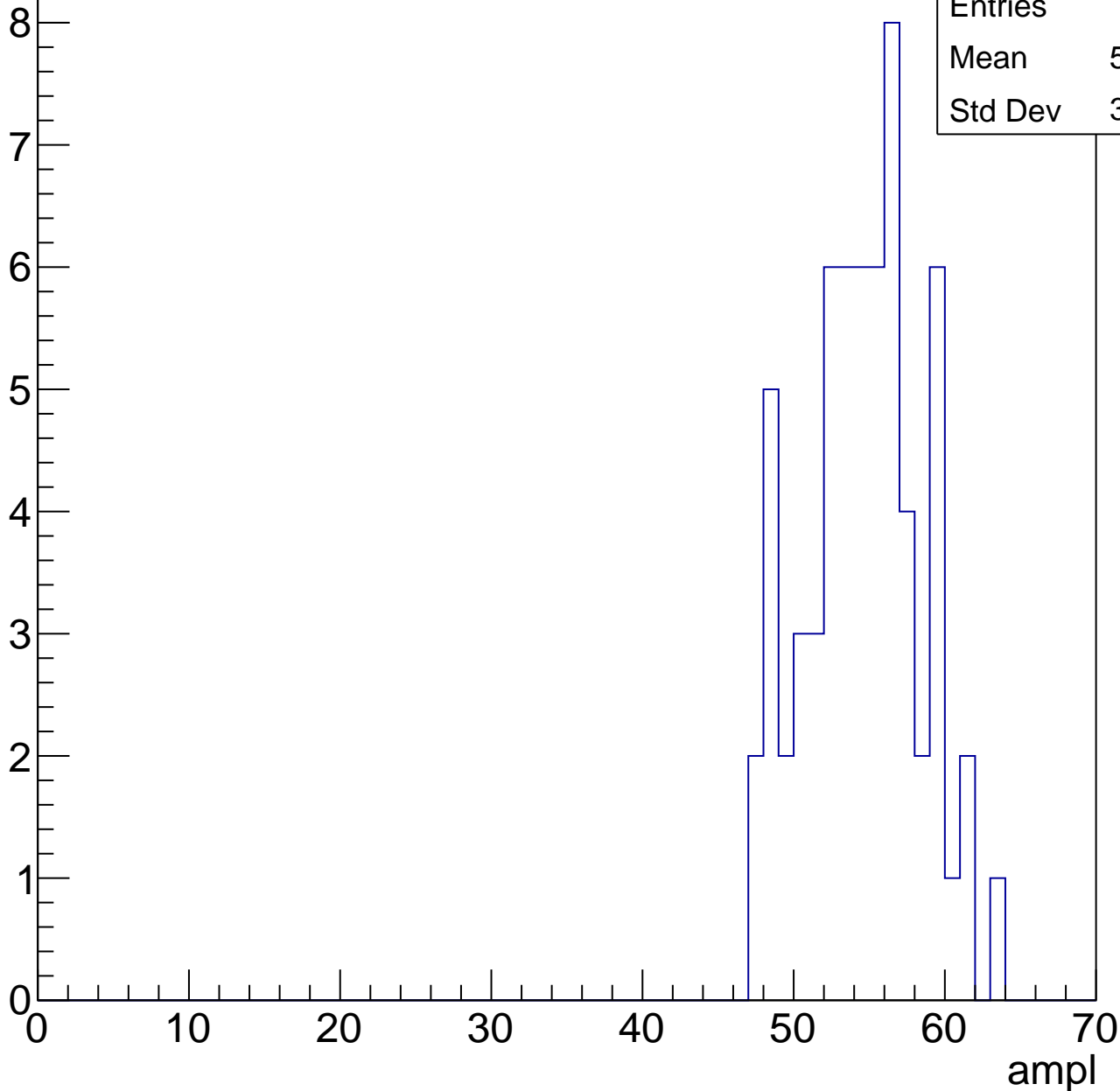


# B1L103S, U16-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	54.13
Std Dev	3.786

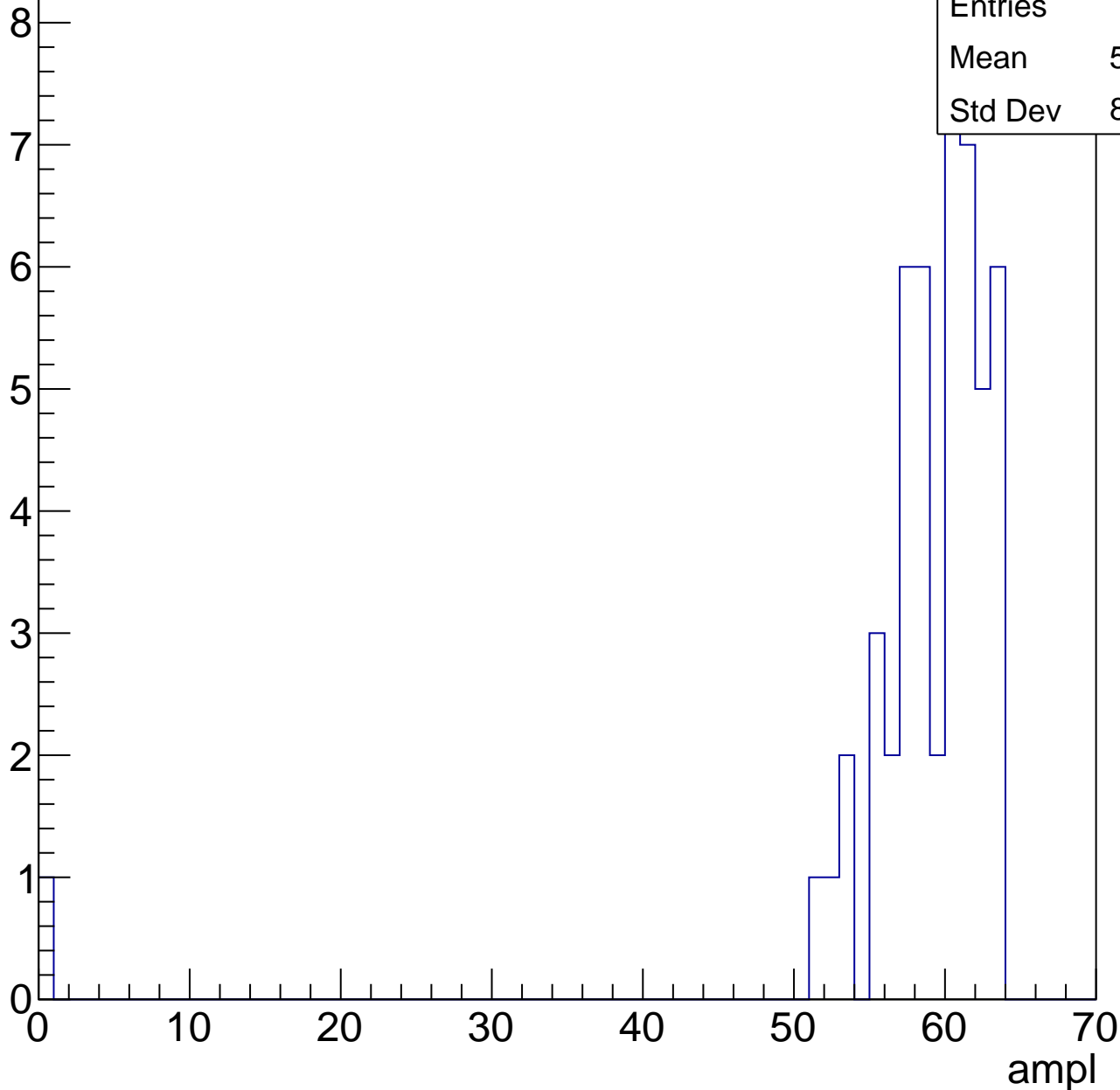


# B1L103S, U16-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	57.78
Std Dev	8.792

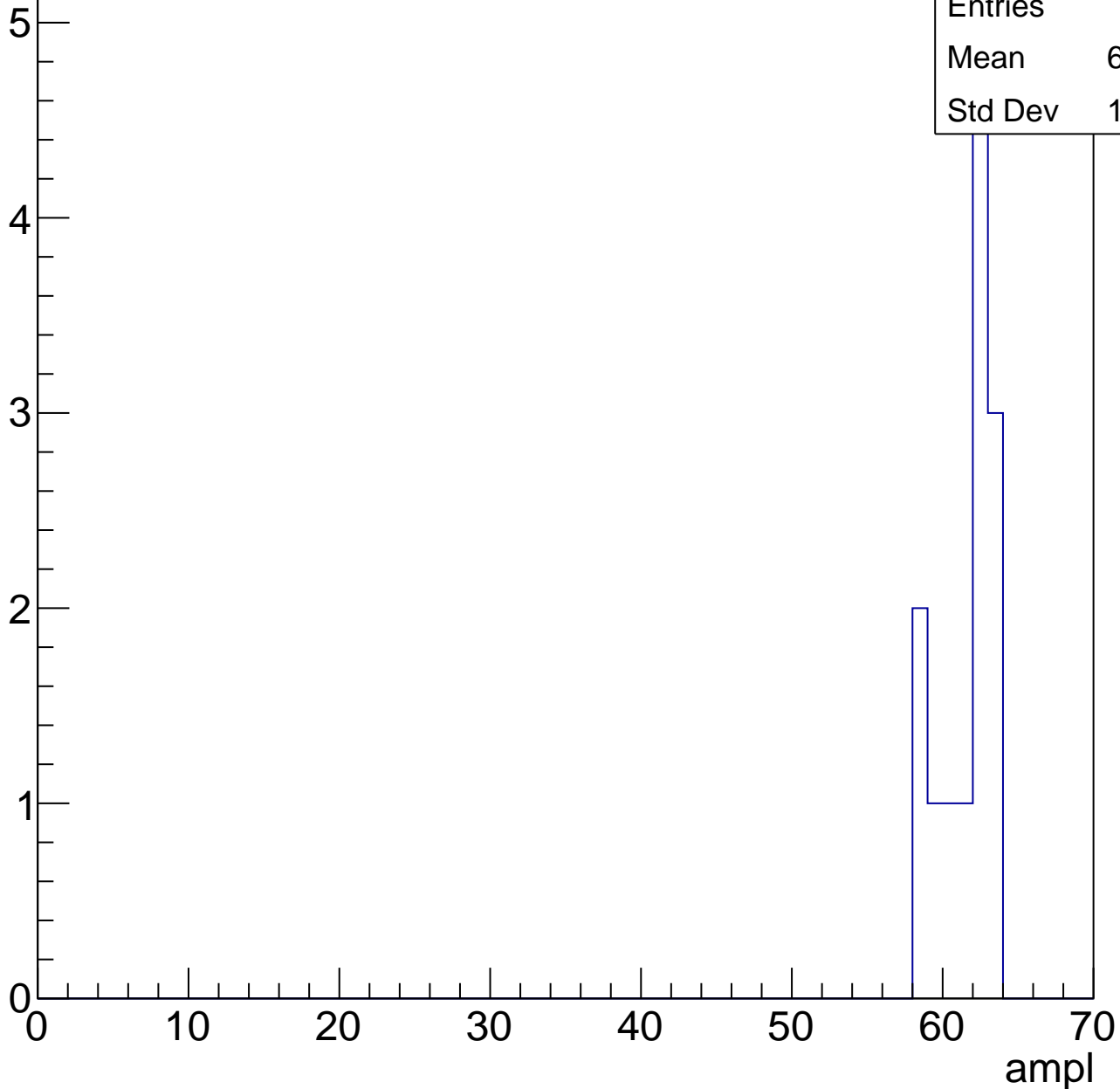


# B1L103S, U16-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	13
Mean	61.15
Std Dev	1.747





# B1L103S, U16-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch107, adc0

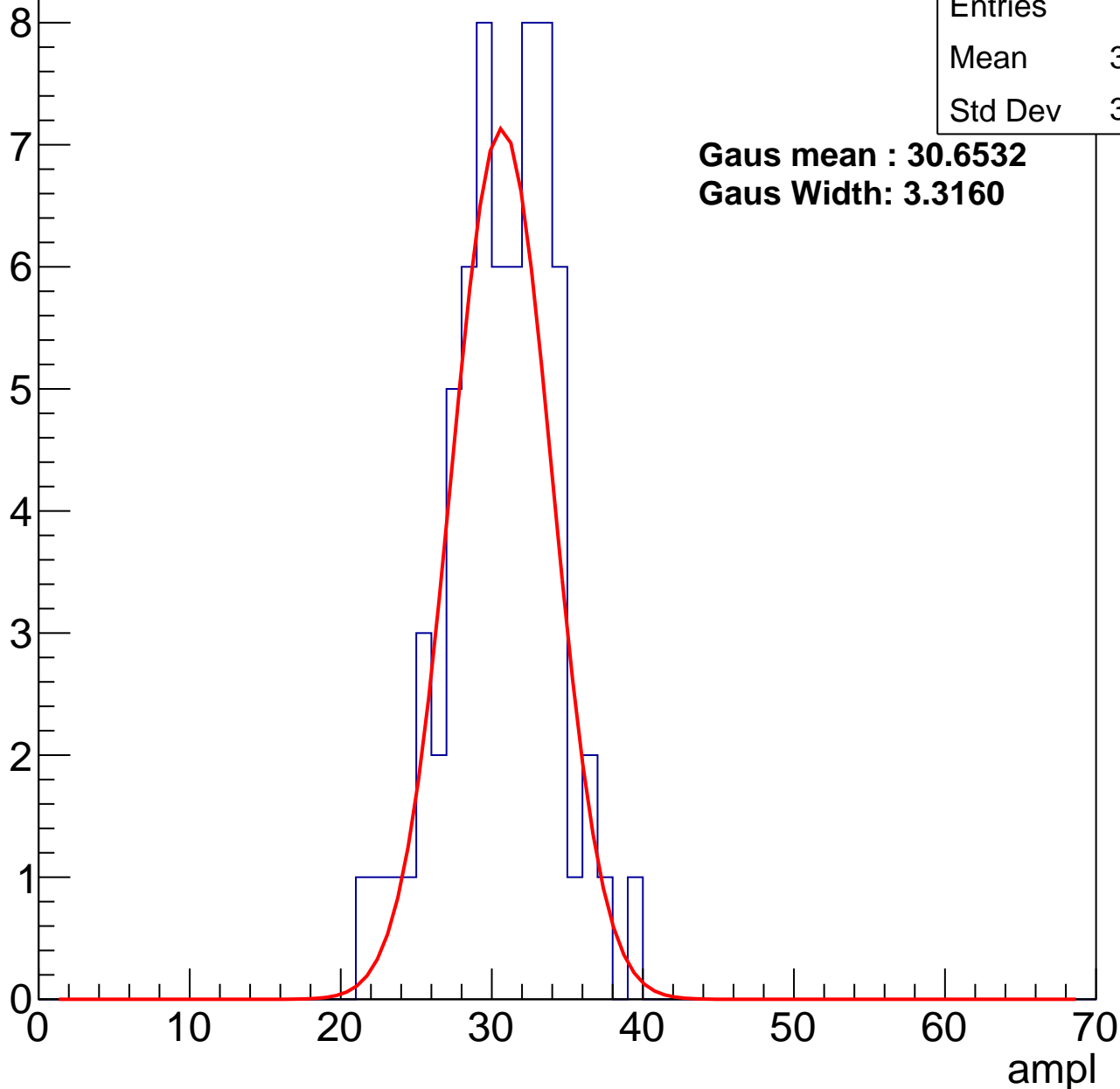
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	30.22
Std Dev	3.548

**Gaus mean : 30.6532**

**Gaus Width: 3.3160**



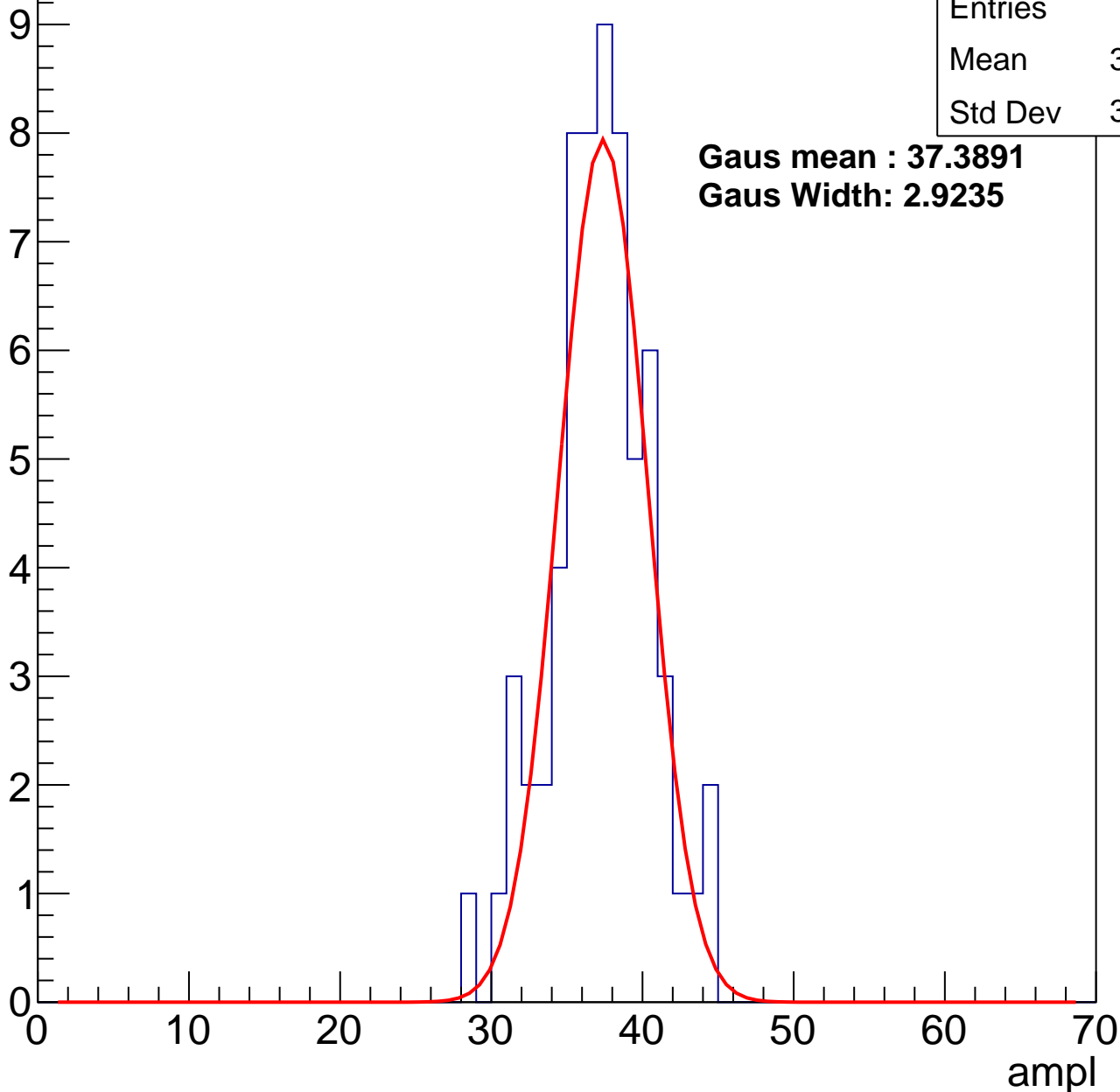
# B1L103S, U16-ch107, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	36.77
Std Dev	3.263

**Gaus mean : 37.3891**  
**Gaus Width: 2.9235**



# B1L103S, U16-ch107, adc2

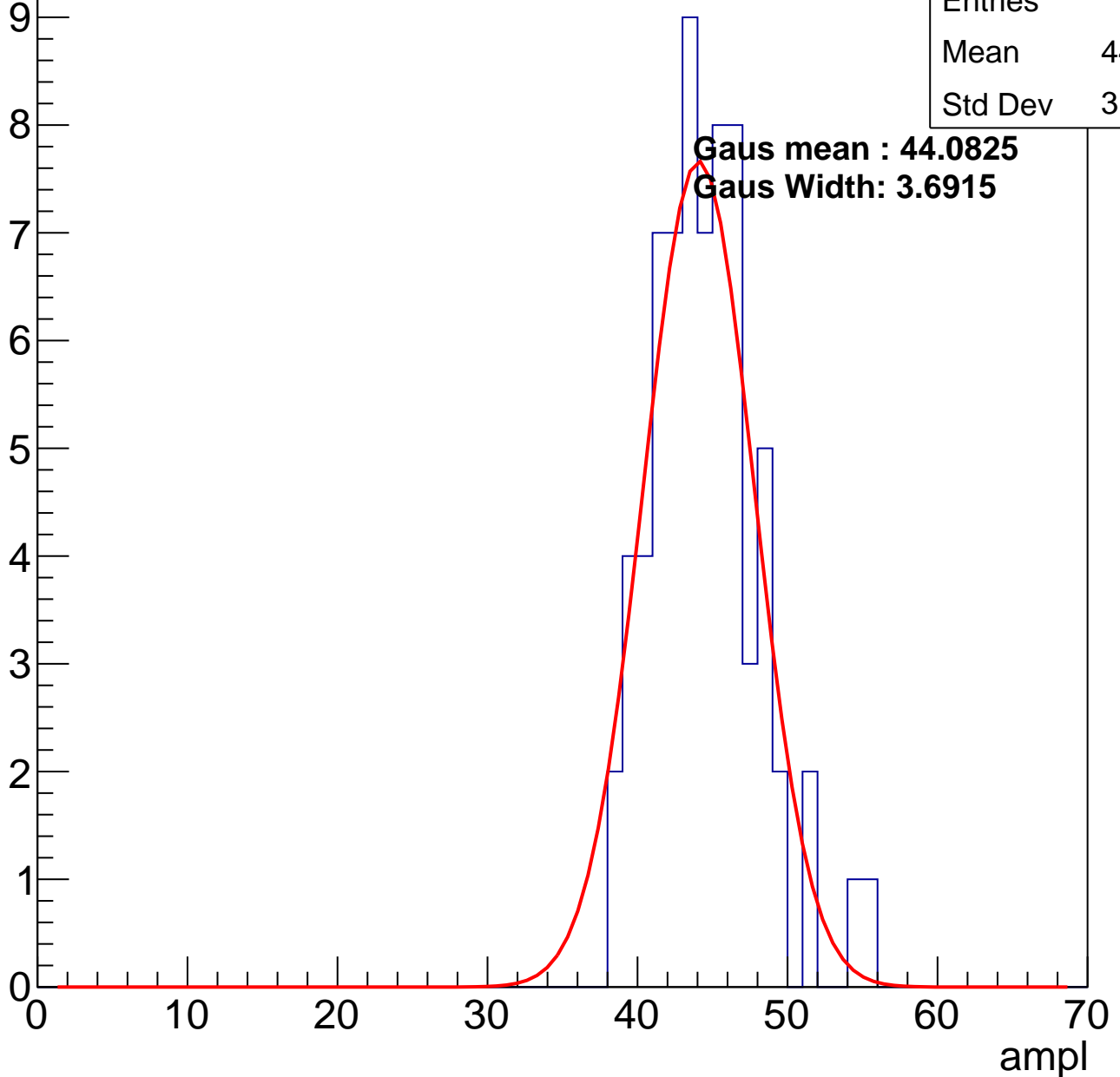
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	44.09
Std Dev	3.488

**Gaus mean : 44.0825**

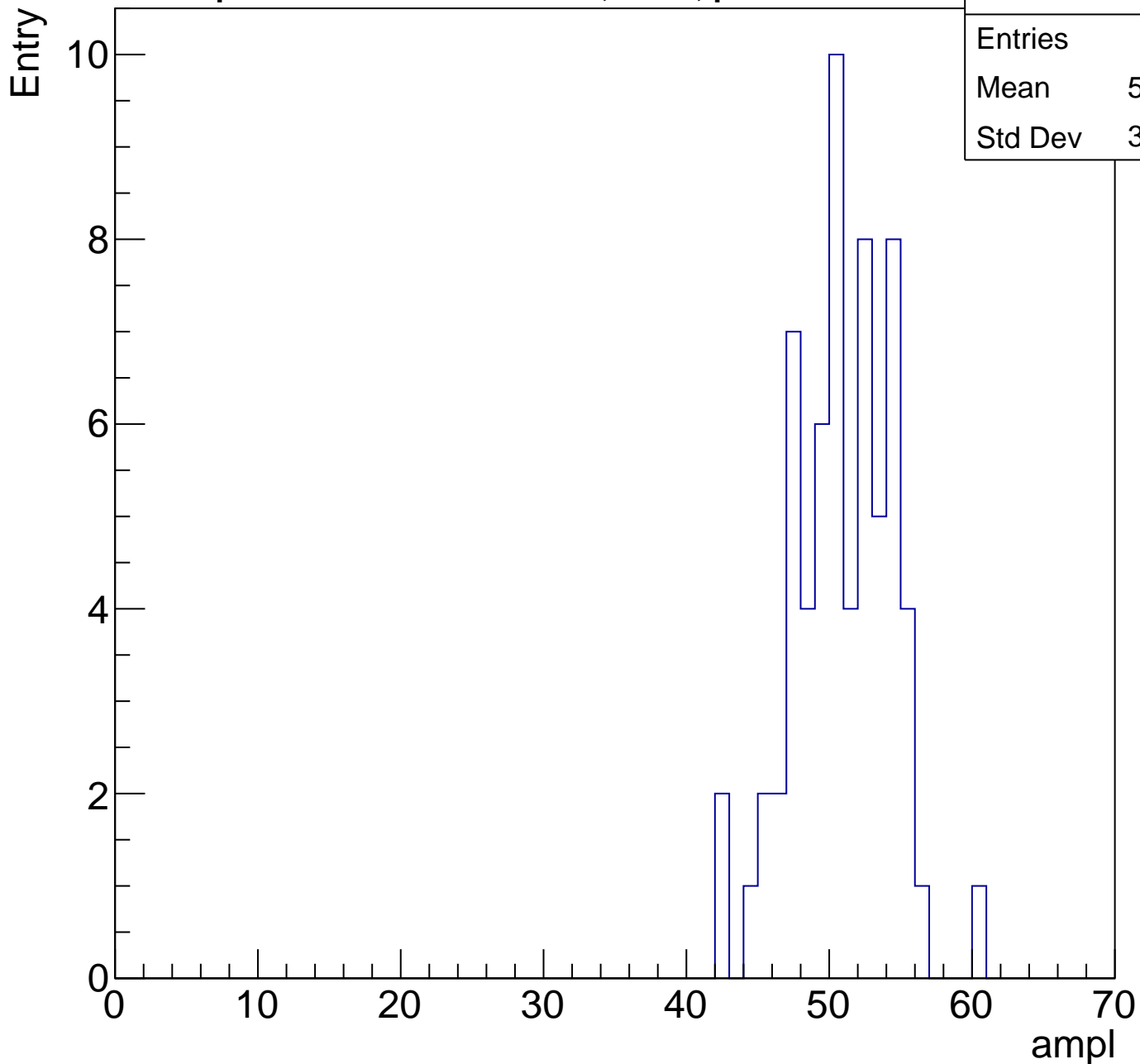
**Gaus Width: 3.6915**



# B1L103S, U16-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

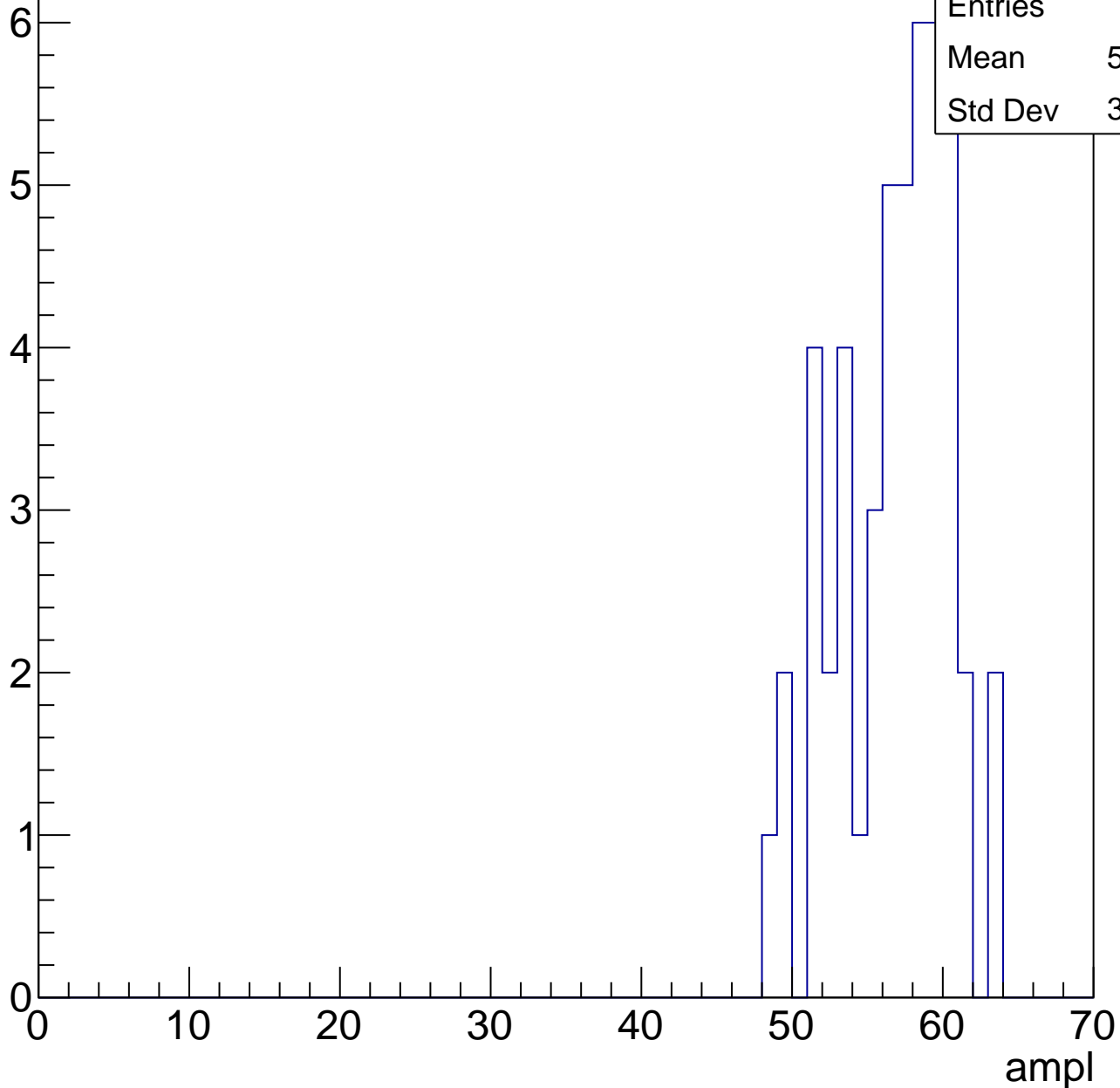
Entries	65
Mean	50.43
Std Dev	3.428



# B1L103S, U16-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



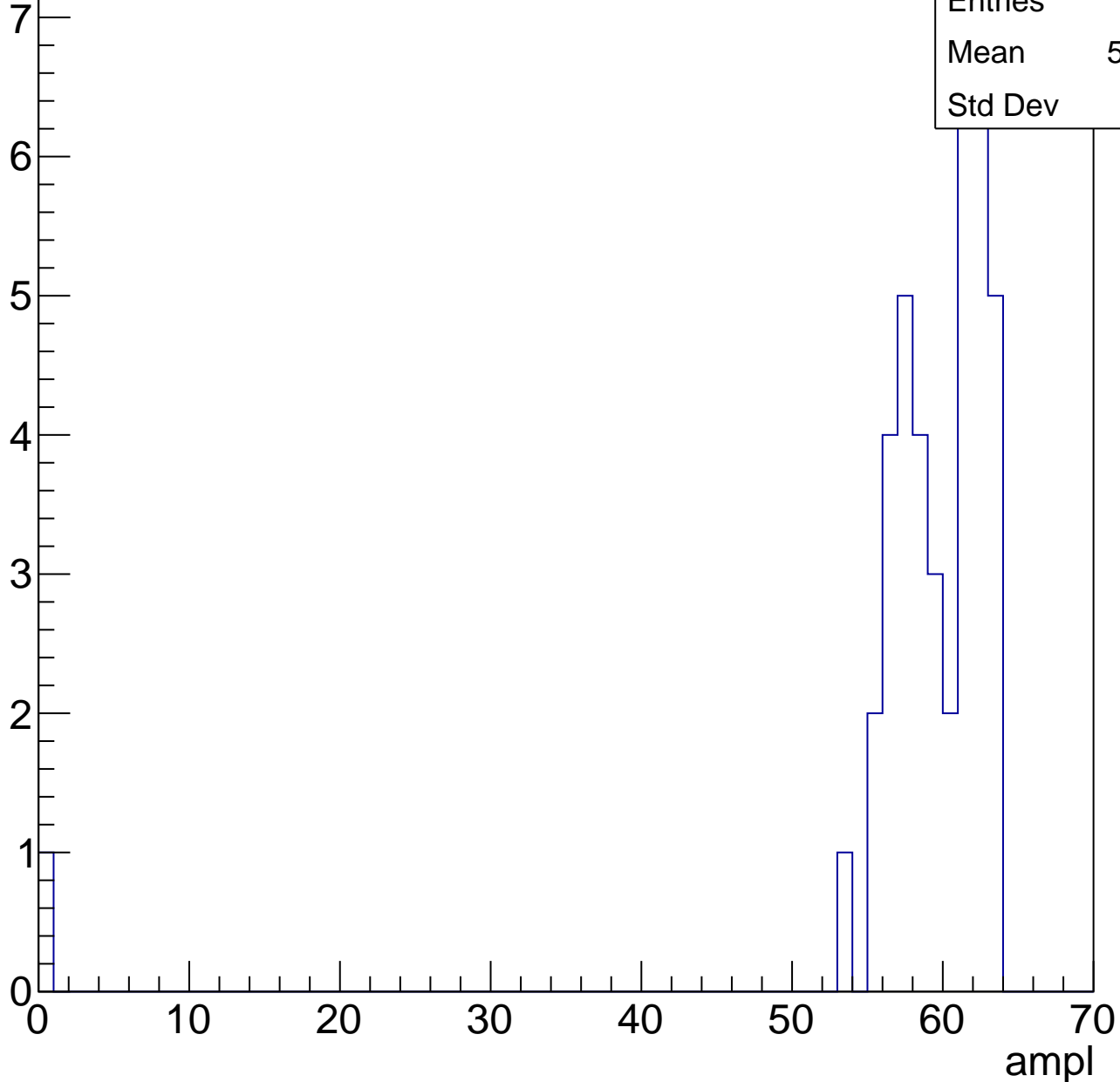
Entries	49
Mean	56.33
Std Dev	3.667

# B1L103S, U16-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

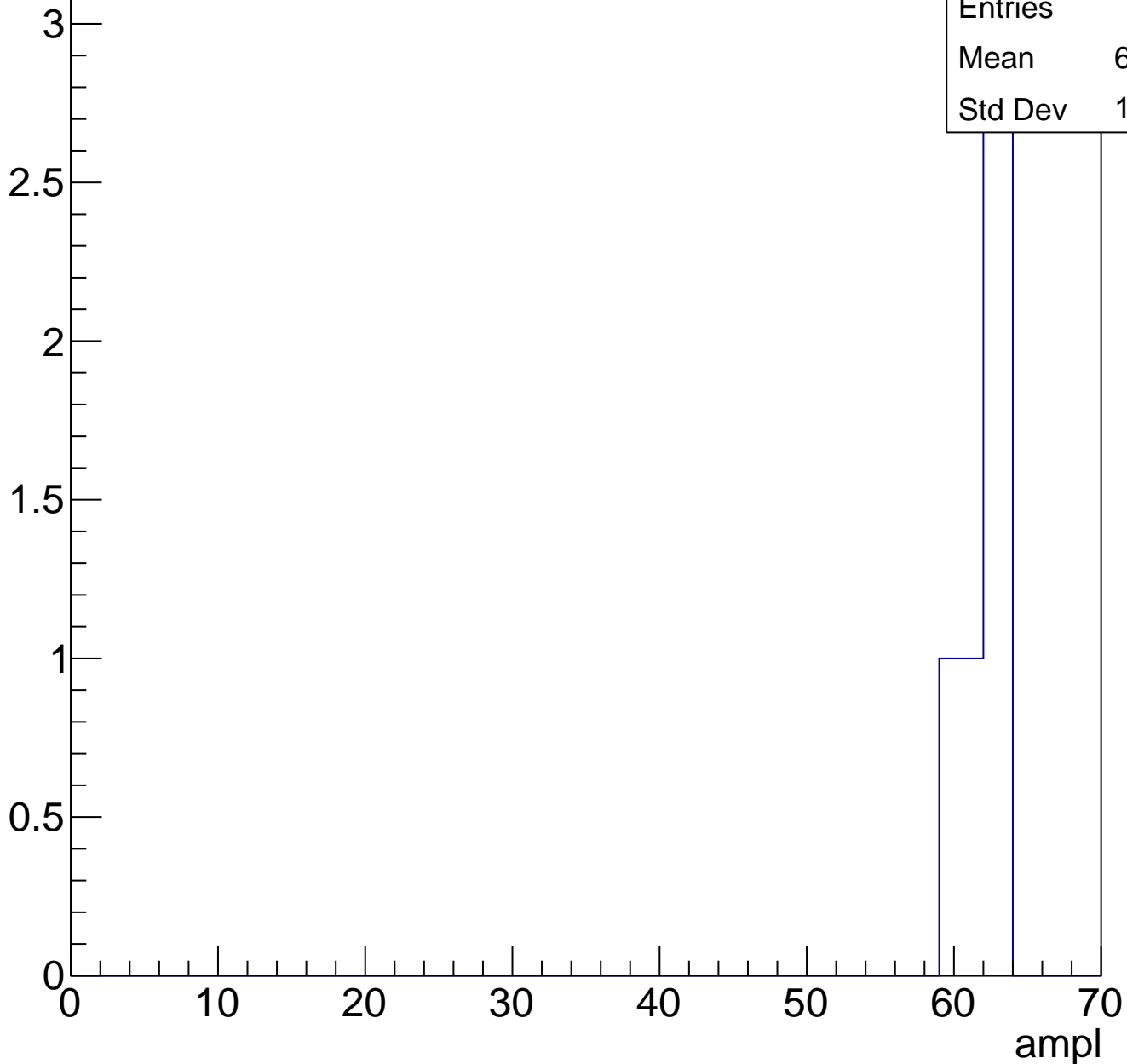
Entries	41
Mean	57.98
Std Dev	9.55



# B1L103S, U16-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U16-ch108, adc0

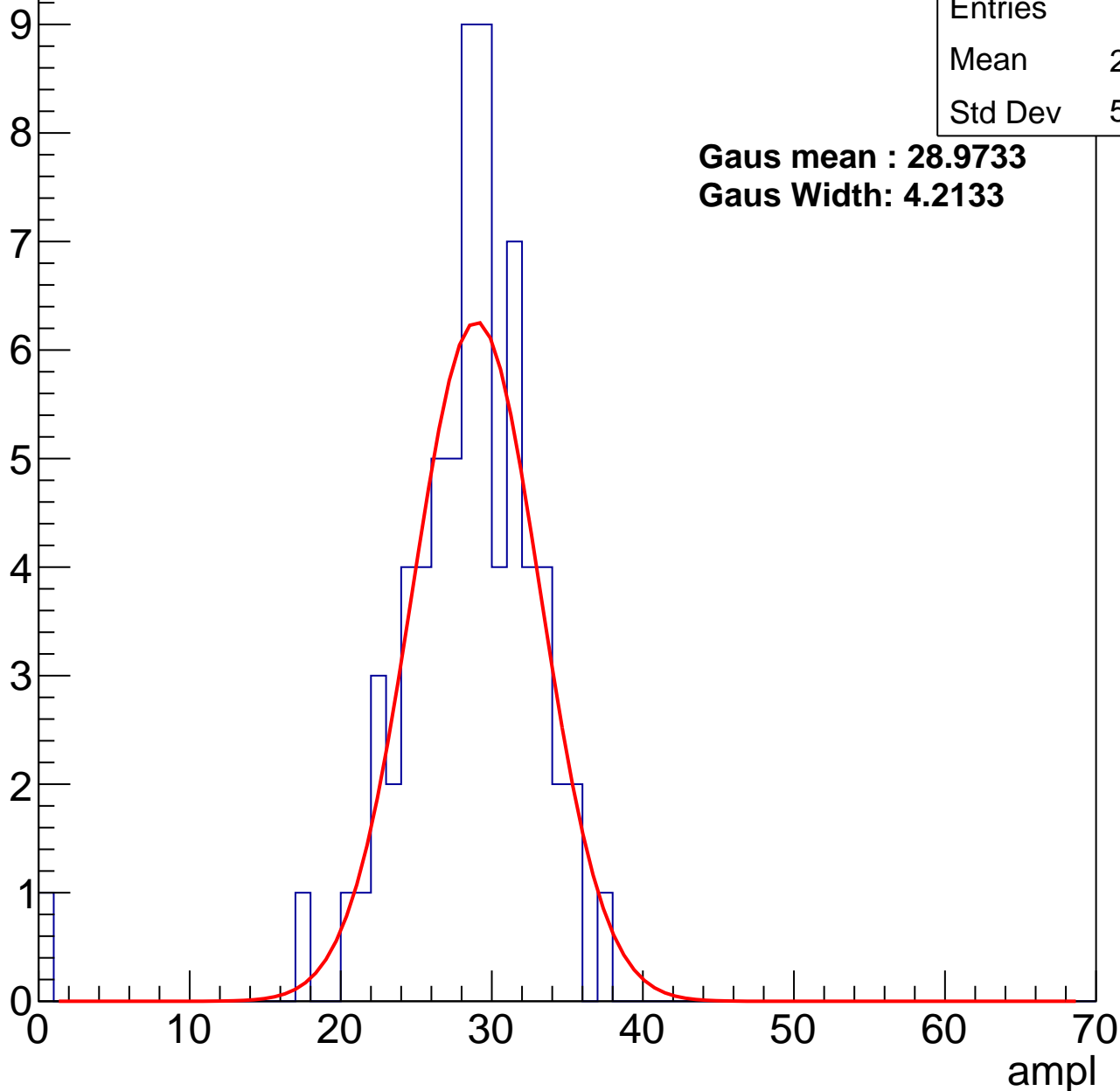
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	27.77
Std Dev	5.108

**Gaus mean : 28.9733**

**Gaus Width: 4.2133**



# B1L103S, U16-ch108, adc1

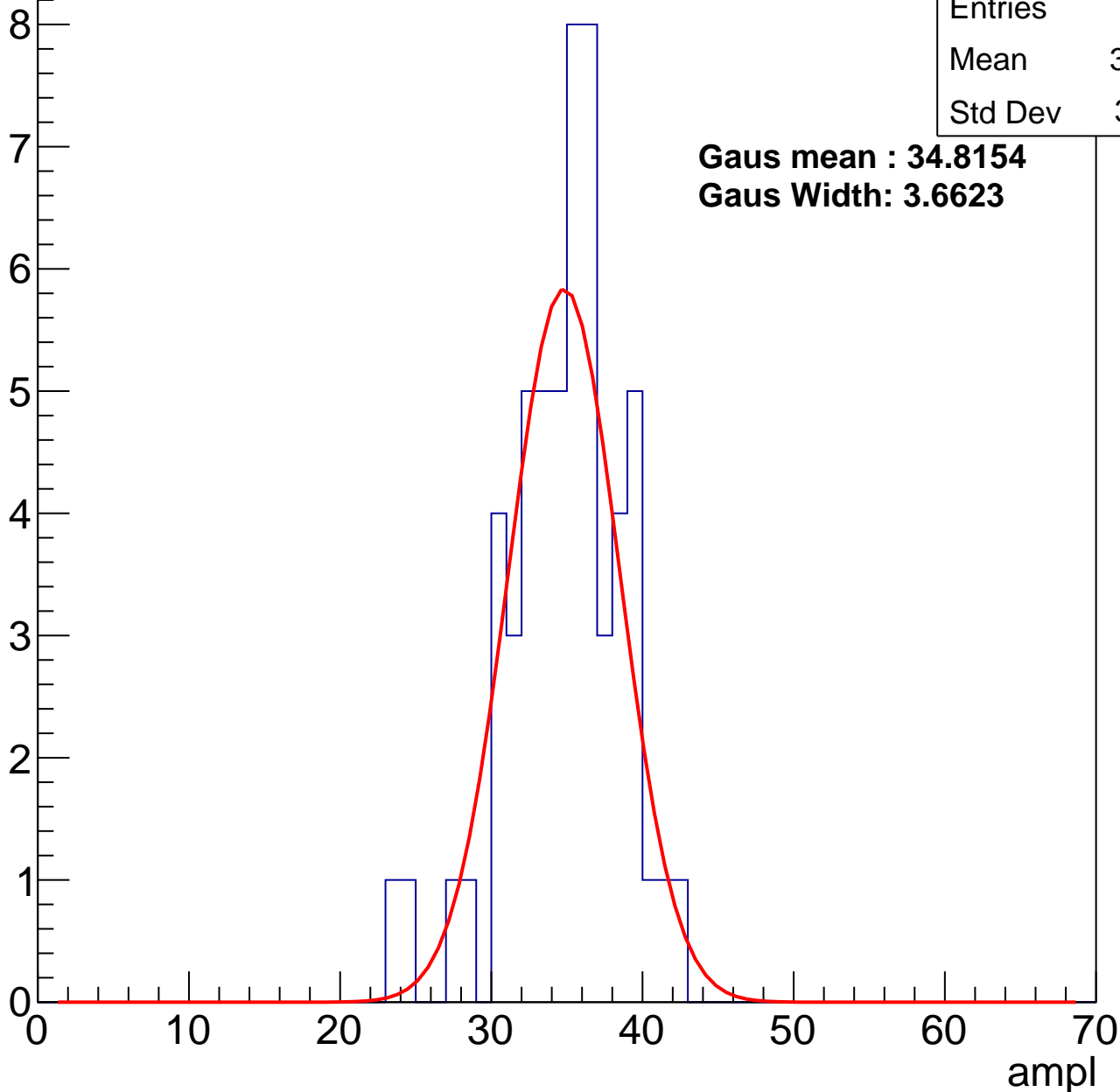
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	34.37
Std Dev	3.791

**Gaus mean : 34.8154**

**Gaus Width: 3.6623**



# B1L103S, U16-ch108, adc2

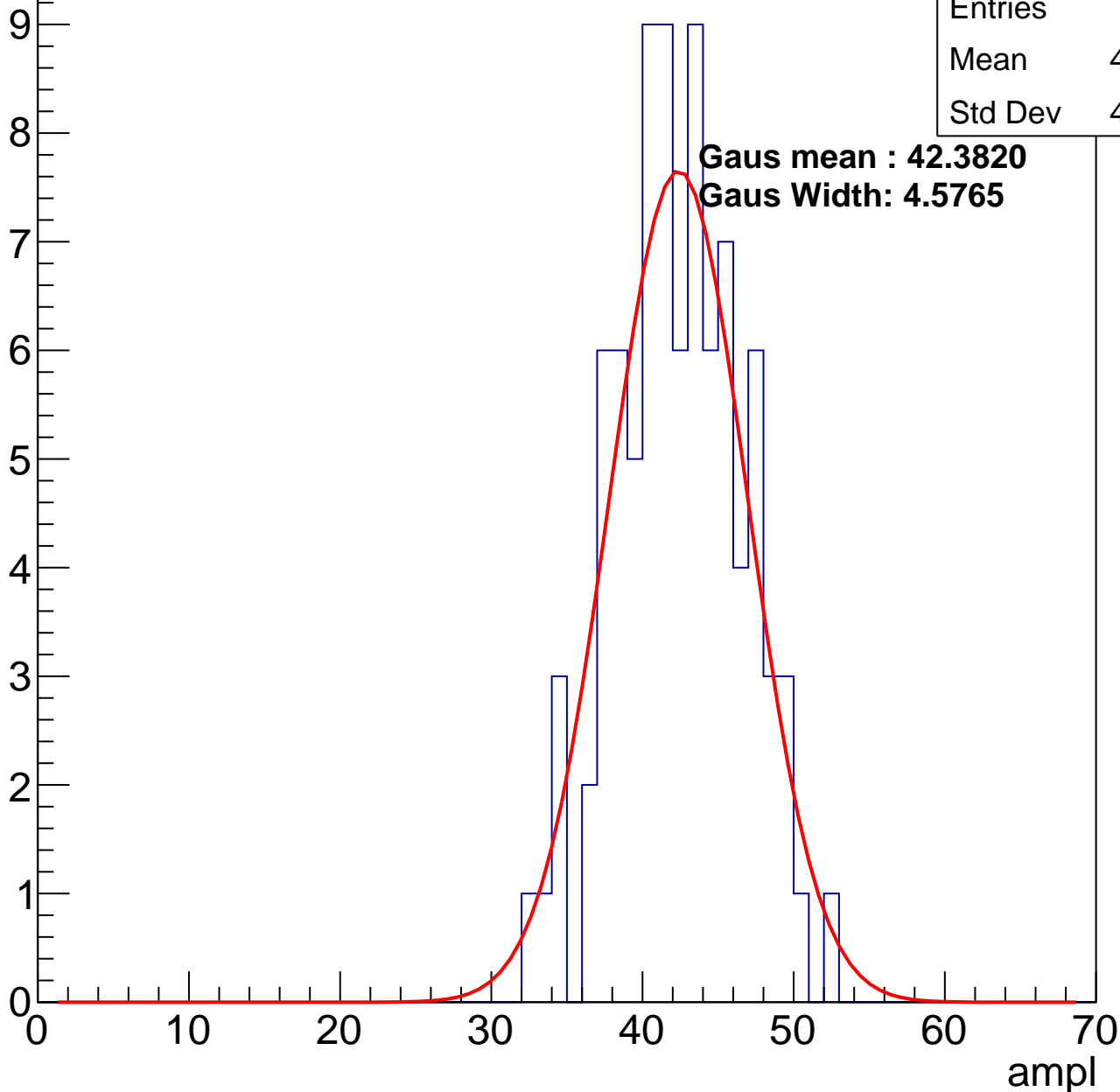
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	88
Mean	41.93
Std Dev	4.142

**Gaus mean : 42.3820**

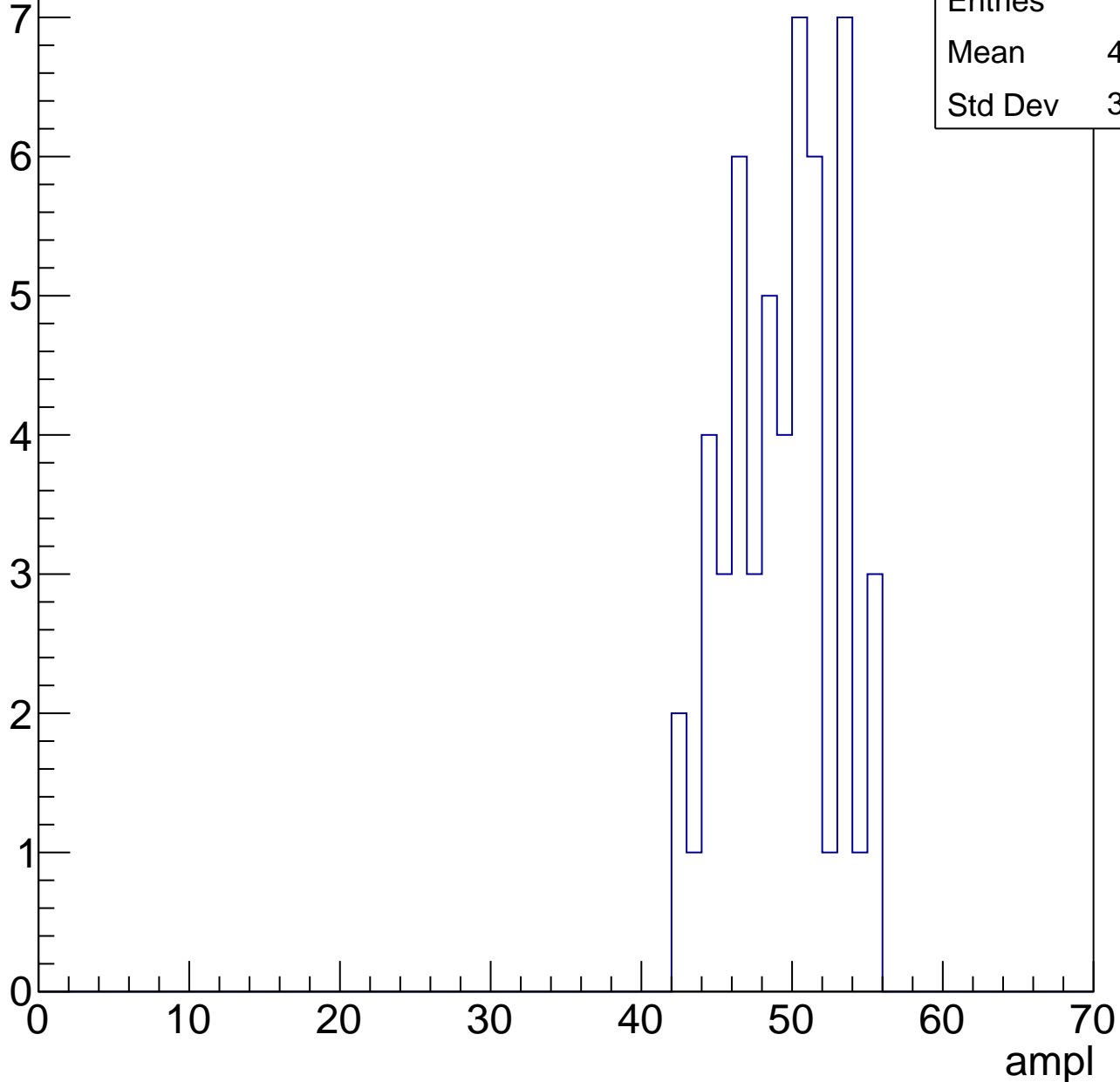
**Gaus Width: 4.5765**



# B1L103S, U16-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



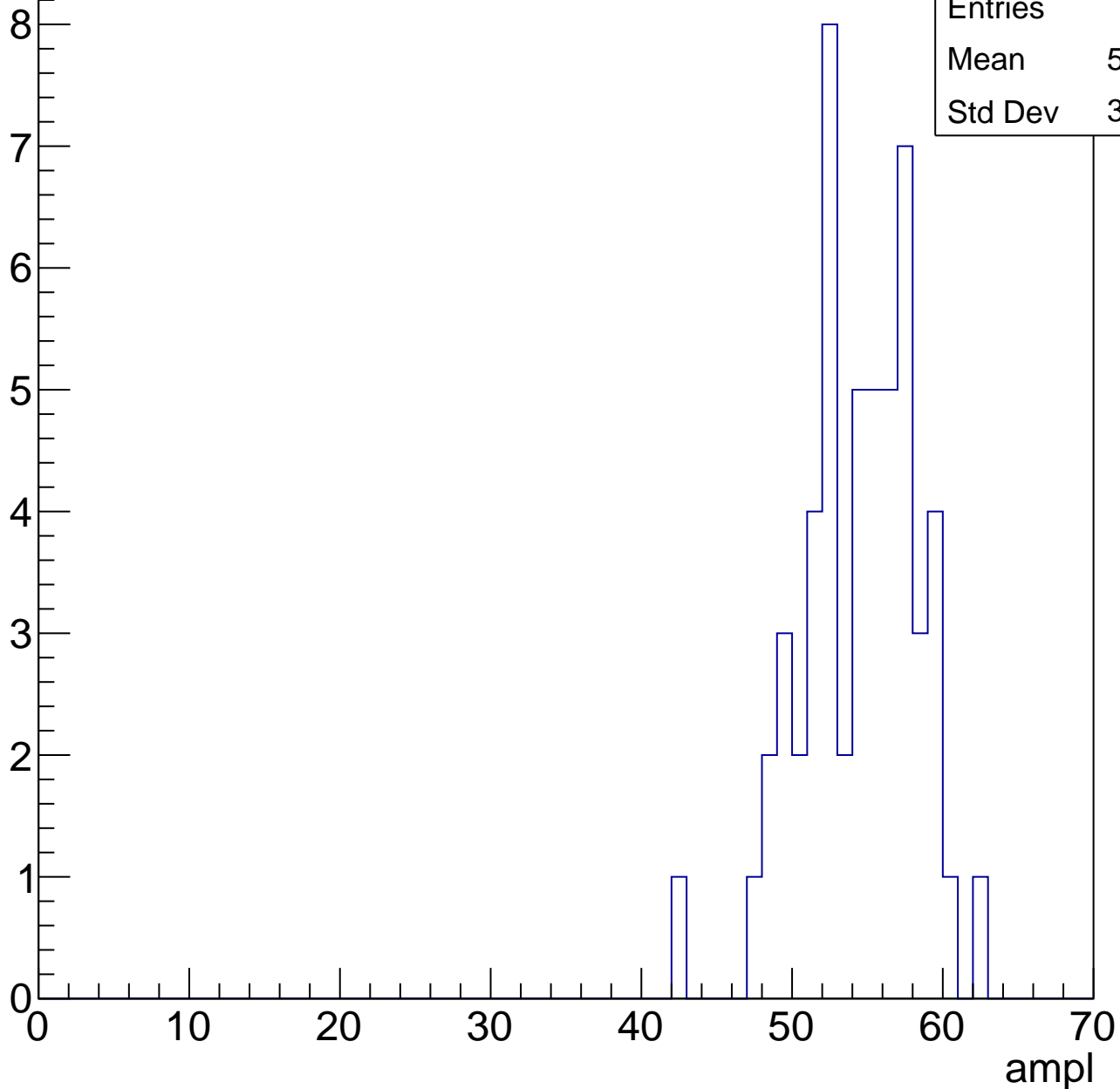
Entries	53
Mean	48.85
Std Dev	3.466

# B1L103S, U16-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	53.96
Std Dev	3.796

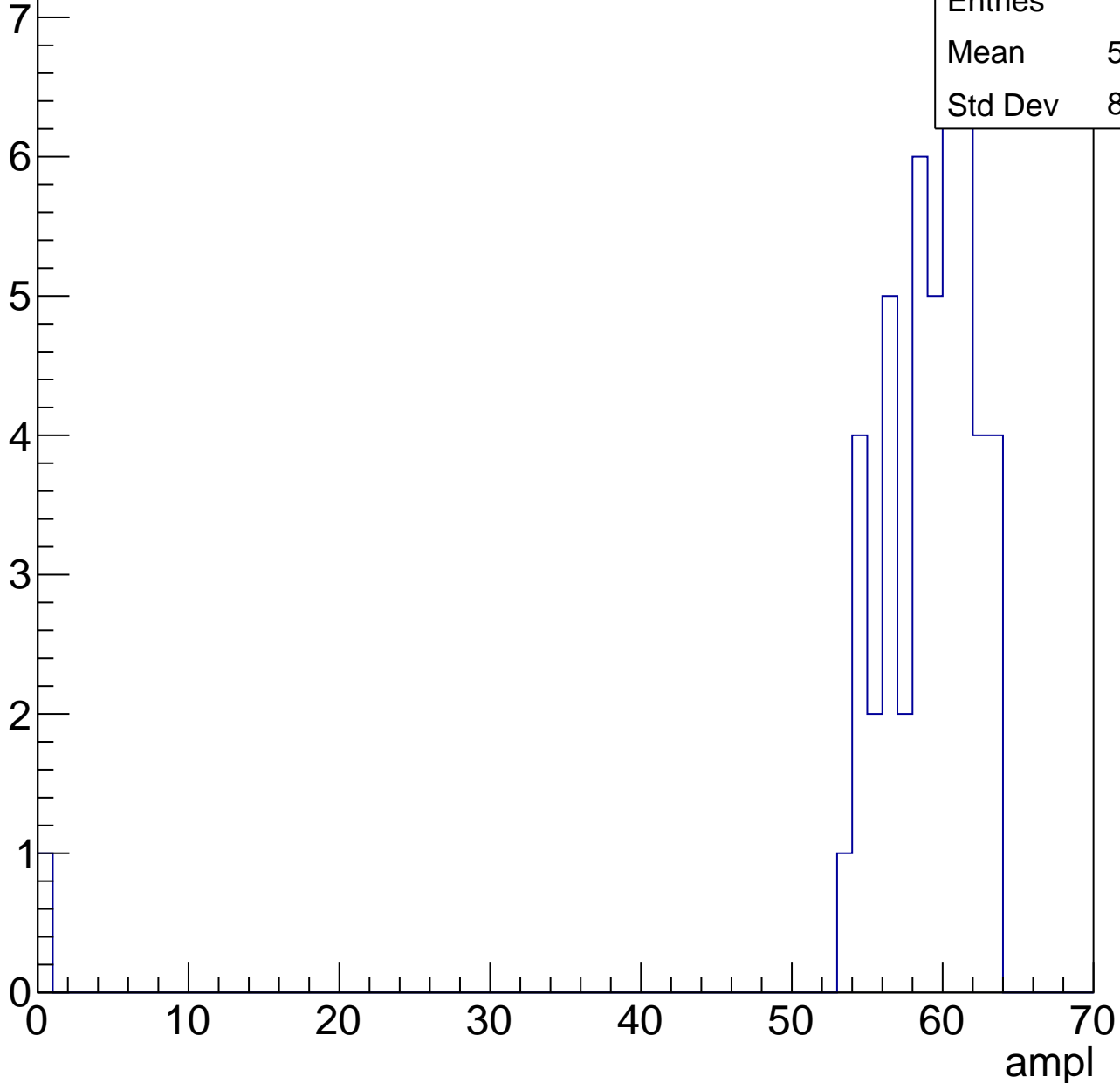


# B1L103S, U16-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	57.56
Std Dev	8.832

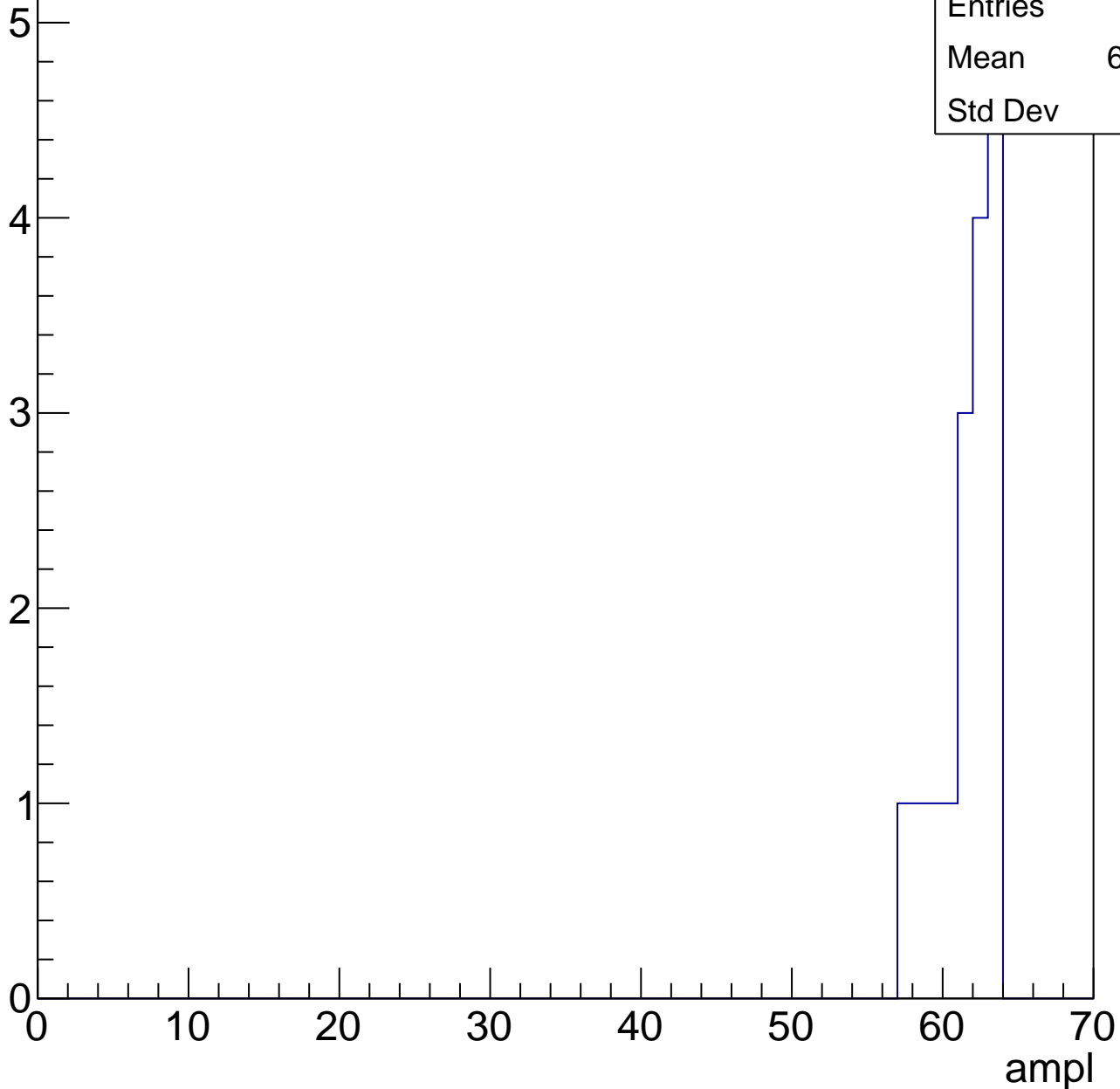


# B1L103S, U16-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	16
Mean	61.25
Std Dev	1.82

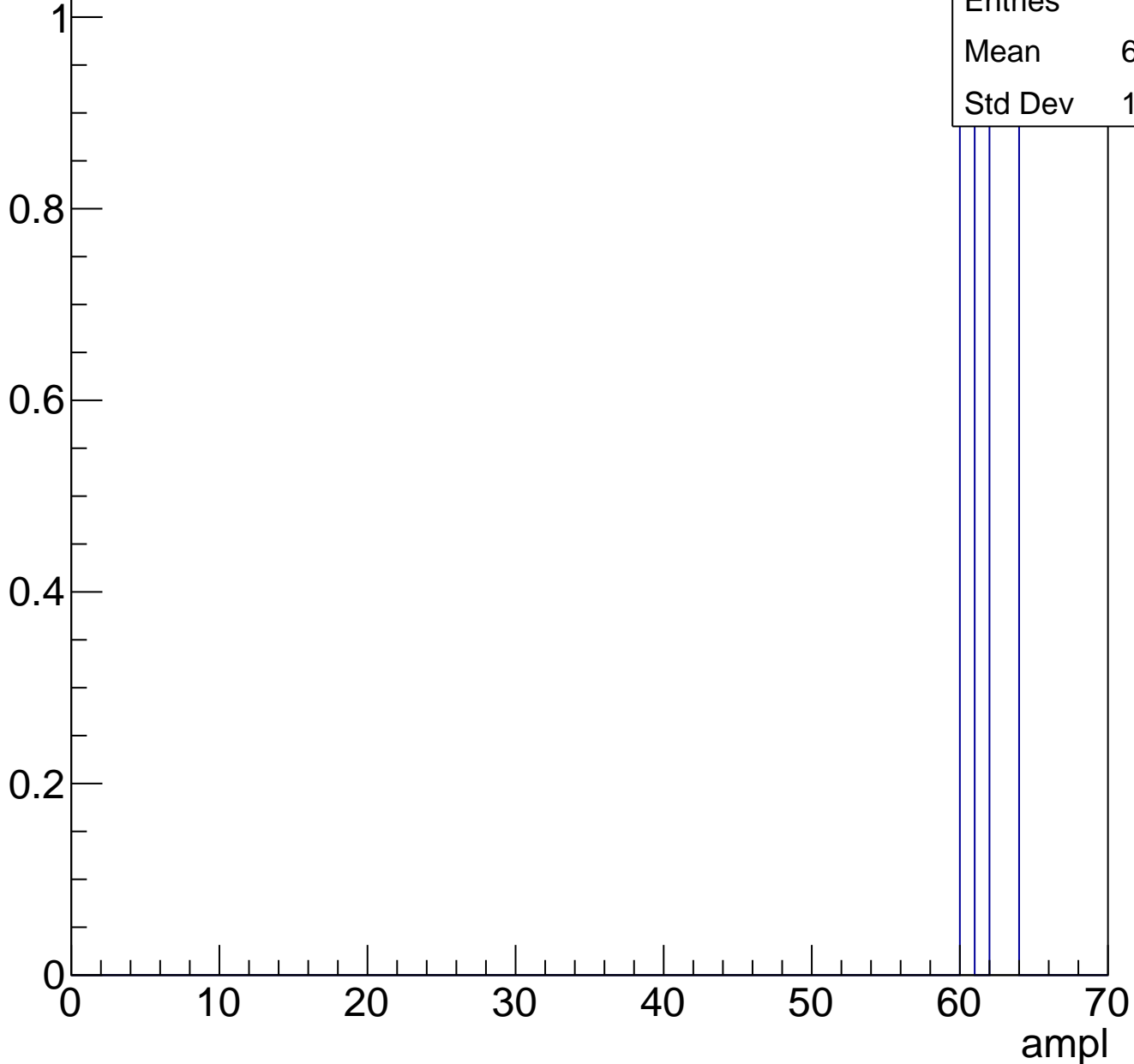




# B1L103S, U16-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch109, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	71
Mean	30.87
Std Dev	5.222

**Gaus mean : 31.4409**

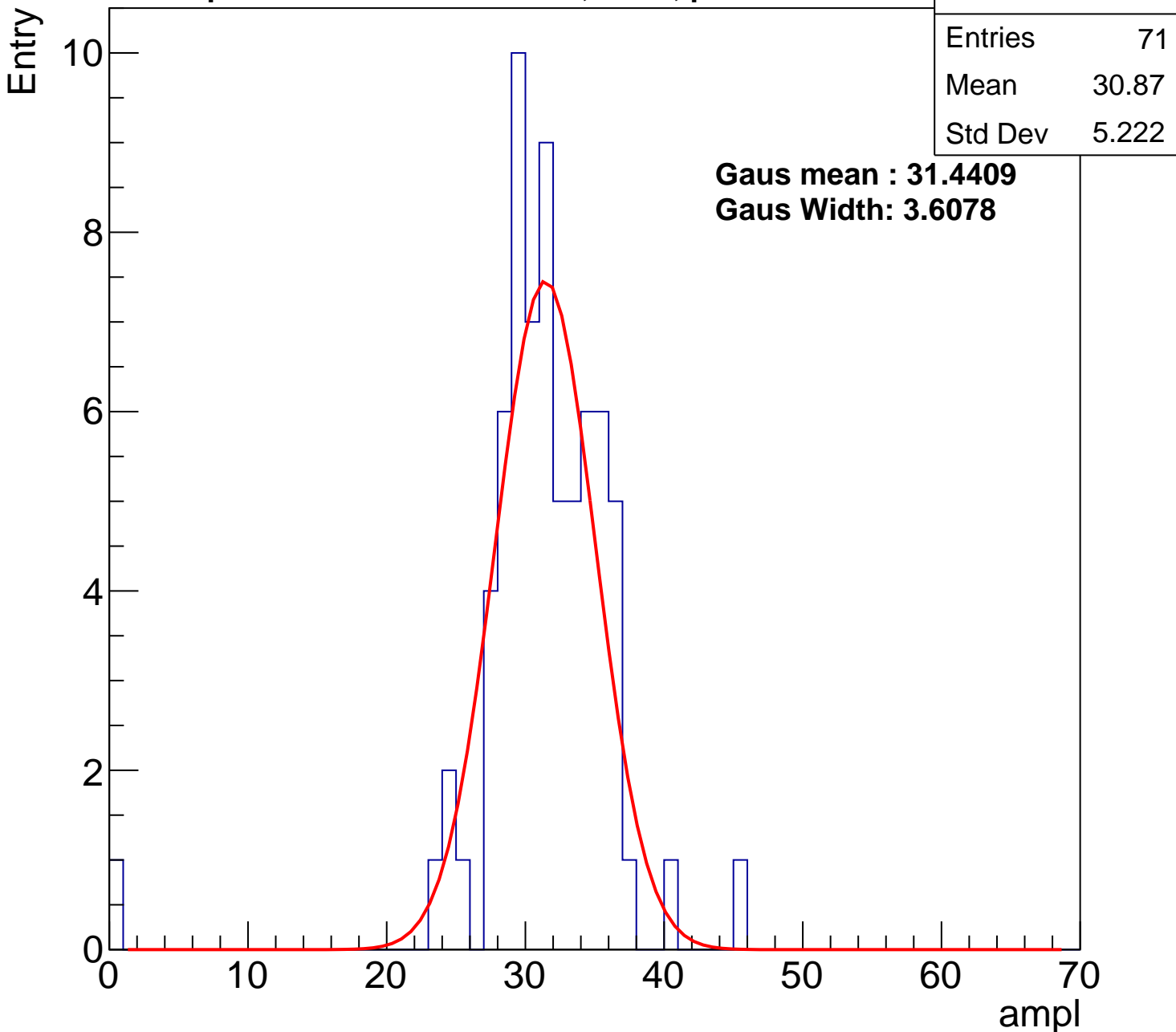
**Gaus Width: 3.6078**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U16-ch109, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	65
Mean	38.48
Std Dev	3.216

**Gaus mean : 38.8538**

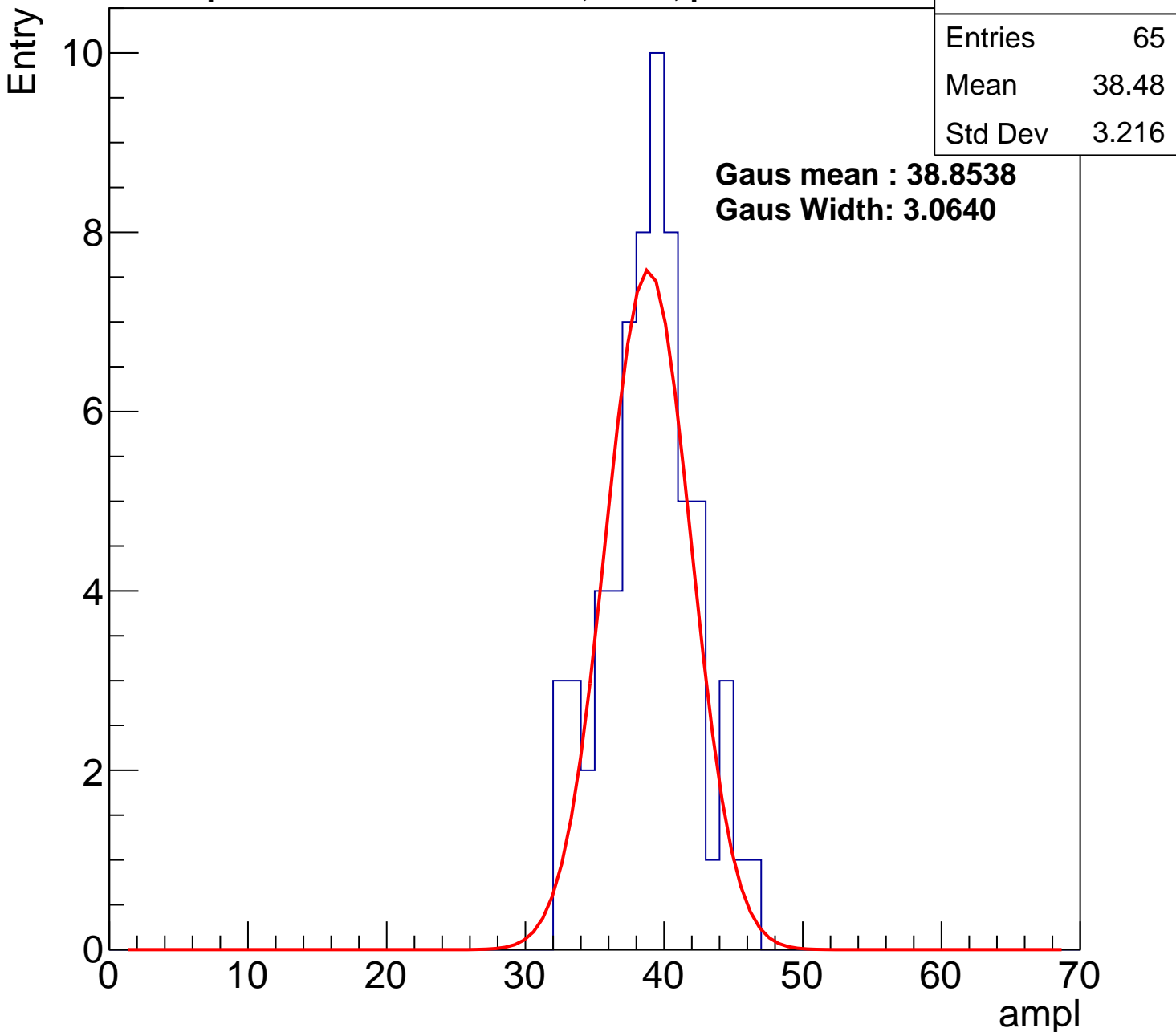
**Gaus Width: 3.0640**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U16-ch109, adc2

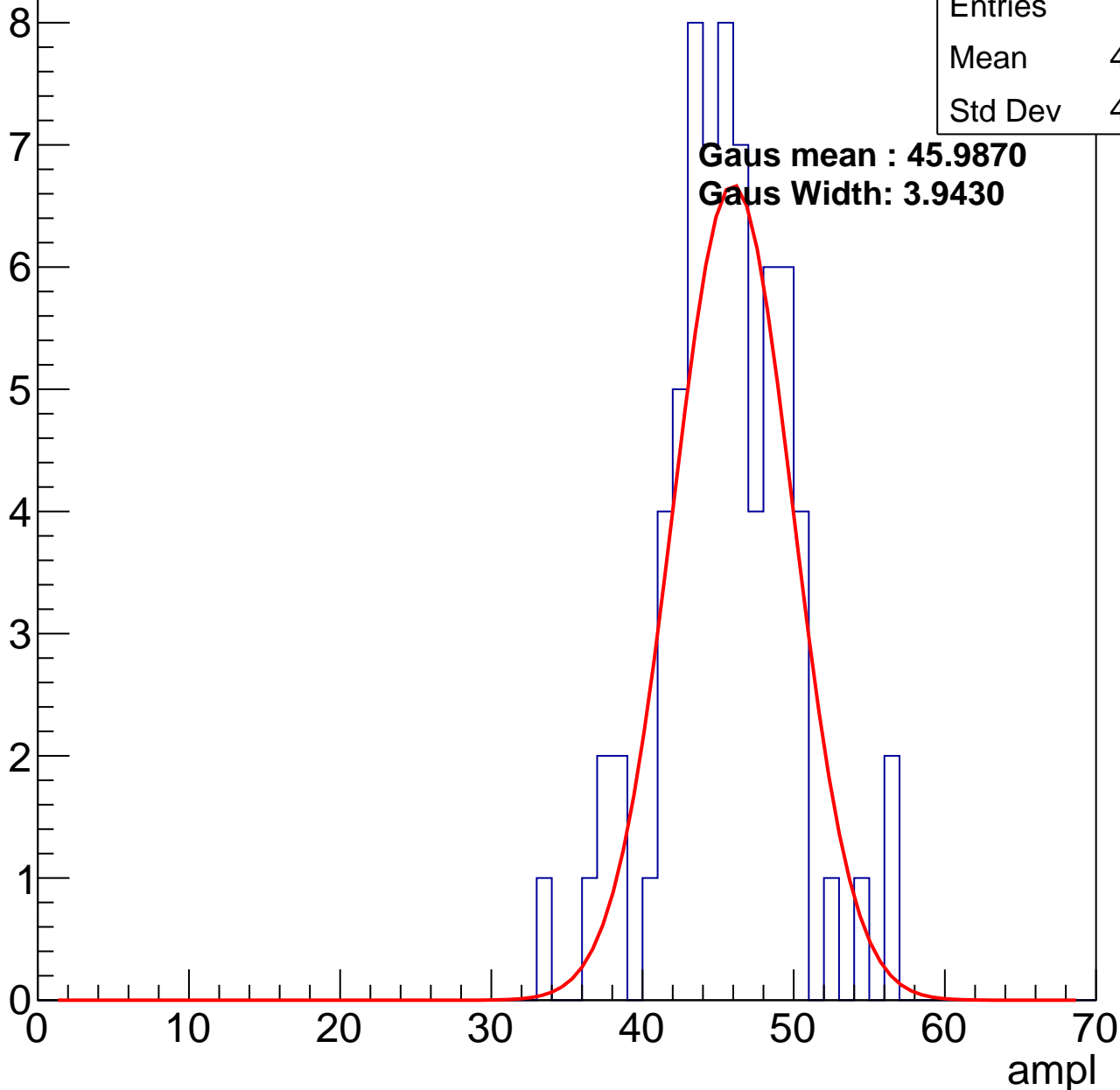
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	45.07
Std Dev	4.257

**Gaus mean : 45.9870**

**Gaus Width: 3.9430**

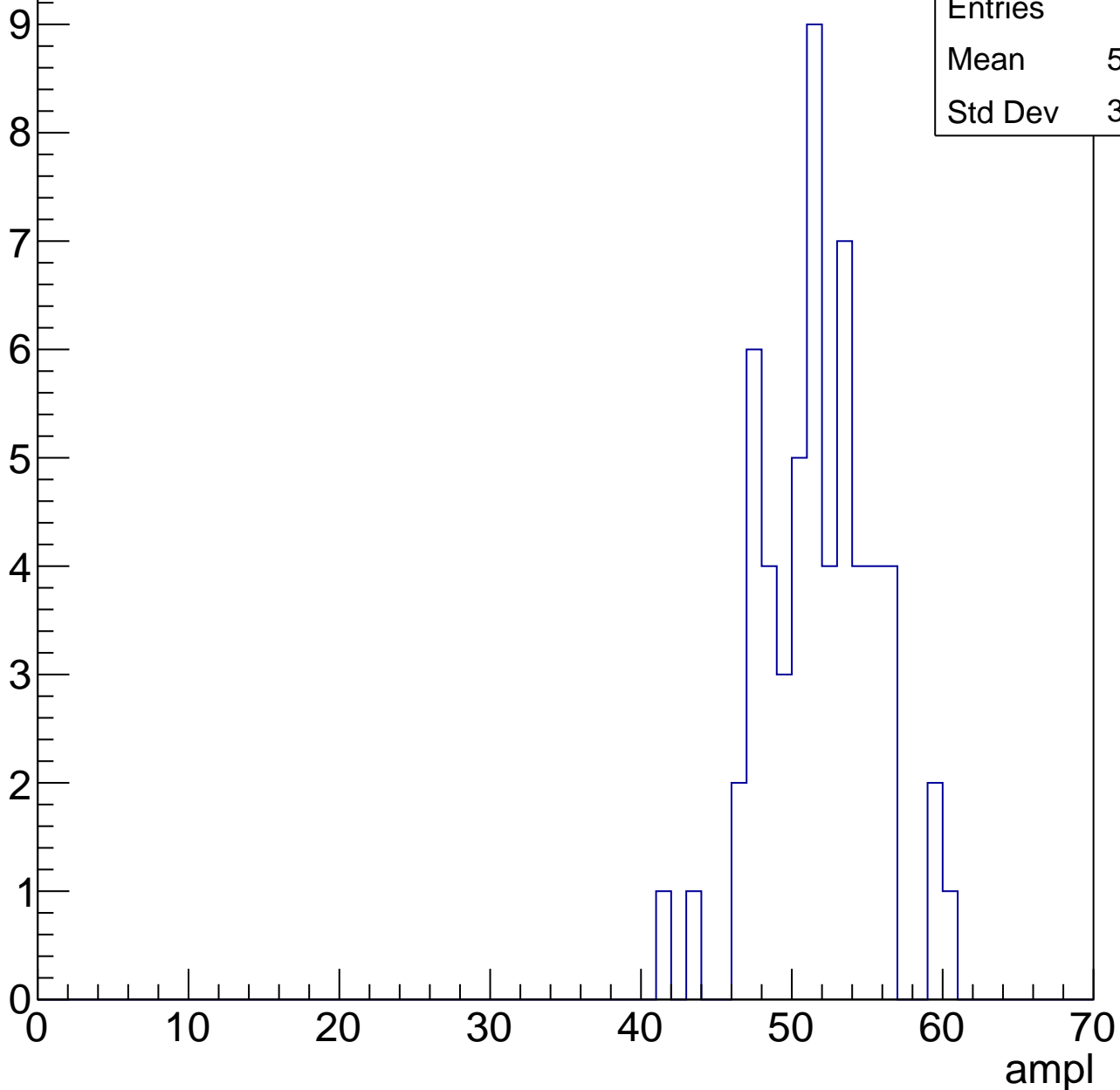


# B1L103S, U16-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	51.28
Std Dev	3.745

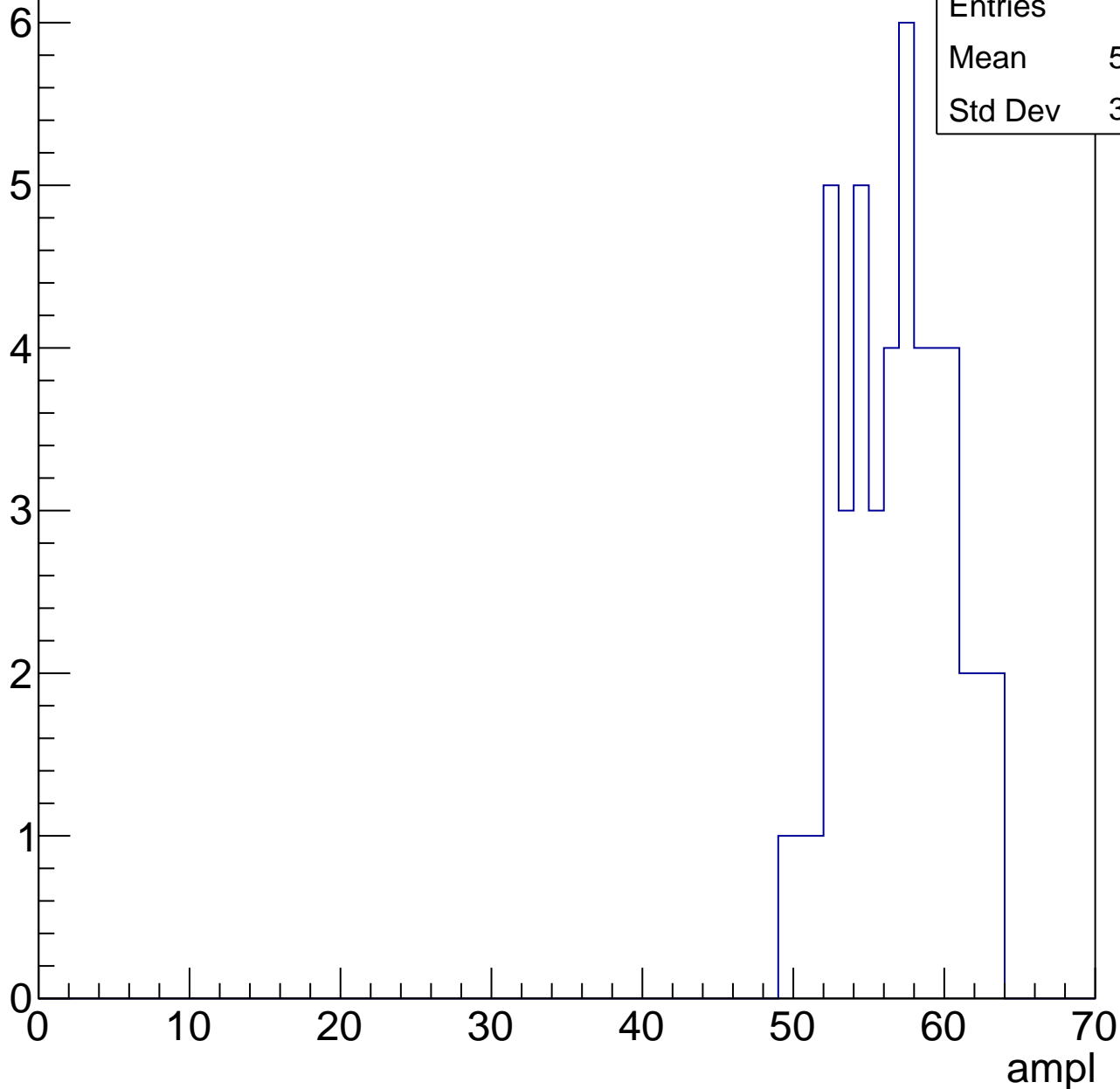


# B1L103S, U16-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	56.38
Std Dev	3.498

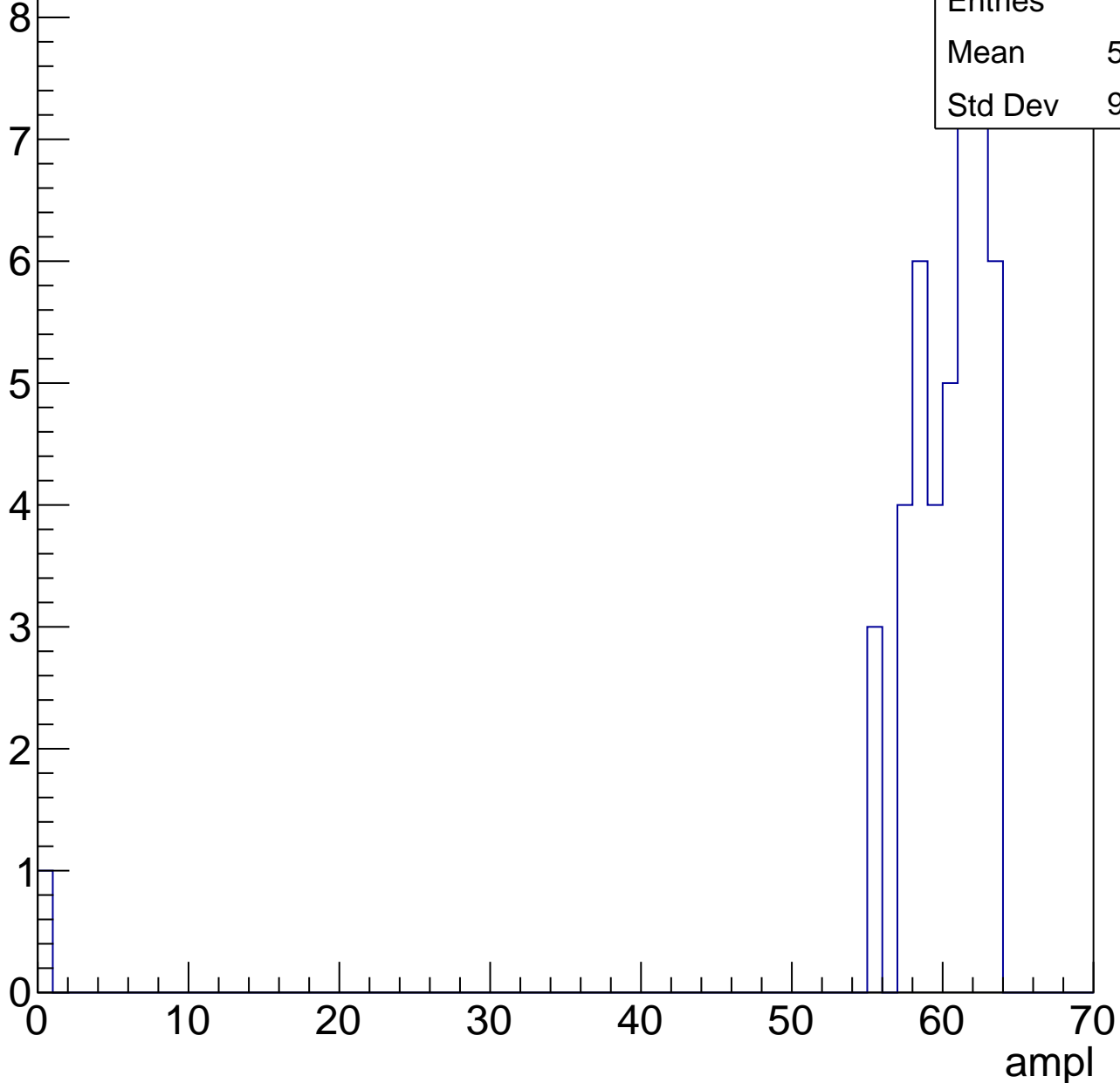


# B1L103S, U16-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	58.64
Std Dev	9.129



# B1L103S, U16-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U16-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch110, adc0

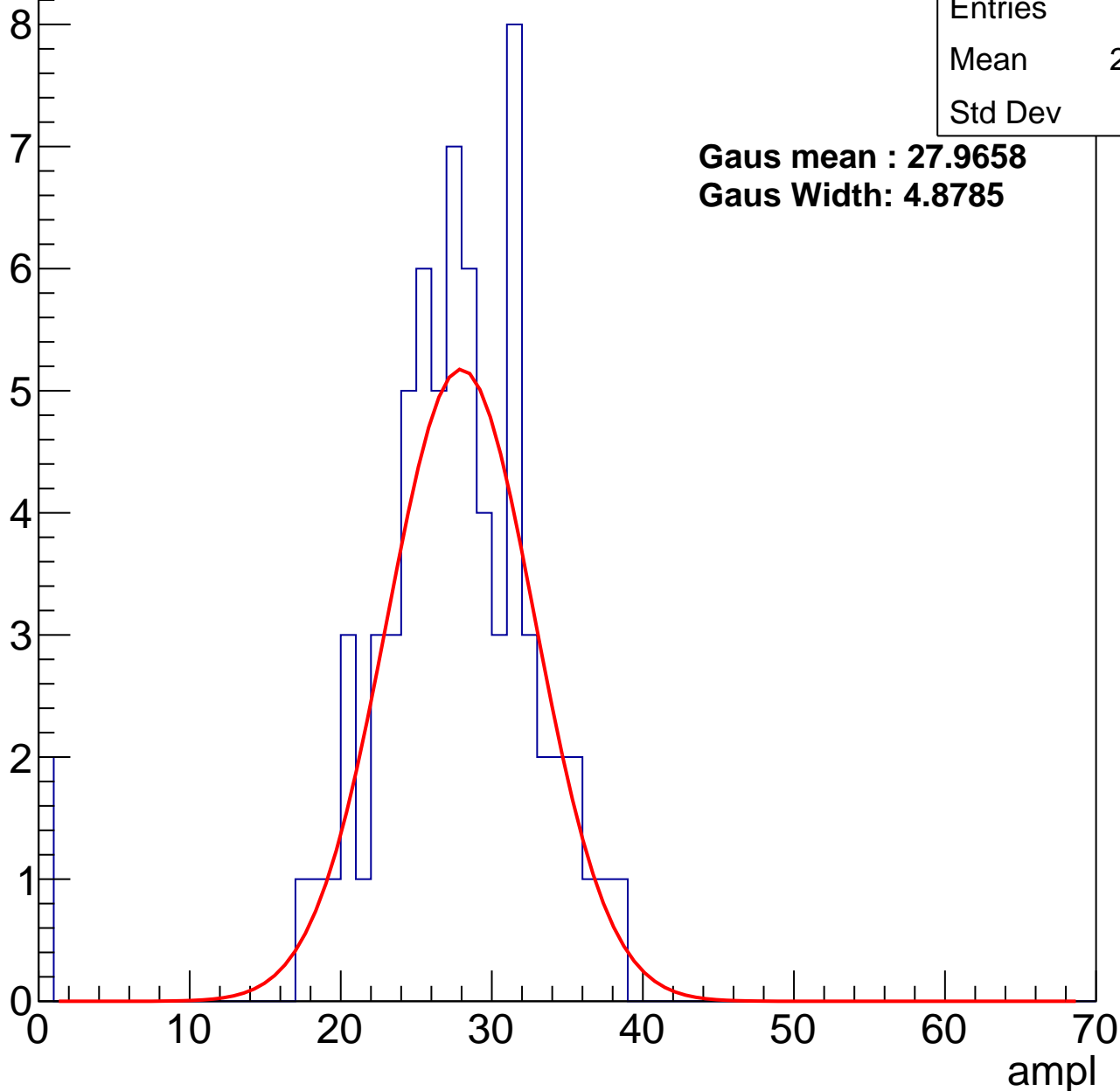
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	26.65
Std Dev	6.42

**Gaus mean : 27.9658**

**Gaus Width: 4.8785**



# B1L103S, U16-ch110, adc1

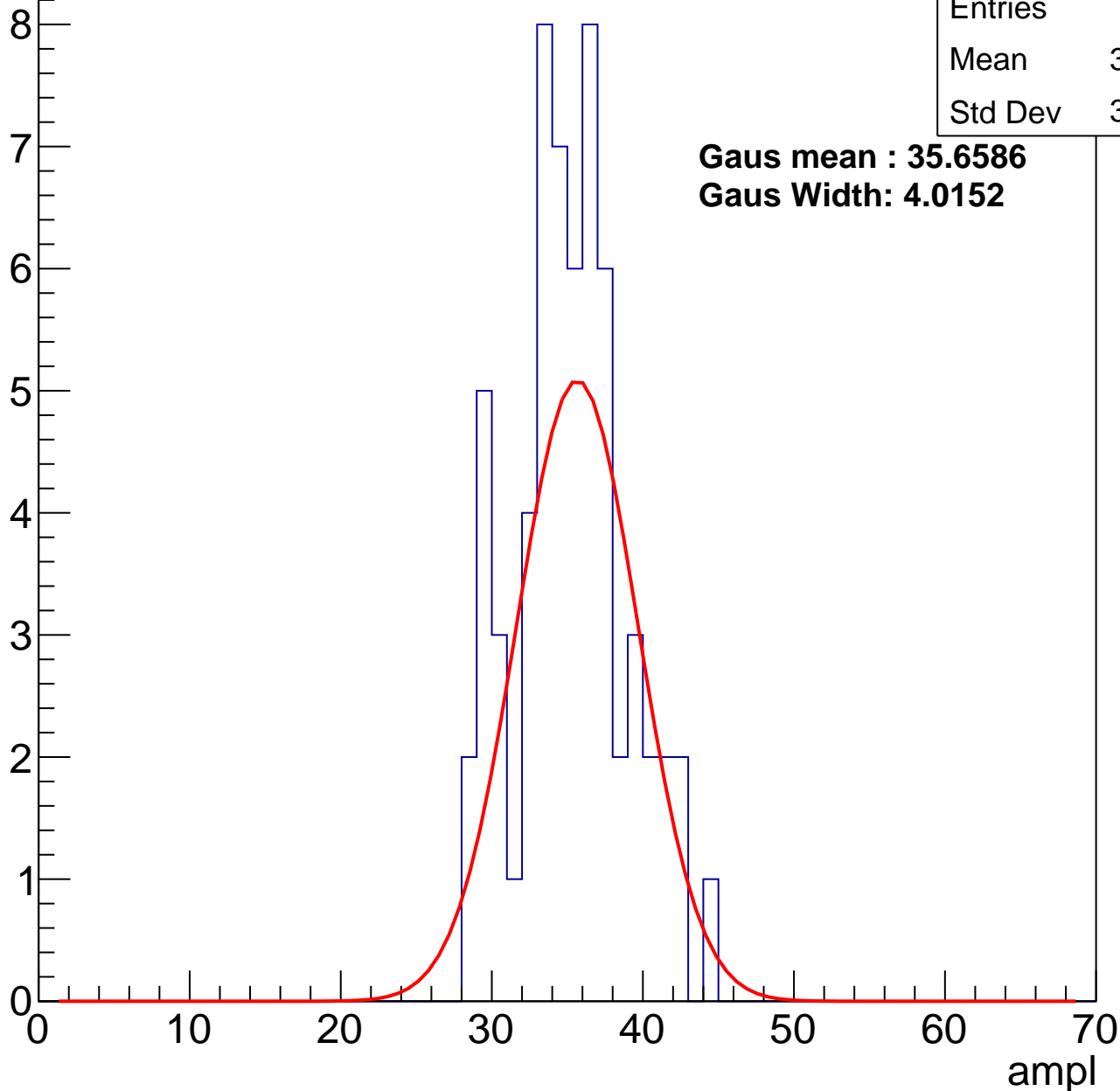
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	34.76
Std Dev	3.679

**Gaus mean : 35.6586**

**Gaus Width: 4.0152**



# B1L103S, U16-ch110, adc2

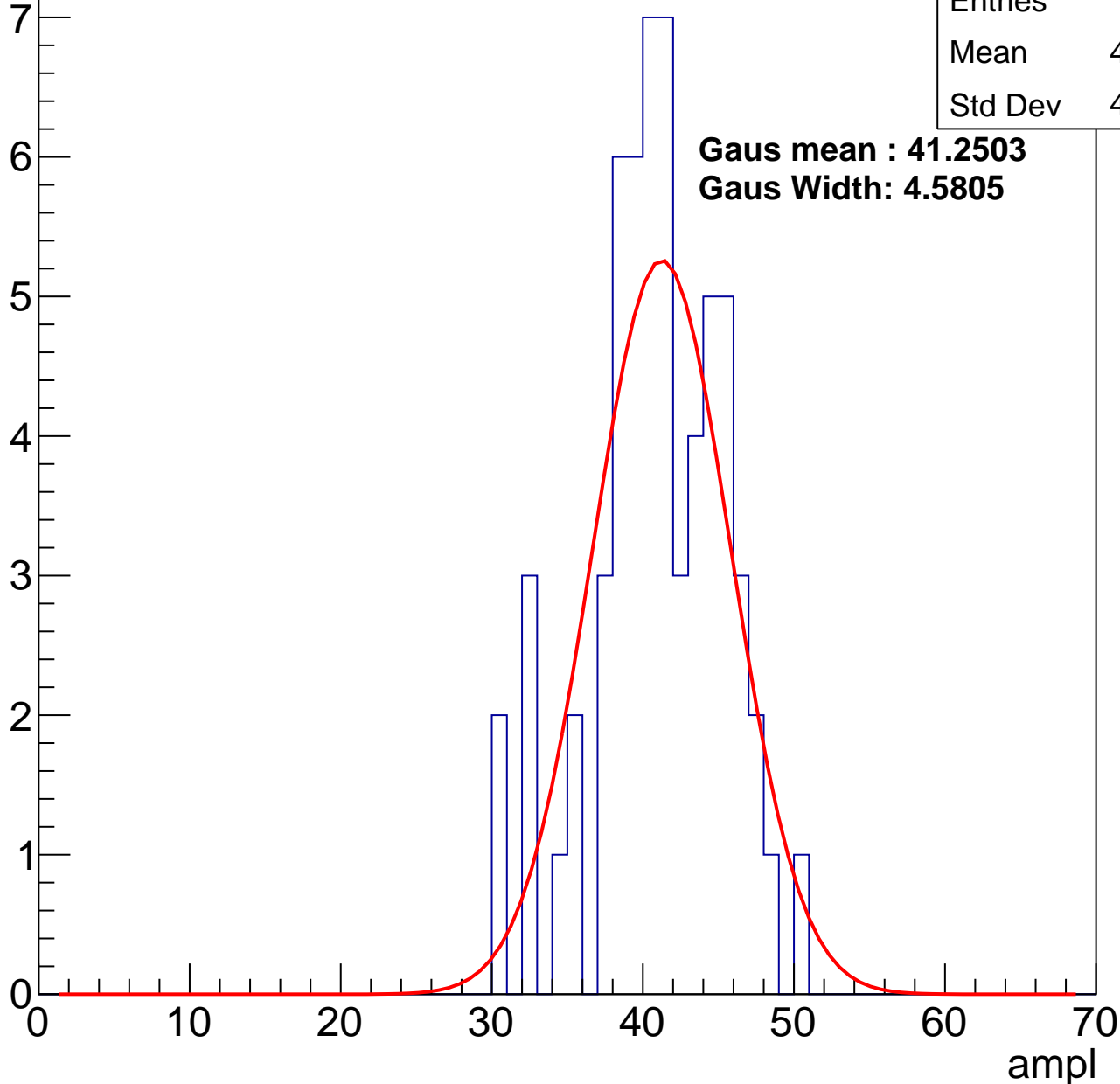
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	40.54
Std Dev	4.337

**Gaus mean : 41.2503**

**Gaus Width: 4.5805**

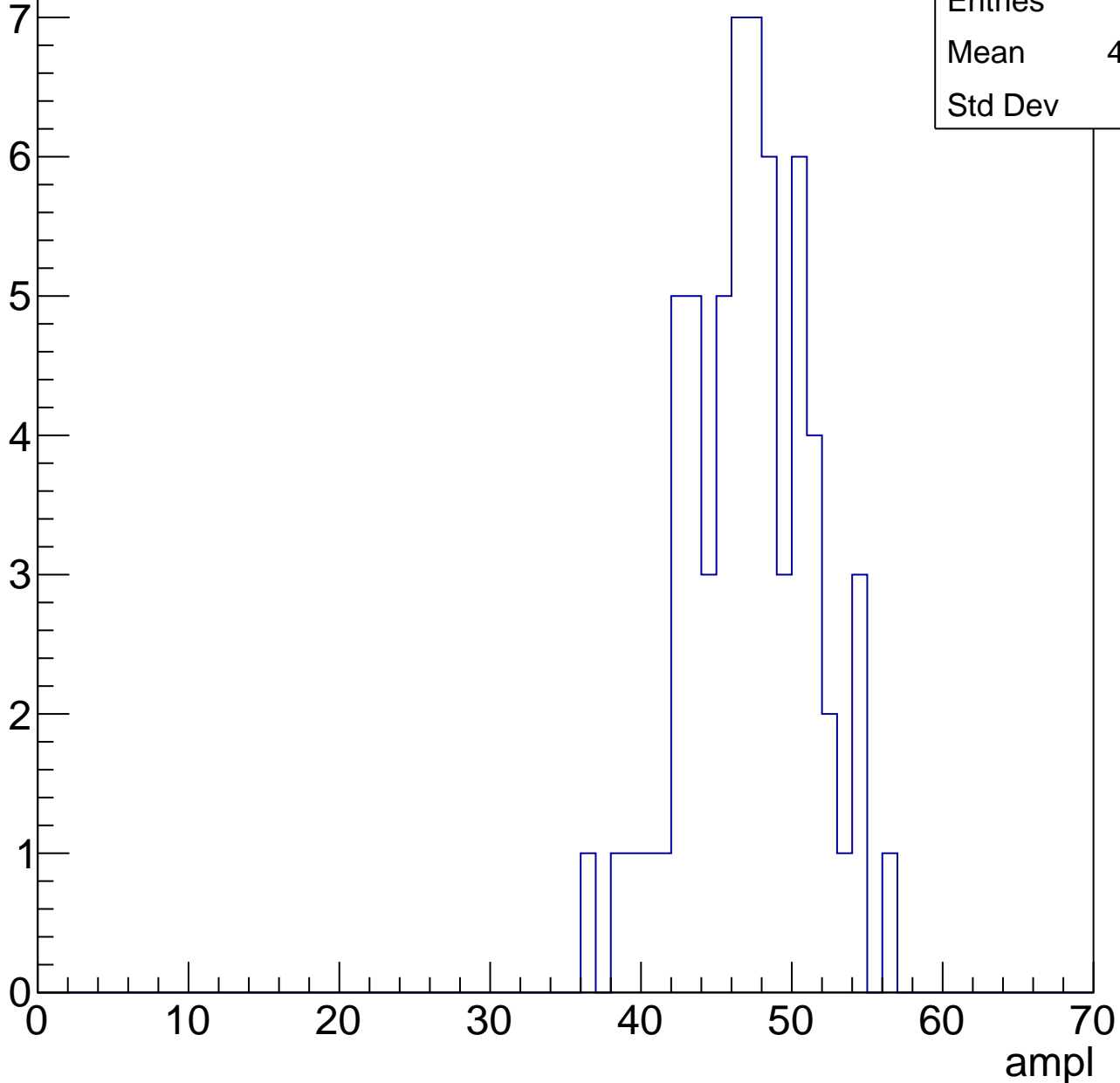


# B1L103S, U16-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	46.68
Std Dev	4.09

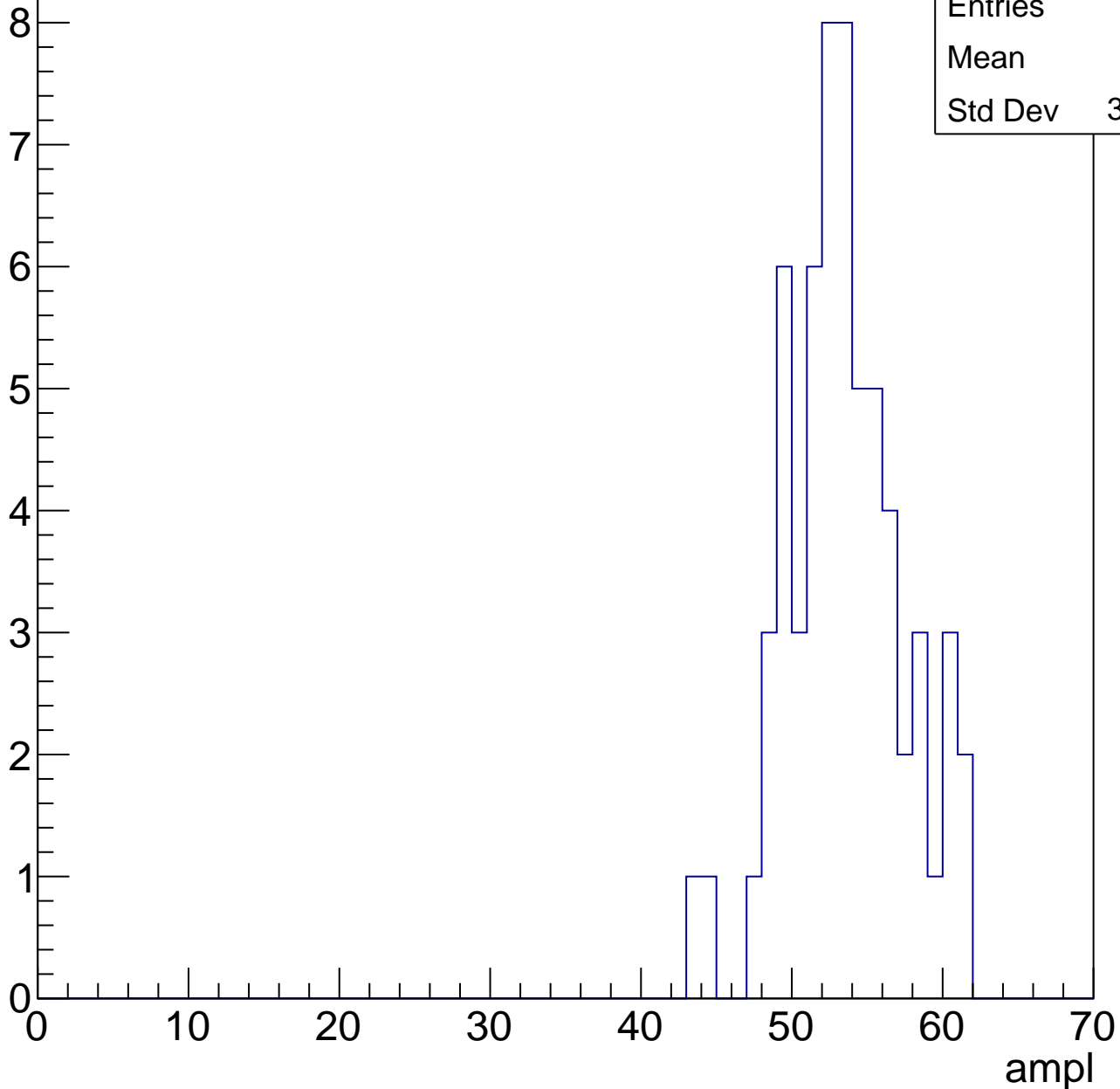


# B1L103S, U16-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	53
Std Dev	3.865

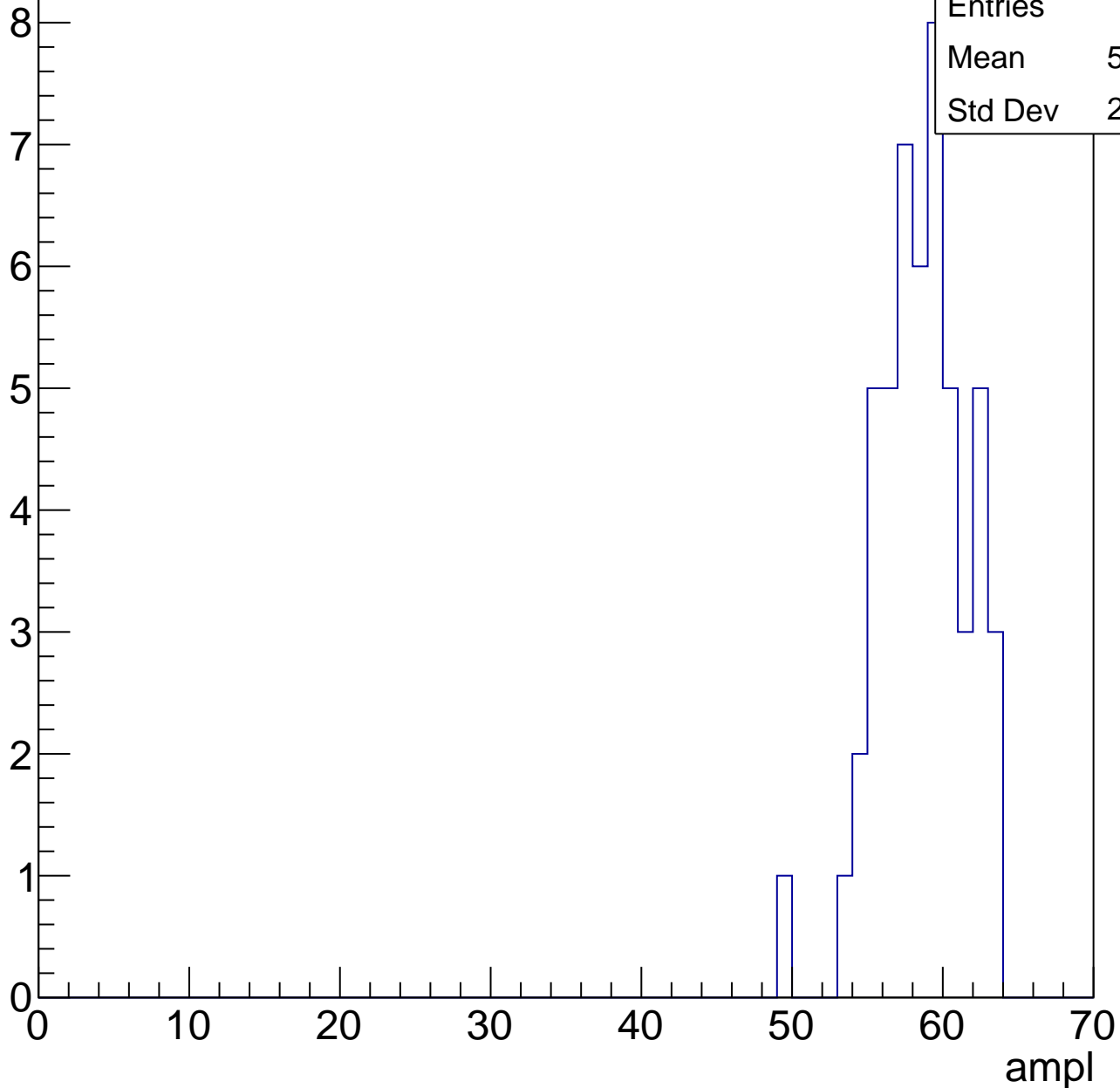


# B1L103S, U16-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	58.16
Std Dev	2.865

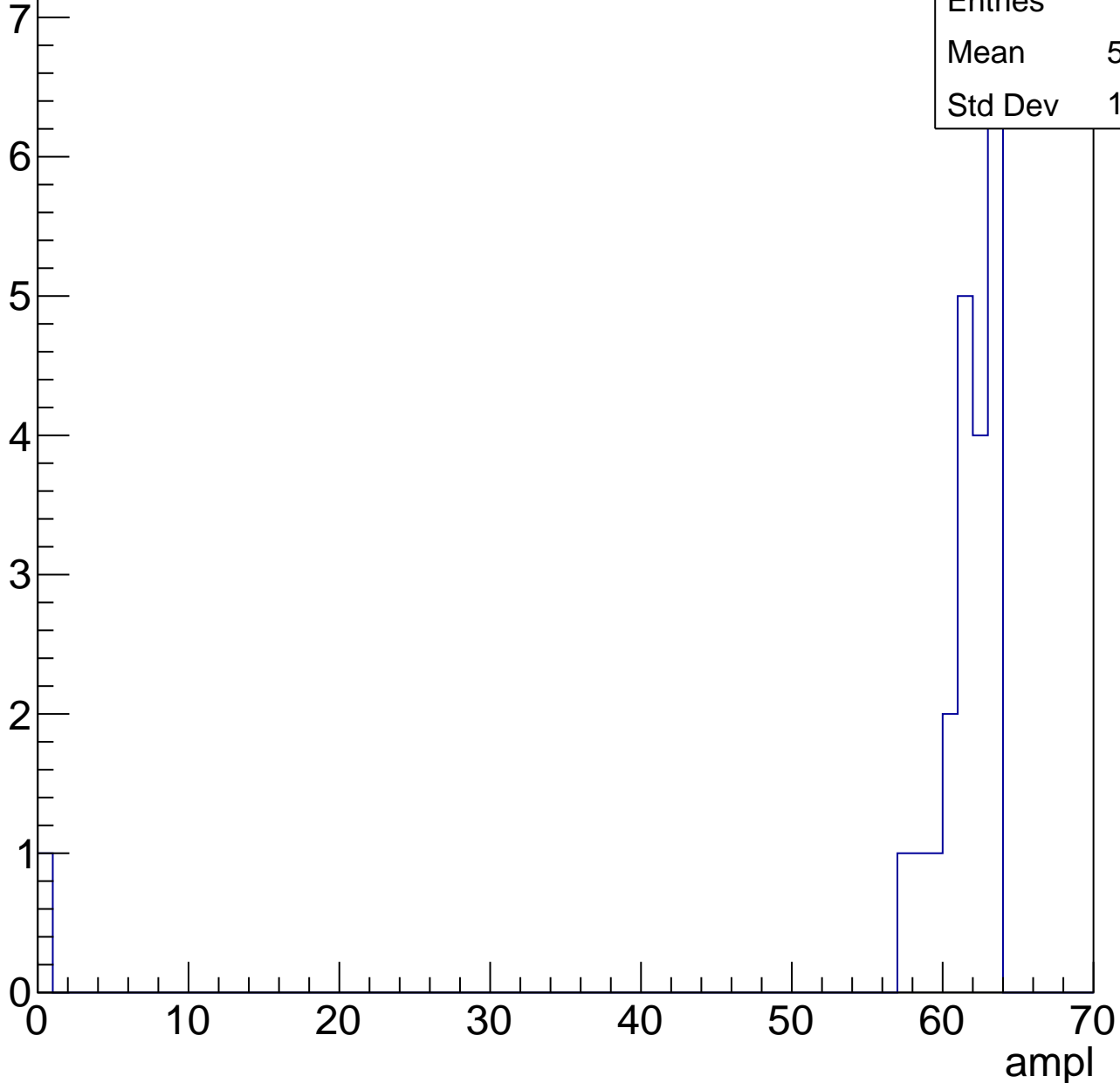


# B1L103S, U16-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	22
Mean	58.55
Std Dev	12.88





# B1L103S, U16-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	20.67
Std Dev	29.23

# B1L103S, U16-ch111, adc0

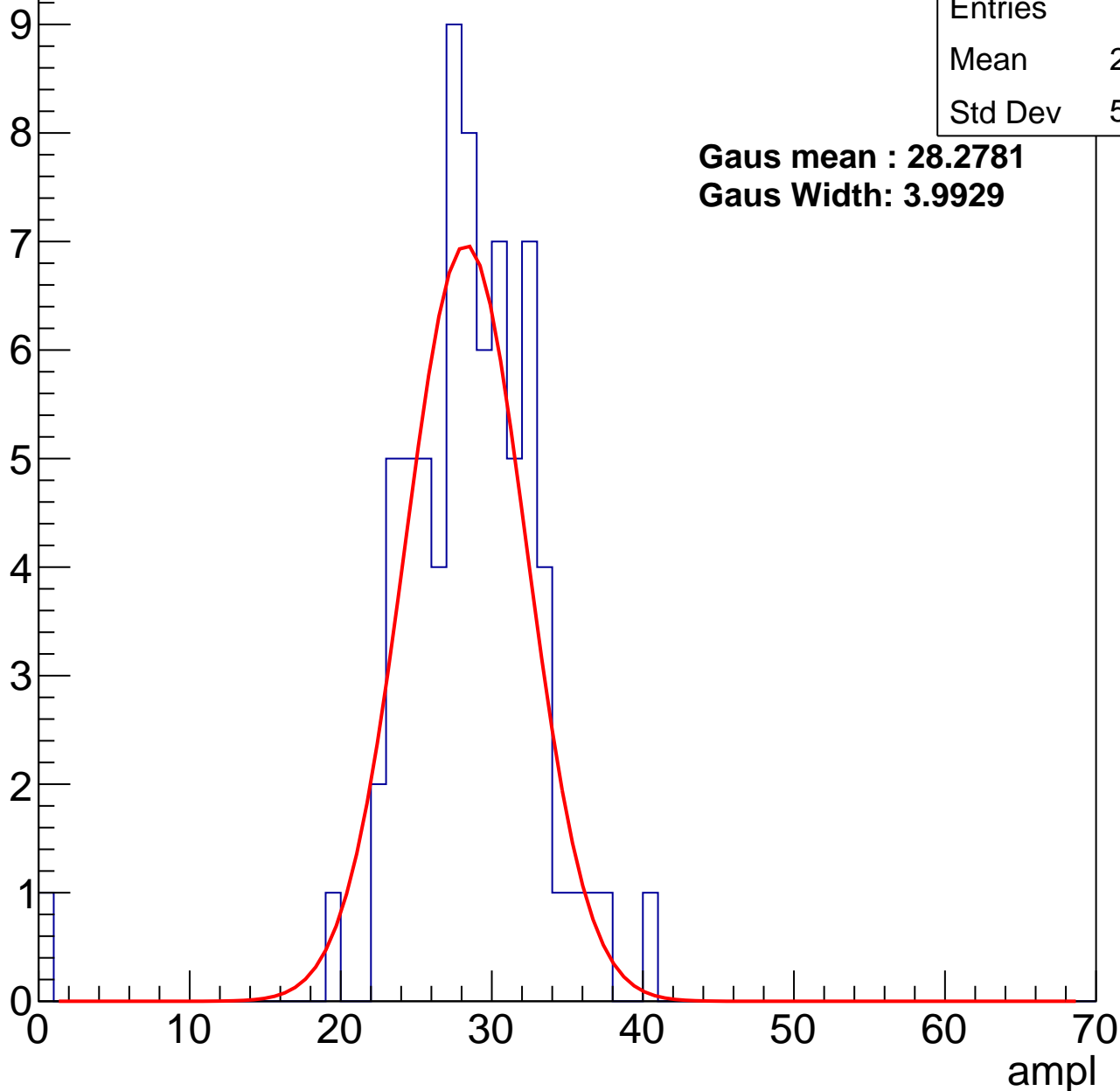
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	27.99
Std Dev	5.036

**Gaus mean : 28.2781**

**Gaus Width: 3.9929**



# B1L103S, U16-ch111, adc1

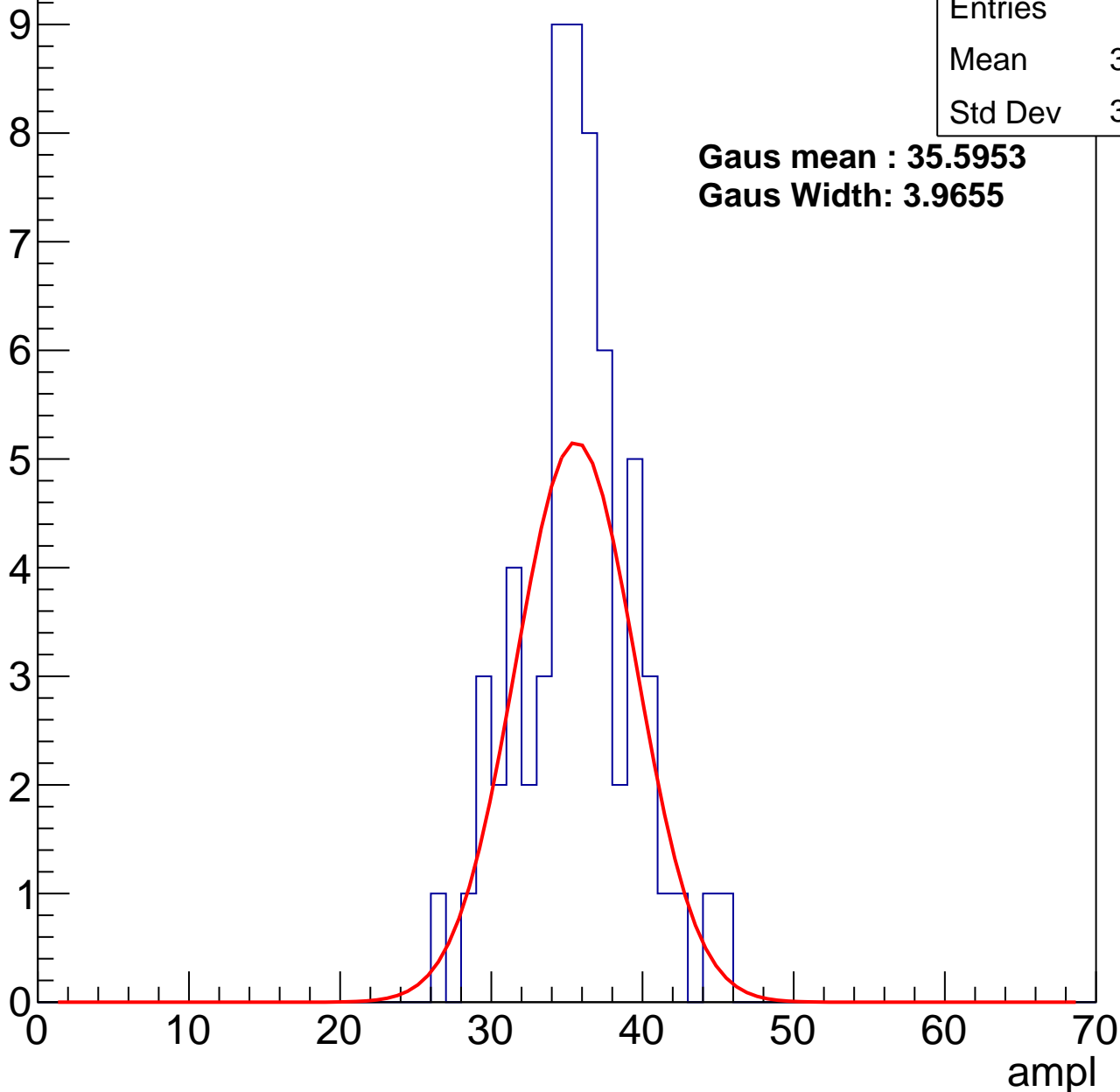
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	35.19
Std Dev	3.724

**Gaus mean : 35.5953**

**Gaus Width: 3.9655**



# B1L103S, U16-ch111, adc2

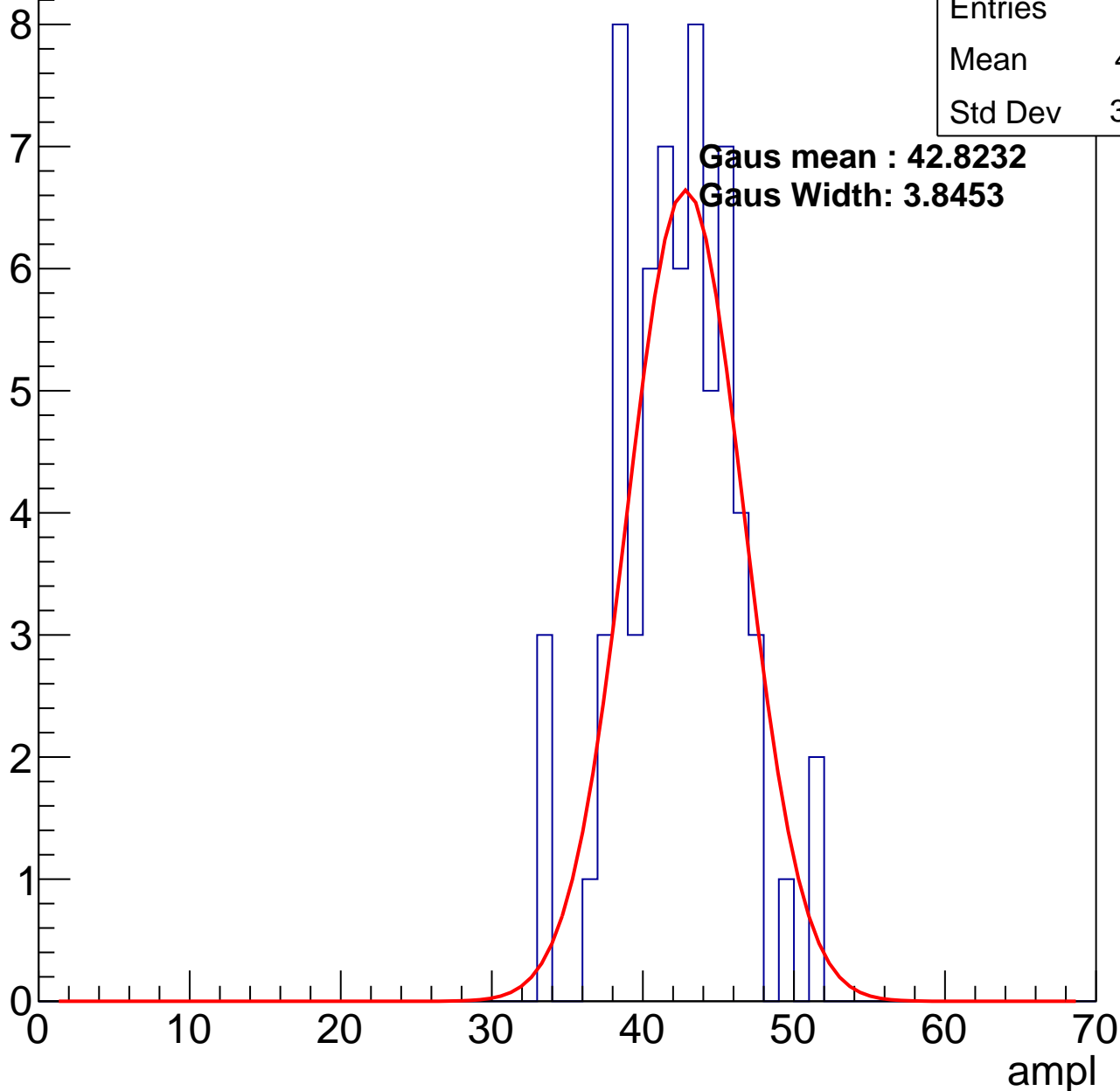
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	41.81
Std Dev	3.822

**Gaus mean : 42.8232**

**Gaus Width: 3.8453**

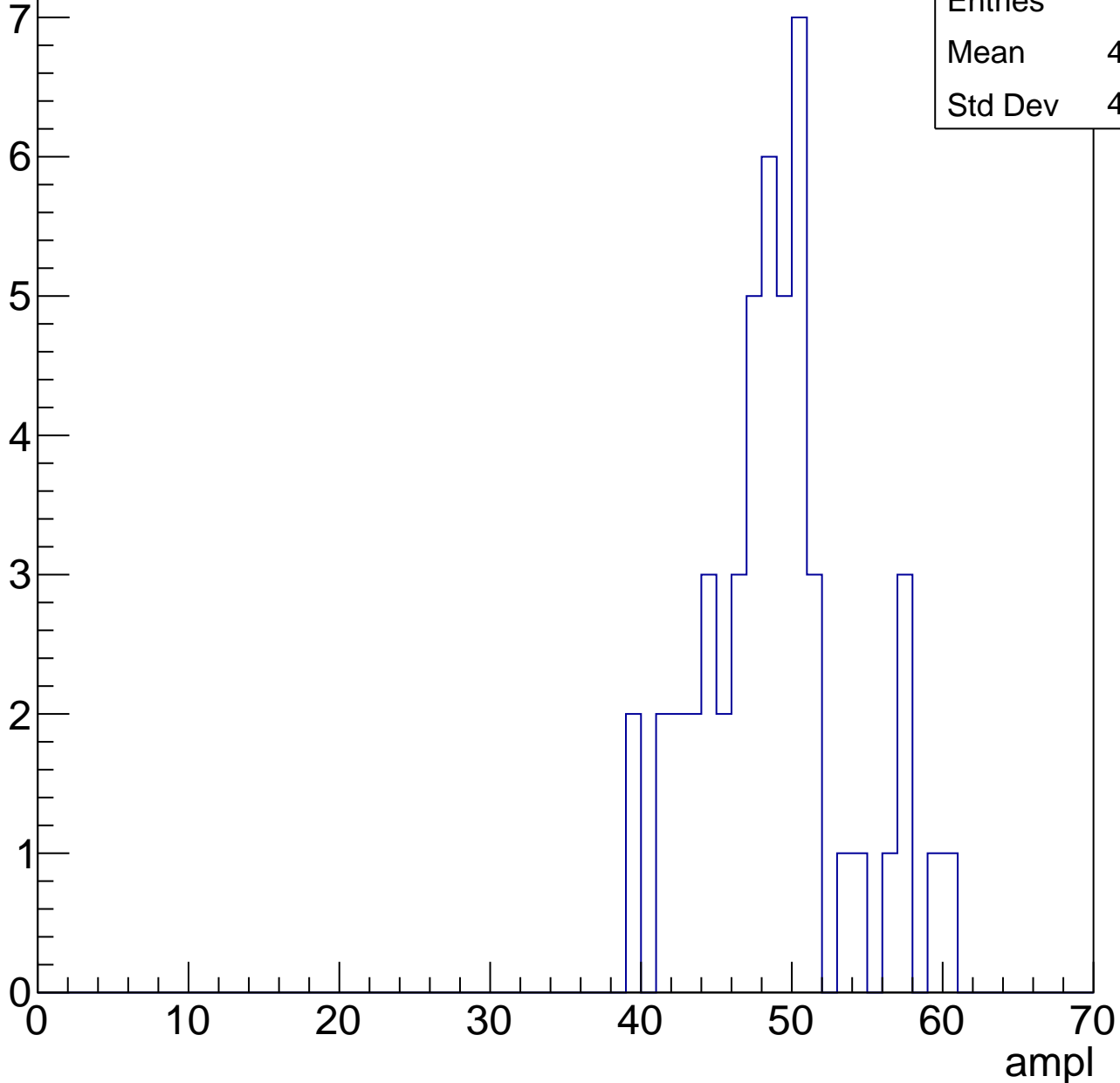


# B1L103S, U16-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

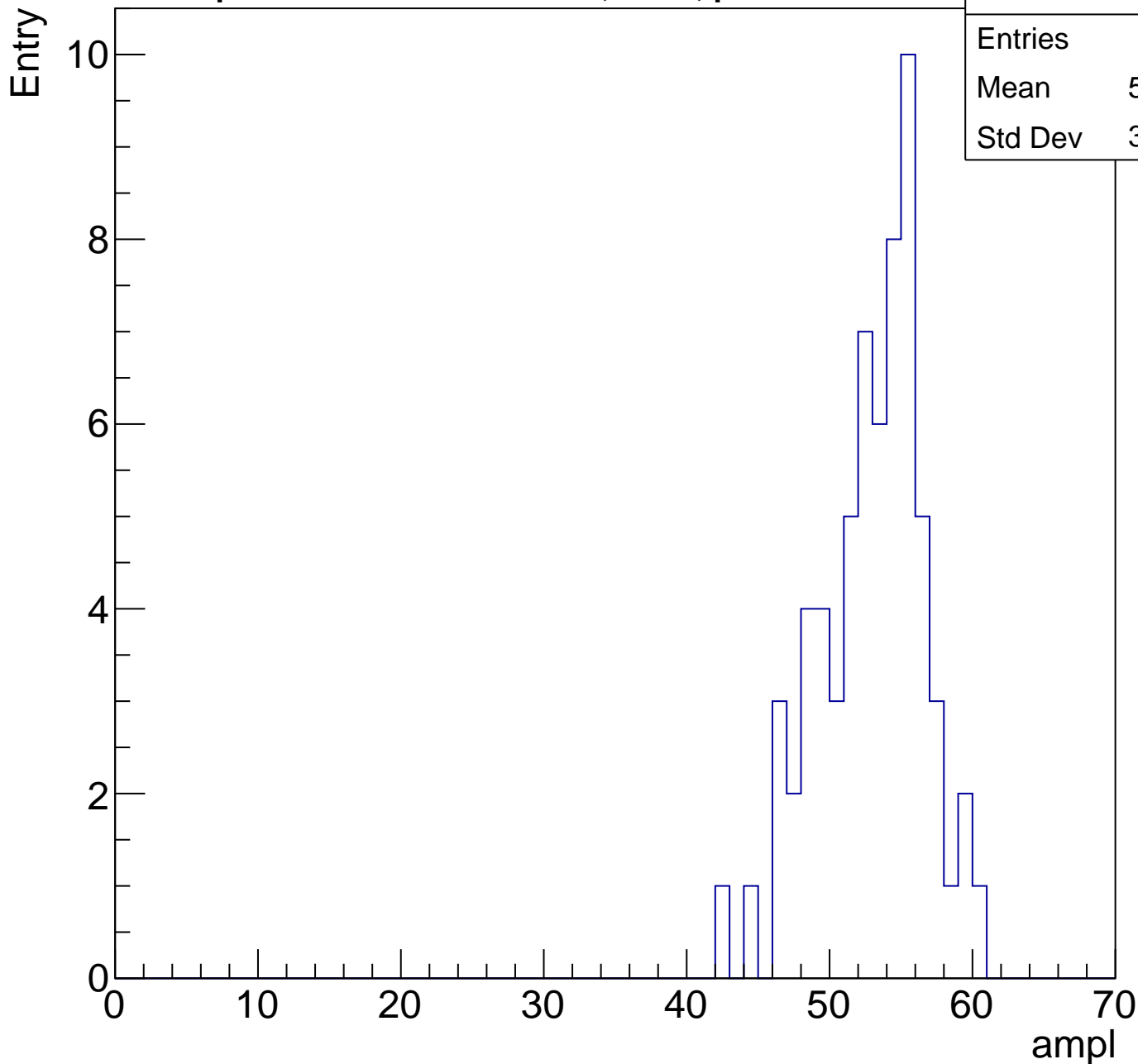
Entries	50
Mean	48.28
Std Dev	4.804



# B1L103S, U16-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	66
Mean	52.45
Std Dev	3.706



# B1L103S, U16-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	62
Mean	59.03
Std Dev	2.994

Entry

10

8

6

4

2

0

0

10

20

30

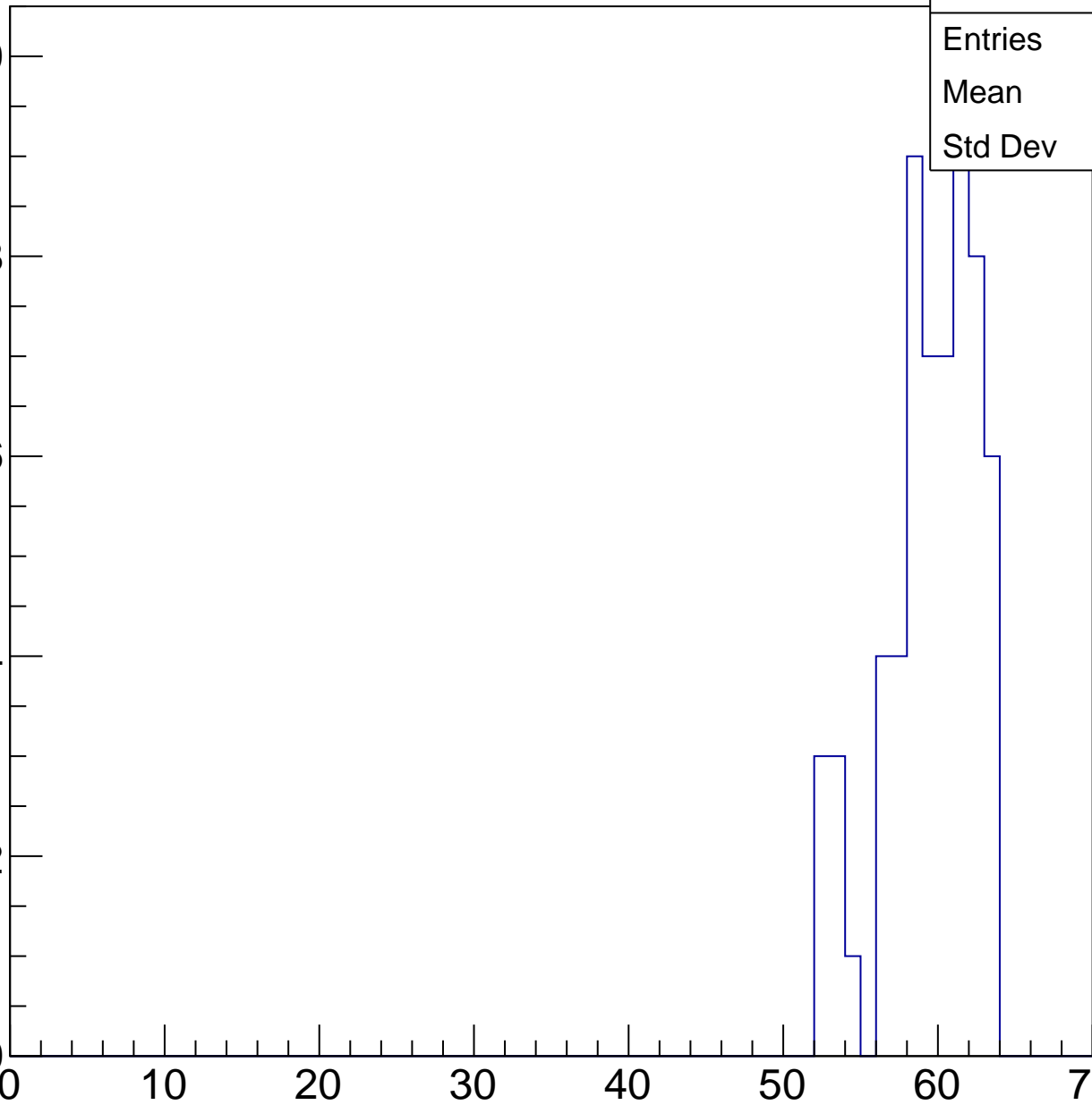
40

50

60

70

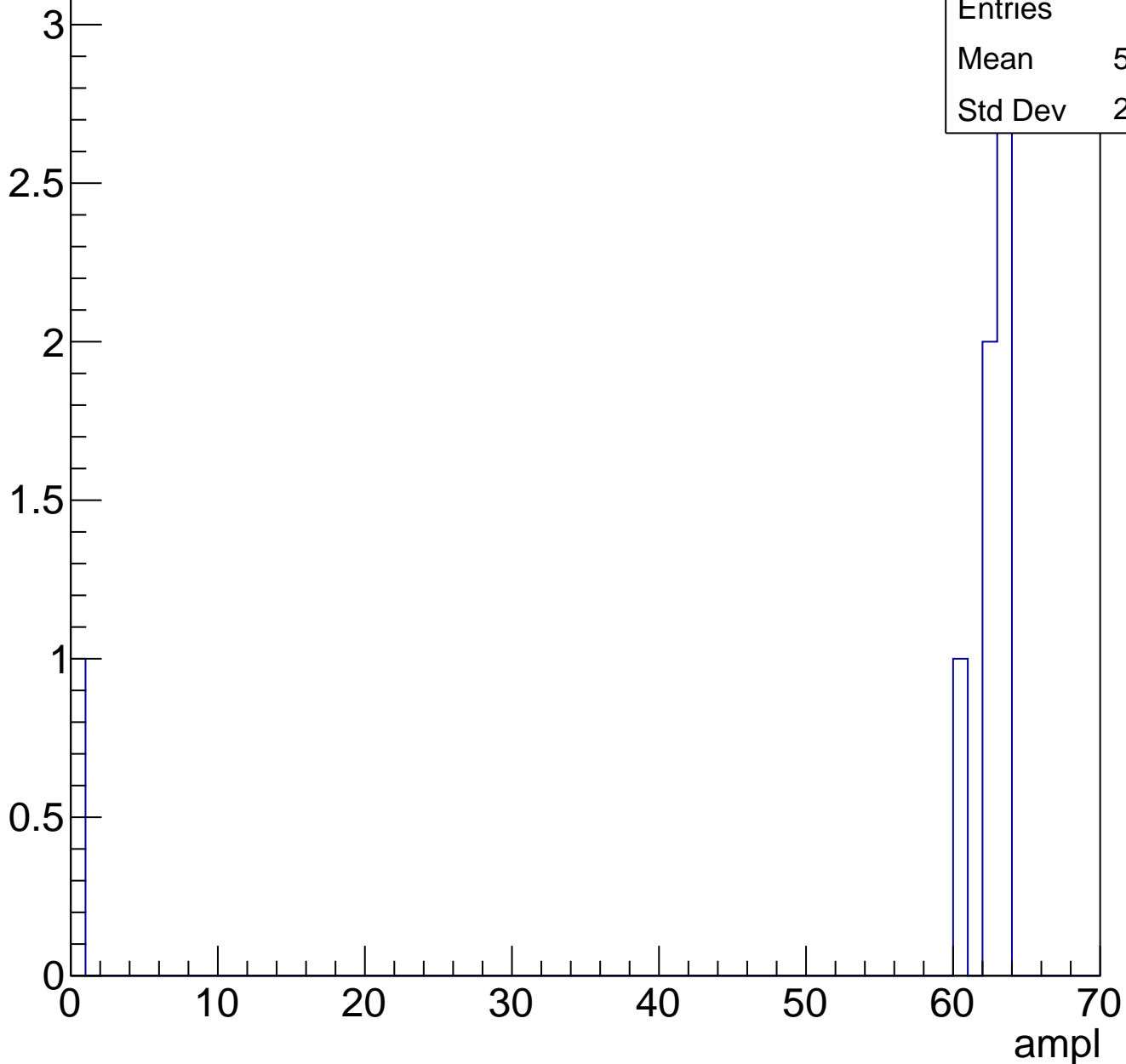
ampl



# B1L103S, U16-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch112, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	88
Mean	28.58
Std Dev	6.018

**Gaus mean : 29.8736**

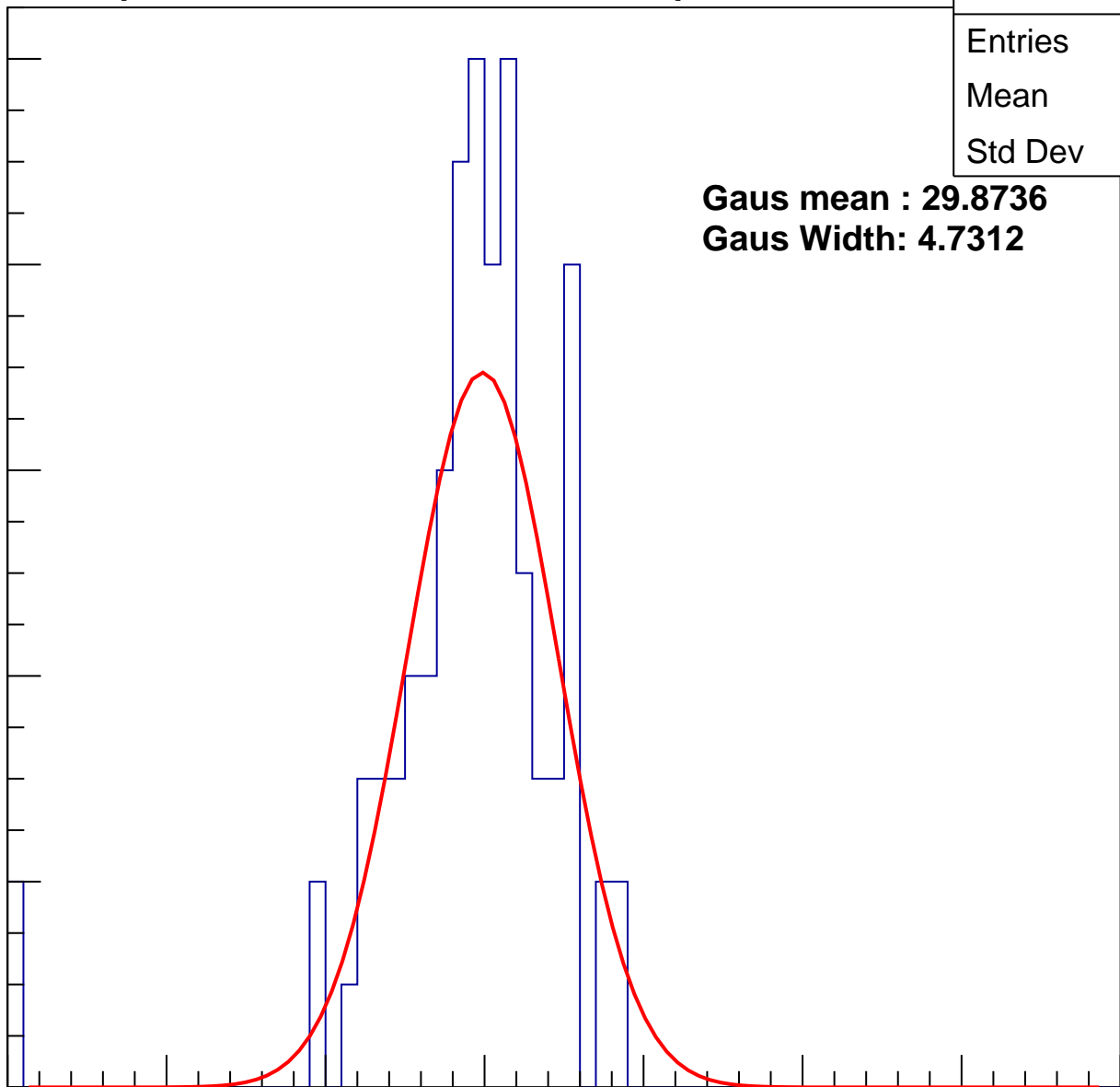
**Gaus Width: 4.7312**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U16-ch112, adc1

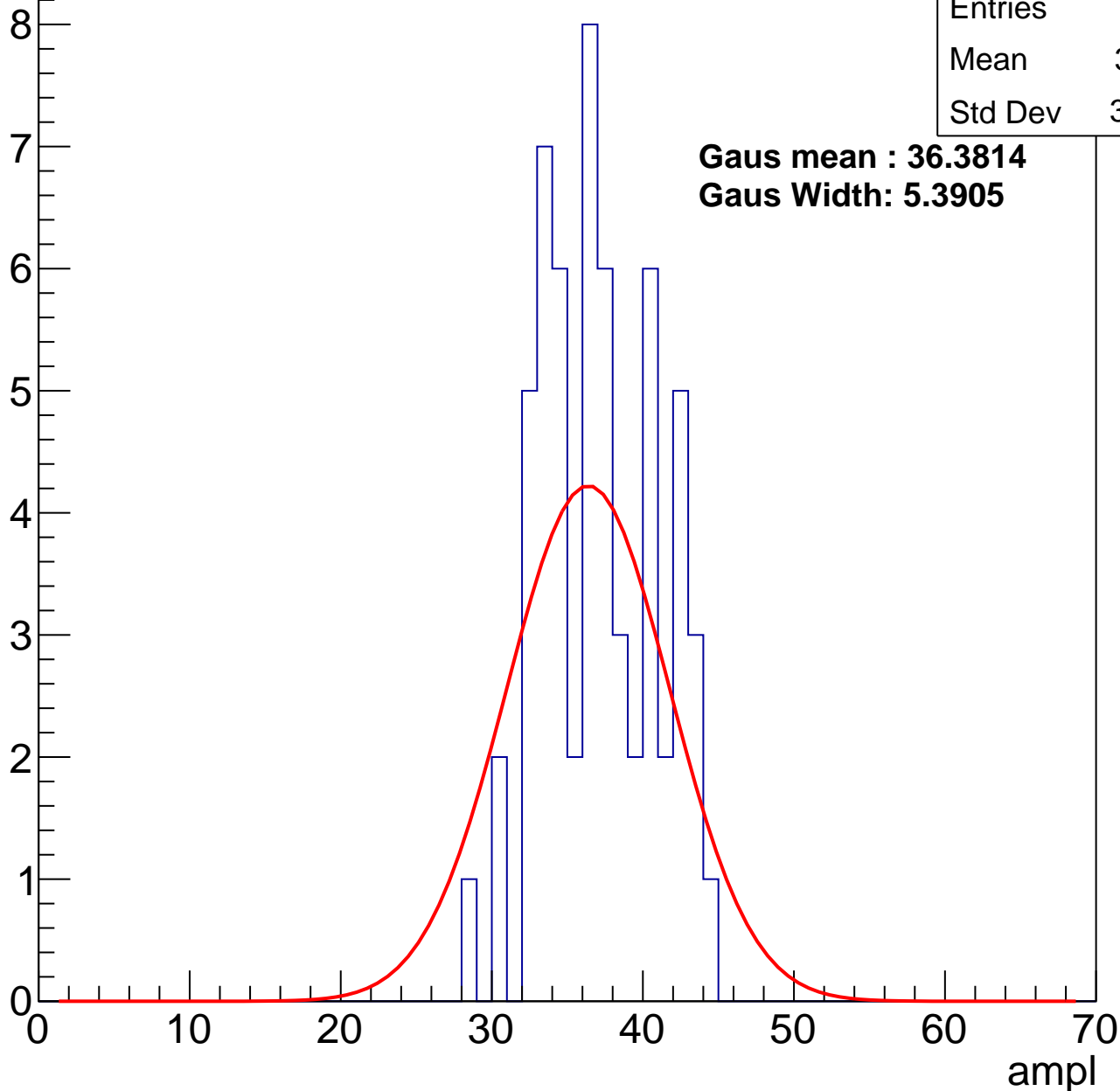
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	36.61
Std Dev	3.809

**Gaus mean : 36.3814**

**Gaus Width: 5.3905**



# B1L103S, U16-ch112, adc2

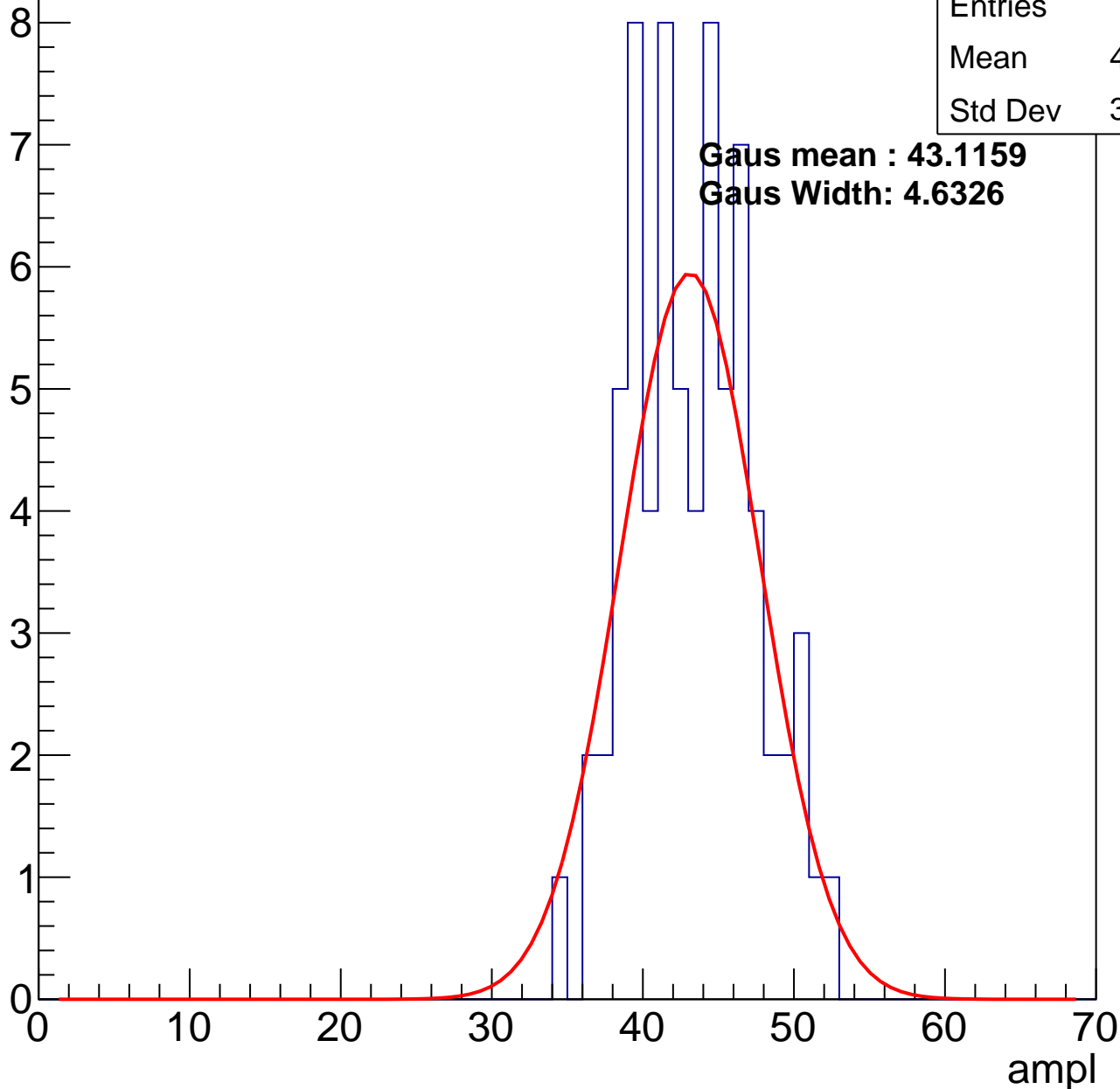
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	42.86
Std Dev	3.987

**Gaus mean : 43.1159**

**Gaus Width: 4.6326**

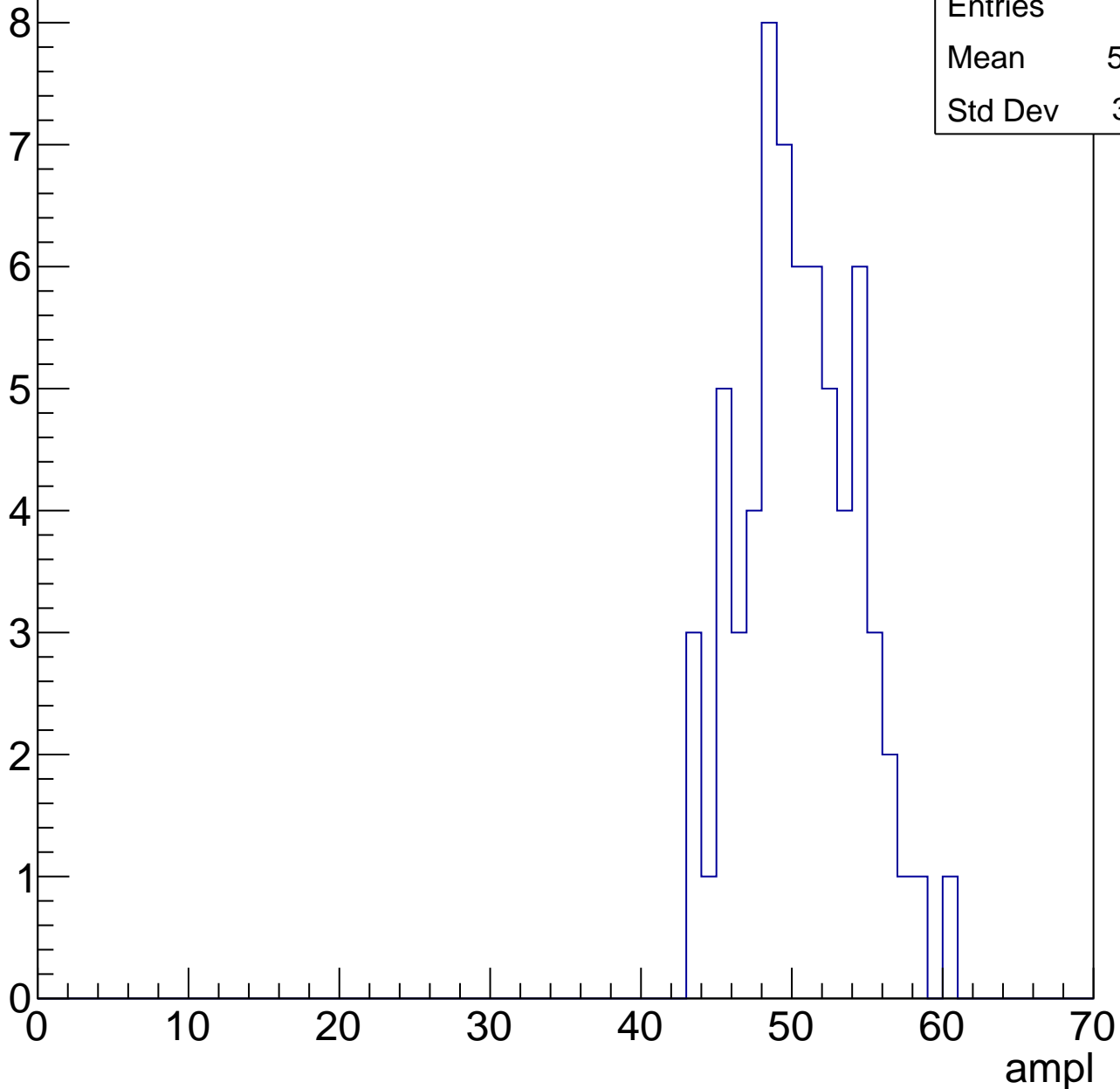


# B1L103S, U16-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	50.08
Std Dev	3.791

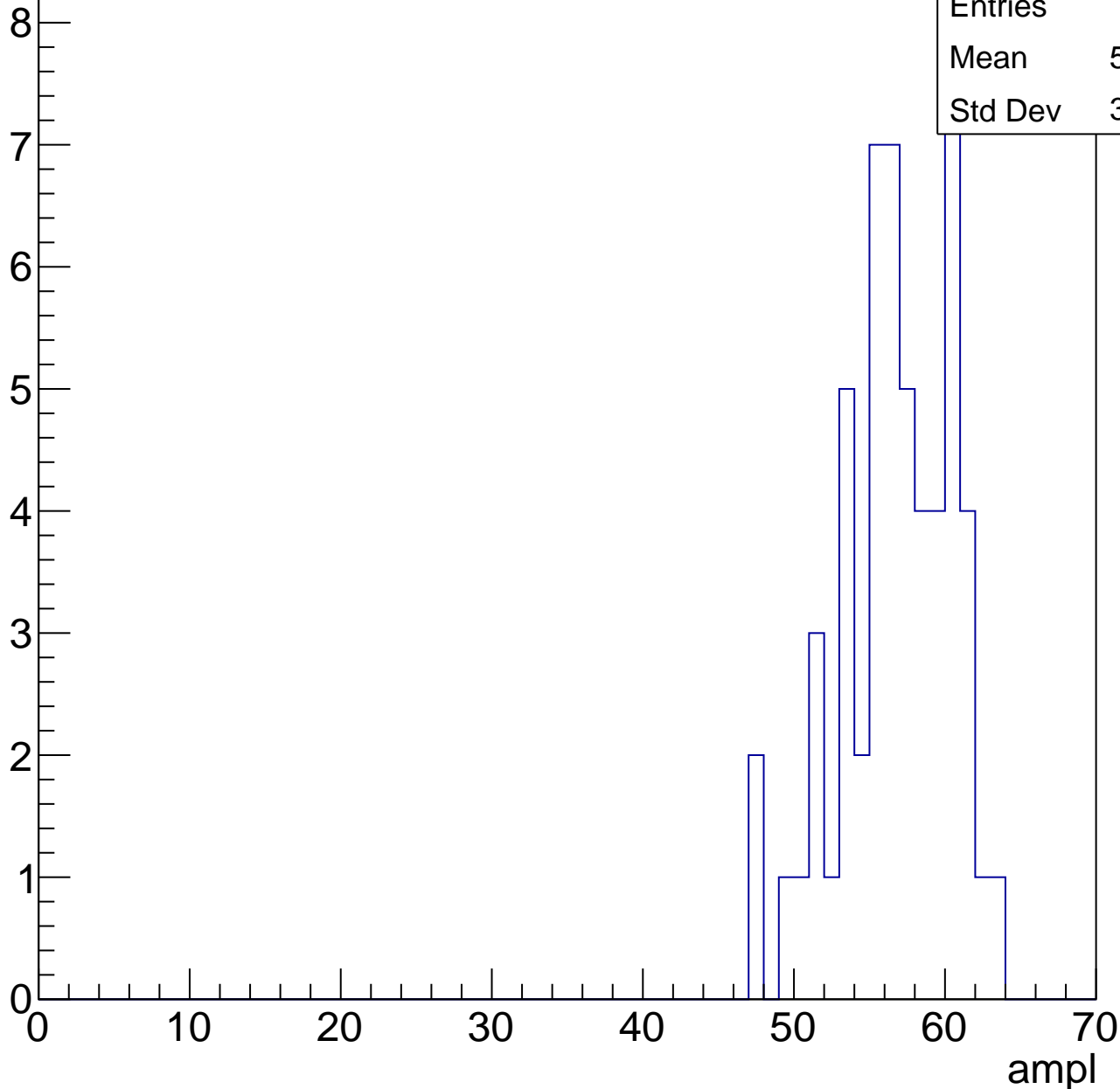


# B1L103S, U16-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	56.25
Std Dev	3.695

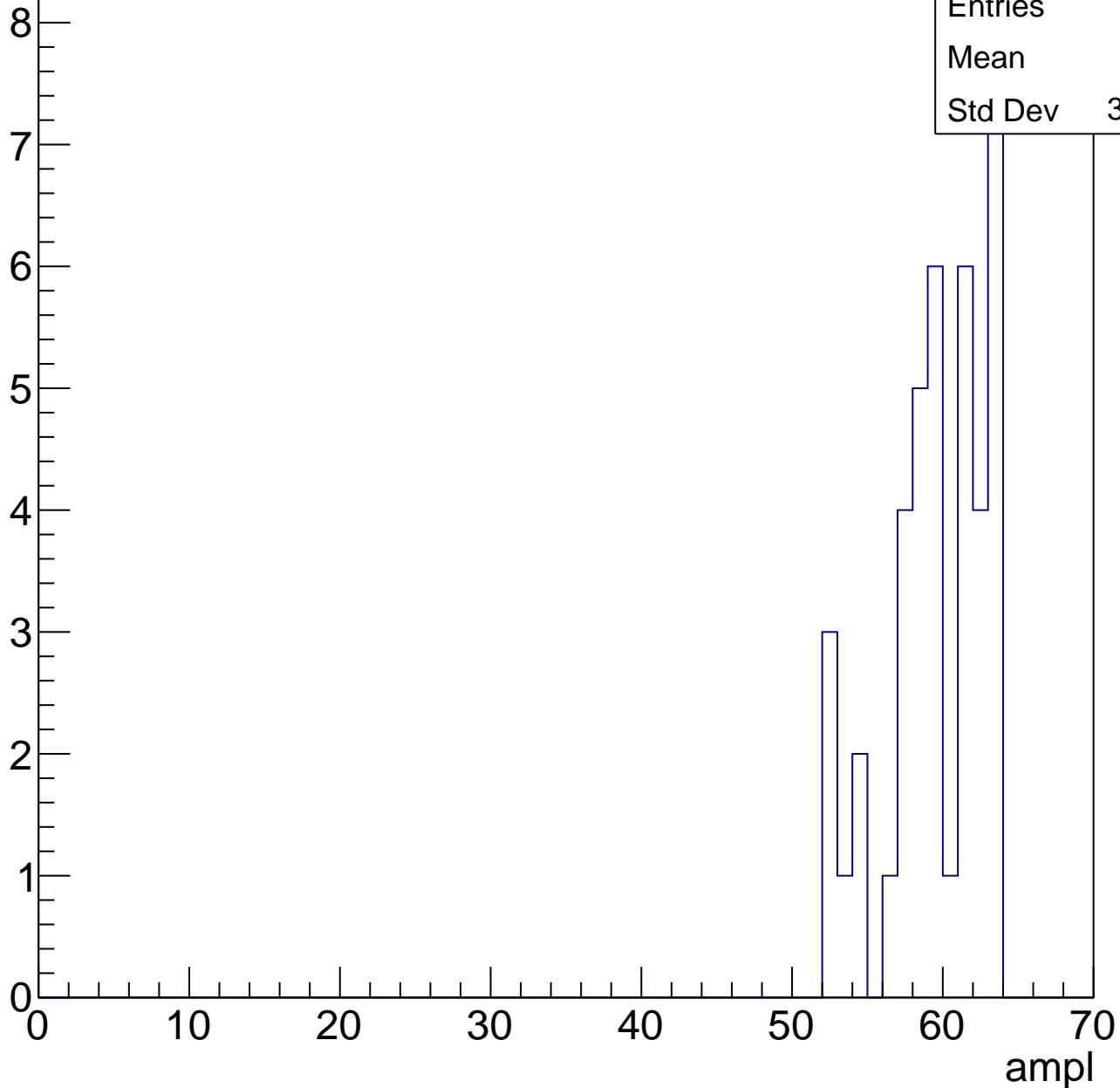


# B1L103S, U16-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

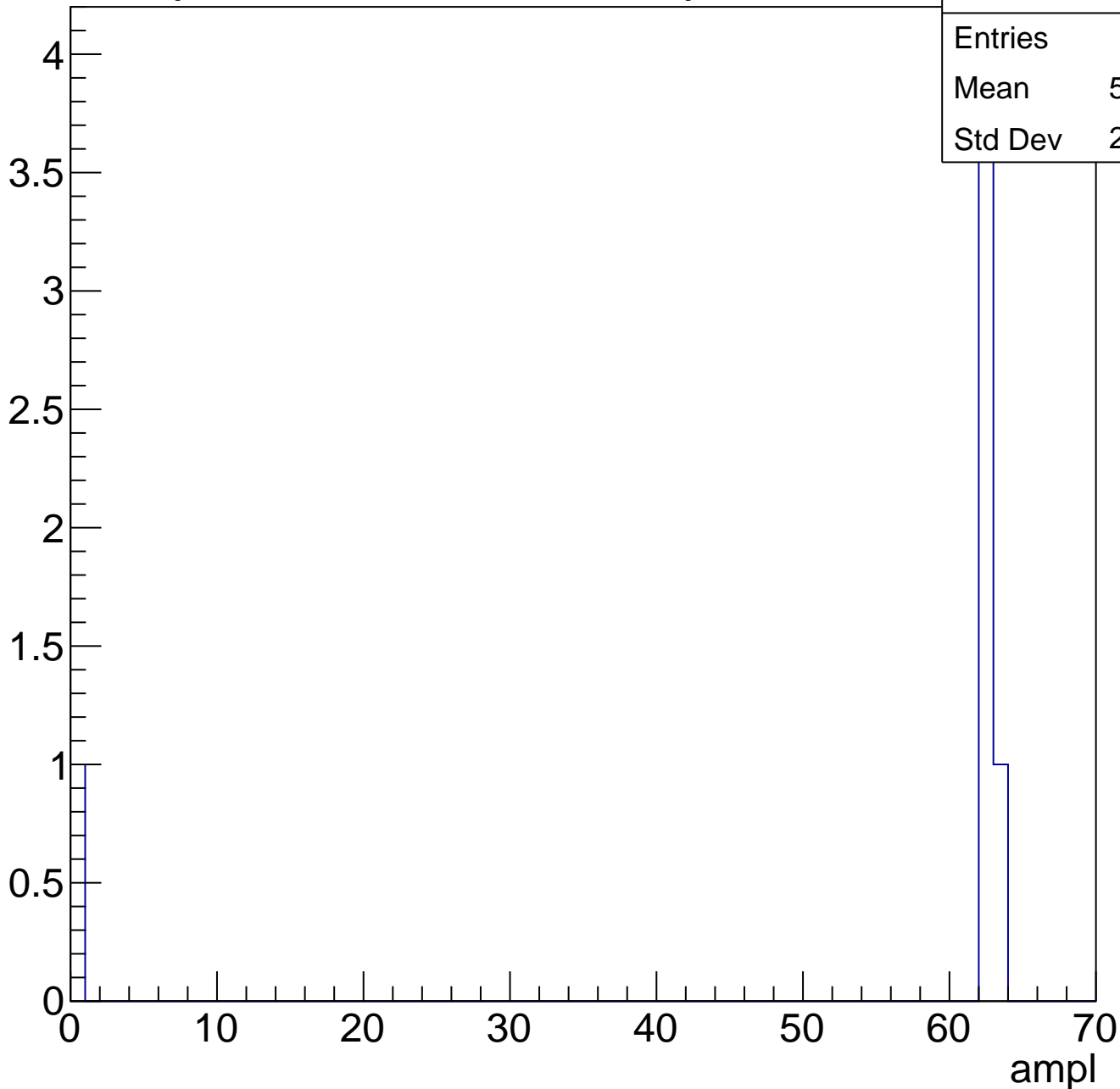
Entries	41
Mean	59.1
Std Dev	3.319



# B1L103S, U16-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	62
Std Dev	0

# B1L103S, U16-ch113, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	83
Mean	27.78
Std Dev	3.859

**Gaus mean : 27.7585**

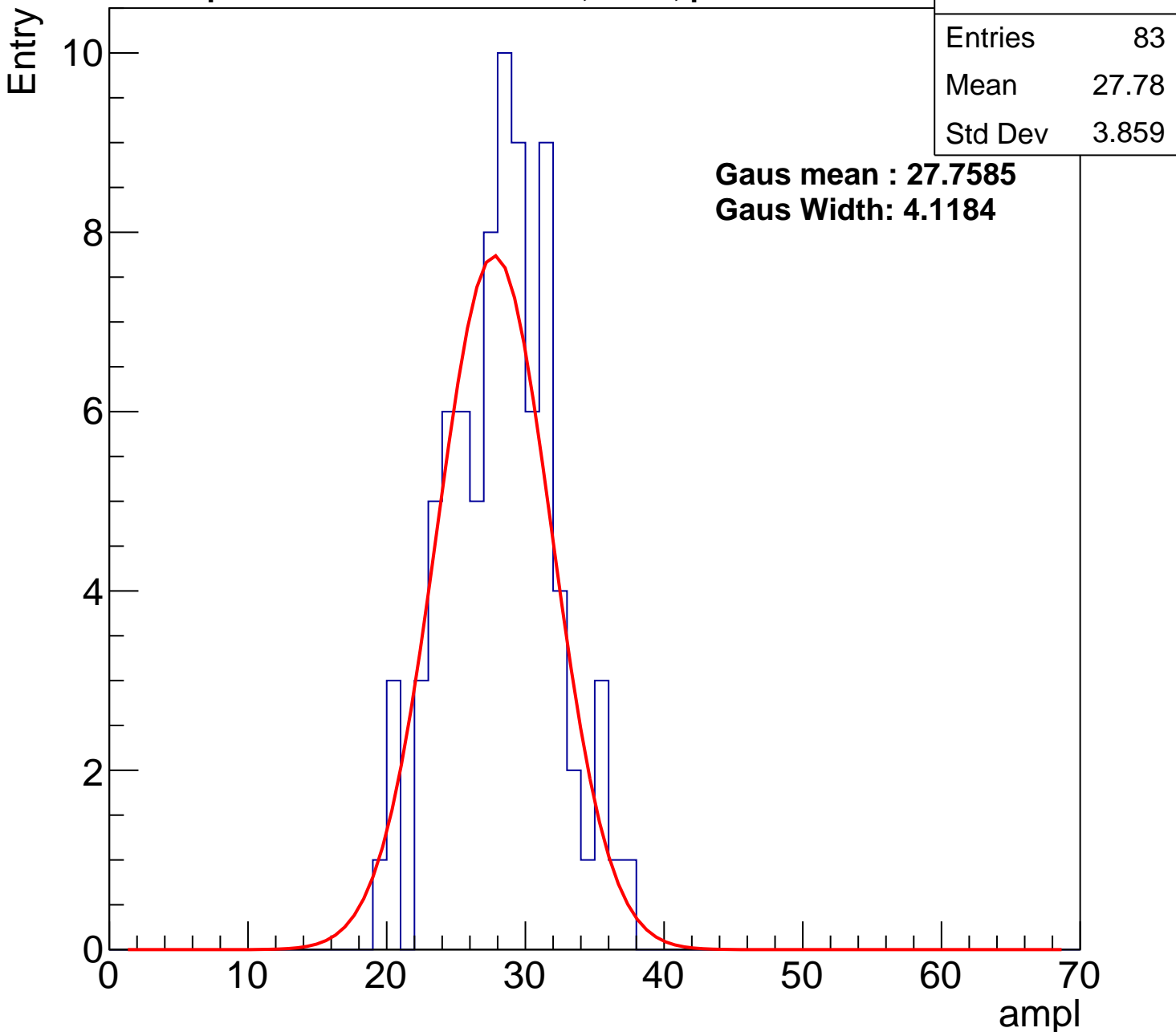
**Gaus Width: 4.1184**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U16-ch113, adc1

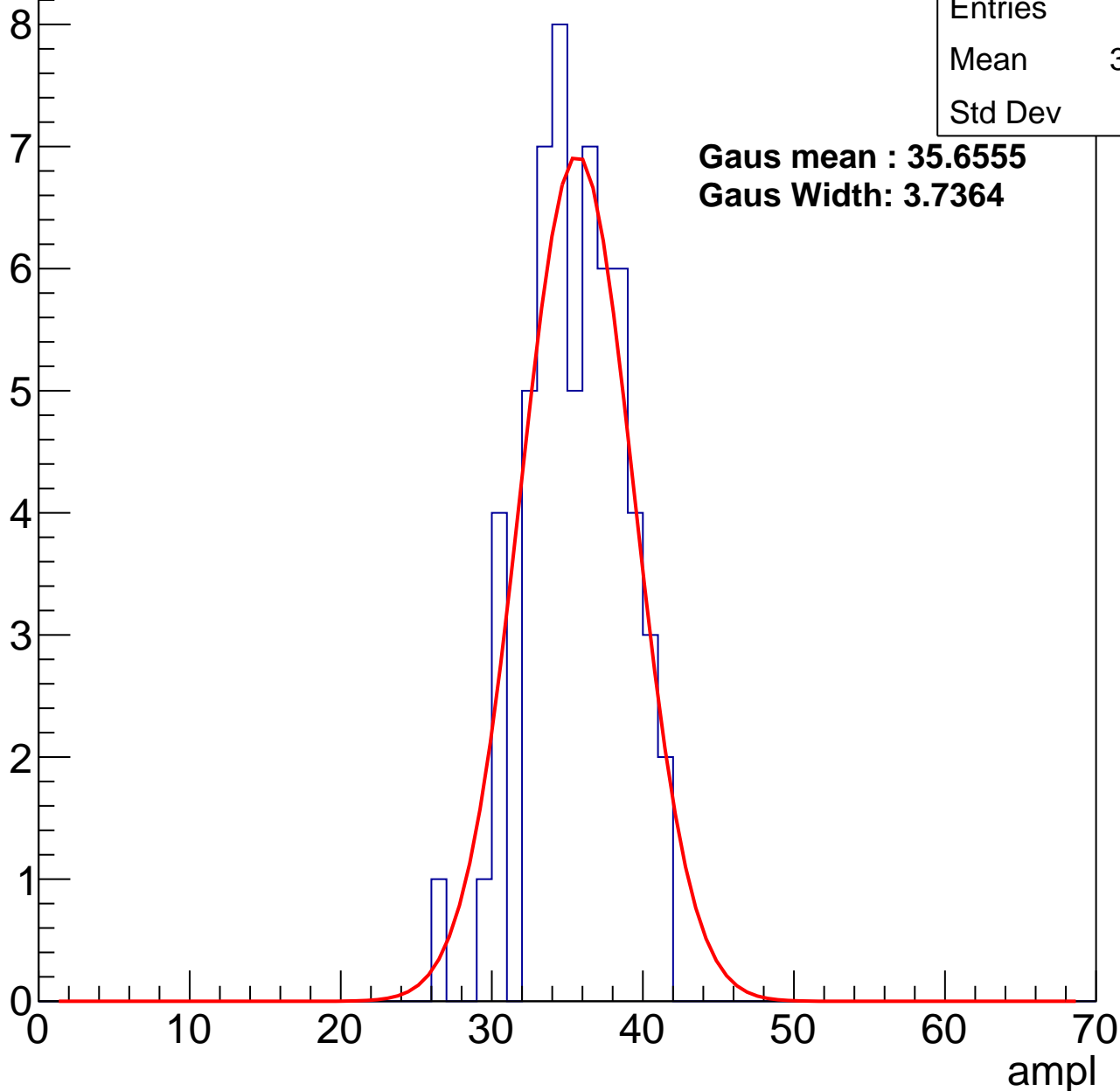
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	35.14
Std Dev	3.17

**Gaus mean : 35.6555**

**Gaus Width: 3.7364**



# B1L103S, U16-ch113, adc2

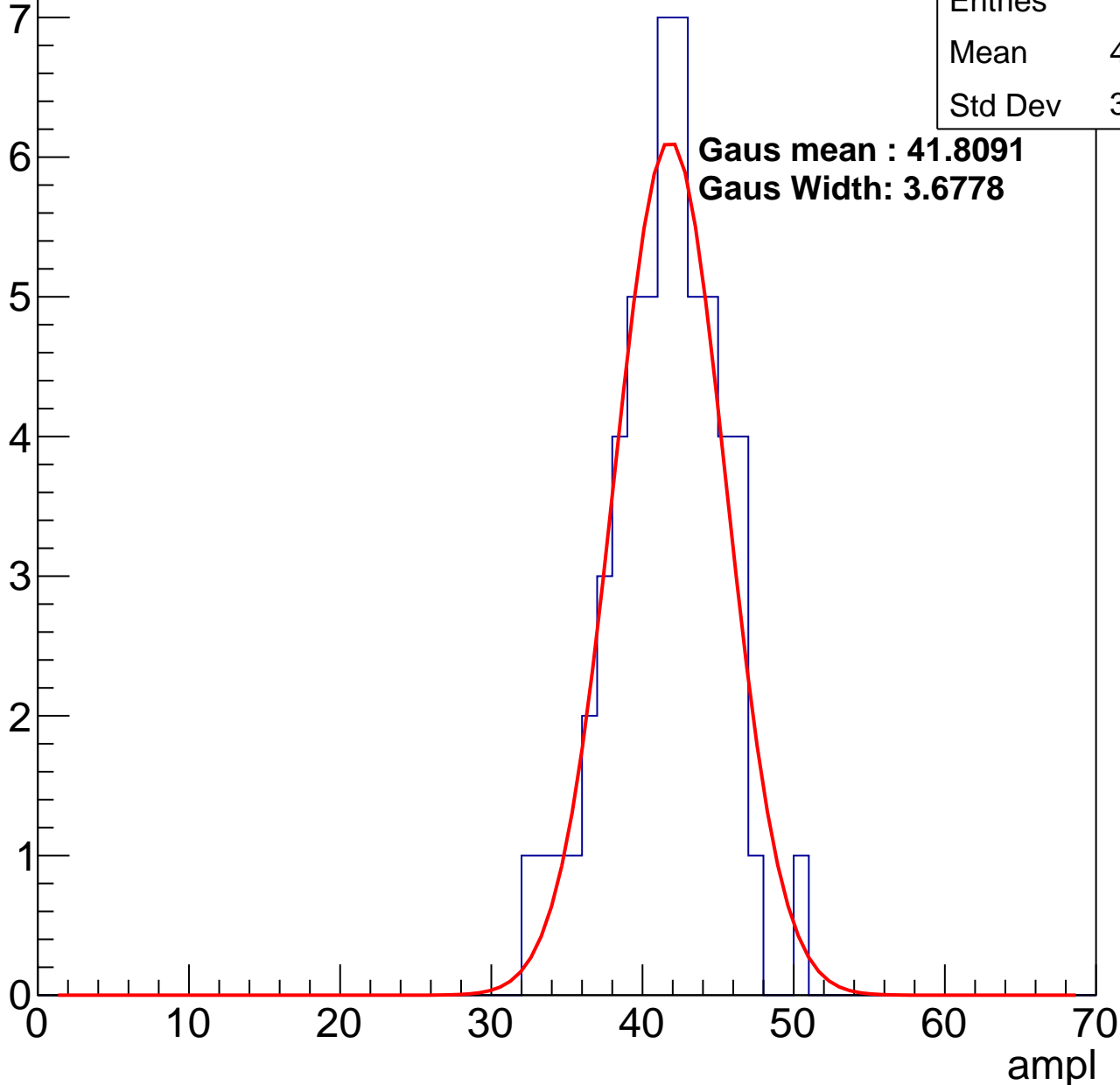
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	41.07
Std Dev	3.607

**Gaus mean : 41.8091**

**Gaus Width: 3.6778**

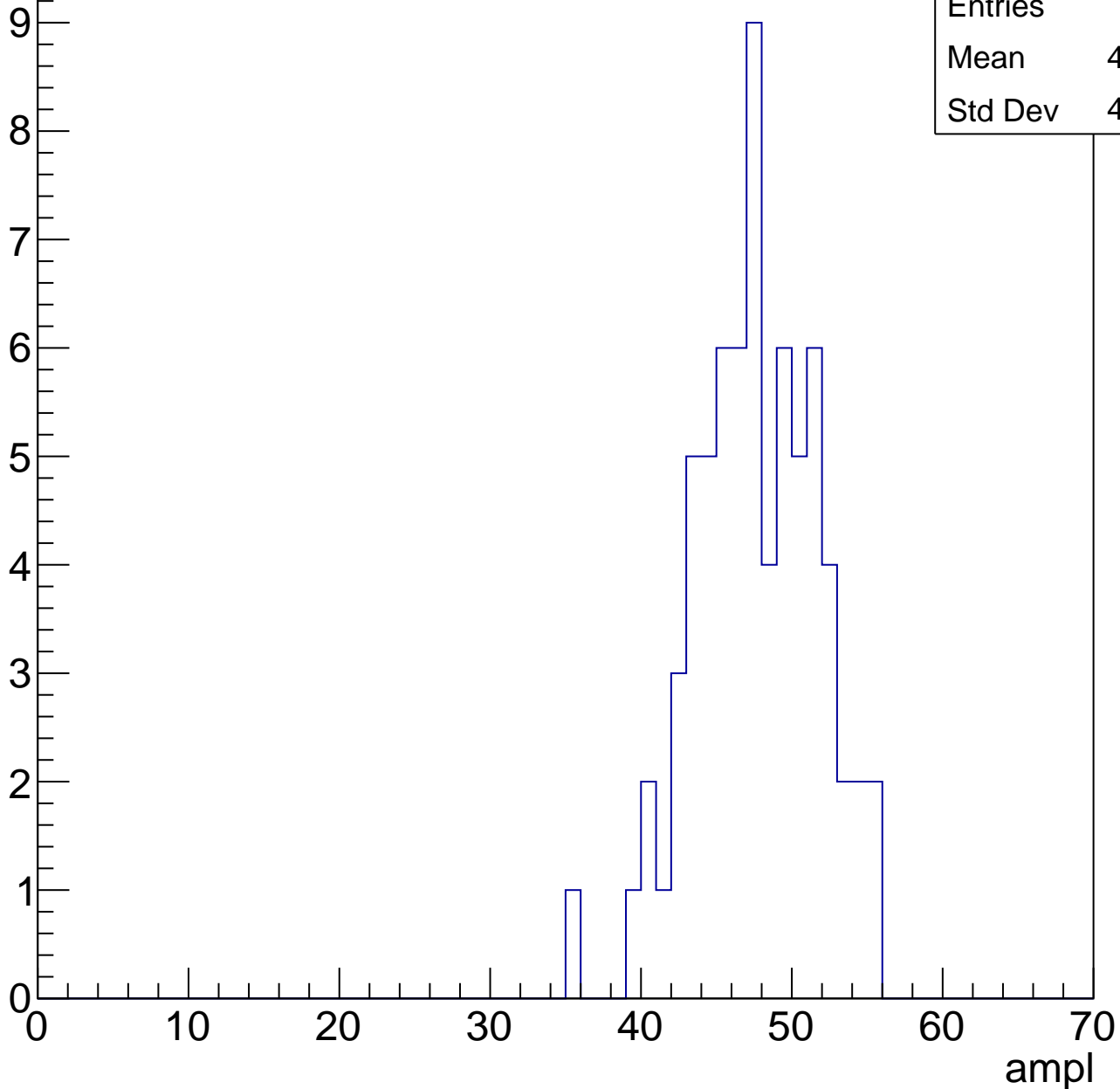


# B1L103S, U16-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	47.13
Std Dev	4.032

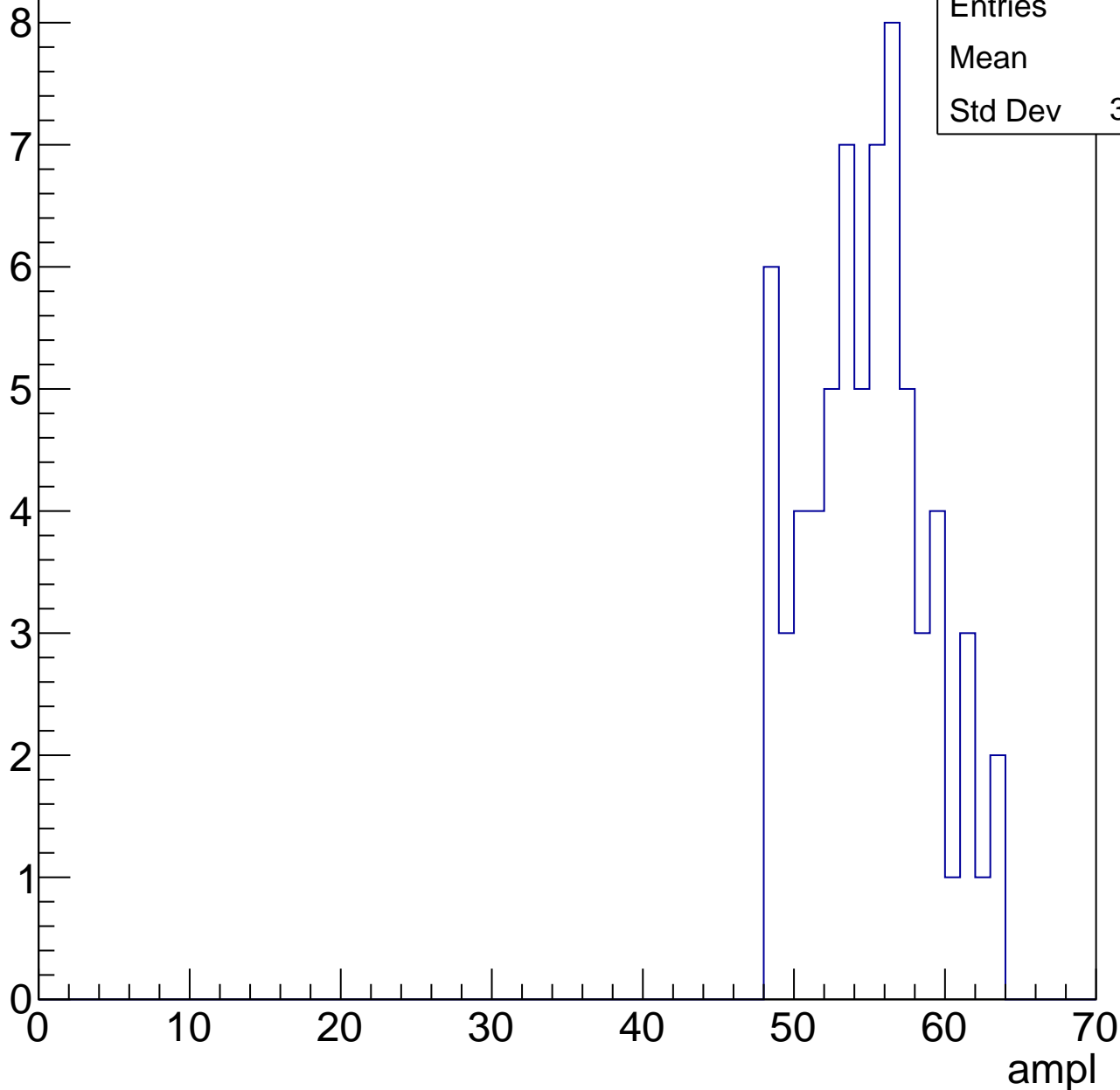


# B1L103S, U16-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	54.4
Std Dev	3.926

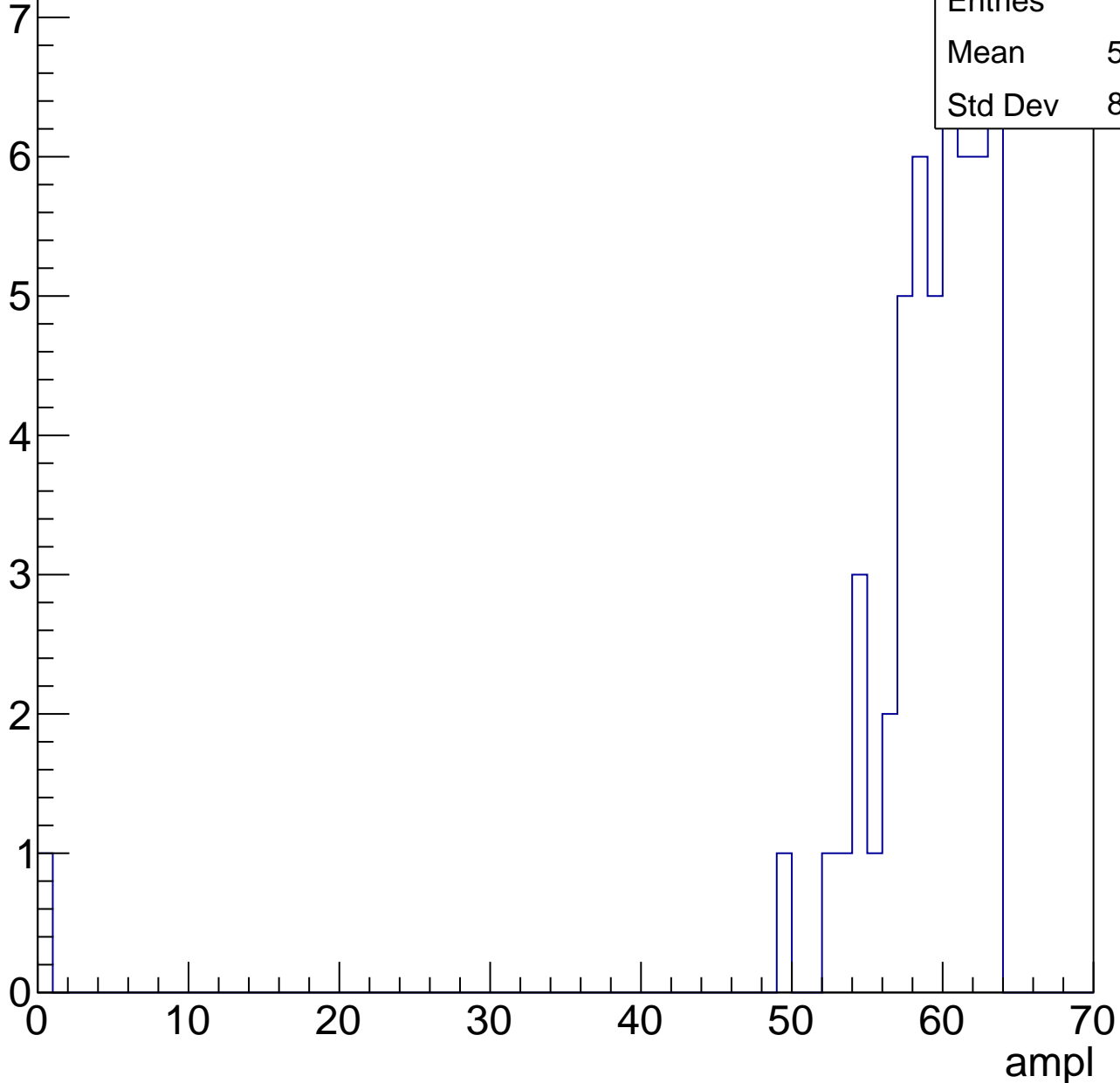


# B1L103S, U16-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

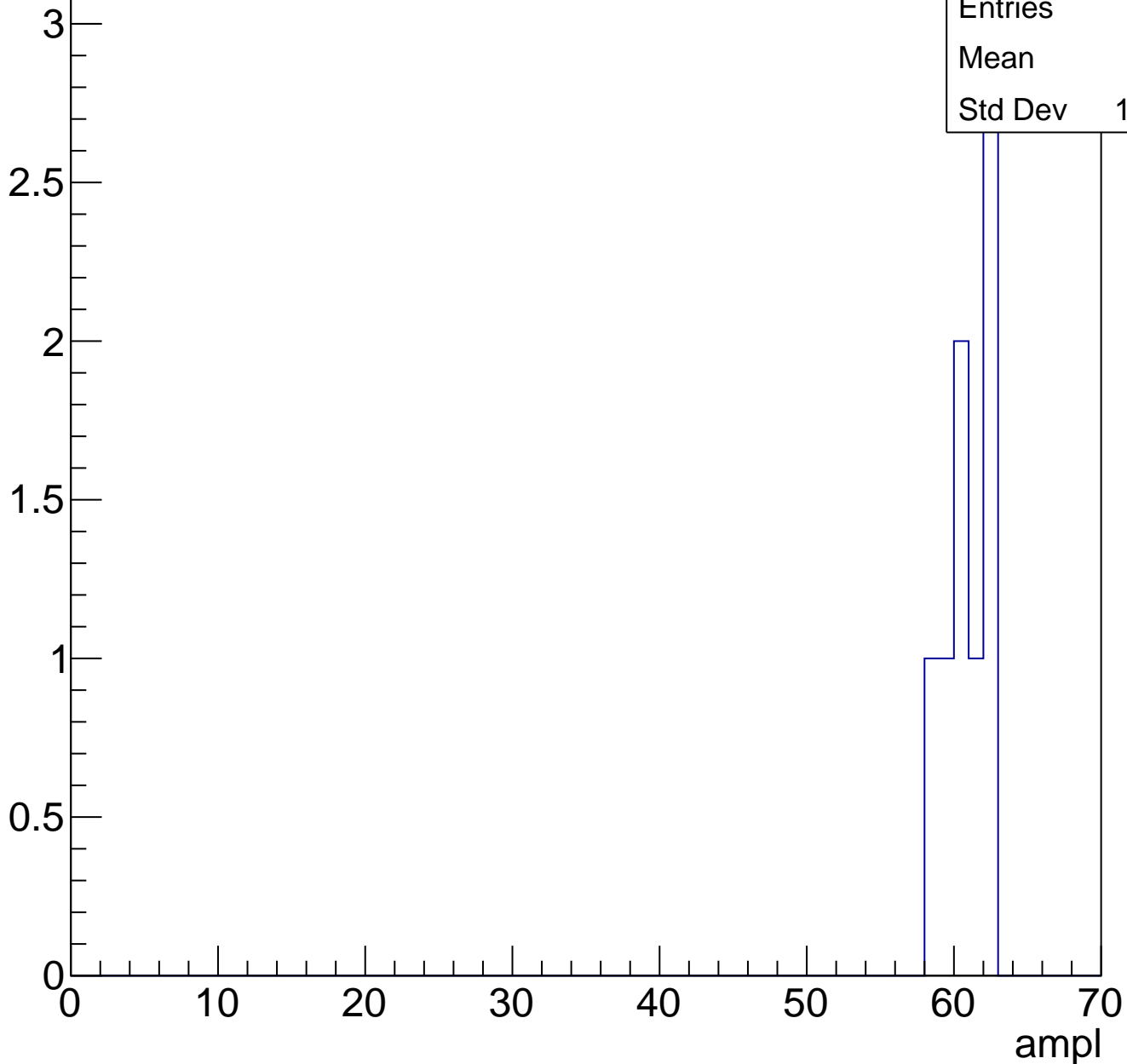
Entries	52
Mean	57.88
Std Dev	8.697



# B1L103S, U16-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch114, adc0

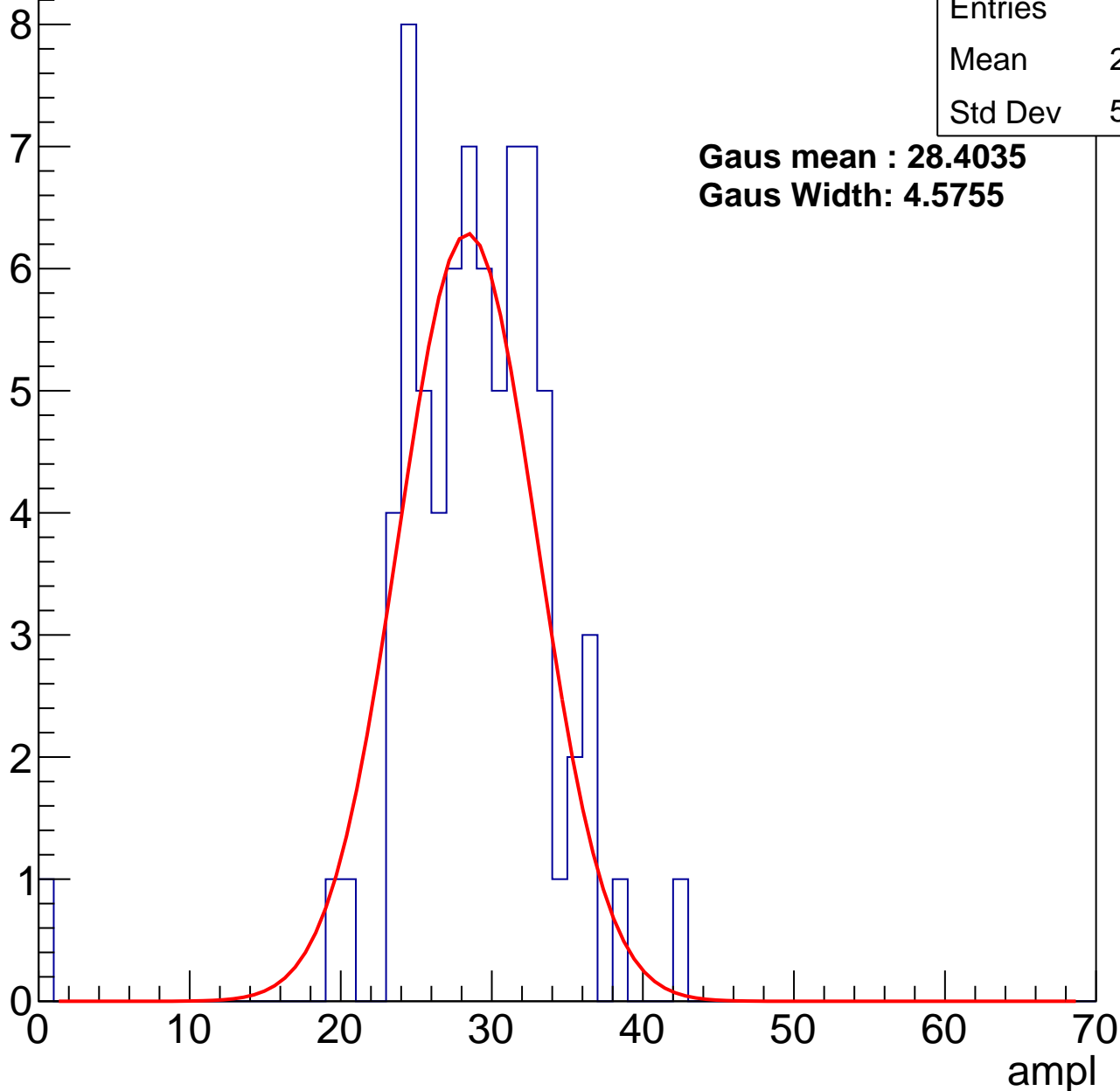
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	28.43
Std Dev	5.365

**Gaus mean : 28.4035**

**Gaus Width: 4.5755**



# B1L103S, U16-ch114, adc1

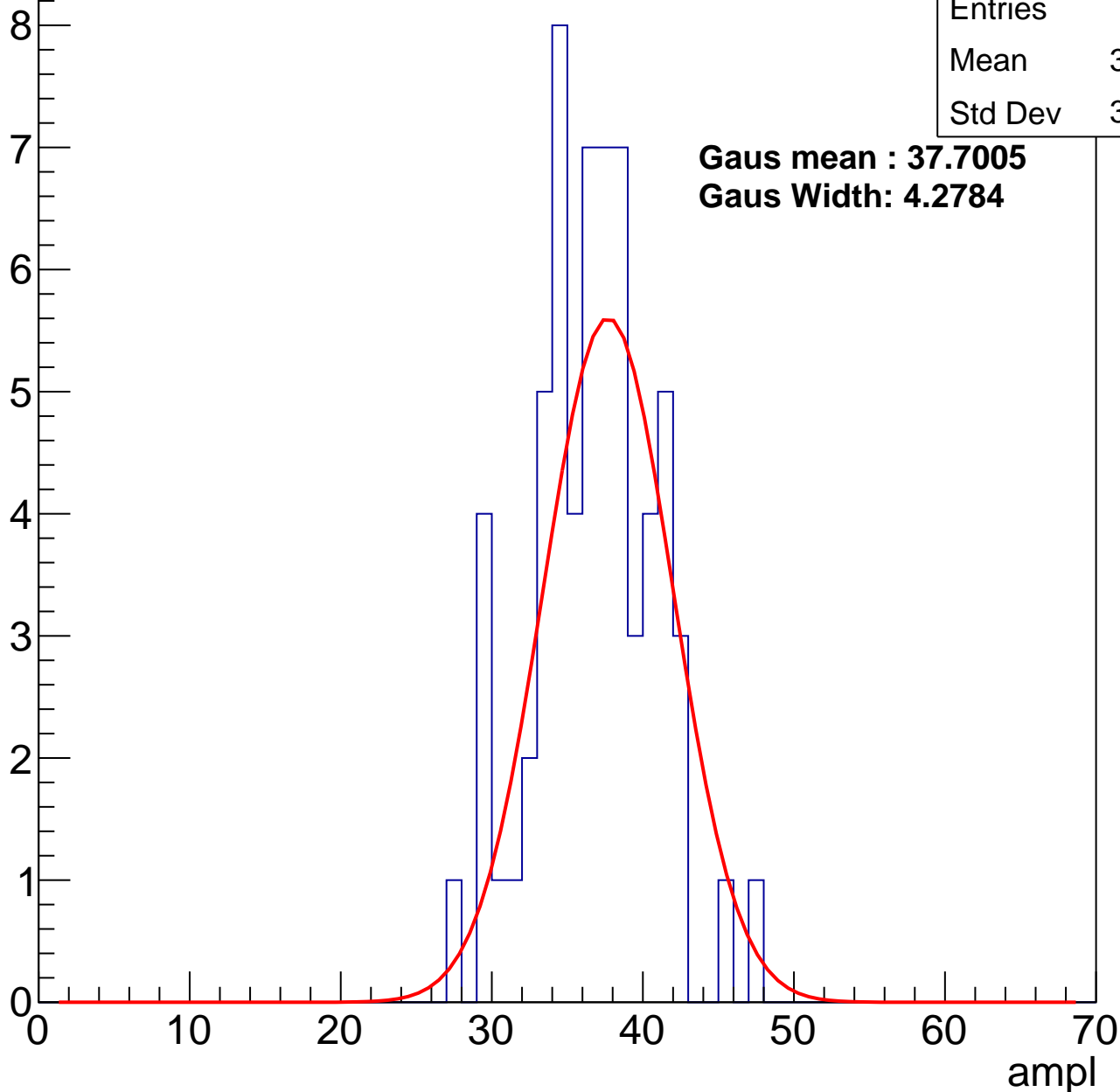
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	36.28
Std Dev	3.967

**Gaus mean : 37.7005**

**Gaus Width: 4.2784**



# B1L103S, U16-ch114, adc2

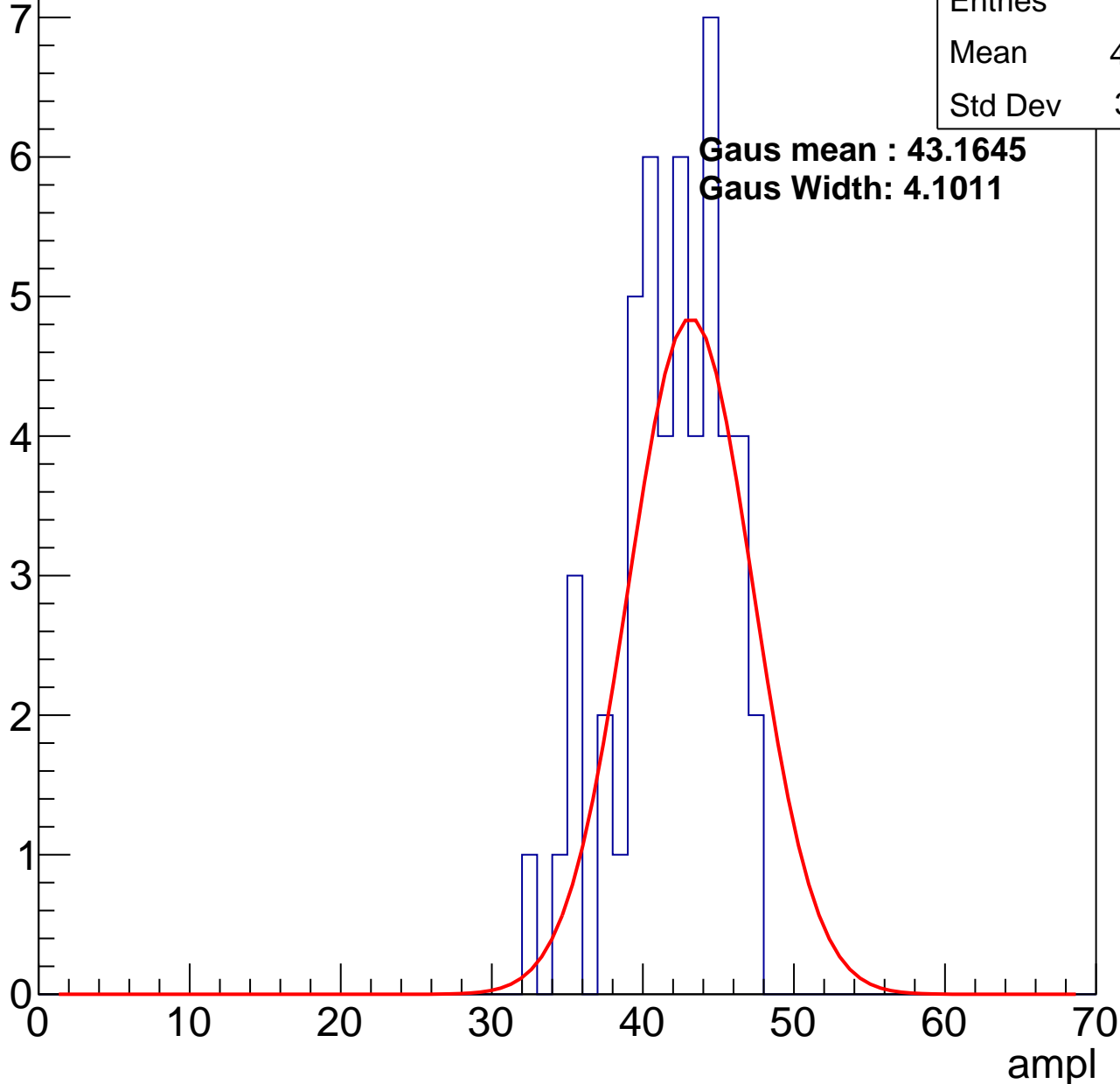
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	41.44
Std Dev	3.511

**Gaus mean : 43.1645**

**Gaus Width: 4.1011**



# B1L103S, U16-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

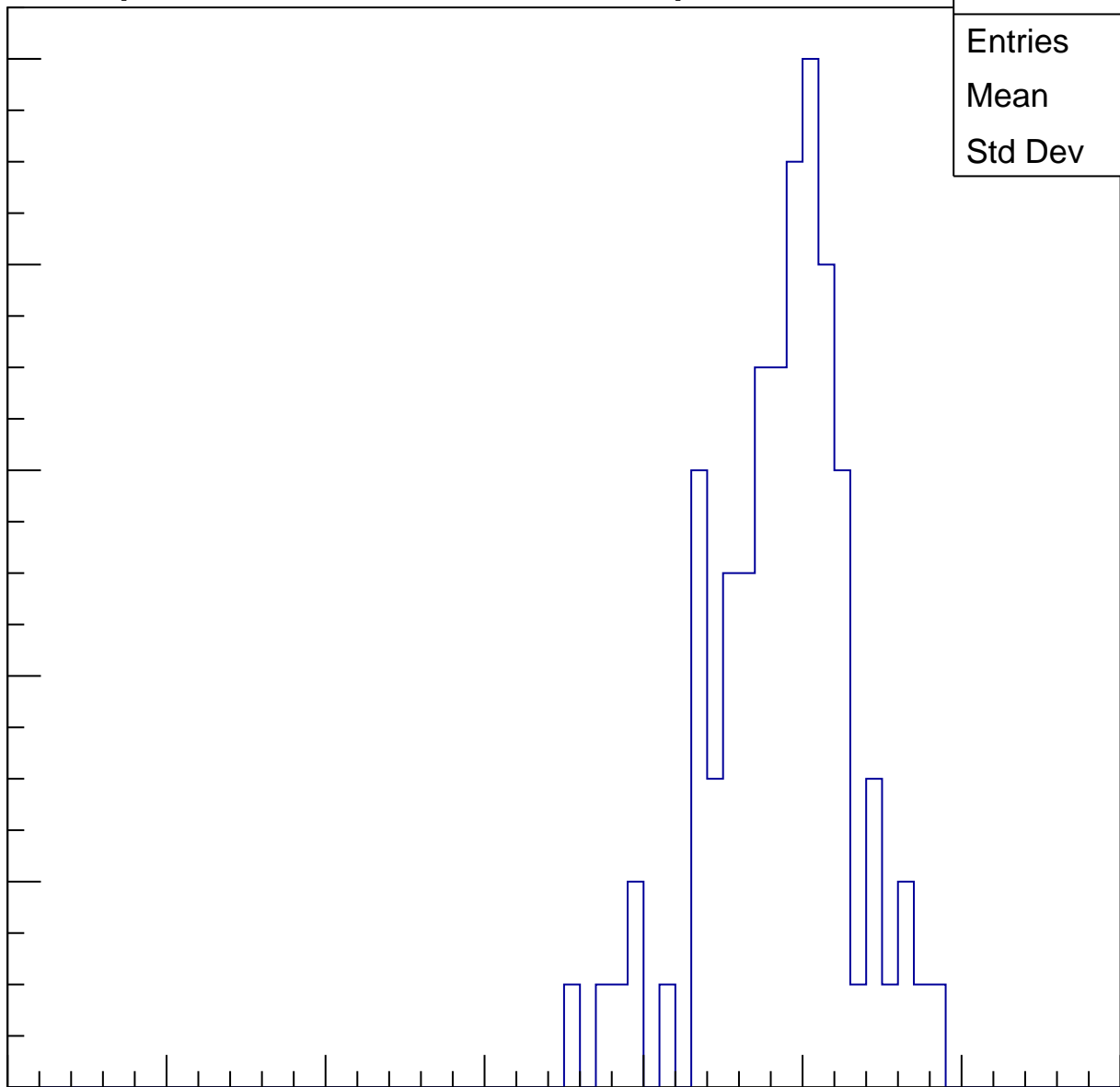
Entries	81
Mean	48.11
Std Dev	4.414

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

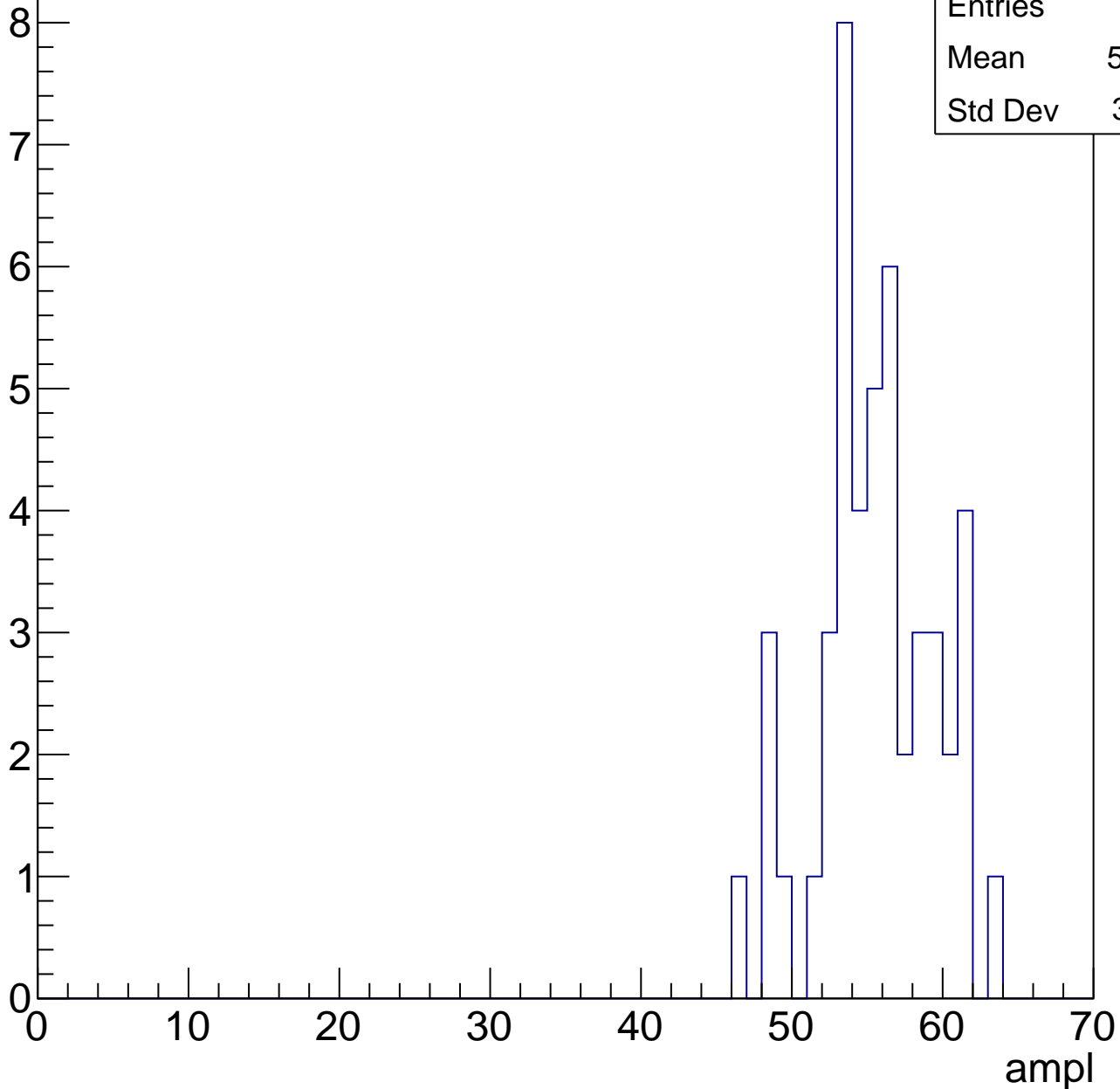


# B1L103S, U16-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

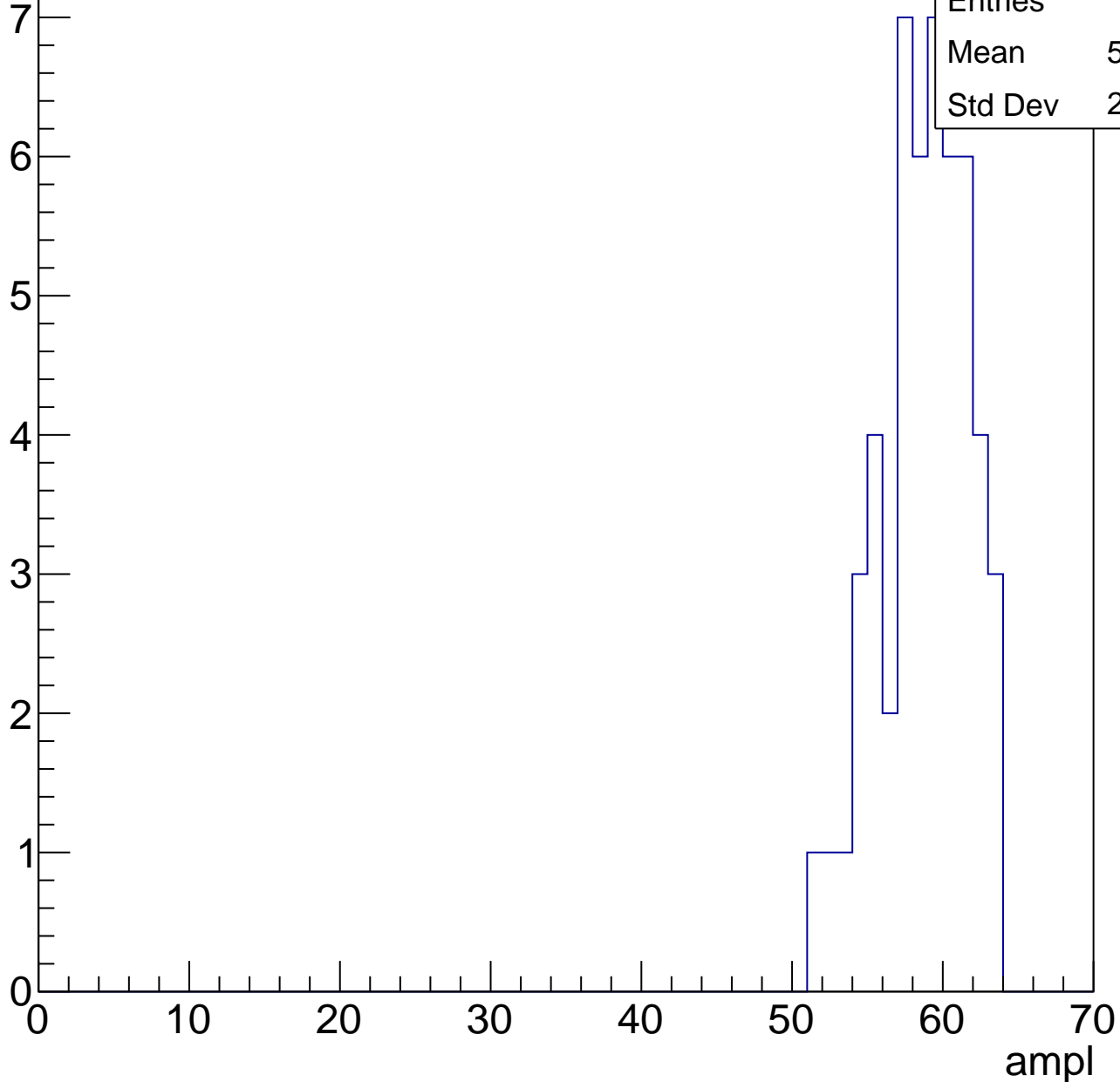
Entries	47
Mean	55.09
Std Dev	3.831



# B1L103S, U16-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

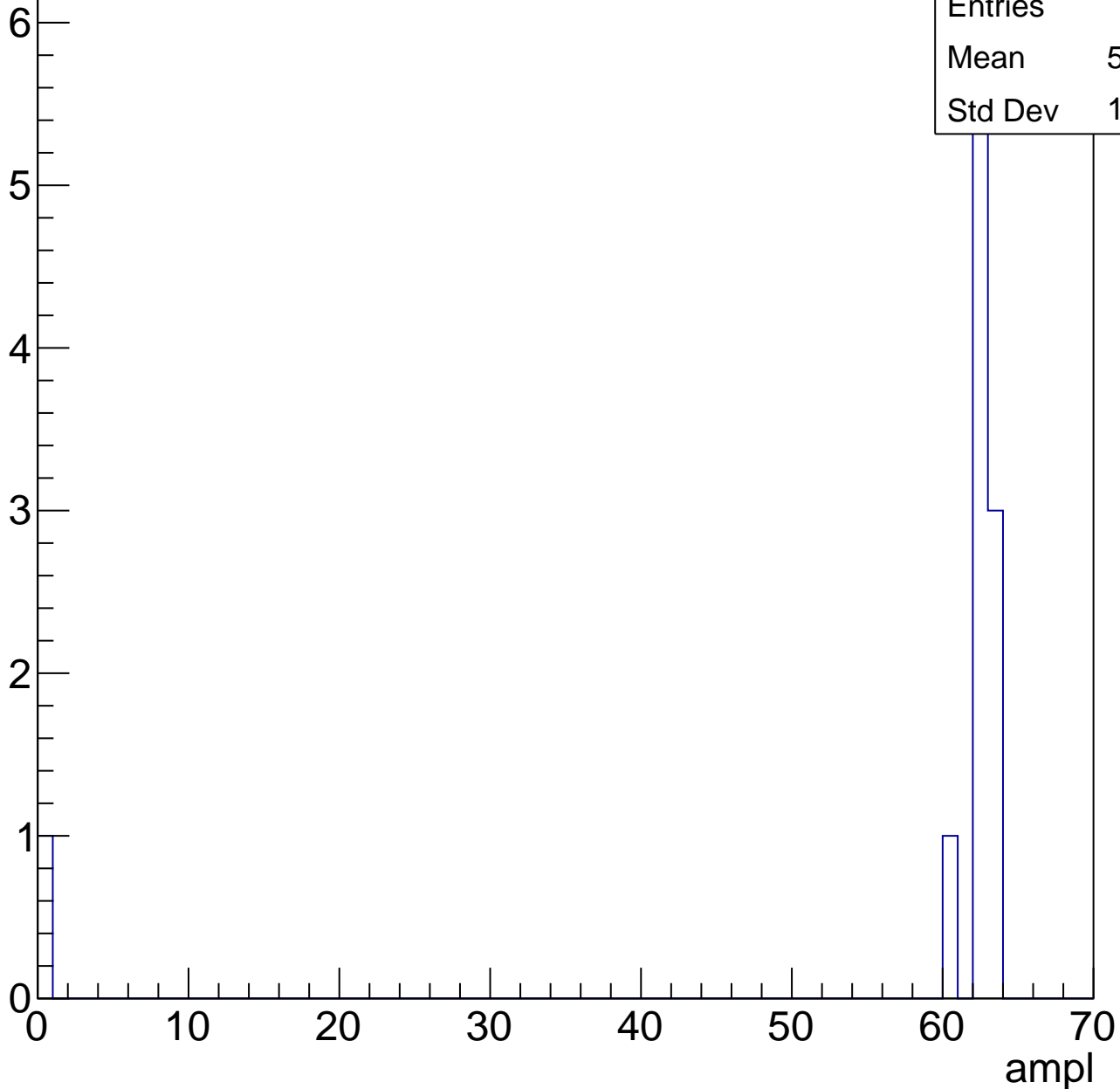


# B1L103S, U16-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	11
Mean	56.45
Std Dev	17.87

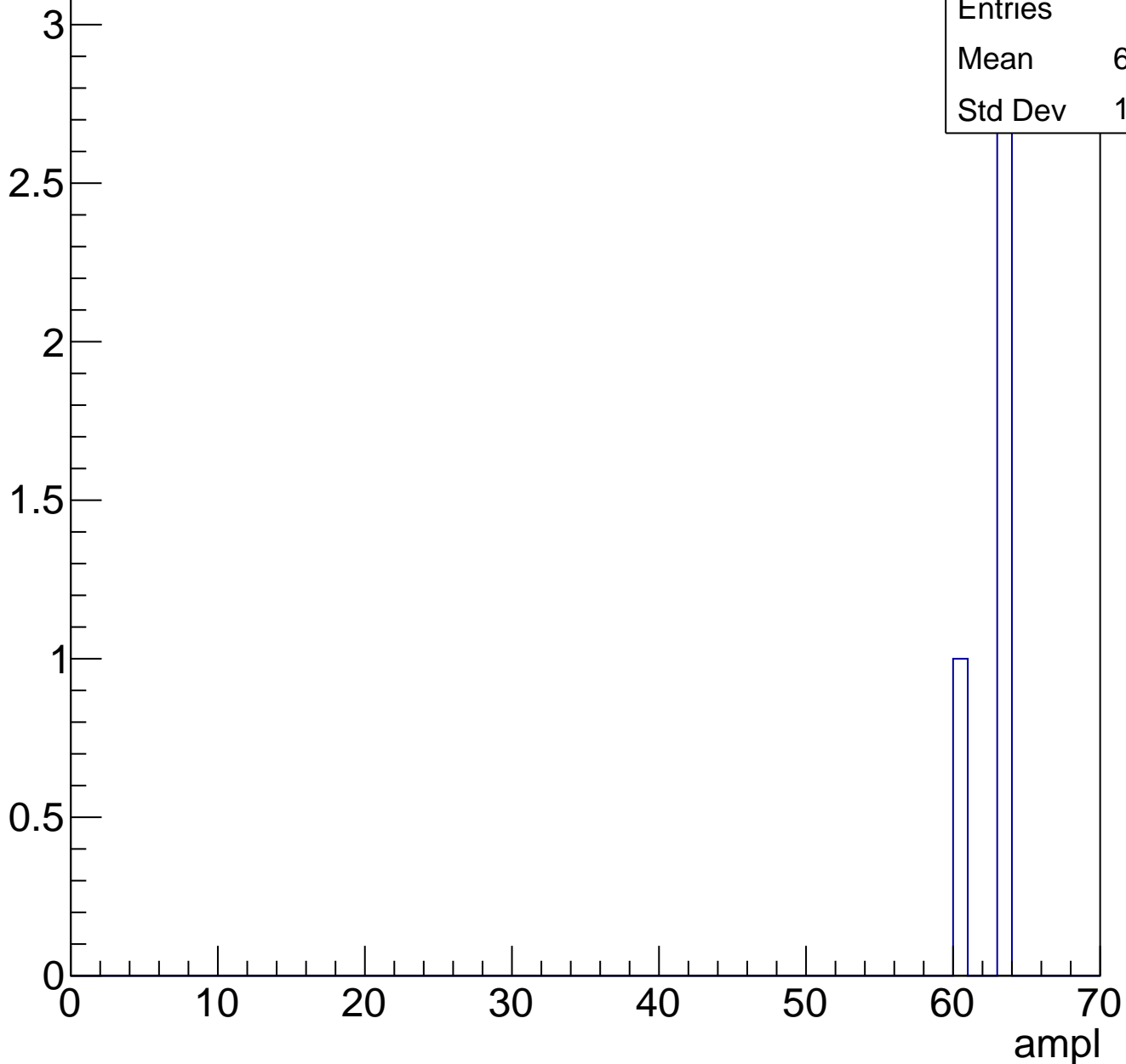




# B1L103S, U16-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch115, adc0

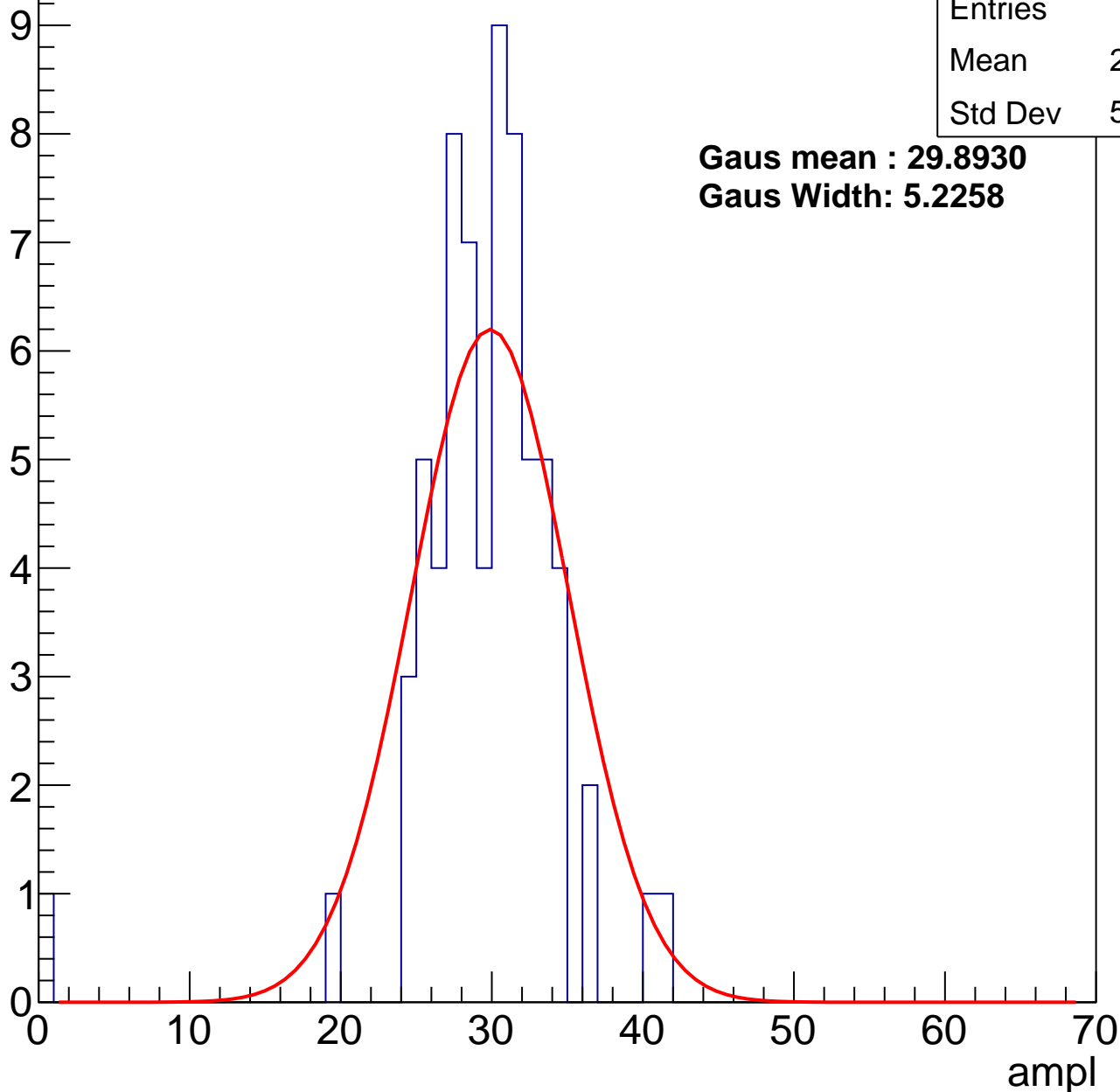
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	29.12
Std Dev	5.144

**Gaus mean : 29.8930**

**Gaus Width: 5.2258**



# B1L103S, U16-ch115, adc1

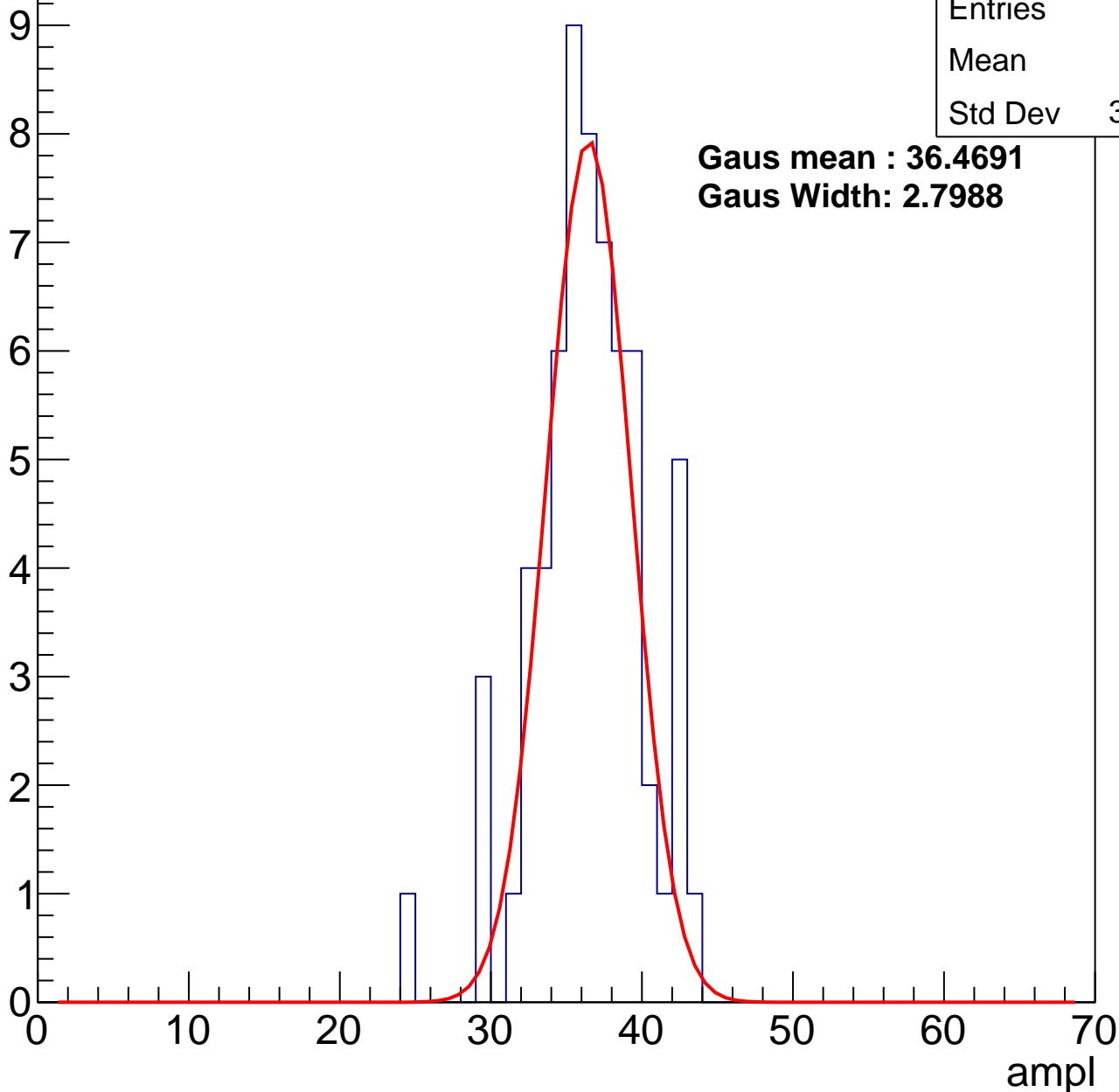
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	36
Std Dev	3.579

**Gaus mean : 36.4691**

**Gaus Width: 2.7988**



# B1L103S, U16-ch115, adc2

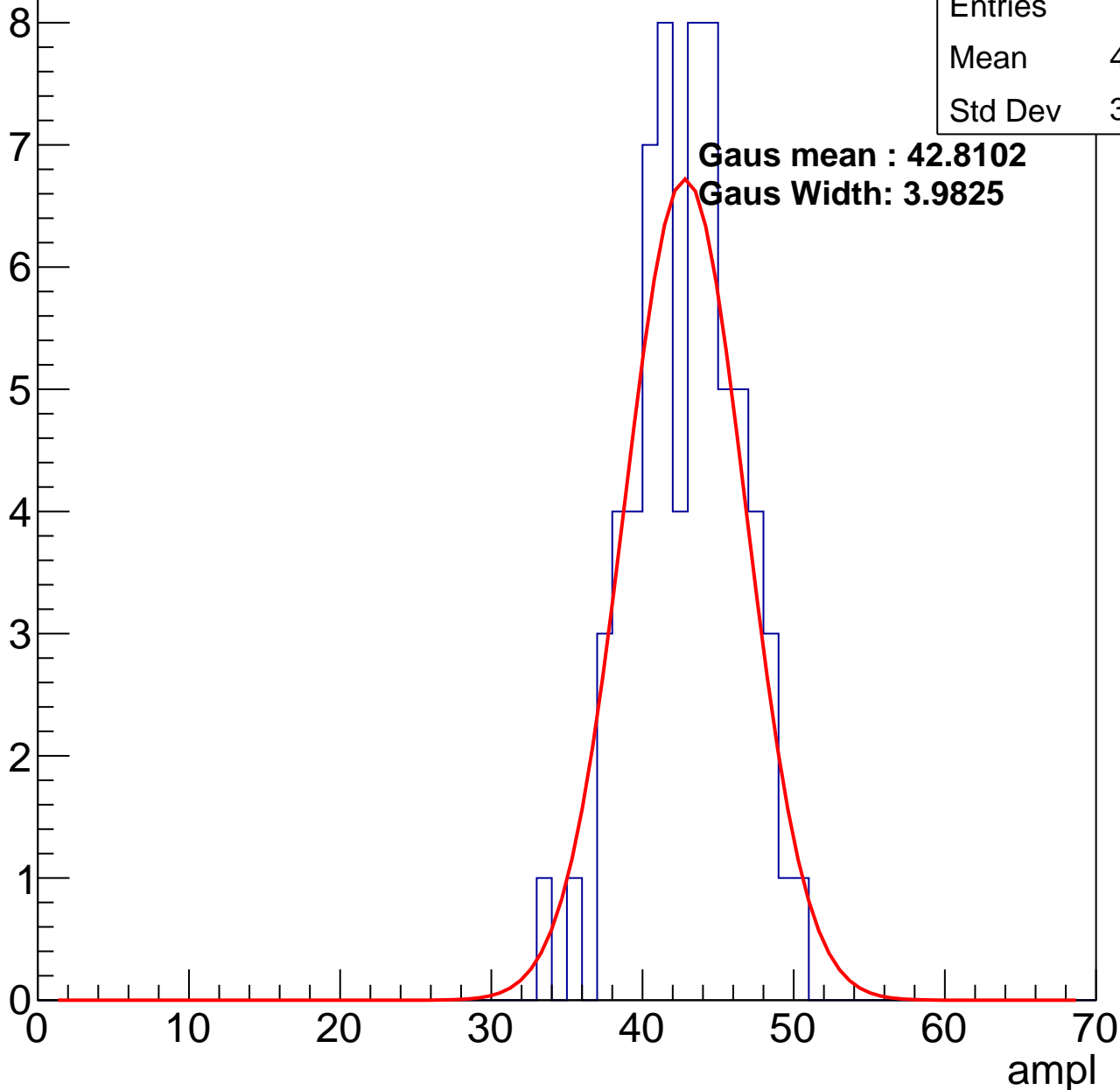
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	42.46
Std Dev	3.483

**Gaus mean : 42.8102**

**Gaus Width: 3.9825**

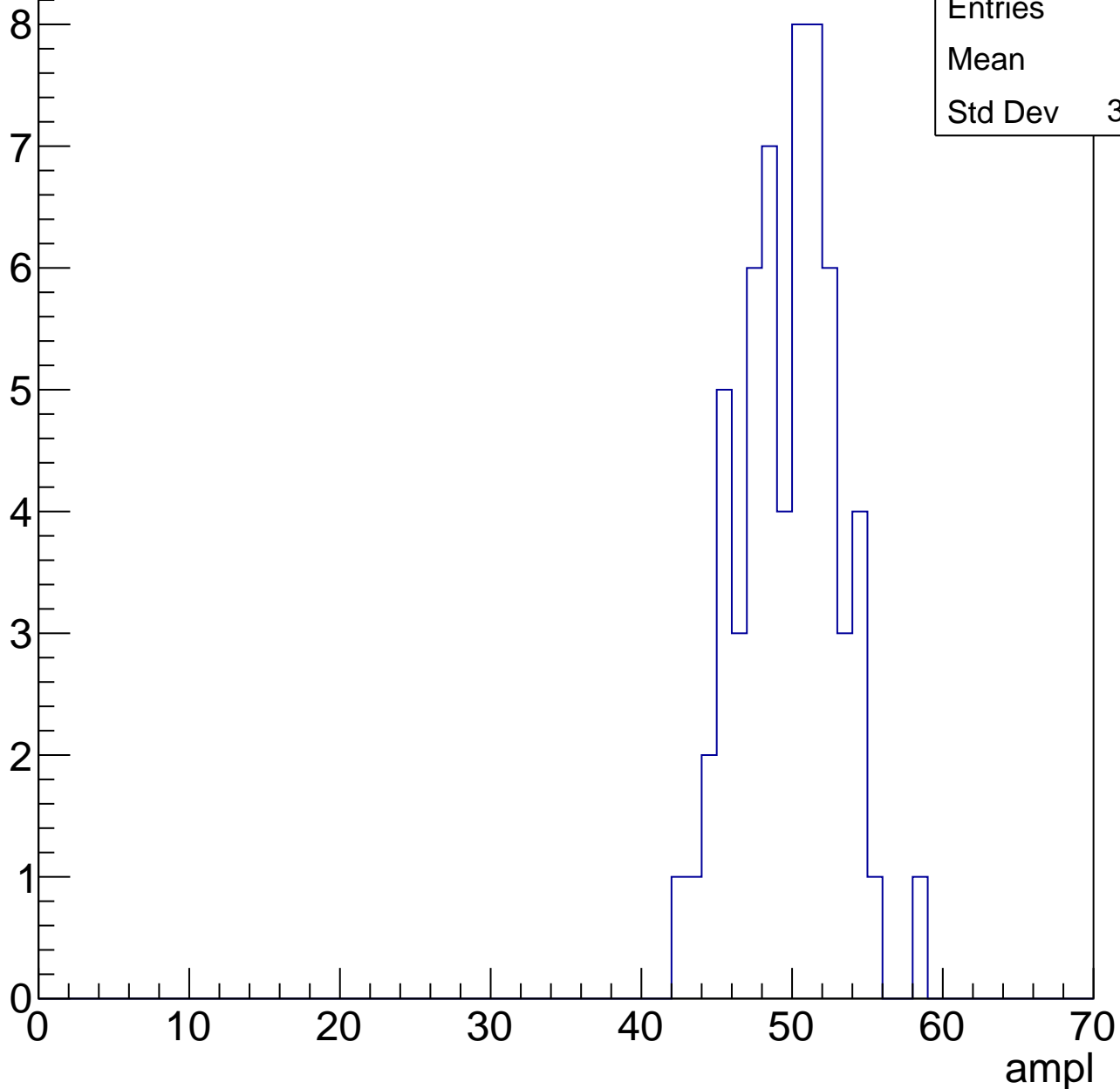


# B1L103S, U16-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	49.3
Std Dev	3.232



# B1L103S, U16-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

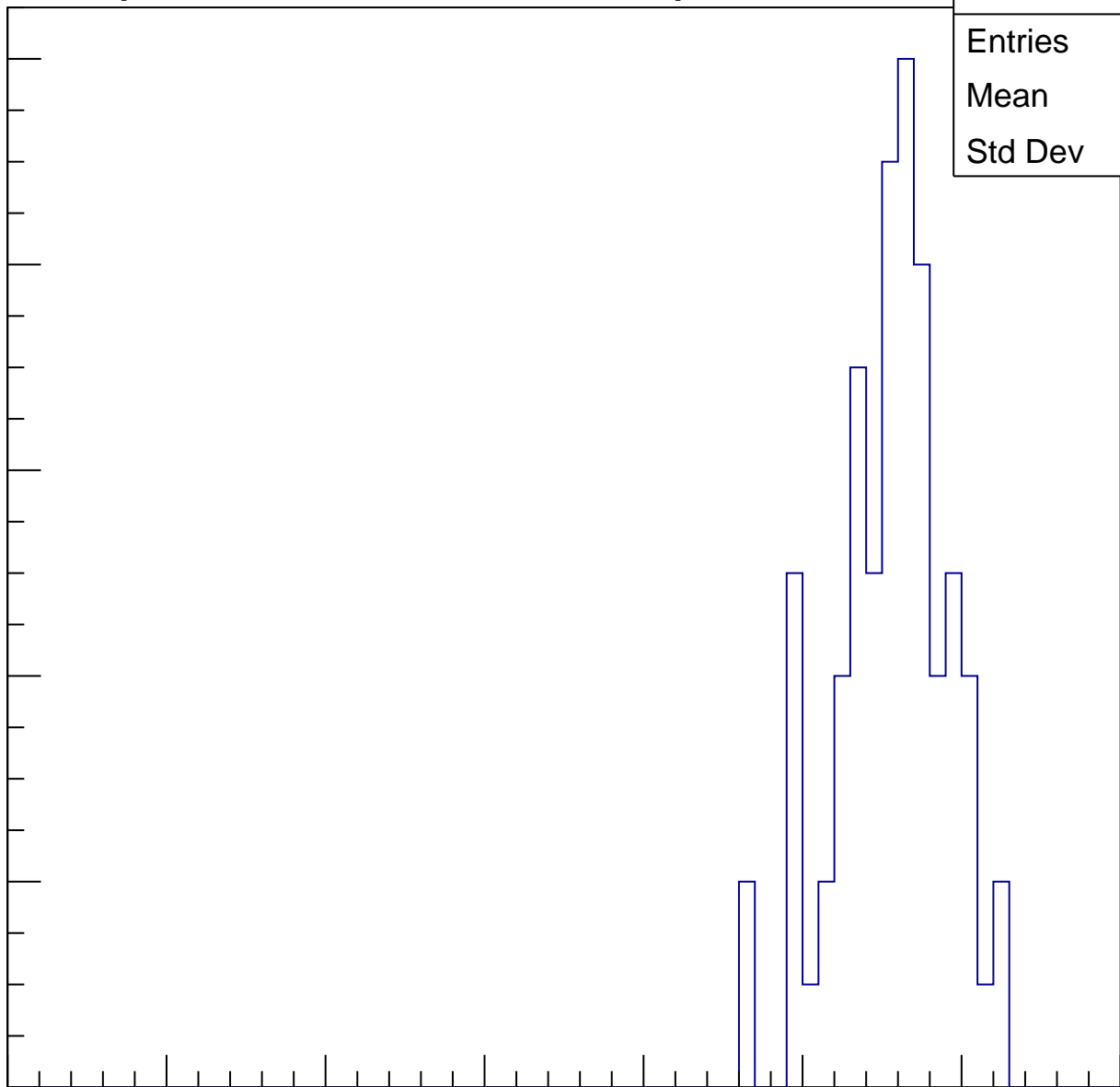
Entries	69
Mean	55.09
Std Dev	3.529

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

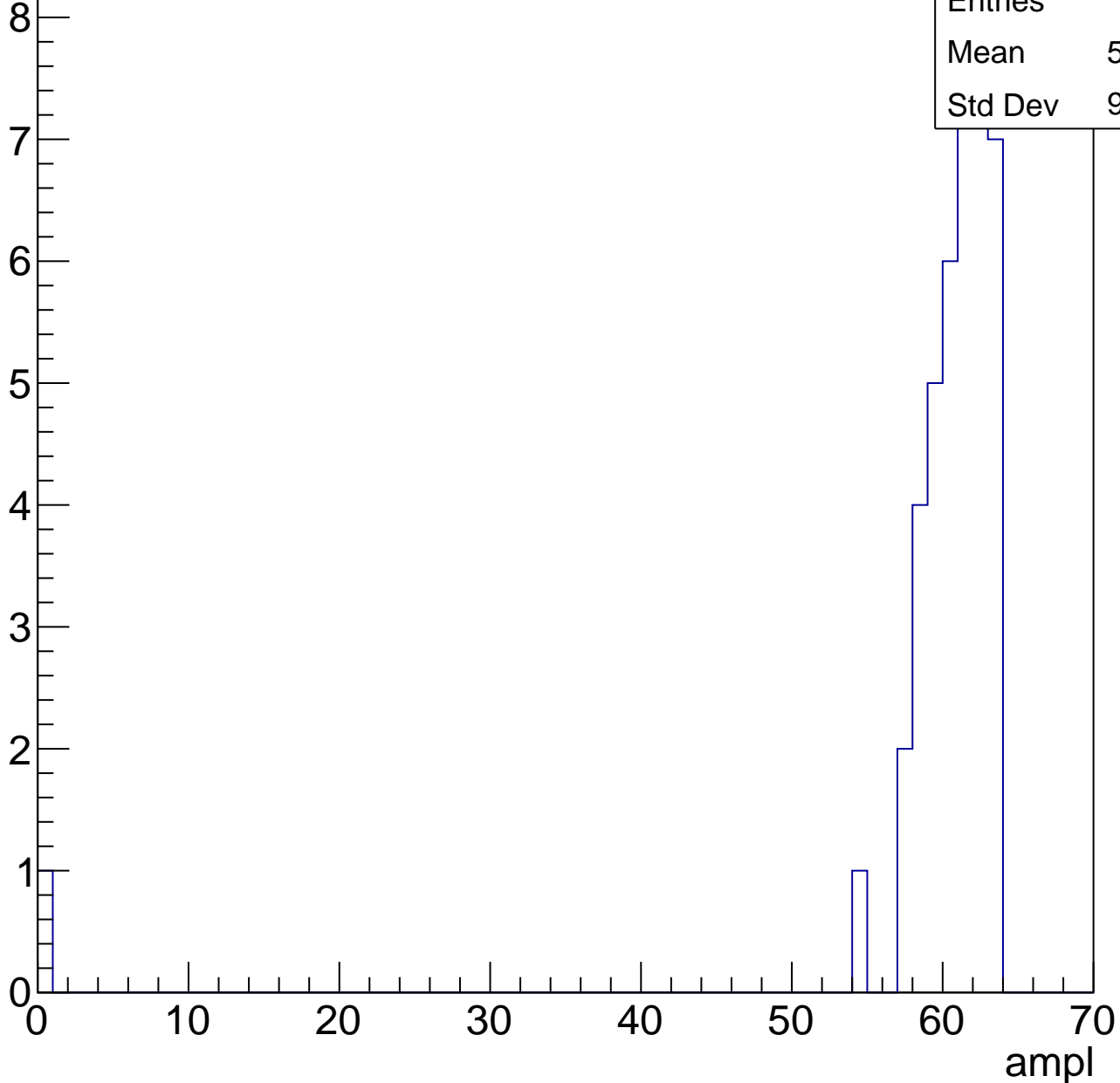


# B1L103S, U16-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

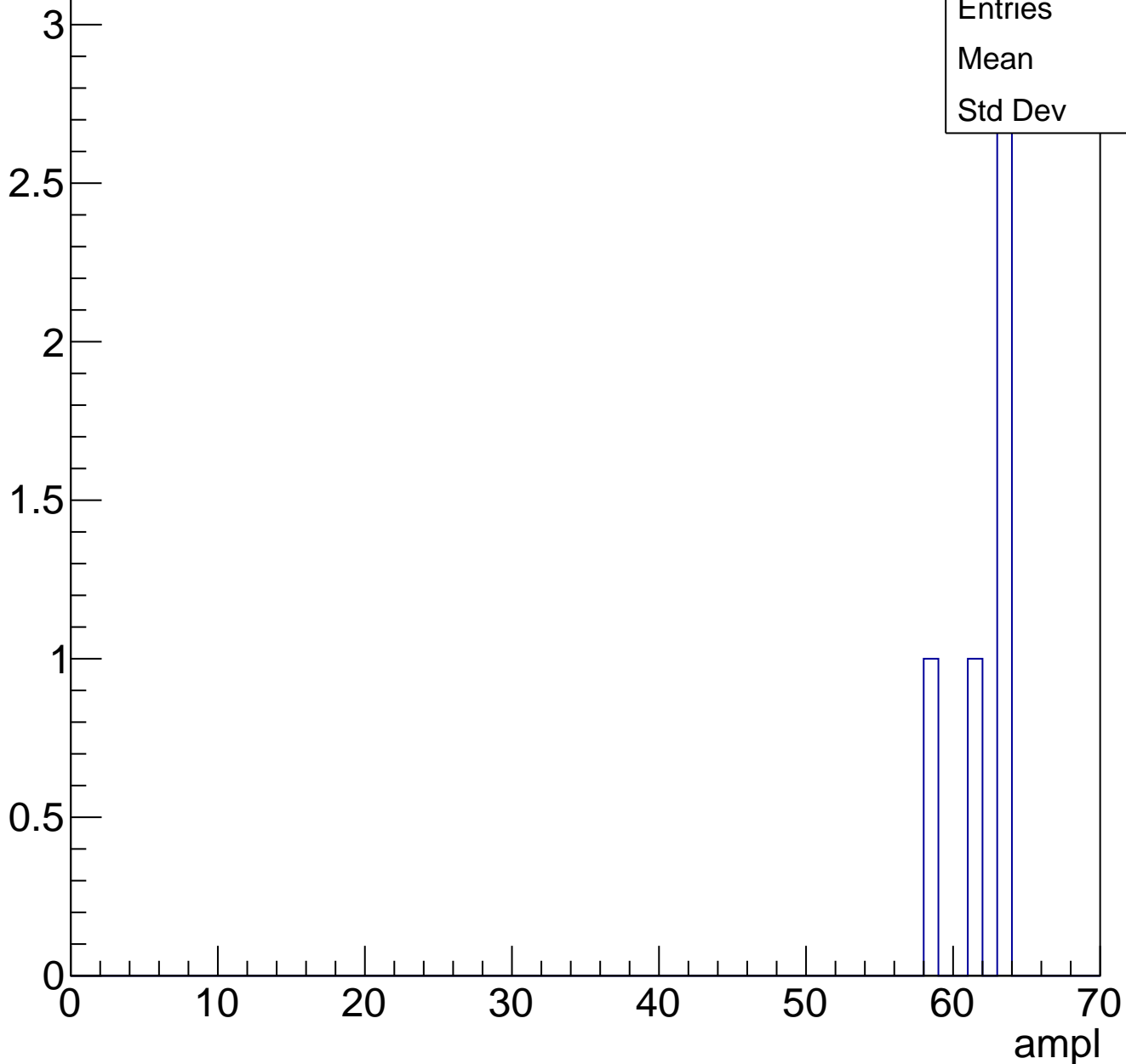
Entries	42
Mean	59.05
Std Dev	9.436



# B1L103S, U16-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U16-ch116, adc0

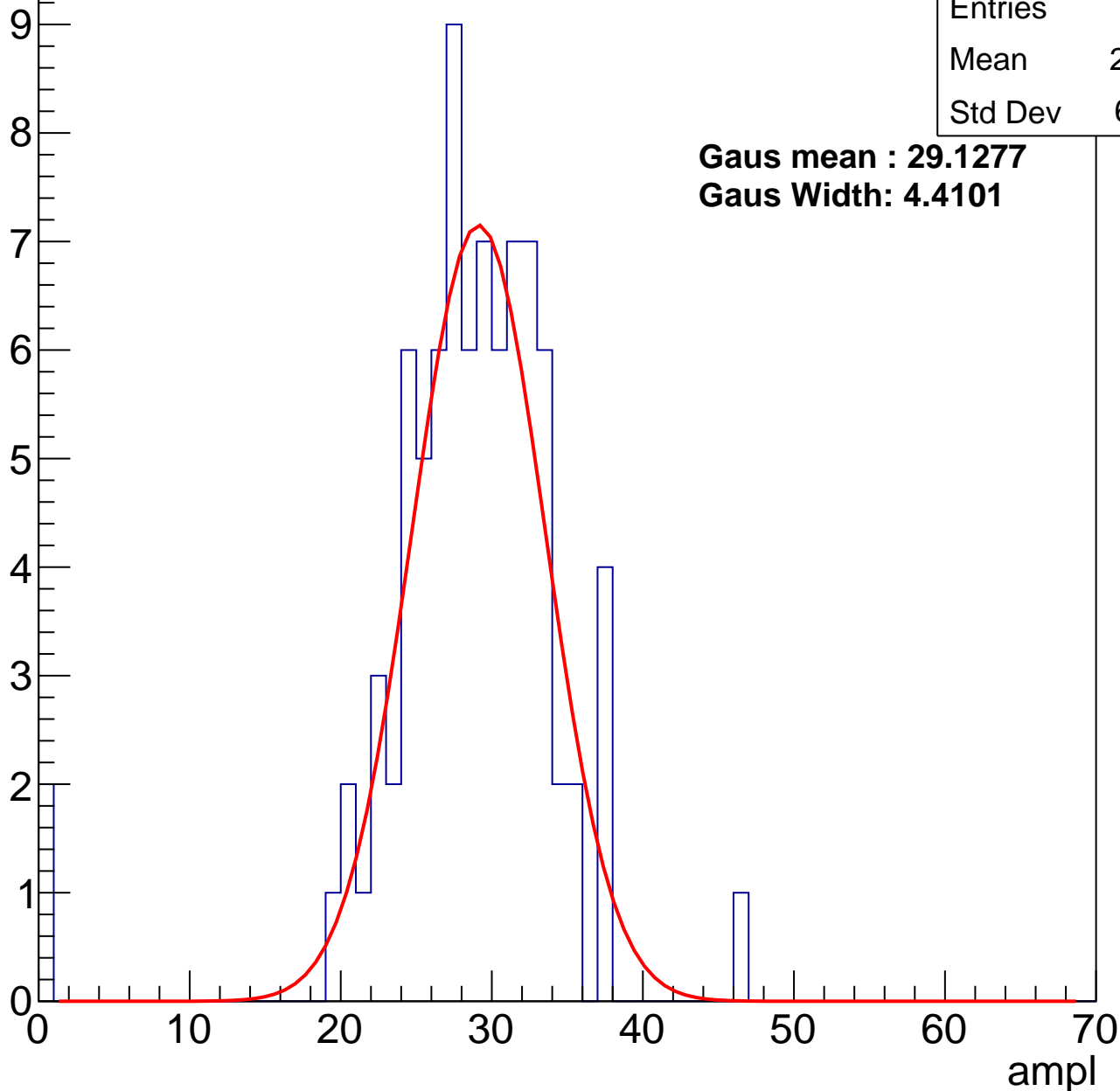
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	85
Mean	28.02
Std Dev	6.261

**Gaus mean : 29.1277**

**Gaus Width: 4.4101**



# B1L103S, U16-ch116, adc1

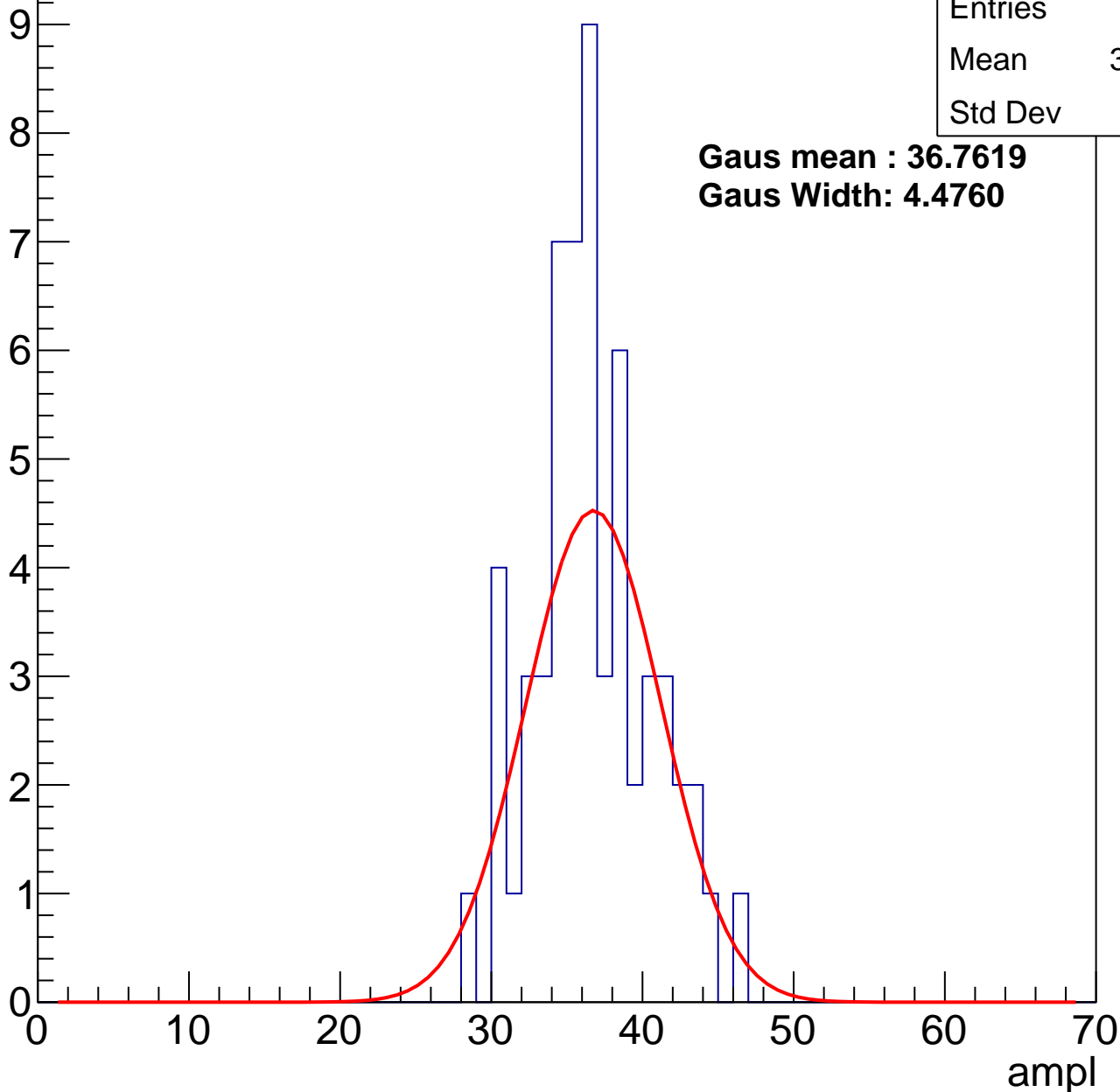
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	36.22
Std Dev	3.81

**Gaus mean : 36.7619**

**Gaus Width: 4.4760**



# B1L103S, U16-ch116, adc2

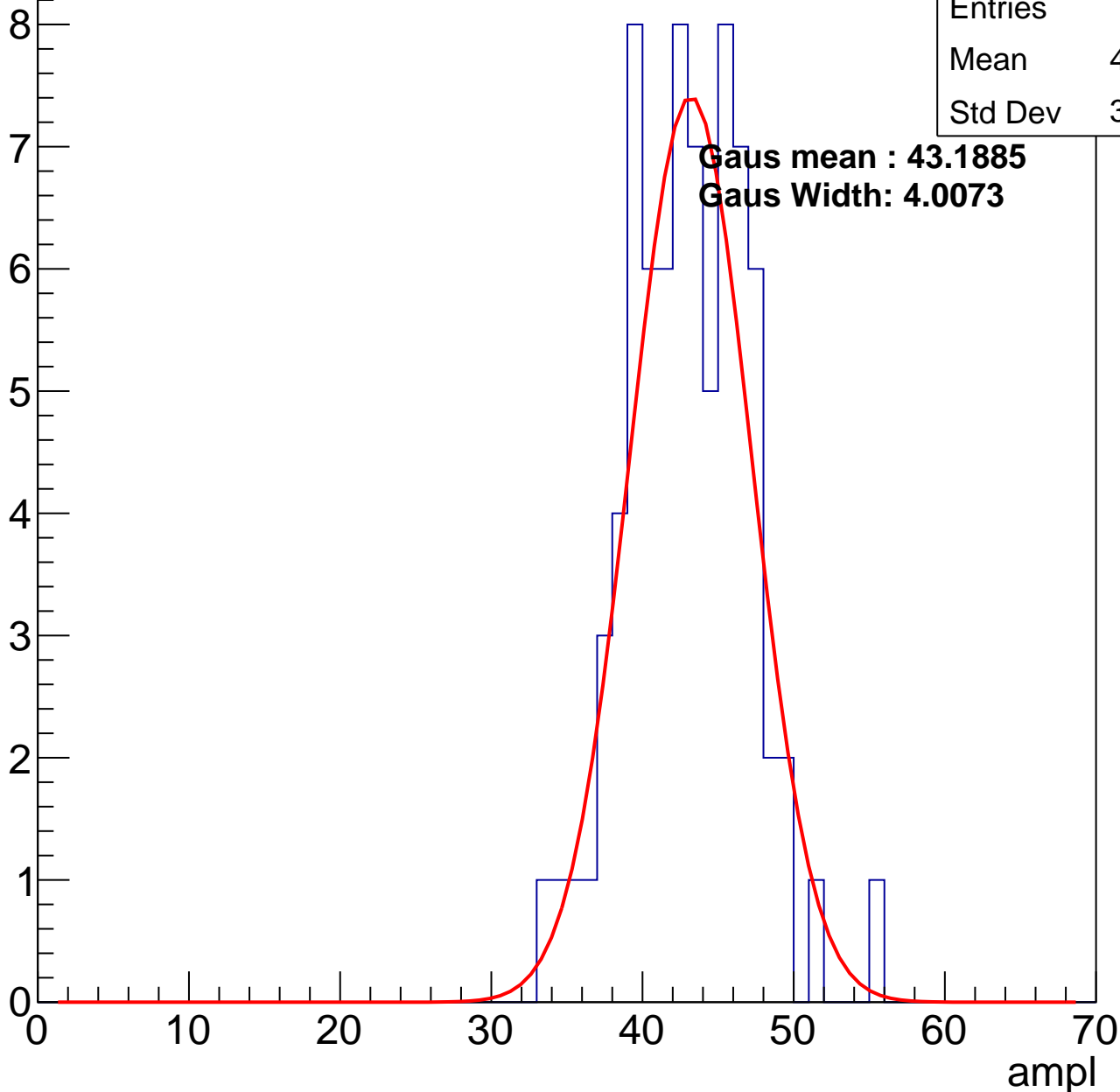
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	42.56
Std Dev	3.966

**Gaus mean : 43.1885**

**Gaus Width: 4.0073**

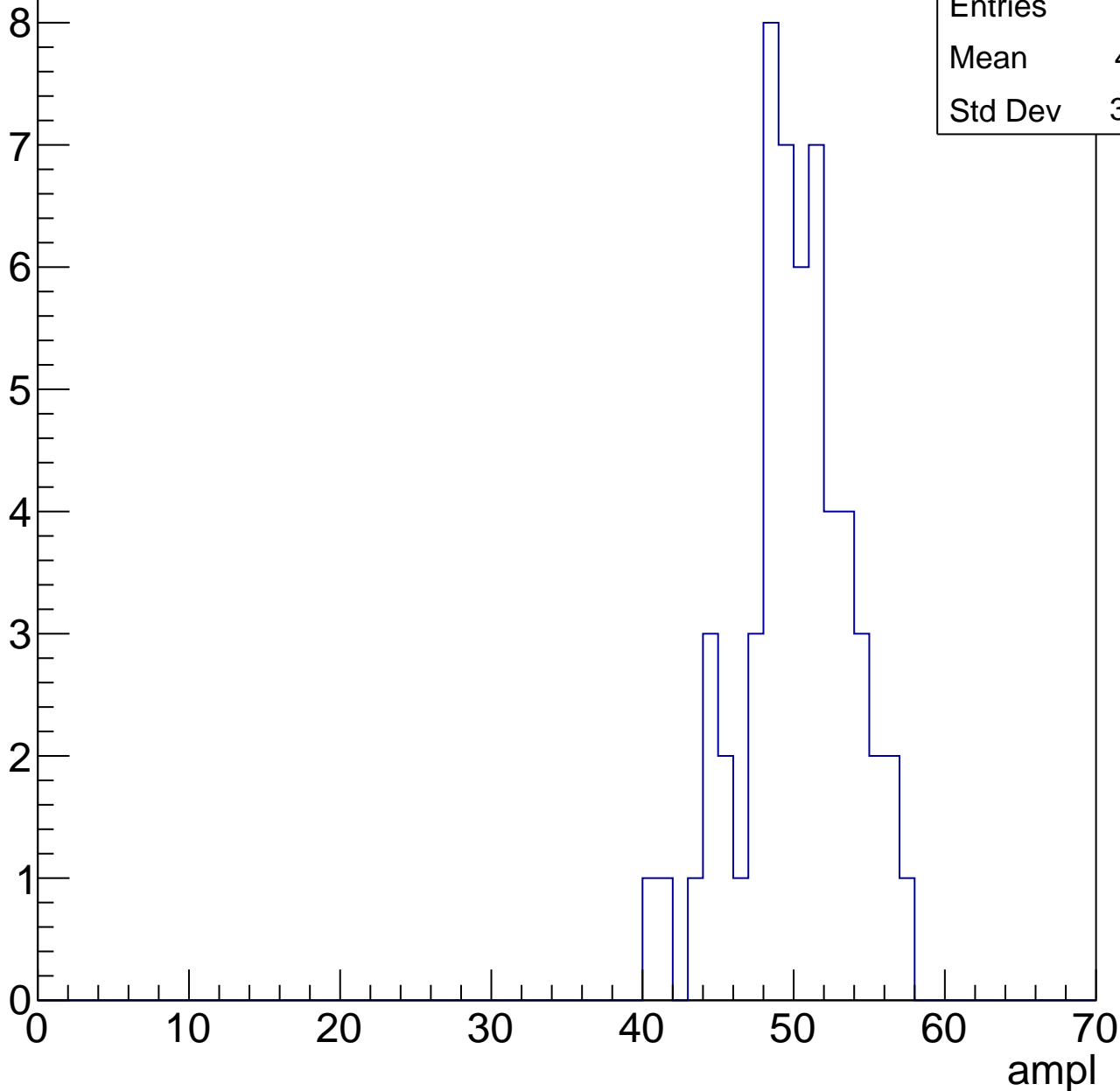


# B1L103S, U16-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	49.61
Std Dev	3.634

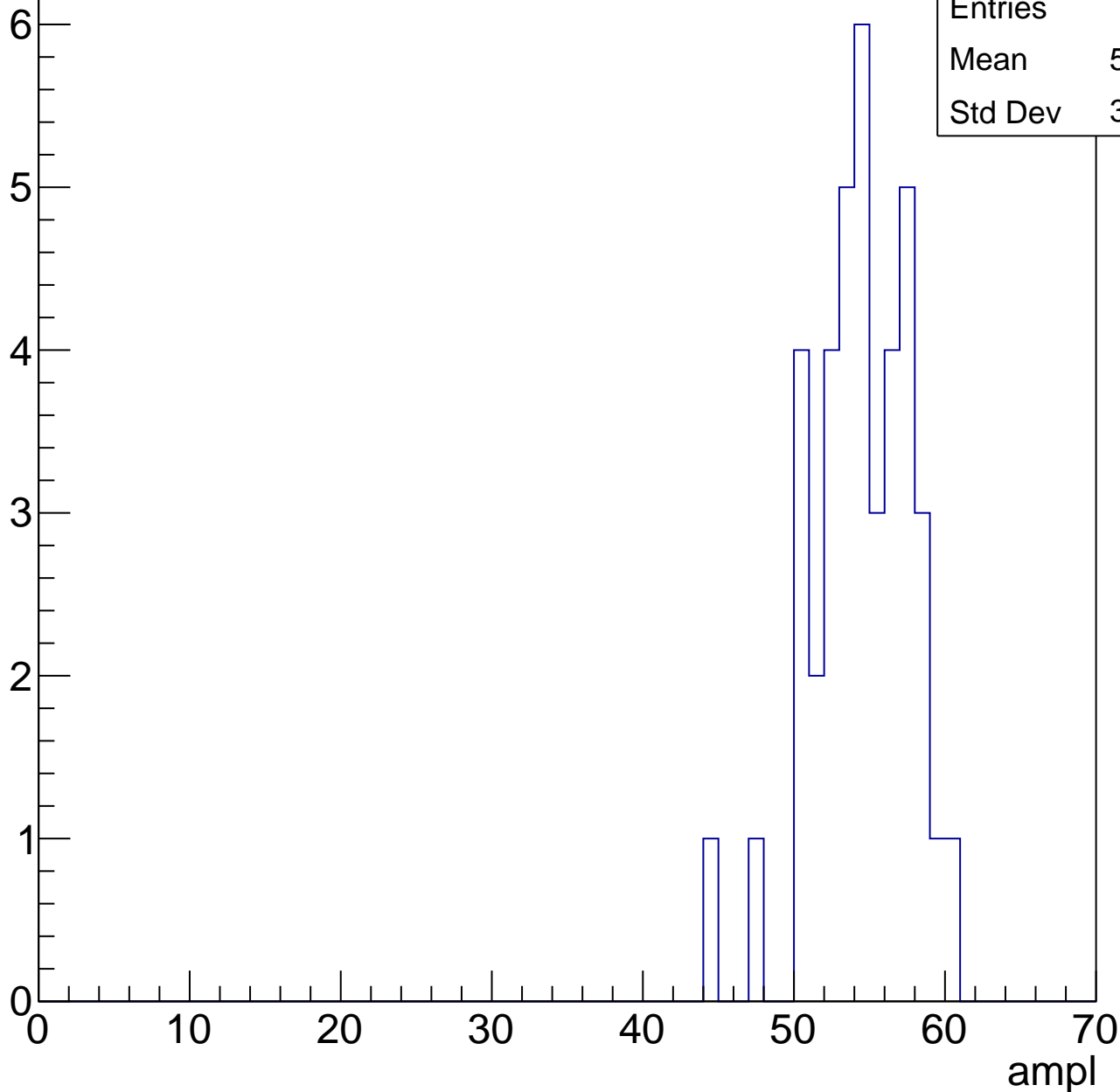


# B1L103S, U16-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

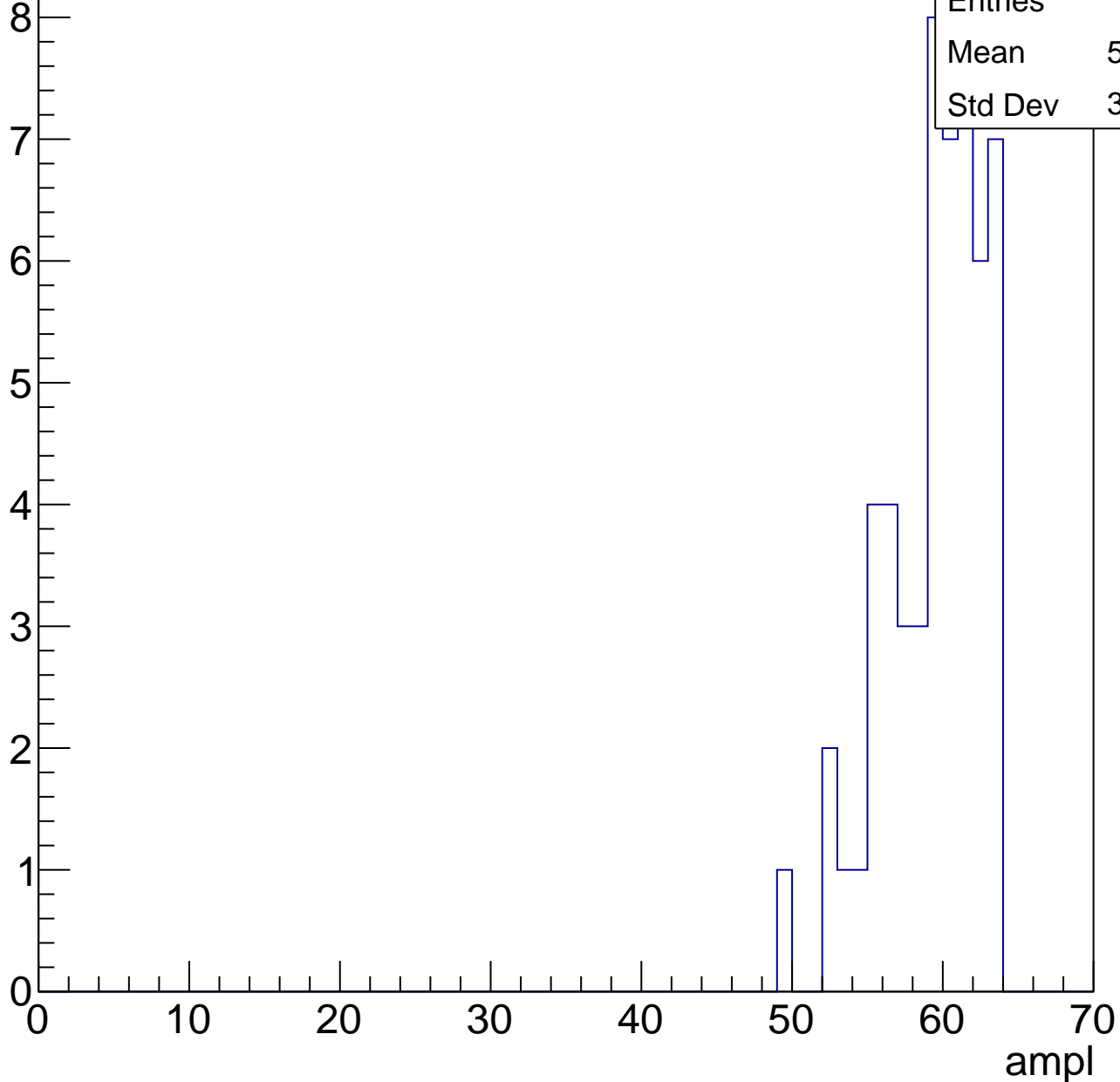
Entries	40
Mean	53.92
Std Dev	3.259



# B1L103S, U16-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

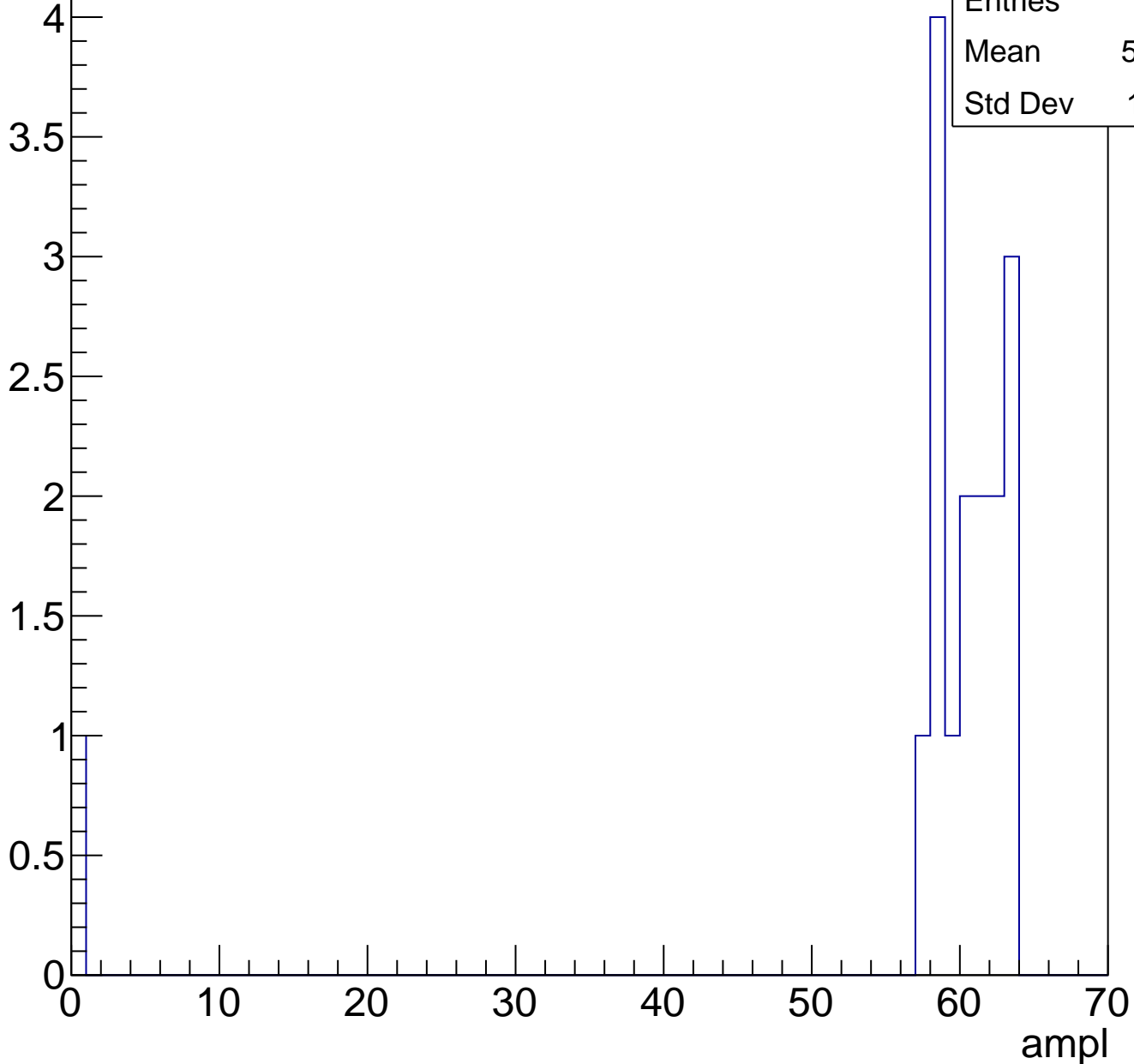
Entry



# B1L103S, U16-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

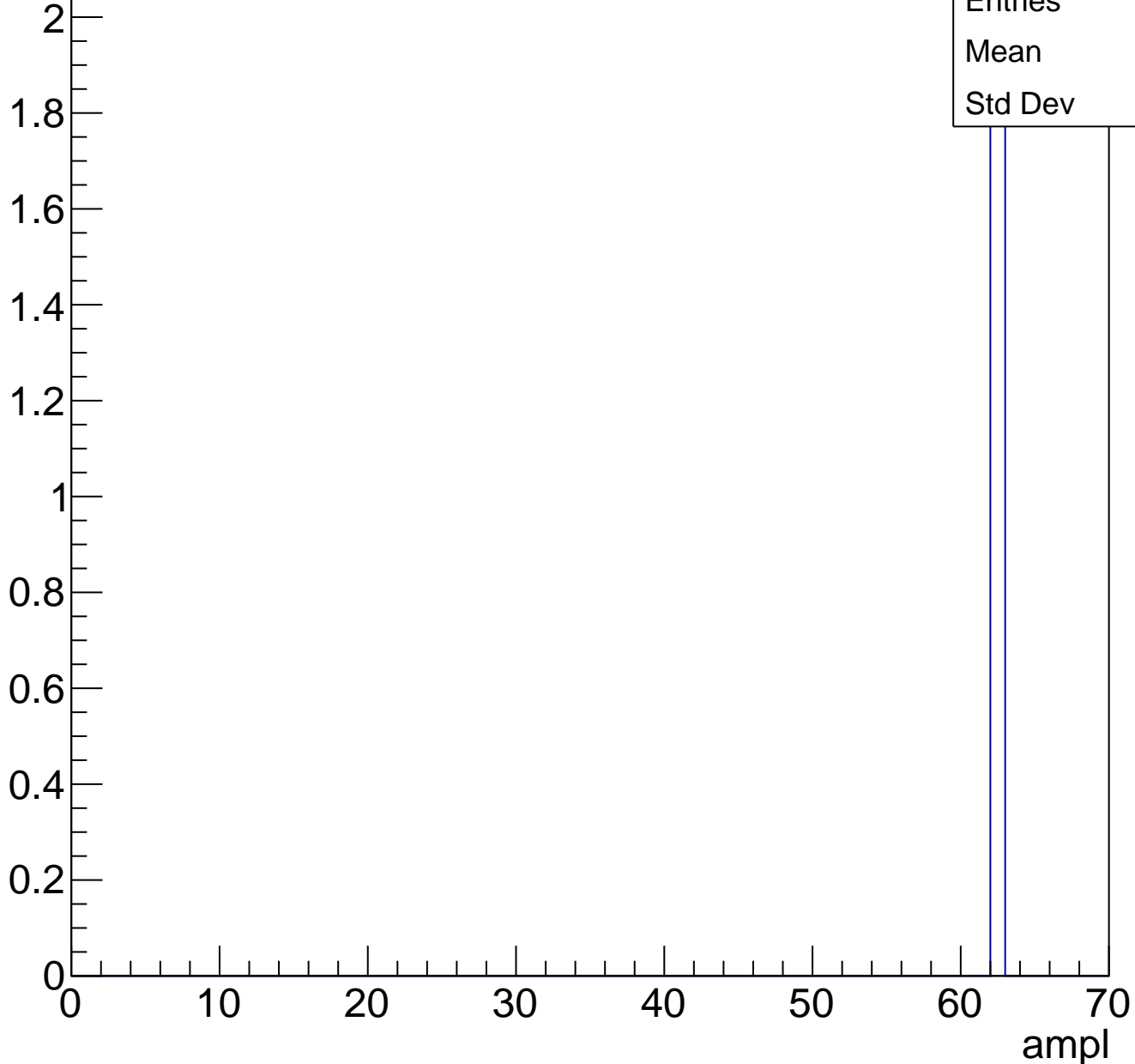




# B1L103S, U16-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	62
Std Dev	0

# B1L103S, U16-ch117, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	74
Mean	26.8
Std Dev	6.598

**Gaus mean : 28.1688**

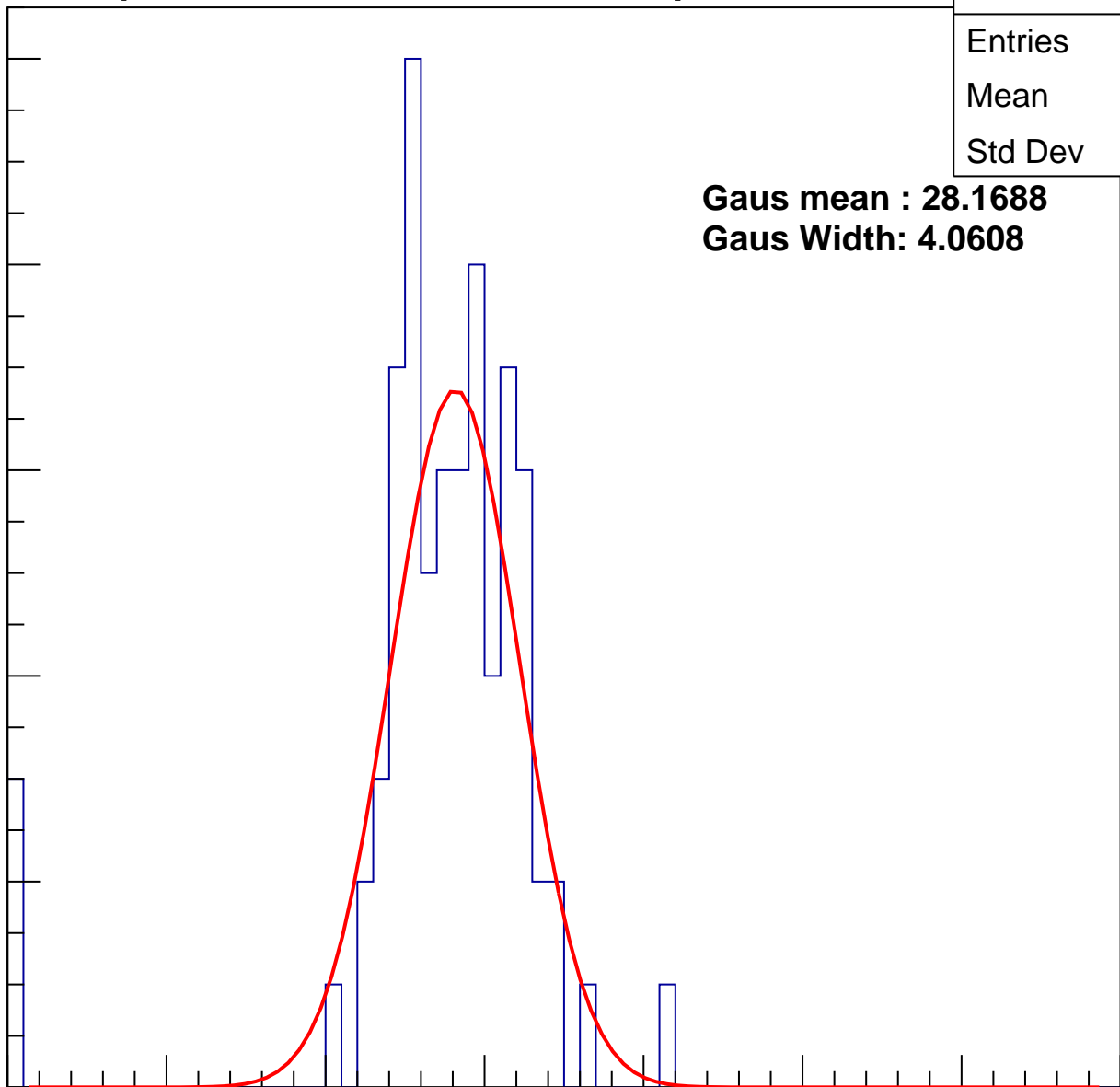
**Gaus Width: 4.0608**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U16-ch117, adc1

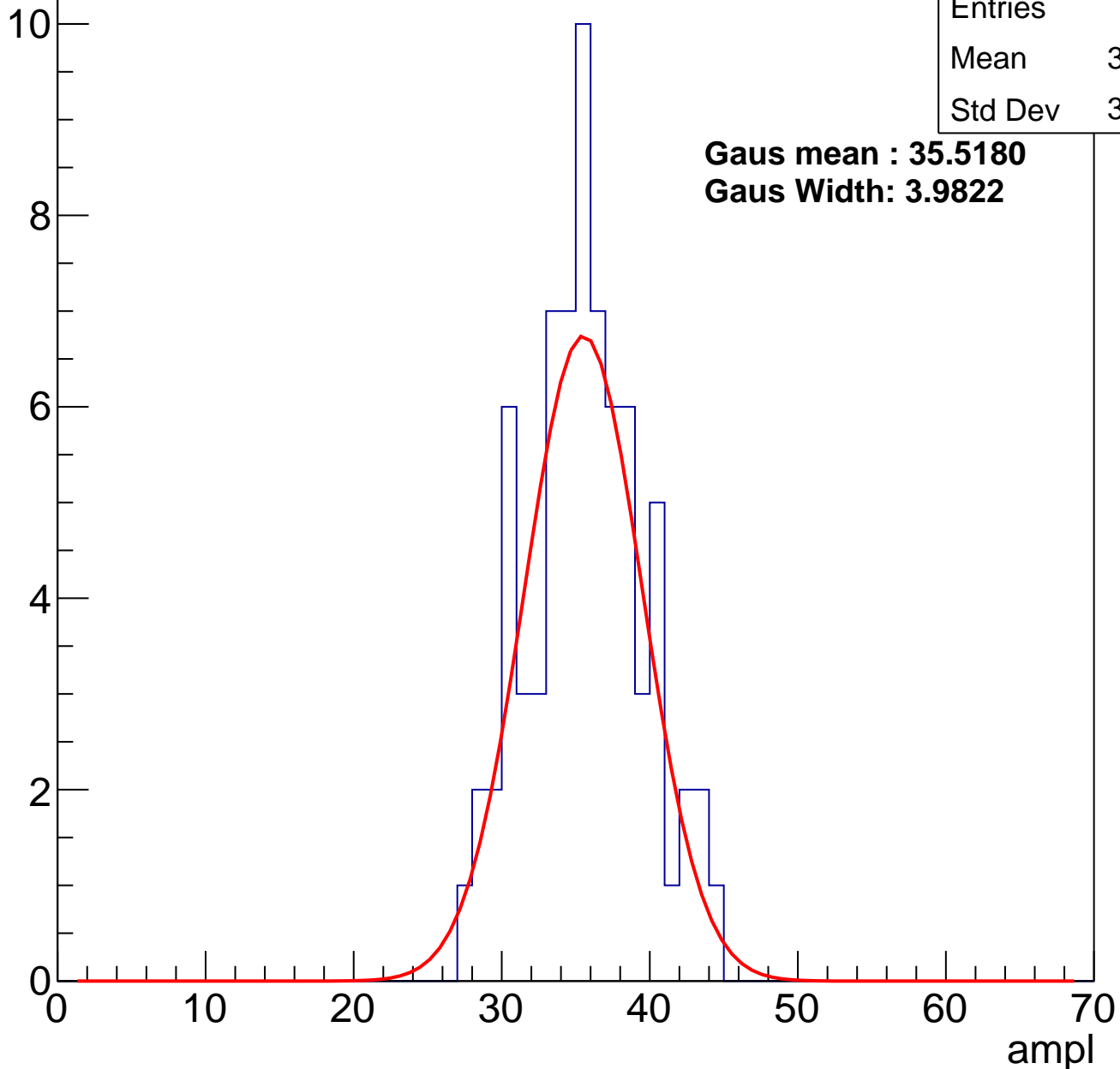
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	74
Mean	35.18
Std Dev	3.843

**Gaus mean : 35.5180**

**Gaus Width: 3.9822**

Entry



# B1L103S, U16-ch117, adc2

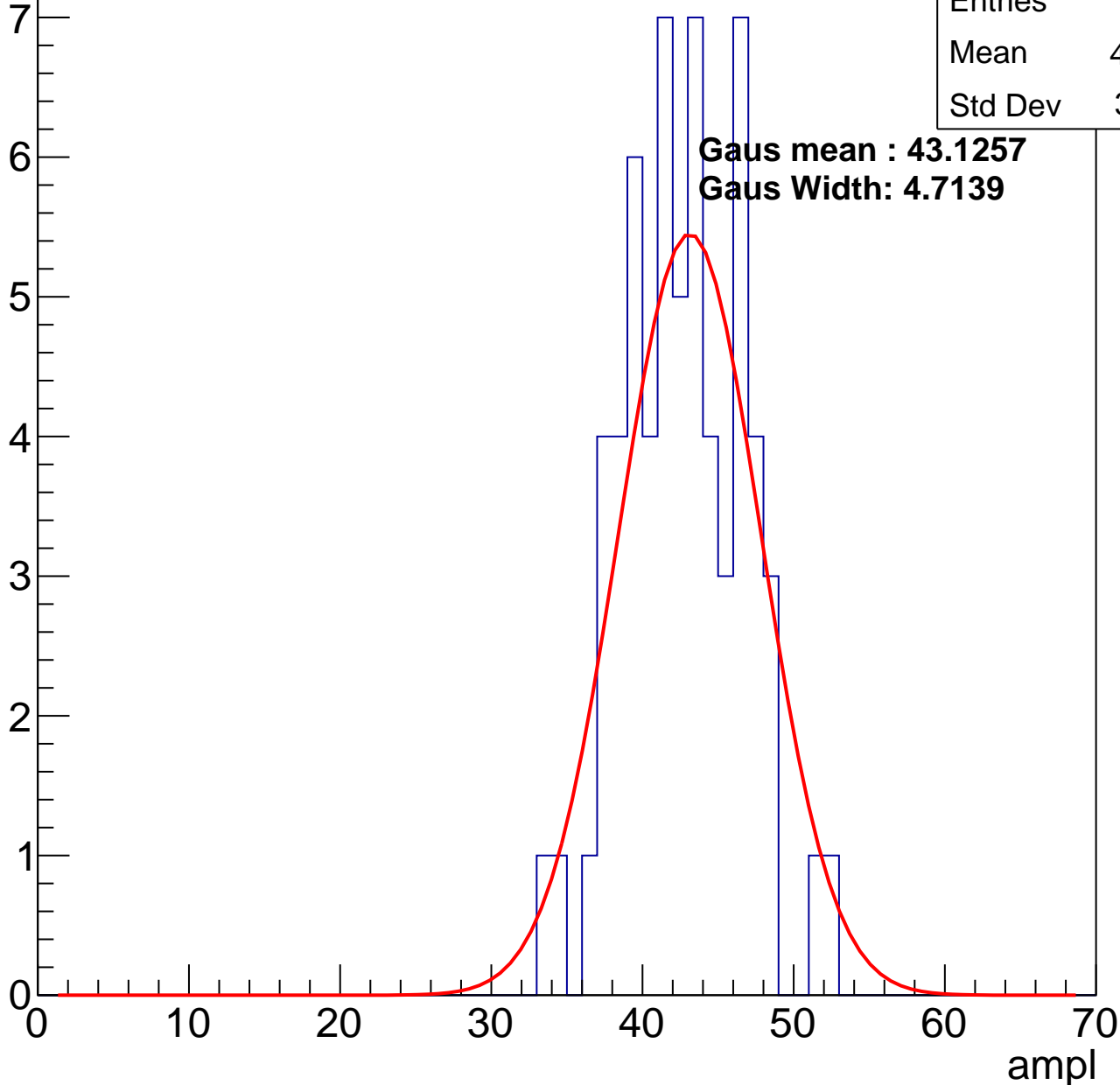
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	42.27
Std Dev	3.921

**Gaus mean : 43.1257**

**Gaus Width: 4.7139**

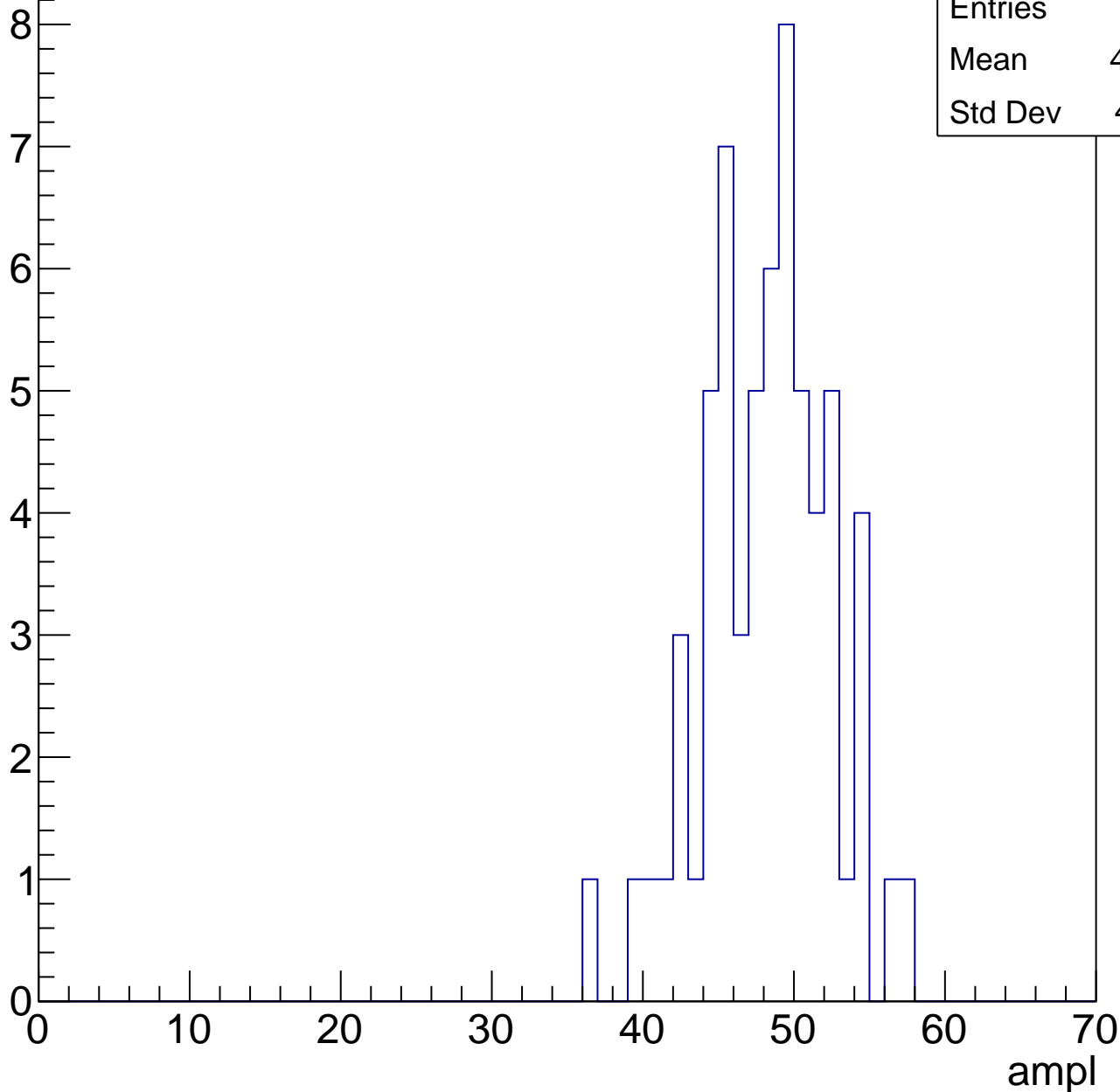


# B1L103S, U16-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	47.76
Std Dev	4.151

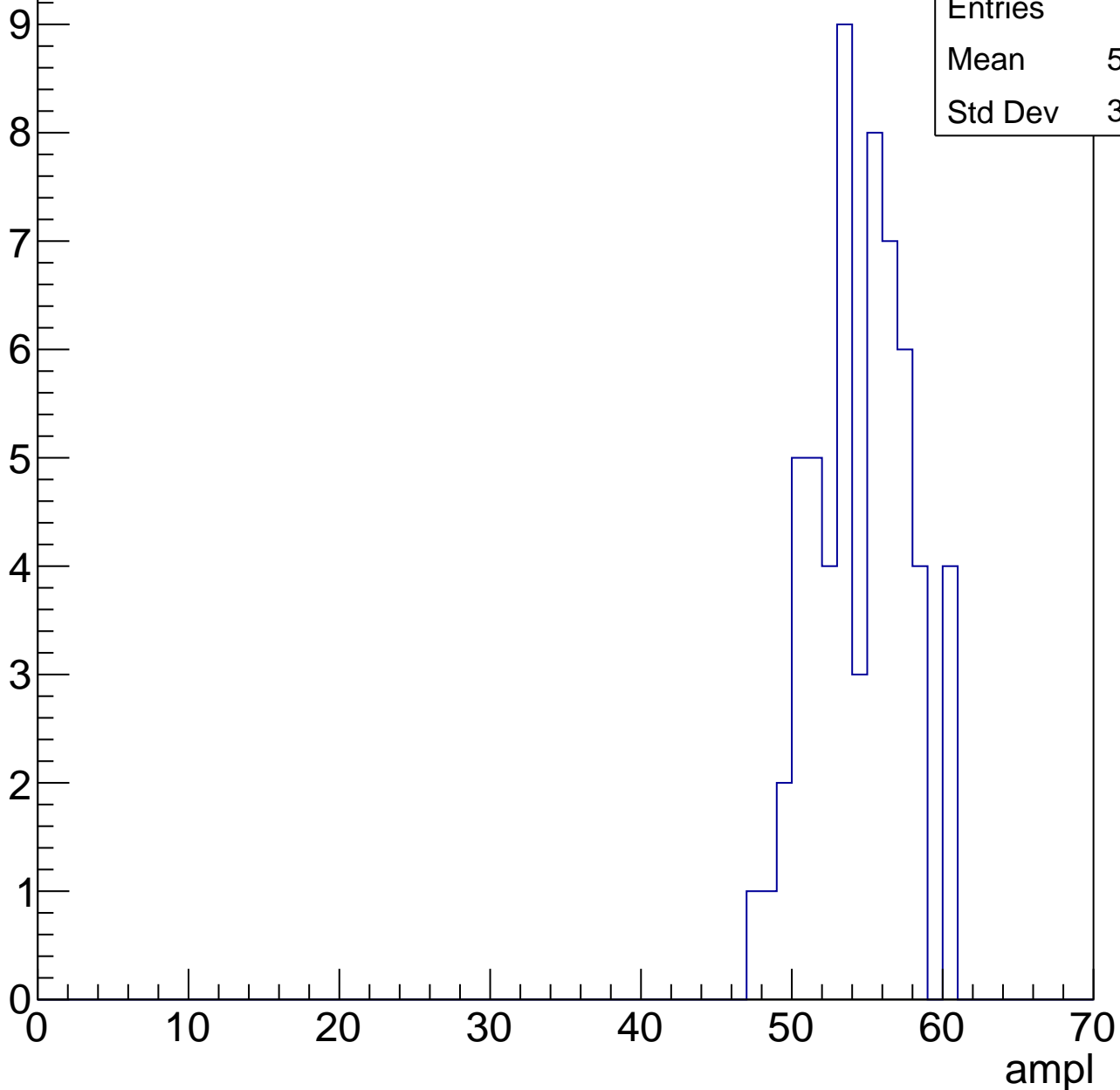


# B1L103S, U16-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

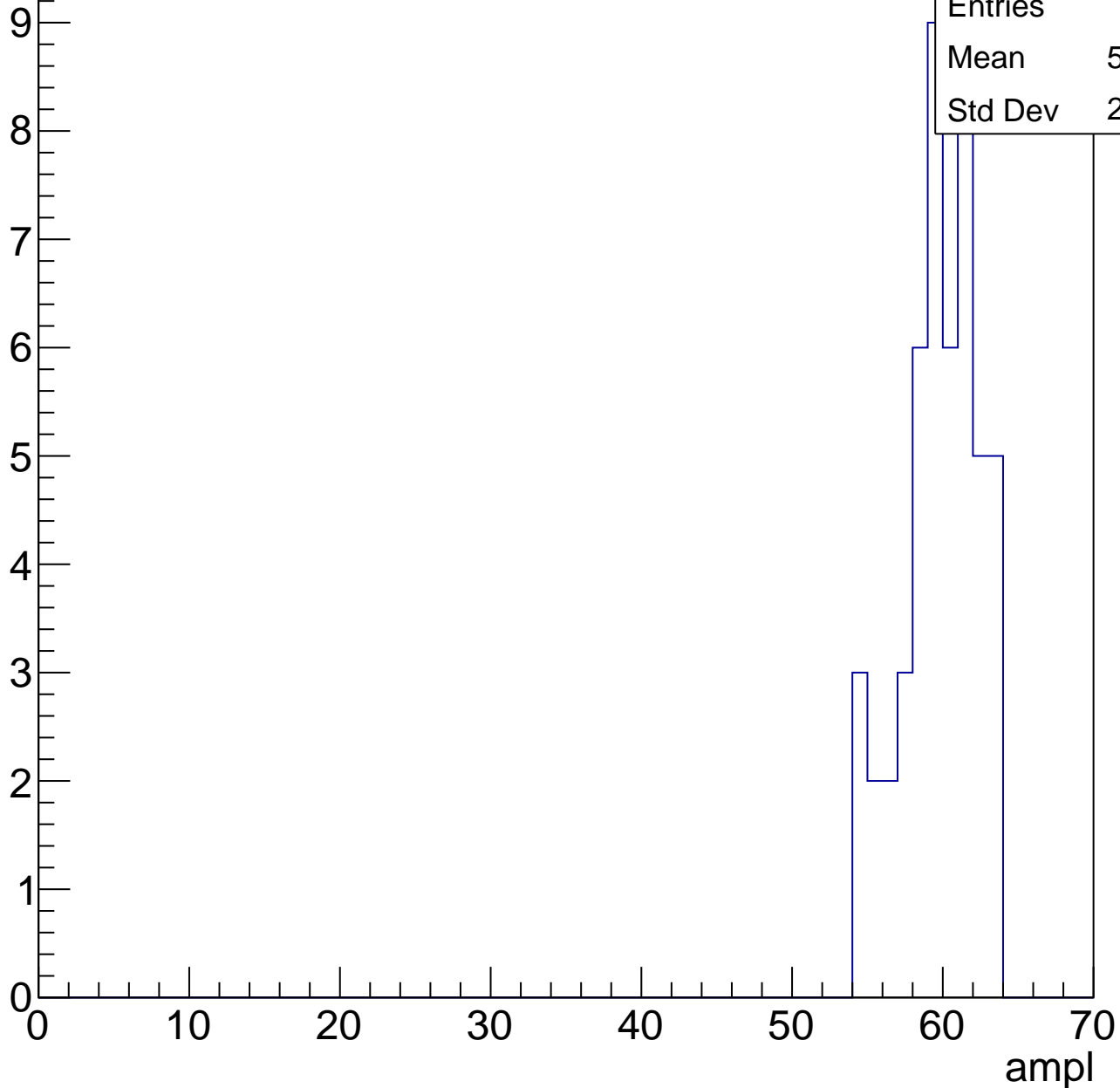
Entries	59
Mean	54.08
Std Dev	3.142



# B1L103S, U16-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

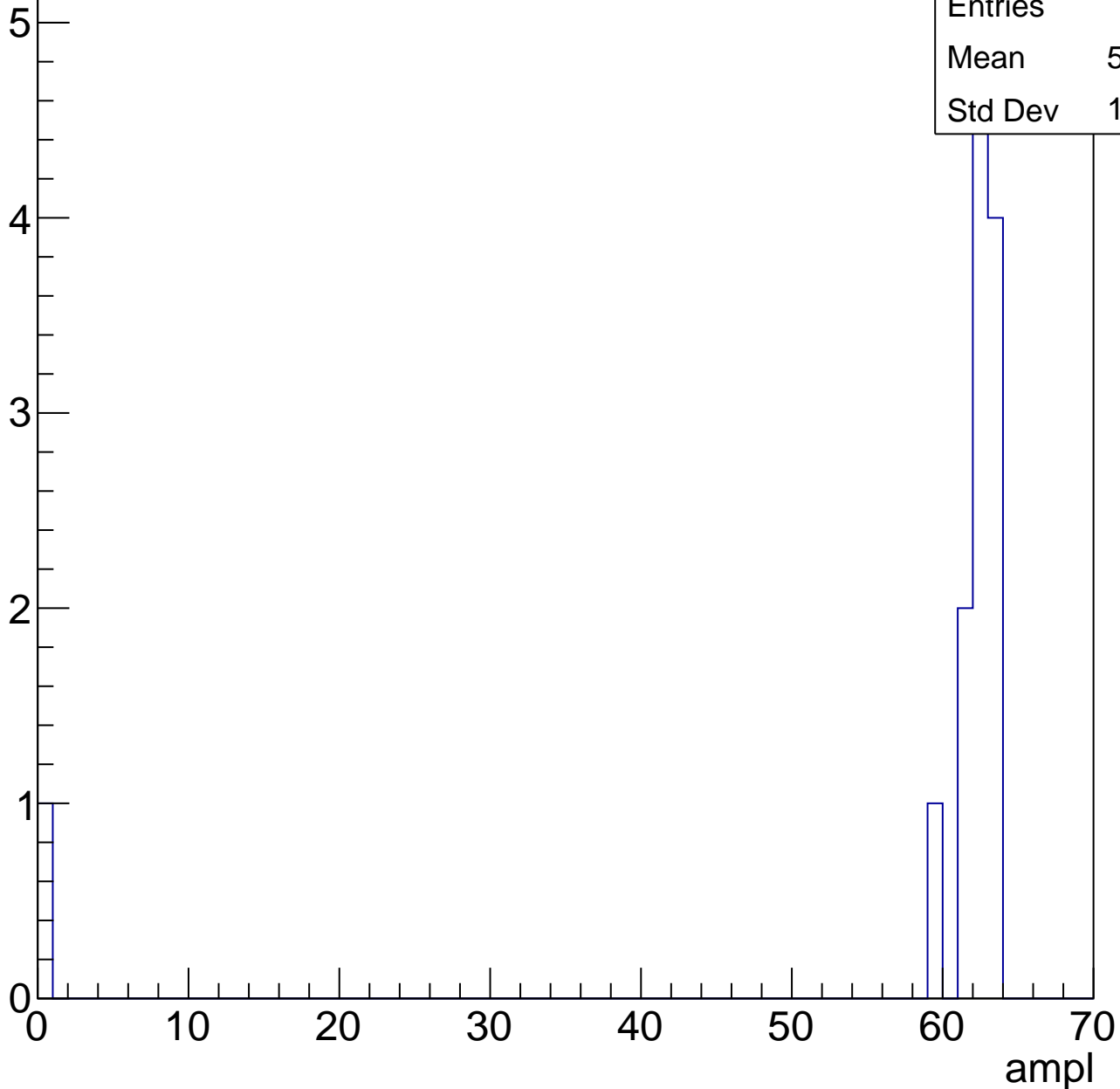


# B1L103S, U16-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	13
Mean	57.15
Std Dev	16.53





# B1L103S, U16-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch118, adc0

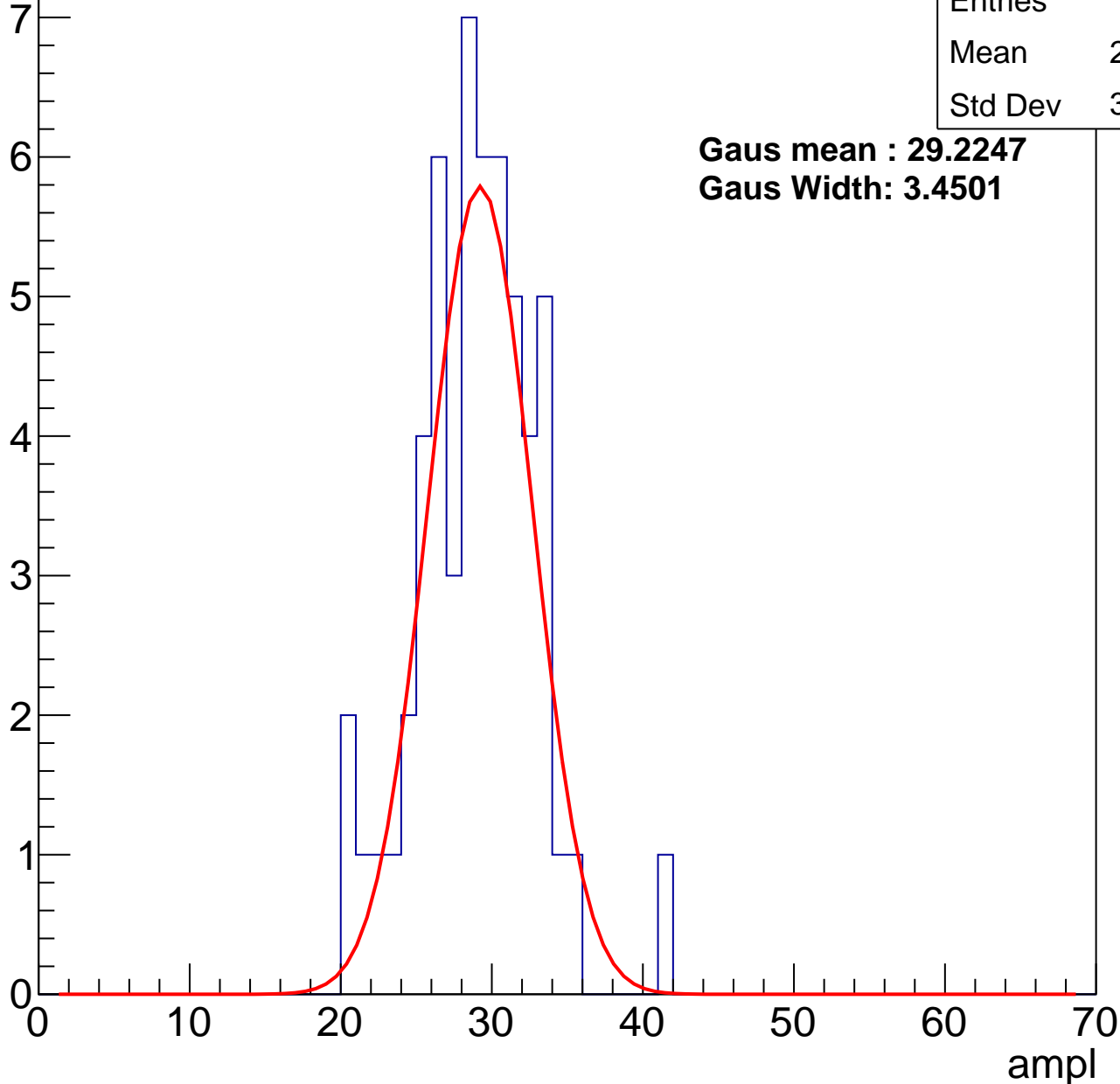
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	28.55
Std Dev	3.859

**Gaus mean : 29.2247**

**Gaus Width: 3.4501**



# B1L103S, U16-ch118, adc1

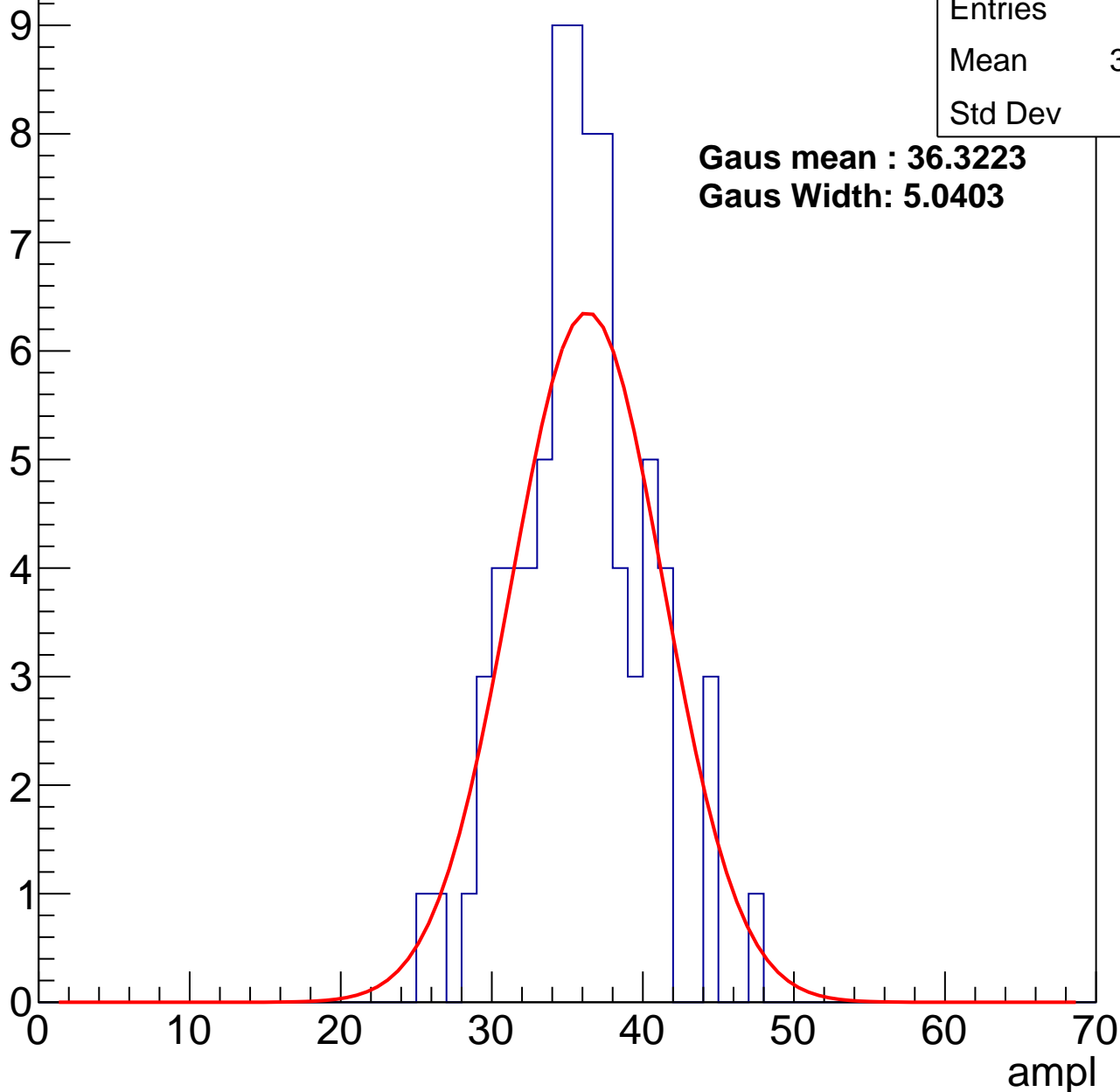
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	35.32
Std Dev	4.17

**Gaus mean : 36.3223**

**Gaus Width: 5.0403**



# B1L103S, U16-ch118, adc2

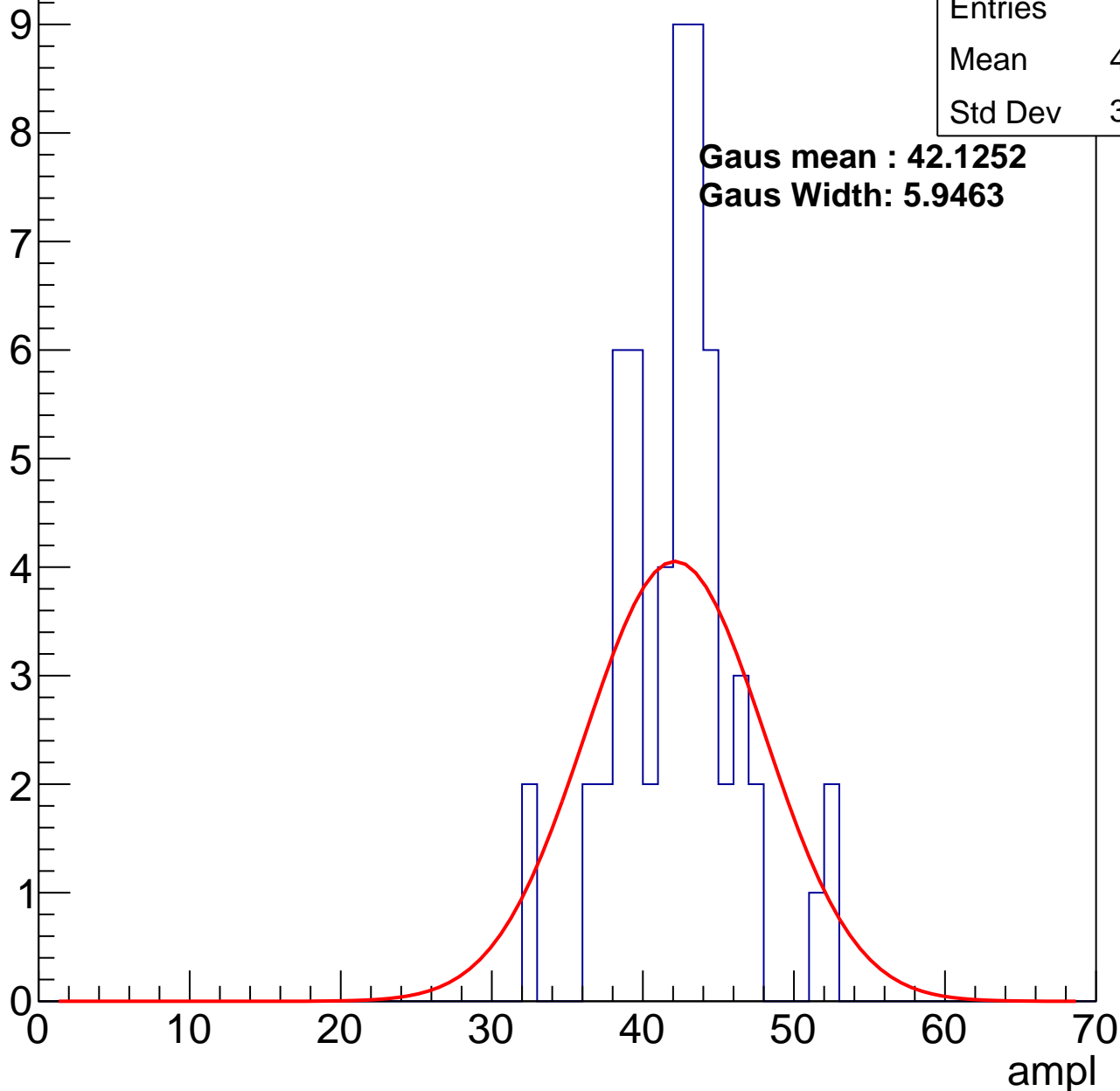
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	41.76
Std Dev	3.962

**Gaus mean : 42.1252**

**Gaus Width: 5.9463**



# B1L103S, U16-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	62
Mean	47.95
Std Dev	3.791

Entry

10

8

6

4

2

0

0

10

20

30

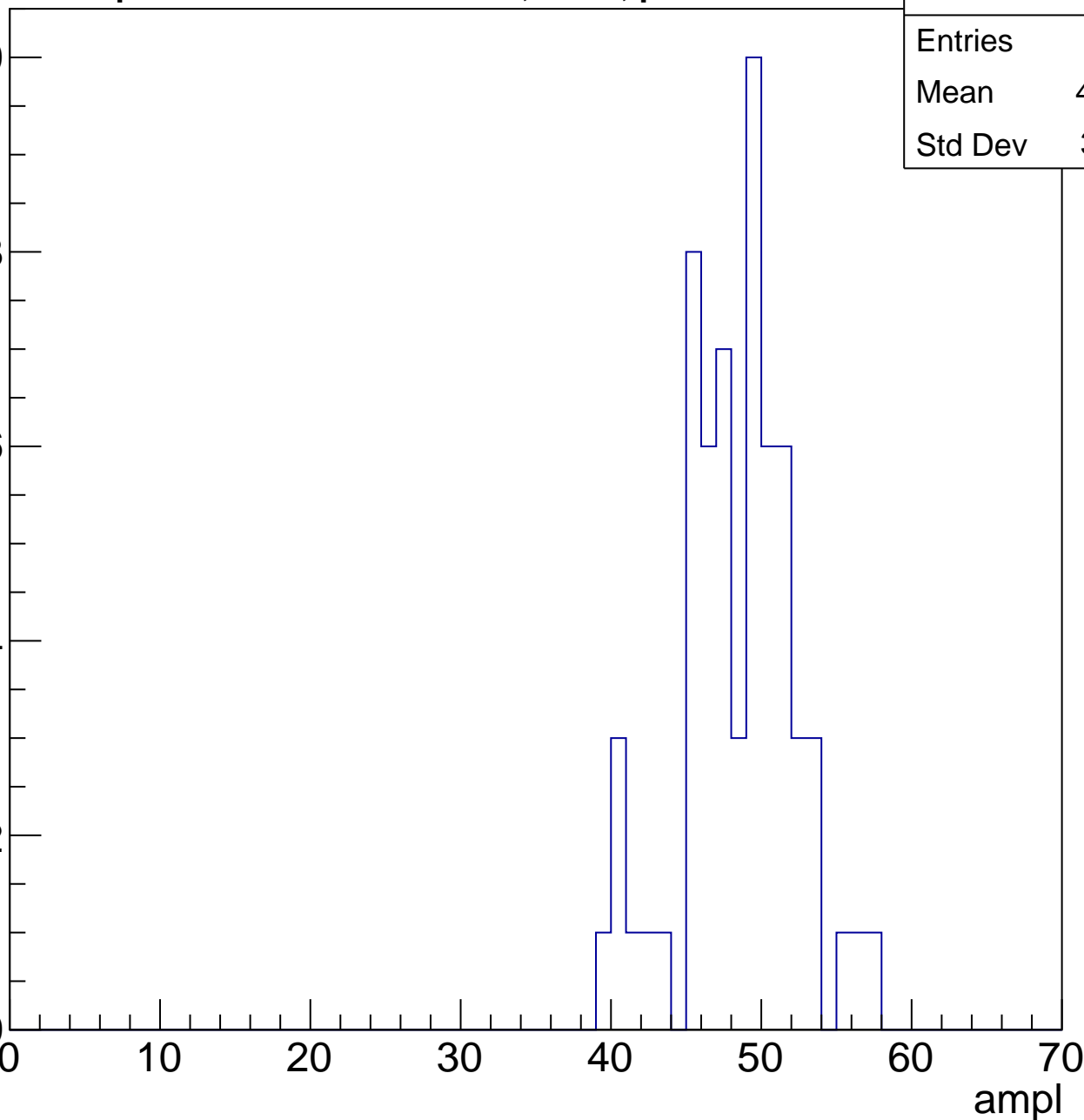
40

50

60

70

ampl

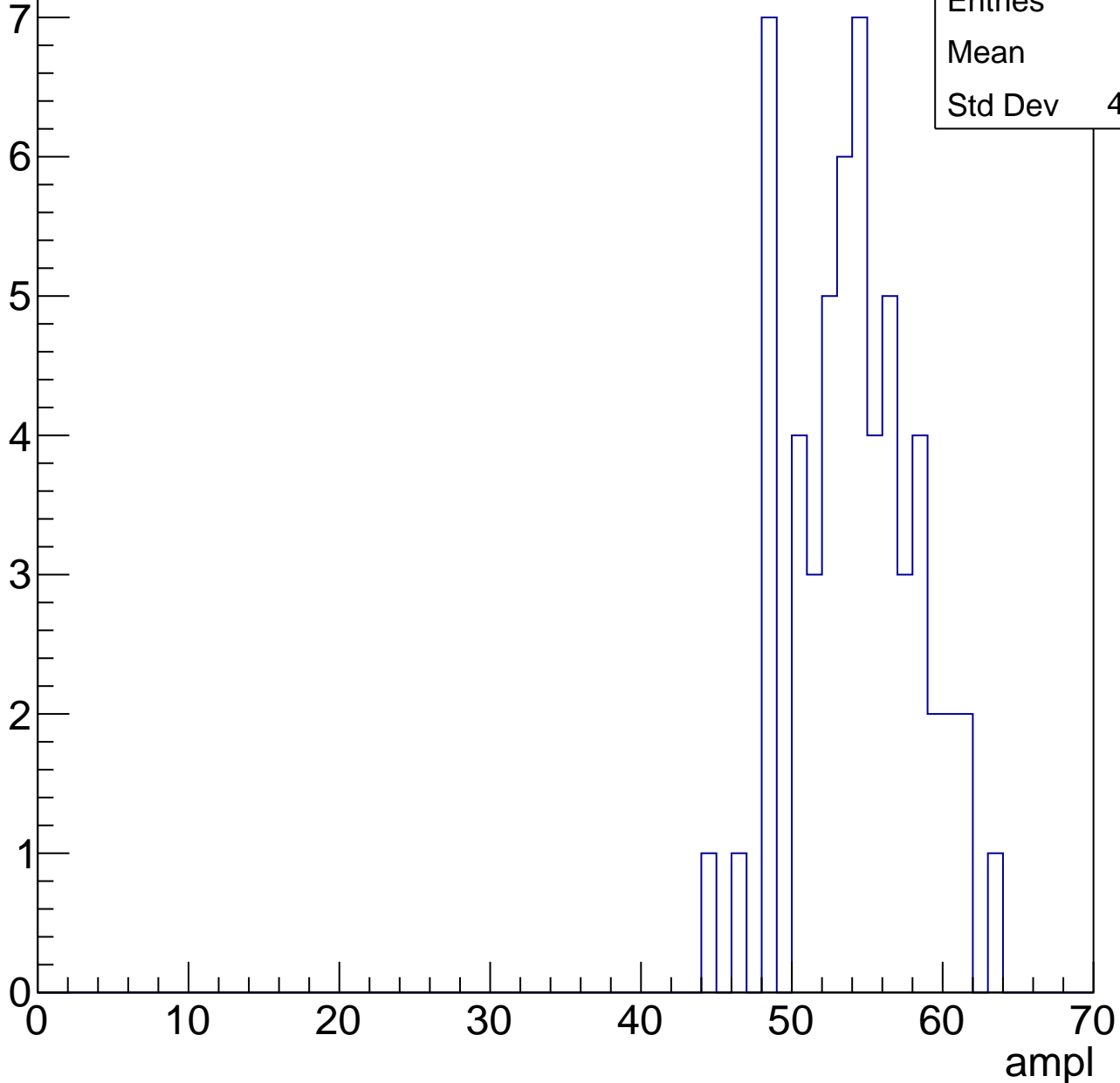


# B1L103S, U16-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

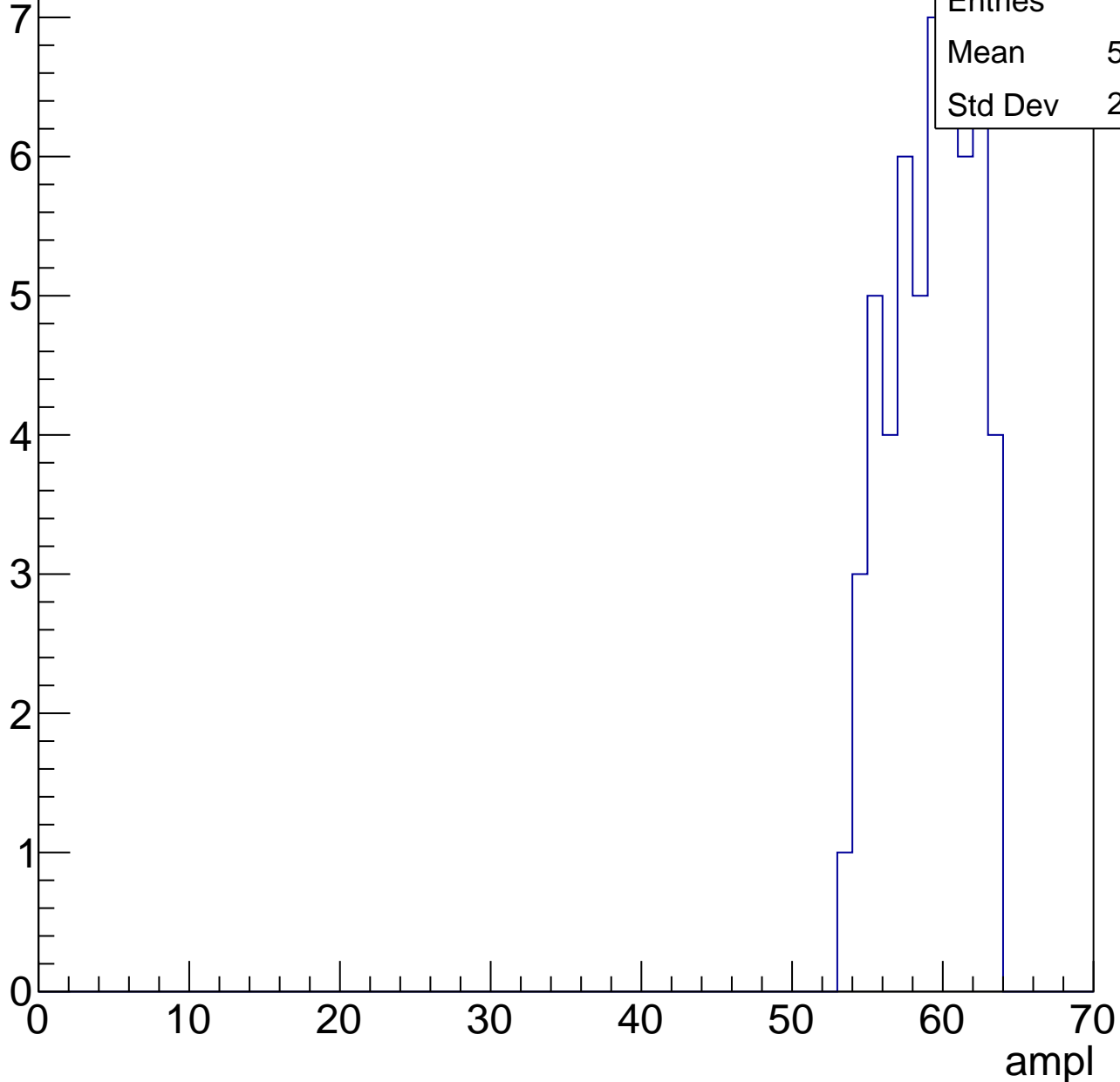
Entries	57
Mean	53.7
Std Dev	4.069



# B1L103S, U16-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

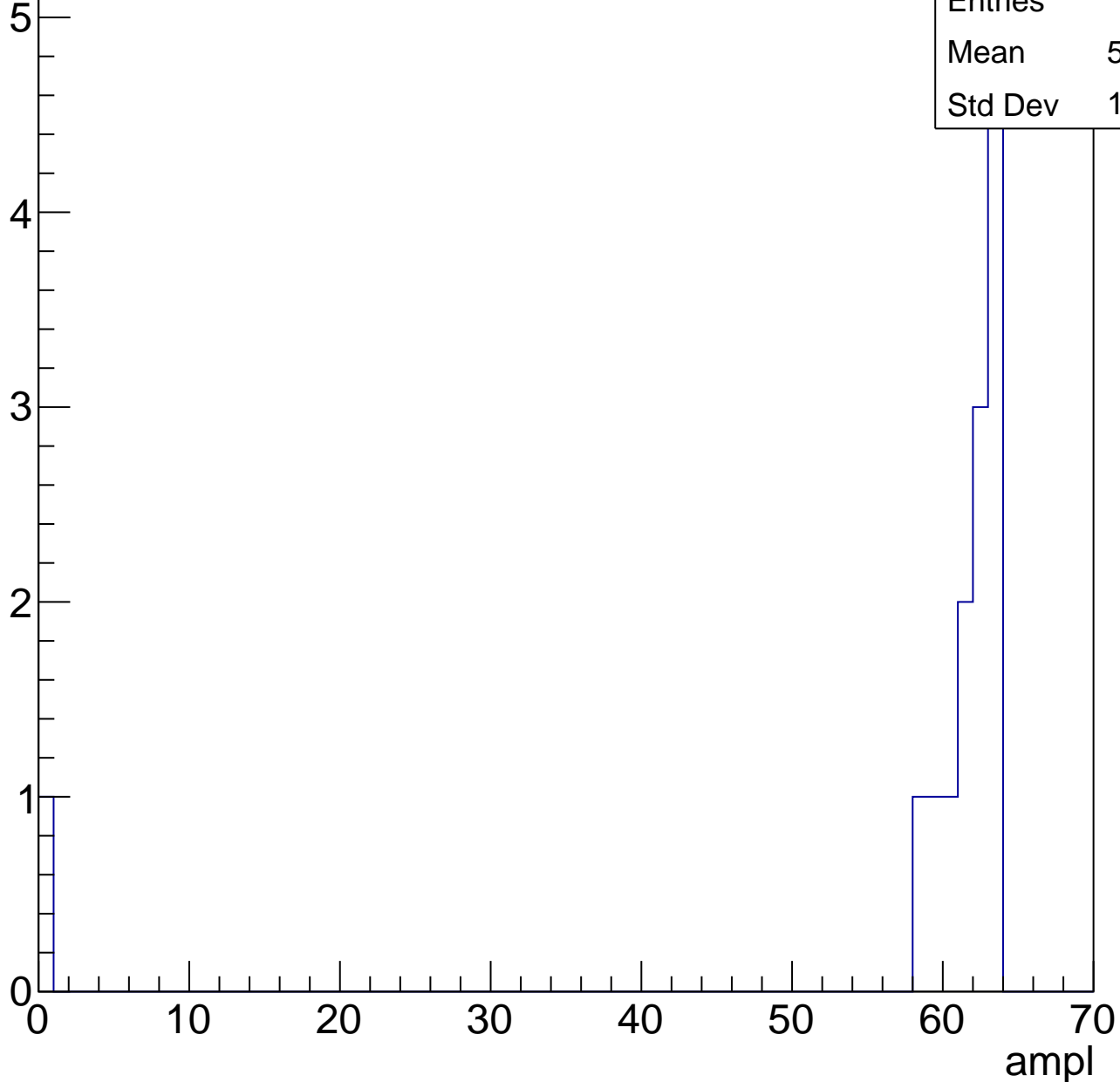


# B1L103S, U16-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	14
Mean	57.14
Std Dev	15.92





# B1L103S, U16-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch119, adc0

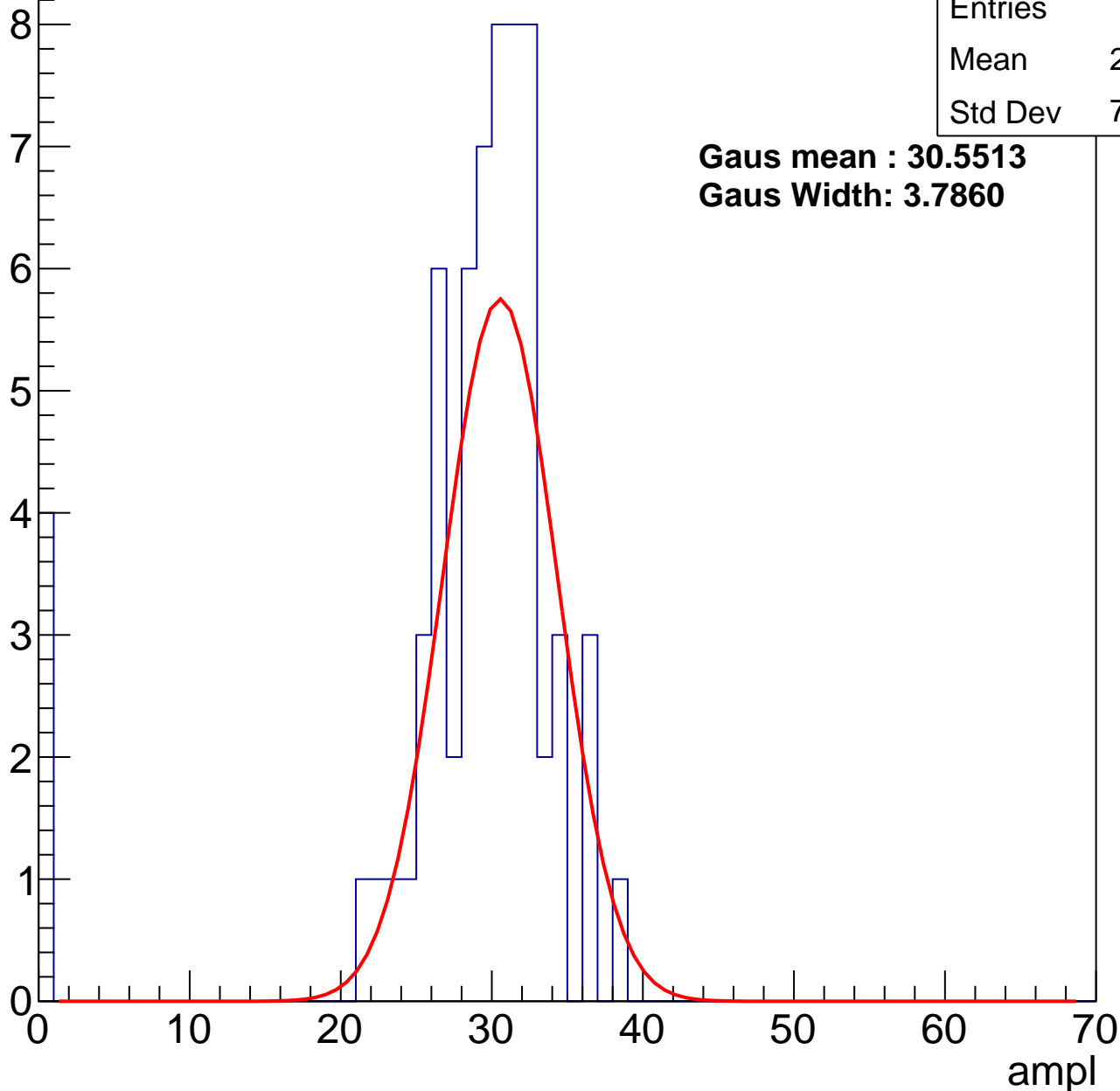
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	27.75
Std Dev	7.845

**Gaus mean : 30.5513**

**Gaus Width: 3.7860**



# B1L103S, U16-ch119, adc1

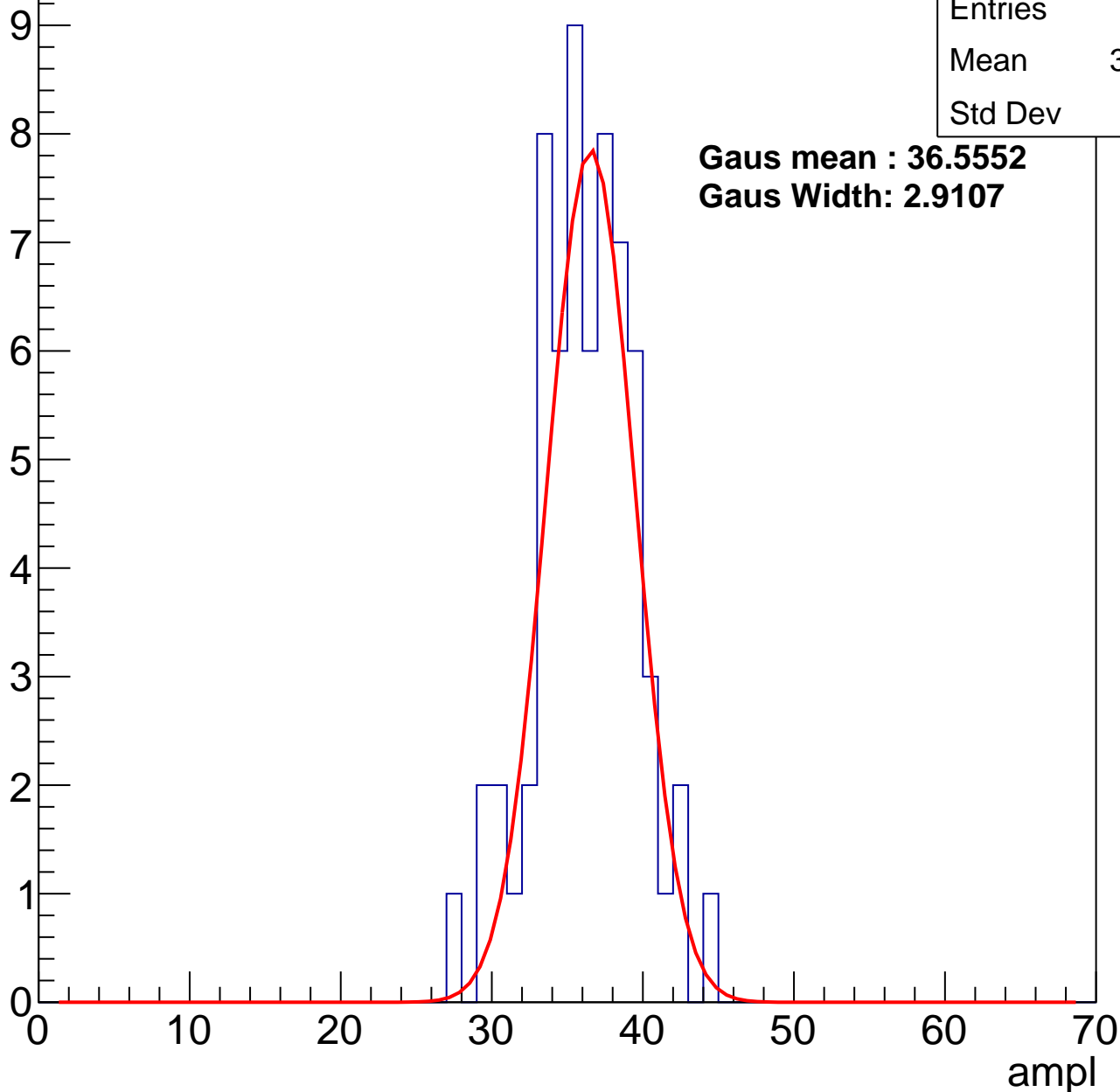
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	35.75
Std Dev	3.3

**Gaus mean : 36.5552**

**Gaus Width: 2.9107**



# B1L103S, U16-ch119, adc2

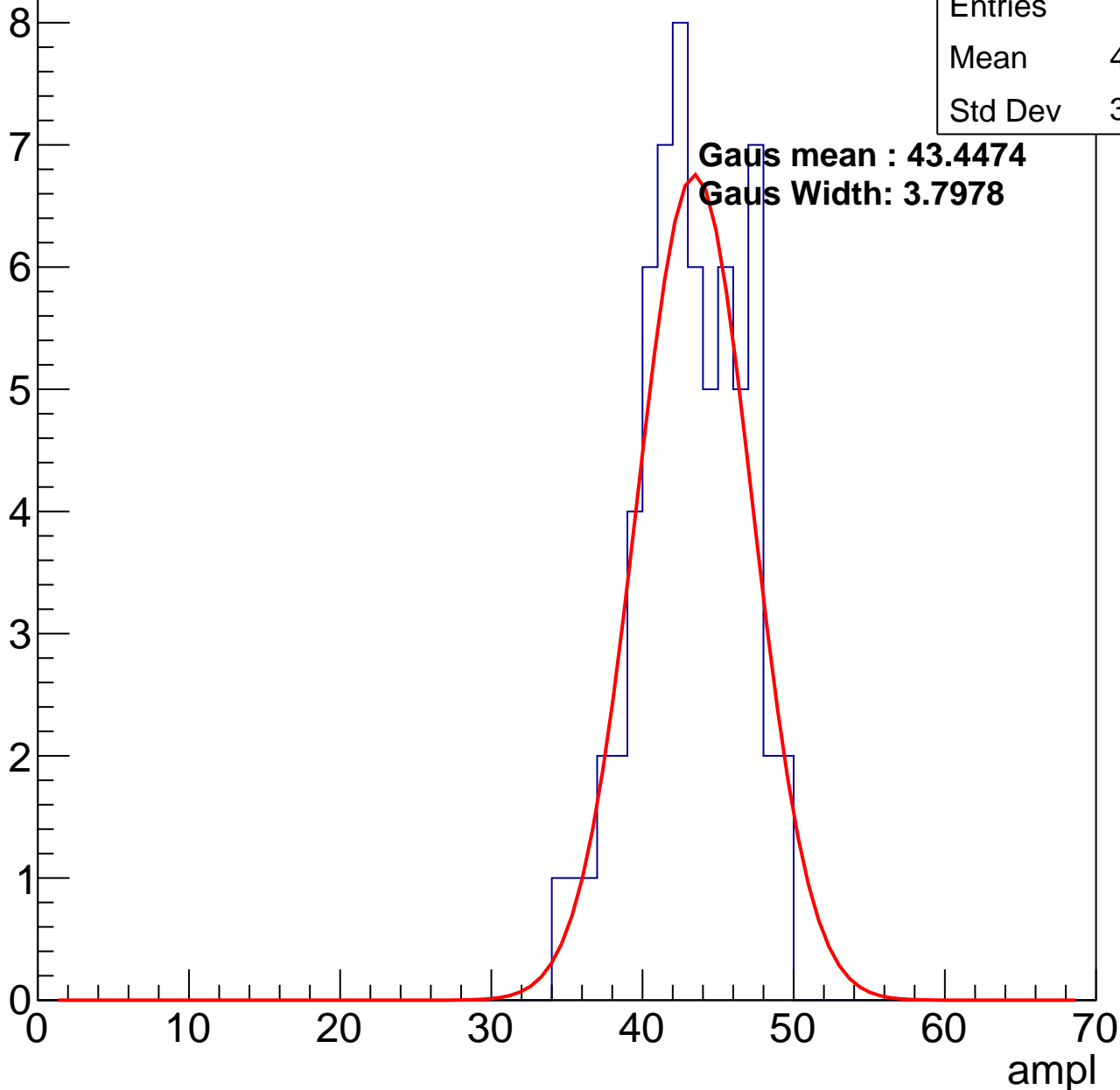
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	42.69
Std Dev	3.446

**Gaus mean : 43.4474**

**Gaus Width: 3.7978**

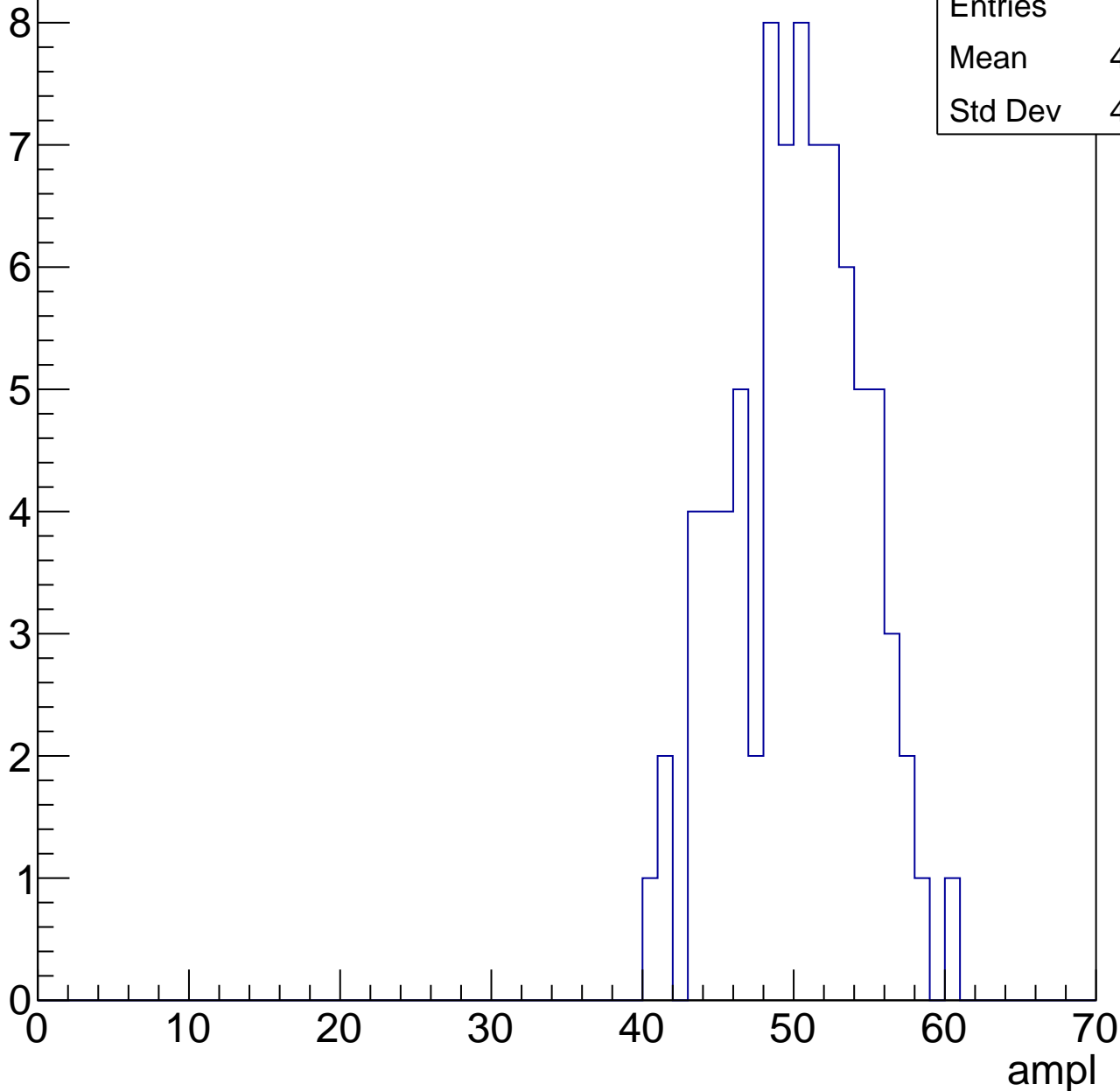


# B1L103S, U16-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	82
Mean	49.82
Std Dev	4.277

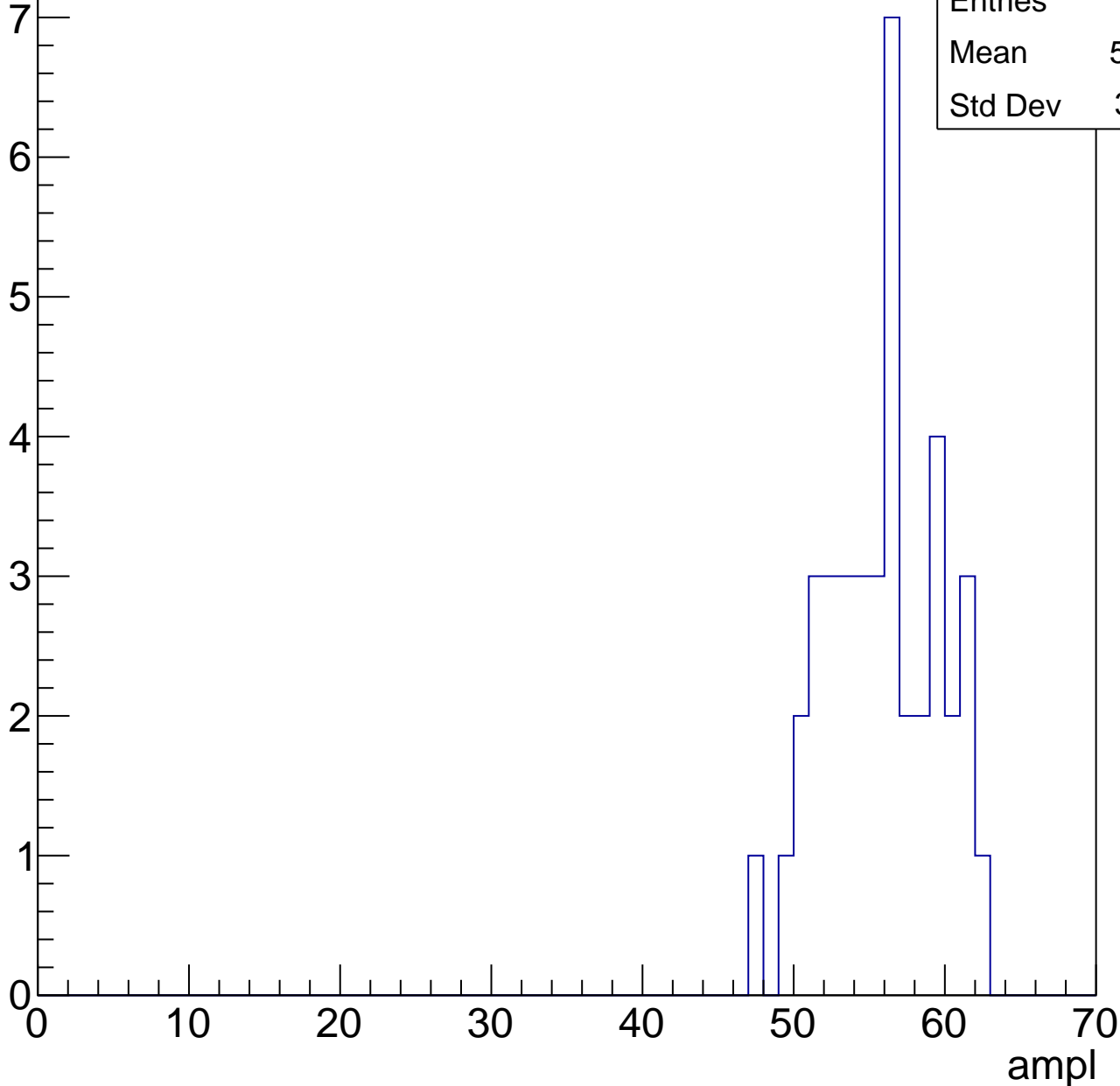


# B1L103S, U16-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	40
Mean	55.35
Std Dev	3.671

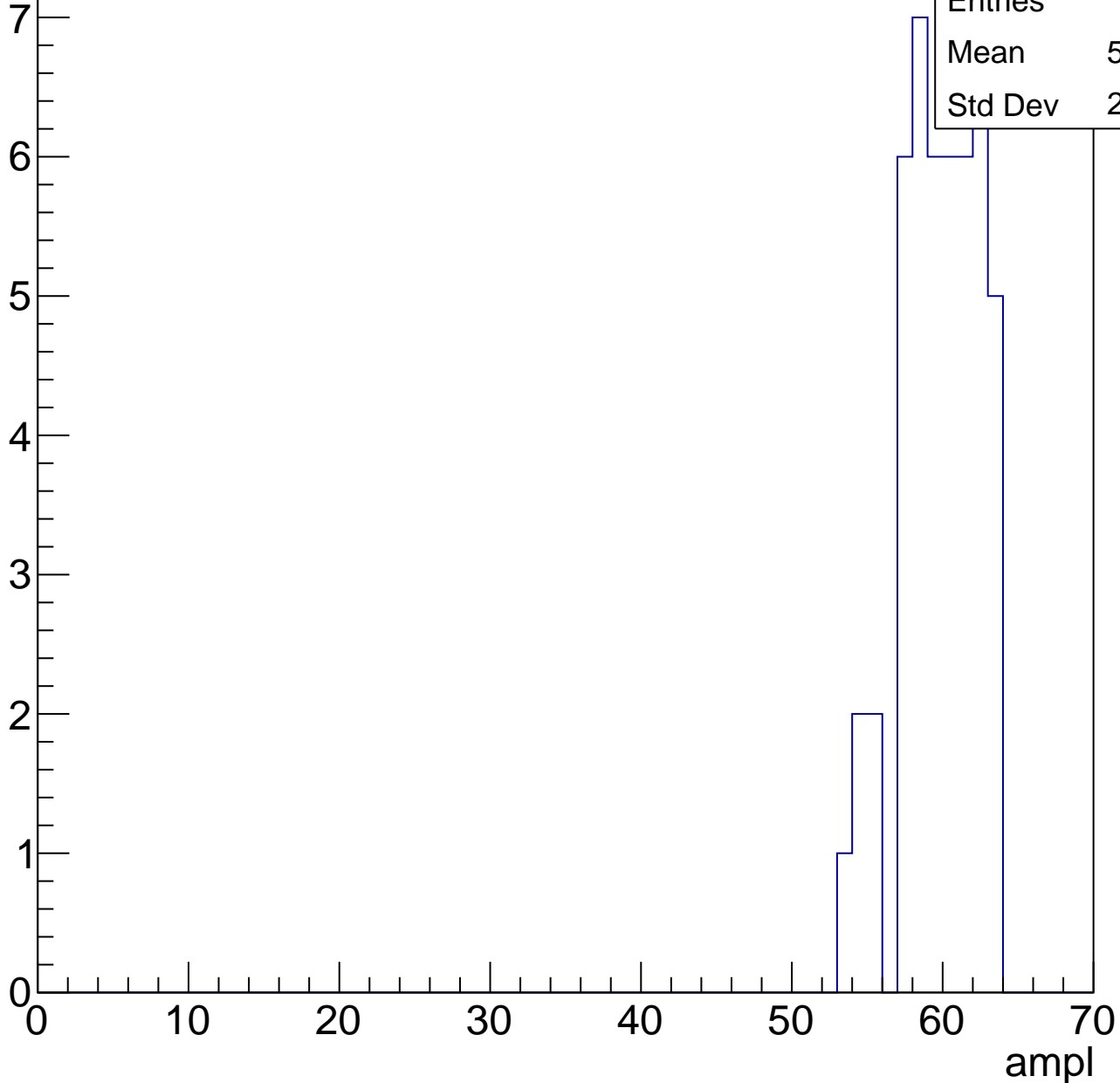


# B1L103S, U16-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	59.33
Std Dev	2.569

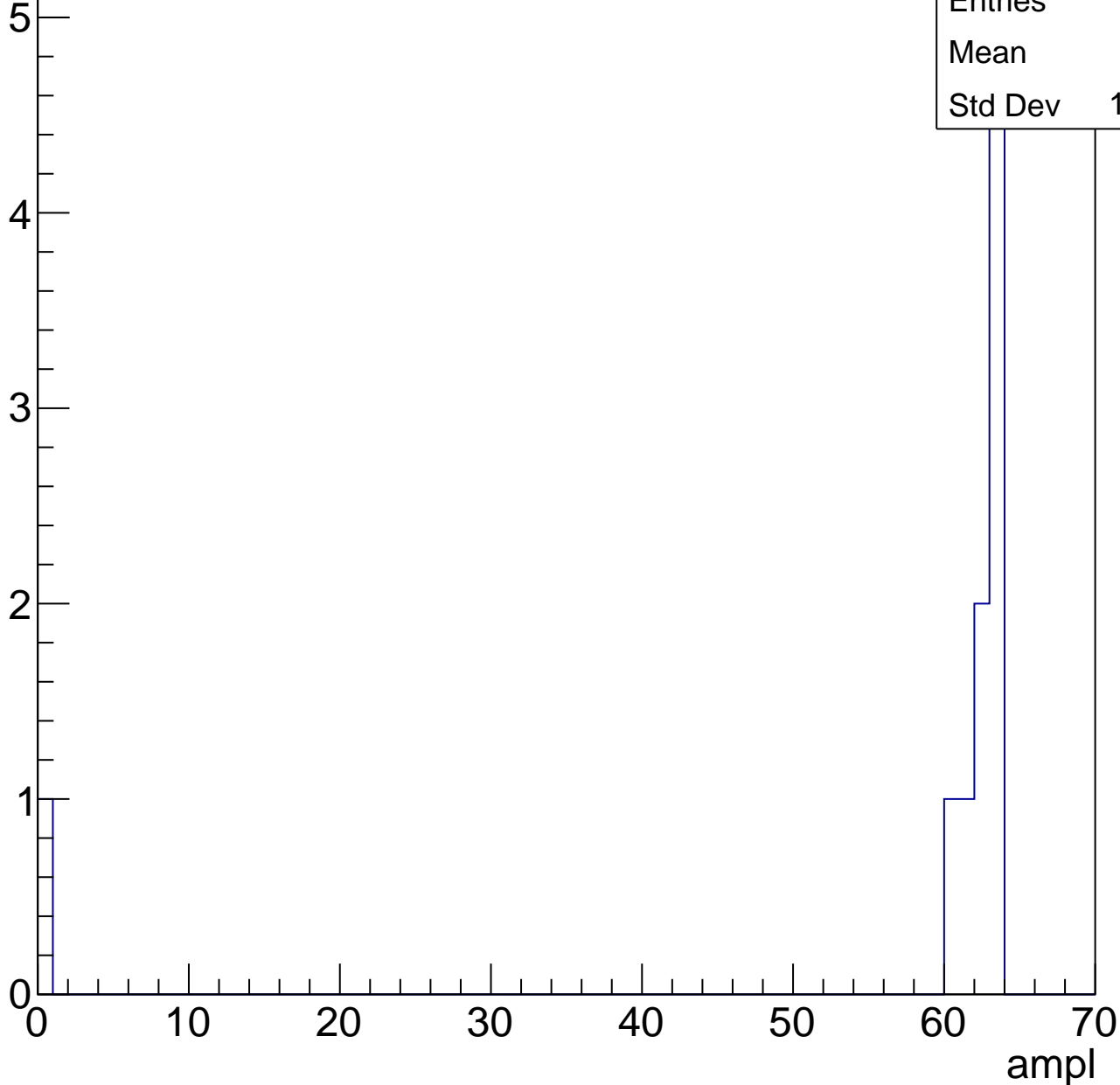


# B1L103S, U16-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	10
Mean	56
Std Dev	18.69





# B1L103S, U16-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	21
Std Dev	0

ampl

# B1L103S, U16-ch120, adc0

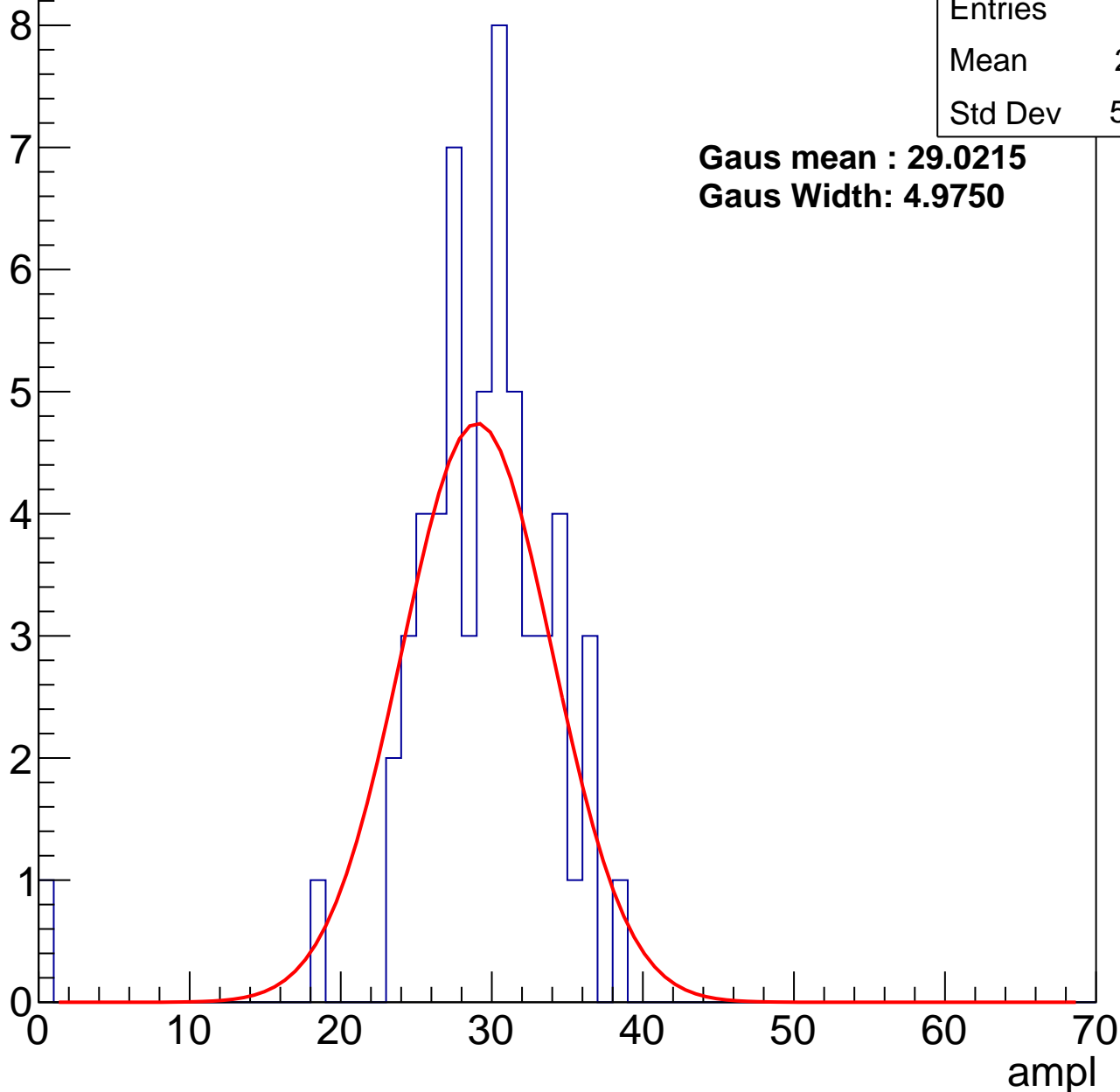
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	28.71
Std Dev	5.417

**Gaus mean : 29.0215**

**Gaus Width: 4.9750**



# B1L103S, U16-ch120, adc1

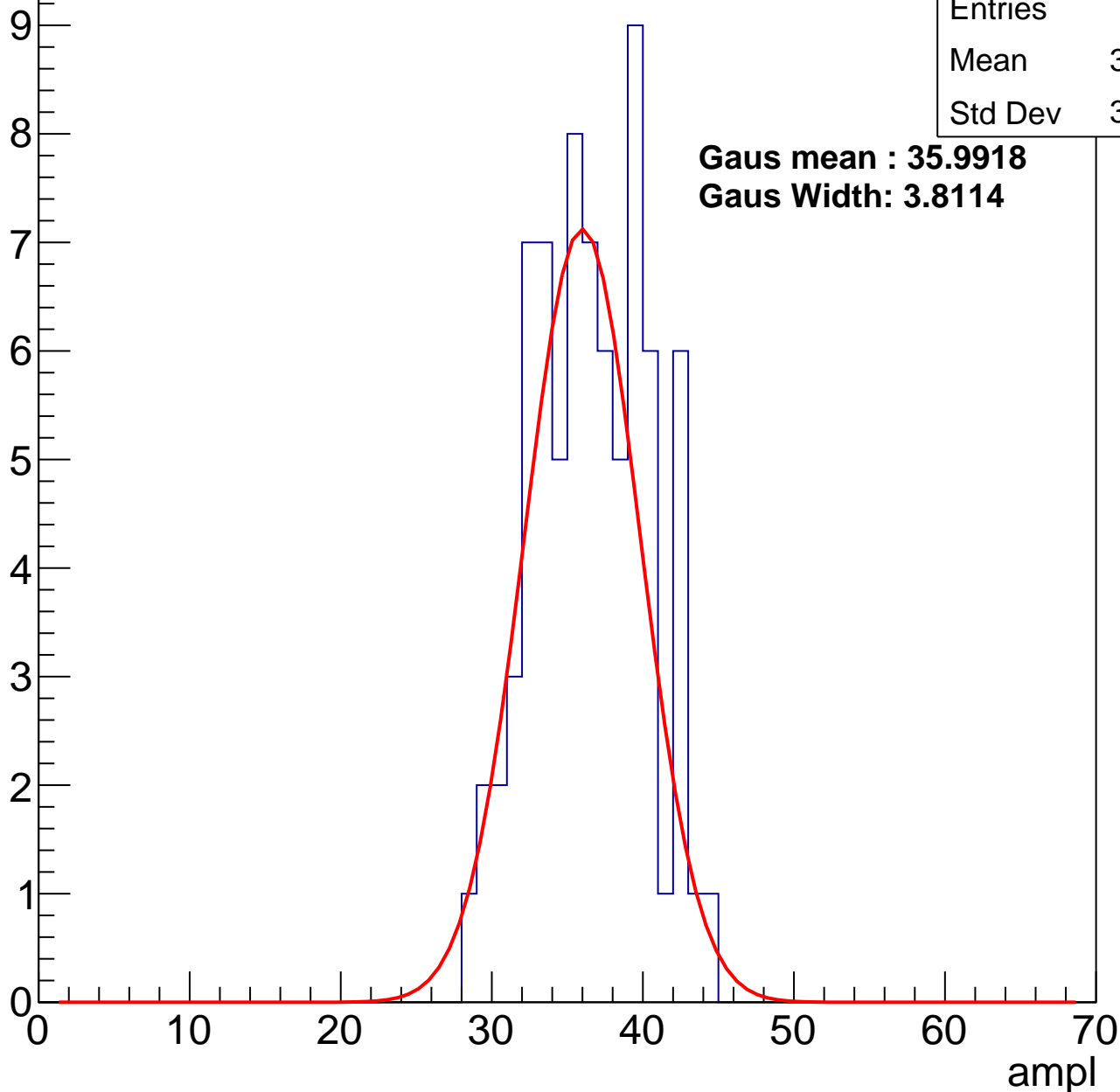
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	36.09
Std Dev	3.725

**Gaus mean : 35.9918**

**Gaus Width: 3.8114**



# B1L103S, U16-ch120, adc2

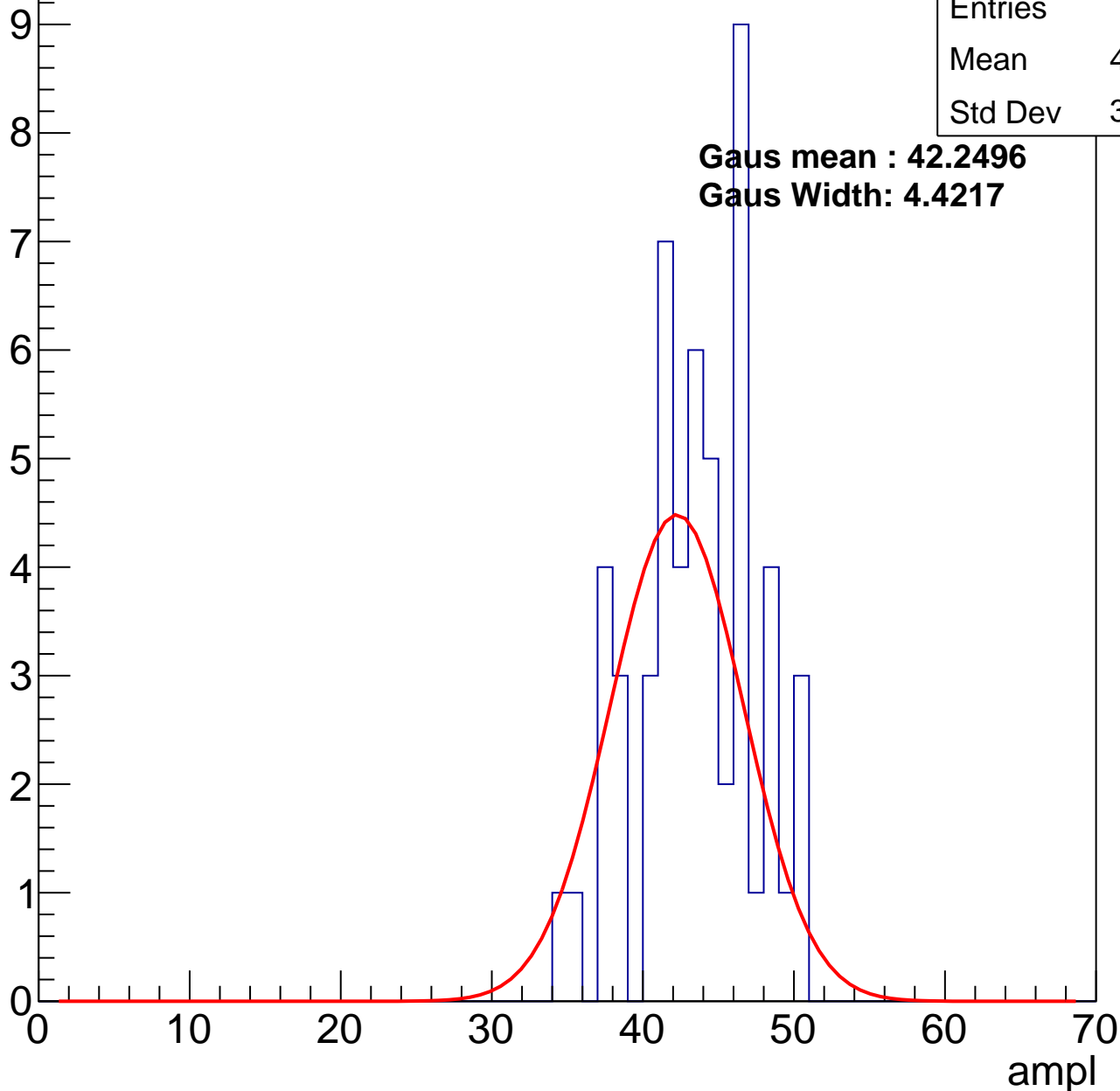
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	43.07
Std Dev	3.887

**Gaus mean : 42.2496**

**Gaus Width: 4.4217**

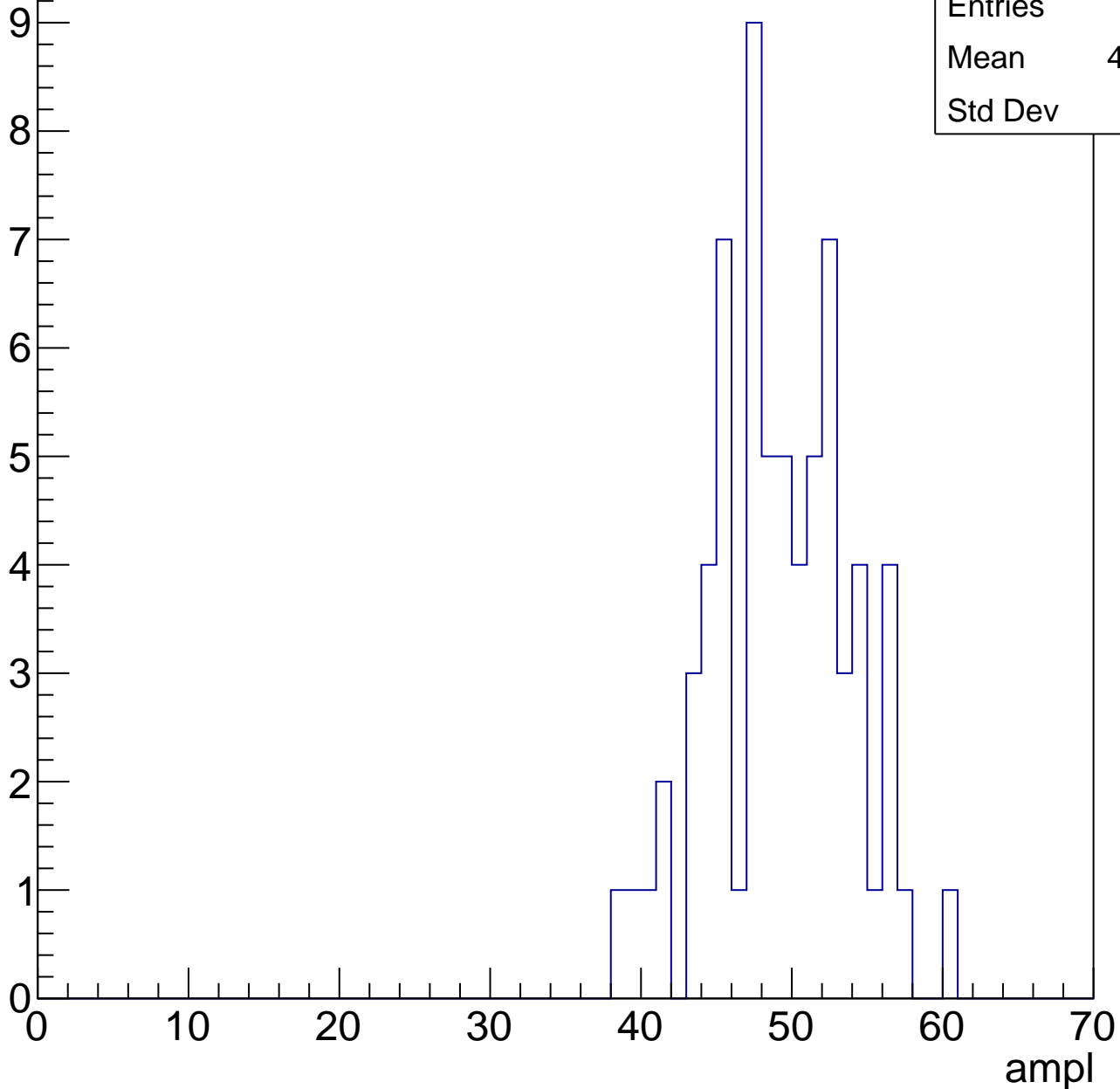


# B1L103S, U16-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	48.74
Std Dev	4.58

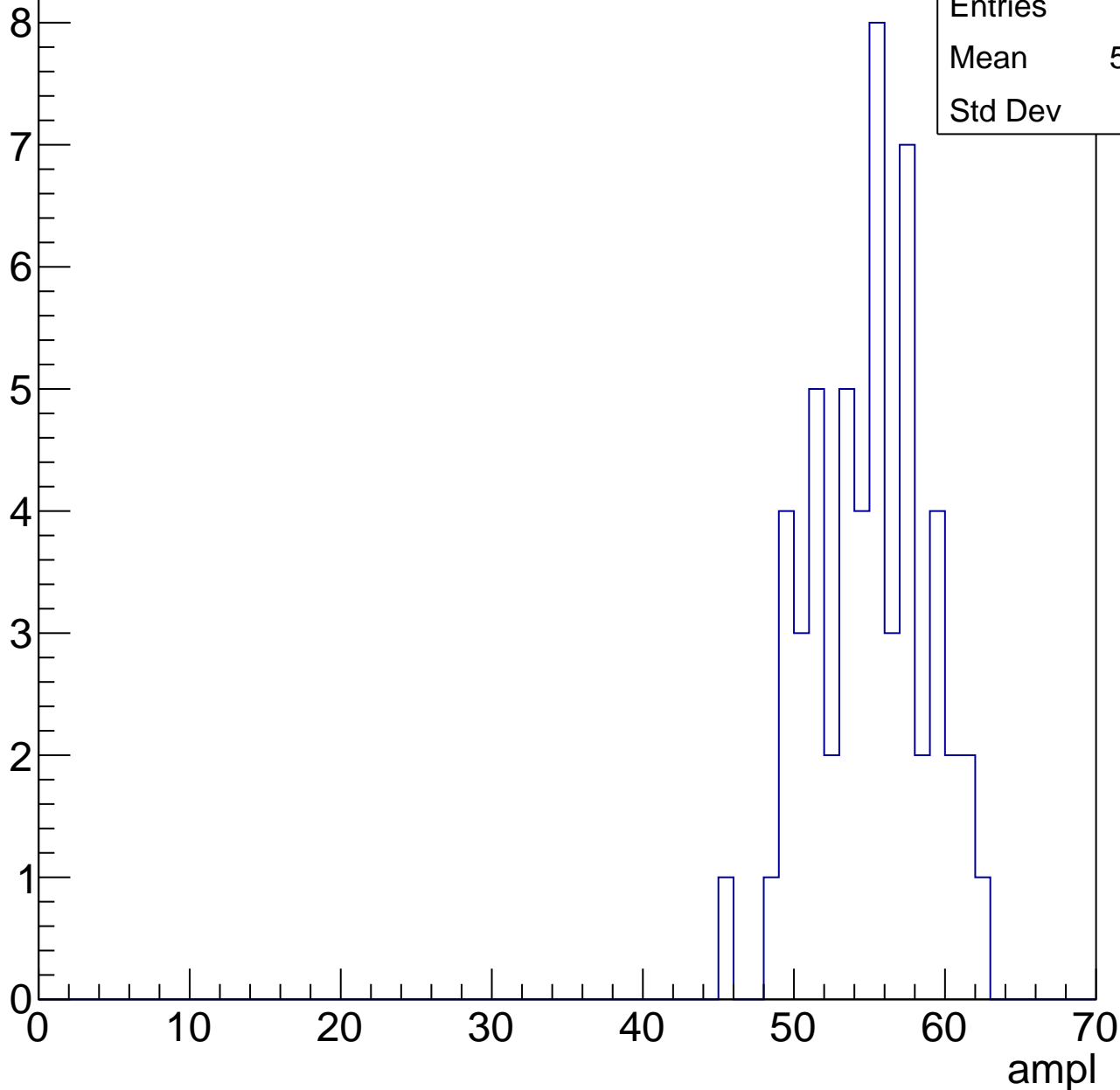


# B1L103S, U16-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	54.48
Std Dev	3.75

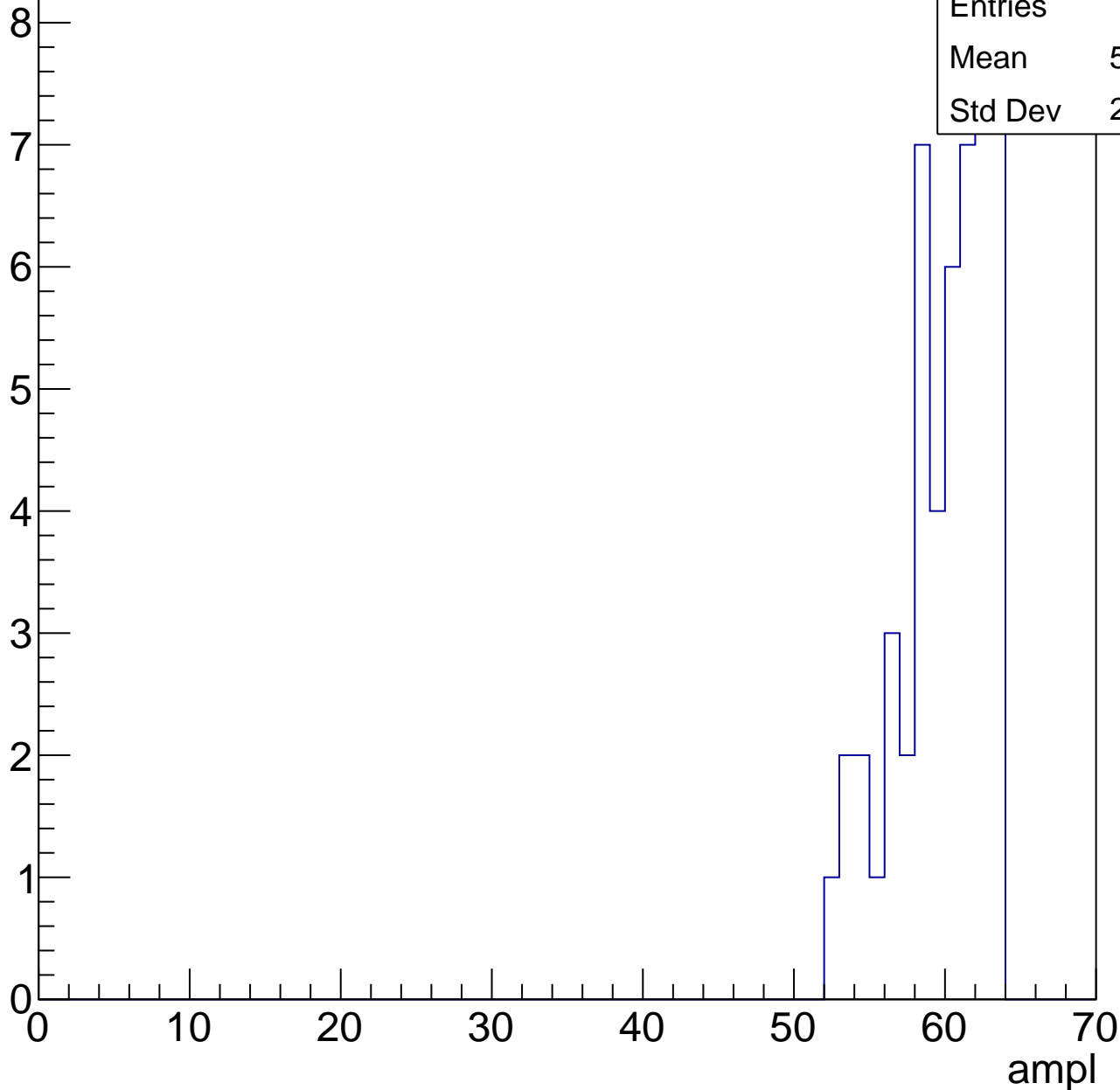


# B1L103S, U16-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	59.45
Std Dev	2.979



# B1L103S, U16-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

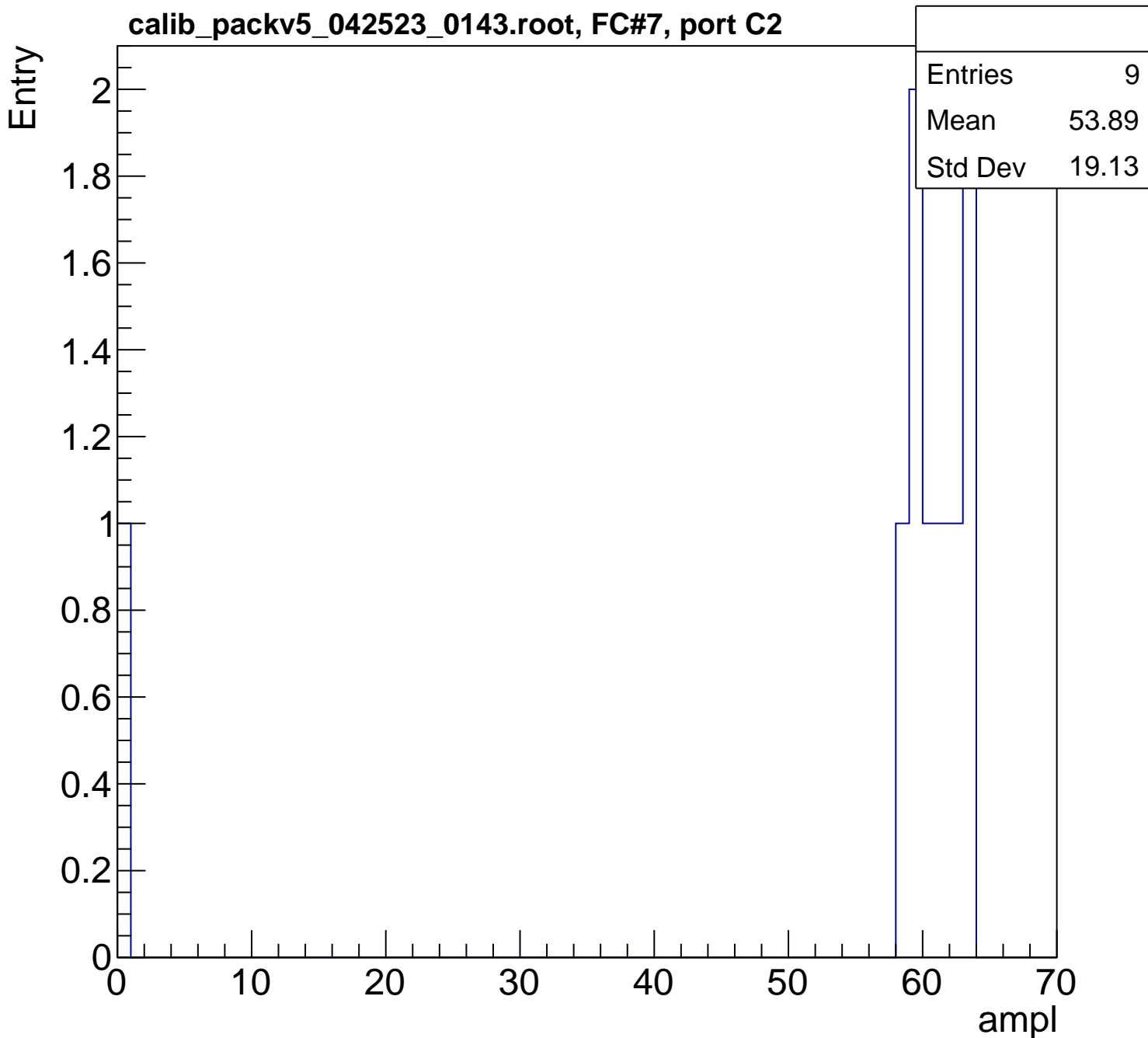
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	9
Mean	53.89
Std Dev	19.13

0 10 20 30 40 50 60 70

ampl





# B1L103S, U16-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U16-ch121, adc0

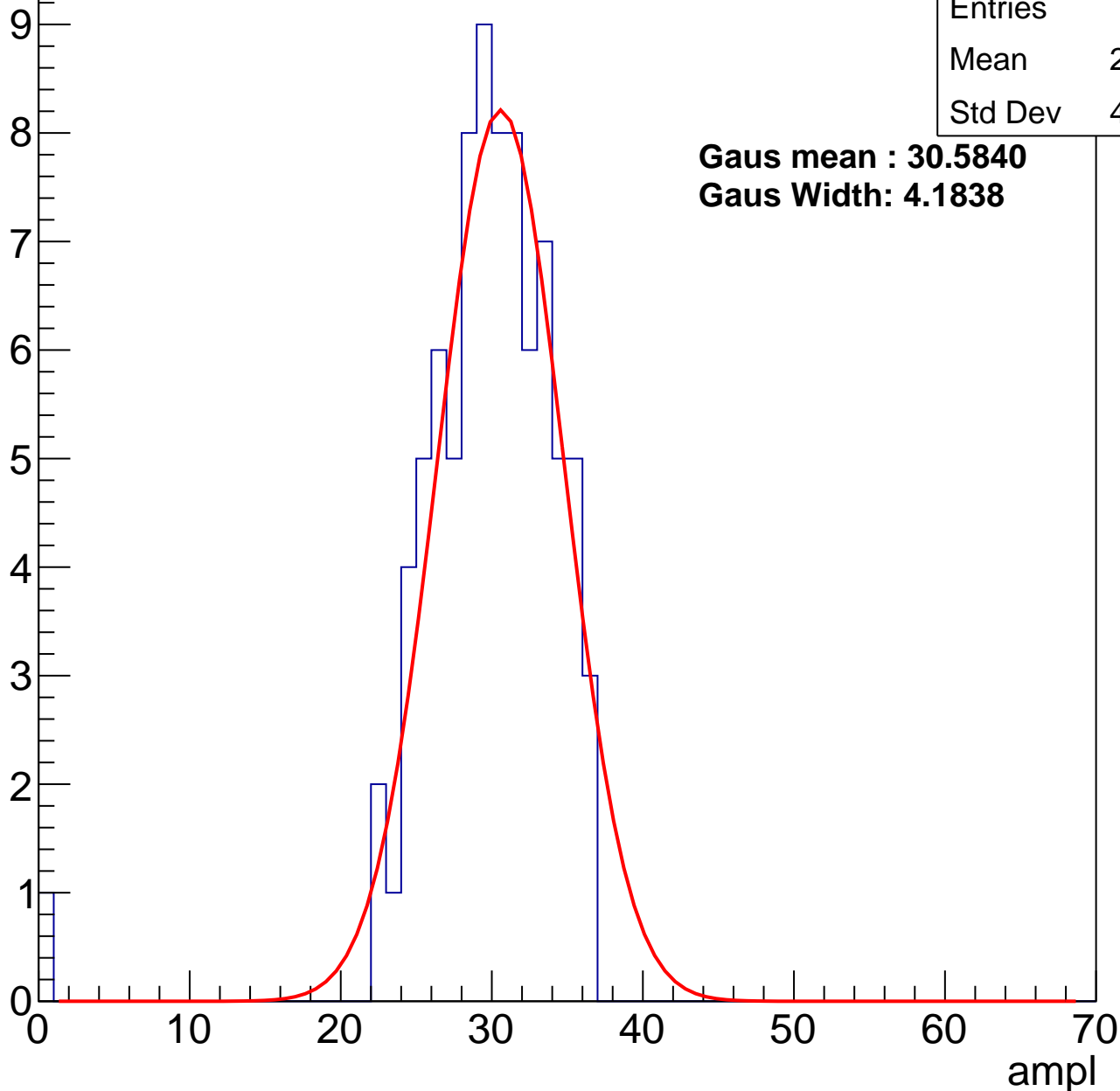
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	29.25
Std Dev	4.772

**Gaus mean : 30.5840**

**Gaus Width: 4.1838**



# B1L103S, U16-ch121, adc1

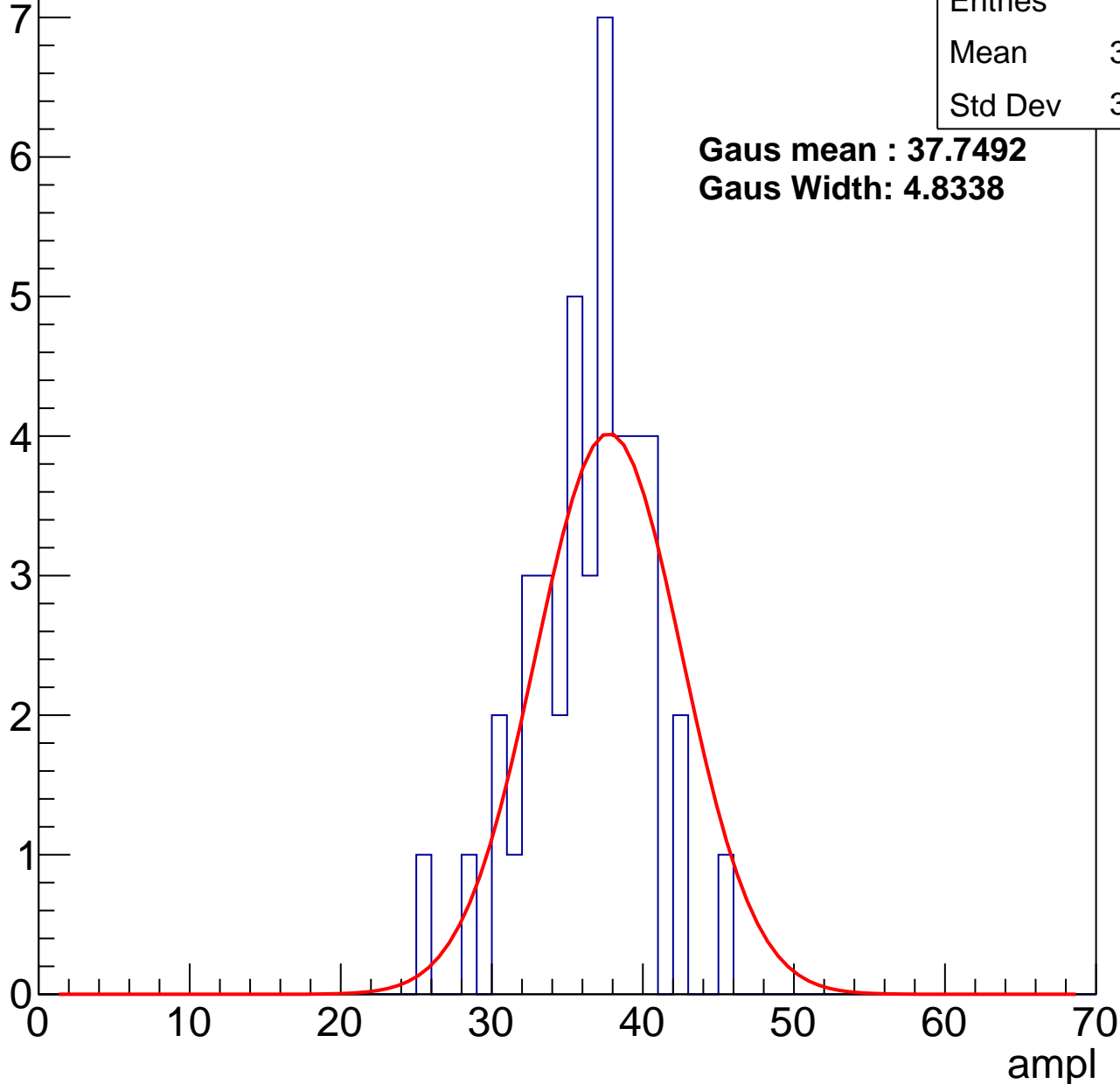
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	43
Mean	35.95
Std Dev	3.876

**Gaus mean : 37.7492**

**Gaus Width: 4.8338**



# B1L103S, U16-ch121, adc2

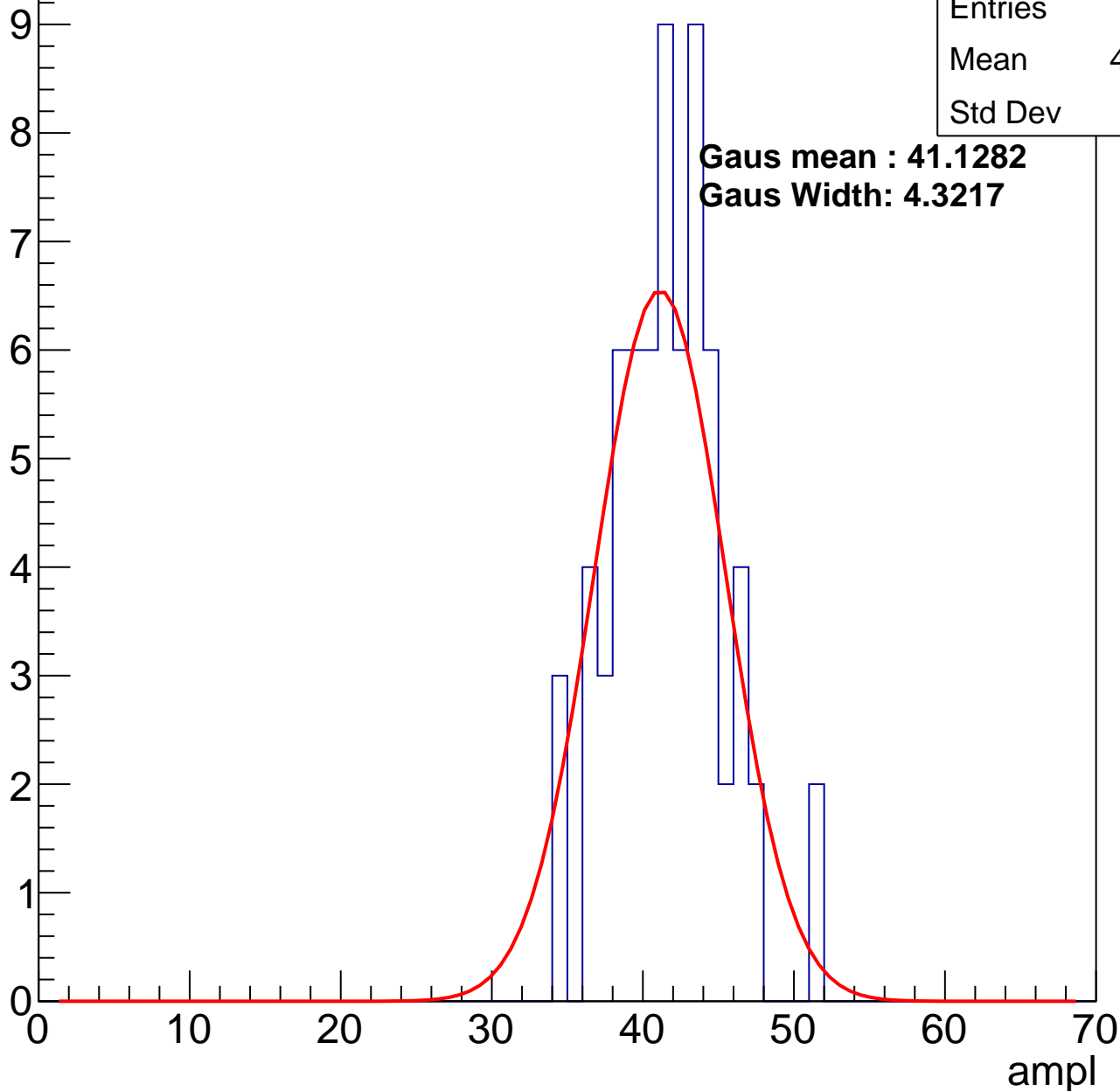
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	41.19
Std Dev	3.59

**Gaus mean : 41.1282**

**Gaus Width: 4.3217**



# B1L103S, U16-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

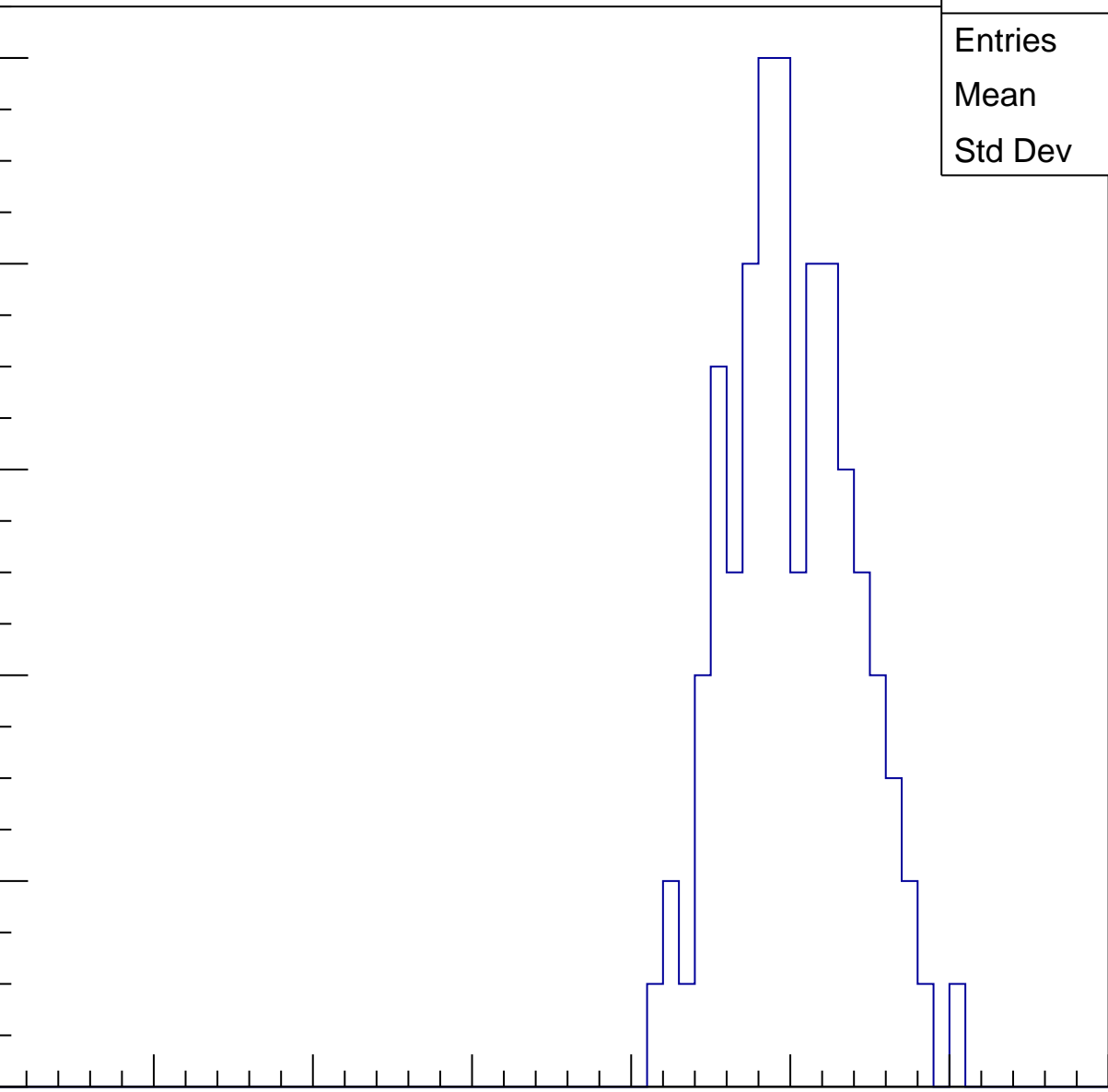
Entries	91
Mean	49.64
Std Dev	3.938

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

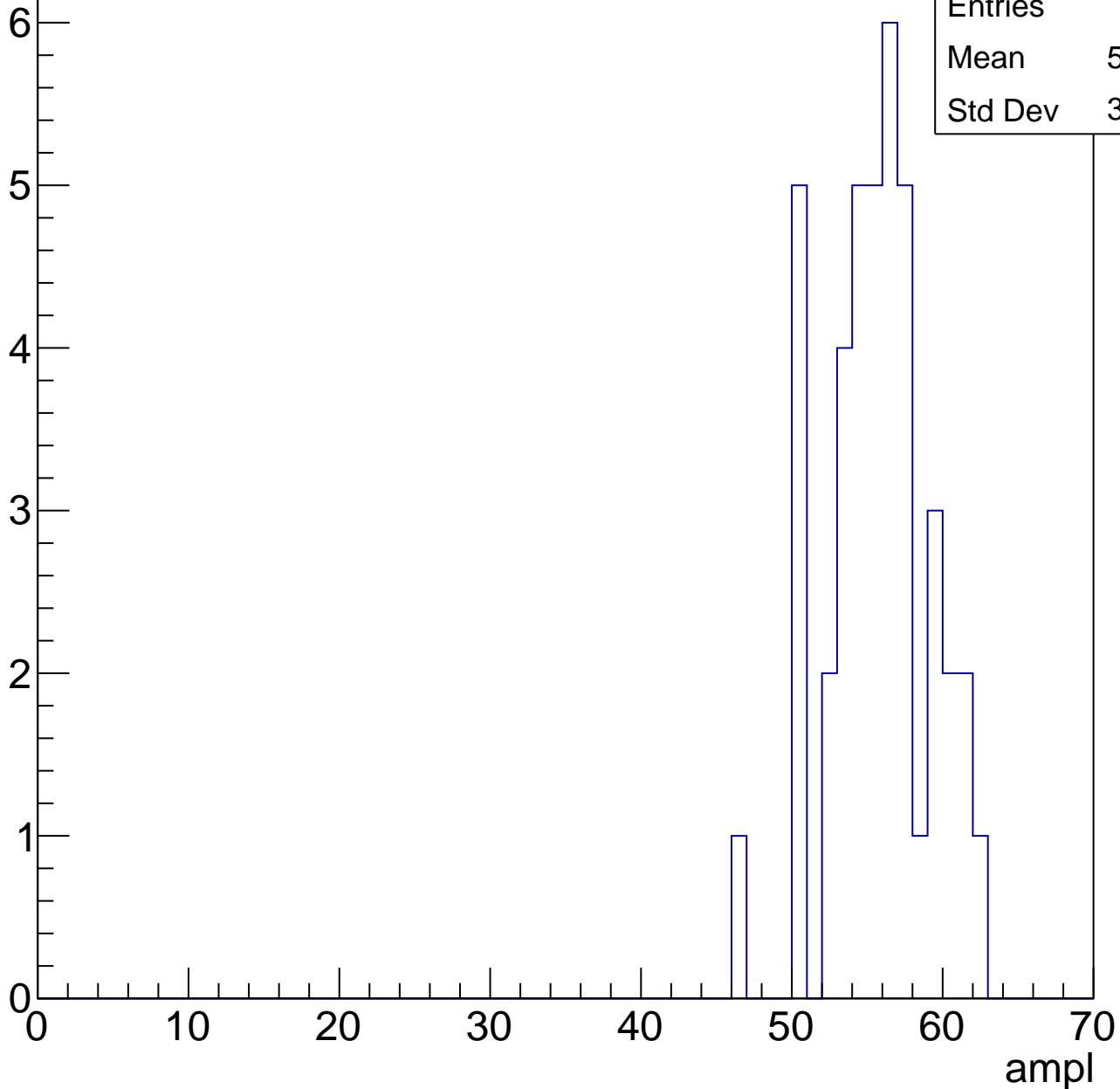


# B1L103S, U16-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	42
Mean	55.17
Std Dev	3.443

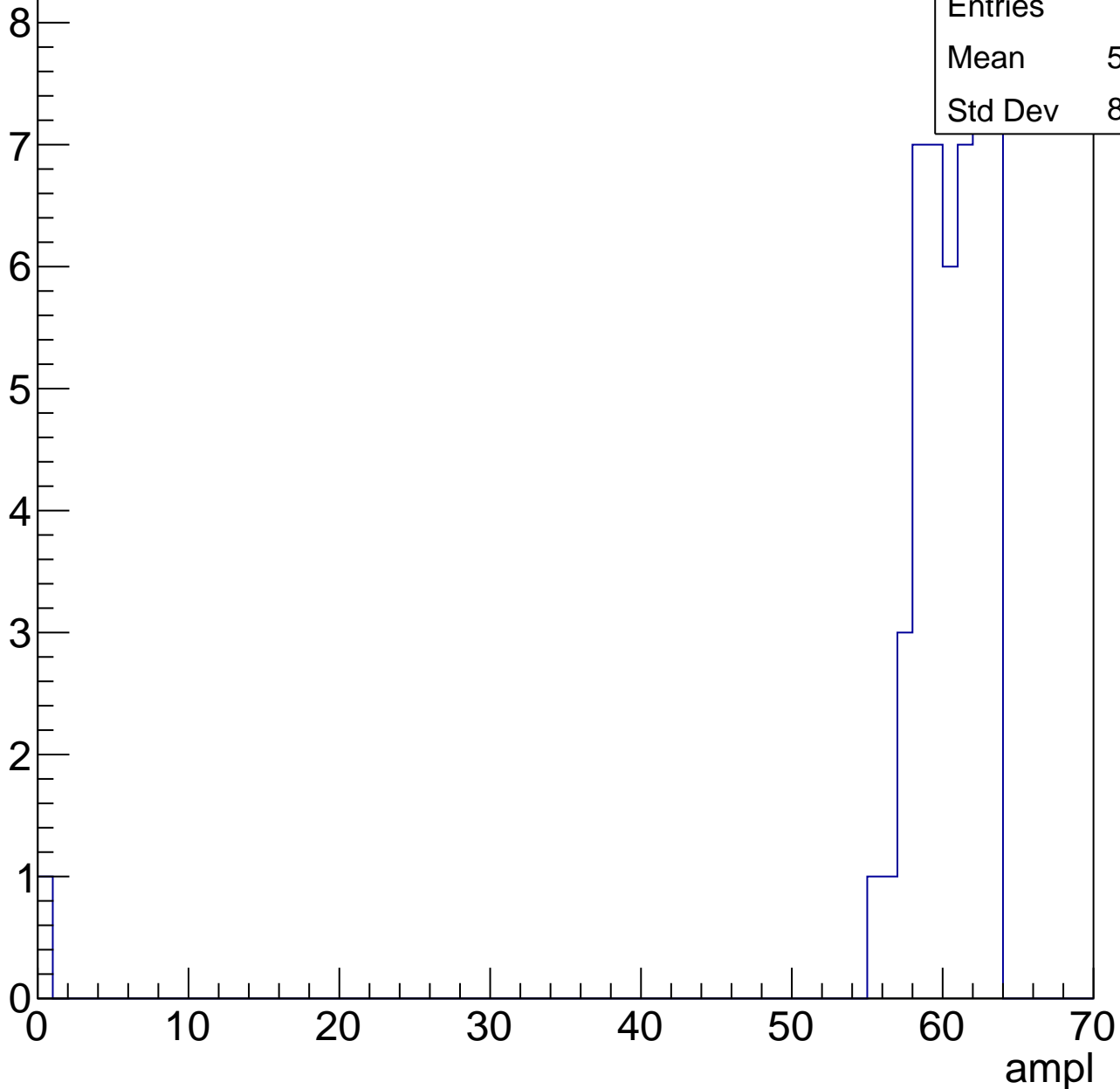


# B1L103S, U16-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	58.94
Std Dev	8.758



# B1L103S, U16-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

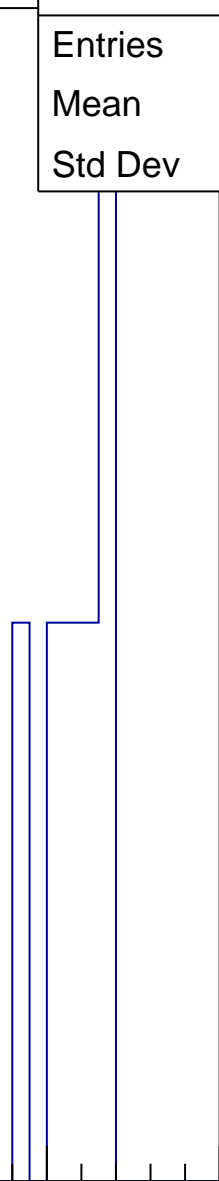
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.17
Std Dev	1.772

0 10 20 30 40 50 60 70

ampl





# B1L103S, U16-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U16-ch122, adc0

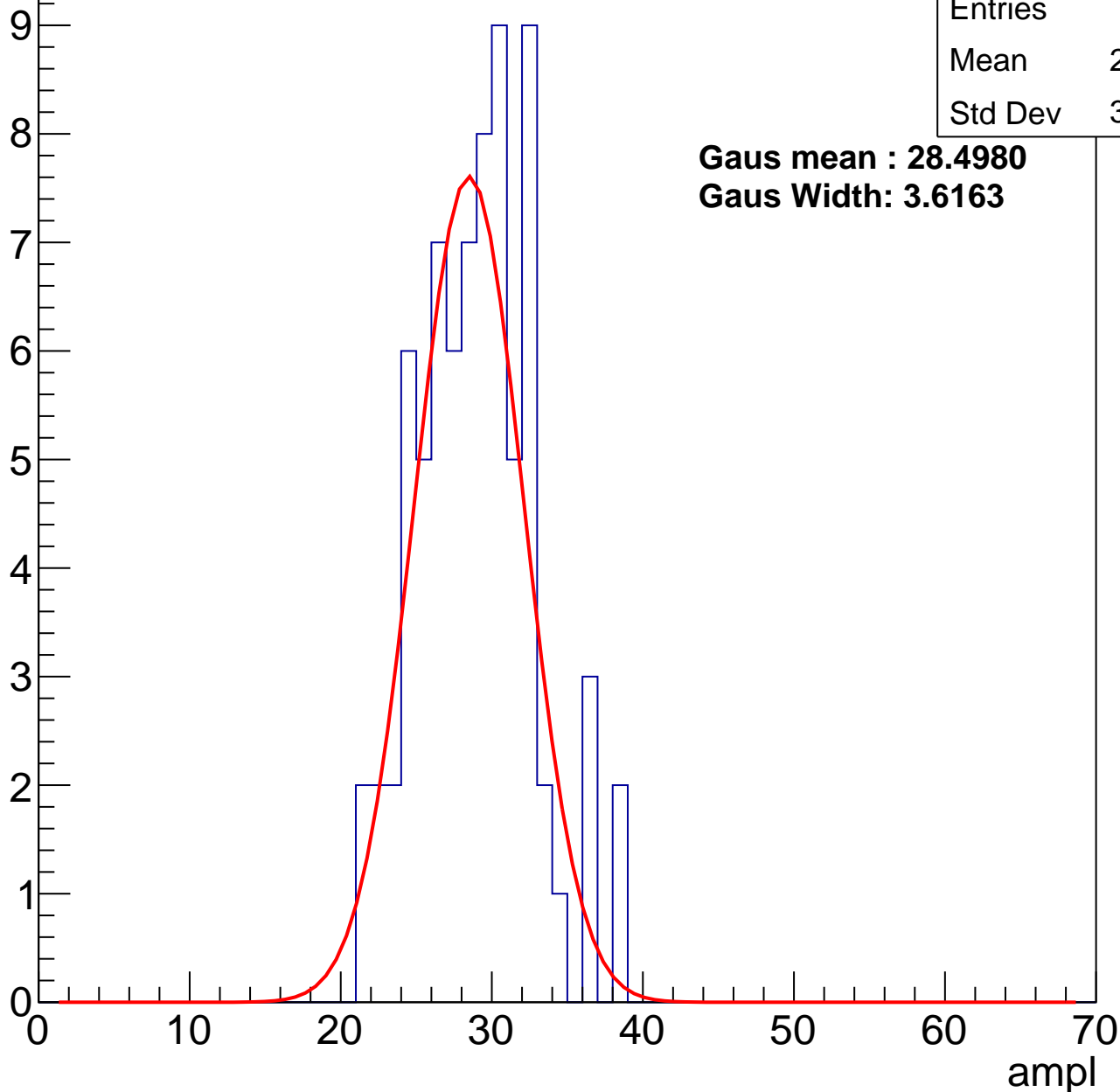
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	28.55
Std Dev	3.775

**Gaus mean : 28.4980**

**Gaus Width: 3.6163**



# B1L103S, U16-ch122, adc1

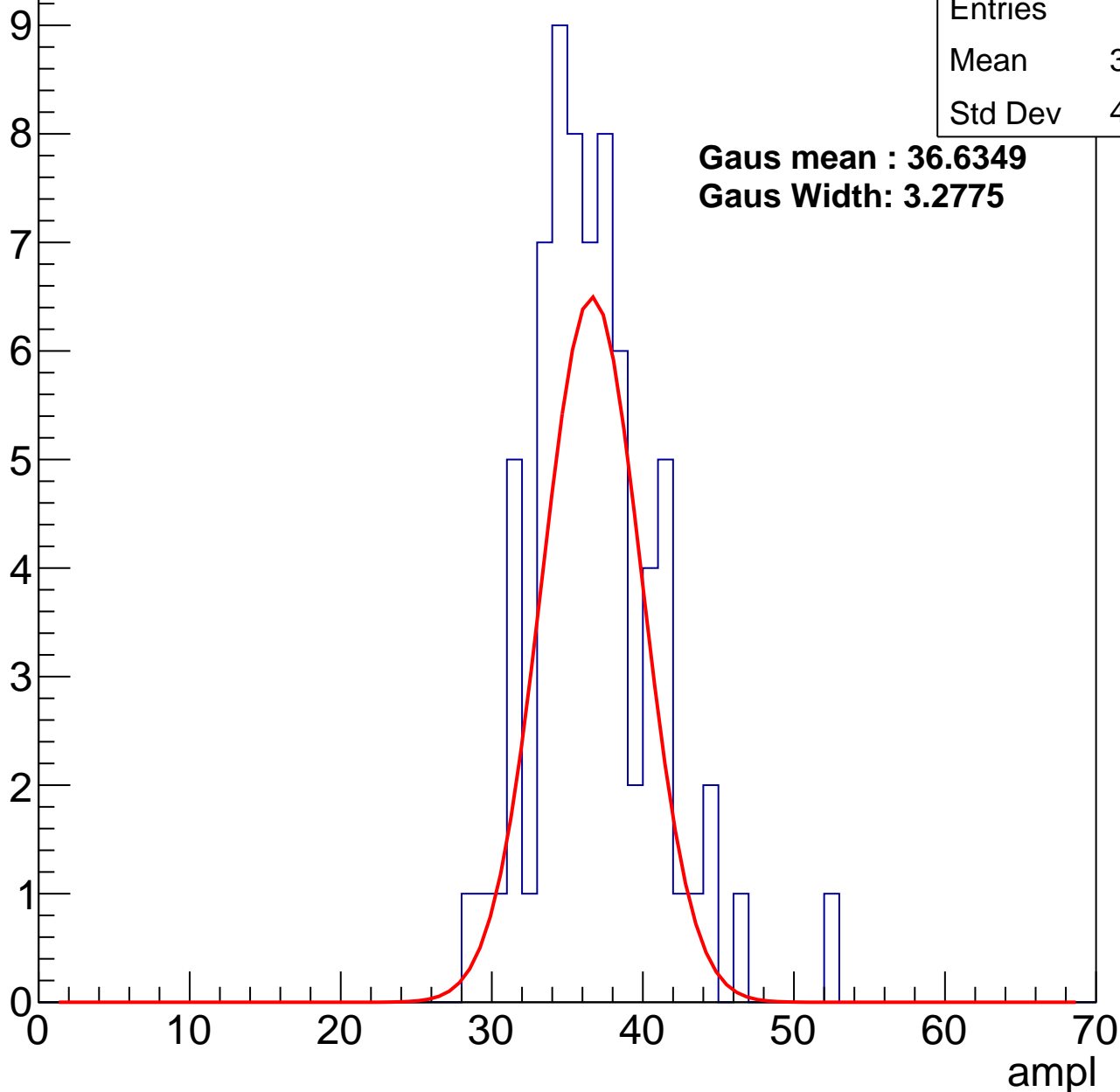
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	36.35
Std Dev	4.105

**Gaus mean : 36.6349**

**Gaus Width: 3.2775**



# B1L103S, U16-ch122, adc2

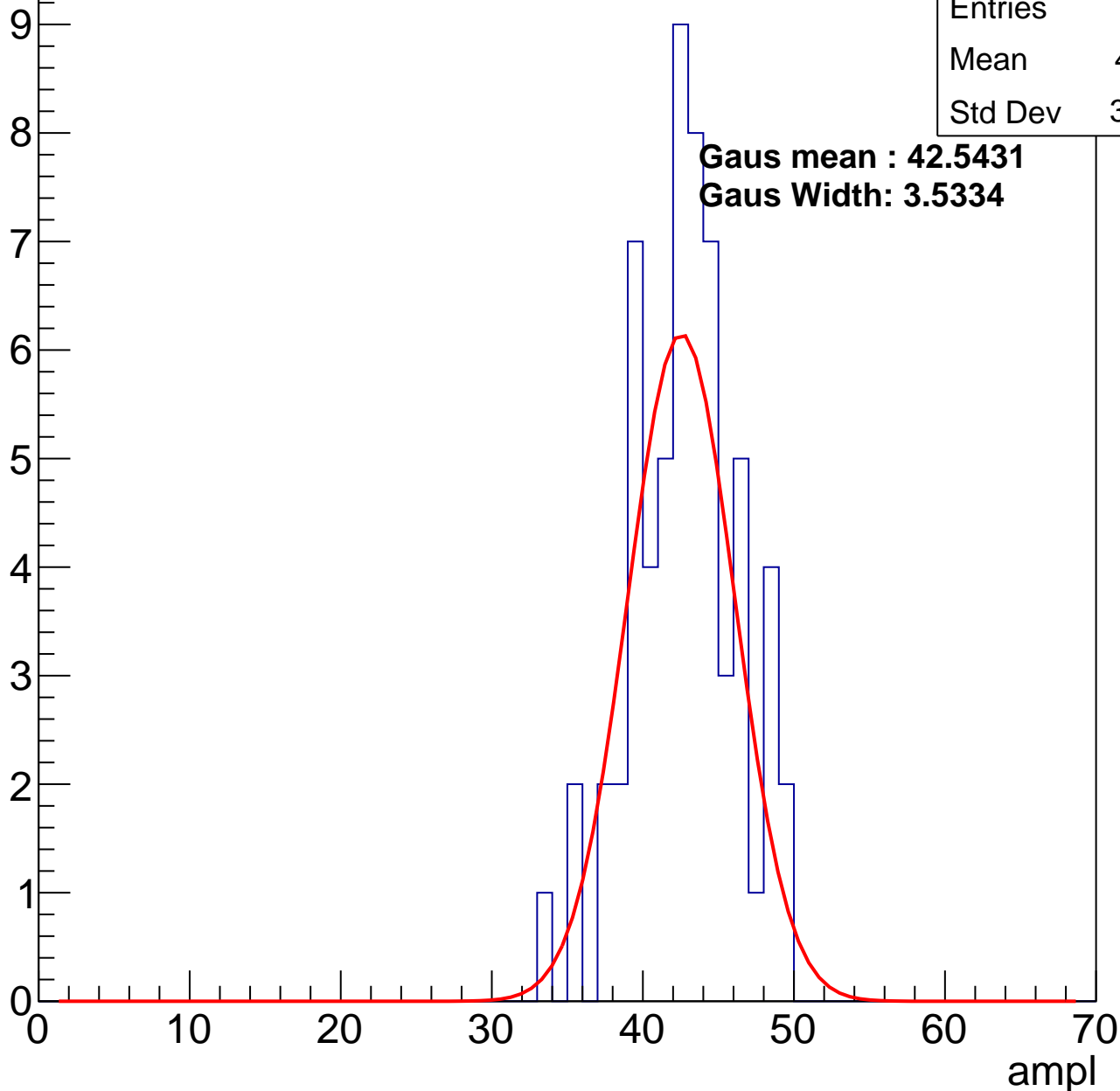
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	42.31
Std Dev	3.476

**Gaus mean : 42.5431**

**Gaus Width: 3.5334**

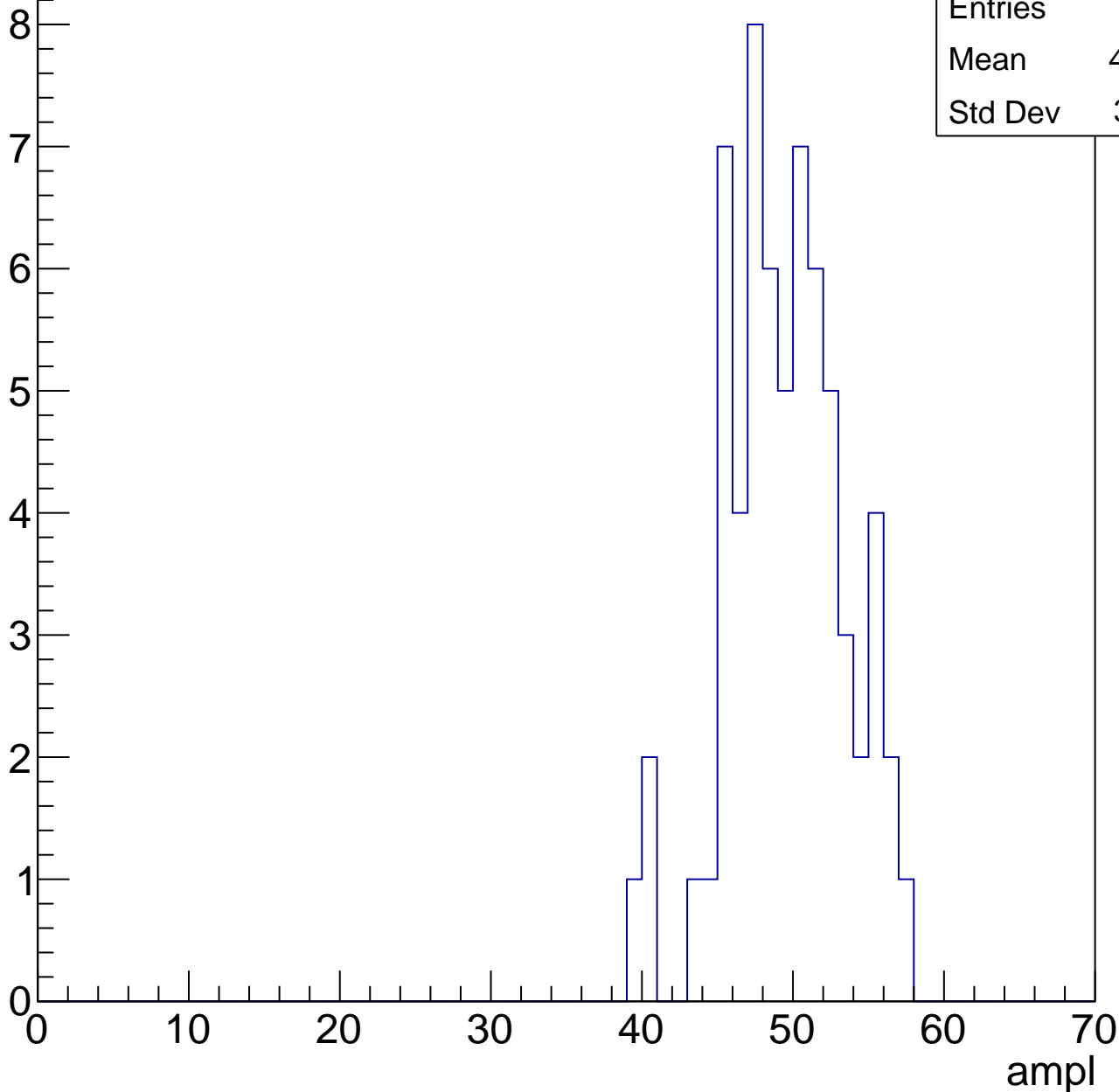


# B1L103S, U16-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	49.02
Std Dev	3.901

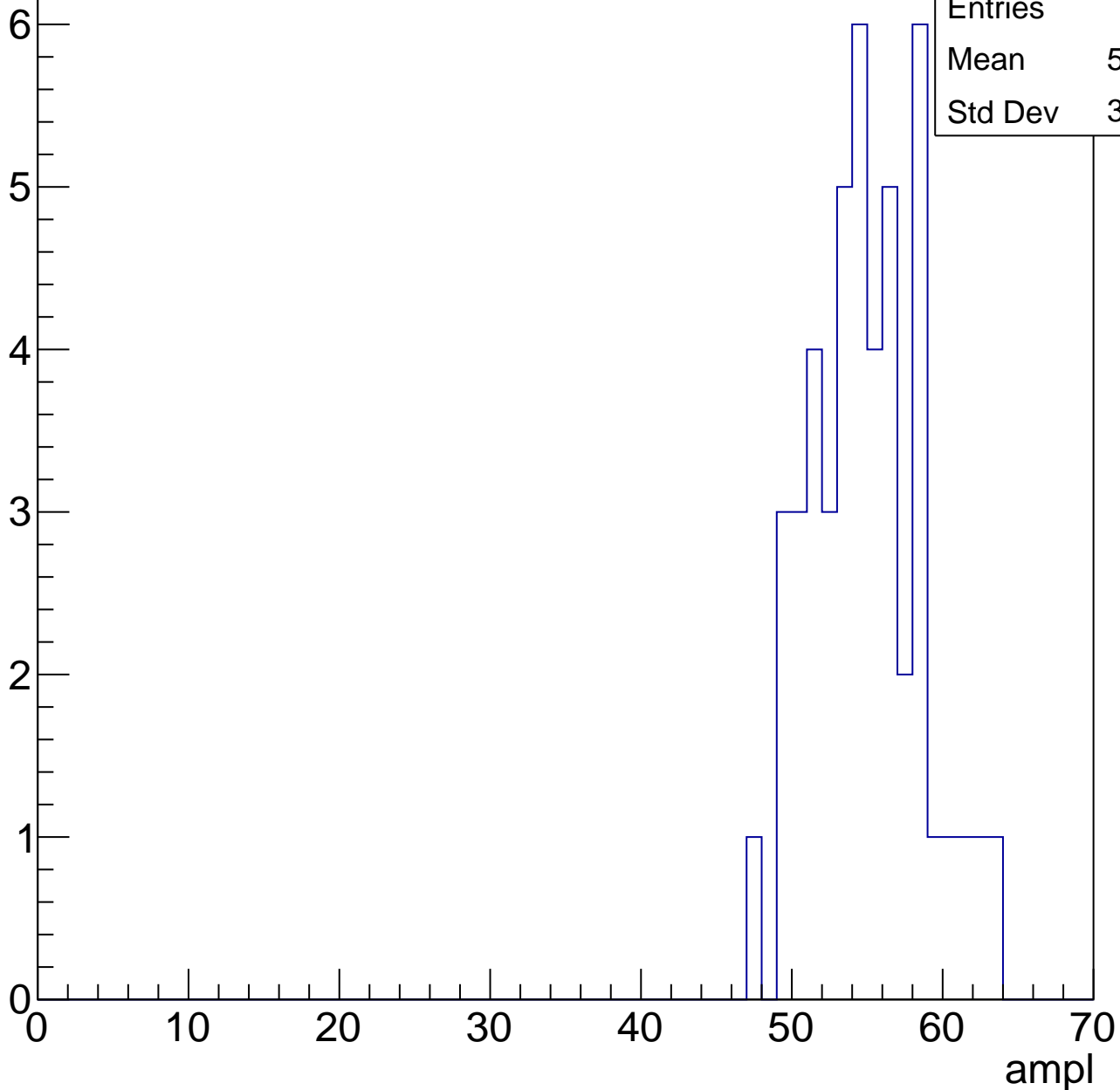


# B1L103S, U16-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

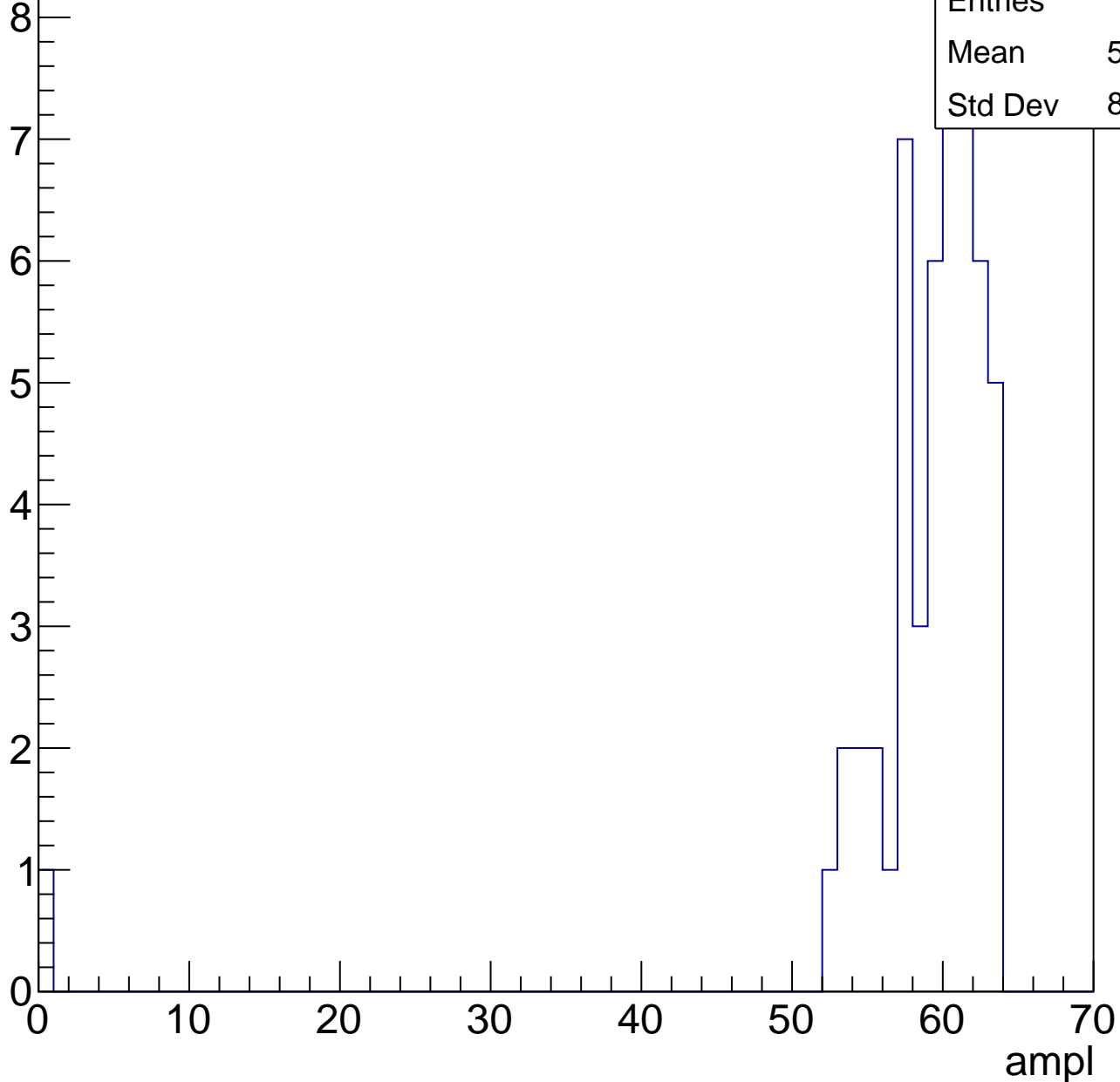
Entries	47
Mean	54.47
Std Dev	3.596



# B1L103S, U16-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

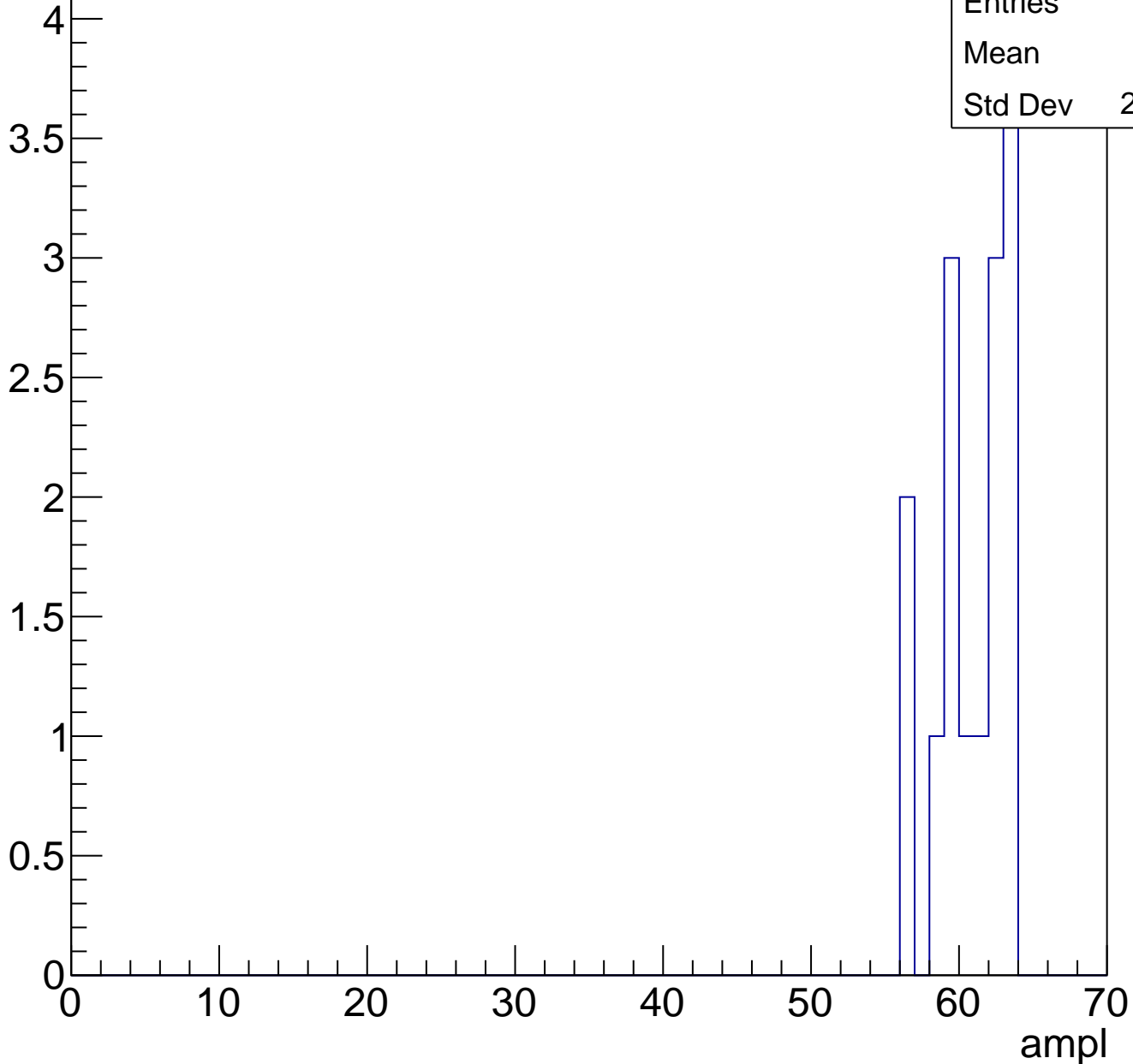
Entry



# B1L103S, U16-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch123, adc0

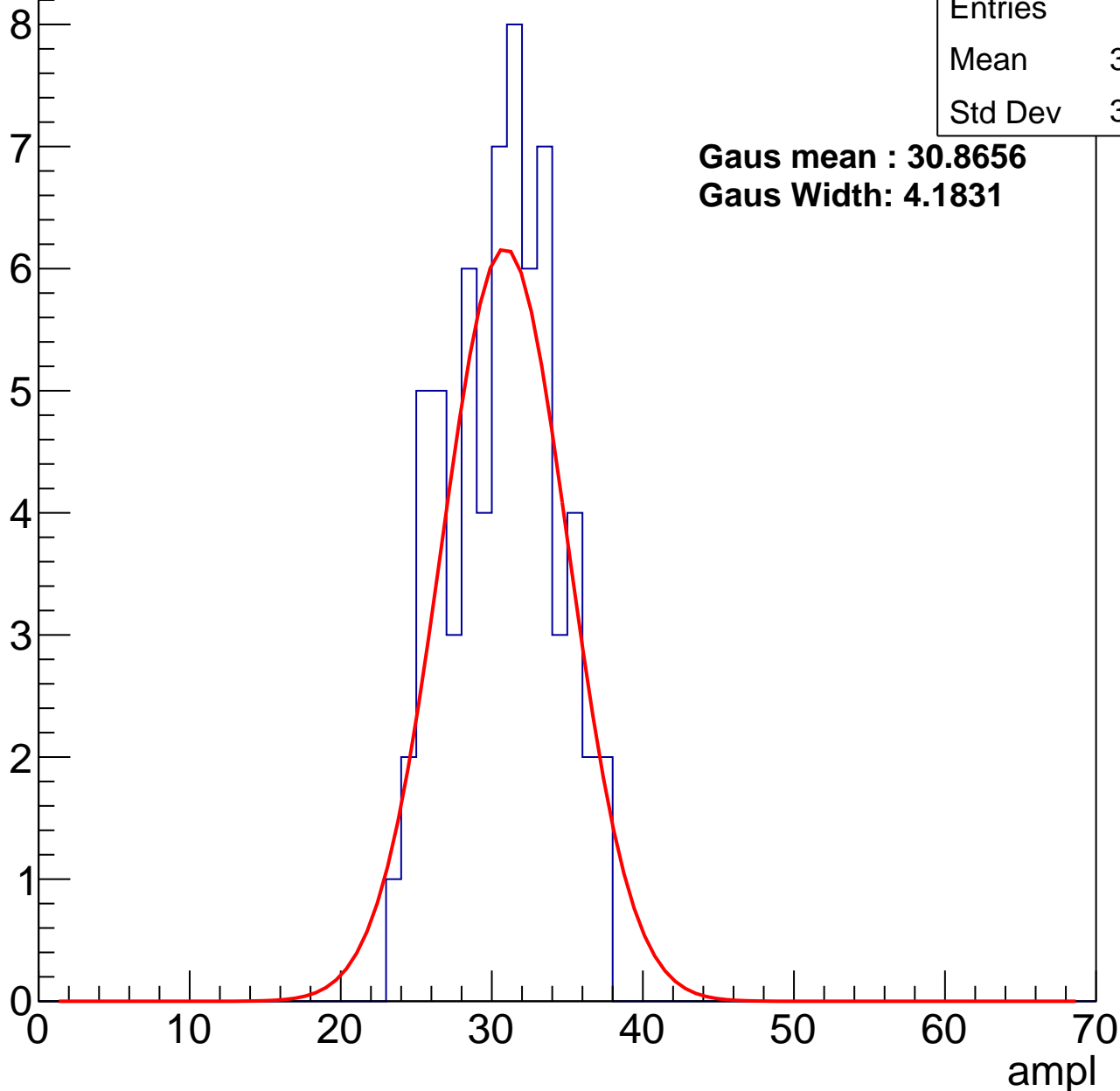
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	30.15
Std Dev	3.492

**Gaus mean : 30.8656**

**Gaus Width: 4.1831**



# B1L103S, U16-ch123, adc1

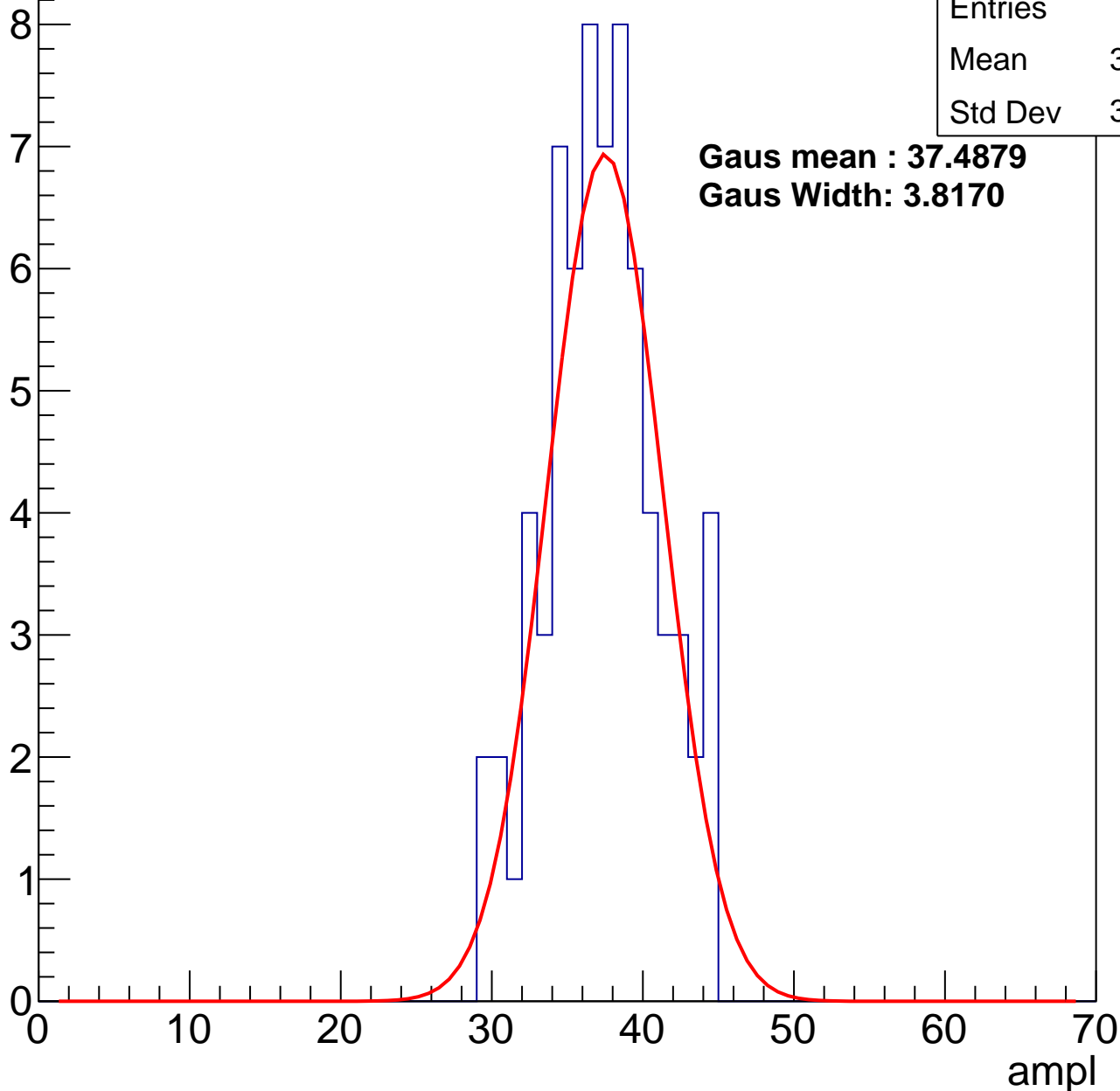
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	36.86
Std Dev	3.708

**Gaus mean : 37.4879**

**Gaus Width: 3.8170**



# B1L103S, U16-ch123, adc2

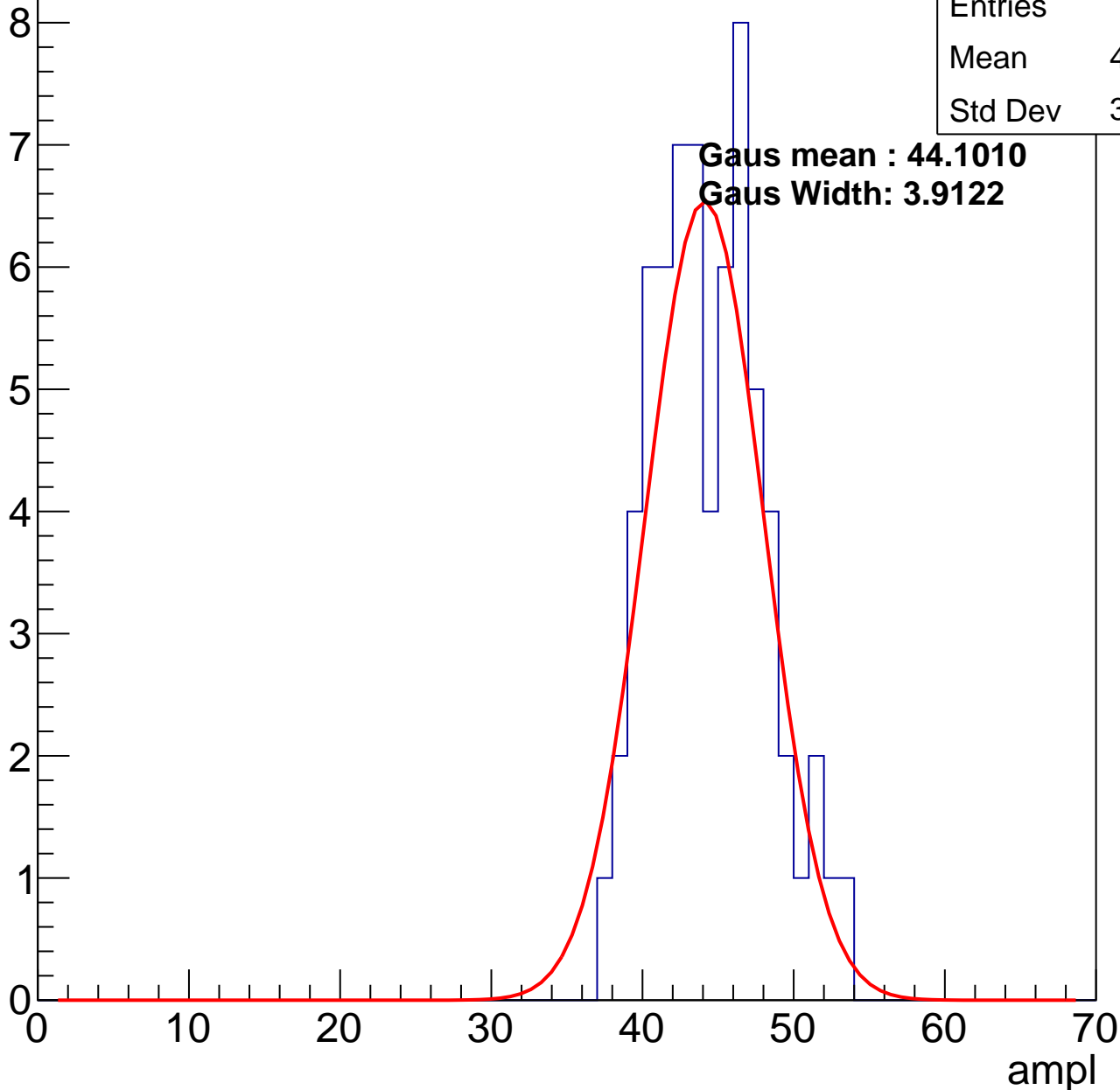
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	43.97
Std Dev	3.628

**Gaus mean : 44.1010**

**Gaus Width: 3.9122**

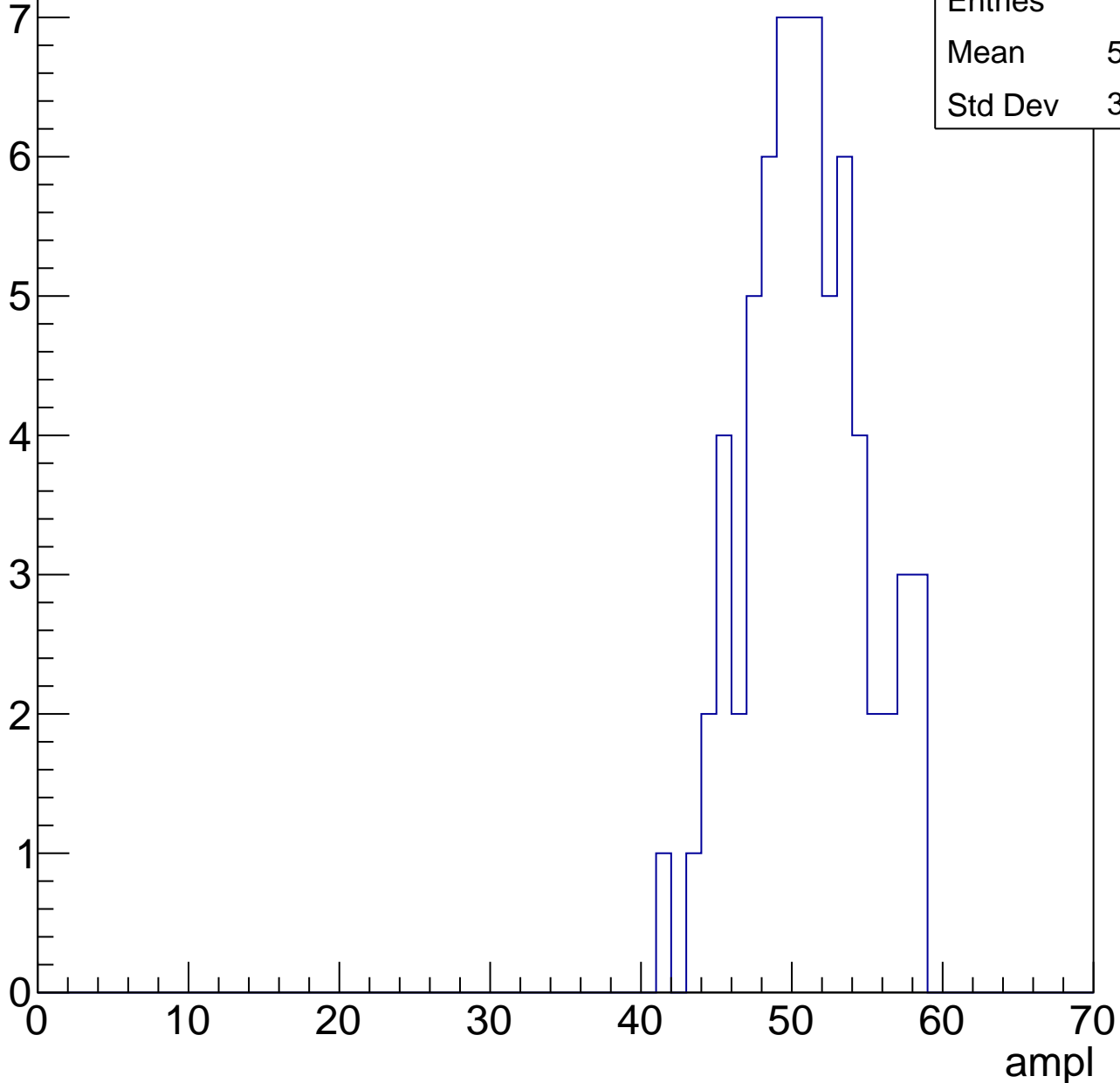


# B1L103S, U16-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	50.42
Std Dev	3.872

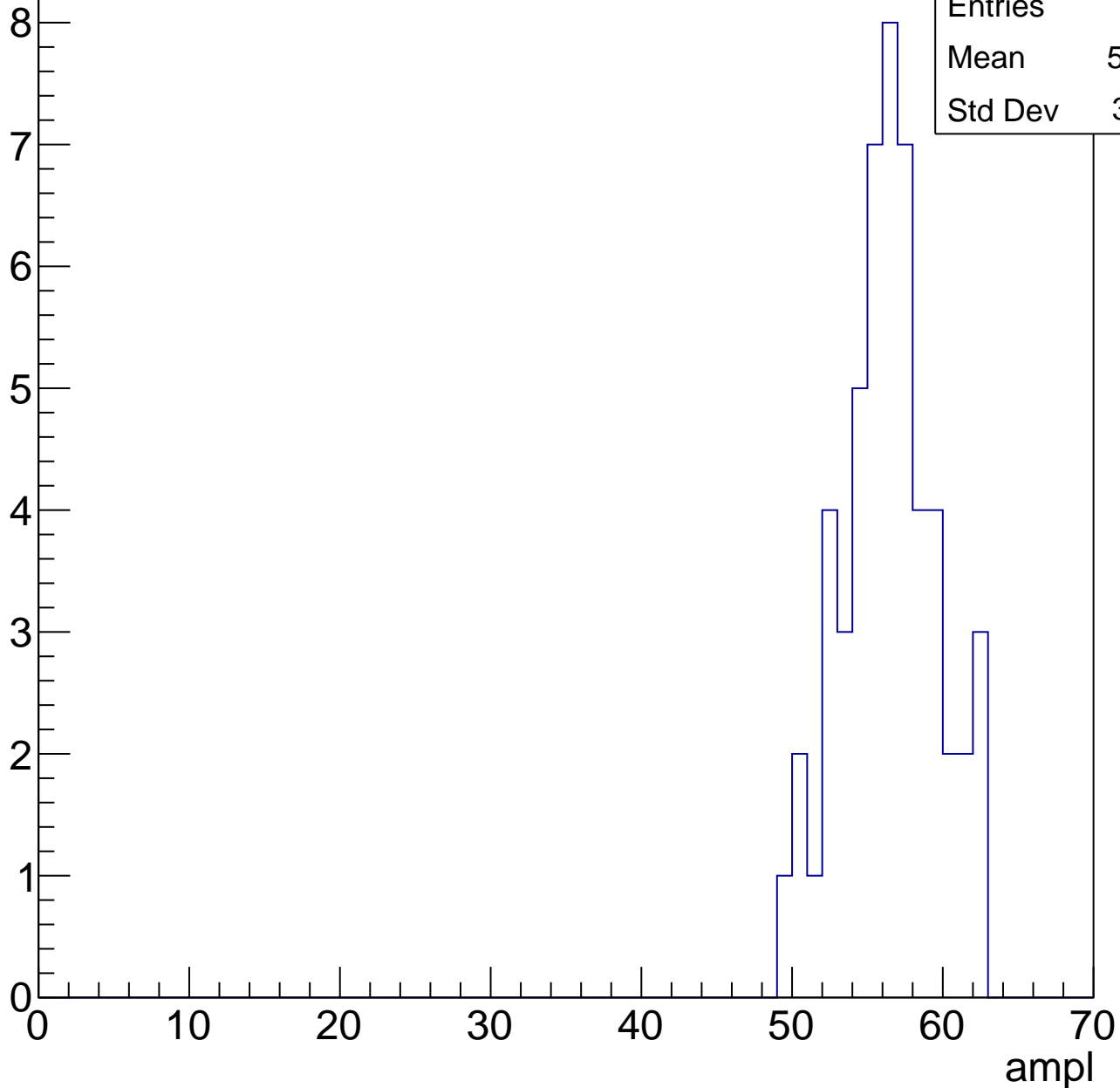


# B1L103S, U16-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	55.94
Std Dev	3.111

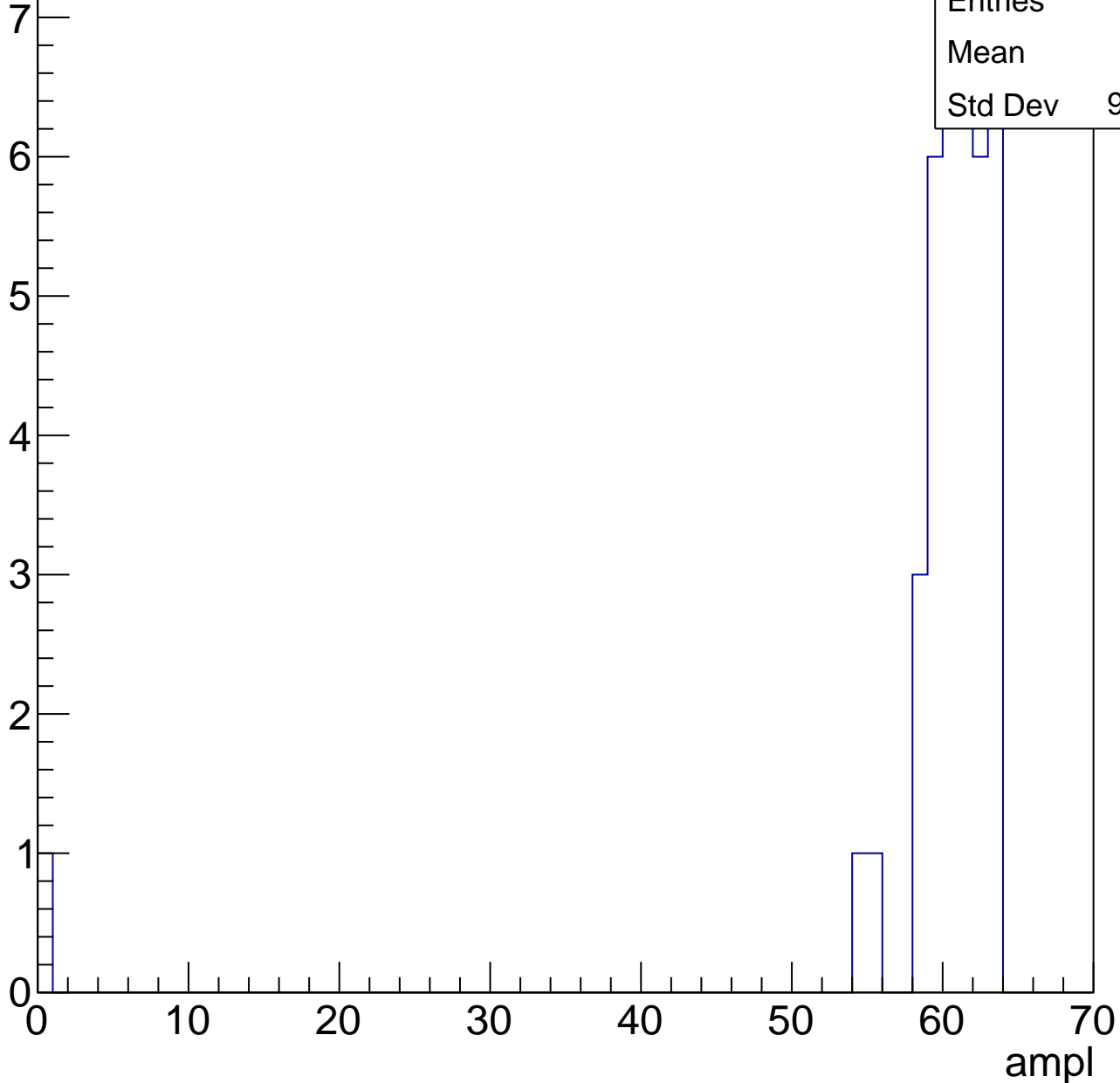


# B1L103S, U16-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	39
Mean	58.9
Std Dev	9.774



# B1L103S, U16-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch124, adc0

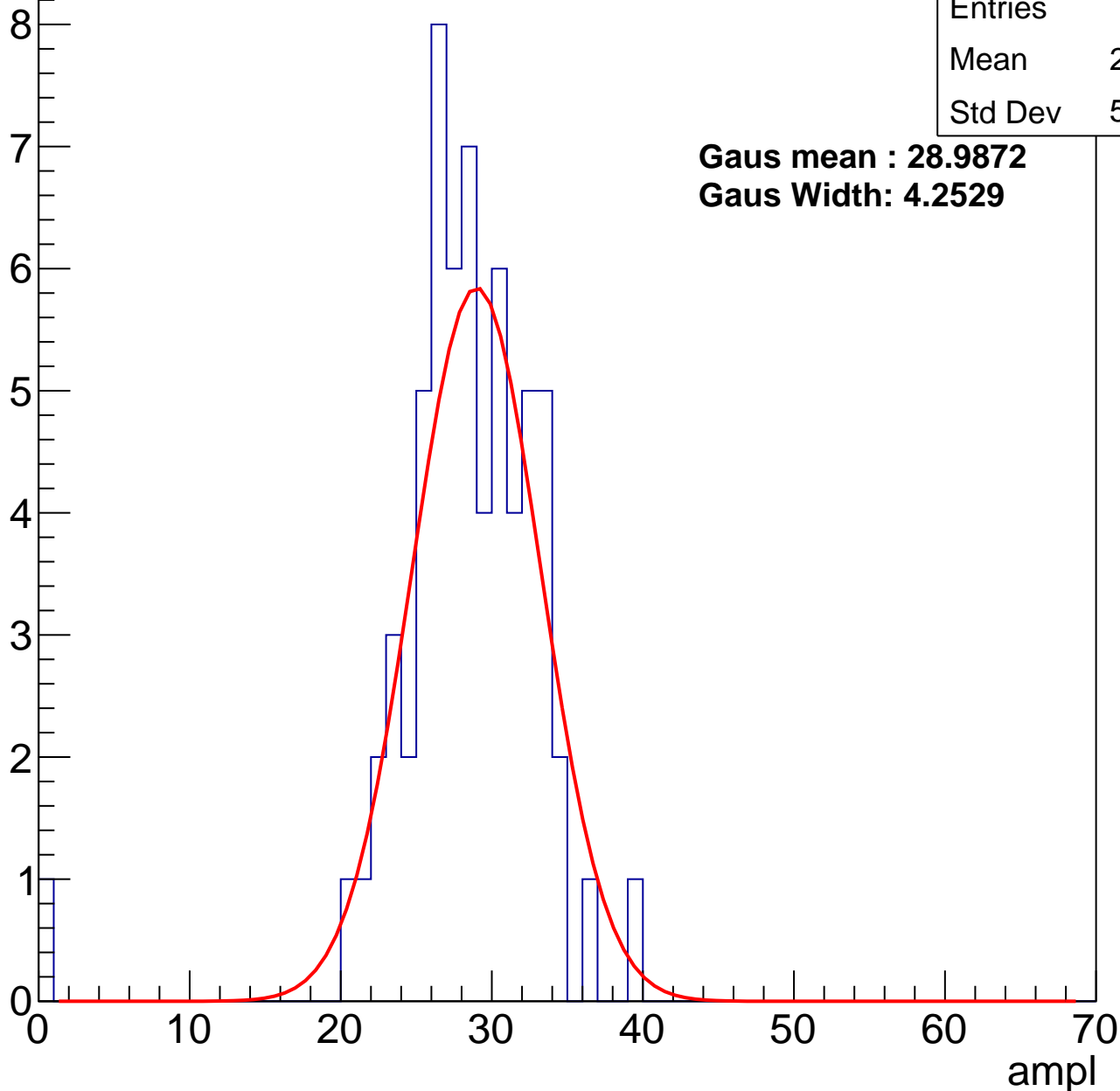
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	27.83
Std Dev	5.128

**Gaus mean : 28.9872**

**Gaus Width: 4.2529**



# B1L103S, U16-ch124, adc1

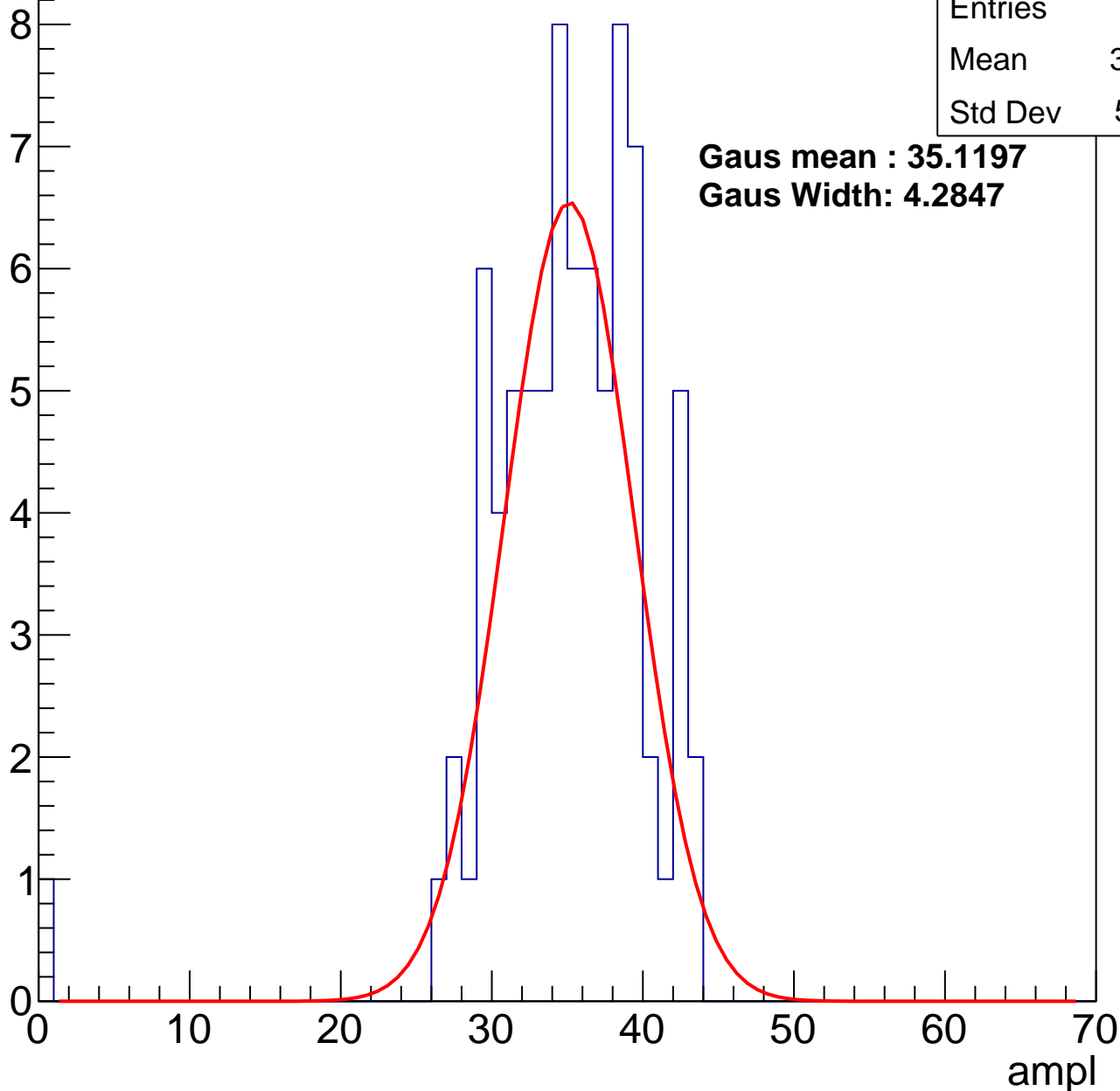
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	34.49
Std Dev	5.701

**Gaus mean : 35.1197**

**Gaus Width: 4.2847**



# B1L103S, U16-ch124, adc2

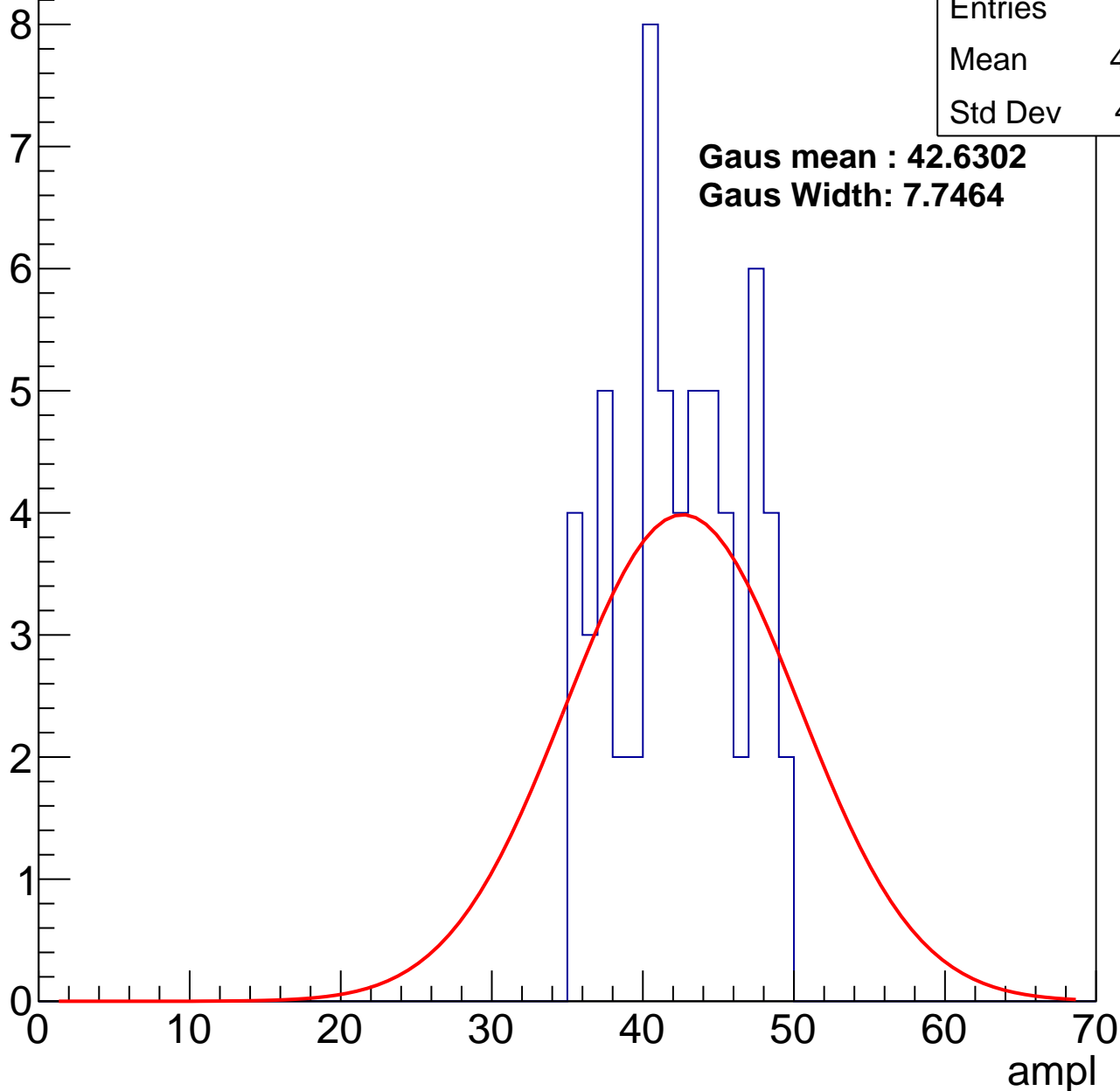
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	41.95
Std Dev	4.051

**Gaus mean : 42.6302**

**Gaus Width: 7.7464**

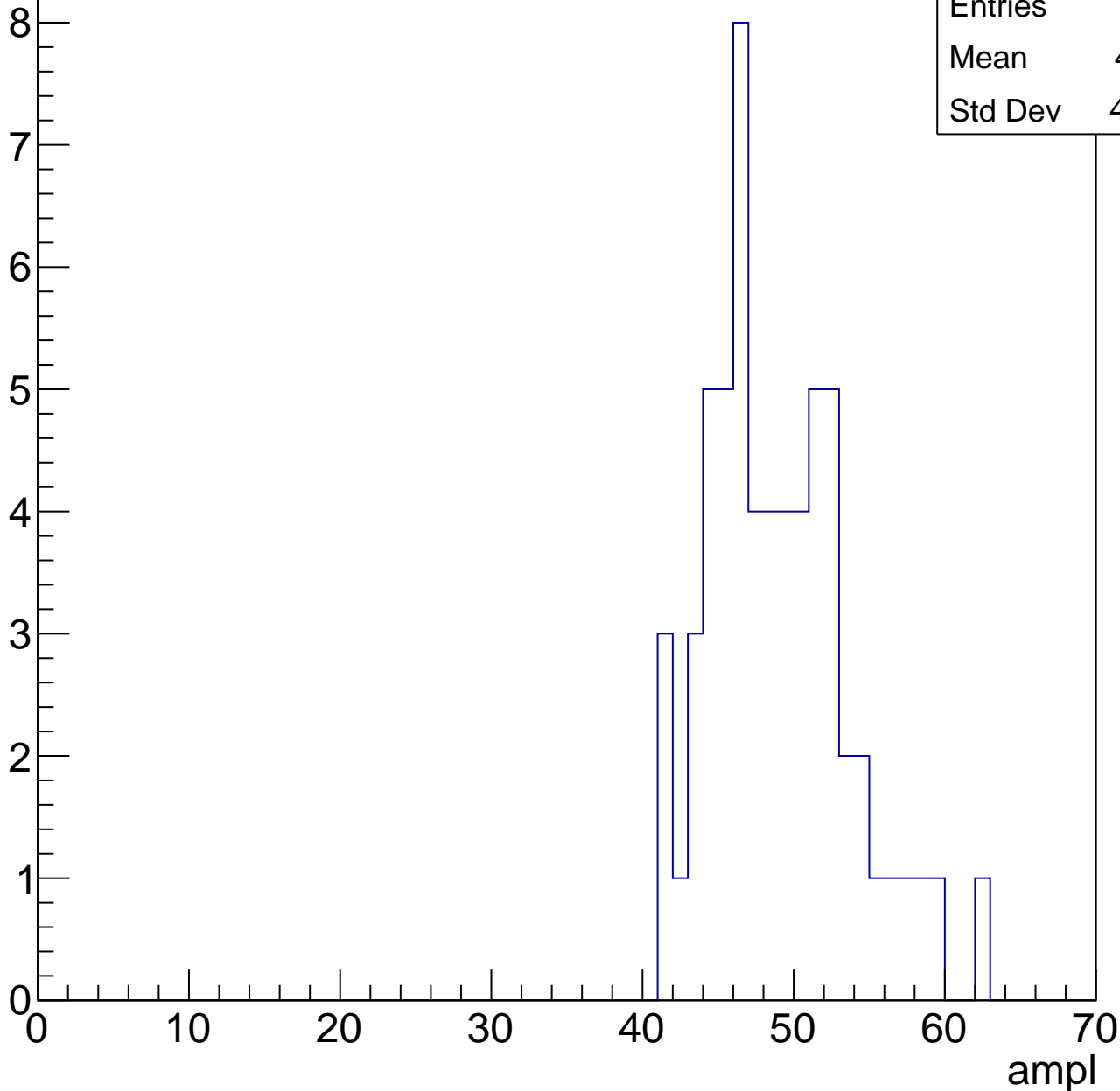


# B1L103S, U16-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	48.51
Std Dev	4.583

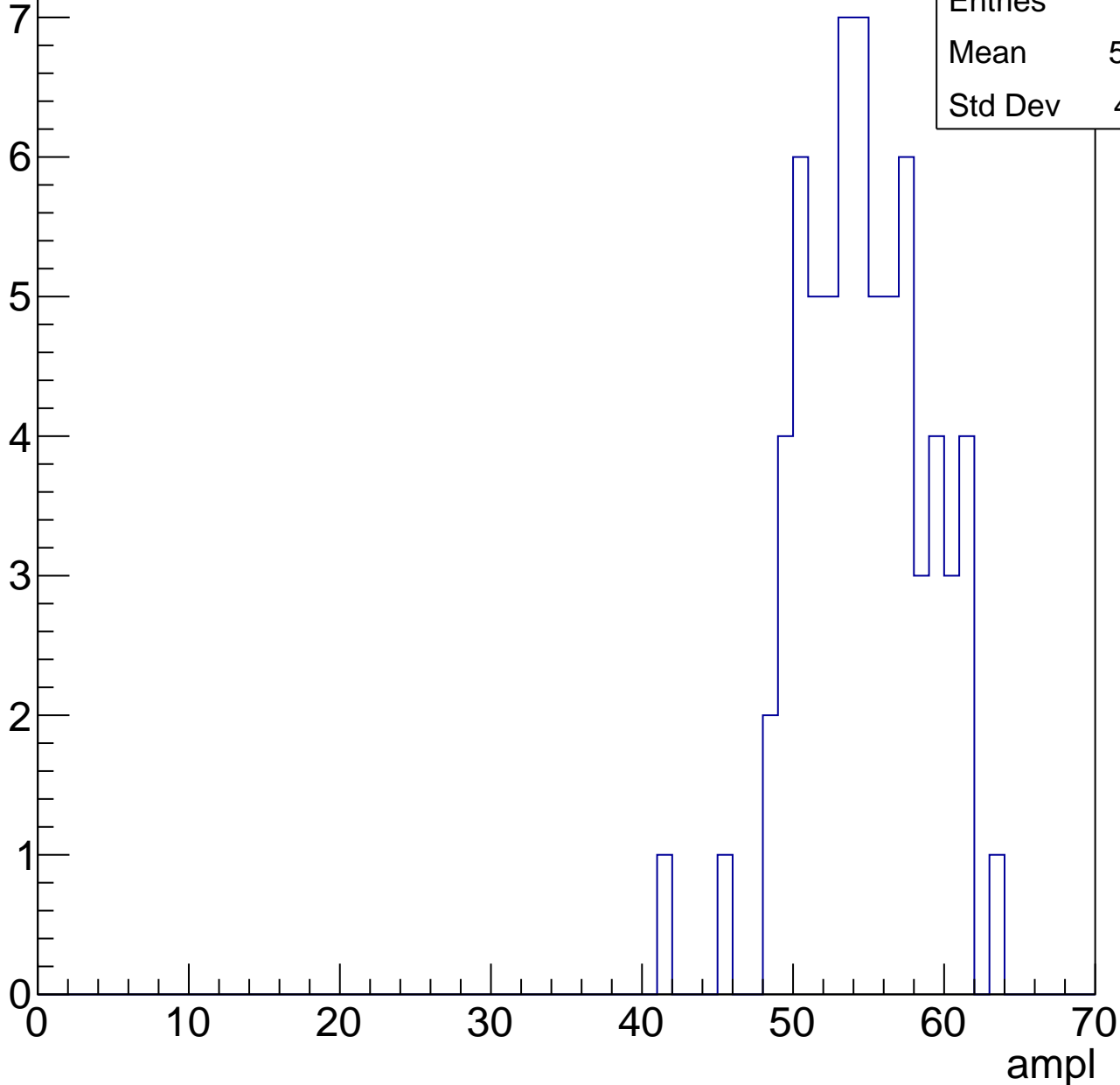


# B1L103S, U16-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

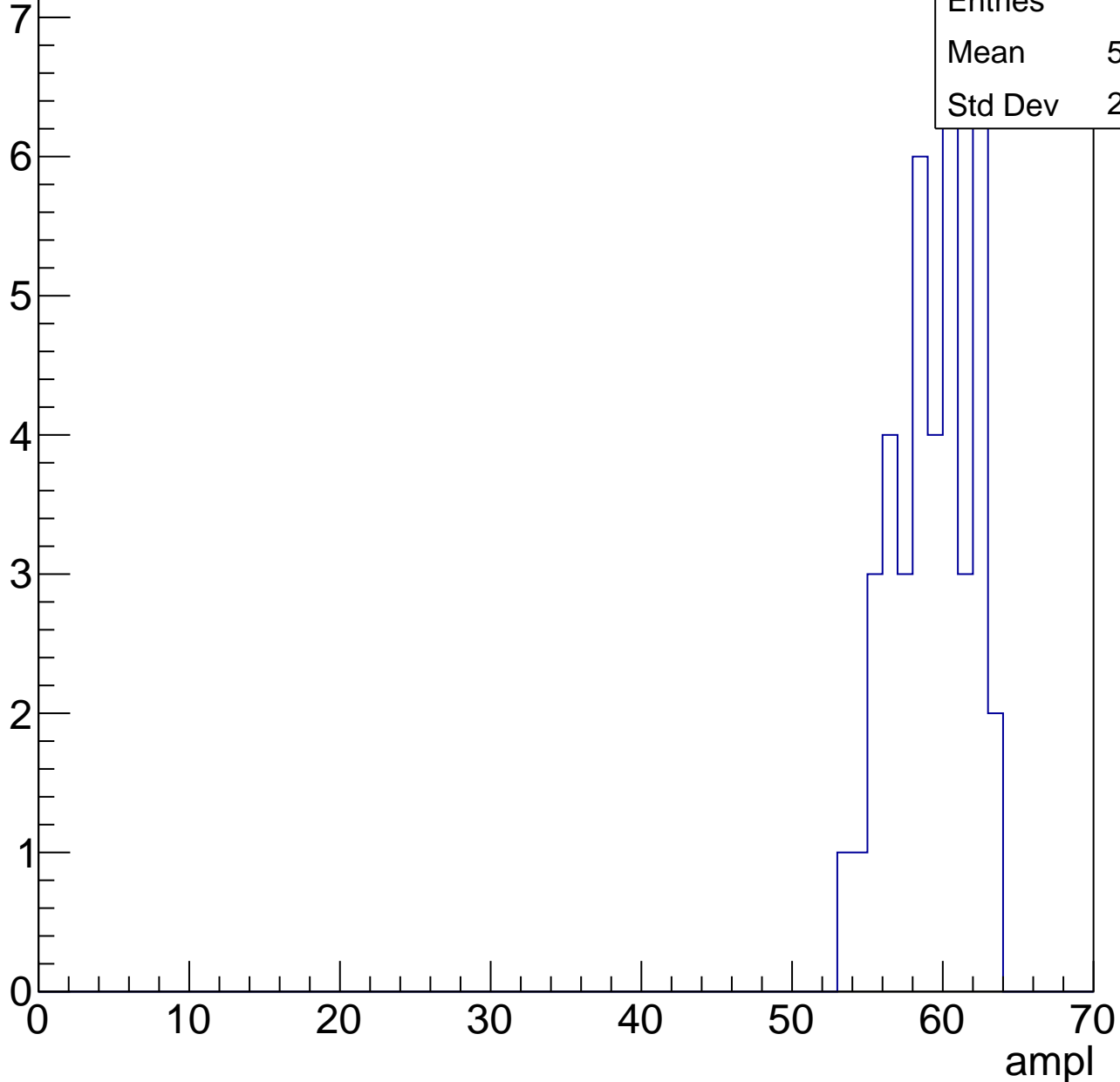
Entries	69
Mean	54.14
Std Dev	4.171



# B1L103S, U16-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

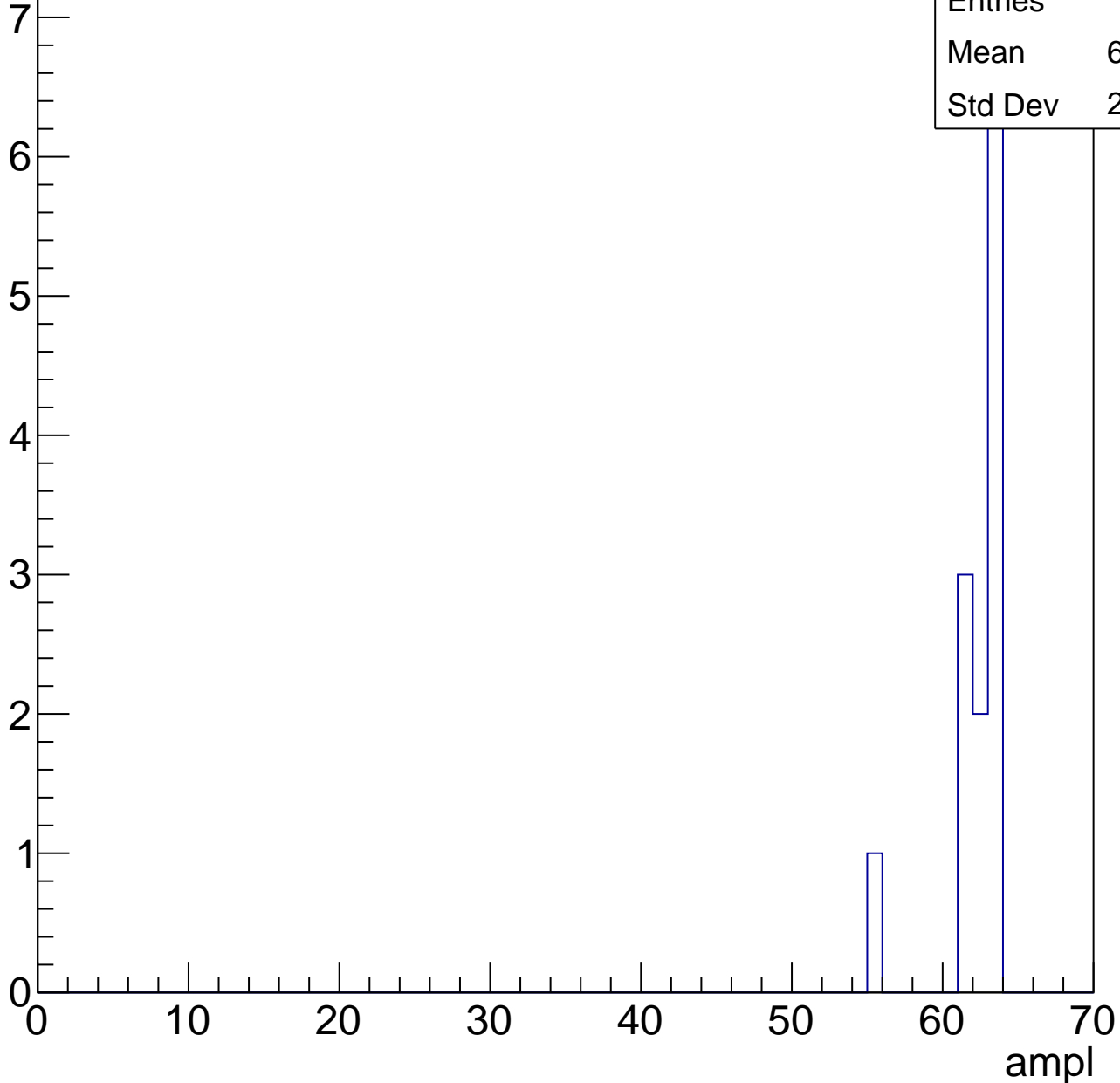


# B1L103S, U16-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	13
Mean	61.77
Std Dev	2.118

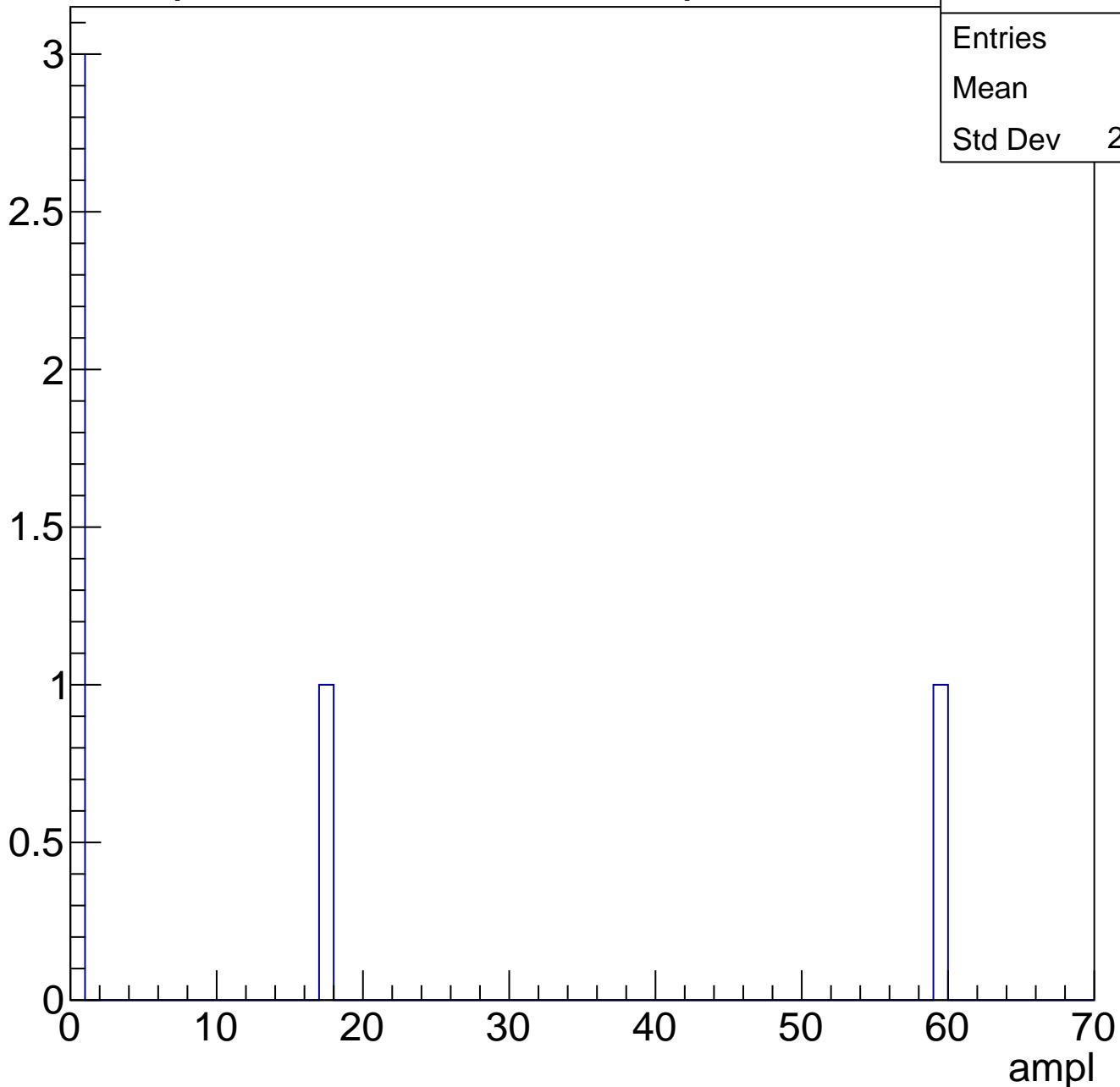




# B1L103S, U16-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	5
Mean	15.2
Std Dev	22.87

# B1L103S, U16-ch125, adc0

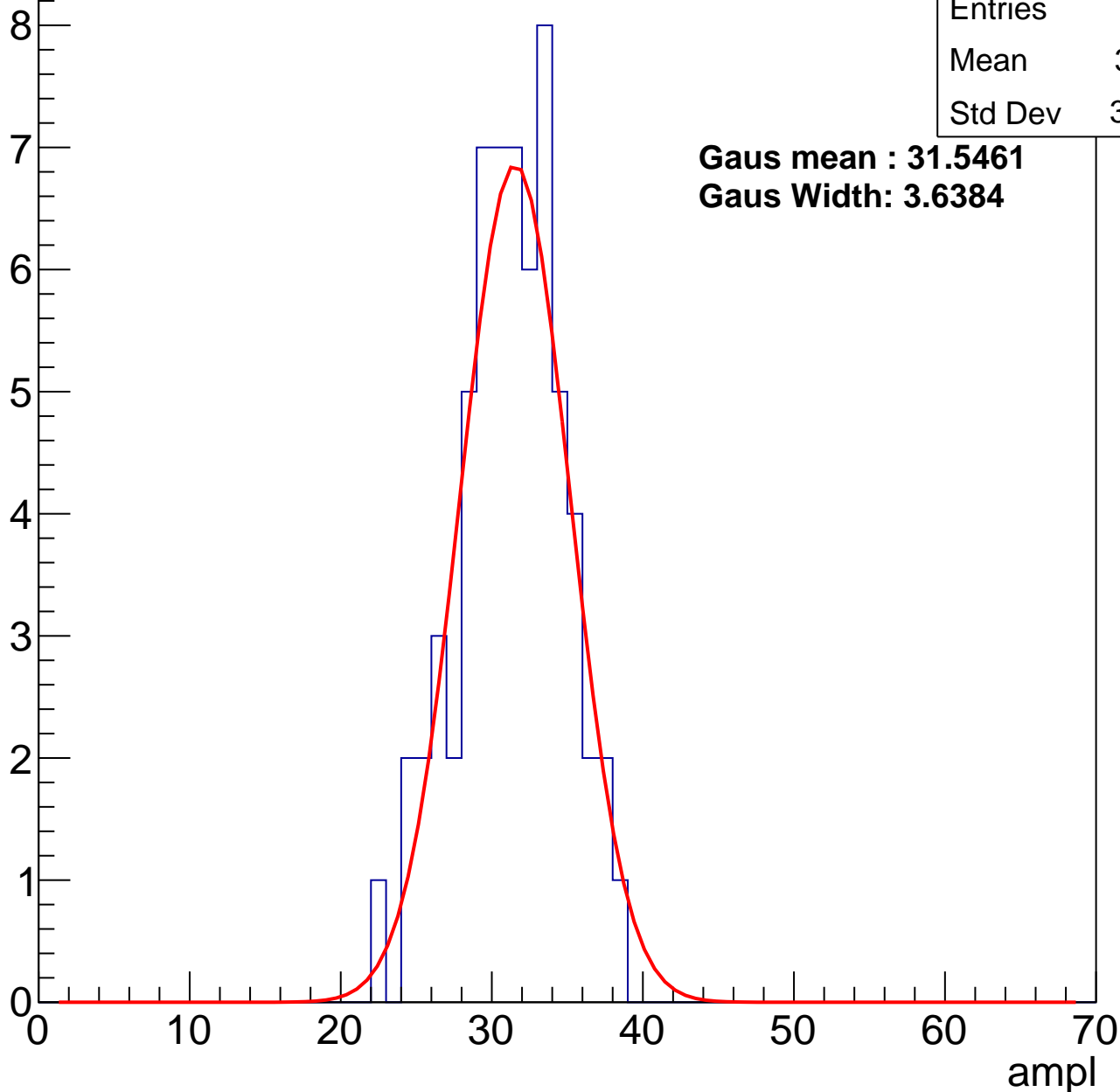
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	30.81
Std Dev	3.432

**Gaus mean : 31.5461**

**Gaus Width: 3.6384**



# B1L103S, U16-ch125, adc1

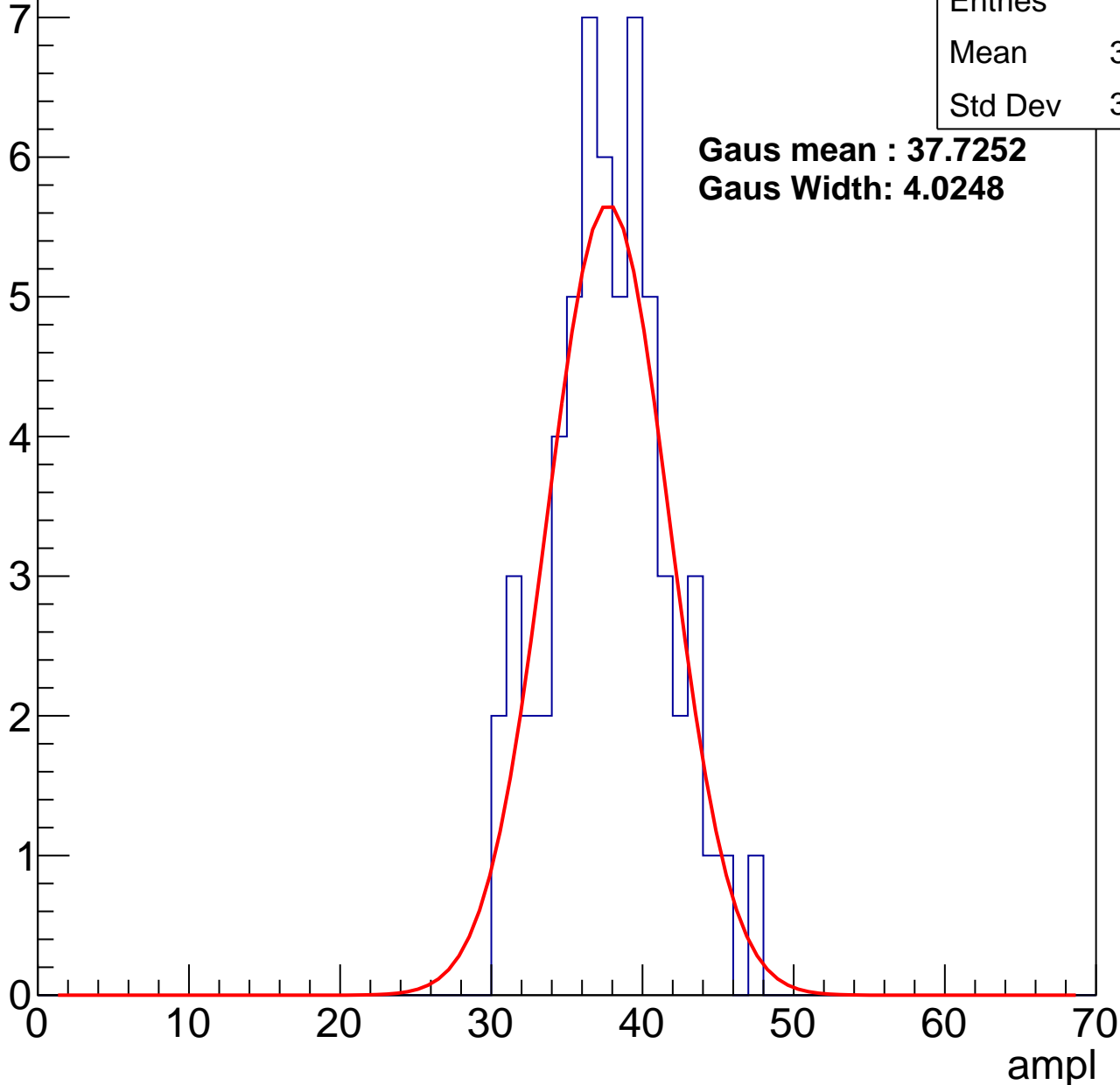
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	37.34
Std Dev	3.776

**Gaus mean : 37.7252**

**Gaus Width: 4.0248**



# B1L103S, U16-ch125, adc2

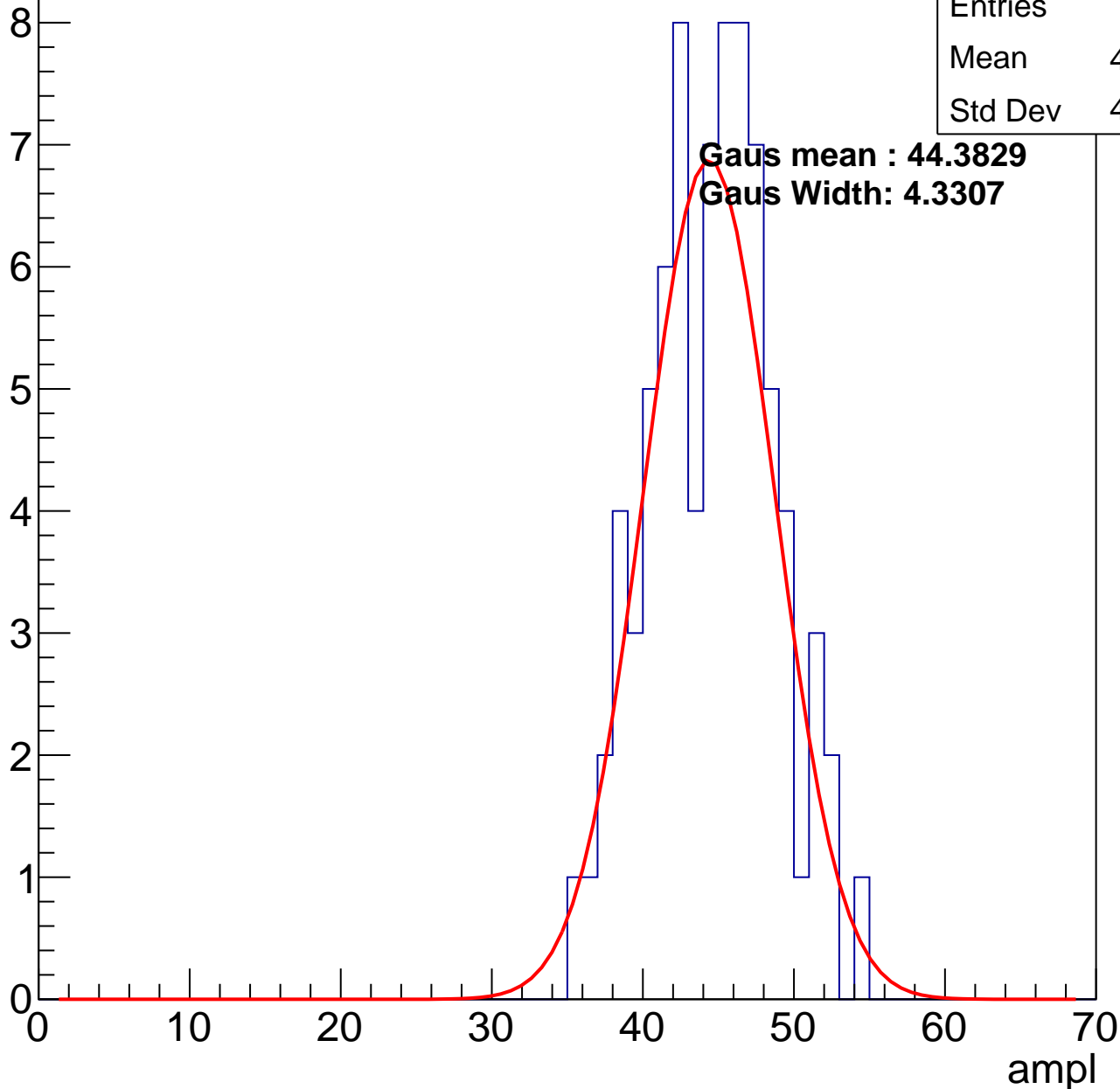
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	44.12
Std Dev	4.069

**Gaus mean : 44.3829**

**Gaus Width: 4.3307**

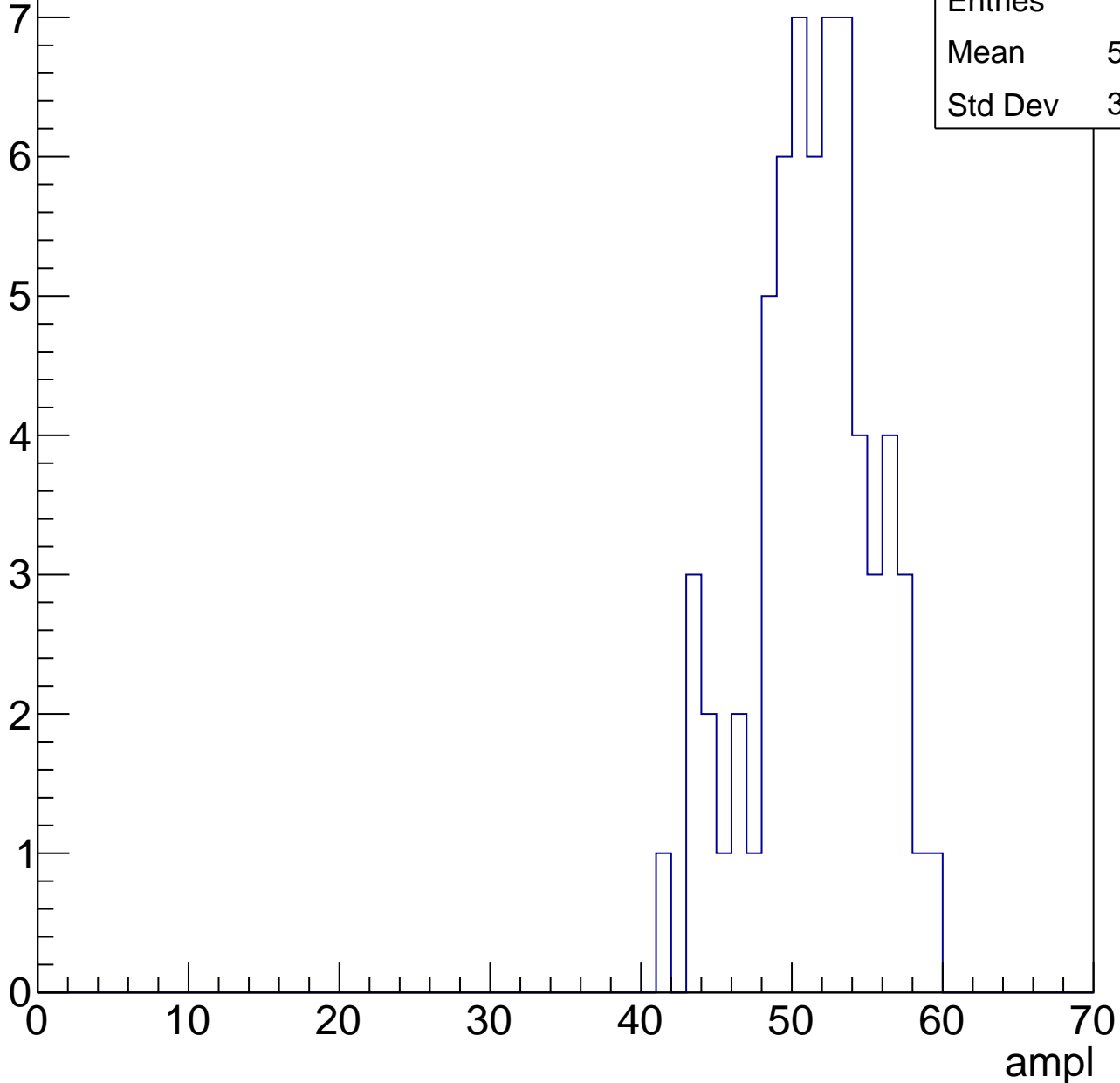


# B1L103S, U16-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	50.94
Std Dev	3.968

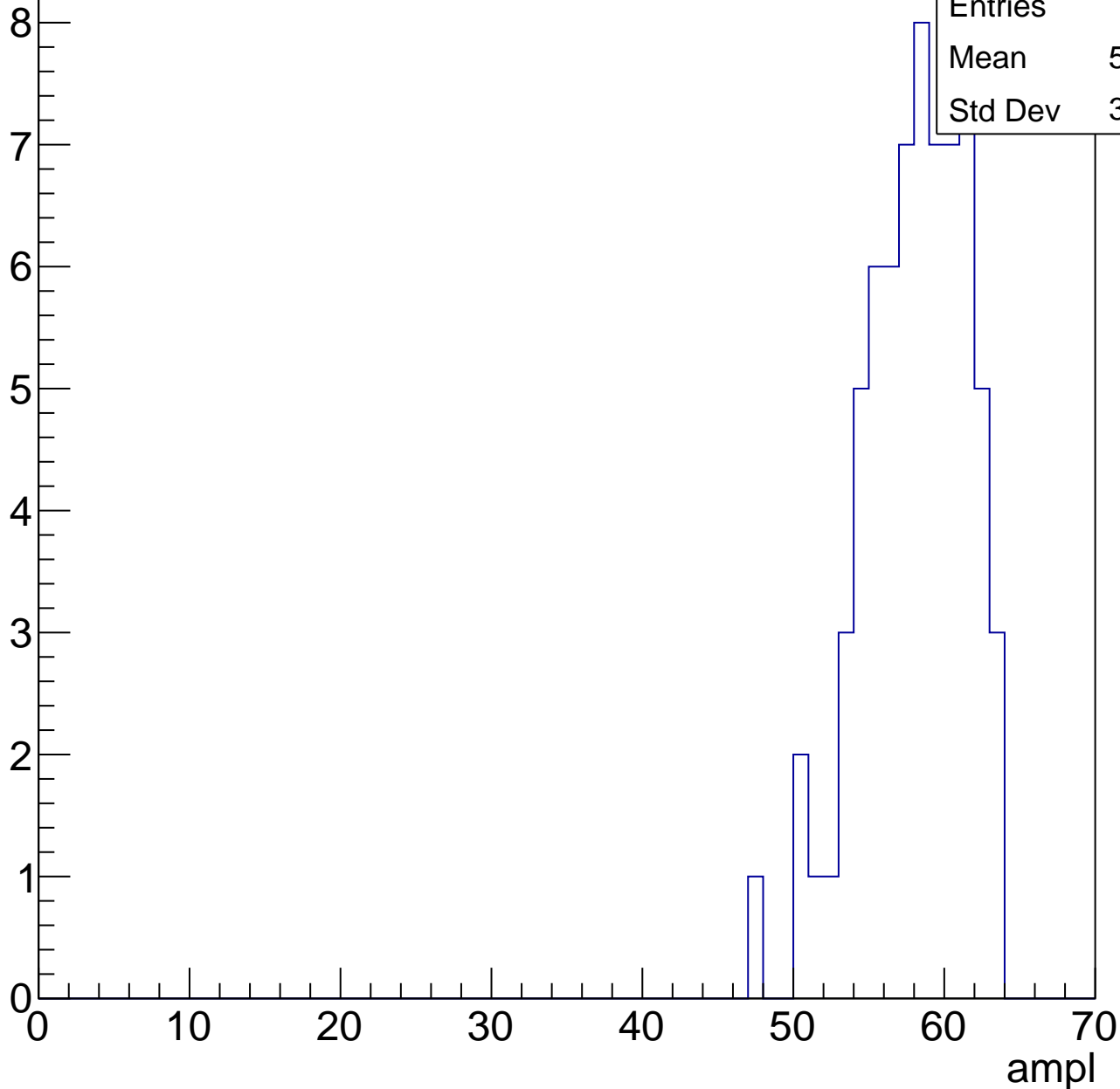


# B1L103S, U16-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	57.54
Std Dev	3.425

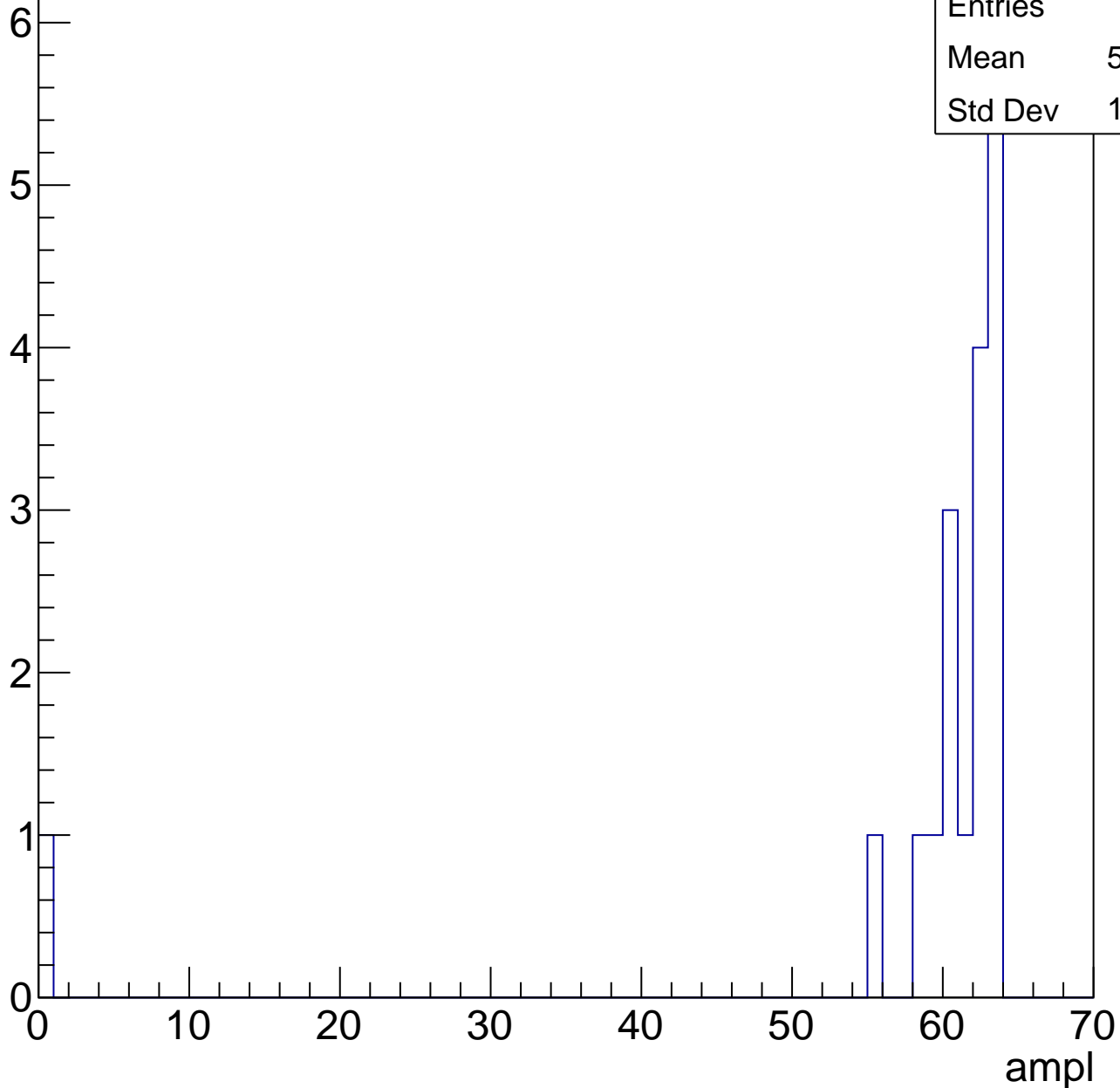


# B1L103S, U16-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

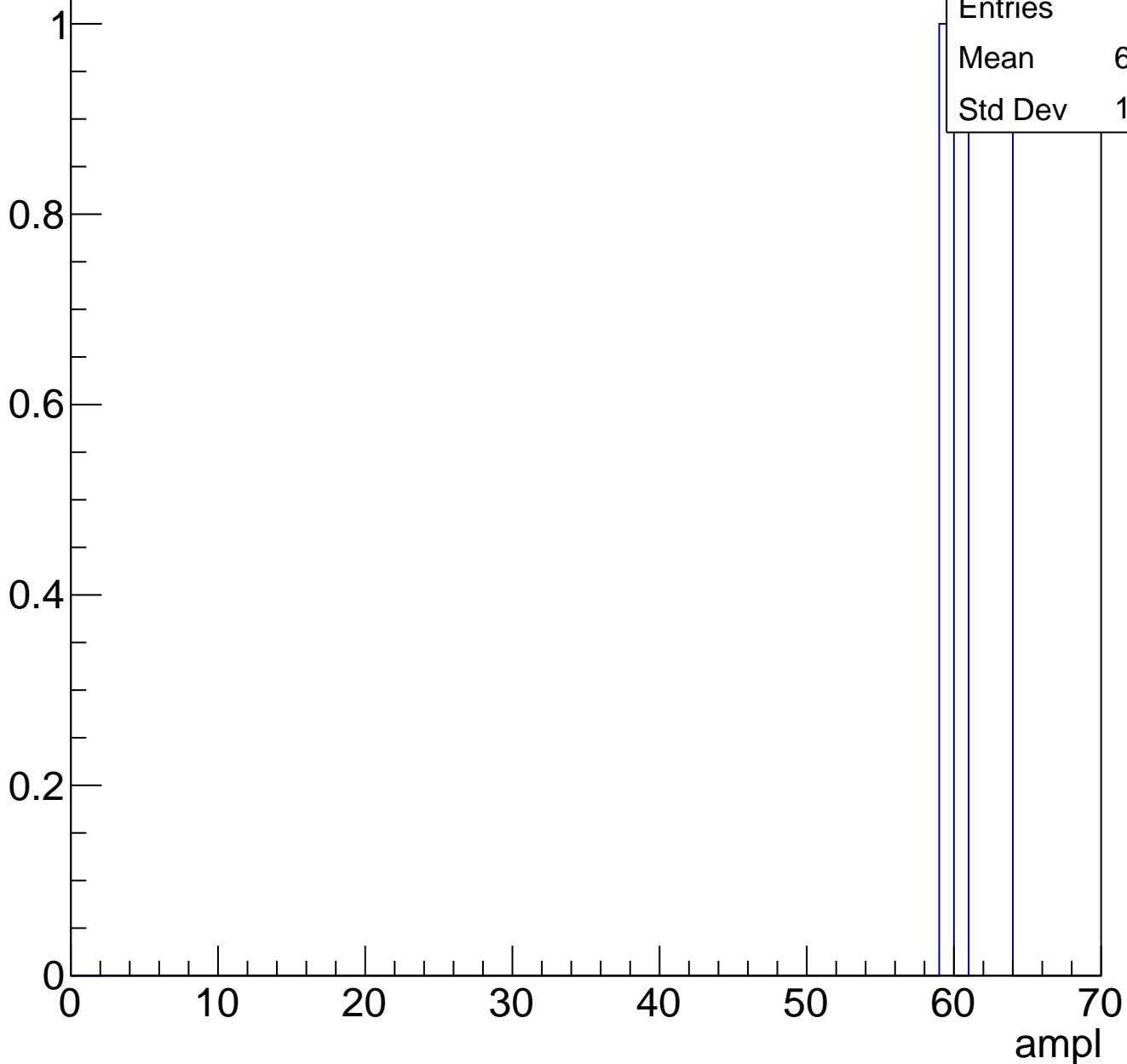
Entries	18
Mean	57.72
Std Dev	14.16



# B1L103S, U16-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U16-ch126, adc0

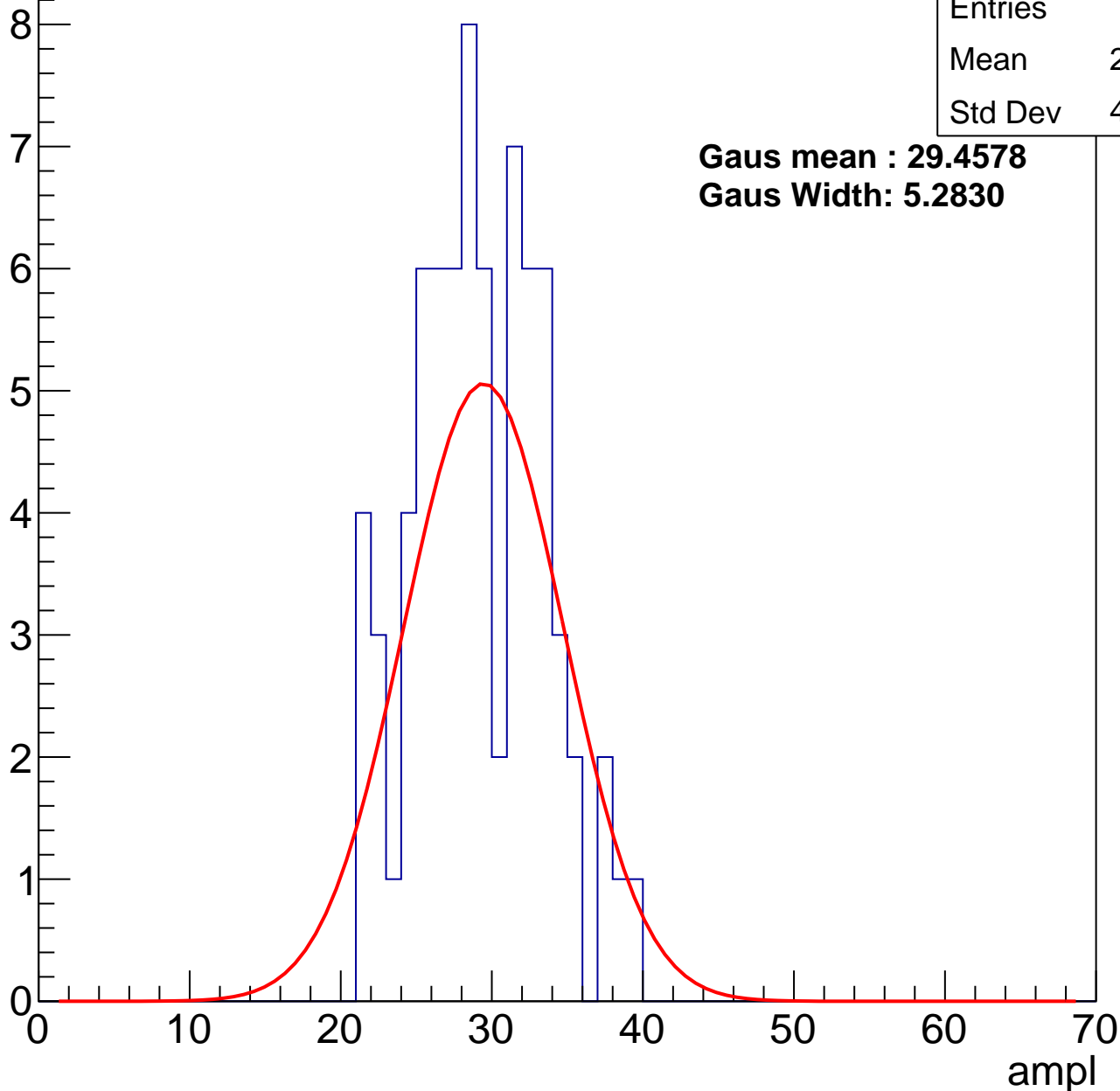
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	28.72
Std Dev	4.273

**Gaus mean : 29.4578**

**Gaus Width: 5.2830**



# B1L103S, U16-ch126, adc1

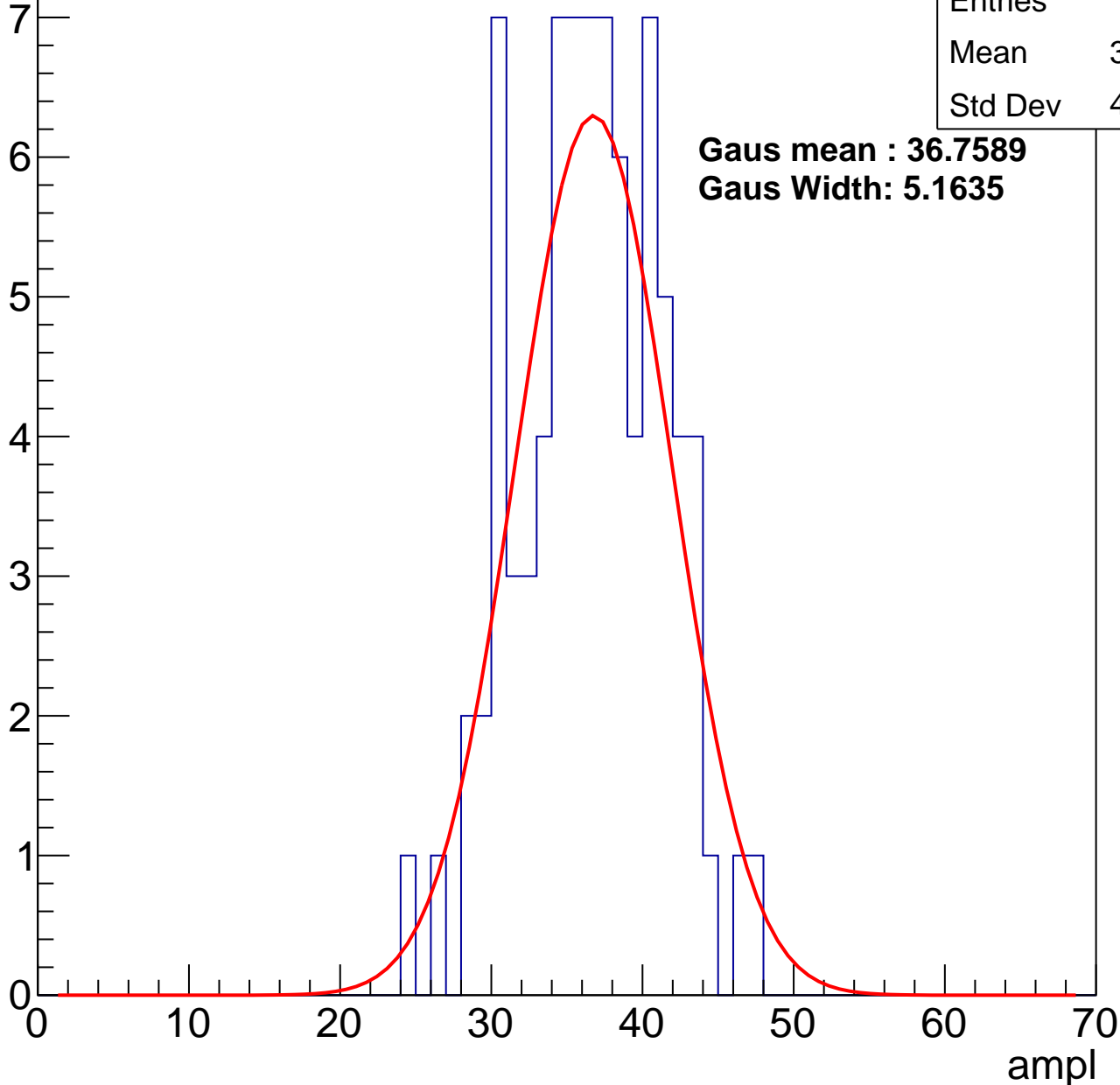
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	84
Mean	36.13
Std Dev	4.685

**Gaus mean : 36.7589**

**Gaus Width: 5.1635**



# B1L103S, U16-ch126, adc2

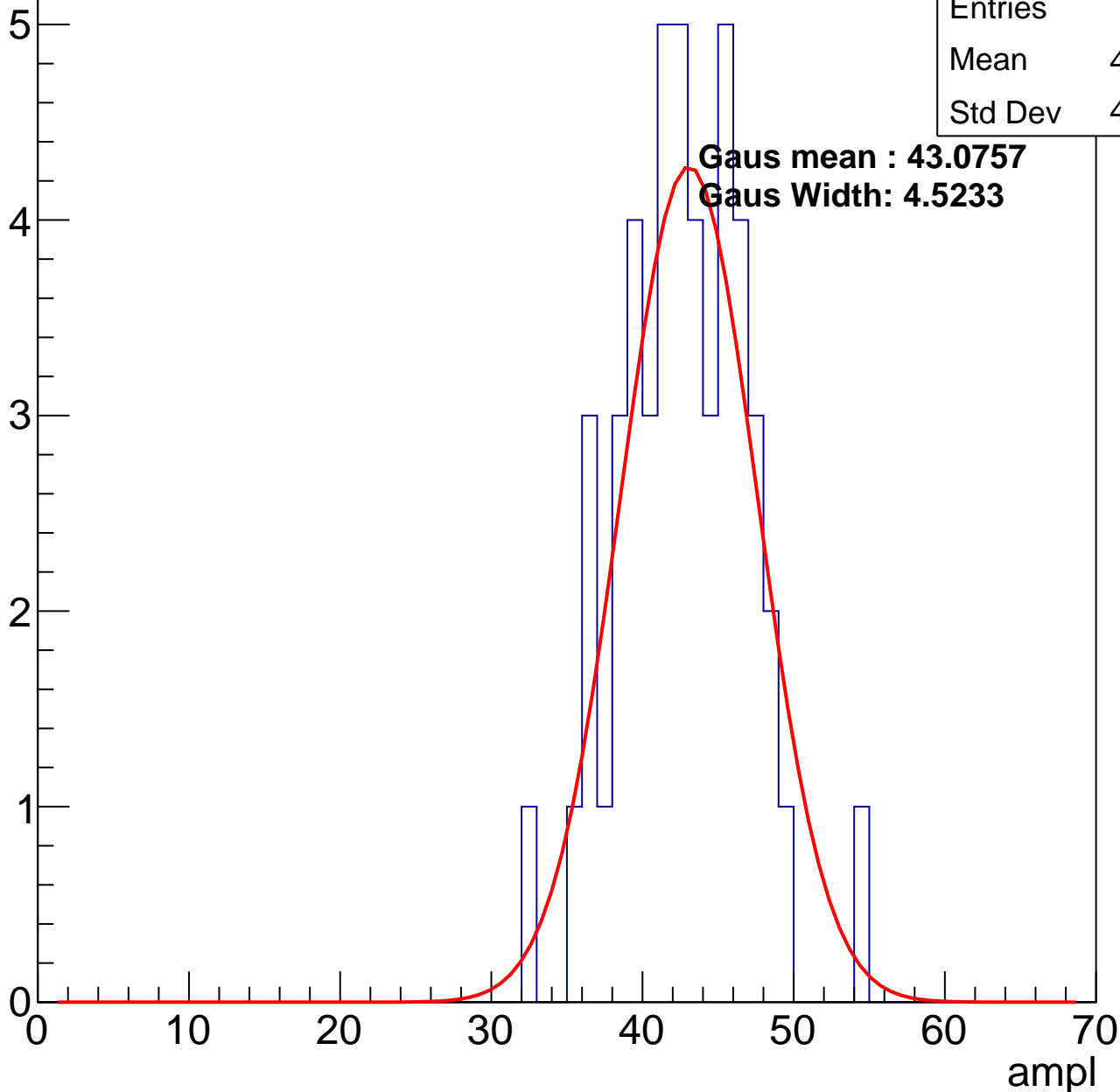
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	42.24
Std Dev	4.153

**Gaus mean : 43.0757**

**Gaus Width: 4.5233**

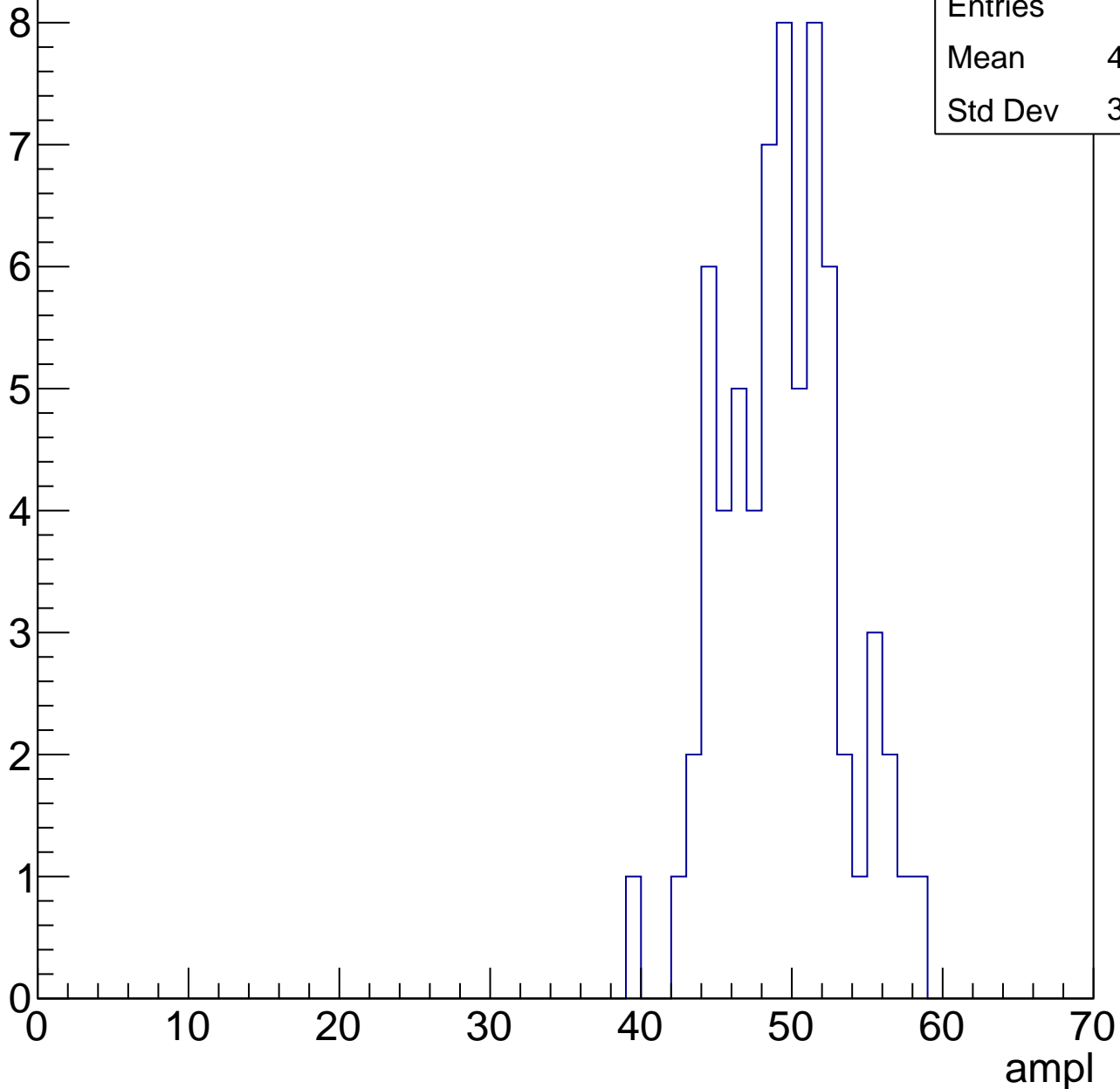


# B1L103S, U16-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	48.94
Std Dev	3.867

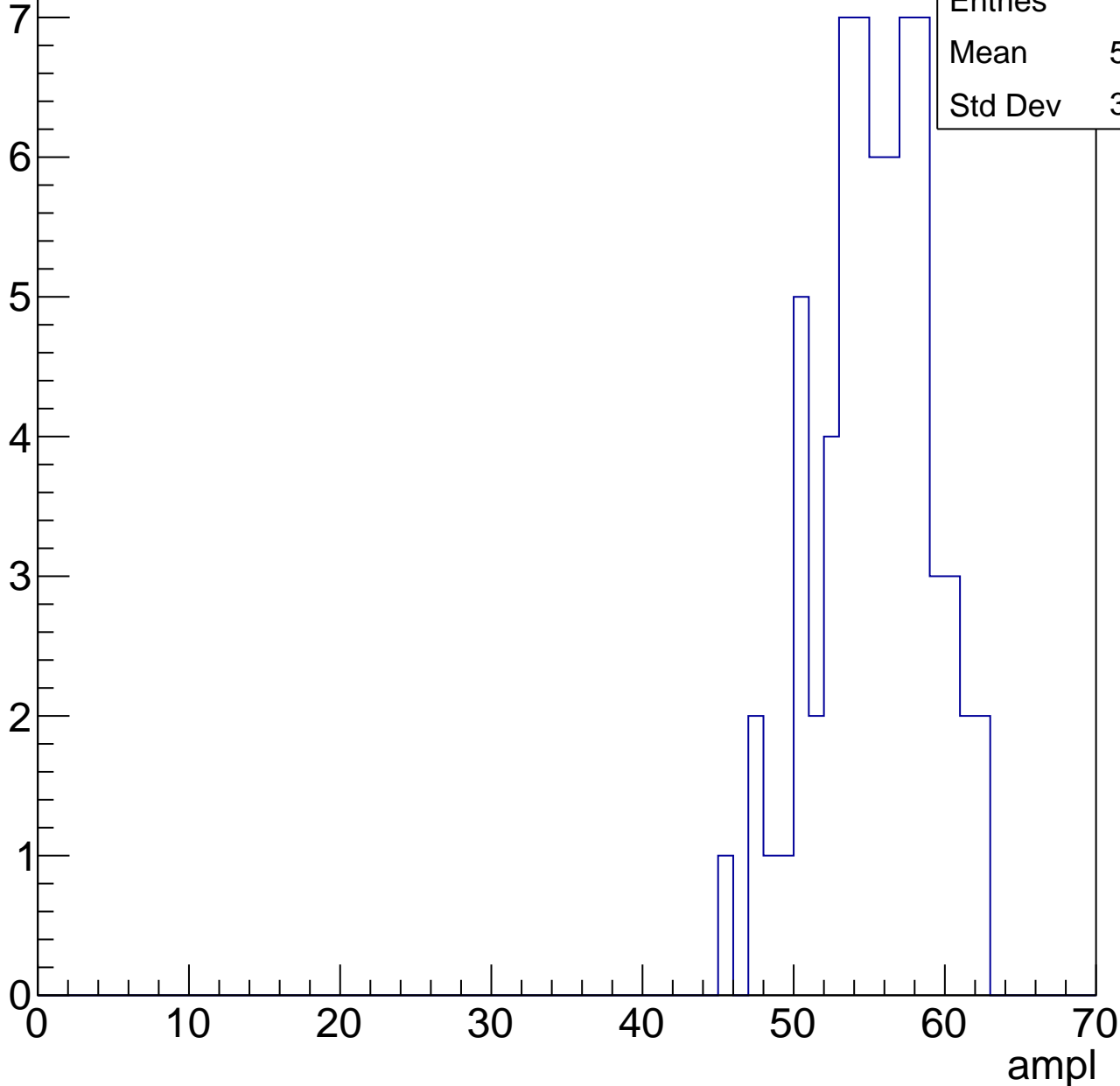


# B1L103S, U16-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	54.83
Std Dev	3.752

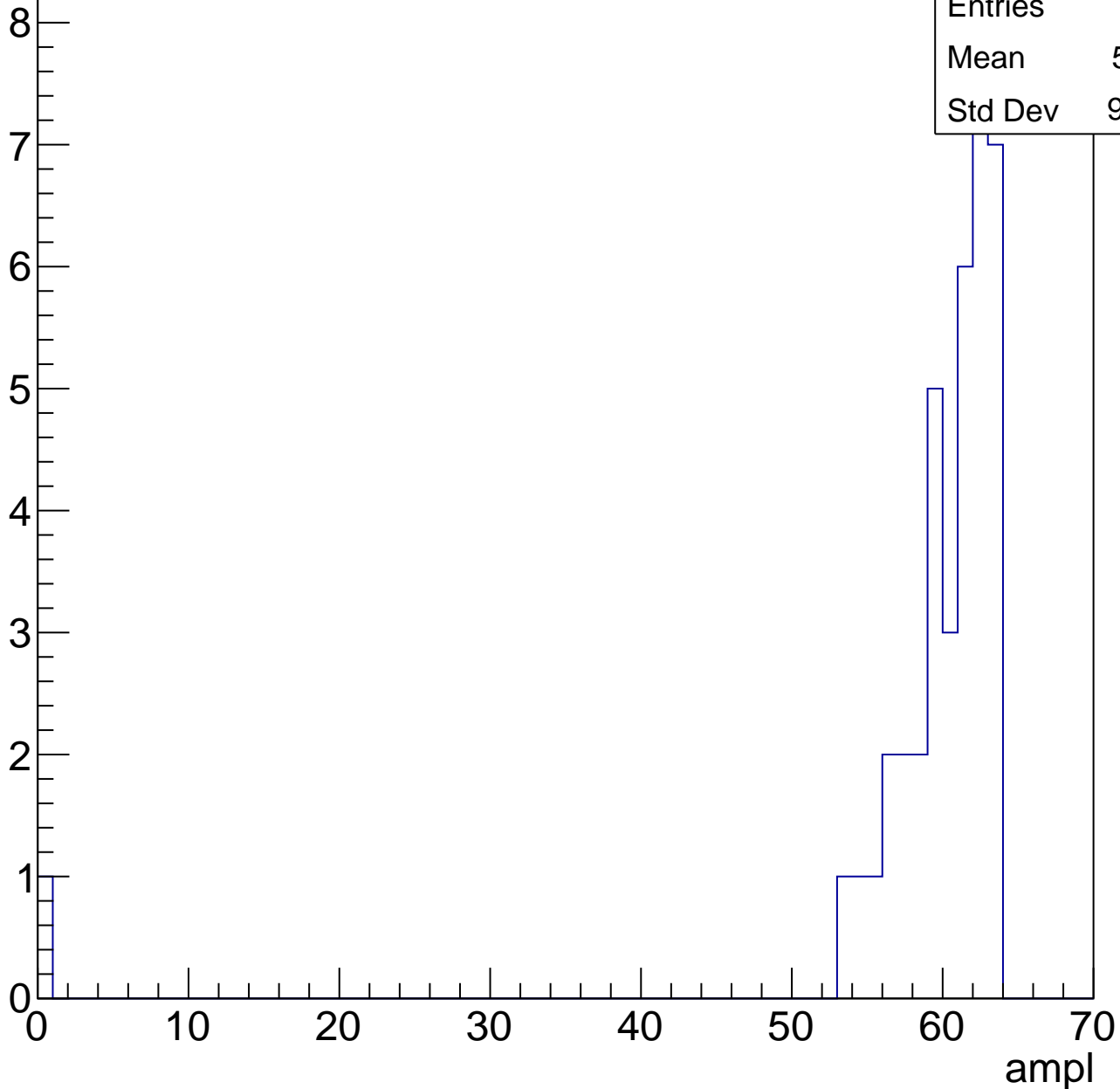


# B1L103S, U16-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

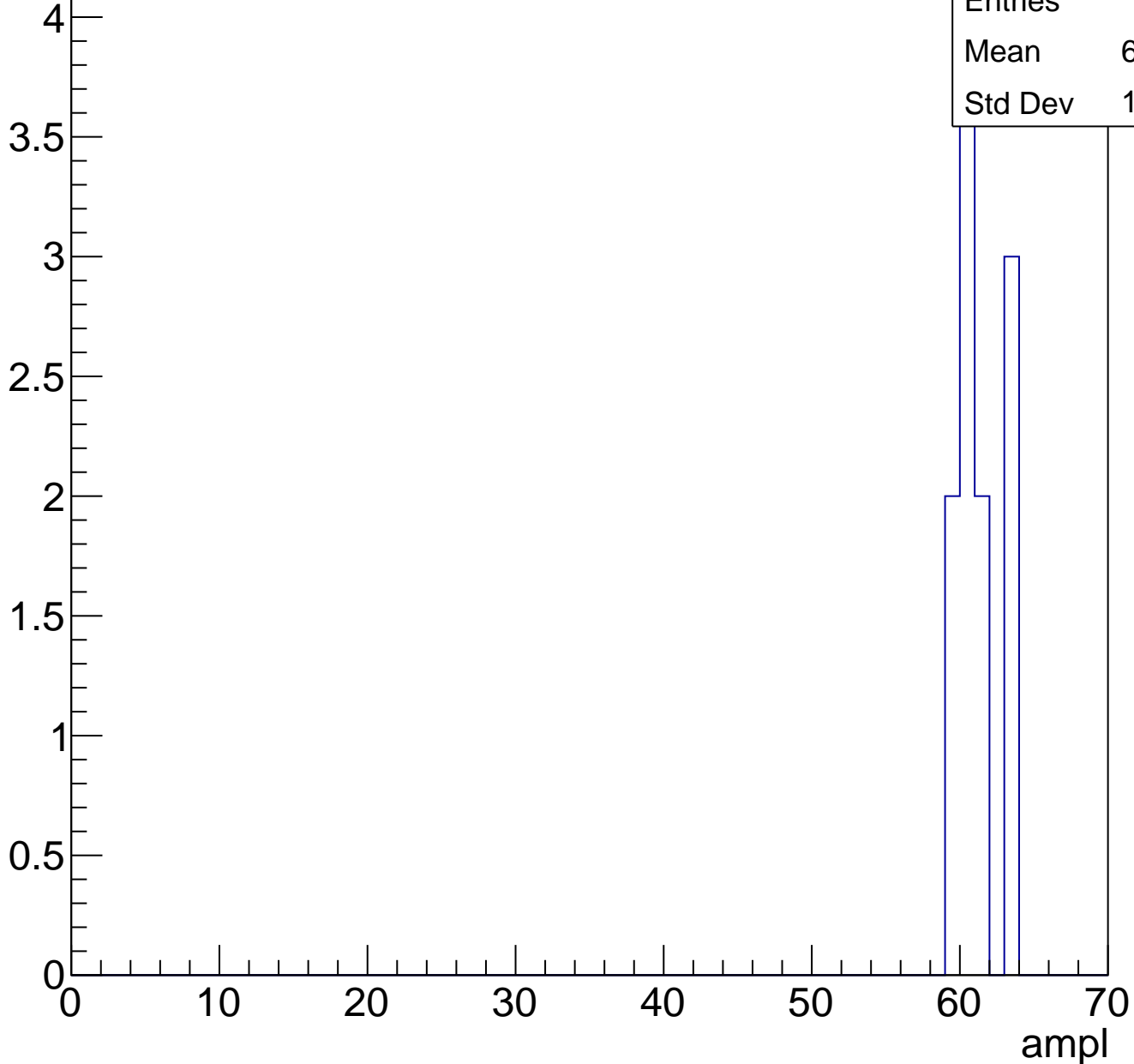
Entries	39
Mean	58.51
Std Dev	9.855



# B1L103S, U16-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

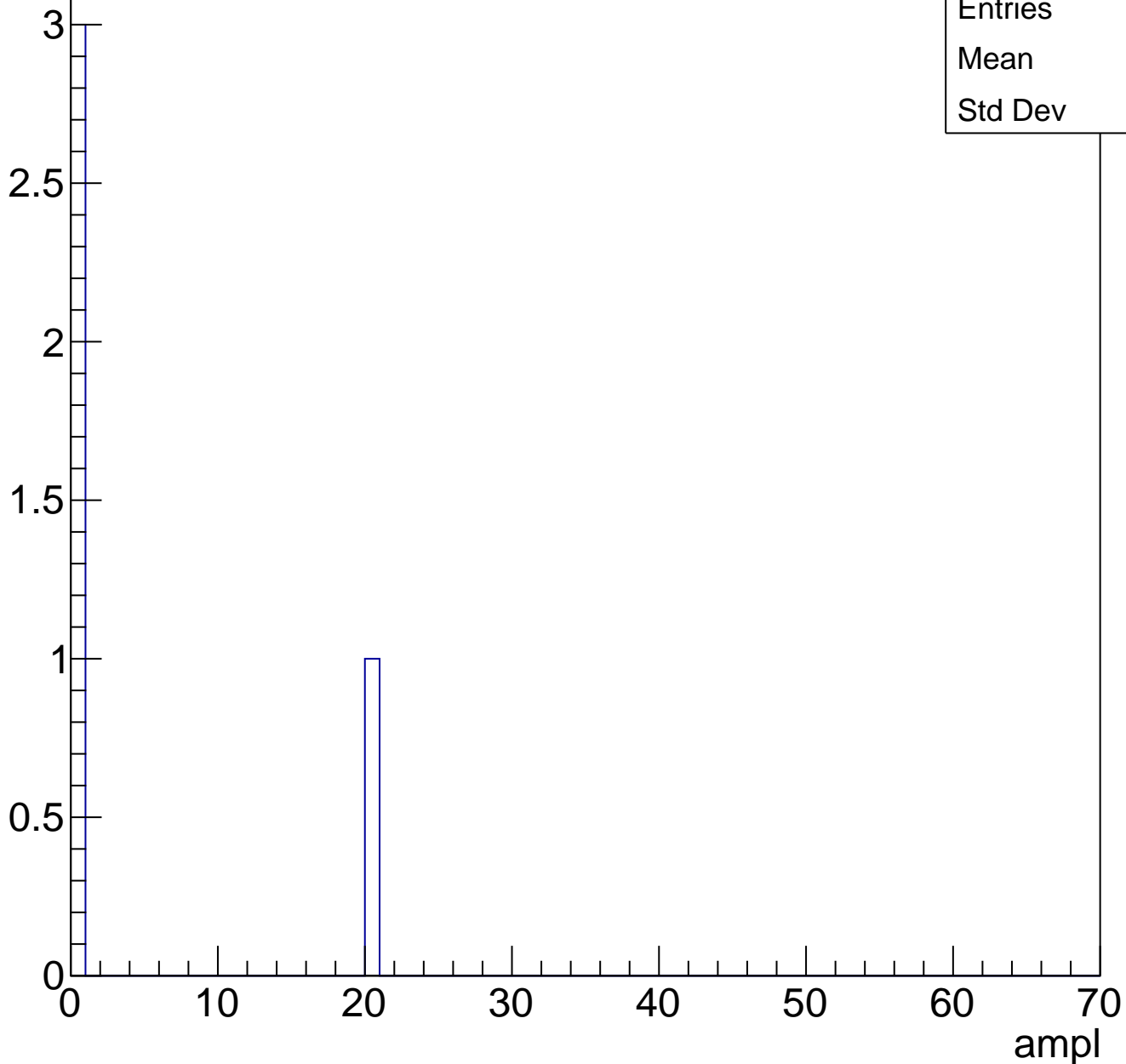




# B1L103S, U16-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	4
Mean	5
Std Dev	8.66

# B1L103S, U16-ch127, adc0

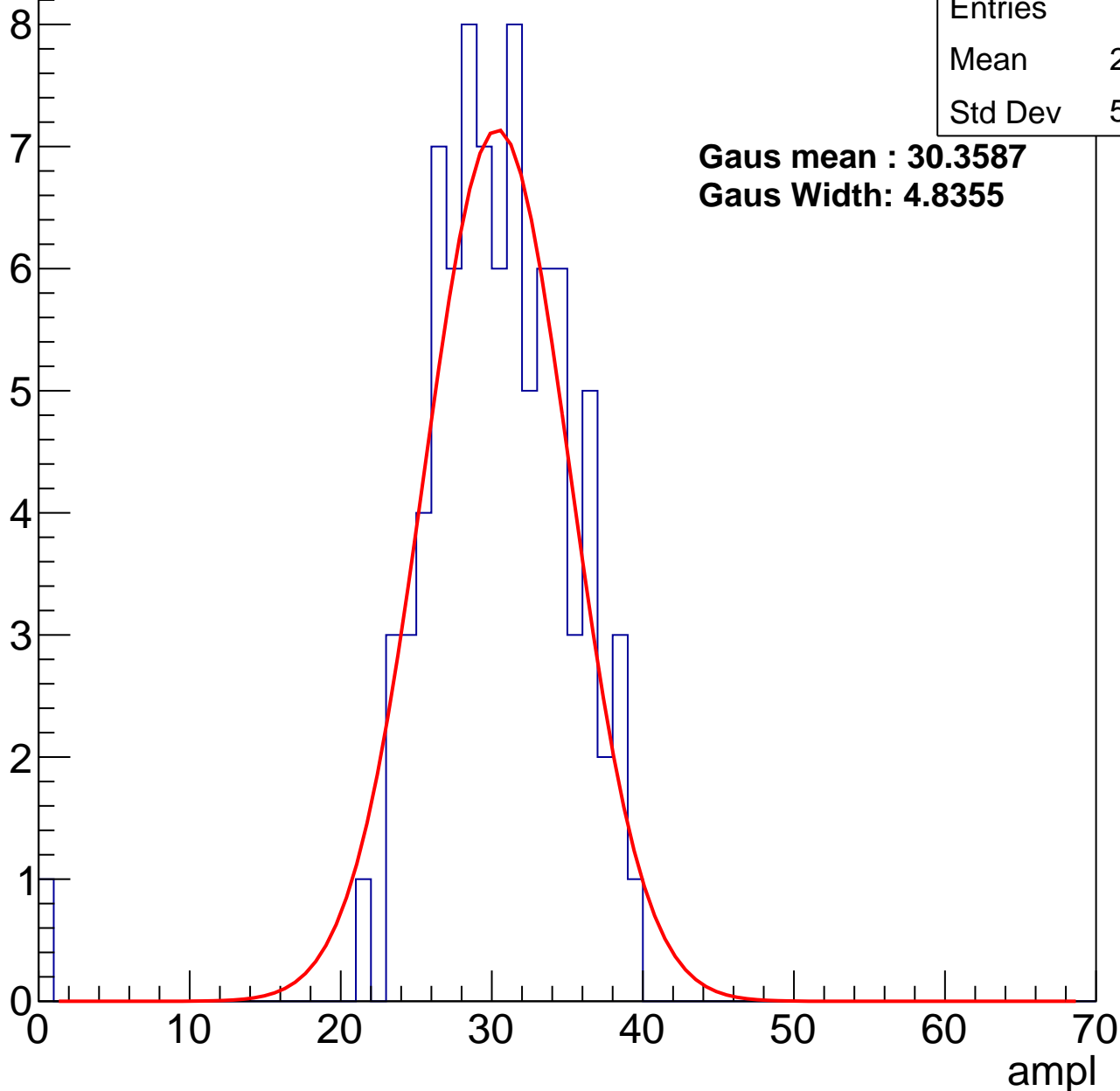
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	85
Mean	29.82
Std Dev	5.249

**Gaus mean : 30.3587**

**Gaus Width: 4.8355**



# B1L103S, U16-ch127, adc1

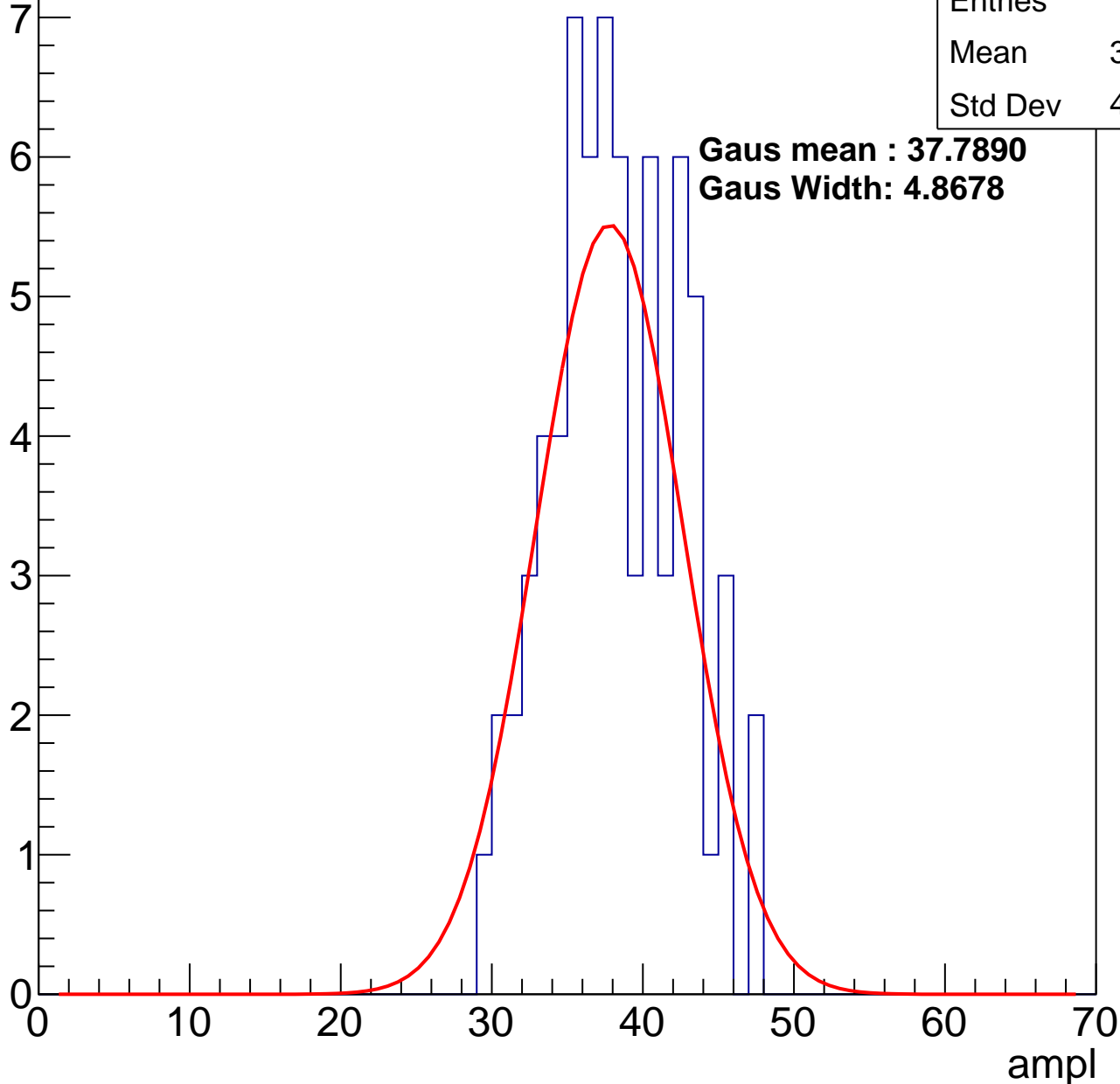
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	37.79
Std Dev	4.262

**Gaus mean : 37.7890**

**Gaus Width: 4.8678**



# B1L103S, U16-ch127, adc2

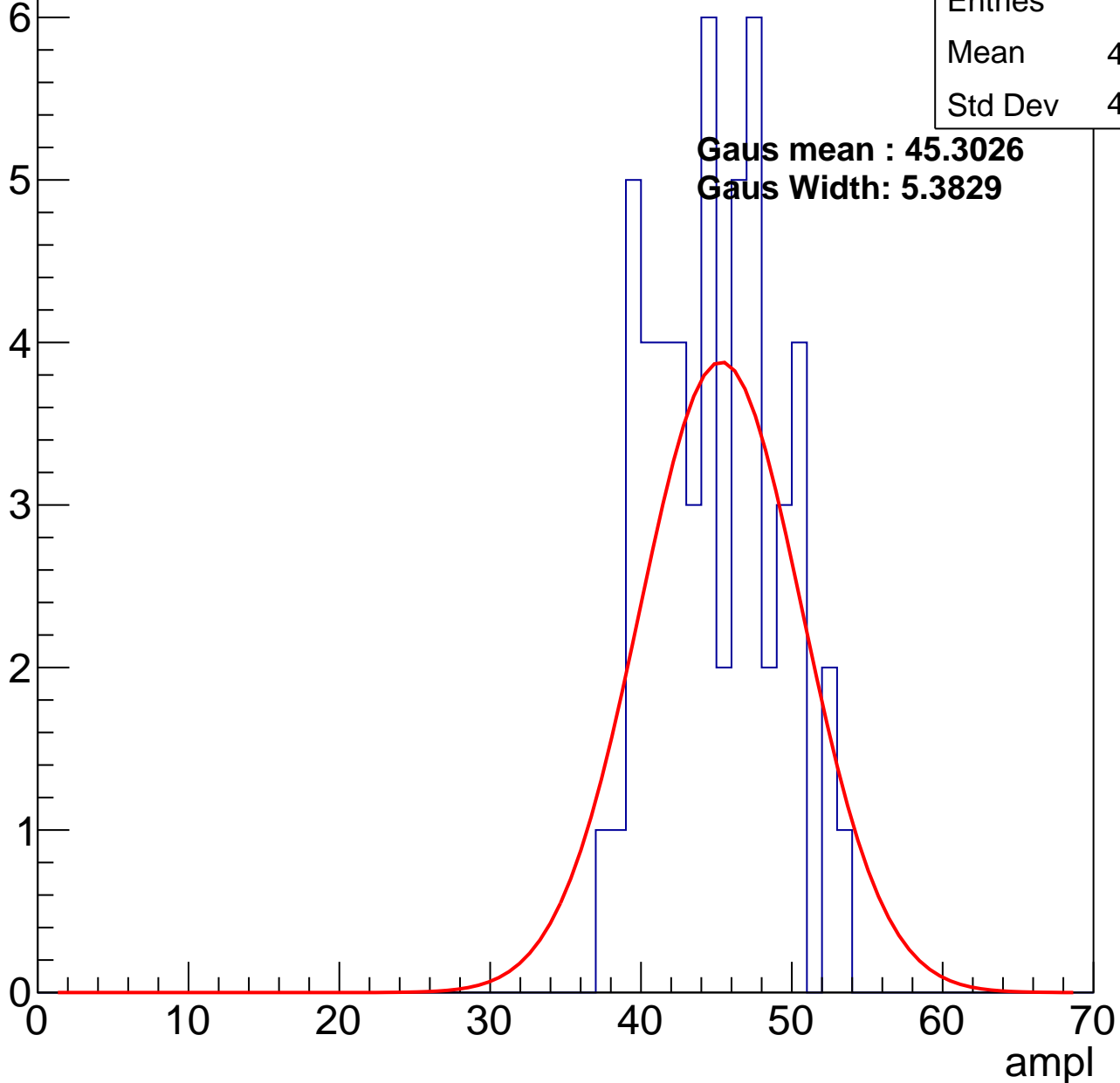
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	44.47
Std Dev	4.012

**Gaus mean : 45.3026**

**Gaus Width: 5.3829**

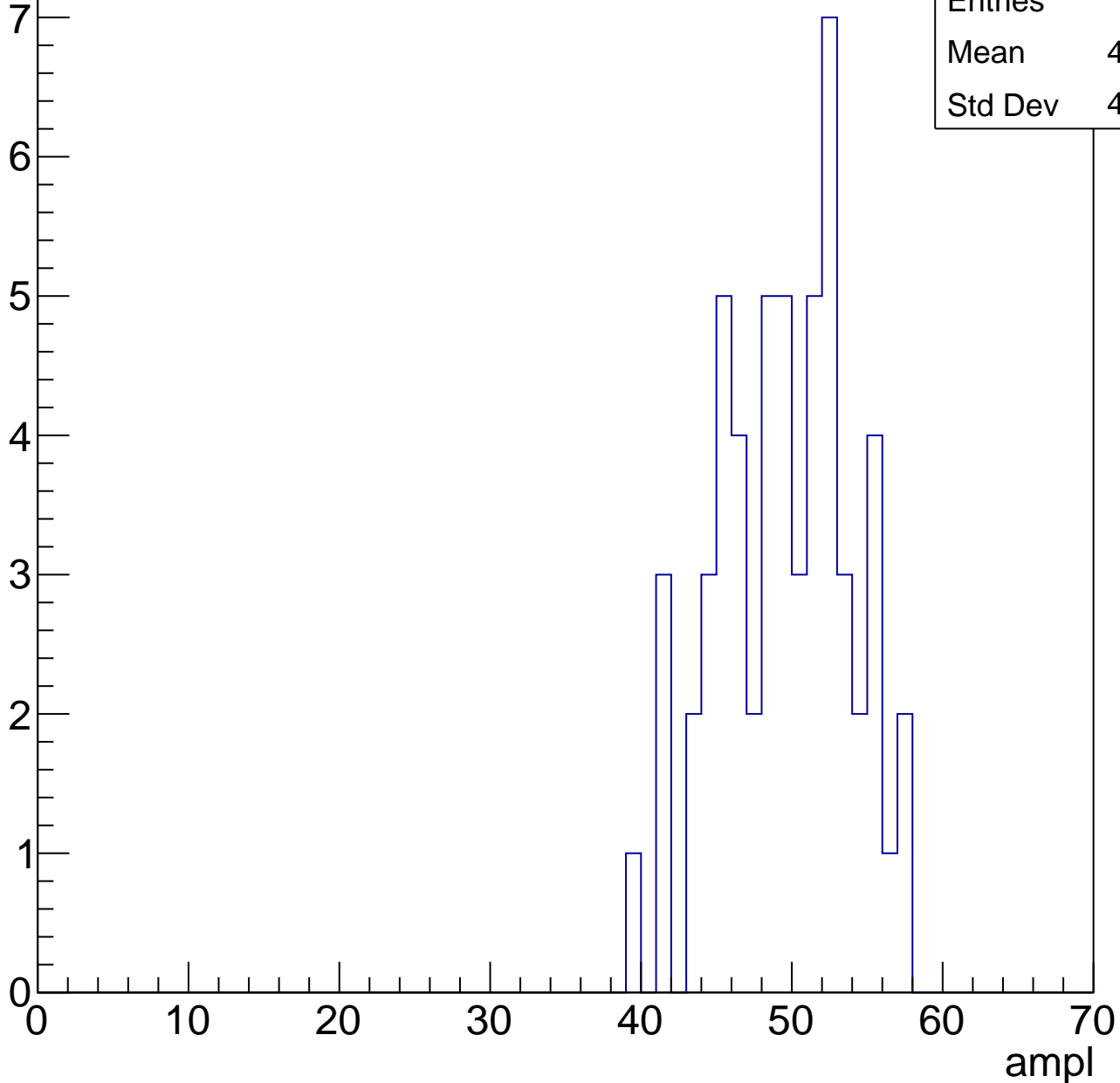


# B1L103S, U16-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	49.02
Std Dev	4.339

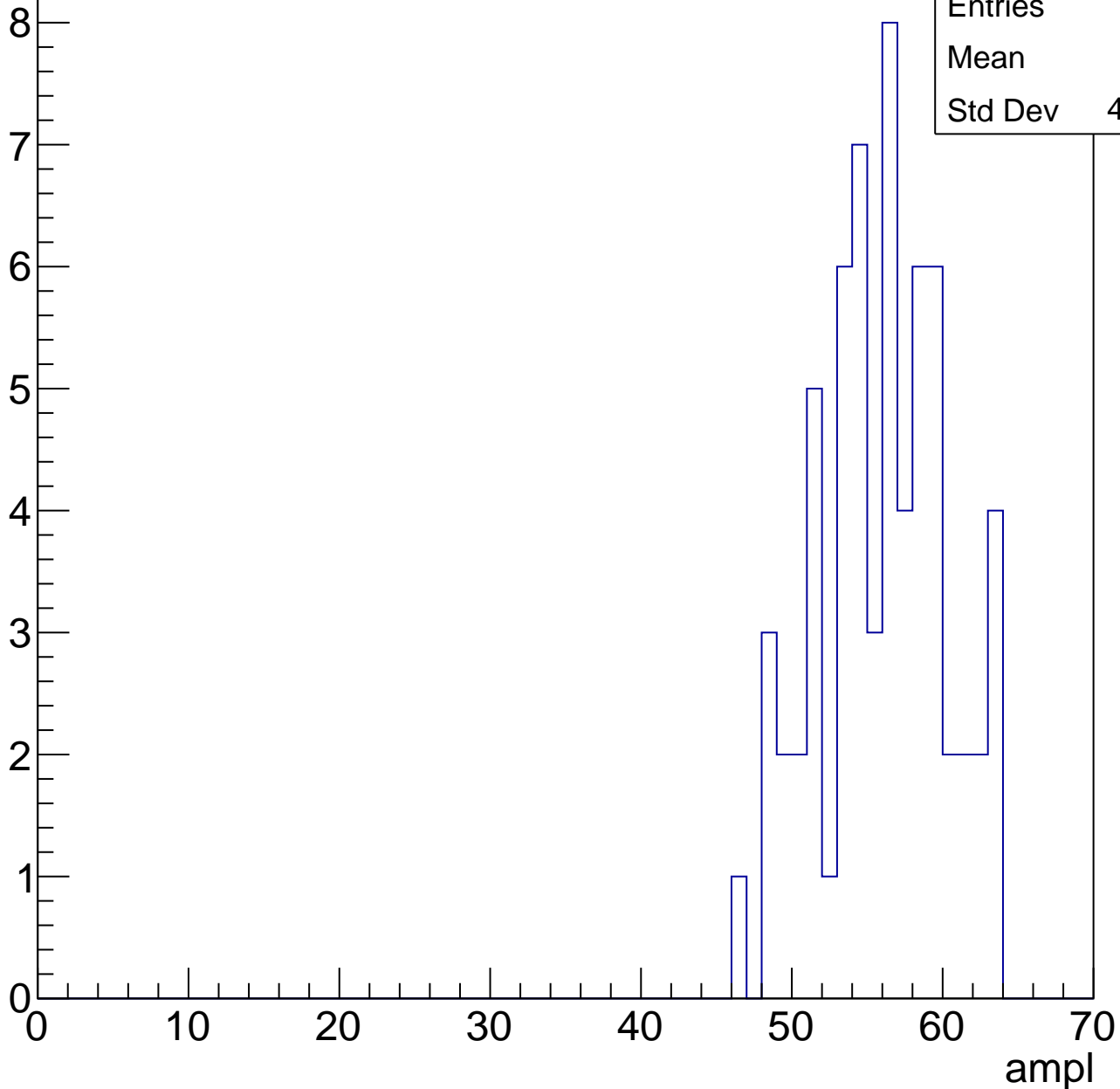


# B1L103S, U16-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	55.5
Std Dev	4.153

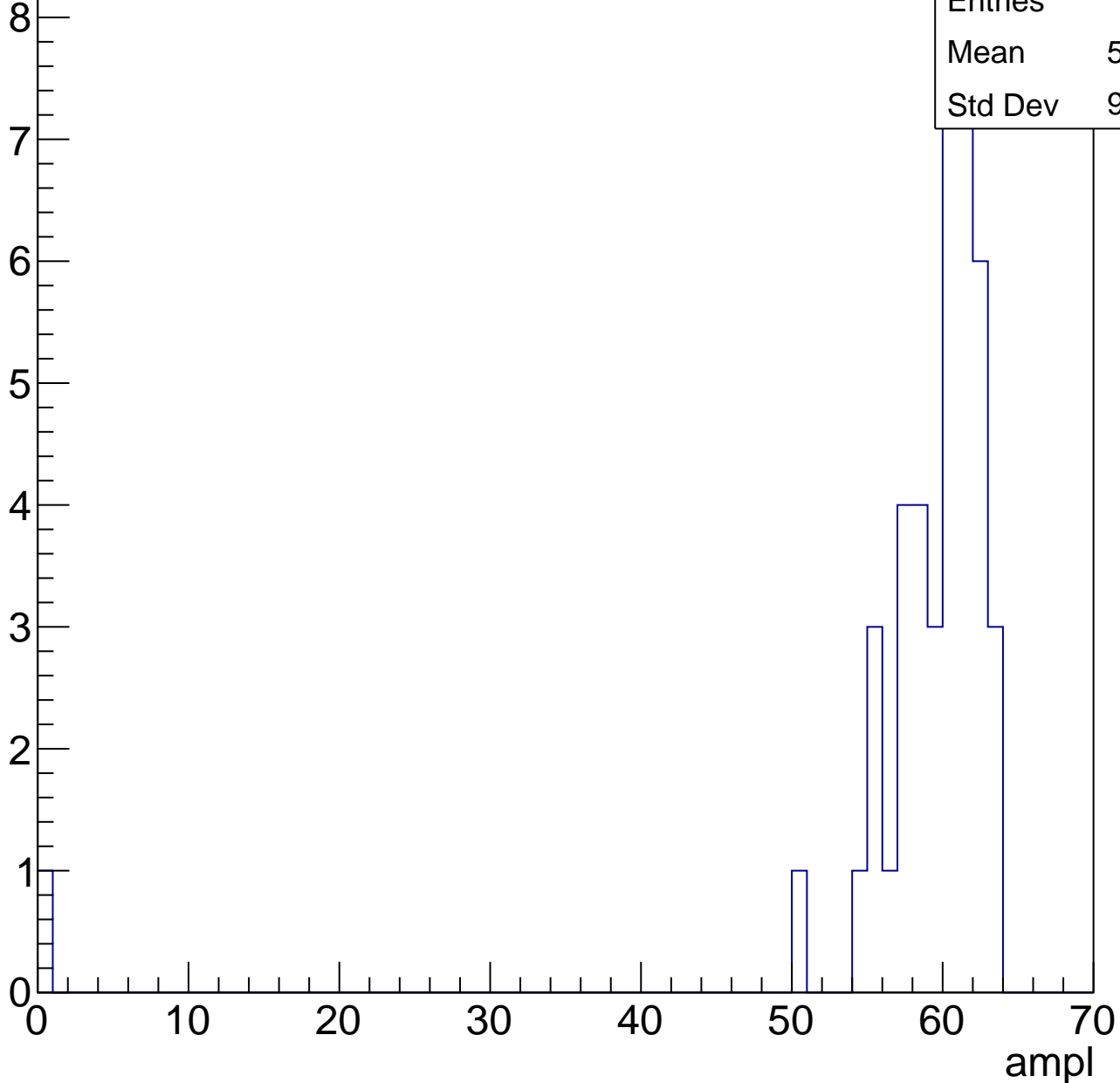


# B1L103S, U16-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	43
Mean	57.93
Std Dev	9.347



# B1L103S, U16-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U16-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U16-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0