



# B1L101S, U8-ch0, adc0

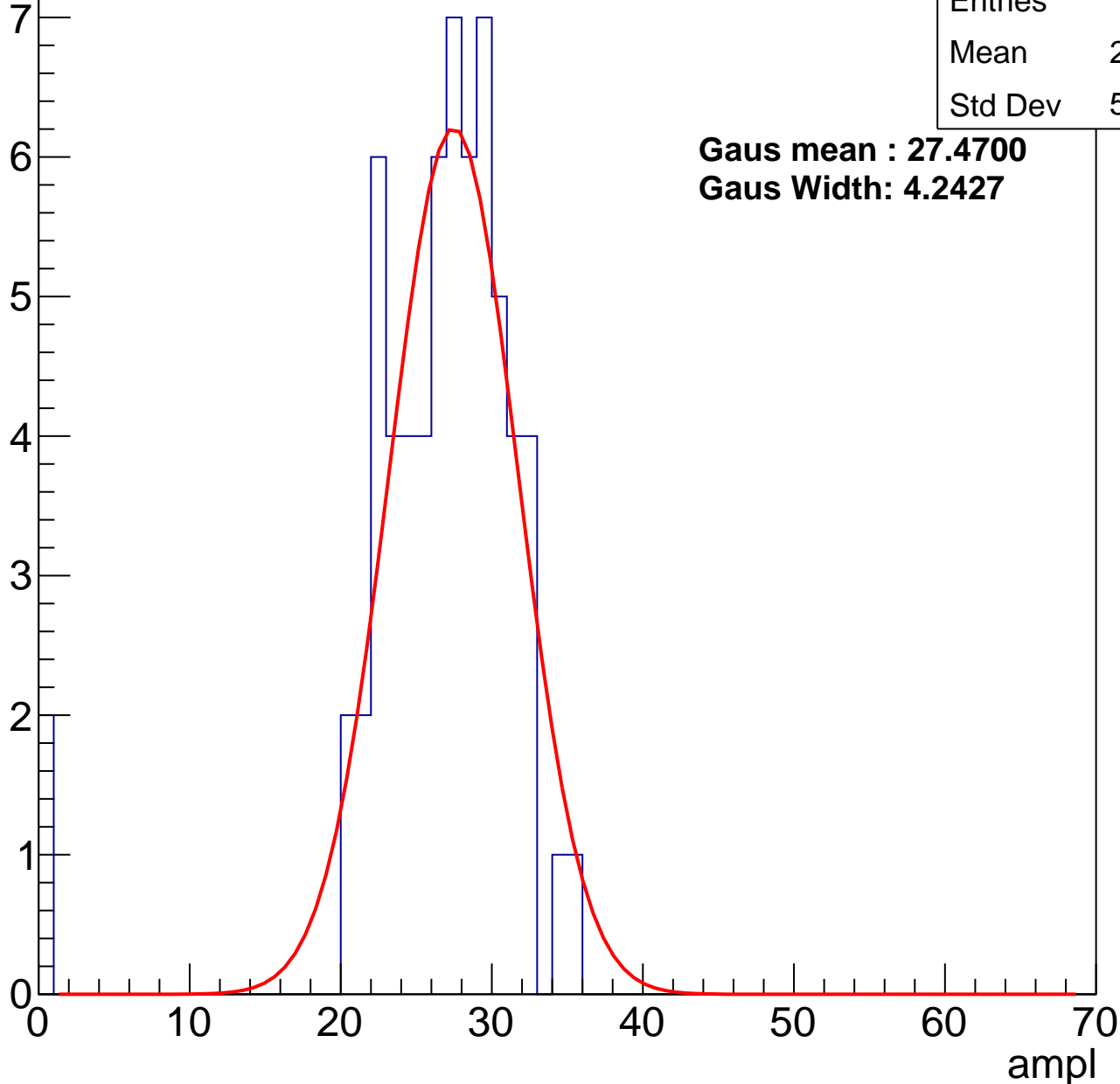
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	25.98
Std Dev	5.803

**Gaus mean : 27.4700**

**Gaus Width: 4.2427**



# B1L101S, U8-ch0, adc1

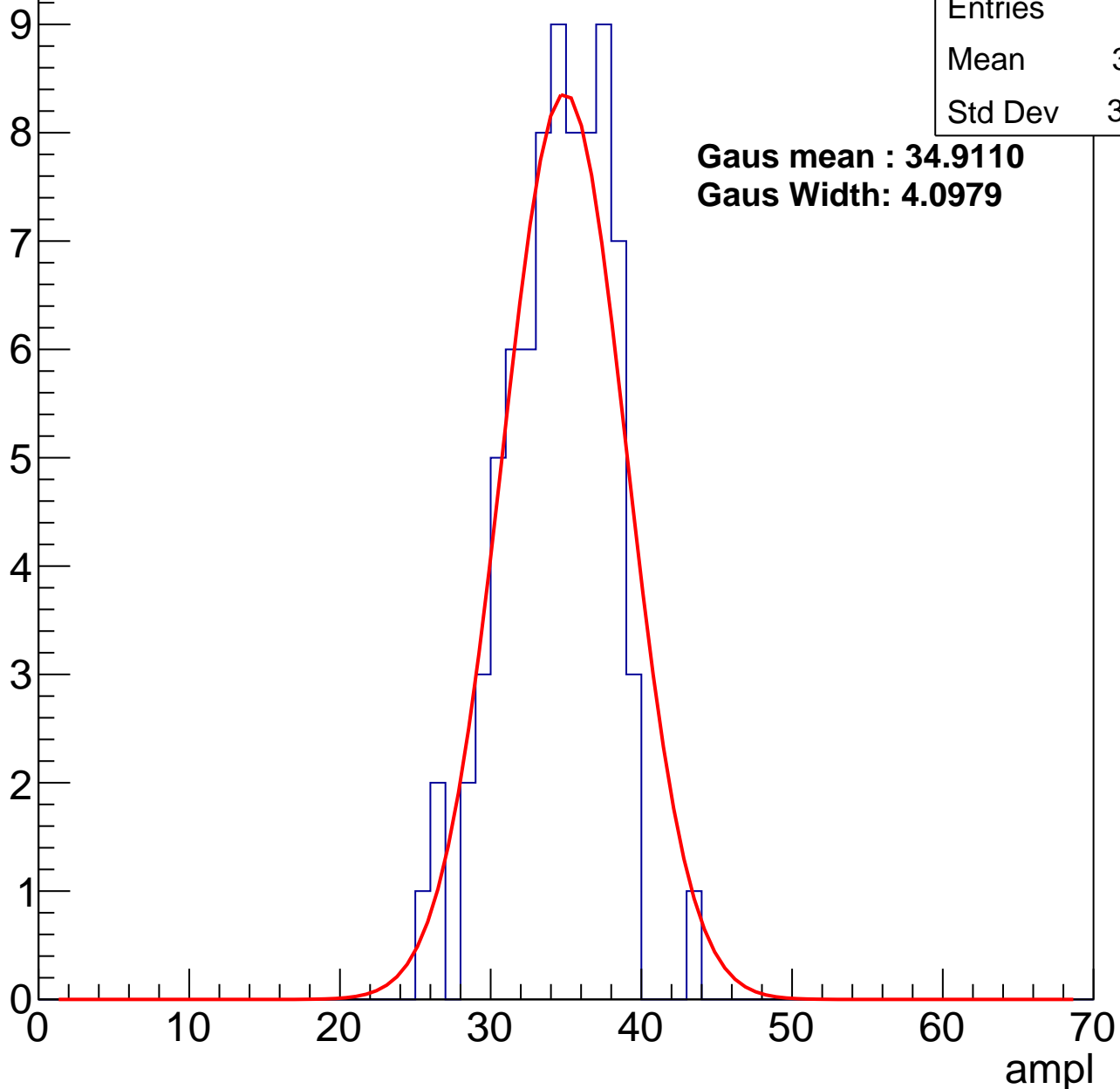
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	33.91
Std Dev	3.416

**Gaus mean : 34.9110**

**Gaus Width: 4.0979**



# B1L101S, U8-ch0, adc2

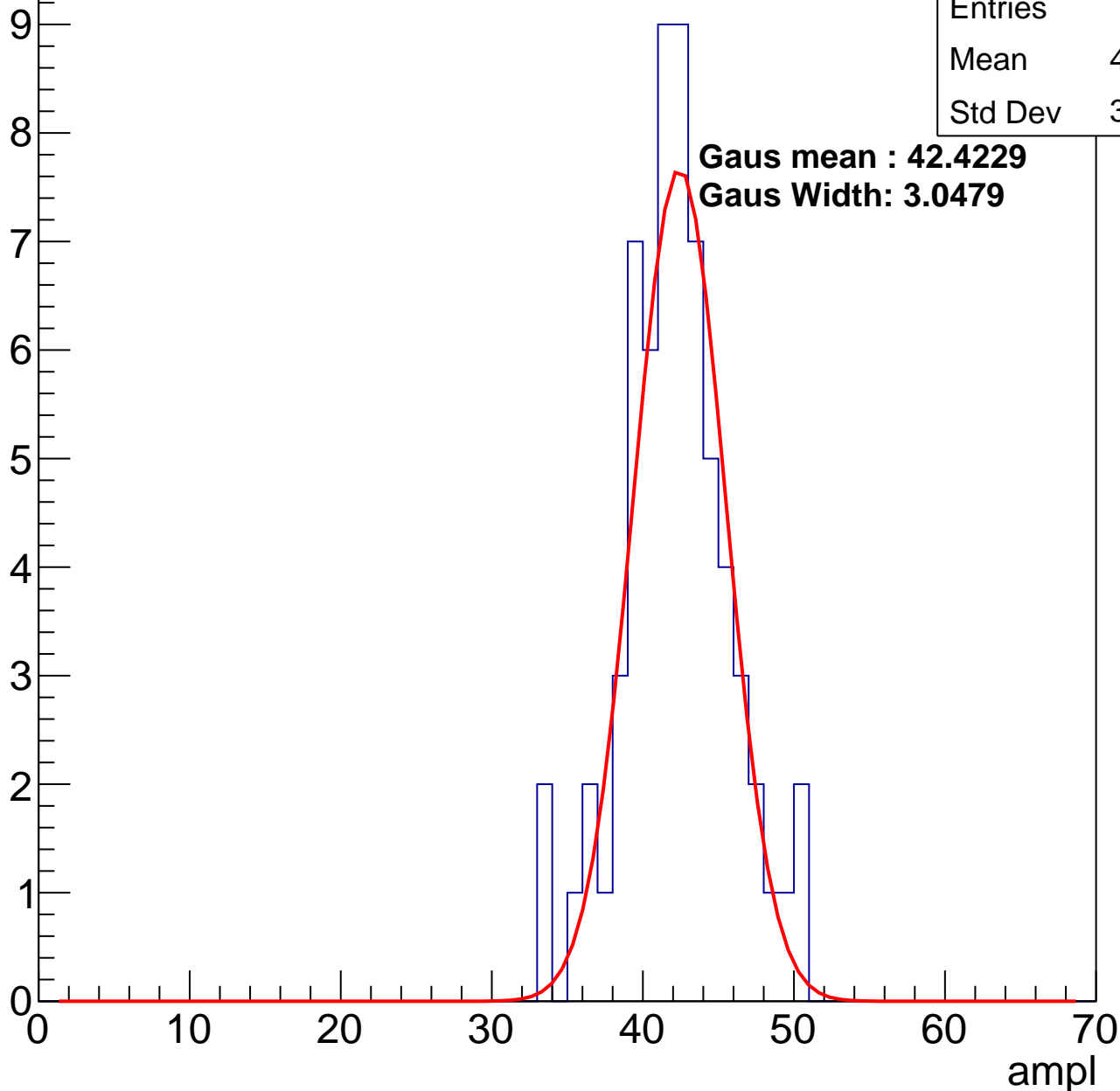
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	41.75
Std Dev	3.556

**Gaus mean : 42.4229**

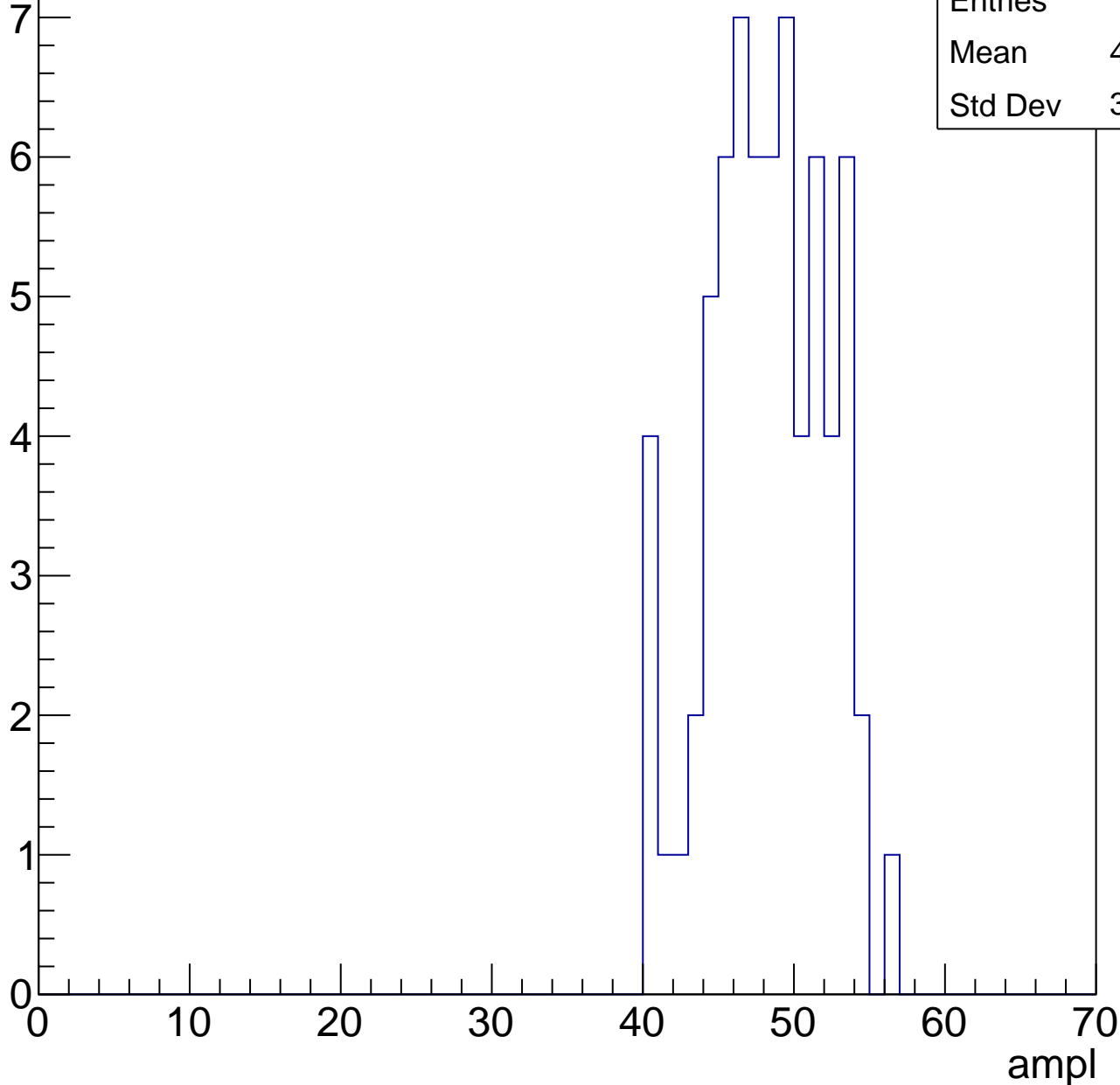
**Gaus Width: 3.0479**



# B1L101S, U8-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

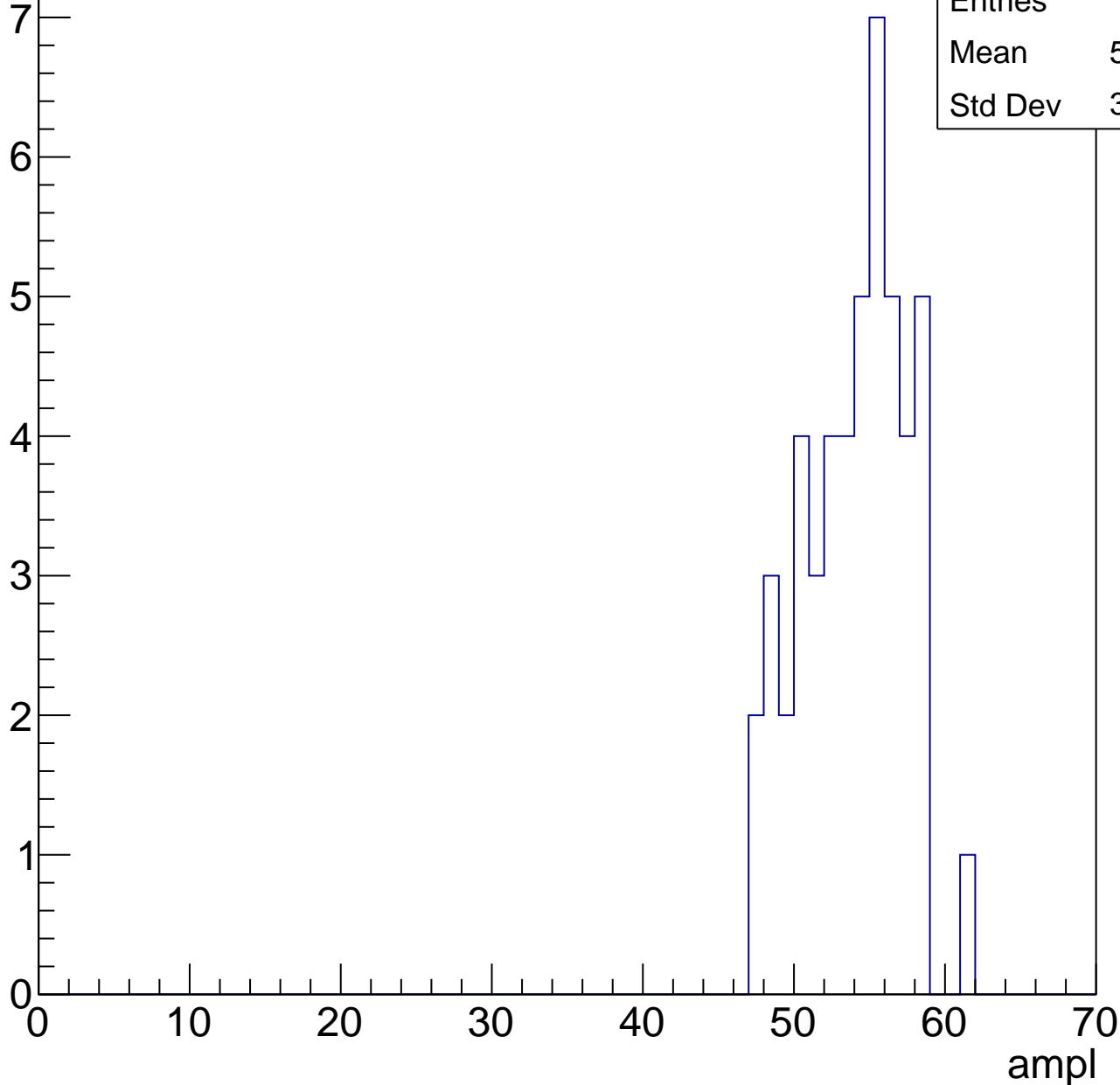


Entries	68
Mean	47.79
Std Dev	3.802

# B1L101S, U8-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

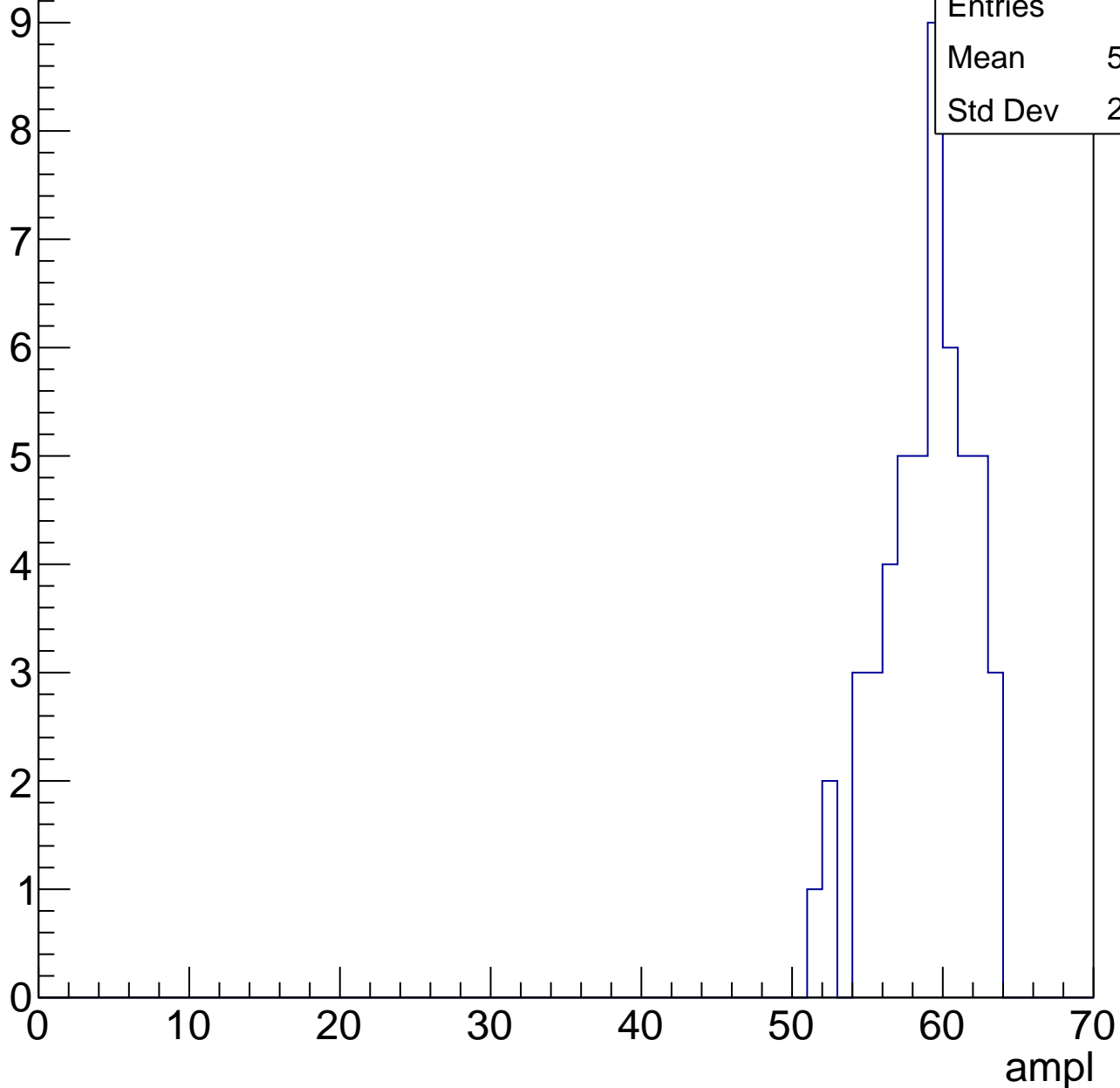
Entry



# B1L101S, U8-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



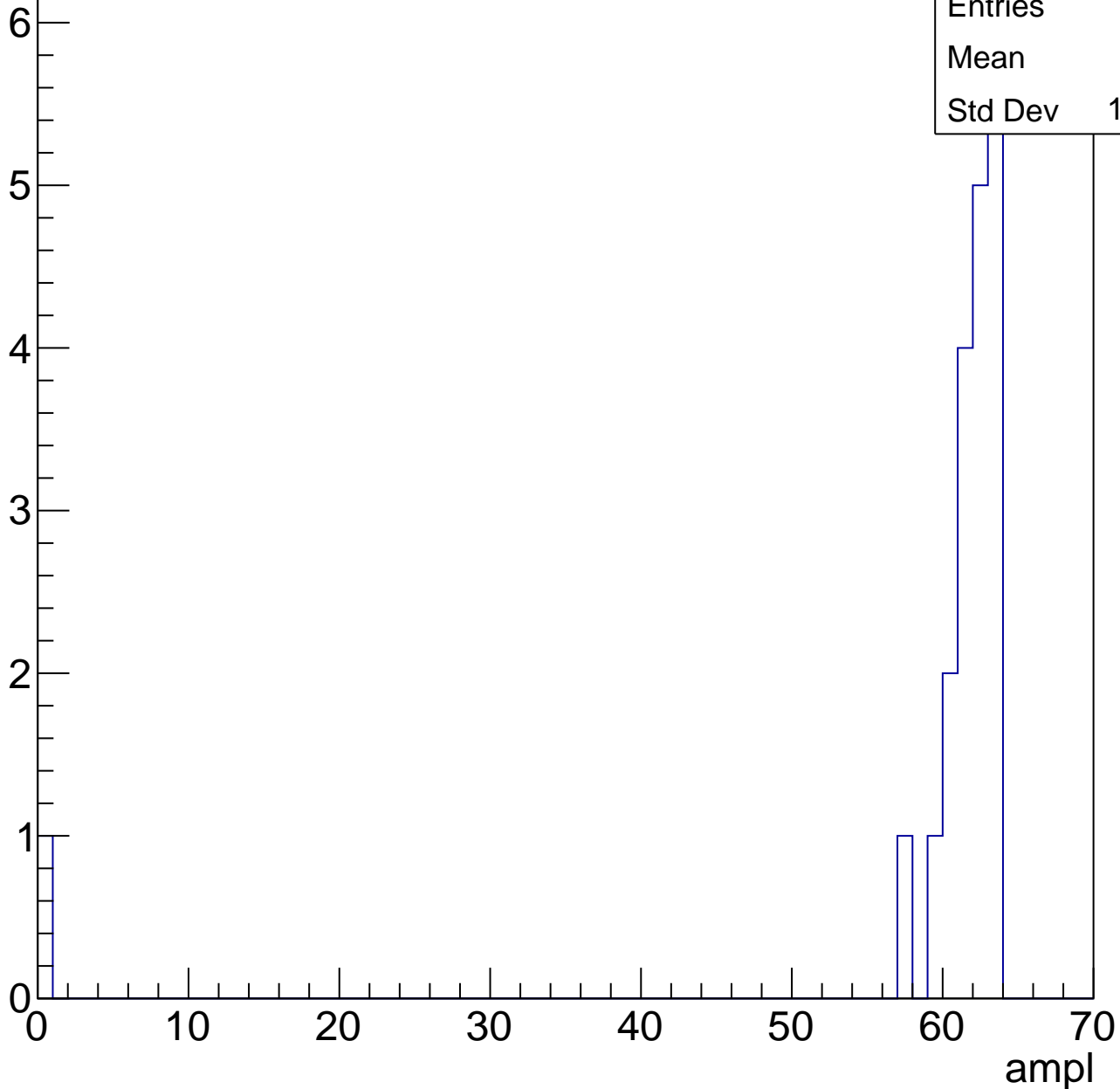
Entries	51
Mean	58.35
Std Dev	2.949

# B1L101S, U8-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	20
Mean	58.4
Std Dev	13.48





# B1L101S, U8-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

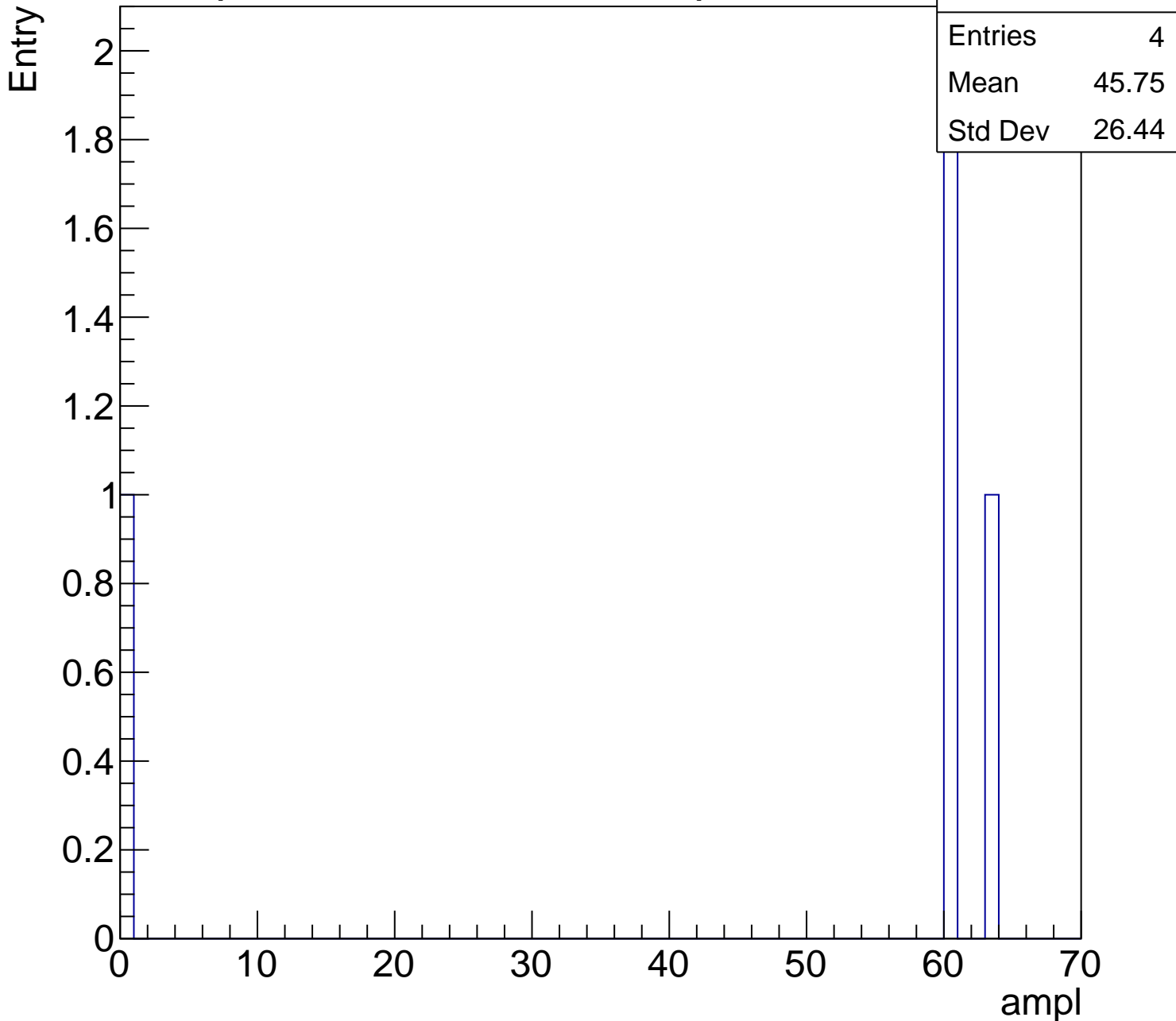
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	45.75
Std Dev	26.44

0 10 20 30 40 50 60 70

ampl



# B1L101S, U8-ch1, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	85
Mean	29.78
Std Dev	5.166

**Gaus mean : 30.3883**

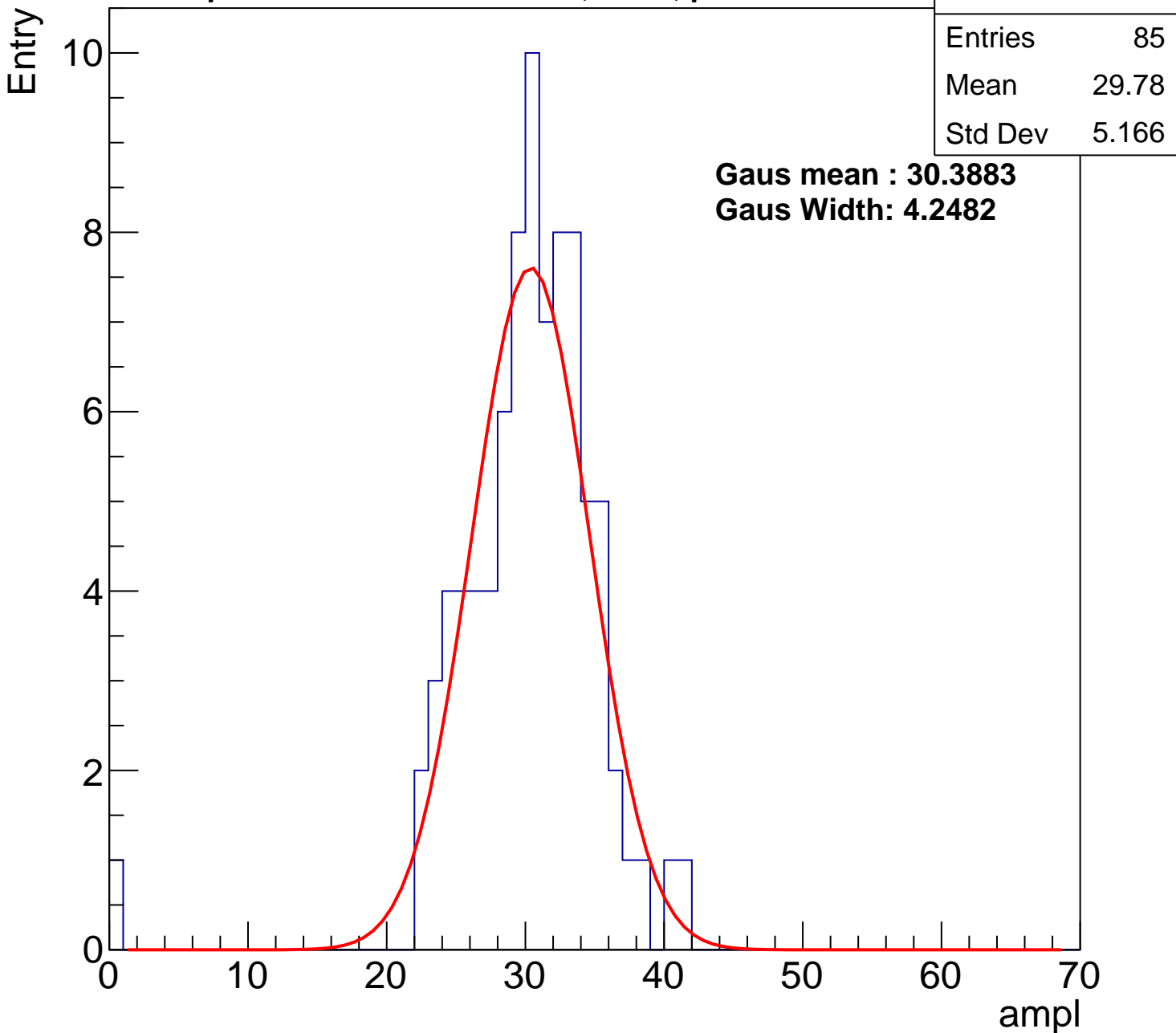
**Gaus Width: 4.2482**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U8-ch1, adc1

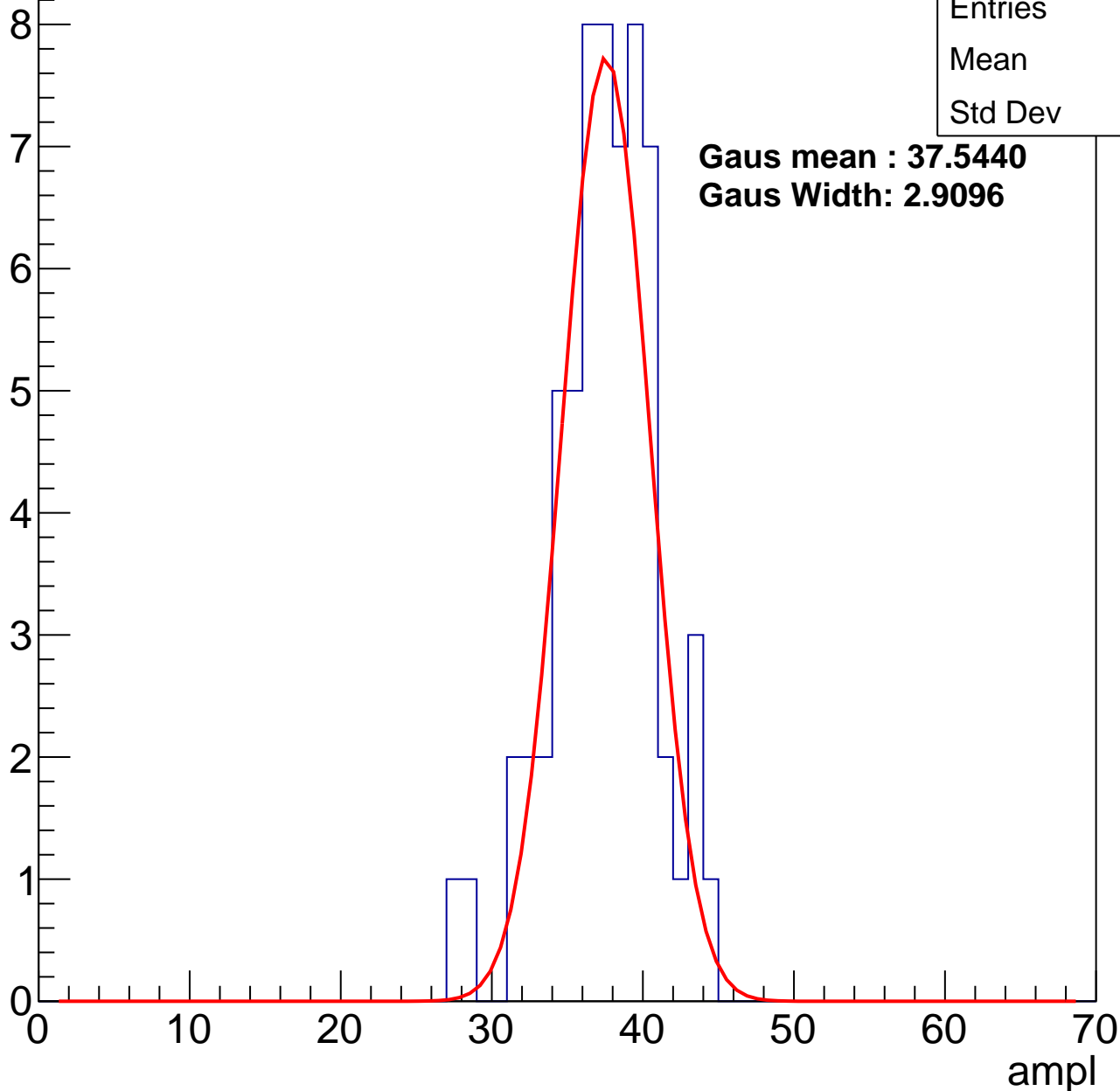
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	37
Std Dev	3.39

**Gaus mean : 37.5440**

**Gaus Width: 2.9096**



# B1L101S, U8-ch1, adc2

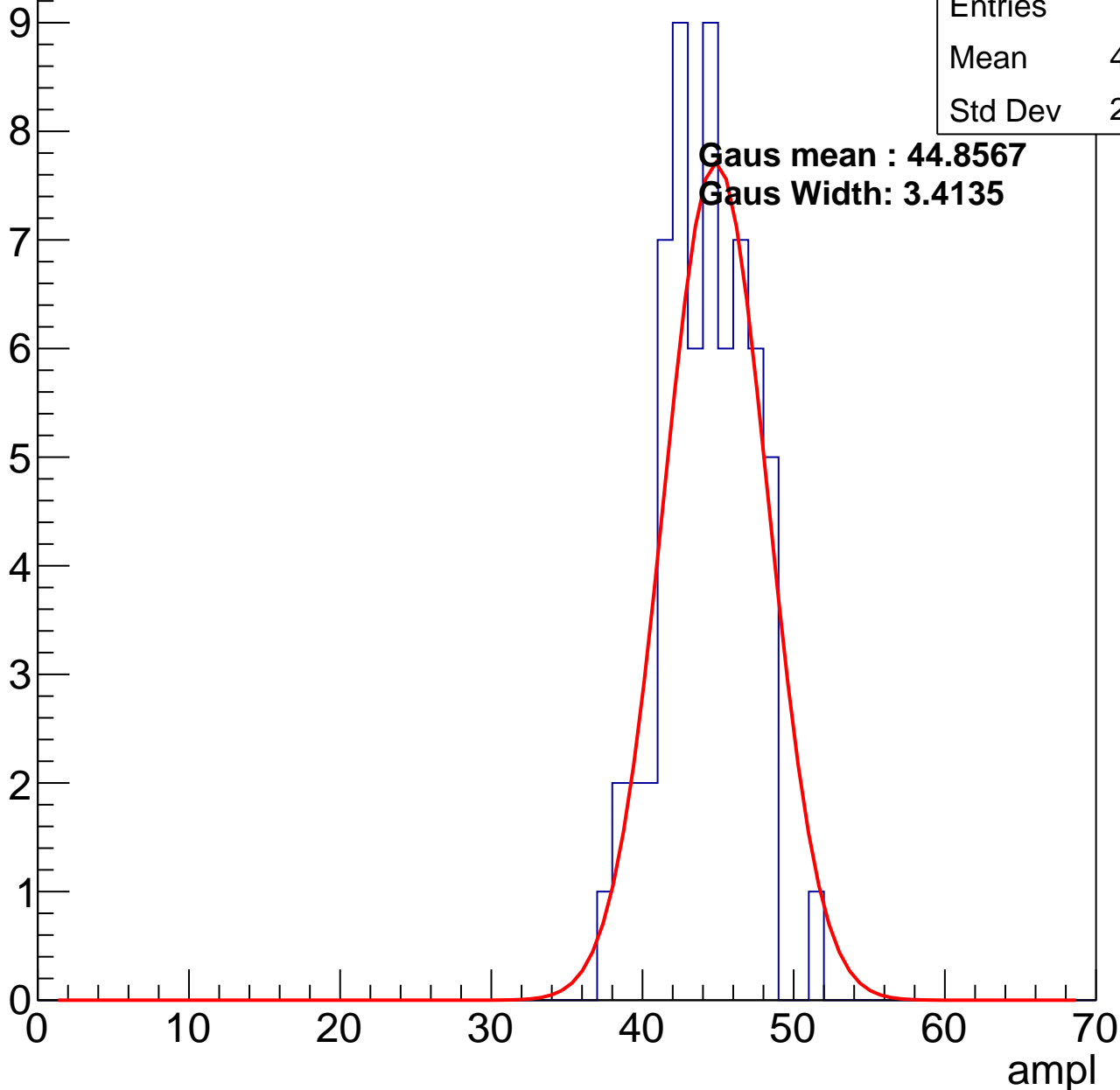
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	43.73
Std Dev	2.874

**Gaus mean : 44.8567**

**Gaus Width: 3.4135**



# B1L101S, U8-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

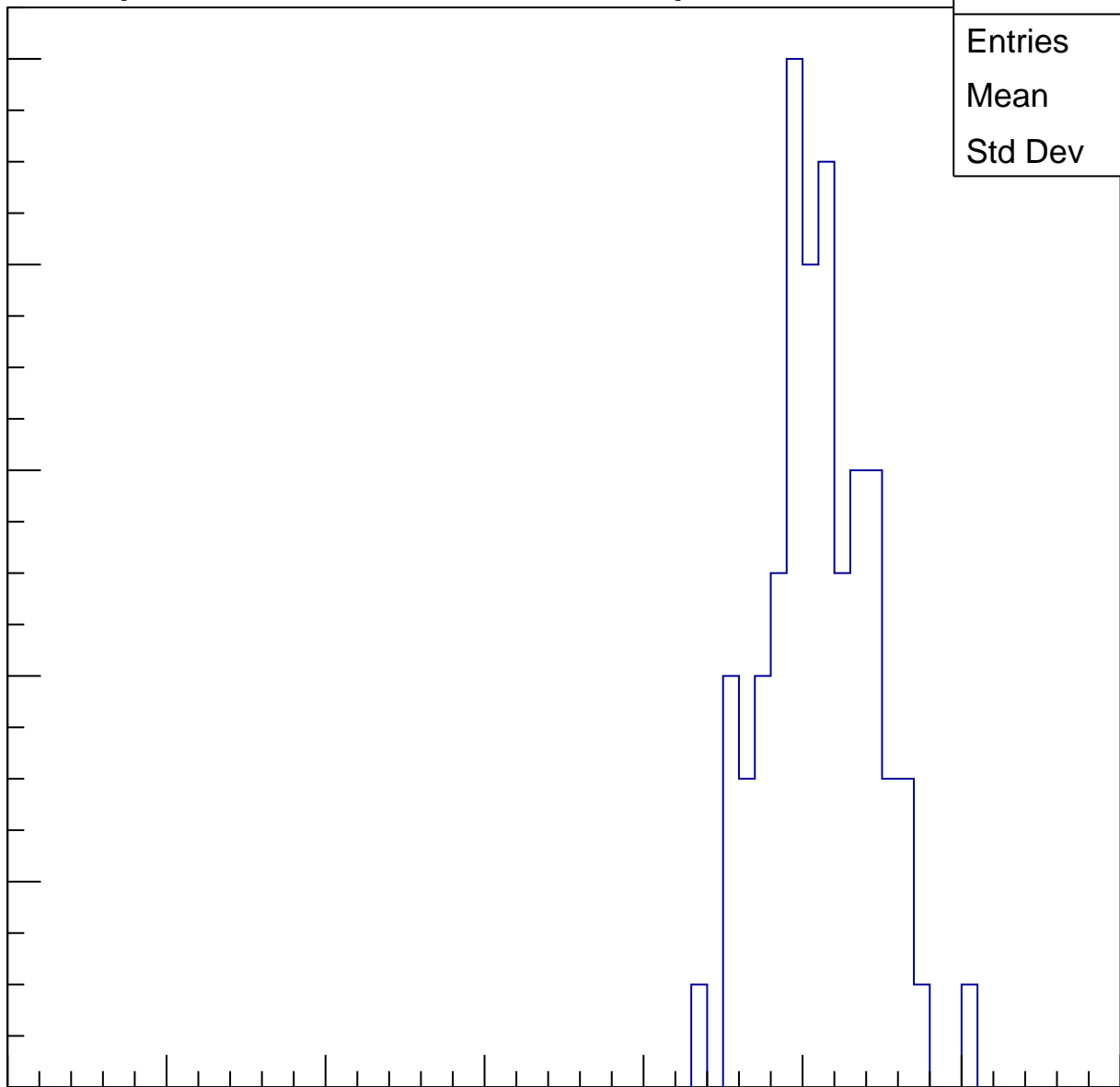
Entries	69
Mean	50.58
Std Dev	3.299

Entry

10  
8  
6  
4  
2  
0

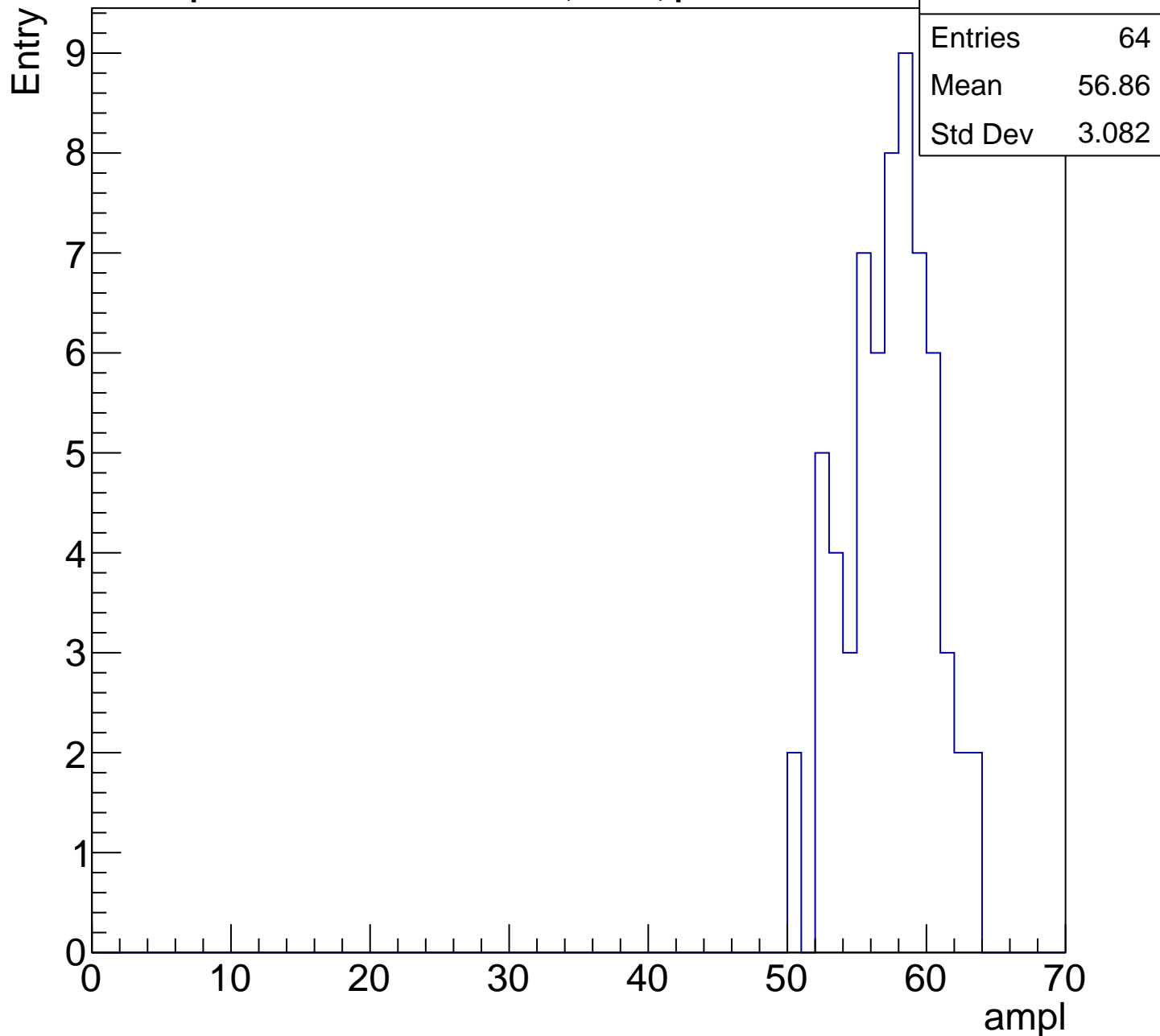
0 10 20 30 40 50 60 70

ampl



# B1L101S, U8-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U8-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

Entries	31
Mean	58.81
Std Dev	10.96

ampl

0

10

20

30

40

50

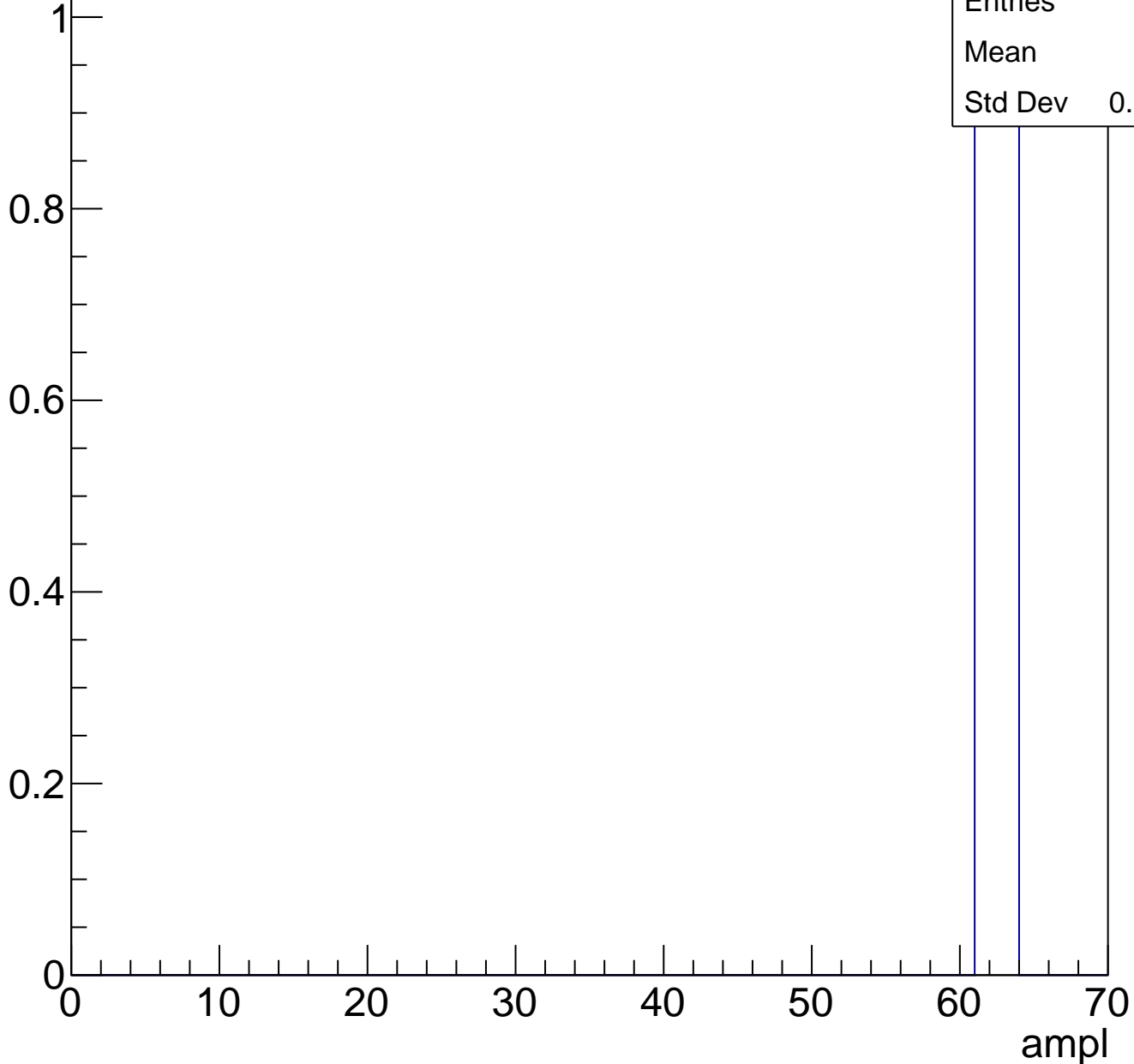
60

70

# B1L101S, U8-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U8-ch2, adc0

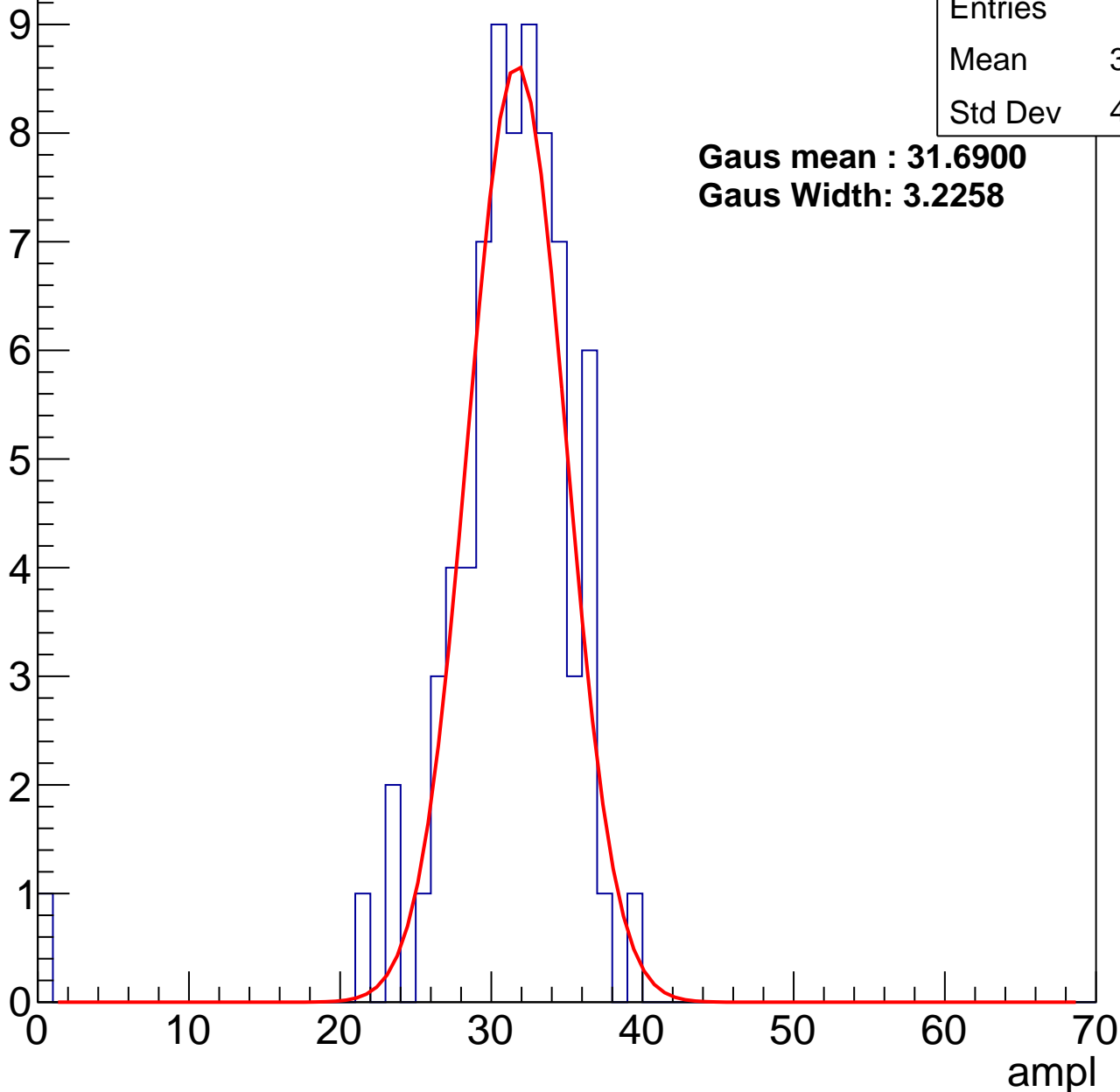
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	30.64
Std Dev	4.939

**Gaus mean : 31.6900**

**Gaus Width: 3.2258**



# B1L101S, U8-ch2, adc1

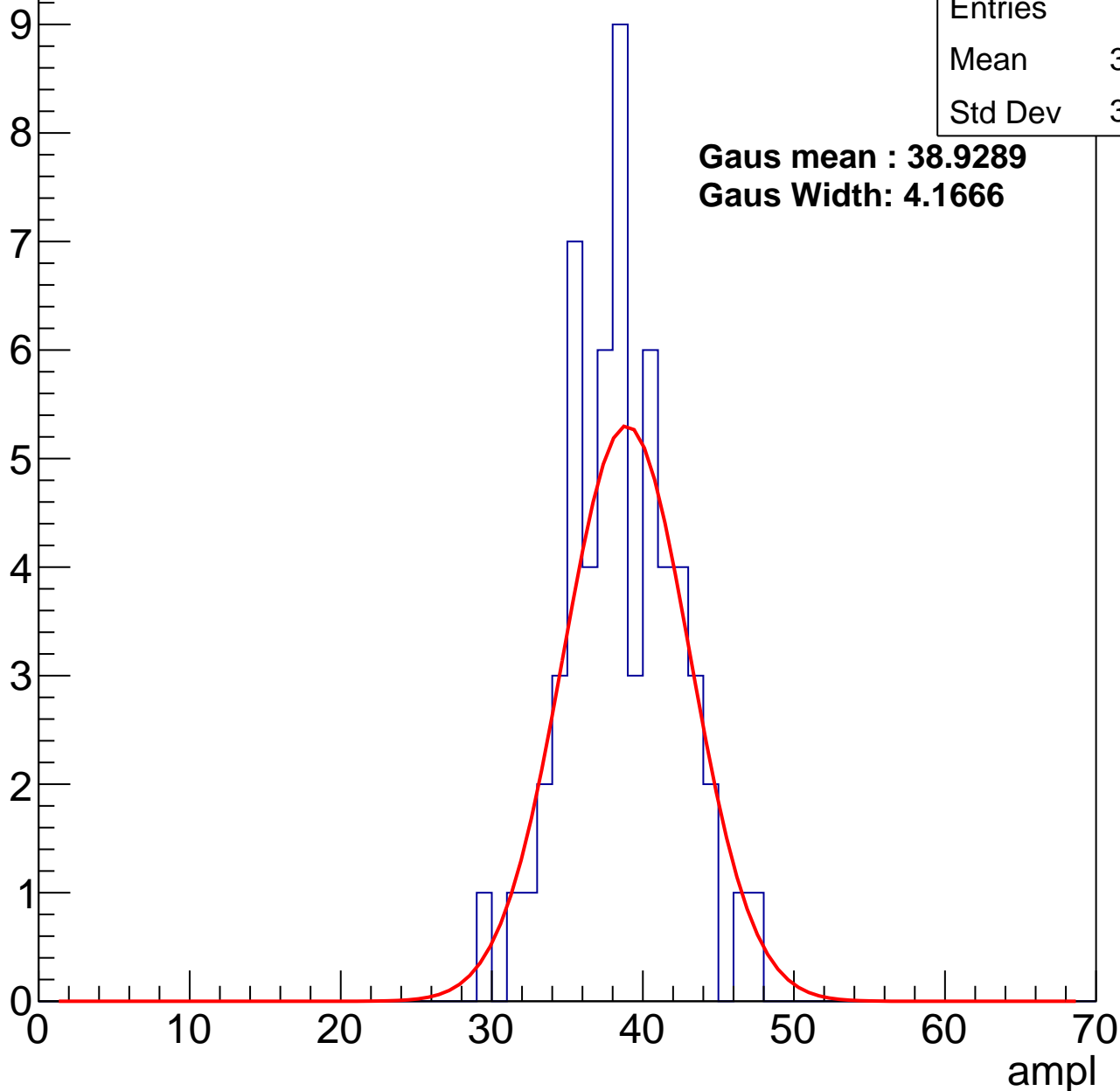
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	38.14
Std Dev	3.636

**Gaus mean : 38.9289**

**Gaus Width: 4.1666**



# B1L101S, U8-ch2, adc2

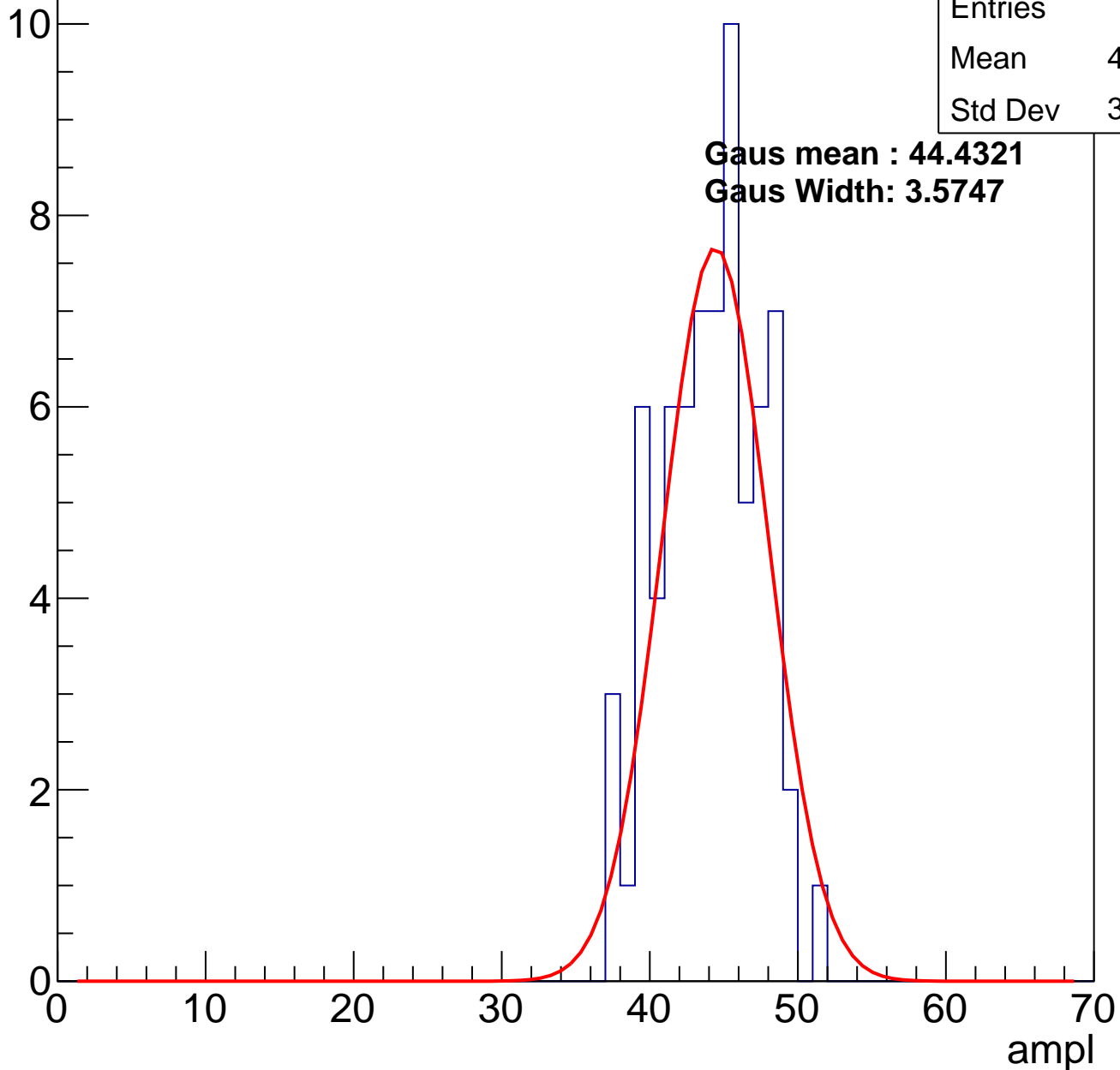
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	71
Mean	43.62
Std Dev	3.286

**Gaus mean : 44.4321**

**Gaus Width: 3.5747**

Entry



# B1L101S, U8-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

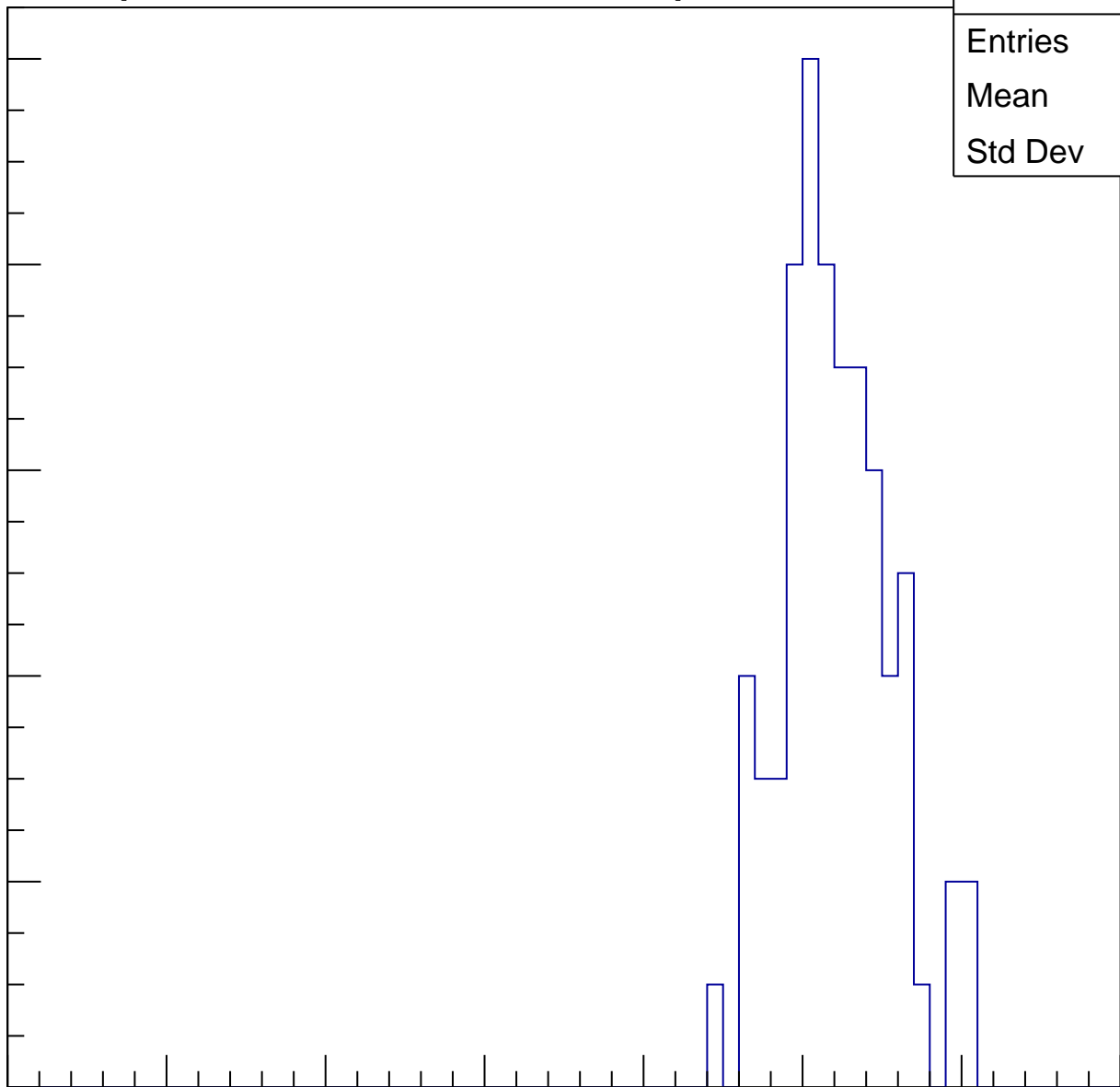
Entries	71
Mean	51.65
Std Dev	3.44

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U8-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

6

5

4

3

2

1

0

Entries	47
Mean	57.02
Std Dev	3.035

10

20

30

40

50

60

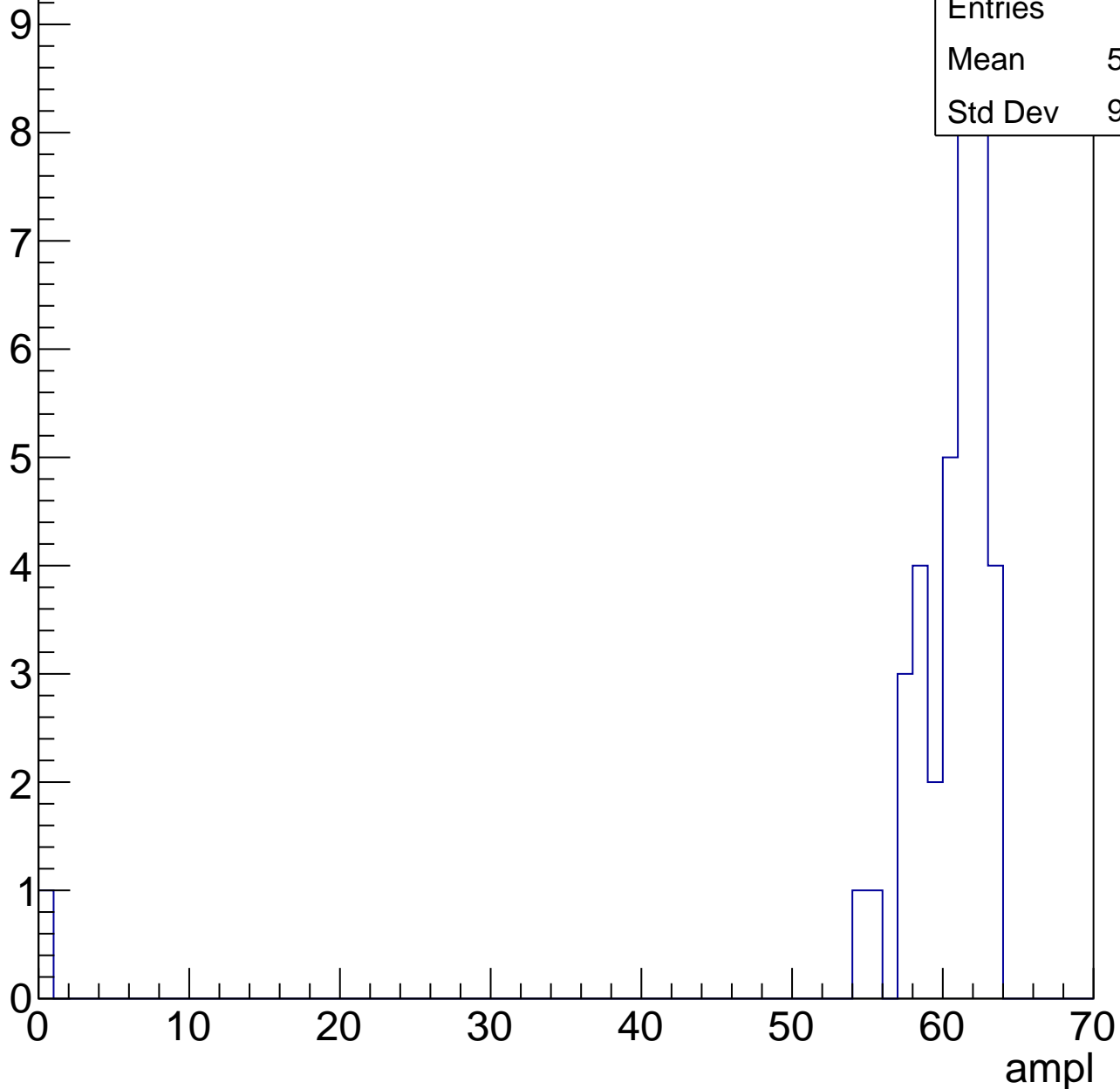
70

ampl

# B1L101S, U8-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

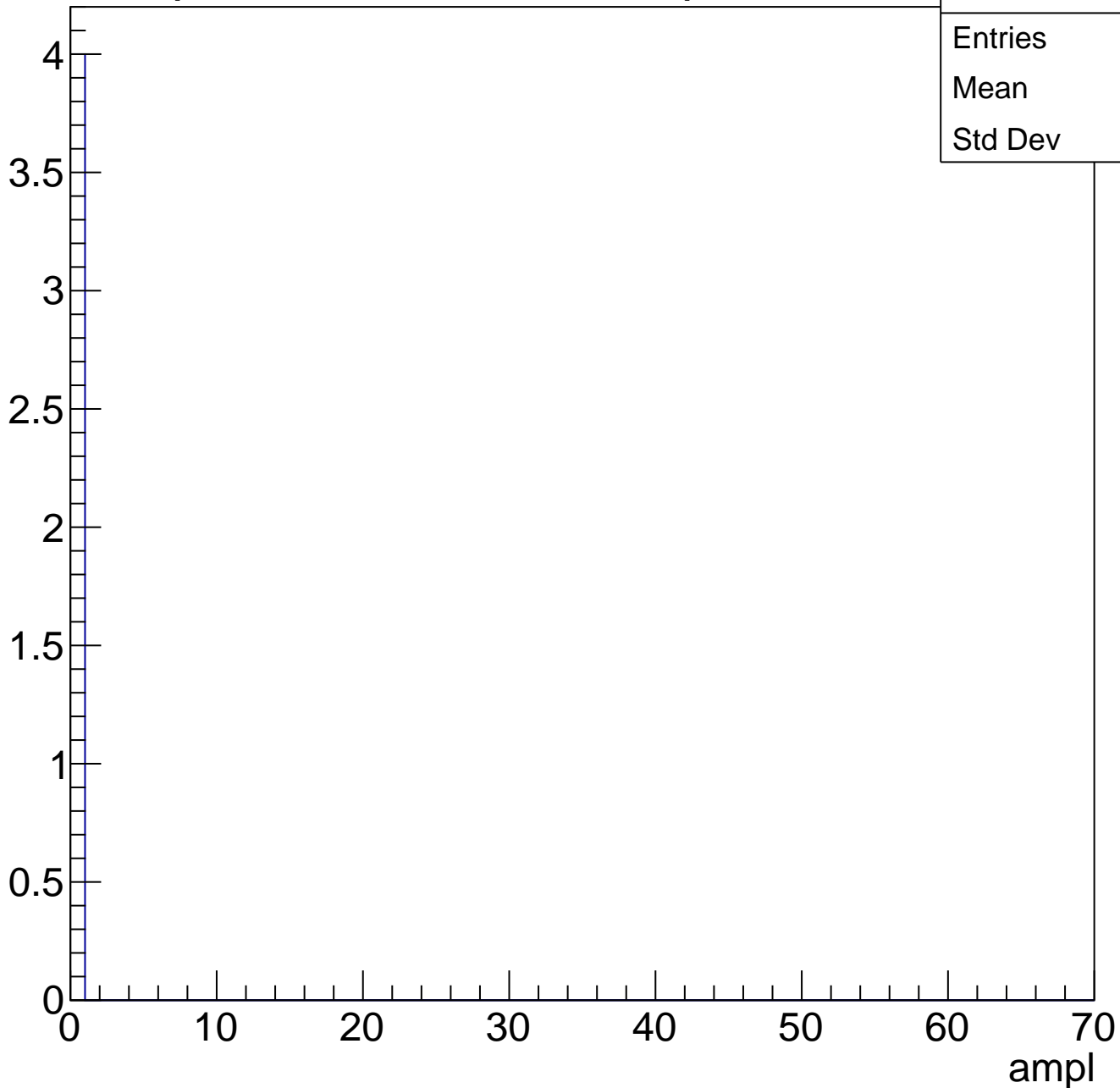




# B1L101S, U8-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	4
Mean	0
Std Dev	0

# B1L101S, U8-ch3, adc0

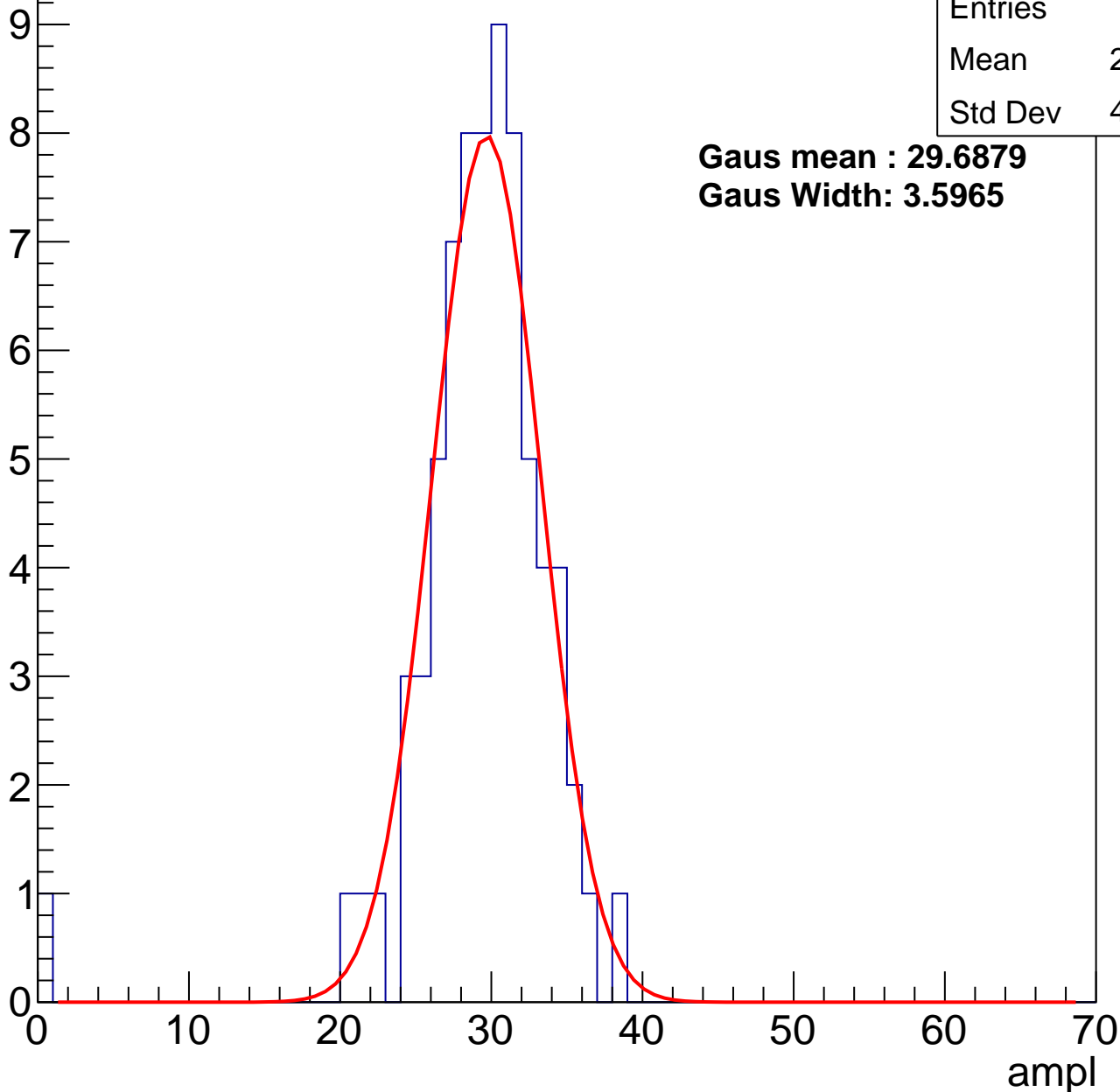
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	28.82
Std Dev	4.843

**Gaus mean : 29.6879**

**Gaus Width: 3.5965**



# B1L101S, U8-ch3, adc1

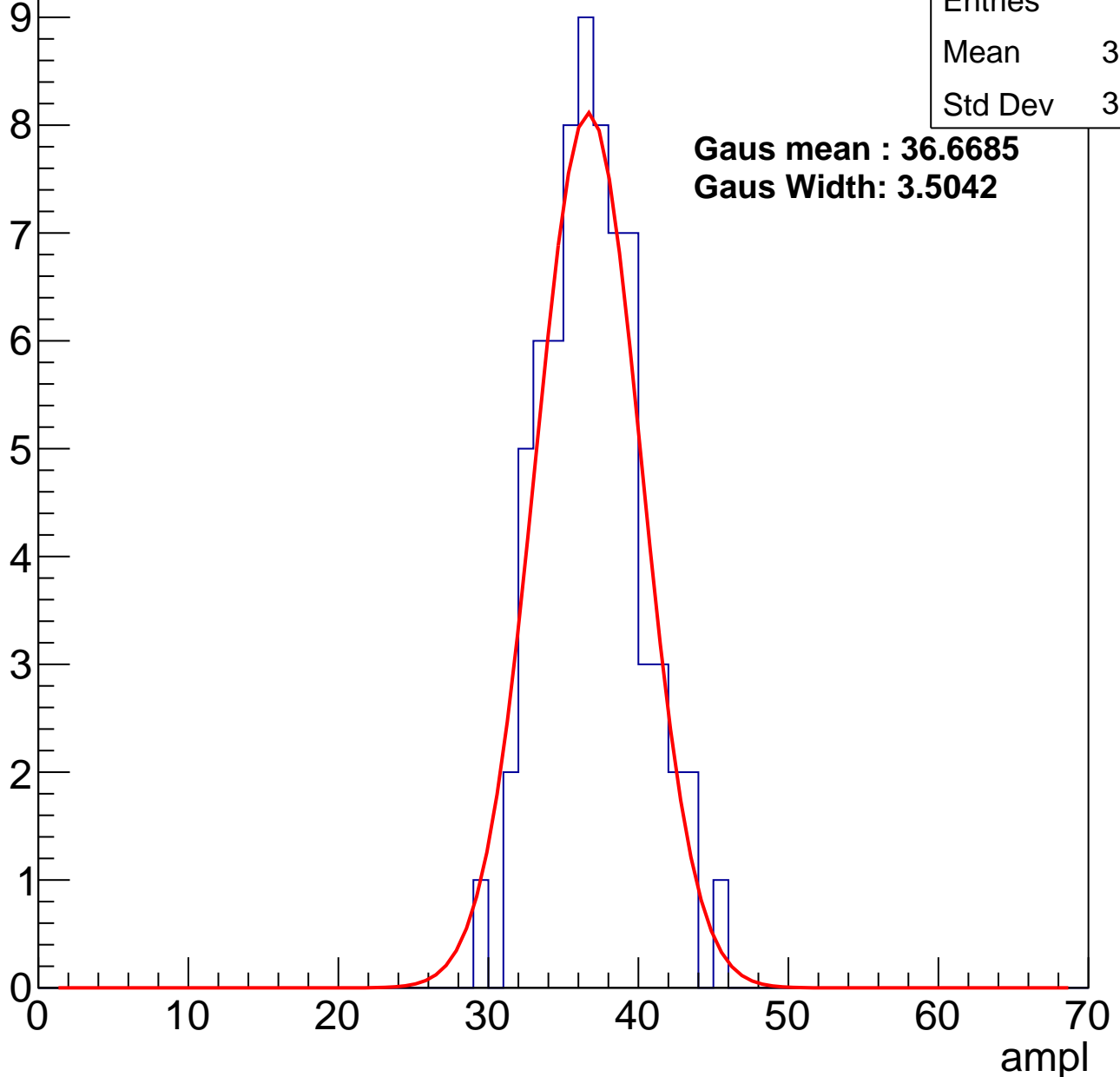
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	36.43
Std Dev	3.219

**Gaus mean : 36.6685**

**Gaus Width: 3.5042**



# B1L101S, U8-ch3, adc2

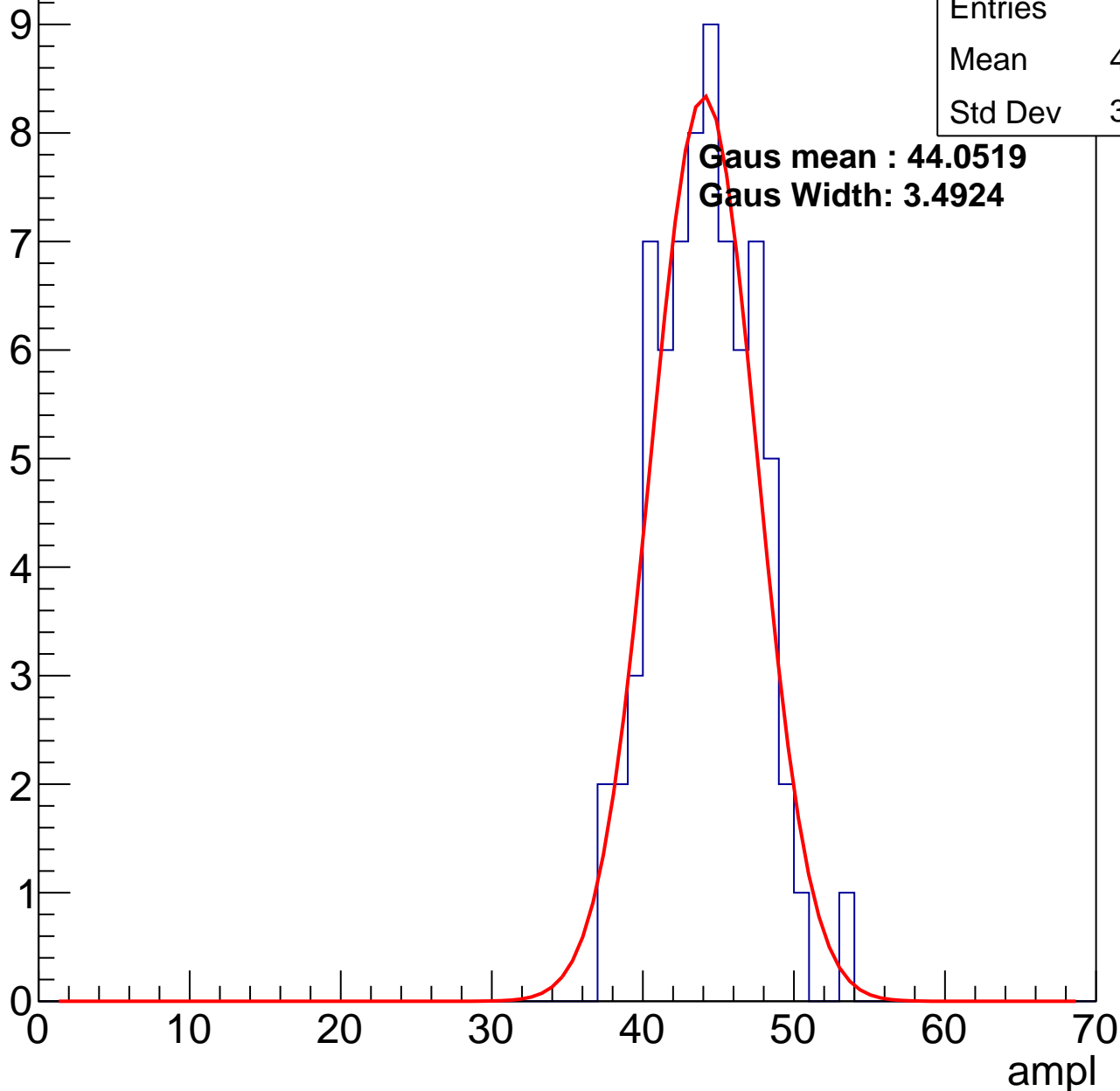
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	43.67
Std Dev	3.269

**Gaus mean : 44.0519**

**Gaus Width: 3.4924**

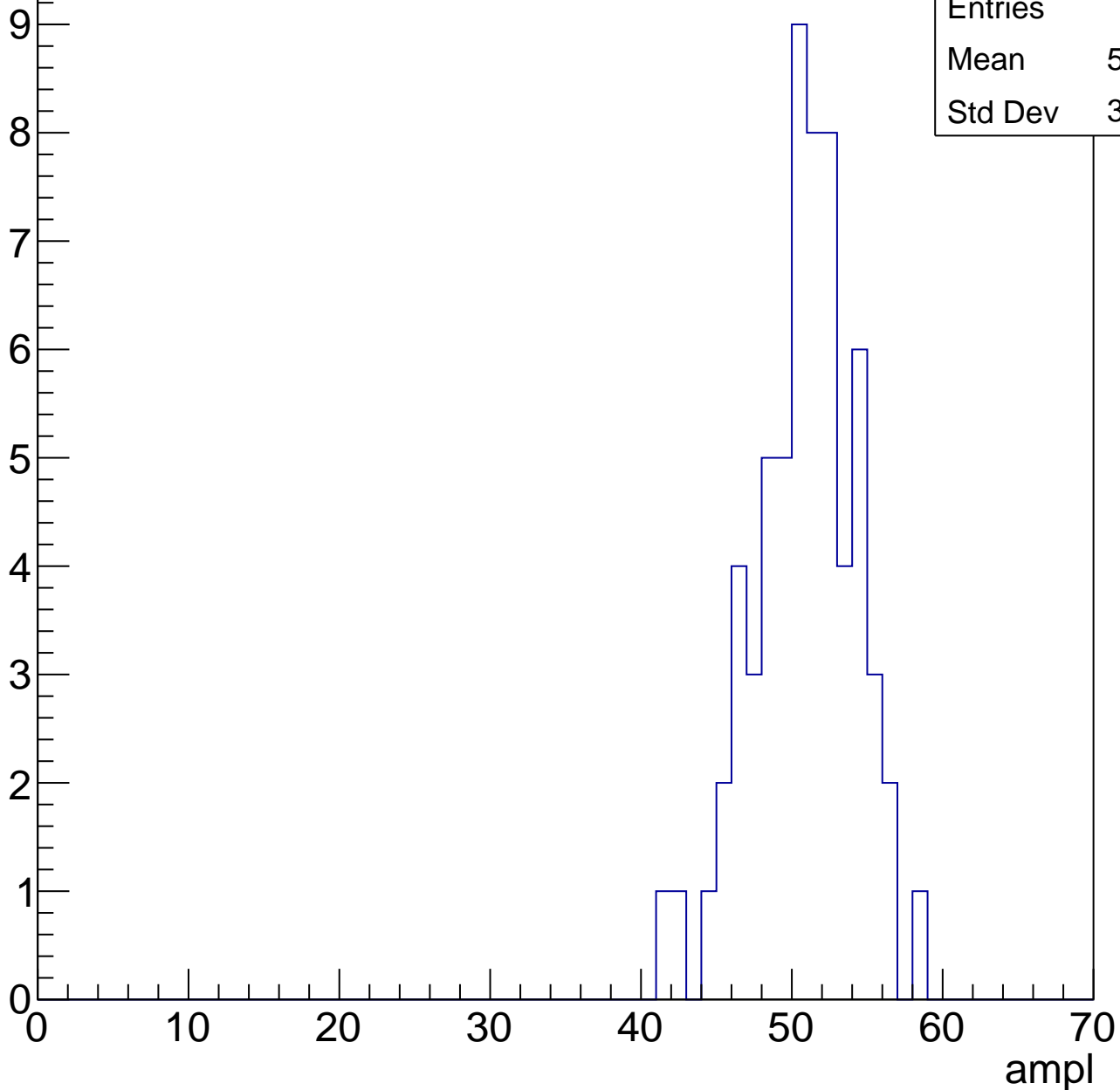


# B1L101S, U8-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

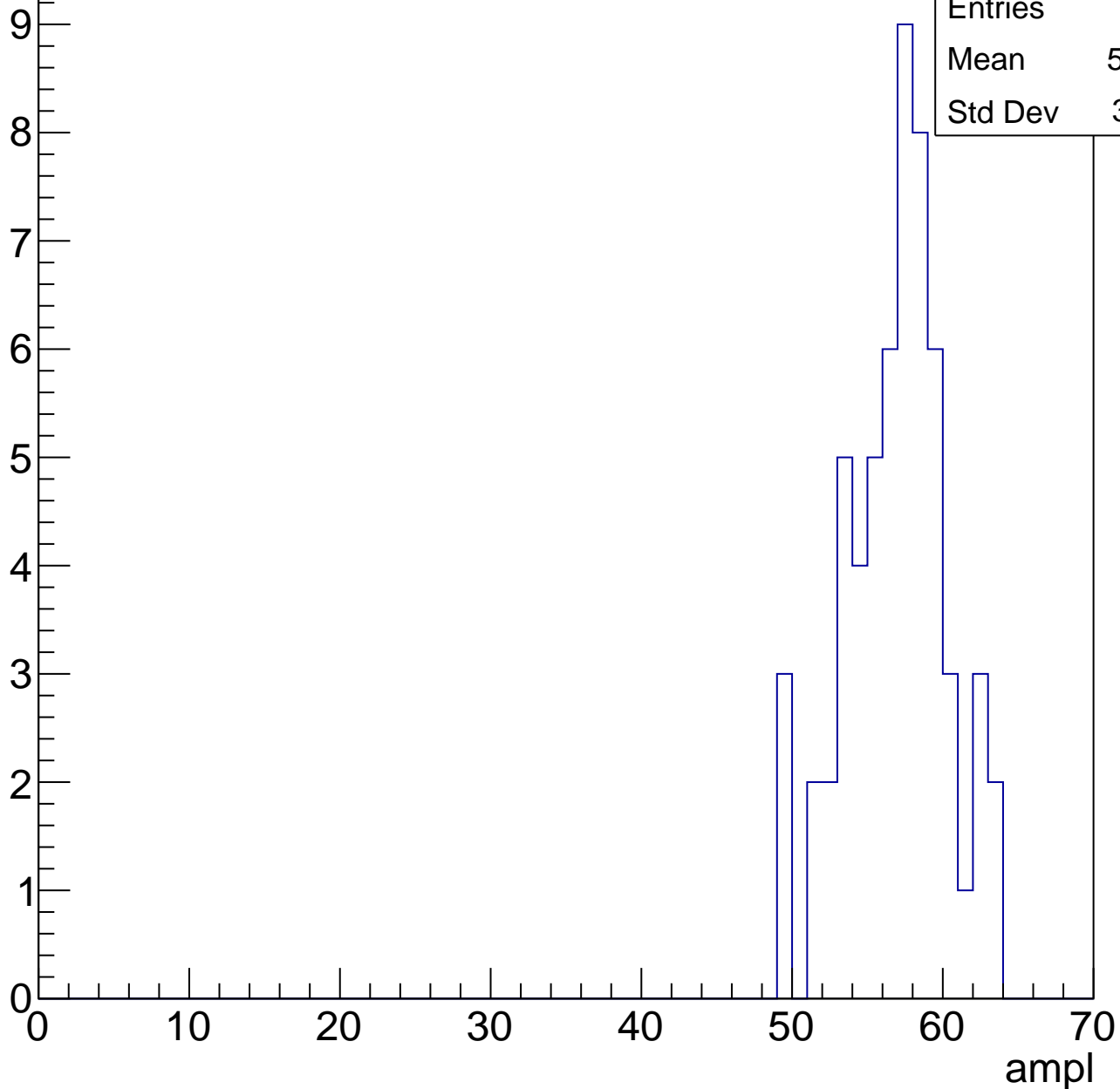
Entries	63
Mean	50.35
Std Dev	3.386



# B1L101S, U8-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

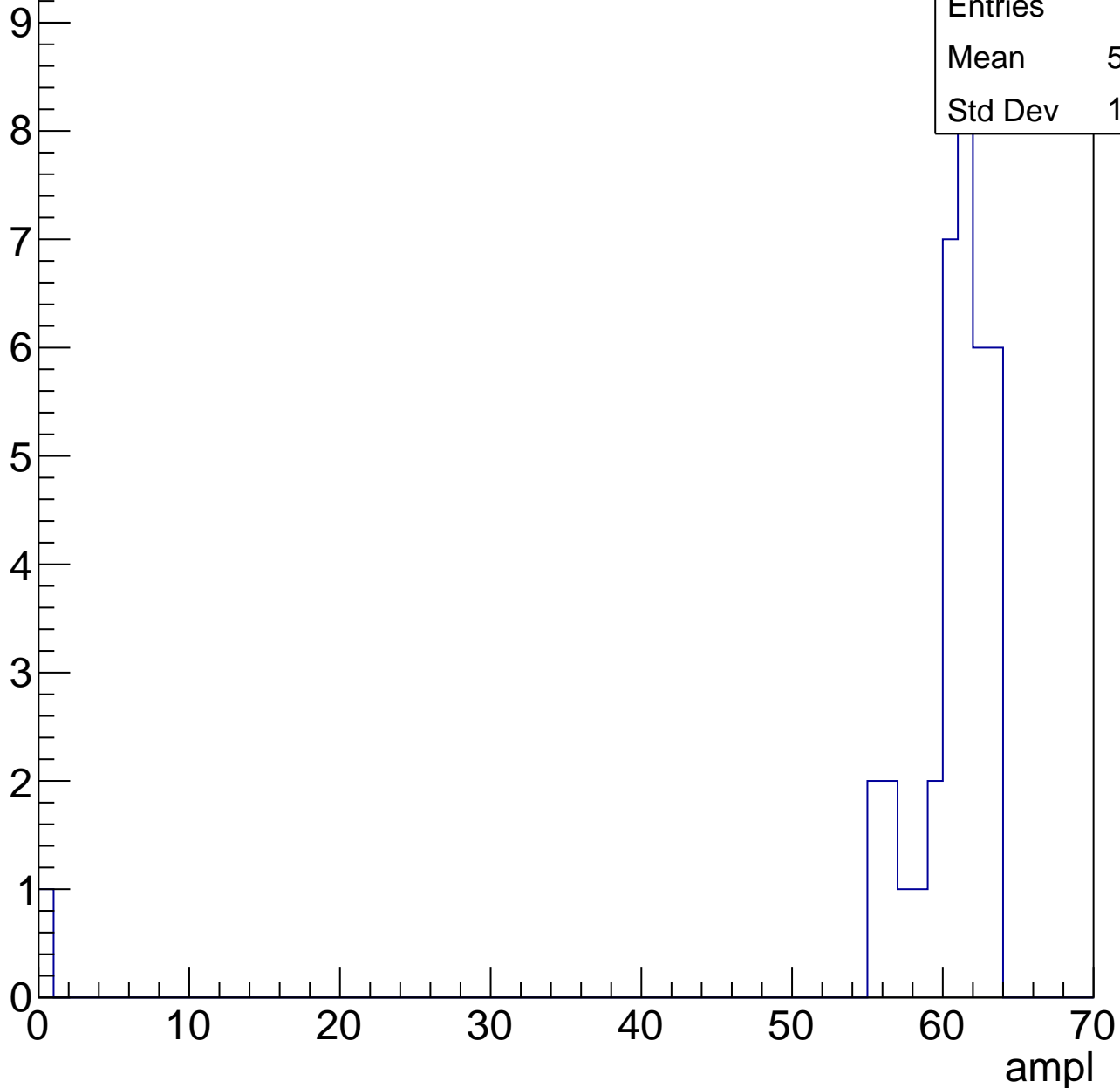


Entries	59
Mean	56.42
Std Dev	3.341

# B1L101S, U8-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

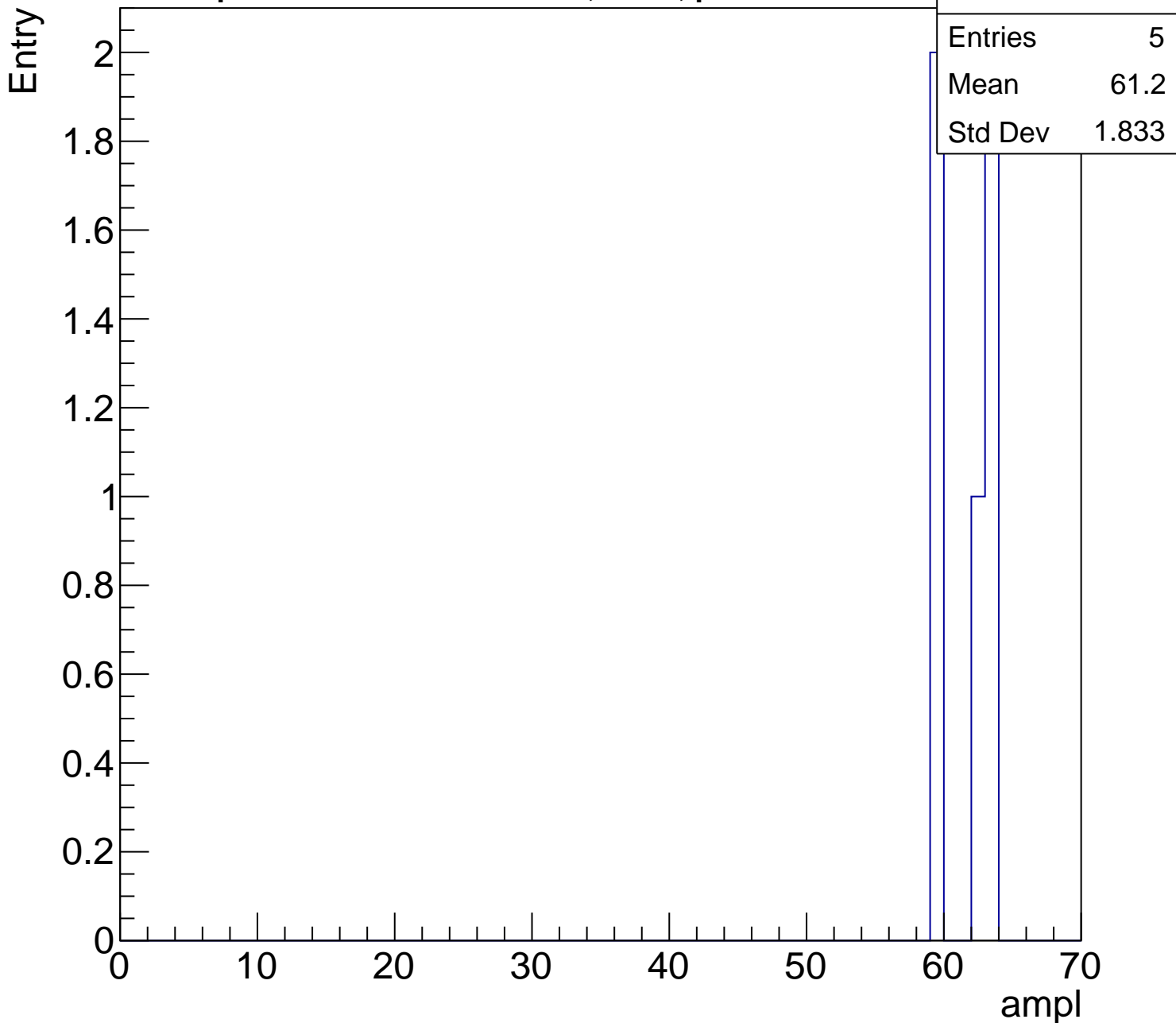
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.2
Std Dev	1.833

0 10 20 30 40 50 60 70

ampl





# B1L101S, U8-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	20
Std Dev	0

ampl

# B1L101S, U8-ch4, adc0

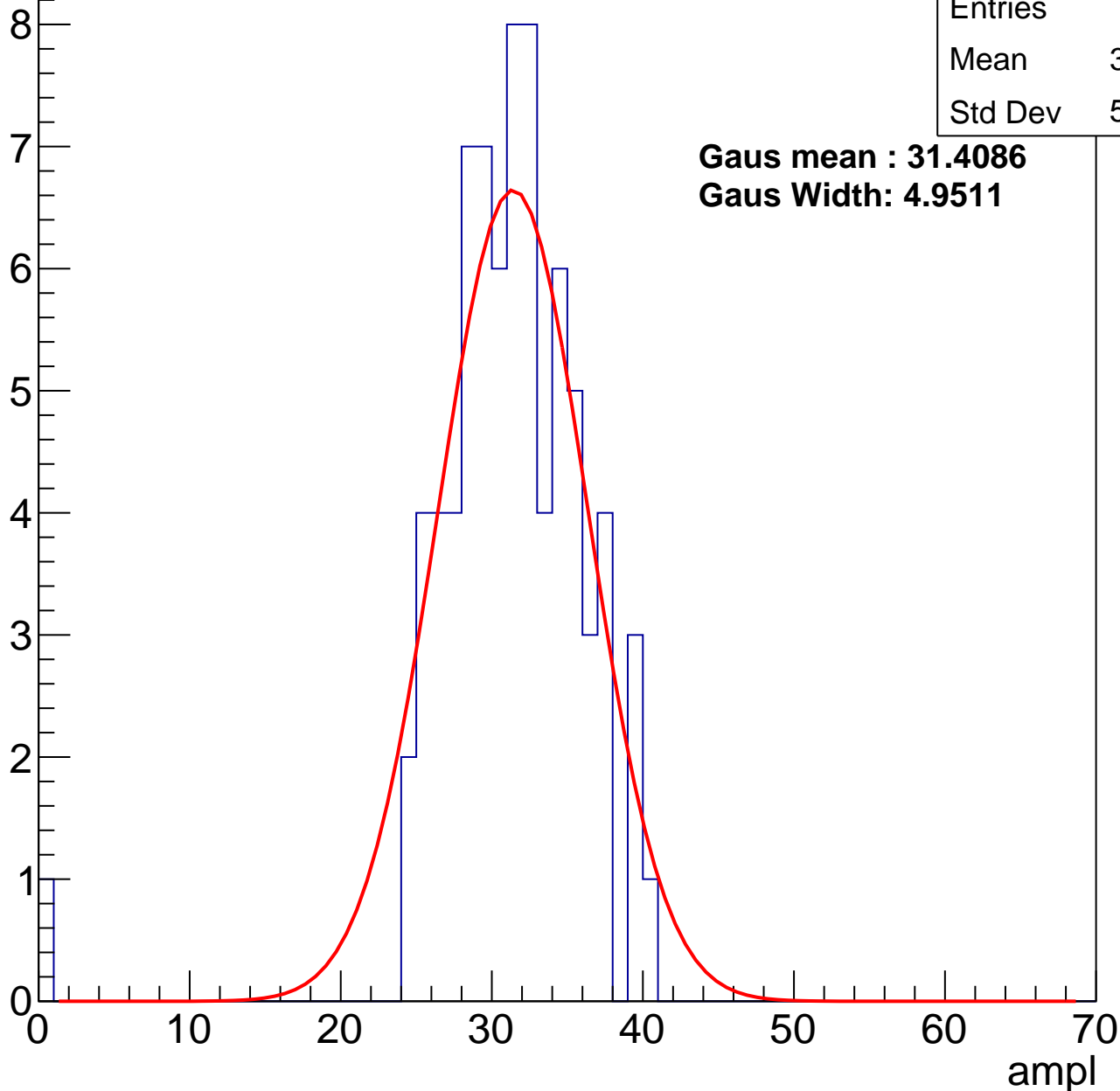
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	30.74
Std Dev	5.233

**Gaus mean : 31.4086**

**Gaus Width: 4.9511**



# B1L101S, U8-ch4, adc1

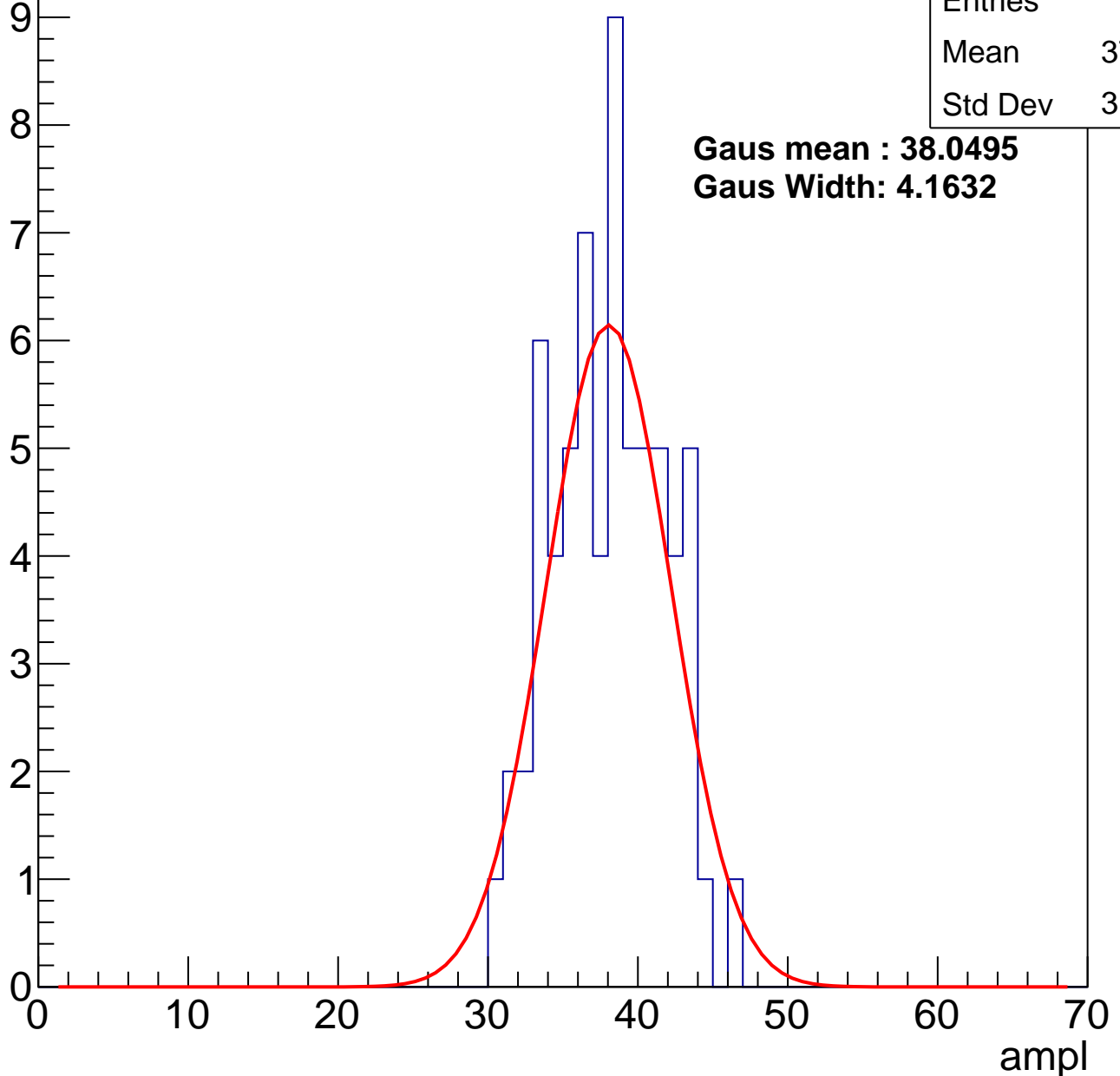
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	37.58
Std Dev	3.635

**Gaus mean : 38.0495**

**Gaus Width: 4.1632**



# B1L101S, U8-ch4, adc2

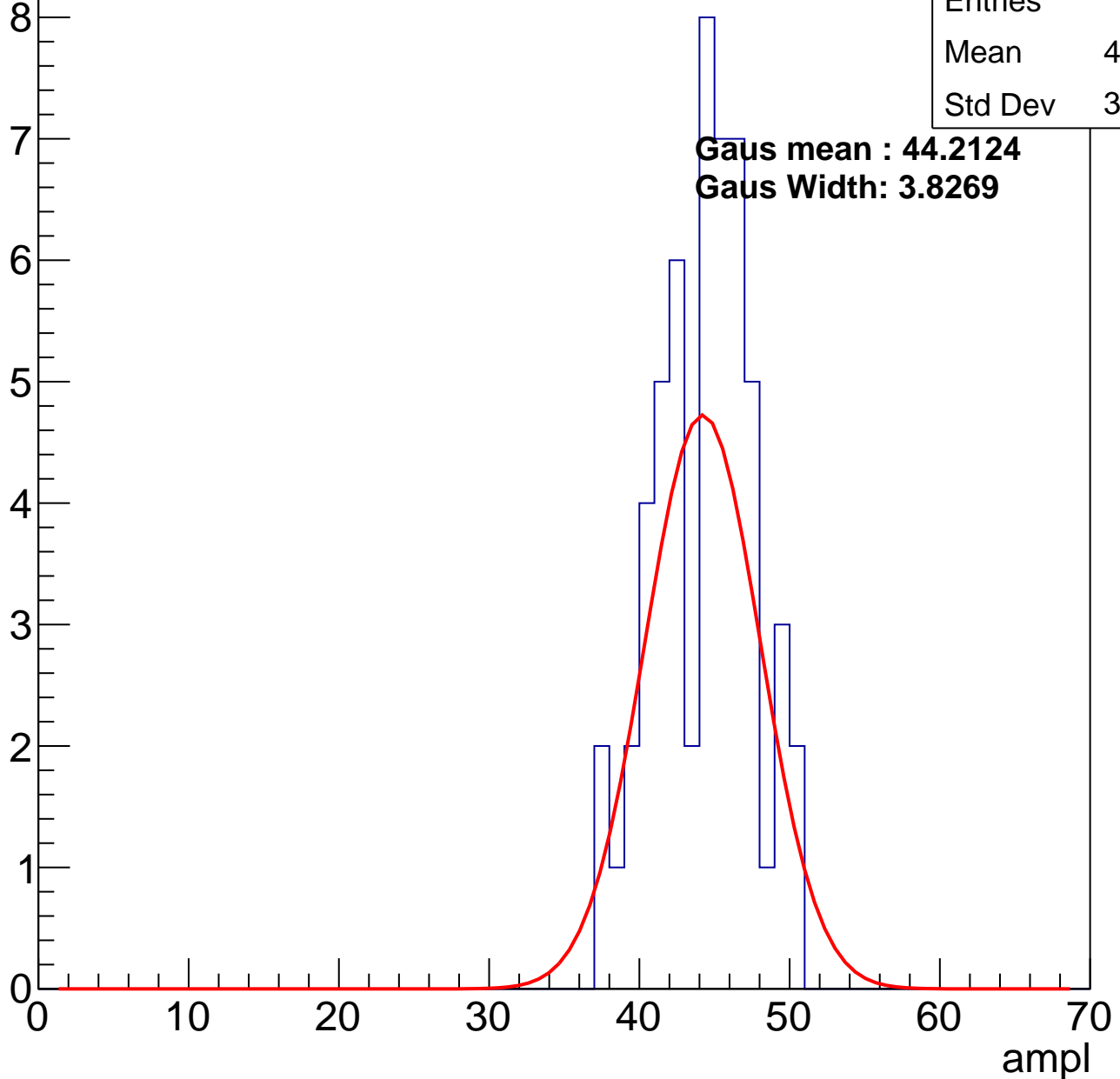
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	43.85
Std Dev	3.193

**Gaus mean : 44.2124**

**Gaus Width: 3.8269**

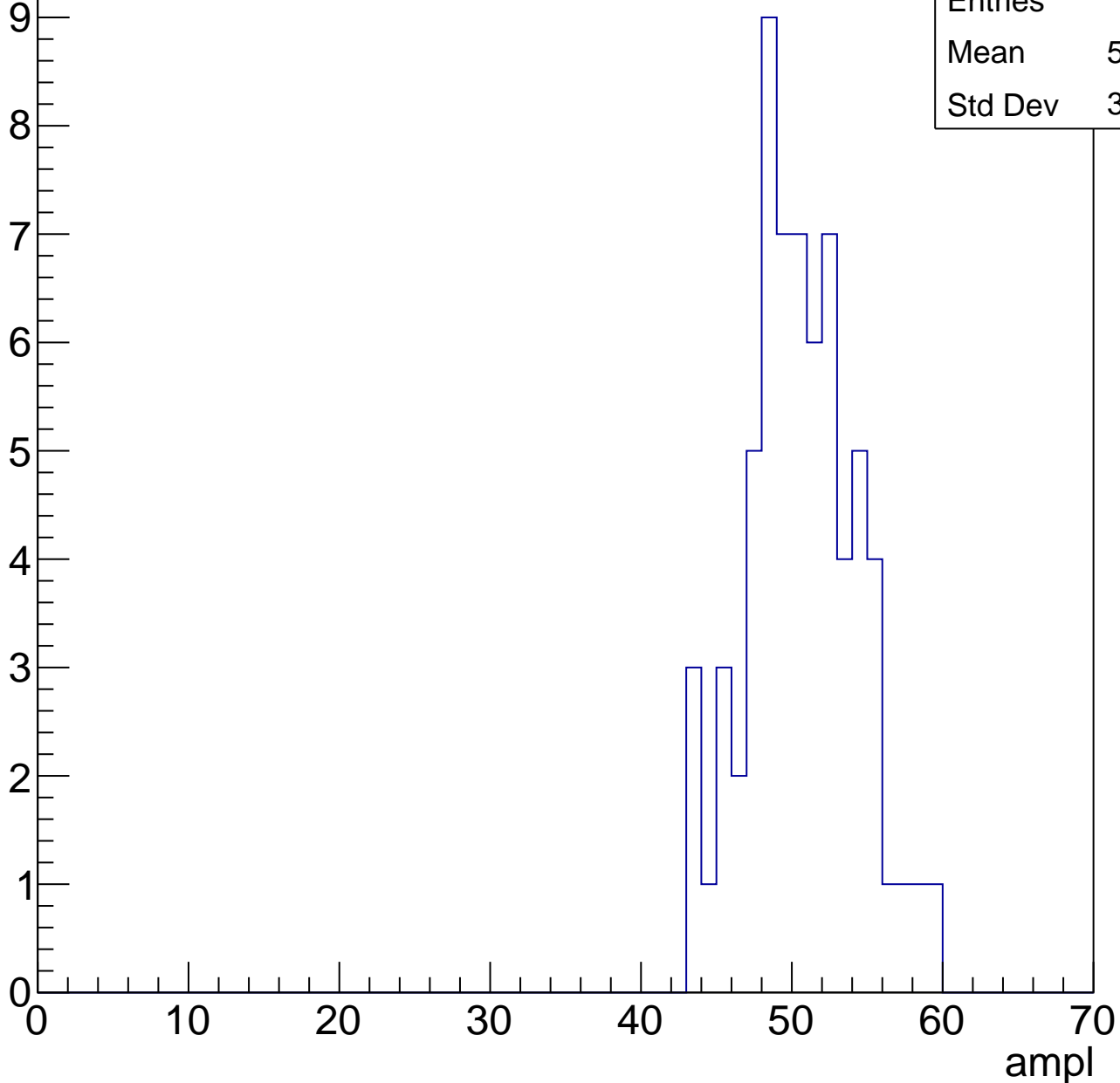


# B1L101S, U8-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	50.18
Std Dev	3.574

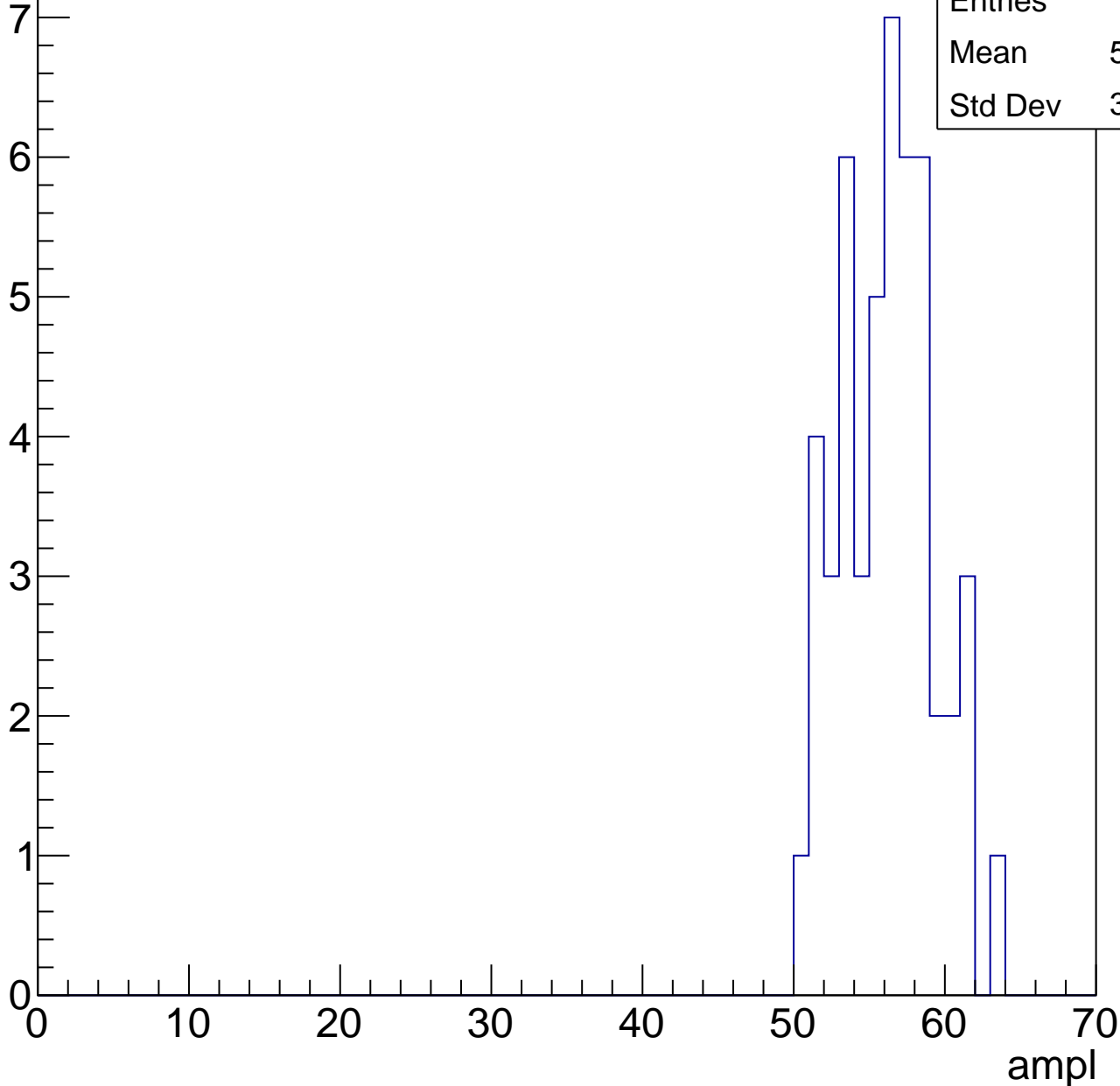


# B1L101S, U8-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	55.73
Std Dev	3.049

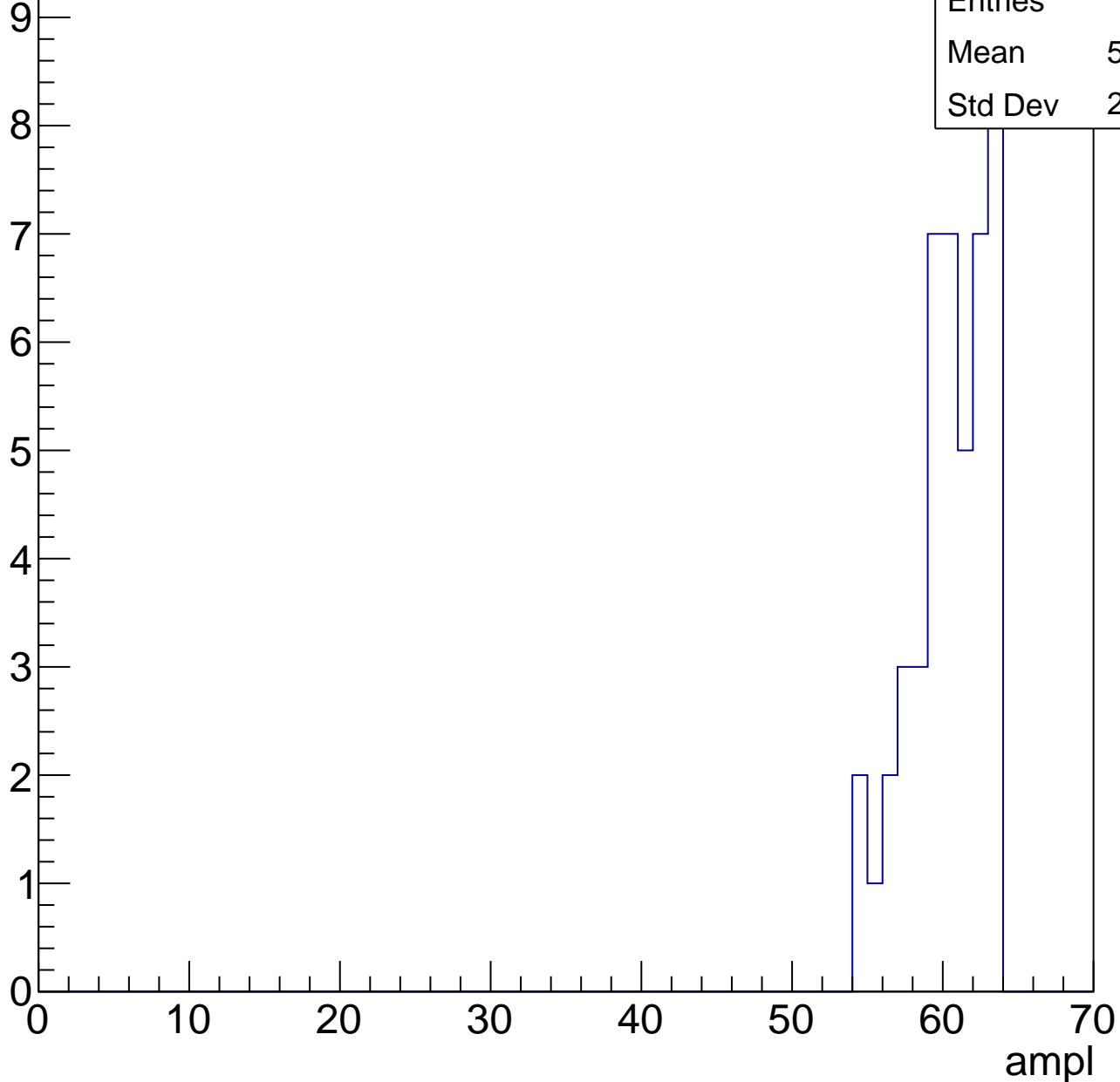


# B1L101S, U8-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

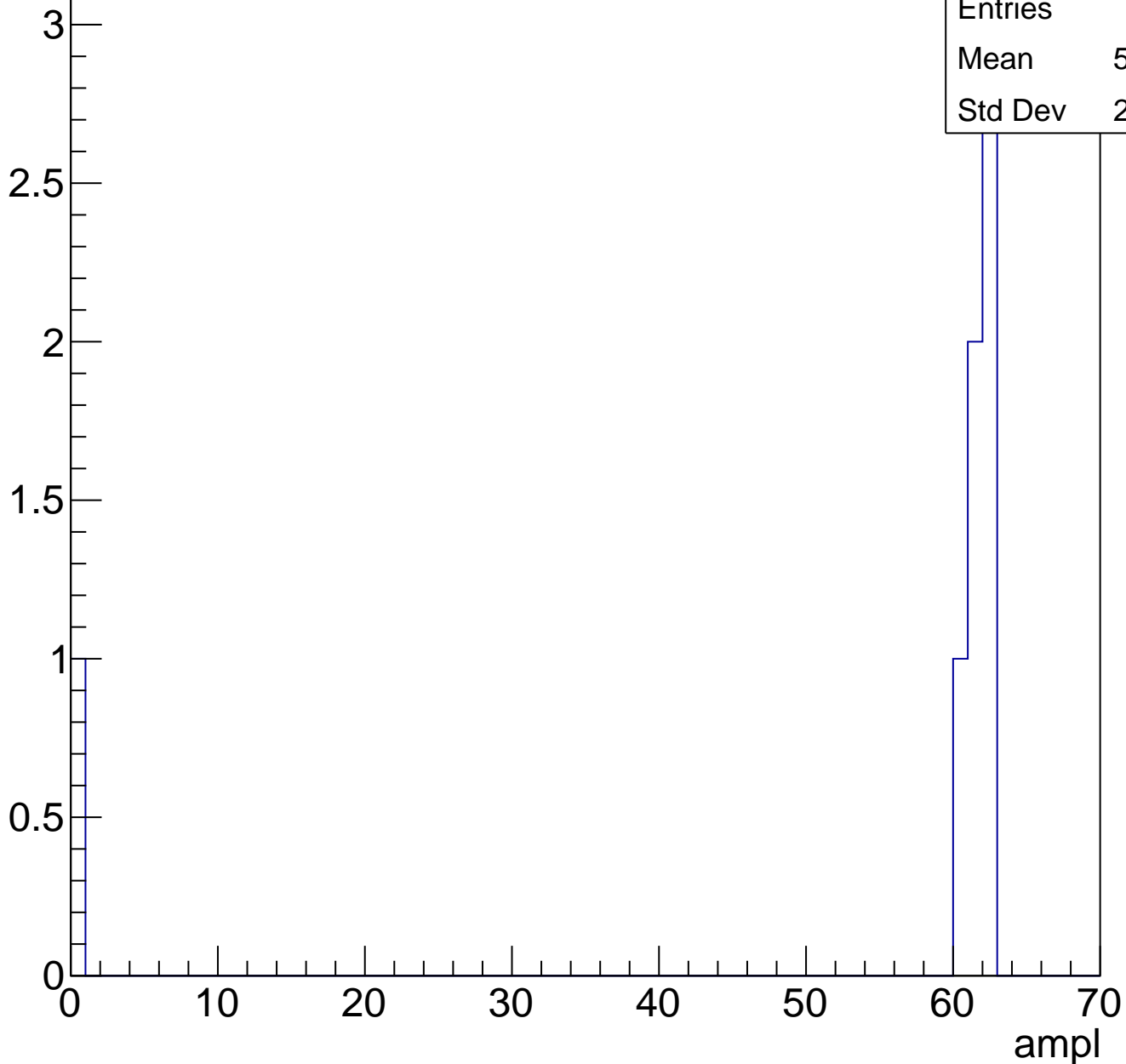
Entries	46
Mean	59.98
Std Dev	2.506



# B1L101S, U8-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U8-ch5, adc0

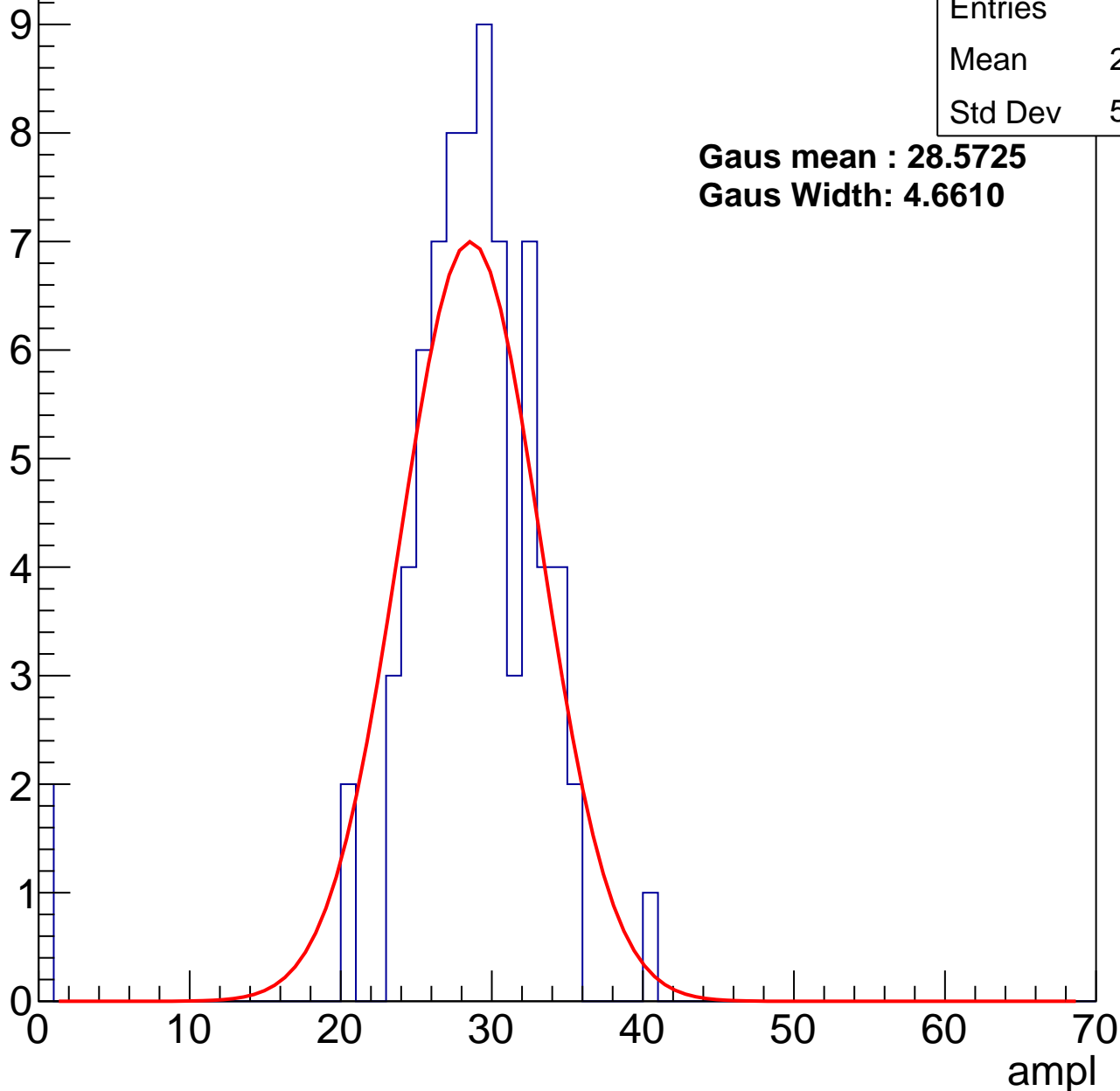
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	27.83
Std Dev	5.794

**Gaus mean : 28.5725**

**Gaus Width: 4.6610**



# B1L101S, U8-ch5, adc1

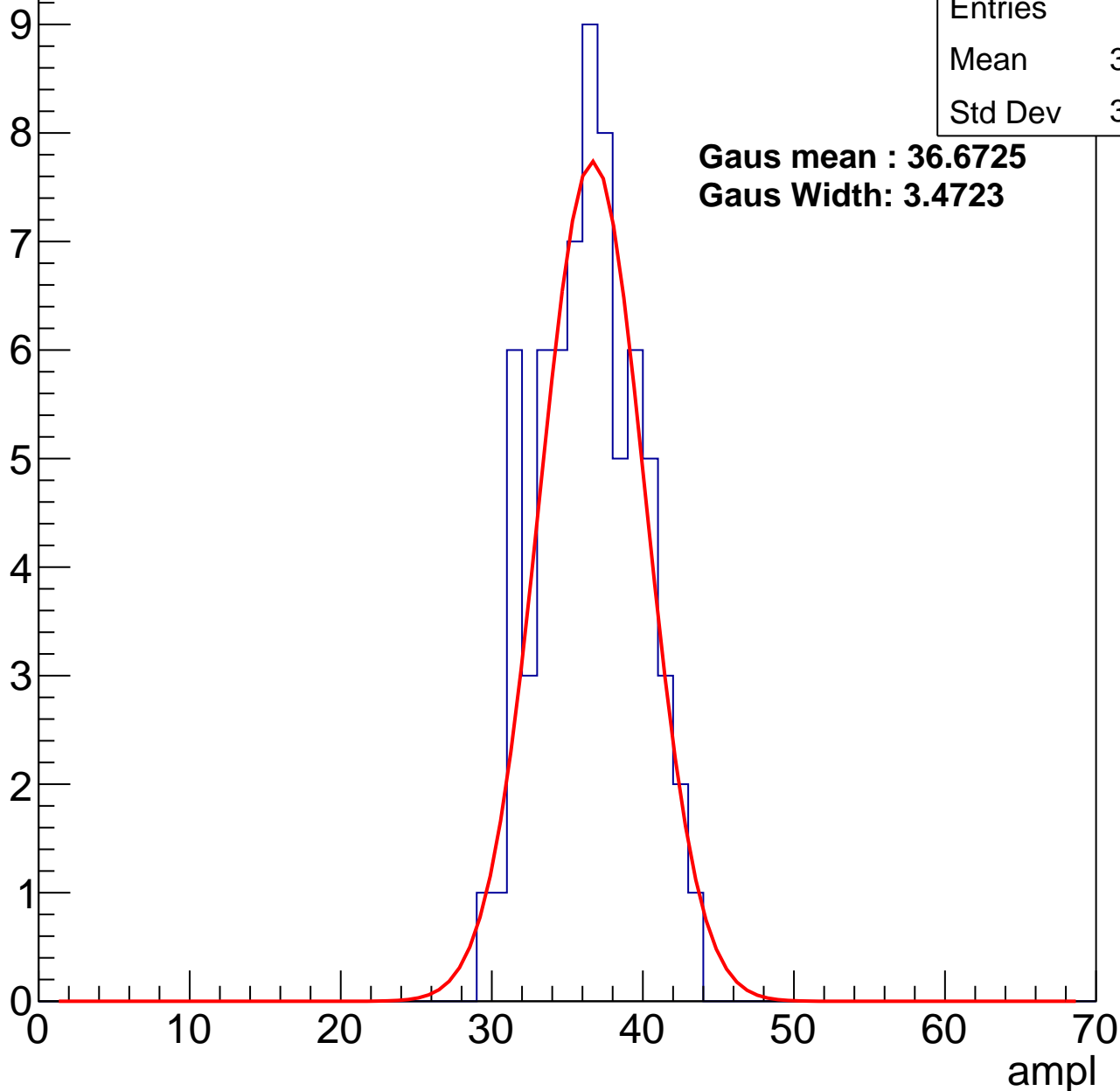
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	35.97
Std Dev	3.244

**Gaus mean : 36.6725**

**Gaus Width: 3.4723**



# B1L101S, U8-ch5, adc2

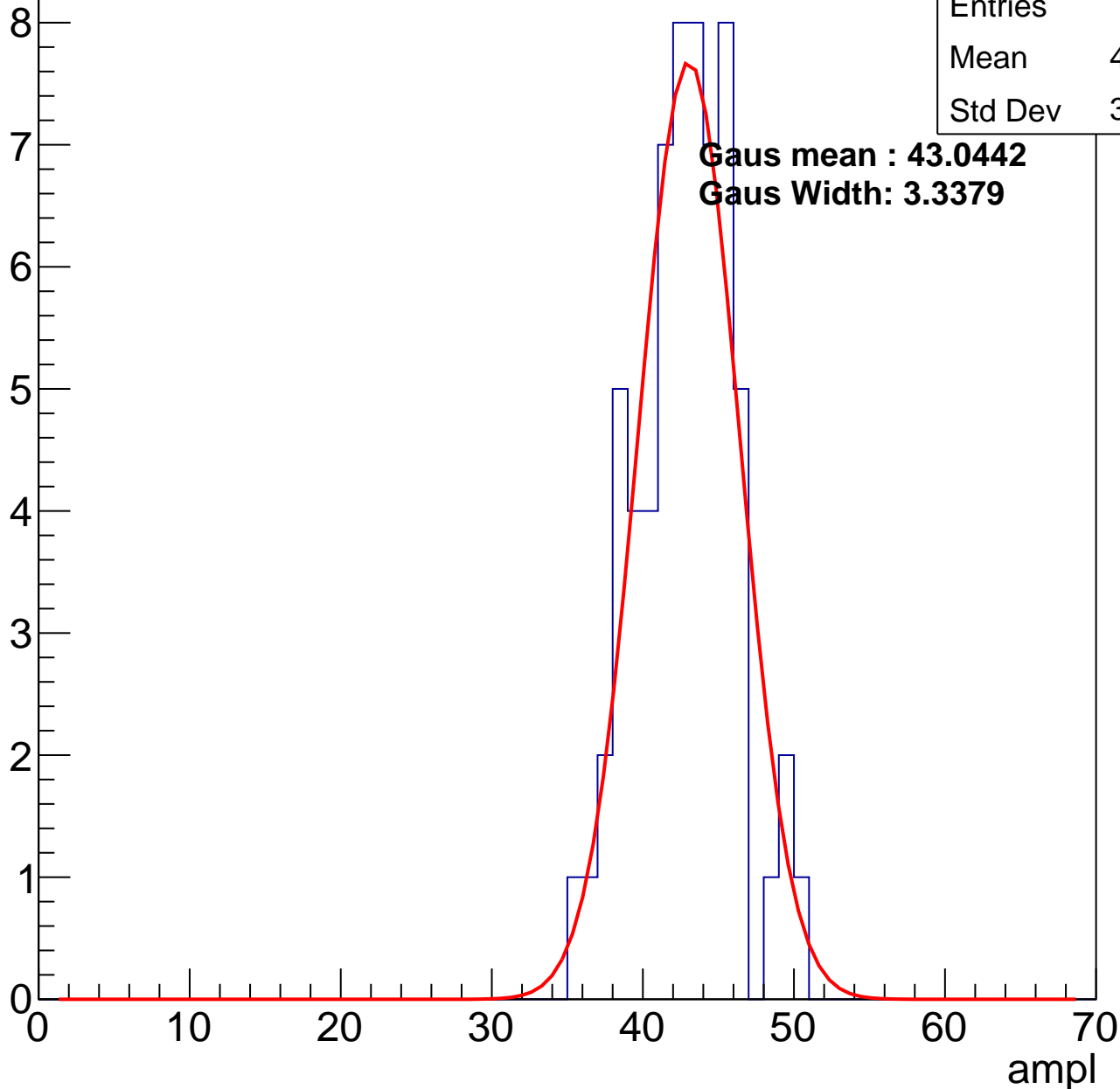
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	42.38
Std Dev	3.189

**Gaus mean : 43.0442**

**Gaus Width: 3.3379**

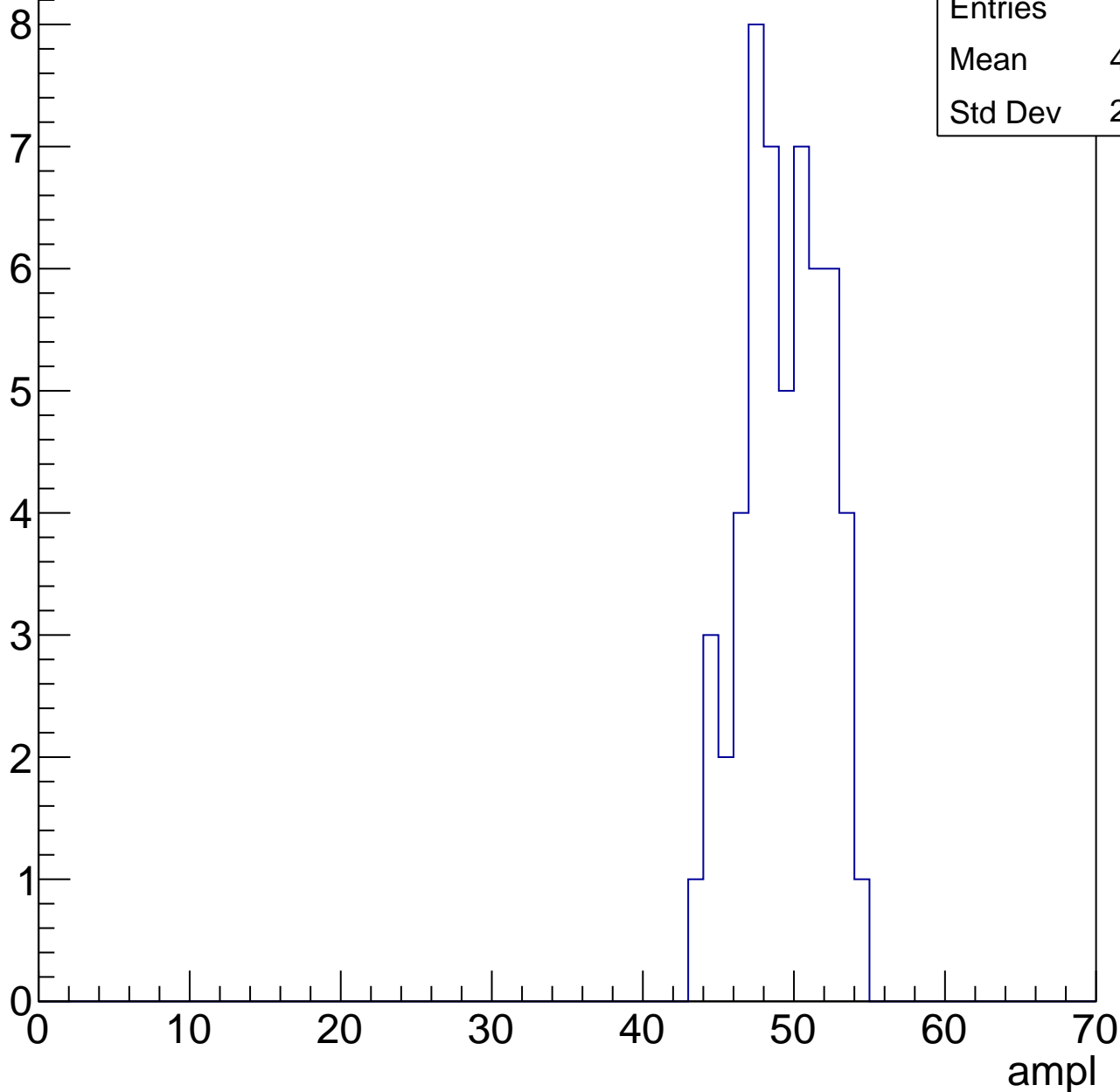


# B1L101S, U8-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	48.89
Std Dev	2.692

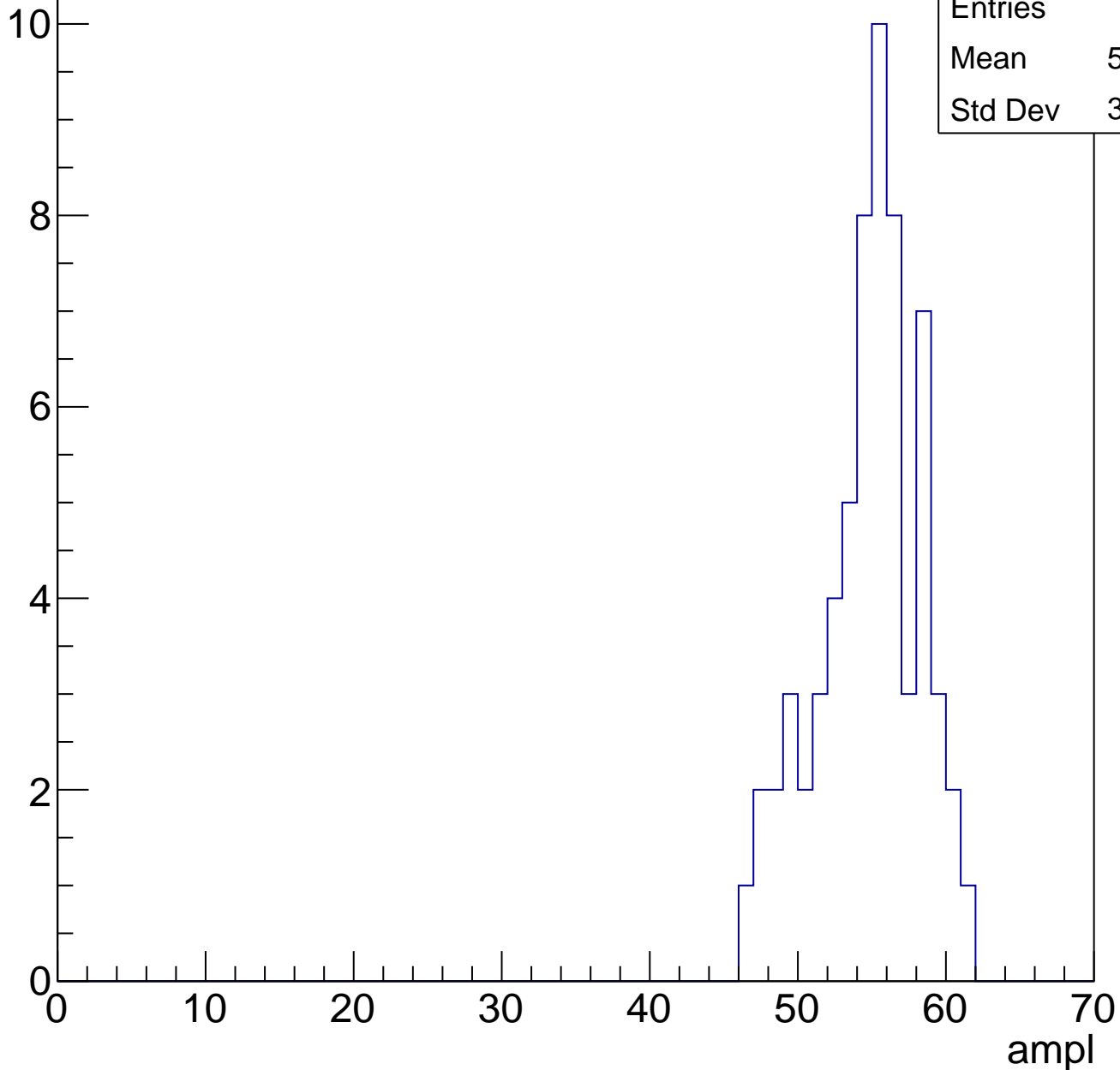


# B1L101S, U8-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	64
Mean	54.28
Std Dev	3.448

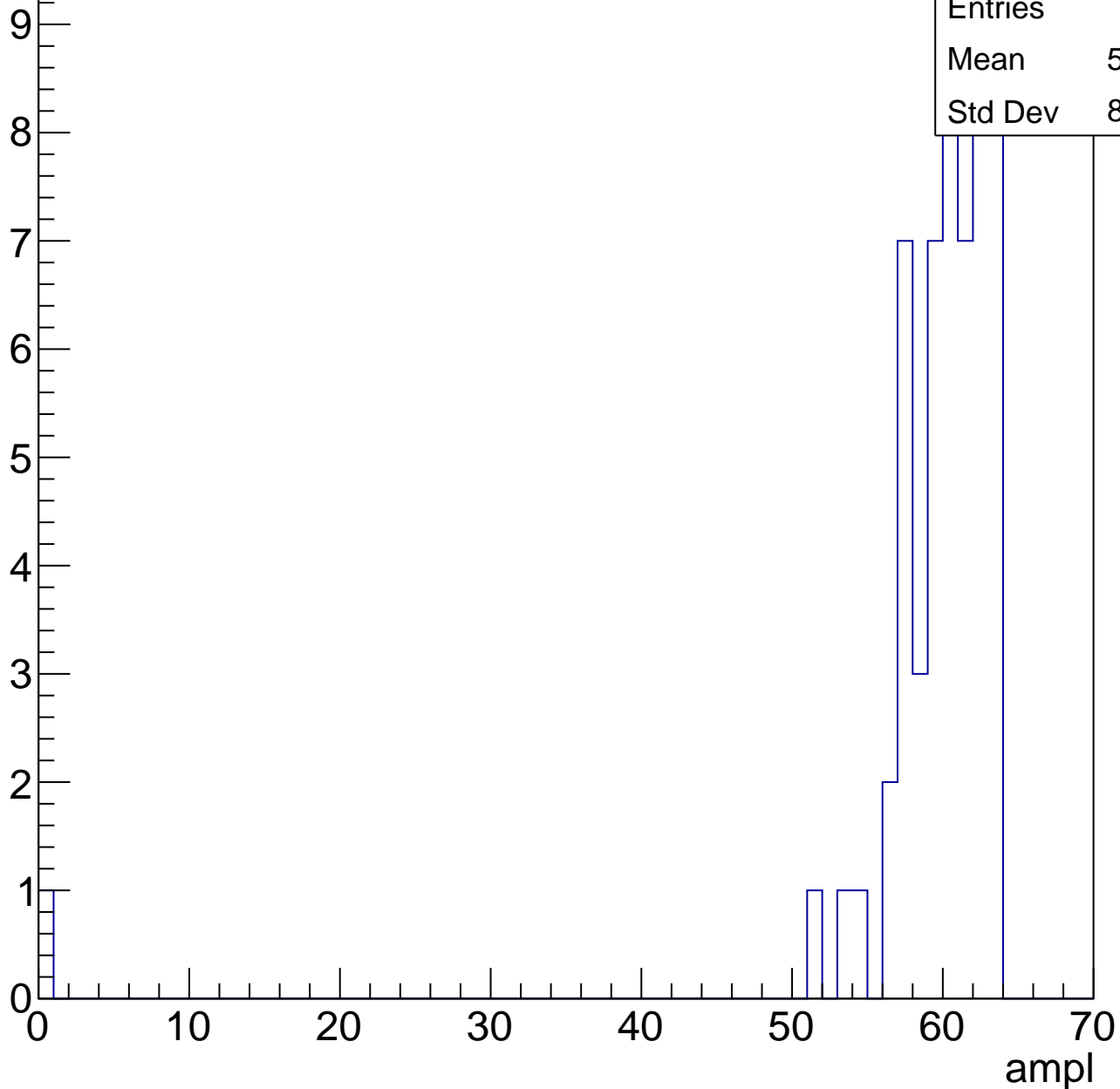
Entry



# B1L101S, U8-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

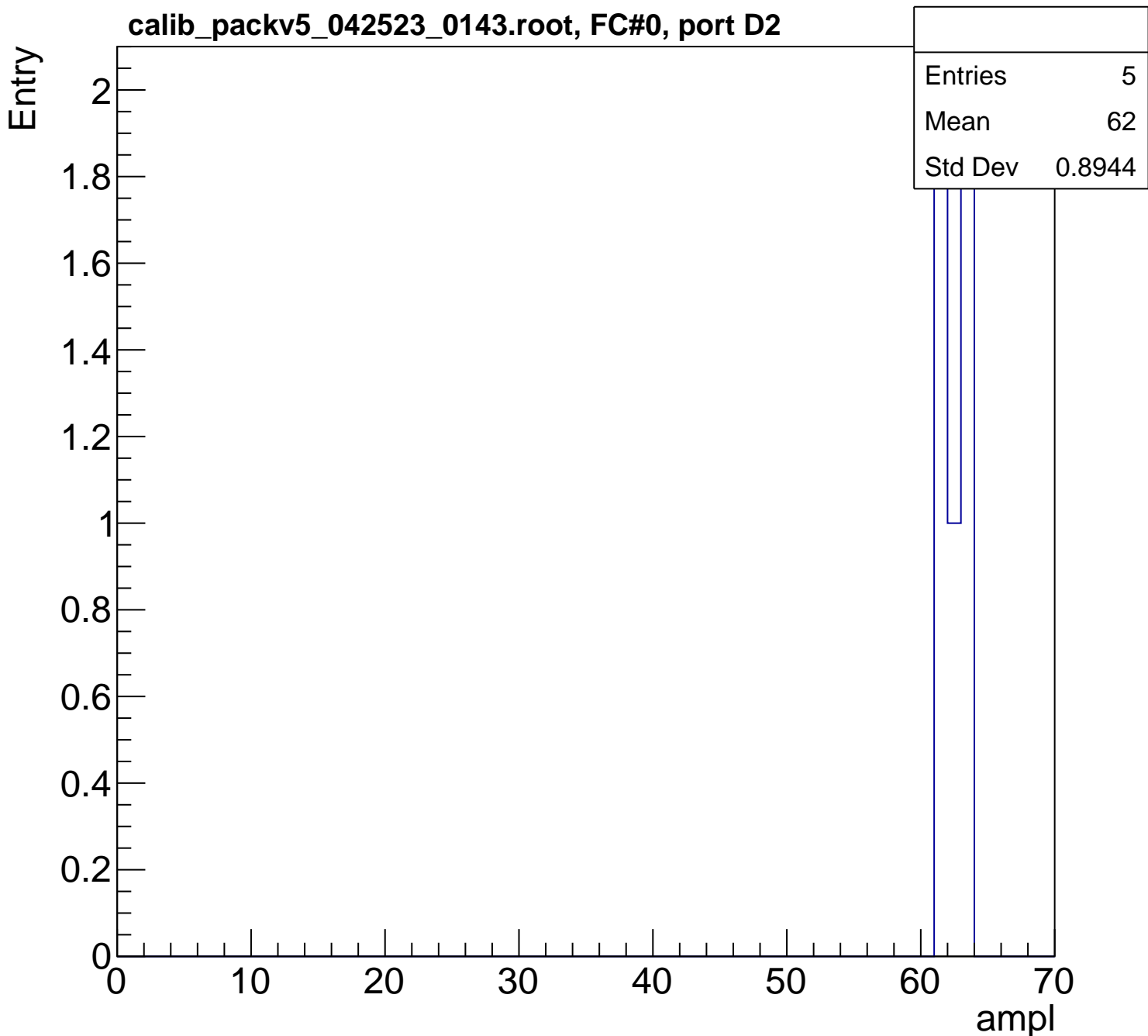
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	62
Std Dev	0.8944

0 10 20 30 40 50 60 70

ampl





# B1L101S, U8-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch6, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	65
Mean	27.92
Std Dev	6.016

**Gaus mean : 28.7792**

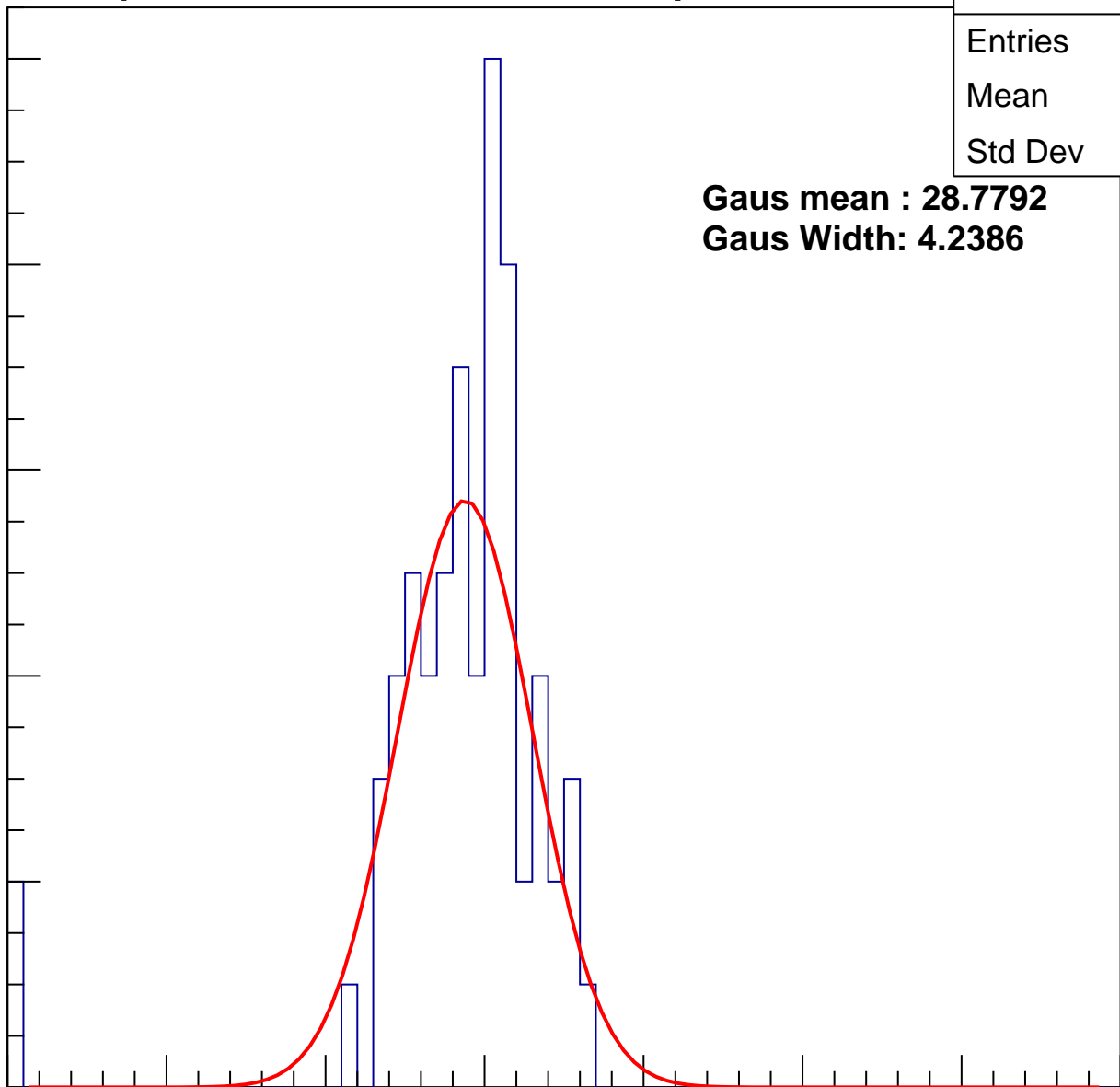
**Gaus Width: 4.2386**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



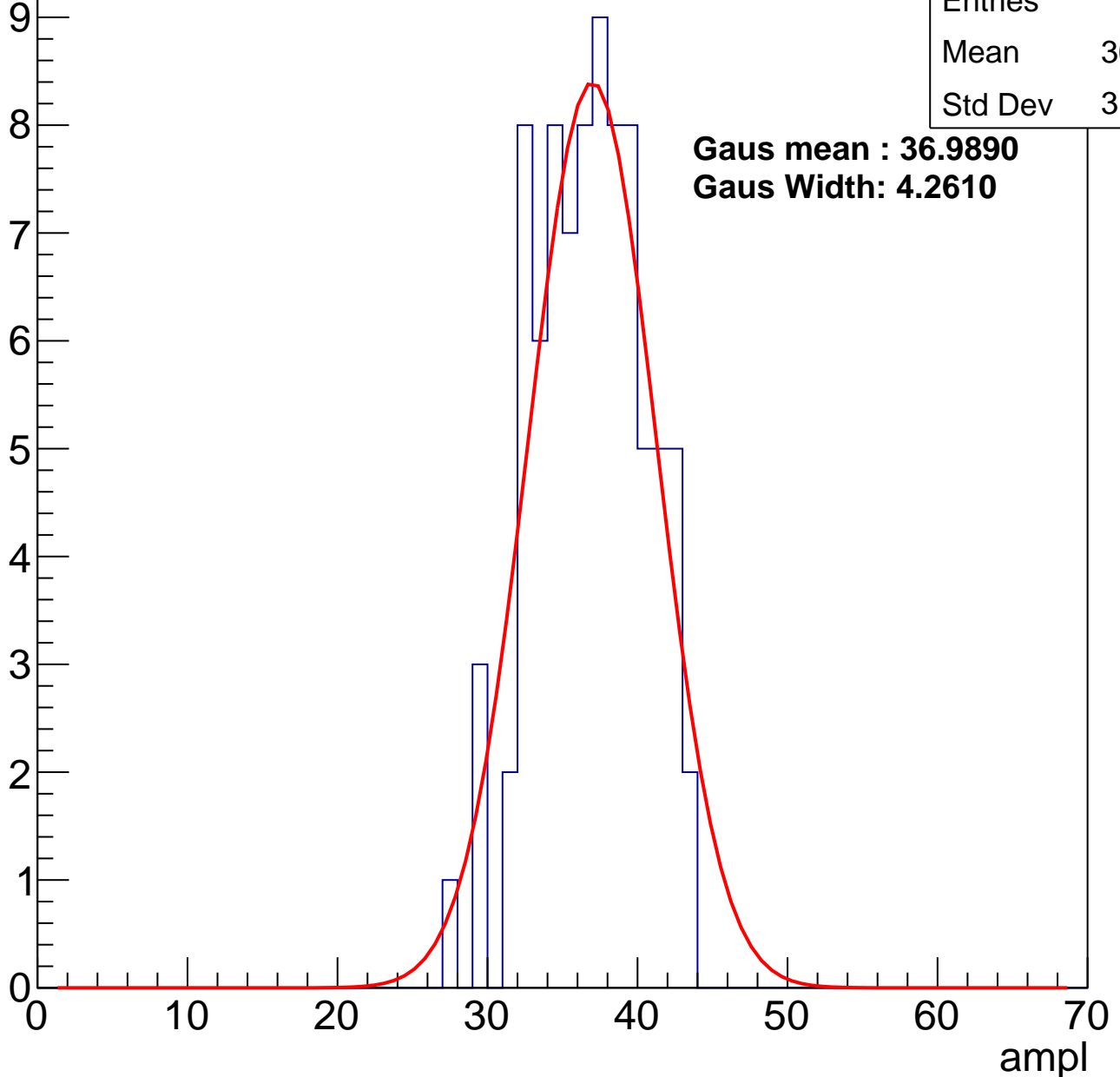
# B1L101S, U8-ch6, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	85
Mean	36.29
Std Dev	3.577

**Gaus mean : 36.9890**  
**Gaus Width: 4.2610**



# B1L101S, U8-ch6, adc2

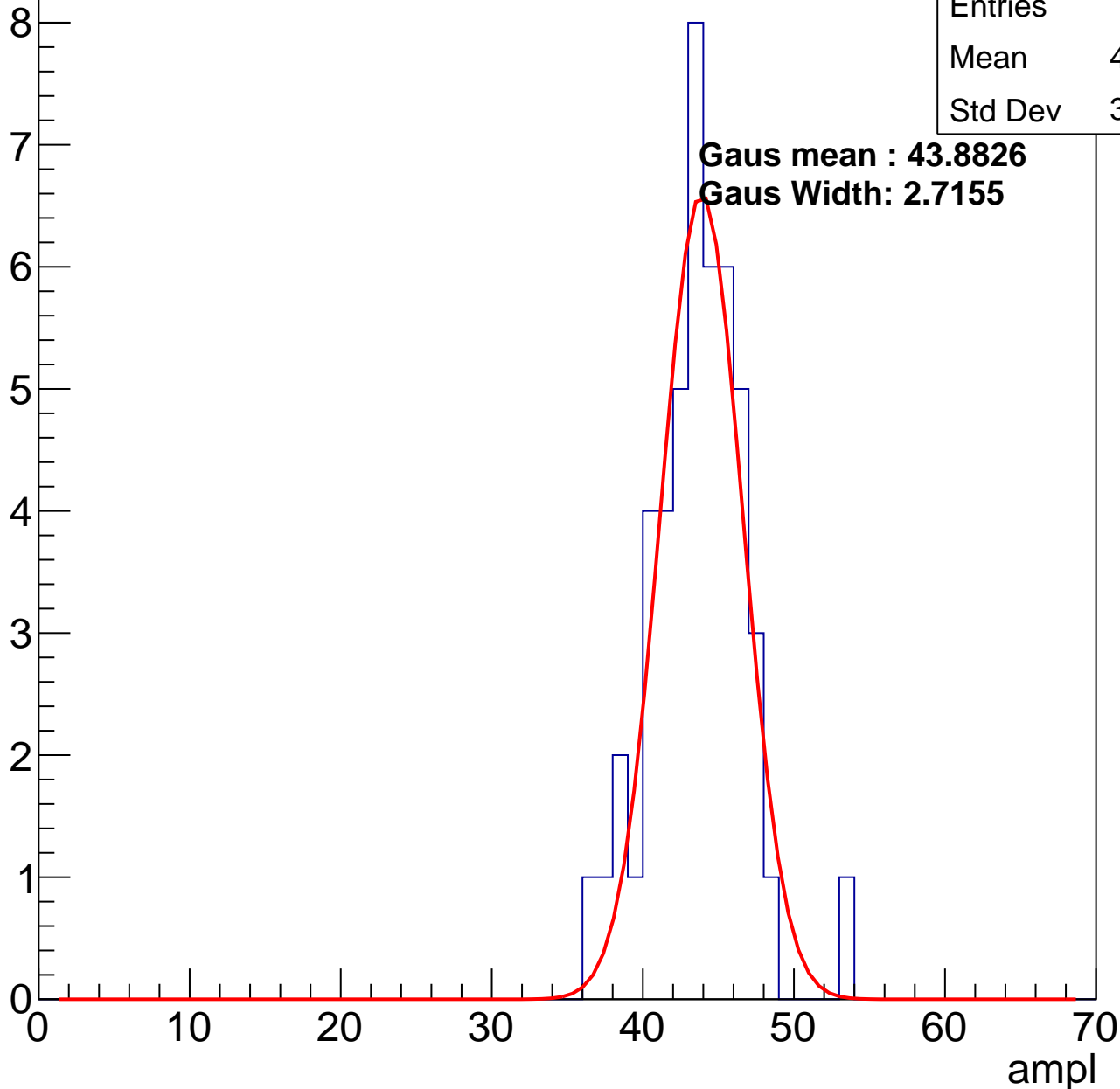
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	43.17
Std Dev	3.078

**Gaus mean : 43.8826**

**Gaus Width: 2.7155**



# B1L101S, U8-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

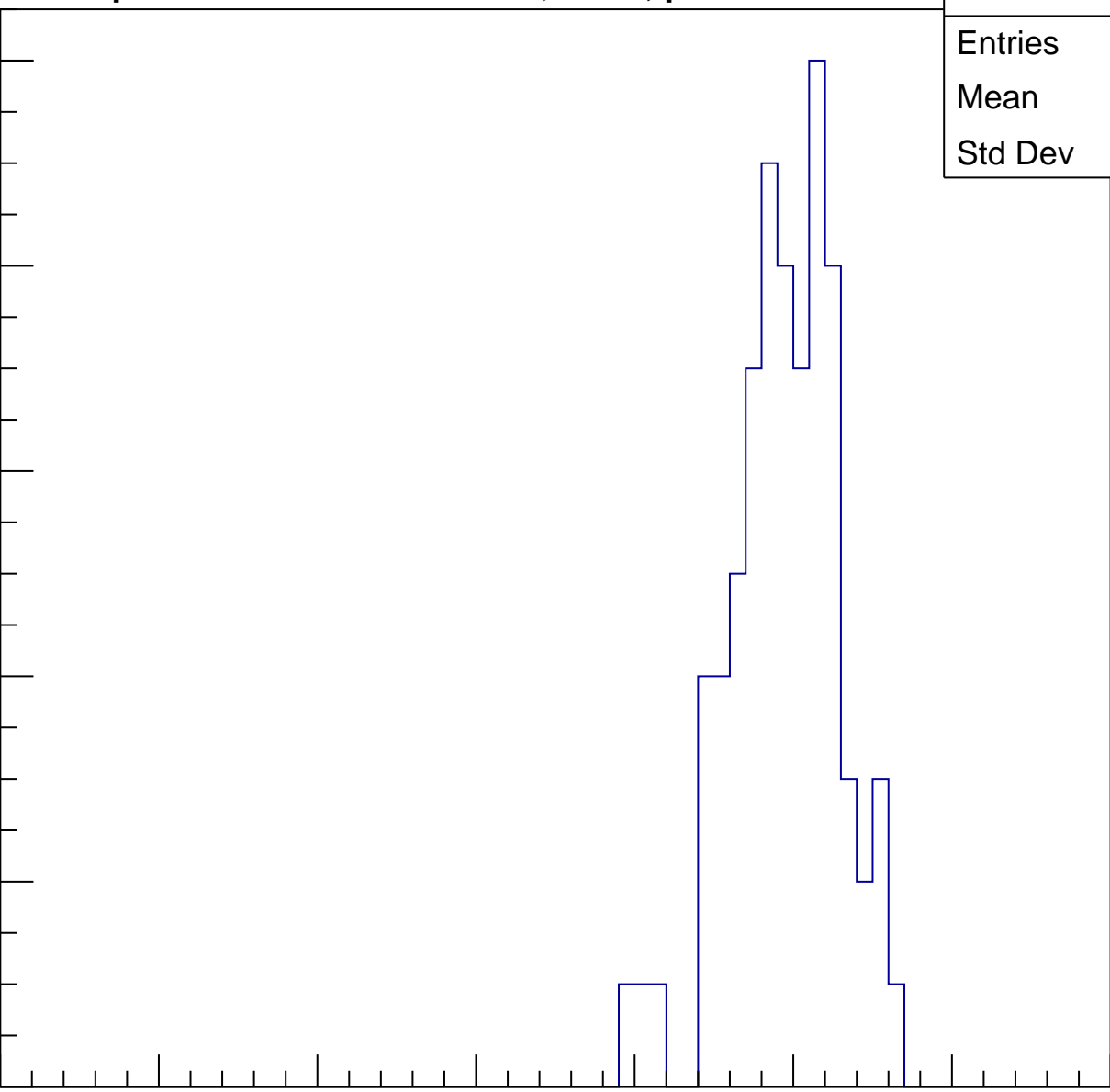
Entries	74
Mean	48.96
Std Dev	3.419

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

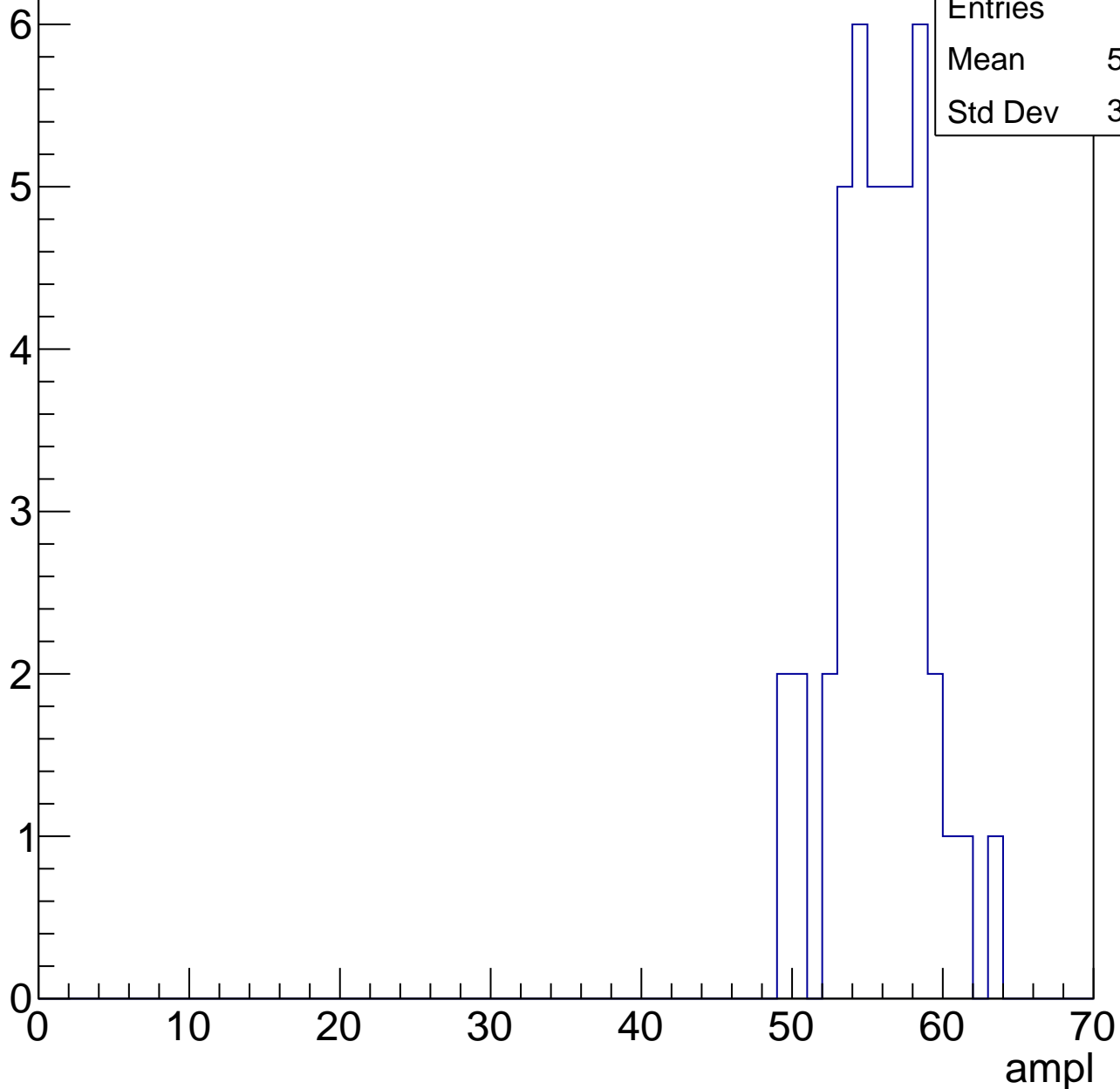


# B1L101S, U8-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	55.37
Std Dev	3.035

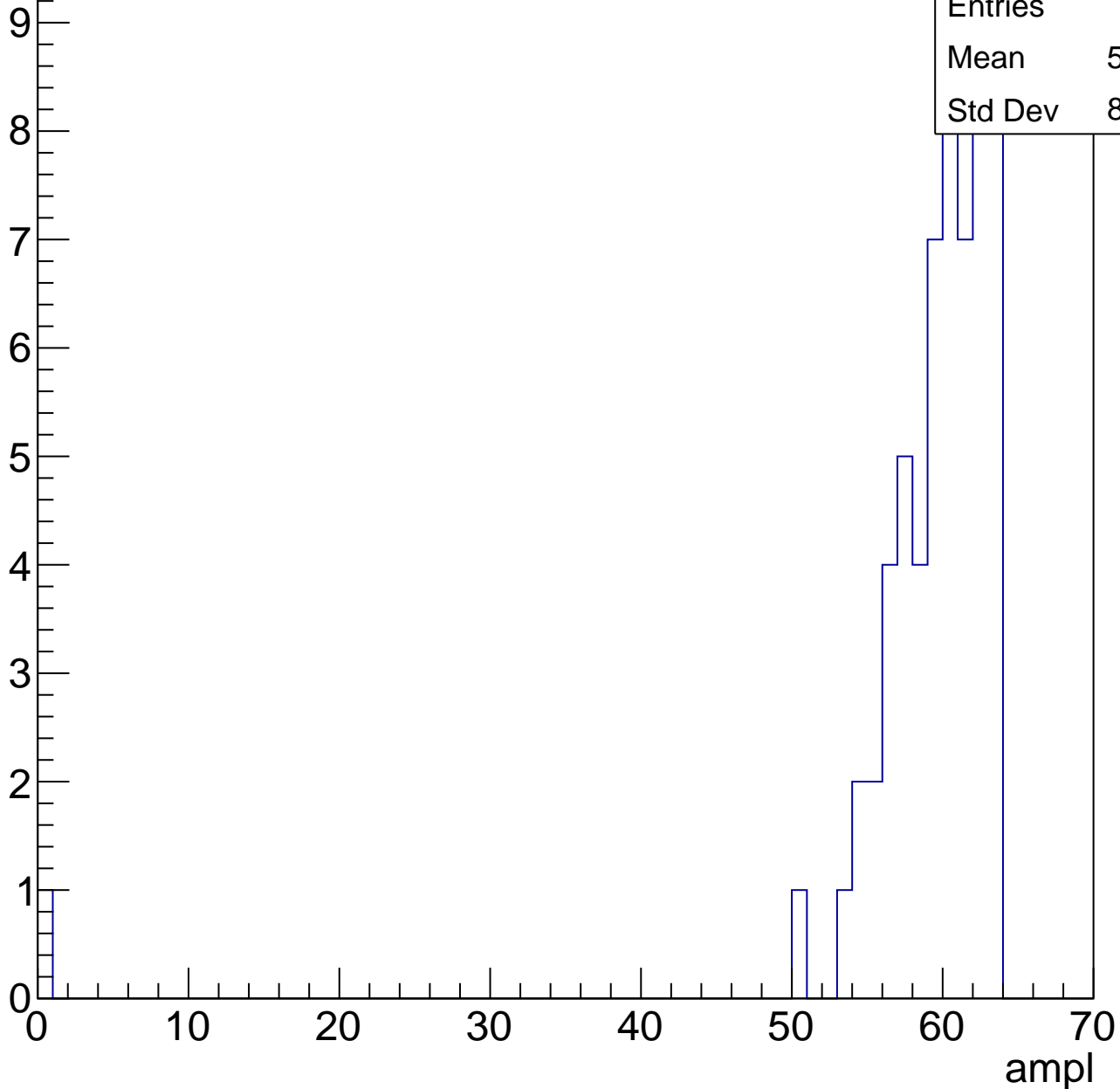


# B1L101S, U8-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

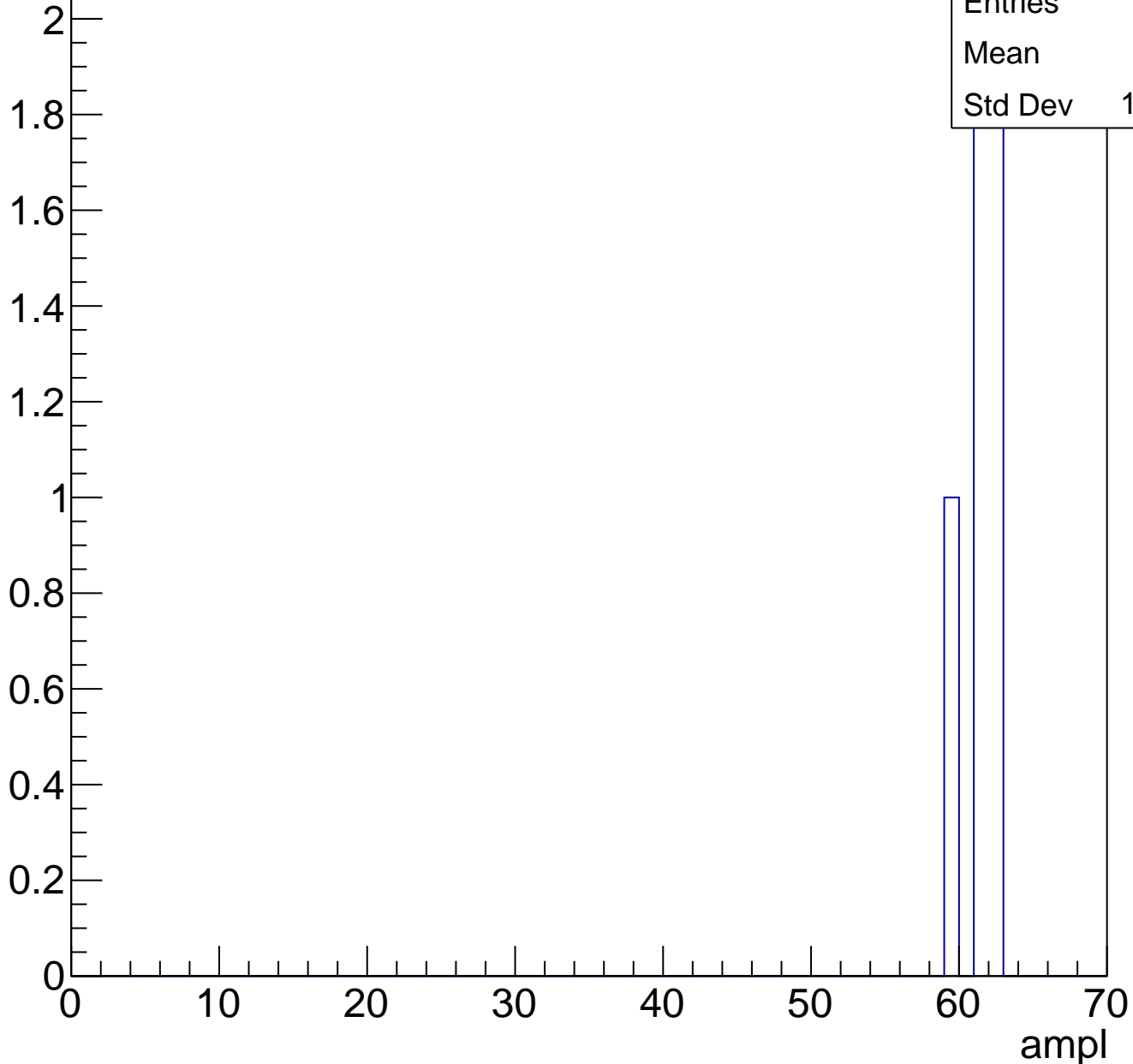
Entries	60
Mean	58.42
Std Dev	8.137



# B1L101S, U8-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U8-ch7, adc0

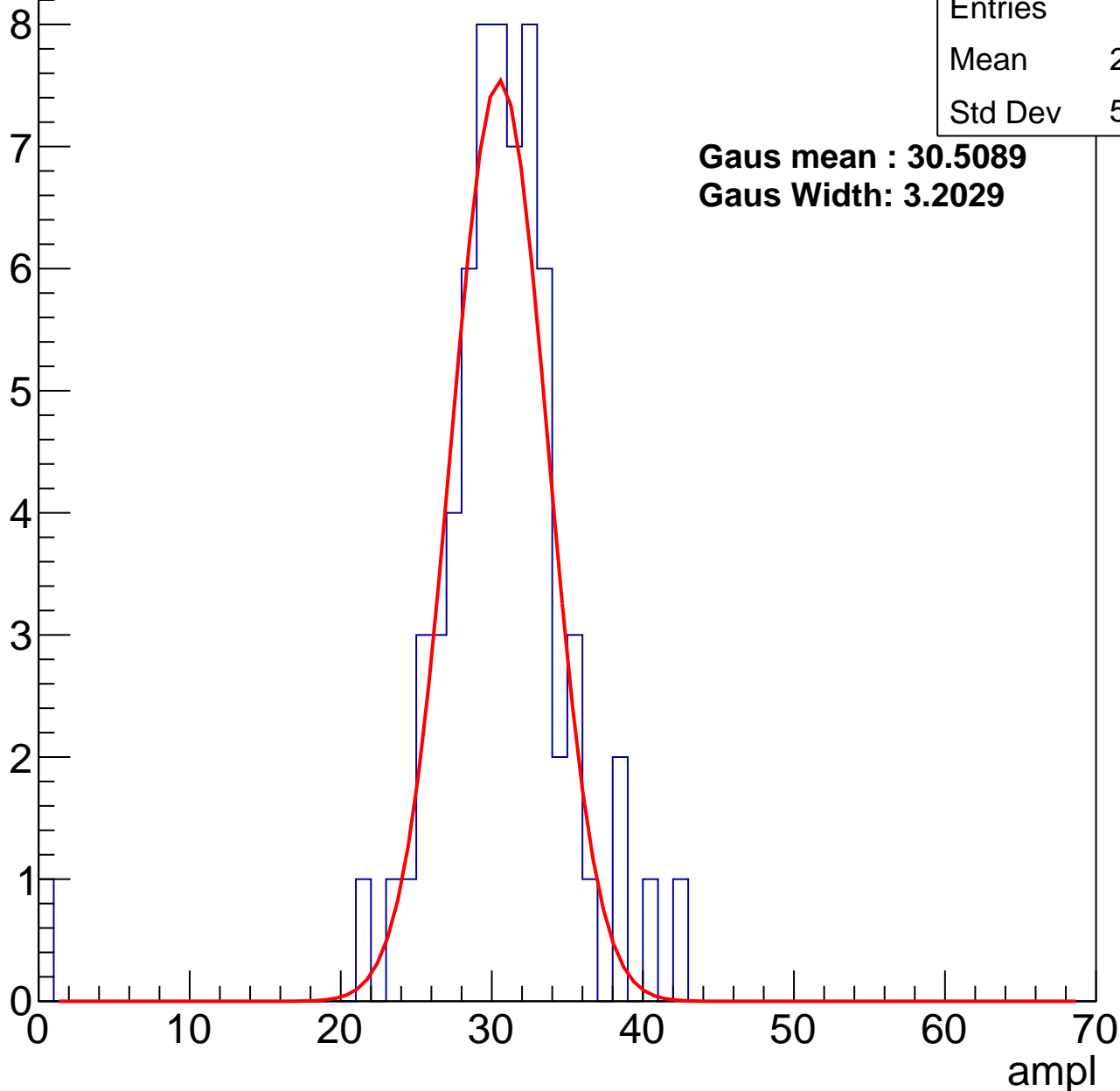
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	29.96
Std Dev	5.276

**Gaus mean : 30.5089**

**Gaus Width: 3.2029**

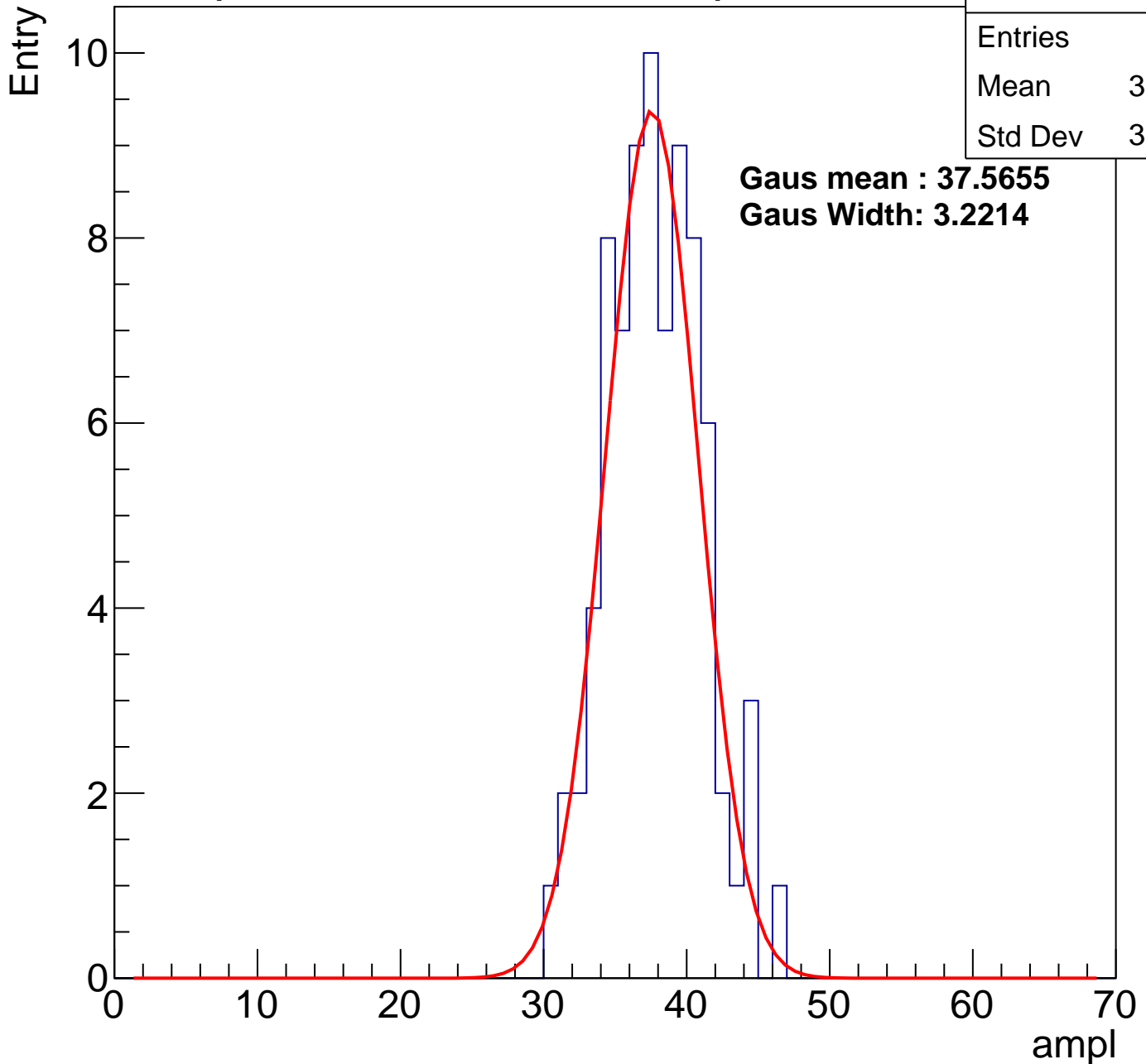


# B1L101S, U8-ch7, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	80
Mean	37.34
Std Dev	3.279

**Gaus mean : 37.5655**  
**Gaus Width: 3.2214**



# B1L101S, U8-ch7, adc2

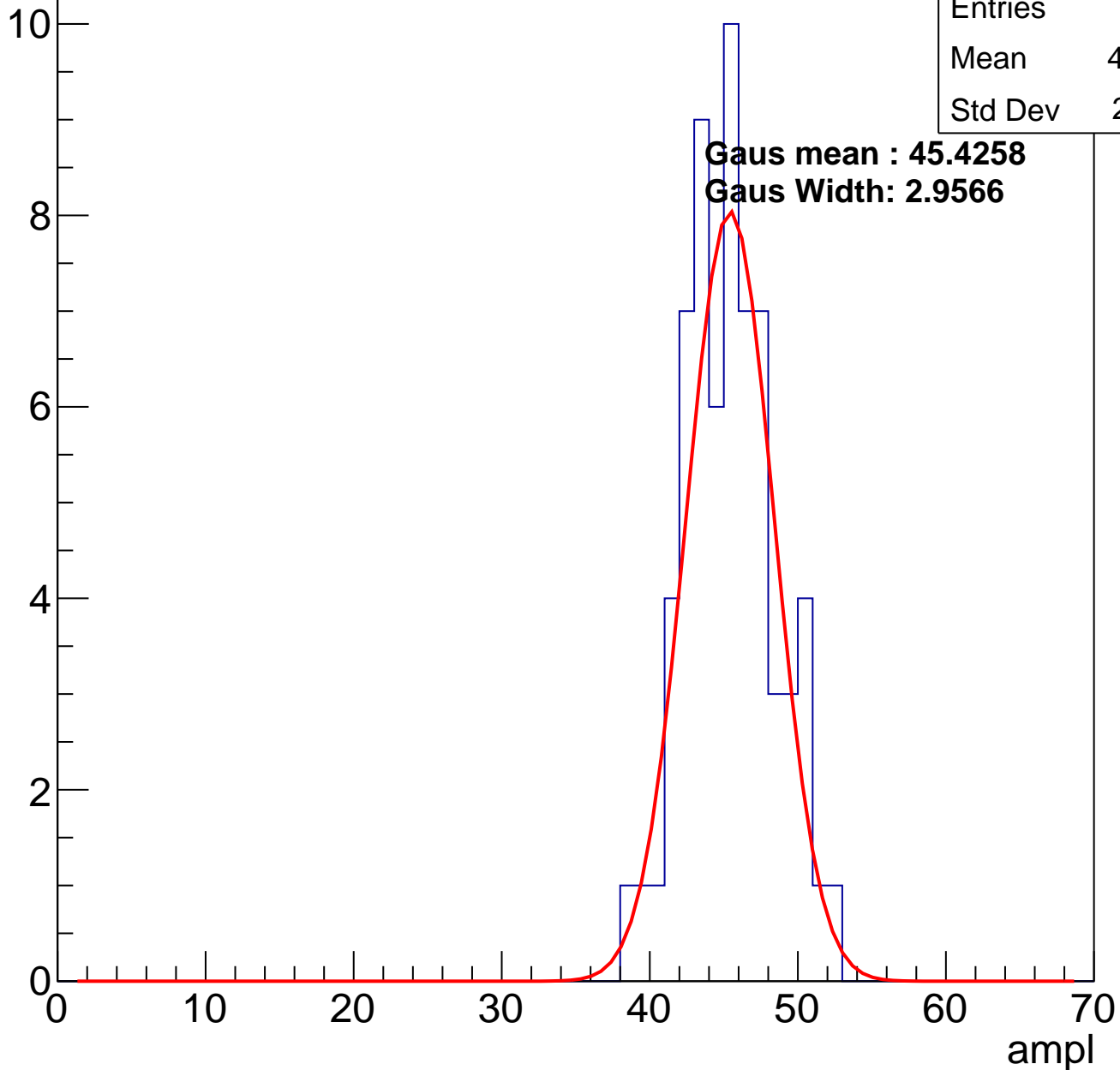
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	65
Mean	44.94
Std Dev	2.971

**Gaus mean : 45.4258**

**Gaus Width: 2.9566**

Entry

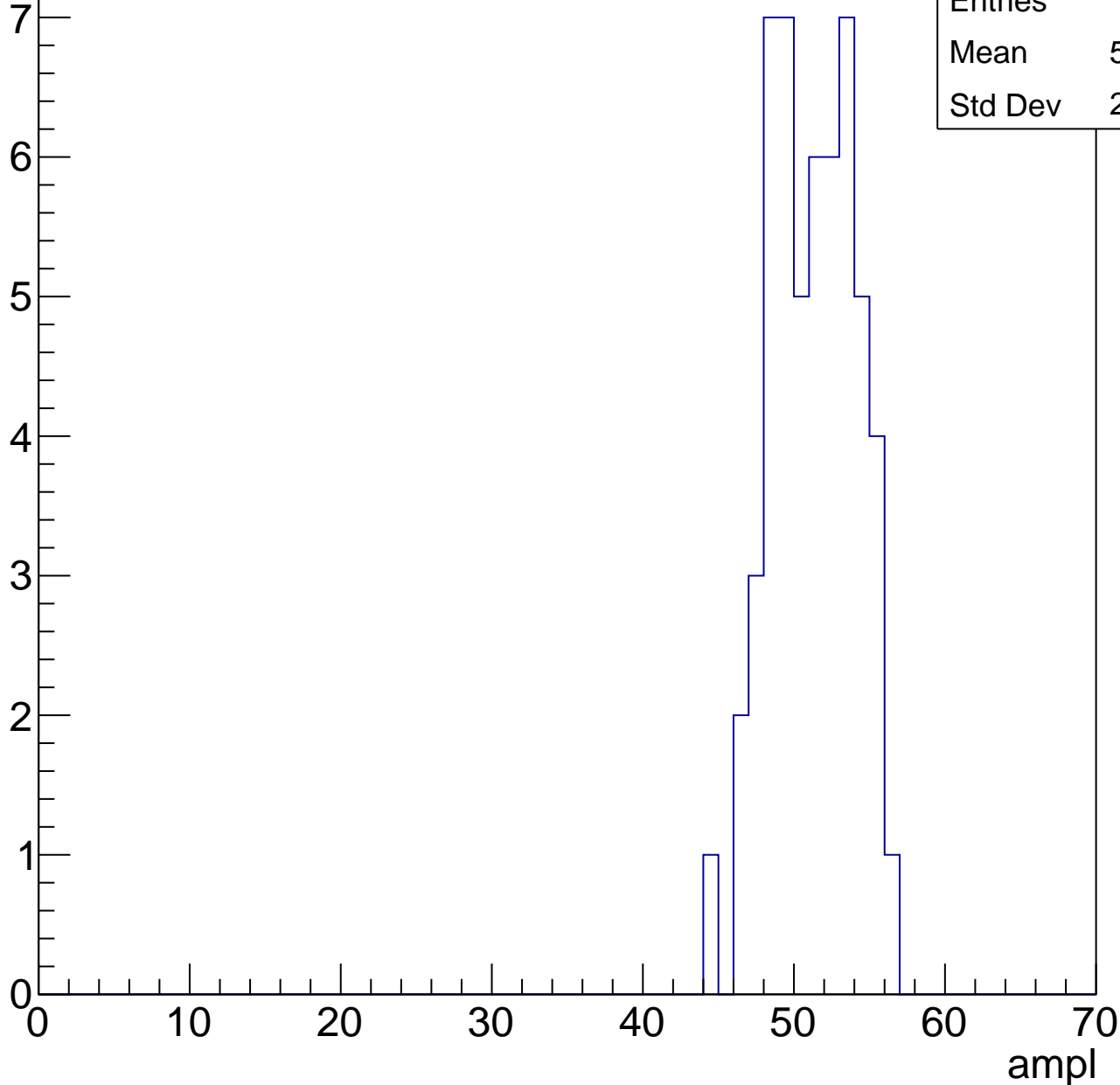


# B1L101S, U8-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	50.76
Std Dev	2.748

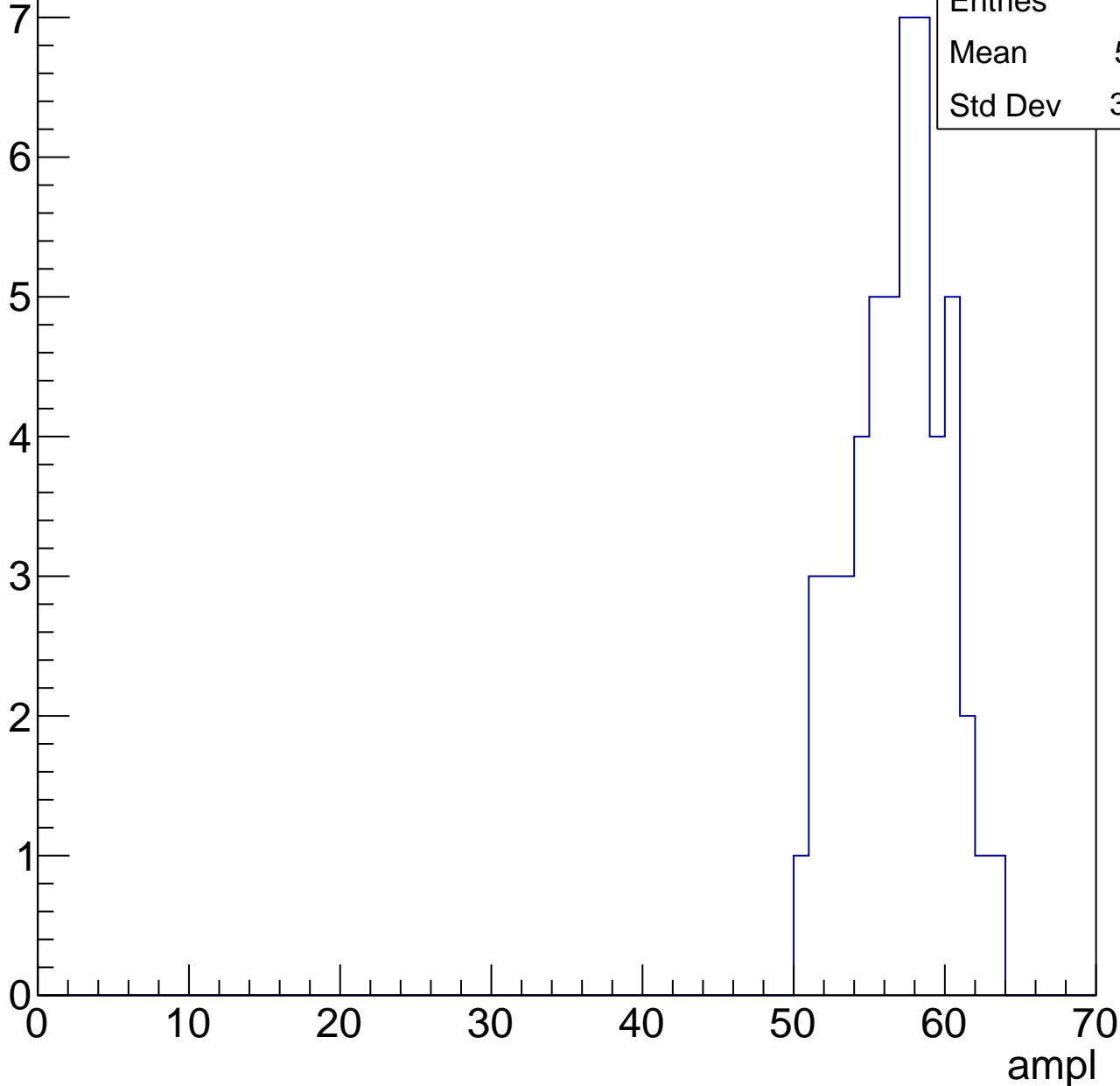


# B1L101S, U8-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	56.41
Std Dev	3.082

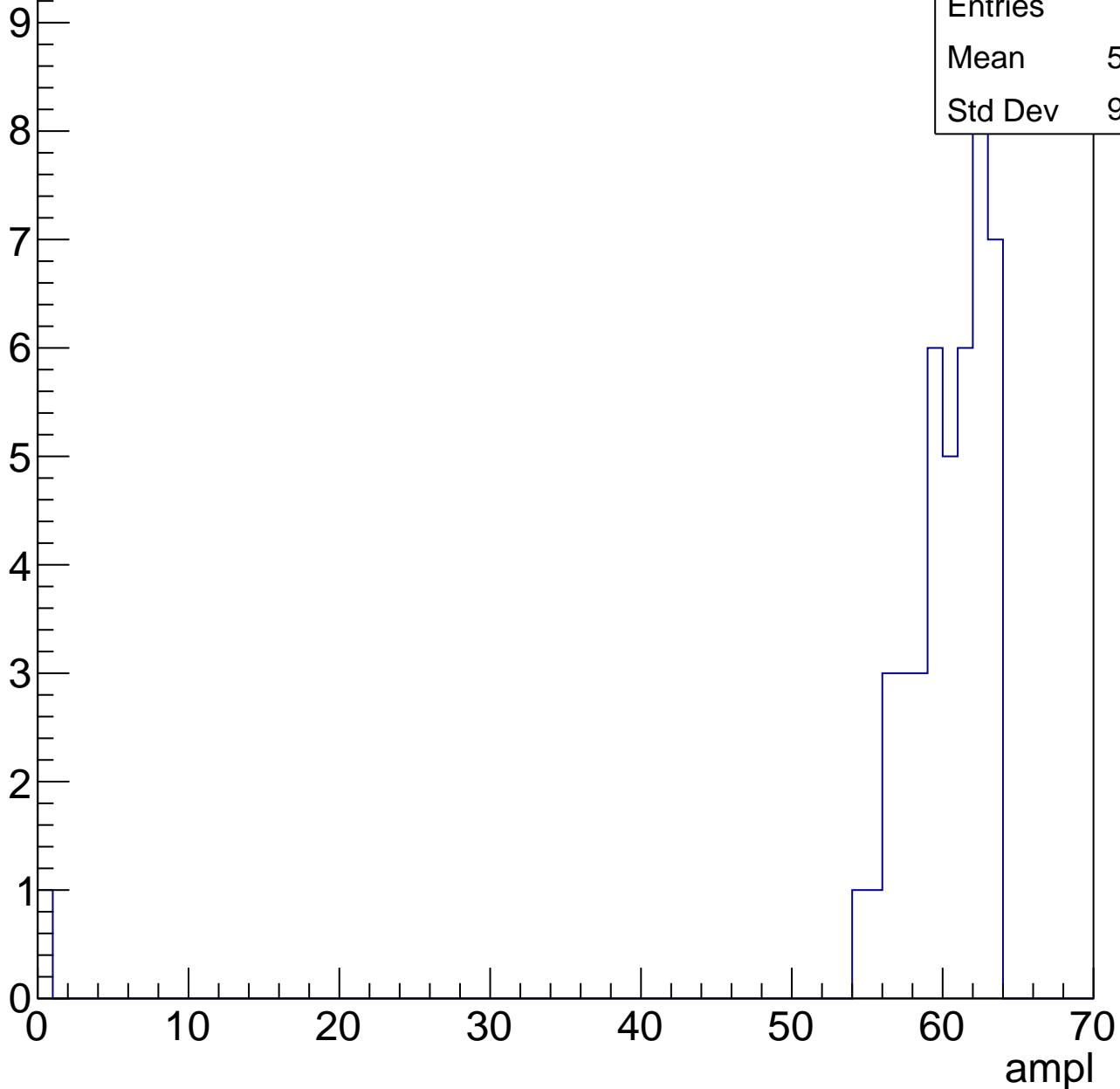


# B1L101S, U8-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

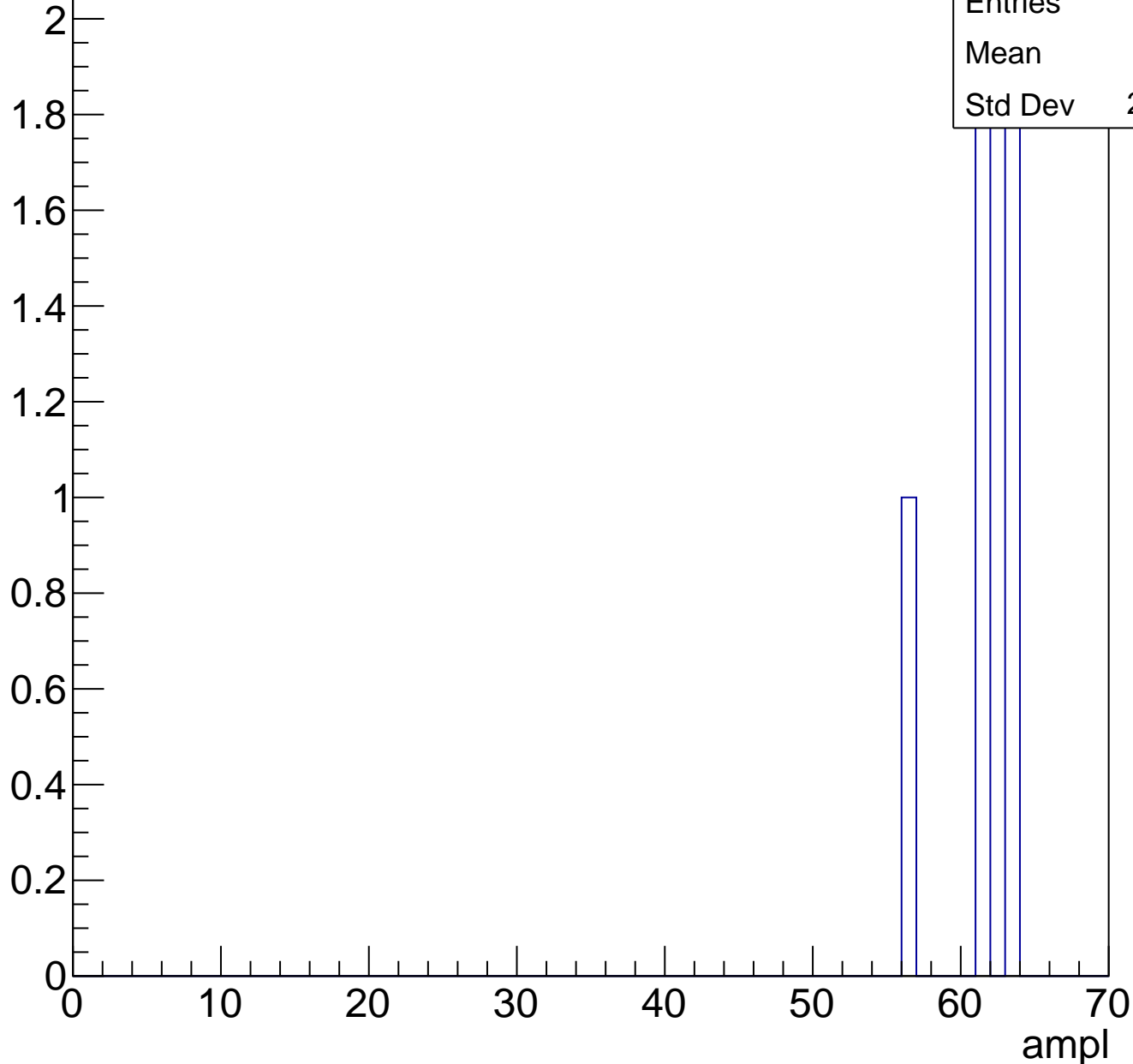
Entries	45
Mean	58.69
Std Dev	9.167



# B1L101S, U8-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U8-ch8, adc0

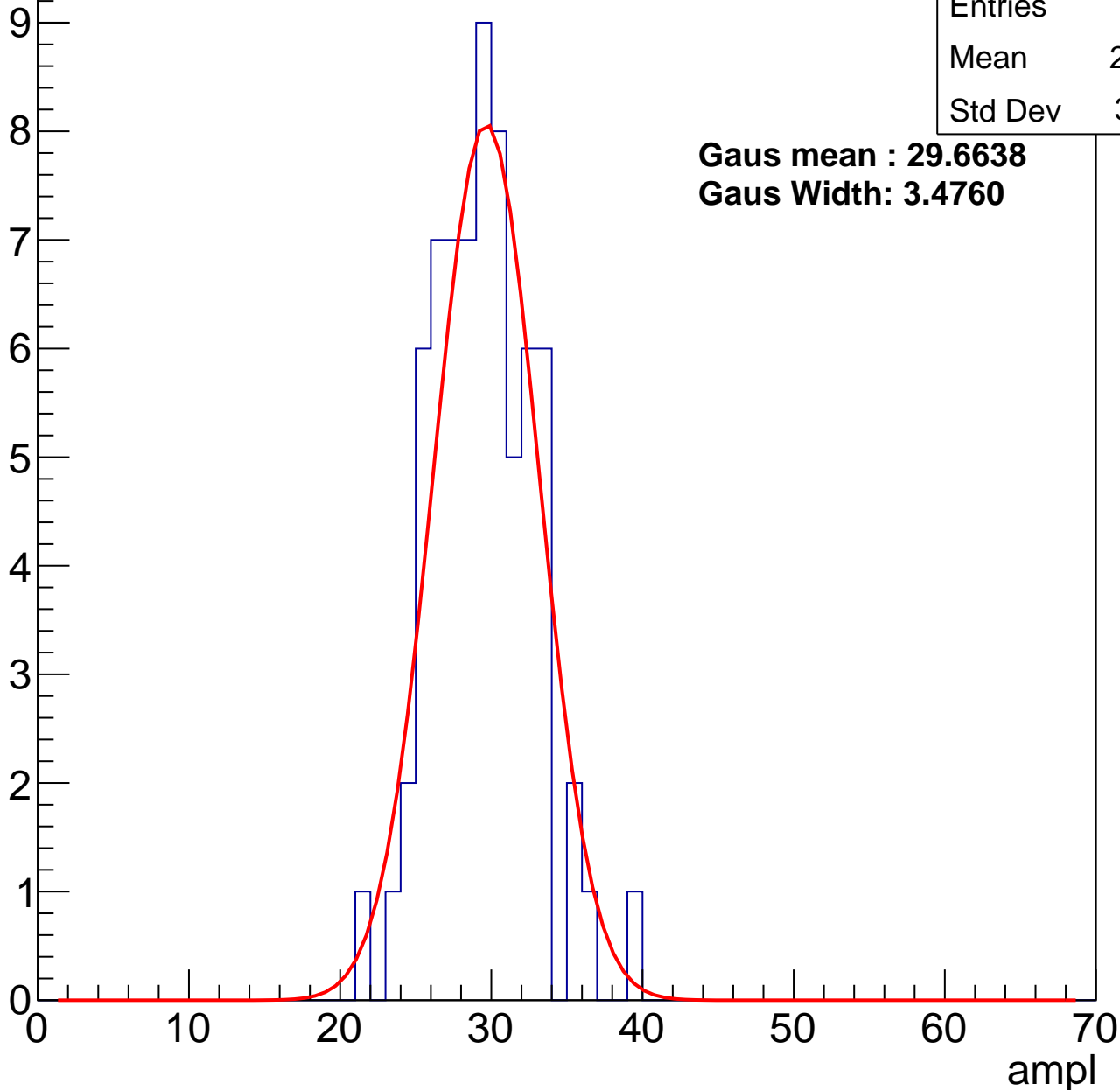
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	28.99
Std Dev	3.281

**Gaus mean : 29.6638**

**Gaus Width: 3.4760**



# B1L101S, U8-ch8, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	67
Mean	35.76
Std Dev	2.968

**Gaus mean : 36.3558**

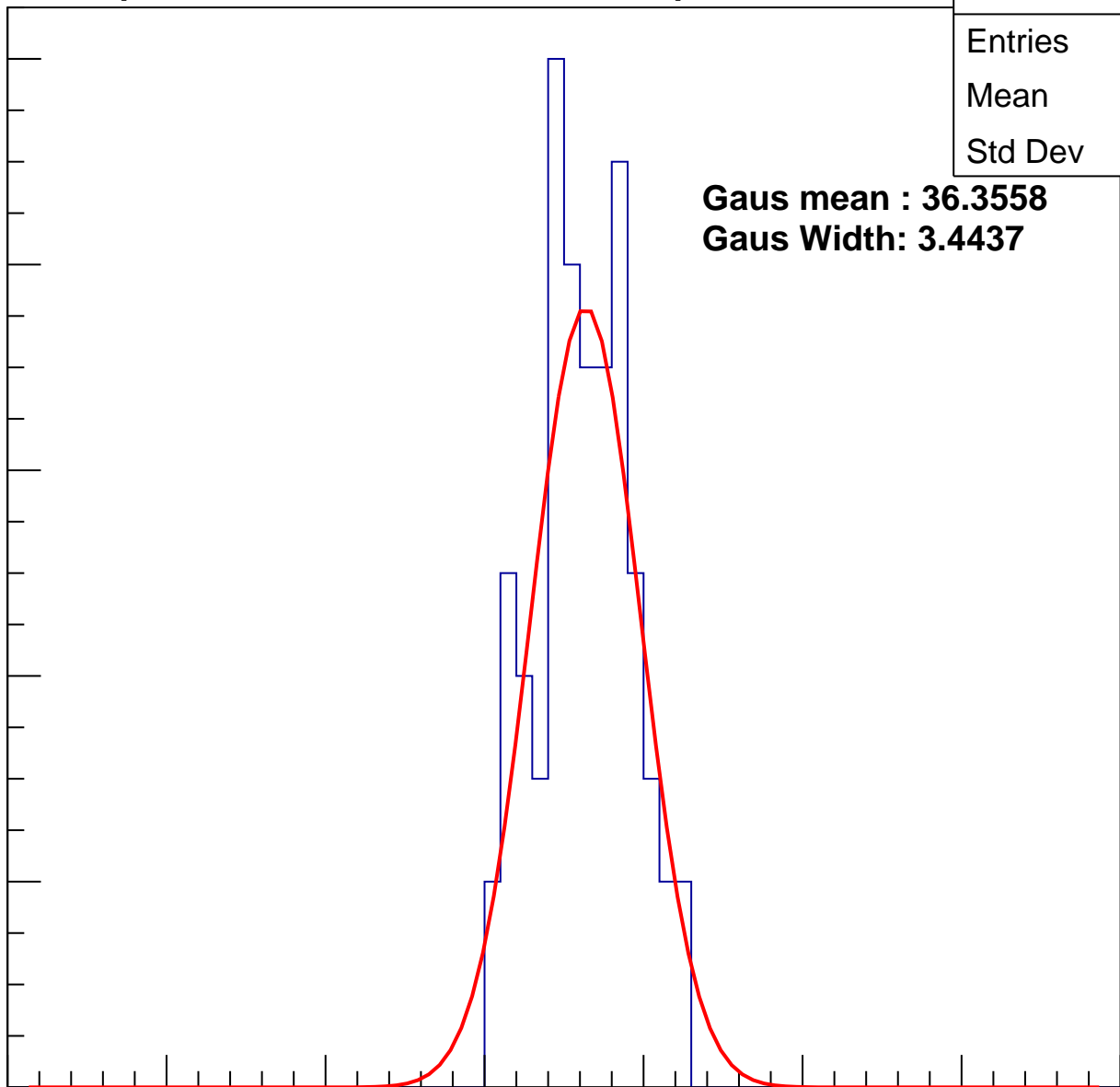
**Gaus Width: 3.4437**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U8-ch8, adc2

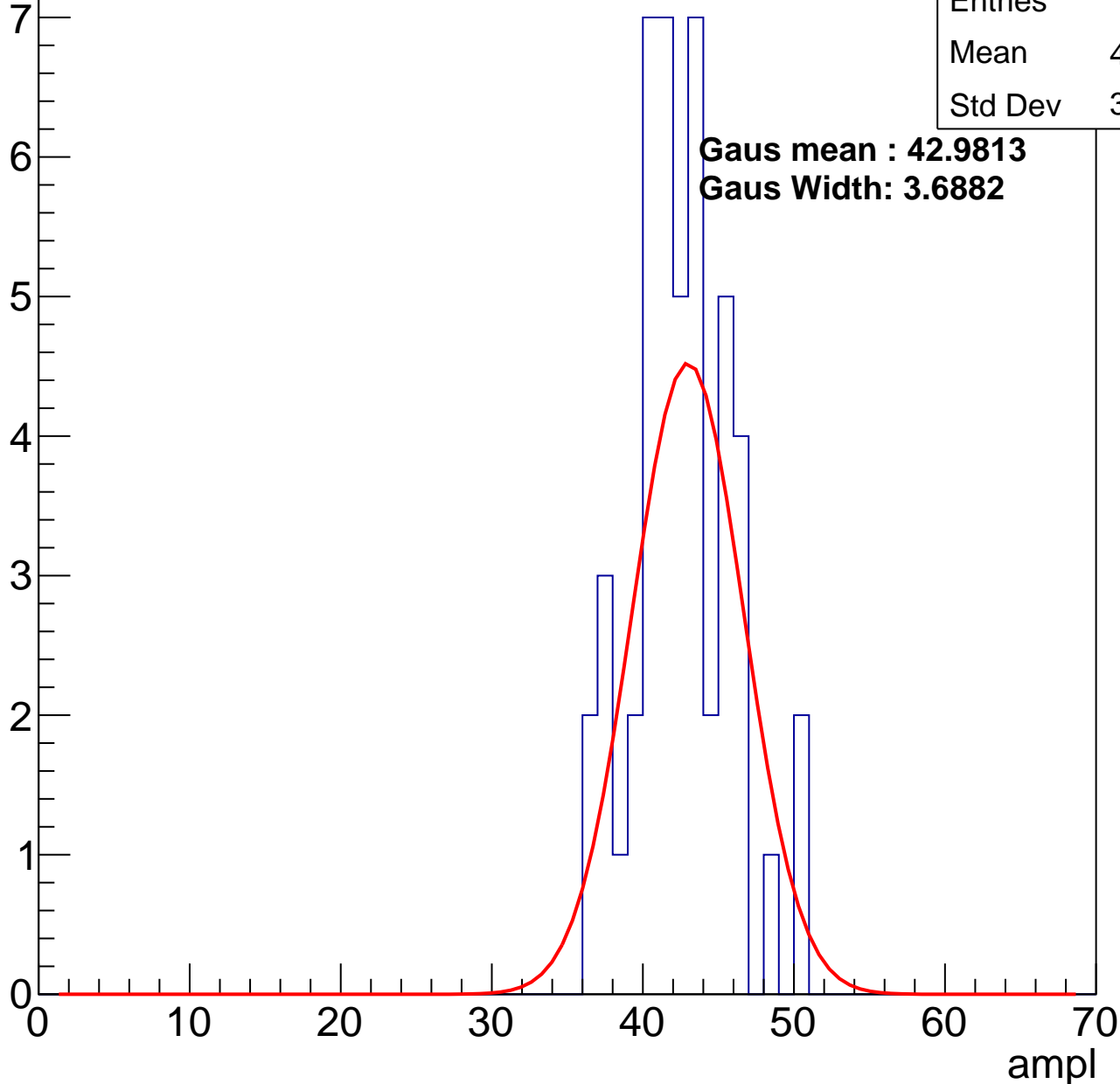
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	42.12
Std Dev	3.238

**Gaus mean : 42.9813**

**Gaus Width: 3.6882**



# B1L101S, U8-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

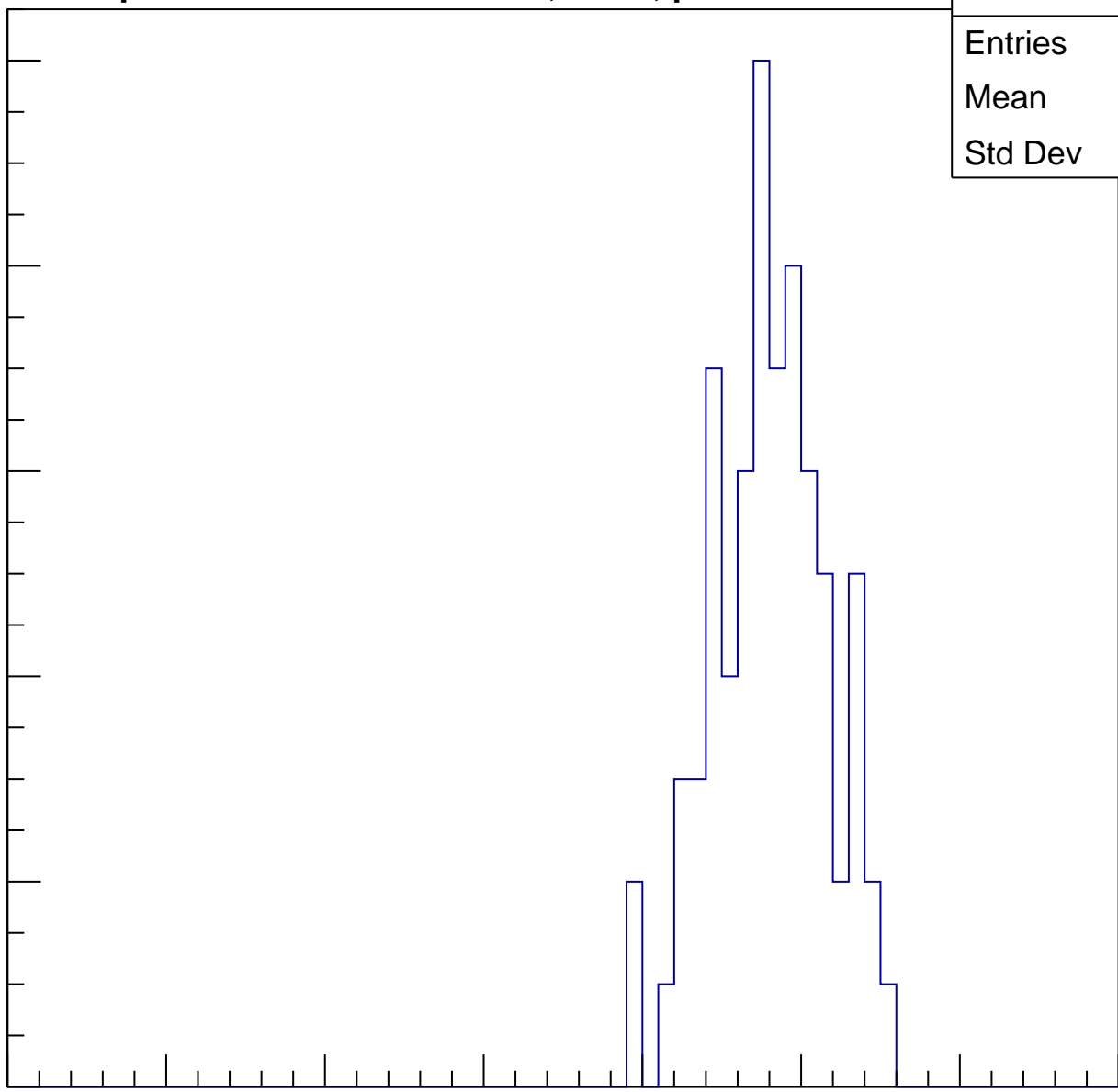
Entries	72
Mean	47.54
Std Dev	3.567

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

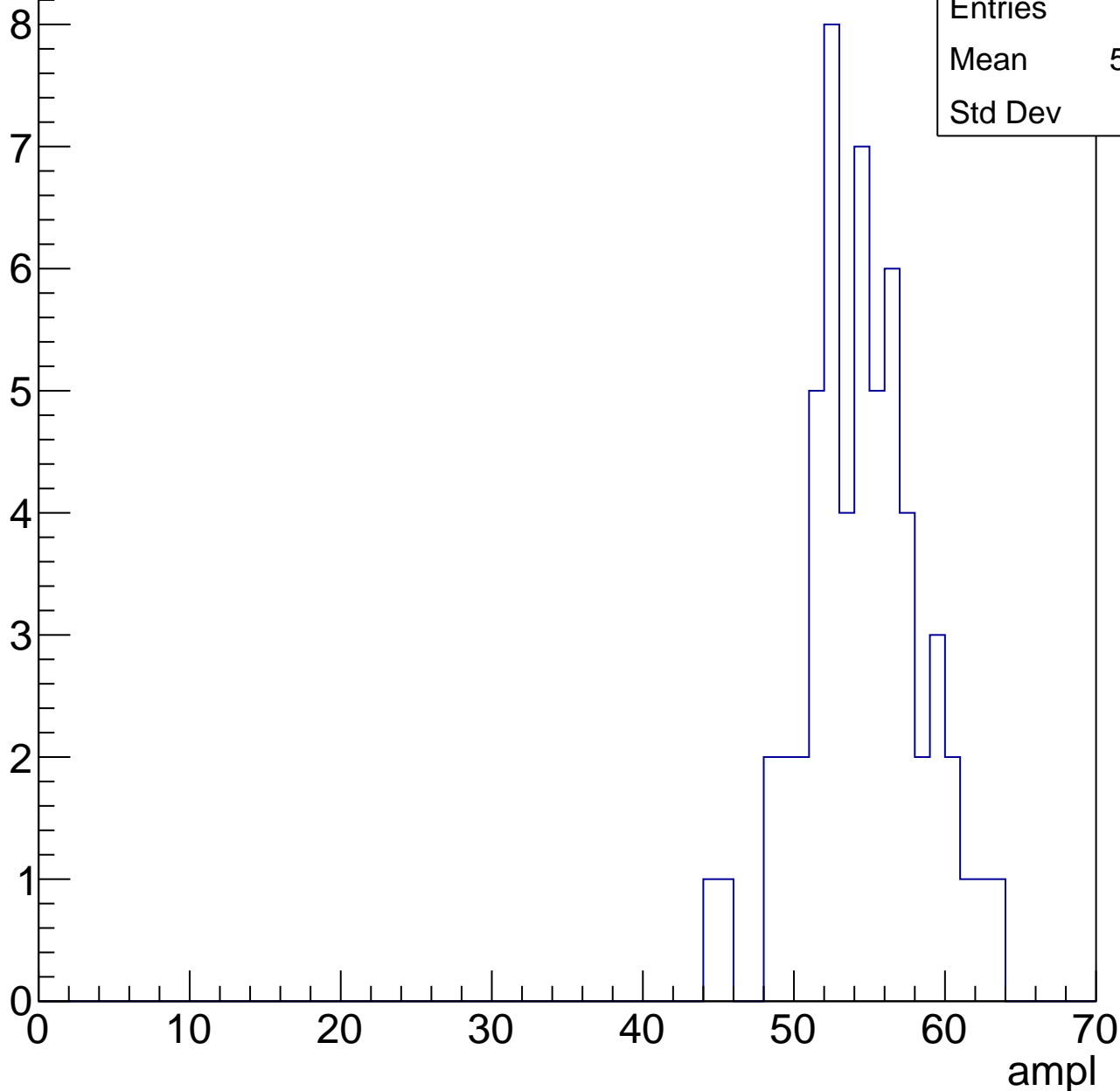


# B1L101S, U8-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	54.07
Std Dev	3.87



# B1L101S, U8-ch8, adc5

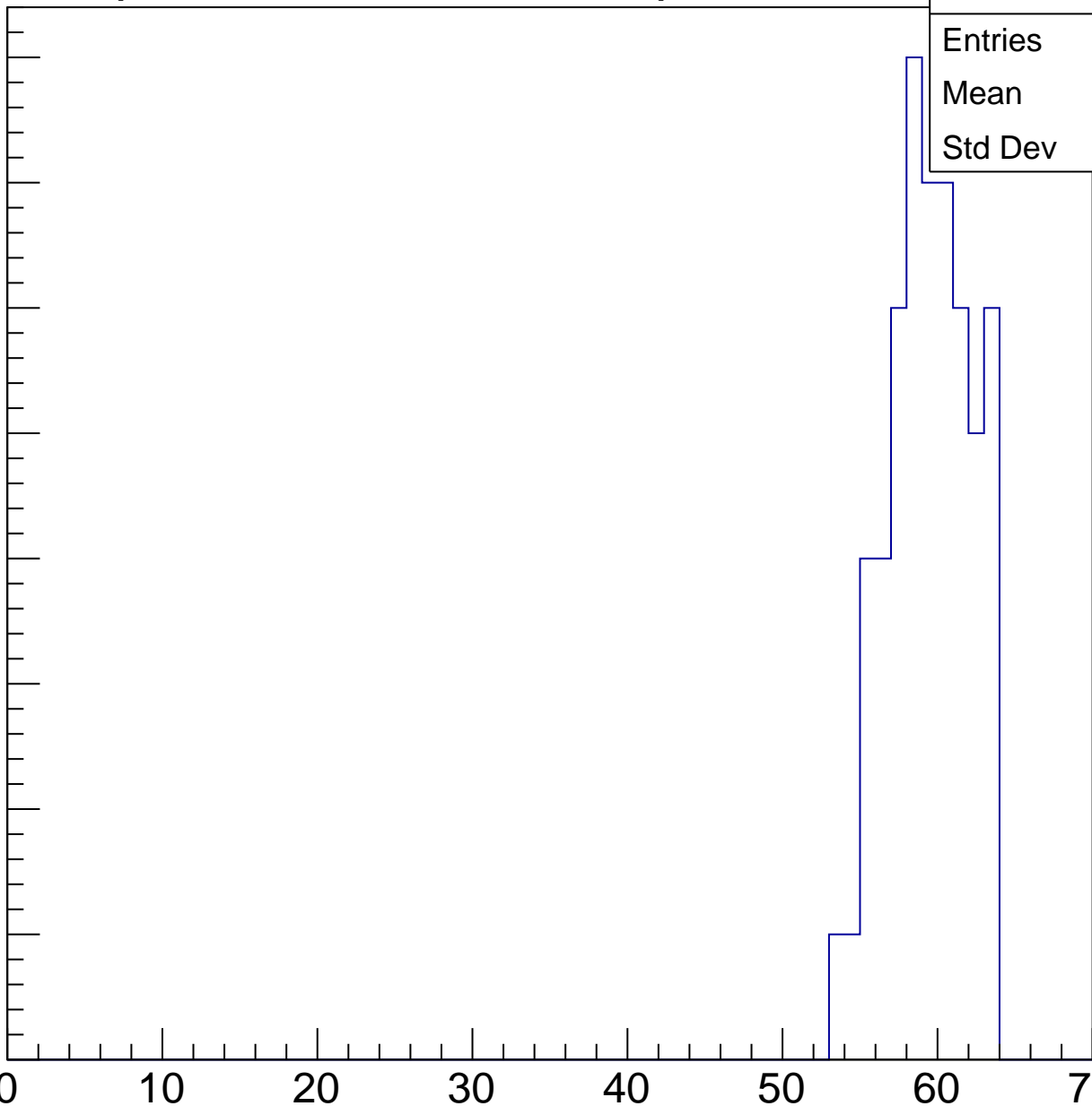
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	55
Mean	58.98
Std Dev	2.576

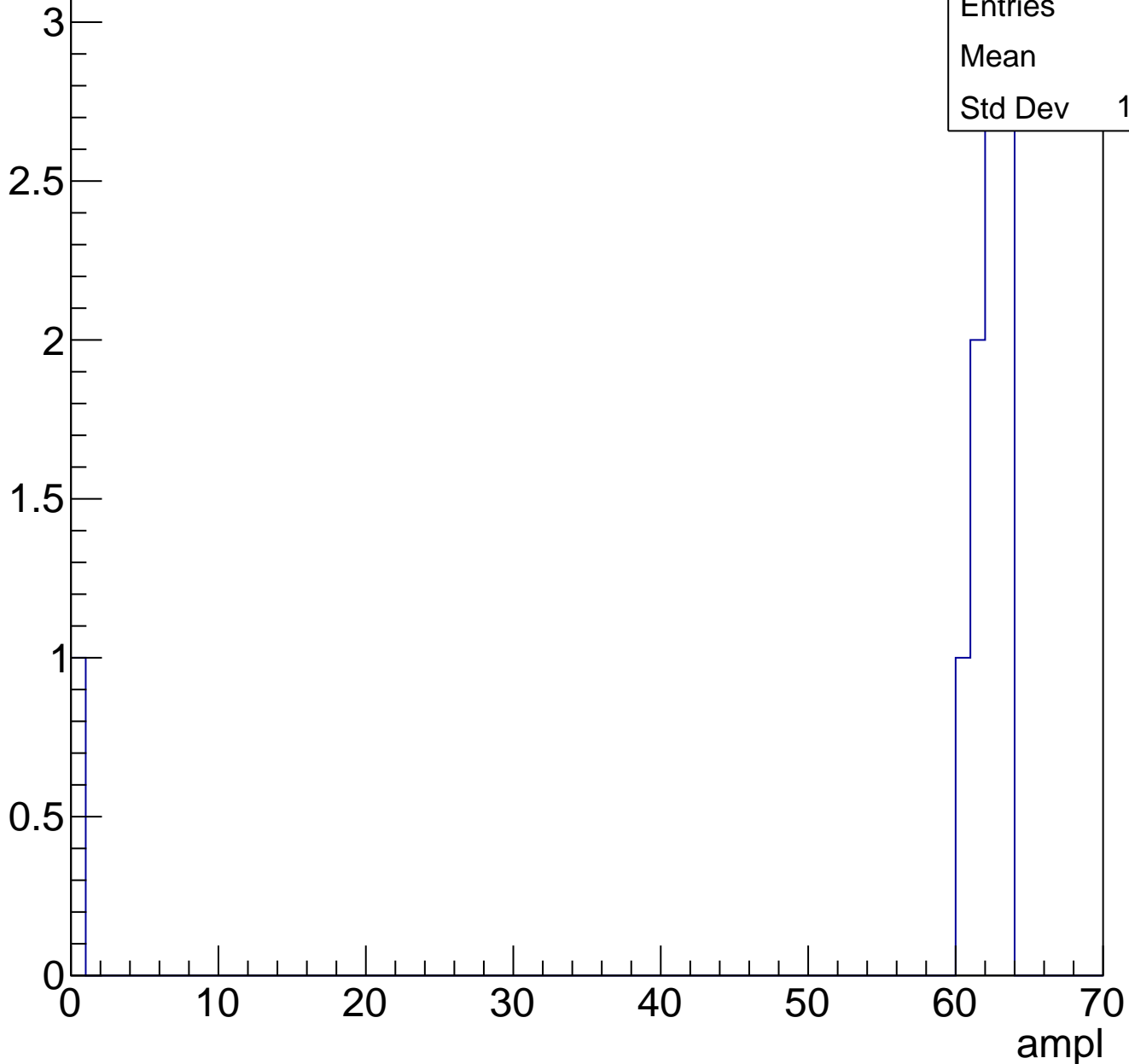
ampl



# B1L101S, U8-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

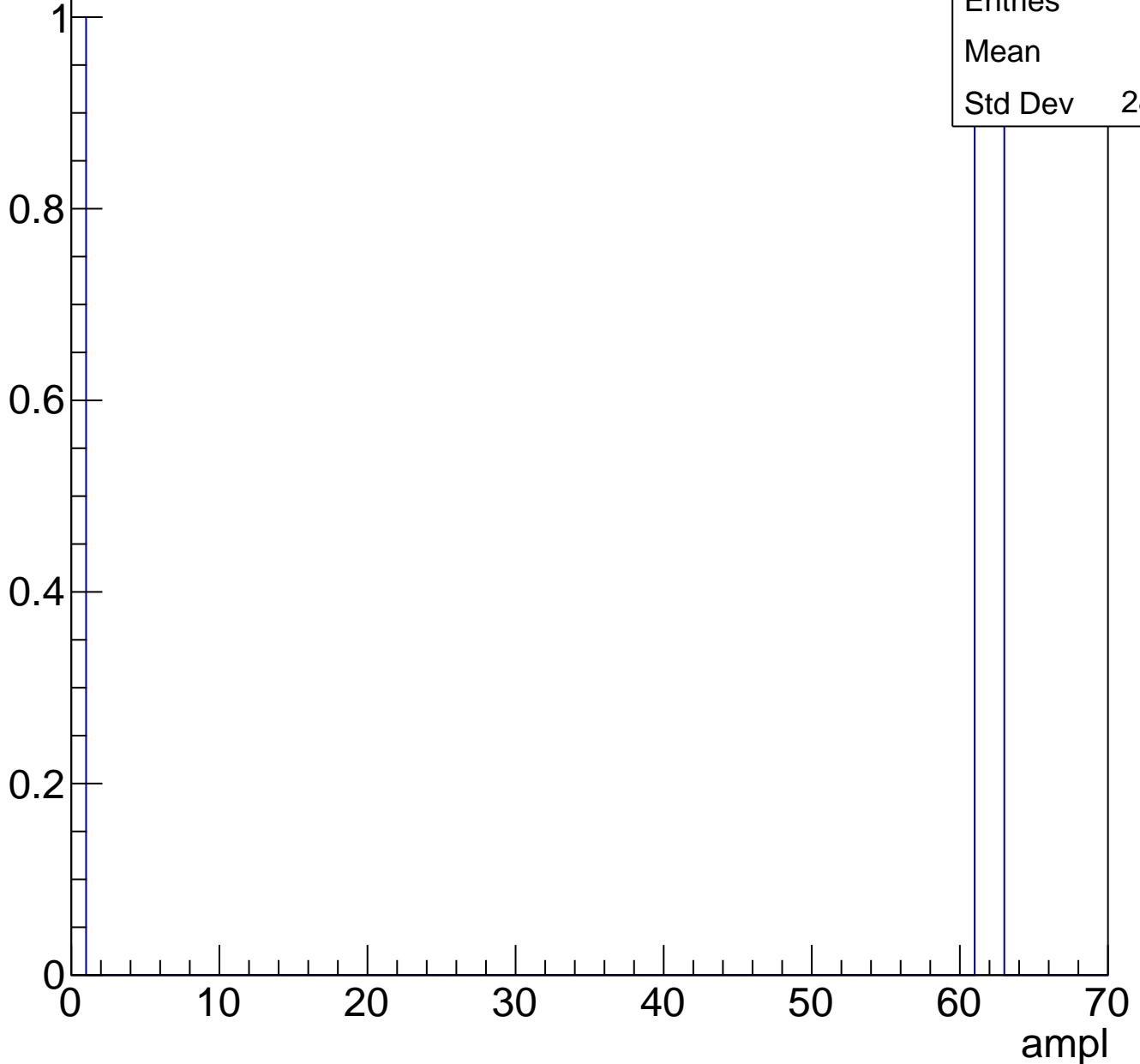




# B1L101S, U8-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



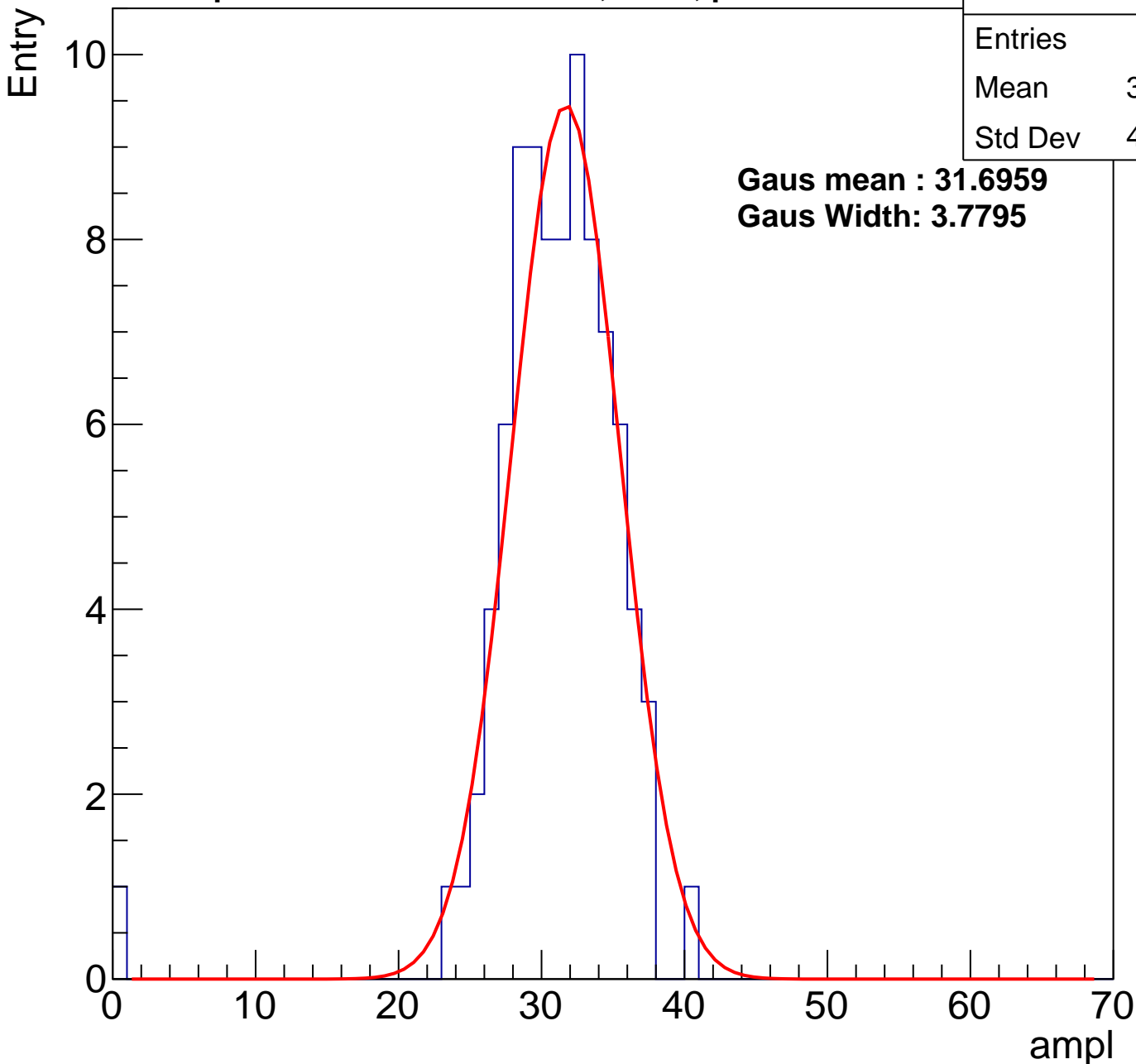
# B1L101S, U8-ch9, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	88
Mean	30.58
Std Dev	4.697

**Gaus mean : 31.6959**

**Gaus Width: 3.7795**



# B1L101S, U8-ch9, adc1

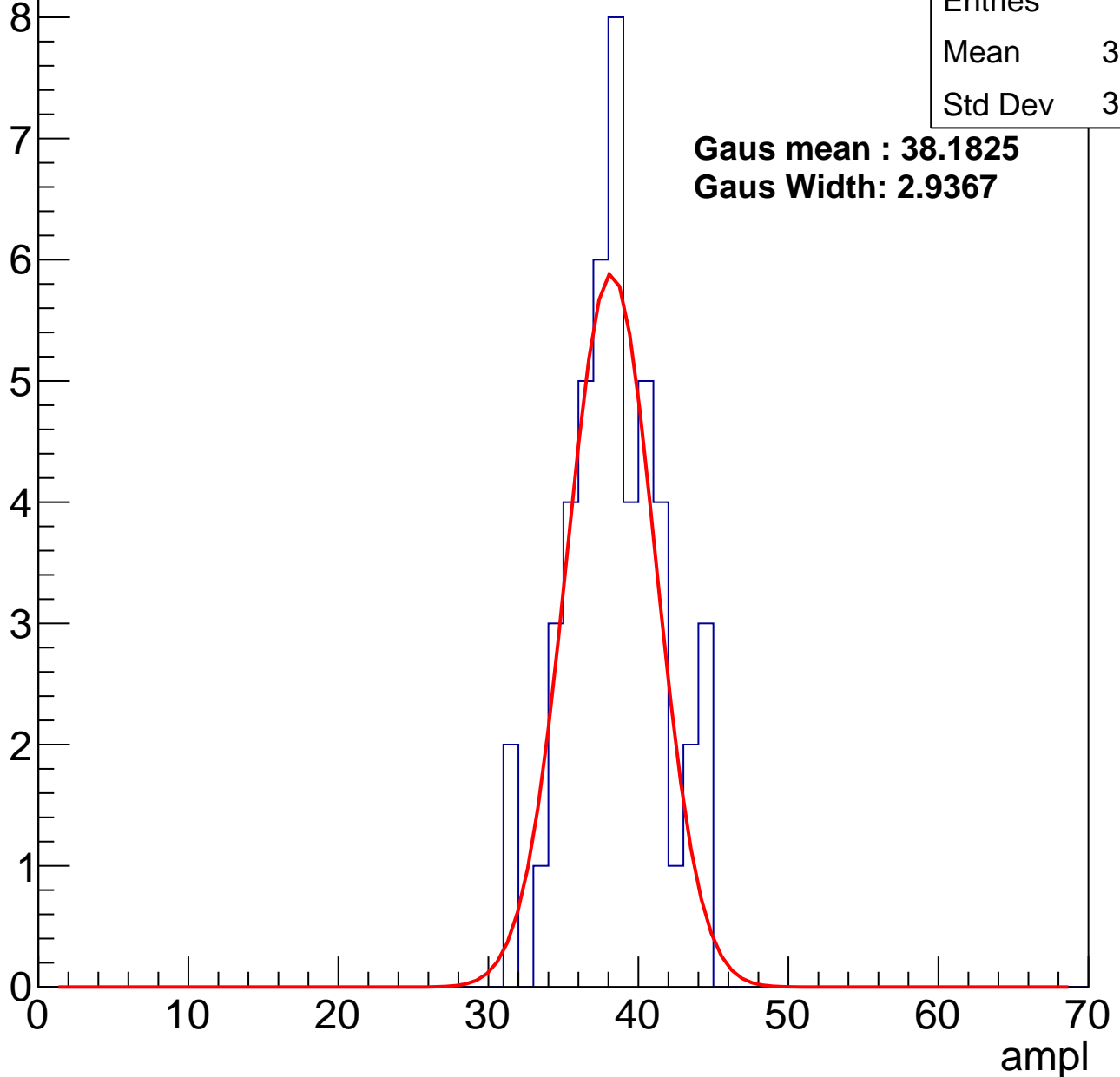
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	37.98
Std Dev	3.119

**Gaus mean : 38.1825**

**Gaus Width: 2.9367**



# B1L101S, U8-ch9, adc2

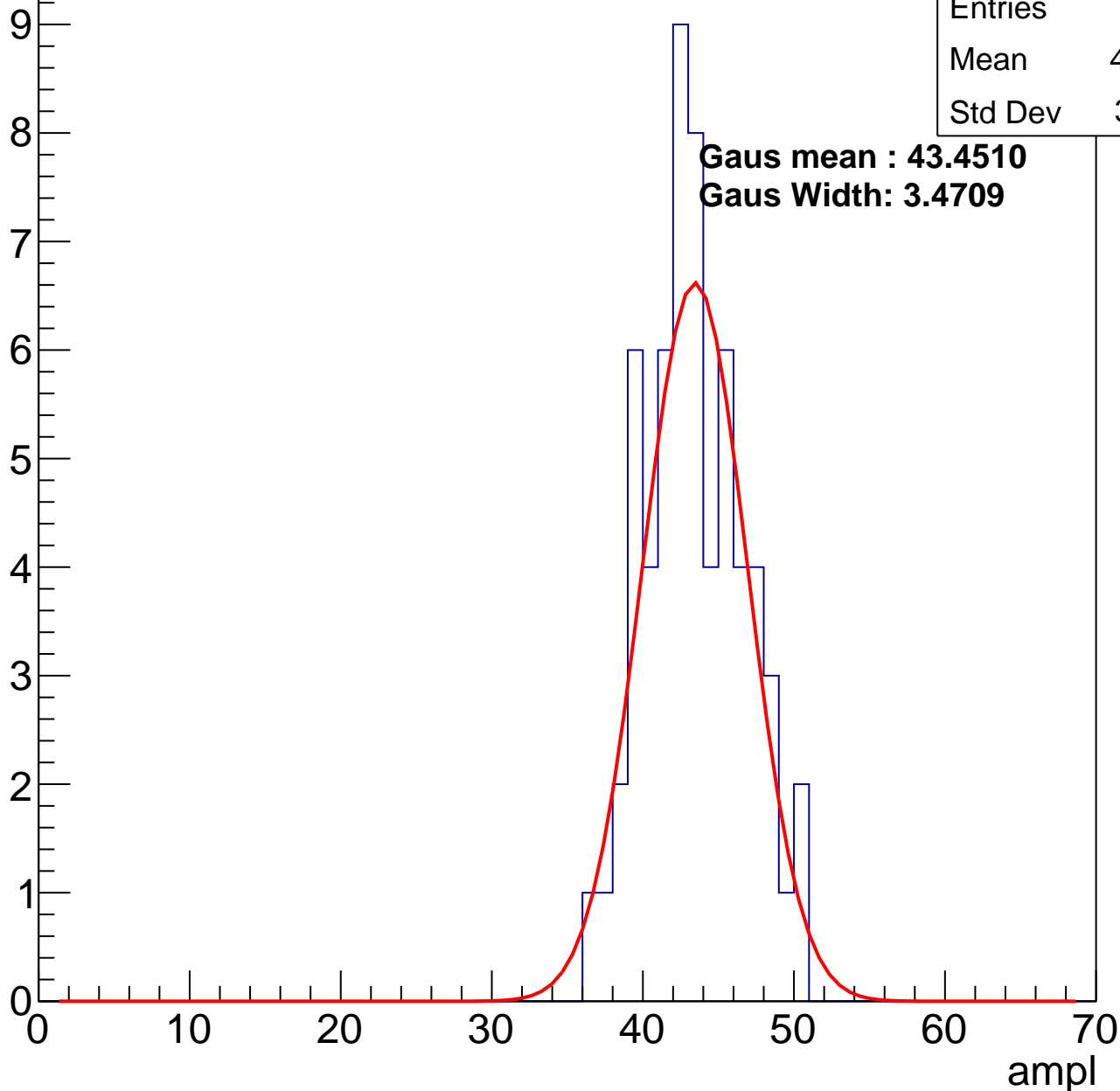
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	42.98
Std Dev	3.231

**Gaus mean : 43.4510**

**Gaus Width: 3.4709**

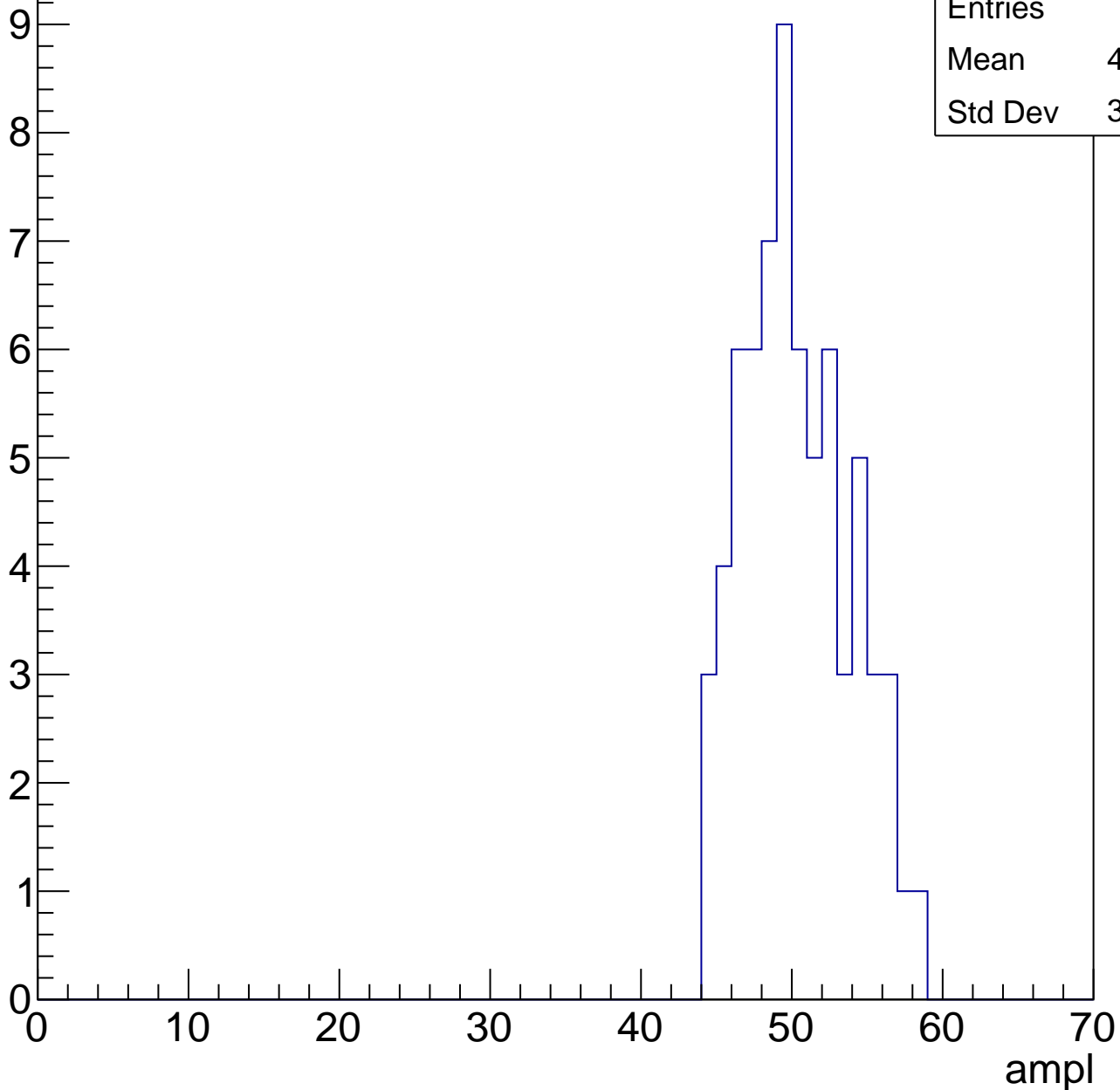


# B1L101S, U8-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

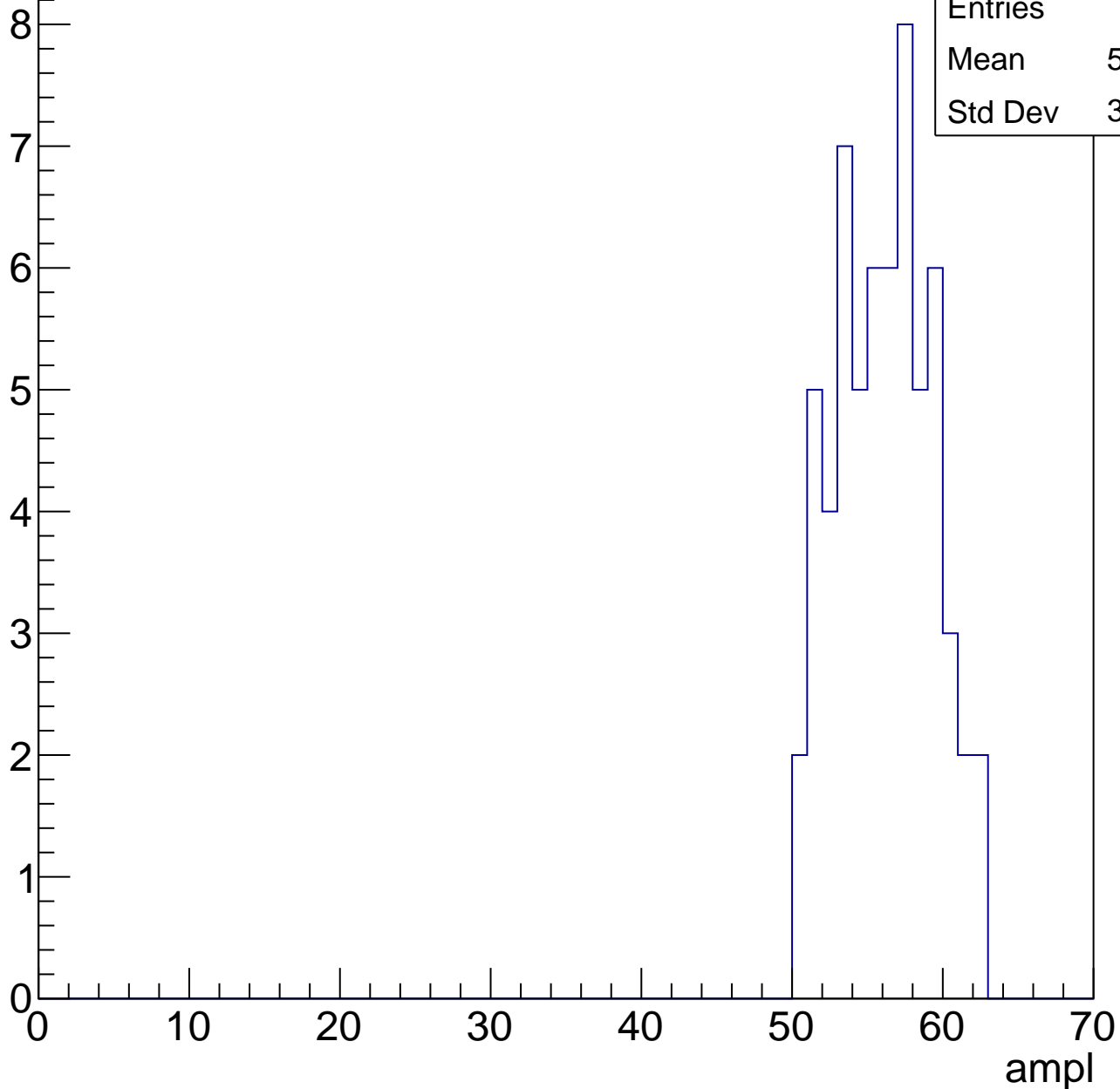
Entries	68
Mean	49.87
Std Dev	3.485



# B1L101S, U8-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

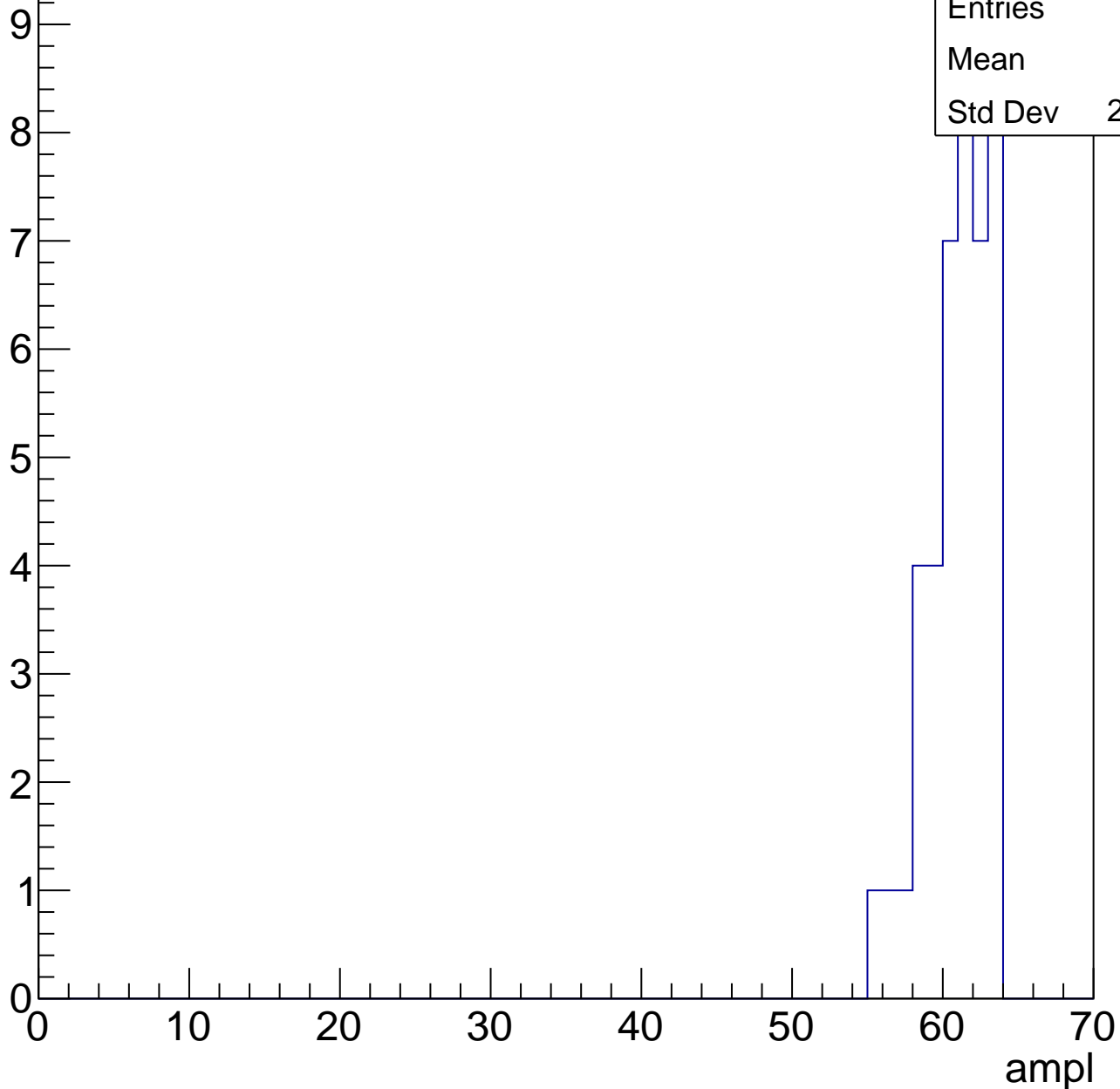
Entry



# B1L101S, U8-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

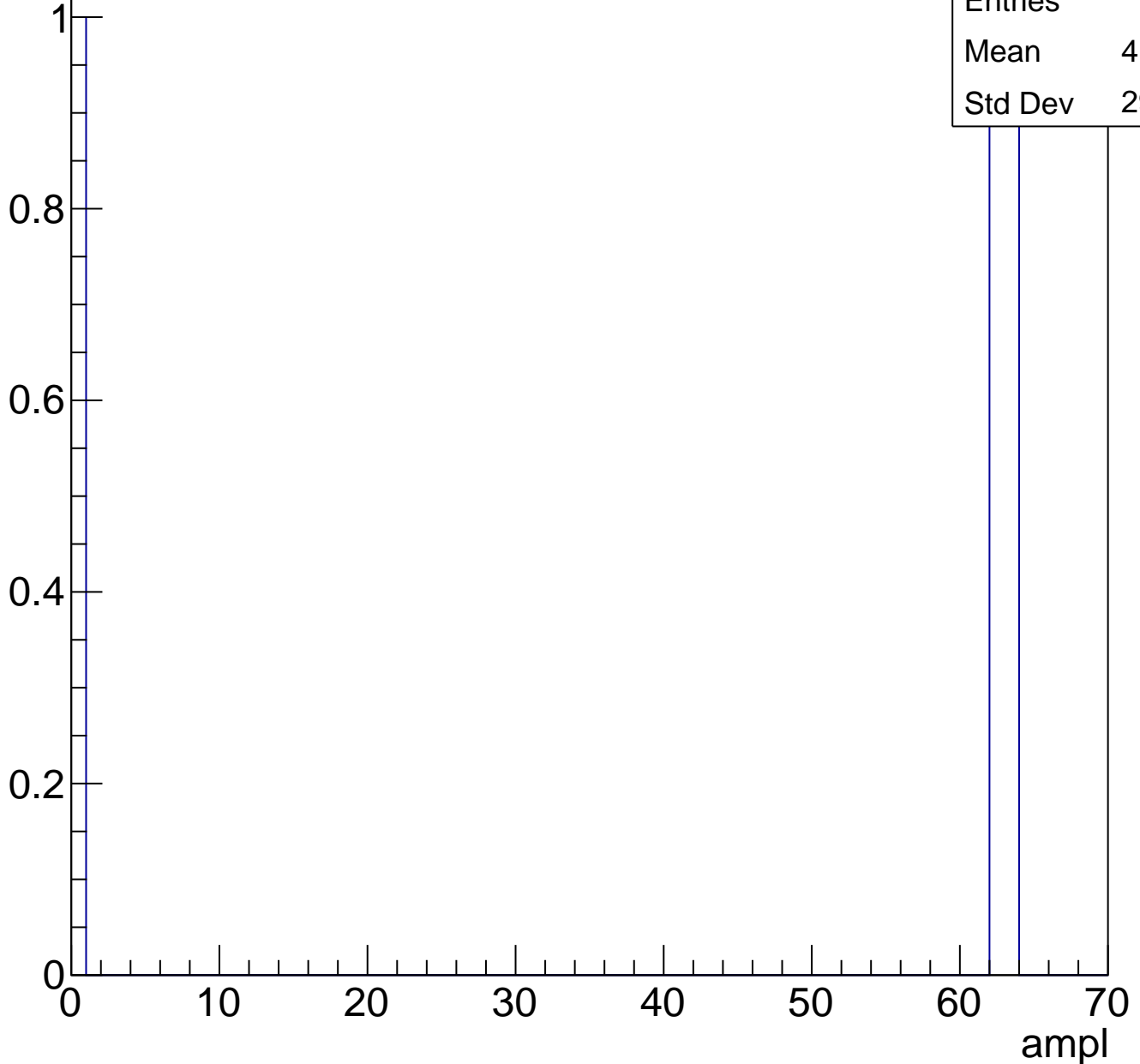
Entry



# B1L101S, U8-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch10, adc0

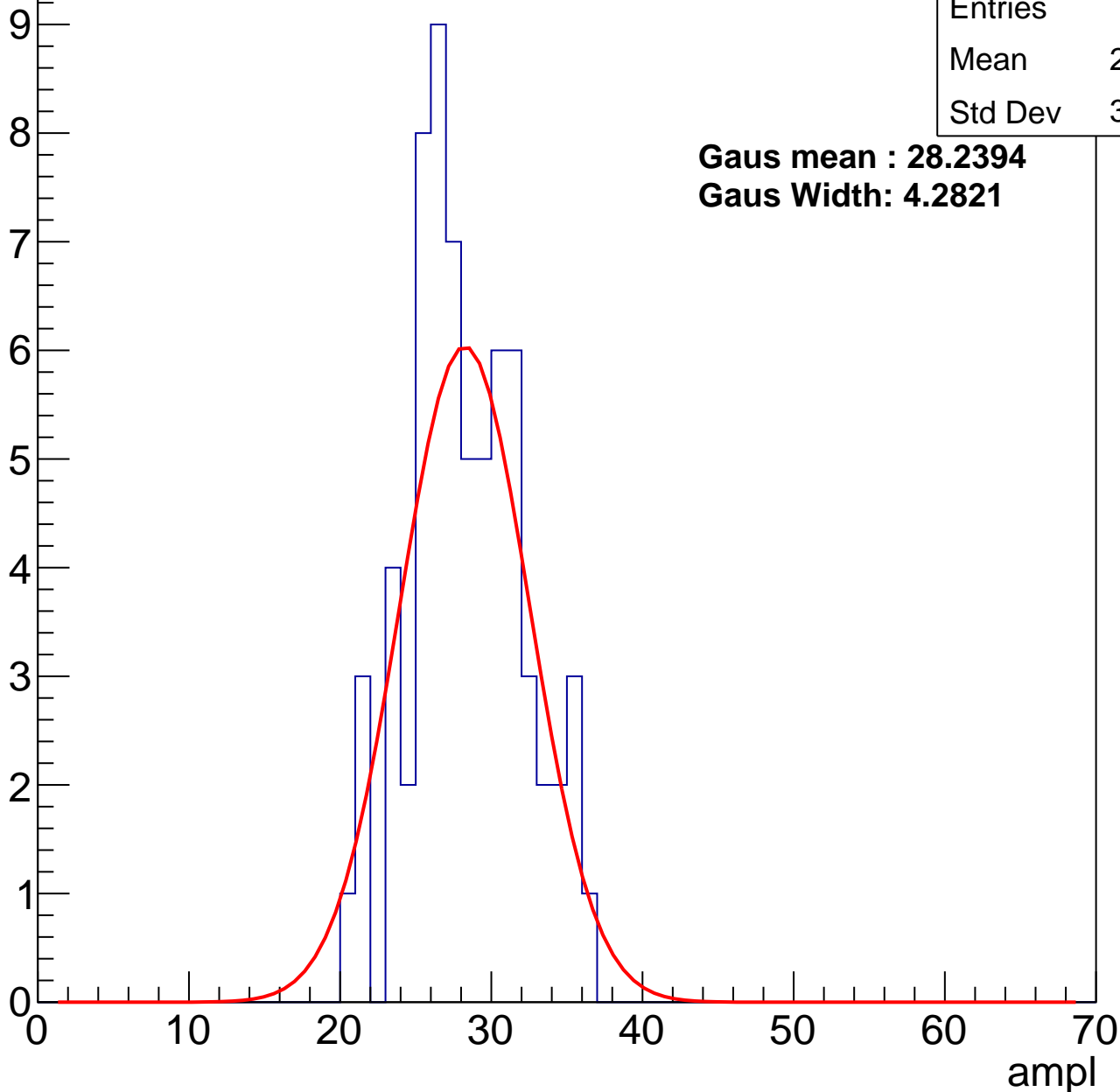
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	27.88
Std Dev	3.708

**Gaus mean : 28.2394**

**Gaus Width: 4.2821**



# B1L101S, U8-ch10, adc1

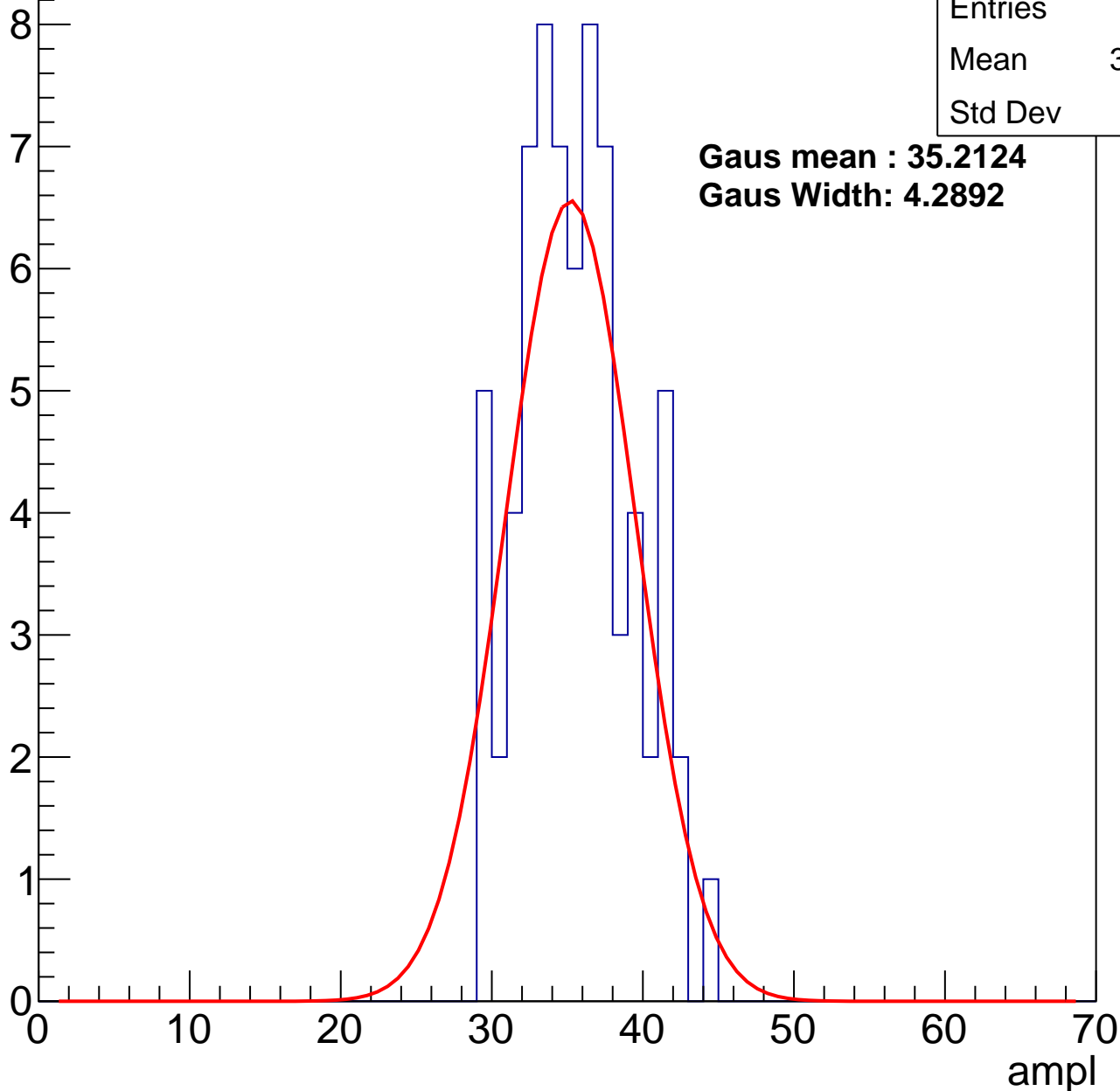
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	35.14
Std Dev	3.62

**Gaus mean : 35.2124**

**Gaus Width: 4.2892**



# B1L101S, U8-ch10, adc2

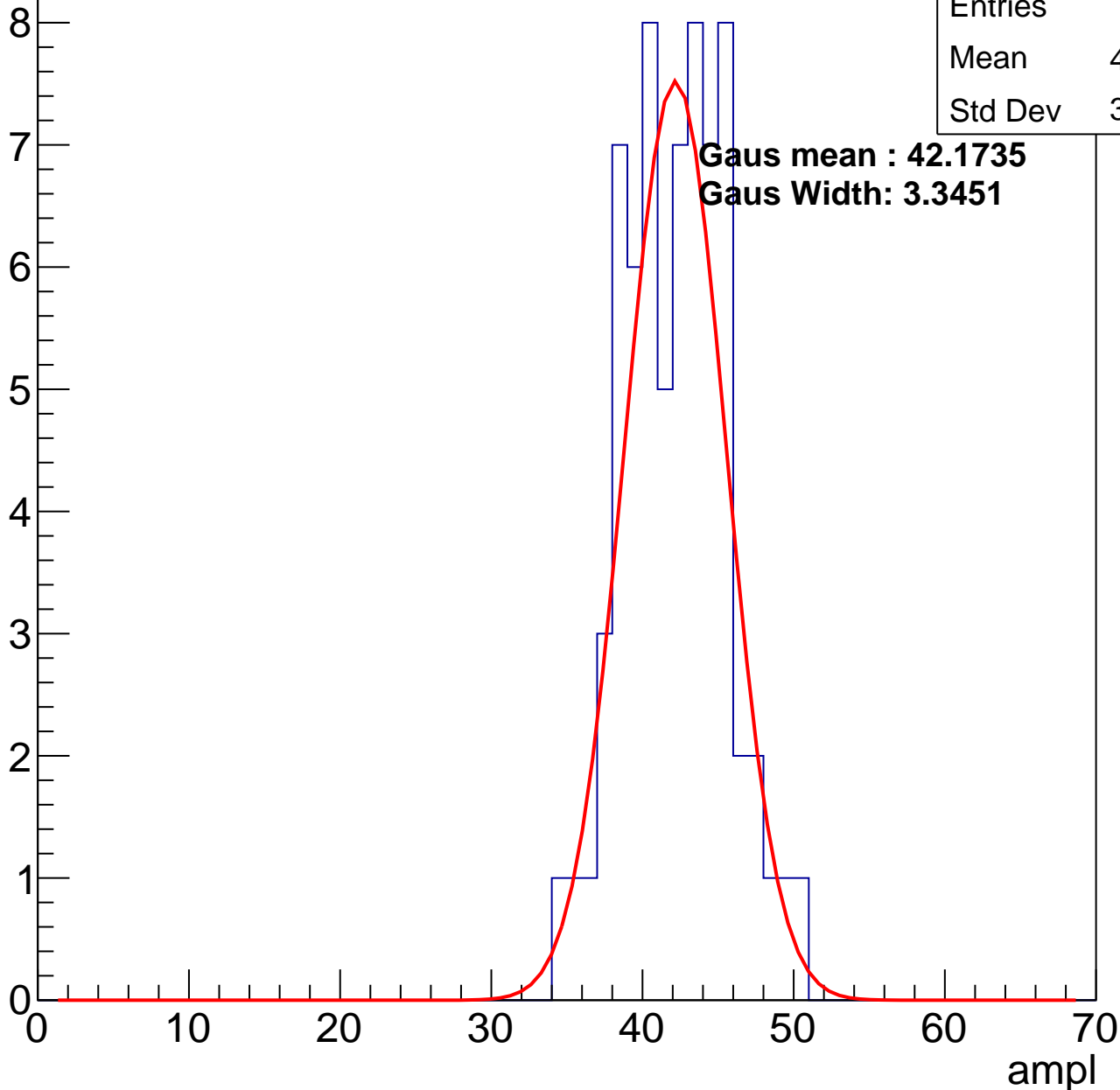
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	41.74
Std Dev	3.322

**Gaus mean : 42.1735**

**Gaus Width: 3.3451**

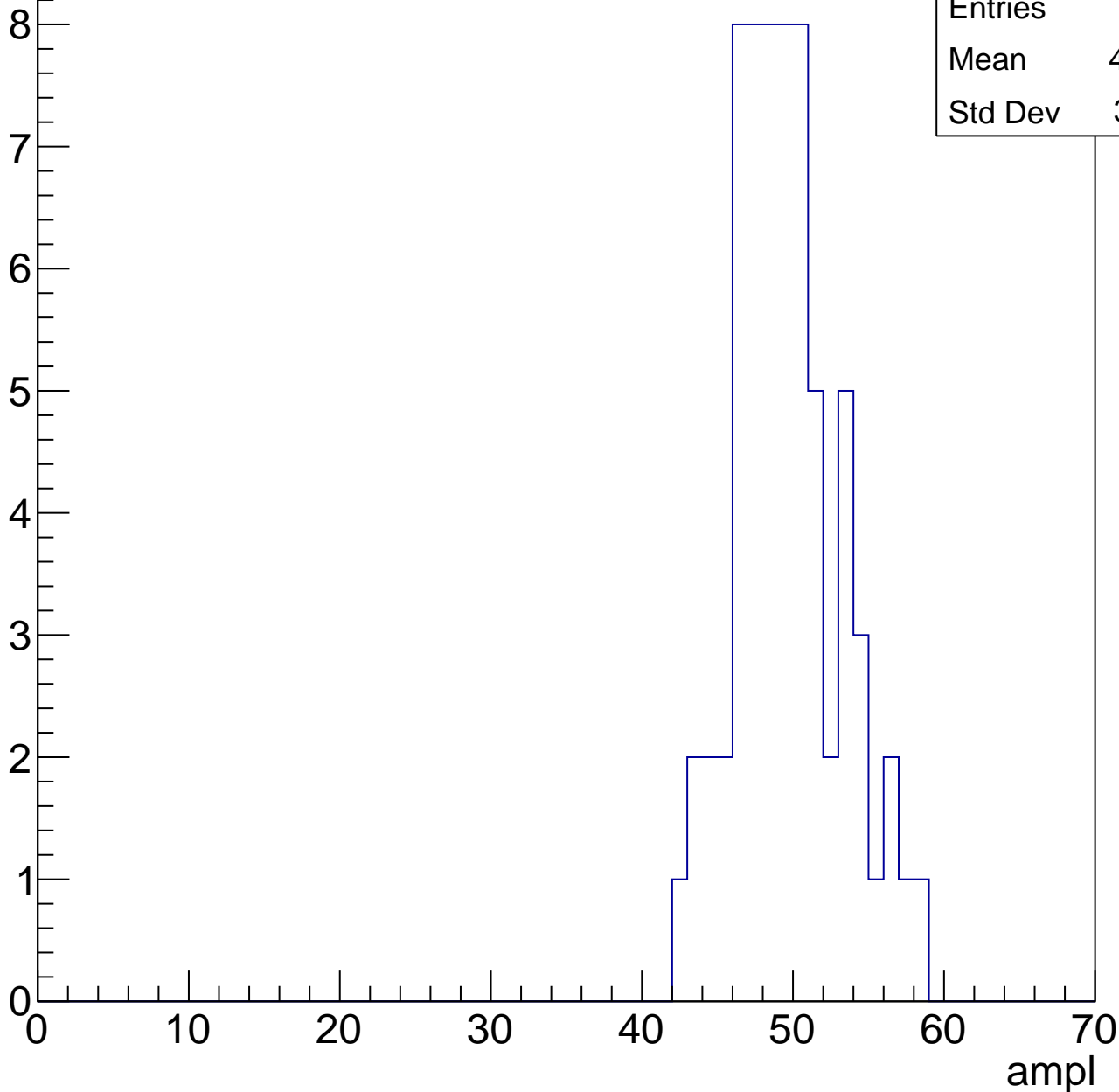


# B1L101S, U8-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

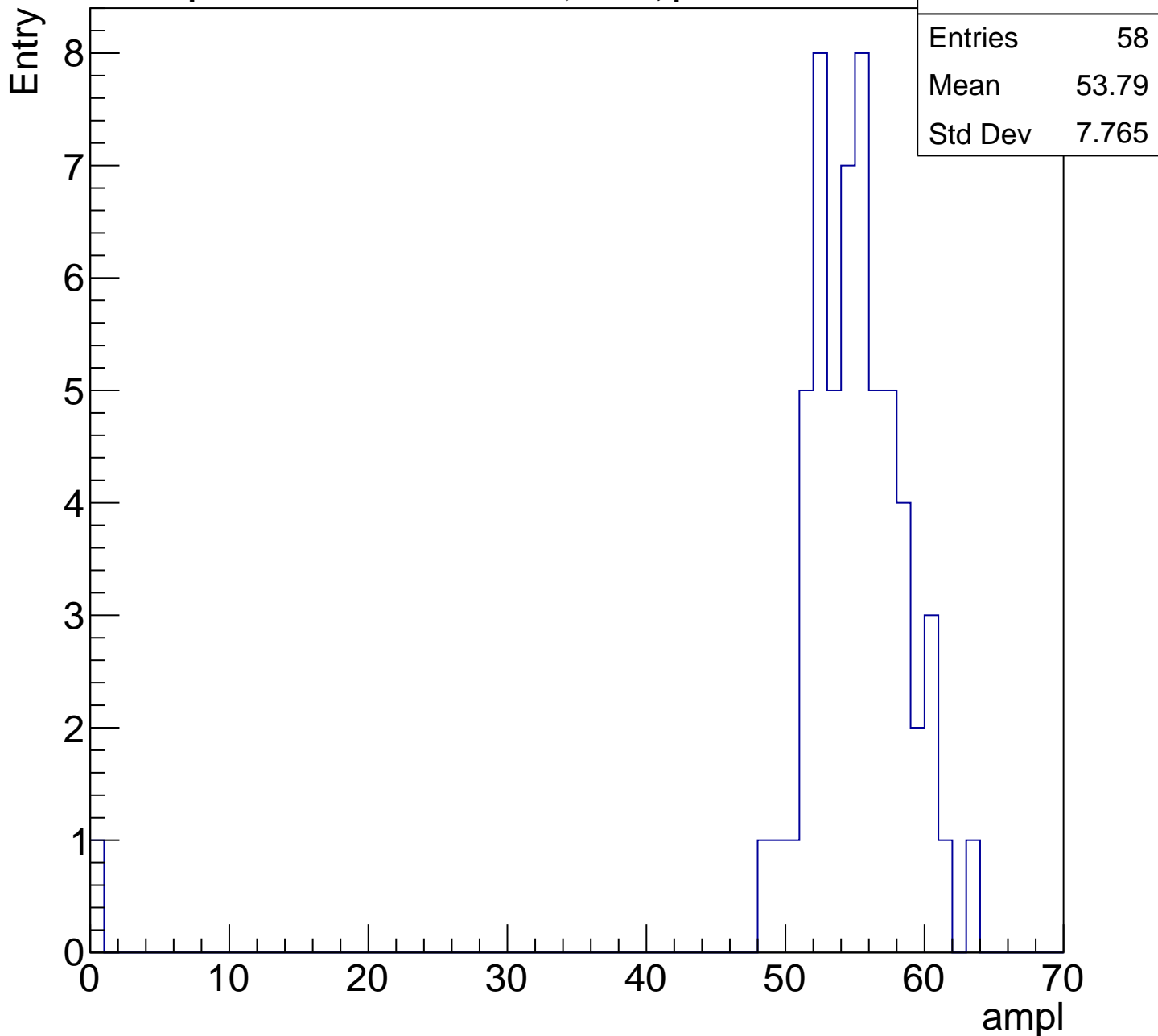
Entry

Entries	67
Mean	49.16
Std Dev	3.441



# B1L101S, U8-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U8-ch10, adc5

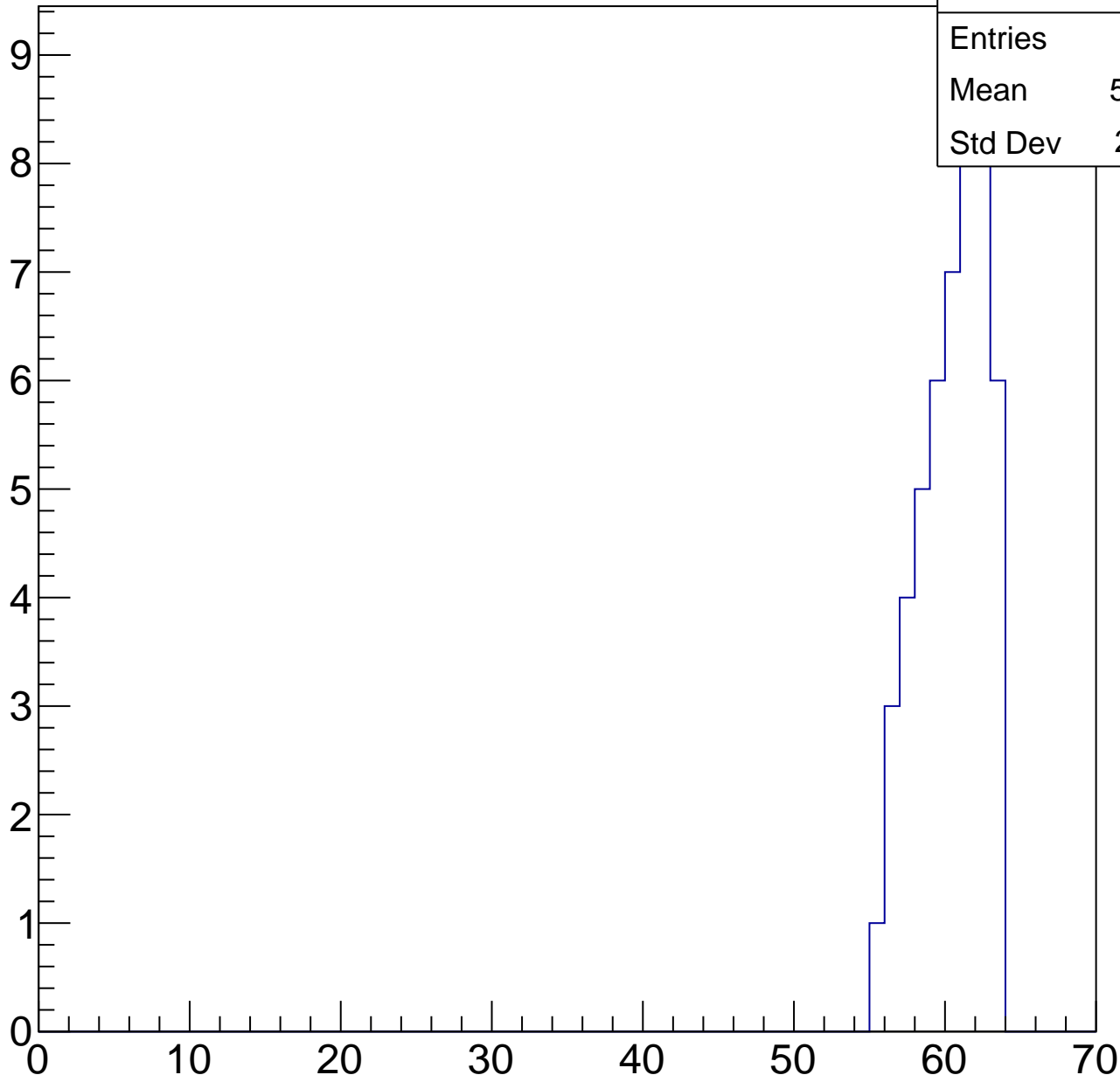
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	59.98
Std Dev	2.181

ampl



# B1L101S, U8-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

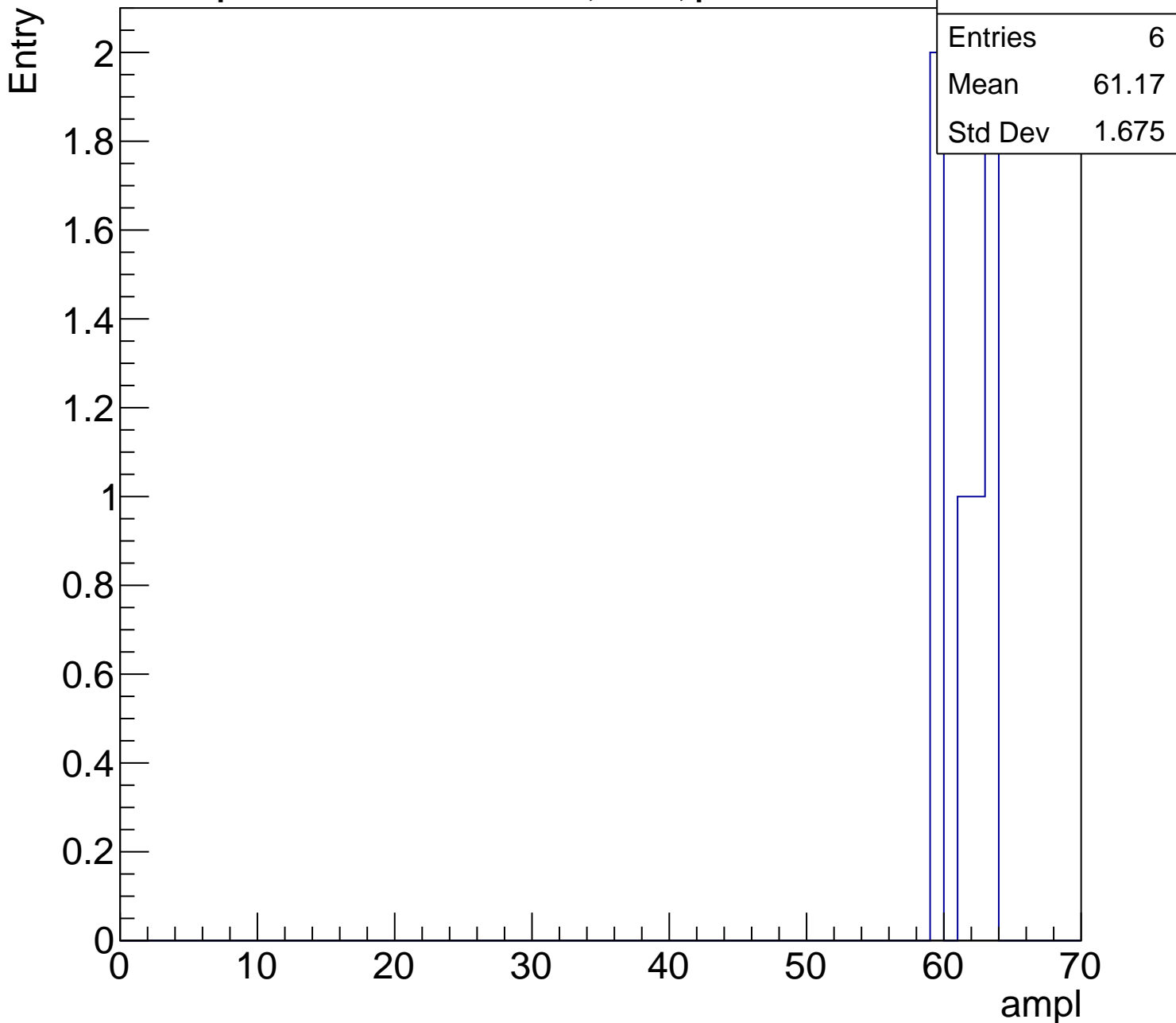
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.17
Std Dev	1.675

0 10 20 30 40 50 60 70

ampl





# B1L101S, U8-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch11, adc0

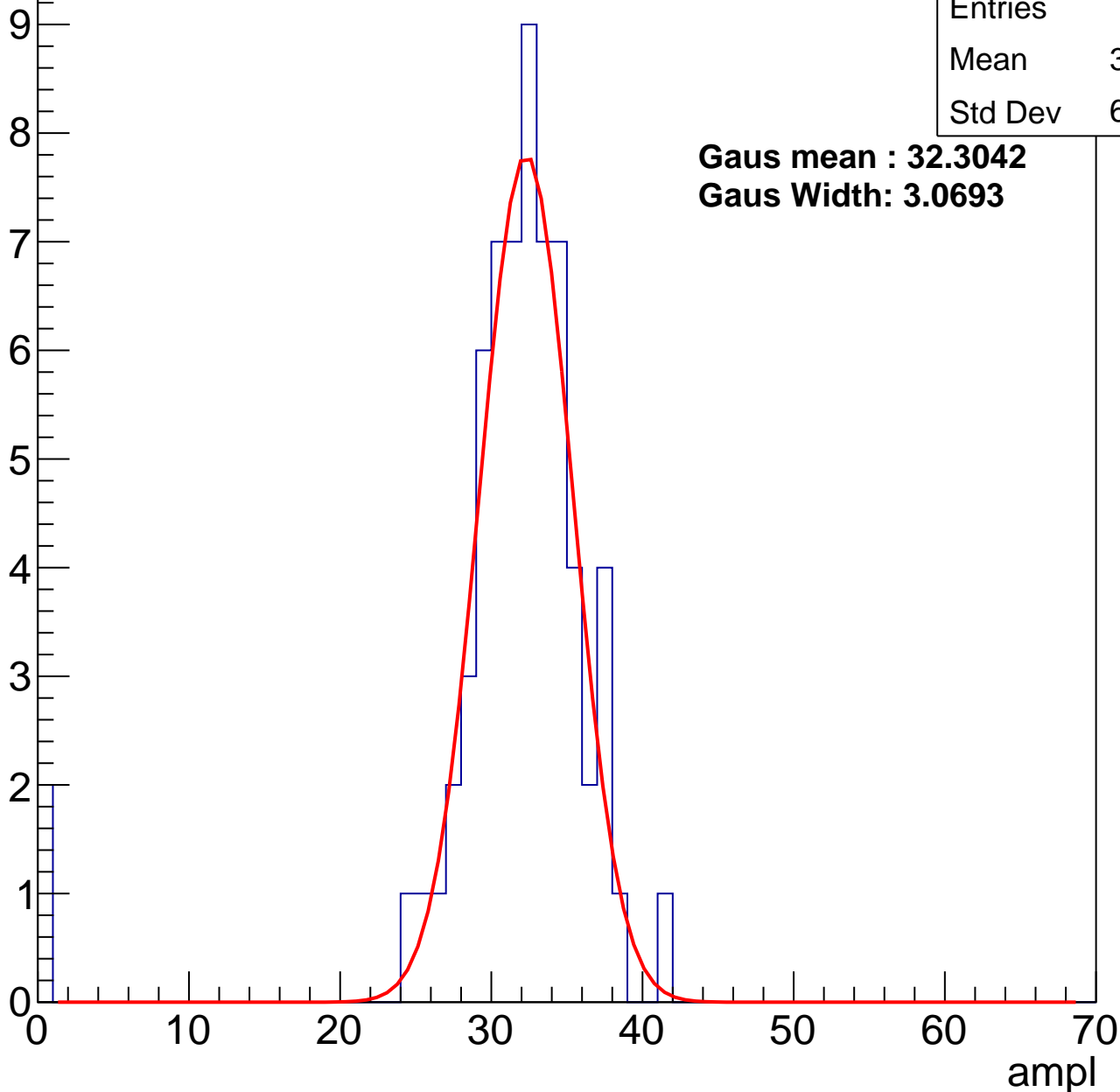
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	30.92
Std Dev	6.359

**Gaus mean : 32.3042**

**Gaus Width: 3.0693**



# B1L101S, U8-ch11, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	81
Mean	38.7
Std Dev	3.602

**Gaus mean : 39.3254**

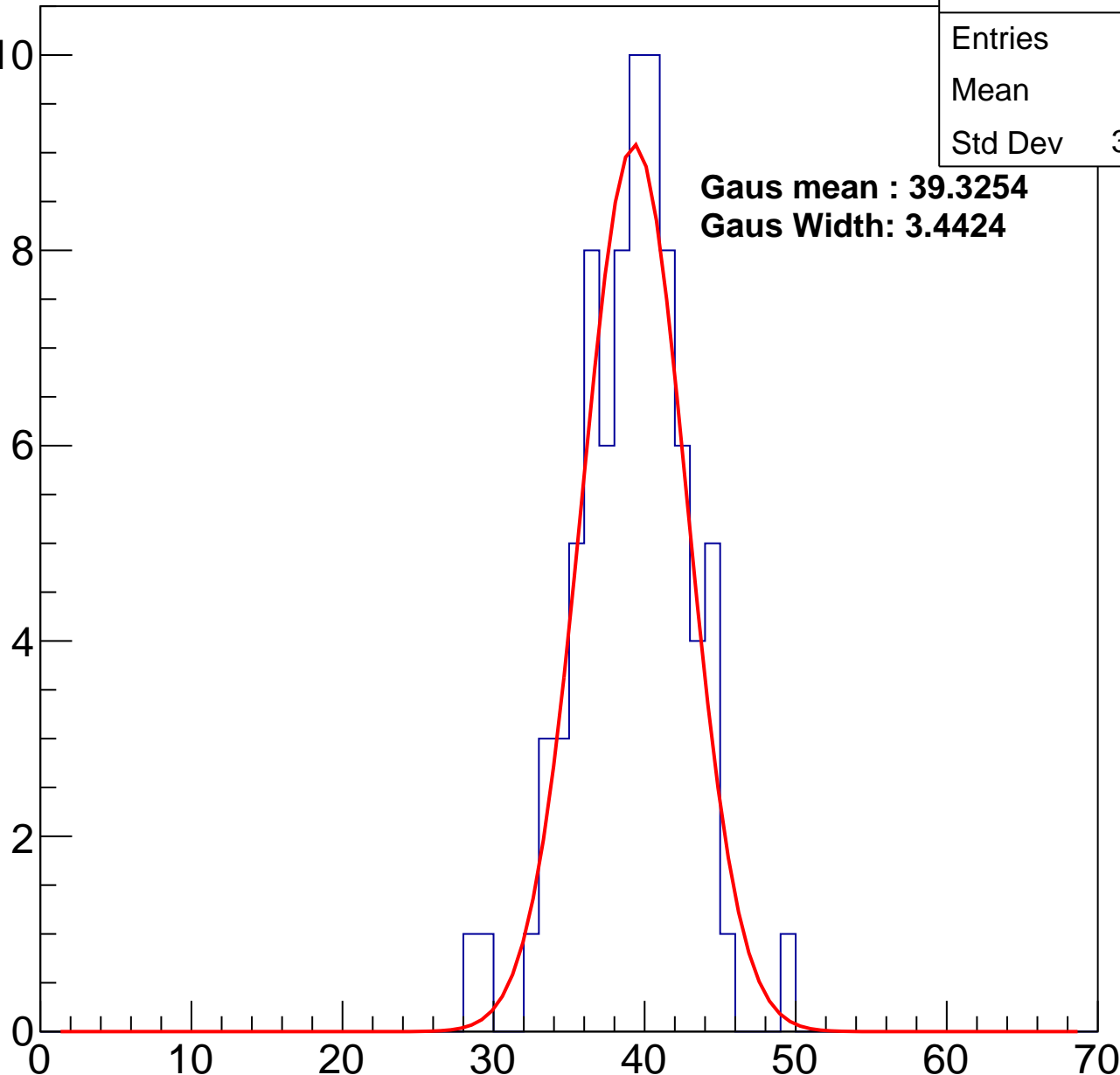
**Gaus Width: 3.4424**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U8-ch11, adc2

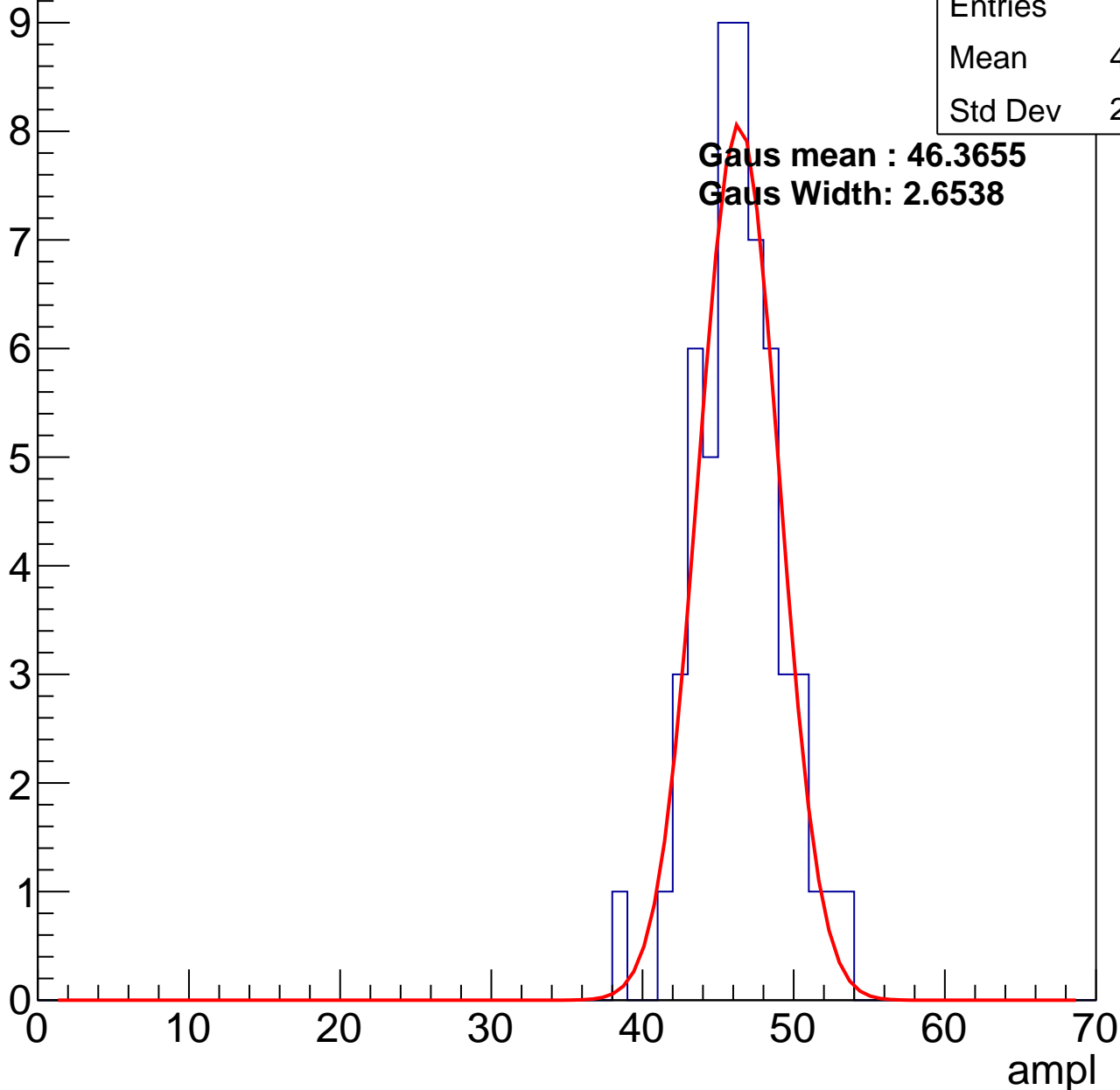
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	45.93
Std Dev	2.789

**Gaus mean : 46.3655**

**Gaus Width: 2.6538**

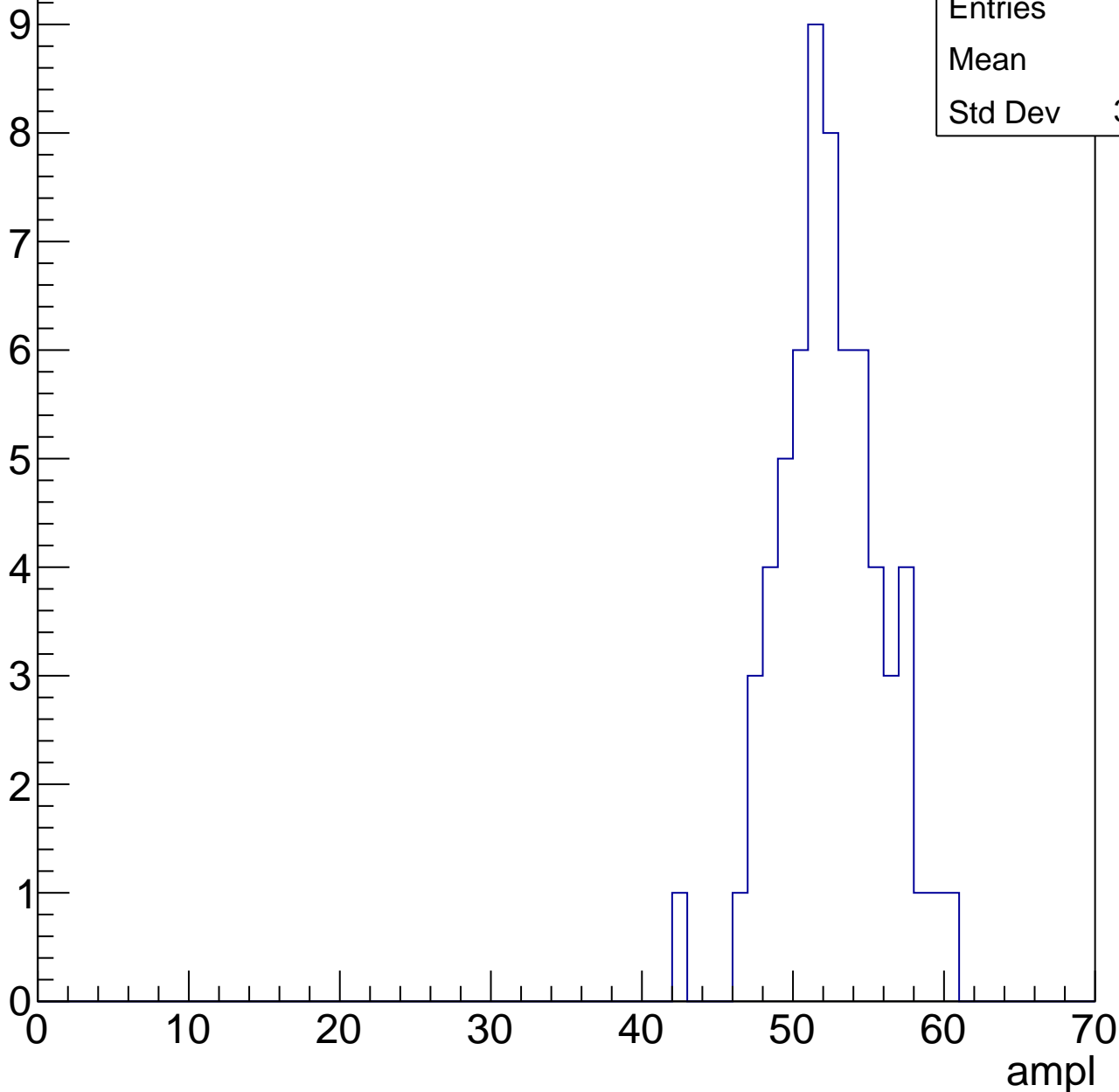


# B1L101S, U8-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	52
Std Dev	3.371

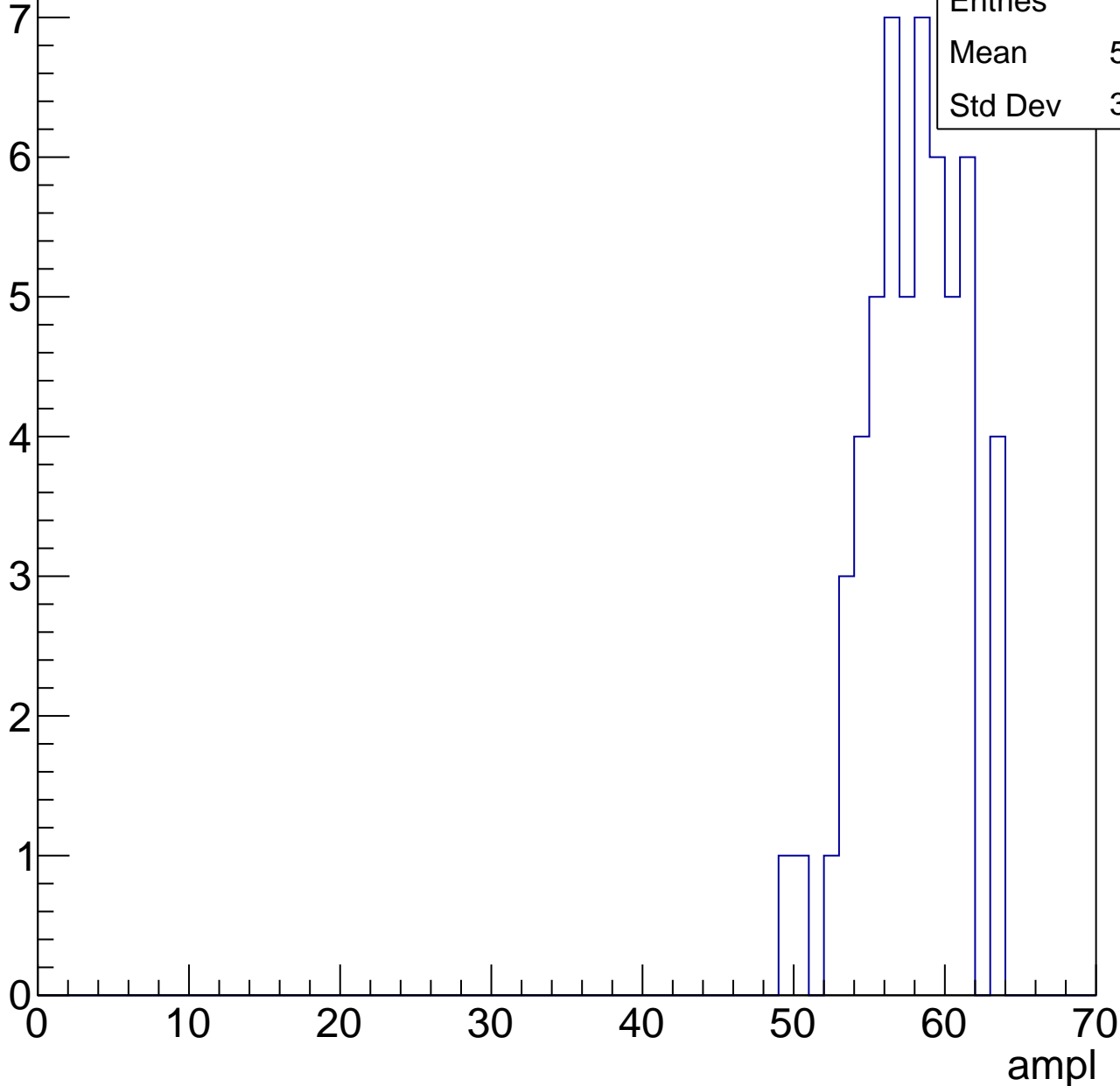


# B1L101S, U8-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	57.38
Std Dev	3.182

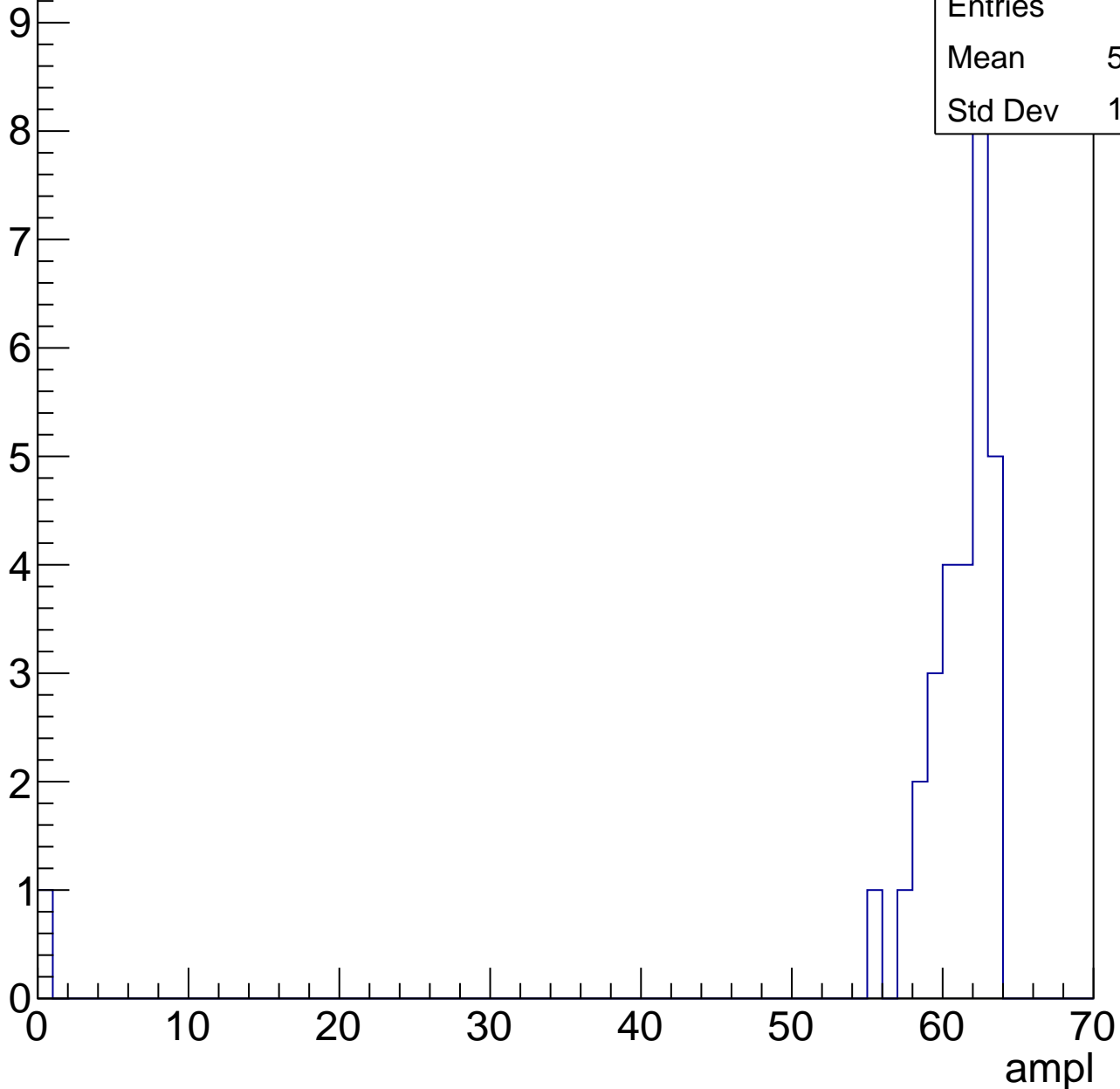


# B1L101S, U8-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	30
Mean	58.73
Std Dev	11.08



# B1L101S, U8-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U8-ch12, adc0

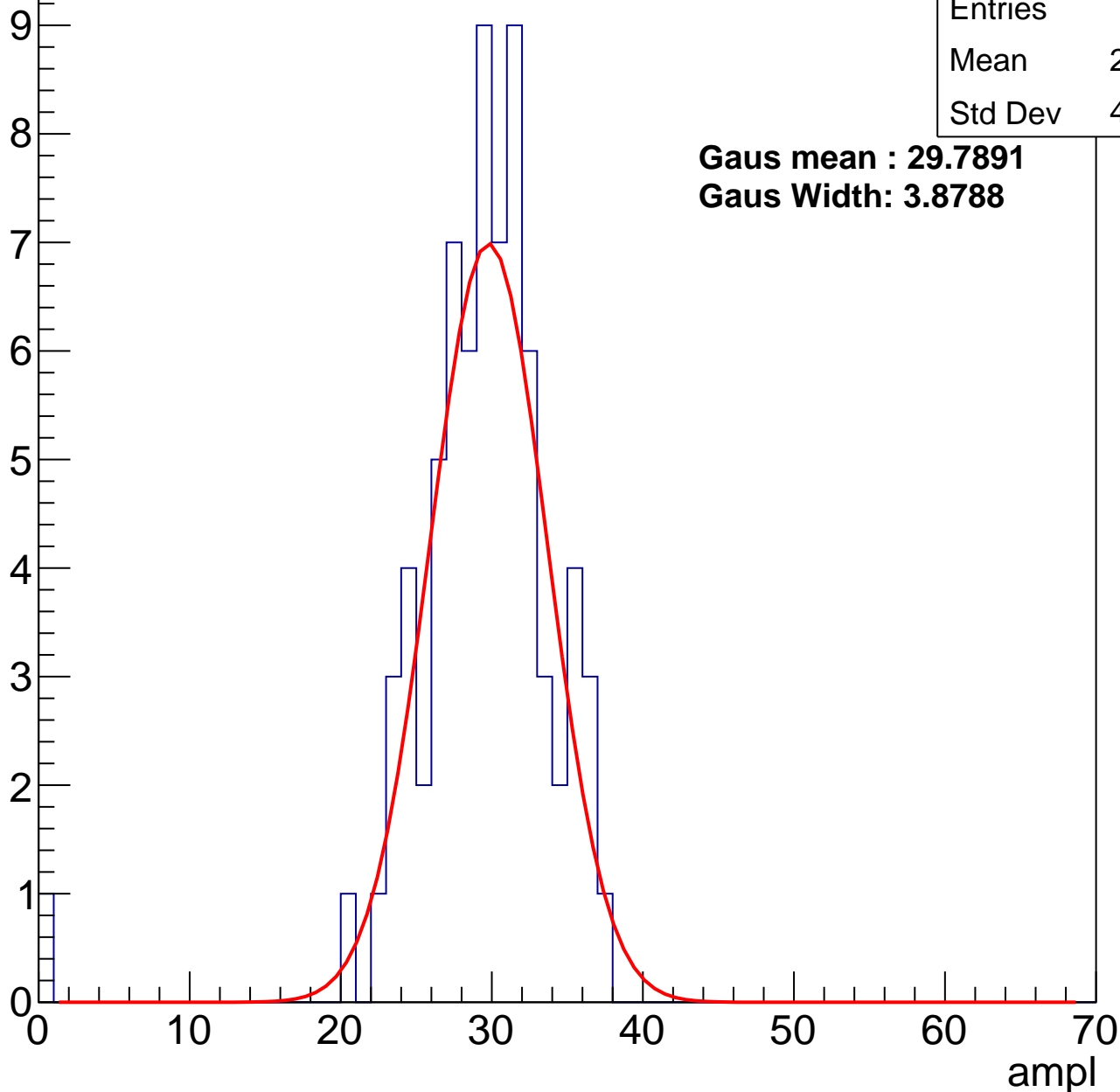
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	28.89
Std Dev	4.985

**Gaus mean : 29.7891**

**Gaus Width: 3.8788**



# B1L101S, U8-ch12, adc1

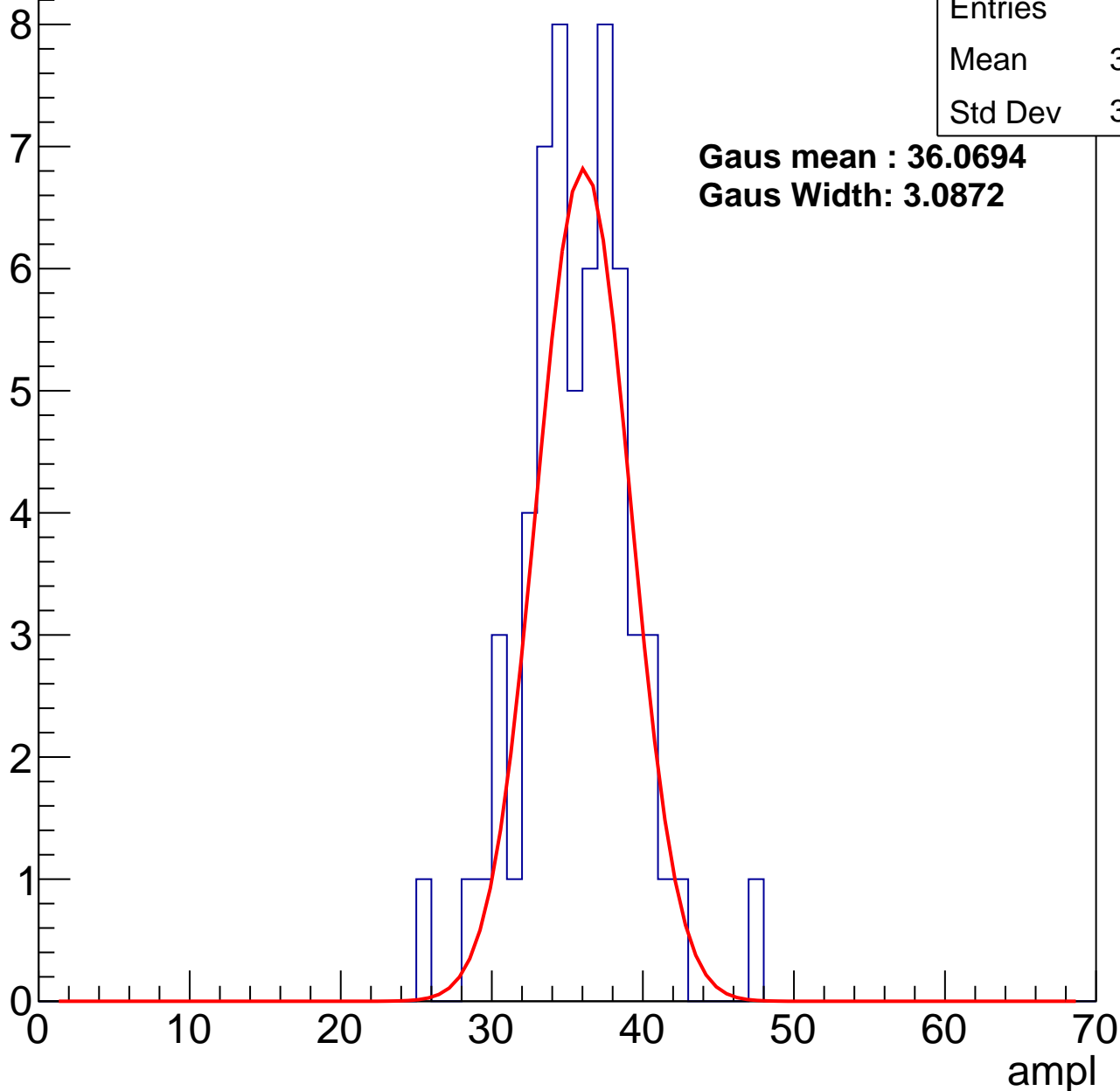
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	35.27
Std Dev	3.623

**Gaus mean : 36.0694**

**Gaus Width: 3.0872**



# B1L101S, U8-ch12, adc2

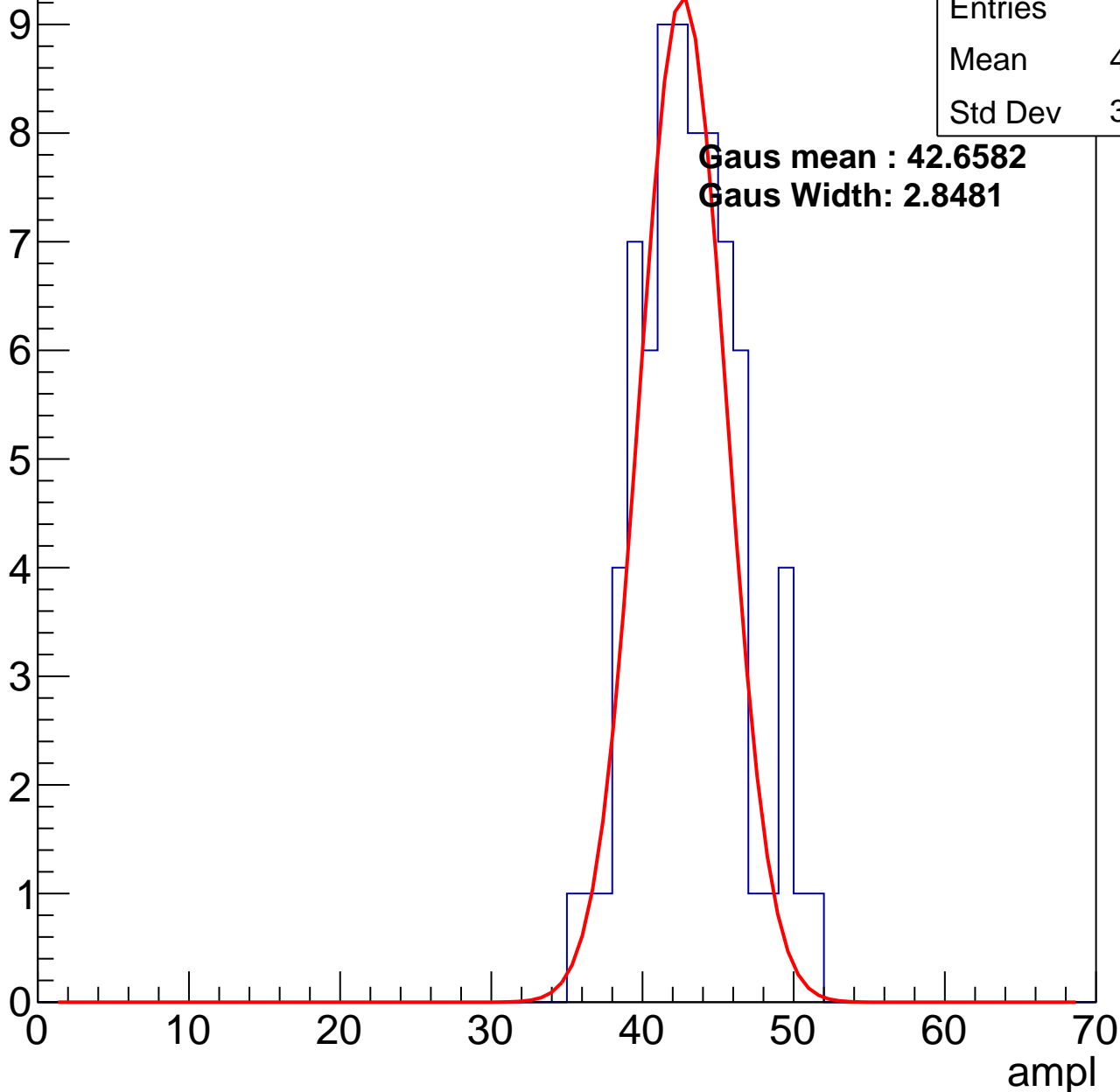
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	42.65
Std Dev	3.345

**Gaus mean : 42.6582**

**Gaus Width: 2.8481**

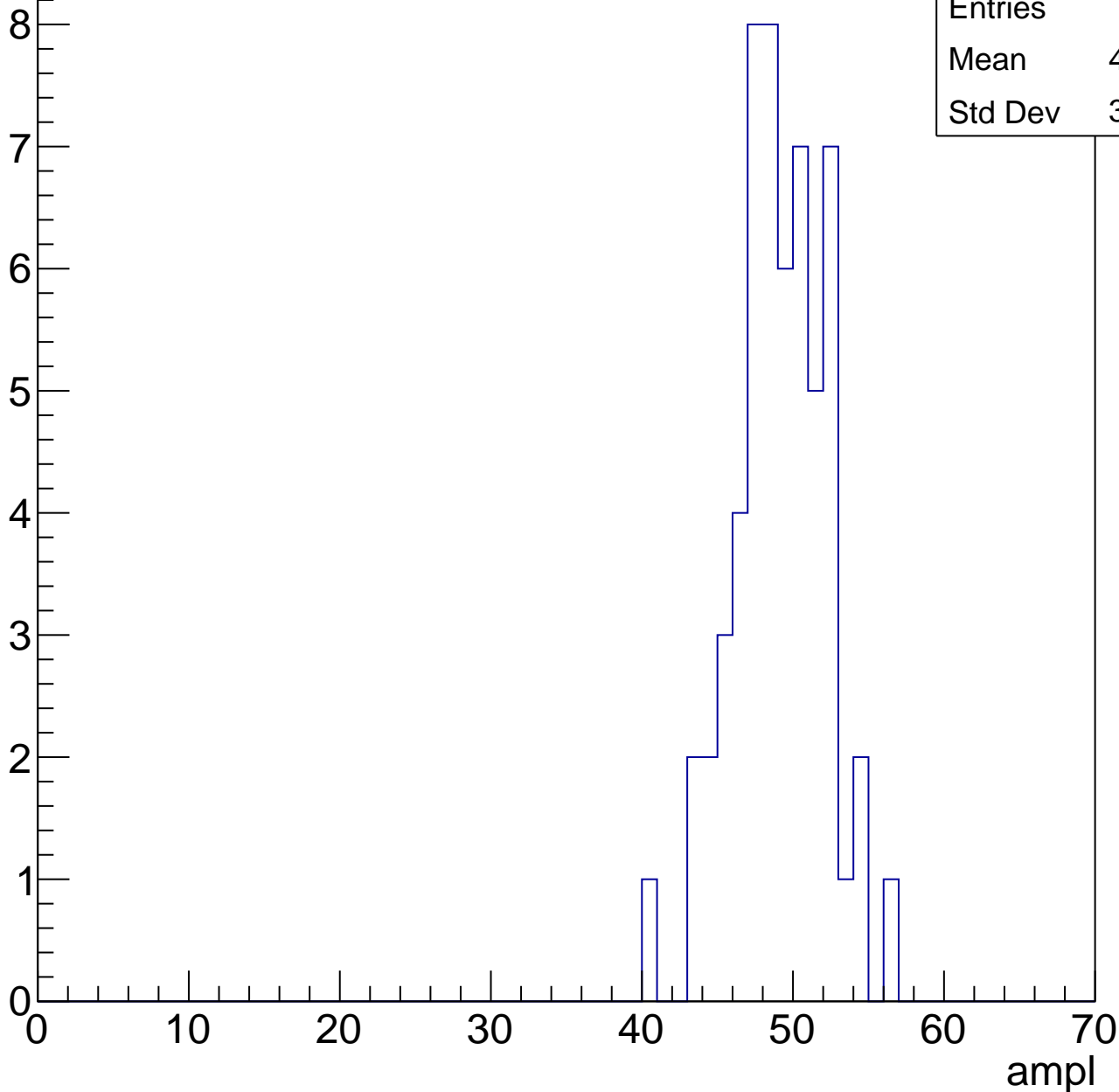


# B1L101S, U8-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	48.65
Std Dev	3.035



# B1L101S, U8-ch12, adc4

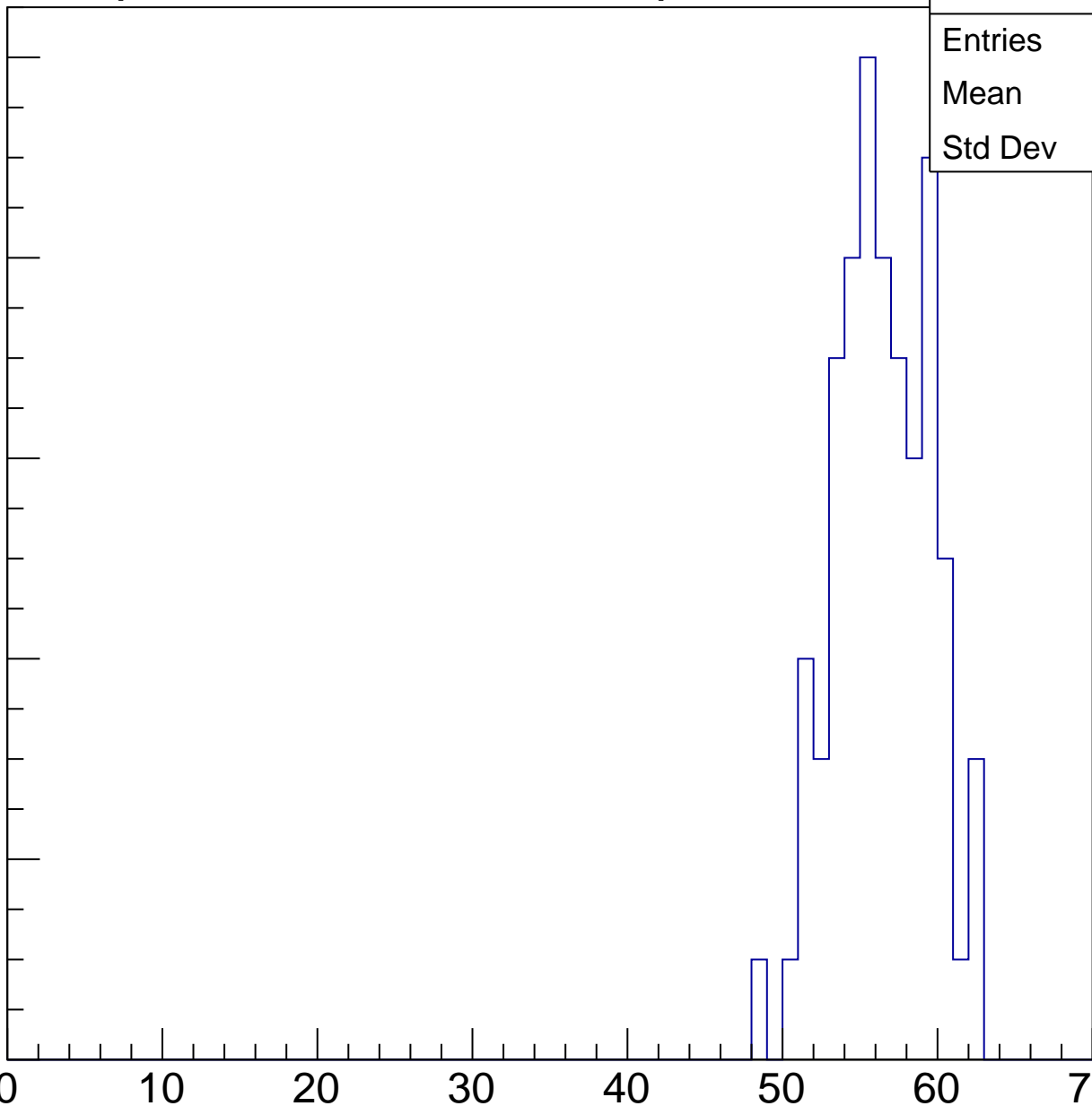
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

10  
8  
6  
4  
2  
0

Entries	73
Mean	55.95
Std Dev	3.047

ampl

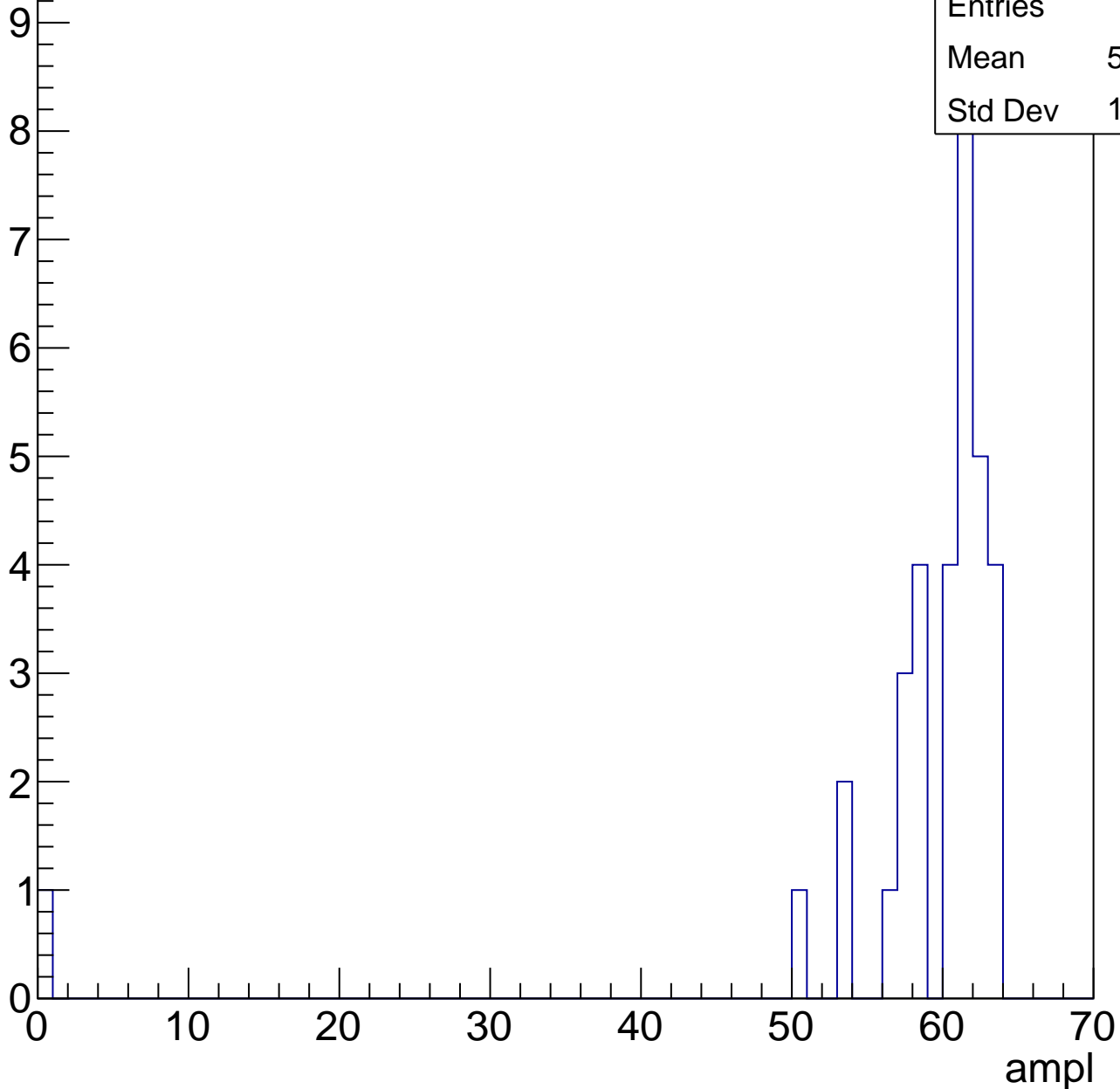


# B1L101S, U8-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	34
Mean	57.82
Std Dev	10.52

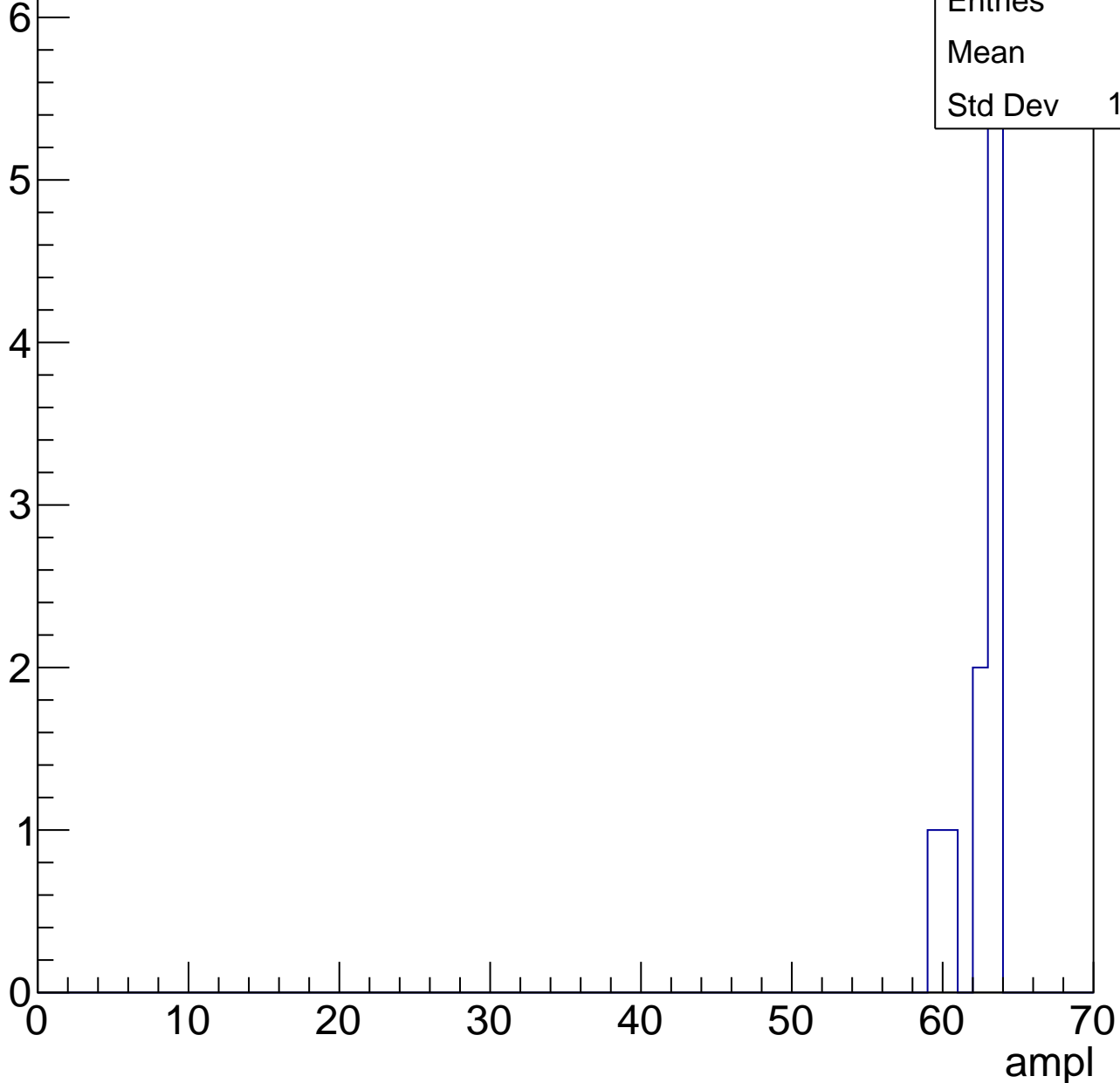


# B1L101S, U8-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	10
Mean	62.1
Std Dev	1.375





# B1L101S, U8-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U8-ch13, adc0

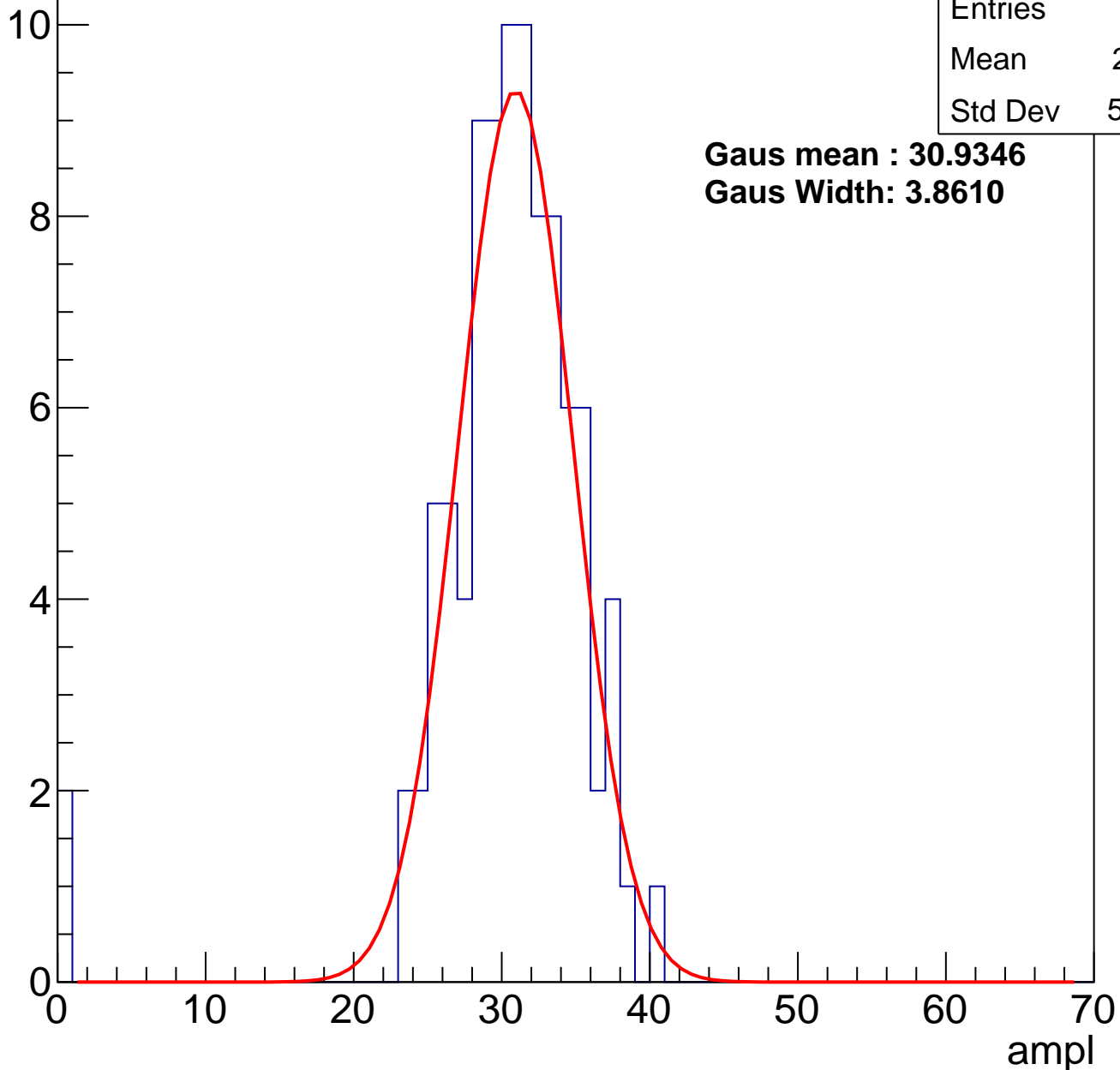
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	94
Mean	29.91
Std Dev	5.694

**Gaus mean : 30.9346**

**Gaus Width: 3.8610**

Entry



# B1L101S, U8-ch13, adc1

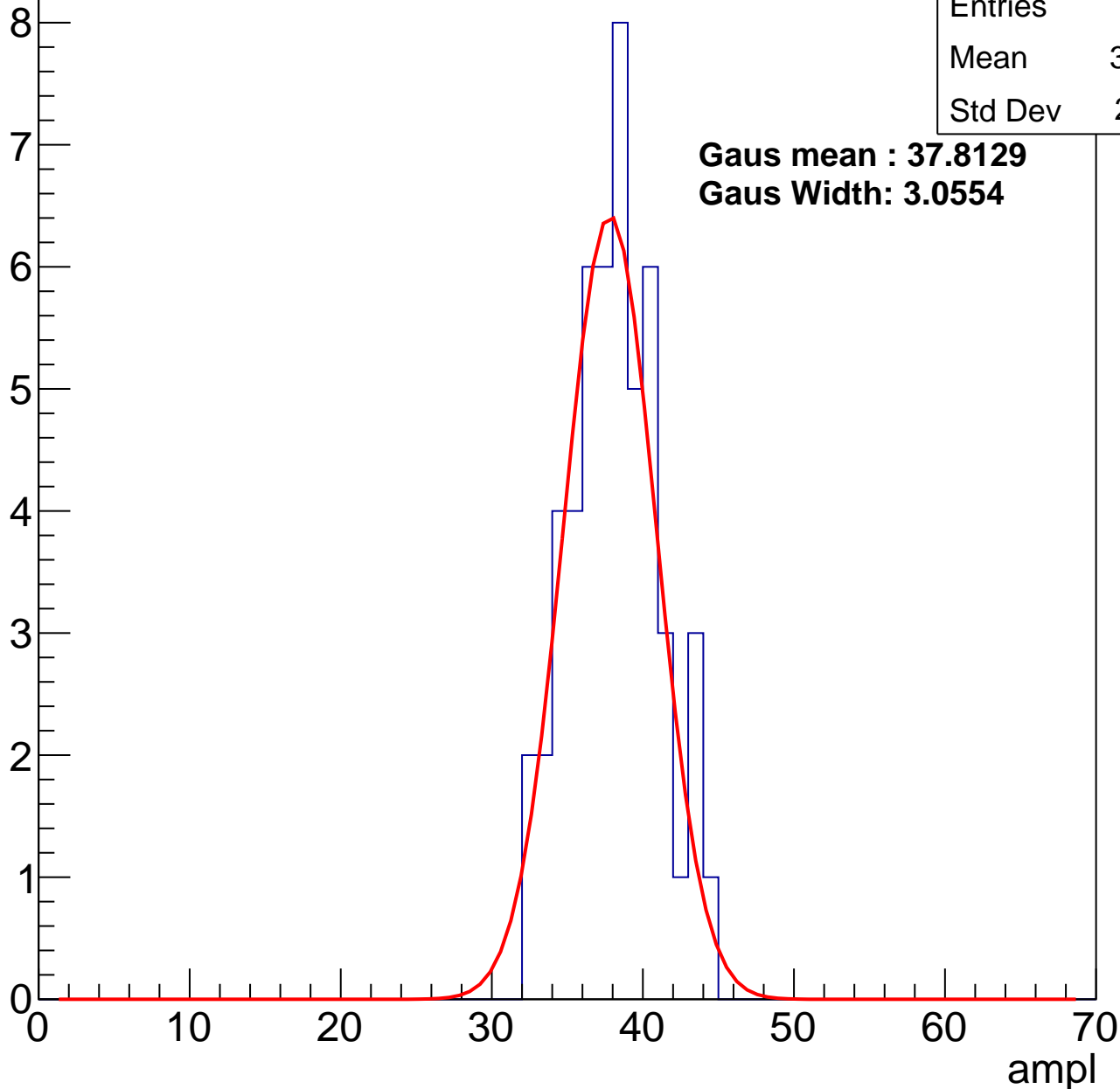
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	37.67
Std Dev	2.901

**Gaus mean : 37.8129**

**Gaus Width: 3.0554**



# B1L101S, U8-ch13, adc2

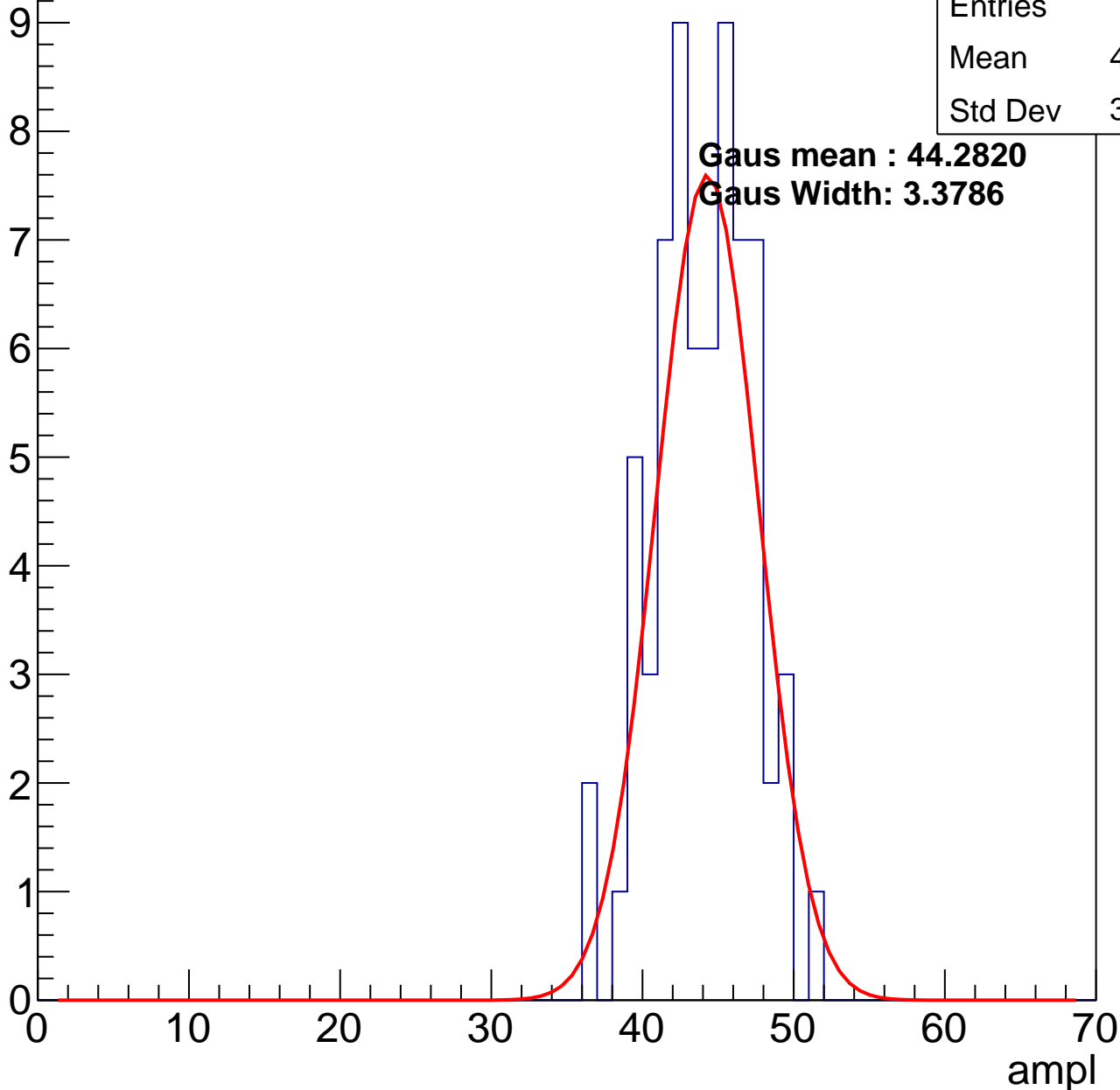
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	43.56
Std Dev	3.173

**Gaus mean : 44.2820**

**Gaus Width: 3.3786**



# B1L101S, U8-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	71
Mean	50.54
Std Dev	3.352

Entry

10

8

6

4

2

0

0

10

20

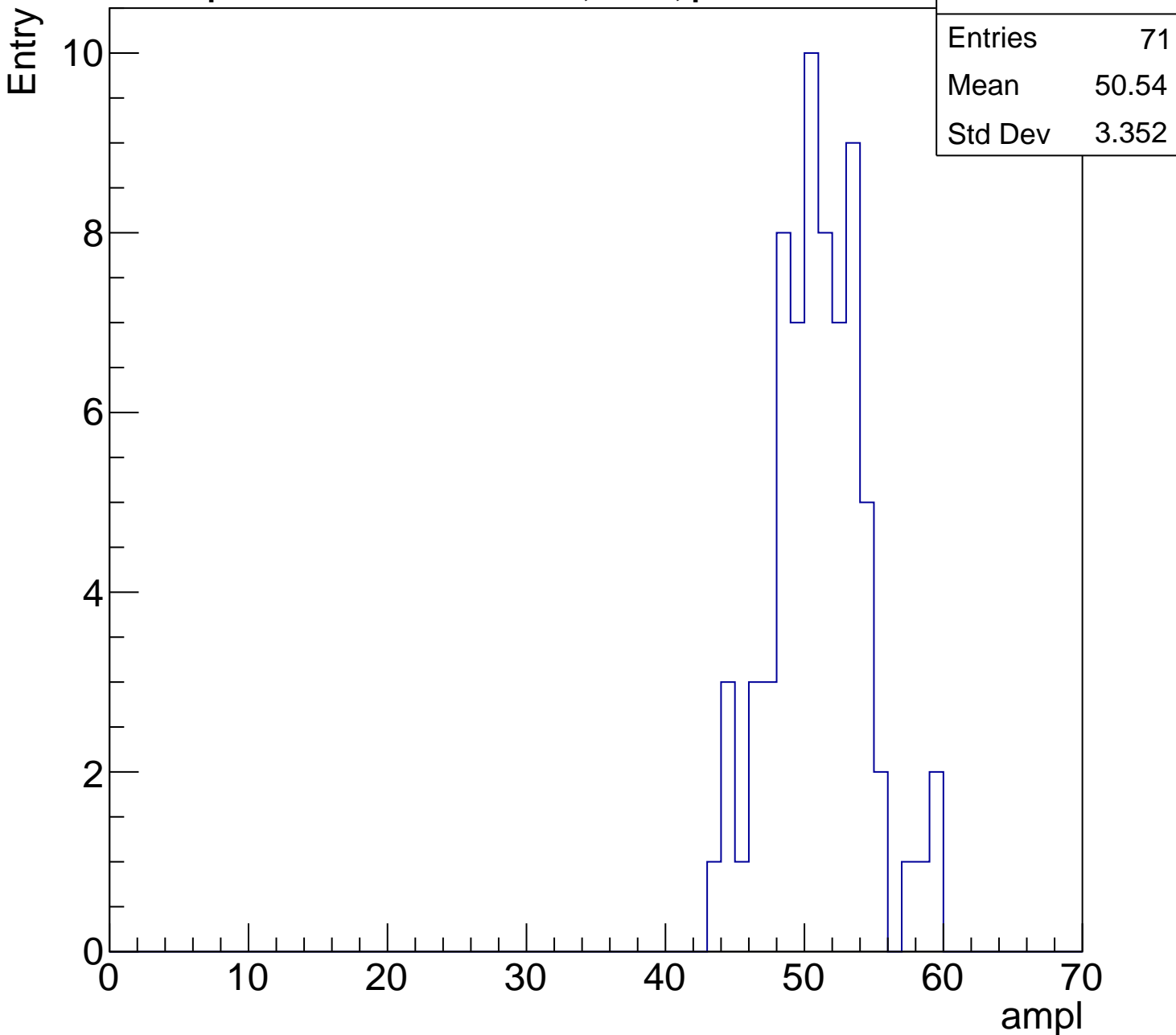
30

40

50

60

ampl

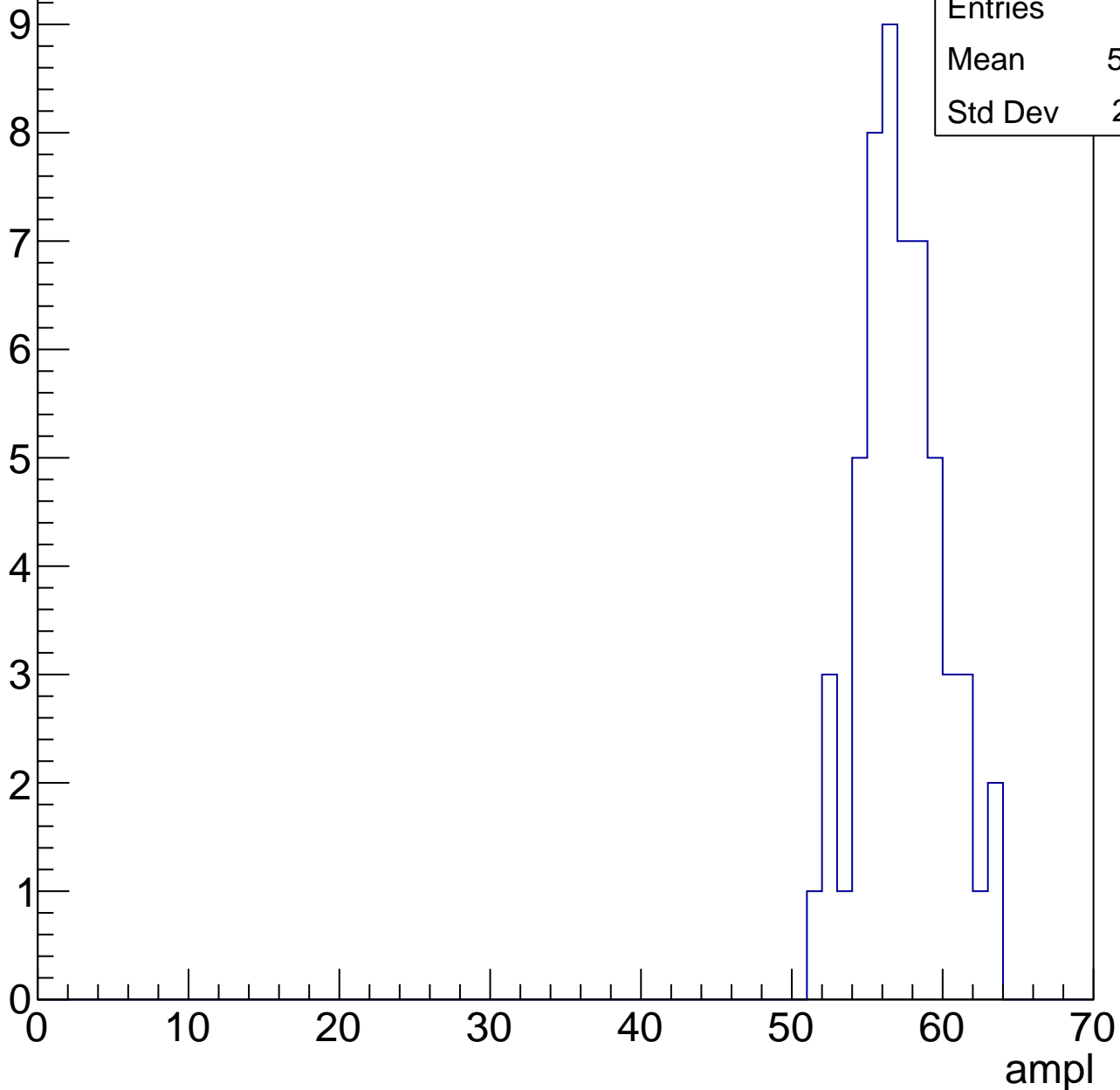


# B1L101S, U8-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	56.82
Std Dev	2.731



# B1L101S, U8-ch13, adc5

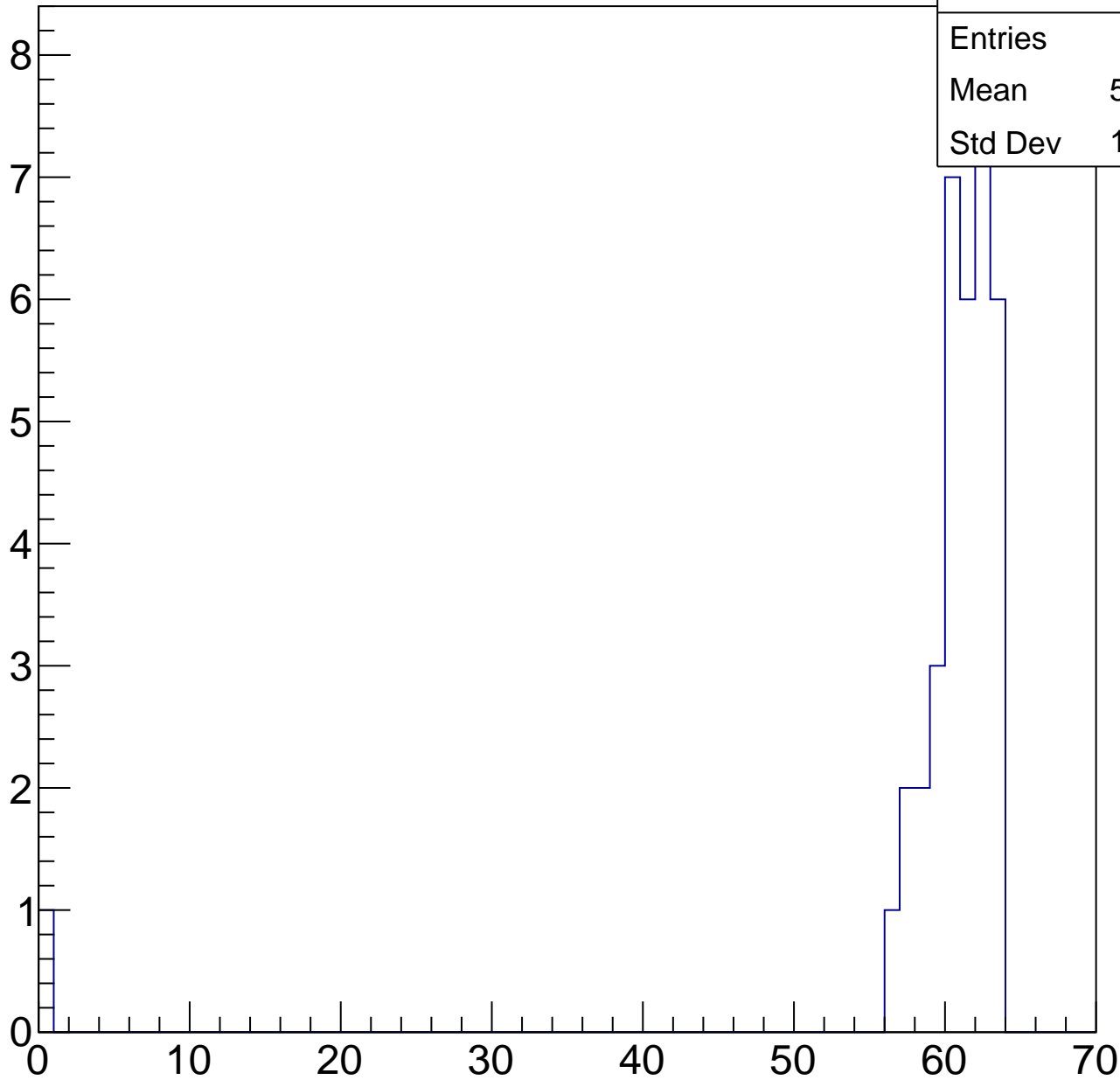
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	36
Mean	58.97
Std Dev	10.14

ampl



# B1L101S, U8-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U8-ch14, adc0

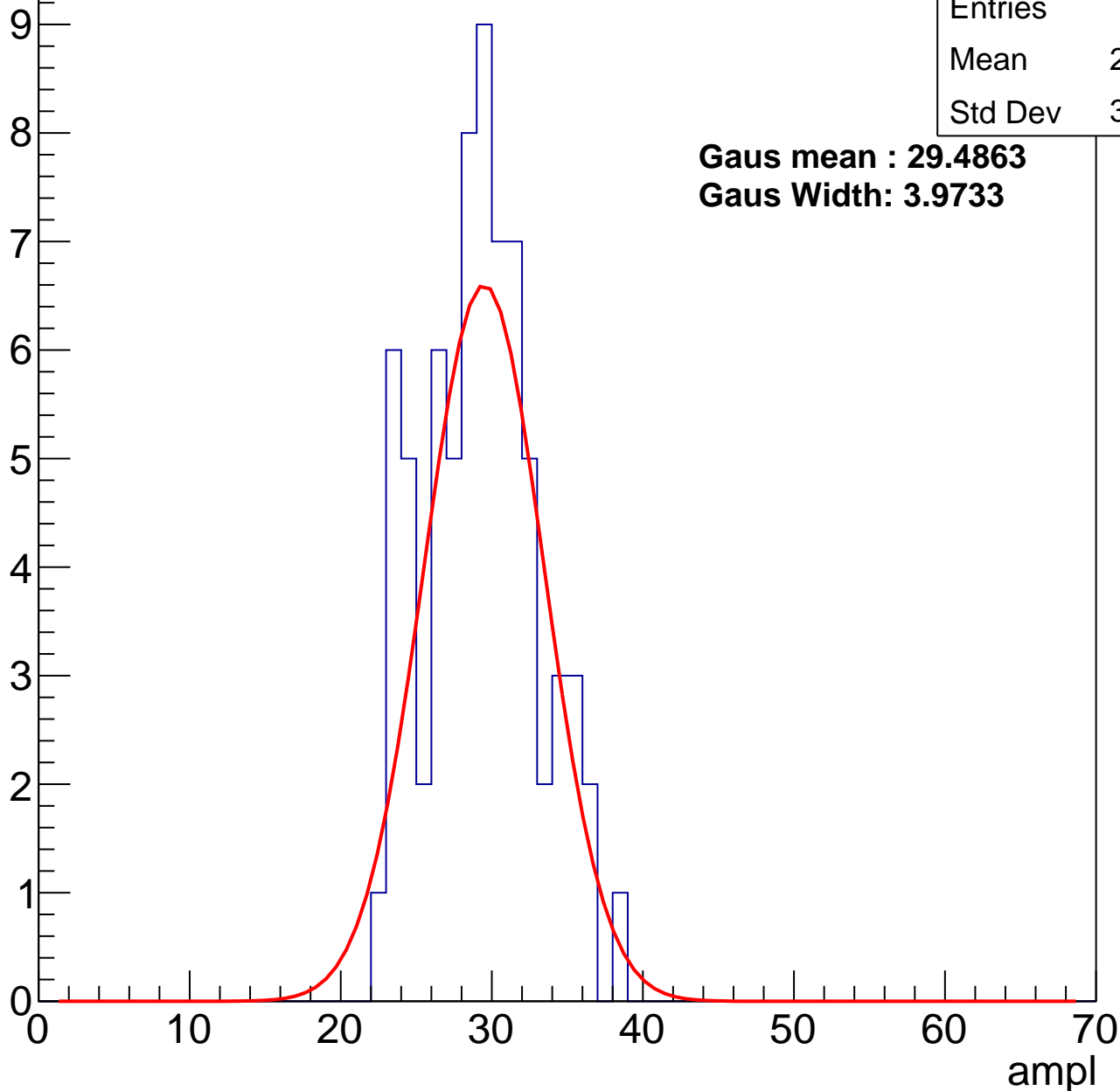
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	28.83
Std Dev	3.682

**Gaus mean : 29.4863**

**Gaus Width: 3.9733**



# B1L101S, U8-ch14, adc1

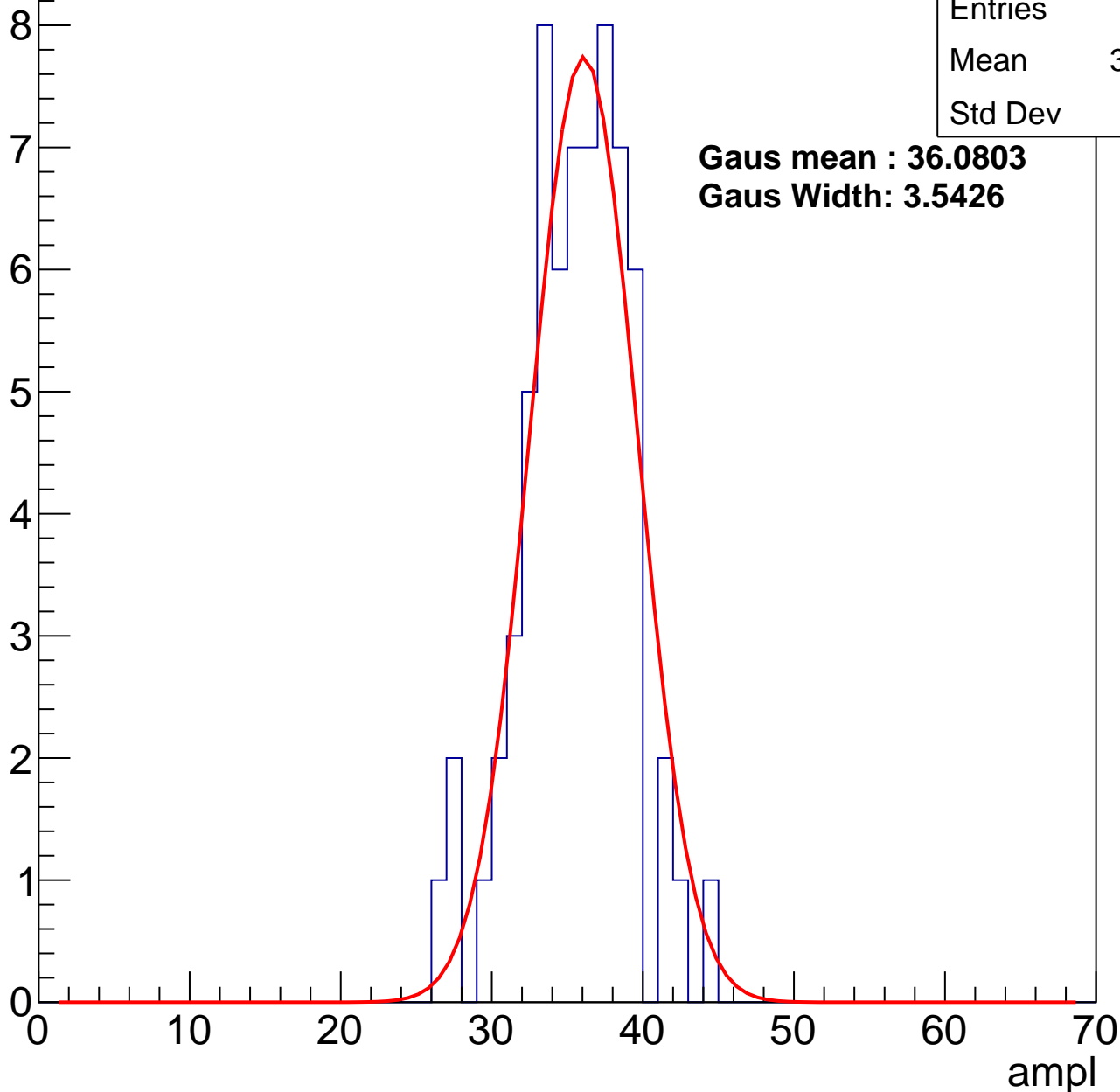
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	35.09
Std Dev	3.51

**Gaus mean : 36.0803**

**Gaus Width: 3.5426**



# B1L101S, U8-ch14, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	65
Mean	42.29
Std Dev	3.156

**Gaus mean : 42.9360**

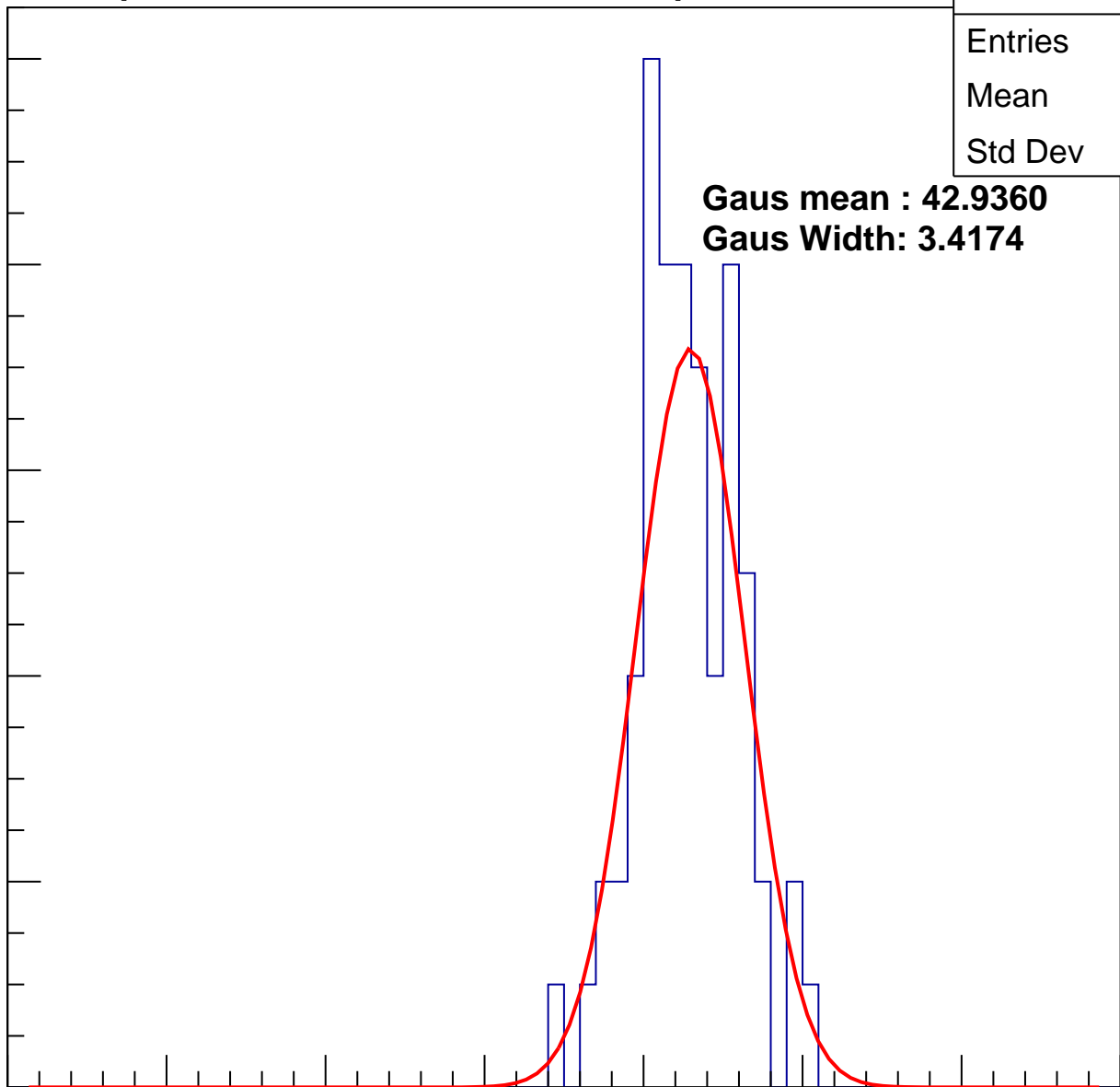
**Gaus Width: 3.4174**

Entry

10  
8  
6  
4  
2  
0

ampl

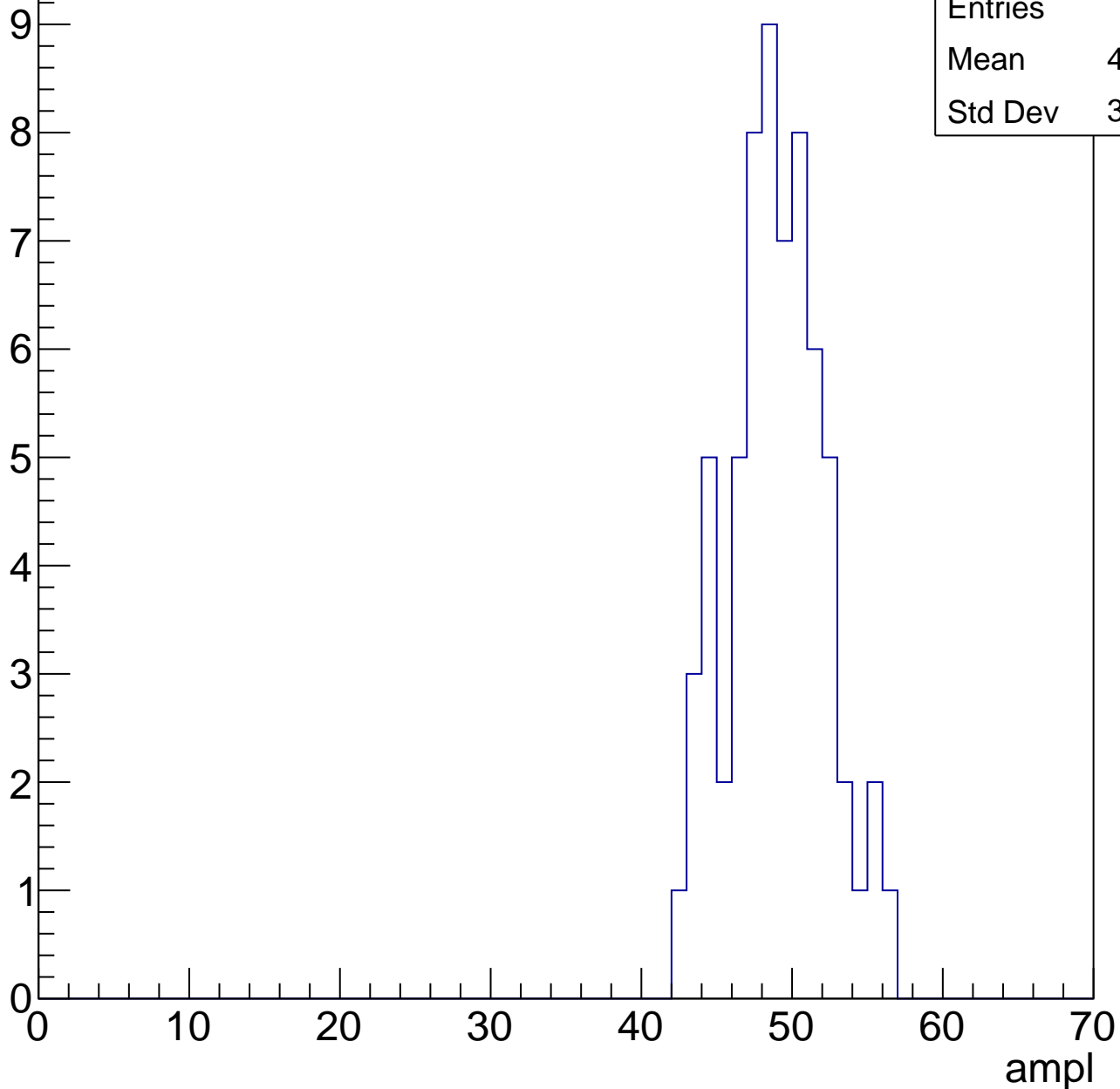
0 10 20 30 40 50 60 70



# B1L101S, U8-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	65
Mean	48.52
Std Dev	3.138

# B1L101S, U8-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

Entries 49

Mean 54.76

Std Dev 3.101

ampl

0

10

20

30

40

50

60

70

0

1

2

3

4

5

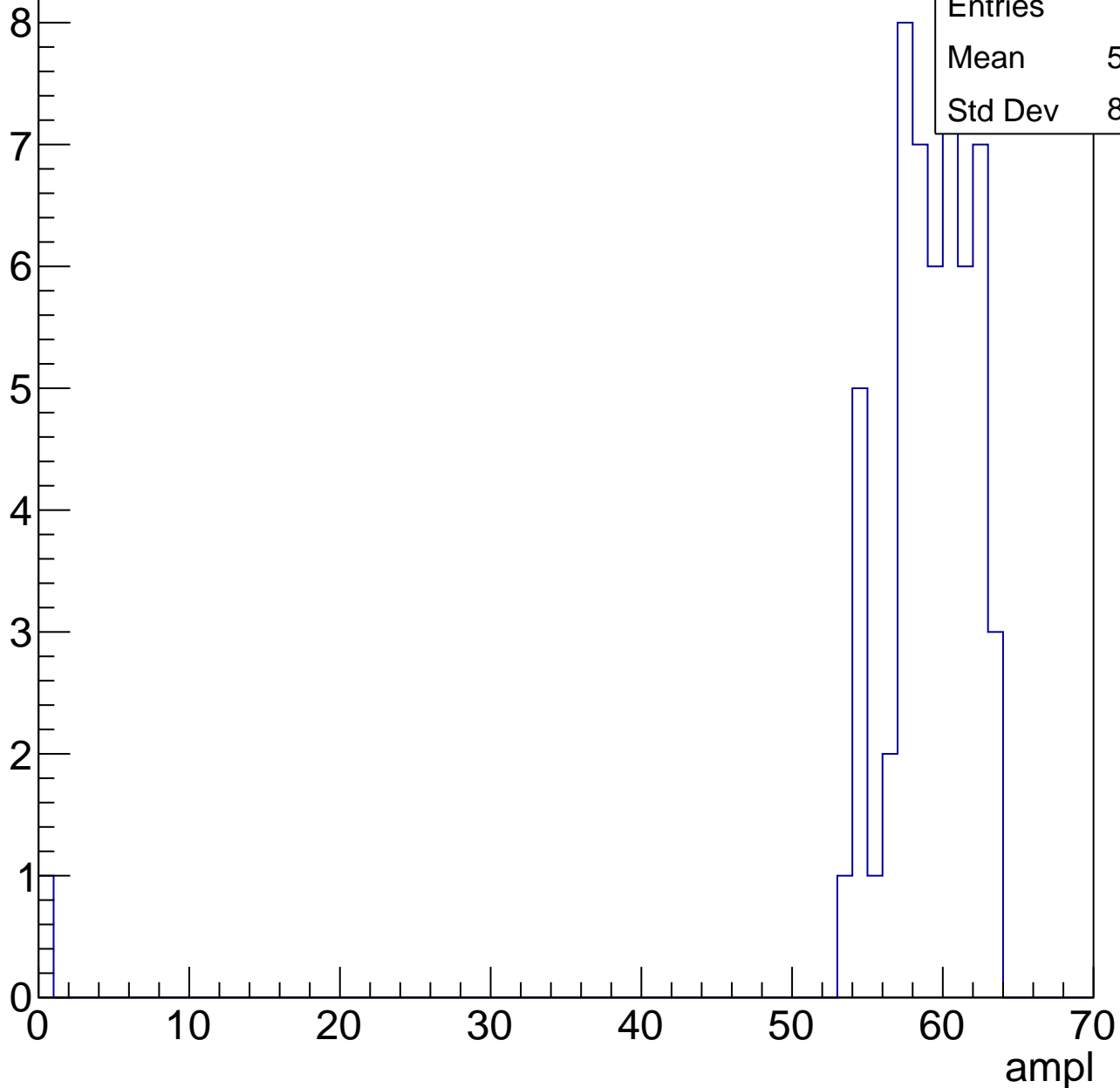
6

7

# B1L101S, U8-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

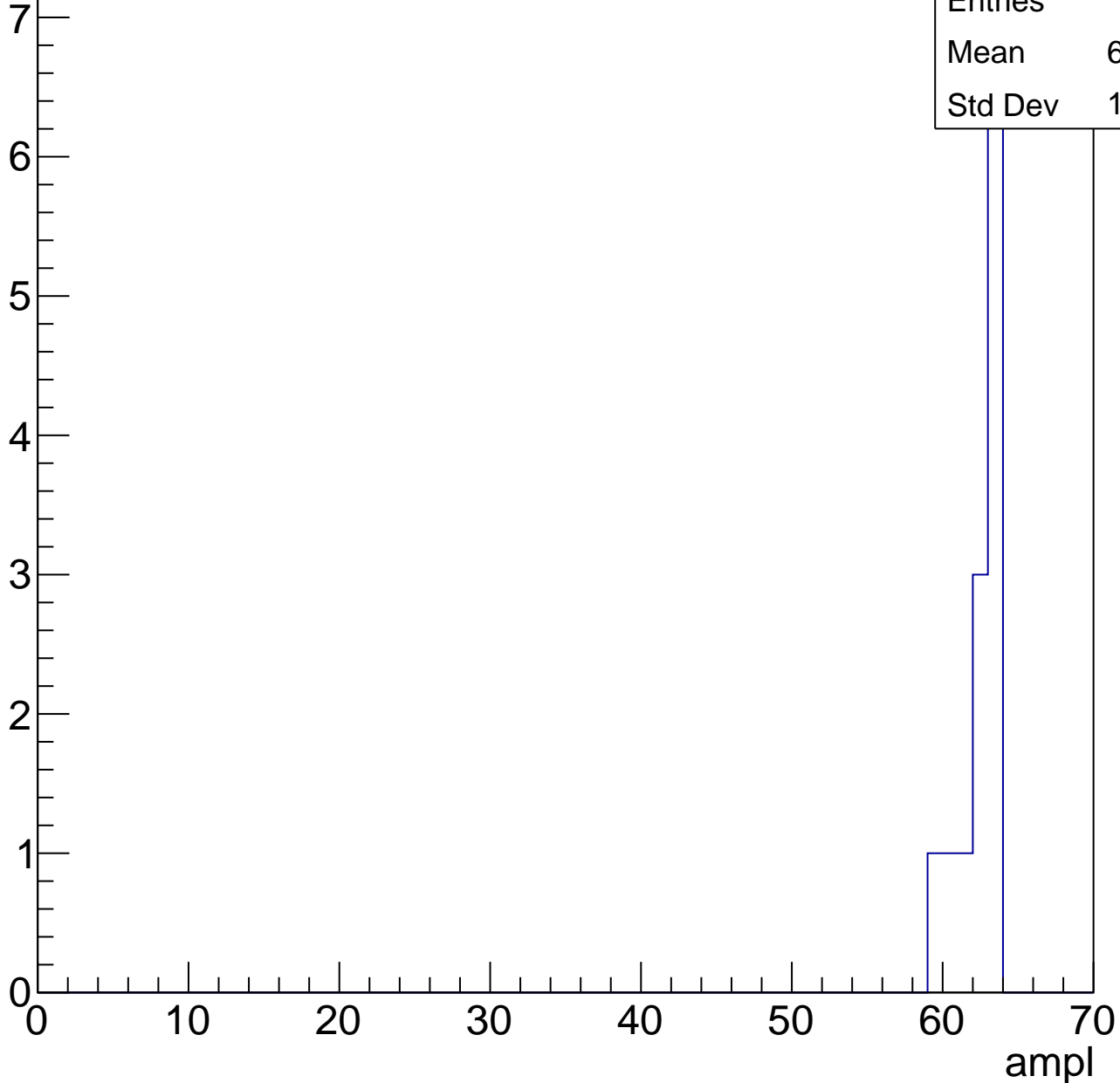
Entry



# B1L101S, U8-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	10
Std Dev	10

# B1L101S, U8-ch15, adc0

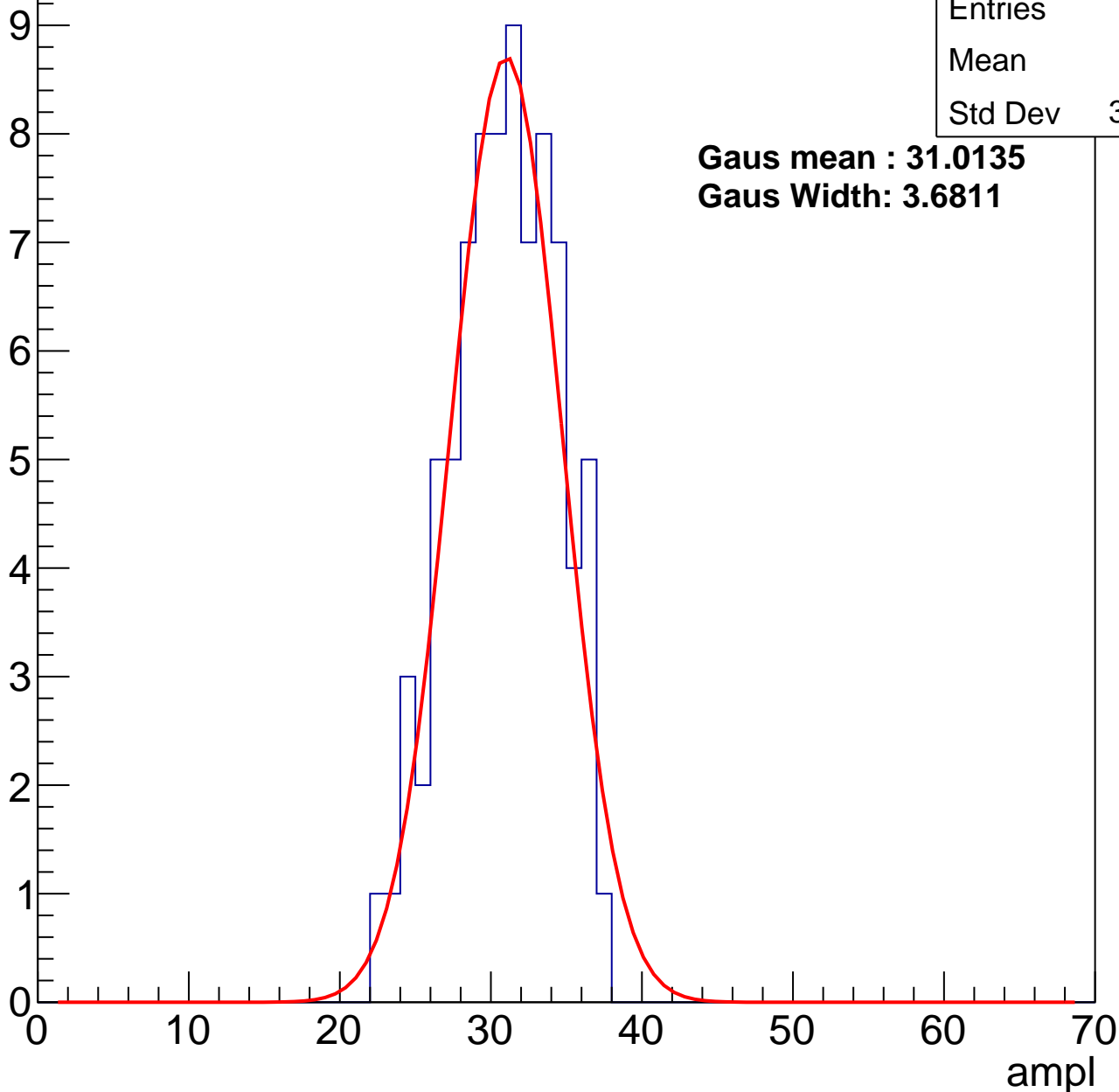
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	30.4
Std Dev	3.459

**Gaus mean : 31.0135**

**Gaus Width: 3.6811**



# B1L101S, U8-ch15, adc1

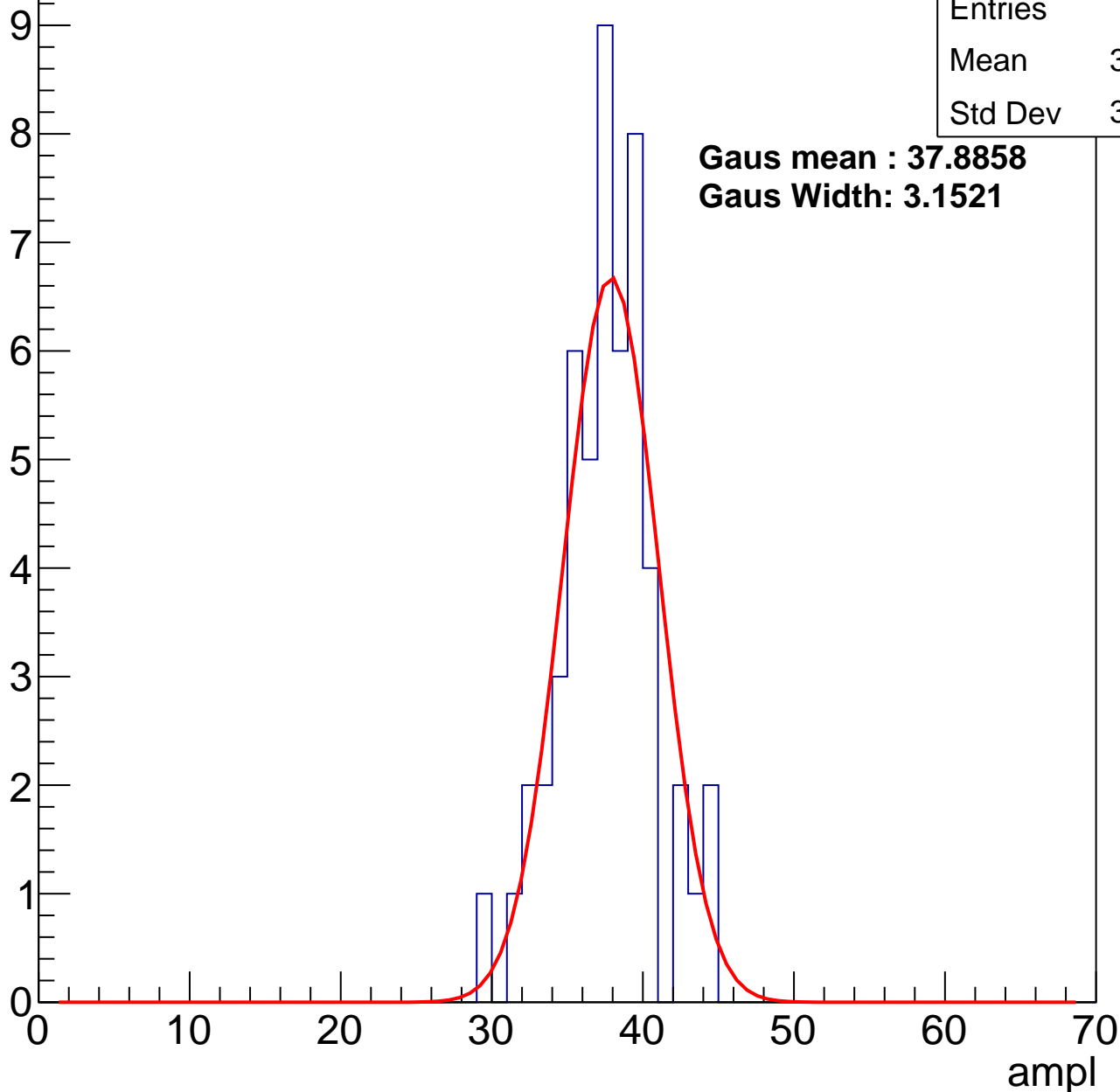
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	37.12
Std Dev	3.086

**Gaus mean : 37.8858**

**Gaus Width: 3.1521**



# B1L101S, U8-ch15, adc2

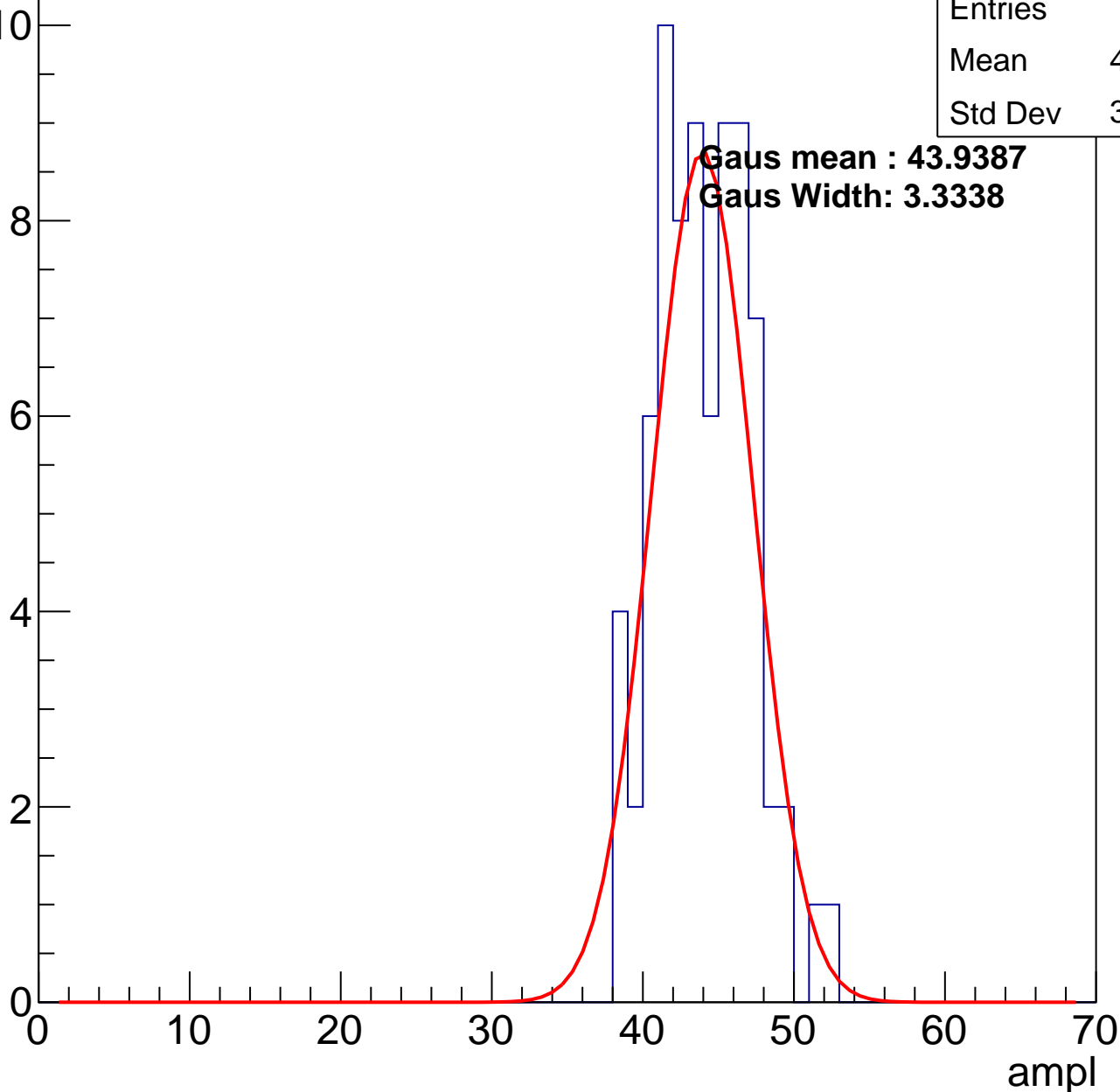
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	43.58
Std Dev	3.058

**Gaus mean : 43.9387**

**Gaus Width: 3.3338**

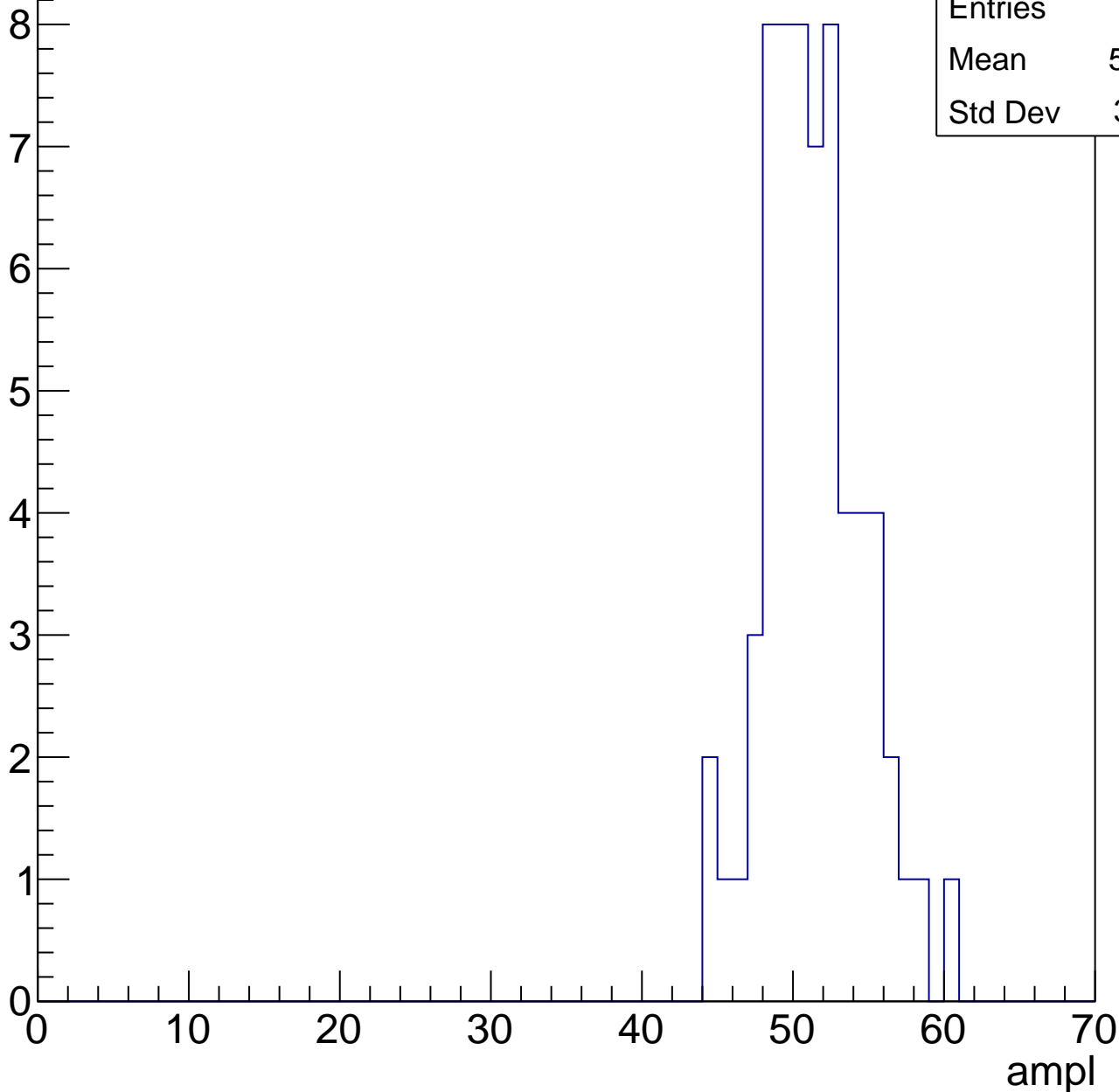


# B1L101S, U8-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

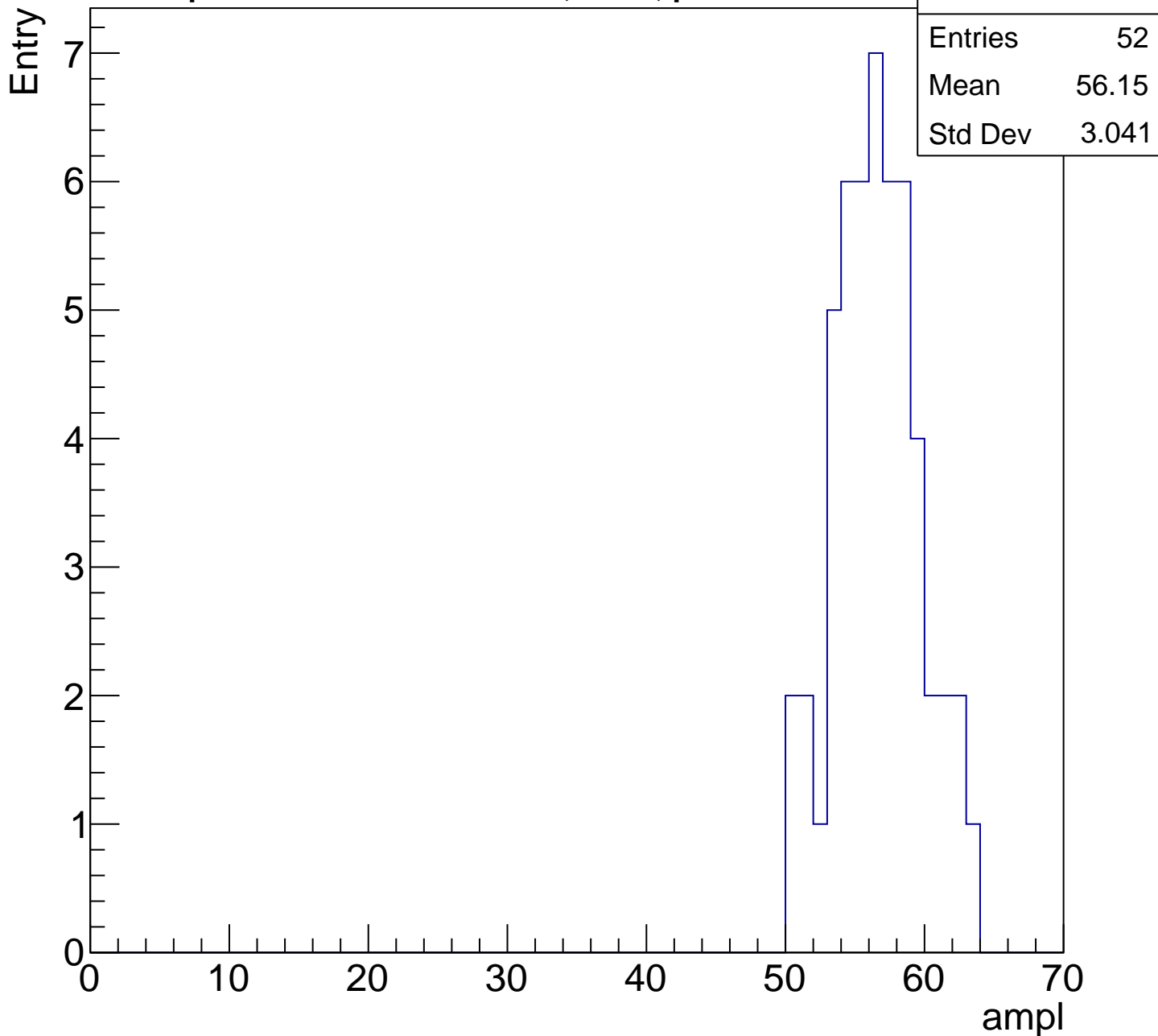
Entry

Entries	63
Mean	50.86
Std Dev	3.231



# B1L101S, U8-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

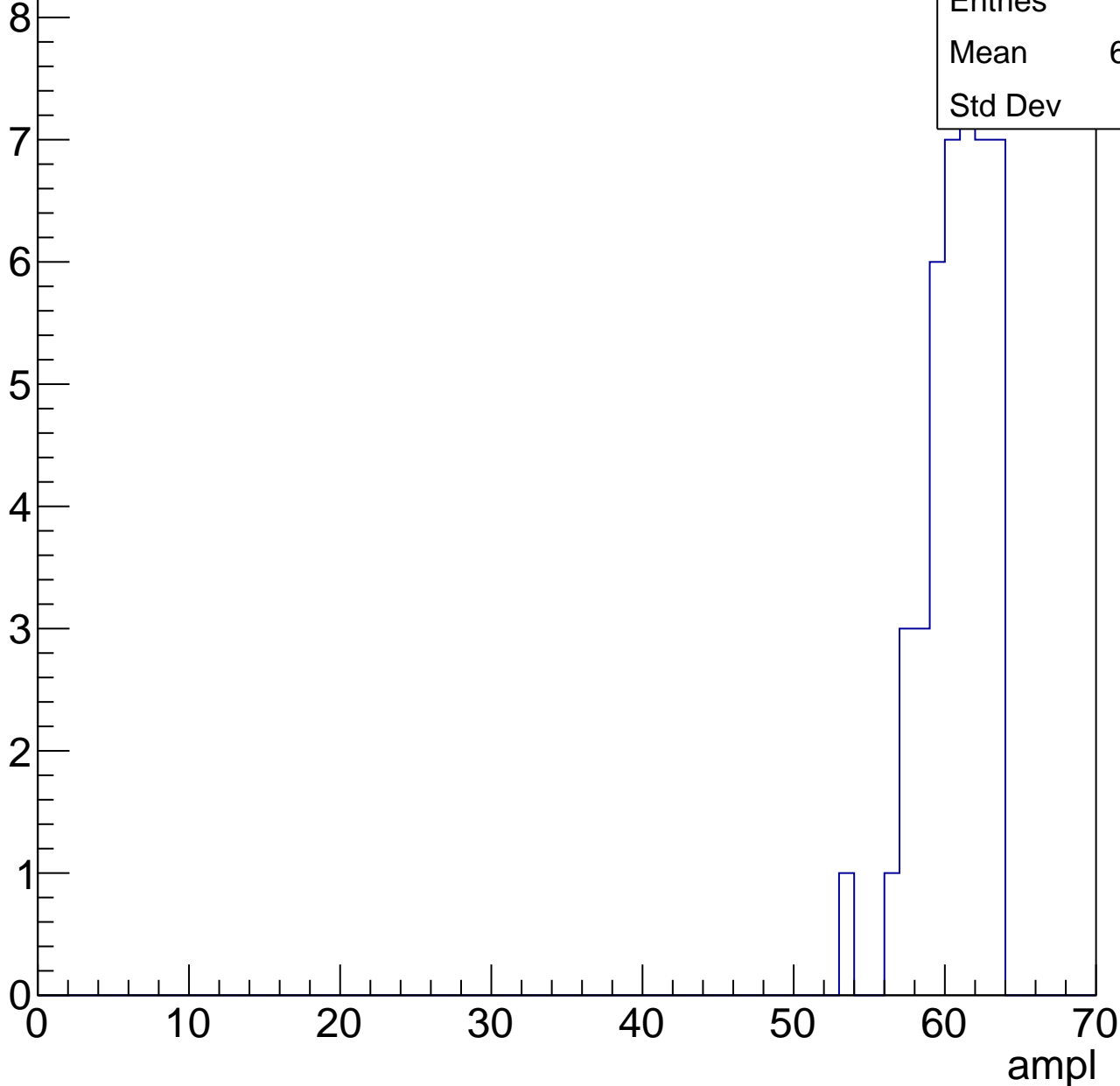


# B1L101S, U8-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	60.26
Std Dev	2.19



# B1L101S, U8-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch16, adc0

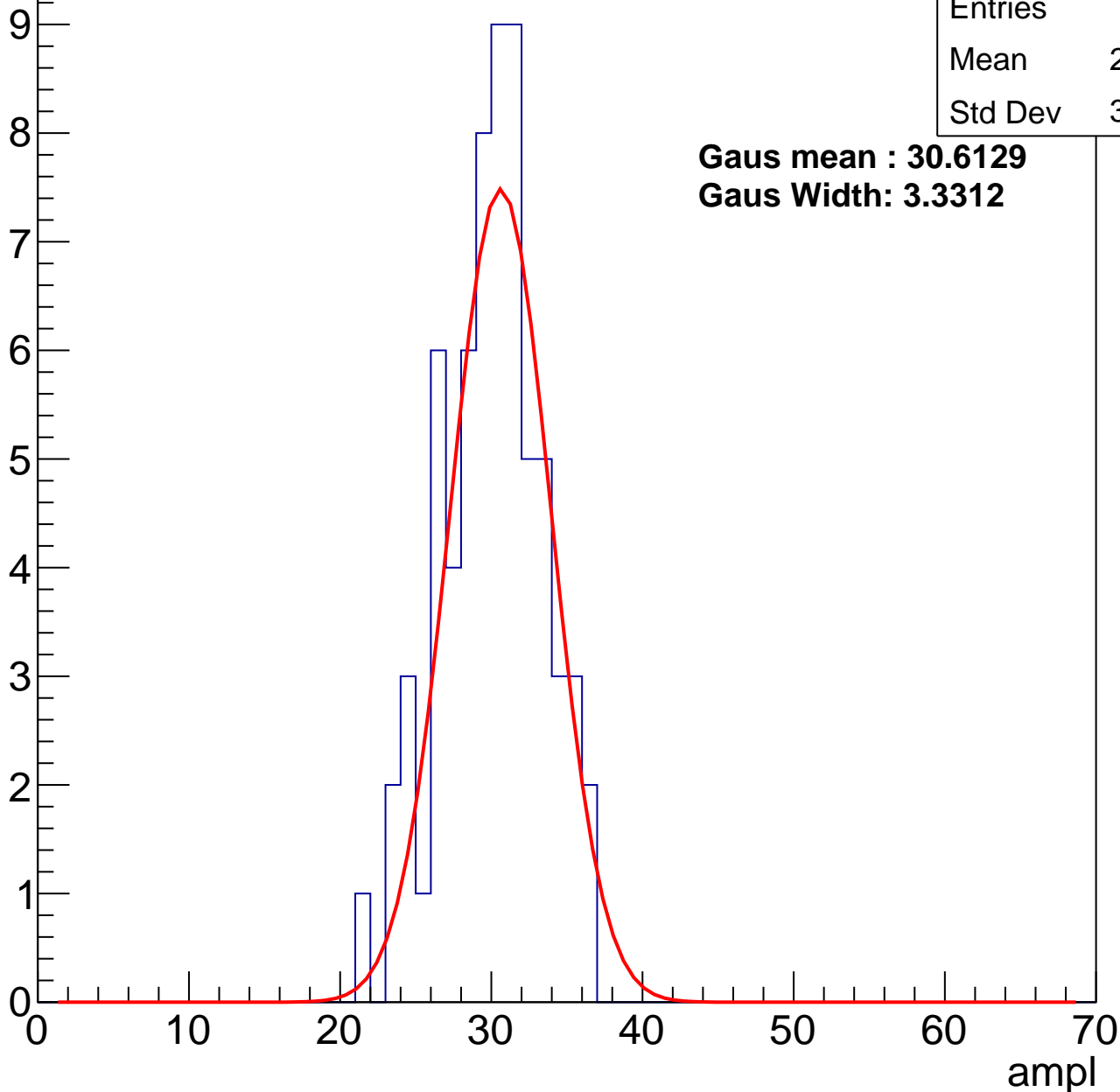
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	29.57
Std Dev	3.306

**Gaus mean : 30.6129**

**Gaus Width: 3.3312**



# B1L101S, U8-ch16, adc1

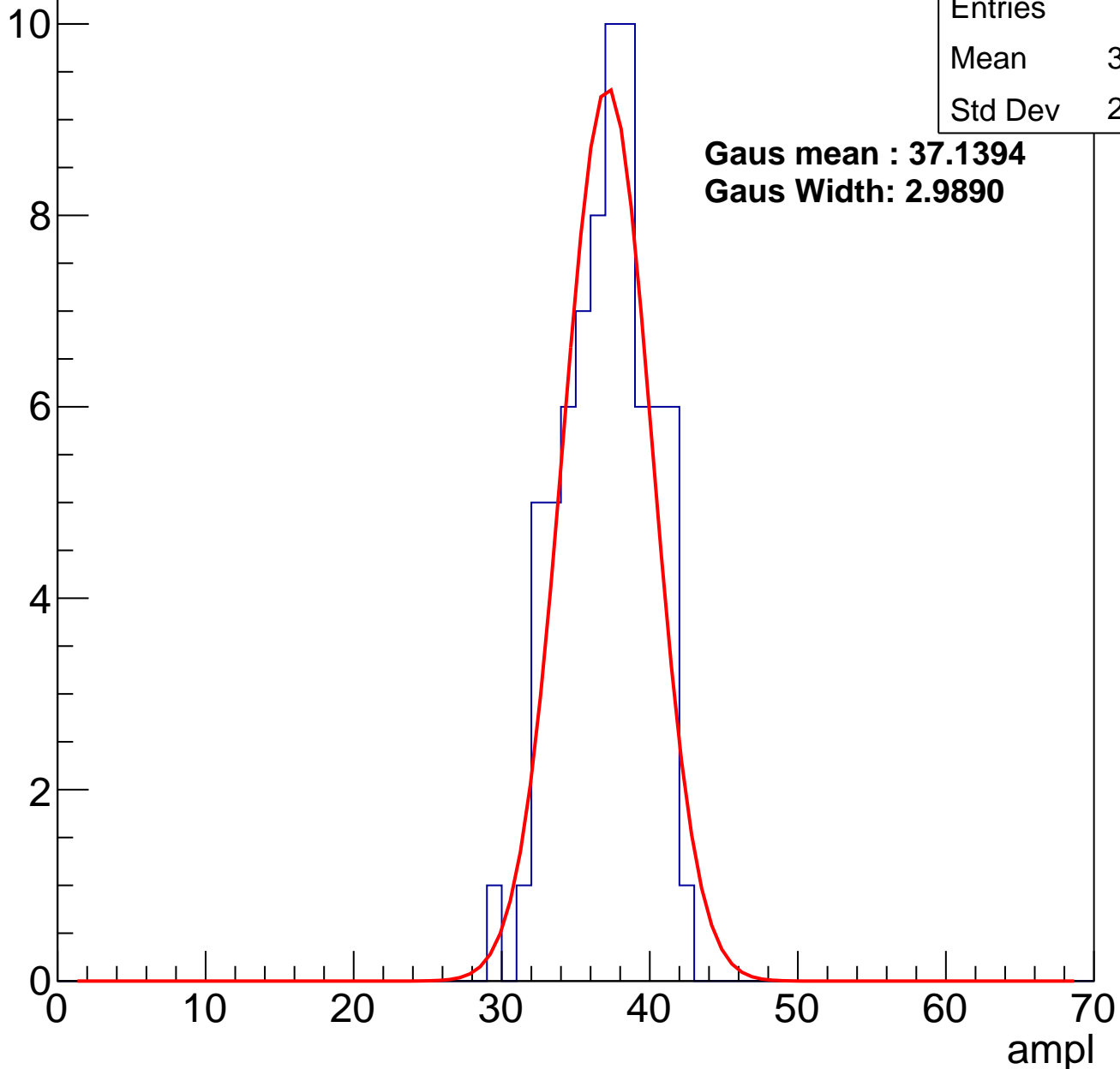
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	72
Mean	36.58
Std Dev	2.866

**Gaus mean : 37.1394**

**Gaus Width: 2.9890**

Entry



# B1L101S, U8-ch16, adc2

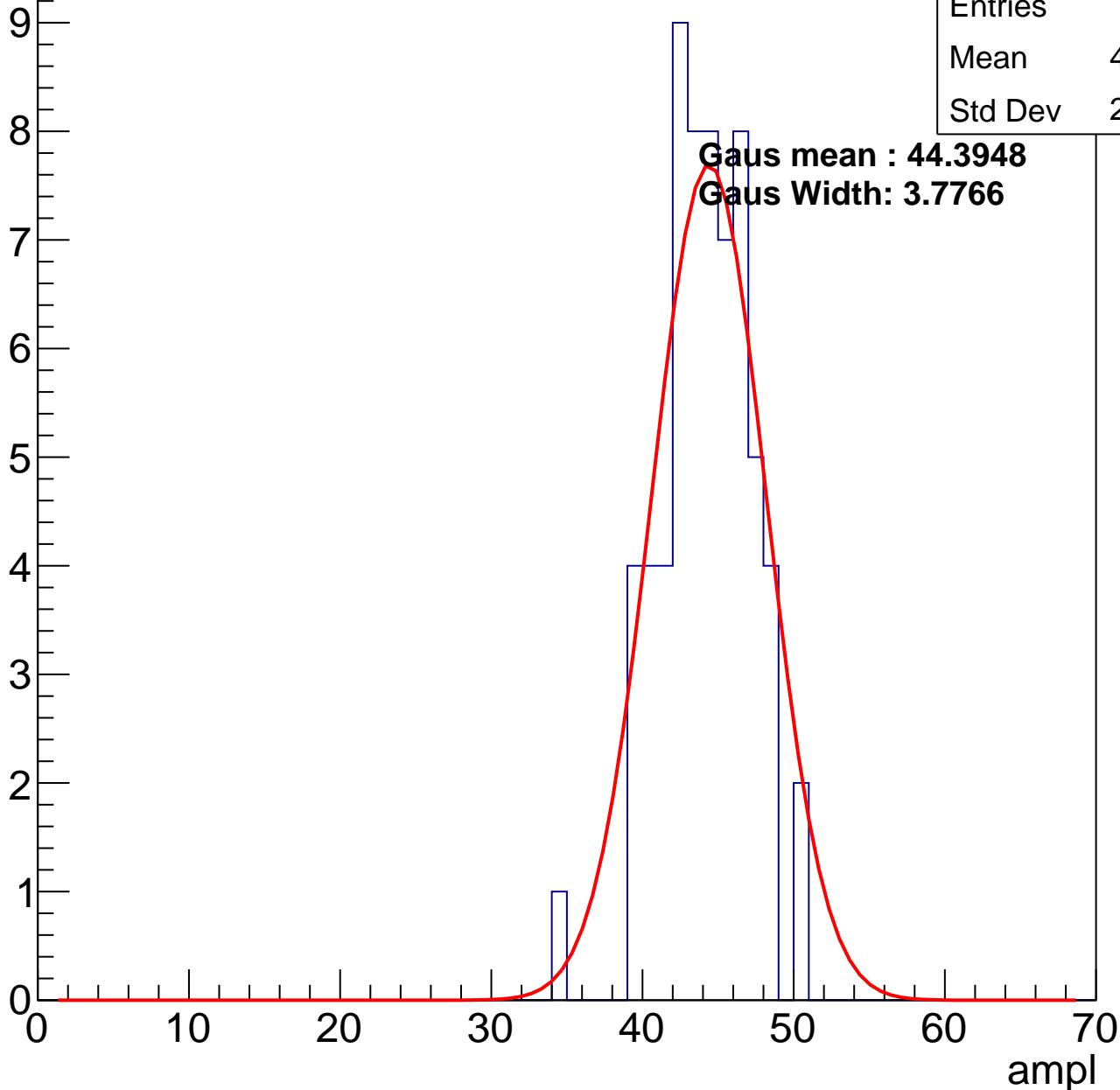
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	43.72
Std Dev	2.955

**Gaus mean : 44.3948**

**Gaus Width: 3.7766**

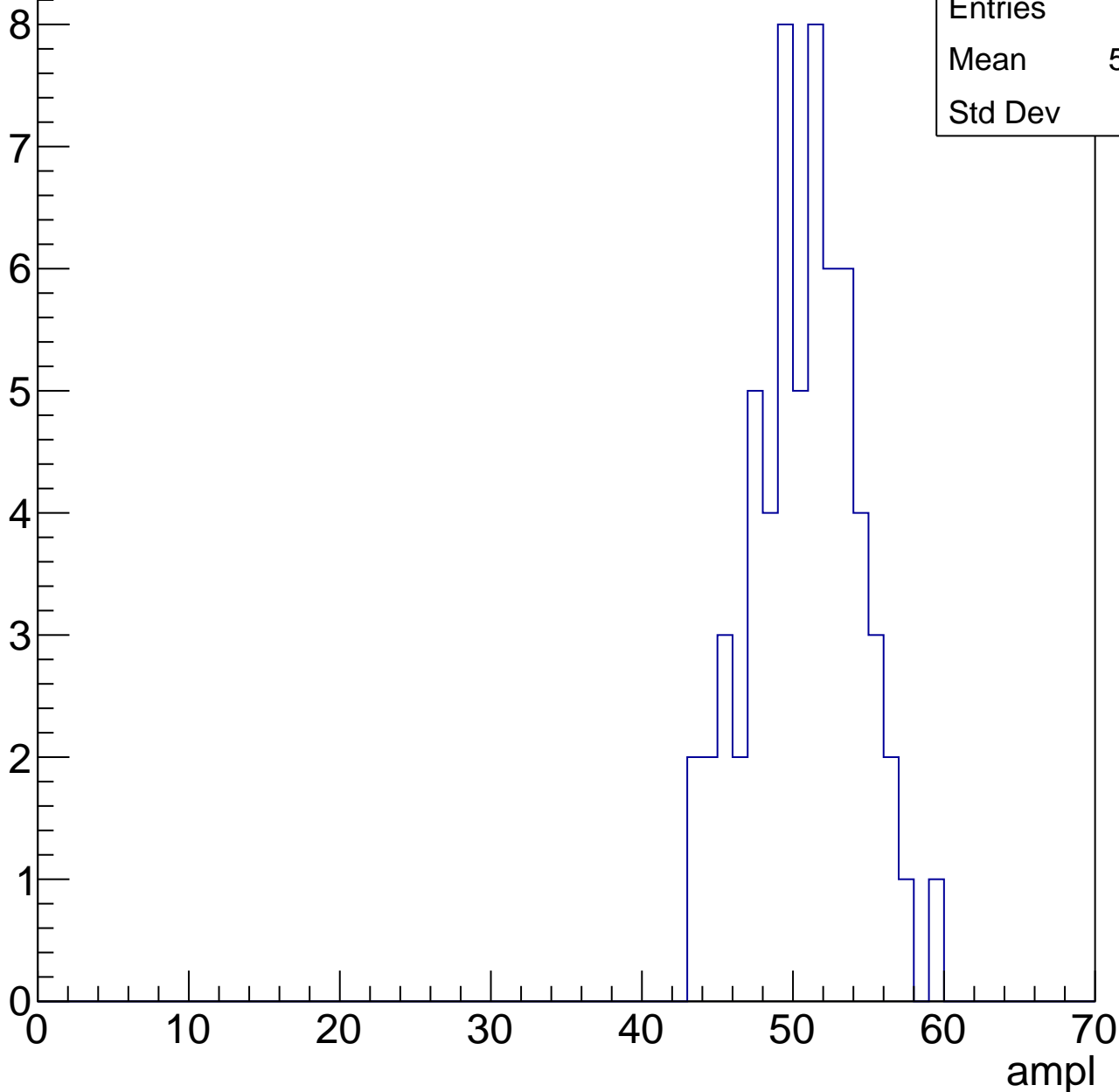


# B1L101S, U8-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

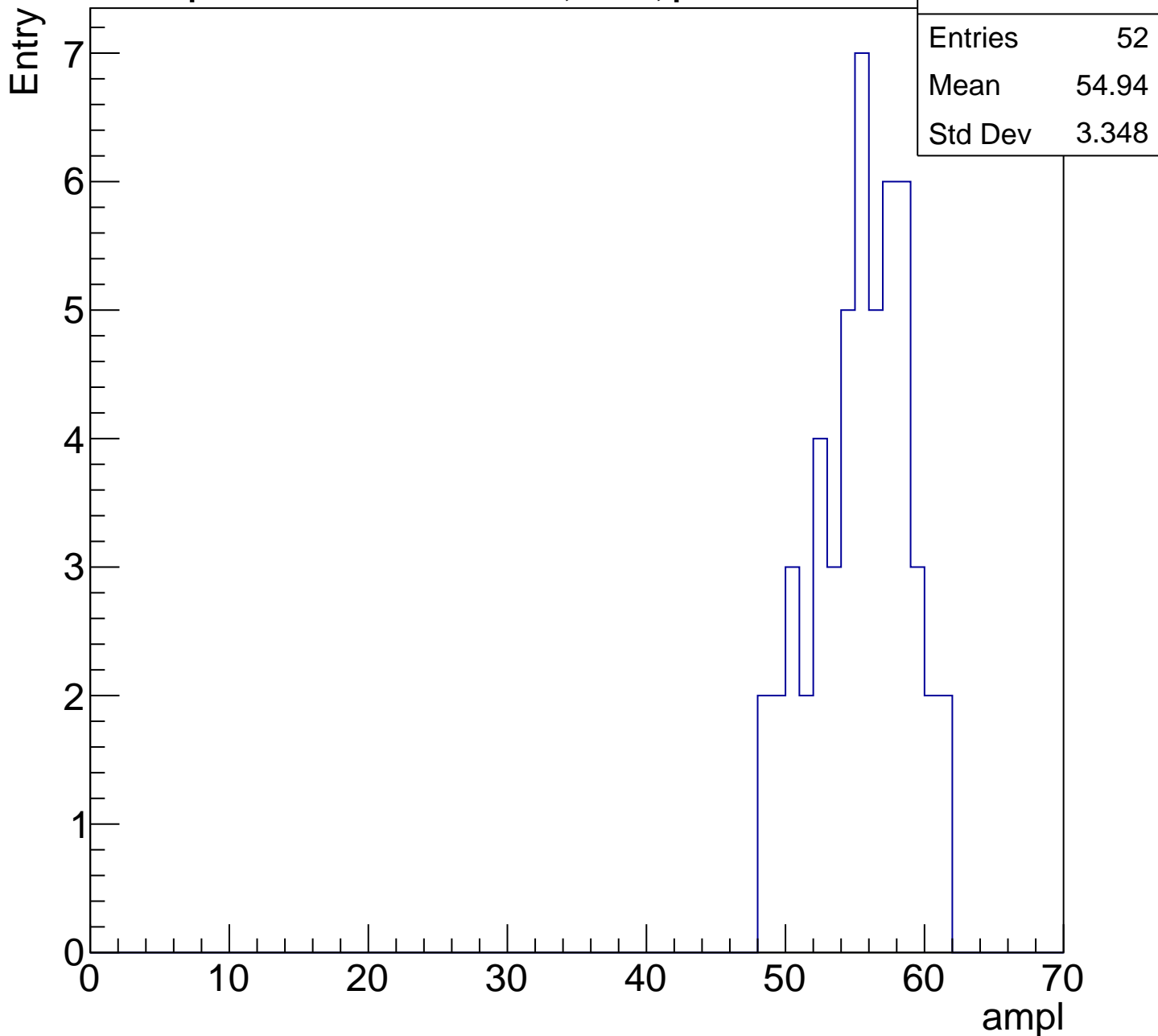
Entry

Entries	62
Mean	50.27
Std Dev	3.52



# B1L101S, U8-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

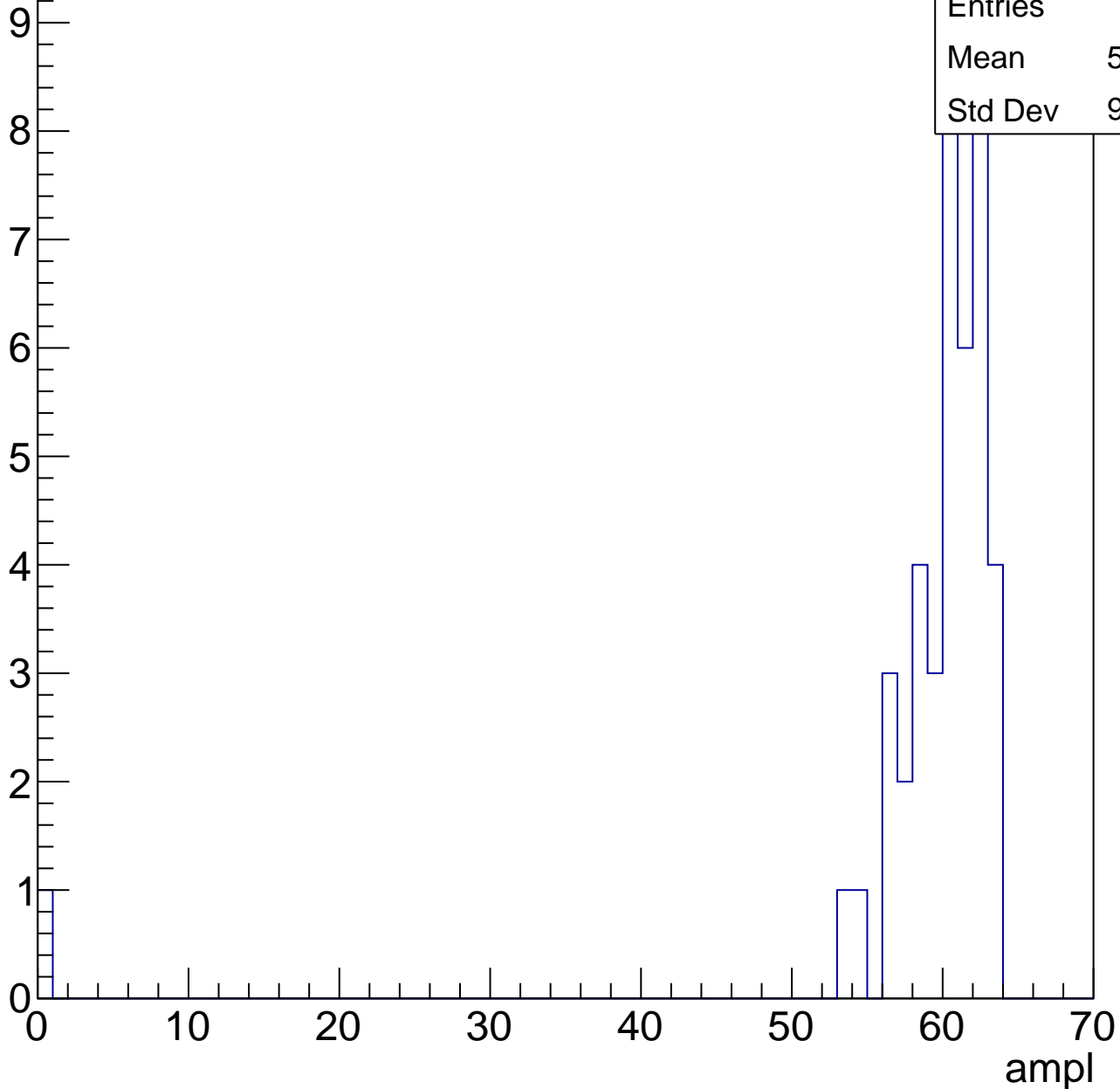


# B1L101S, U8-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	58.43
Std Dev	9.442

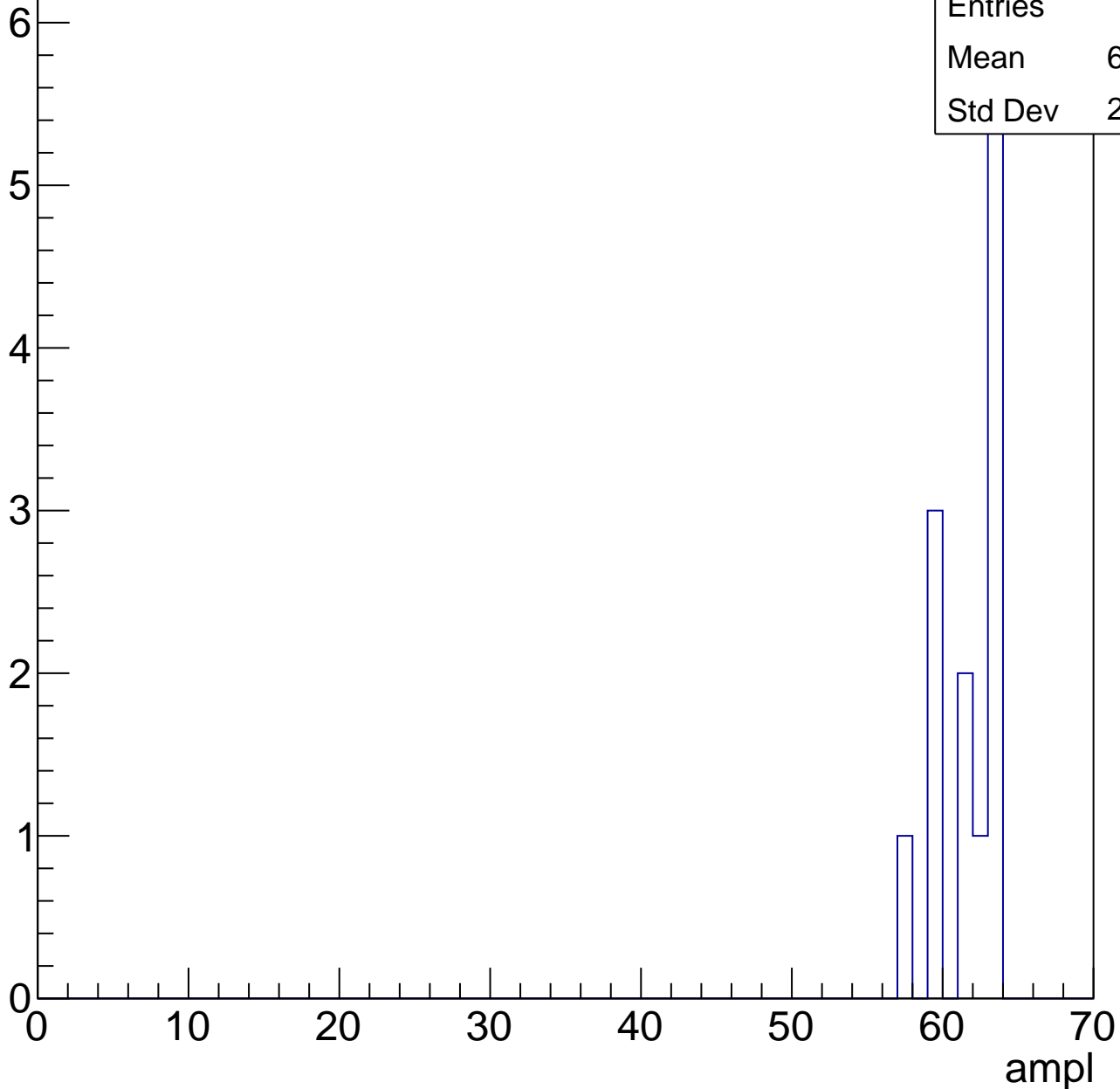


# B1L101S, U8-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	13
Mean	61.23
Std Dev	2.006





# B1L101S, U8-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U8-ch17, adc0

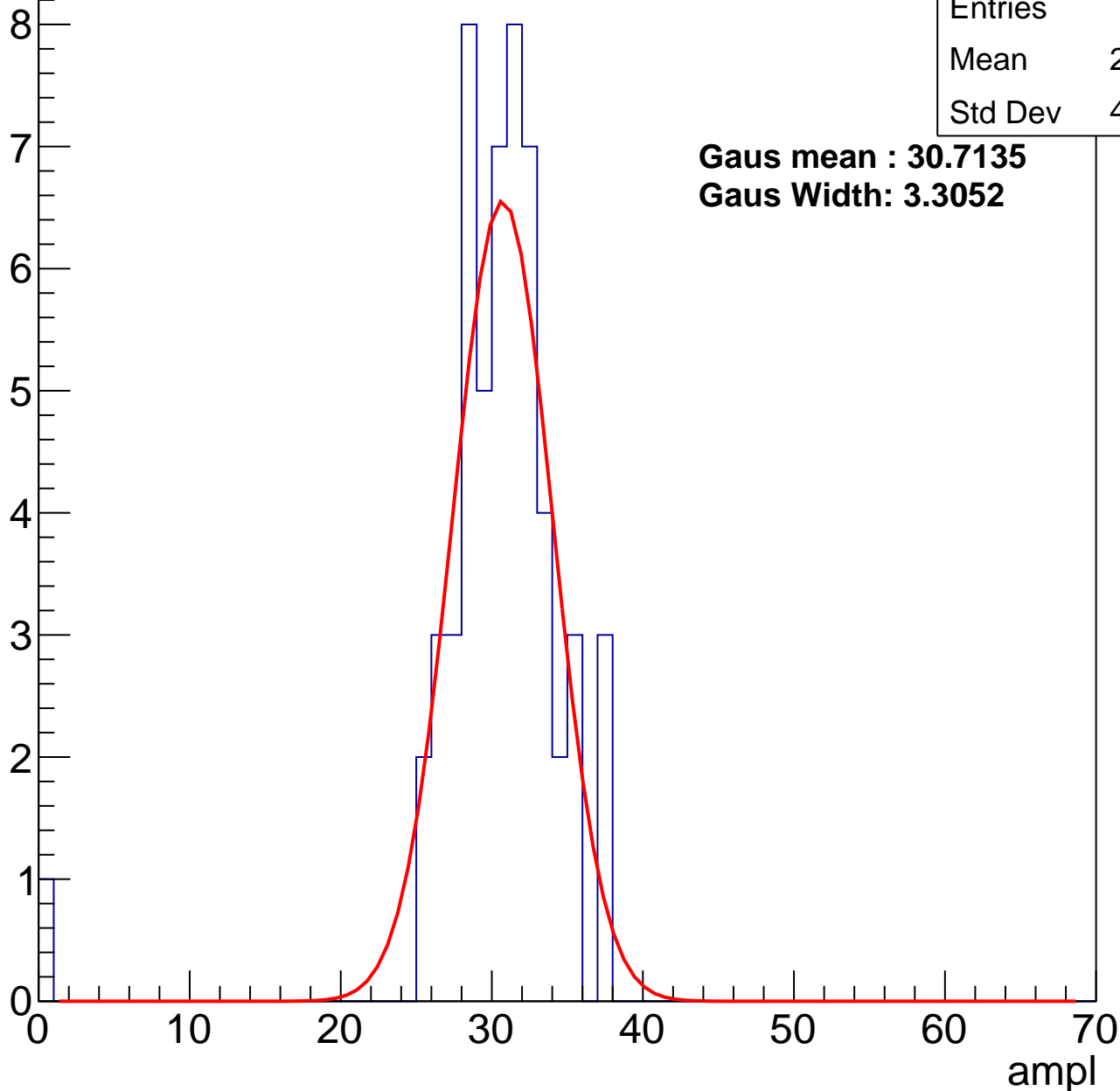
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	29.93
Std Dev	4.978

**Gaus mean : 30.7135**

**Gaus Width: 3.3052**



# B1L101S, U8-ch17, adc1

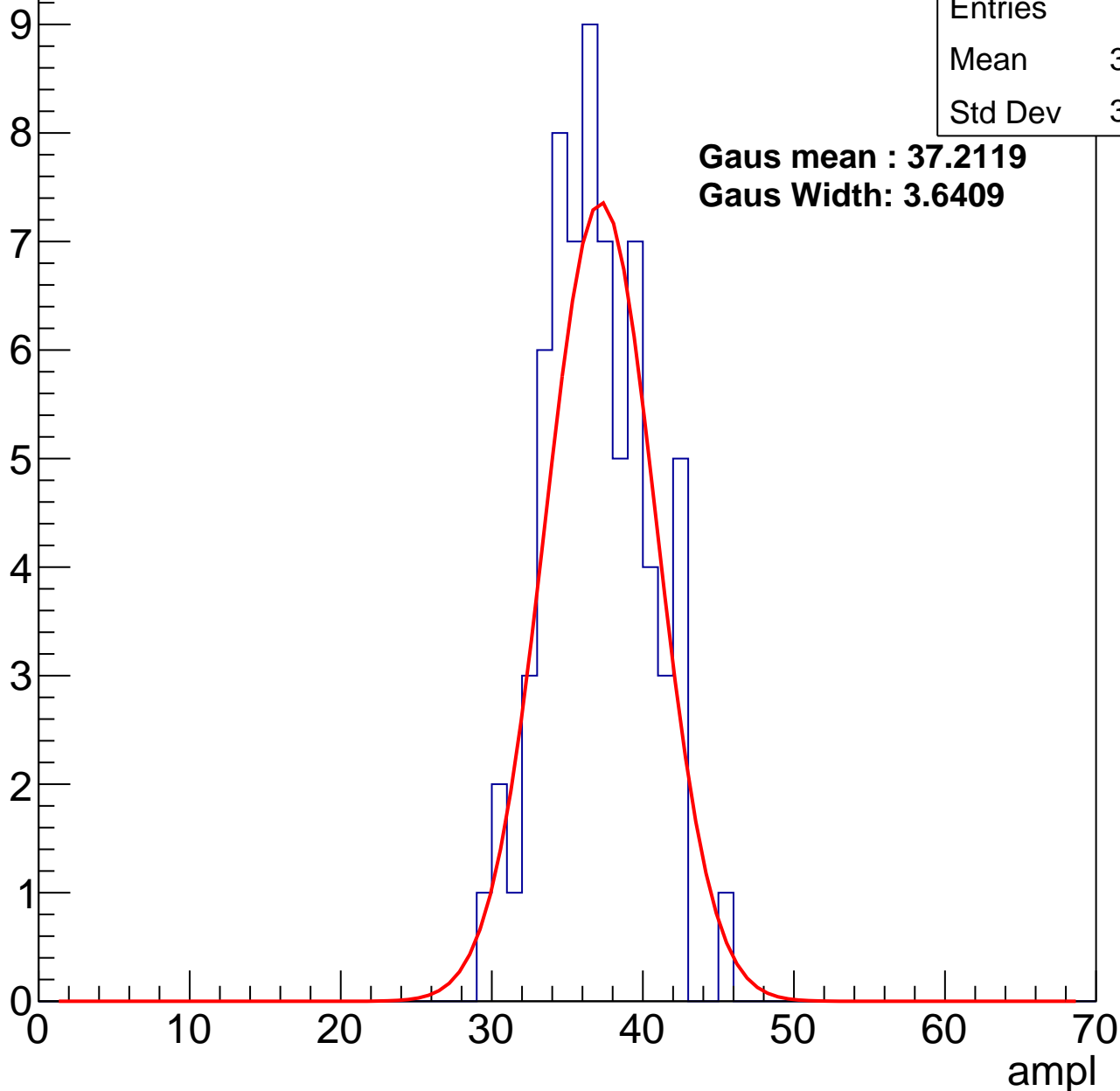
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	36.45
Std Dev	3.326

**Gaus mean : 37.2119**

**Gaus Width: 3.6409**



# B1L101S, U8-ch17, adc2

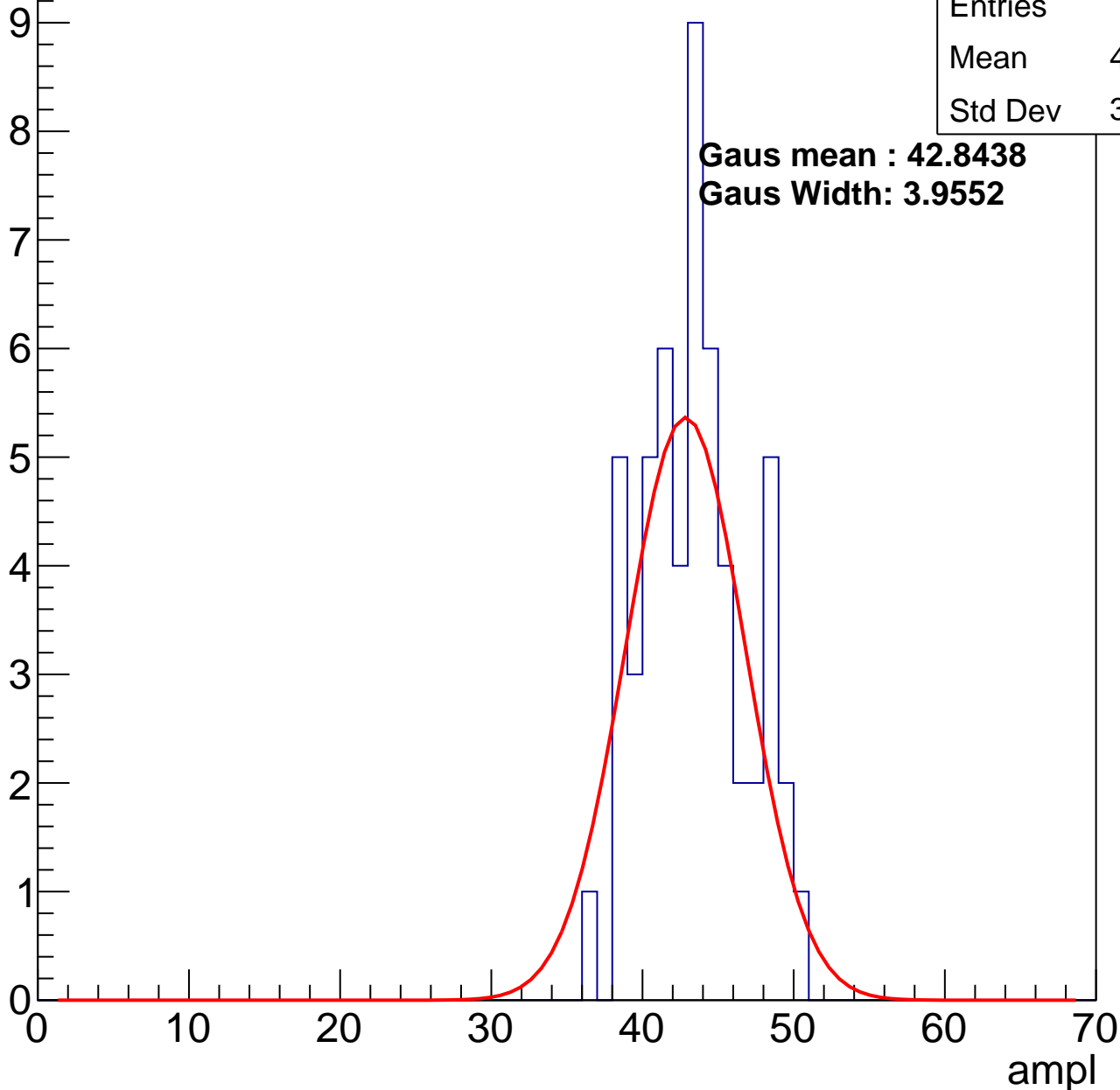
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	42.95
Std Dev	3.338

**Gaus mean : 42.8438**

**Gaus Width: 3.9552**

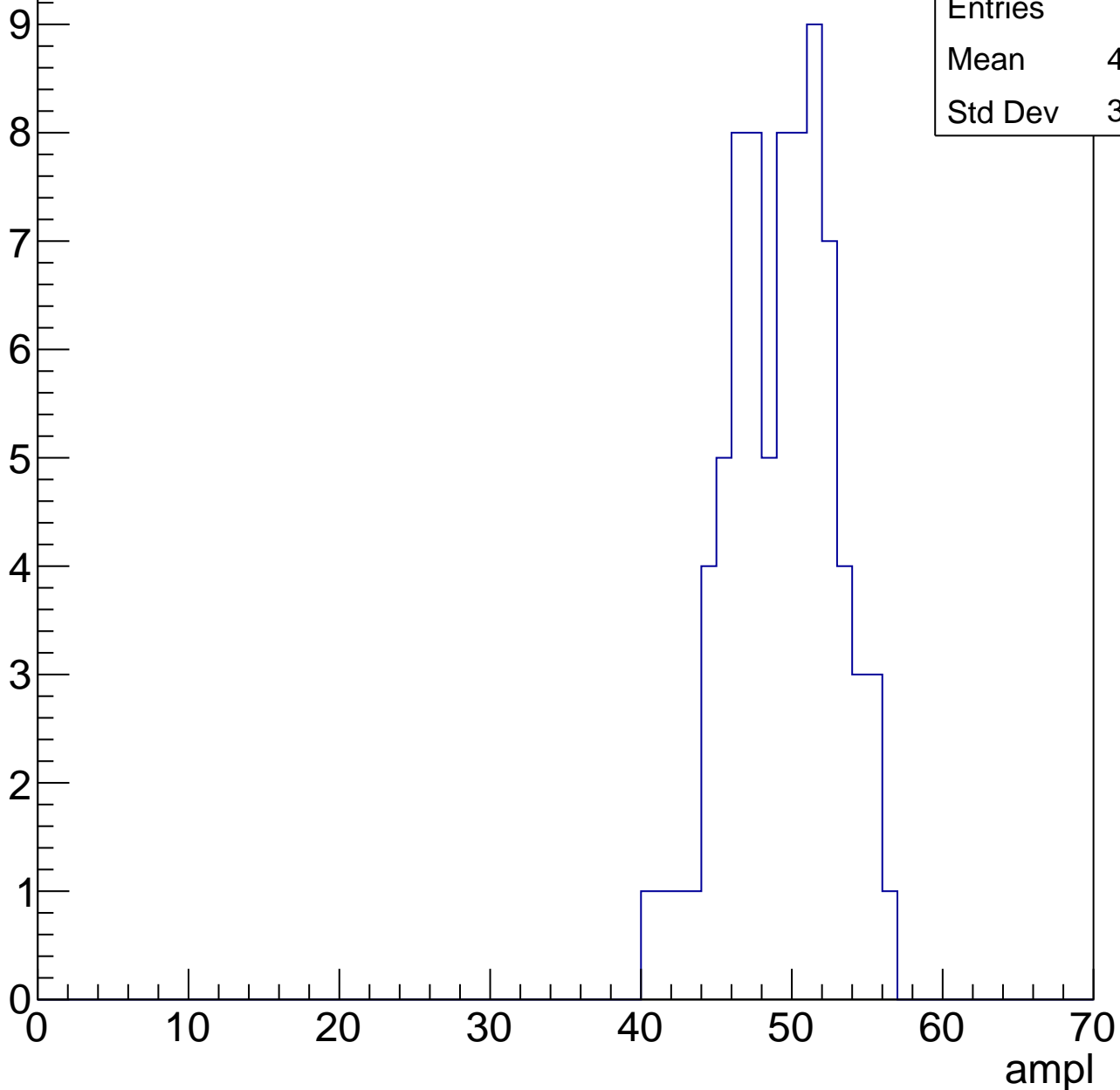


# B1L101S, U8-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

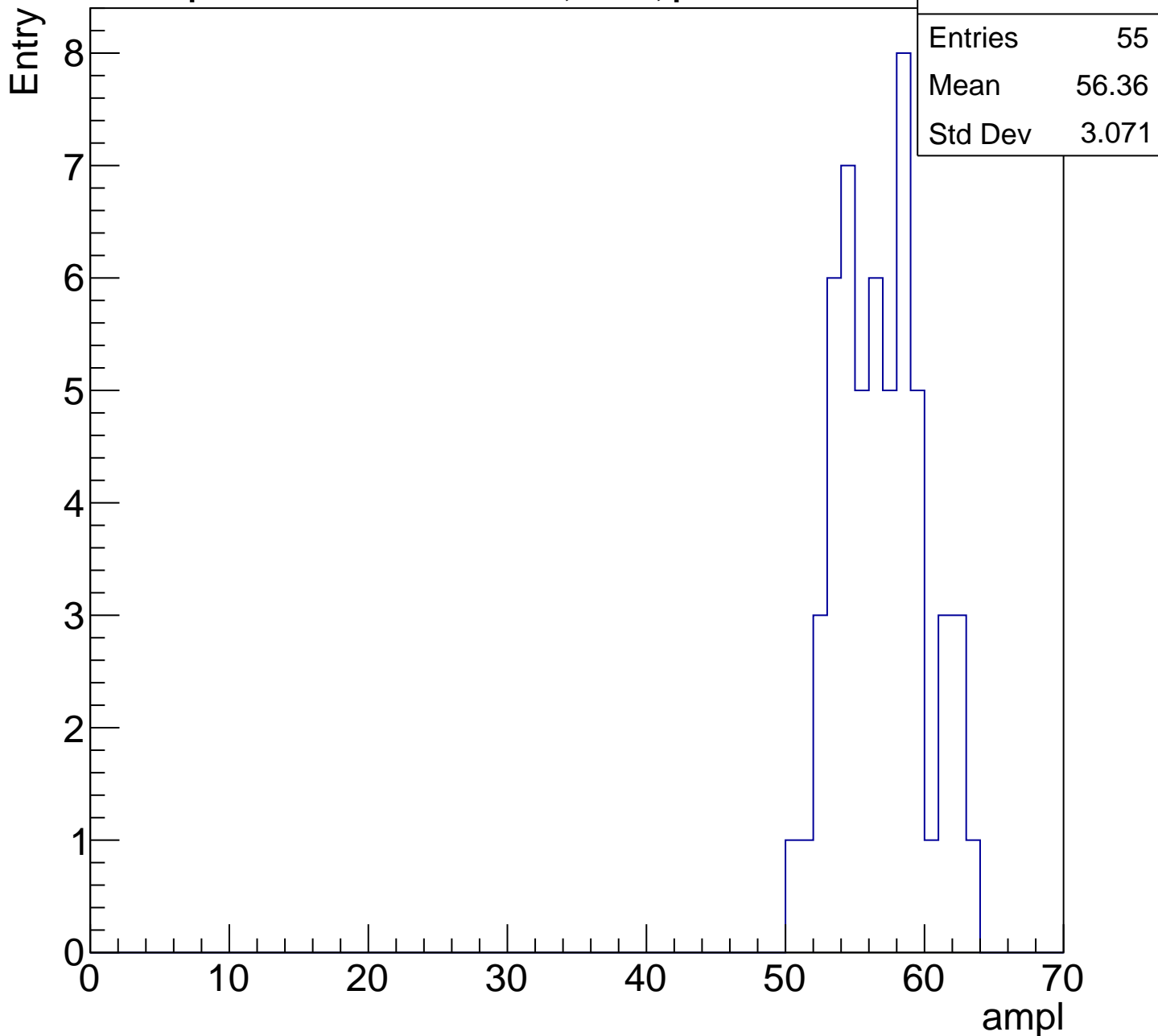
Entry

Entries	77
Mean	48.84
Std Dev	3.457



# B1L101S, U8-ch17, adc4

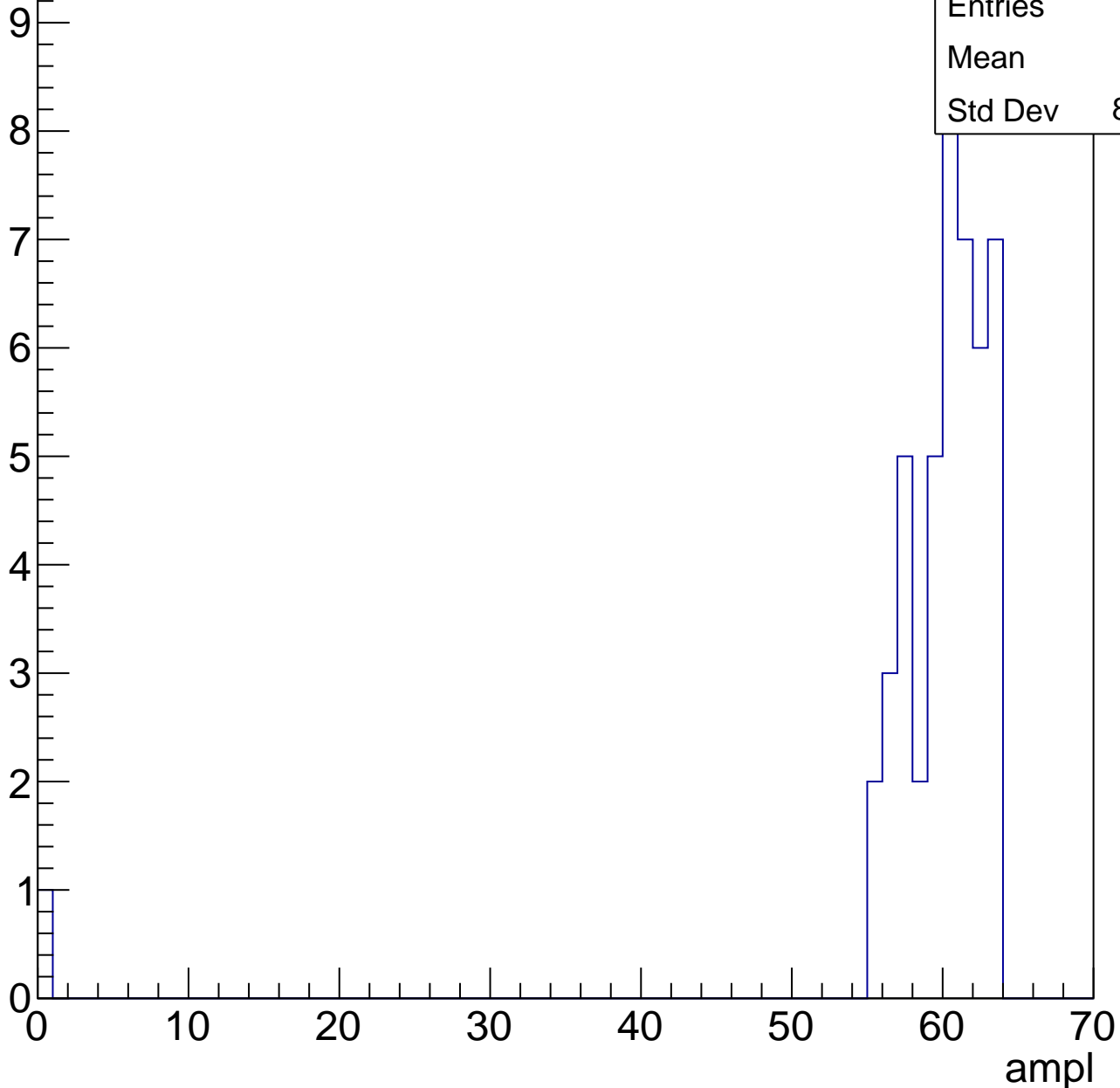
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U8-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch18, adc0

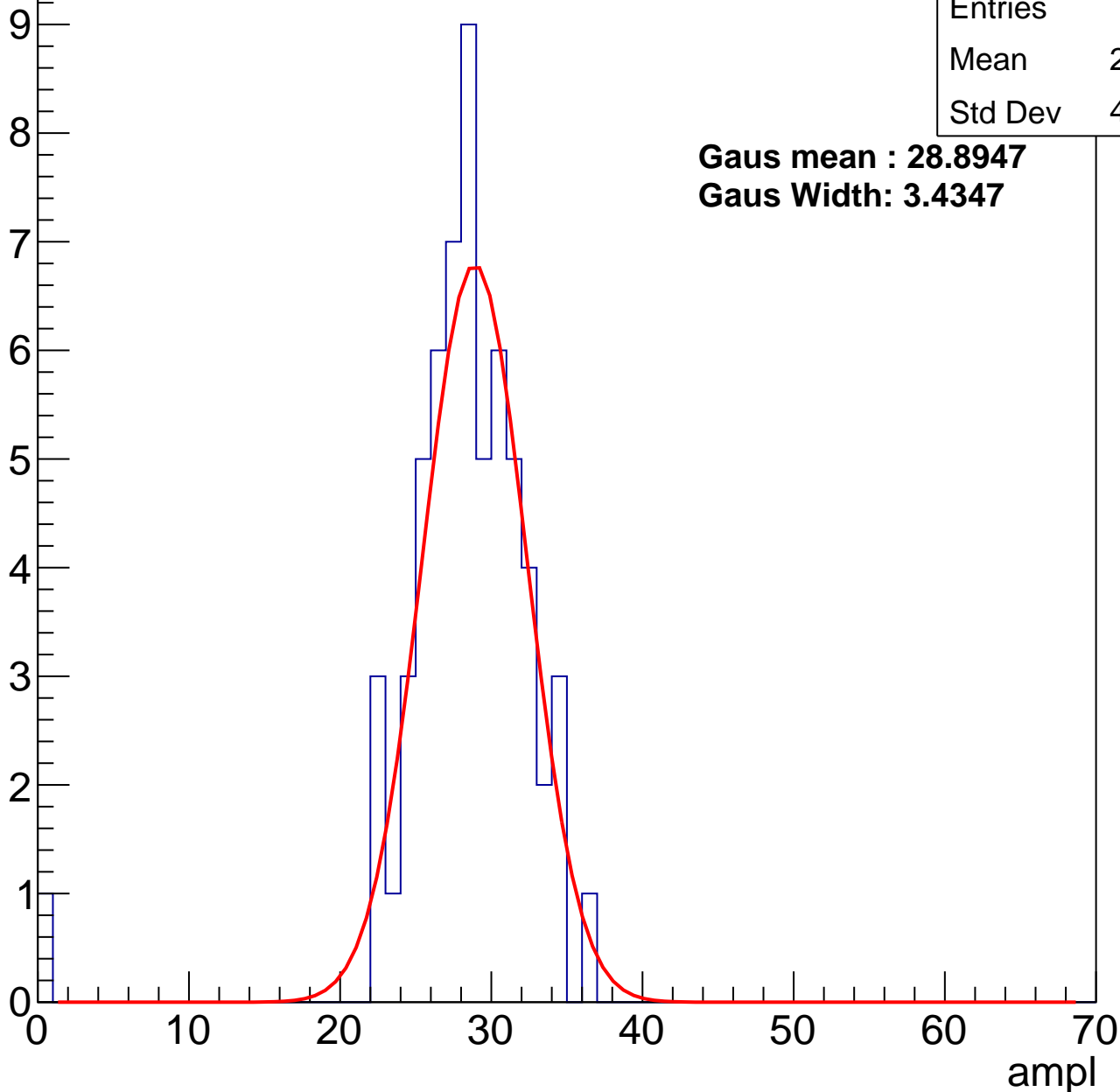
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	27.79
Std Dev	4.788

**Gaus mean : 28.8947**

**Gaus Width: 3.4347**



# B1L101S, U8-ch18, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	72
Mean	34.74
Std Dev	3.508

**Gaus mean : 34.8483**

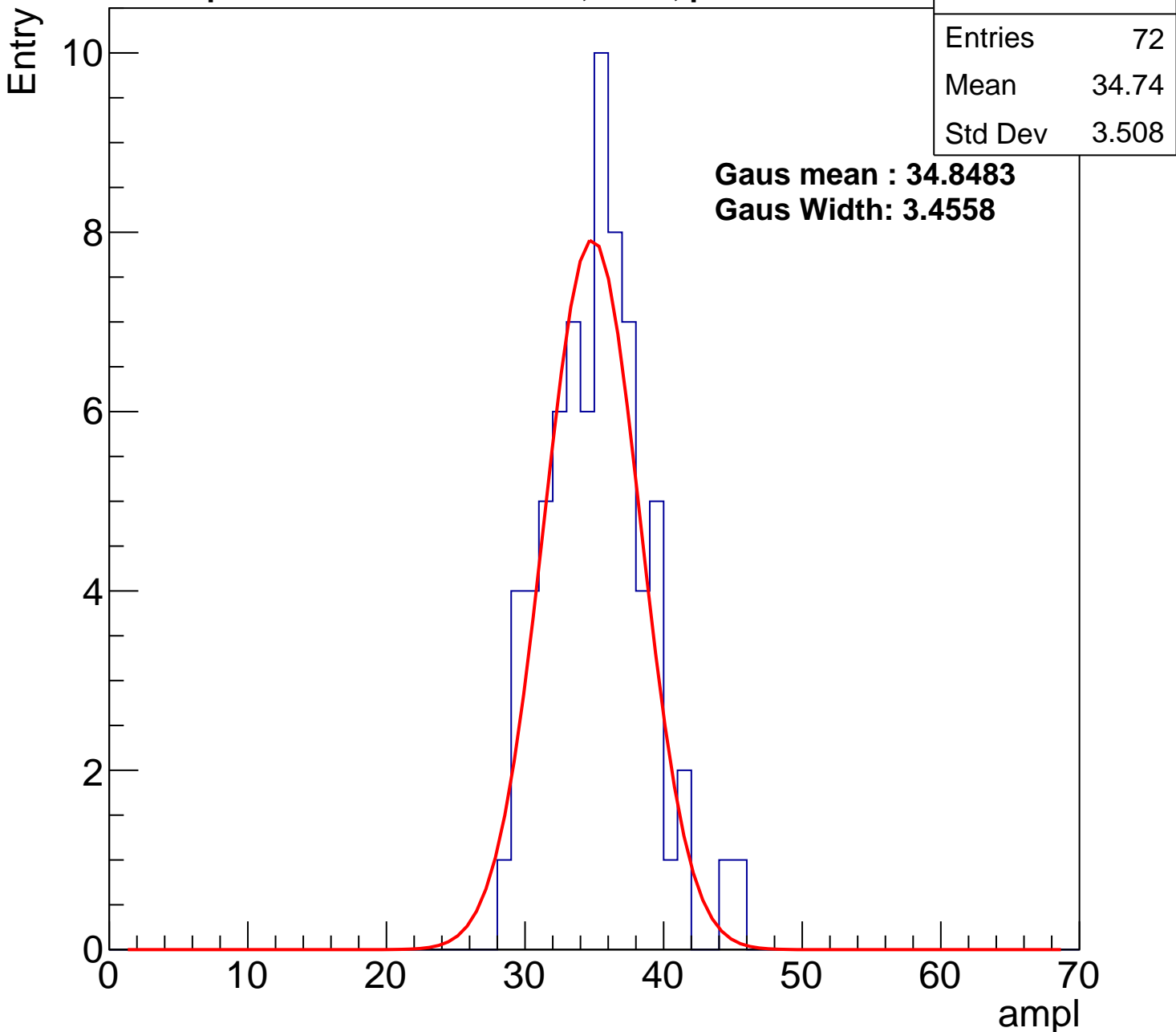
**Gaus Width: 3.4558**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U8-ch18, adc2

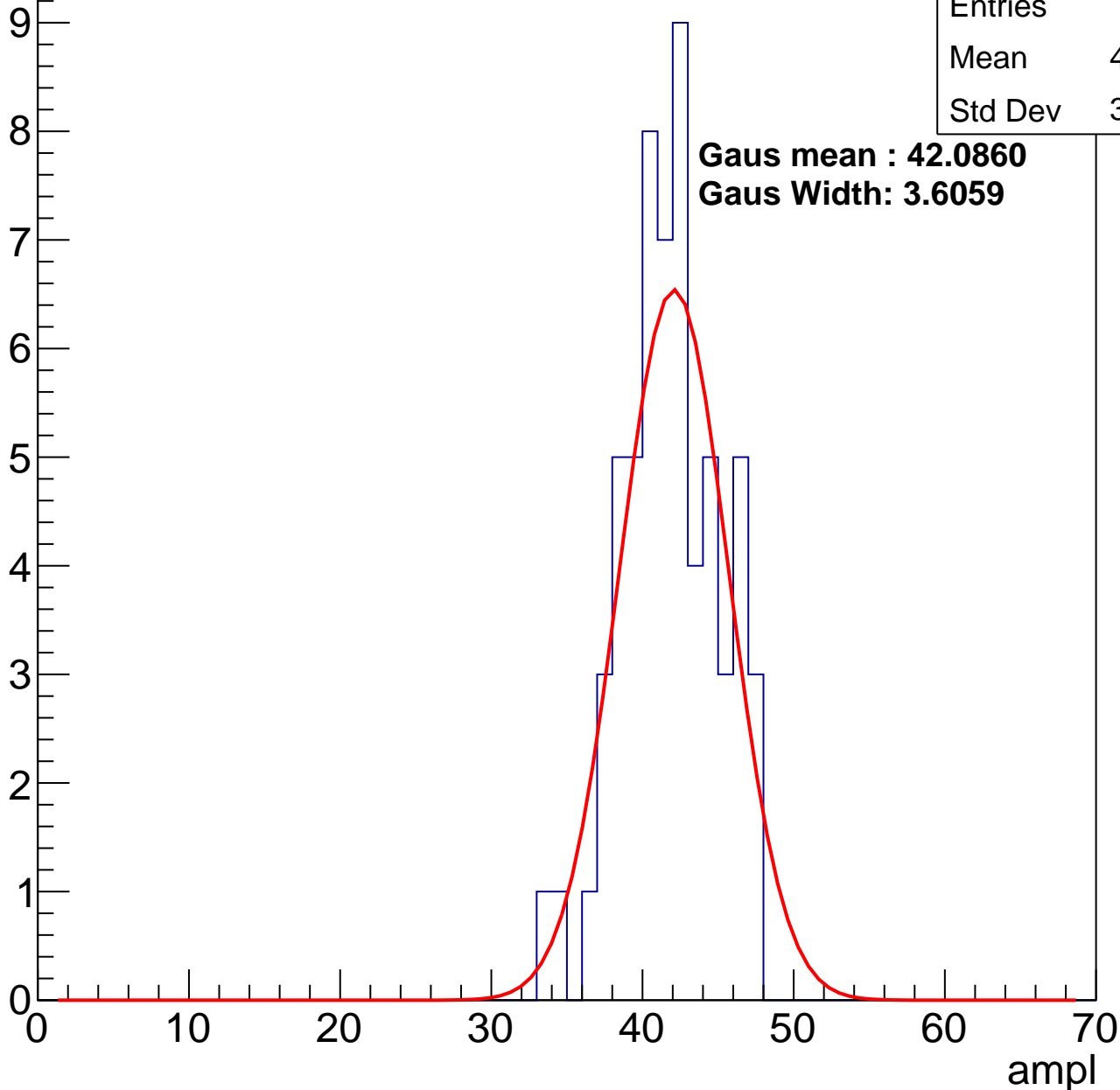
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	41.37
Std Dev	3.167

**Gaus mean : 42.0860**

**Gaus Width: 3.6059**



# B1L101S, U8-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

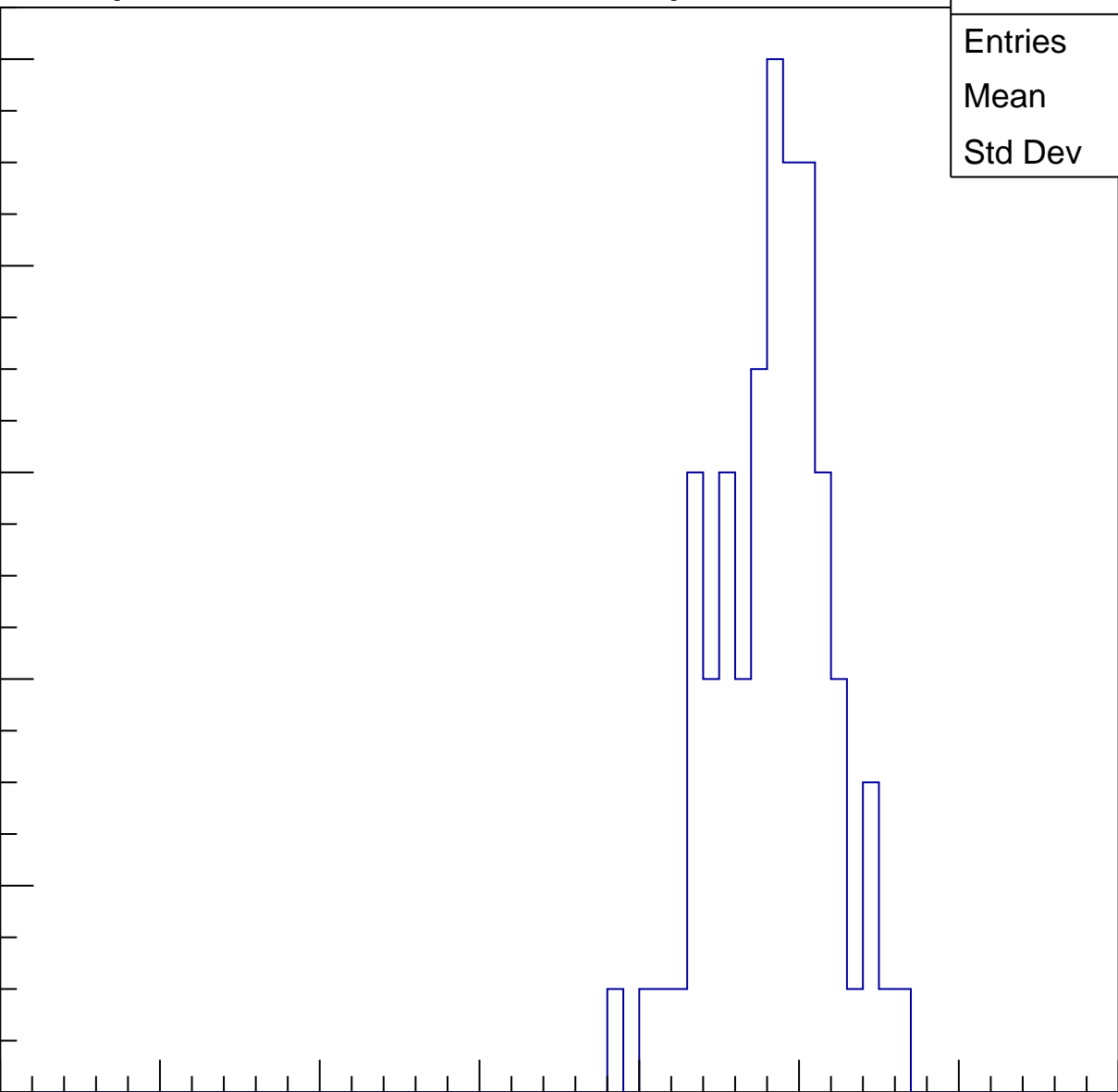
Entries	75
Mean	47.85
Std Dev	3.554

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

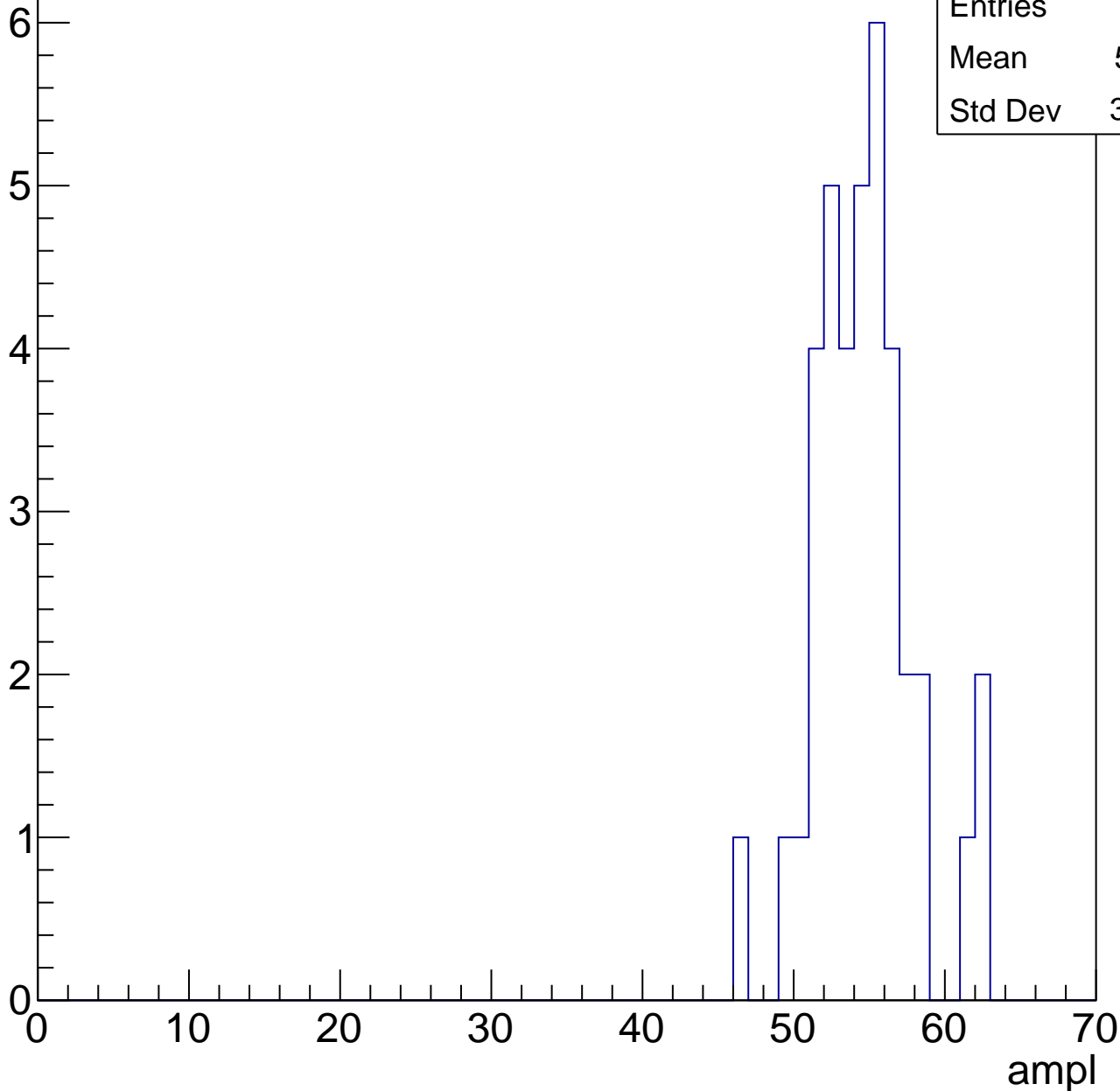


# B1L101S, U8-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	38
Mean	54.21
Std Dev	3.294



# B1L101S, U8-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

10

Entries 68

Mean 58.4

Std Dev 2.834

8

6

4

2

0

0

10

20

30

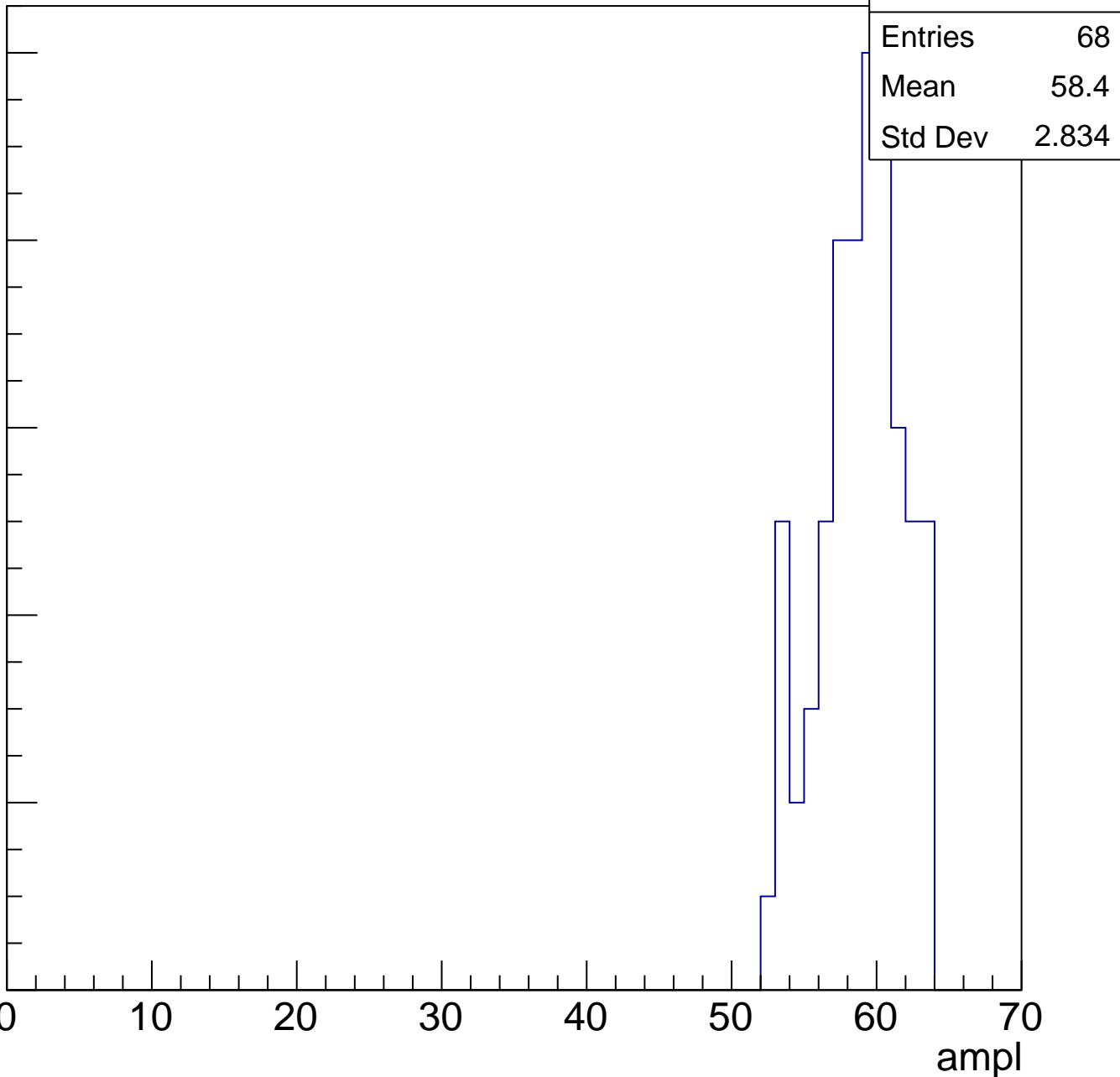
40

50

60

70

ampl

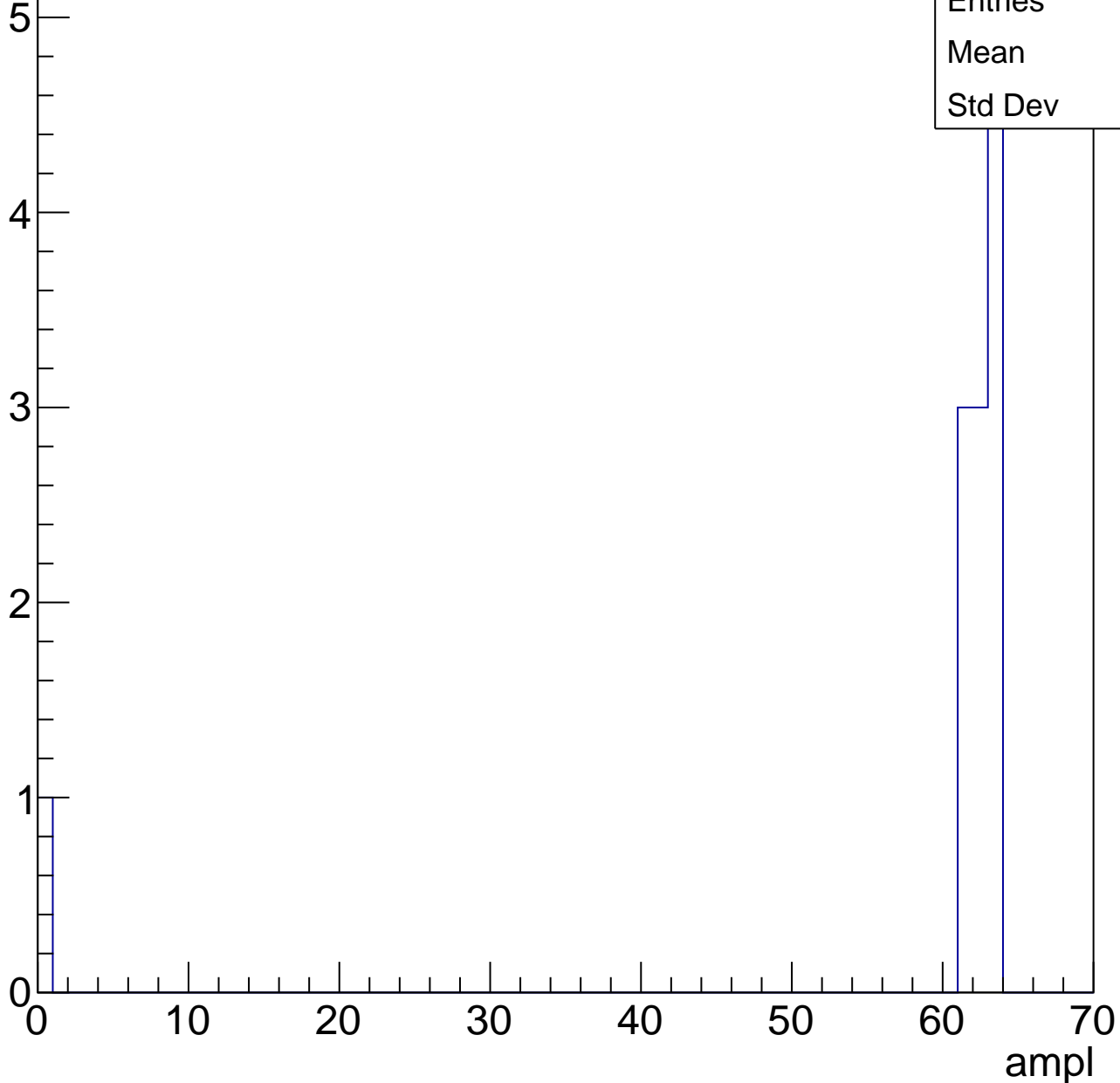


# B1L101S, U8-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	12
Mean	57
Std Dev	17.2





# B1L101S, U8-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	7.333
Std Dev	10.37

# B1L101S, U8-ch19, adc0

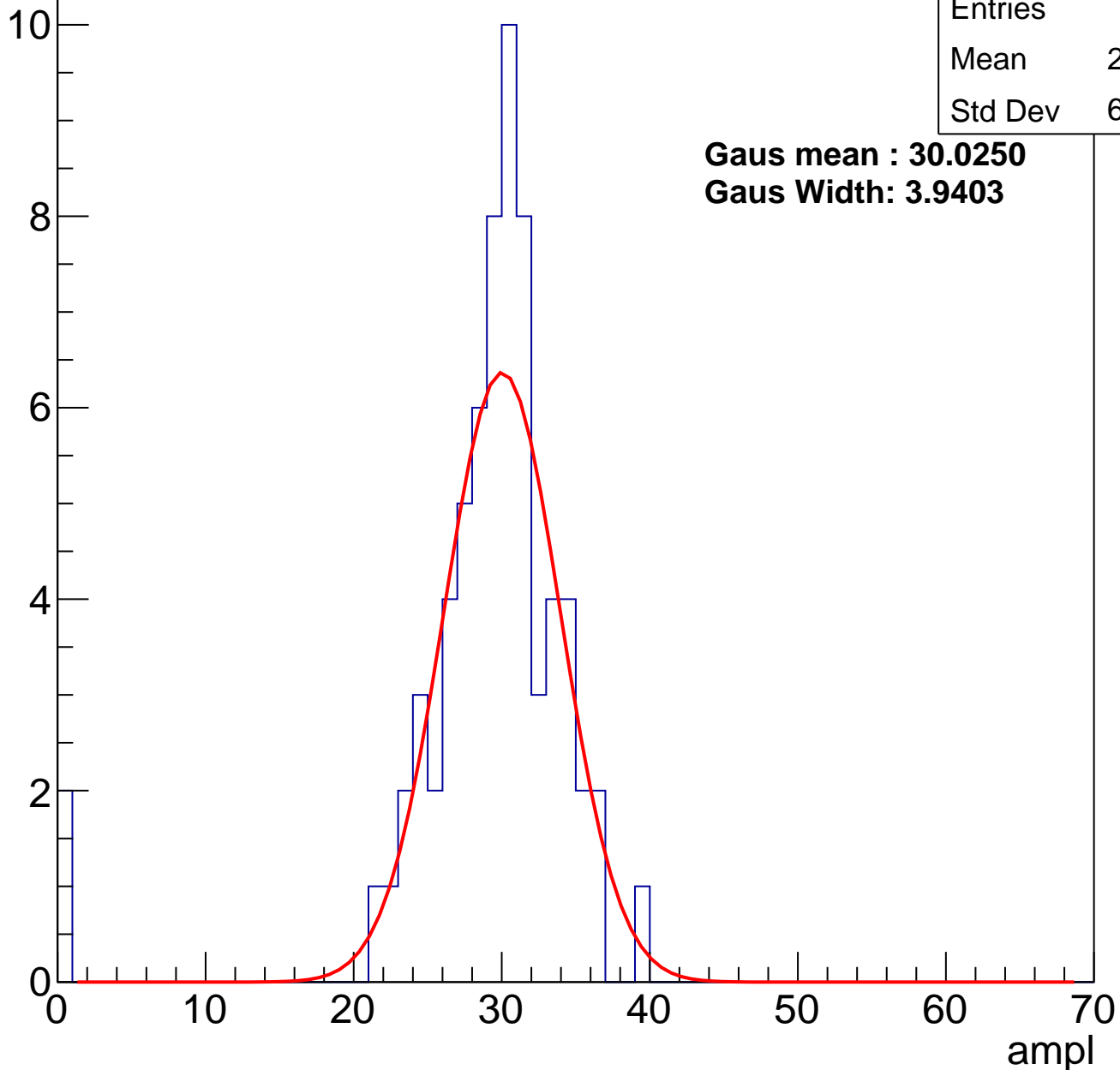
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	68
Mean	28.57
Std Dev	6.096

**Gaus mean : 30.0250**

**Gaus Width: 3.9403**

Entry



# B1L101S, U8-ch19, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	84
Mean	36.12
Std Dev	5.176

**Gaus mean : 36.5528**

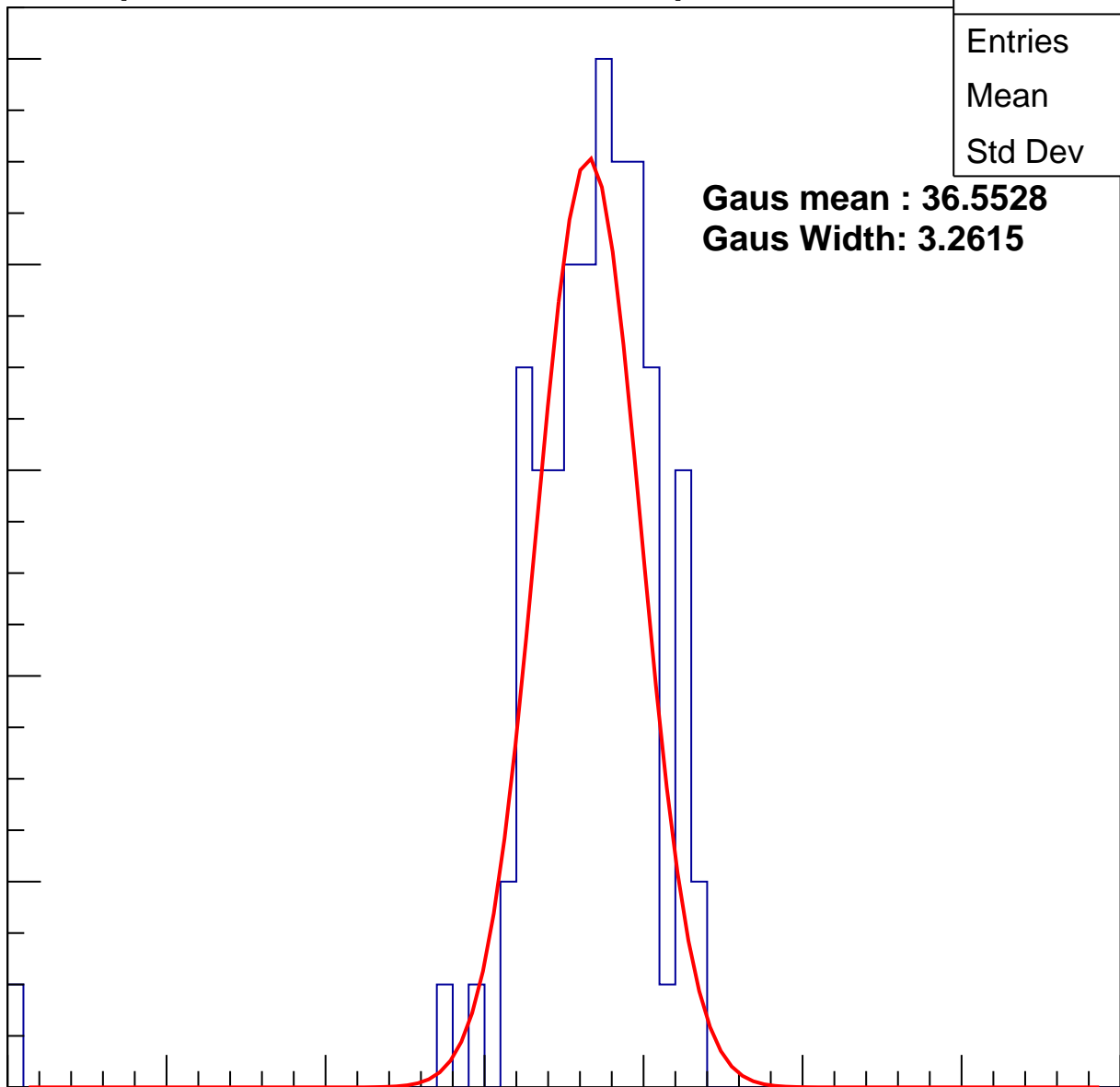
**Gaus Width: 3.2615**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U8-ch19, adc2

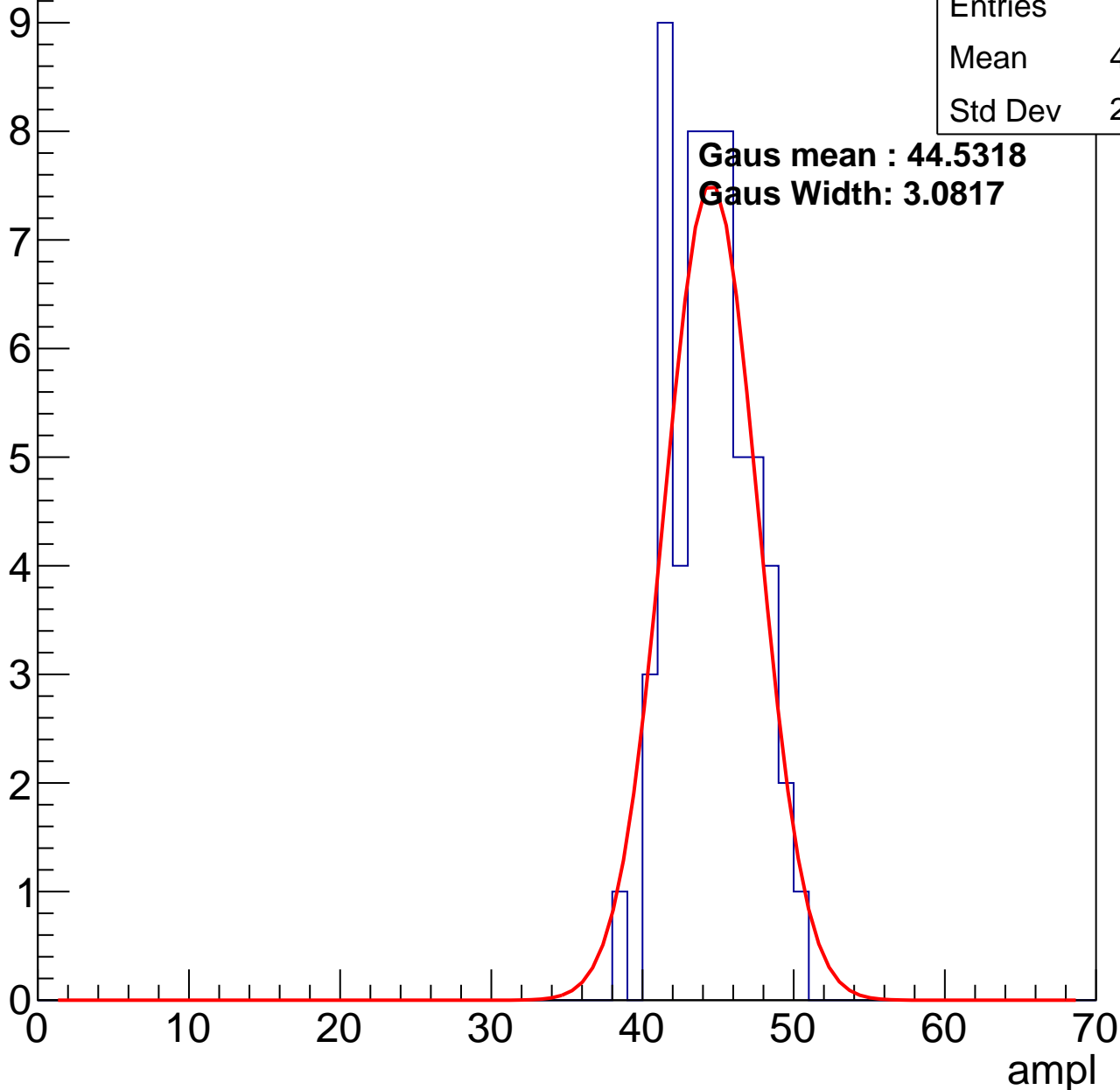
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	44.07
Std Dev	2.664

**Gaus mean : 44.5318**

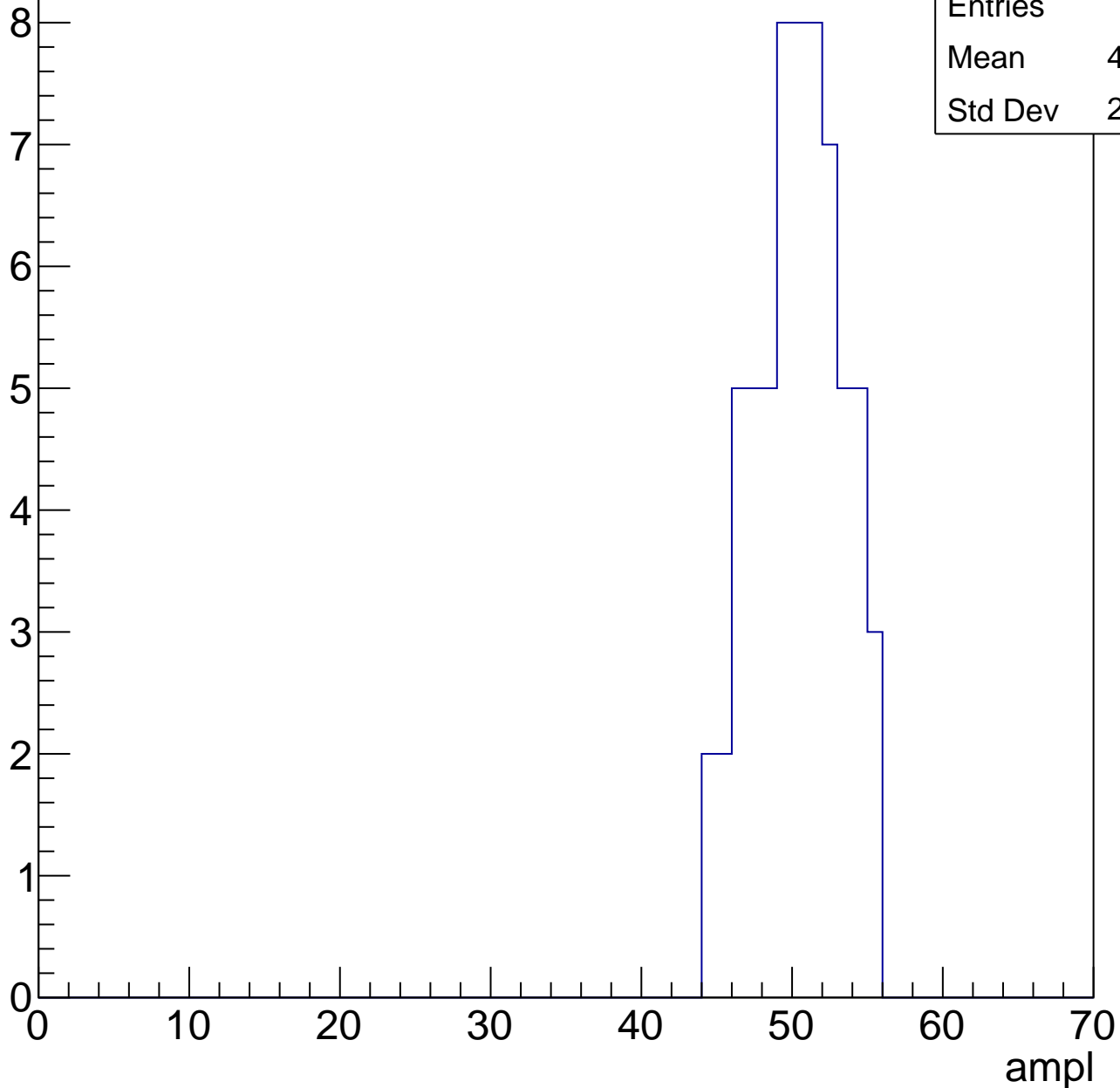
**Gaus Width: 3.0817**



# B1L101S, U8-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



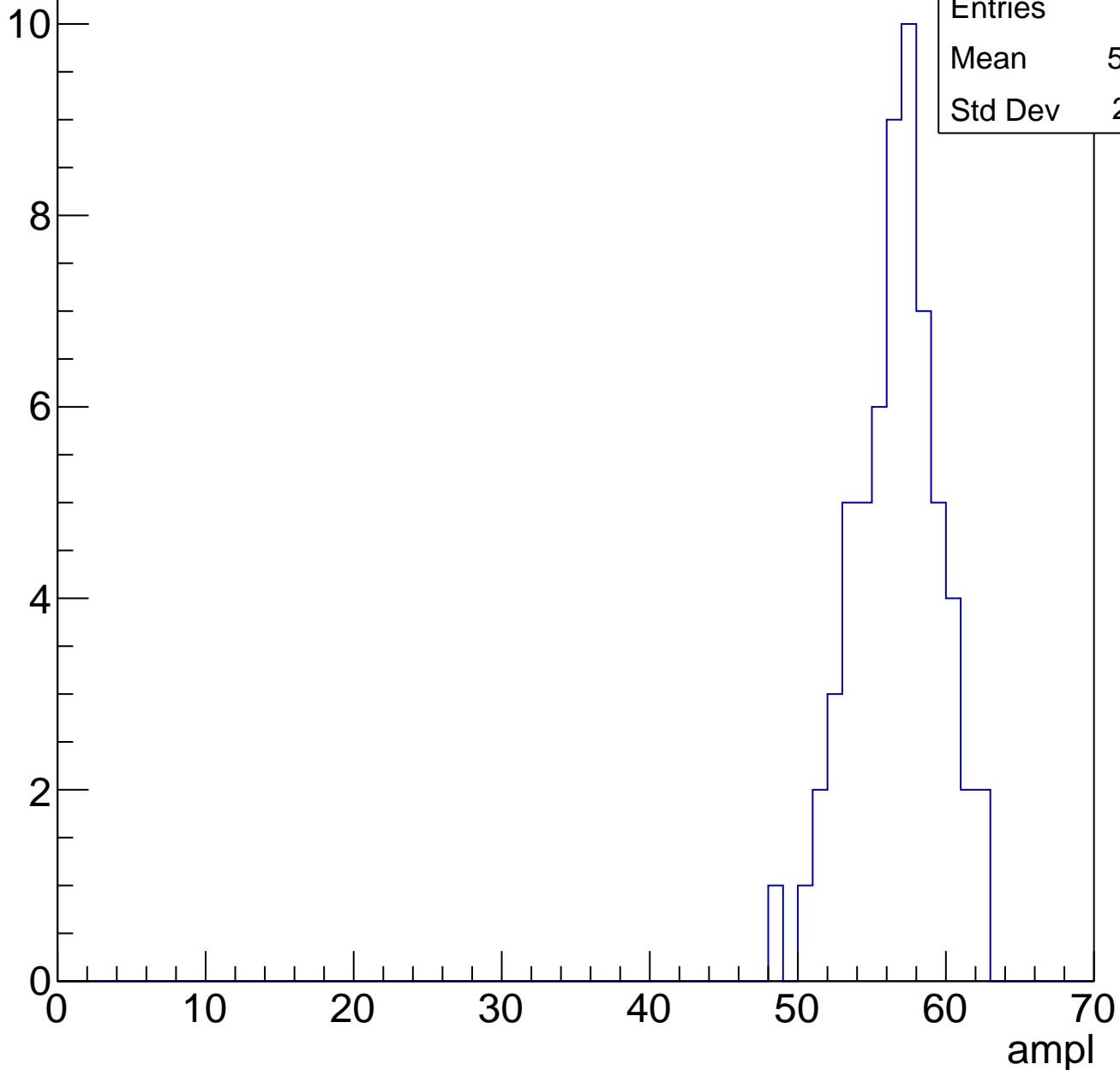
Entries	63
Mean	49.95
Std Dev	2.848

# B1L101S, U8-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	62
Mean	56.16
Std Dev	2.941

Entry

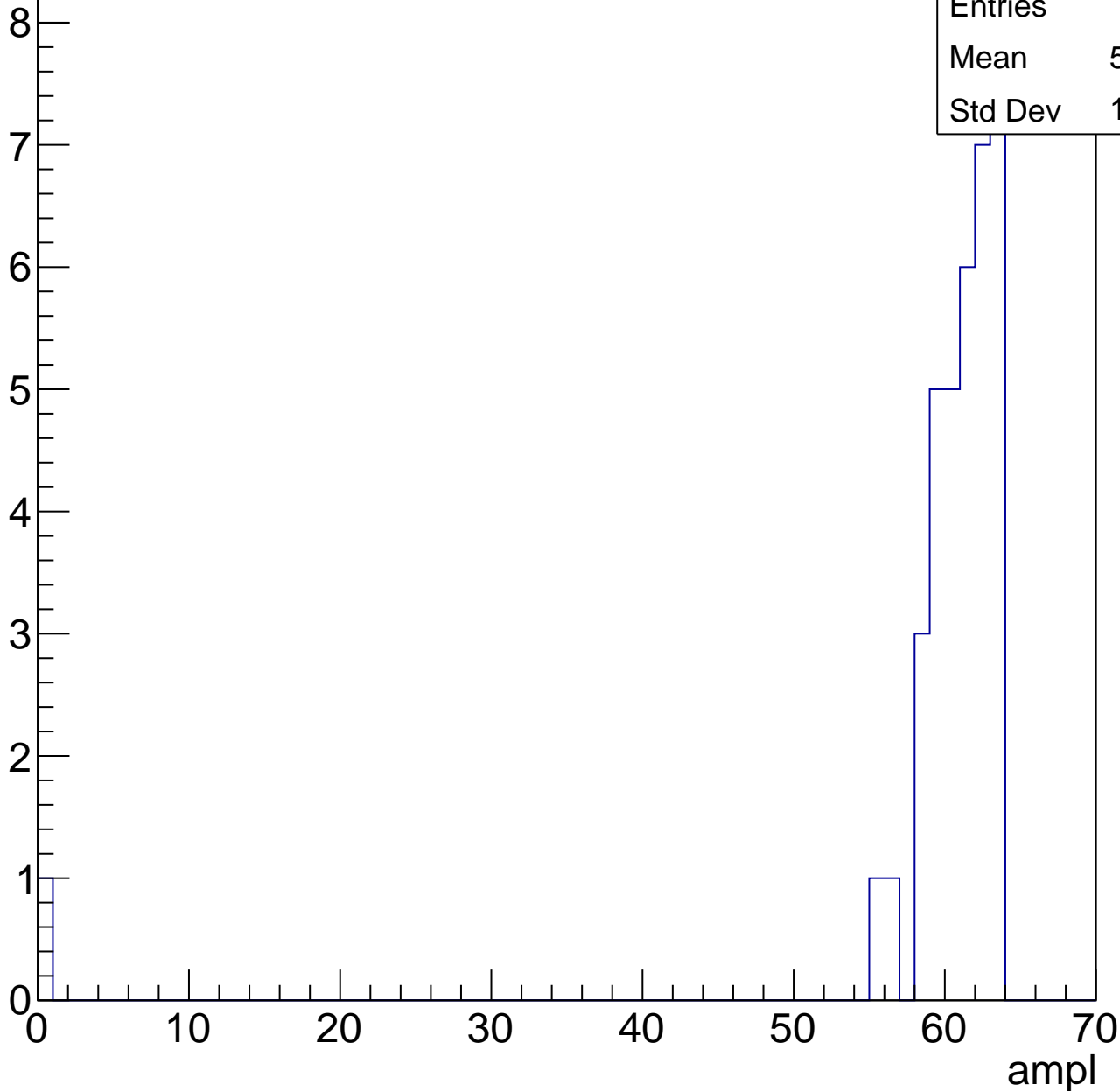


# B1L101S, U8-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	37
Mean	59.03
Std Dev	10.04



# B1L101S, U8-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.67
Std Dev	1.106

ampl

0 10 20 30 40 50 60 70



# B1L101S, U8-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U8-ch20, adc0

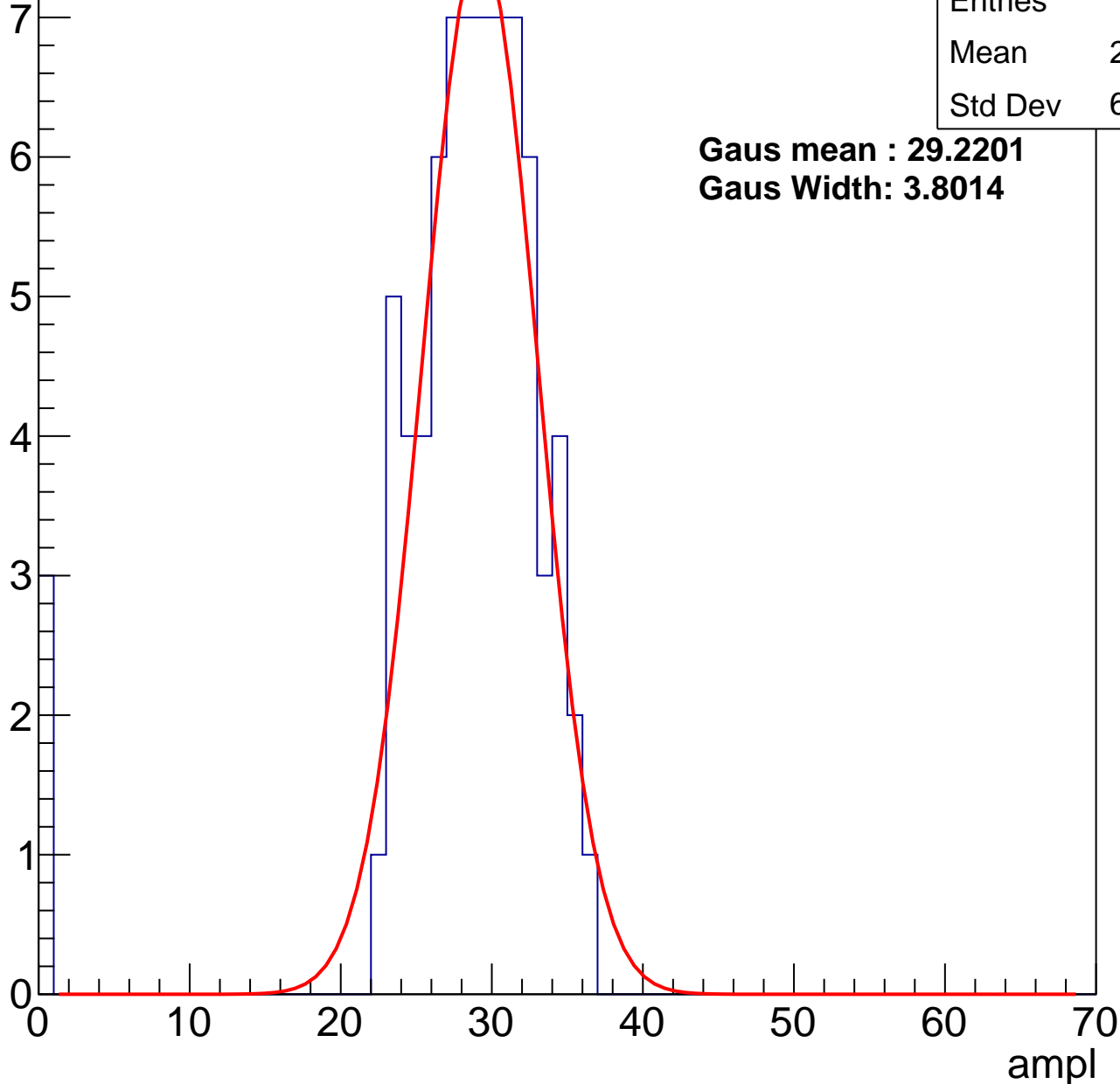
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	27.53
Std Dev	6.578

**Gaus mean : 29.2201**

**Gaus Width: 3.8014**



# B1L101S, U8-ch20, adc1

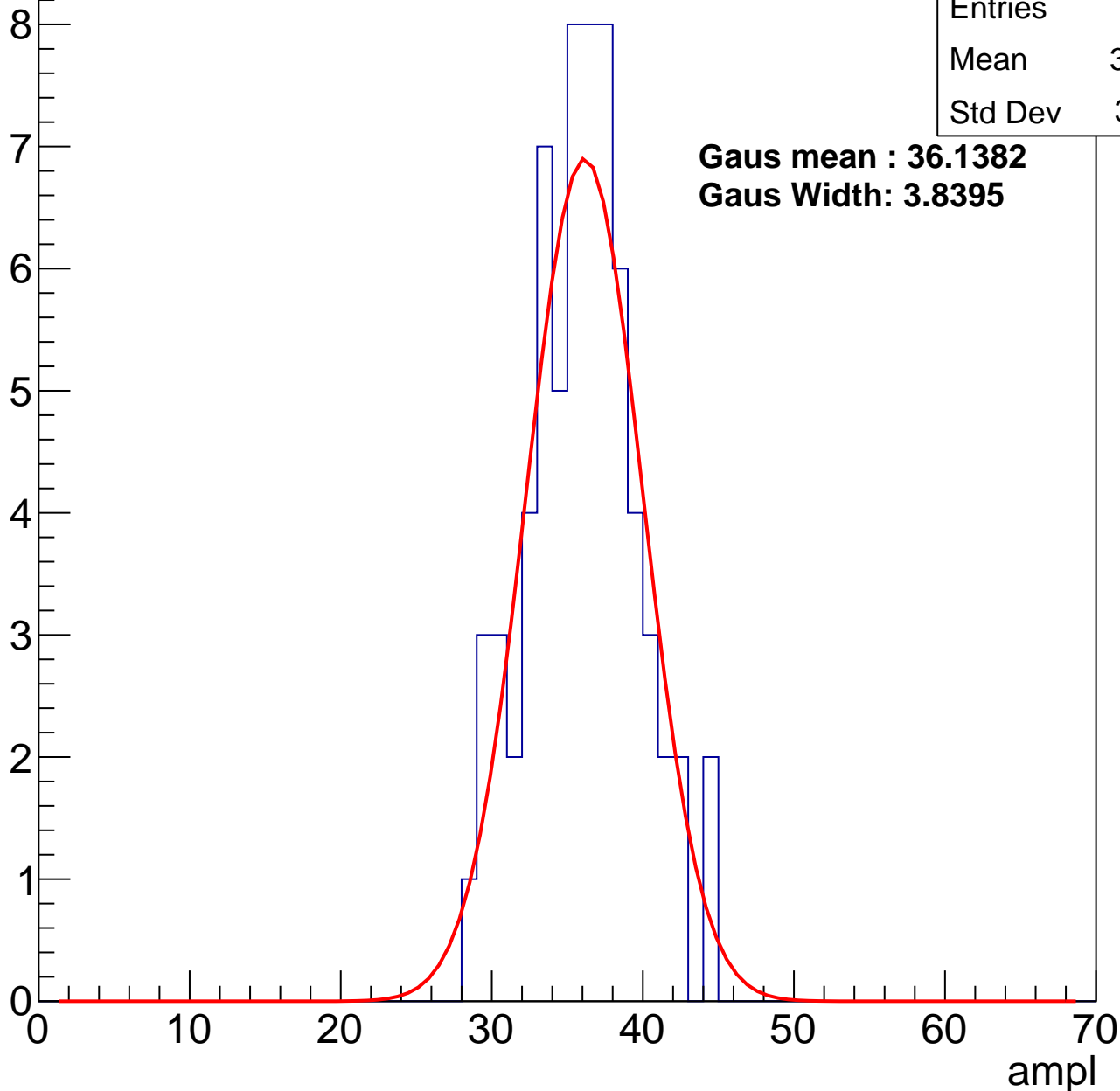
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	35.56
Std Dev	3.591

**Gaus mean : 36.1382**

**Gaus Width: 3.8395**



# B1L101S, U8-ch20, adc2

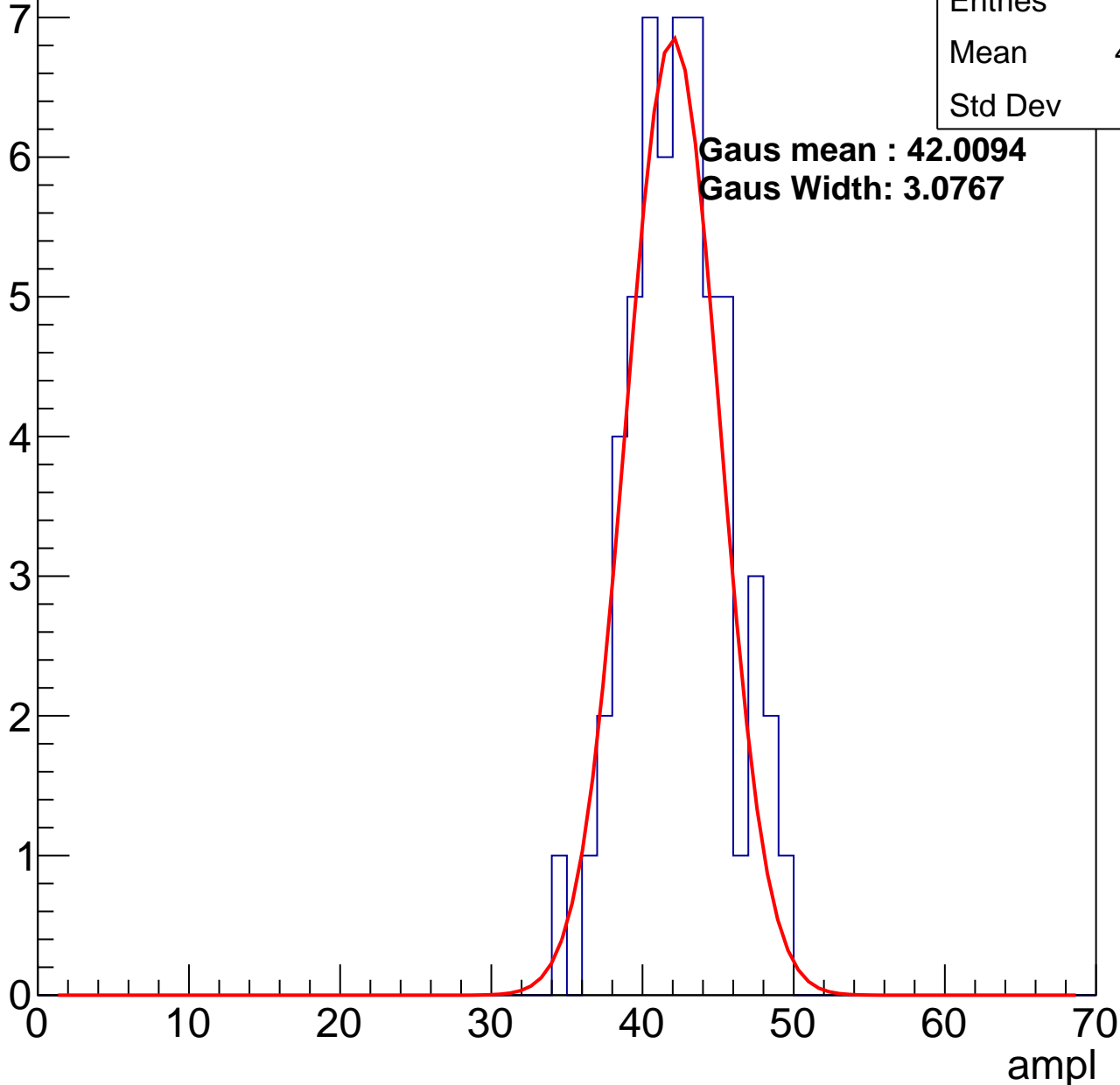
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	41.91
Std Dev	3.18

**Gaus mean : 42.0094**

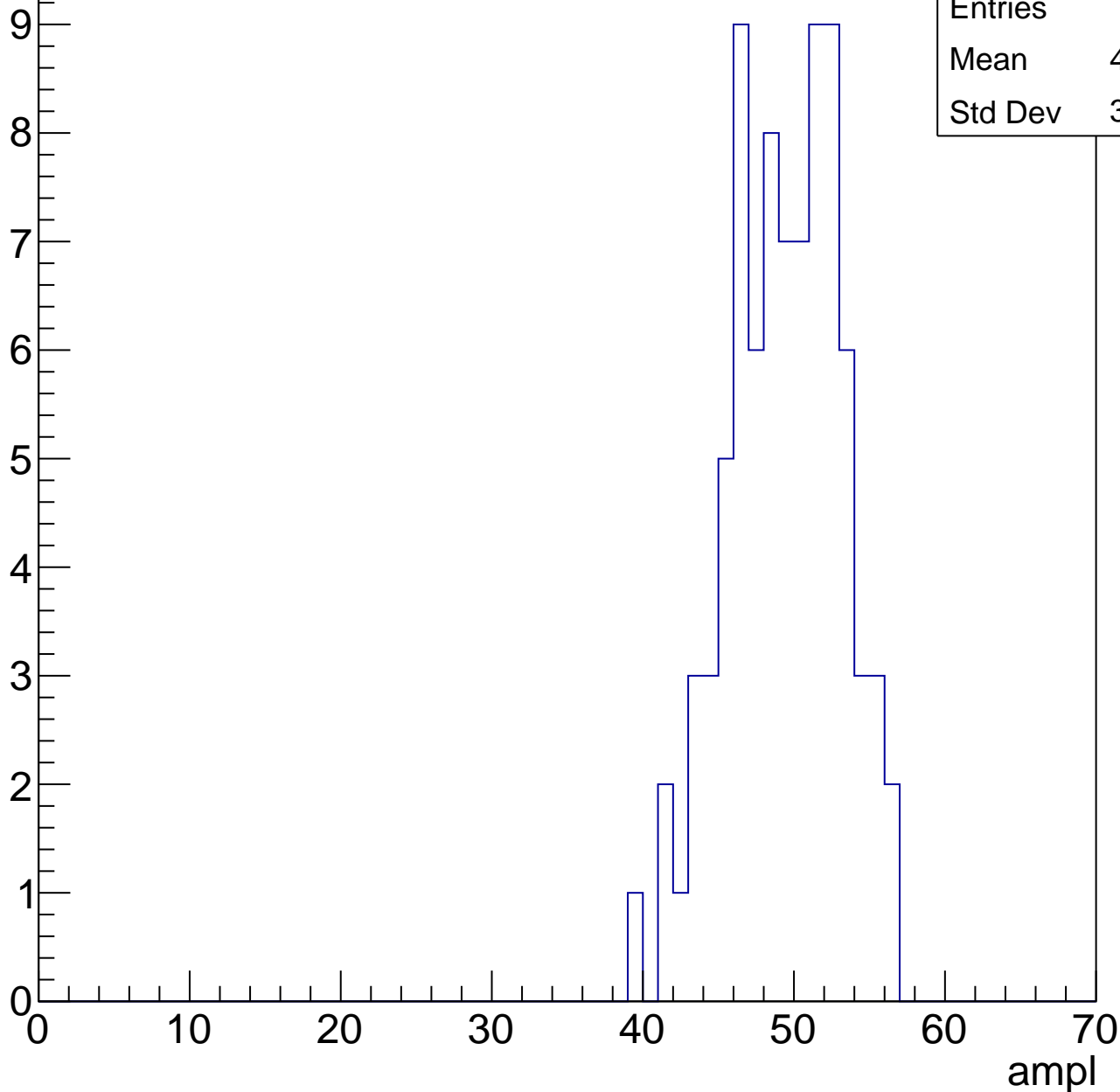
**Gaus Width: 3.0767**



# B1L101S, U8-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

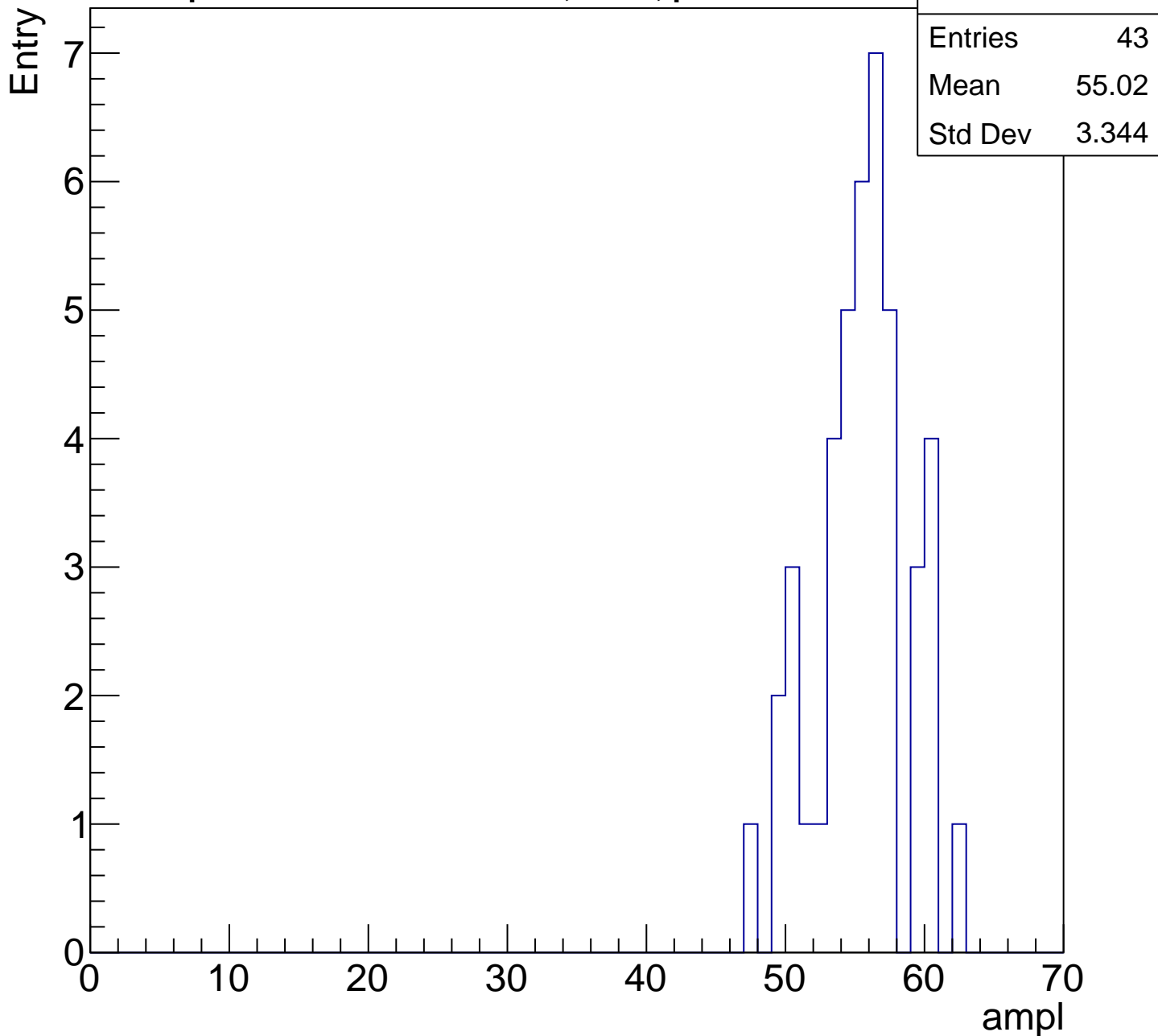
Entry



Entries	84
Mean	48.88
Std Dev	3.705

# B1L101S, U8-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

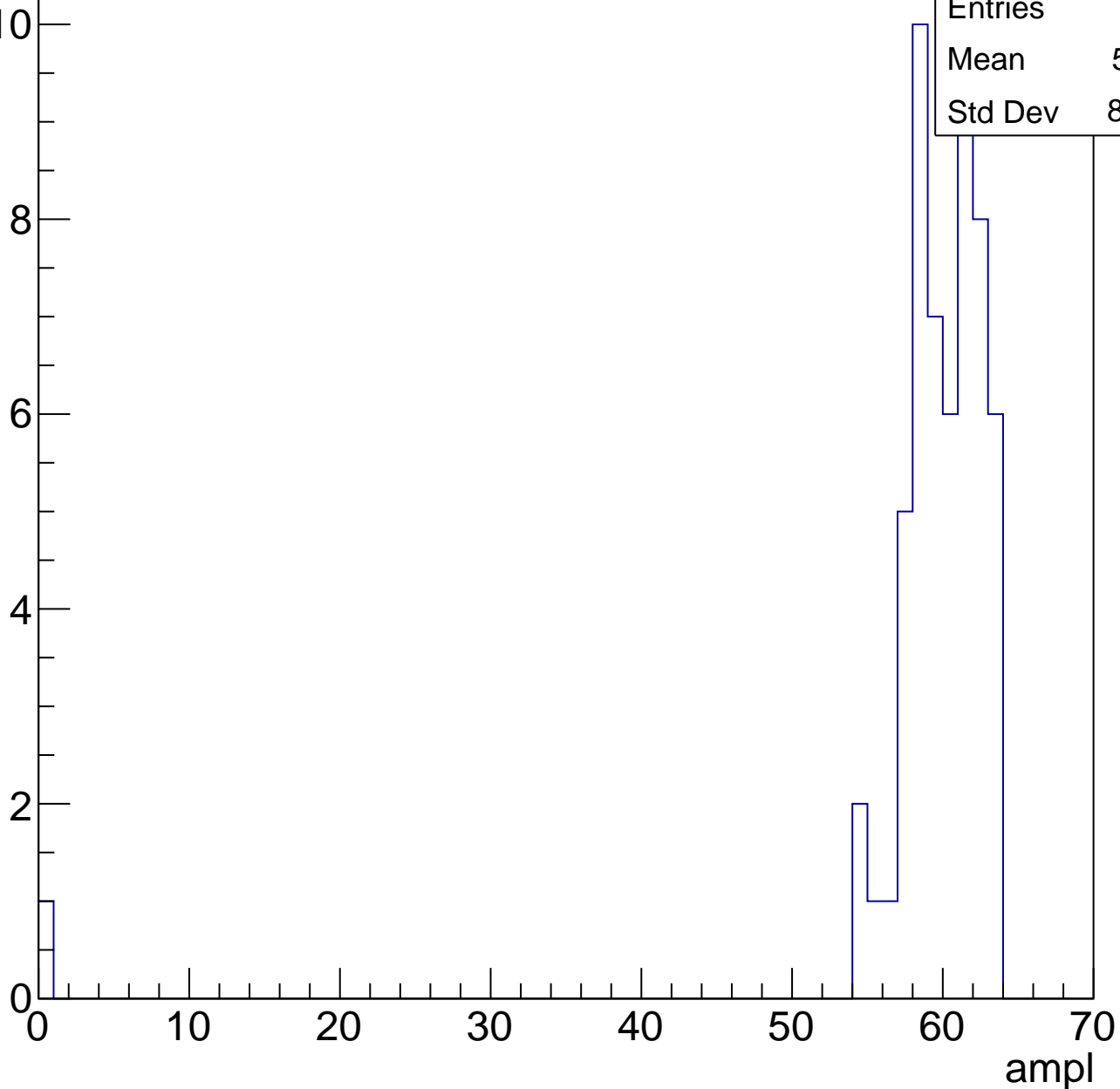


# B1L101S, U8-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	58.61
Std Dev	8.156



# B1L101S, U8-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



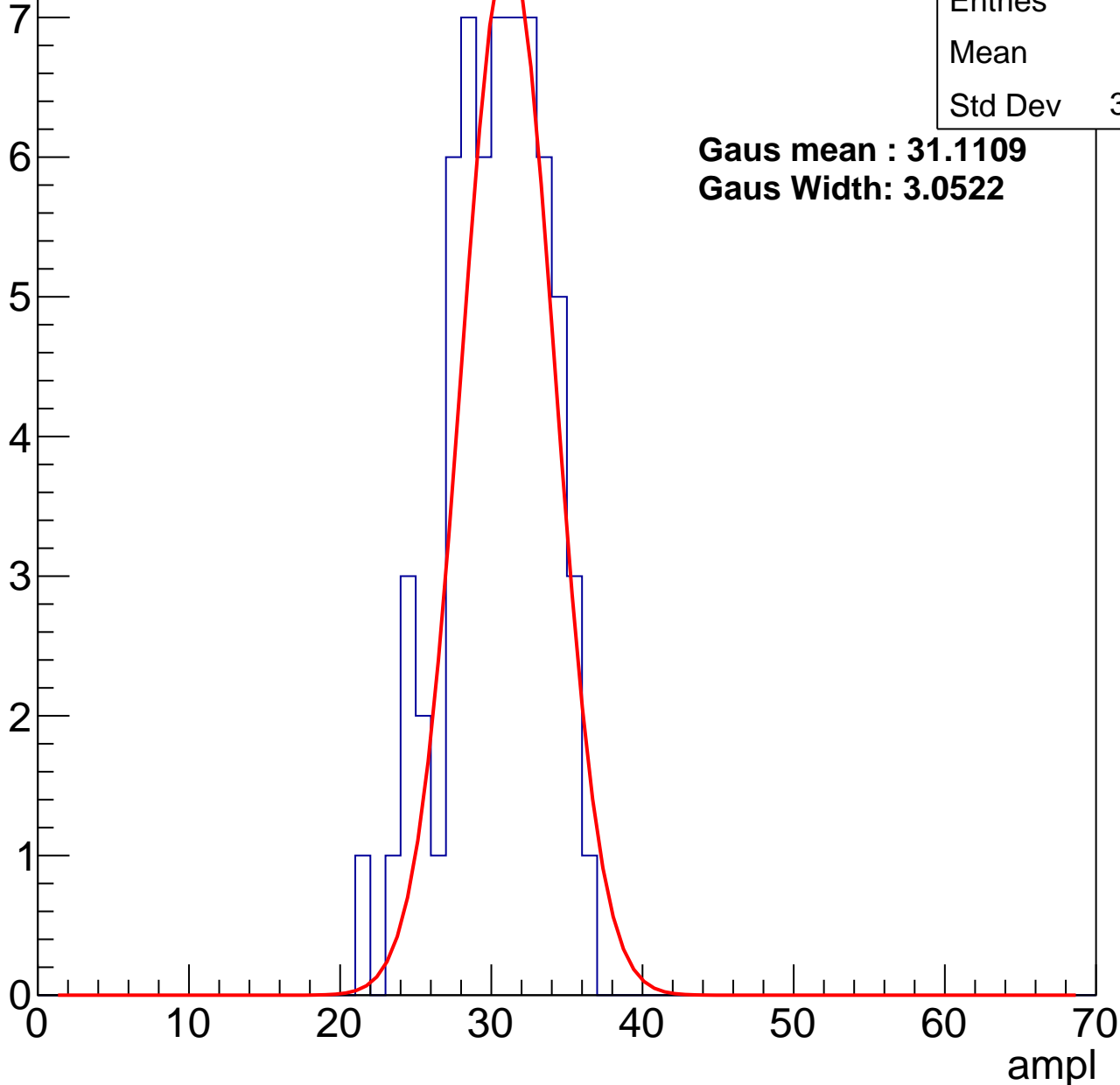
# B1L101S, U8-ch21, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	29.9
Std Dev	3.265

**Gaus mean : 31.1109**  
**Gaus Width: 3.0522**



# B1L101S, U8-ch21, adc1

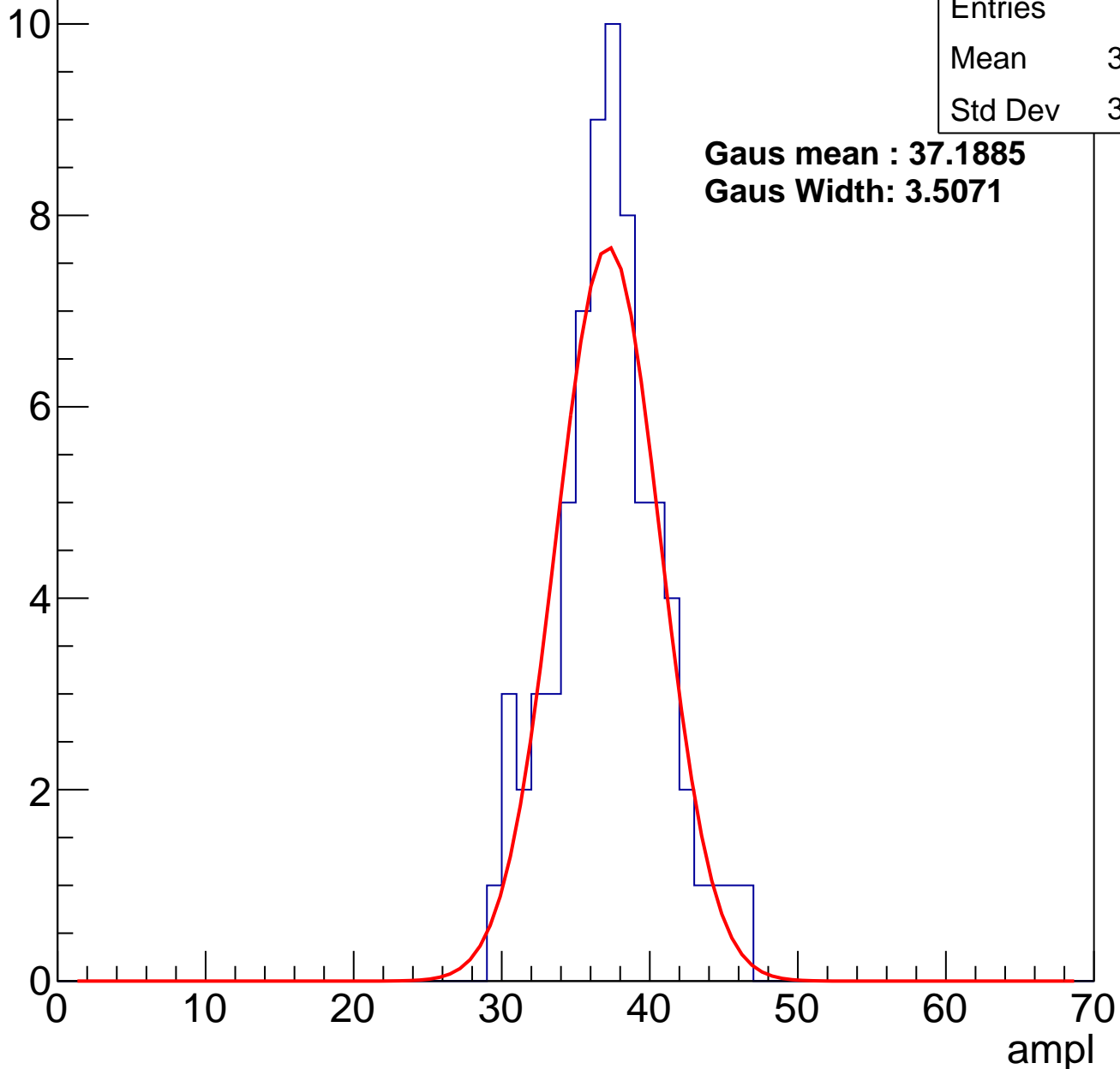
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	71
Mean	36.76
Std Dev	3.562

**Gaus mean : 37.1885**

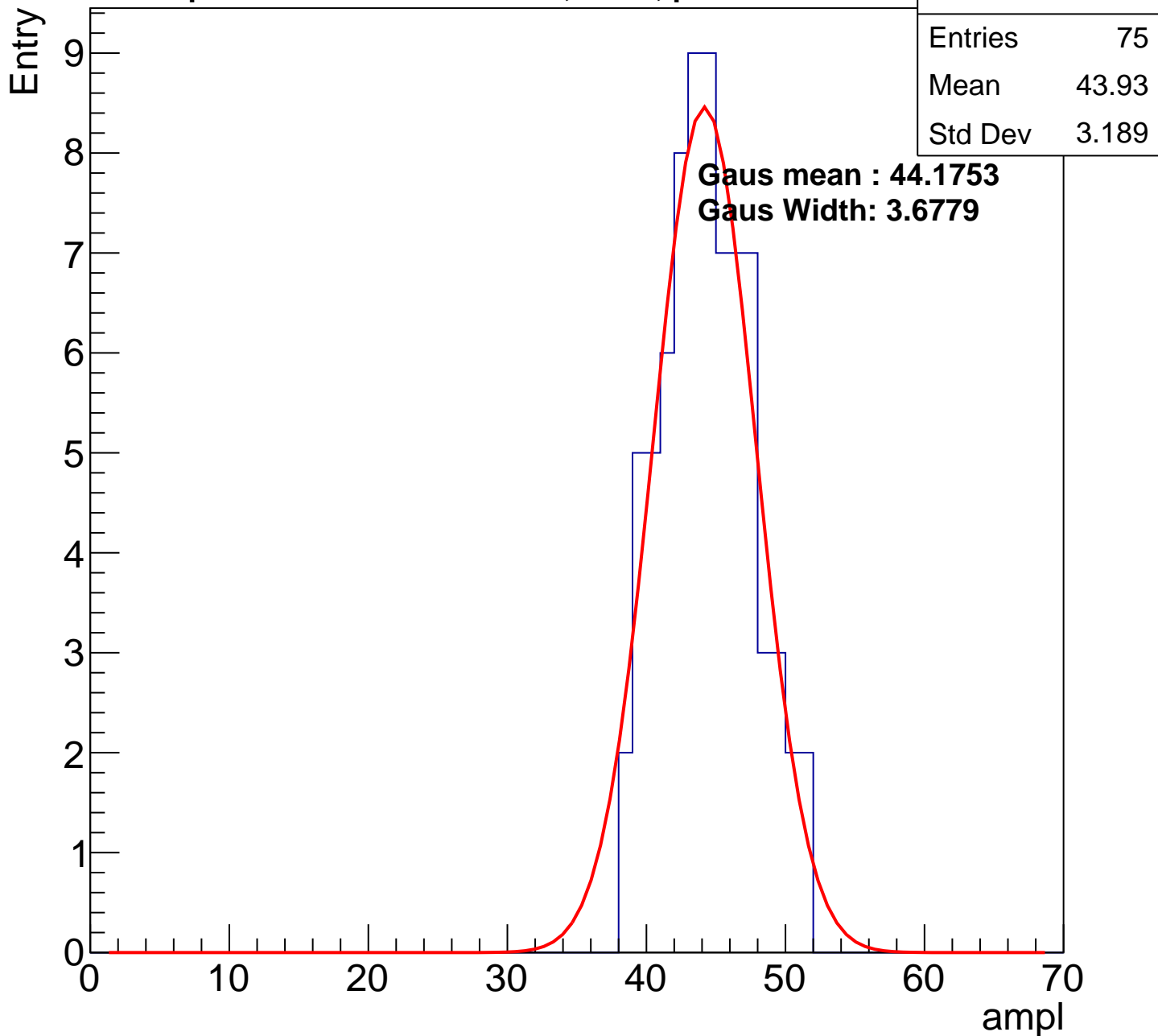
**Gaus Width: 3.5071**

Entry



# B1L101S, U8-ch21, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

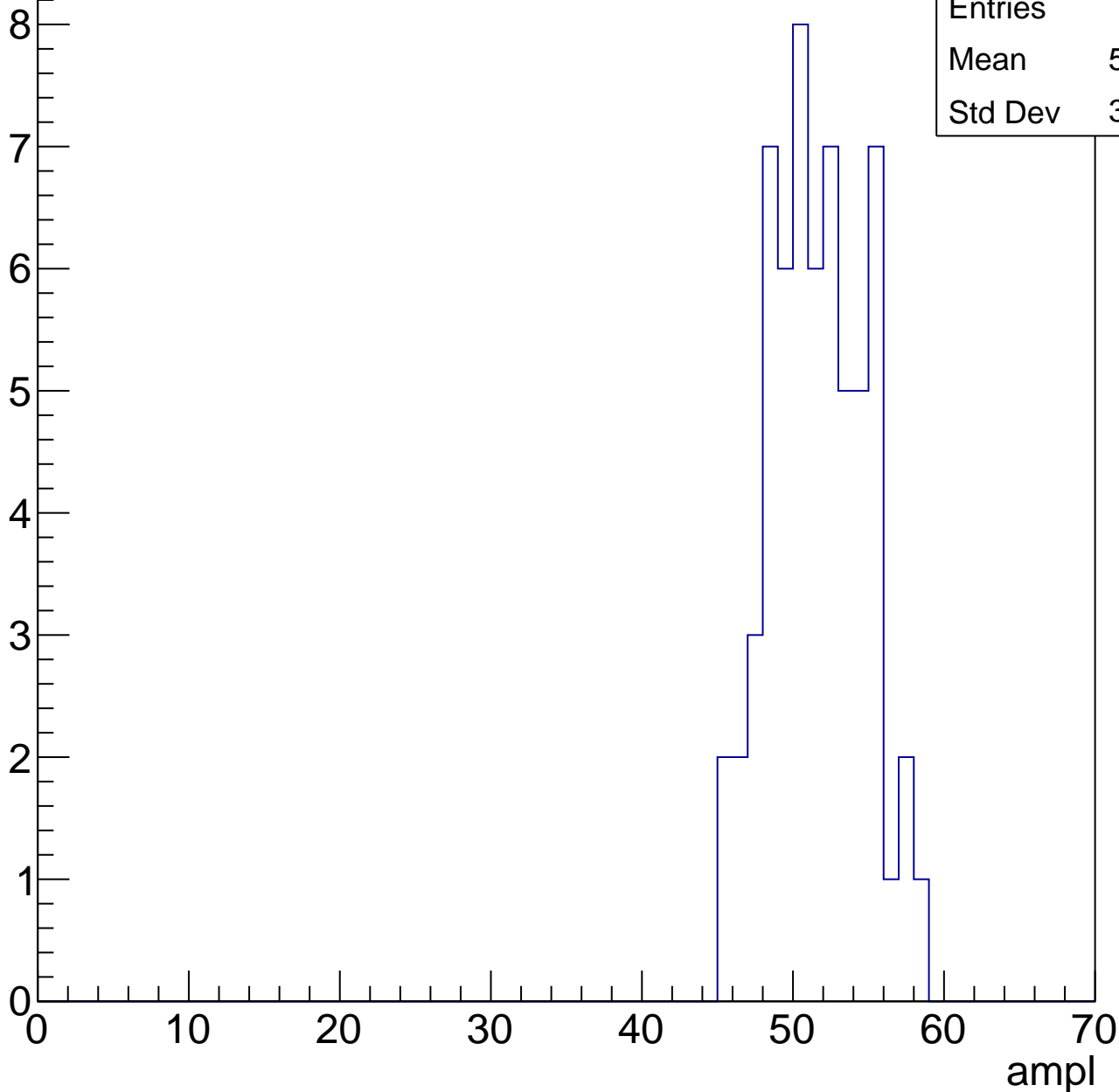


# B1L101S, U8-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	51.15
Std Dev	3.094

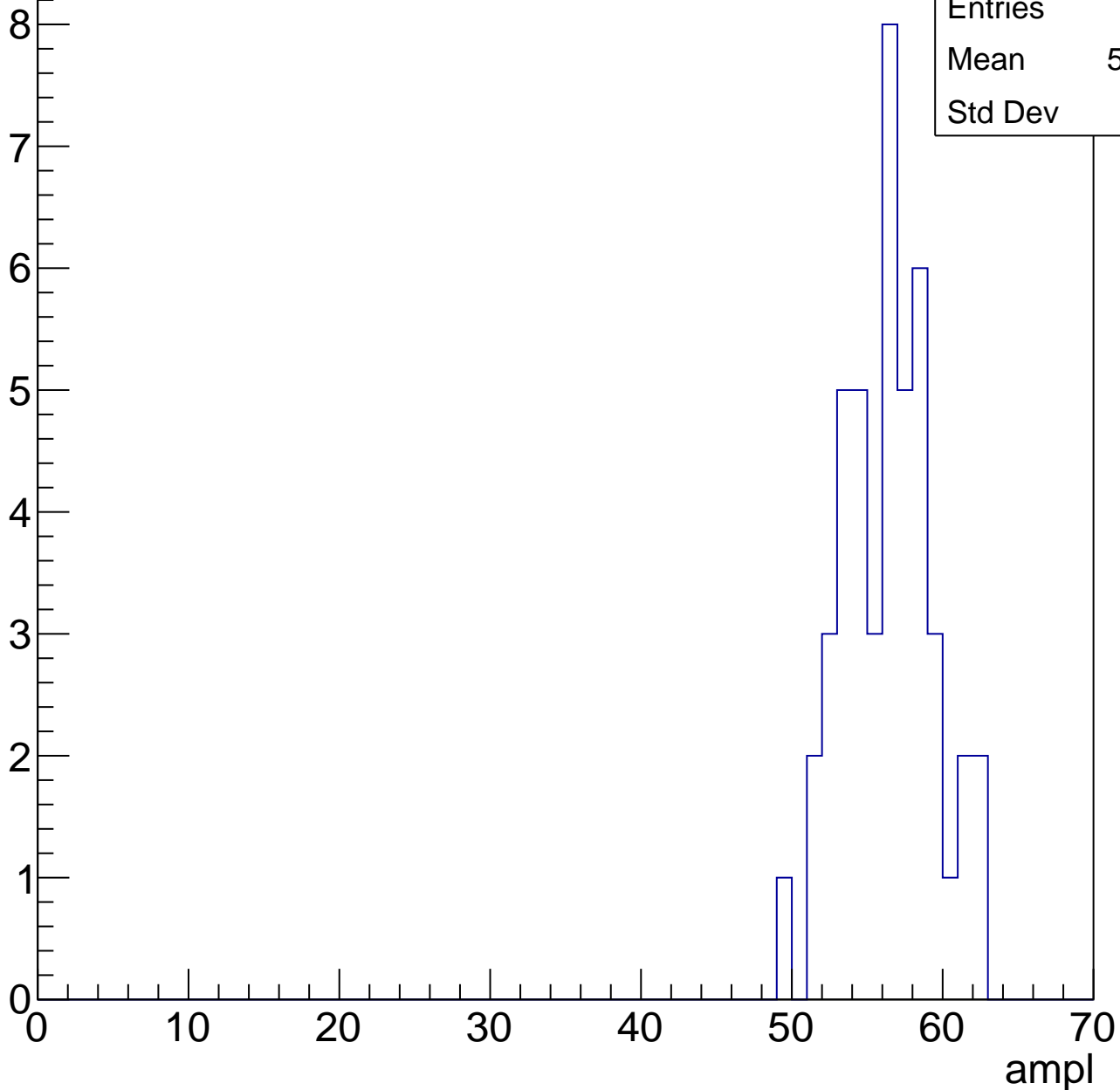


# B1L101S, U8-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

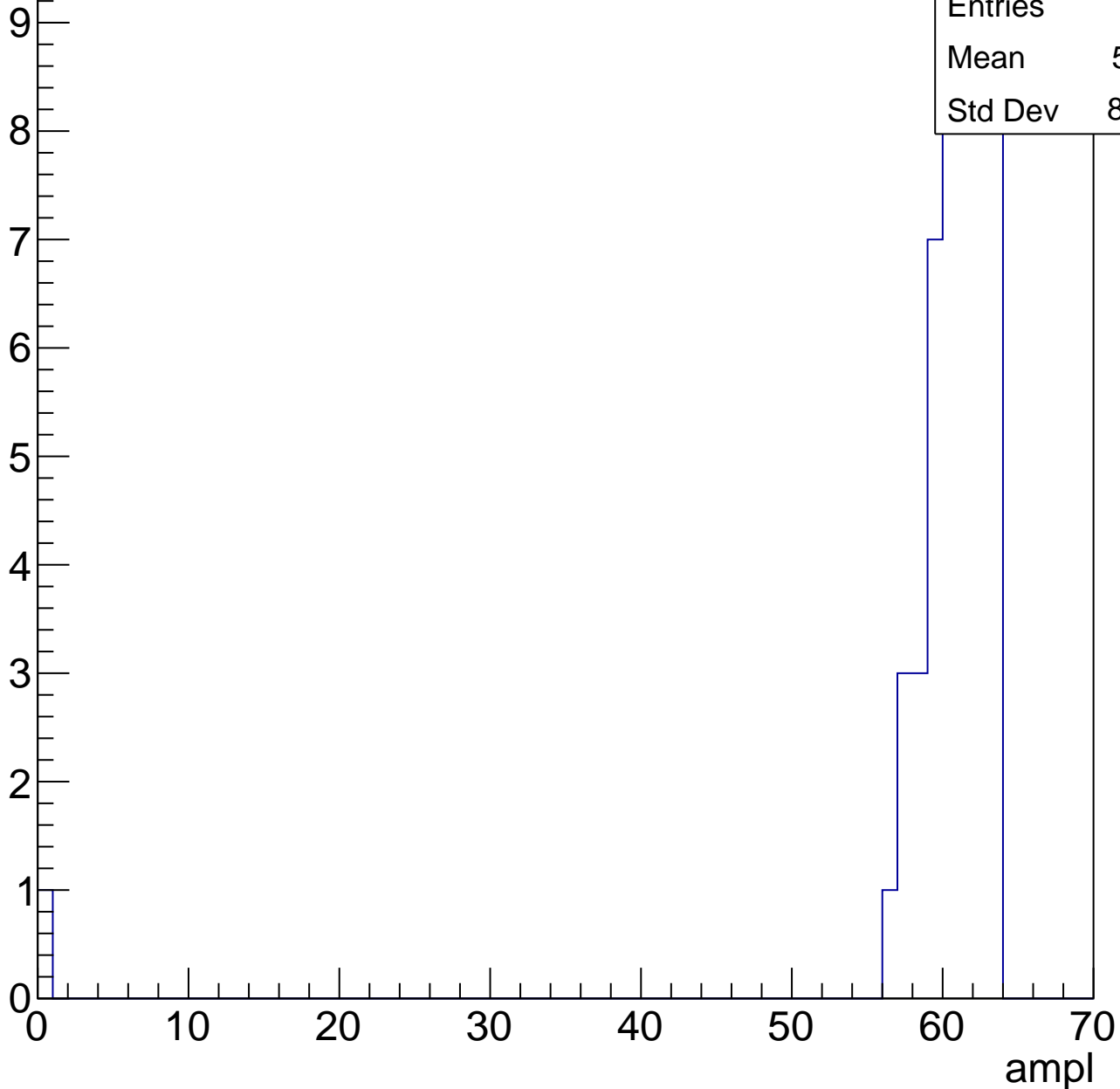
Entries	46
Mean	55.89
Std Dev	2.98



# B1L101S, U8-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch22, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	66
Mean	30.44
Std Dev	3.331

**Gaus mean : 30.7711**

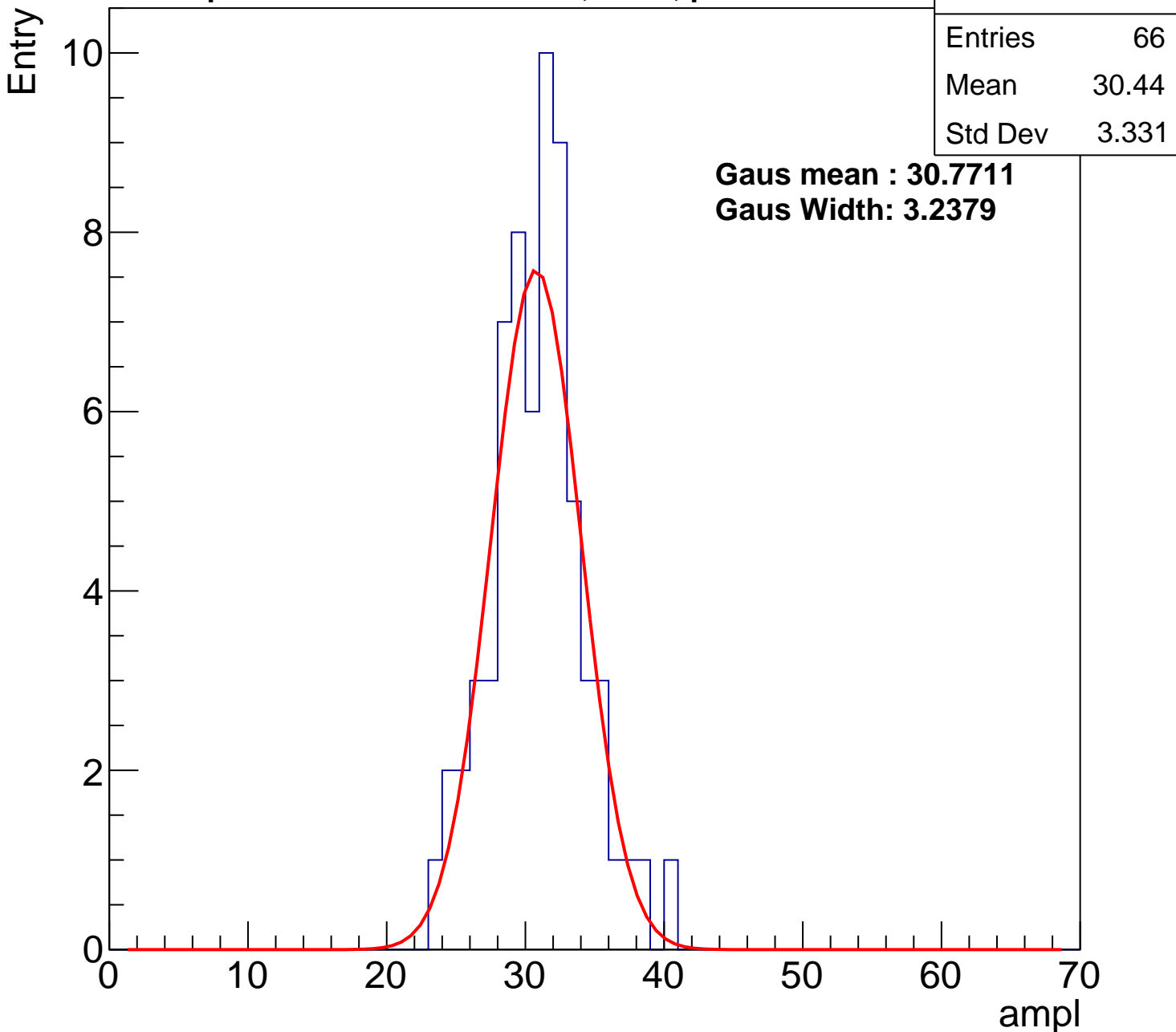
**Gaus Width: 3.2379**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U8-ch22, adc1

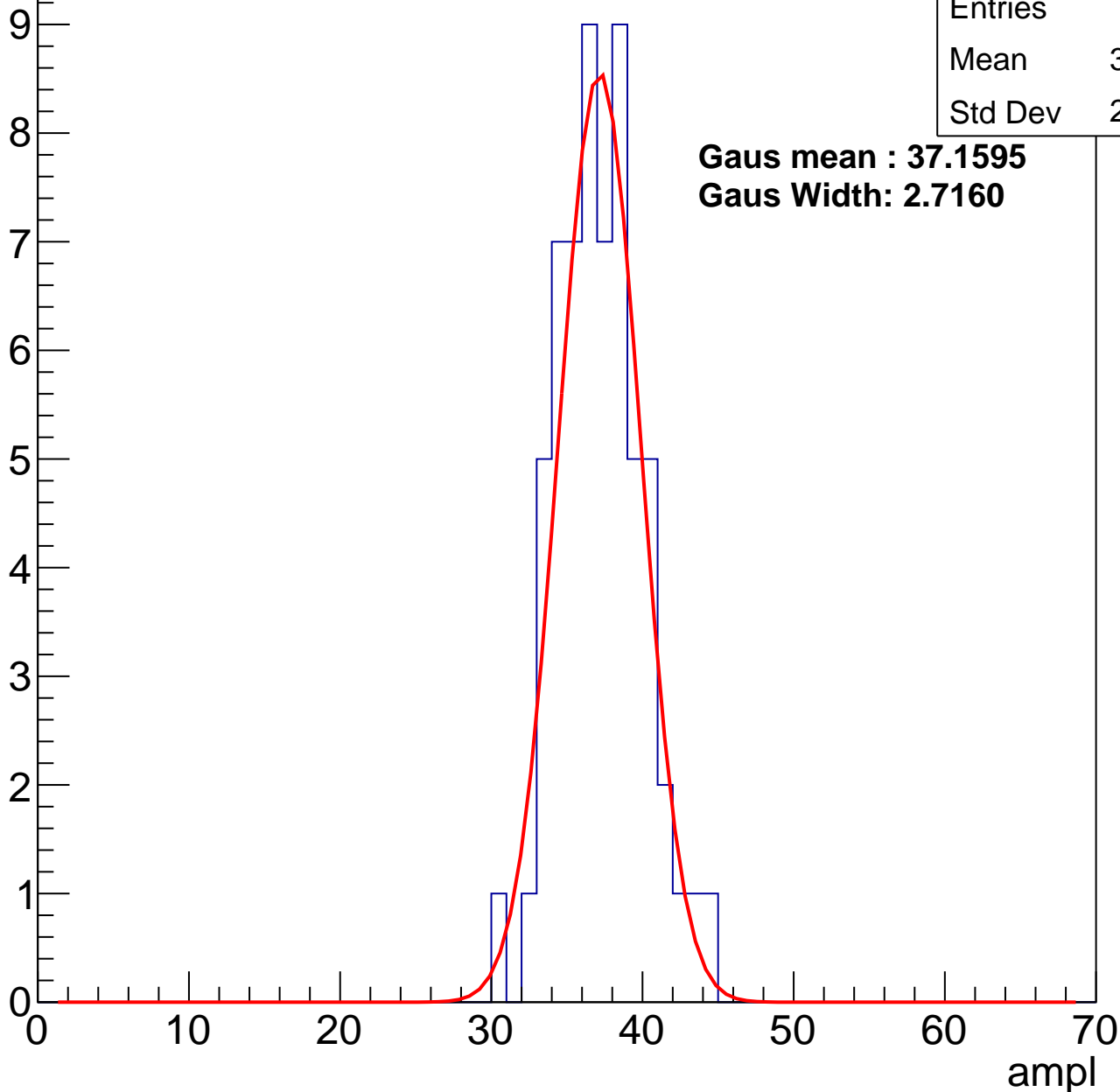
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	36.74
Std Dev	2.763

**Gaus mean : 37.1595**

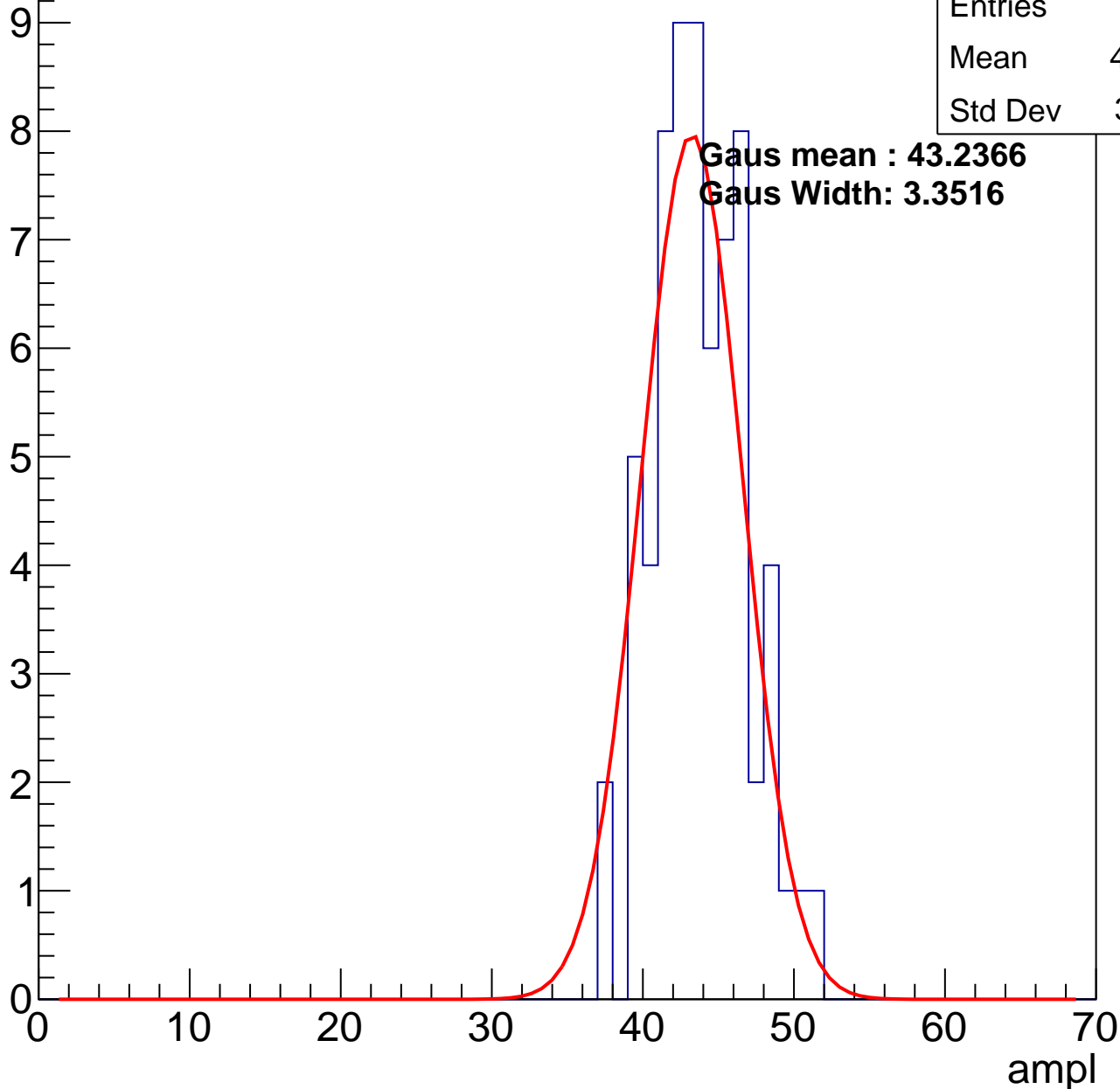
**Gaus Width: 2.7160**



# B1L101S, U8-ch22, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

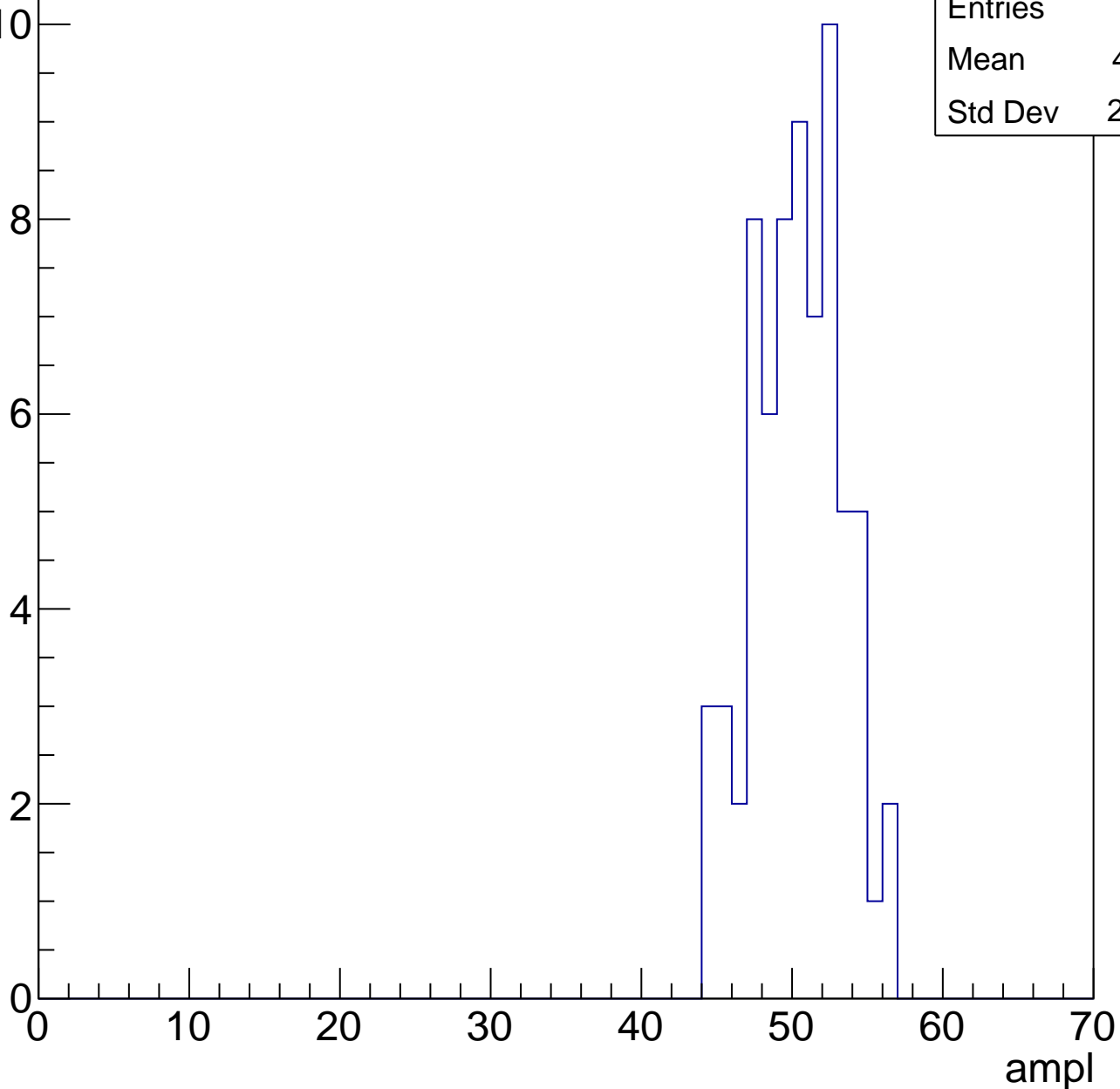


# B1L101S, U8-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

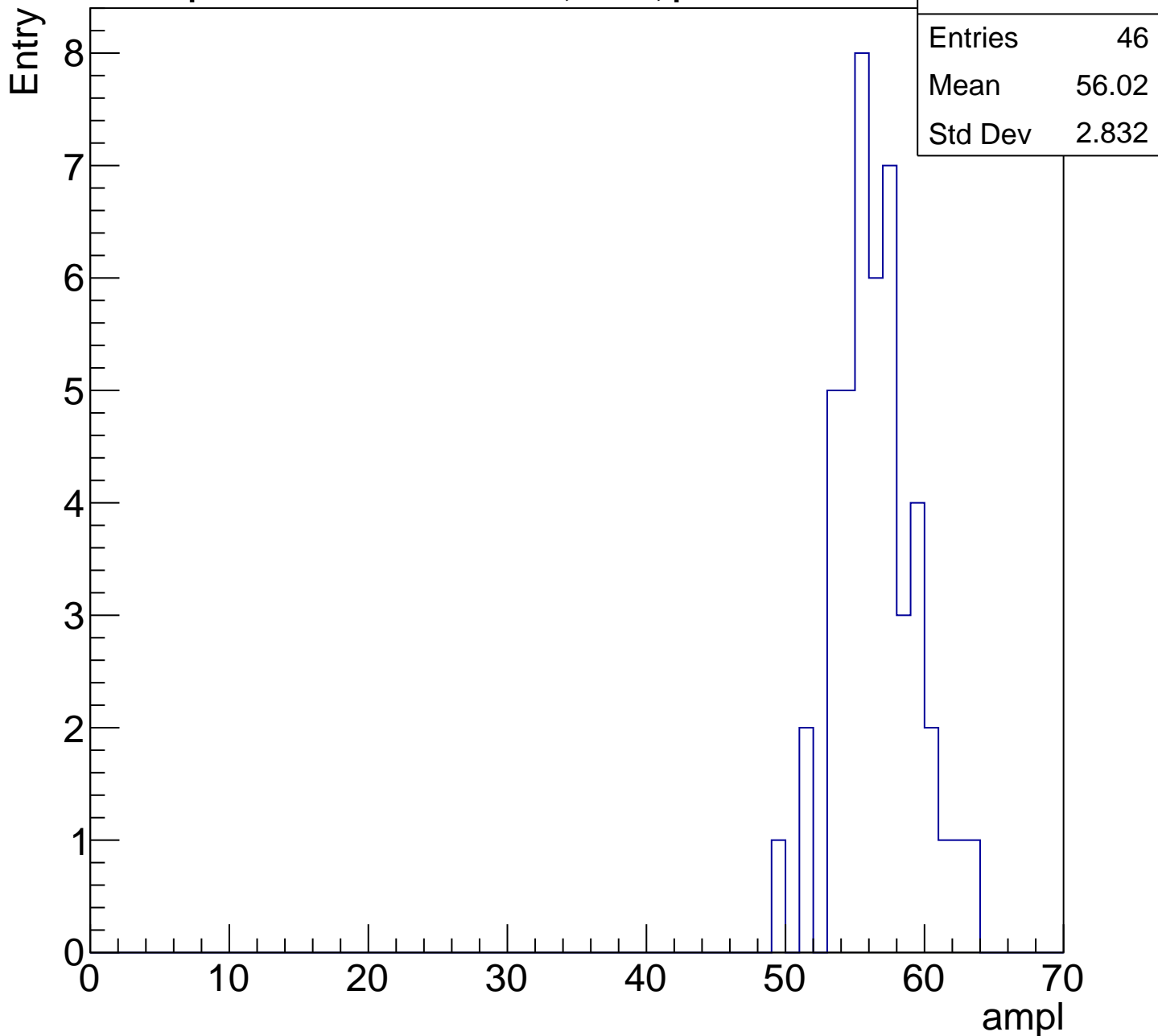
Entry

Entries	69
Mean	49.91
Std Dev	2.918



# B1L101S, U8-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U8-ch22, adc5

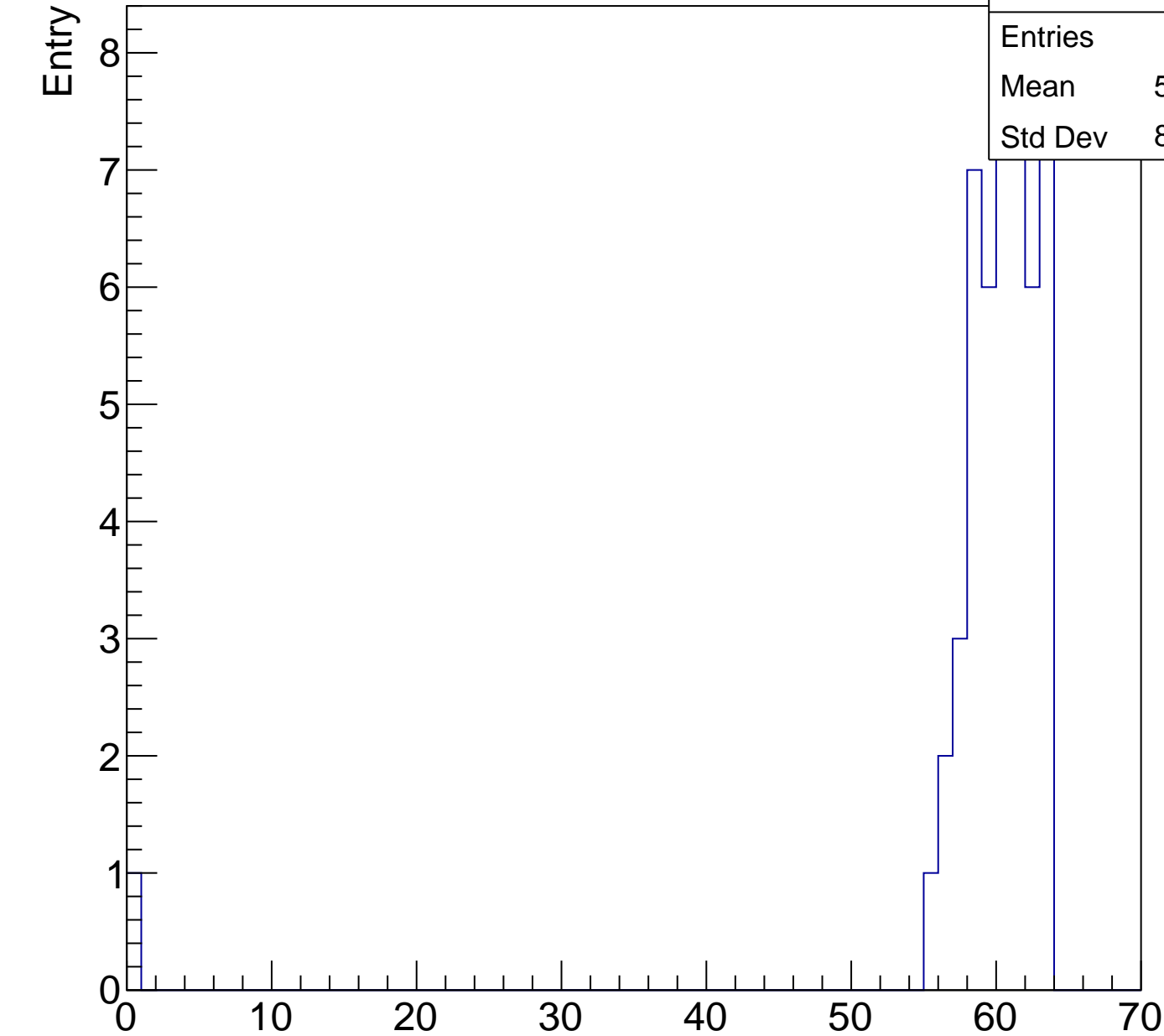
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	50
Mean	58.84
Std Dev	8.666

ampl



# B1L101S, U8-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch23, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	74
Mean	29.51
Std Dev	5.086

**Gaus mean : 29.6659**

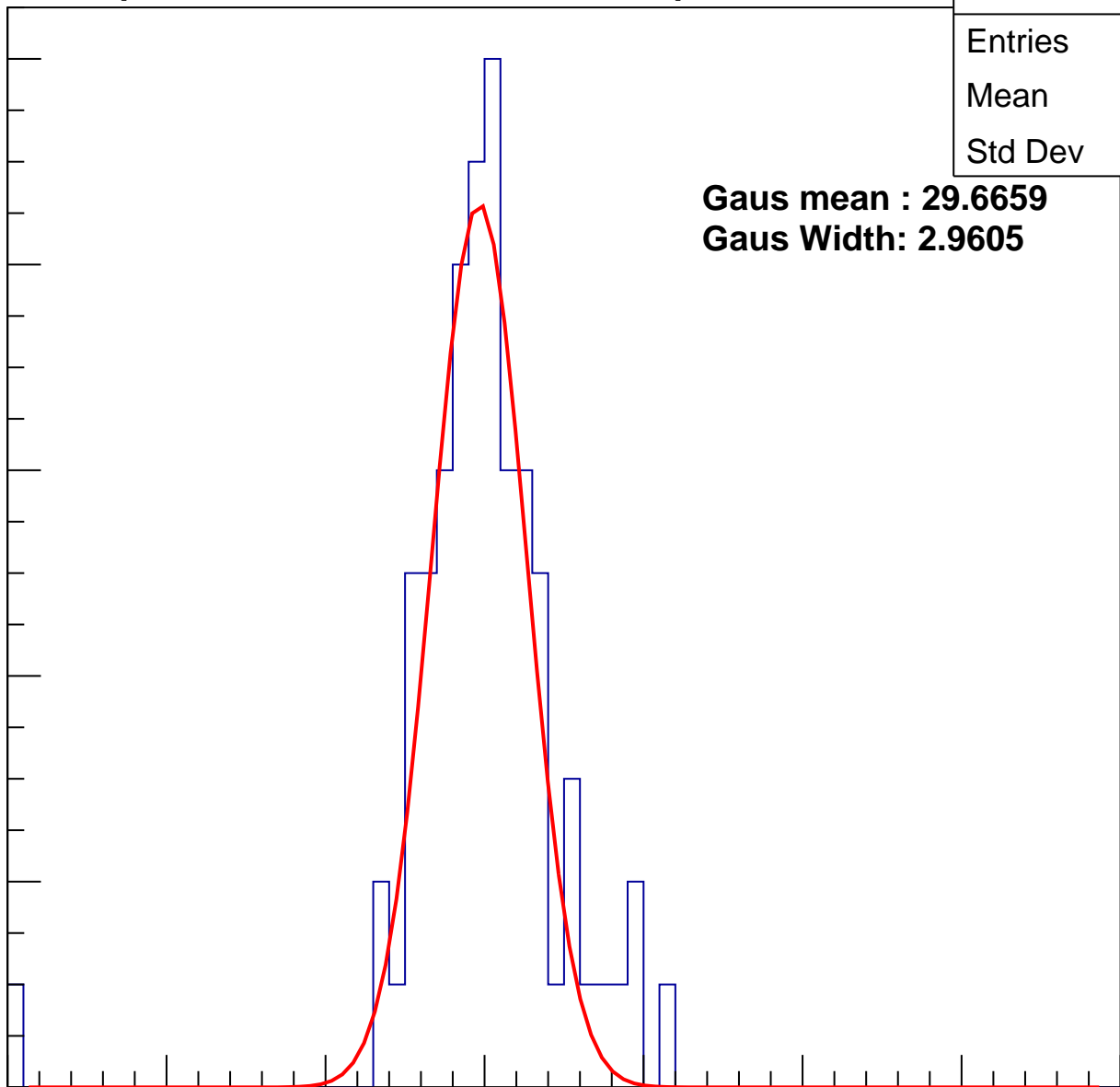
**Gaus Width: 2.9605**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U8-ch23, adc1

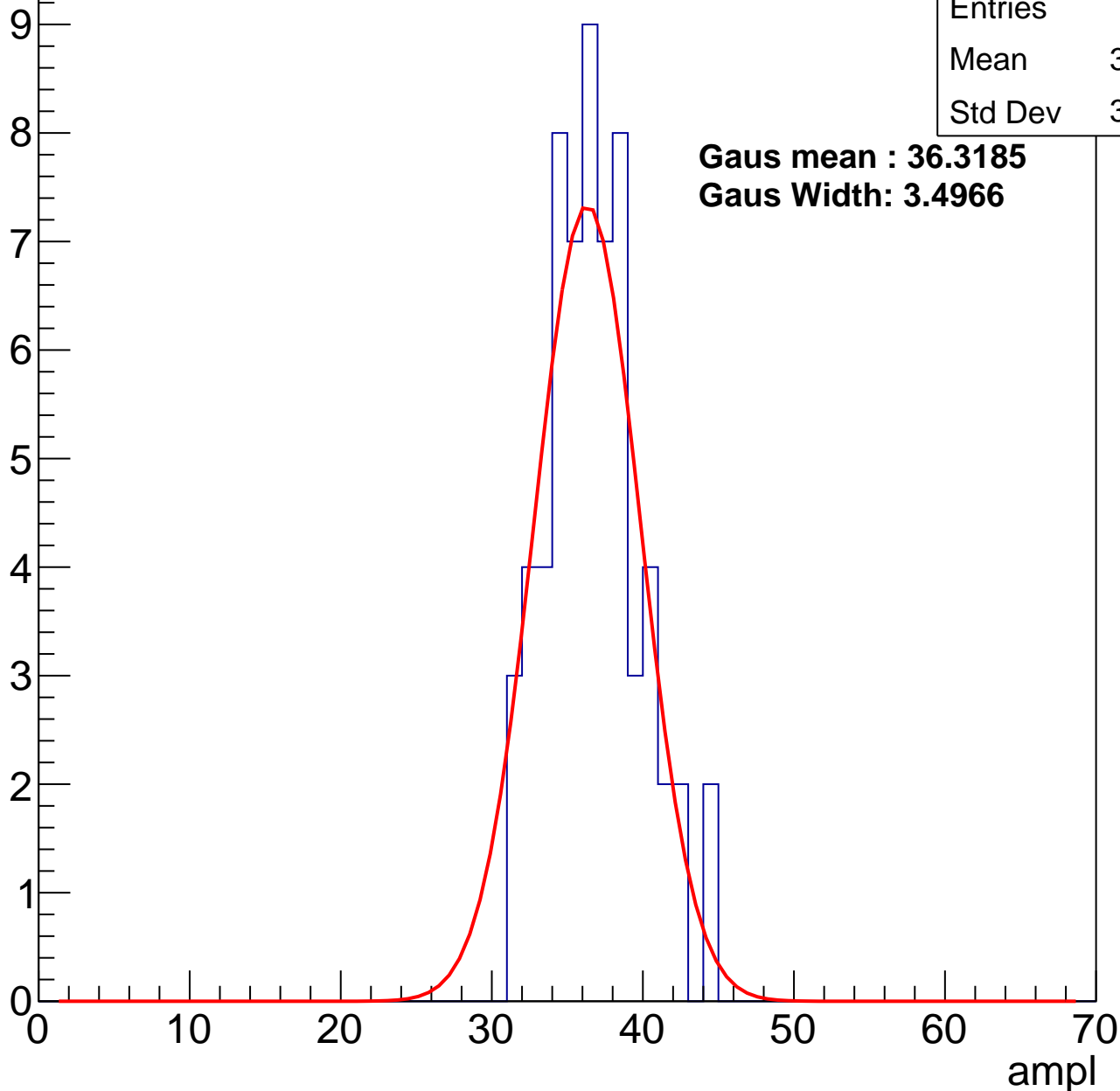
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	36.32
Std Dev	3.054

**Gaus mean : 36.3185**

**Gaus Width: 3.4966**



# B1L101S, U8-ch23, adc2

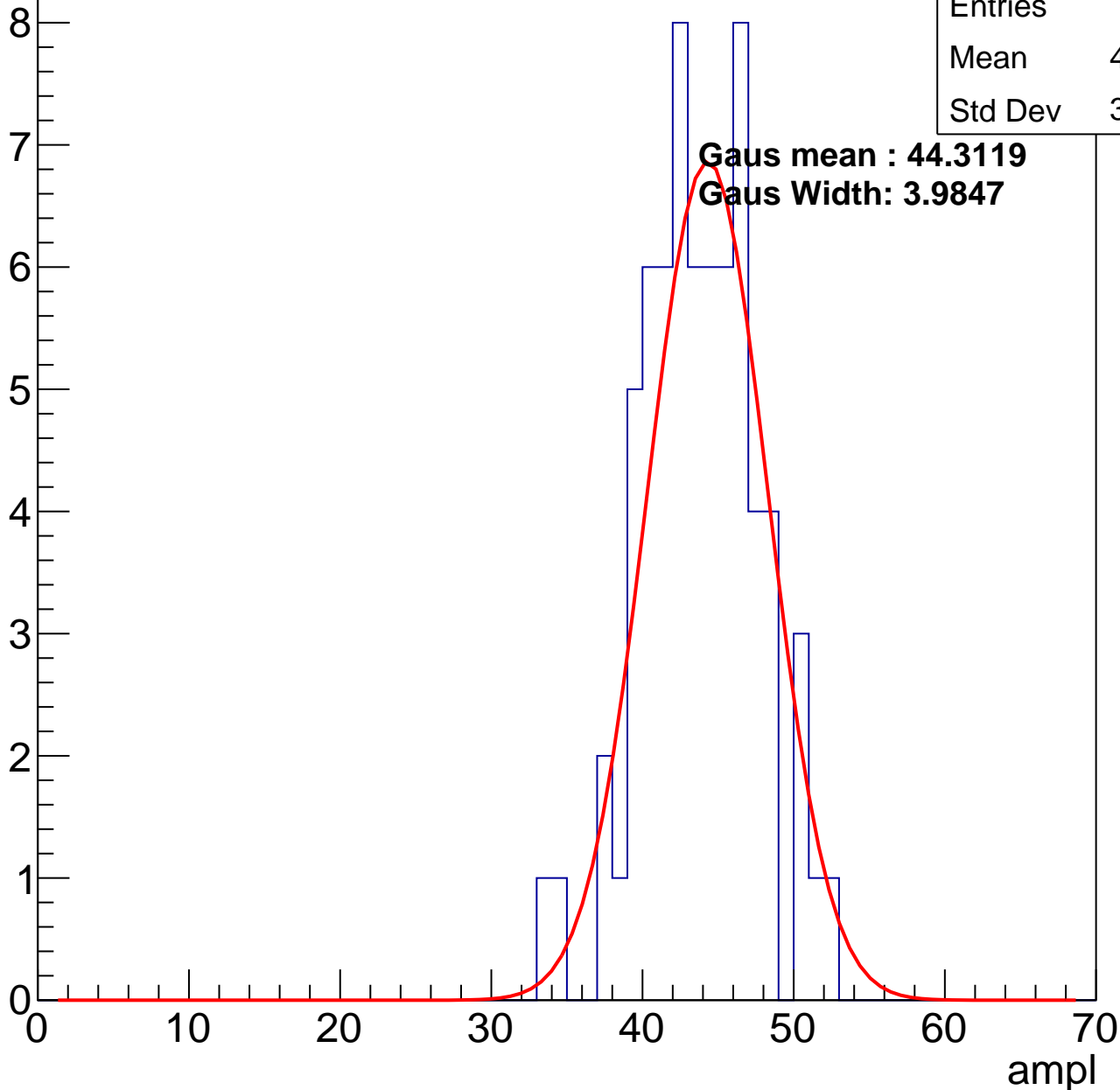
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	43.32
Std Dev	3.797

**Gaus mean : 44.3119**

**Gaus Width: 3.9847**



# B1L101S, U8-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

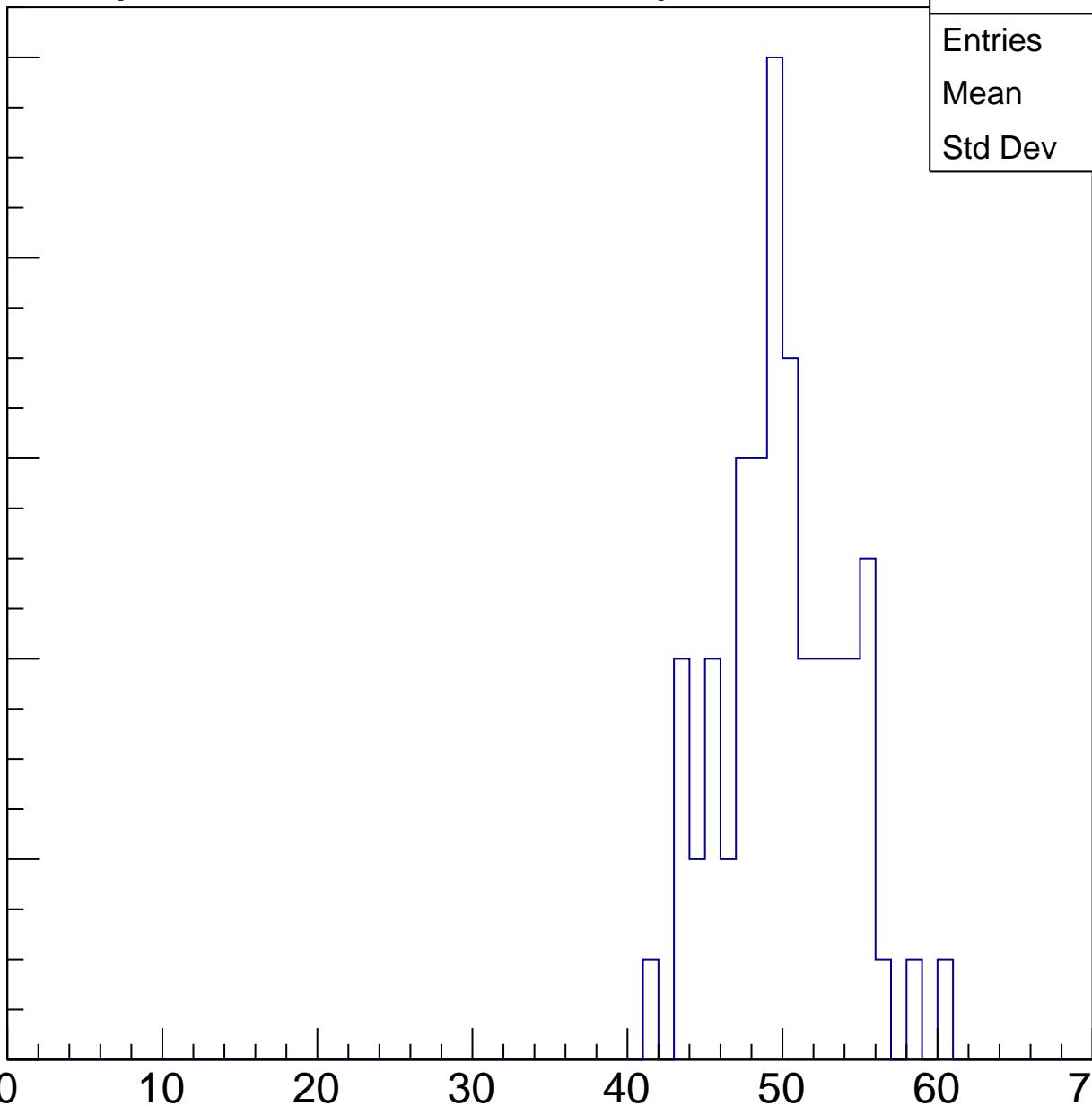
Entries	66
Mean	49.58
Std Dev	3.897

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

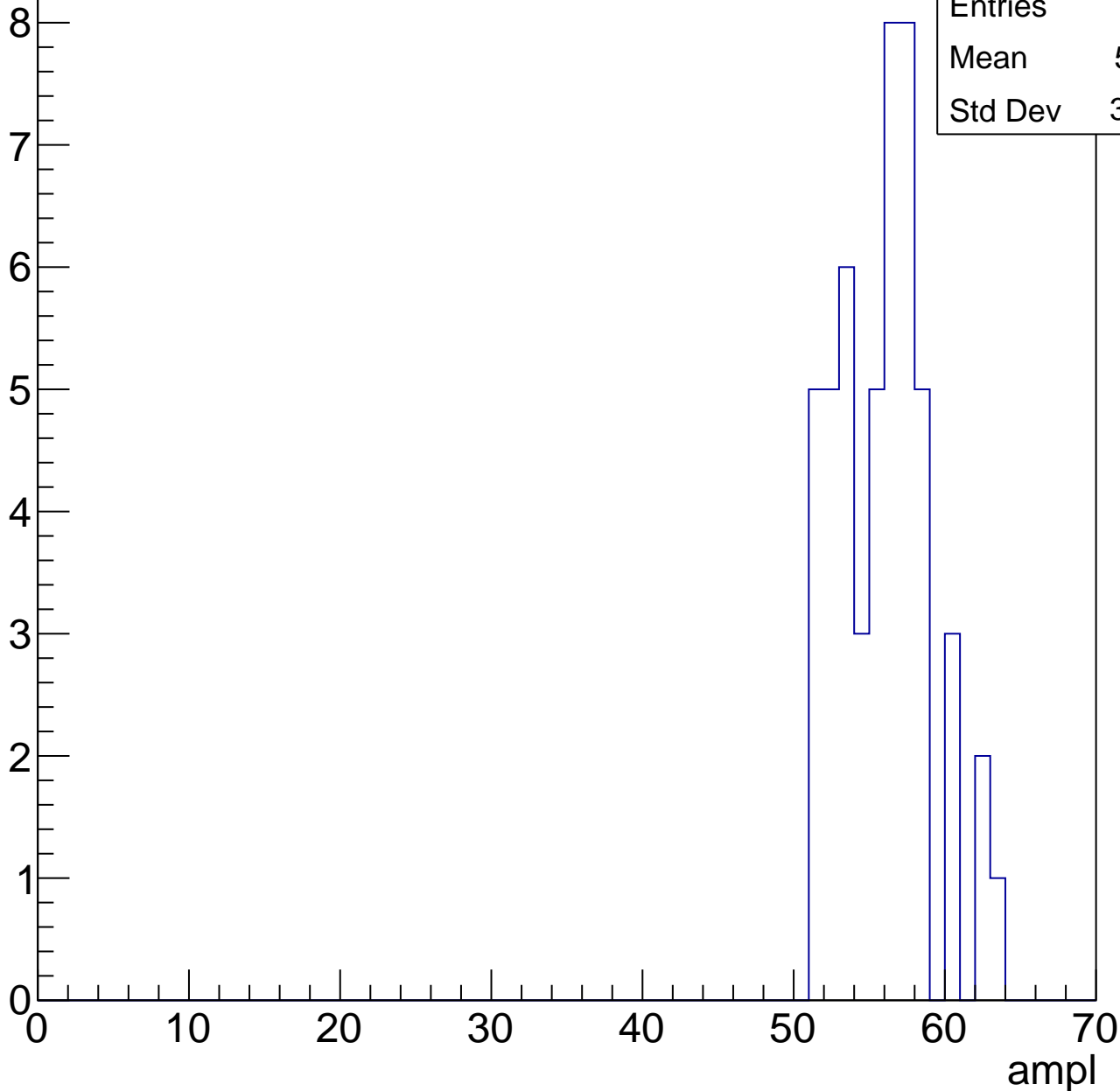


# B1L101S, U8-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	55.51
Std Dev	3.006



# B1L101S, U8-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

10

Entries 48

Mean 58.6

Std Dev 8.852

8

6

4

2

0

0

10

20

30

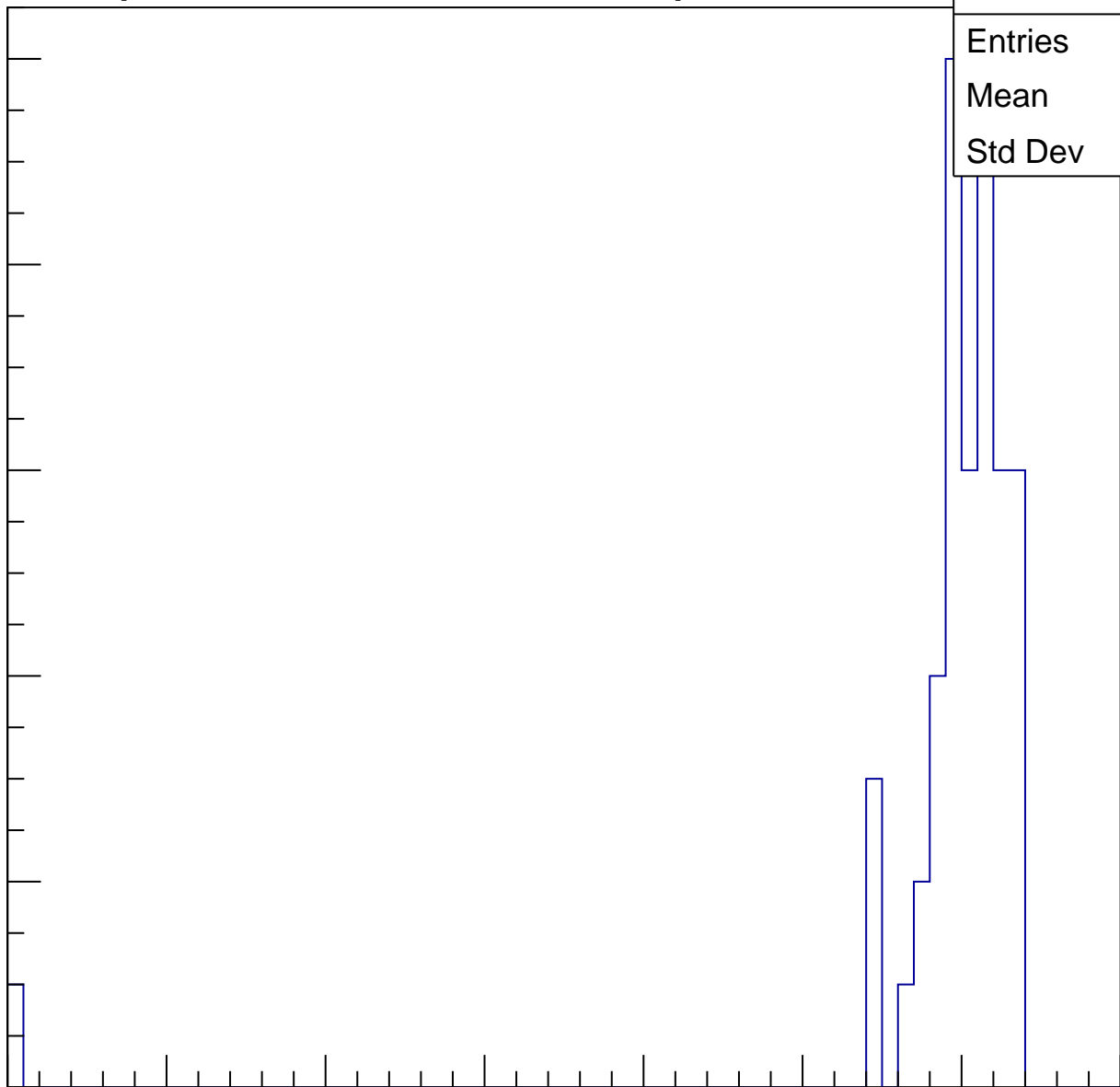
40

50

60

70

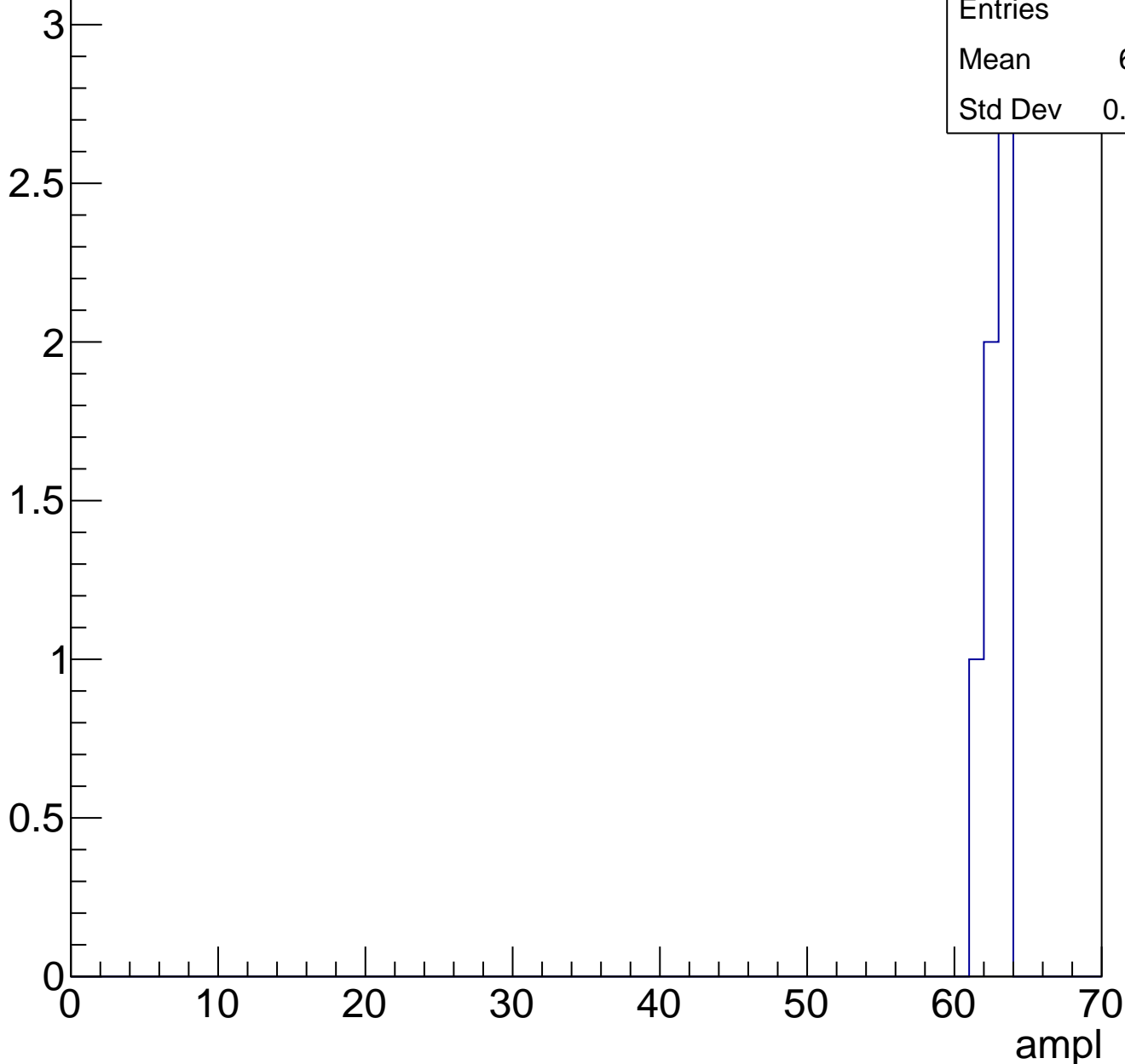
ampl



# B1L101S, U8-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U8-ch24, adc0

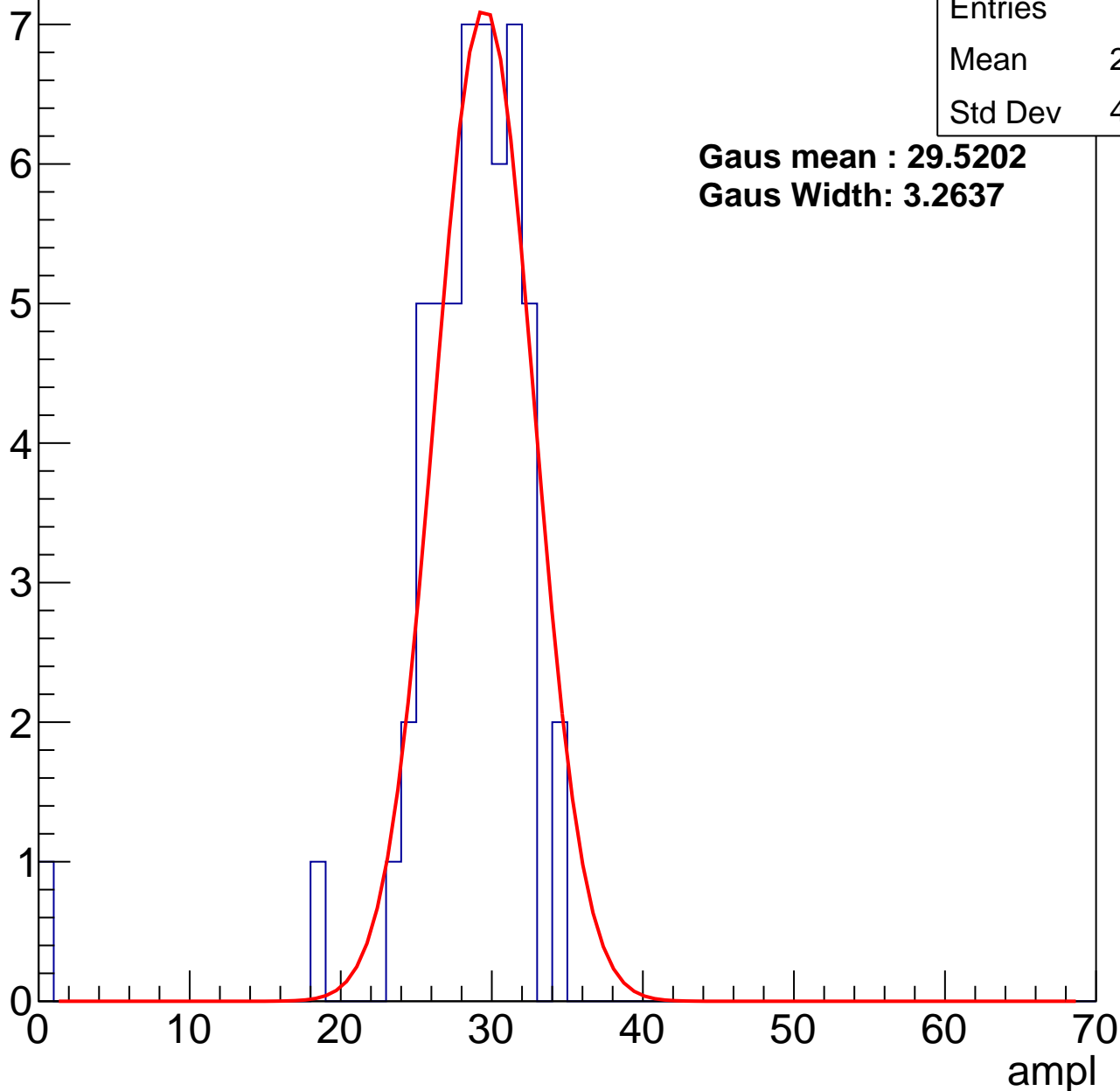
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	27.83
Std Dev	4.822

**Gaus mean : 29.5202**

**Gaus Width: 3.2637**



# B1L101S, U8-ch24, adc1

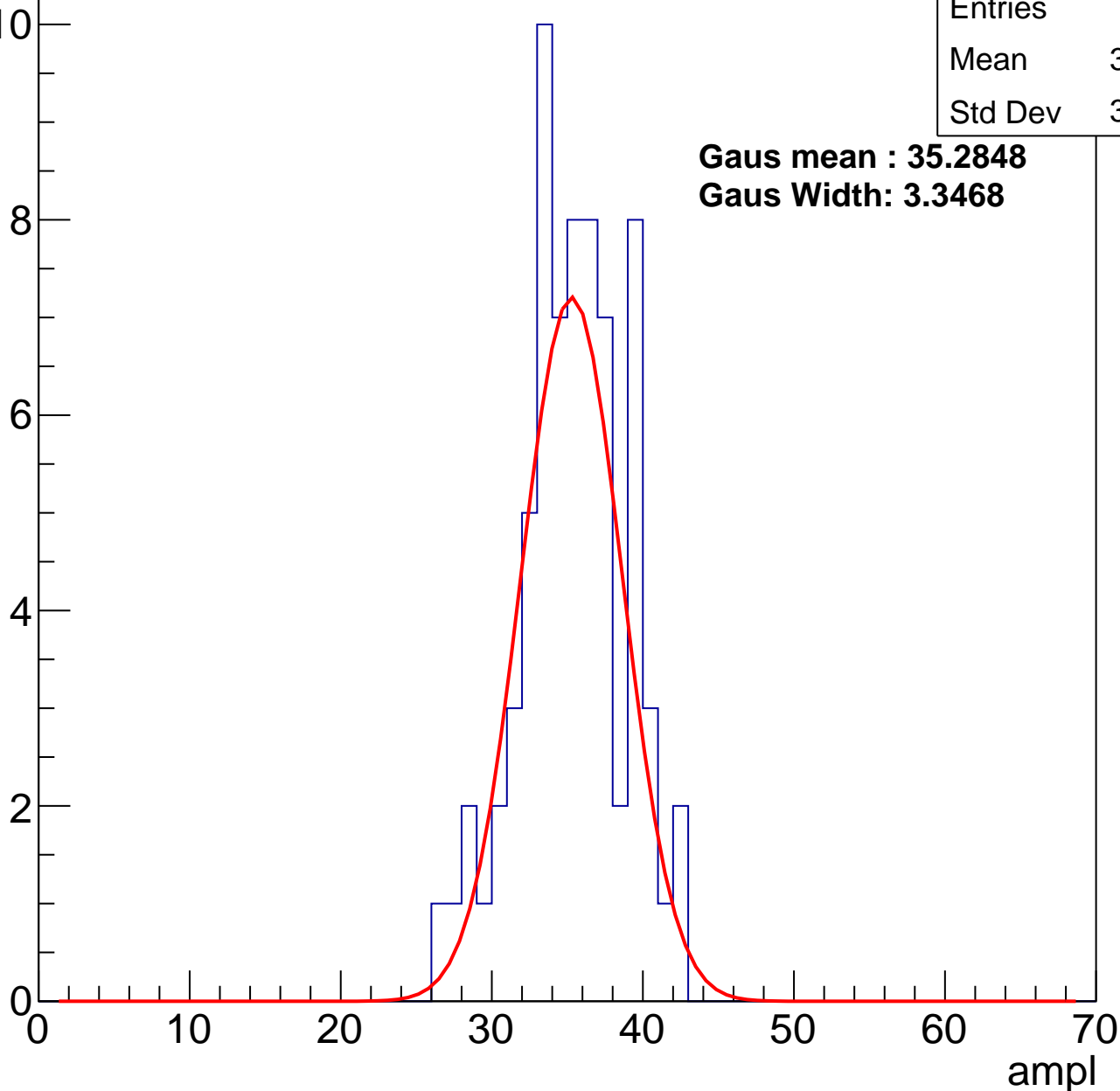
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	34.92
Std Dev	3.479

**Gaus mean : 35.2848**

**Gaus Width: 3.3468**



# B1L101S, U8-ch24, adc2

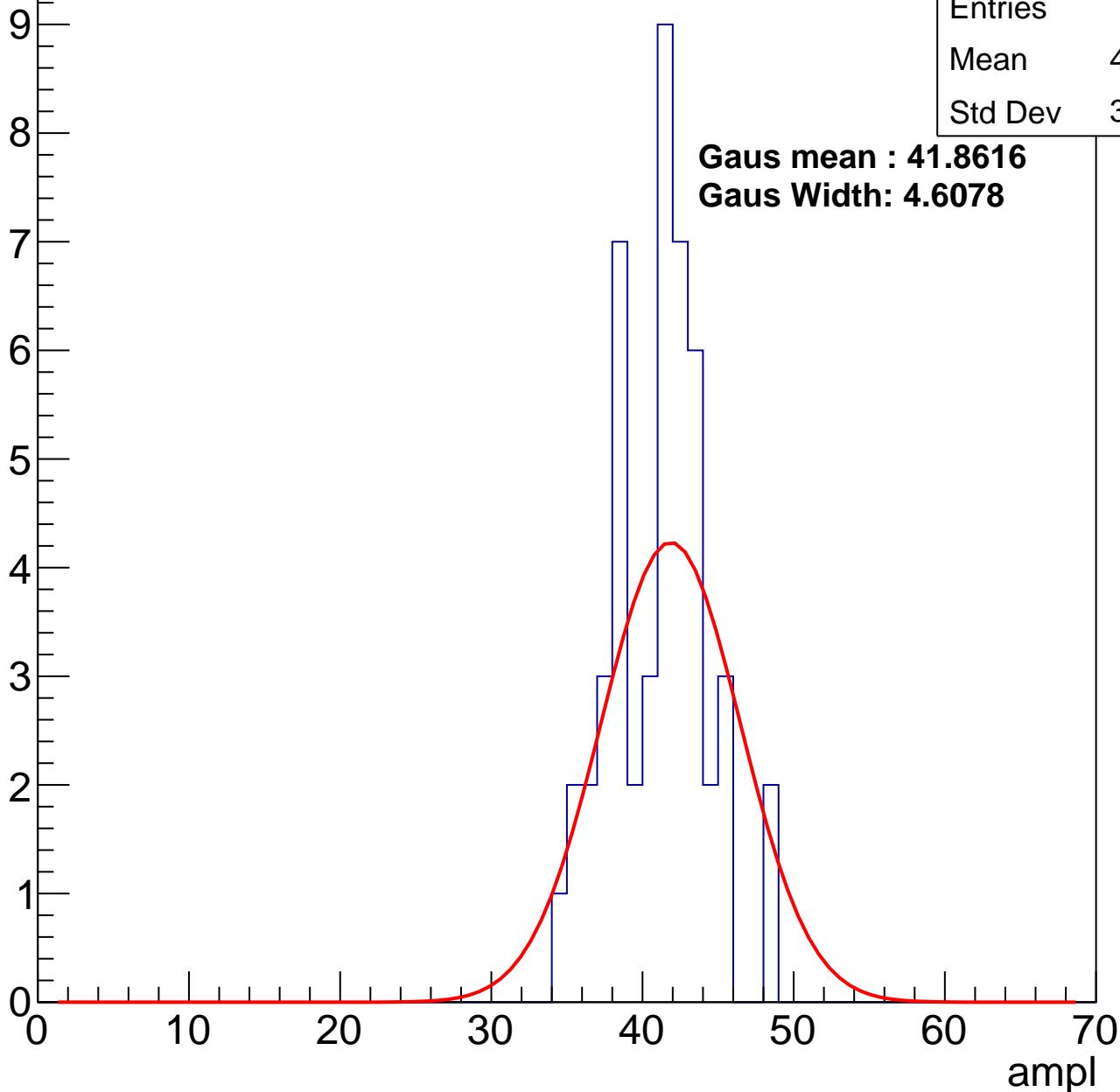
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	40.63
Std Dev	3.134

**Gaus mean : 41.8616**

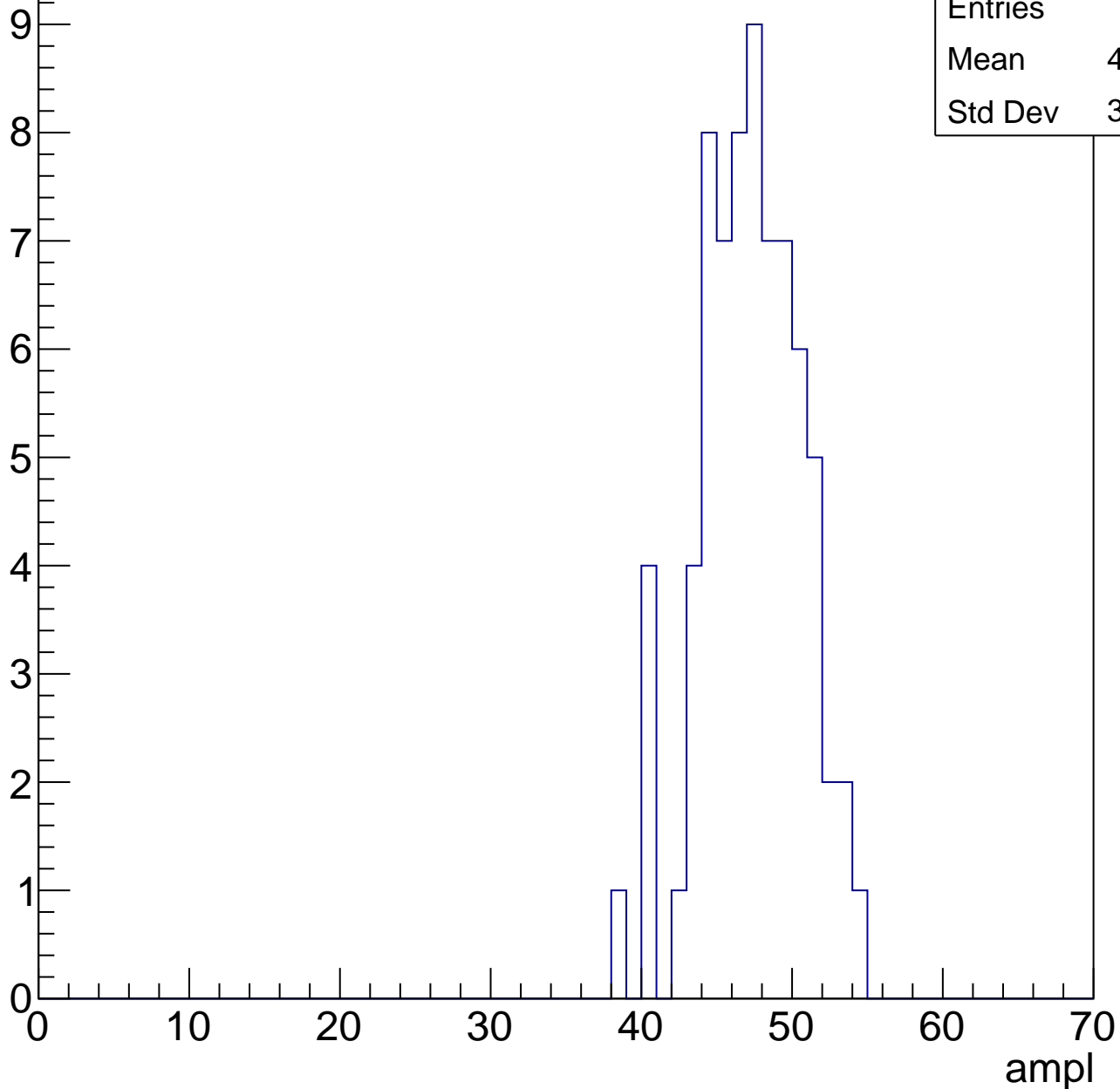
**Gaus Width: 4.6078**



# B1L101S, U8-ch24, adc3

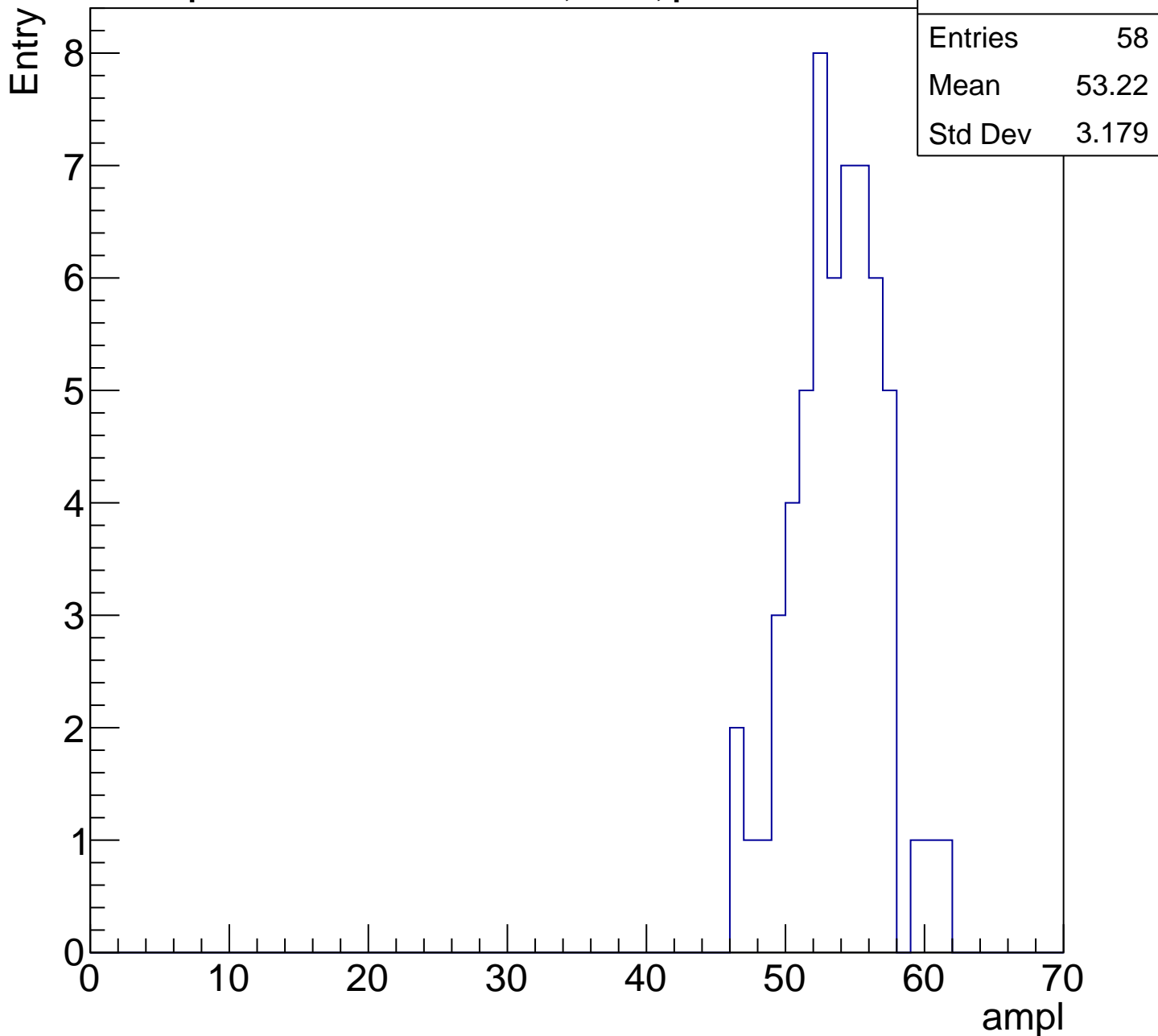
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

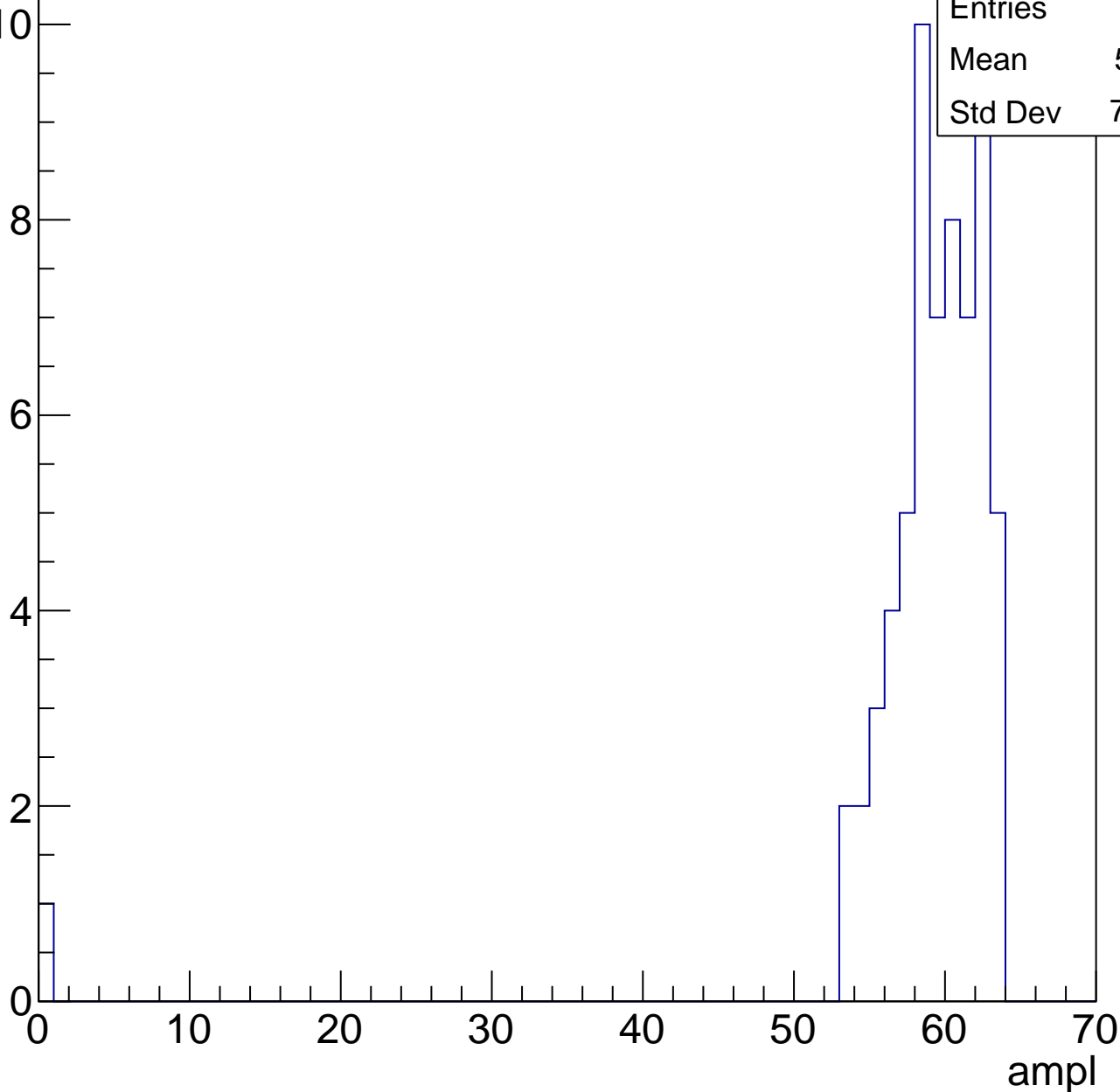


# B1L101S, U8-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	58.11
Std Dev	7.832

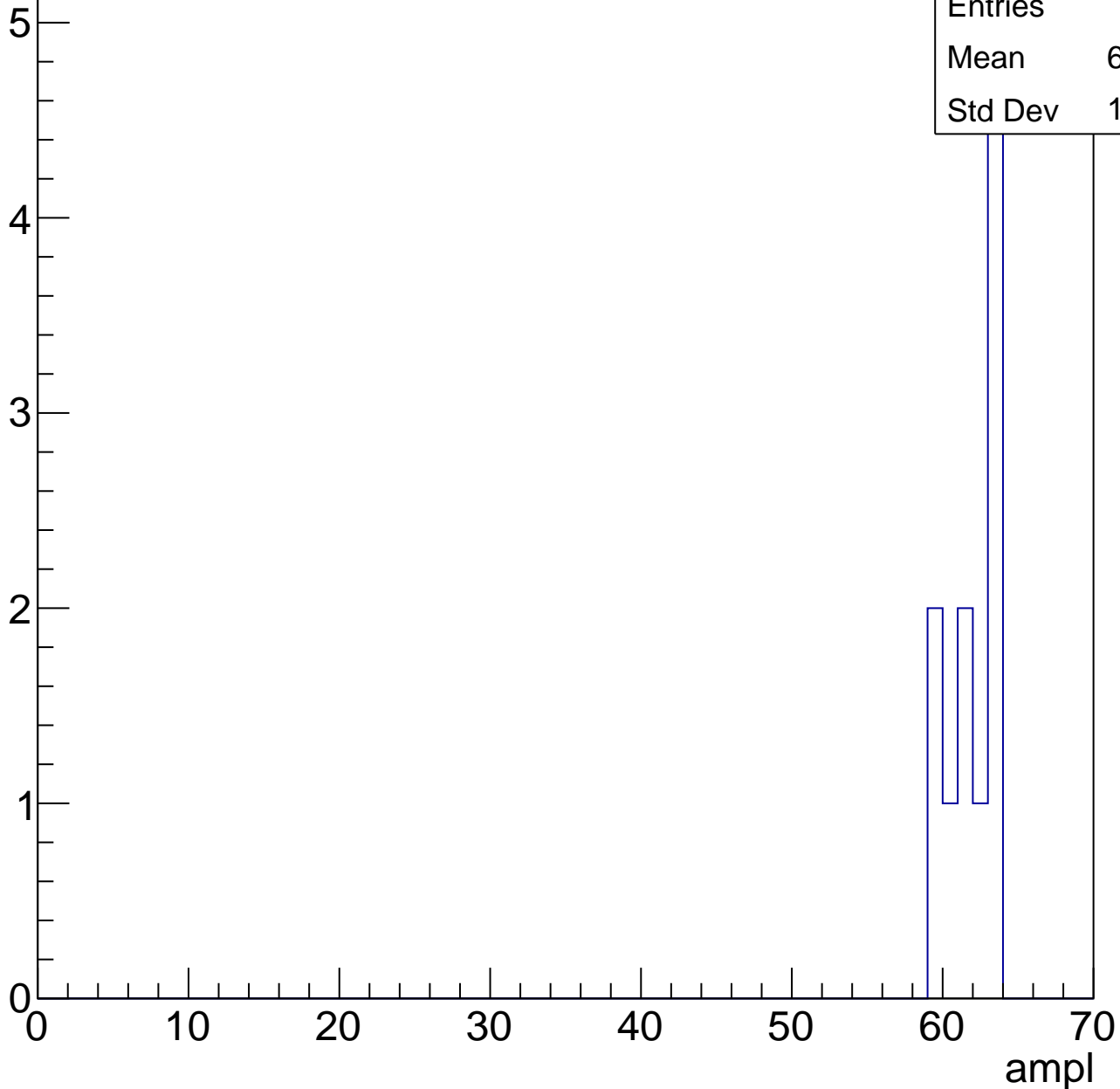


# B1L101S, U8-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	11
Mean	61.55
Std Dev	1.559





# B1L101S, U8-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch25, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	92
Mean	29.53
Std Dev	5.73

**Gaus mean : 30.9633**

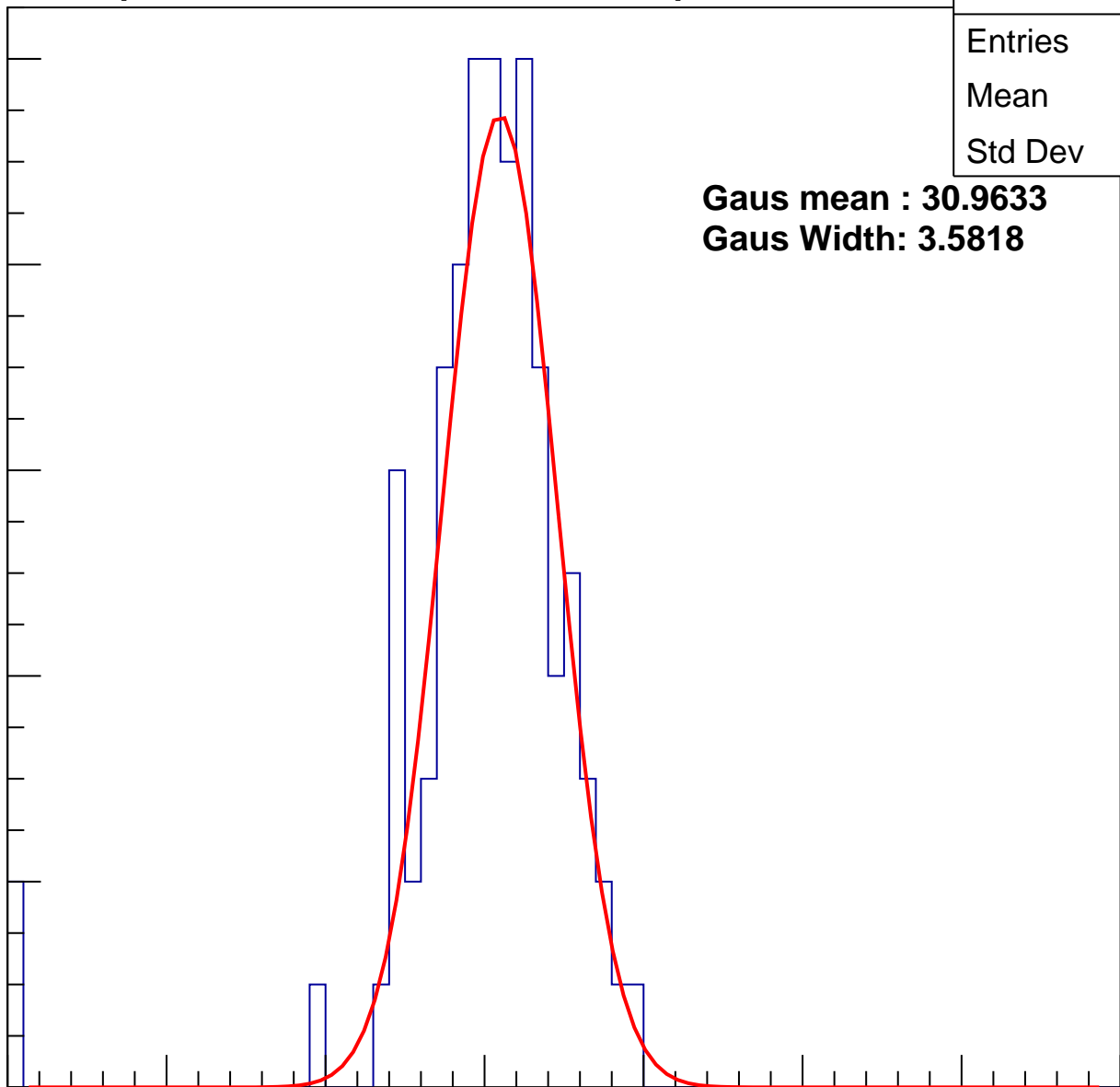
**Gaus Width: 3.5818**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U8-ch25, adc1

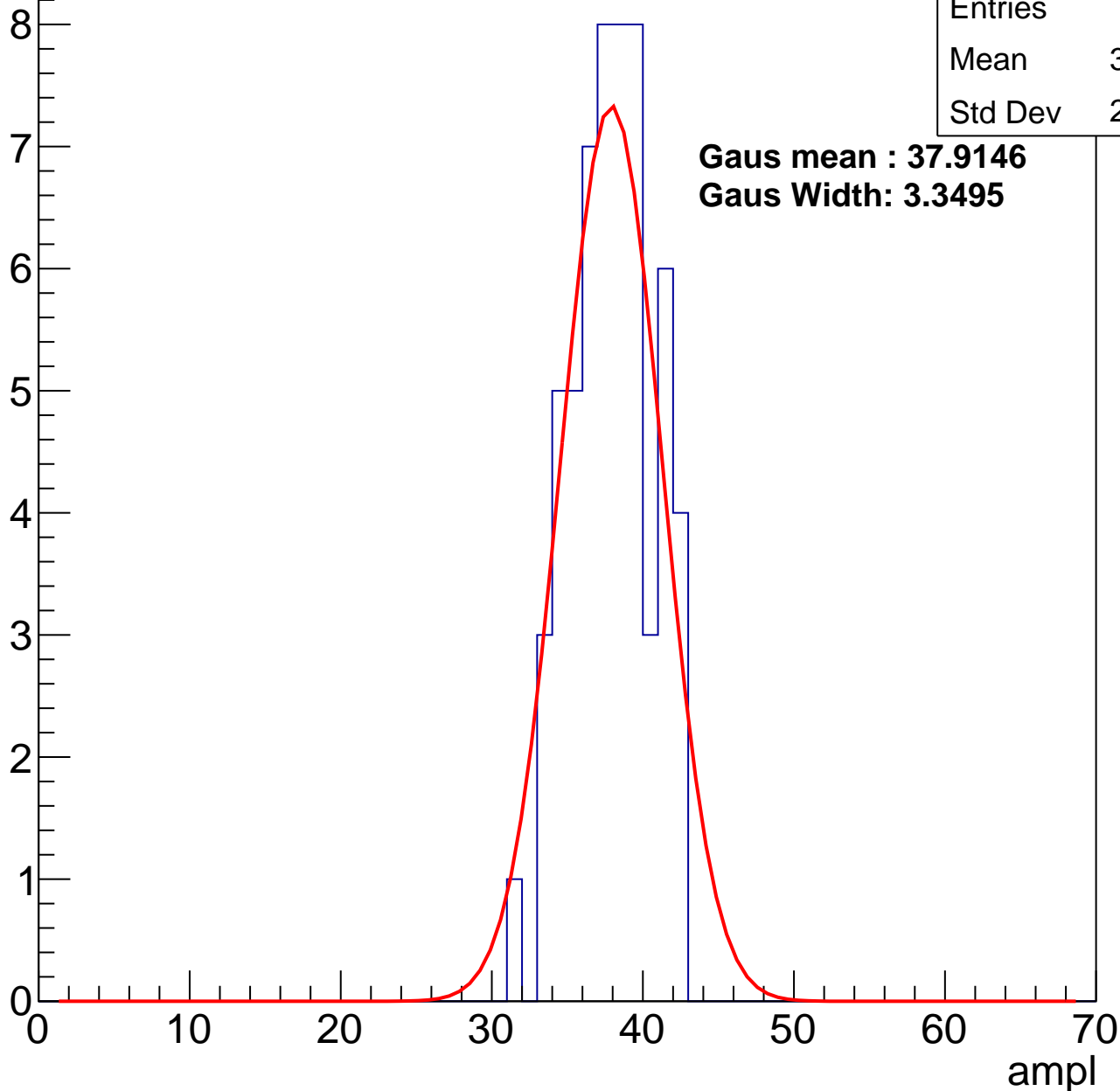
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	37.47
Std Dev	2.647

**Gaus mean : 37.9146**

**Gaus Width: 3.3495**



# B1L101S, U8-ch25, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	82
Mean	44.74
Std Dev	3.523

**Gaus mean : 45.6158**

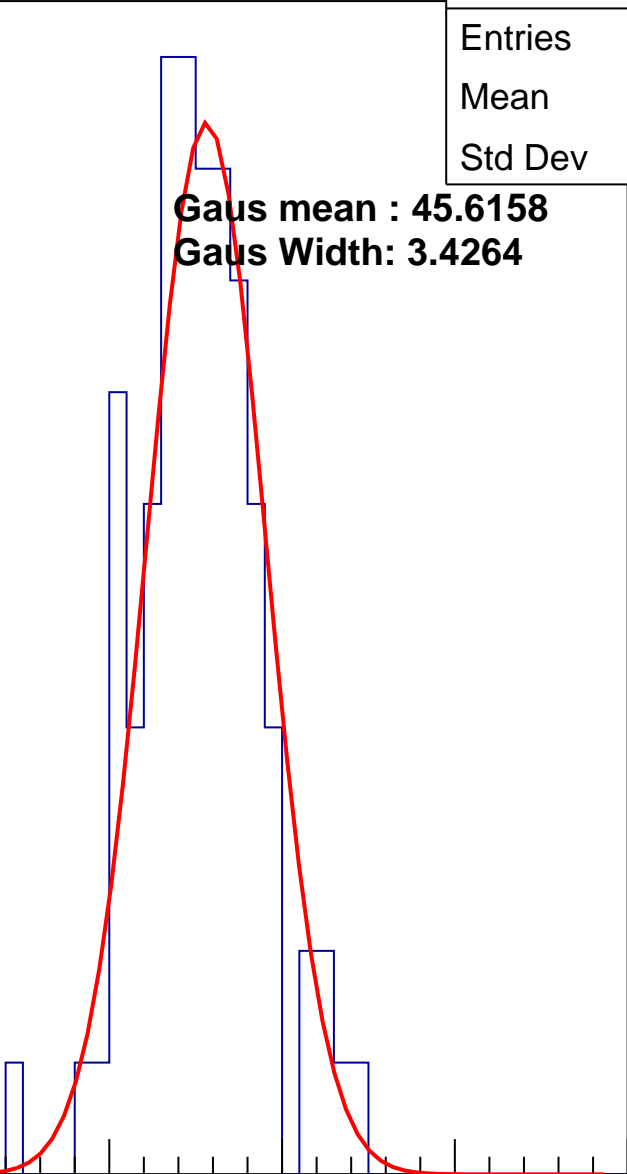
**Gaus Width: 3.4264**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

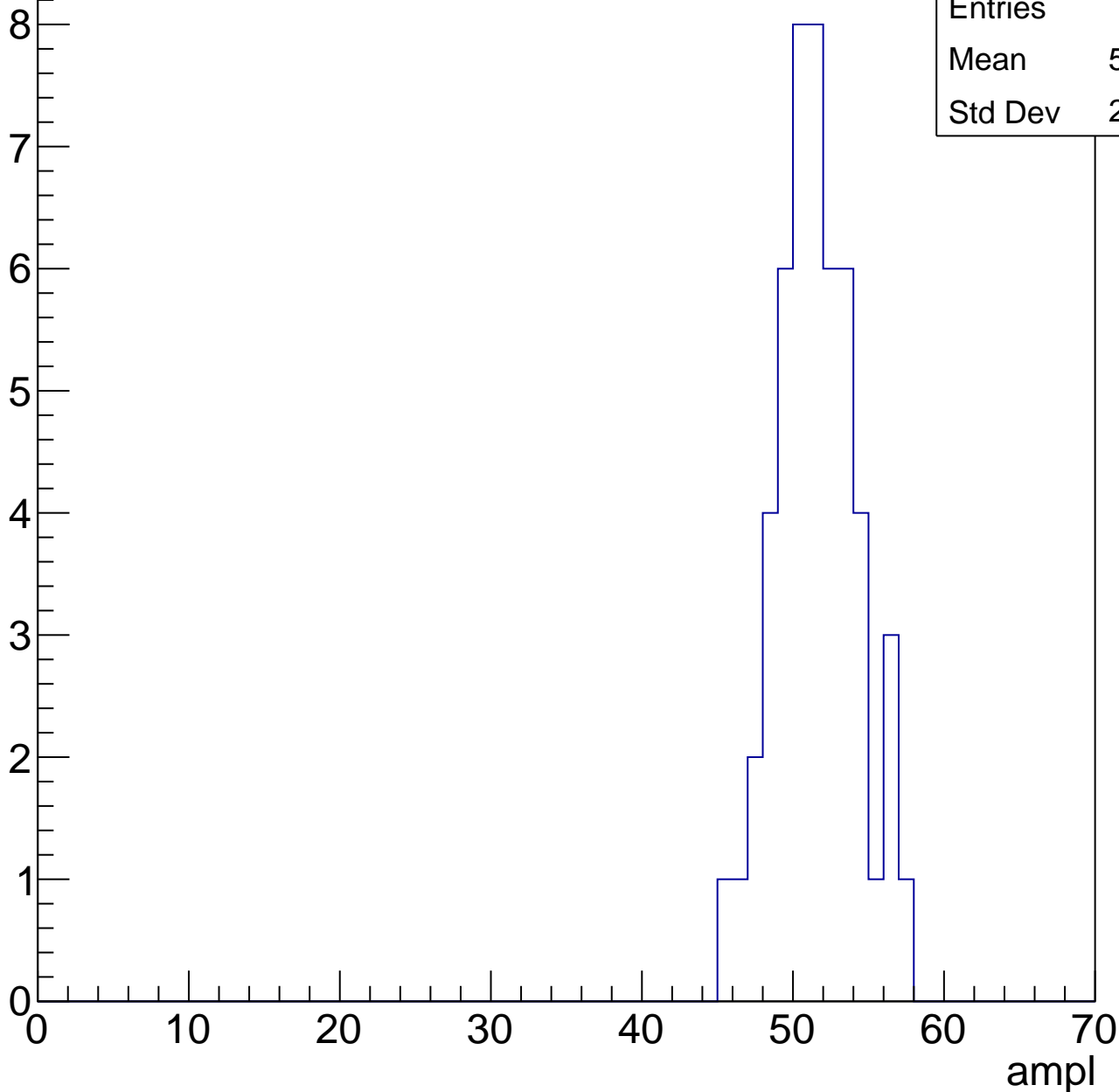


# B1L101S, U8-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	51.08
Std Dev	2.633

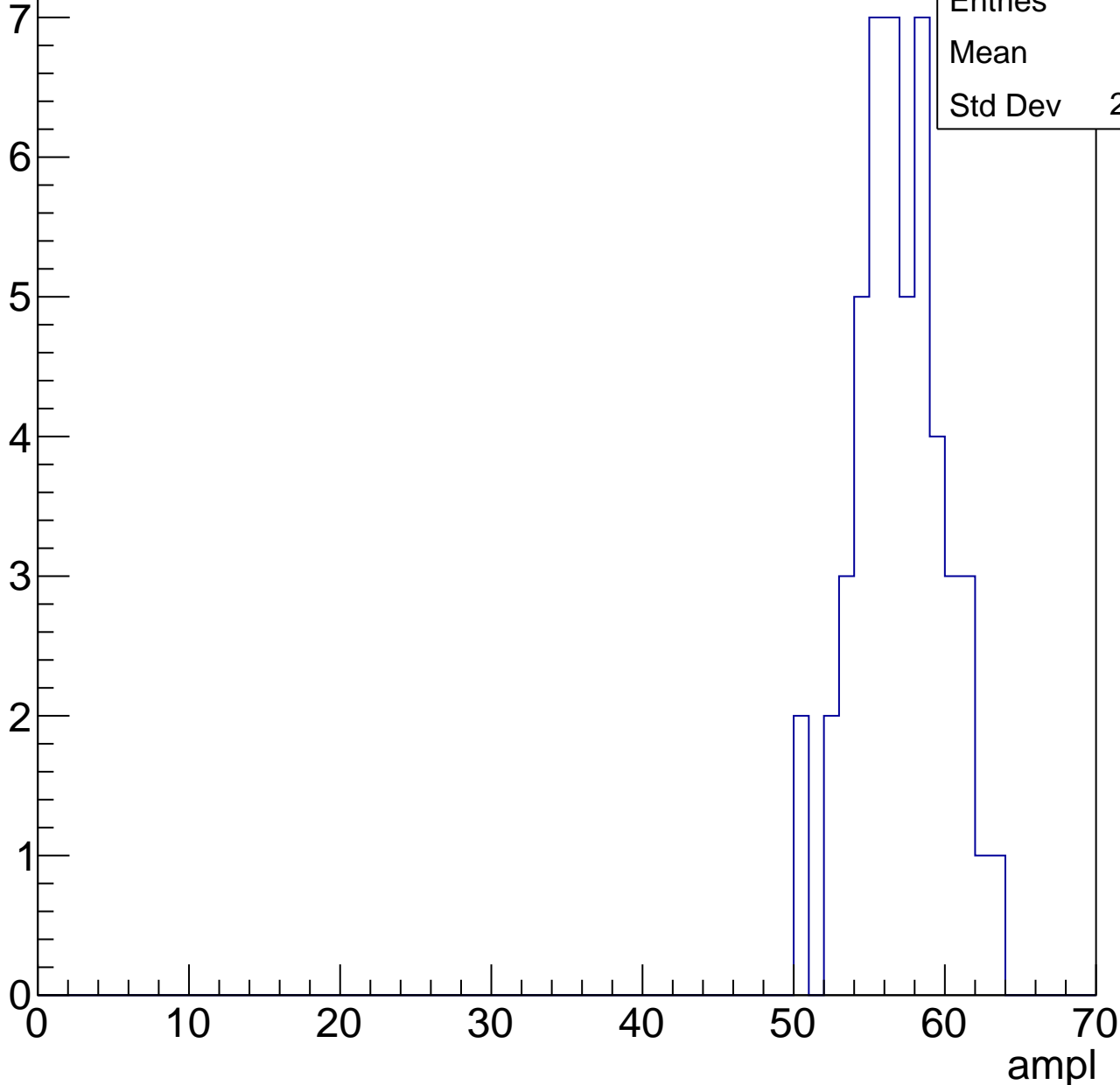


# B1L101S, U8-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	56.5
Std Dev	2.907

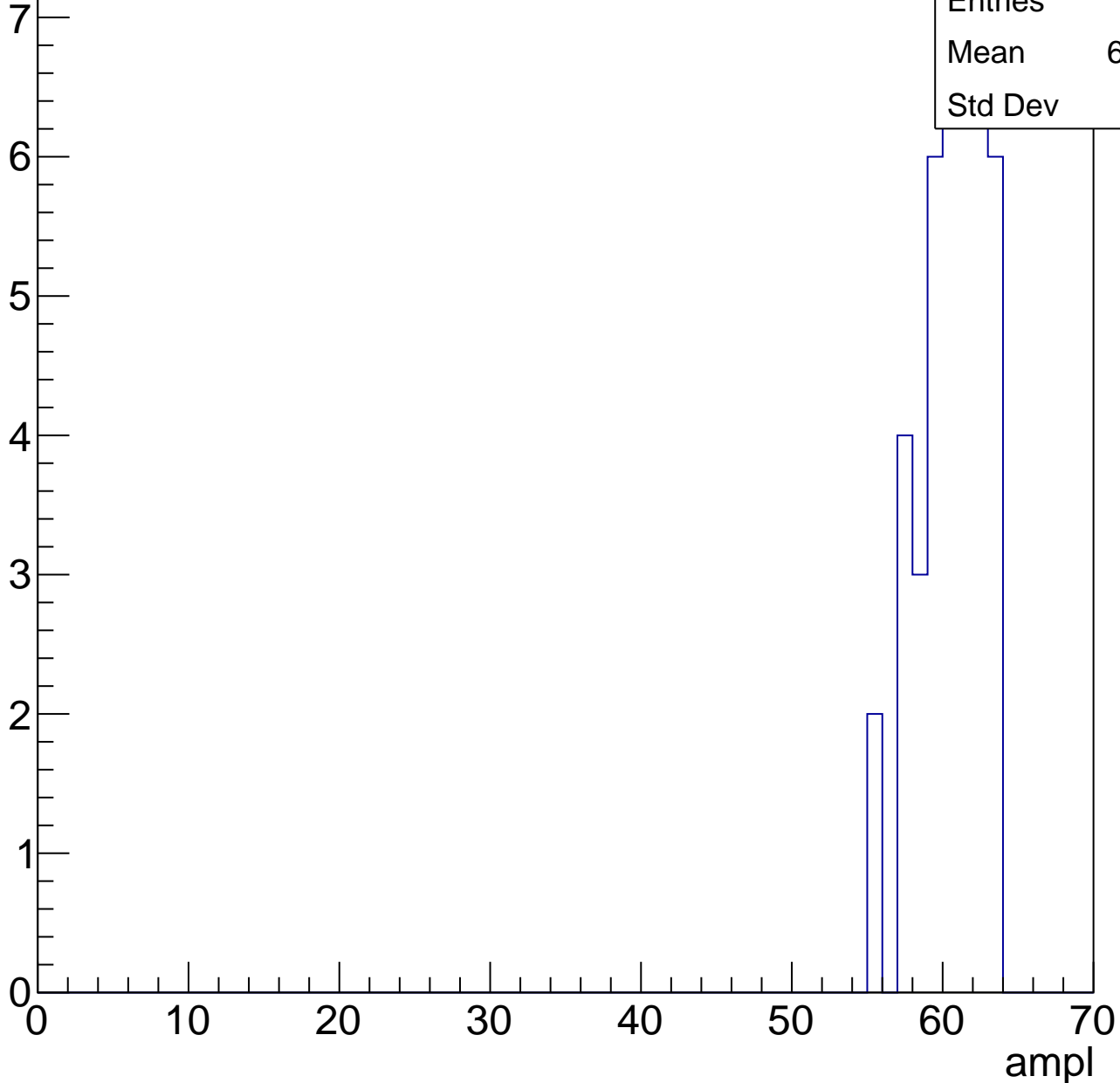


# B1L101S, U8-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

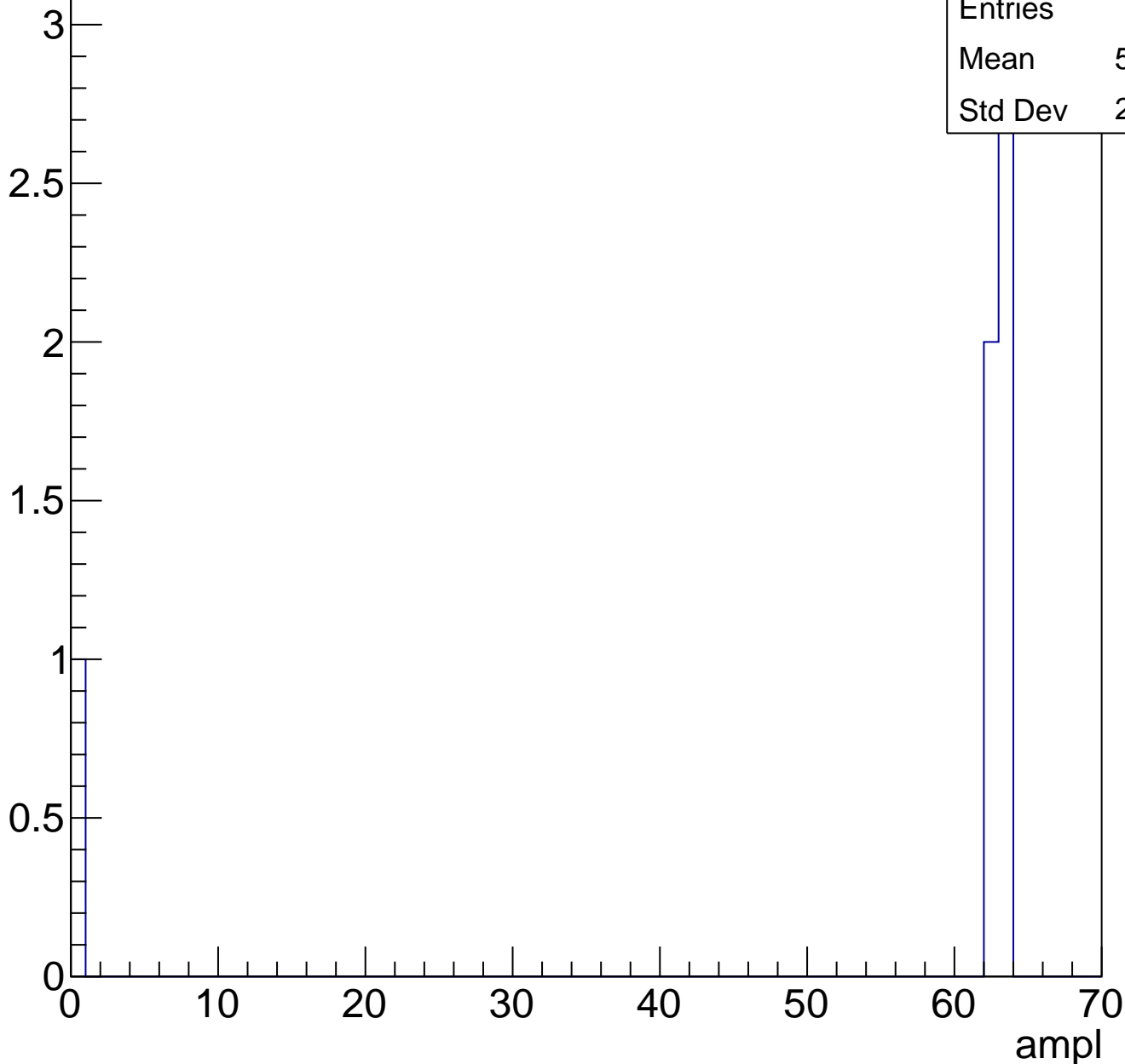
Entries	42
Mean	60.12
Std Dev	2.14



# B1L101S, U8-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U8-ch26, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	69
Mean	26.42
Std Dev	5.663

**Gaus mean : 27.4970**

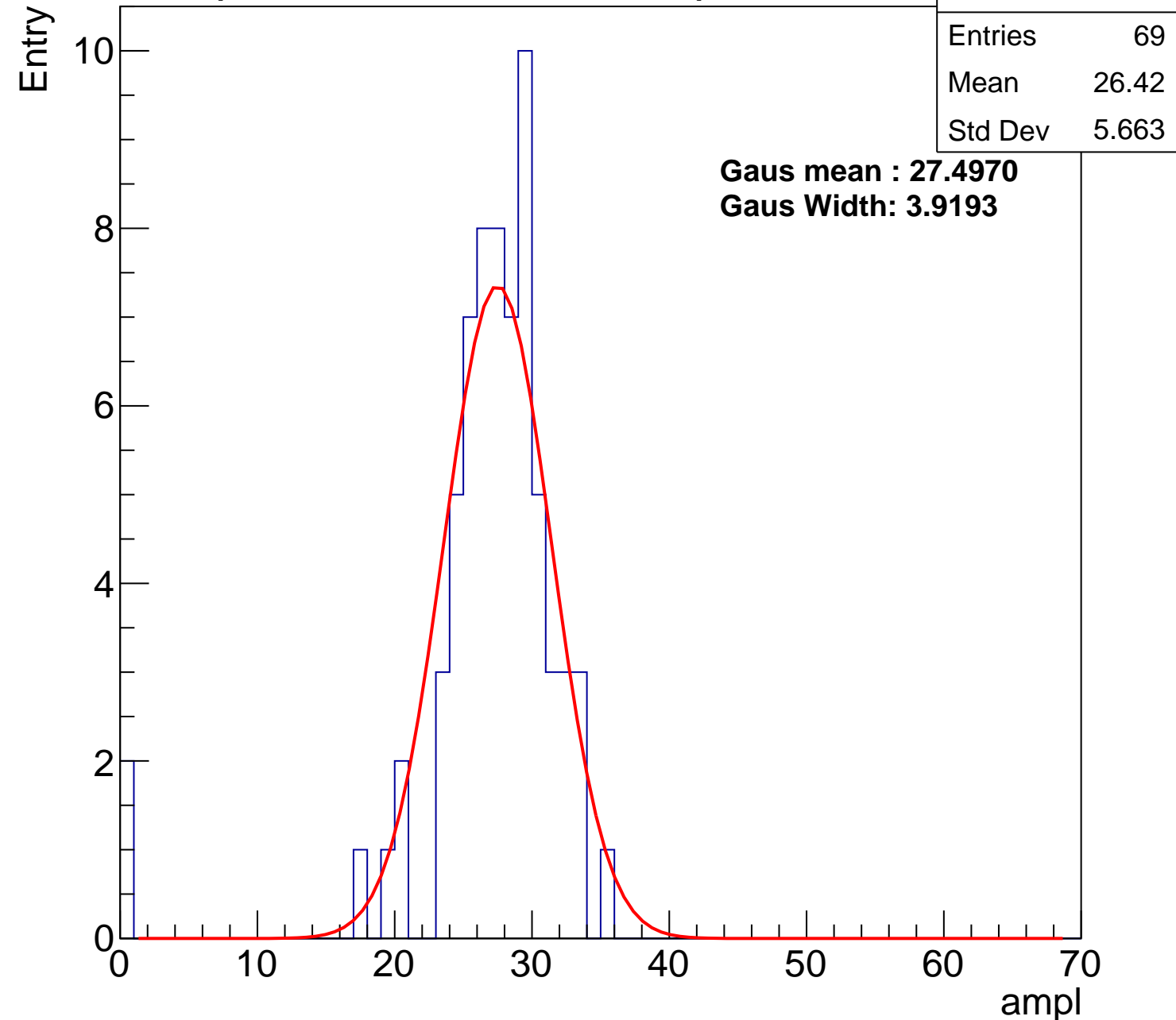
**Gaus Width: 3.9193**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U8-ch26, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	78
Mean	35.06
Std Dev	3.746

**Gaus mean : 34.6338**

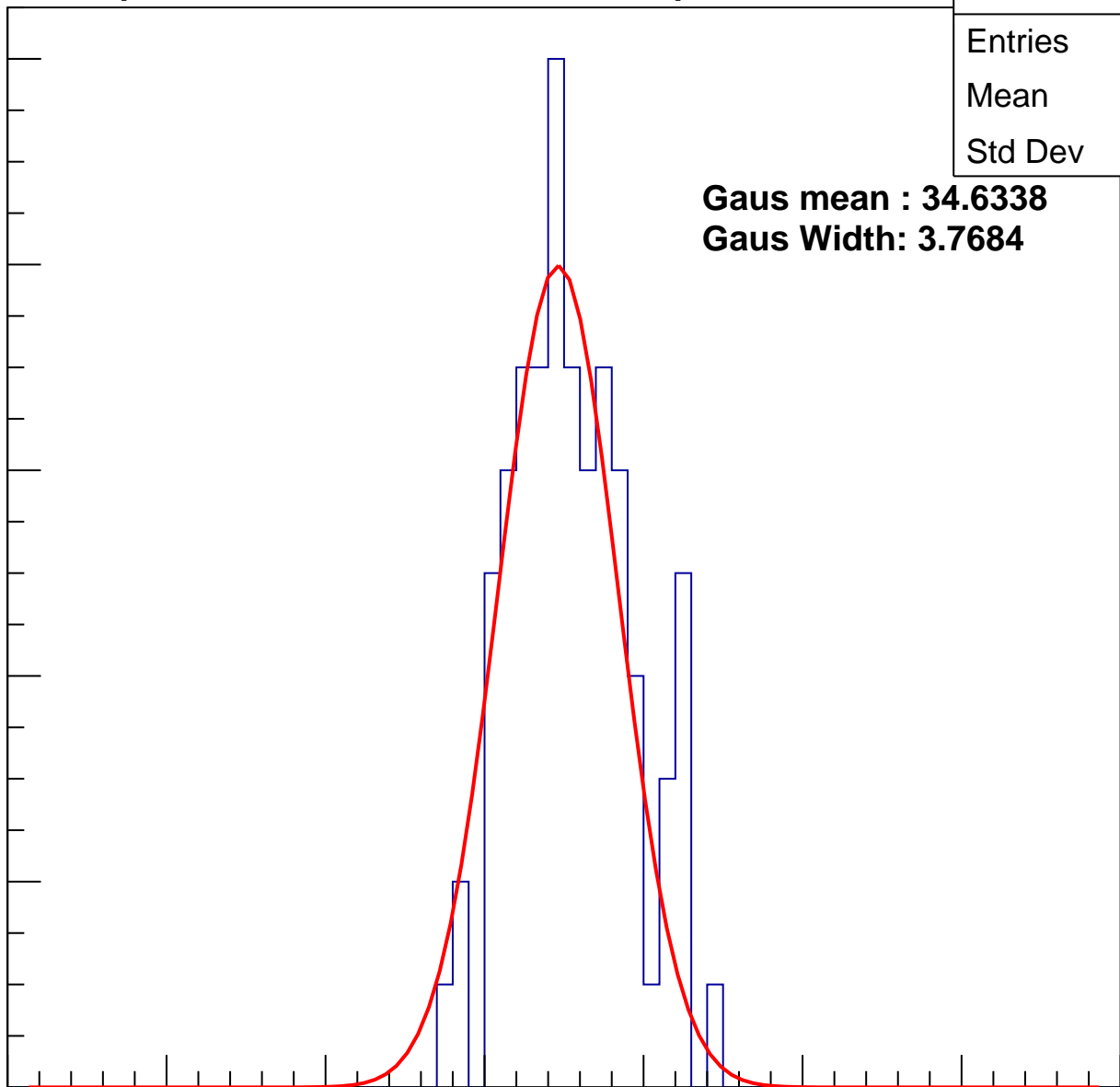
**Gaus Width: 3.7684**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U8-ch26, adc2

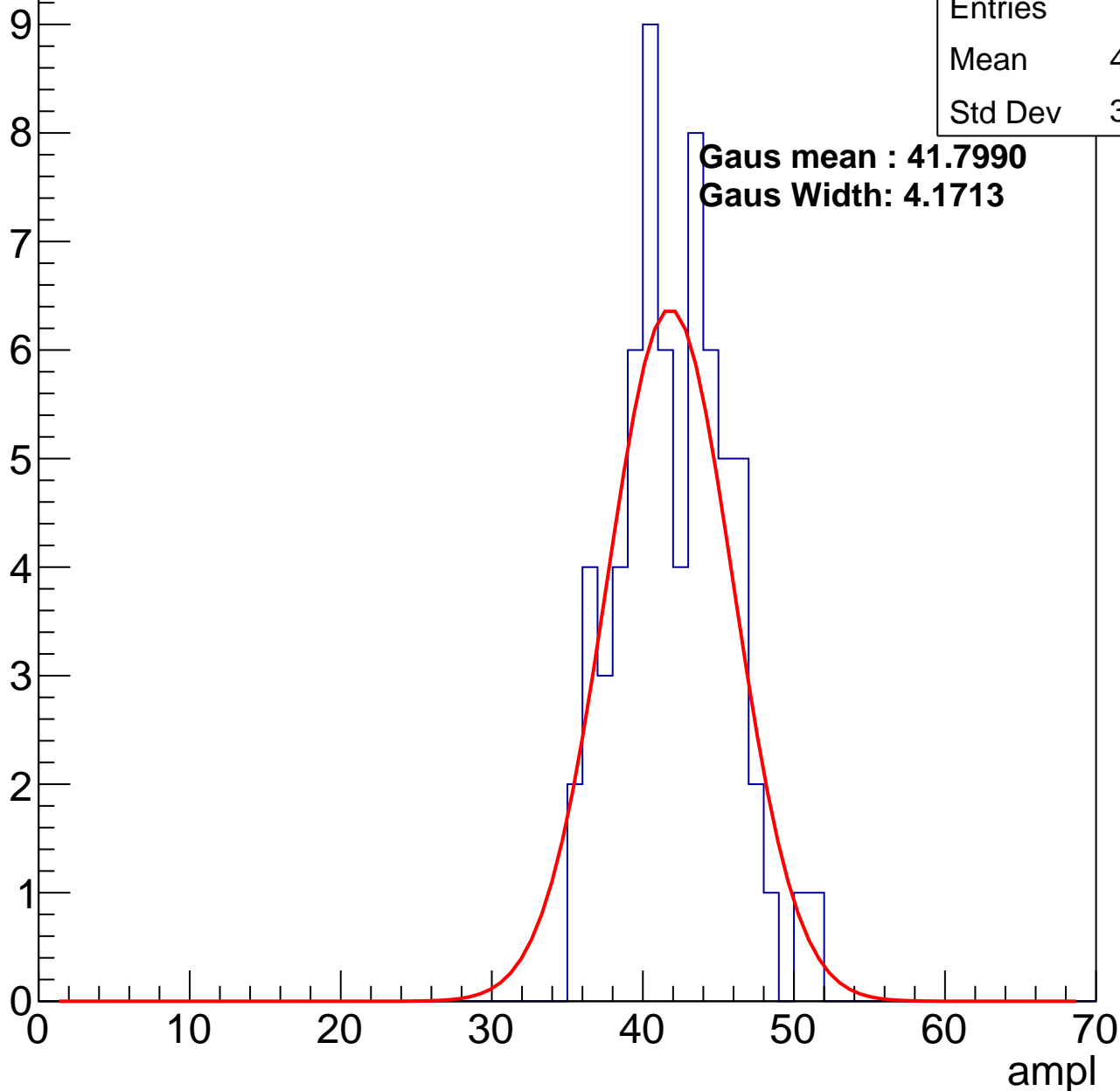
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	41.66
Std Dev	3.577

**Gaus mean : 41.7990**

**Gaus Width: 4.1713**



# B1L101S, U8-ch26, adc3

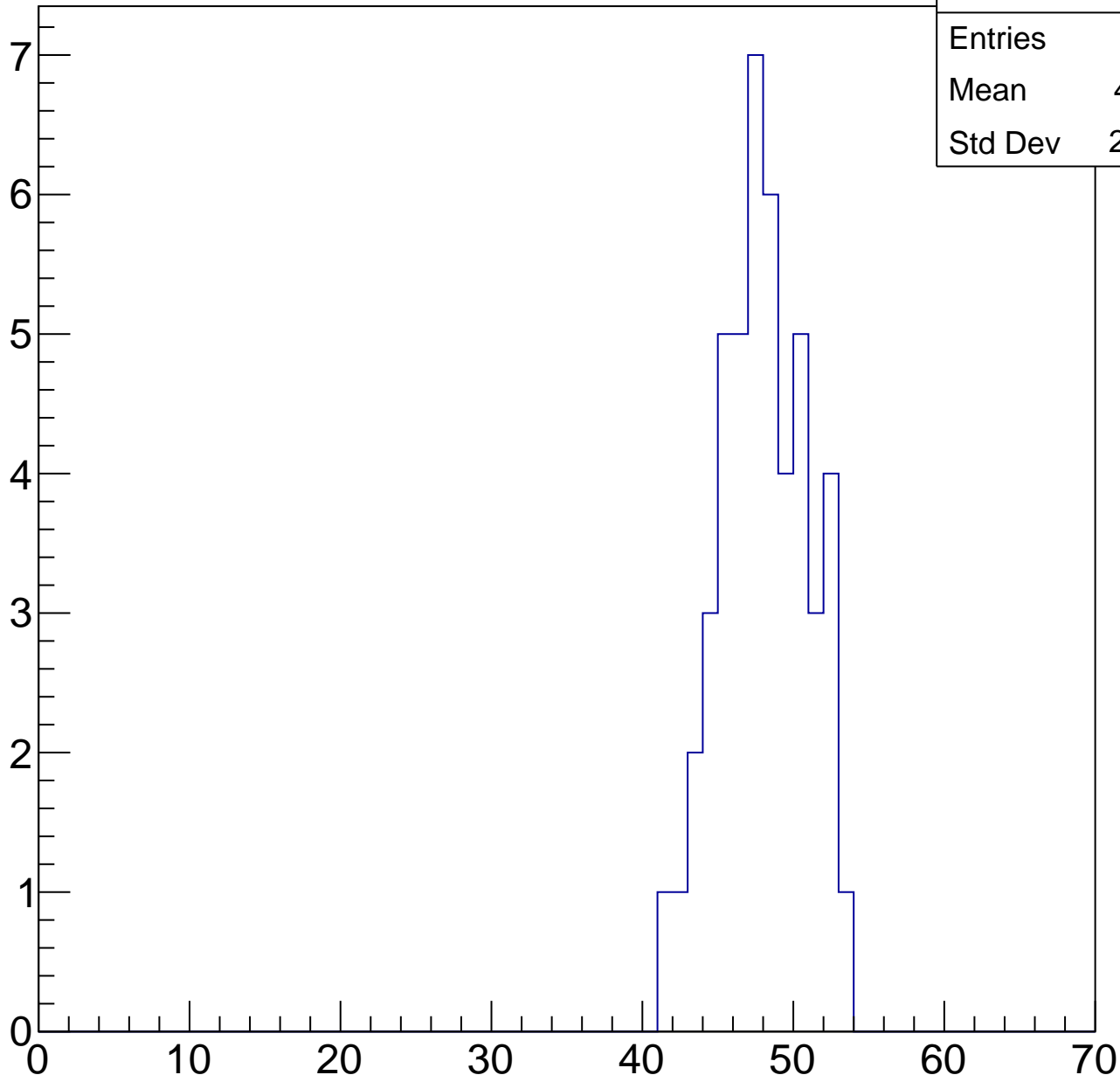
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	47
Mean	47.51
Std Dev	2.857

ampl



# B1L101S, U8-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

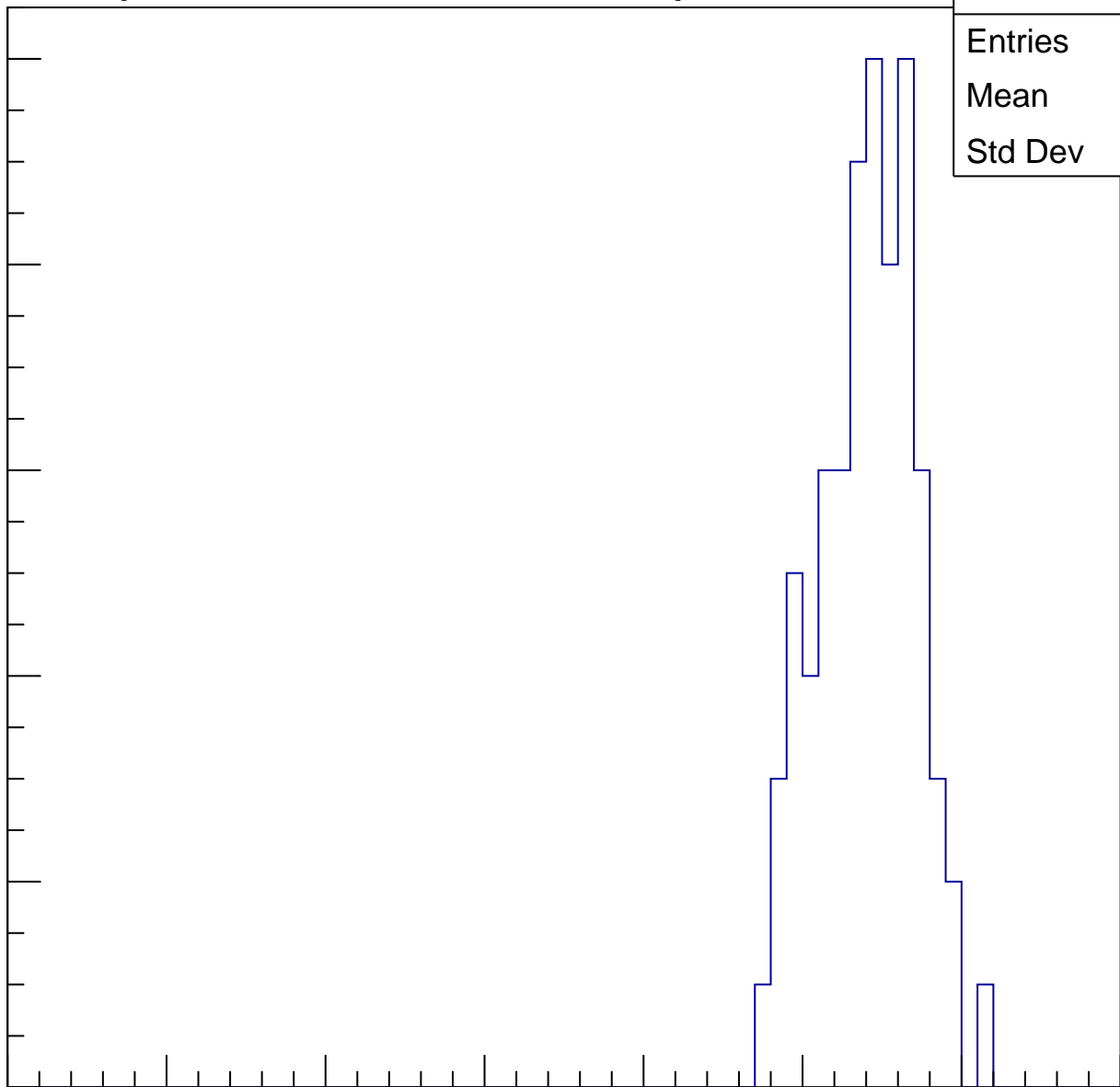
Entries	74
Mean	53.59
Std Dev	3.009

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U8-ch26, adc5

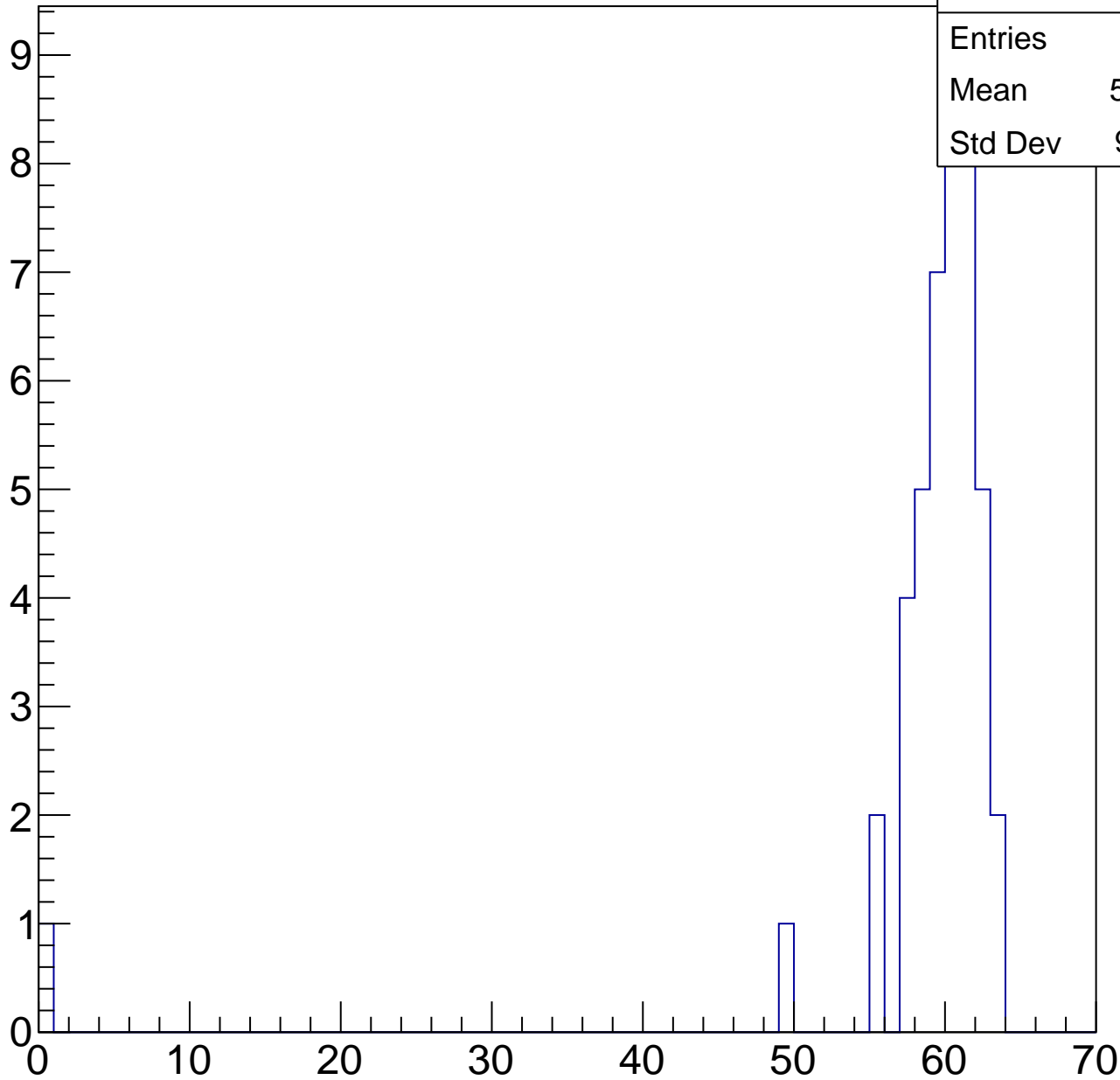
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	44
Mean	58.07
Std Dev	9.191

ampl

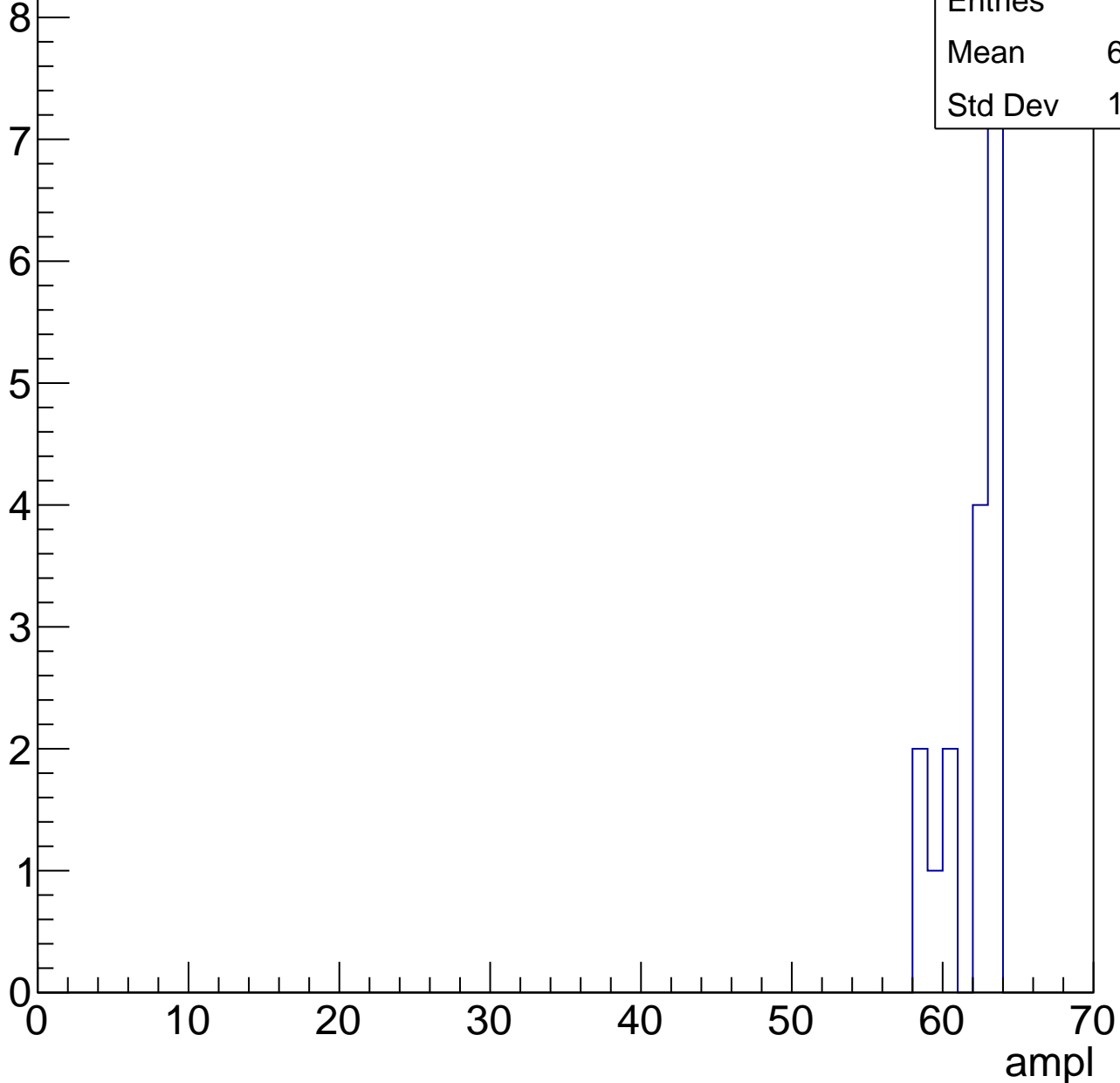


# B1L101S, U8-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	17
Mean	61.59
Std Dev	1.784





# B1L101S, U8-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch27, adc0

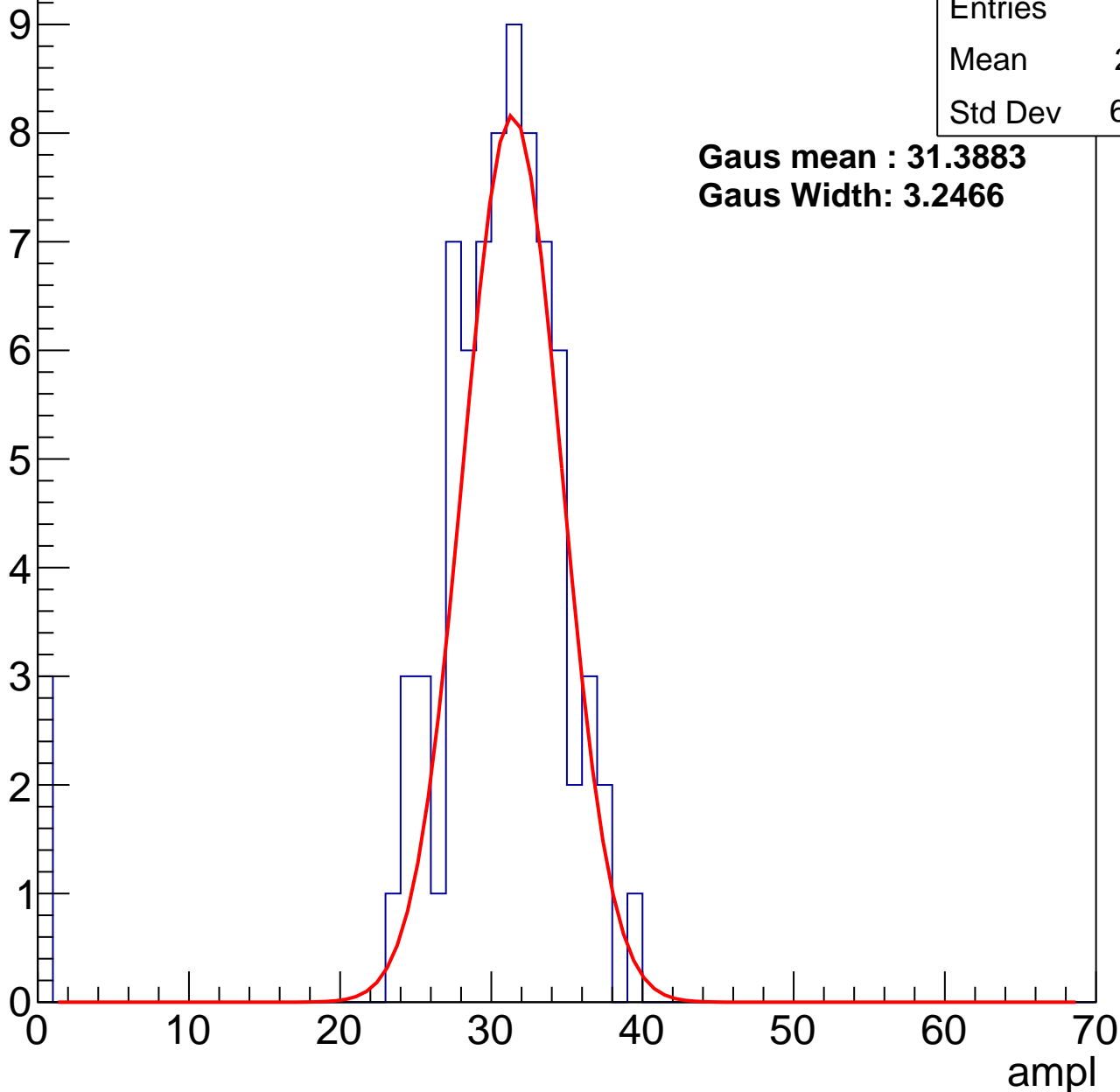
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	29.31
Std Dev	6.783

**Gaus mean : 31.3883**

**Gaus Width: 3.2466**



# B1L101S, U8-ch27, adc1

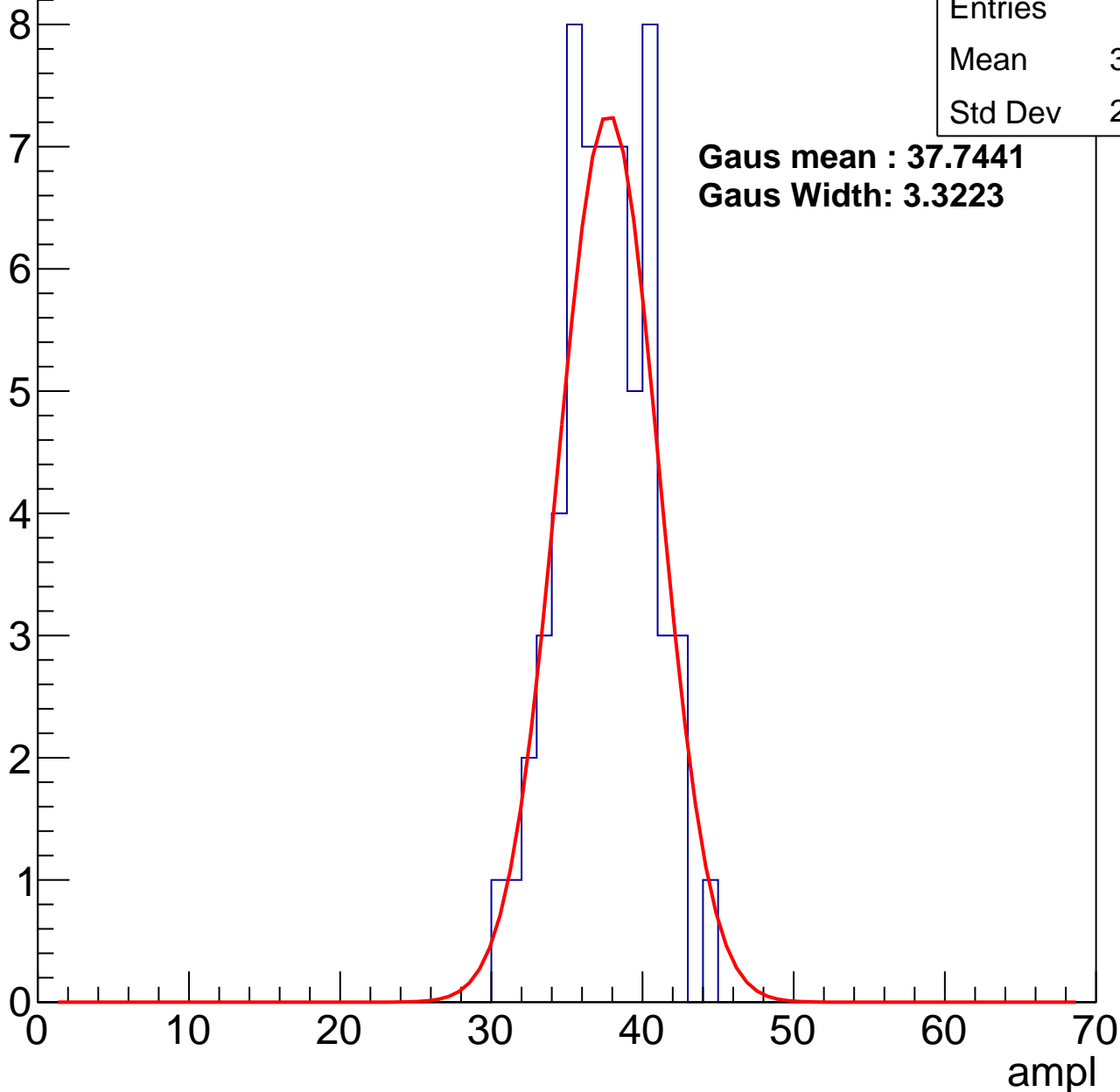
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	37.08
Std Dev	2.968

**Gaus mean : 37.7441**

**Gaus Width: 3.3223**



# B1L101S, U8-ch27, adc2

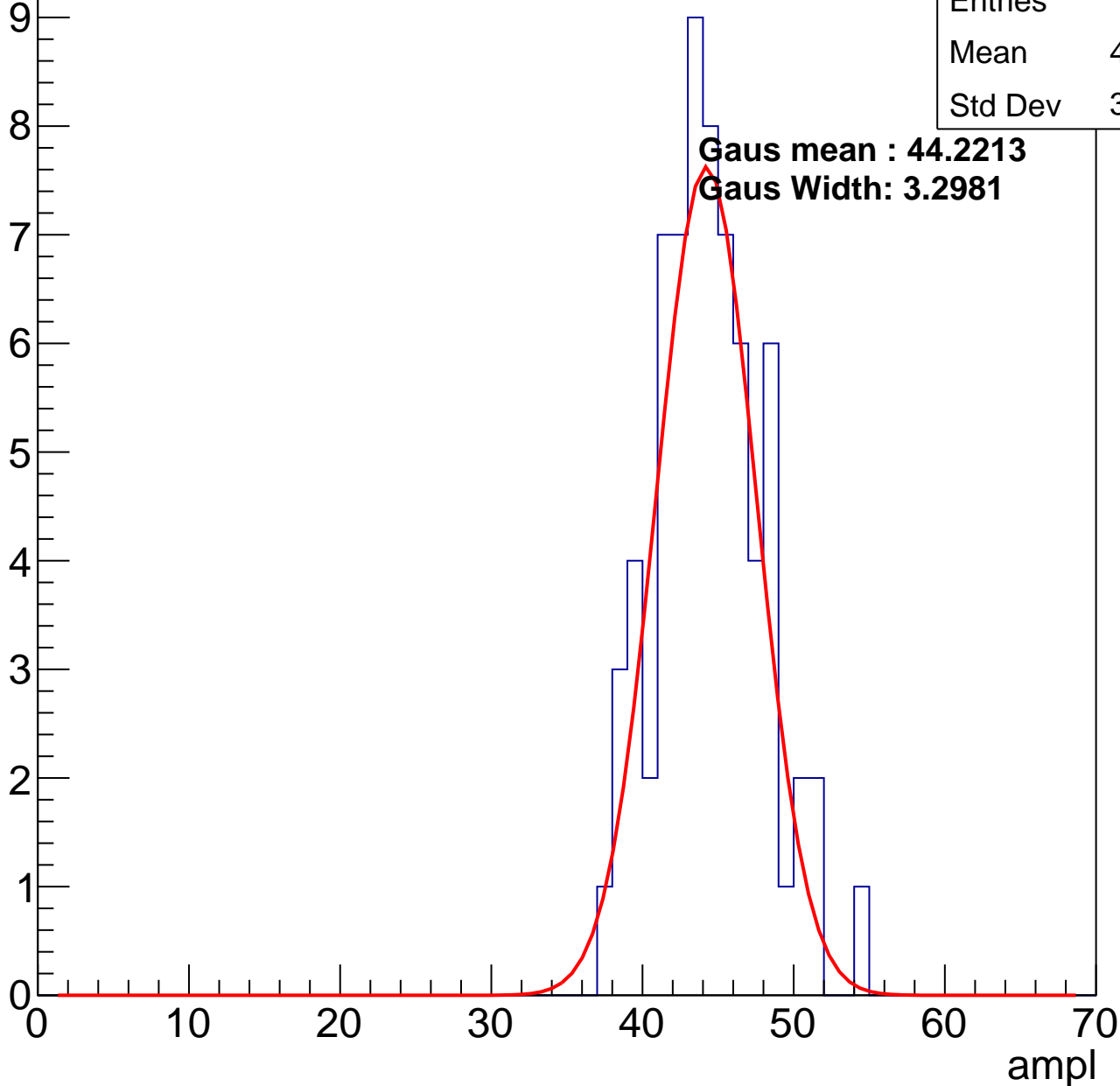
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	43.99
Std Dev	3.478

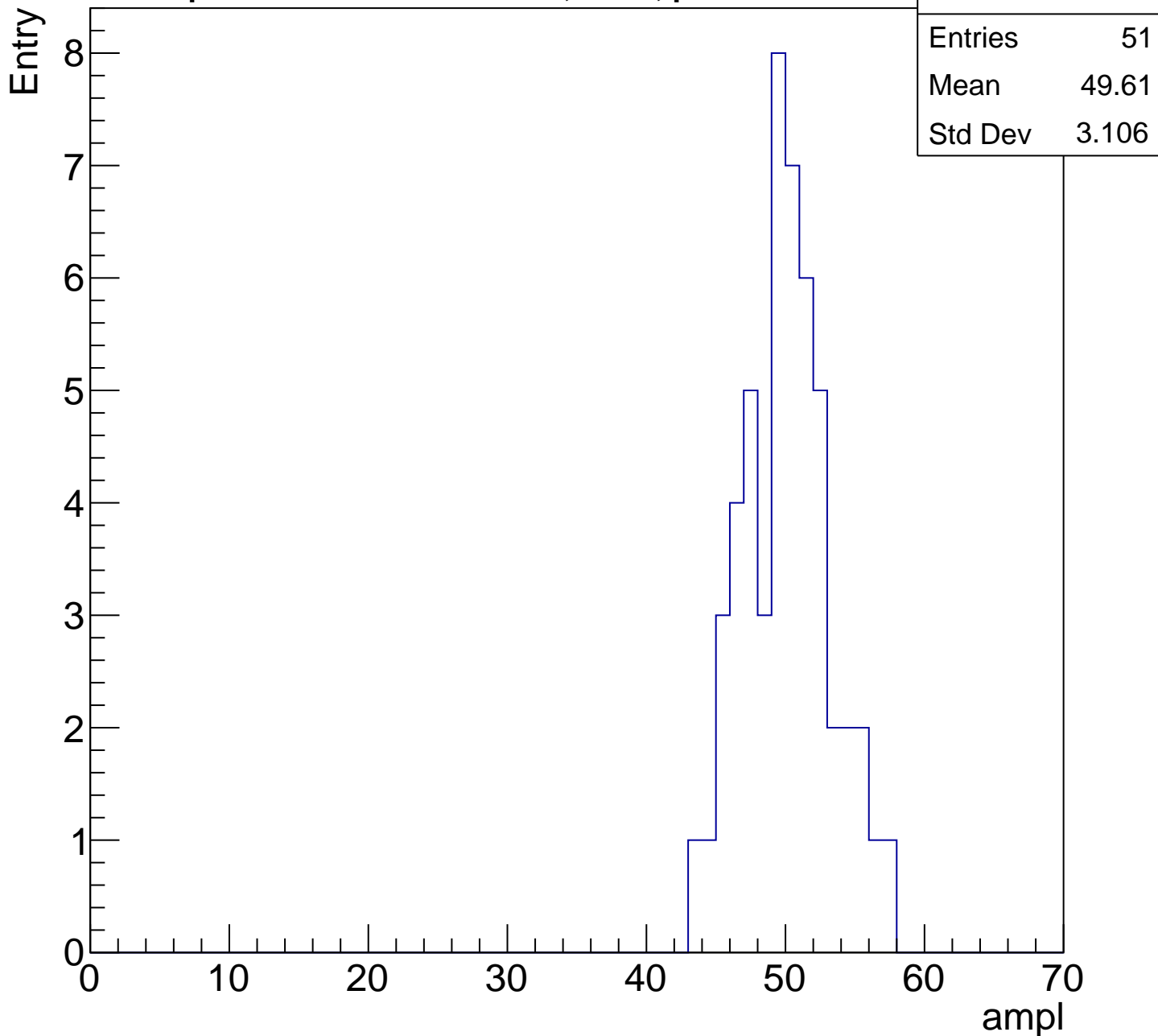
**Gaus mean : 44.2213**

**Gaus Width: 3.2981**



# B1L101S, U8-ch27, adc3

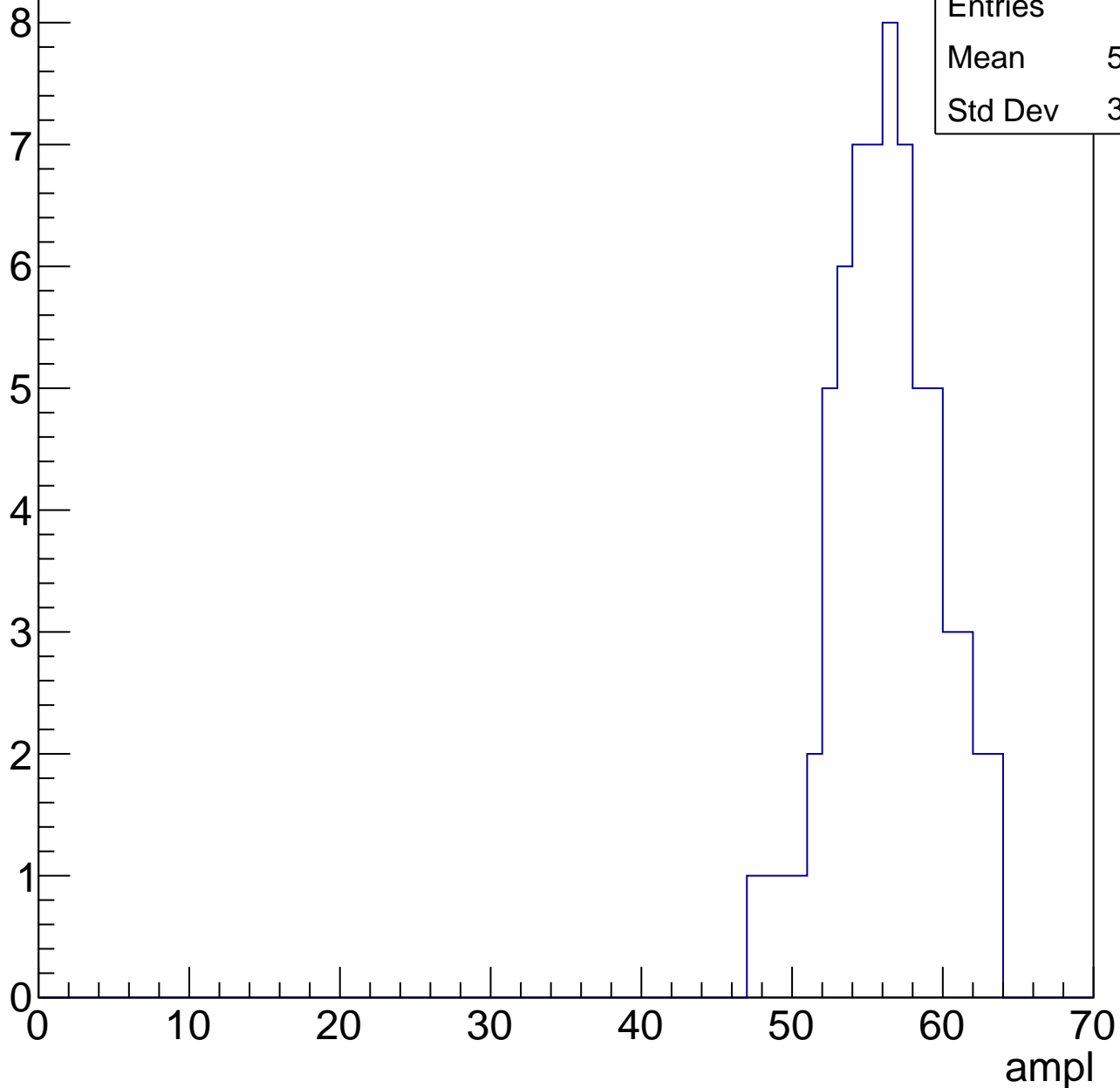
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U8-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

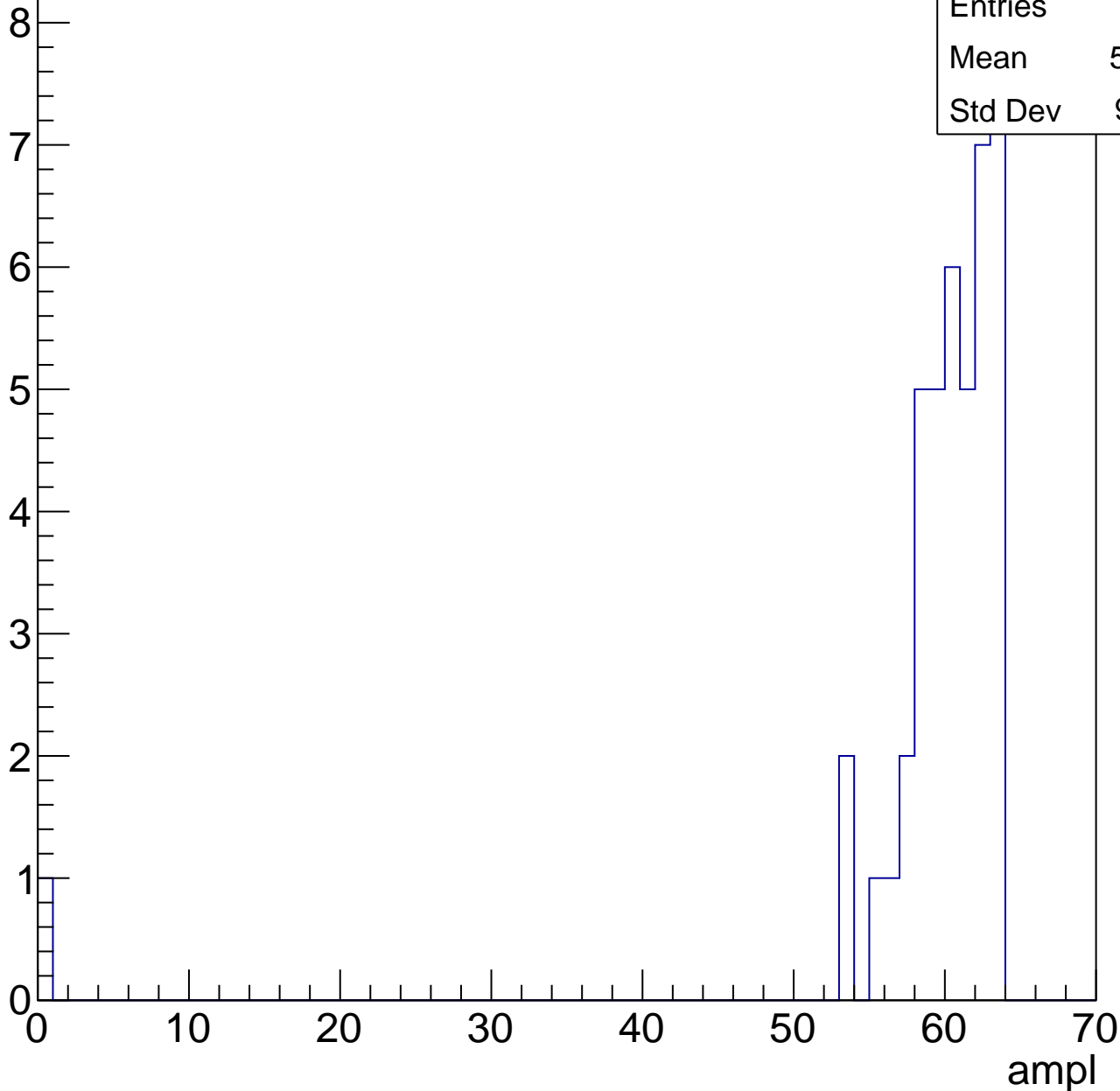


# B1L101S, U8-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

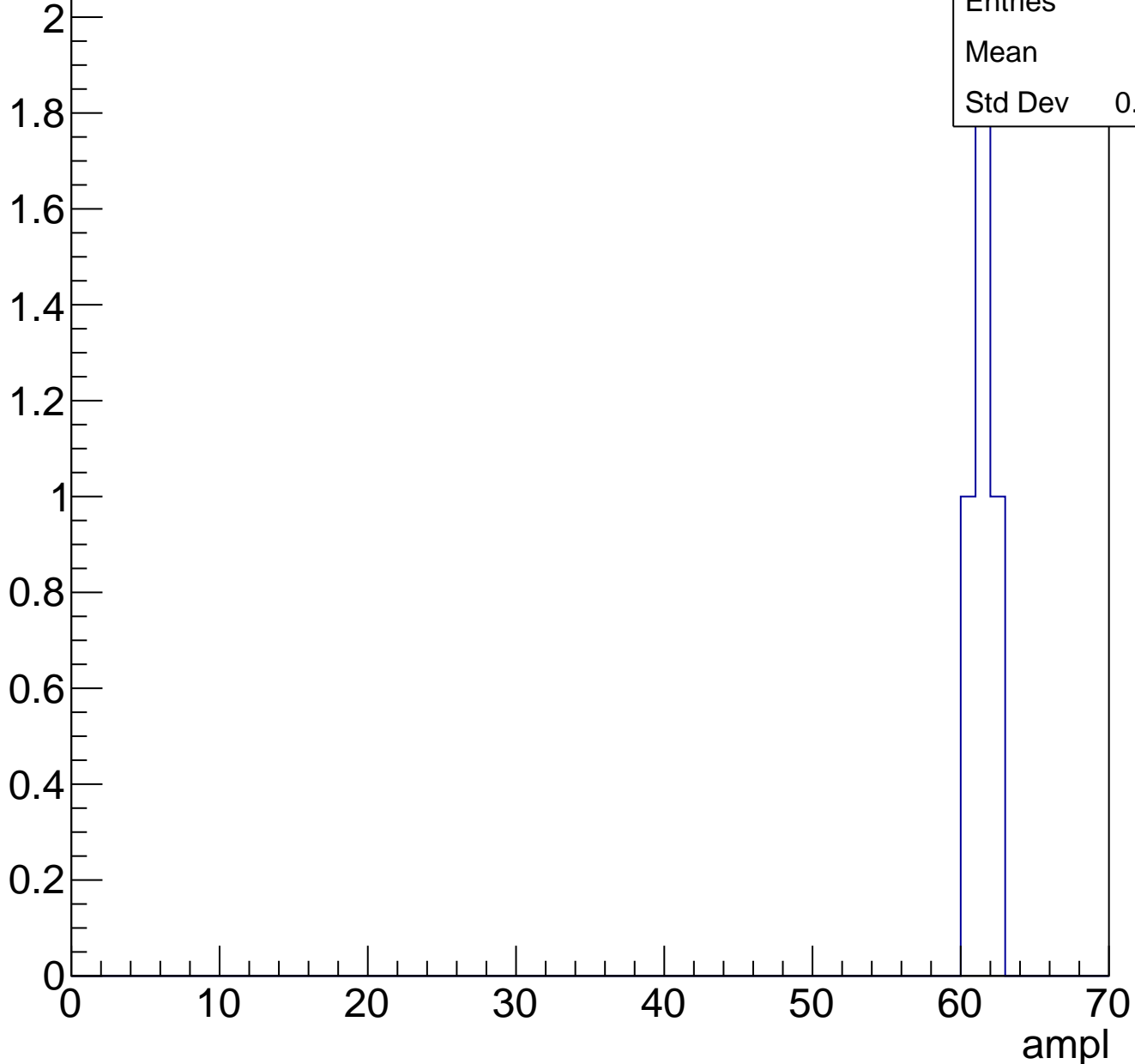
Entries	43
Mean	58.58
Std Dev	9.401



# B1L101S, U8-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	4
Mean	61
Std Dev	0.7071



# B1L101S, U8-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch28, adc0

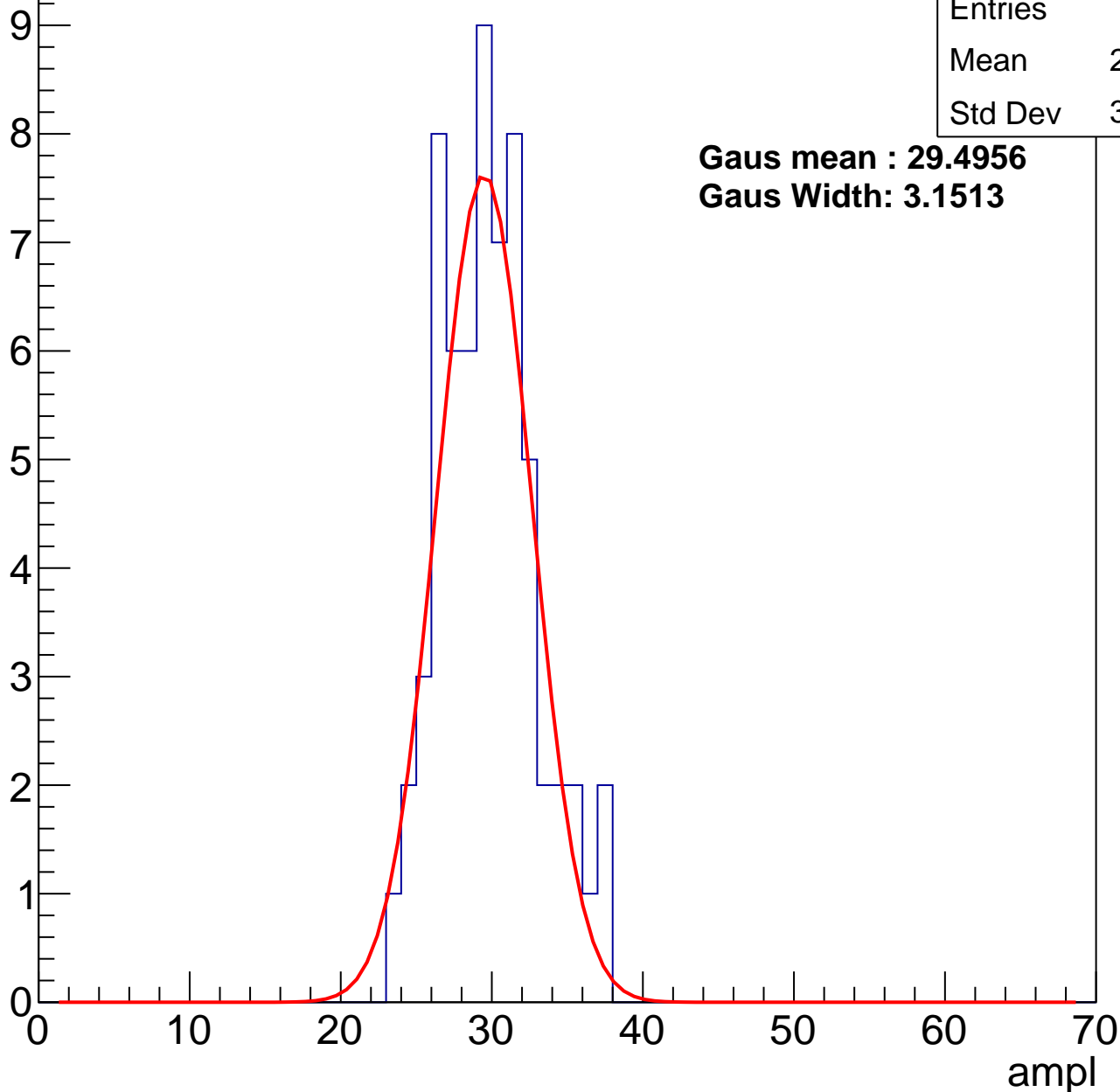
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	29.33
Std Dev	3.172

**Gaus mean : 29.4956**

**Gaus Width: 3.1513**



# B1L101S, U8-ch28, adc1

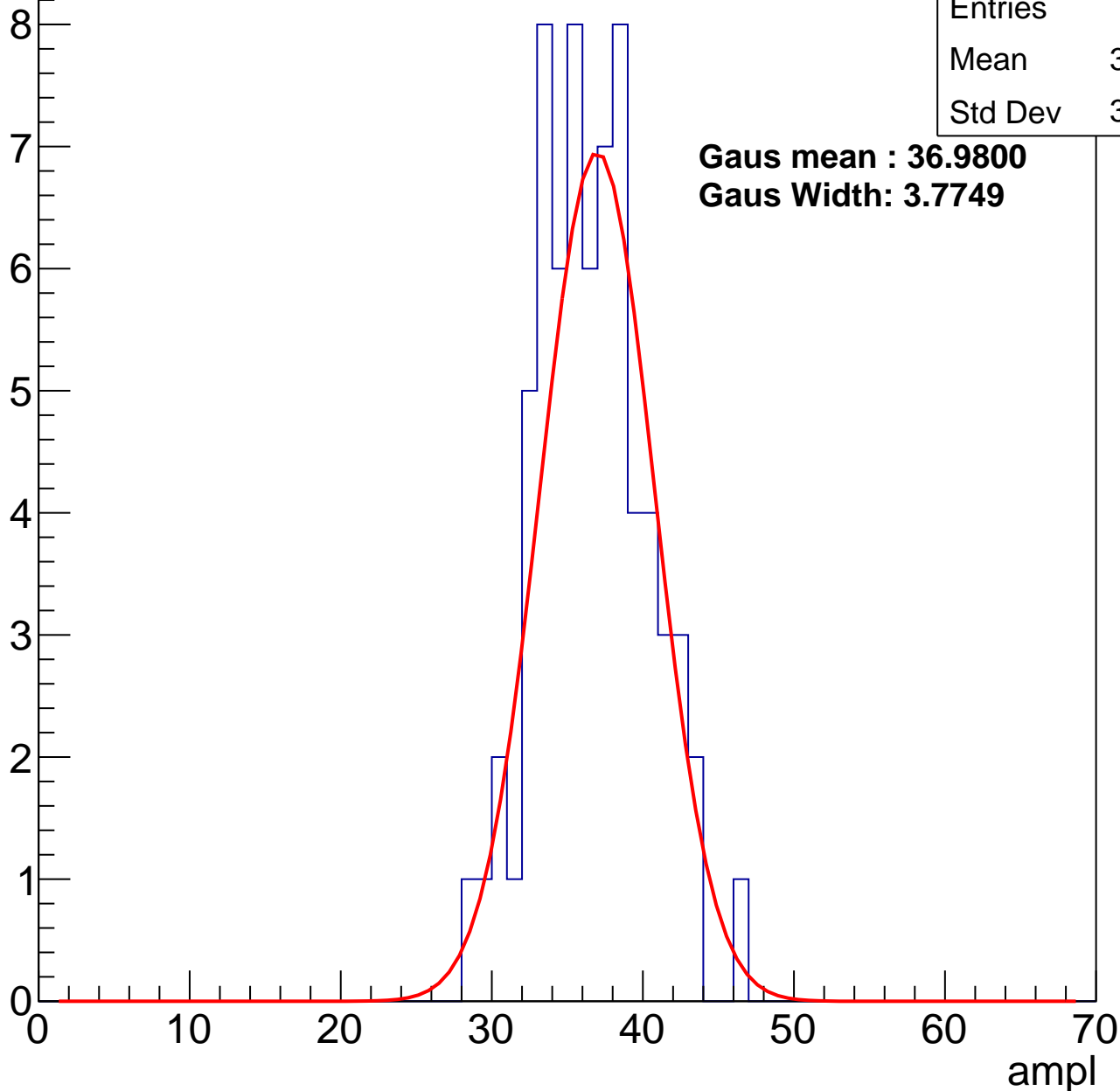
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	36.17
Std Dev	3.609

**Gaus mean : 36.9800**

**Gaus Width: 3.7749**

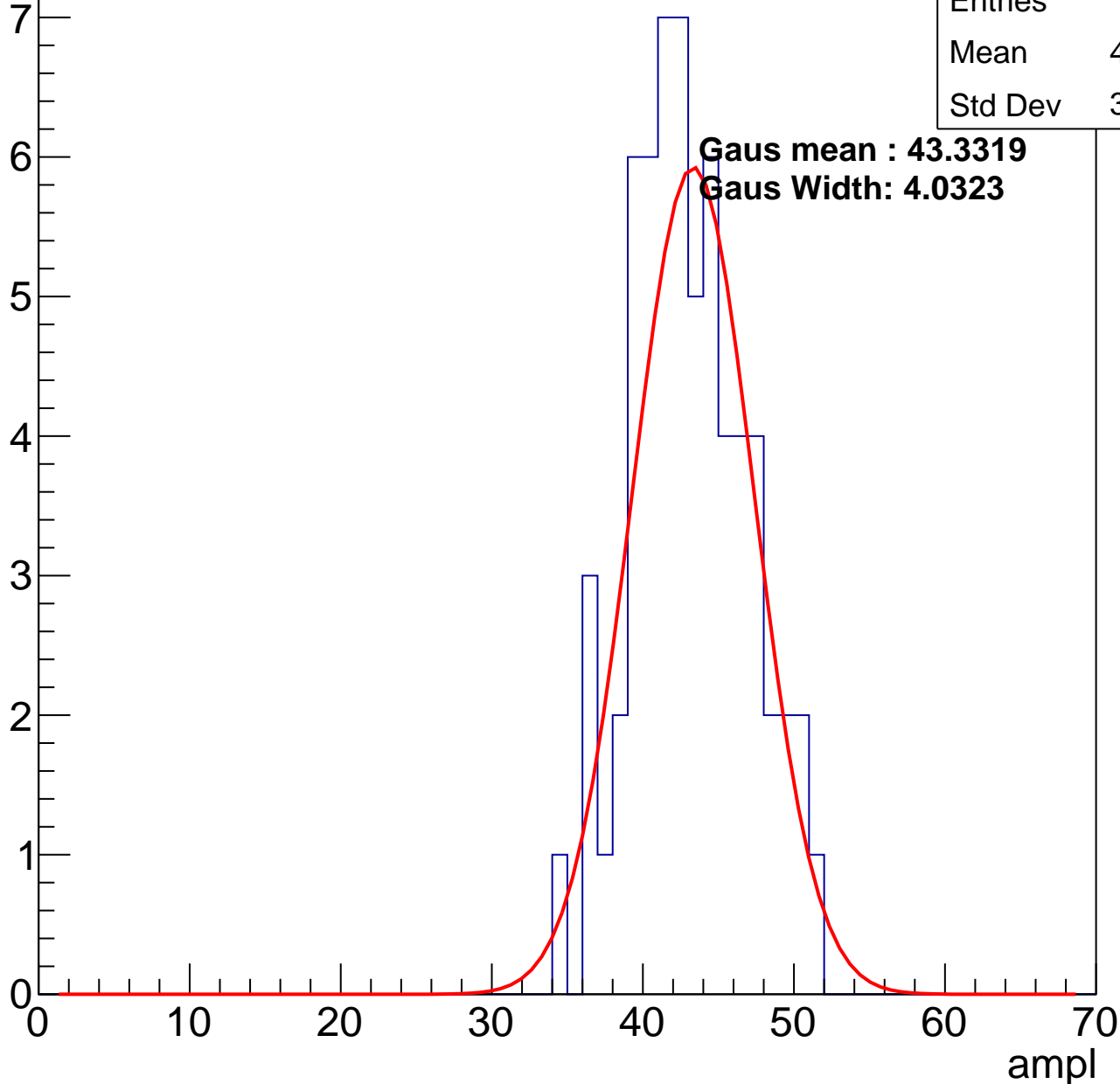


# B1L101S, U8-ch28, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

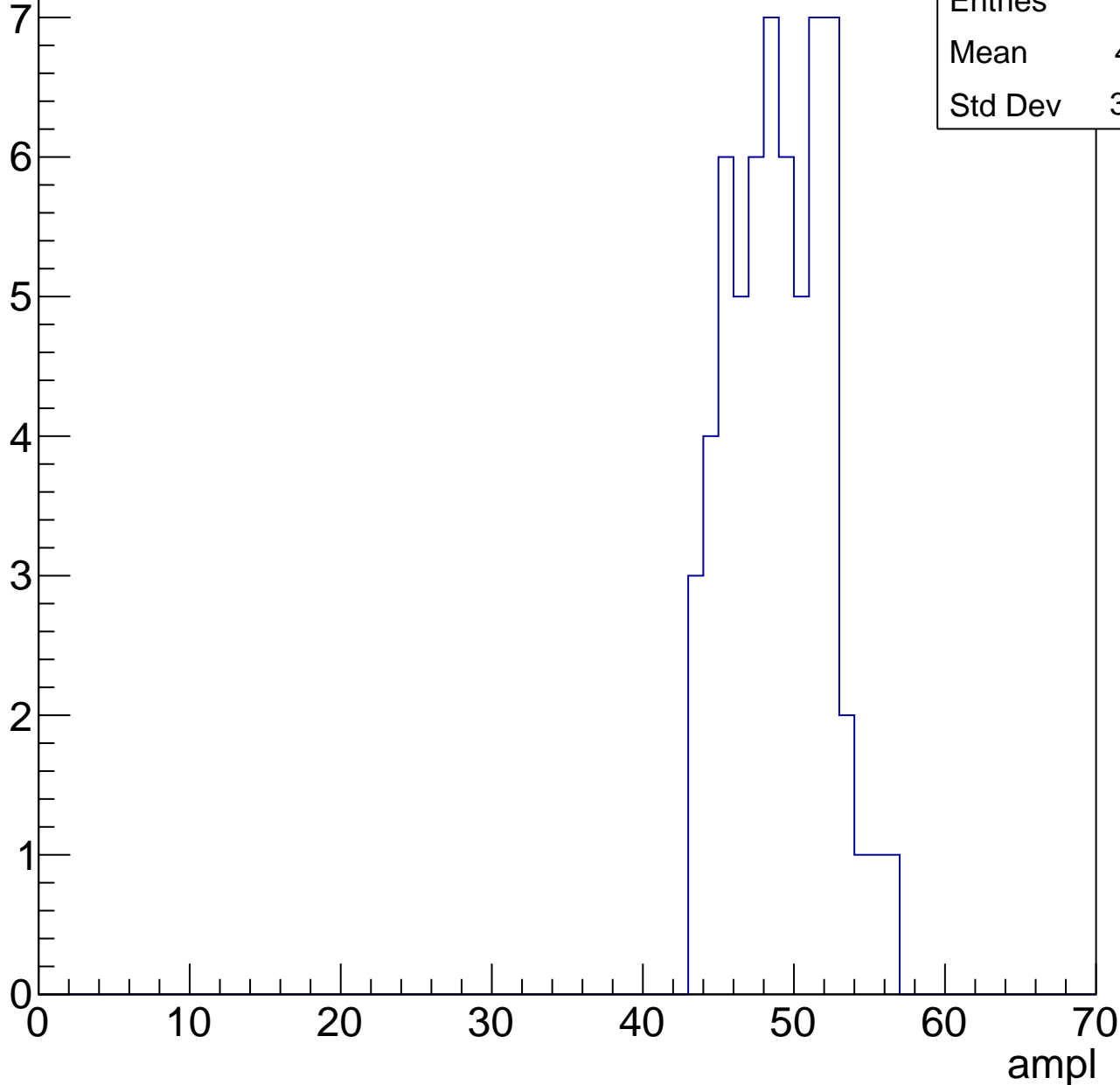
Entries	63
Mean	42.63
Std Dev	3.773



# B1L101S, U8-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

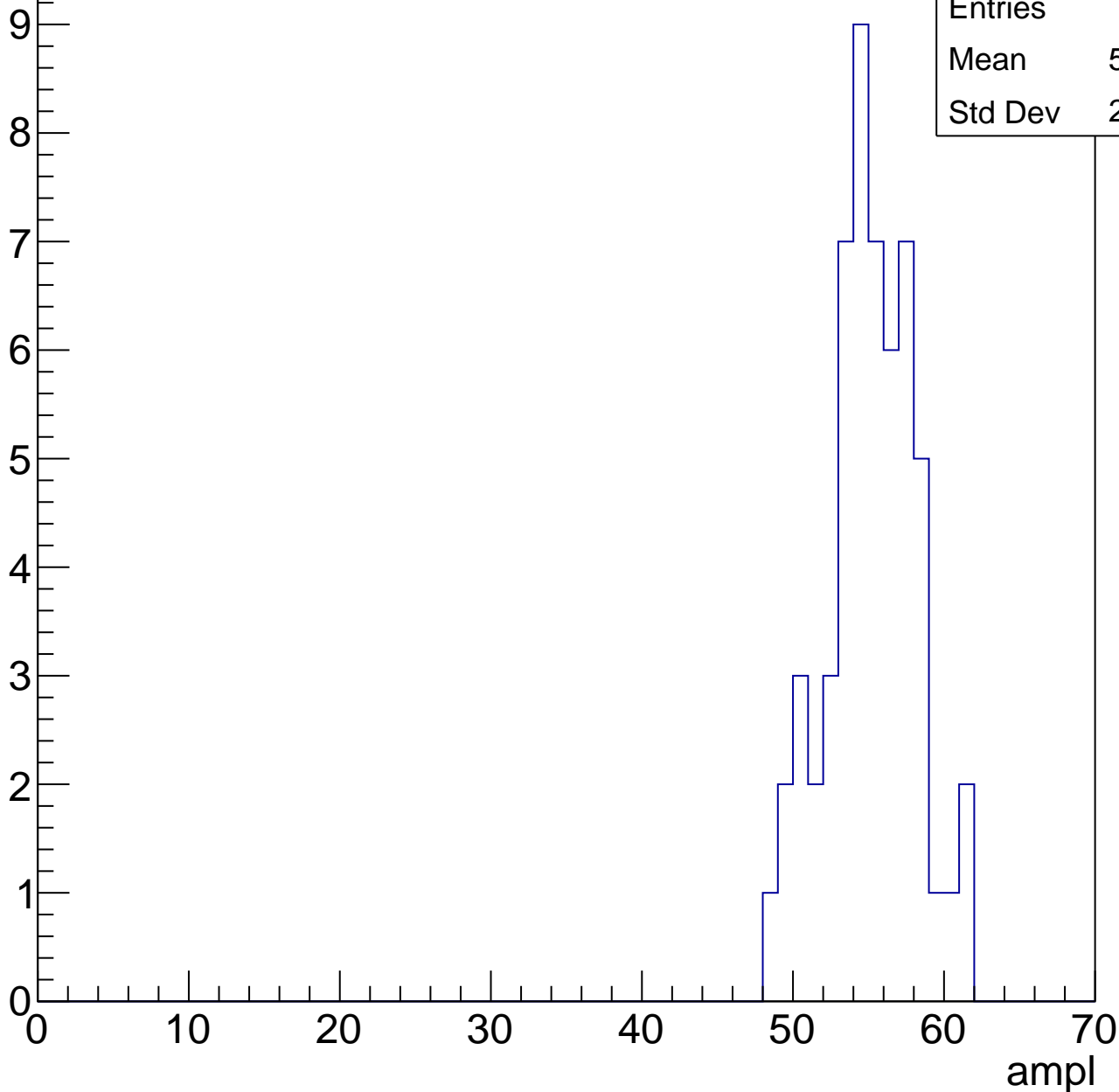


# B1L101S, U8-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	54.68
Std Dev	2.922

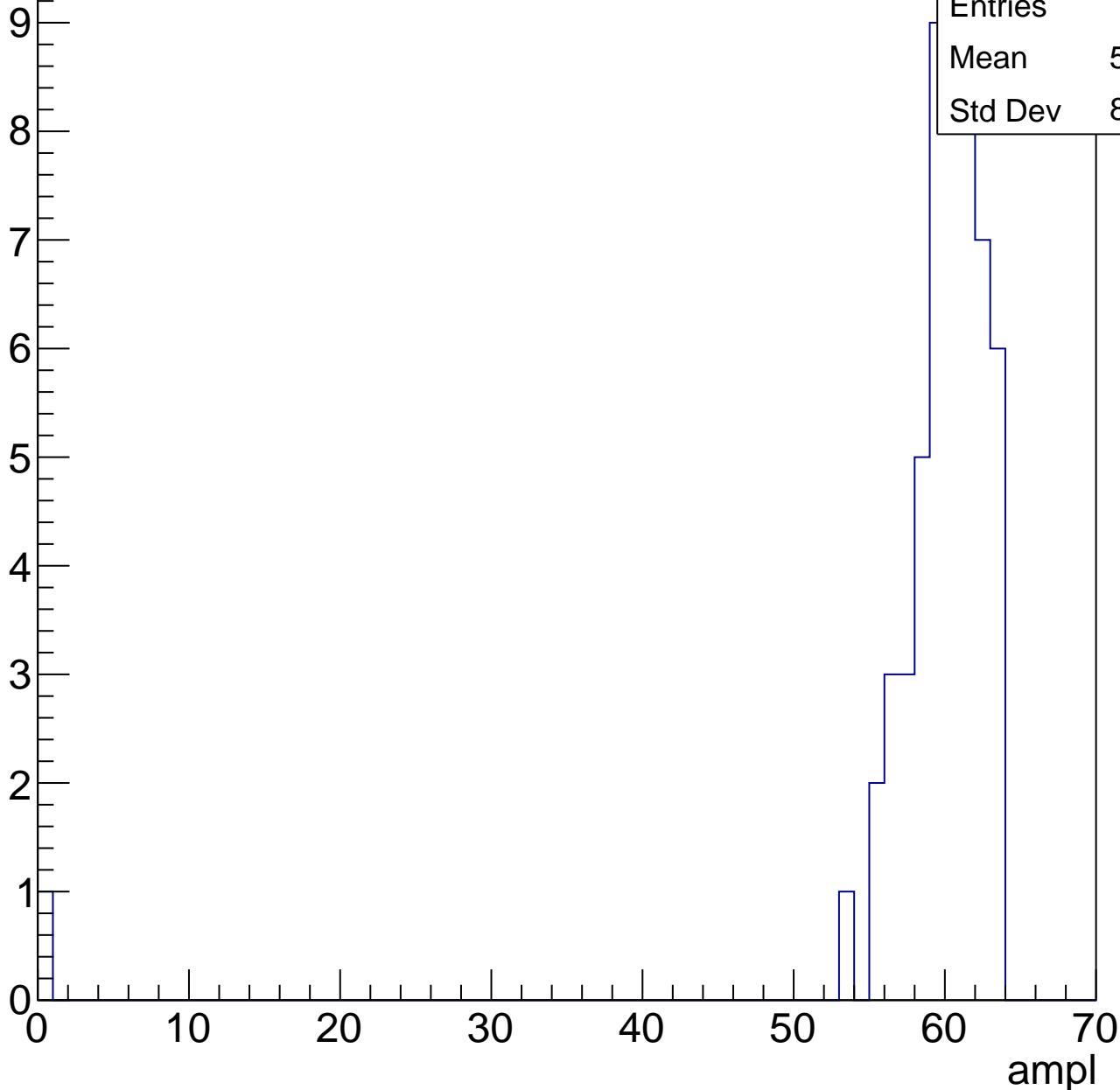


# B1L101S, U8-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

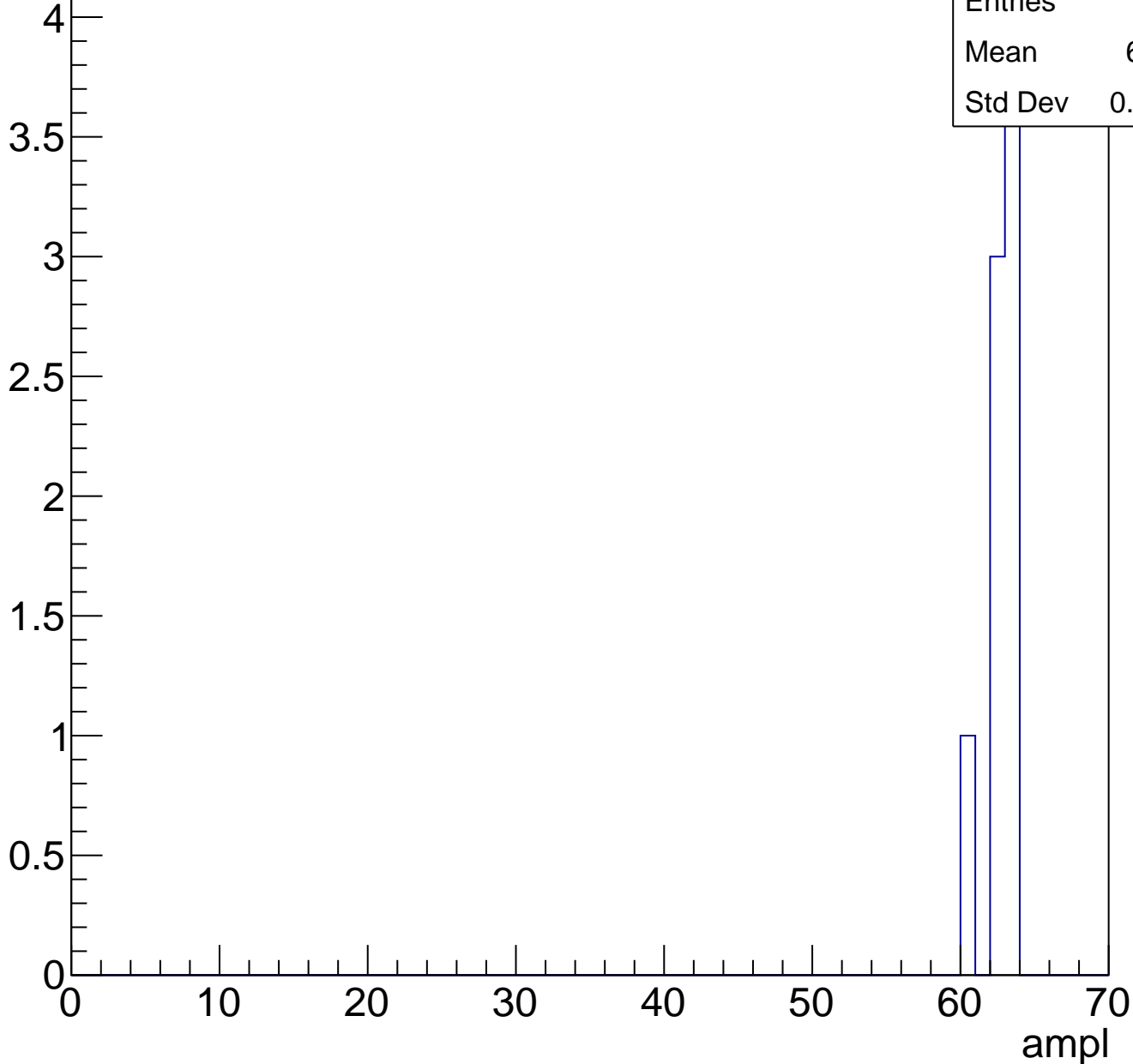
Entries	53
Mean	58.55
Std Dev	8.446



# B1L101S, U8-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U8-ch29, adc0

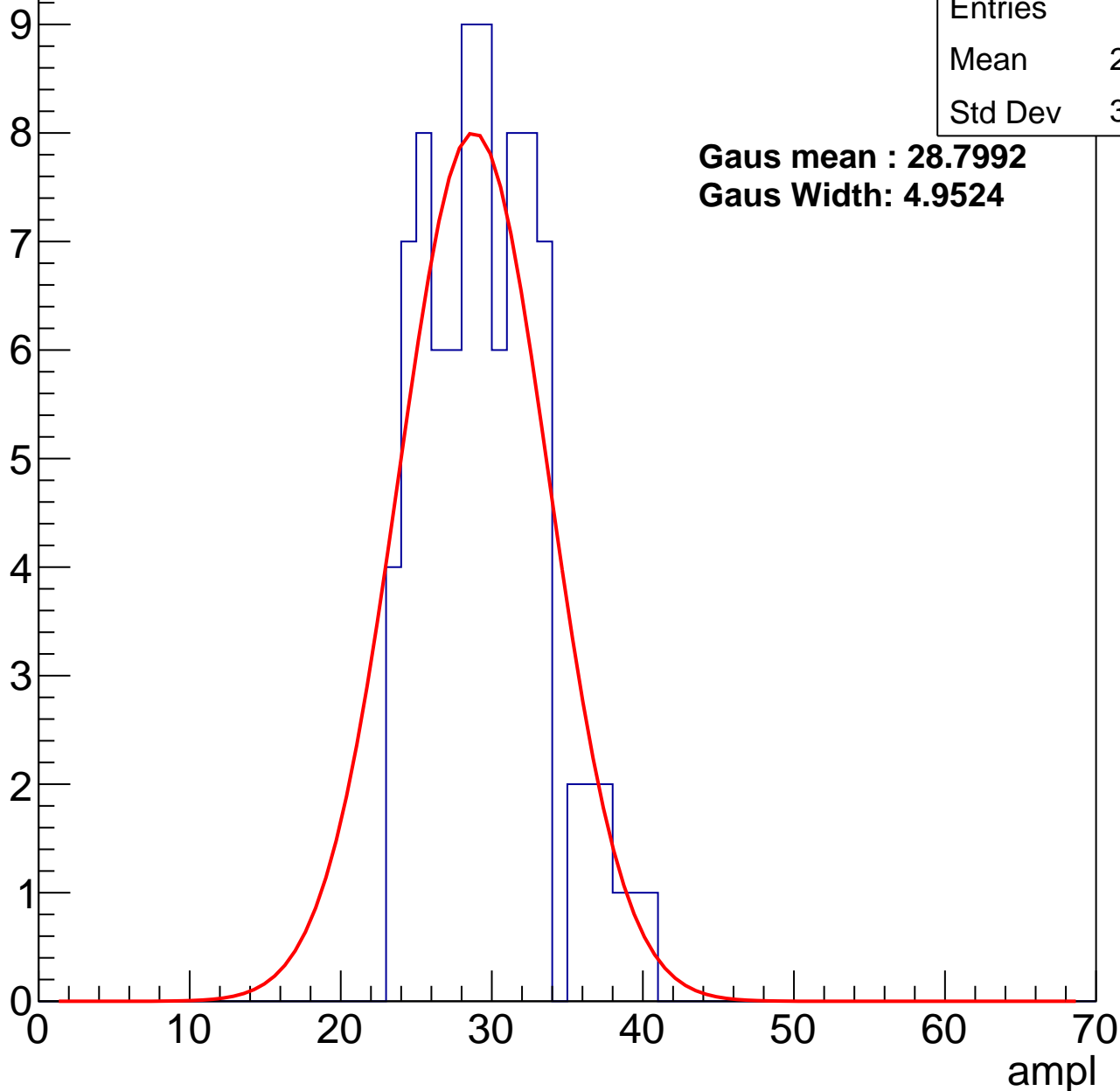
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	87
Mean	29.18
Std Dev	3.944

**Gaus mean : 28.7992**

**Gaus Width: 4.9524**



# B1L101S, U8-ch29, adc1

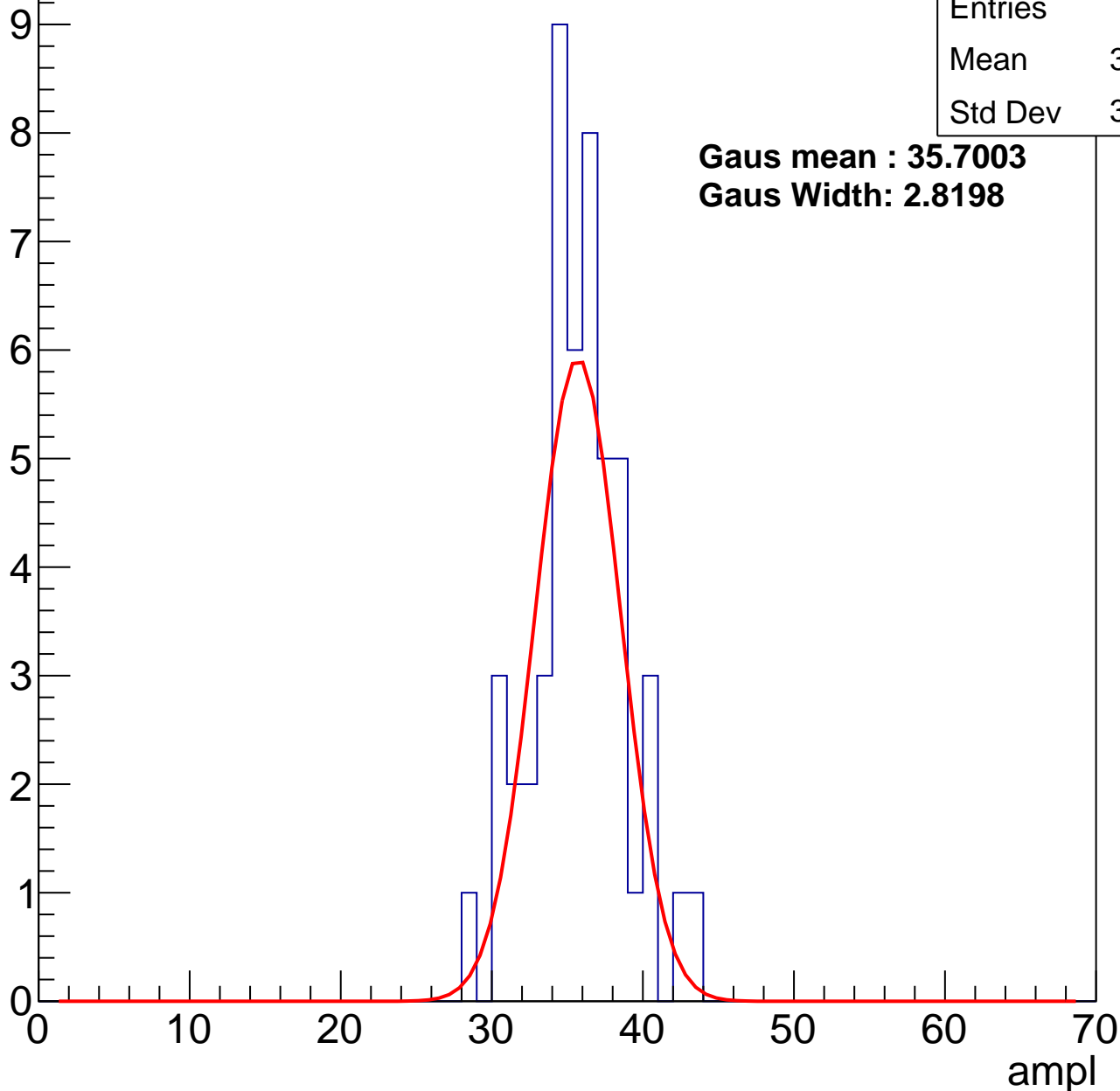
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	35.32
Std Dev	3.056

**Gaus mean : 35.7003**

**Gaus Width: 2.8198**



# B1L101S, U8-ch29, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	74
Mean	42.05
Std Dev	3.246

**Gaus mean : 42.4149**

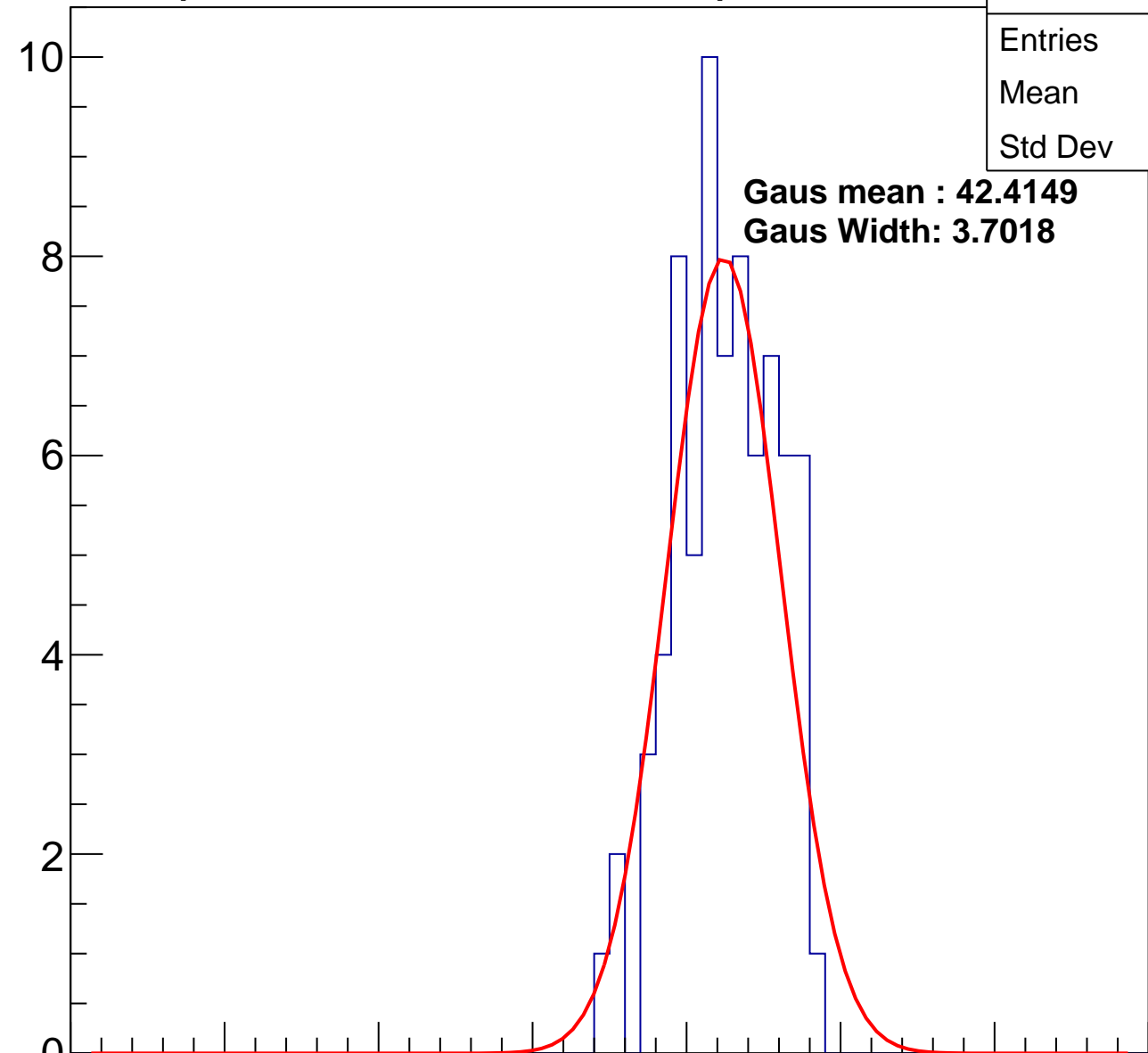
**Gaus Width: 3.7018**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

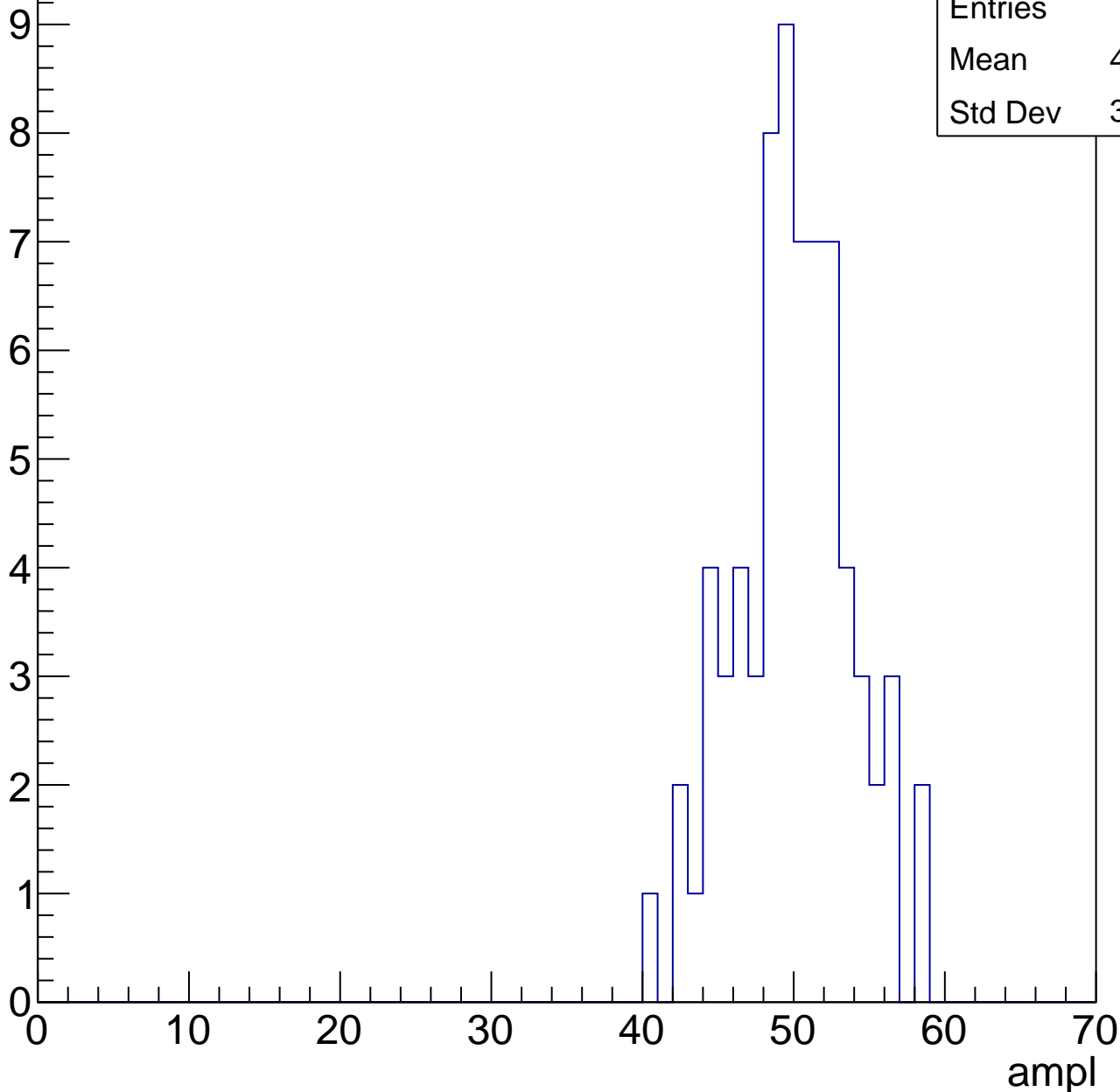


# B1L101S, U8-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	49.53
Std Dev	3.812

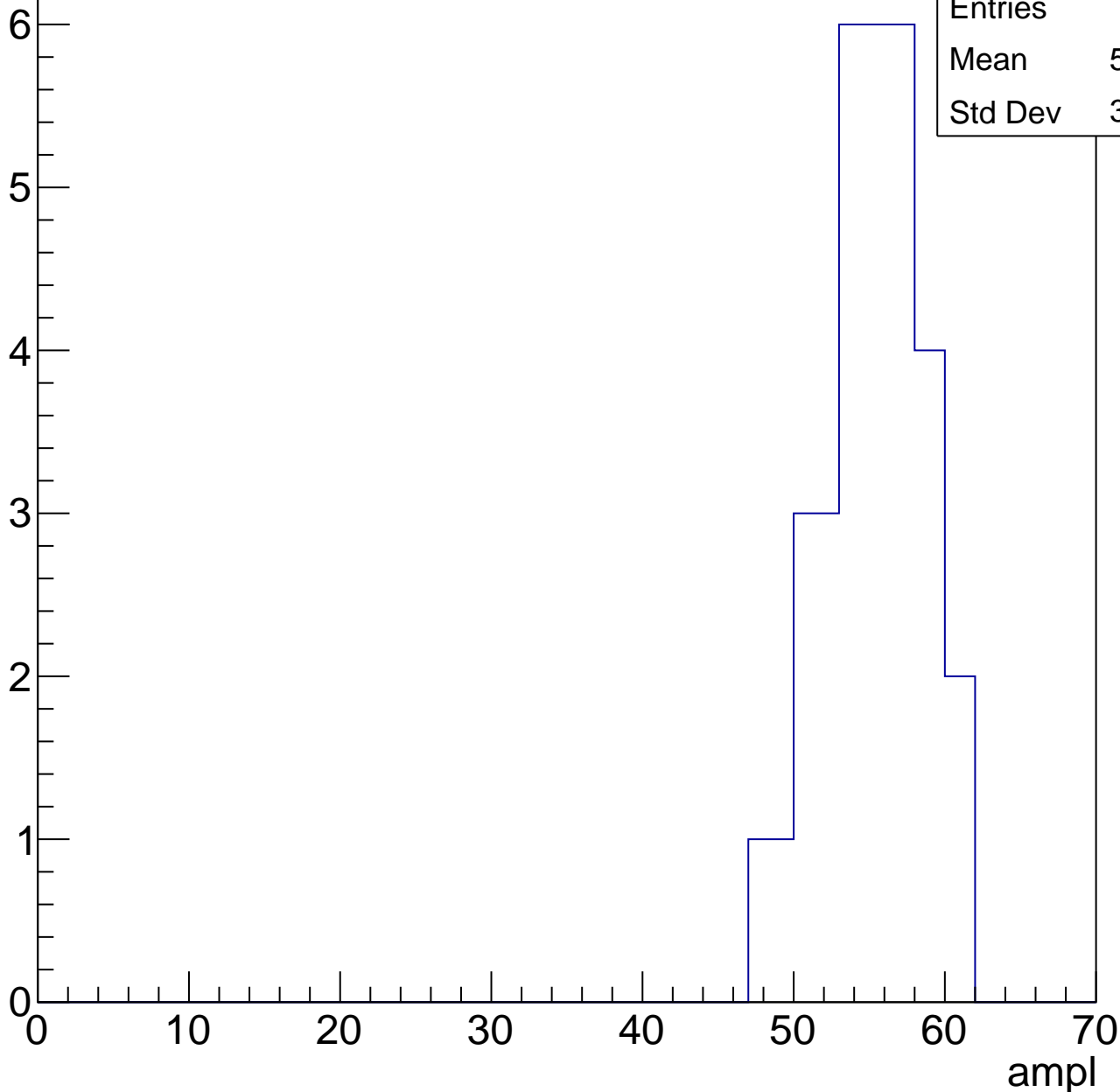


# B1L101S, U8-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	54.87
Std Dev	3.278



# B1L101S, U8-ch29, adc5

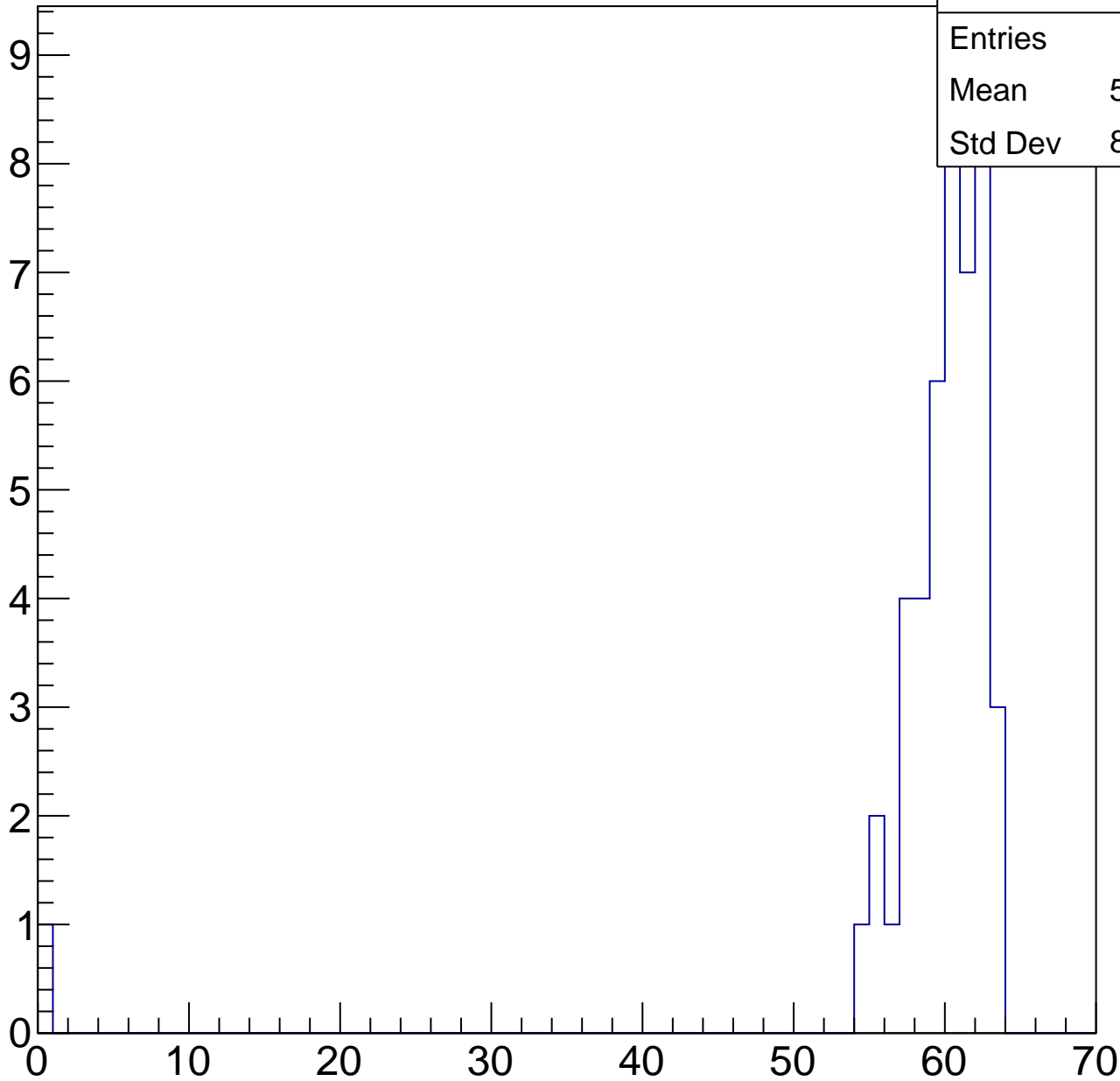
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	46
Mean	58.43
Std Dev	8.989

ampl

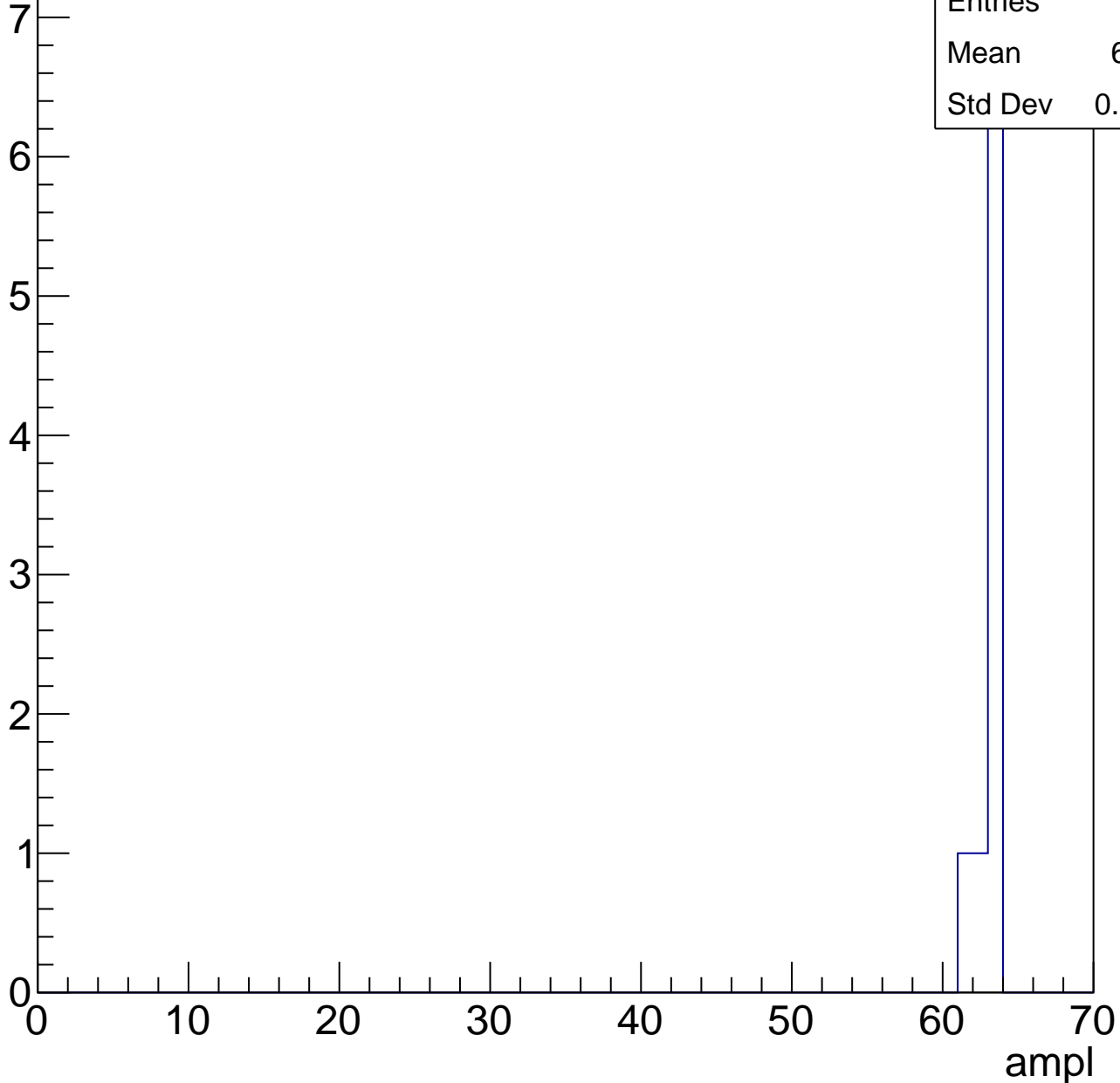


# B1L101S, U8-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	9
Mean	62.67
Std Dev	0.6667

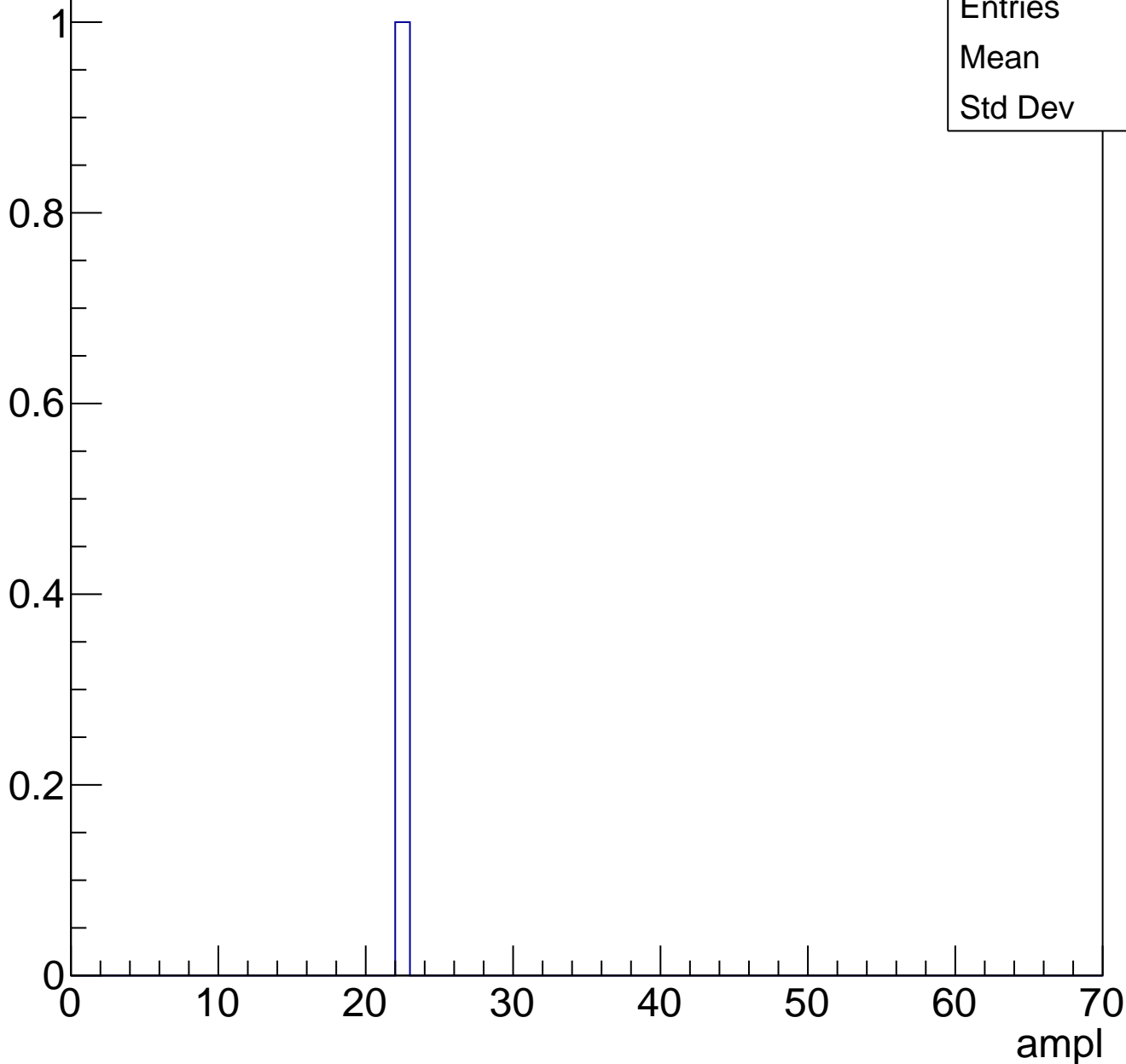




# B1L101S, U8-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch30, adc0

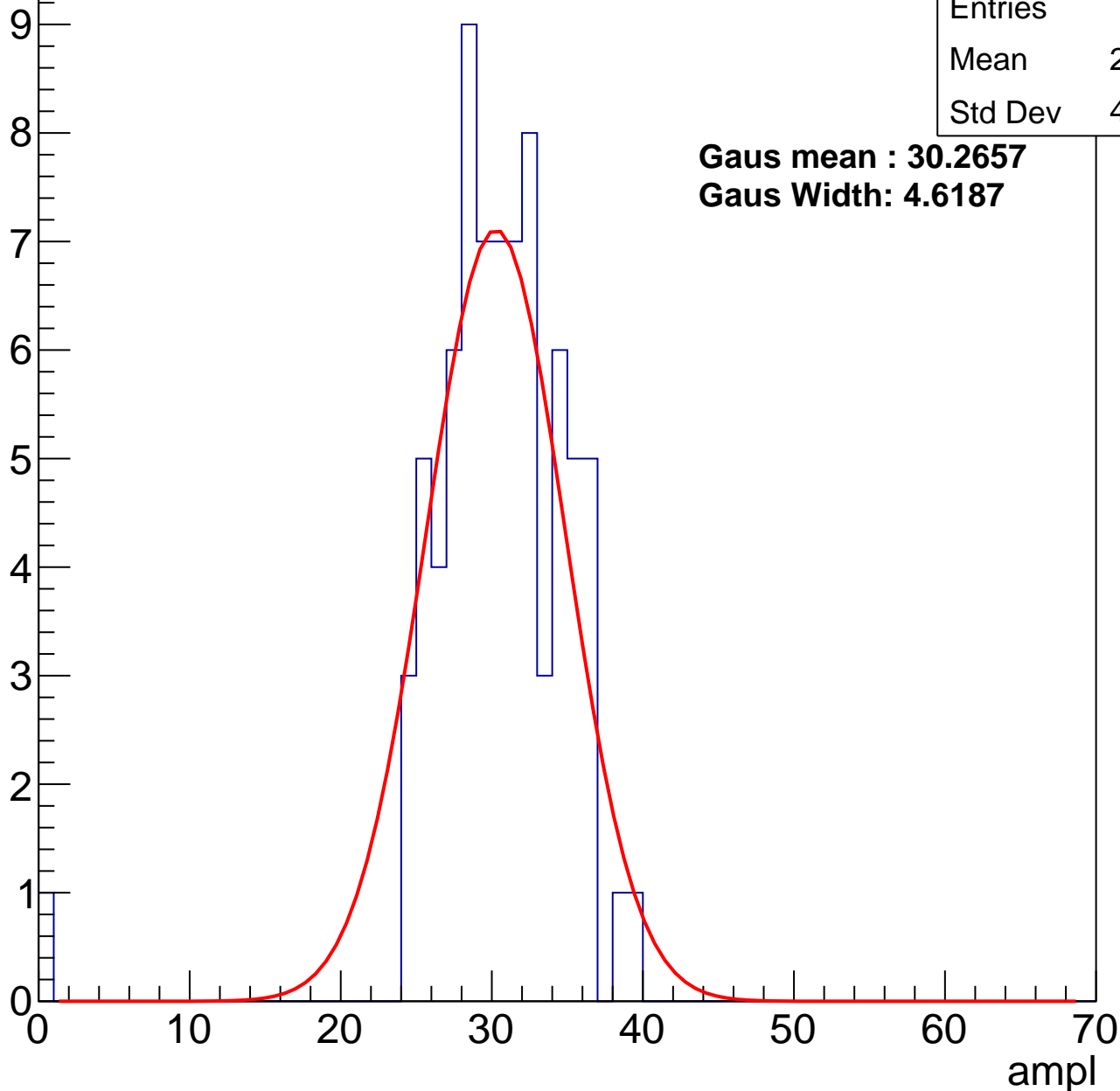
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	29.95
Std Dev	4.943

**Gaus mean : 30.2657**

**Gaus Width: 4.6187**



# B1L101S, U8-ch30, adc1

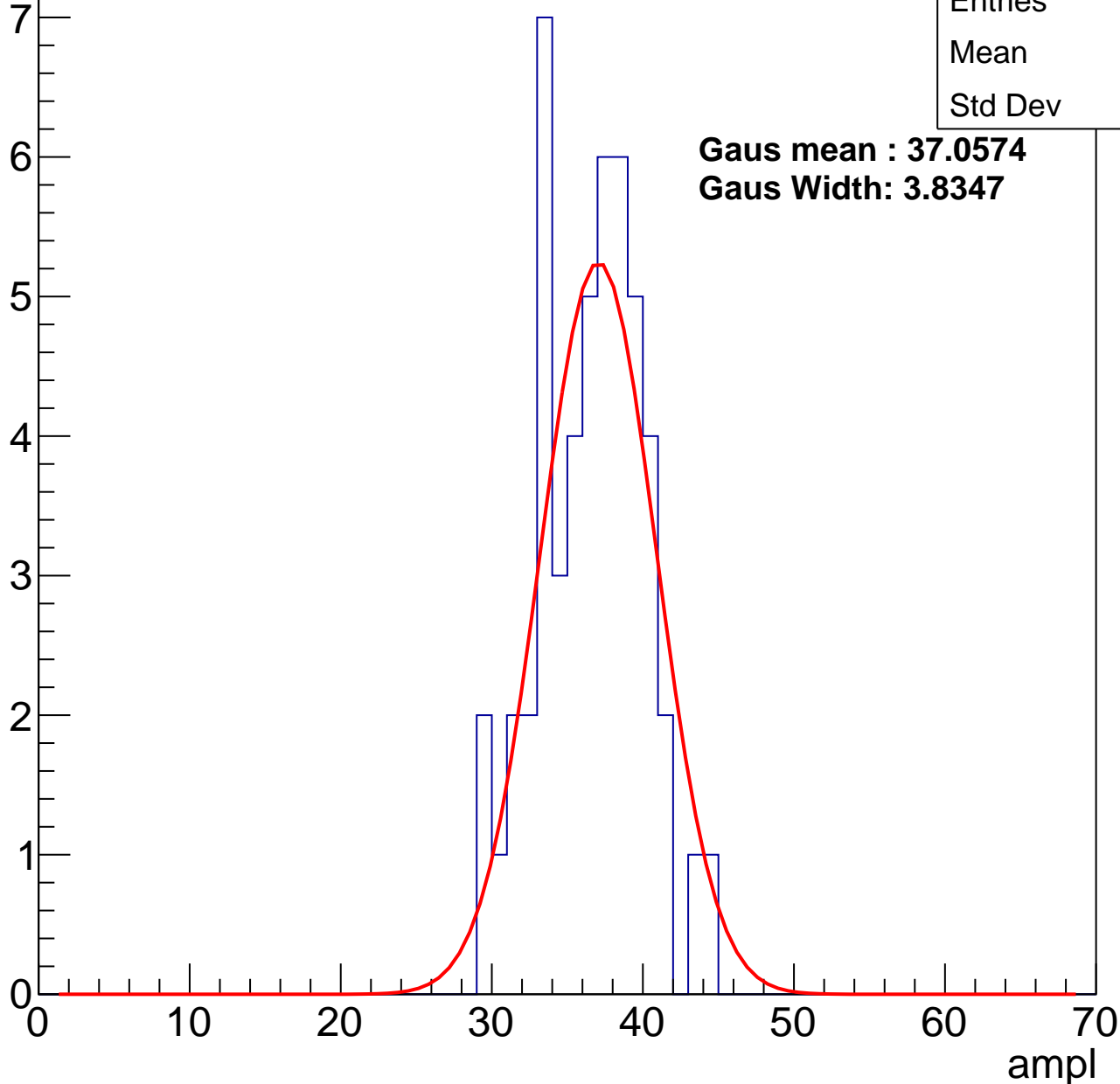
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	36.1
Std Dev	3.42

**Gaus mean : 37.0574**

**Gaus Width: 3.8347**



# B1L101S, U8-ch30, adc2

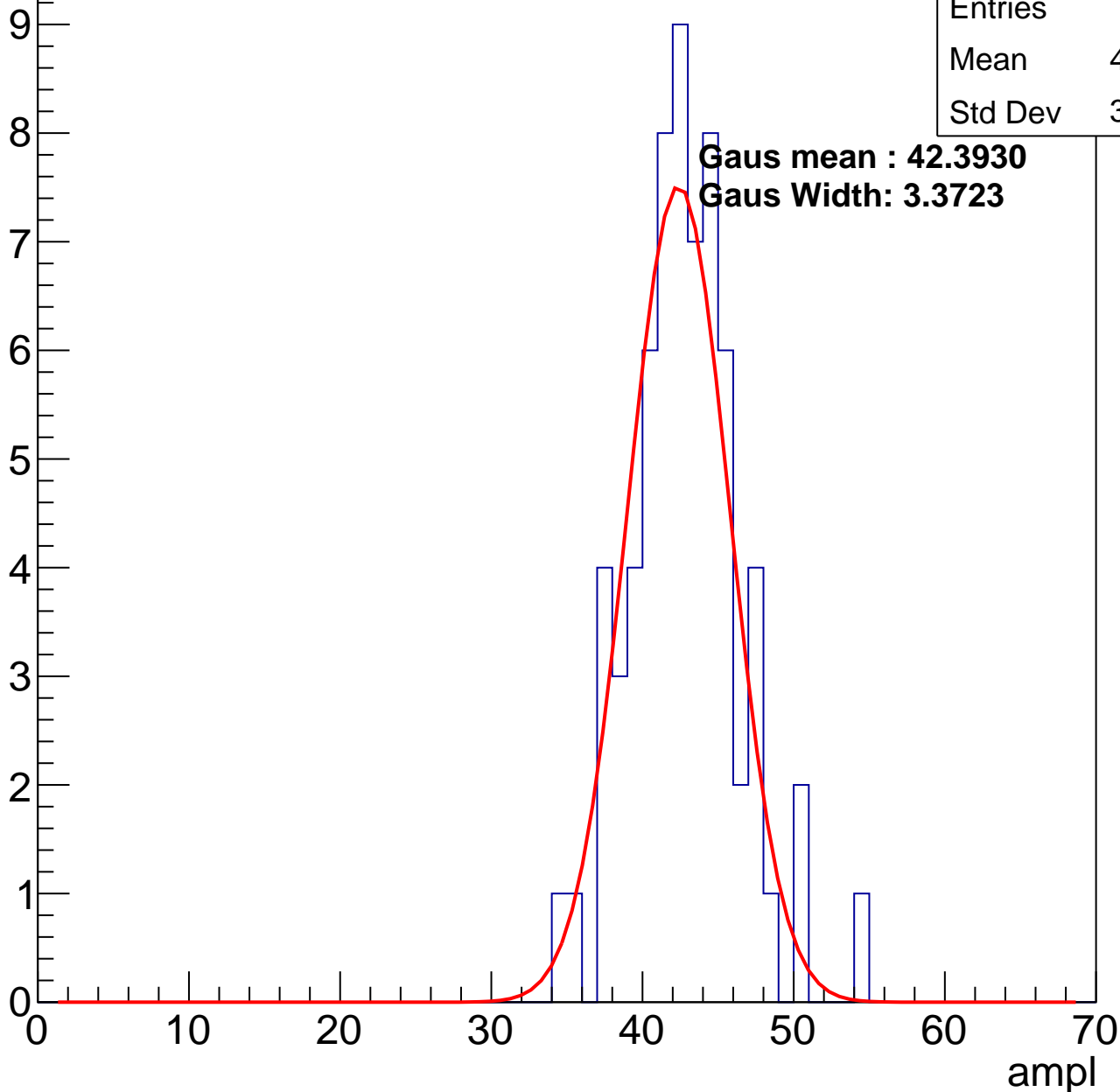
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	42.36
Std Dev	3.569

**Gaus mean : 42.3930**

**Gaus Width: 3.3723**

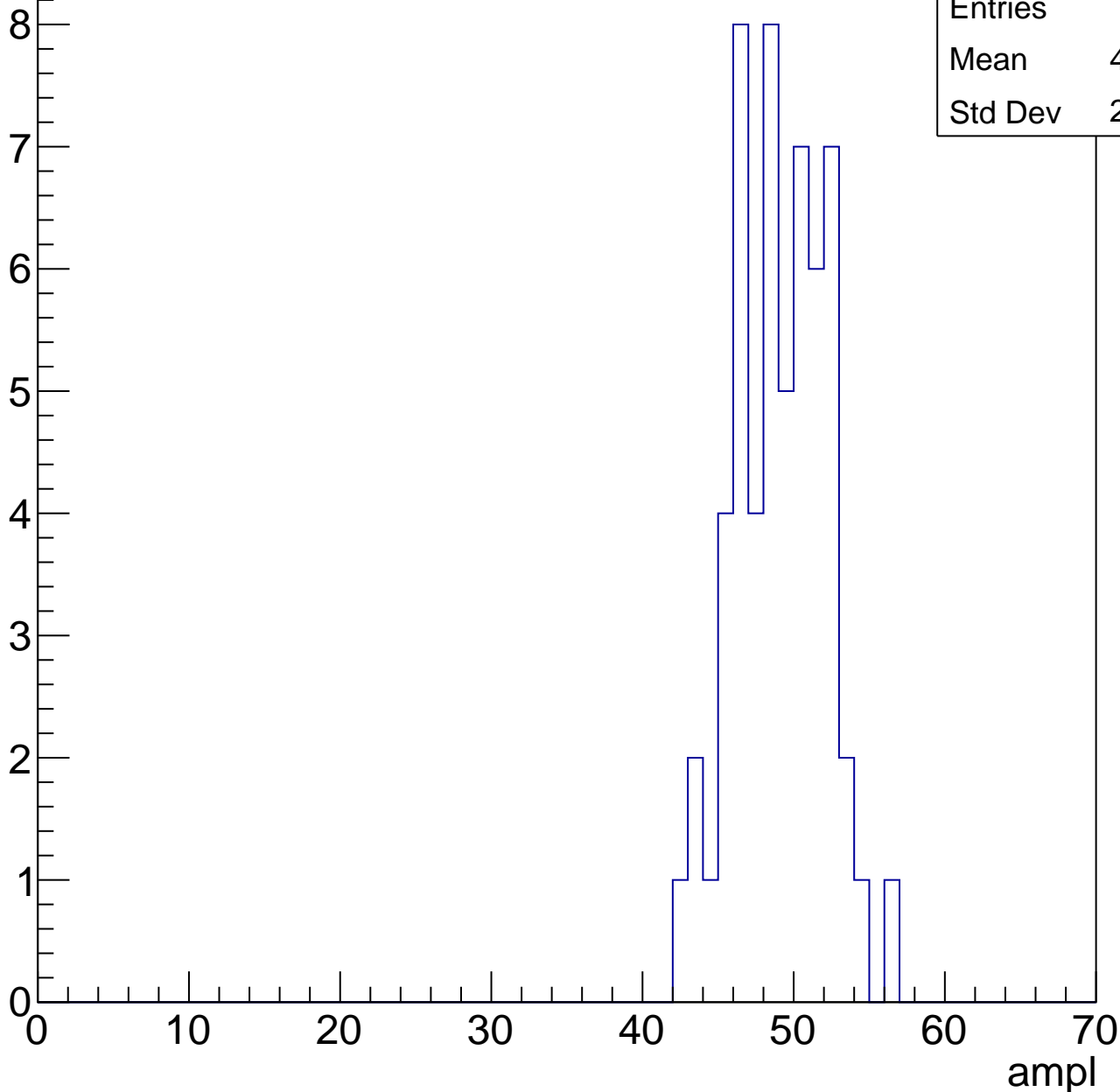


# B1L101S, U8-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

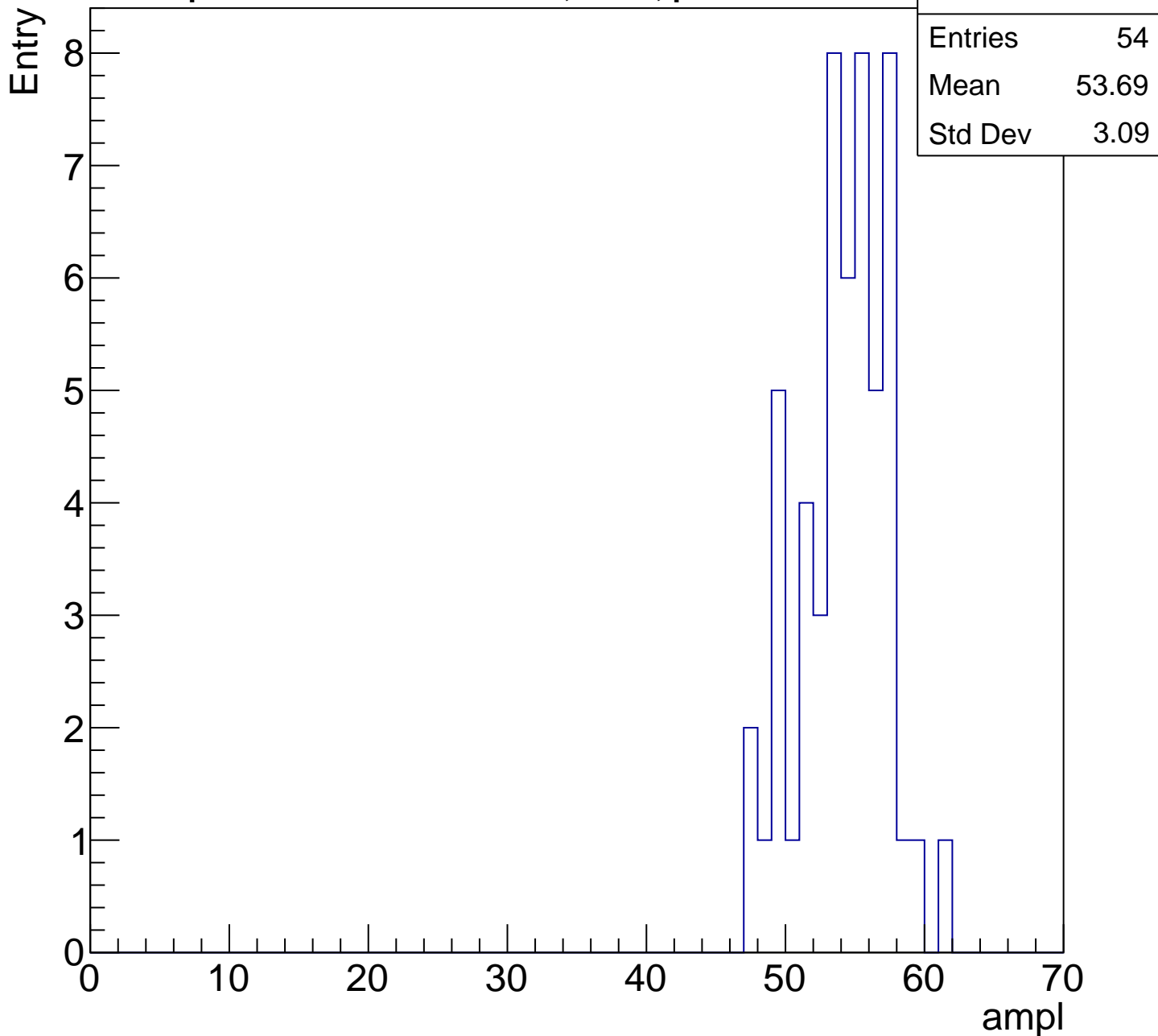
Entry

Entries	57
Mean	48.65
Std Dev	2.959



# B1L101S, U8-ch30, adc4

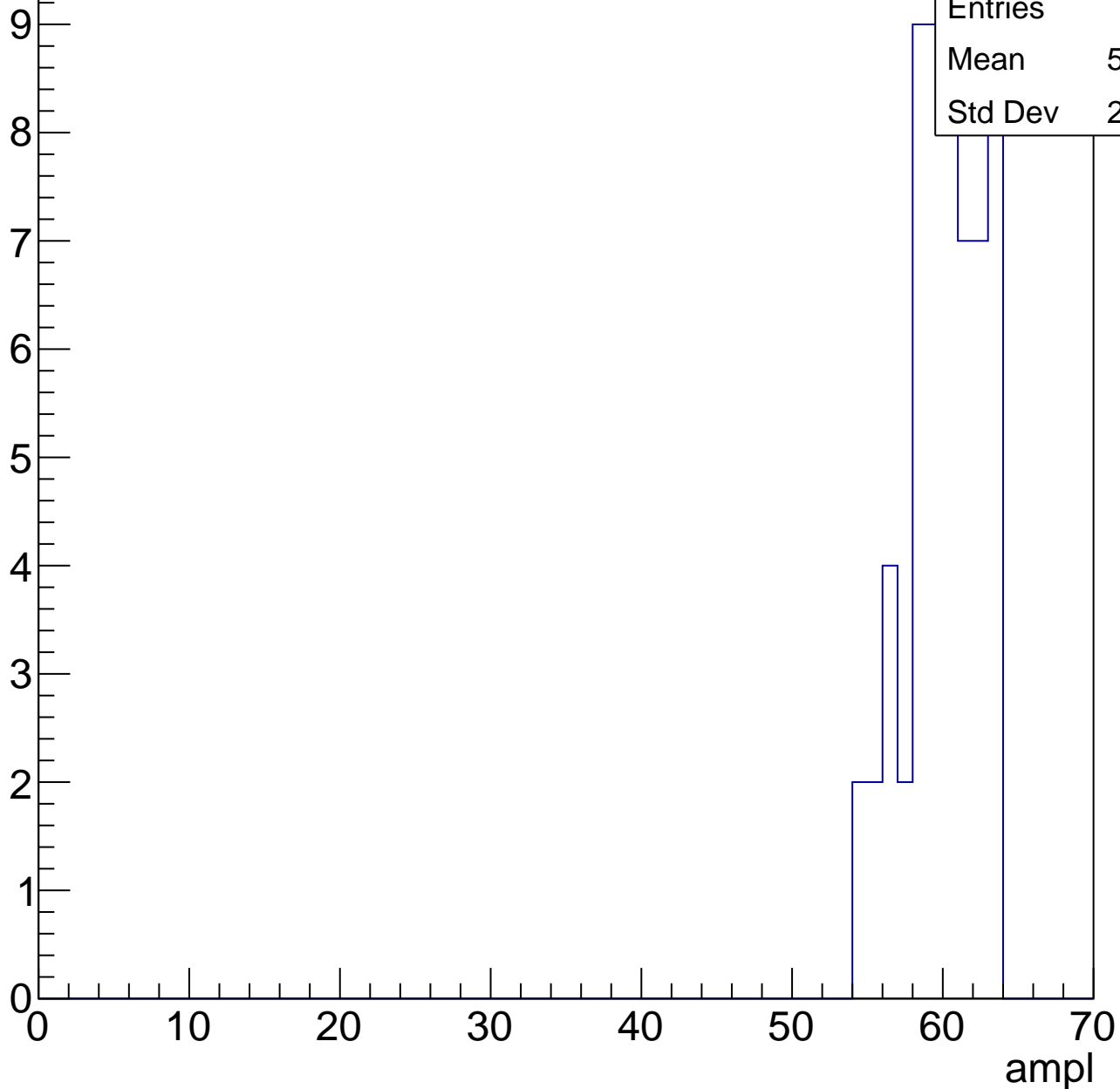
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U8-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

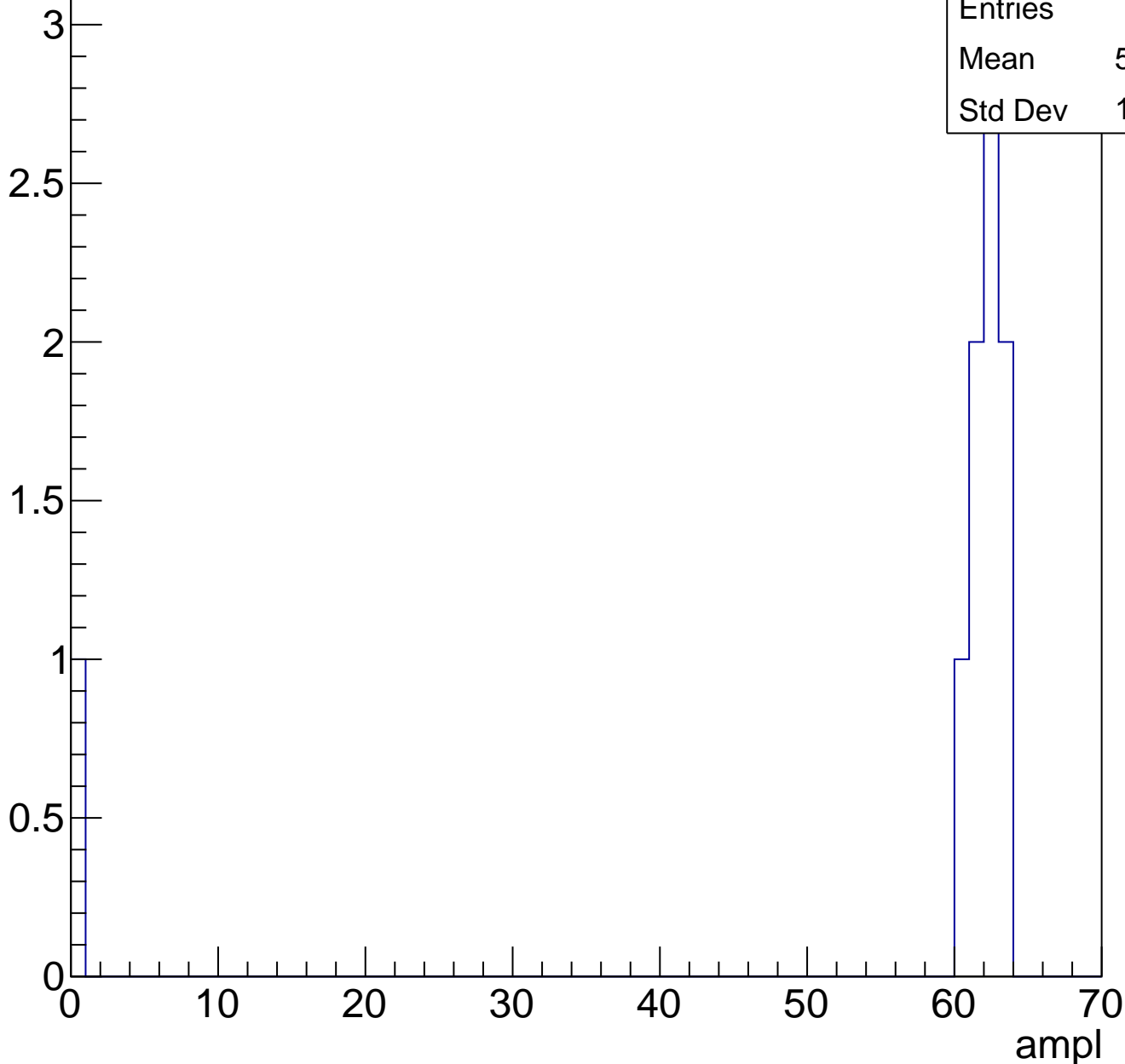
Entry



# B1L101S, U8-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch31, adc0

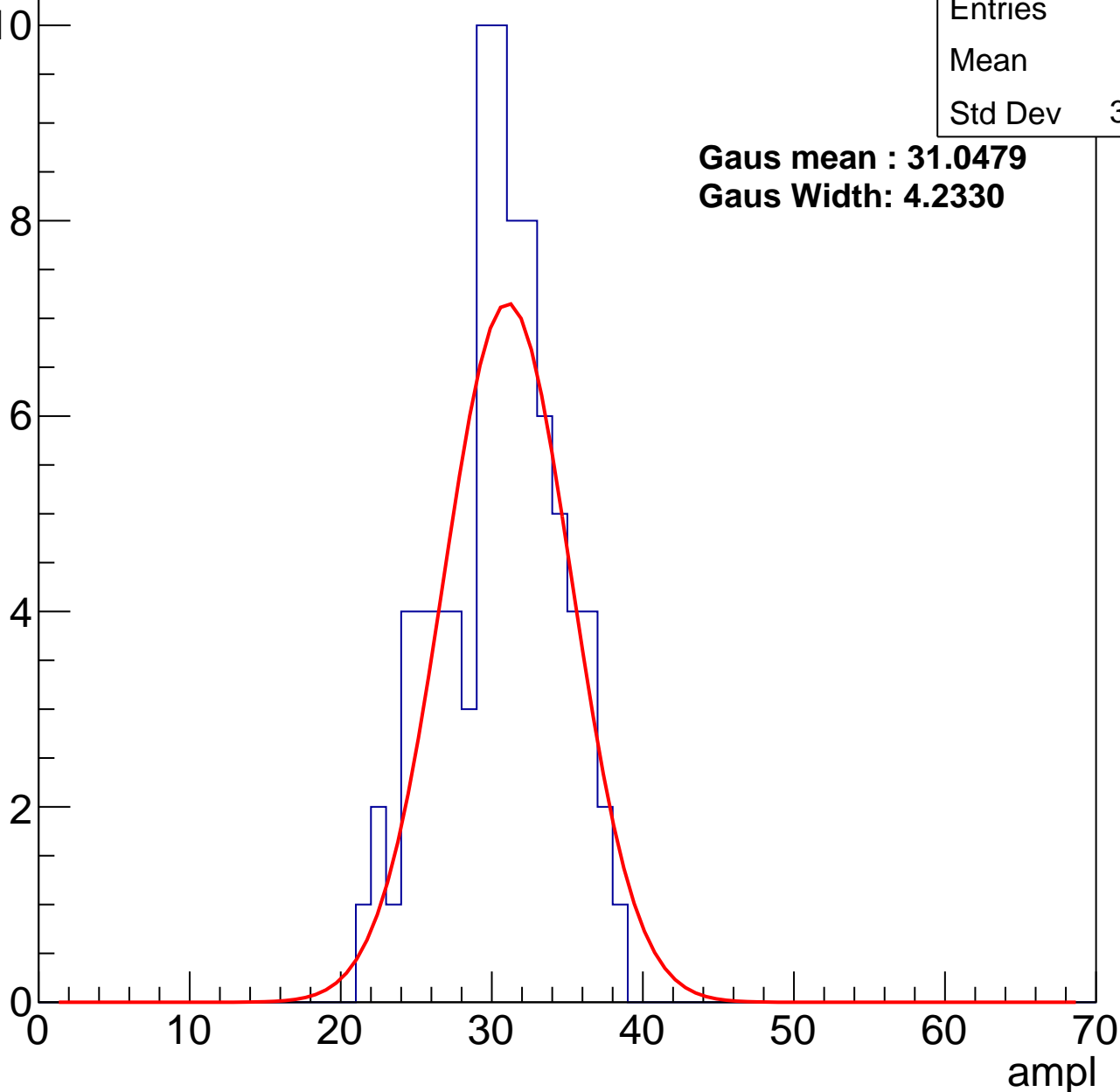
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	30.1
Std Dev	3.854

**Gaus mean : 31.0479**

**Gaus Width: 4.2330**



# B1L101S, U8-ch31, adc1

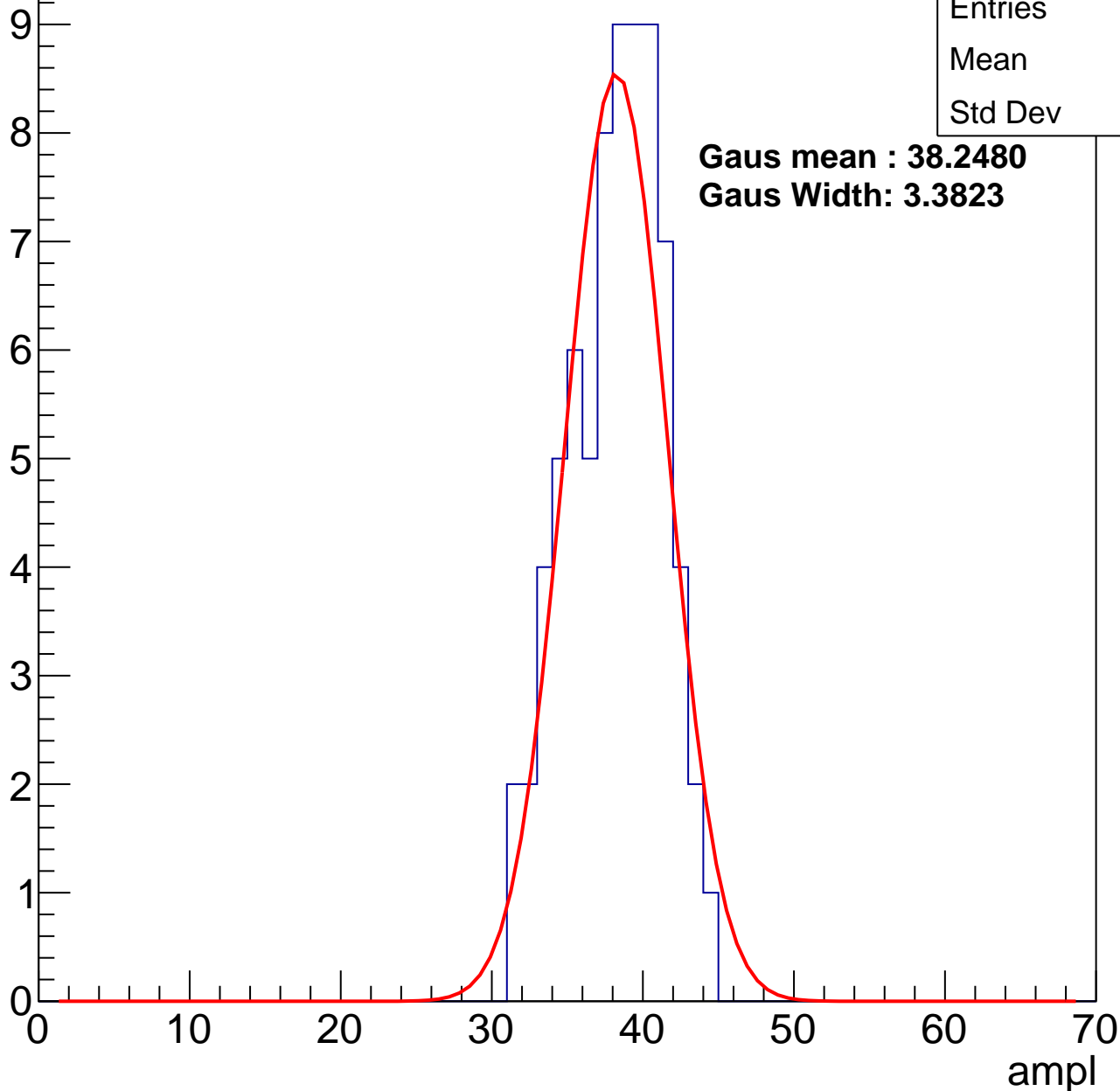
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	37.7
Std Dev	3.06

**Gaus mean : 38.2480**

**Gaus Width: 3.3823**



# B1L101S, U8-ch31, adc2

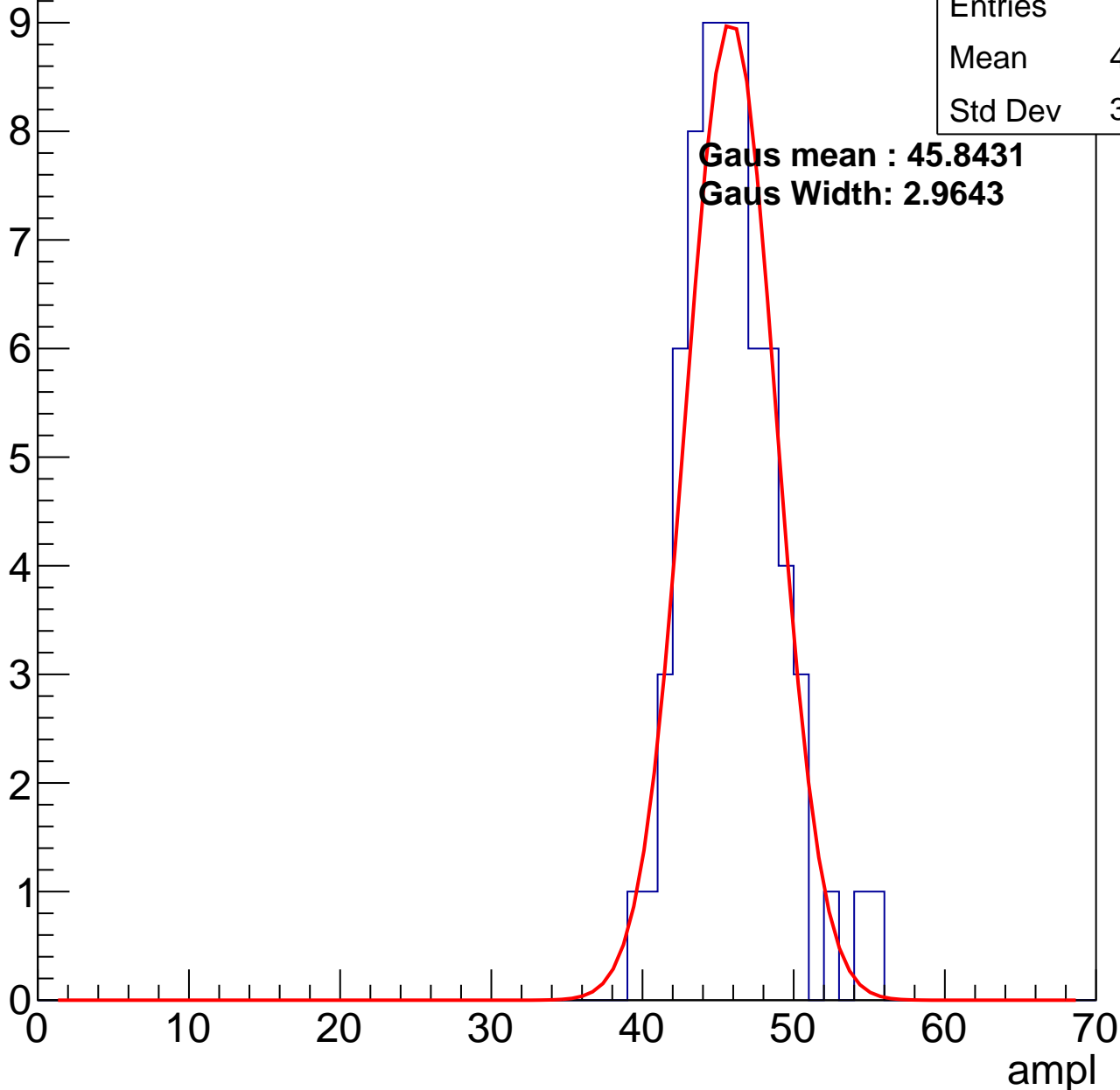
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	45.44
Std Dev	3.084

**Gaus mean : 45.8431**

**Gaus Width: 2.9643**

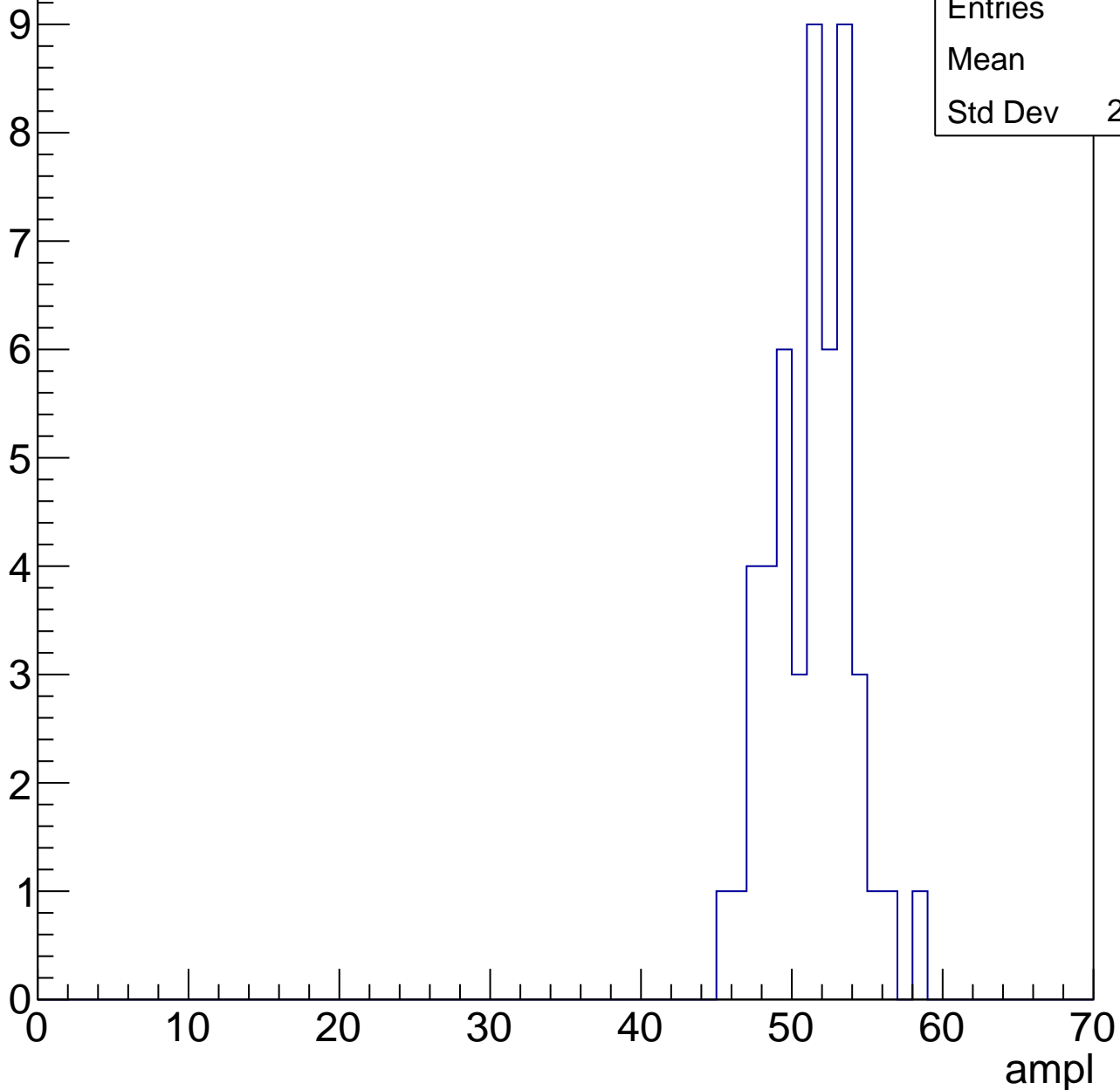


# B1L101S, U8-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	50.9
Std Dev	2.659

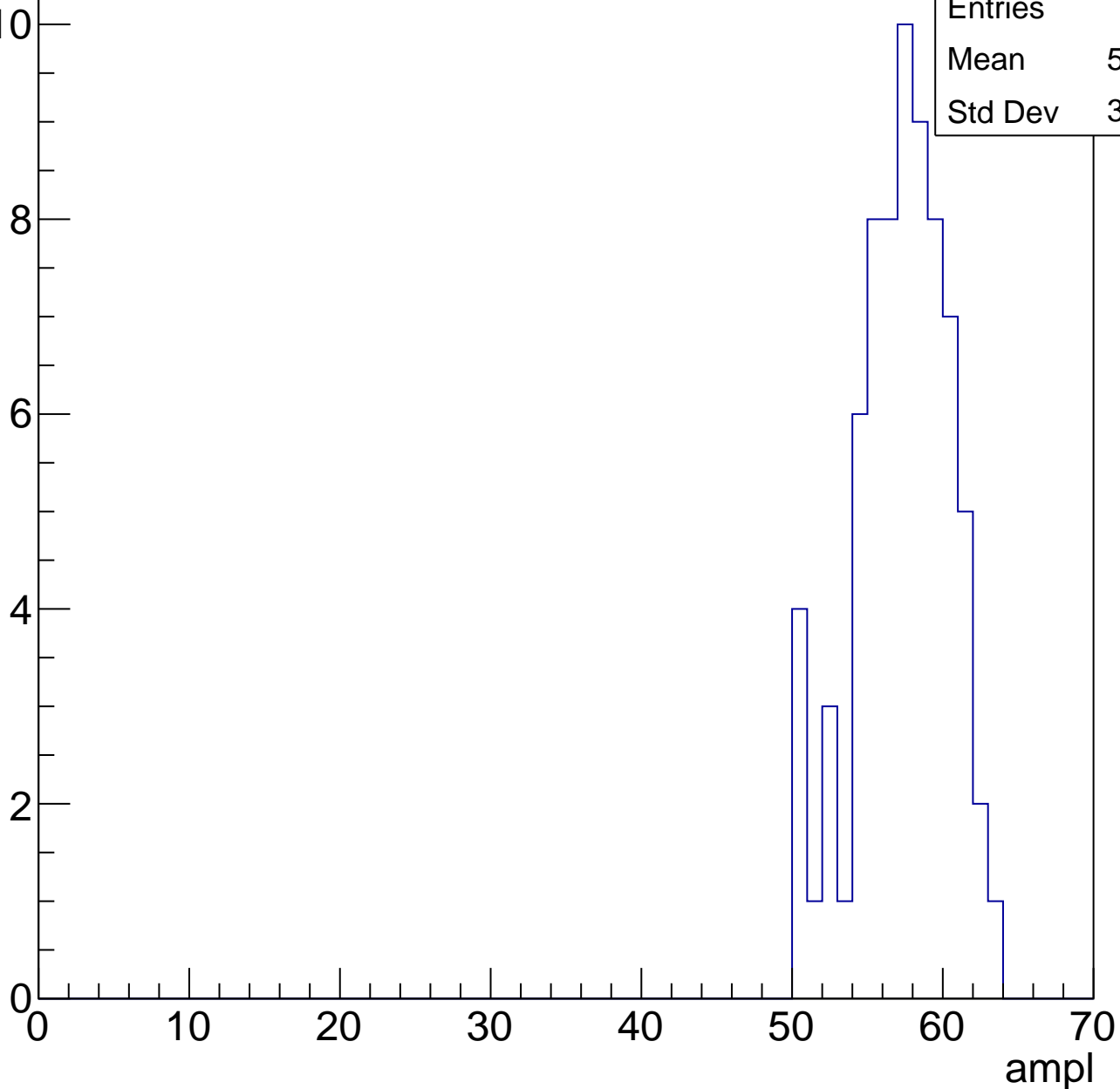


# B1L101S, U8-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	56.82
Std Dev	3.063

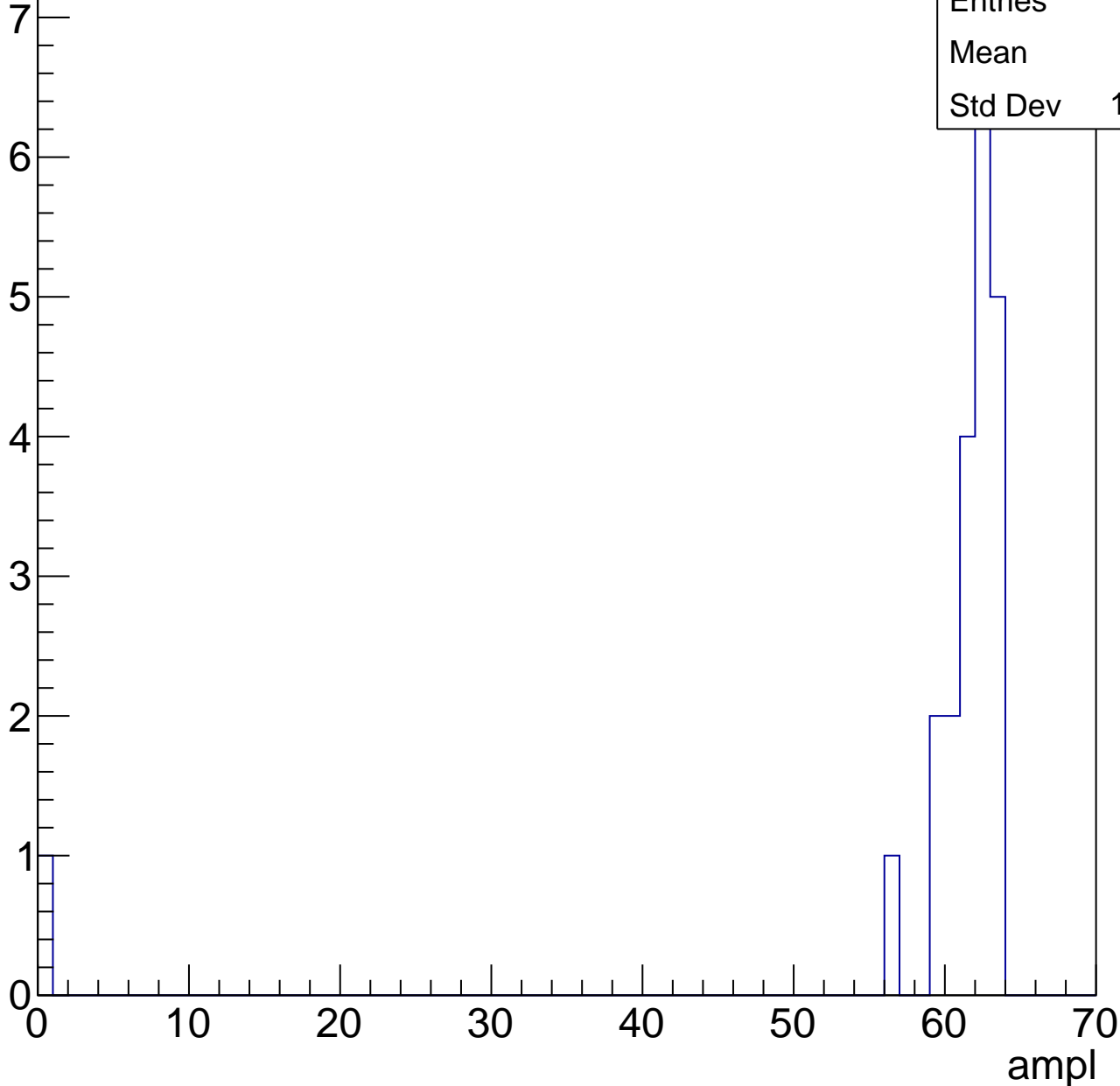


# B1L101S, U8-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

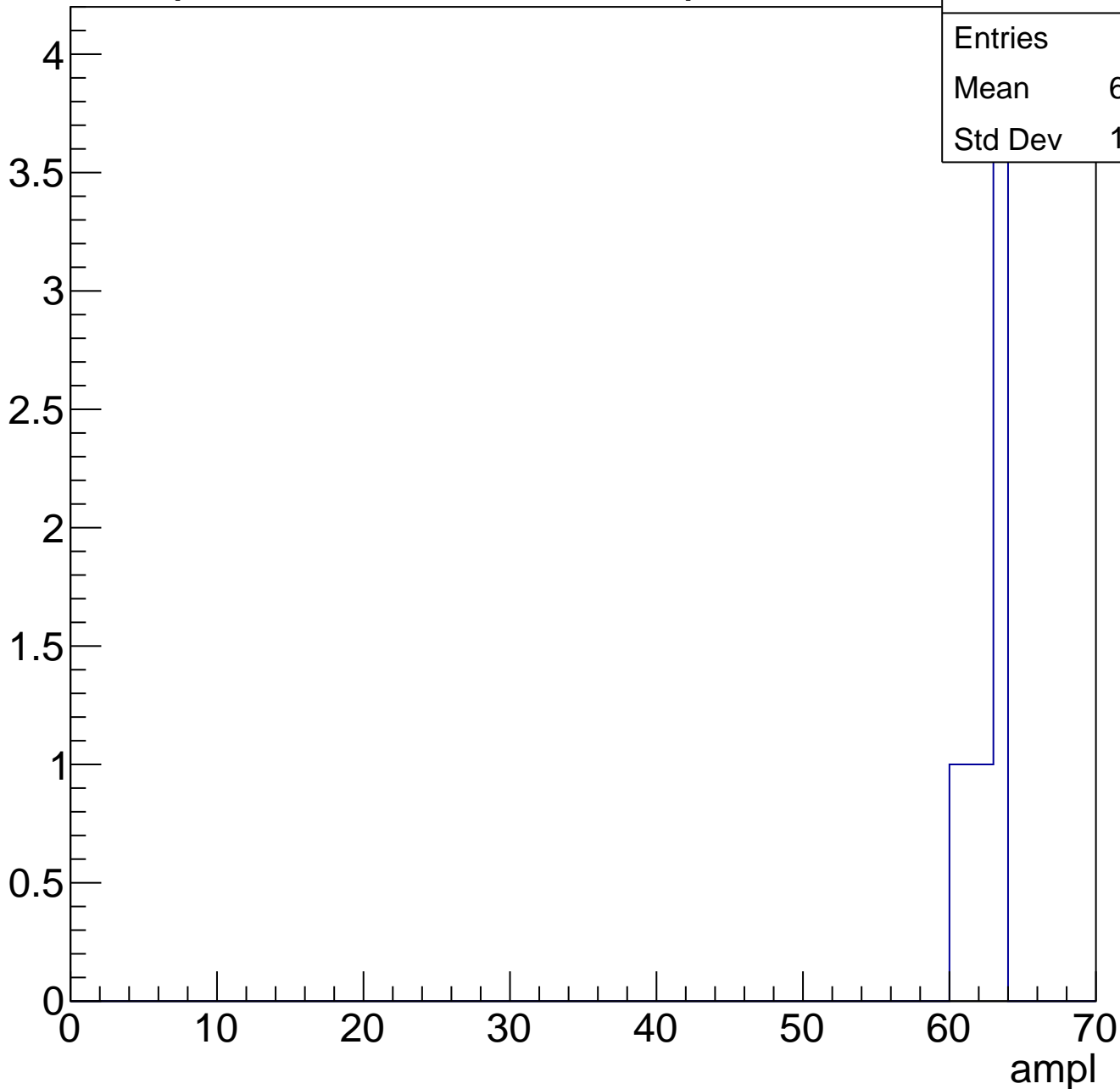
Entries	22
Mean	58.5
Std Dev	12.87



# B1L101S, U8-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U8-ch32, adc0

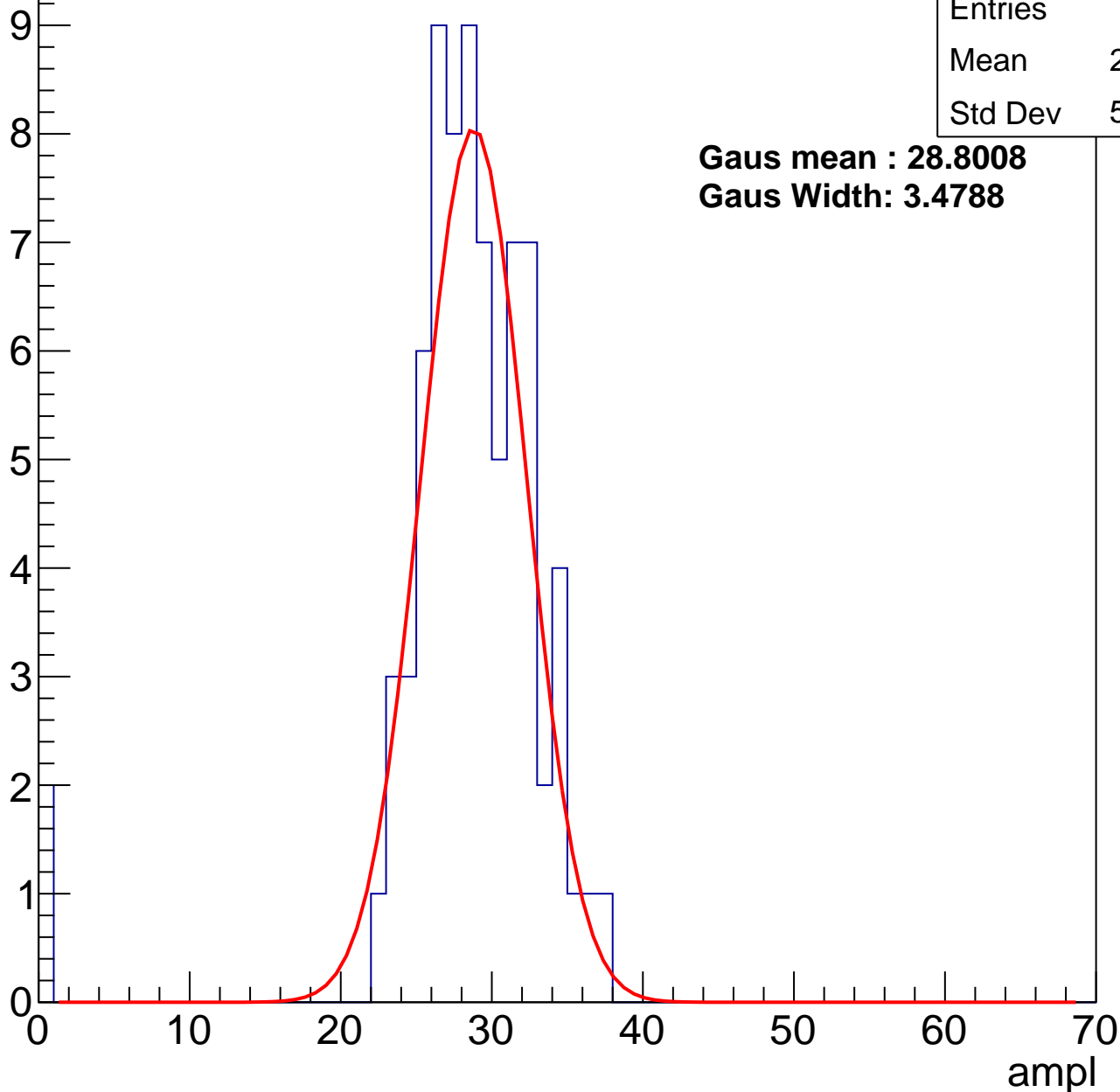
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	27.88
Std Dev	5.636

**Gaus mean : 28.8008**

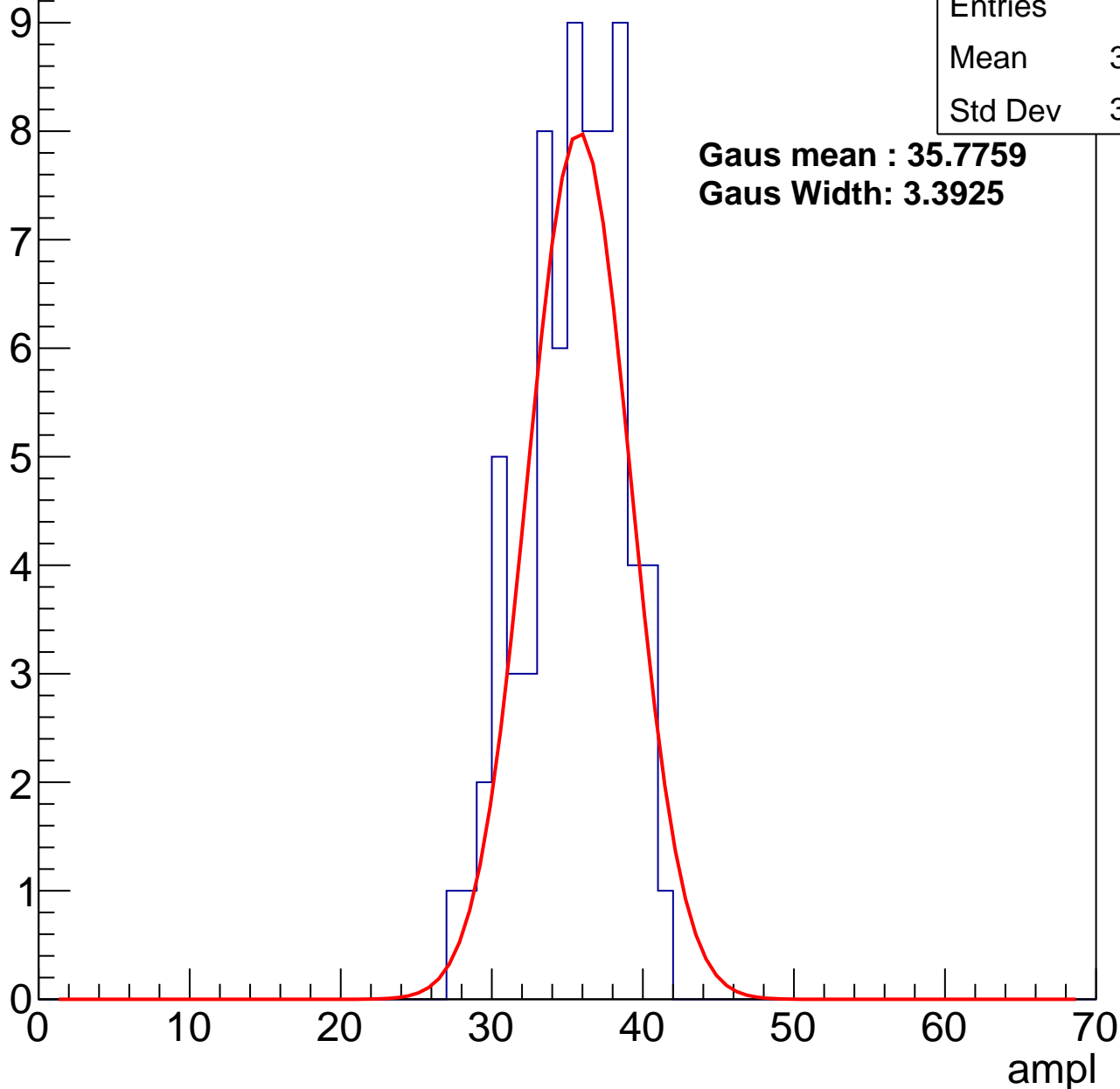
**Gaus Width: 3.4788**



# B1L101S, U8-ch32, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	72
Mean	34.97
Std Dev	3.214

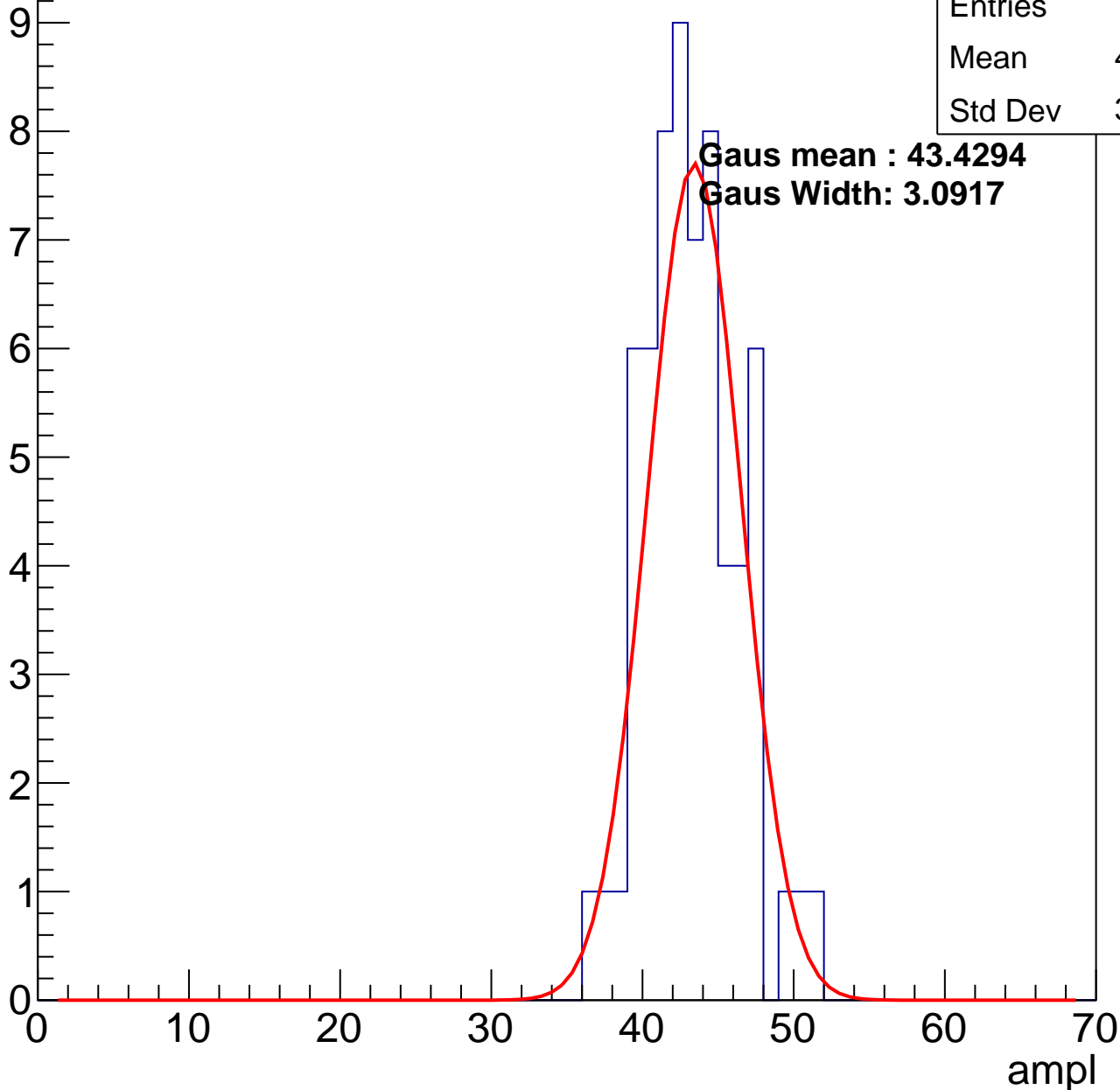
# B1L101S, U8-ch32, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	42.81
Std Dev	3.071

**Gaus mean : 43.4294**  
**Gaus Width: 3.0917**



# B1L101S, U8-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

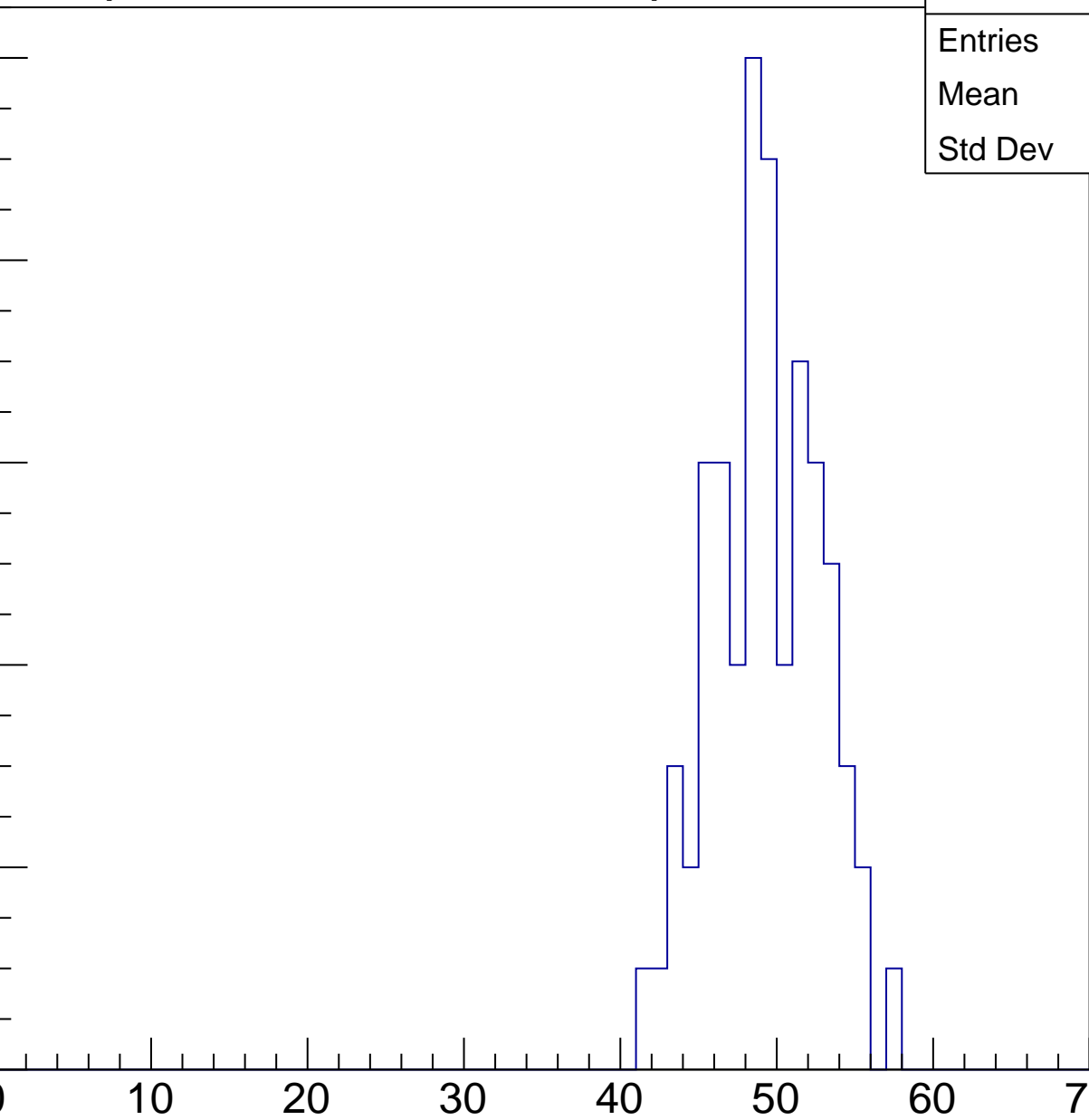
Entries	70
Mean	48.83
Std Dev	3.427

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

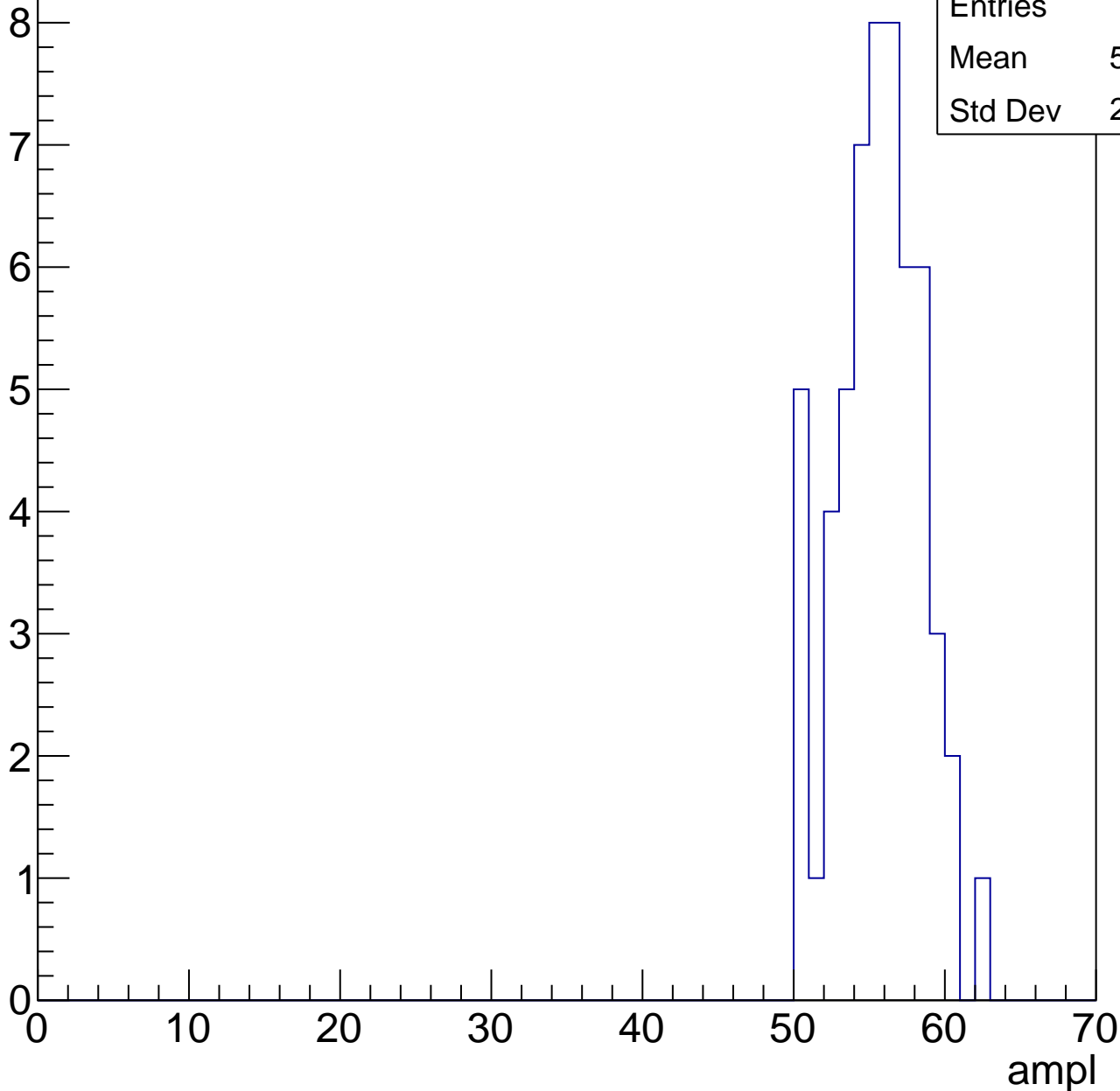


# B1L101S, U8-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	55.16
Std Dev	2.789

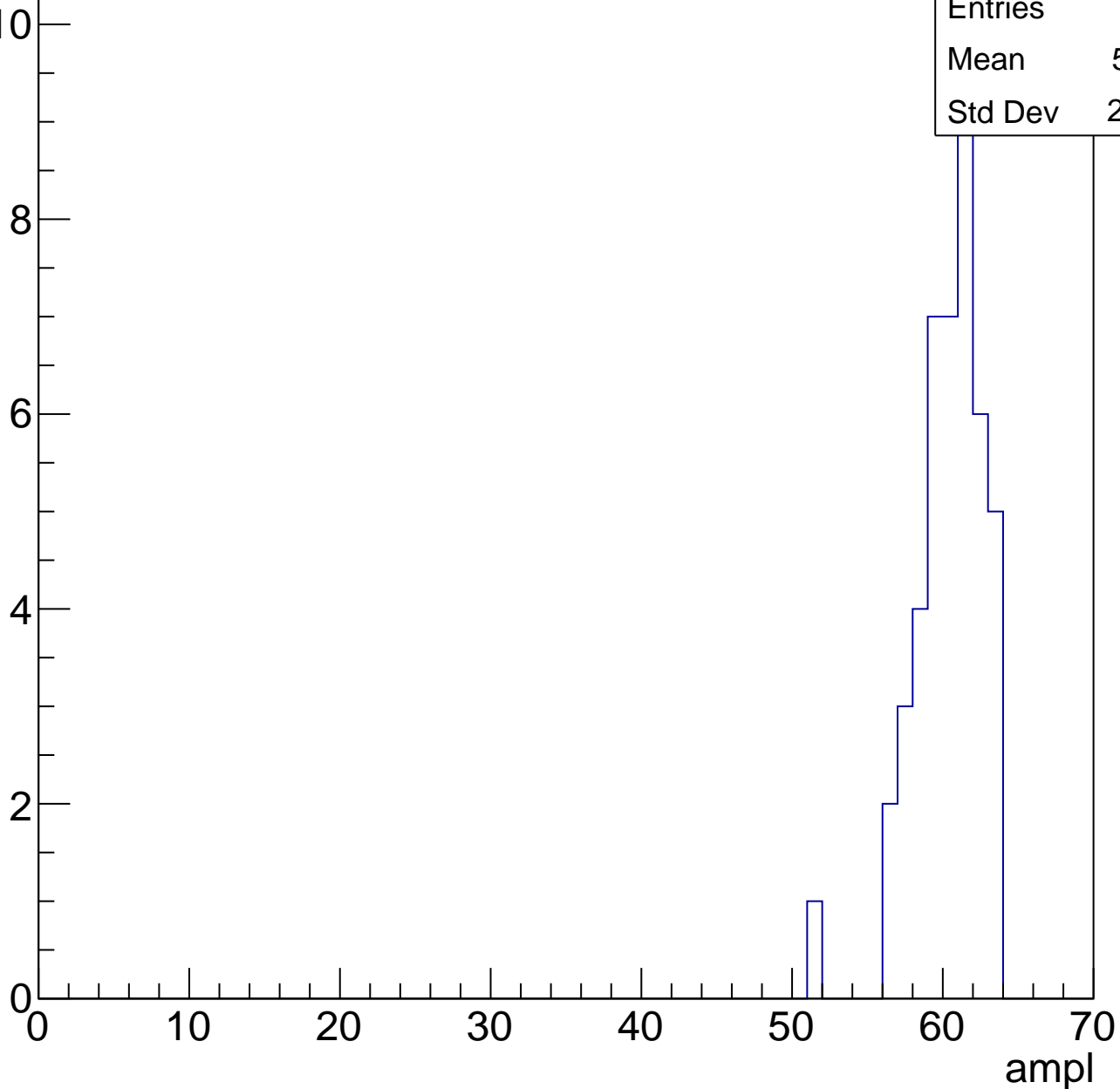


# B1L101S, U8-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	59.91
Std Dev	2.317

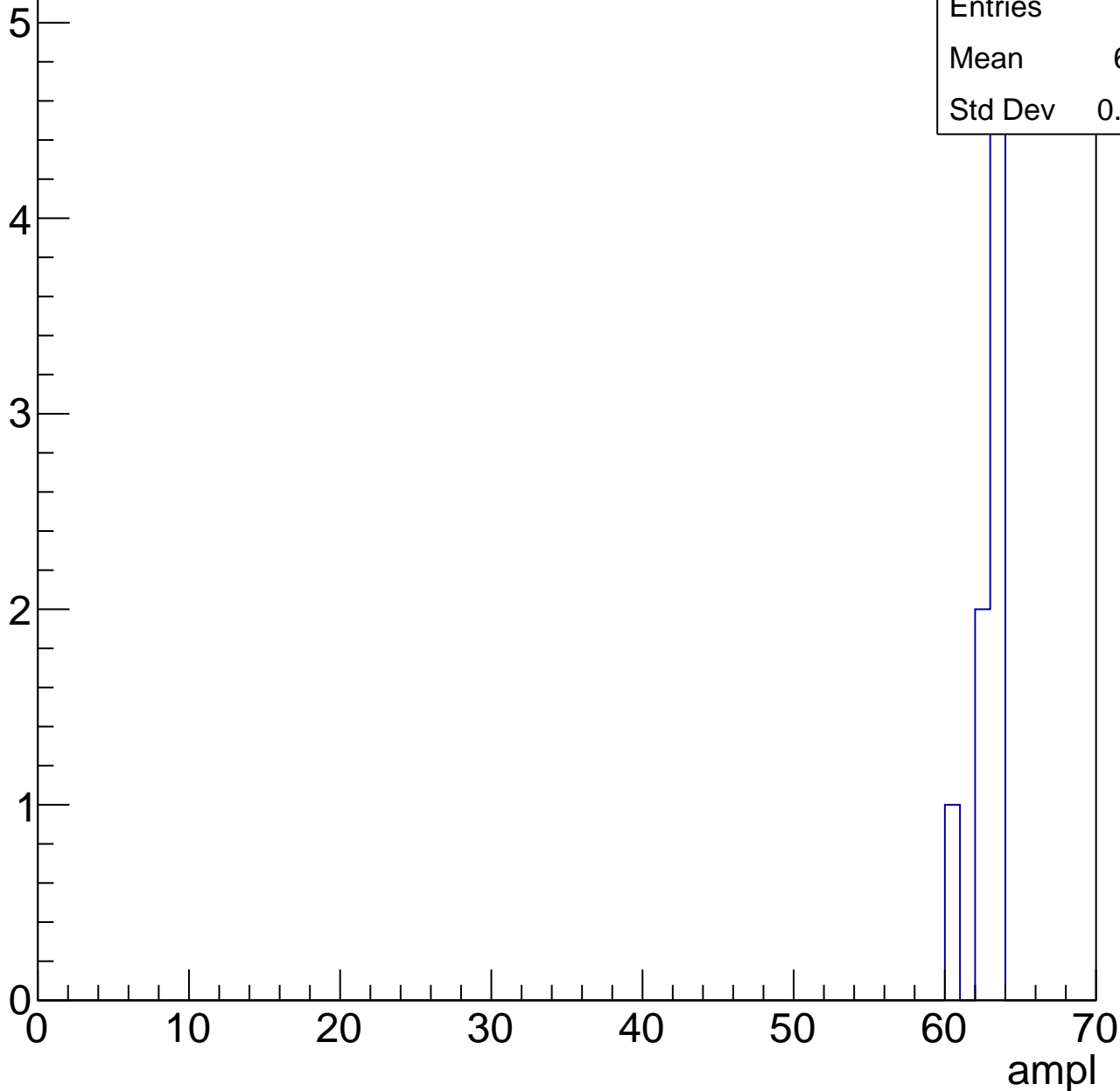


# B1L101S, U8-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	8
Mean	62.38
Std Dev	0.9922





# B1L101S, U8-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch33, adc0

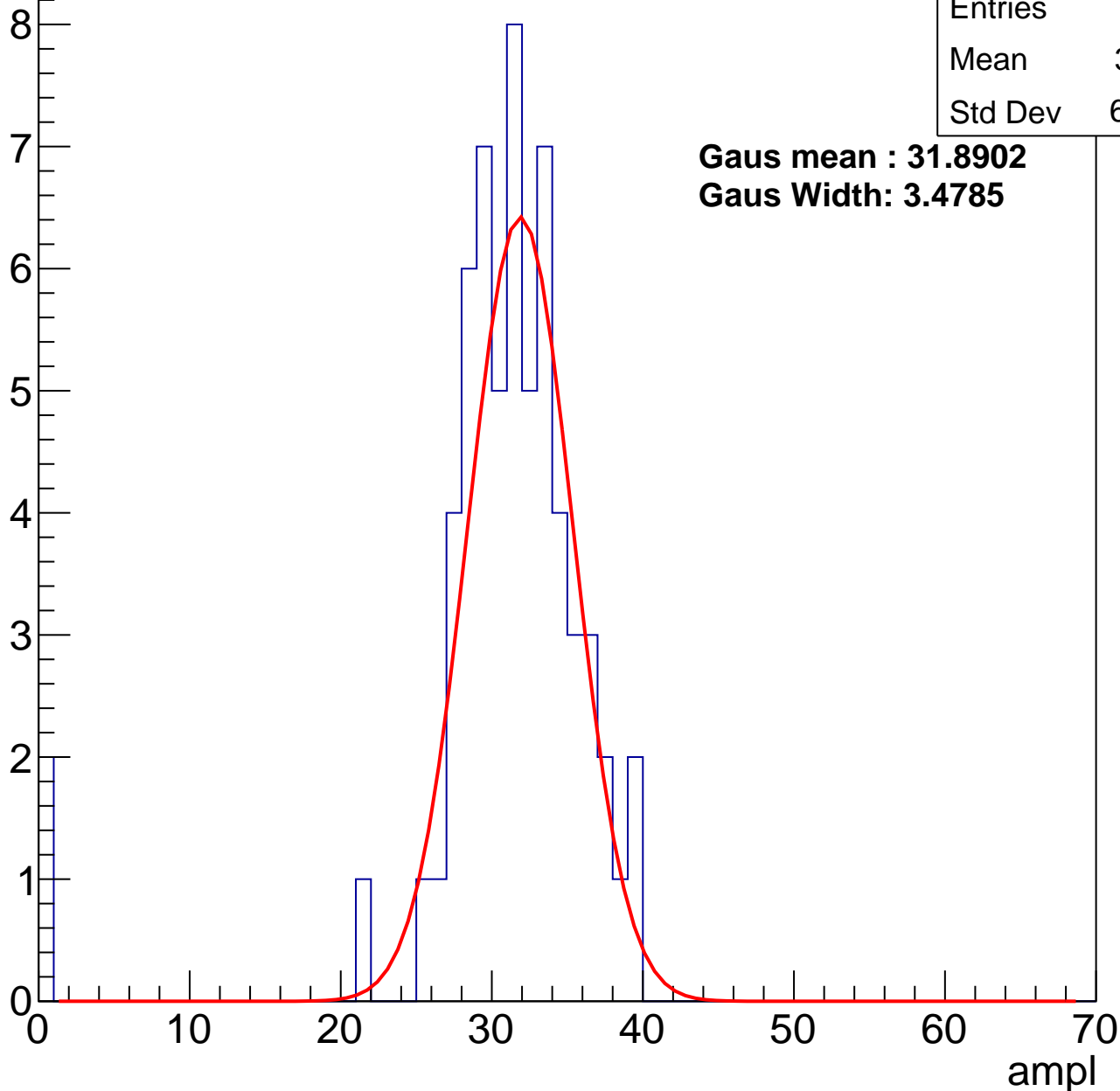
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	30.31
Std Dev	6.532

**Gaus mean : 31.8902**

**Gaus Width: 3.4785**



# B1L101S, U8-ch33, adc1

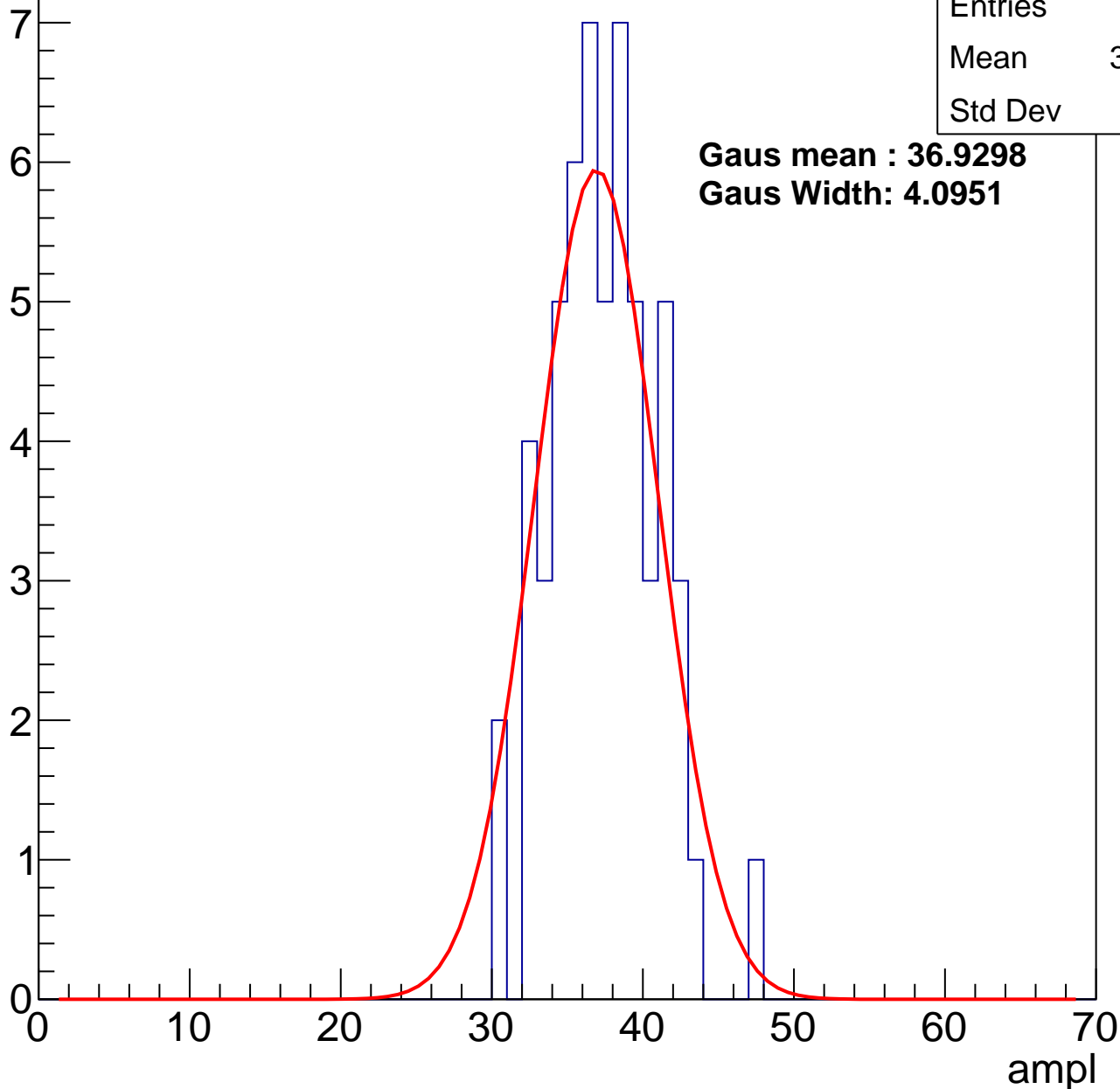
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	36.95
Std Dev	3.42

**Gaus mean : 36.9298**

**Gaus Width: 4.0951**



# B1L101S, U8-ch33, adc2

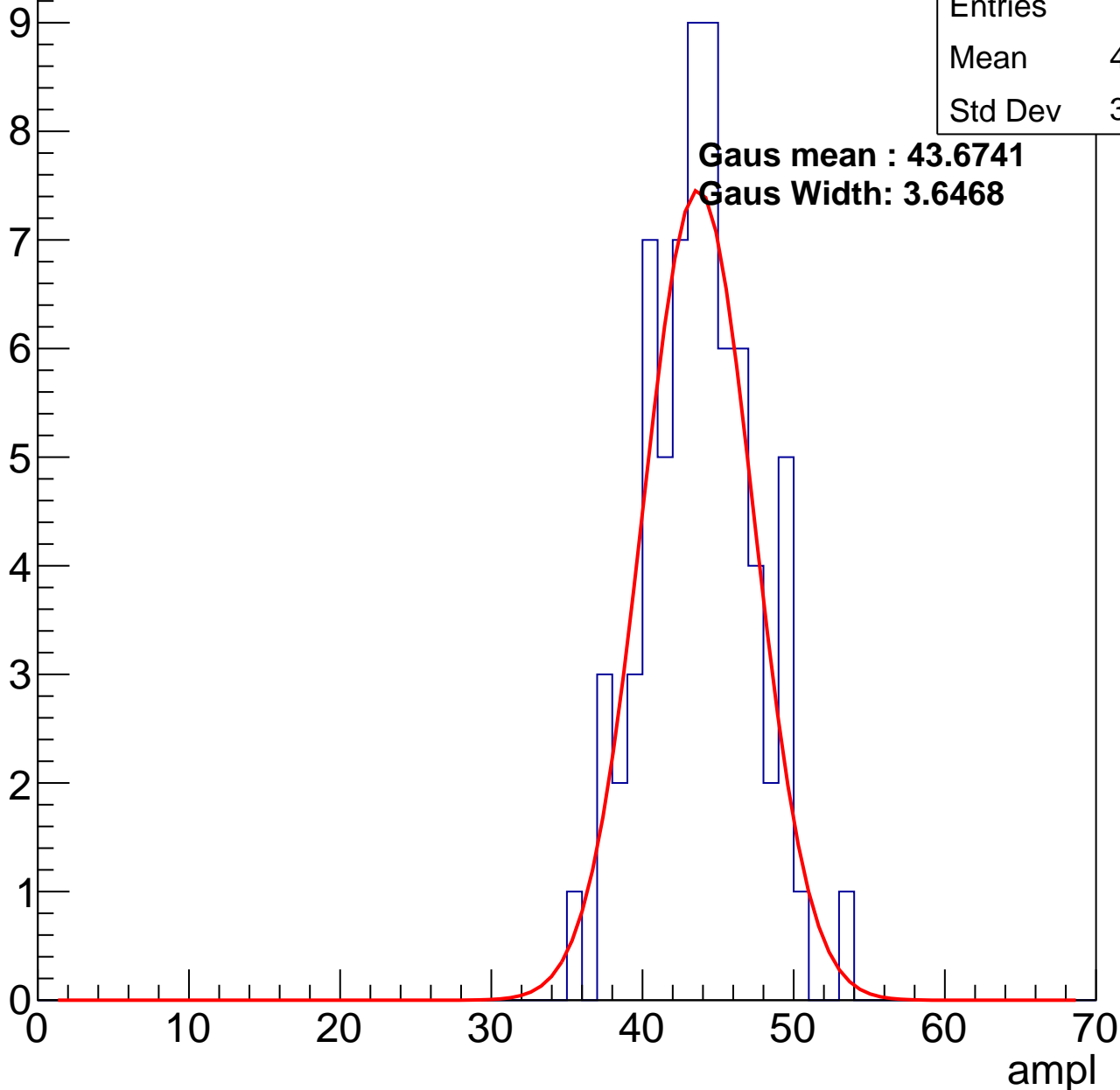
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	43.37
Std Dev	3.522

**Gaus mean : 43.6741**

**Gaus Width: 3.6468**



# B1L101S, U8-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	72
Mean	50.31
Std Dev	3.026

Entry

10

8

6

4

2

0

0

10

20

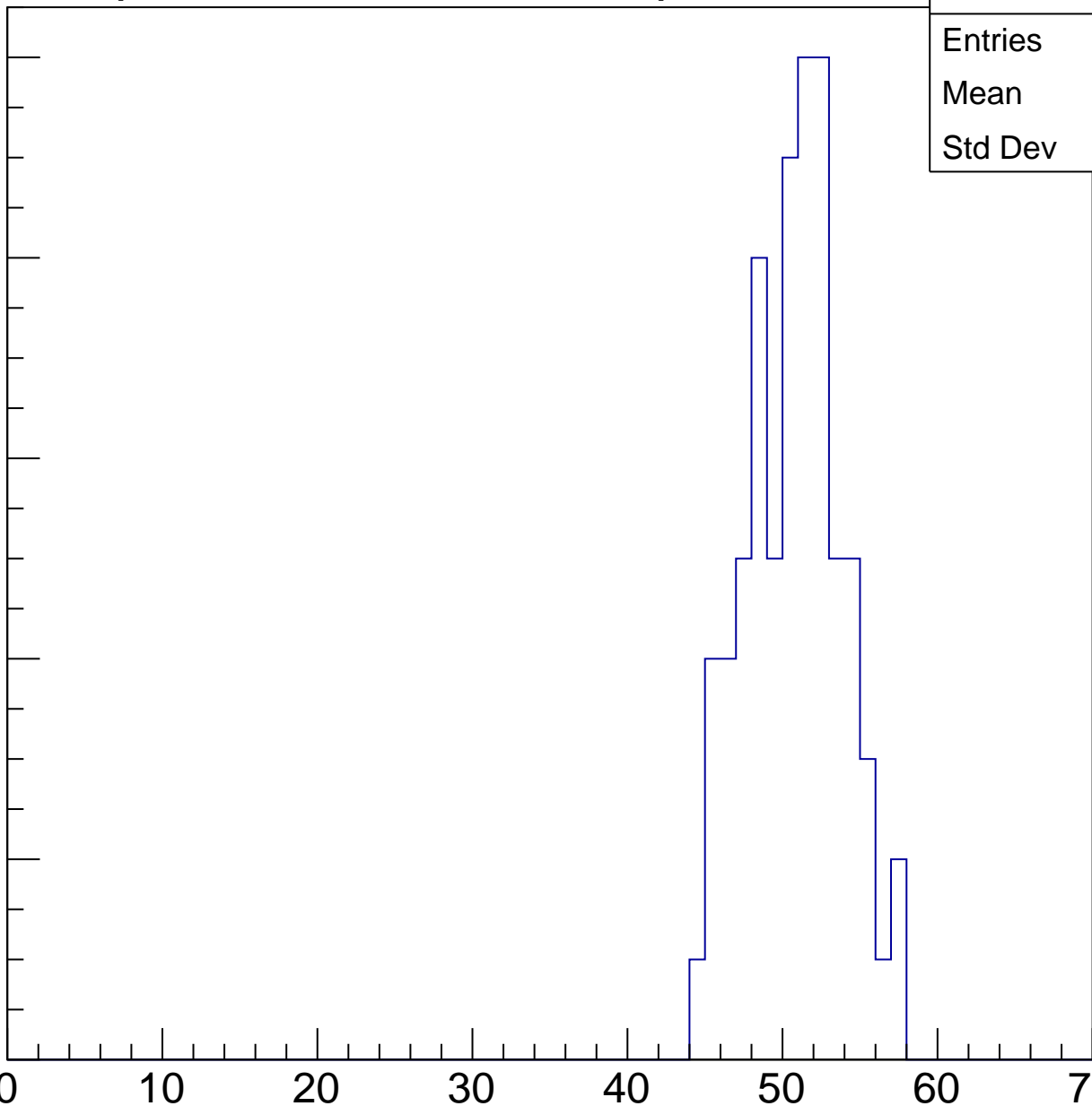
30

40

50

60

ampl

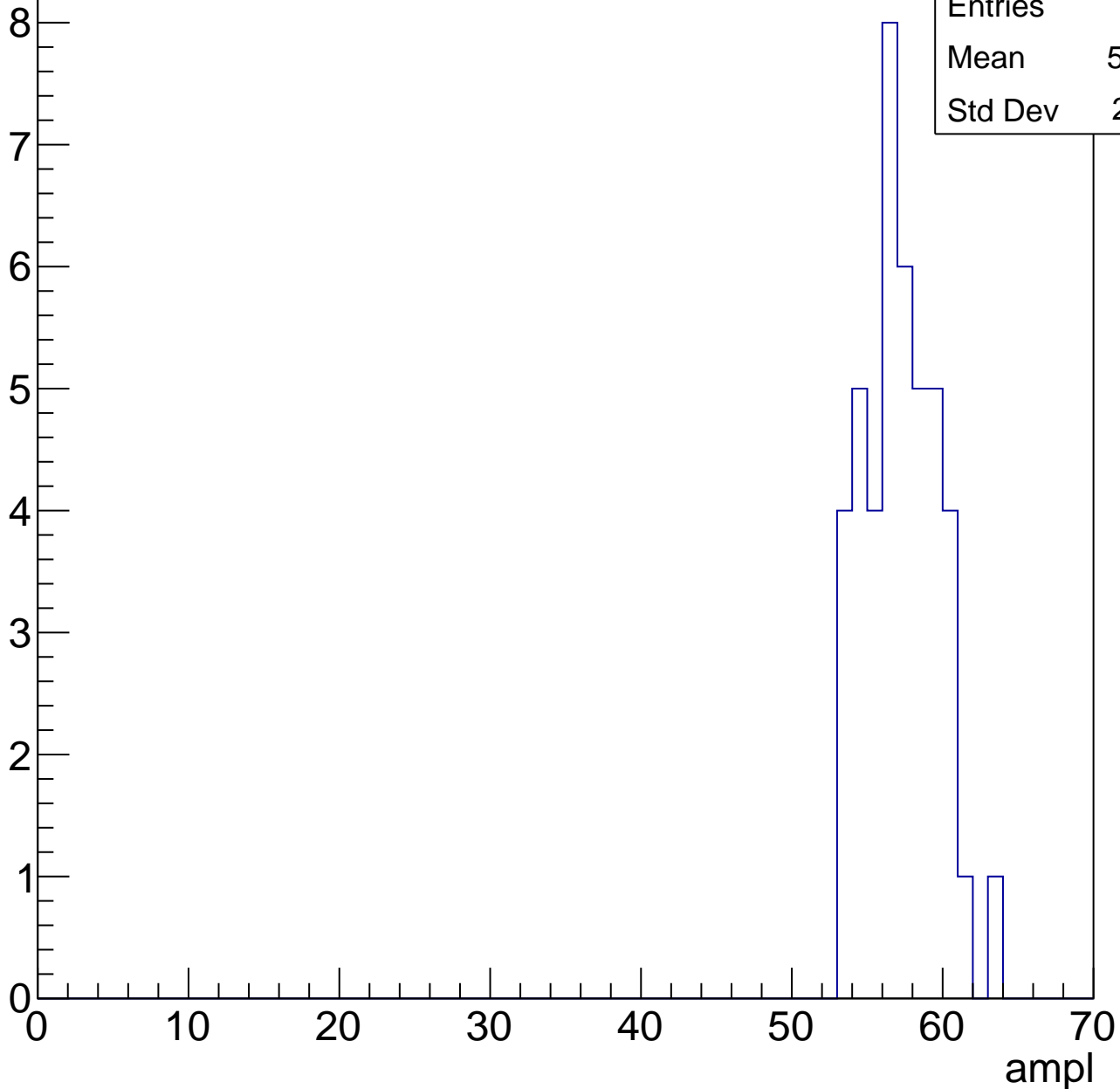


# B1L101S, U8-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	56.77
Std Dev	2.381

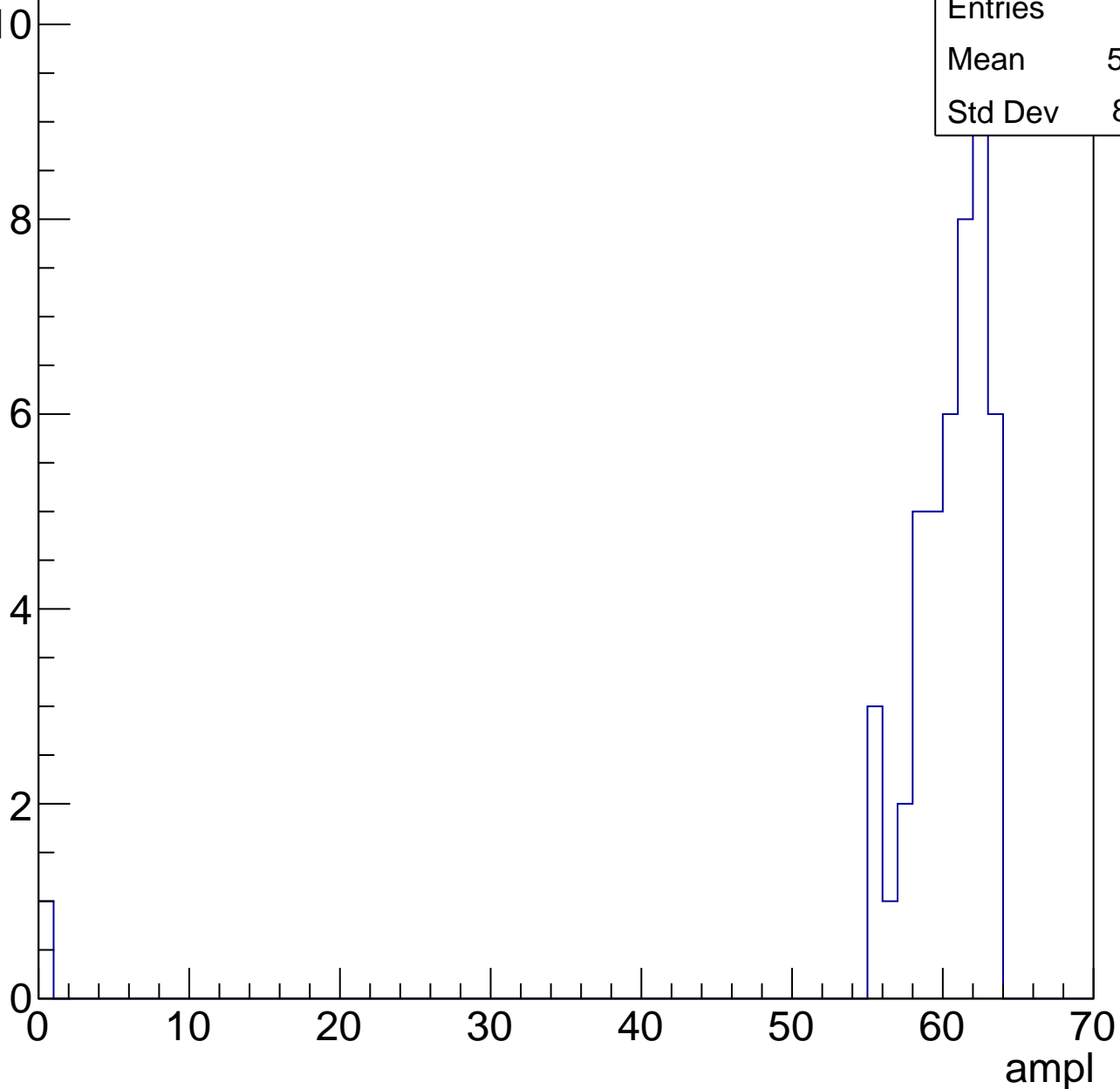


# B1L101S, U8-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	58.85
Std Dev	8.961



# B1L101S, U8-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U8-ch34, adc0

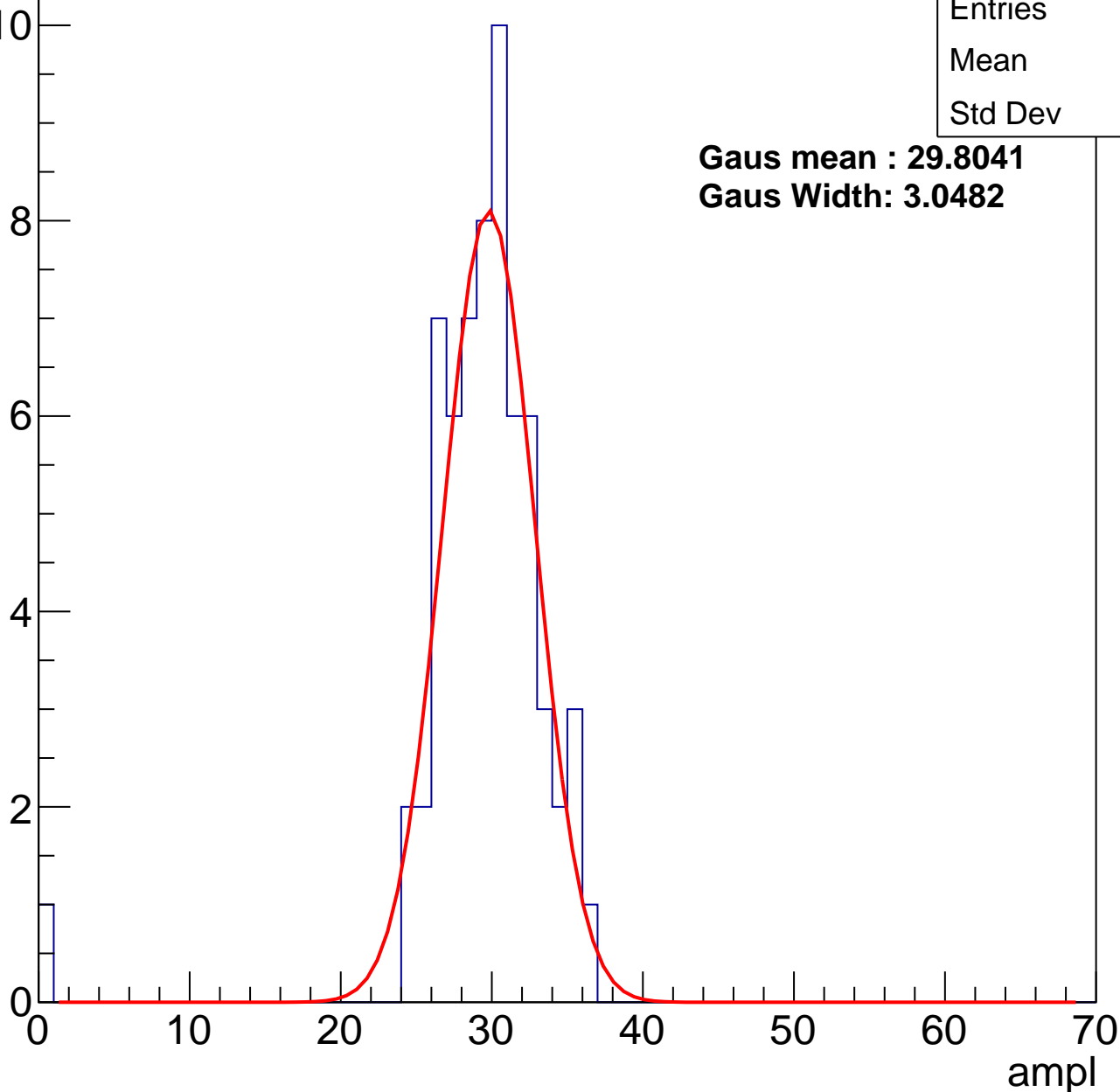
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	29
Std Dev	4.61

**Gaus mean : 29.8041**

**Gaus Width: 3.0482**



# B1L101S, U8-ch34, adc1

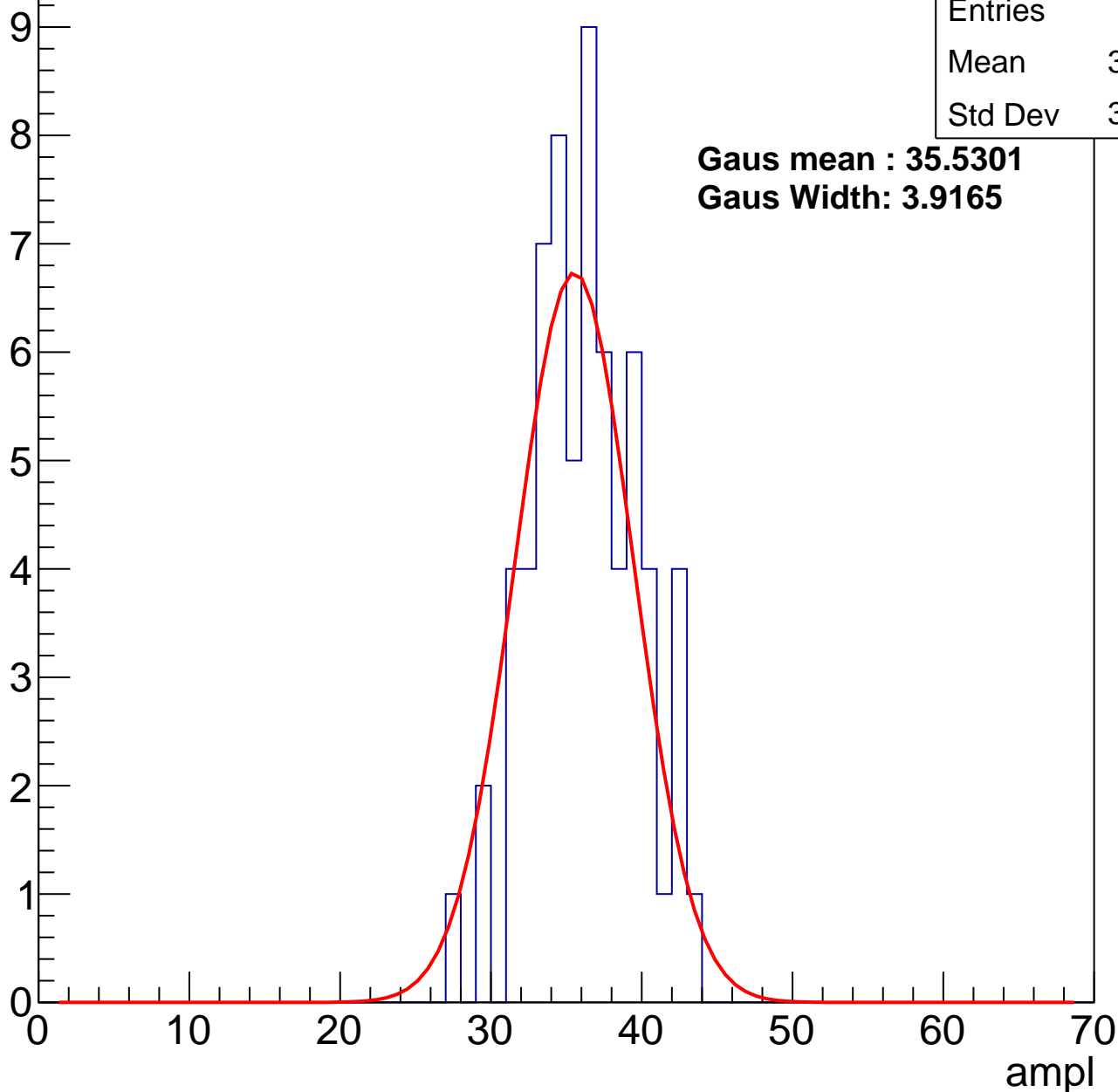
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	35.74
Std Dev	3.474

**Gaus mean : 35.5301**

**Gaus Width: 3.9165**



# B1L101S, U8-ch34, adc2

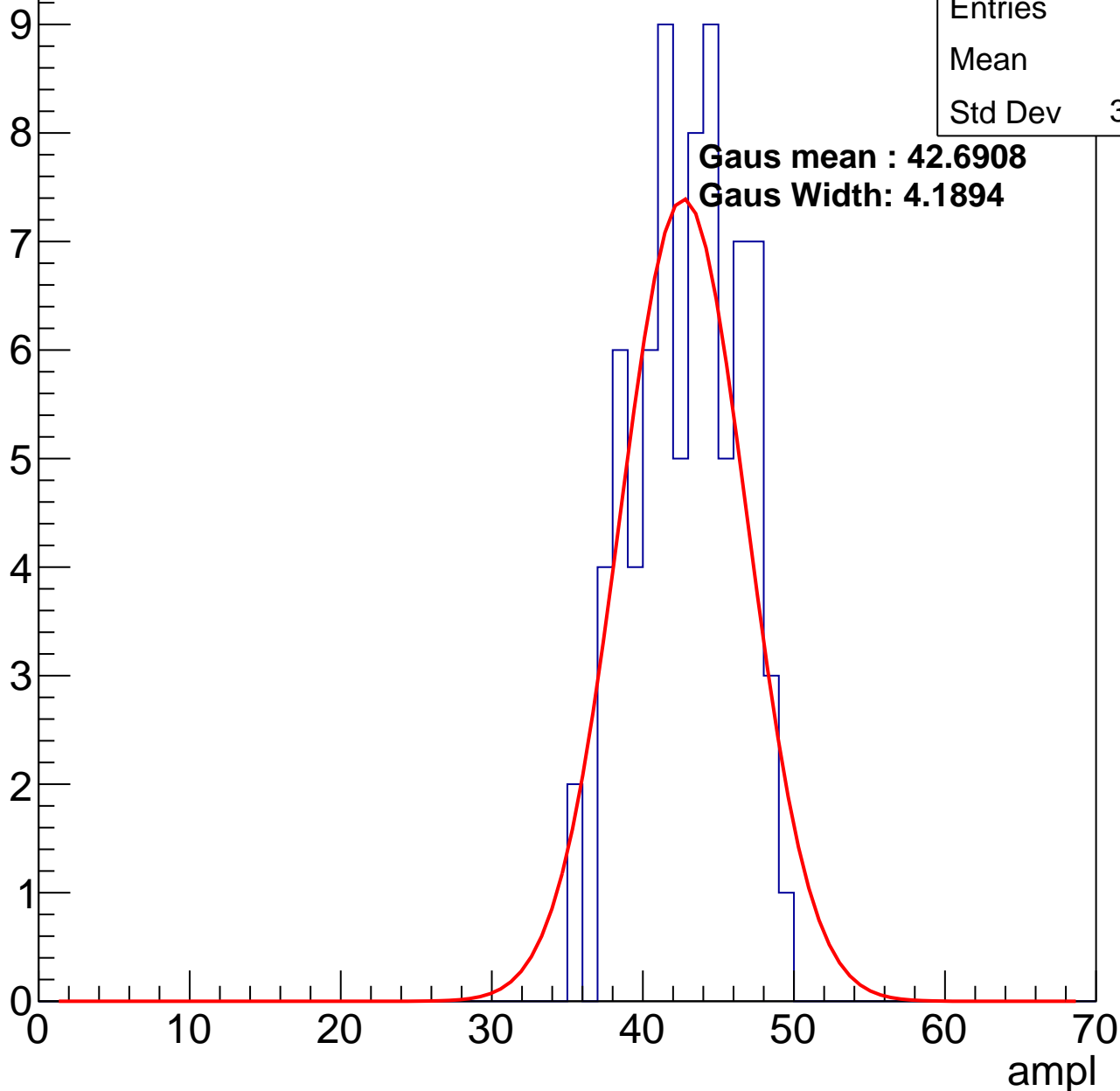
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	42.5
Std Dev	3.397

**Gaus mean : 42.6908**

**Gaus Width: 4.1894**

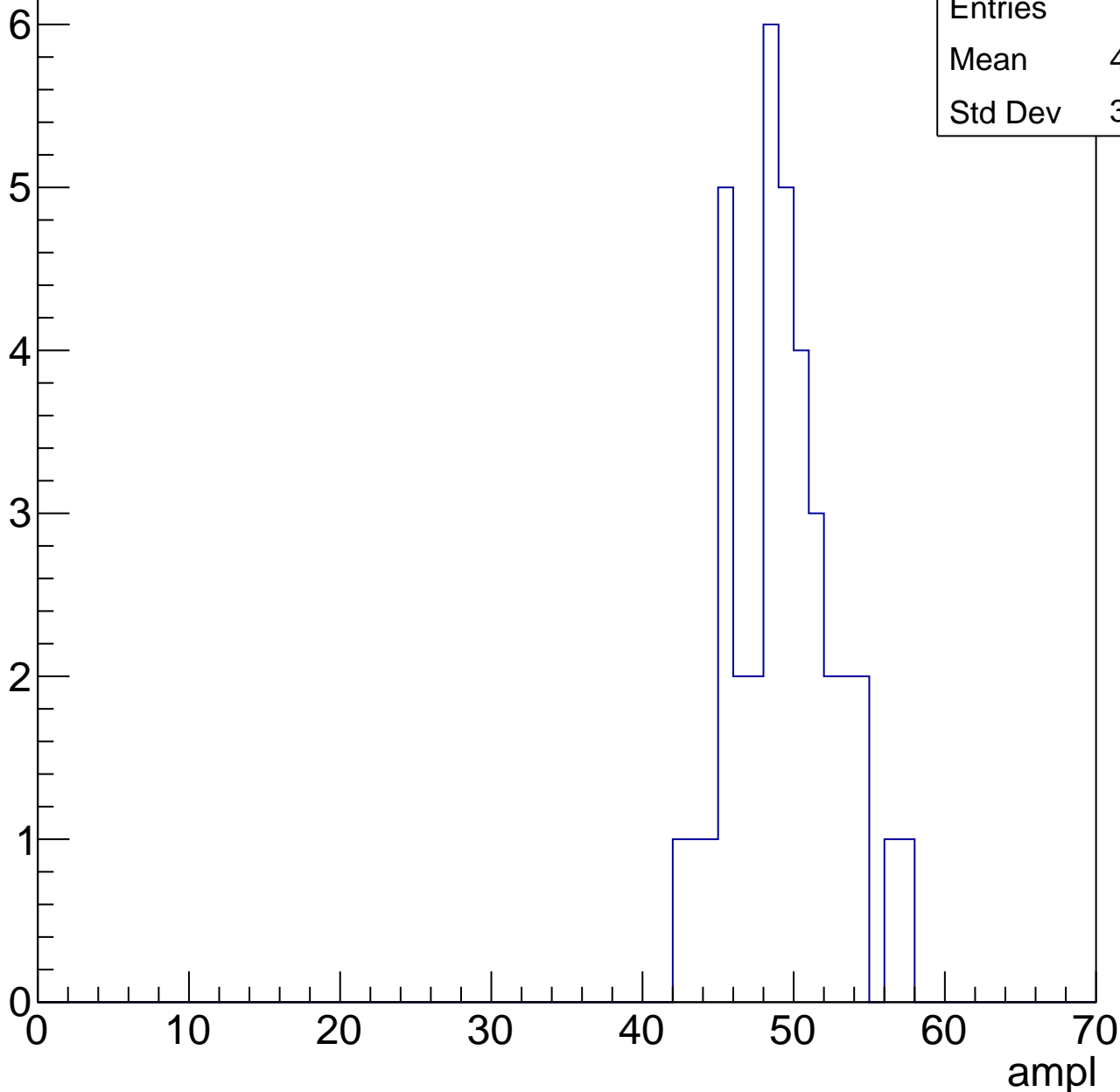


# B1L101S, U8-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	38
Mean	48.87
Std Dev	3.443

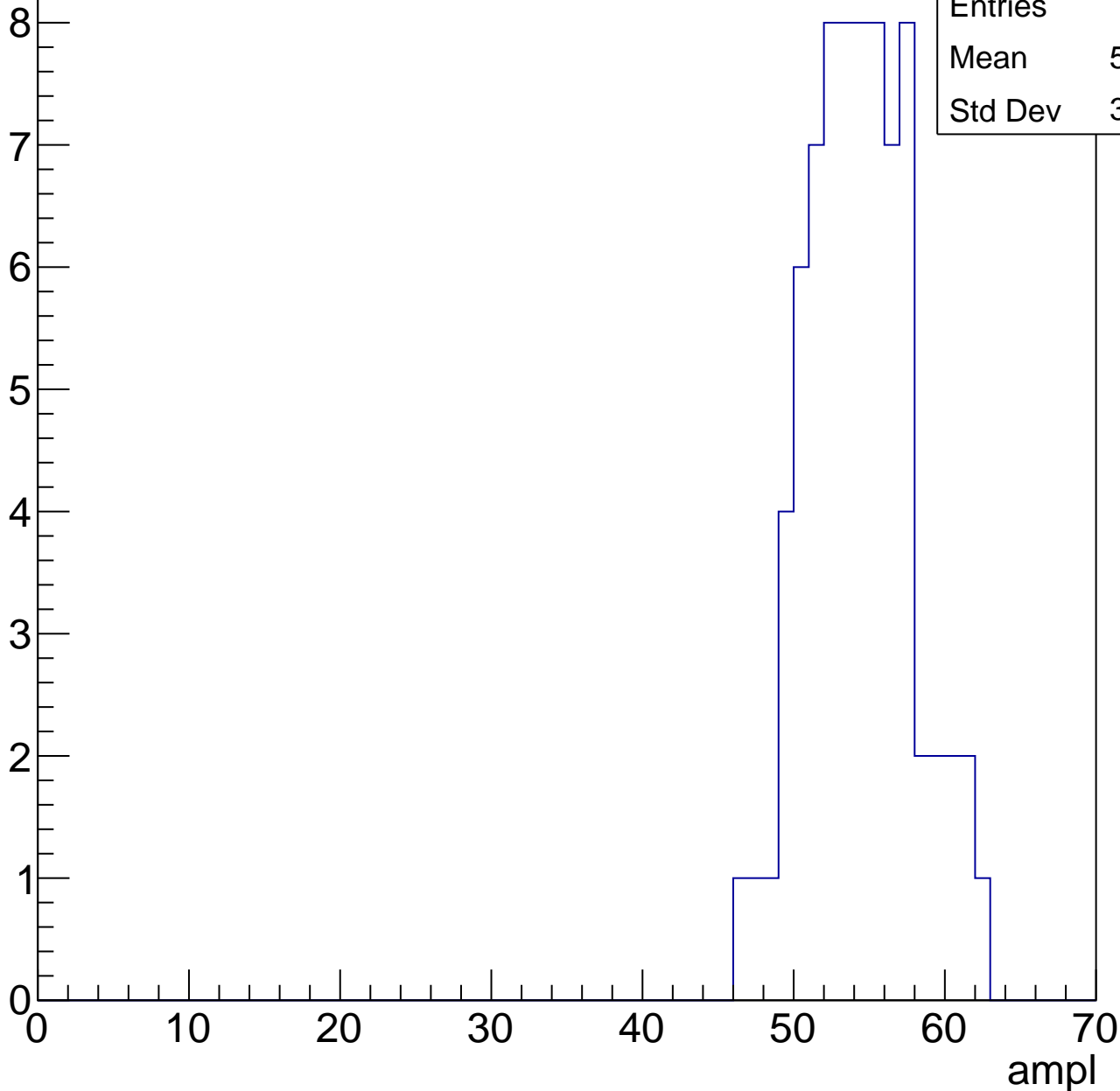


# B1L101S, U8-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	53.84
Std Dev	3.384



# B1L101S, U8-ch34, adc5

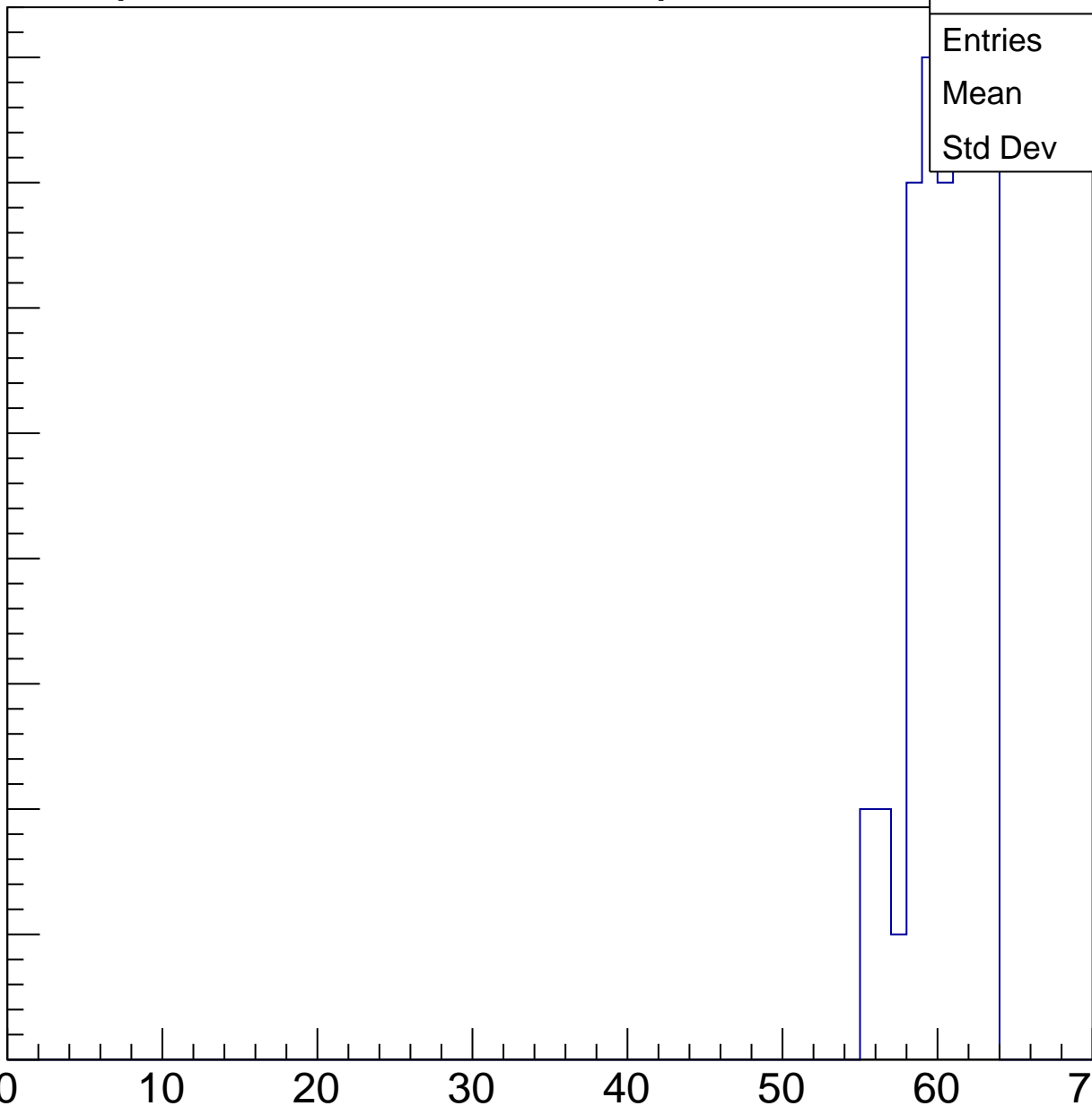
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	60.1
Std Dev	2.163

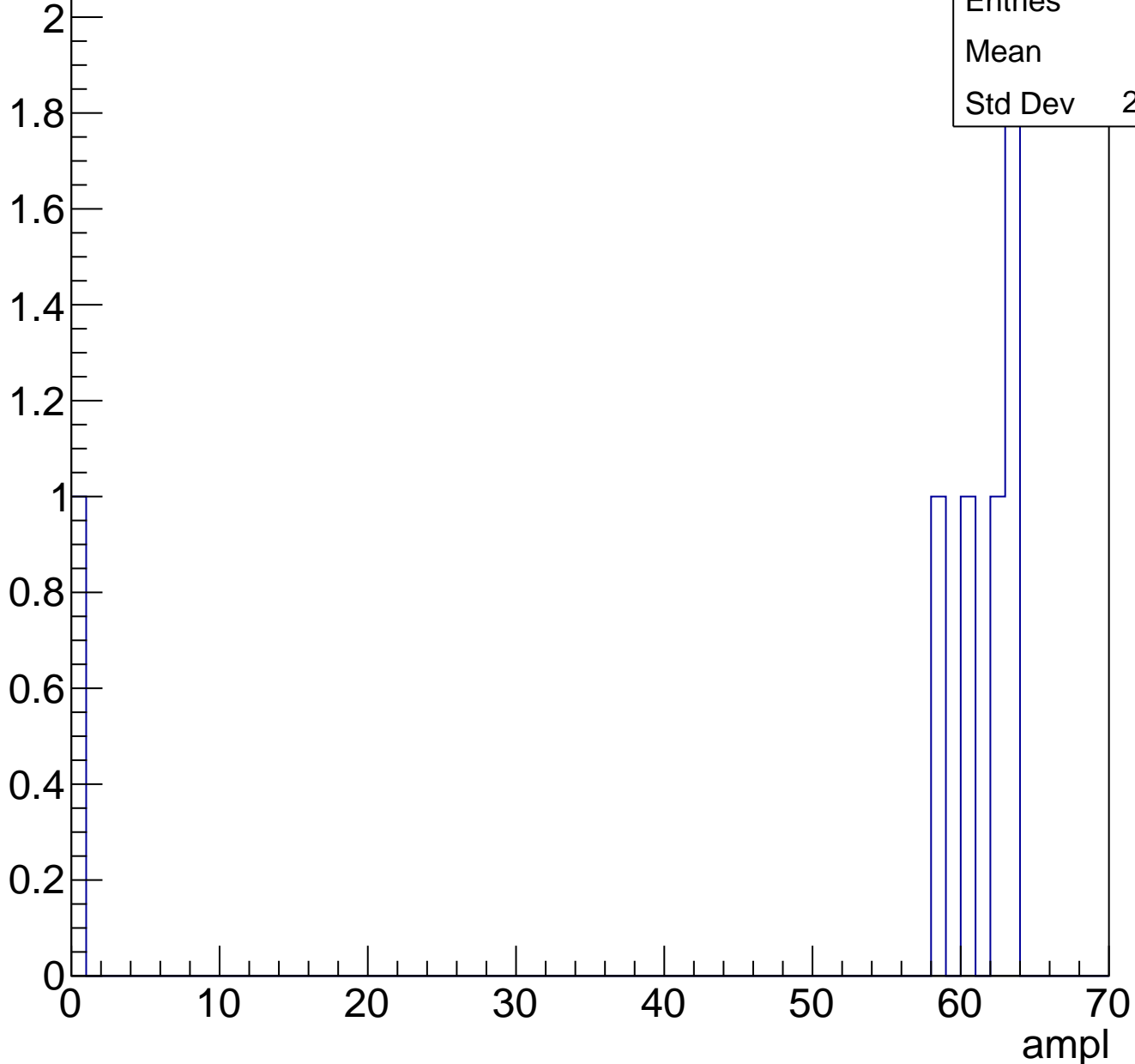
ampl



# B1L101S, U8-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	23
Std Dev	0

ampl

# B1L101S, U8-ch35, adc0

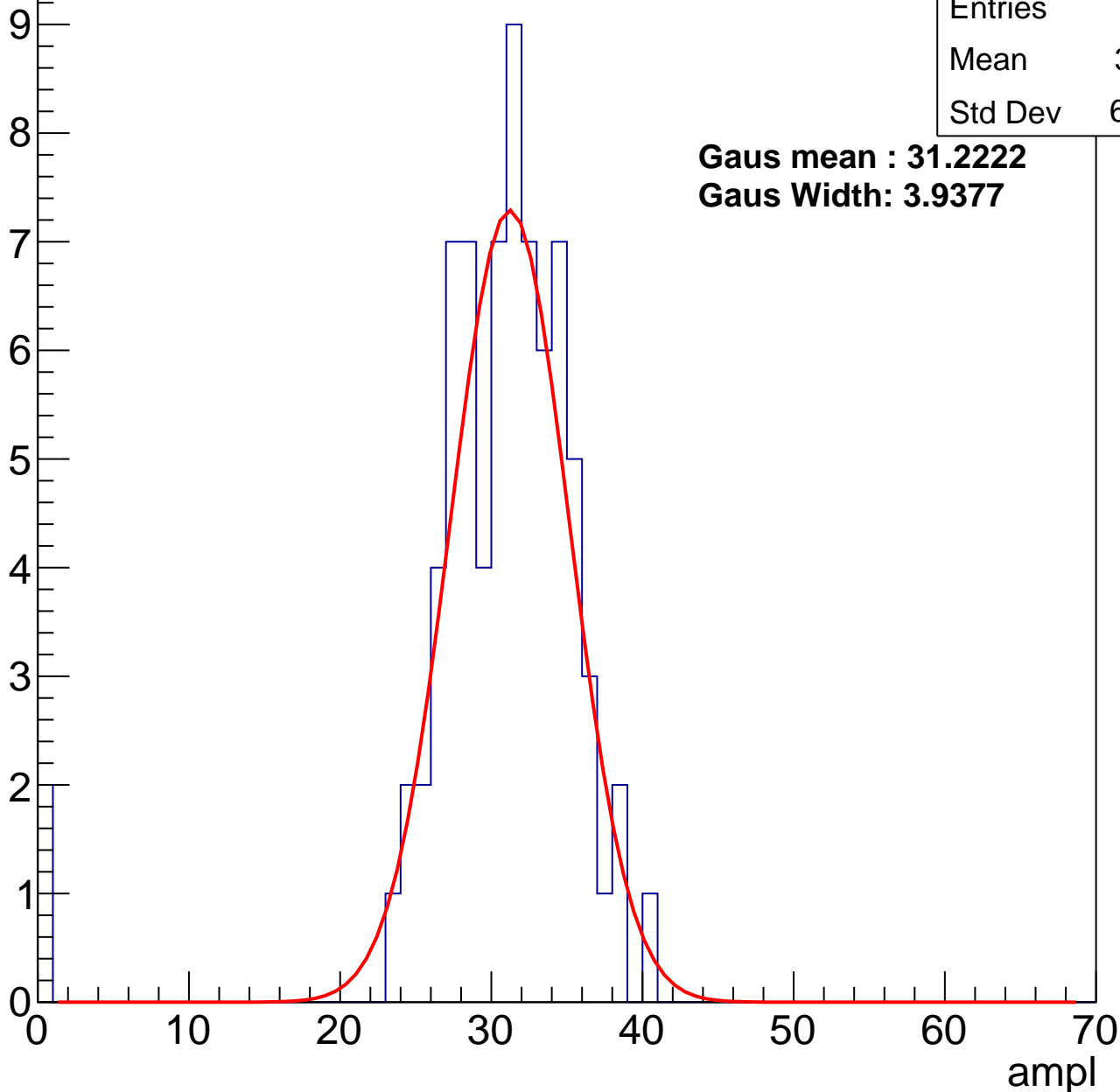
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	30.01
Std Dev	6.076

**Gaus mean : 31.2222**

**Gaus Width: 3.9377**



# B1L101S, U8-ch35, adc1

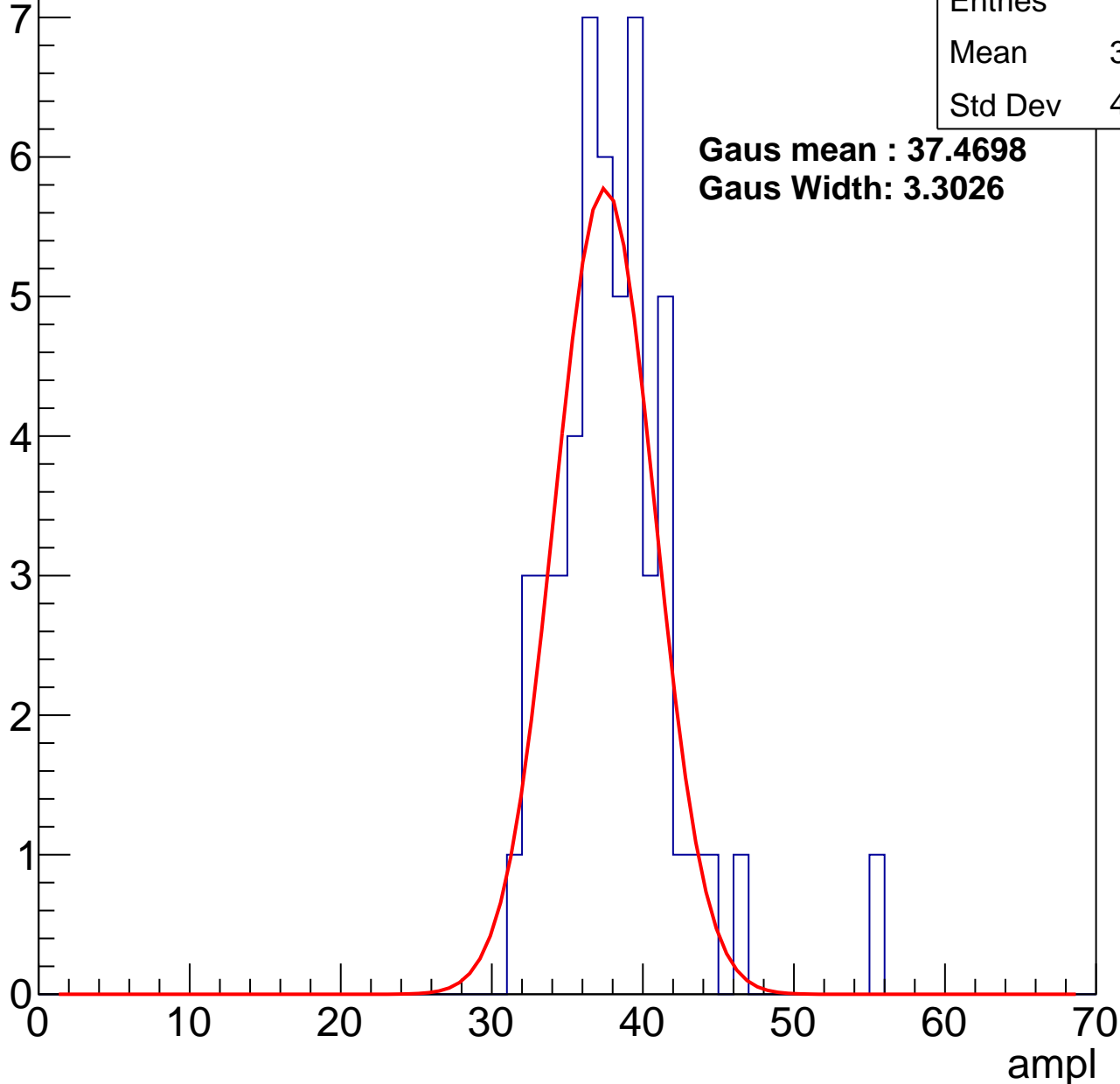
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	37.69
Std Dev	4.017

**Gaus mean : 37.4698**

**Gaus Width: 3.3026**



# B1L101S, U8-ch35, adc2

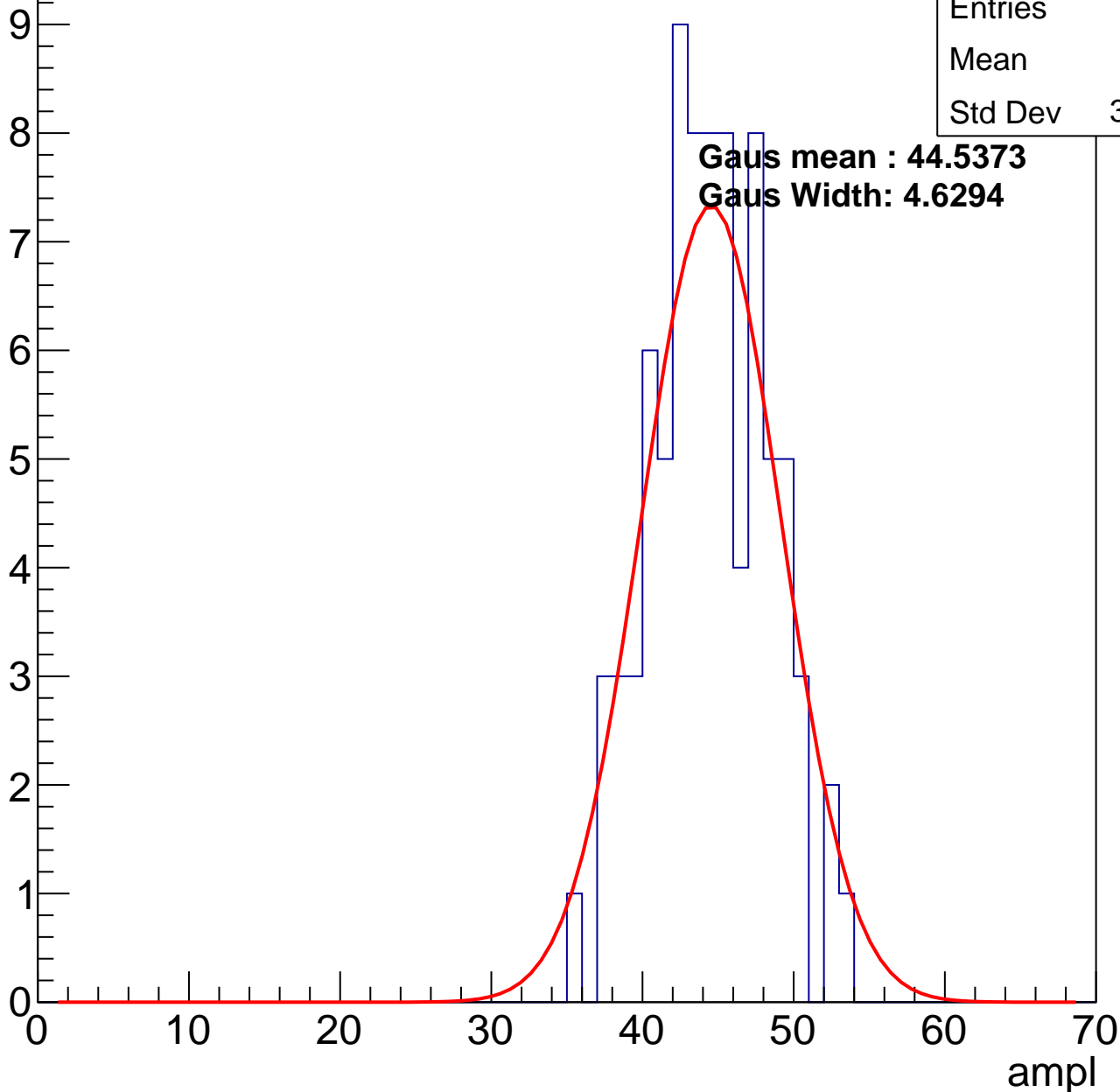
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	44
Std Dev	3.848

**Gaus mean : 44.5373**

**Gaus Width: 4.6294**

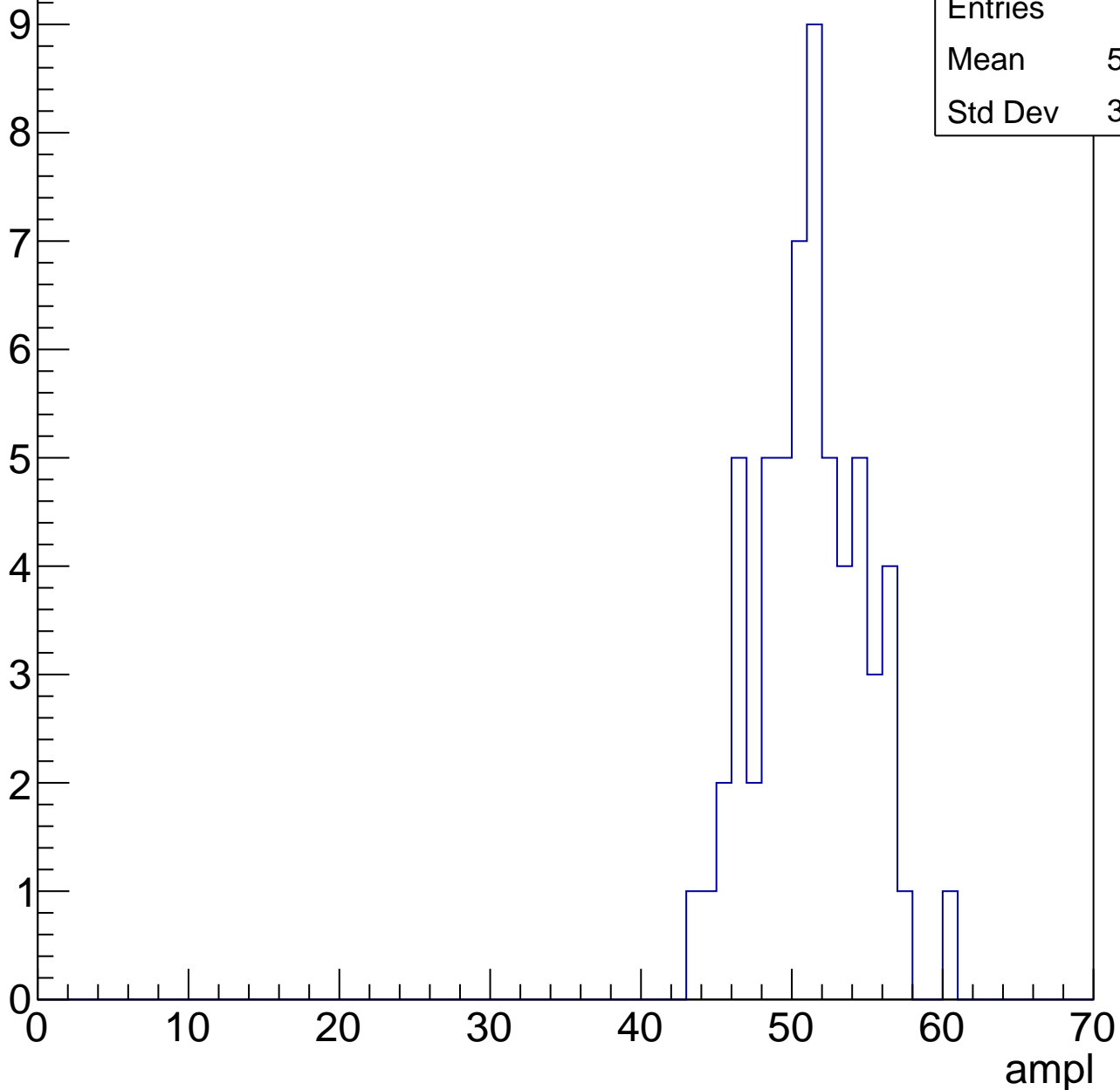


# B1L101S, U8-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	50.72
Std Dev	3.512

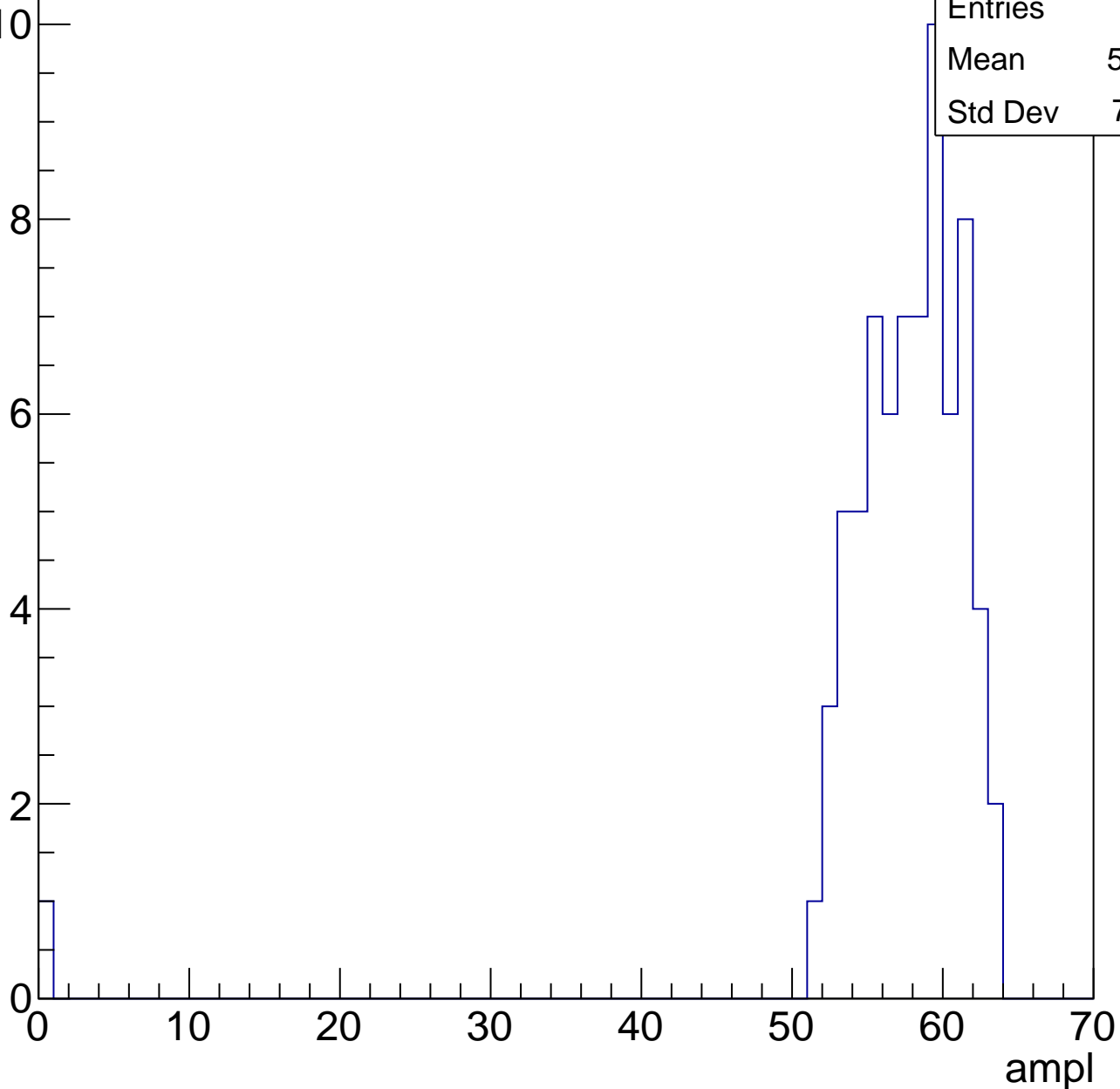


# B1L101S, U8-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	56.67
Std Dev	7.371

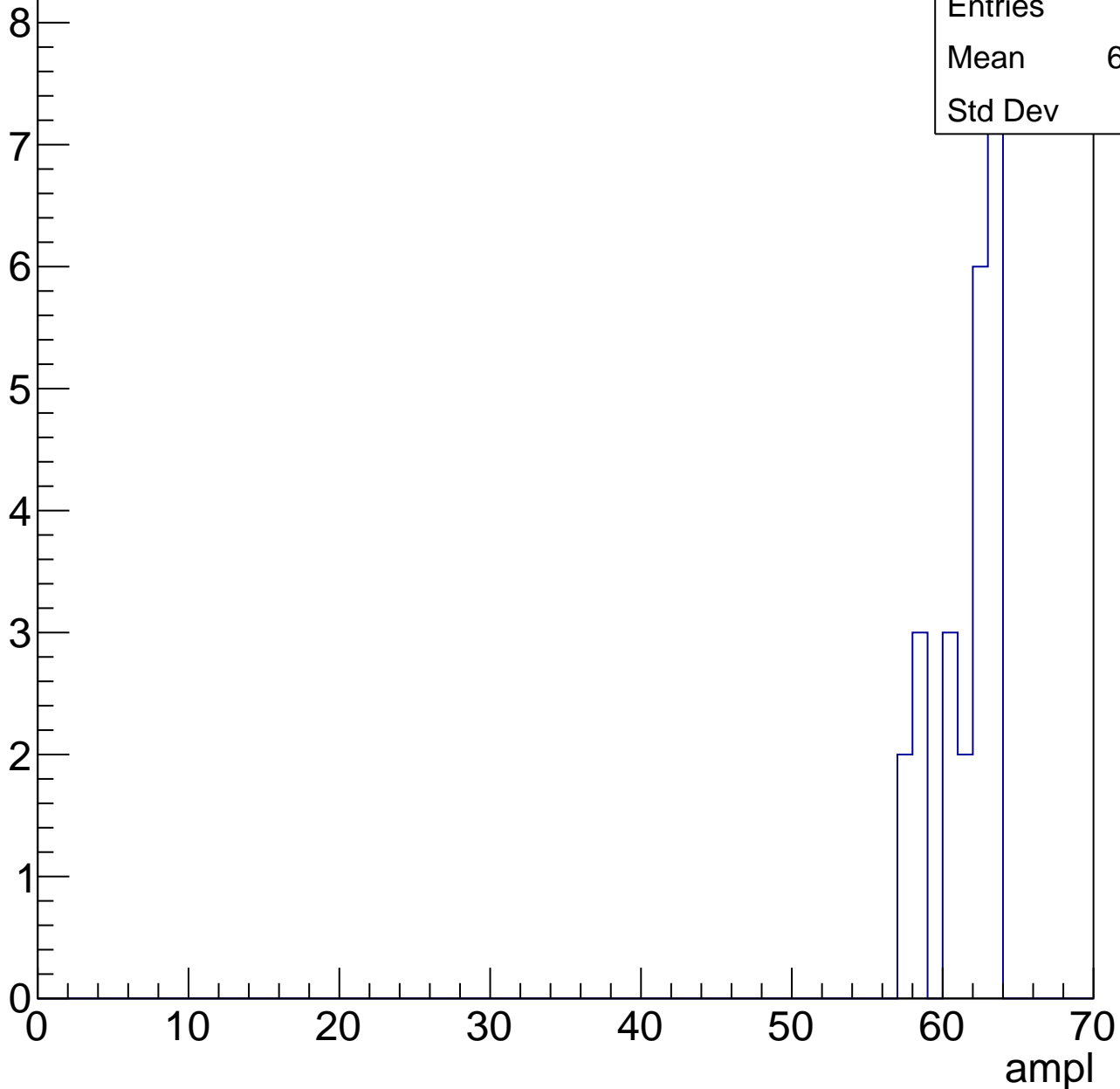


# B1L101S, U8-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	24
Mean	61.08
Std Dev	2.04



# B1L101S, U8-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L101S, U8-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U8-ch36, adc0

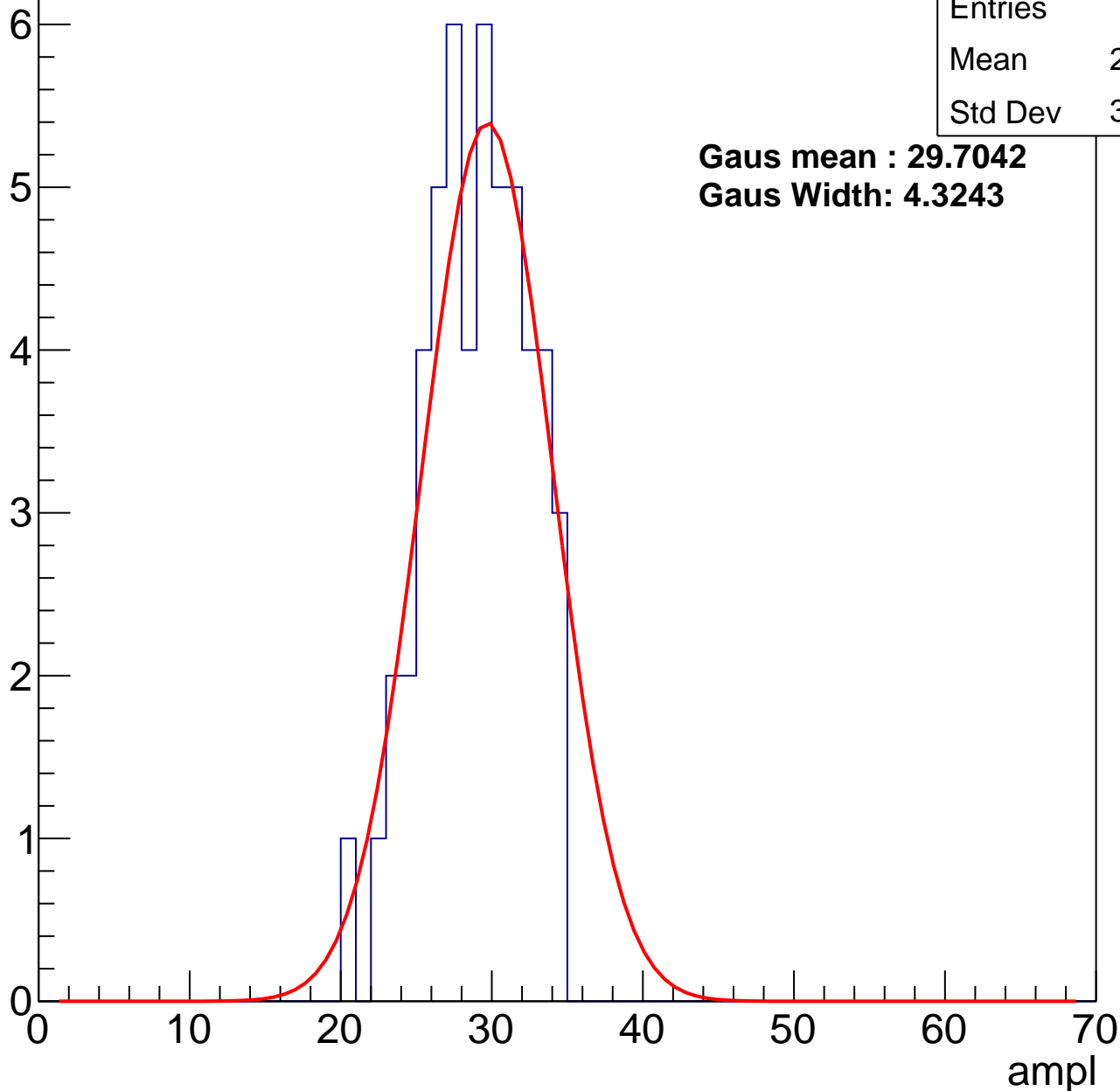
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	28.48
Std Dev	3.325

**Gaus mean : 29.7042**

**Gaus Width: 4.3243**



# B1L101S, U8-ch36, adc1

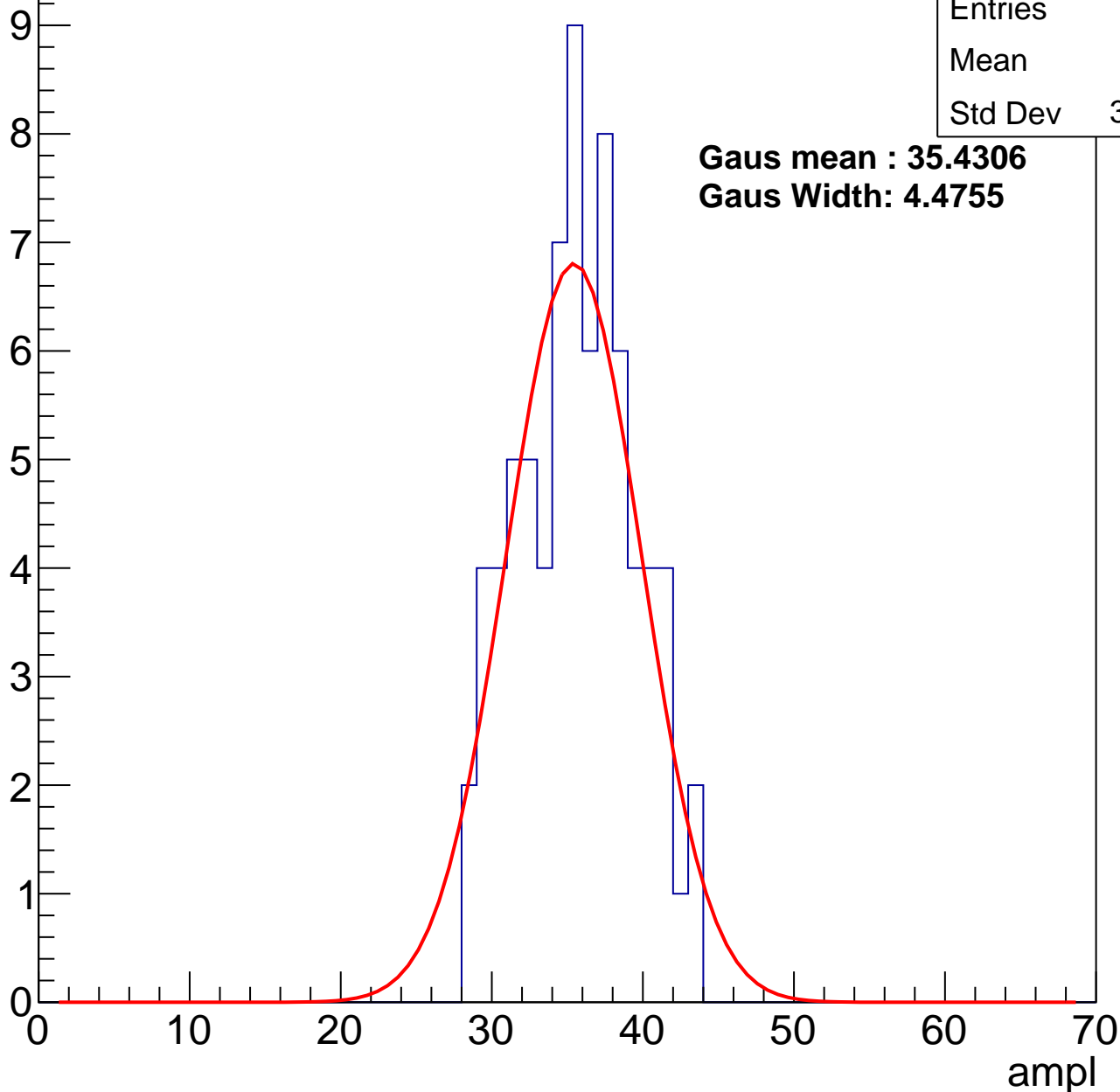
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	35.2
Std Dev	3.767

**Gaus mean : 35.4306**

**Gaus Width: 4.4755**



# B1L101S, U8-ch36, adc2

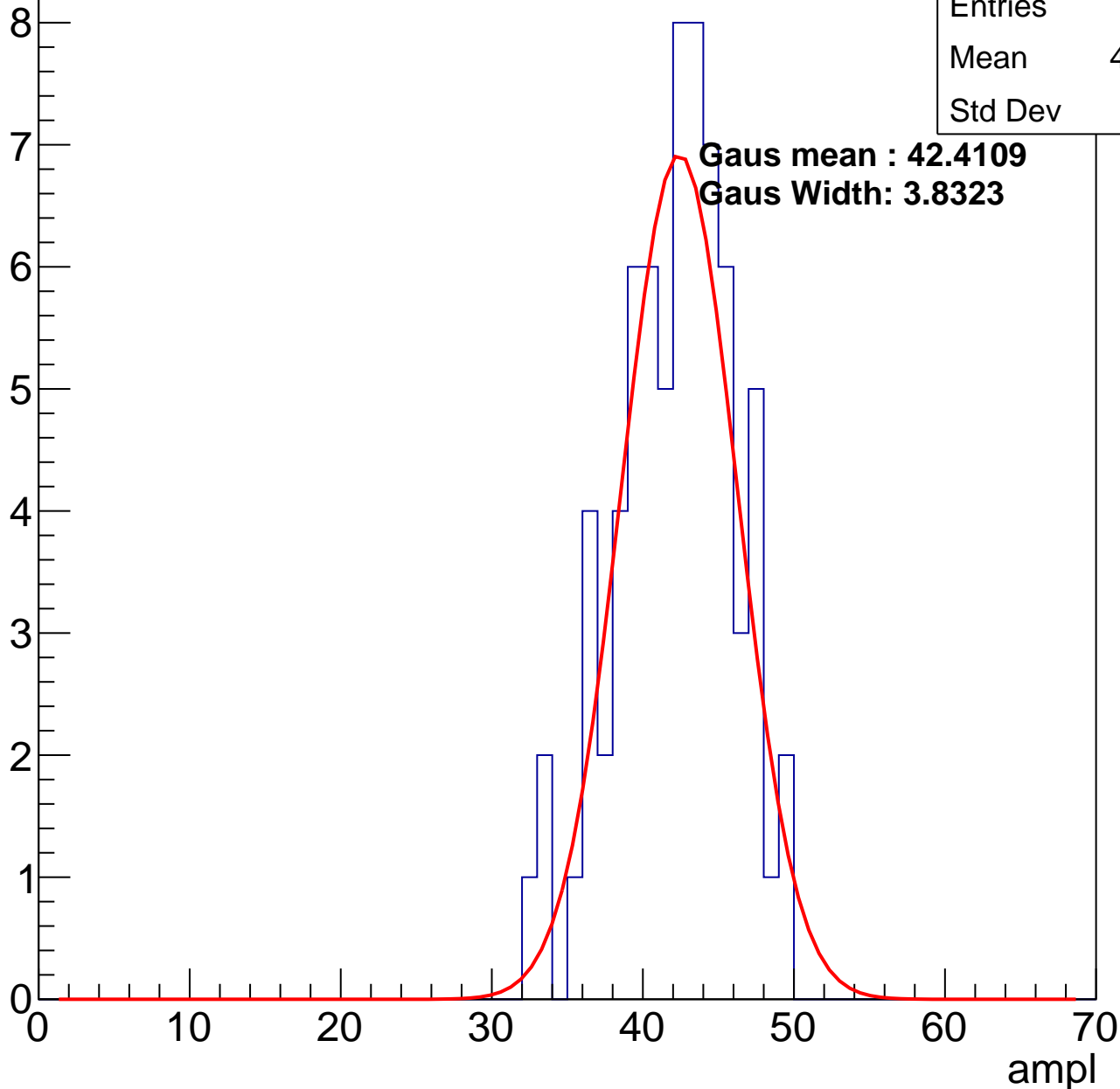
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	41.68
Std Dev	3.83

**Gaus mean : 42.4109**

**Gaus Width: 3.8323**

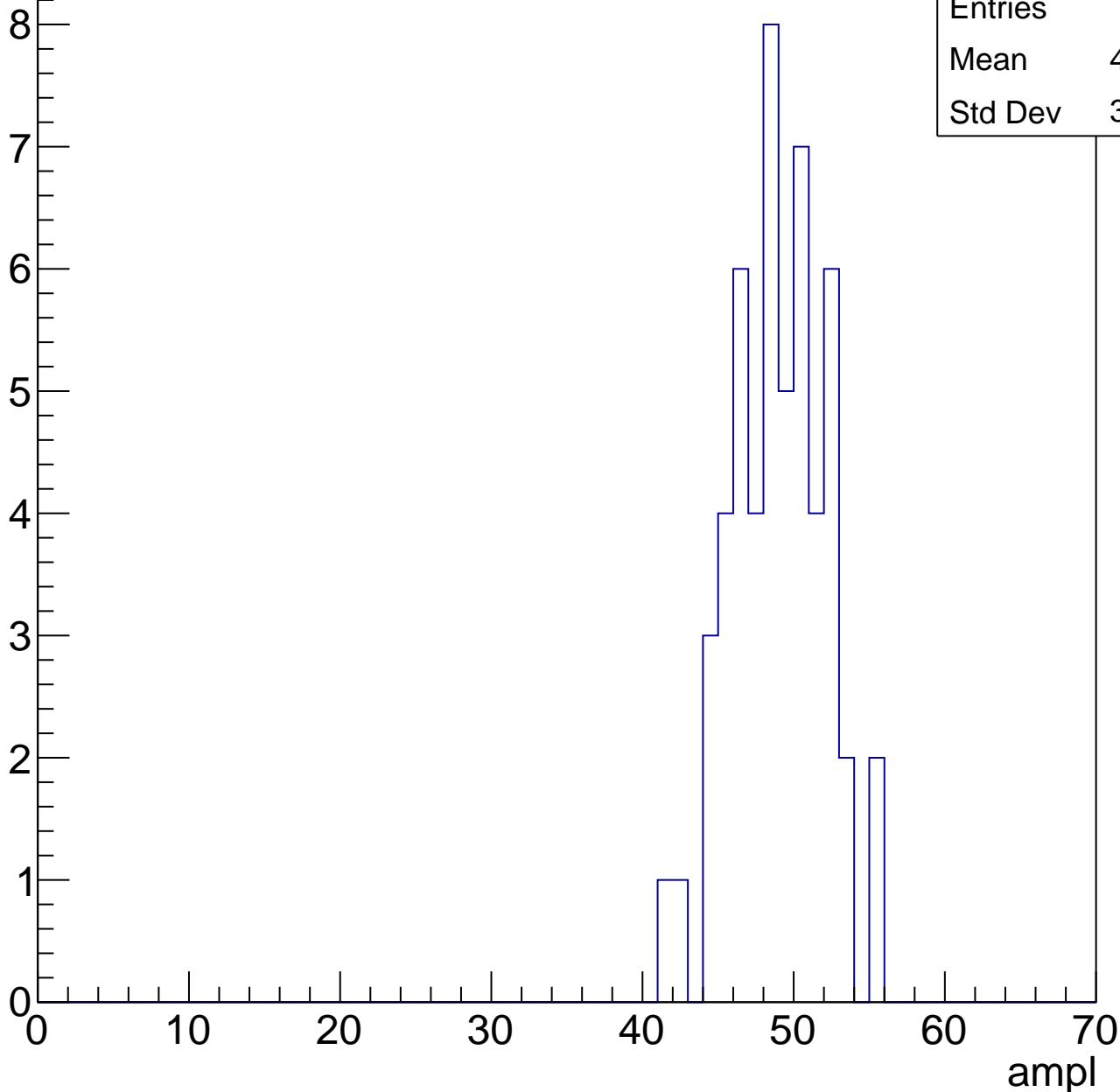


# B1L101S, U8-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	48.49
Std Dev	3.063

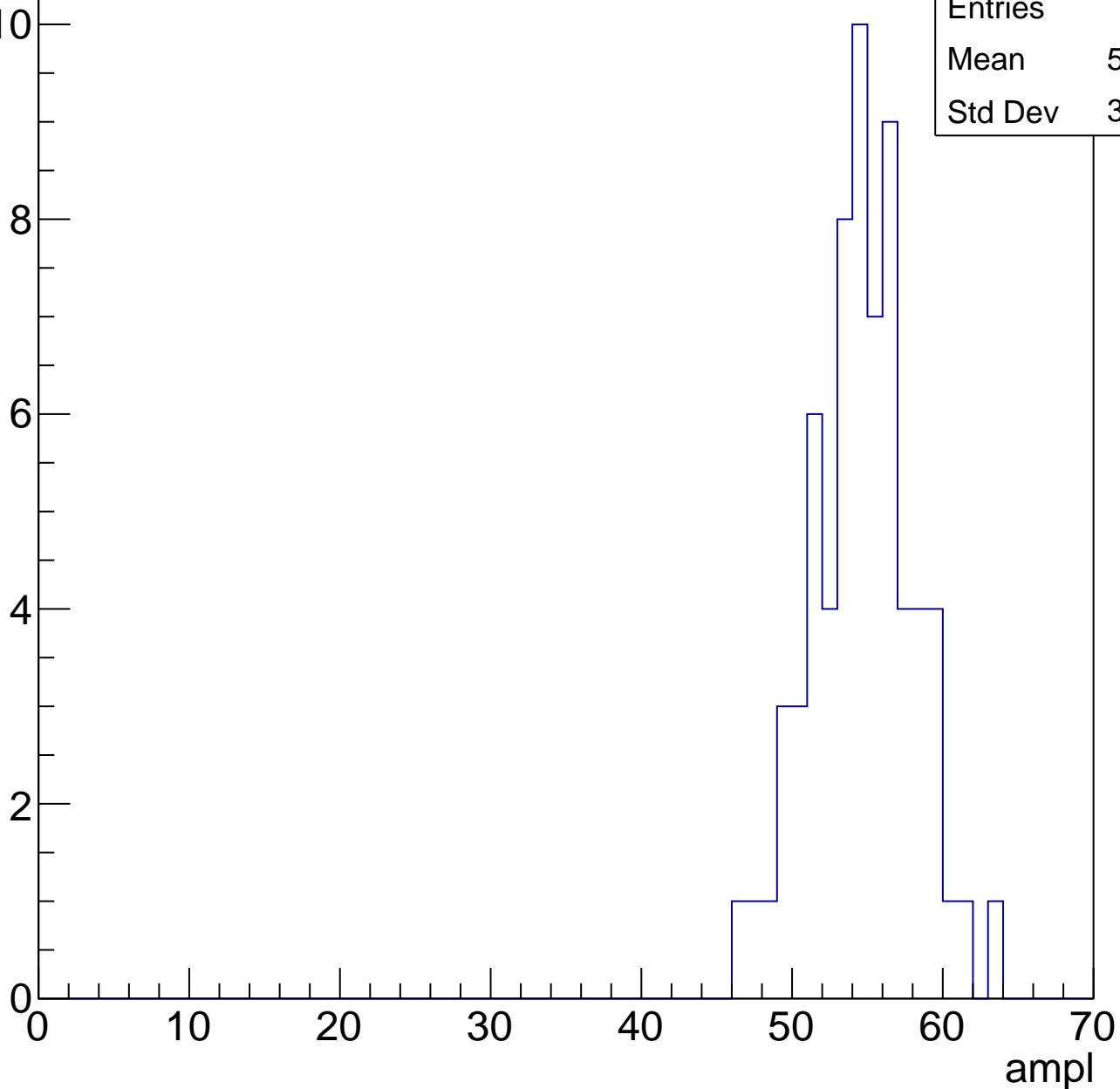


# B1L101S, U8-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	54.19
Std Dev	3.335



# B1L101S, U8-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

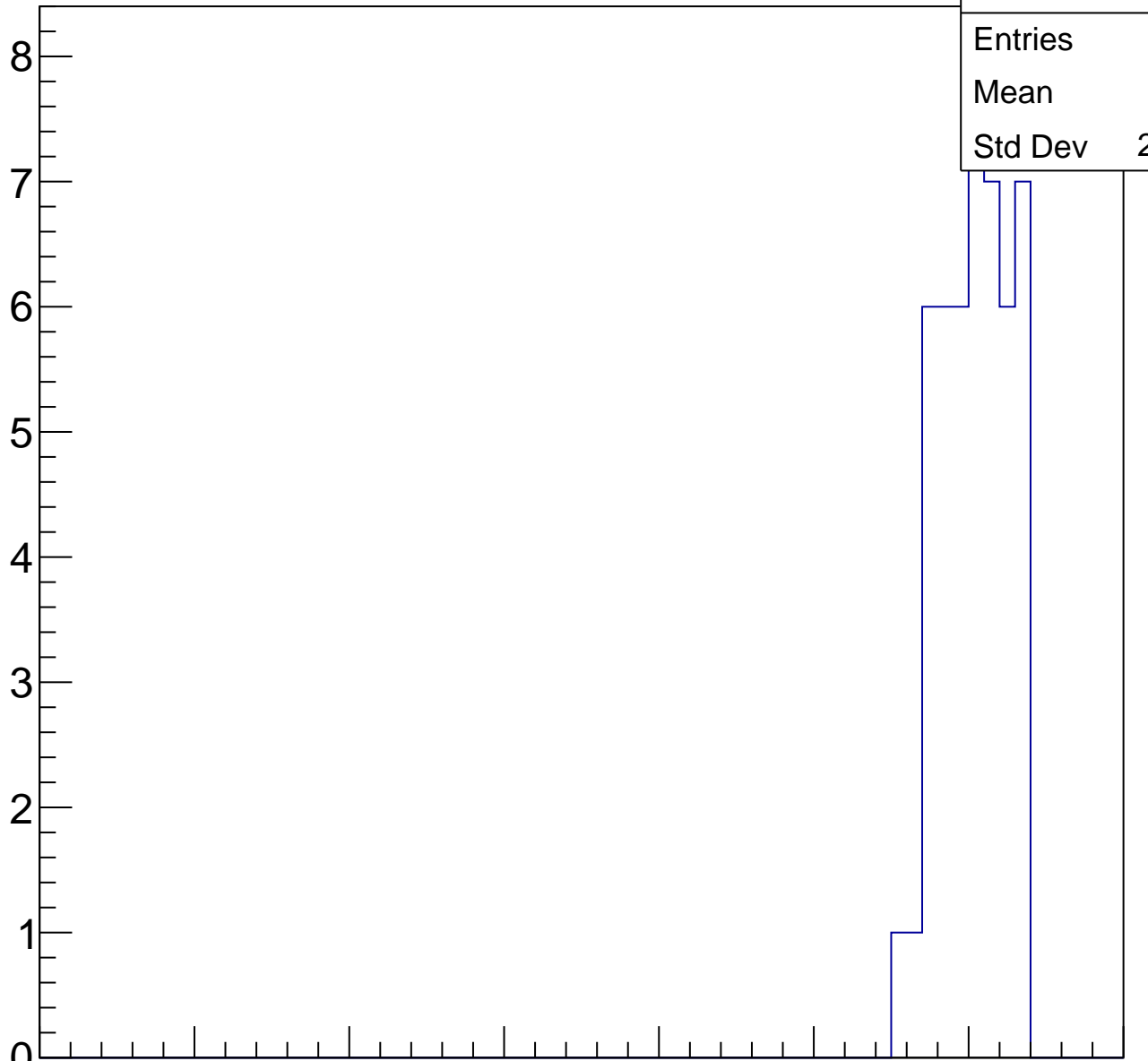
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	59.9
Std Dev	2.133

ampl

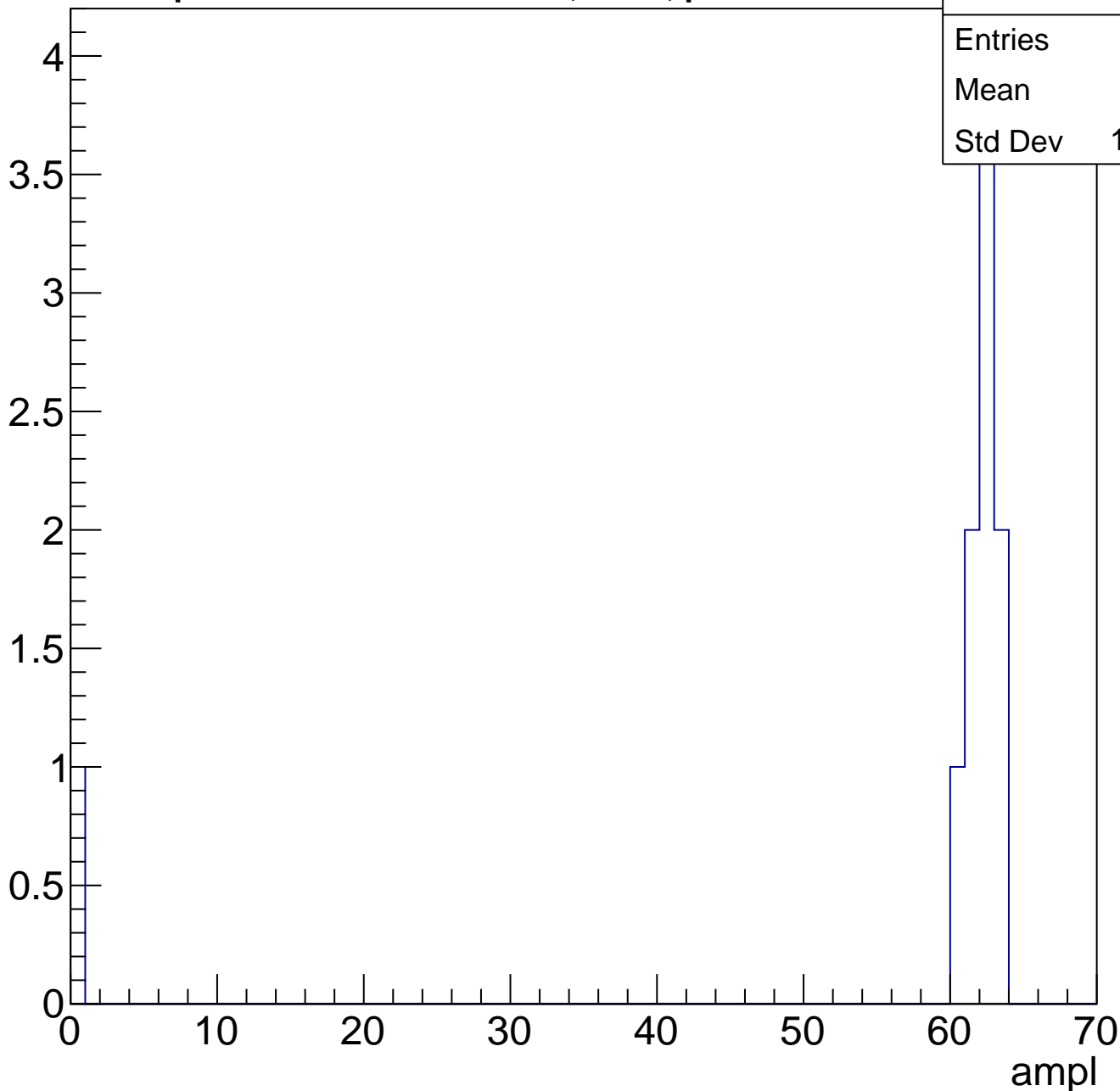
0 10 20 30 40 50 60 70



# B1L101S, U8-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	10
Mean	55.6
Std Dev	18.55



# B1L101S, U8-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

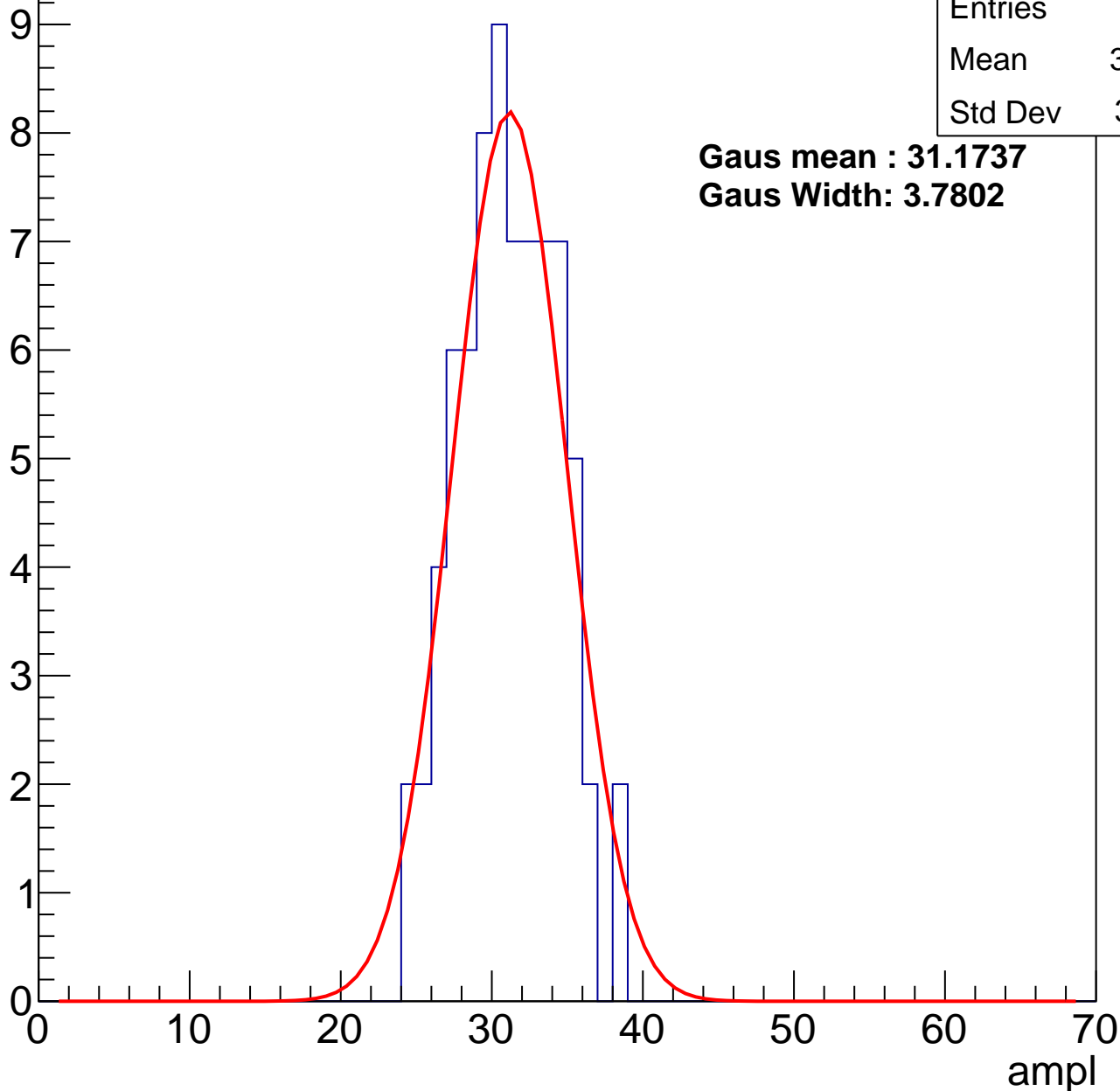


Entries	1
Mean	0
Std Dev	0

# B1L101S, U8-ch37, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch37, adc1

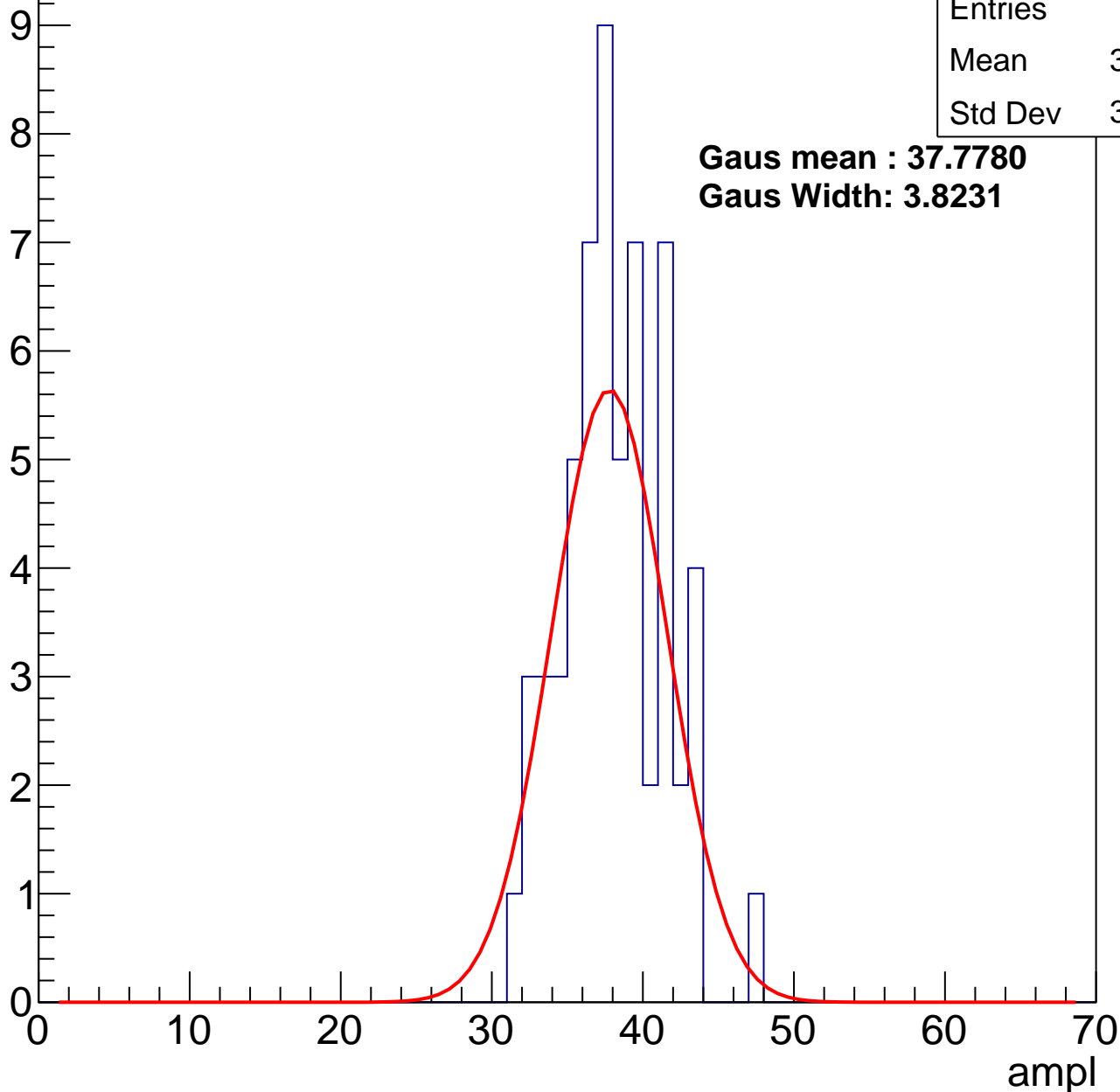
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	37.64
Std Dev	3.308

**Gaus mean : 37.7780**

**Gaus Width: 3.8231**



# B1L101S, U8-ch37, adc2

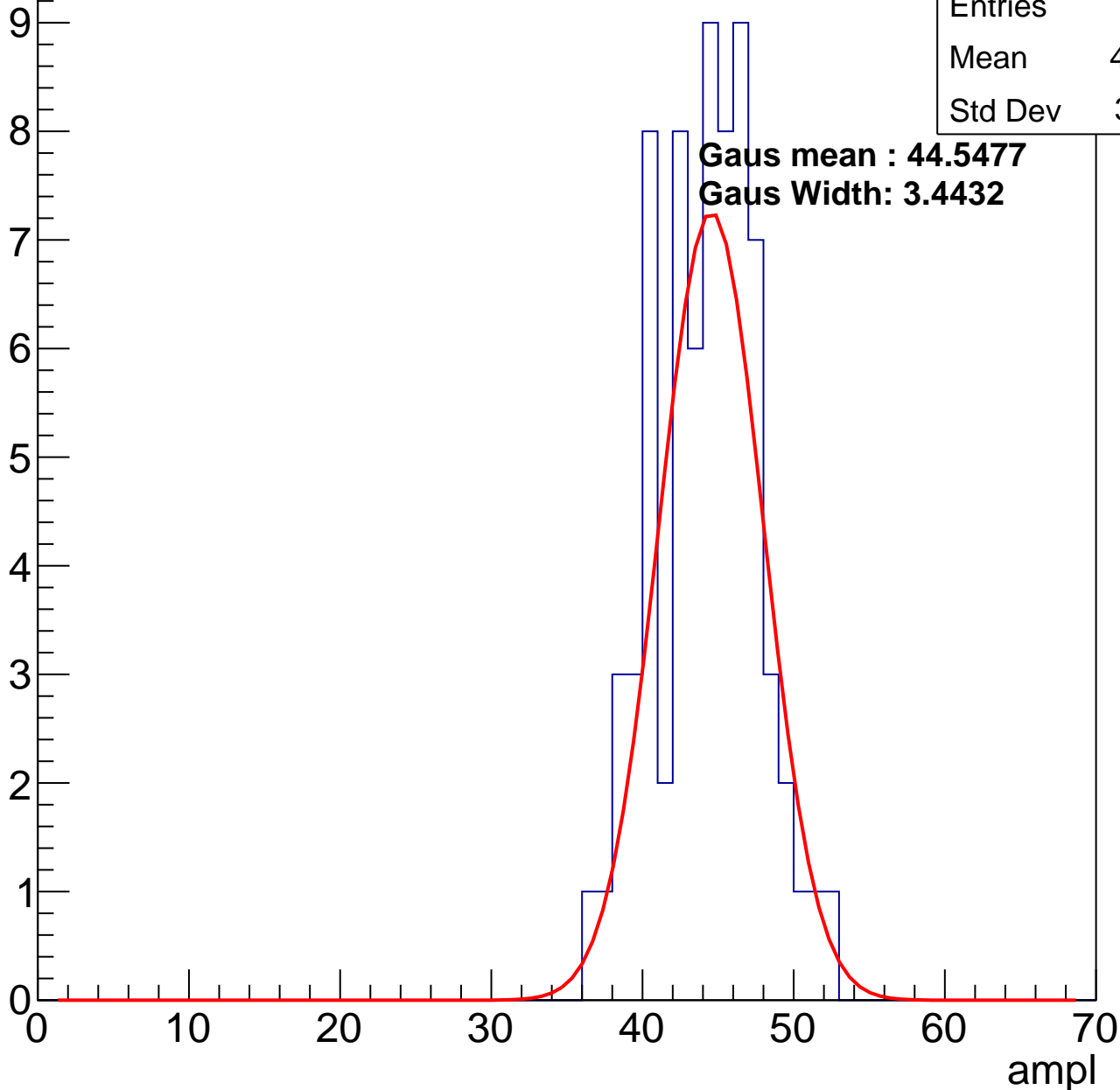
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	43.75
Std Dev	3.371

**Gaus mean : 44.5477**

**Gaus Width: 3.4432**

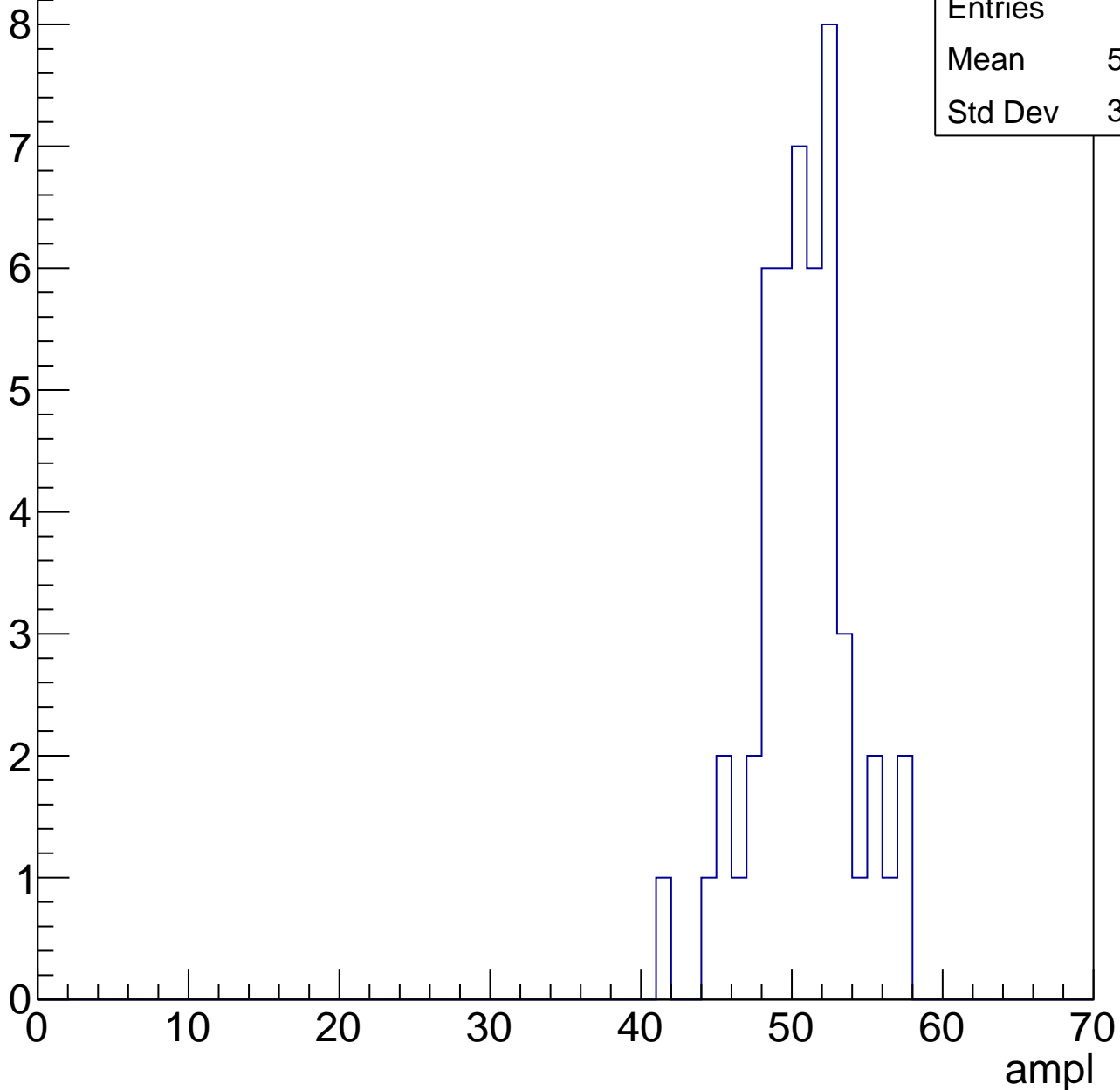


# B1L101S, U8-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

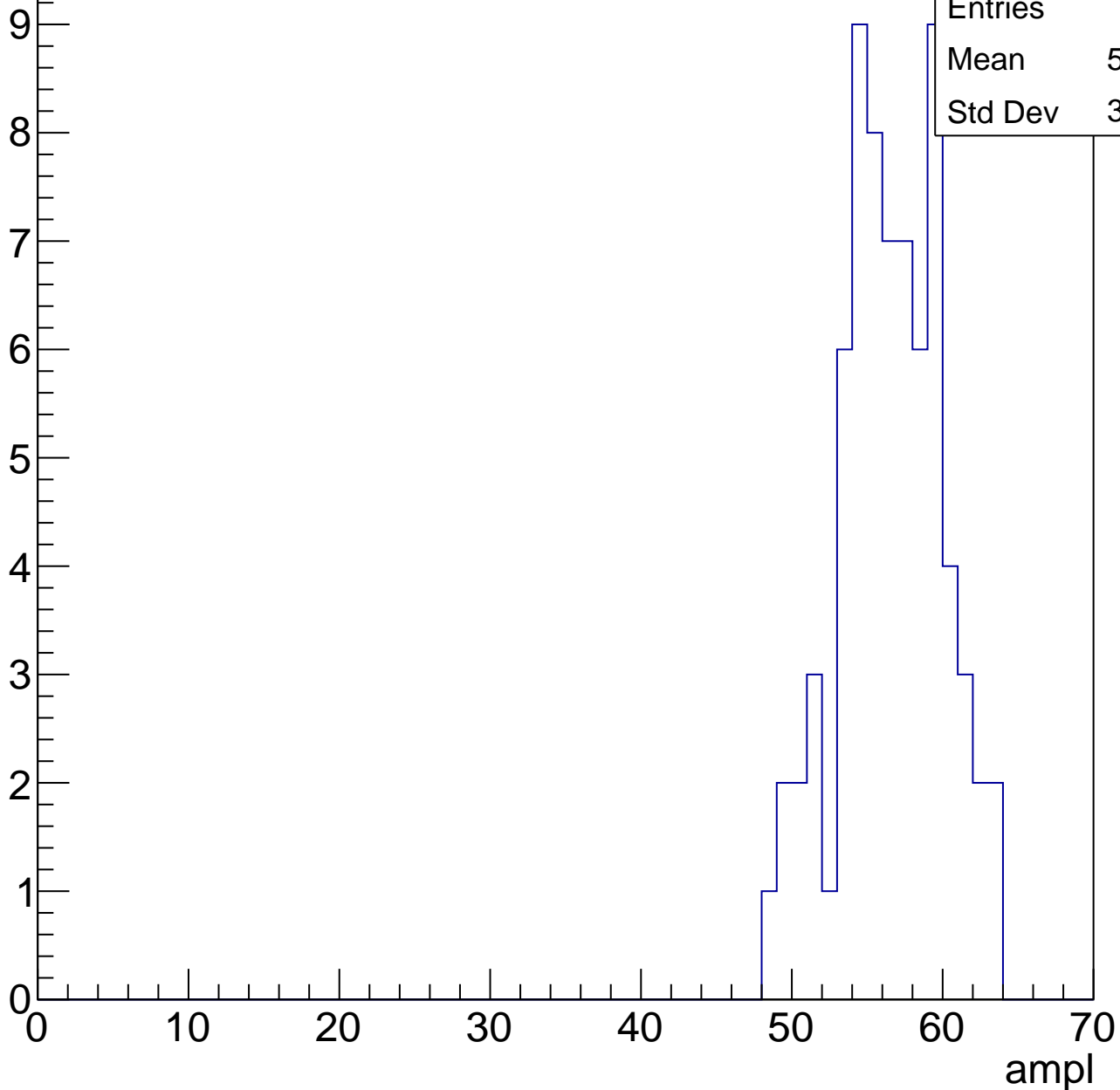
Entries	49
Mean	50.24
Std Dev	3.172



# B1L101S, U8-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

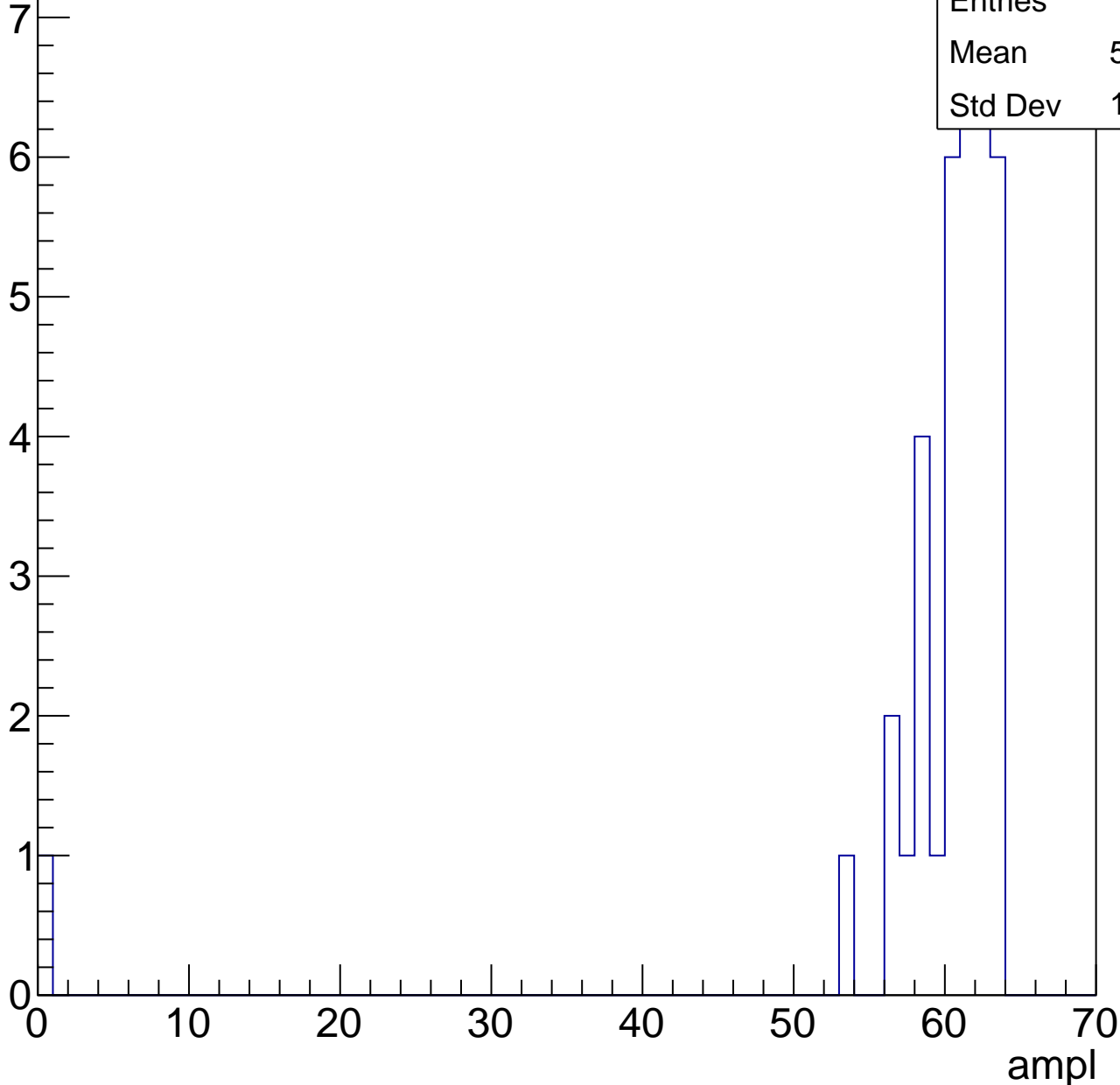


# B1L101S, U8-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	36
Mean	58.67
Std Dev	10.18



# B1L101S, U8-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch38, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	78
Mean	27.09
Std Dev	3.45

**Gaus mean : 27.0920**

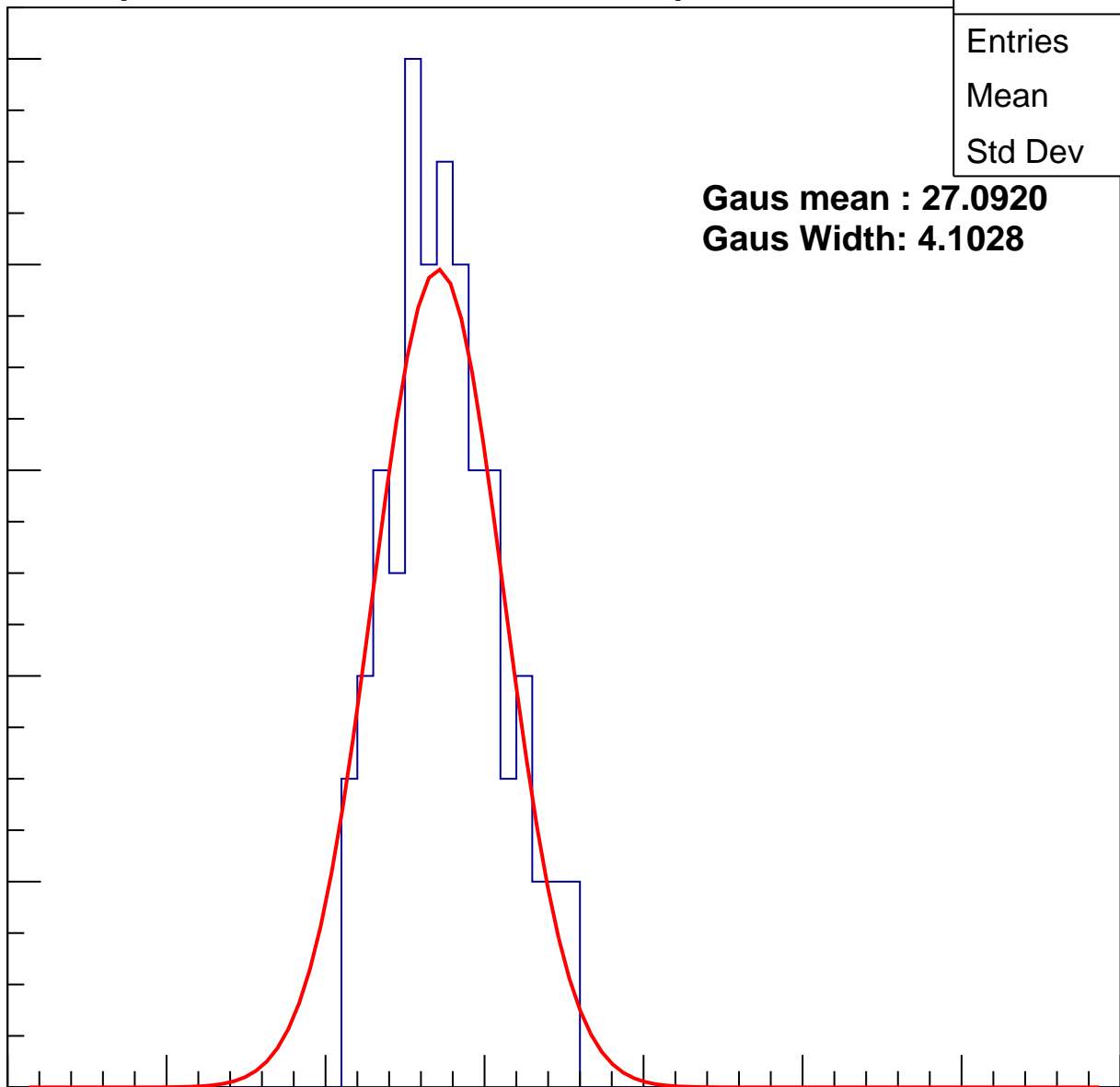
**Gaus Width: 4.1028**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U8-ch38, adc1

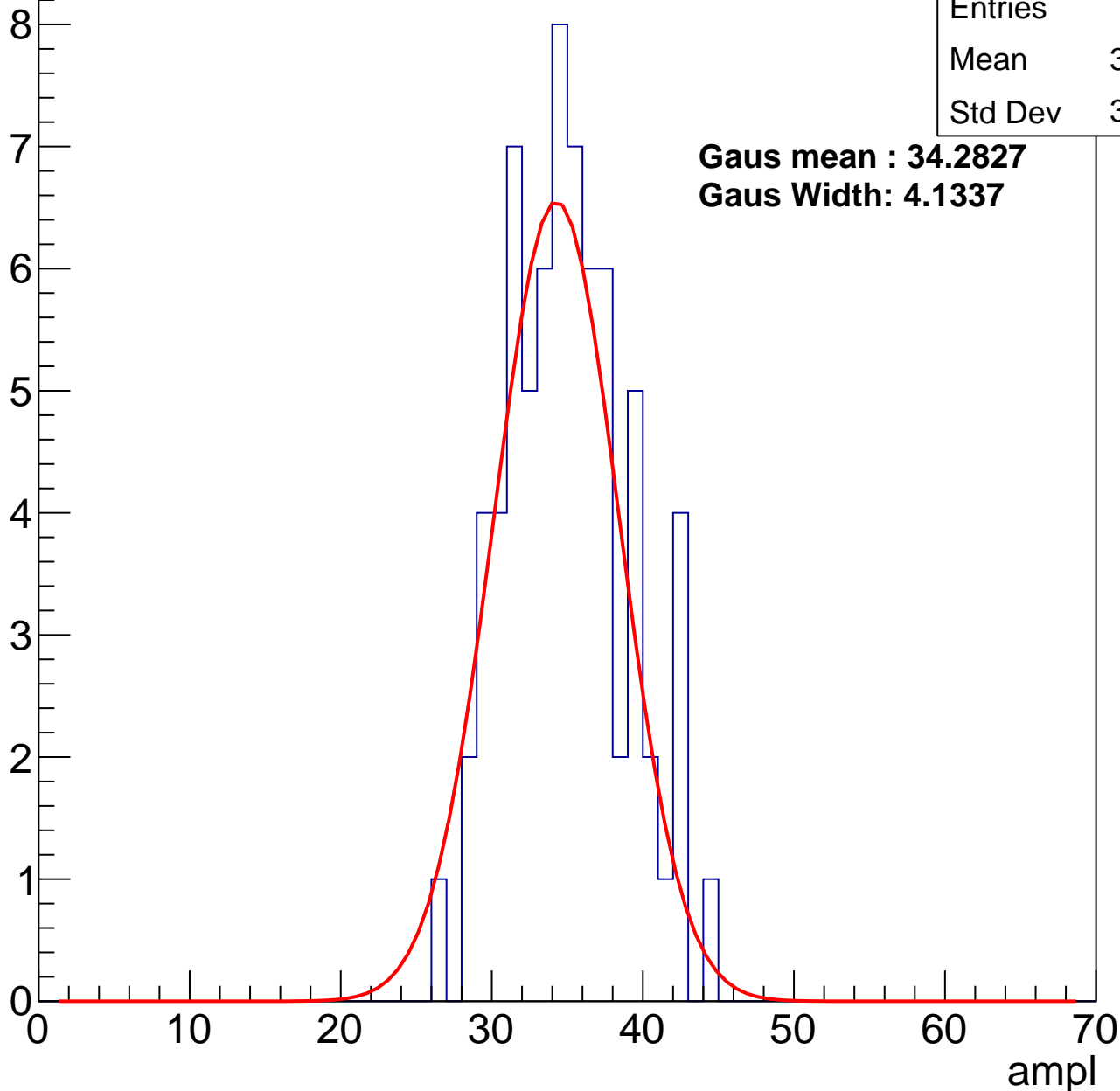
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	34.54
Std Dev	3.914

**Gaus mean : 34.2827**

**Gaus Width: 4.1337**



# B1L101S, U8-ch38, adc2

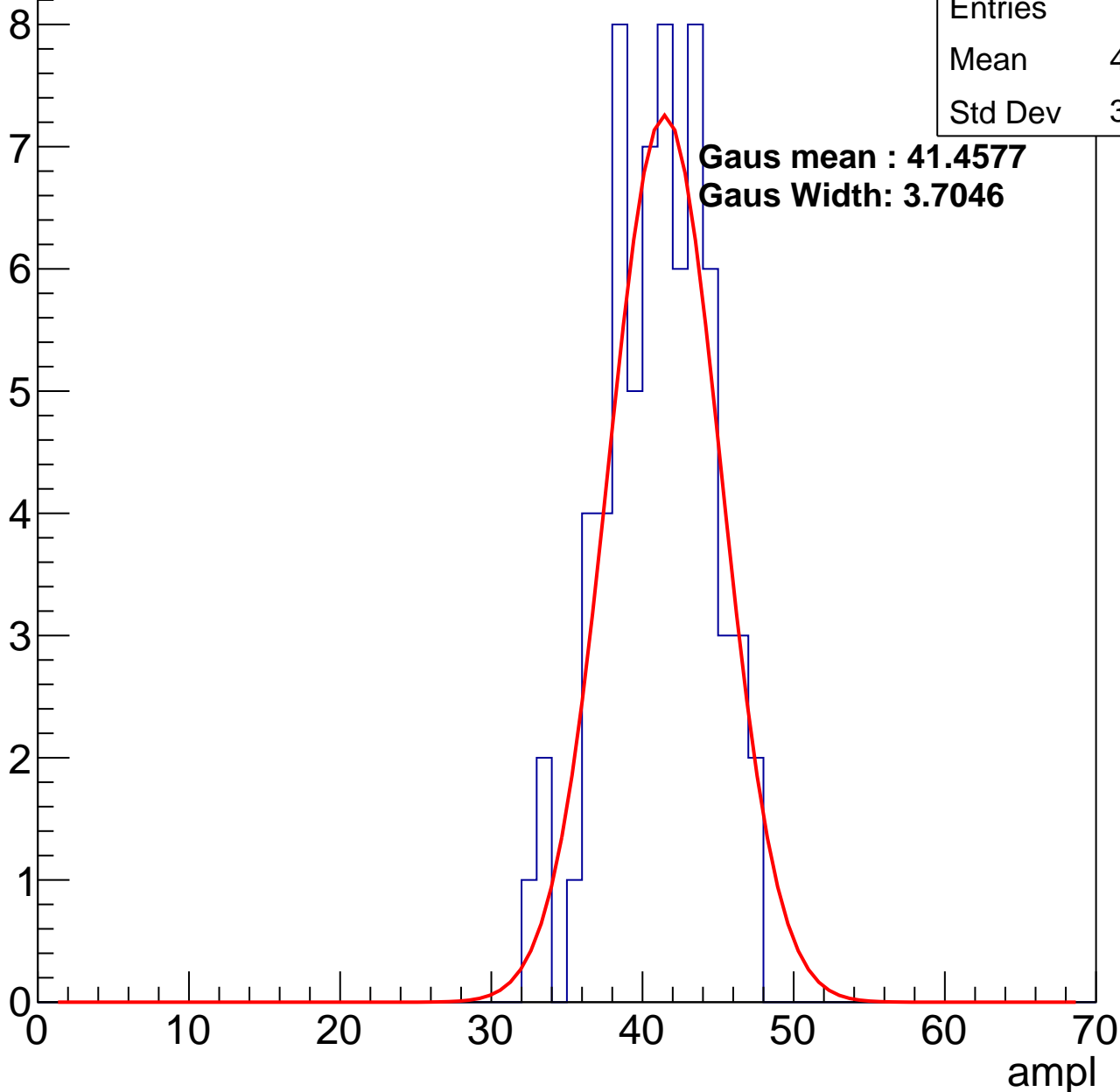
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	40.57
Std Dev	3.393

**Gaus mean : 41.4577**

**Gaus Width: 3.7046**

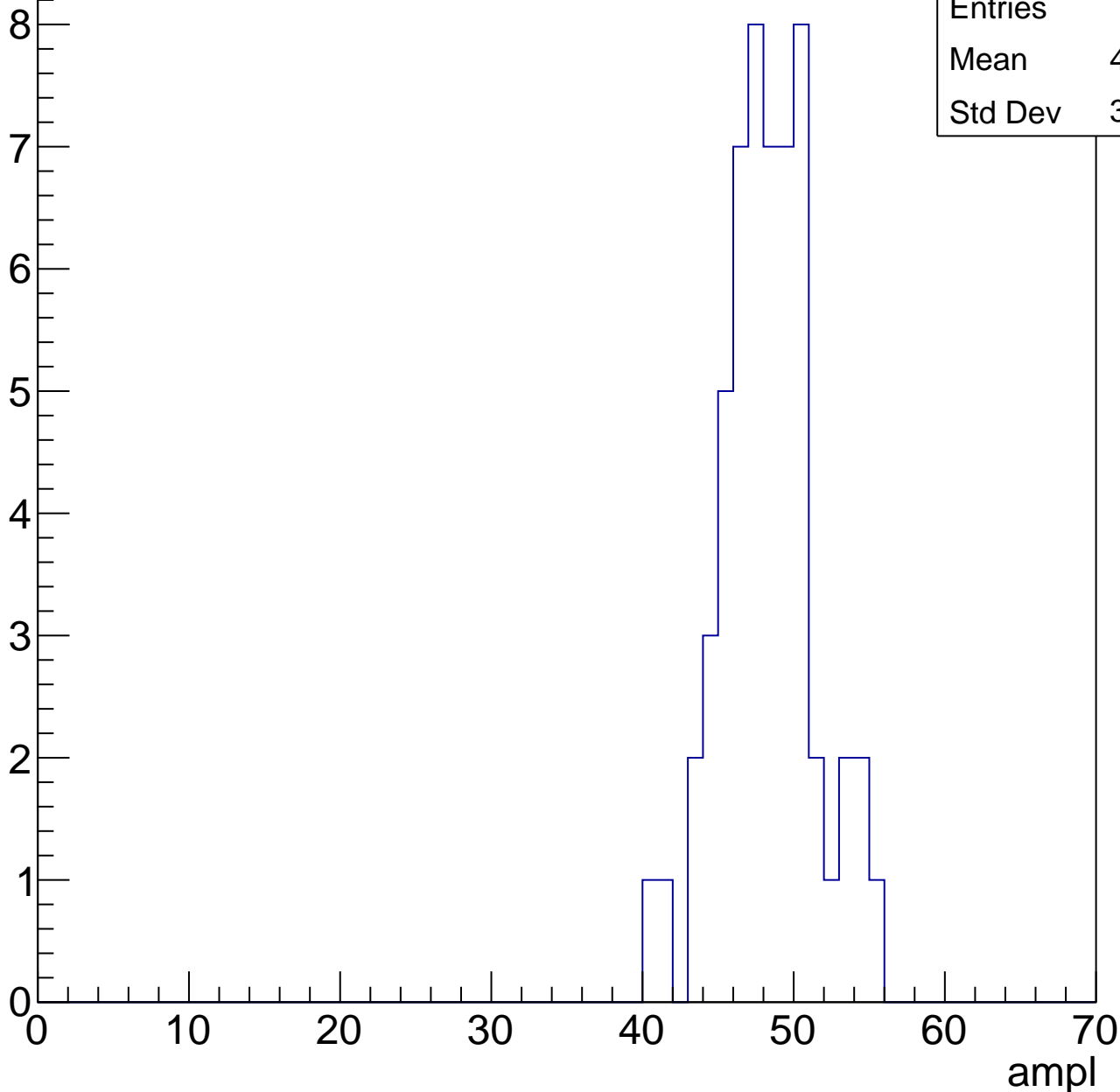


# B1L101S, U8-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	47.79
Std Dev	3.059

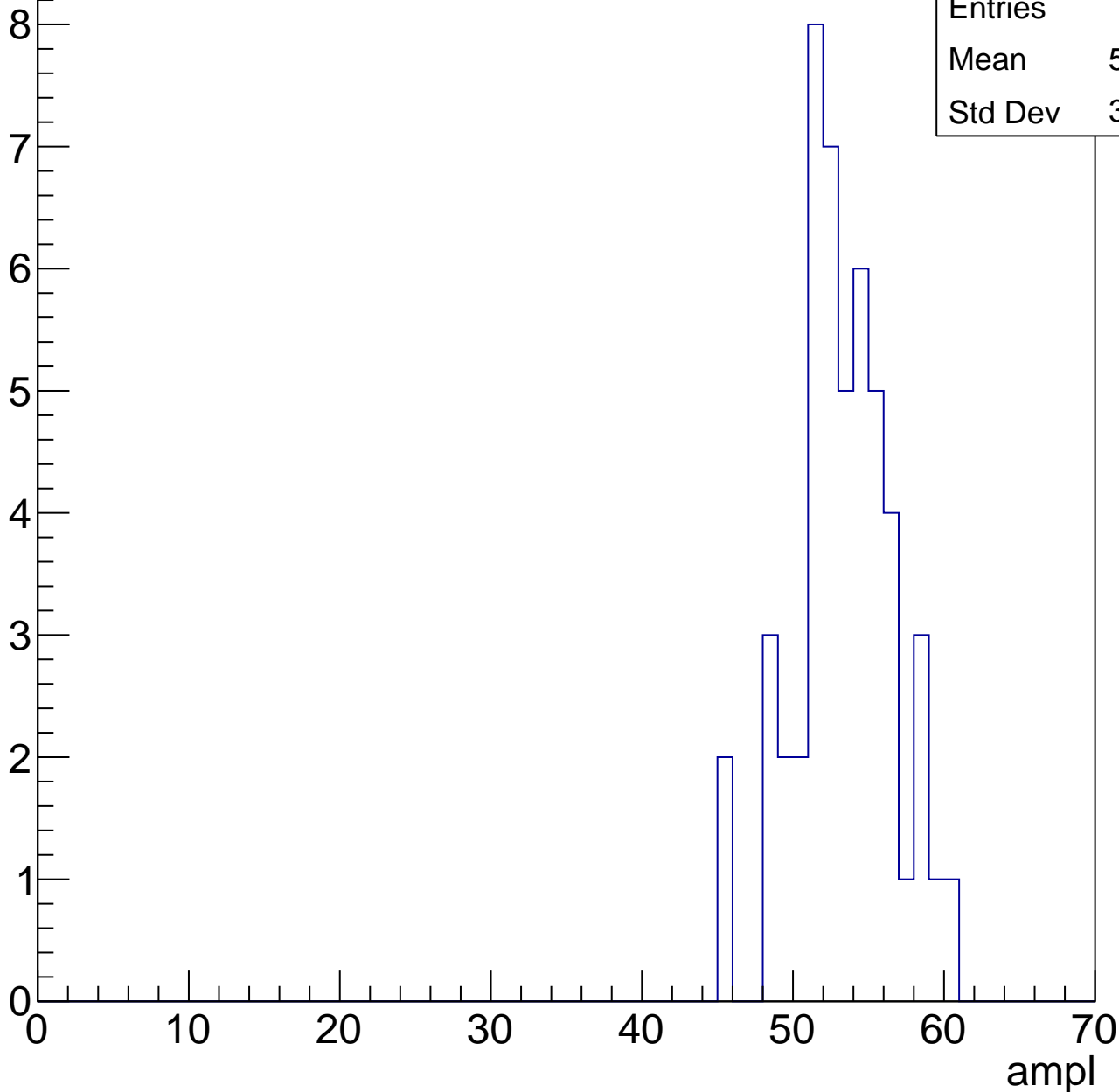


# B1L101S, U8-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

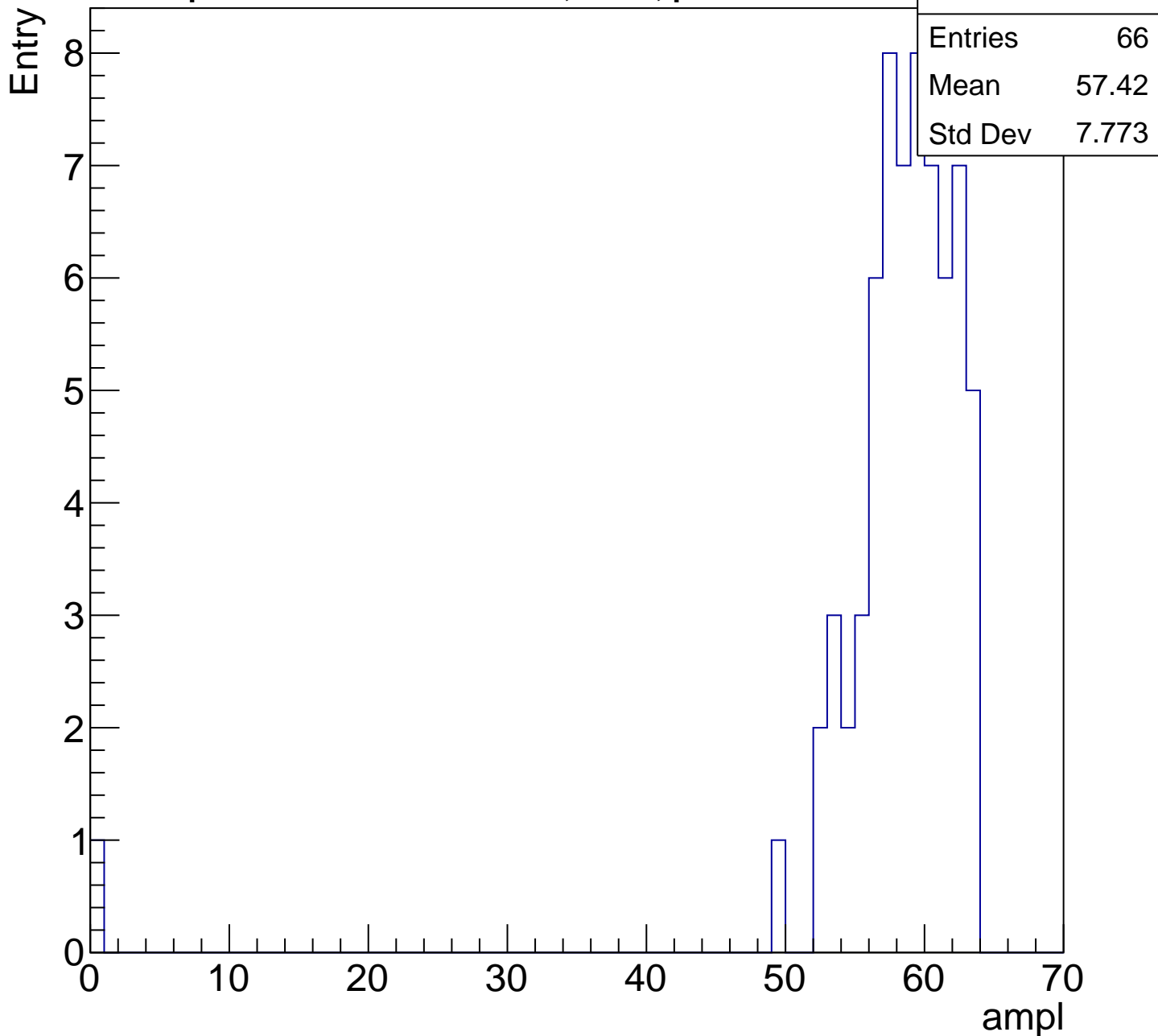
Entry

Entries	50
Mean	52.84
Std Dev	3.252



# B1L101S, U8-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

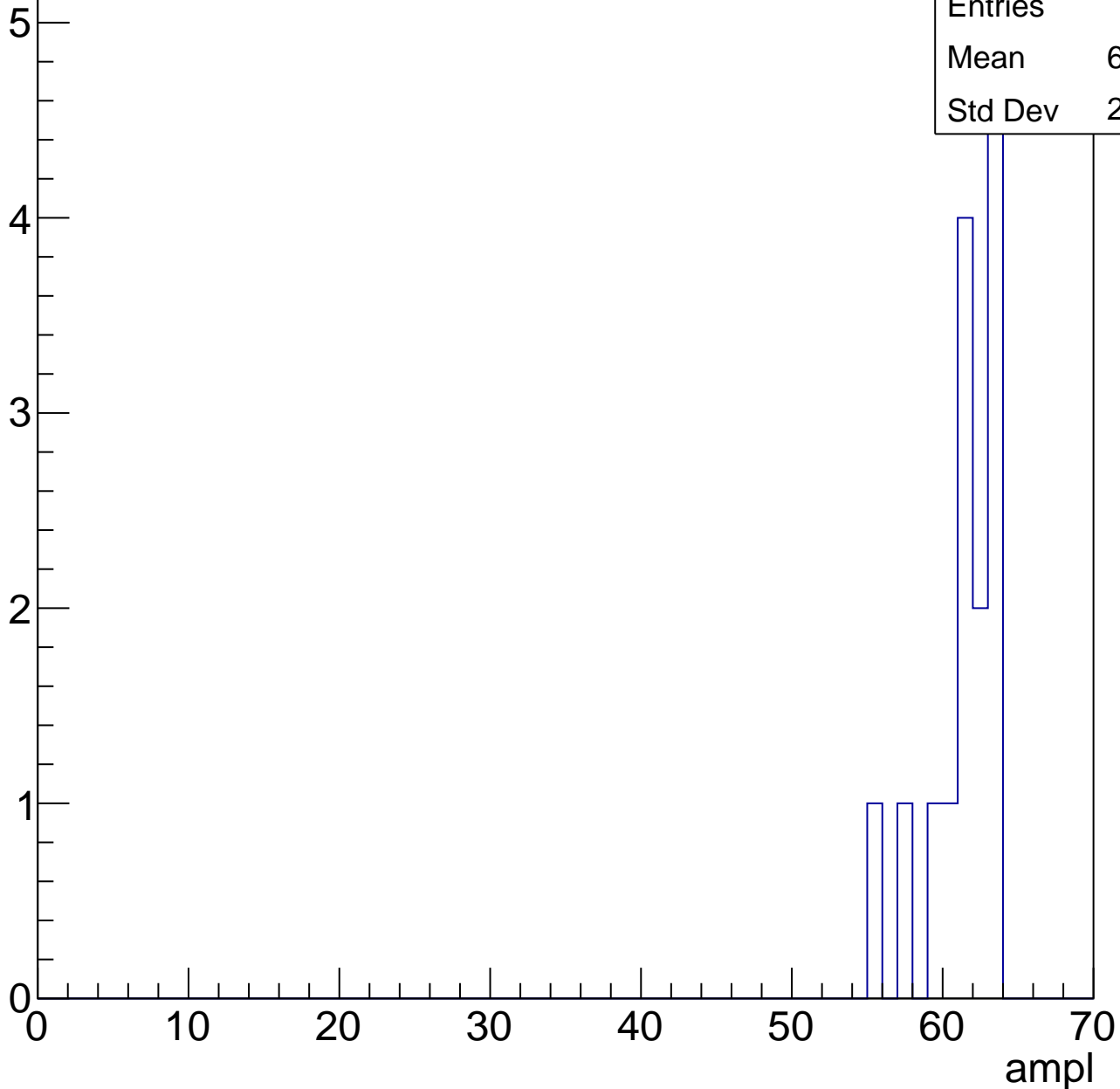


# B1L101S, U8-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	15
Mean	60.93
Std Dev	2.294

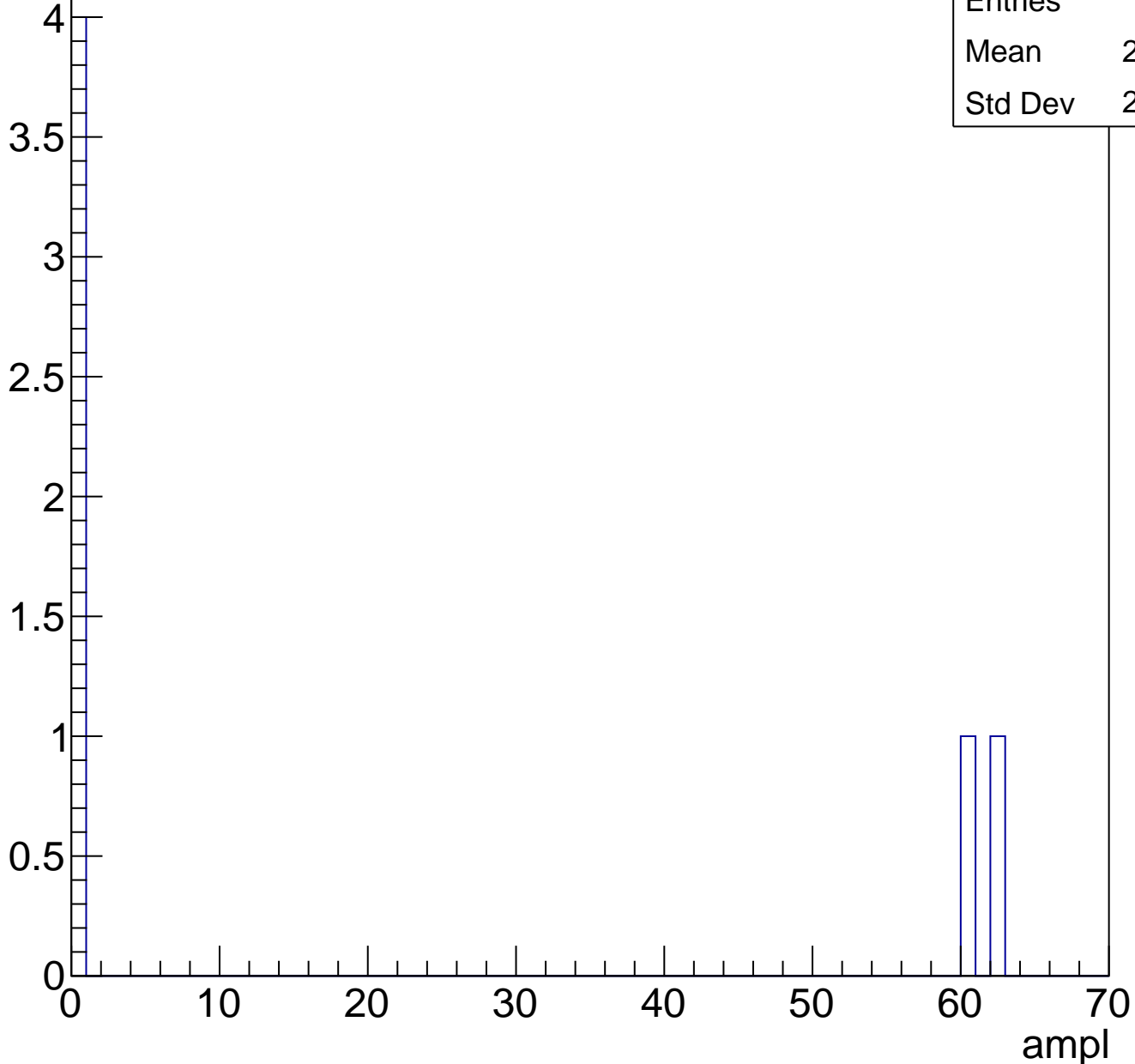




# B1L101S, U8-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	6
Mean	20.33
Std Dev	28.76

# B1L101S, U8-ch39, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	79
Mean	28.18
Std Dev	6.752

**Gaus mean : 30.0109**

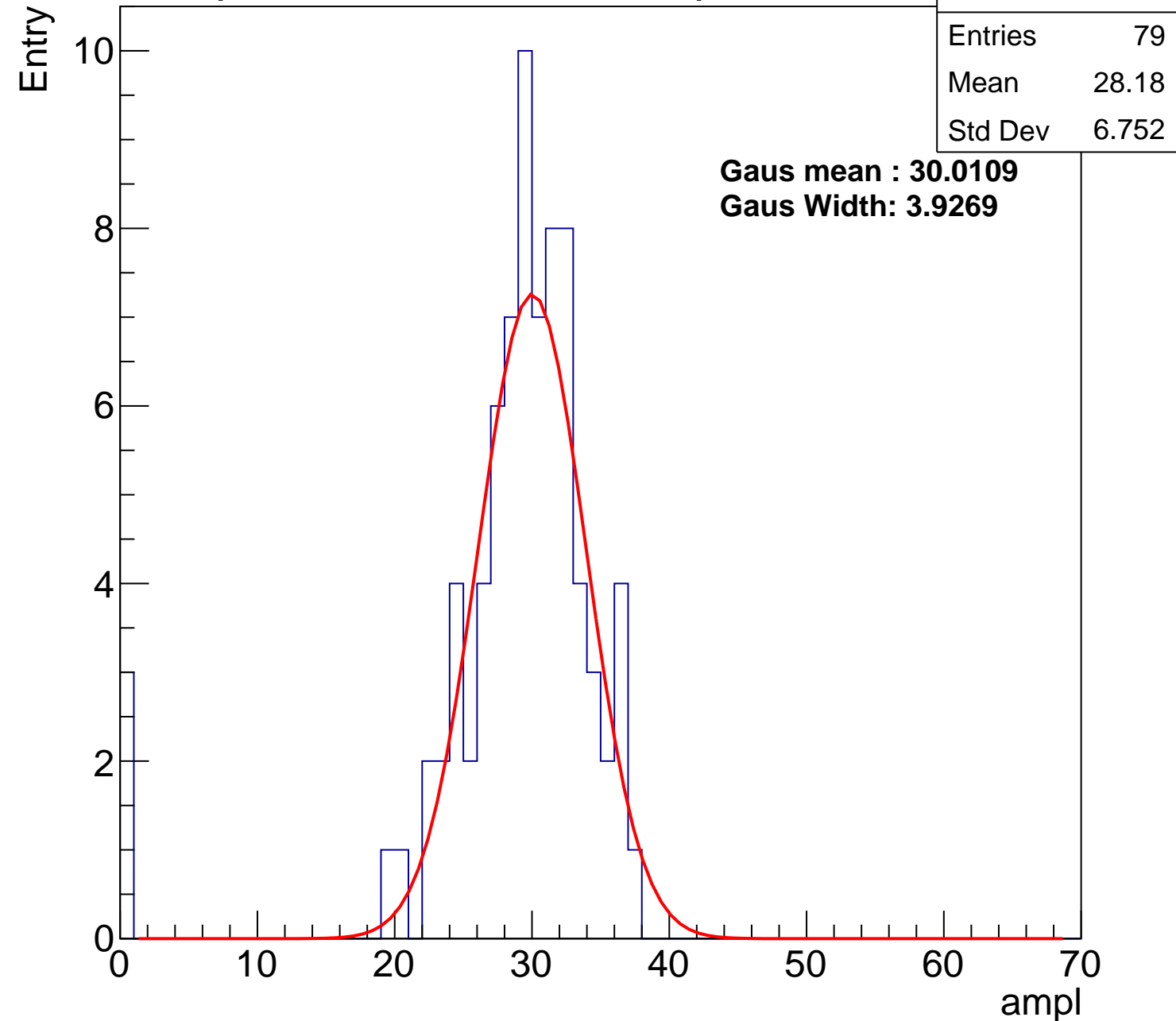
**Gaus Width: 3.9269**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U8-ch39, adc1

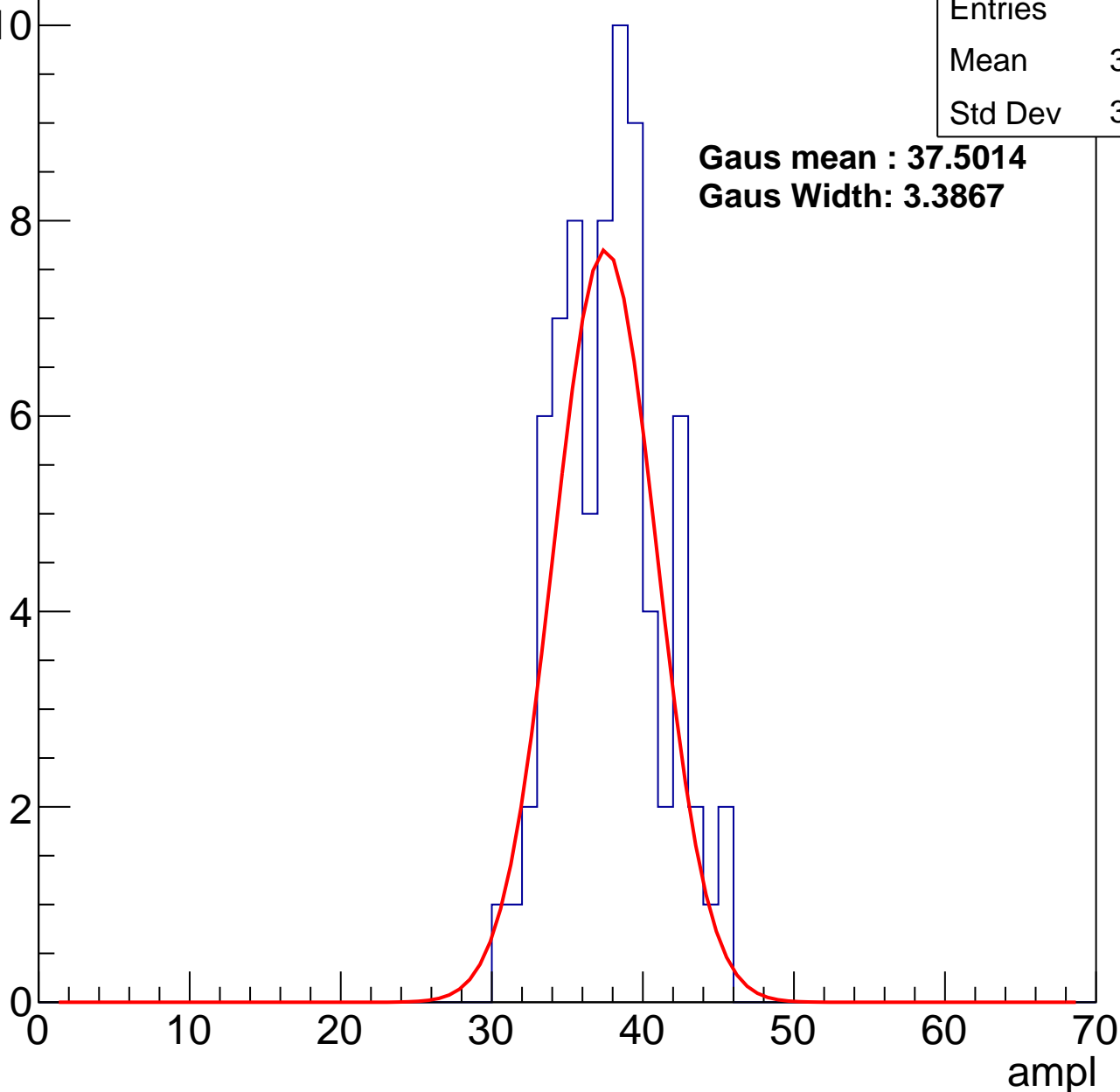
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	37.32
Std Dev	3.362

**Gaus mean : 37.5014**

**Gaus Width: 3.3867**



# B1L101S, U8-ch39, adc2

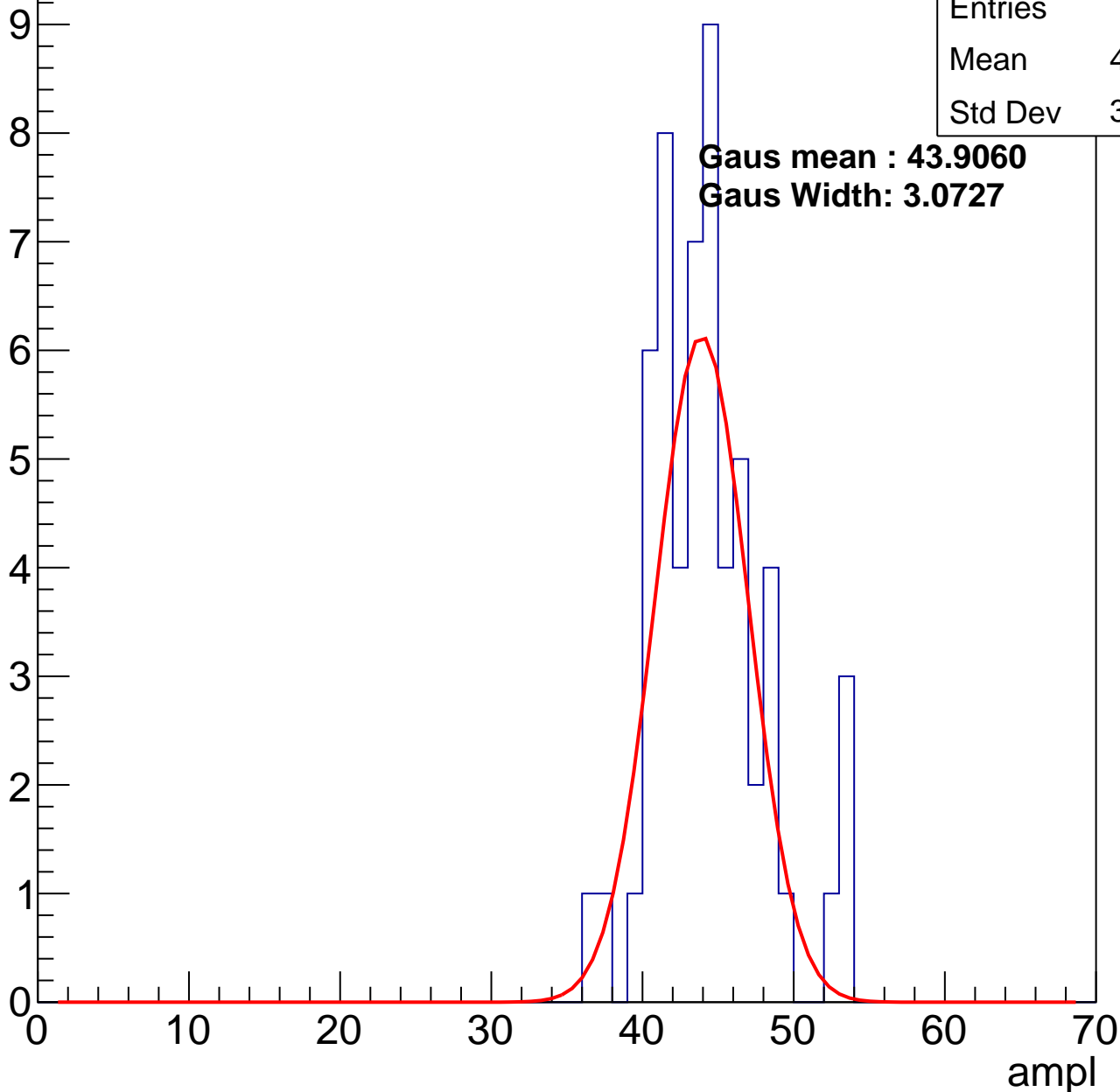
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	43.88
Std Dev	3.666

**Gaus mean : 43.9060**

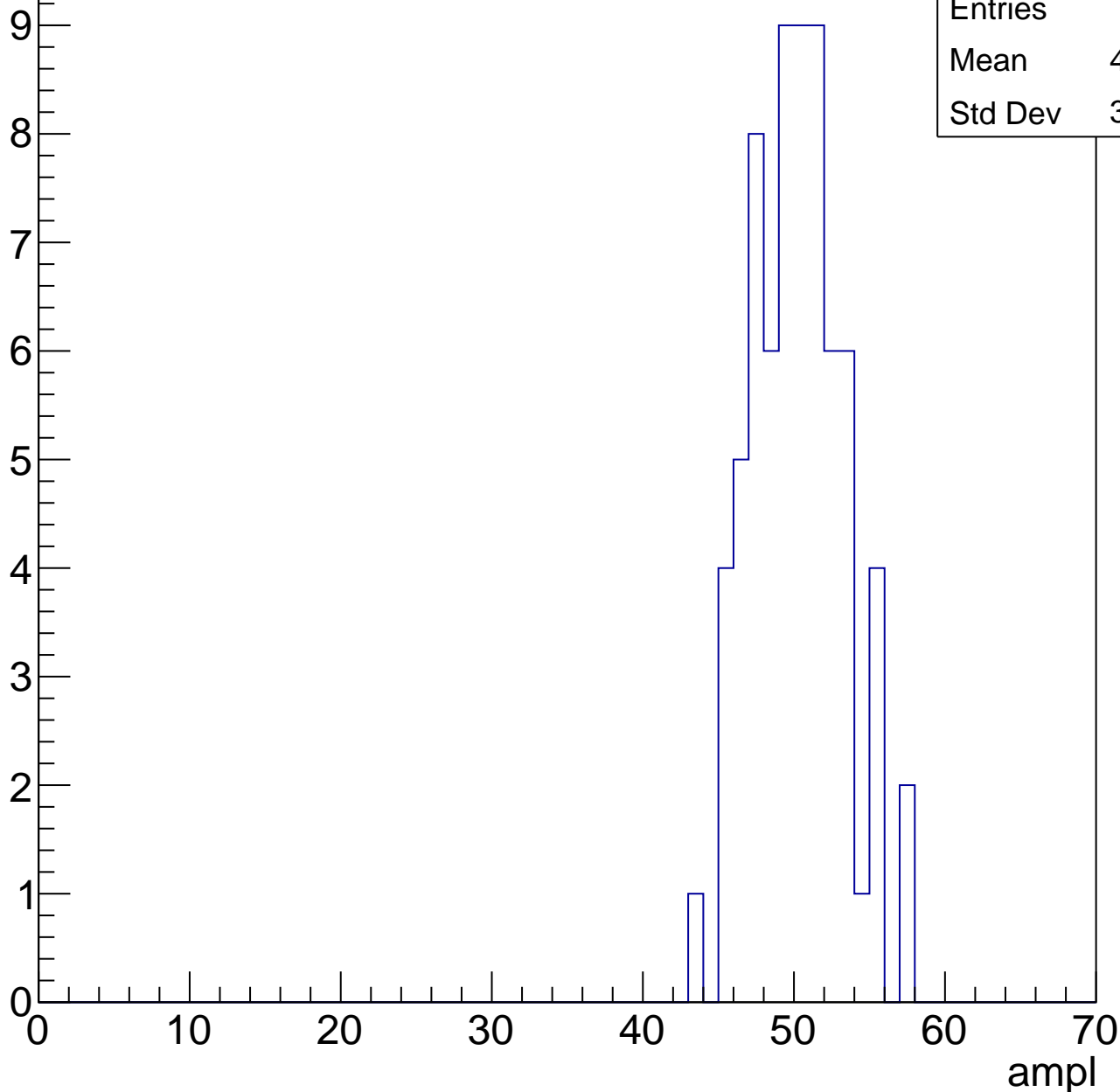
**Gaus Width: 3.0727**



# B1L101S, U8-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

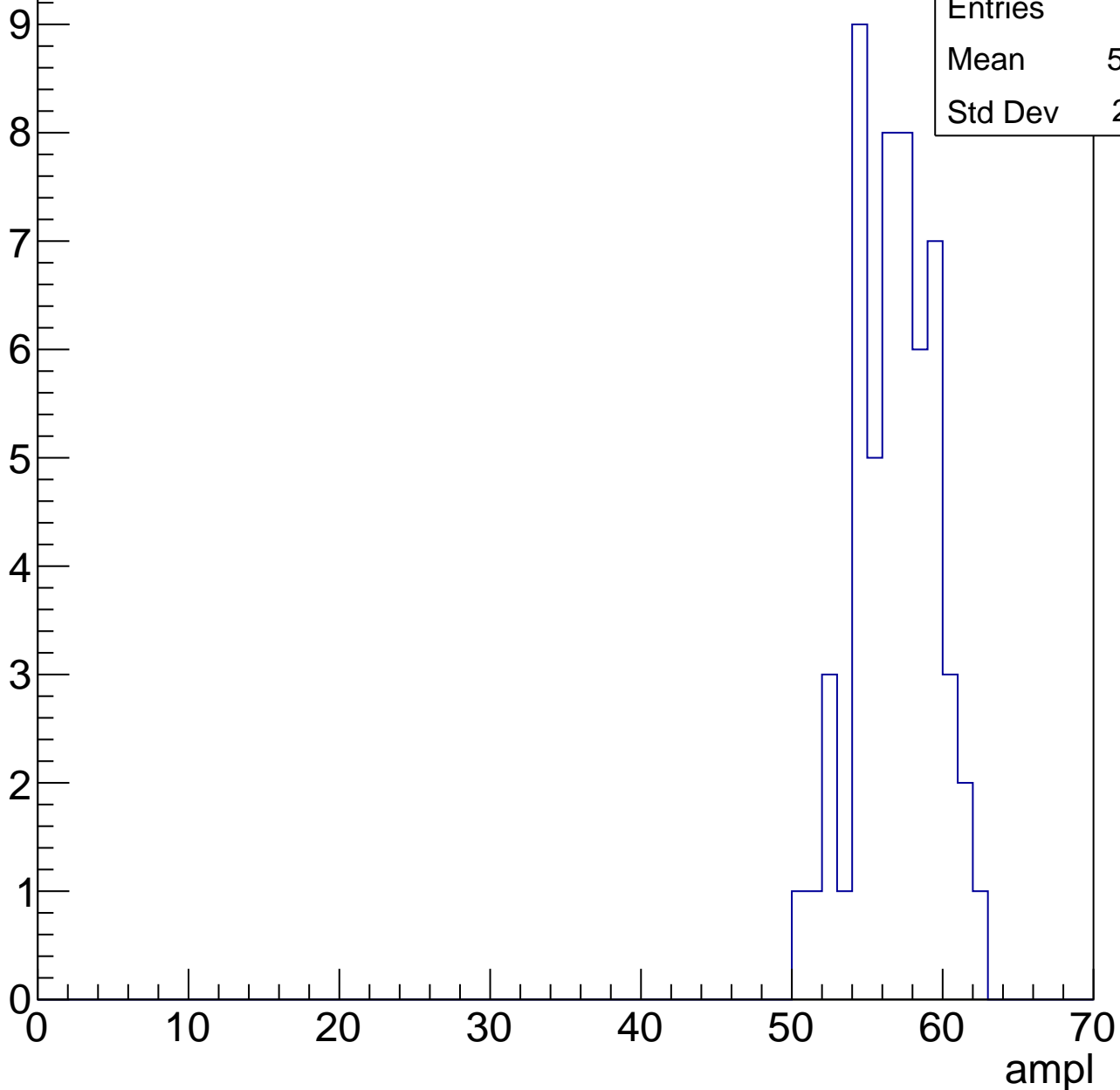


# B1L101S, U8-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	56.36
Std Dev	2.631

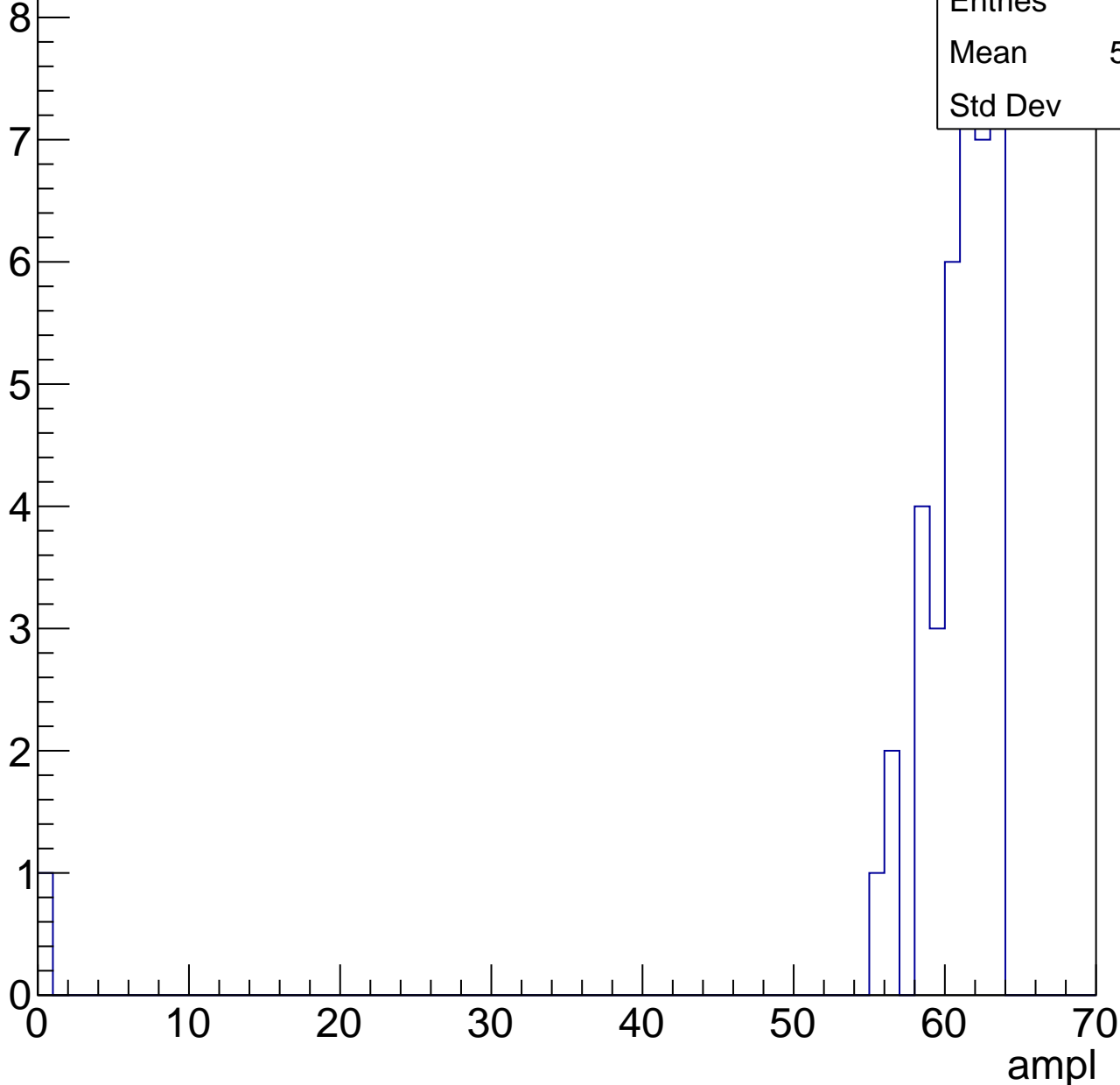


# B1L101S, U8-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	40
Mean	59.05
Std Dev	9.68



# B1L101S, U8-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U8-ch40, adc0

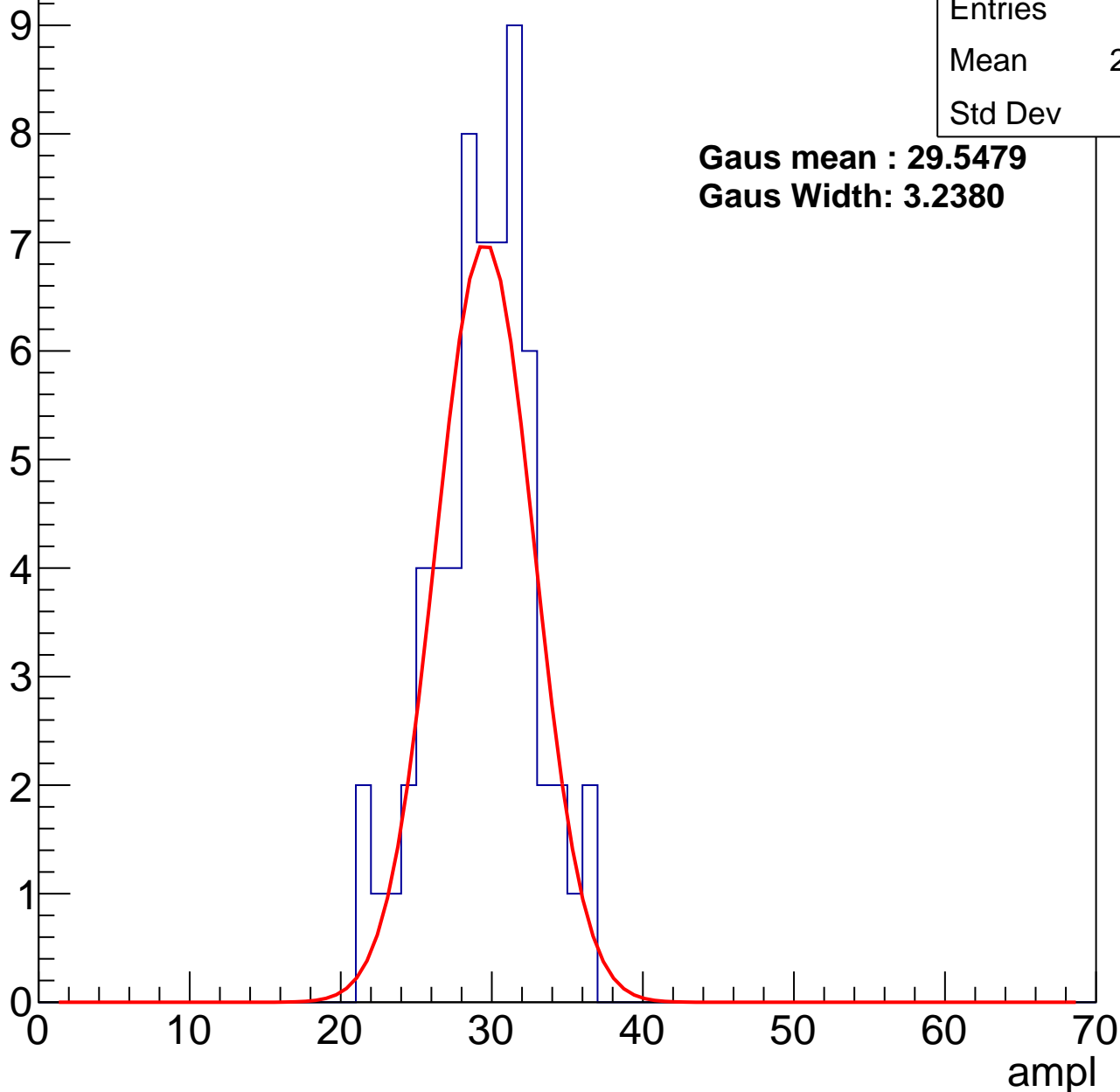
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	28.97
Std Dev	3.36

**Gaus mean : 29.5479**

**Gaus Width: 3.2380**



# B1L101S, U8-ch40, adc1

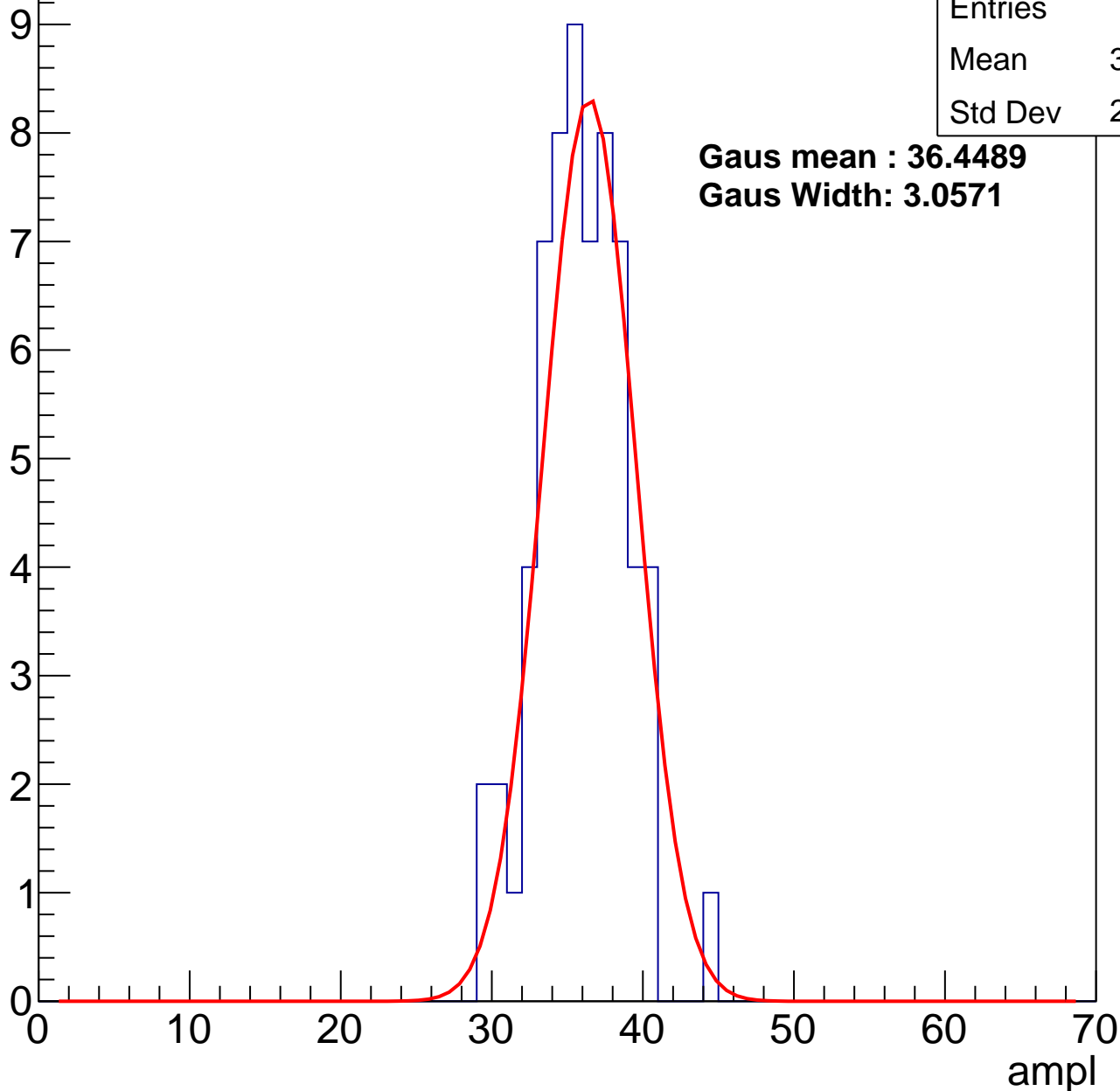
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	35.45
Std Dev	2.915

**Gaus mean : 36.4489**

**Gaus Width: 3.0571**



# B1L101S, U8-ch40, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	70
Mean	42.19
Std Dev	3.035

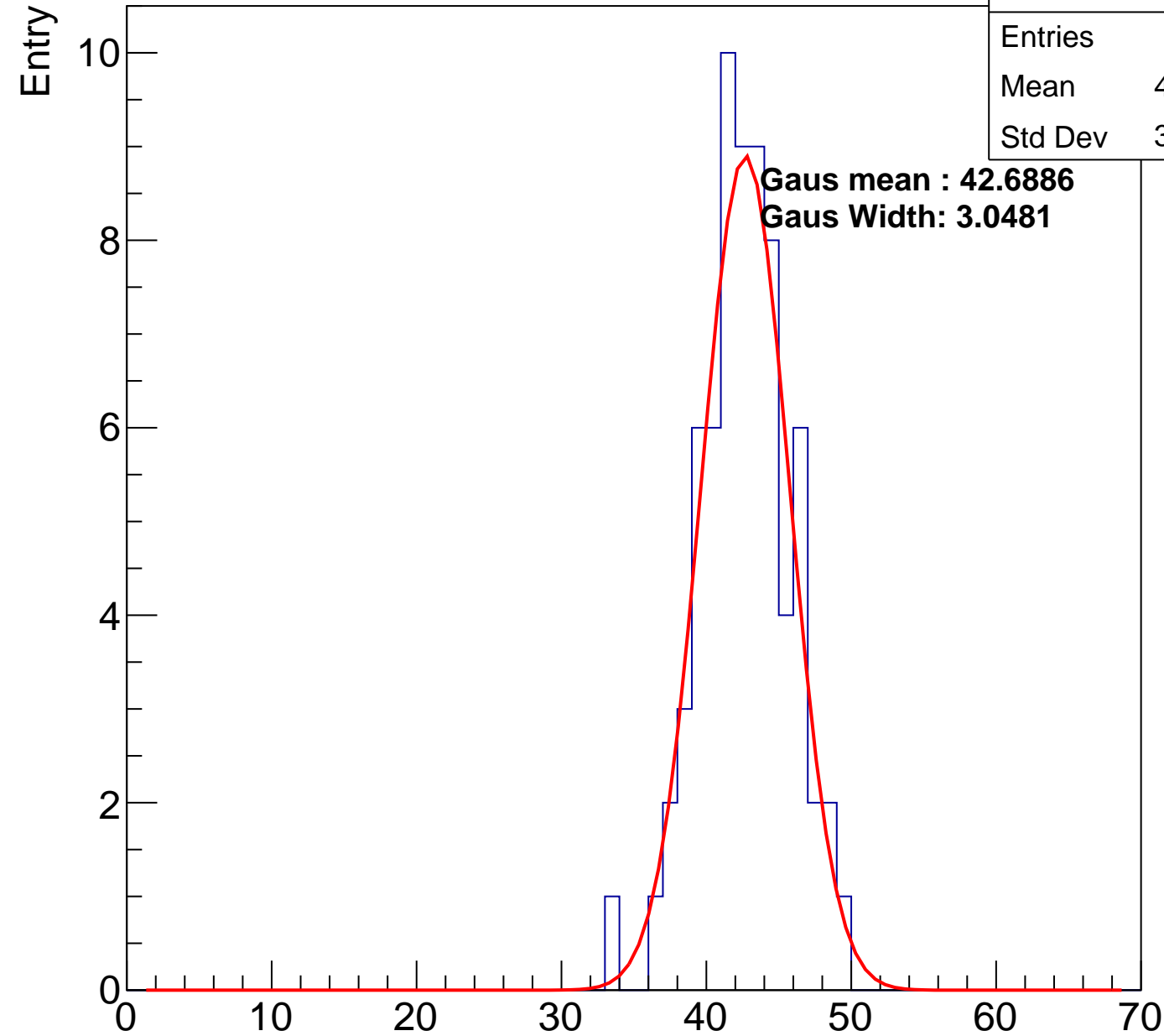
**Gaus mean : 42.6886**

**Gaus Width: 3.0481**

Entry

10  
8  
6  
4  
2  
0

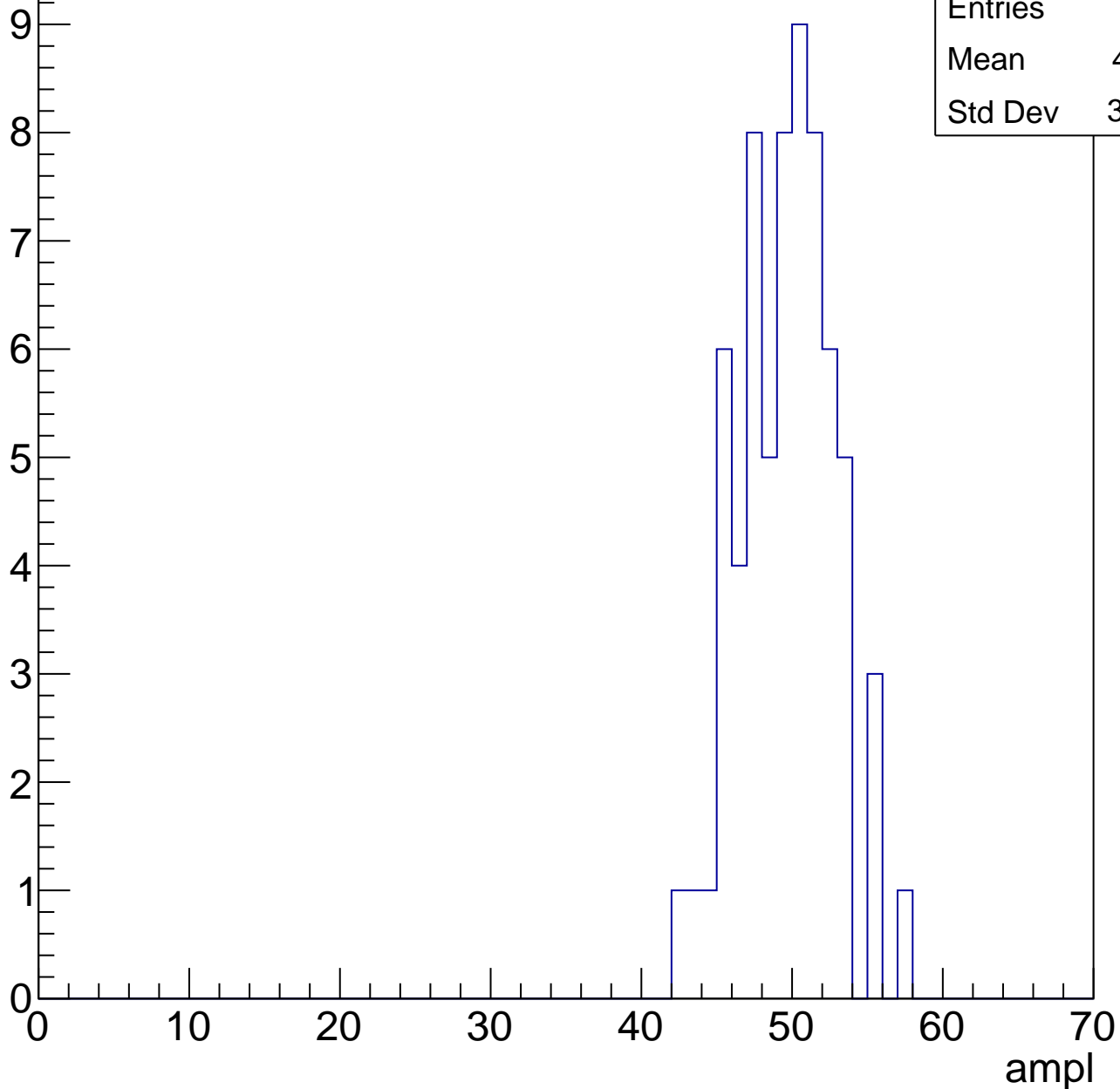
ampl



# B1L101S, U8-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

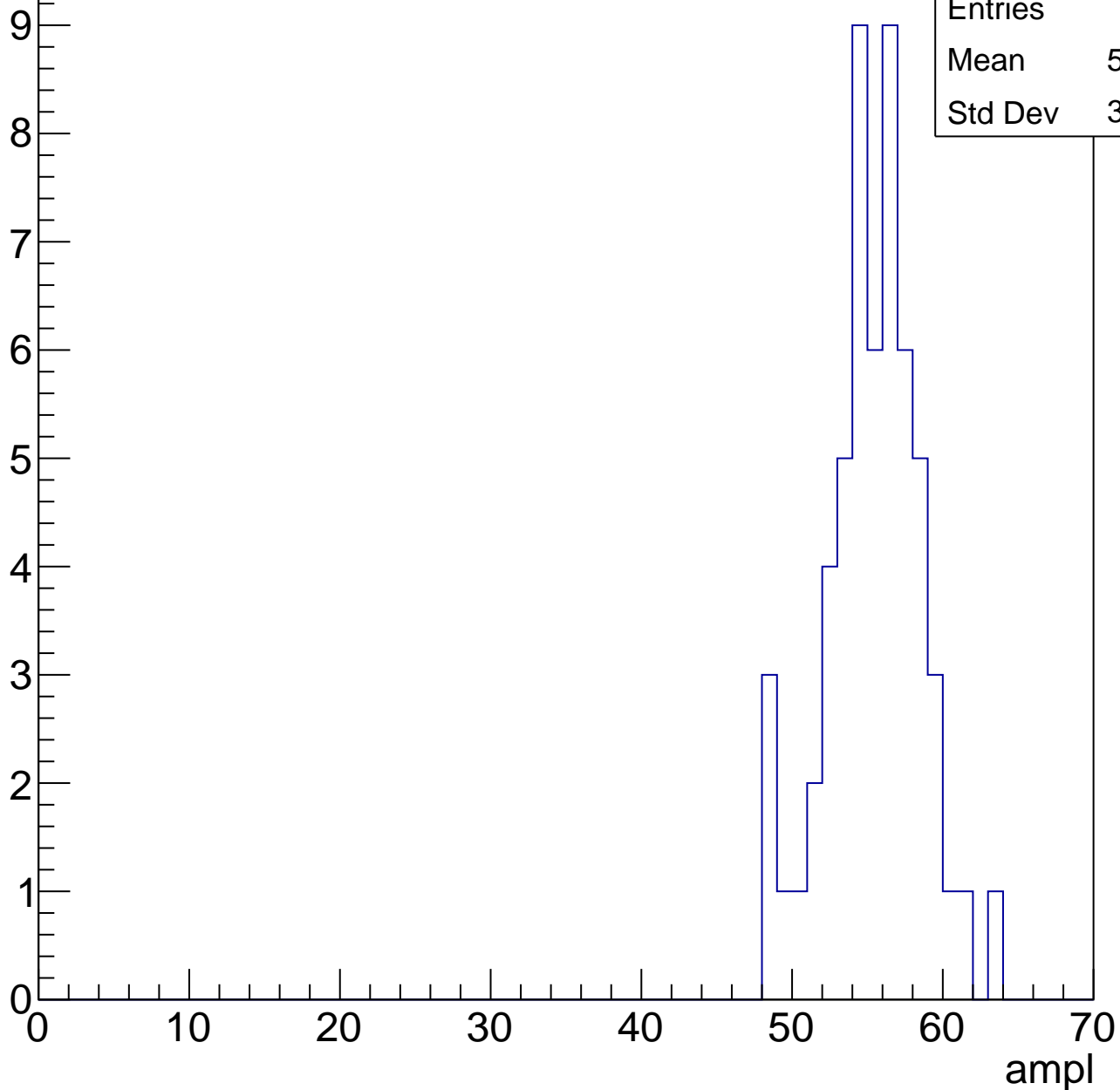
Entry



# B1L101S, U8-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

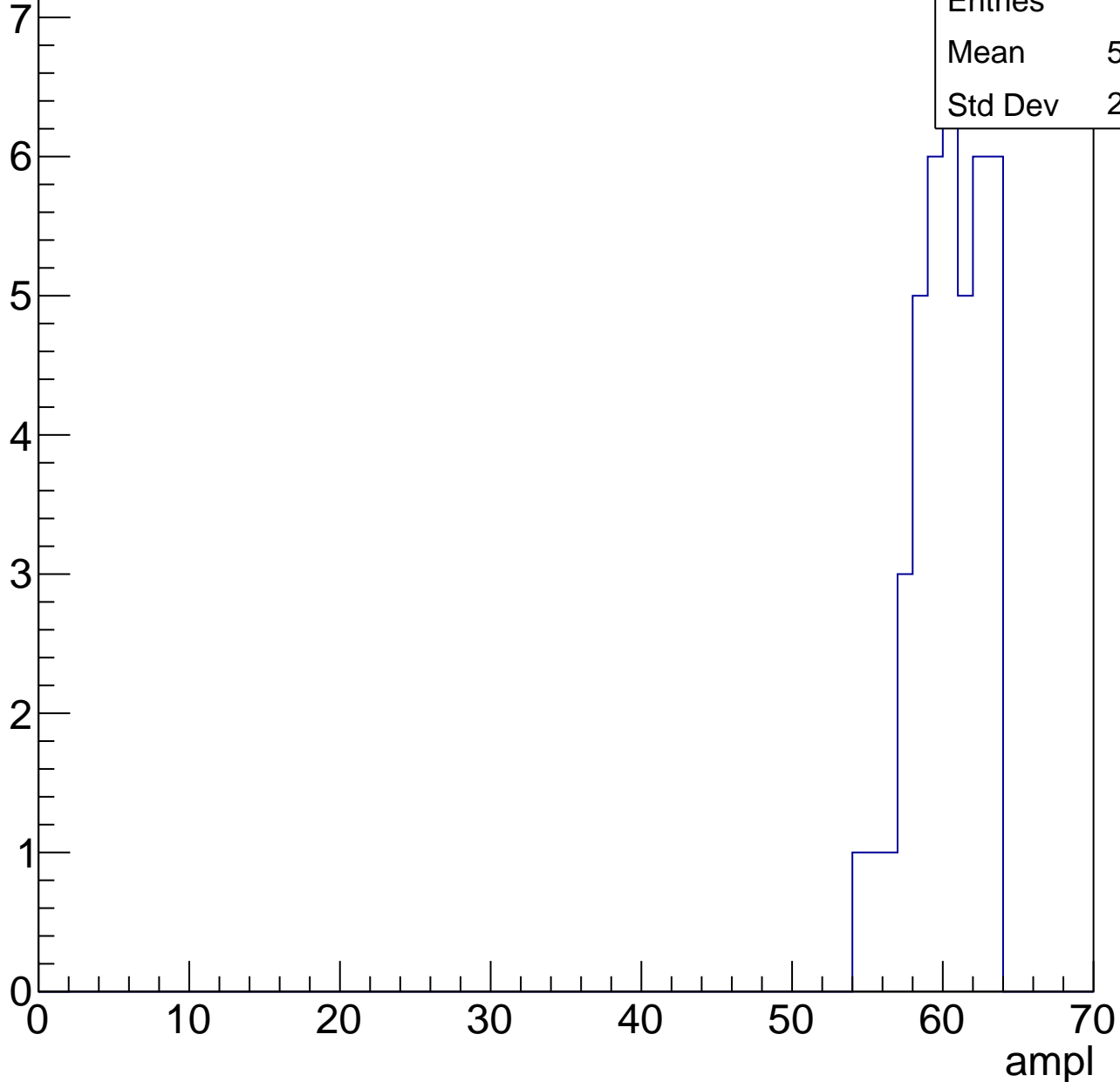


Entries	57
Mean	54.93
Std Dev	3.122

# B1L101S, U8-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

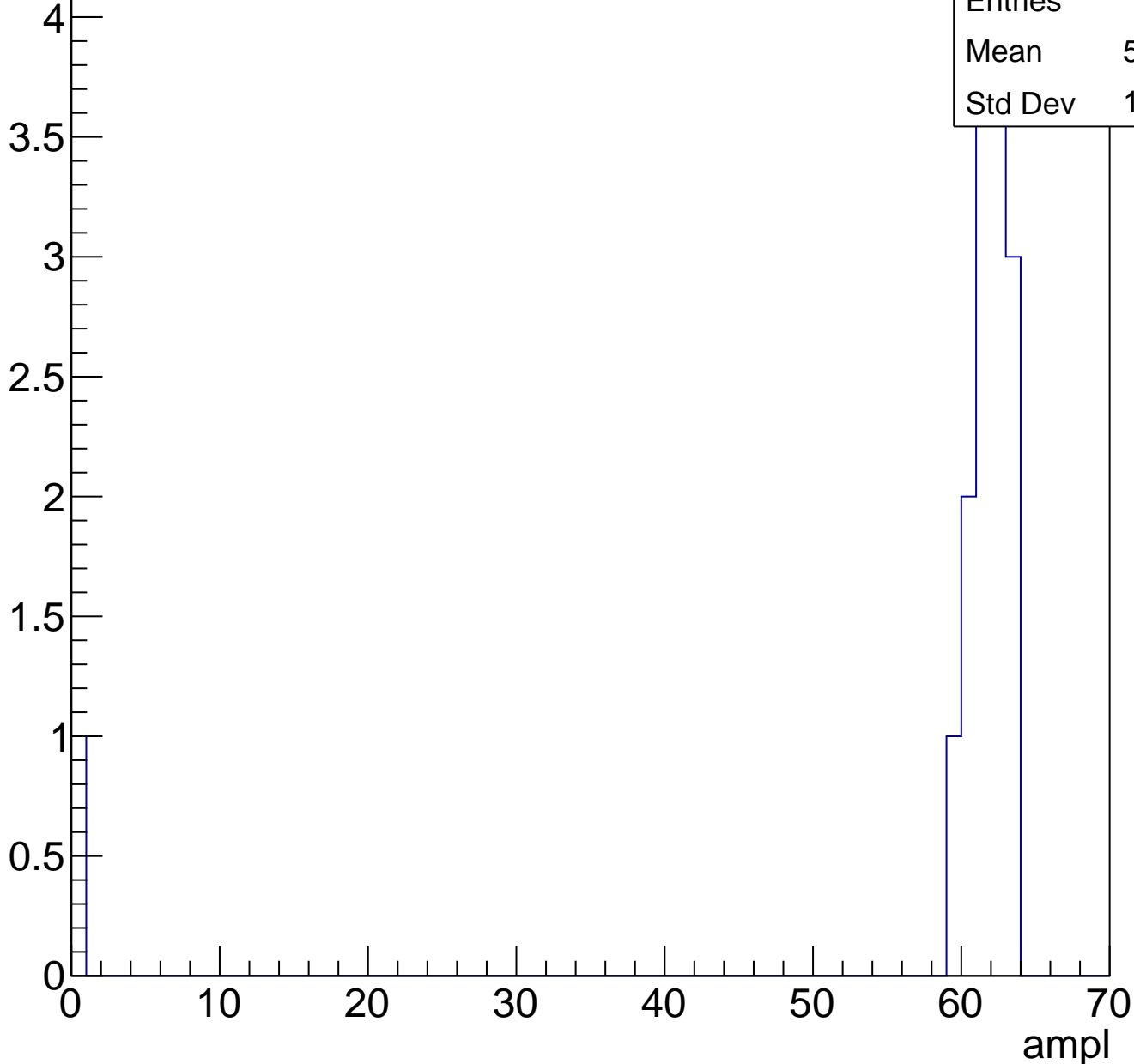
Entry



# B1L101S, U8-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U8-ch41, adc0

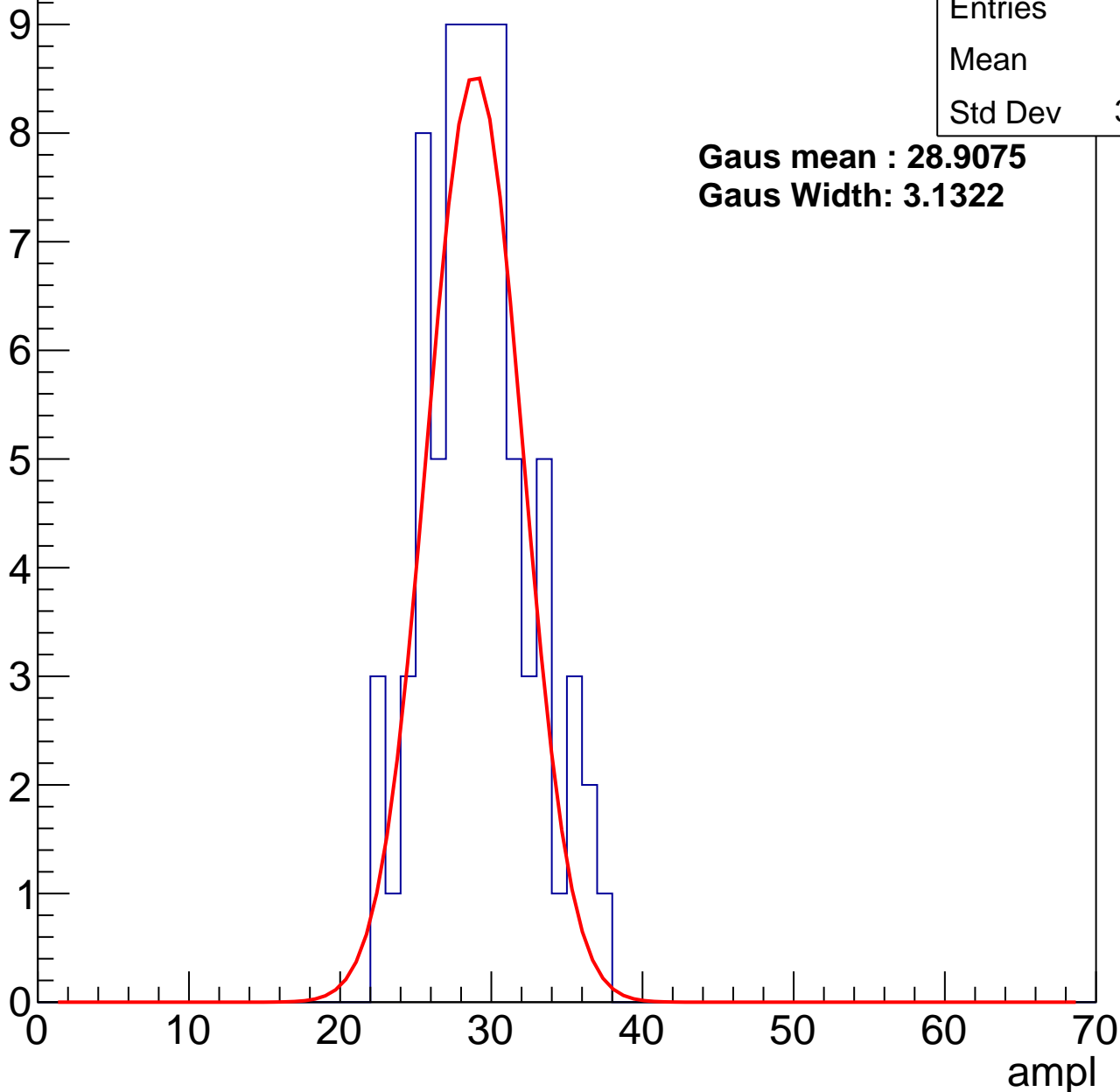
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	28.7
Std Dev	3.441

**Gaus mean : 28.9075**

**Gaus Width: 3.1322**



# B1L101S, U8-ch41, adc1

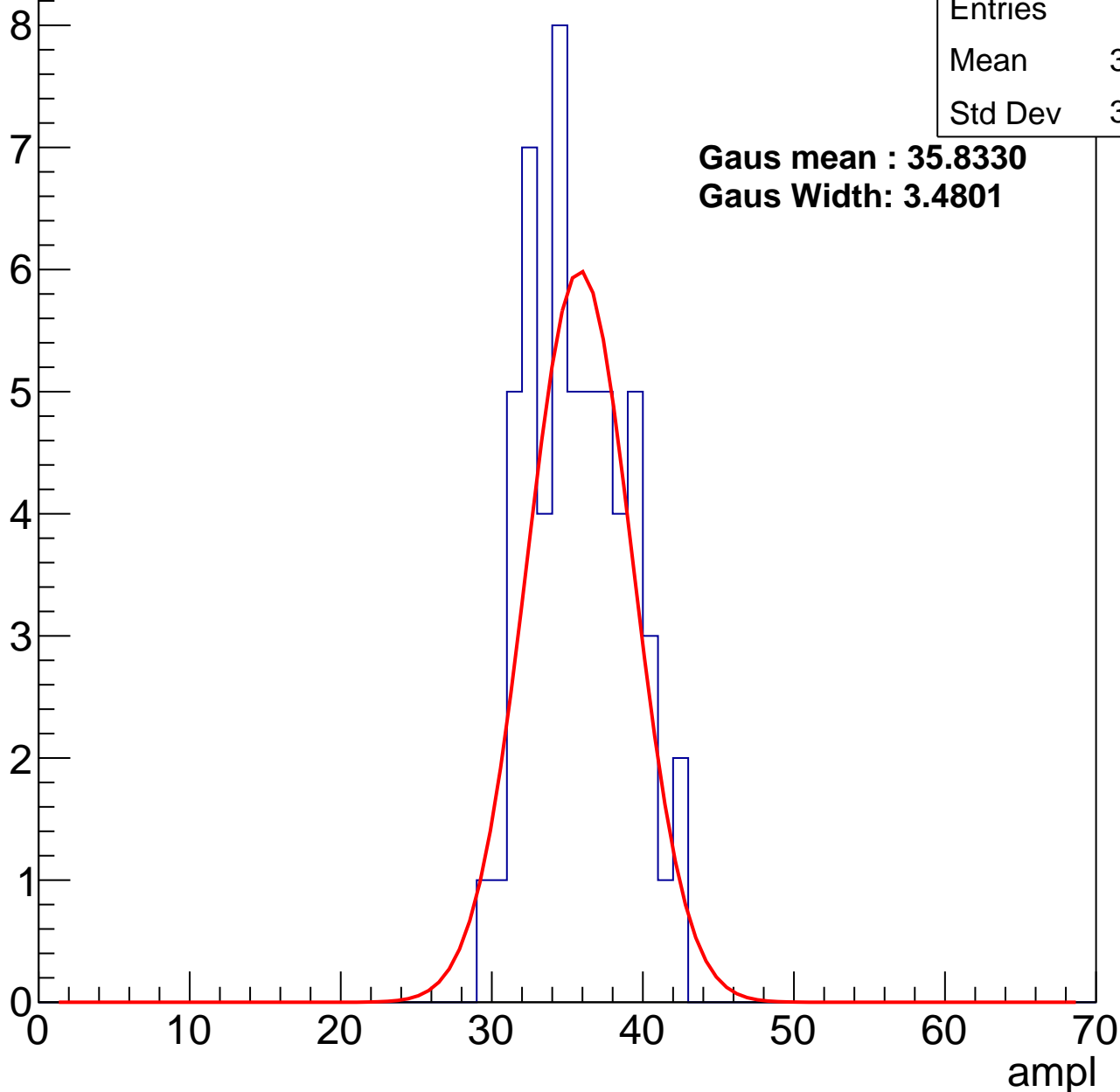
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	35.25
Std Dev	3.203

**Gaus mean : 35.8330**

**Gaus Width: 3.4801**



# B1L101S, U8-ch41, adc2

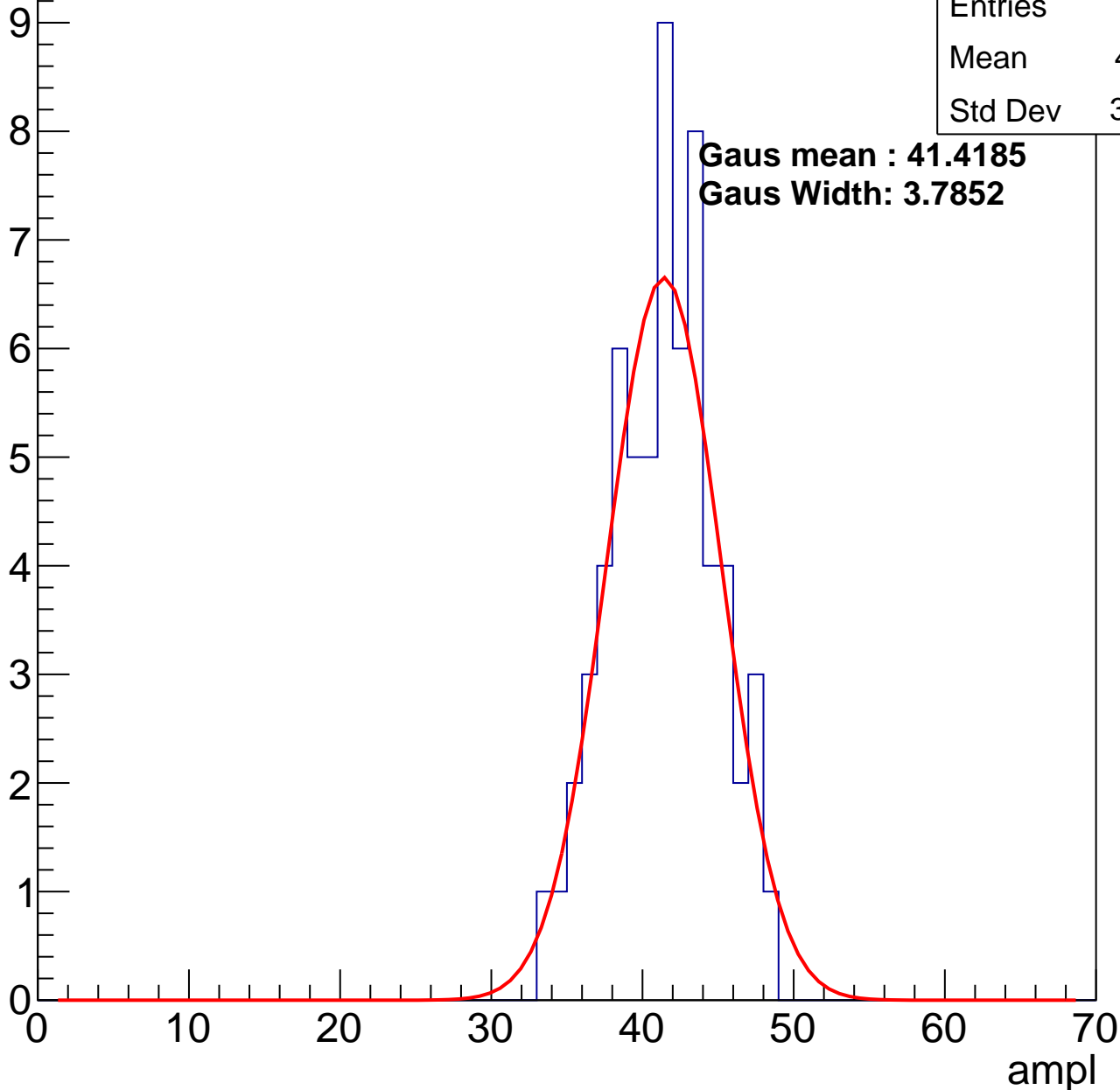
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	40.91
Std Dev	3.417

**Gaus mean : 41.4185**

**Gaus Width: 3.7852**

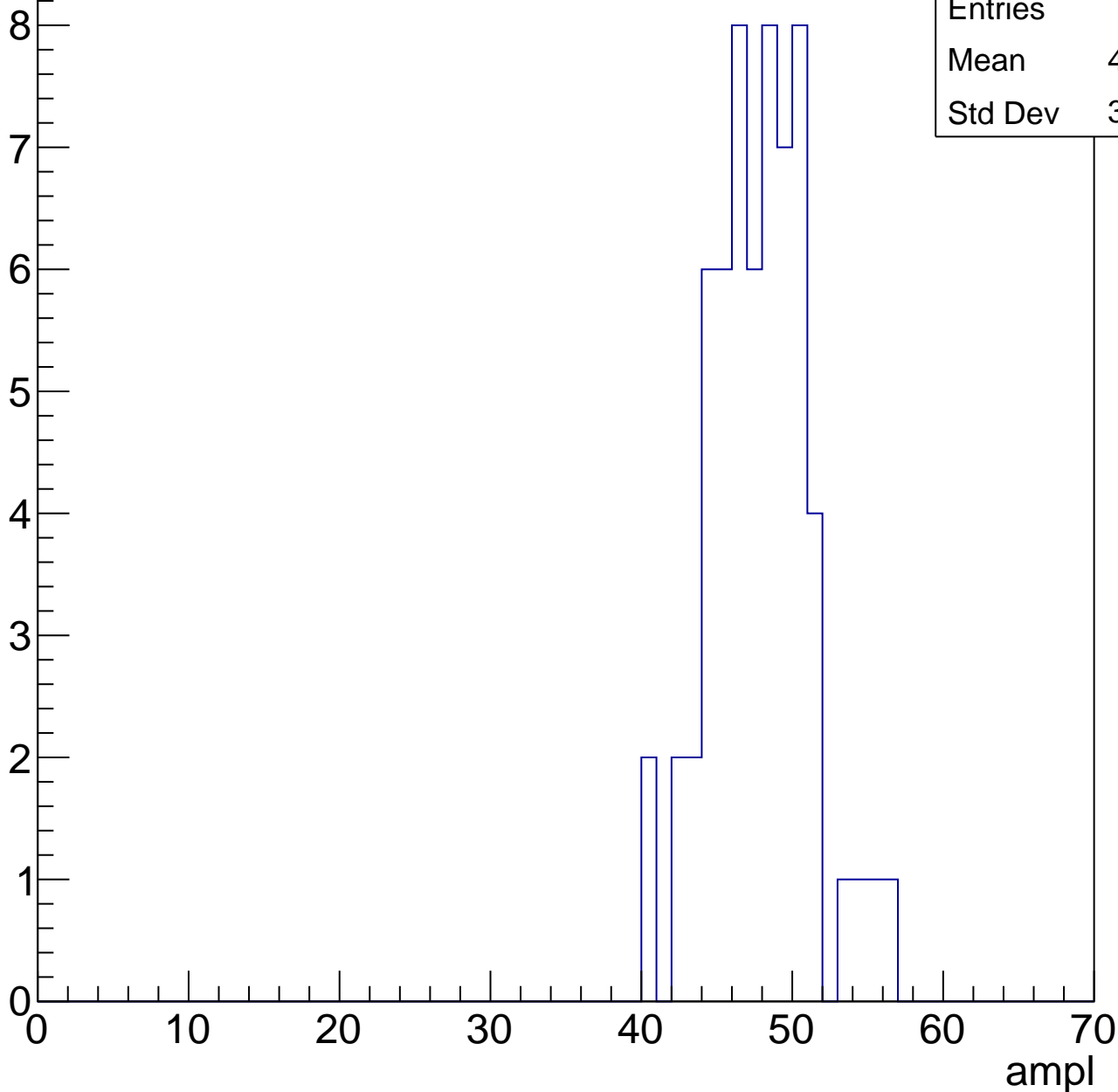


# B1L101S, U8-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	47.35
Std Dev	3.237



# B1L101S, U8-ch41, adc4

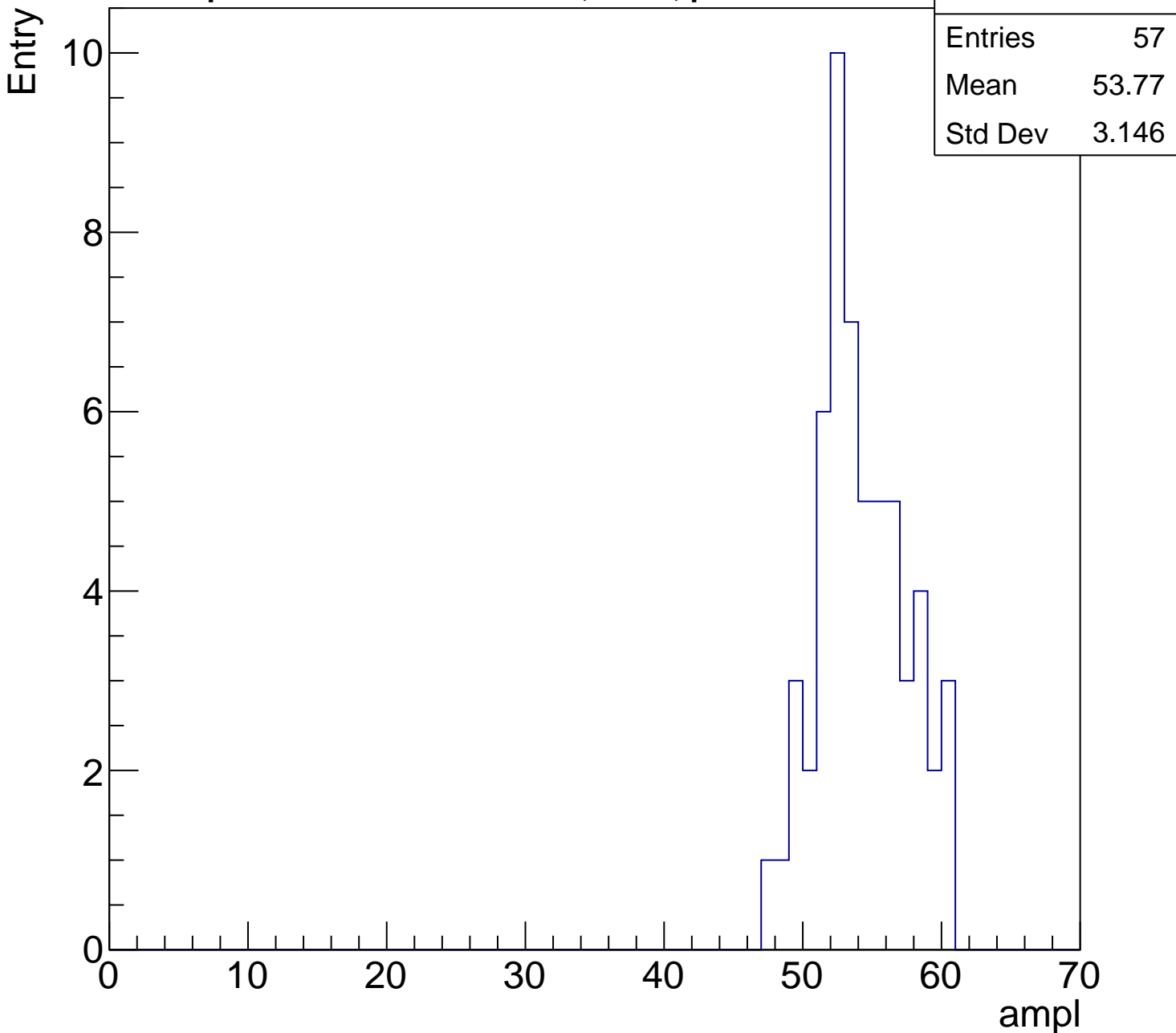
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	57
Mean	53.77
Std Dev	3.146

Entry

10  
8  
6  
4  
2  
0

ampl



# B1L101S, U8-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	61
Mean	58.82
Std Dev	2.86

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

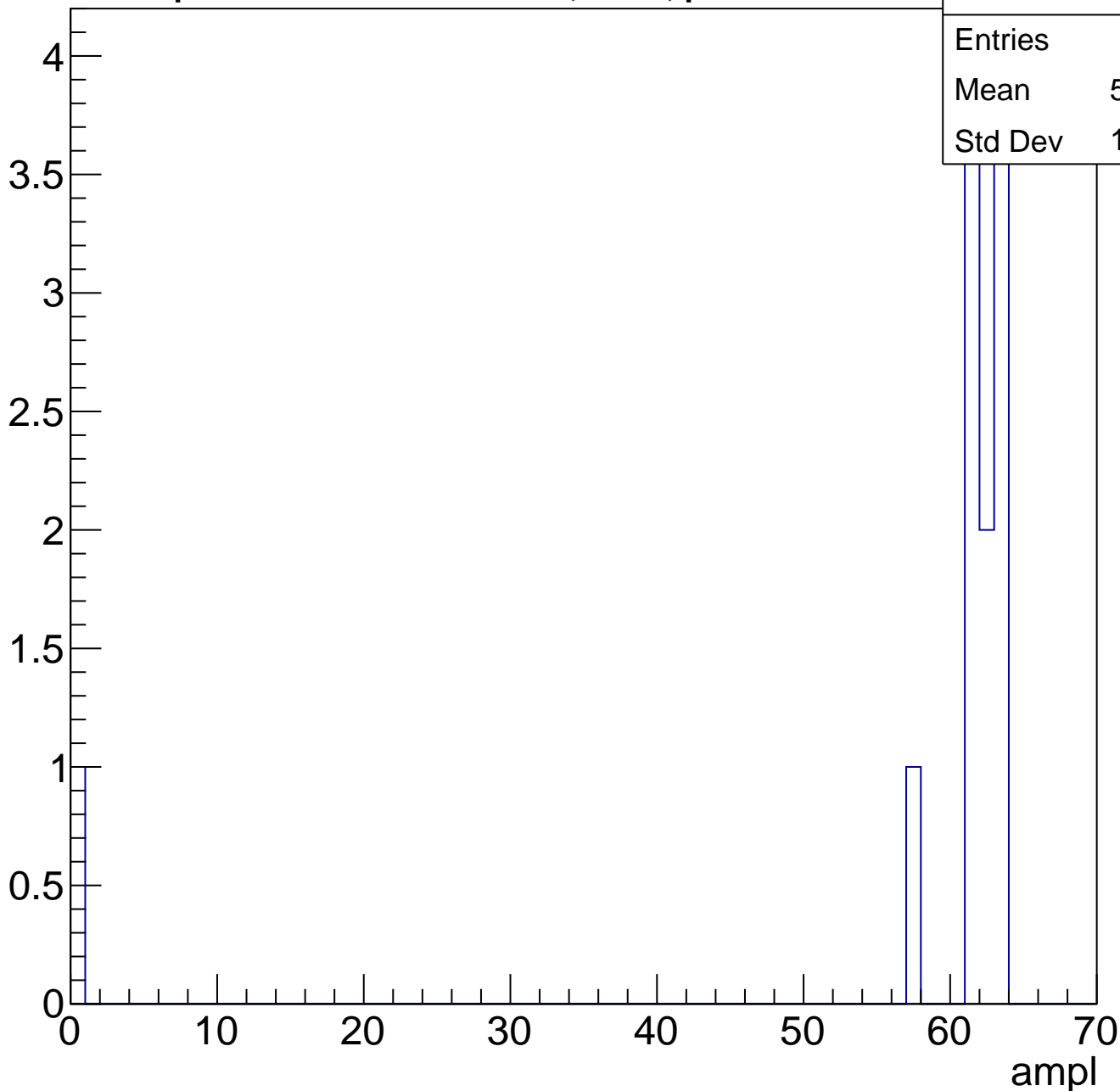
7

8

# B1L101S, U8-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	12
Mean	56.42
Std Dev	17.09



# B1L101S, U8-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch42, adc0

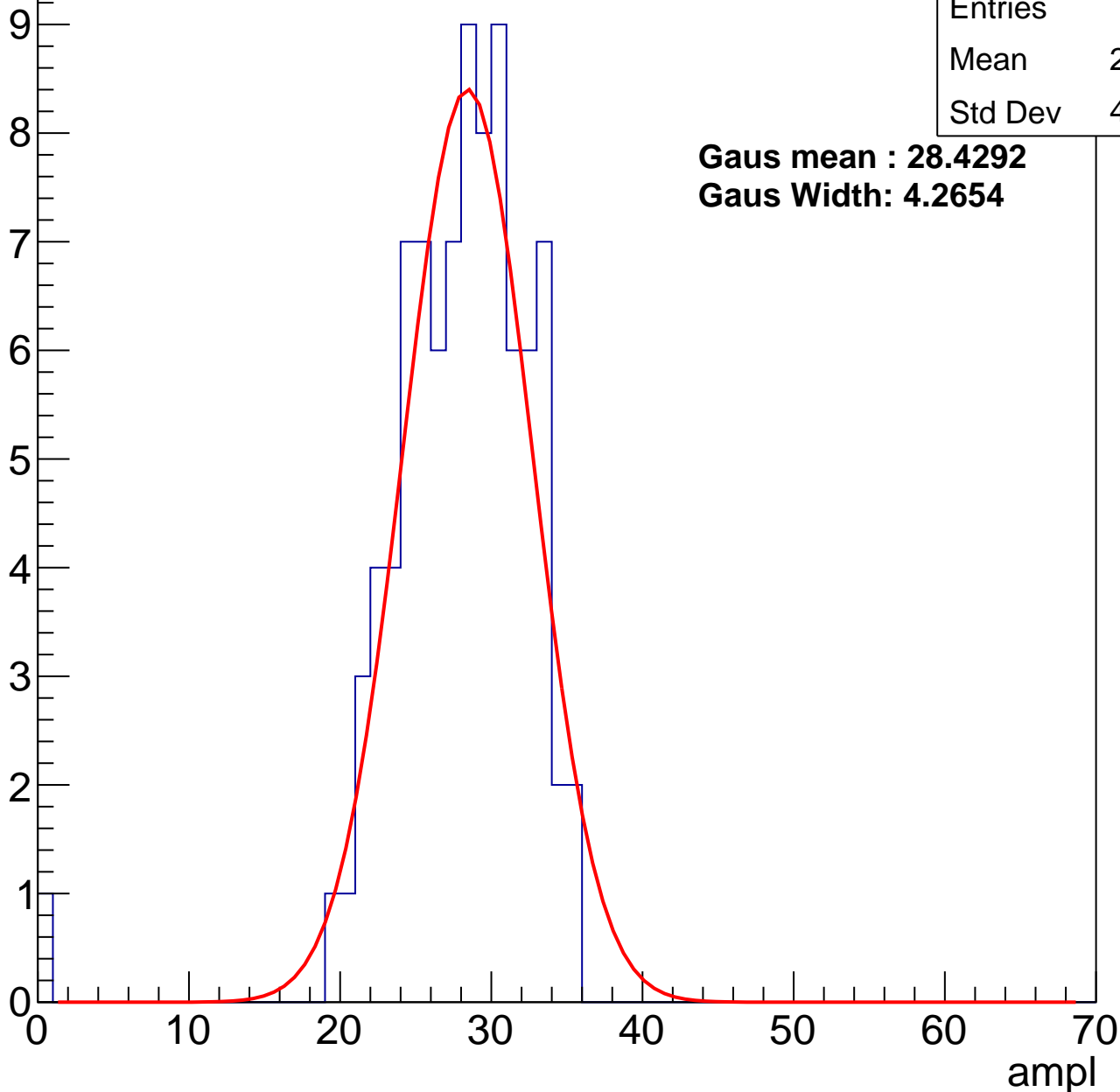
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	90
Mean	27.46
Std Dev	4.759

**Gaus mean : 28.4292**

**Gaus Width: 4.2654**



# B1L101S, U8-ch42, adc1

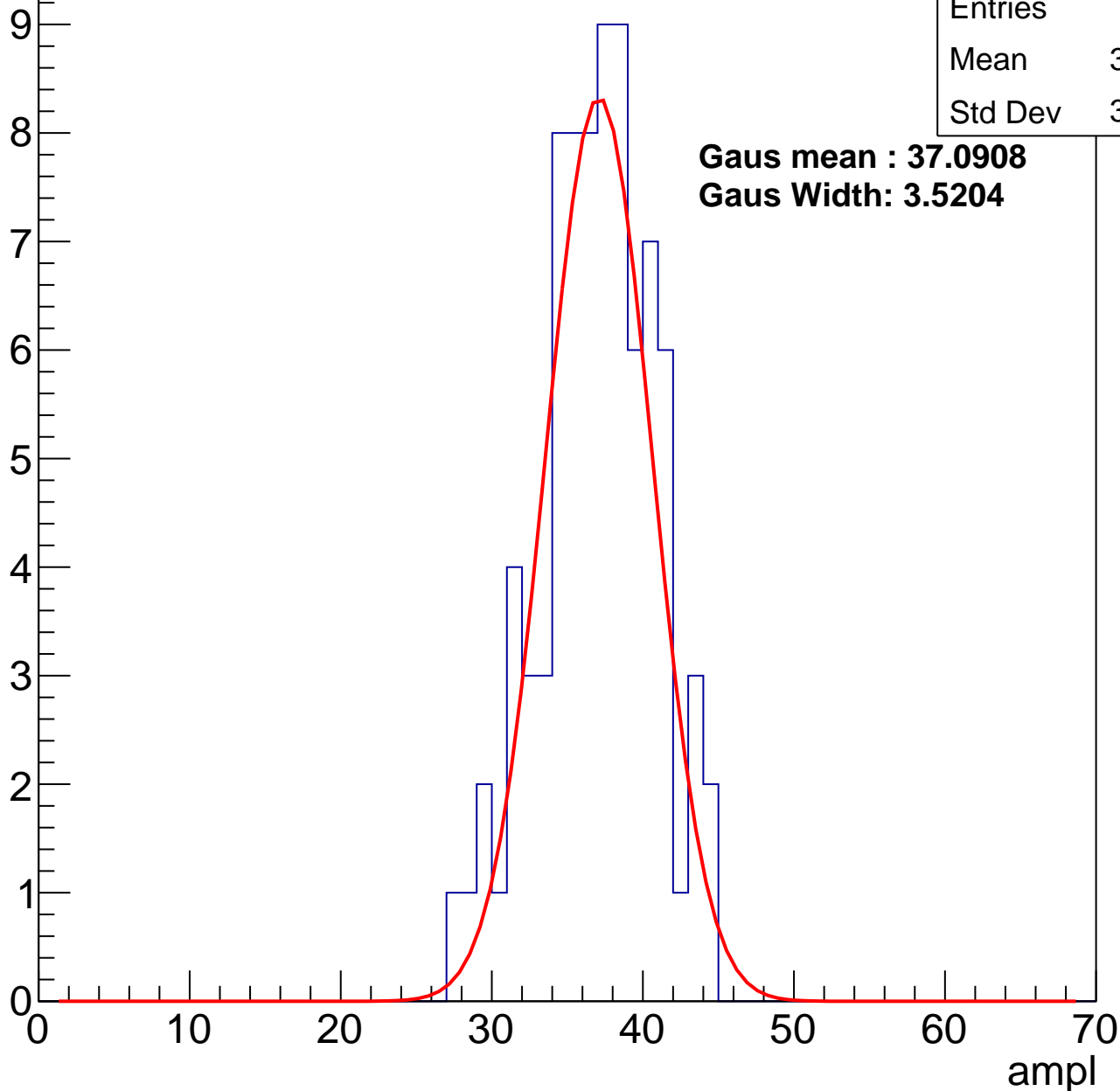
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	36.54
Std Dev	3.733

**Gaus mean : 37.0908**

**Gaus Width: 3.5204**



# B1L101S, U8-ch42, adc2

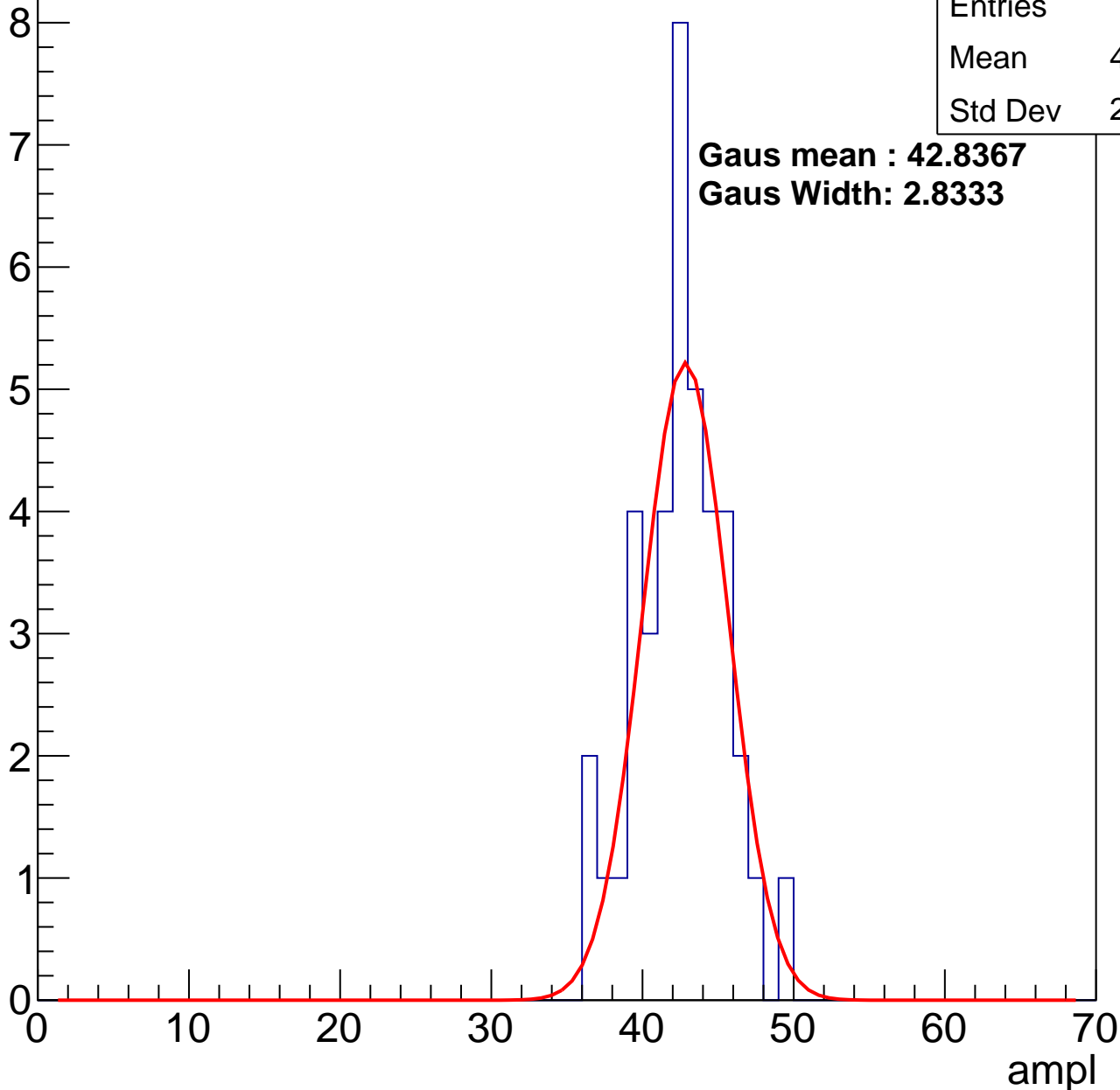
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	40
Mean	42.05
Std Dev	2.863

**Gaus mean : 42.8367**

**Gaus Width: 2.8333**



# B1L101S, U8-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	64
Mean	48.22
Std Dev	3.13

Entry

10

8

6

4

2

0

0

10

20

30

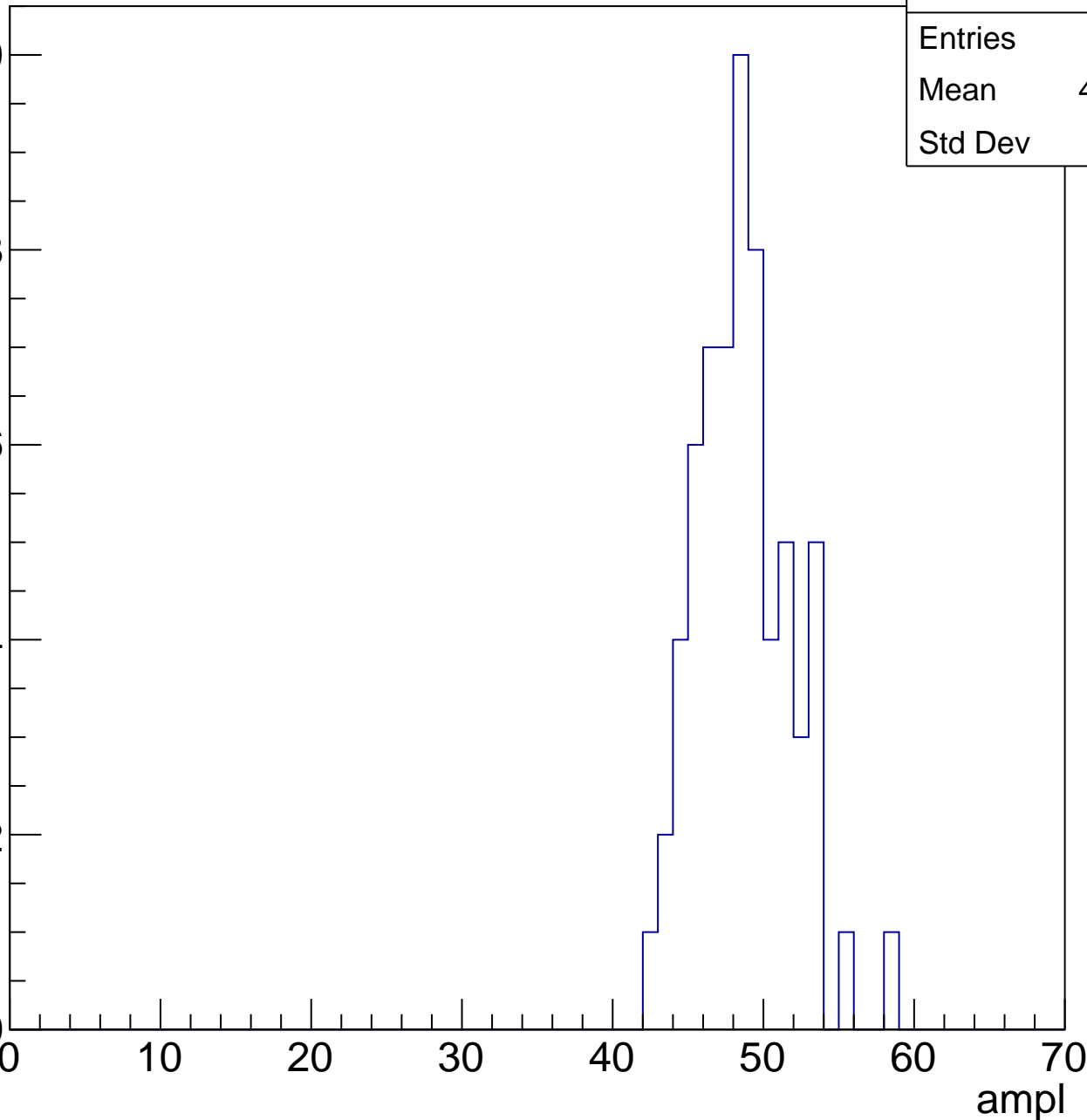
40

50

60

ampl

70

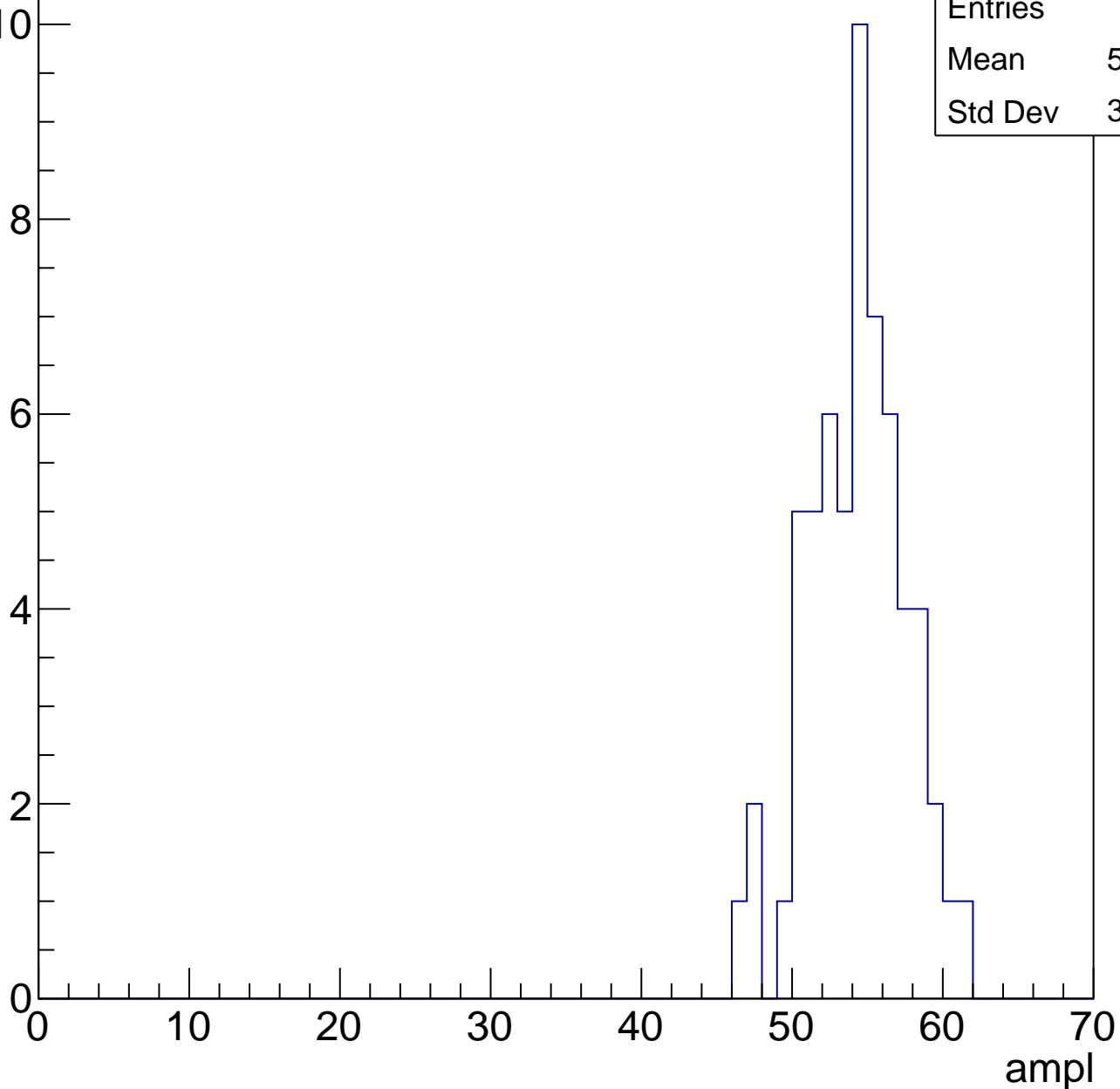


# B1L101S, U8-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	53.85
Std Dev	3.177

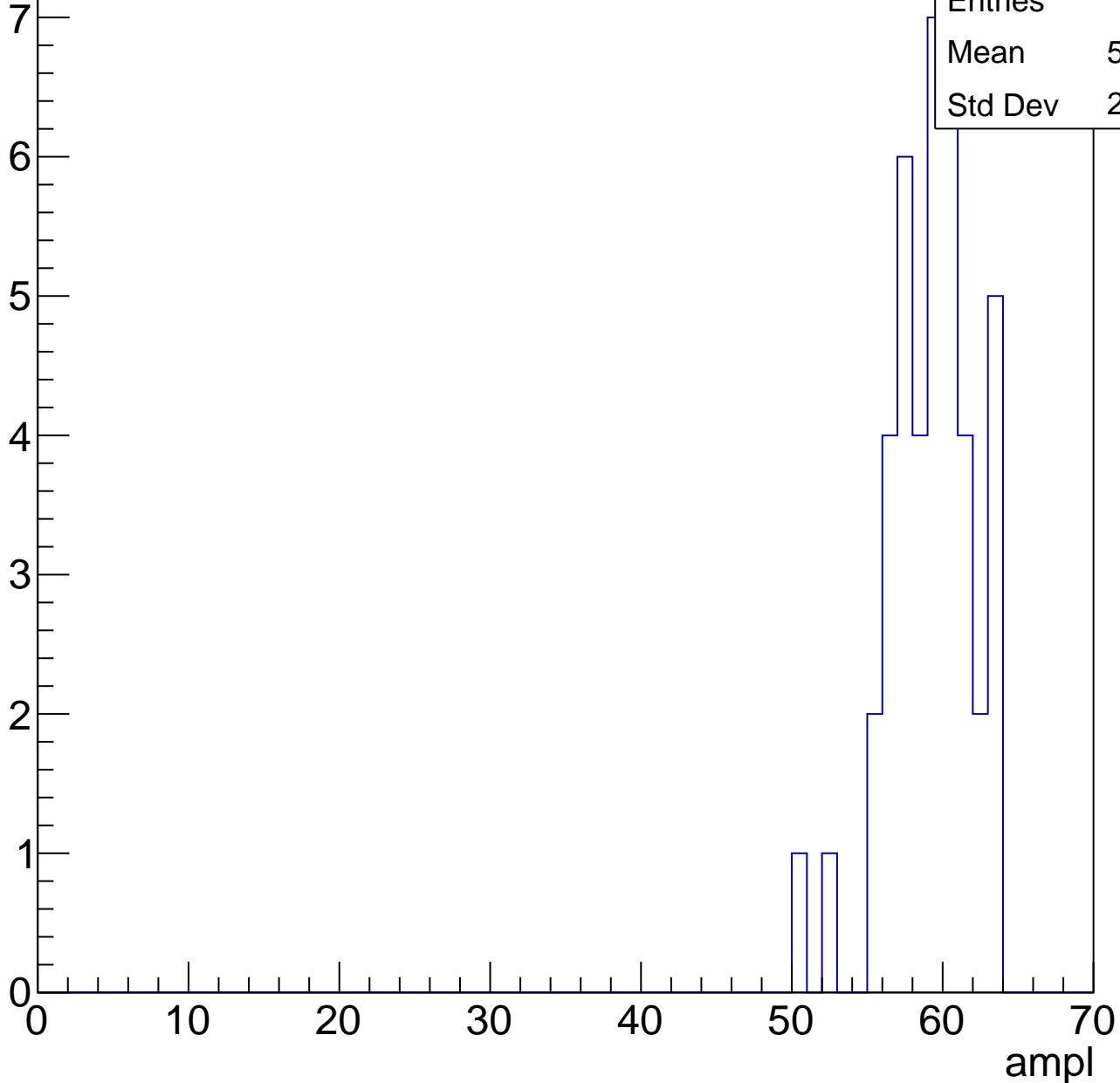


# B1L101S, U8-ch42, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	58.74
Std Dev	2.829

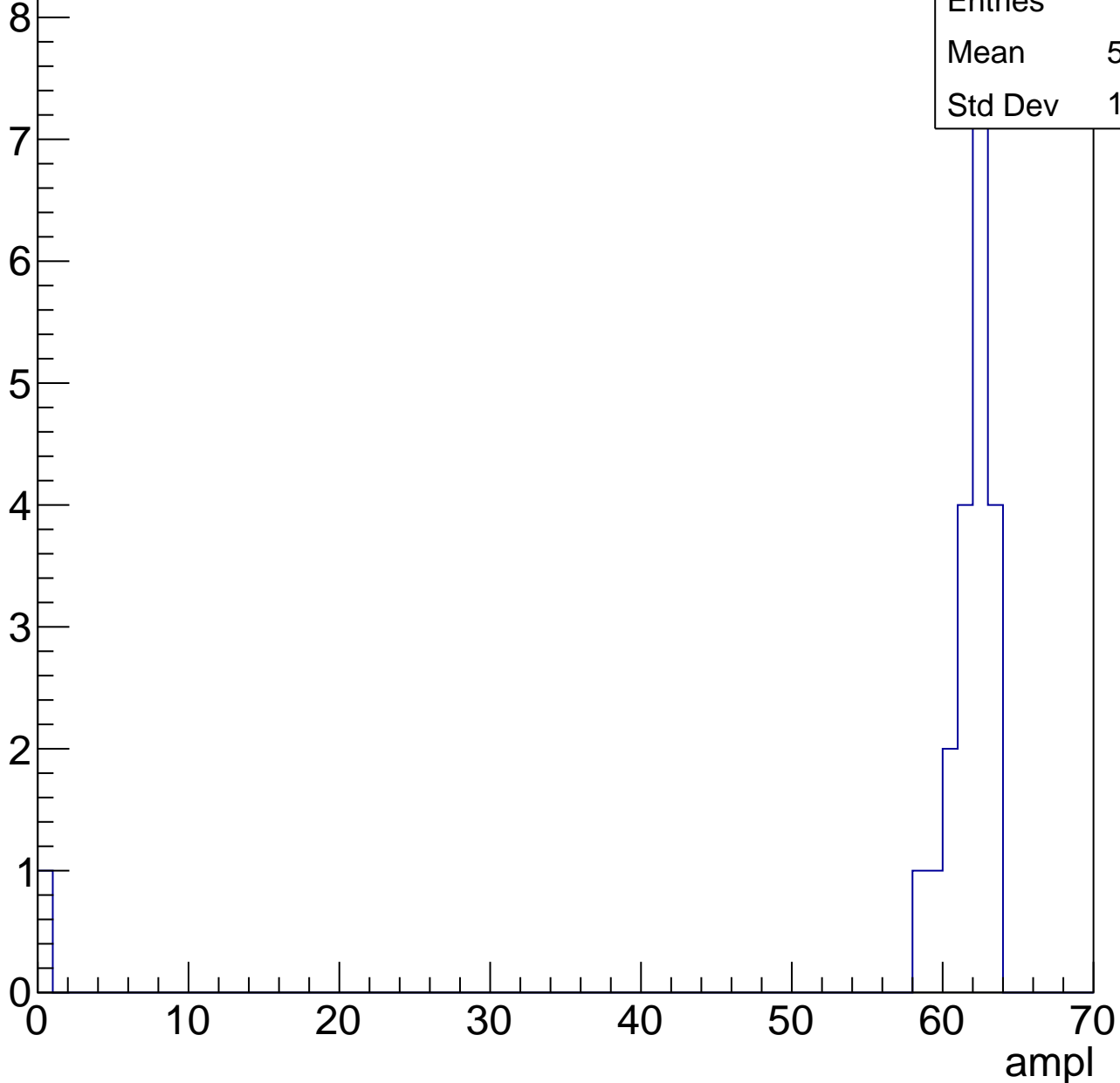


# B1L101S, U8-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	21
Mean	58.52
Std Dev	13.15

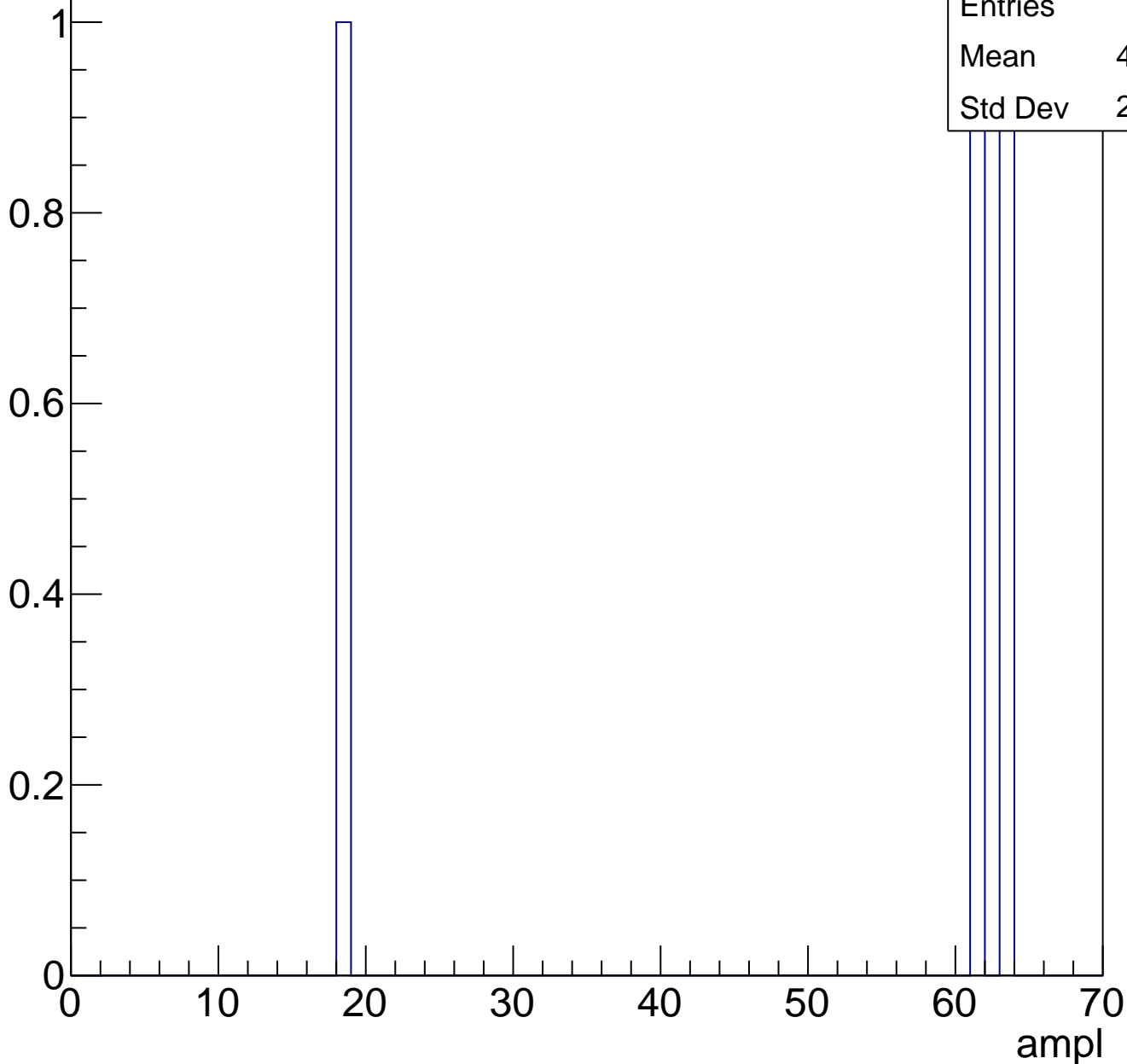




# B1L101S, U8-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch43, adc0

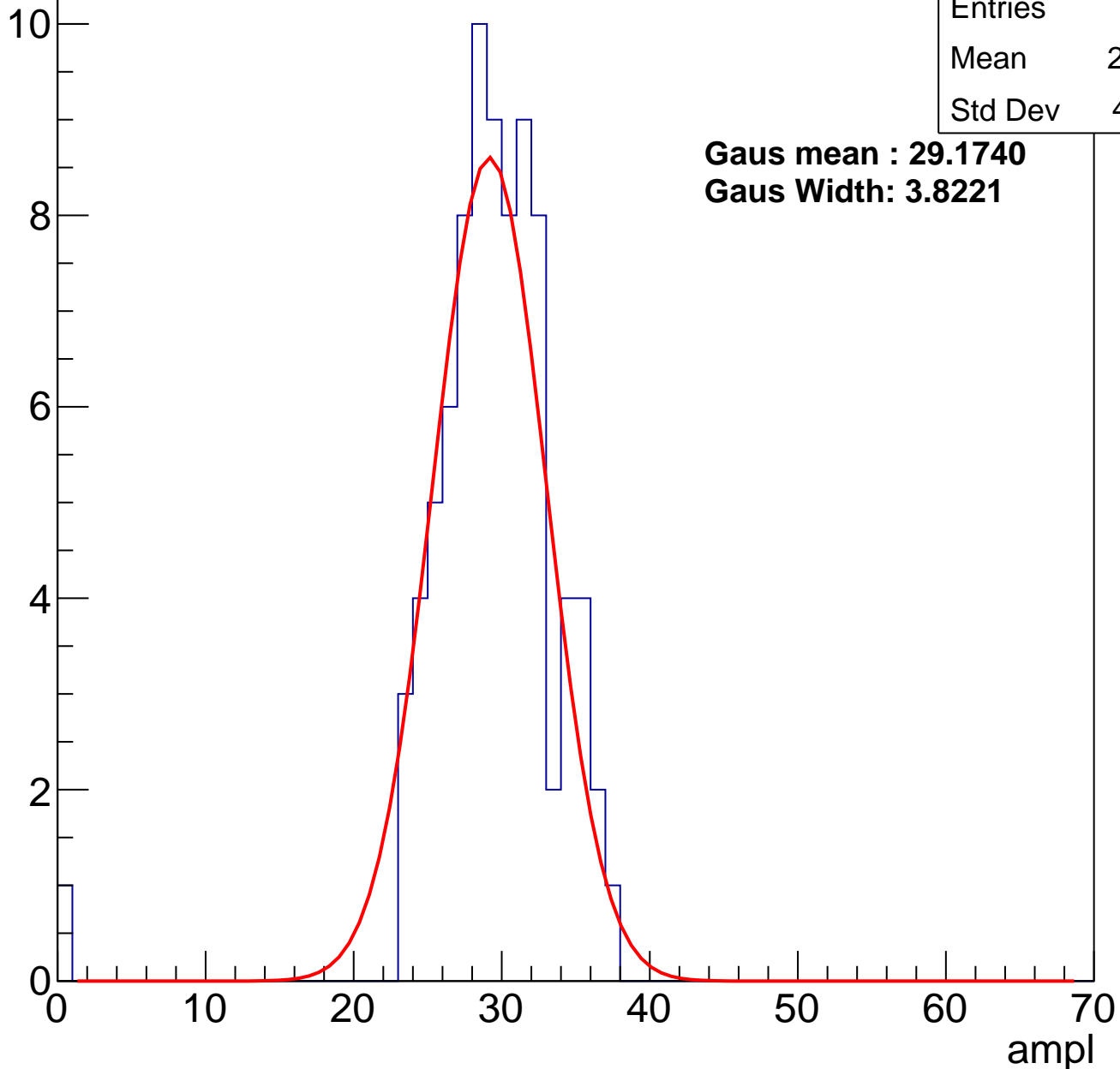
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	84
Mean	28.92
Std Dev	4.601

**Gaus mean : 29.1740**

**Gaus Width: 3.8221**

Entry



# B1L101S, U8-ch43, adc1

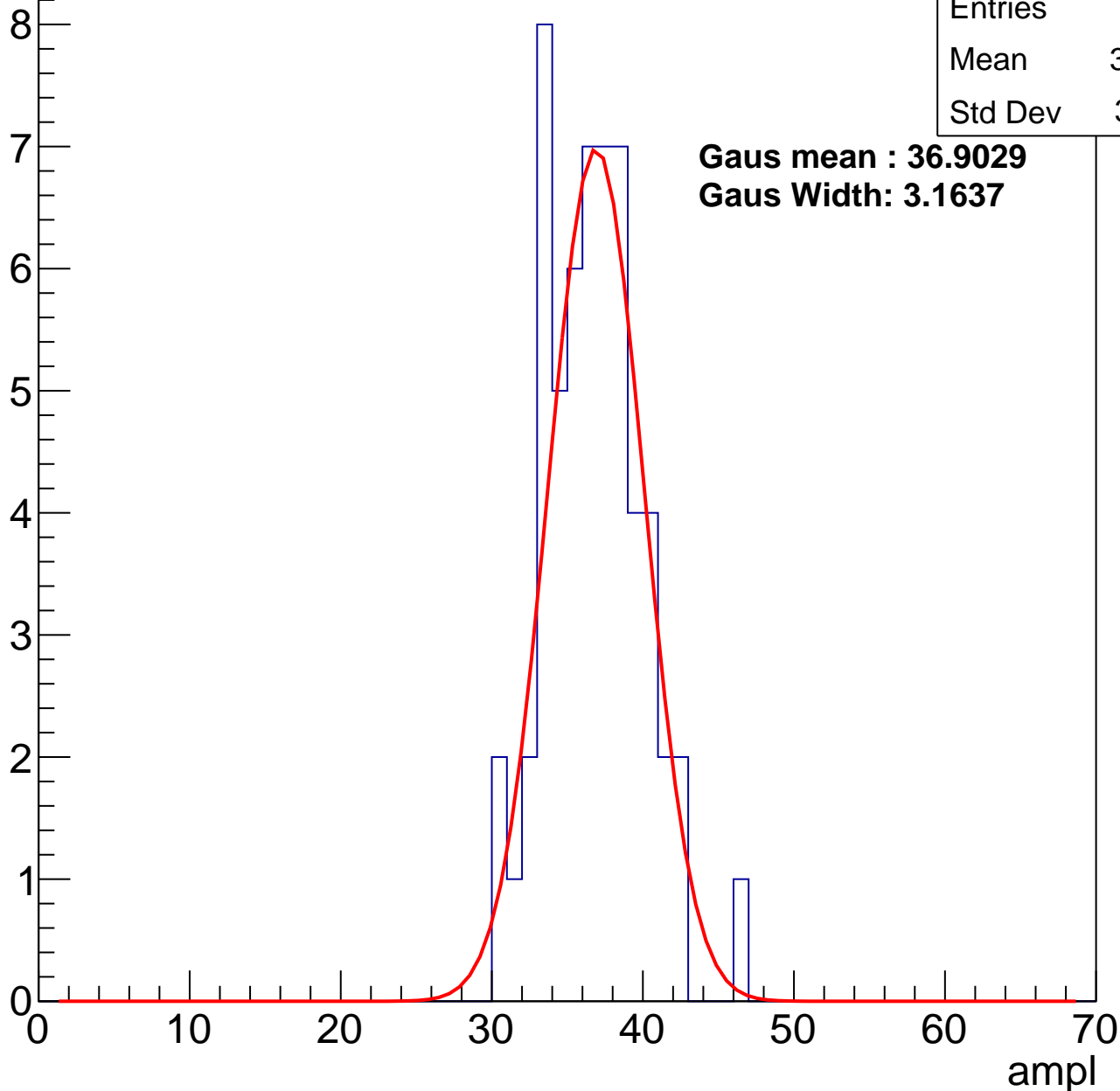
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	36.28
Std Dev	3.161

**Gaus mean : 36.9029**

**Gaus Width: 3.1637**



# B1L101S, U8-ch43, adc2

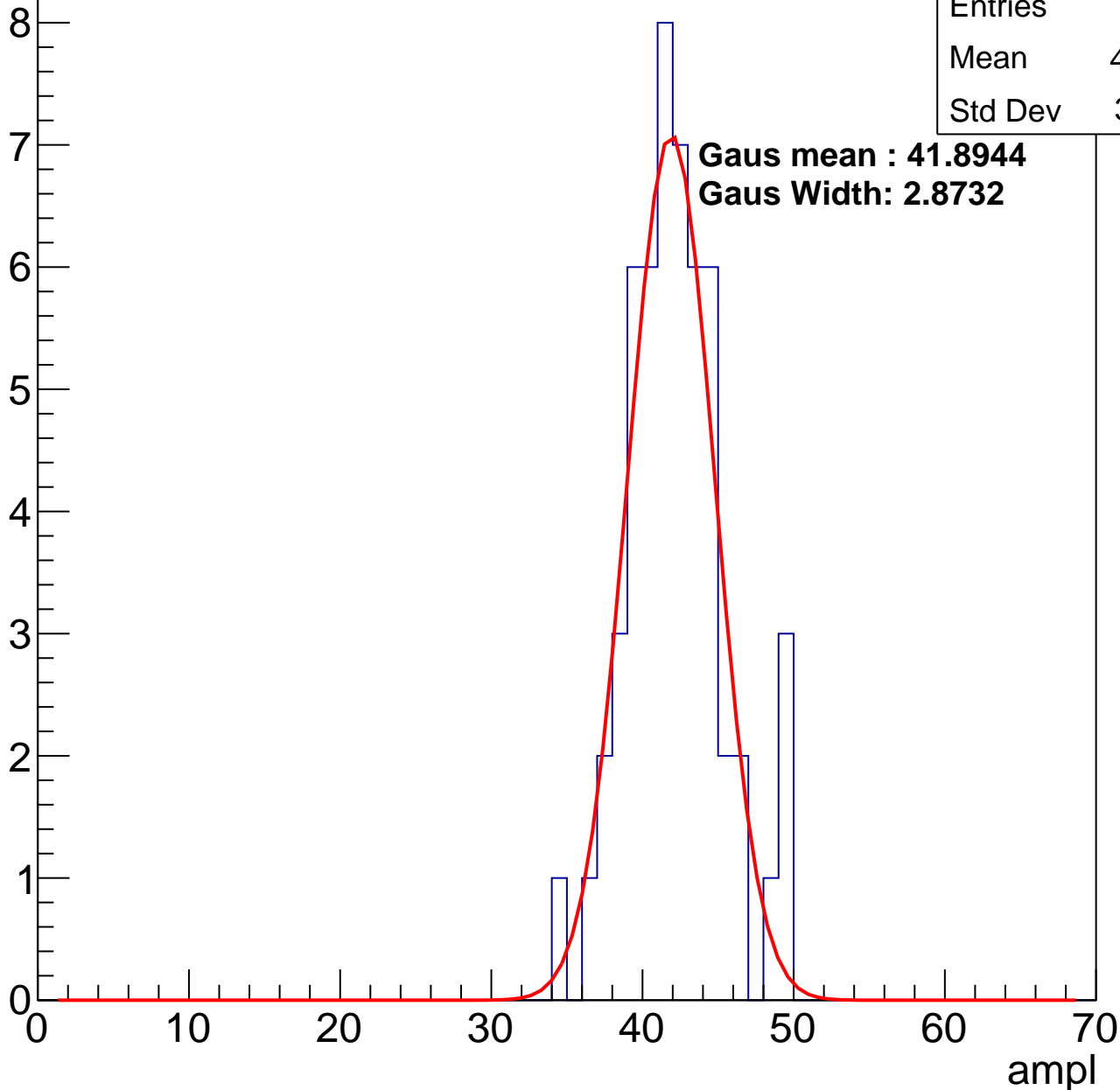
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	41.72
Std Dev	3.171

**Gaus mean : 41.8944**

**Gaus Width: 2.8732**



# B1L101S, U8-ch43, adc3

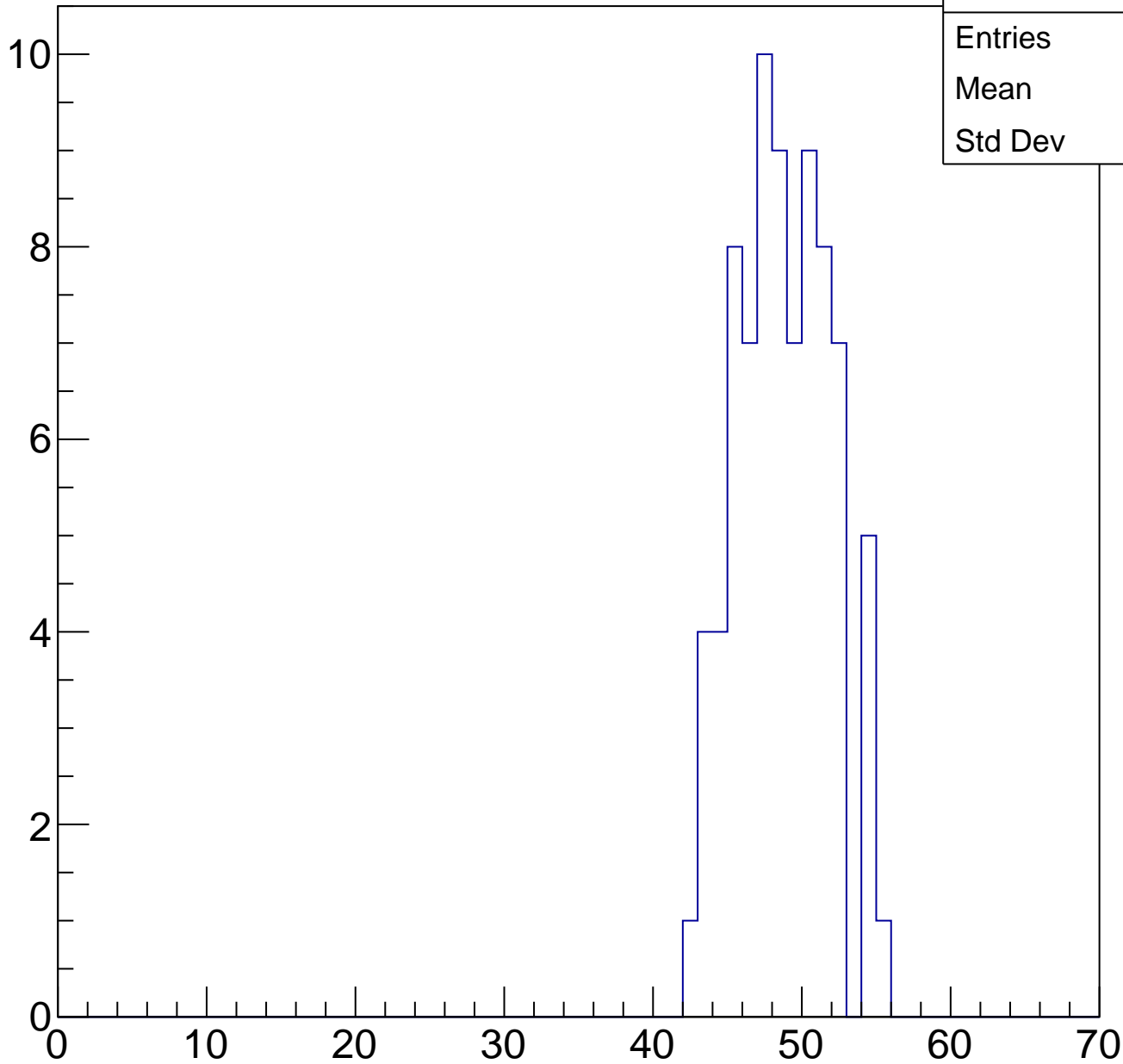
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

10  
8  
6  
4  
2  
0

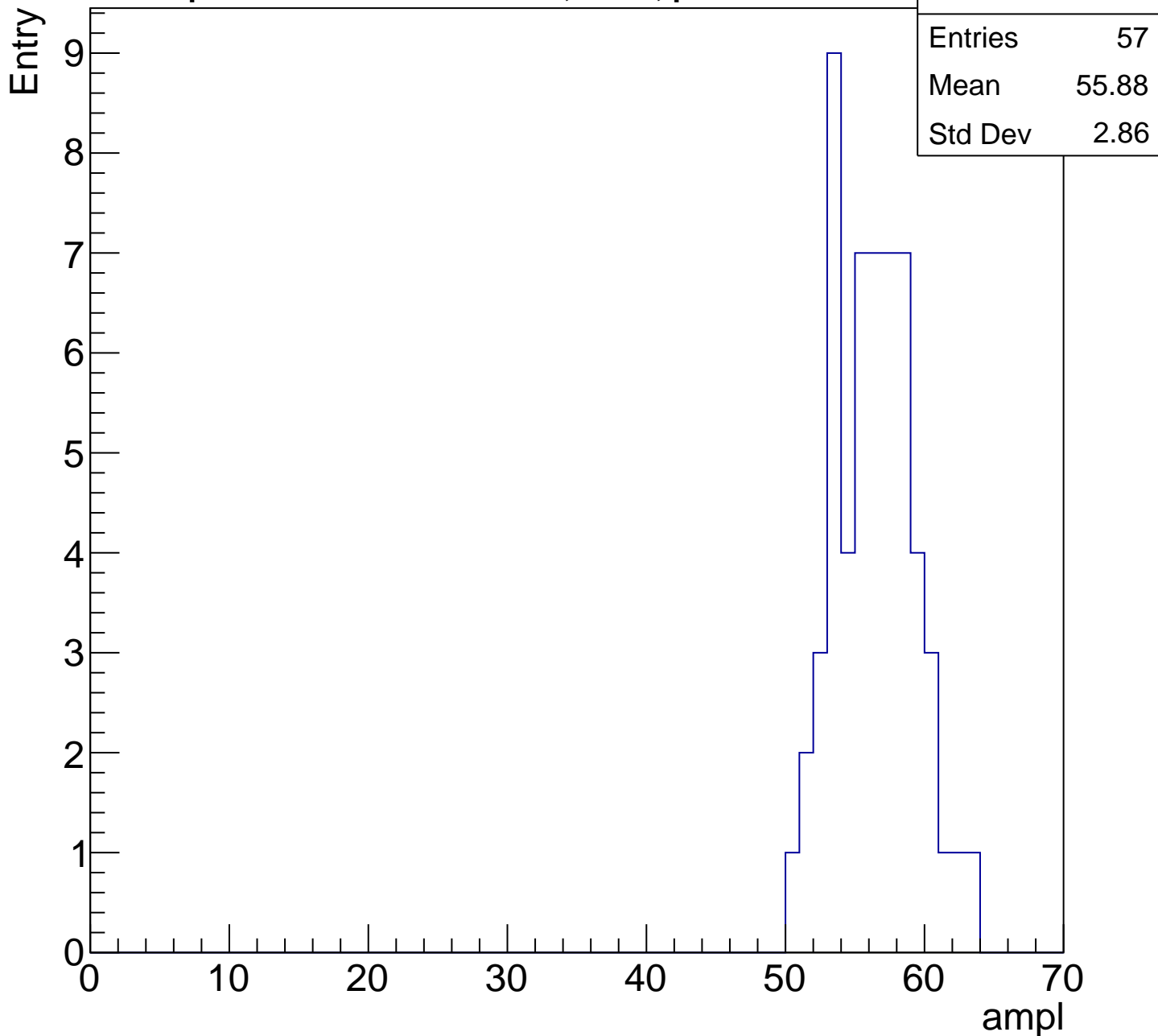
Entries	80
Mean	48.3
Std Dev	3.08

ampl



# B1L101S, U8-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U8-ch43, adc5

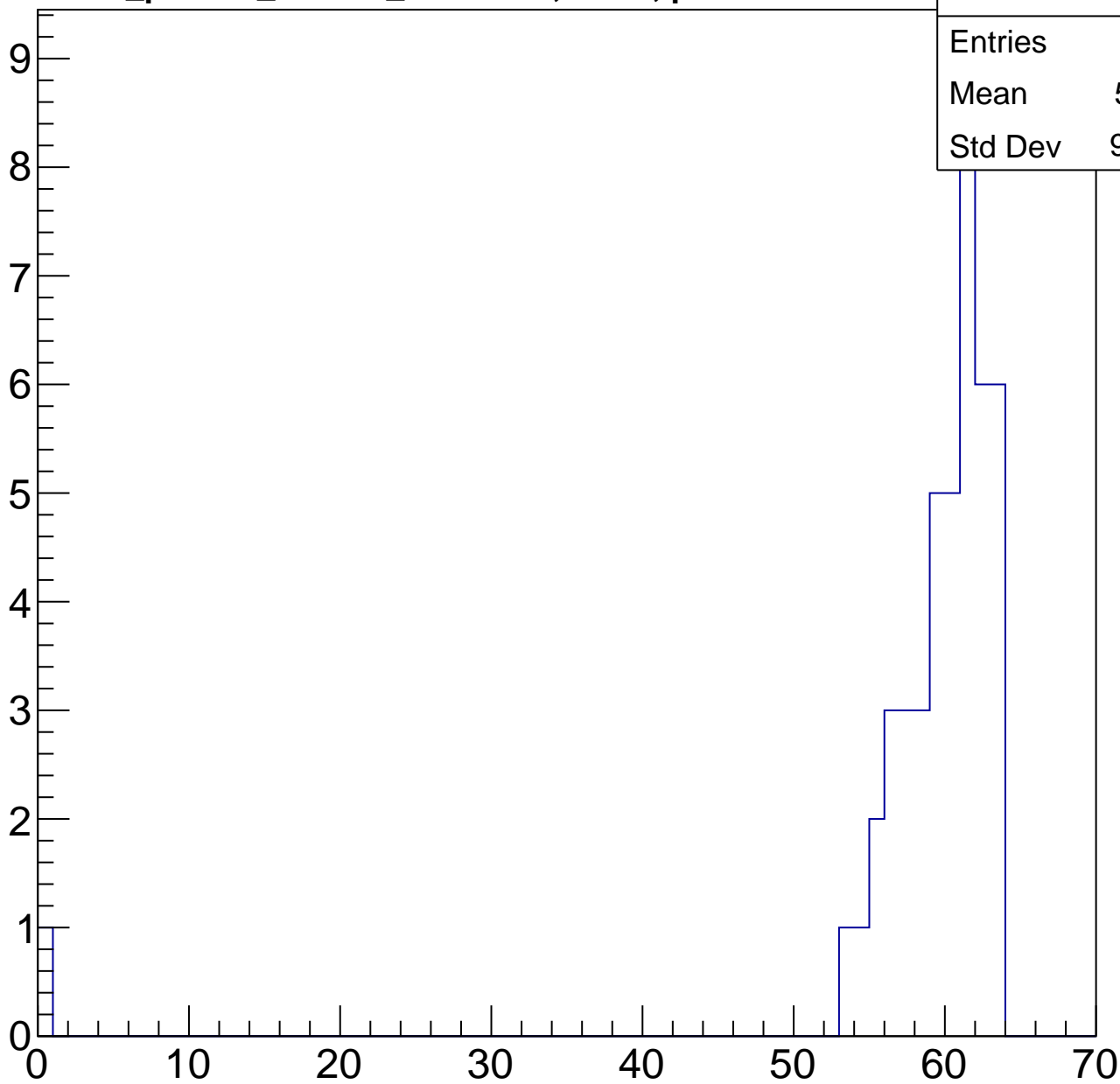
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	45
Mean	58.31
Std Dev	9.172

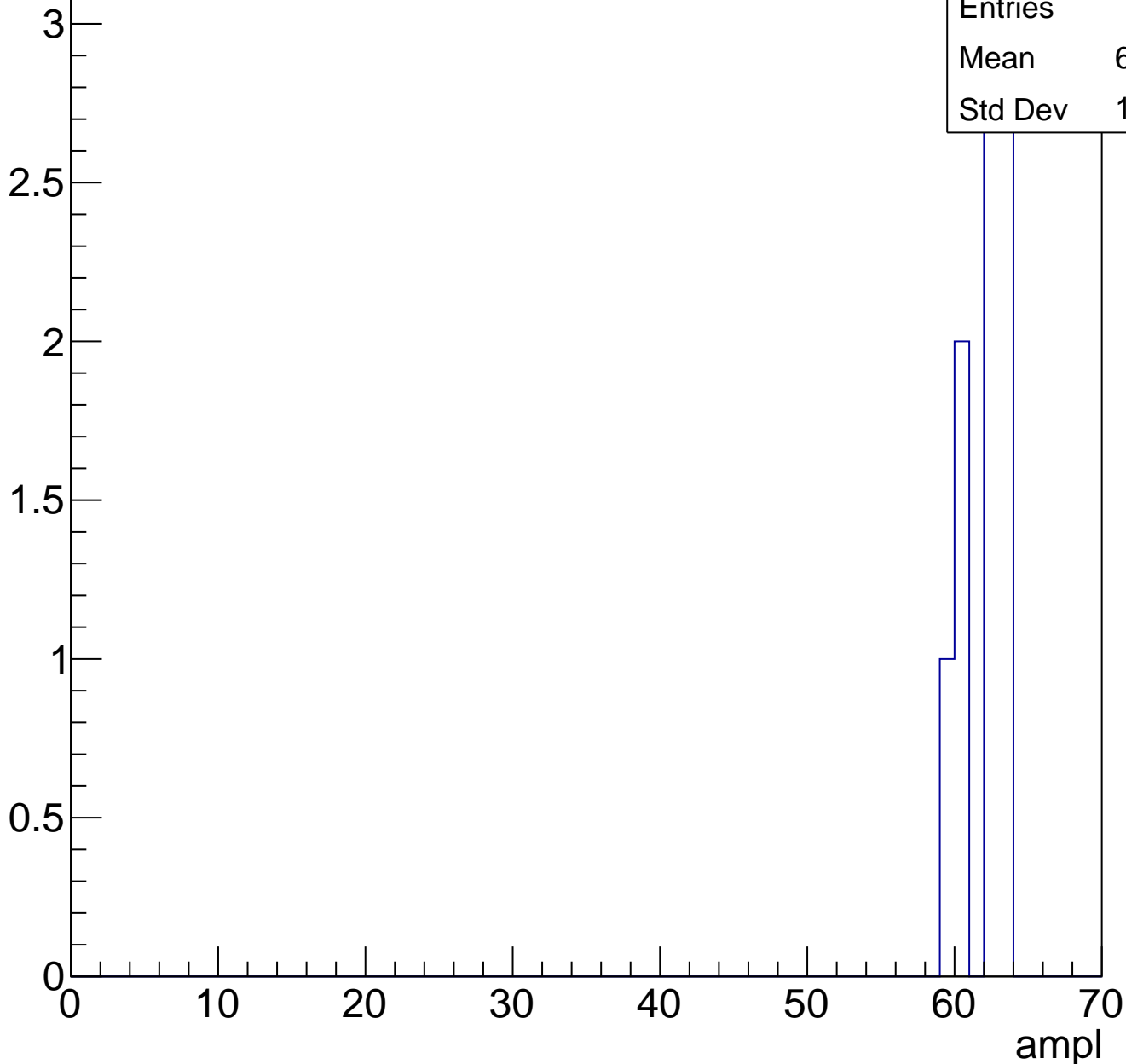
ampl



# B1L101S, U8-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U8-ch44, adc0

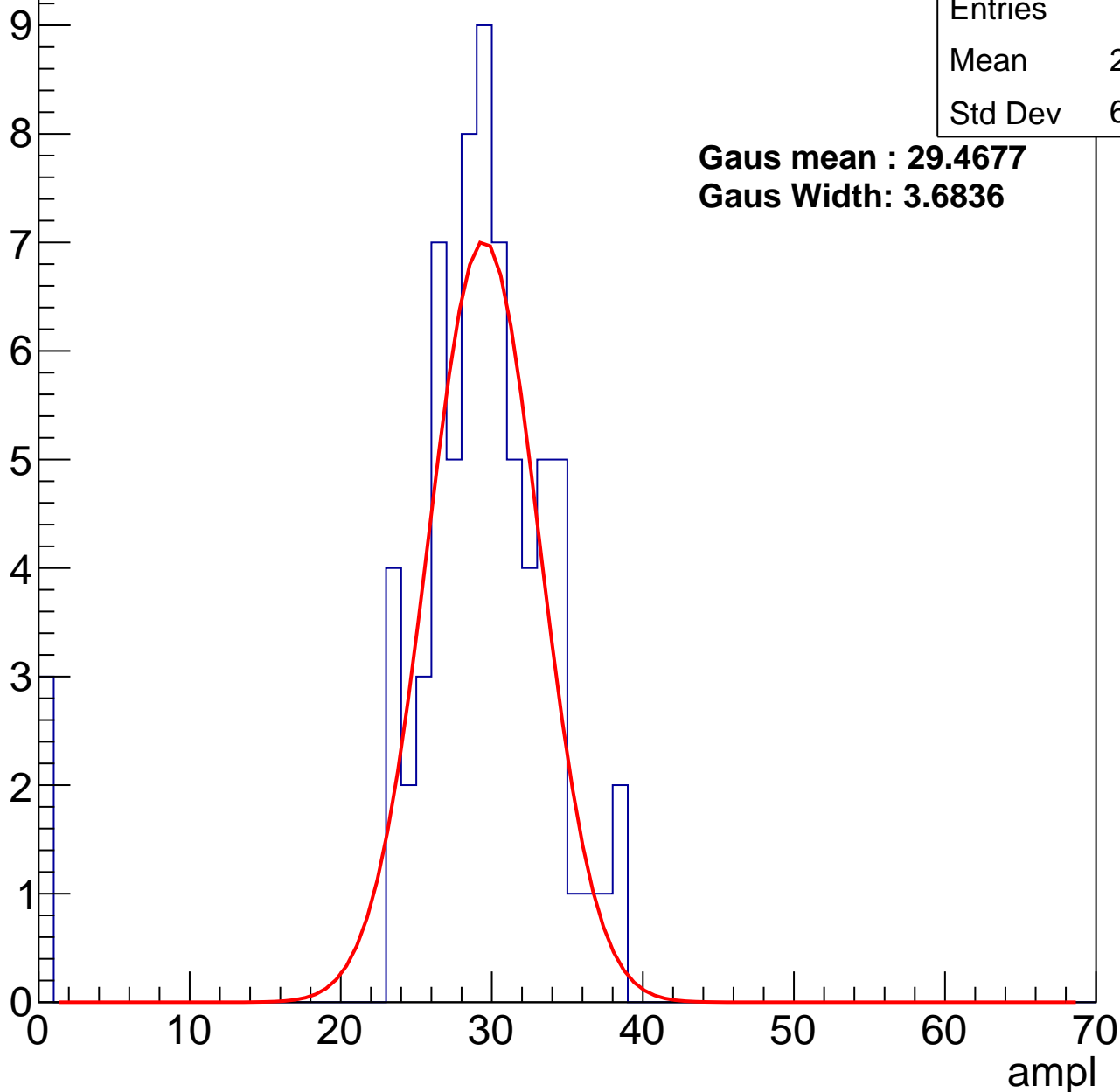
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	28.18
Std Dev	6.858

**Gaus mean : 29.4677**

**Gaus Width: 3.6836**



# B1L101S, U8-ch44, adc1

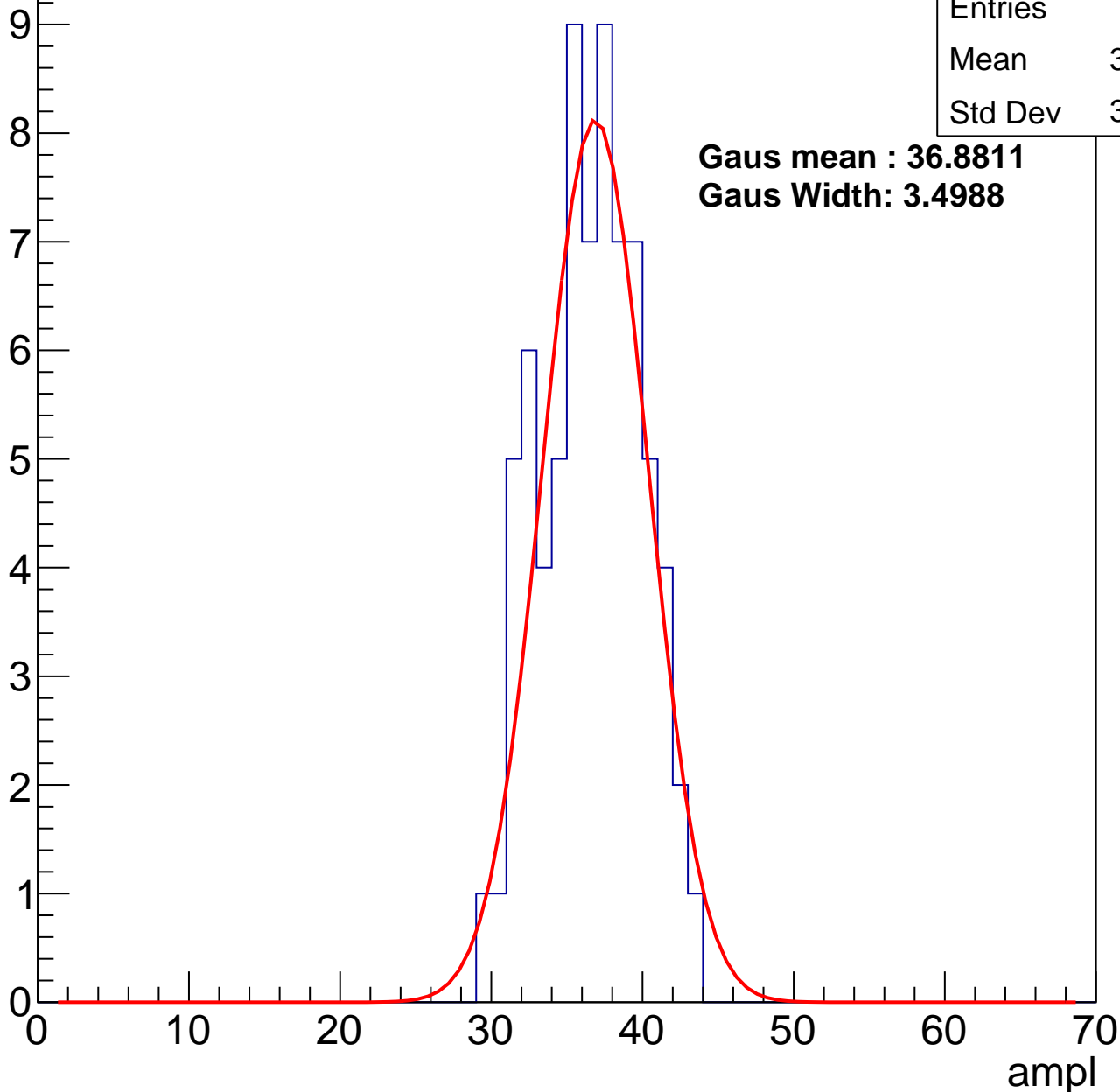
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	36.14
Std Dev	3.249

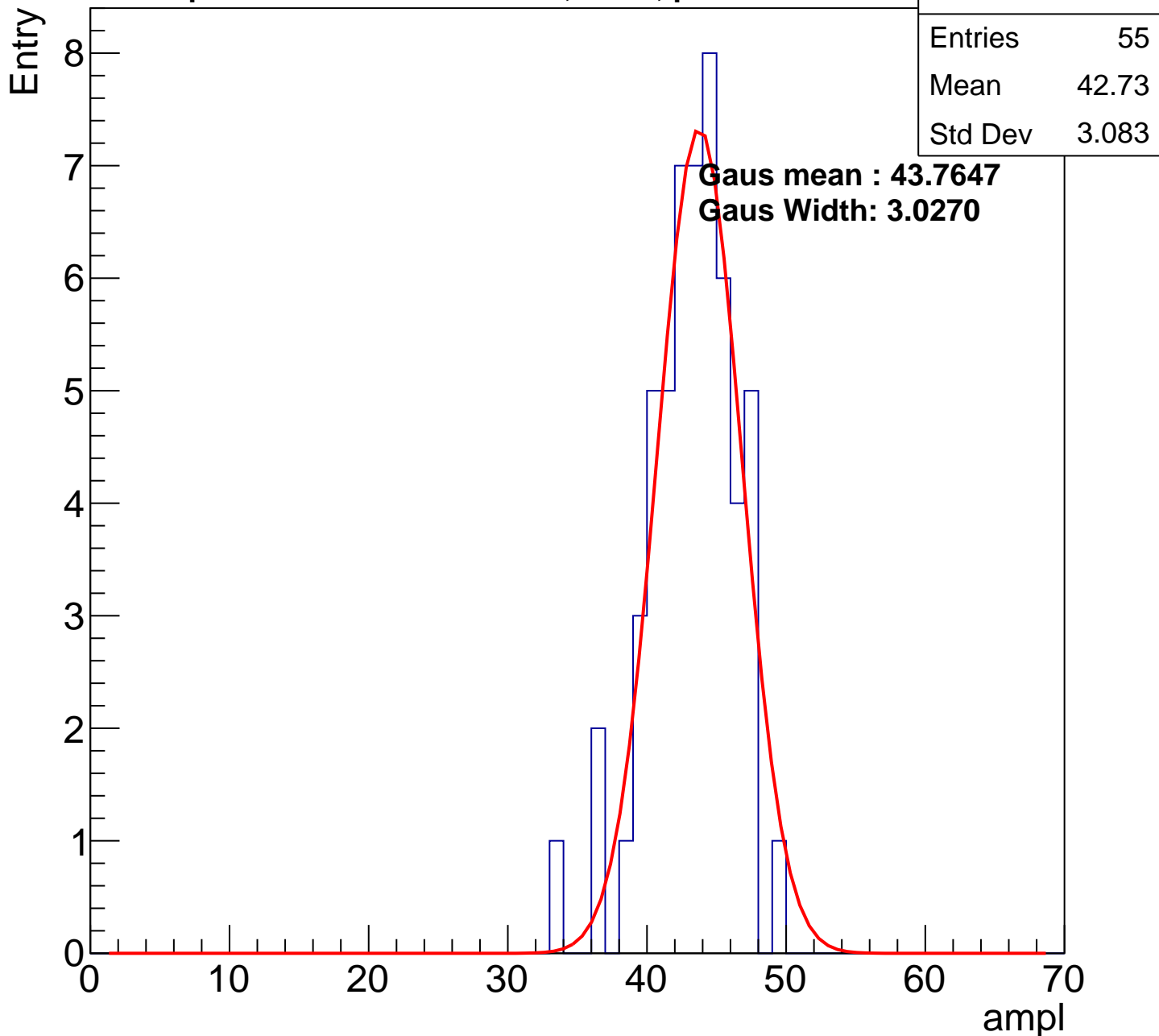
**Gaus mean : 36.8811**

**Gaus Width: 3.4988**



# B1L101S, U8-ch44, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

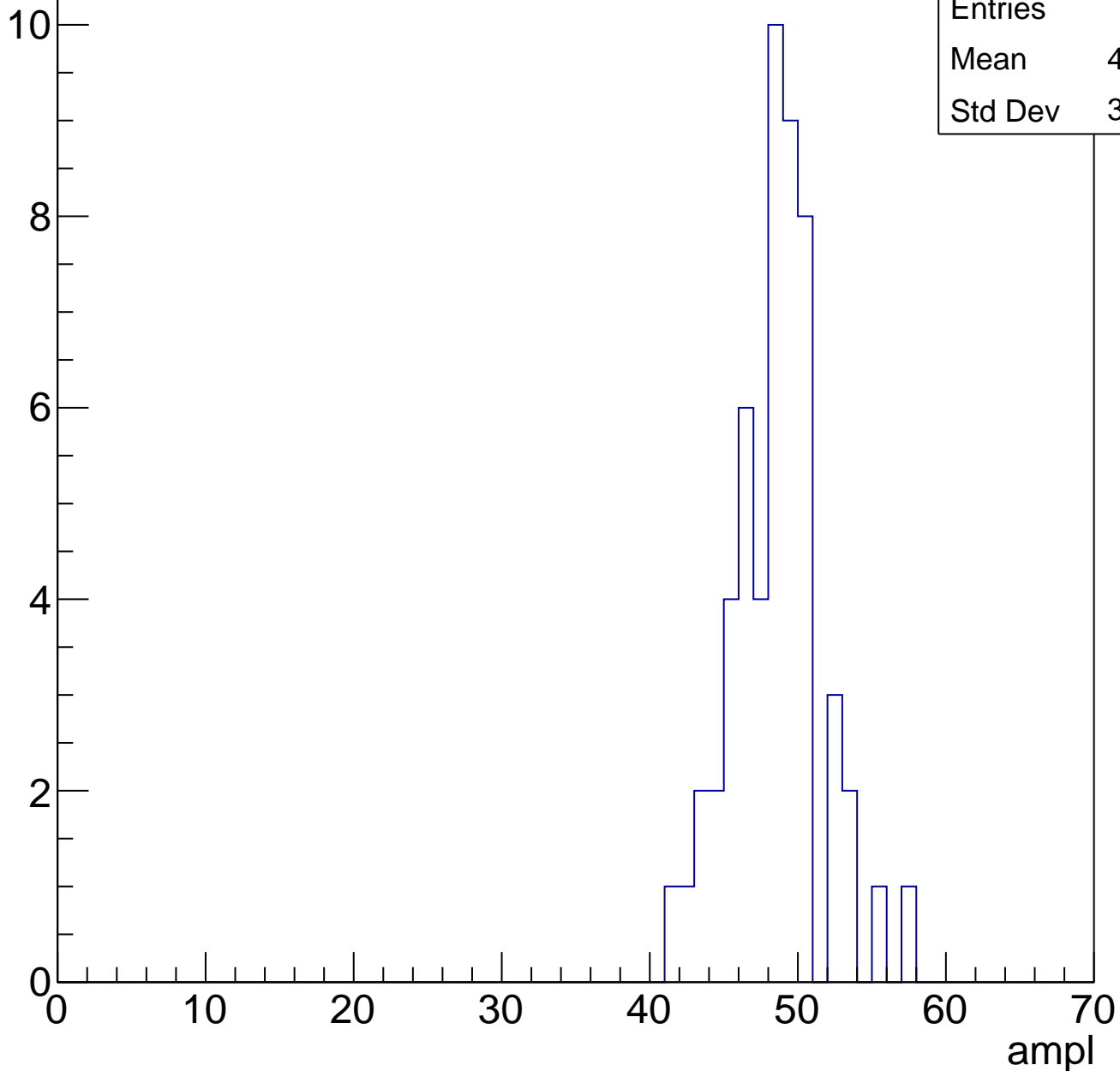


# B1L101S, U8-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	54
Mean	48.07
Std Dev	3.042

Entry

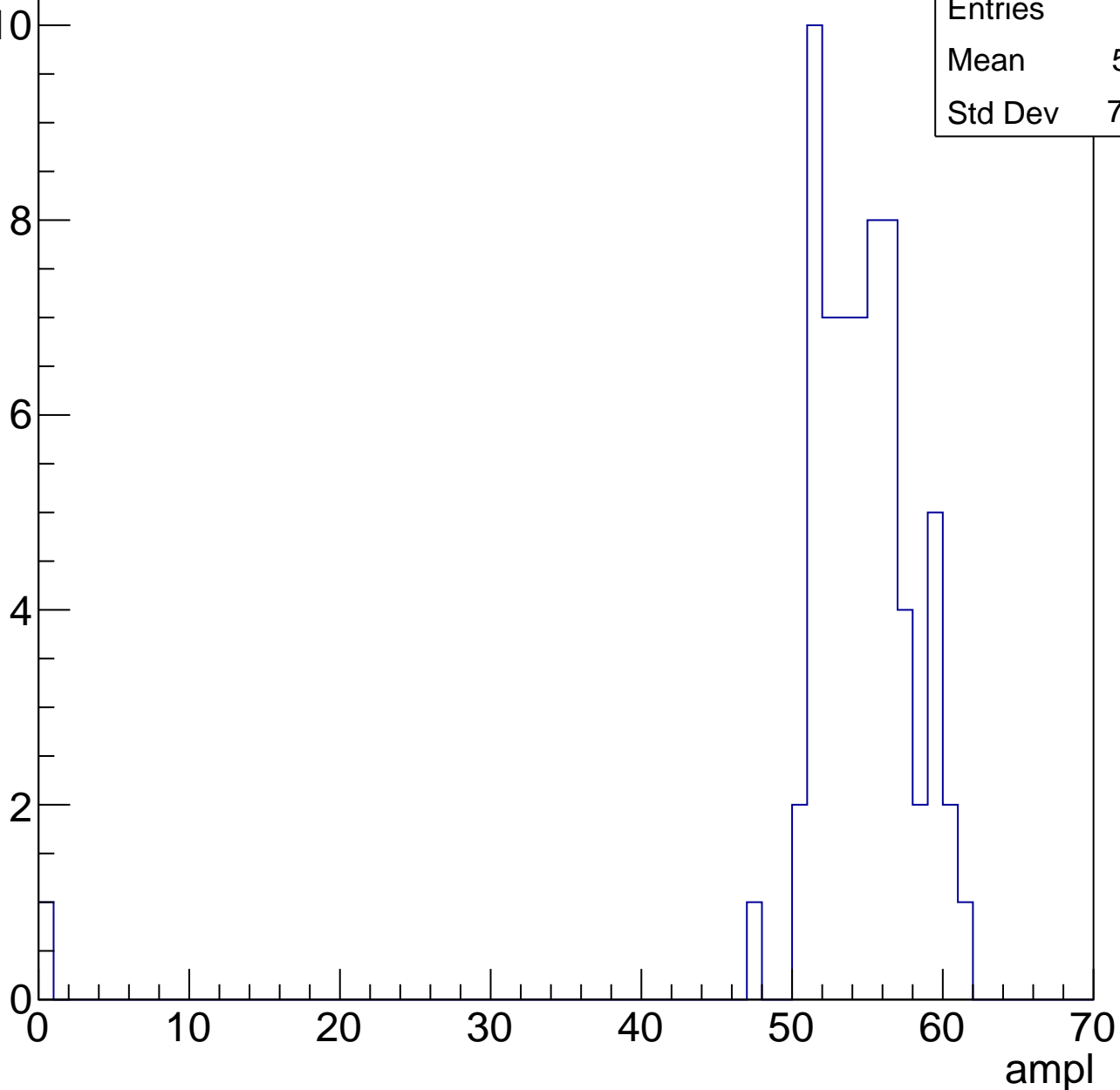


# B1L101S, U8-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

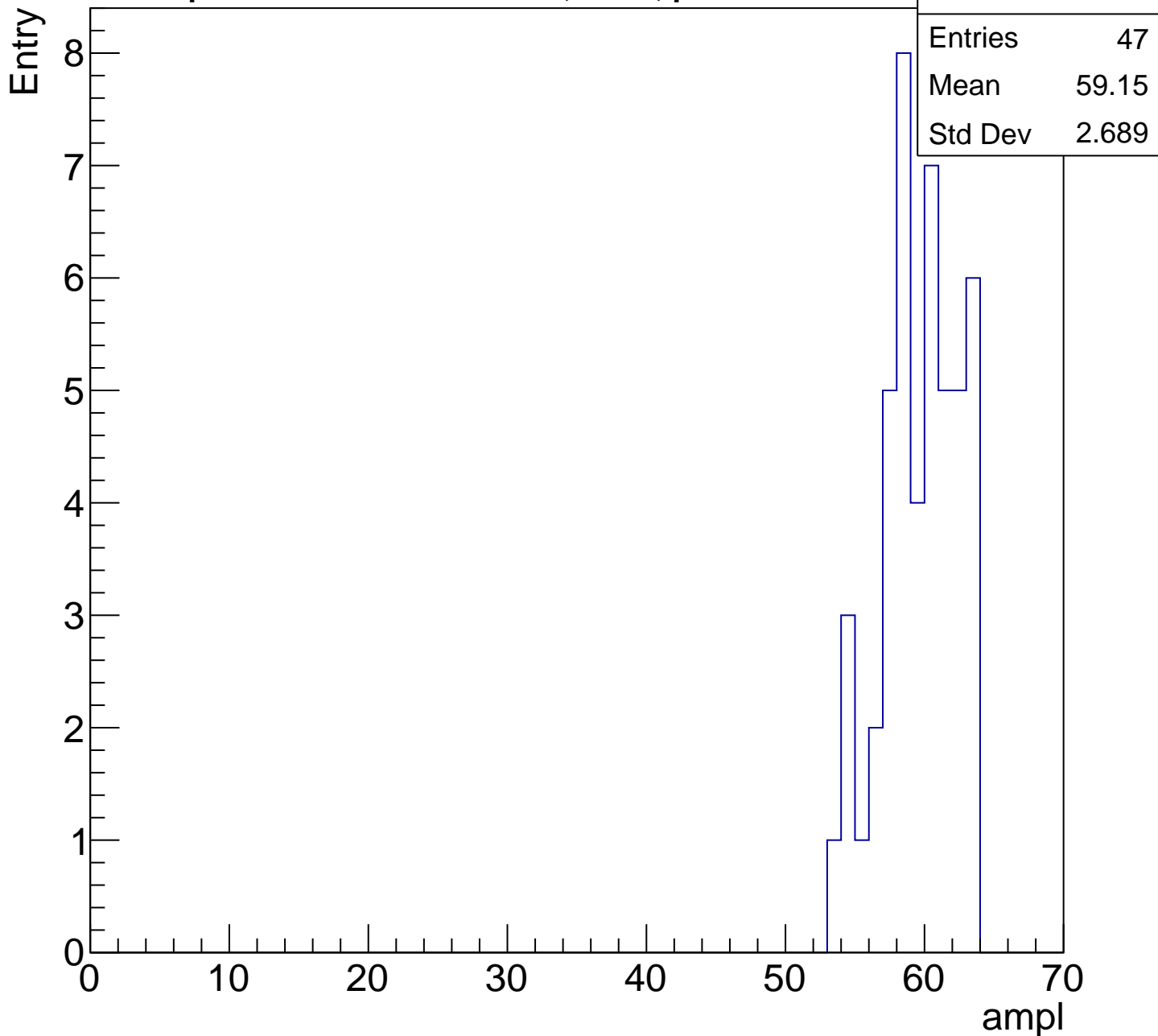
Entry

Entries	65
Mean	53.51
Std Dev	7.296



# B1L101S, U8-ch44, adc5

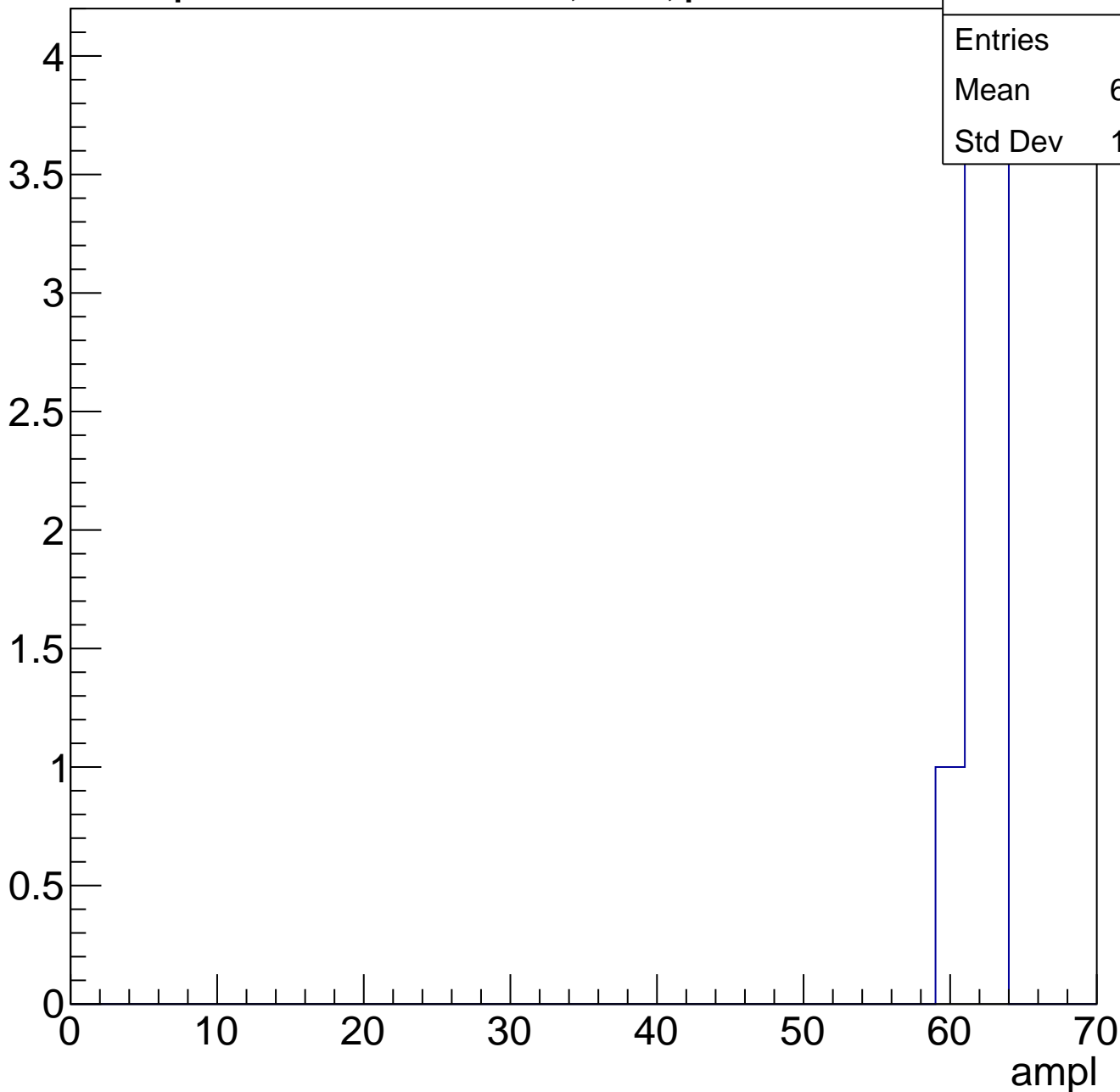
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U8-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch45, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	80
Mean	28.36
Std Dev	3.812

**Gaus mean : 28.9911**

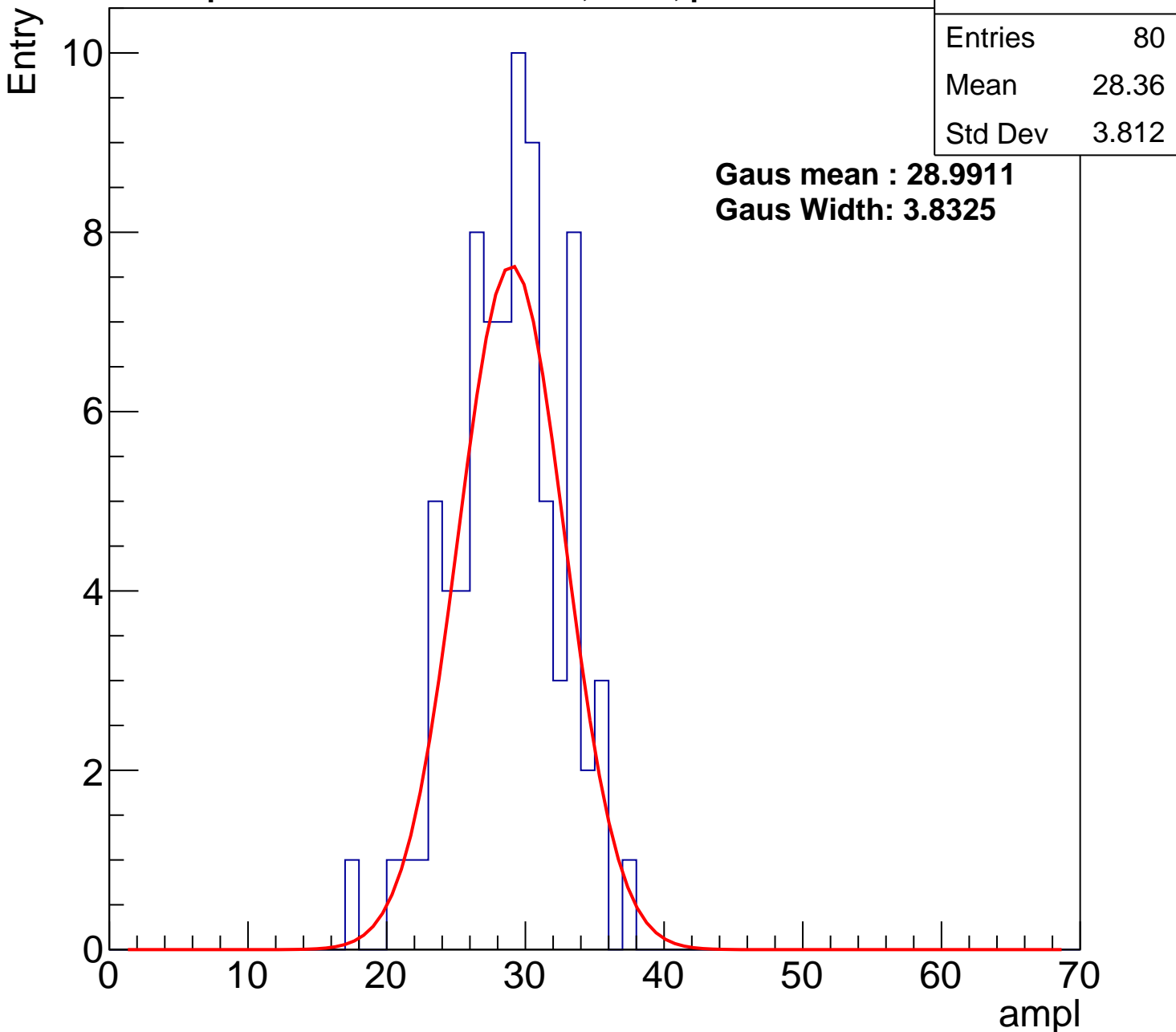
**Gaus Width: 3.8325**

Entry

10  
8  
6  
4  
2  
0

ampl

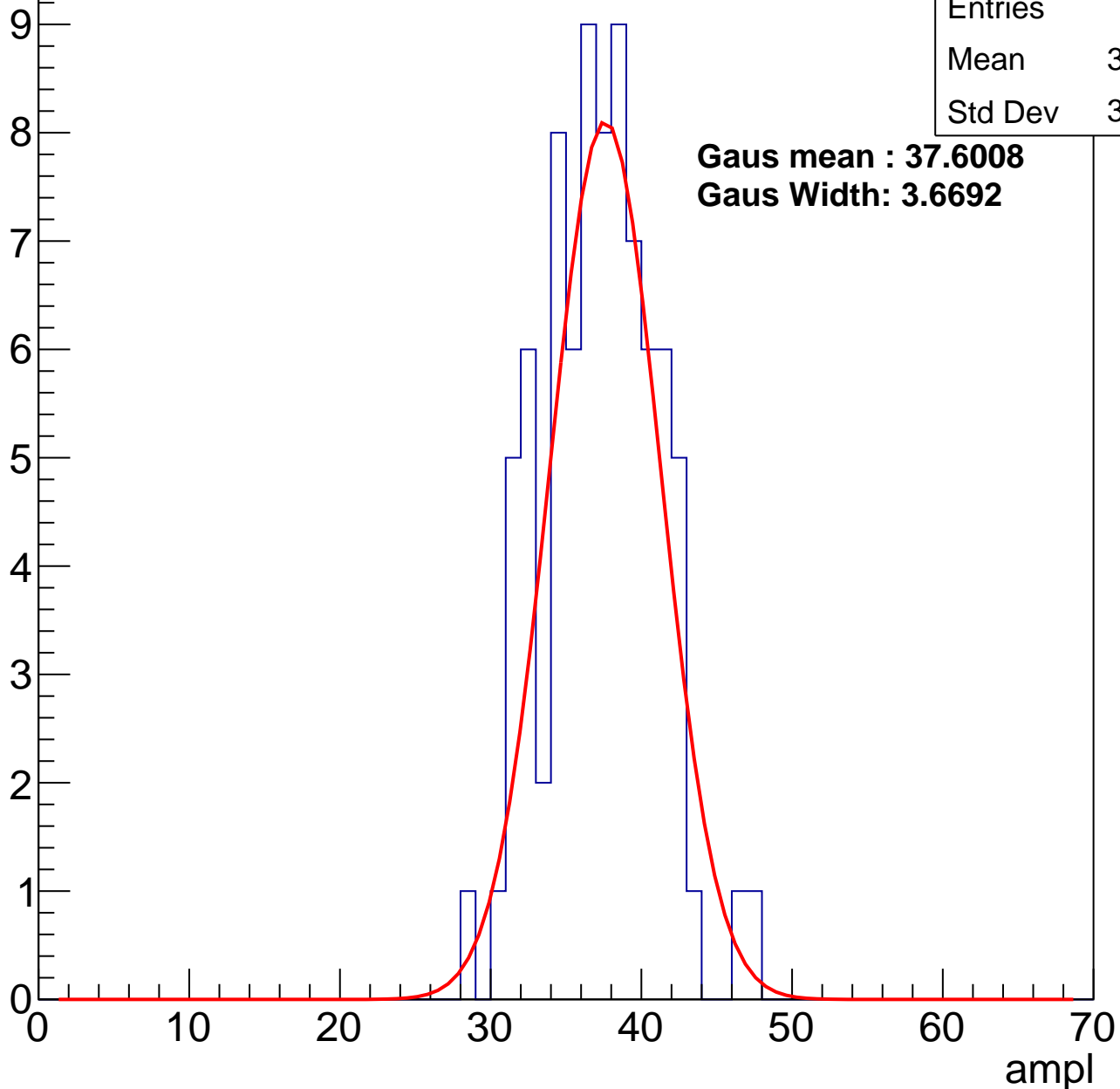
0 10 20 30 40 50 60 70



# B1L101S, U8-ch45, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	82
Mean	36.83
Std Dev	3.702

**Gaus mean : 37.6008**

**Gaus Width: 3.6692**

# B1L101S, U8-ch45, adc2

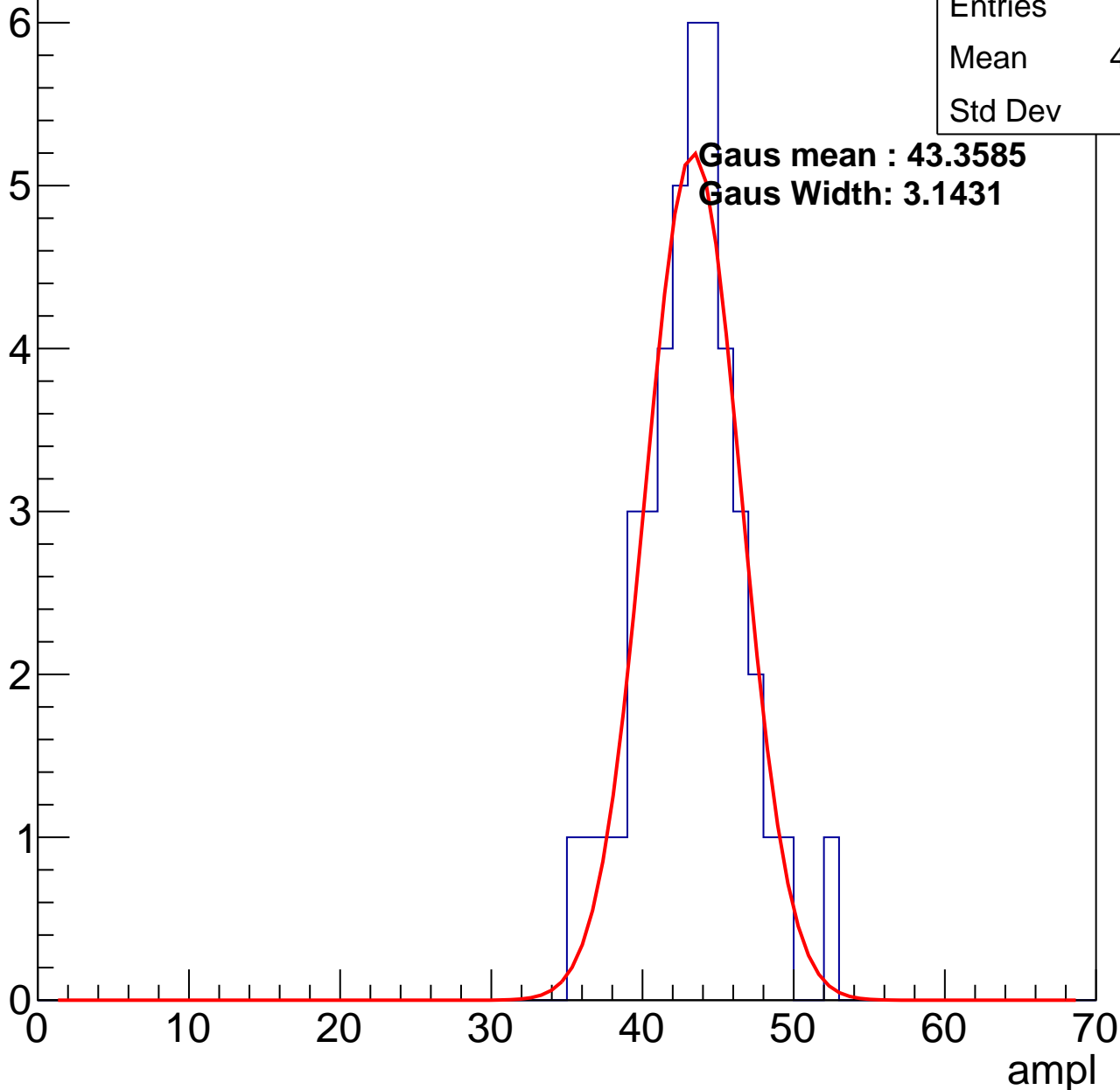
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	42.79
Std Dev	3.38

**Gaus mean : 43.3585**

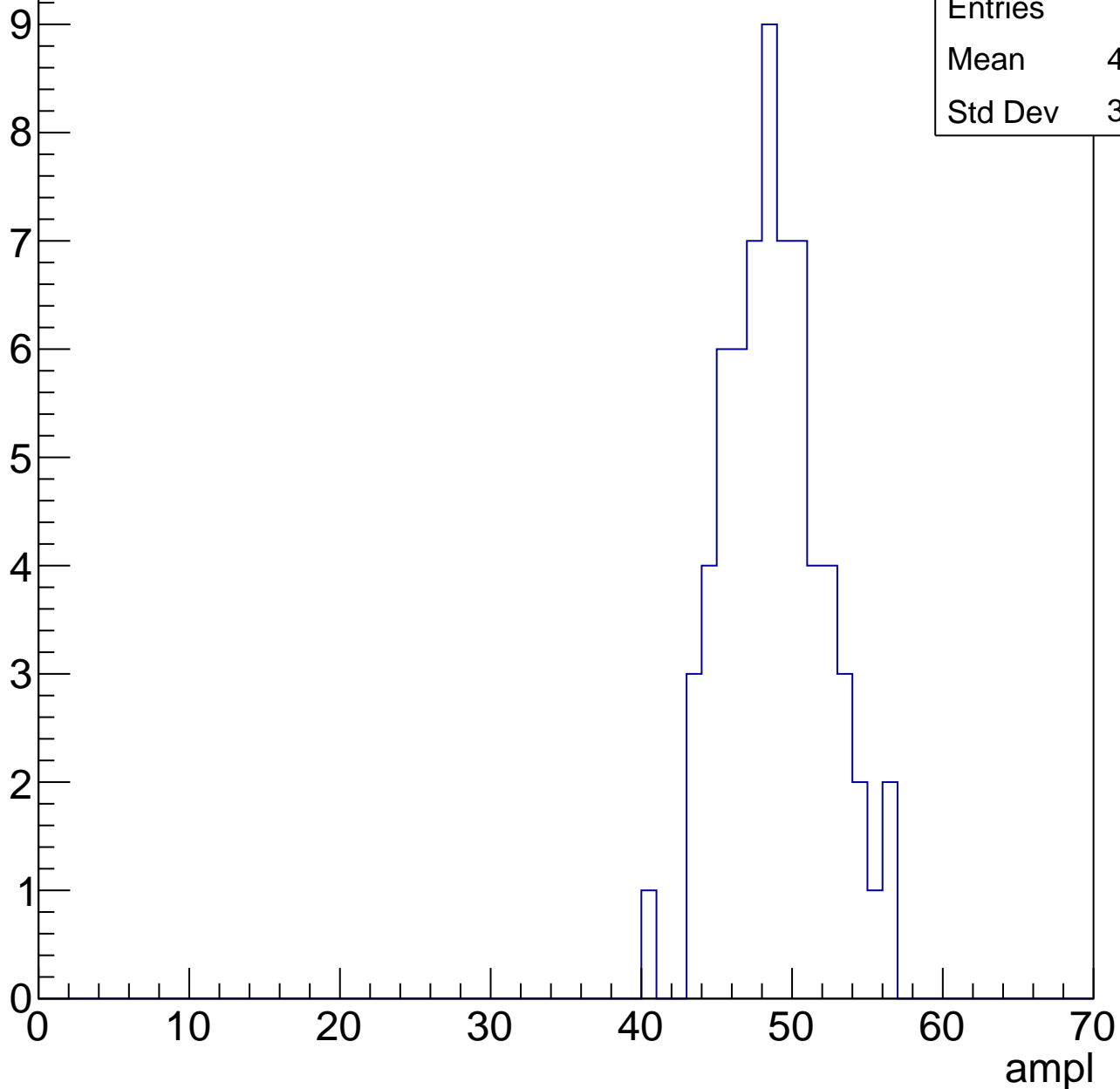
**Gaus Width: 3.1431**



# B1L101S, U8-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



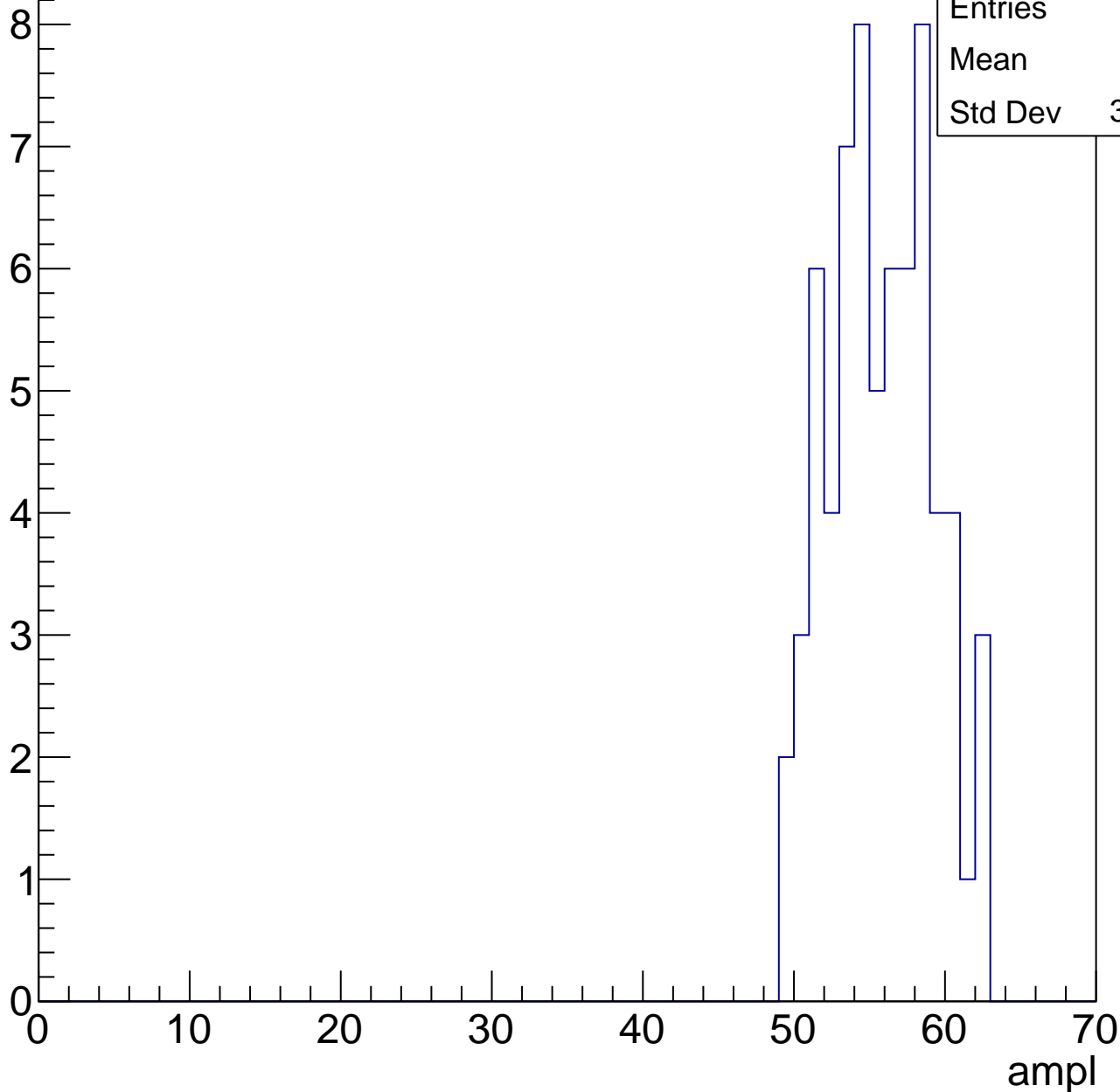
Entries	66
Mean	48.35
Std Dev	3.346

# B1L101S, U8-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	55.3
Std Dev	3.364

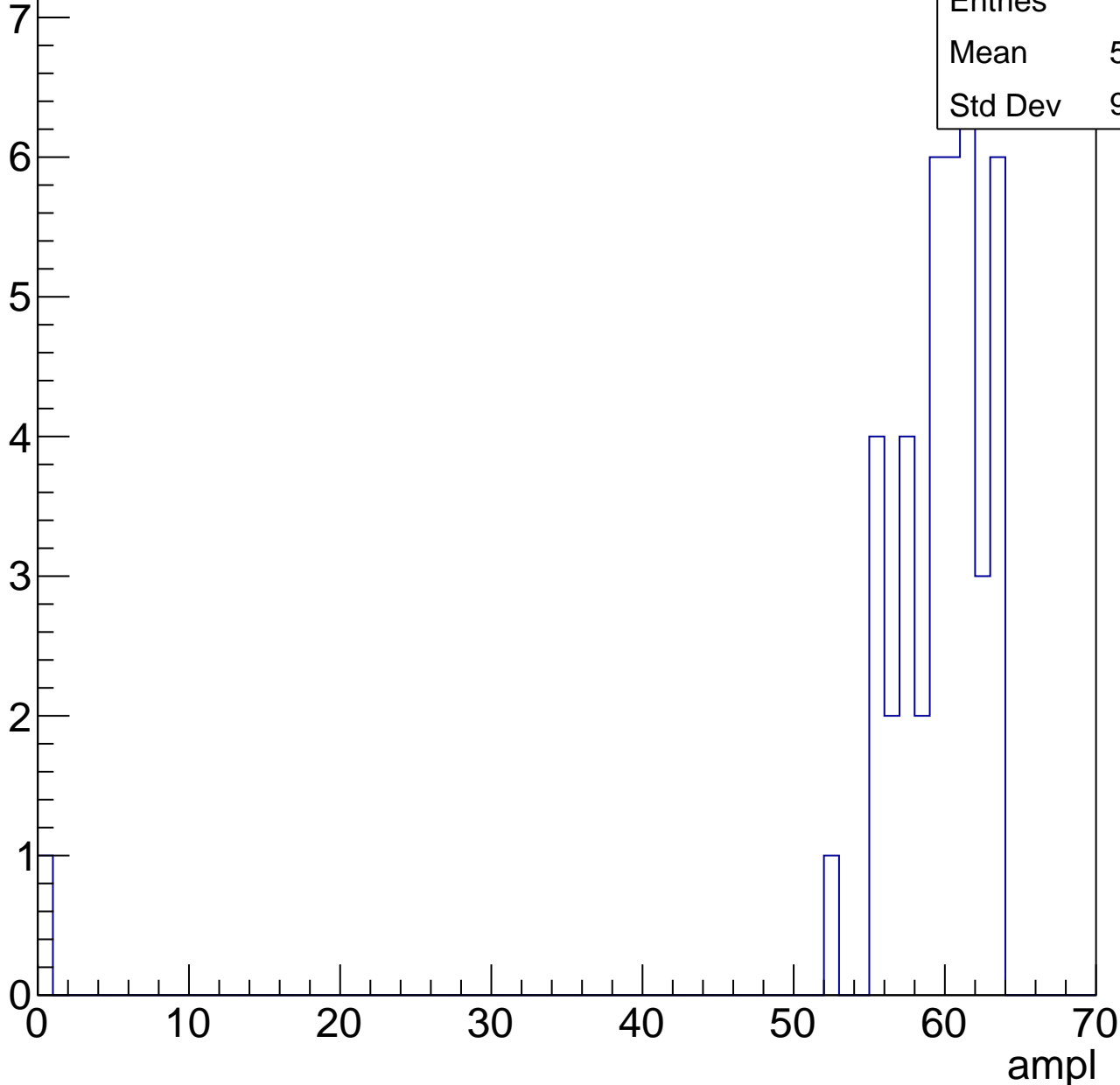


# B1L101S, U8-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	57.93
Std Dev	9.435



# B1L101S, U8-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

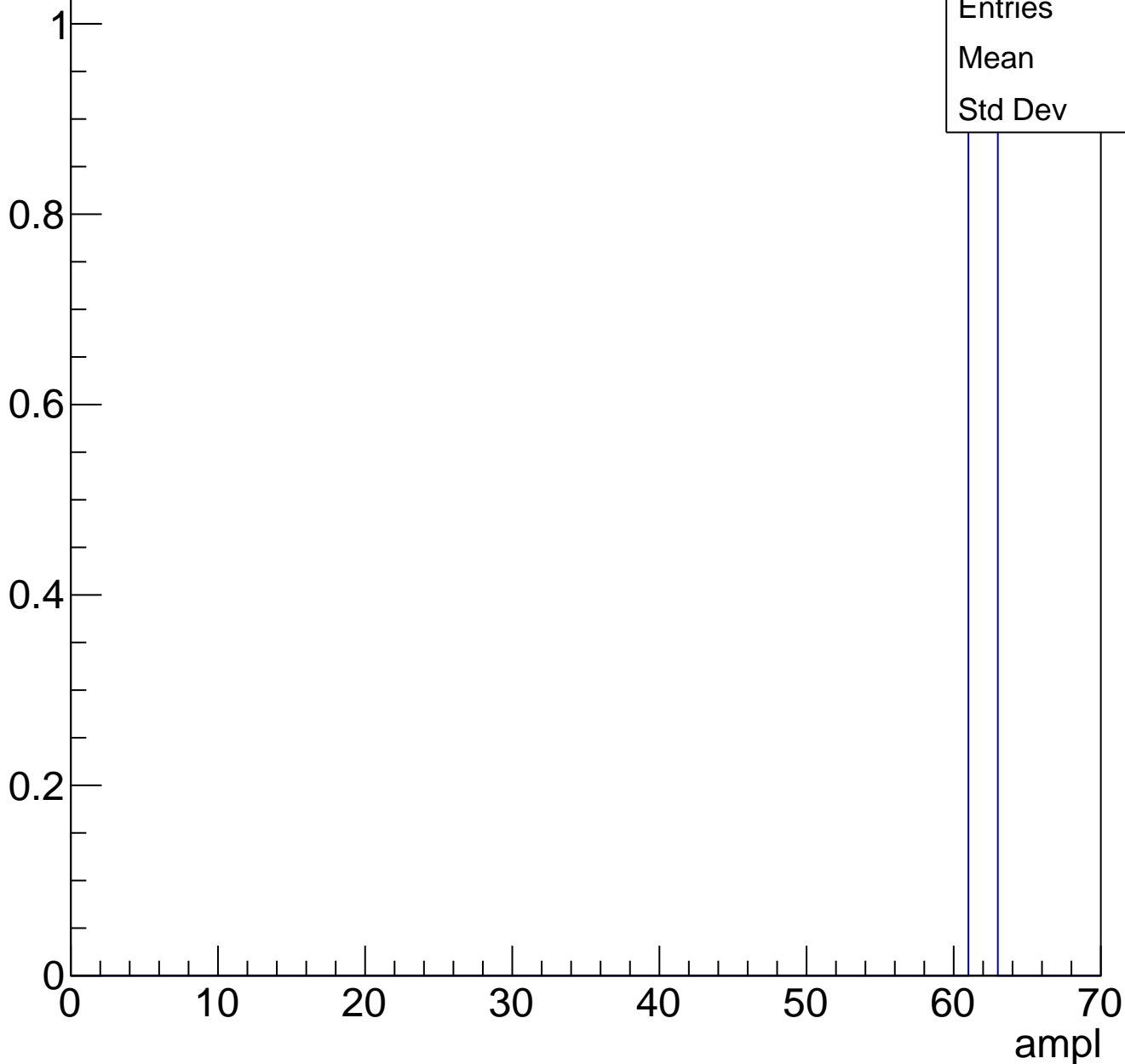




# B1L101S, U8-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch46, adc0

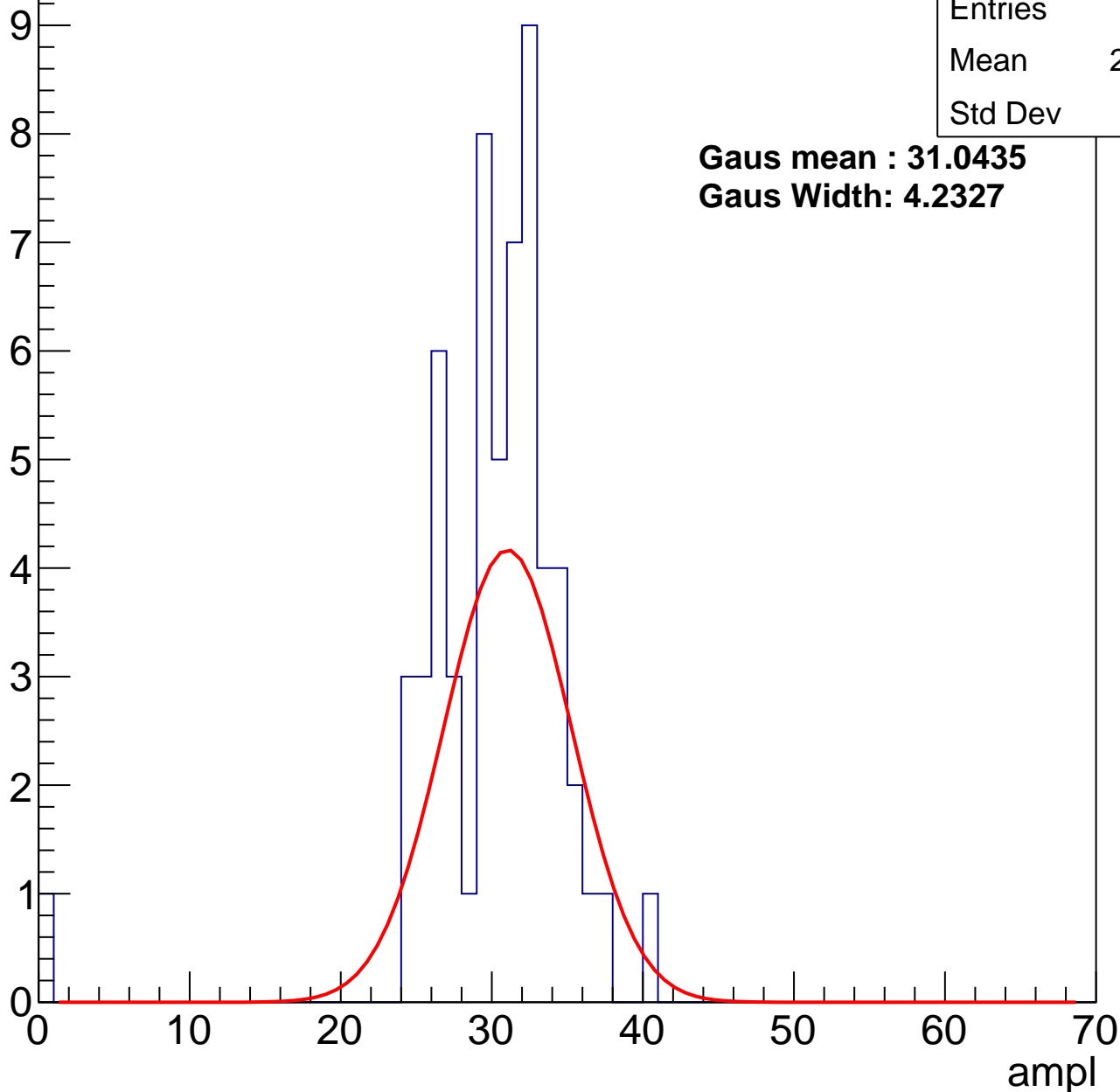
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	29.66
Std Dev	5.19

**Gaus mean : 31.0435**

**Gaus Width: 4.2327**



# B1L101S, U8-ch46, adc1

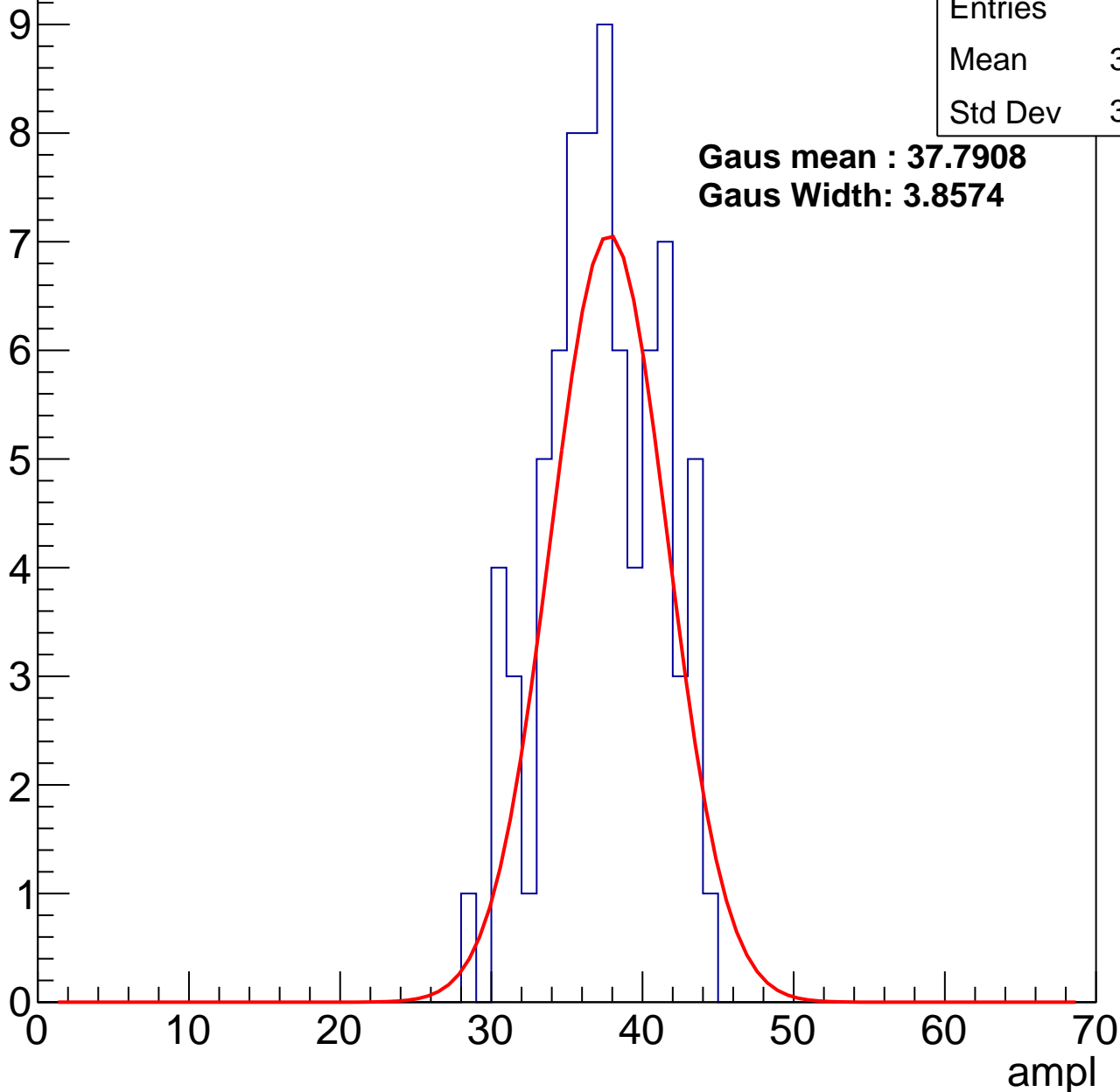
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	36.87
Std Dev	3.736

**Gaus mean : 37.7908**

**Gaus Width: 3.8574**



# B1L101S, U8-ch46, adc2

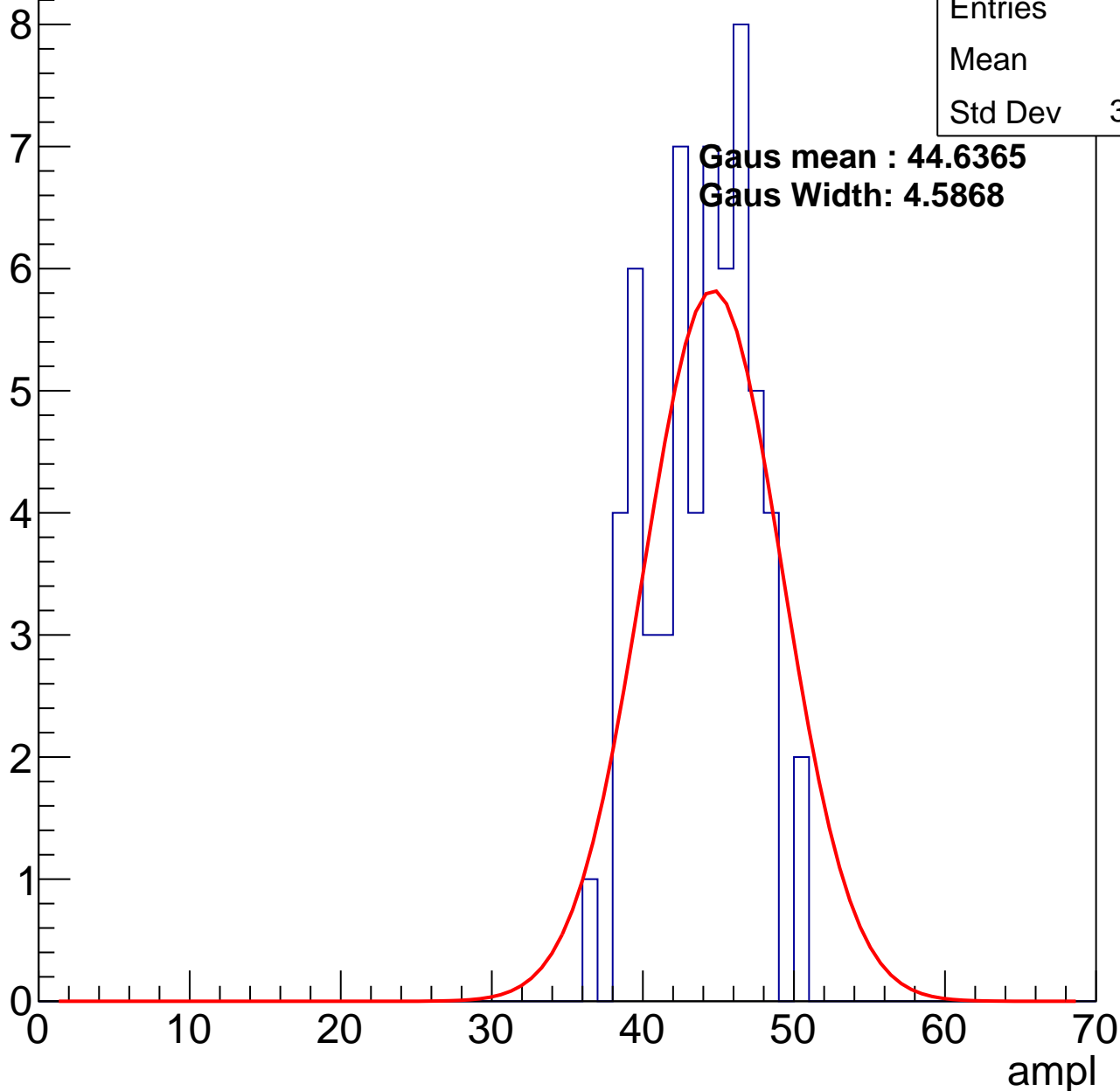
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	43.4
Std Dev	3.323

**Gaus mean : 44.6365**

**Gaus Width: 4.5868**

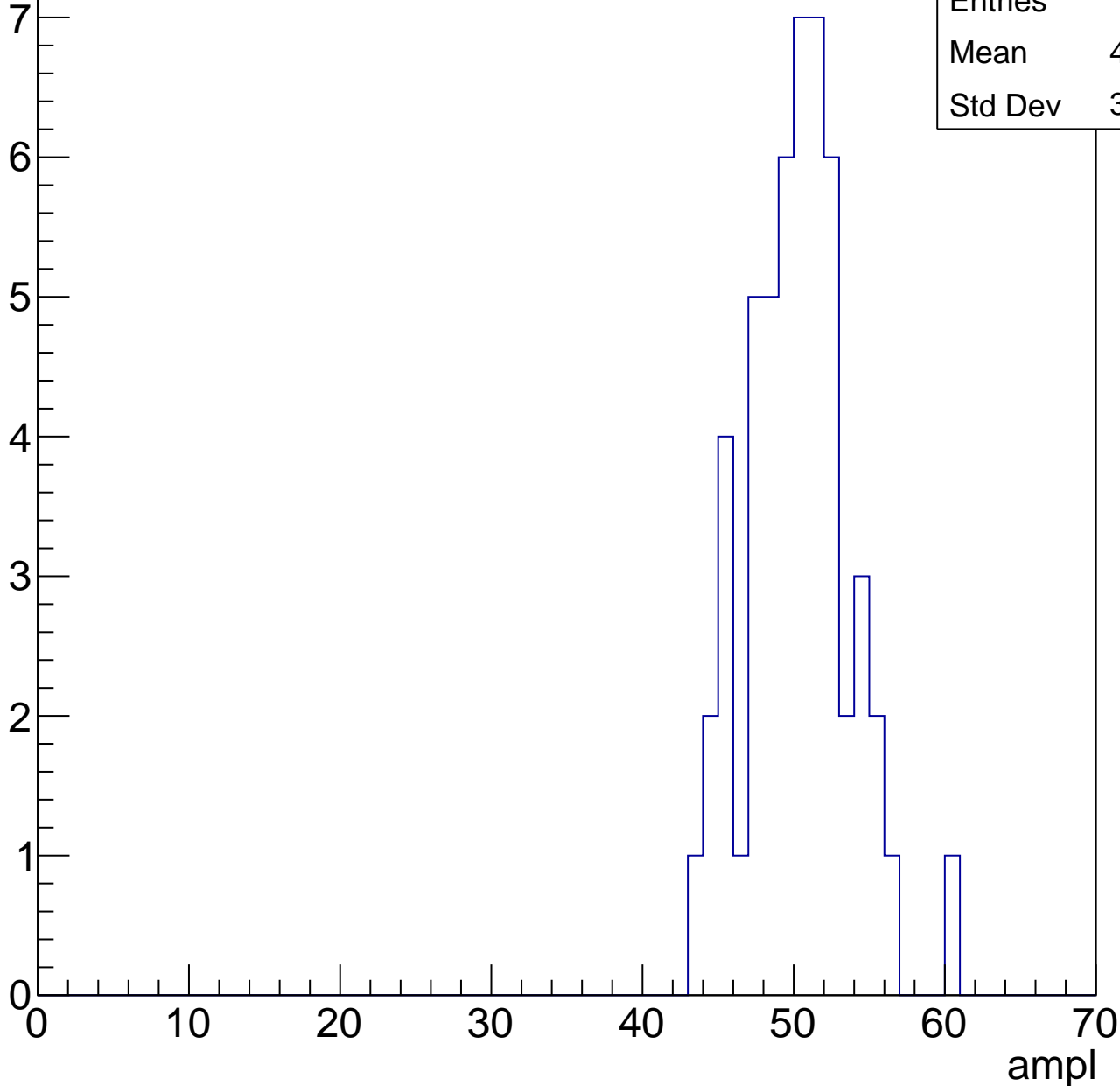


# B1L101S, U8-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

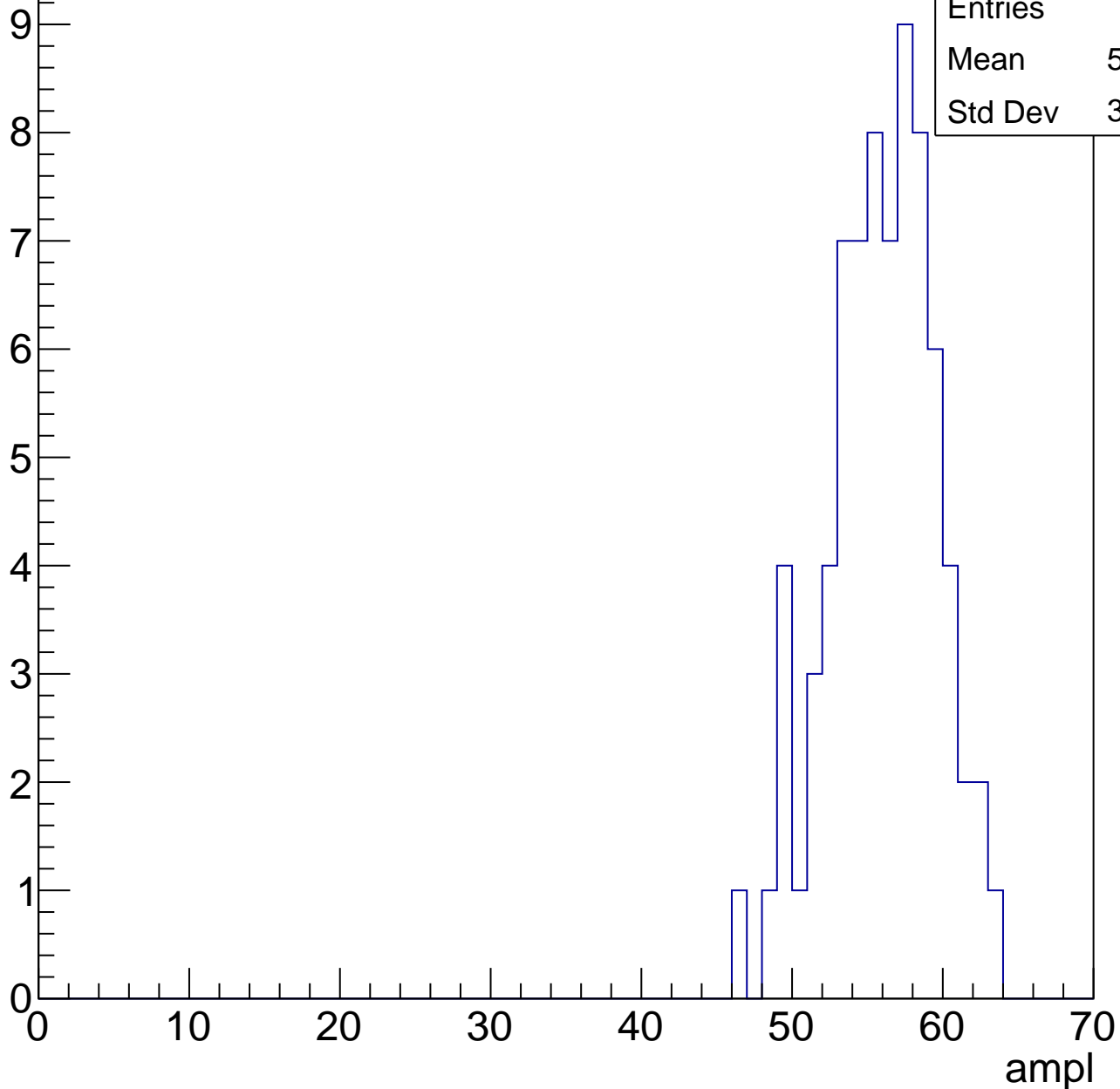
Entries	53
Mean	49.79
Std Dev	3.333



# B1L101S, U8-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



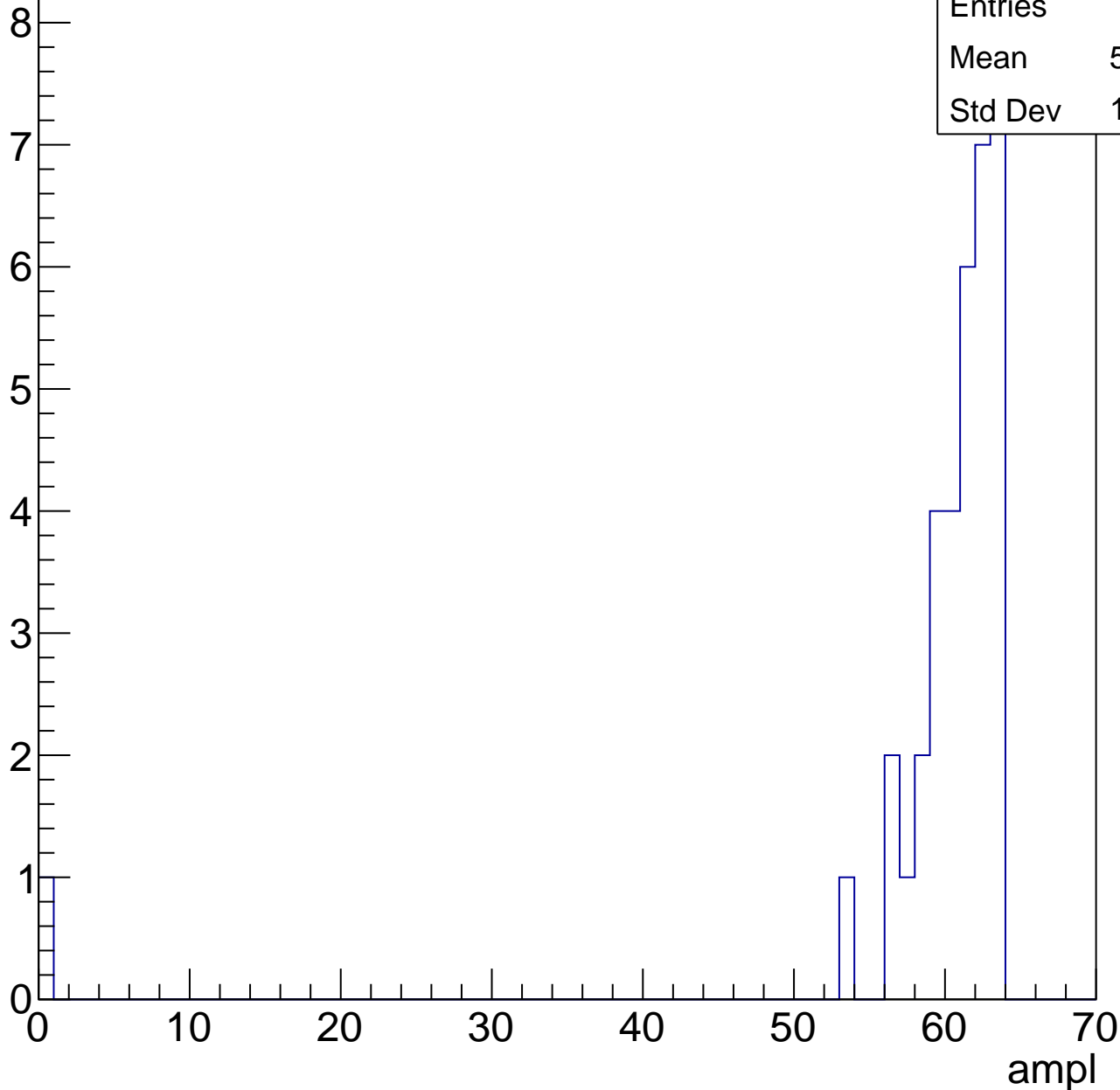
Entries	75
Mean	55.49
Std Dev	3.549

# B1L101S, U8-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	36
Mean	58.83
Std Dev	10.22



# B1L101S, U8-ch46, adc6

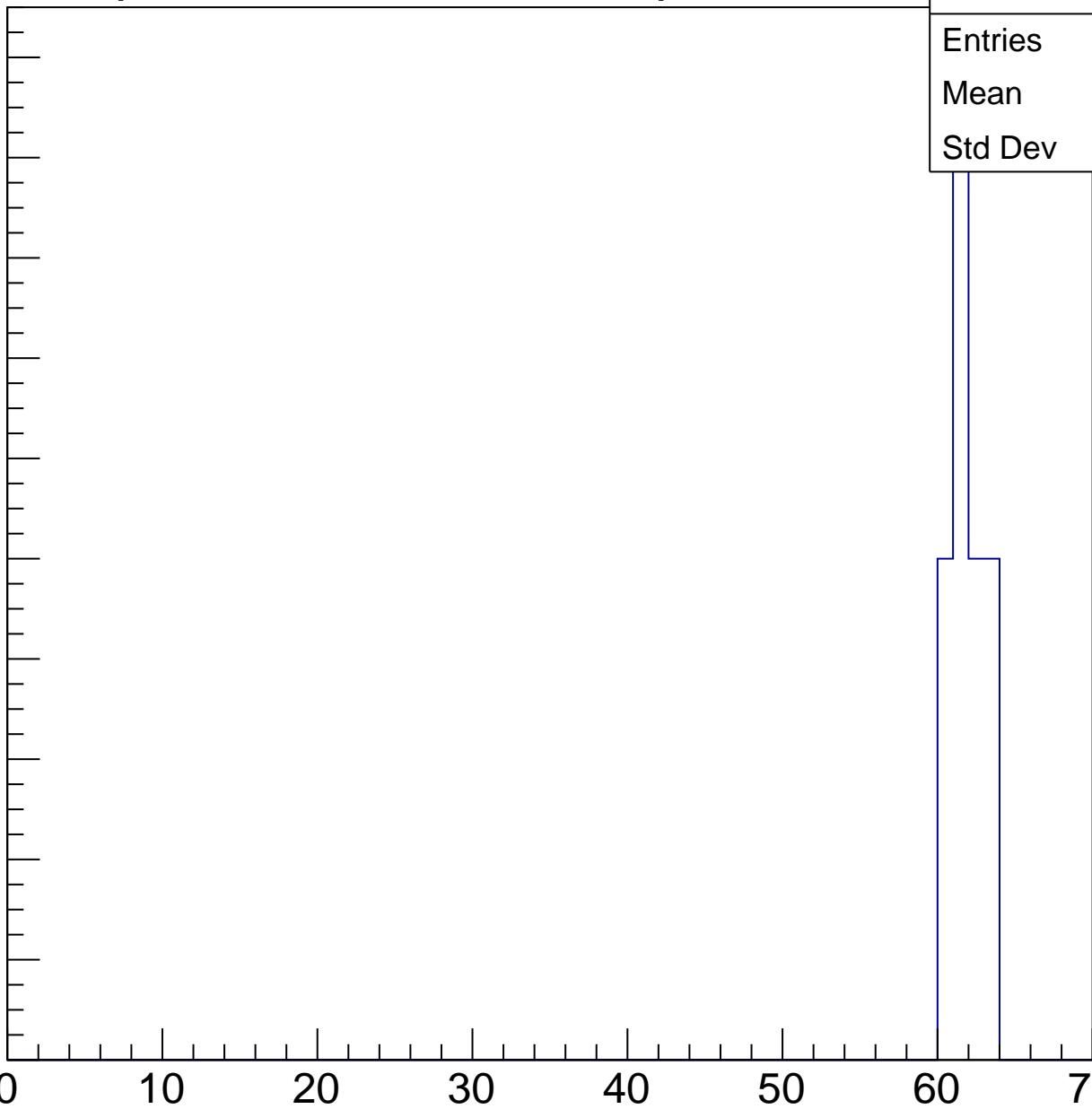
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.4
Std Dev	1.02

ampl





# B1L101S, U8-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch47, adc0

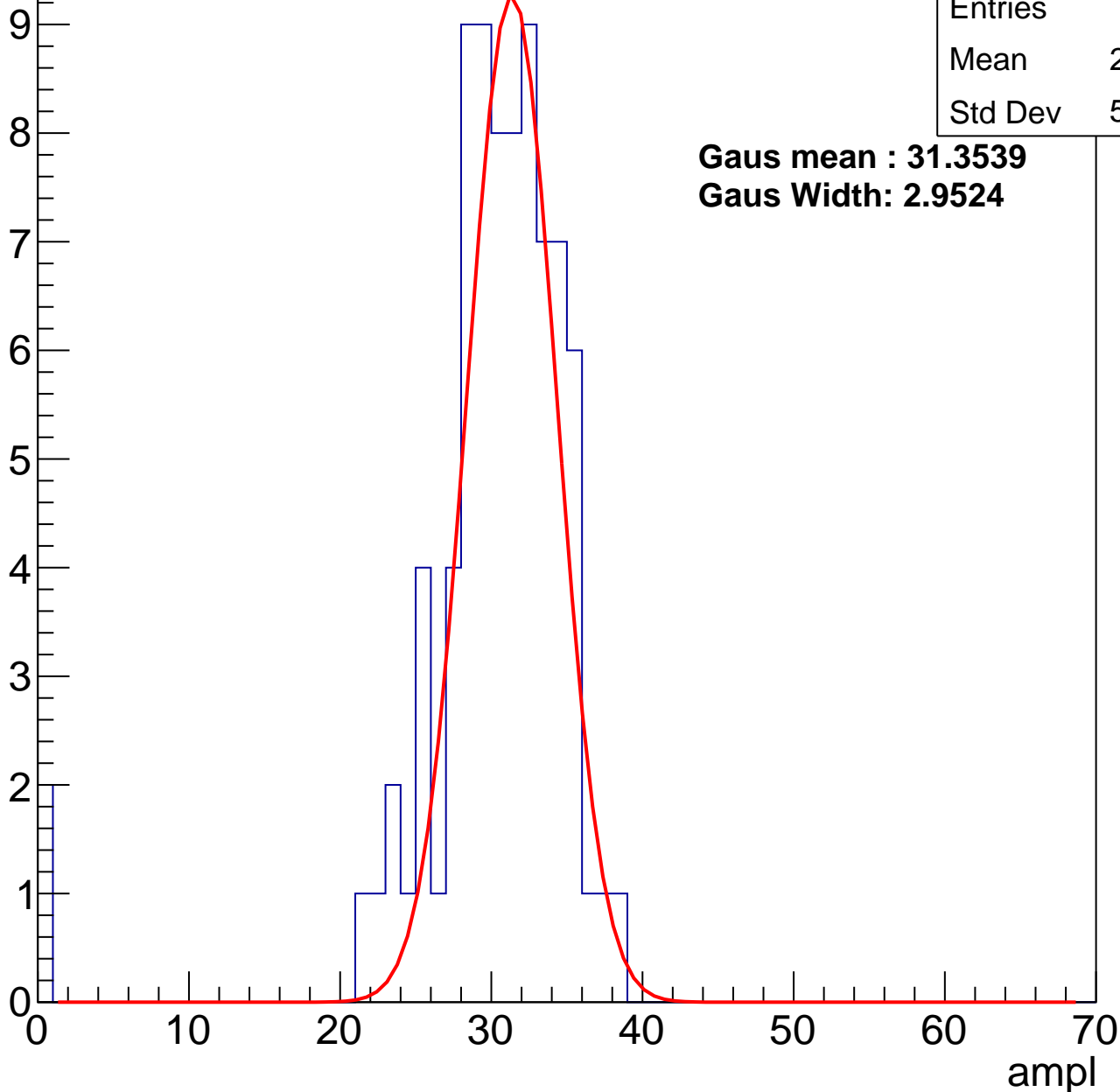
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	29.59
Std Dev	5.822

**Gaus mean : 31.3539**

**Gaus Width: 2.9524**



# B1L101S, U8-ch47, adc1

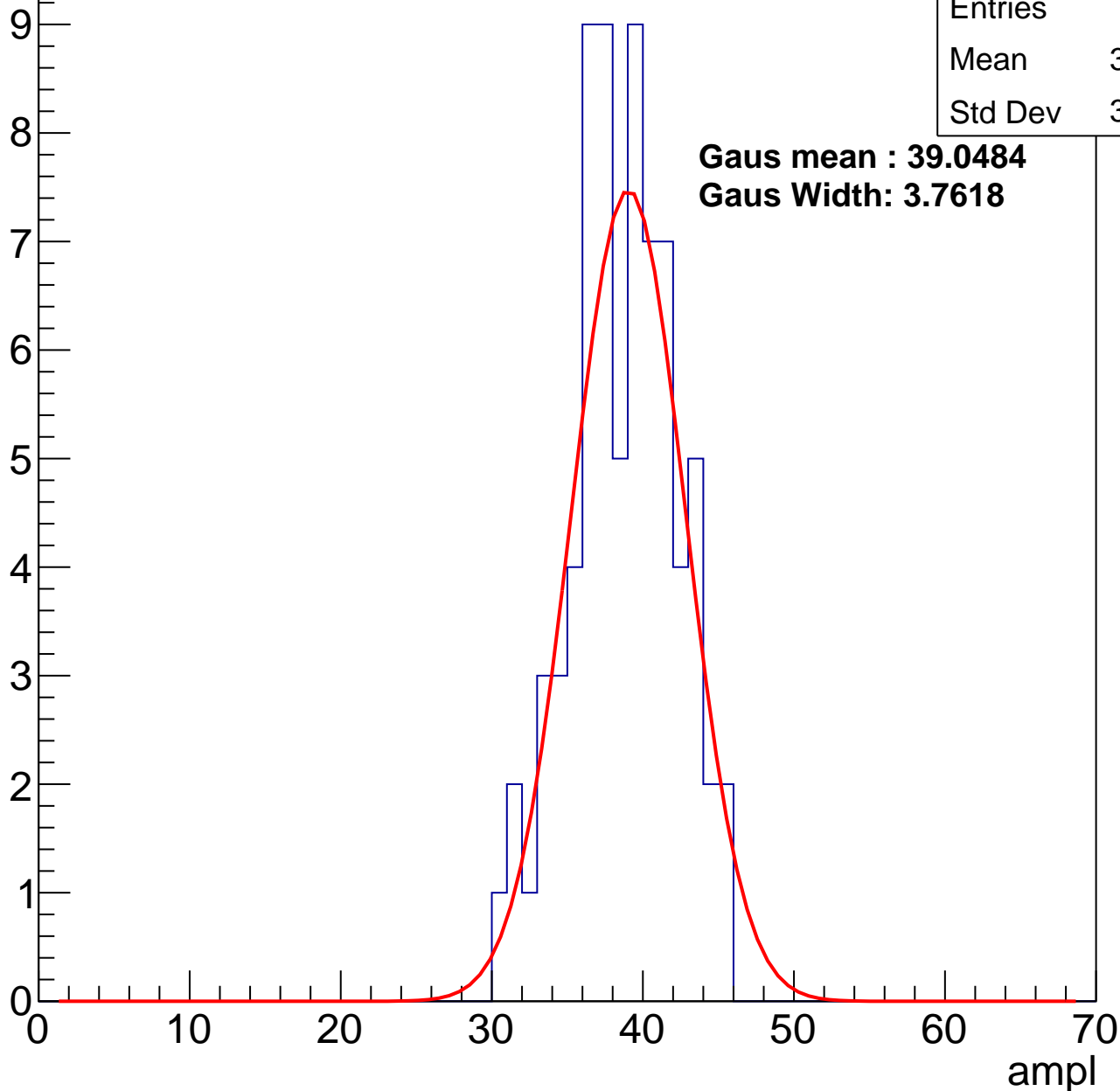
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	38.23
Std Dev	3.426

**Gaus mean : 39.0484**

**Gaus Width: 3.7618**



# B1L101S, U8-ch47, adc2

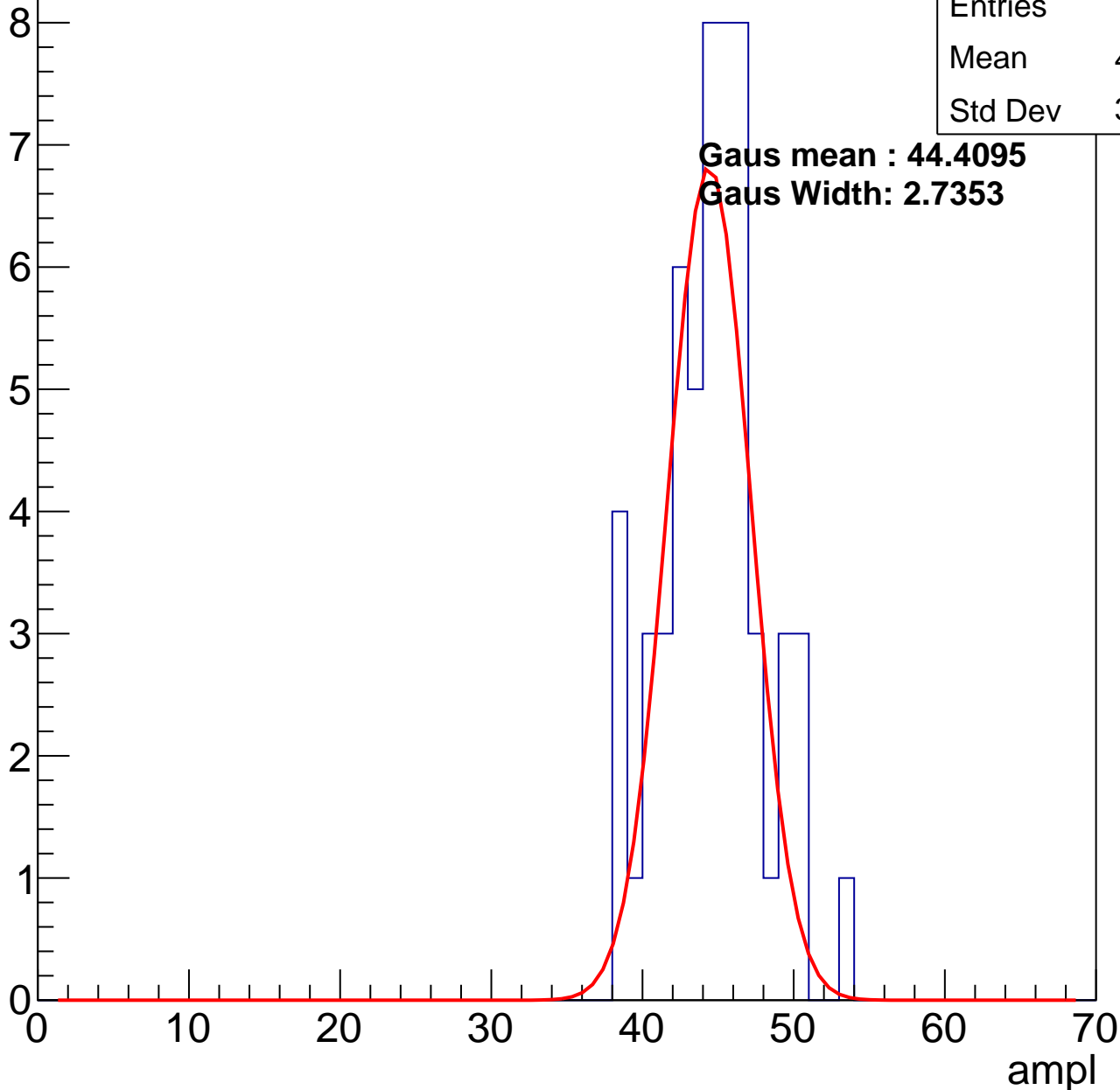
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	44.21
Std Dev	3.291

**Gaus mean : 44.4095**

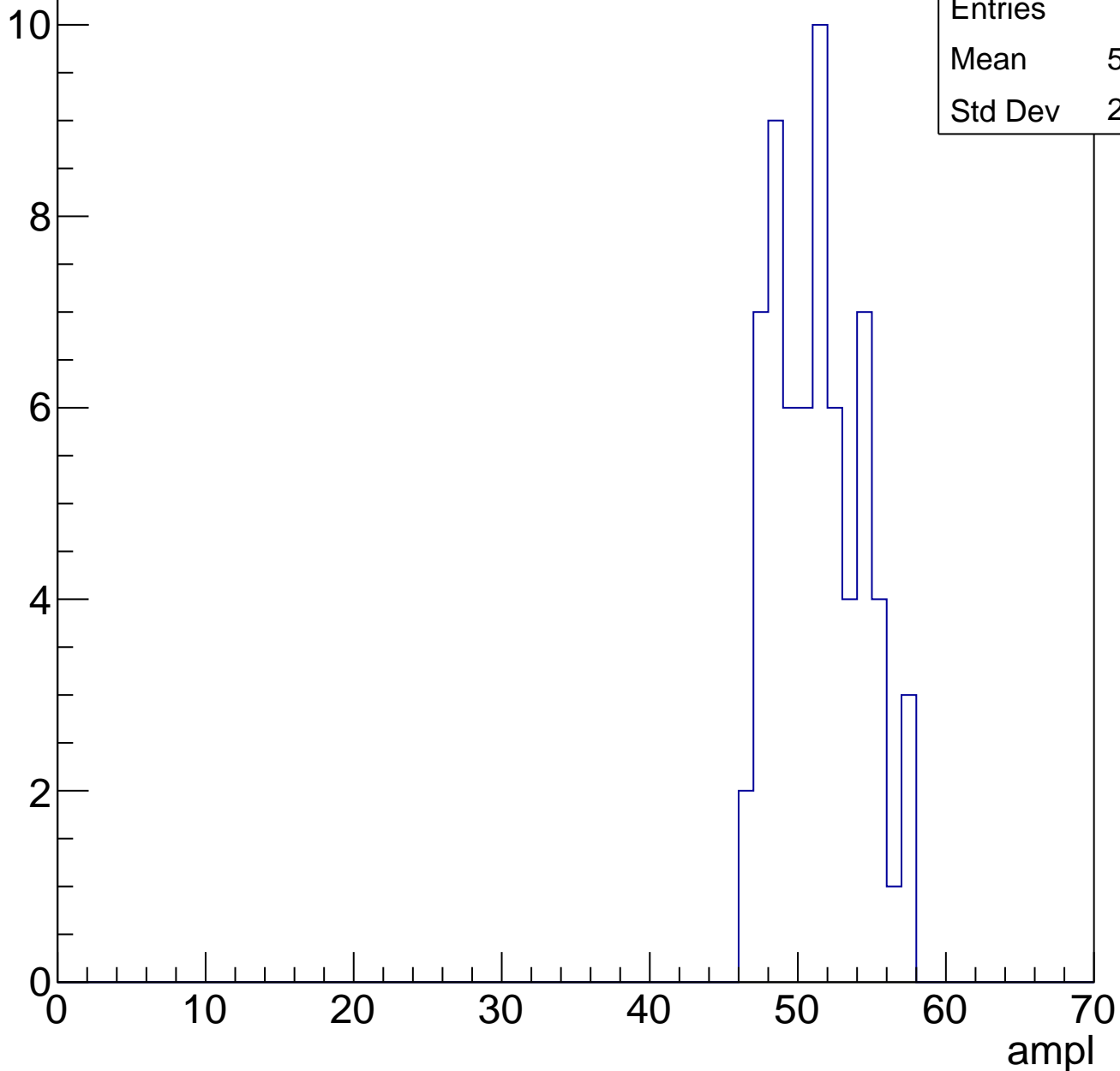
**Gaus Width: 2.7353**



# B1L101S, U8-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

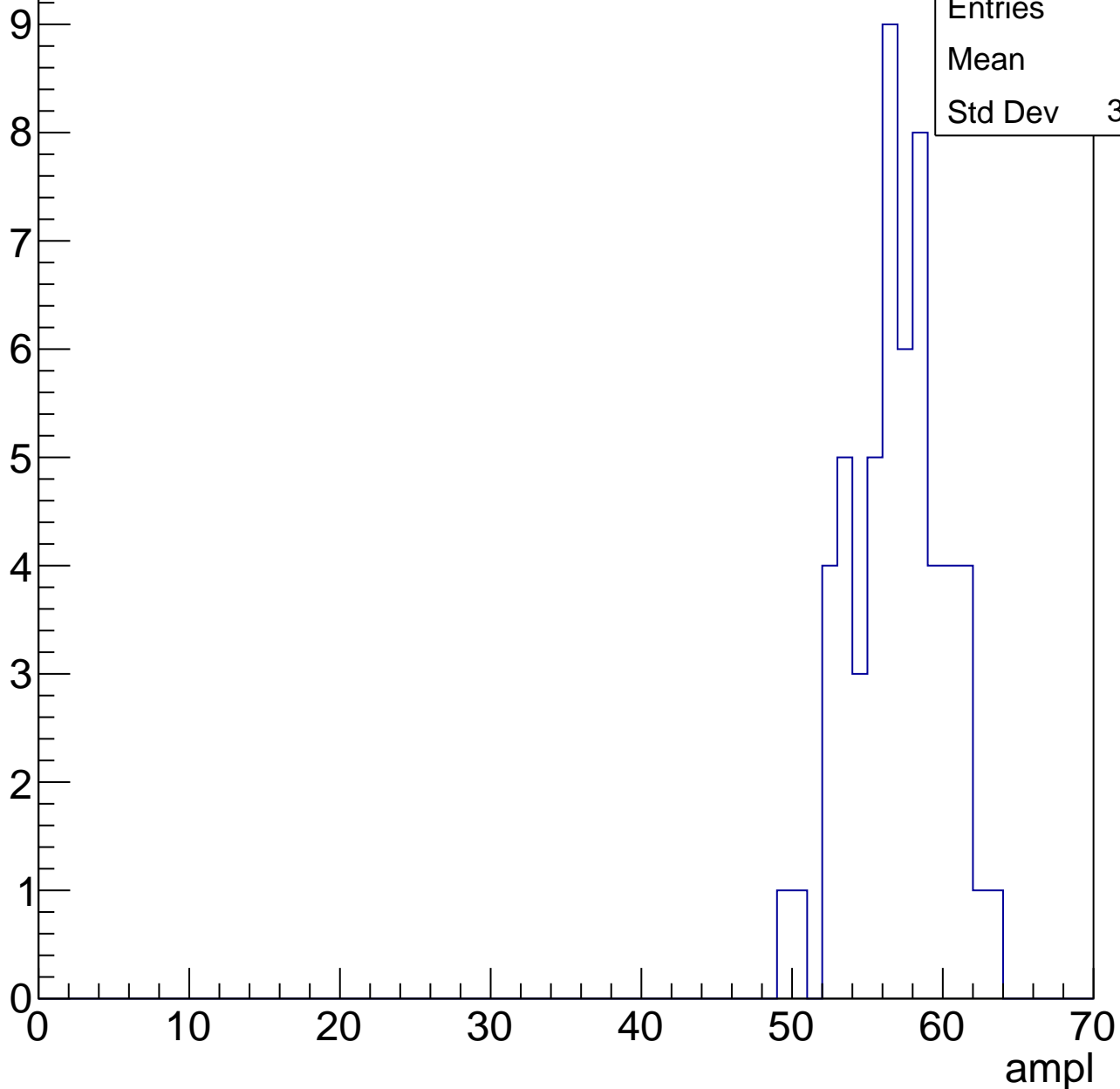
Entry



# B1L101S, U8-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

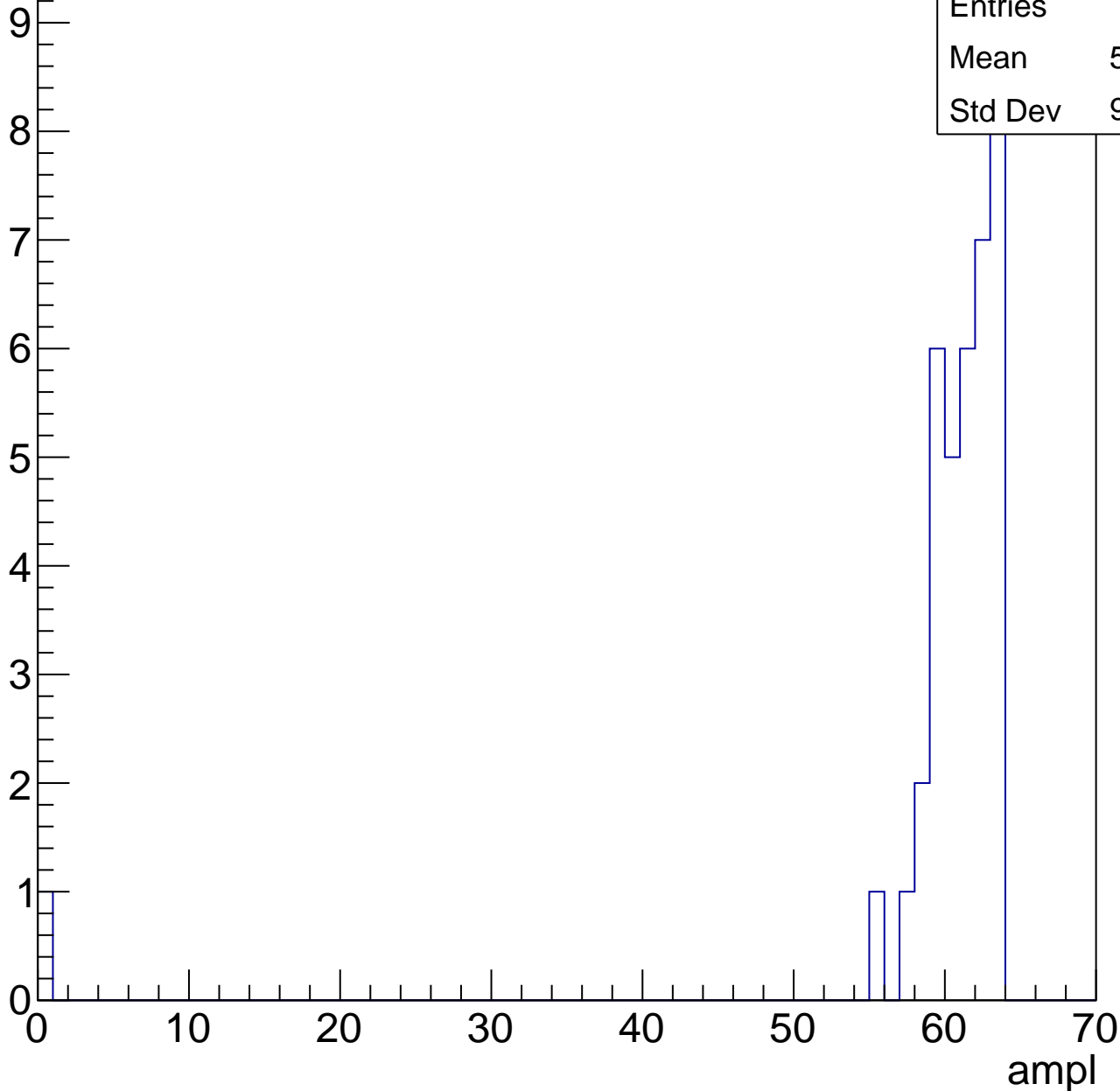


# B1L101S, U8-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

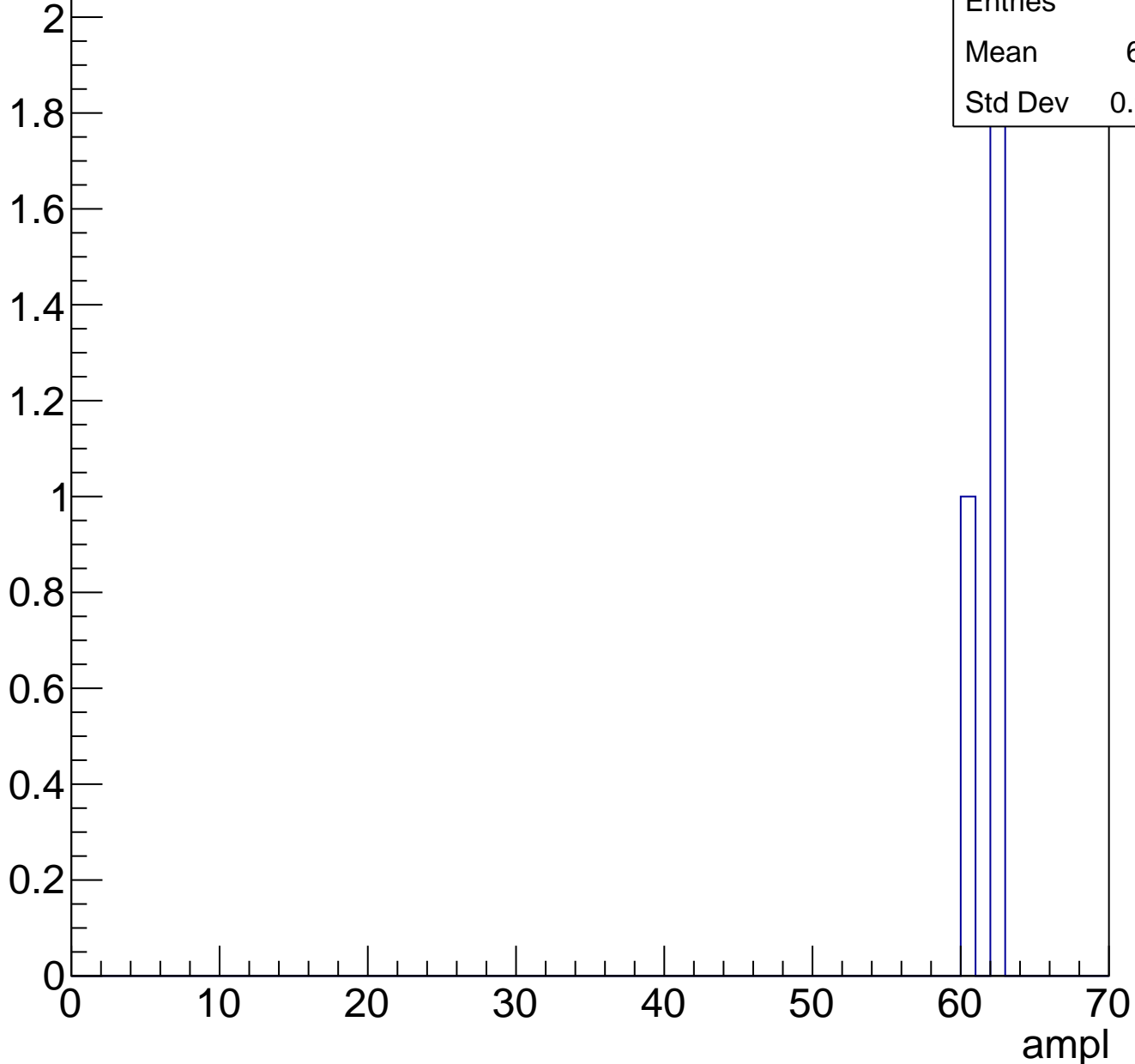
Entries	38
Mean	59.18
Std Dev	9.918



# B1L101S, U8-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	61.33
Std Dev	0.9428



# B1L101S, U8-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U8-ch48, adc0

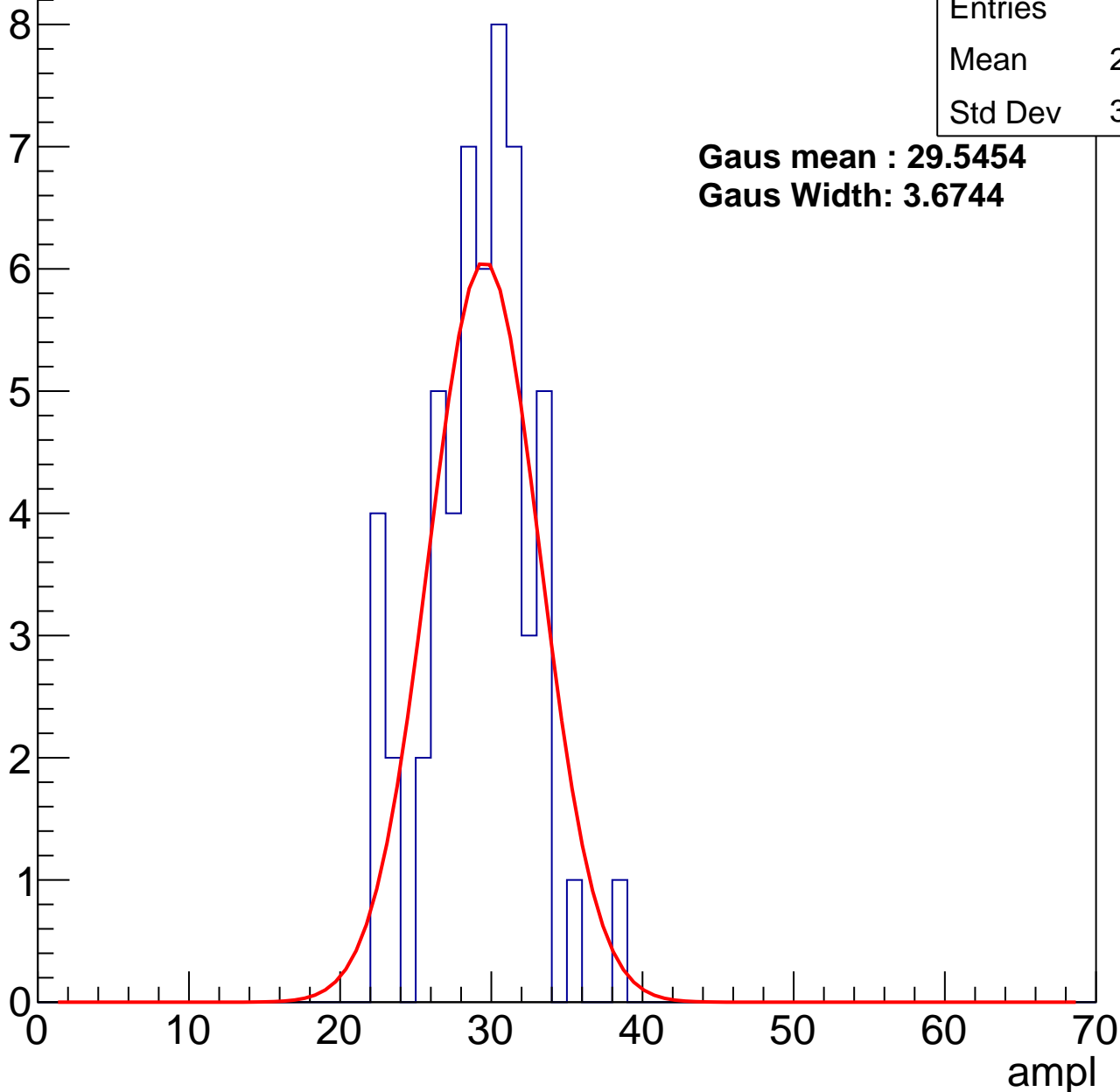
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	28.78
Std Dev	3.372

**Gaus mean : 29.5454**

**Gaus Width: 3.6744**



# B1L101S, U8-ch48, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	35.71
Std Dev	3.455

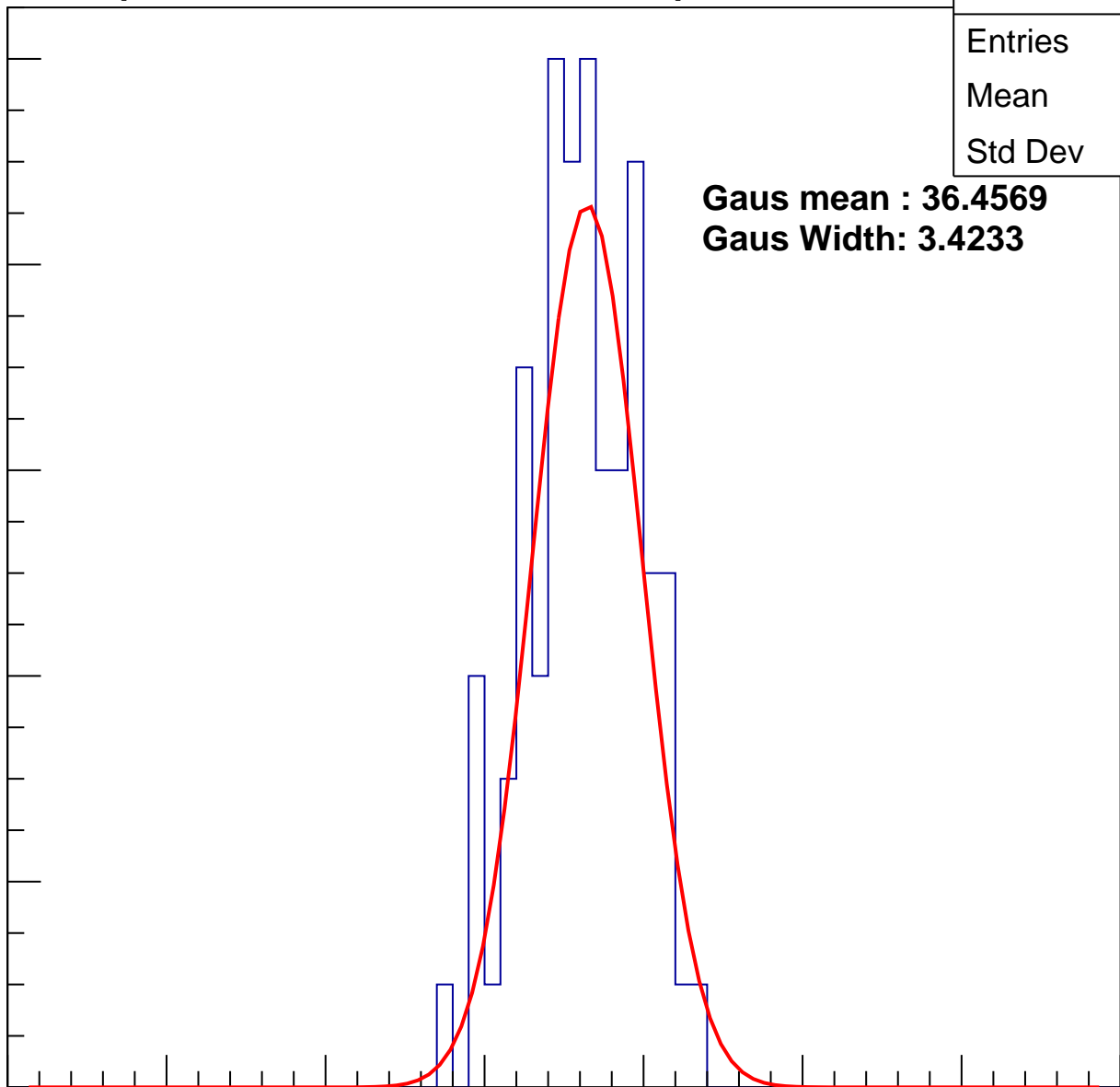
**Gaus mean : 36.4569**

**Gaus Width: 3.4233**

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U8-ch48, adc2

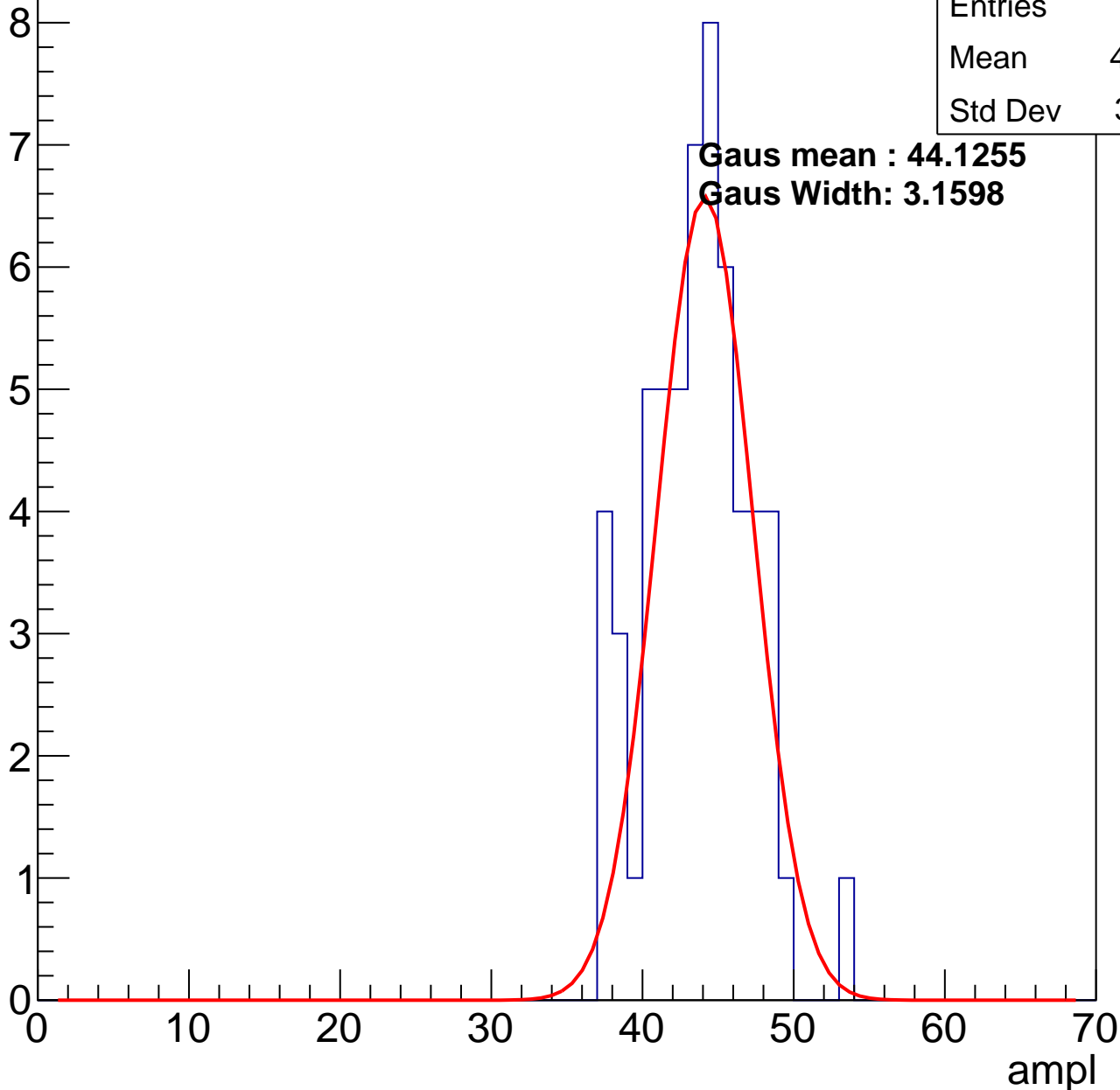
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	43.19
Std Dev	3.401

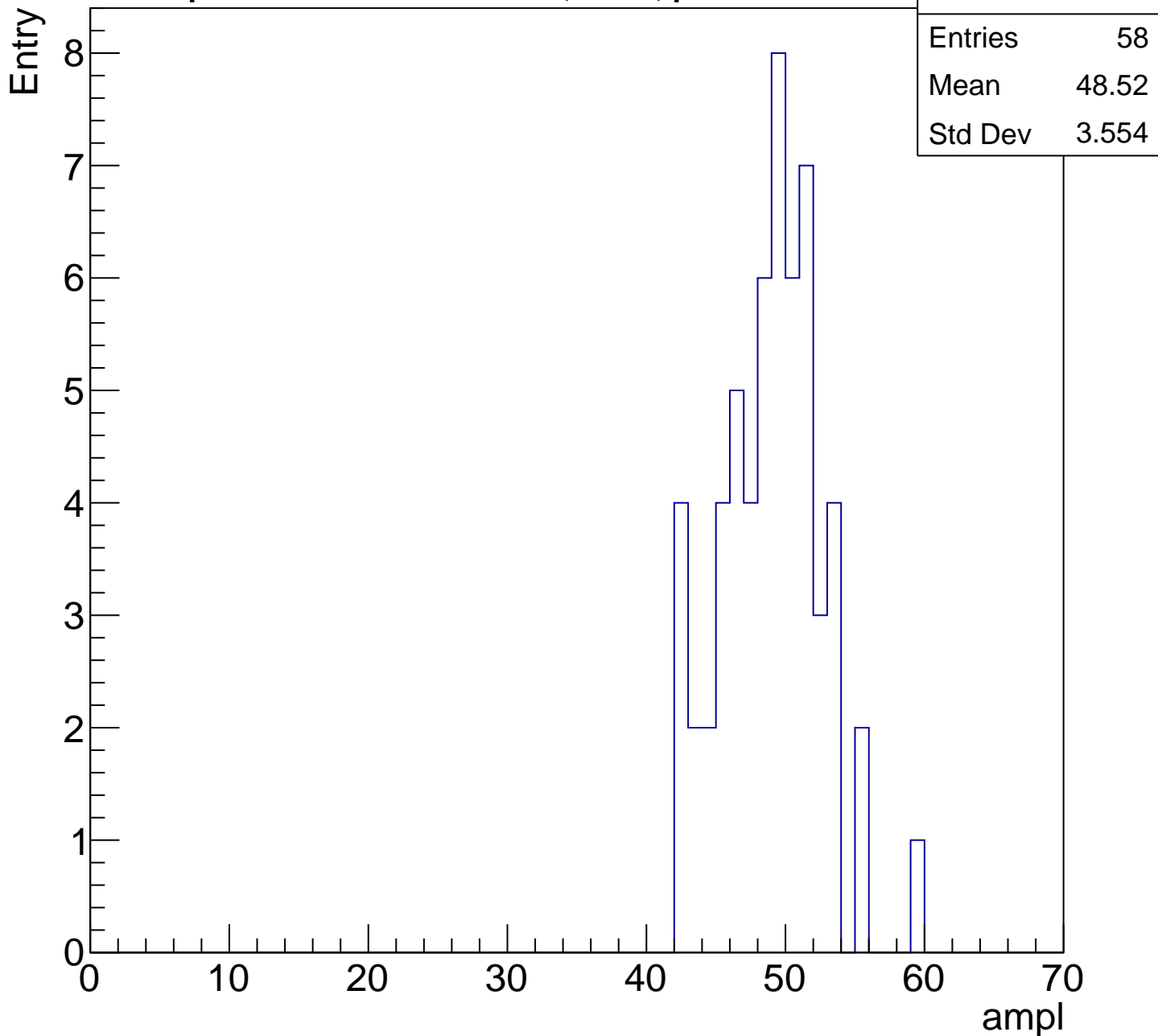
**Gaus mean : 44.1255**

**Gaus Width: 3.1598**



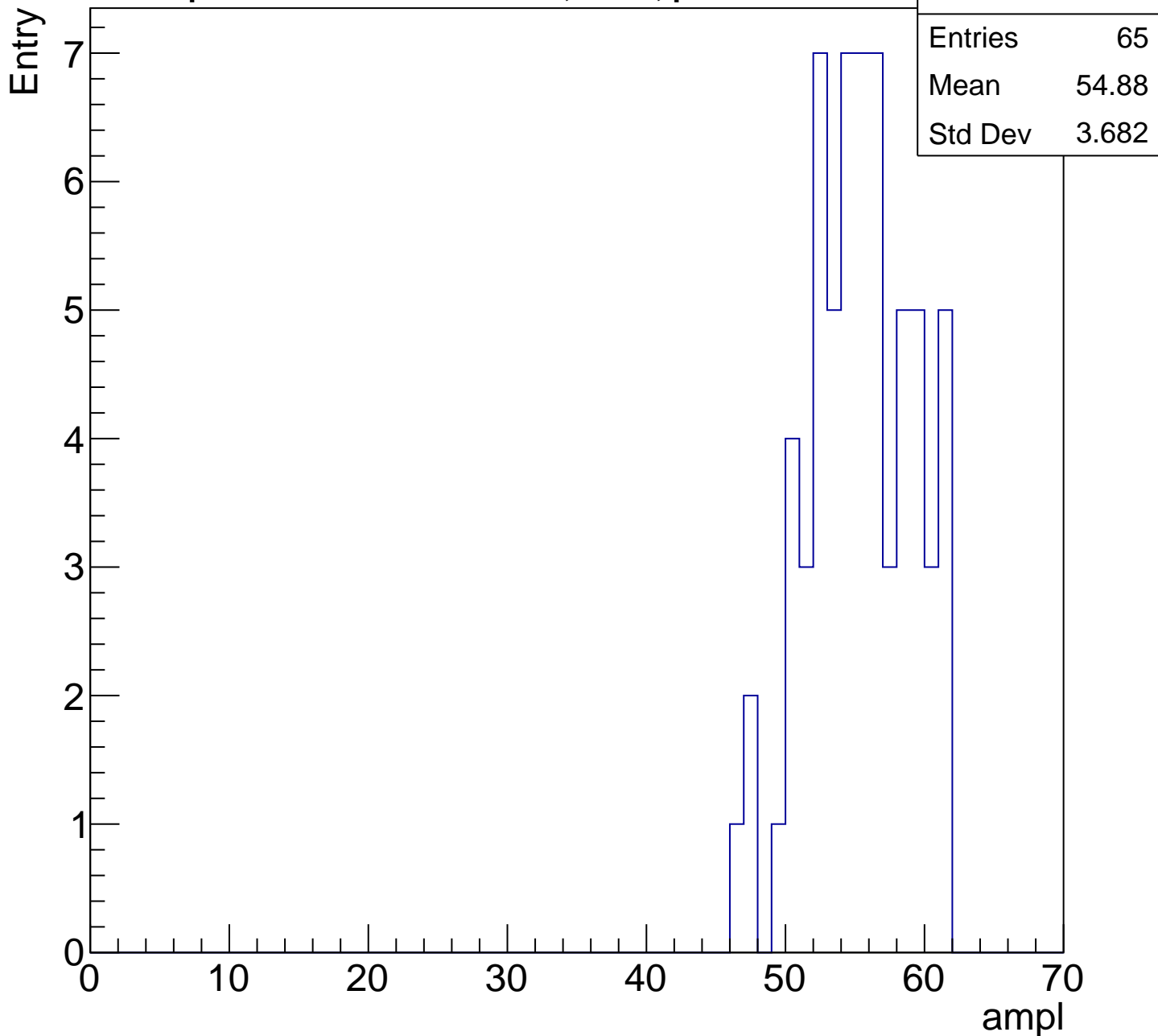
# B1L101S, U8-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U8-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

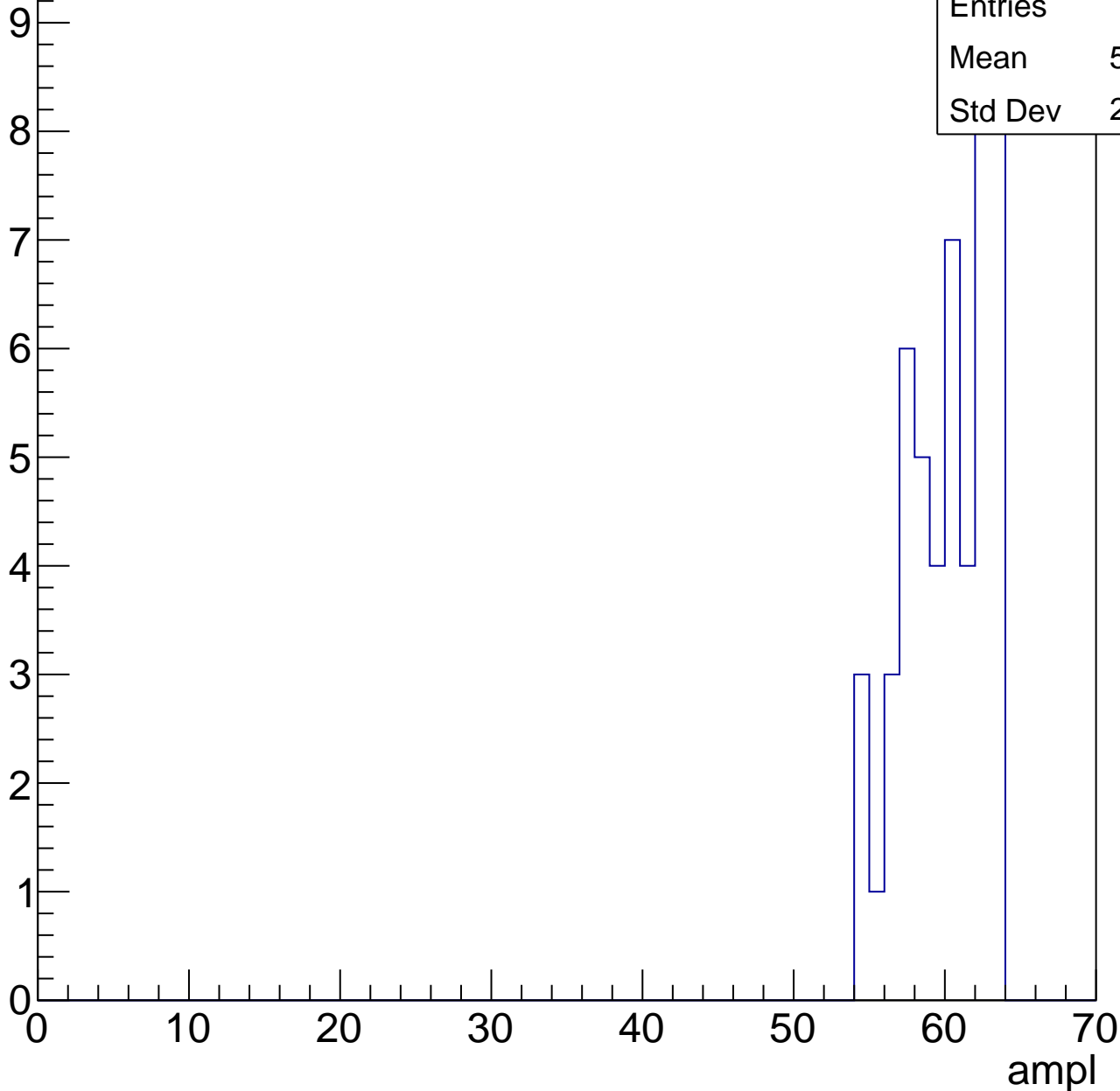


# B1L101S, U8-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

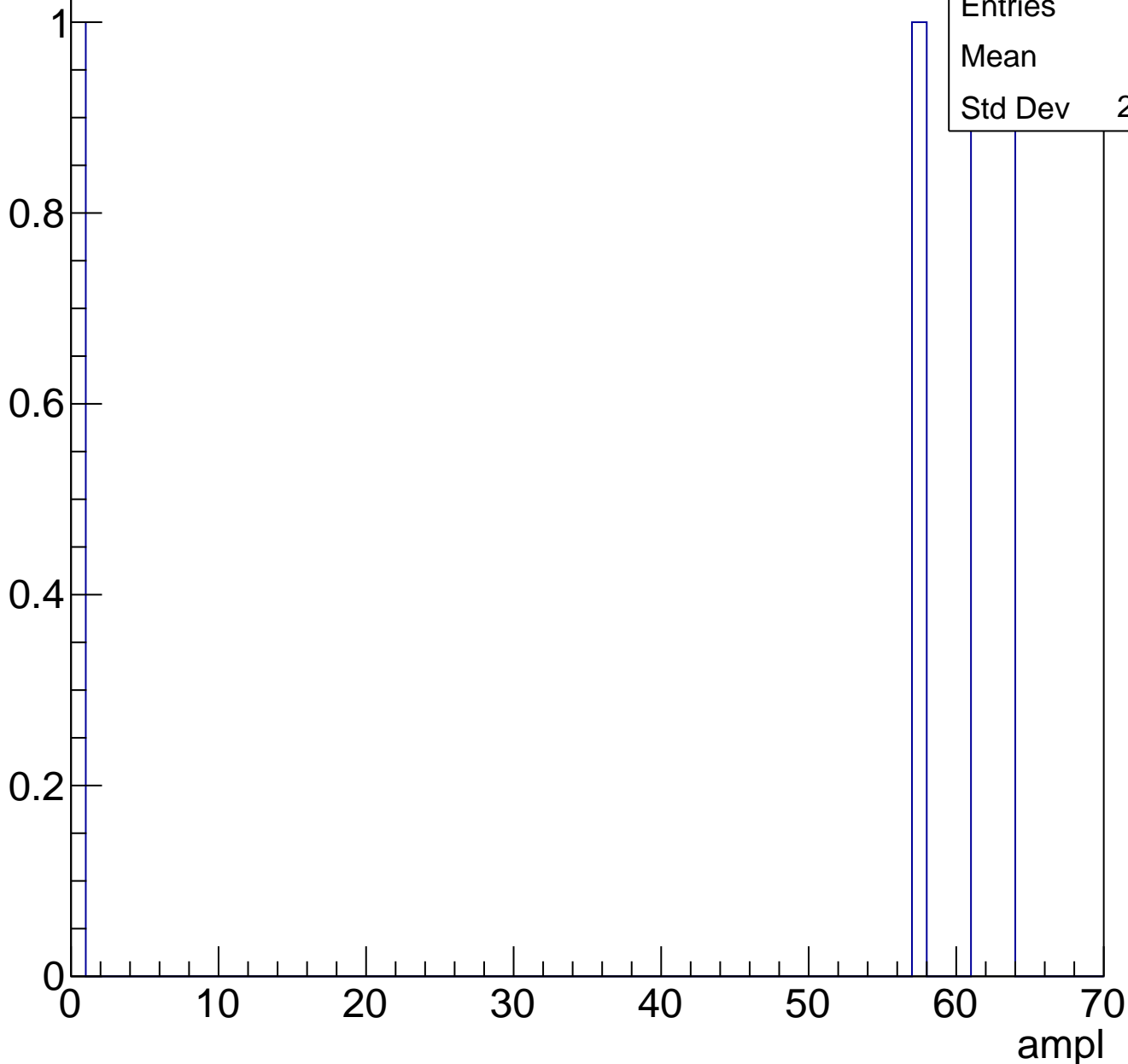
Entries	51
Mean	59.65
Std Dev	2.707



# B1L101S, U8-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U8-ch49, adc0

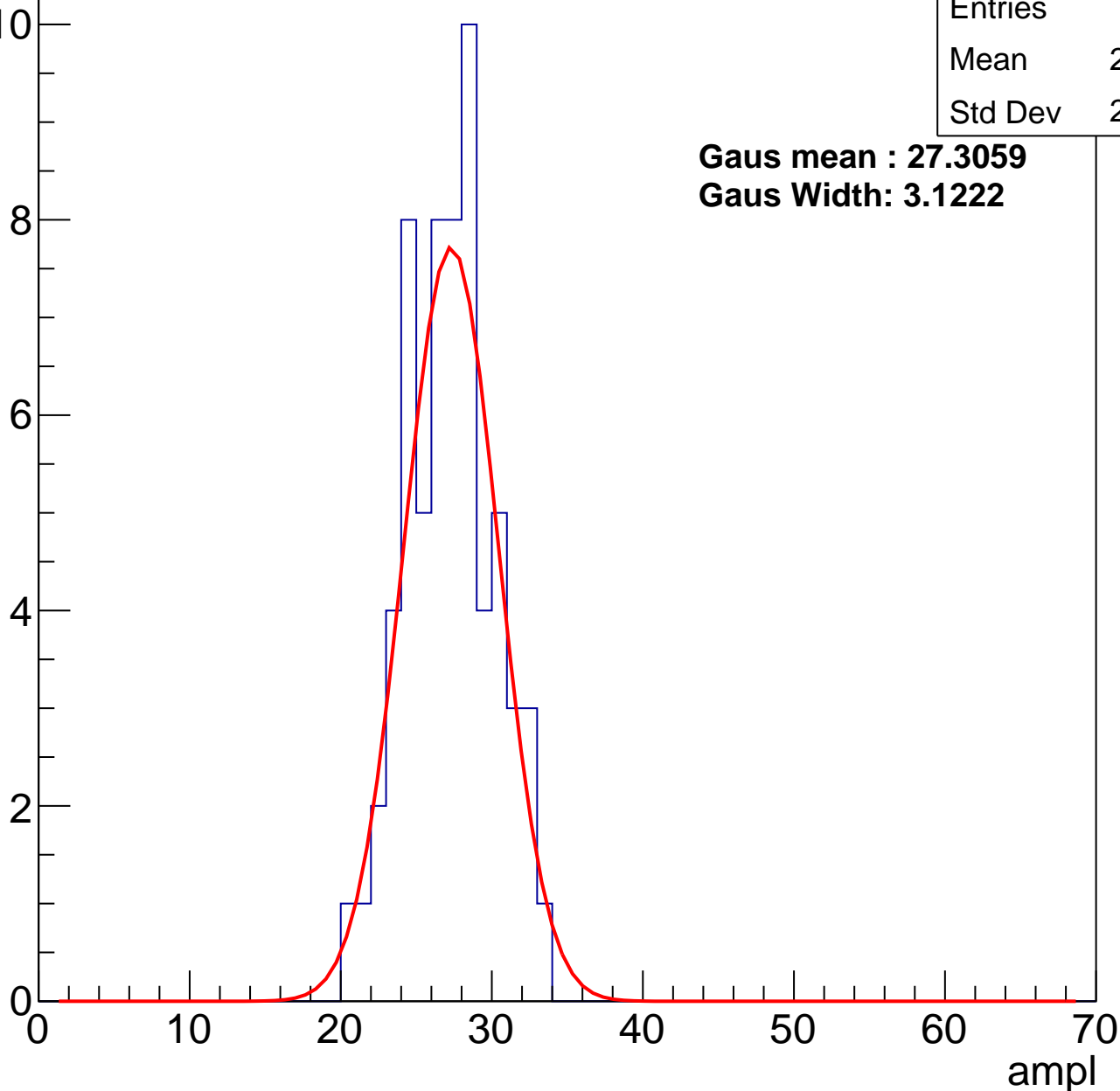
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	26.76
Std Dev	2.888

**Gaus mean : 27.3059**

**Gaus Width: 3.1222**



# B1L101S, U8-ch49, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	72
Mean	33.44
Std Dev	3.27

**Gaus mean : 33.5832**

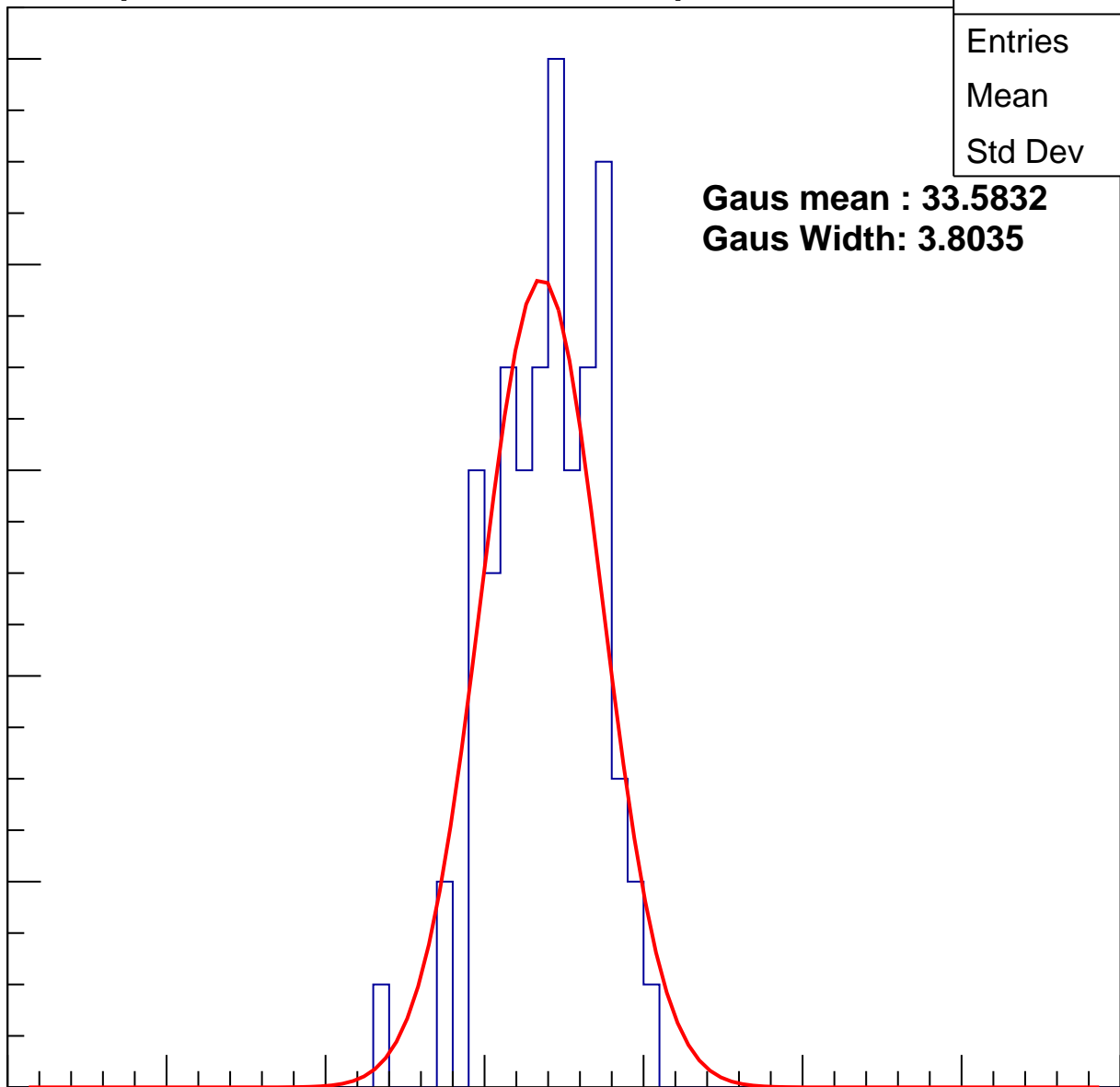
**Gaus Width: 3.8035**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U8-ch49, adc2

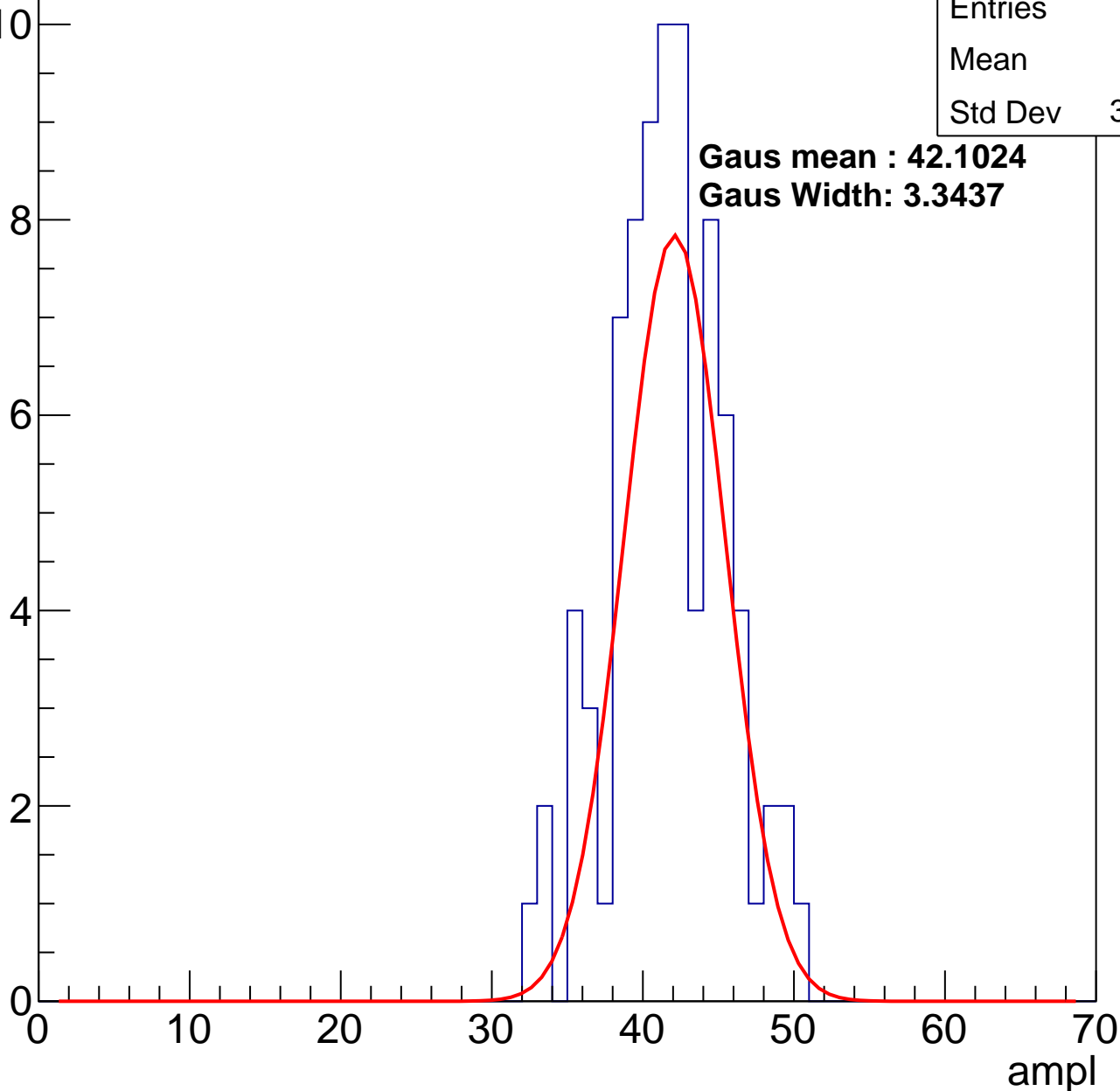
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	83
Mean	41.2
Std Dev	3.773

**Gaus mean : 42.1024**

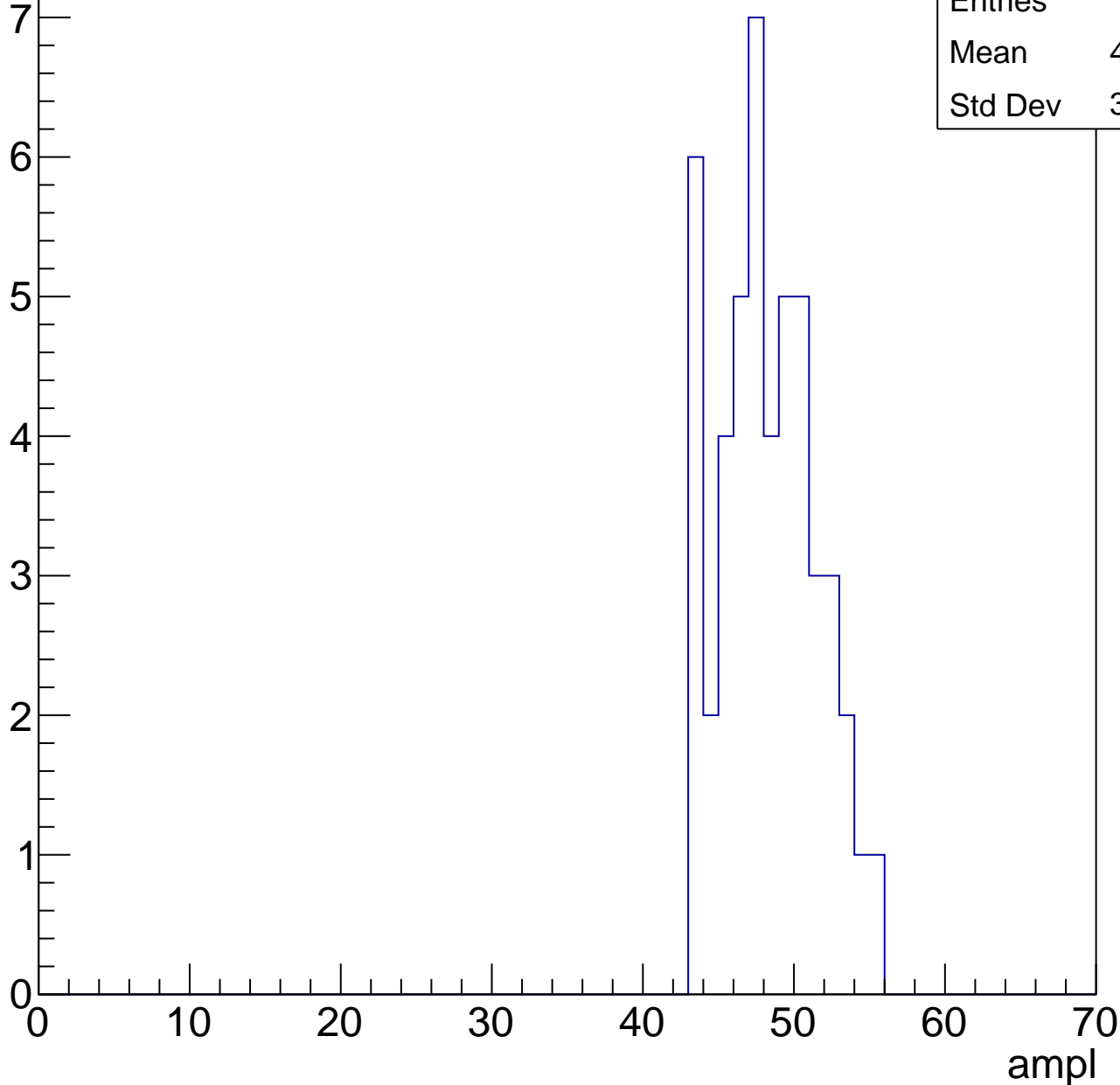
**Gaus Width: 3.3437**



# B1L101S, U8-ch49, adc3

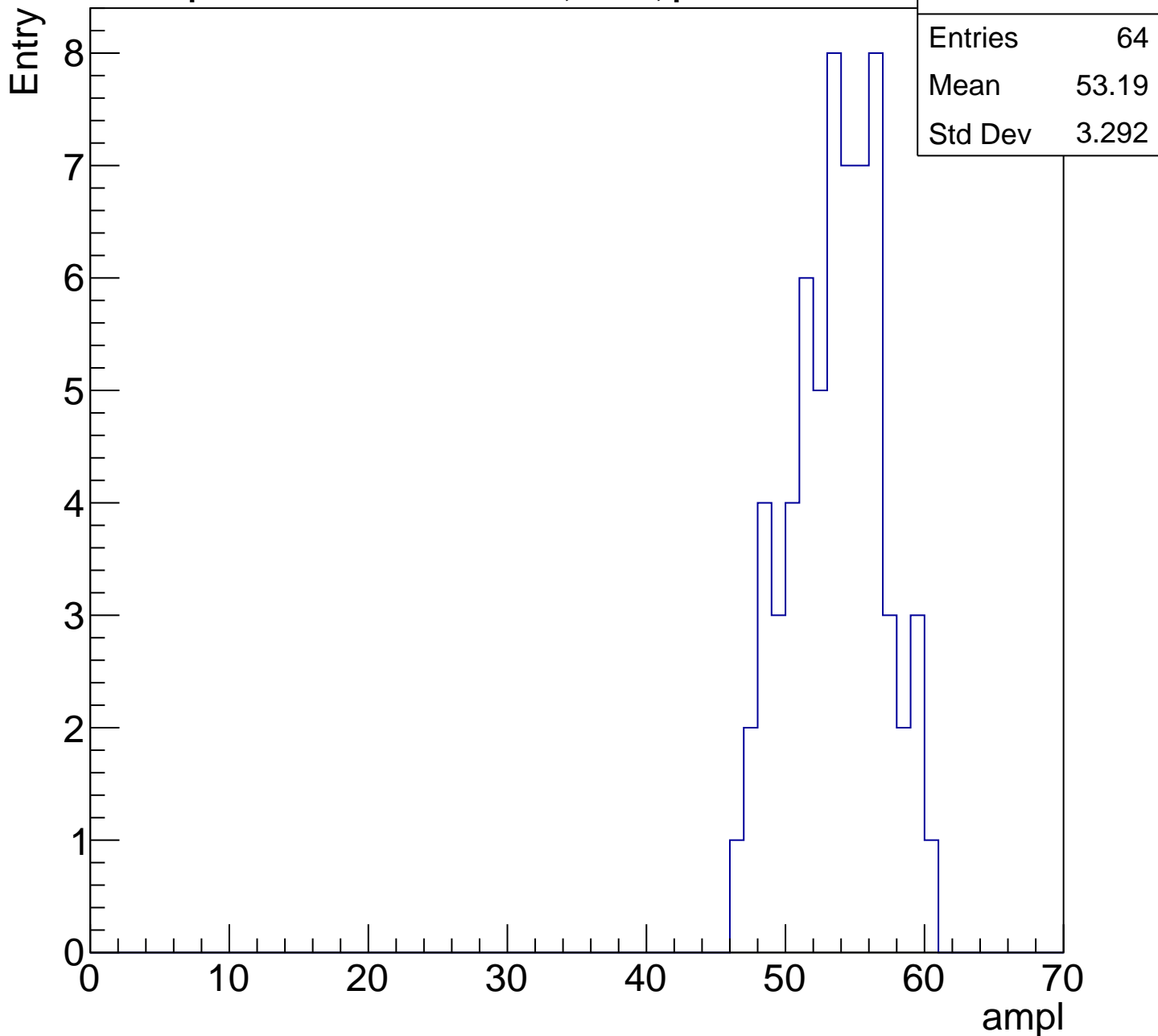
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch49, adc4

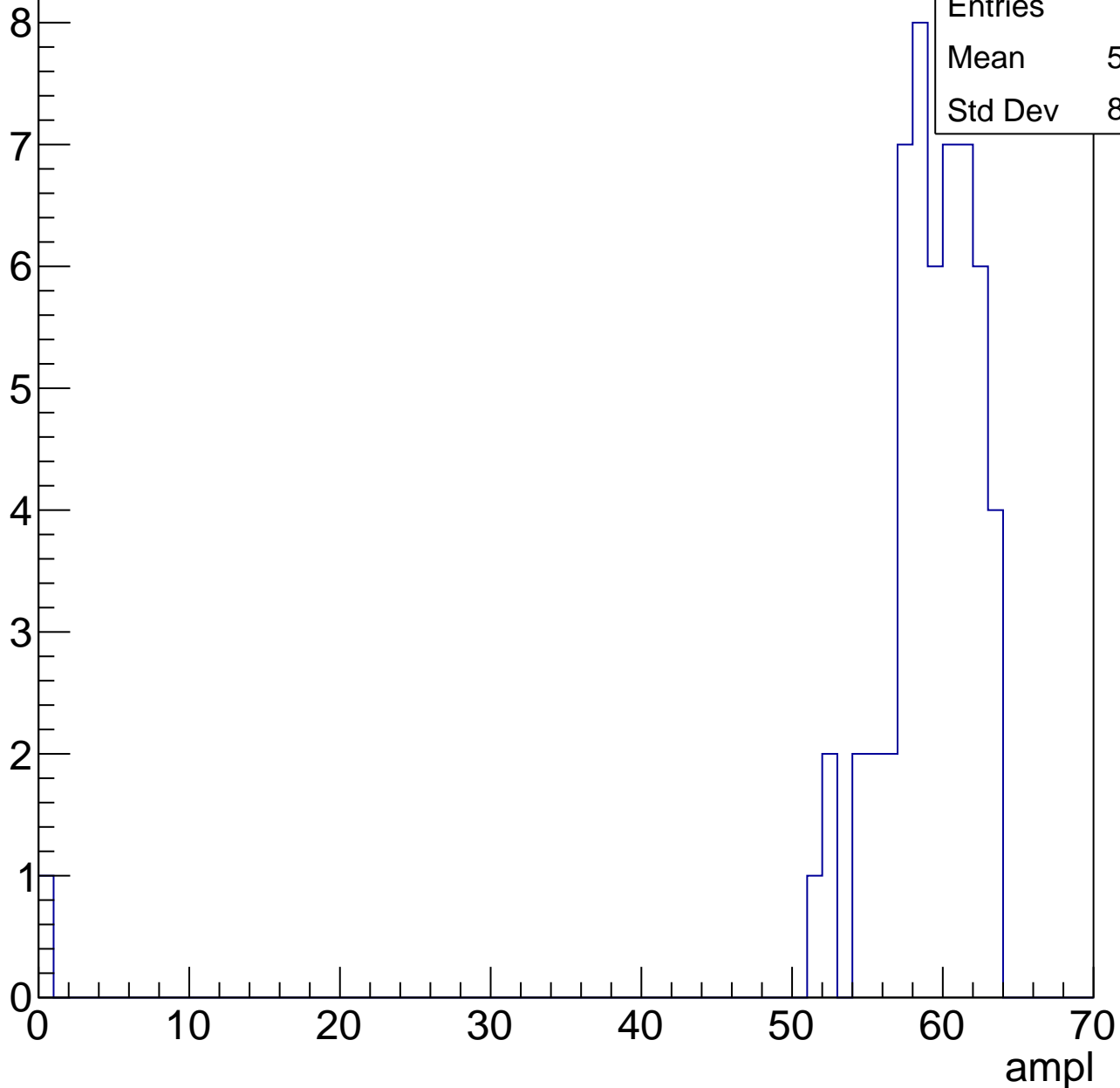
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U8-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

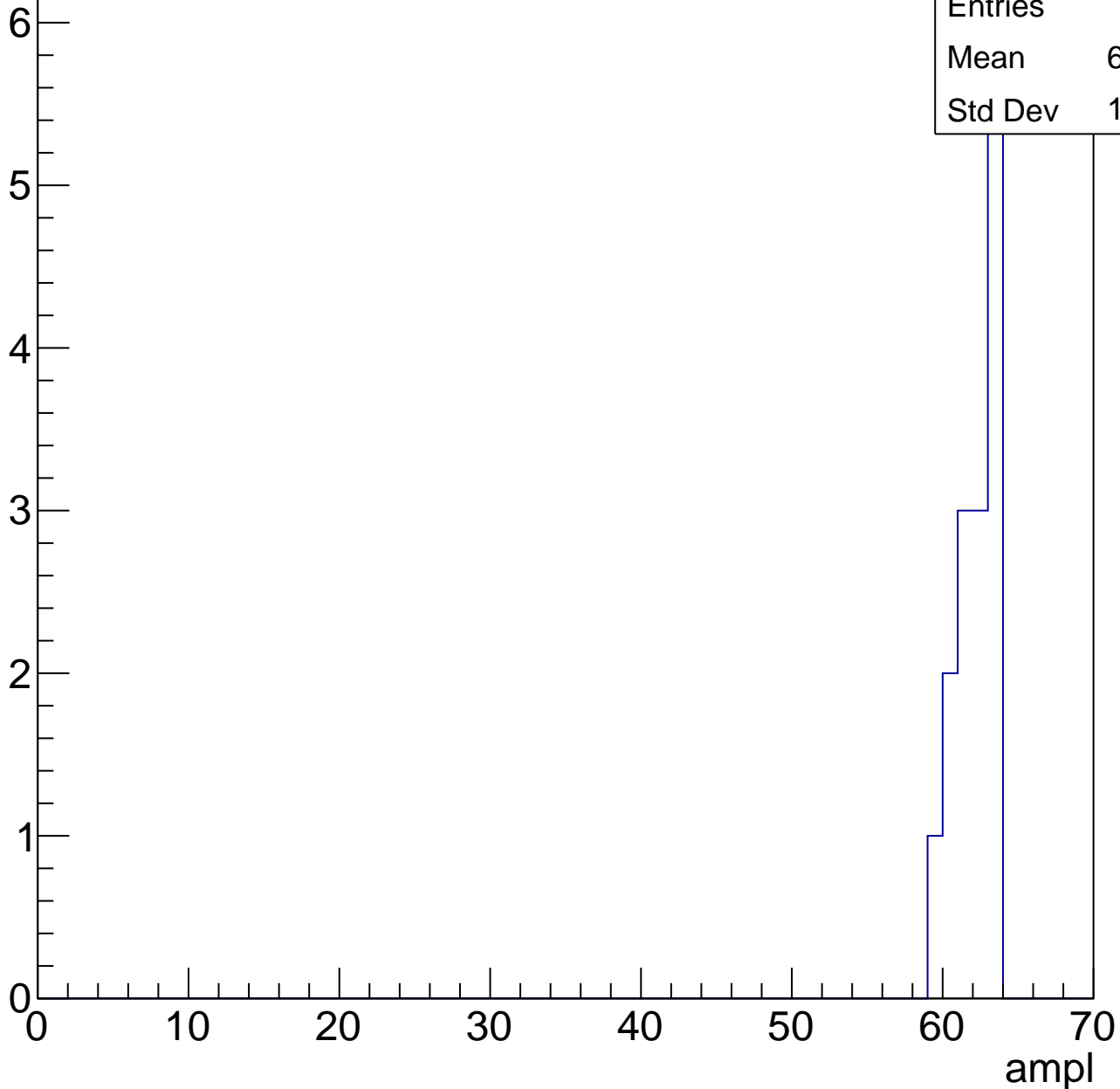


# B1L101S, U8-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	15
Mean	61.73
Std Dev	1.289





# B1L101S, U8-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

1

Mean

62

Std Dev

0

# B1L101S, U8-ch50, adc0

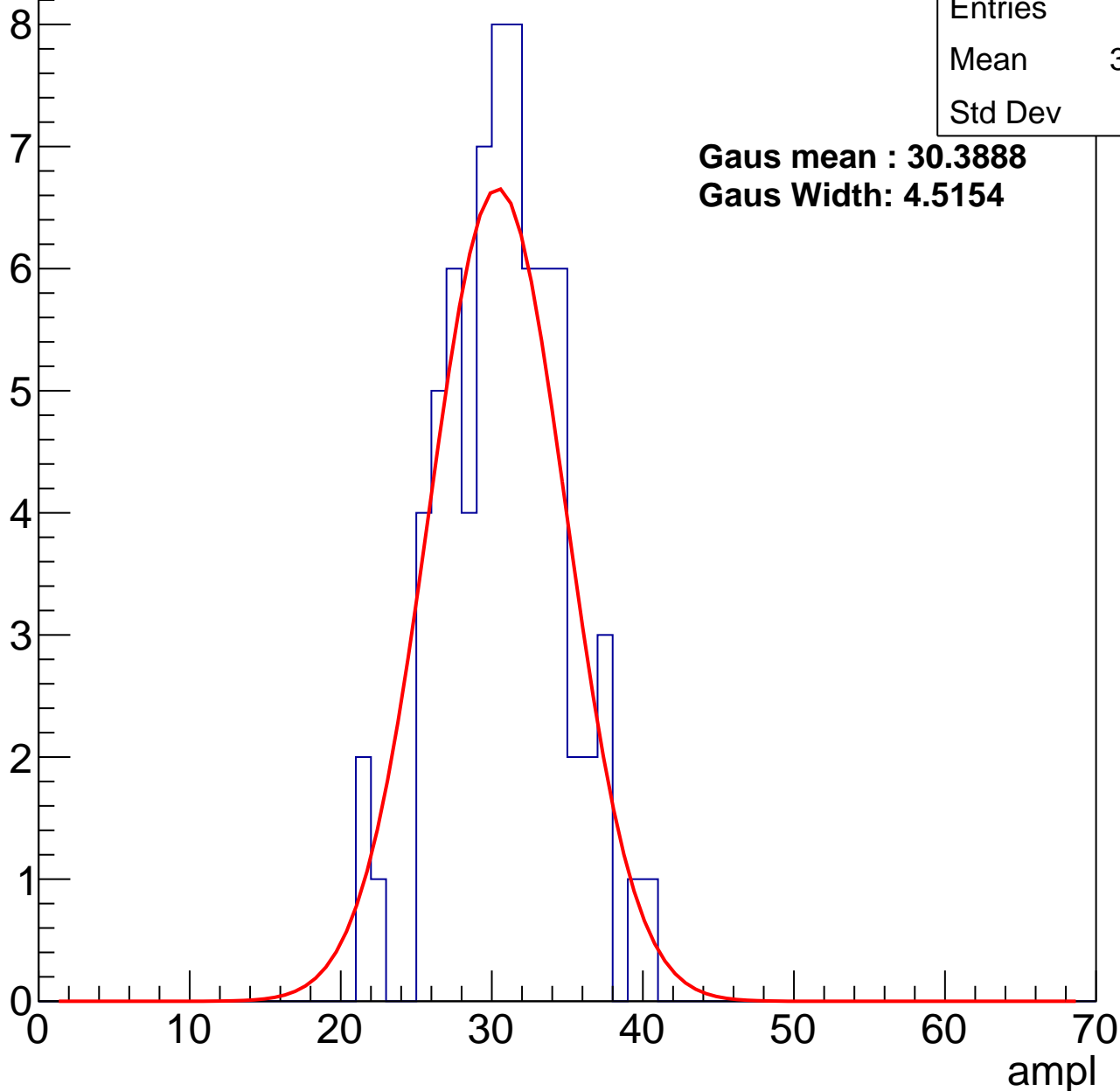
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	30.35
Std Dev	3.92

**Gaus mean : 30.3888**

**Gaus Width: 4.5154**



# B1L101S, U8-ch50, adc1

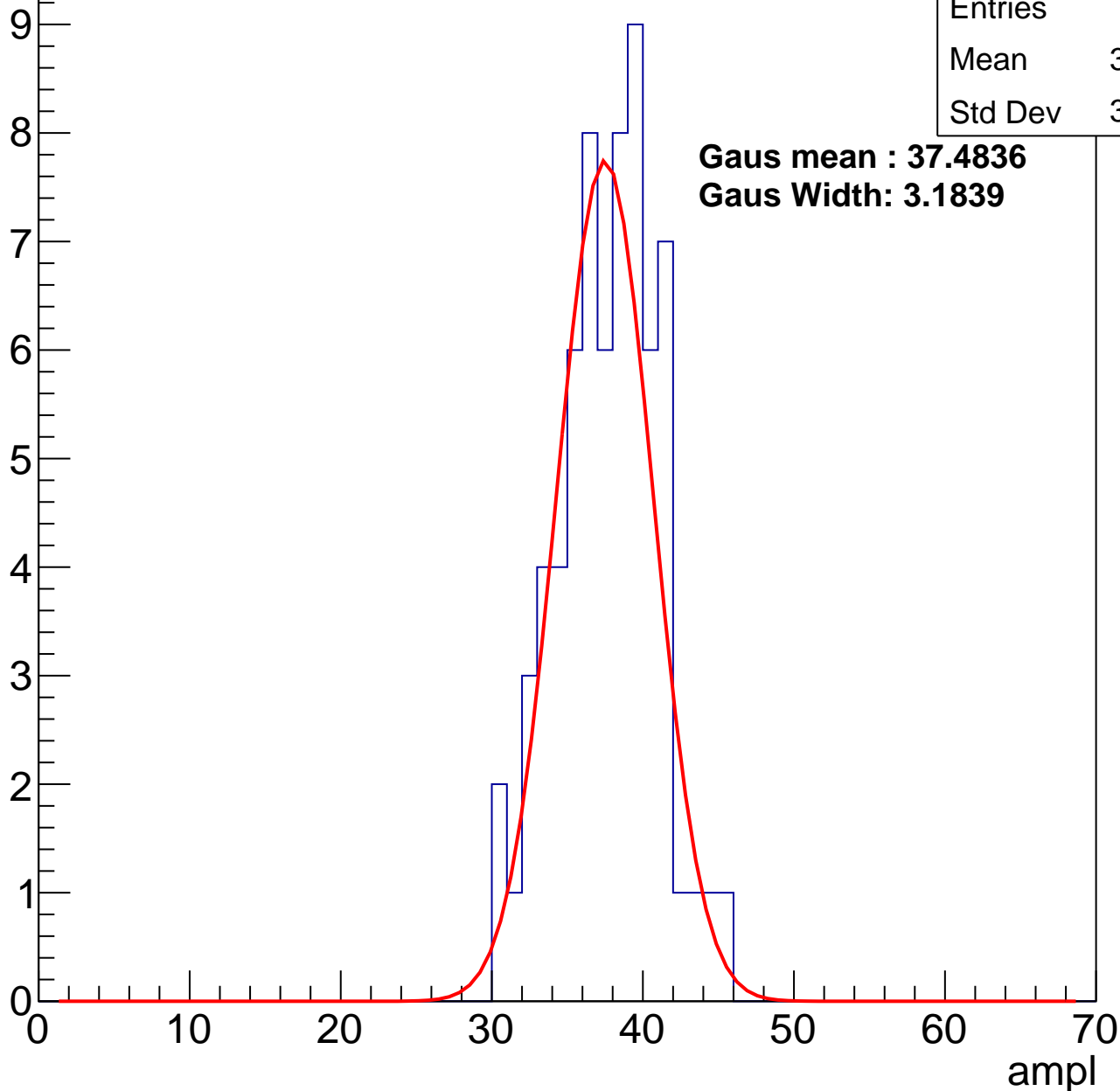
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	37.22
Std Dev	3.258

**Gaus mean : 37.4836**

**Gaus Width: 3.1839**



# B1L101S, U8-ch50, adc2

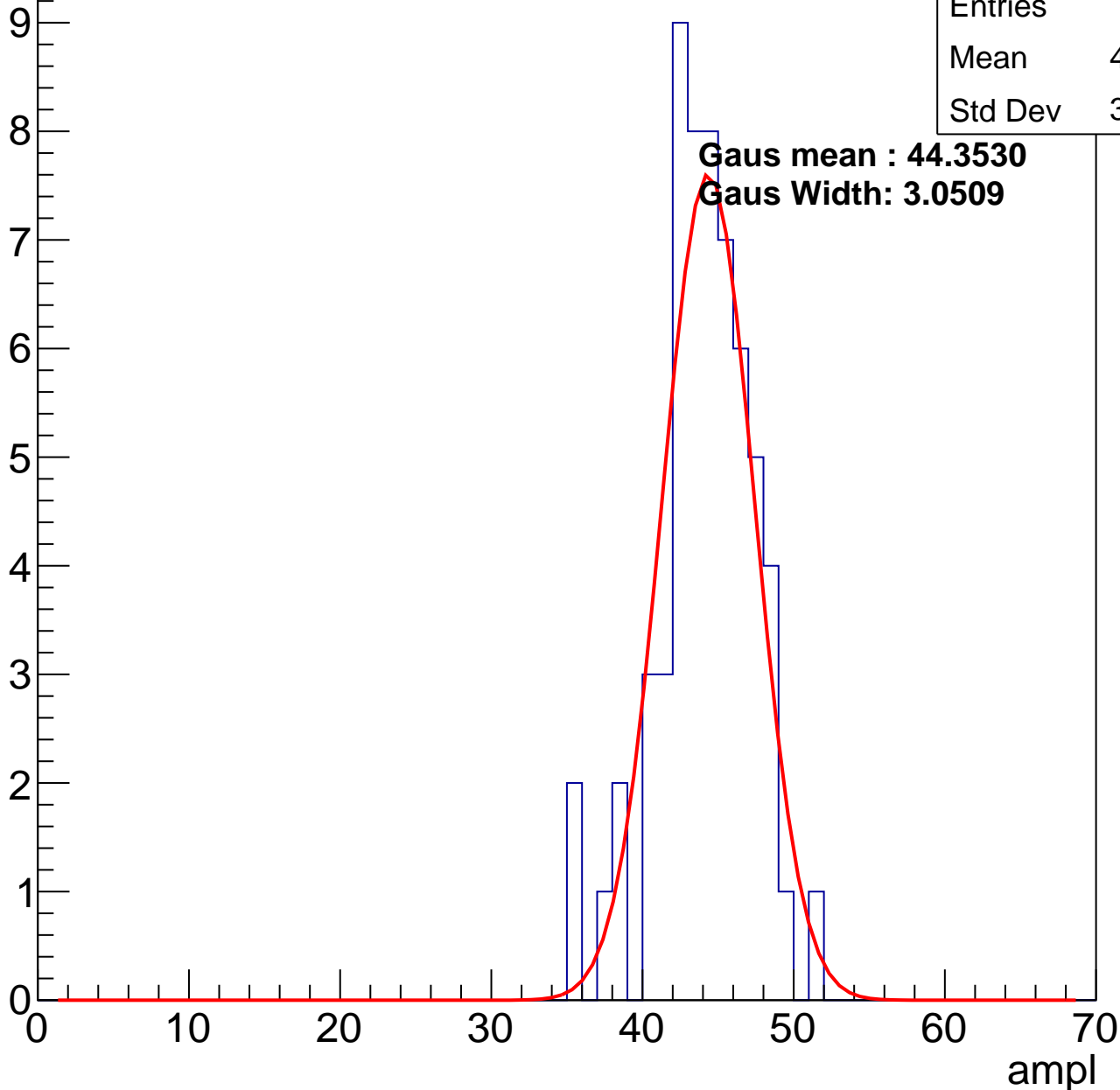
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	43.63
Std Dev	3.183

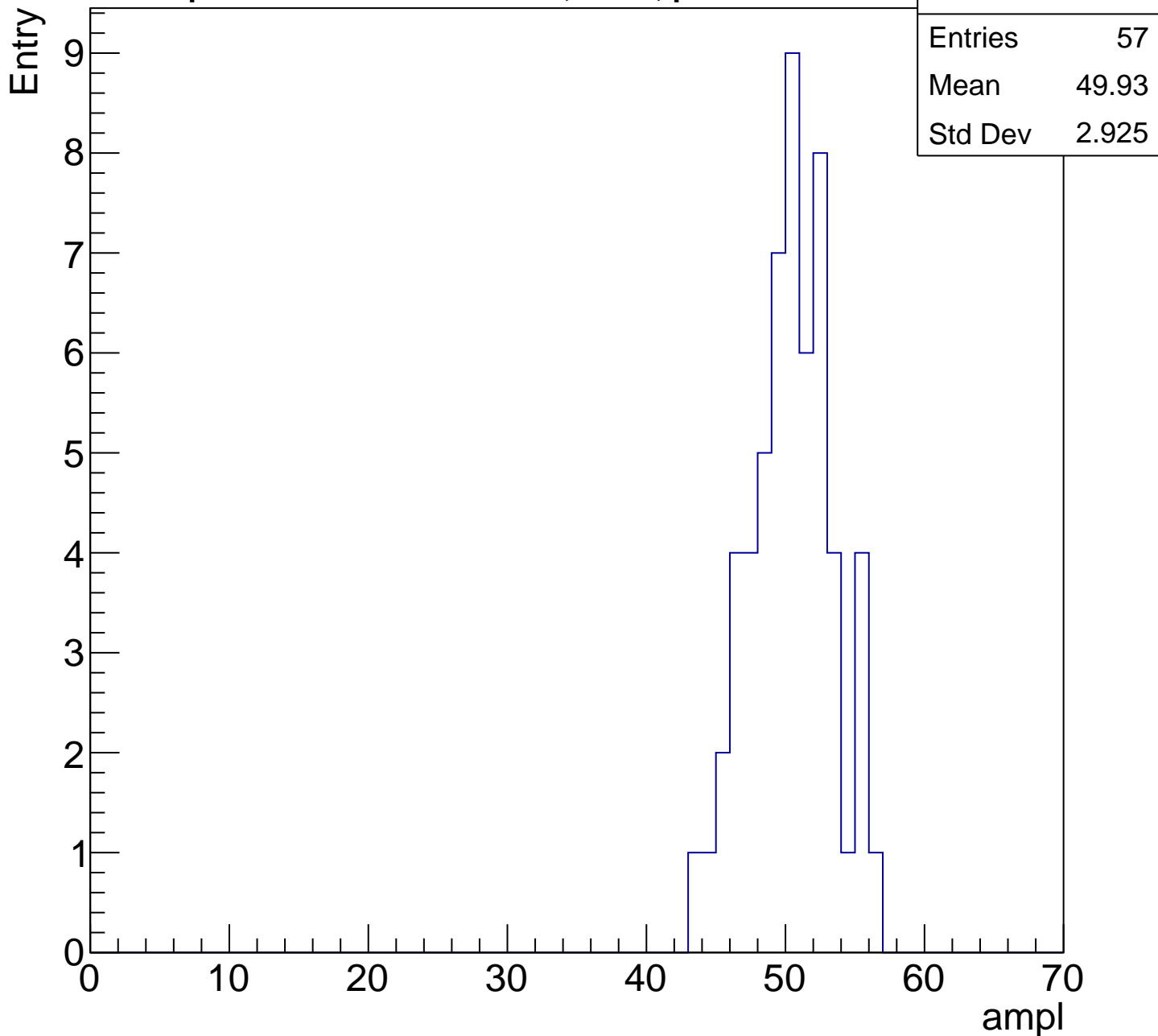
**Gaus mean : 44.3530**

**Gaus Width: 3.0509**



# B1L101S, U8-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

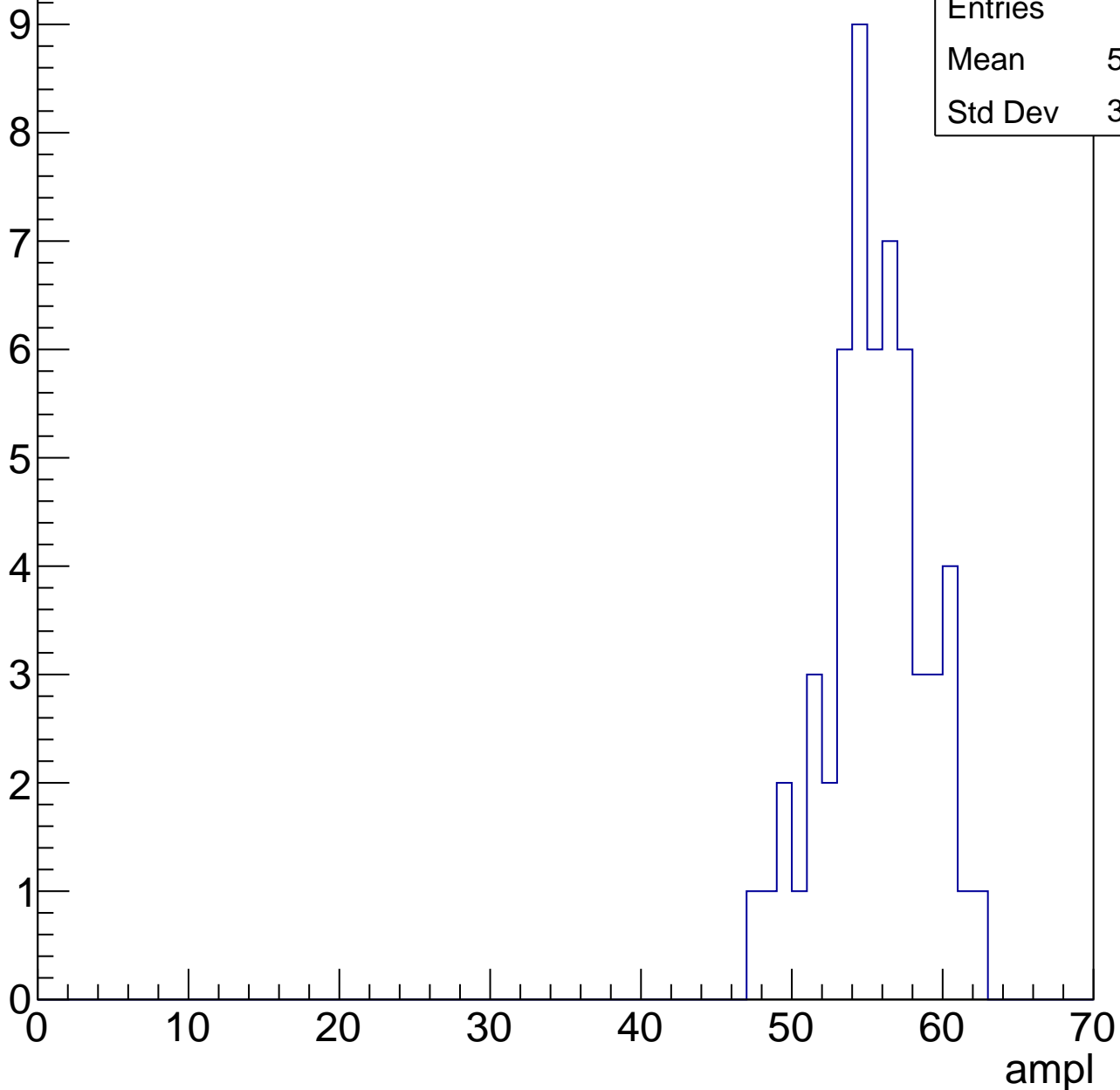


# B1L101S, U8-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	55.04
Std Dev	3.273



# B1L101S, U8-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	45
Mean	58.64
Std Dev	9.07

ampl

0

10

20

30

40

50

60

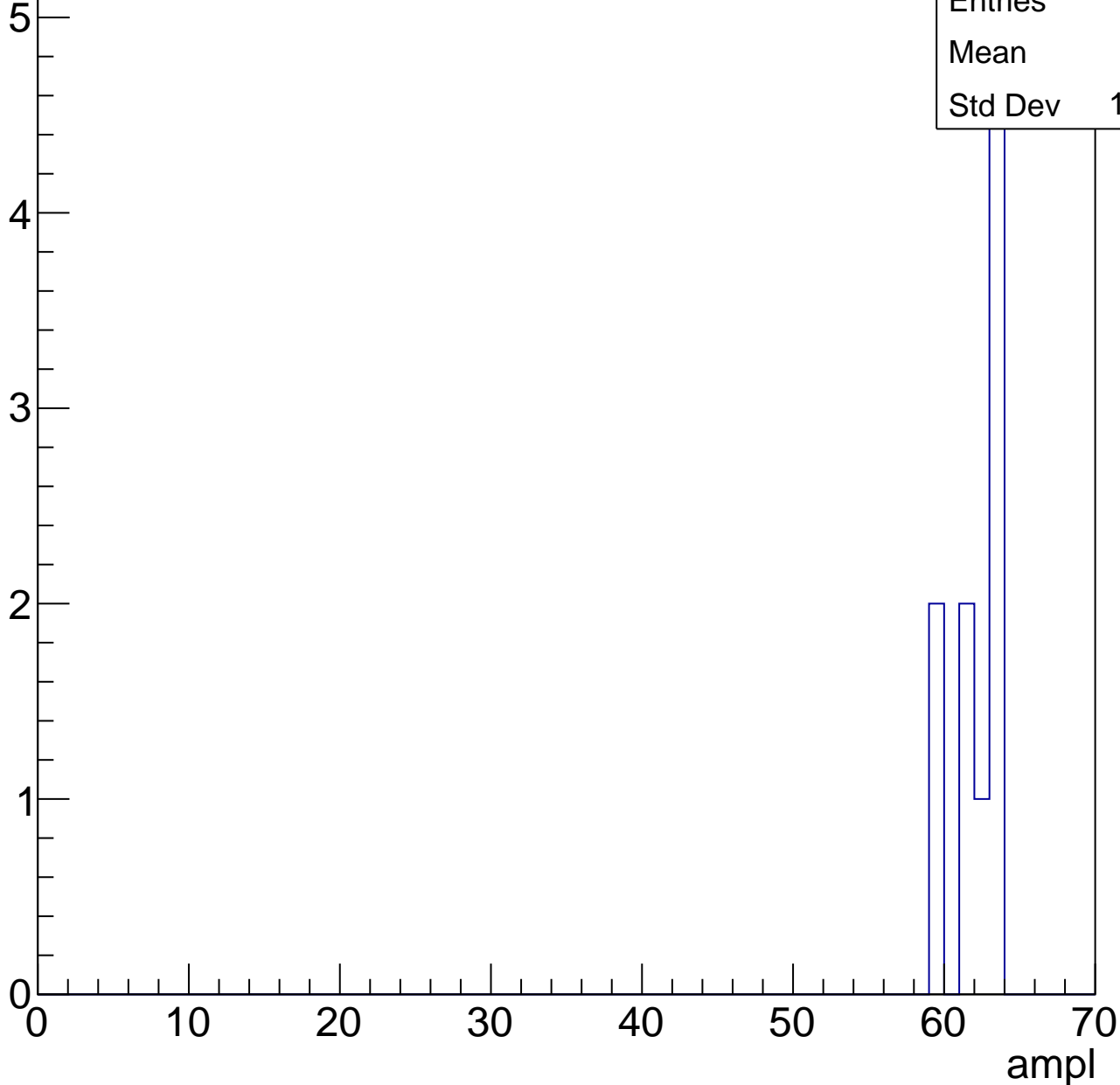
70

# B1L101S, U8-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	10
Mean	61.7
Std Dev	1.552





# B1L101S, U8-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch51, adc0

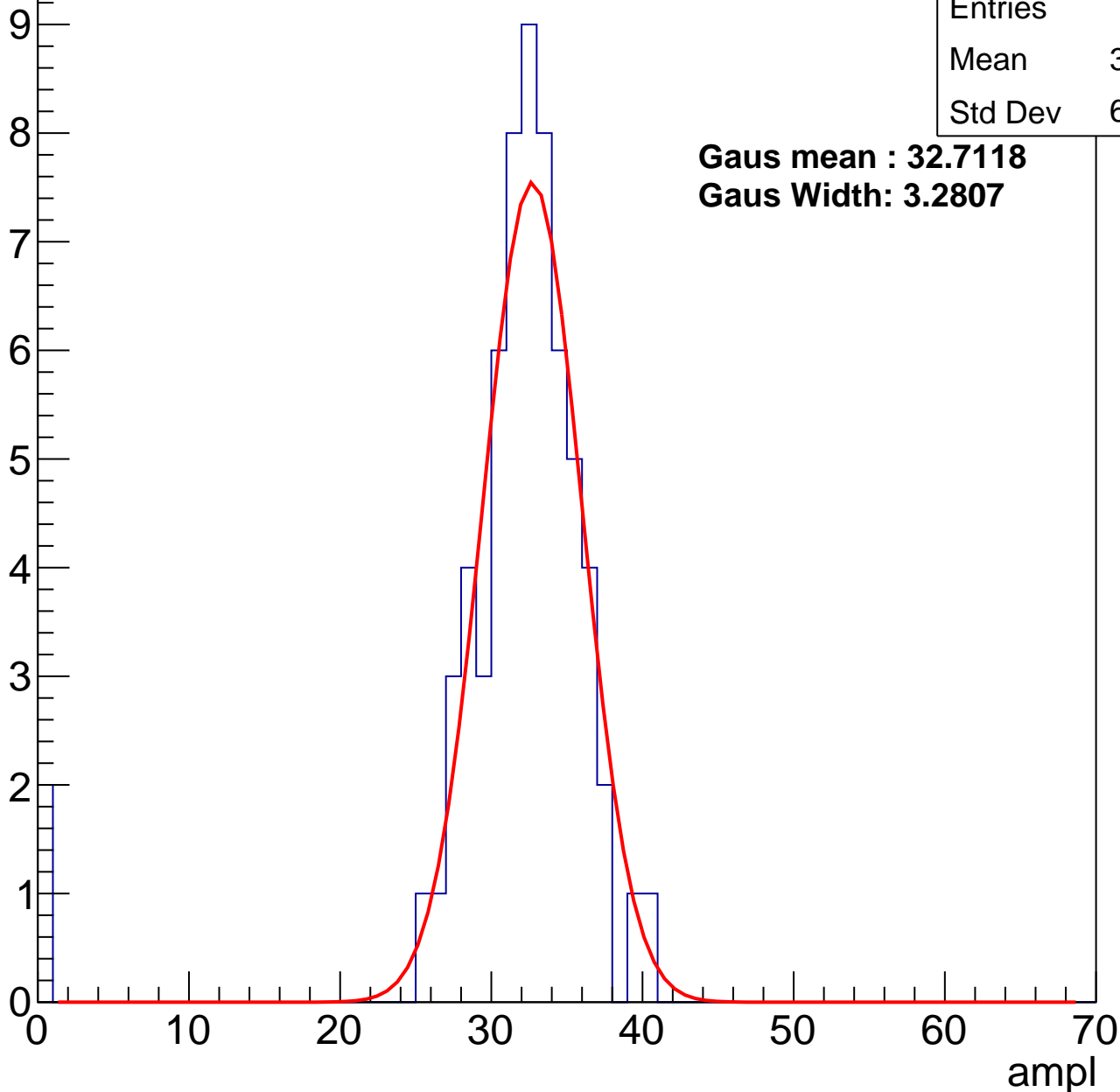
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	31.05
Std Dev	6.345

**Gaus mean : 32.7118**

**Gaus Width: 3.2807**



# B1L101S, U8-ch51, adc1

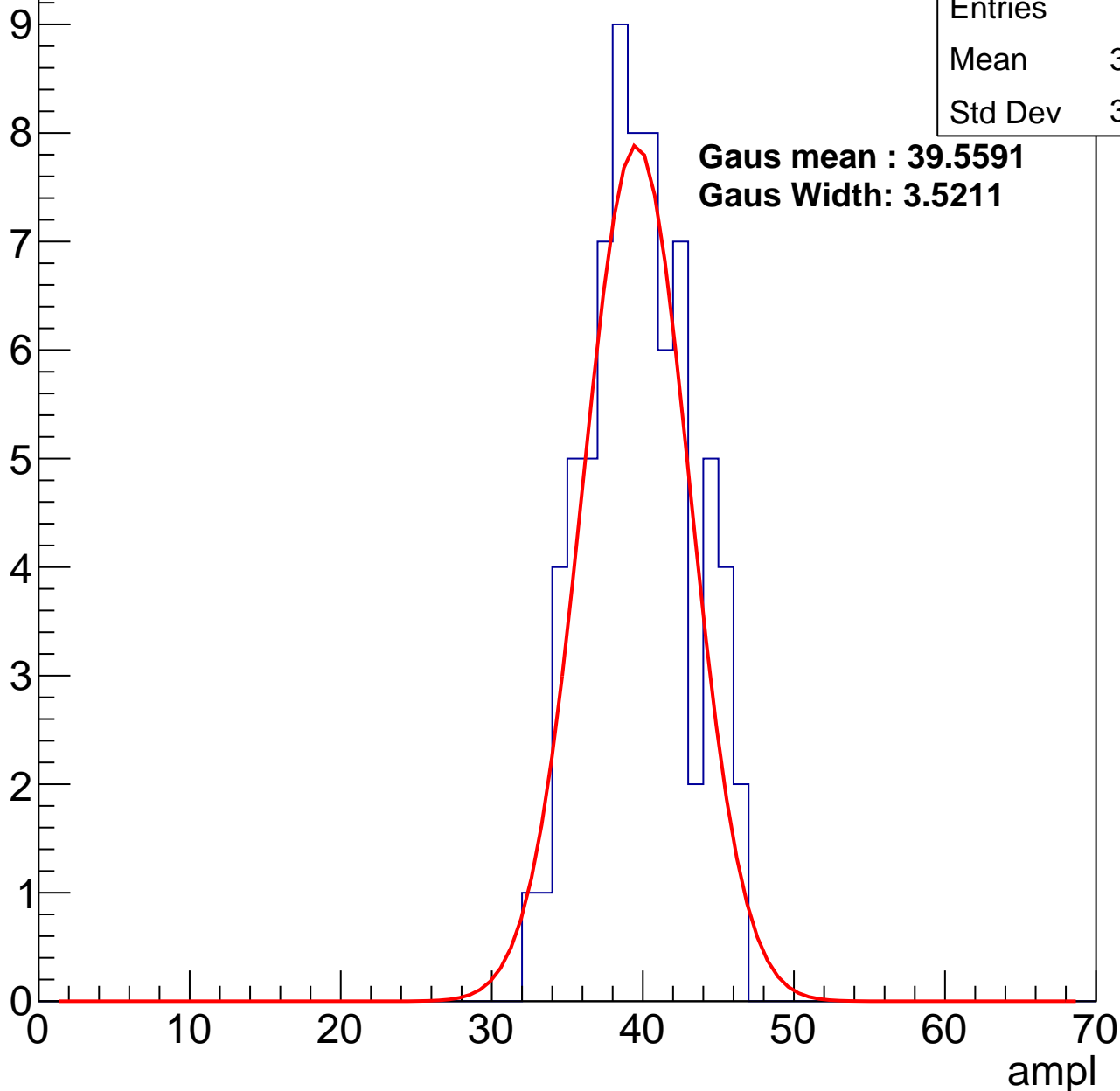
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	39.28
Std Dev	3.359

**Gaus mean : 39.5591**

**Gaus Width: 3.5211**



# B1L101S, U8-ch51, adc2

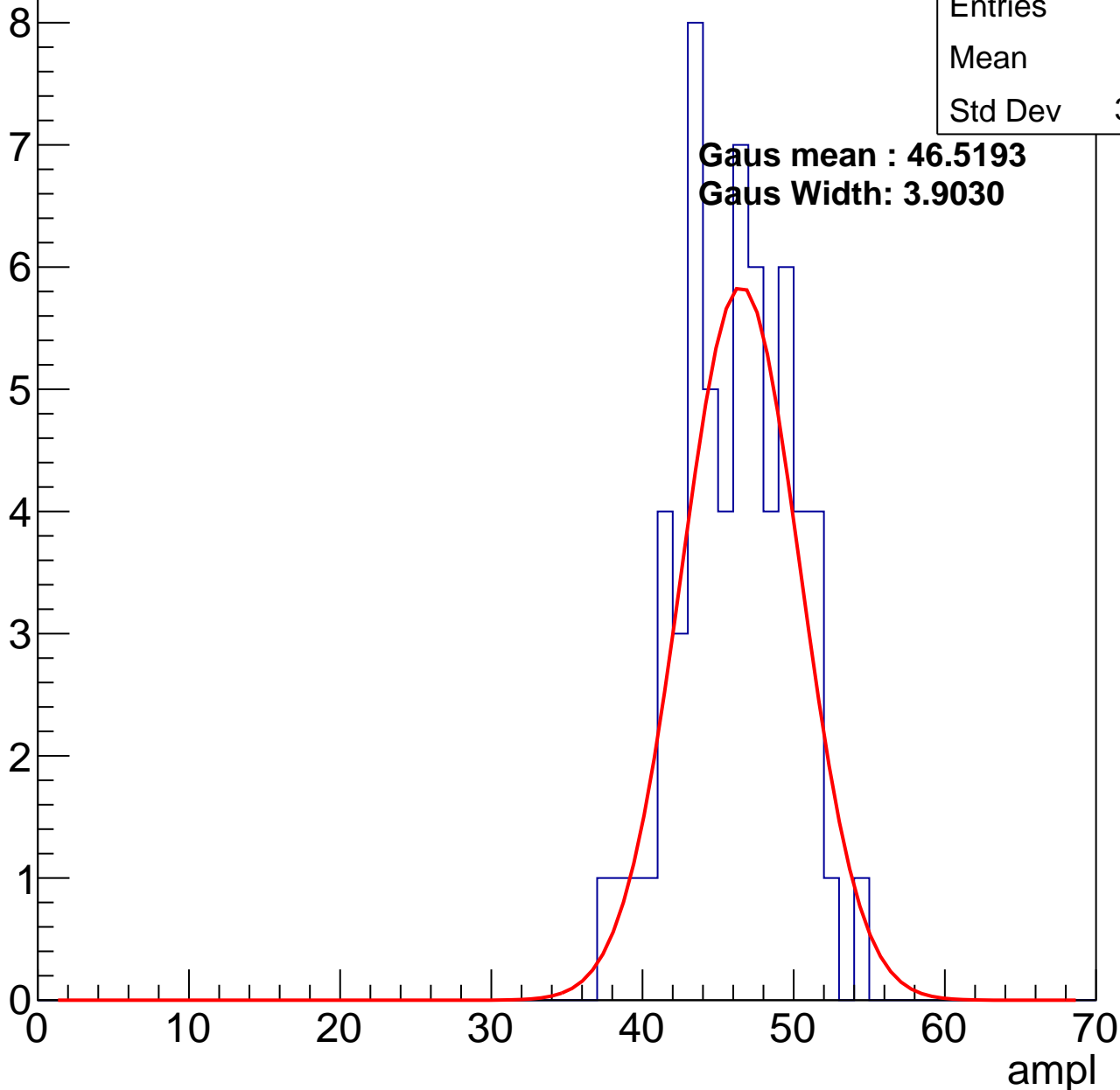
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	45.7
Std Dev	3.641

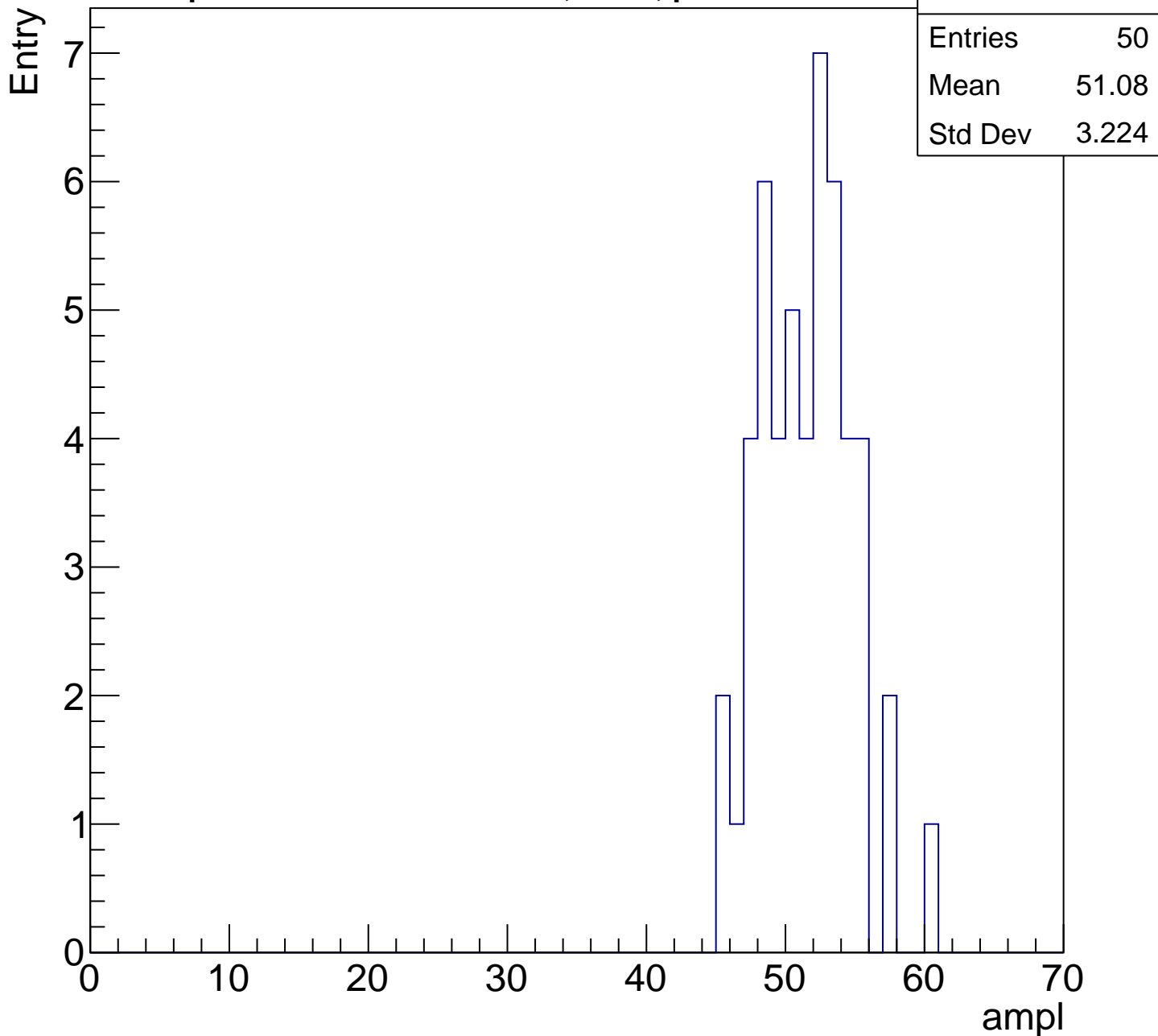
**Gaus mean : 46.5193**

**Gaus Width: 3.9030**



# B1L101S, U8-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

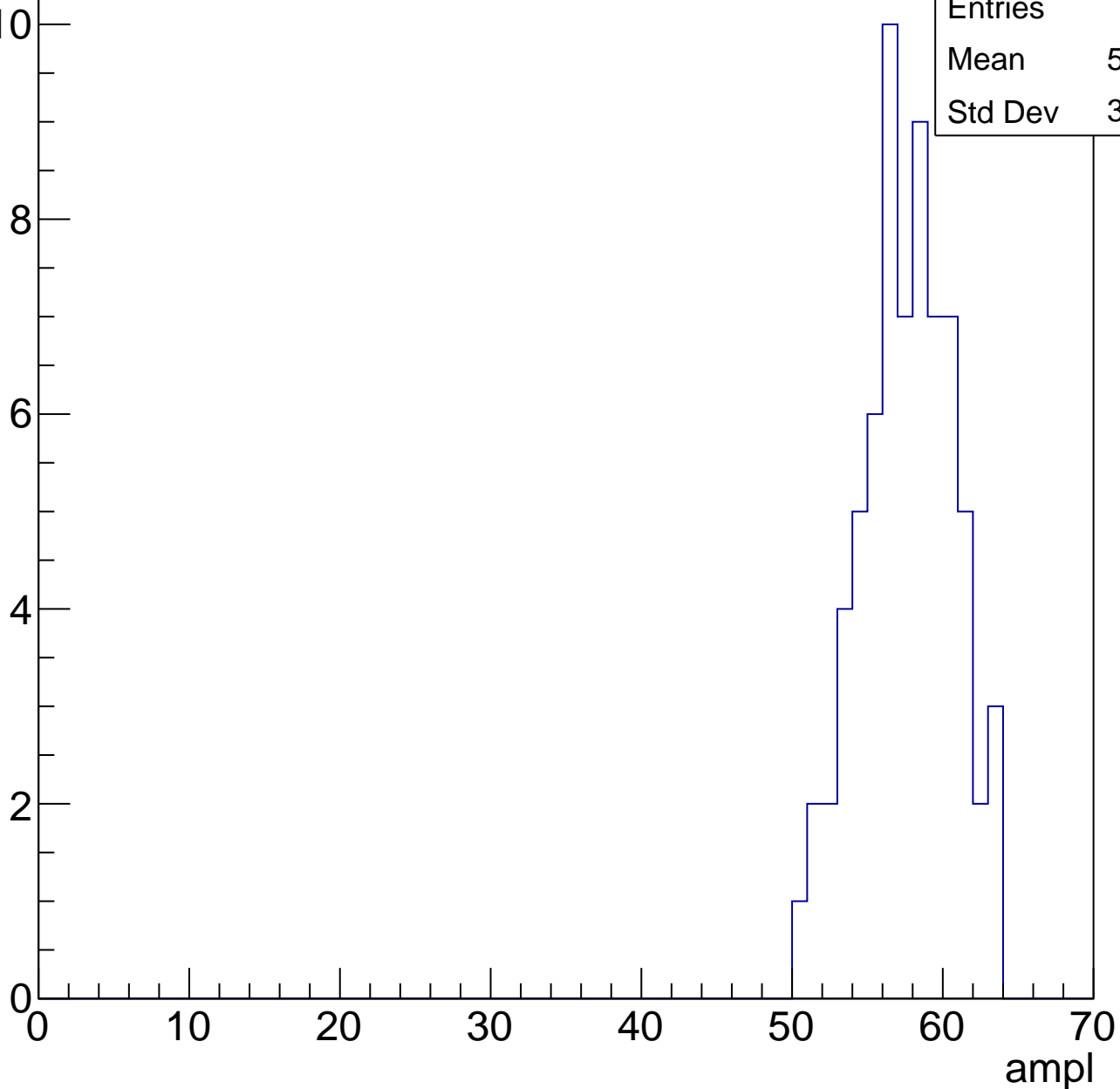


# B1L101S, U8-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	57.14
Std Dev	3.049



# B1L101S, U8-ch51, adc5

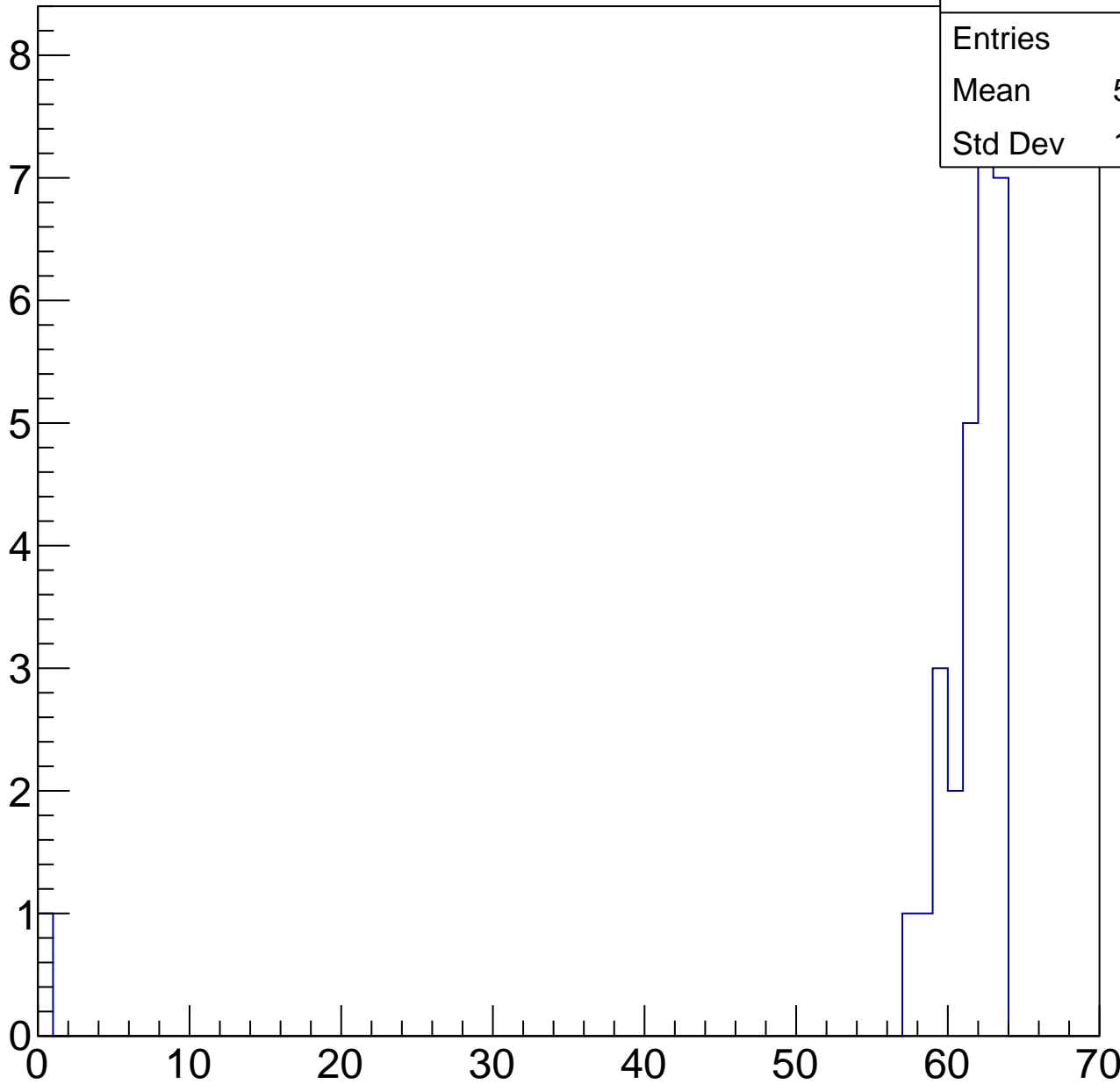
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	28
Mean	59.07
Std Dev	11.48

ampl



# B1L101S, U8-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L101S, U8-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch52, adc0

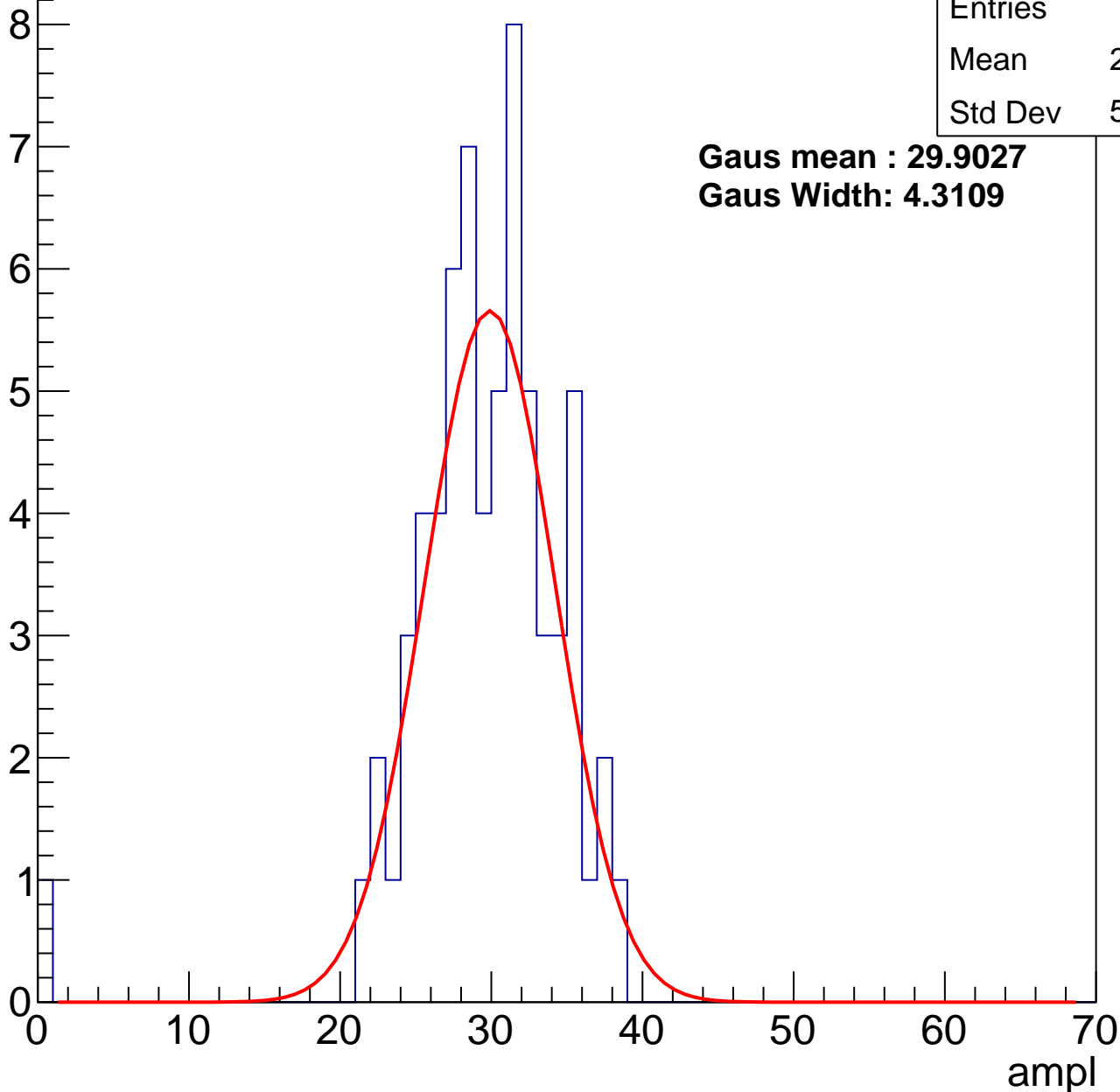
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	29.09
Std Dev	5.348

**Gaus mean : 29.9027**

**Gaus Width: 4.3109**



# B1L101S, U8-ch52, adc1

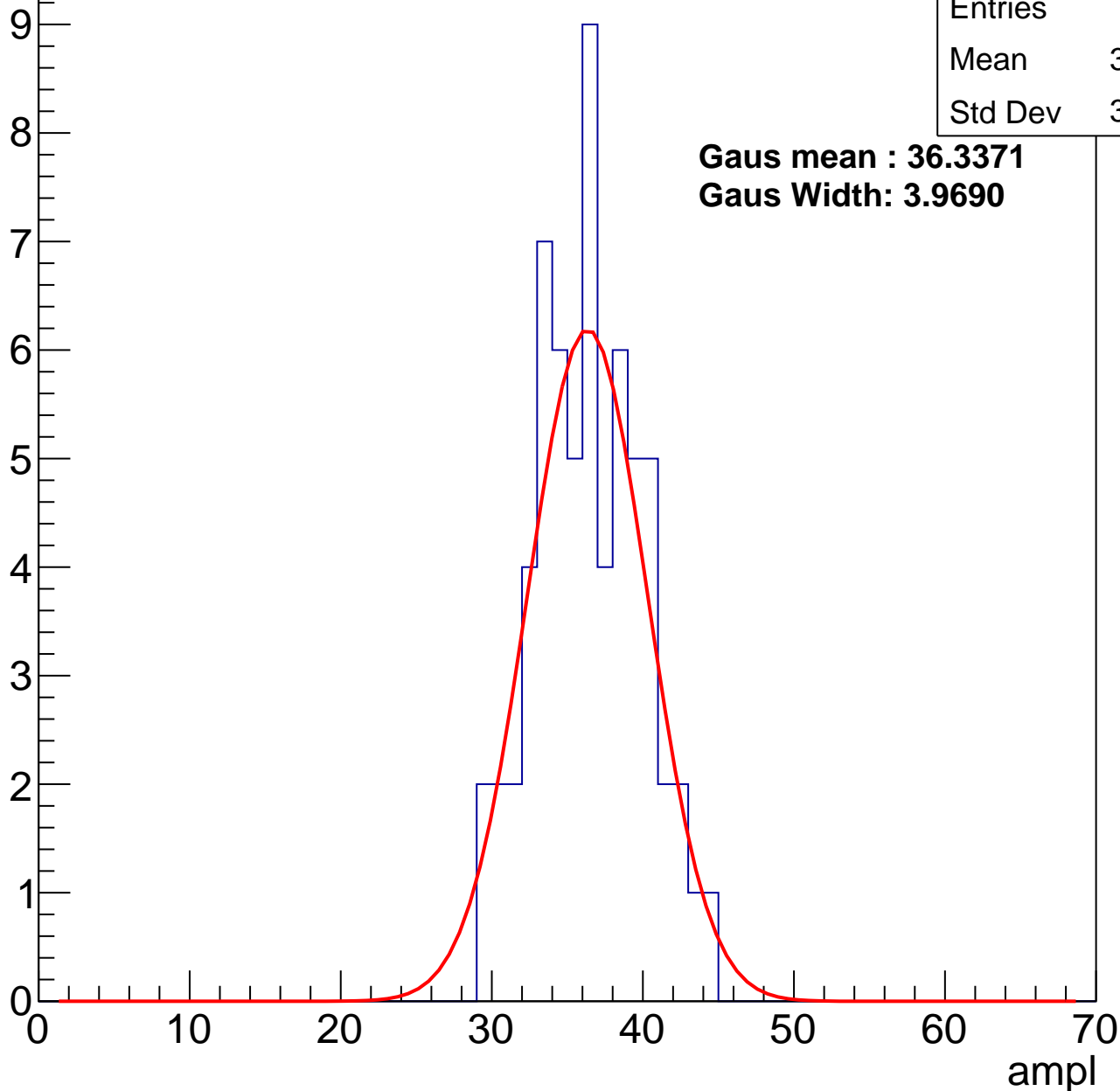
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	35.97
Std Dev	3.482

**Gaus mean : 36.3371**

**Gaus Width: 3.9690**



# B1L101S, U8-ch52, adc2

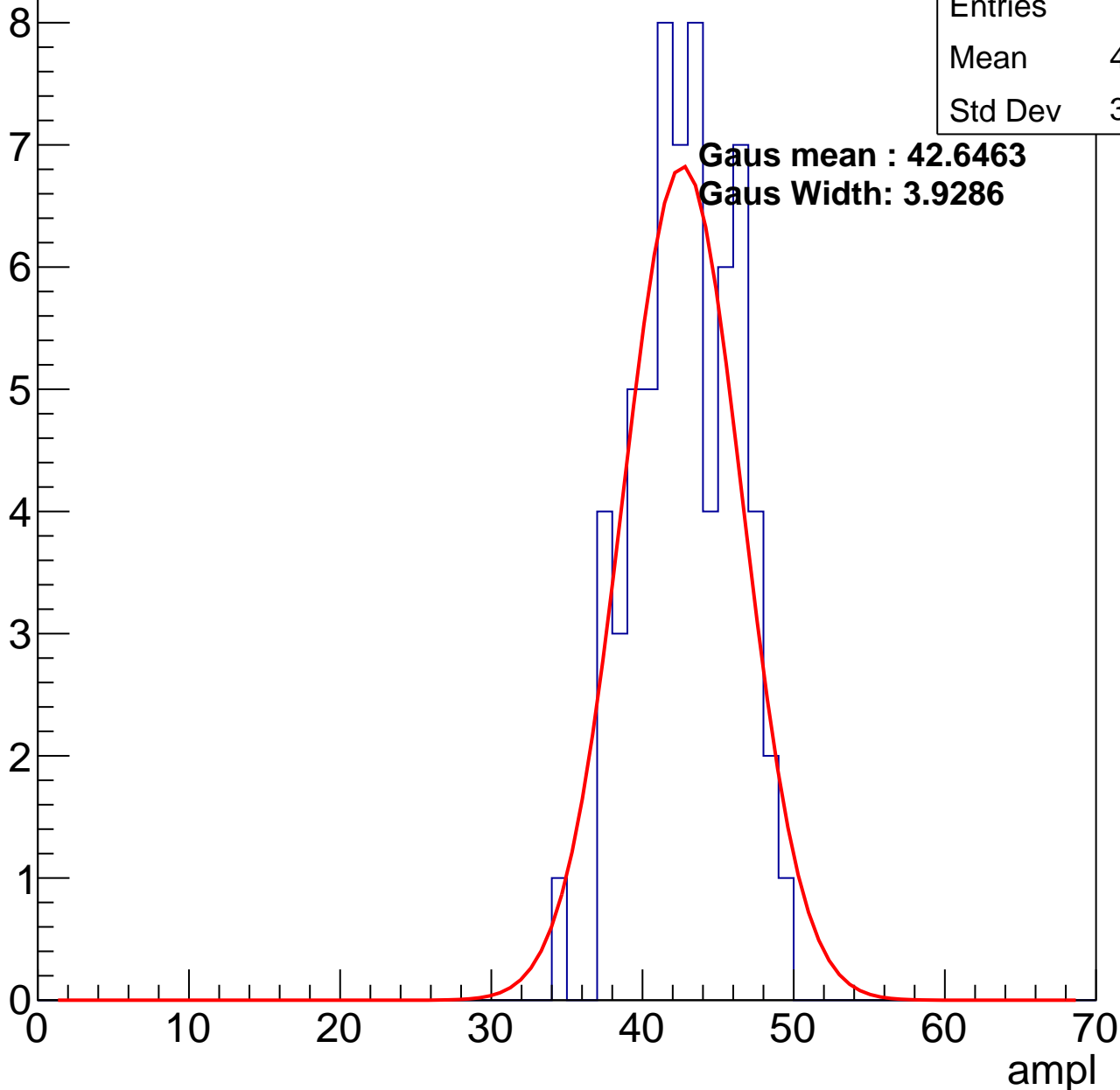
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	42.43
Std Dev	3.244

**Gaus mean : 42.6463**

**Gaus Width: 3.9286**

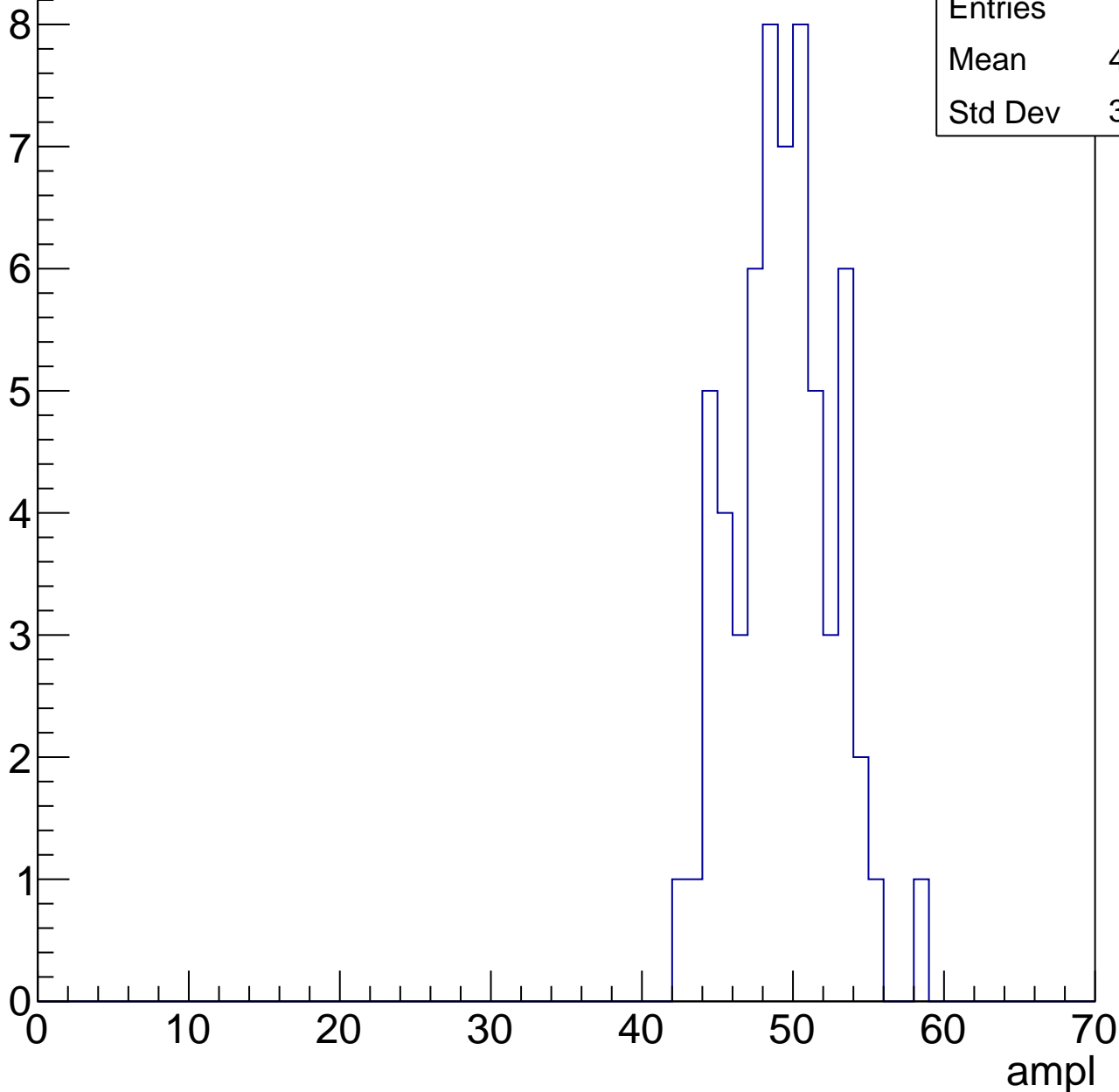


# B1L101S, U8-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

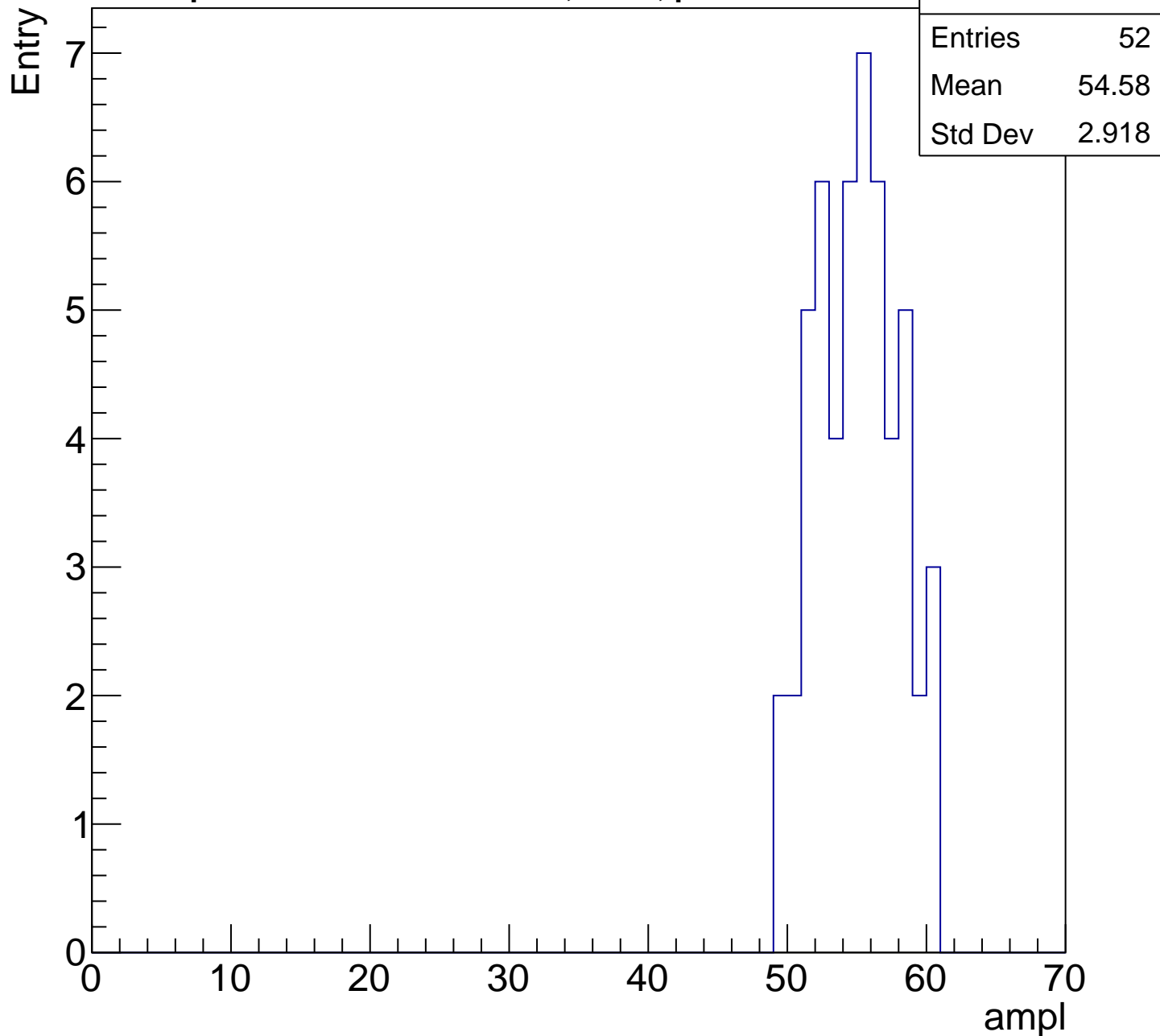
Entry

Entries	61
Mean	48.89
Std Dev	3.265



# B1L101S, U8-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

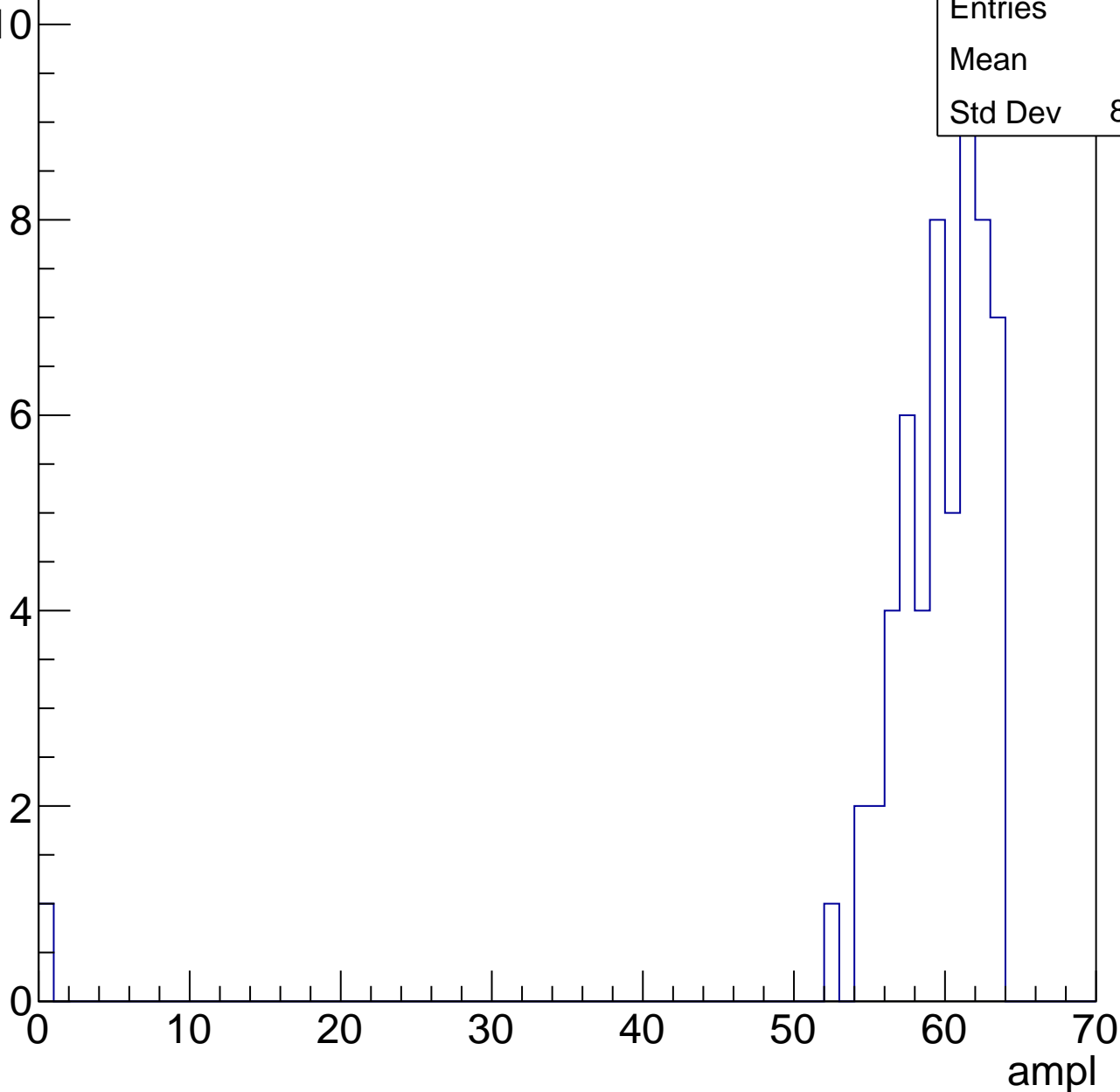


# B1L101S, U8-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

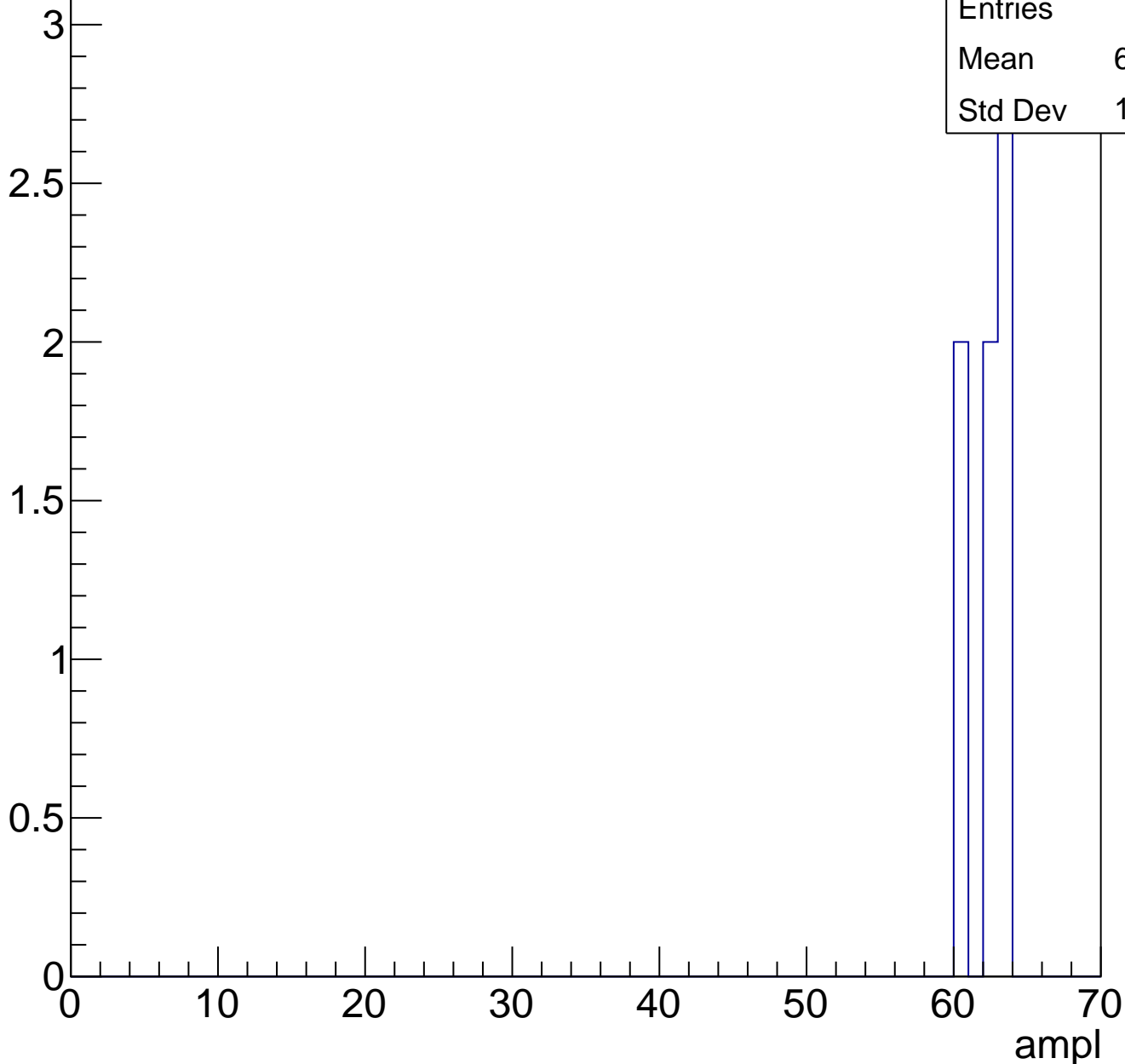
Entries	58
Mean	58.4
Std Dev	8.183



# B1L101S, U8-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch53, adc0

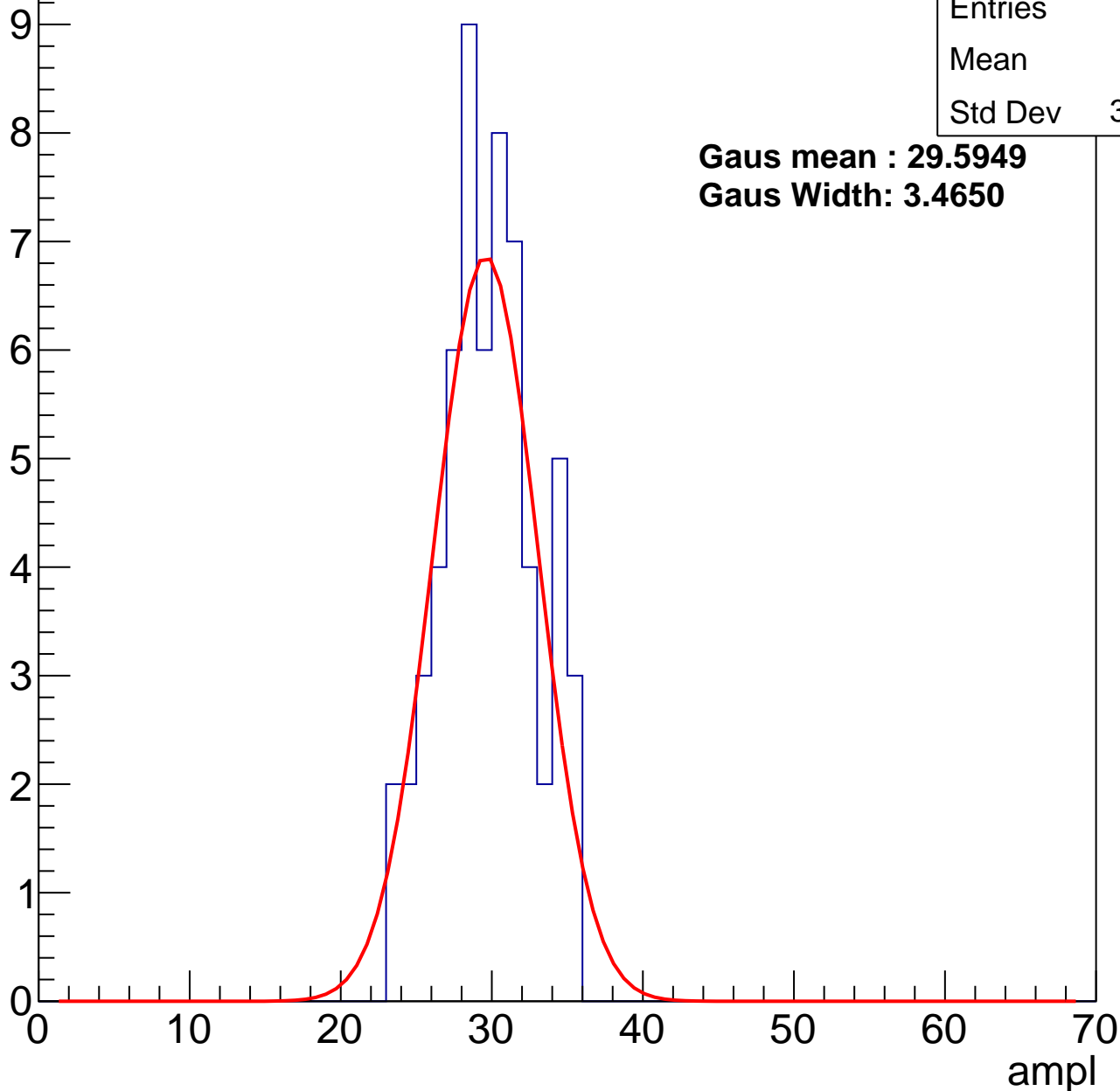
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	29.3
Std Dev	3.059

**Gaus mean : 29.5949**

**Gaus Width: 3.4650**



# B1L101S, U8-ch53, adc1

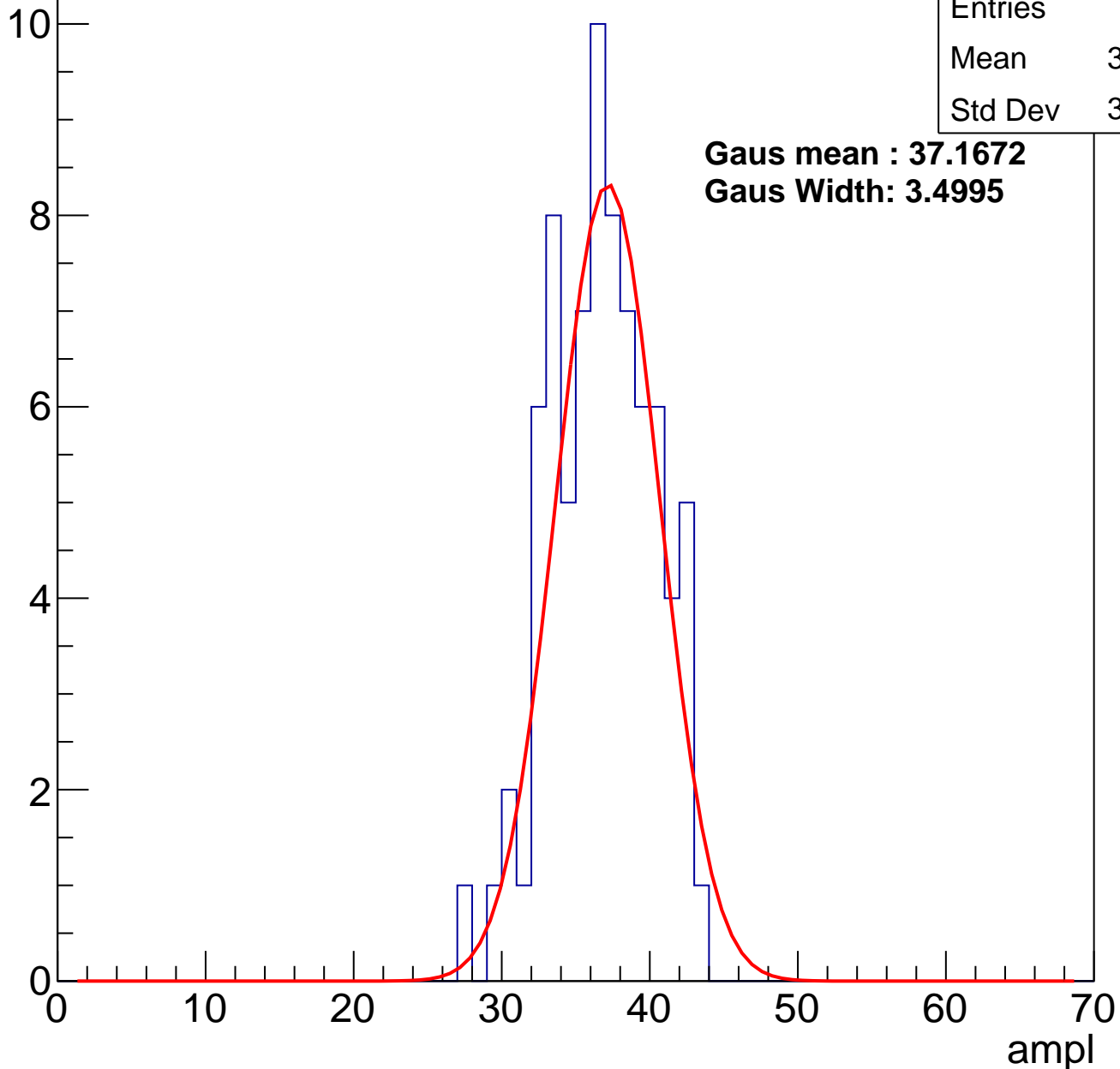
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	78
Mean	36.29
Std Dev	3.453

**Gaus mean : 37.1672**

**Gaus Width: 3.4995**

Entry



# B1L101S, U8-ch53, adc2

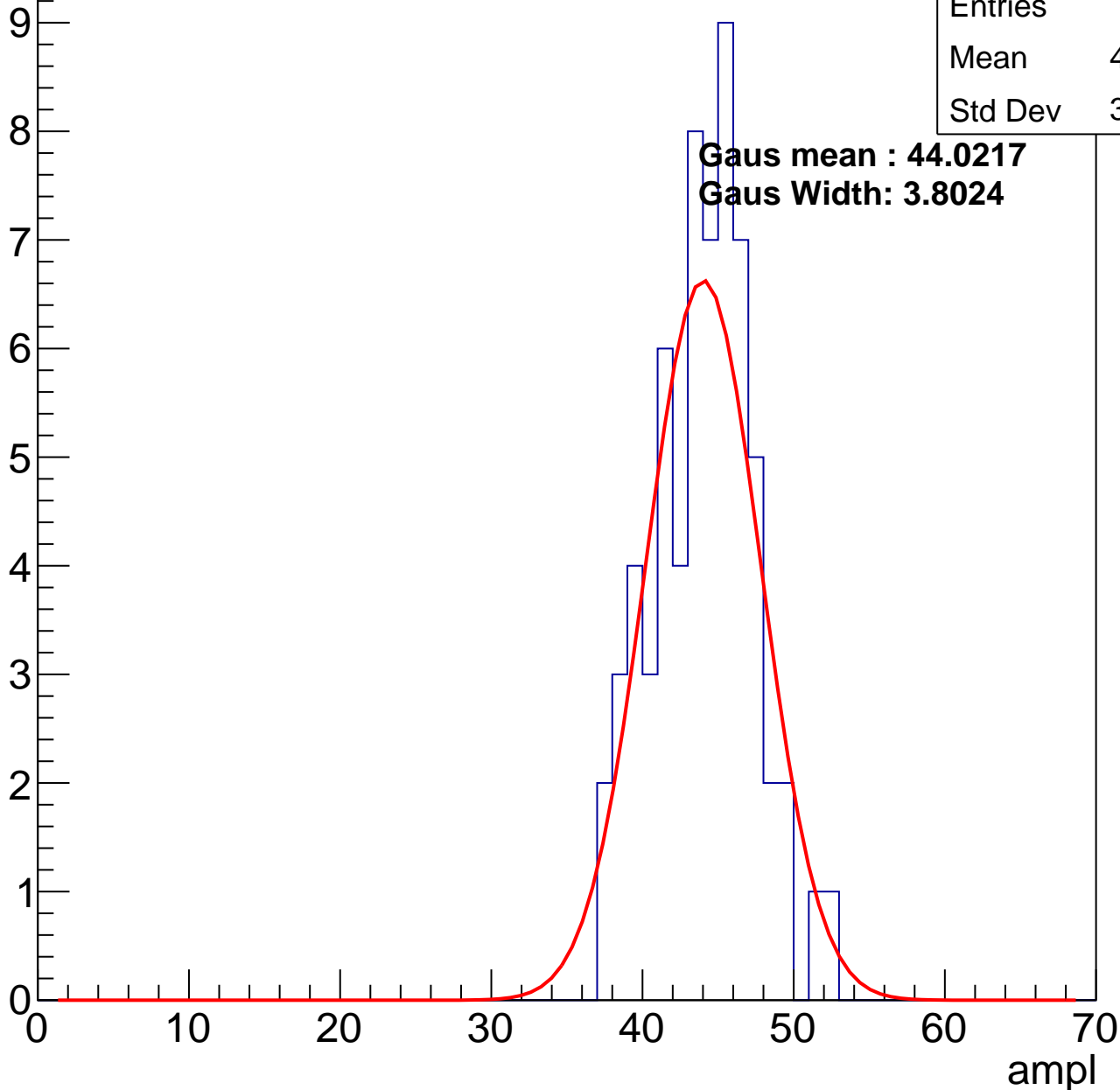
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	43.58
Std Dev	3.302

**Gaus mean : 44.0217**

**Gaus Width: 3.8024**

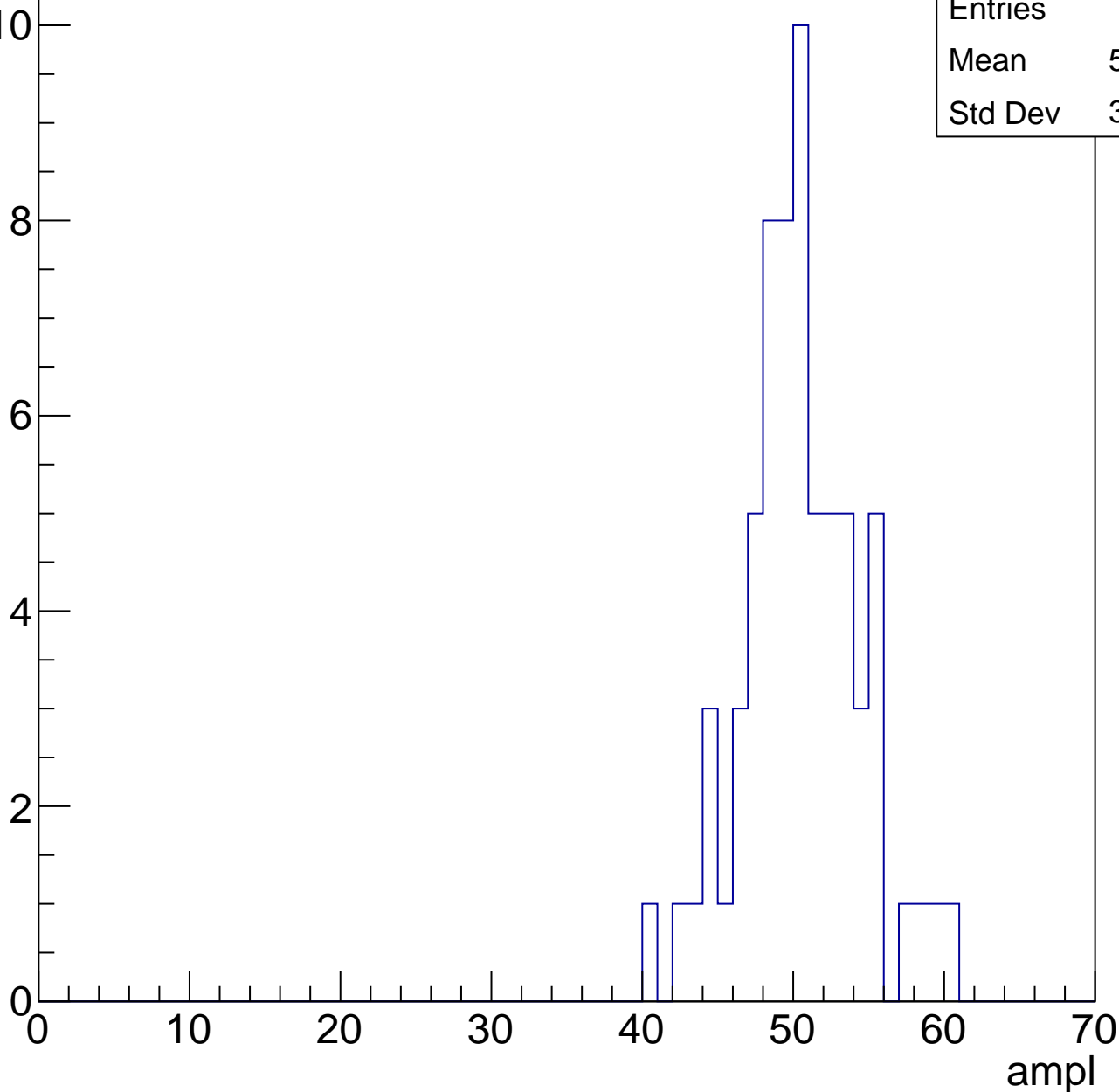


# B1L101S, U8-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	50.03
Std Dev	3.865

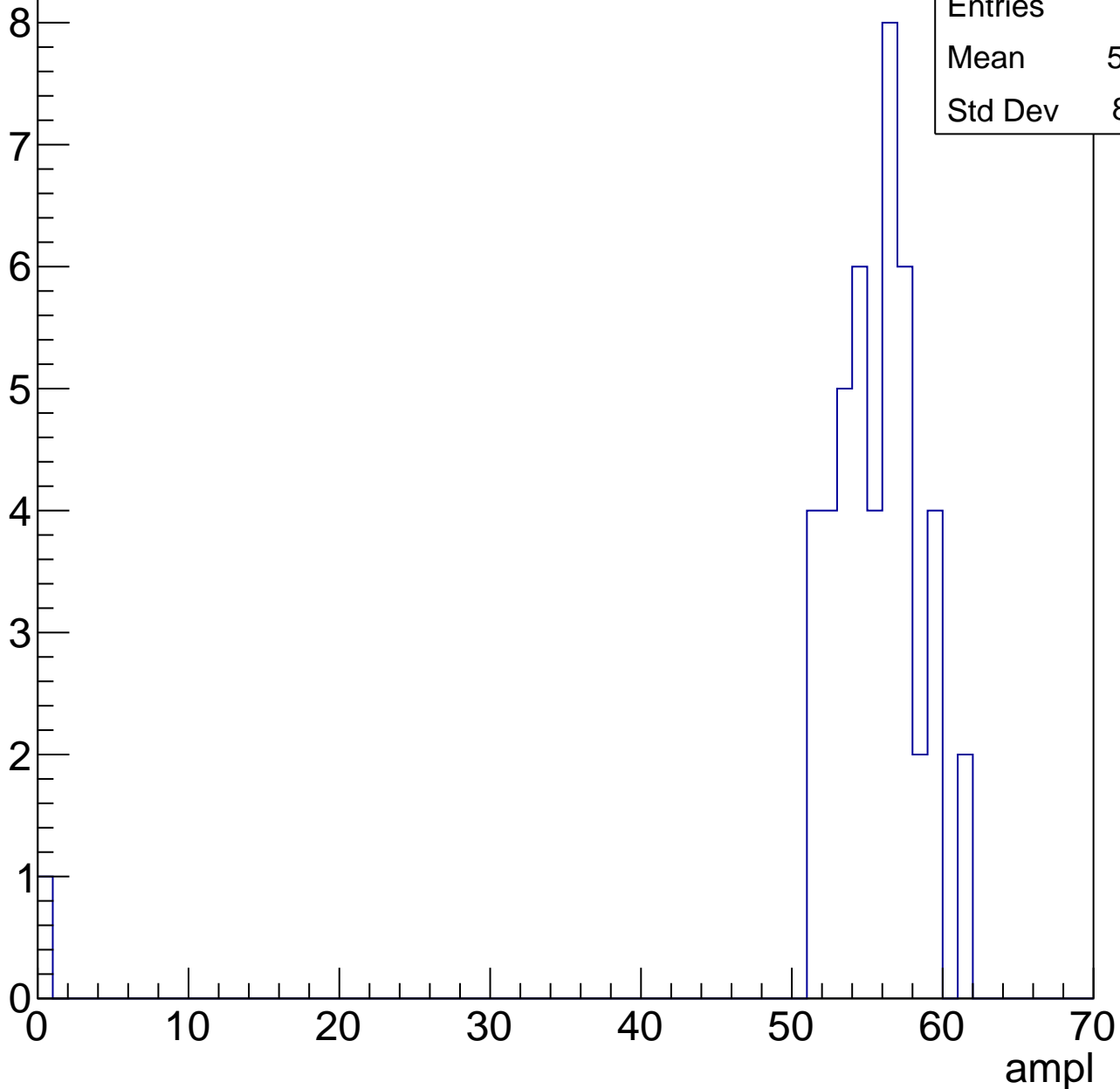


# B1L101S, U8-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	54.02
Std Dev	8.461



# B1L101S, U8-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	60.02
Std Dev	2.29

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

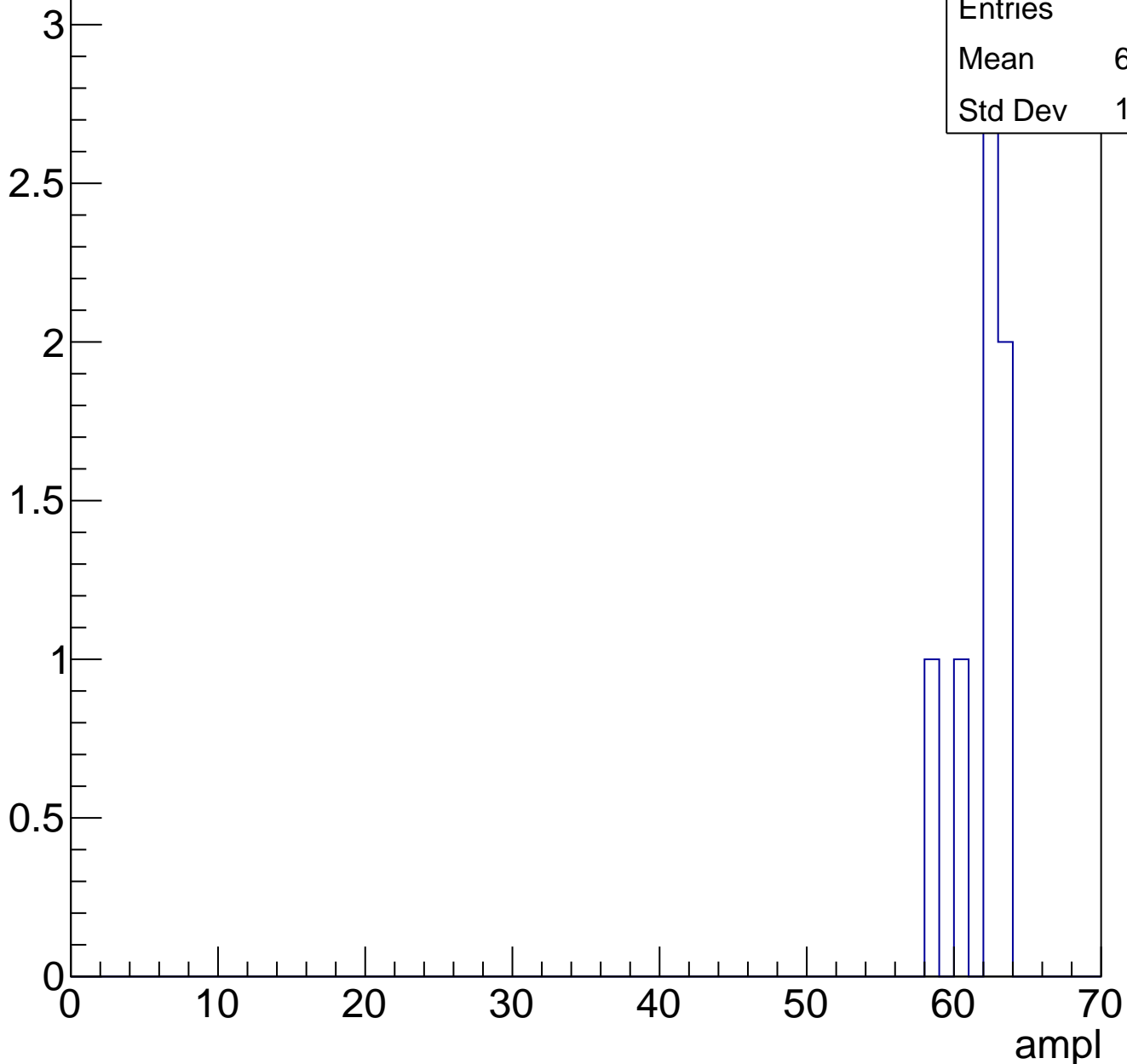
7

8

# B1L101S, U8-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	7
Mean	61.43
Std Dev	1.678



# B1L101S, U8-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch54, adc0

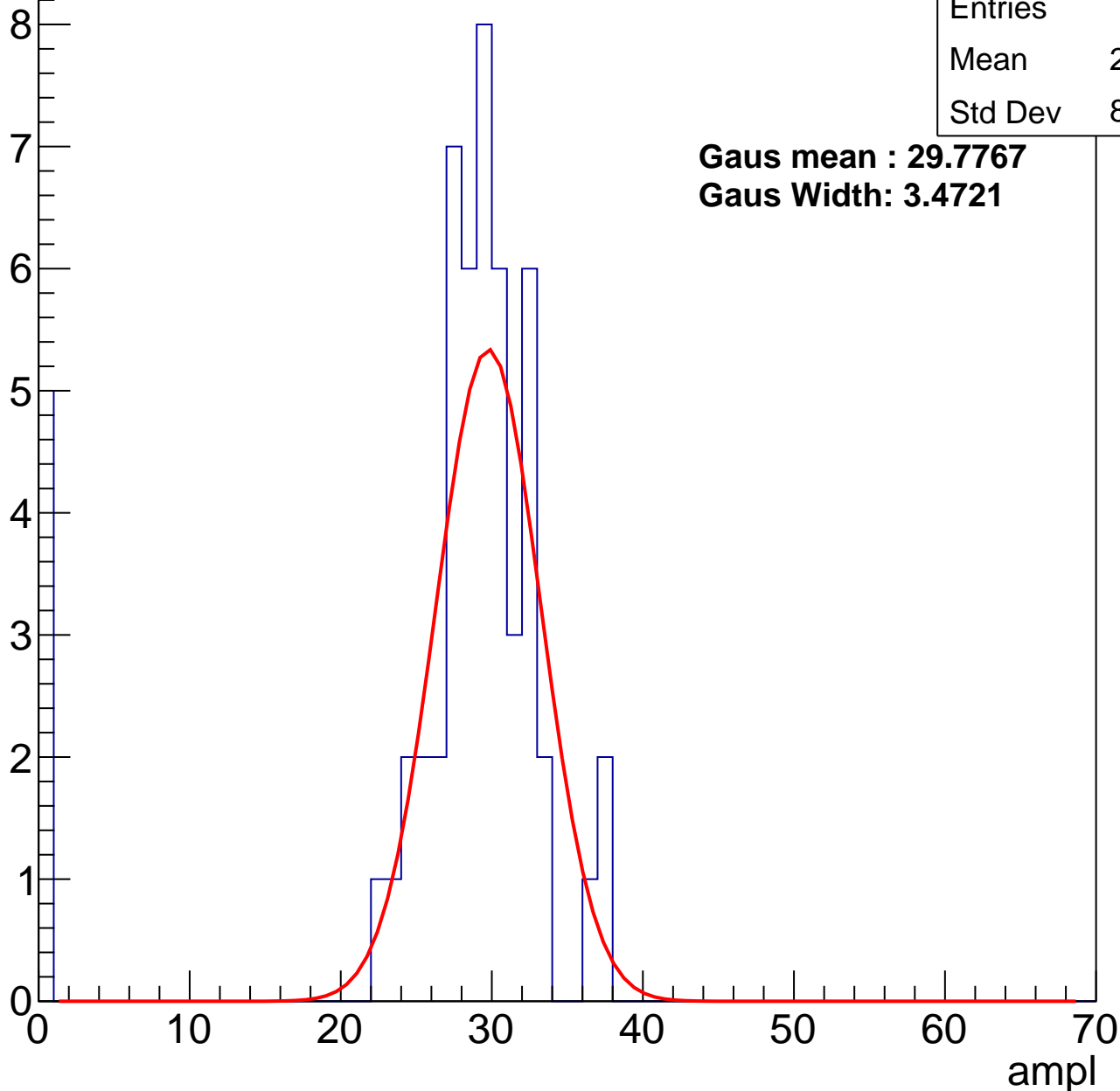
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	26.39
Std Dev	8.962

**Gaus mean : 29.7767**

**Gaus Width: 3.4721**



# B1L101S, U8-ch54, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	82
Mean	35.7
Std Dev	3.449

**Gaus mean : 36.1941**

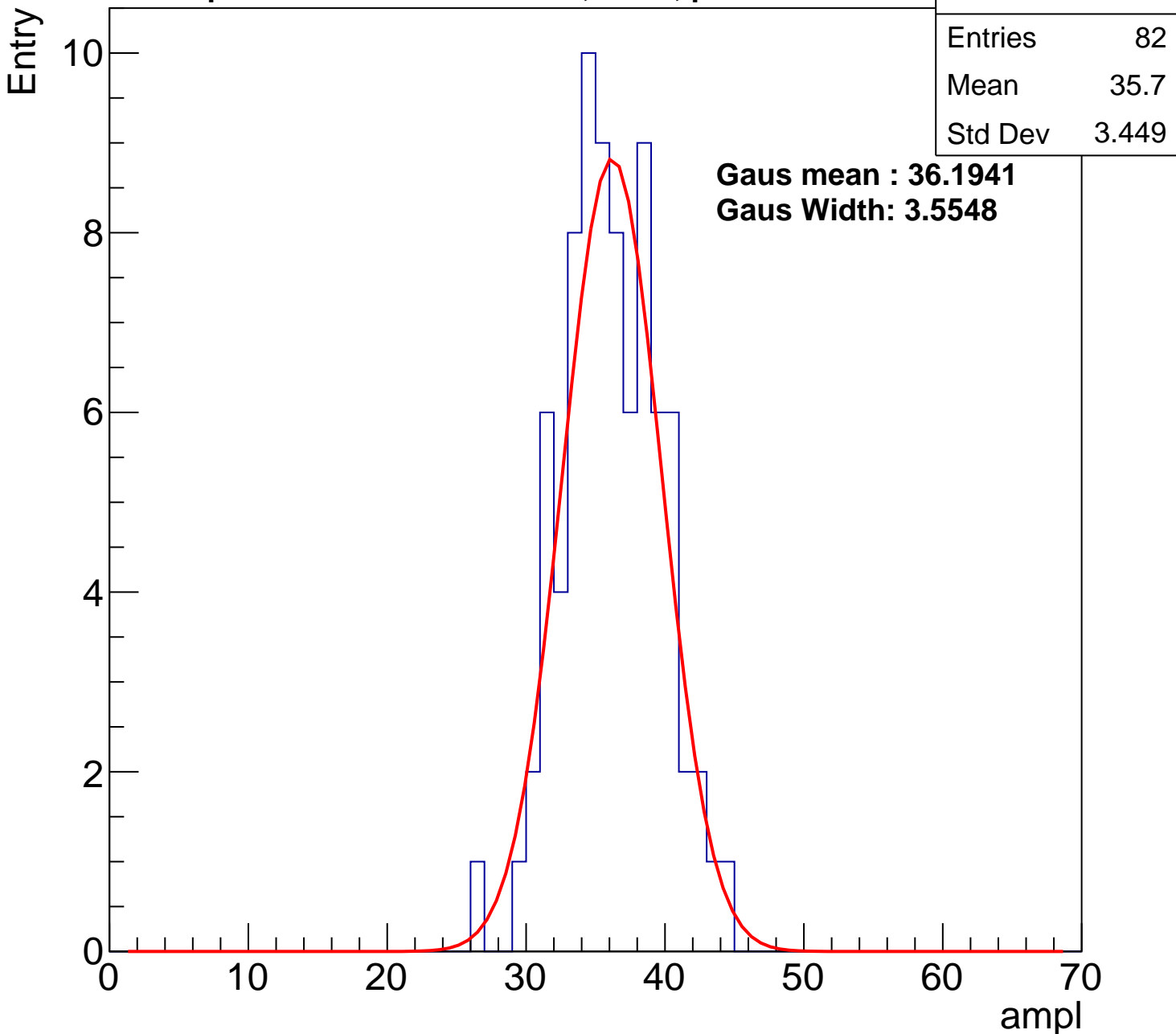
**Gaus Width: 3.5548**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U8-ch54, adc2

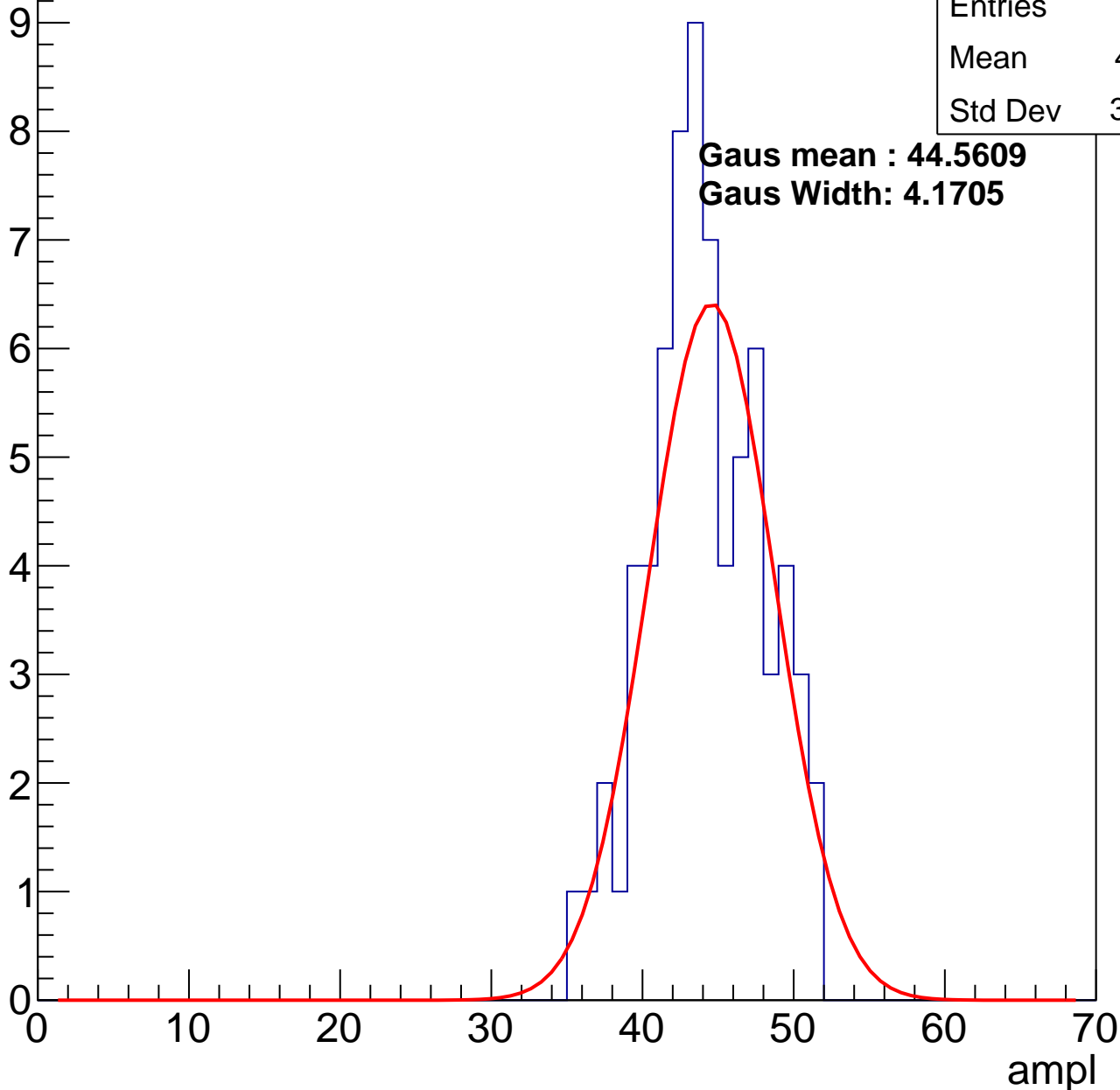
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	43.71
Std Dev	3.712

**Gaus mean : 44.5609**

**Gaus Width: 4.1705**

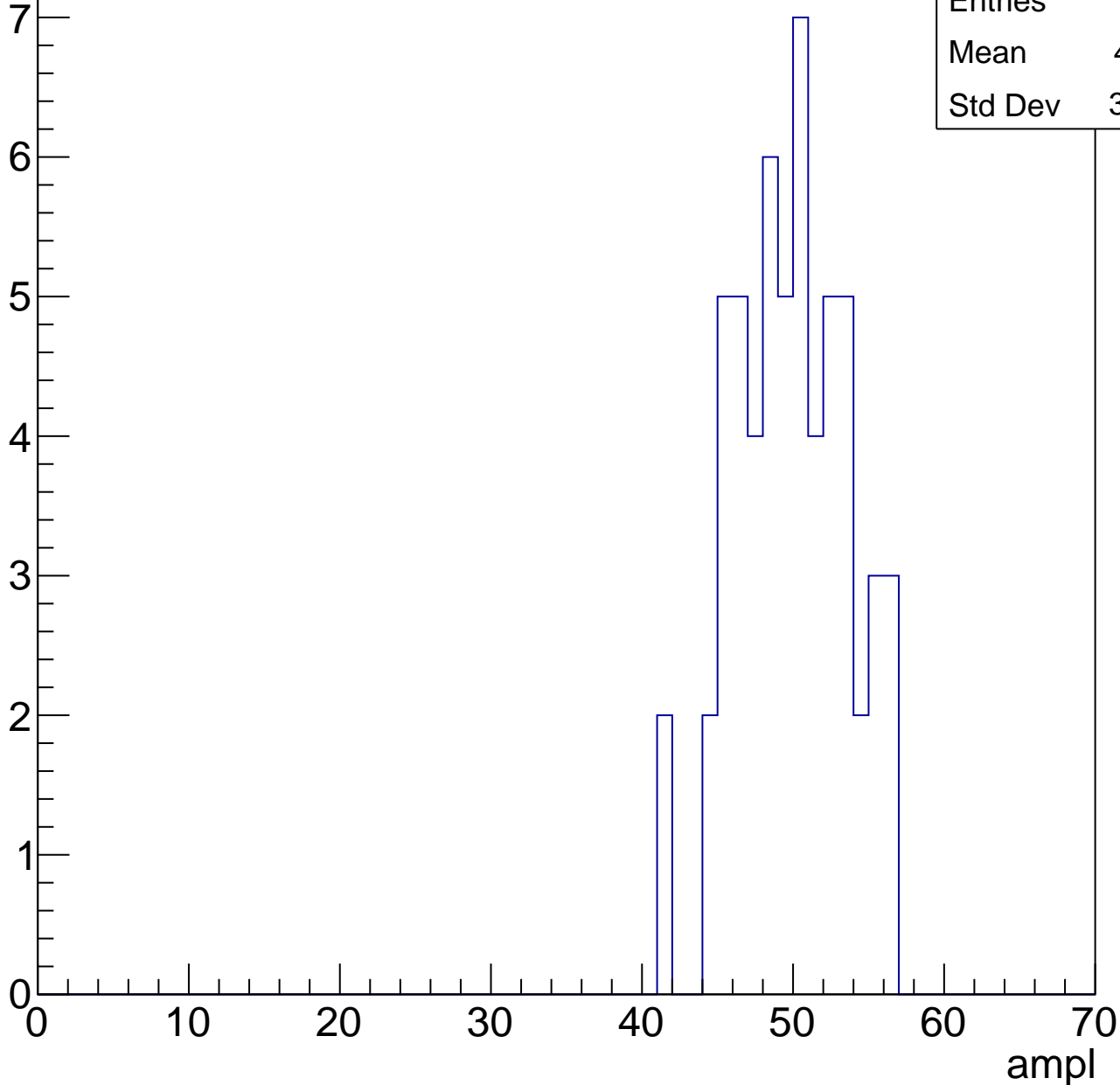


# B1L101S, U8-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	49.41
Std Dev	3.639

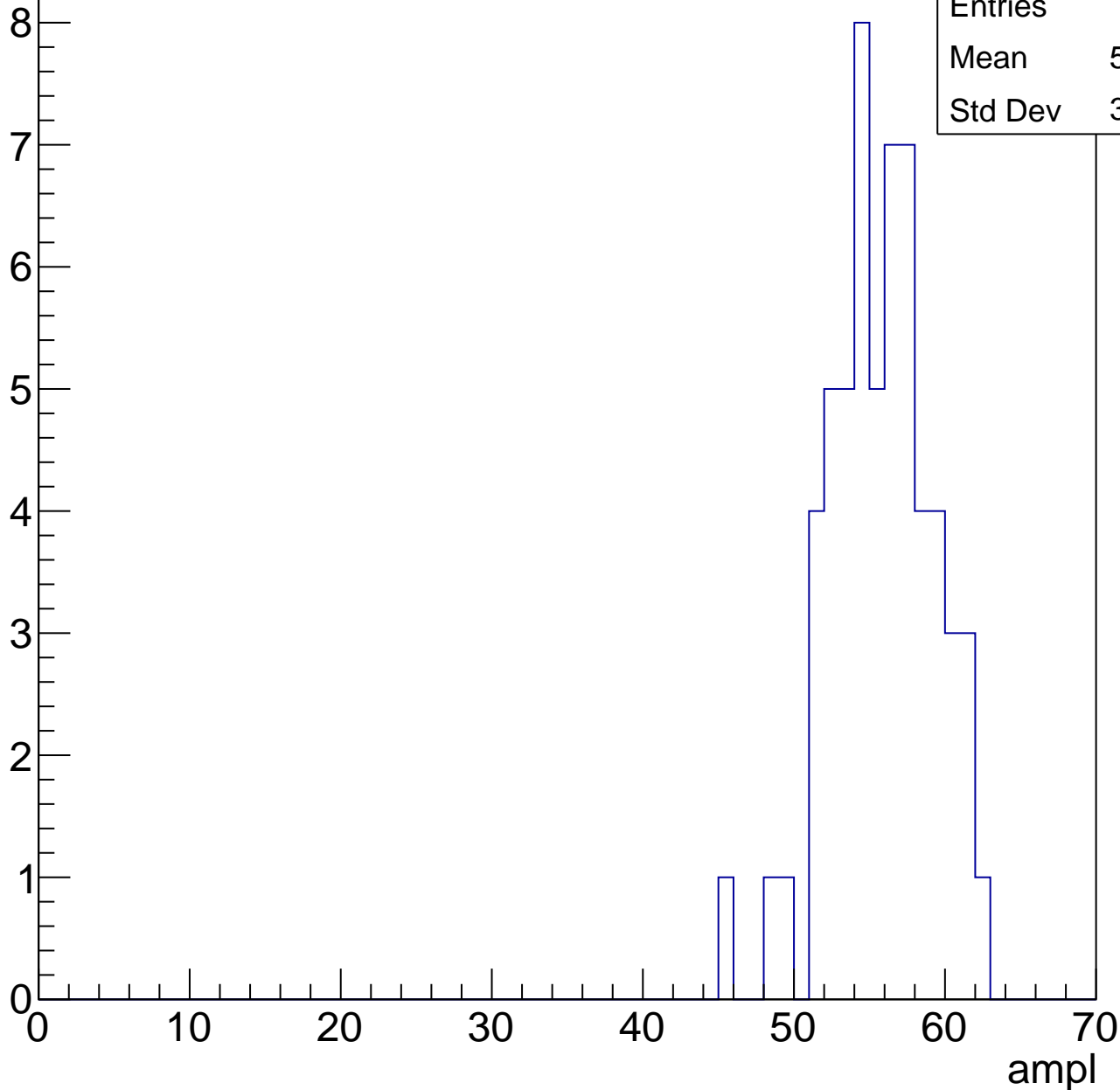


# B1L101S, U8-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	55.29
Std Dev	3.405

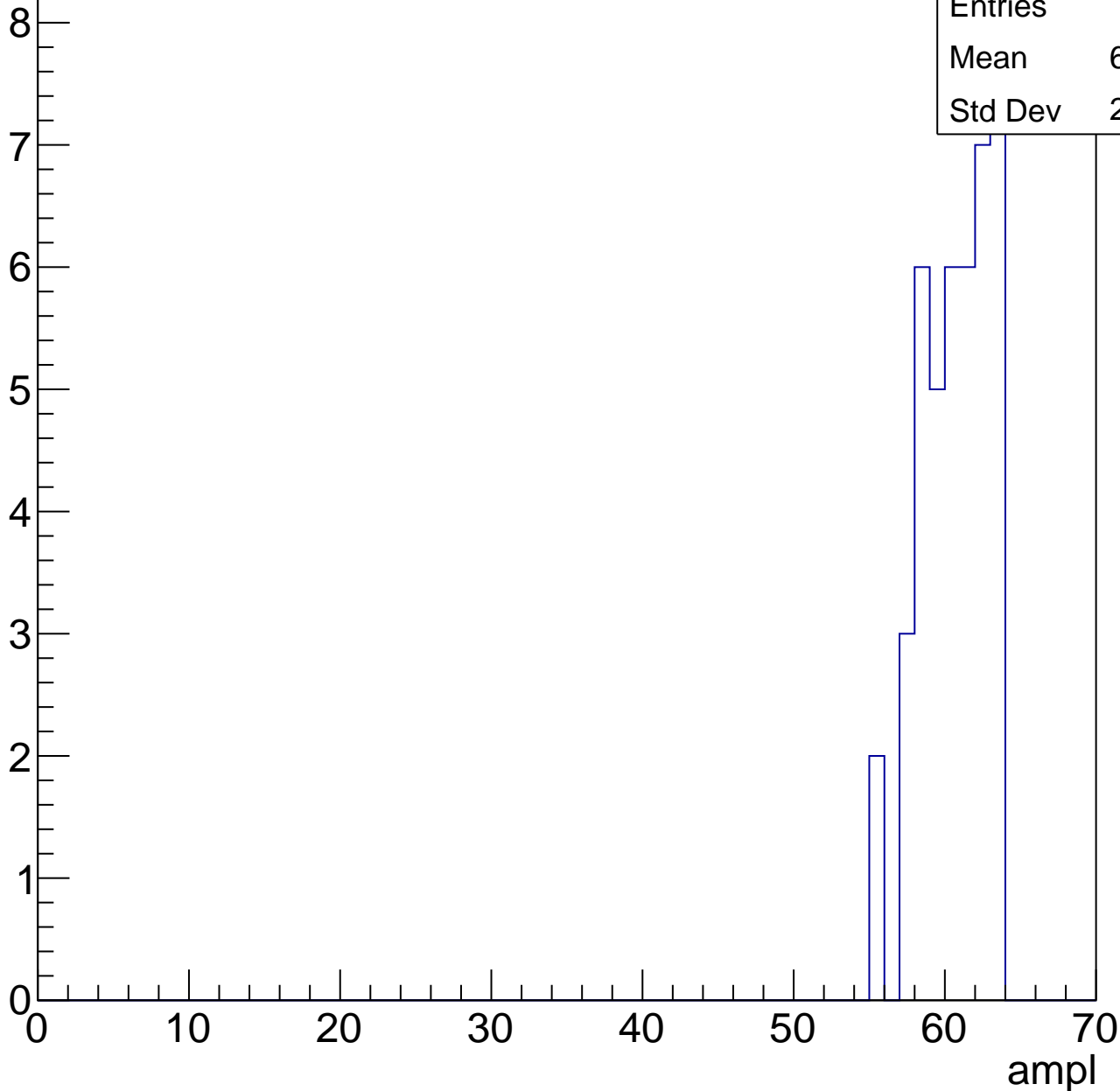


# B1L101S, U8-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	60.19
Std Dev	2.213



# B1L101S, U8-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

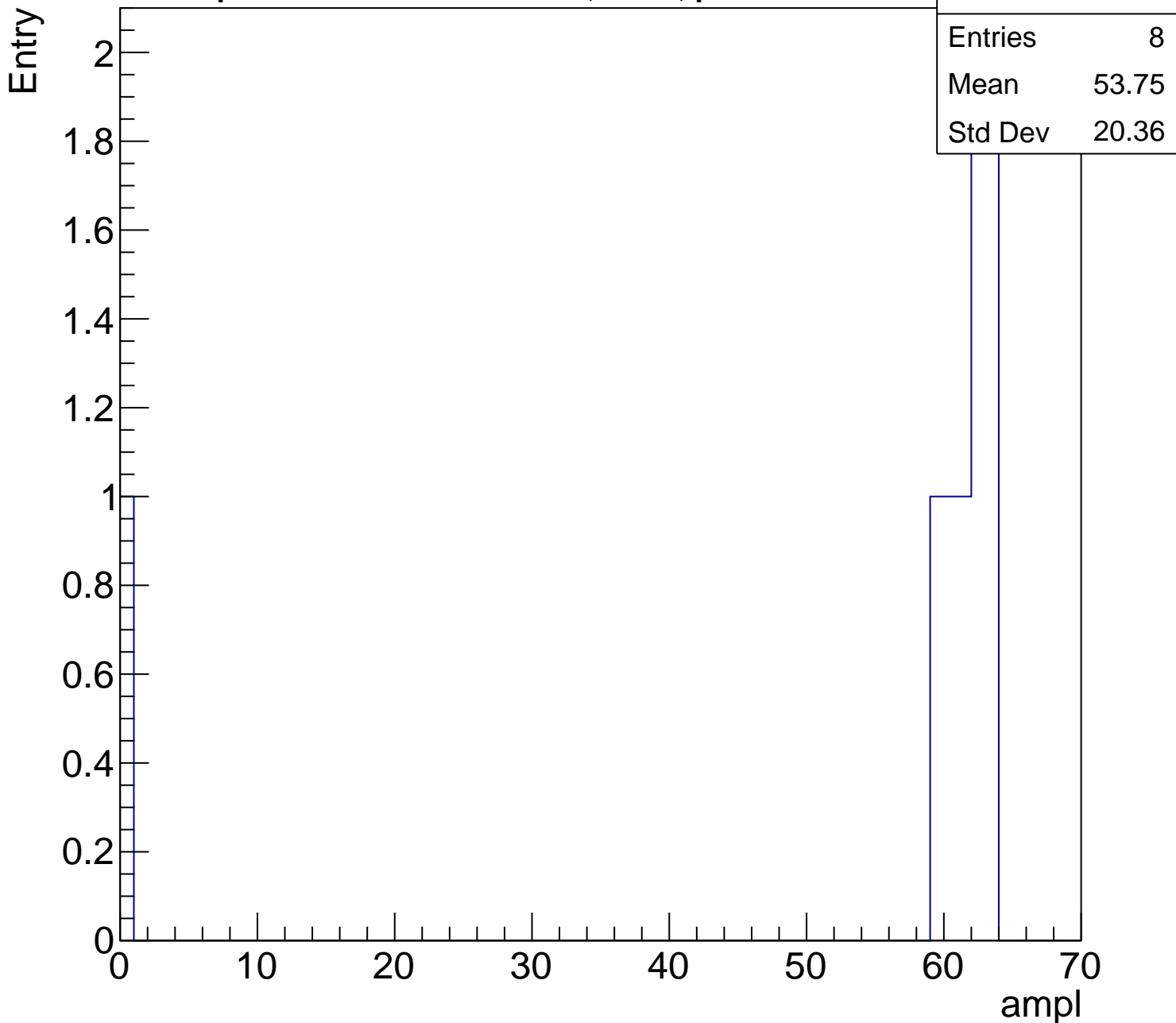
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	8
Mean	53.75
Std Dev	20.36

0 10 20 30 40 50 60 70

ampl





# B1L101S, U8-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U8-ch55, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	67
Mean	31.18
Std Dev	3.363

**Gaus mean : 31.3644**

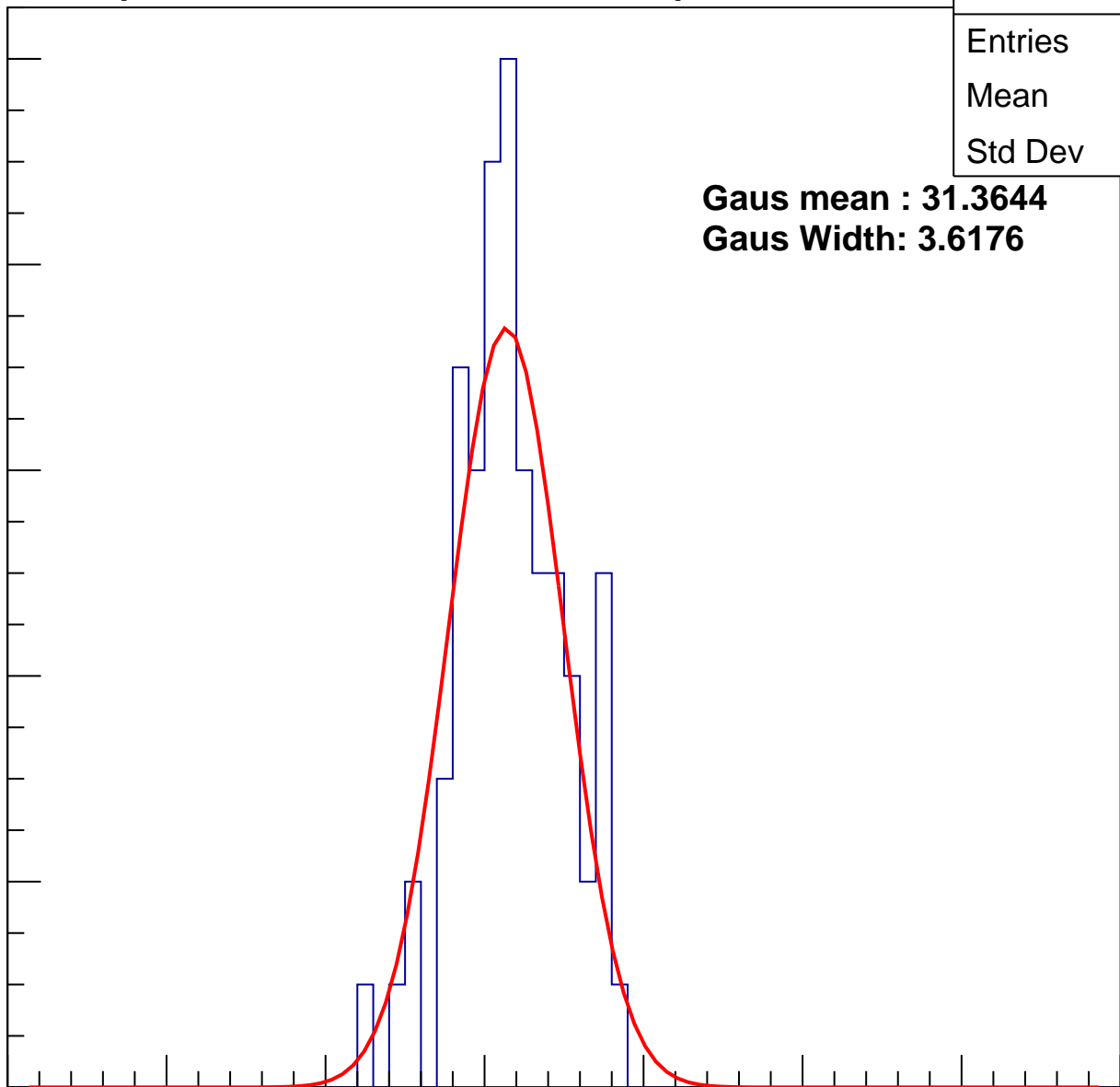
**Gaus Width: 3.6176**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U8-ch55, adc1

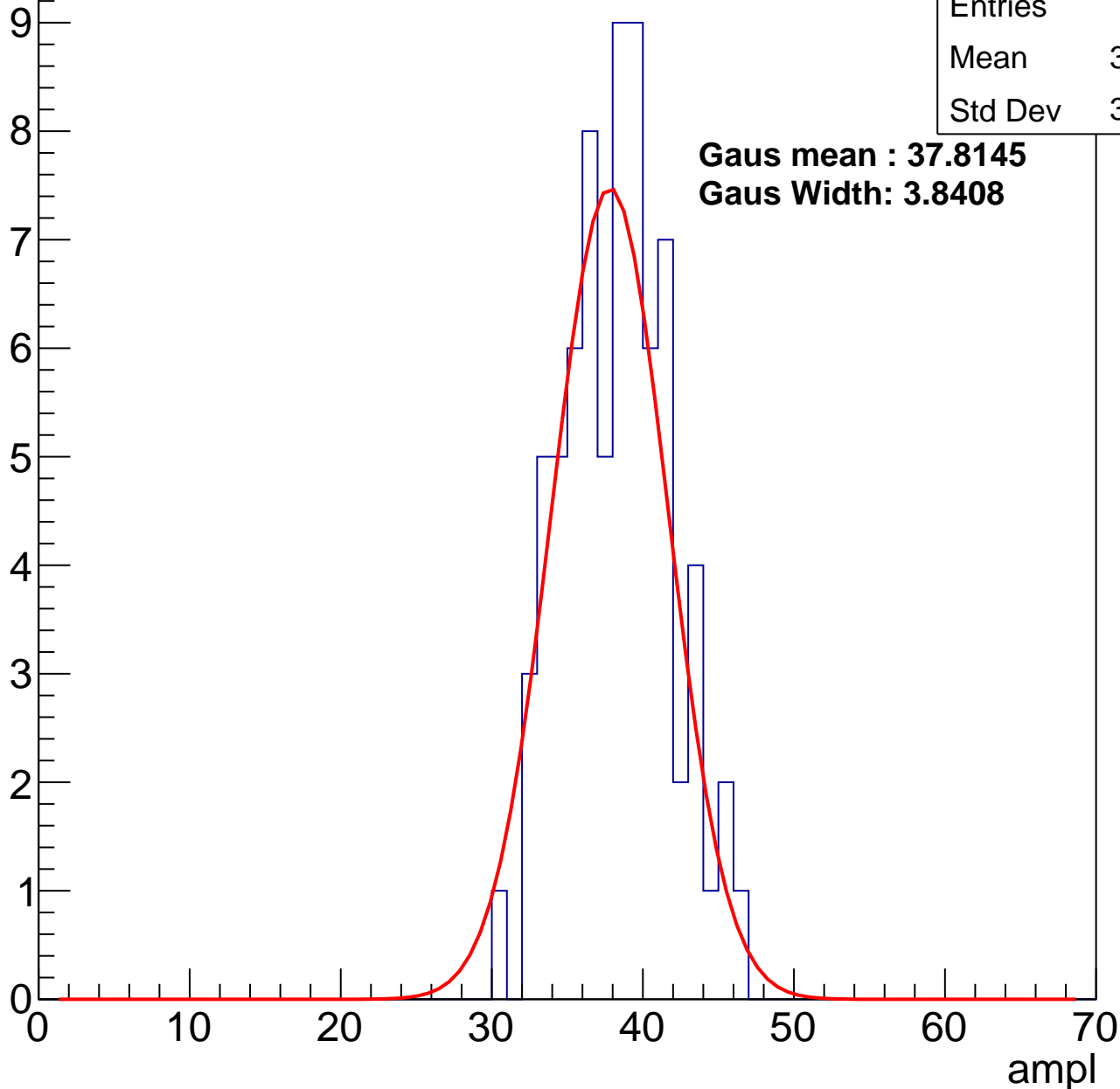
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	37.84
Std Dev	3.472

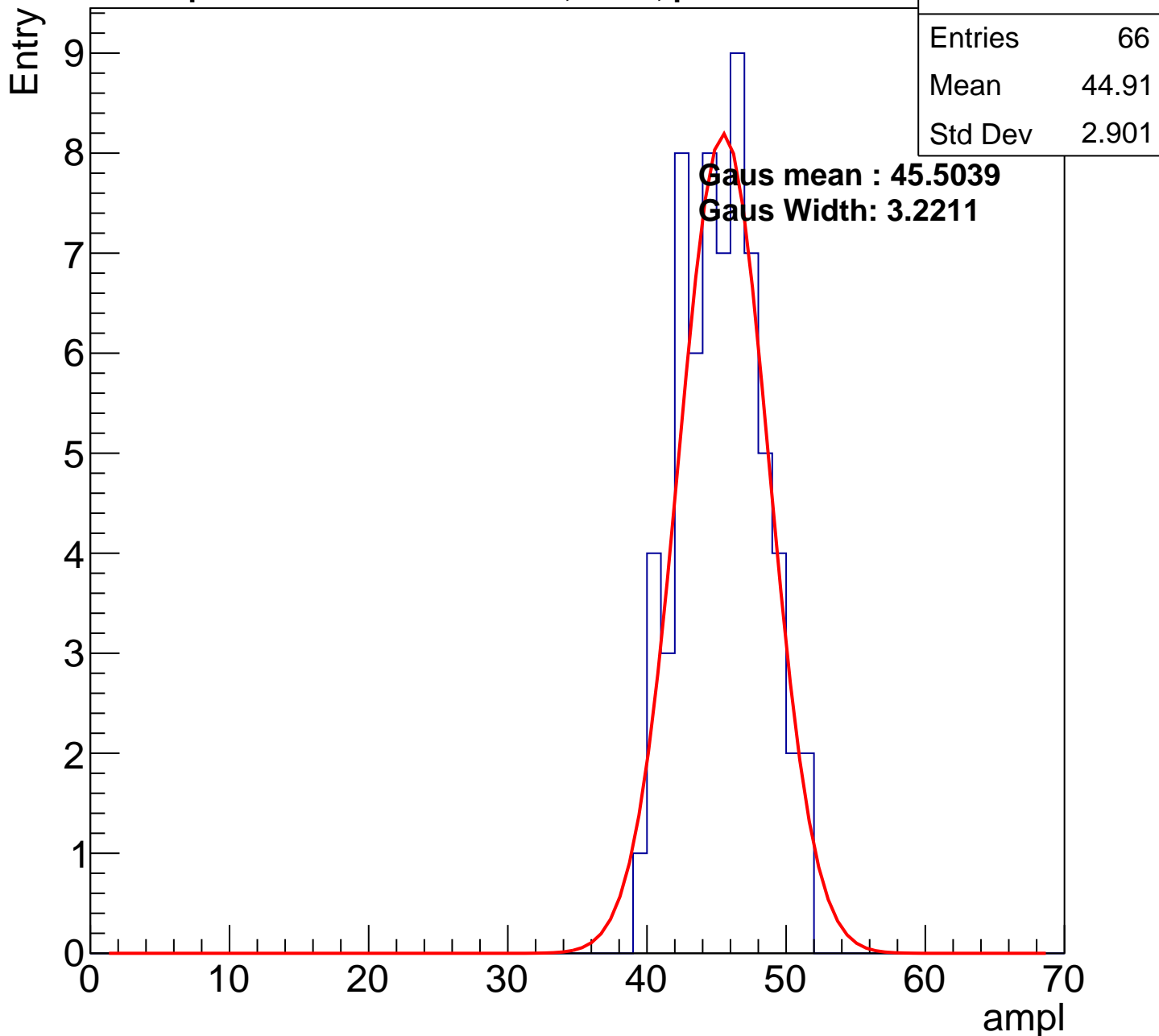
**Gaus mean : 37.8145**

**Gaus Width: 3.8408**



# B1L101S, U8-ch55, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

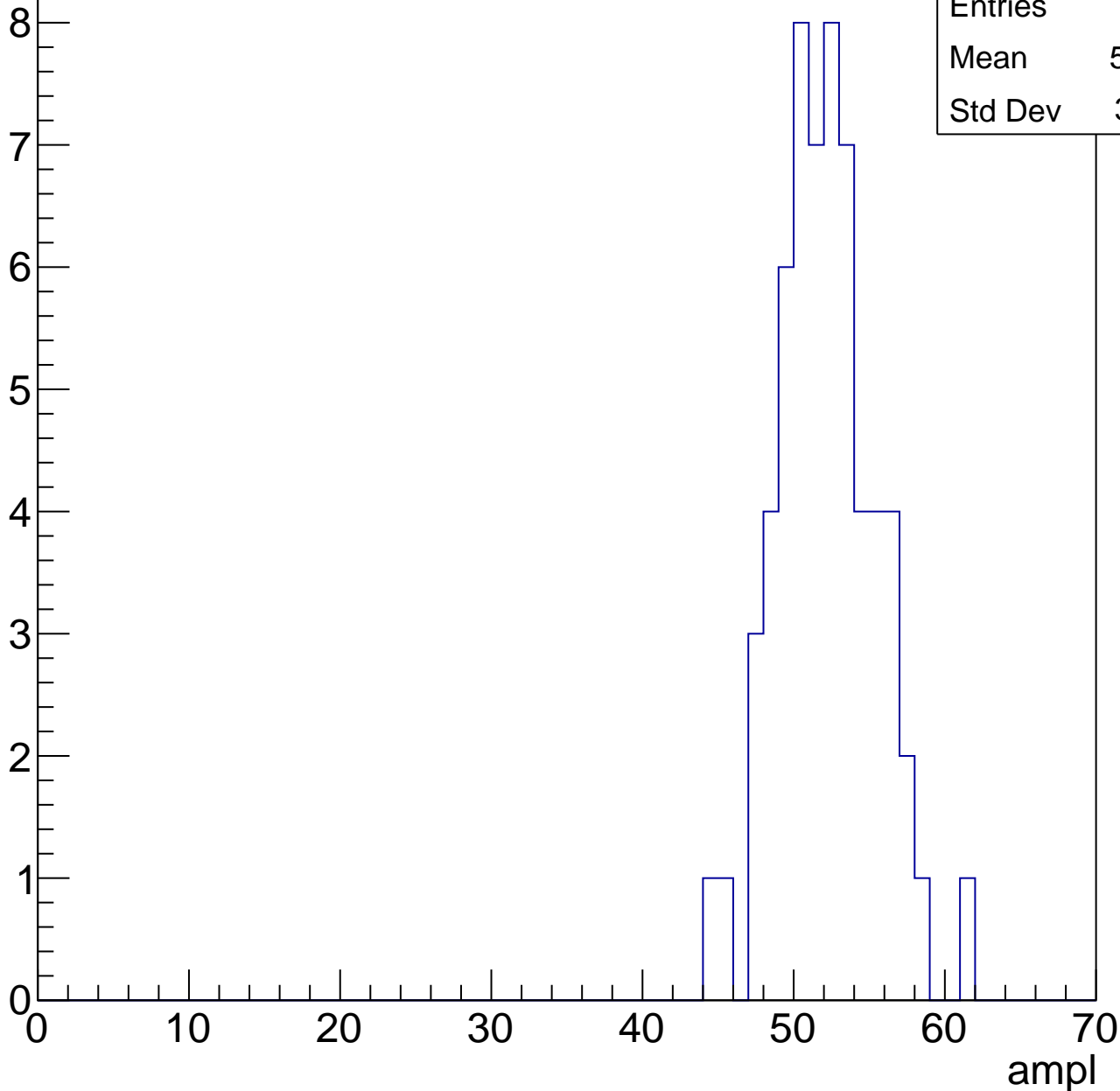


# B1L101S, U8-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

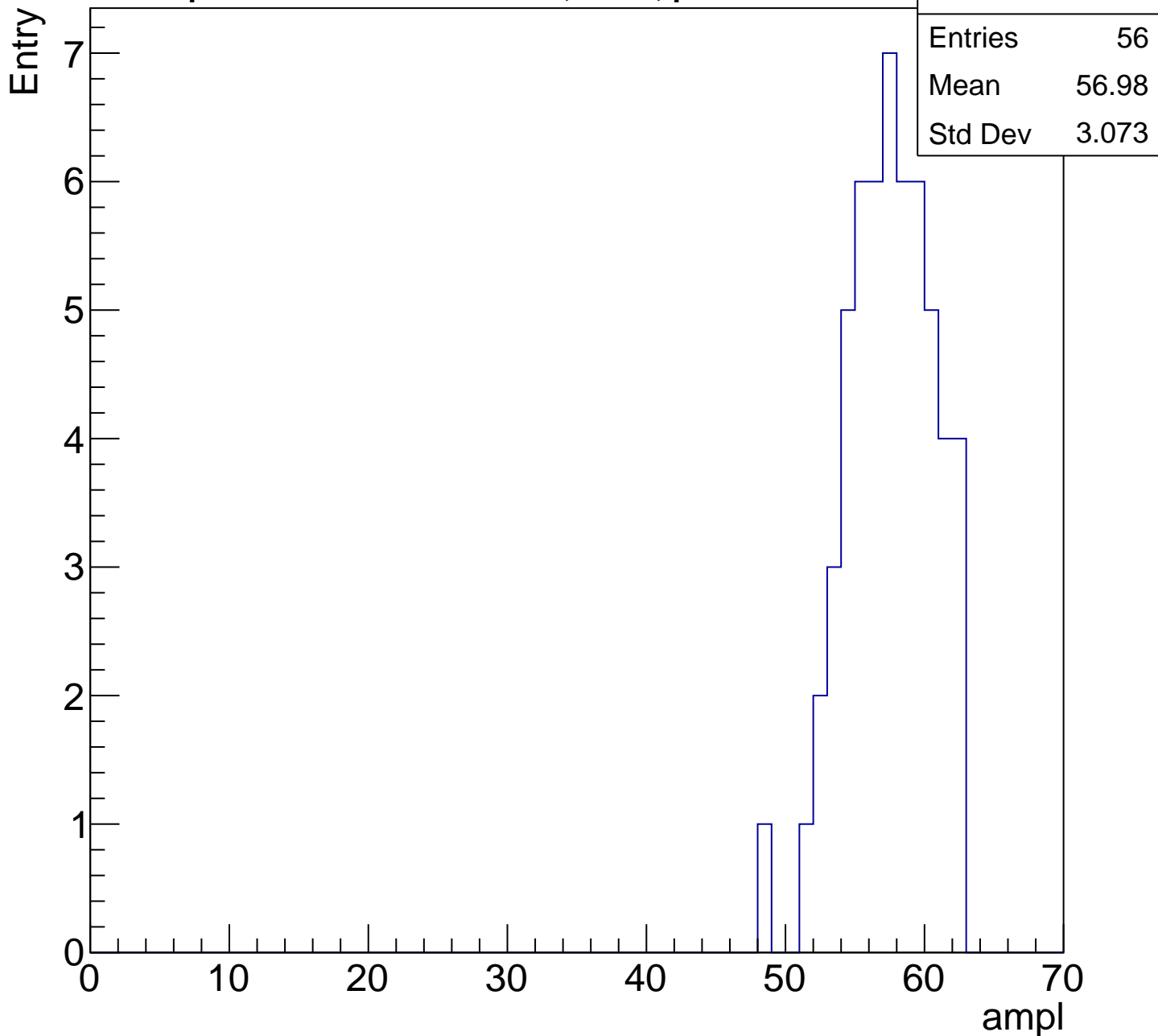
Entry

Entries	61
Mean	51.69
Std Dev	3.211



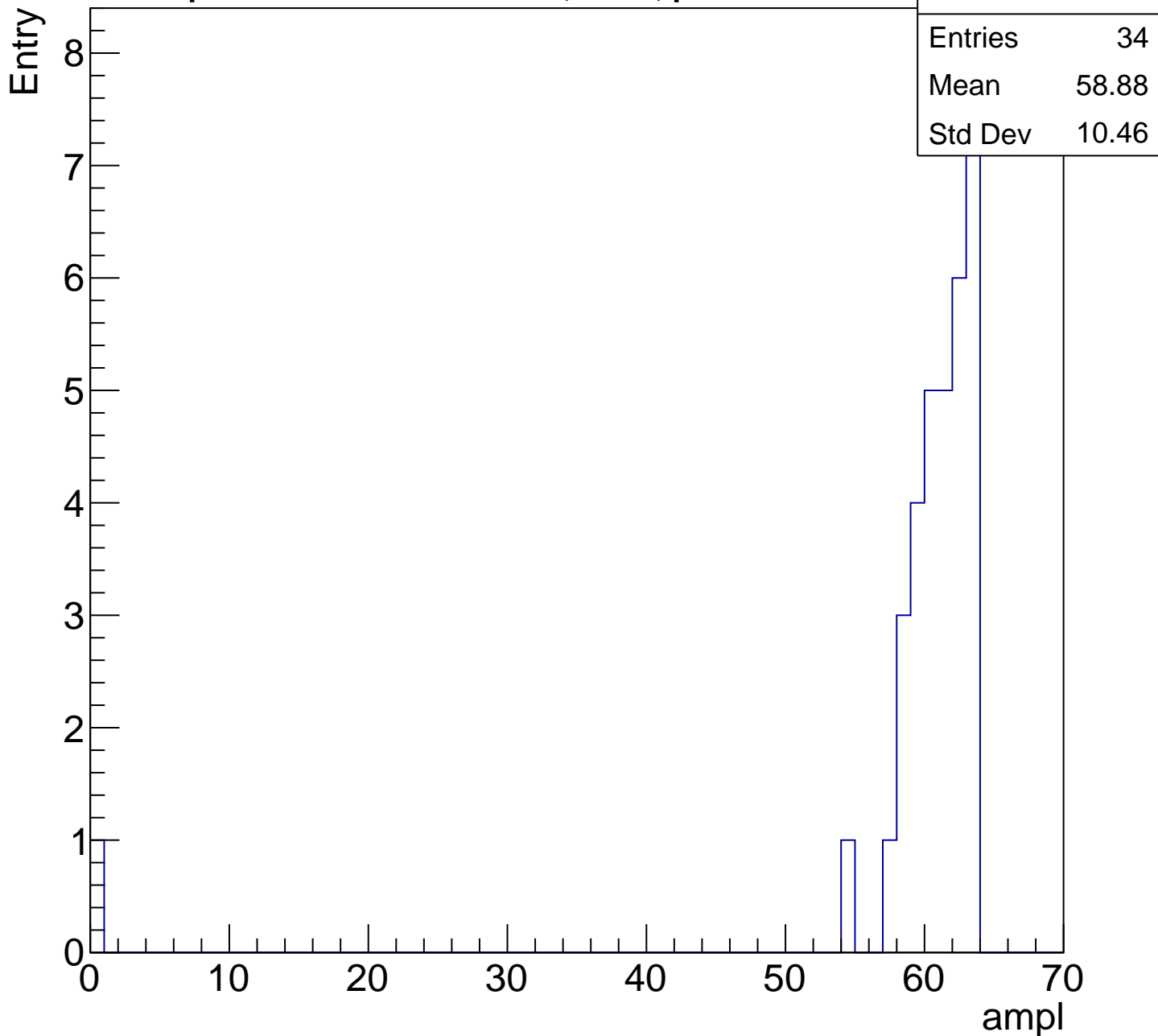
# B1L101S, U8-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U8-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U8-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch56, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	76
Mean	29.32
Std Dev	3.488

**Gaus mean : 29.7227**

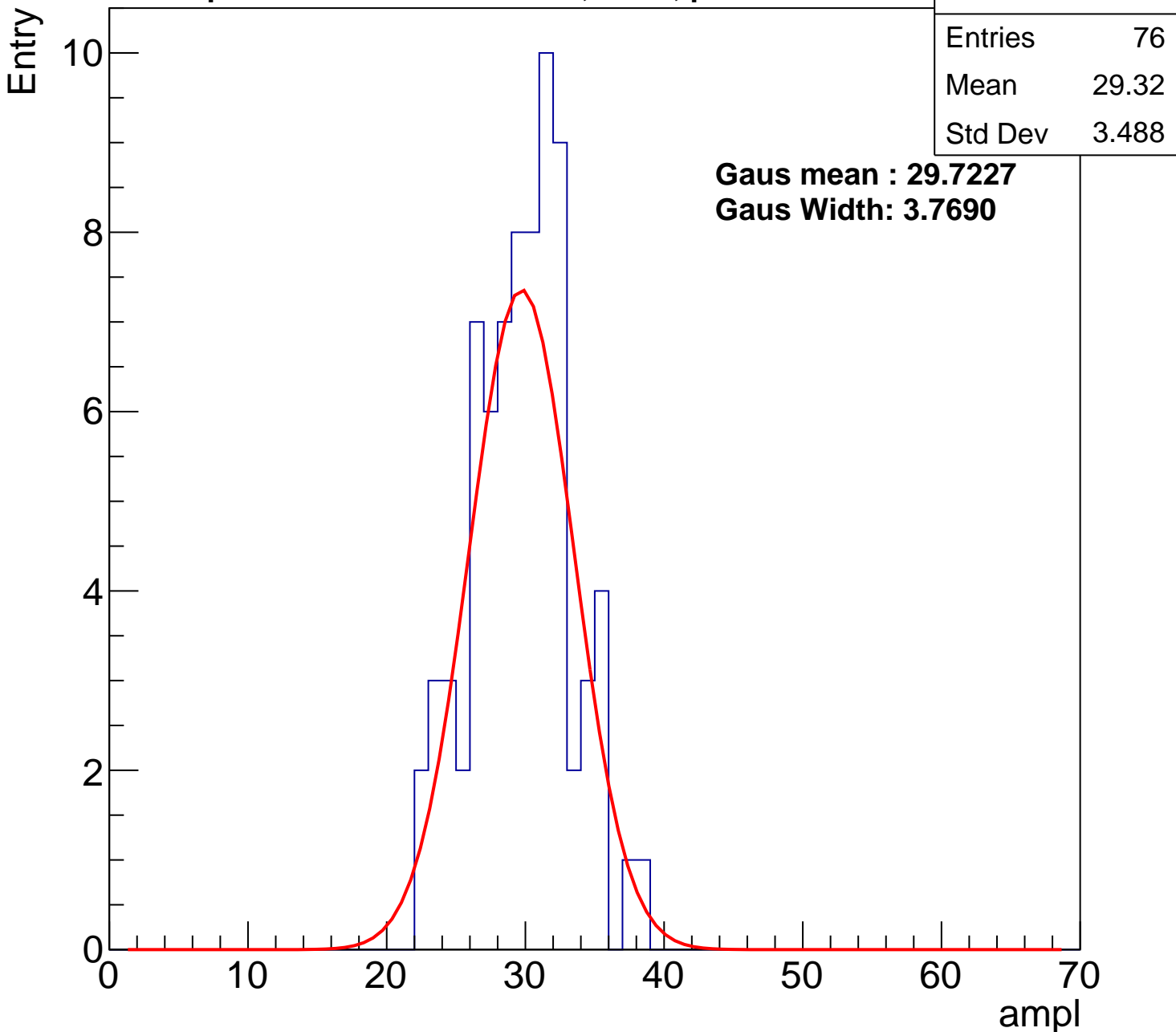
**Gaus Width: 3.7690**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U8-ch56, adc1

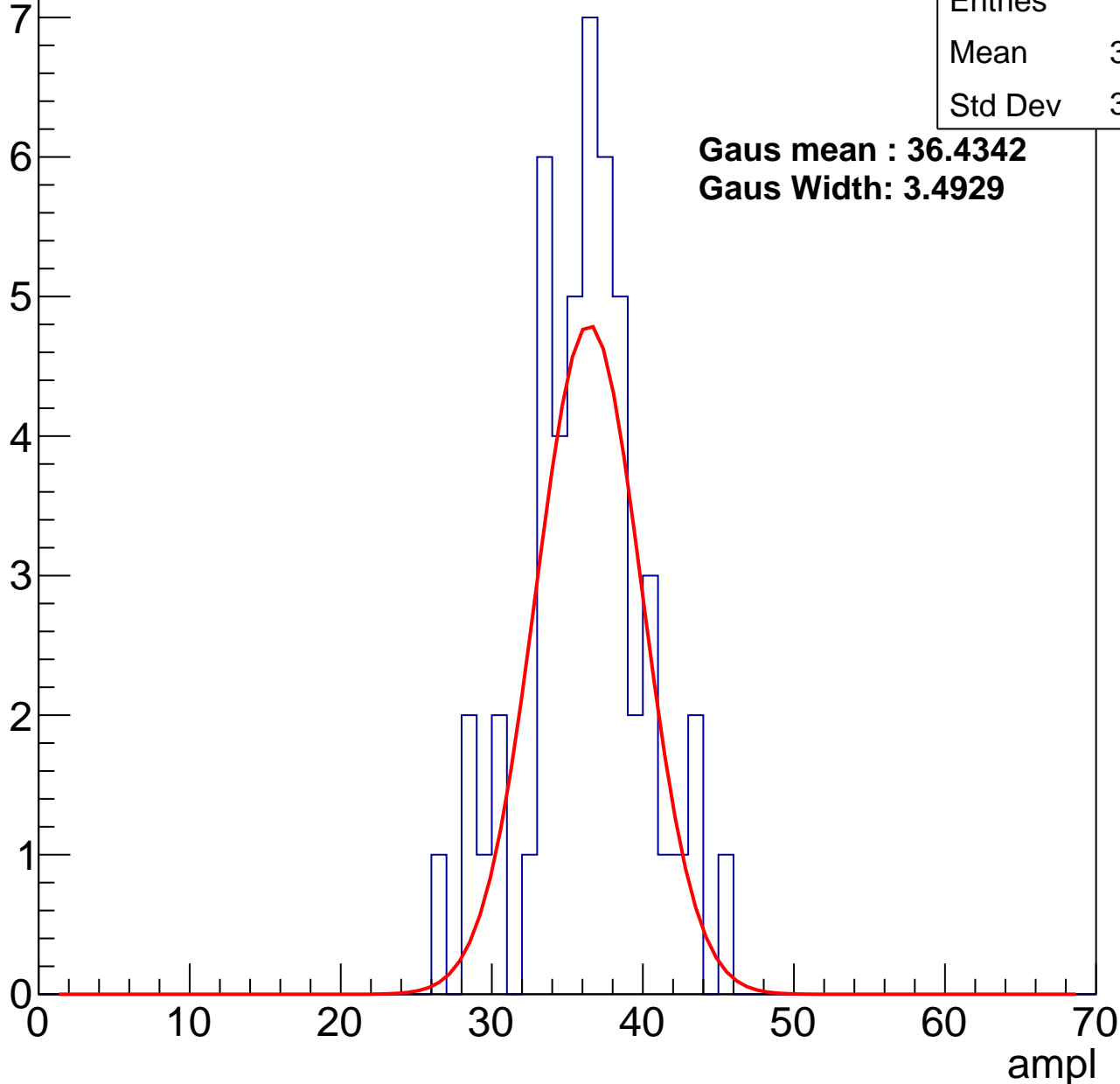
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	35.76
Std Dev	3.922

**Gaus mean : 36.4342**

**Gaus Width: 3.4929**



# B1L101S, U8-ch56, adc2

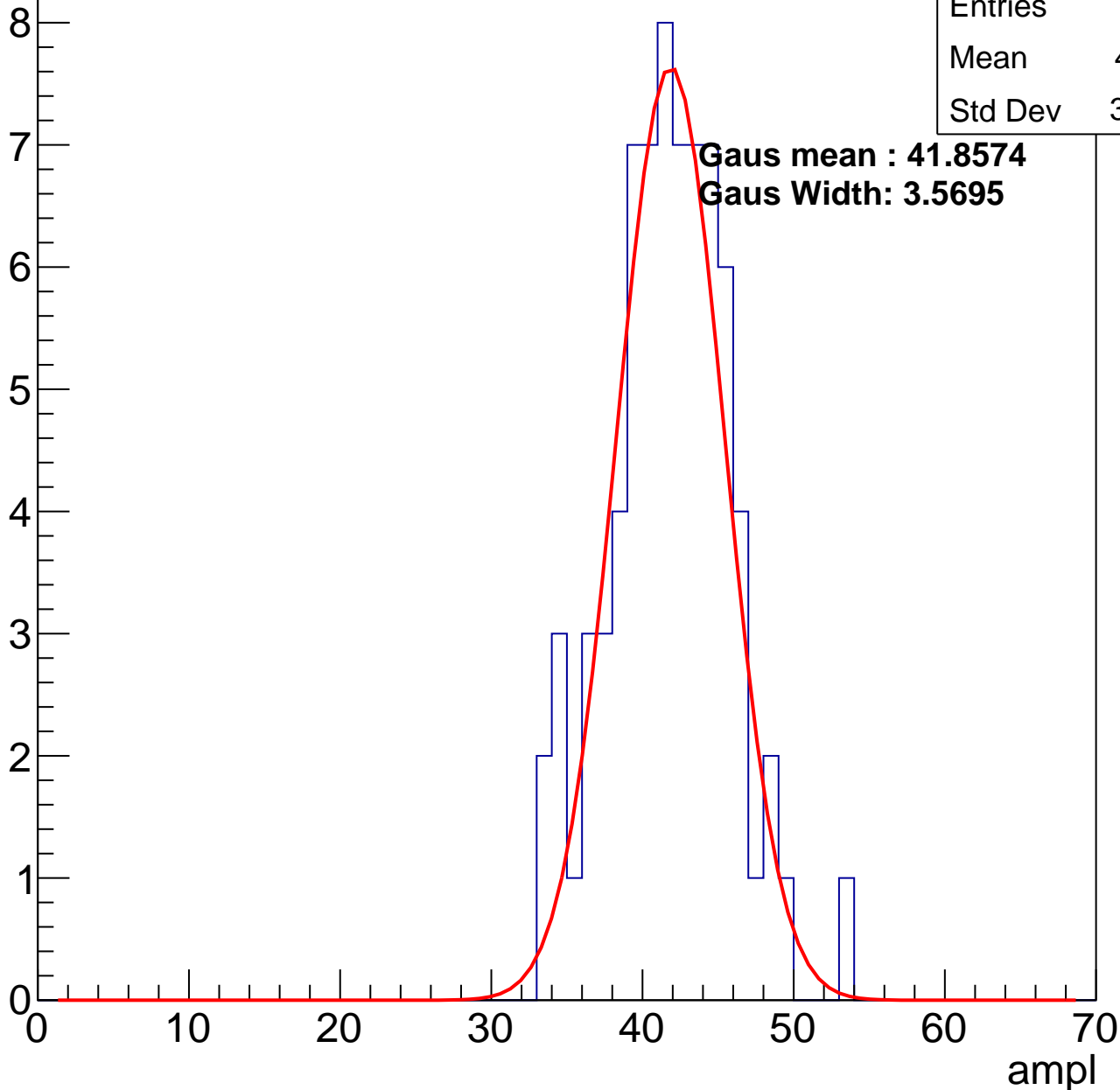
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	41.31
Std Dev	3.914

**Gaus mean : 41.8574**

**Gaus Width: 3.5695**

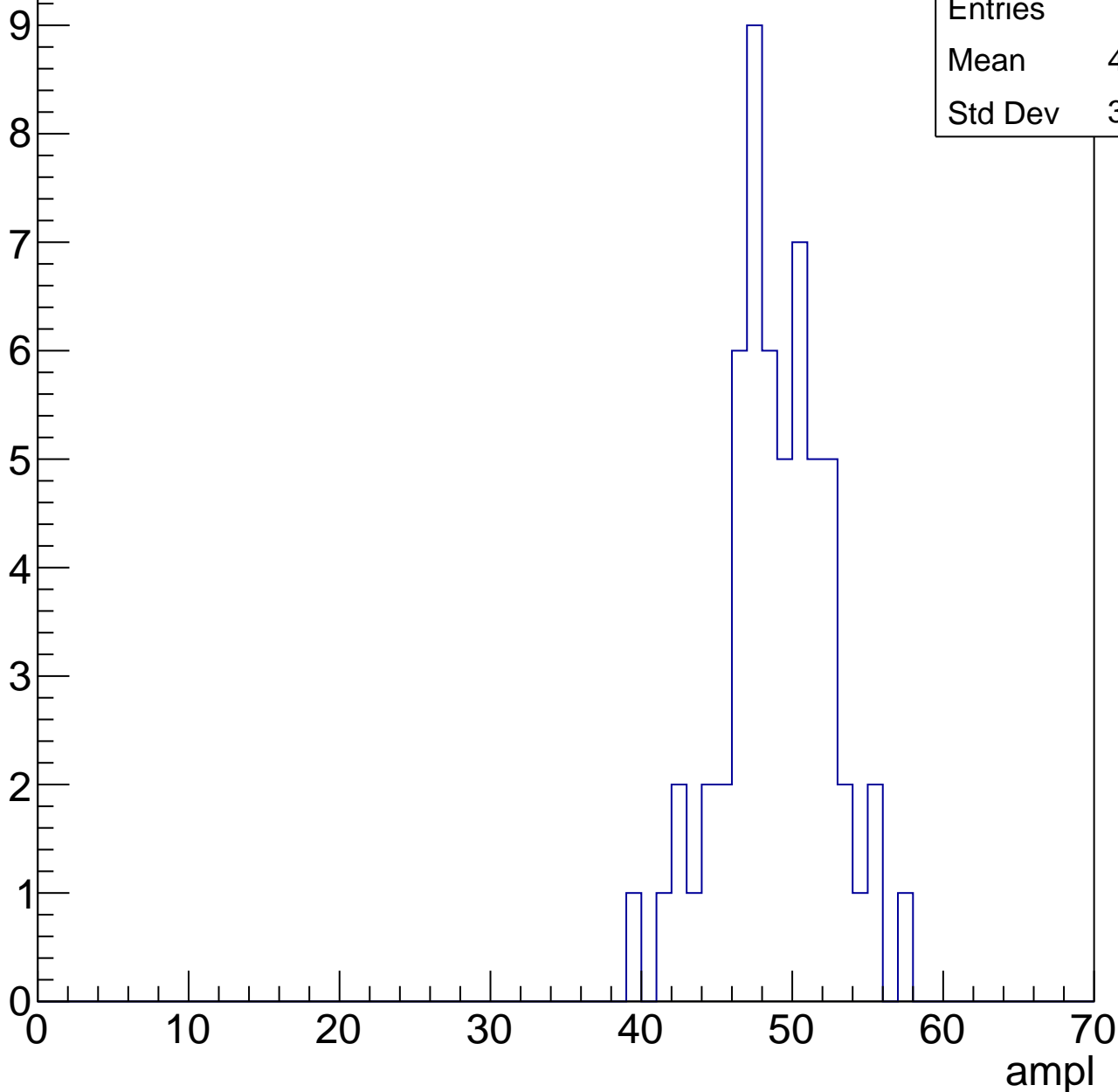


# B1L101S, U8-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

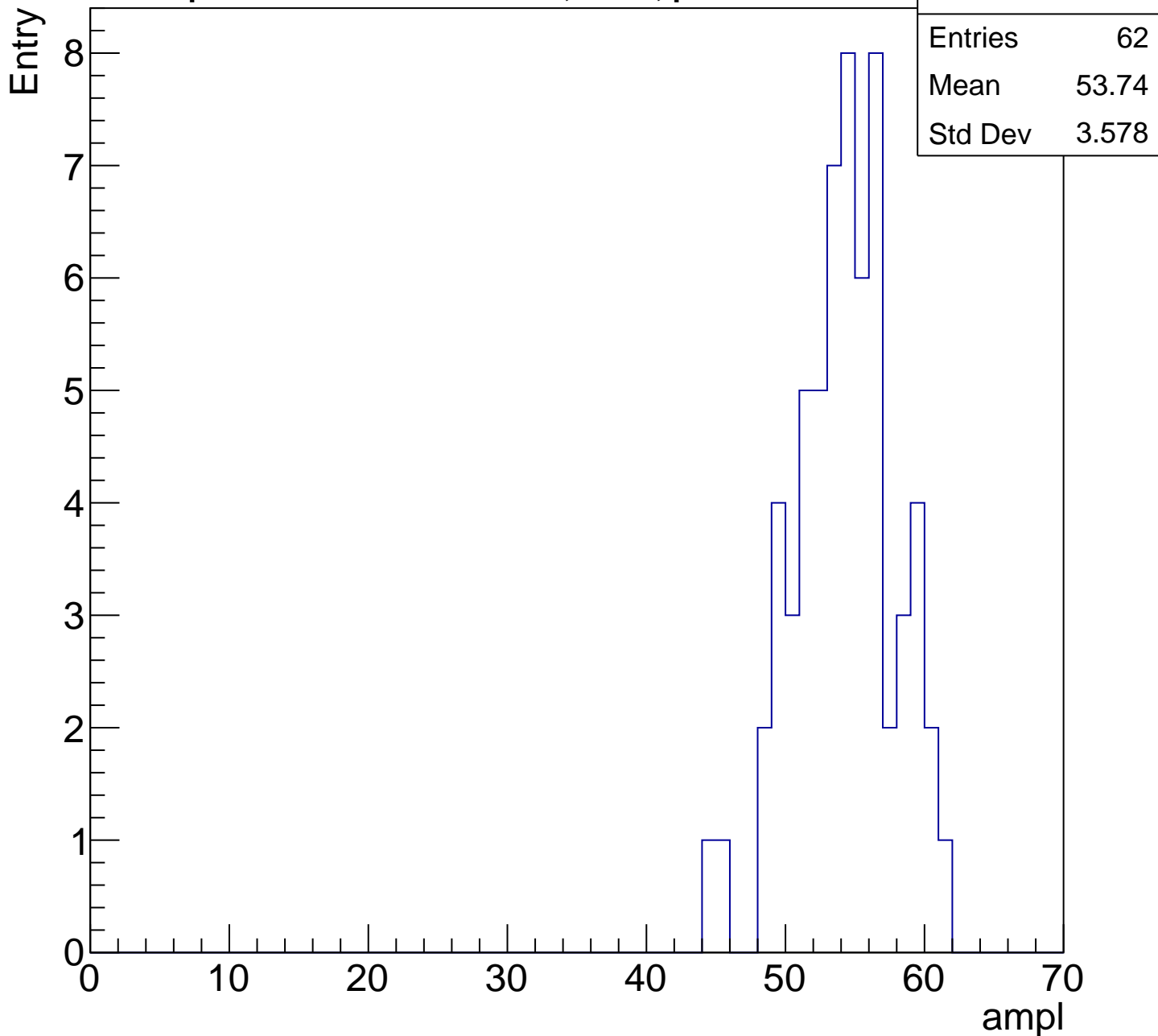
Entry

Entries	58
Mean	48.43
Std Dev	3.529



# B1L101S, U8-ch56, adc4

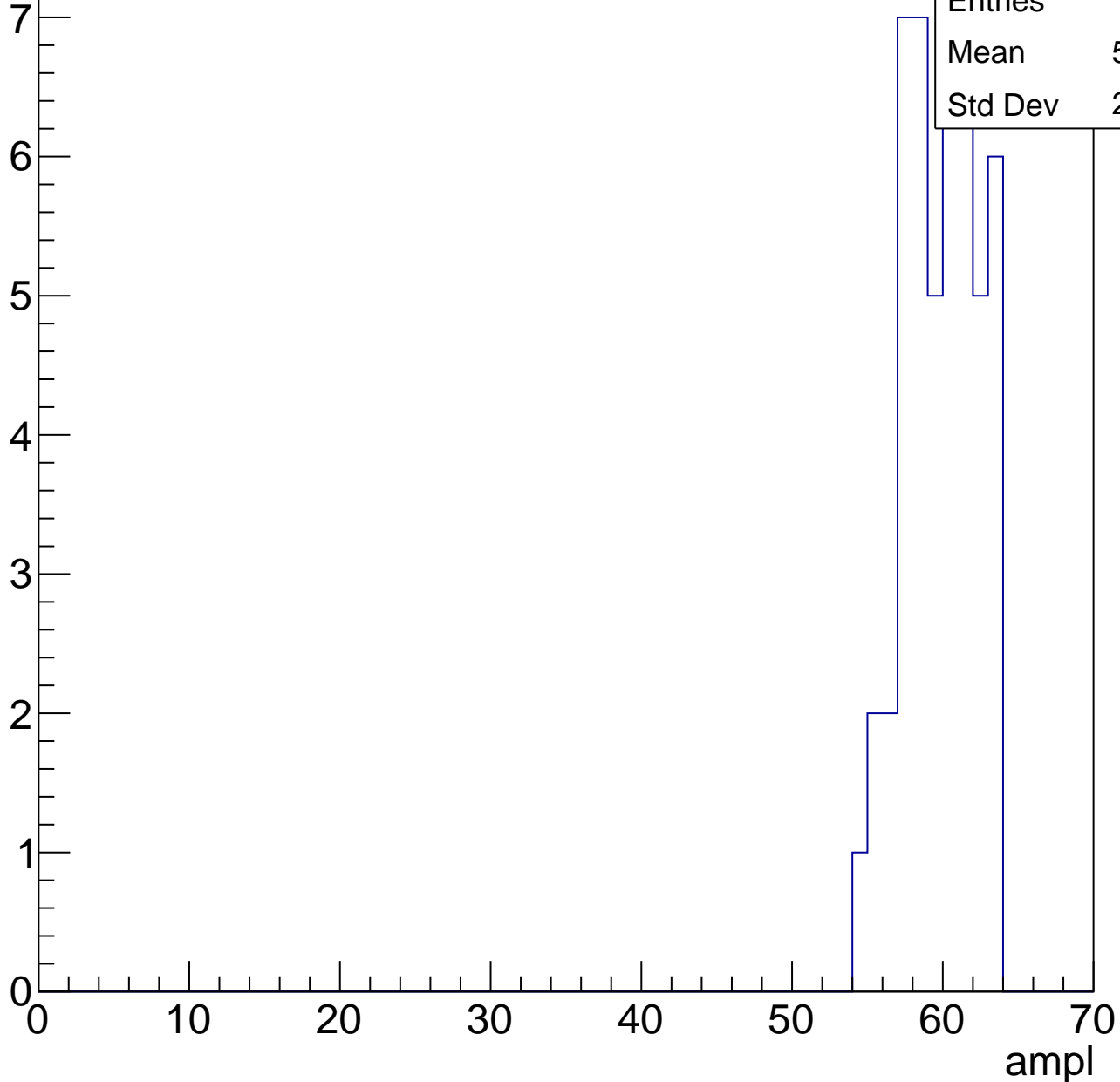
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U8-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

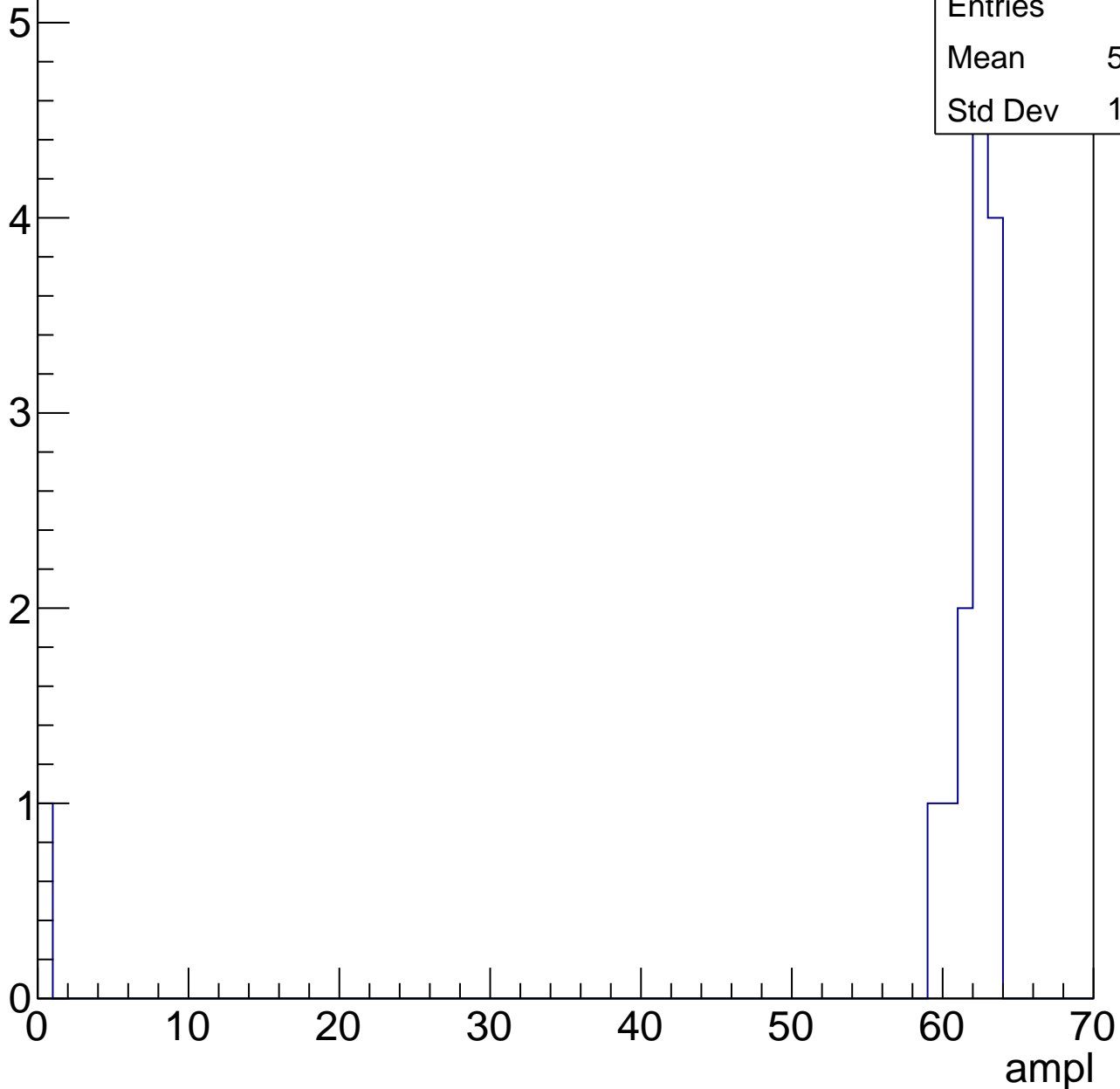


# B1L101S, U8-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	14
Mean	57.36
Std Dev	15.95

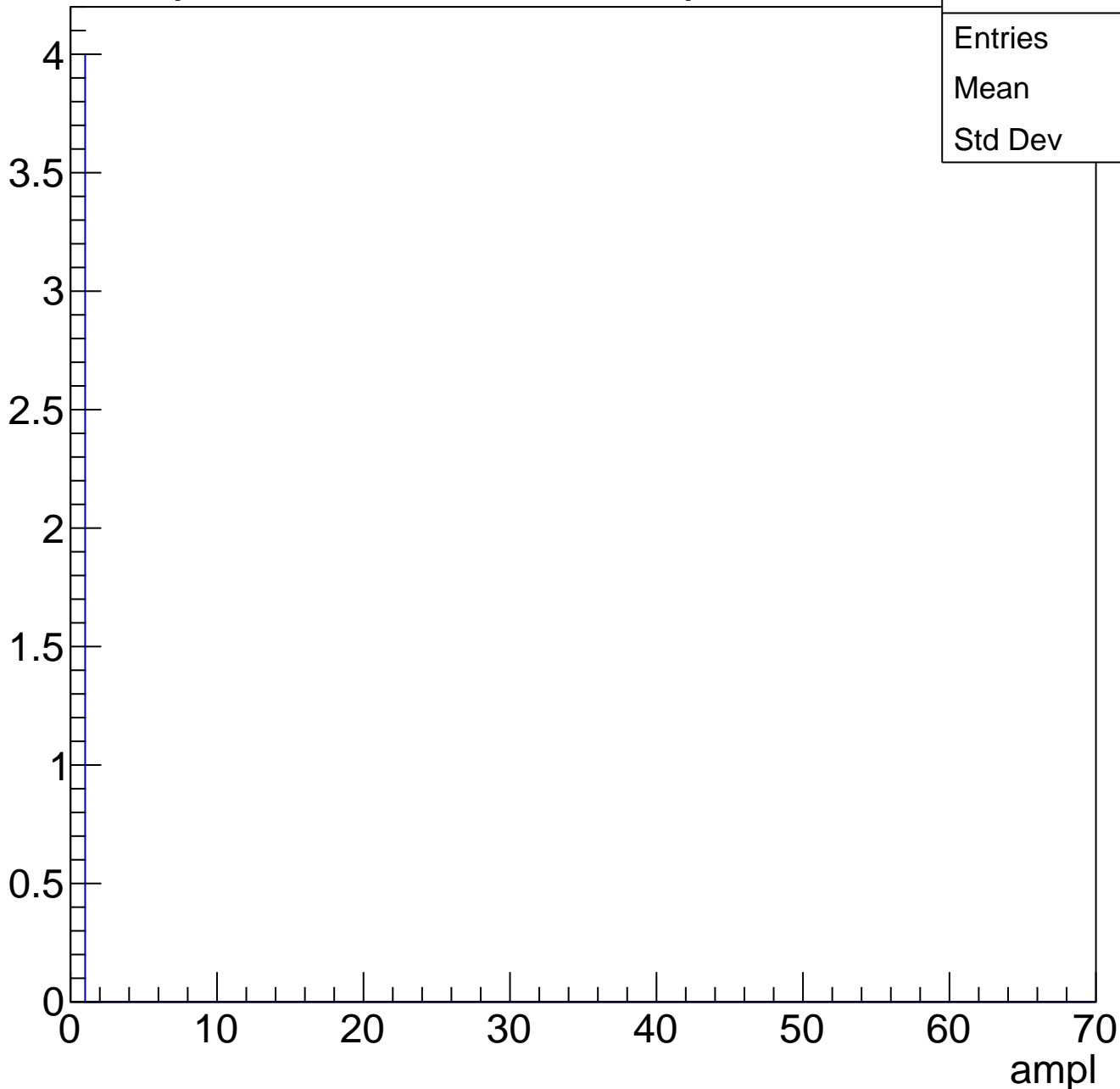




# B1L101S, U8-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	4
Mean	0
Std Dev	0

# B1L101S, U8-ch57, adc0

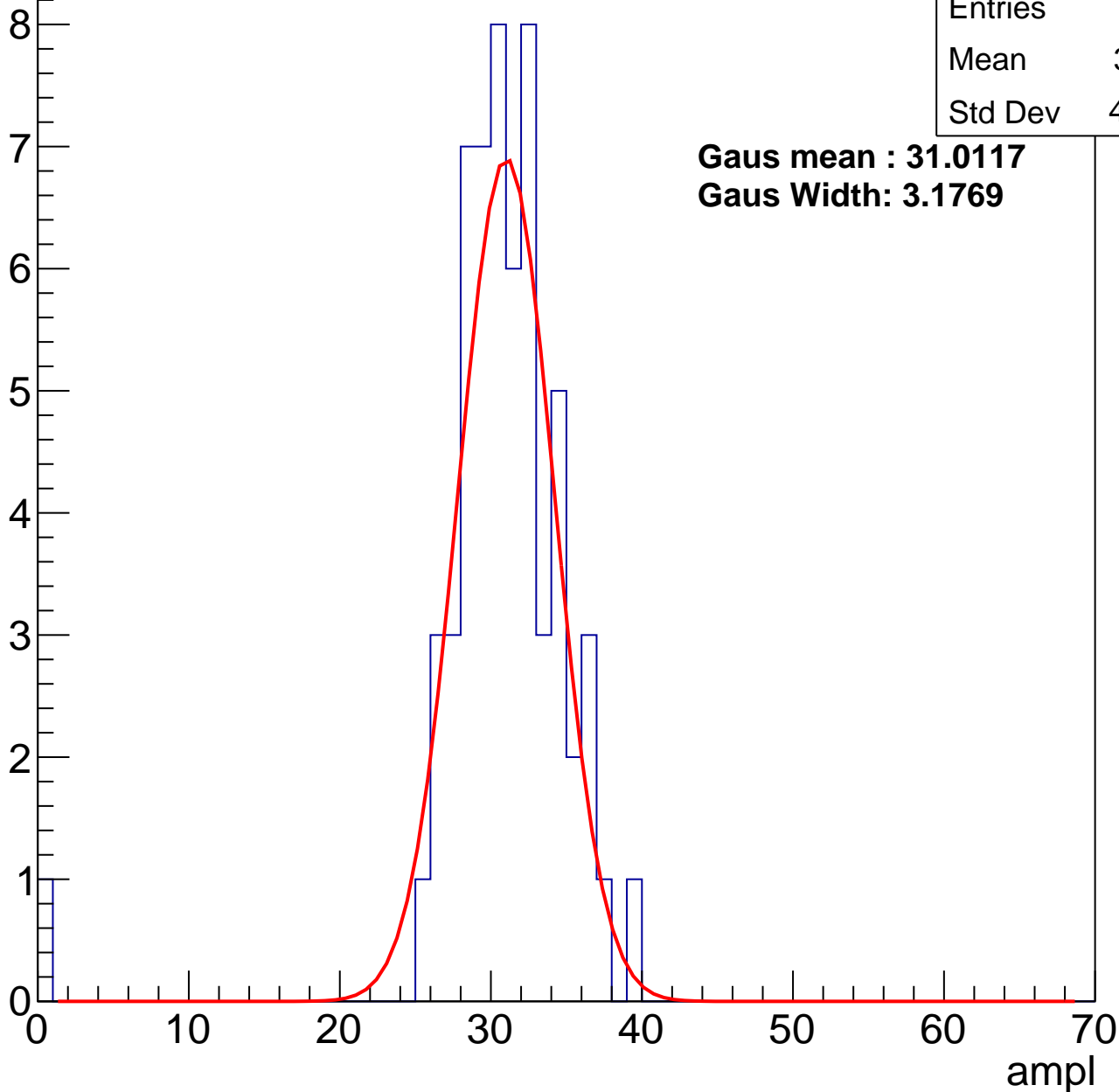
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	30.31
Std Dev	4.979

**Gaus mean : 31.0117**

**Gaus Width: 3.1769**



# B1L101S, U8-ch57, adc1

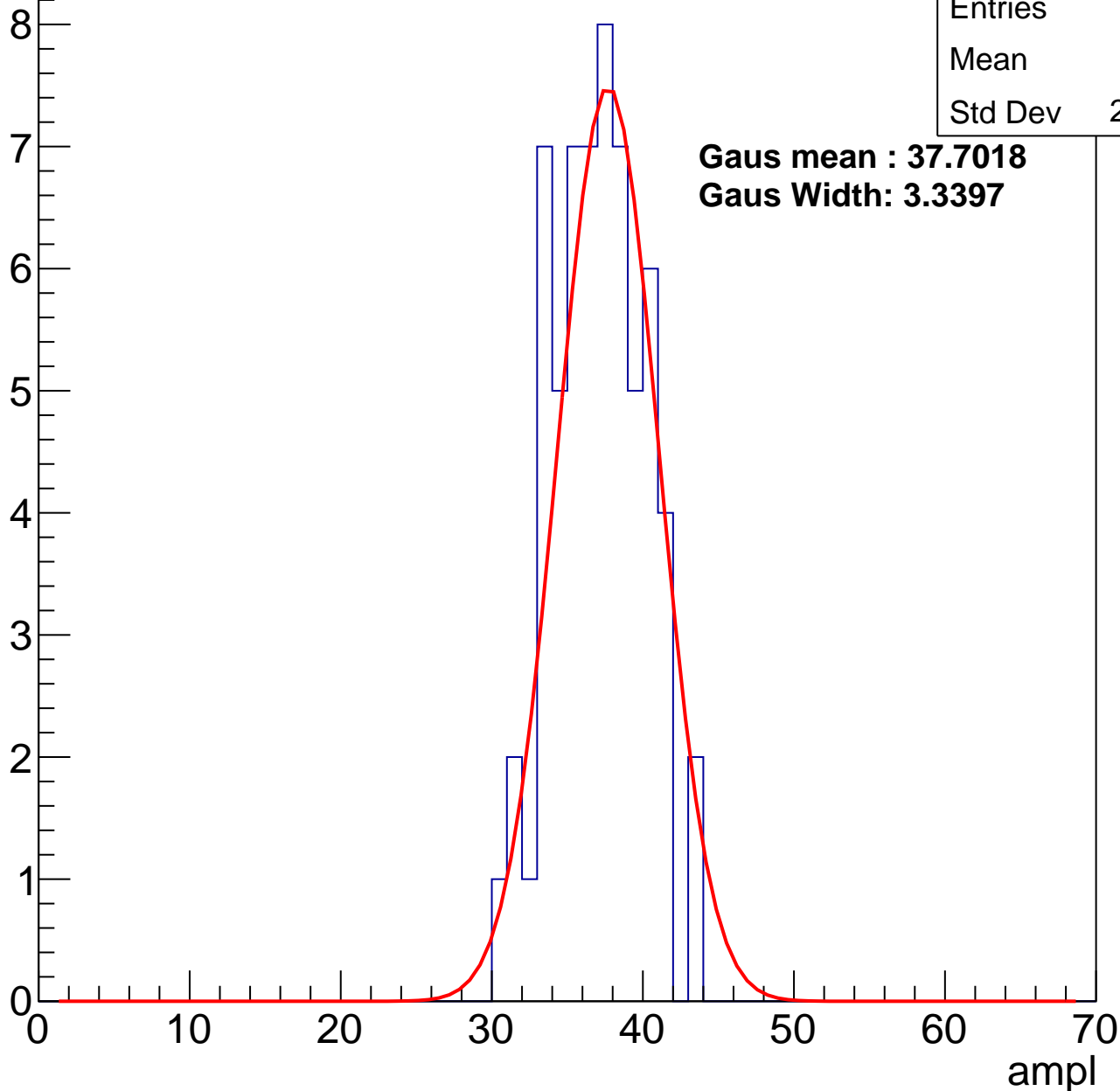
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	36.6
Std Dev	2.965

**Gaus mean : 37.7018**

**Gaus Width: 3.3397**



# B1L101S, U8-ch57, adc2

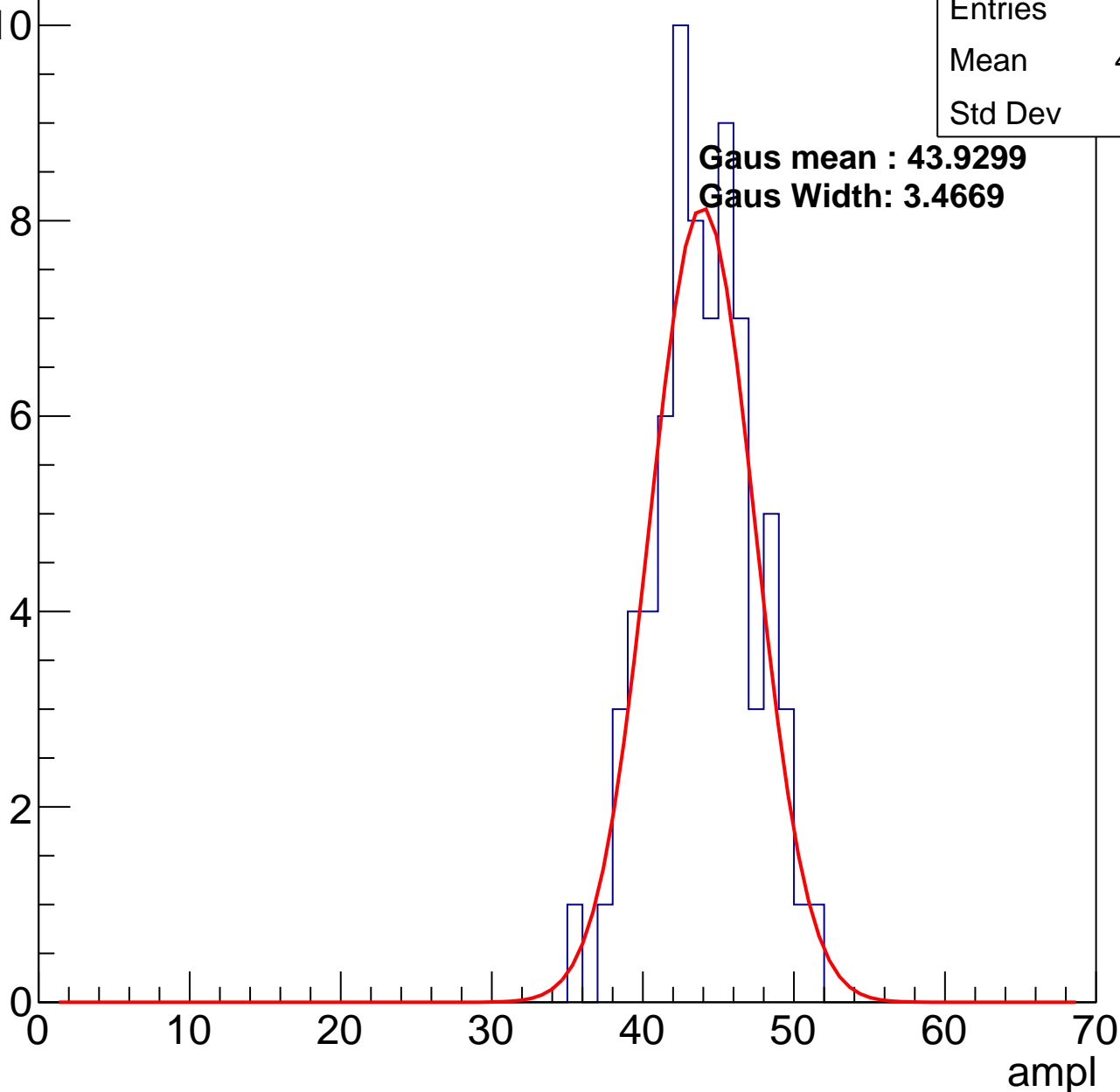
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	43.51
Std Dev	3.29

**Gaus mean : 43.9299**

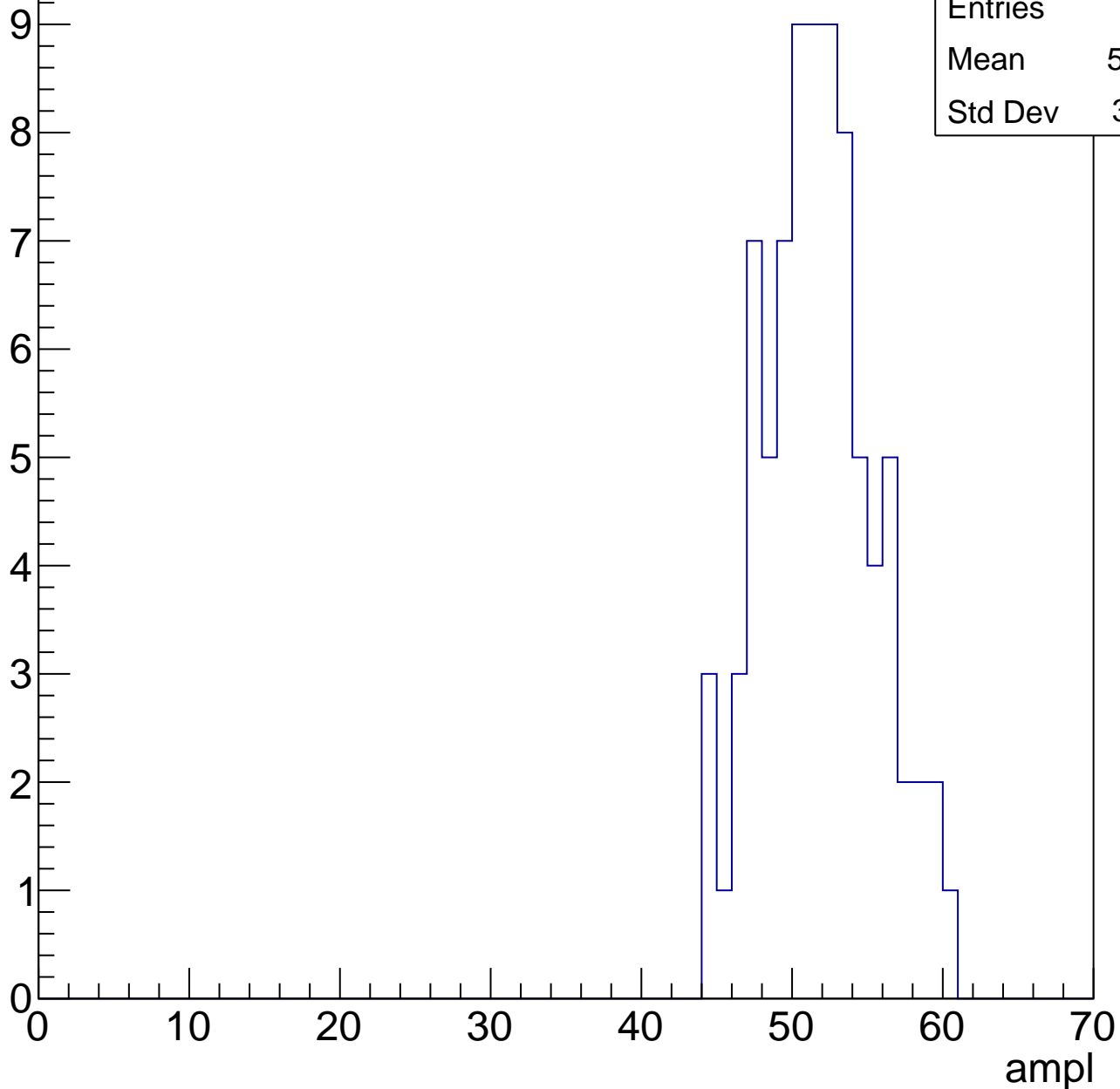
**Gaus Width: 3.4669**



# B1L101S, U8-ch57, adc3

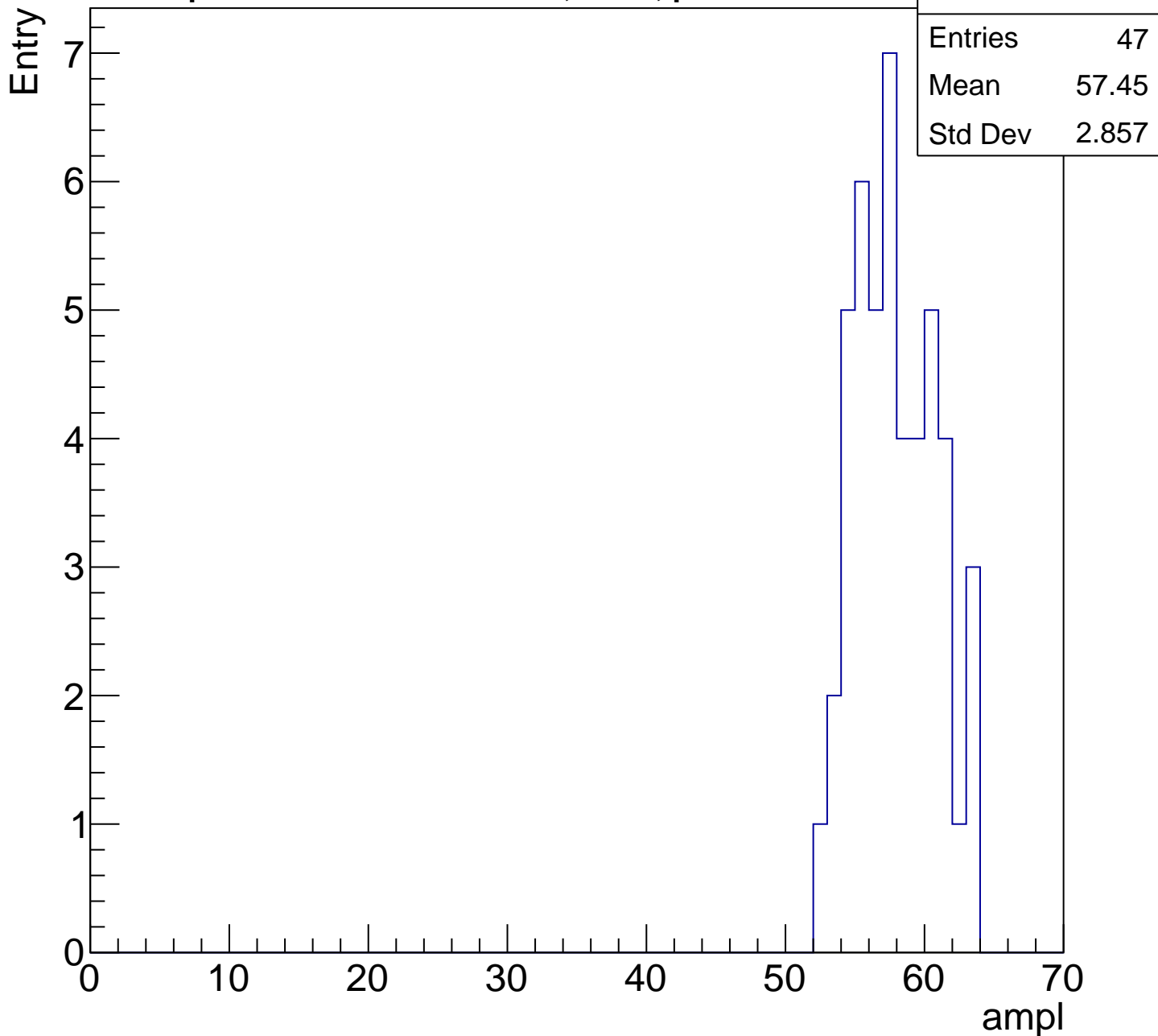
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

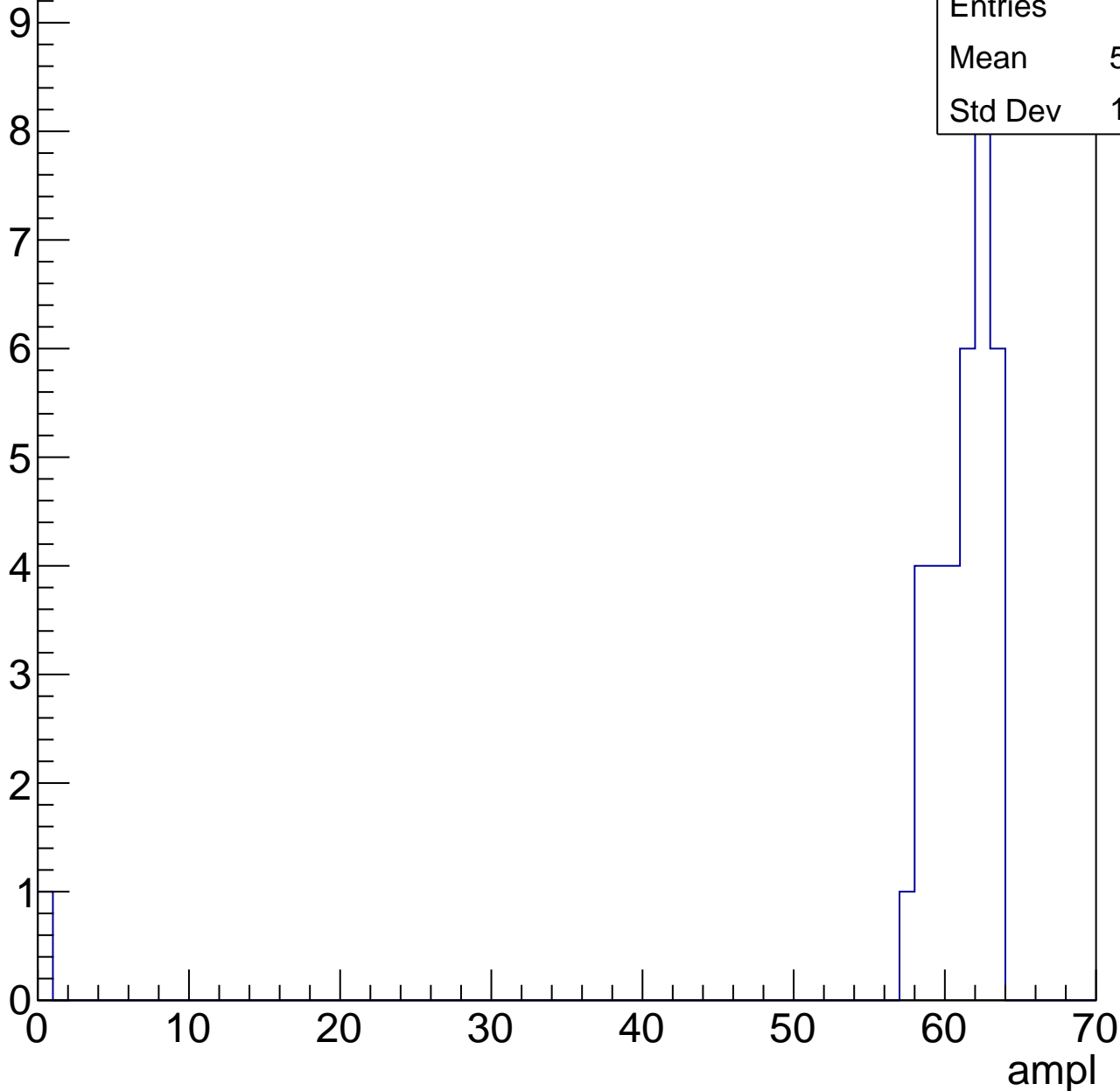


# B1L101S, U8-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	35
Mean	59.06
Std Dev	10.27



# B1L101S, U8-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U8-ch58, adc0

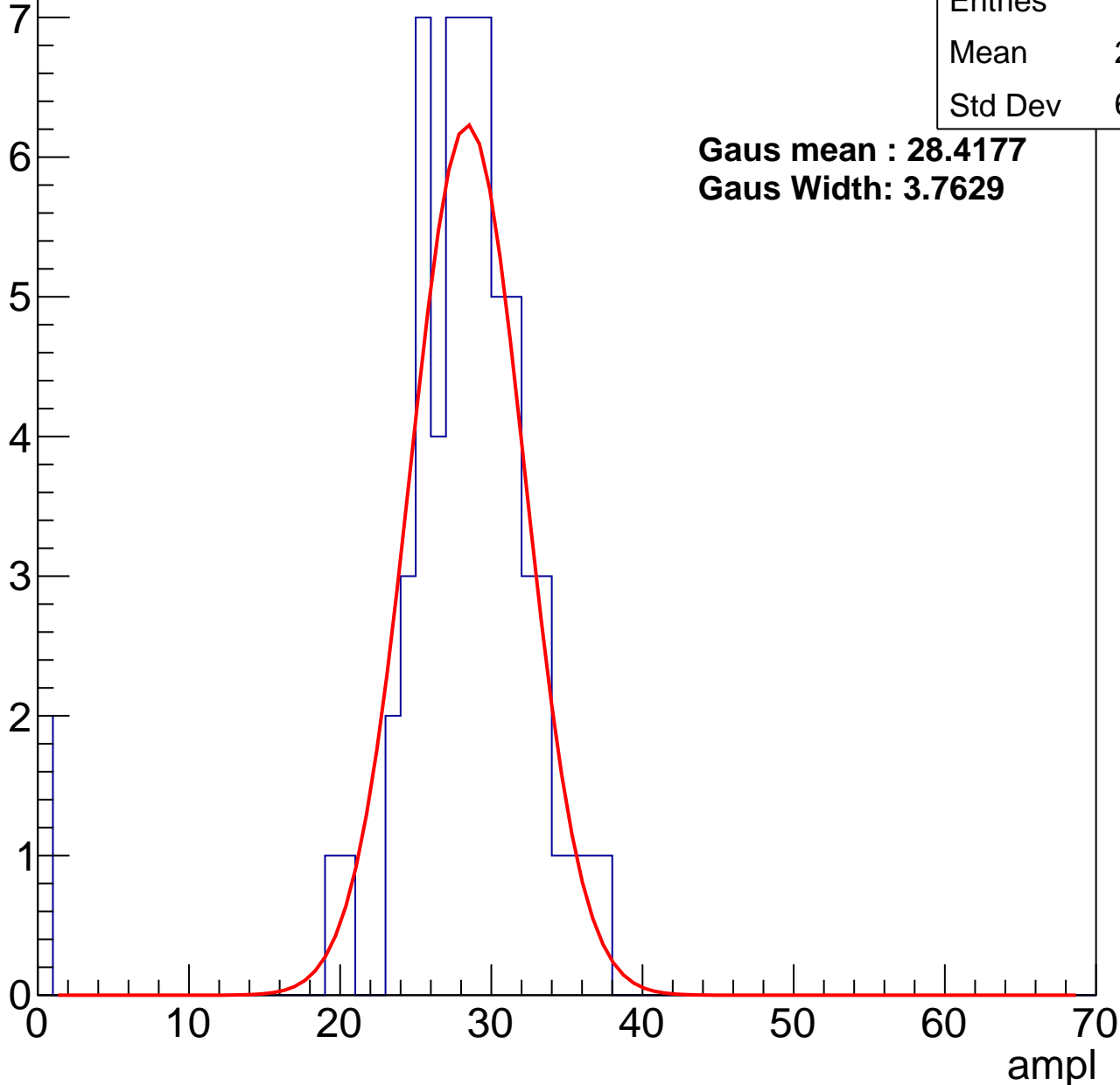
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	27.31
Std Dev	6.131

**Gaus mean : 28.4177**

**Gaus Width: 3.7629**



# B1L101S, U8-ch58, adc1

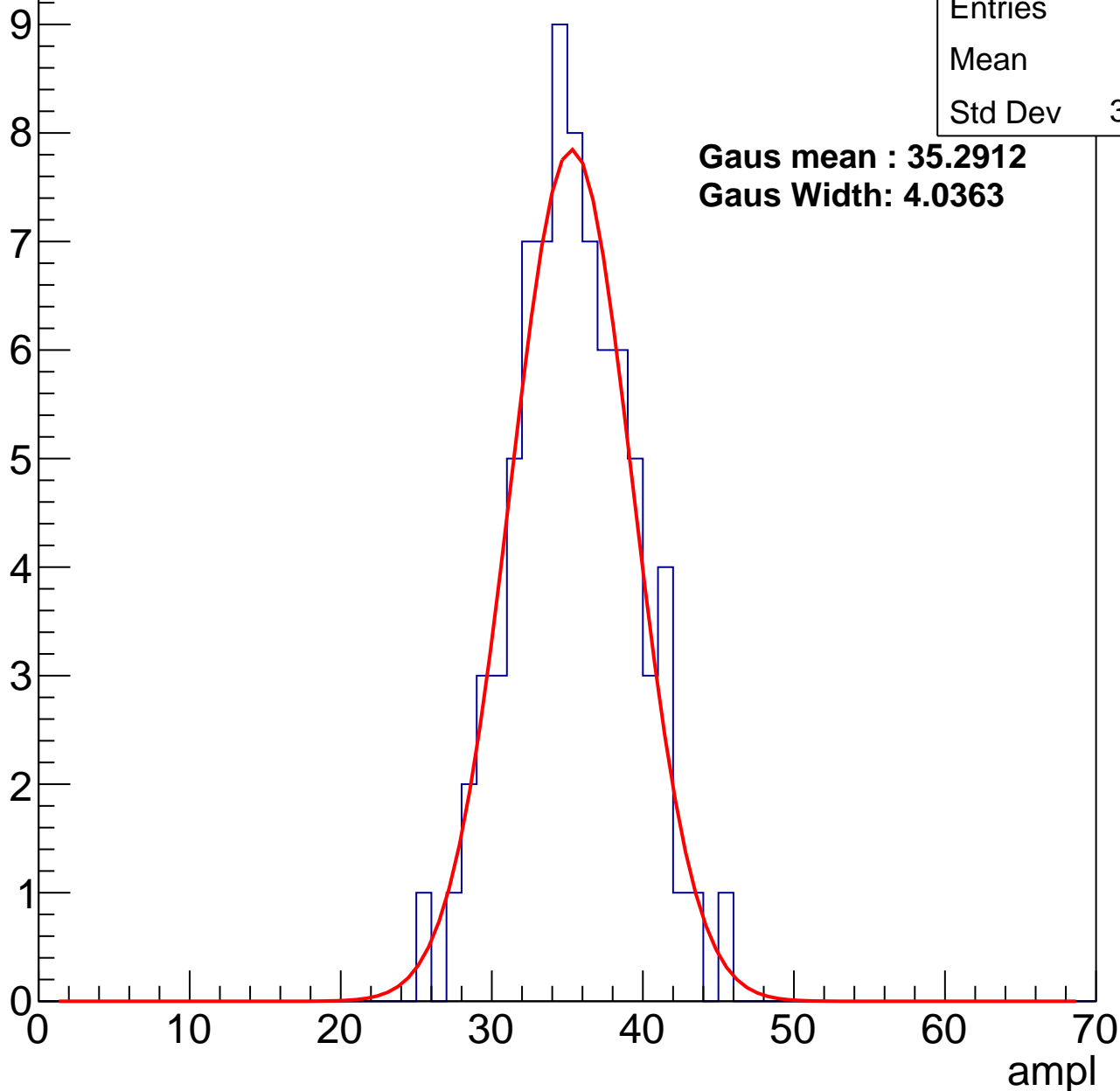
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	34.9
Std Dev	3.907

**Gaus mean : 35.2912**

**Gaus Width: 4.0363**



# B1L101S, U8-ch58, adc2

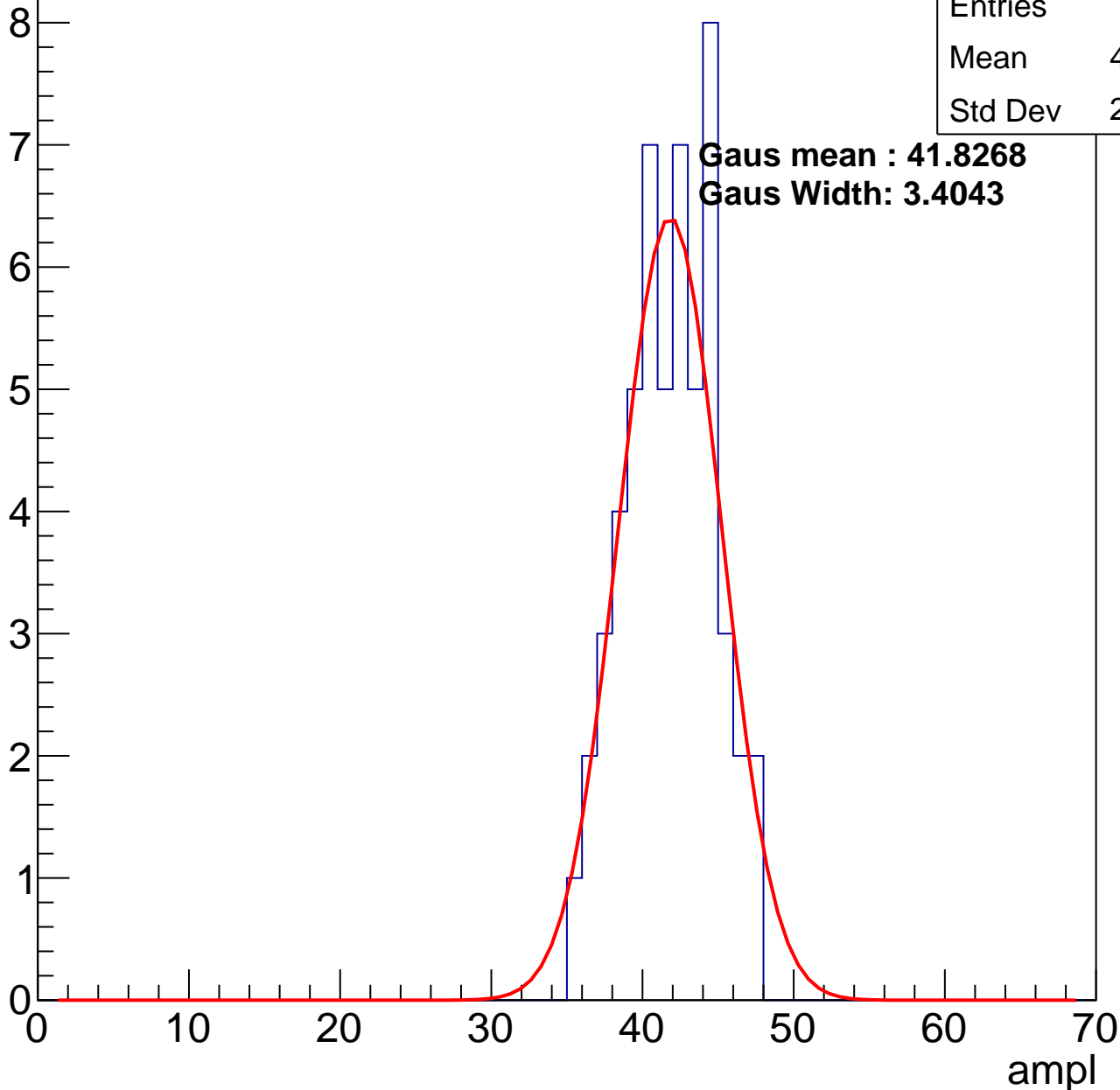
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	41.33
Std Dev	2.919

**Gaus mean : 41.8268**

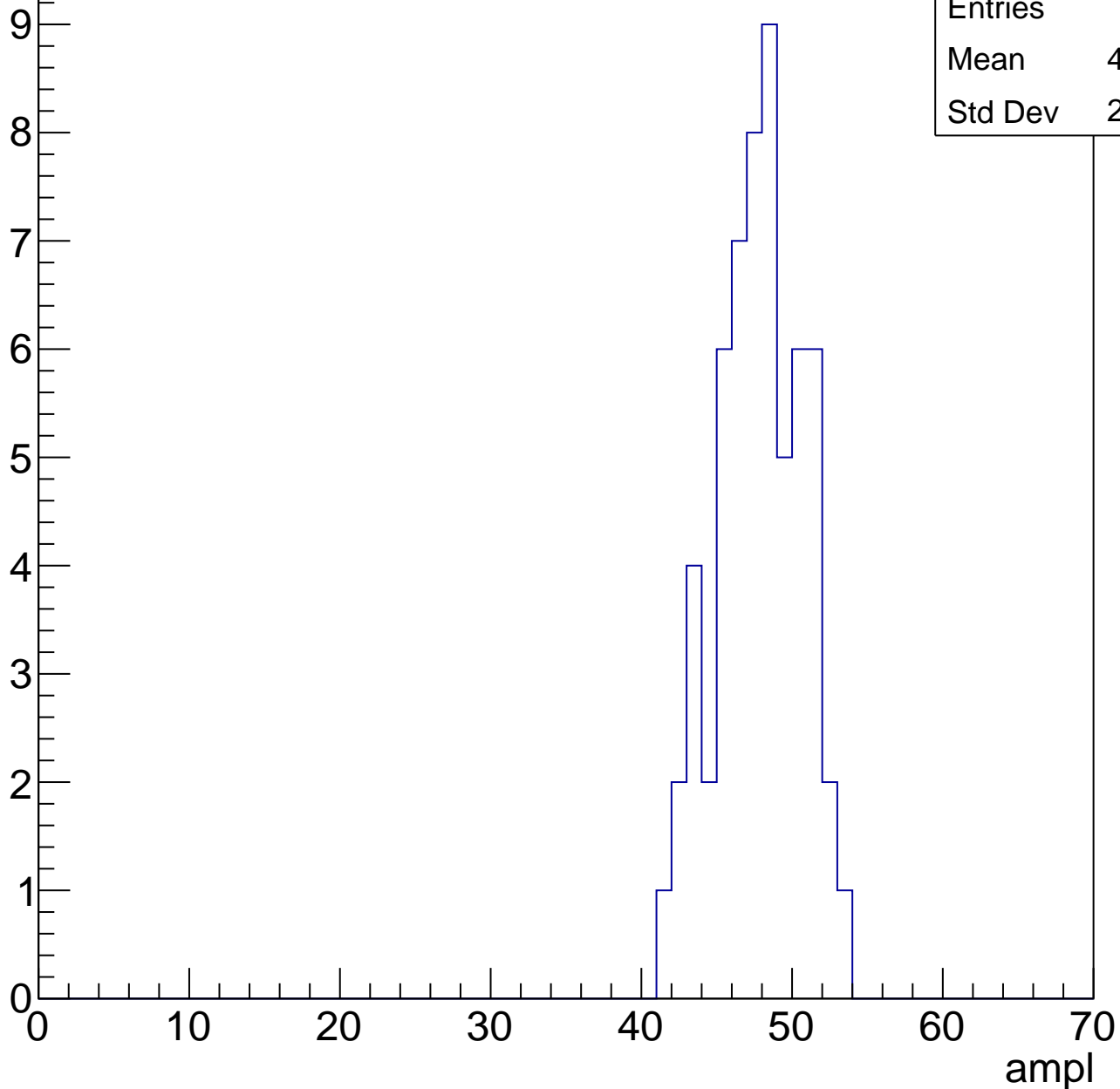
**Gaus Width: 3.4043**



# B1L101S, U8-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

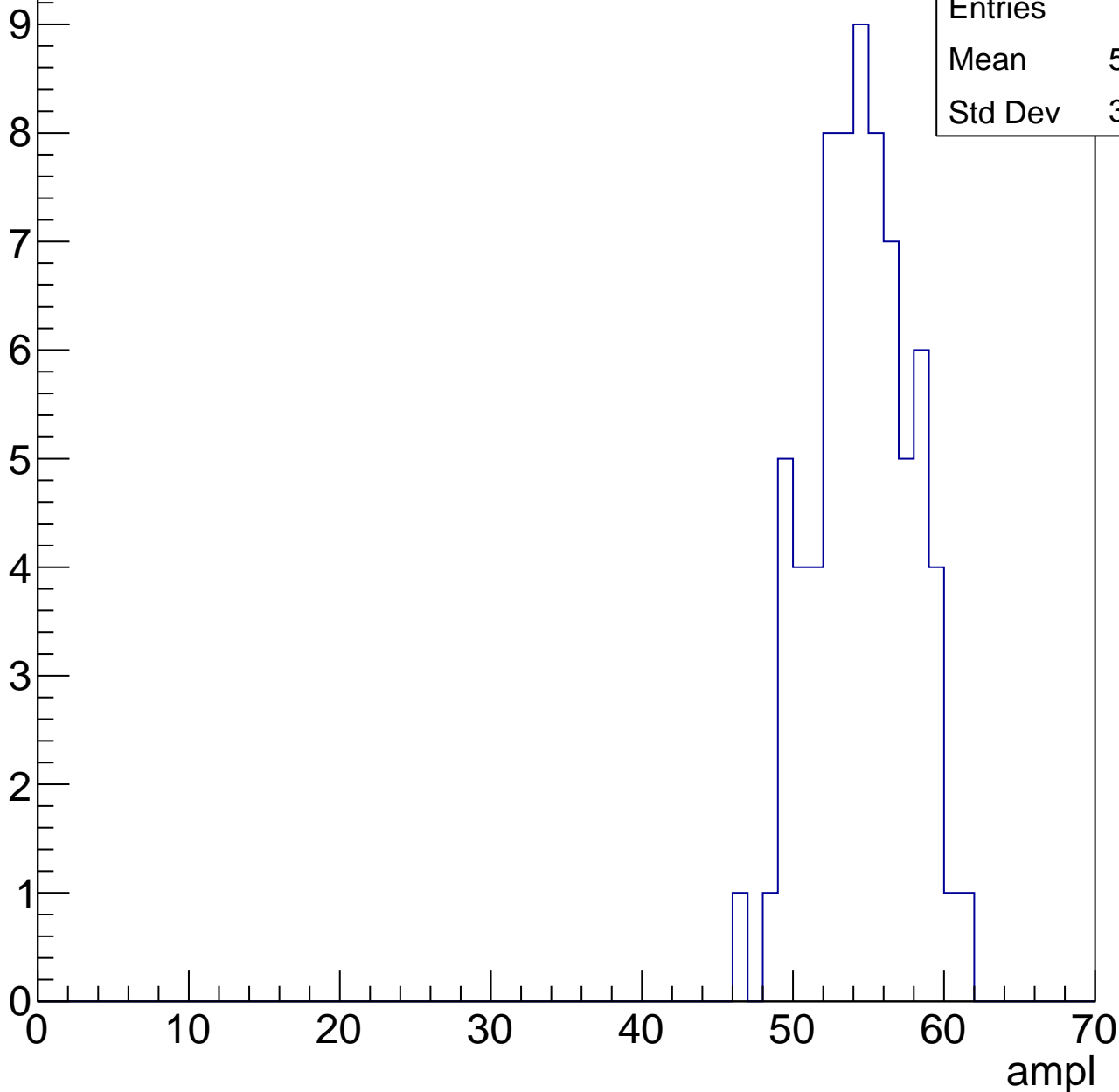
Entry



# B1L101S, U8-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch58, adc5

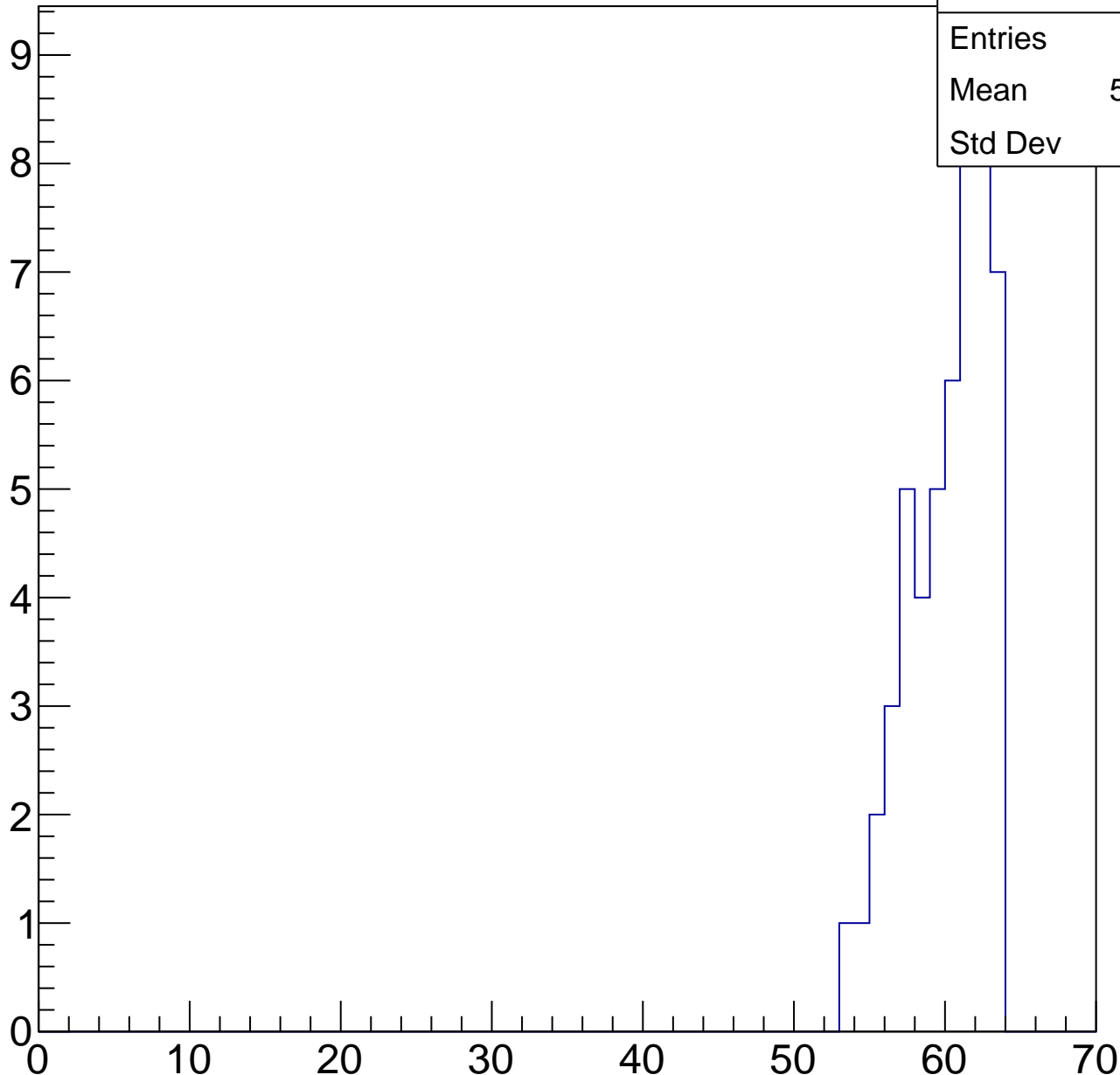
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	59.67
Std Dev	2.61

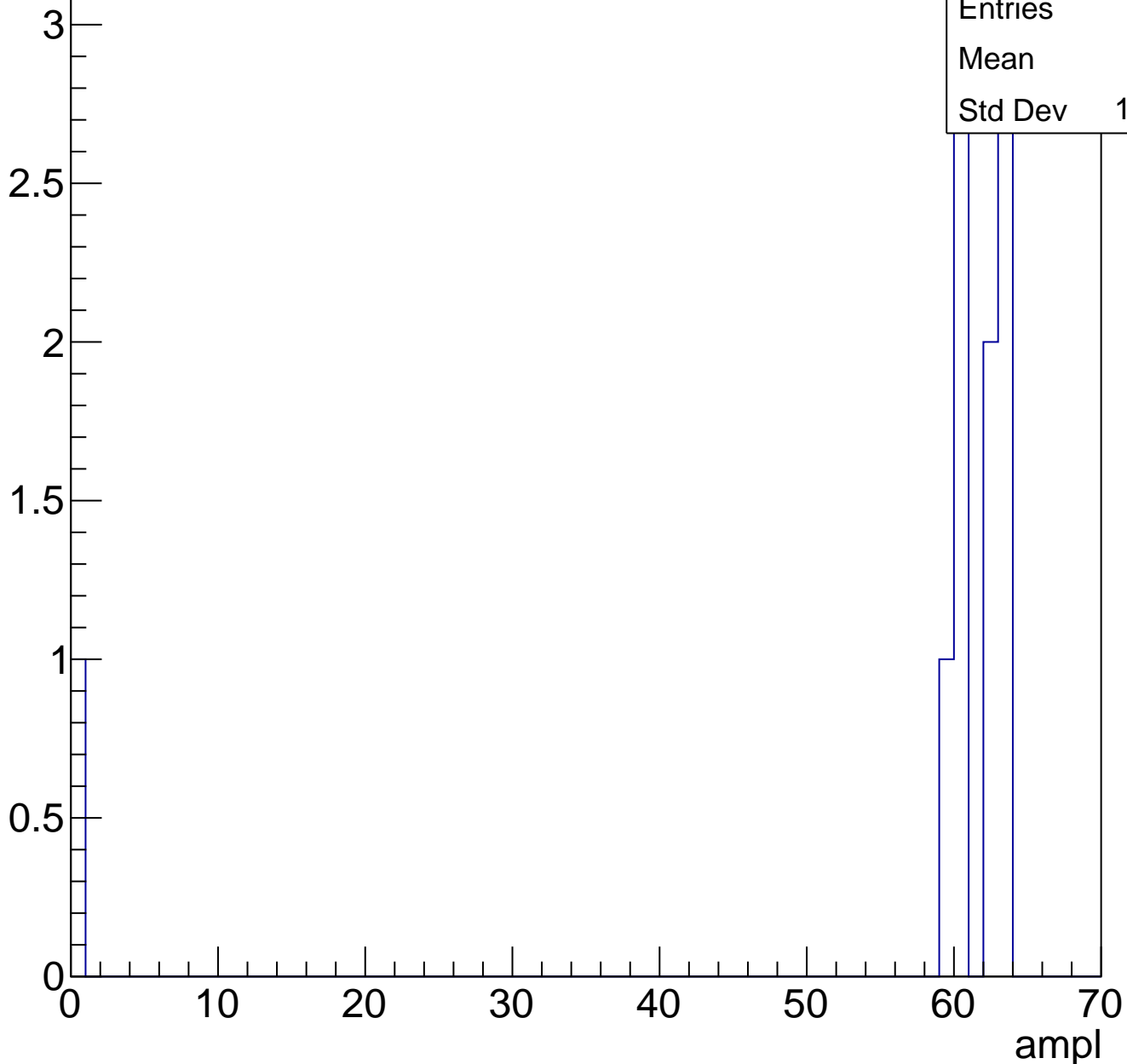
ampl



# B1L101S, U8-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U8-ch59, adc0

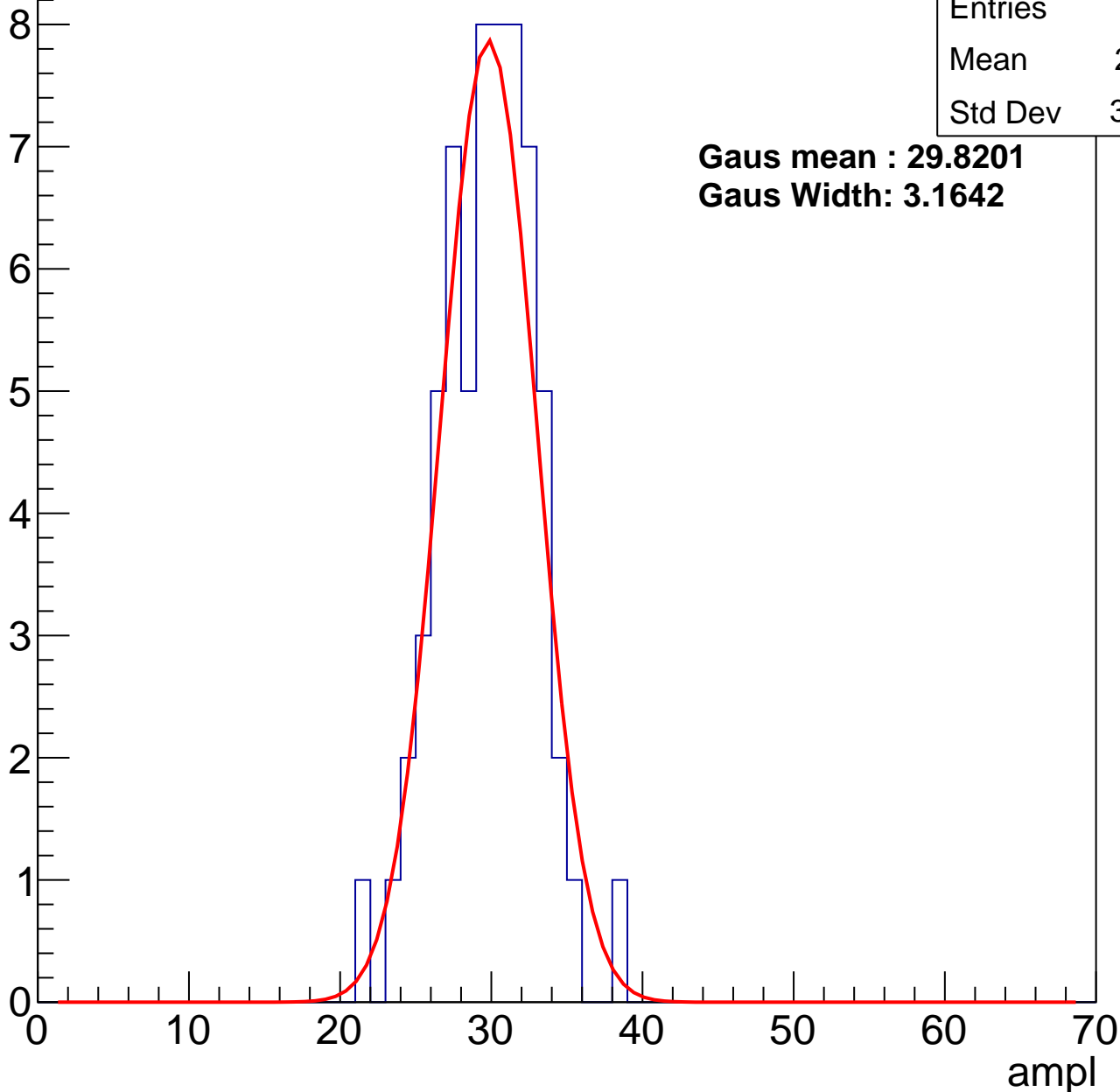
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	29.31
Std Dev	3.112

**Gaus mean : 29.8201**

**Gaus Width: 3.1642**



# B1L101S, U8-ch59, adc1

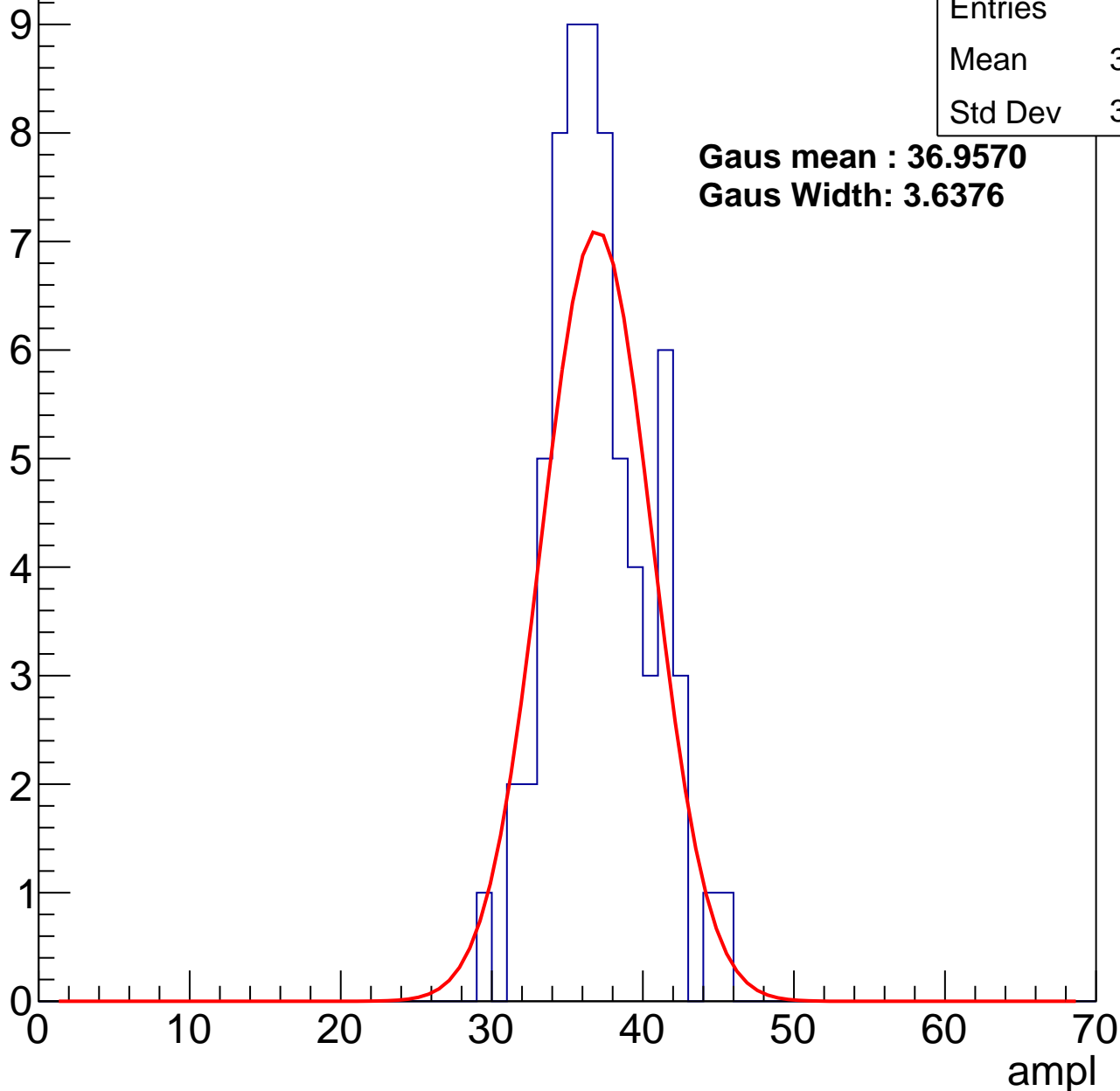
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	36.63
Std Dev	3.245

**Gaus mean : 36.9570**

**Gaus Width: 3.6376**



# B1L101S, U8-ch59, adc2

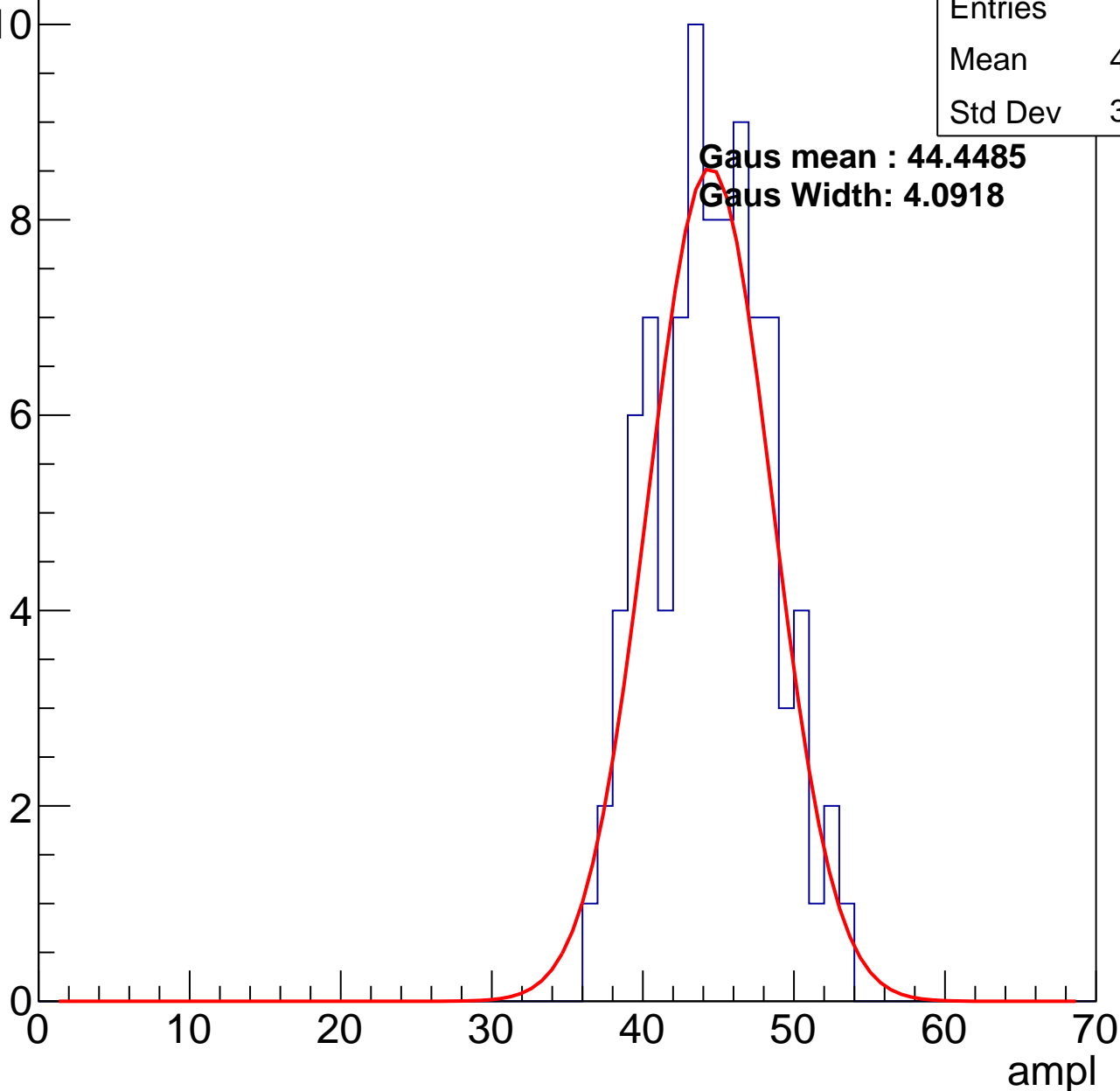
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	91
Mean	44.07
Std Dev	3.834

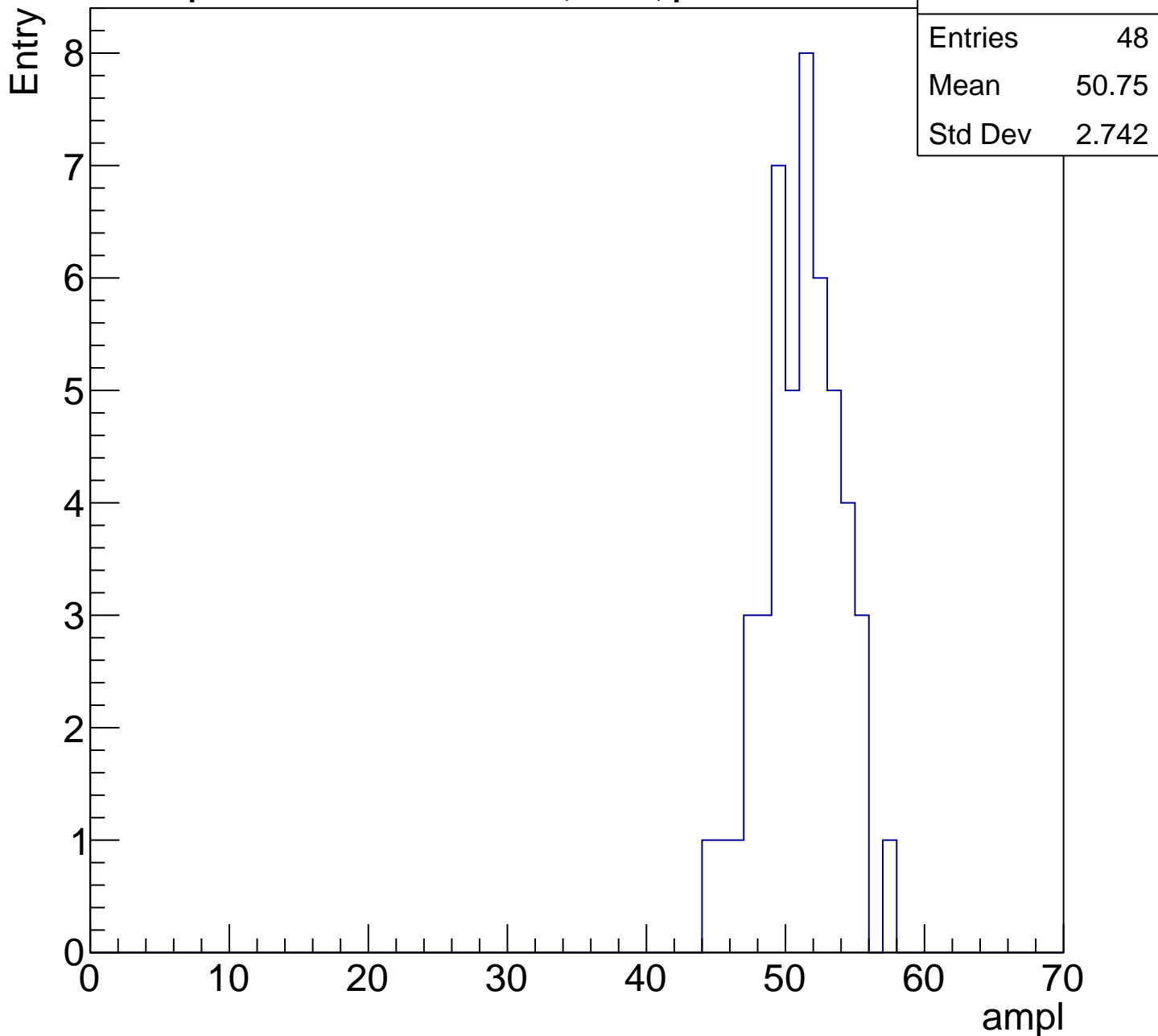
**Gaus mean : 44.4485**

**Gaus Width: 4.0918**



# B1L101S, U8-ch59, adc3

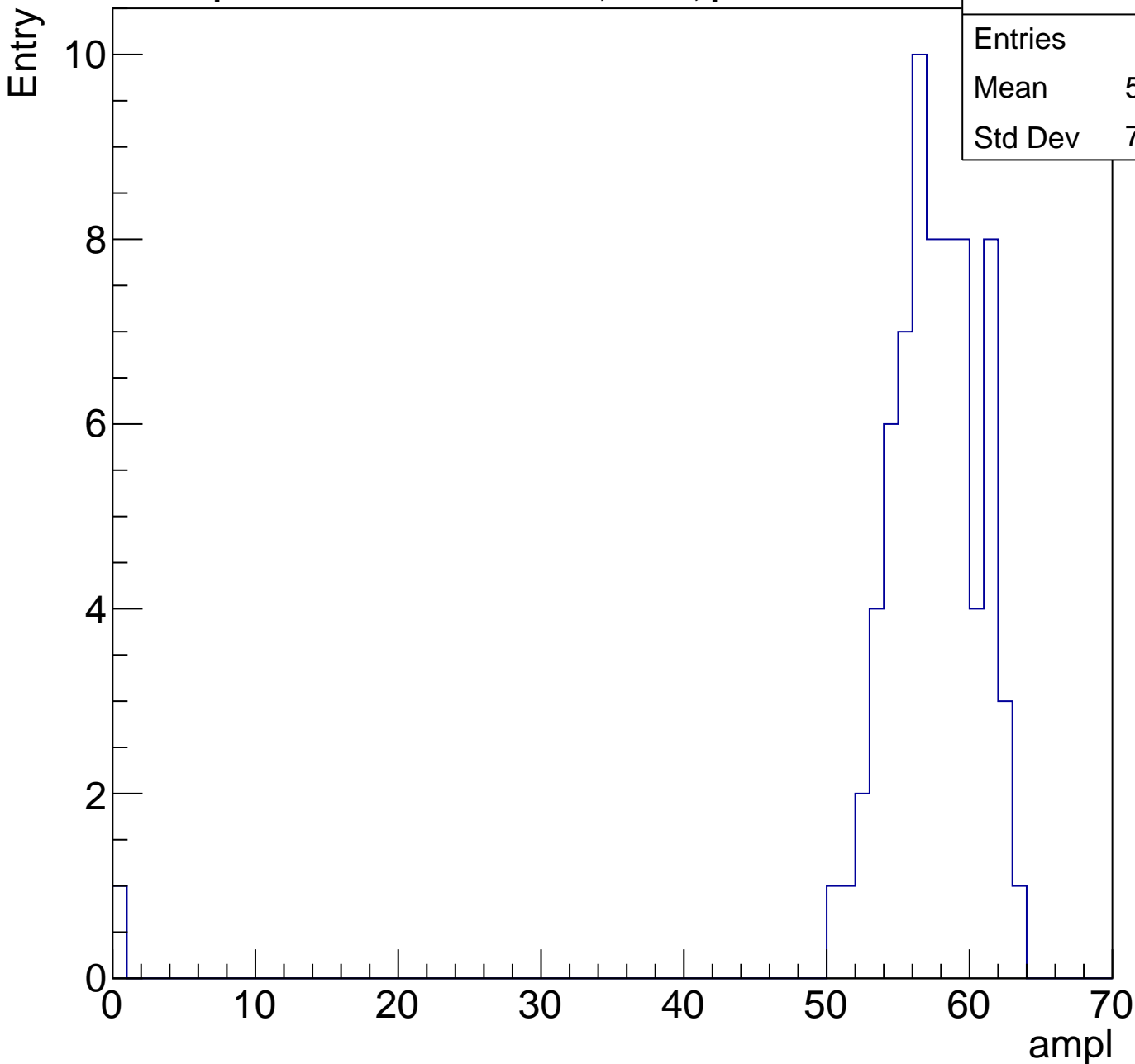
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U8-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	72
Mean	56.32
Std Dev	7.286

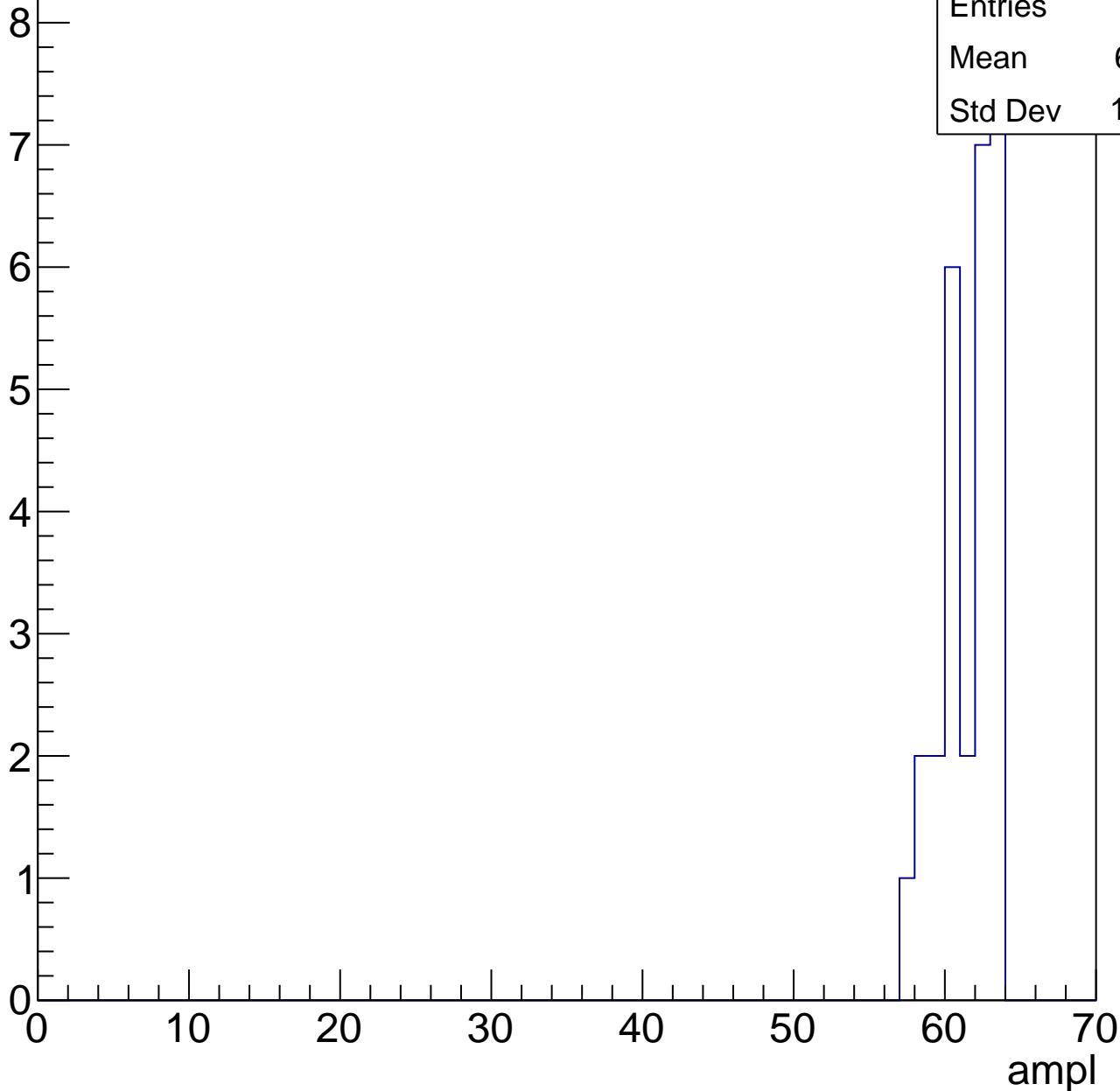


# B1L101S, U8-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	28
Mean	61.11
Std Dev	1.759



# B1L101S, U8-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch60, adc0

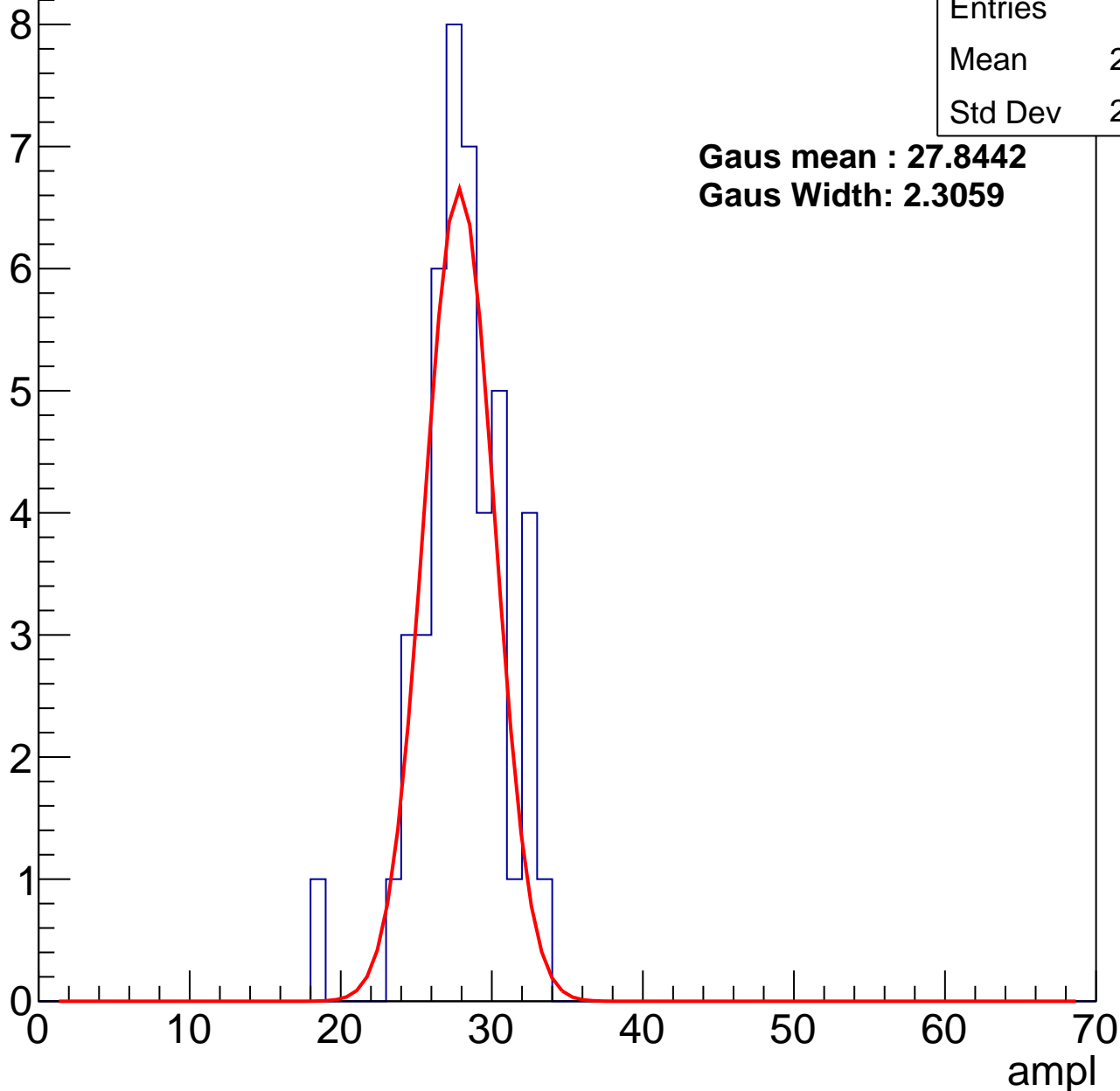
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	44
Mean	27.59
Std Dev	2.807

**Gaus mean : 27.8442**

**Gaus Width: 2.3059**



# B1L101S, U8-ch60, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	83
Mean	33.76
Std Dev	3.672

**Gaus mean : 34.1636**

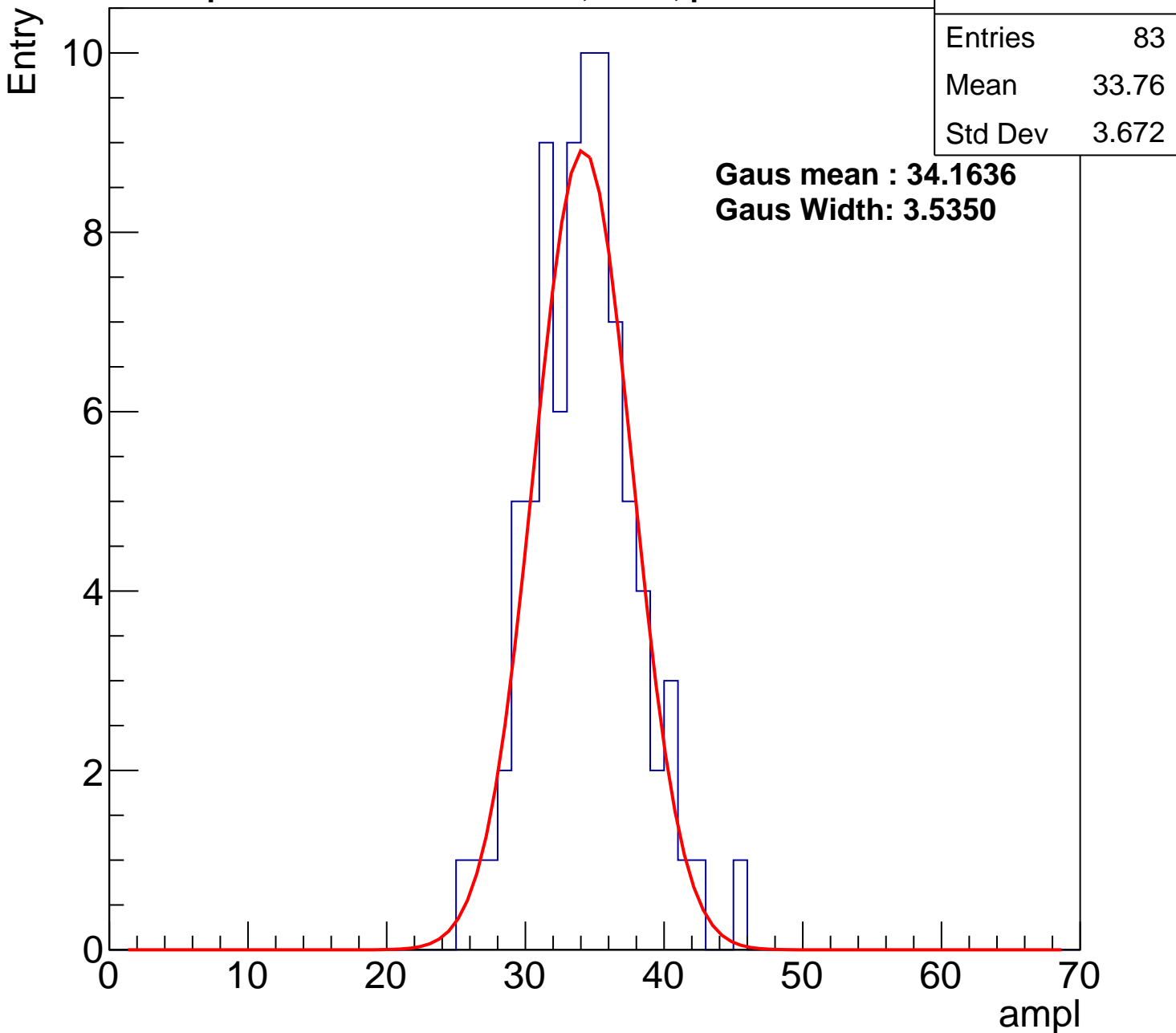
**Gaus Width: 3.5350**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U8-ch60, adc2

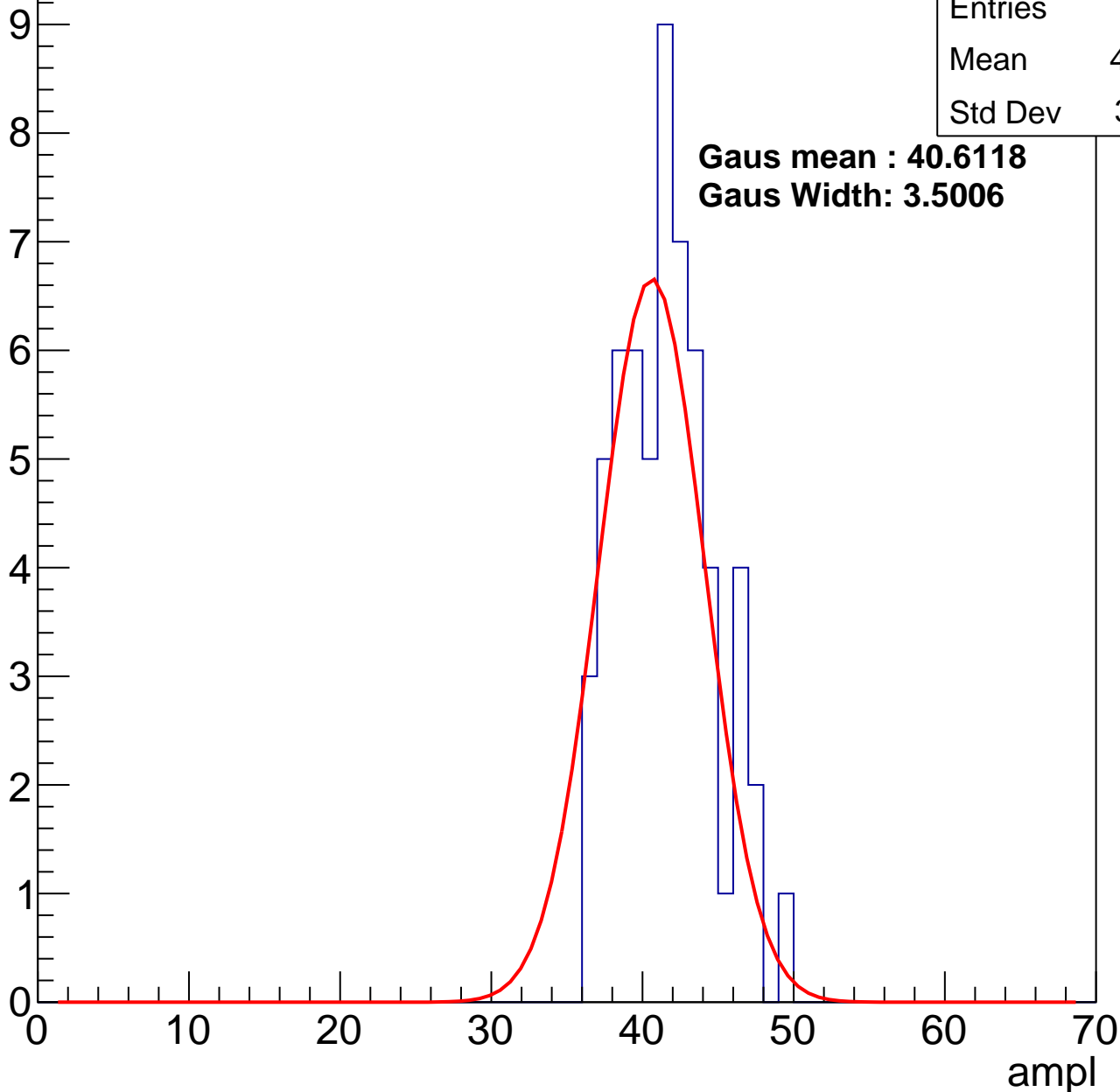
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	41.08
Std Dev	3.071

**Gaus mean : 40.6118**

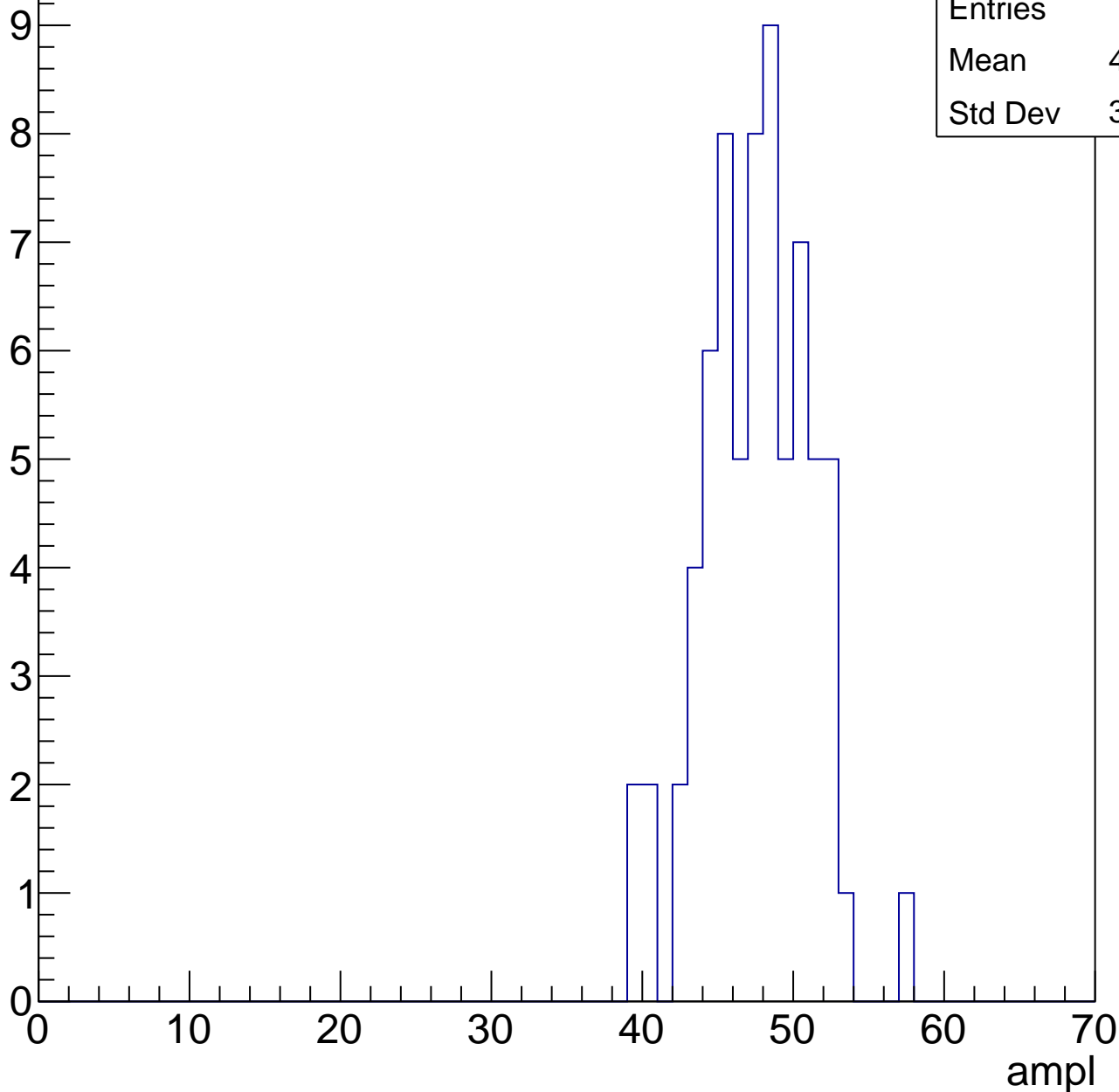
**Gaus Width: 3.5006**



# B1L101S, U8-ch60, adc3

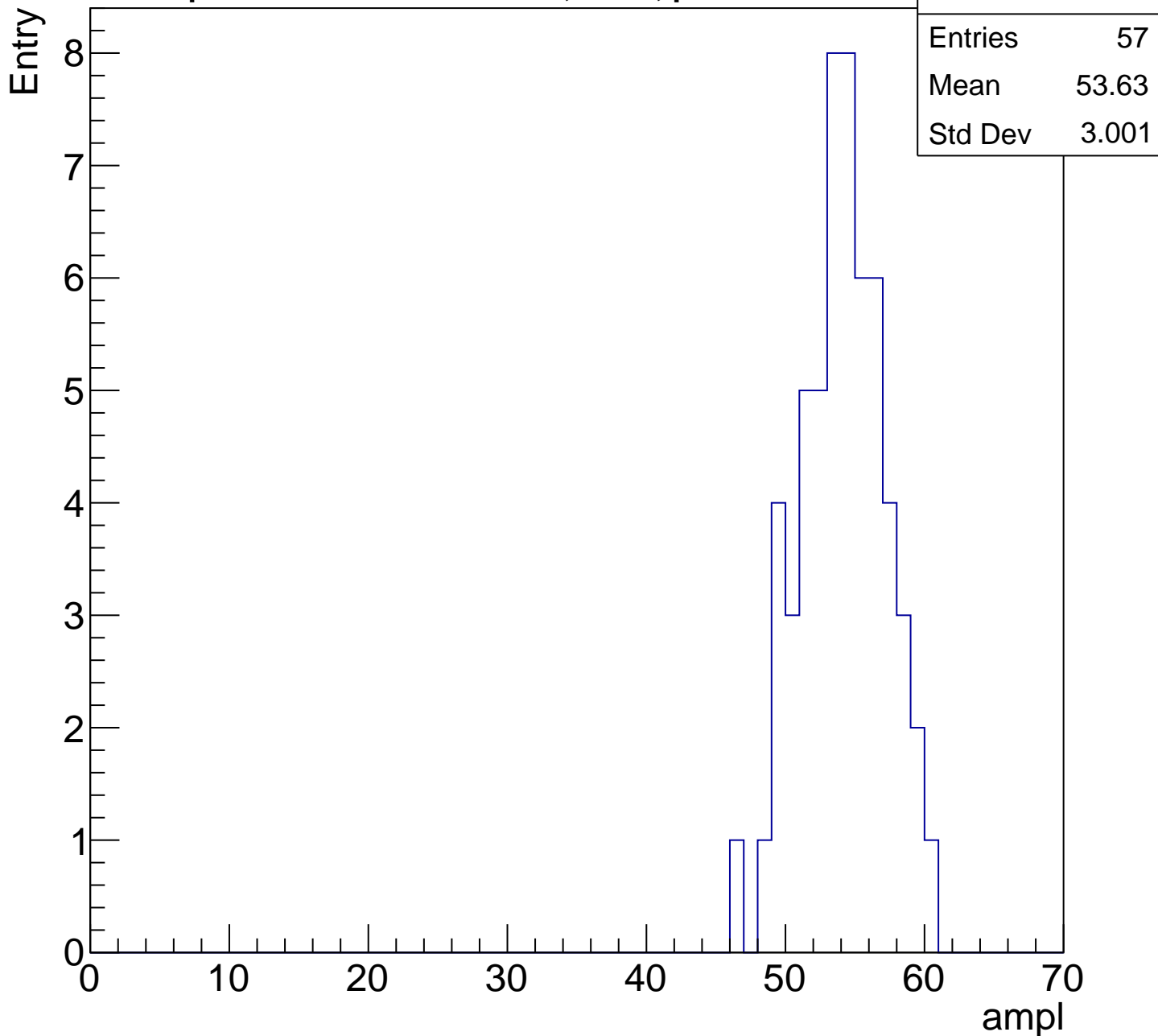
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



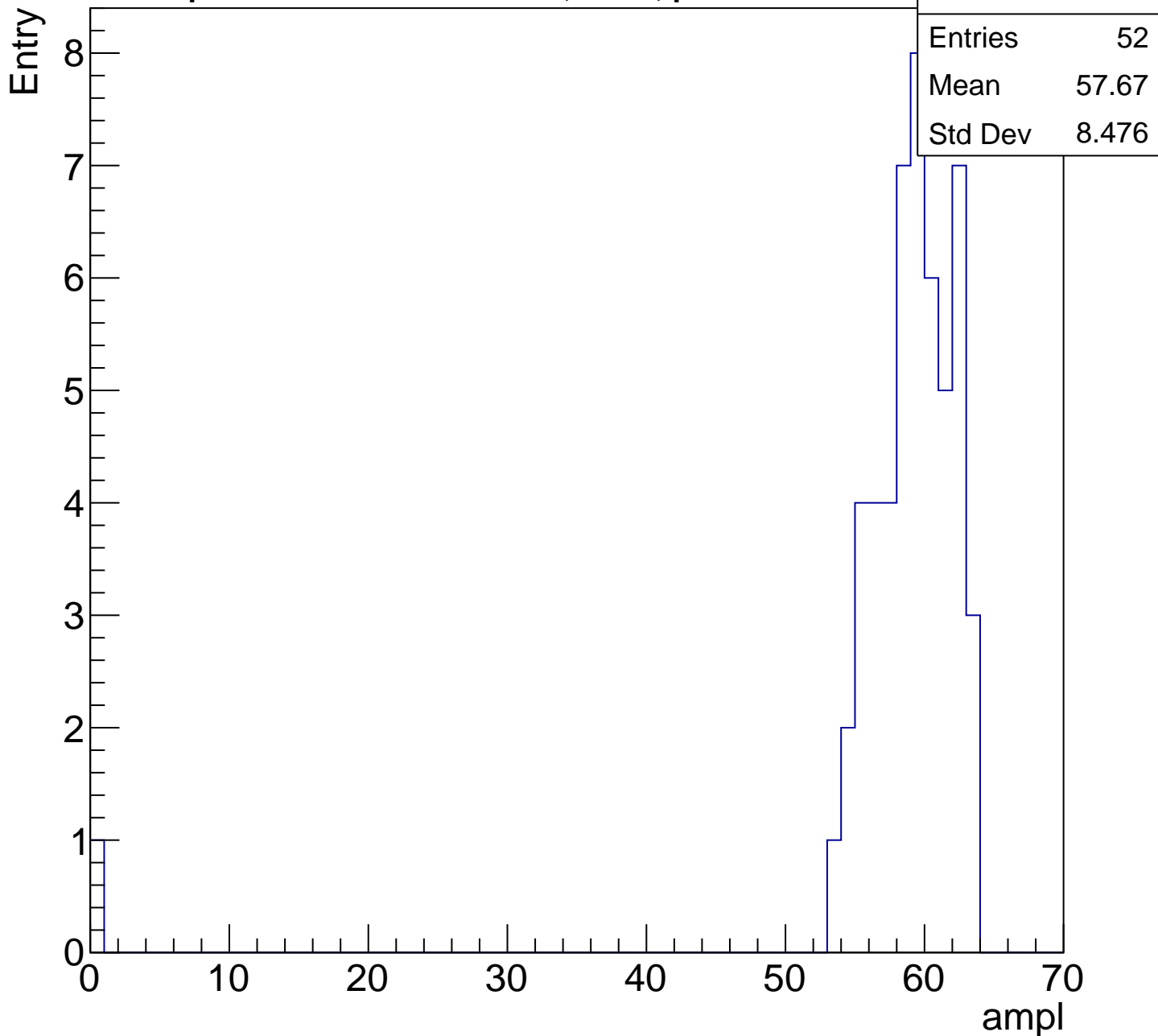
# B1L101S, U8-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U8-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

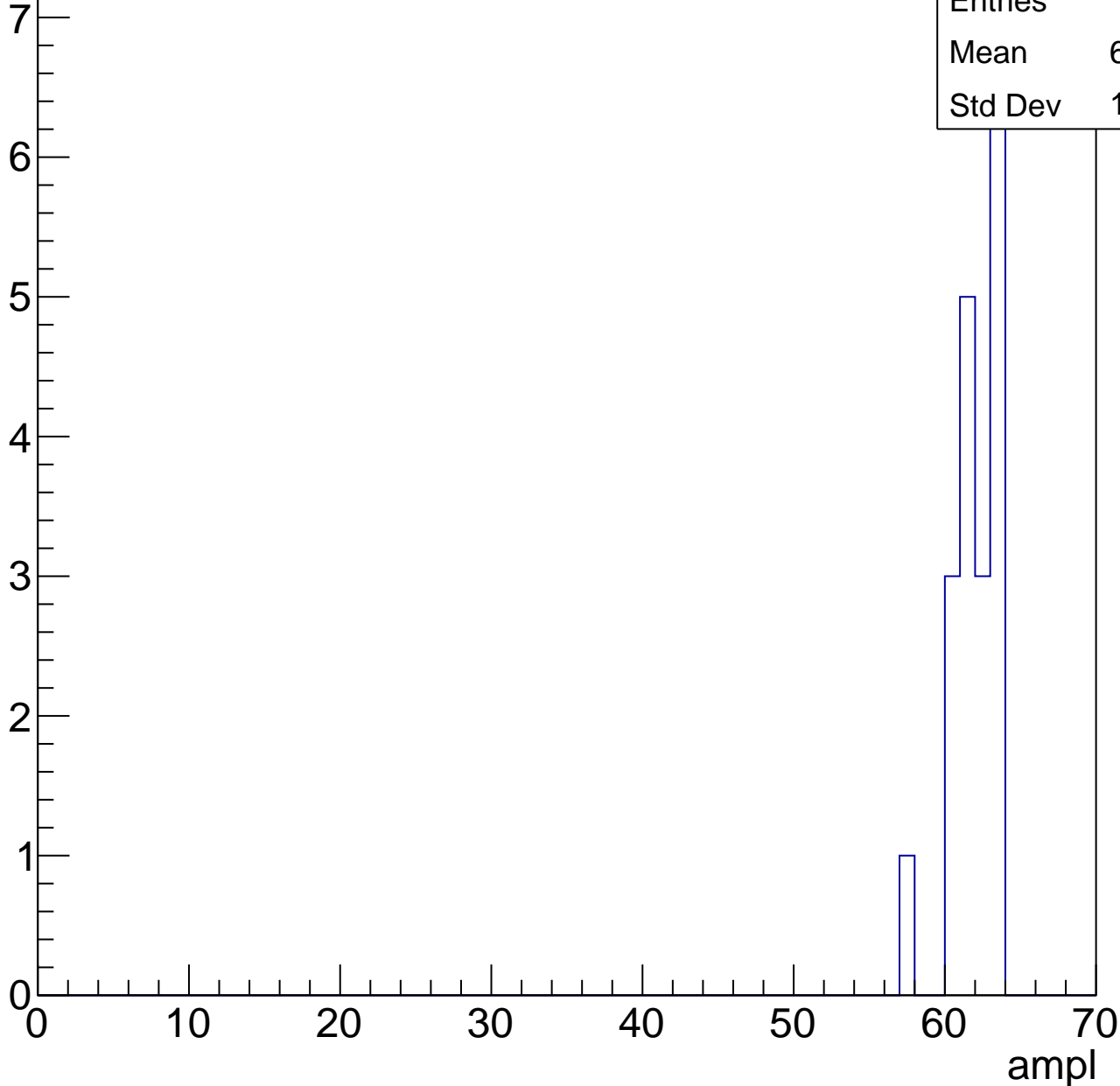


# B1L101S, U8-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	19
Mean	61.53
Std Dev	1.534





# B1L101S, U8-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



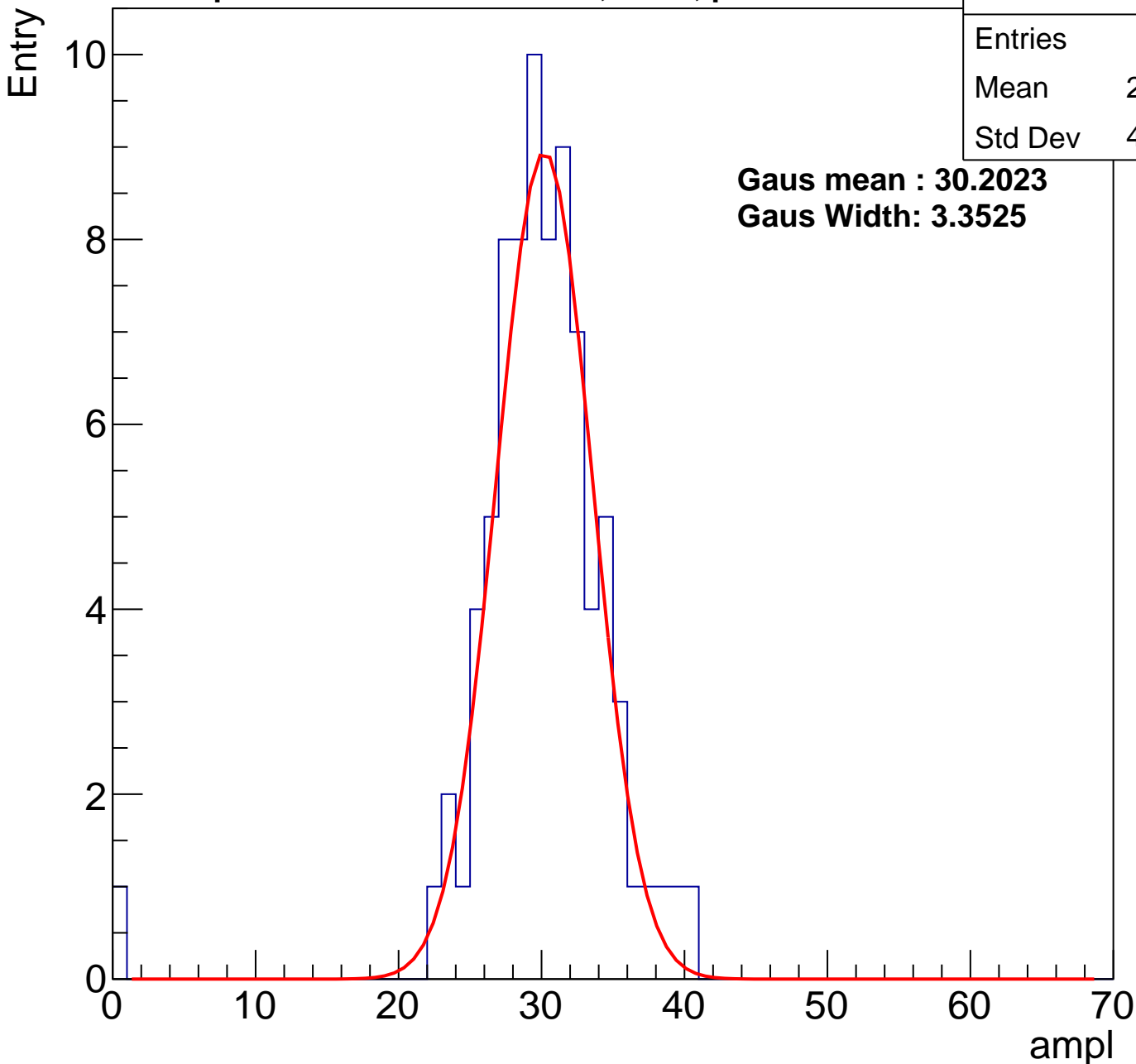
# B1L101S, U8-ch61, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	81
Mean	29.53
Std Dev	4.884

**Gaus mean : 30.2023**

**Gaus Width: 3.3525**



# B1L101S, U8-ch61, adc1

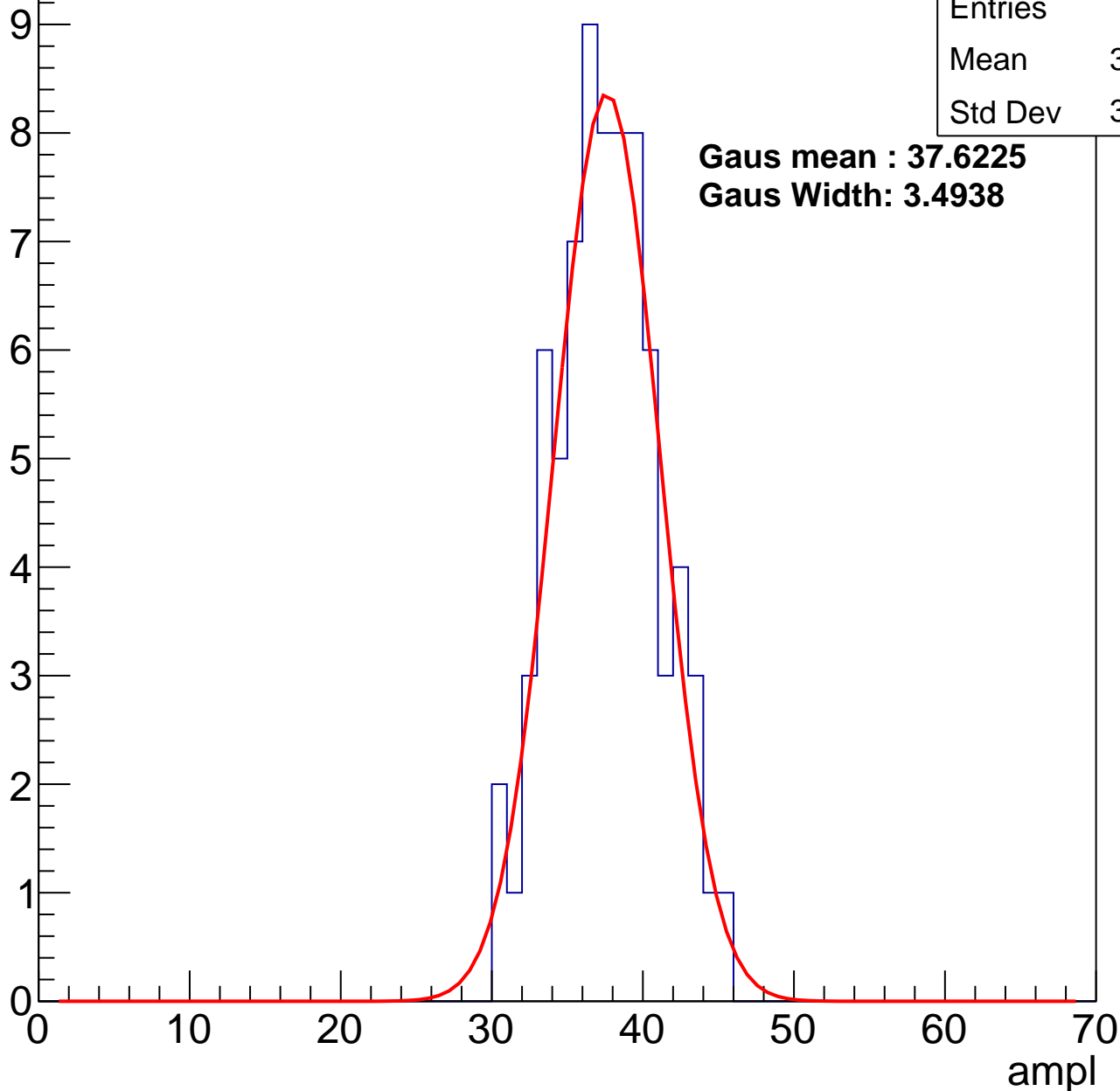
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	37.13
Std Dev	3.364

**Gaus mean : 37.6225**

**Gaus Width: 3.4938**



# B1L101S, U8-ch61, adc2

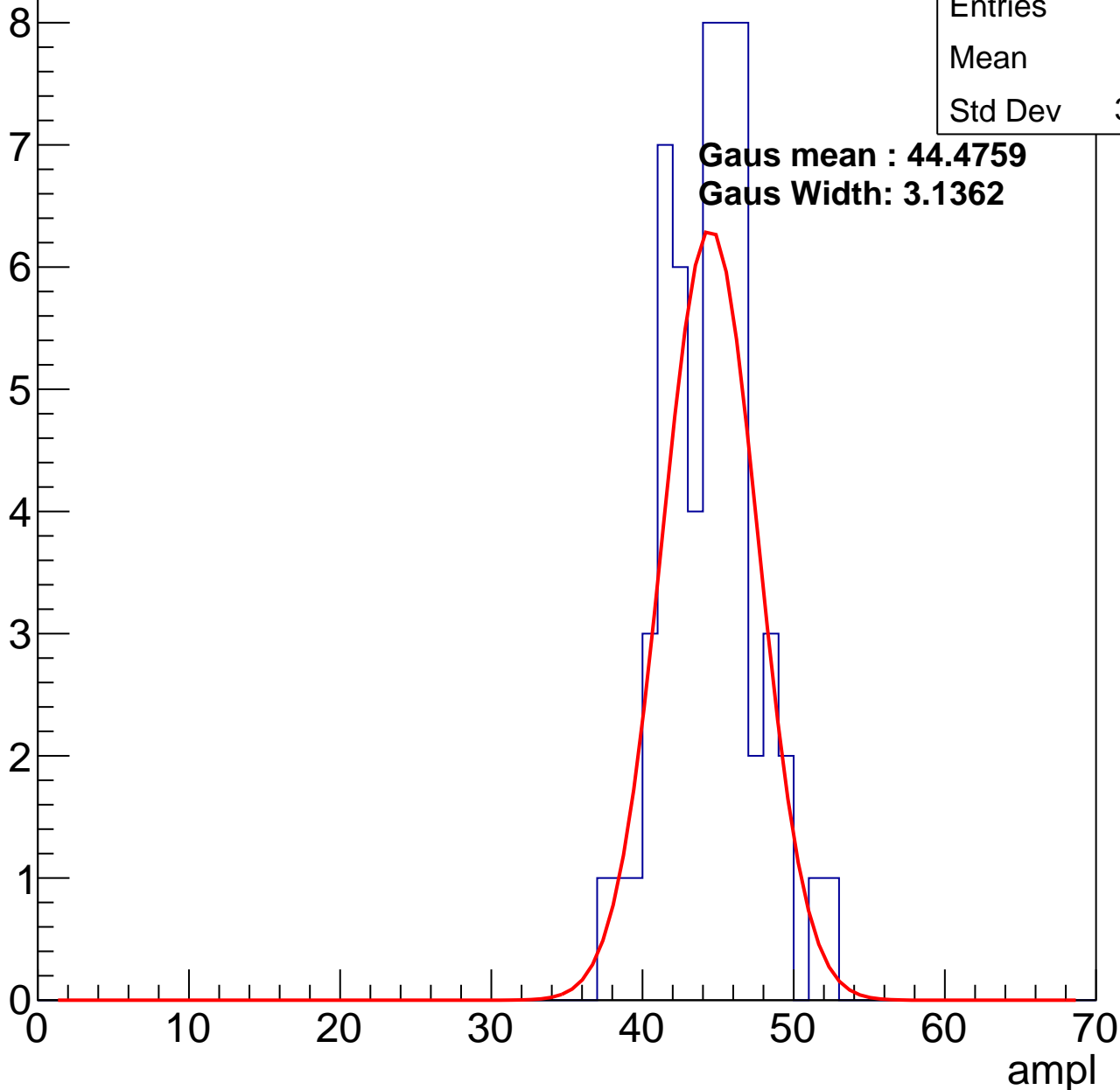
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	44
Std Dev	3.041

**Gaus mean : 44.4759**

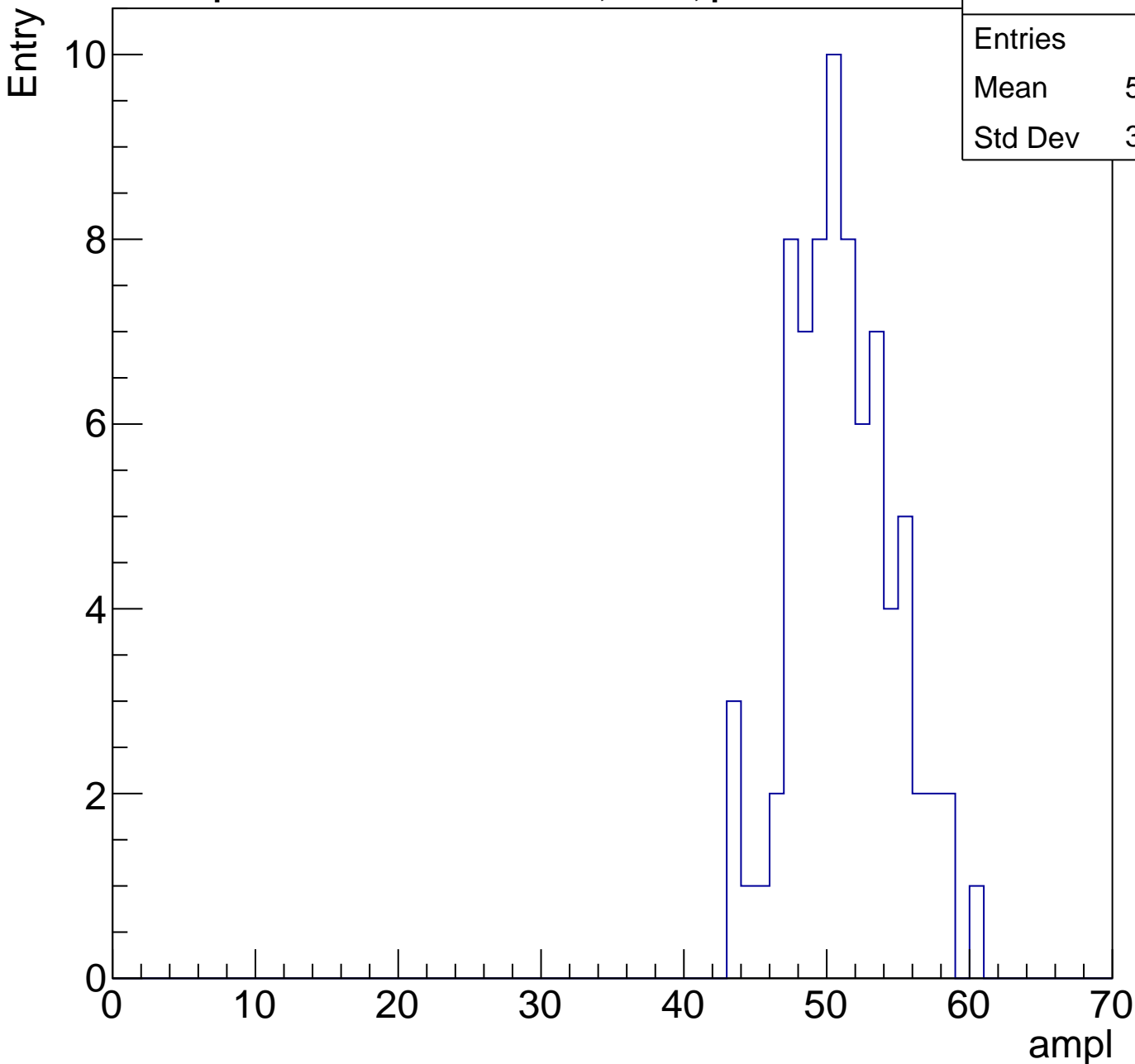
**Gaus Width: 3.1362**



# B1L101S, U8-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	77
Mean	50.62
Std Dev	3.604

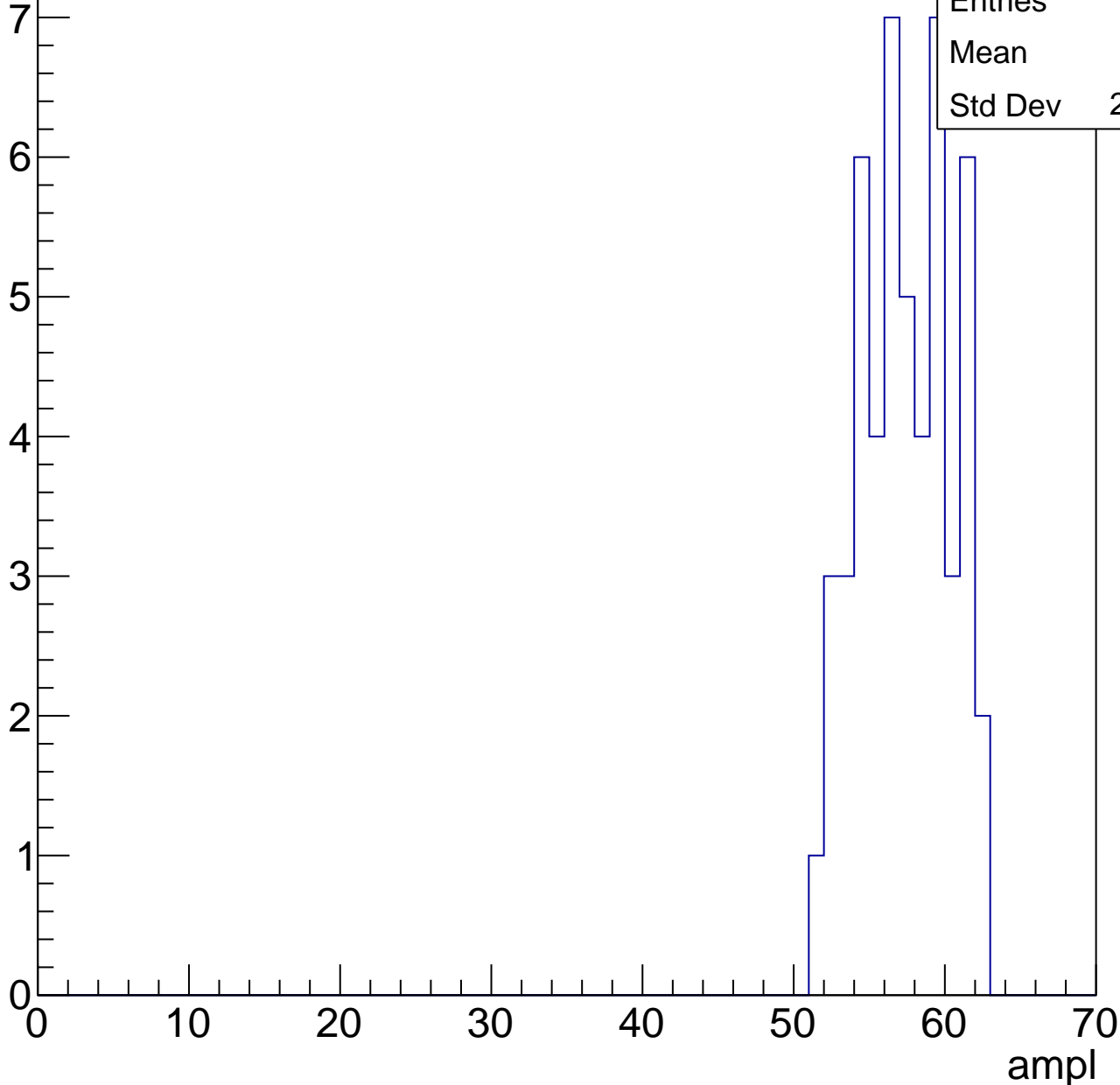


# B1L101S, U8-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	56.9
Std Dev	2.939

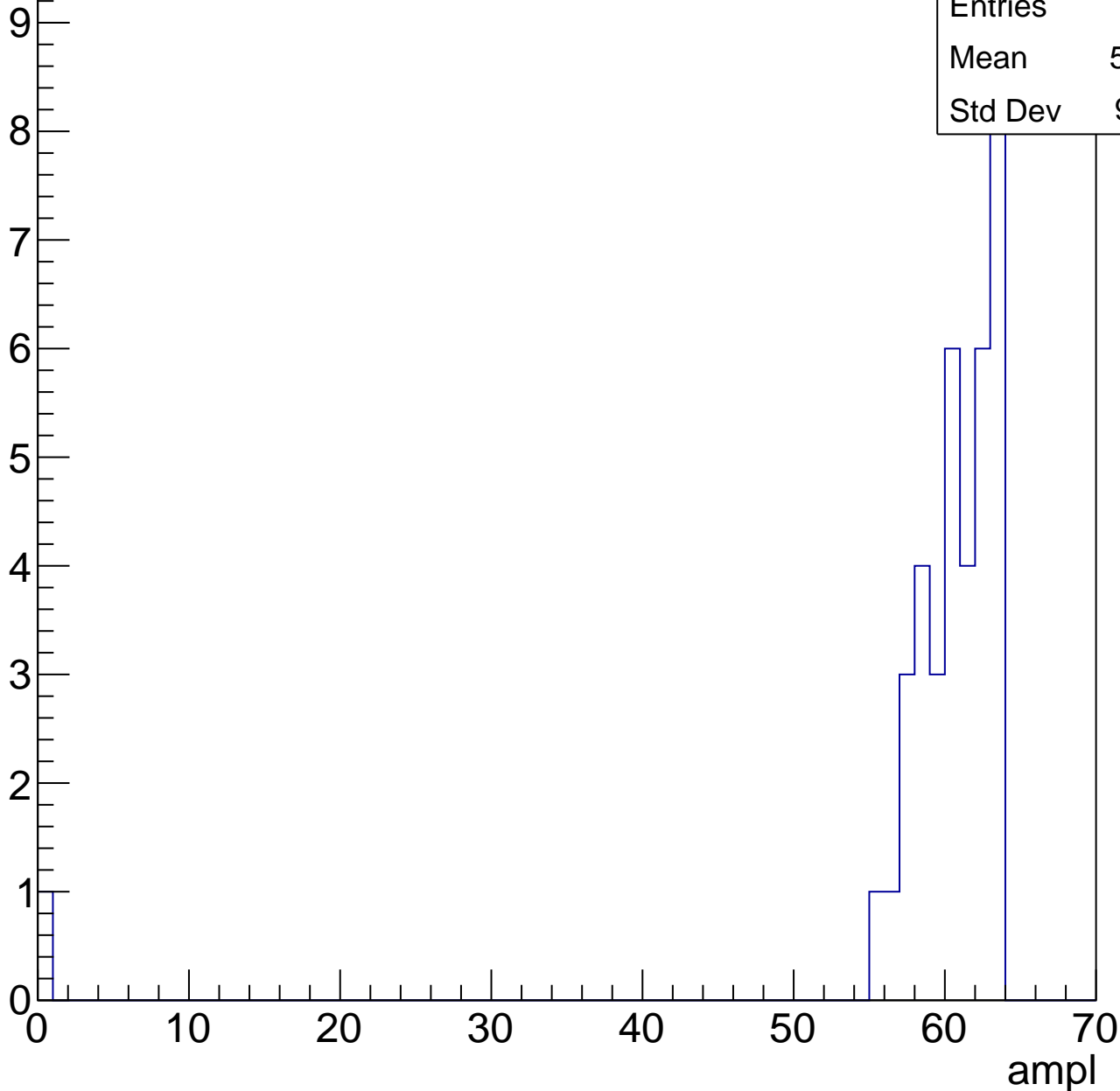


# B1L101S, U8-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	38
Mean	58.79
Std Dev	9.921



# B1L101S, U8-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U8-ch62, adc0

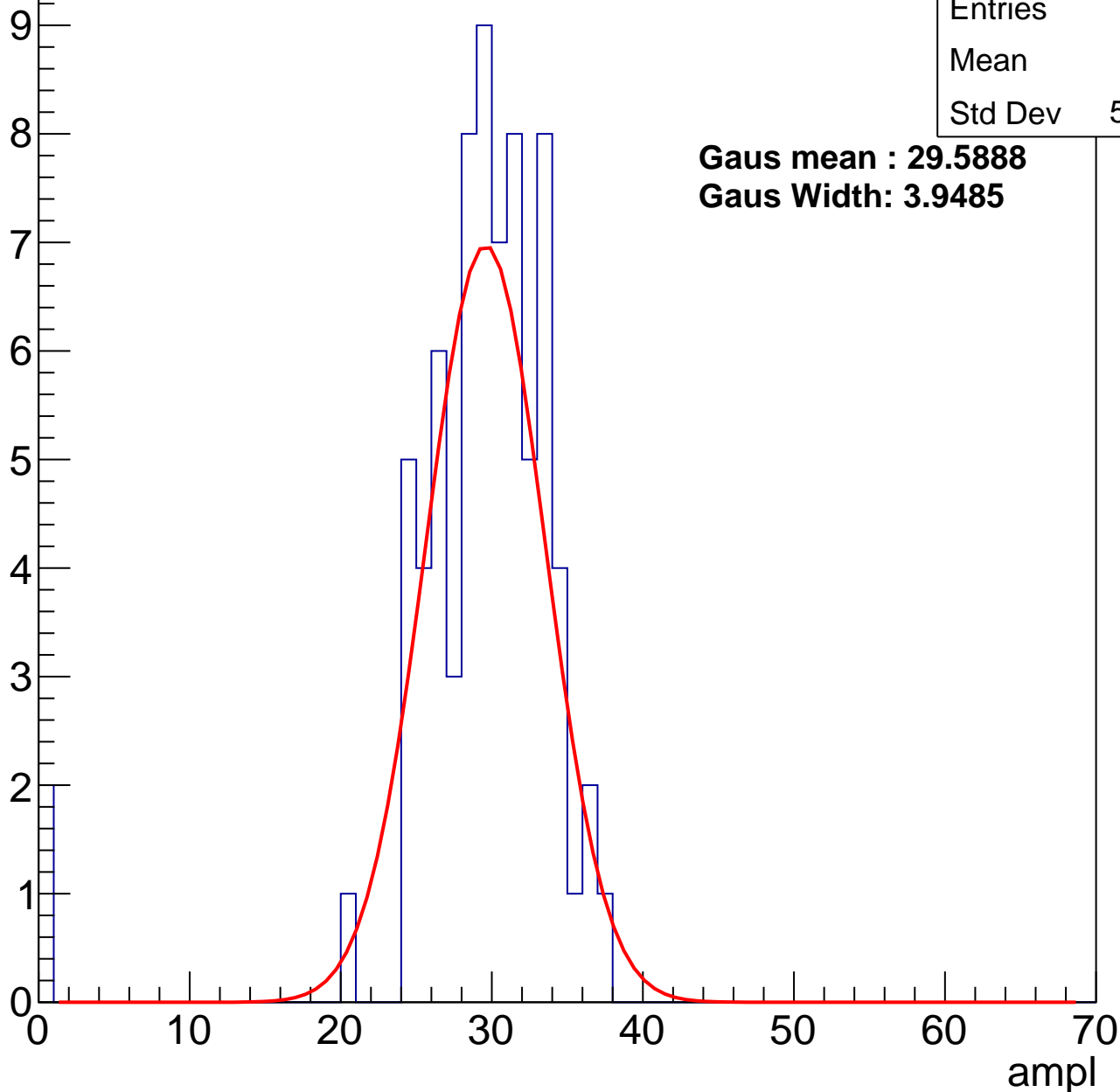
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	28.7
Std Dev	5.847

**Gaus mean : 29.5888**

**Gaus Width: 3.9485**



# B1L101S, U8-ch62, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	77
Mean	36.56
Std Dev	3.573

**Gaus mean : 37.1328**

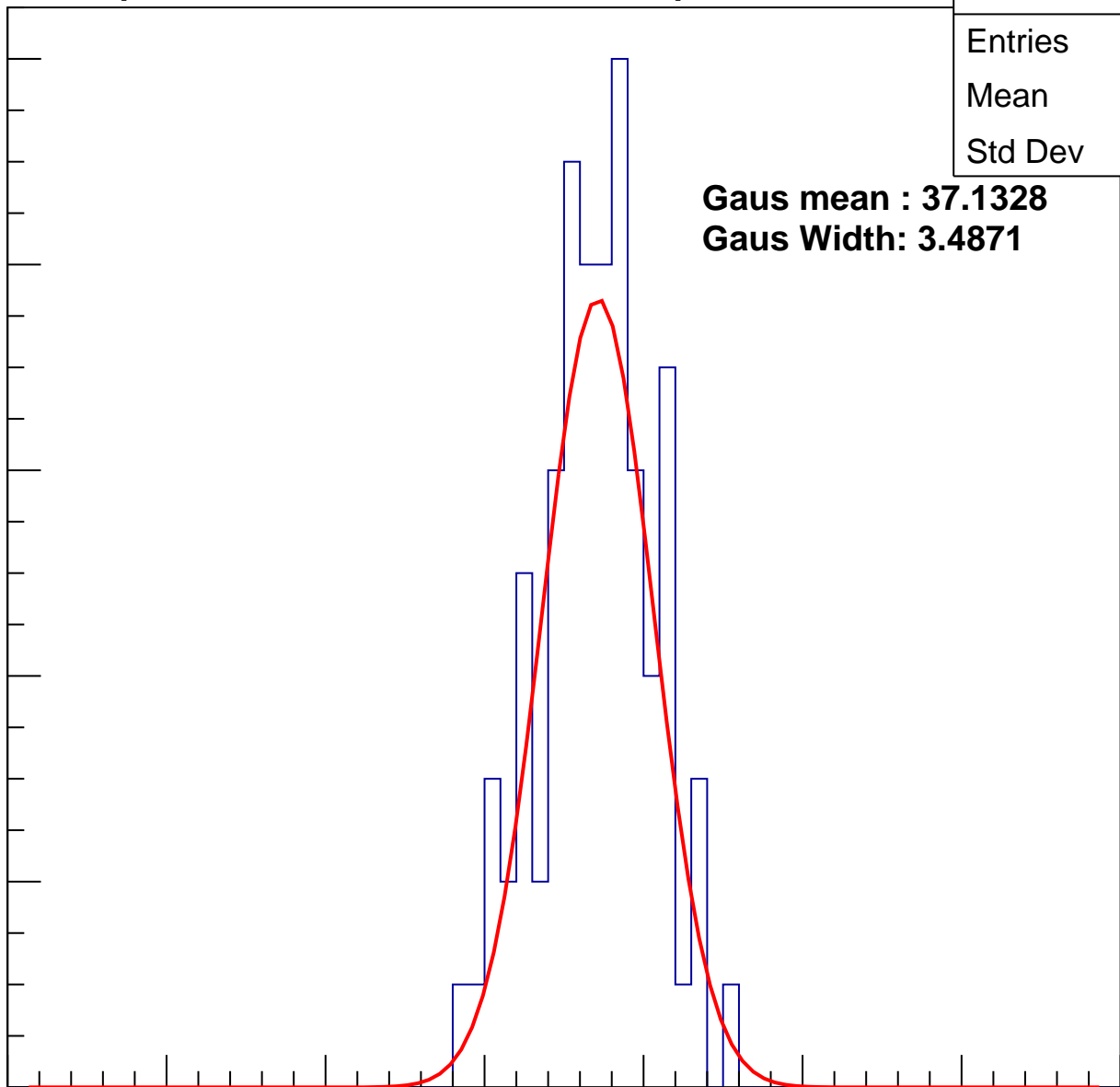
**Gaus Width: 3.4871**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U8-ch62, adc2

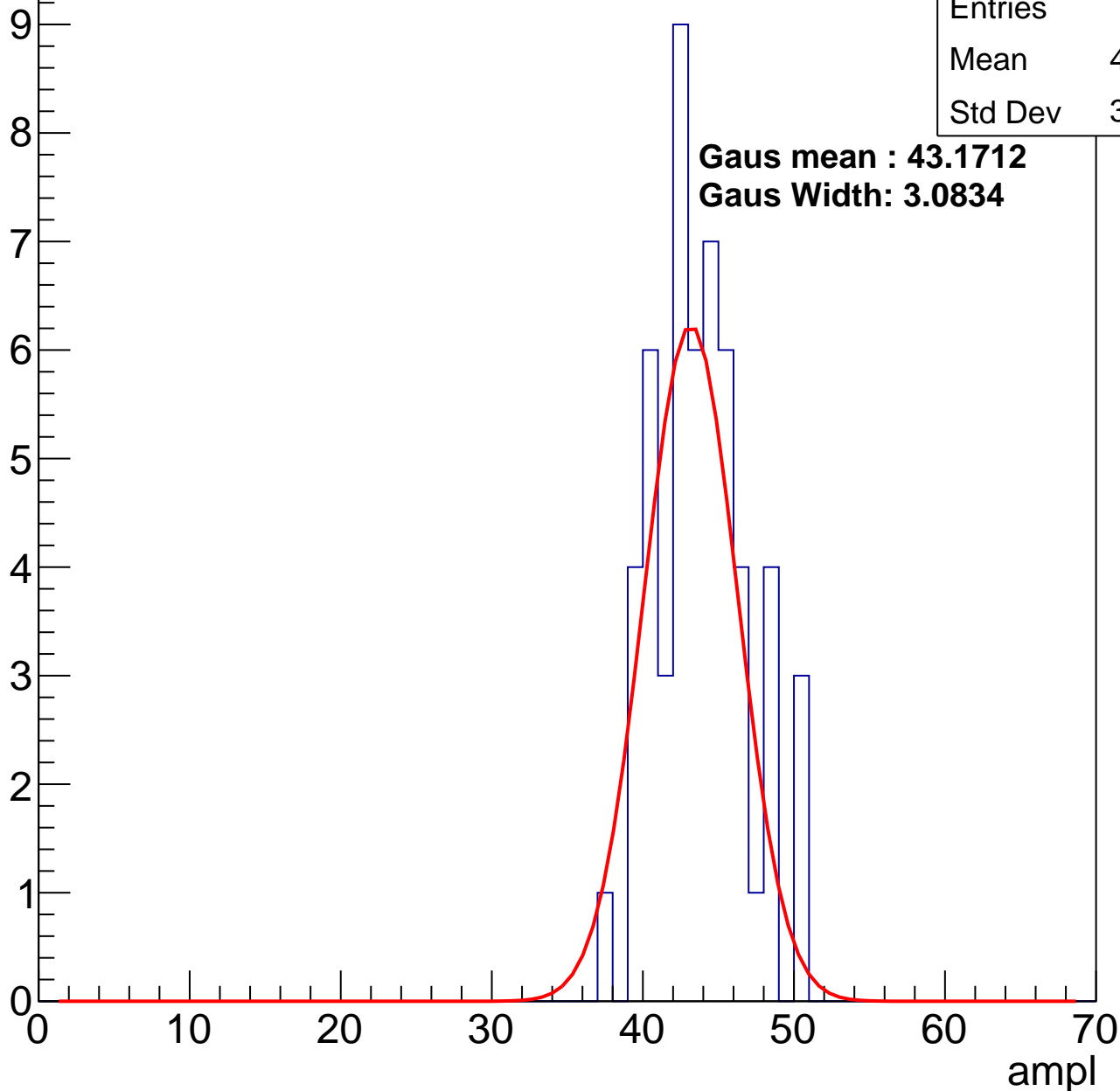
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	43.39
Std Dev	3.033

**Gaus mean : 43.1712**

**Gaus Width: 3.0834**

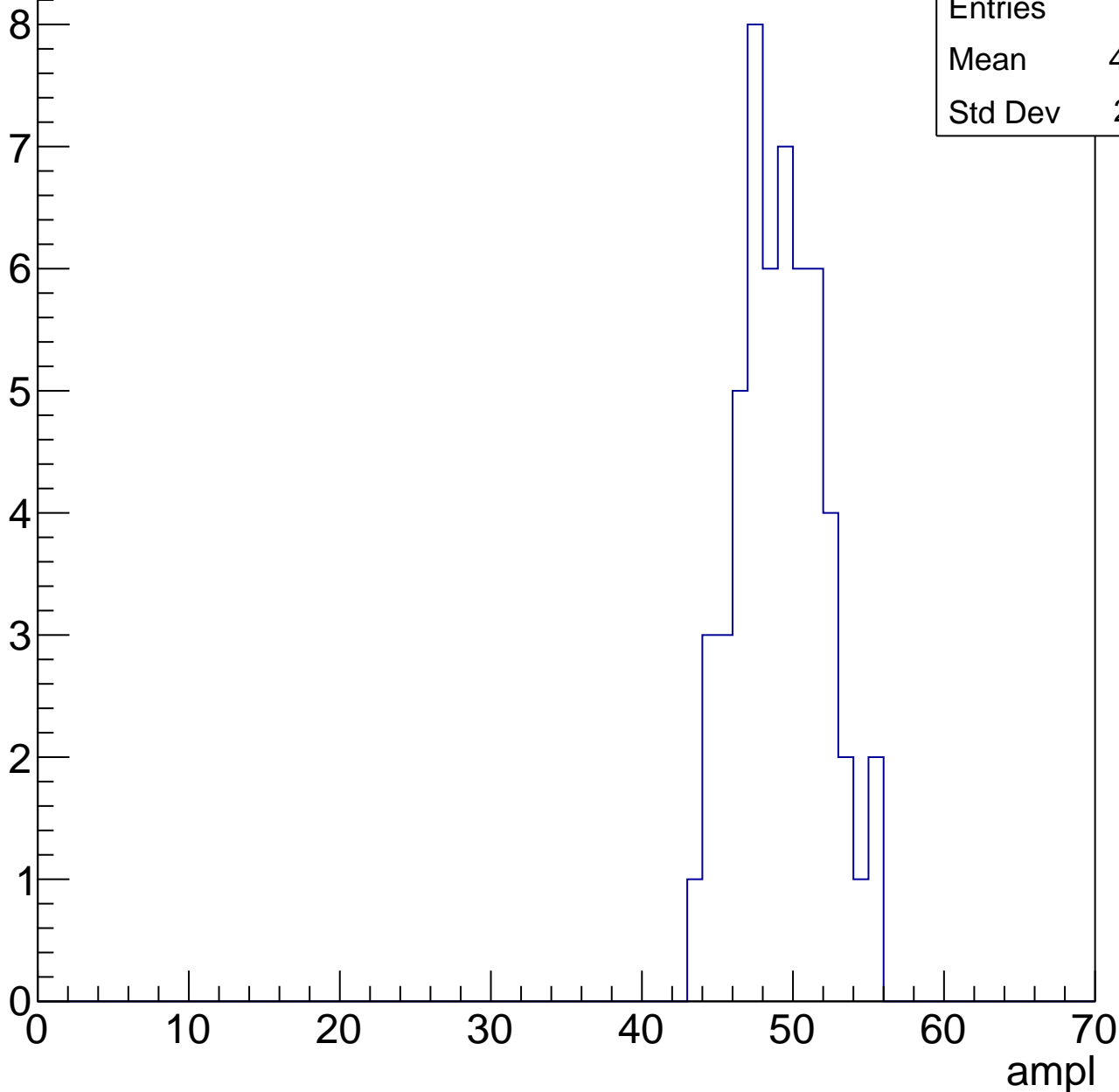


# B1L101S, U8-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	48.72
Std Dev	2.831

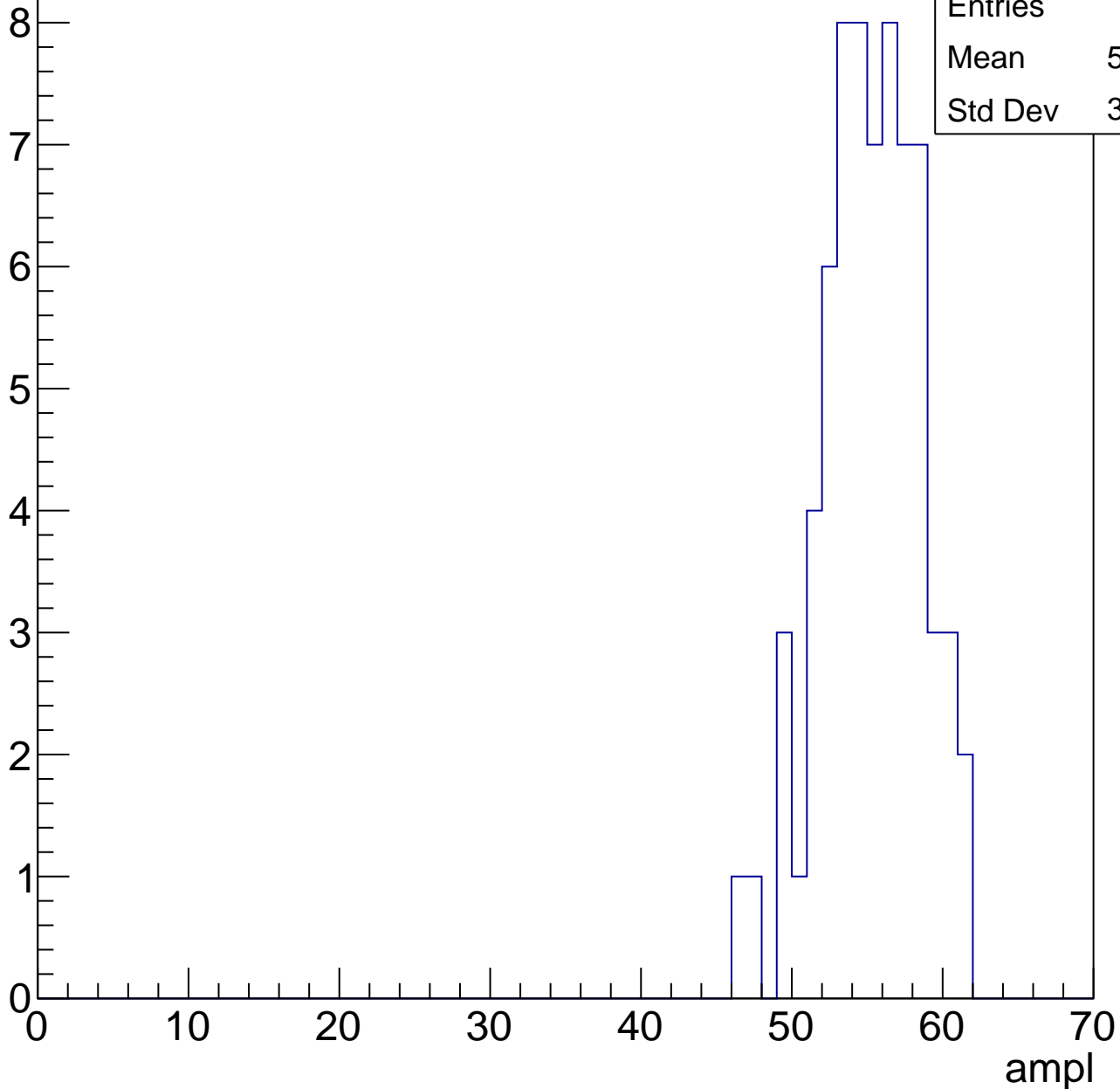


# B1L101S, U8-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	54.77
Std Dev	3.244



# B1L101S, U8-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	58.92
Std Dev	8.799

ampl

0

10

20

30

40

50

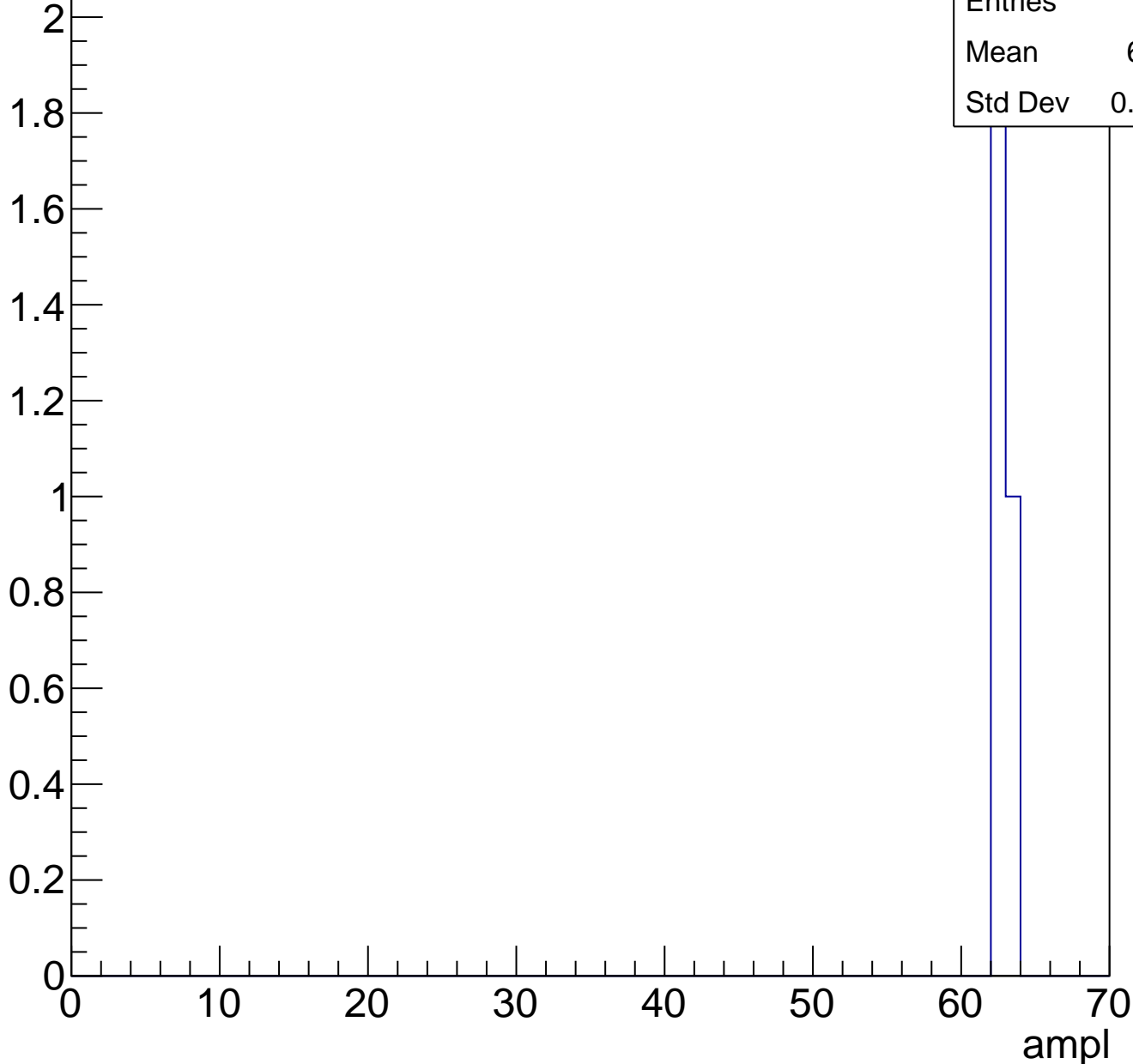
60

70

# B1L101S, U8-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

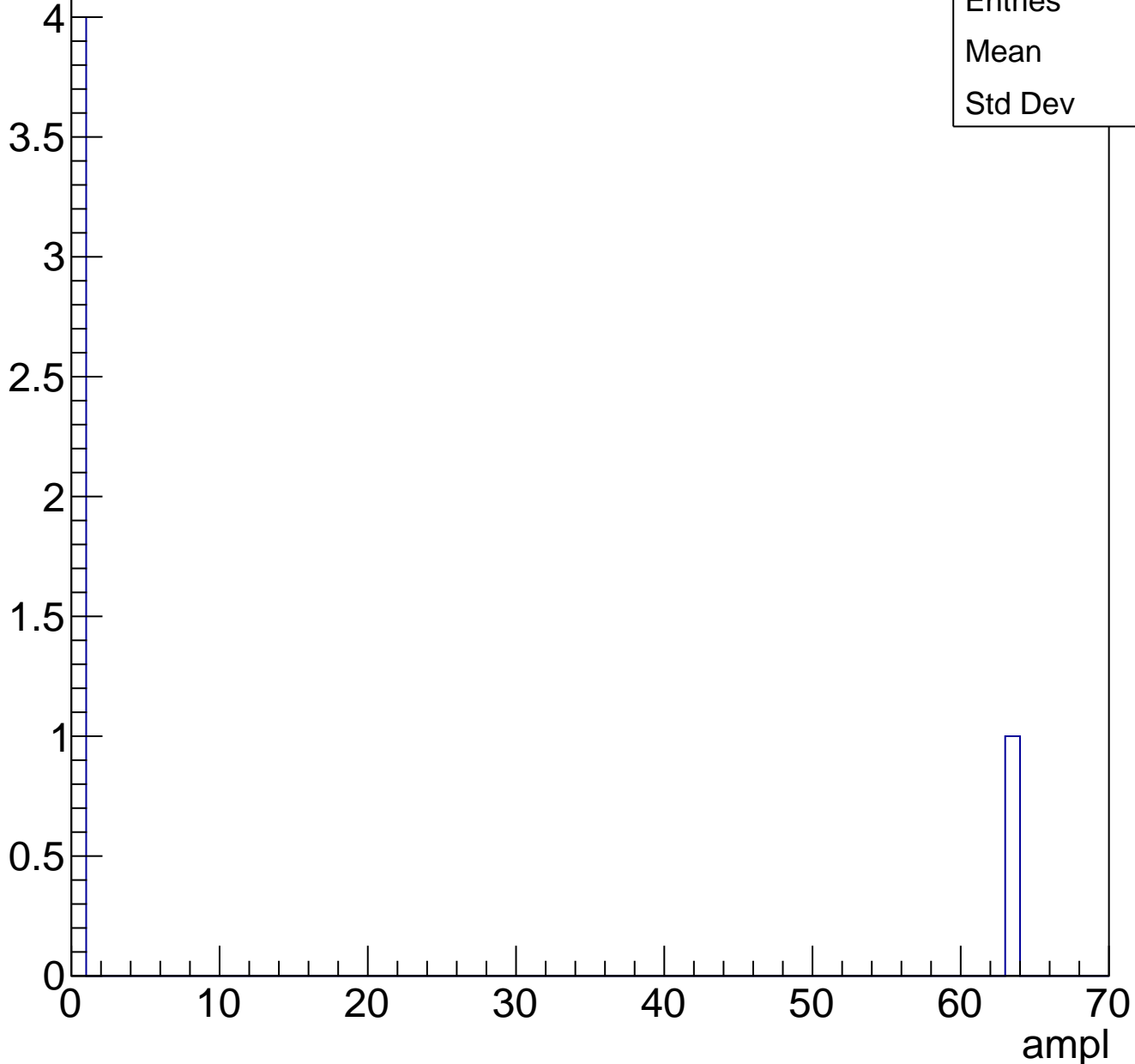




# B1L101S, U8-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch63, adc0

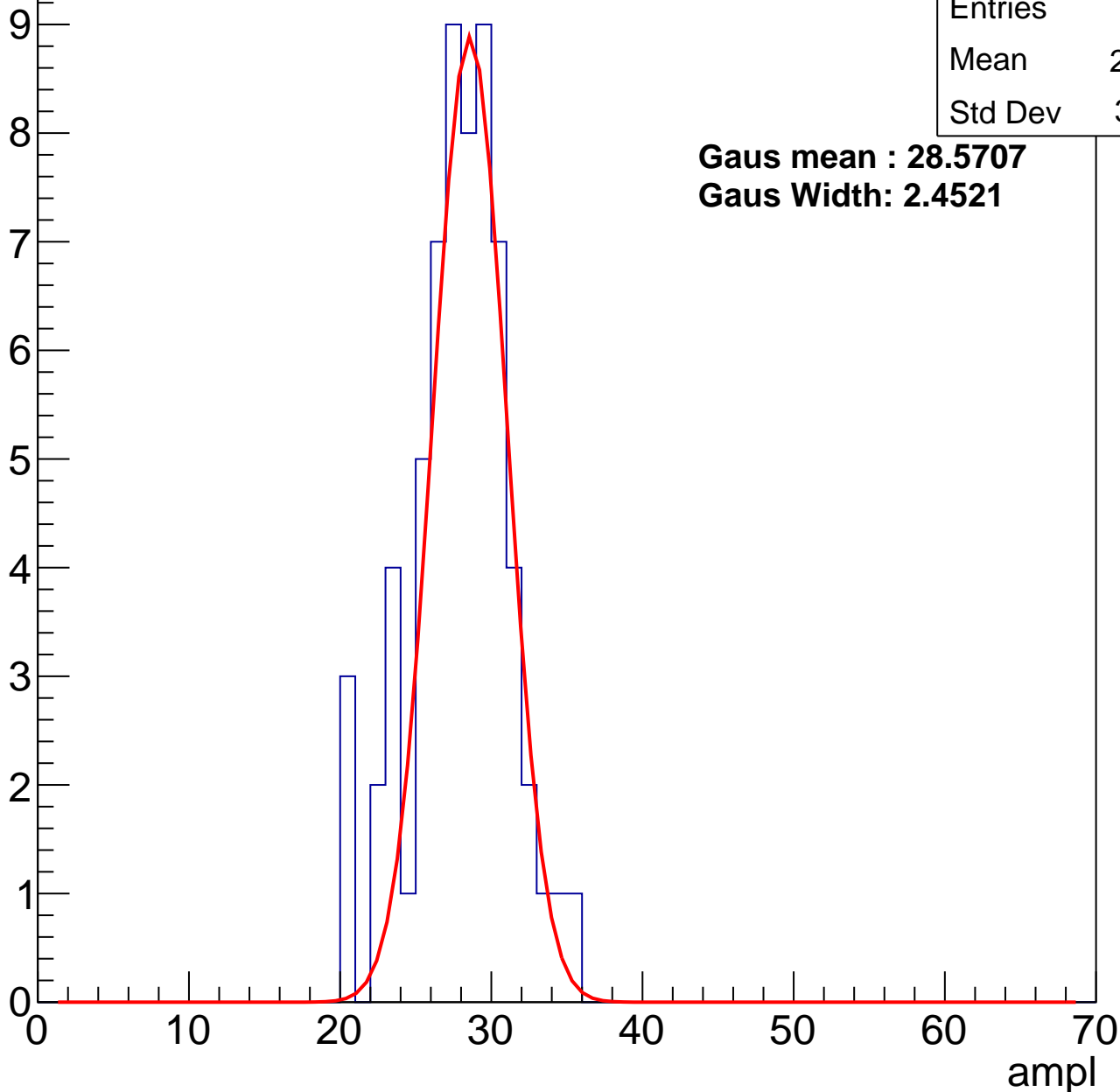
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	27.42
Std Dev	3.201

**Gaus mean : 28.5707**

**Gaus Width: 2.4521**



# B1L101S, U8-ch63, adc1

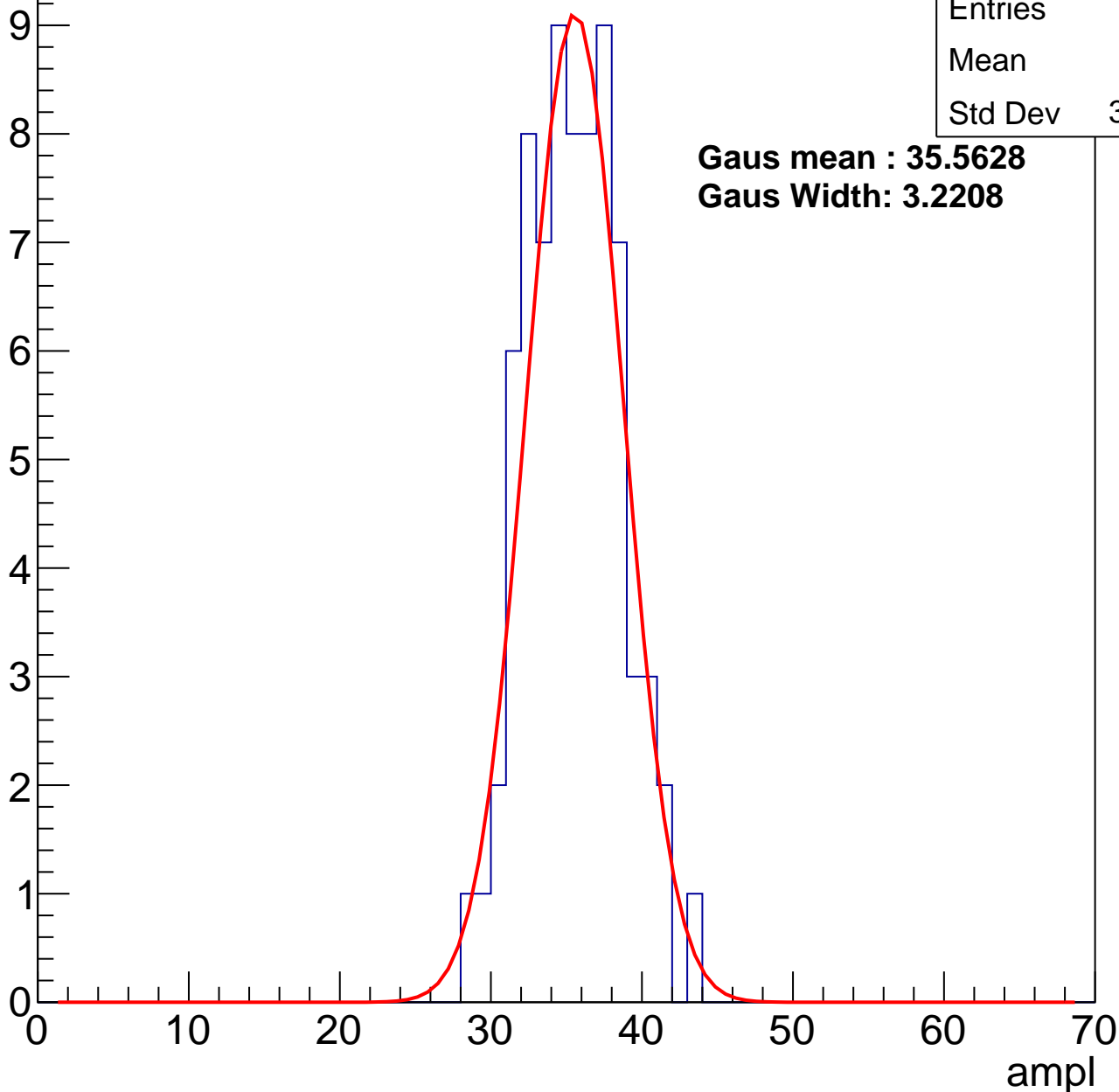
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	35
Std Dev	3.068

**Gaus mean : 35.5628**

**Gaus Width: 3.2208**



# B1L101S, U8-ch63, adc2

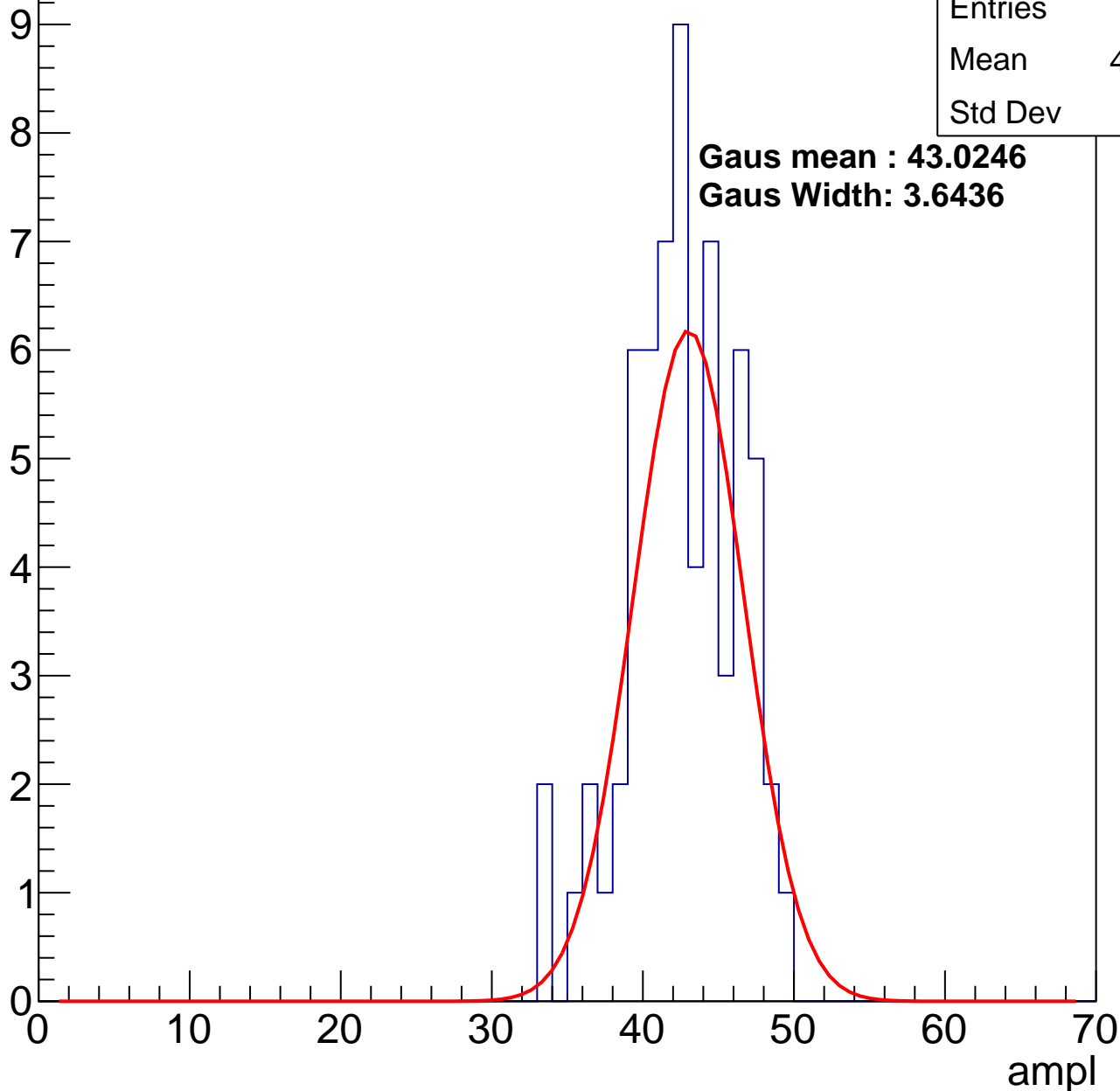
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	42.12
Std Dev	3.59

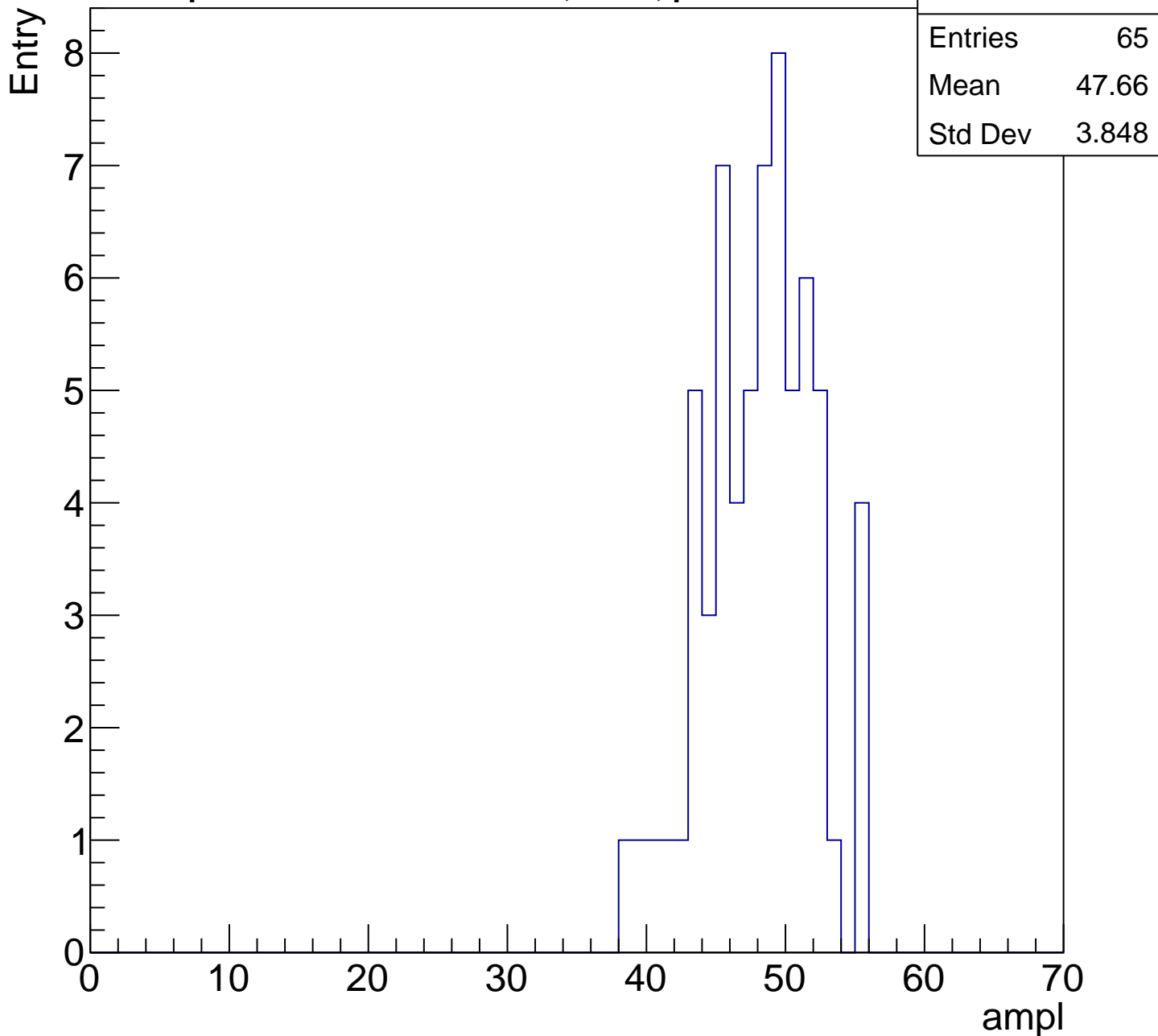
**Gaus mean : 43.0246**

**Gaus Width: 3.6436**



# B1L101S, U8-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

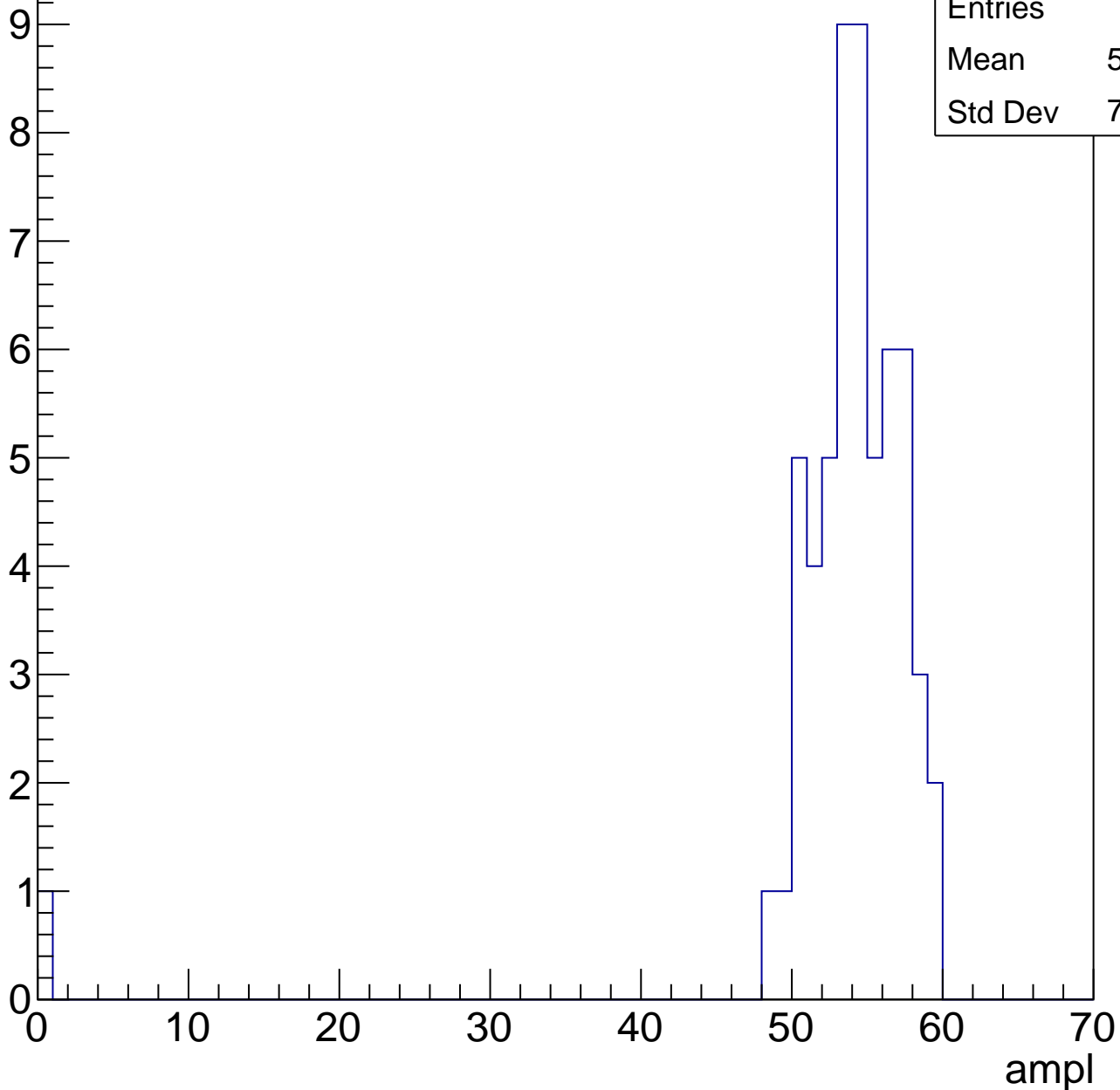


# B1L101S, U8-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	52.96
Std Dev	7.542



# B1L101S, U8-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

Entries	57
Mean	59.63
Std Dev	2.182

0

2

4

6

8

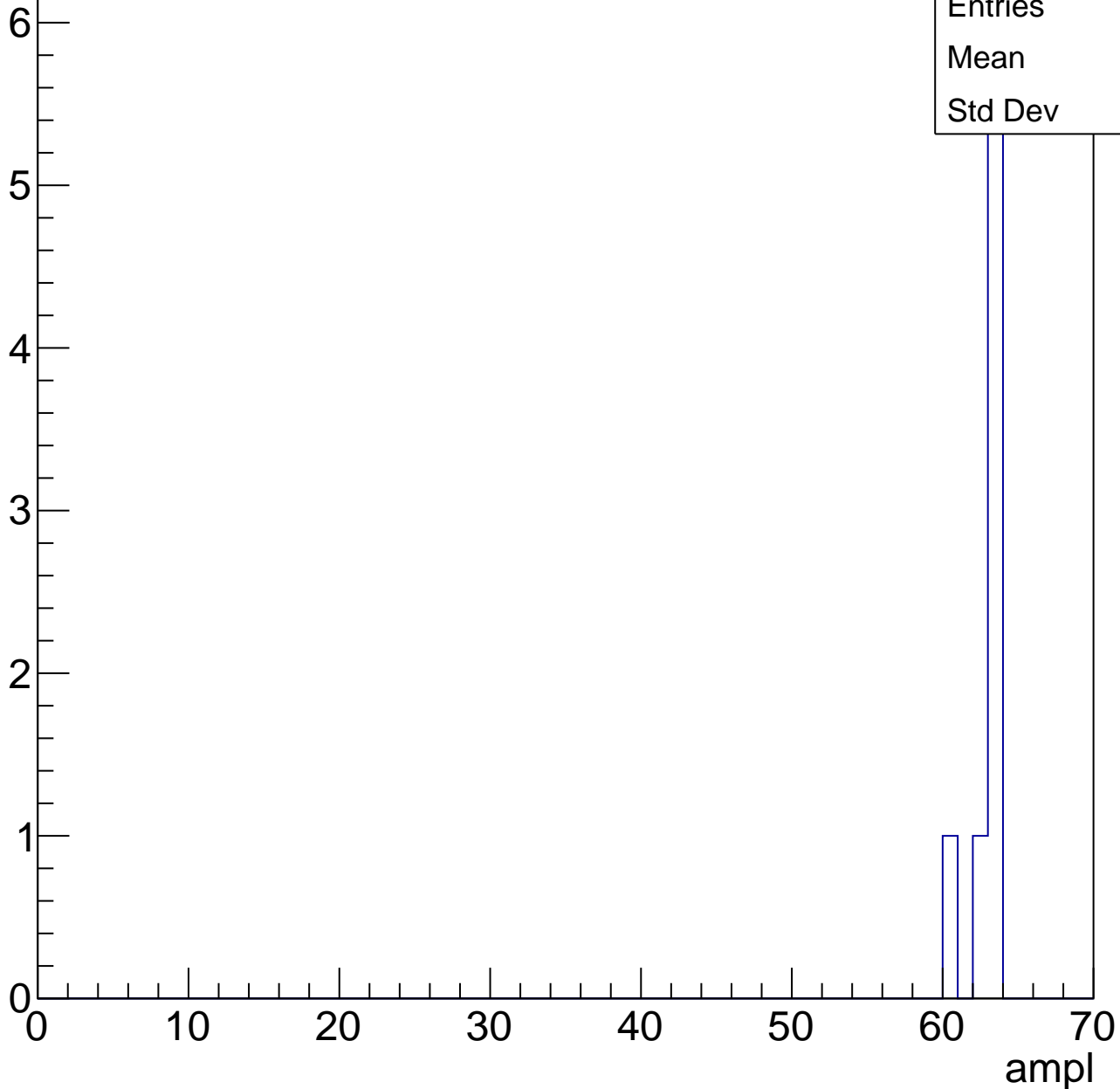
10

# B1L101S, U8-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	8
Mean	62.5
Std Dev	1

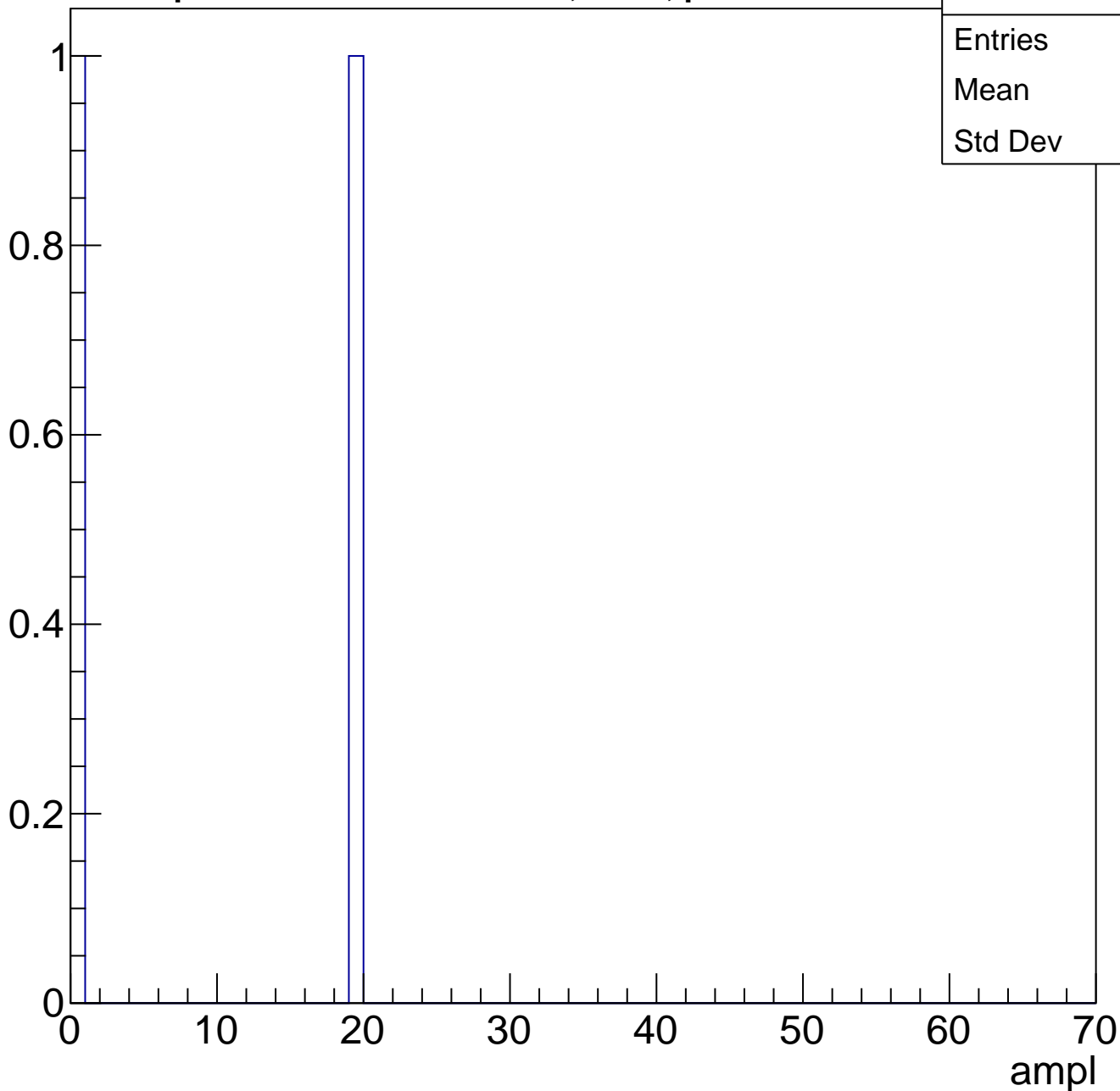




# B1L101S, U8-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	9.5
Std Dev	9.5

# B1L101S, U8-ch64, adc0

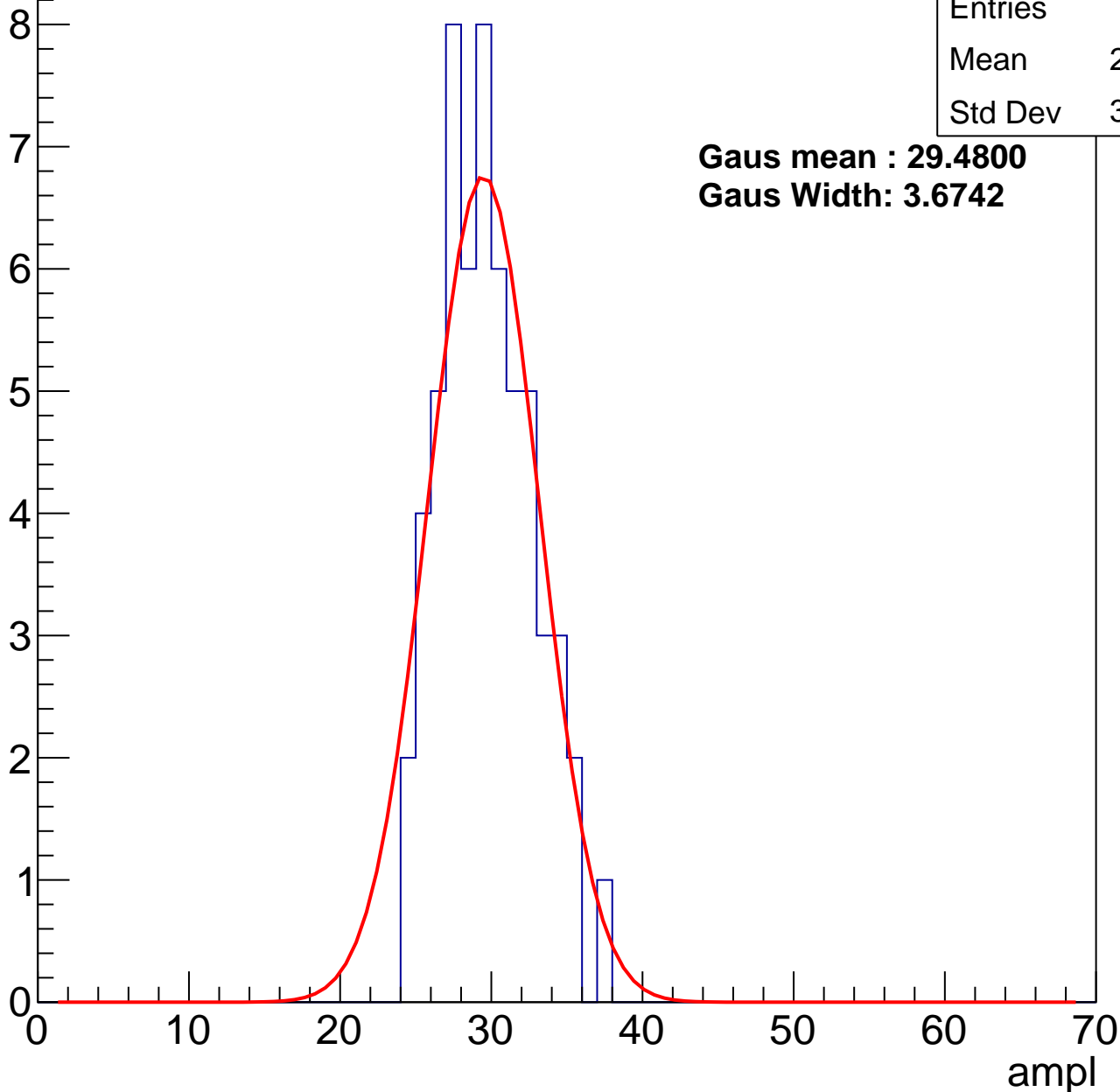
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	29.26
Std Dev	3.003

**Gaus mean : 29.4800**

**Gaus Width: 3.6742**



# B1L101S, U8-ch64, adc1

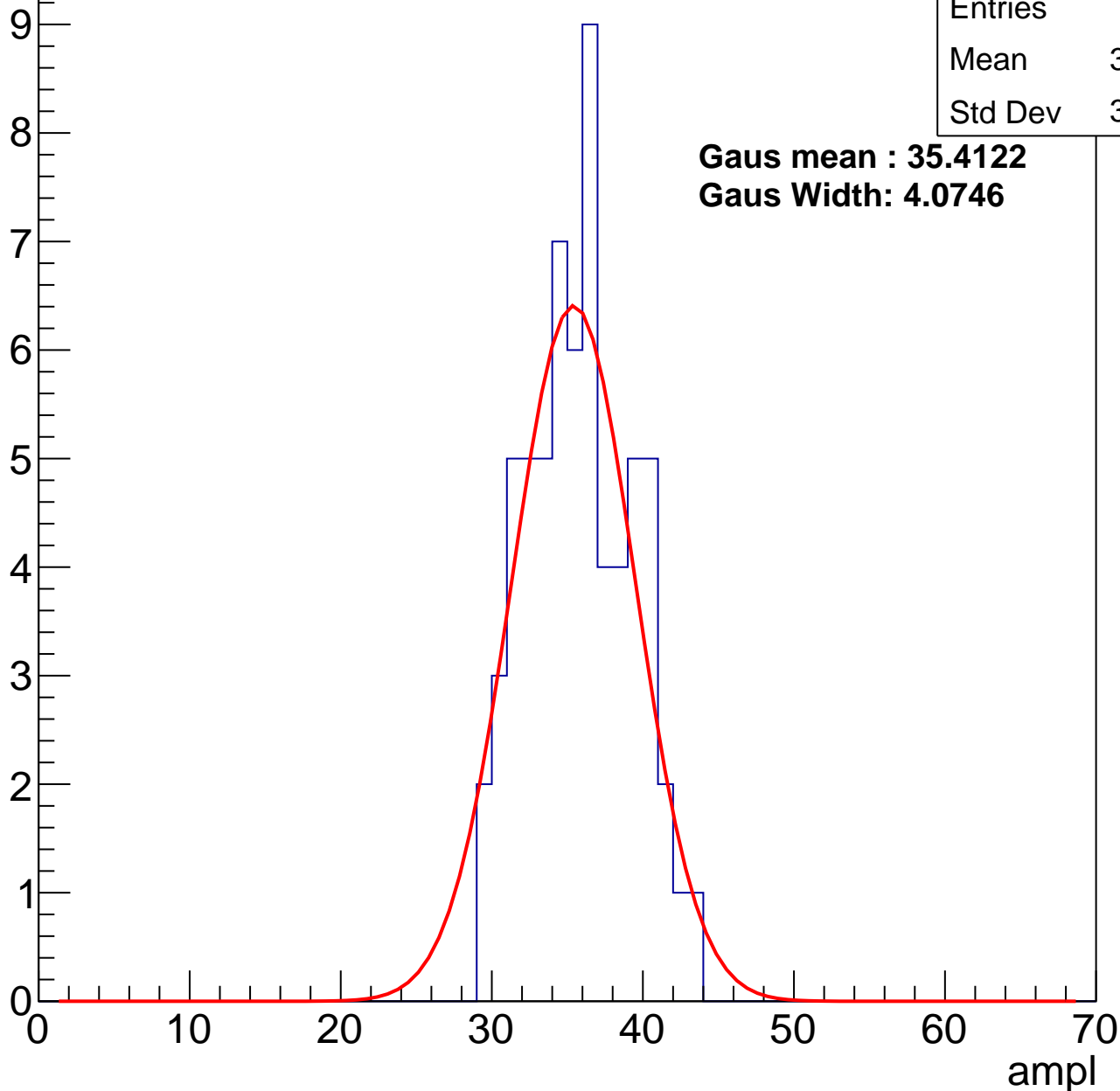
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	35.34
Std Dev	3.406

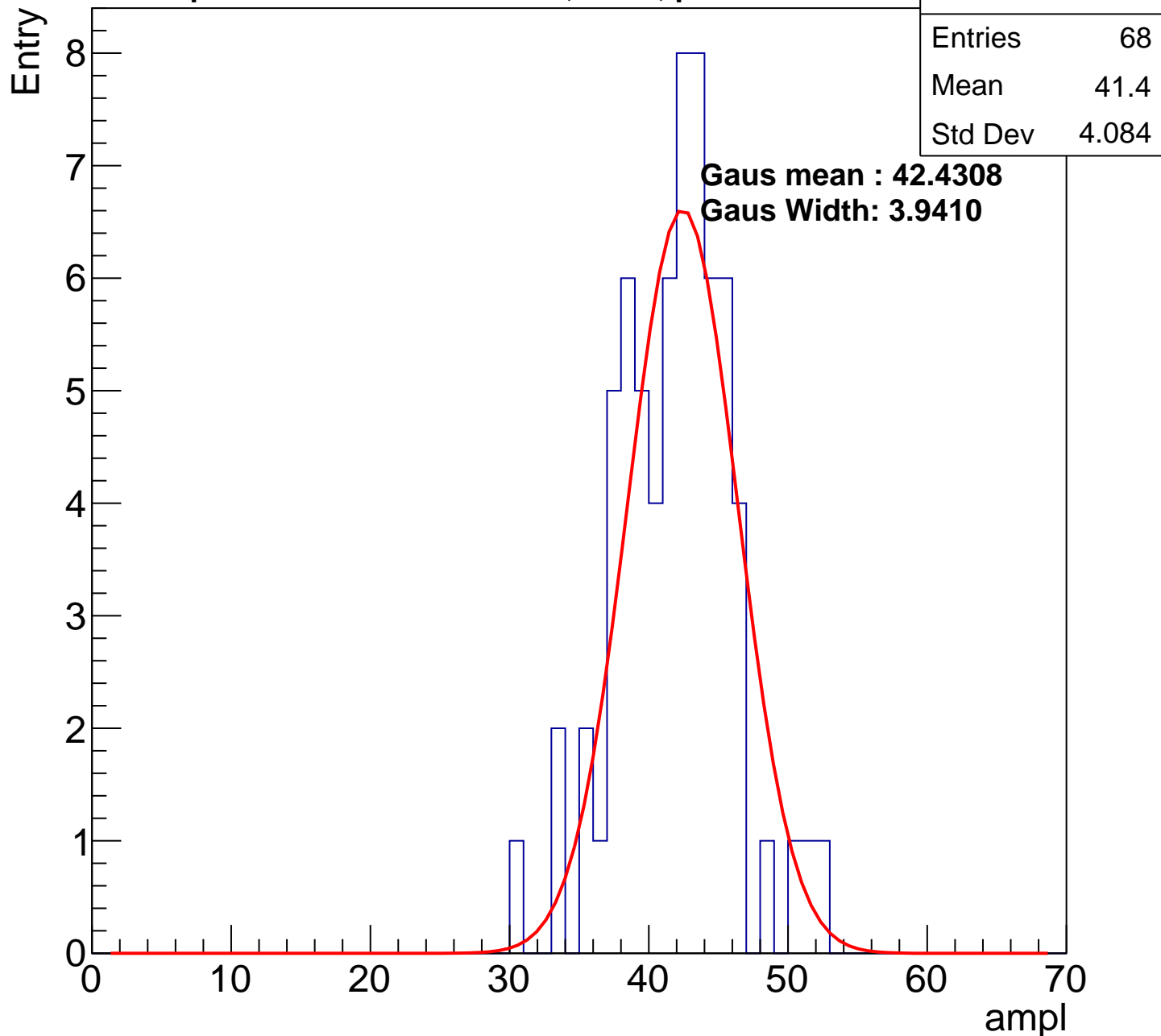
**Gaus mean : 35.4122**

**Gaus Width: 4.0746**



# B1L101S, U8-ch64, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U8-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

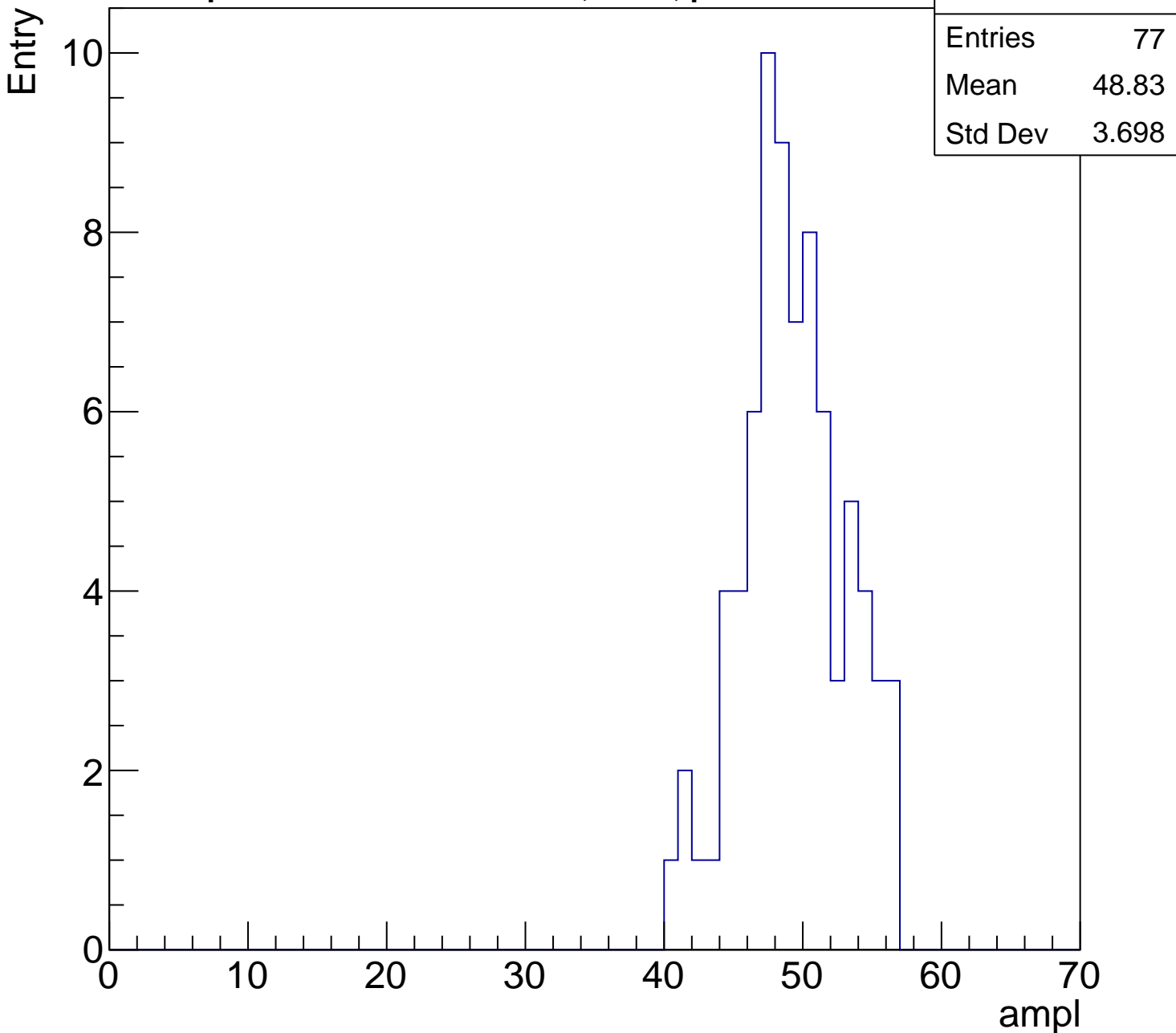
Entries	77
Mean	48.83
Std Dev	3.698

Entry

10  
8  
6  
4  
2  
0

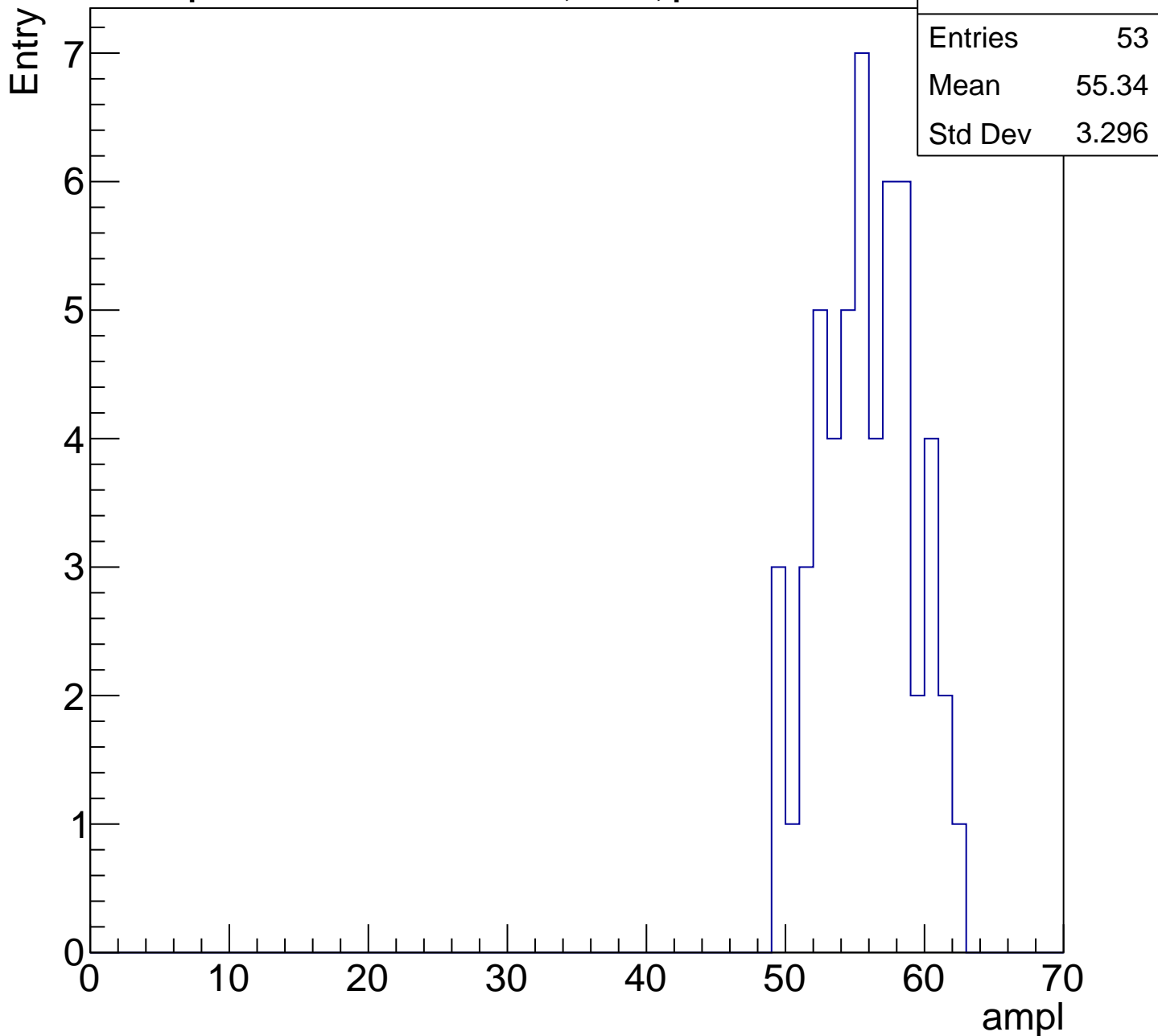
0 10 20 30 40 50 60 70

ampl



# B1L101S, U8-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U8-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	44
Mean	58.07
Std Dev	9.272

ampl

0 10 20 30 40 50 60 70

1

2

3

4

5

6

7

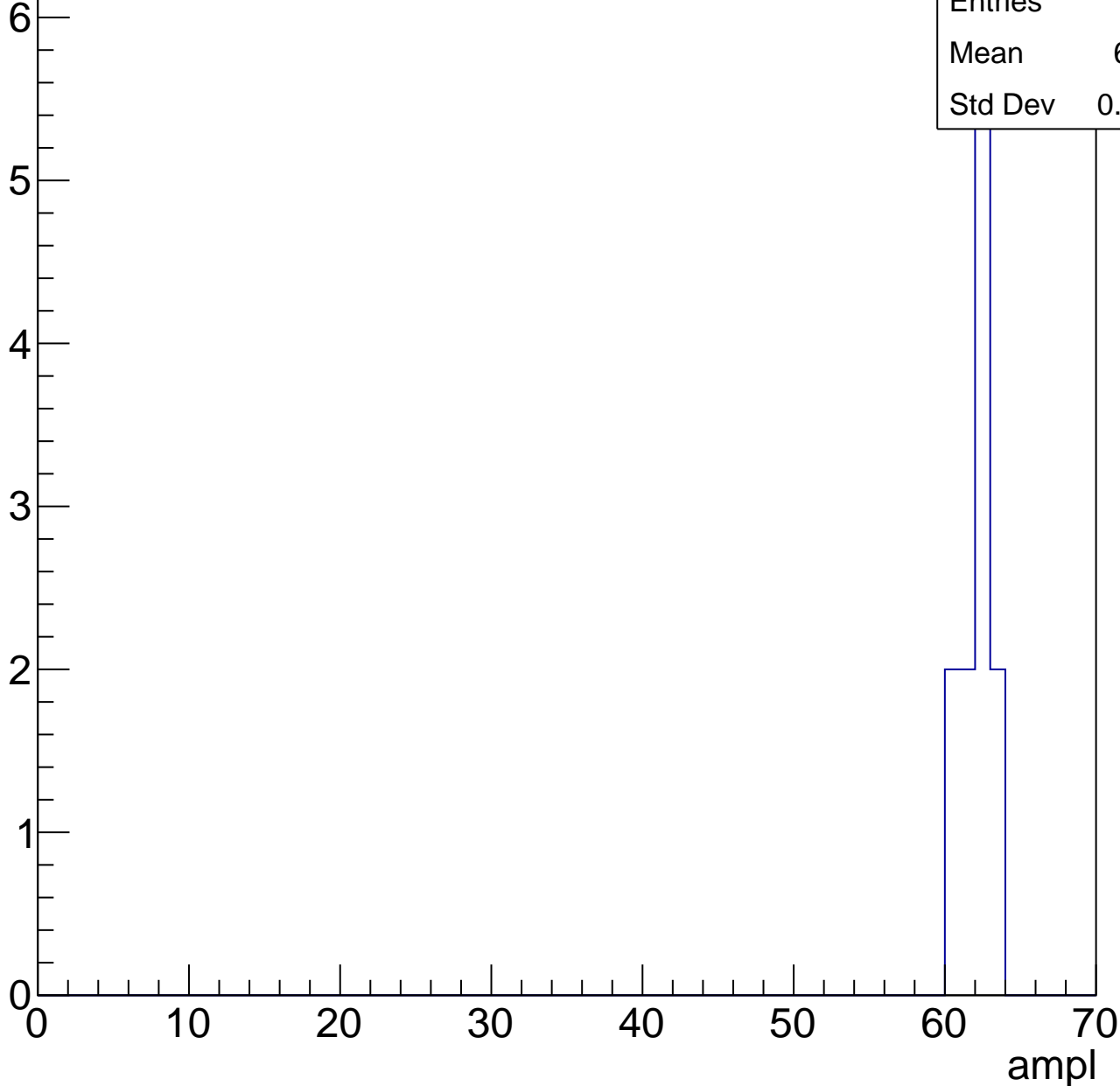
8

# B1L101S, U8-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	12
Mean	61.67
Std Dev	0.9428





# B1L101S, U8-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U8-ch65, adc0

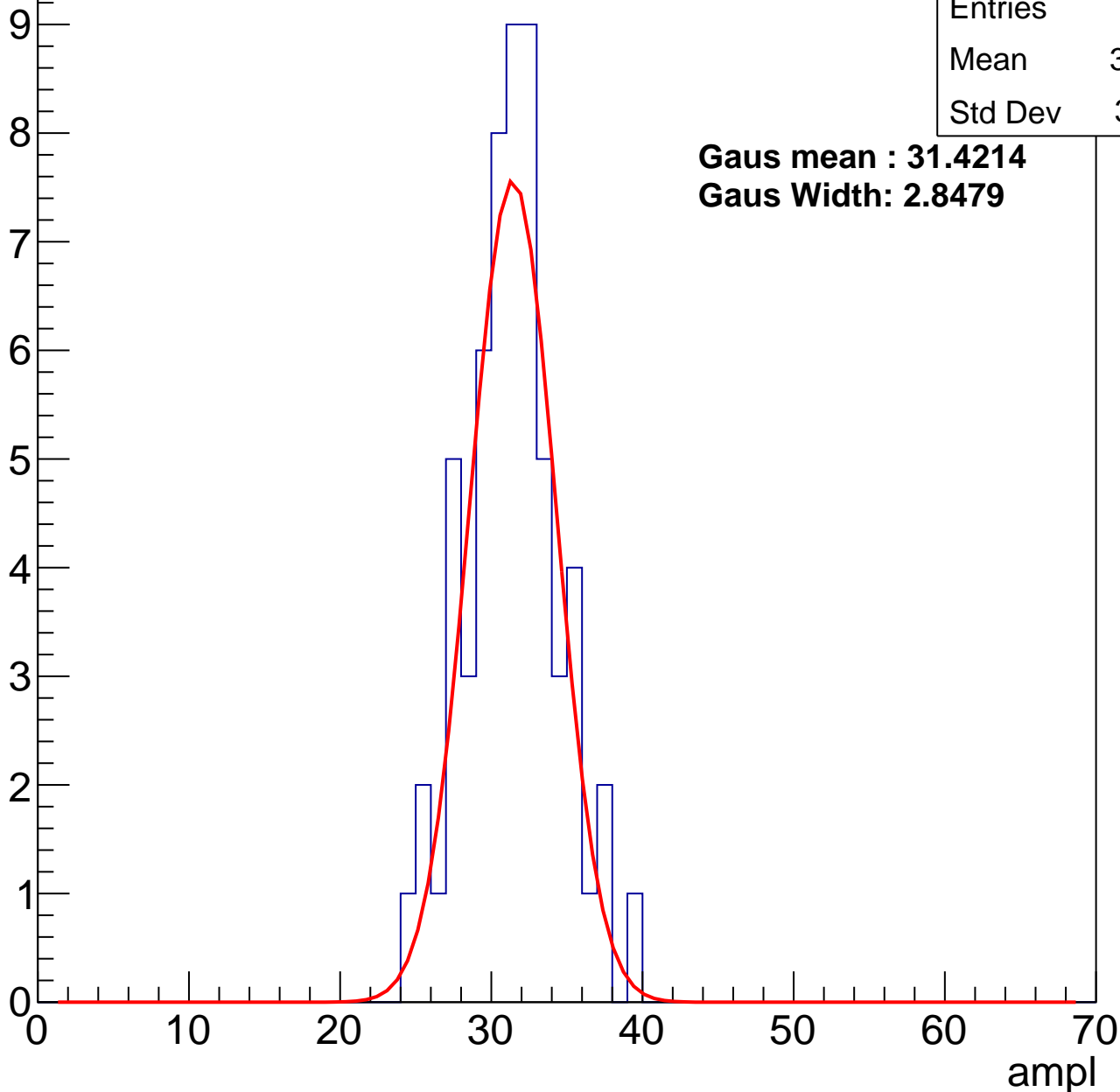
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	30.93
Std Dev	3.071

**Gaus mean : 31.4214**

**Gaus Width: 2.8479**



# B1L101S, U8-ch65, adc1

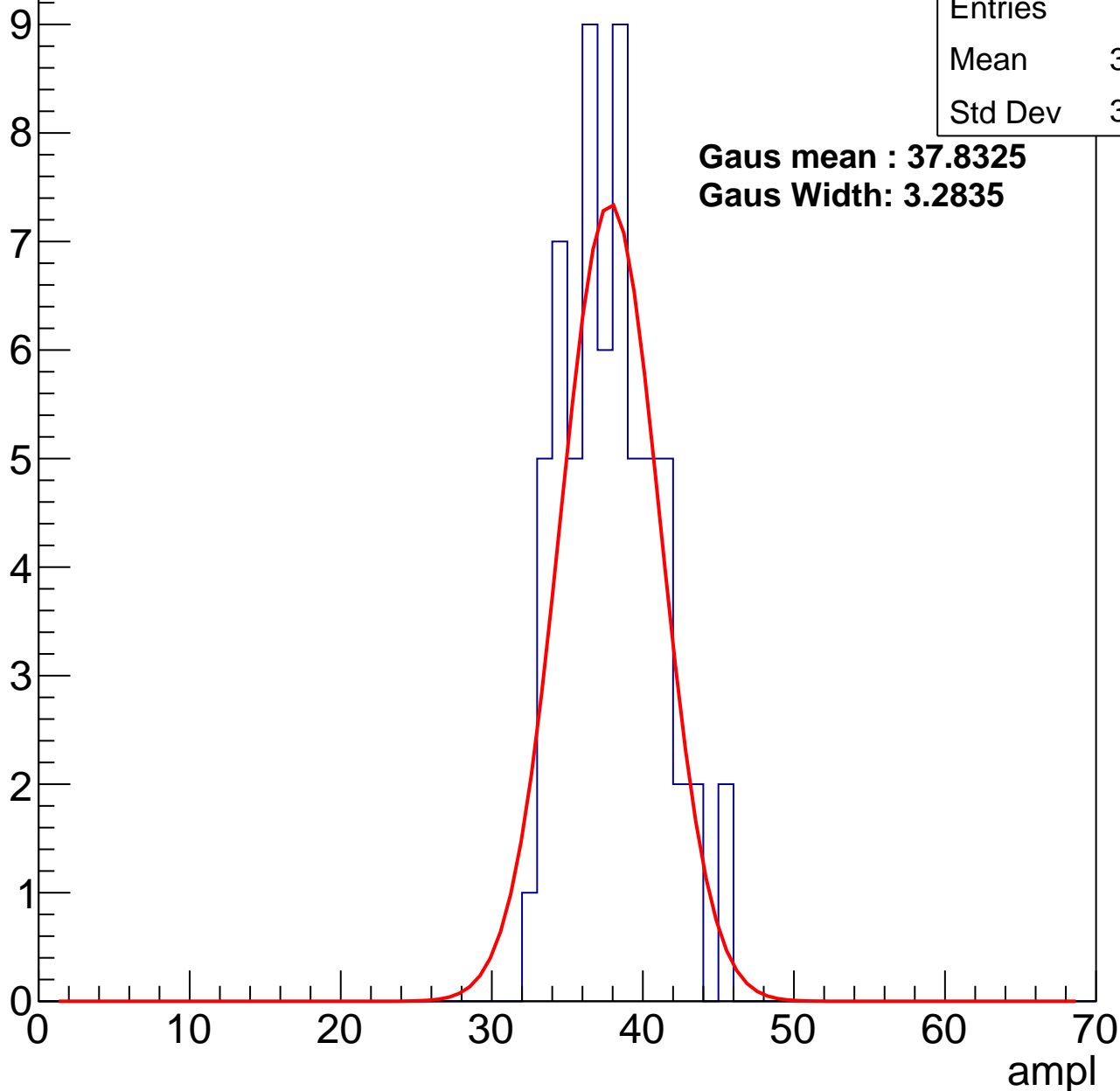
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	37.43
Std Dev	3.059

**Gaus mean : 37.8325**

**Gaus Width: 3.2835**



# B1L101S, U8-ch65, adc2

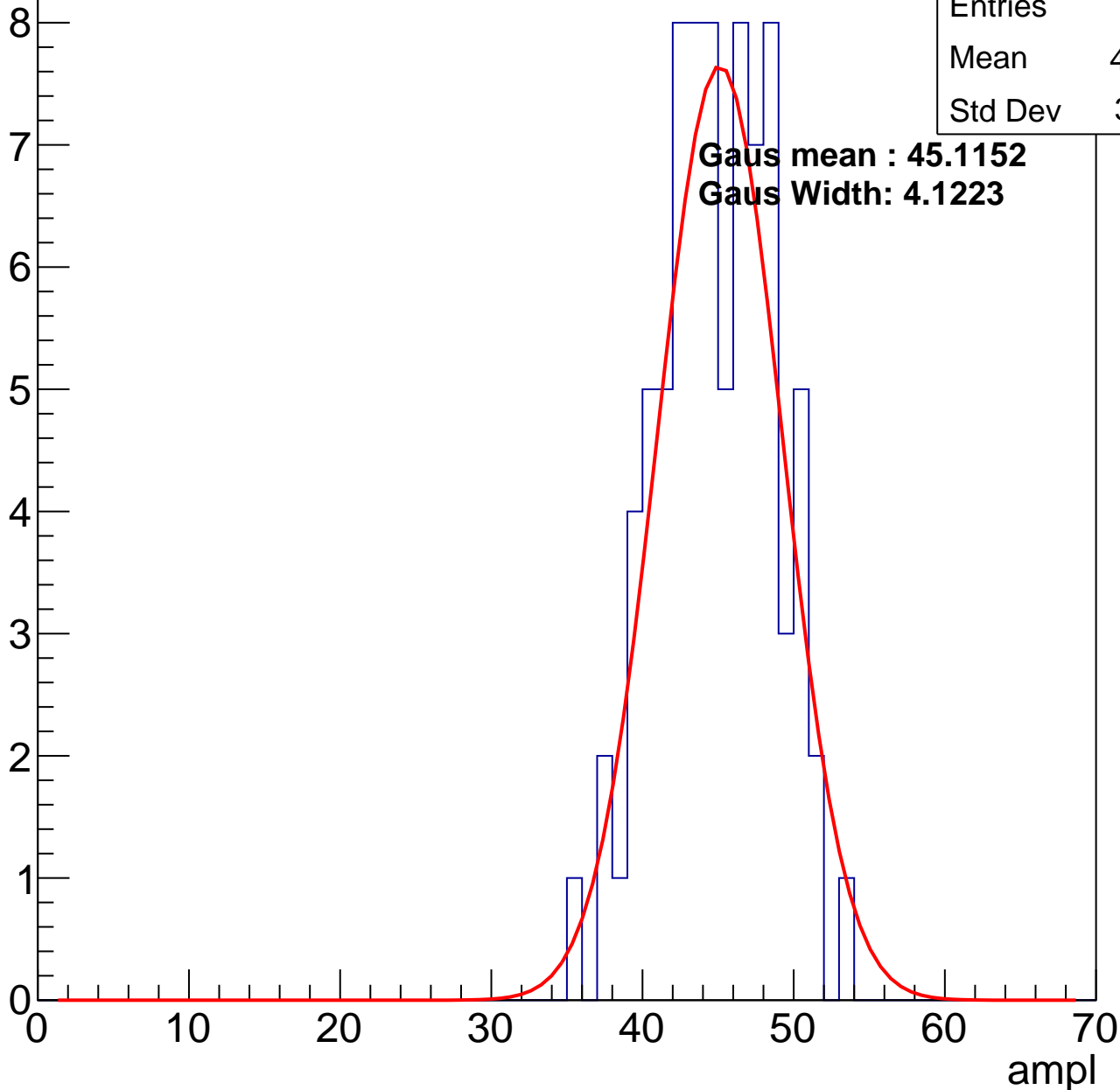
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	44.42
Std Dev	3.731

**Gaus mean : 45.1152**

**Gaus Width: 4.1223**

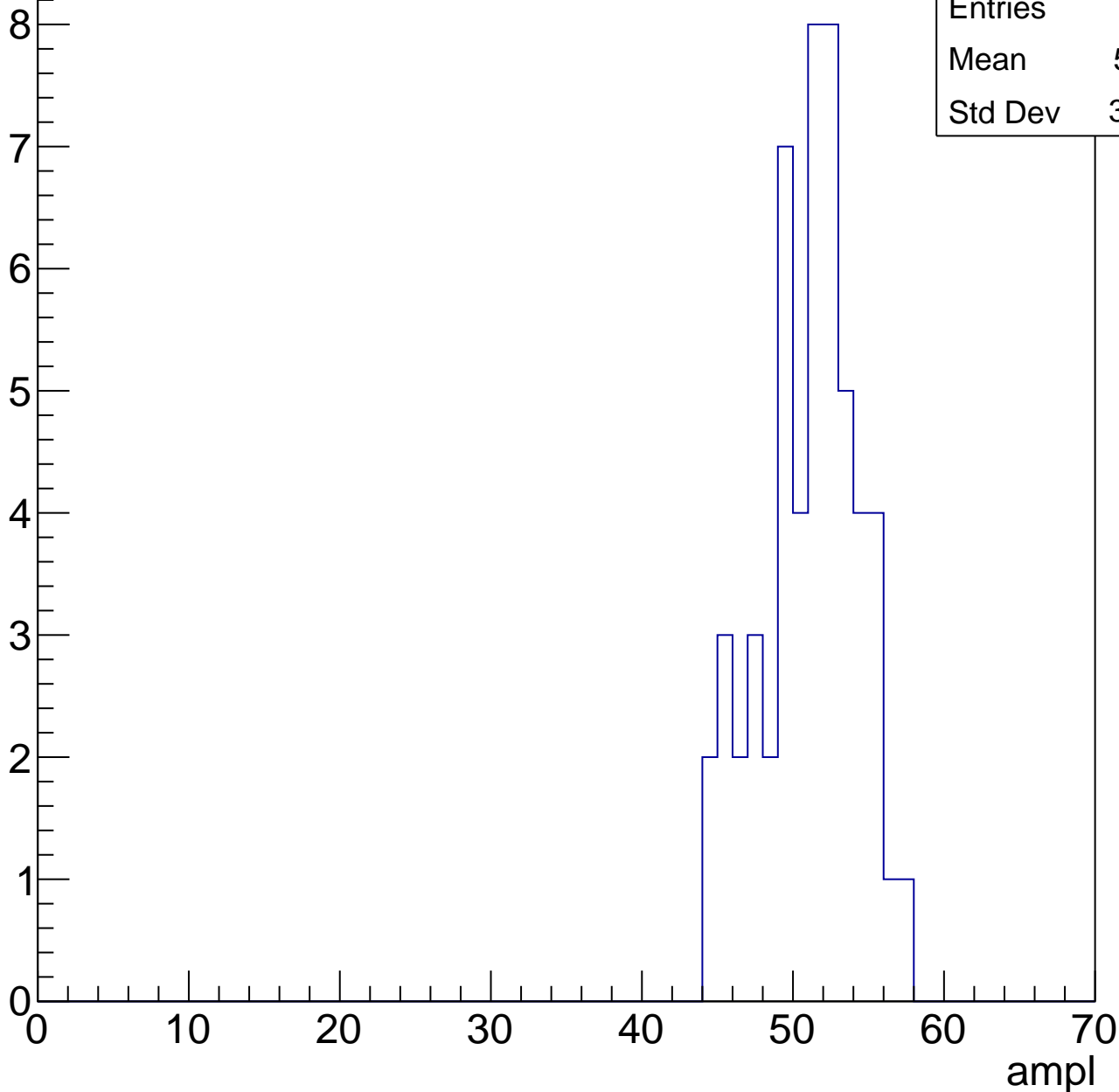


# B1L101S, U8-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

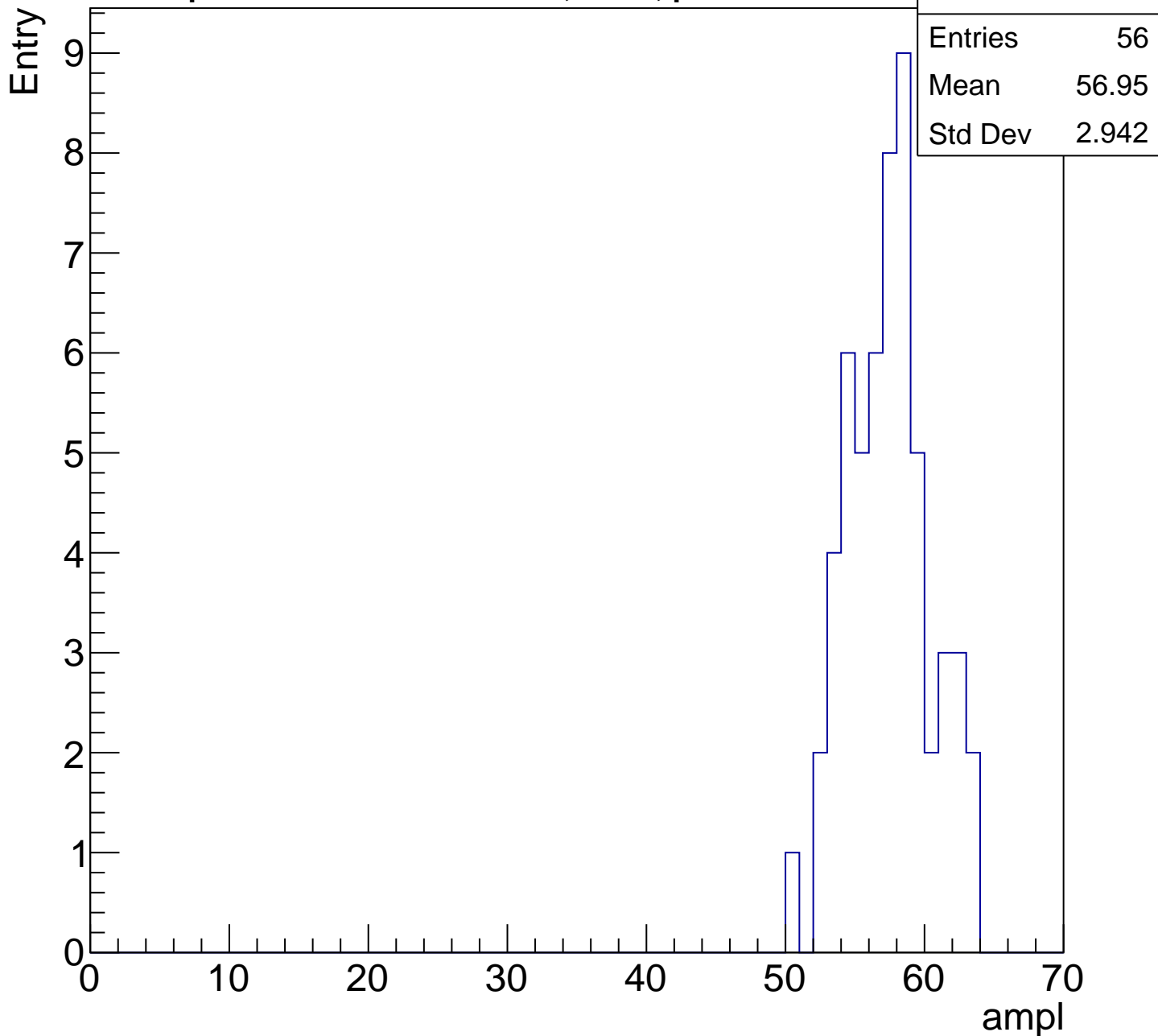
Entry

Entries	54
Mean	50.61
Std Dev	3.147



# B1L101S, U8-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U8-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

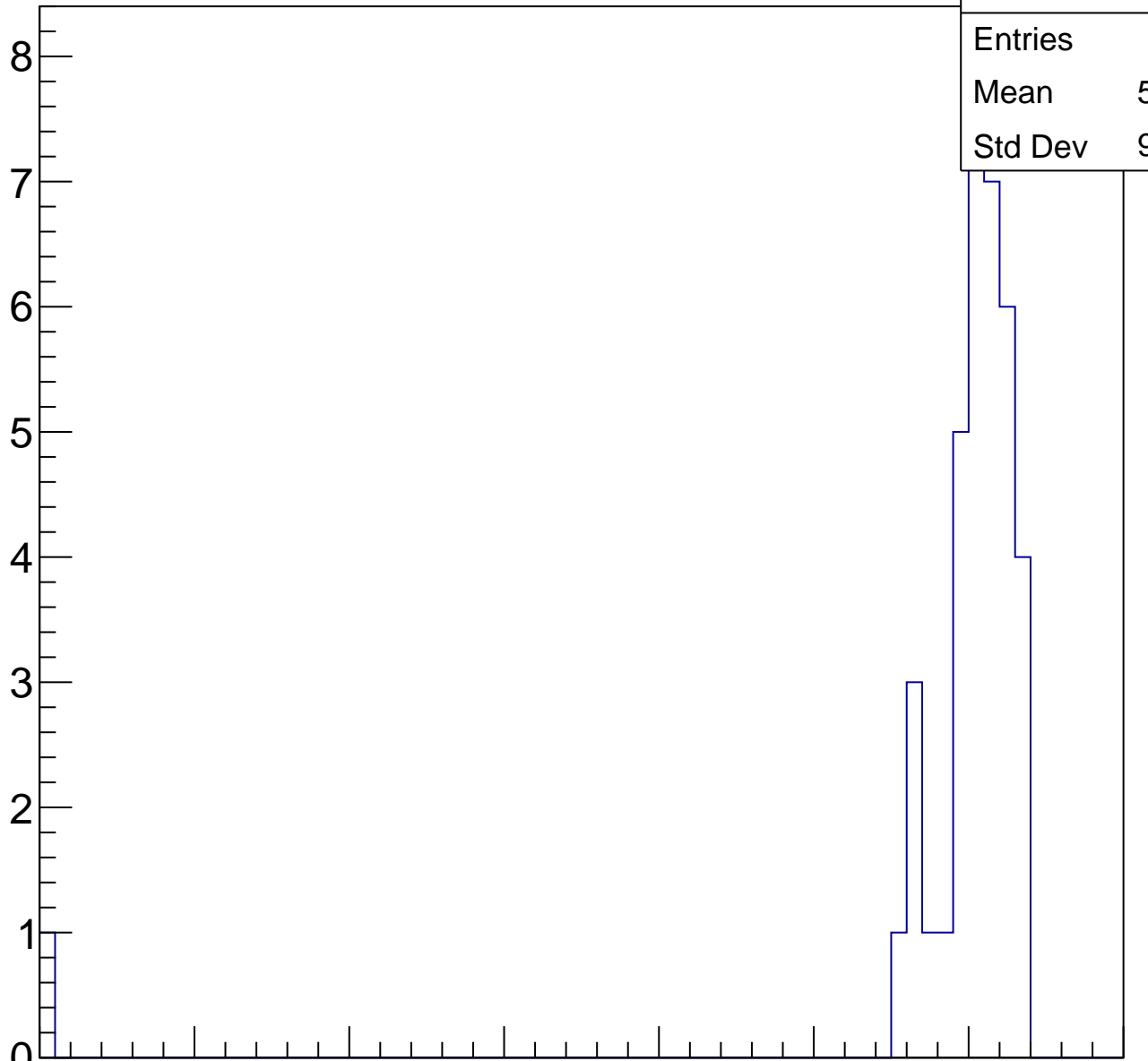
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	37
Mean	58.49
Std Dev	9.964

ampl

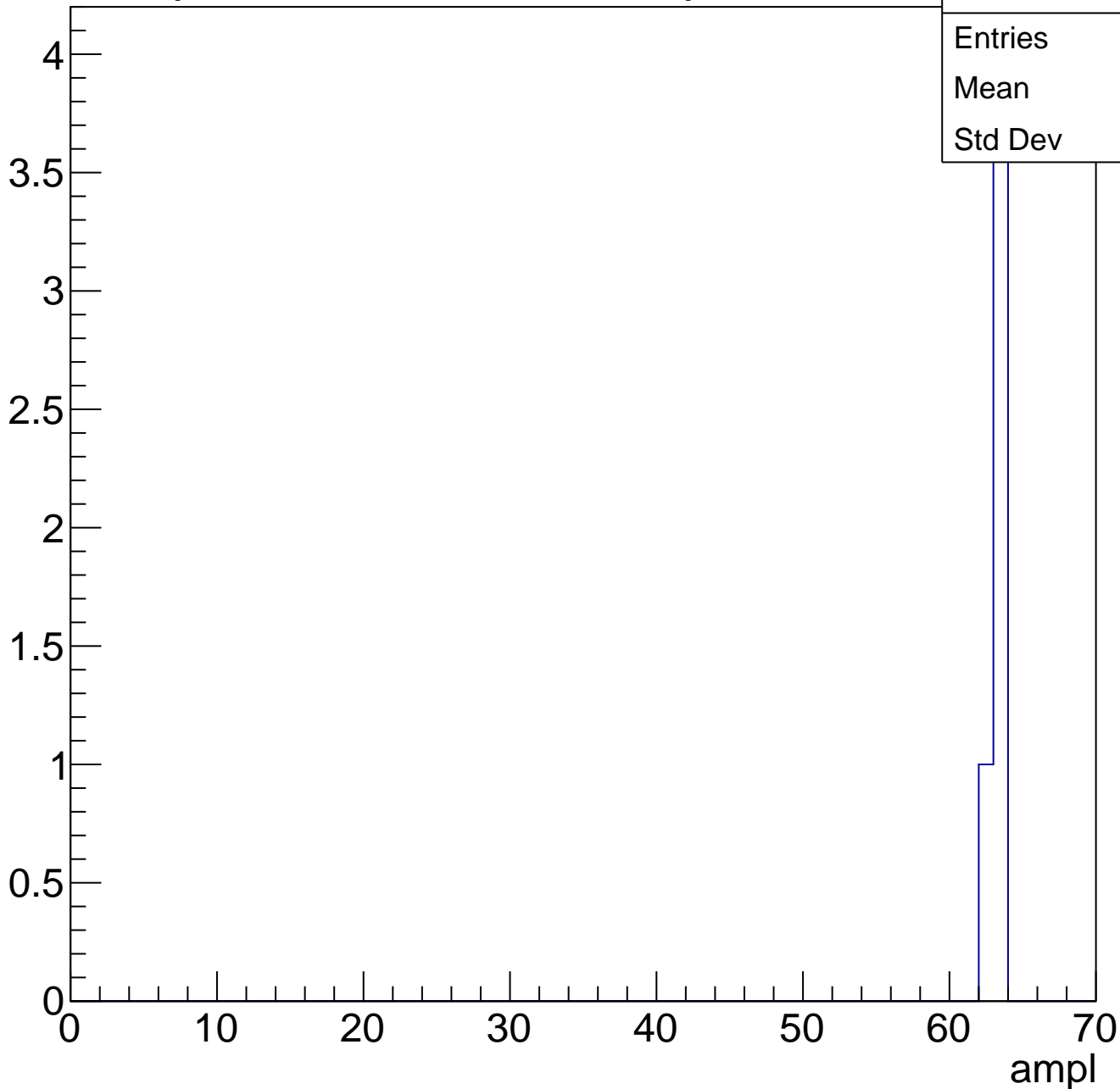
0 10 20 30 40 50 60 70



# B1L101S, U8-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U8-ch66, adc0

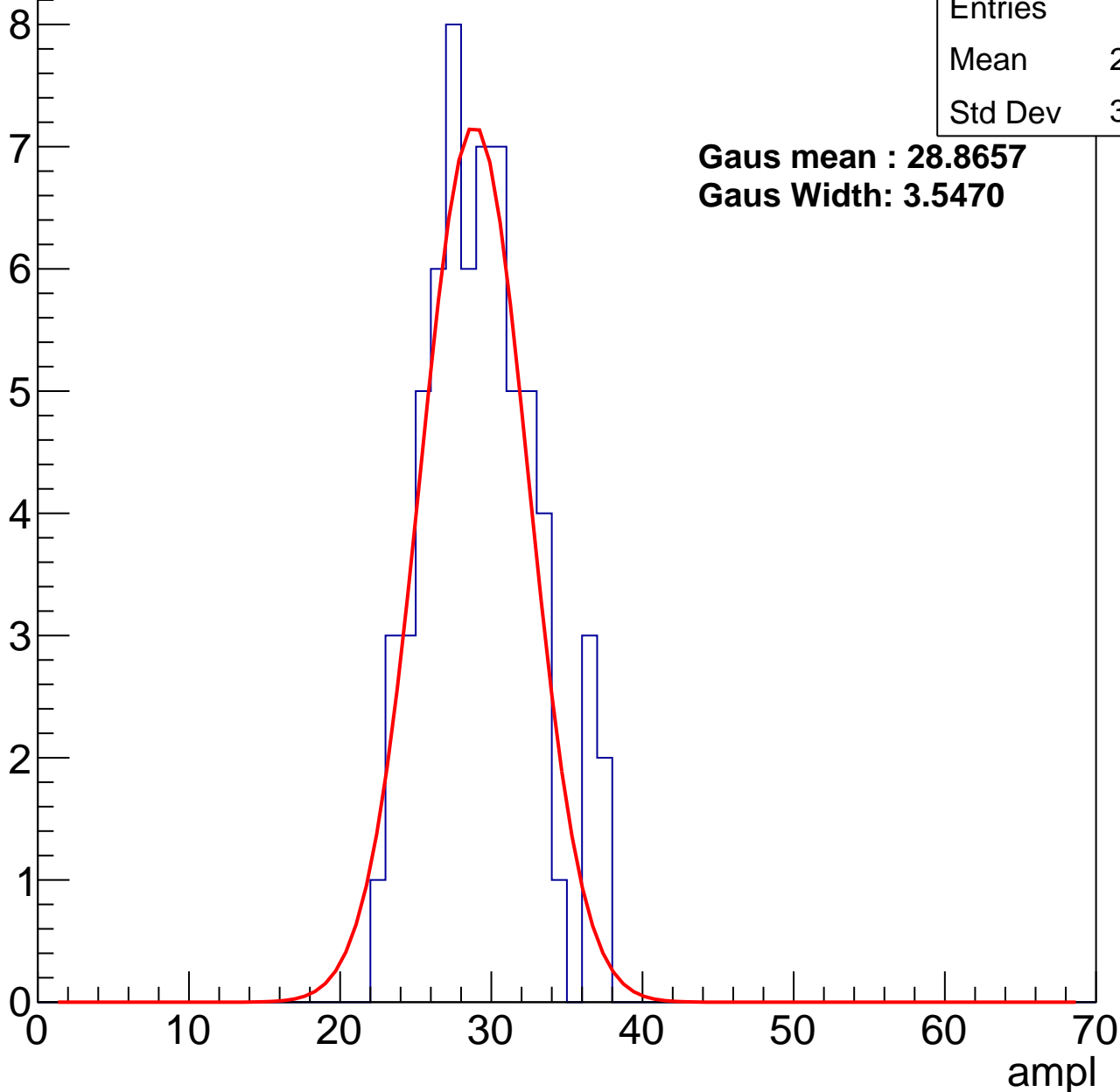
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	28.85
Std Dev	3.564

**Gaus mean : 28.8657**

**Gaus Width: 3.5470**



# B1L101S, U8-ch66, adc1

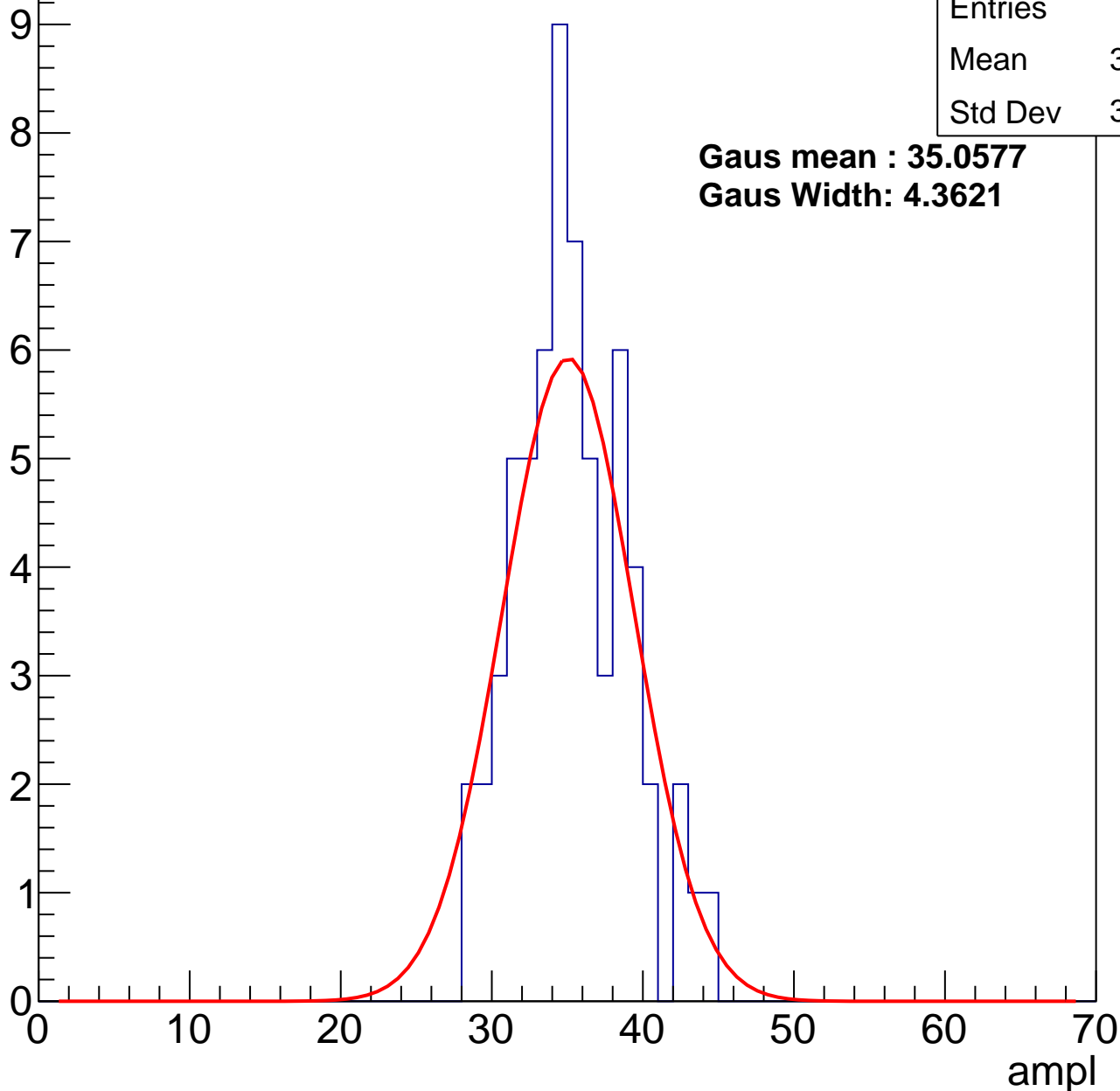
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	34.83
Std Dev	3.628

**Gaus mean : 35.0577**

**Gaus Width: 4.3621**



# B1L101S, U8-ch66, adc2

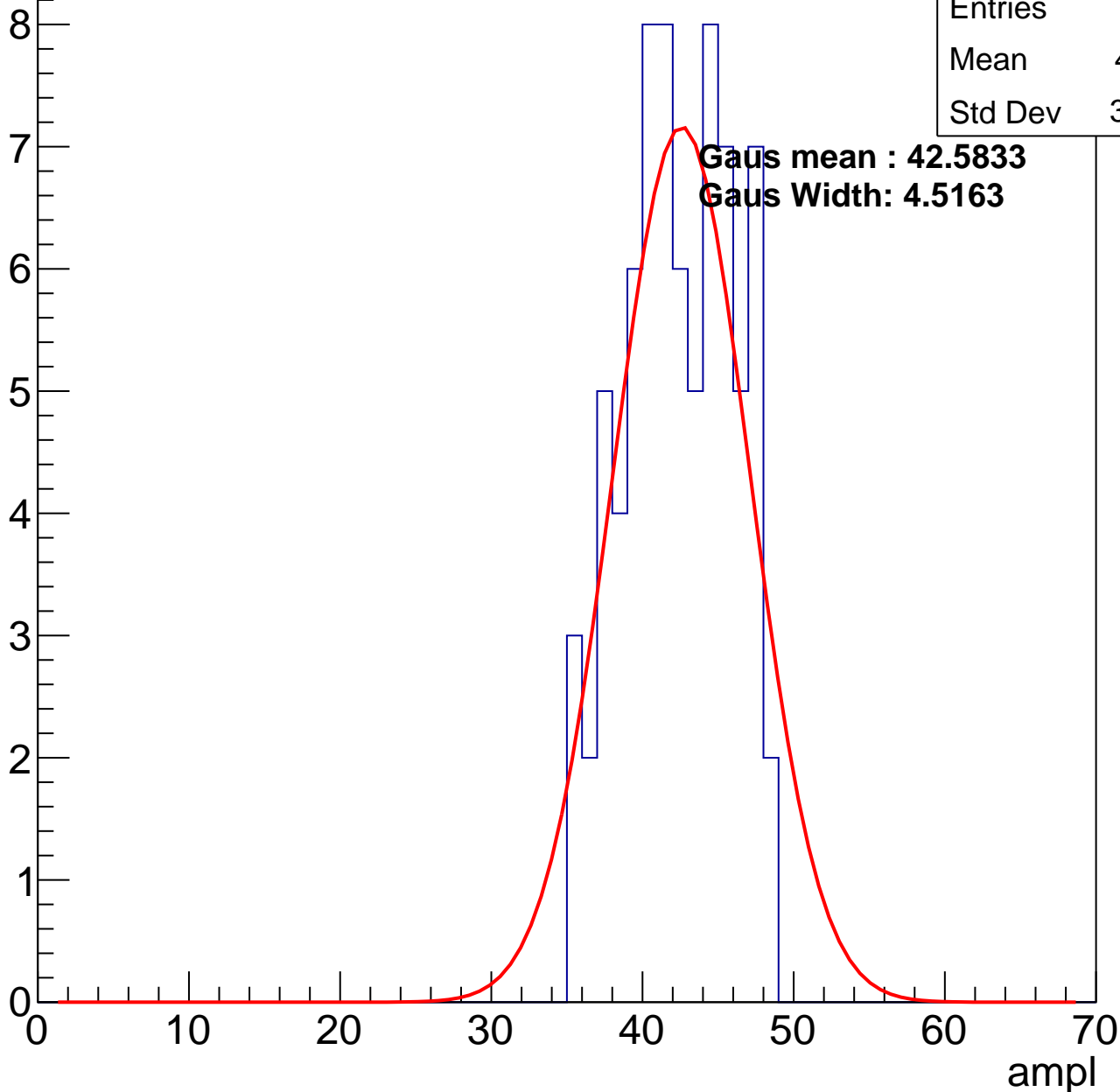
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	41.91
Std Dev	3.495

**Gaus mean : 42.5833**

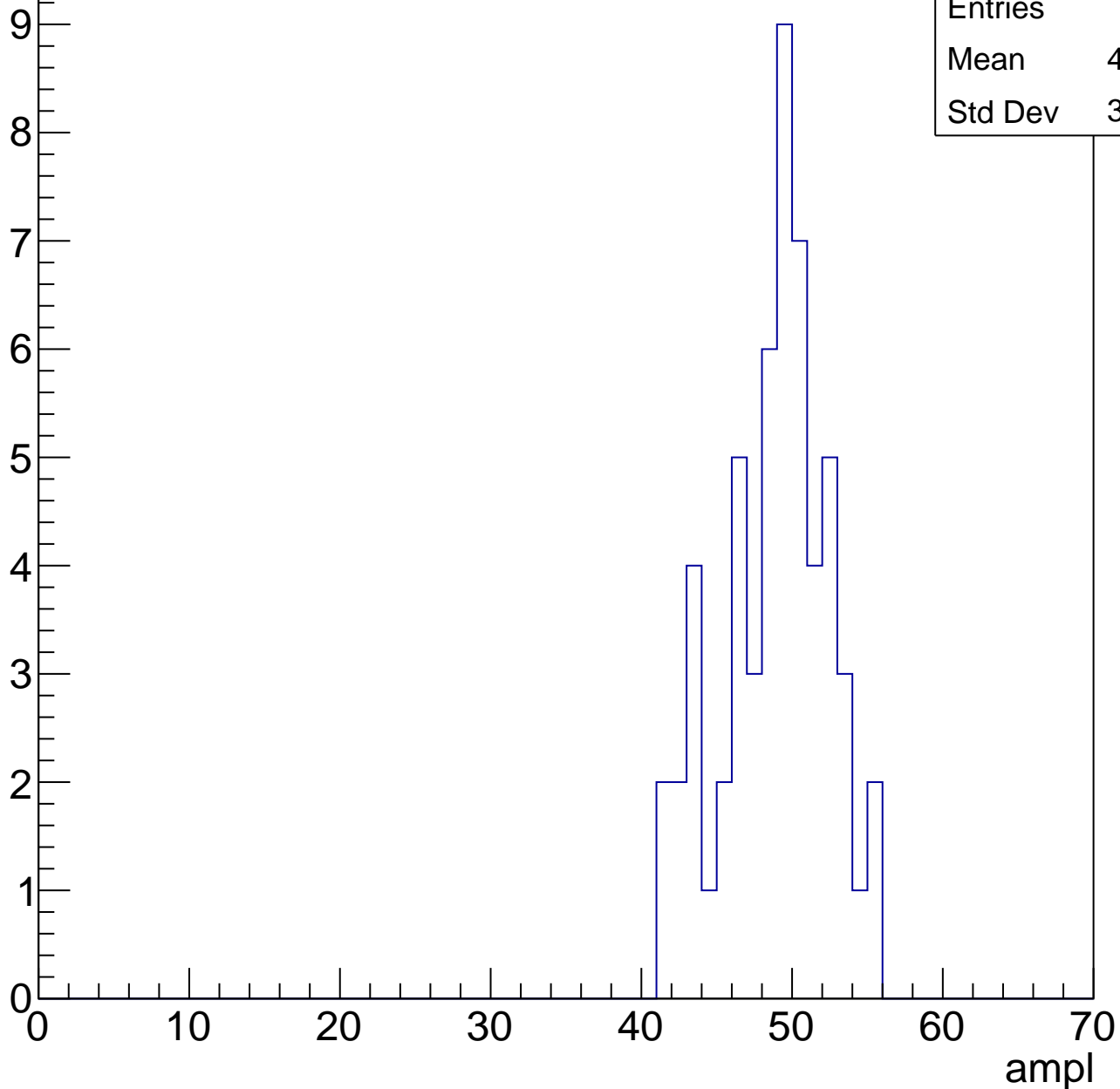
**Gaus Width: 4.5163**



# B1L101S, U8-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

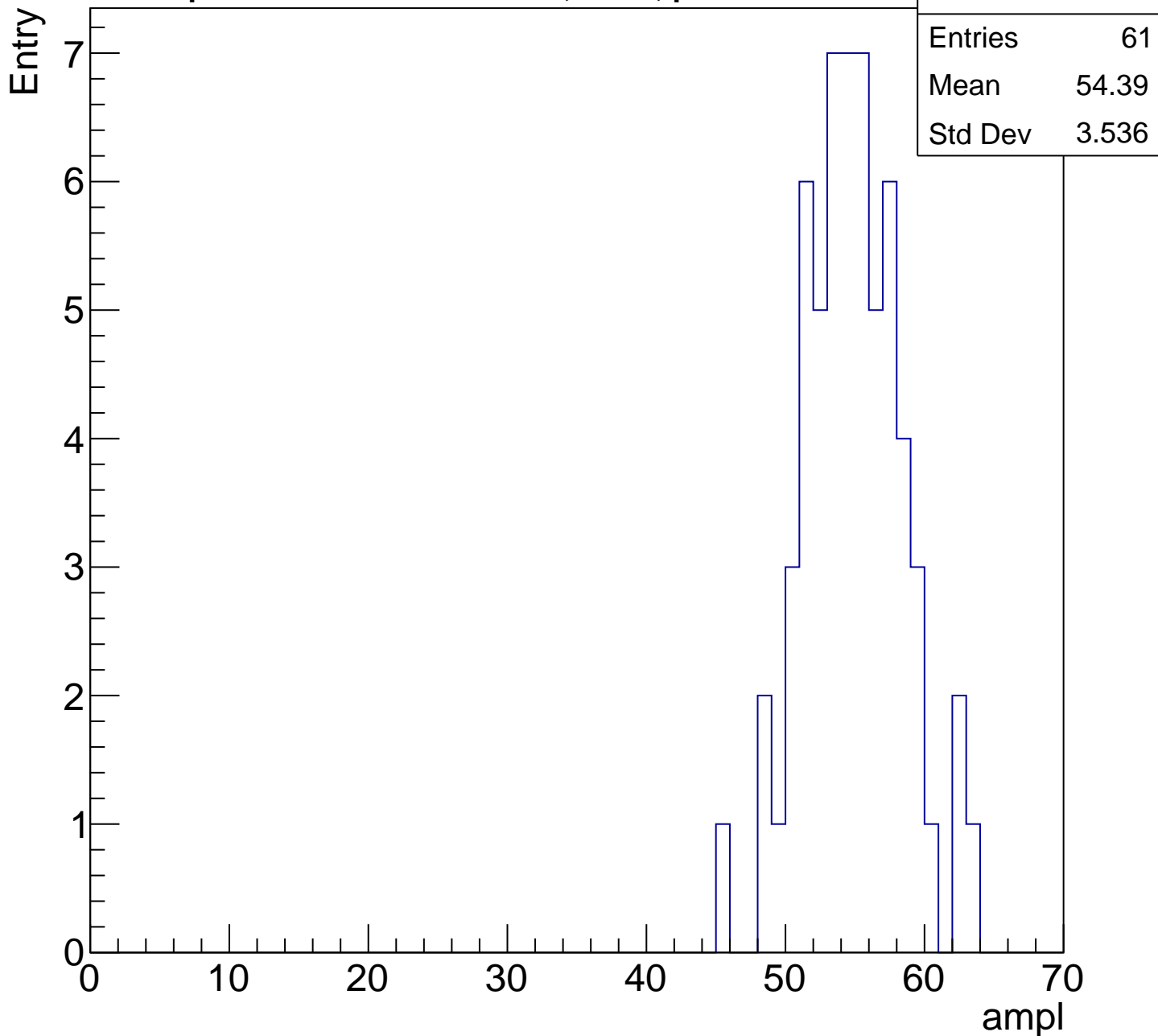
Entry



Entries	56
Mean	48.38
Std Dev	3.488

# B1L101S, U8-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U8-ch66, adc5

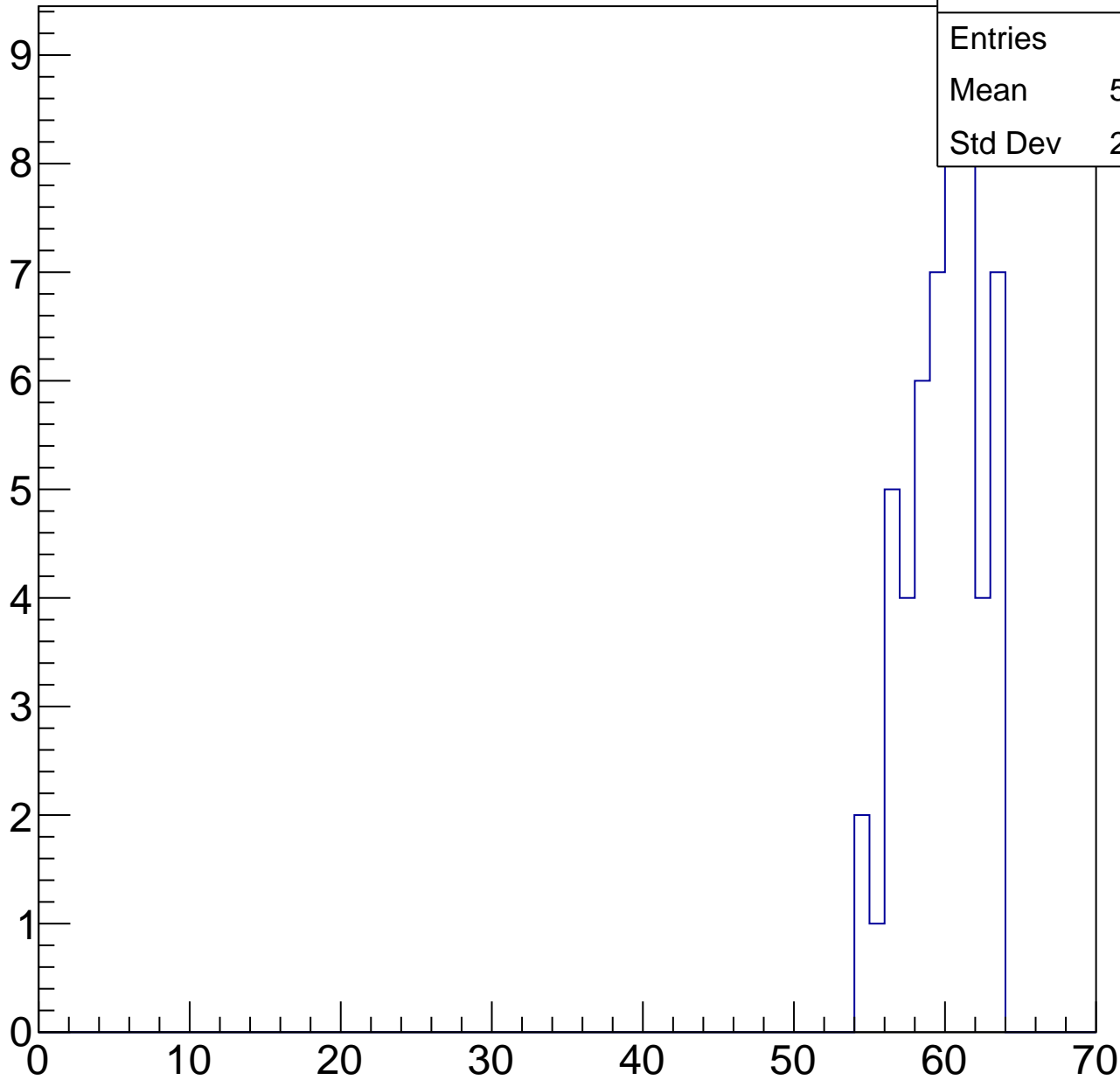
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	54
Mean	59.44
Std Dev	2.417

ampl



# B1L101S, U8-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

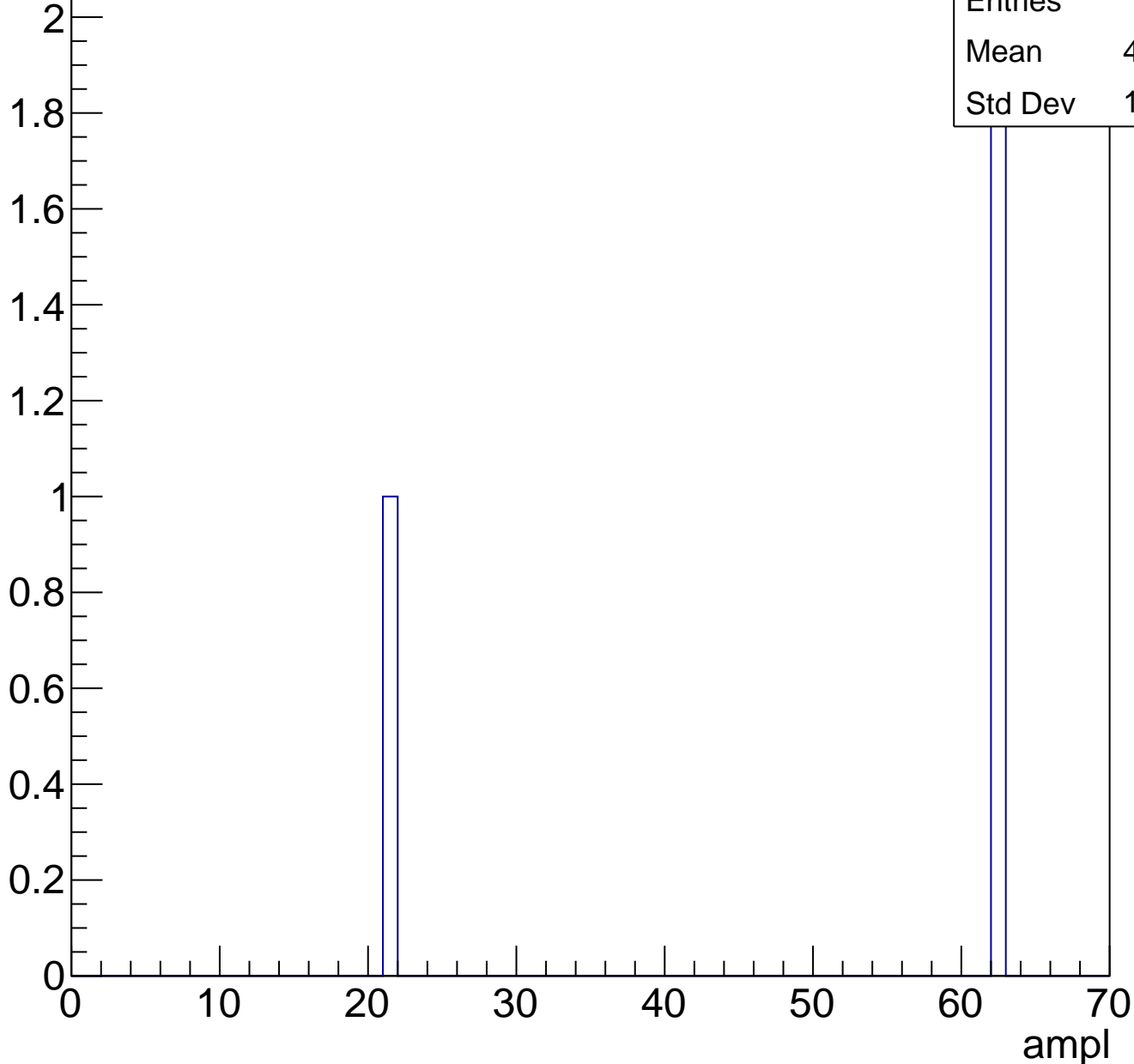




# B1L101S, U8-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	48.33
Std Dev	19.33

# B1L101S, U8-ch67, adc0

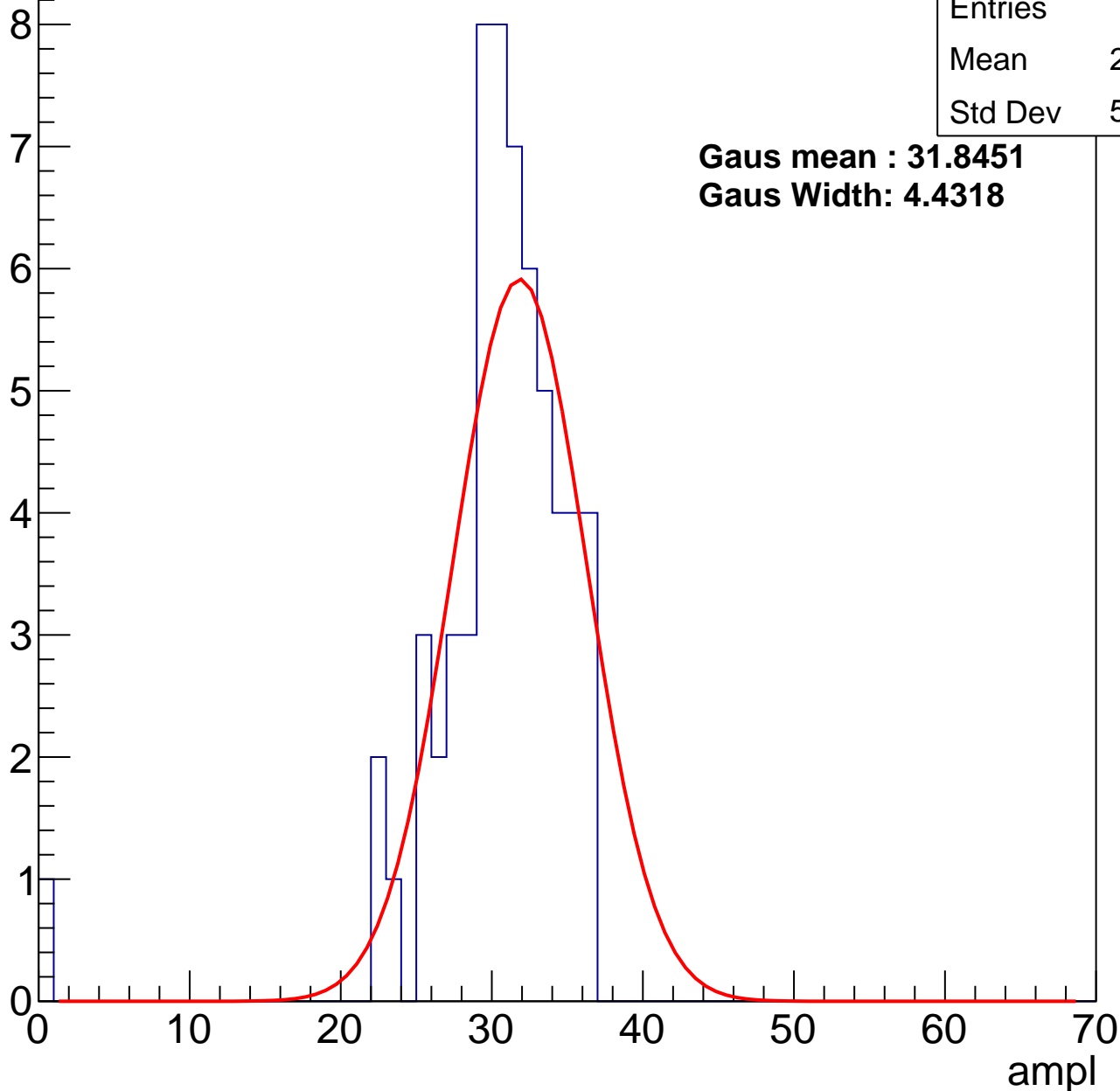
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	29.92
Std Dev	5.145

**Gaus mean : 31.8451**

**Gaus Width: 4.4318**



# B1L101S, U8-ch67, adc1

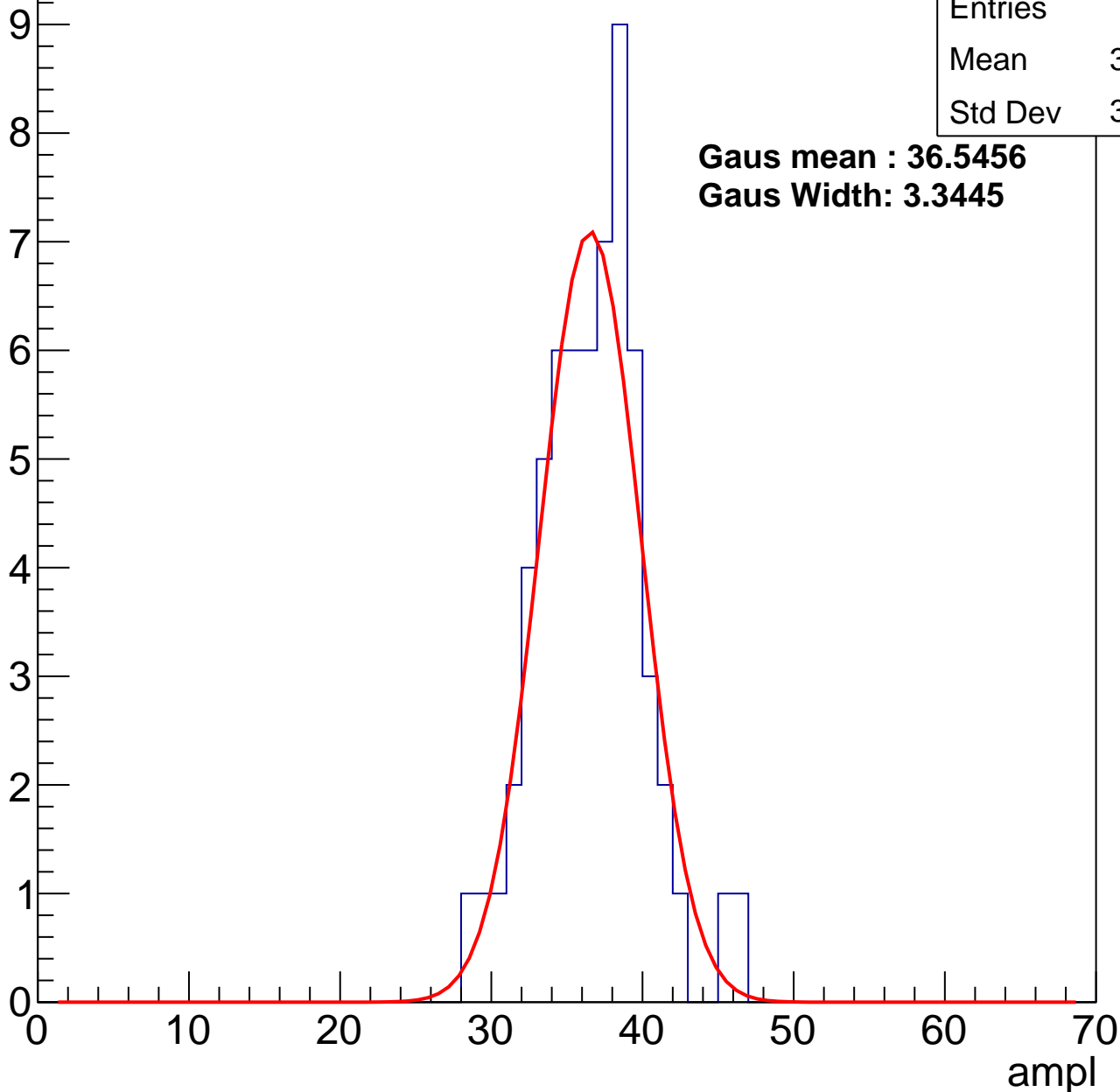
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	36.16
Std Dev	3.474

**Gaus mean : 36.5456**

**Gaus Width: 3.3445**



# B1L101S, U8-ch67, adc2

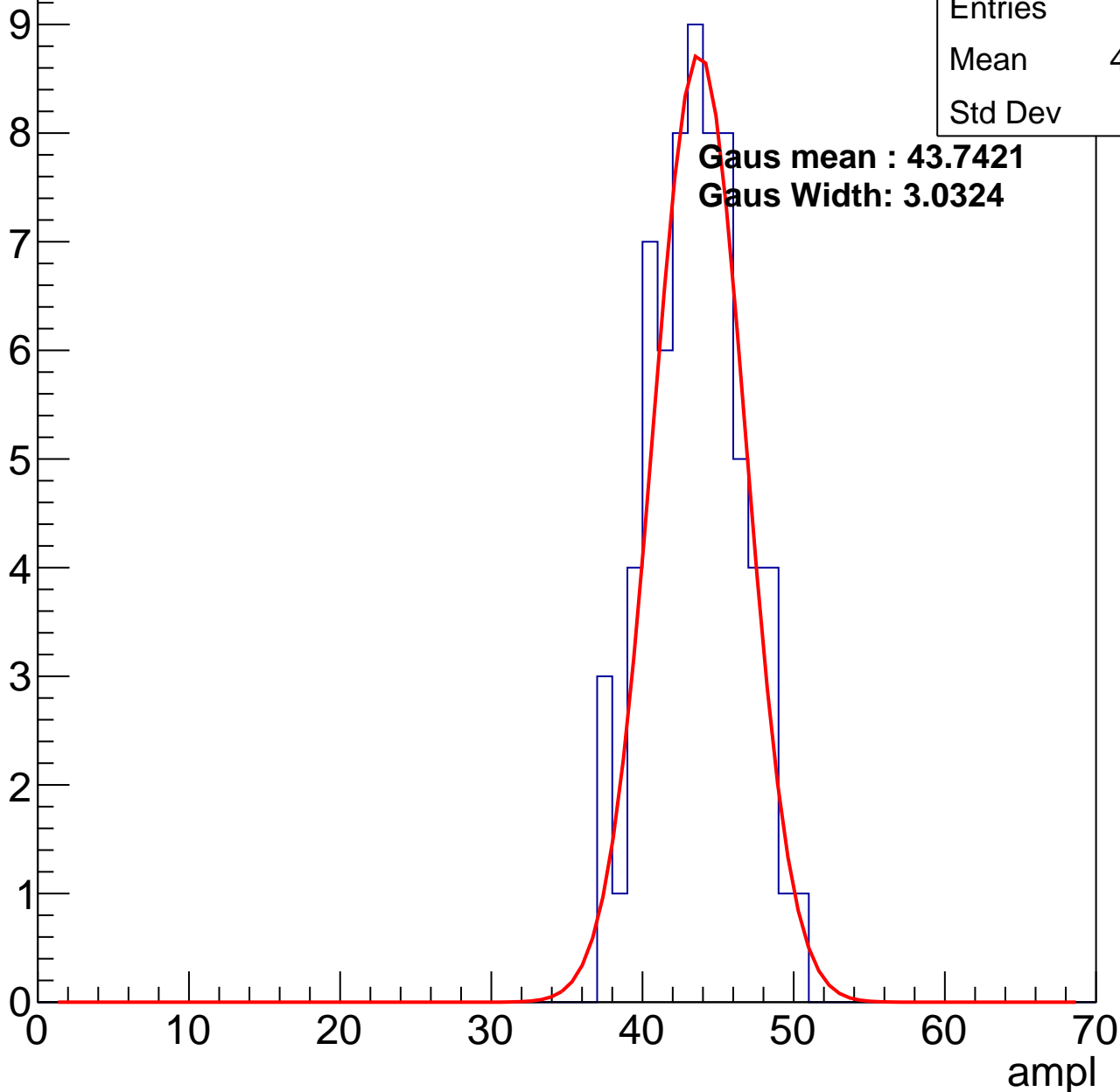
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	43.12
Std Dev	3.01

**Gaus mean : 43.7421**

**Gaus Width: 3.0324**

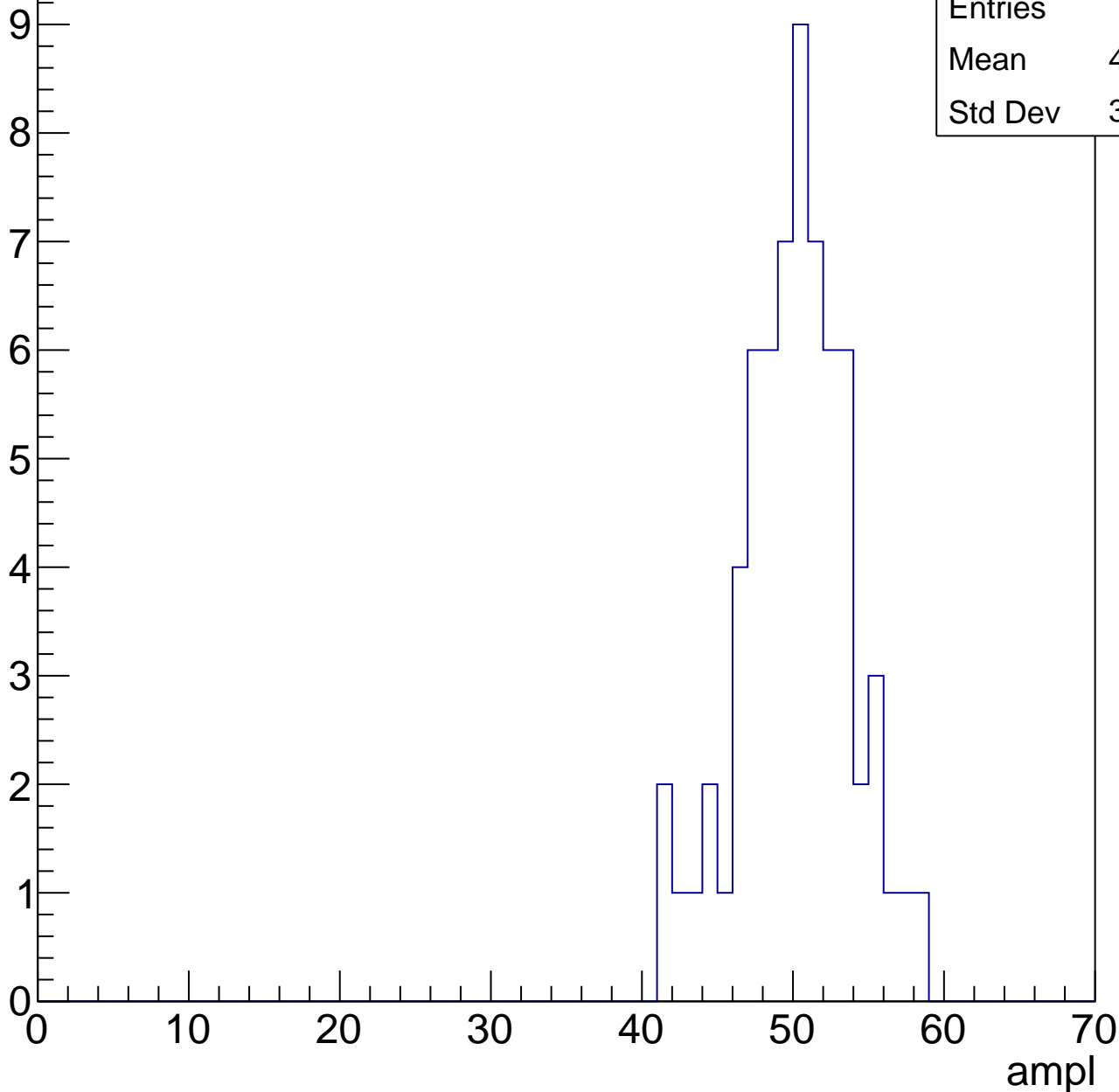


# B1L101S, U8-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

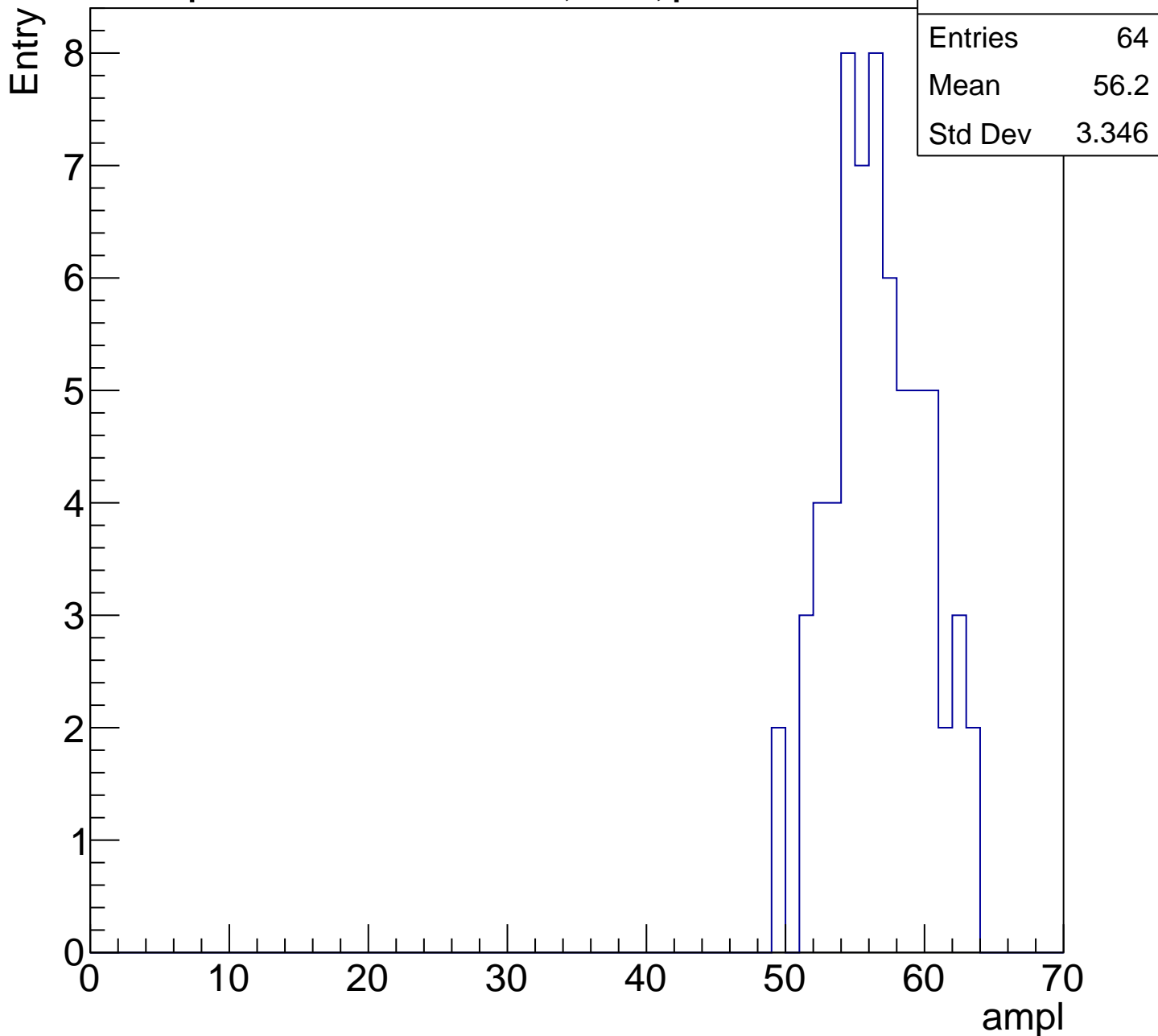
Entry

Entries	66
Mean	49.67
Std Dev	3.599



# B1L101S, U8-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

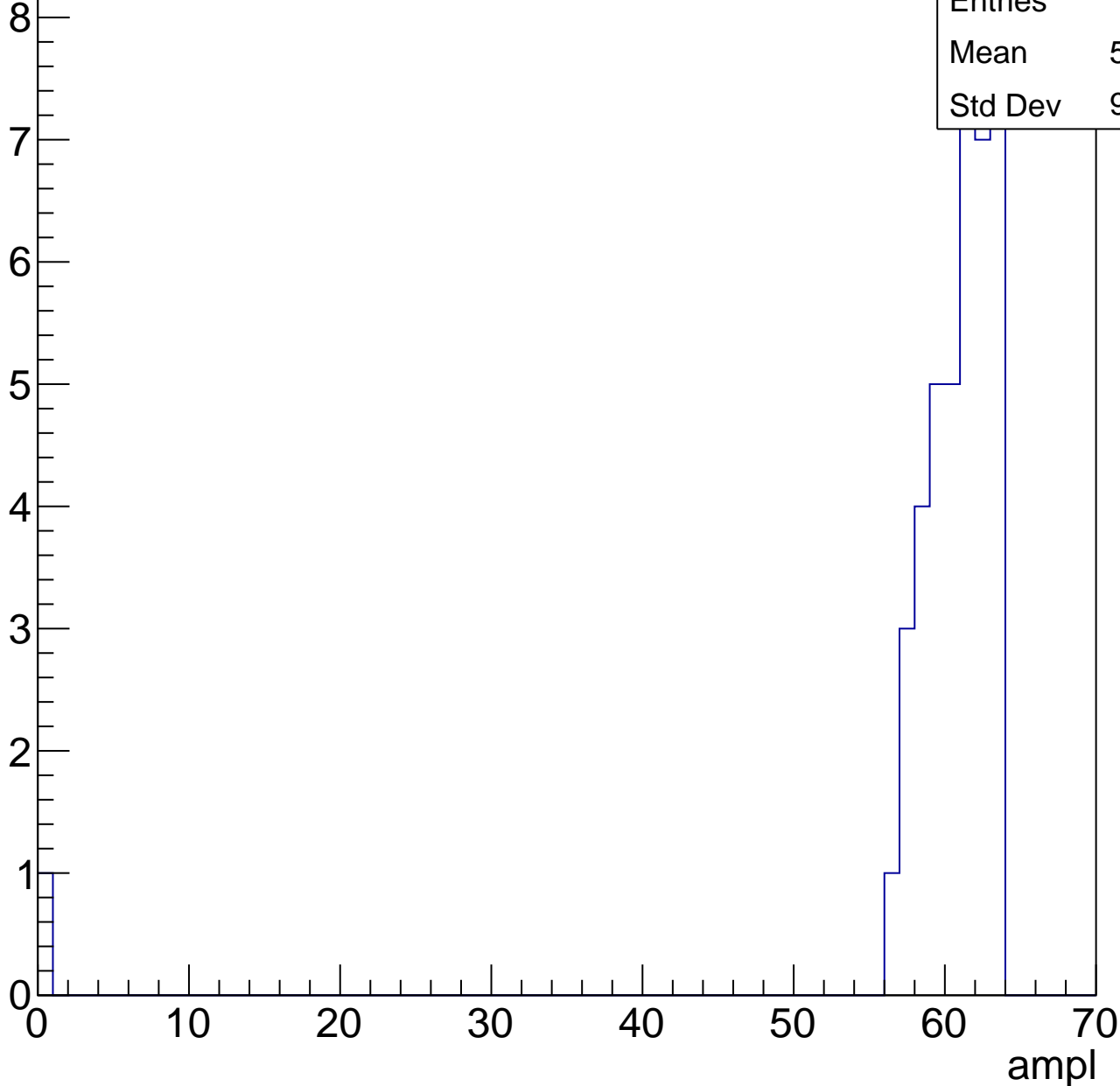


# B1L101S, U8-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	59.05
Std Dev	9.429



# B1L101S, U8-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L101S, U8-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch68, adc0

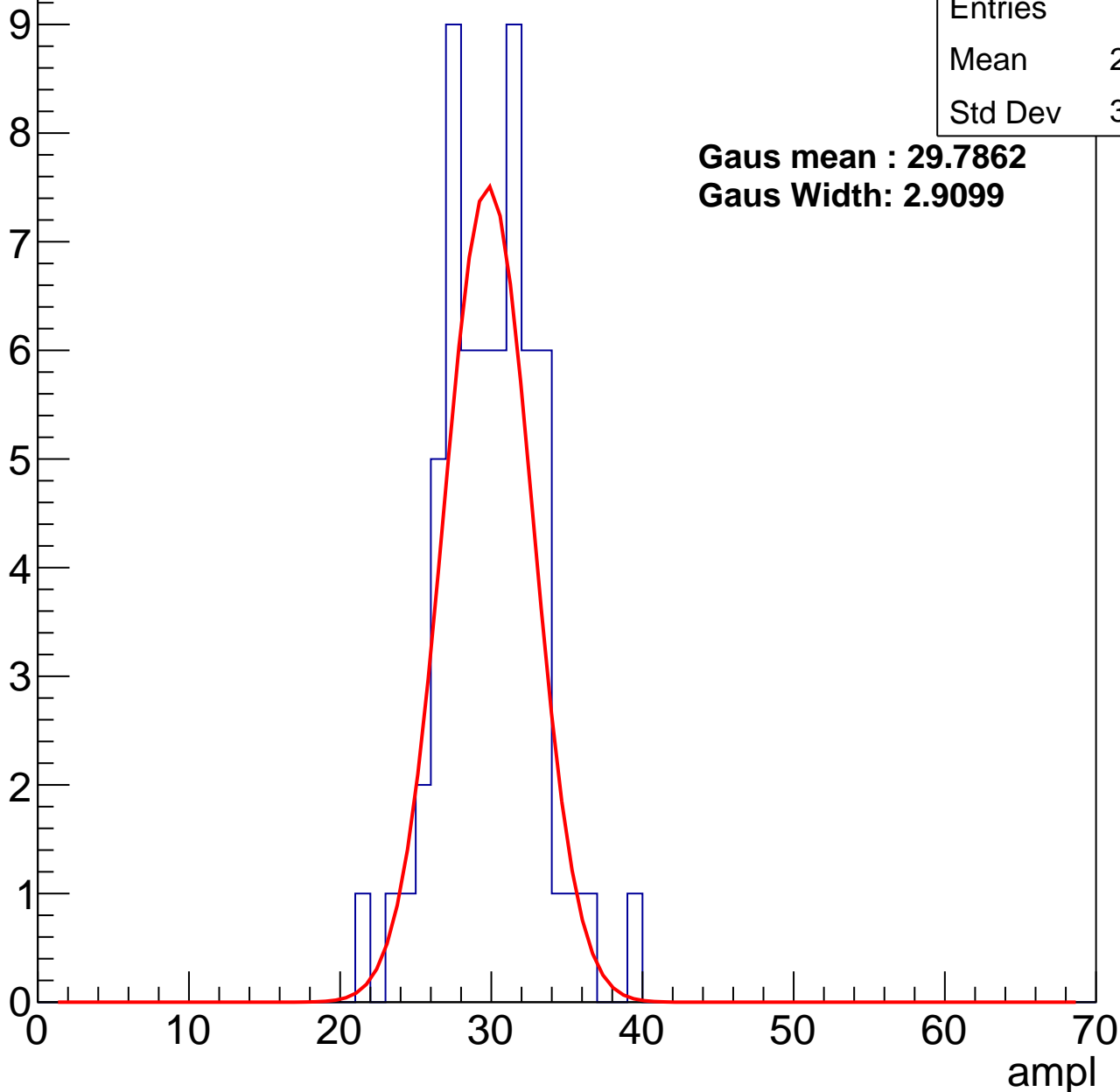
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	29.45
Std Dev	3.196

**Gaus mean : 29.7862**

**Gaus Width: 2.9099**



# B1L101S, U8-ch68, adc1

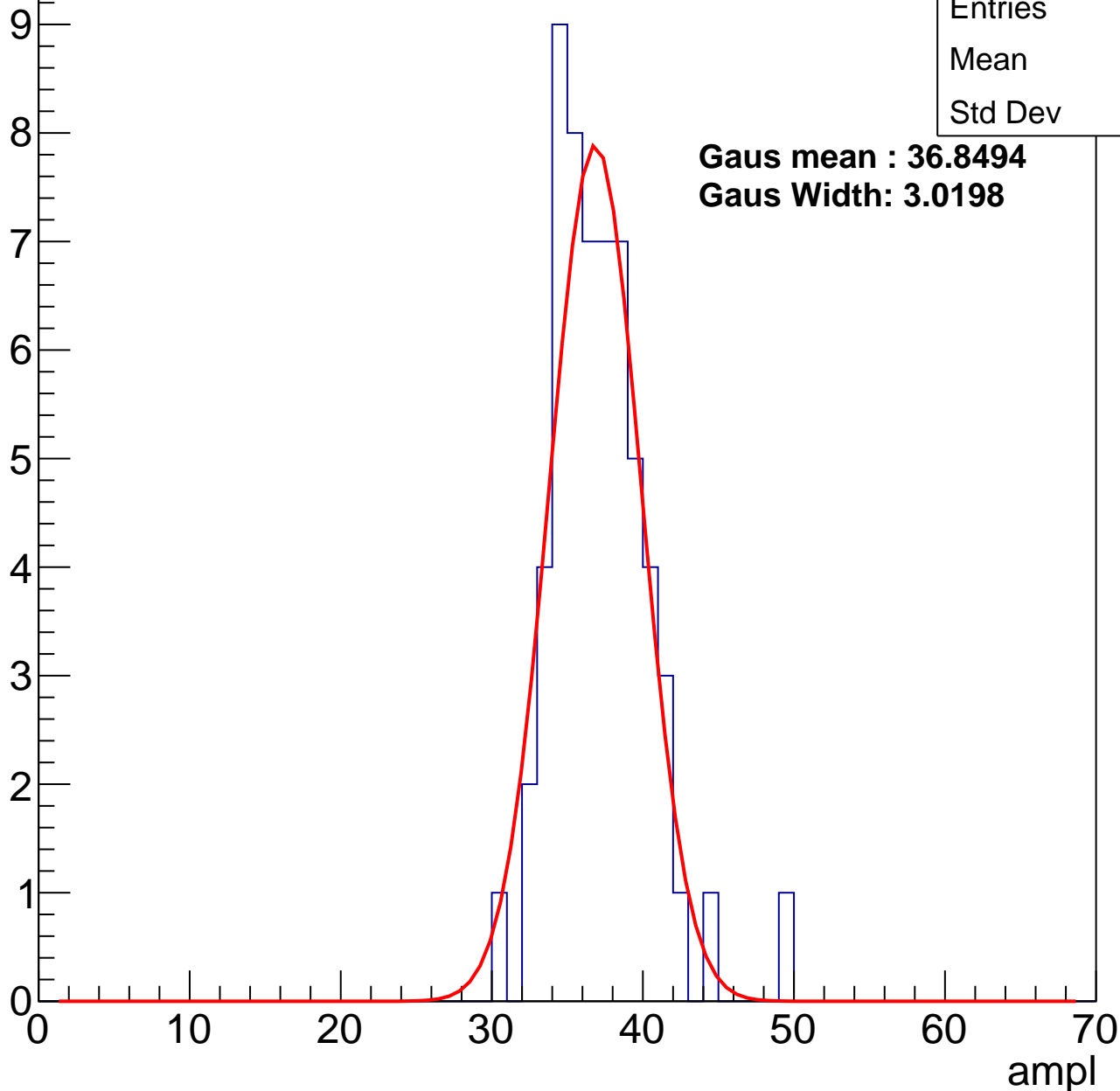
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	36.7
Std Dev	3.18

**Gaus mean : 36.8494**

**Gaus Width: 3.0198**



# B1L101S, U8-ch68, adc2

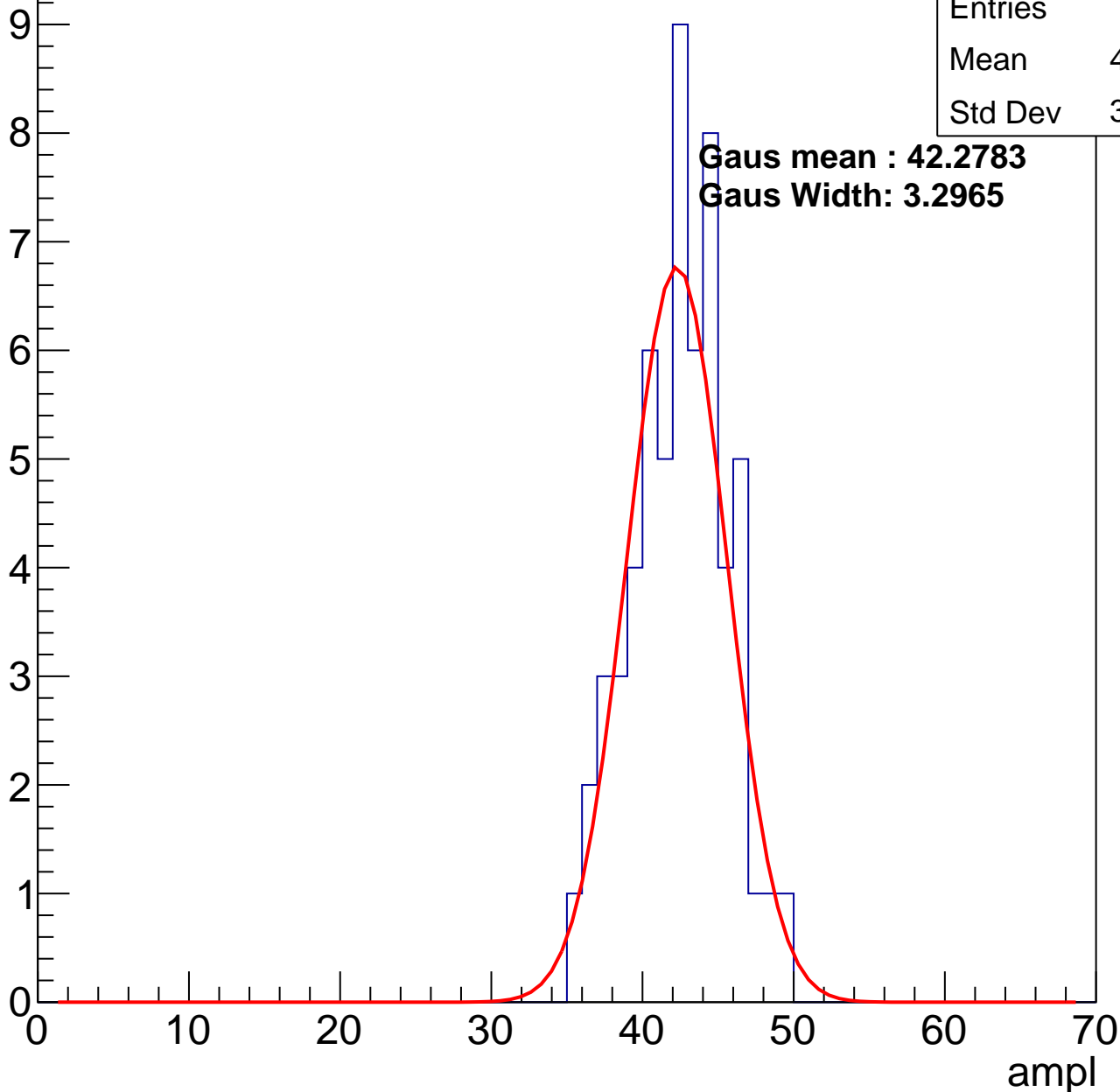
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	41.95
Std Dev	3.116

**Gaus mean : 42.2783**

**Gaus Width: 3.2965**



# B1L101S, U8-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

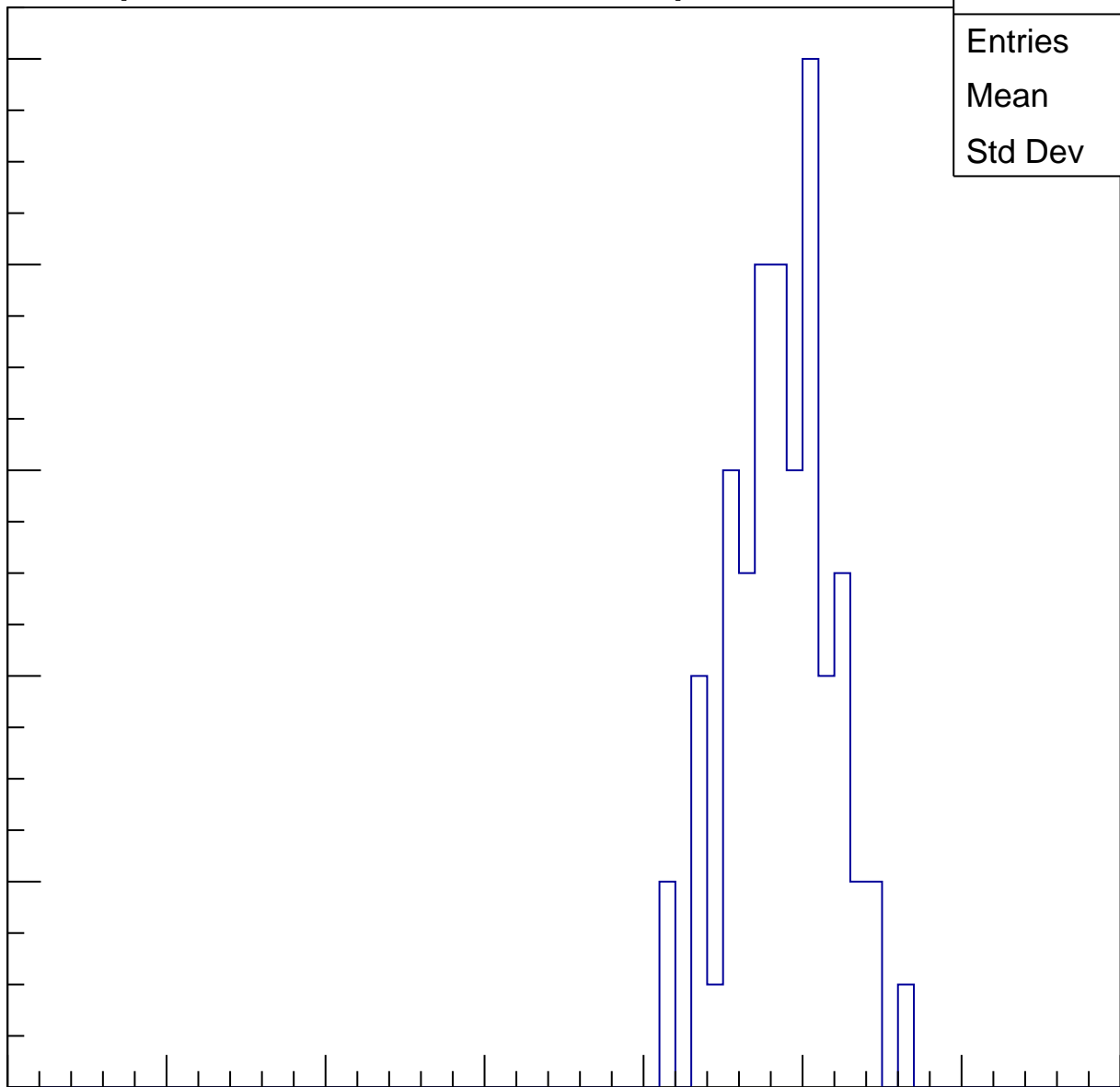
Entries	64
Mean	48.22
Std Dev	3.165

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

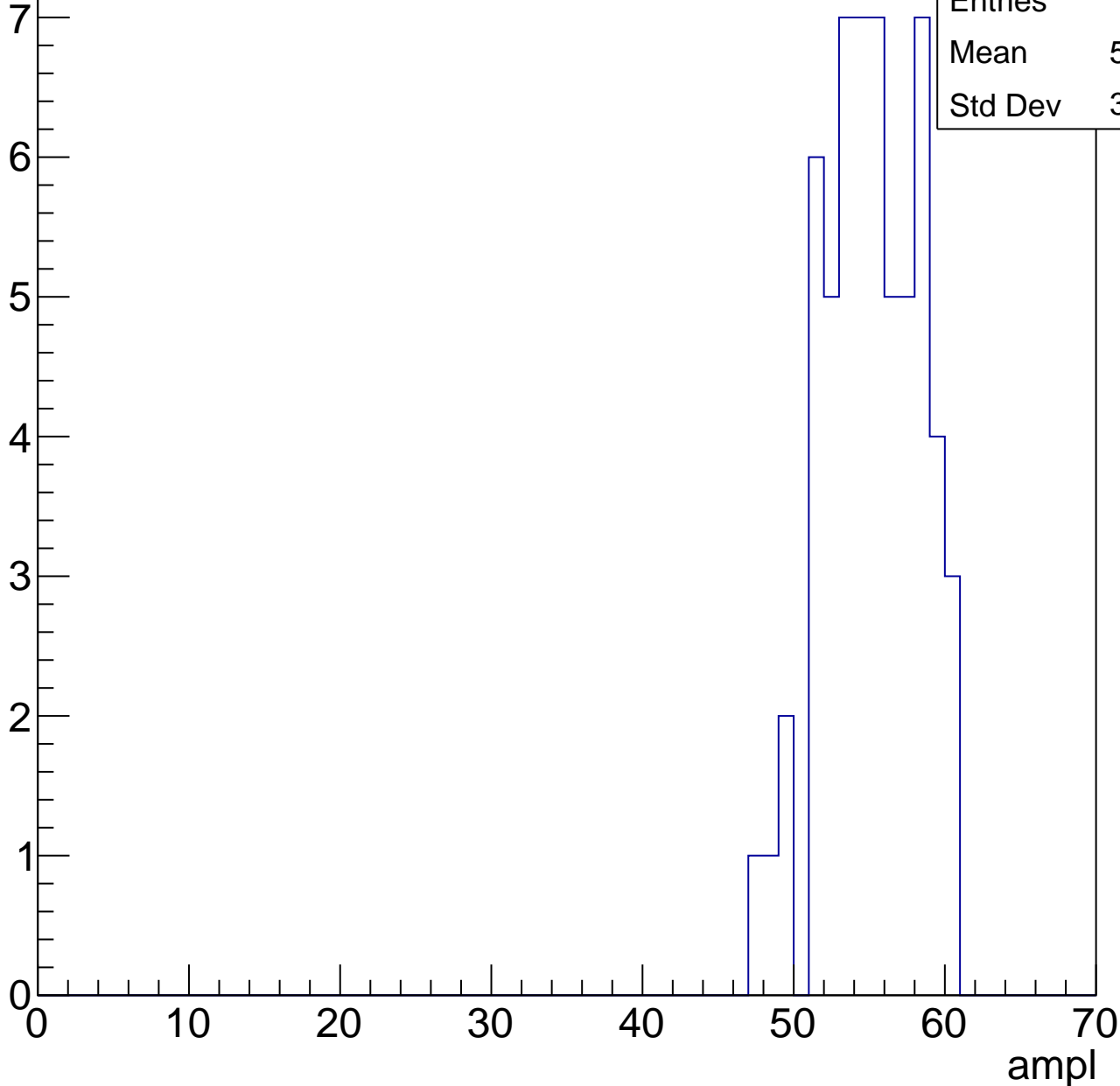


# B1L101S, U8-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

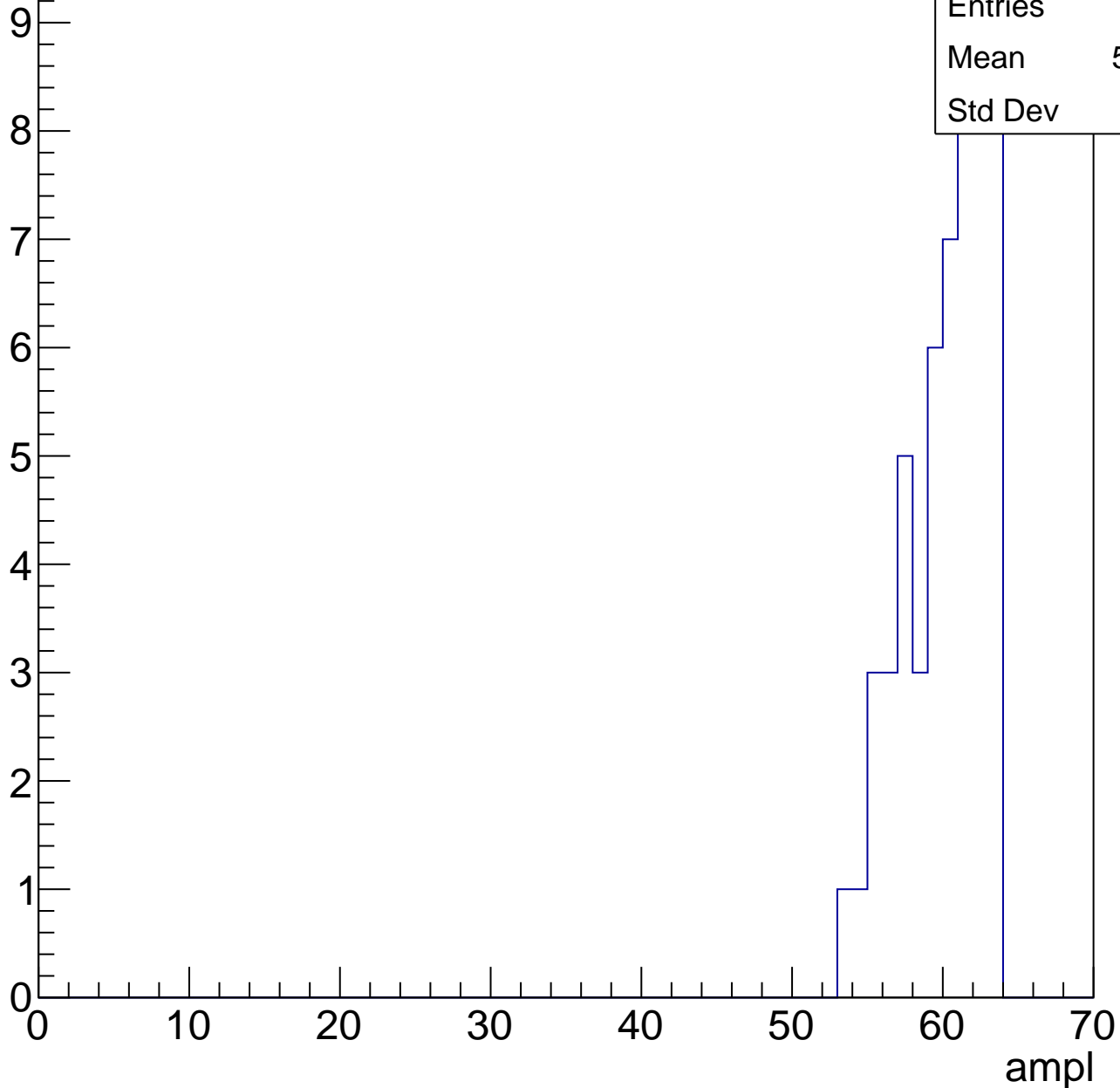
Entries	60
Mean	54.67
Std Dev	3.113



# B1L101S, U8-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

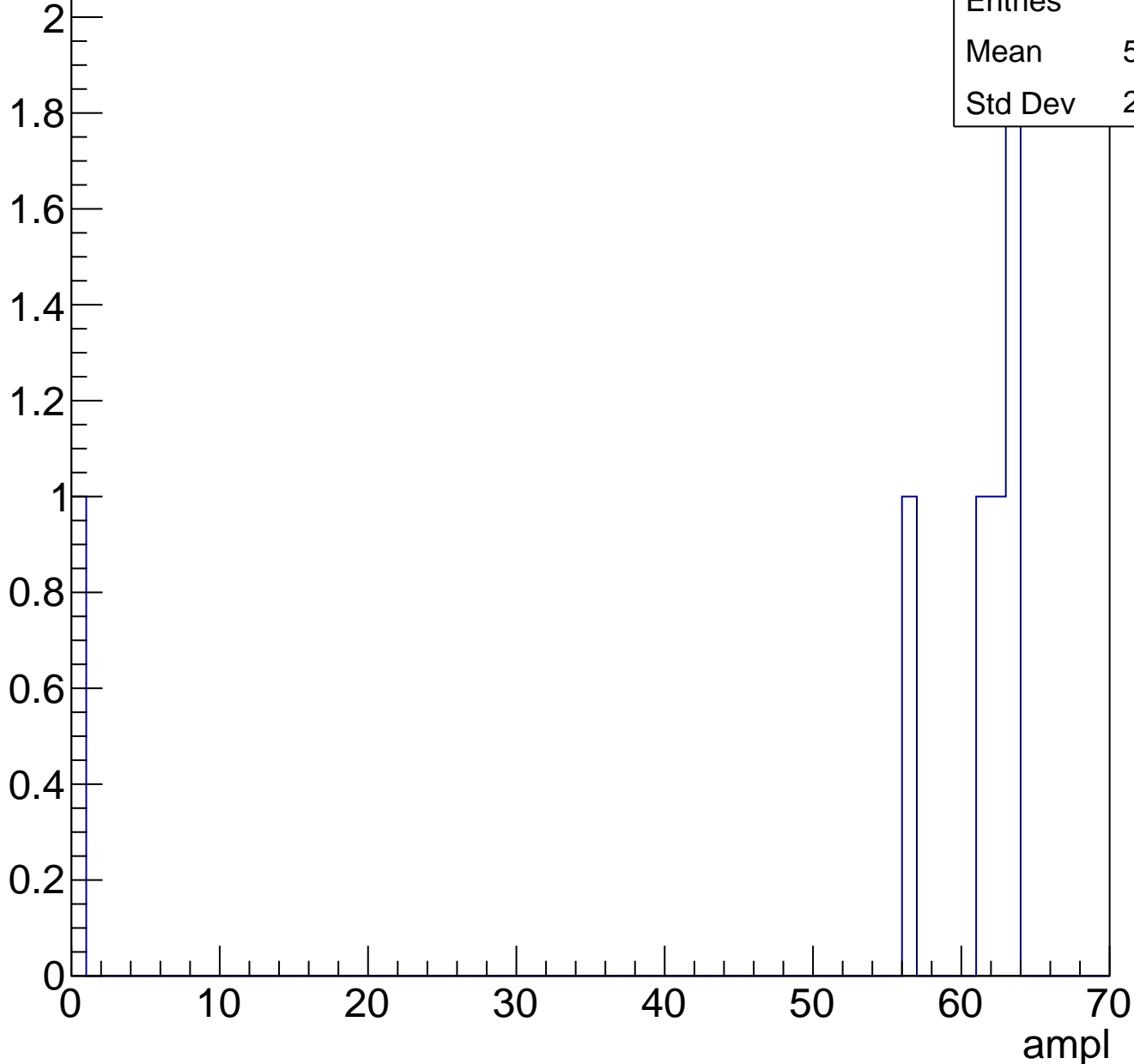
Entry



# B1L101S, U8-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch69, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	67
Mean	29.9
Std Dev	3.529

**Gaus mean : 30.7030**

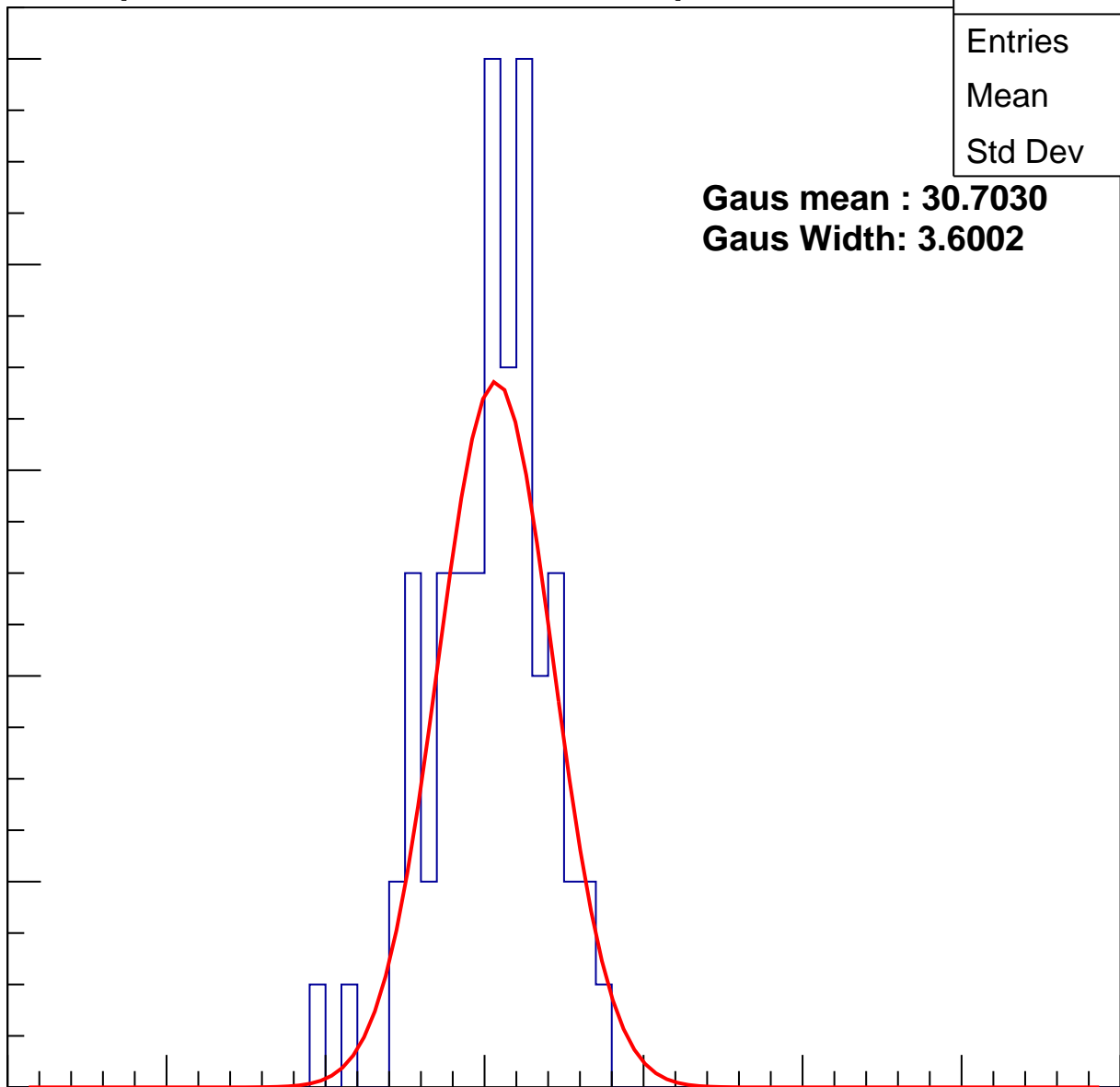
**Gaus Width: 3.6002**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U8-ch69, adc1

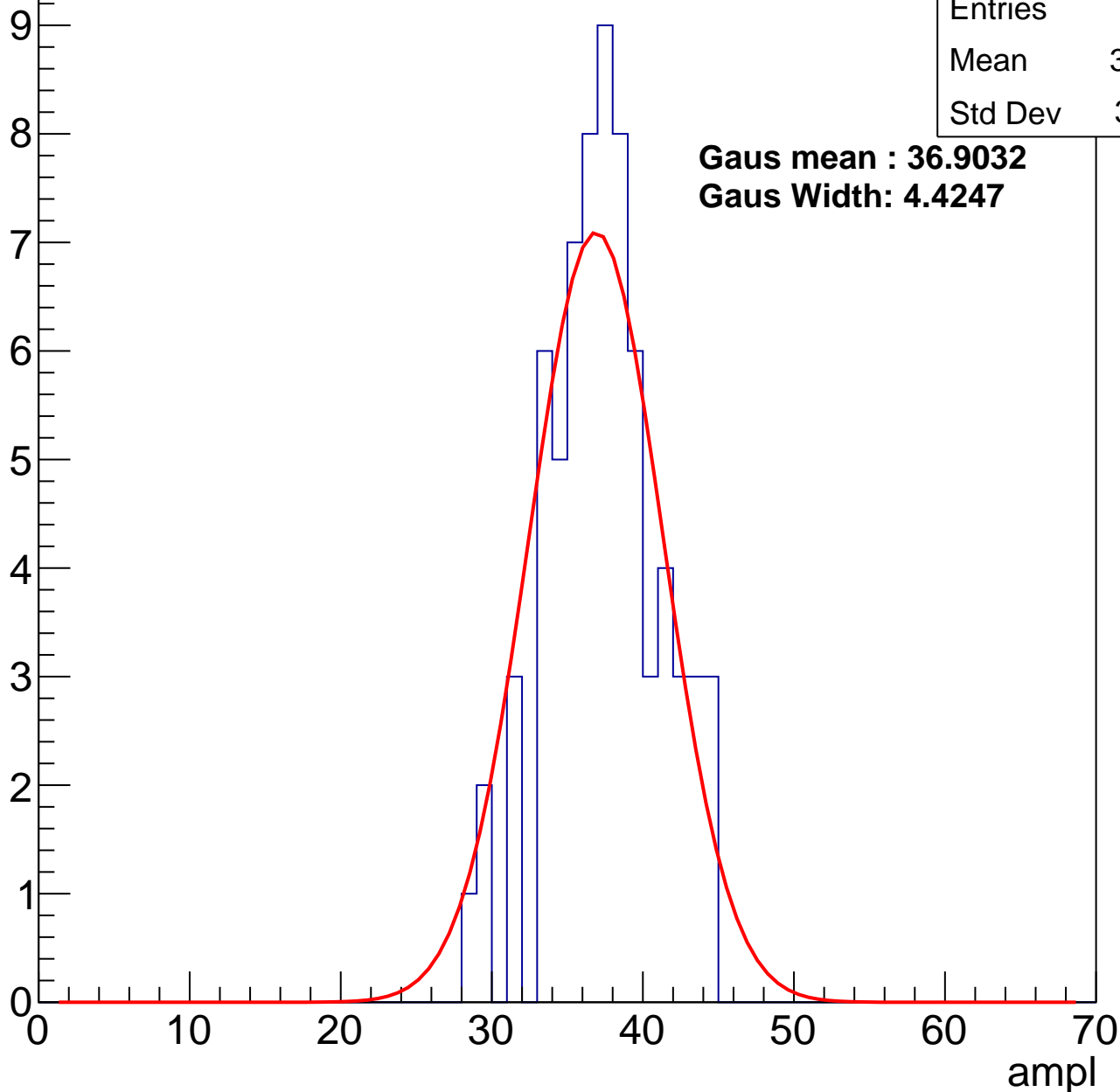
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	36.93
Std Dev	3.651

**Gaus mean : 36.9032**

**Gaus Width: 4.4247**



# B1L101S, U8-ch69, adc2

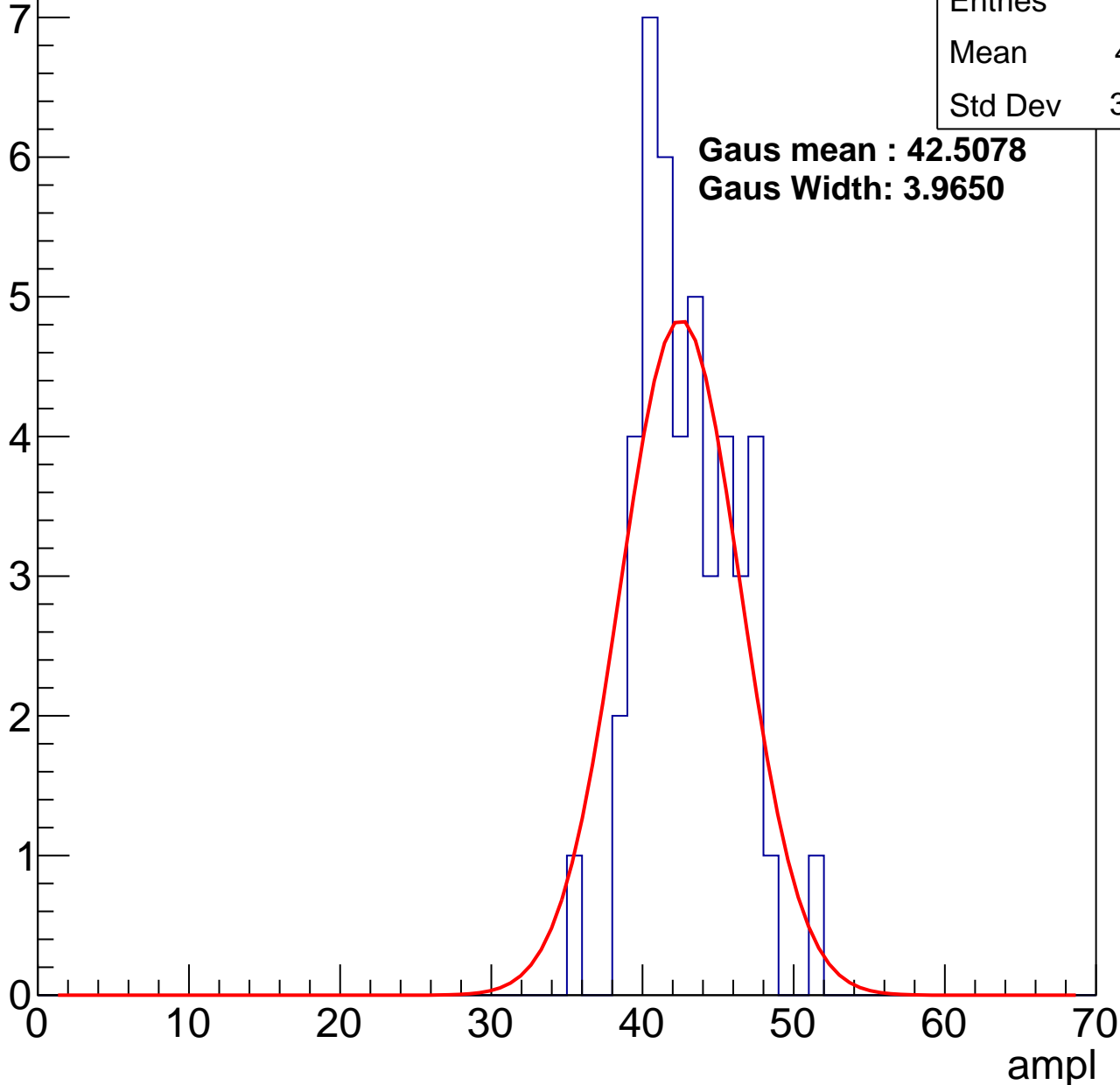
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	42.51
Std Dev	3.188

**Gaus mean : 42.5078**

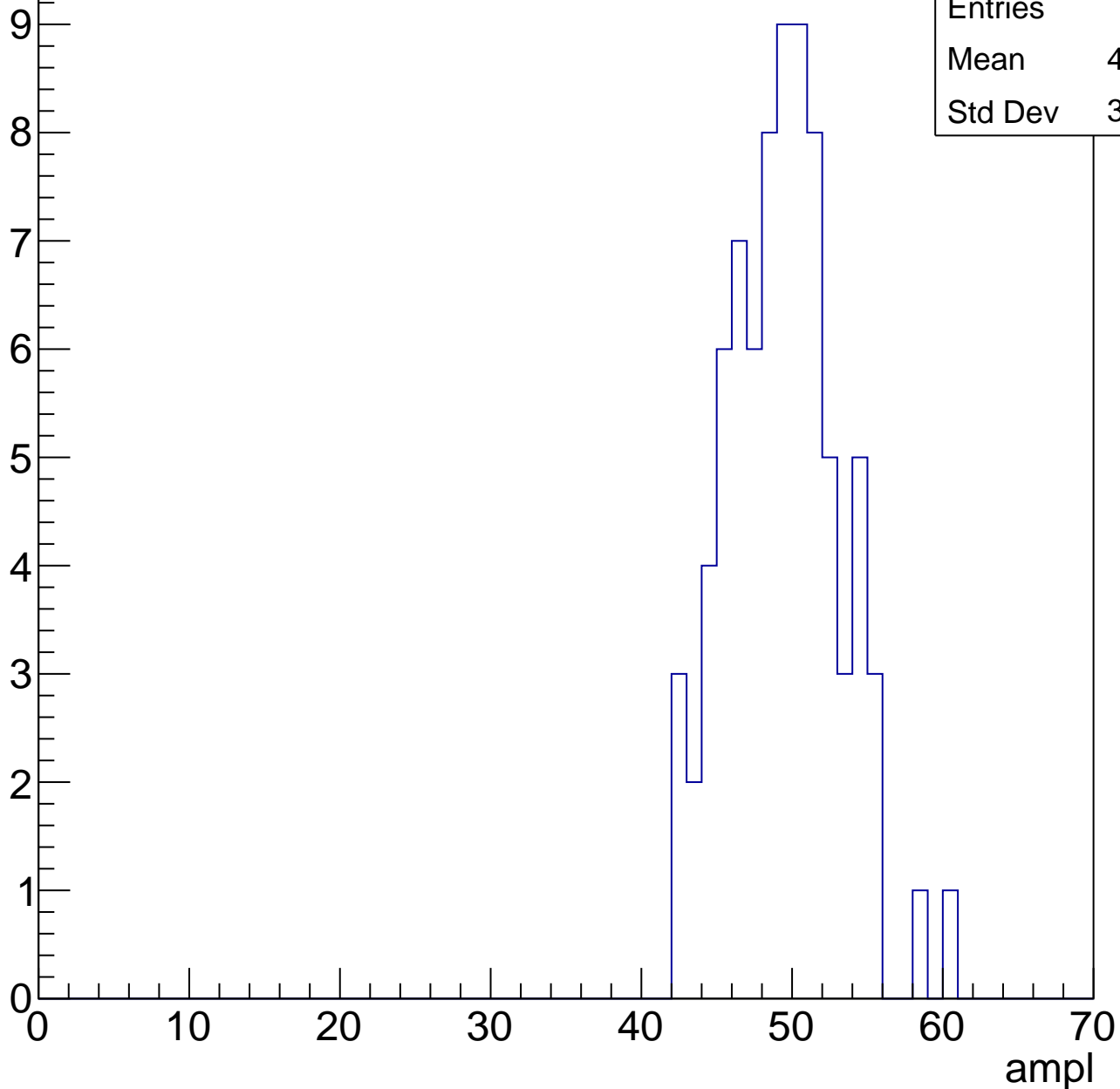
**Gaus Width: 3.9650**



# B1L101S, U8-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

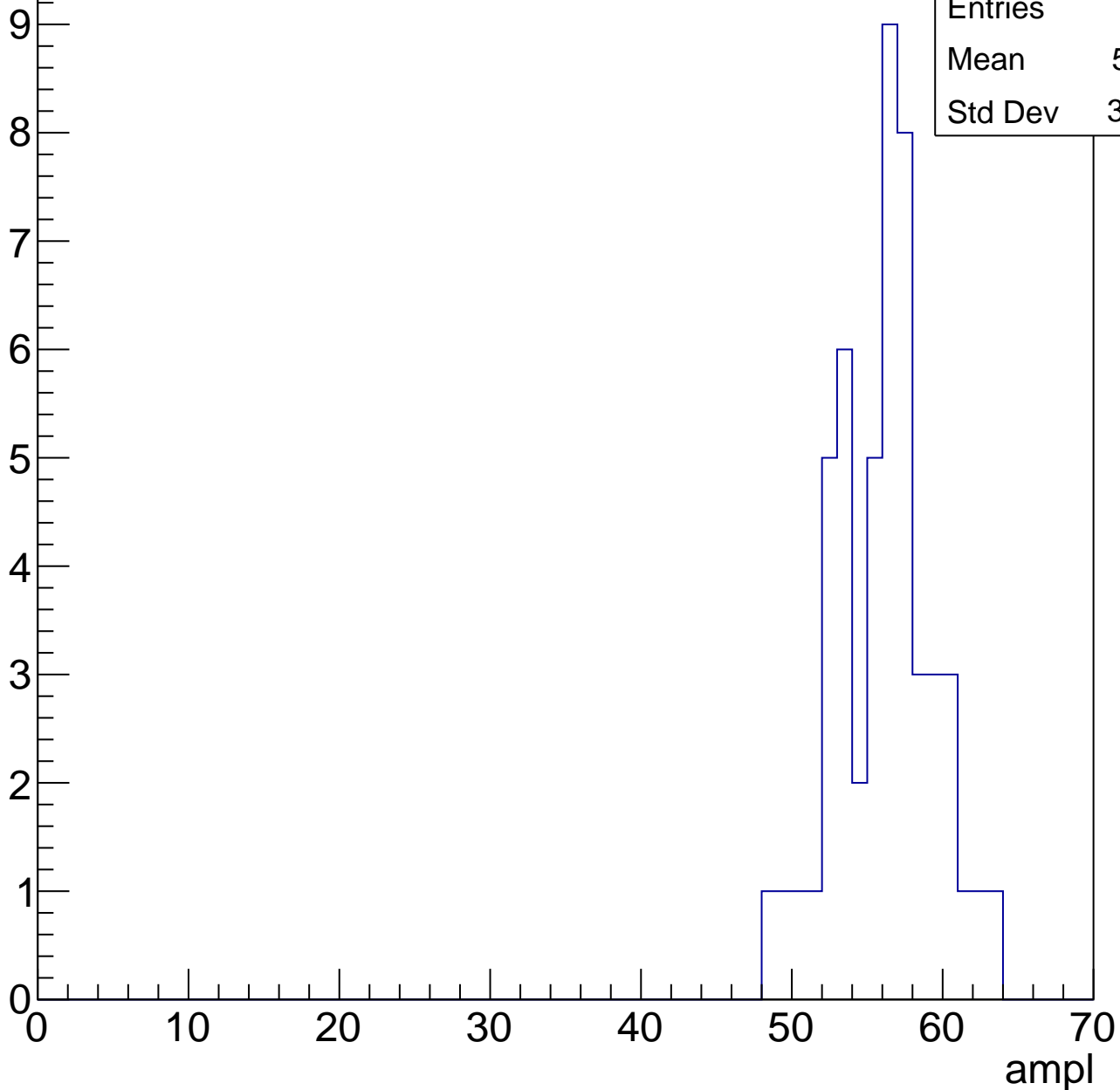


# B1L101S, U8-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	55.61
Std Dev	3.187



# B1L101S, U8-ch69, adc5

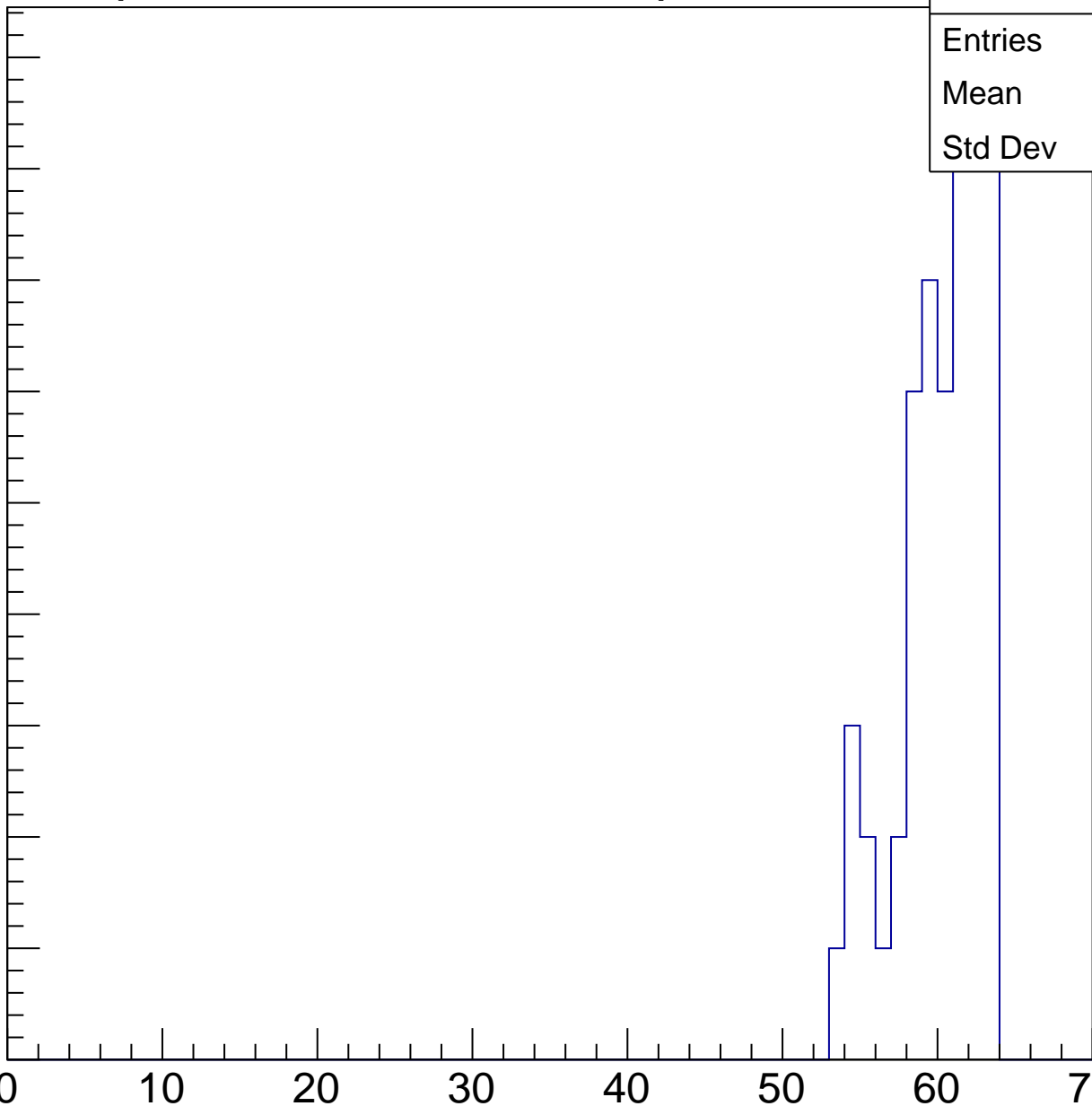
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	53
Mean	59.72
Std Dev	2.68

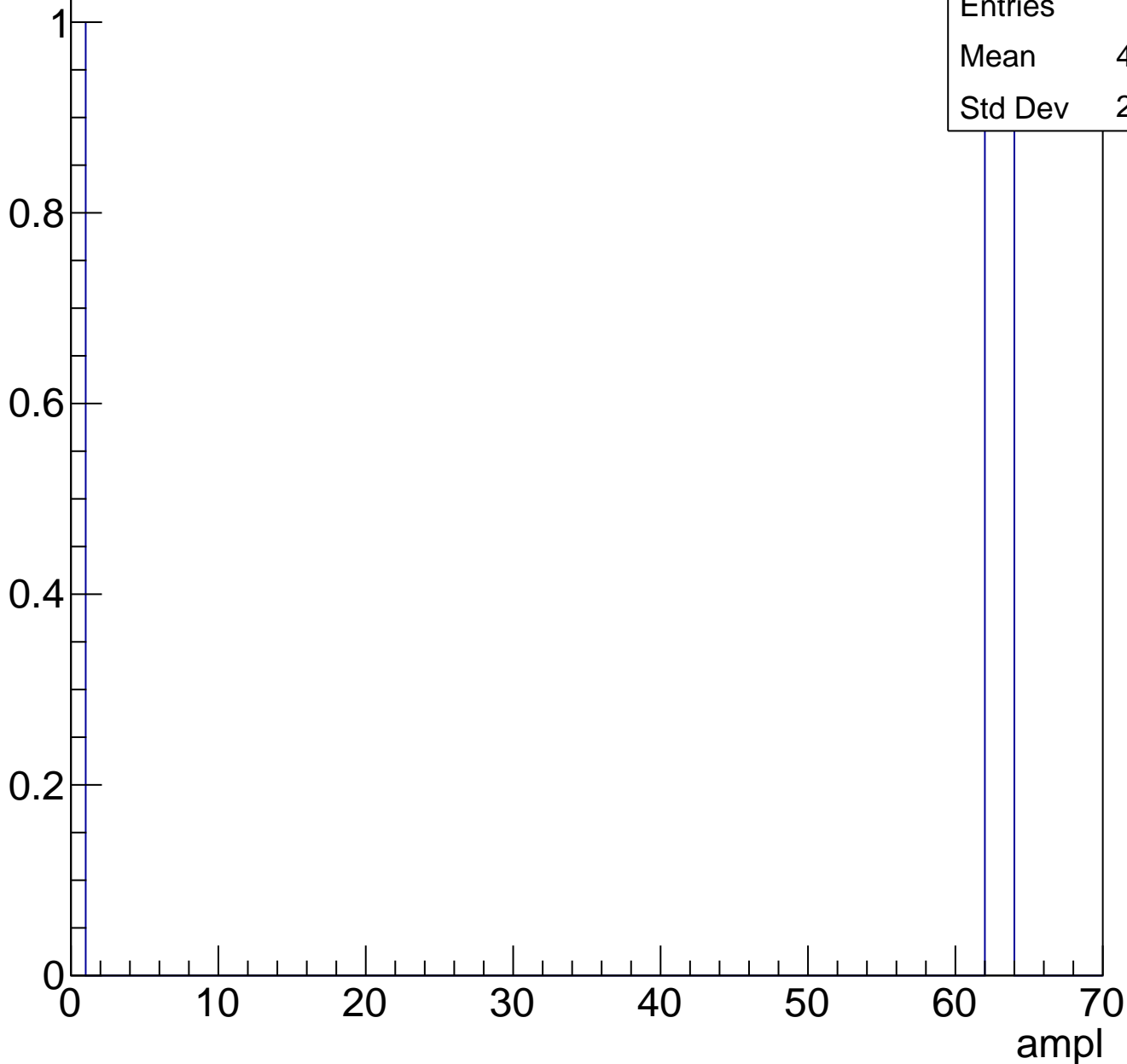
ampl



# B1L101S, U8-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U8-ch70, adc0

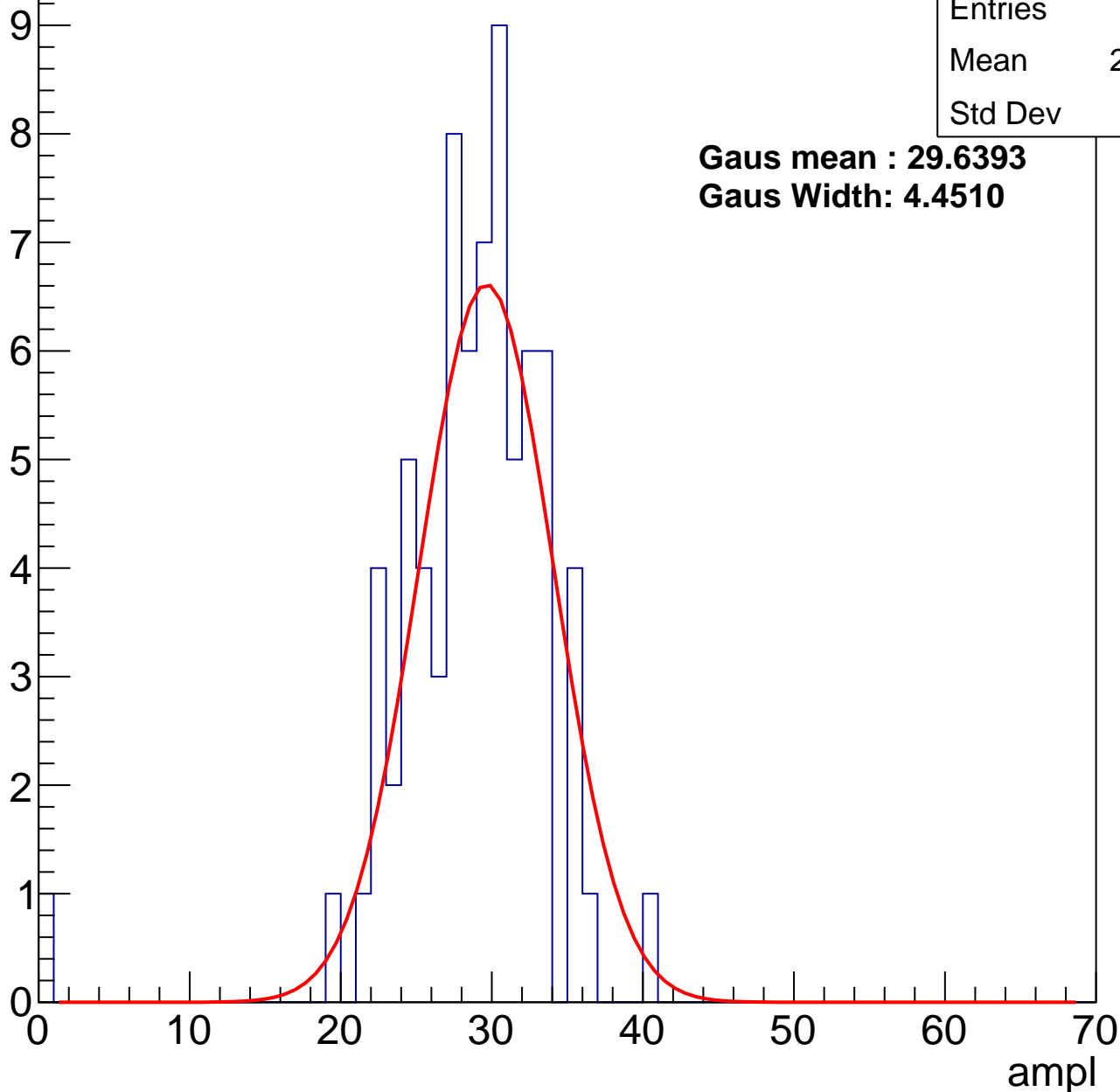
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	28.24
Std Dev	5.17

**Gaus mean : 29.6393**

**Gaus Width: 4.4510**



# B1L101S, U8-ch70, adc1

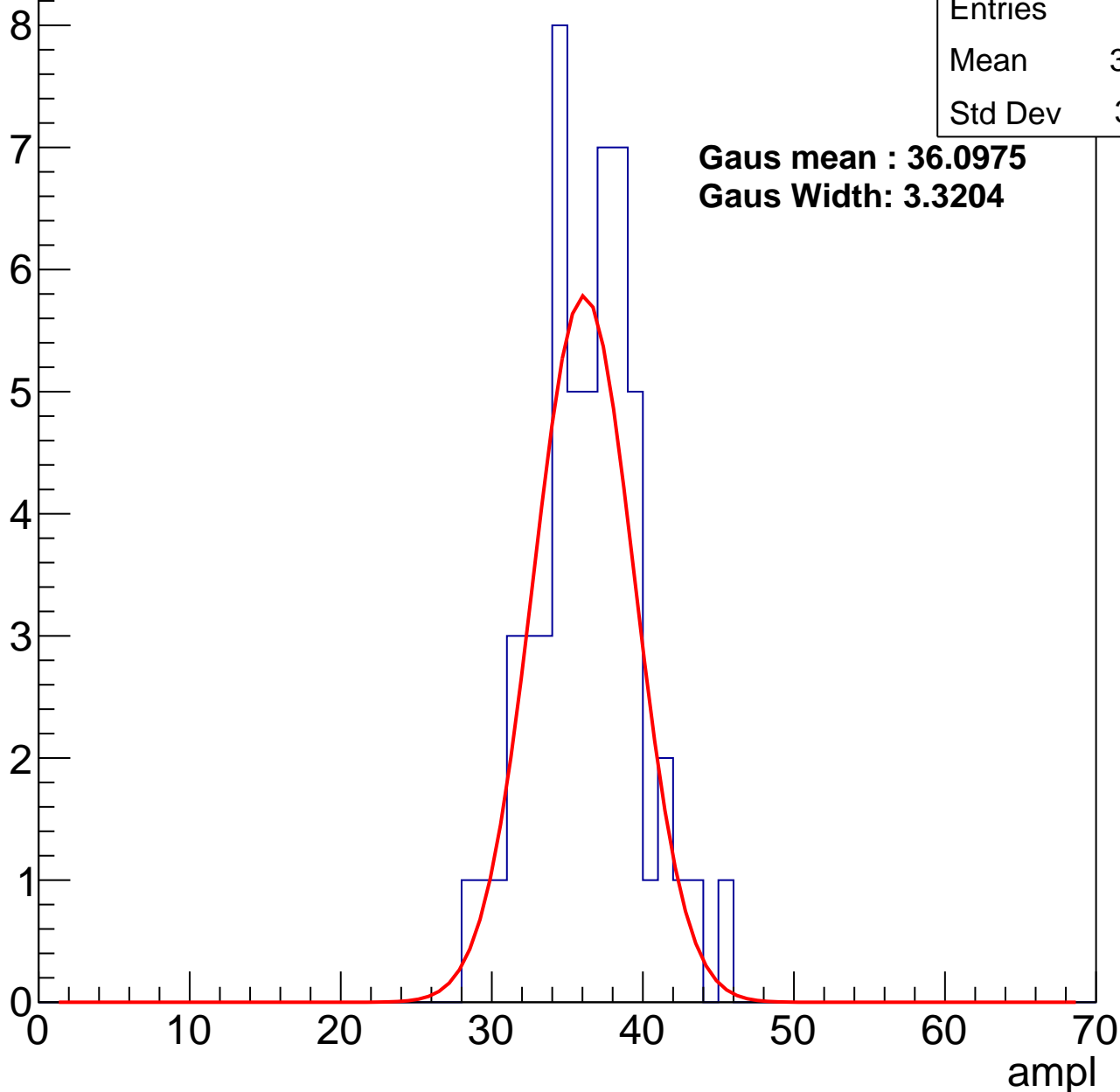
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	35.89
Std Dev	3.431

**Gaus mean : 36.0975**

**Gaus Width: 3.3204**



# B1L101S, U8-ch70, adc2

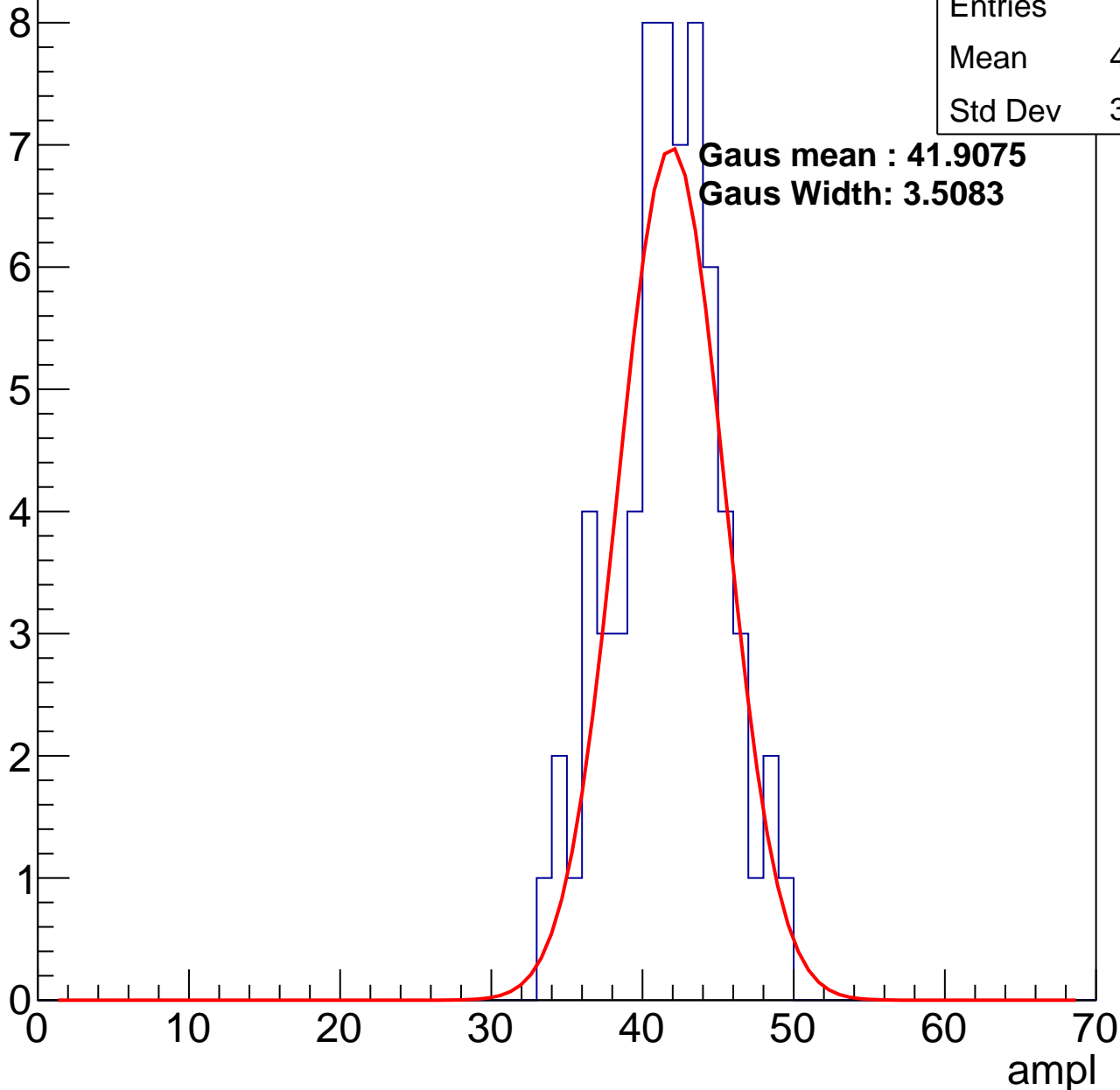
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	41.23
Std Dev	3.533

**Gaus mean : 41.9075**

**Gaus Width: 3.5083**

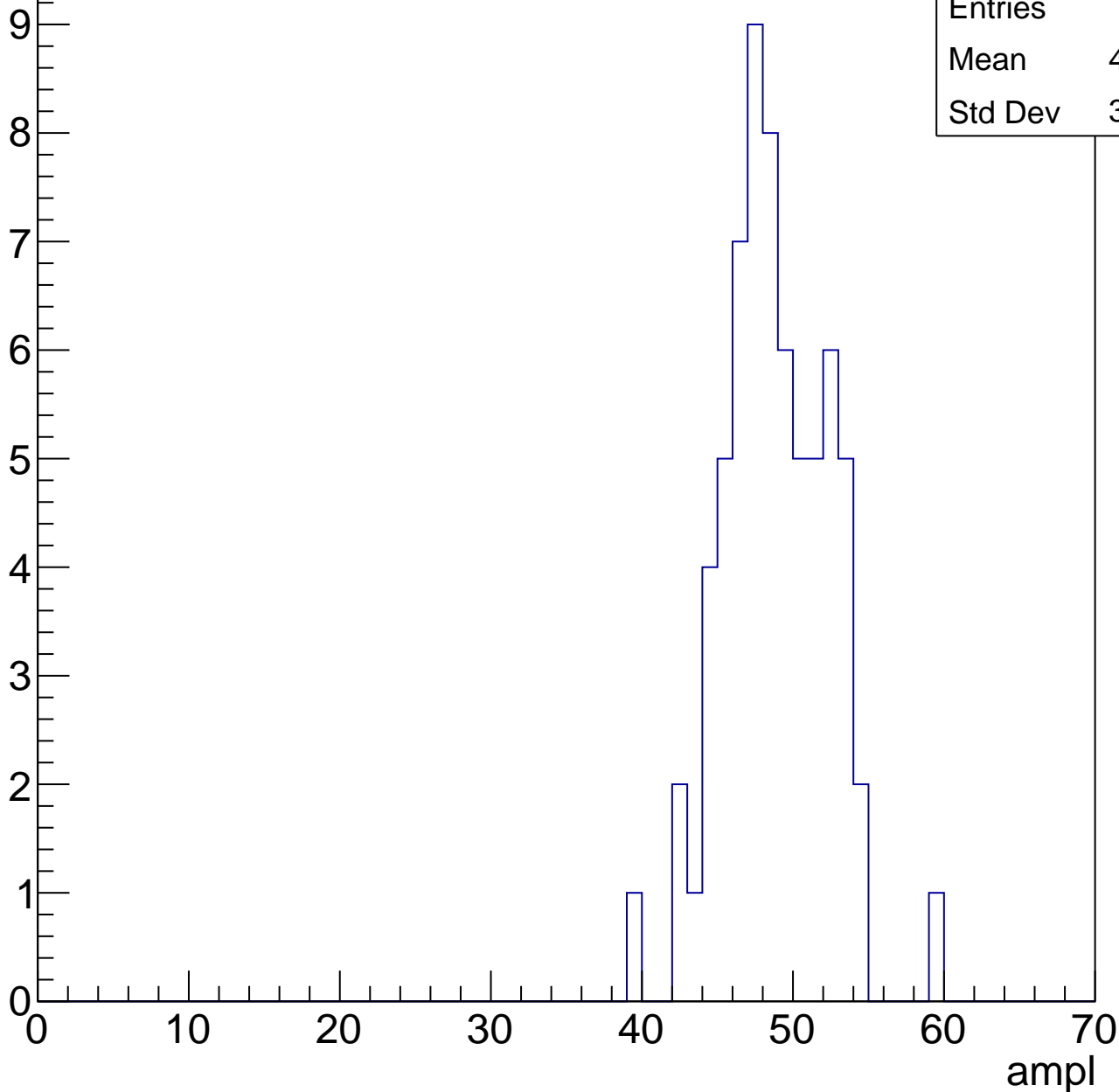


# B1L101S, U8-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

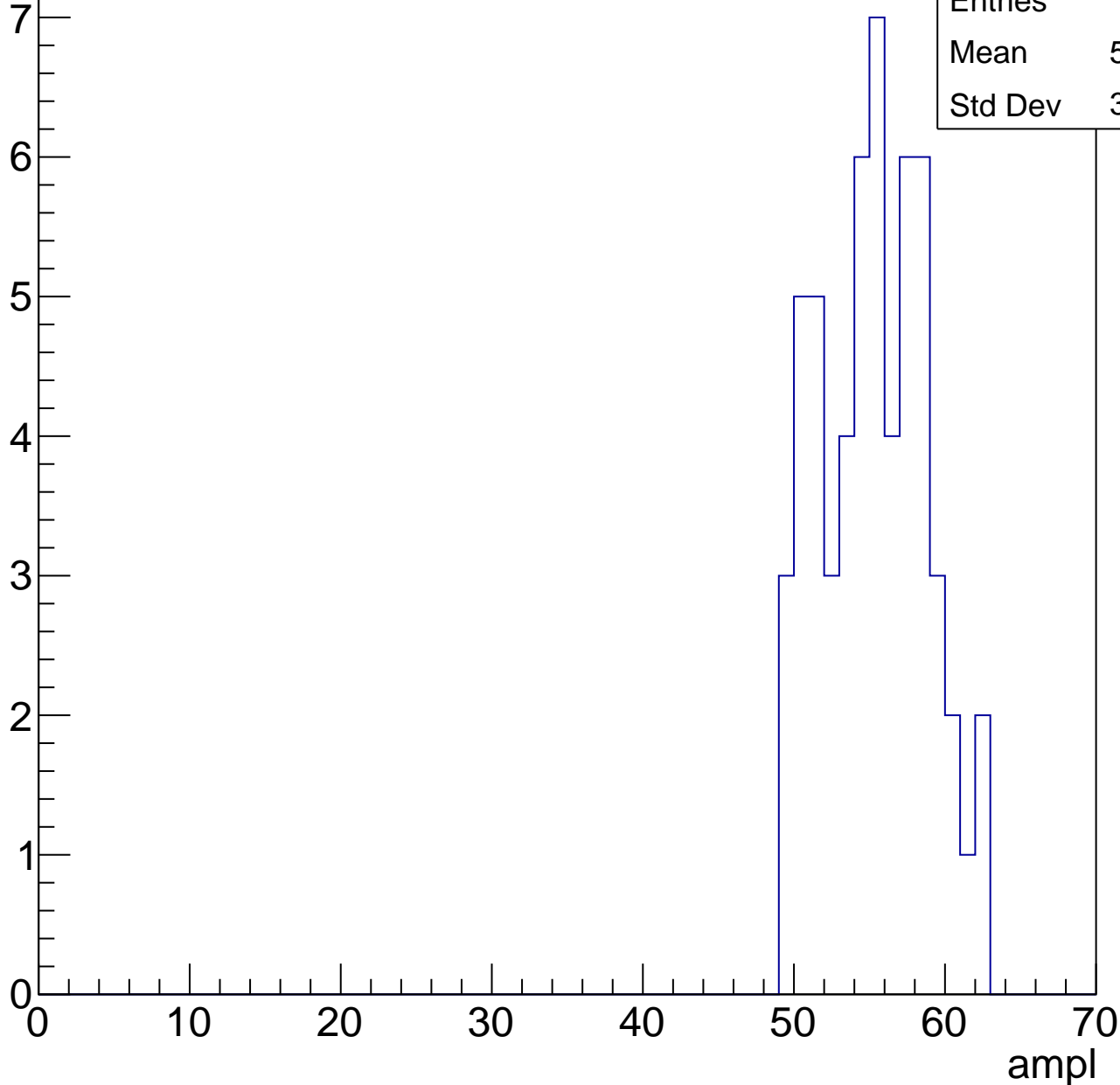
Entries	67
Mean	48.34
Std Dev	3.458



# B1L101S, U8-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

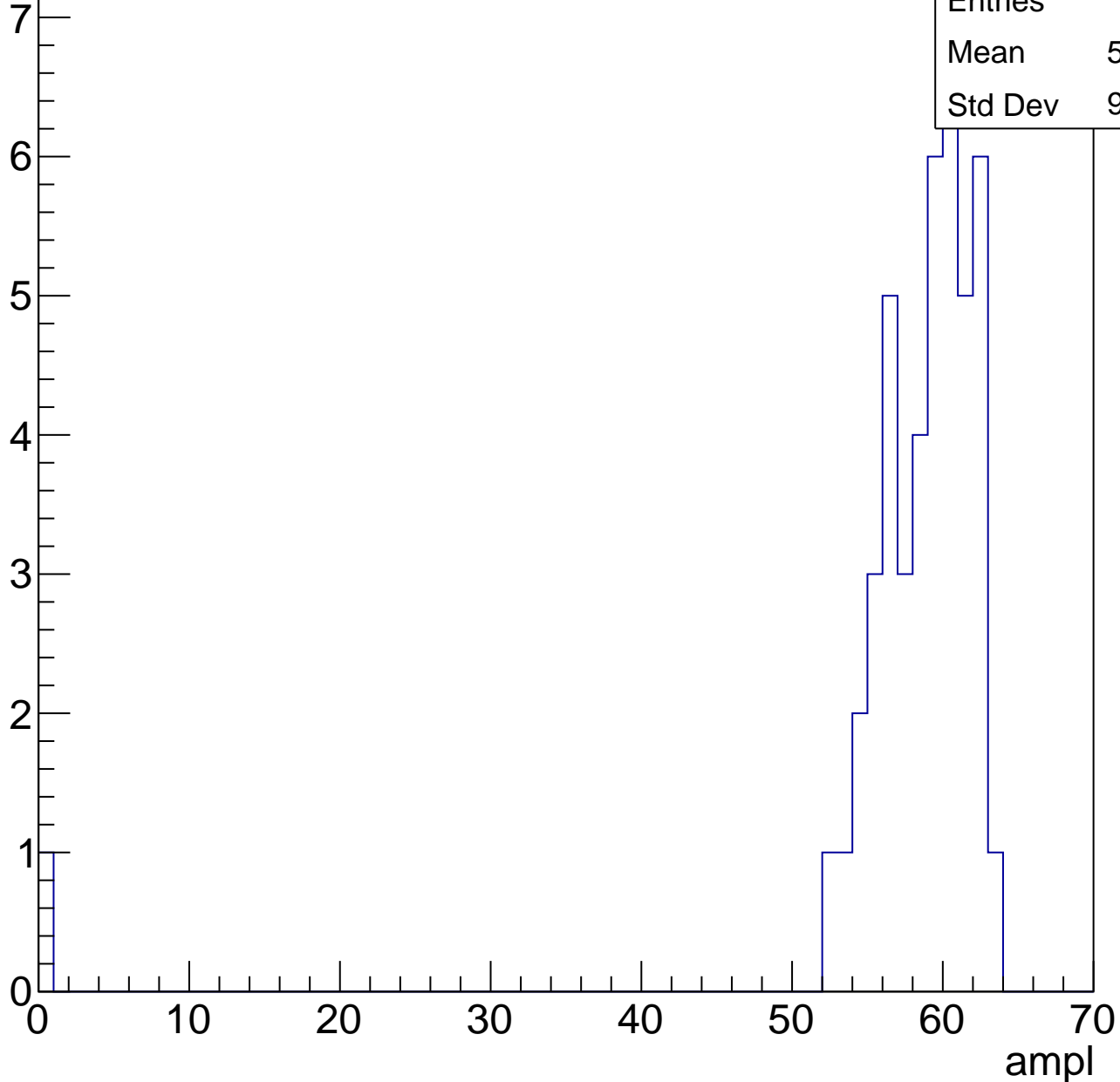
Entry



# B1L101S, U8-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

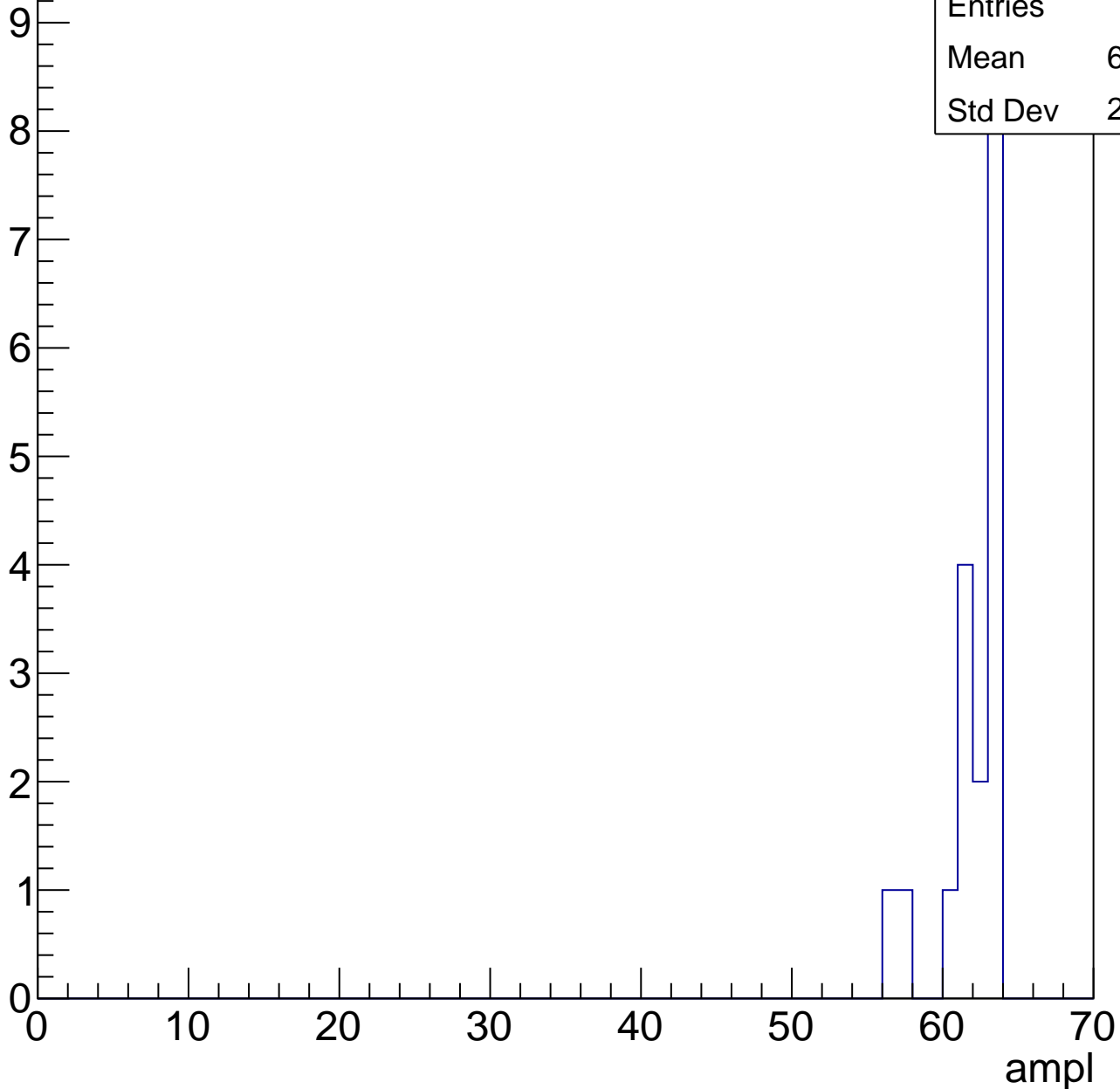


# B1L101S, U8-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	18
Mean	61.56
Std Dev	2.034





# B1L101S, U8-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U8-ch71, adc0

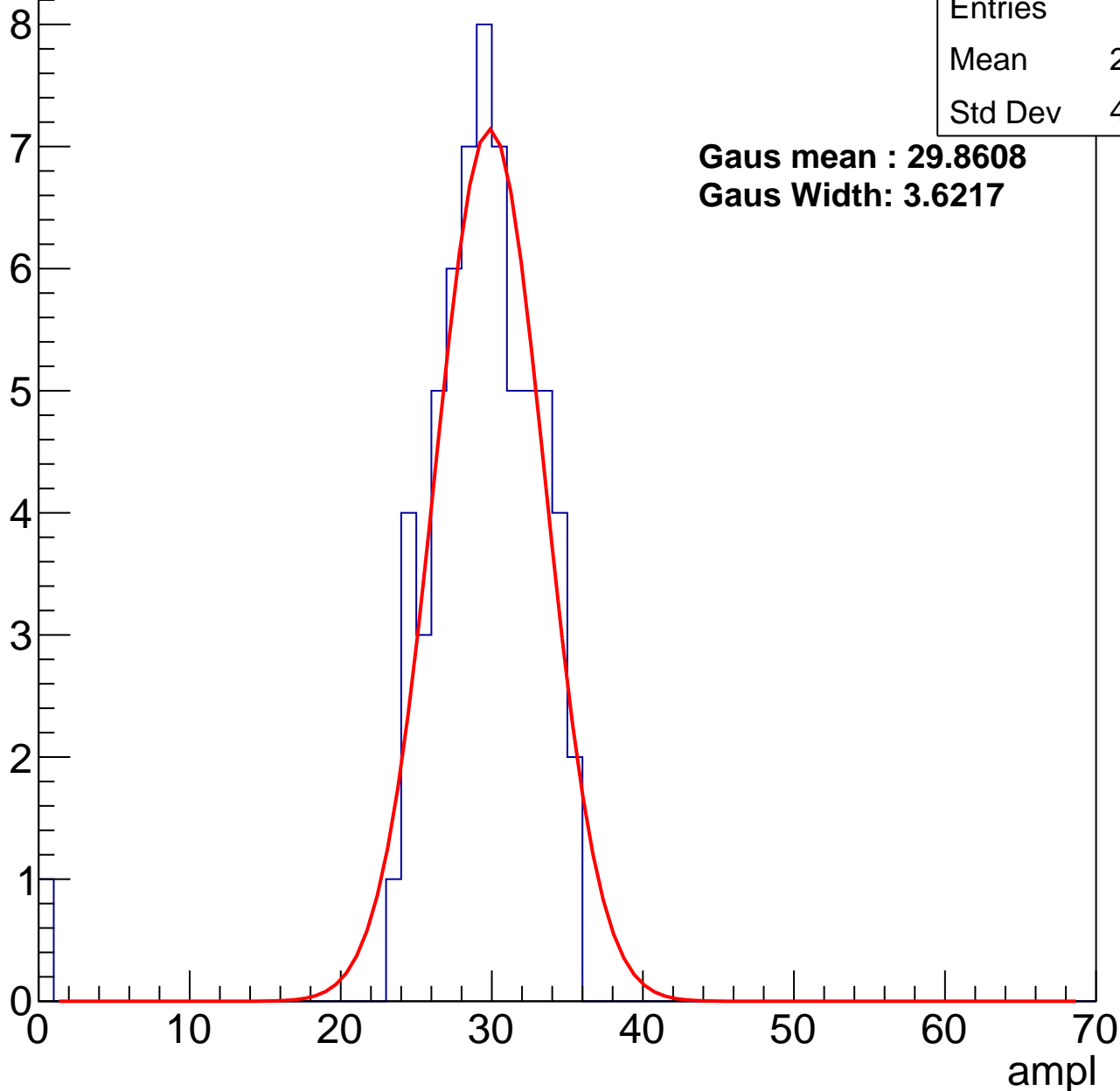
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	28.73
Std Dev	4.748

**Gaus mean : 29.8608**

**Gaus Width: 3.6217**



# B1L101S, U8-ch71, adc1

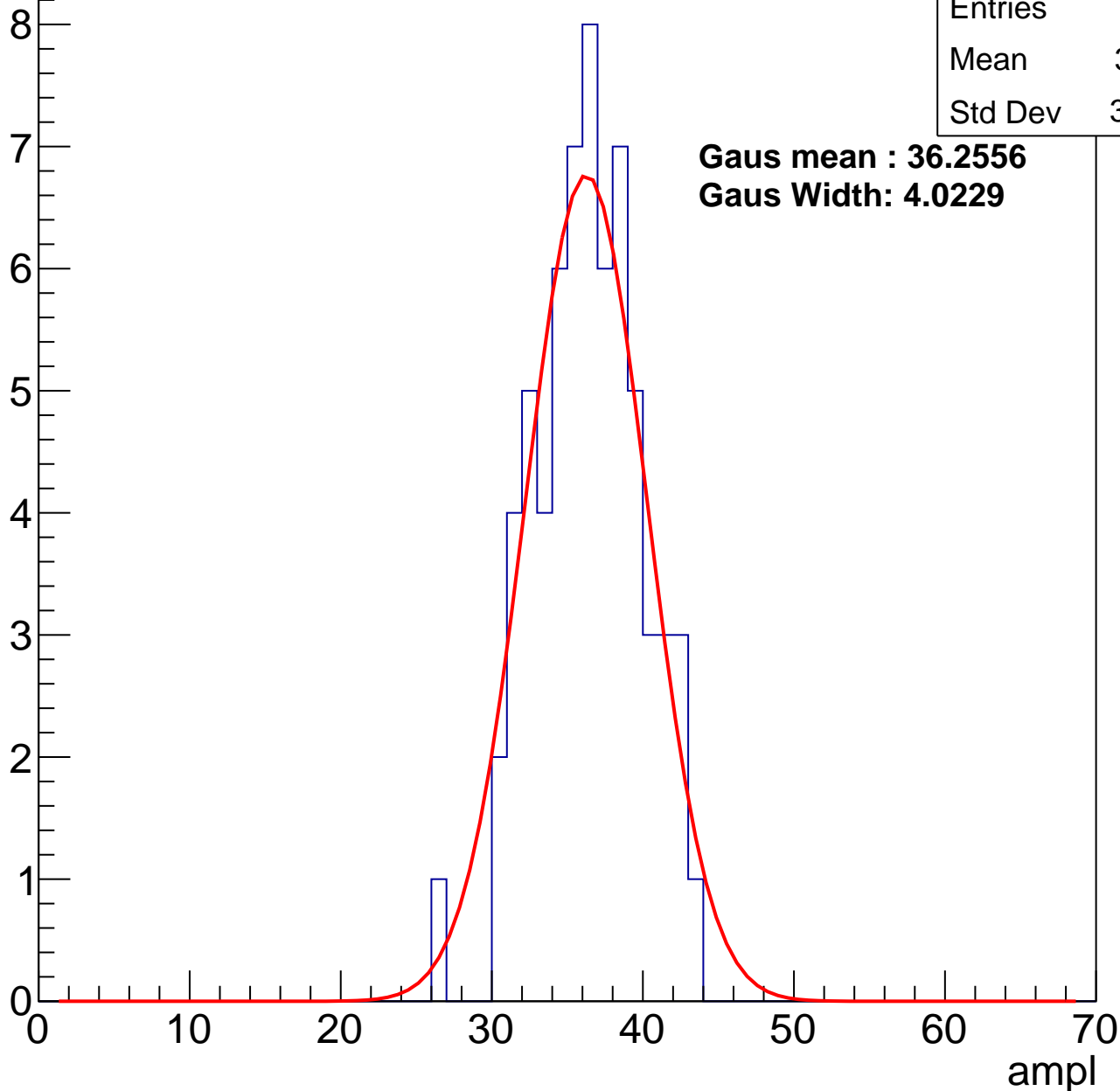
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	35.91
Std Dev	3.458

**Gaus mean : 36.2556**

**Gaus Width: 4.0229**



# B1L101S, U8-ch71, adc2

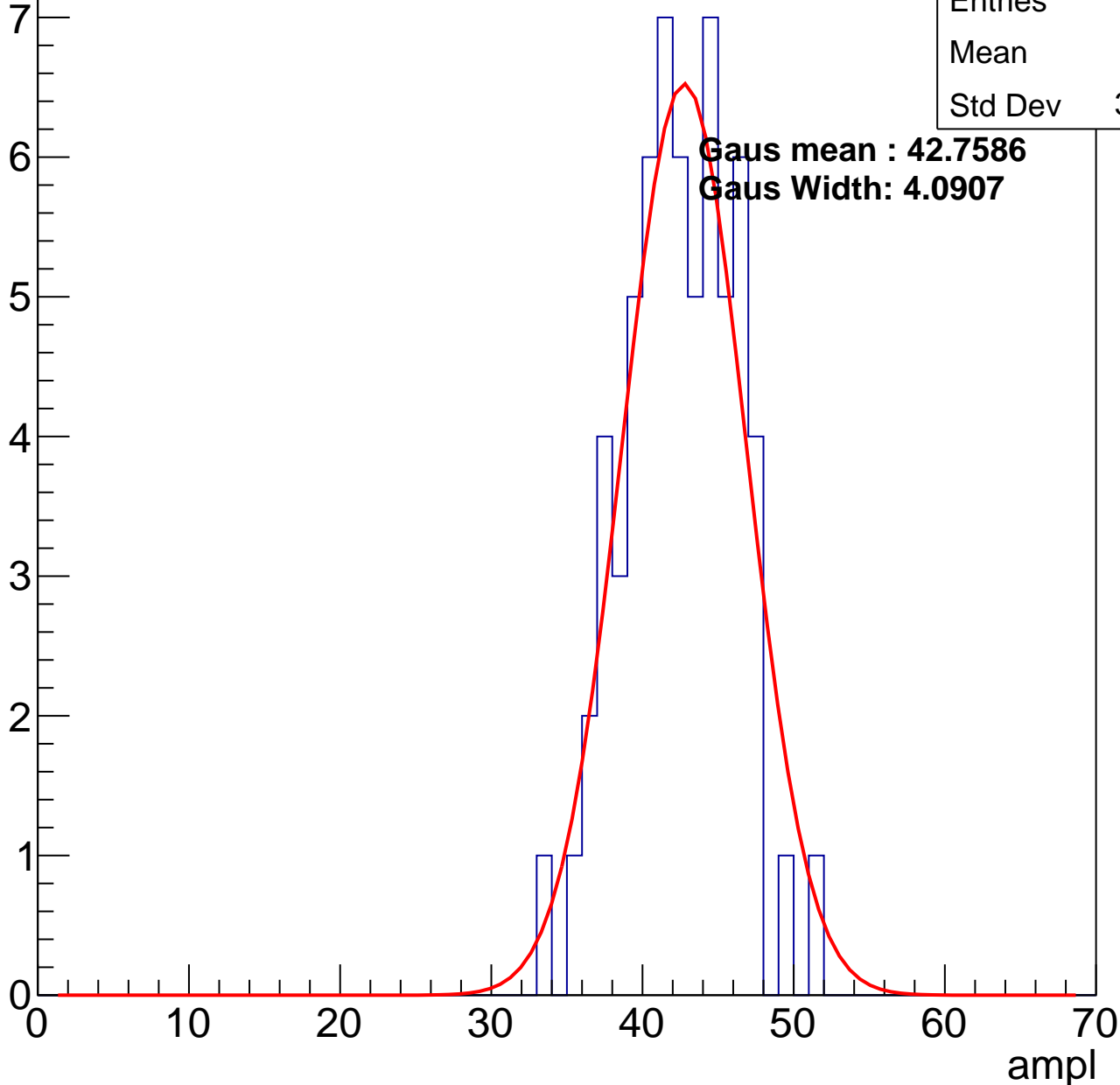
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	42
Std Dev	3.601

**Gaus mean : 42.7586**

**Gaus Width: 4.0907**

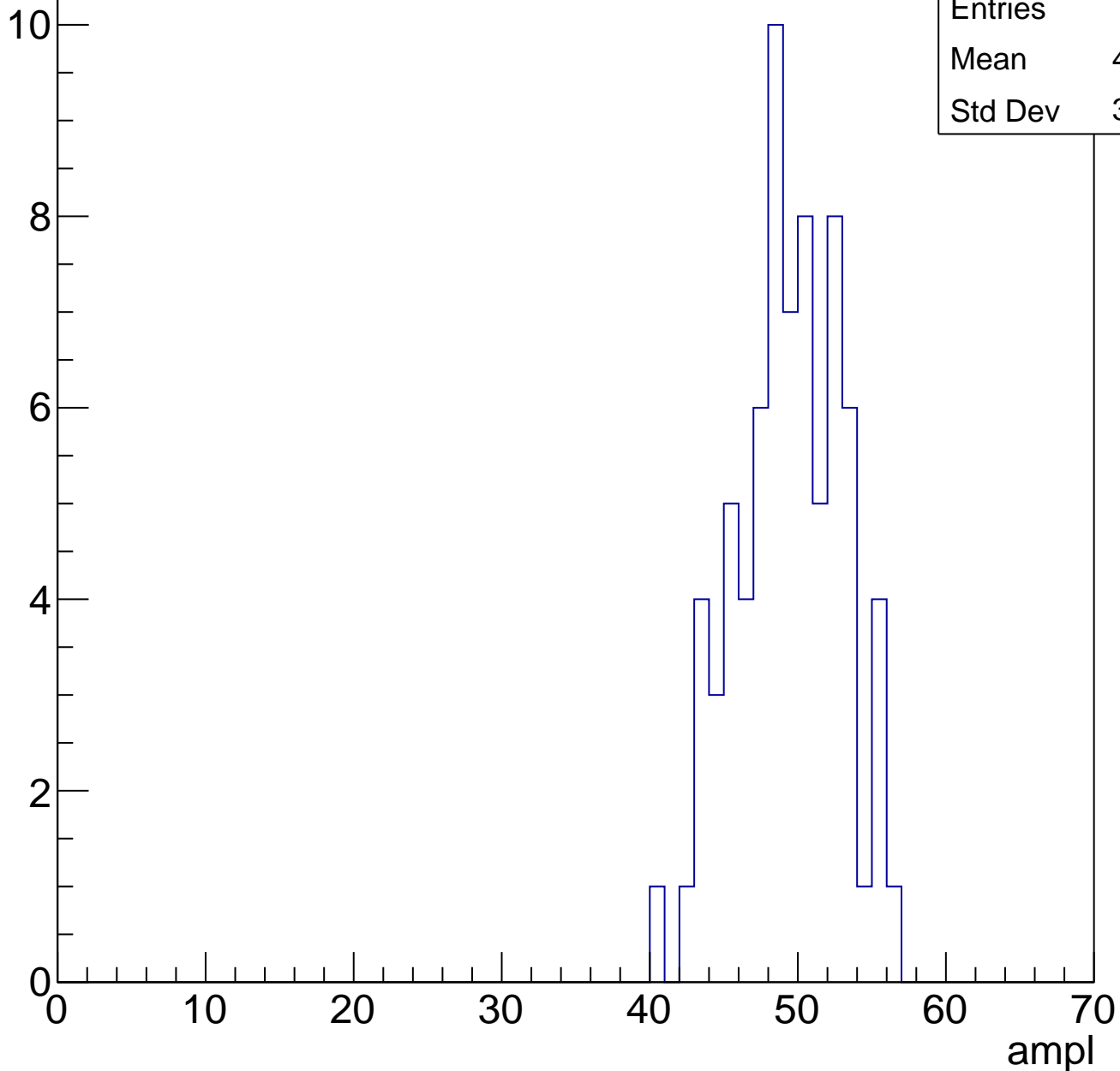


# B1L101S, U8-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

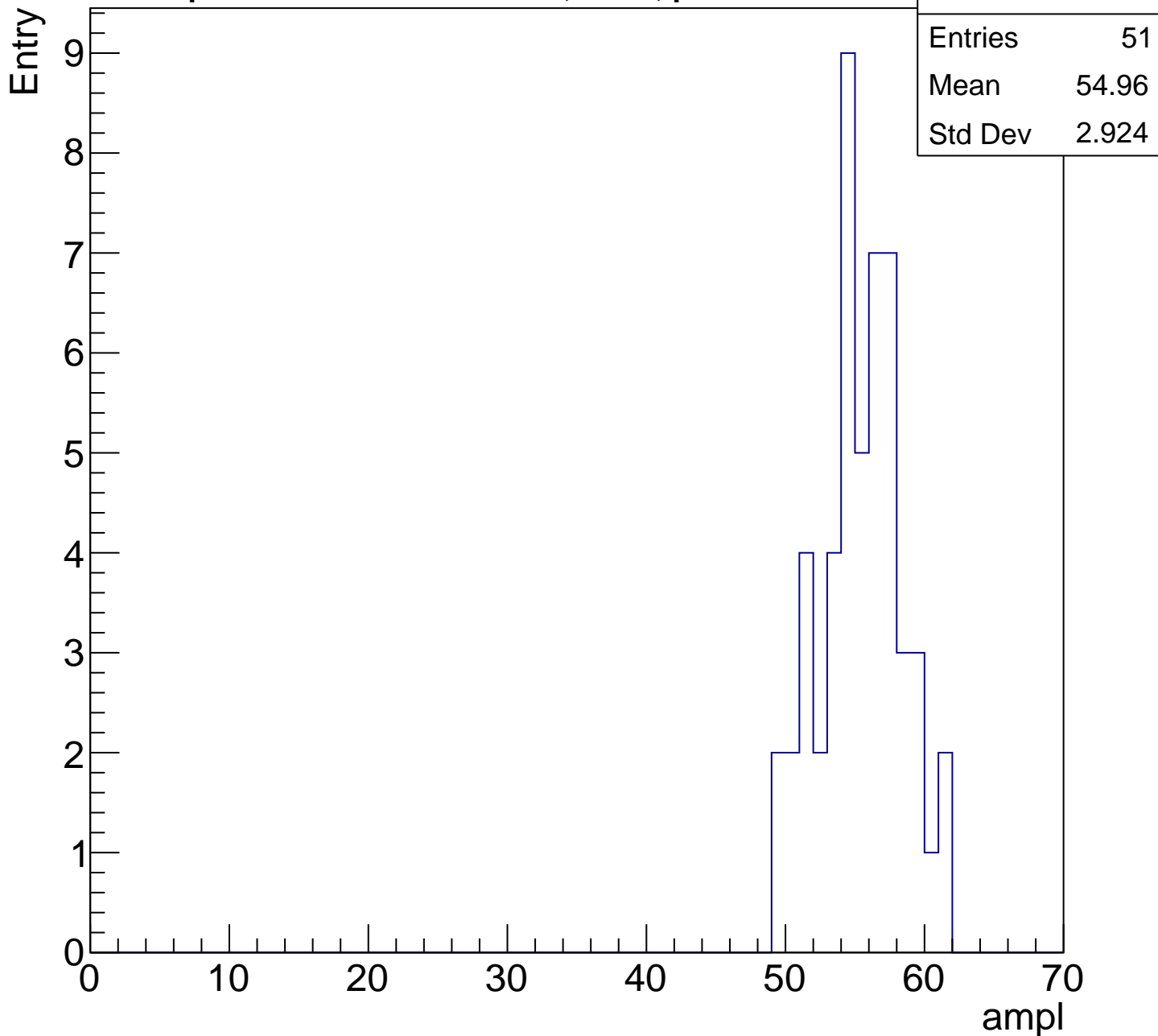
Entries	74
Mean	48.91
Std Dev	3.511

Entry



# B1L101S, U8-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U8-ch71, adc5

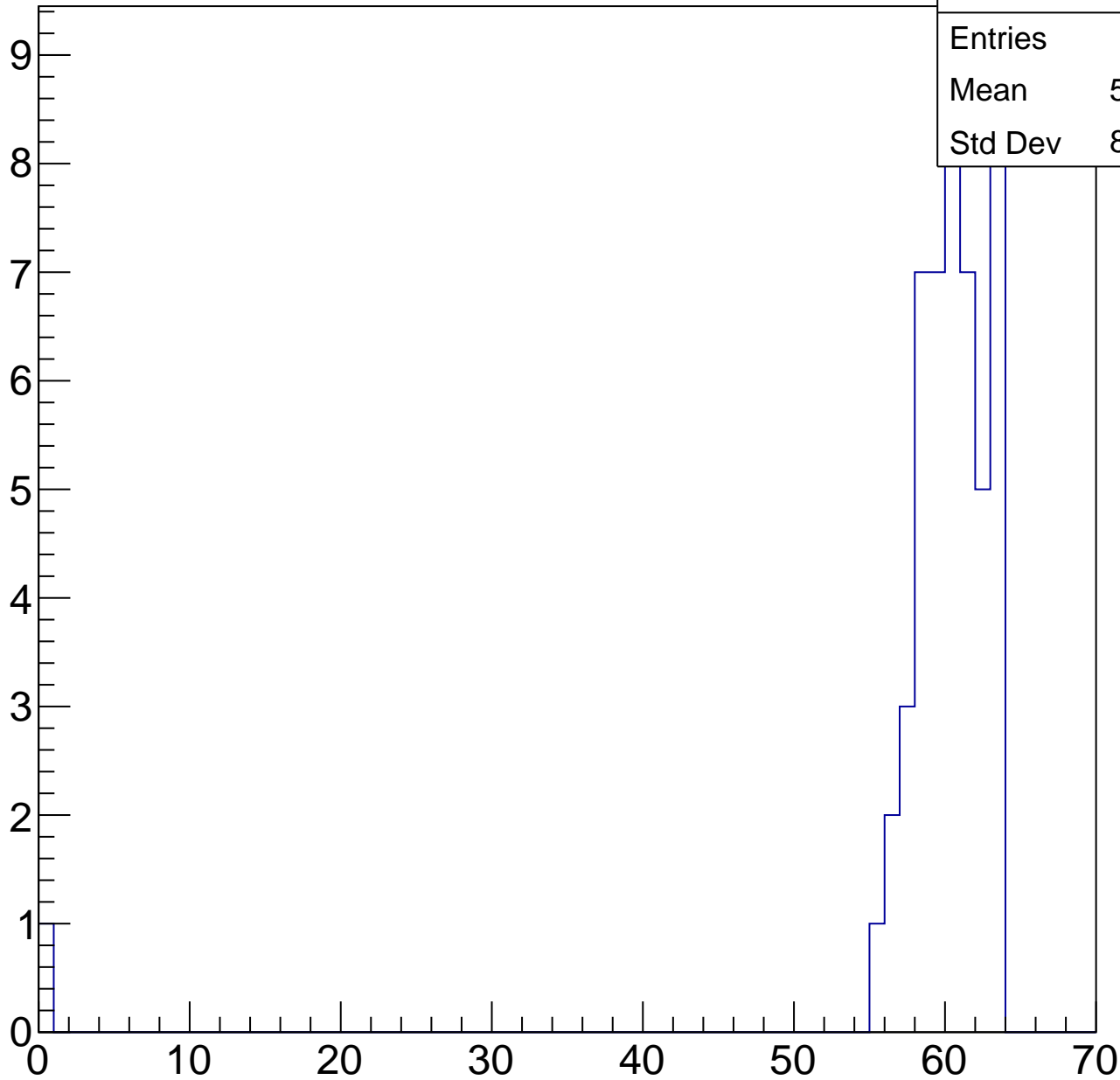
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	50
Mean	58.82
Std Dev	8.669

ampl

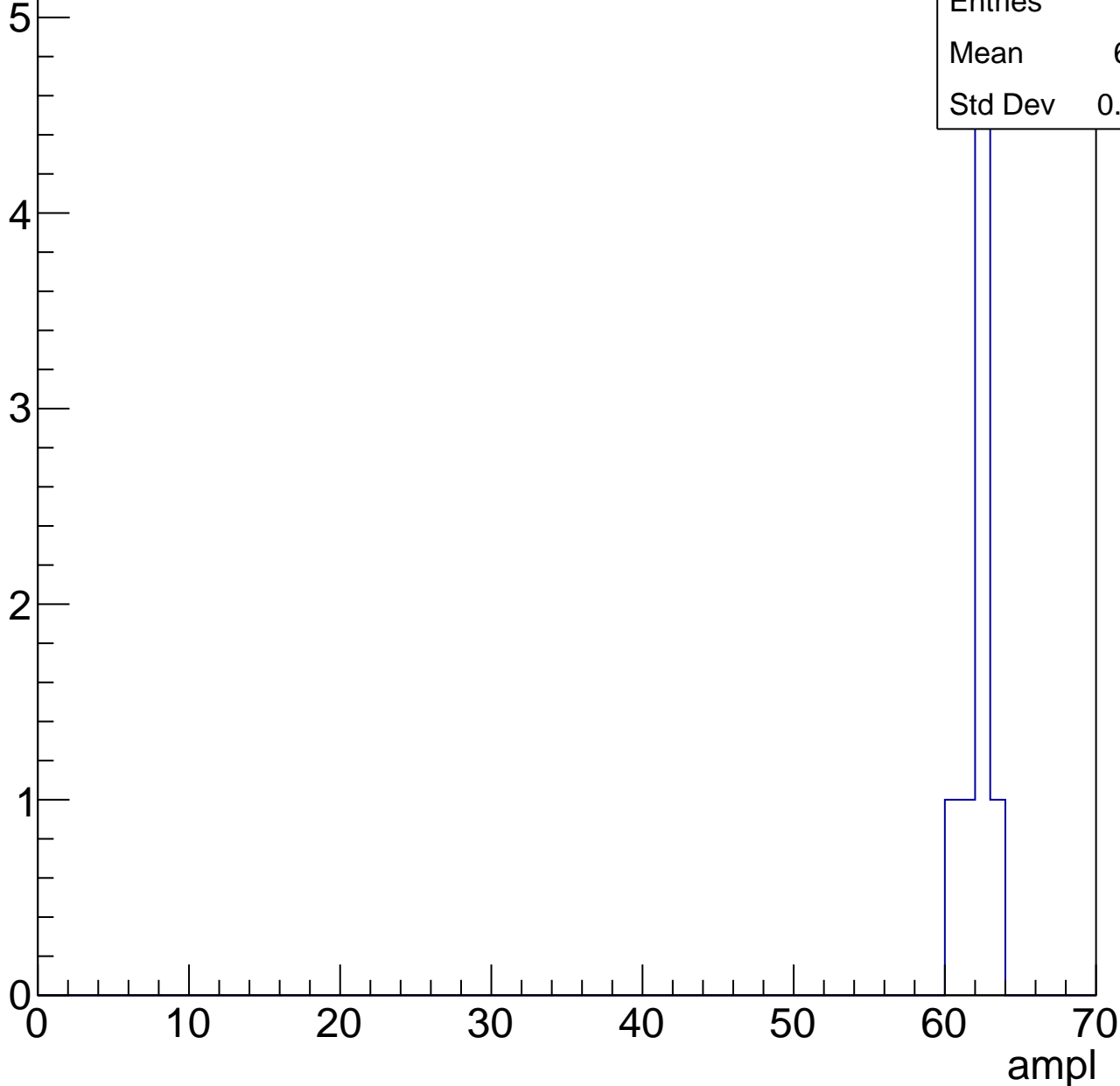


# B1L101S, U8-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	8
Mean	61.75
Std Dev	0.8292





# B1L101S, U8-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U8-ch72, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	68
Mean	27.63
Std Dev	4.527

**Gaus mean : 29.2012**

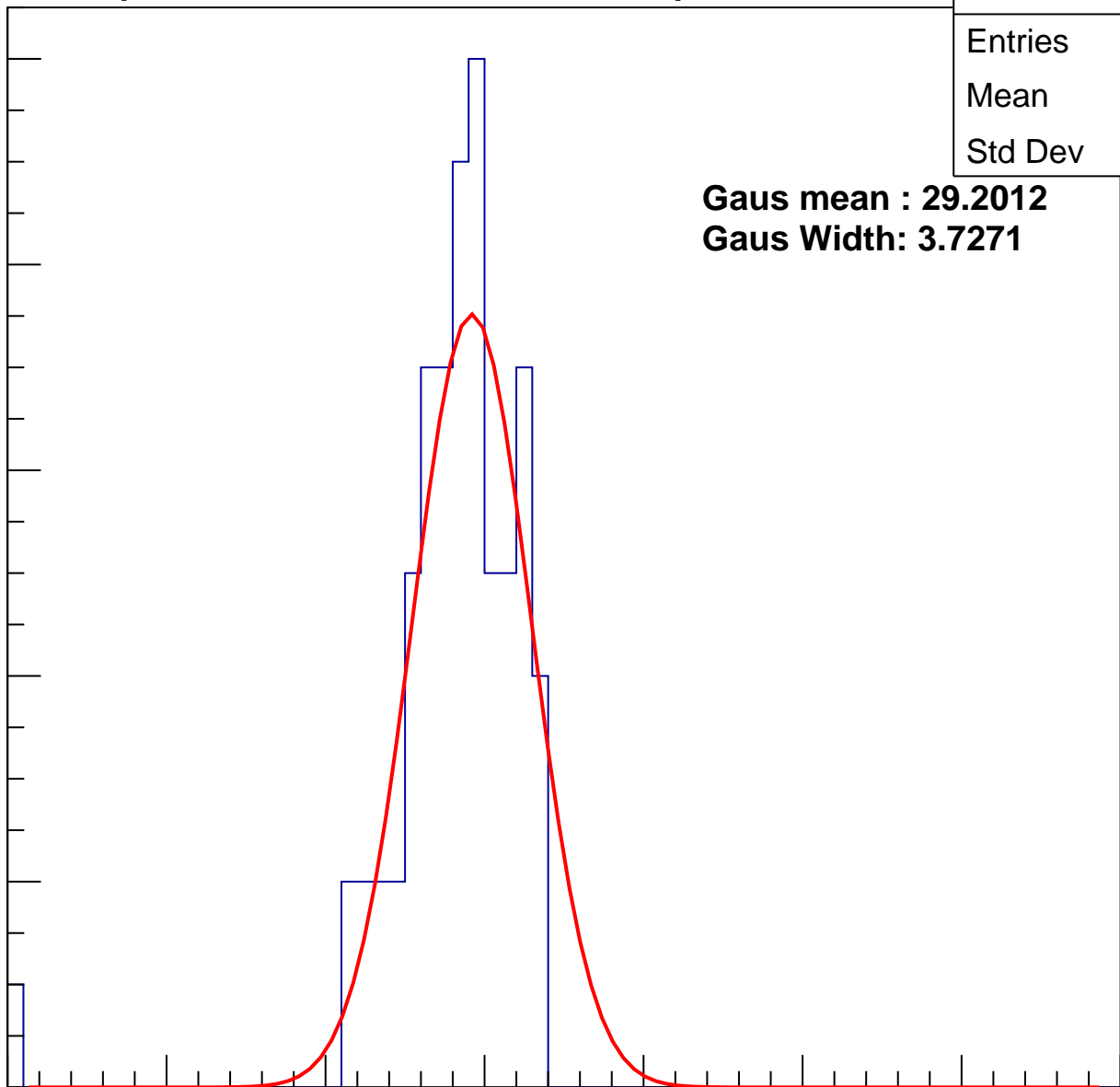
**Gaus Width: 3.7271**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U8-ch72, adc1

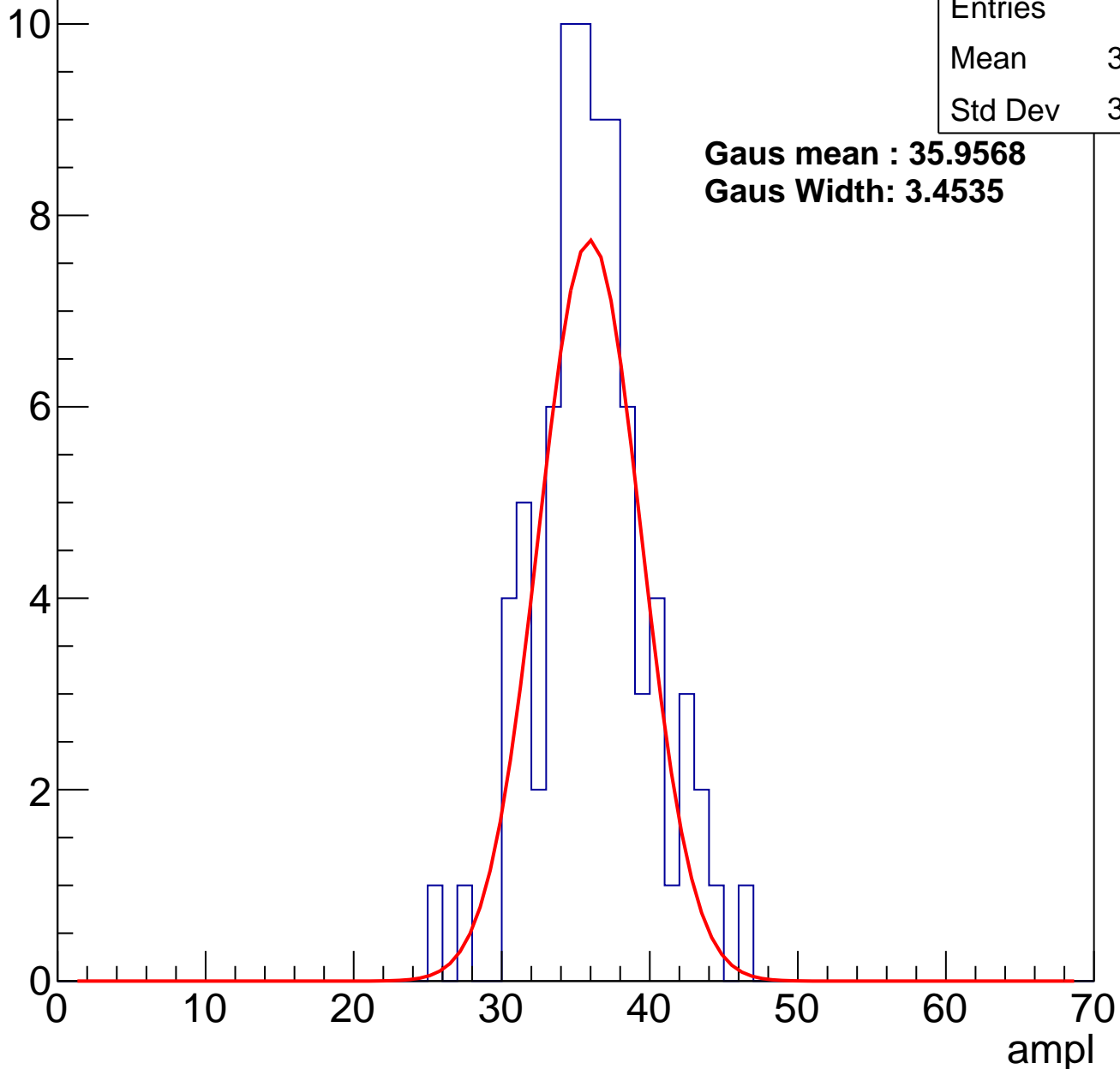
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	78
Mean	35.69
Std Dev	3.787

**Gaus mean : 35.9568**

**Gaus Width: 3.4535**

Entry



# B1L101S, U8-ch72, adc2

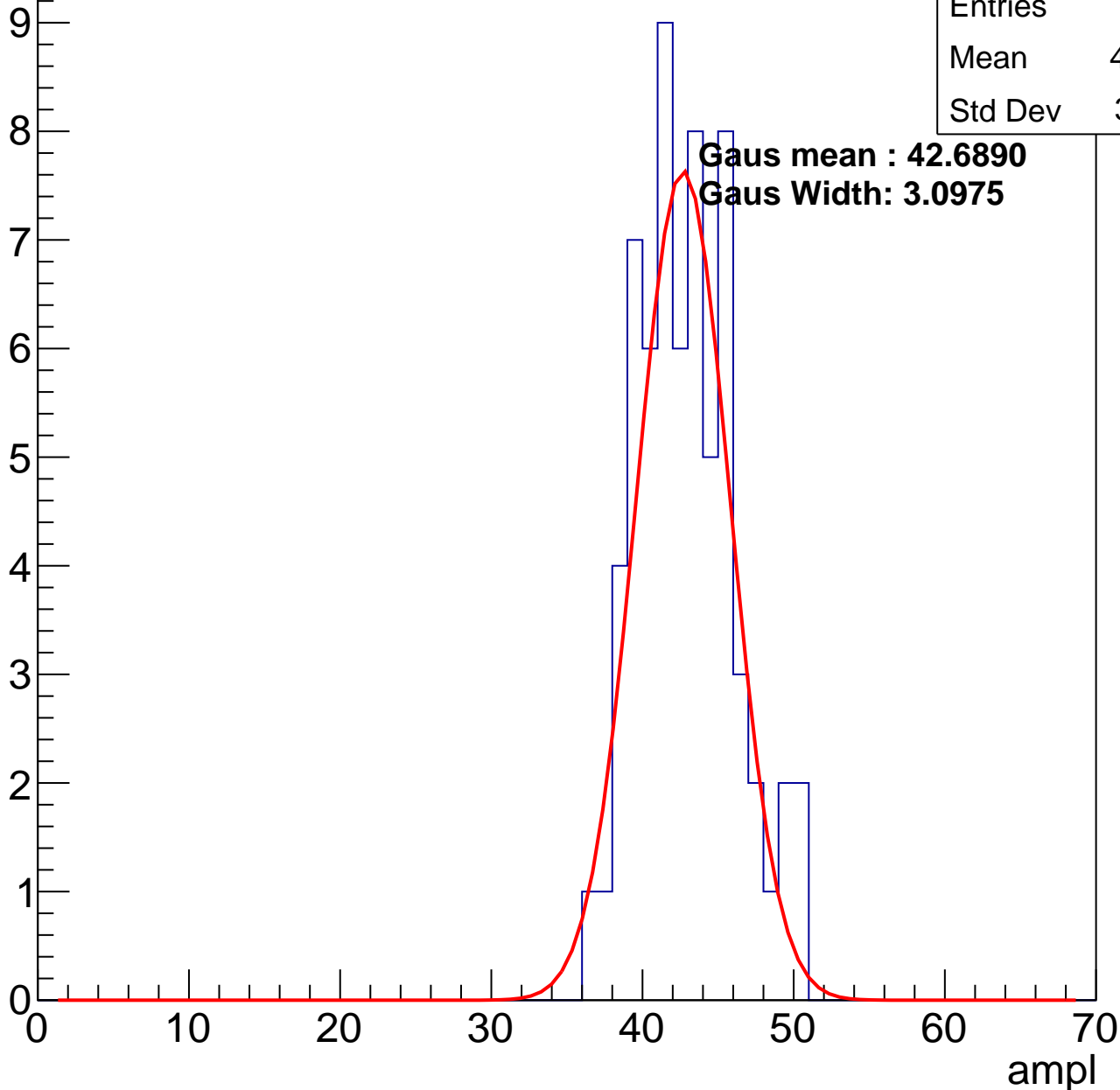
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	42.48
Std Dev	3.201

**Gaus mean : 42.6890**

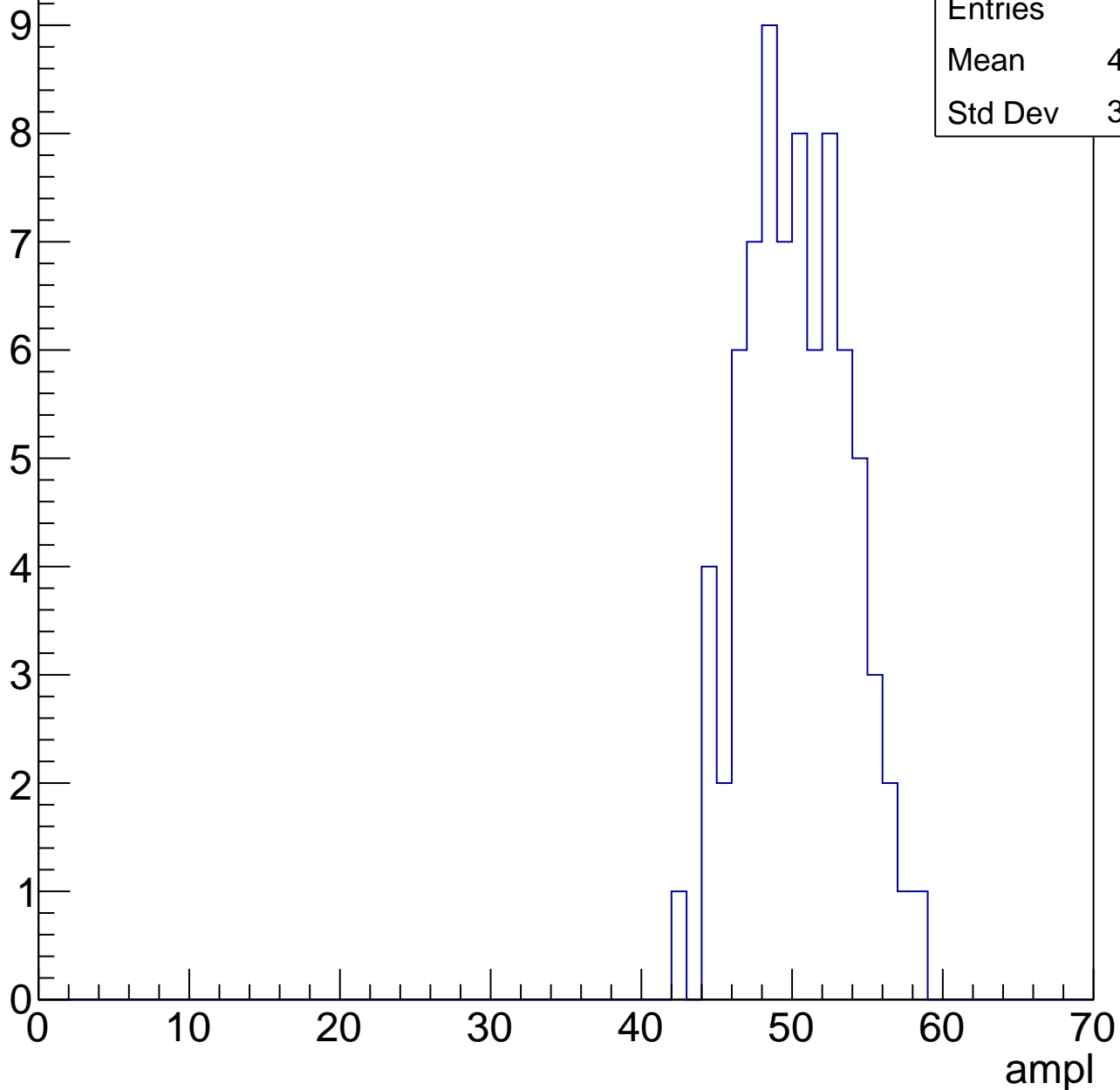
**Gaus Width: 3.0975**



# B1L101S, U8-ch72, adc3

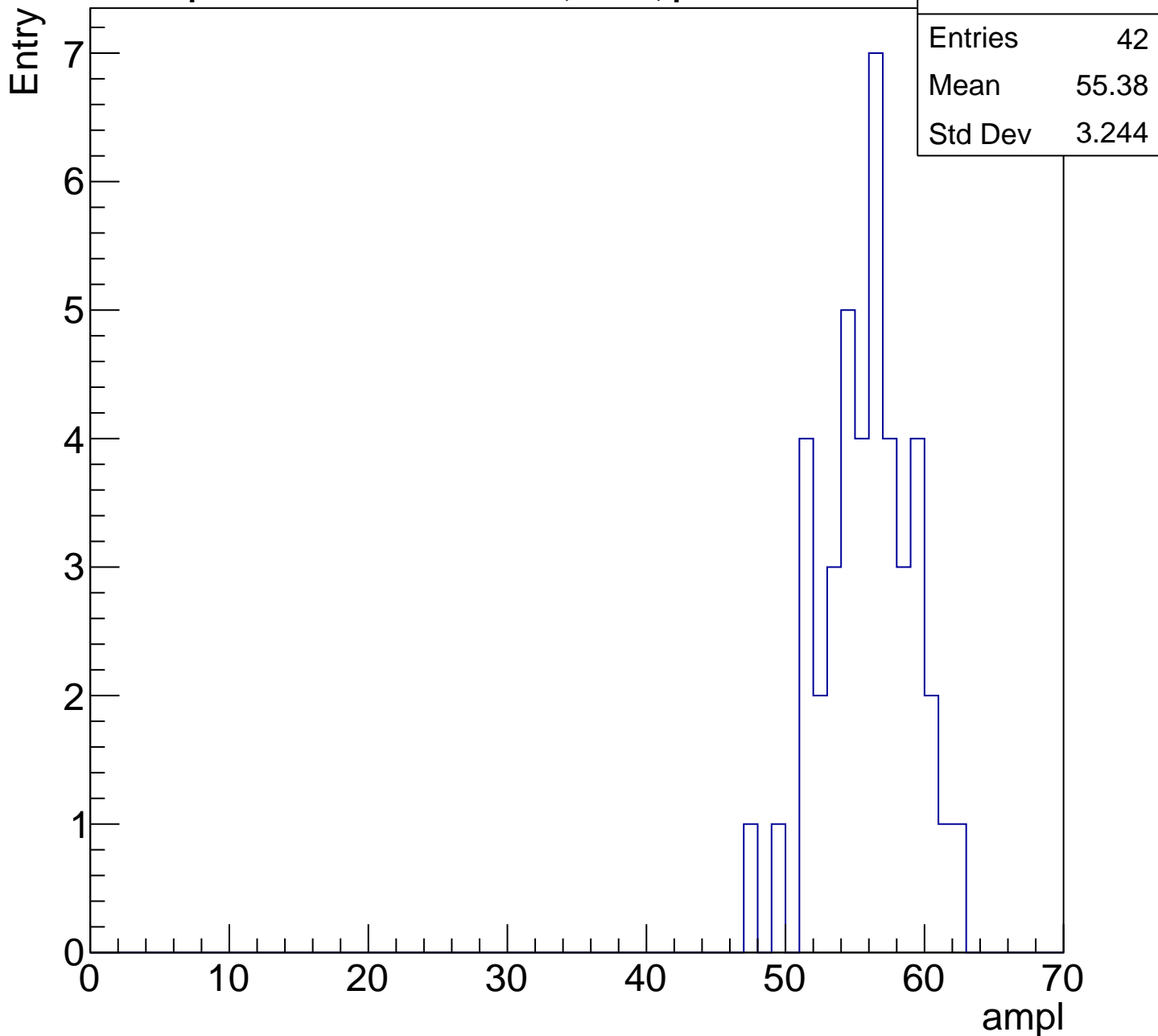
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

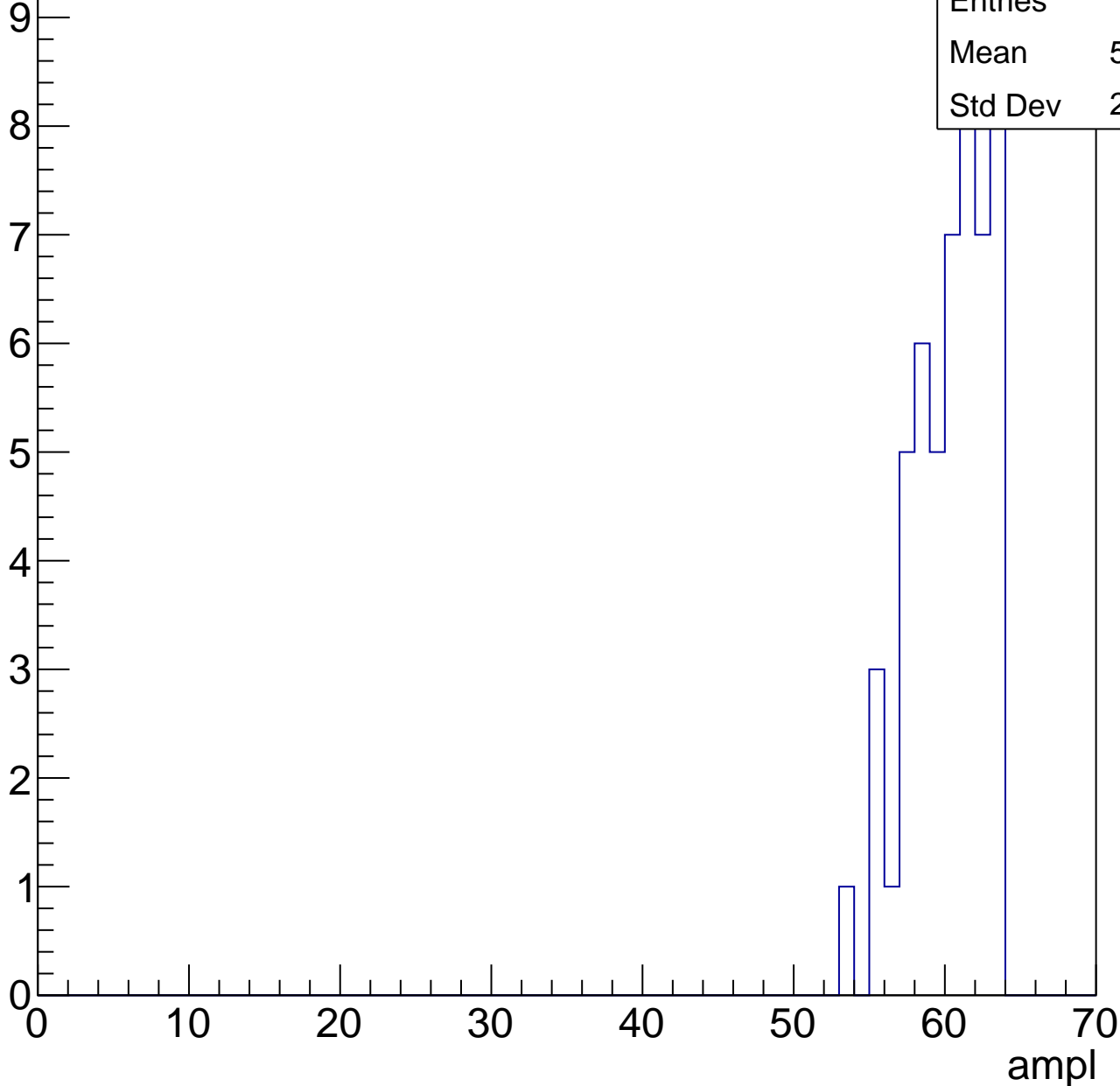


# B1L101S, U8-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	59.85
Std Dev	2.498



# B1L101S, U8-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

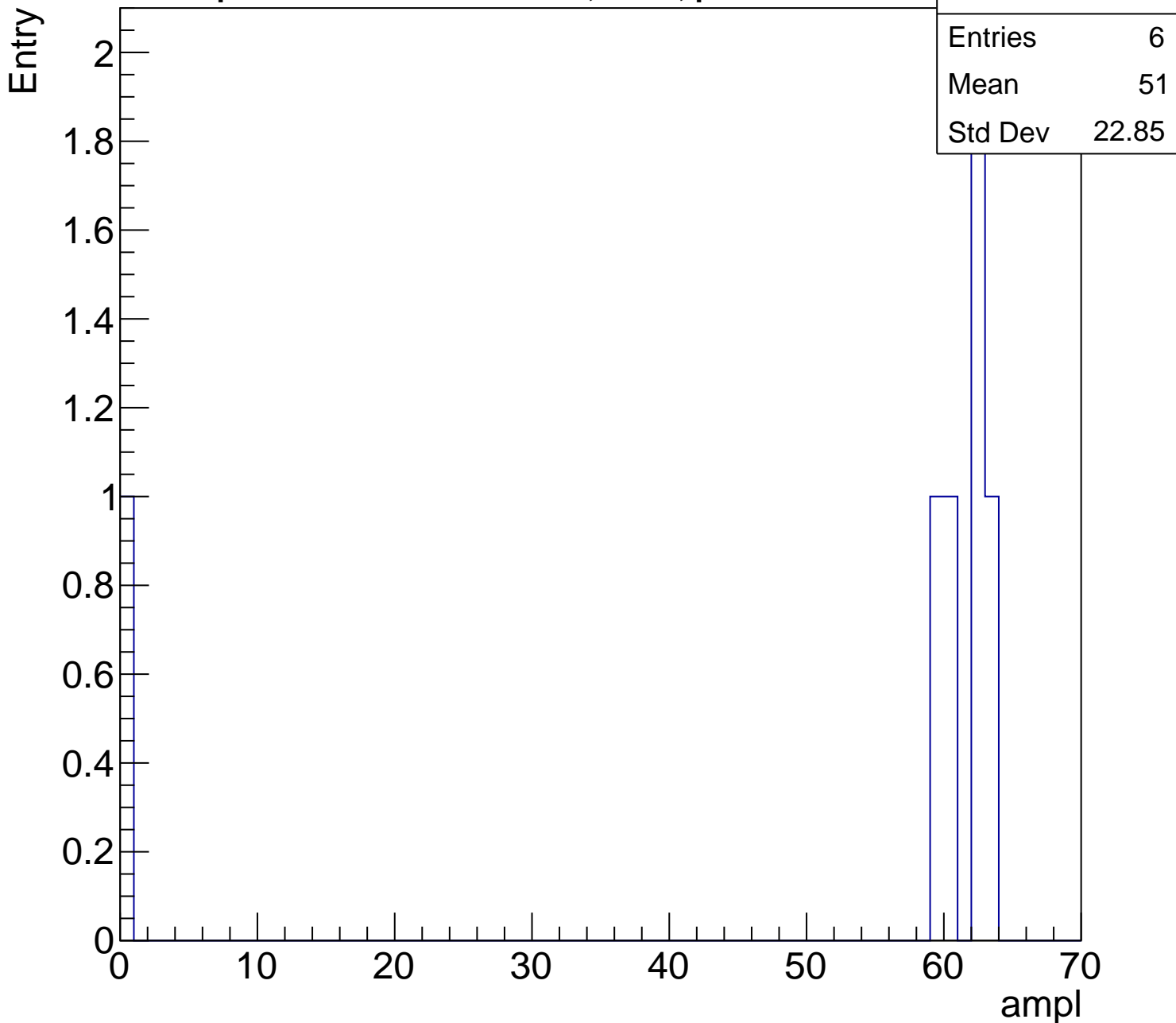
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	51
Std Dev	22.85

0 10 20 30 40 50 60 70

ampl





# B1L101S, U8-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U8-ch73, adc0

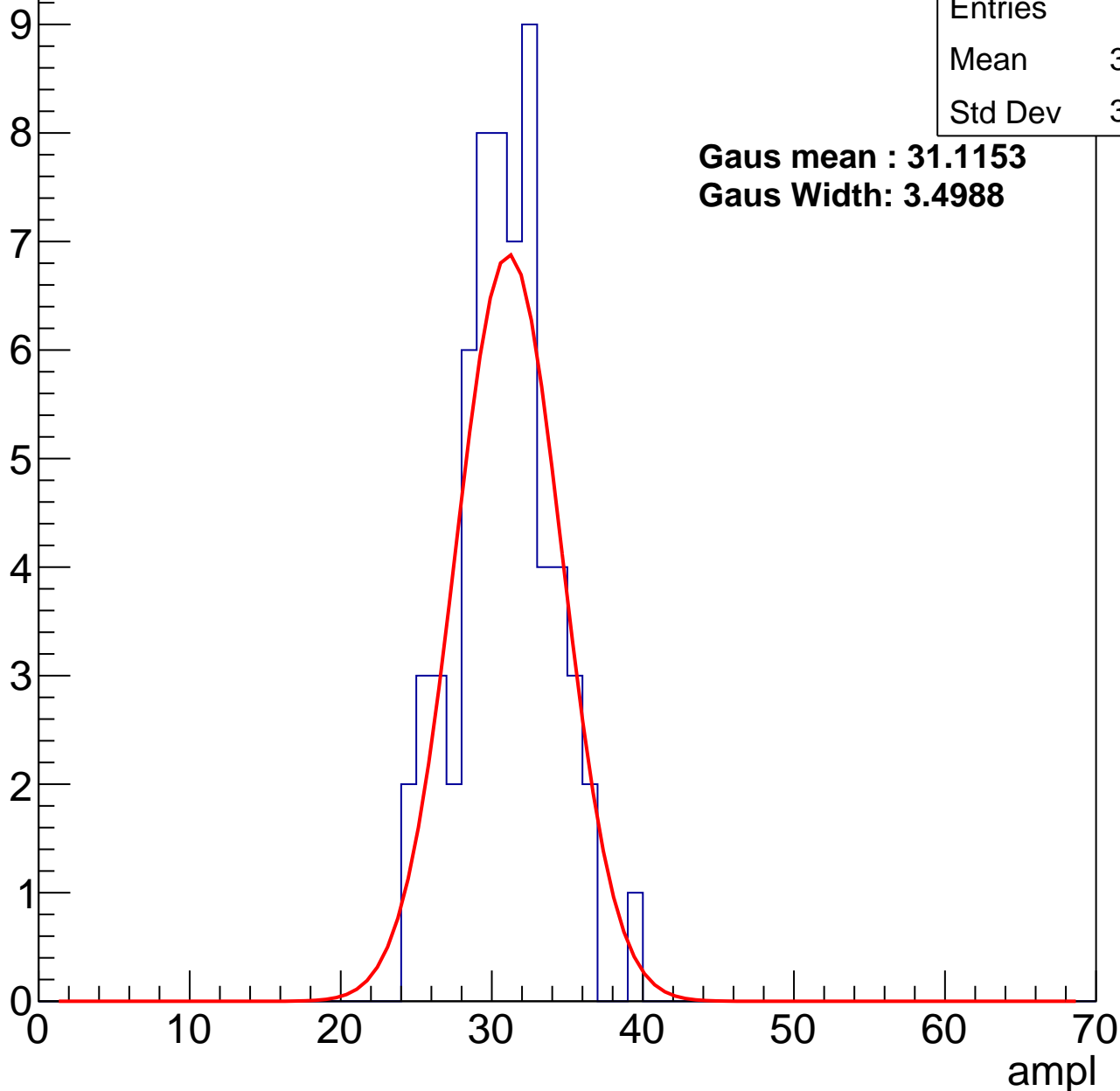
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	30.39
Std Dev	3.128

**Gaus mean : 31.153**

**Gaus Width: 3.4988**



# B1L101S, U8-ch73, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	85
Mean	38.51
Std Dev	3.667

**Gaus mean : 38.6678**

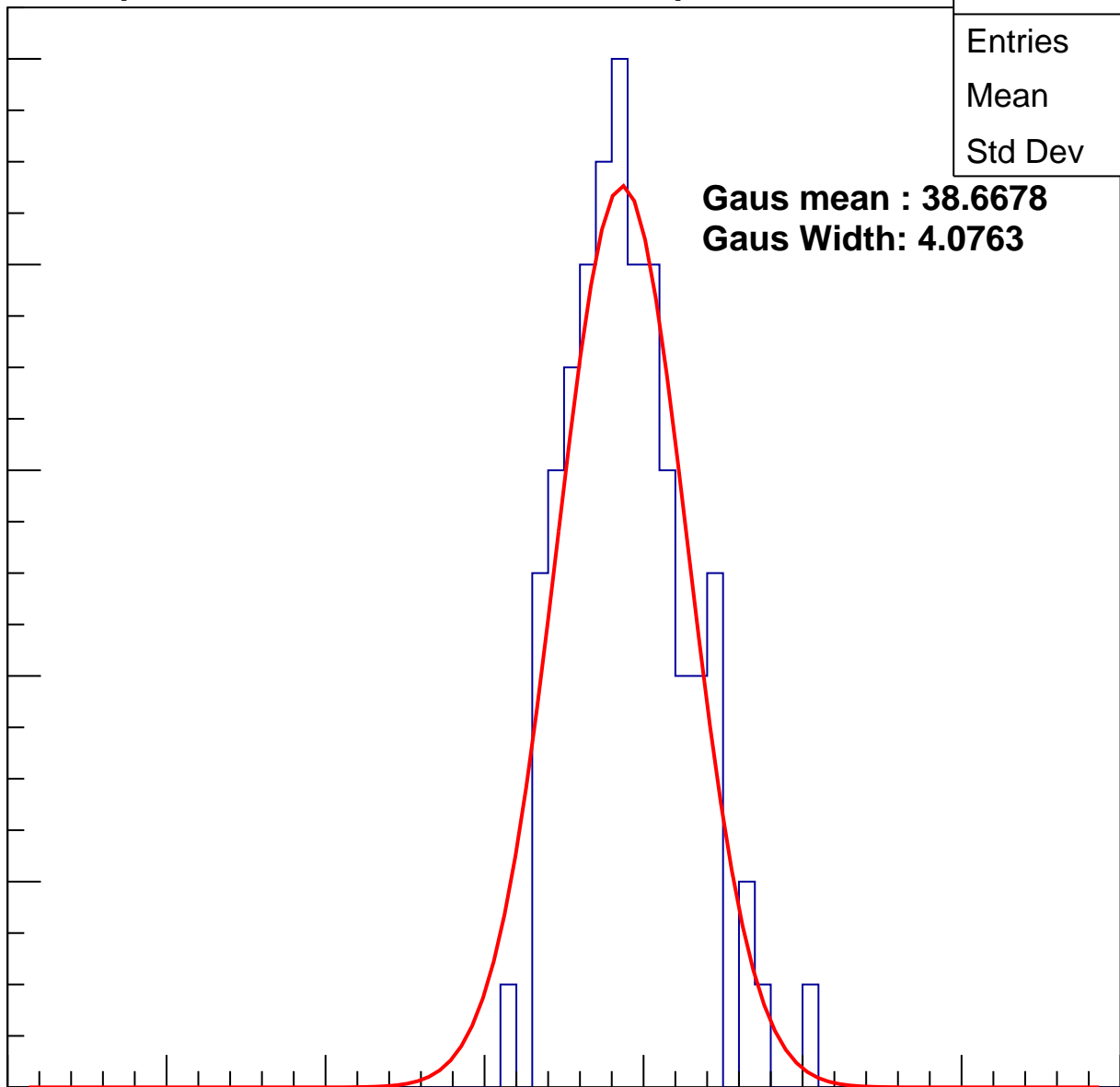
**Gaus Width: 4.0763**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U8-ch73, adc2

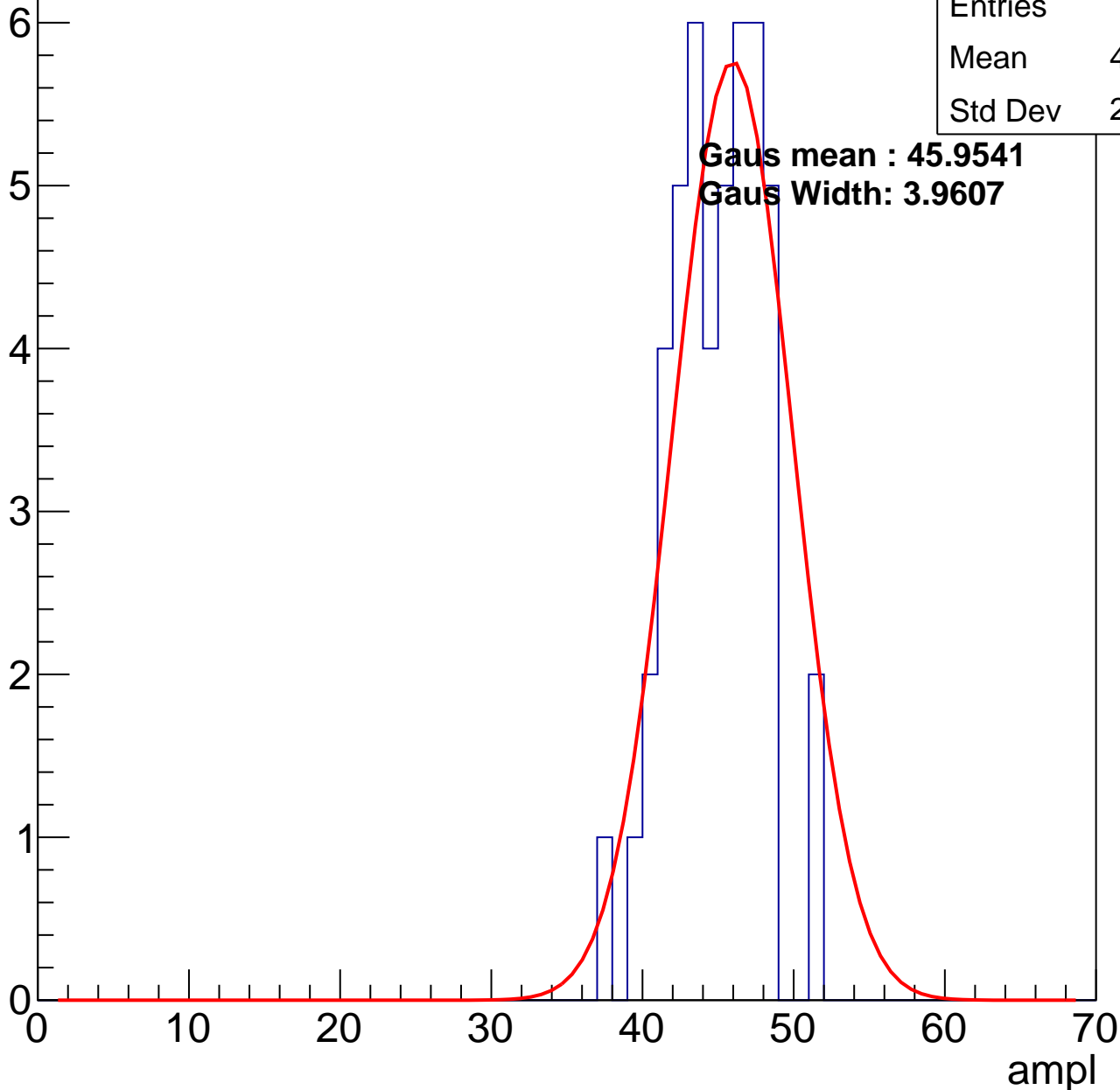
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	44.45
Std Dev	2.988

**Gaus mean : 45.9541**

**Gaus Width: 3.9607**

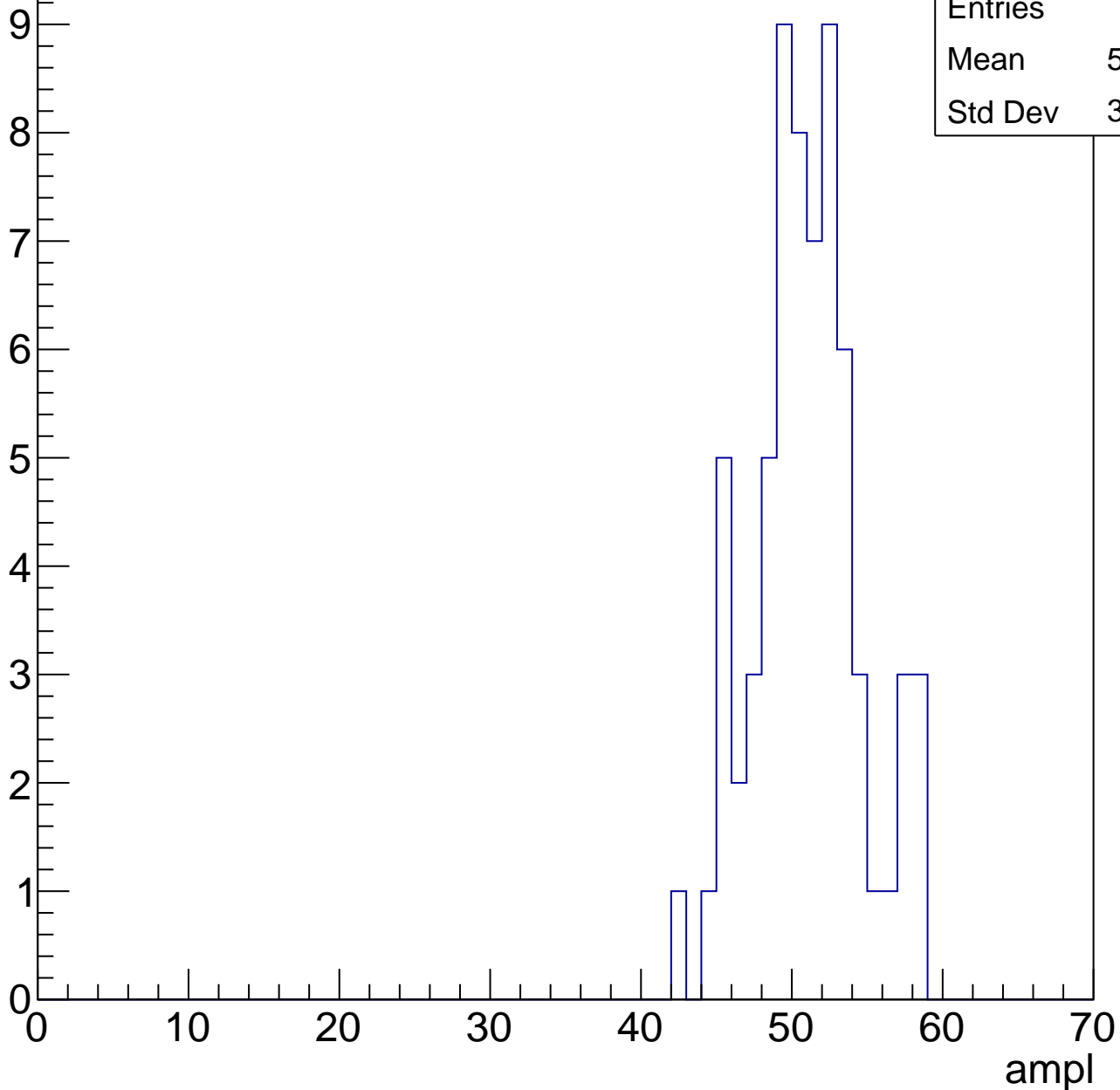


# B1L101S, U8-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

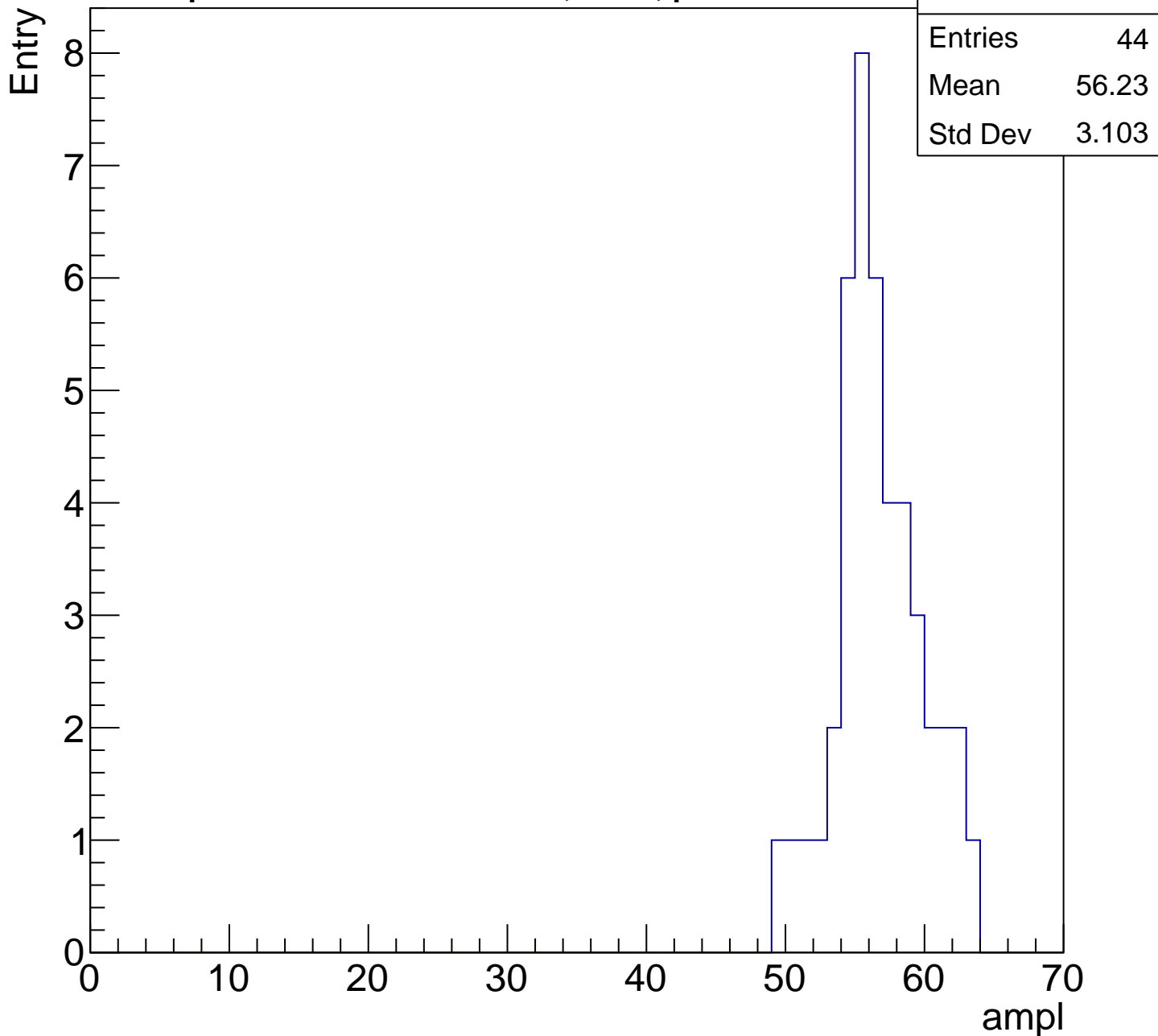
Entry

Entries	67
Mean	50.54
Std Dev	3.538



# B1L101S, U8-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U8-ch73, adc5

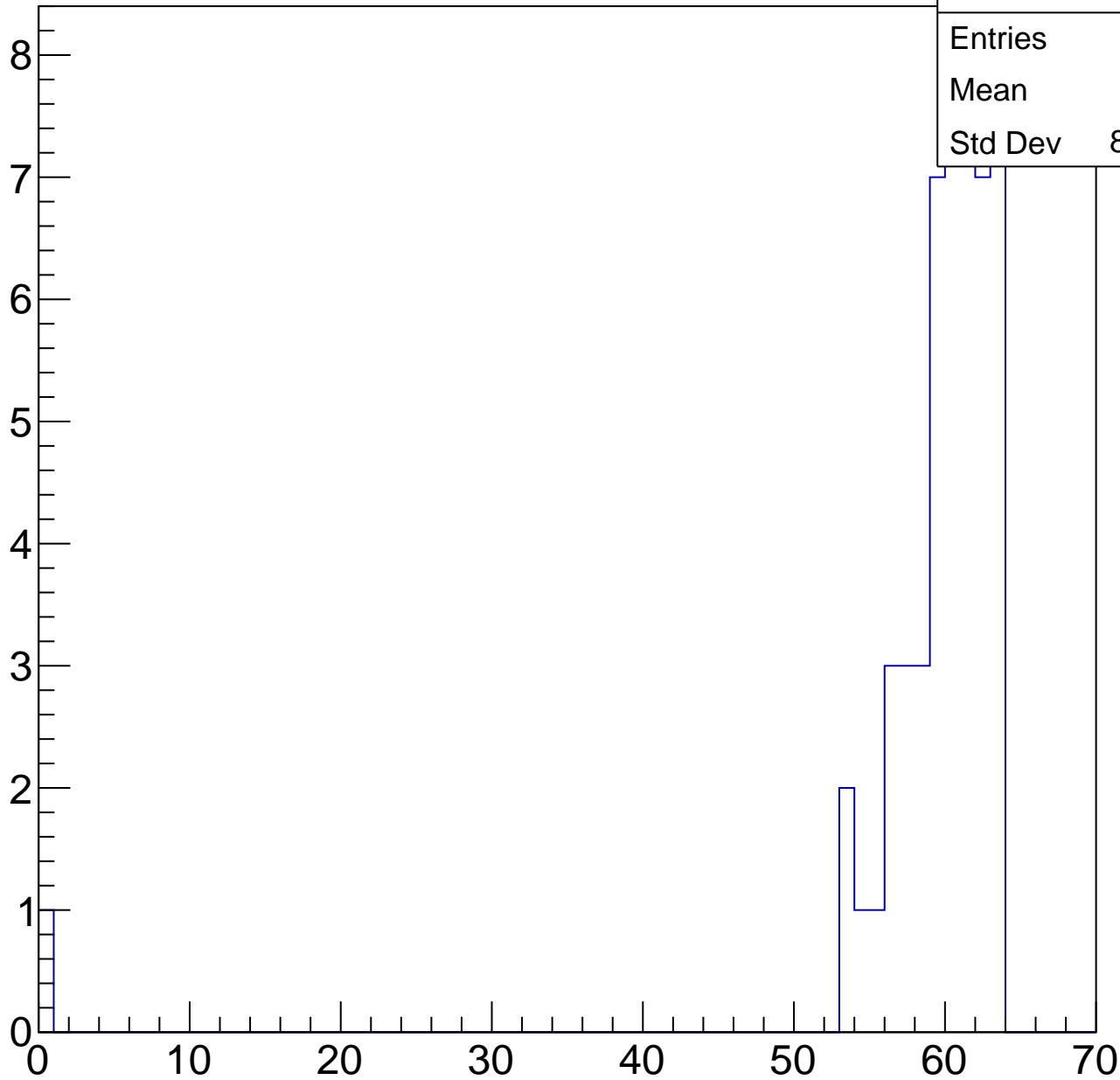
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	52
Mean	58.6
Std Dev	8.614

ampl



# B1L101S, U8-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch74, adc0

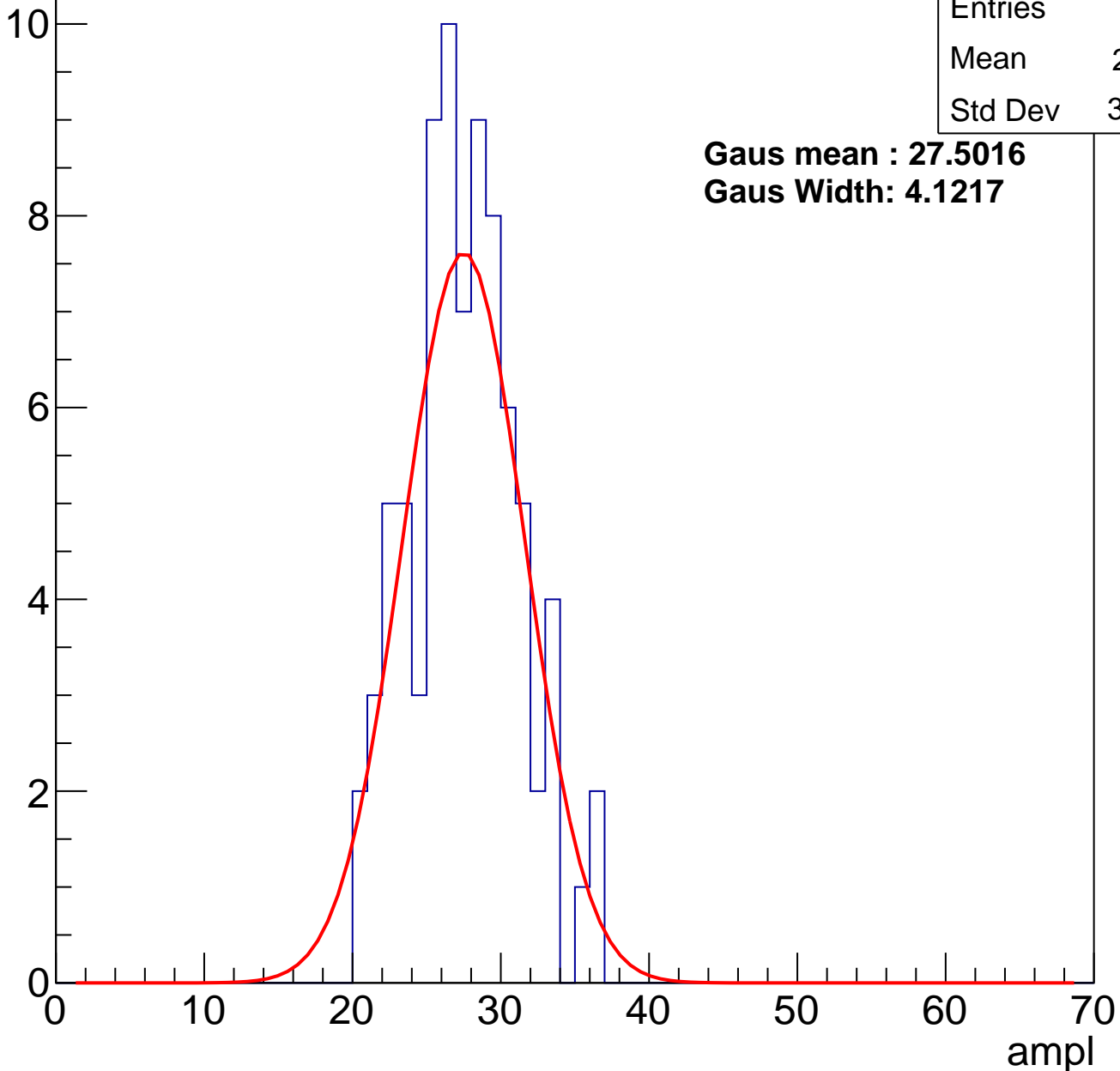
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	81
Mean	27.11
Std Dev	3.648

**Gaus mean : 27.5016**

**Gaus Width: 4.1217**

Entry



# B1L101S, U8-ch74, adc1

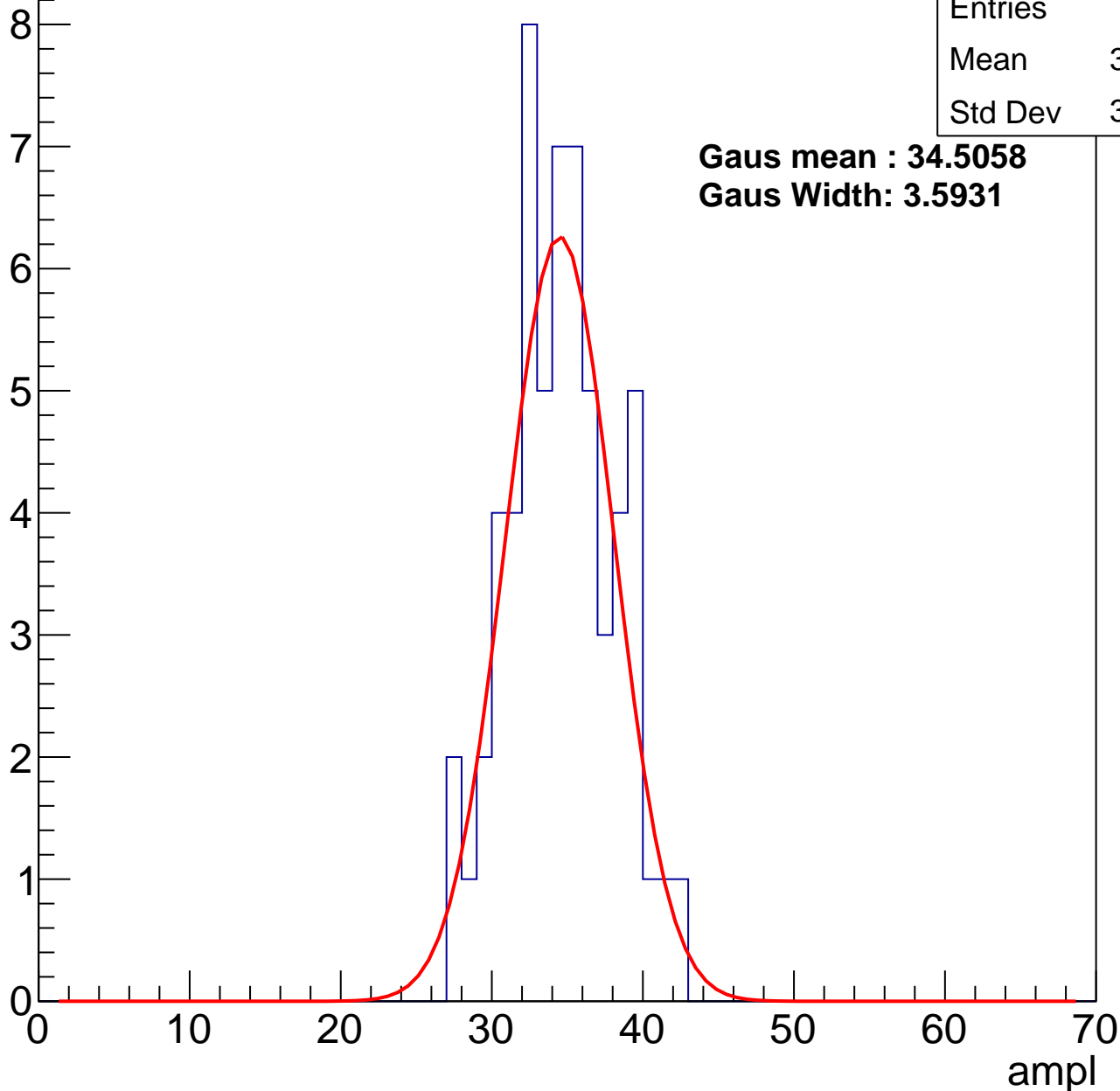
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	34.15
Std Dev	3.444

**Gaus mean : 34.5058**

**Gaus Width: 3.5931**



# B1L101S, U8-ch74, adc2

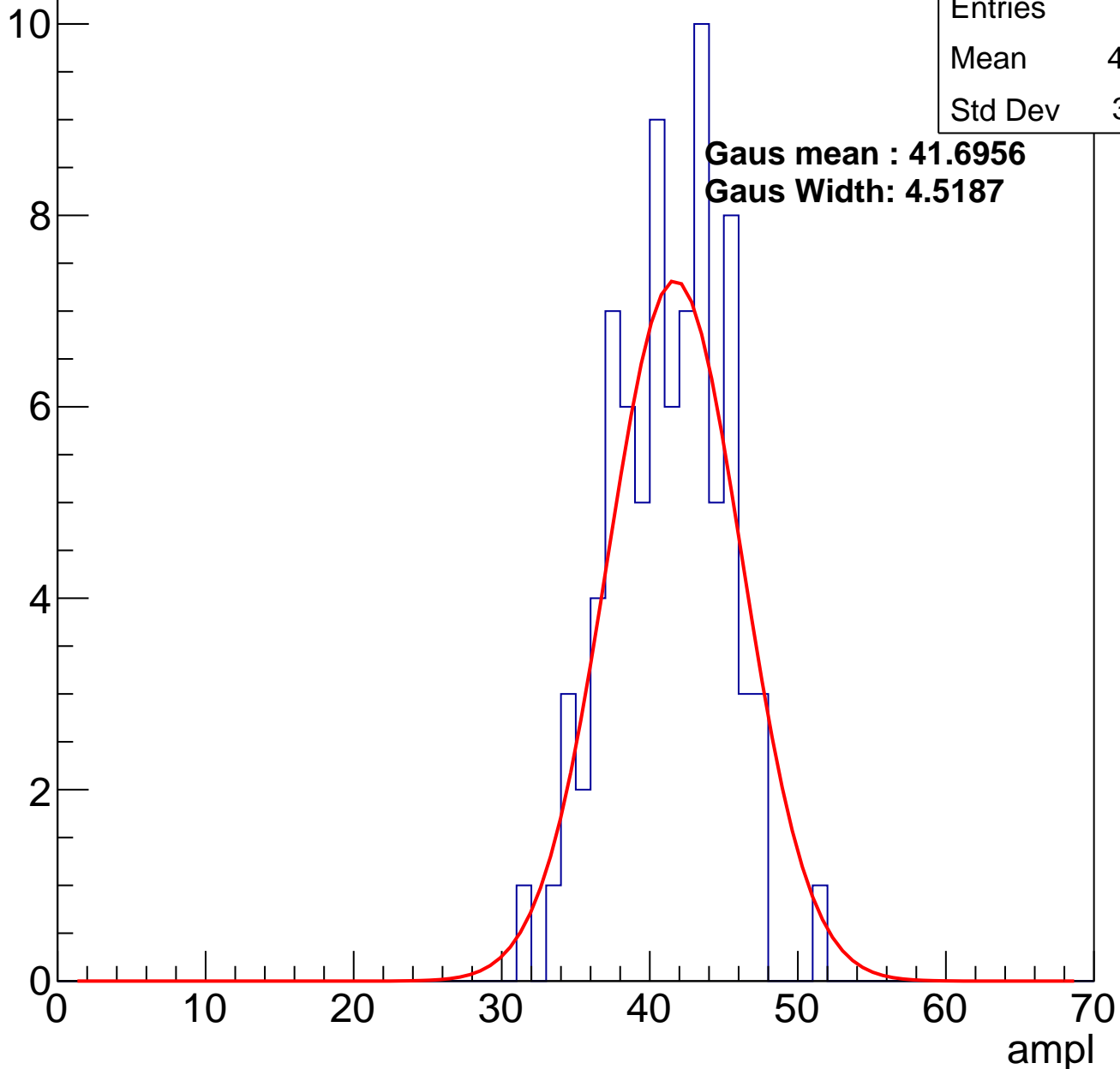
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	81
Mean	40.77
Std Dev	3.811

**Gaus mean : 41.6956**

**Gaus Width: 4.5187**

Entry

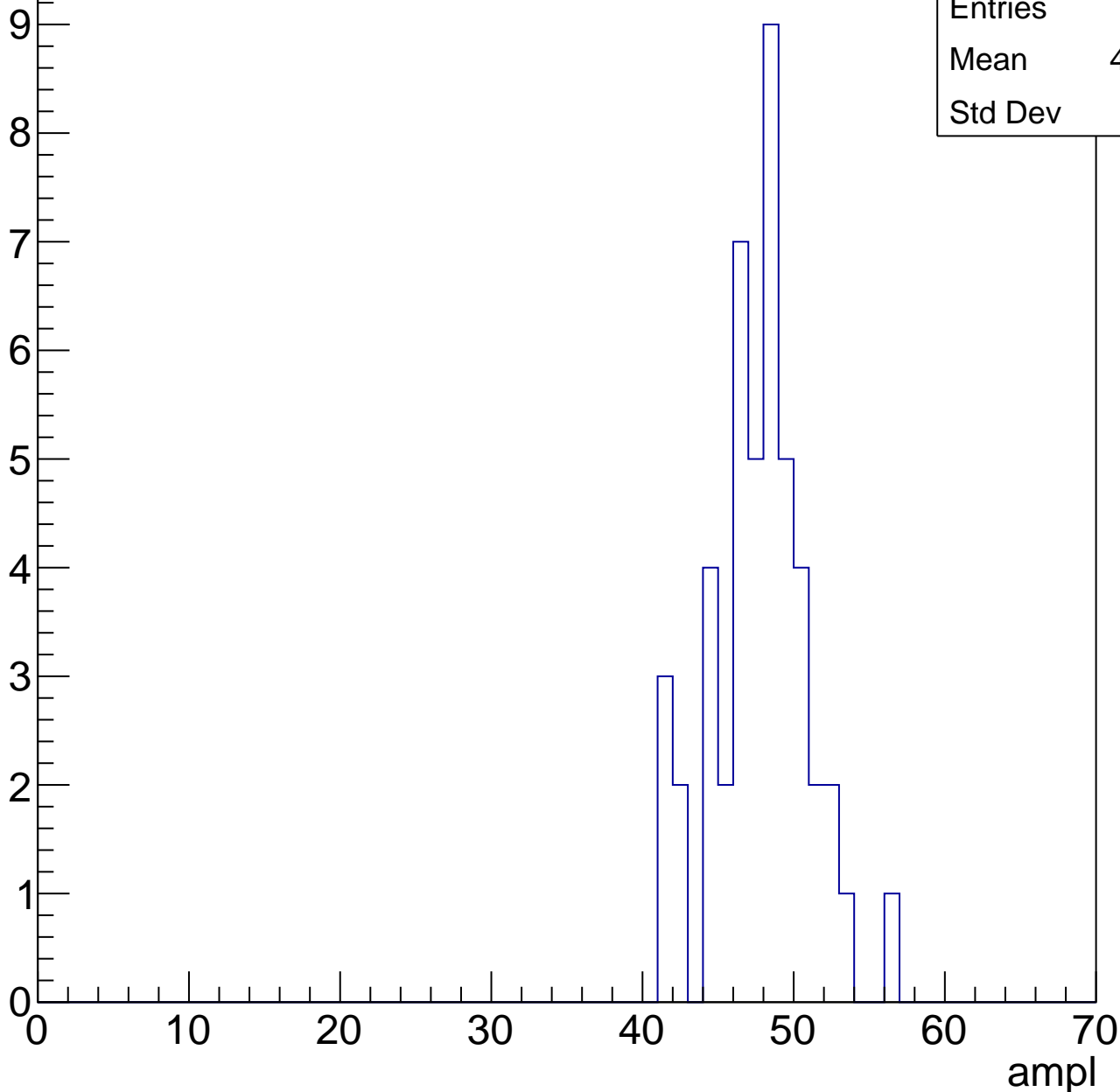


# B1L101S, U8-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

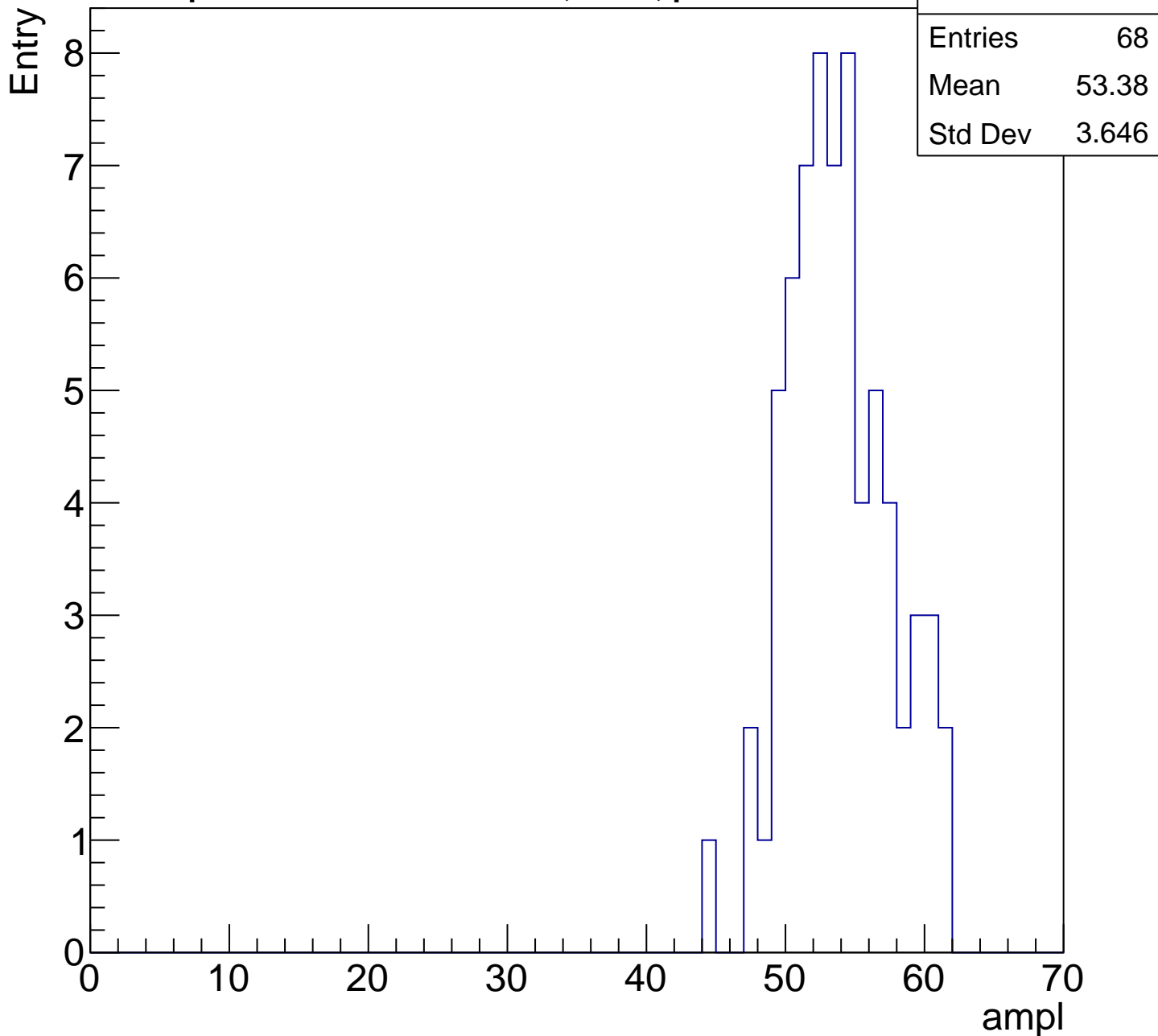
Entry

Entries	47
Mean	47.28
Std Dev	3.16



# B1L101S, U8-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U8-ch74, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

6

5

4

3

2

1

0

0

10

20

30

40

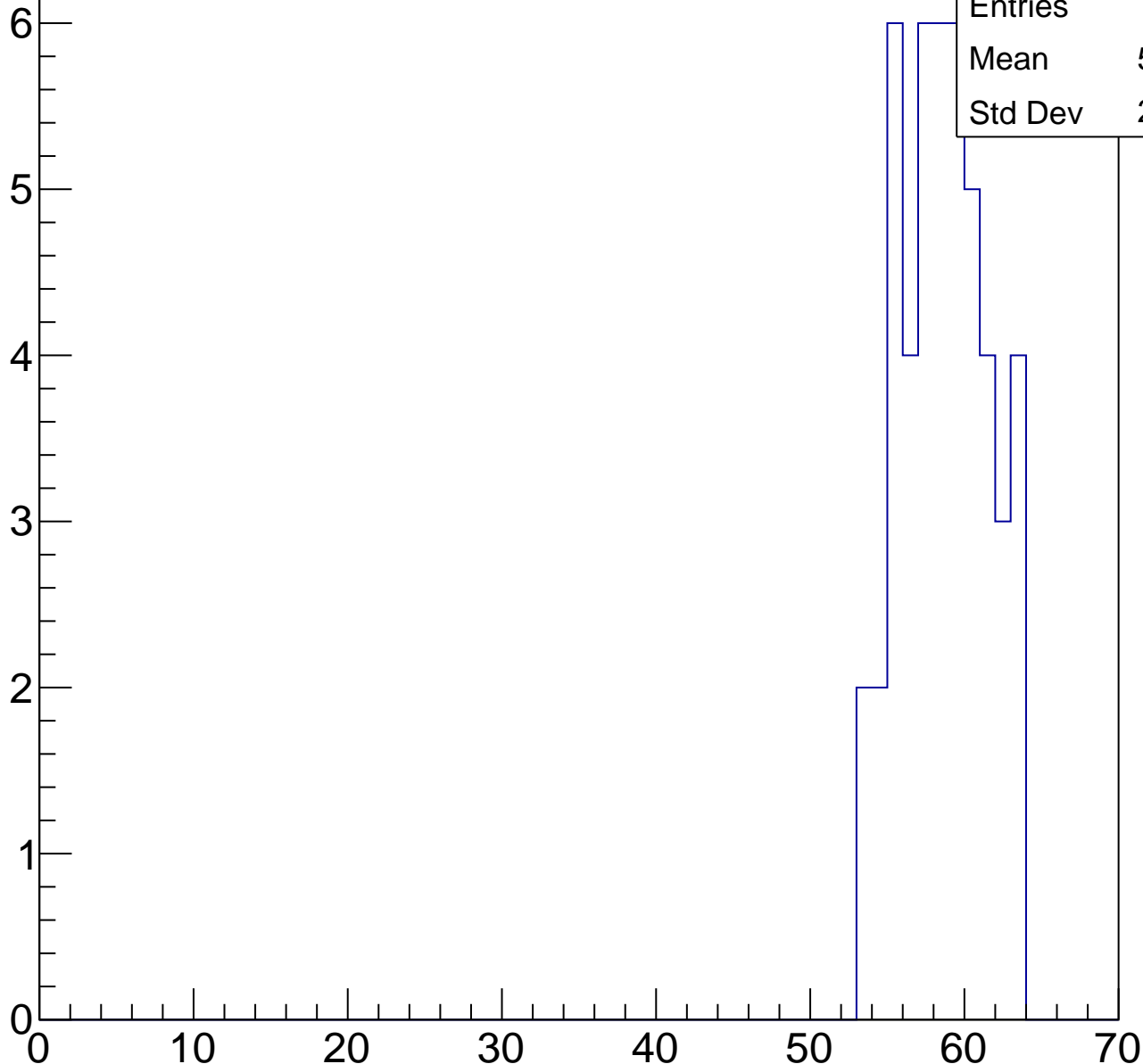
50

60

70

ampl

Entries	48
Mean	58.21
Std Dev	2.761

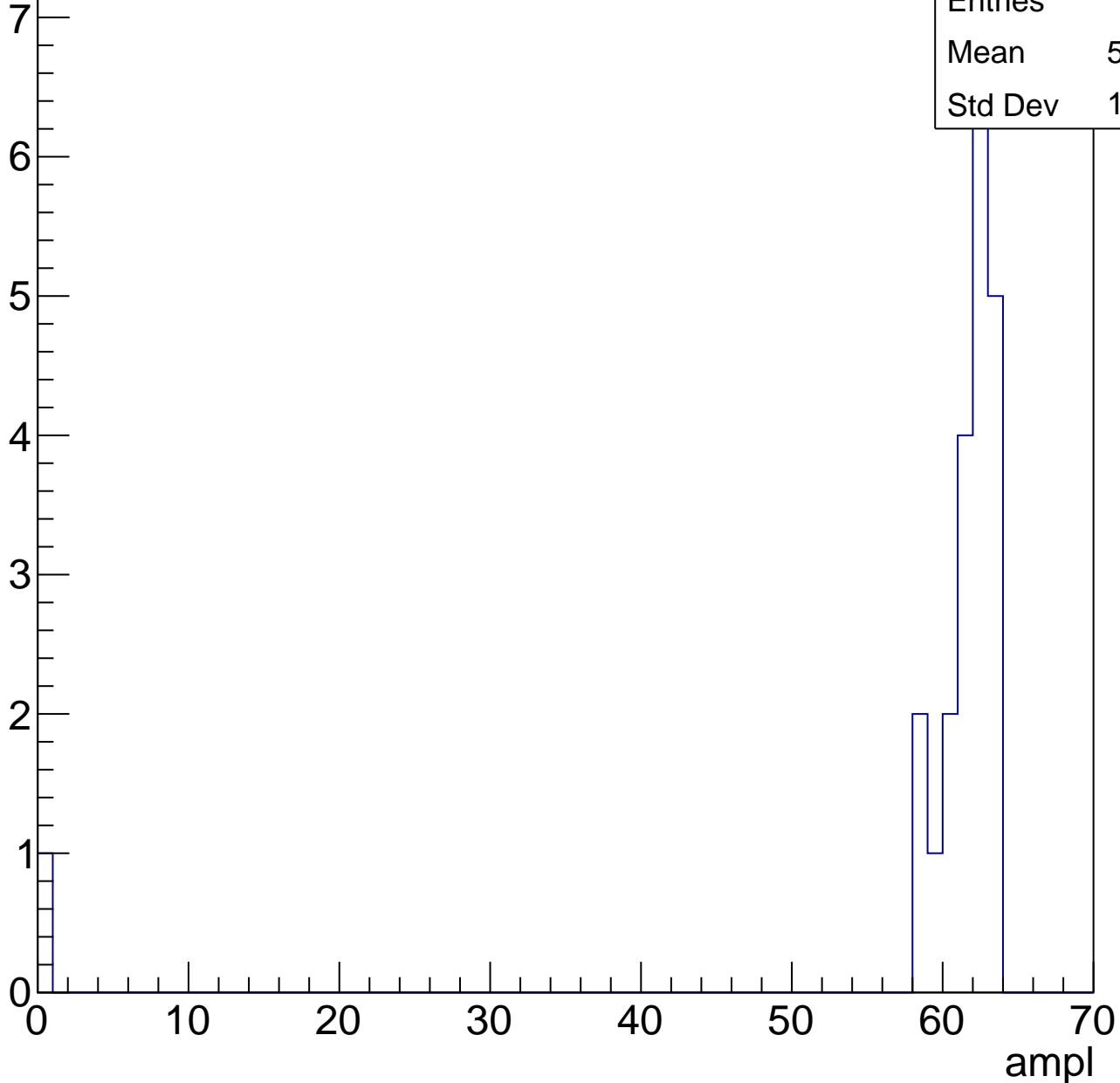


# B1L101S, U8-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	22
Mean	58.55
Std Dev	12.86





# B1L101S, U8-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch75, adc0

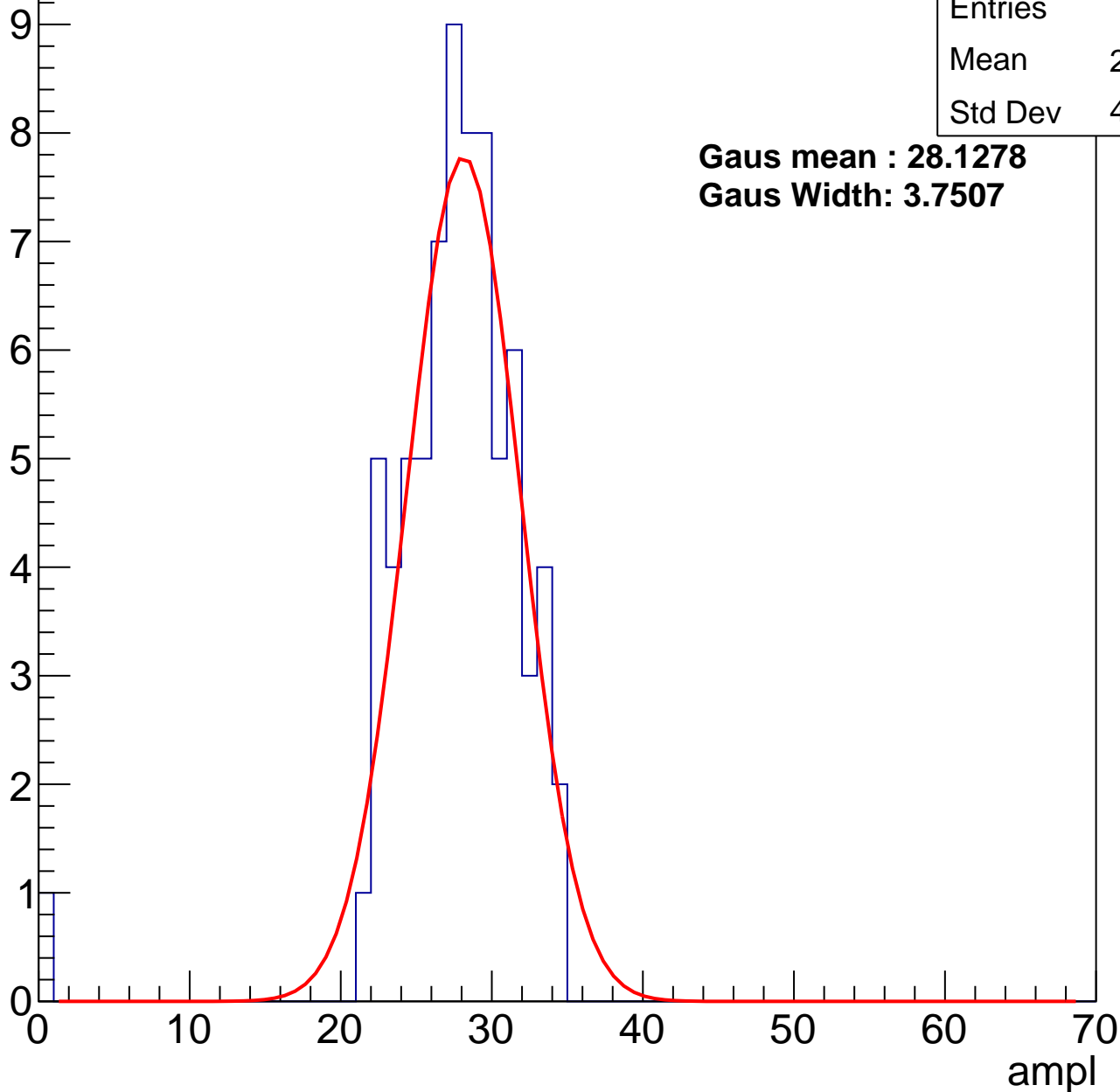
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	27.14
Std Dev	4.567

**Gaus mean : 28.1278**

**Gaus Width: 3.7507**



# B1L101S, U8-ch75, adc1

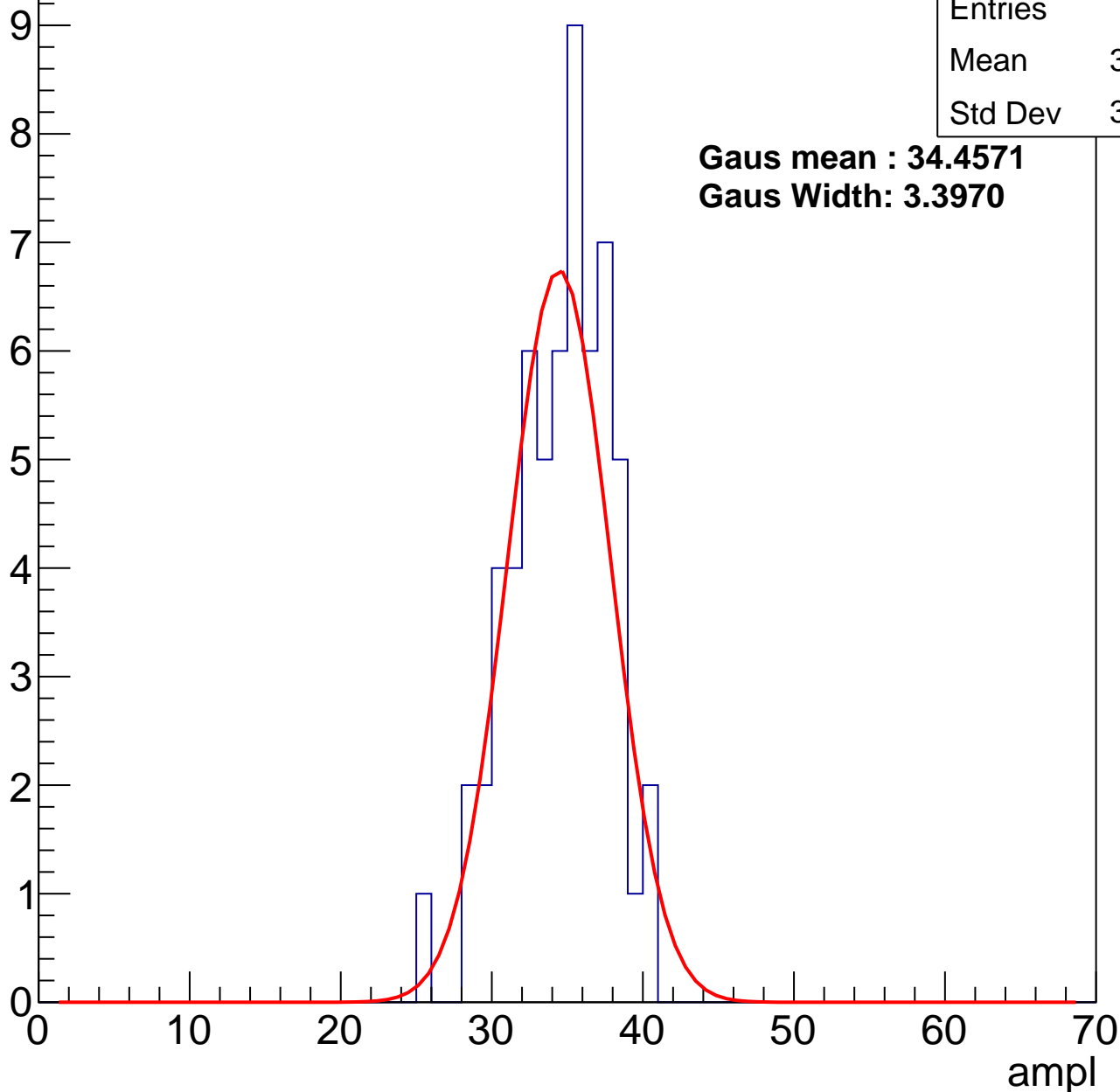
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	34.05
Std Dev	3.175

**Gaus mean : 34.4571**

**Gaus Width: 3.3970**



# B1L101S, U8-ch75, adc2

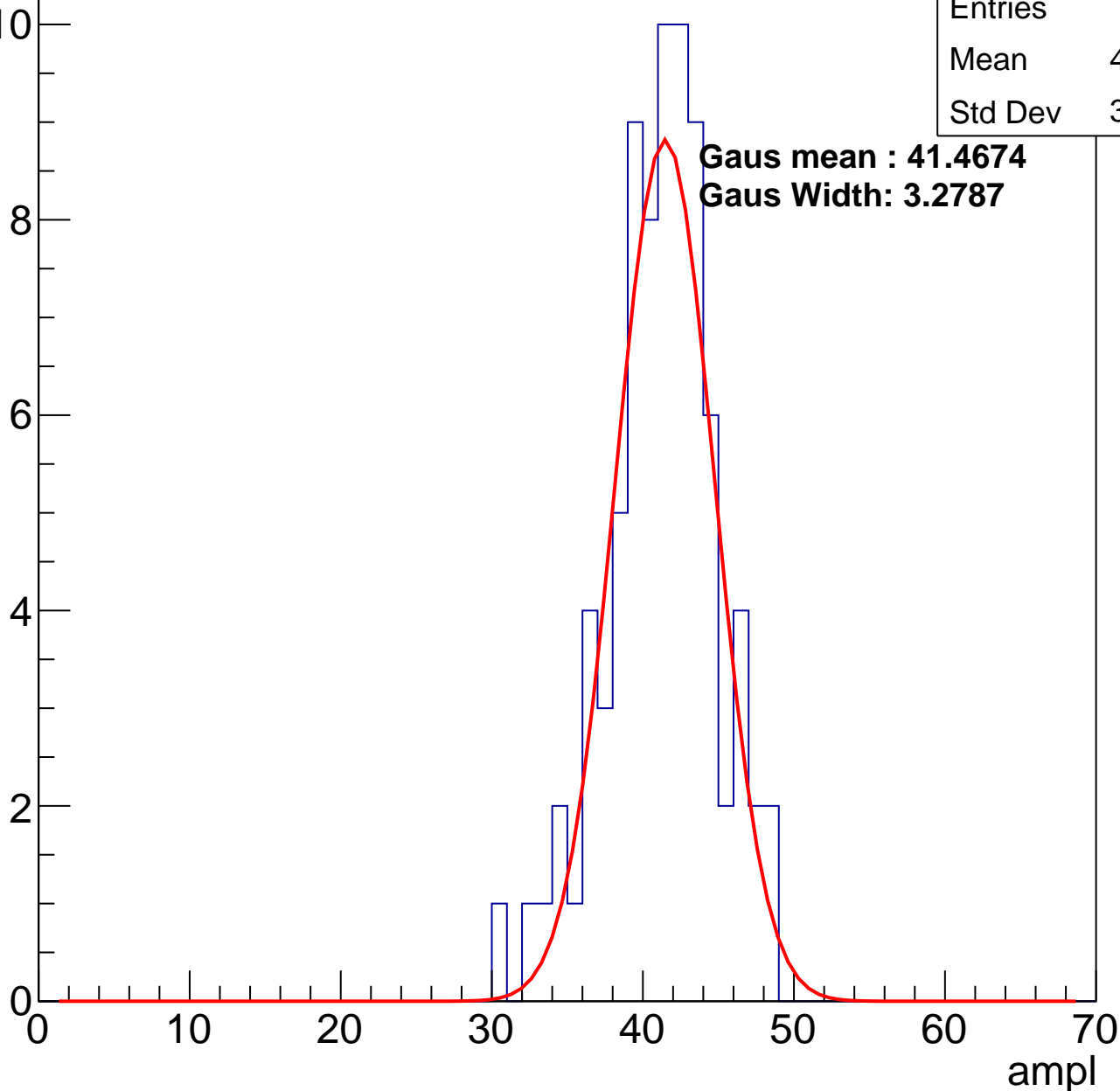
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	40.74
Std Dev	3.594

**Gaus mean : 41.4674**

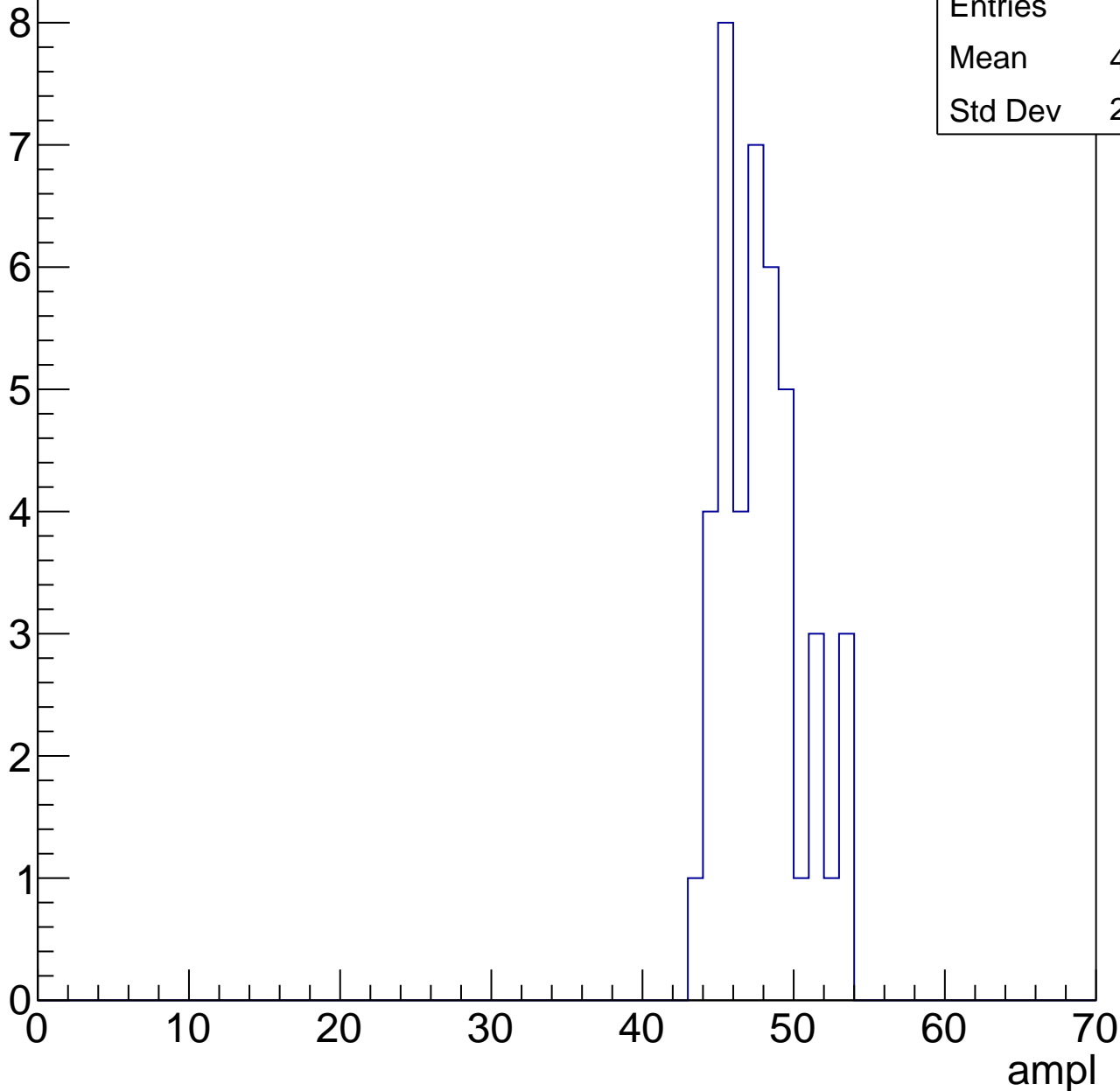
**Gaus Width: 3.2787**



# B1L101S, U8-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

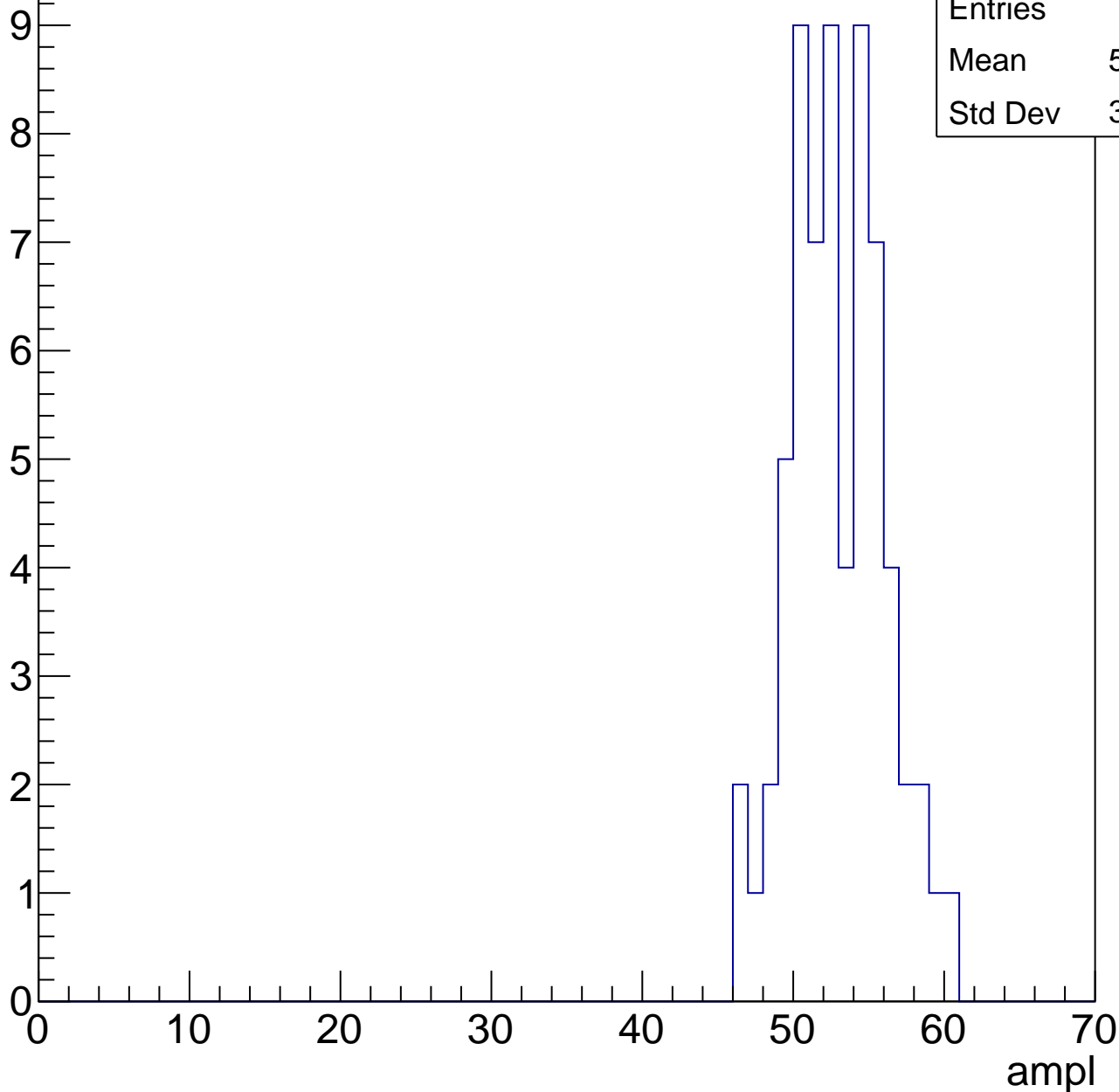


Entries	43
Mean	47.42
Std Dev	2.626

# B1L101S, U8-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	65
Mean	52.48
Std Dev	3.049

# B1L101S, U8-ch75, adc5

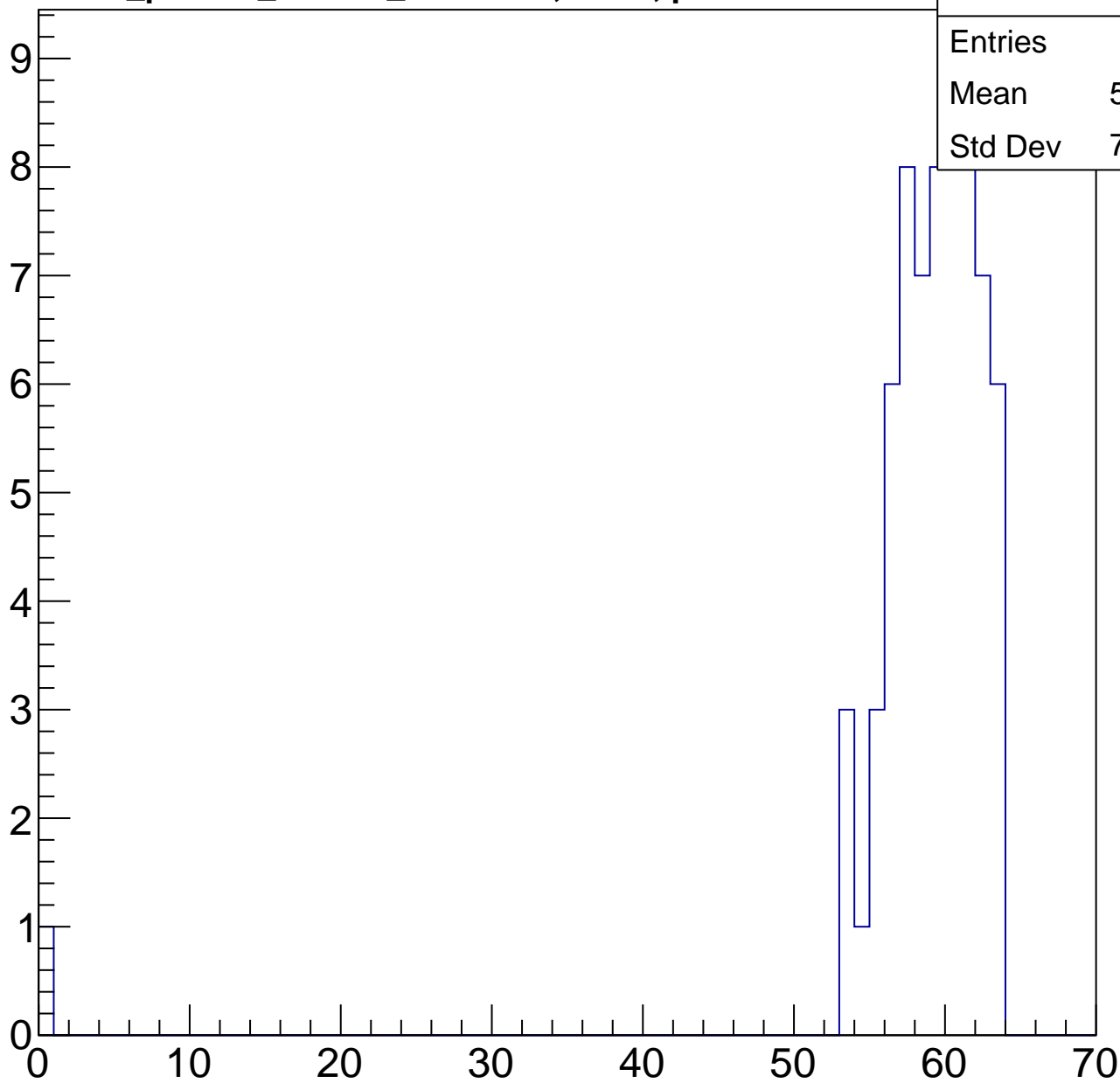
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	67
Mean	58.03
Std Dev	7.622

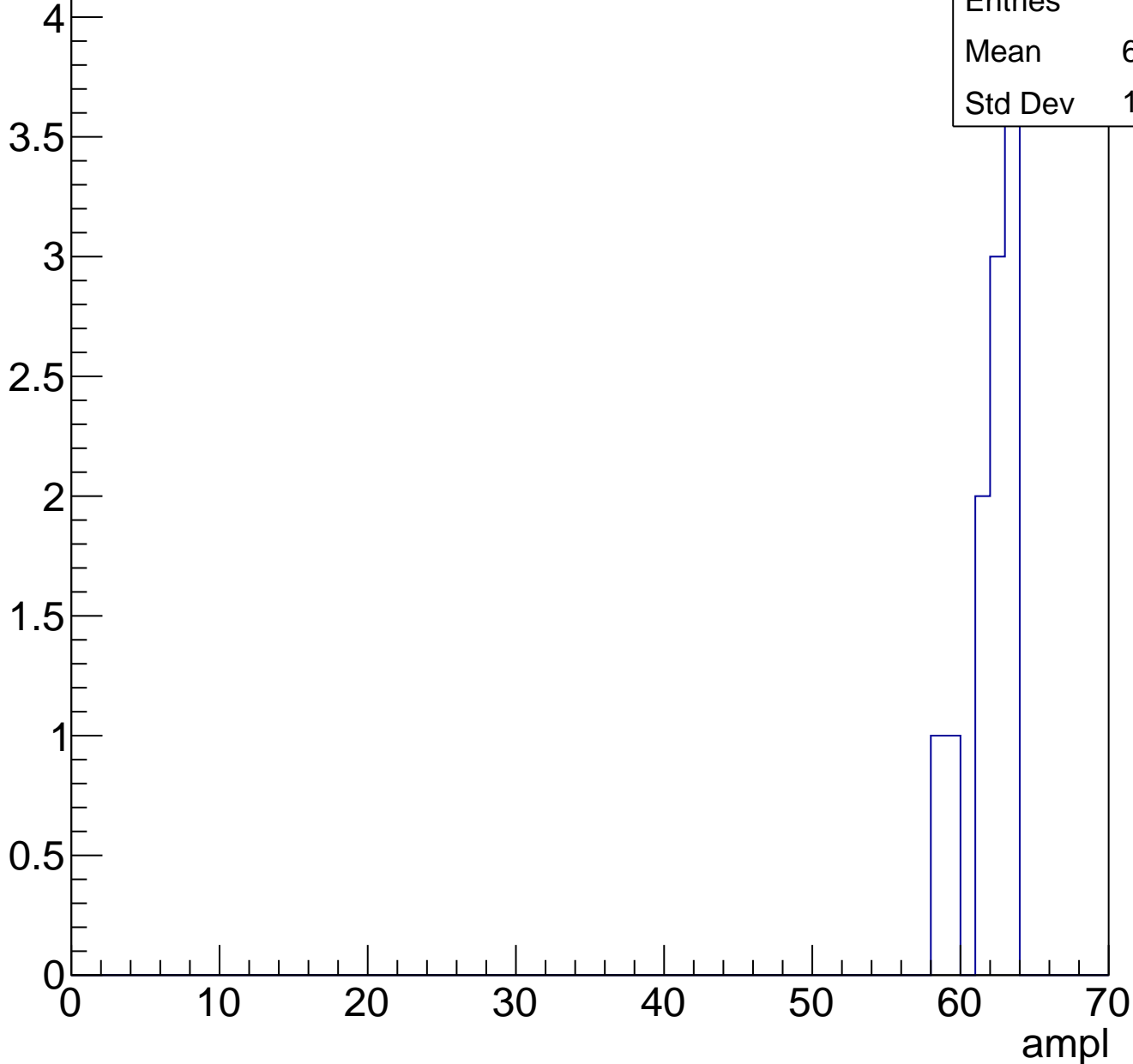
ampl



# B1L101S, U8-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

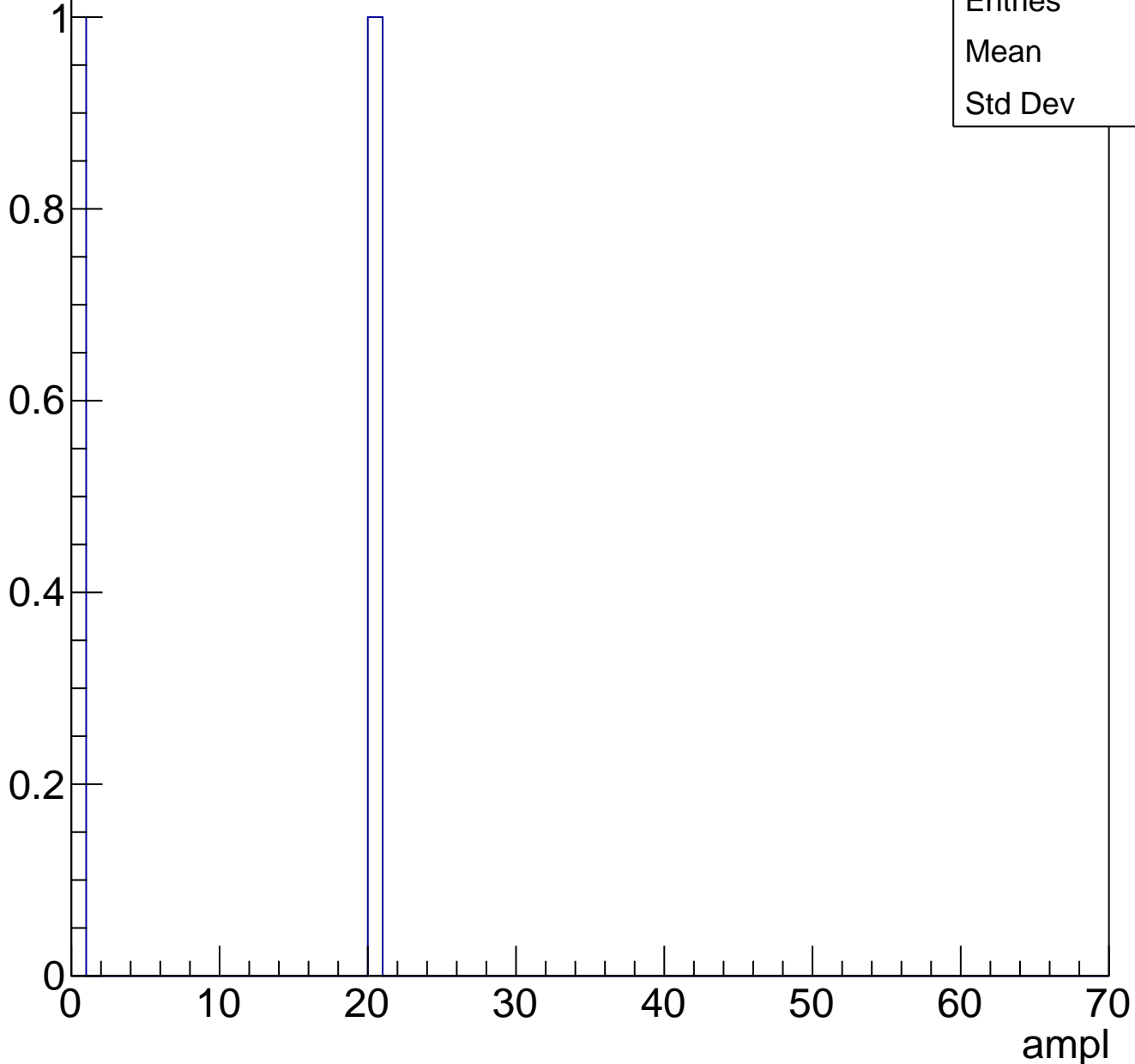




# B1L101S, U8-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	10
Std Dev	10

# B1L101S, U8-ch76, adc0

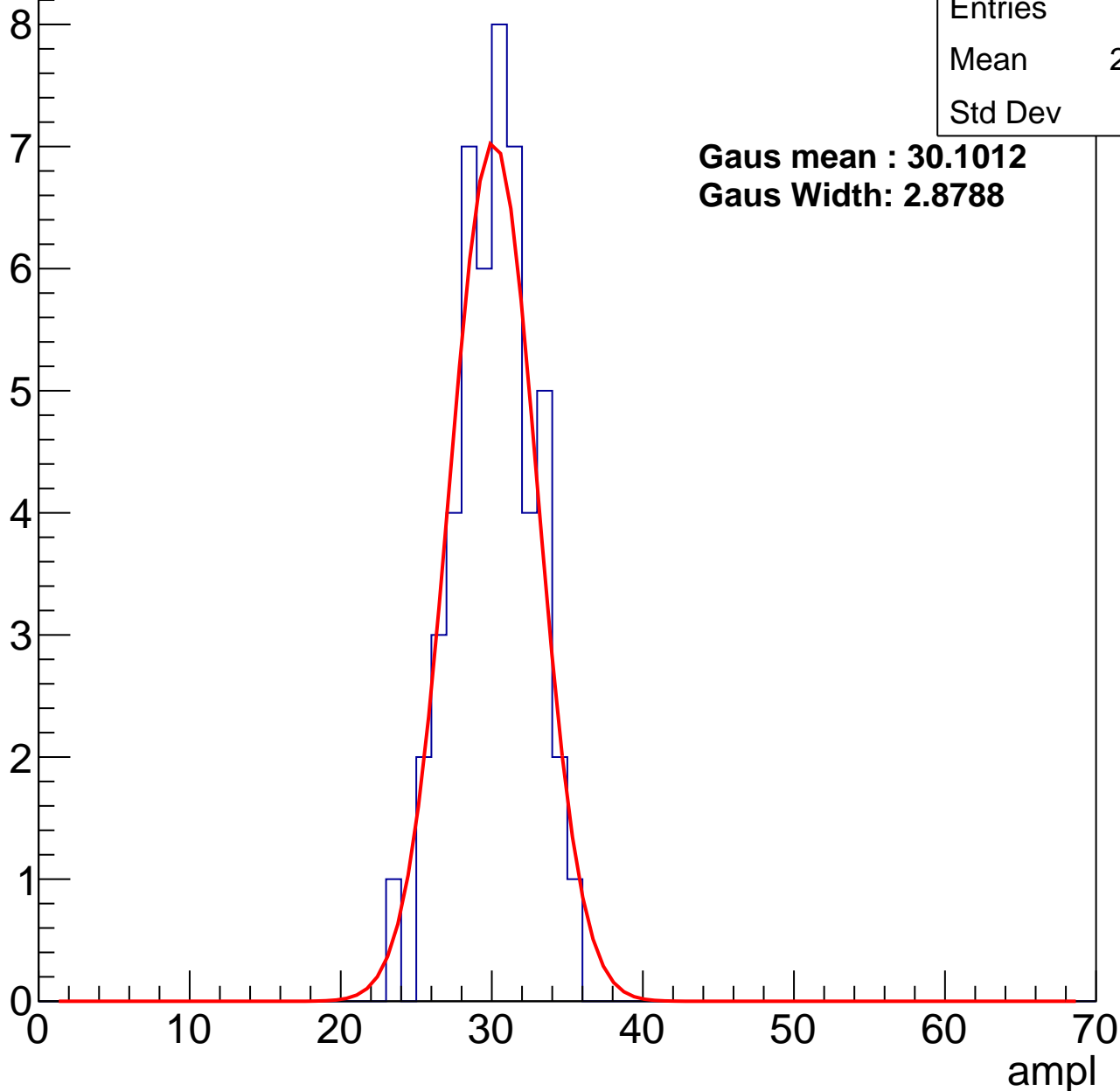
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	29.64
Std Dev	2.59

**Gaus mean : 30.1012**

**Gaus Width: 2.8788**

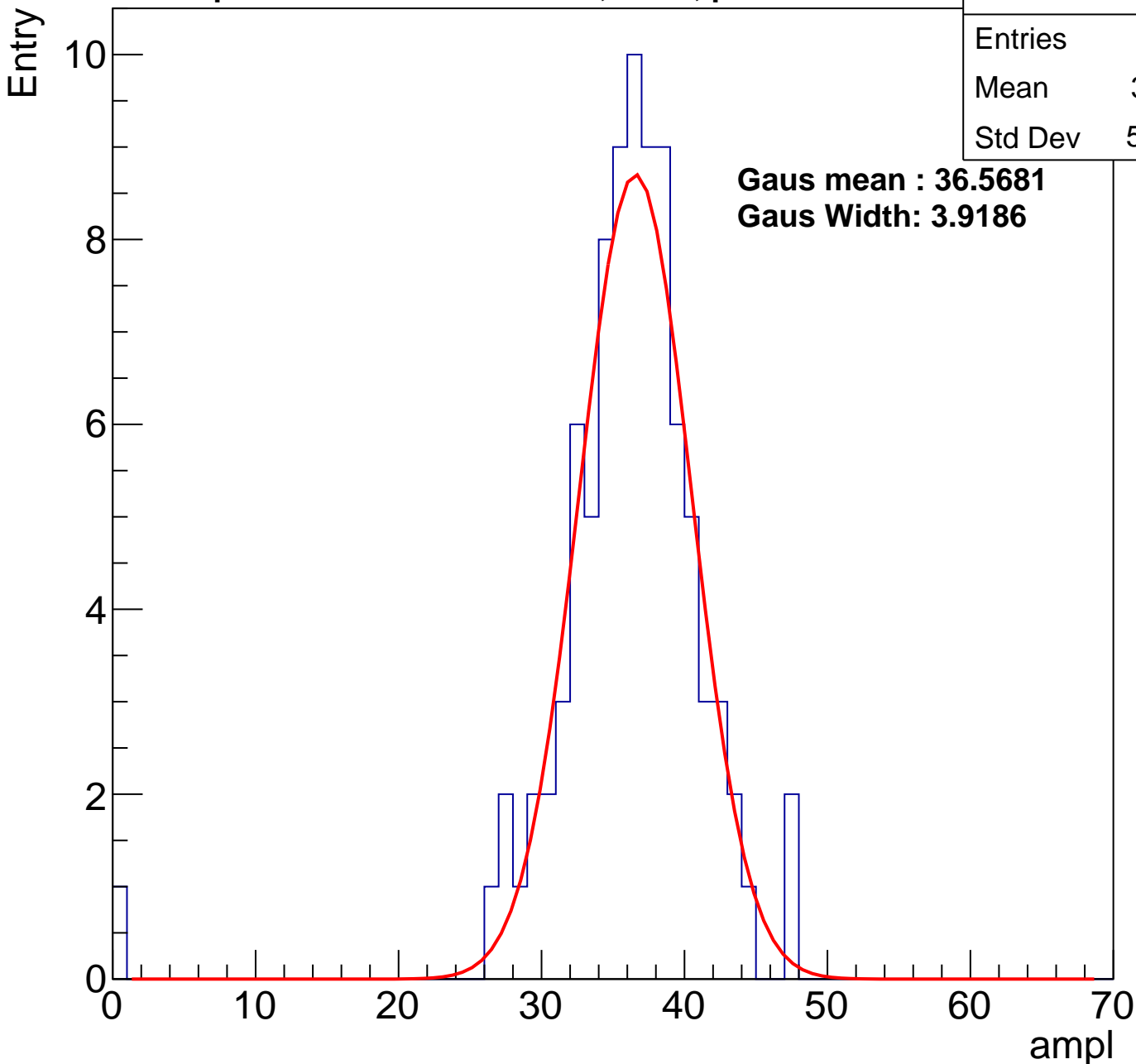


# B1L101S, U8-ch76, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	90
Mean	35.61
Std Dev	5.579

**Gaus mean : 36.5681**  
**Gaus Width: 3.9186**



# B1L101S, U8-ch76, adc2

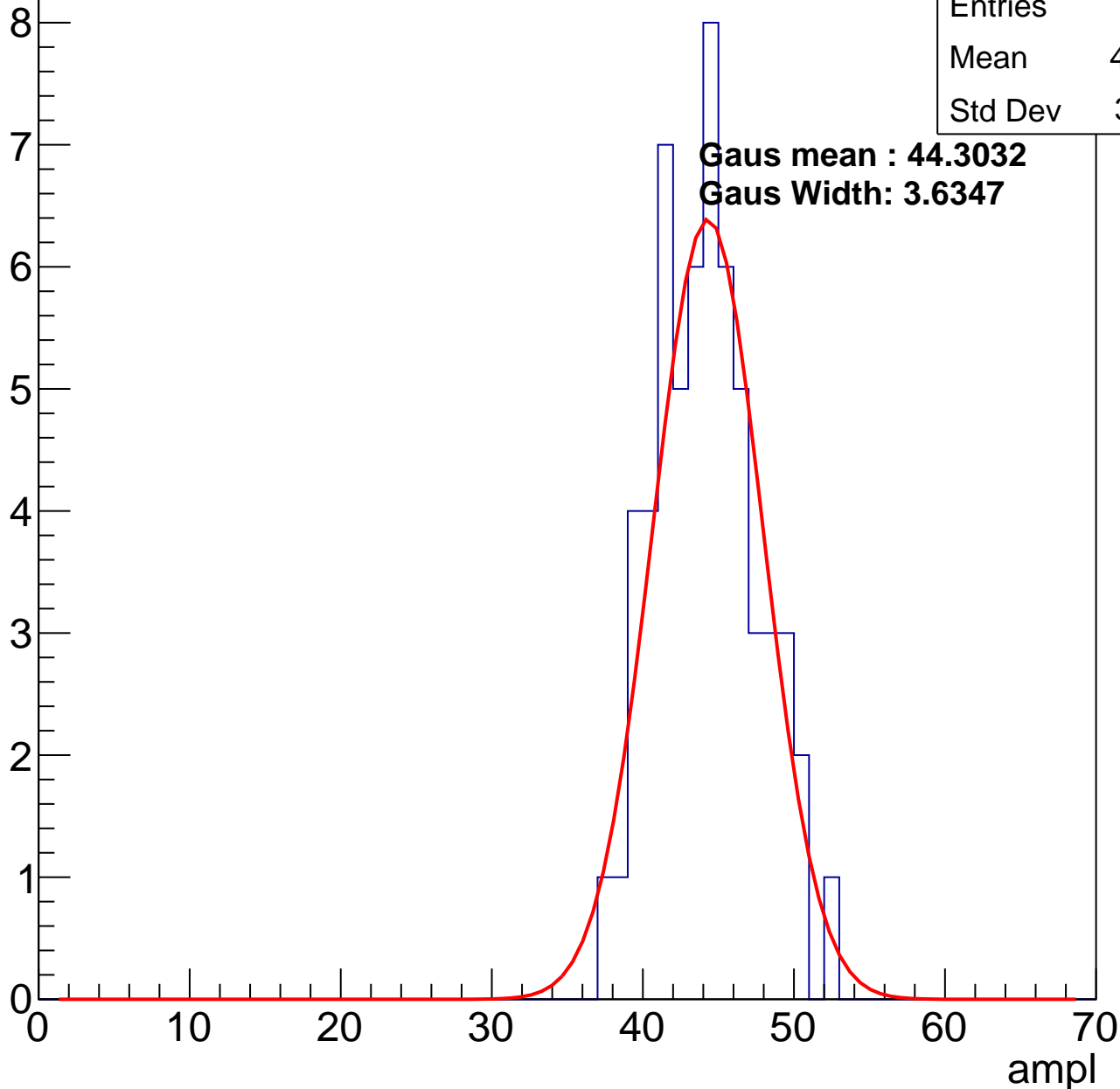
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	43.76
Std Dev	3.311

**Gaus mean : 44.3032**

**Gaus Width: 3.6347**

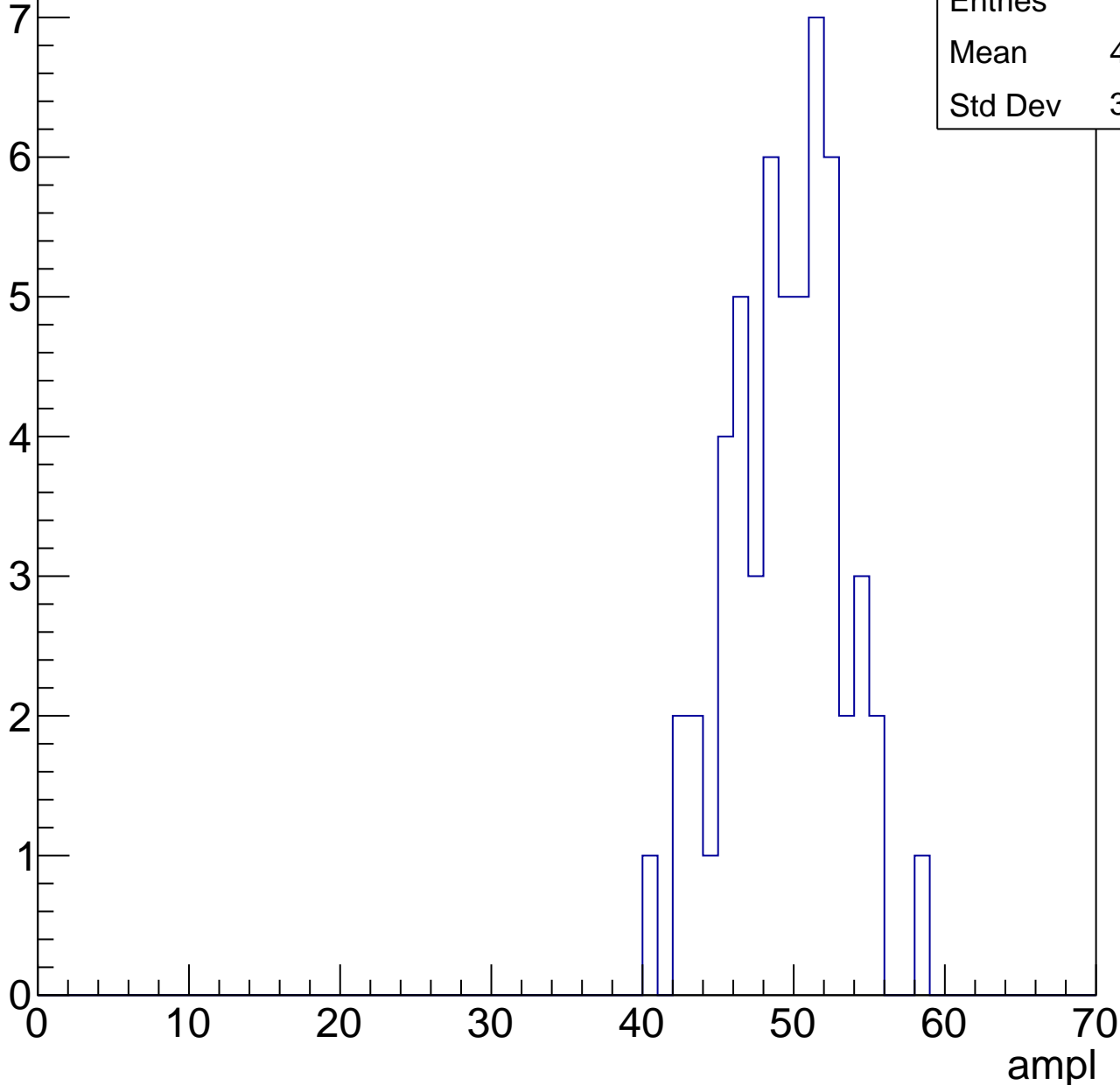


# B1L101S, U8-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	48.96
Std Dev	3.693

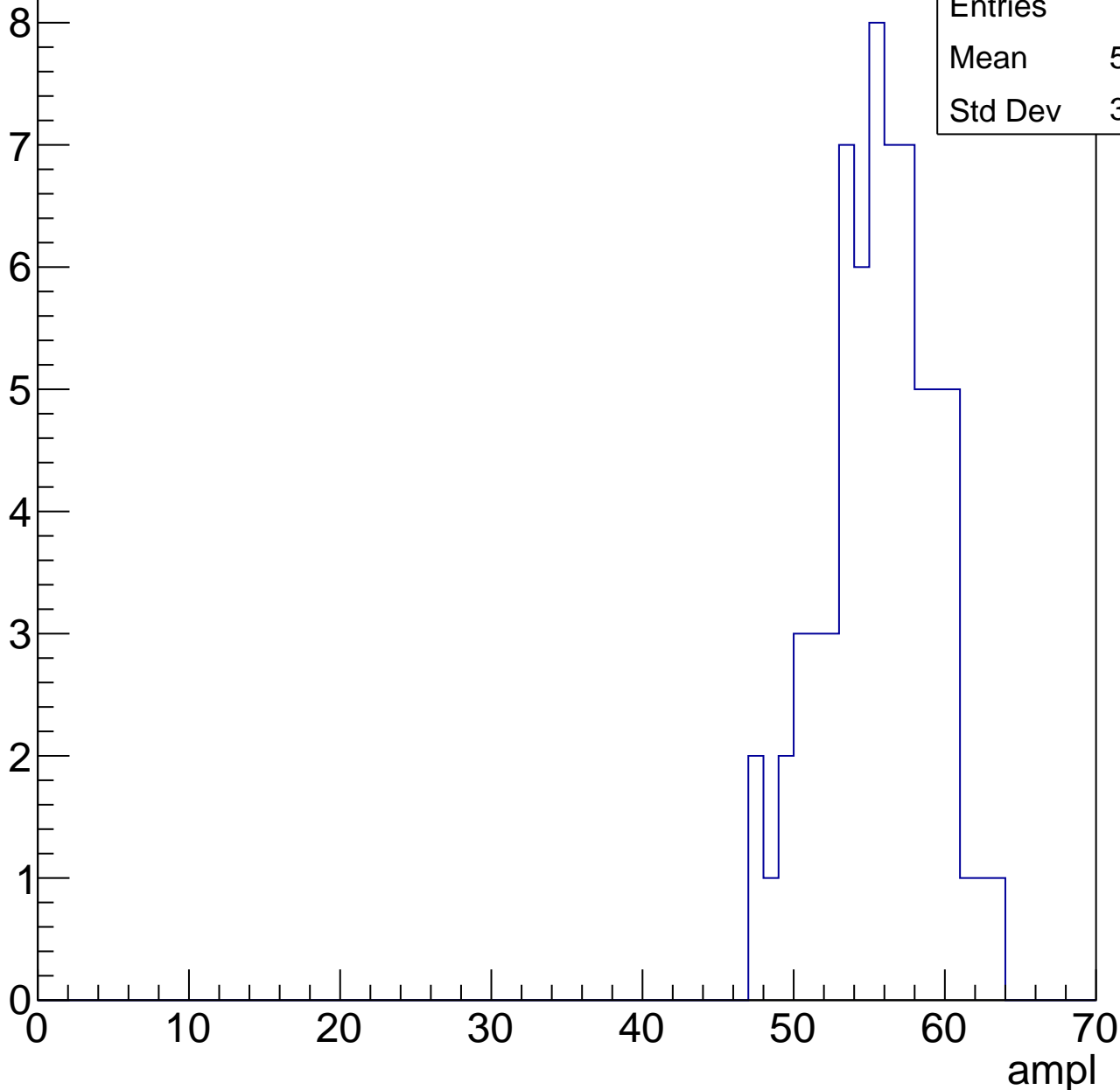


# B1L101S, U8-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	55.16
Std Dev	3.594

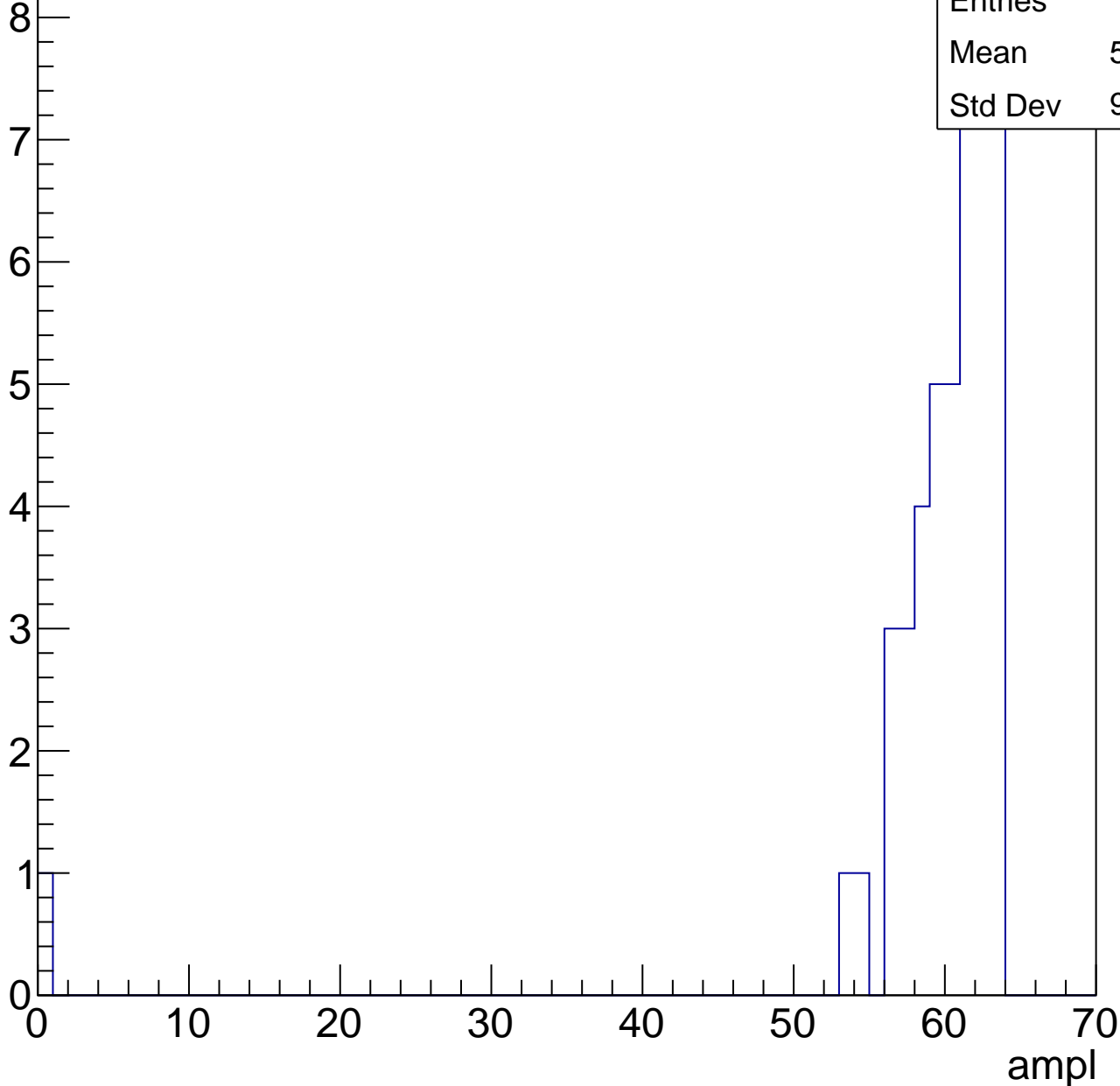


# B1L101S, U8-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

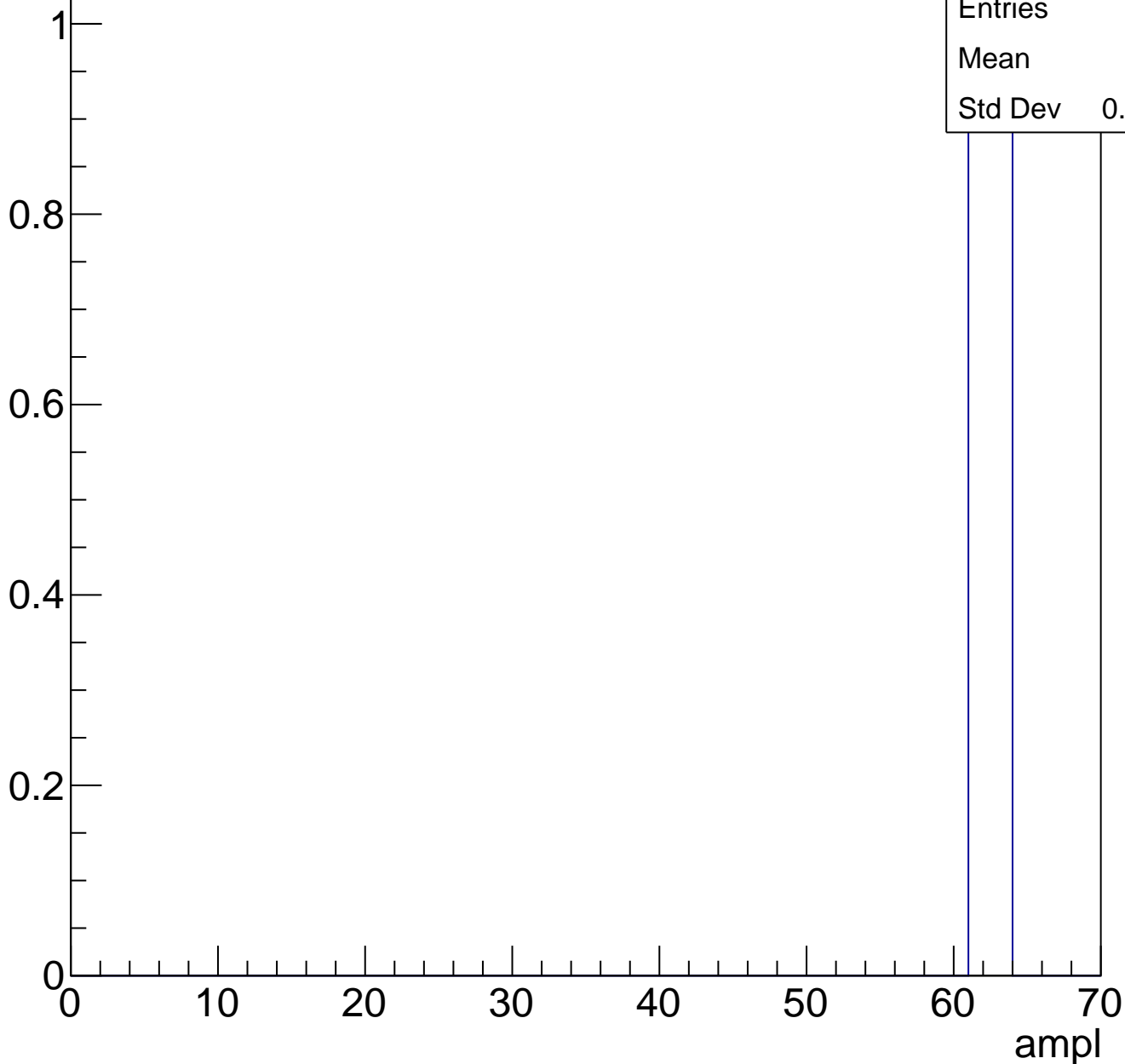
Entries	47
Mean	58.74
Std Dev	9.014



# B1L101S, U8-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U8-ch77, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	69
Mean	28.09
Std Dev	5.81

**Gaus mean : 29.2314**

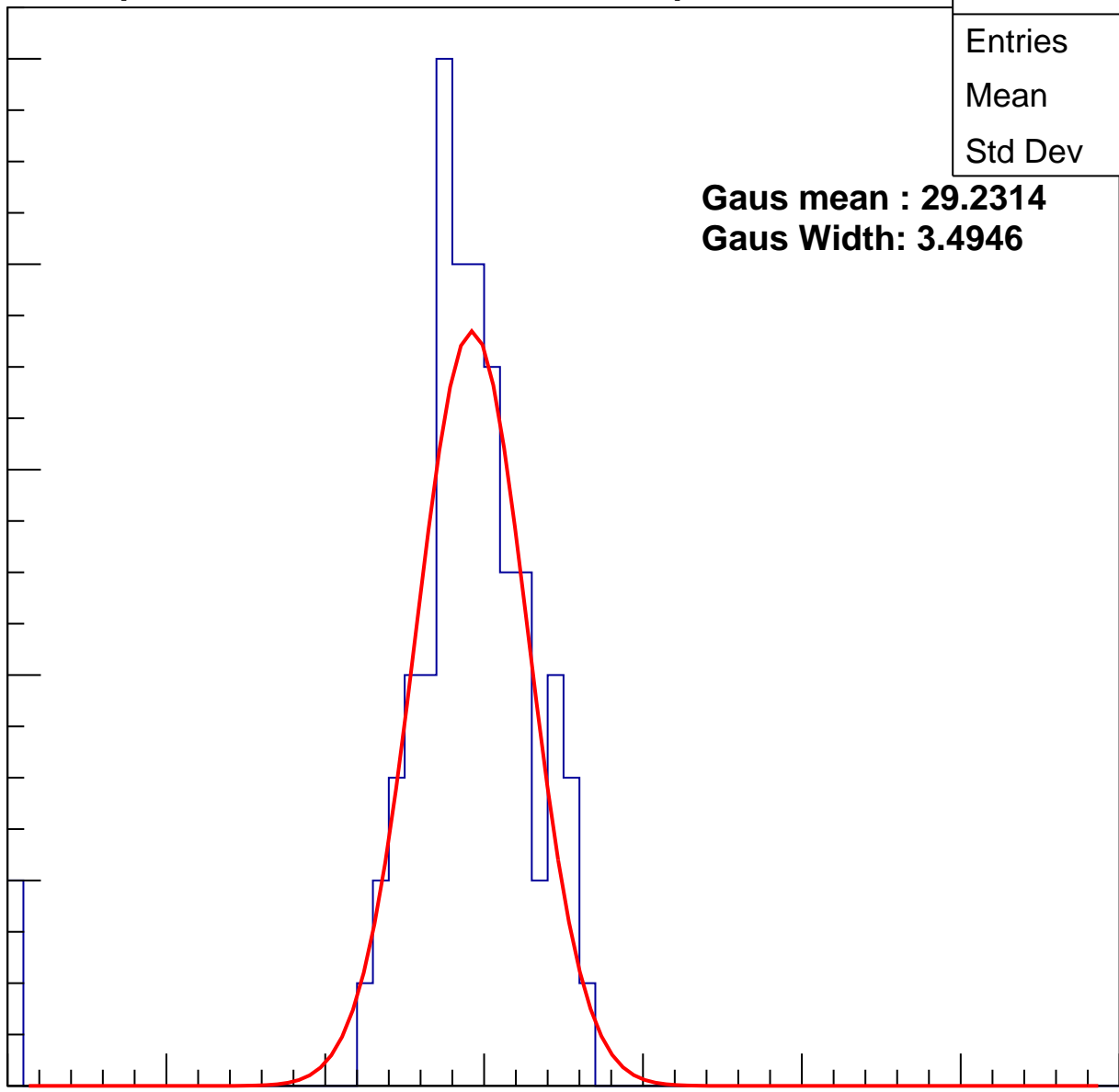
**Gaus Width: 3.4946**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U8-ch77, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	36
Std Dev	3.276

**Gaus mean : 36.2915**

**Gaus Width: 4.0034**

10

8

6

4

2

0

0

10

20

30

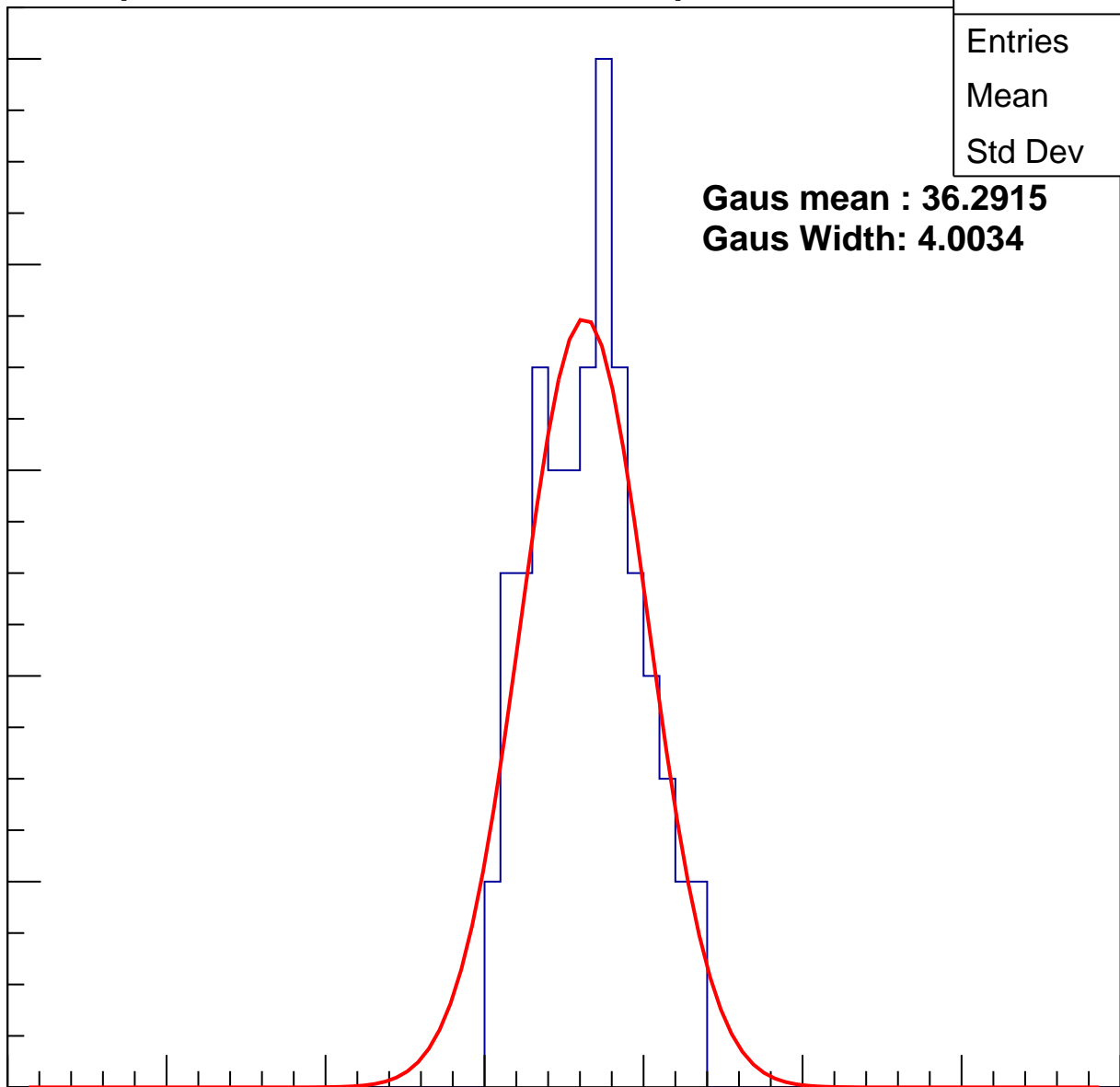
40

50

60

70

ampl



# B1L101S, U8-ch77, adc2

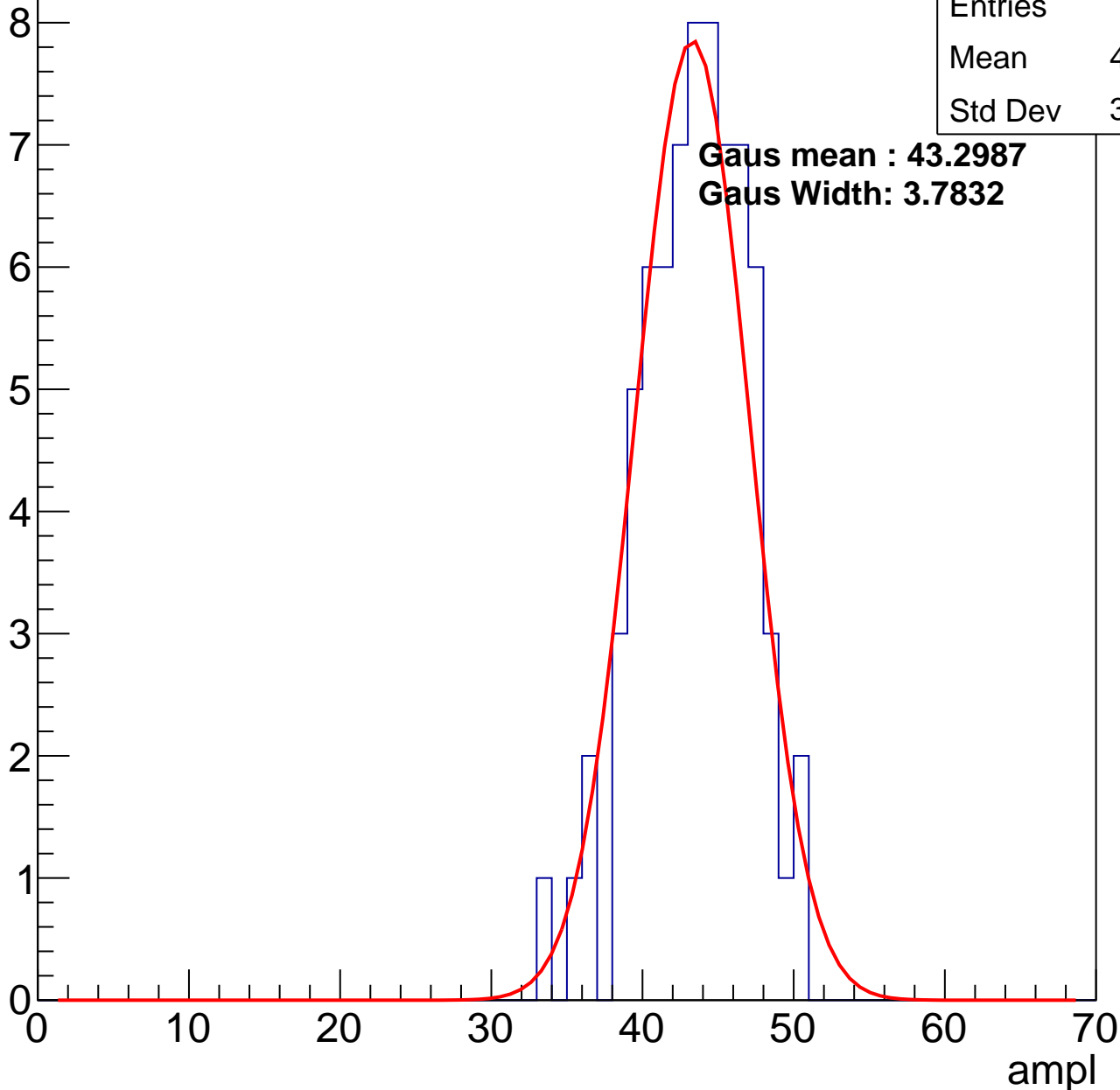
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	42.97
Std Dev	3.523

**Gaus mean : 43.2987**

**Gaus Width: 3.7832**

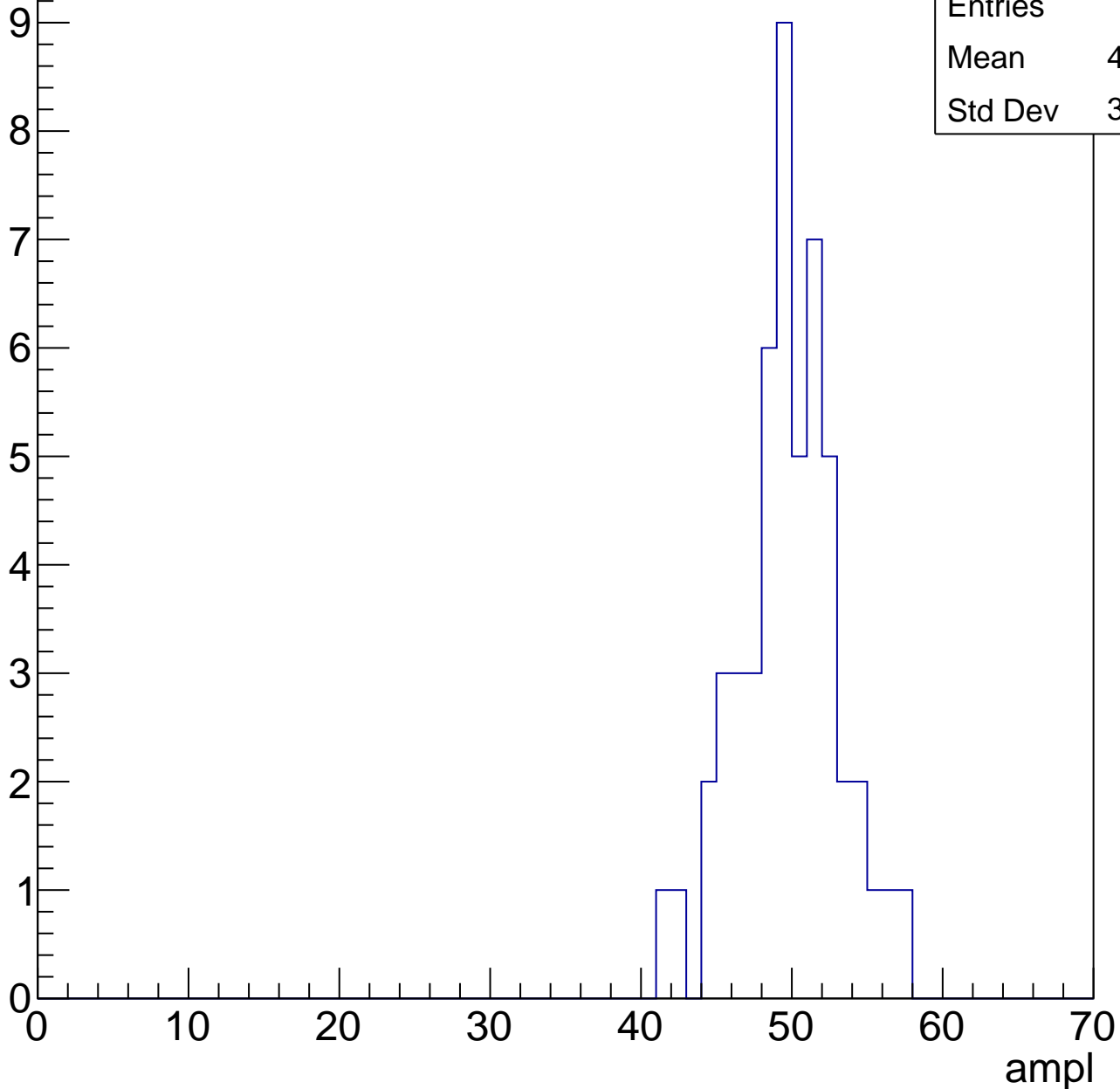


# B1L101S, U8-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	49.29
Std Dev	3.284

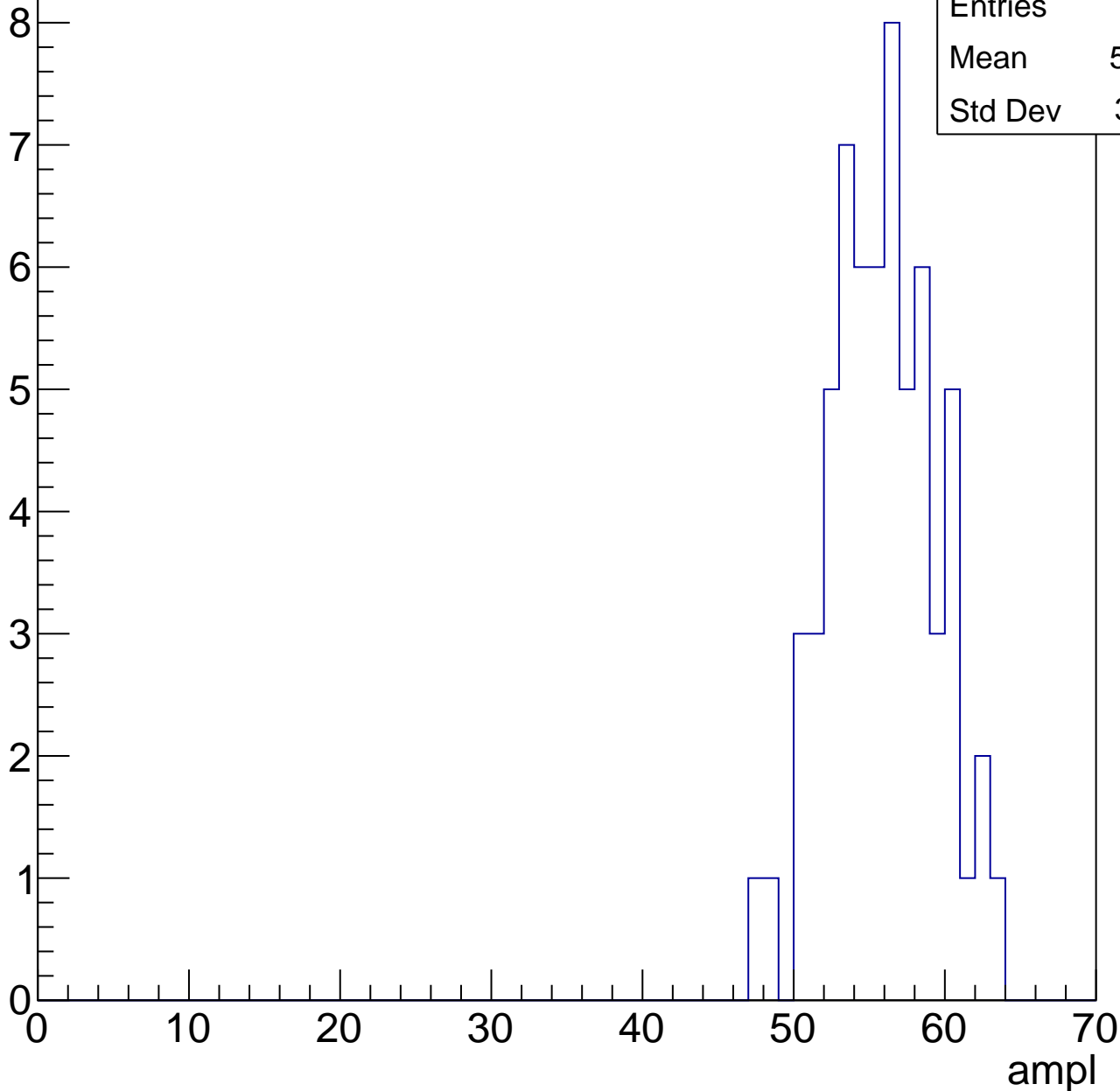


# B1L101S, U8-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	55.38
Std Dev	3.471



# B1L101S, U8-ch77, adc5

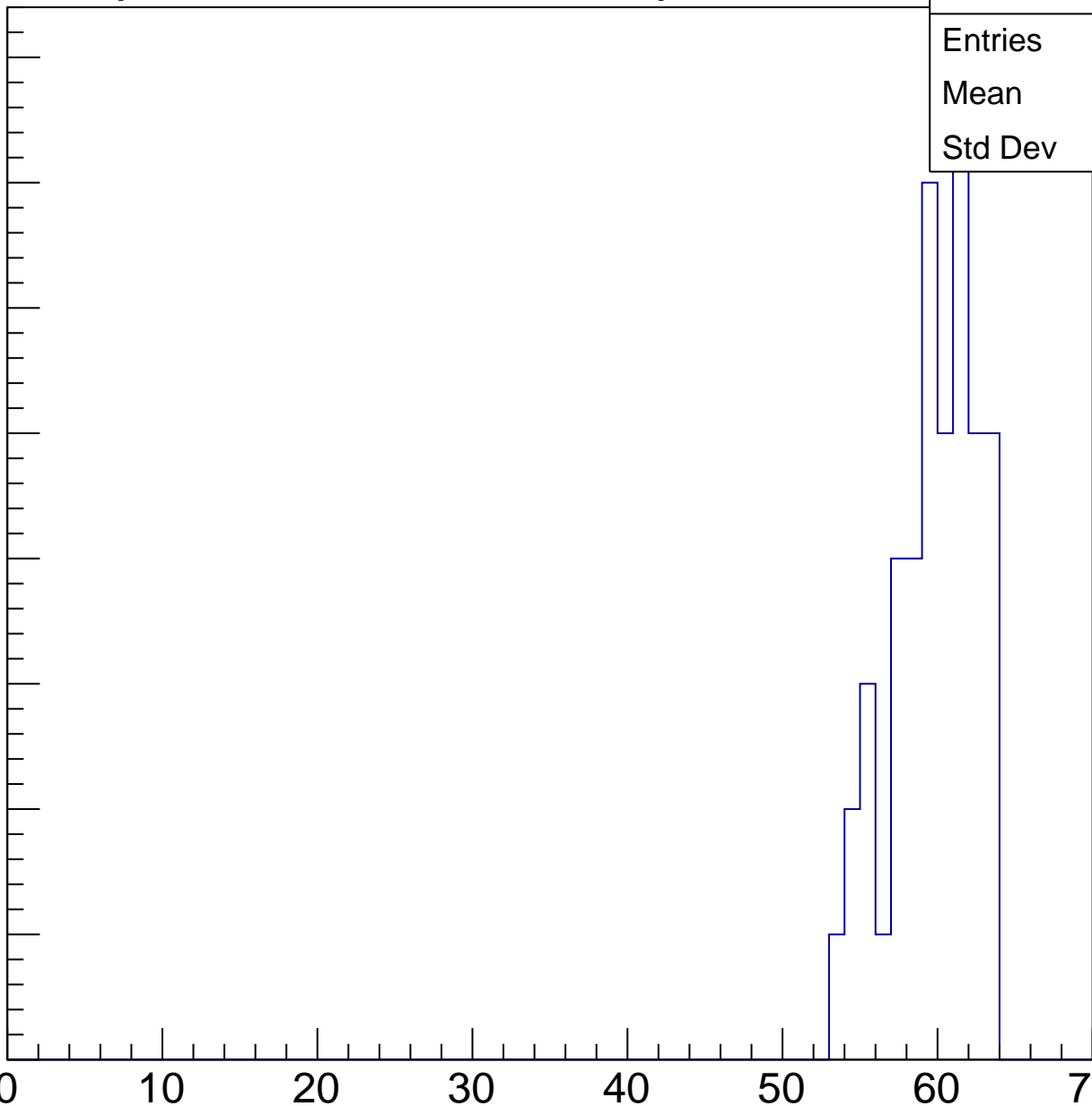
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	45
Mean	59.29
Std Dev	2.672

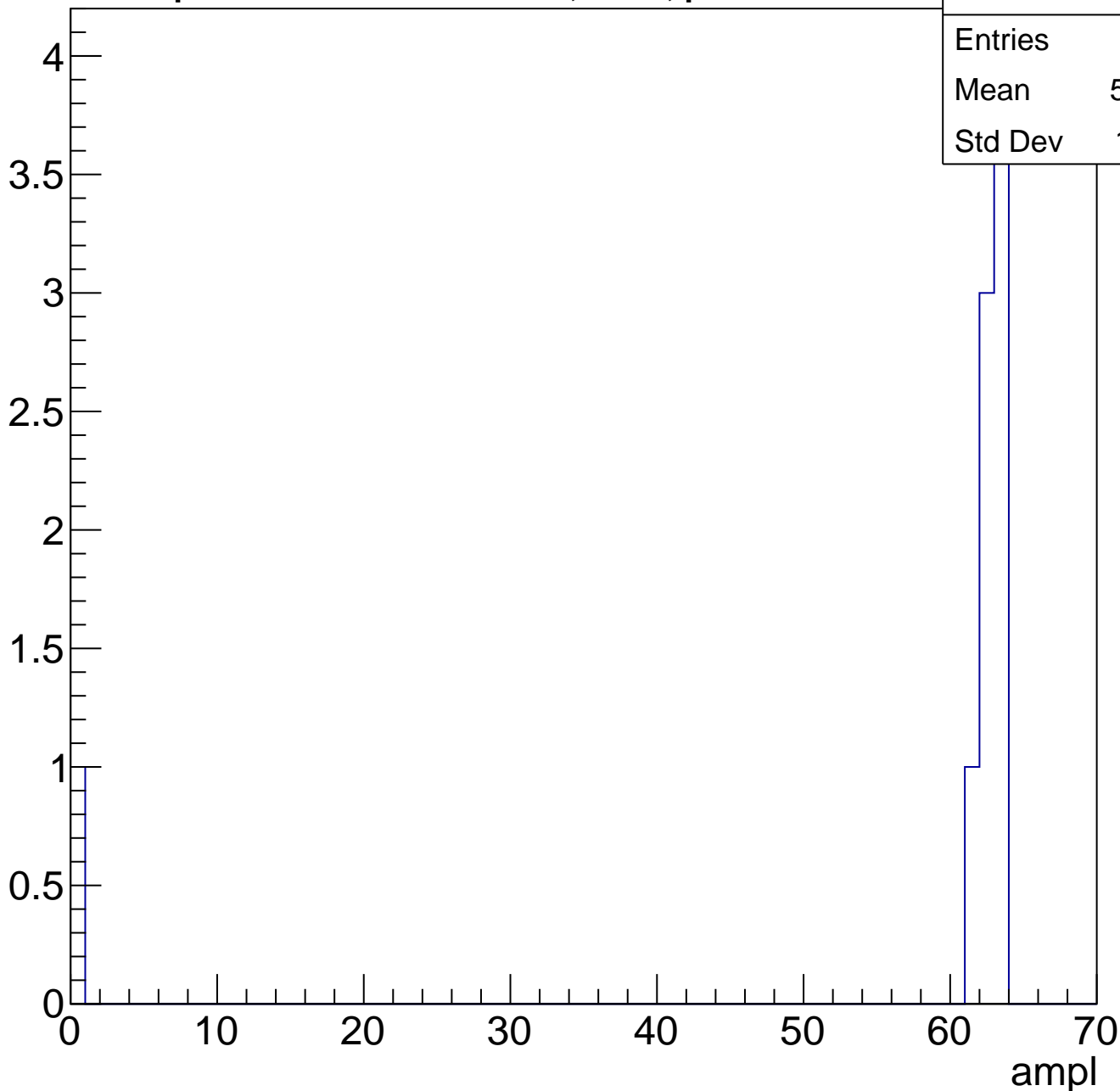
ampl



# B1L101S, U8-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

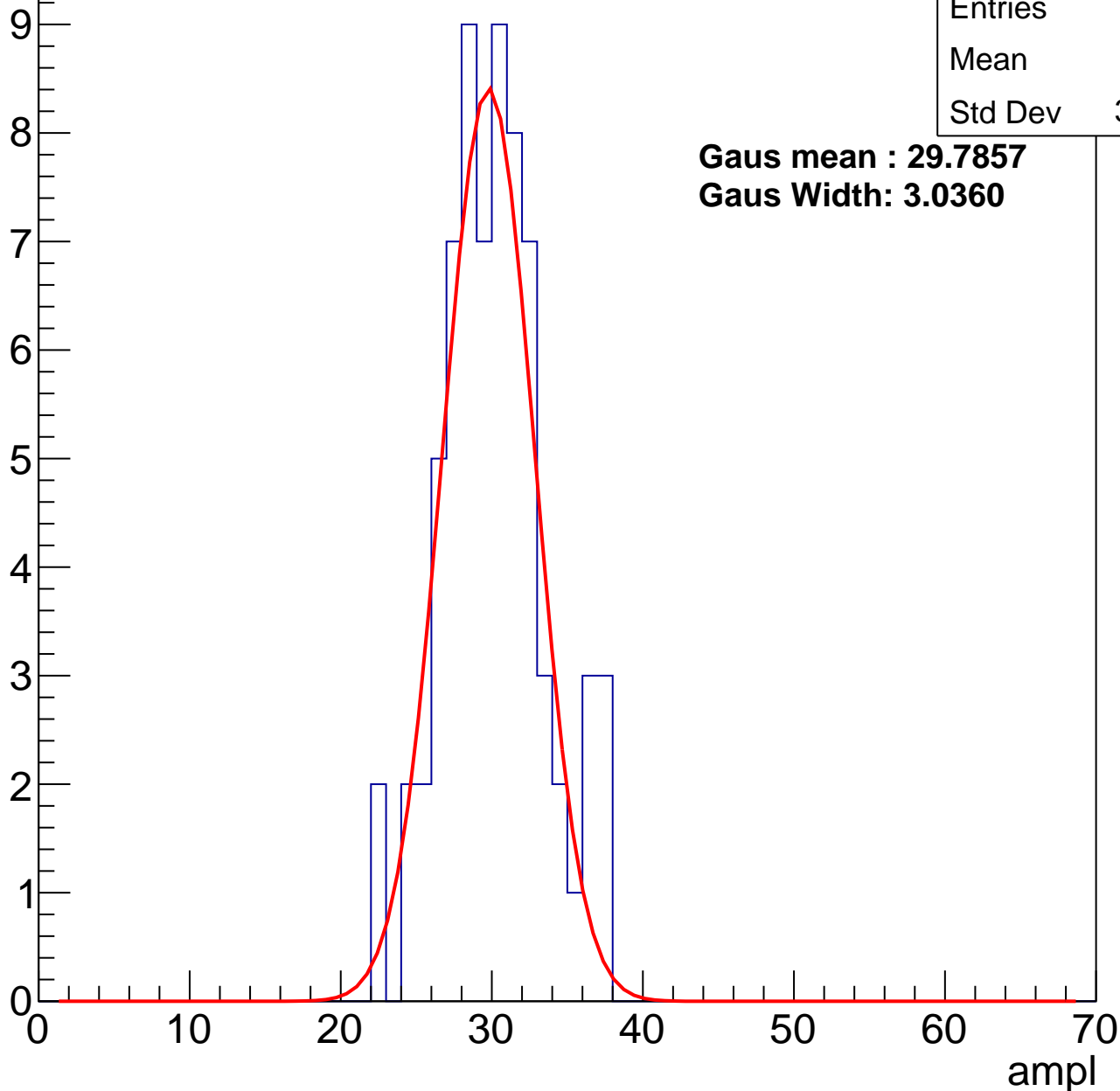
Entry



# B1L101S, U8-ch78, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch78, adc1

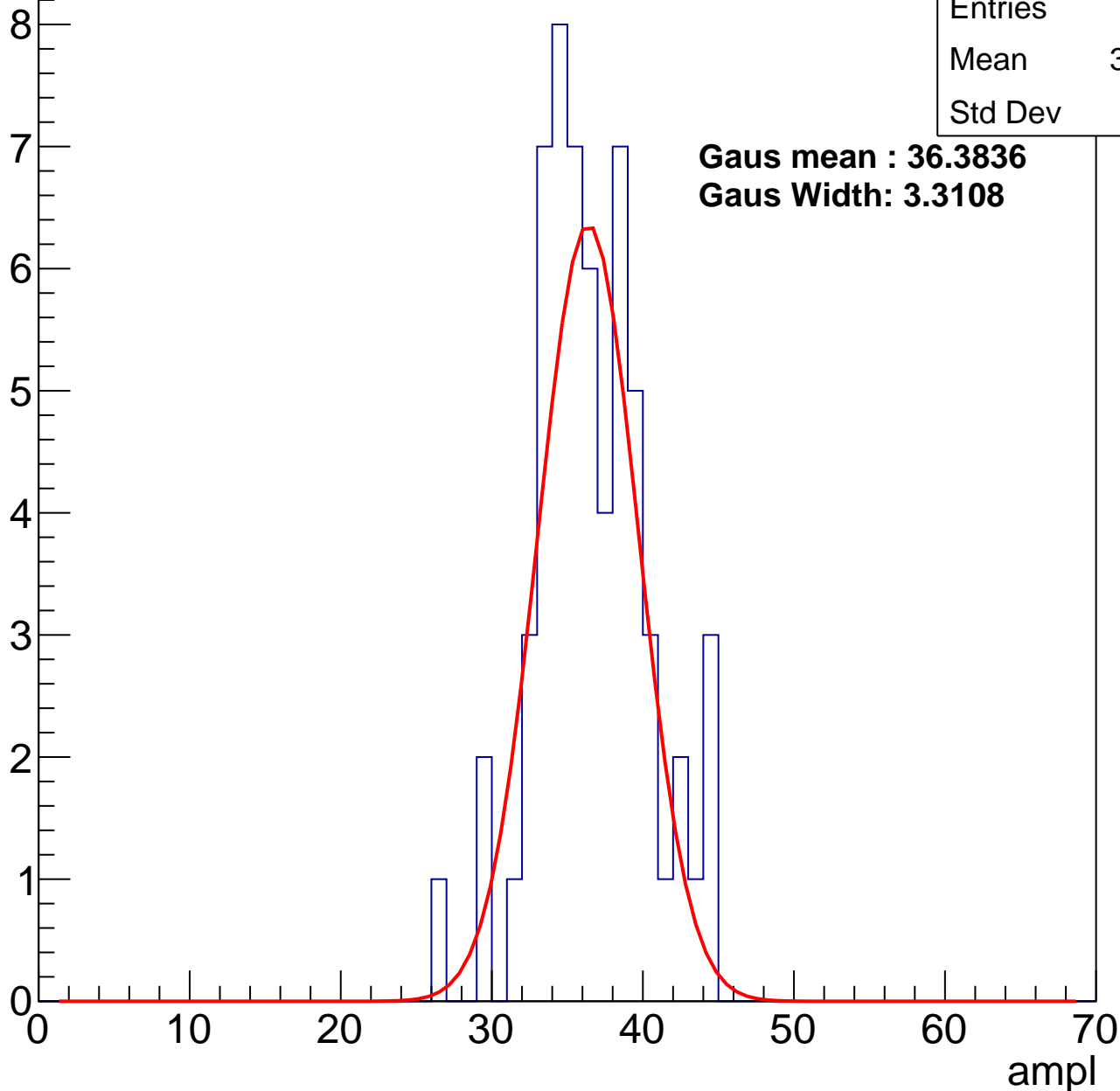
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	36.13
Std Dev	3.7

**Gaus mean : 36.3836**

**Gaus Width: 3.3108**



# B1L101S, U8-ch78, adc2

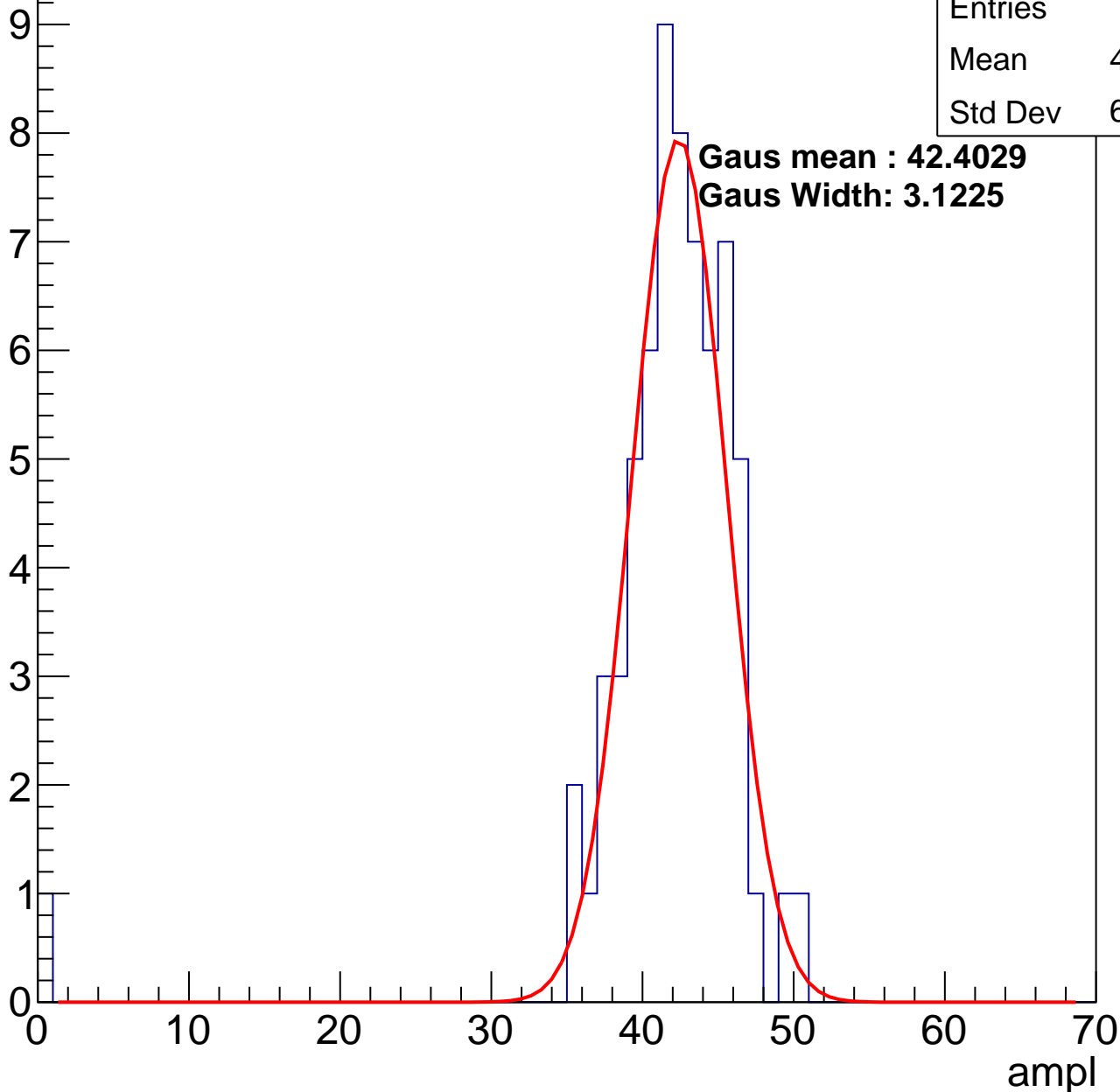
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	41.32
Std Dev	6.005

**Gaus mean : 42.4029**

**Gaus Width: 3.1225**

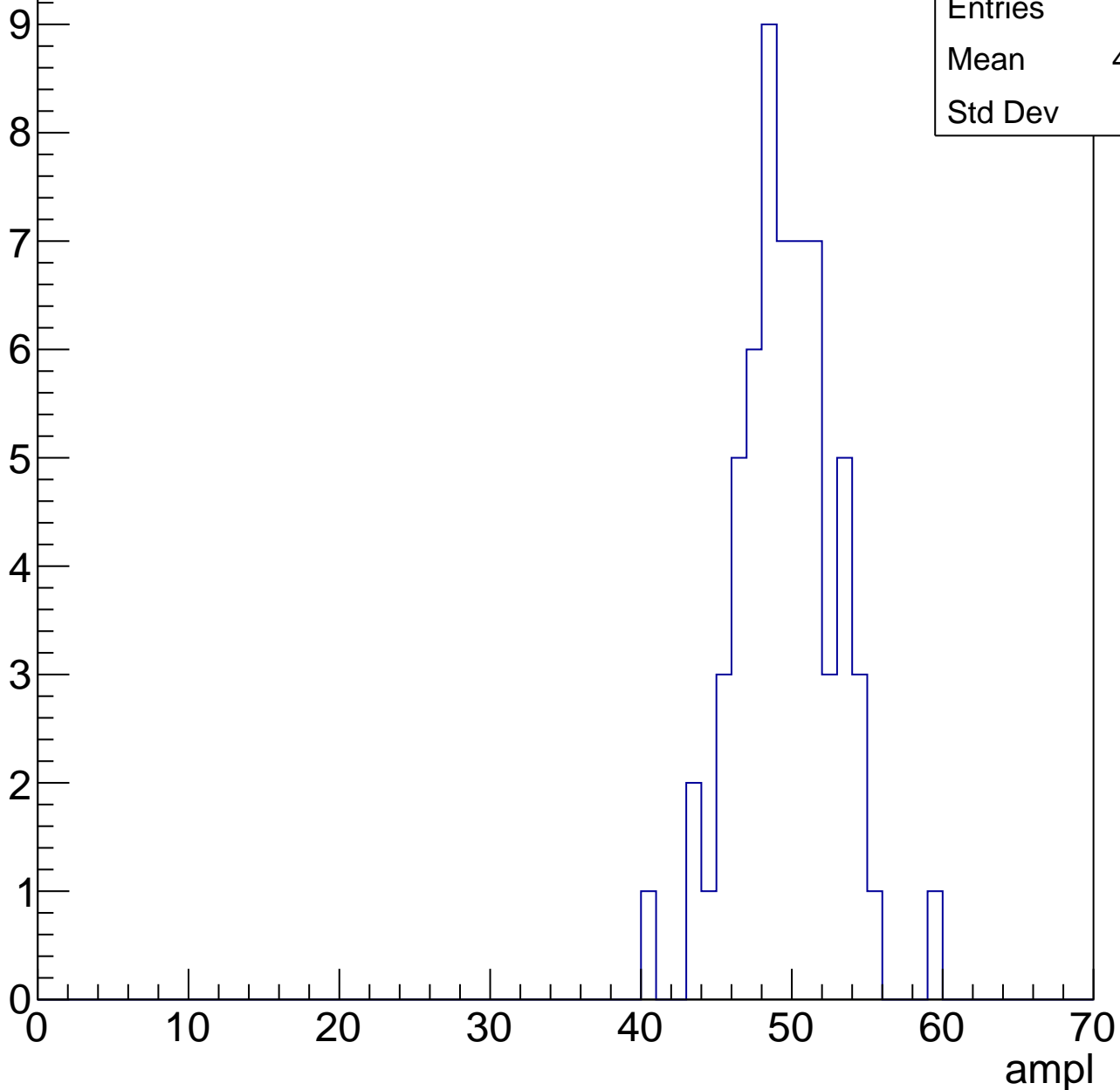


# B1L101S, U8-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	49.11
Std Dev	3.28

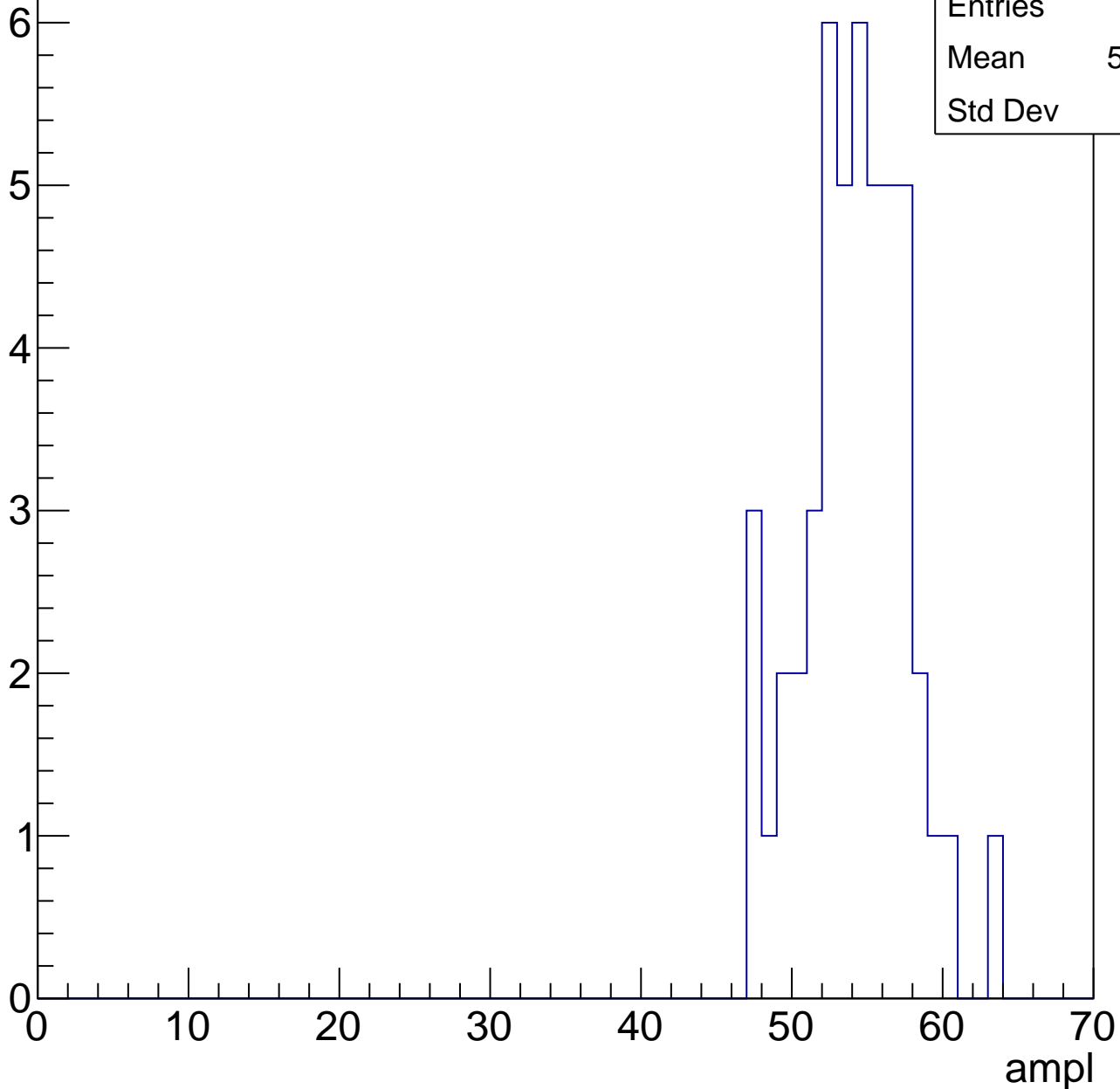


# B1L101S, U8-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	53.73
Std Dev	3.42



# B1L101S, U8-ch78, adc5

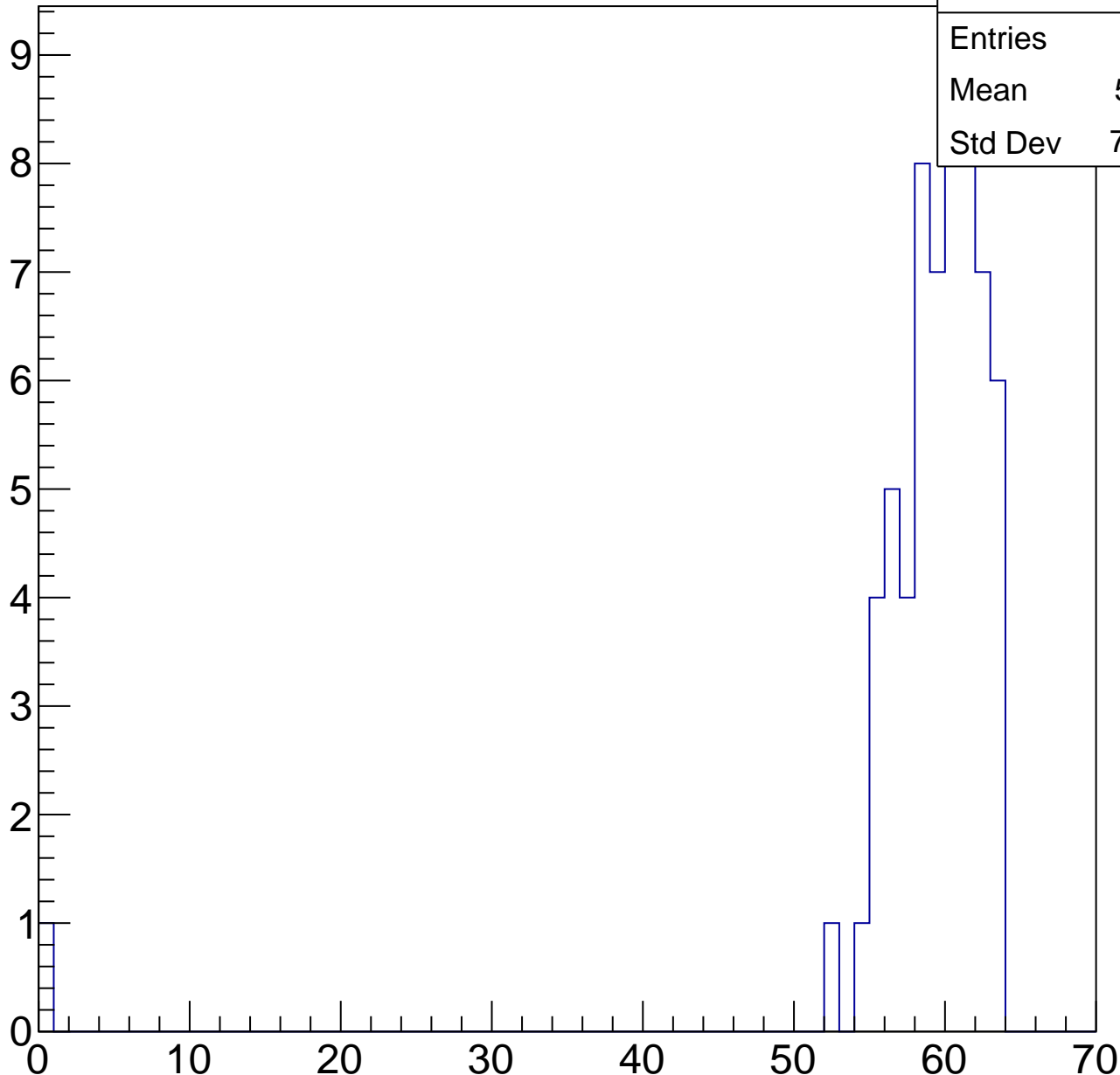
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	61
Mean	58.21
Std Dev	7.945

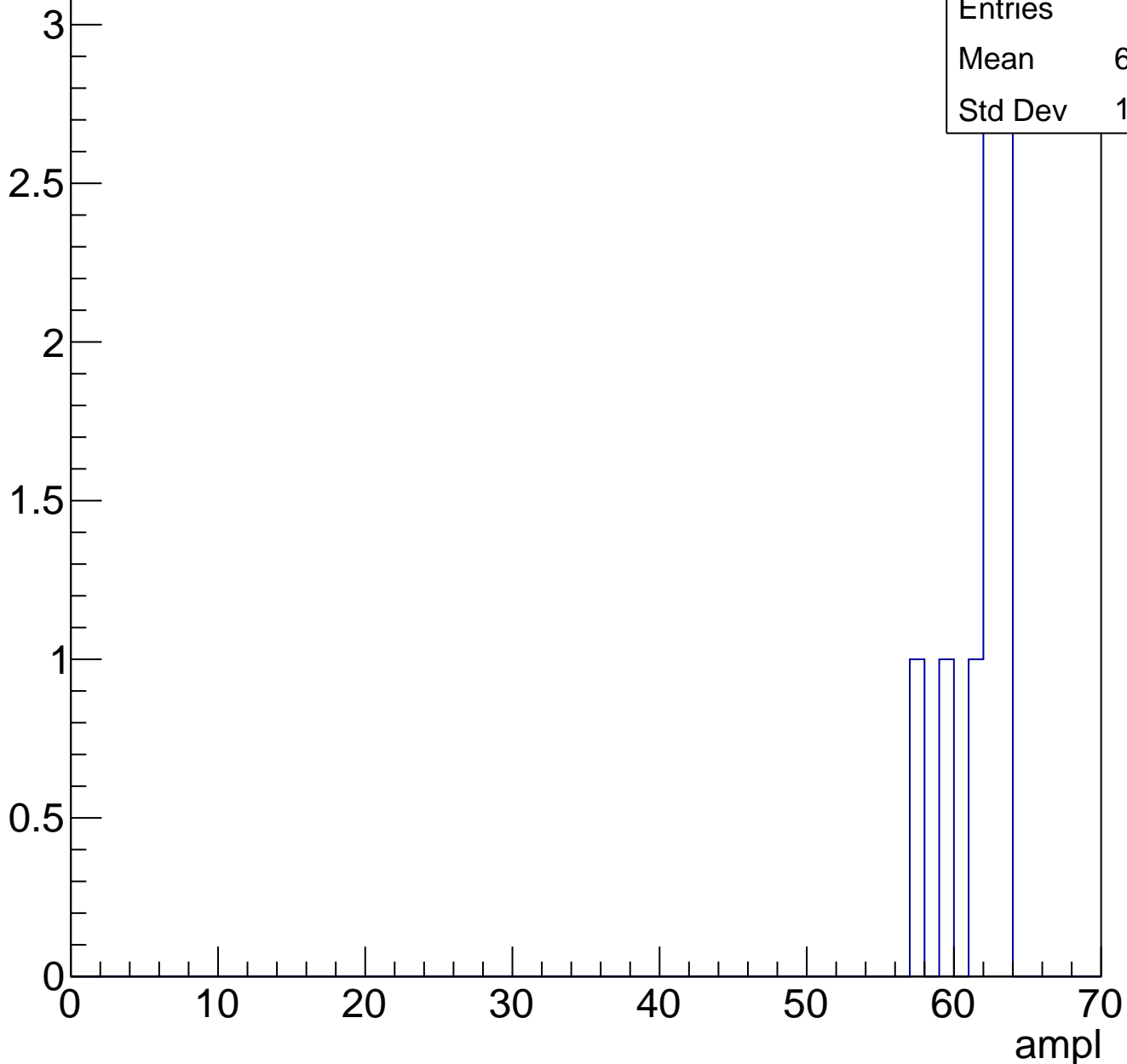
ampl



# B1L101S, U8-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

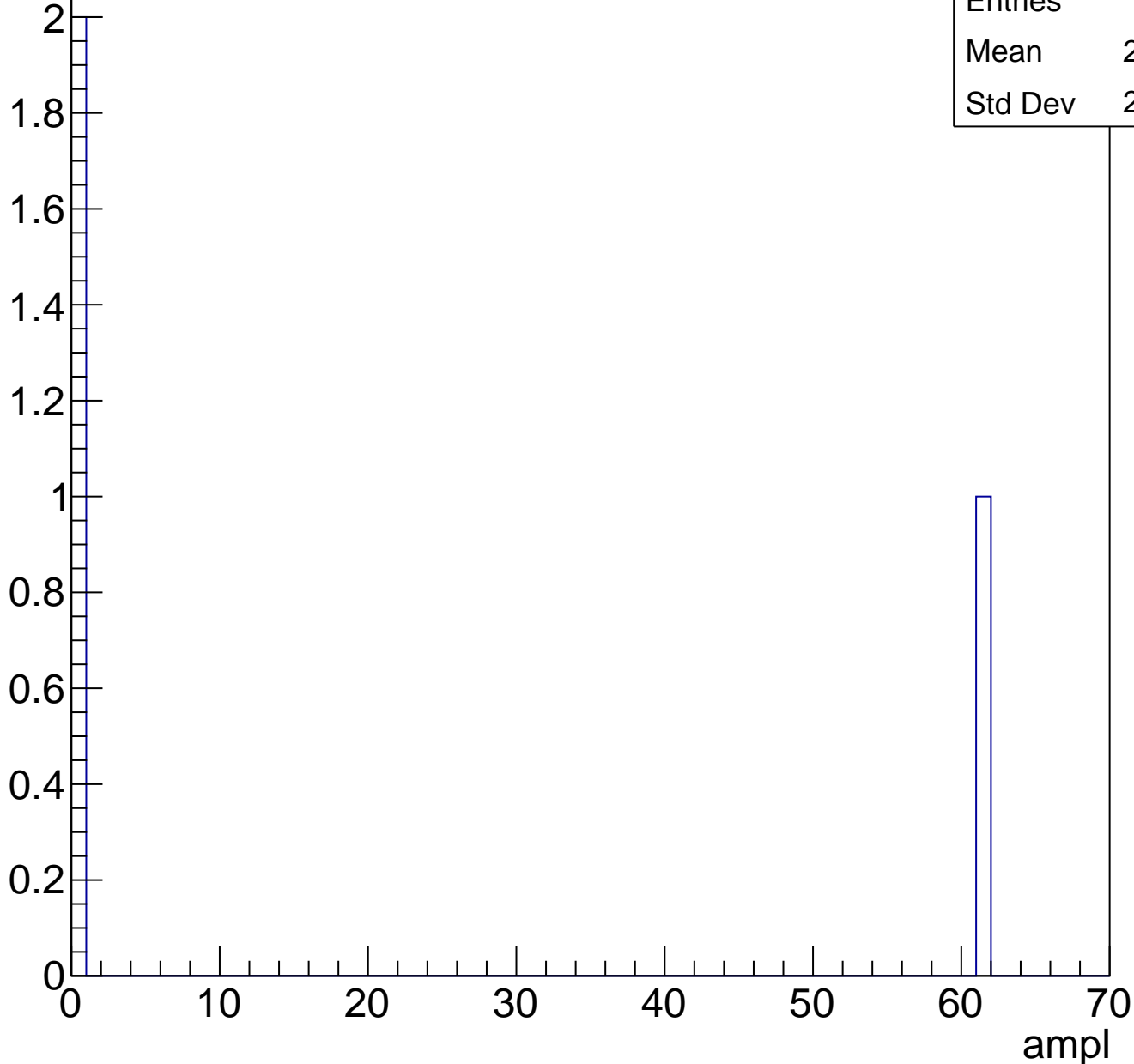




# B1L101S, U8-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch79, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	77
Mean	29.31
Std Dev	5.664

**Gaus mean : 30.5396**

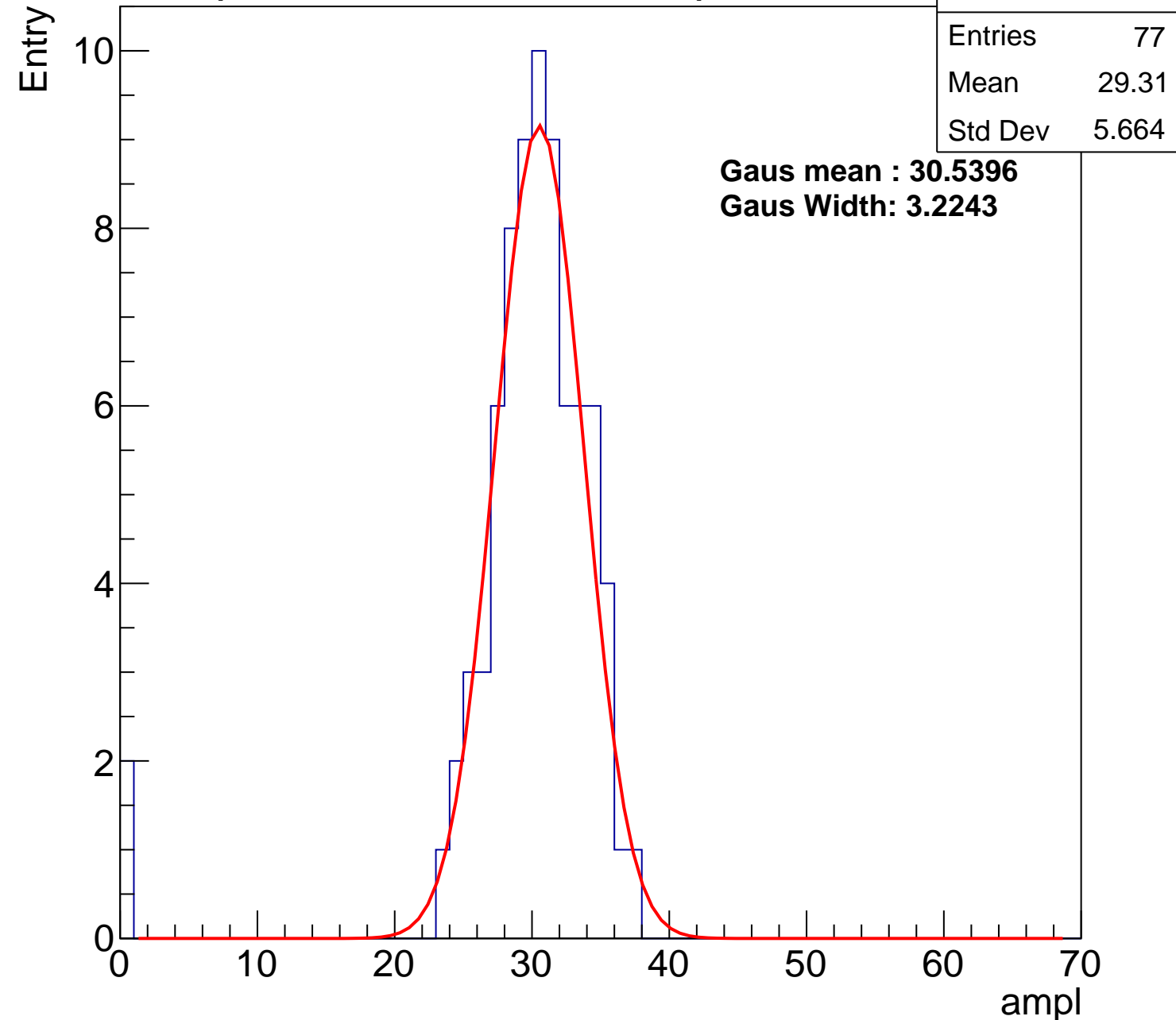
**Gaus Width: 3.2243**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U8-ch79, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	78
Mean	38.28
Std Dev	3.612

**Gaus mean : 38.5063**

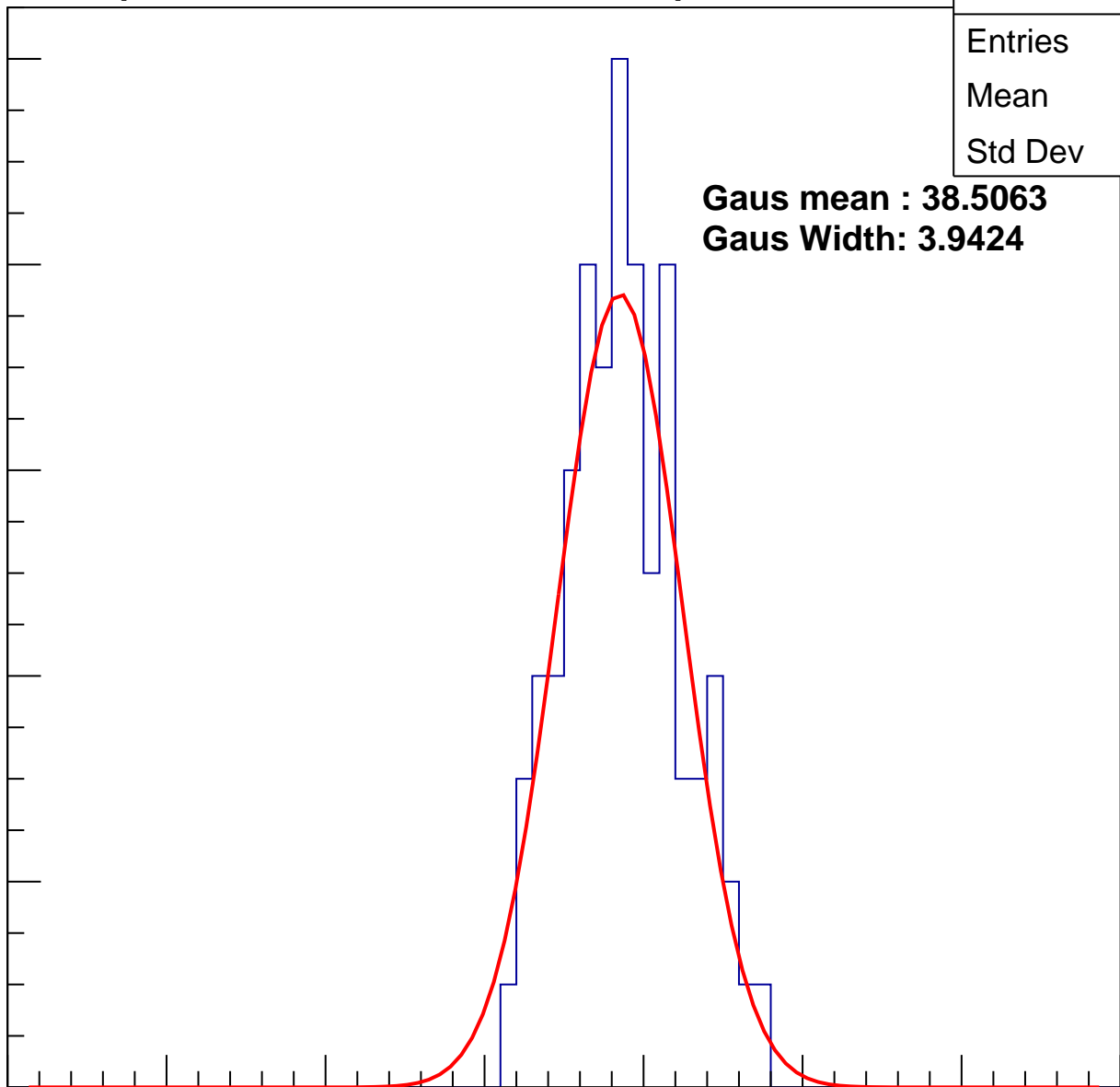
**Gaus Width: 3.9424**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U8-ch79, adc2

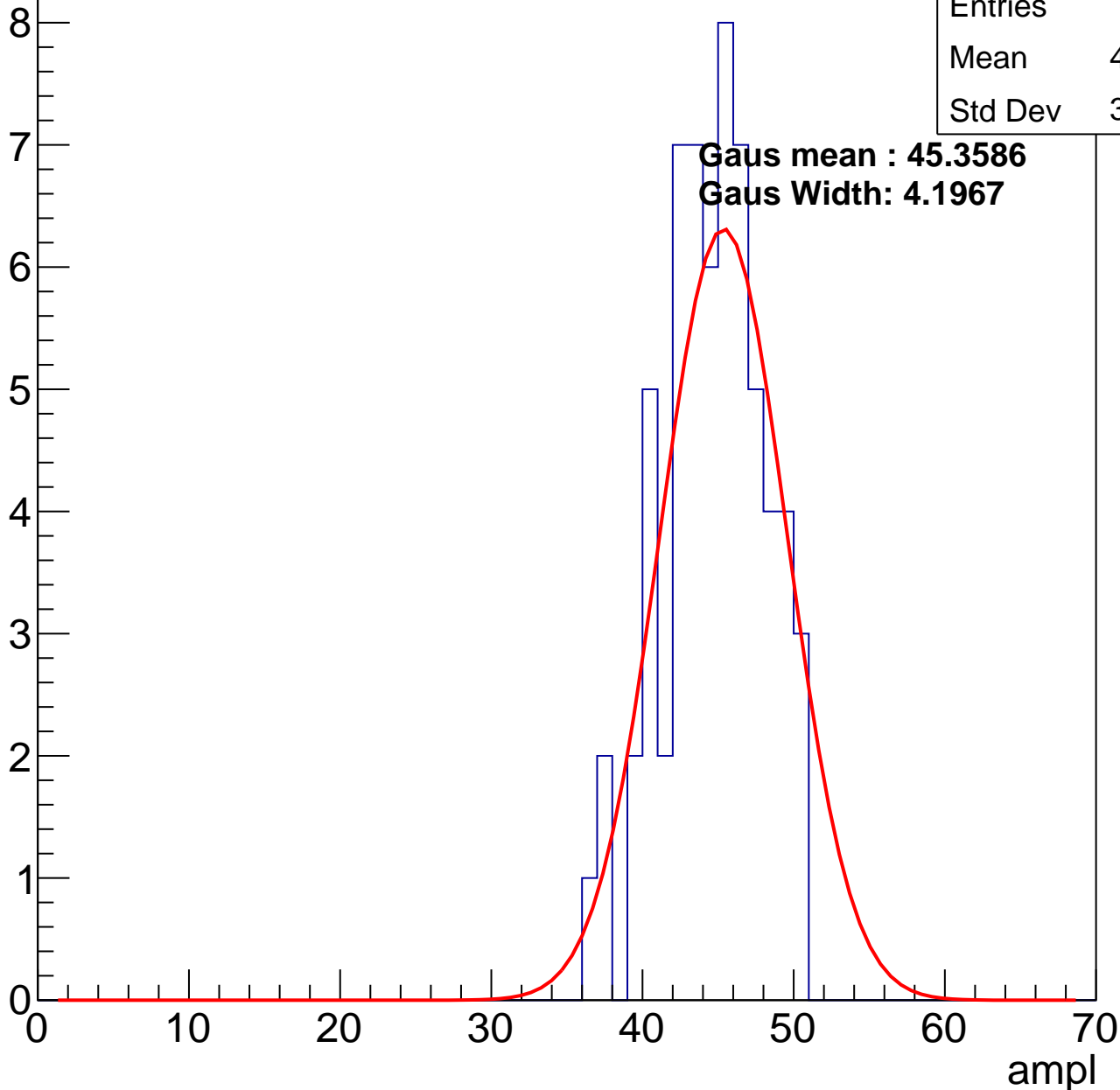
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	44.19
Std Dev	3.323

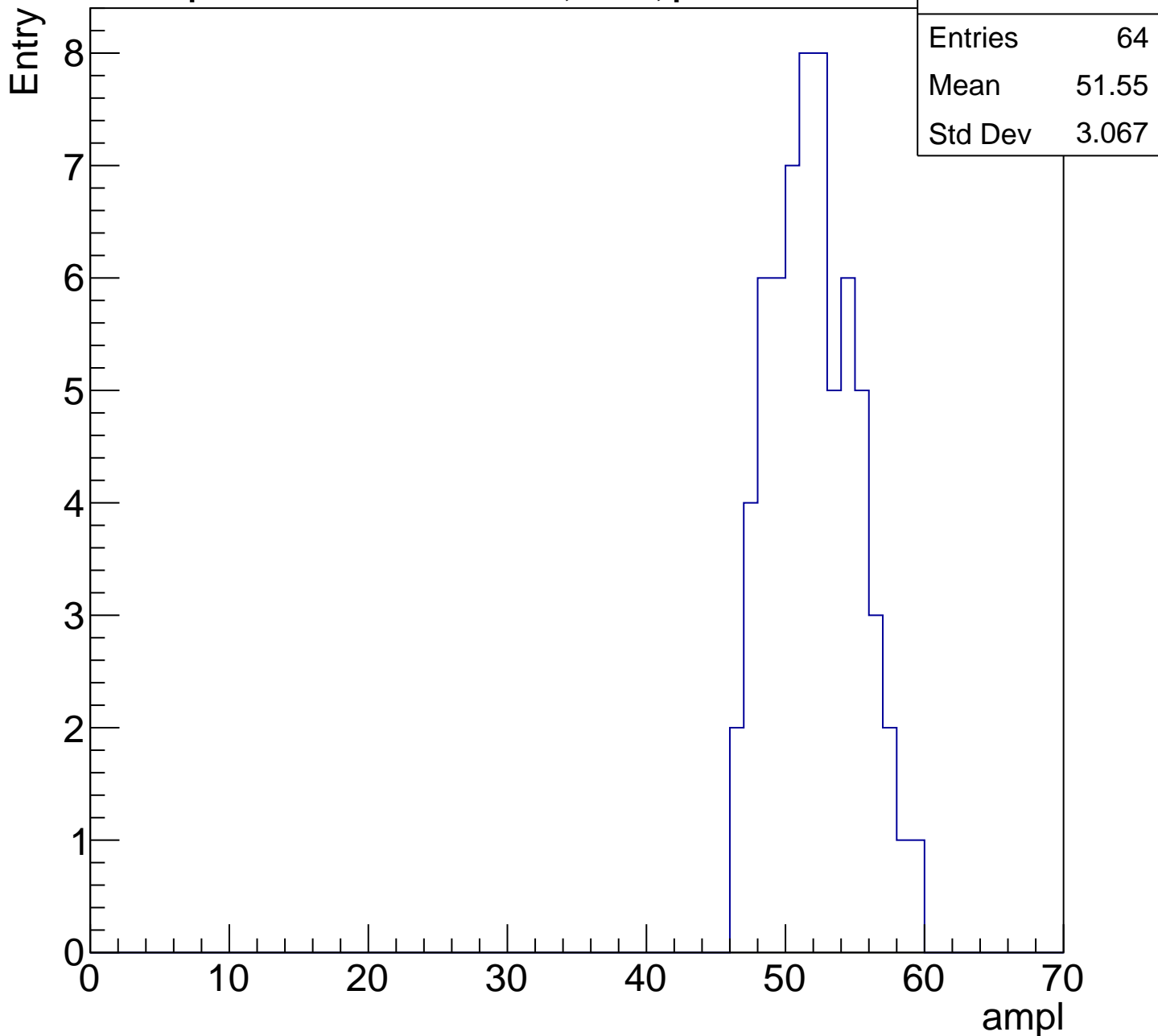
**Gaus mean : 45.3586**

**Gaus Width: 4.1967**



# B1L101S, U8-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

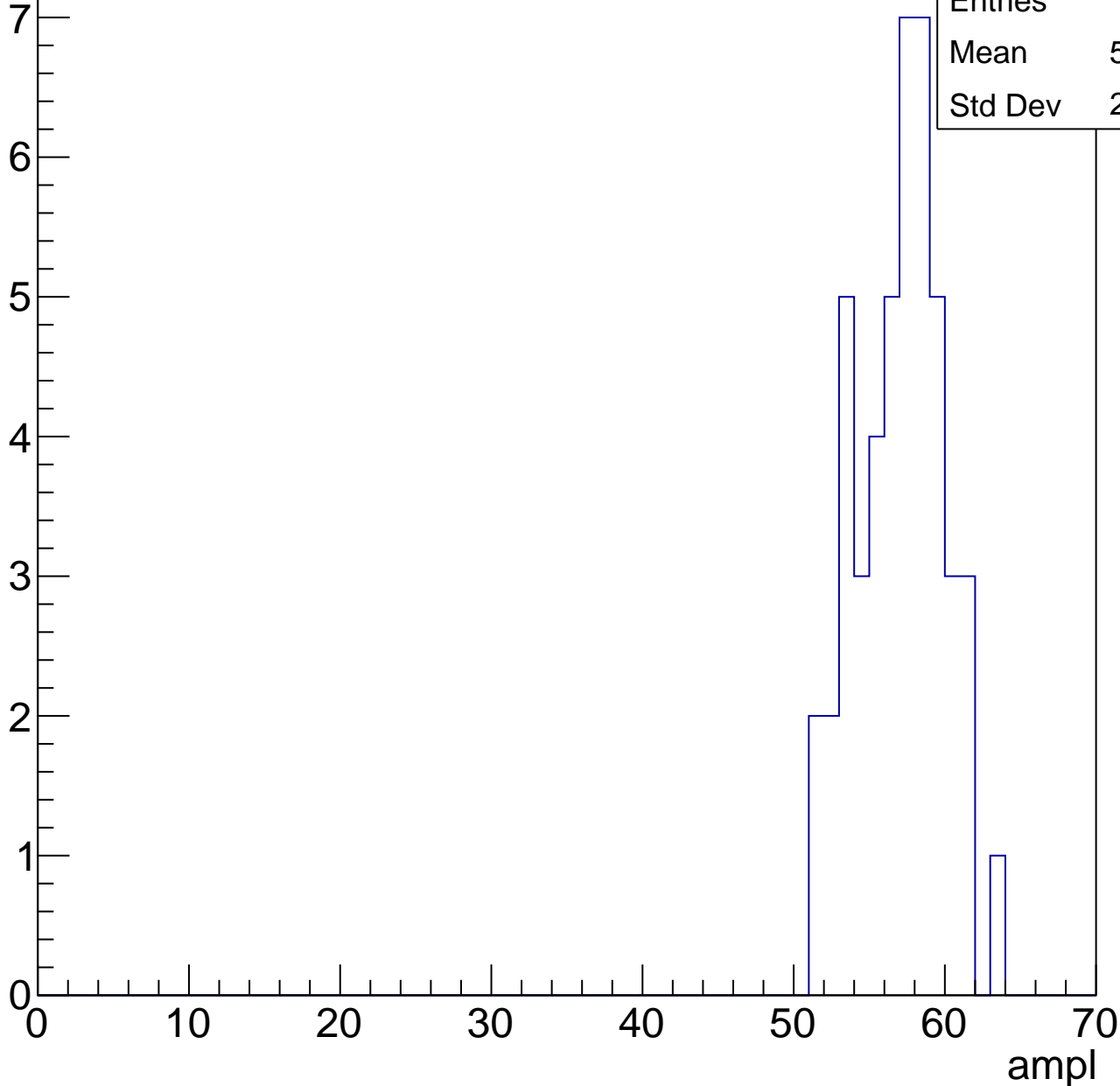


# B1L101S, U8-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	56.57
Std Dev	2.842

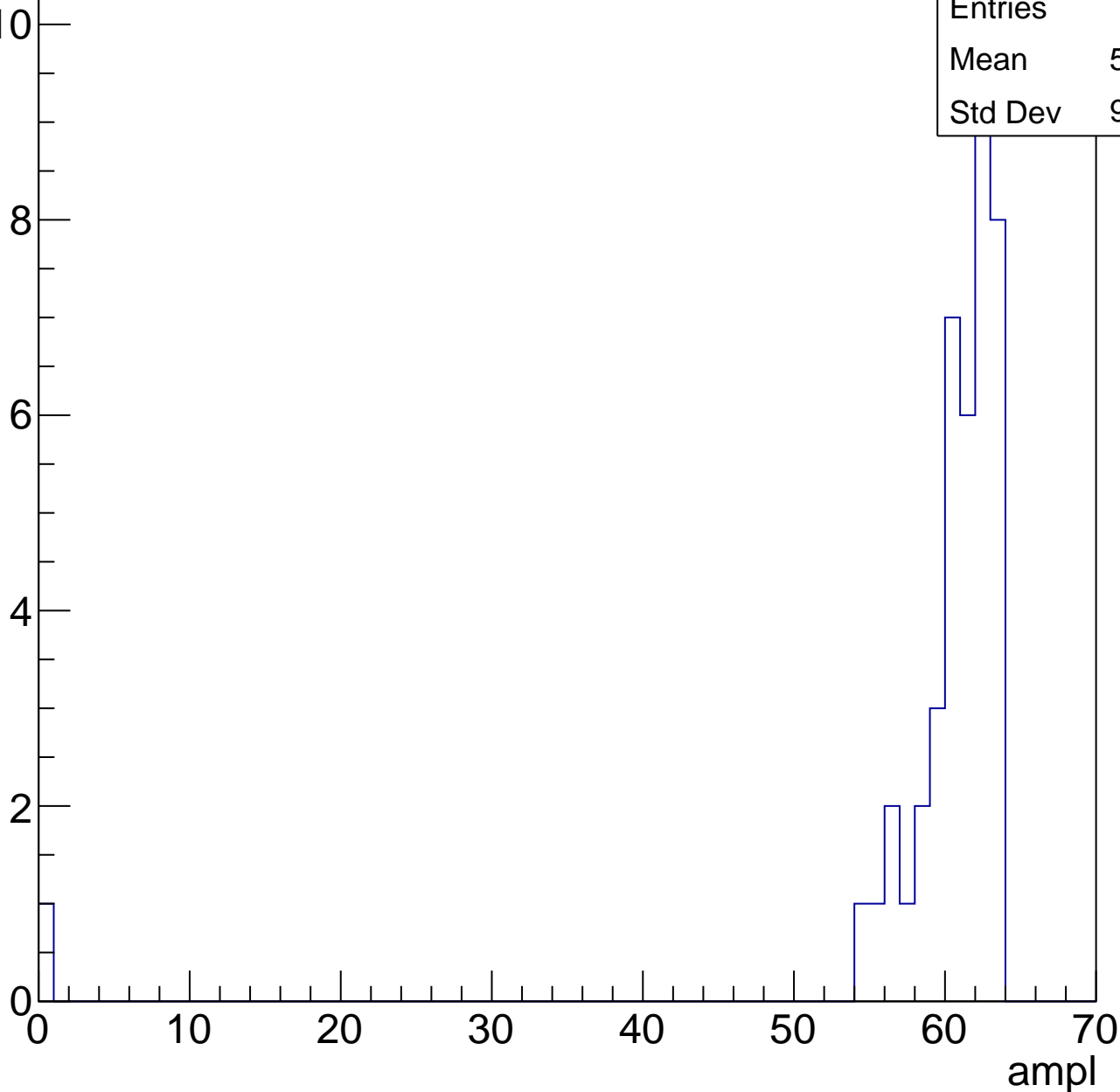


# B1L101S, U8-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

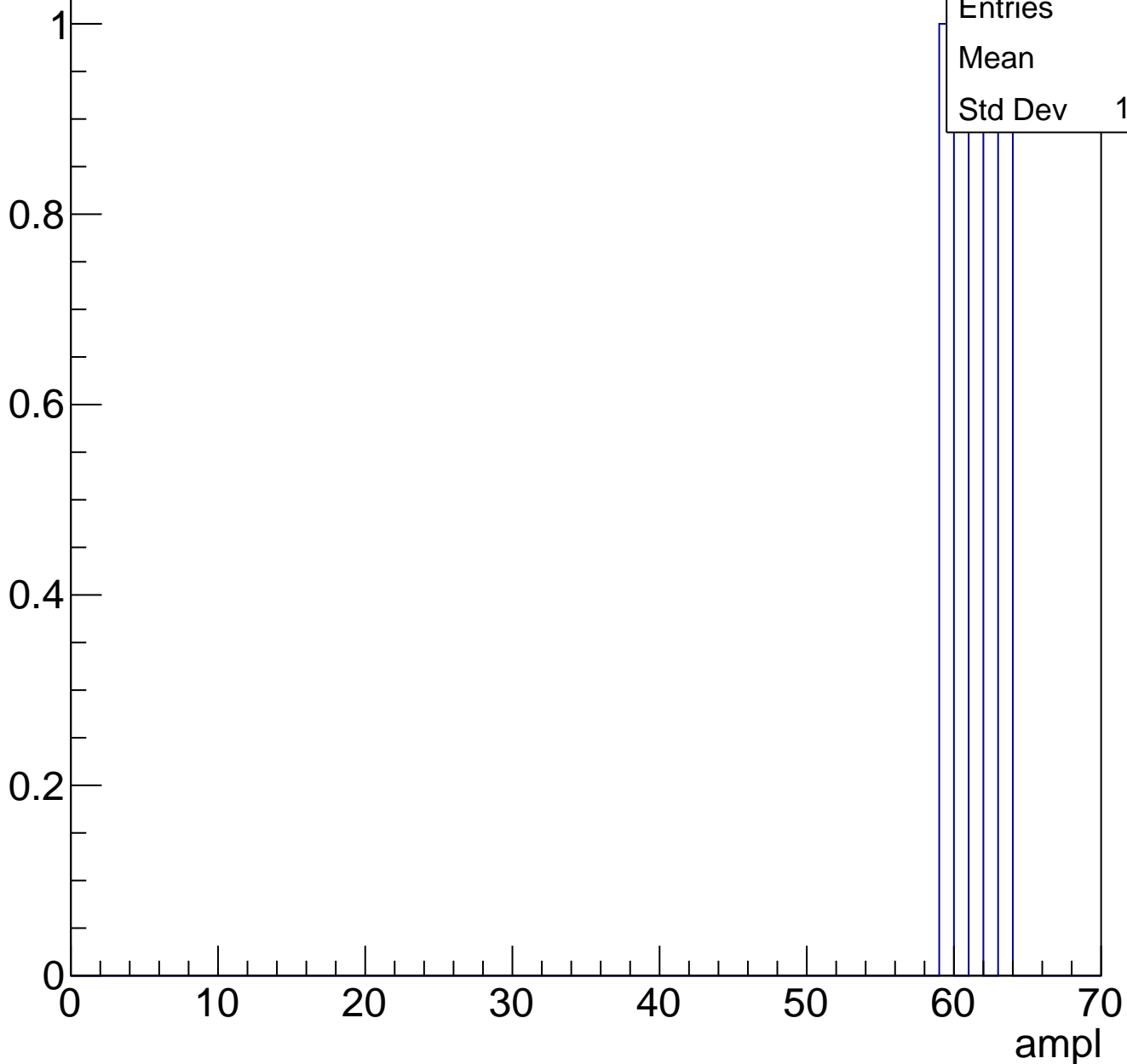
Entries	42
Mean	59.07
Std Dev	9.505



# B1L101S, U8-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch80, adc0

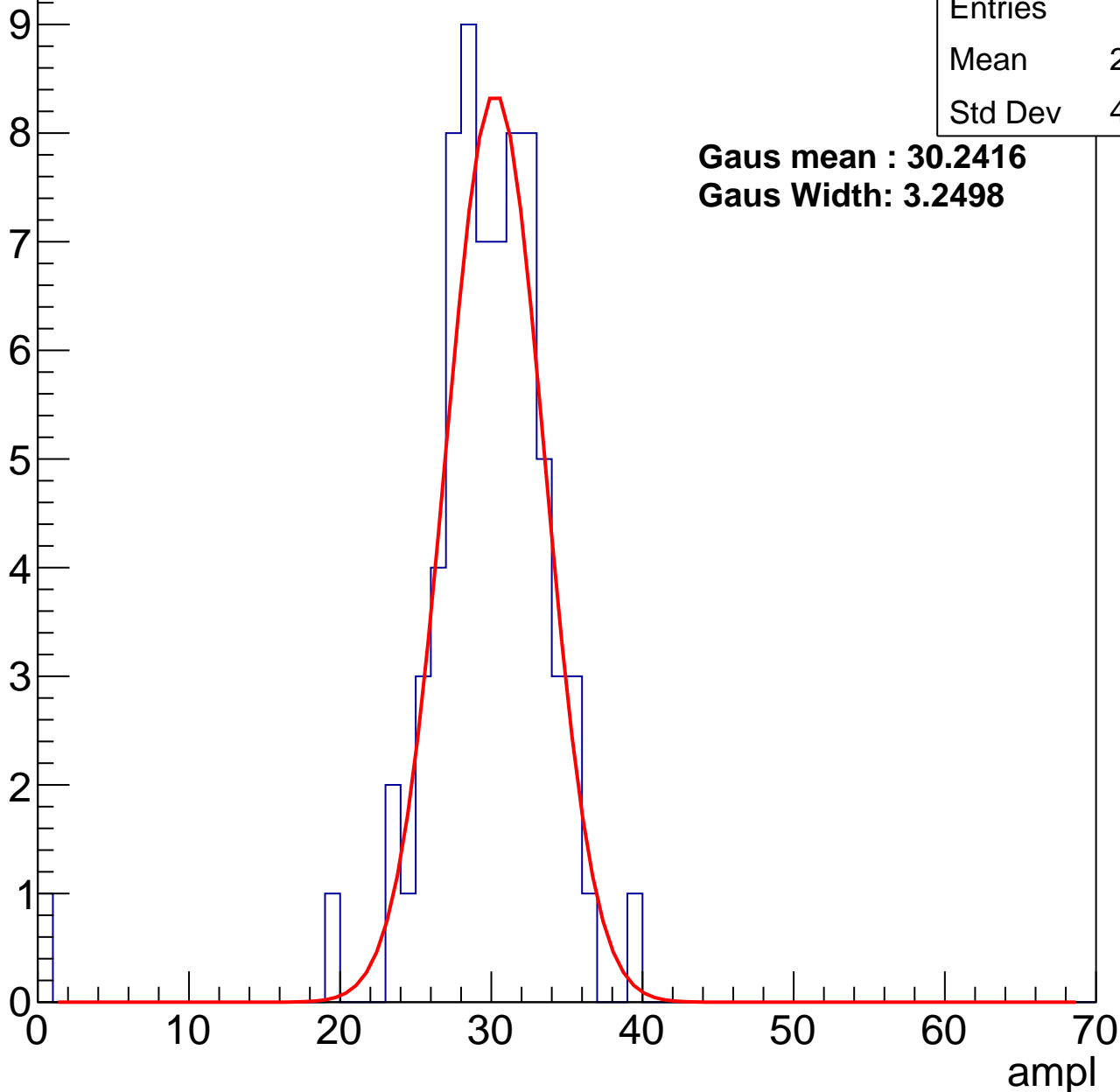
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	29.17
Std Dev	4.836

**Gaus mean : 30.2416**

**Gaus Width: 3.2498**



# B1L101S, U8-ch80, adc1

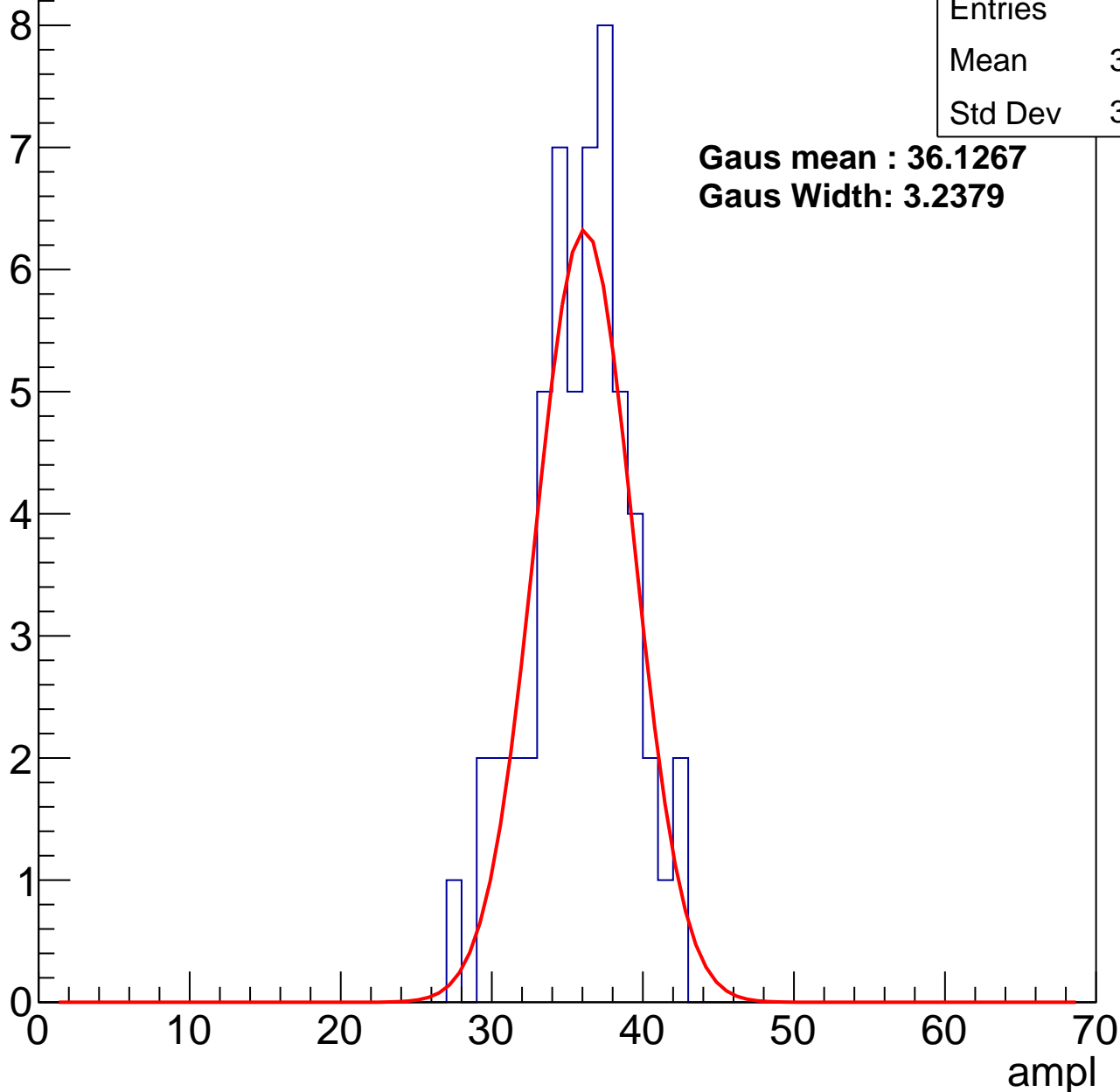
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	35.42
Std Dev	3.262

**Gaus mean : 36.1267**

**Gaus Width: 3.2379**



# B1L101S, U8-ch80, adc2

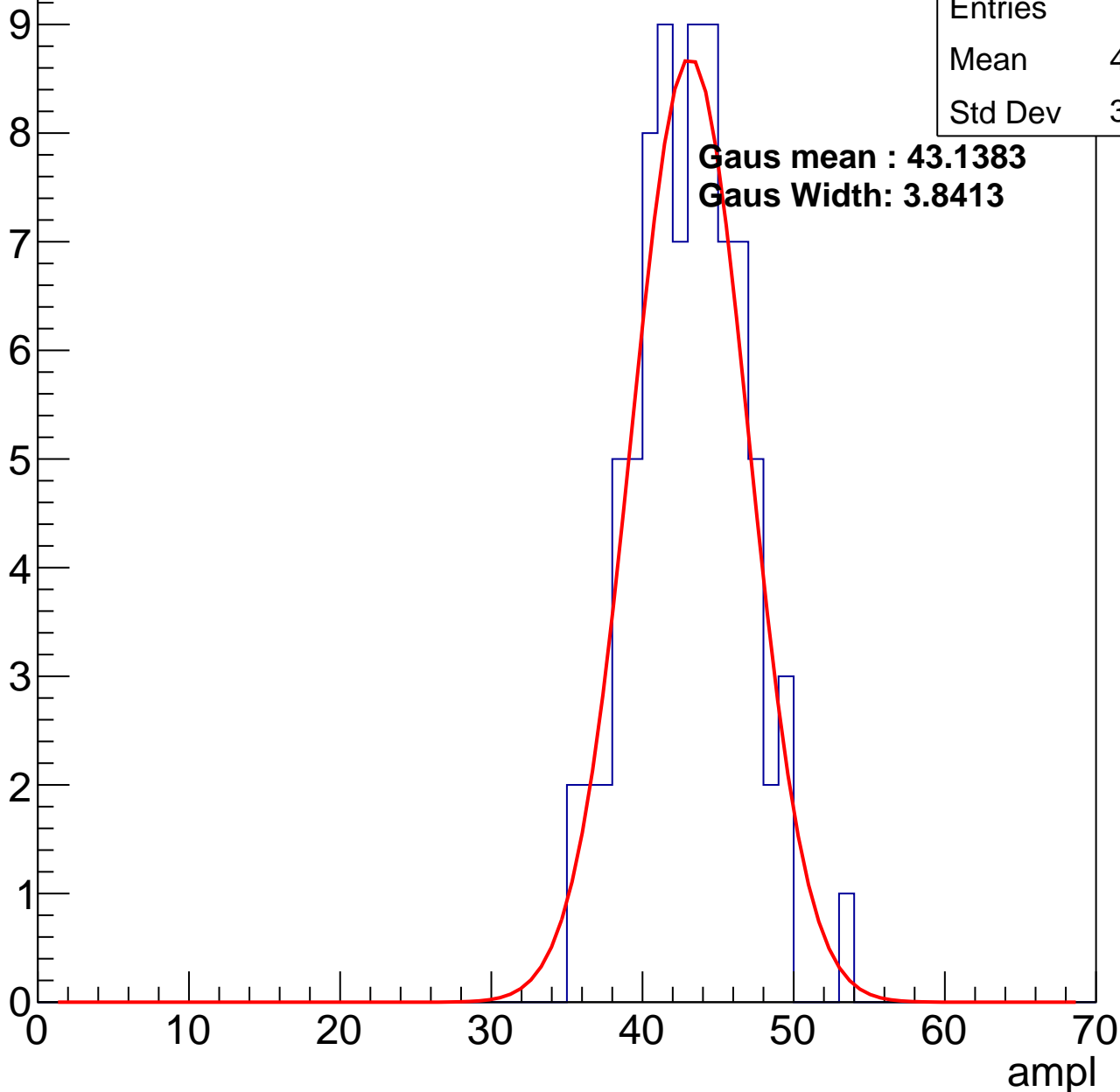
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	83
Mean	42.59
Std Dev	3.543

**Gaus mean : 43.1383**

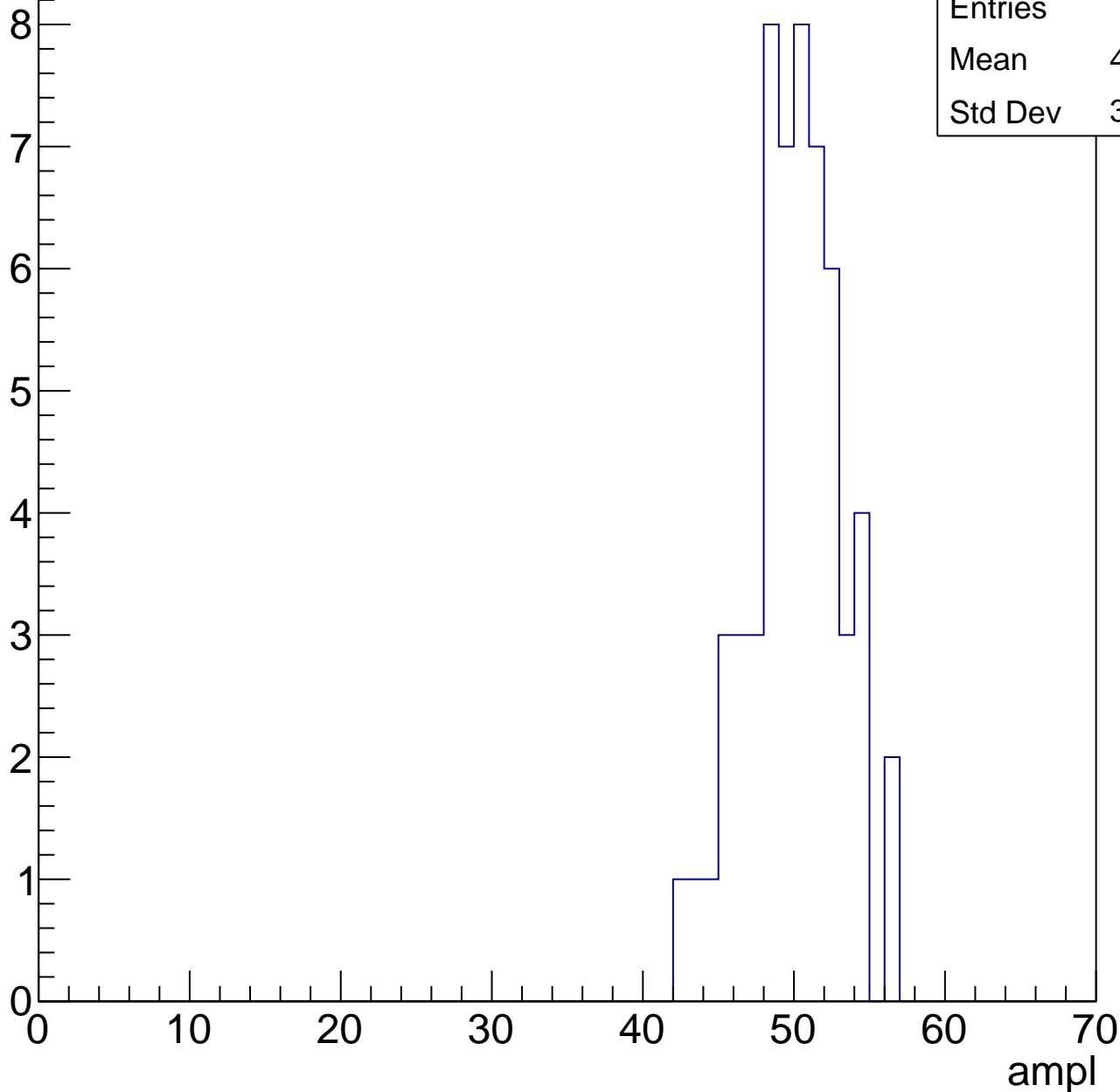
**Gaus Width: 3.8413**



# B1L101S, U8-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

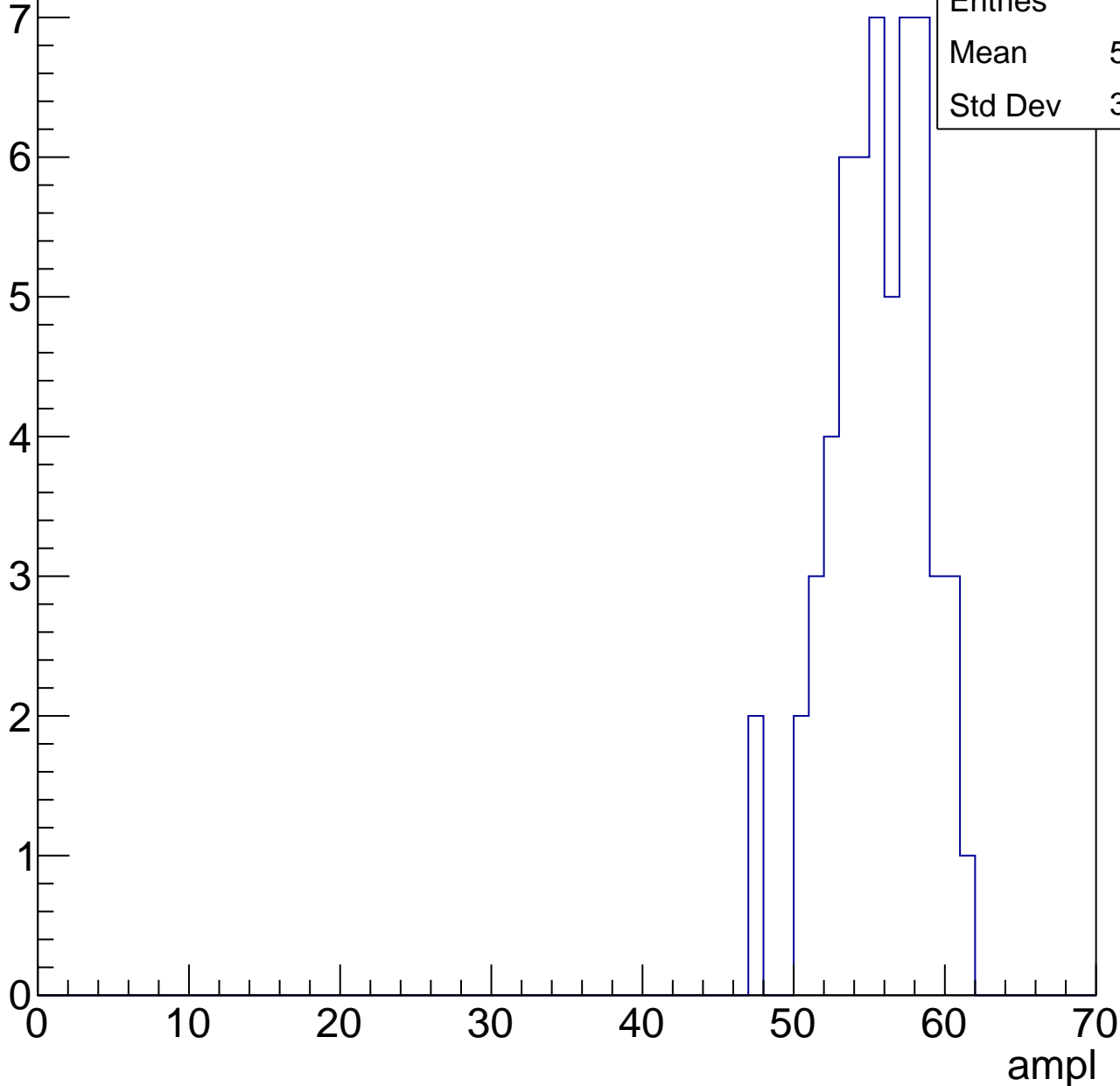


# B1L101S, U8-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	55.09
Std Dev	3.124

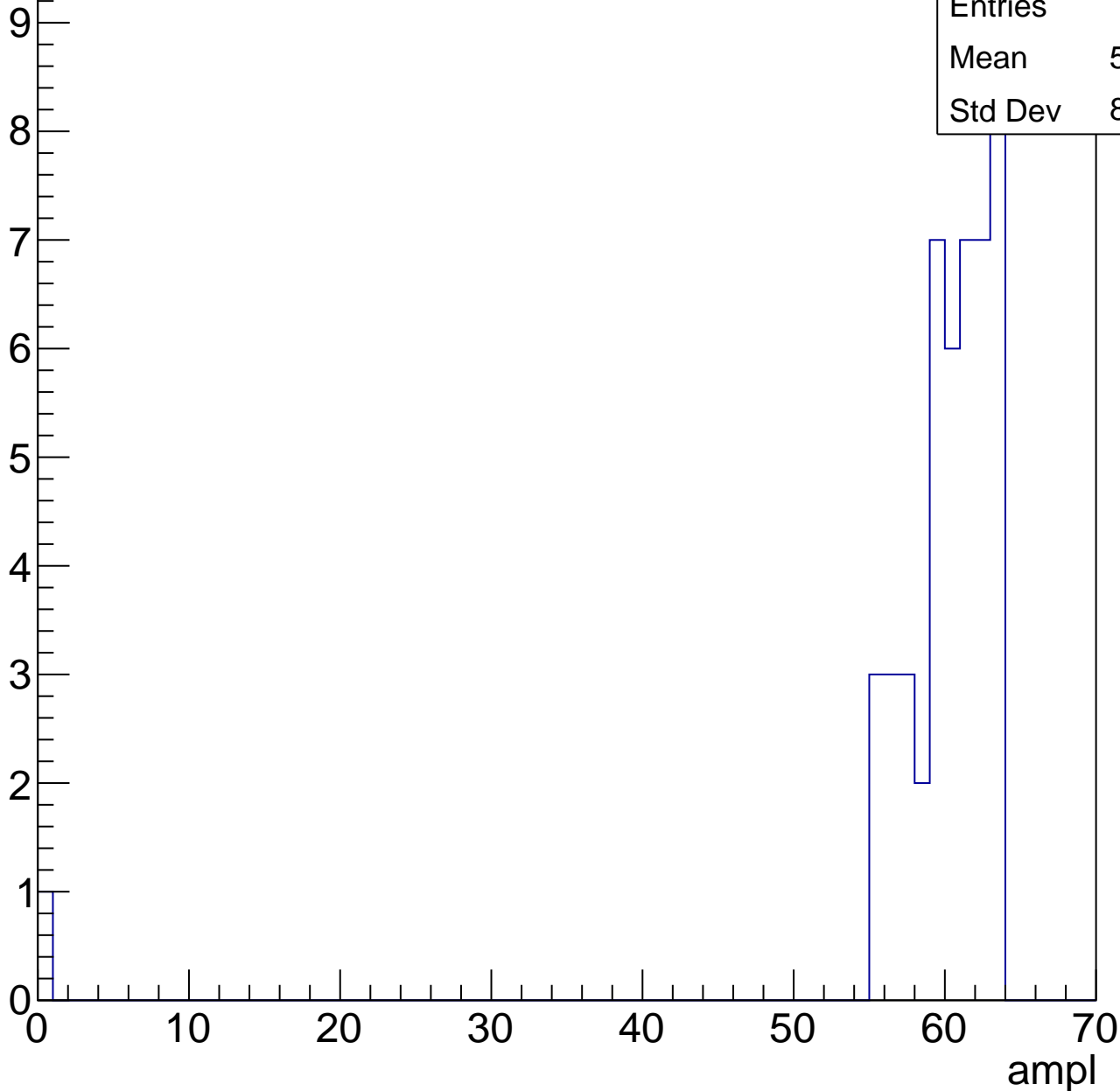


# B1L101S, U8-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

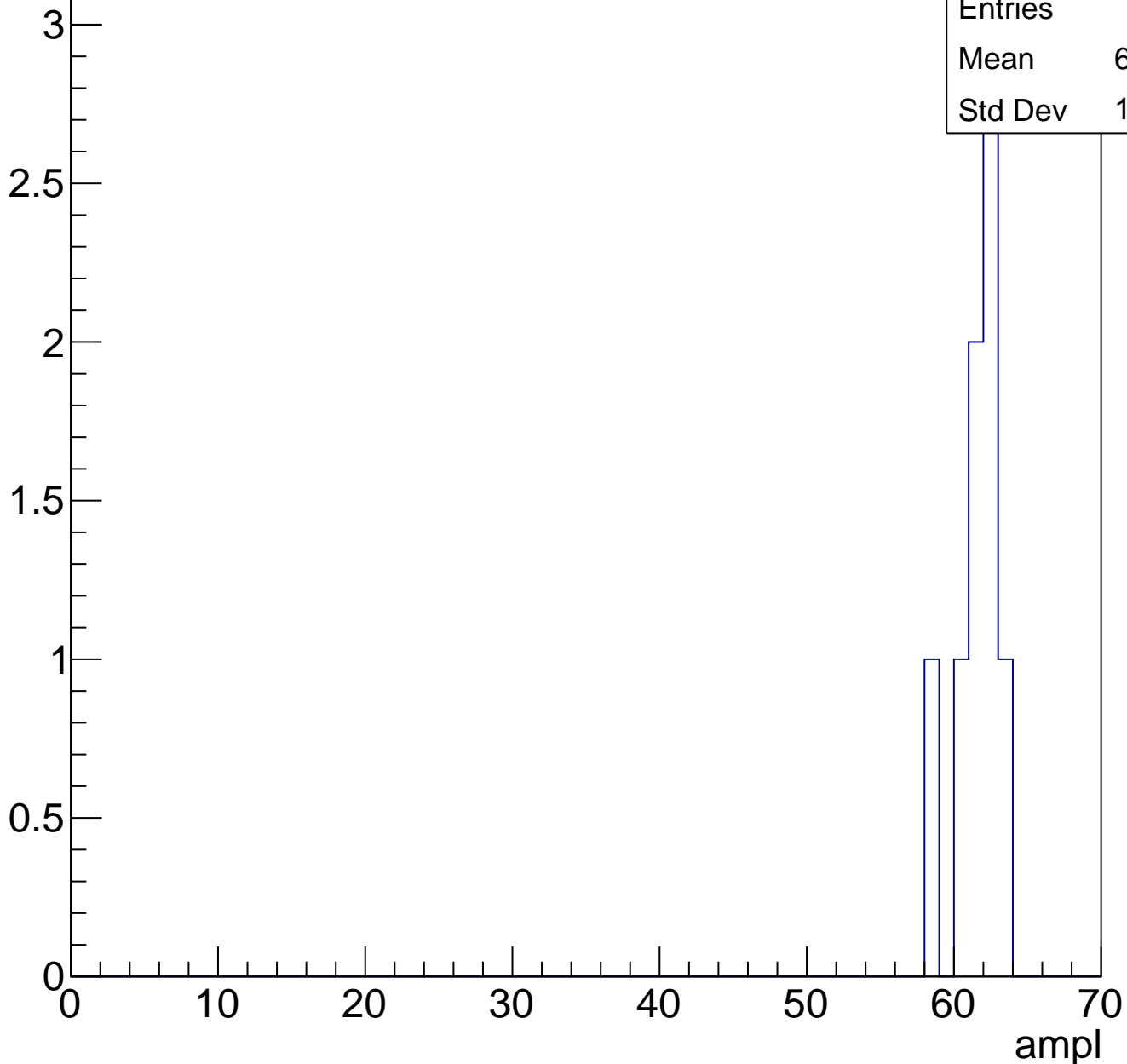
Entries	48
Mean	58.77
Std Dev	8.907



# B1L101S, U8-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U8-ch81, adc0

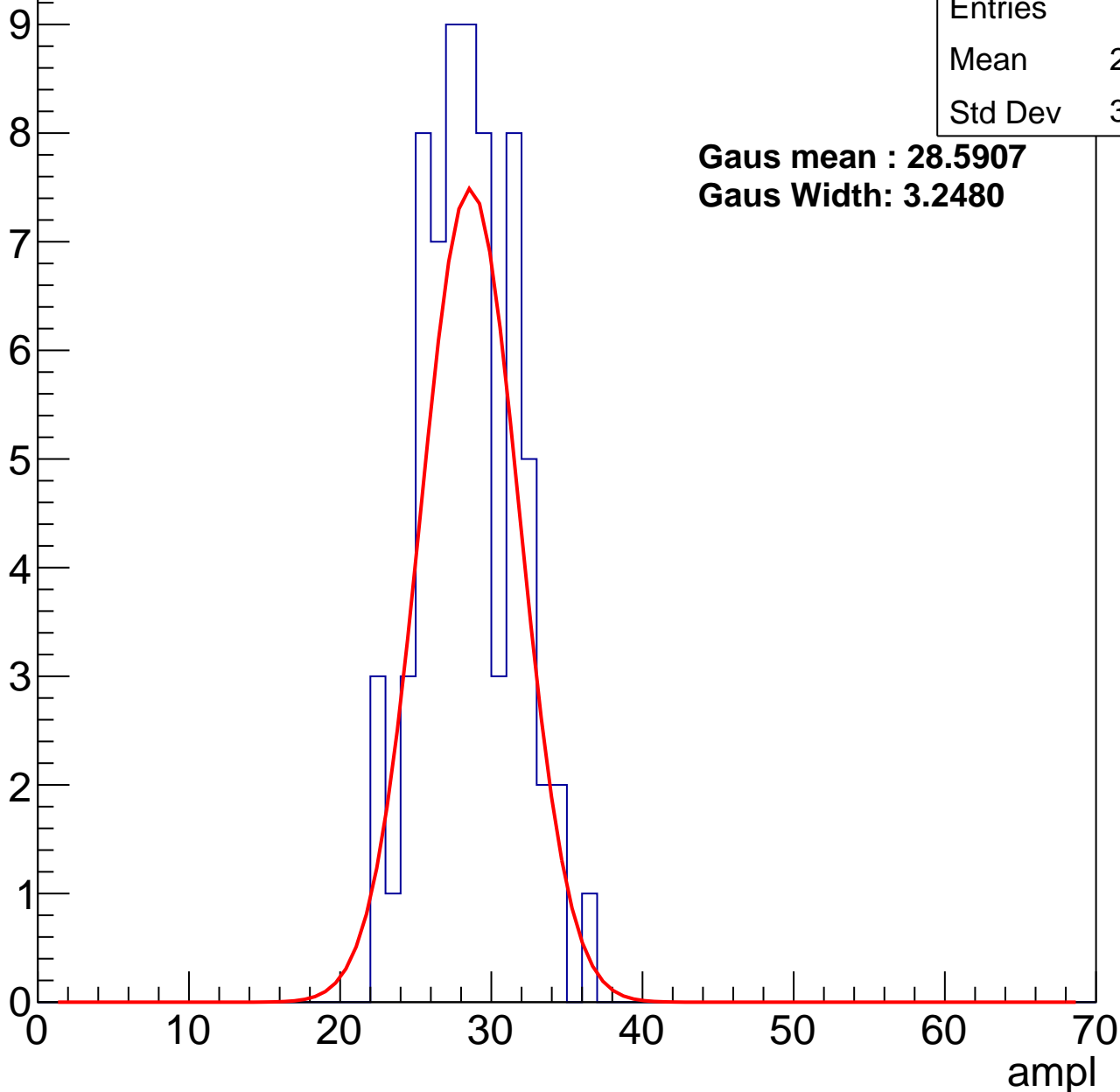
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	28.09
Std Dev	3.063

**Gaus mean : 28.5907**

**Gaus Width: 3.2480**



# B1L101S, U8-ch81, adc1

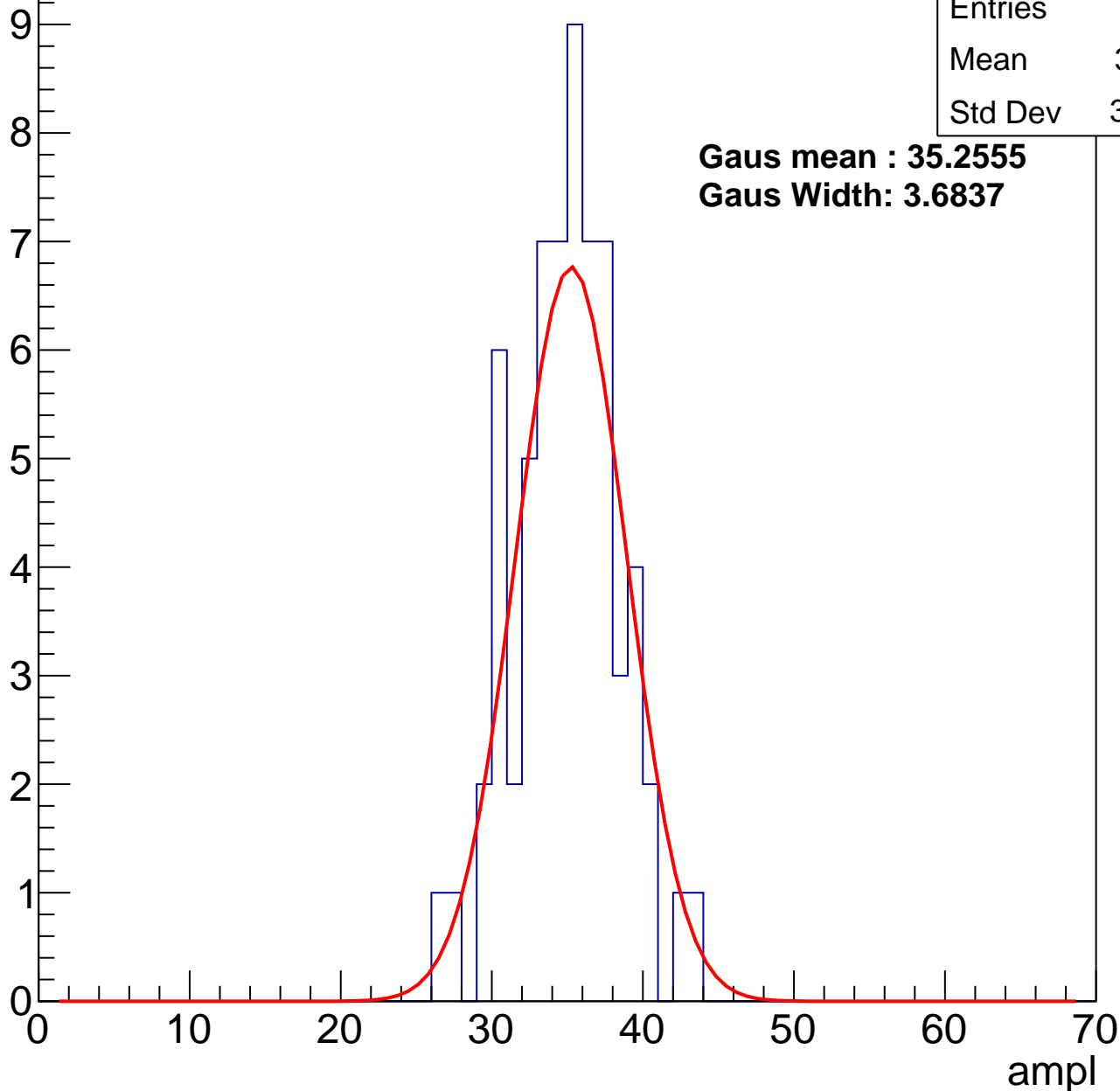
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	34.51
Std Dev	3.402

**Gaus mean : 35.2555**

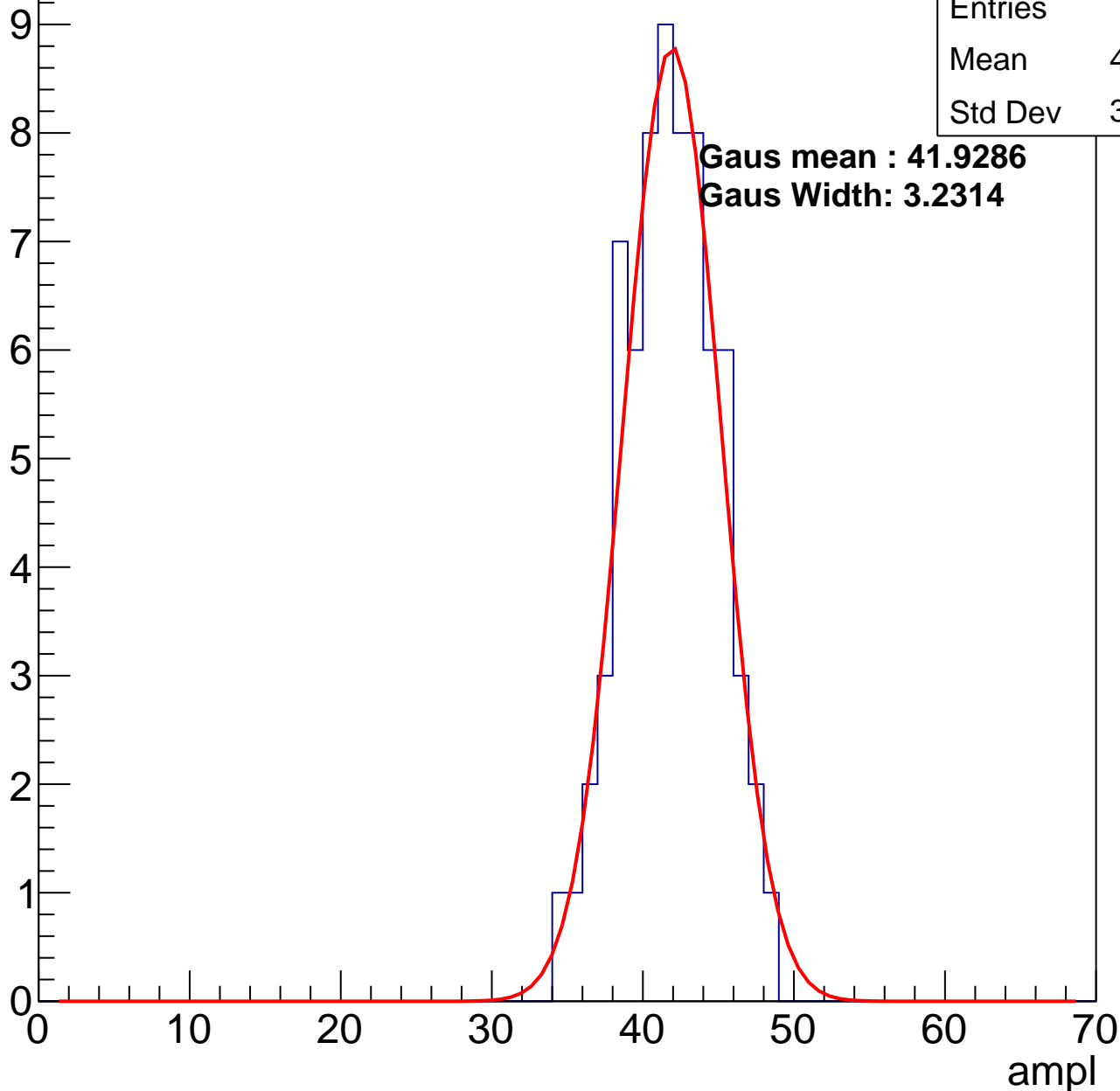
**Gaus Width: 3.6837**



# B1L101S, U8-ch81, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

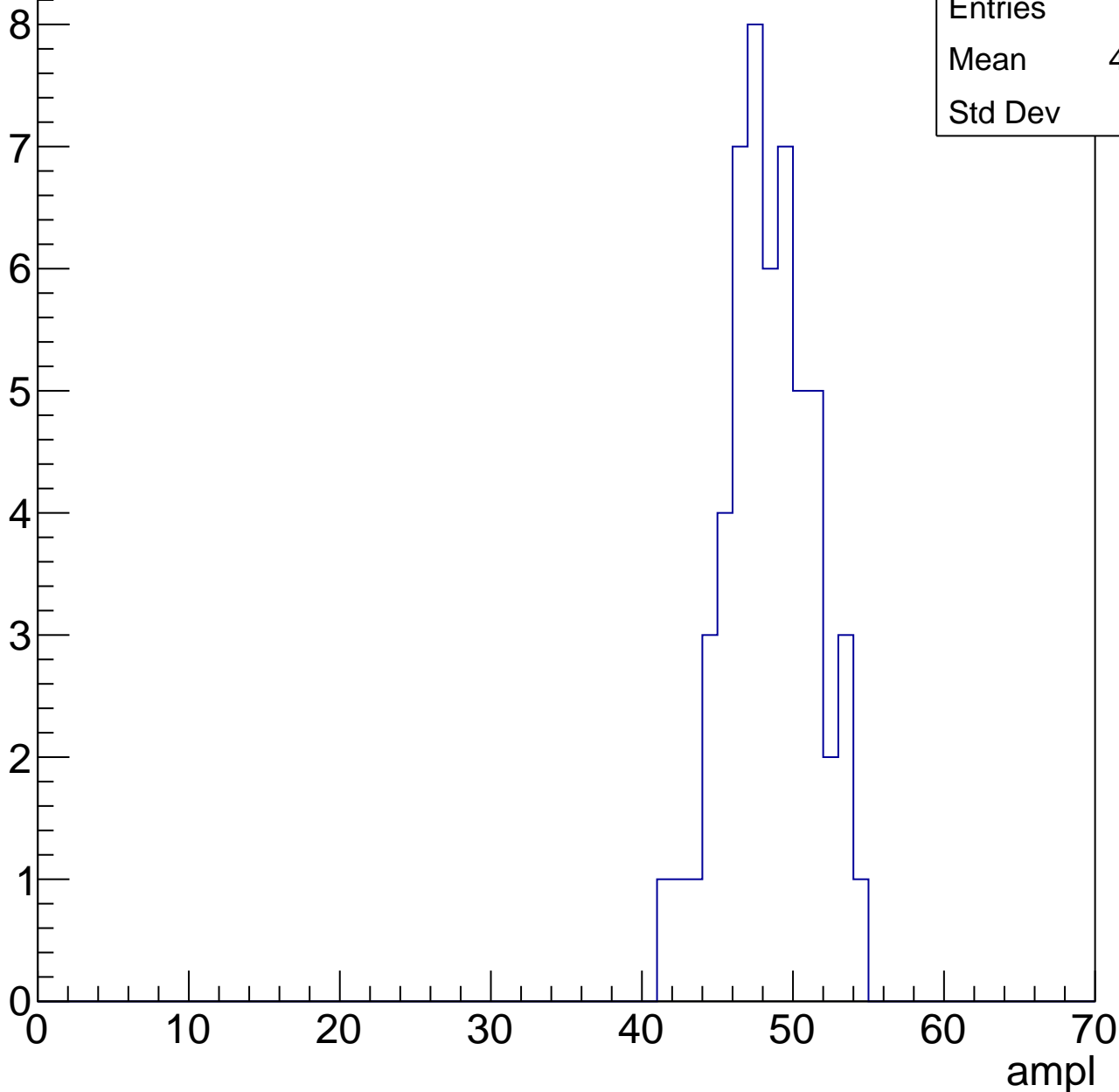


# B1L101S, U8-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

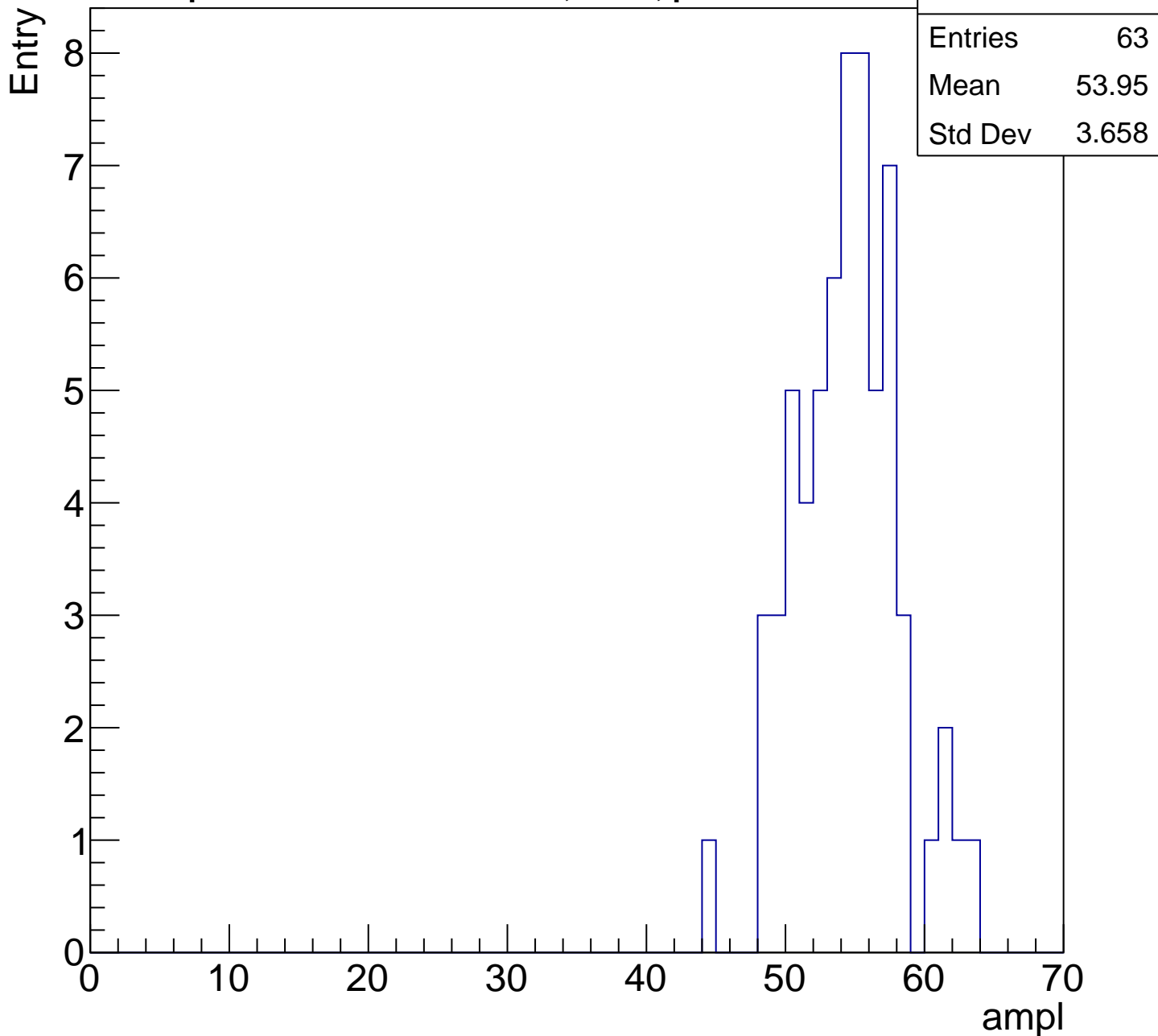
Entry

Entries	54
Mean	47.94
Std Dev	2.87



# B1L101S, U8-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

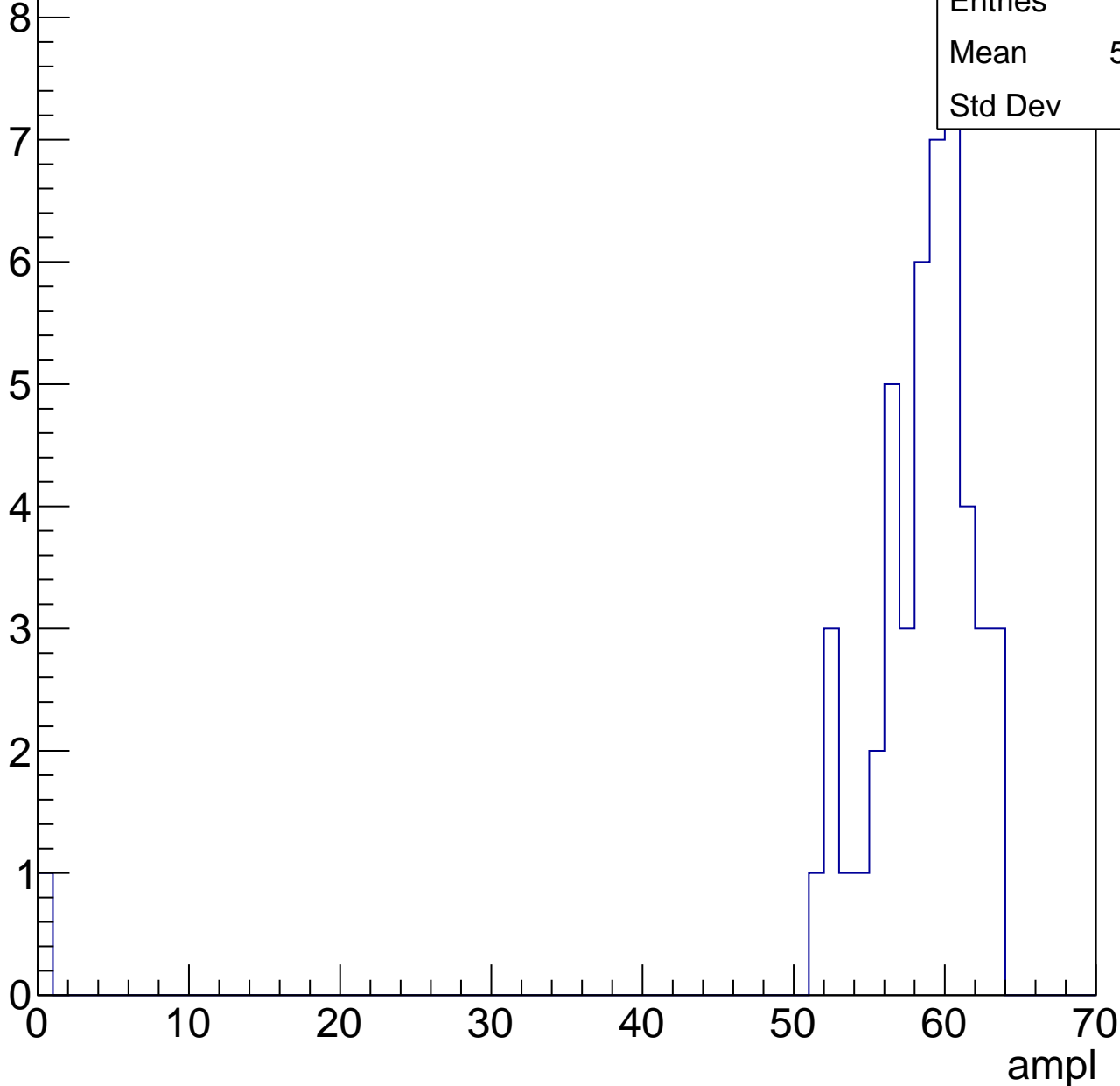


# B1L101S, U8-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	56.98
Std Dev	8.84

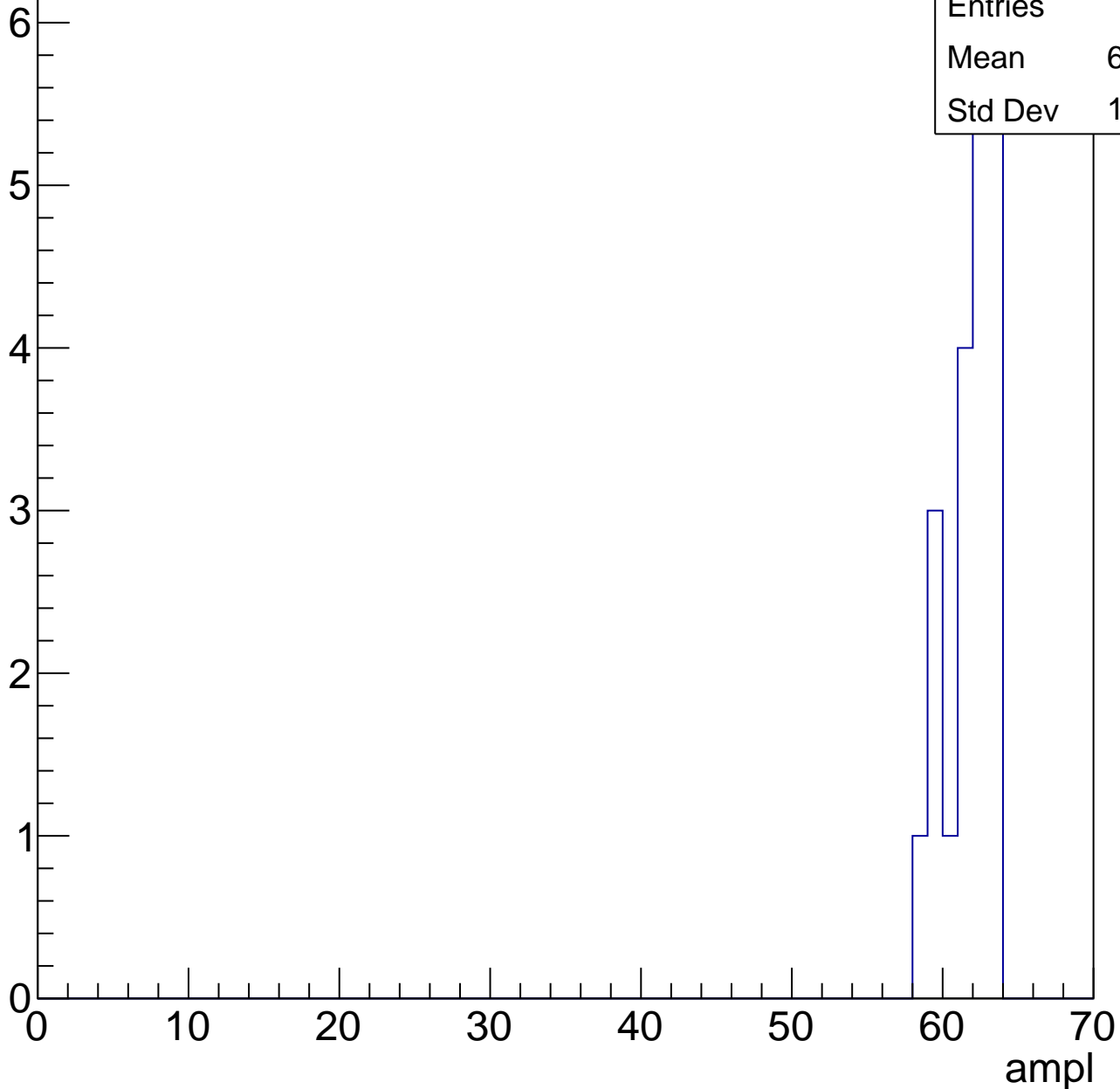


# B1L101S, U8-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	21
Mean	61.38
Std Dev	1.527





# B1L101S, U8-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	10.5
Std Dev	10.5

# B1L101S, U8-ch82, adc0

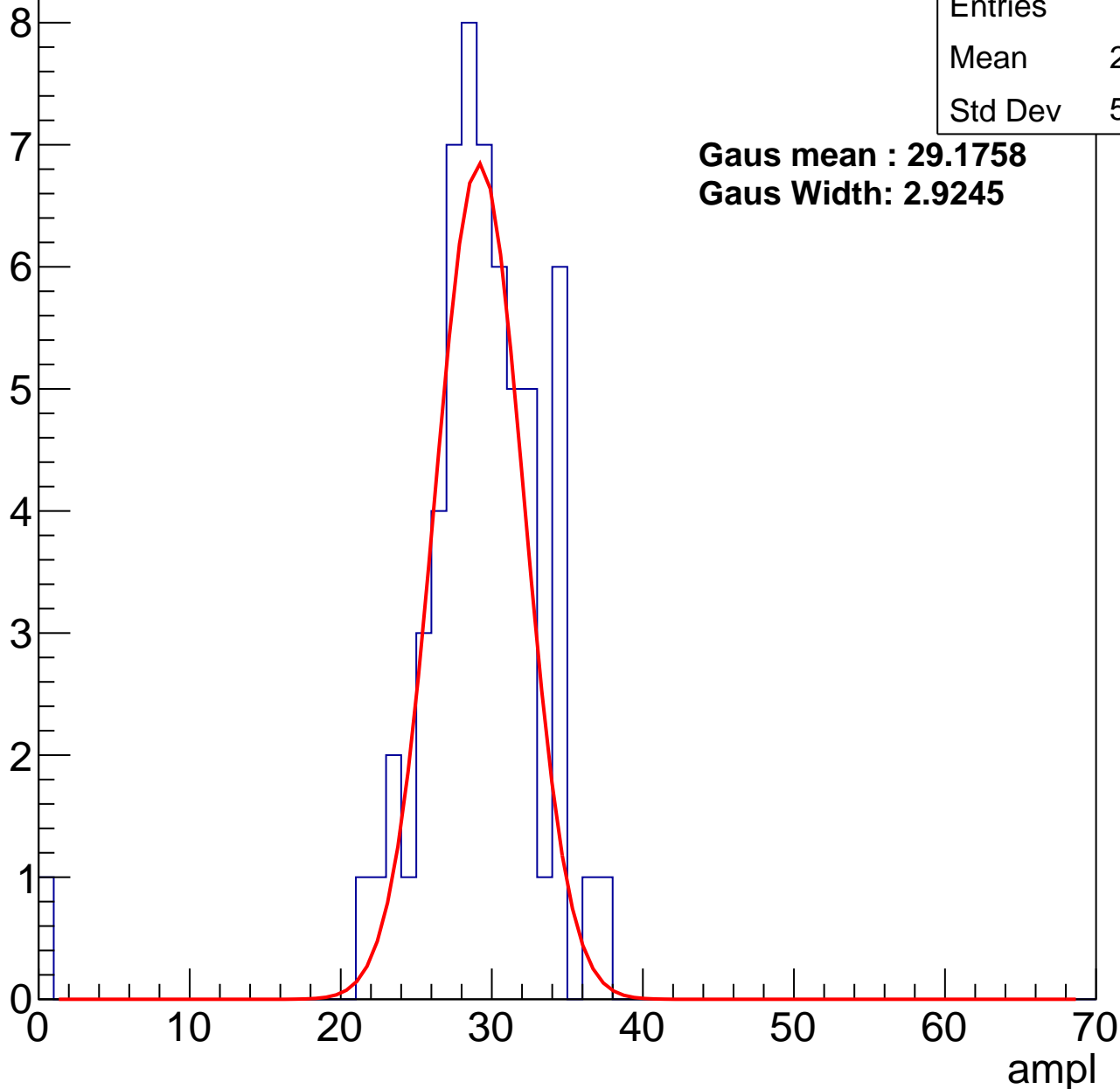
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	28.55
Std Dev	5.015

**Gaus mean : 29.1758**

**Gaus Width: 2.9245**



# B1L101S, U8-ch82, adc1

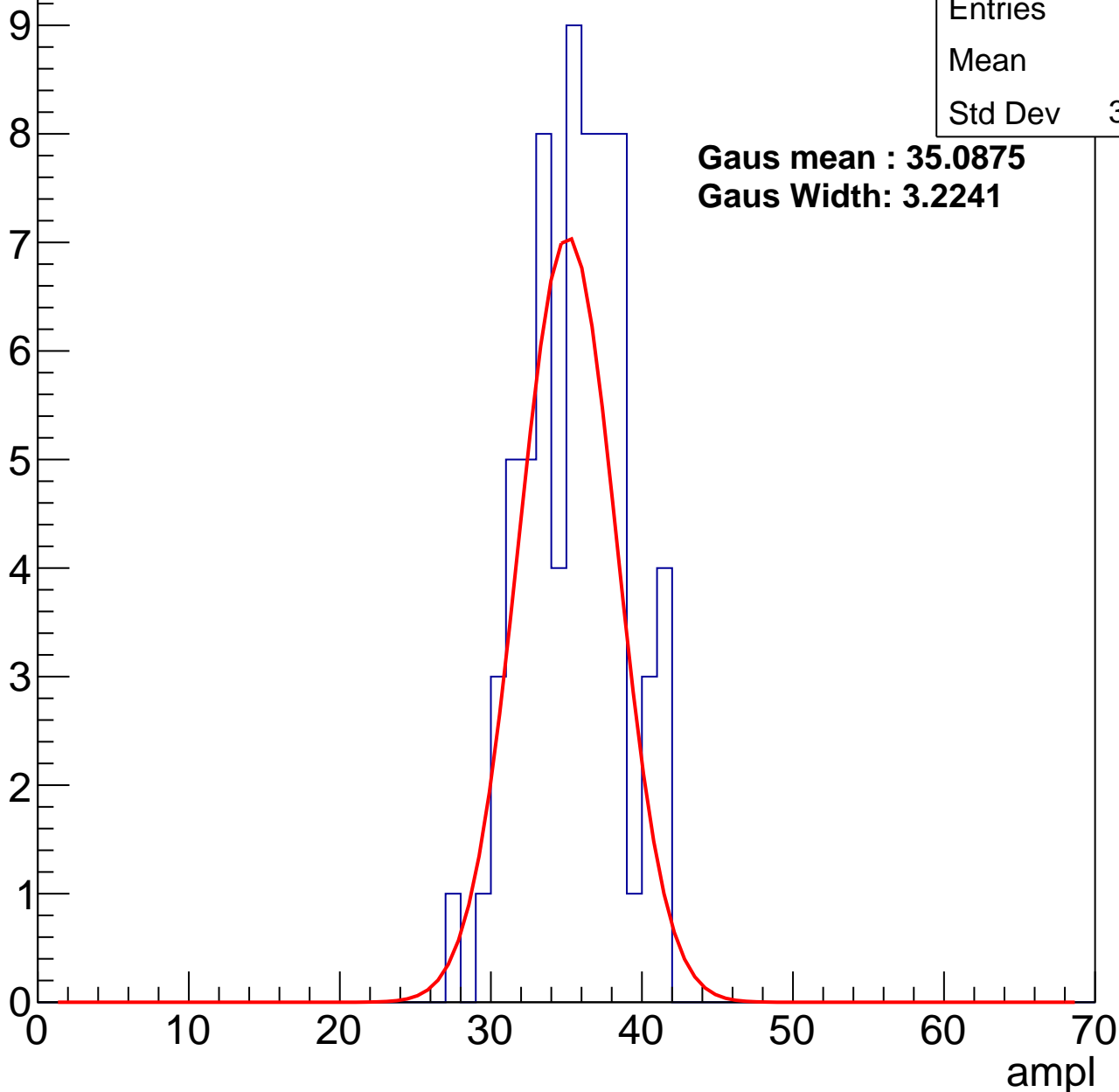
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	35.1
Std Dev	3.168

**Gaus mean : 35.0875**

**Gaus Width: 3.2241**



# B1L101S, U8-ch82, adc2

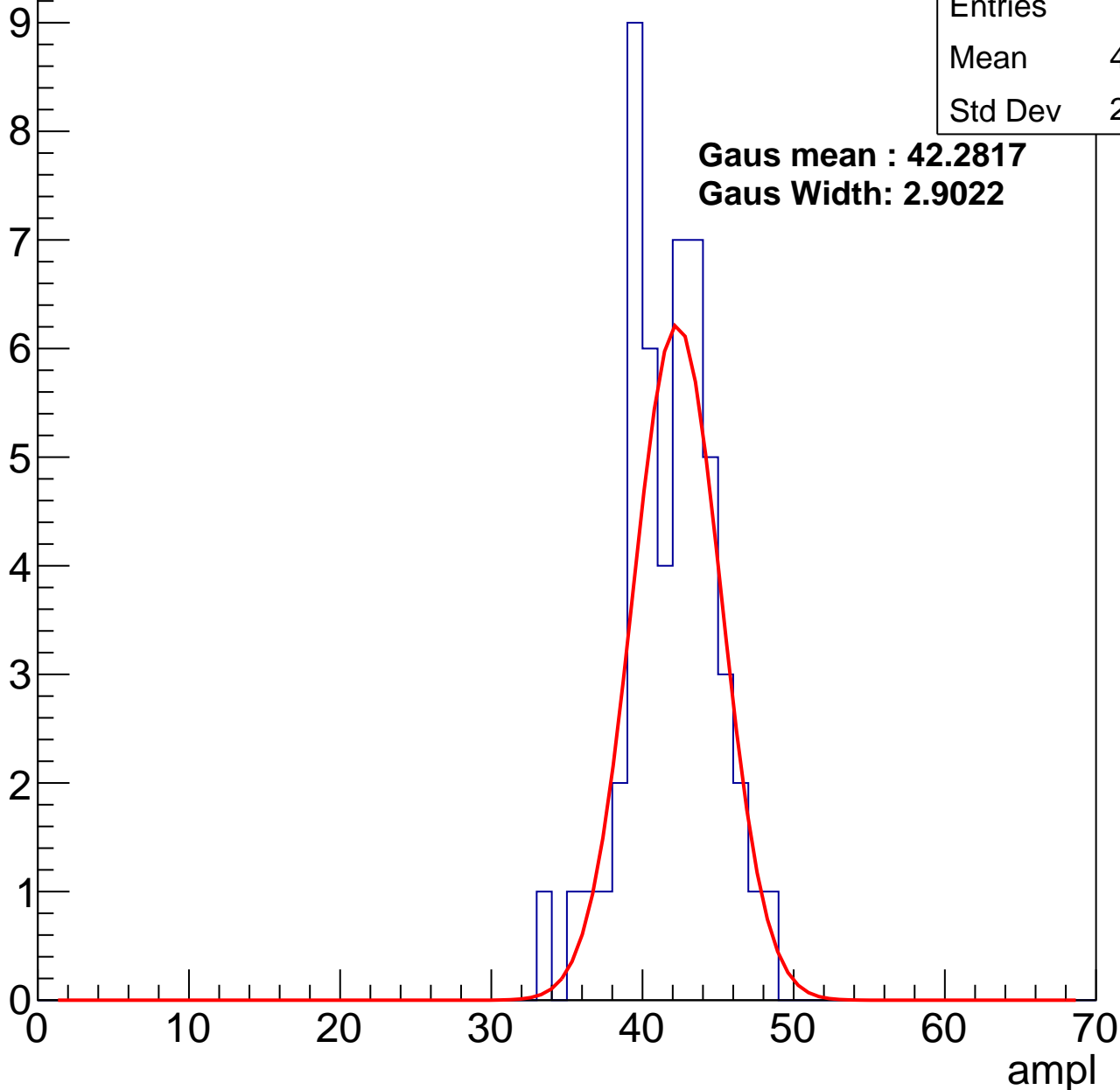
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	41.35
Std Dev	2.996

**Gaus mean : 42.2817**

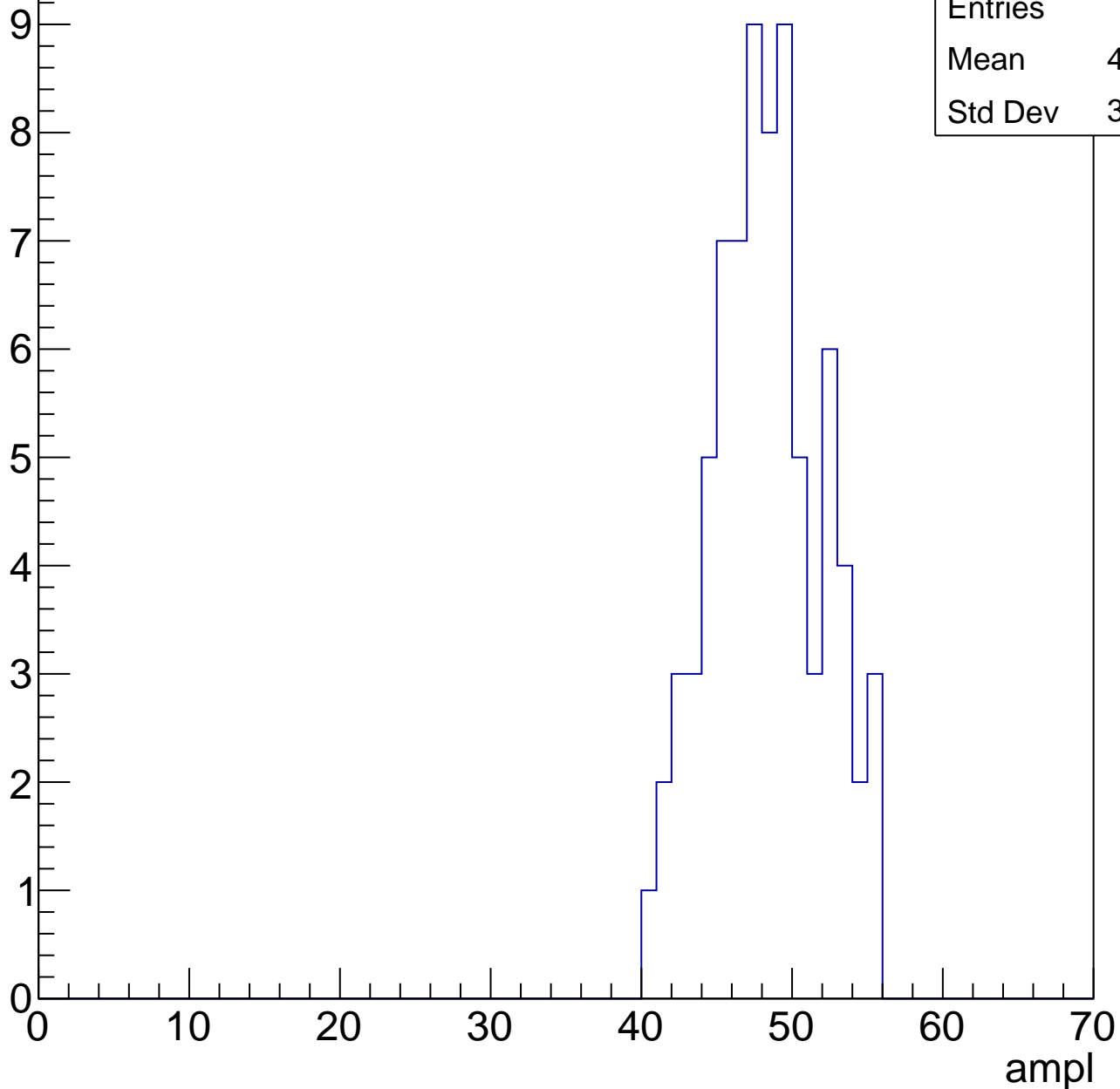
**Gaus Width: 2.9022**



# B1L101S, U8-ch82, adc3

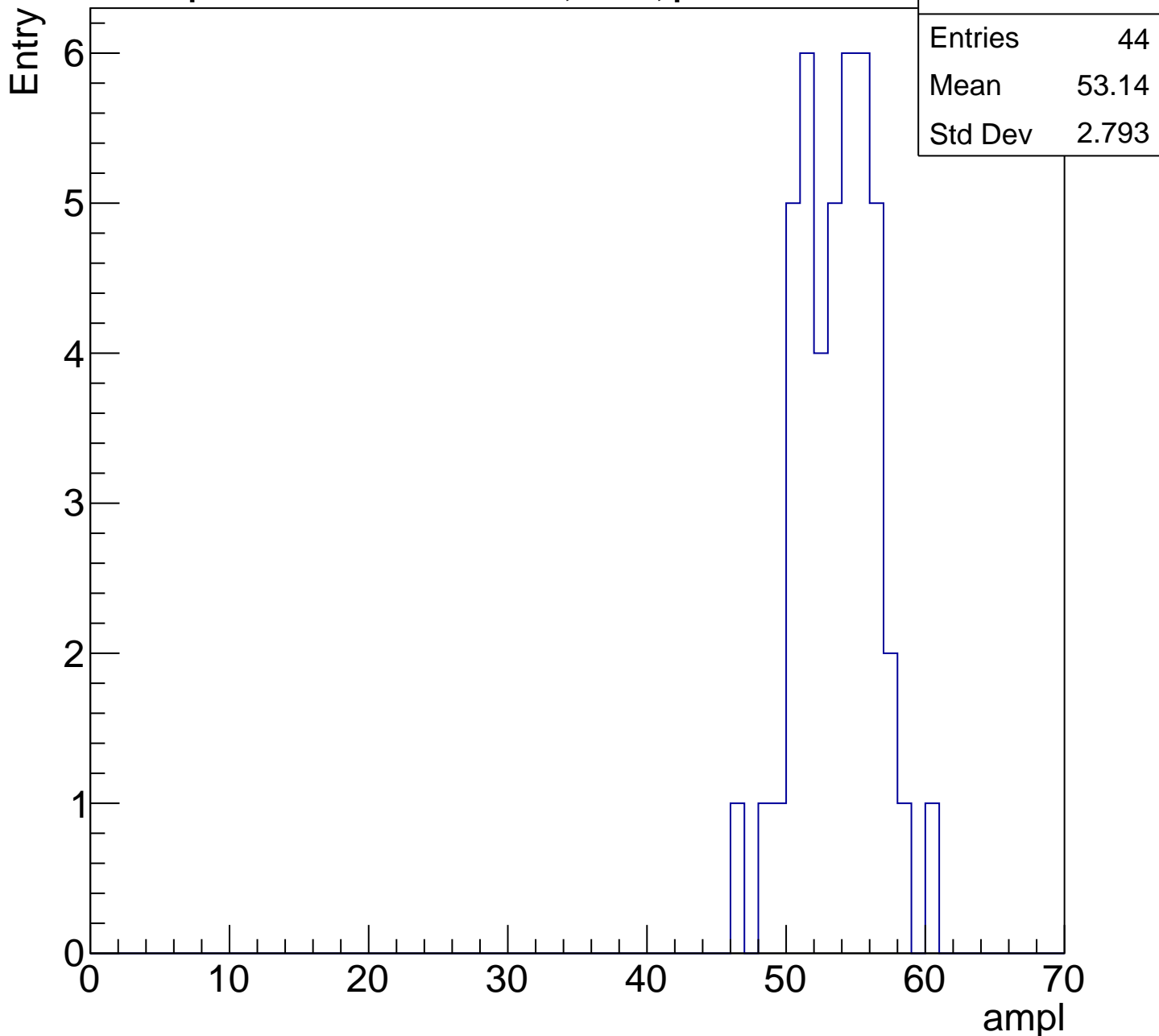
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

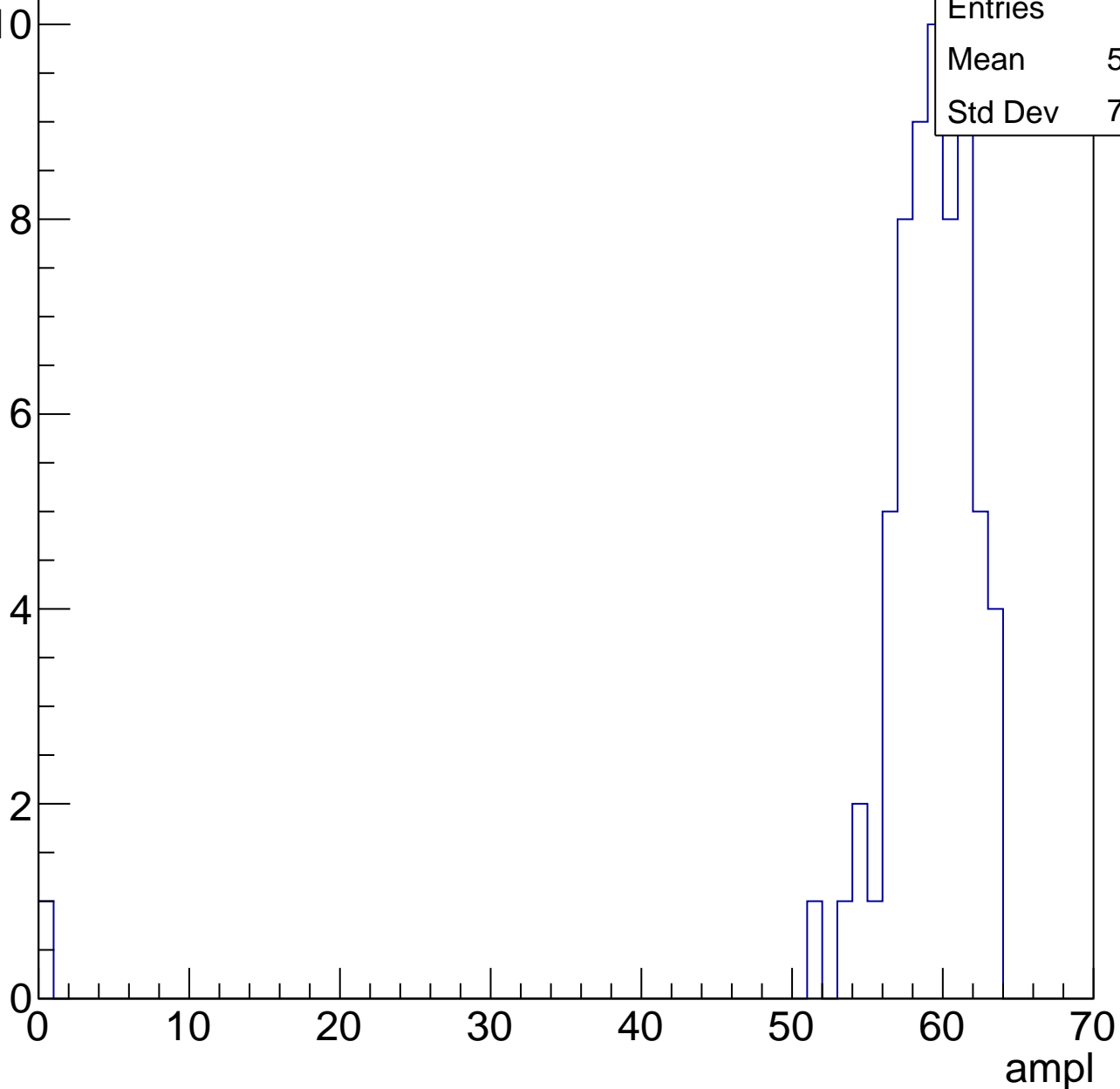


# B1L101S, U8-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

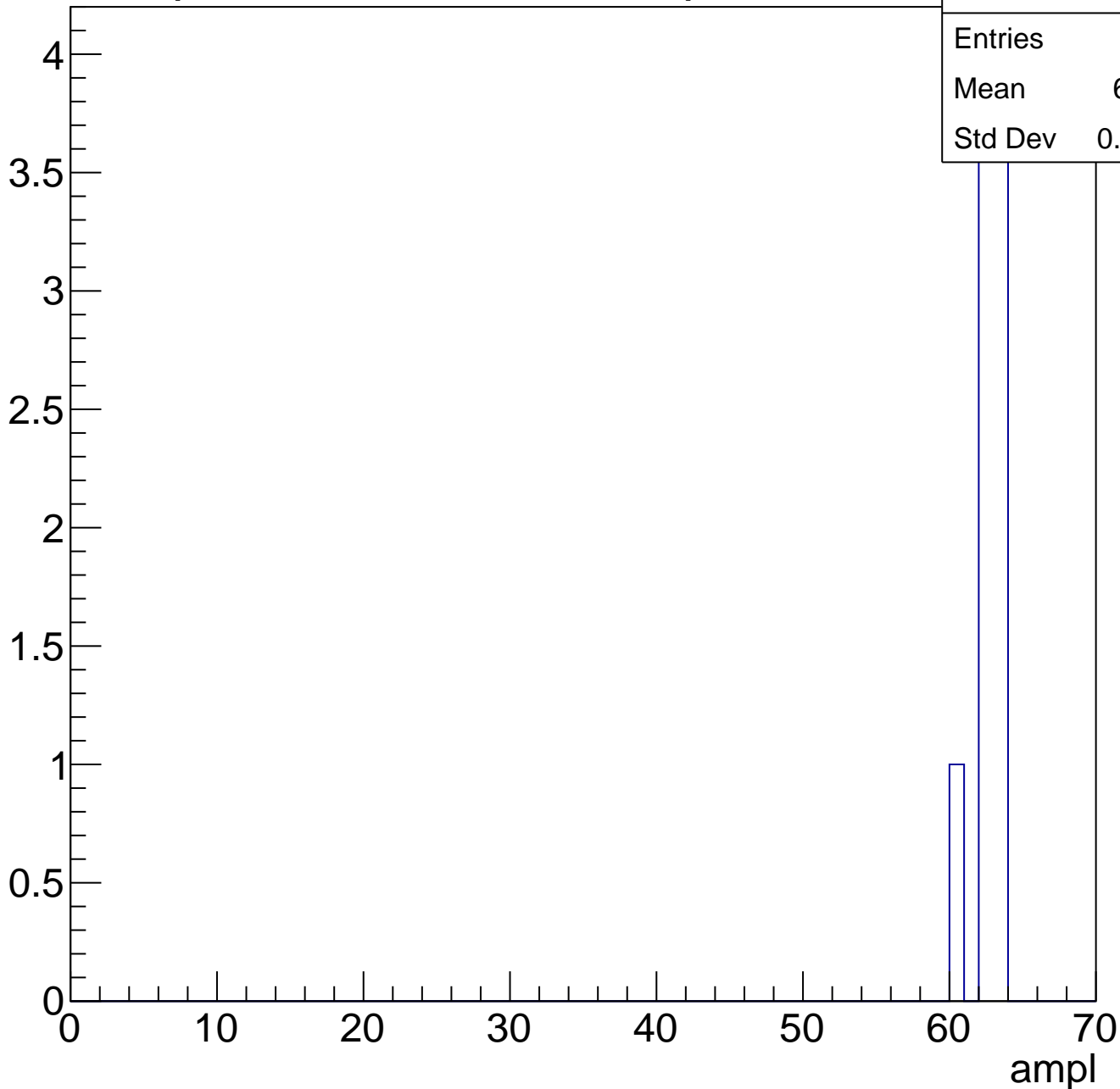
Entries	65
Mean	57.95
Std Dev	7.665



# B1L101S, U8-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

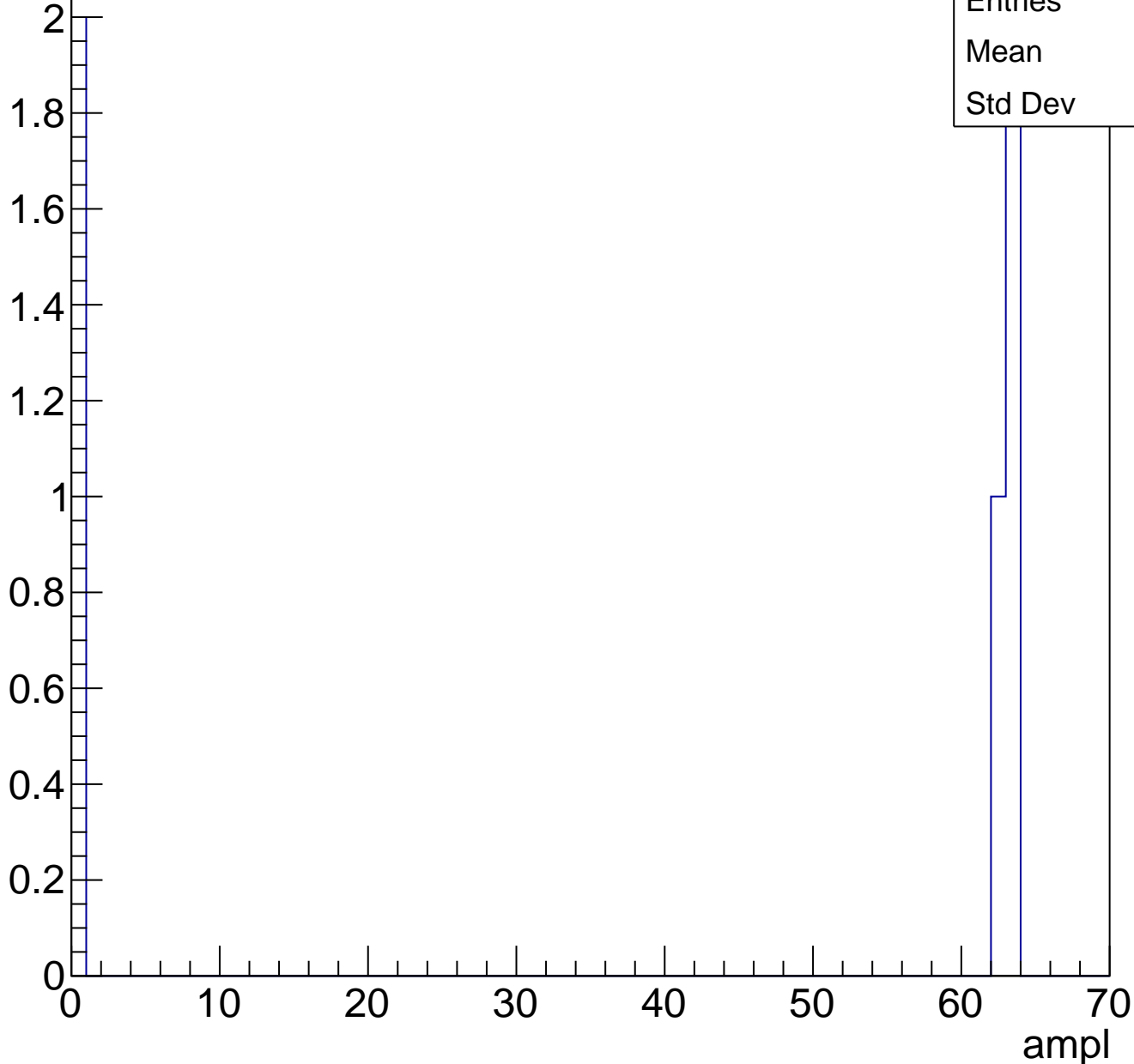




# B1L101S, U8-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch83, adc0

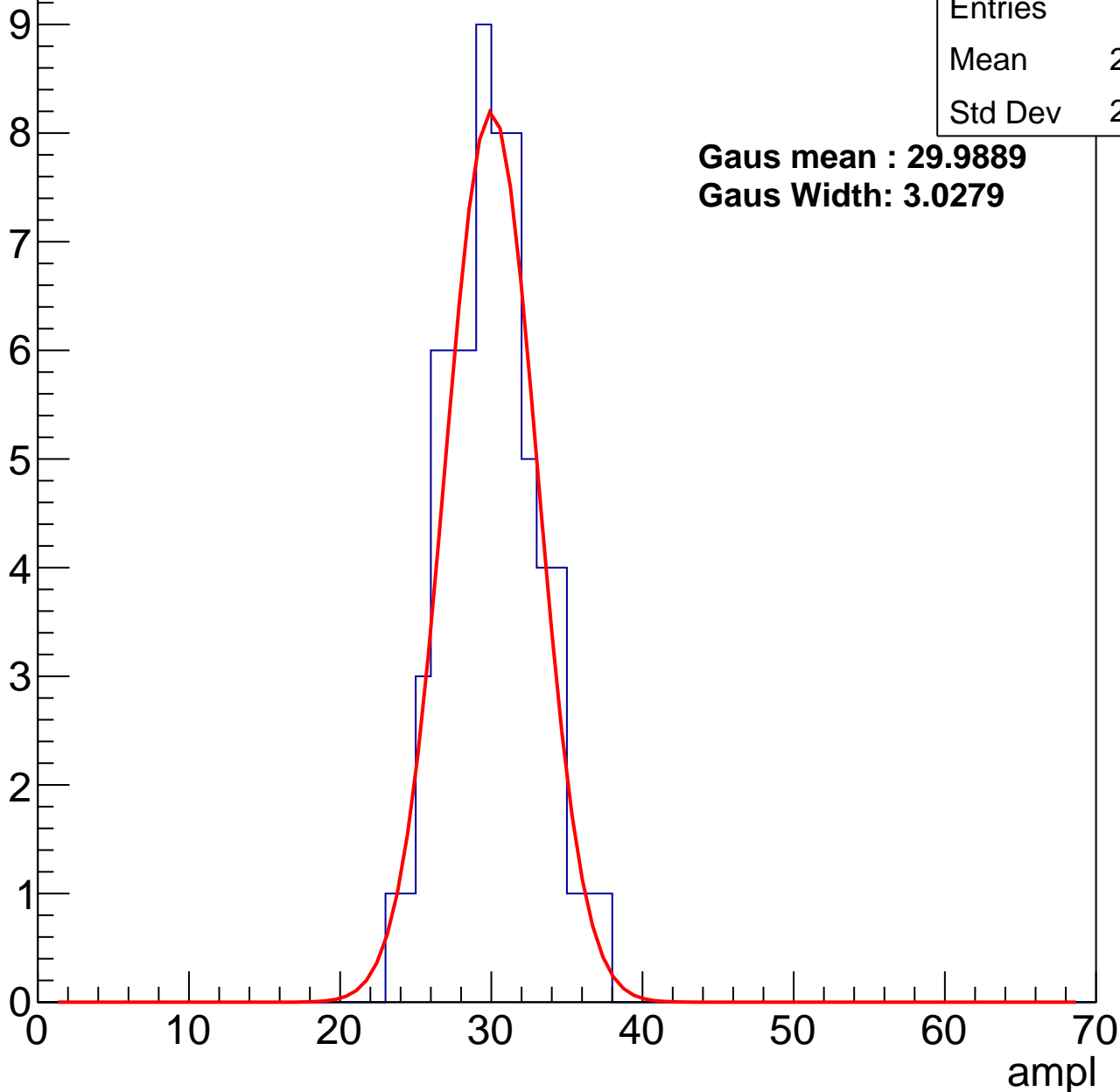
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	29.58
Std Dev	2.983

**Gaus mean : 29.9889**

**Gaus Width: 3.0279**



# B1L101S, U8-ch83, adc1

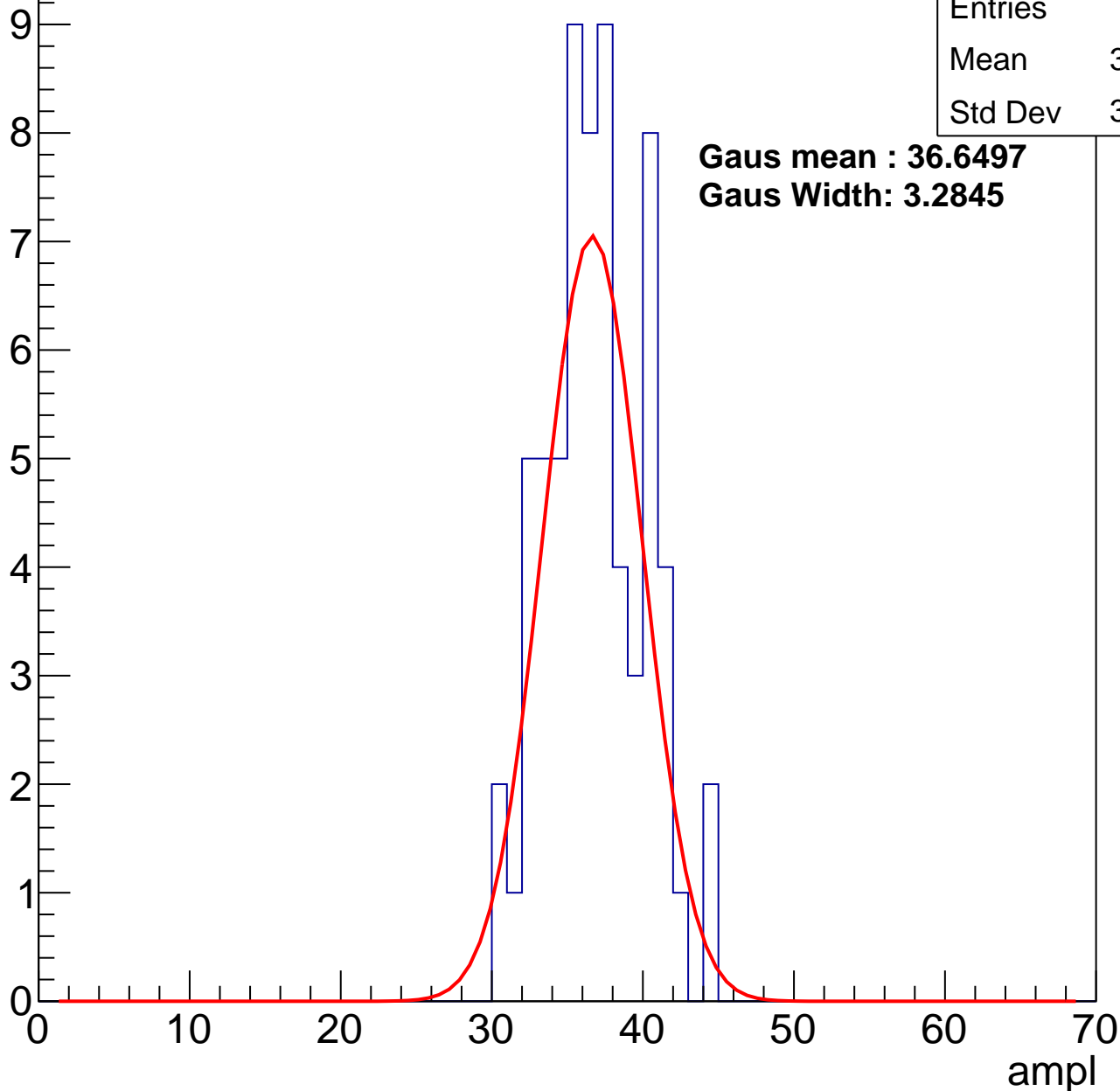
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	36.44
Std Dev	3.215

**Gaus mean : 36.6497**

**Gaus Width: 3.2845**



# B1L101S, U8-ch83, adc2

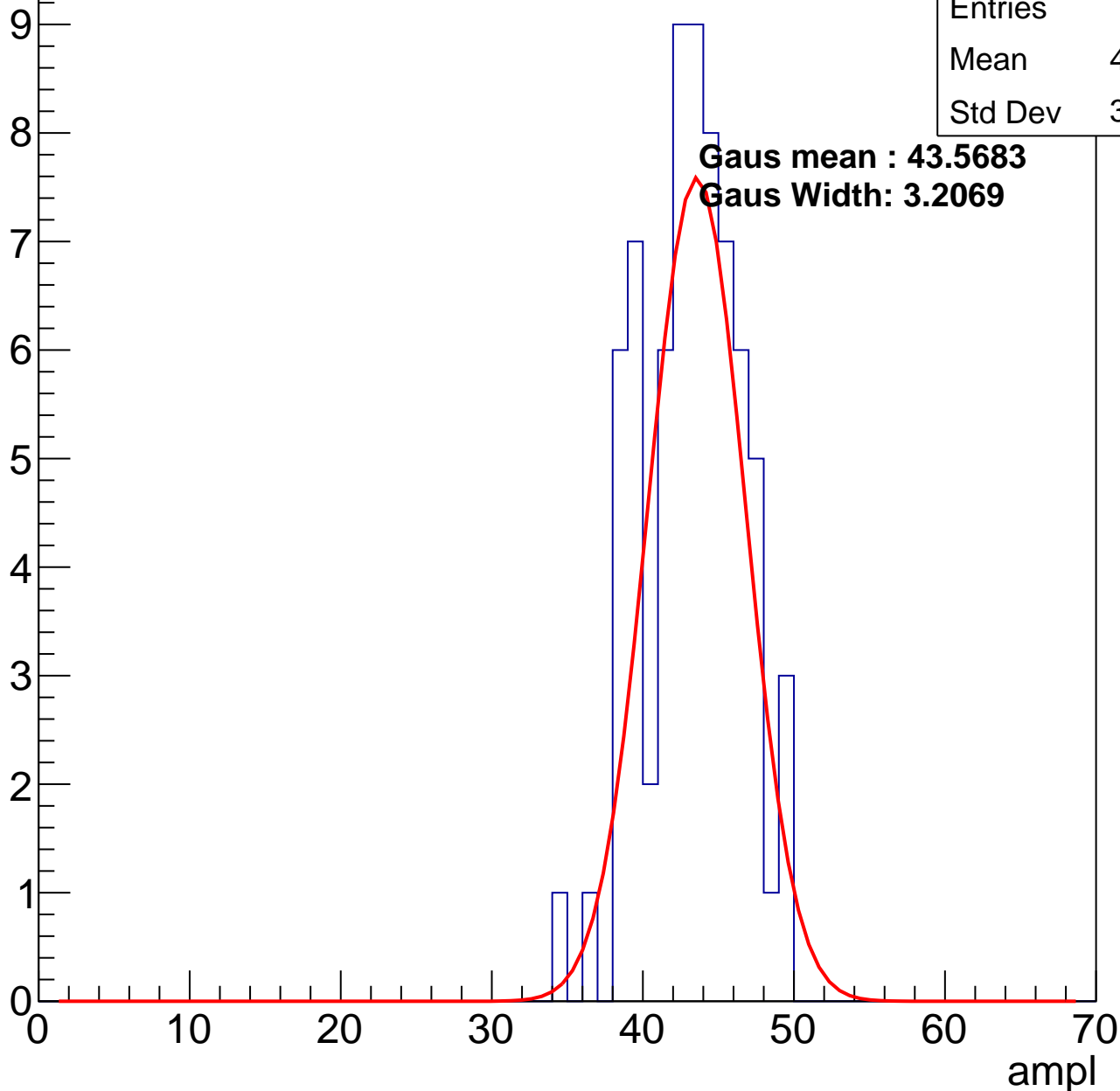
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	42.75
Std Dev	3.232

**Gaus mean : 43.5683**

**Gaus Width: 3.2069**

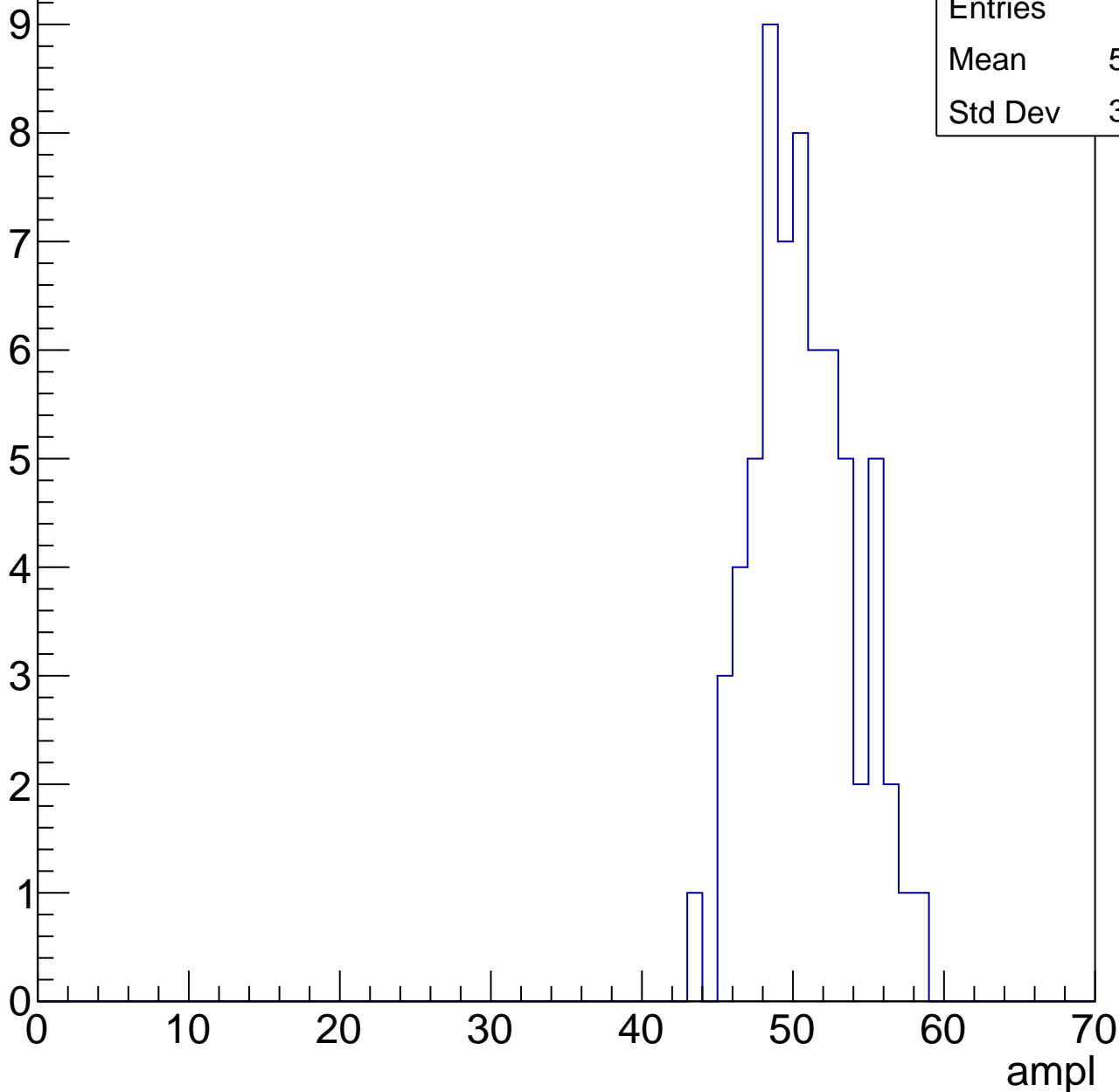


# B1L101S, U8-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	50.23
Std Dev	3.257

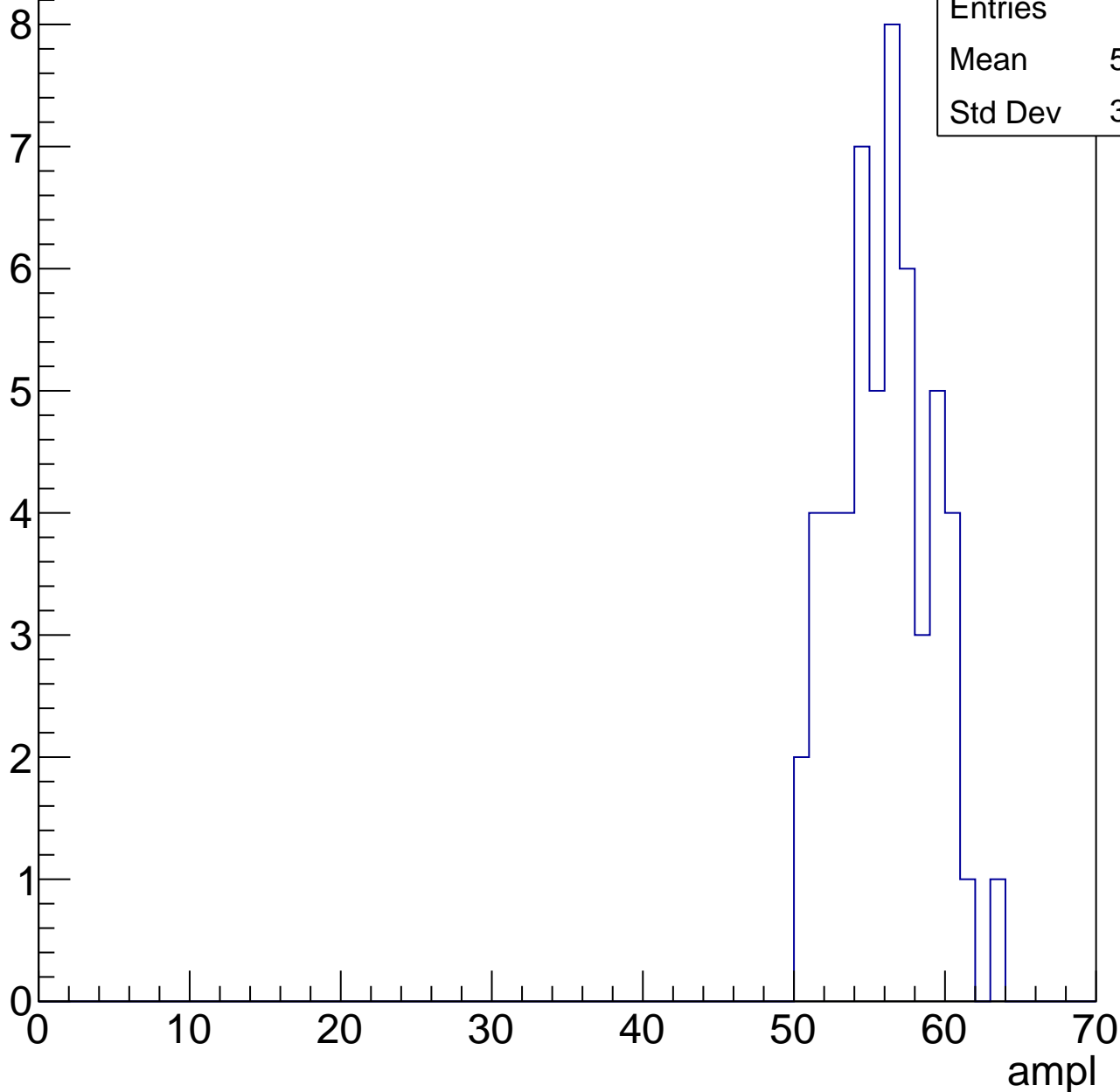


# B1L101S, U8-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	55.56
Std Dev	3.029

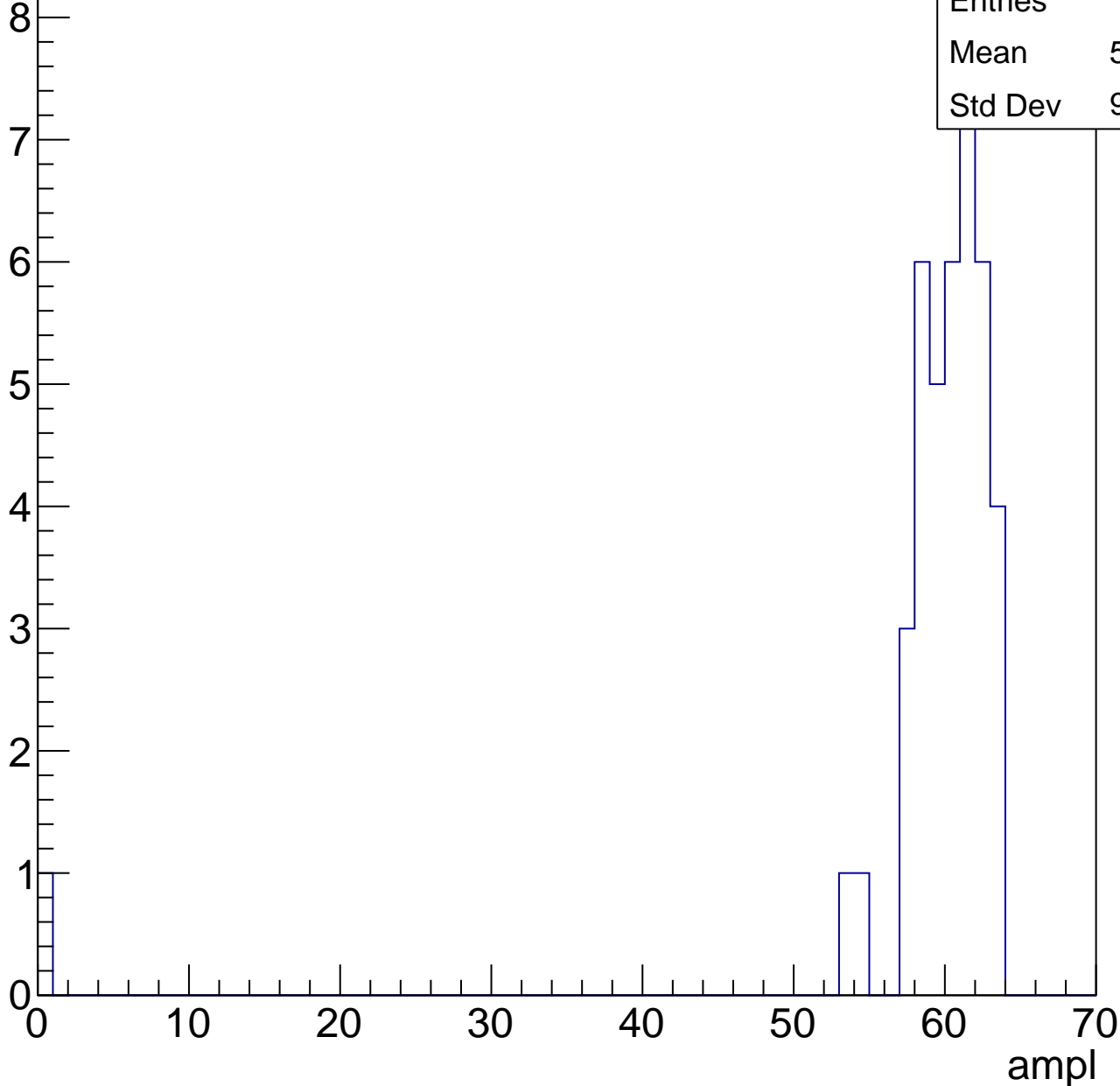


# B1L101S, U8-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	41
Mean	58.37
Std Dev	9.499

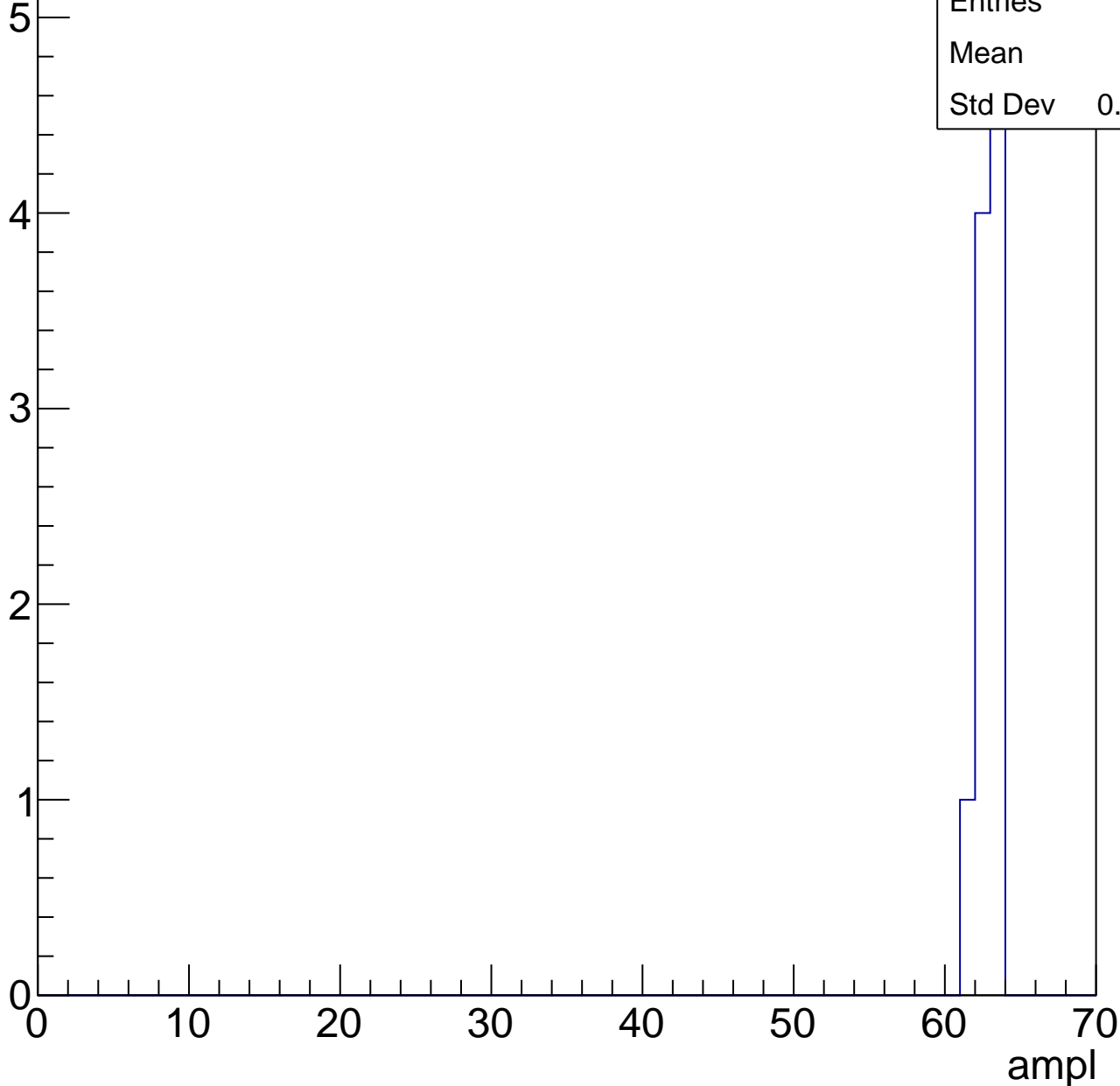


# B1L101S, U8-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	10
Mean	62.4
Std Dev	0.6633





# B1L101S, U8-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	6.667
Std Dev	9.428

# B1L101S, U8-ch84, adc0

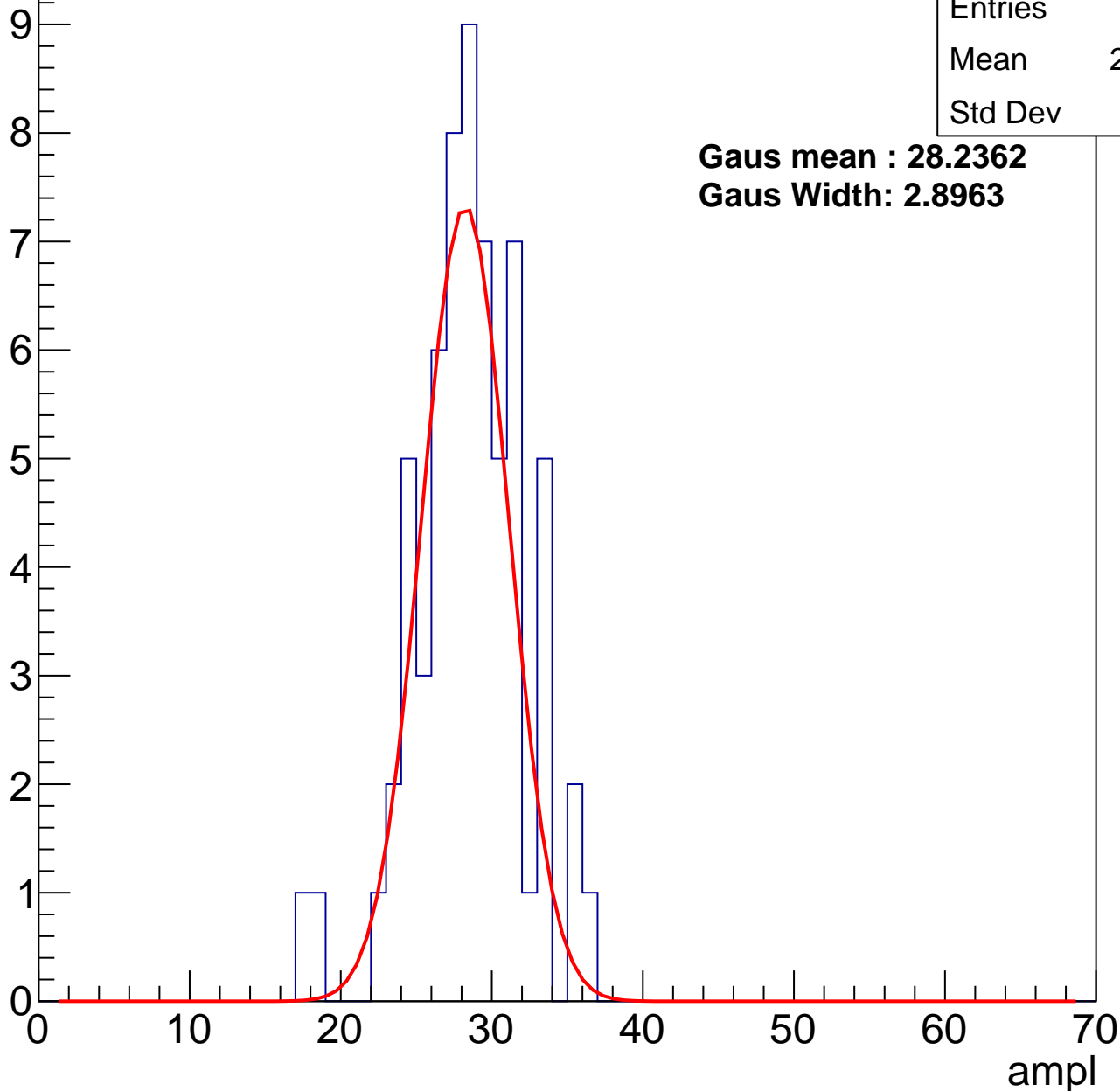
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	28.05
Std Dev	3.62

**Gaus mean : 28.2362**

**Gaus Width: 2.8963**



# B1L101S, U8-ch84, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	74
Mean	35.04
Std Dev	3.185

**Gaus mean : 35.6265**

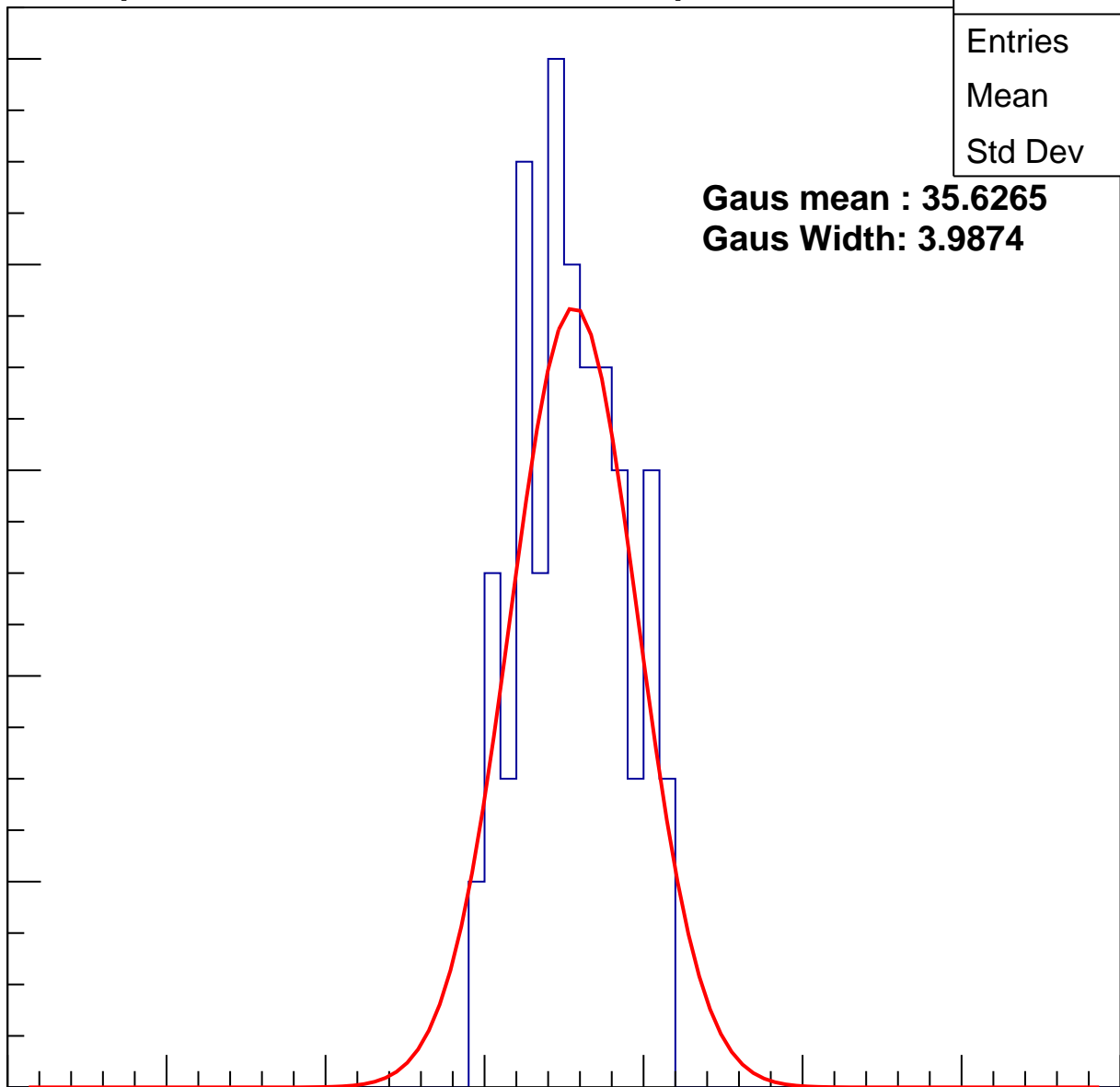
**Gaus Width: 3.9874**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U8-ch84, adc2

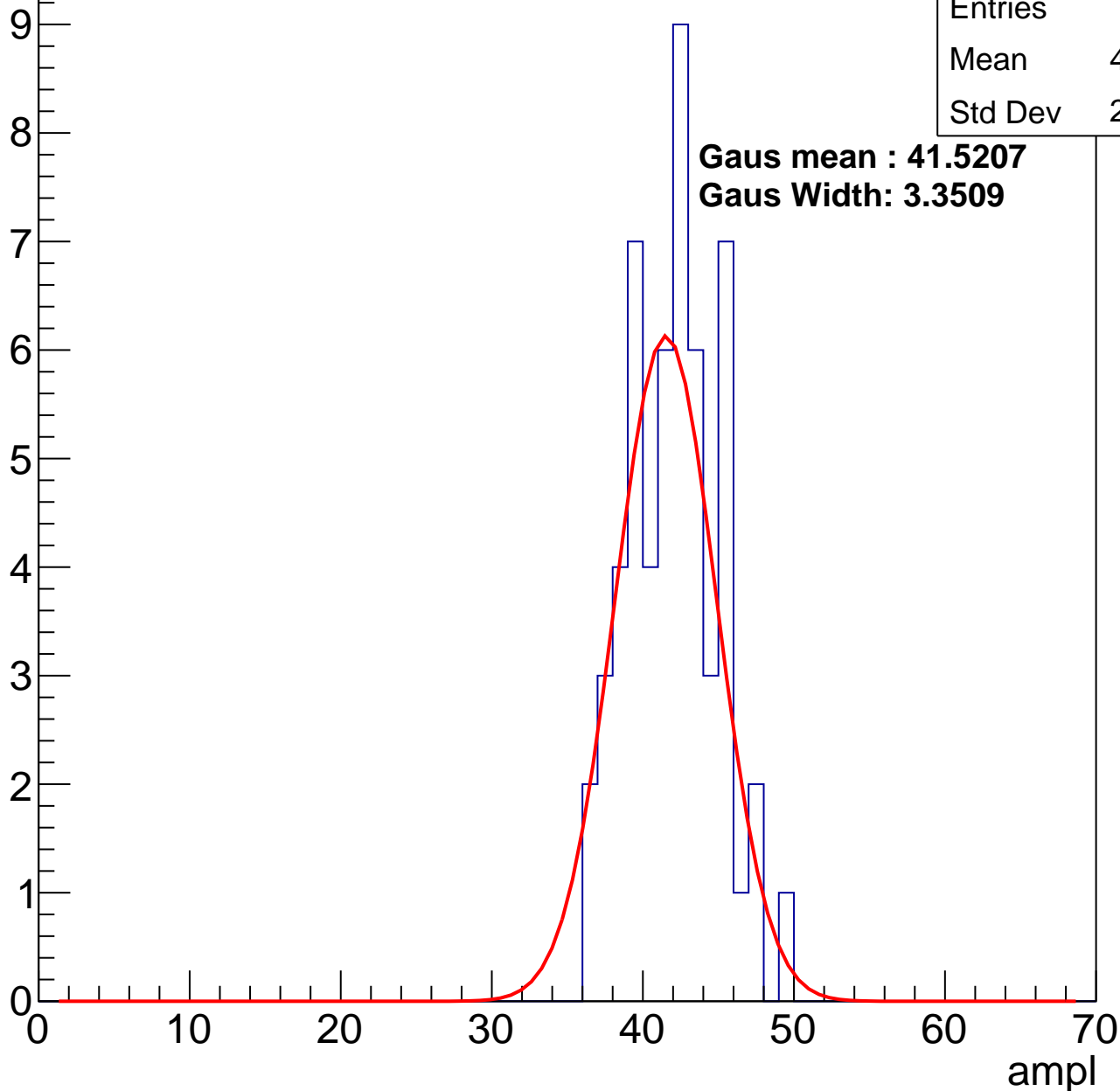
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	41.56
Std Dev	2.959

**Gaus mean : 41.5207**

**Gaus Width: 3.3509**

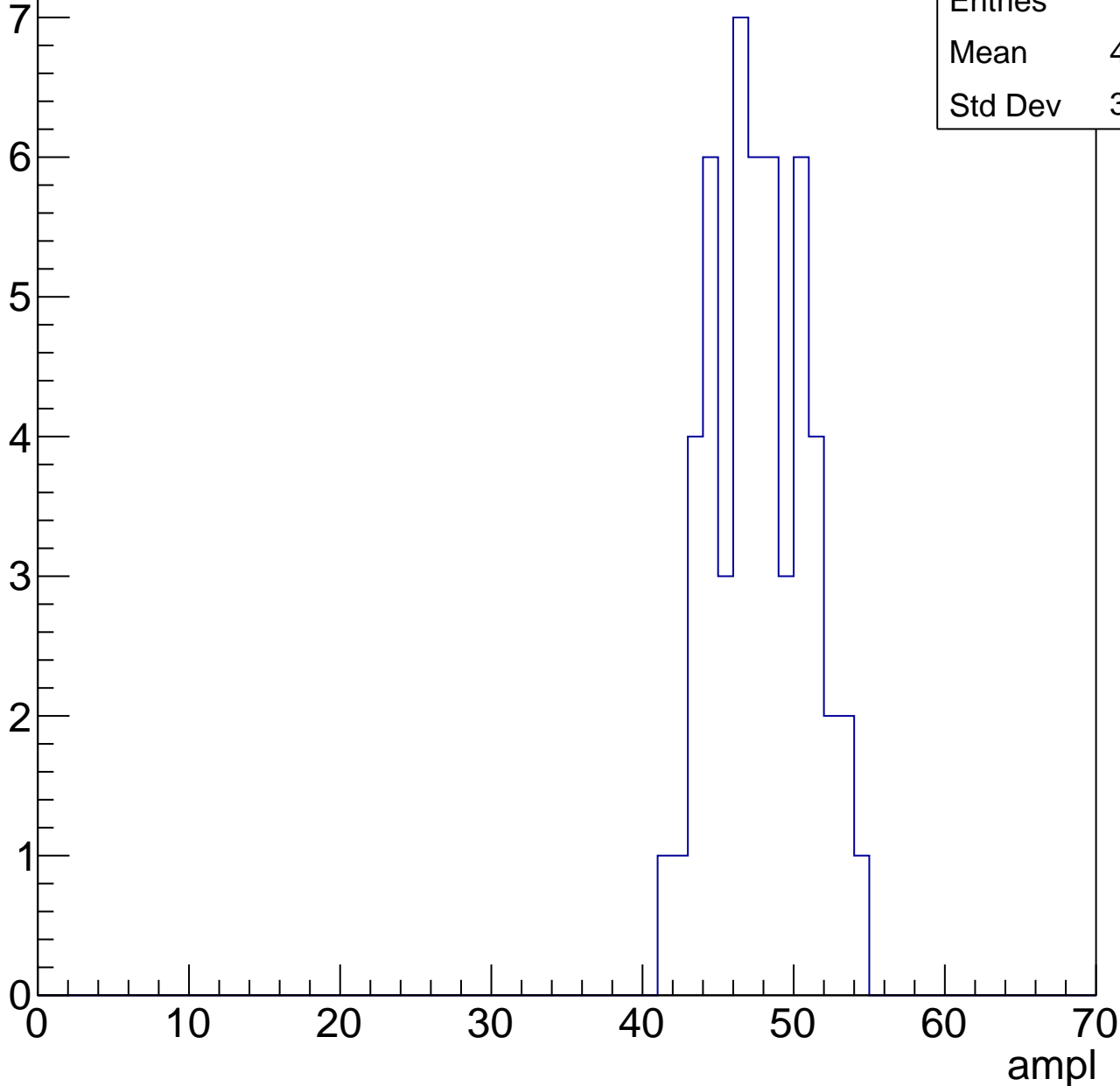


# B1L101S, U8-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

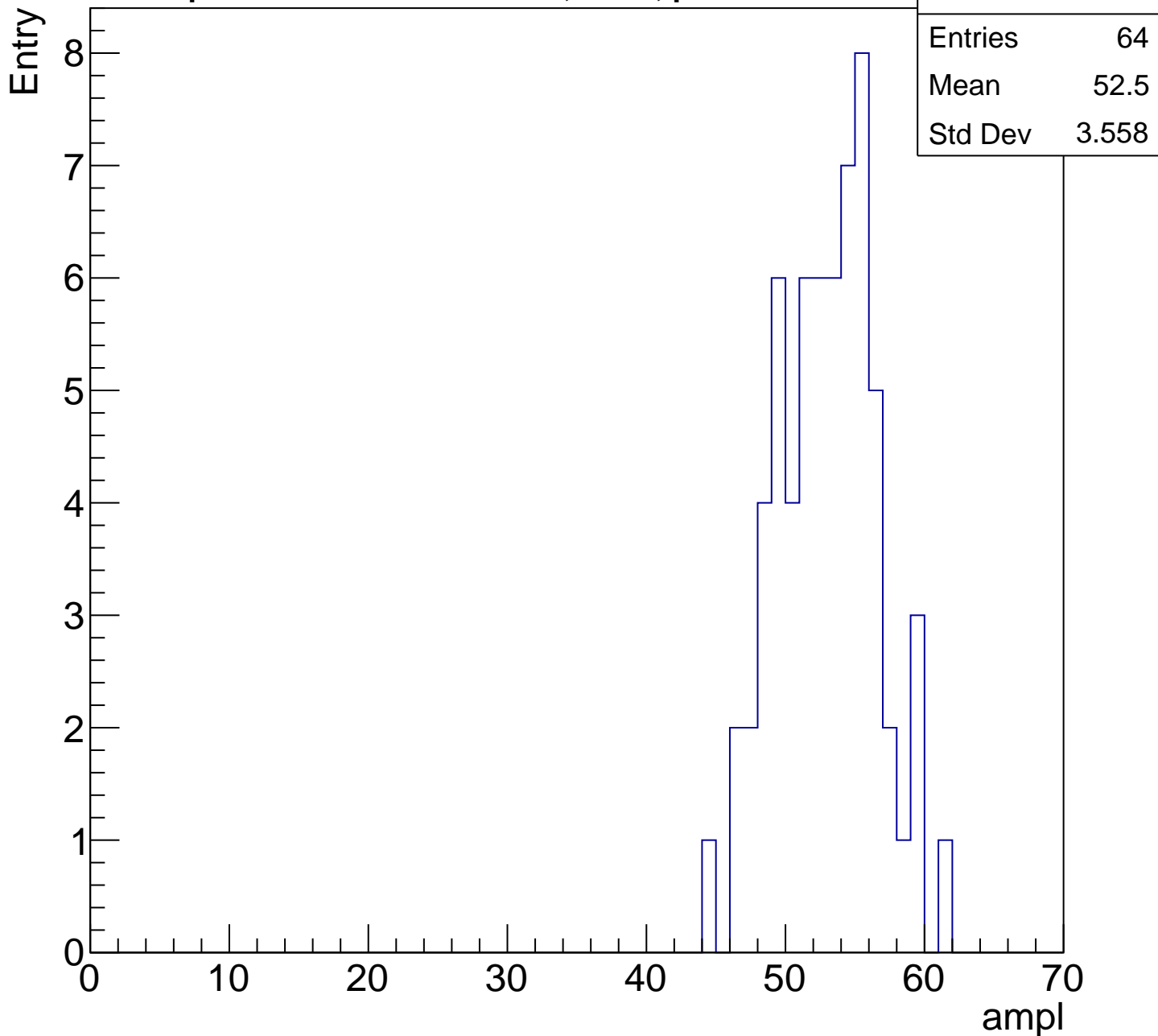
Entry

Entries	52
Mean	47.33
Std Dev	3.099



# B1L101S, U8-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U8-ch84, adc5

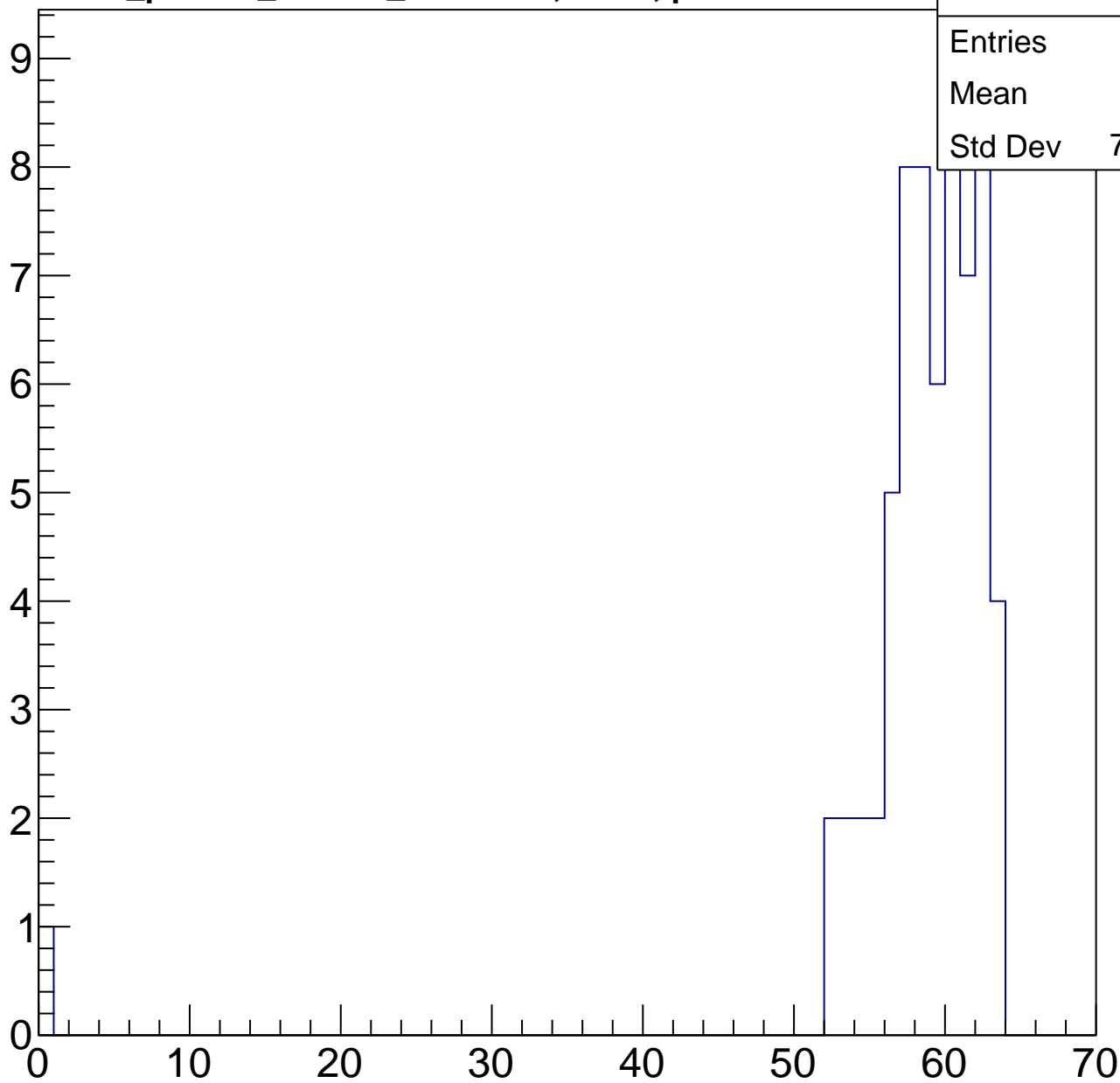
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	64
Mean	57.8
Std Dev	7.813

ampl

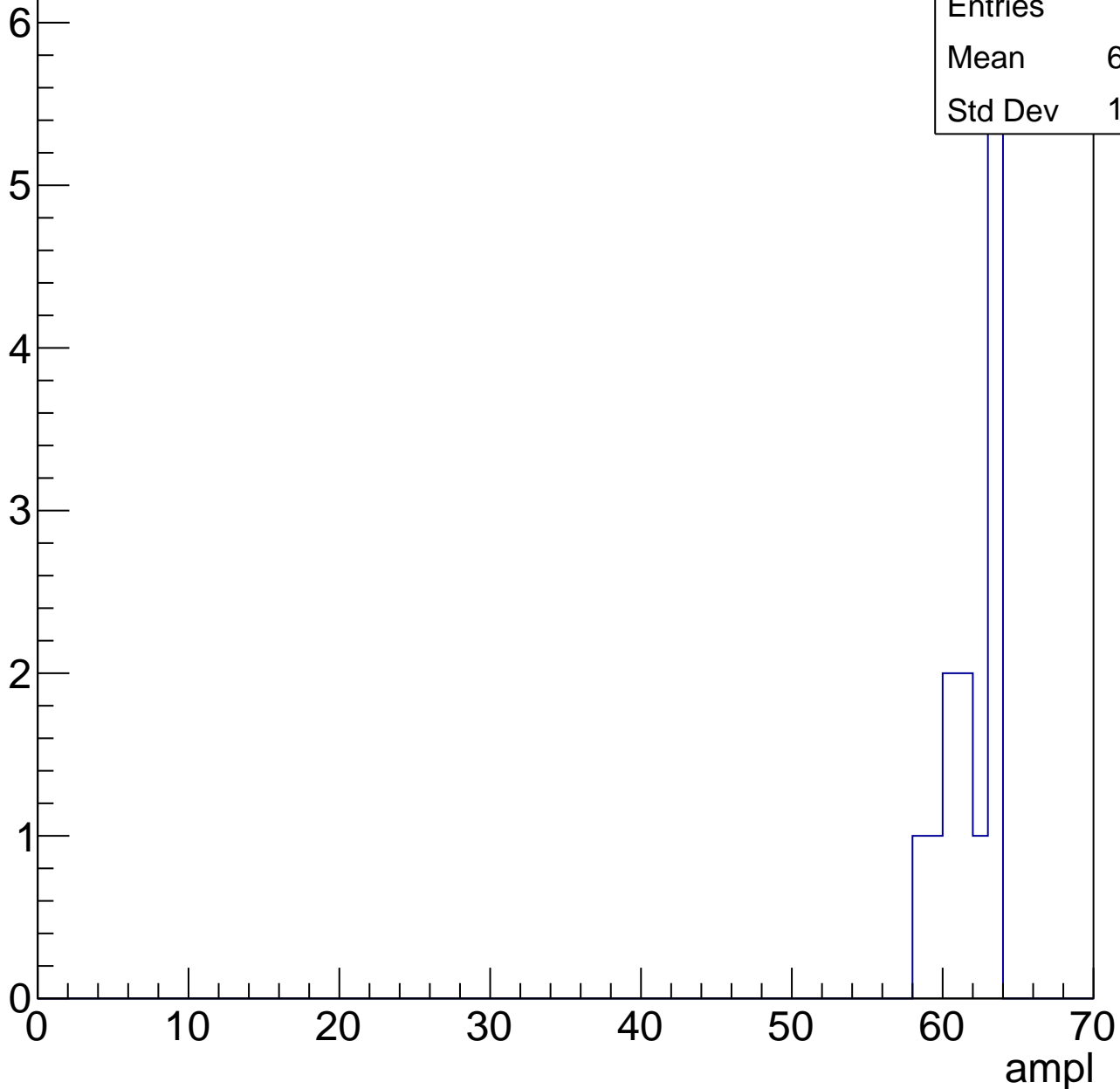


# B1L101S, U8-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	13
Mean	61.46
Std Dev	1.692





# B1L101S, U8-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch85, adc0

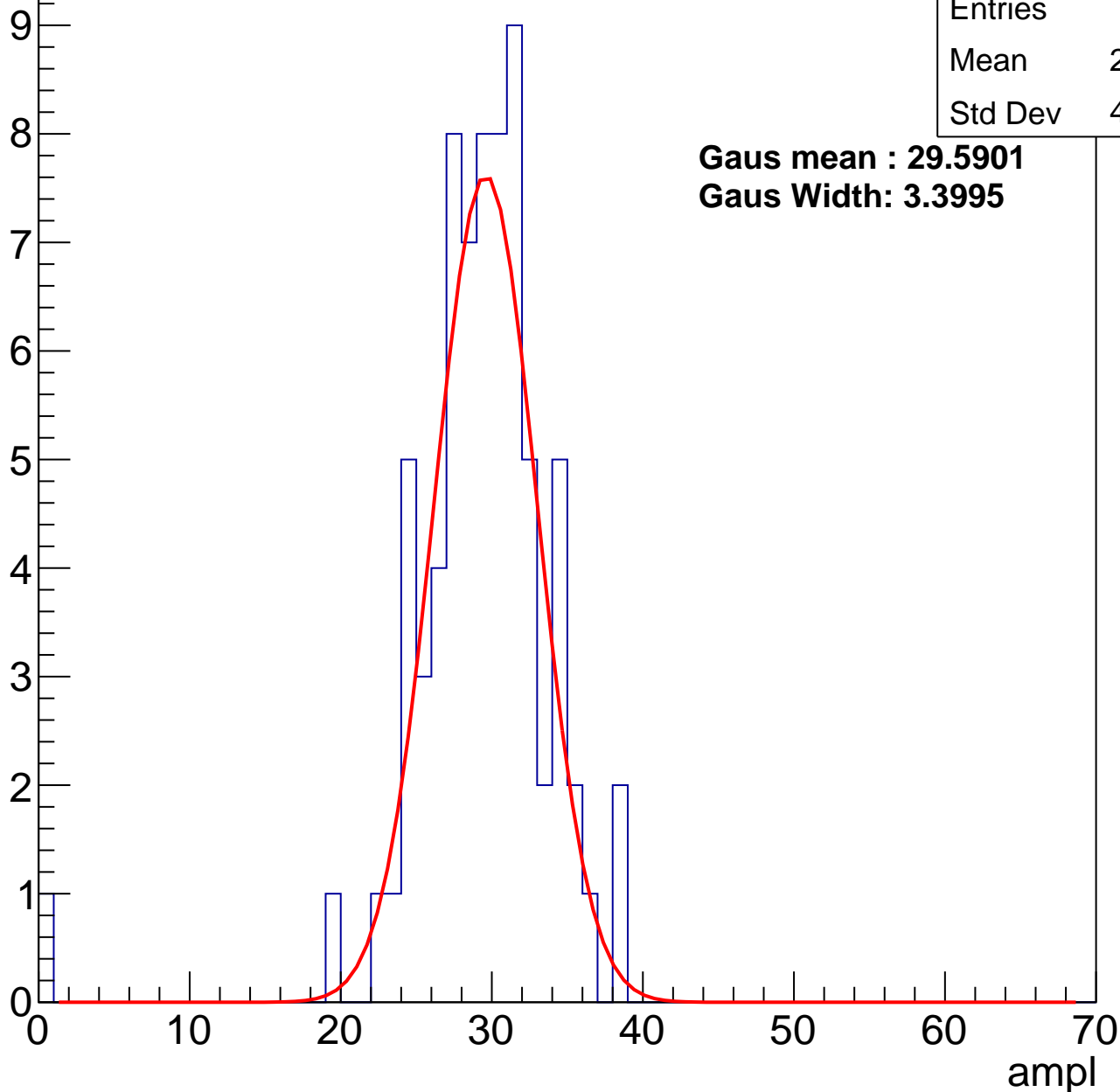
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	28.82
Std Dev	4.967

**Gaus mean : 29.5901**

**Gaus Width: 3.3995**



# B1L101S, U8-ch85, adc1

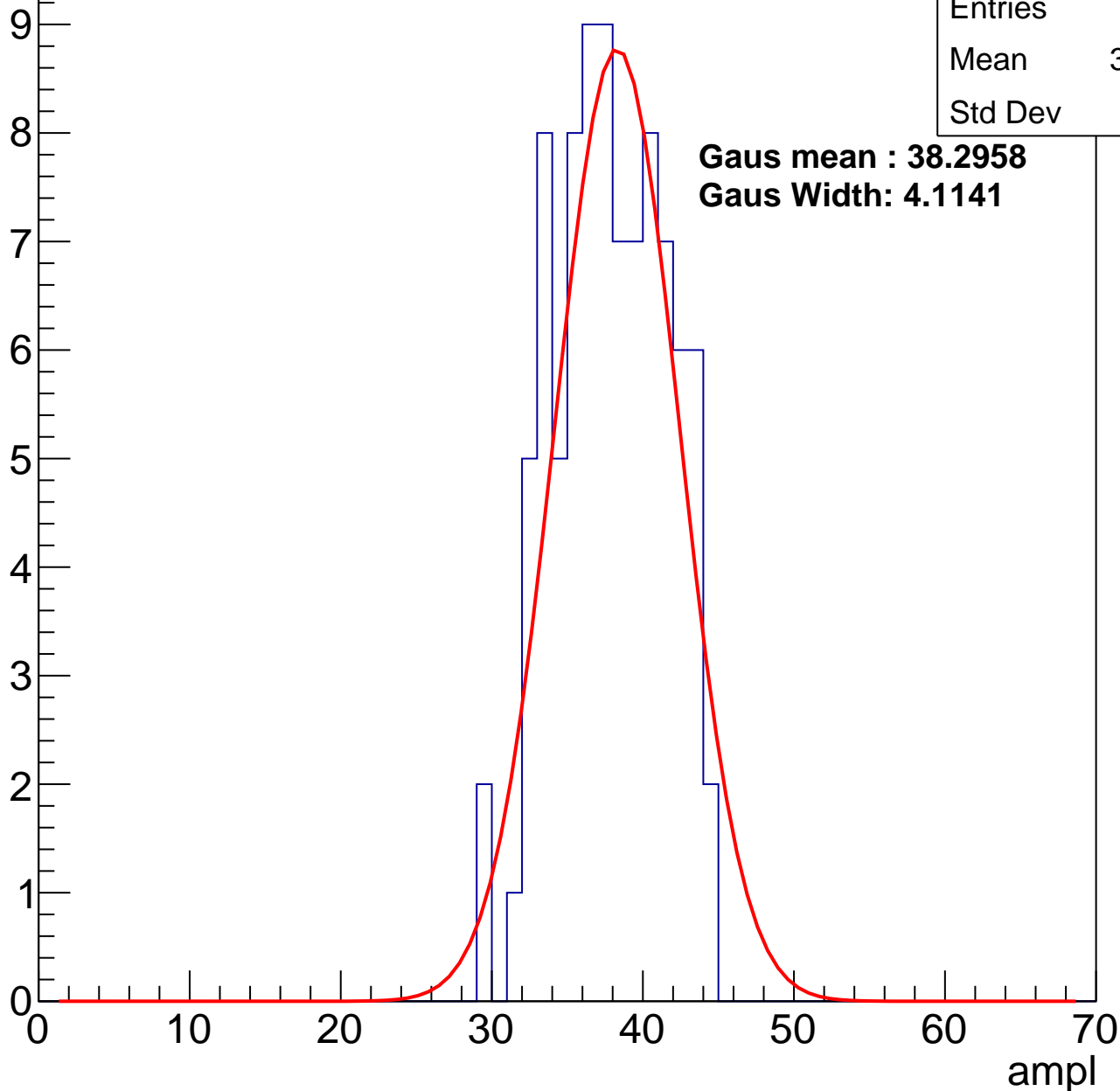
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	90
Mean	37.38
Std Dev	3.61

**Gaus mean : 38.2958**

**Gaus Width: 4.1141**



# B1L101S, U8-ch85, adc2

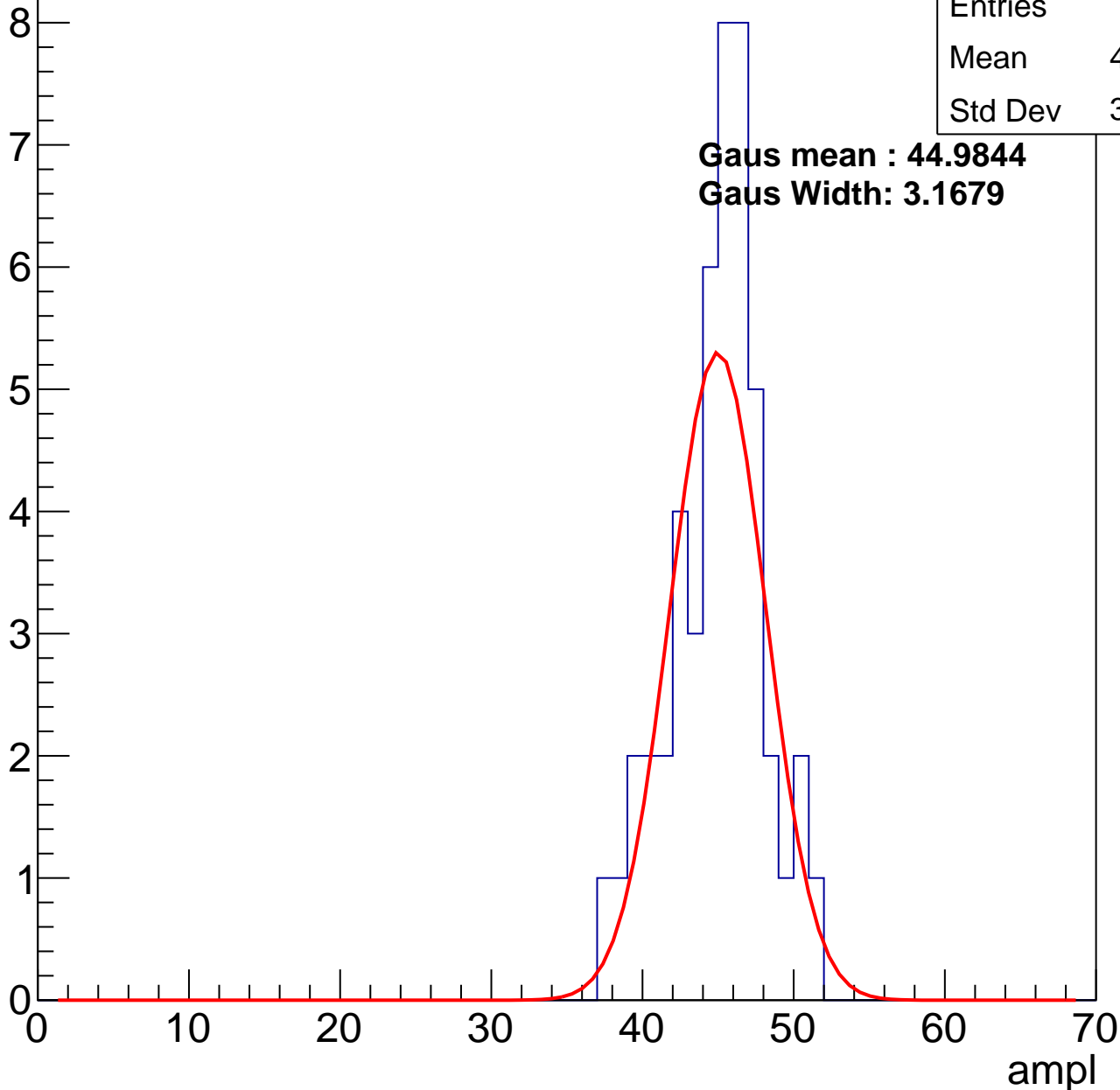
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	44.48
Std Dev	3.082

**Gaus mean : 44.9844**

**Gaus Width: 3.1679**

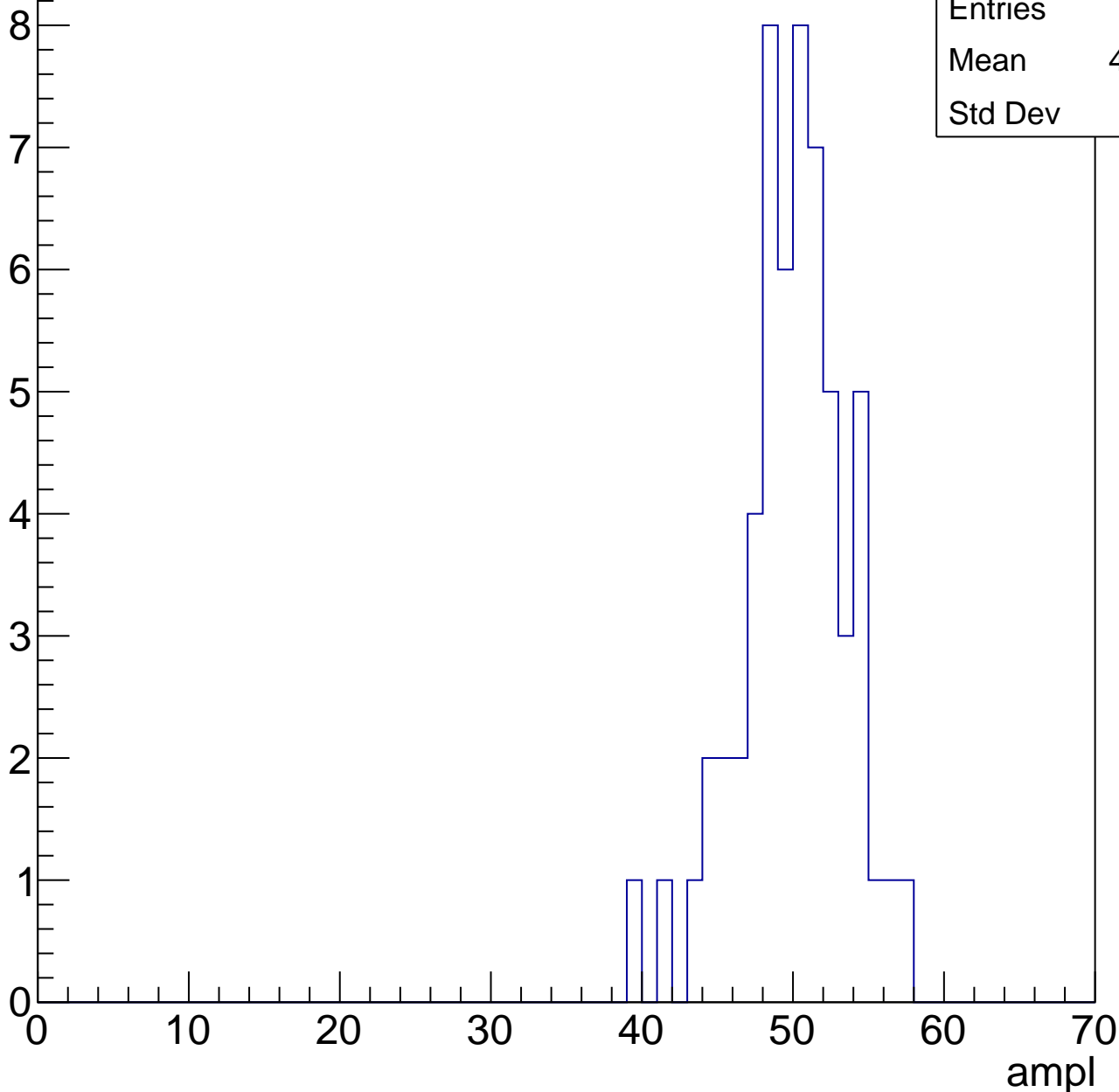


# B1L101S, U8-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	49.53
Std Dev	3.5

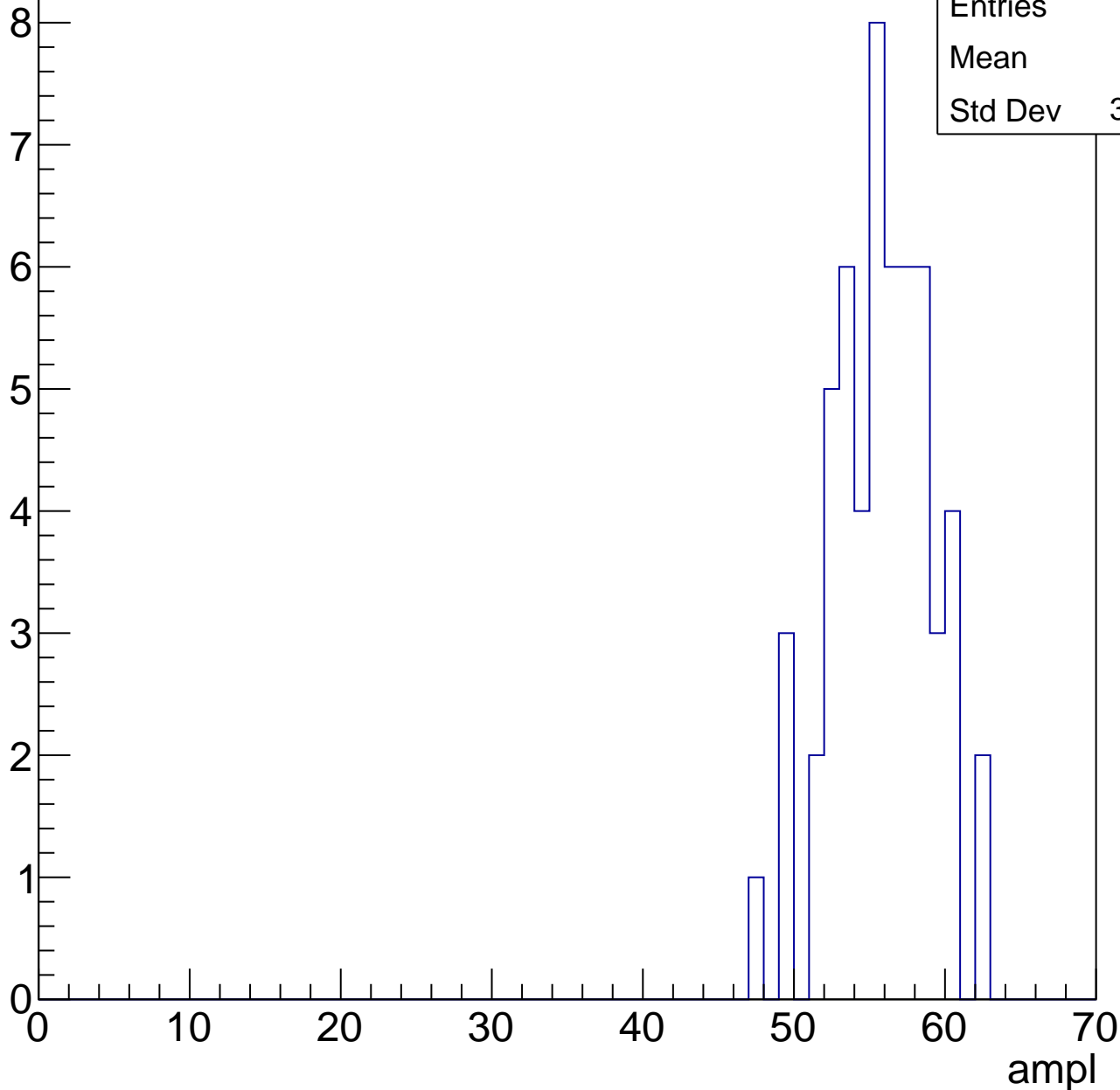


# B1L101S, U8-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	55.3
Std Dev	3.278

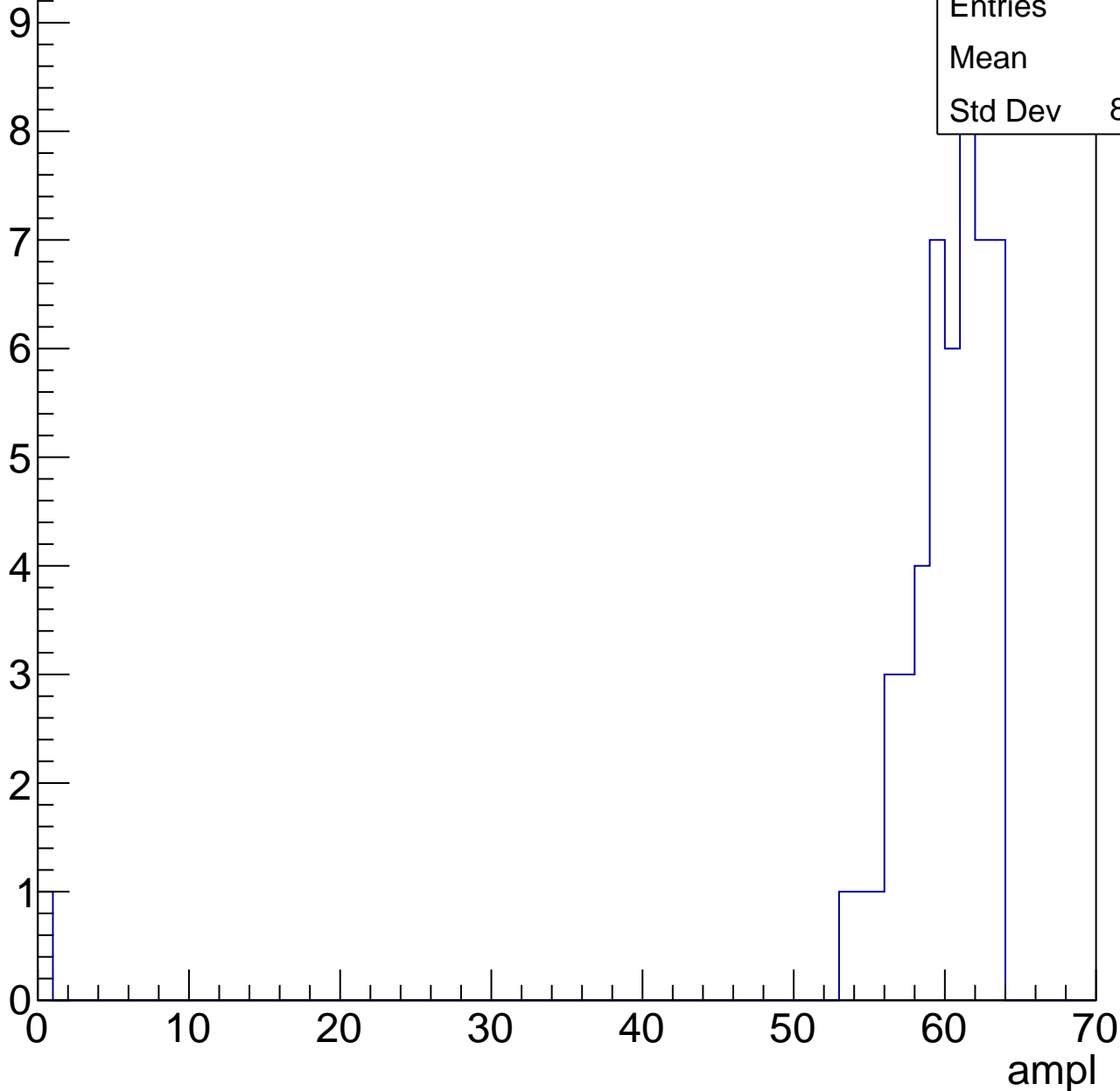


# B1L101S, U8-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	58.6
Std Dev	8.729



# B1L101S, U8-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch86, adc0

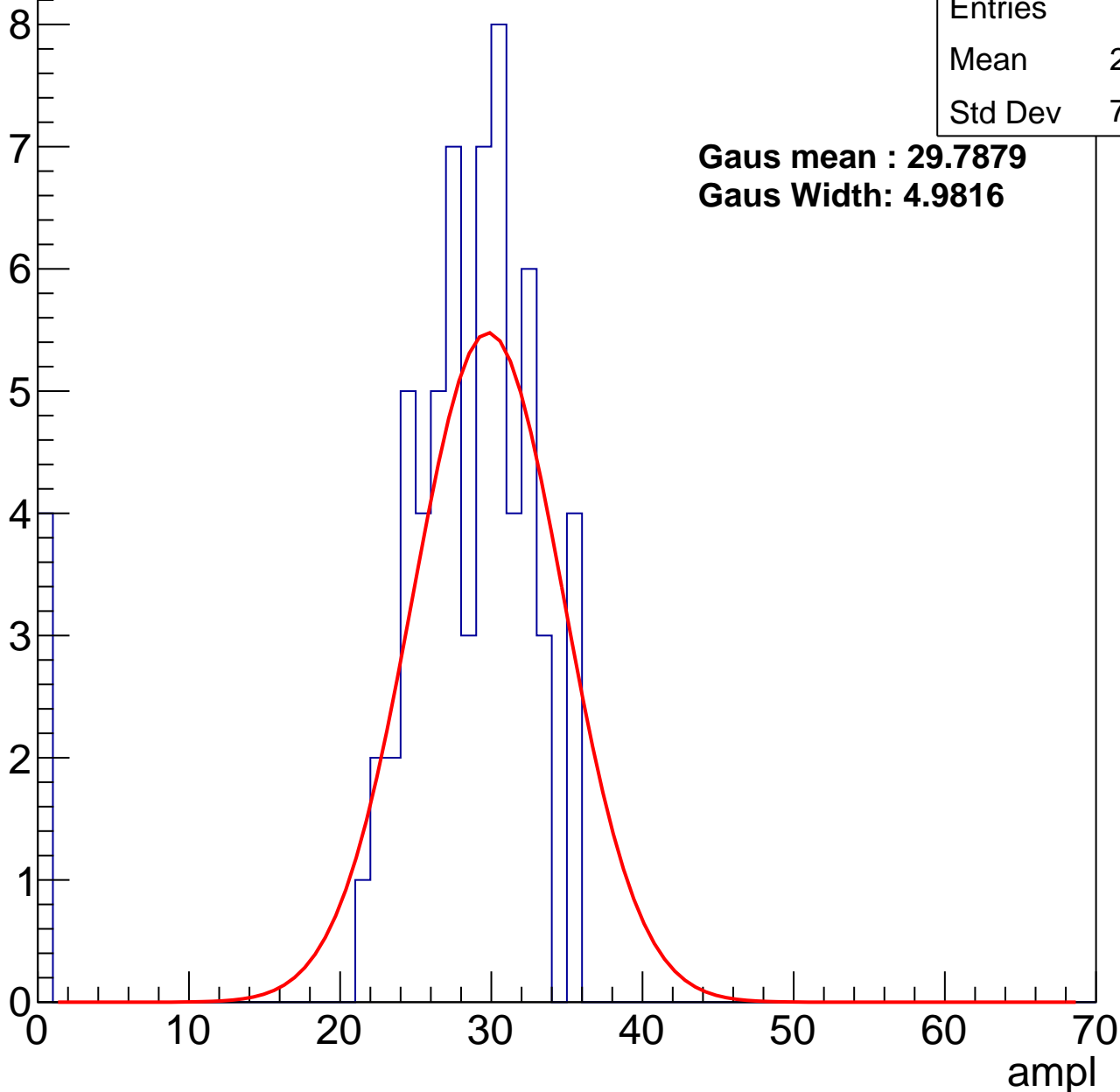
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	26.65
Std Dev	7.619

**Gaus mean : 29.7879**

**Gaus Width: 4.9816**



# B1L101S, U8-ch86, adc1

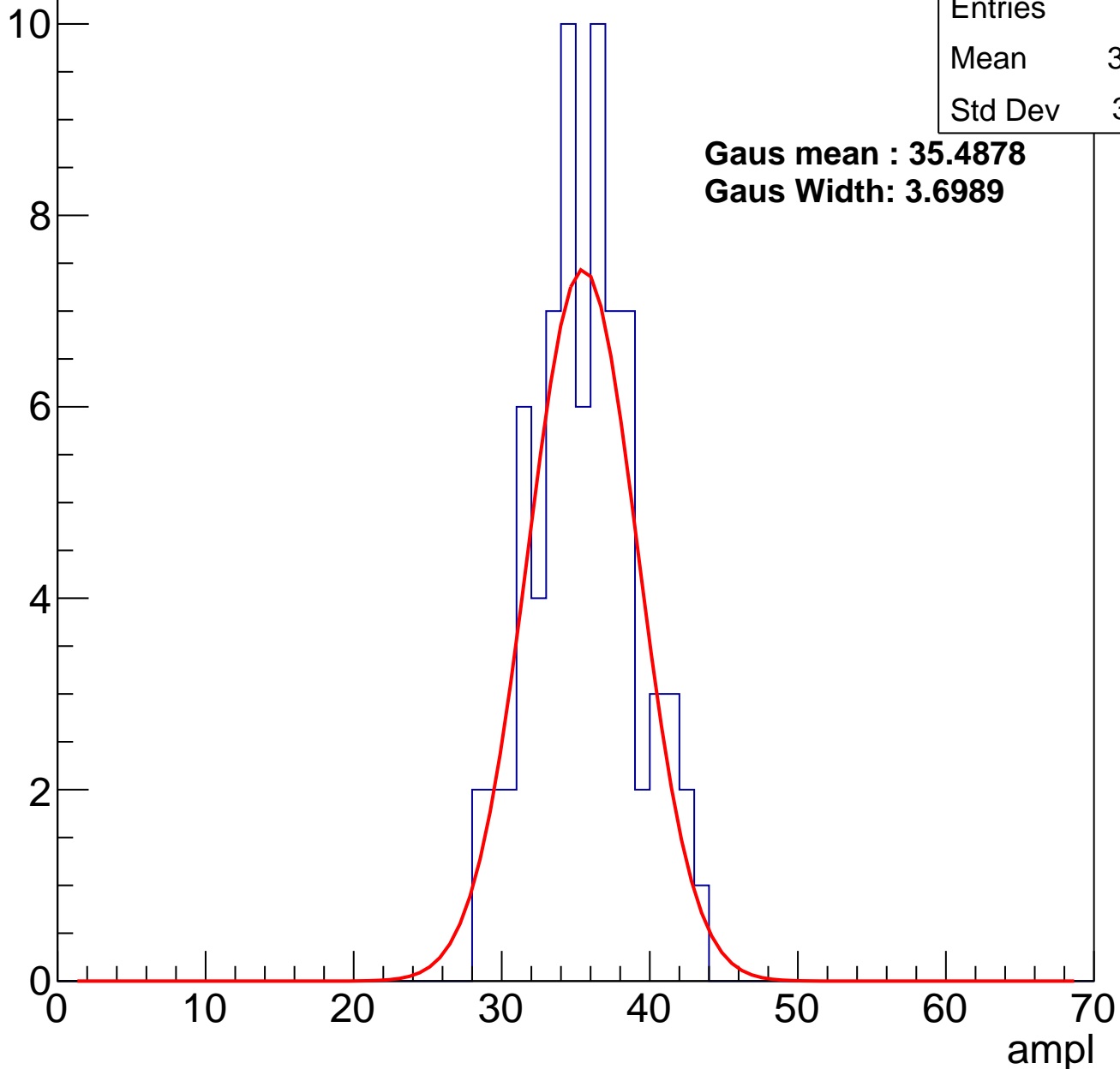
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	74
Mean	35.16
Std Dev	3.421

**Gaus mean : 35.4878**

**Gaus Width: 3.6989**

Entry



# B1L101S, U8-ch86, adc2

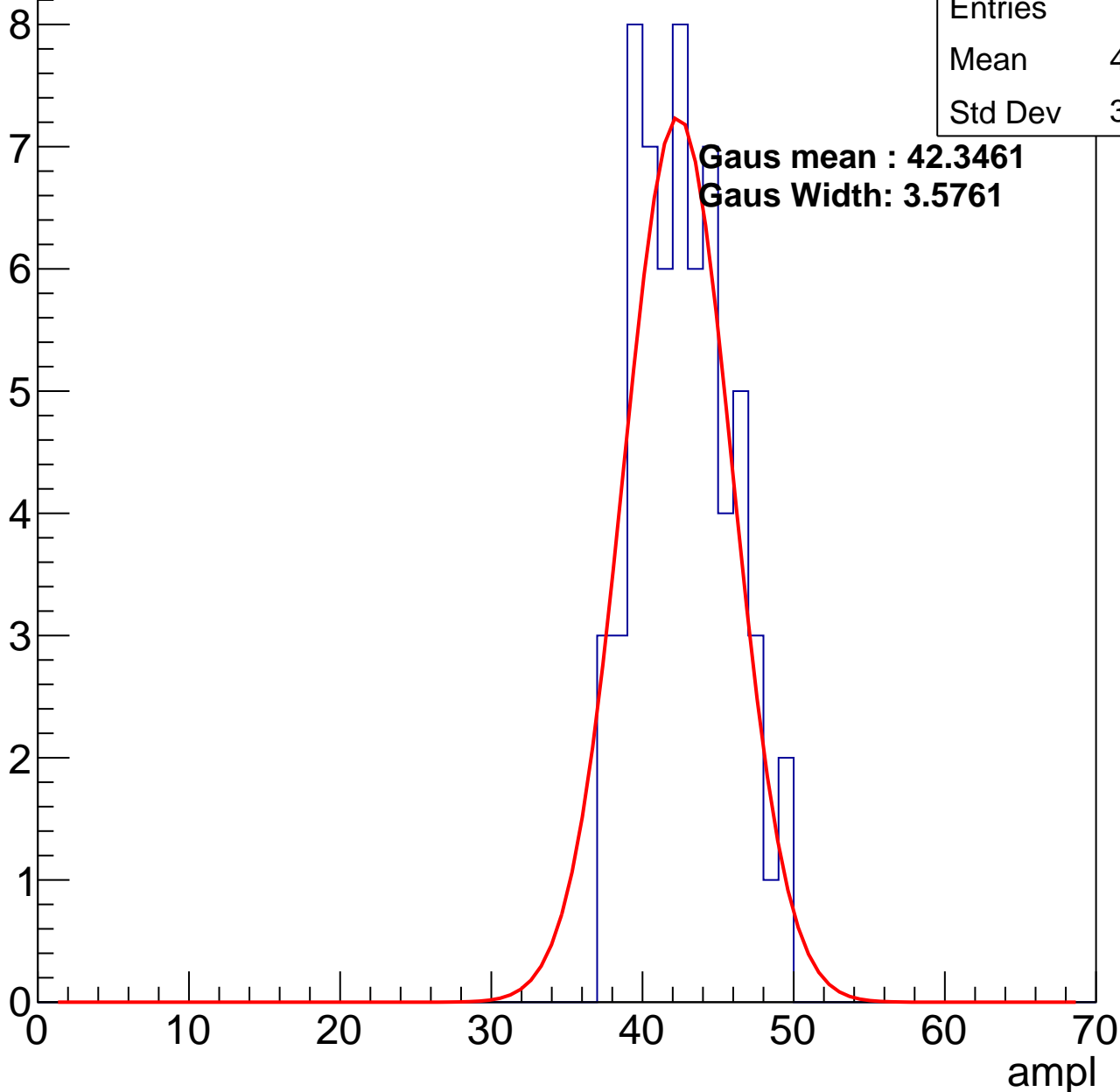
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	42.25
Std Dev	3.044

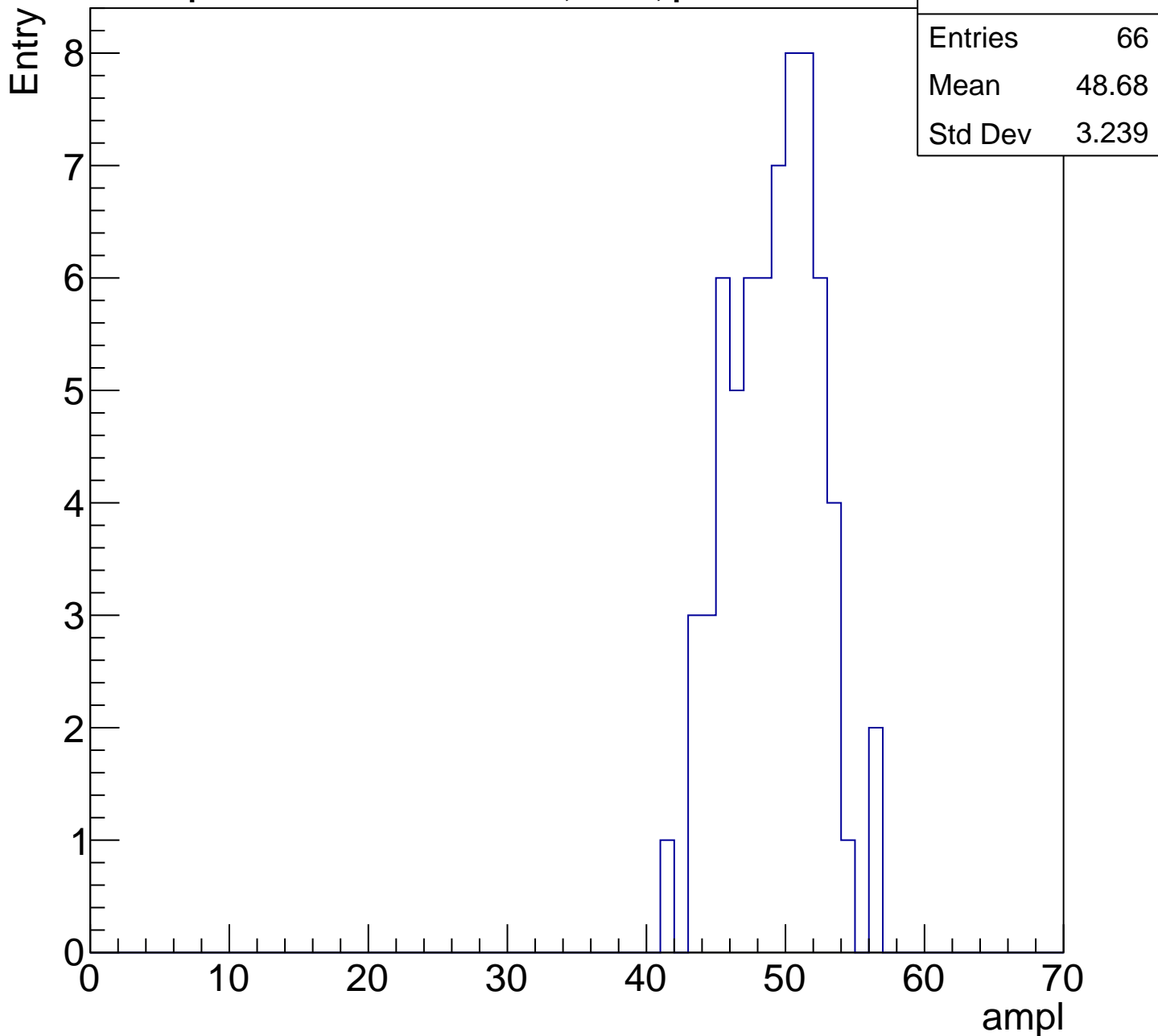
**Gaus mean : 42.3461**

**Gaus Width: 3.5761**



# B1L101S, U8-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

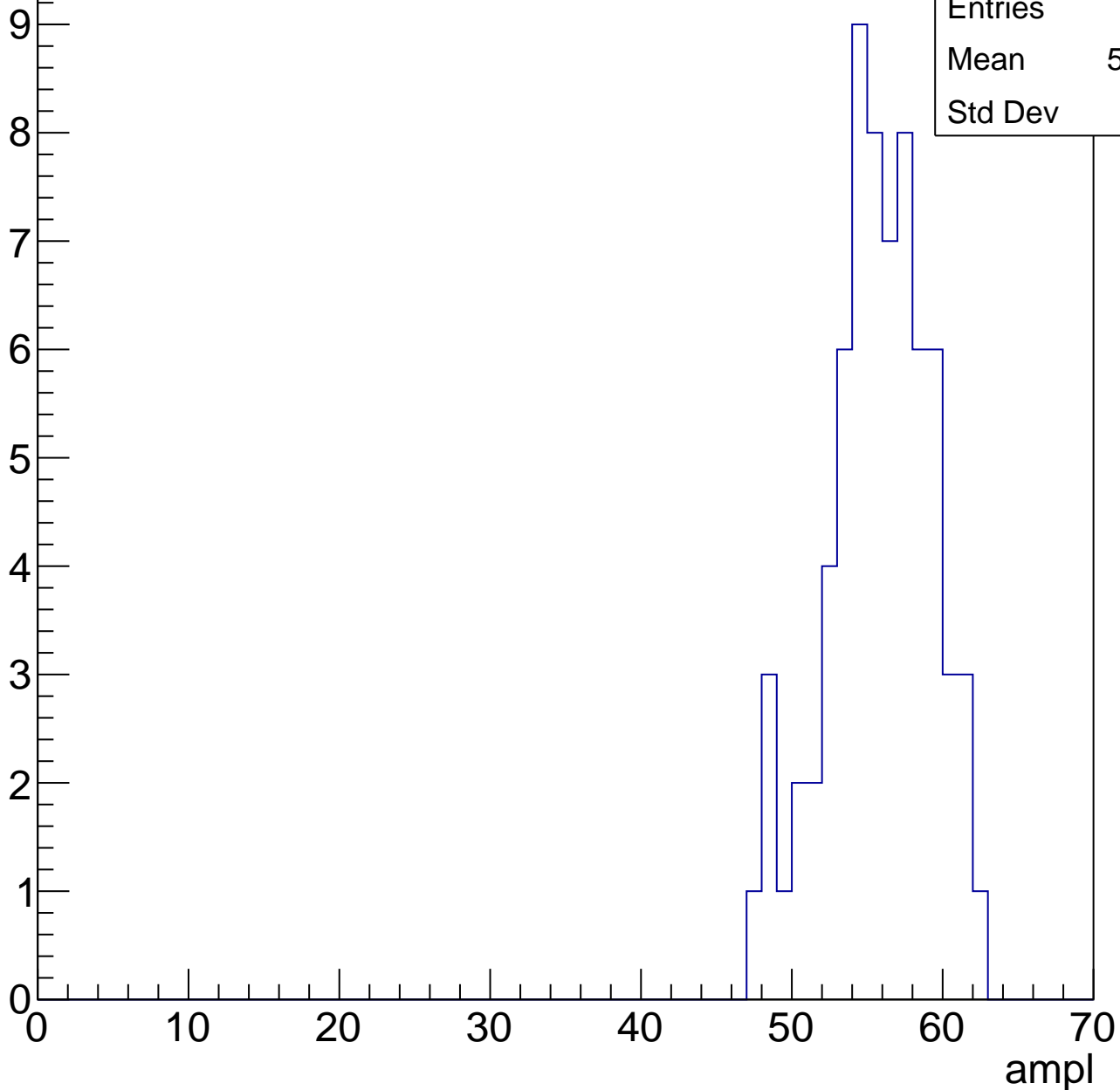


# B1L101S, U8-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	55.27
Std Dev	3.41

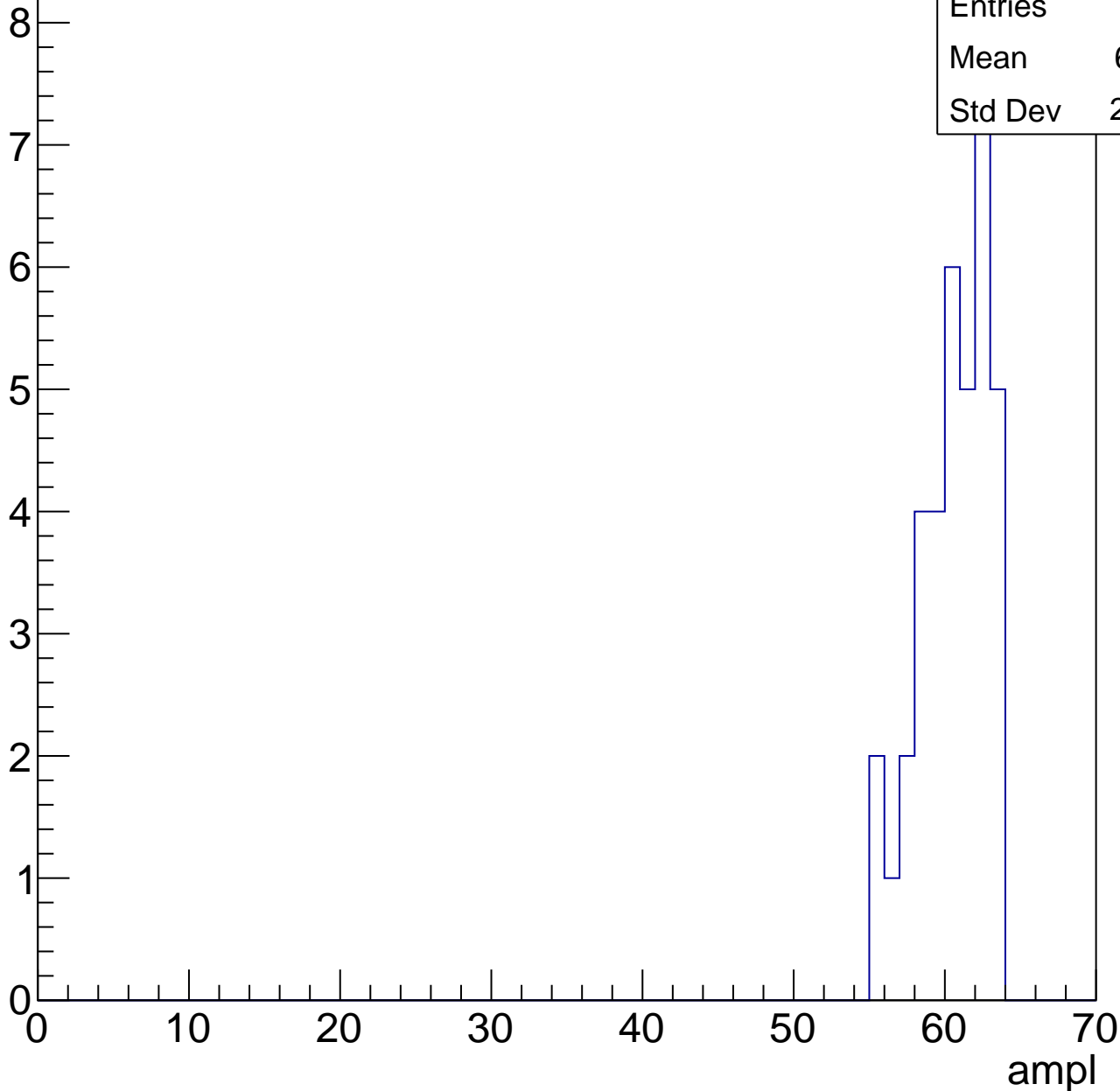


# B1L101S, U8-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	37
Mean	60.11
Std Dev	2.239

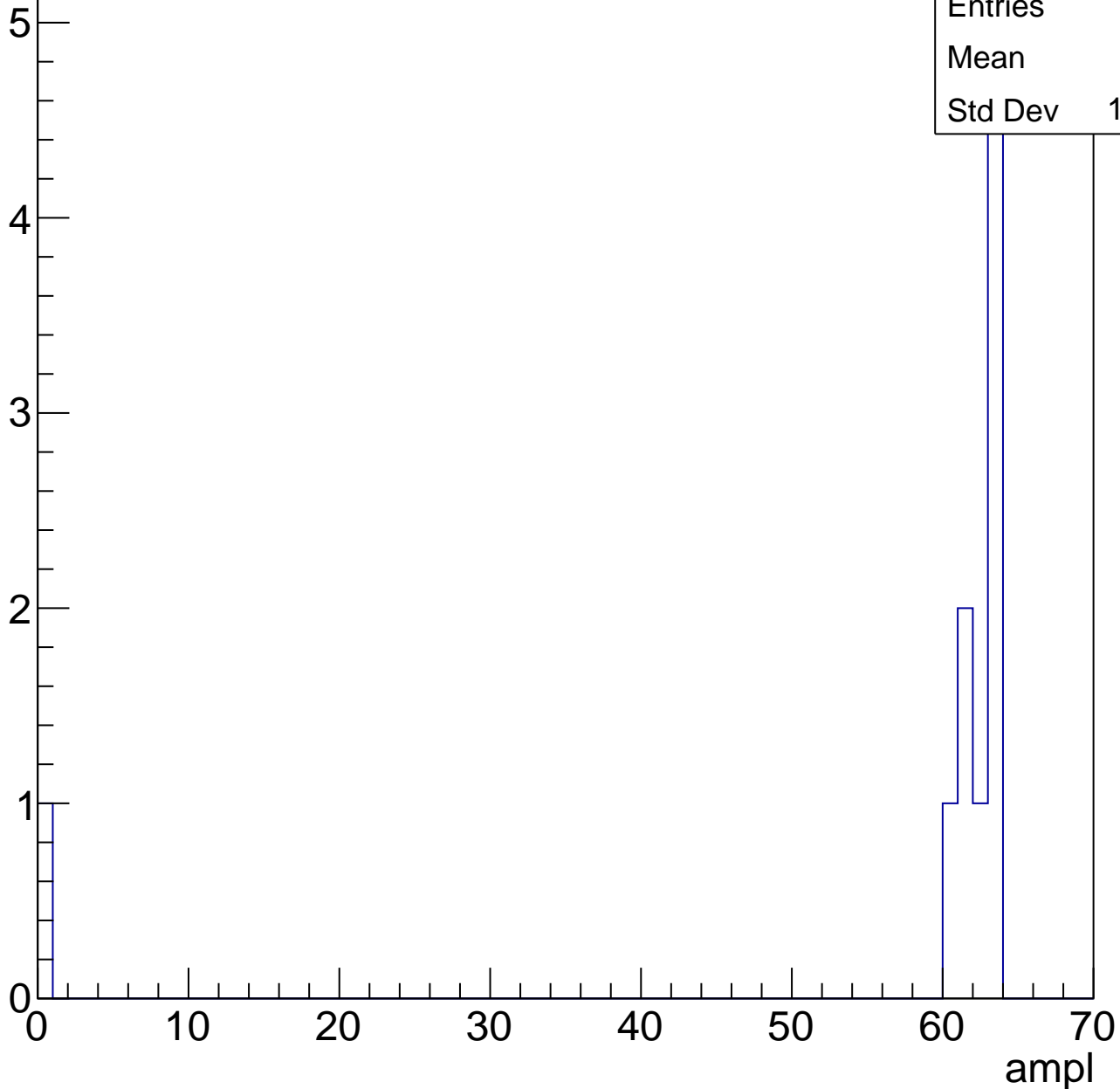


# B1L101S, U8-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	10
Mean	55.9
Std Dev	18.66





# B1L101S, U8-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U8-ch87, adc0

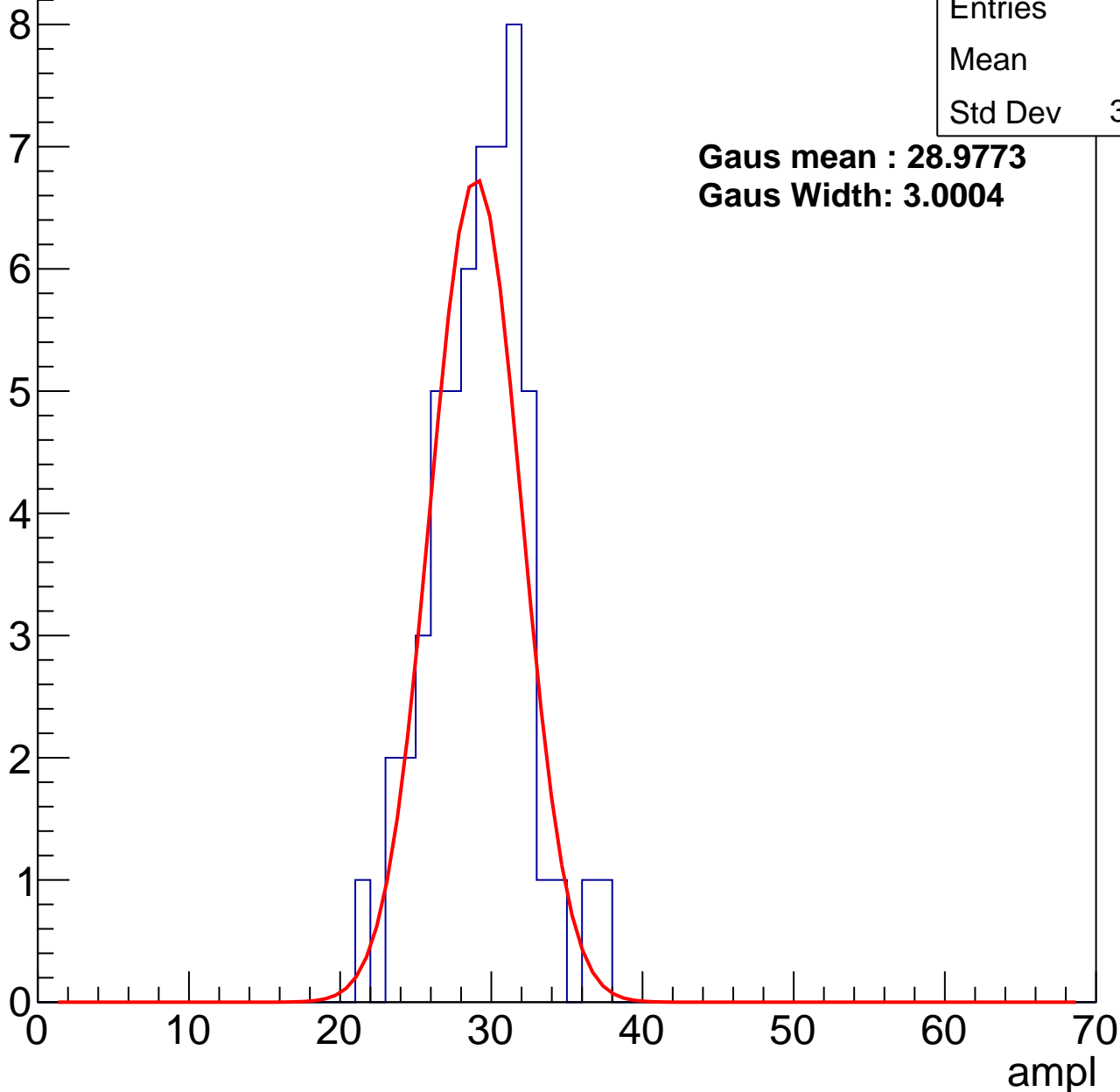
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	28.8
Std Dev	3.136

**Gaus mean : 28.9773**

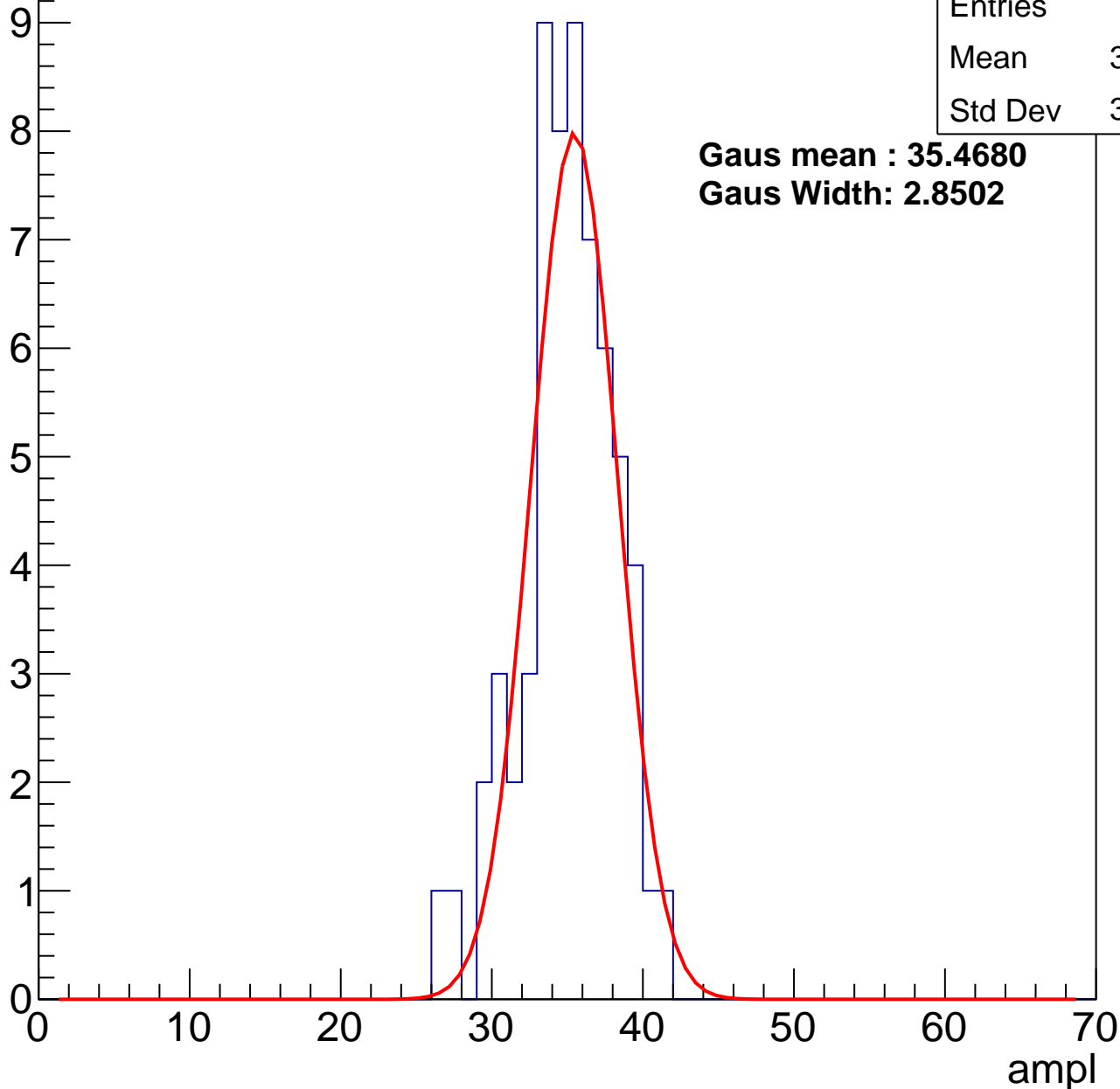
**Gaus Width: 3.0004**



# B1L101S, U8-ch87, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch87, adc2

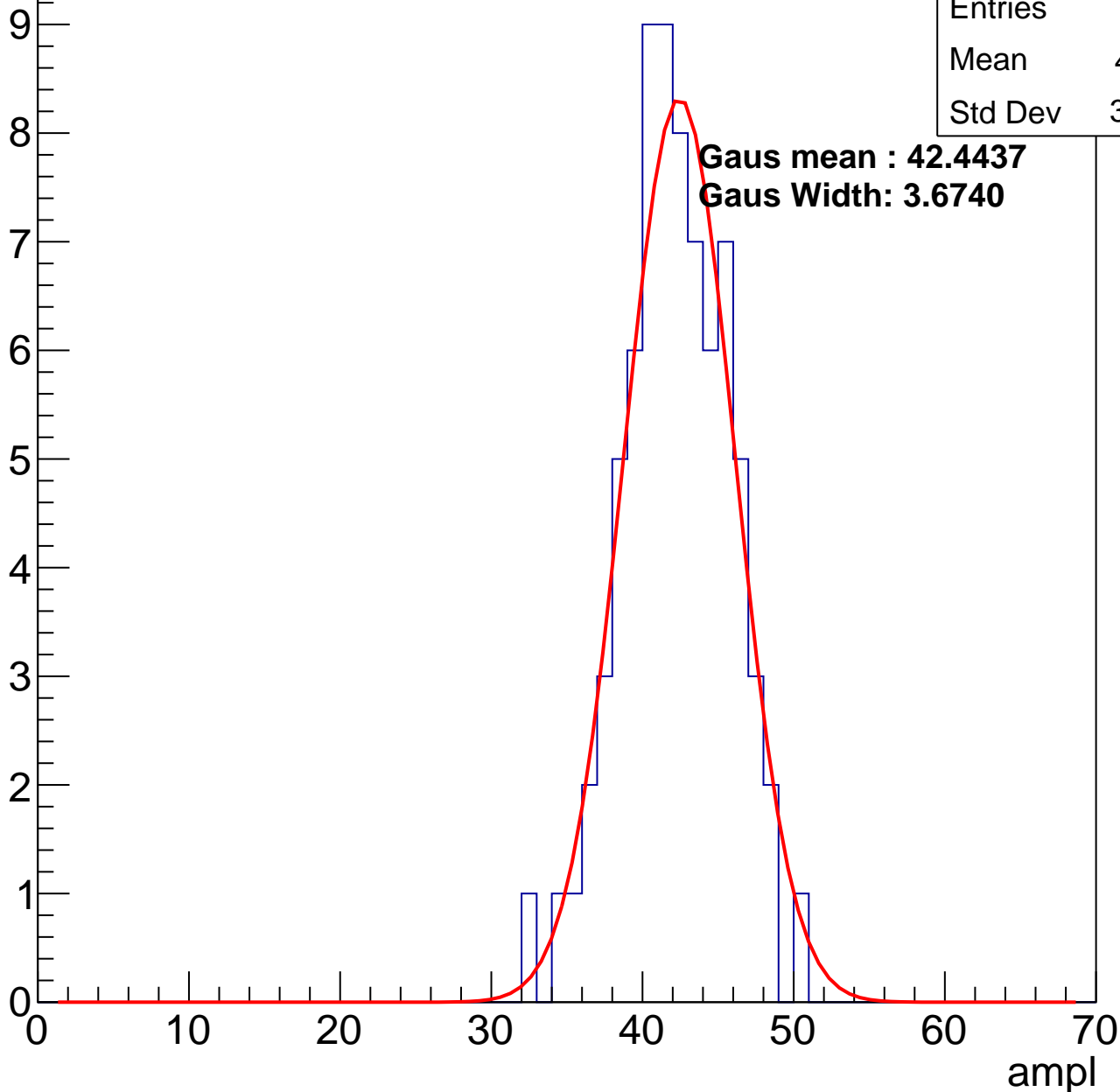
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	41.71
Std Dev	3.475

**Gaus mean : 42.4437**

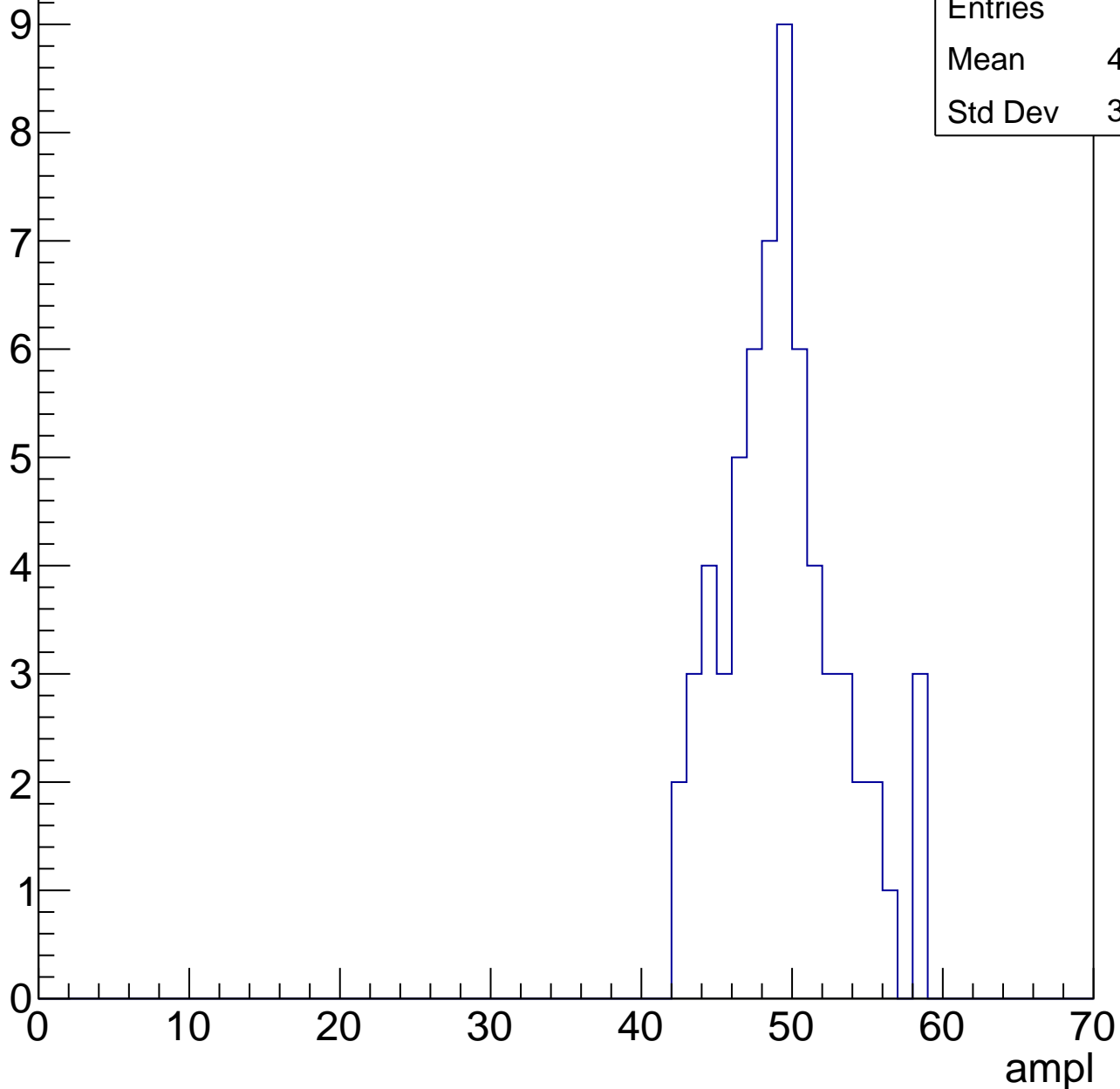
**Gaus Width: 3.6740**



# B1L101S, U8-ch87, adc3

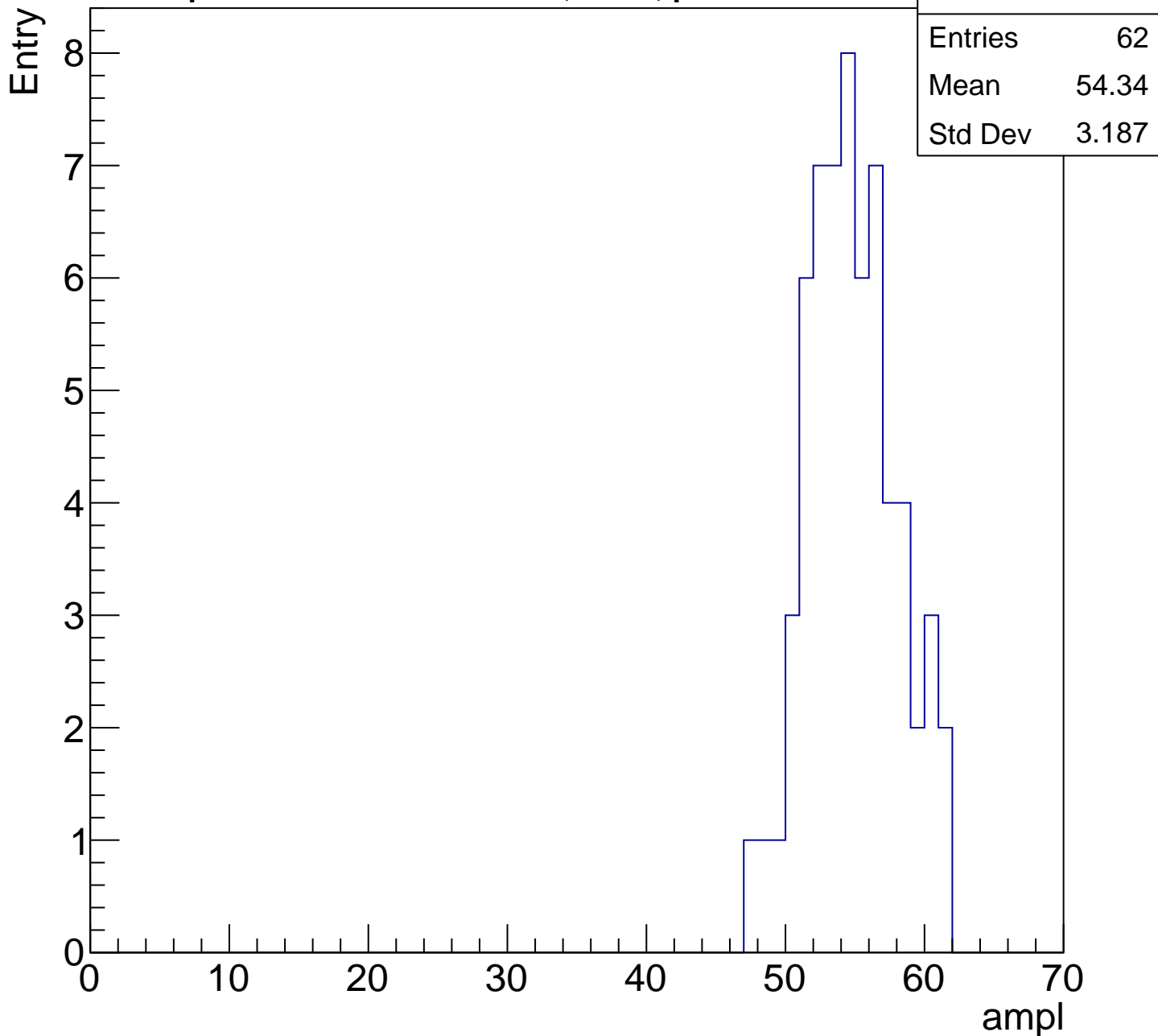
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

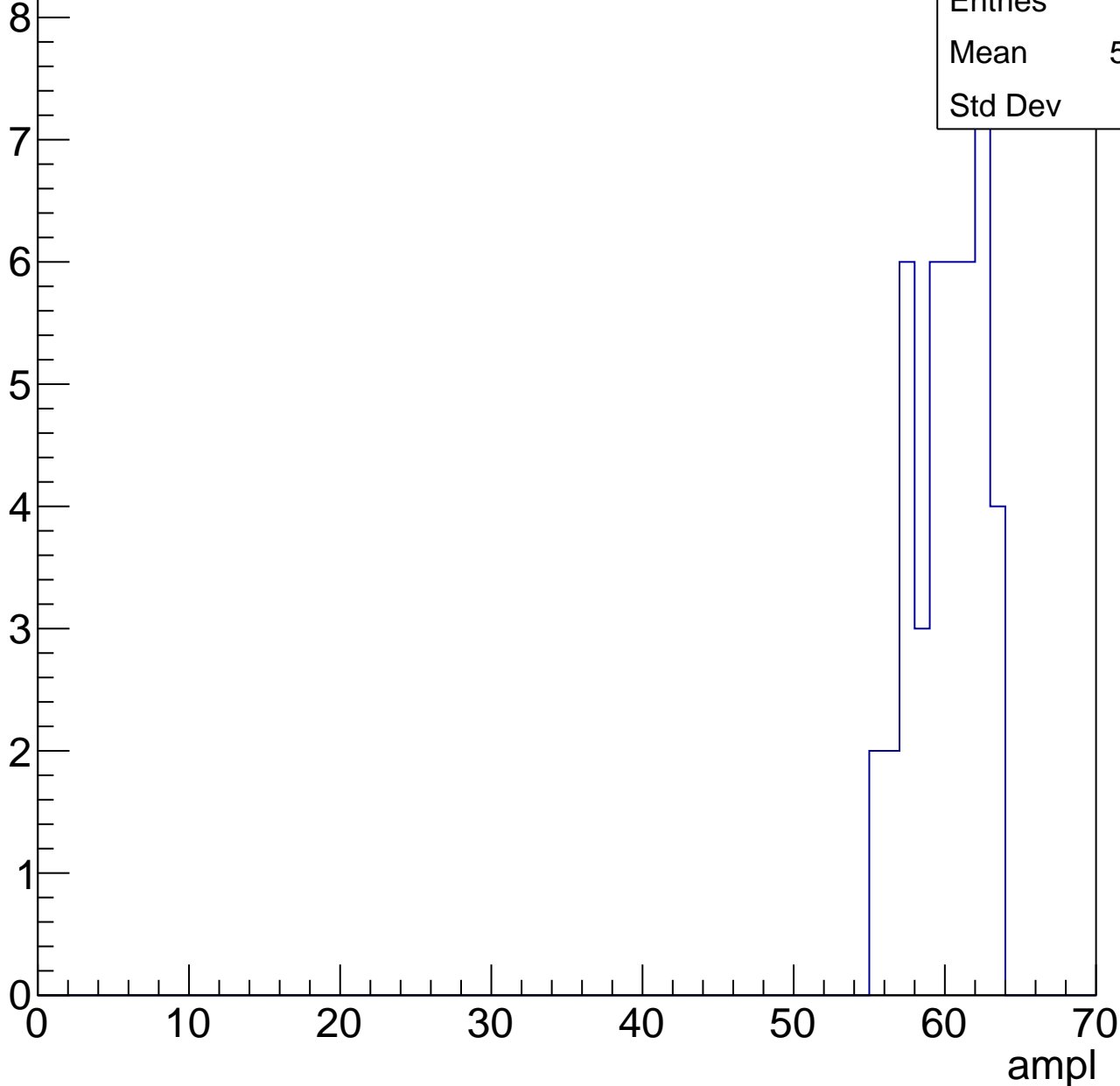


# B1L101S, U8-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	59.67
Std Dev	2.28

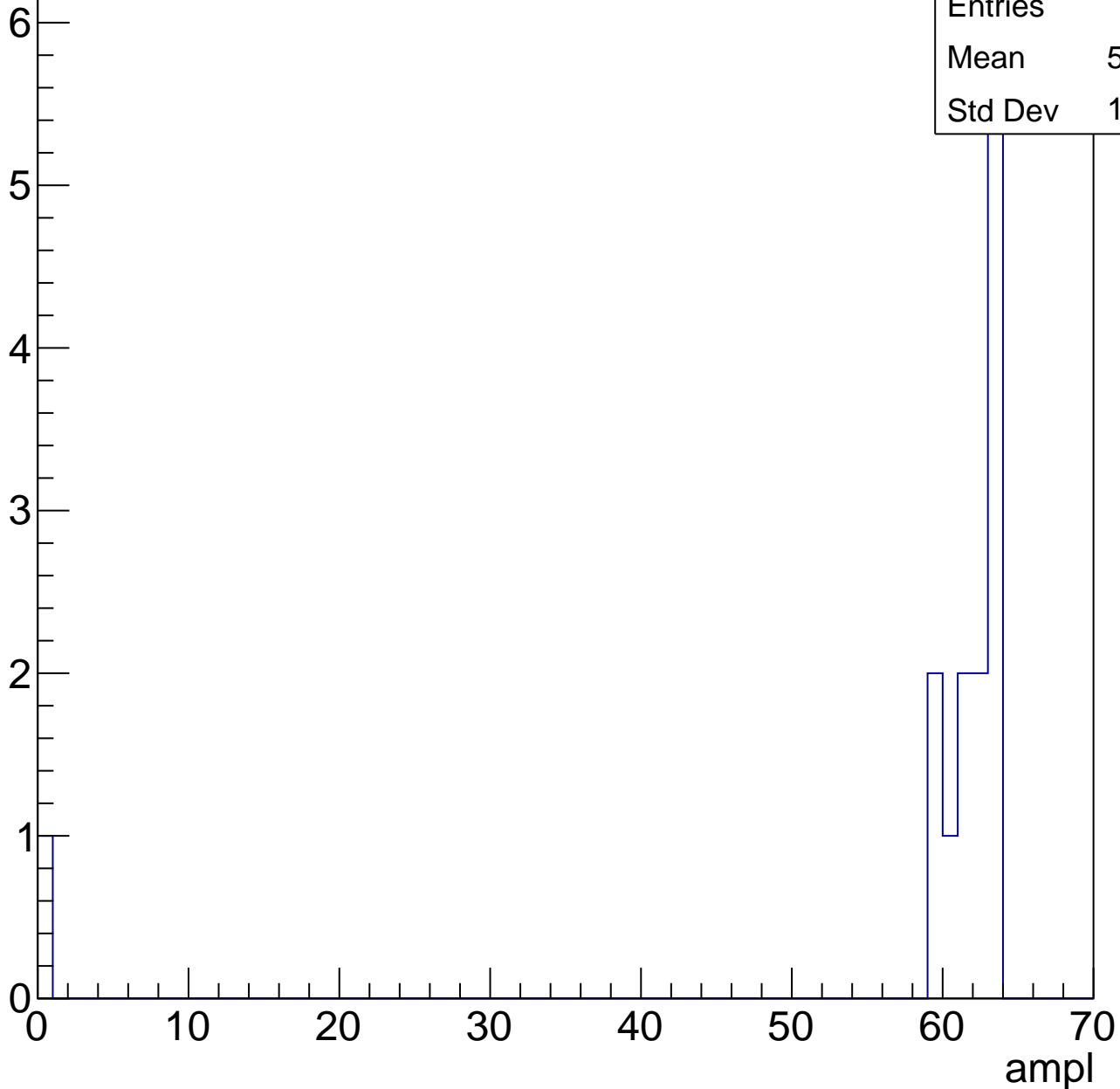


# B1L101S, U8-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	14
Mean	57.29
Std Dev	15.95





# B1L101S, U8-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch88, adc0

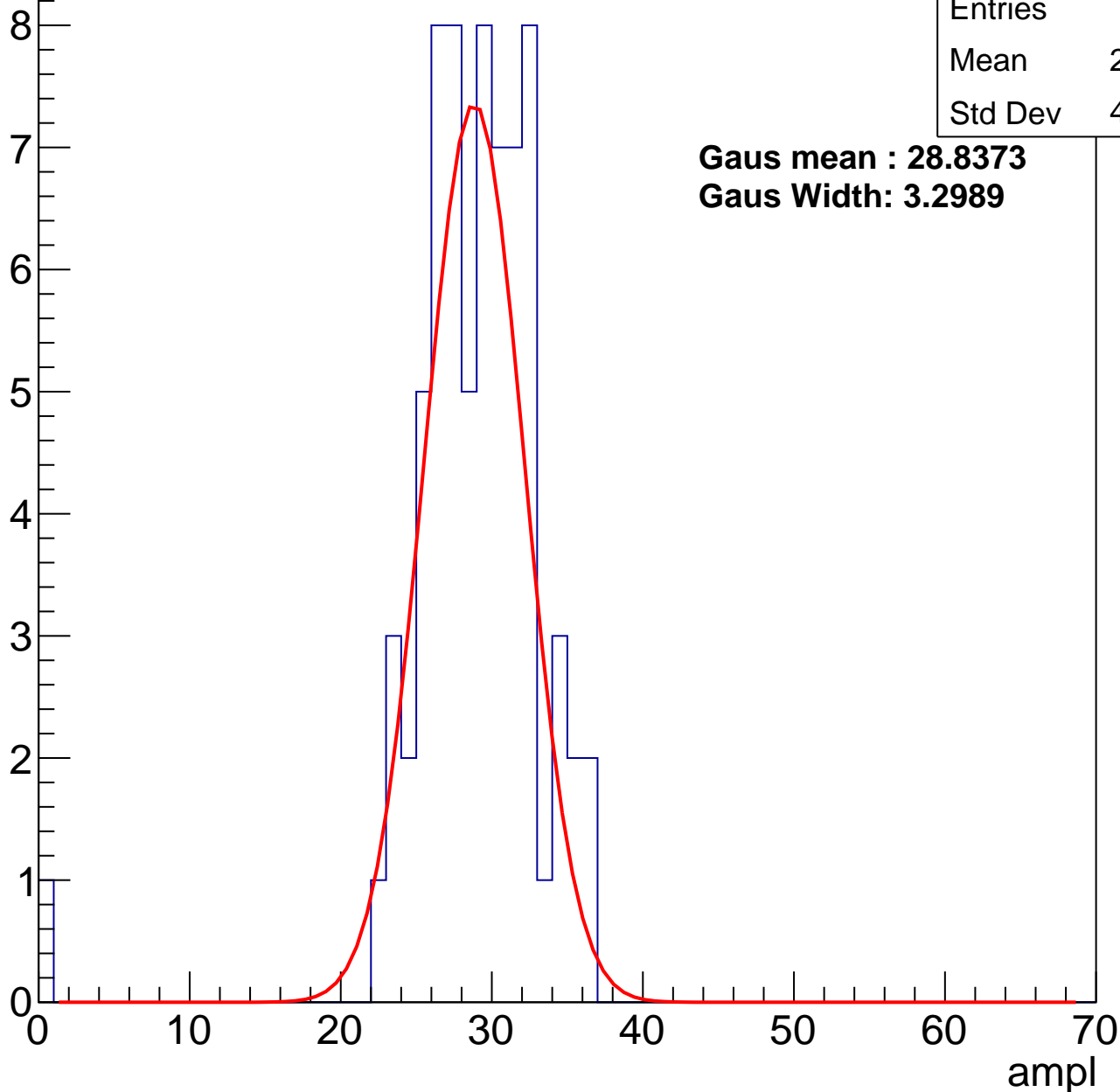
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	28.45
Std Dev	4.723

**Gaus mean : 28.8373**

**Gaus Width: 3.2989**



# B1L101S, U8-ch88, adc1

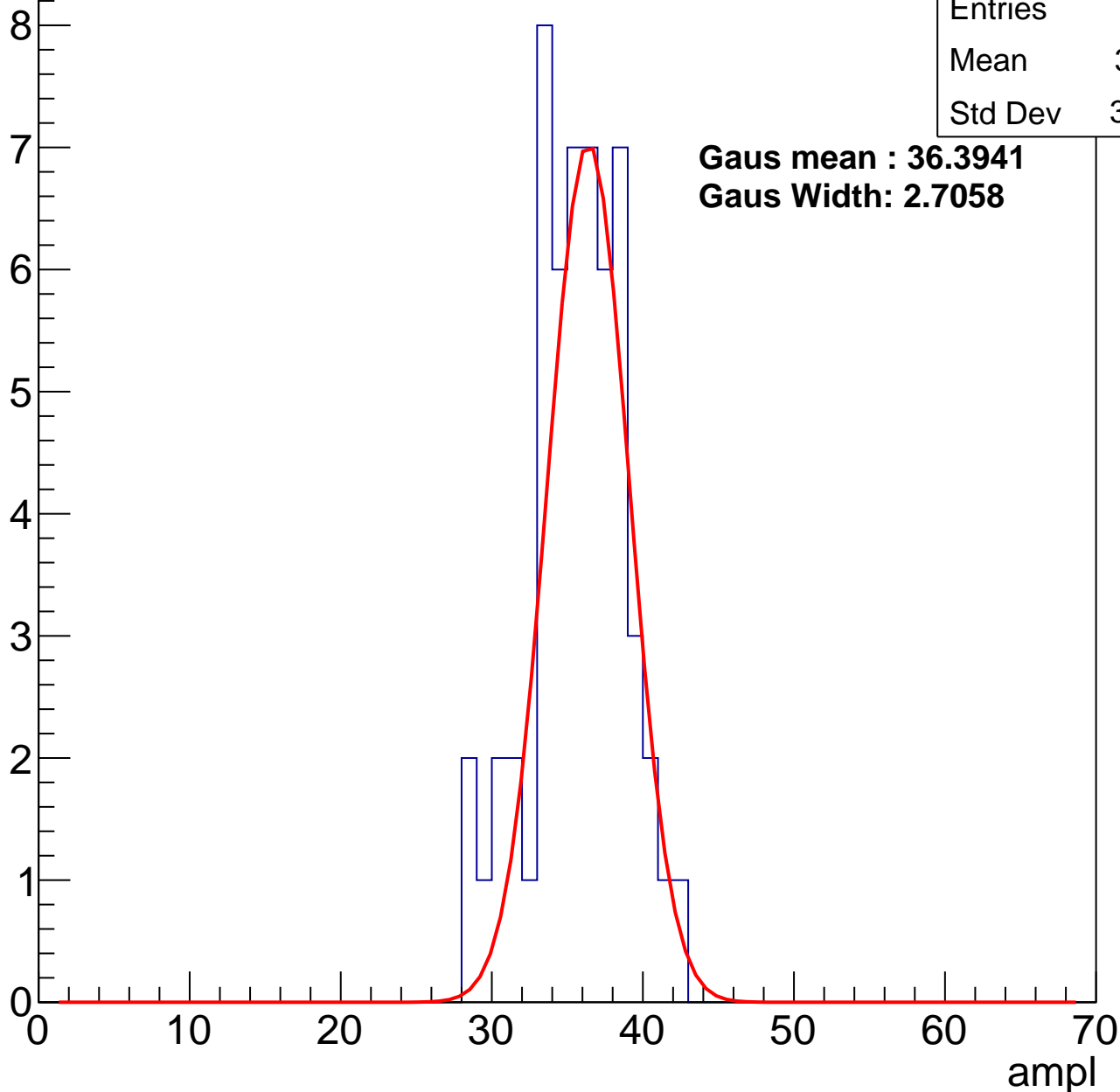
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	35.21
Std Dev	3.098

**Gaus mean : 36.3941**

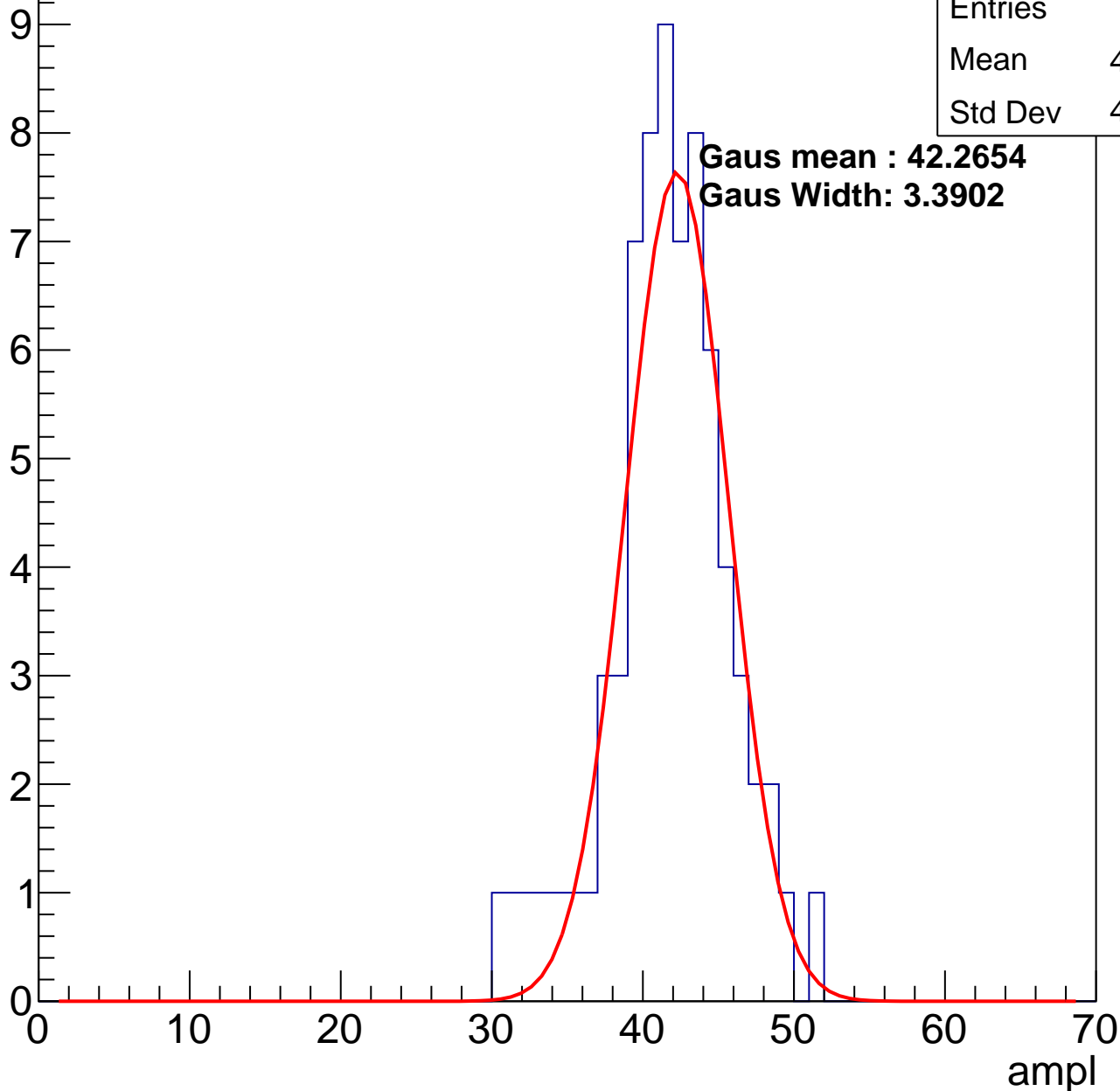
**Gaus Width: 2.7058**



# B1L101S, U8-ch88, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

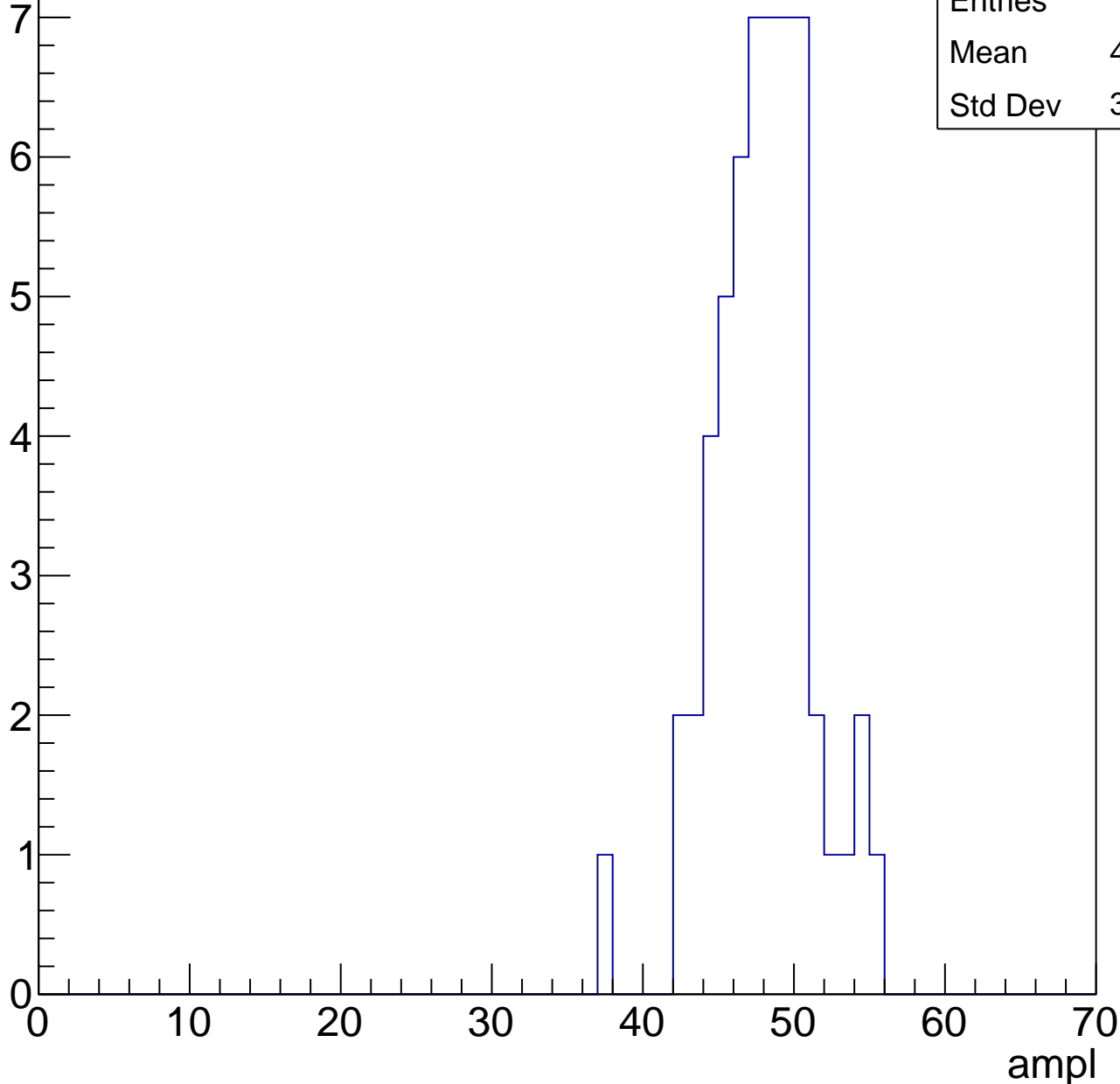


Entries	71
Mean	41.24
Std Dev	4.023

# B1L101S, U8-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



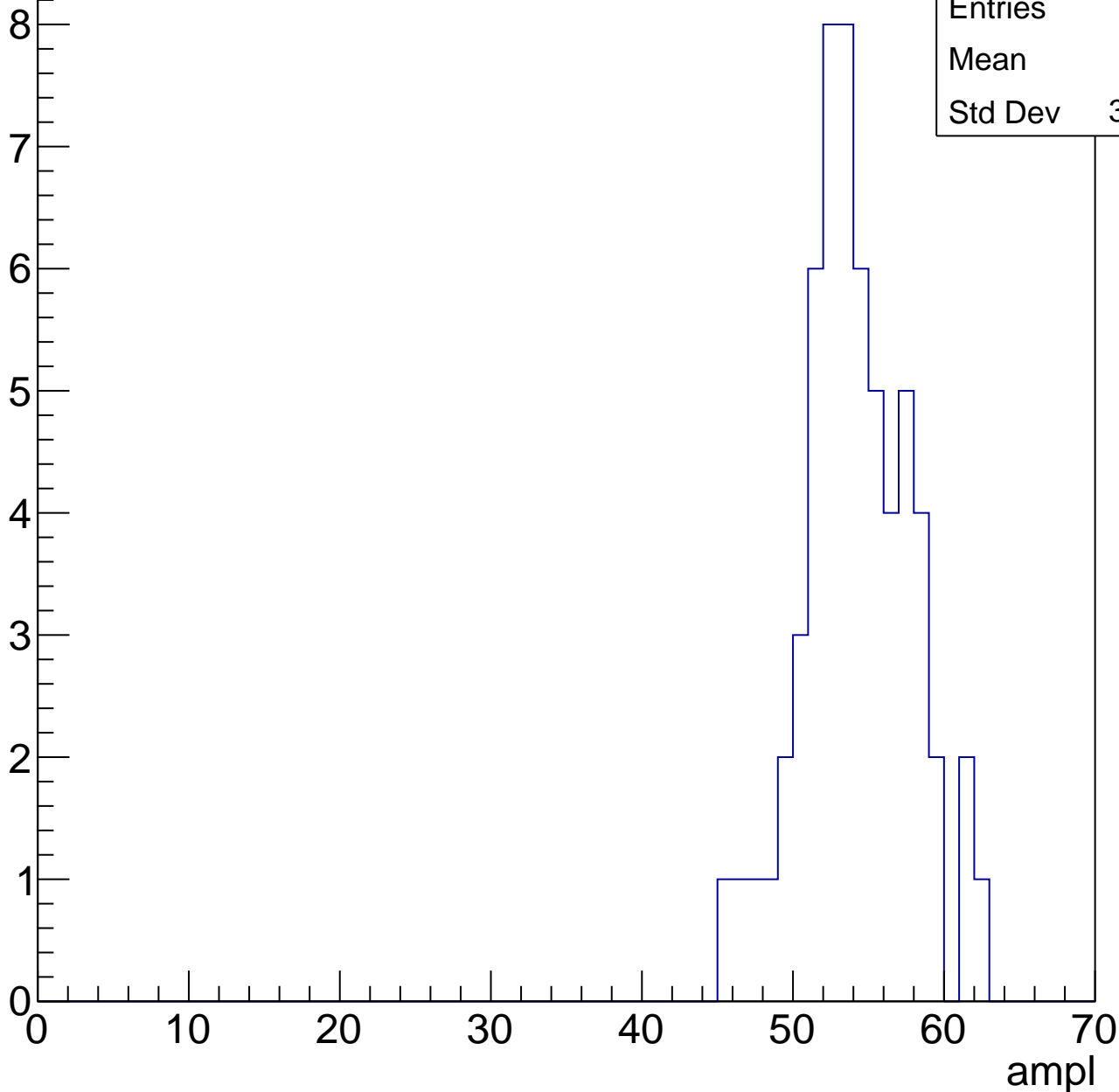
Entries	55
Mean	47.49
Std Dev	3.258

# B1L101S, U8-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	53.7
Std Dev	3.556

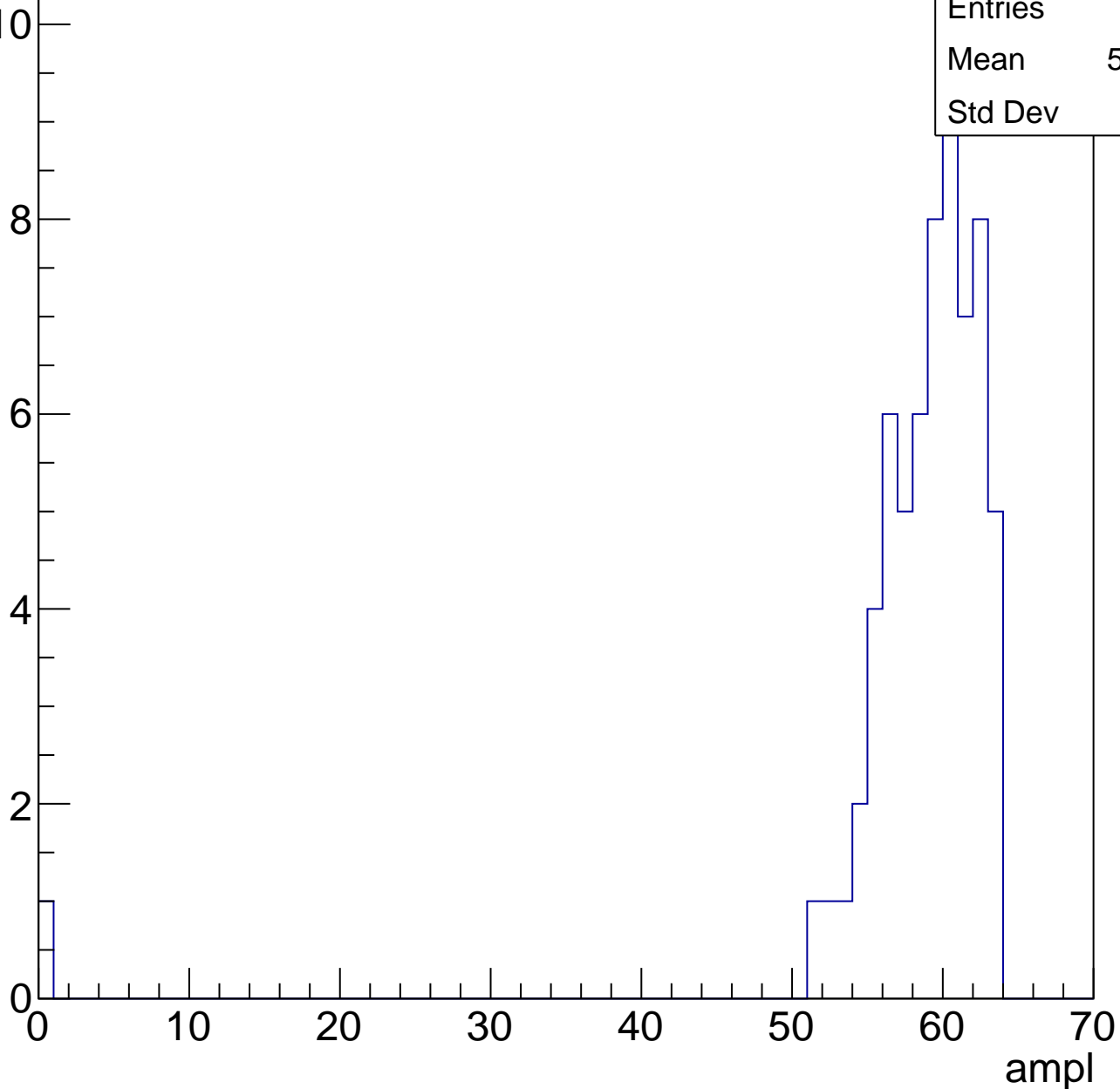


# B1L101S, U8-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	57.89
Std Dev	7.78

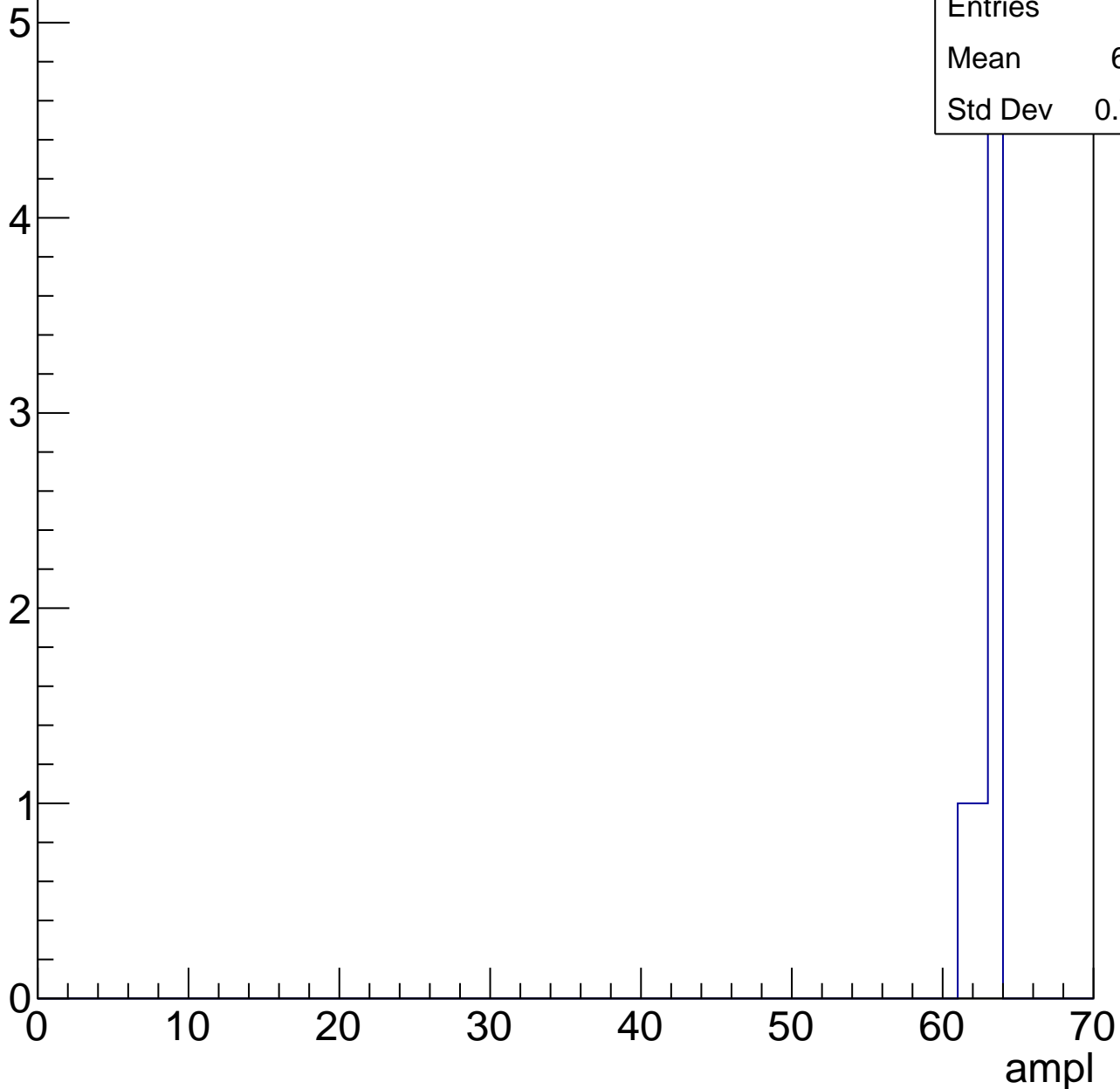


# B1L101S, U8-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	7
Mean	62.57
Std Dev	0.7284





# B1L101S, U8-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U8-ch89, adc0

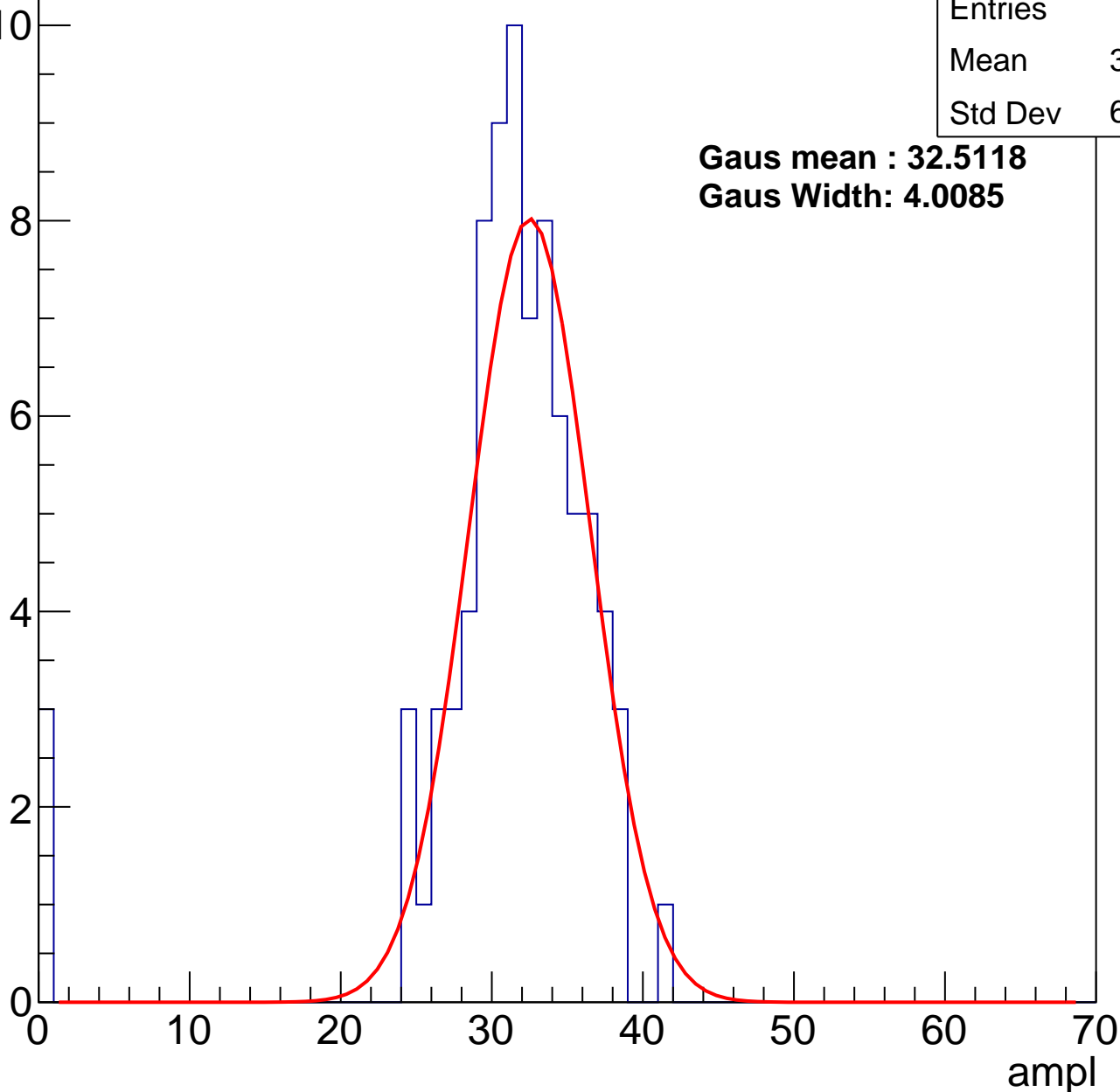
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	83
Mean	30.48
Std Dev	6.883

**Gaus mean : 32.5118**

**Gaus Width: 4.0085**



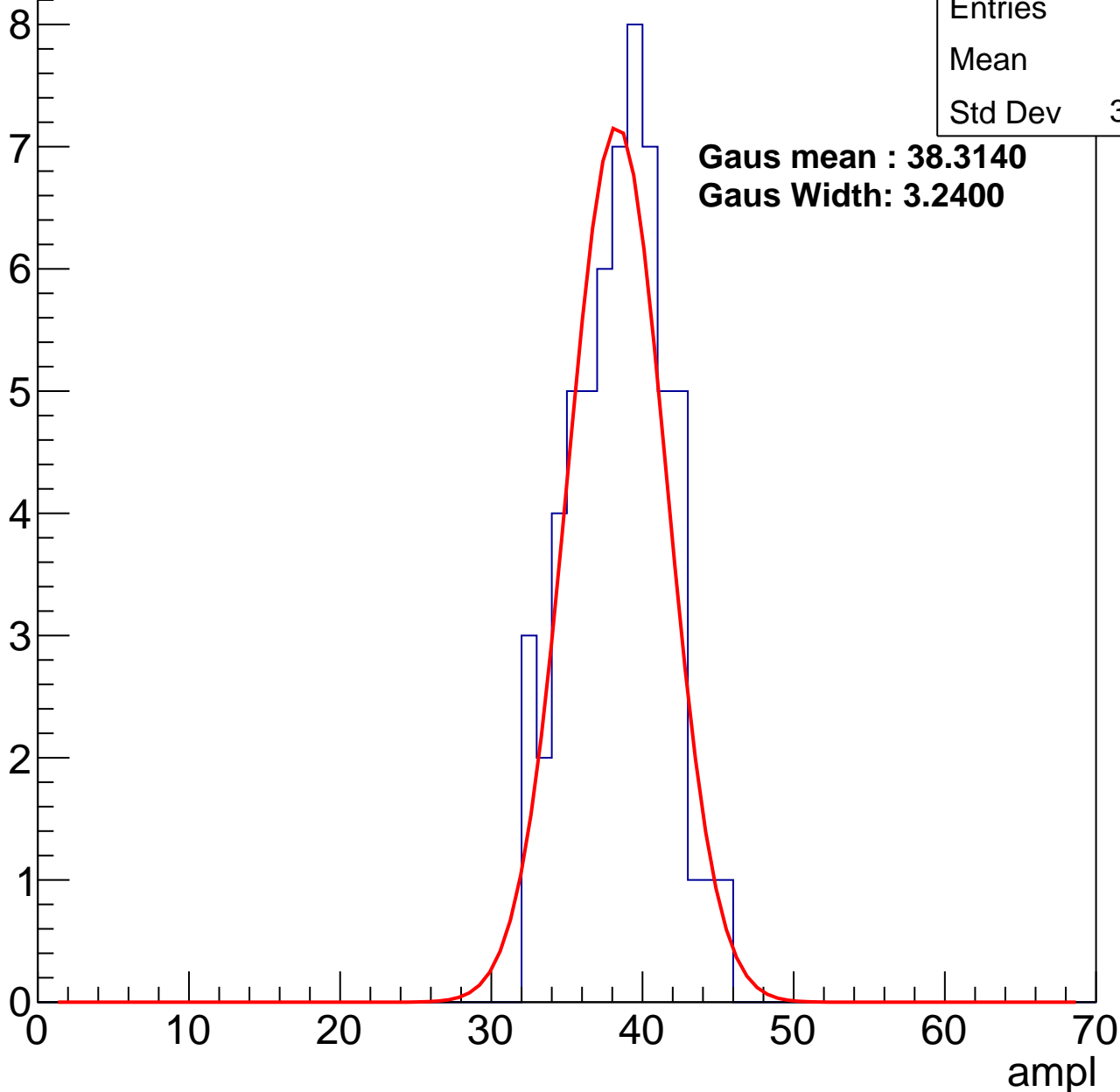
# B1L101S, U8-ch89, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	38
Std Dev	3.066

**Gaus mean : 38.3140**  
**Gaus Width: 3.2400**



# B1L101S, U8-ch89, adc2

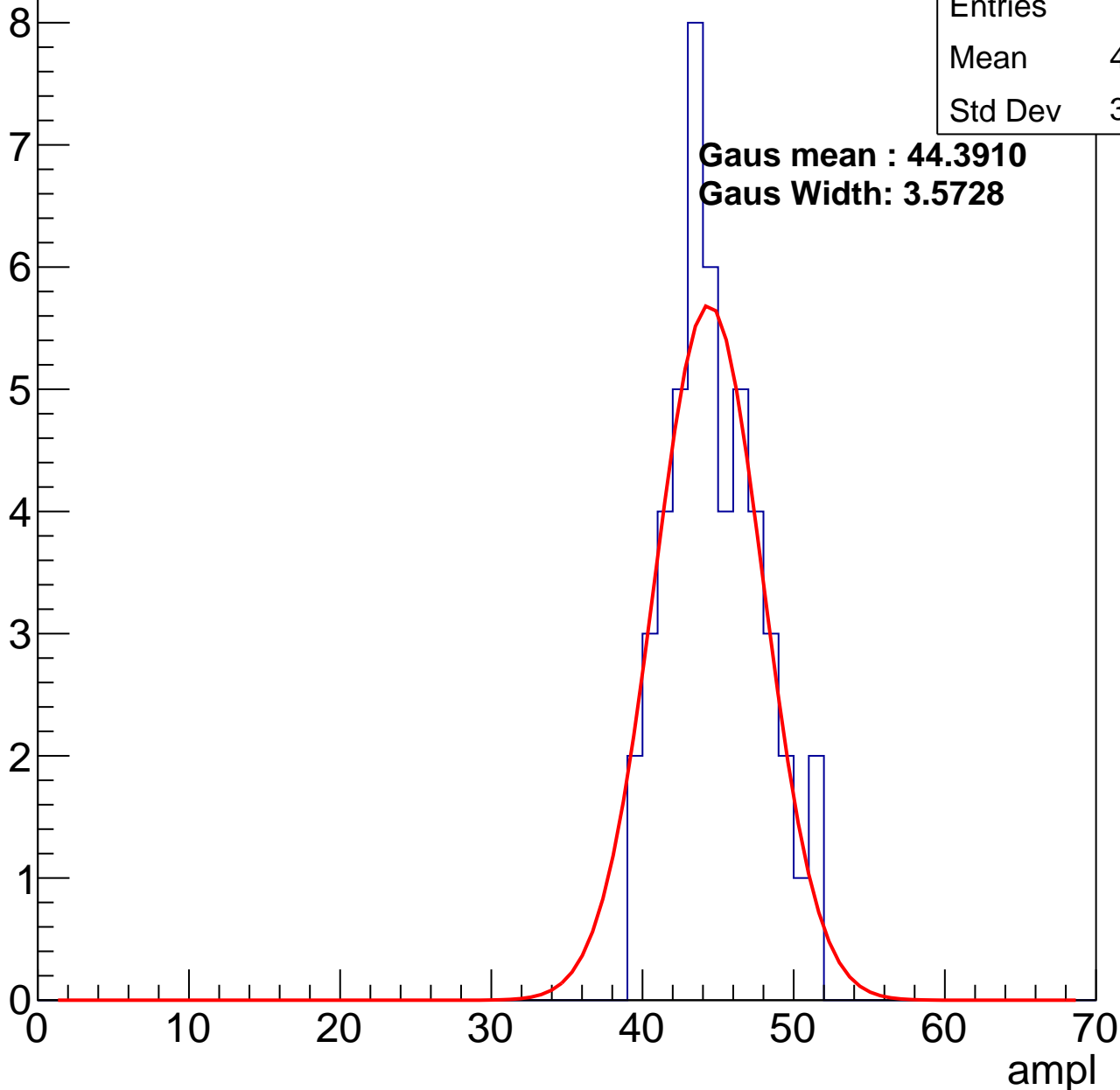
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	44.33
Std Dev	3.026

**Gaus mean : 44.3910**

**Gaus Width: 3.5728**

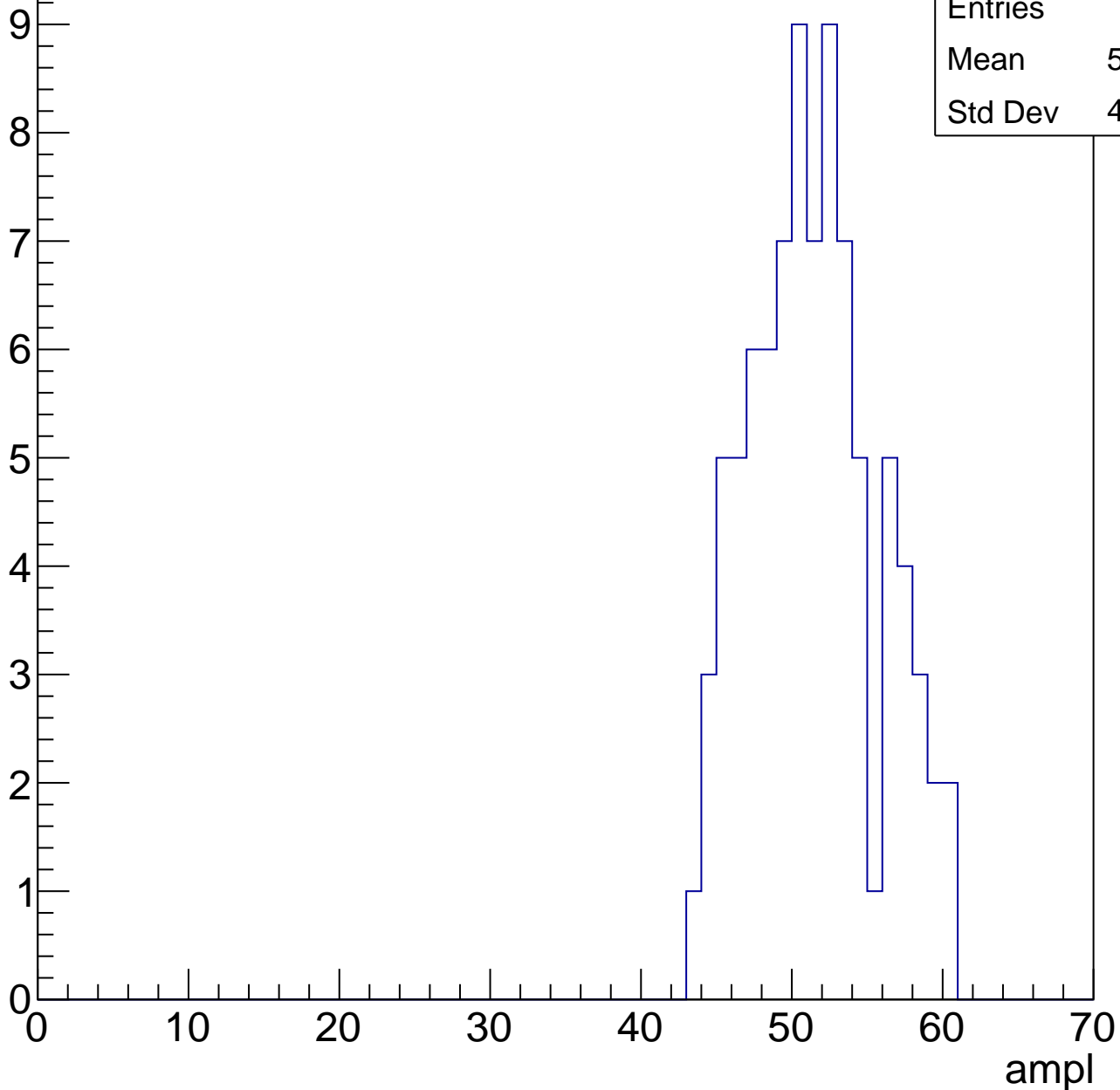


# B1L101S, U8-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

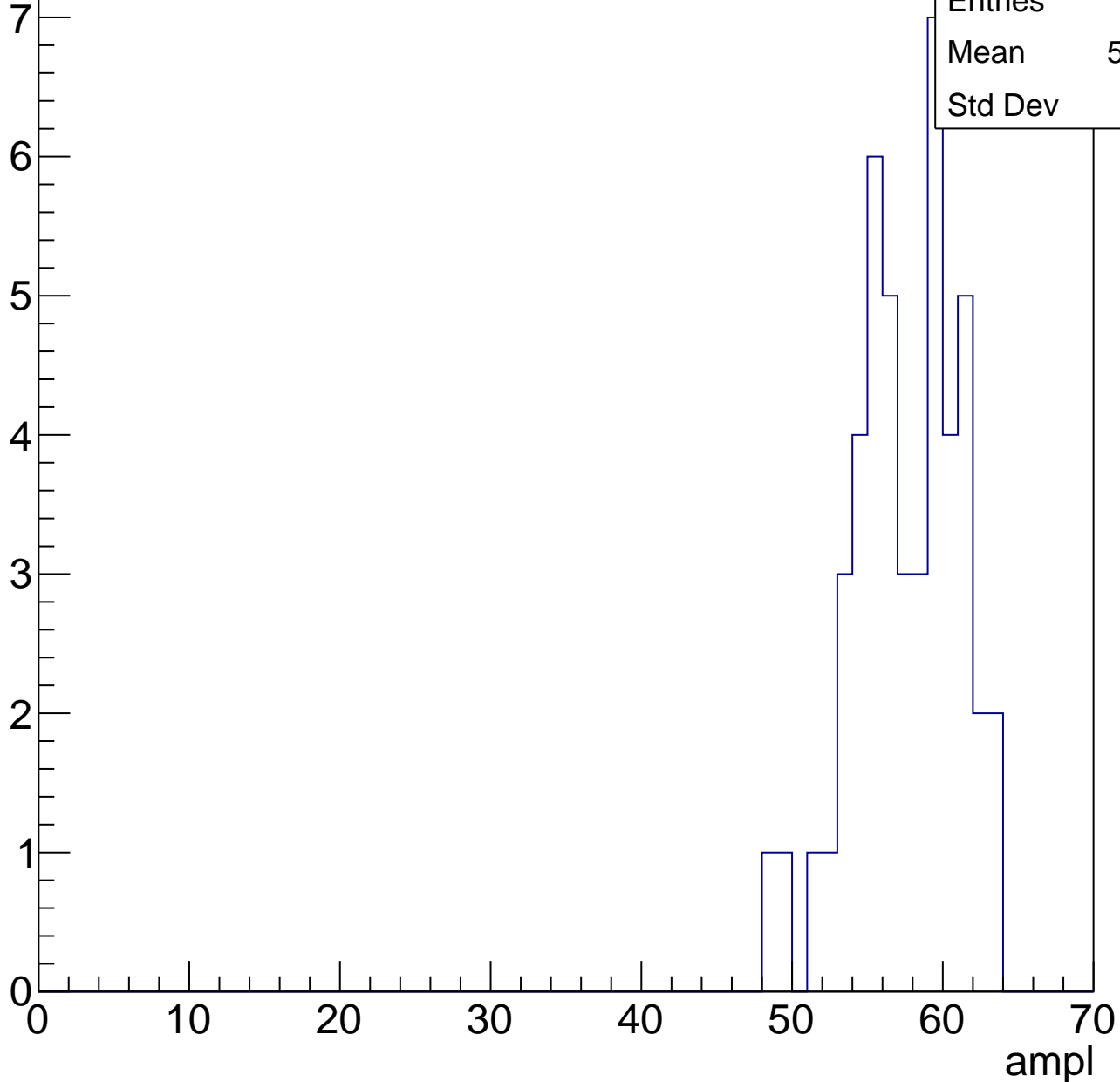
Entries	87
Mean	50.97
Std Dev	4.162



# B1L101S, U8-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

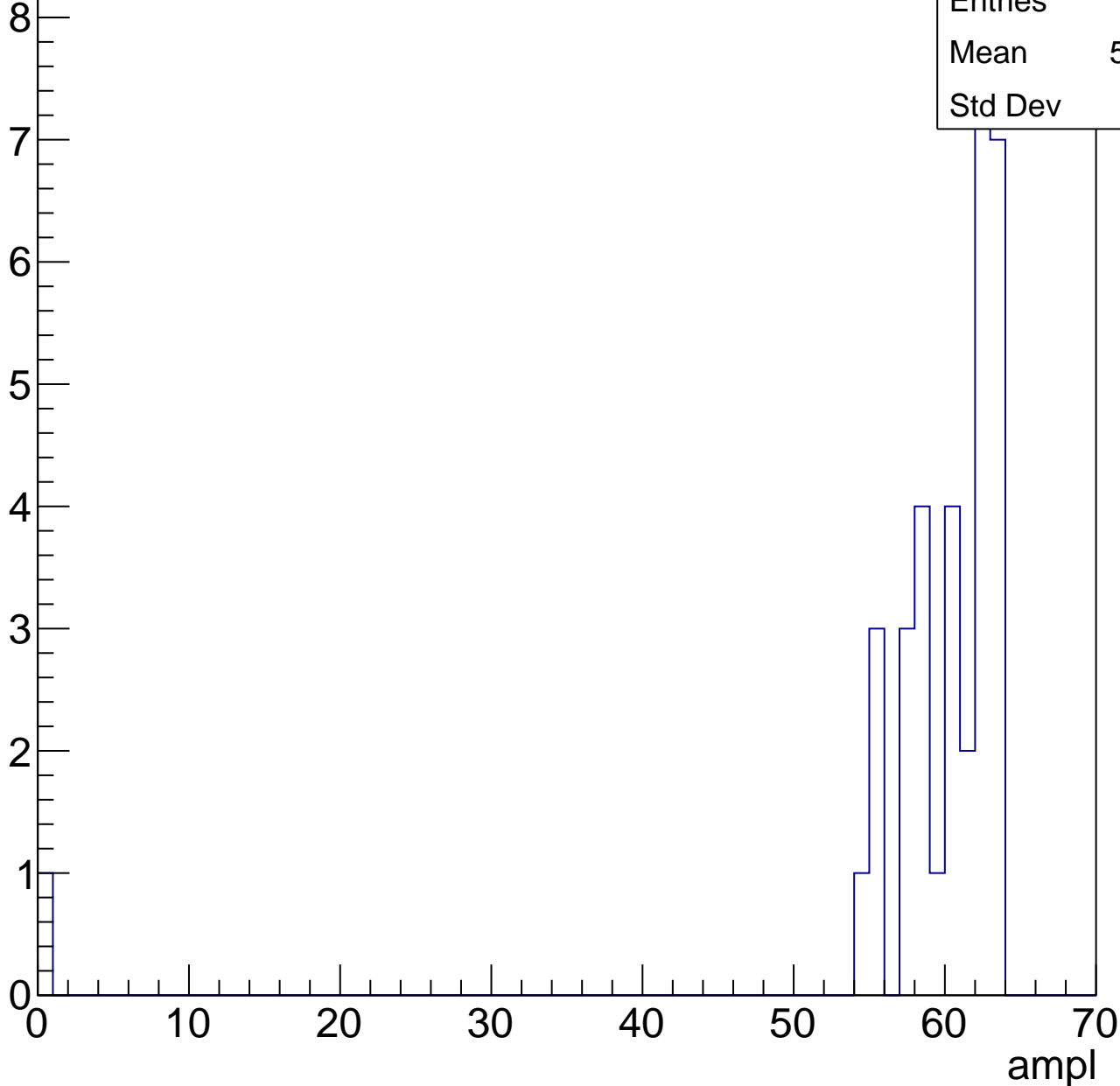


# B1L101S, U8-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

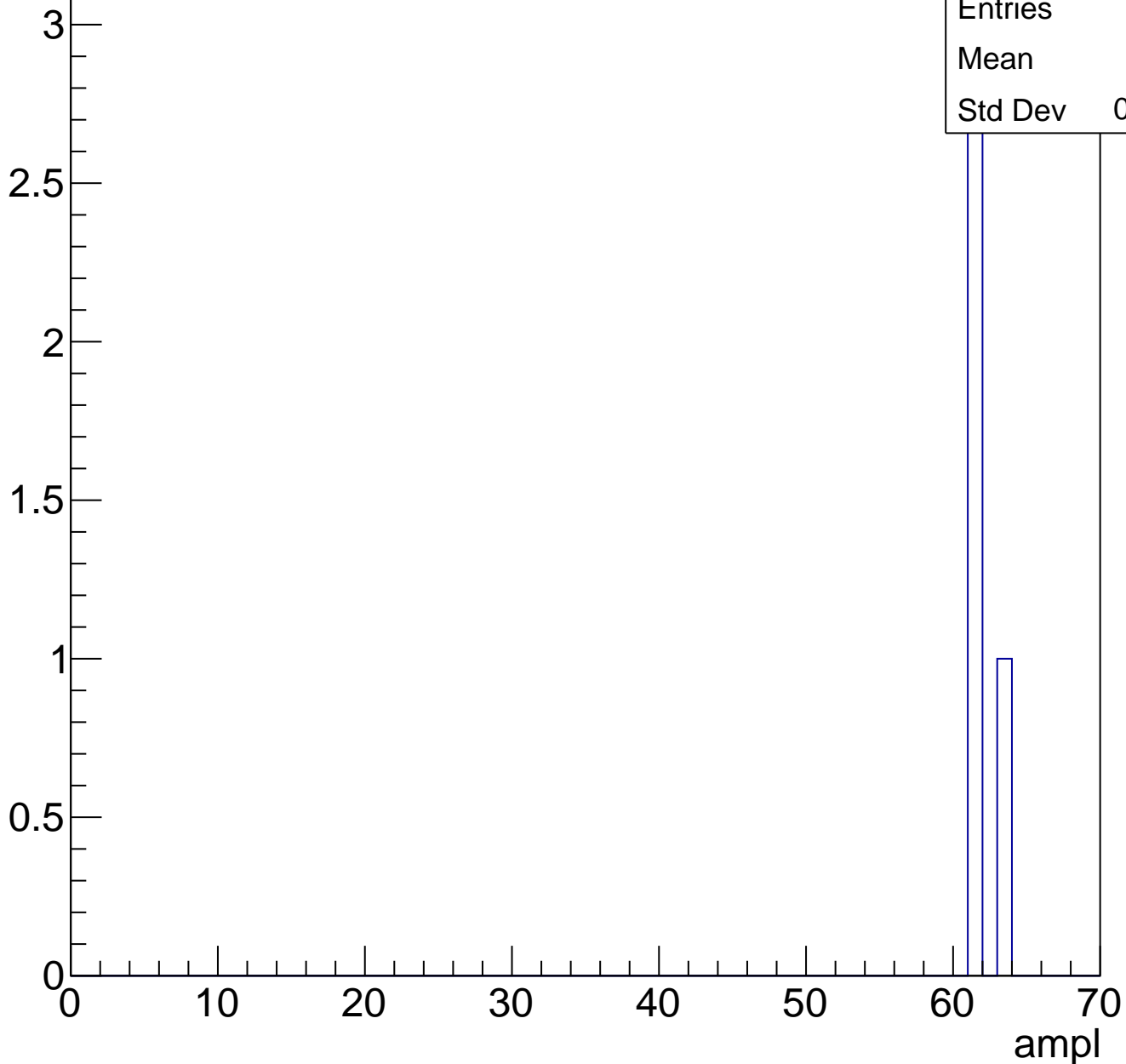
Entries	34
Mean	58.24
Std Dev	10.5



# B1L101S, U8-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U8-ch90, adc0

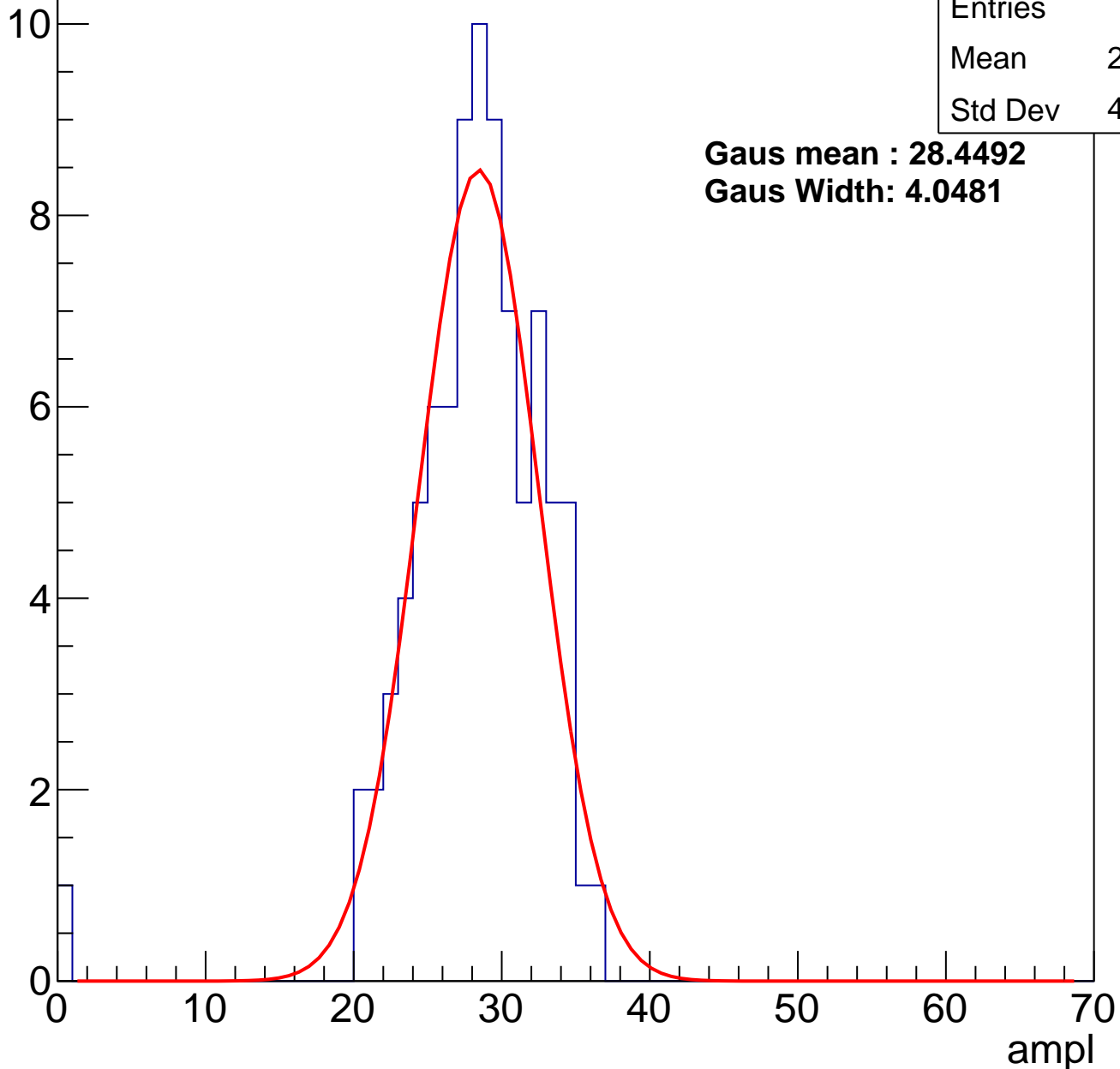
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	88
Mean	27.78
Std Dev	4.759

**Gaus mean : 28.4492**

**Gaus Width: 4.0481**

Entry



# B1L101S, U8-ch90, adc1

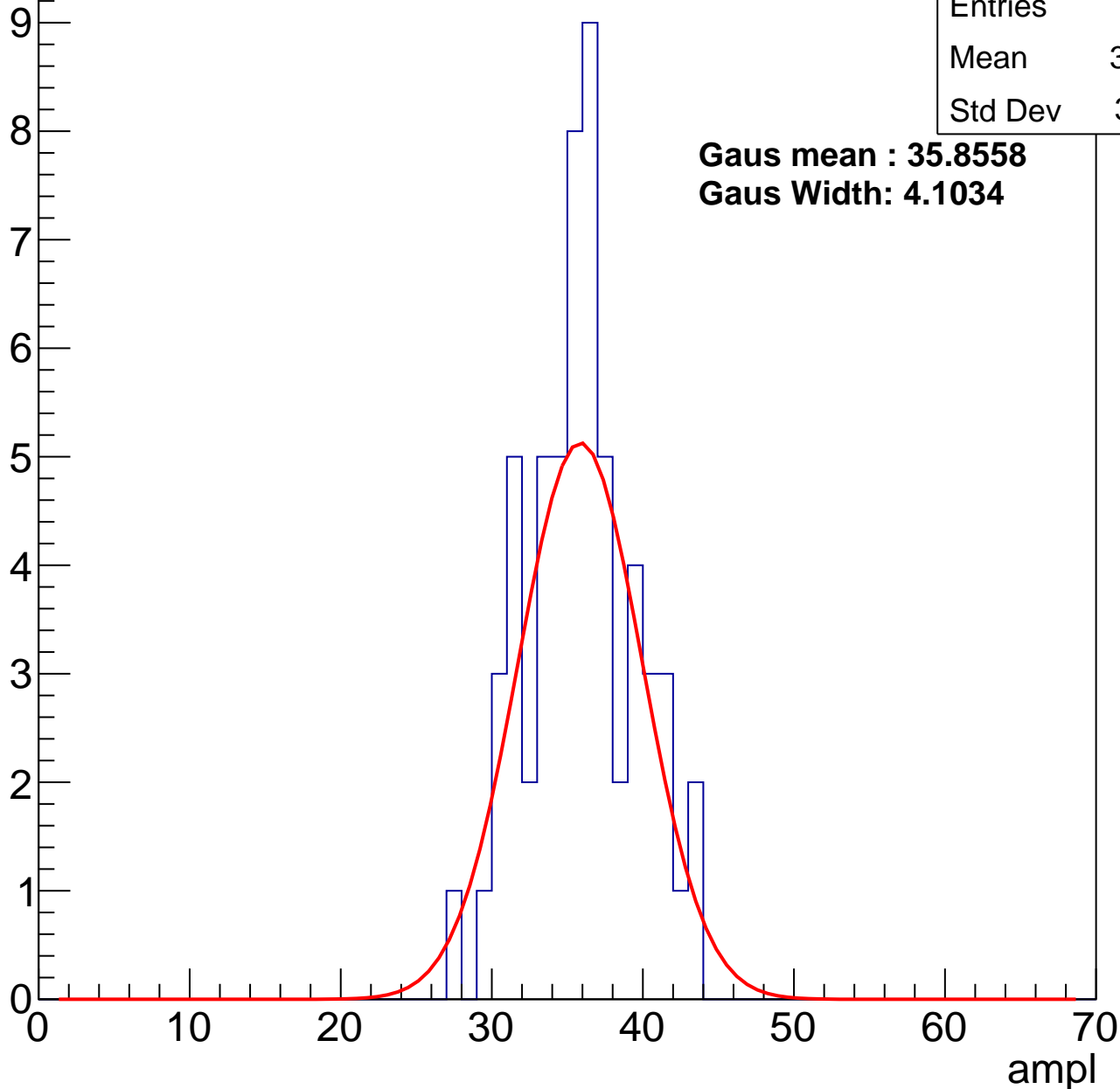
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	35.46
Std Dev	3.581

**Gaus mean : 35.8558**

**Gaus Width: 4.1034**



# B1L101S, U8-ch90, adc2

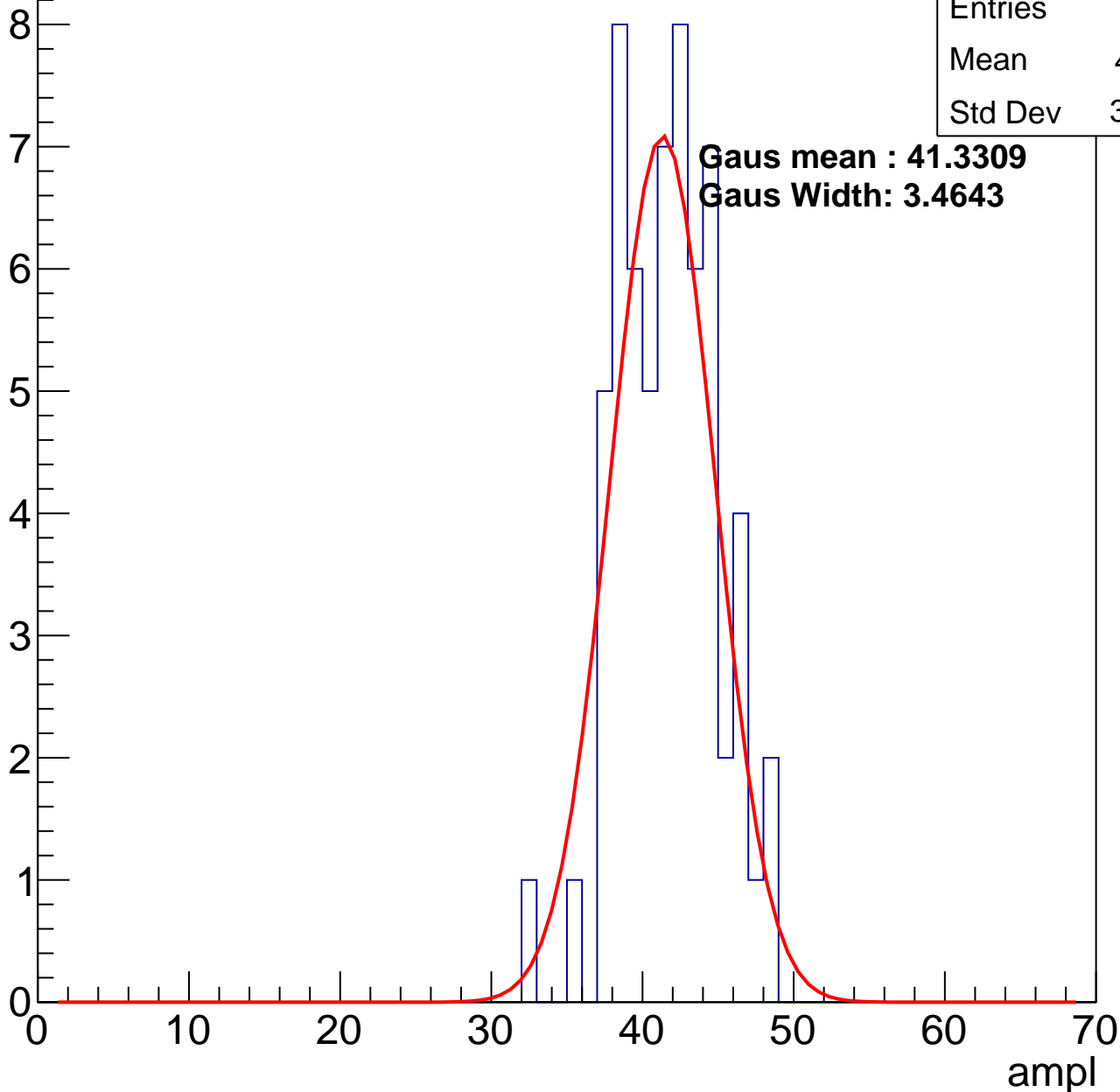
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	41.21
Std Dev	3.228

**Gaus mean : 41.3309**

**Gaus Width: 3.4643**

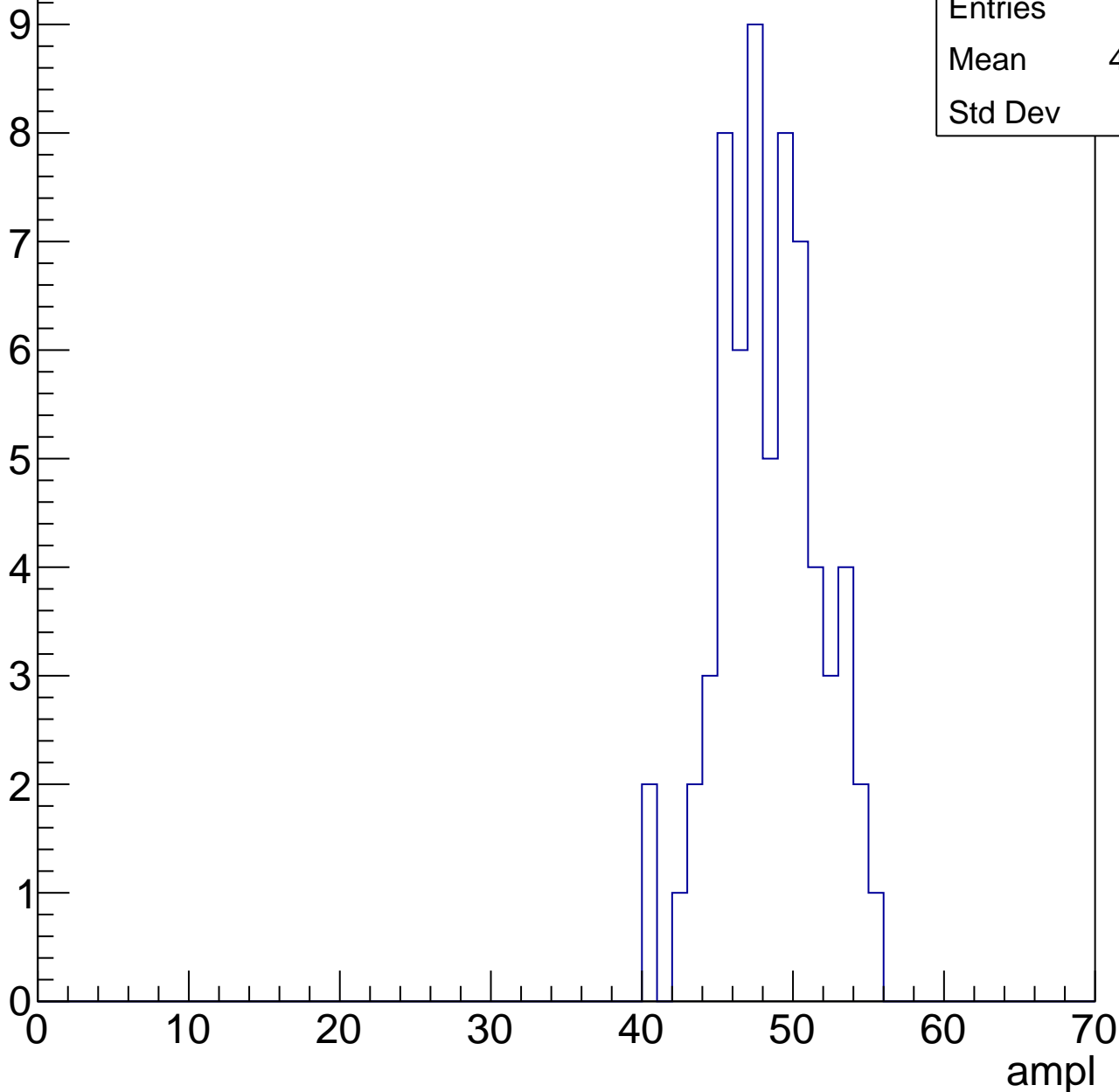


# B1L101S, U8-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	47.94
Std Dev	3.3

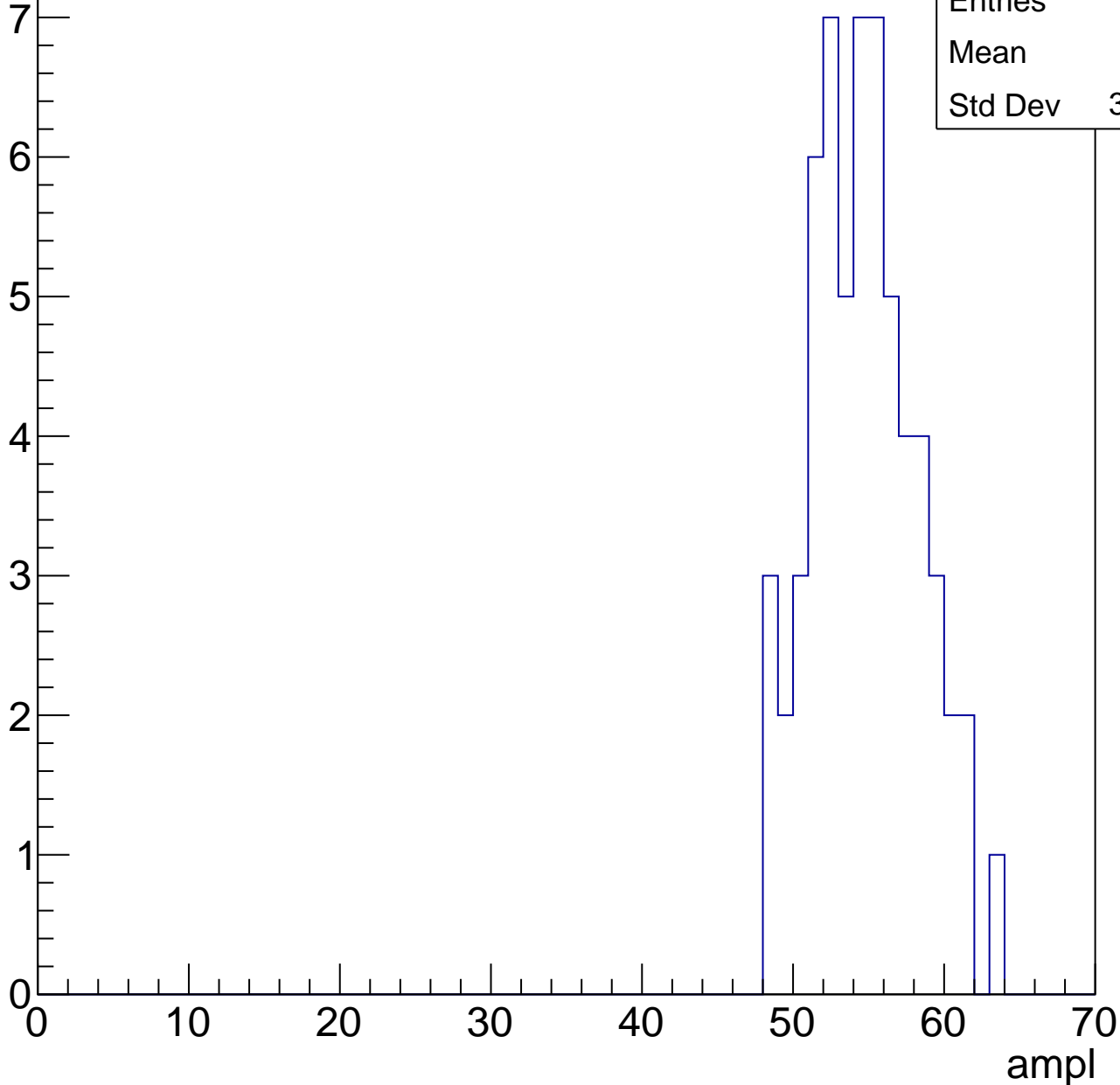


# B1L101S, U8-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	54.3
Std Dev	3.485

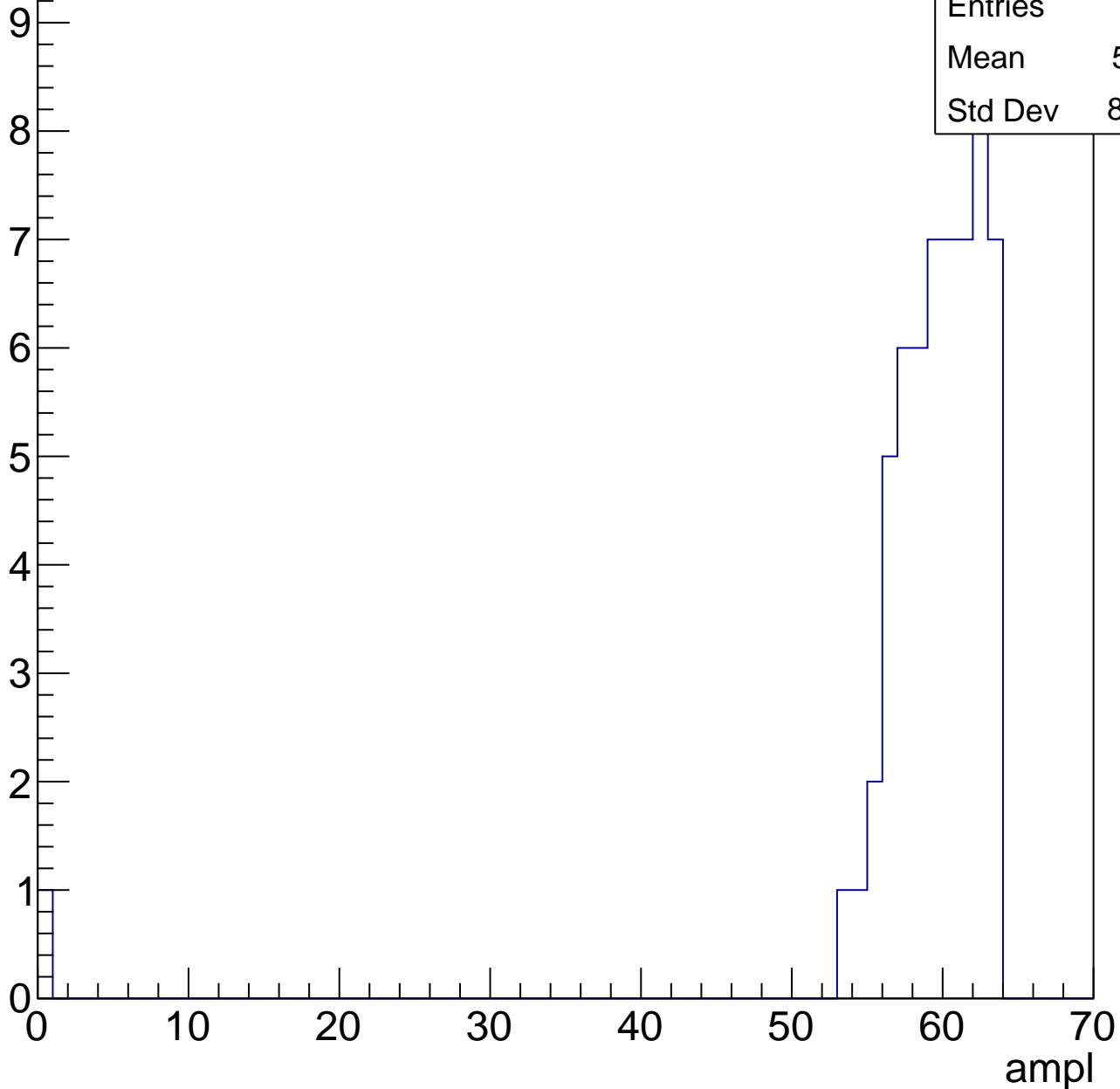


# B1L101S, U8-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	58.41
Std Dev	8.085



# B1L101S, U8-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U8-ch91, adc0

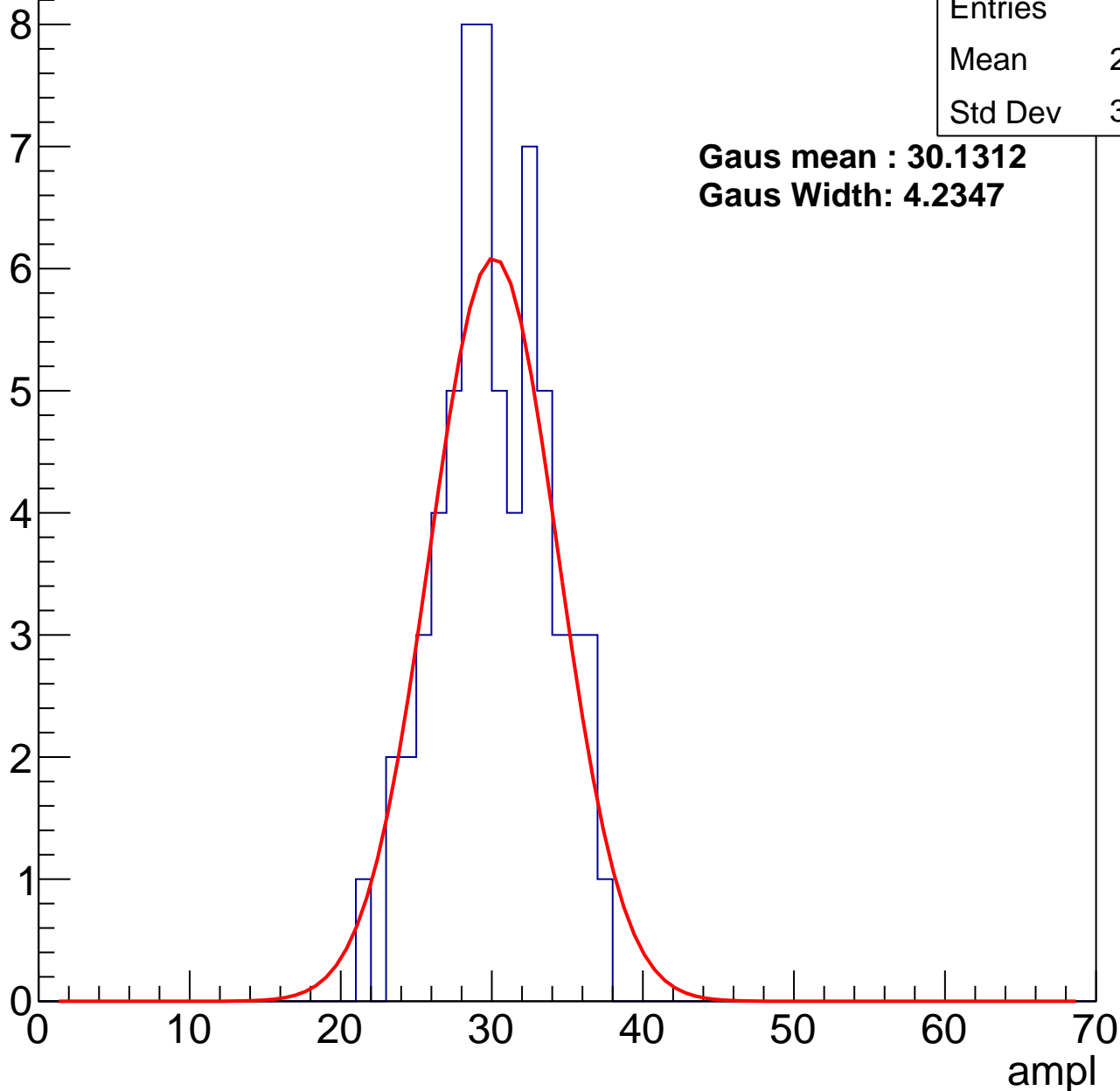
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	29.69
Std Dev	3.592

**Gaus mean : 30.1312**

**Gaus Width: 4.2347**



# B1L101S, U8-ch91, adc1

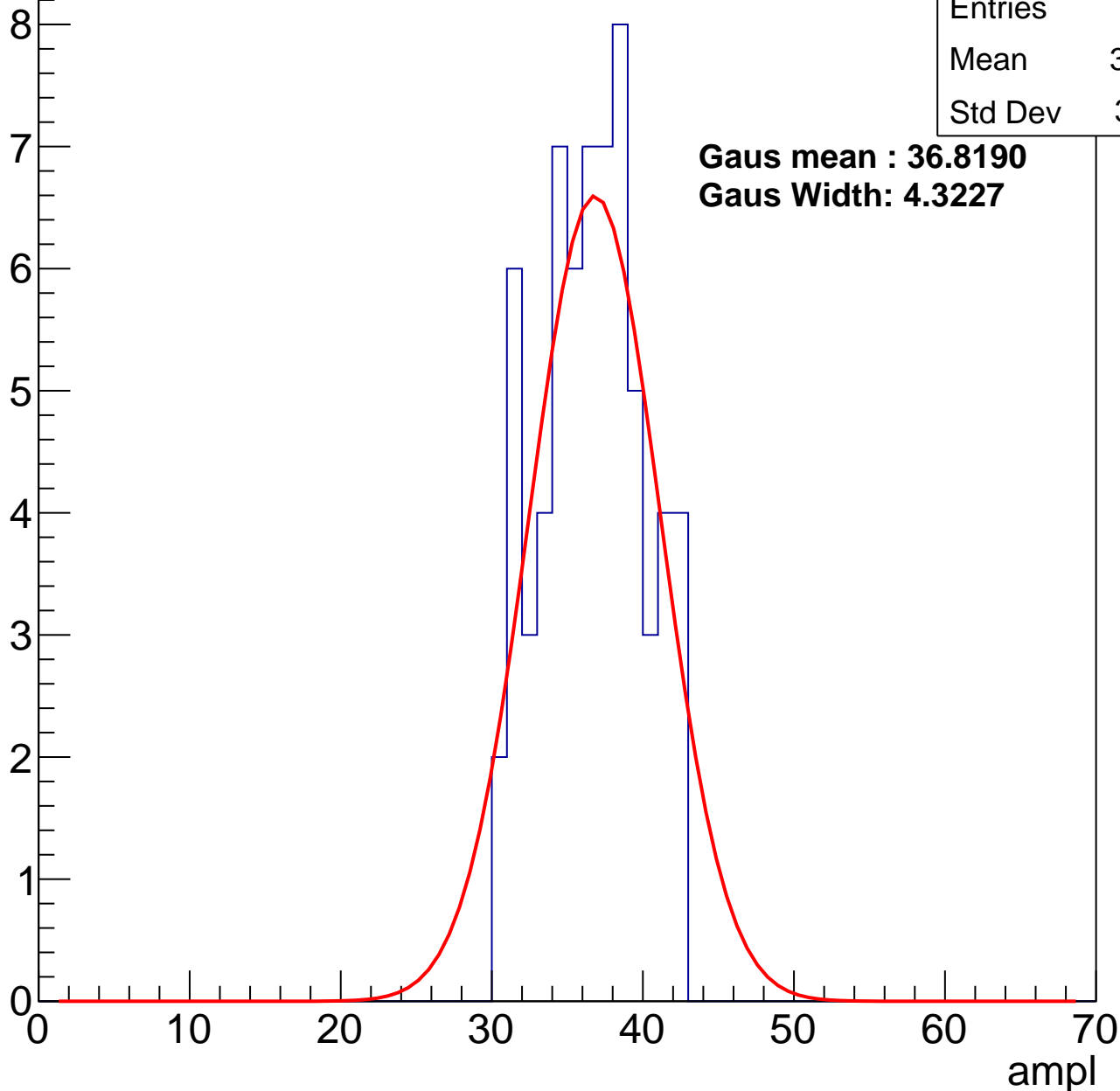
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	36.12
Std Dev	3.291

**Gaus mean : 36.8190**

**Gaus Width: 4.3227**



# B1L101S, U8-ch91, adc2

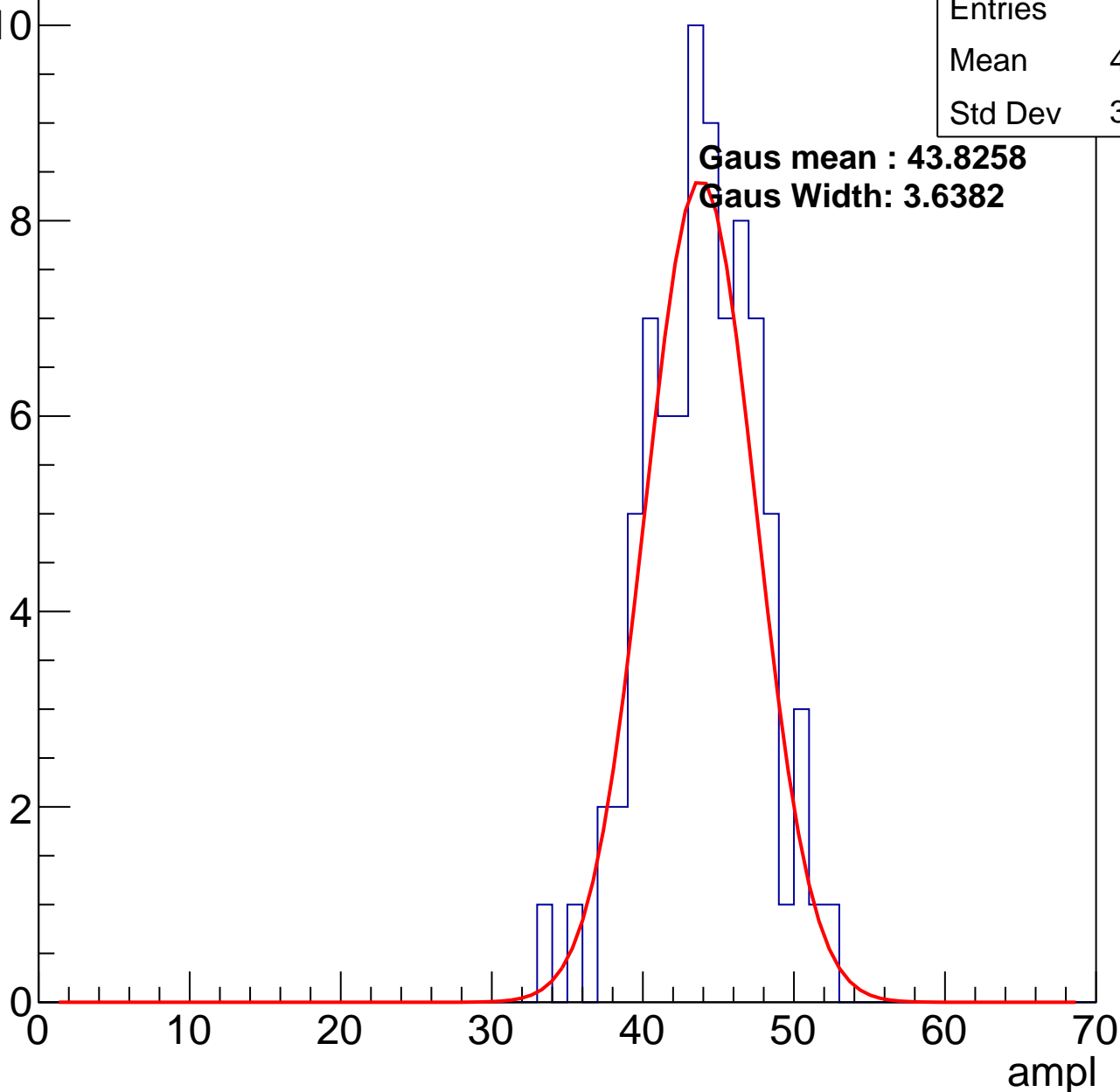
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	43.55
Std Dev	3.676

**Gaus mean : 43.8258**

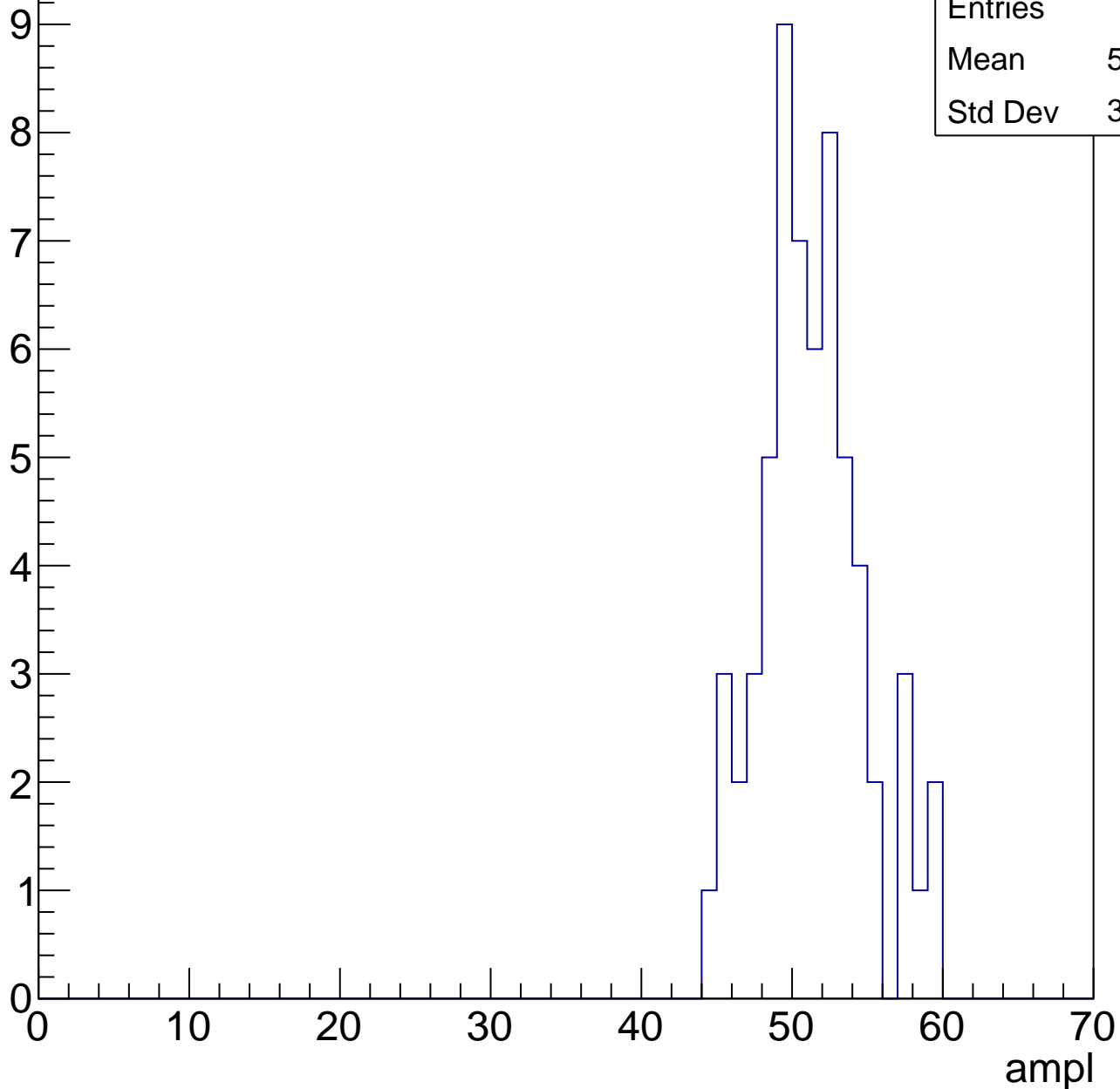
**Gaus Width: 3.6382**



# B1L101S, U8-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

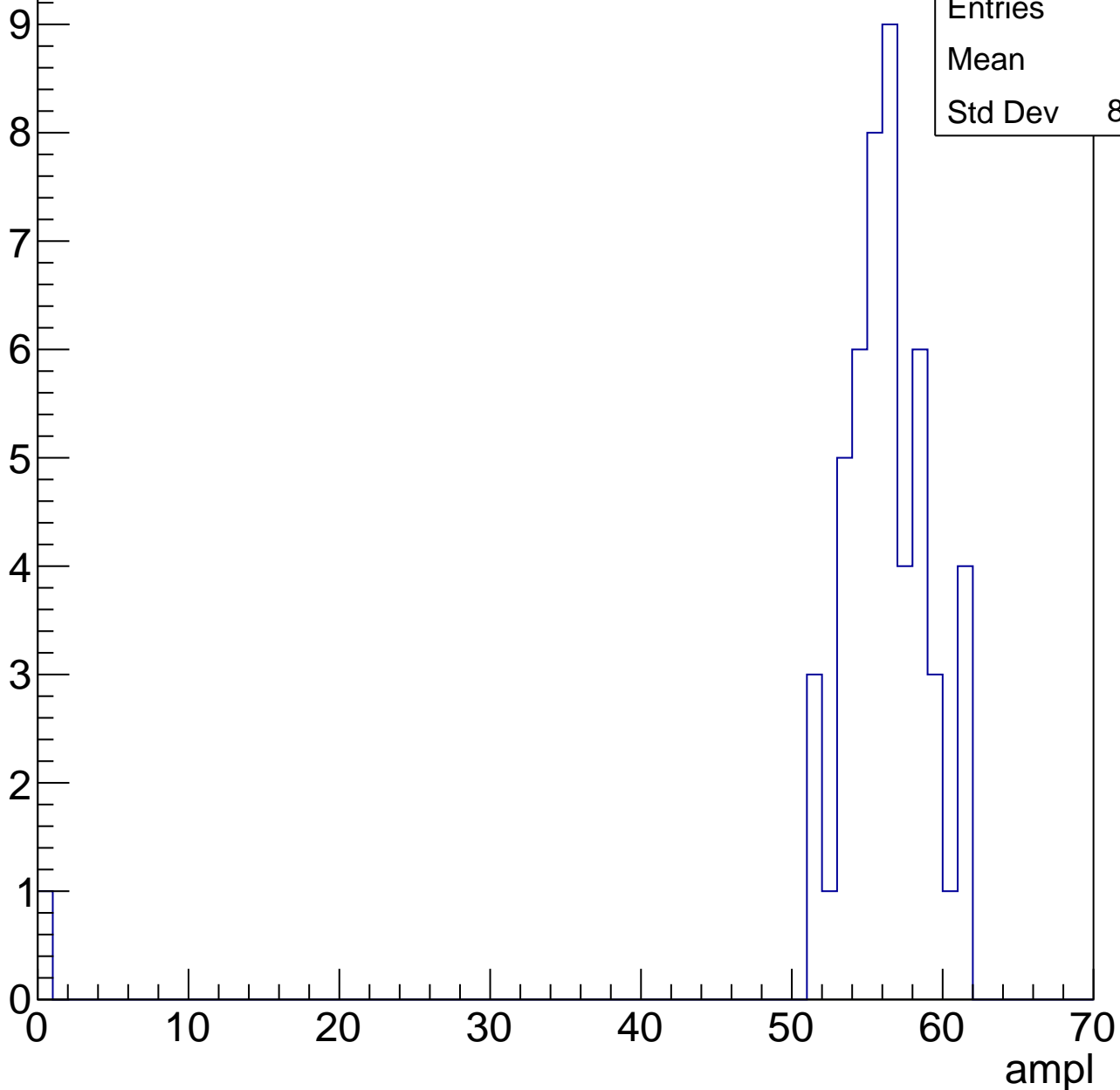


# B1L101S, U8-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	54.8
Std Dev	8.167



# B1L101S, U8-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

Entries	36
Mean	60.31
Std Dev	1.969

ampl

10

20

30

40

50

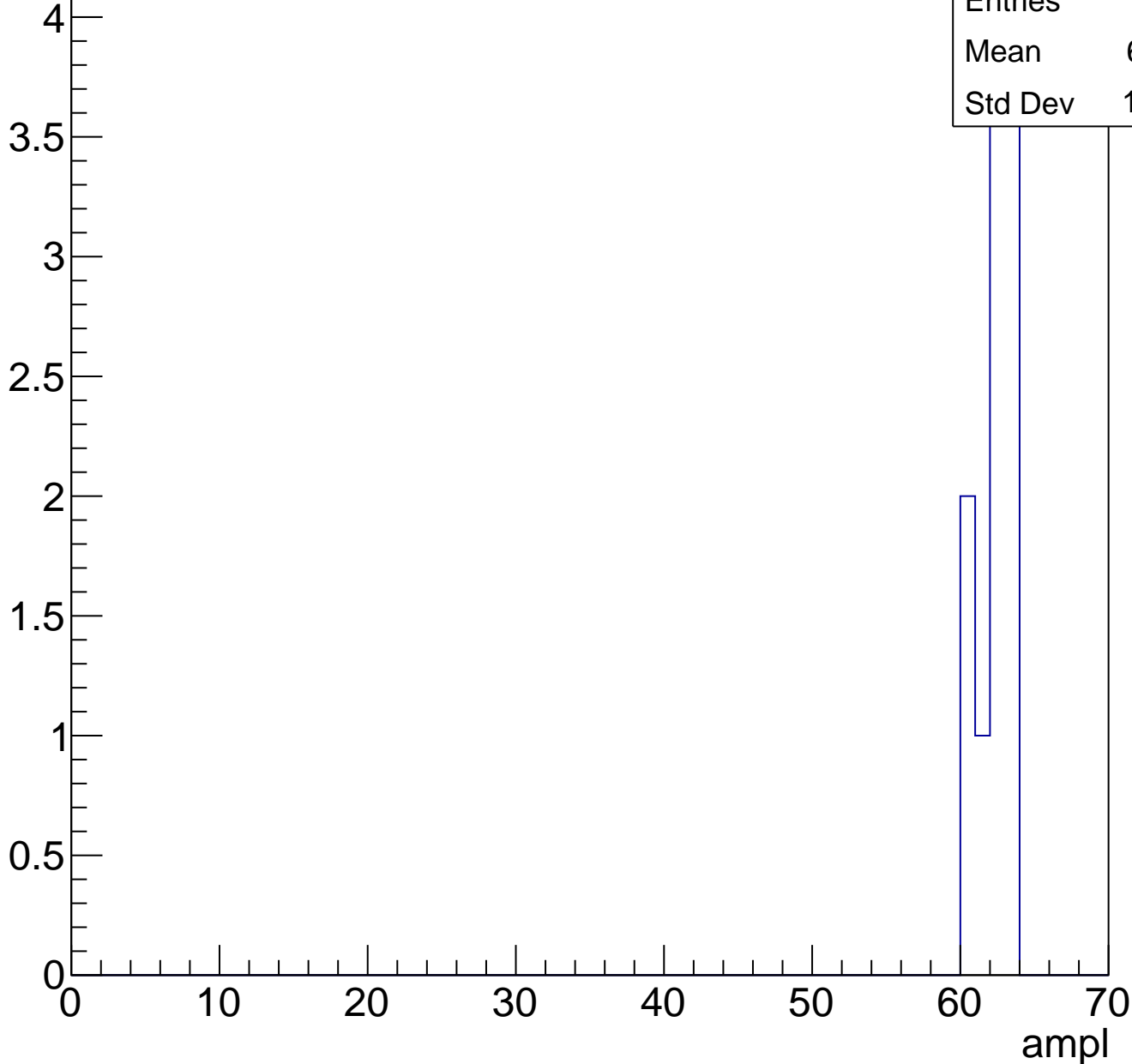
60

70

# B1L101S, U8-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch92, adc0

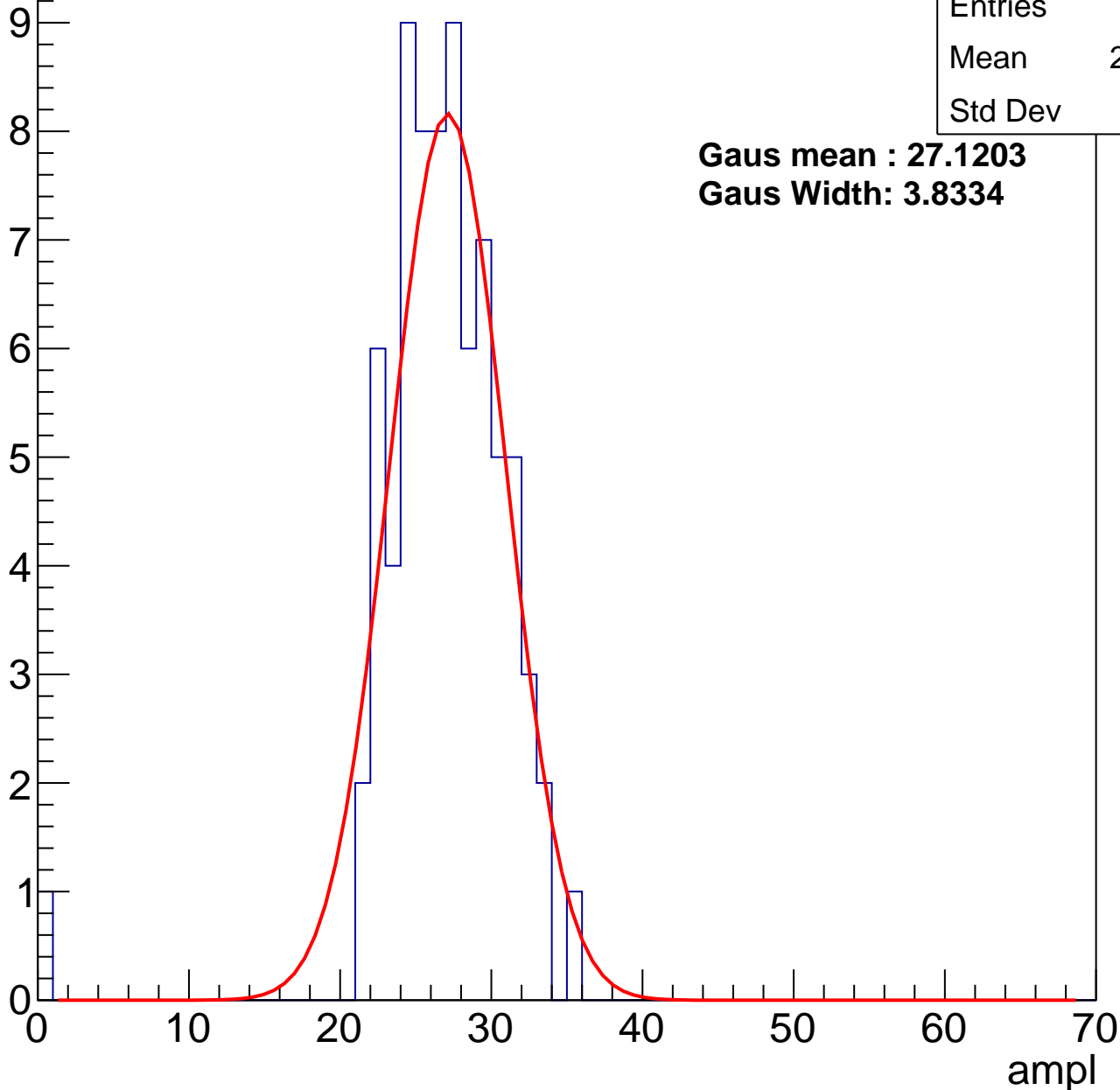
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	26.39
Std Dev	4.41

**Gaus mean : 27.1203**

**Gaus Width: 3.8334**



# B1L101S, U8-ch92, adc1

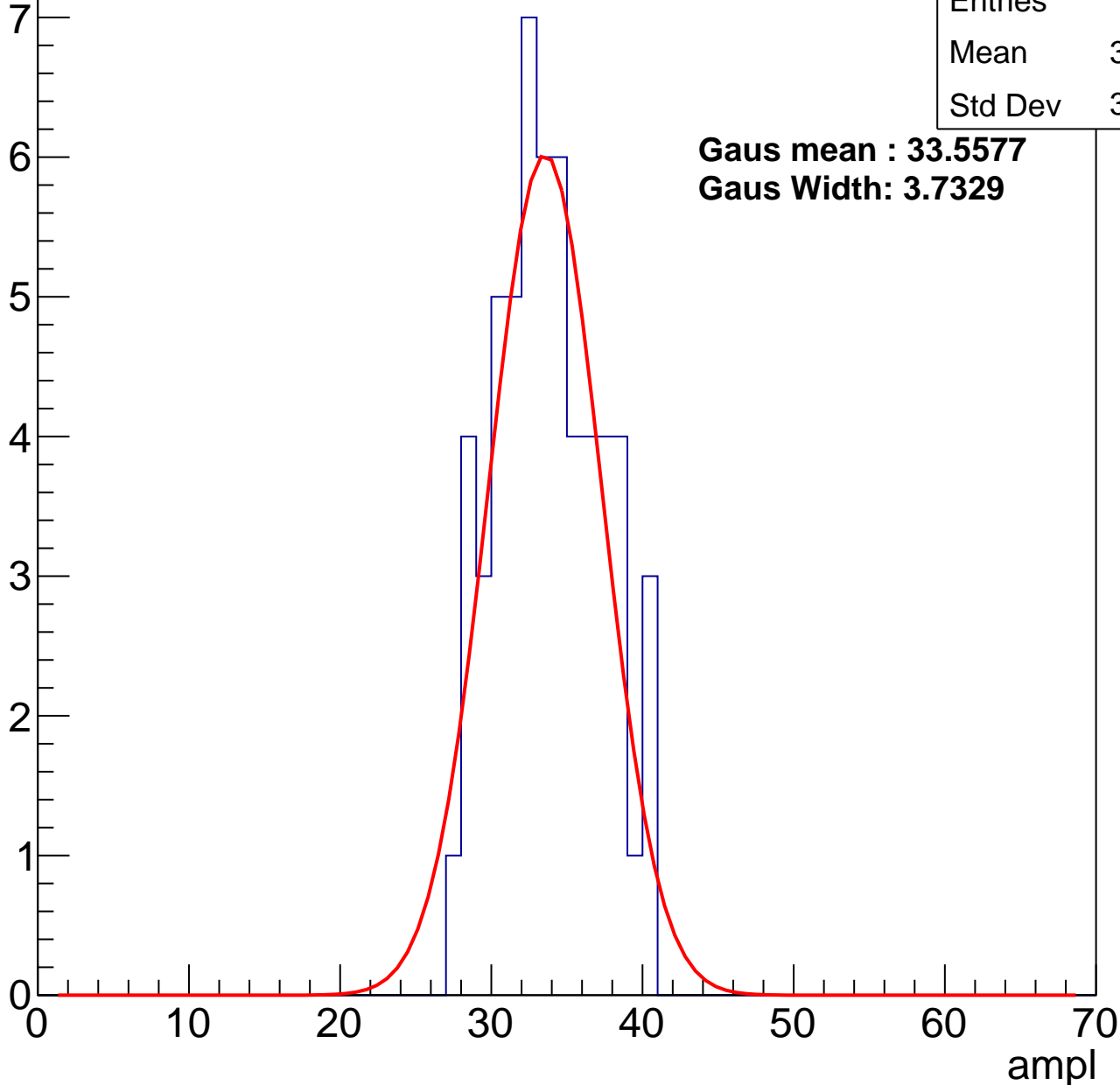
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	33.33
Std Dev	3.389

**Gaus mean : 33.5577**

**Gaus Width: 3.7329**



# B1L101S, U8-ch92, adc2

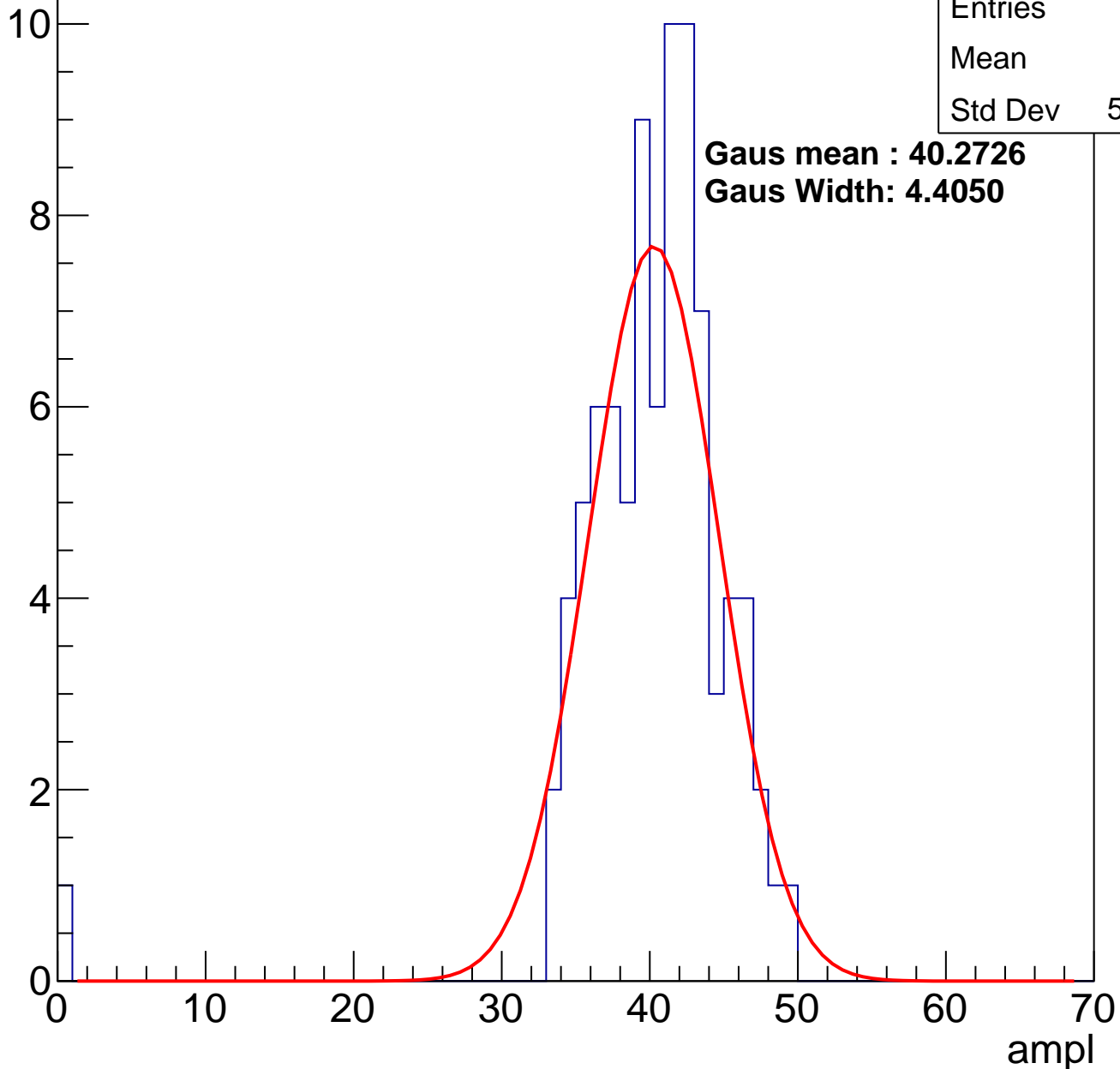
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	86
Mean	39.7
Std Dev	5.692

**Gaus mean : 40.2726**

**Gaus Width: 4.4050**

Entry

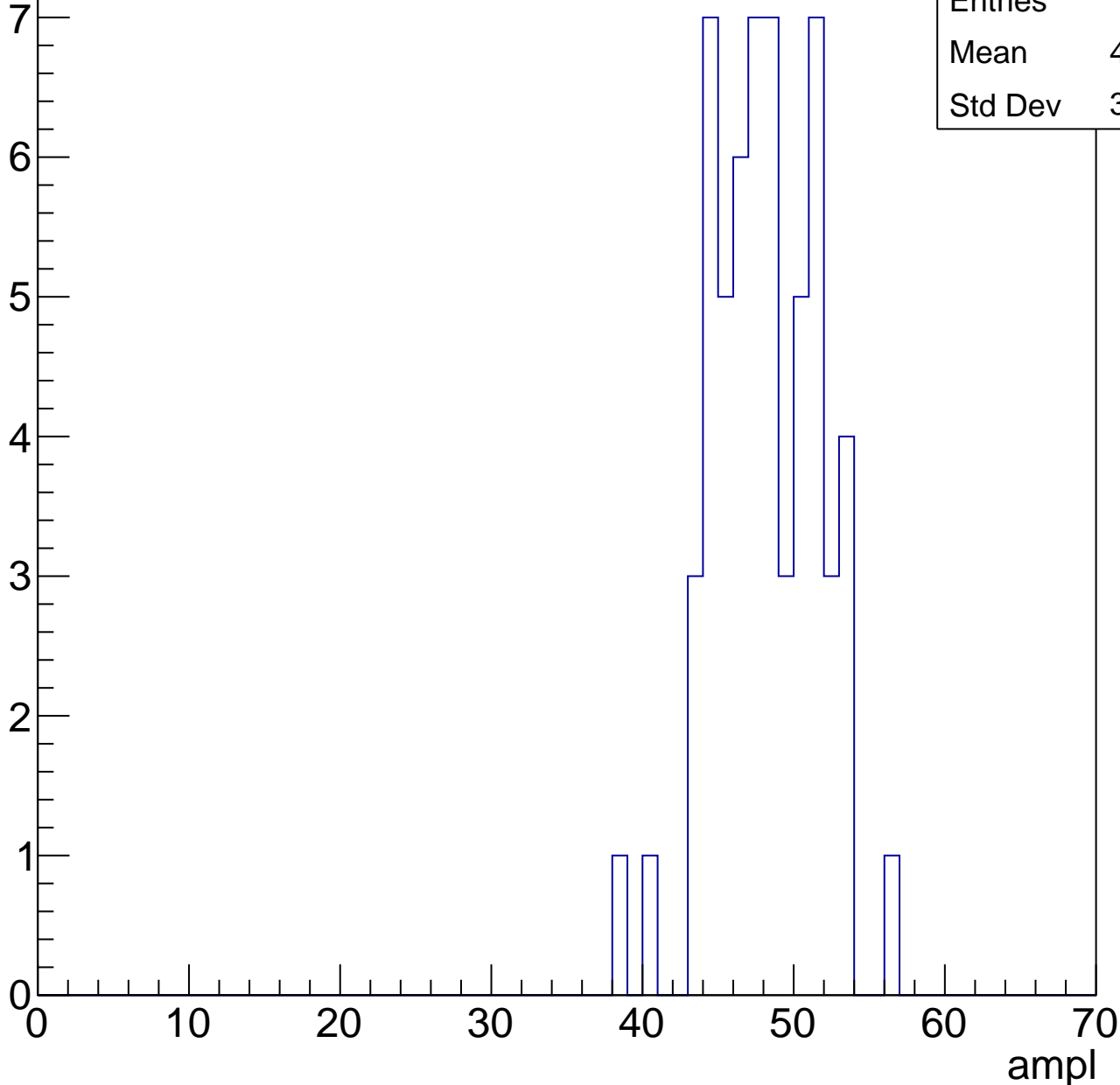


# B1L101S, U8-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	47.65
Std Dev	3.458

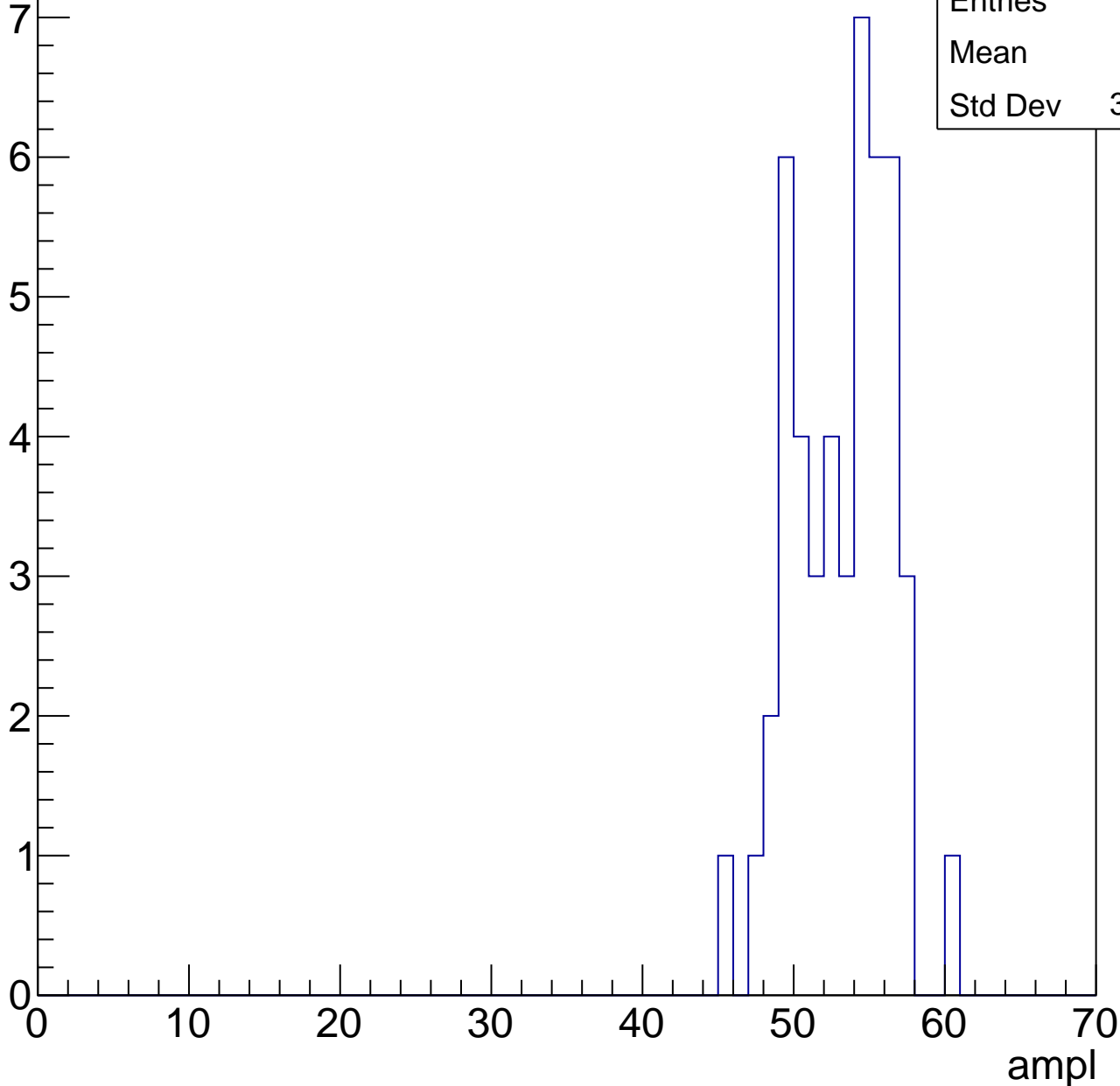


# B1L101S, U8-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	52.7
Std Dev	3.182

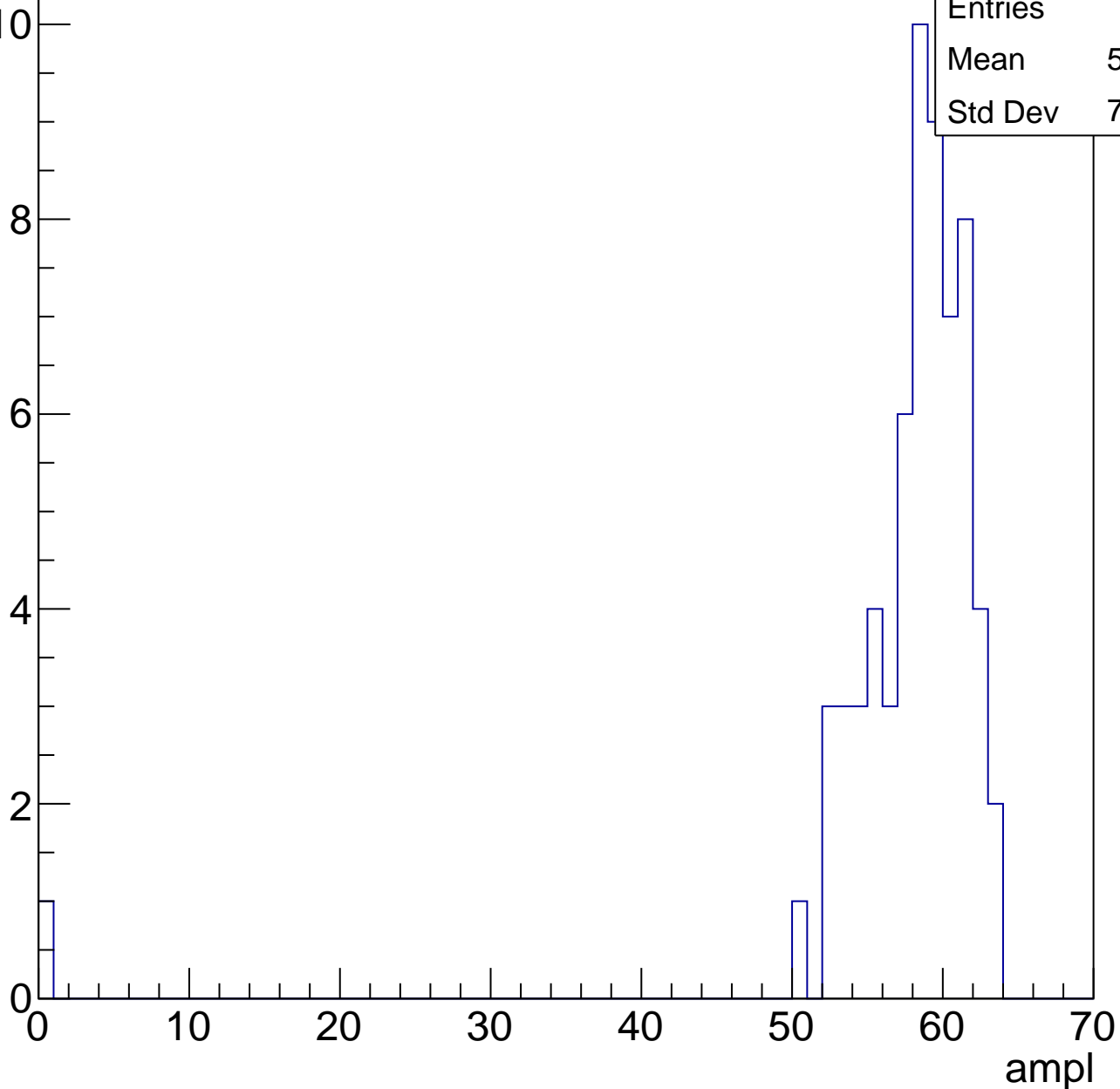


# B1L101S, U8-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	57.03
Std Dev	7.782

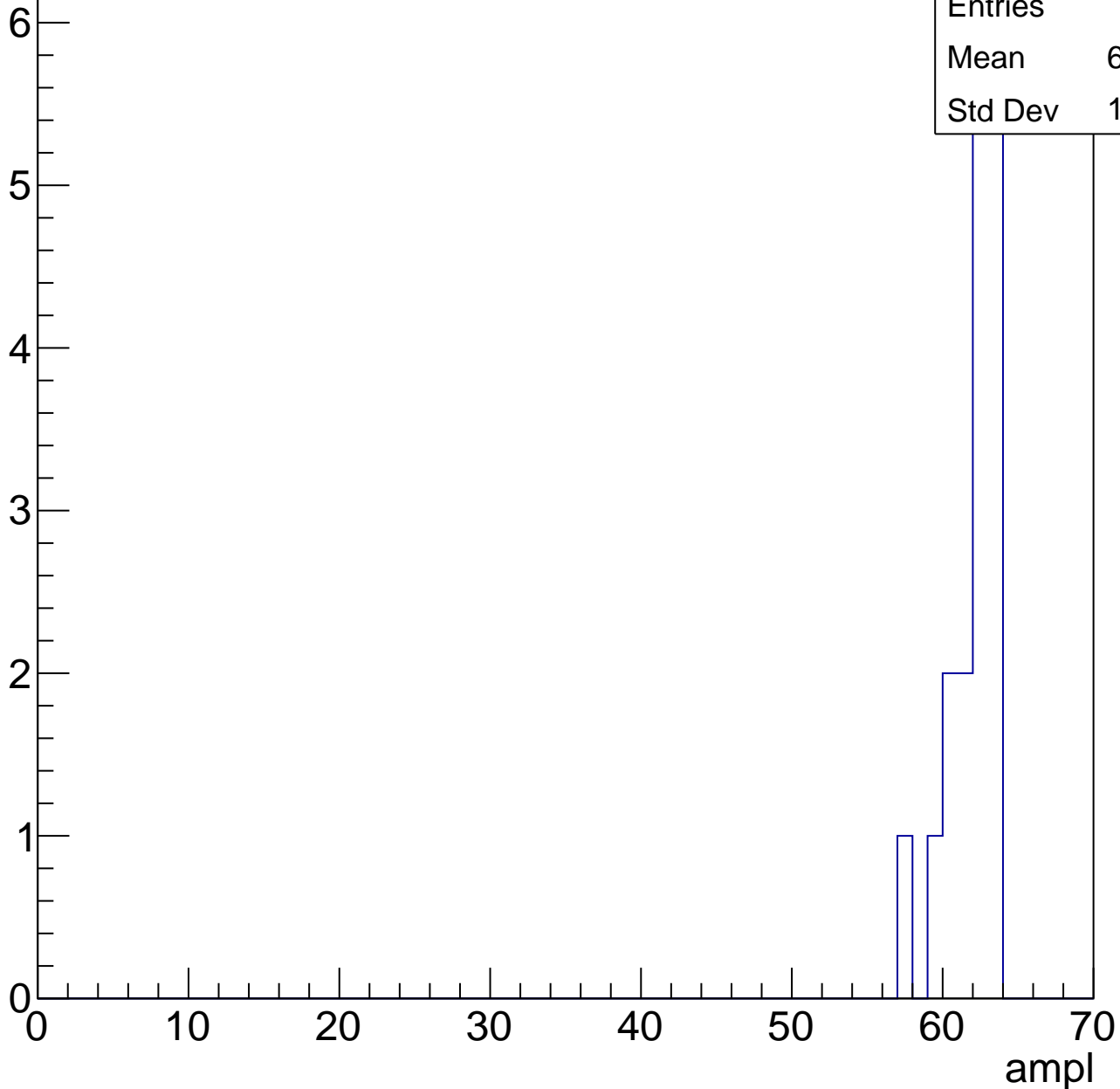


# B1L101S, U8-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	18
Mean	61.56
Std Dev	1.606





# B1L101S, U8-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch93, adc0

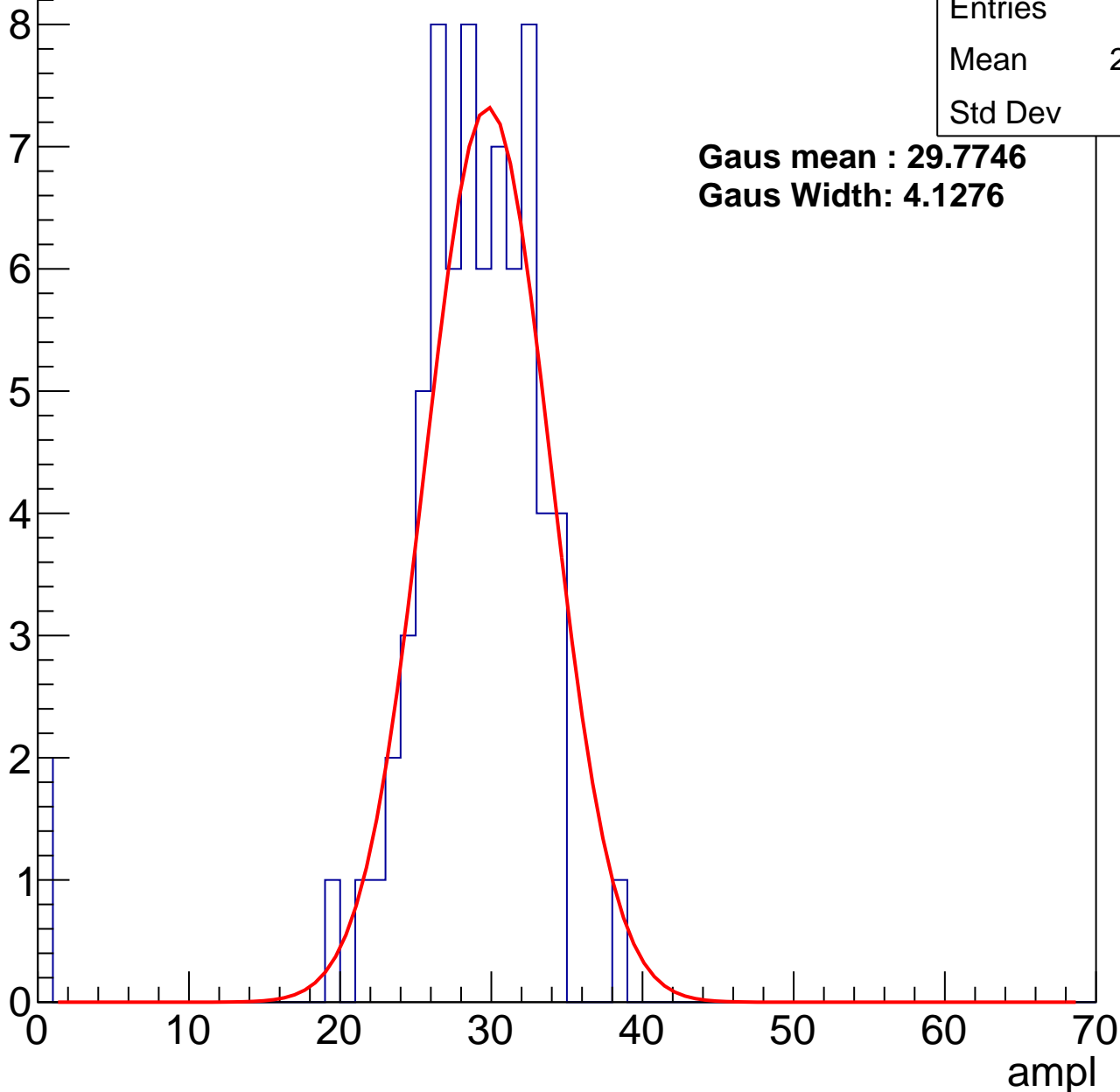
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	27.82
Std Dev	5.82

**Gaus mean : 29.7746**

**Gaus Width: 4.1276**



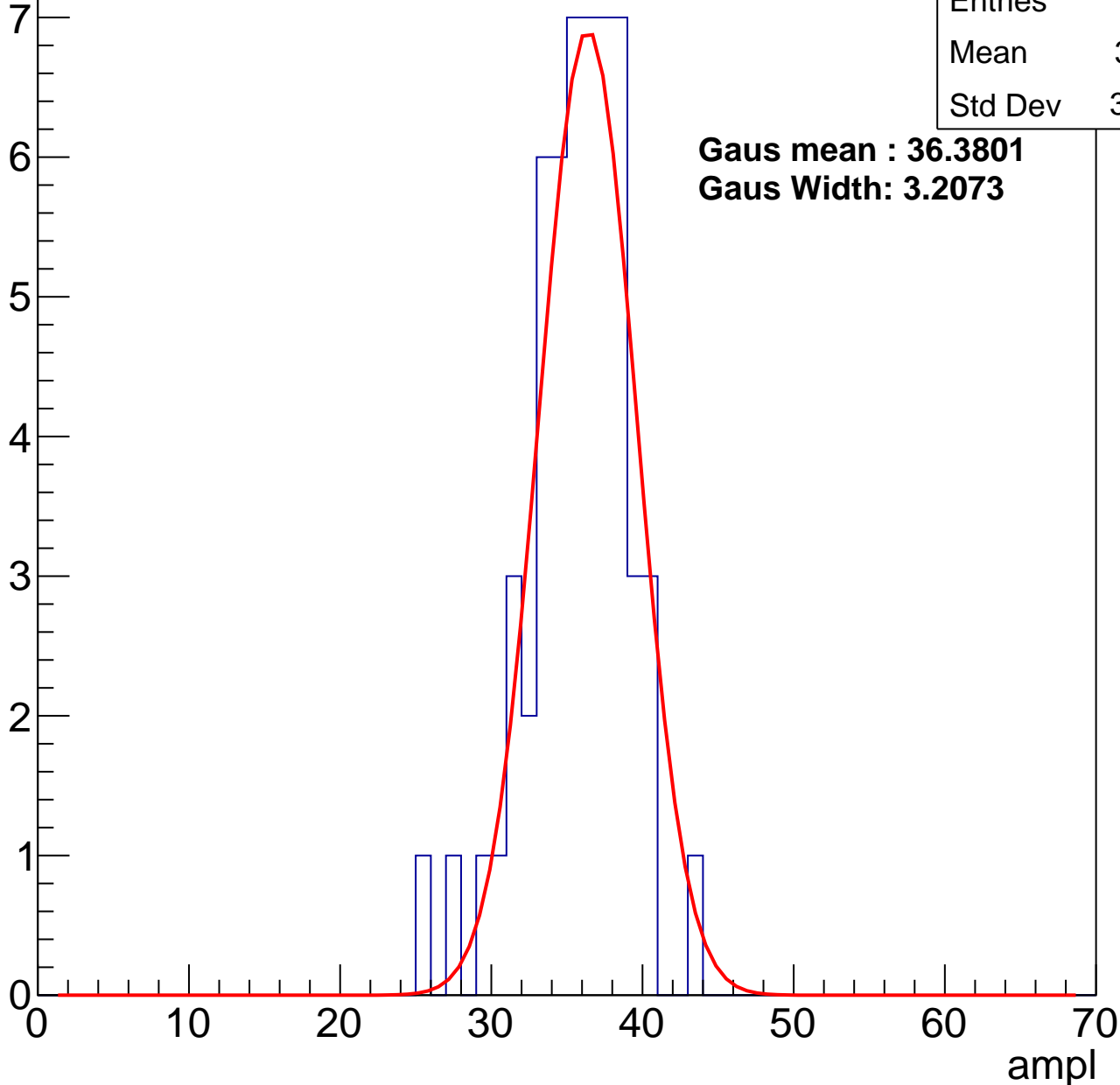
# B1L101S, U8-ch93, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	35.21
Std Dev	3.283

**Gaus mean : 36.3801**  
**Gaus Width: 3.2073**



# B1L101S, U8-ch93, adc2

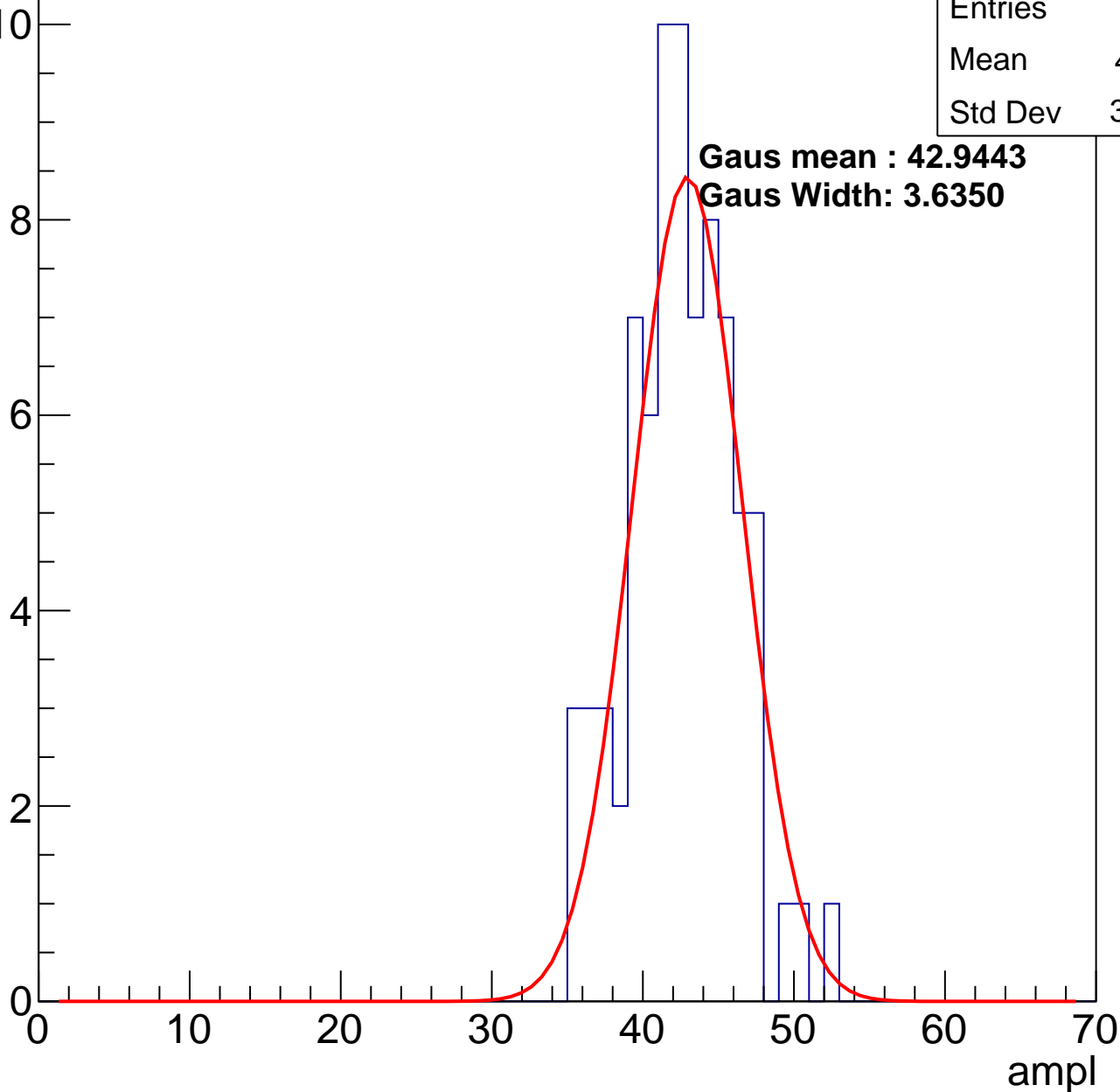
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	42.11
Std Dev	3.518

**Gaus mean : 42.9443**

**Gaus Width: 3.6350**



# B1L101S, U8-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

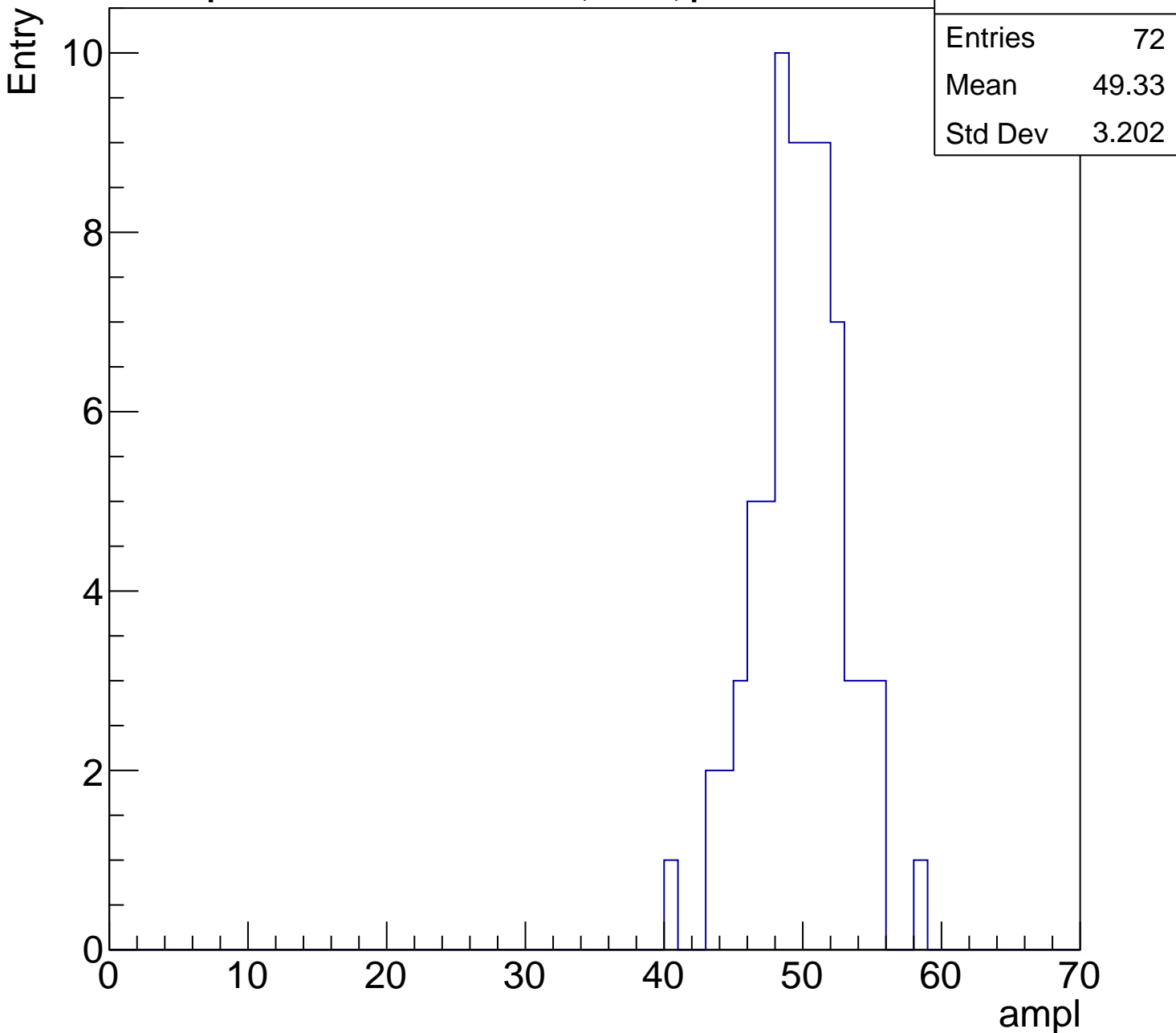
Entries	72
Mean	49.33
Std Dev	3.202

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

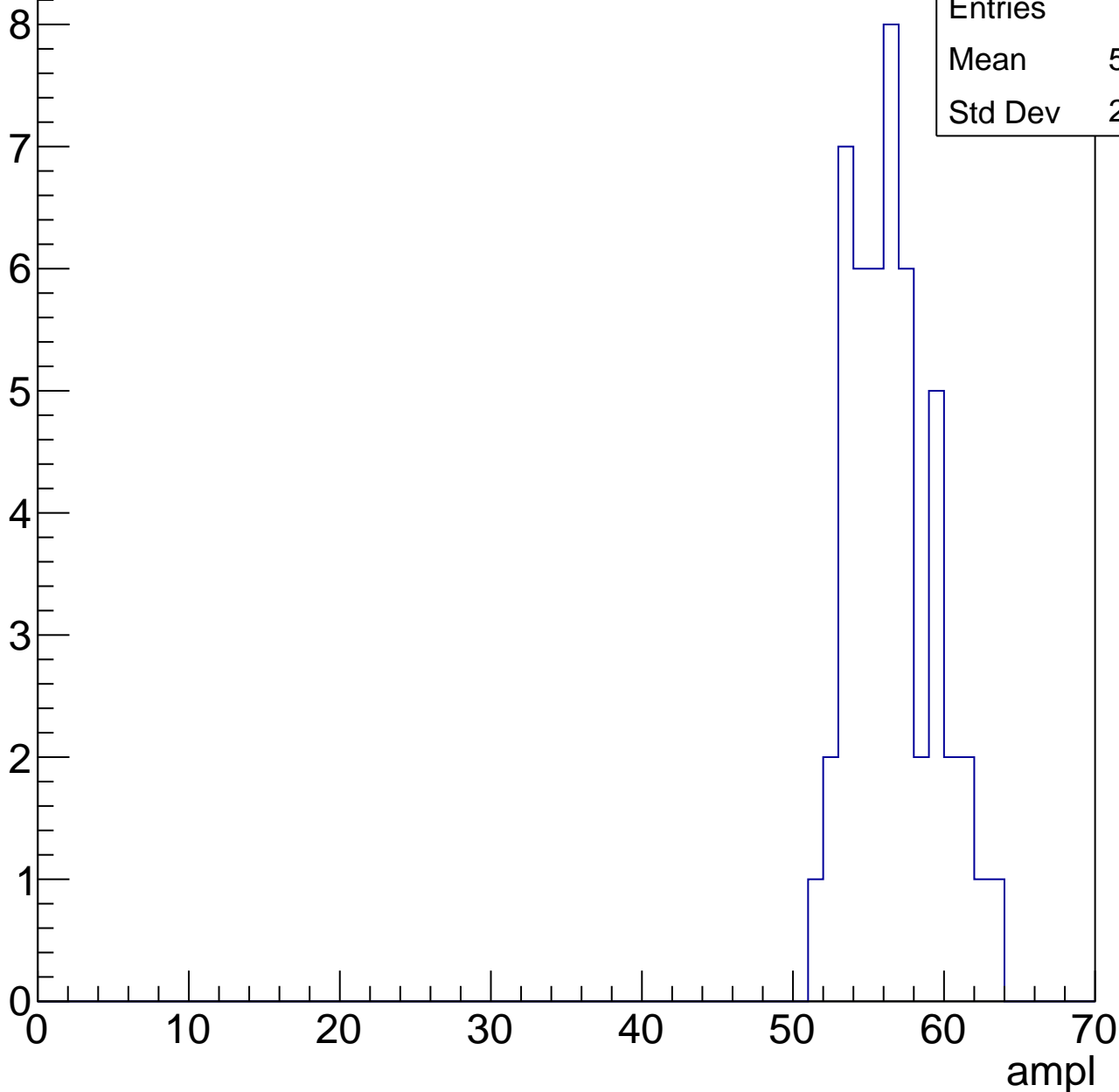


# B1L101S, U8-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	56.08
Std Dev	2.769

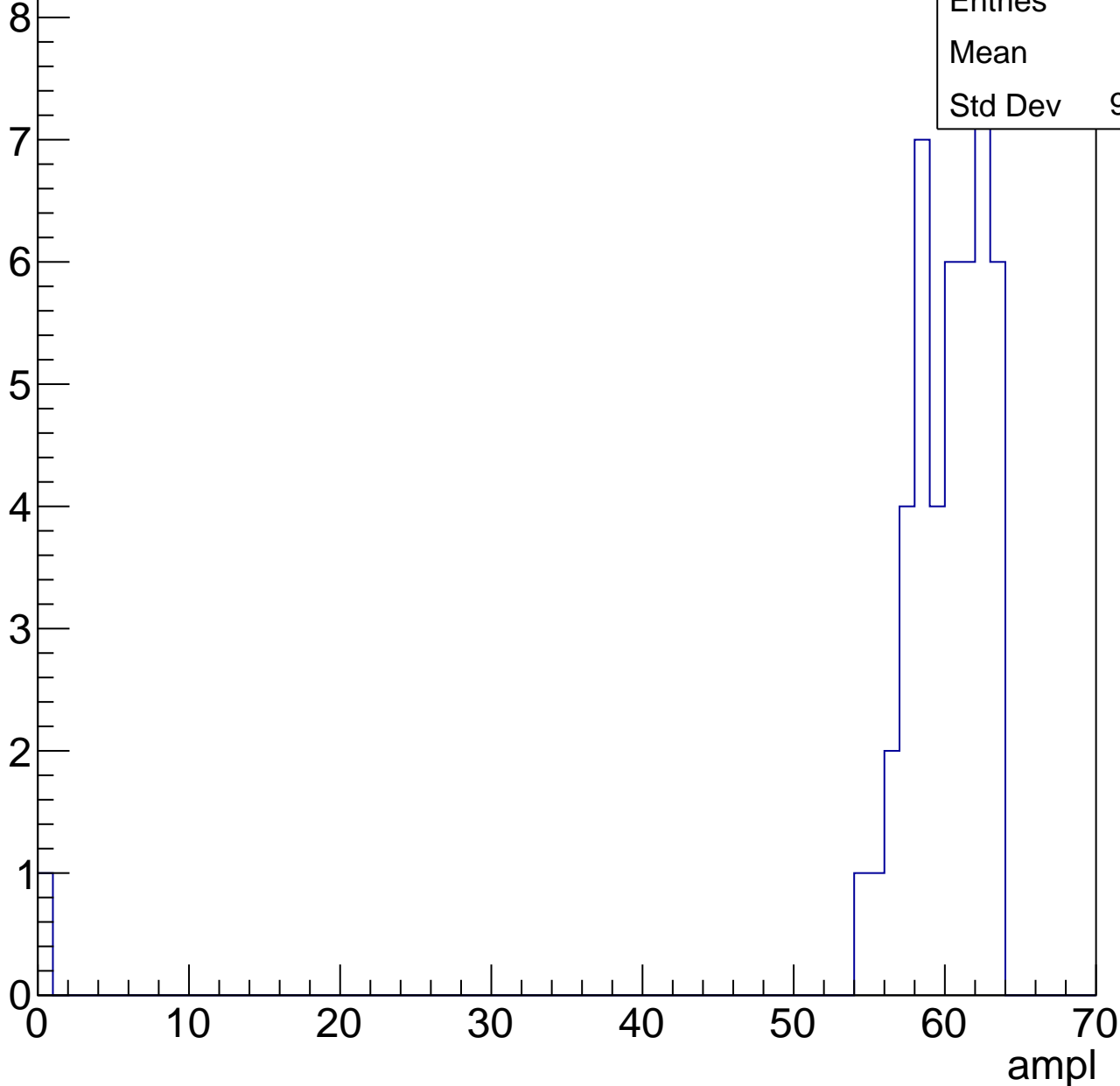


# B1L101S, U8-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	58.5
Std Dev	9.028



# B1L101S, U8-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	8
Mean	61.12
Std Dev	1.364

ampl

0 10 20 30 40 50 60 70



# B1L101S, U8-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch94, adc0

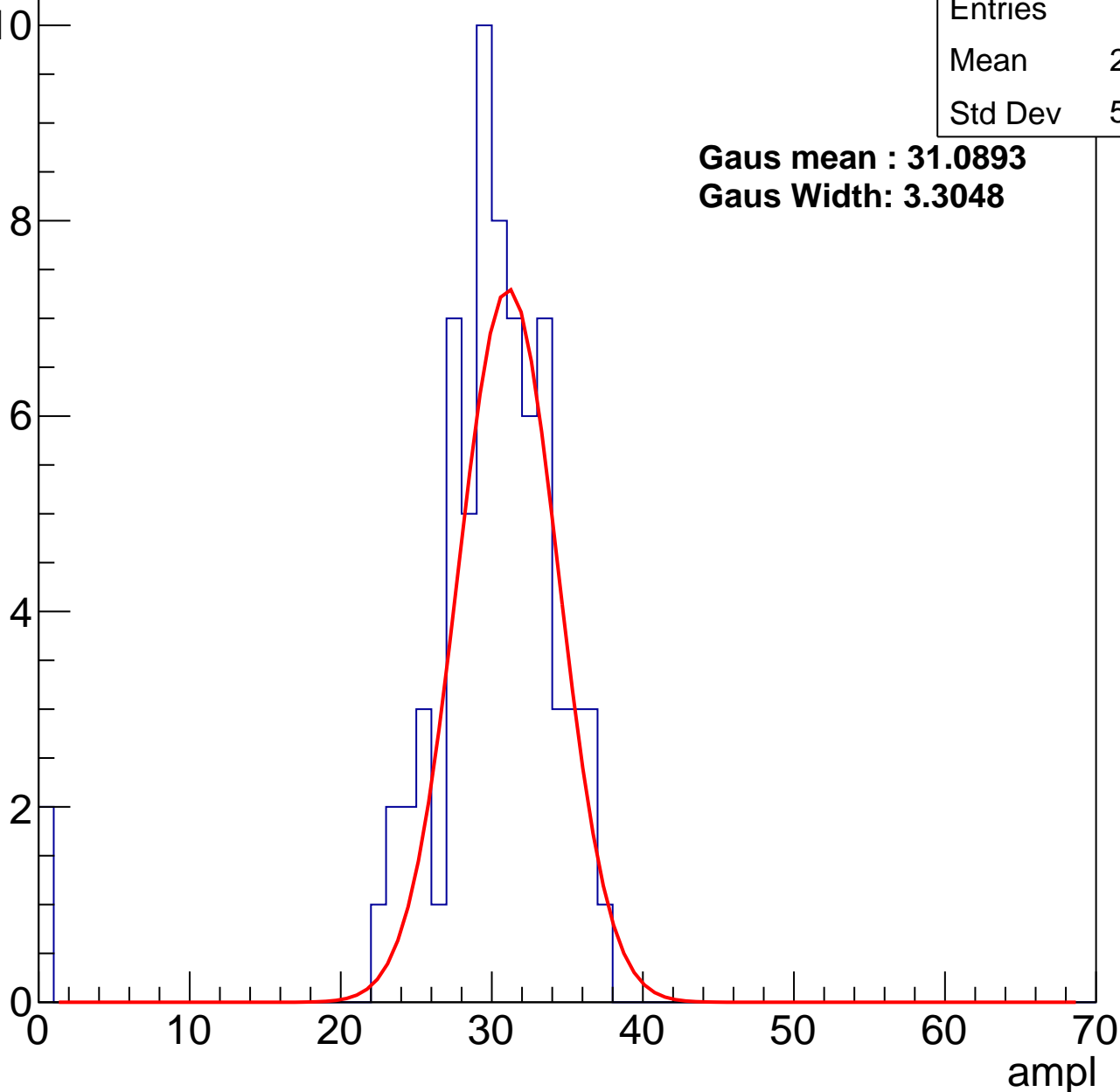
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	29.13
Std Dev	5.979

**Gaus mean : 31.0893**

**Gaus Width: 3.3048**



# B1L101S, U8-ch94, adc1

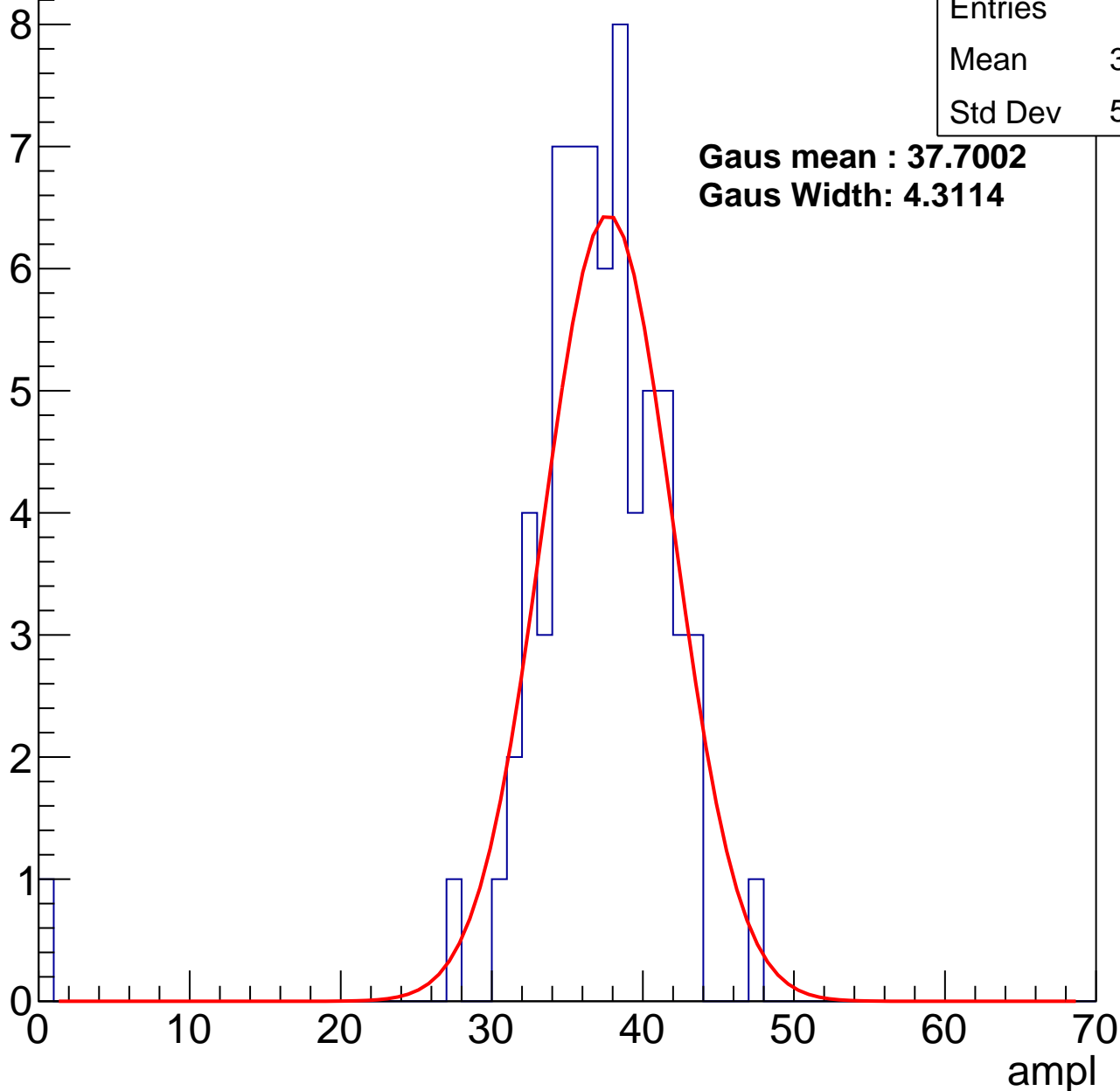
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	36.32
Std Dev	5.735

**Gaus mean : 37.7002**

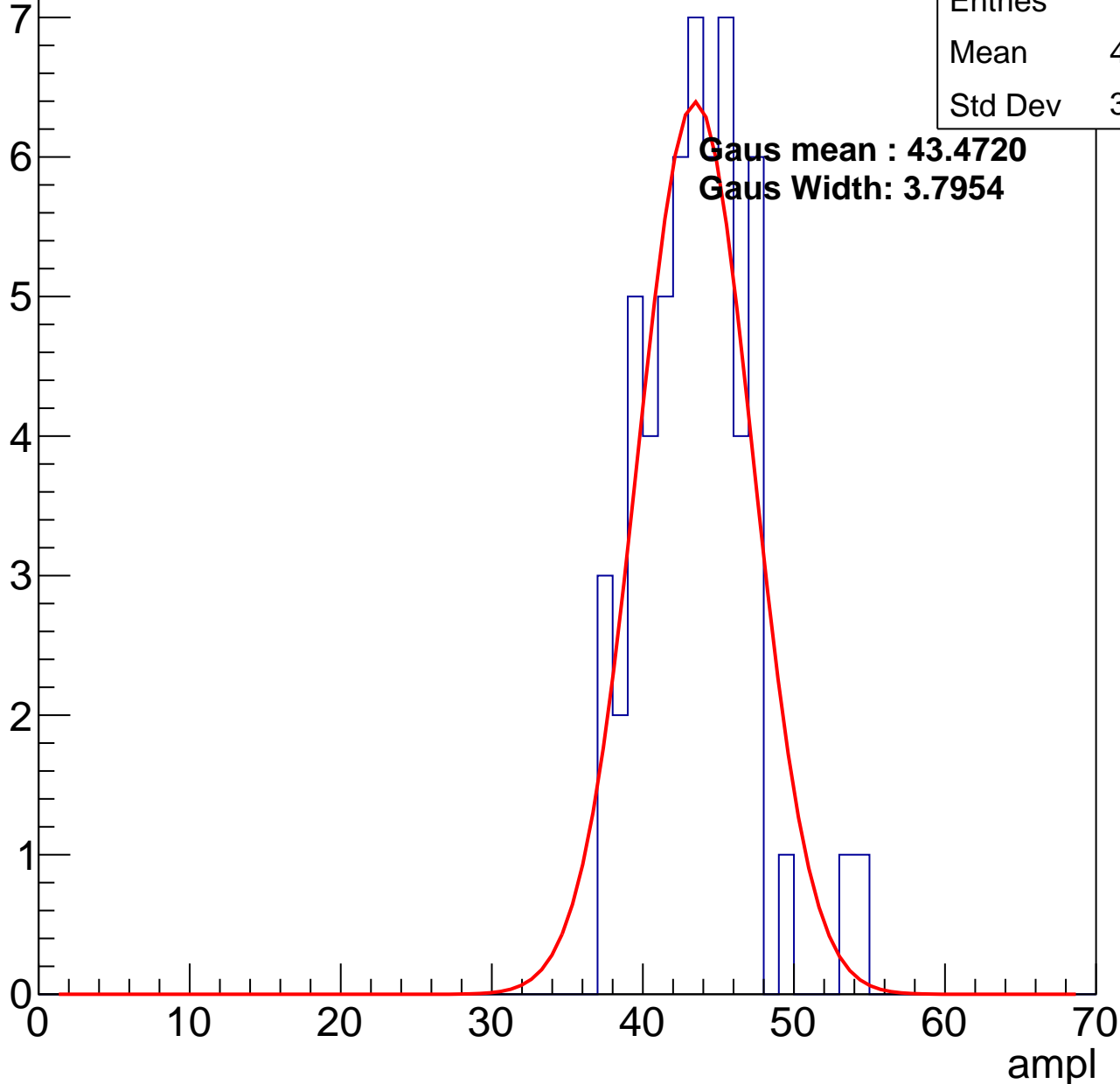
**Gaus Width: 4.3114**



# B1L101S, U8-ch94, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

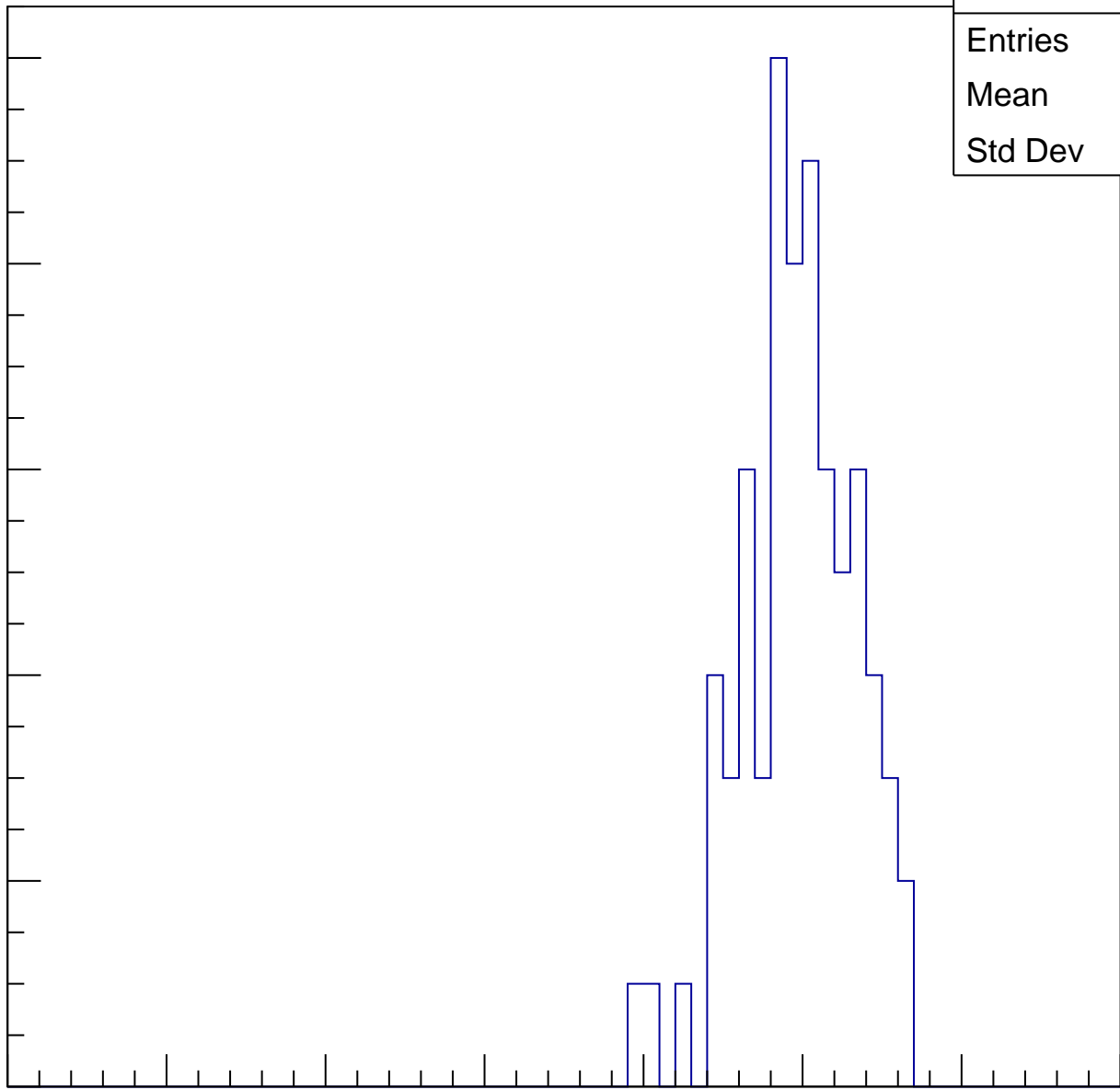
Entries	72
Mean	49.28
Std Dev	3.591

Entry

10  
8  
6  
4  
2  
0

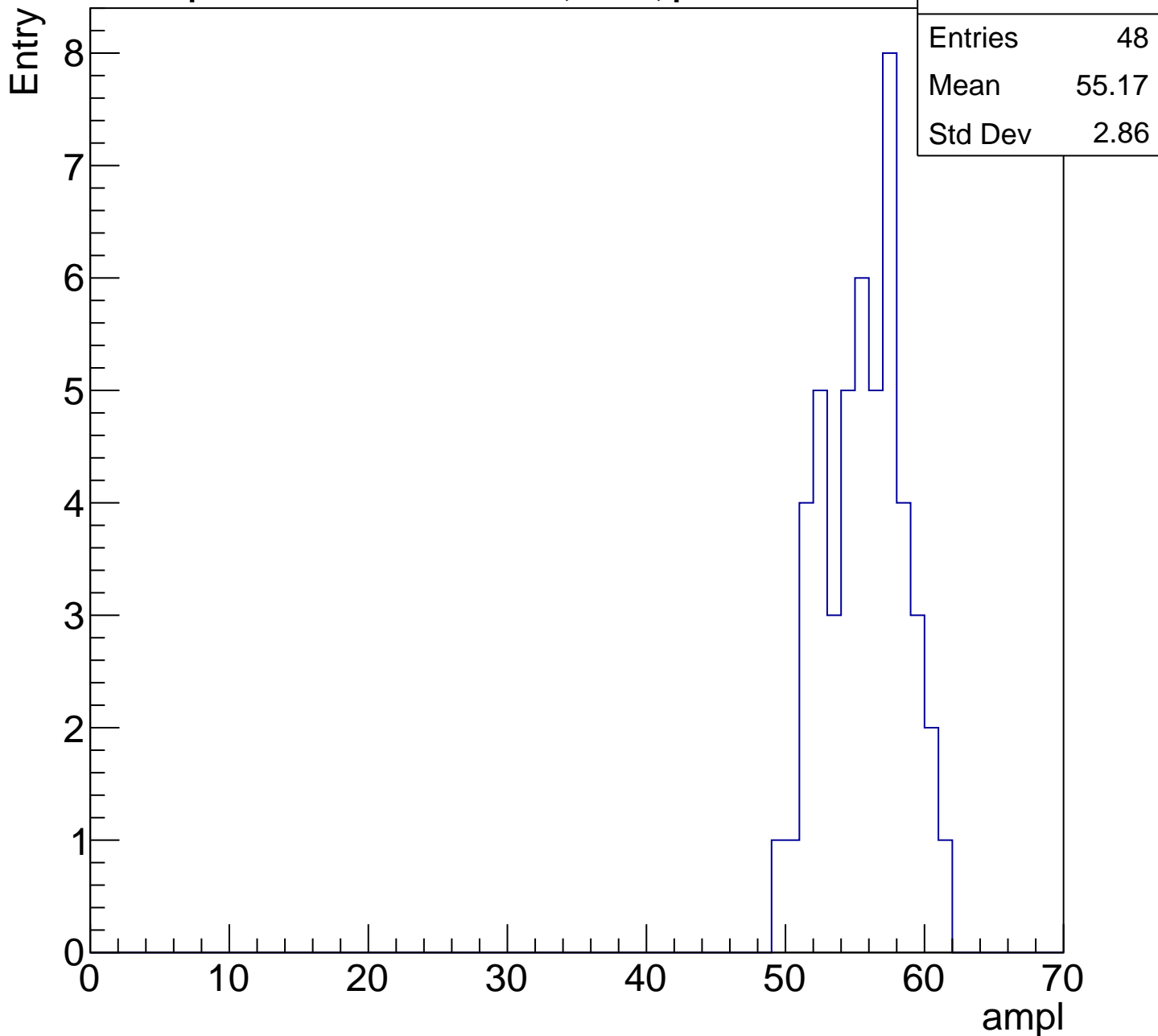
ampl

0 10 20 30 40 50 60 70



# B1L101S, U8-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U8-ch94, adc5

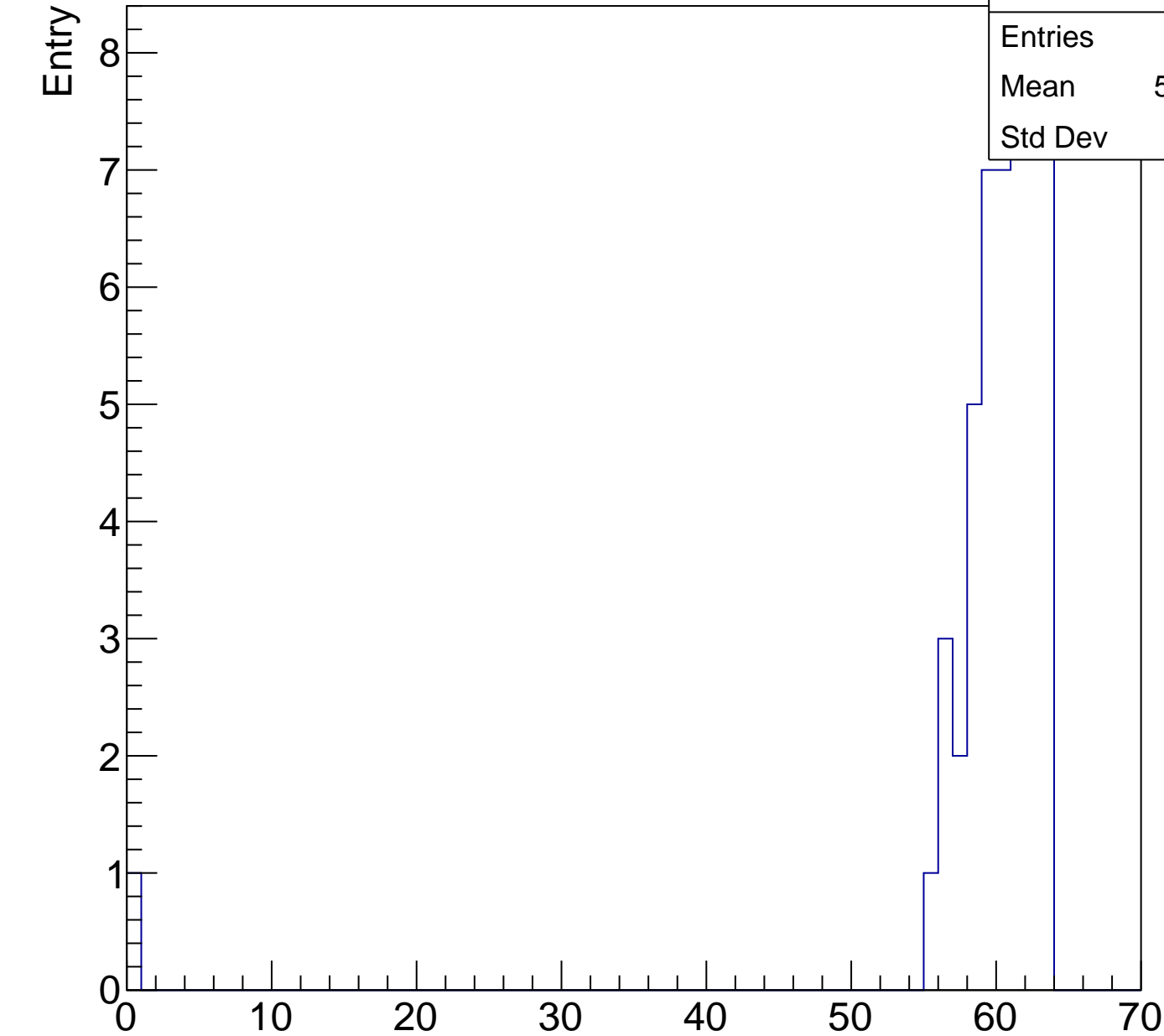
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	50
Mean	58.96
Std Dev	8.69

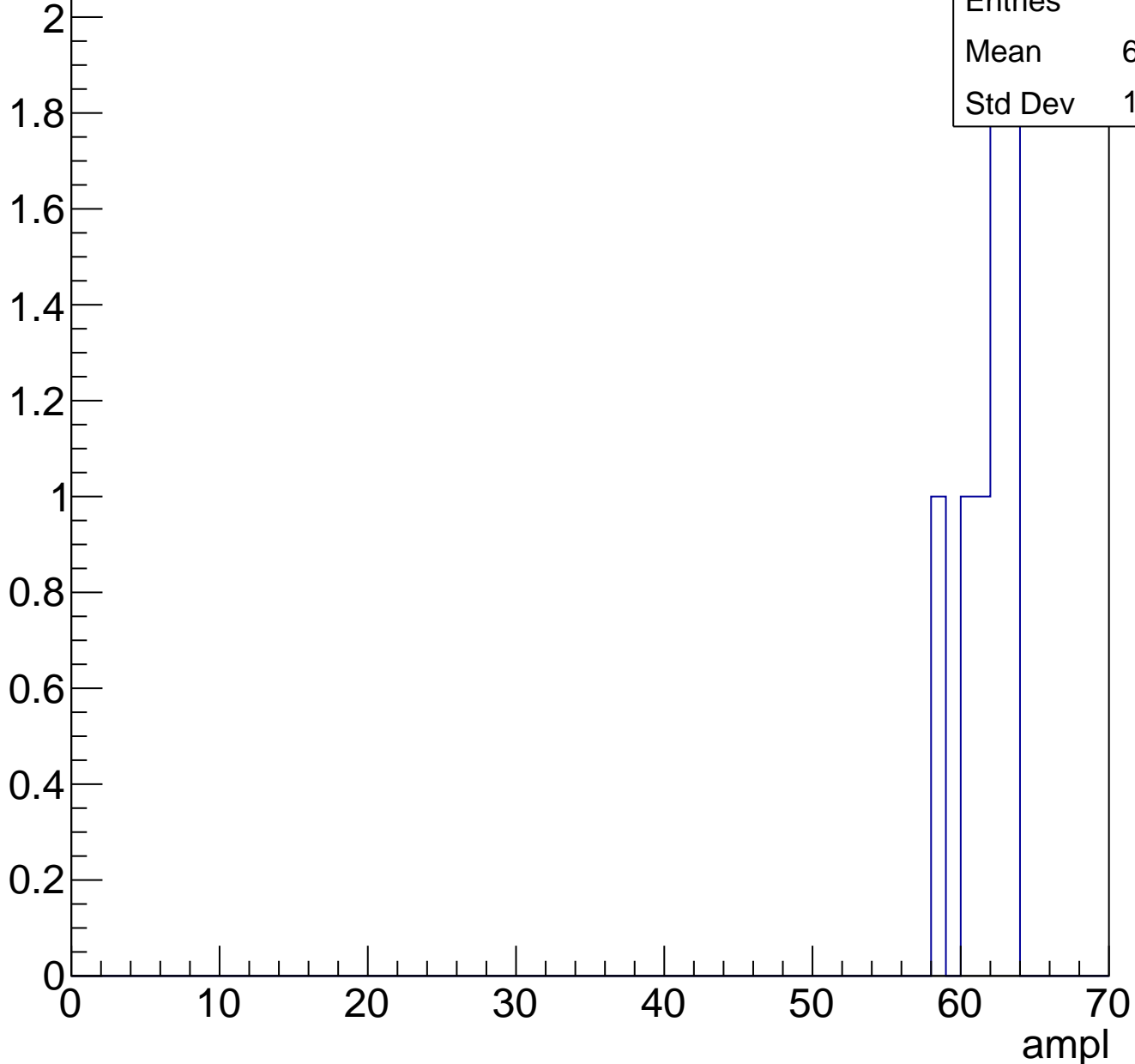
ampl



# B1L101S, U8-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U8-ch95, adc0

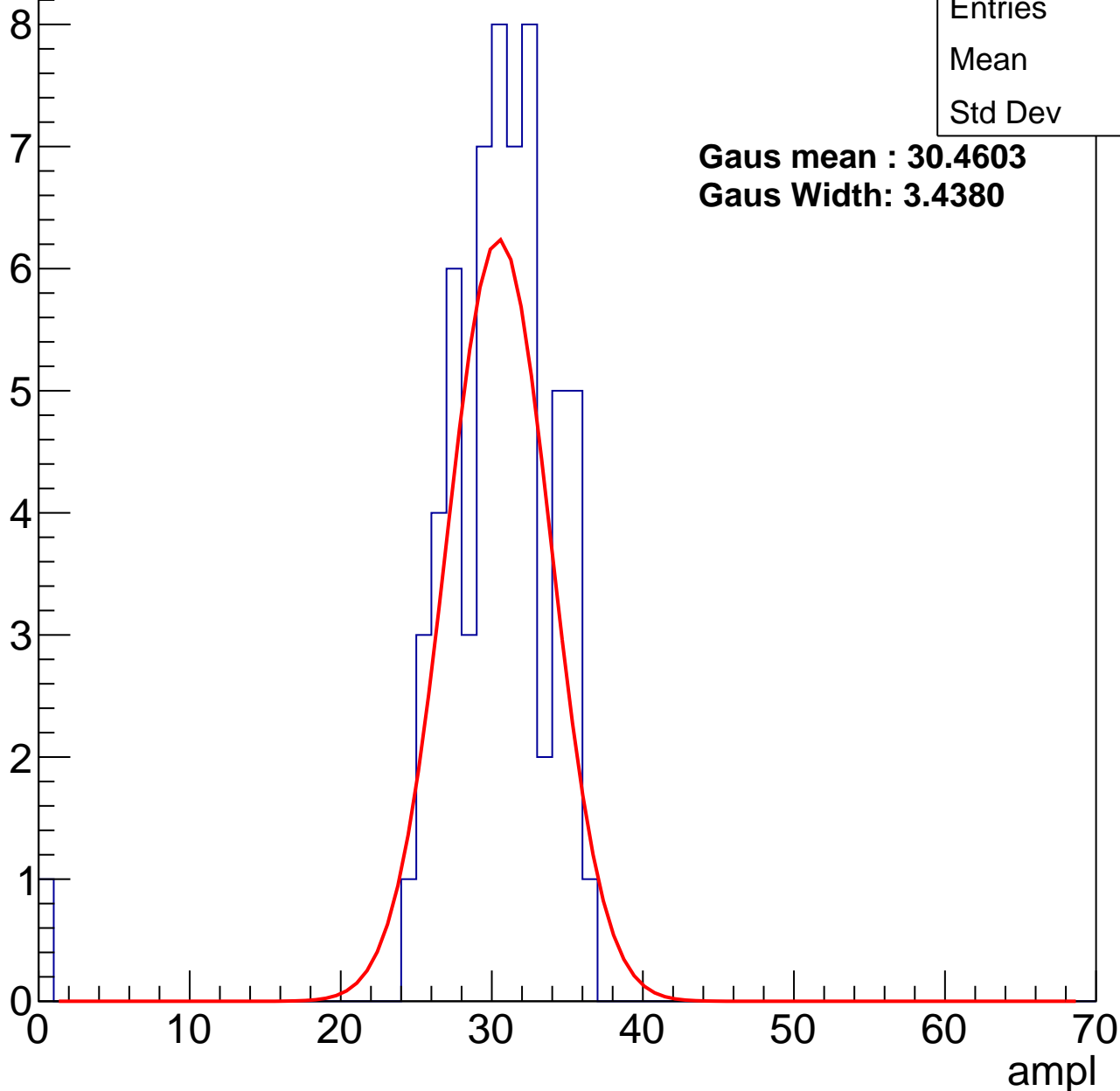
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	29.7
Std Dev	4.86

**Gaus mean : 30.4603**

**Gaus Width: 3.4380**



# B1L101S, U8-ch95, adc1

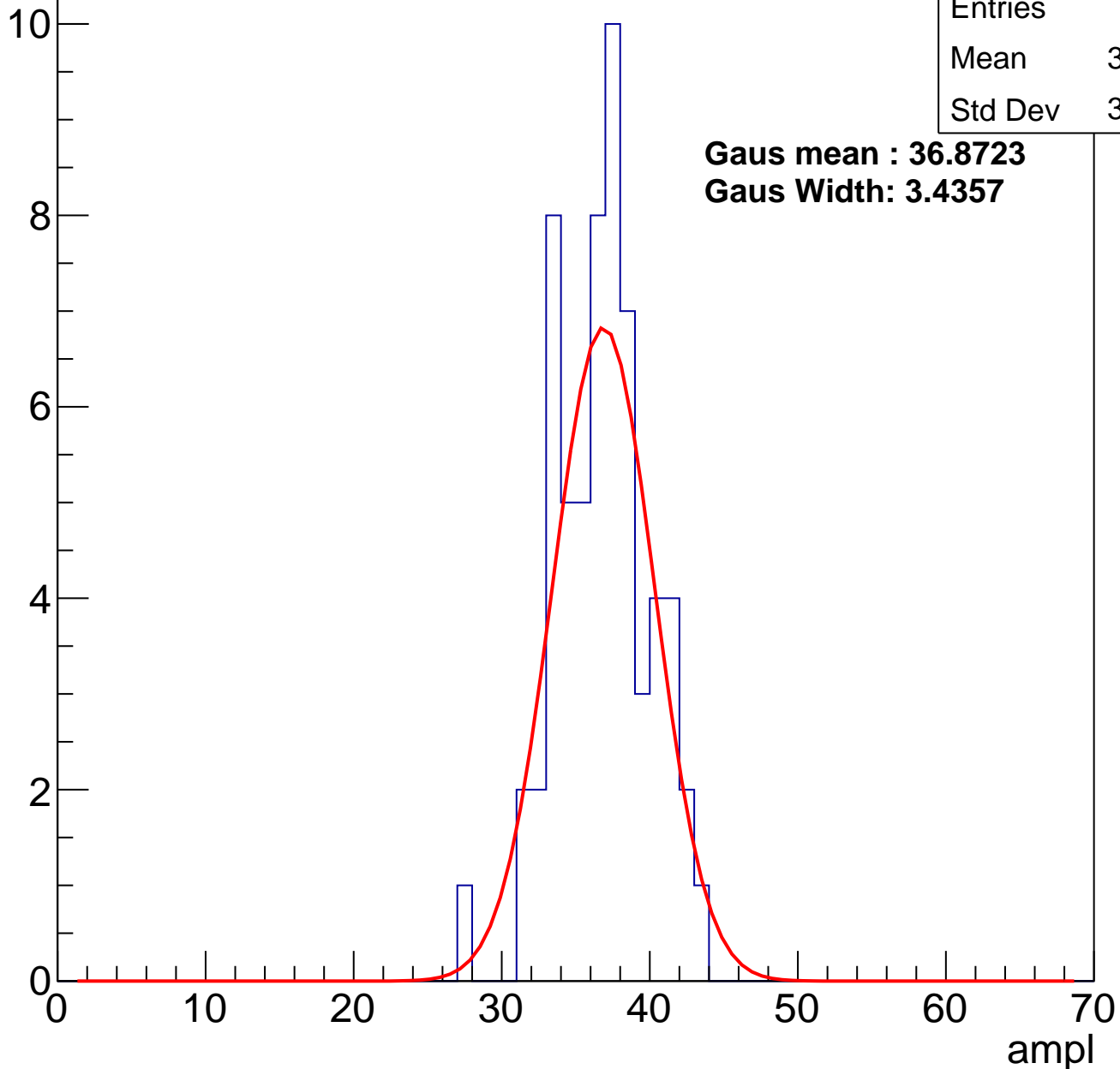
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	62
Mean	36.35
Std Dev	3.117

**Gaus mean : 36.8723**

**Gaus Width: 3.4357**

Entry



# B1L101S, U8-ch95, adc2

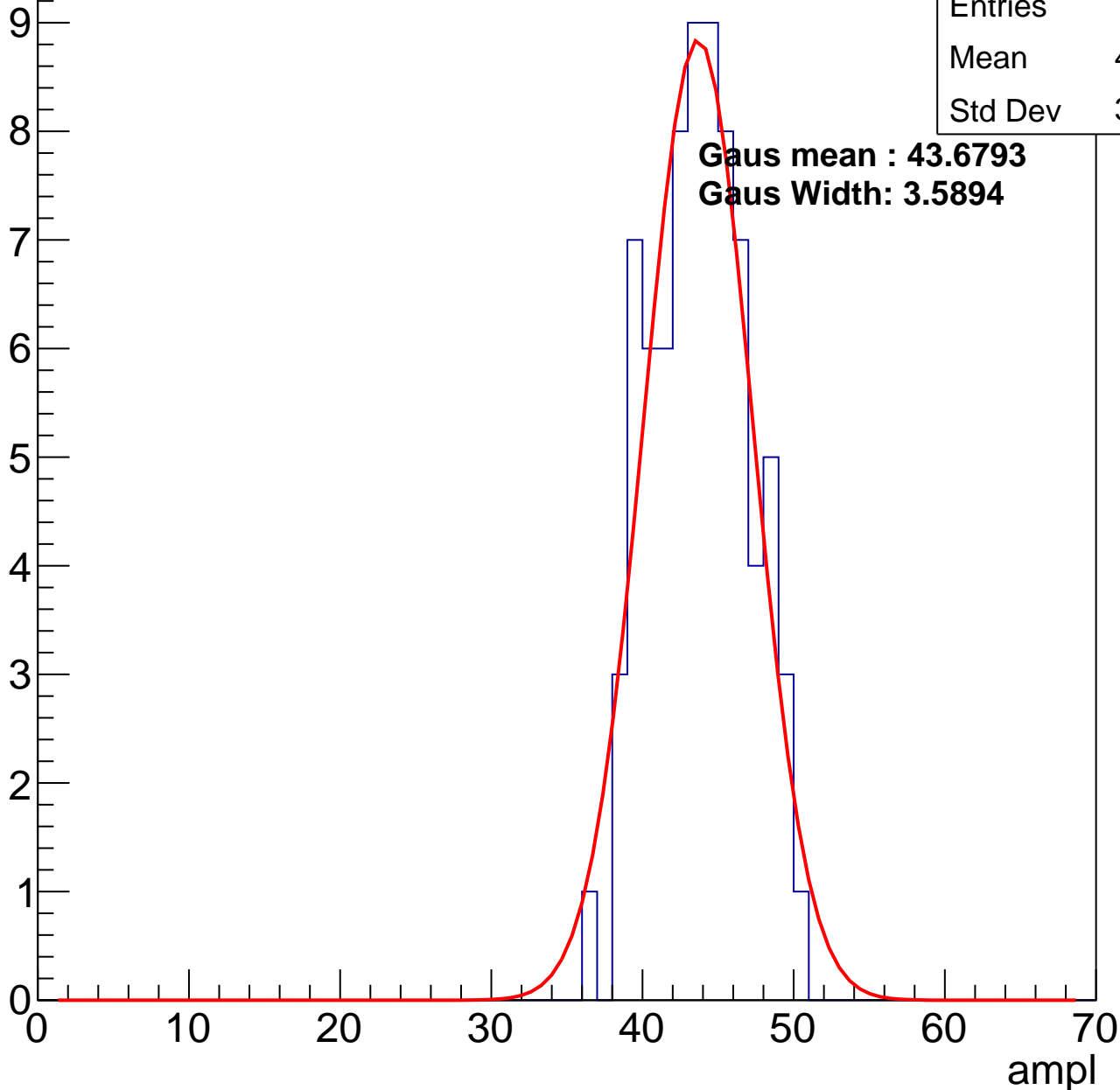
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	43.31
Std Dev	3.151

**Gaus mean : 43.6793**

**Gaus Width: 3.5894**

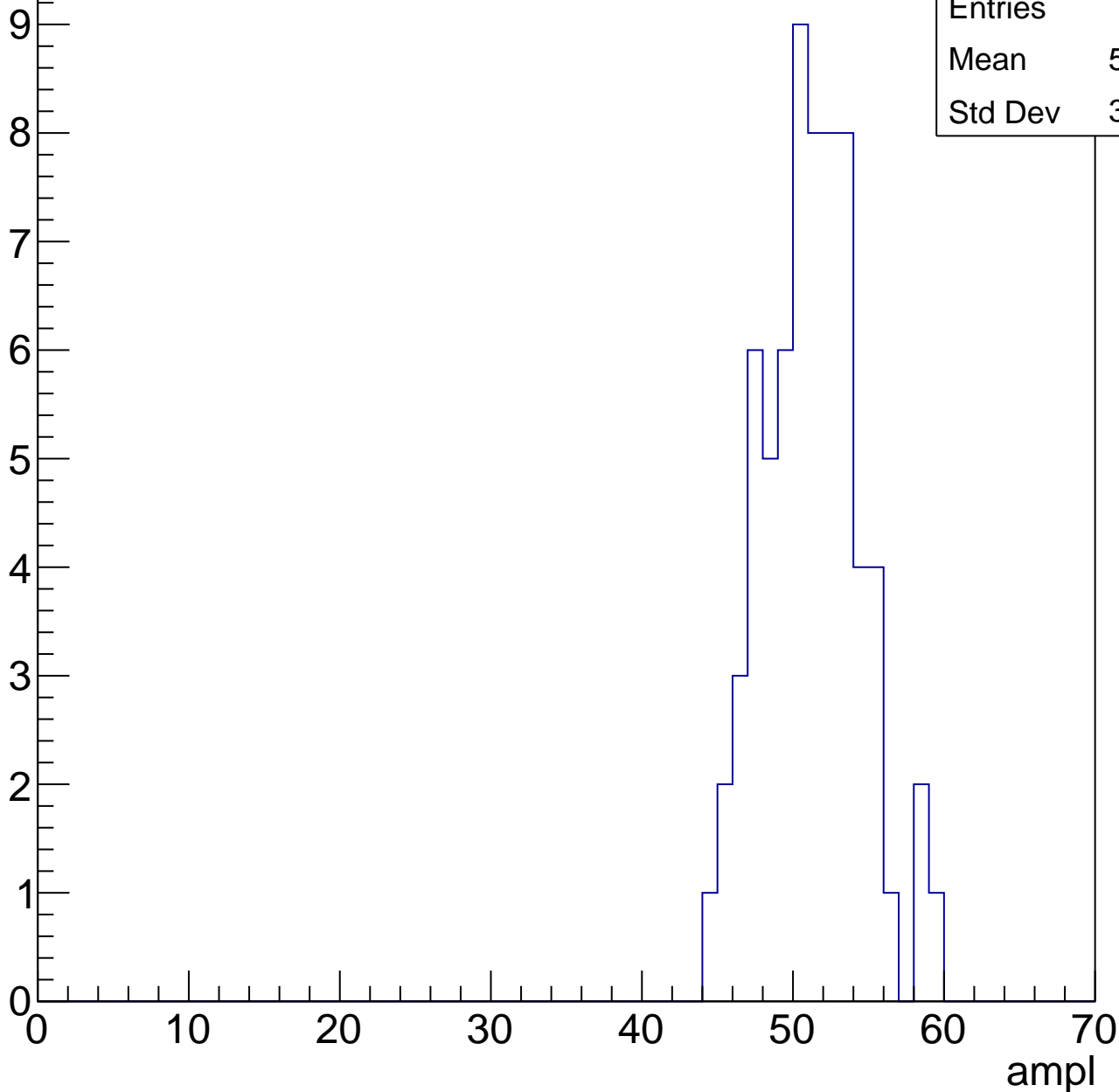


# B1L101S, U8-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	50.78
Std Dev	3.194

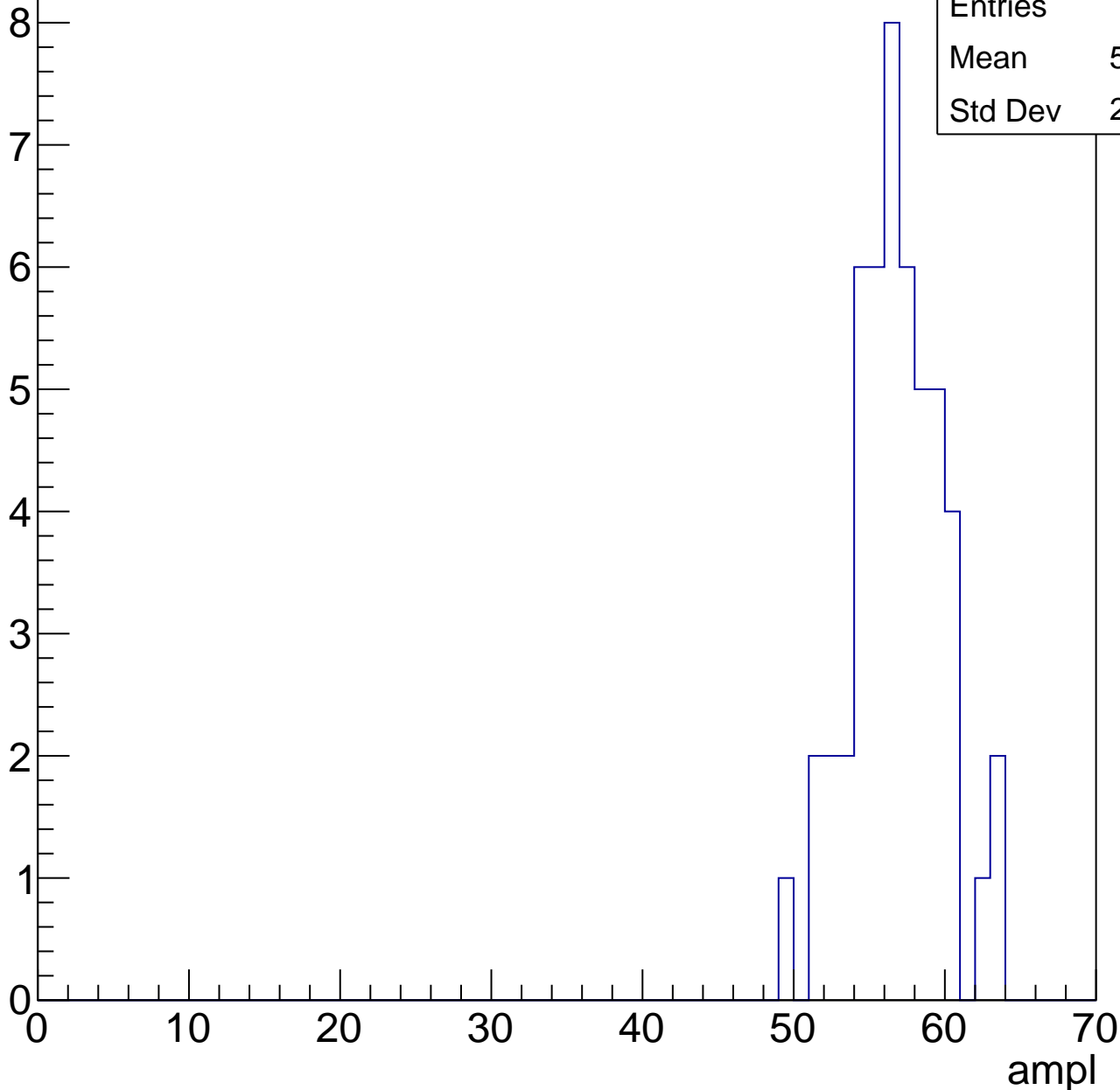


# B1L101S, U8-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	56.36
Std Dev	2.972

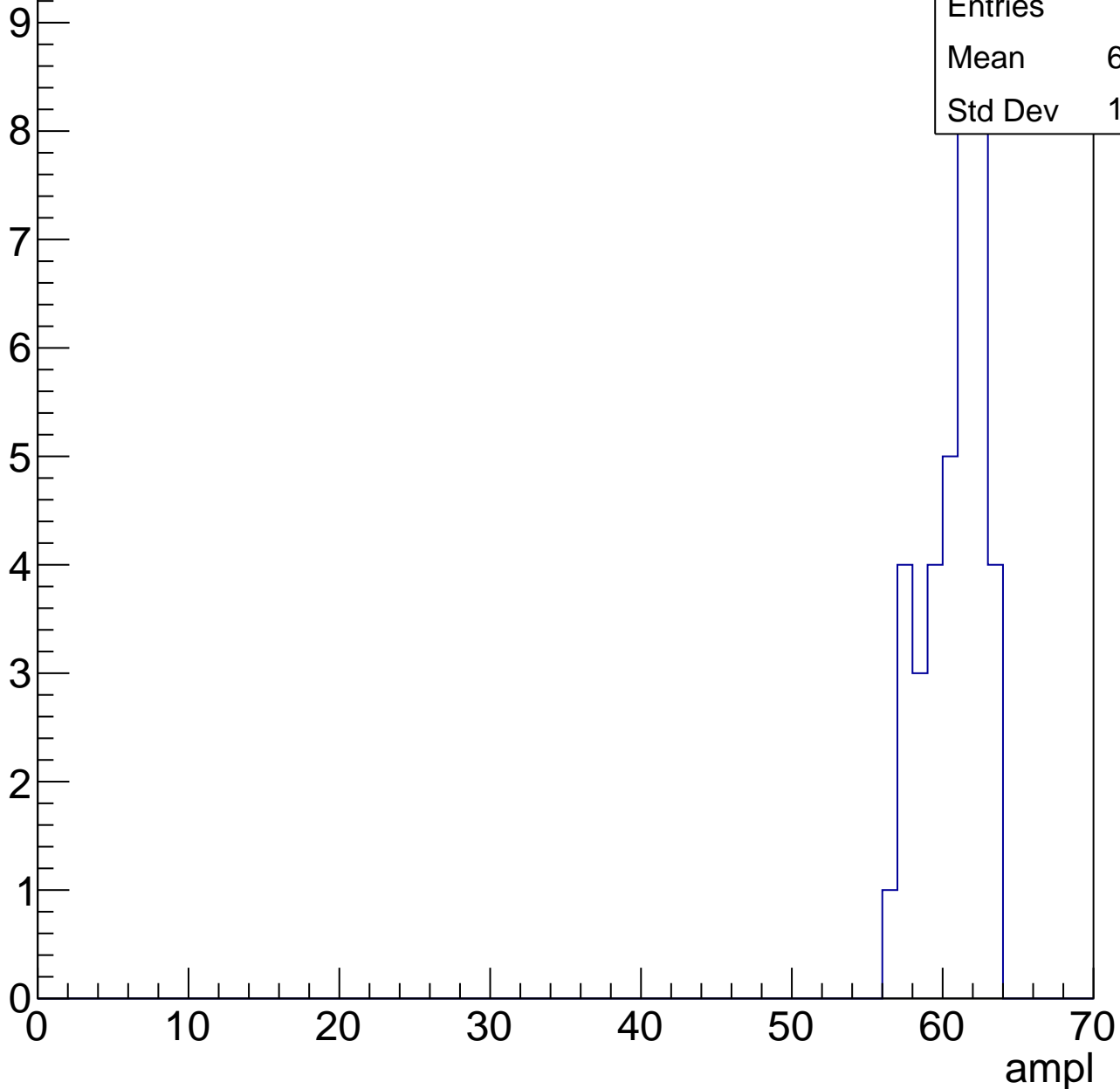


# B1L101S, U8-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

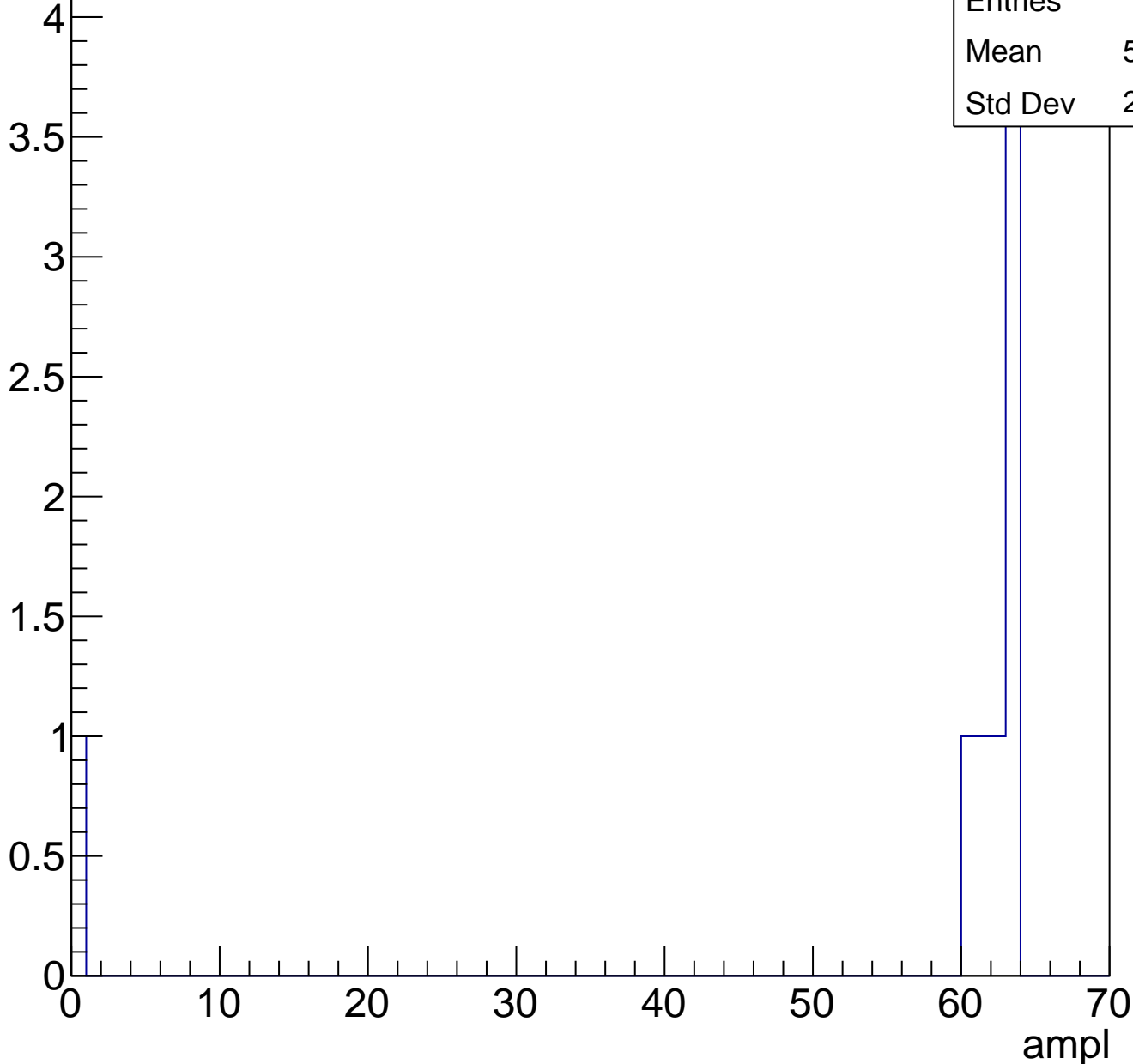
Entries	38
Mean	60.29
Std Dev	1.932



# B1L101S, U8-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U8-ch96, adc0

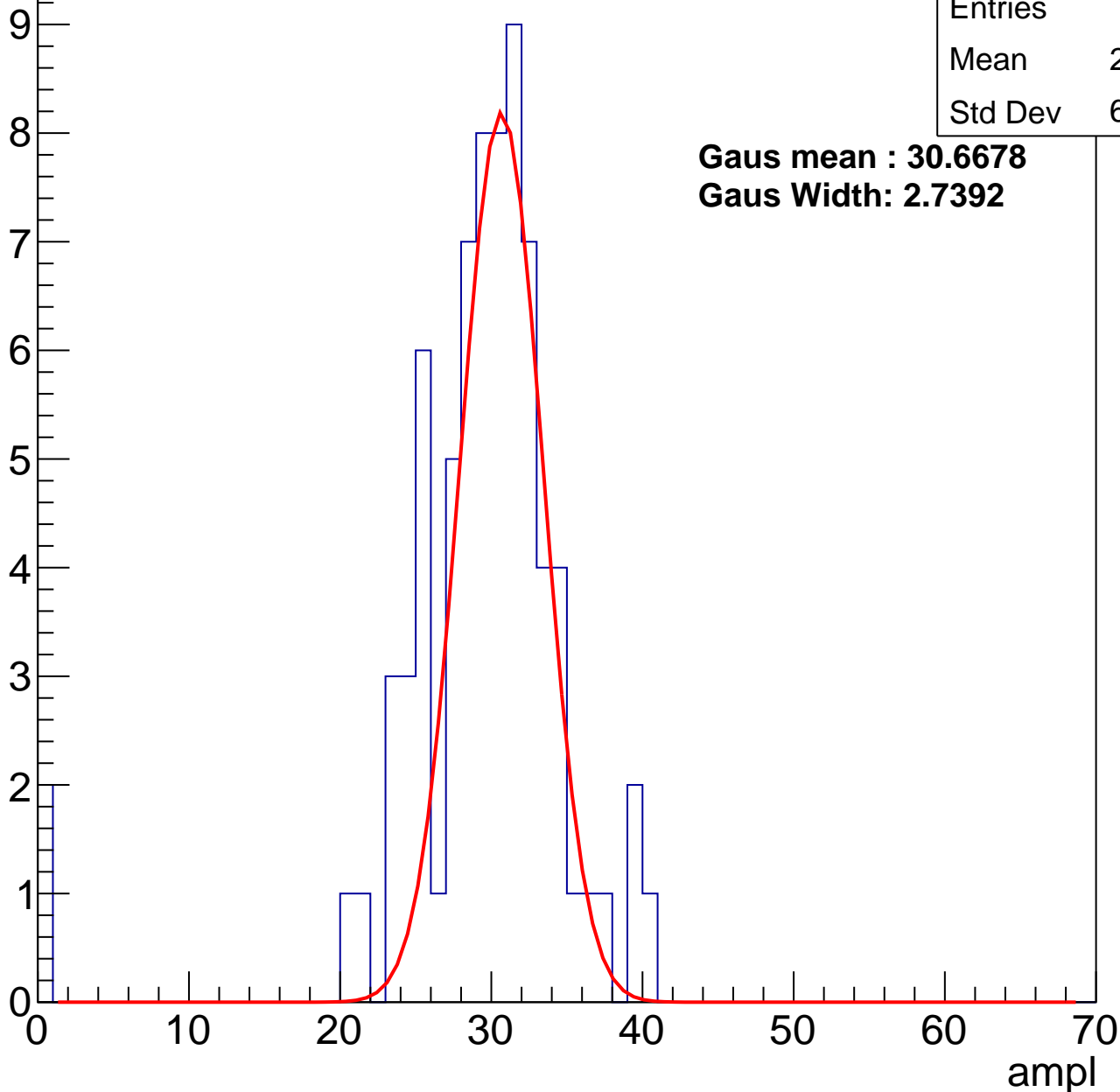
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	28.77
Std Dev	6.196

**Gaus mean : 30.6678**

**Gaus Width: 2.7392**



# B1L101S, U8-ch96, adc1

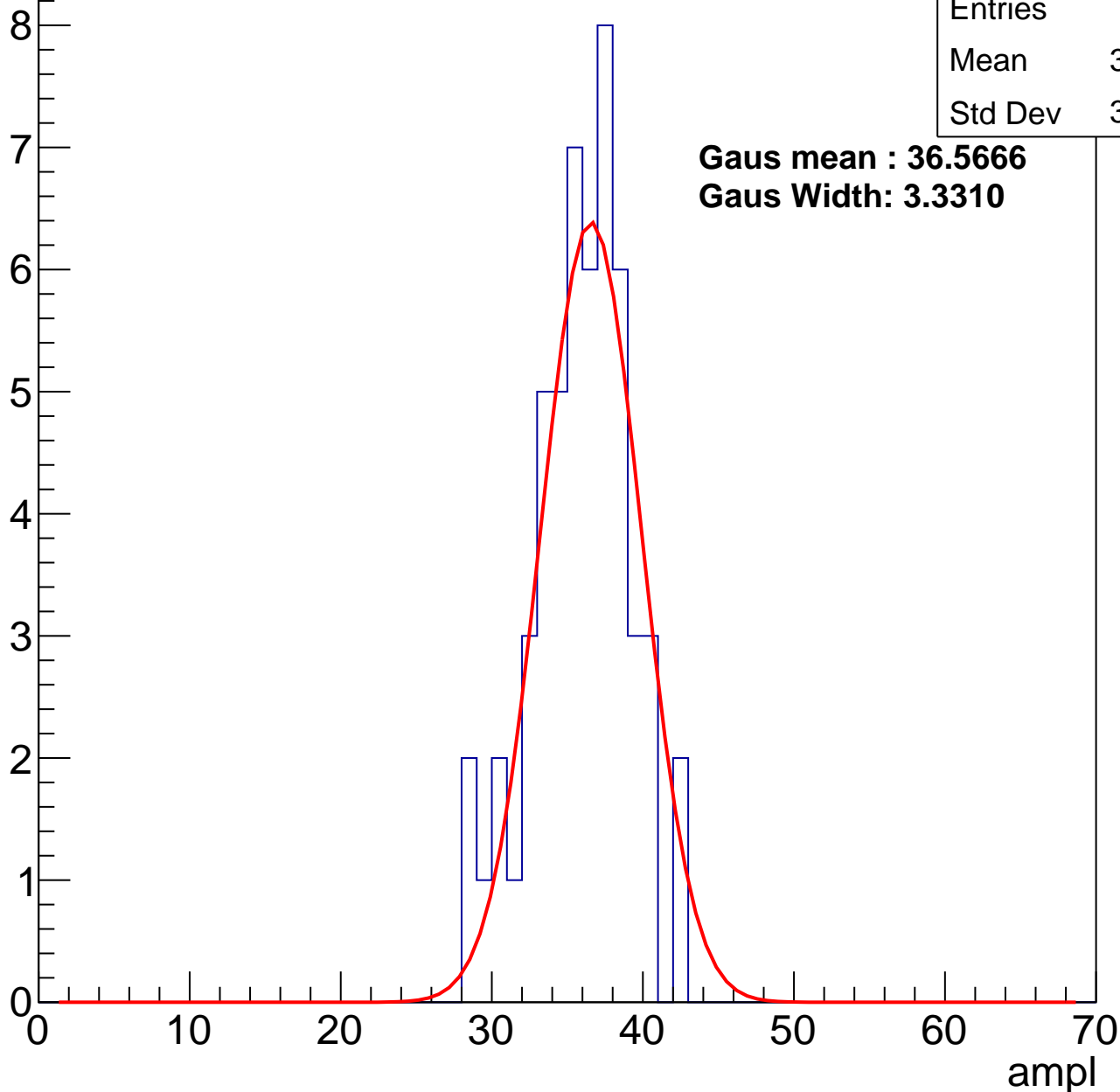
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	35.43
Std Dev	3.206

**Gaus mean : 36.5666**

**Gaus Width: 3.3310**



# B1L101S, U8-ch96, adc2

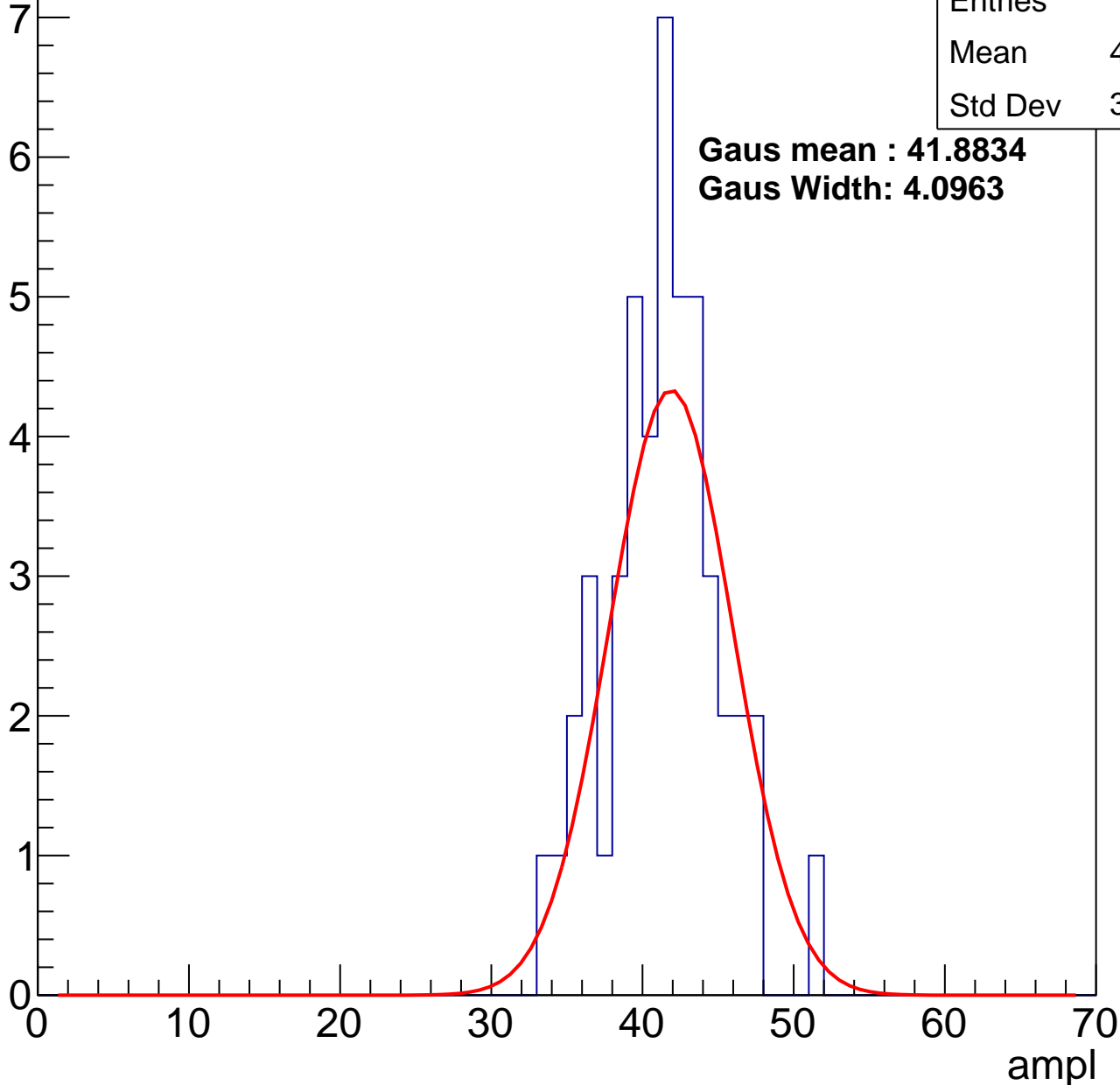
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	40.89
Std Dev	3.668

**Gaus mean : 41.8834**

**Gaus Width: 4.0963**



# B1L101S, U8-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

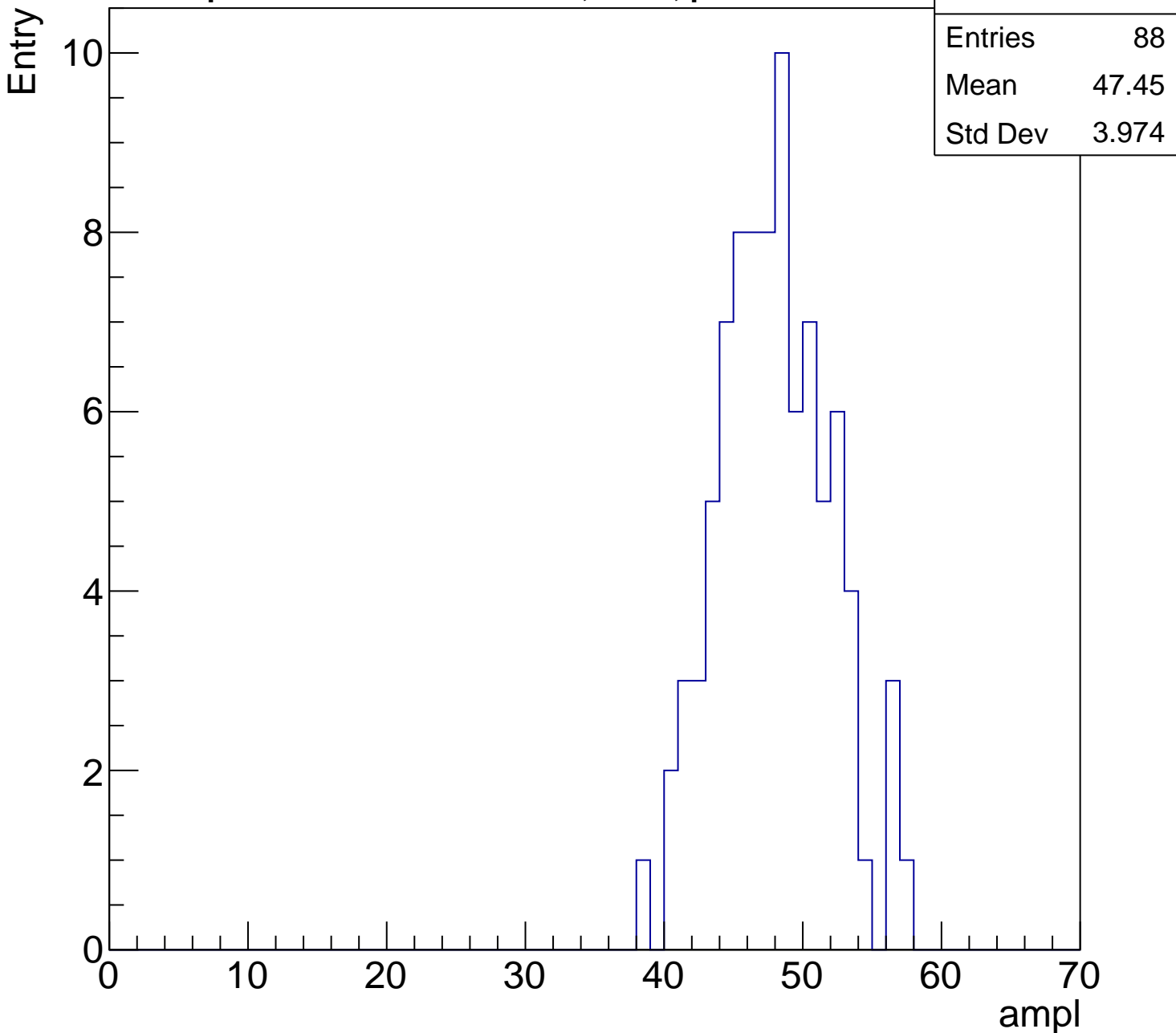
Entries	88
Mean	47.45
Std Dev	3.974

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

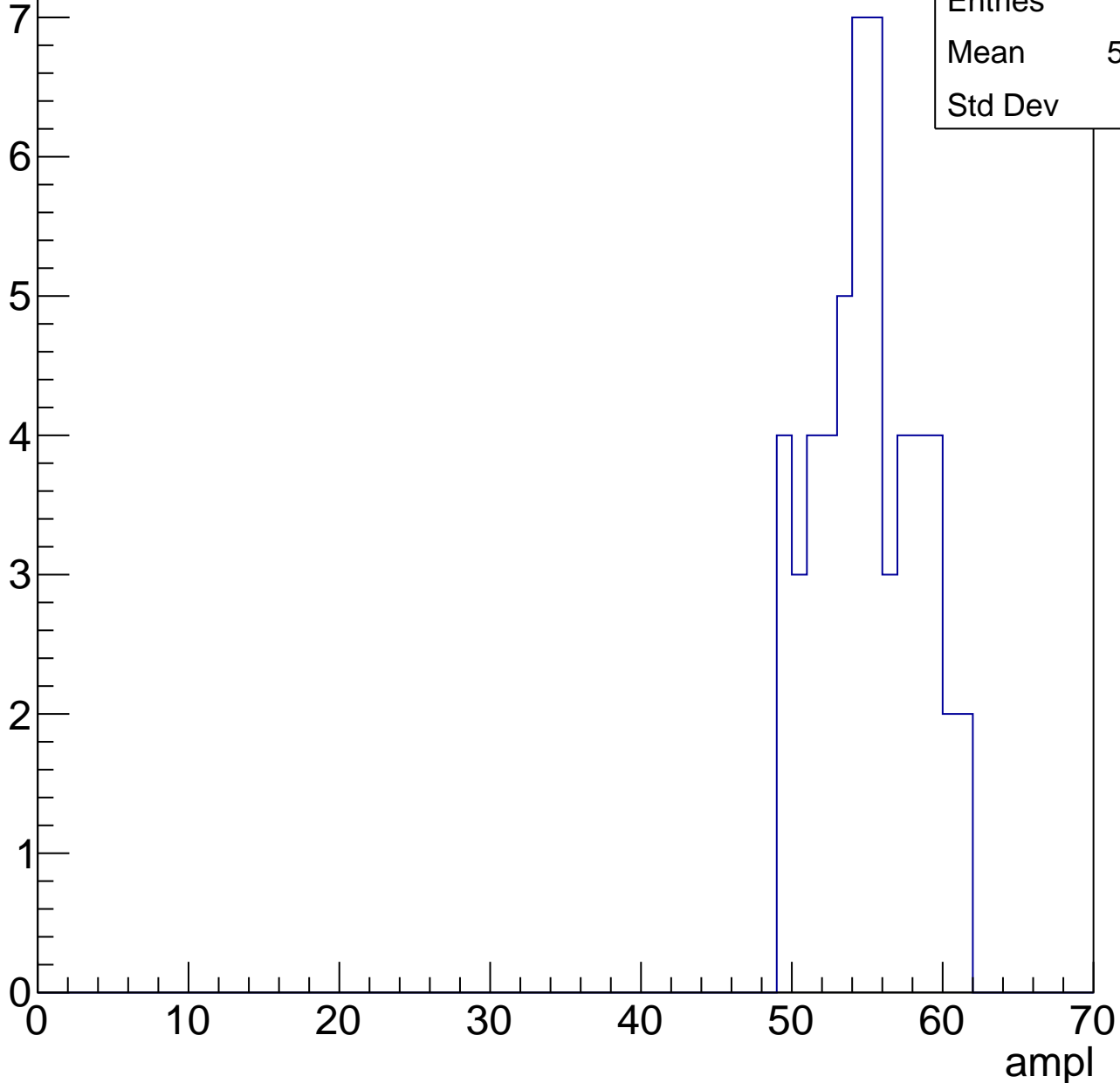


# B1L101S, U8-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

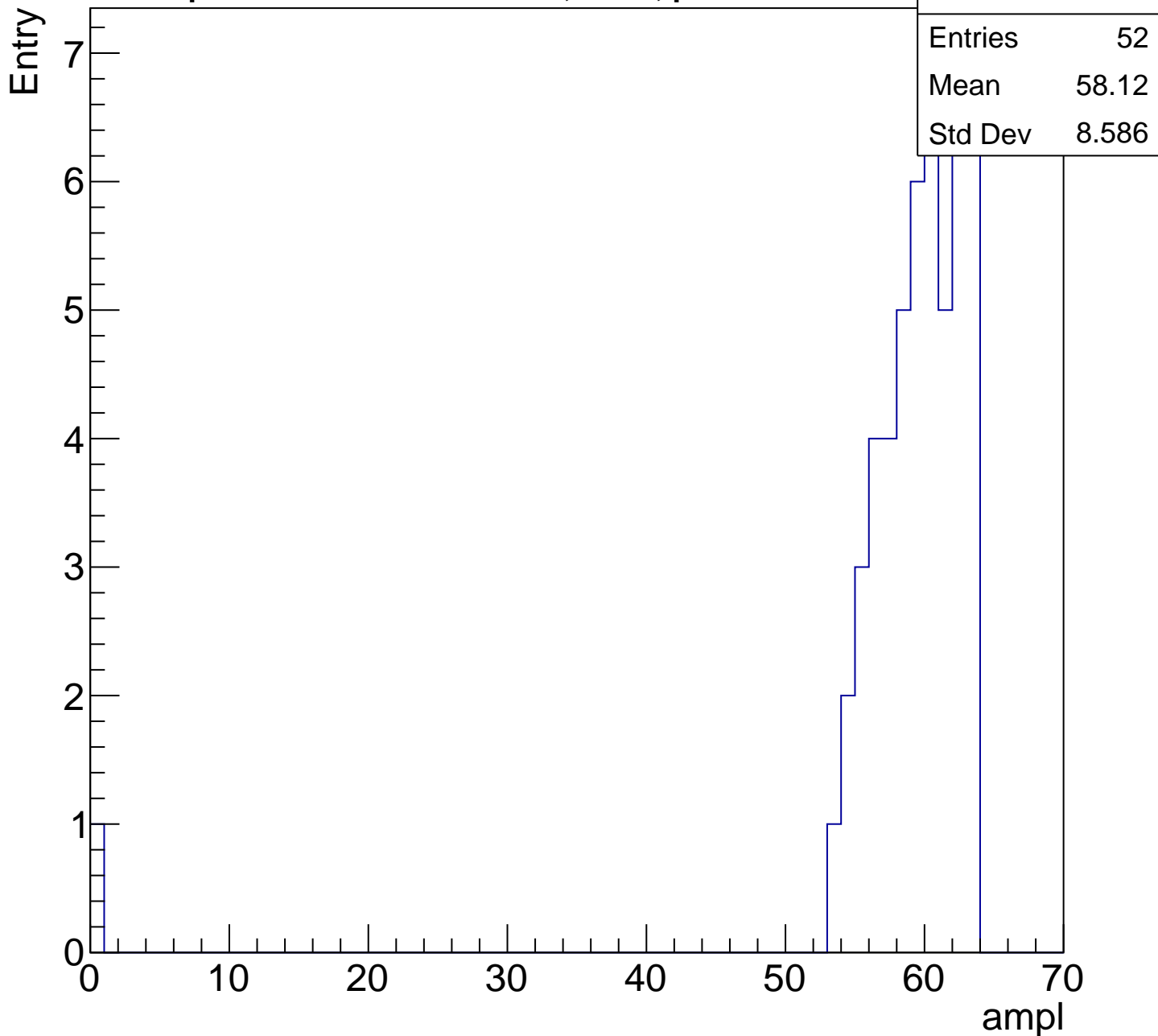
Entry

Entries	53
Mean	54.57
Std Dev	3.3



# B1L101S, U8-ch96, adc5

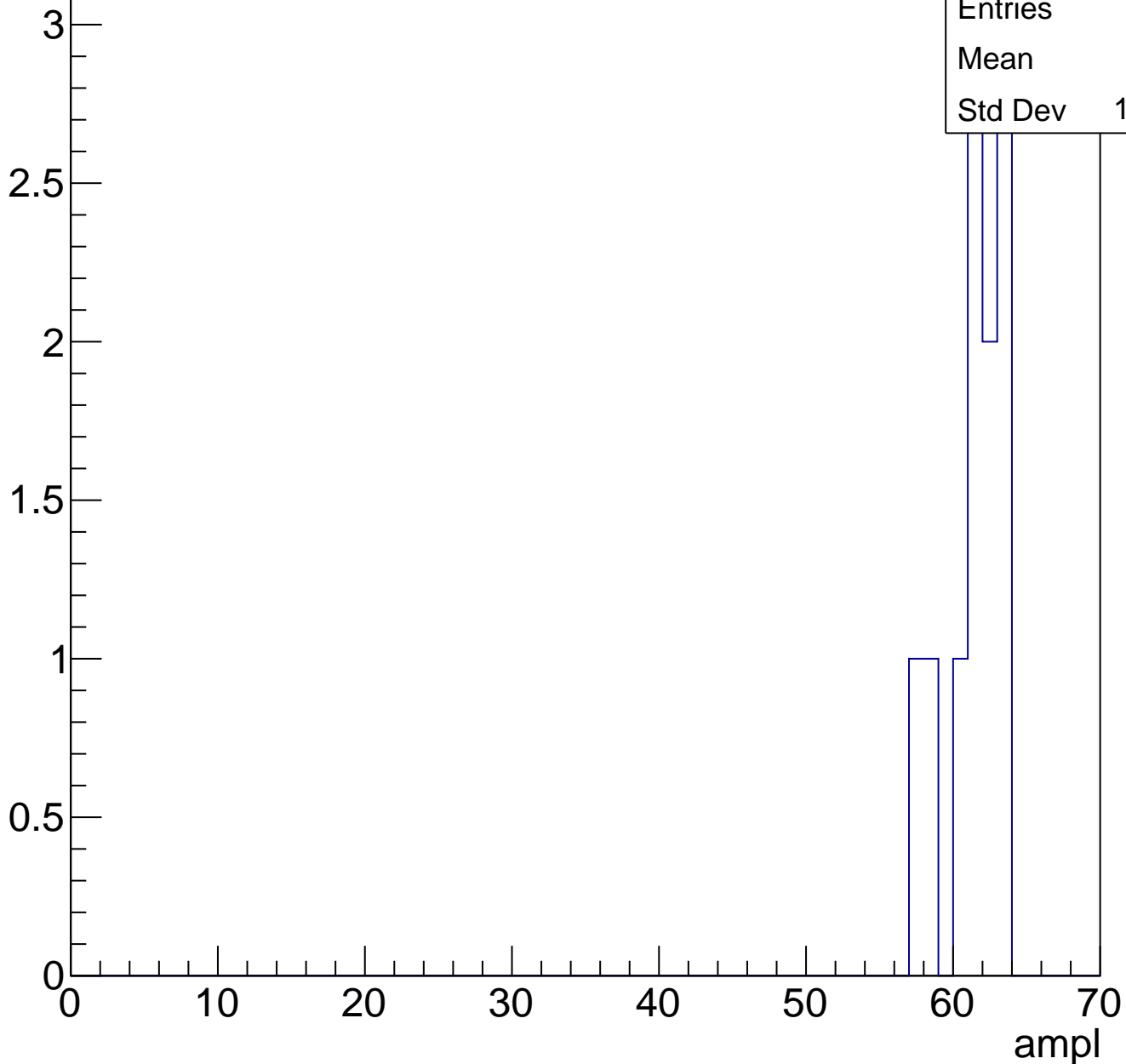
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U8-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

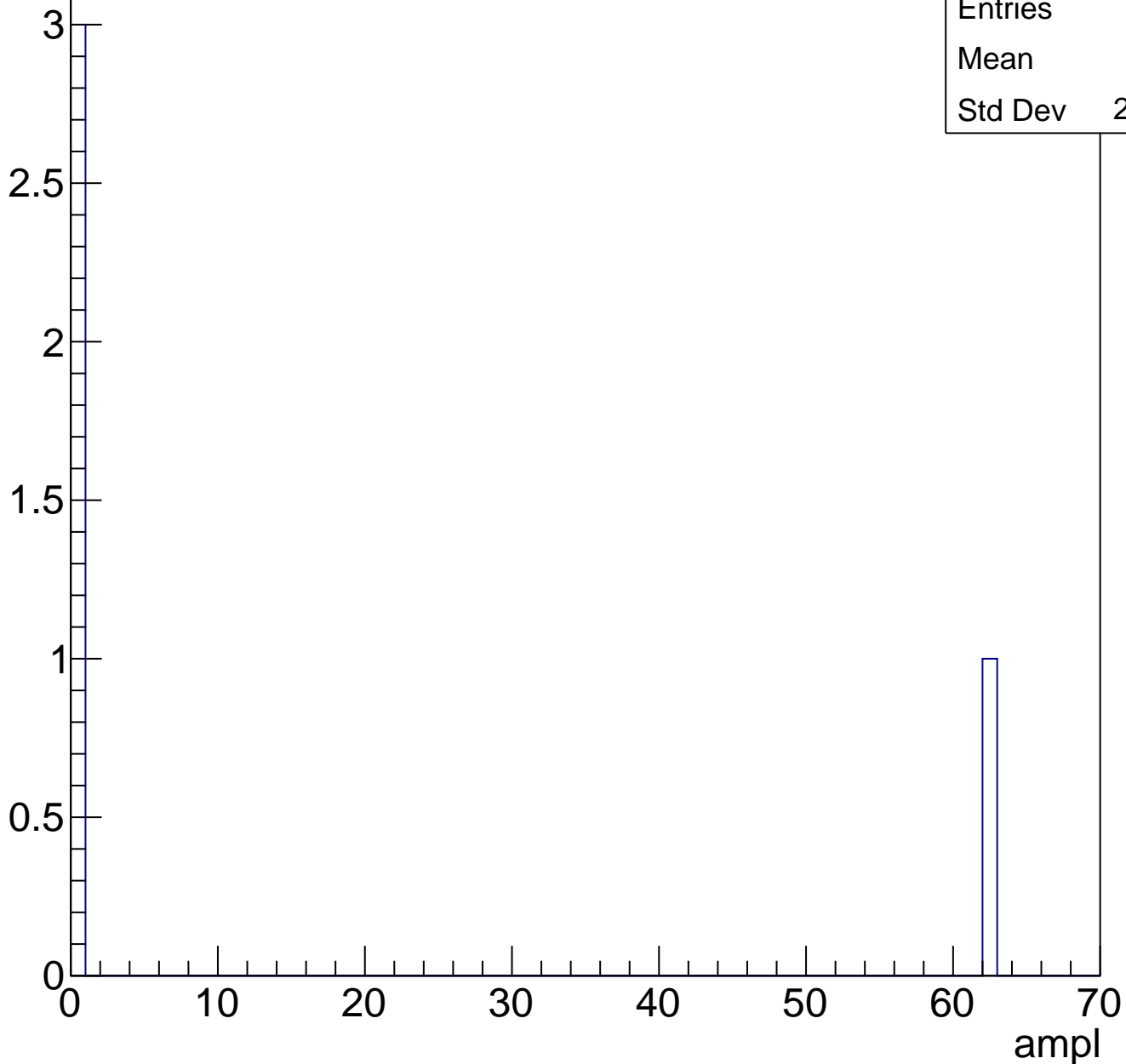




# B1L101S, U8-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch97, adc0

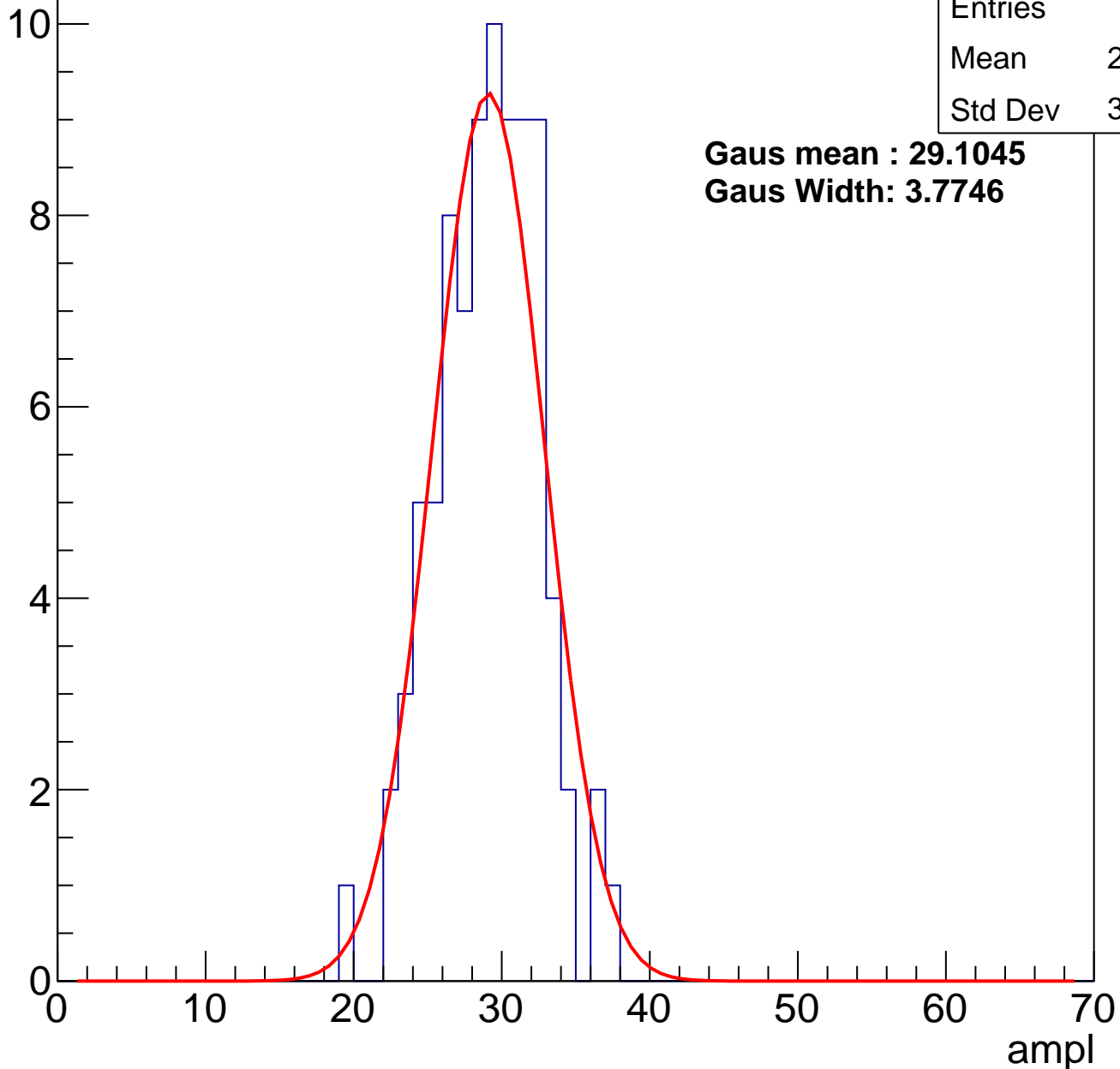
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	86
Mean	28.63
Std Dev	3.427

**Gaus mean : 29.1045**

**Gaus Width: 3.7746**

Entry



# B1L101S, U8-ch97, adc1

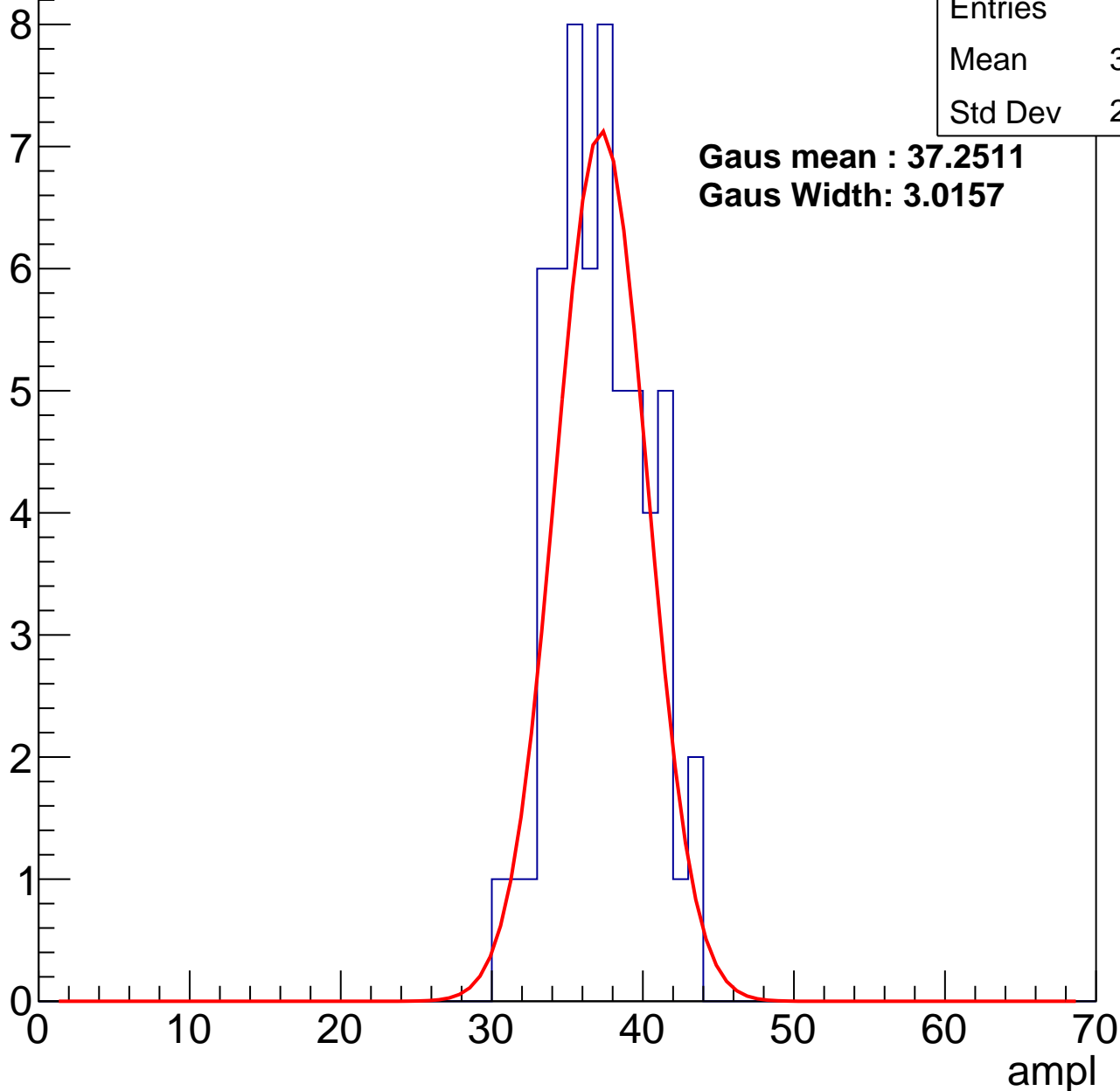
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	36.69
Std Dev	2.999

**Gaus mean : 37.2511**

**Gaus Width: 3.0157**



# B1L101S, U8-ch97, adc2

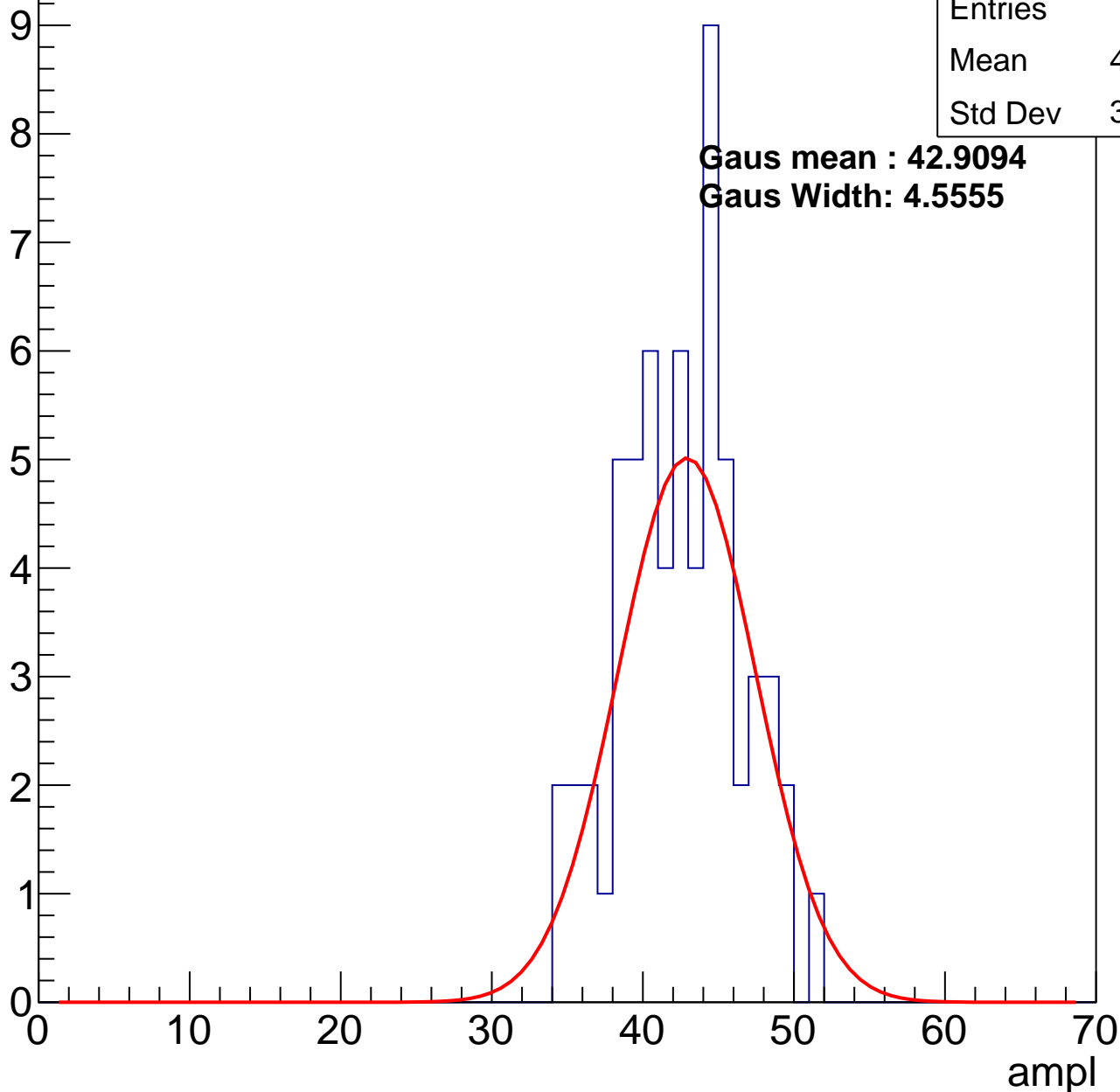
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	42.05
Std Dev	3.924

**Gaus mean : 42.9094**

**Gaus Width: 4.5555**

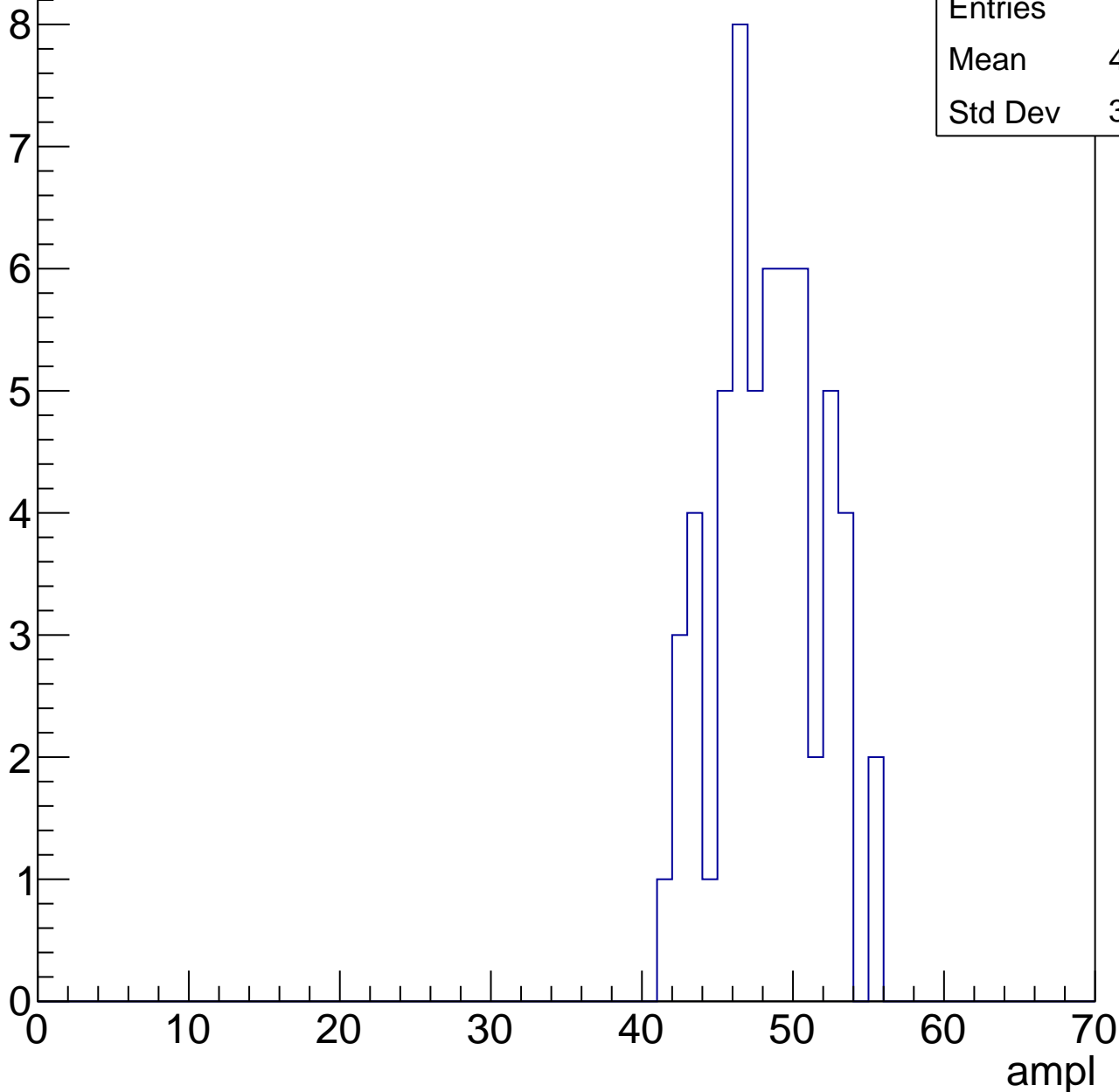


# B1L101S, U8-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	47.88
Std Dev	3.424

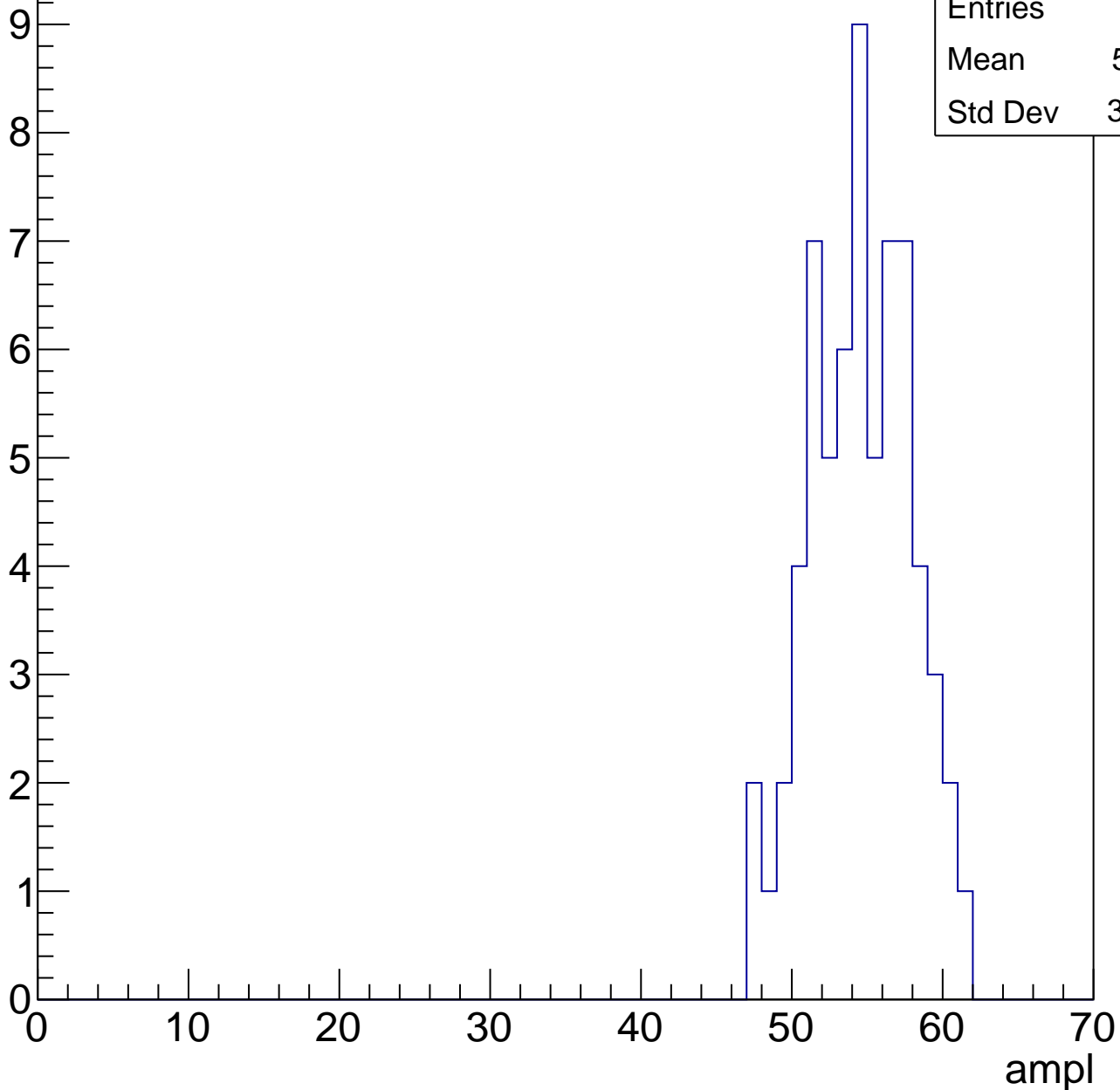


# B1L101S, U8-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	54.11
Std Dev	3.263



# B1L101S, U8-ch97, adc5

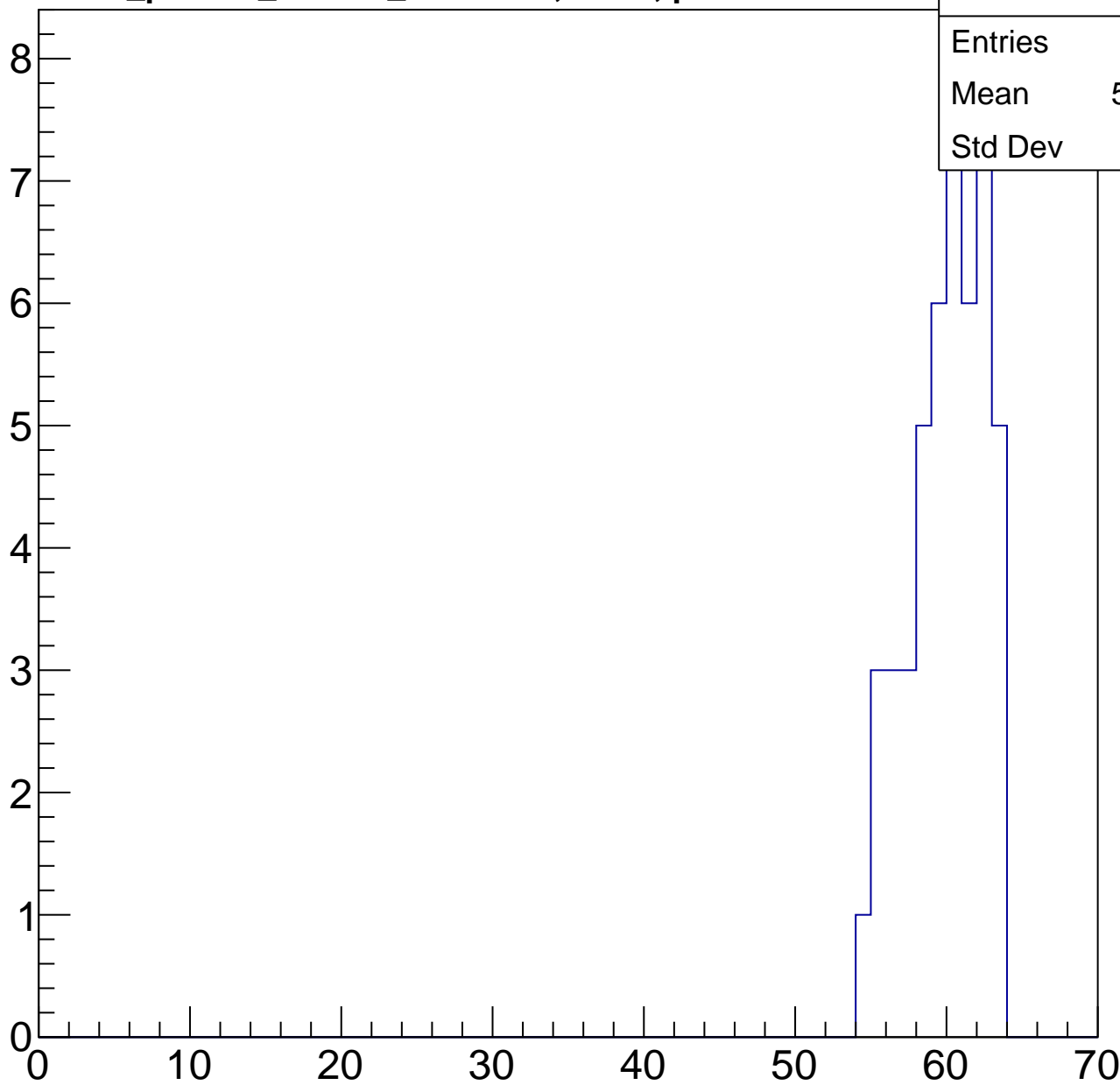
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	59.56
Std Dev	2.44

ampl

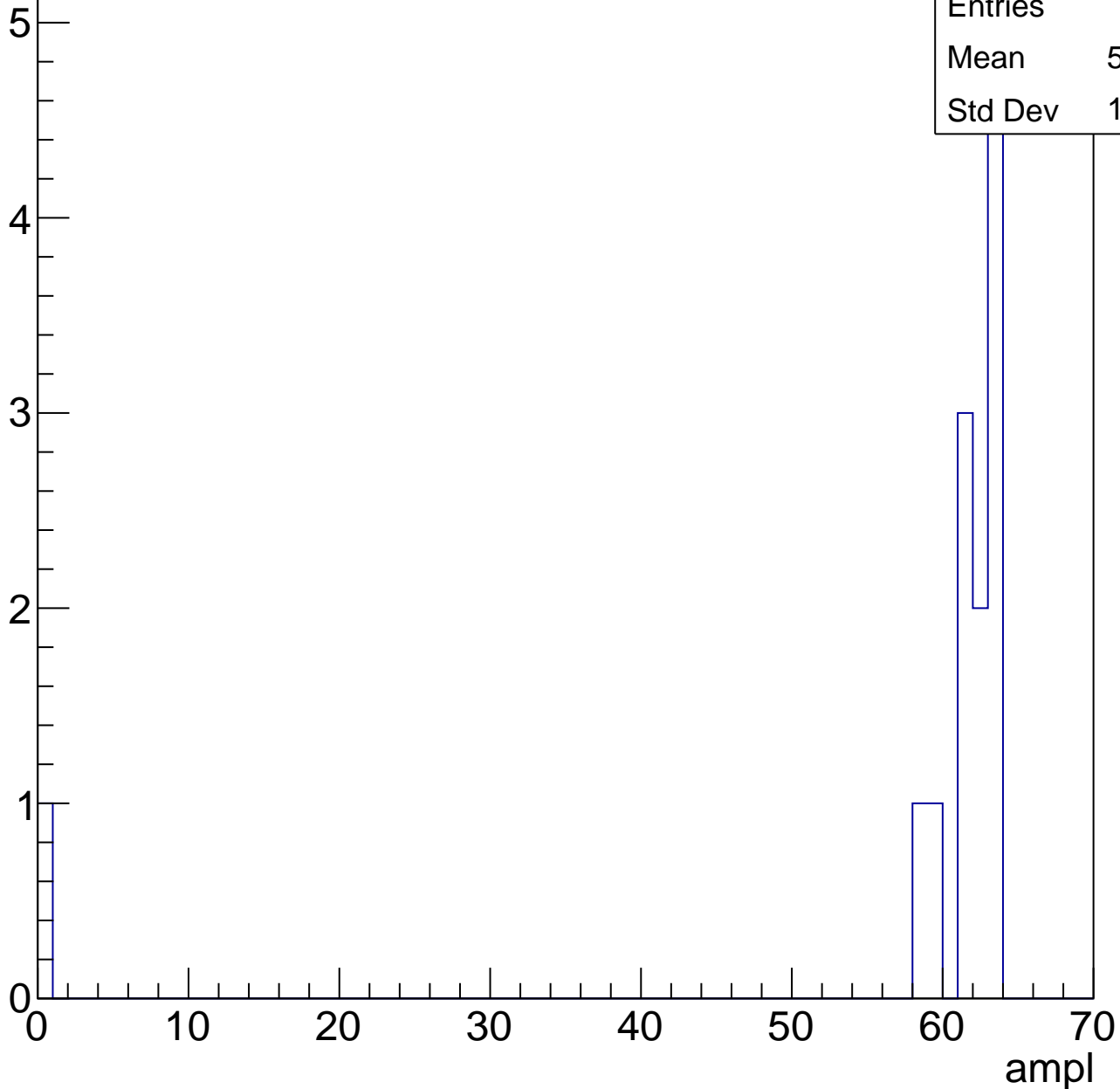


# B1L101S, U8-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	13
Mean	56.85
Std Dev	16.48





# B1L101S, U8-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch98, adc0

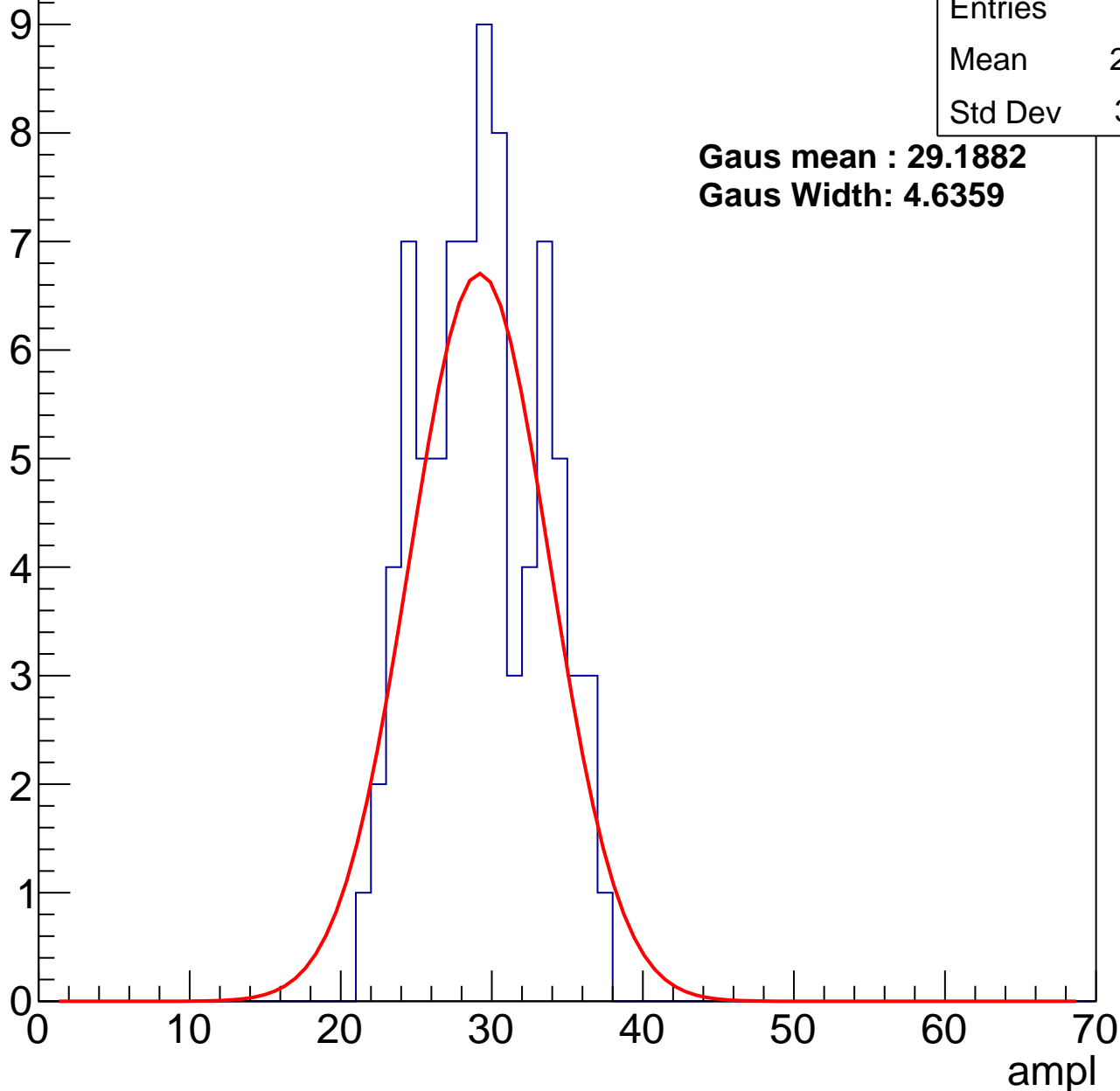
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	28.86
Std Dev	3.931

**Gaus mean : 29.1882**

**Gaus Width: 4.6359**



# B1L101S, U8-ch98, adc1

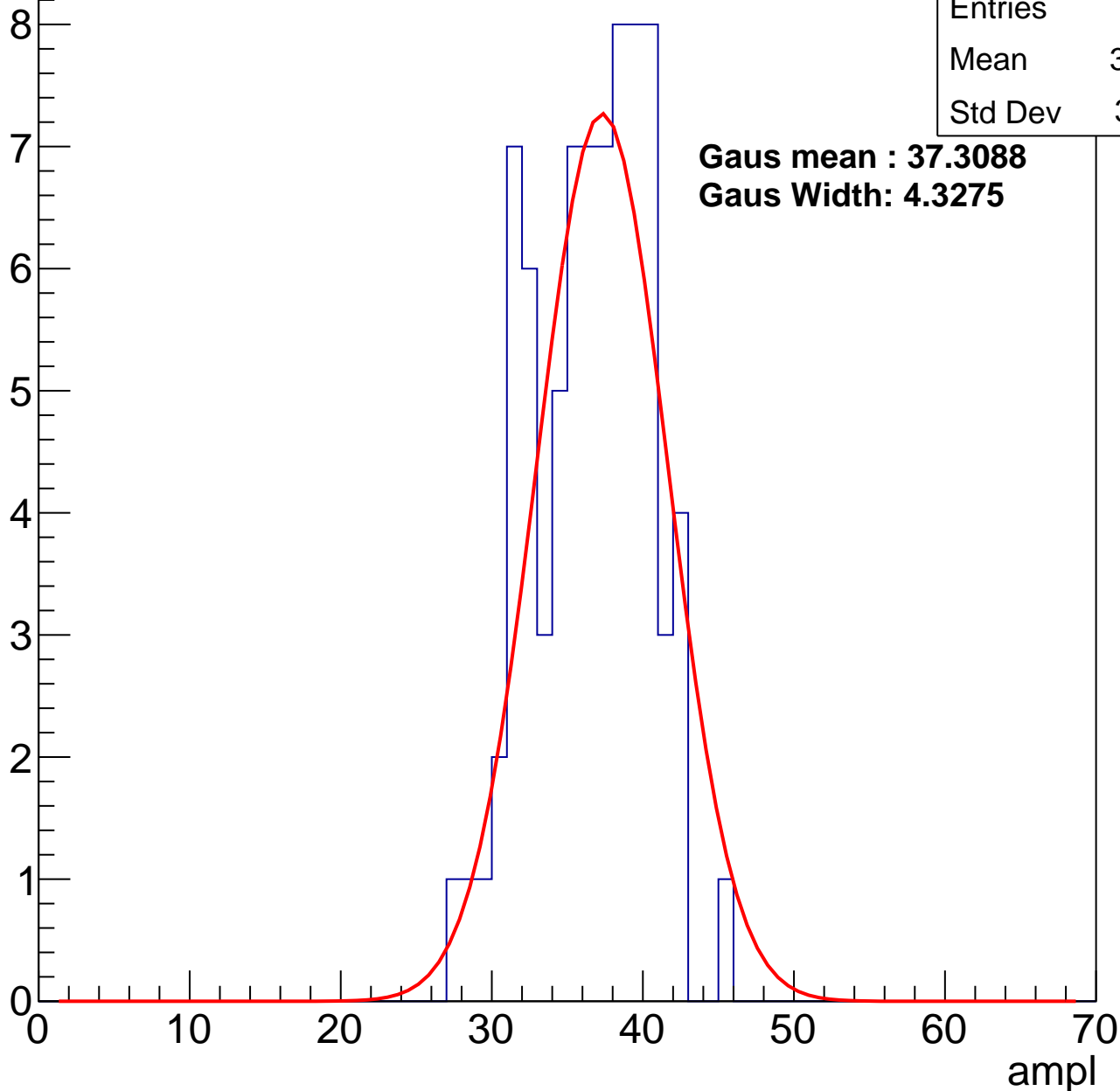
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	36.08
Std Dev	3.781

**Gaus mean : 37.3088**

**Gaus Width: 4.3275**

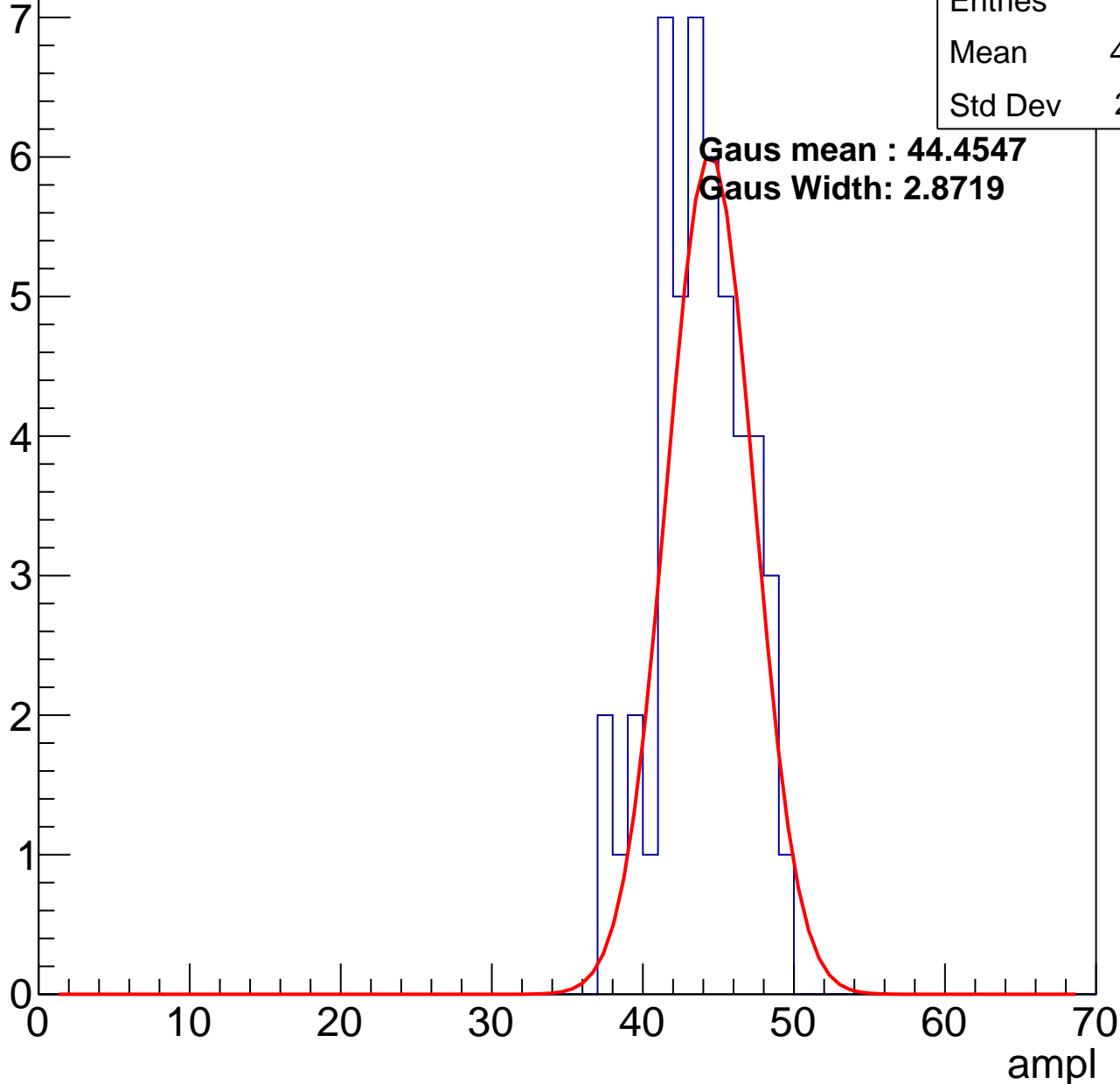


# B1L101S, U8-ch98, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

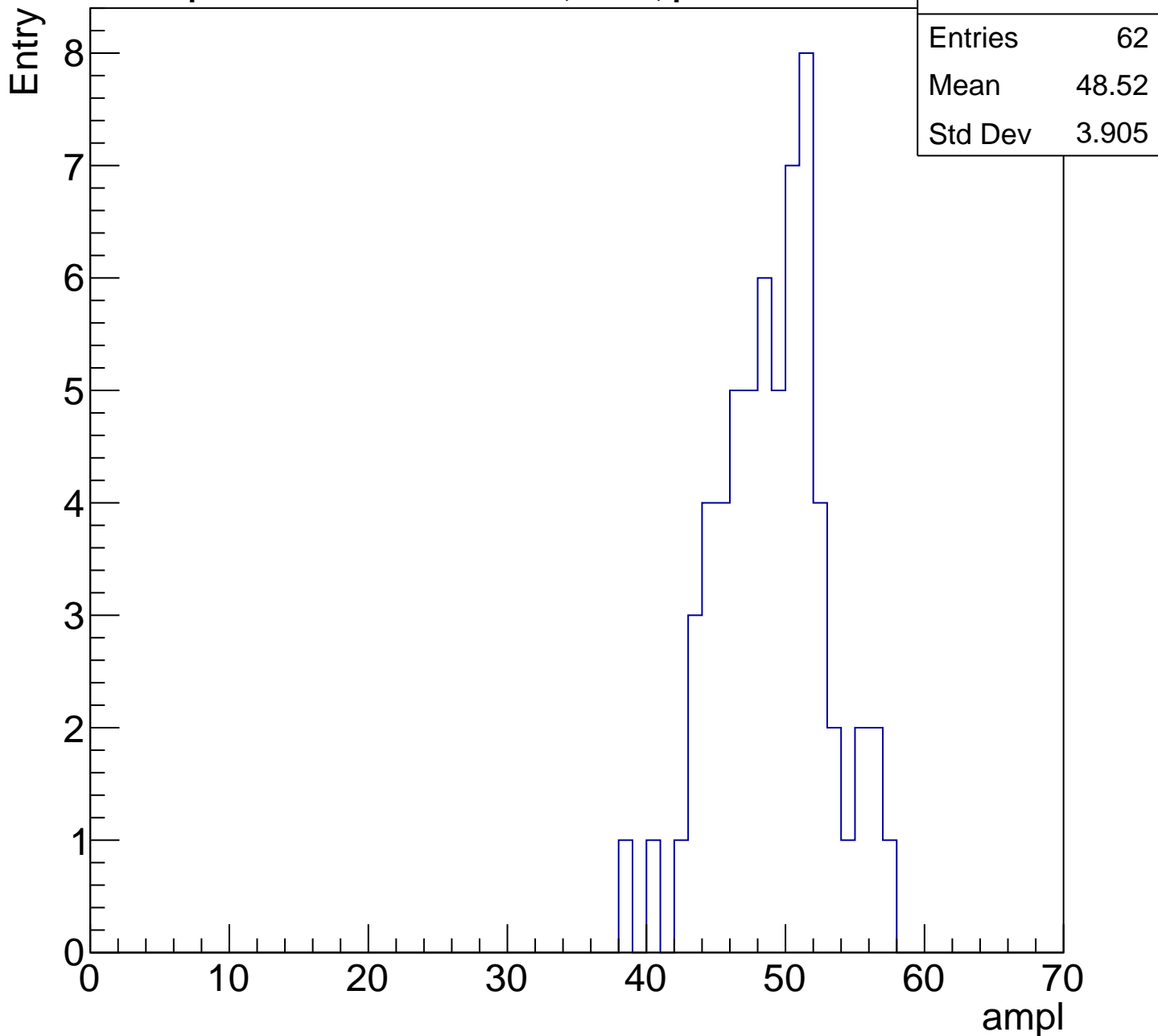
Entry

Entries	48
Mean	43.38
Std Dev	2.891



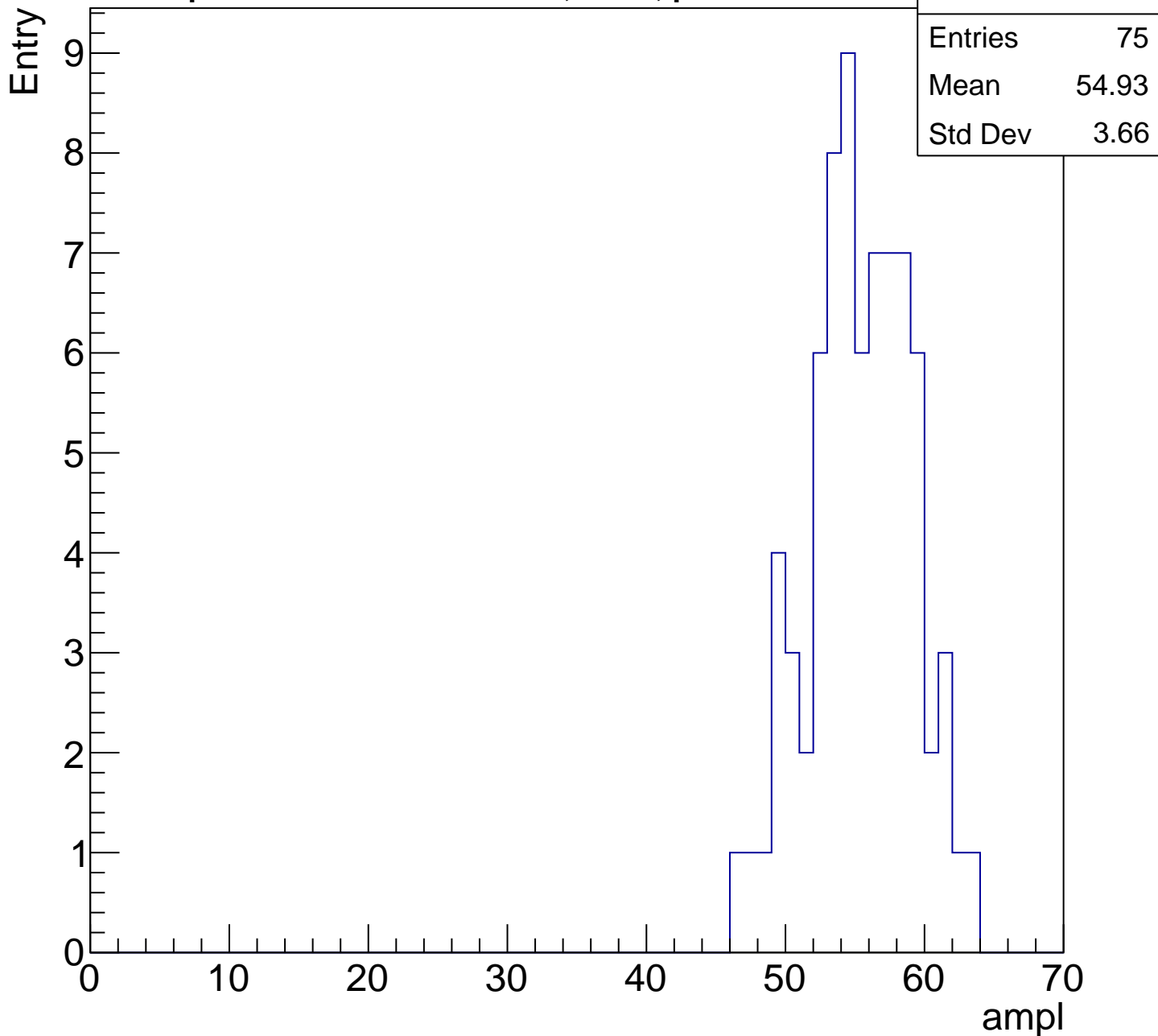
# B1L101S, U8-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U8-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U8-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

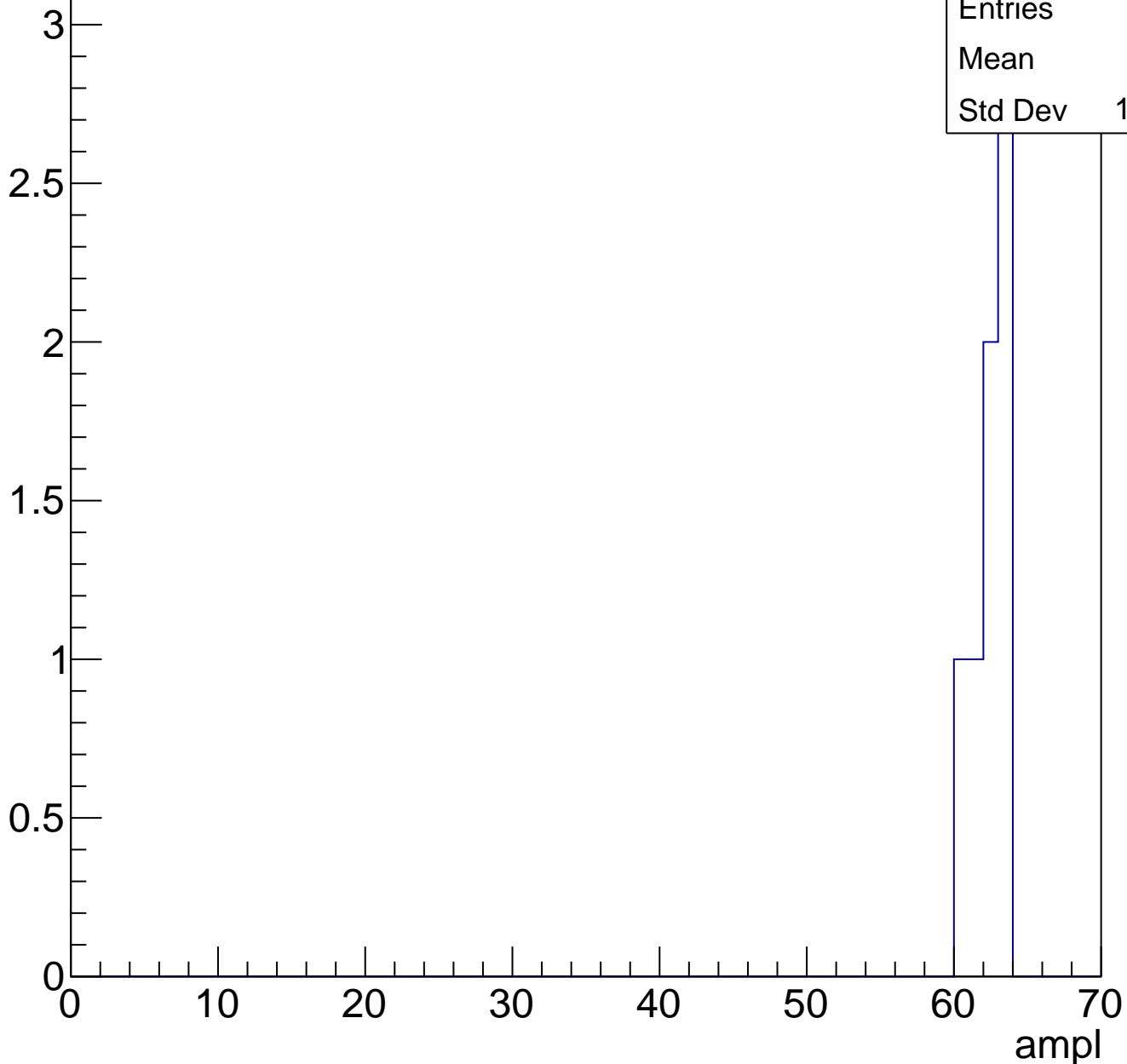
Entries	37
Mean	58.49
Std Dev	9.991

ampl

# B1L101S, U8-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



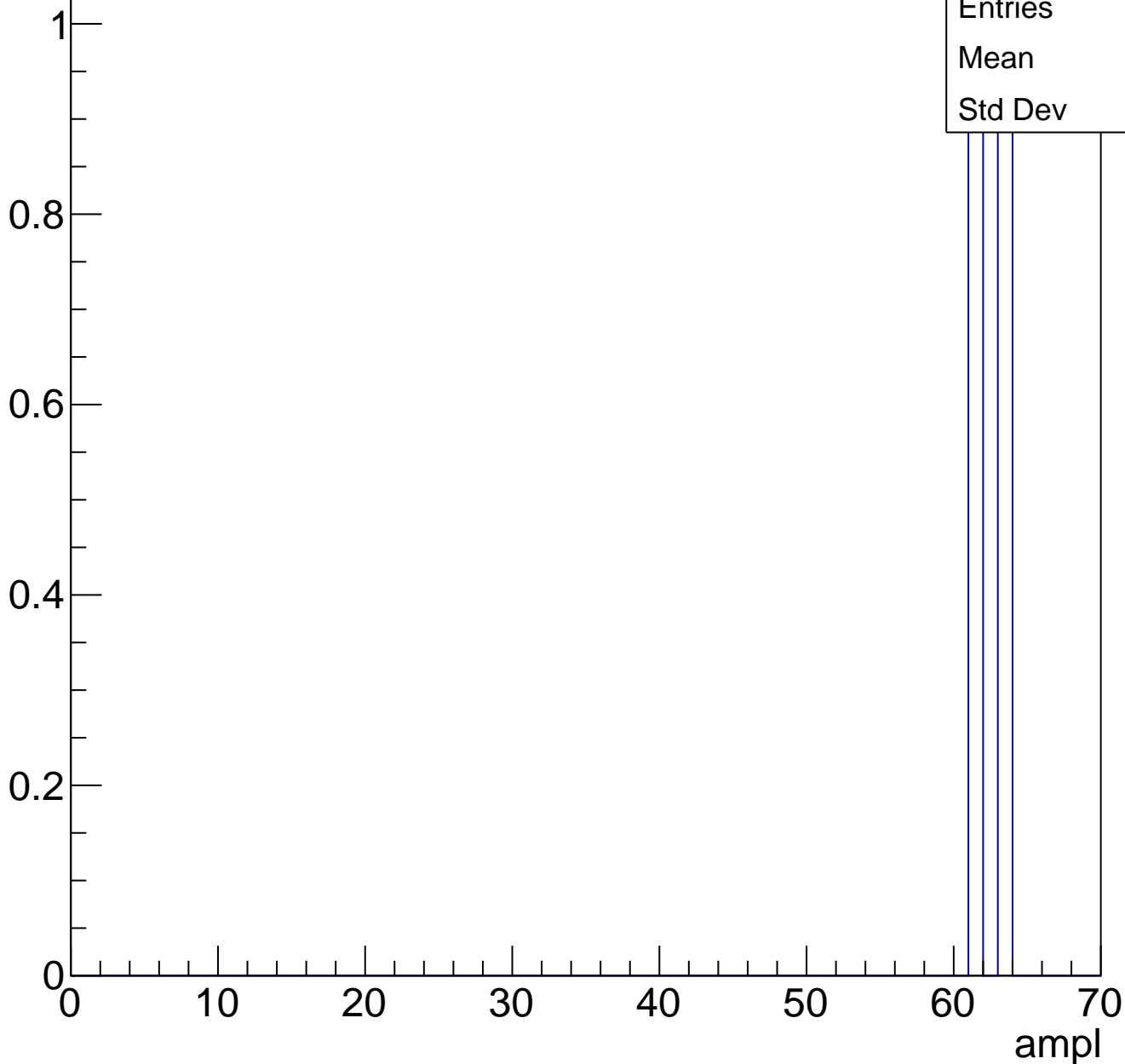
Entries	7
Mean	62
Std Dev	1.069



# B1L101S, U8-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch99, adc0

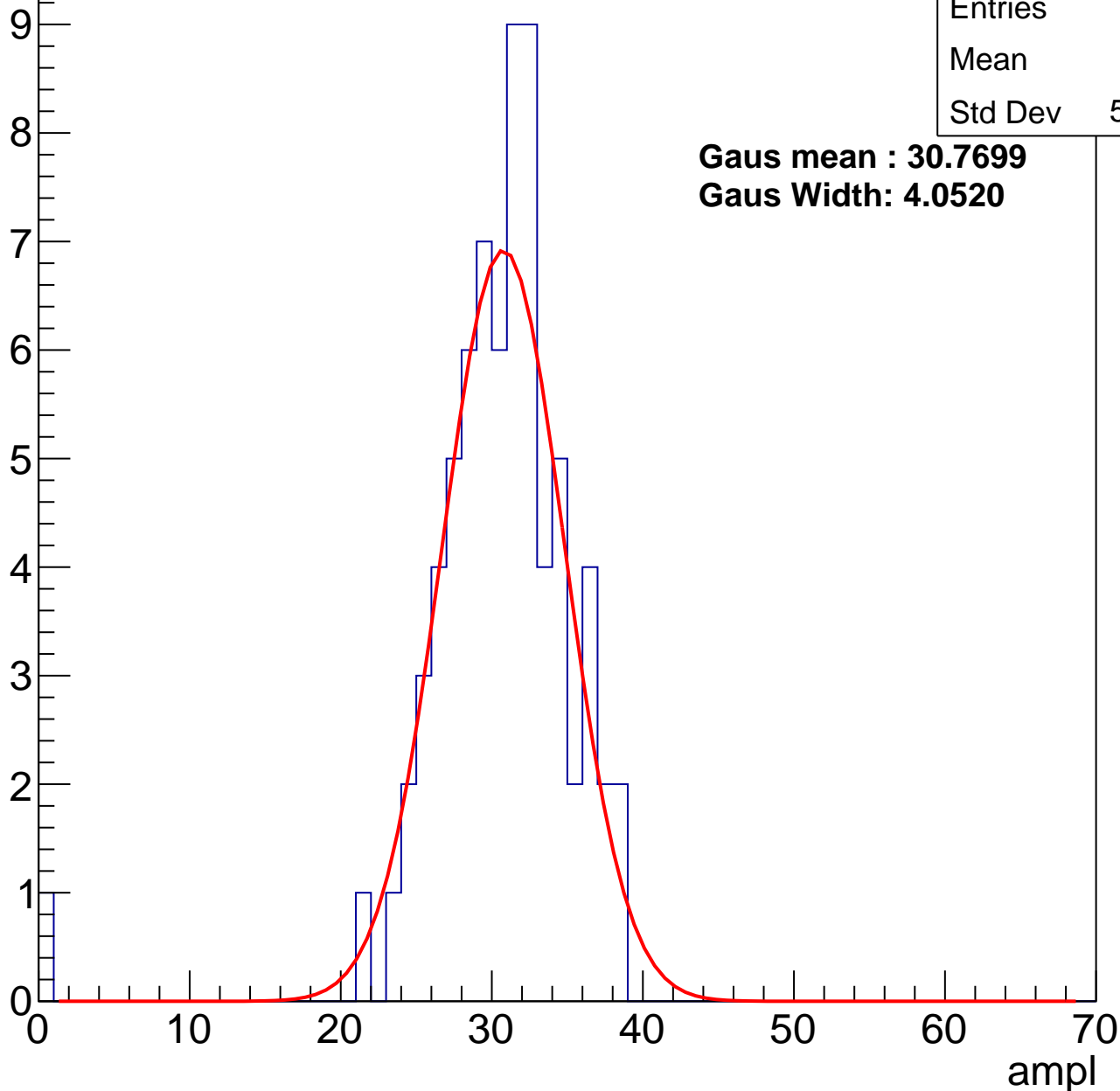
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	30
Std Dev	5.099

**Gaus mean : 30.7699**

**Gaus Width: 4.0520**



# B1L101S, U8-ch99, adc1

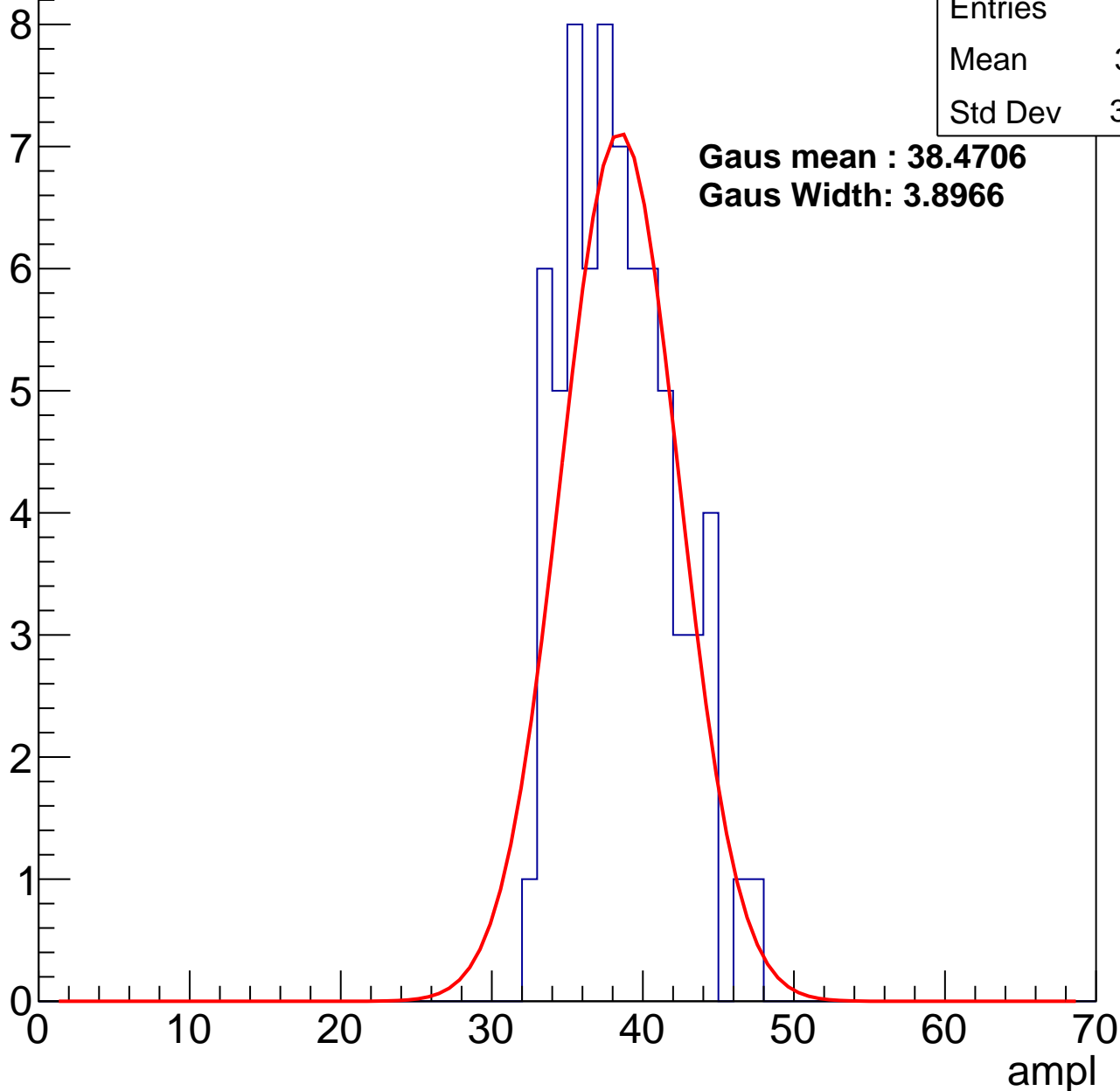
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	38.01
Std Dev	3.499

**Gaus mean : 38.4706**

**Gaus Width: 3.8966**



# B1L101S, U8-ch99, adc2

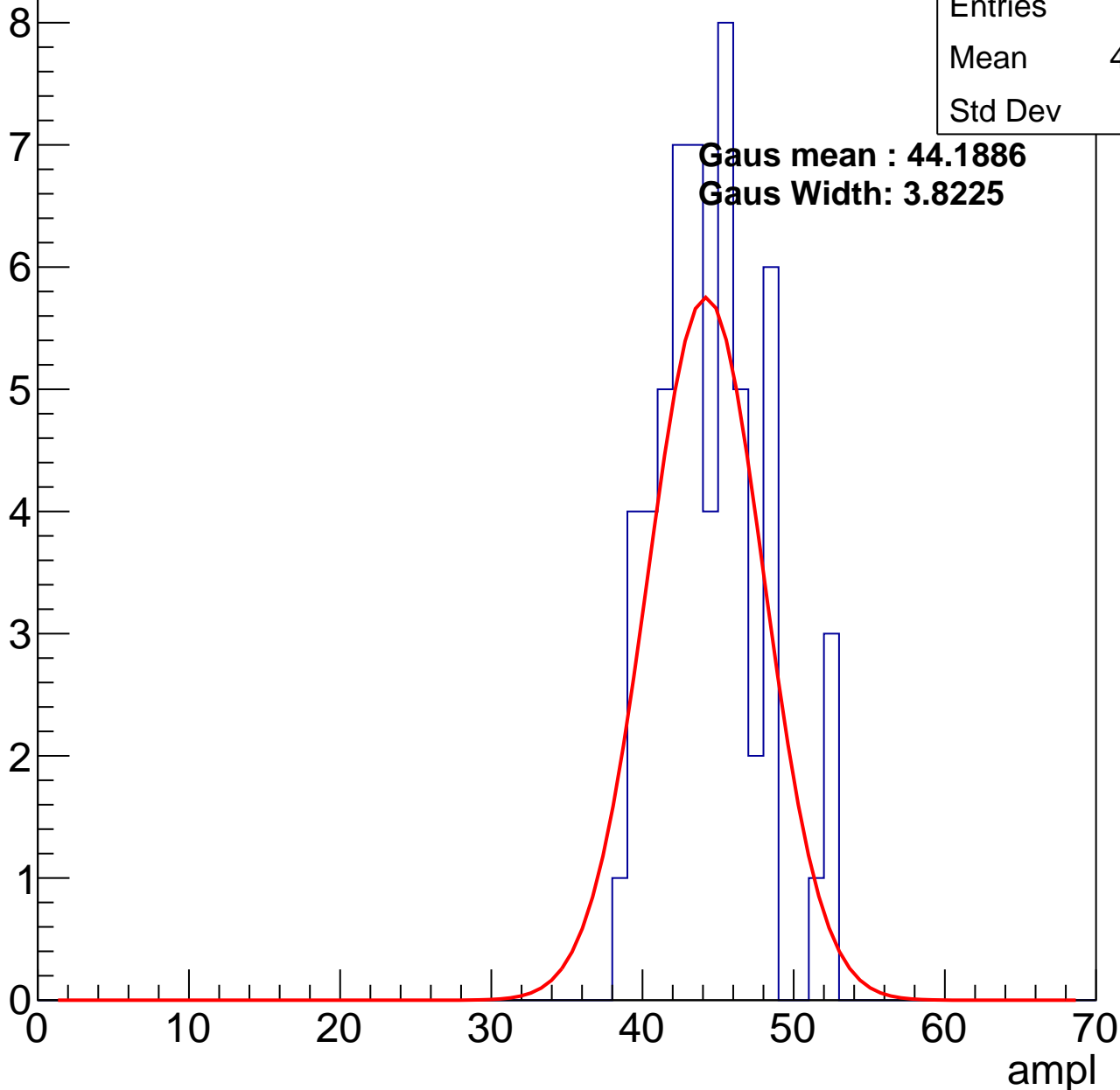
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	44.02
Std Dev	3.41

**Gaus mean : 44.1886**

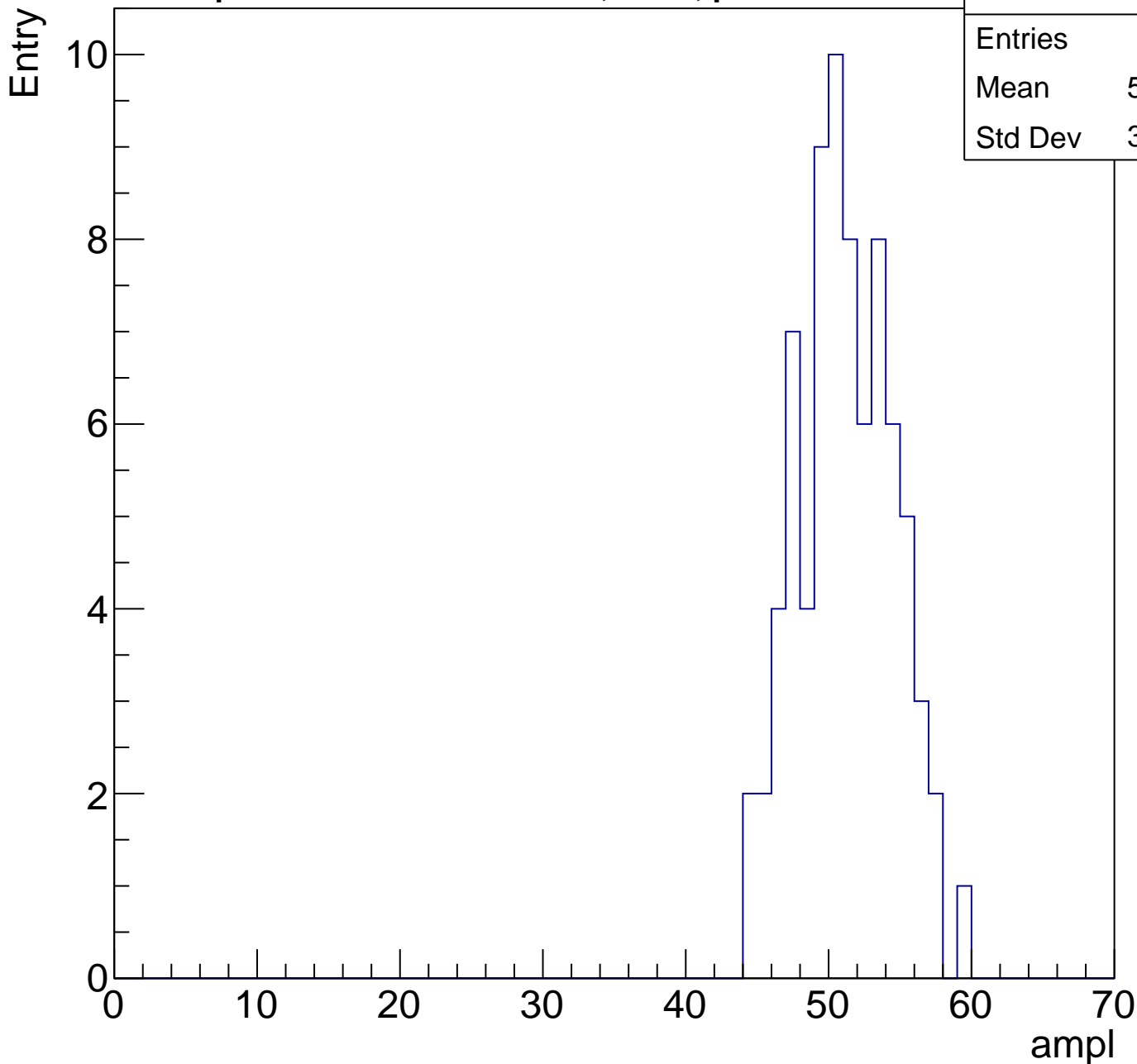
**Gaus Width: 3.8225**



# B1L101S, U8-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

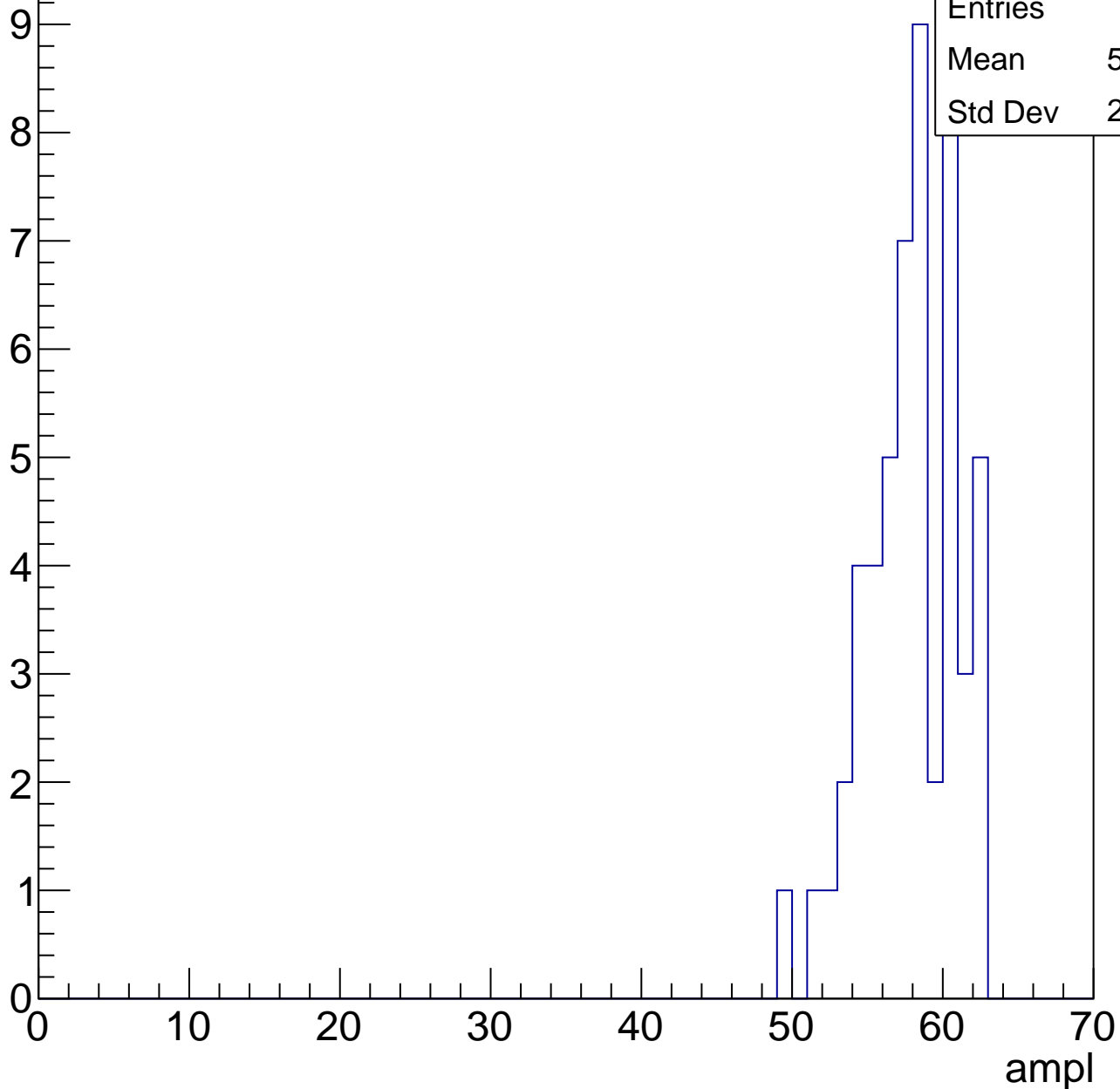
Entries	77
Mean	50.75
Std Dev	3.307



# B1L101S, U8-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



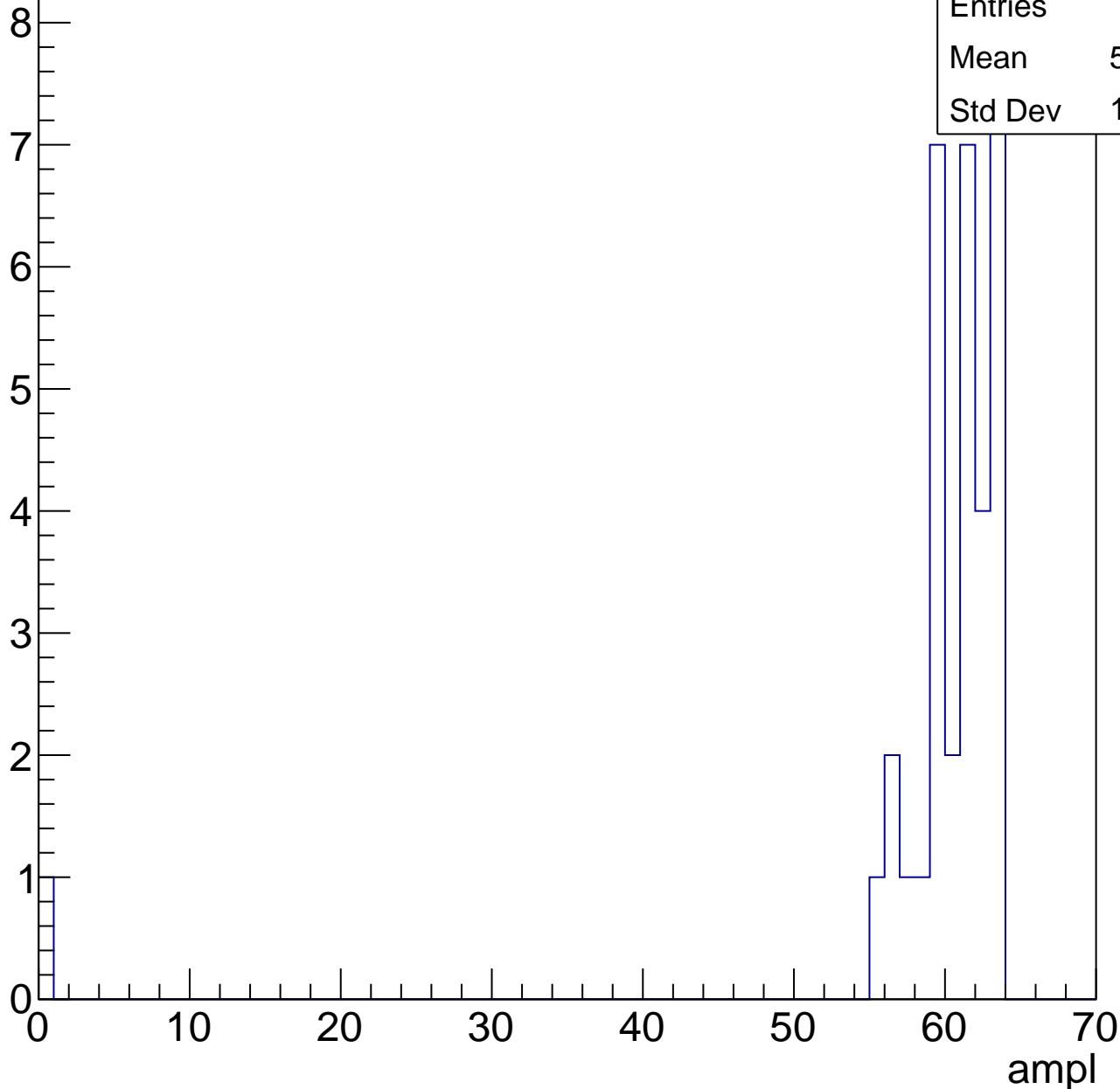
Entries	52
Mean	57.42
Std Dev	2.996

# B1L101S, U8-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	34
Mean	58.65
Std Dev	10.45



# B1L101S, U8-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U8-ch100, adc0

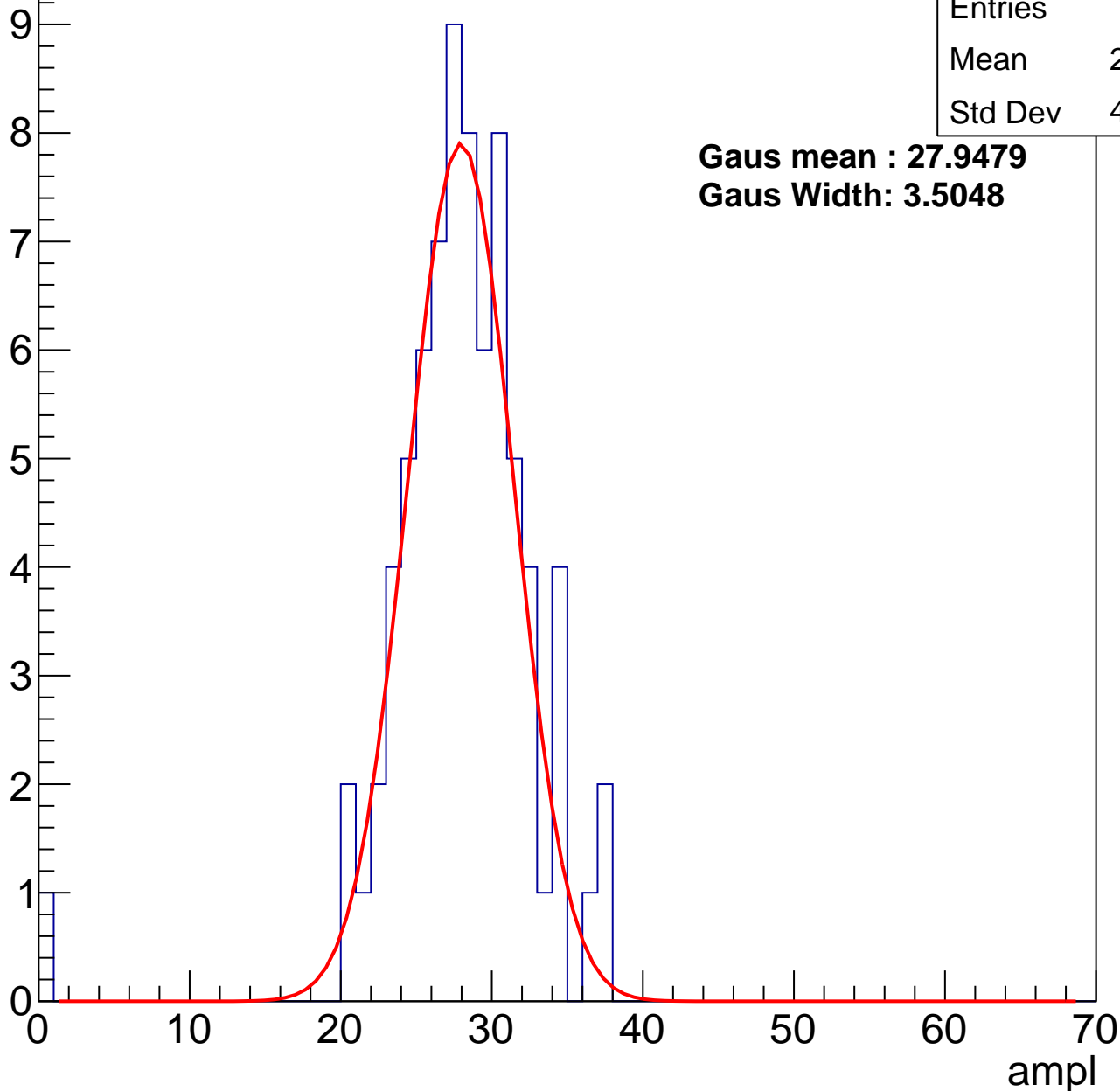
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	27.53
Std Dev	4.906

**Gaus mean : 27.9479**

**Gaus Width: 3.5048**



# B1L101S, U8-ch100, adc1

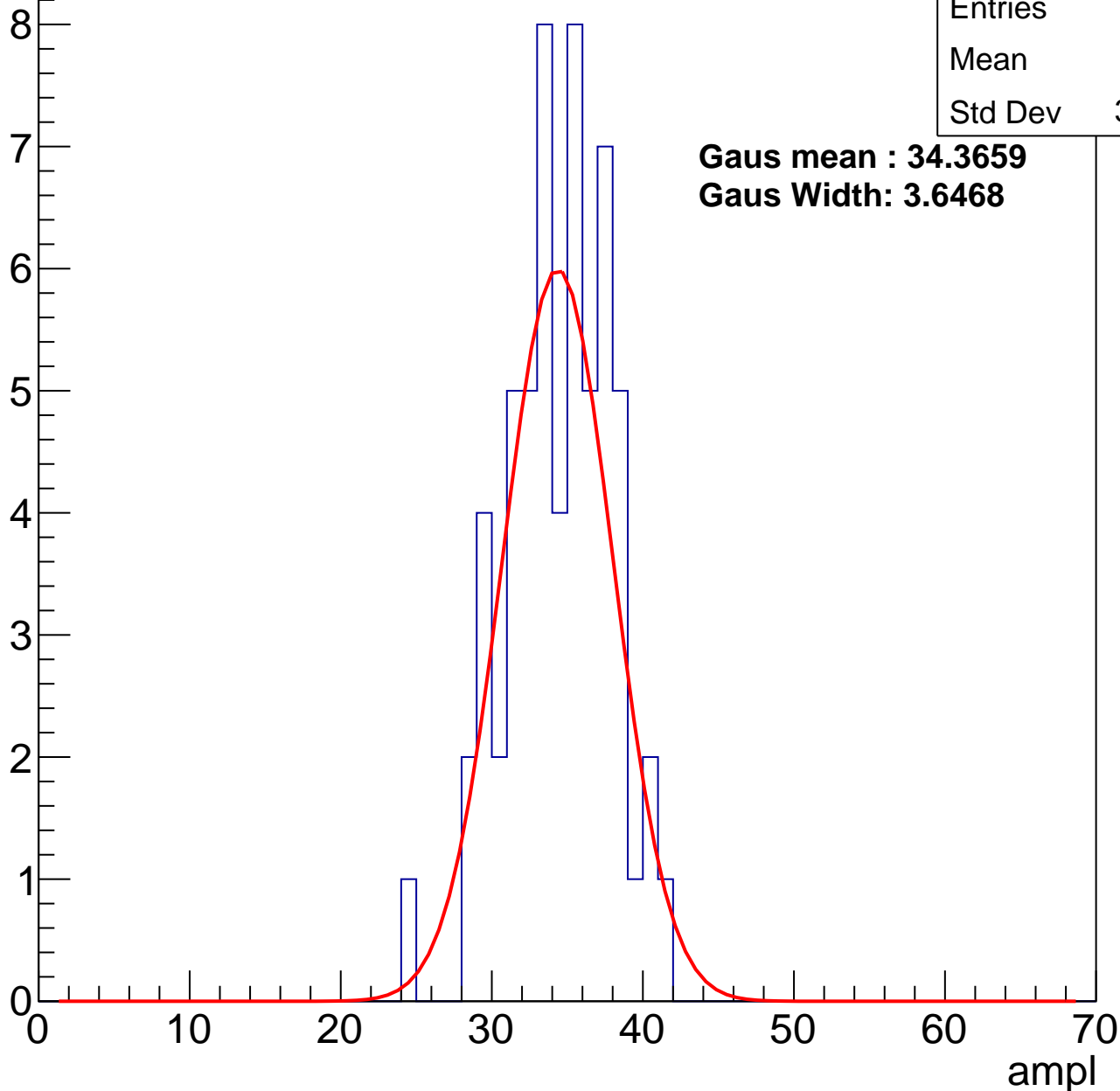
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	34
Std Dev	3.401

**Gaus mean : 34.3659**

**Gaus Width: 3.6468**



# B1L101S, U8-ch100, adc2

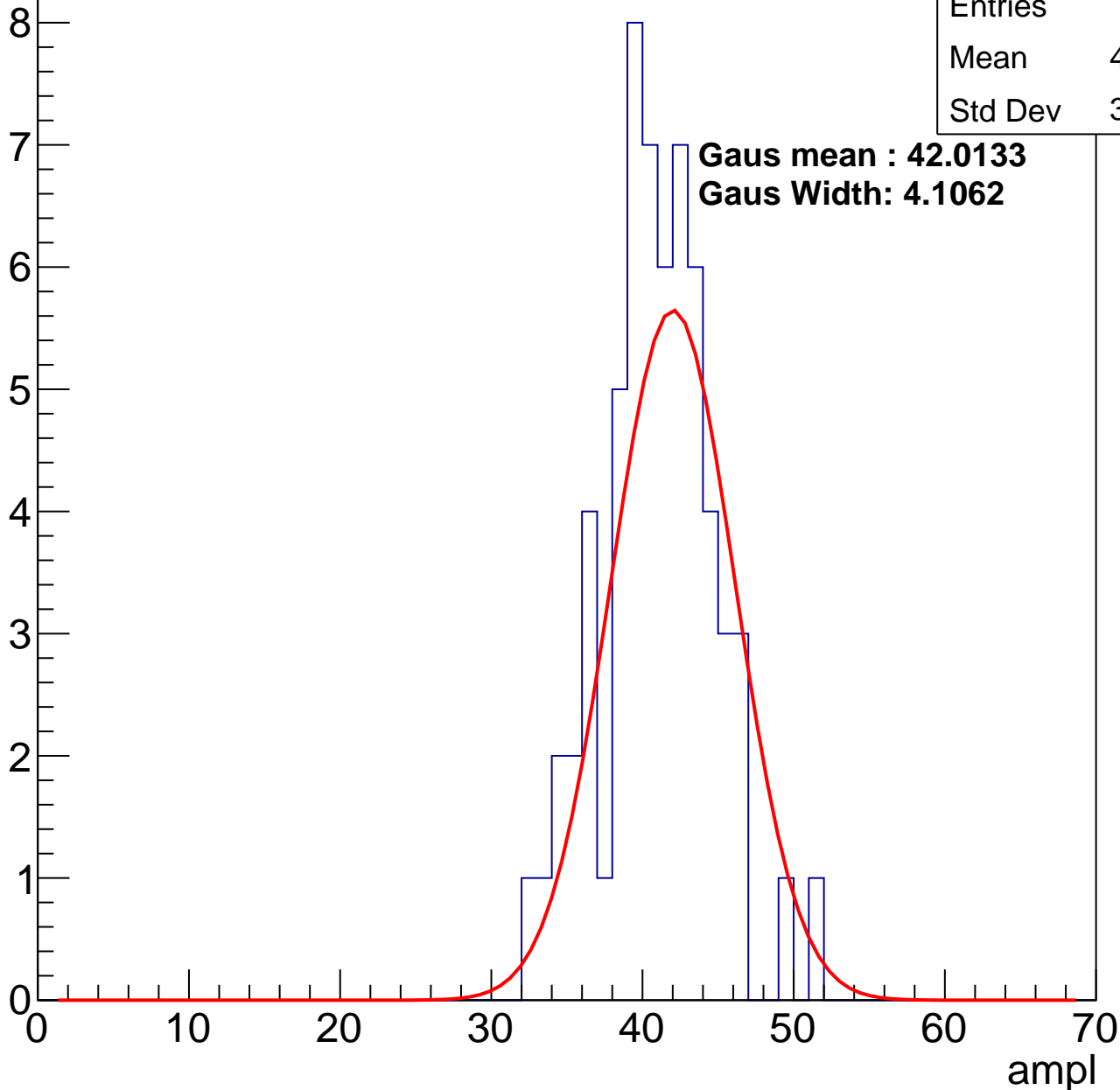
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	40.53
Std Dev	3.714

**Gaus mean : 42.0133**

**Gaus Width: 4.1062**

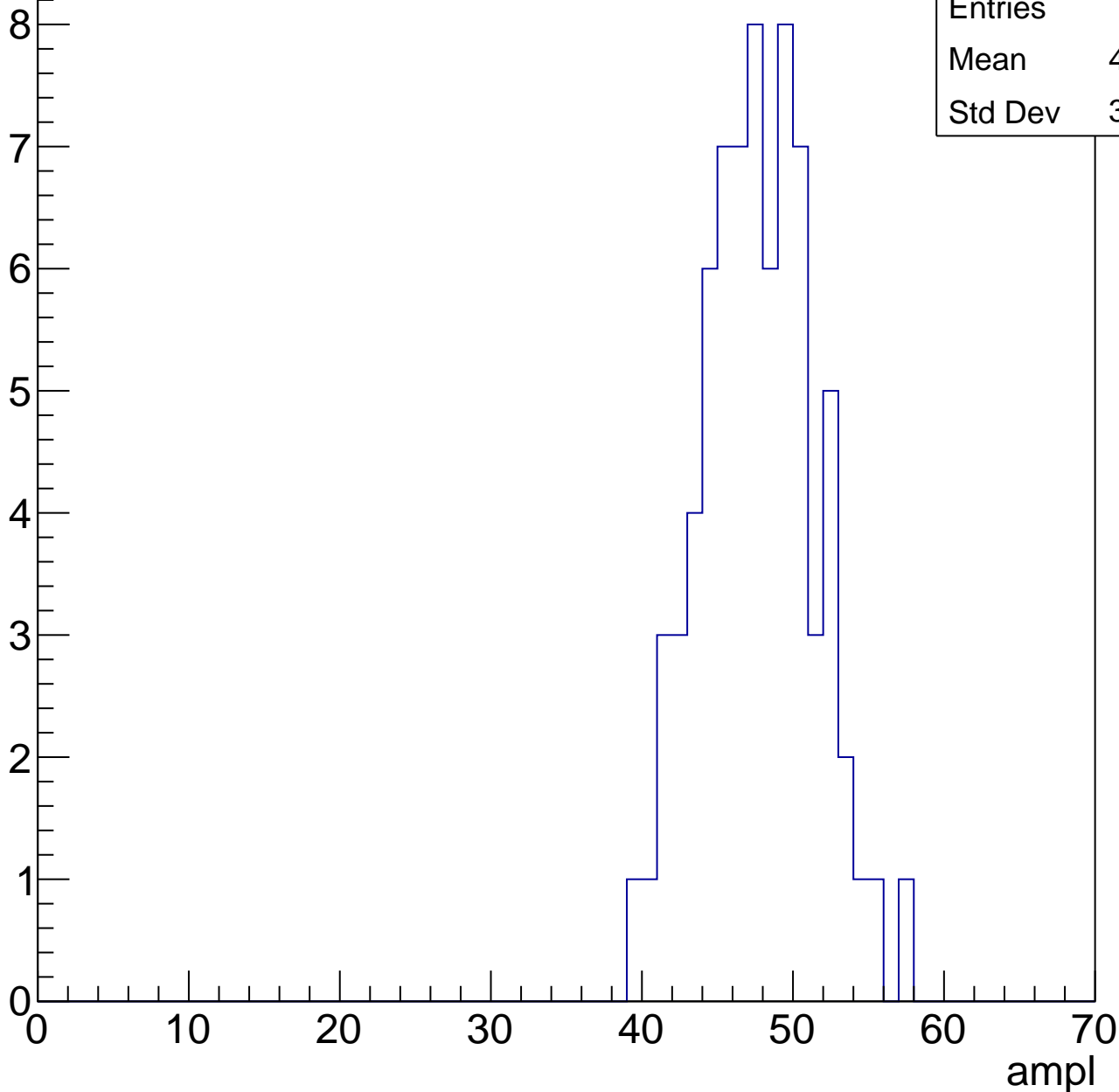


# B1L101S, U8-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	47.19
Std Dev	3.686



# B1L101S, U8-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

Entries 47

Mean 53.4

Std Dev 3.387

ampl

0

10

20

30

40

50

60

70

0

1

2

3

4

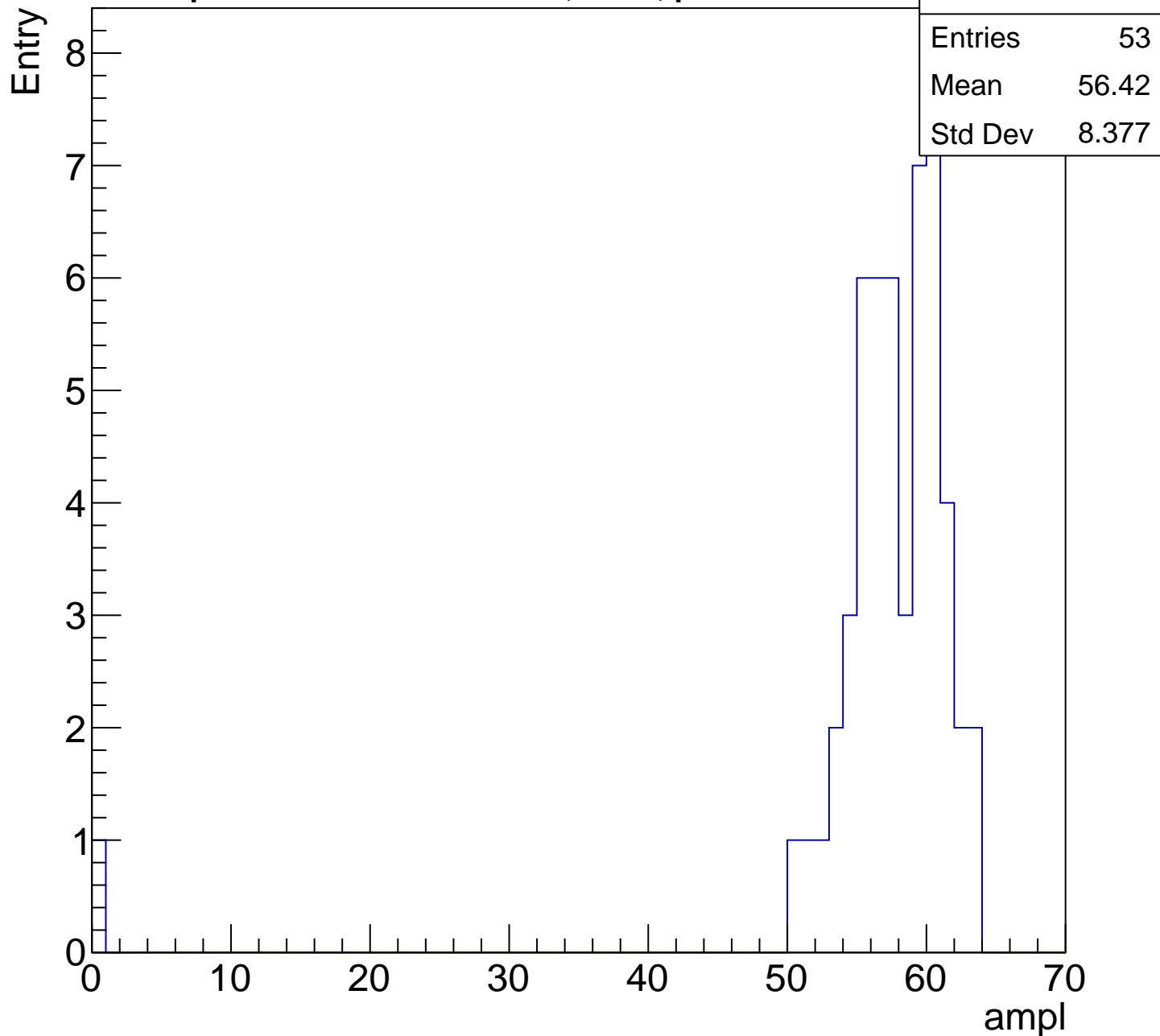
5

6

7

# B1L101S, U8-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

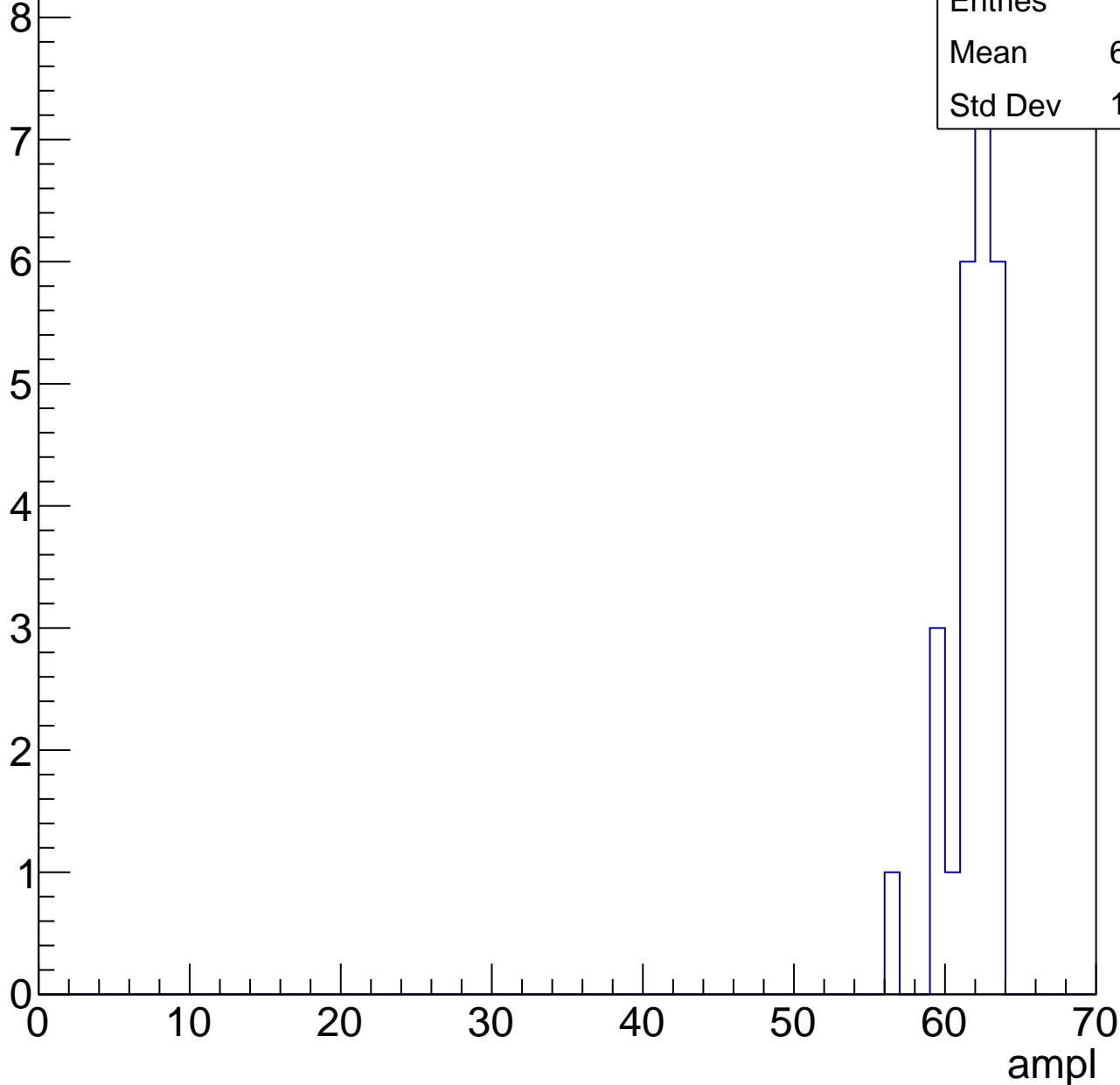


# B1L101S, U8-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	25
Mean	61.32
Std Dev	1.642

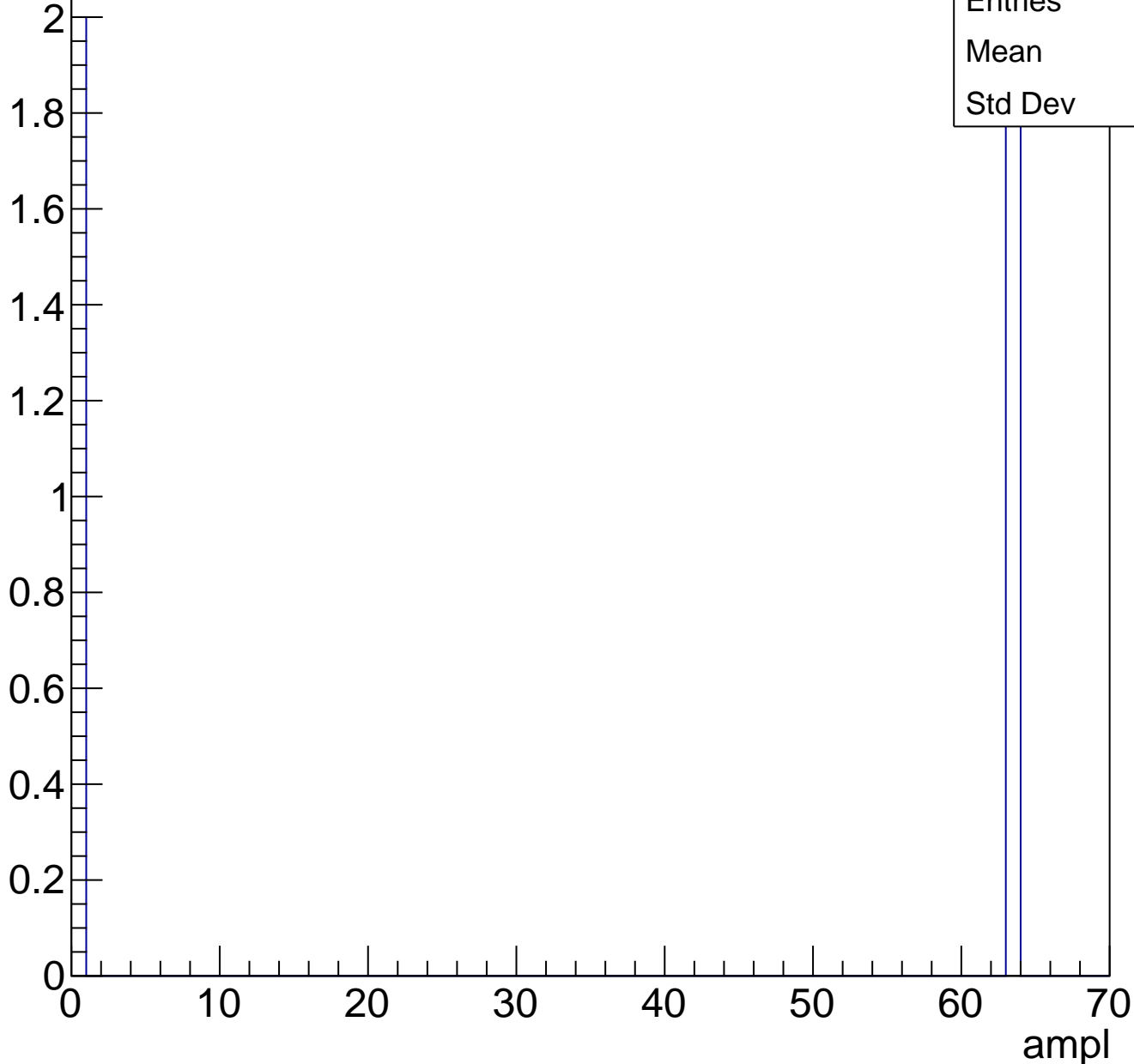




# B1L101S, U8-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch101, adc0

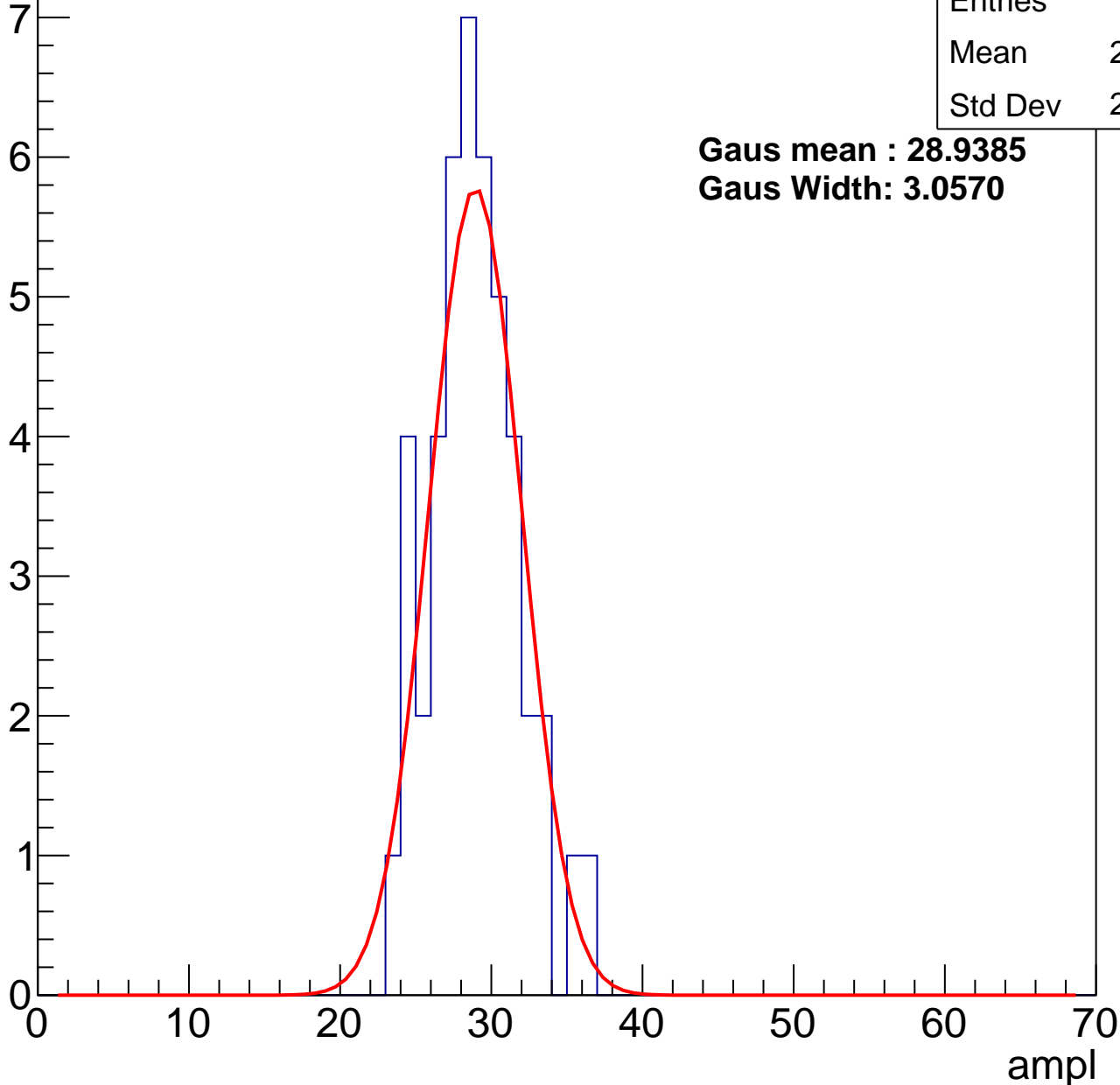
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	28.44
Std Dev	2.895

**Gaus mean : 28.9385**

**Gaus Width: 3.0570**



# B1L101S, U8-ch101, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	93
Mean	35.43
Std Dev	3.59

**Gaus mean : 35.8295**

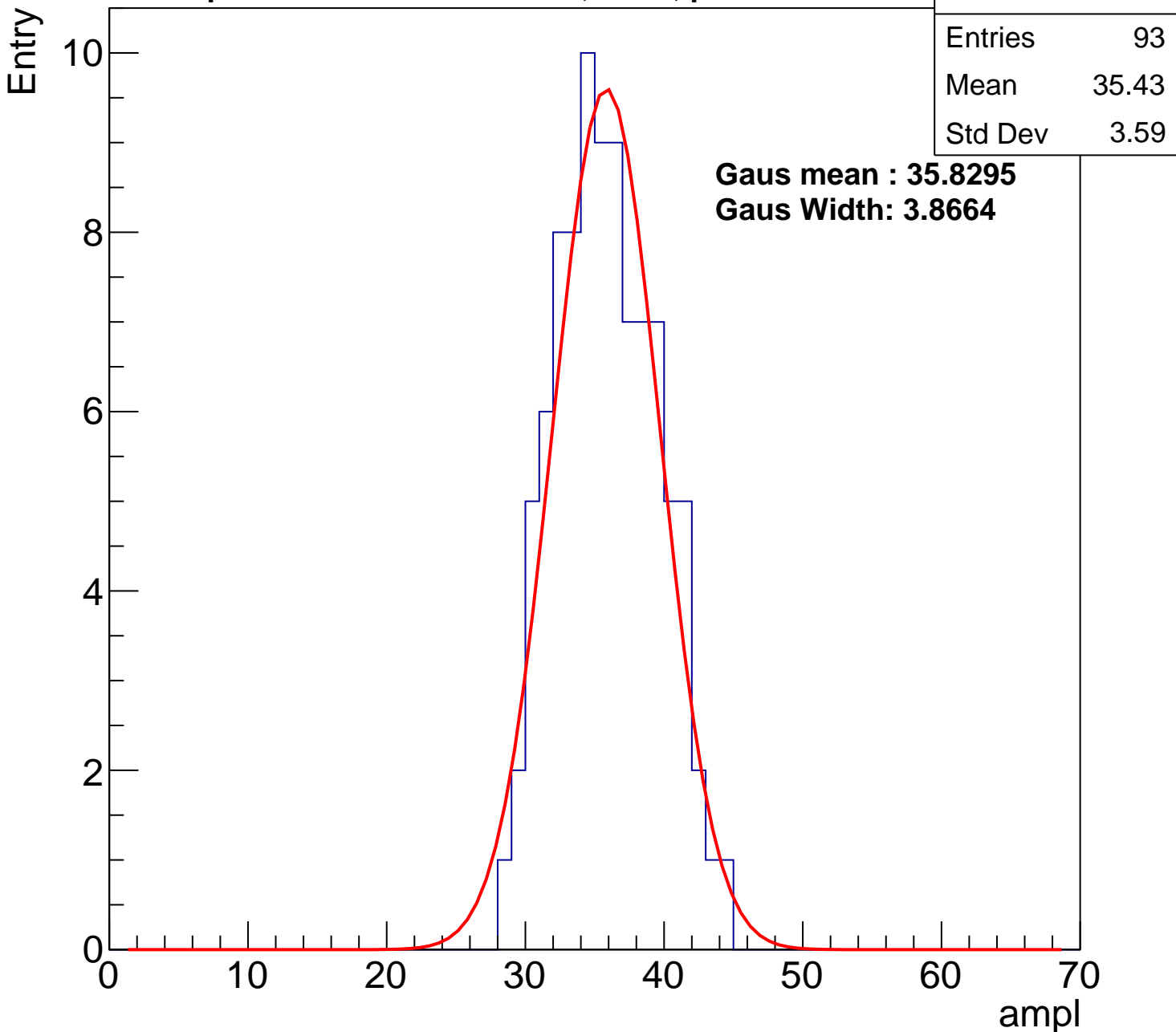
**Gaus Width: 3.8664**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U8-ch101, adc2

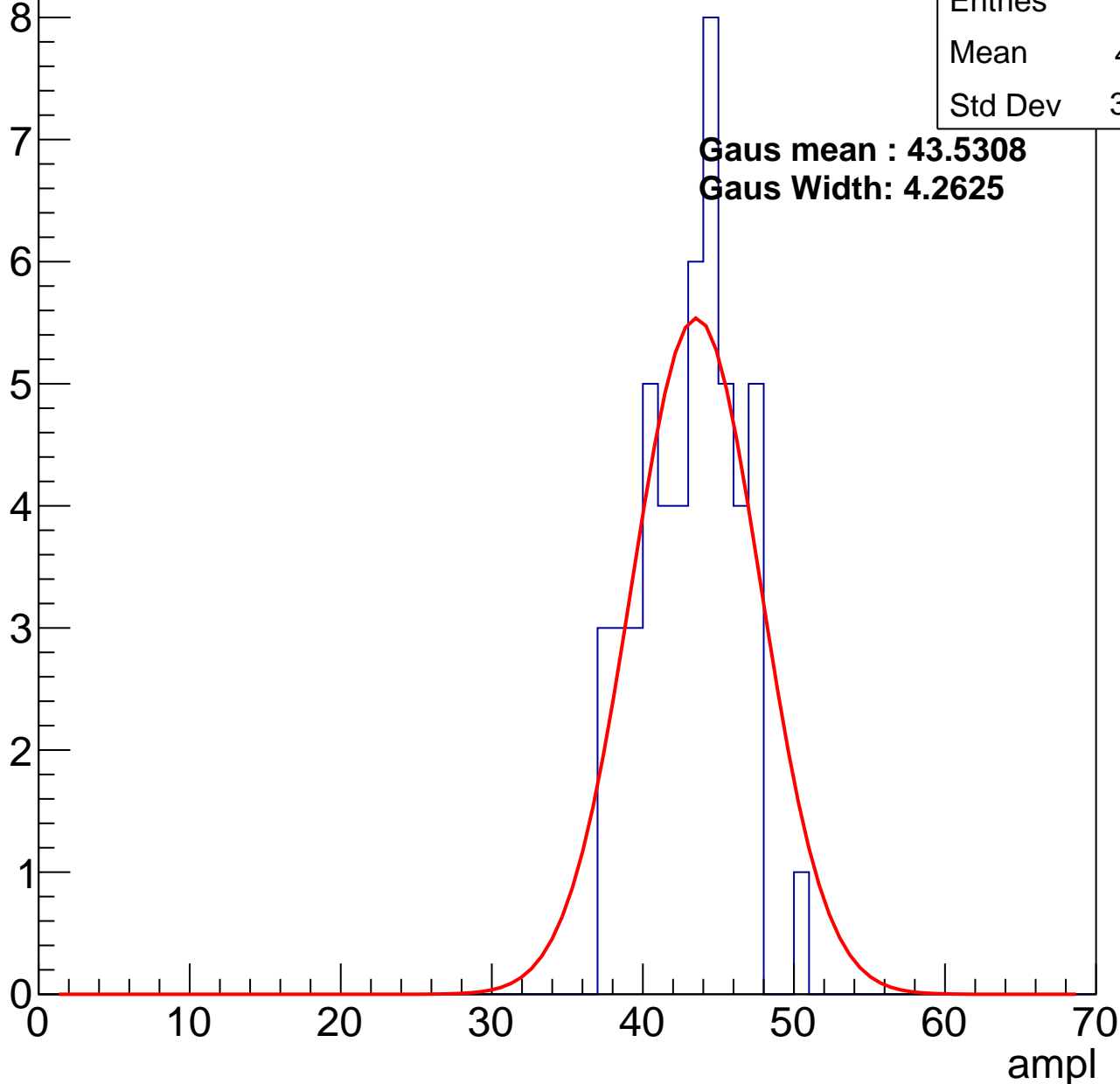
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	42.71
Std Dev	3.082

**Gaus mean : 43.5308**

**Gaus Width: 4.2625**



# B1L101S, U8-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

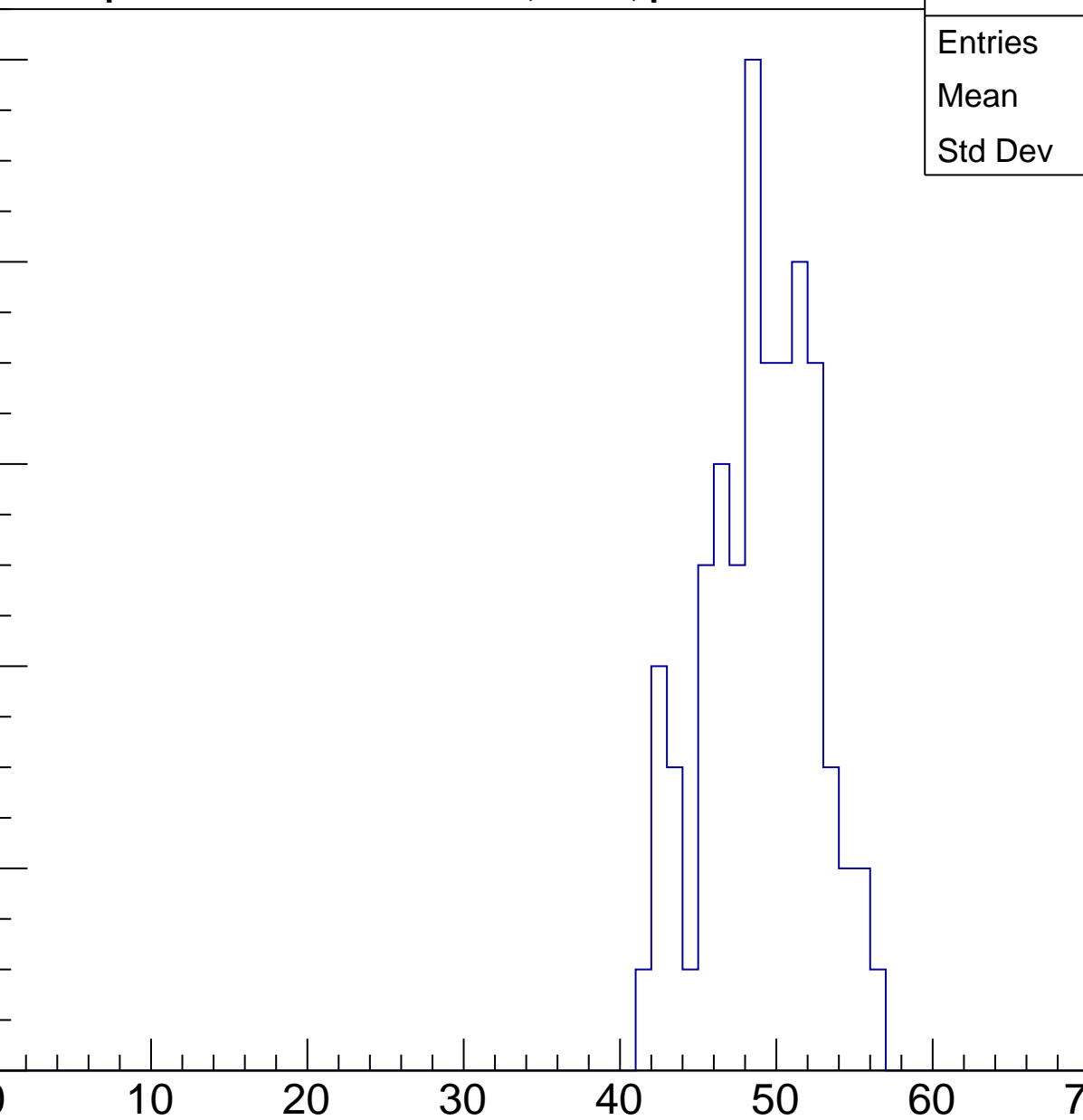
Entries	72
Mean	48.56
Std Dev	3.464

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

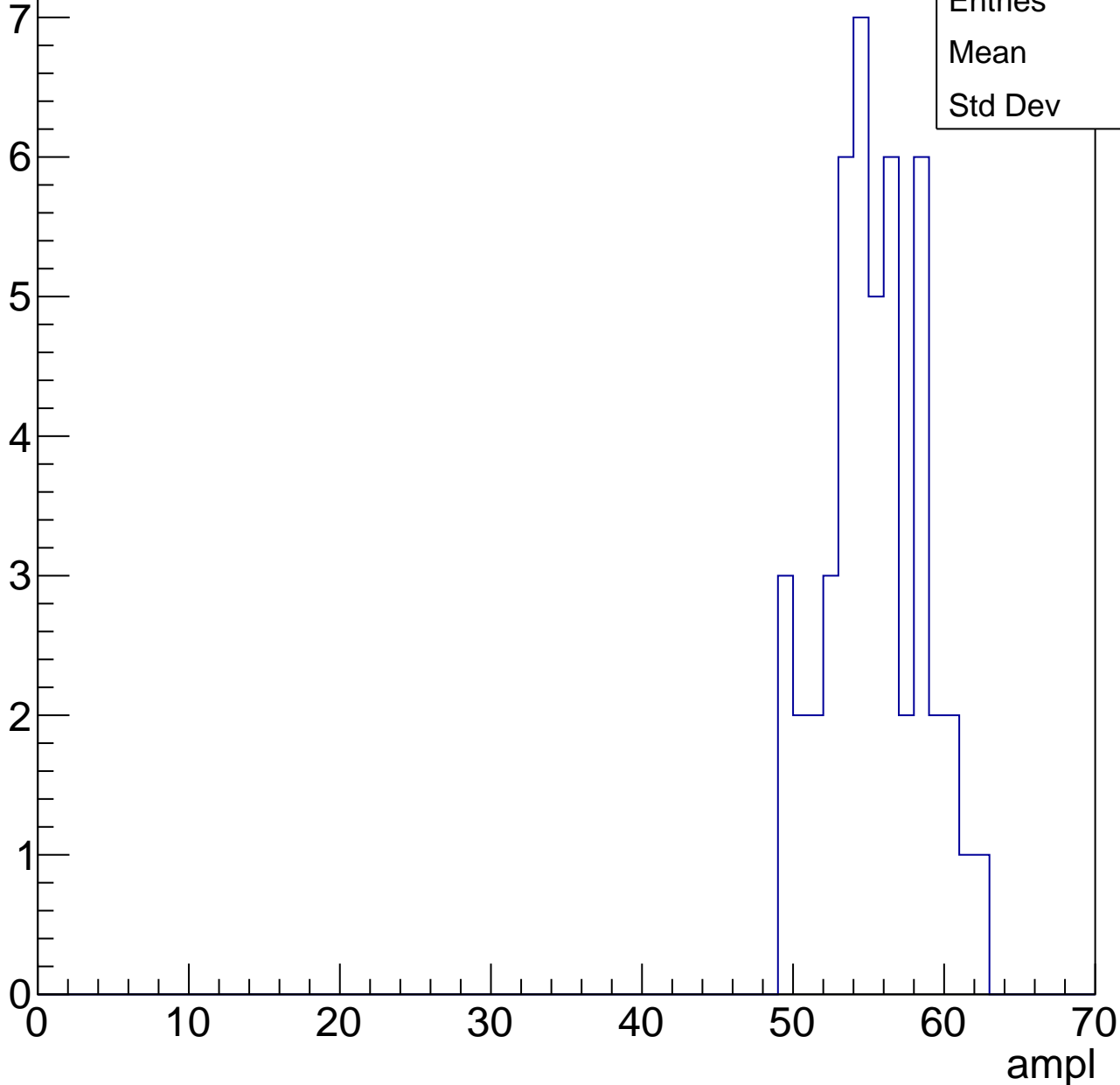


# B1L101S, U8-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	54.9
Std Dev	3.17



# B1L101S, U8-ch101, adc5

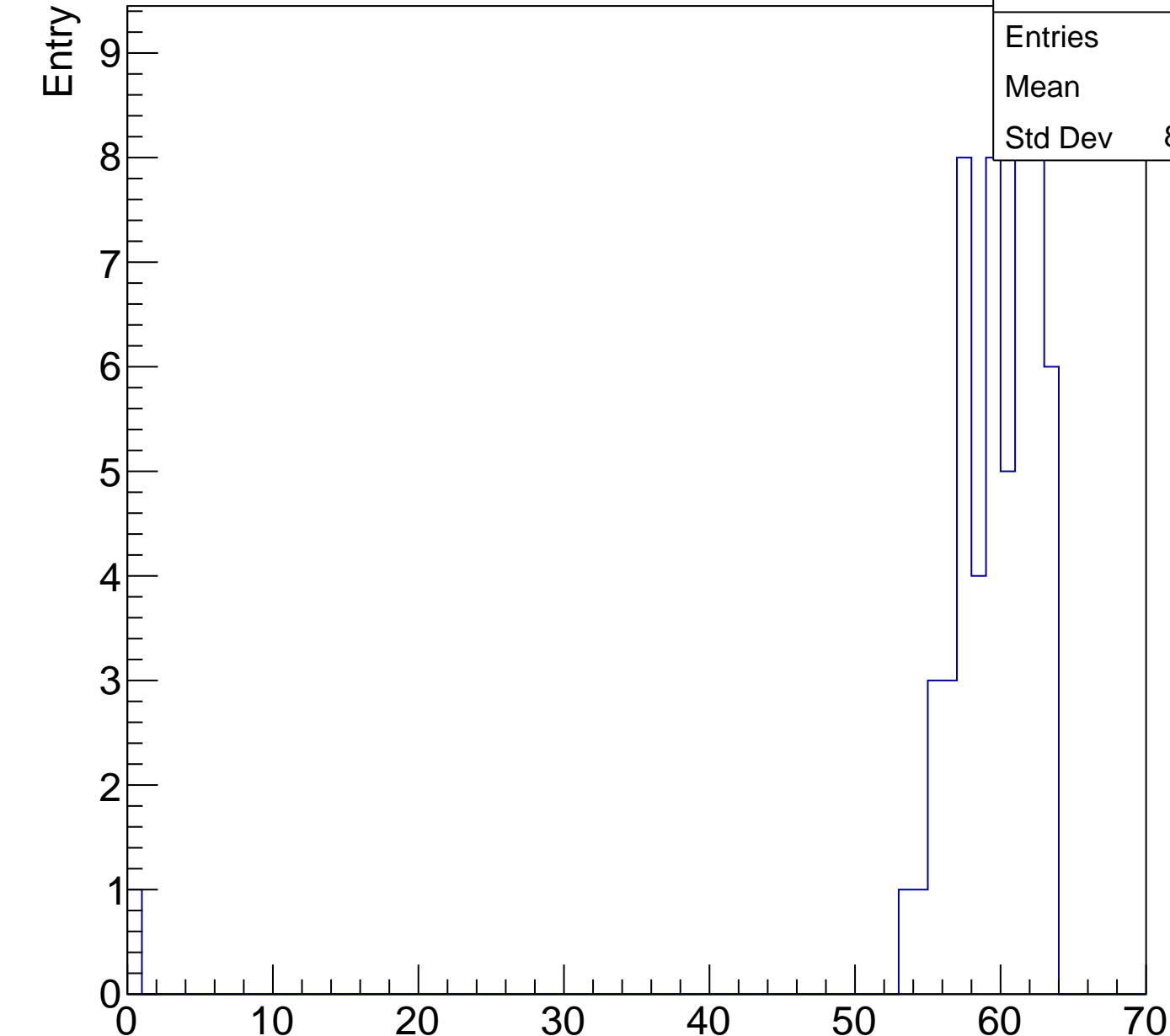
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	57
Mean	58.3
Std Dev	8.201

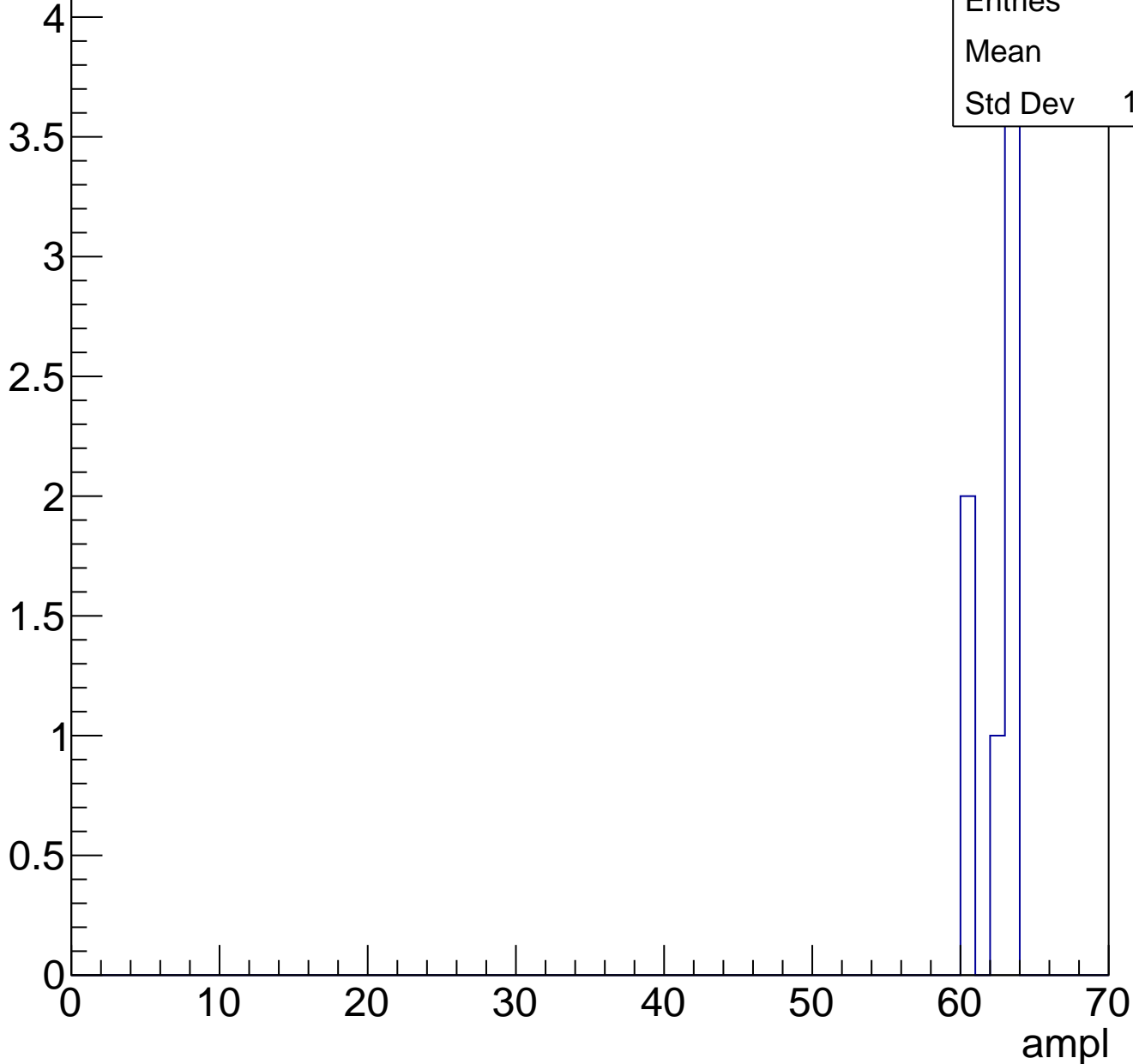
ampl



# B1L101S, U8-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

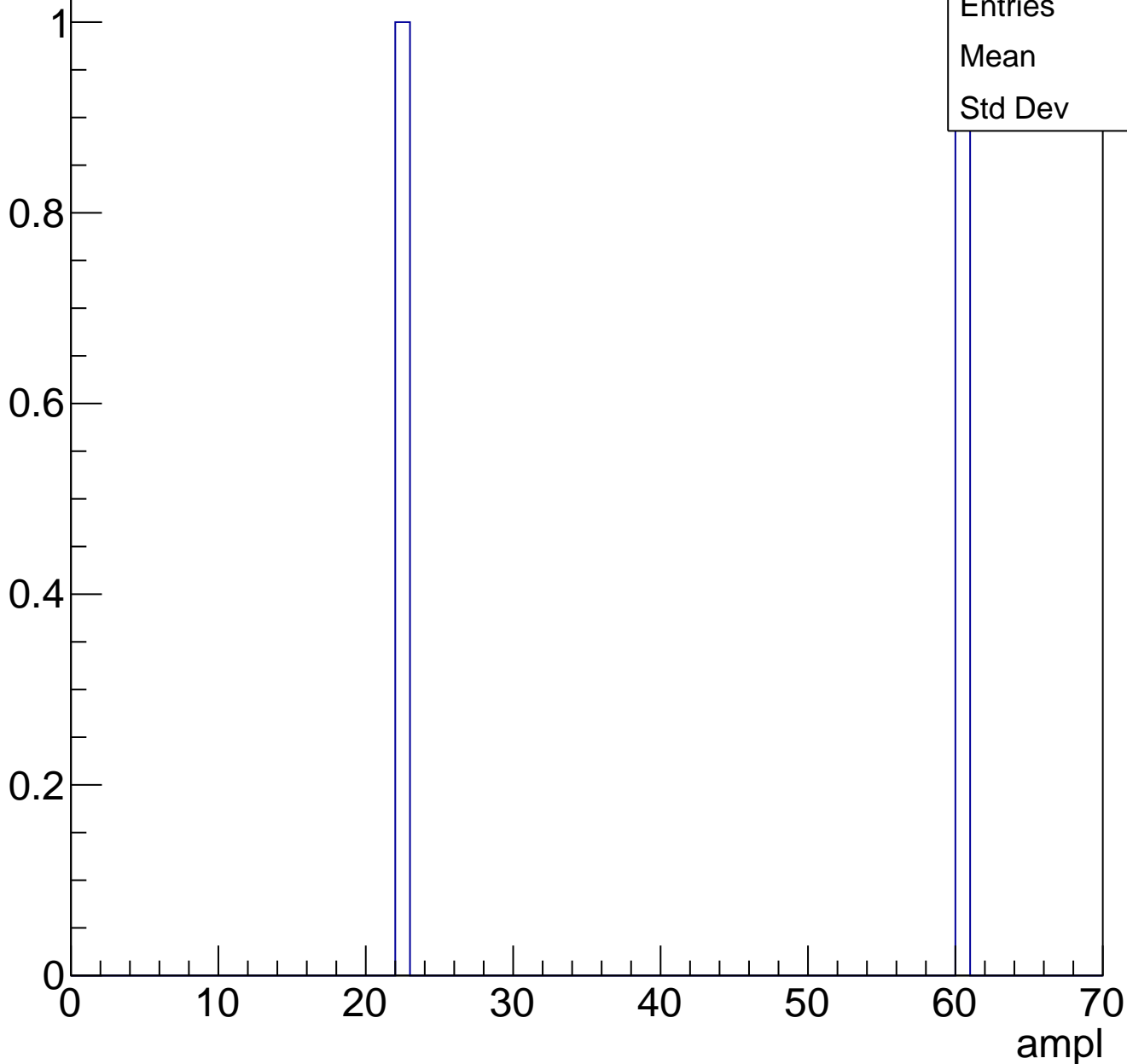




# B1L101S, U8-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch102, adc0

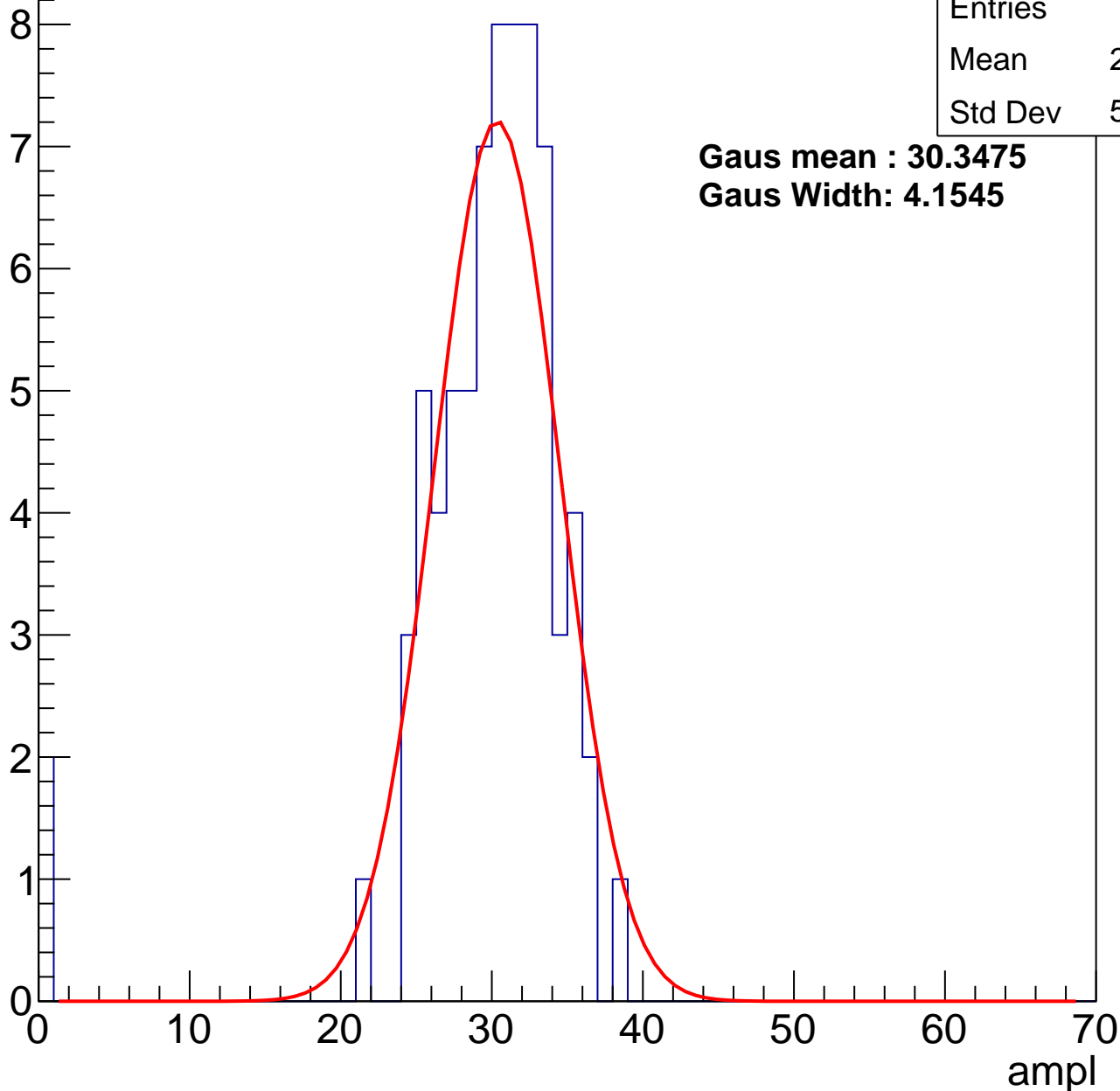
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	29.14
Std Dev	5.948

**Gaus mean : 30.3475**

**Gaus Width: 4.1545**



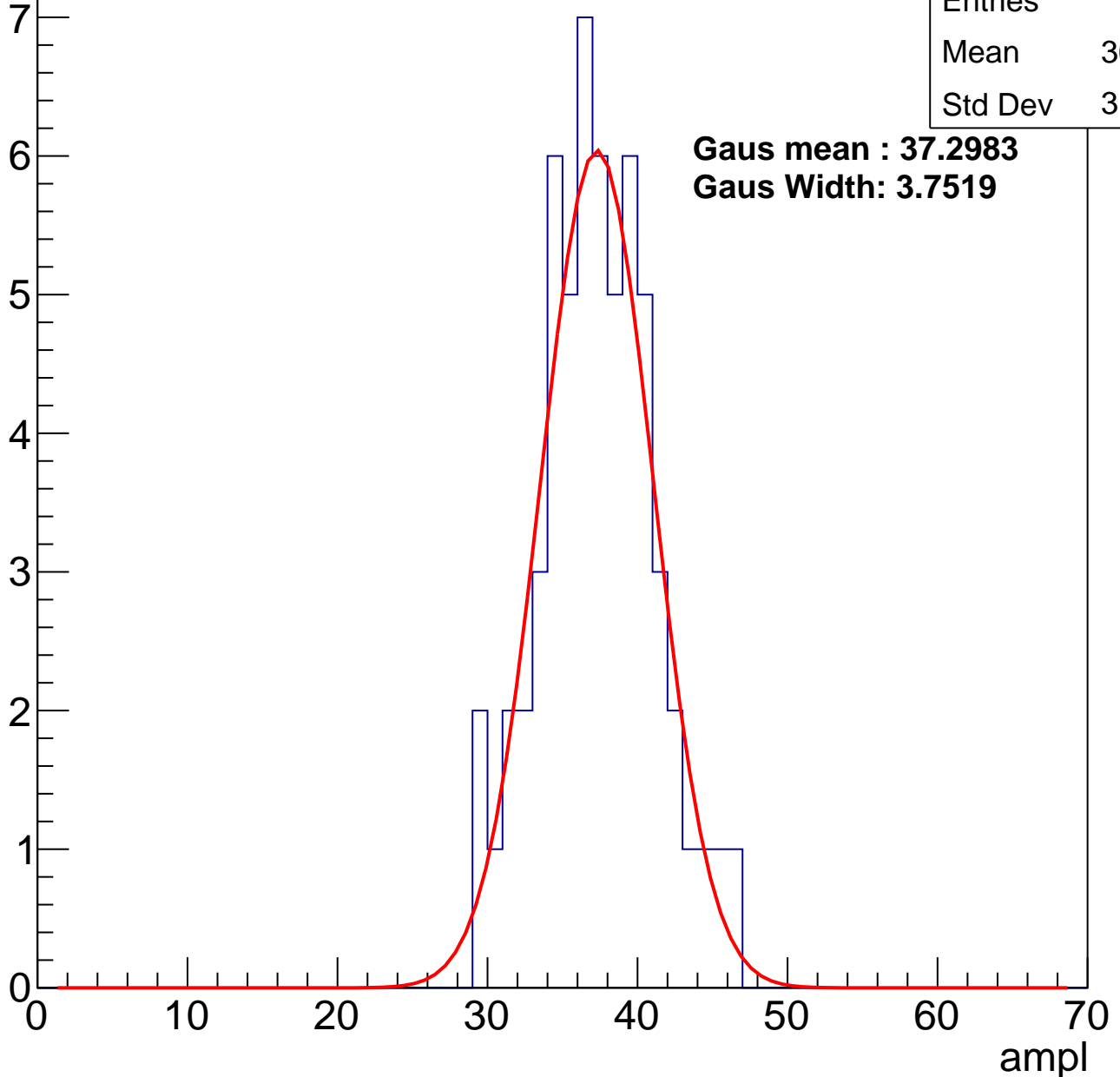
# B1L101S, U8-ch102, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	36.86
Std Dev	3.748

**Gaus mean : 37.2983**  
**Gaus Width: 3.7519**



# B1L101S, U8-ch102, adc2

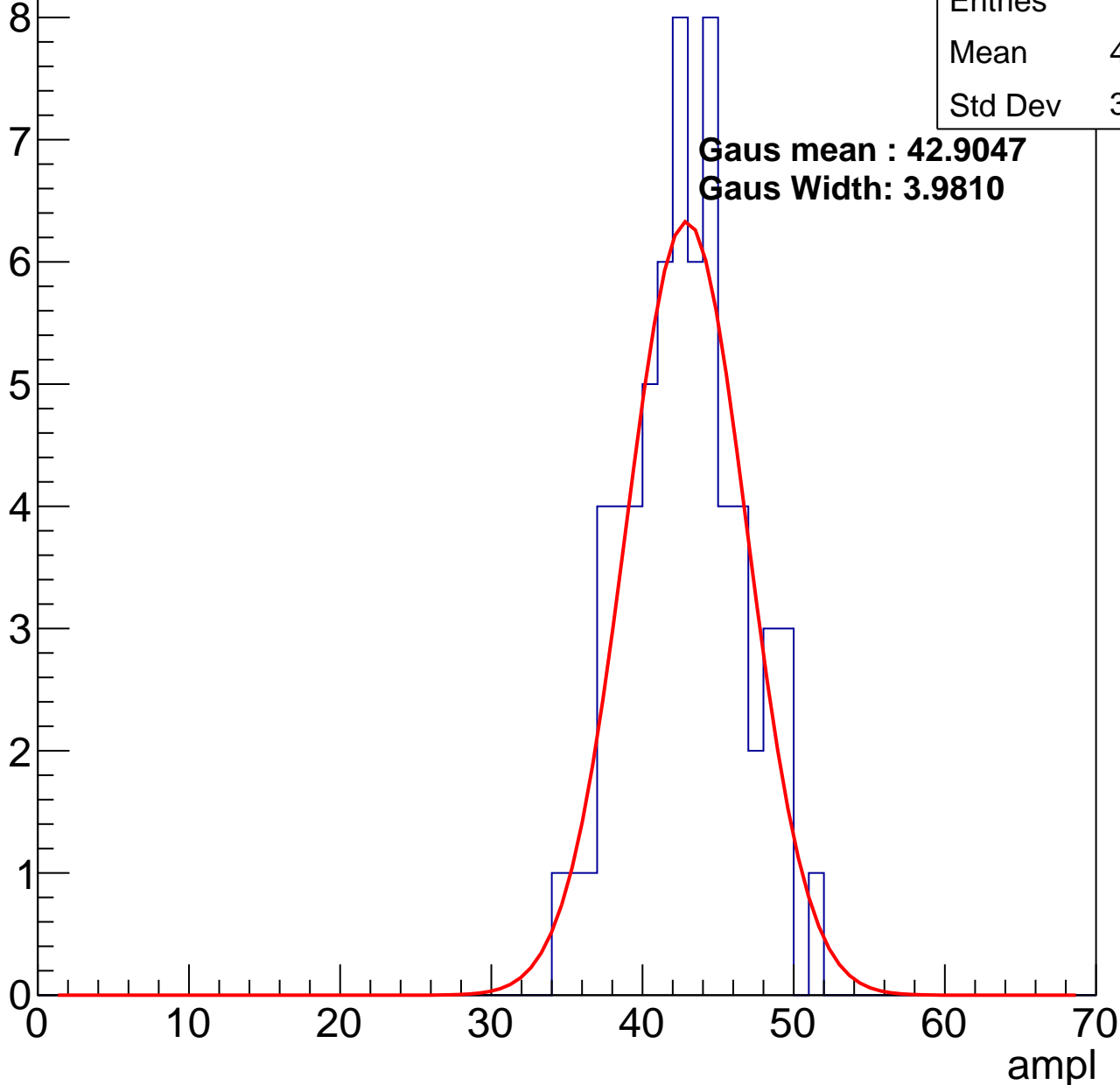
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	42.35
Std Dev	3.702

**Gaus mean : 42.9047**

**Gaus Width: 3.9810**

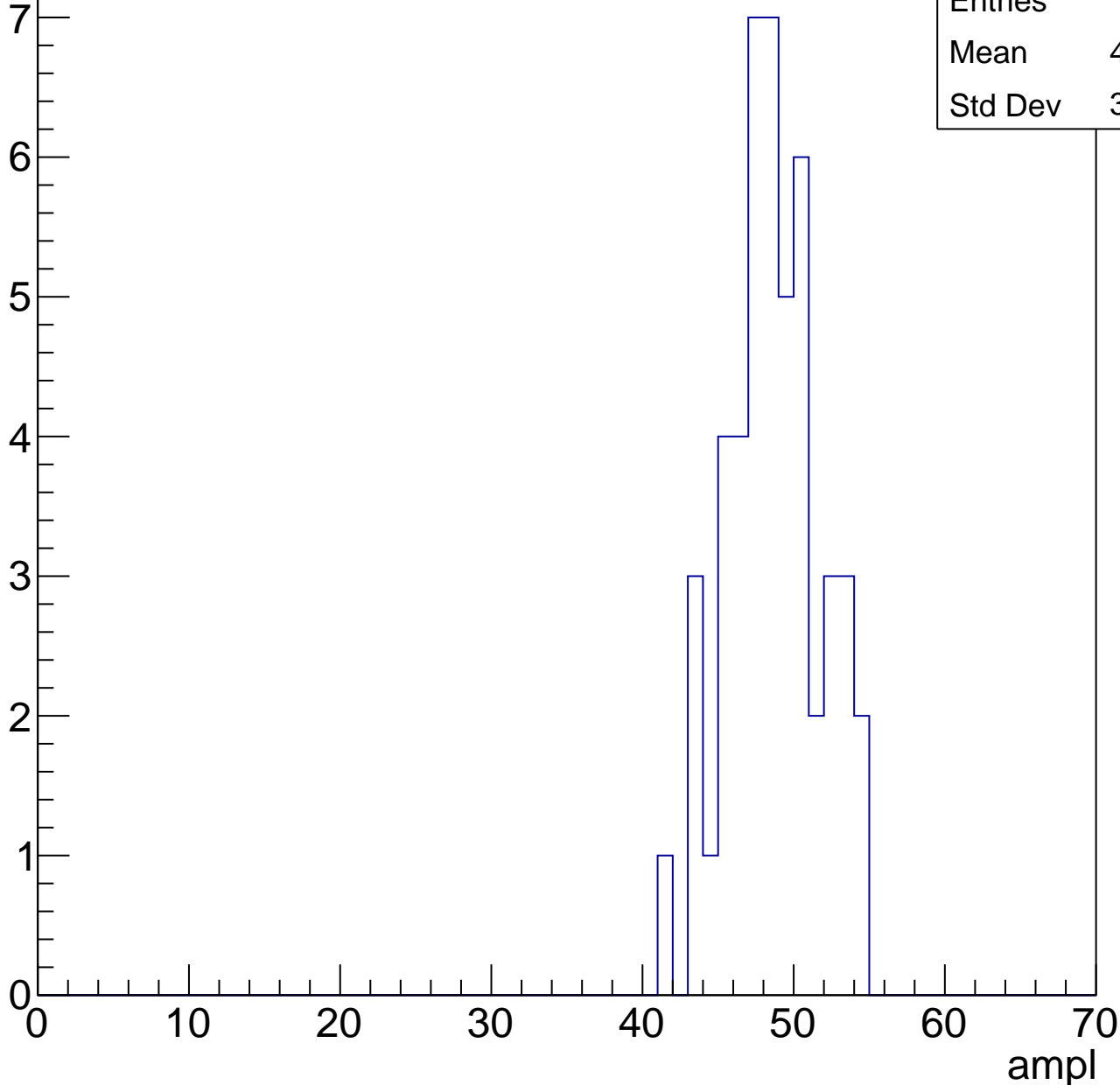


# B1L101S, U8-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	48.19
Std Dev	3.025

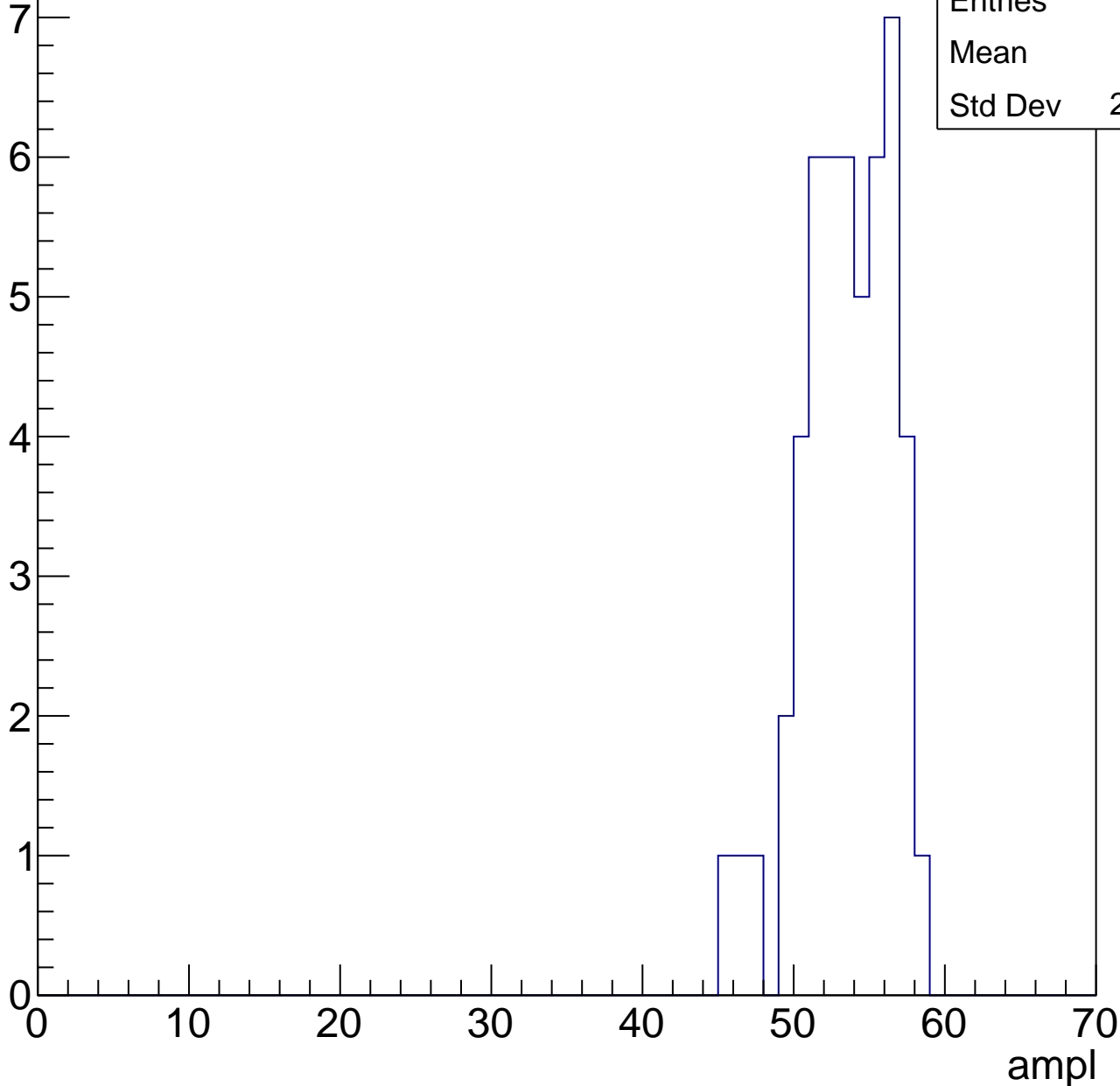


# B1L101S, U8-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	53
Std Dev	2.926



# B1L101S, U8-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

10

8

6

4

2

0

0

10

20

30

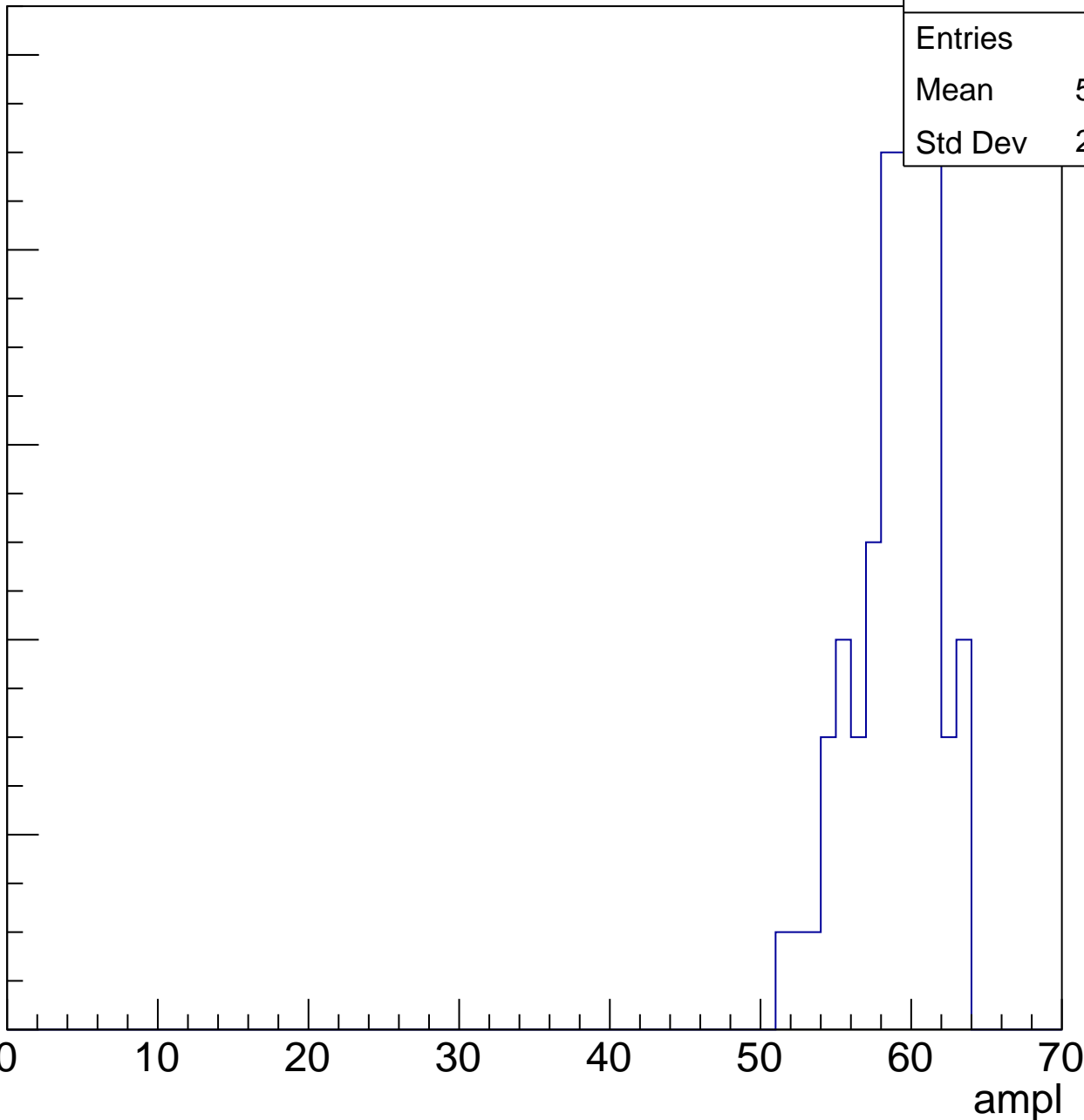
40

50

60

ampl

Entries	62
Mean	58.58
Std Dev	2.762

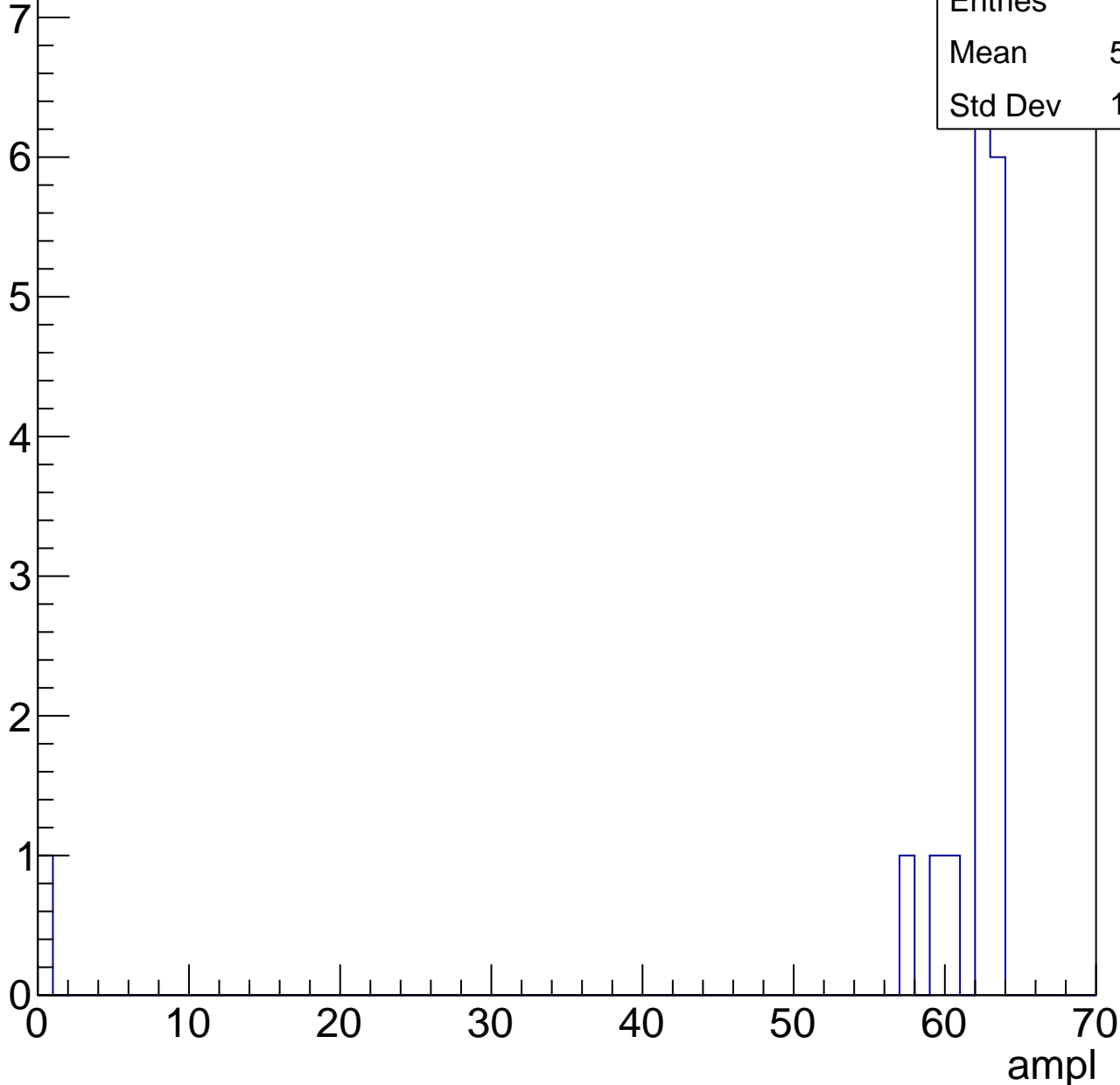


# B1L101S, U8-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	17
Mean	58.12
Std Dev	14.62





# B1L101S, U8-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U8-ch103, adc0

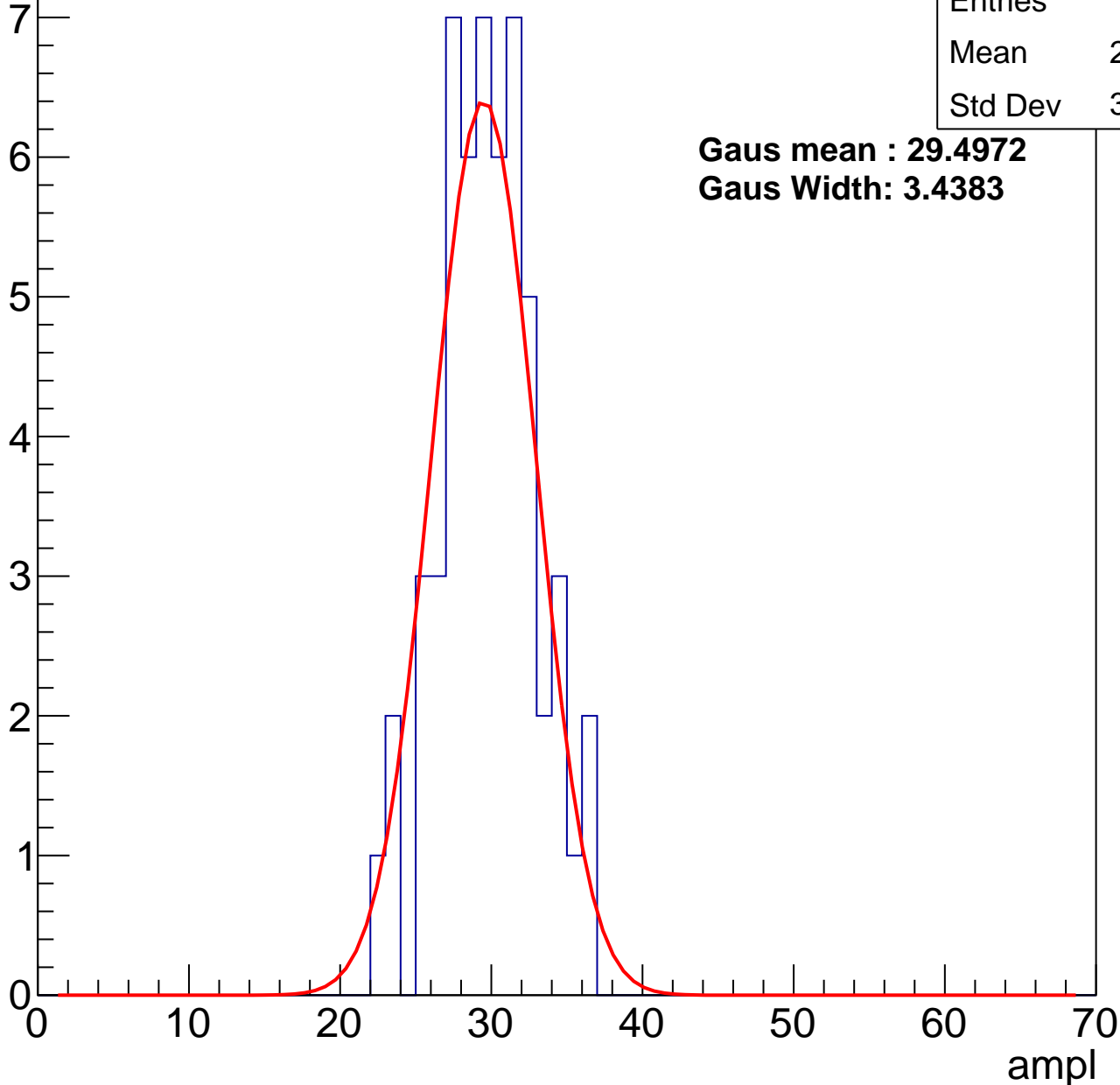
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	29.33
Std Dev	3.145

**Gaus mean : 29.4972**

**Gaus Width: 3.4383**



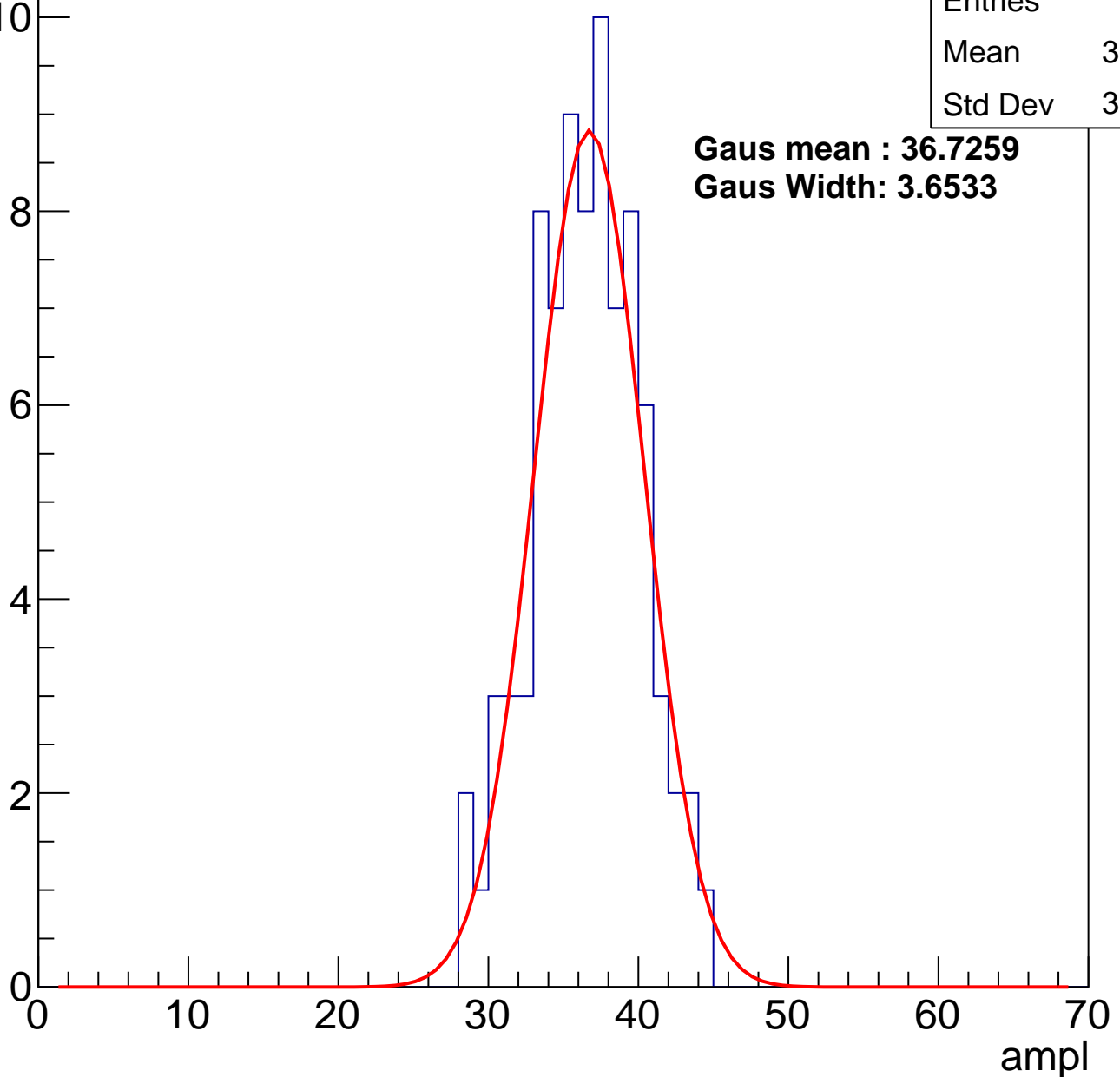
# B1L101S, U8-ch103, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	83
Mean	36.07
Std Dev	3.525

**Gaus mean : 36.7259**  
**Gaus Width: 3.6533**



# B1L101S, U8-ch103, adc2

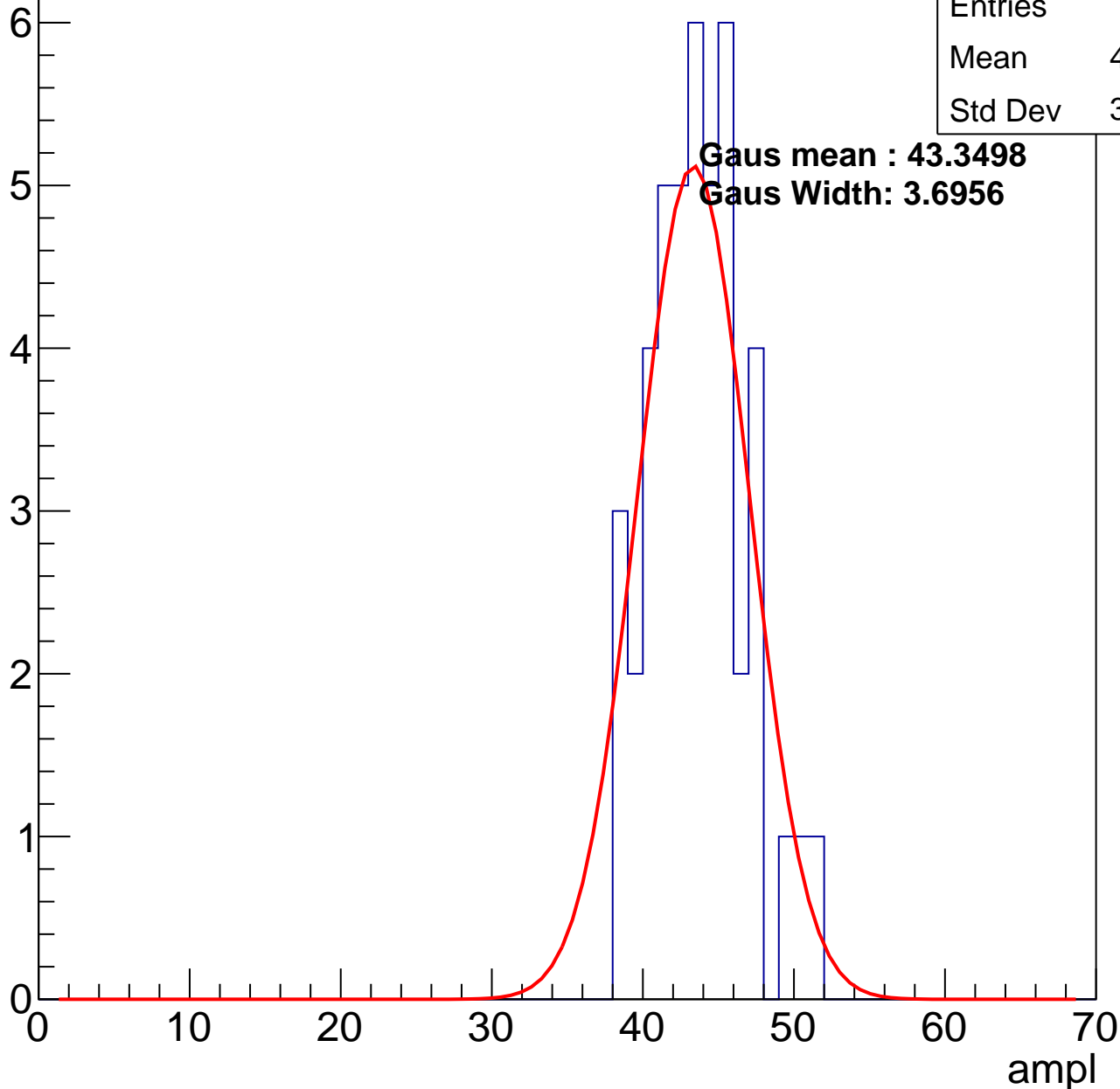
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	43.22
Std Dev	3.076

**Gaus mean : 43.3498**

**Gaus Width: 3.6956**



# B1L101S, U8-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

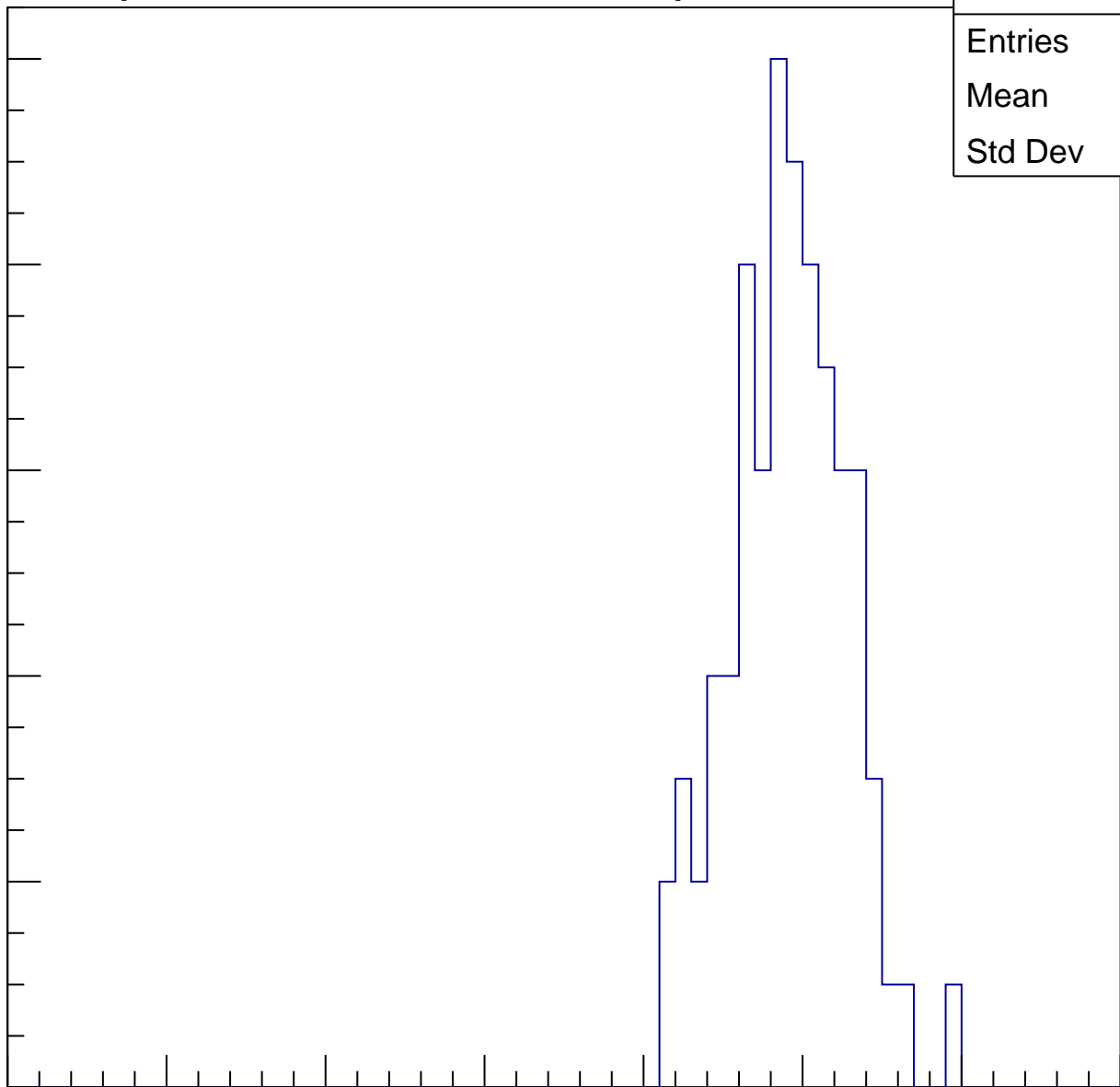
Entries	81
Mean	48.64
Std Dev	3.605

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

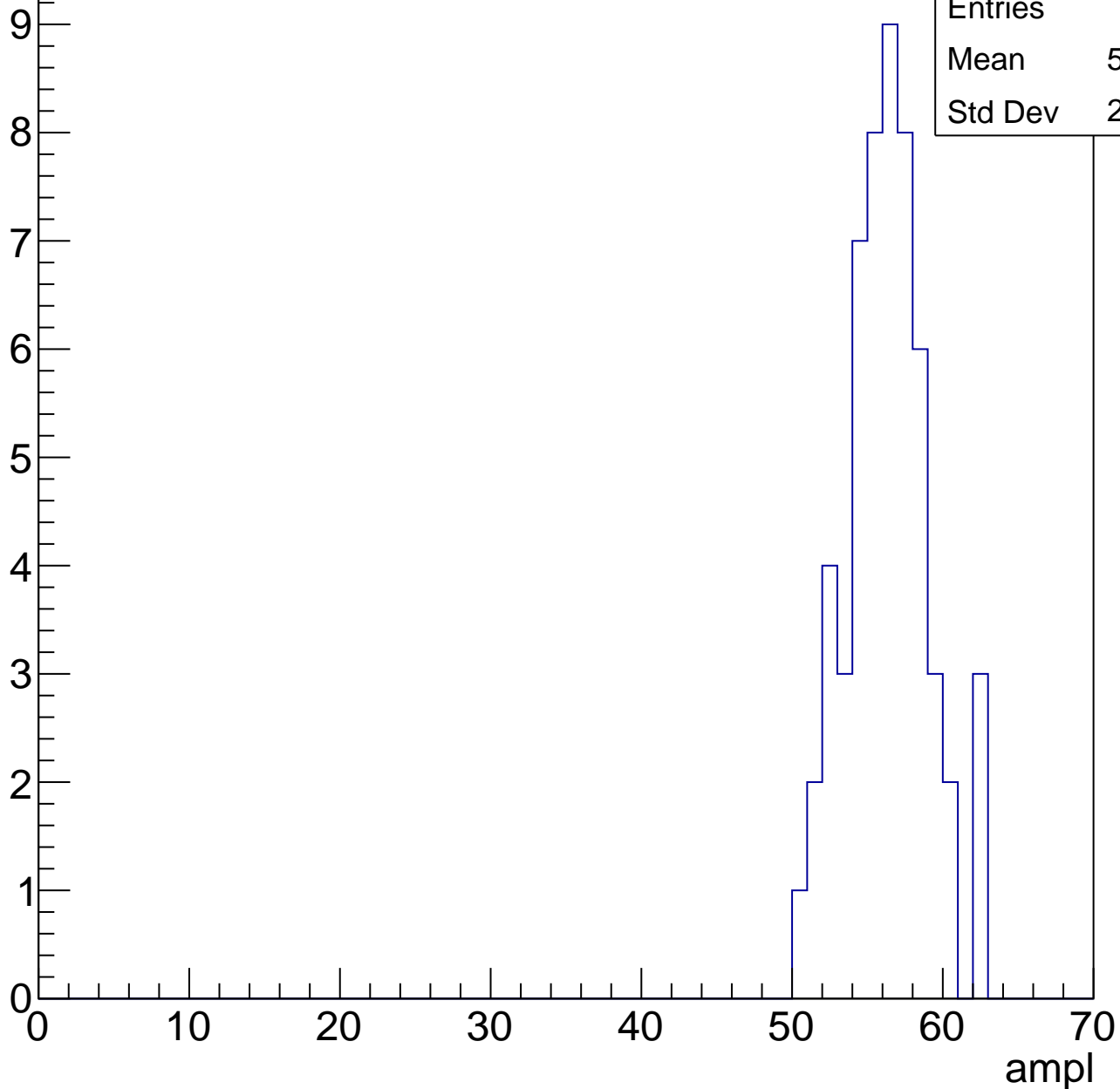
ampl



# B1L101S, U8-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

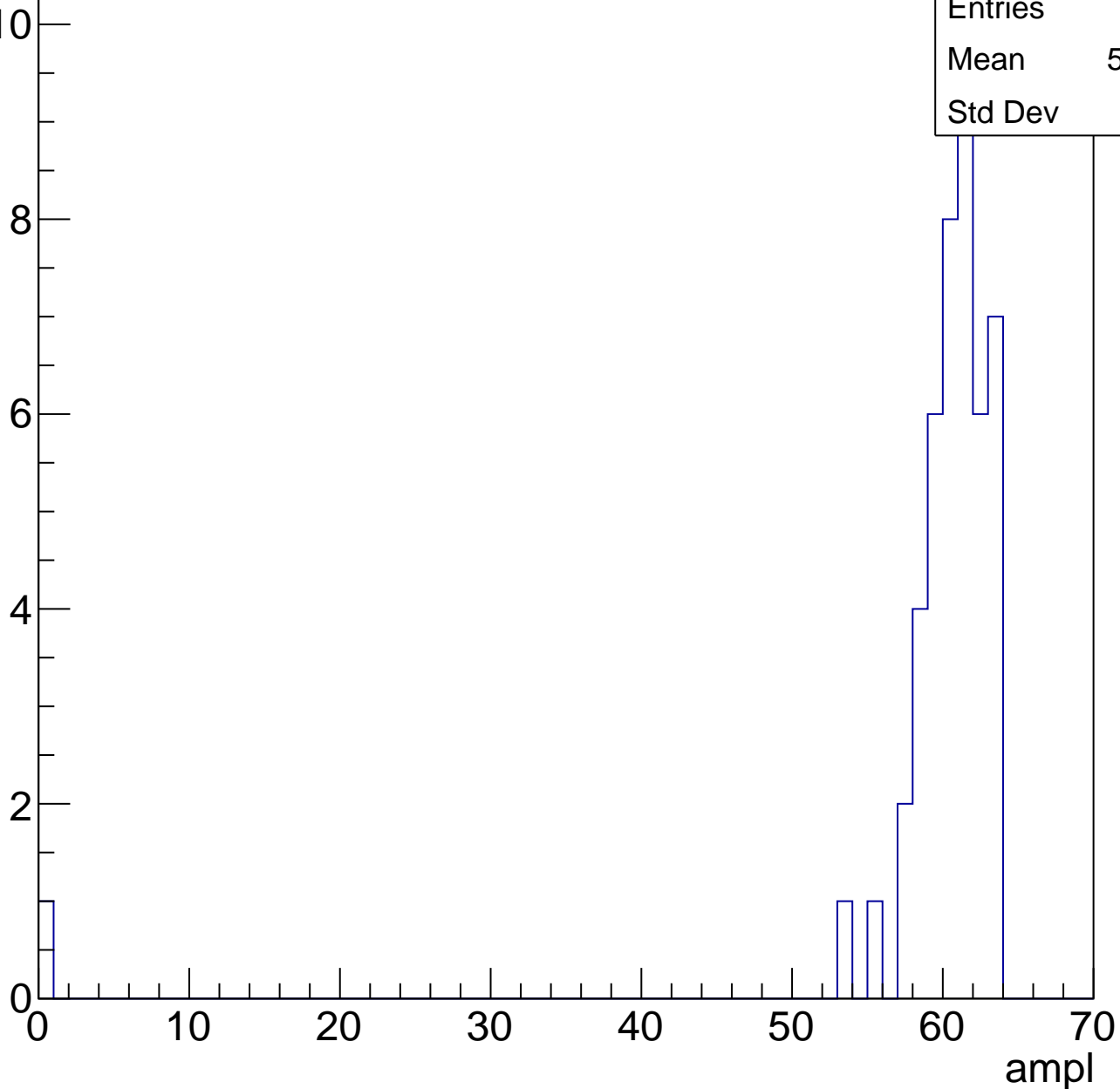


# B1L101S, U8-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	58.93
Std Dev	9.04



# B1L101S, U8-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U8-ch104, adc0

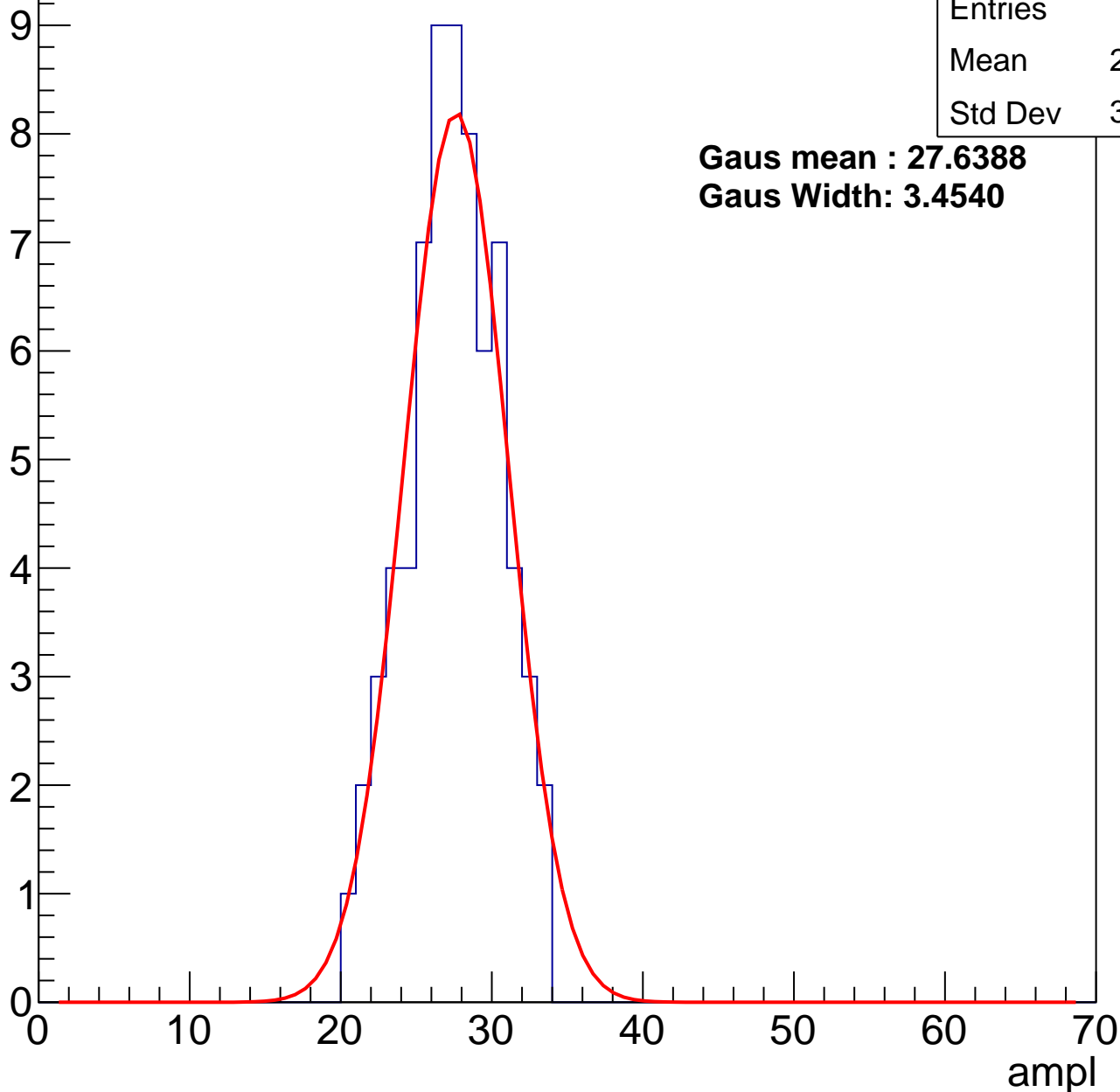
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	26.99
Std Dev	3.043

**Gaus mean : 27.6388**

**Gaus Width: 3.4540**



# B1L101S, U8-ch104, adc1

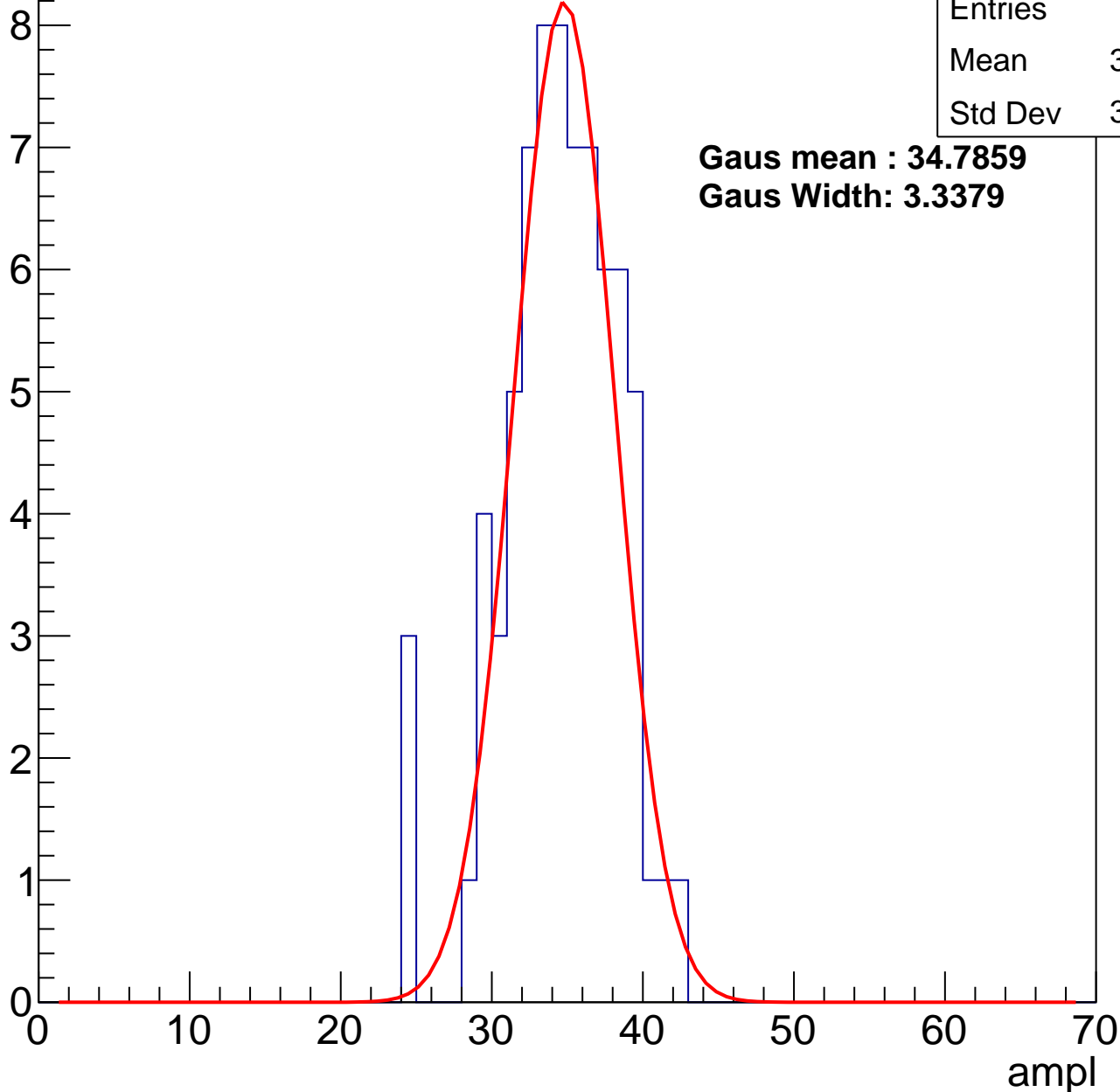
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	34.05
Std Dev	3.745

**Gaus mean : 34.7859**

**Gaus Width: 3.3379**



# B1L101S, U8-ch104, adc2

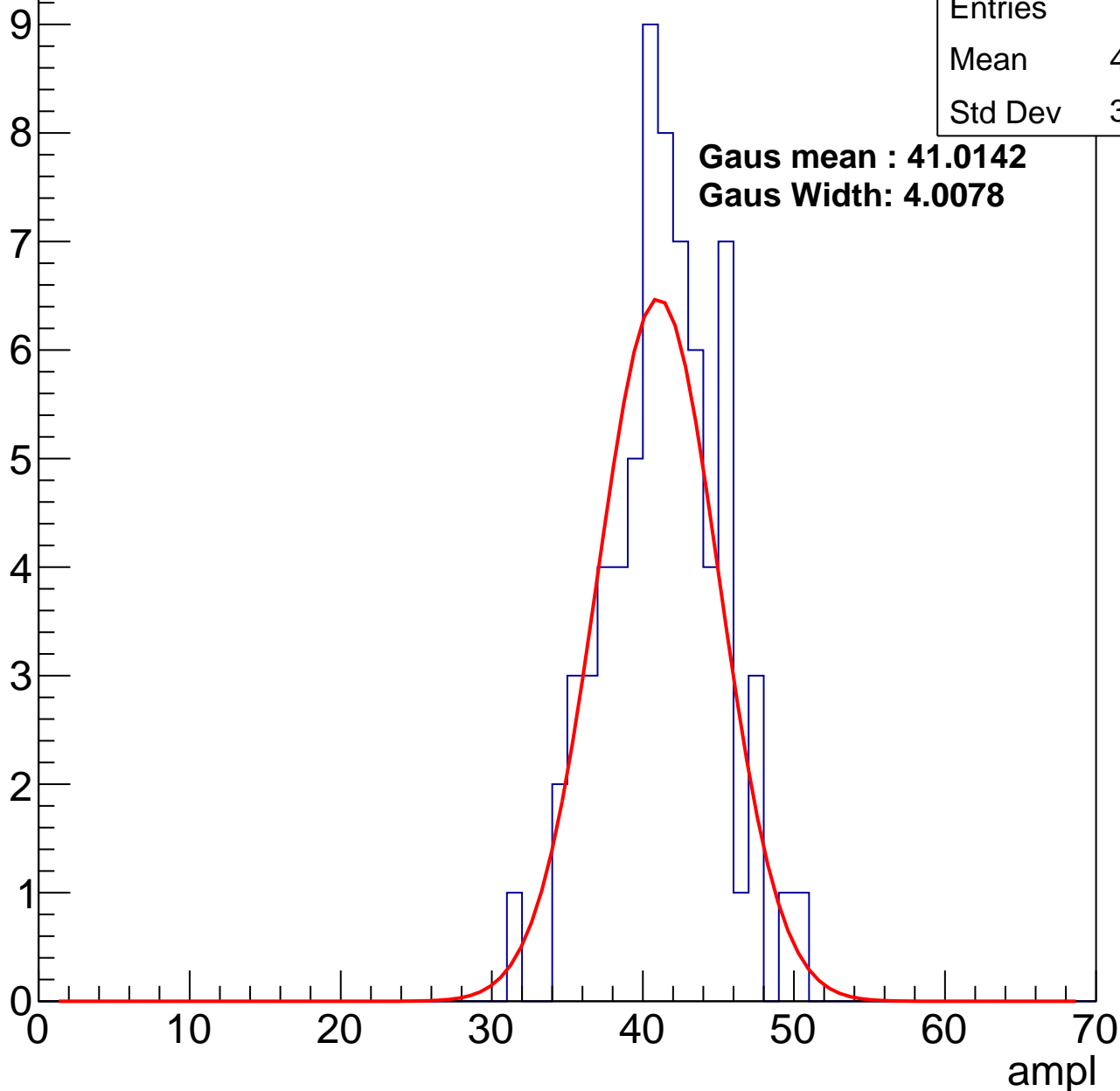
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	40.93
Std Dev	3.743

**Gaus mean : 41.0142**

**Gaus Width: 4.0078**

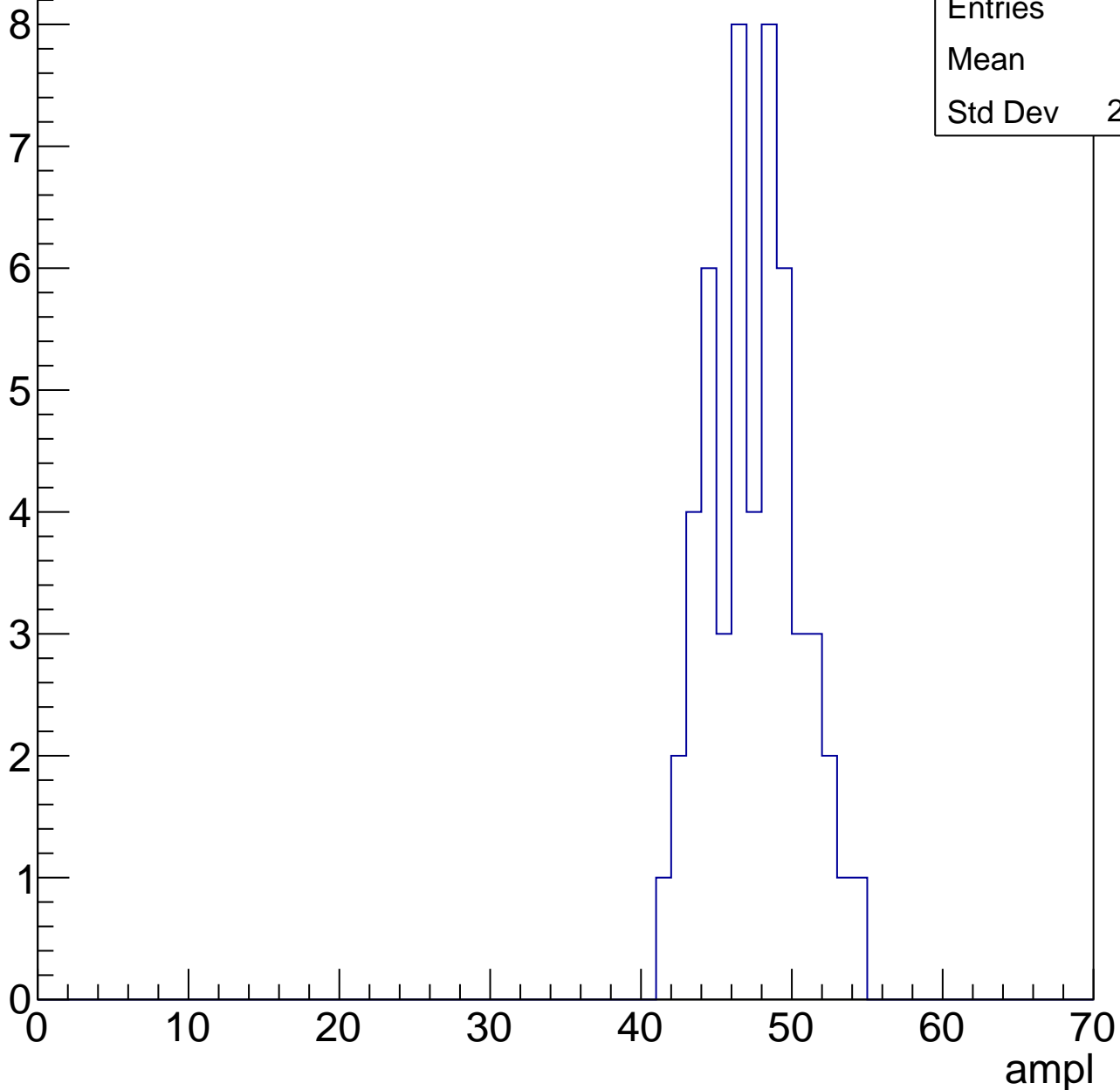


# B1L101S, U8-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	47
Std Dev	2.994

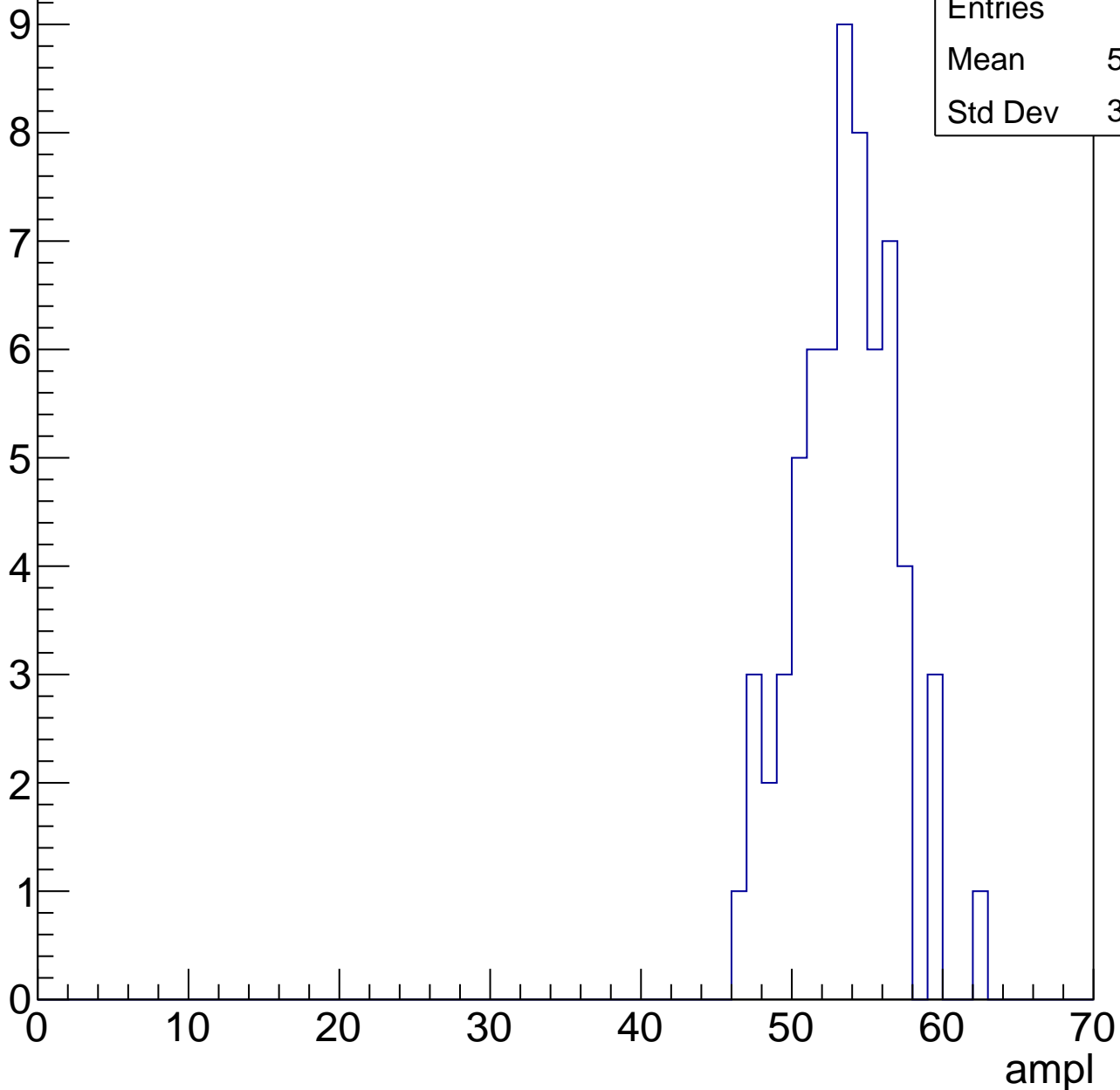


# B1L101S, U8-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	53.06
Std Dev	3.254

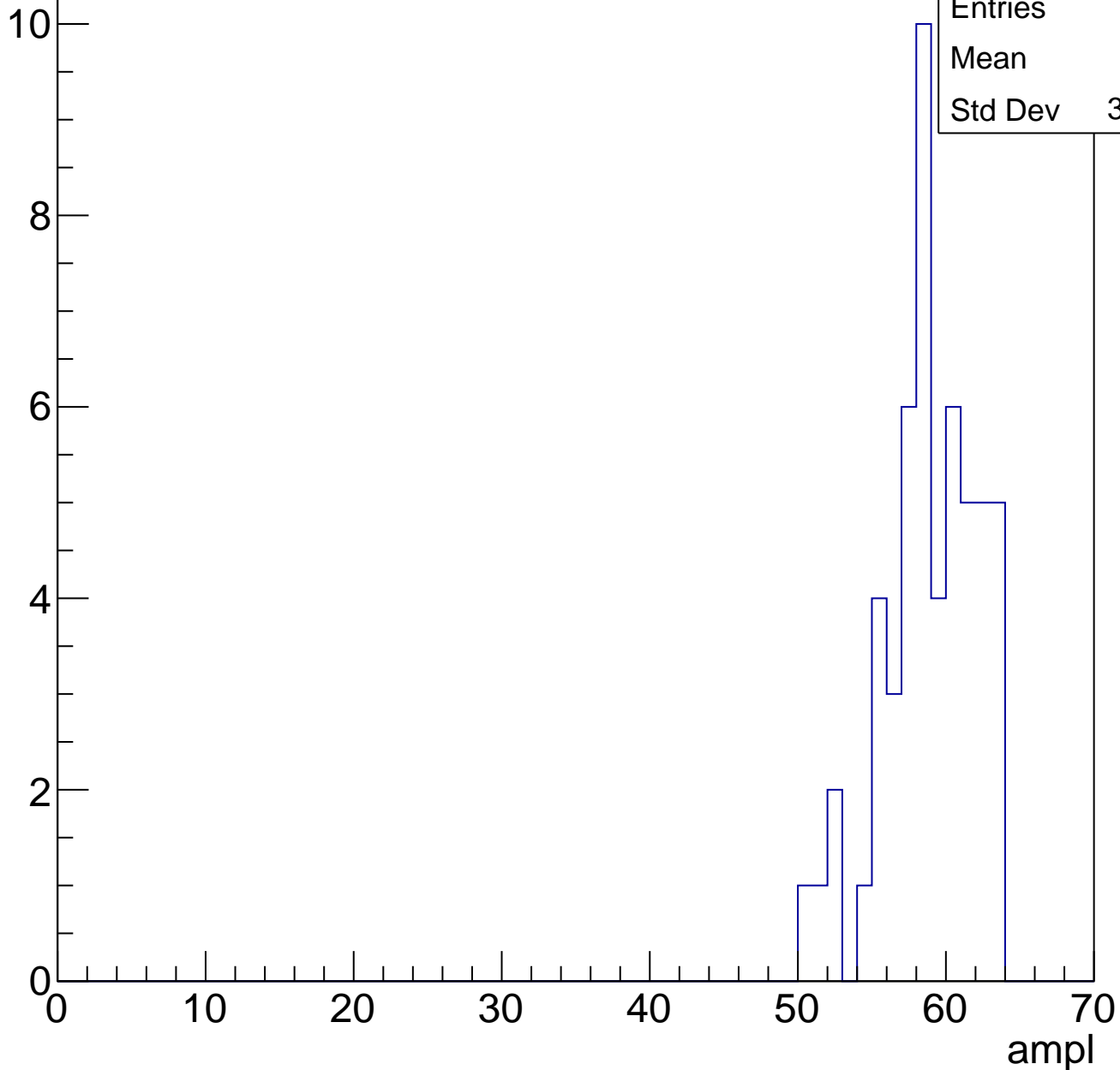


# B1L101S, U8-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	53
Mean	58.4
Std Dev	3.146

Entry



# B1L101S, U8-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

5

4

3

2

1

0

Entries	20
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Mean	61.25
------	-------

Std Dev	1.374
---------	-------

ampl

0

10

20

30

40

50

60

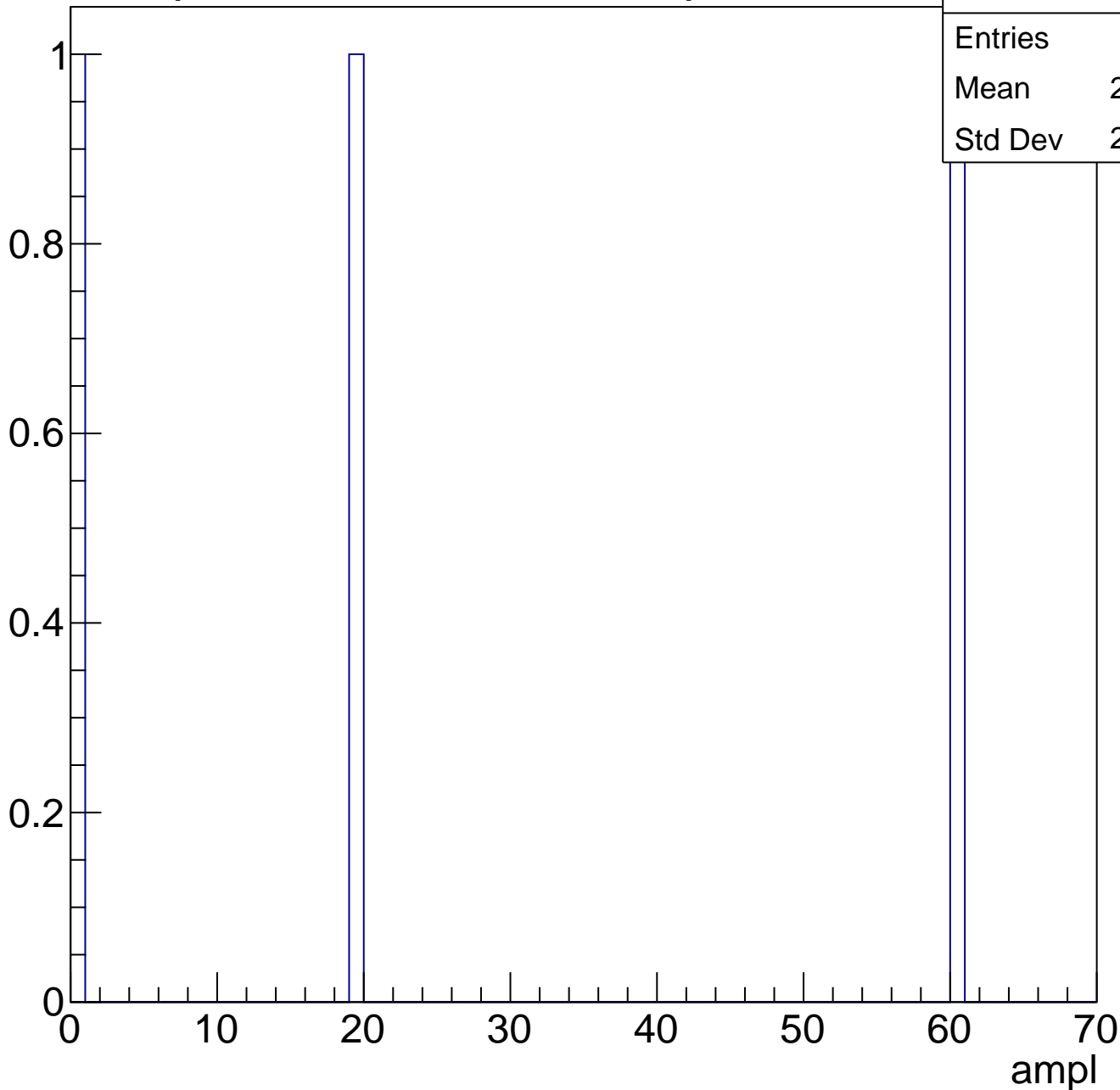
70



# B1L101S, U8-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch105, adc0

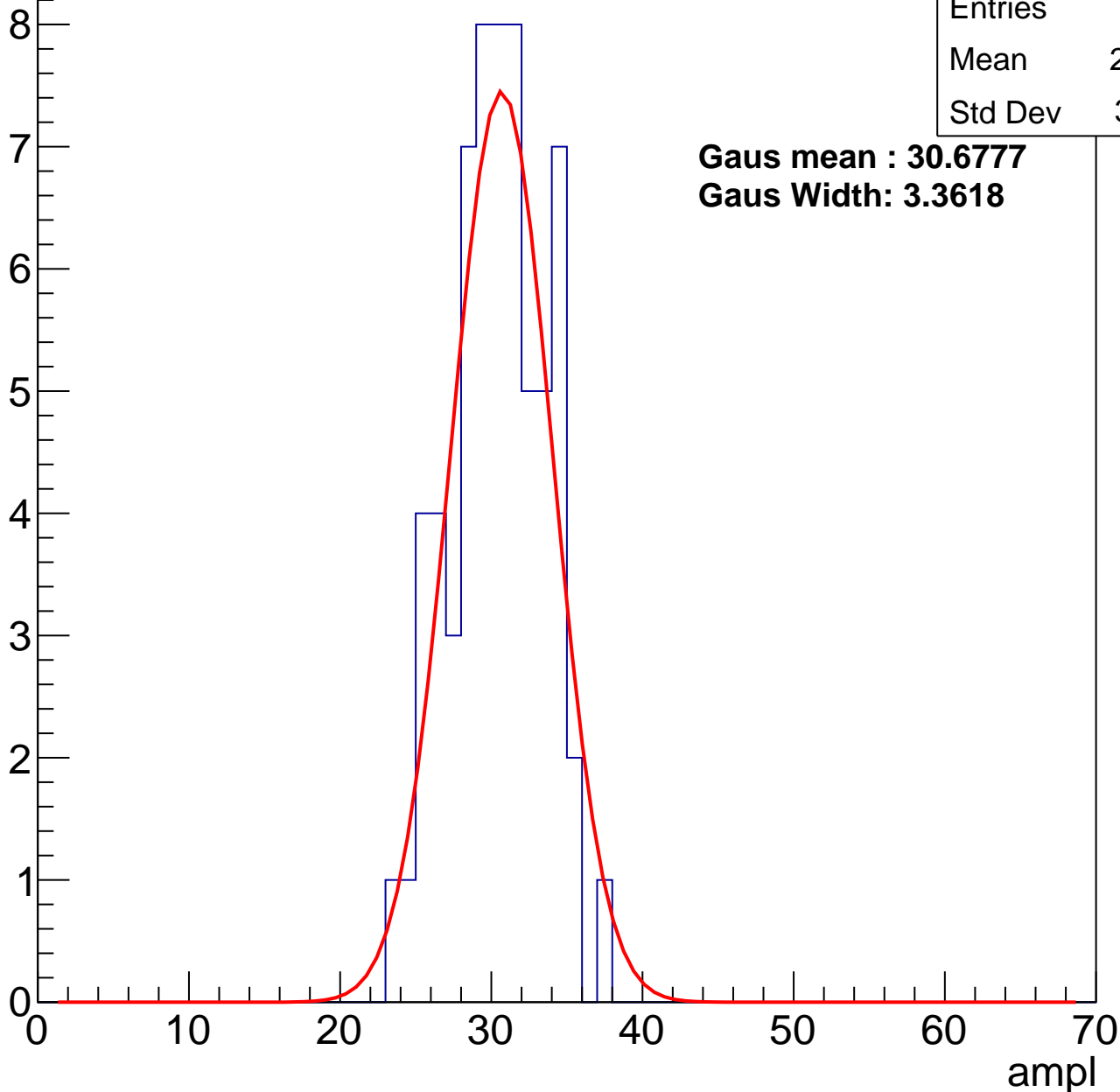
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	29.97
Std Dev	3.051

**Gaus mean : 30.6777**

**Gaus Width: 3.3618**



# B1L101S, U8-ch105, adc1

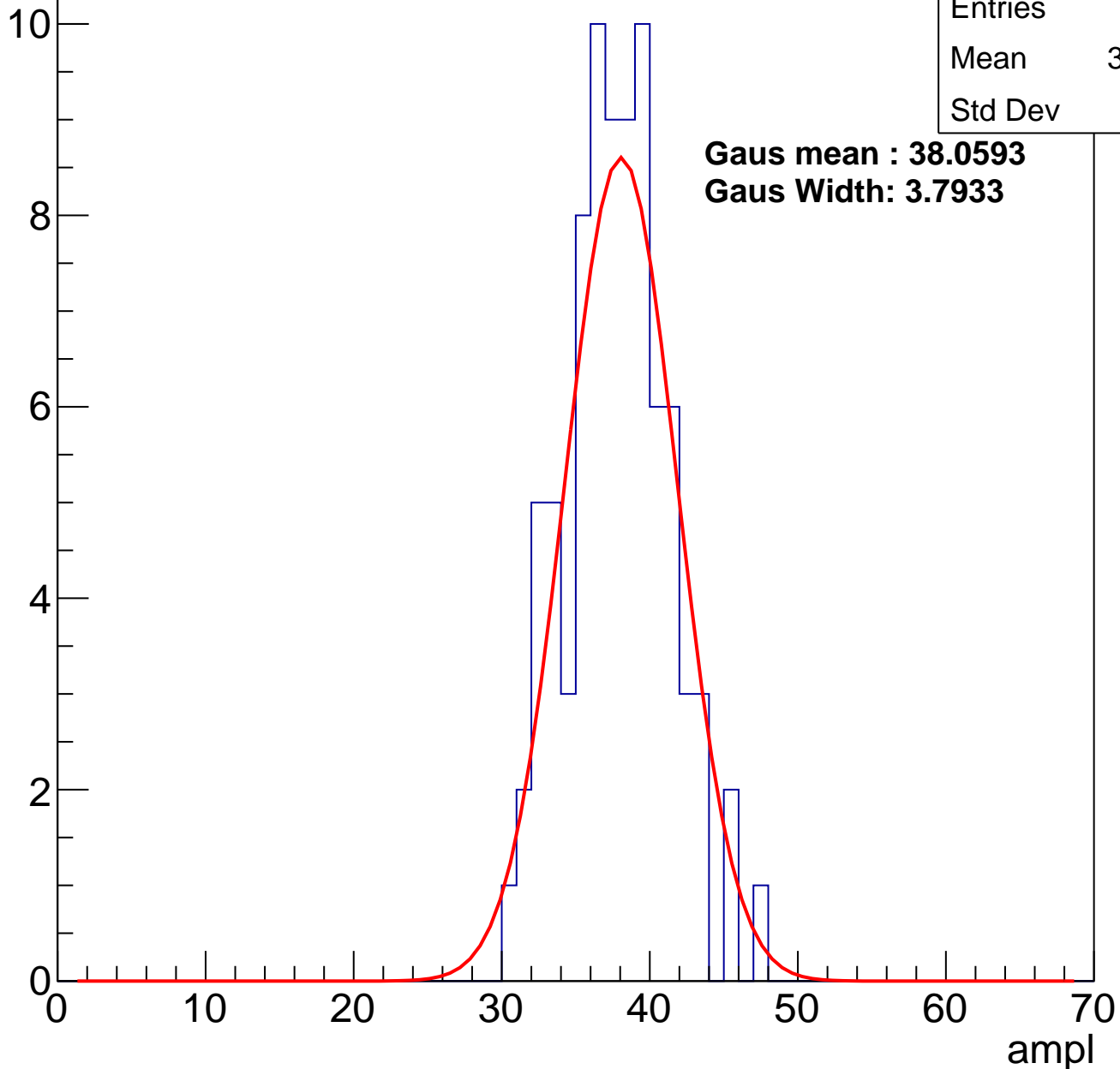
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	83
Mean	37.37
Std Dev	3.46

**Gaus mean : 38.0593**

**Gaus Width: 3.7933**

Entry



# B1L101S, U8-ch105, adc2

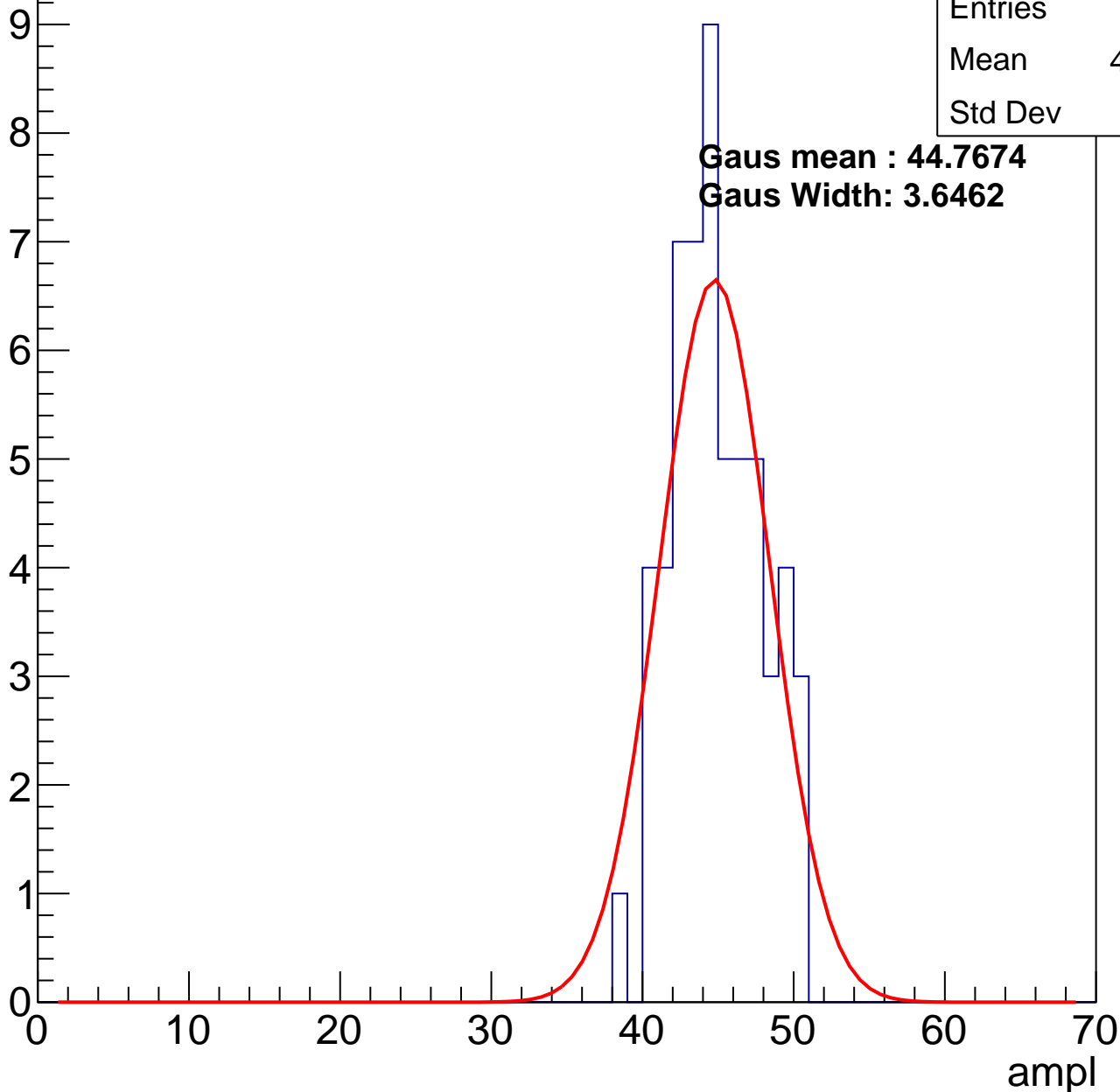
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	44.44
Std Dev	2.92

**Gaus mean : 44.7674**

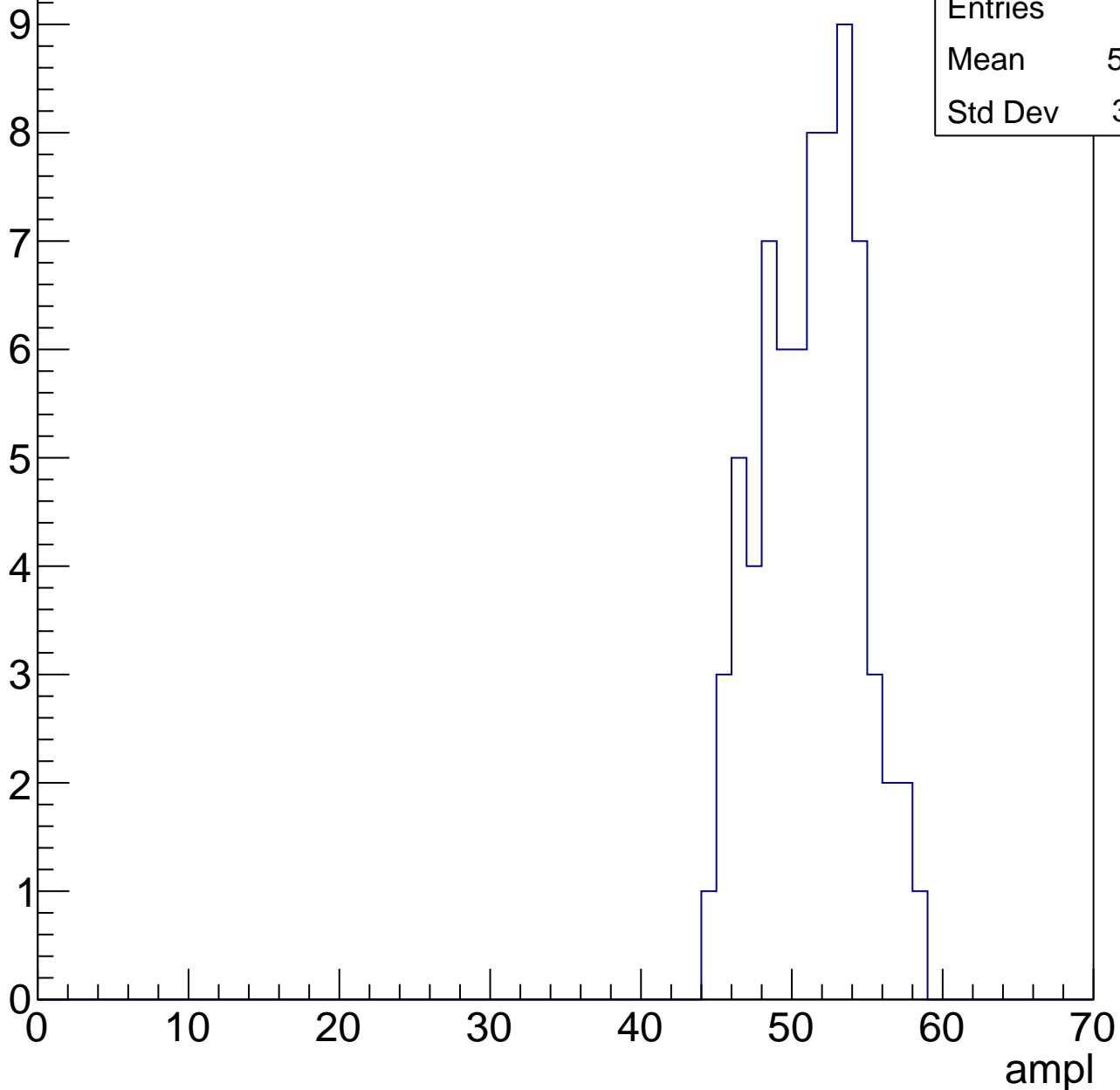
**Gaus Width: 3.6462**



# B1L101S, U8-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

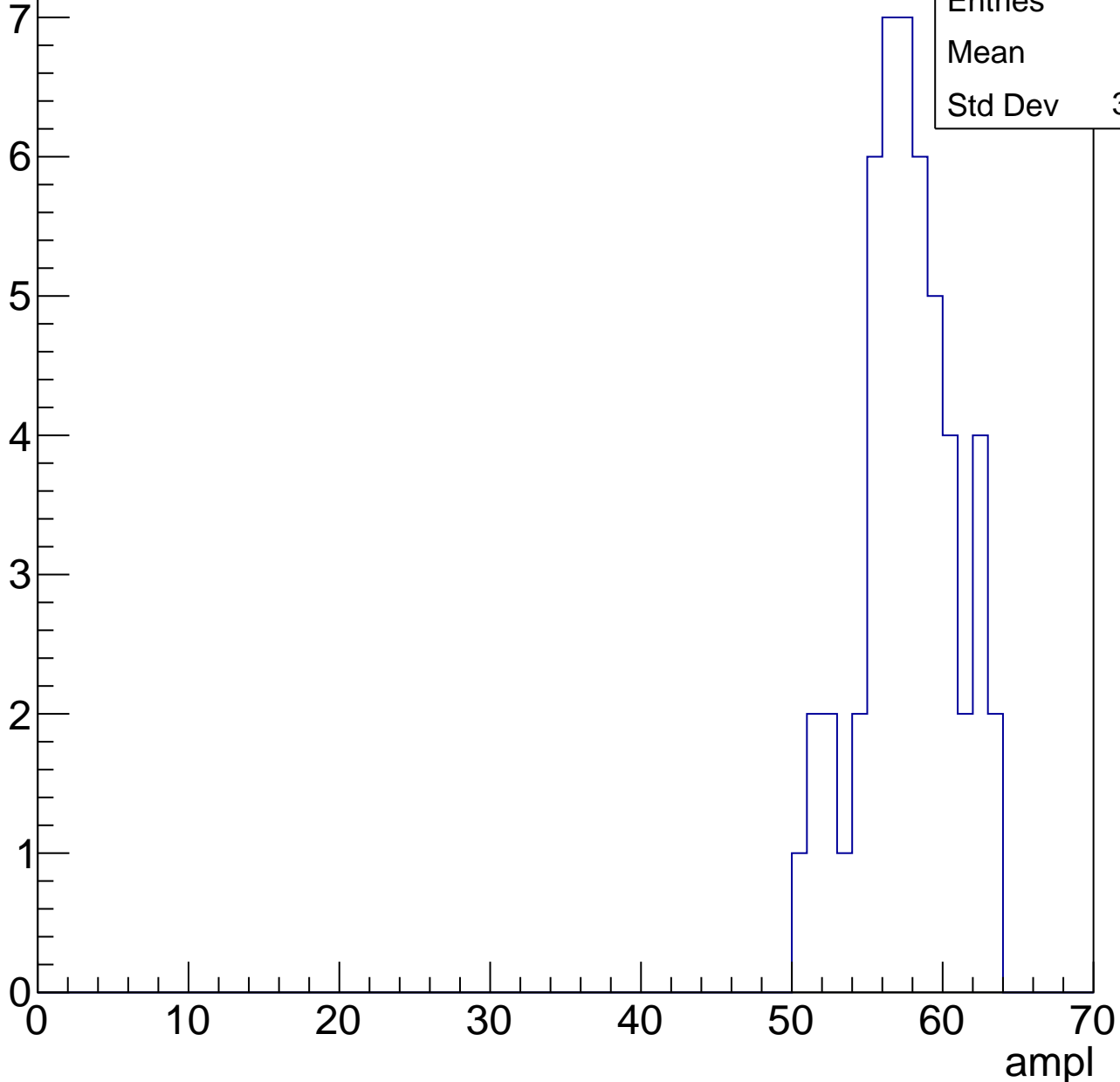


# B1L101S, U8-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	57.2
Std Dev	3.131

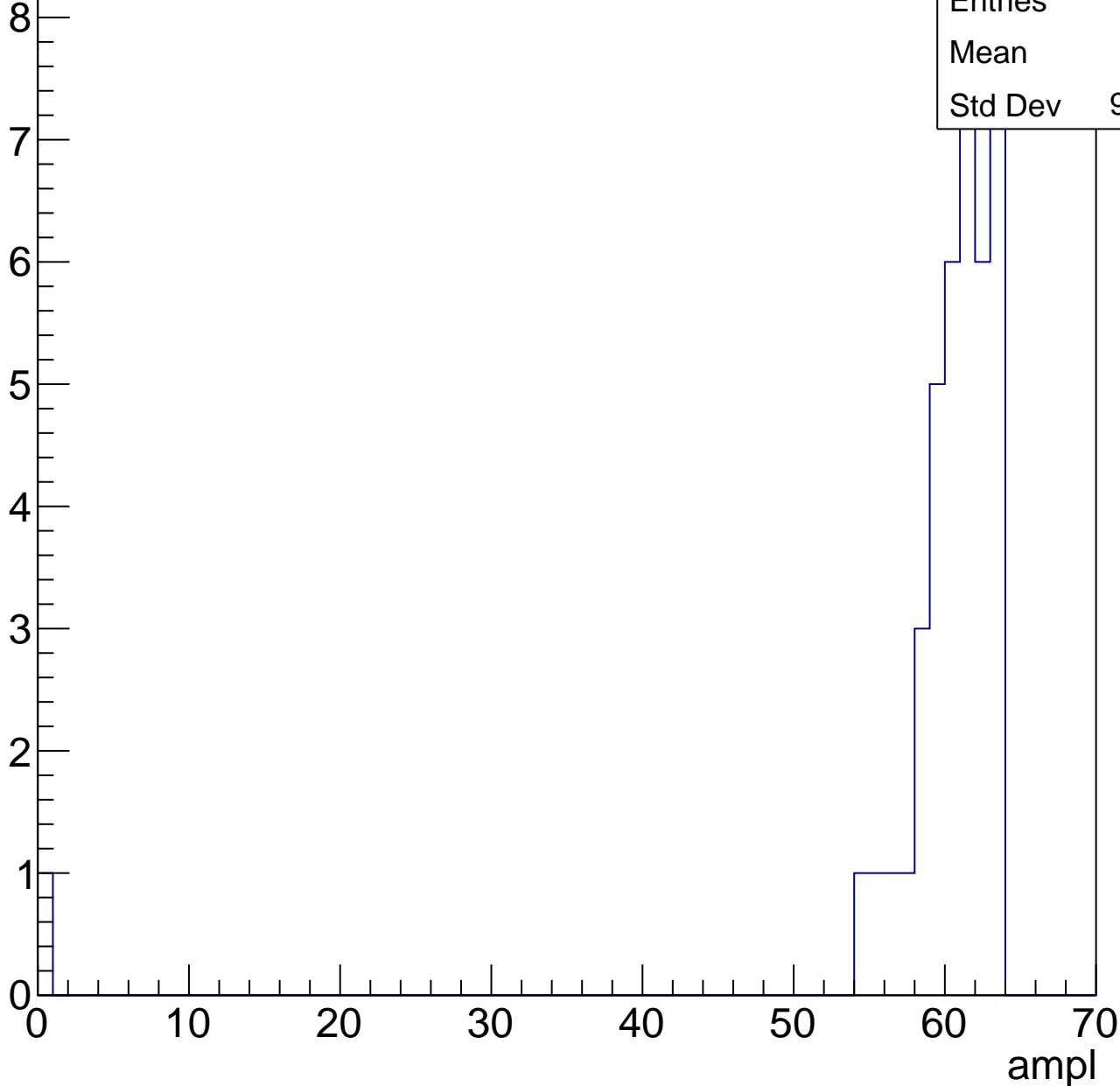


# B1L101S, U8-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	41
Mean	58.9
Std Dev	9.573



# B1L101S, U8-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L101S, U8-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

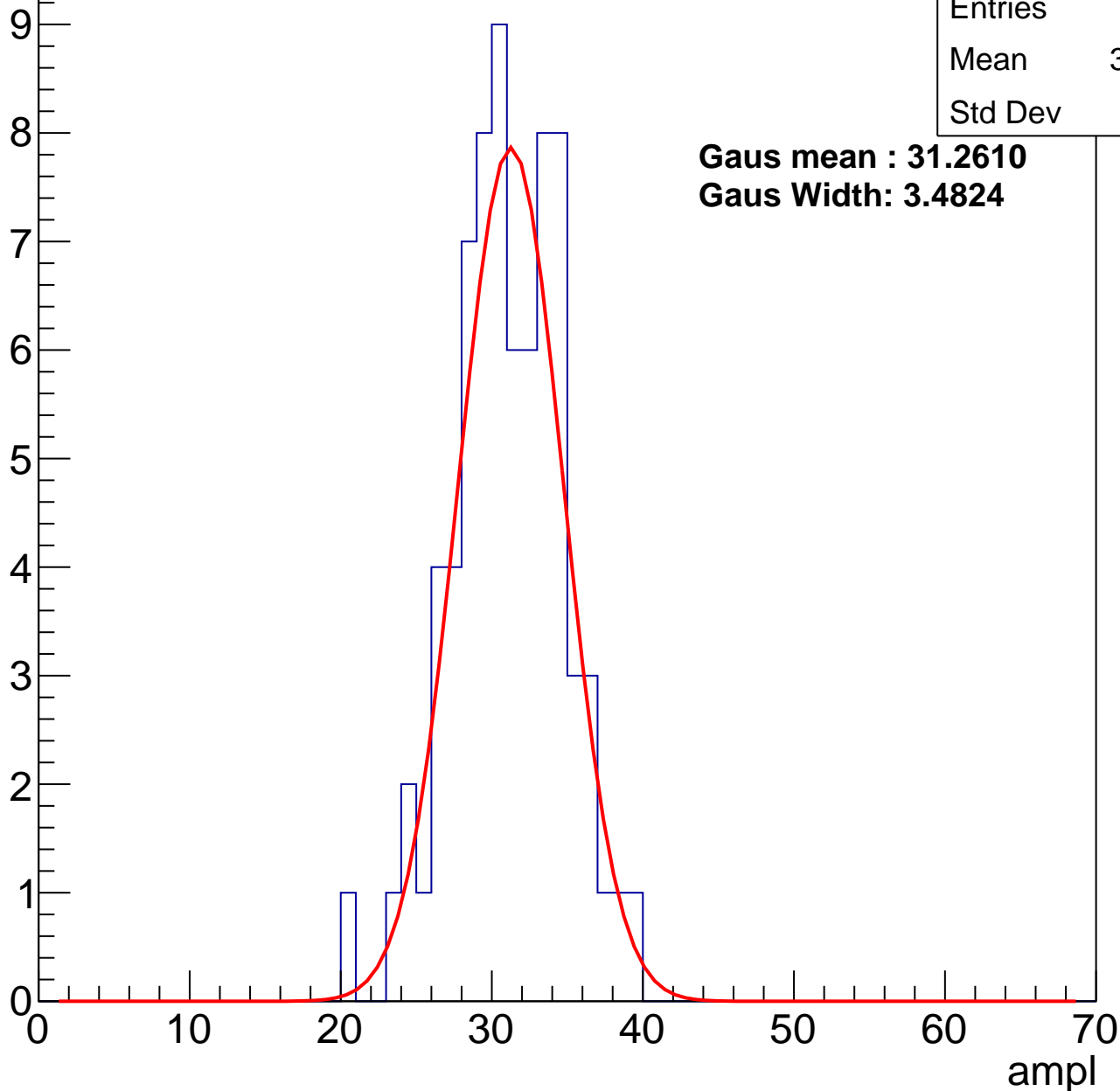


Entries	0
Mean	0
Std Dev	0

# B1L101S, U8-ch106, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	74
Mean	30.64
Std Dev	3.6

# B1L101S, U8-ch106, adc1

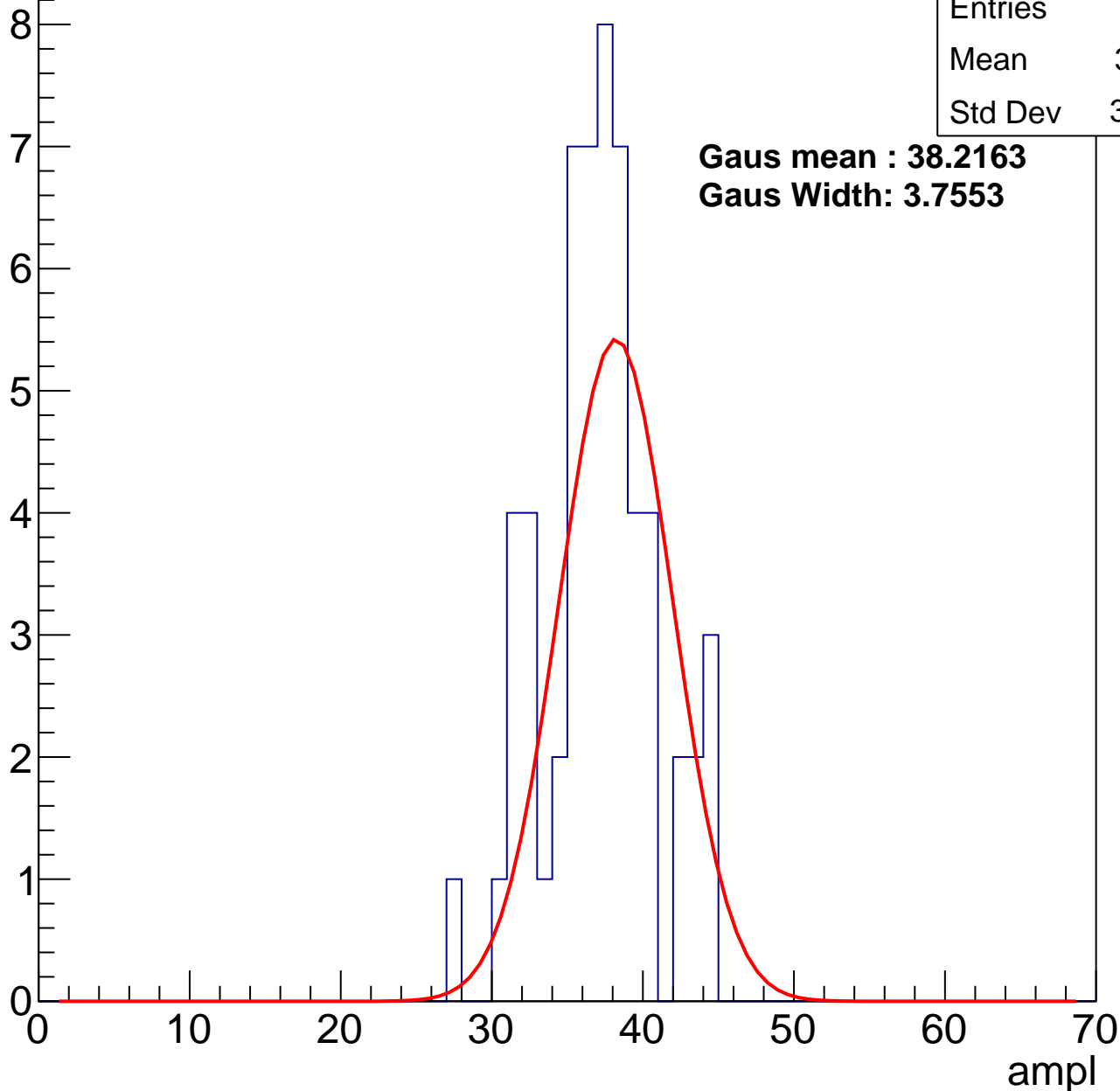
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	36.61
Std Dev	3.703

**Gaus mean : 38.2163**

**Gaus Width: 3.7553**



# B1L101S, U8-ch106, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	77
Mean	43.75
Std Dev	3.476

**Gaus mean : 43.9869**

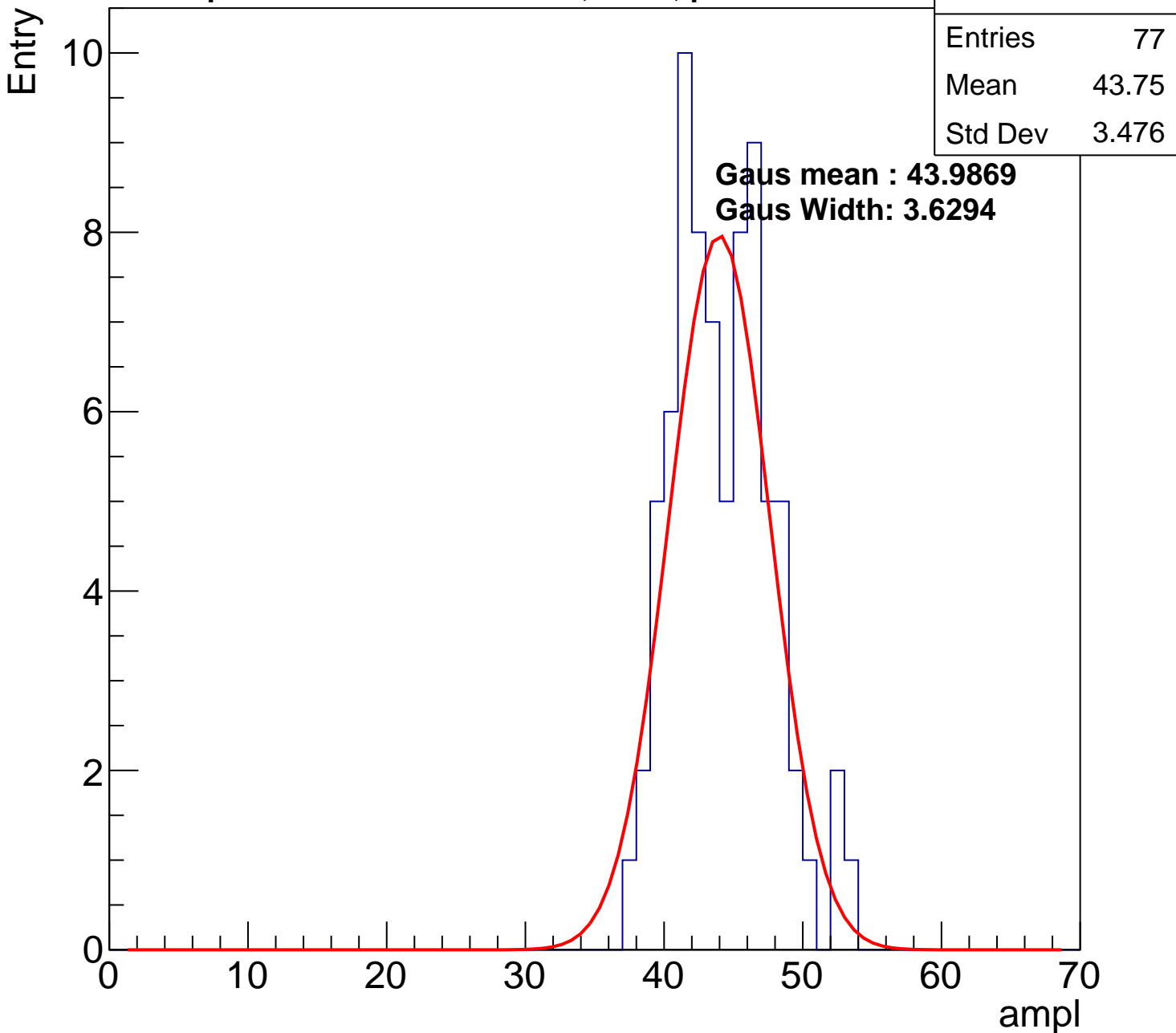
**Gaus Width: 3.6294**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

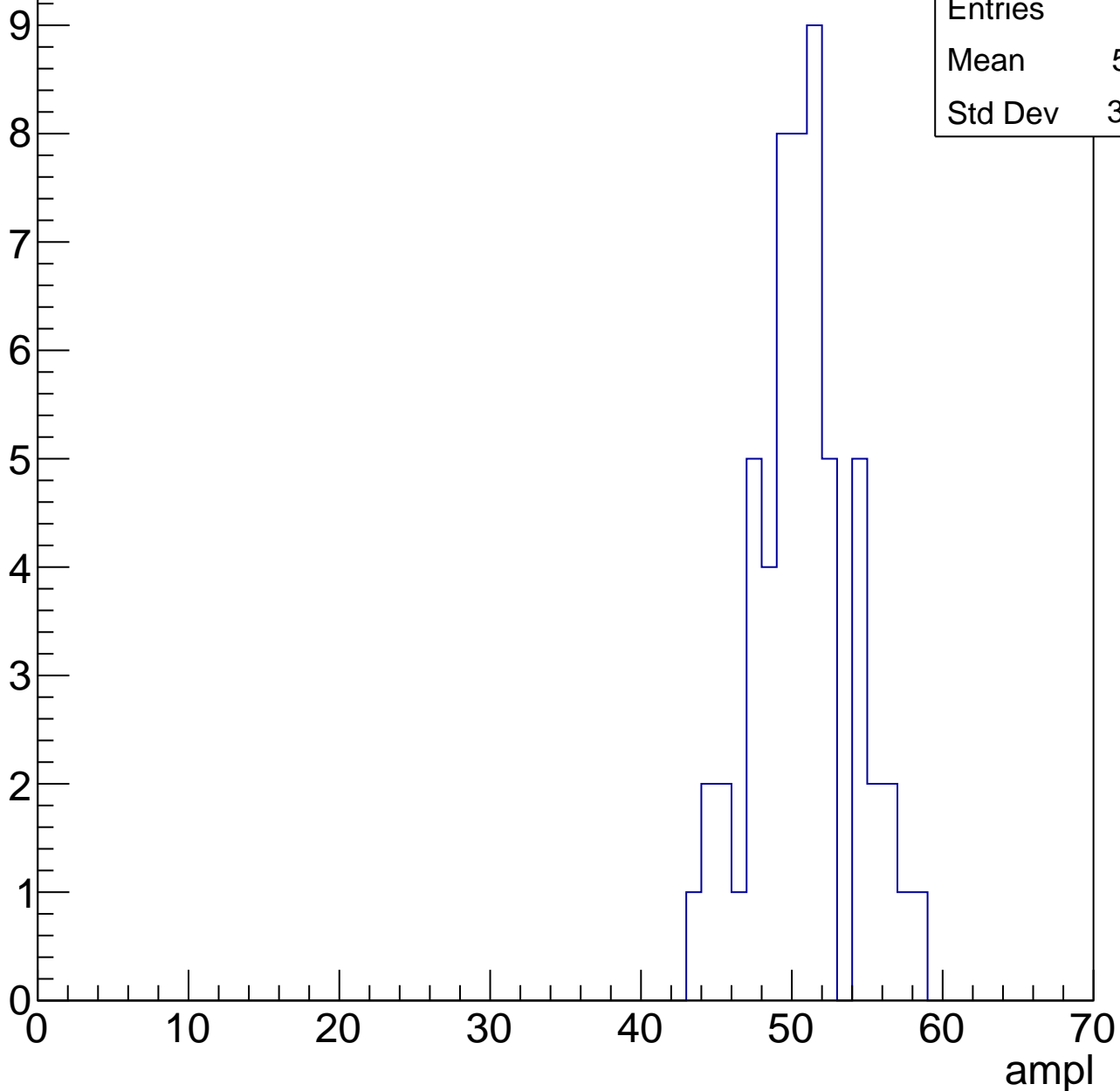


# B1L101S, U8-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	50.21
Std Dev	3.266

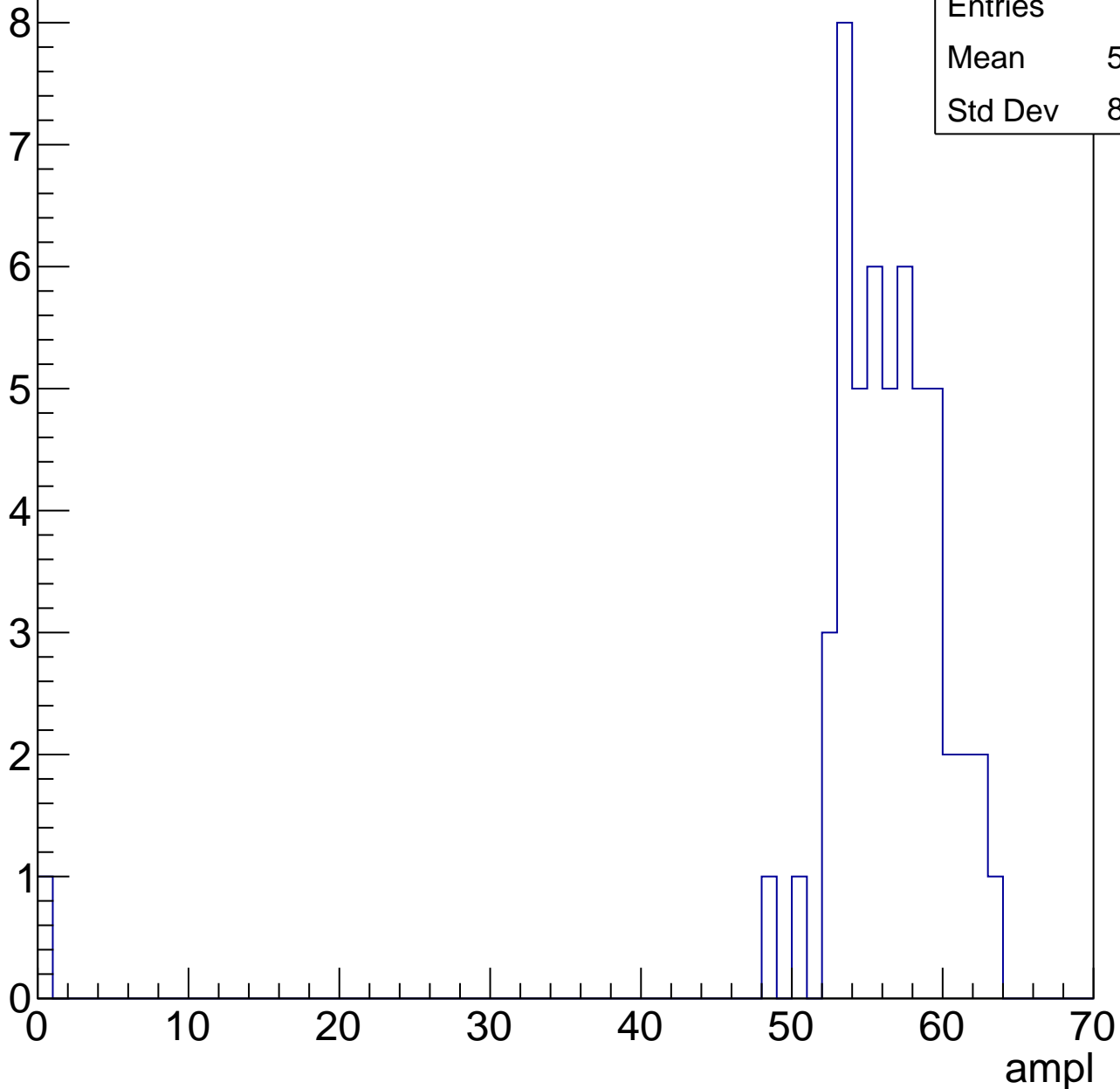


# B1L101S, U8-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

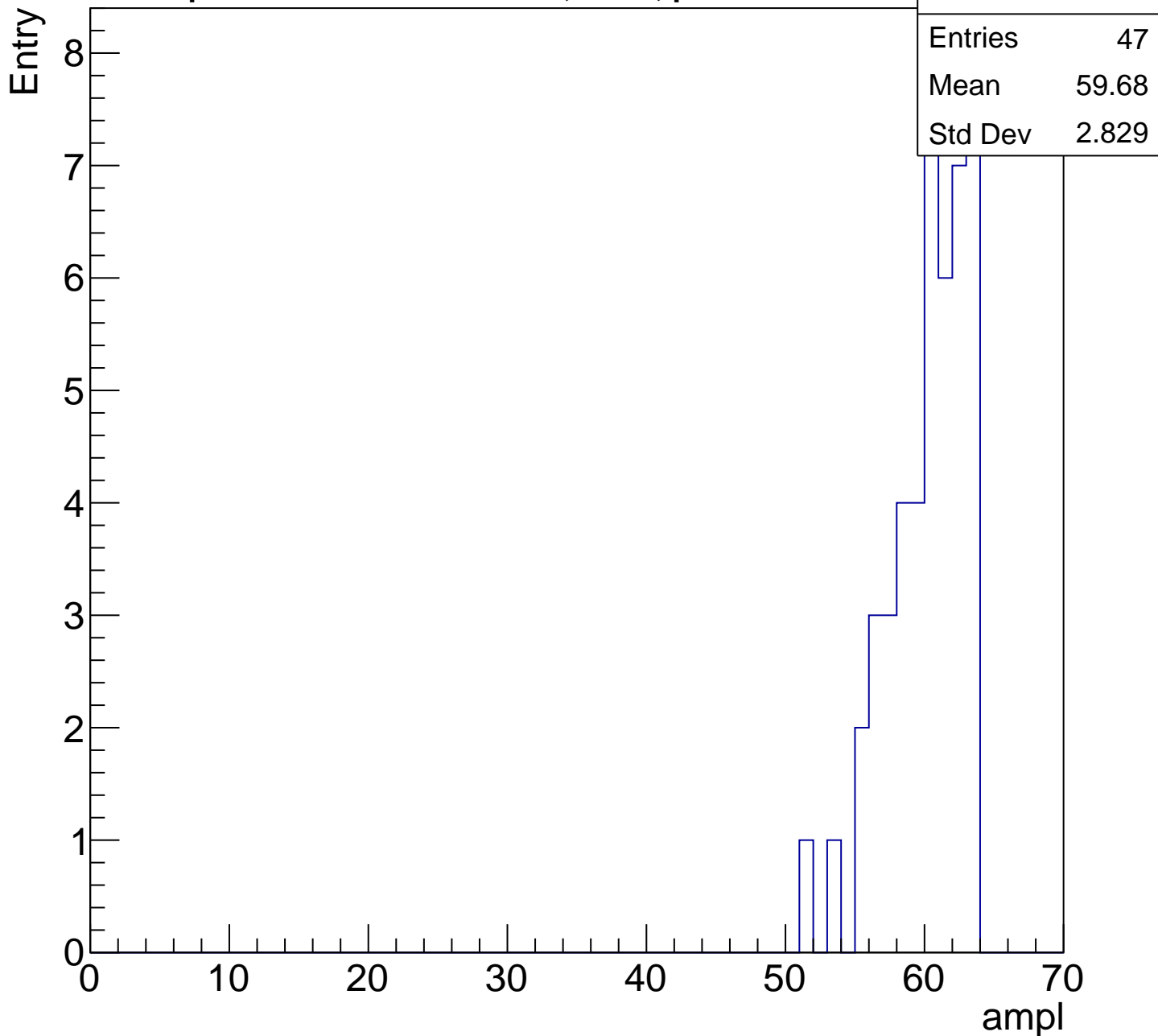
Entry

Entries	53
Mean	54.98
Std Dev	8.243



# B1L101S, U8-ch106, adc5

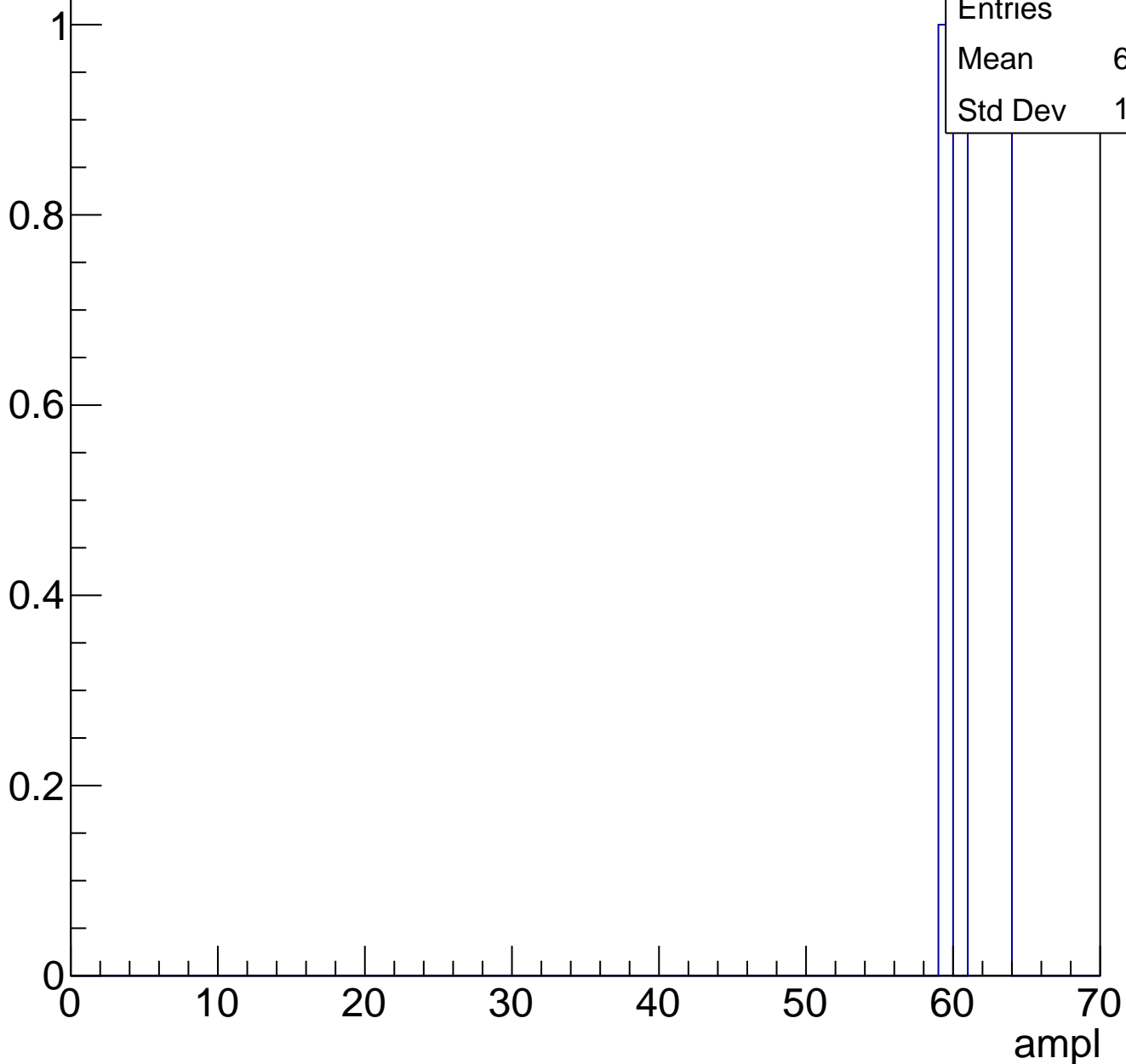
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U8-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

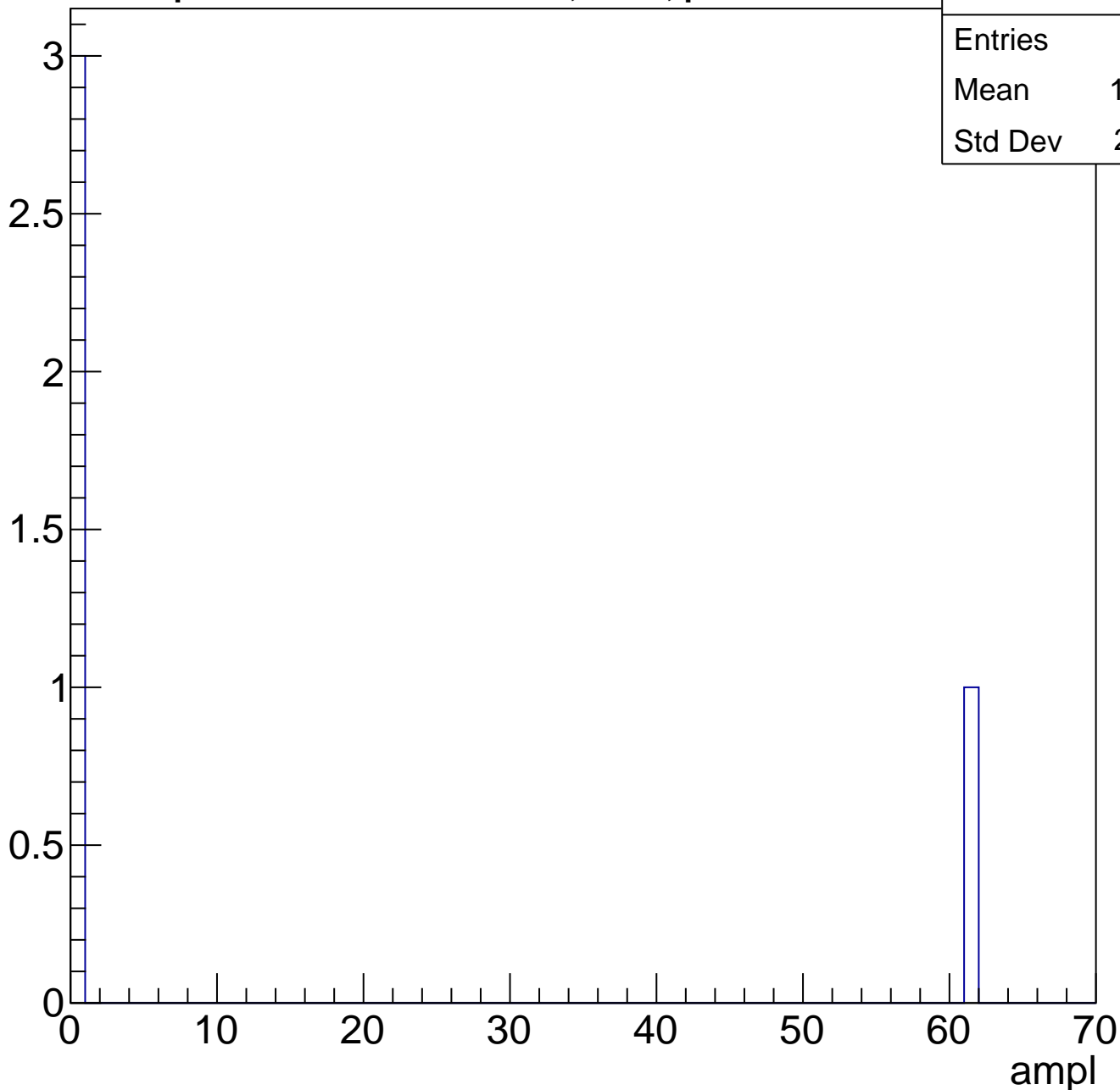




# B1L101S, U8-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch107, adc0

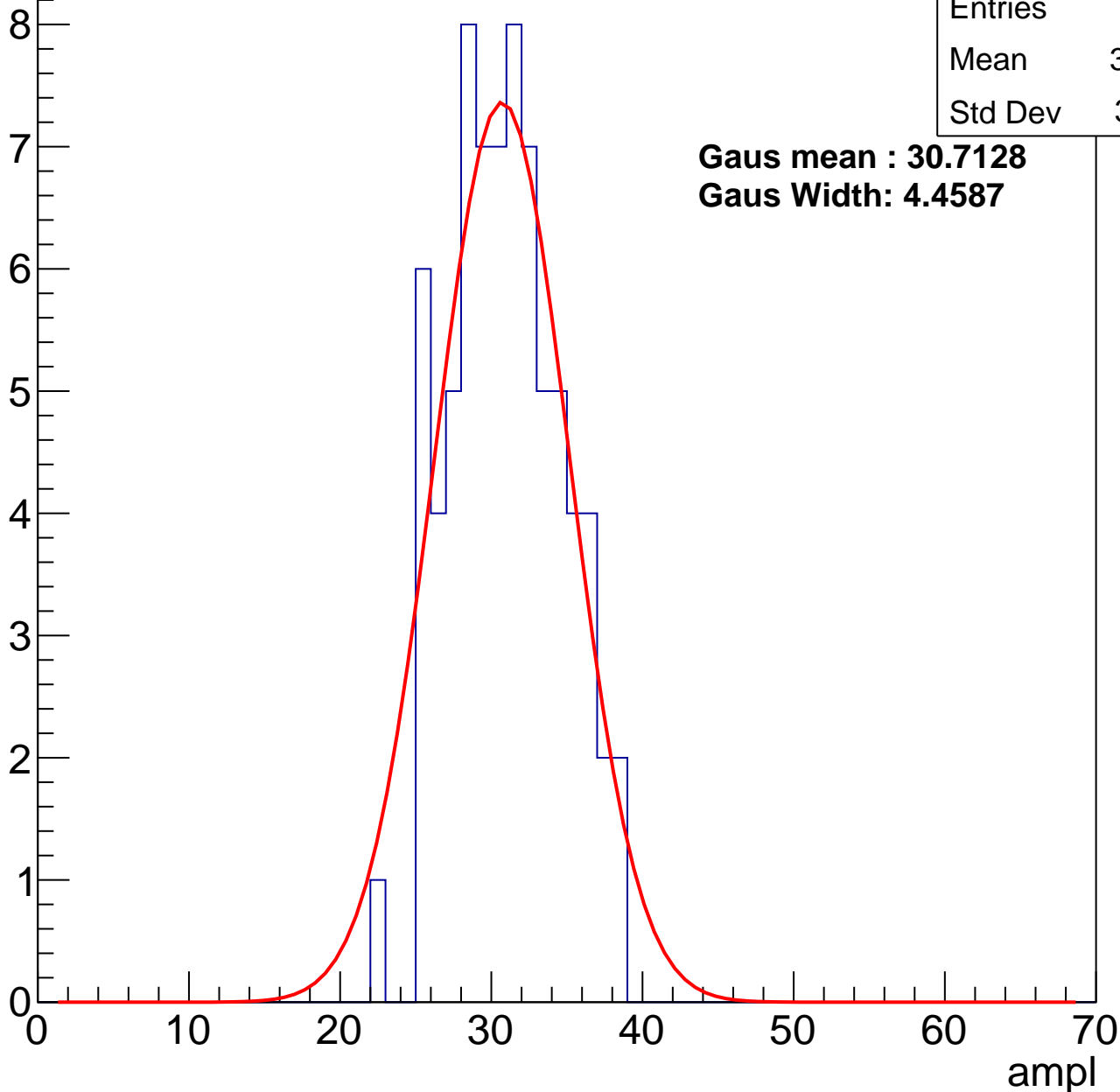
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	30.52
Std Dev	3.601

**Gaus mean : 30.7128**

**Gaus Width: 4.4587**



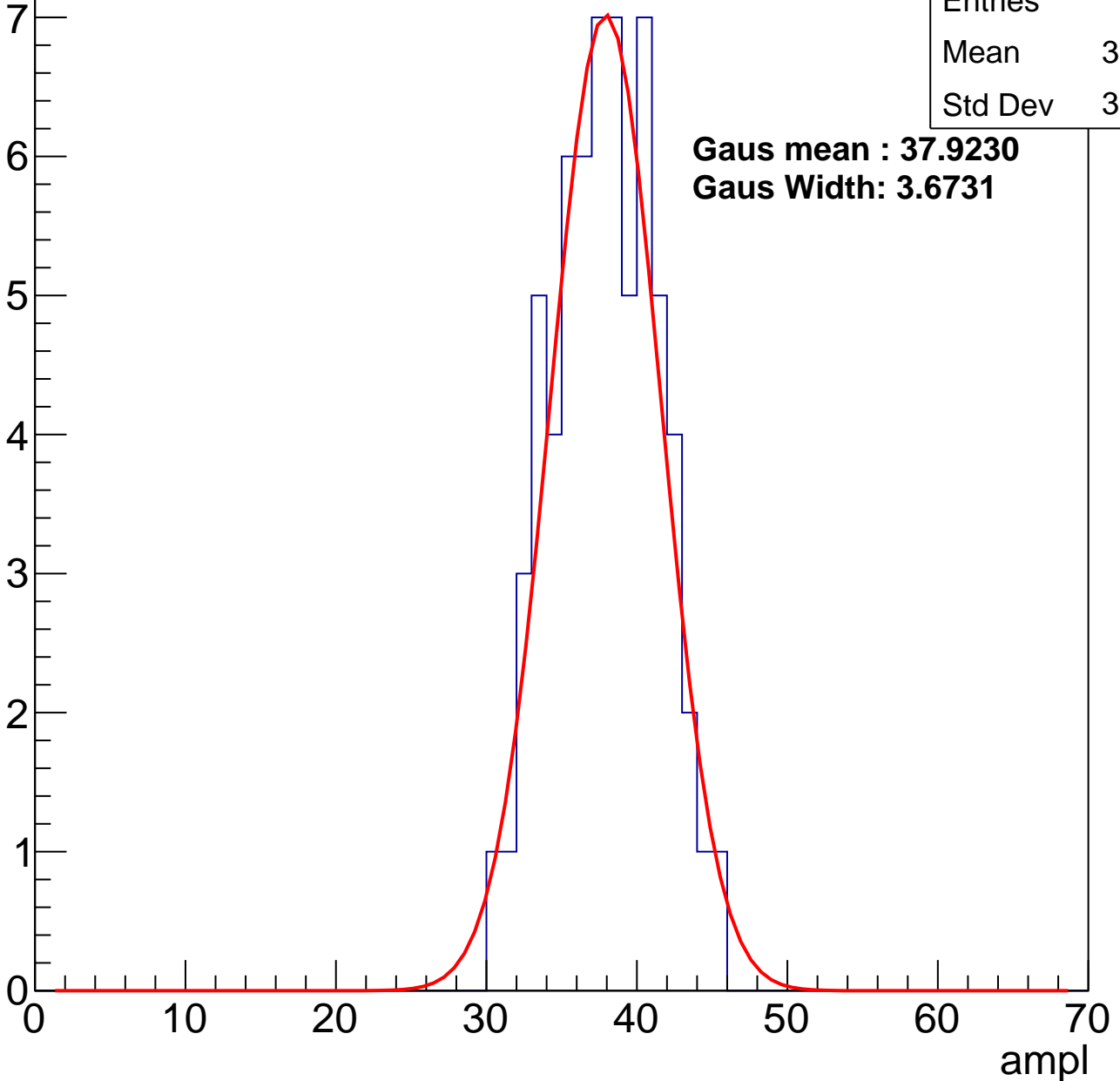
# B1L101S, U8-ch107, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	37.42
Std Dev	3.396

**Gaus mean : 37.9230**  
**Gaus Width: 3.6731**



# B1L101S, U8-ch107, adc2

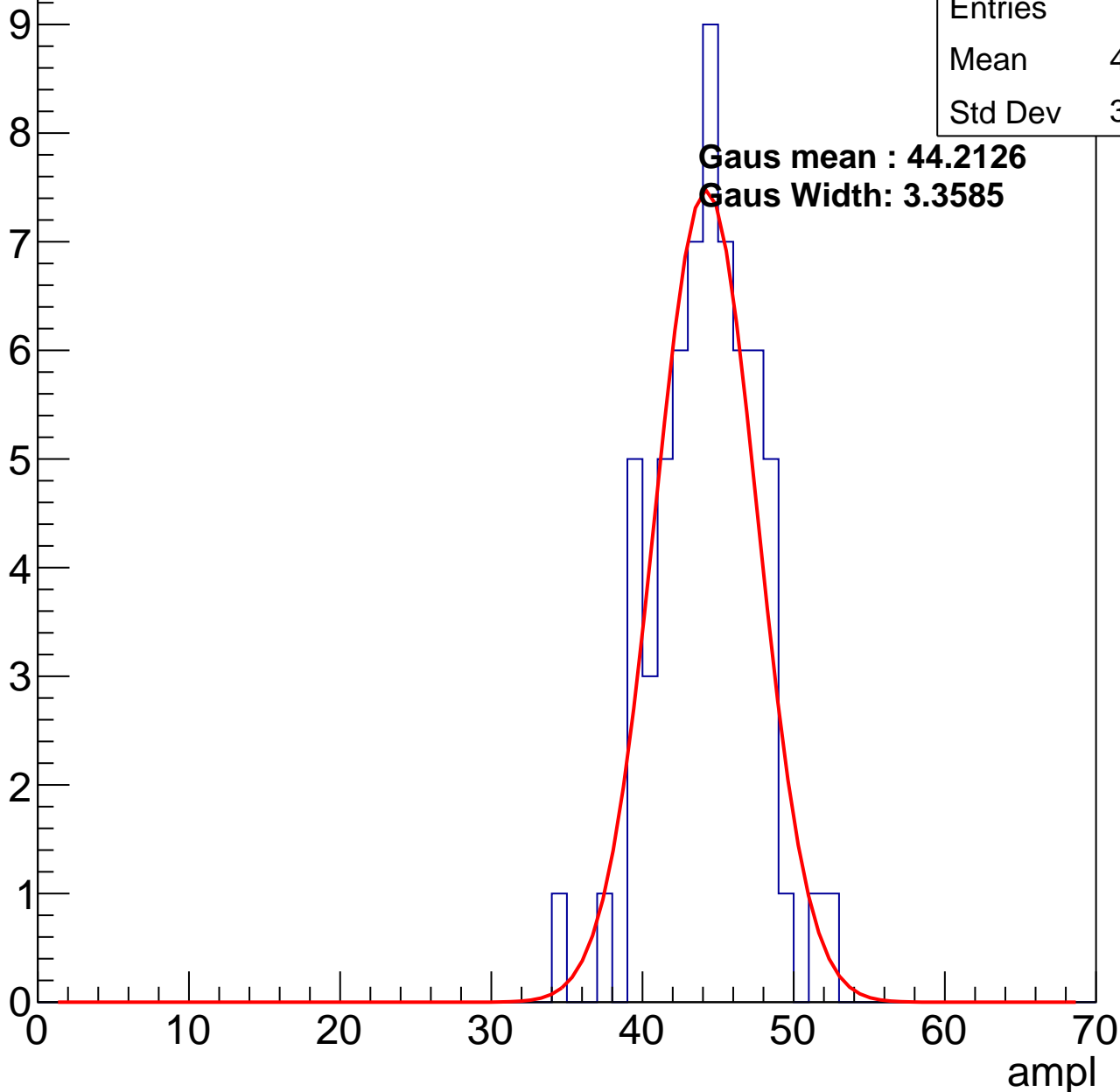
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	43.83
Std Dev	3.305

**Gaus mean : 44.2126**

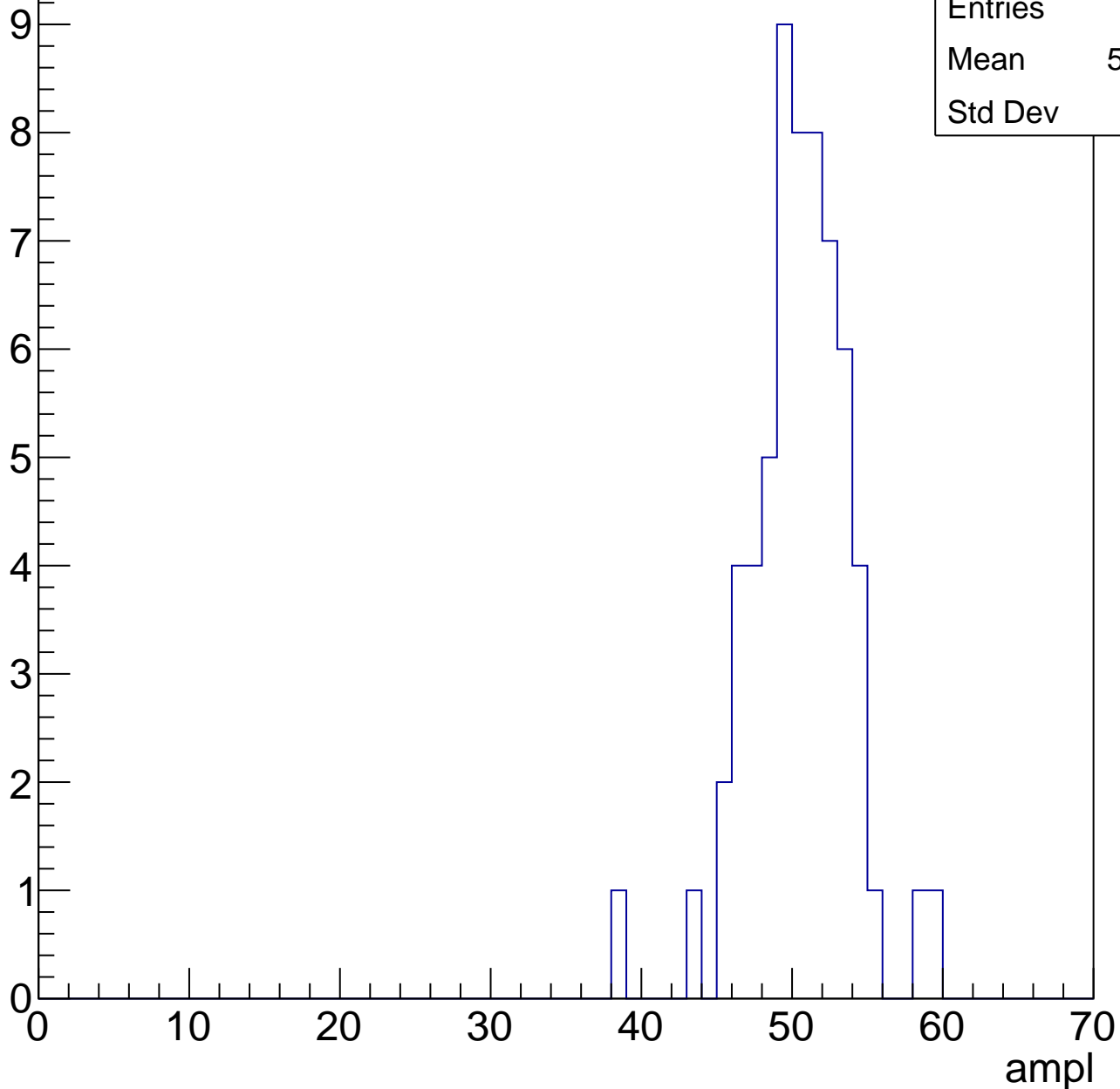
**Gaus Width: 3.3585**



# B1L101S, U8-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



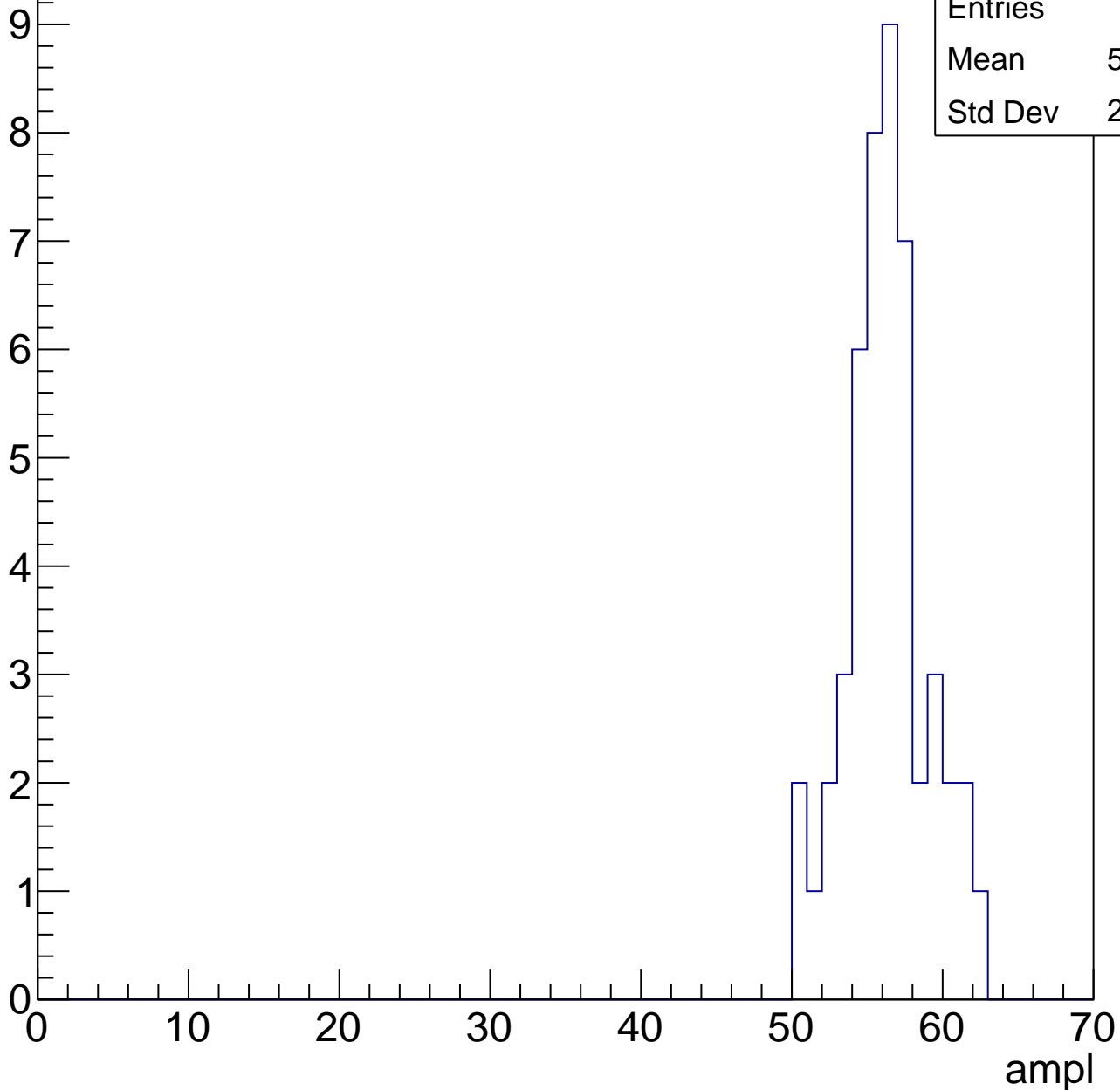
Entries	62
Mean	50.03
Std Dev	3.35

# B1L101S, U8-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	55.79
Std Dev	2.685



# B1L101S, U8-ch107, adc5

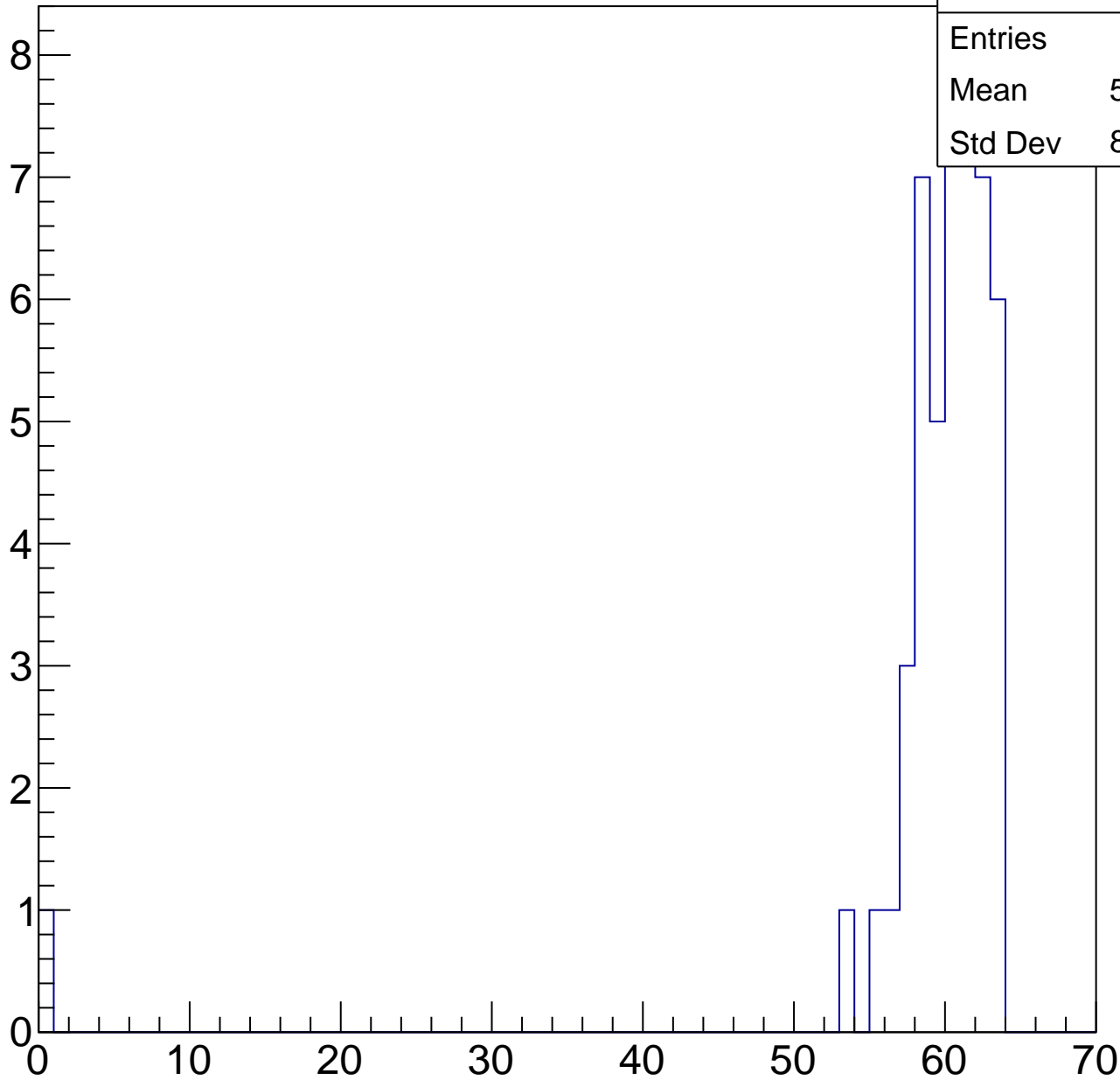
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	58.67
Std Dev	8.844

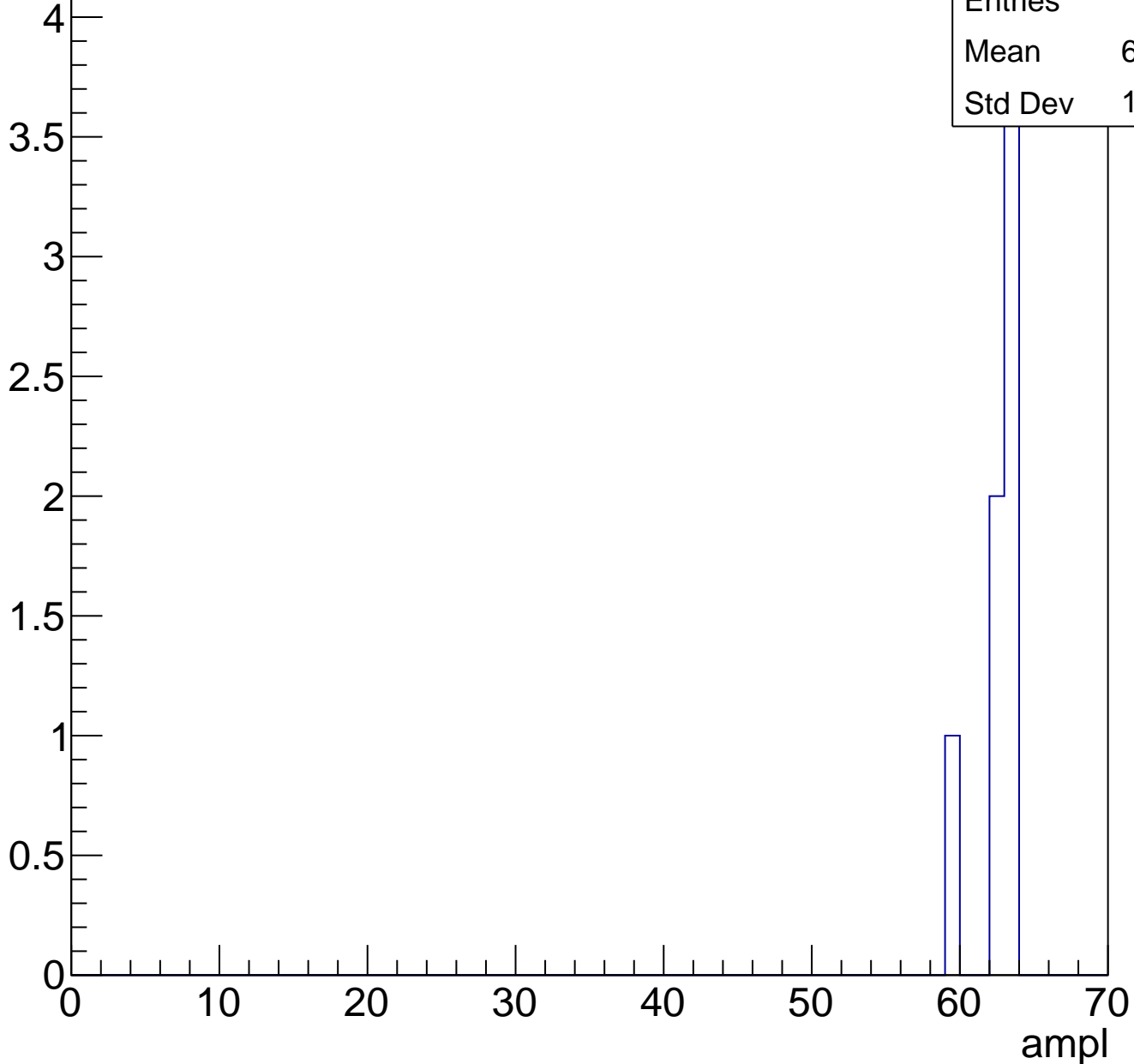
ampl



# B1L101S, U8-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch108, adc0

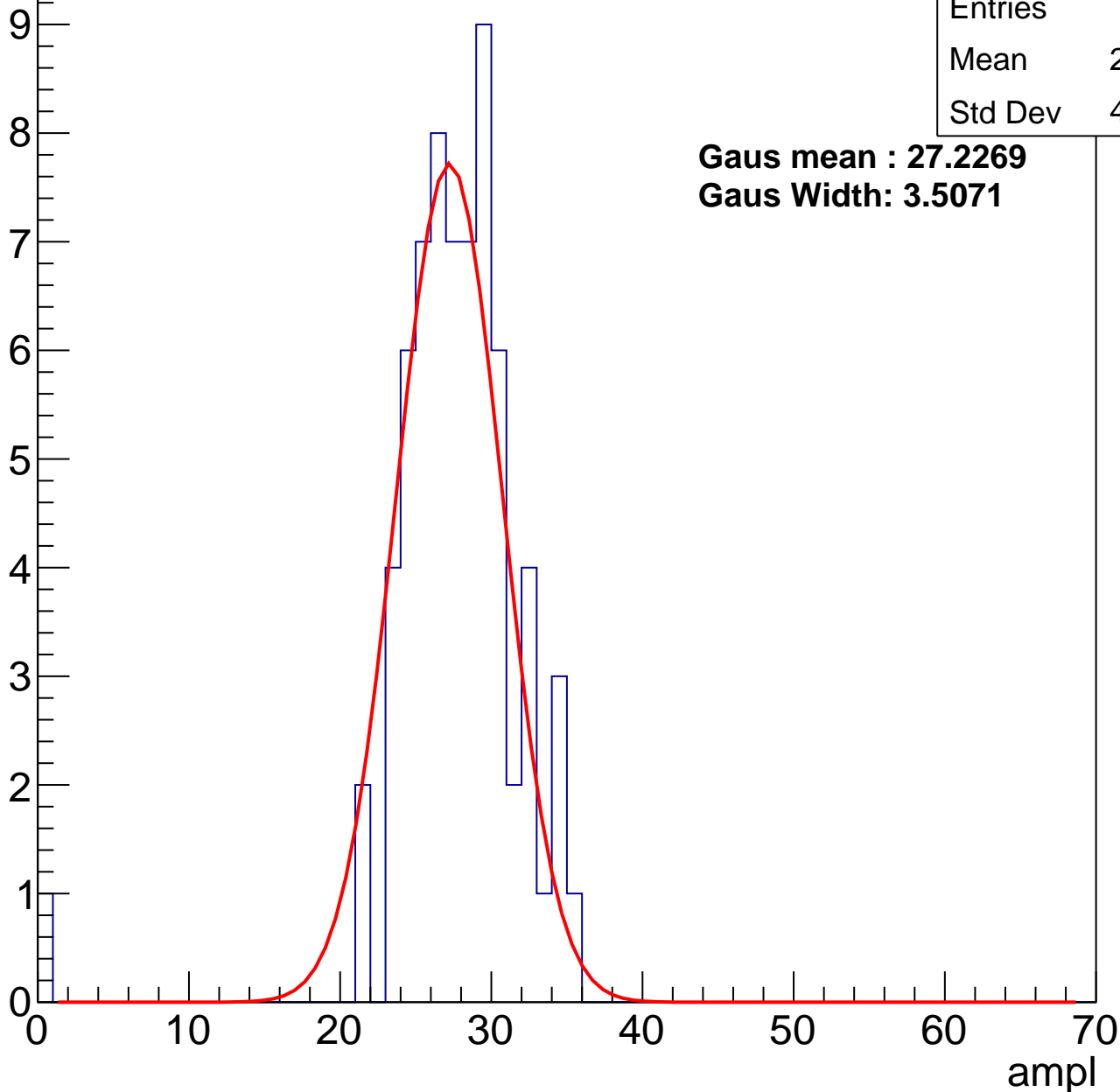
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	27.16
Std Dev	4.585

**Gaus mean : 27.2269**

**Gaus Width: 3.5071**



# B1L101S, U8-ch108, adc1

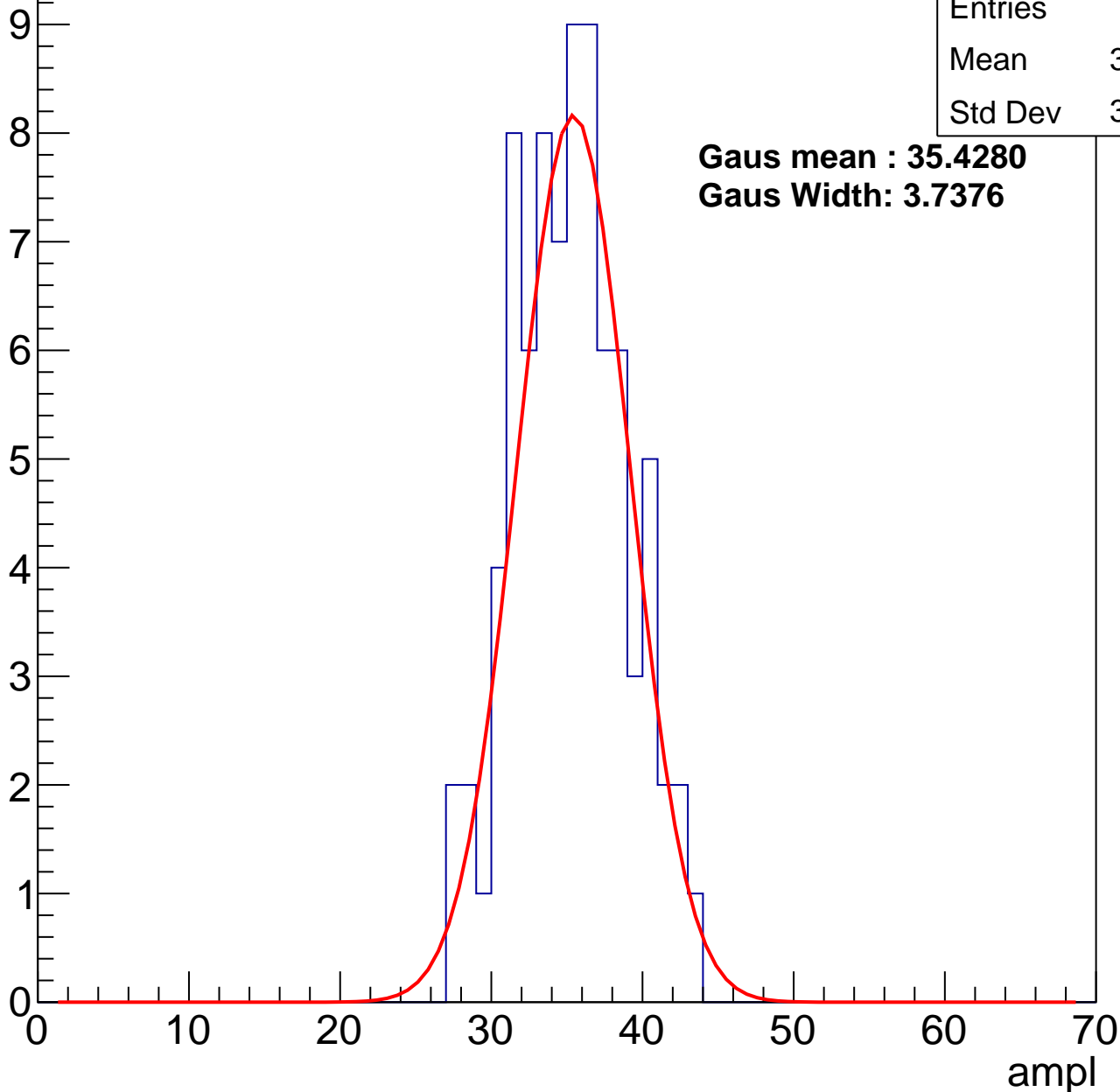
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	34.77
Std Dev	3.639

**Gaus mean : 35.4280**

**Gaus Width: 3.7376**



# B1L101S, U8-ch108, adc2

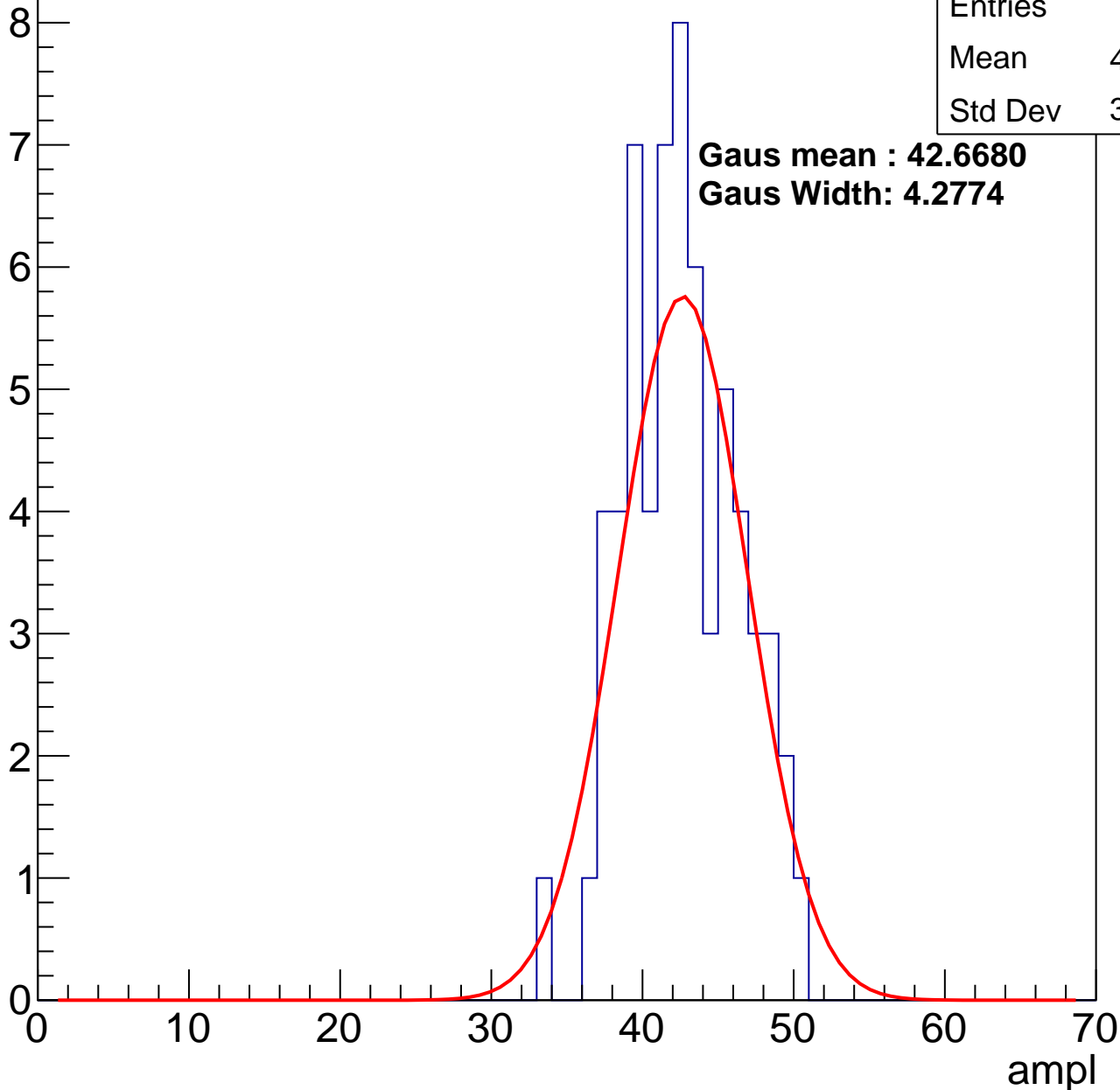
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	42.17
Std Dev	3.645

**Gaus mean : 42.6680**

**Gaus Width: 4.2774**

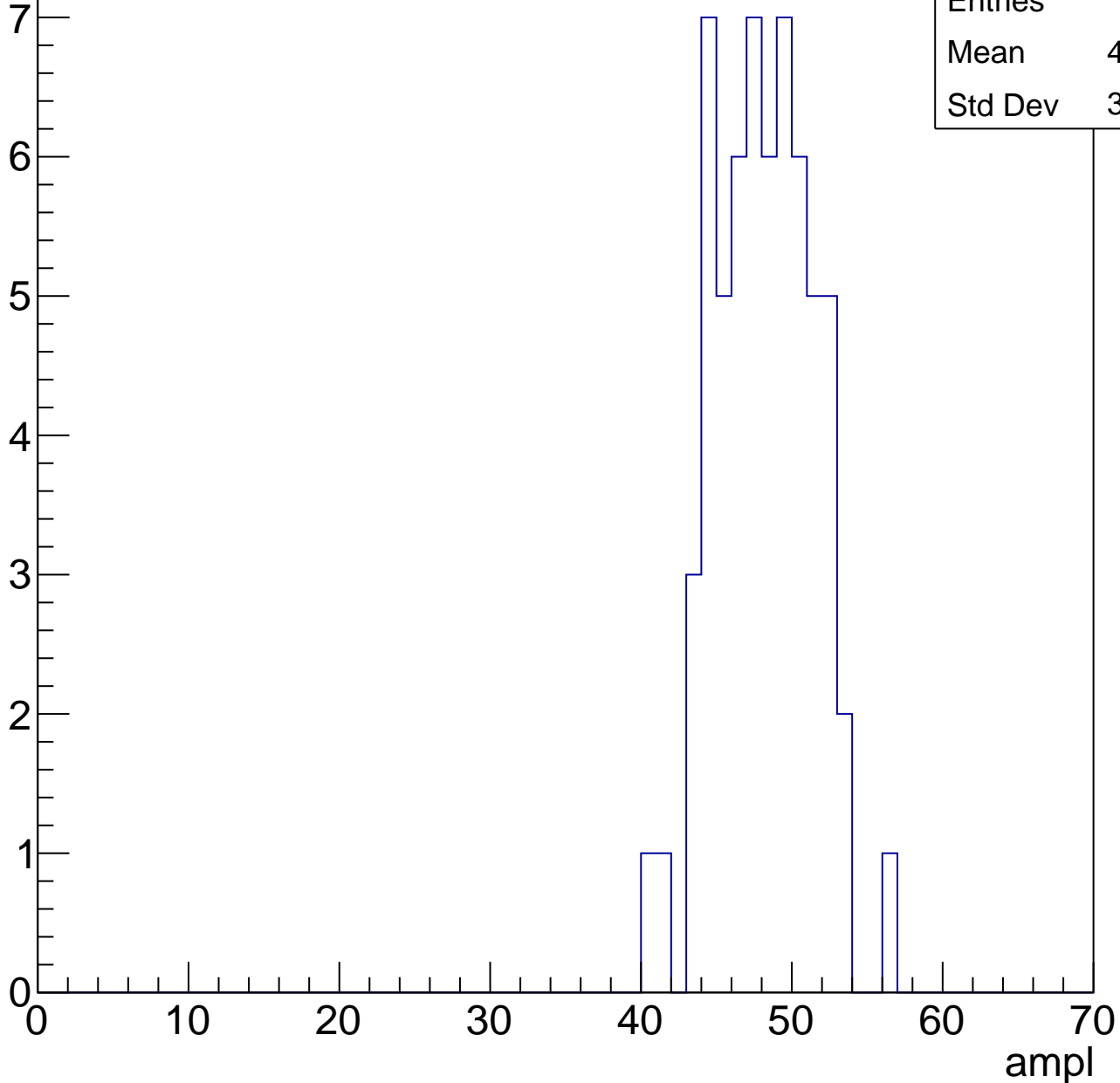


# B1L101S, U8-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	47.68
Std Dev	3.212

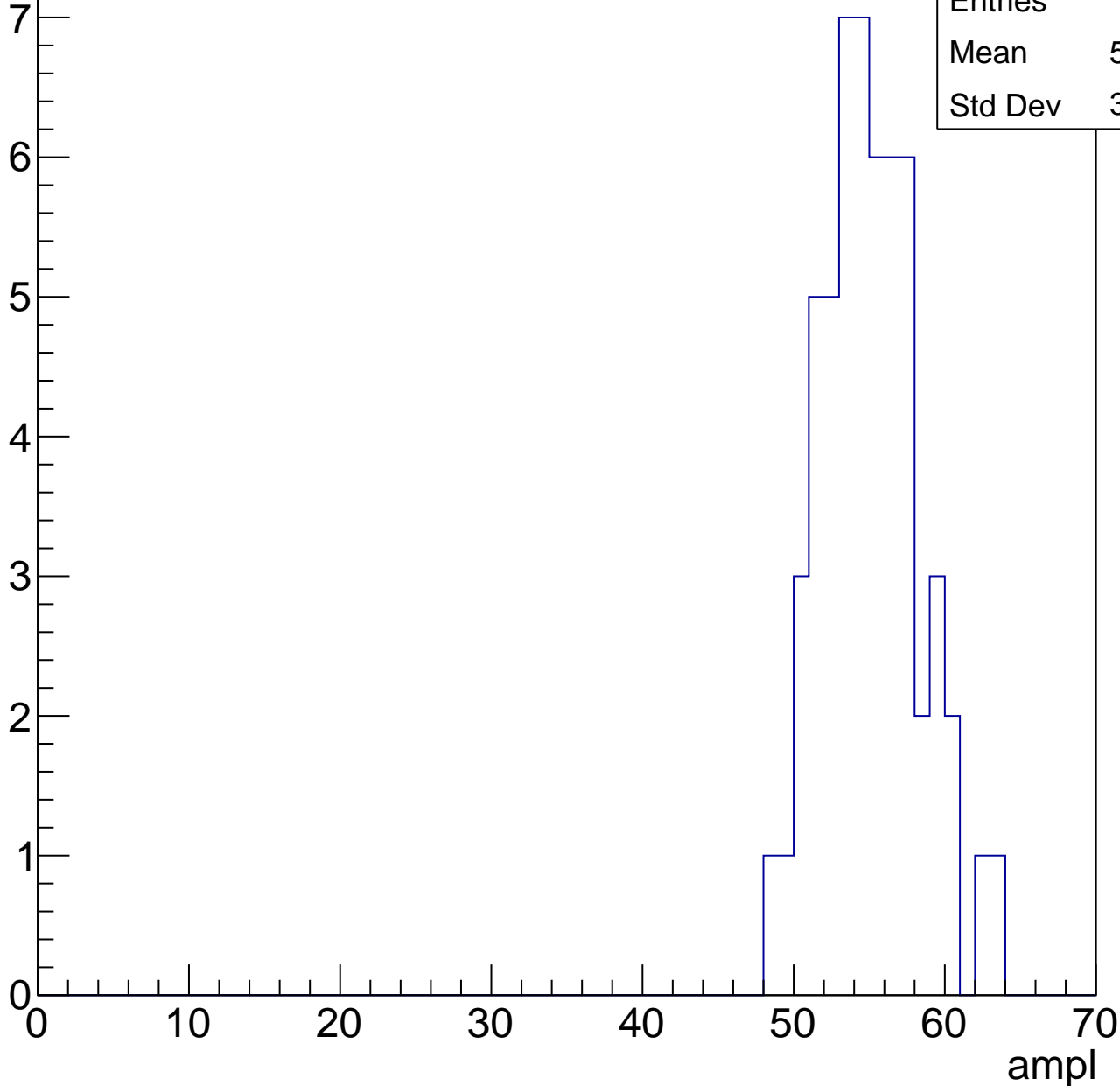


# B1L101S, U8-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	54.59
Std Dev	3.189

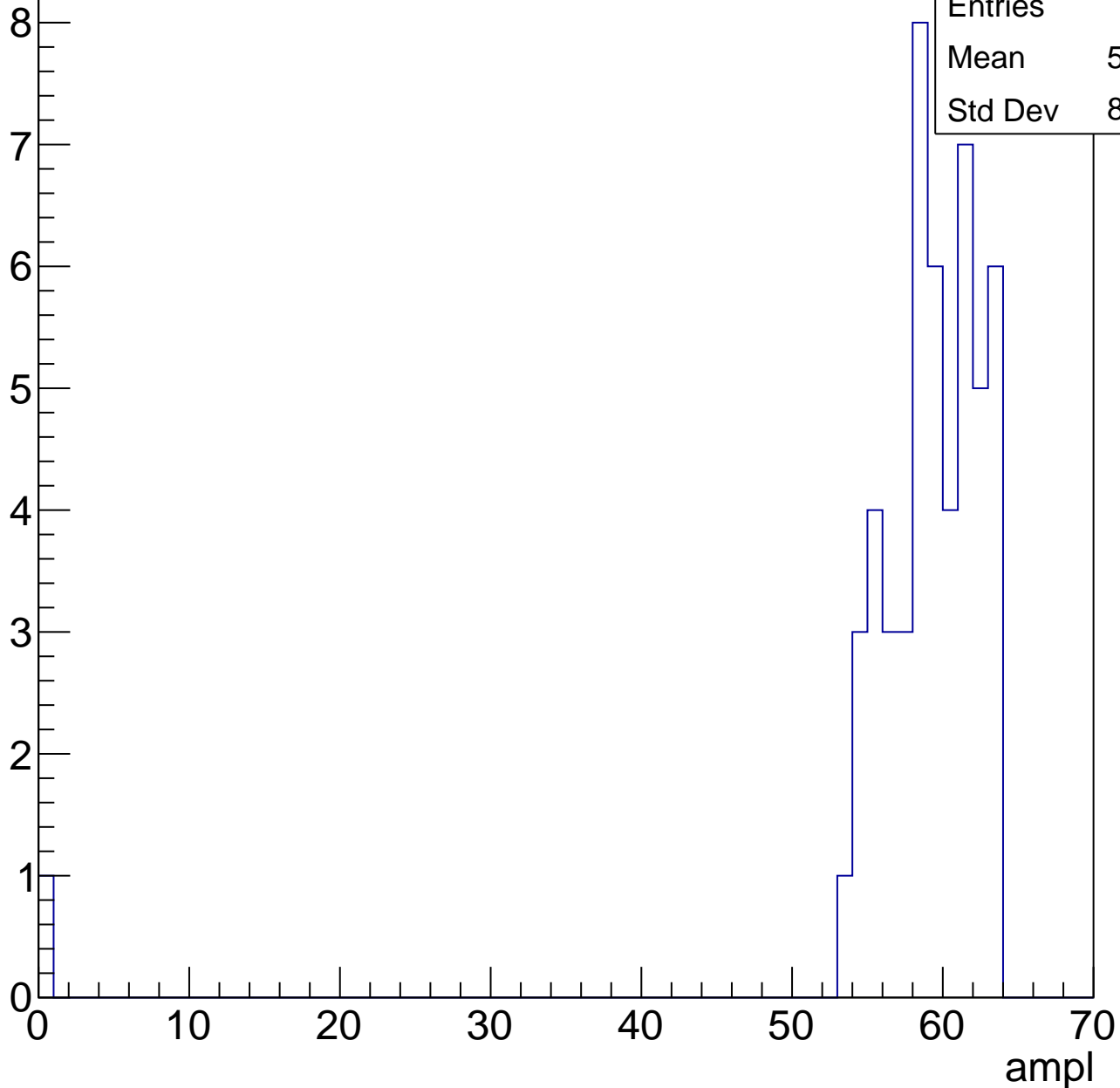


# B1L101S, U8-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

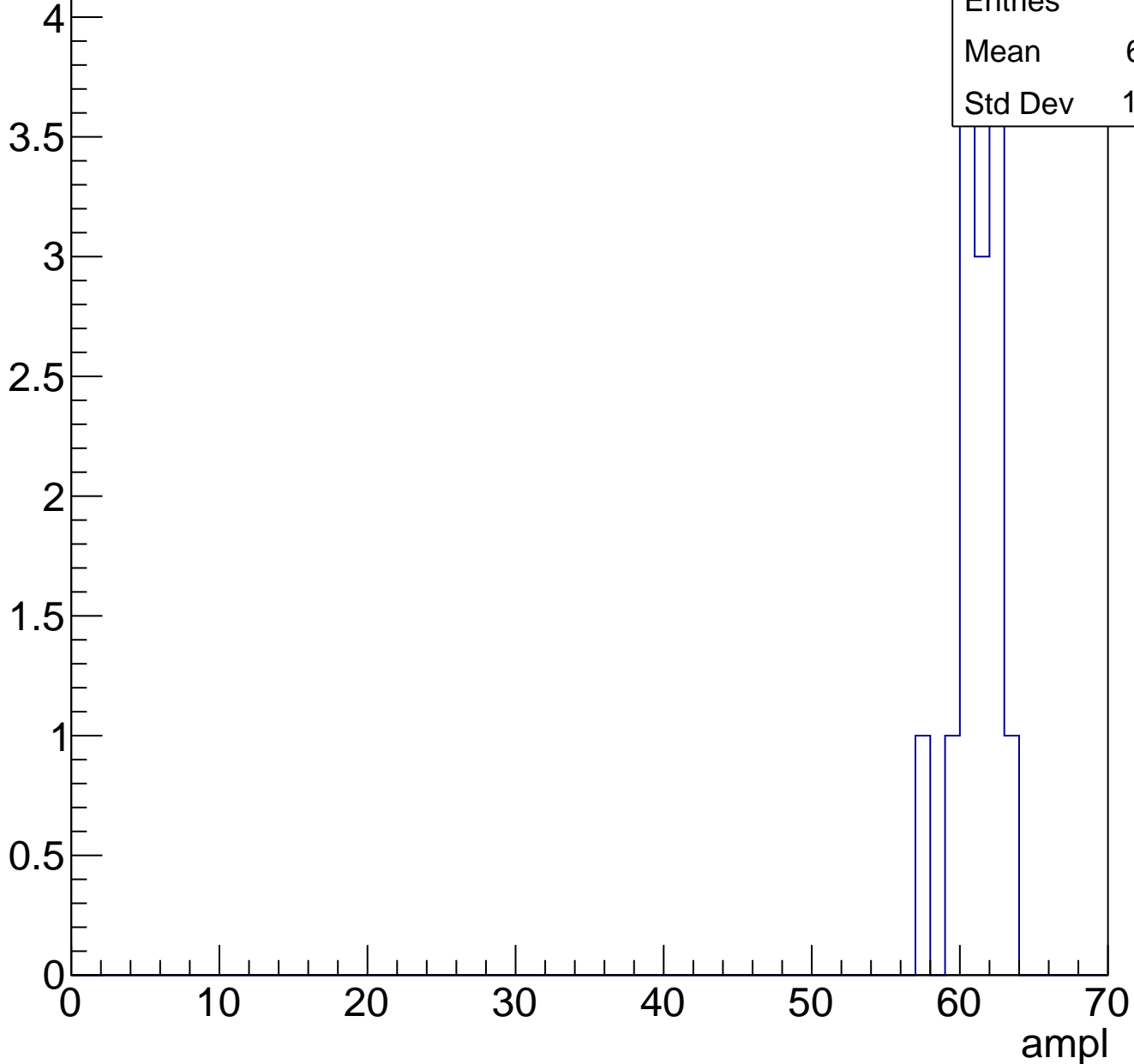
Entries	51
Mean	57.78
Std Dev	8.633



# B1L101S, U8-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



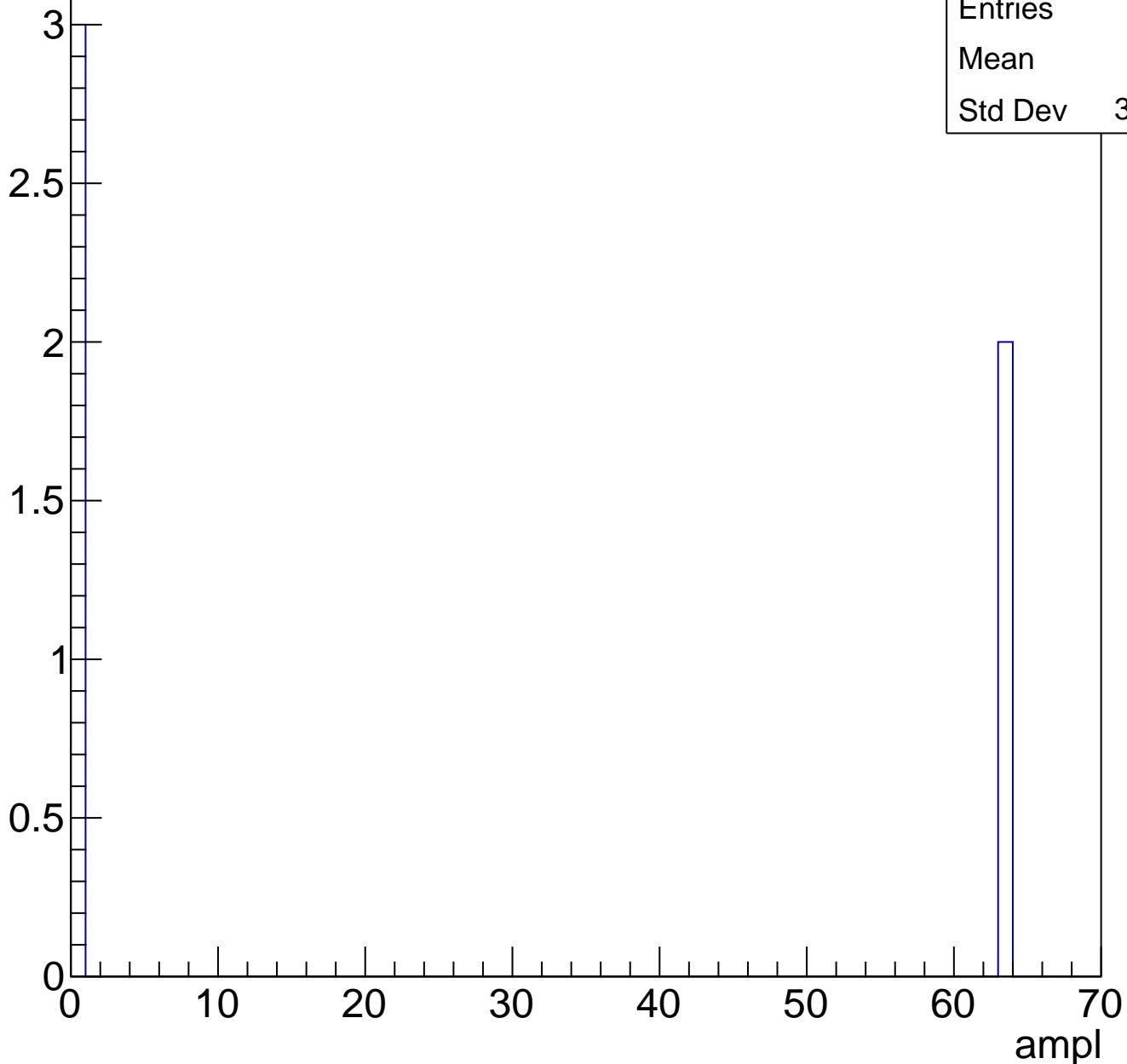
Entries	14
Mean	60.71
Std Dev	1.485



# B1L101S, U8-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch109, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	80
Mean	30.62
Std Dev	4.882

**Gaus mean : 31.2175**

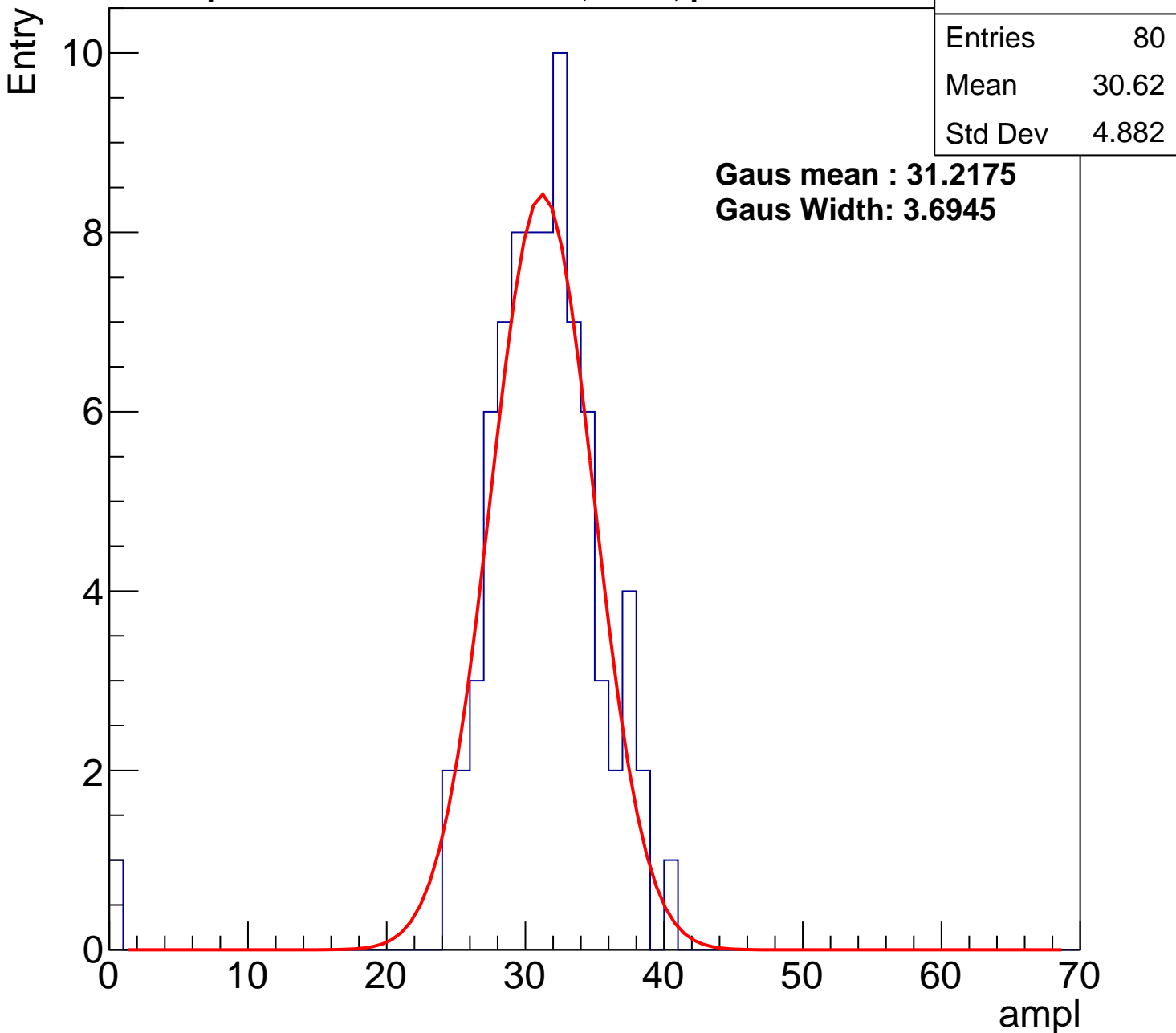
**Gaus Width: 3.6945**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U8-ch109, adc1

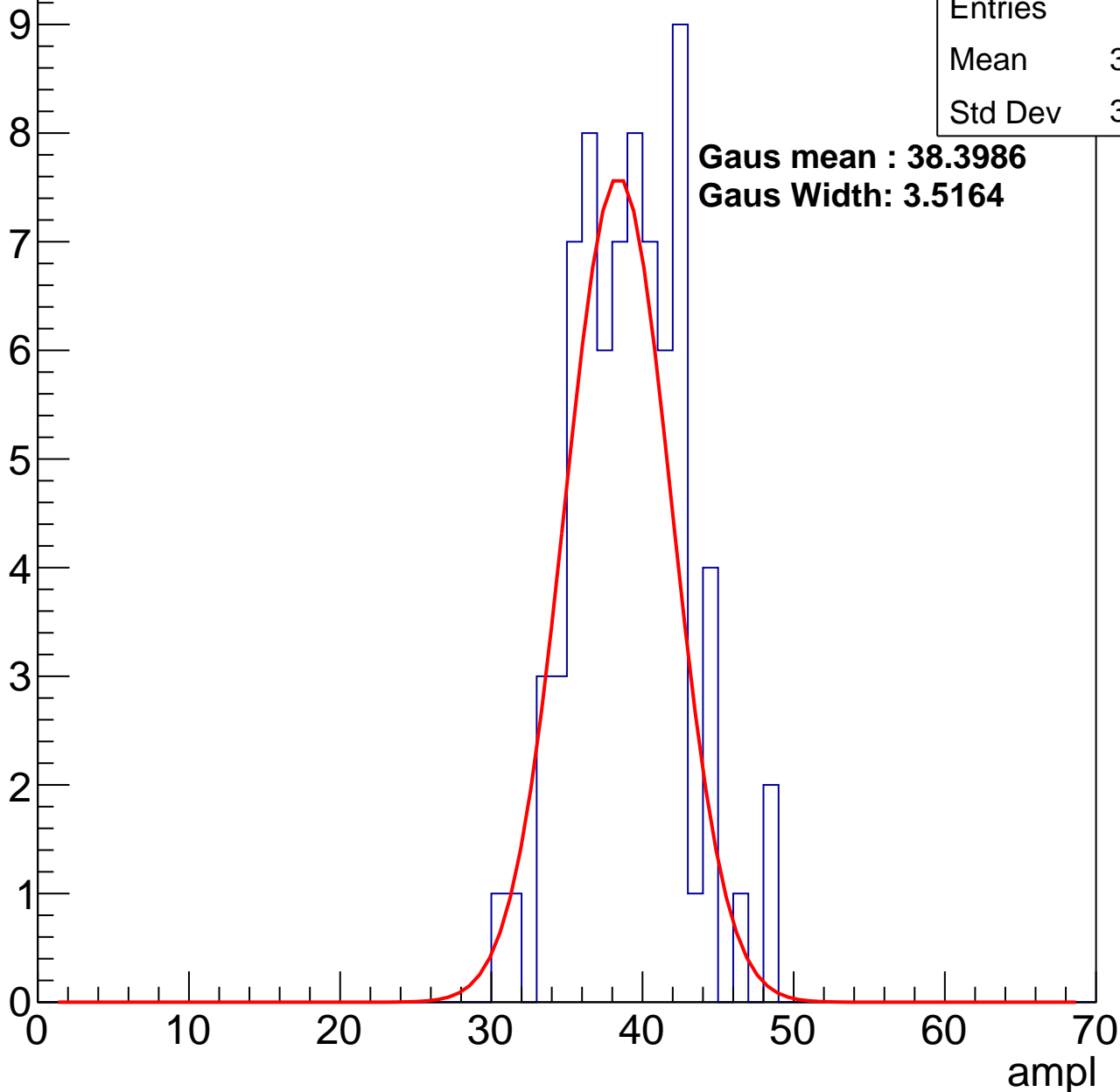
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	38.65
Std Dev	3.626

**Gaus mean : 38.3986**

**Gaus Width: 3.5164**



# B1L101S, U8-ch109, adc2

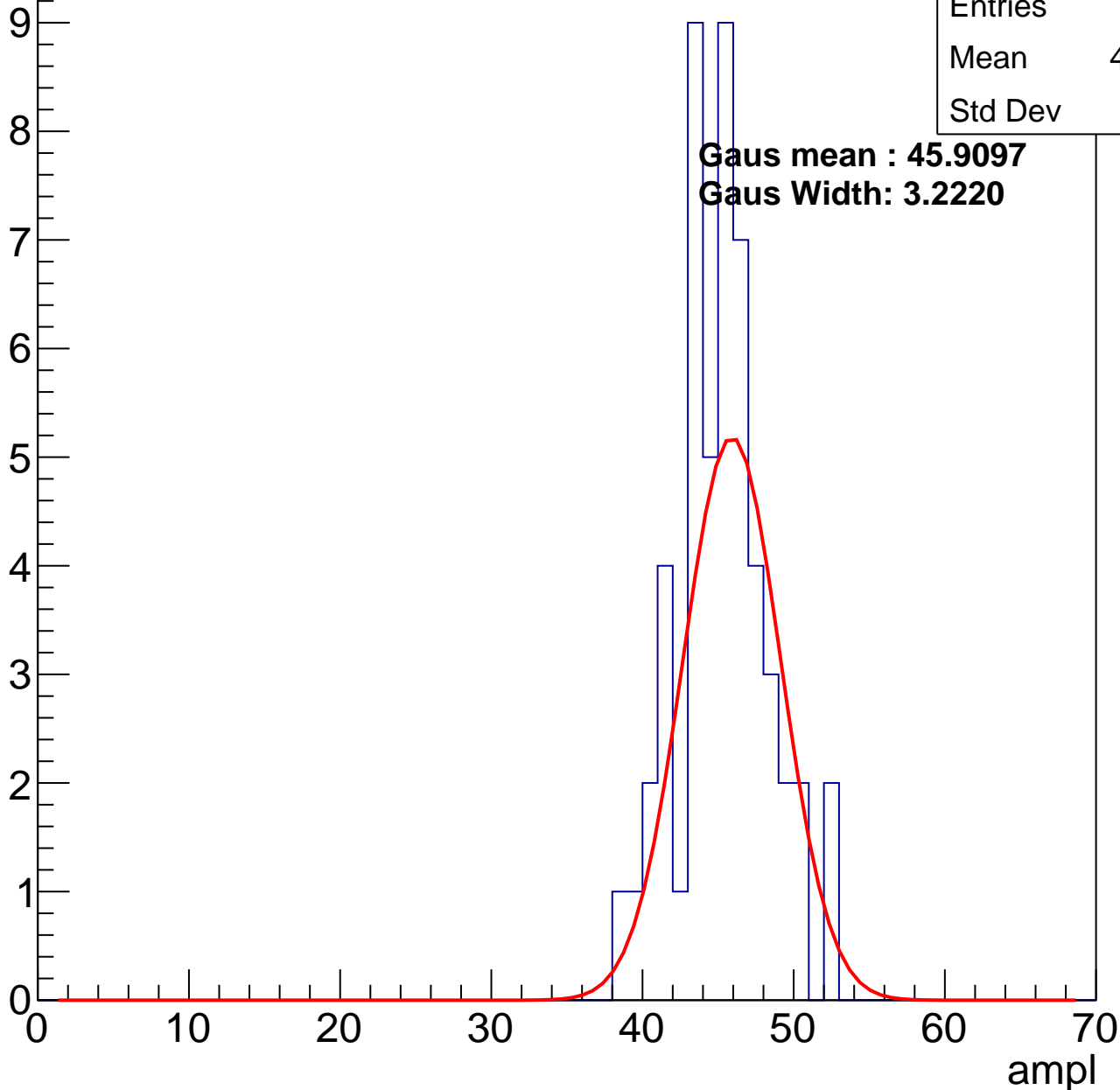
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	44.83
Std Dev	3.03

**Gaus mean : 45.9097**

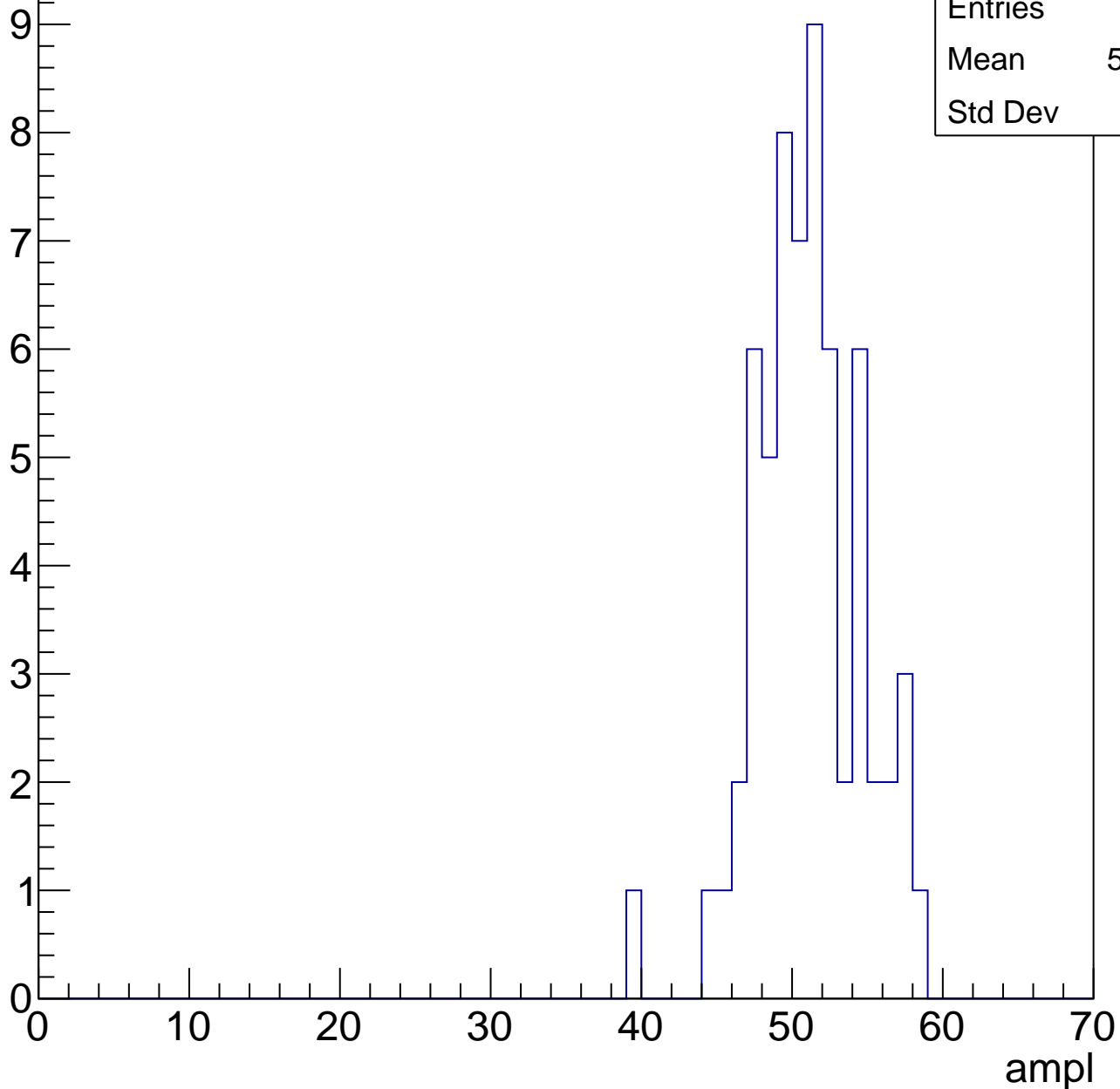
**Gaus Width: 3.2220**



# B1L101S, U8-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

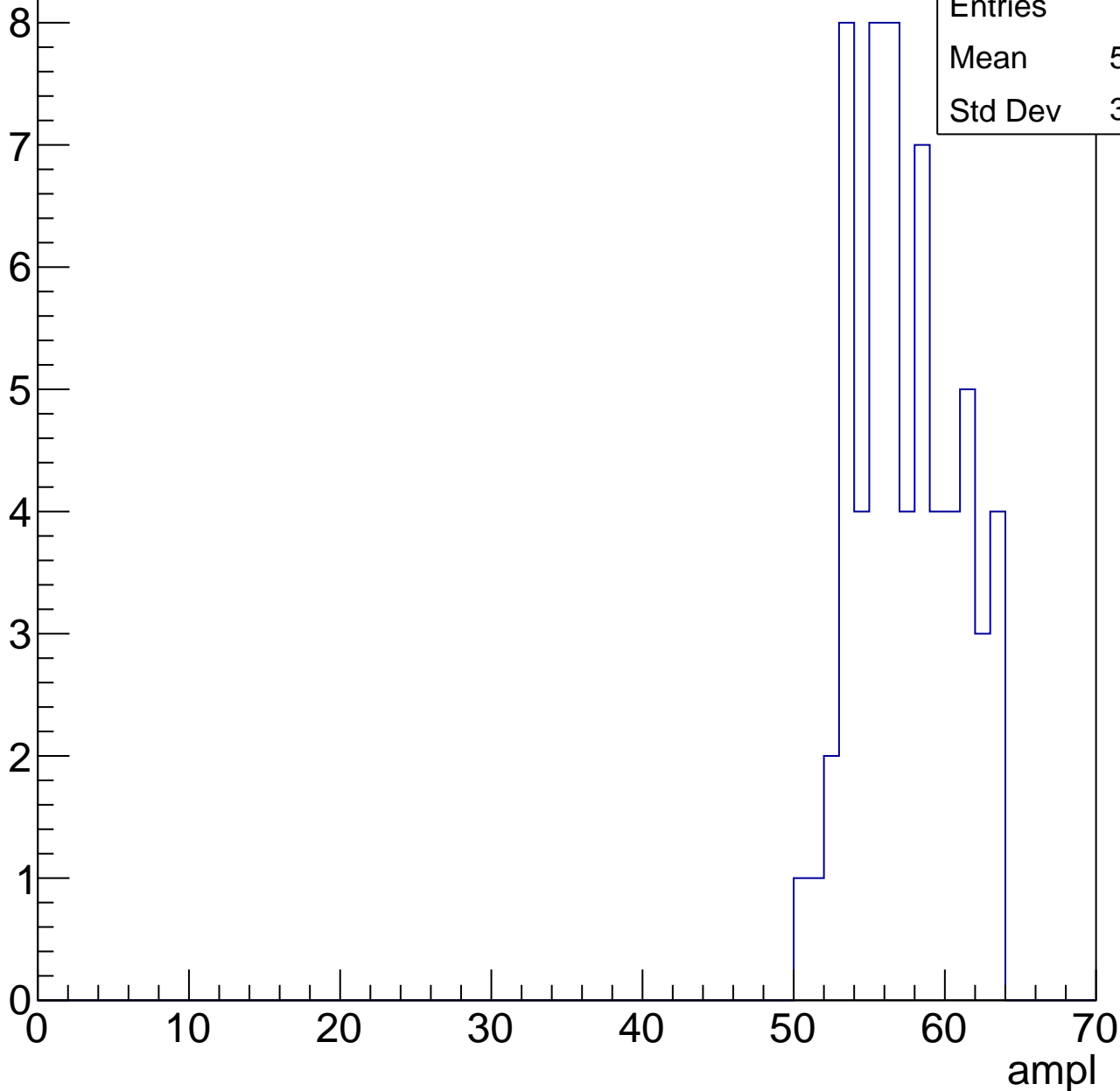


# B1L101S, U8-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

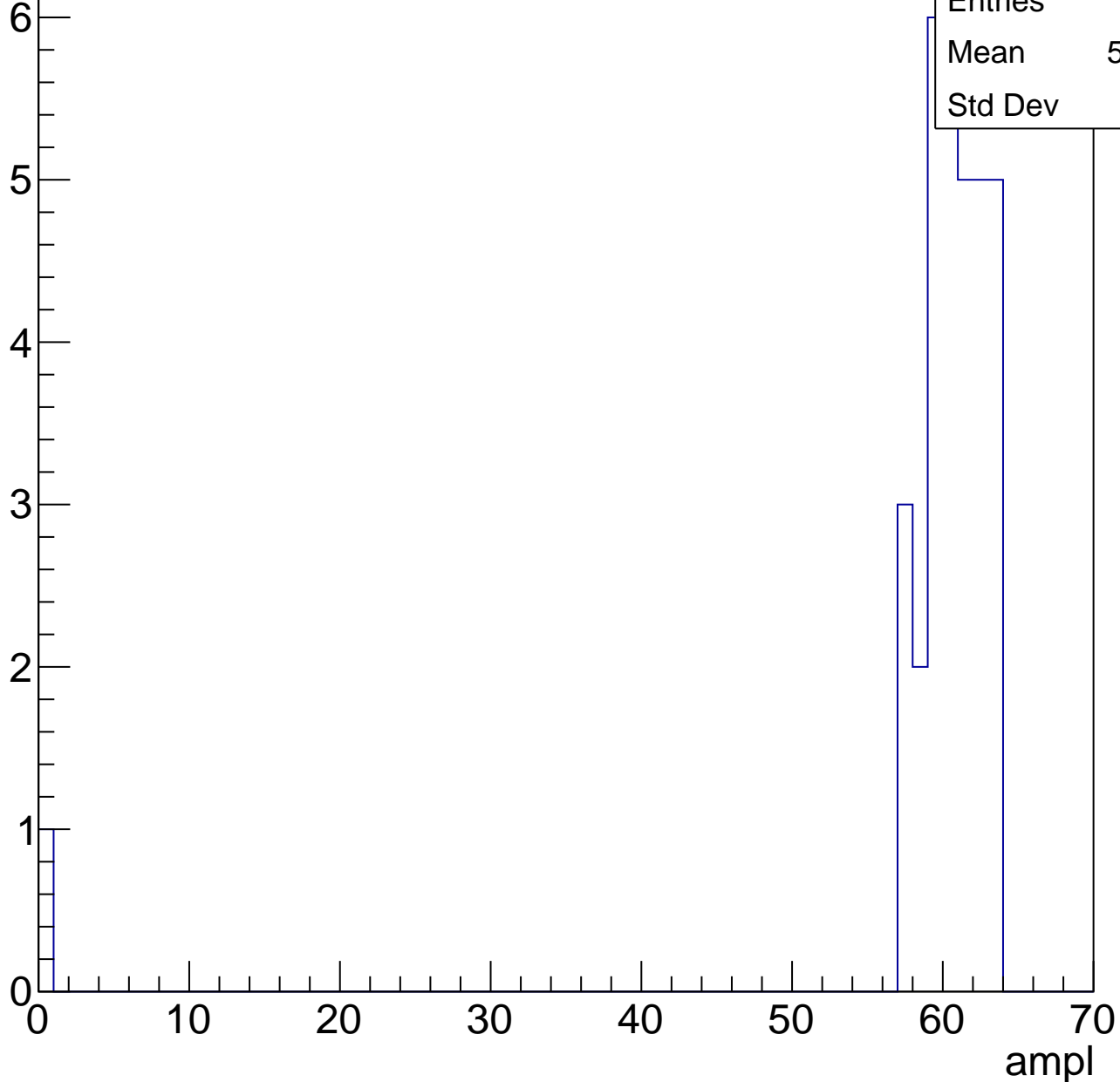
Entries	63
Mean	56.92
Std Dev	3.325



# B1L101S, U8-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.4714

ampl





# B1L101S, U8-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U8-ch110, adc0

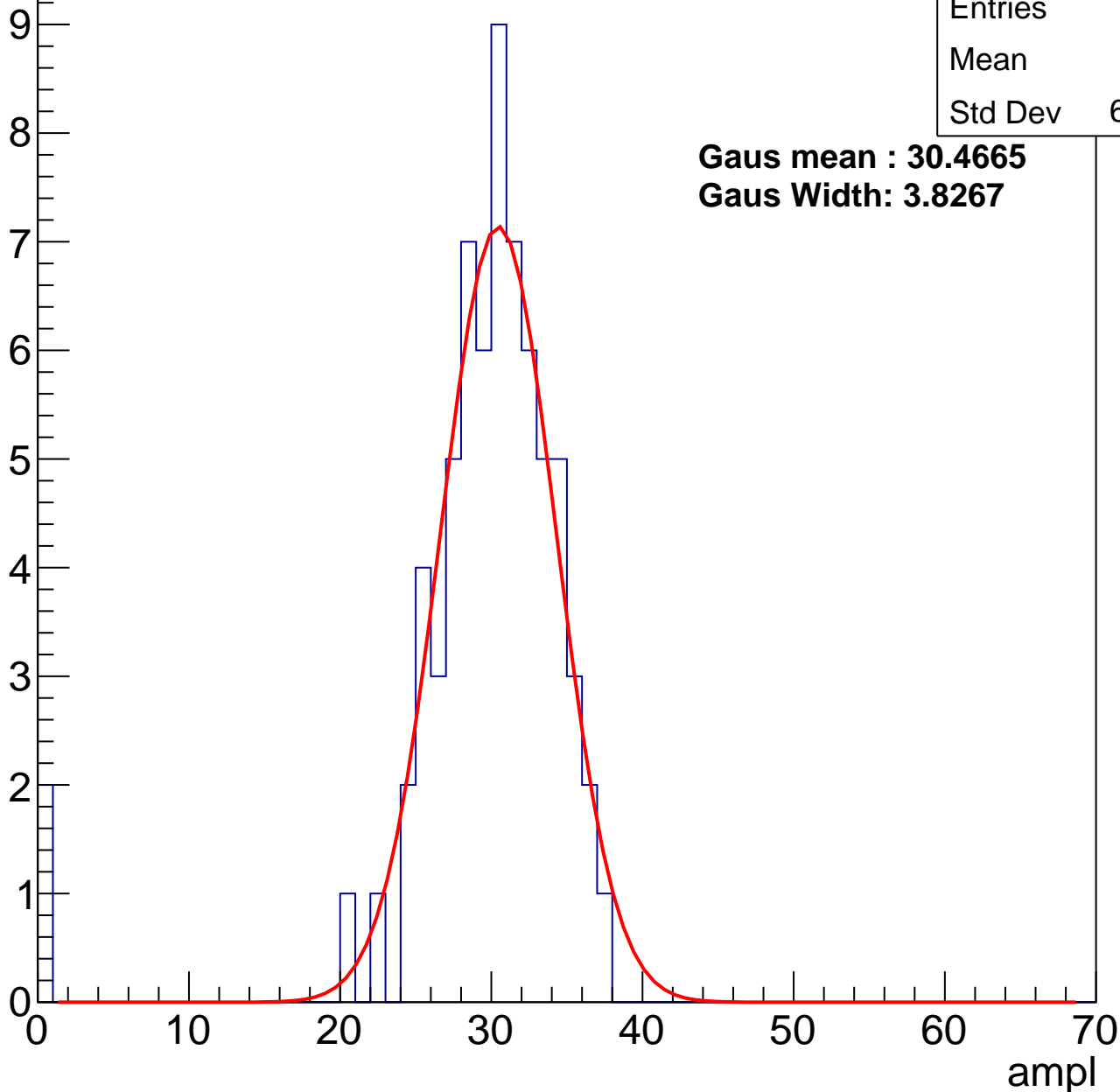
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	29
Std Dev	6.074

**Gaus mean : 30.4665**

**Gaus Width: 3.8267**



# B1L101S, U8-ch110, adc1

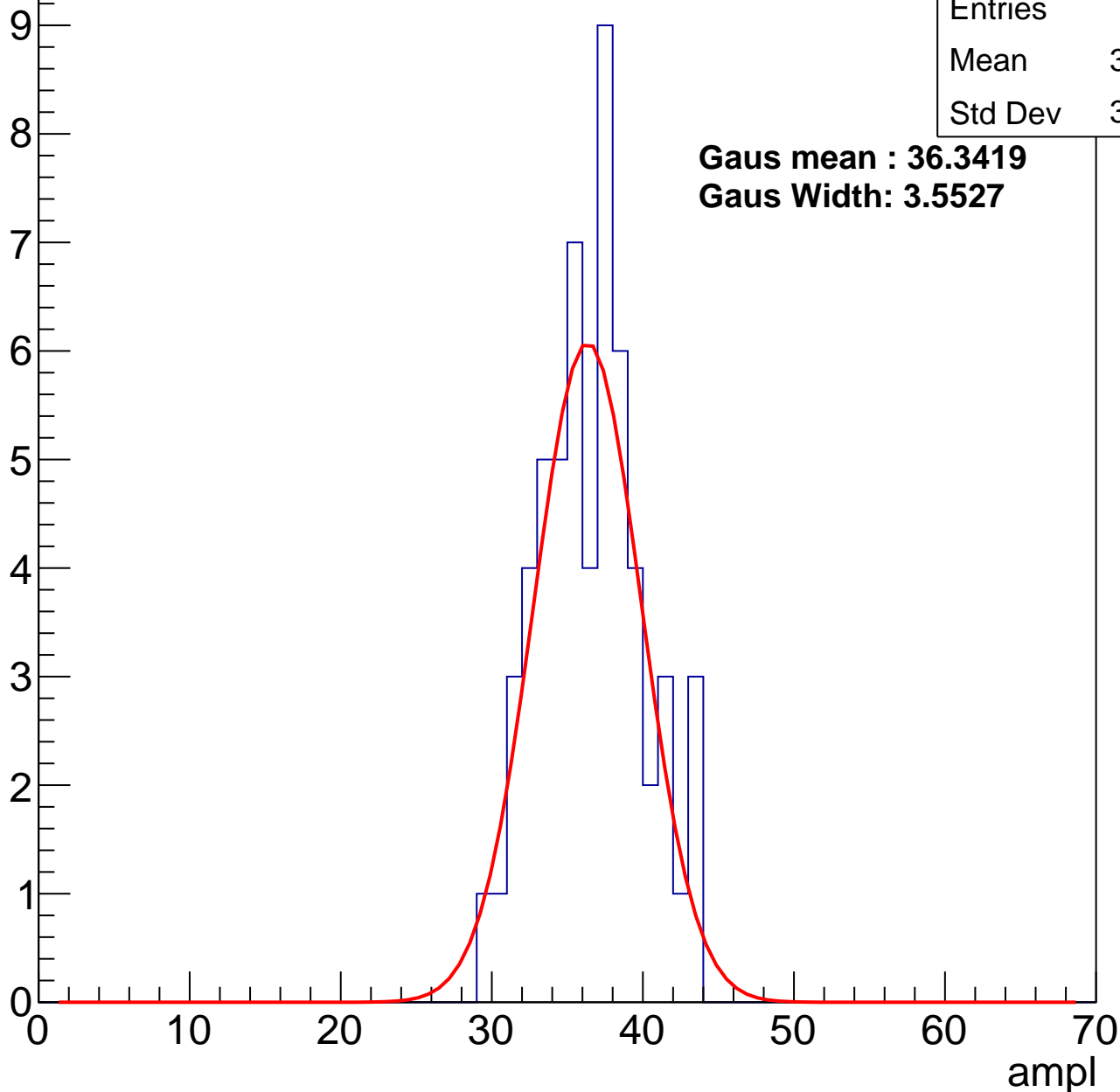
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	36.12
Std Dev	3.358

**Gaus mean : 36.3419**

**Gaus Width: 3.5527**



# B1L101S, U8-ch110, adc2

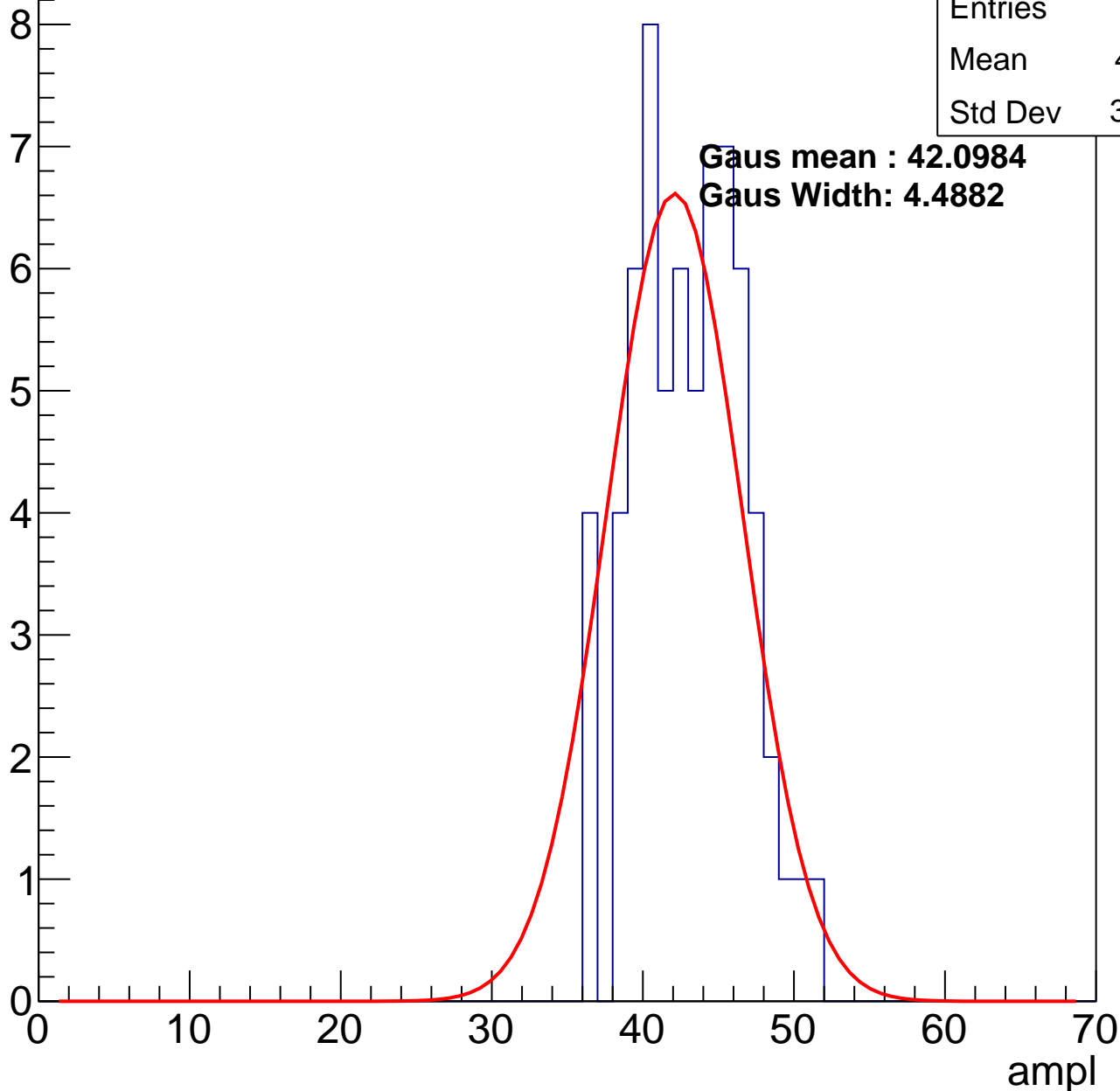
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	42.61
Std Dev	3.524

**Gaus mean : 42.0984**

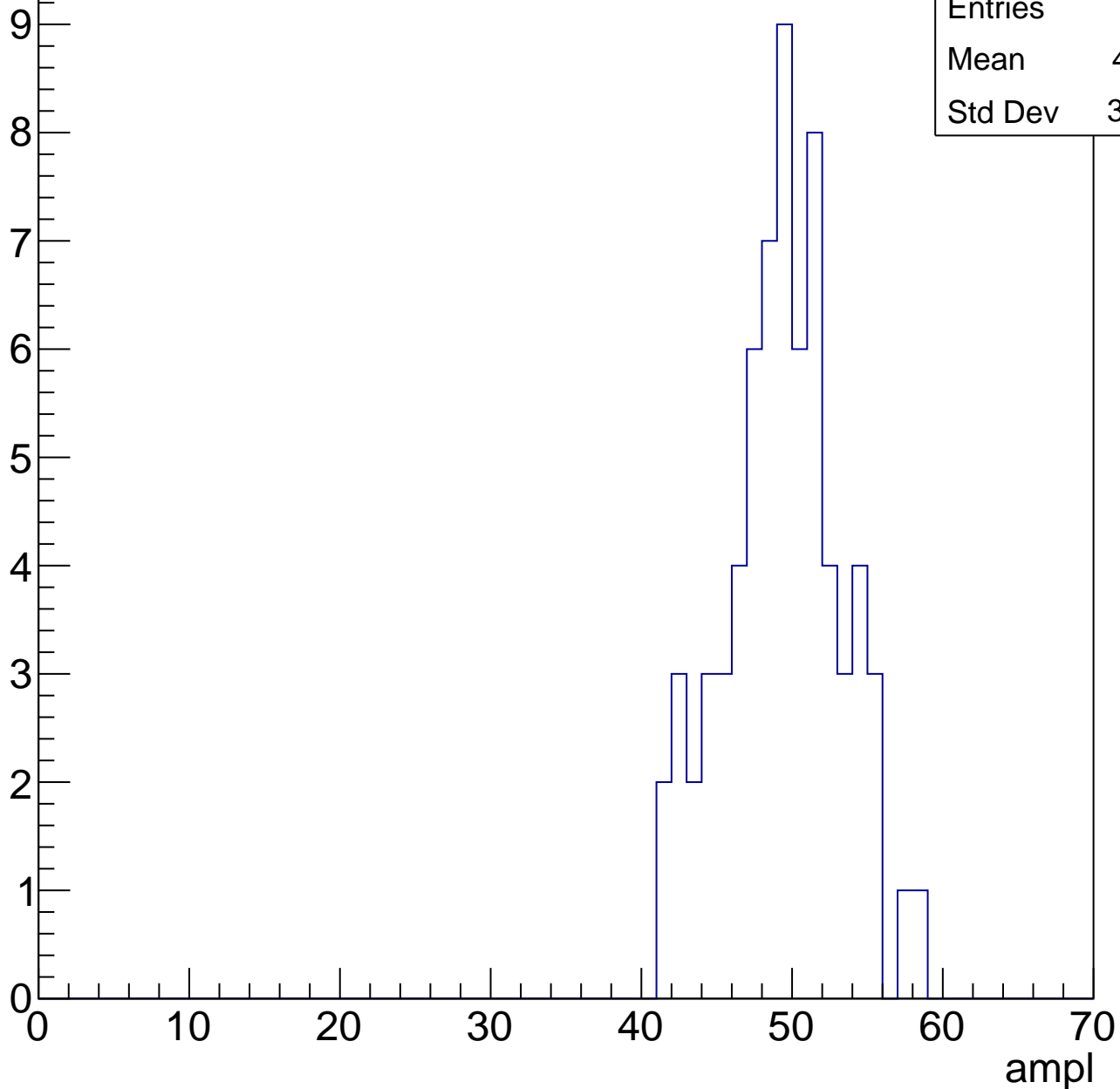
**Gaus Width: 4.4882**



# B1L101S, U8-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

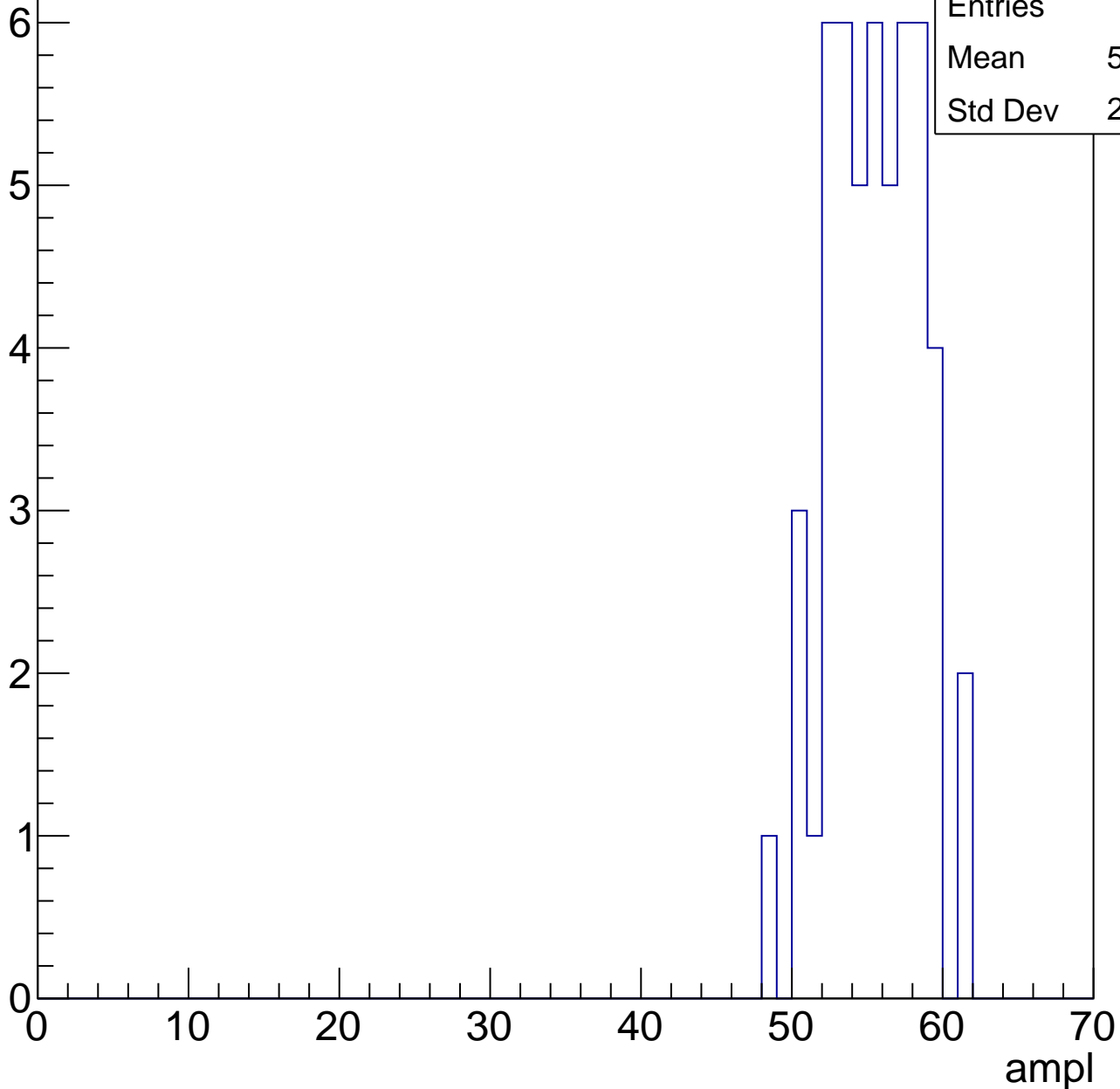


# B1L101S, U8-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

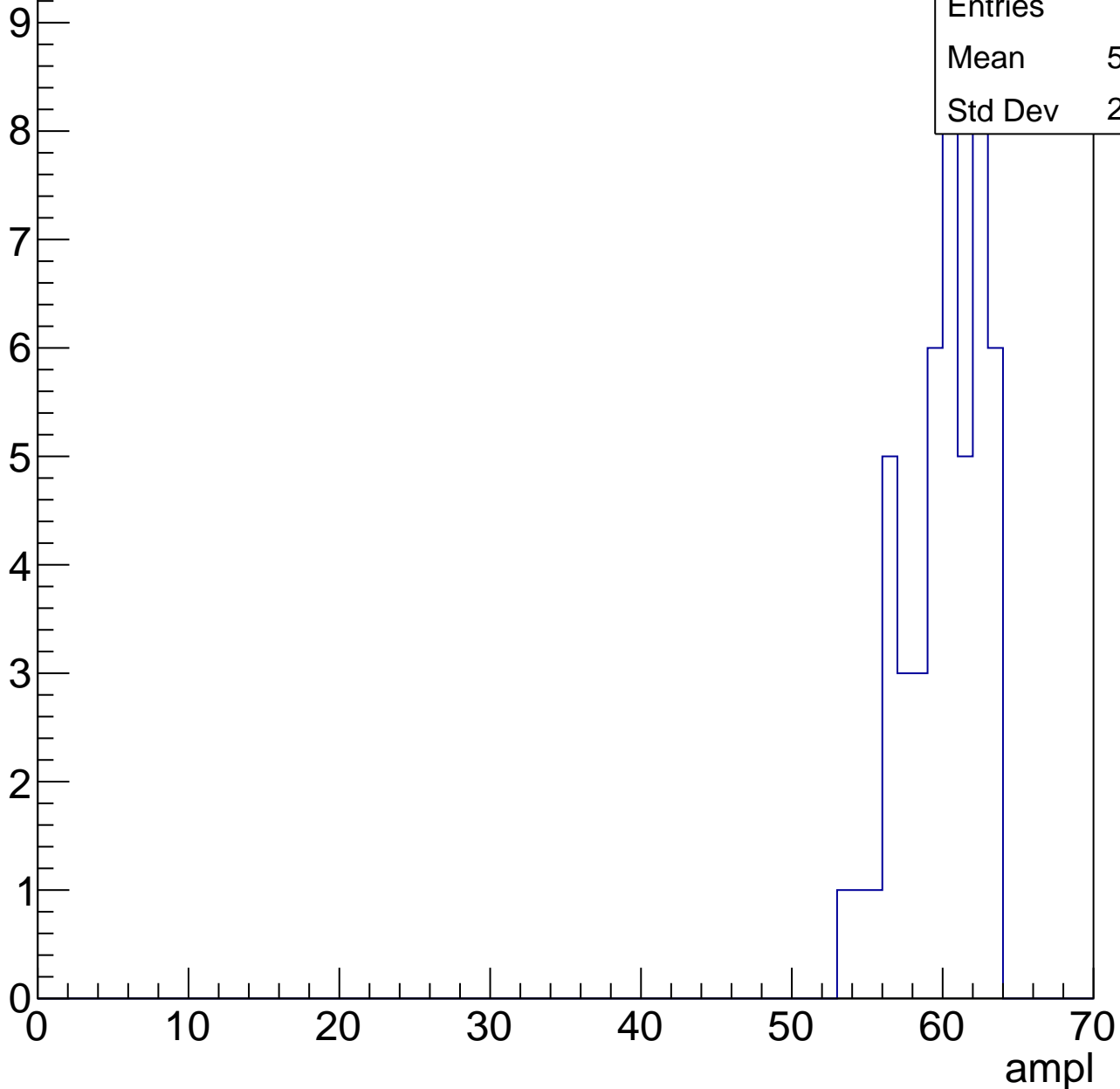
Entries	51
Mean	55.04
Std Dev	2.944



# B1L101S, U8-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

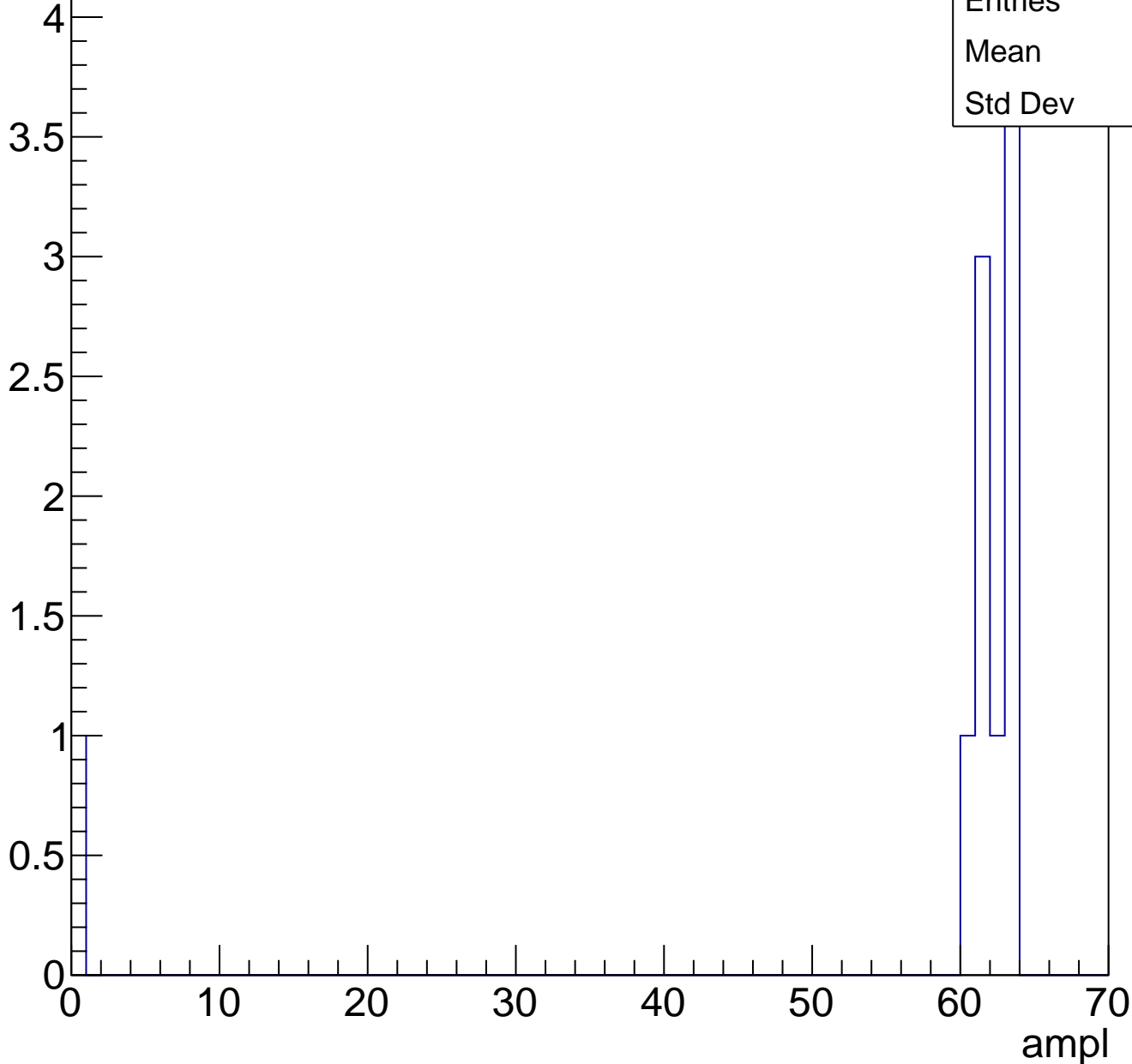


Entries	49
Mean	59.63
Std Dev	2.569

# B1L101S, U8-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch111, adc0

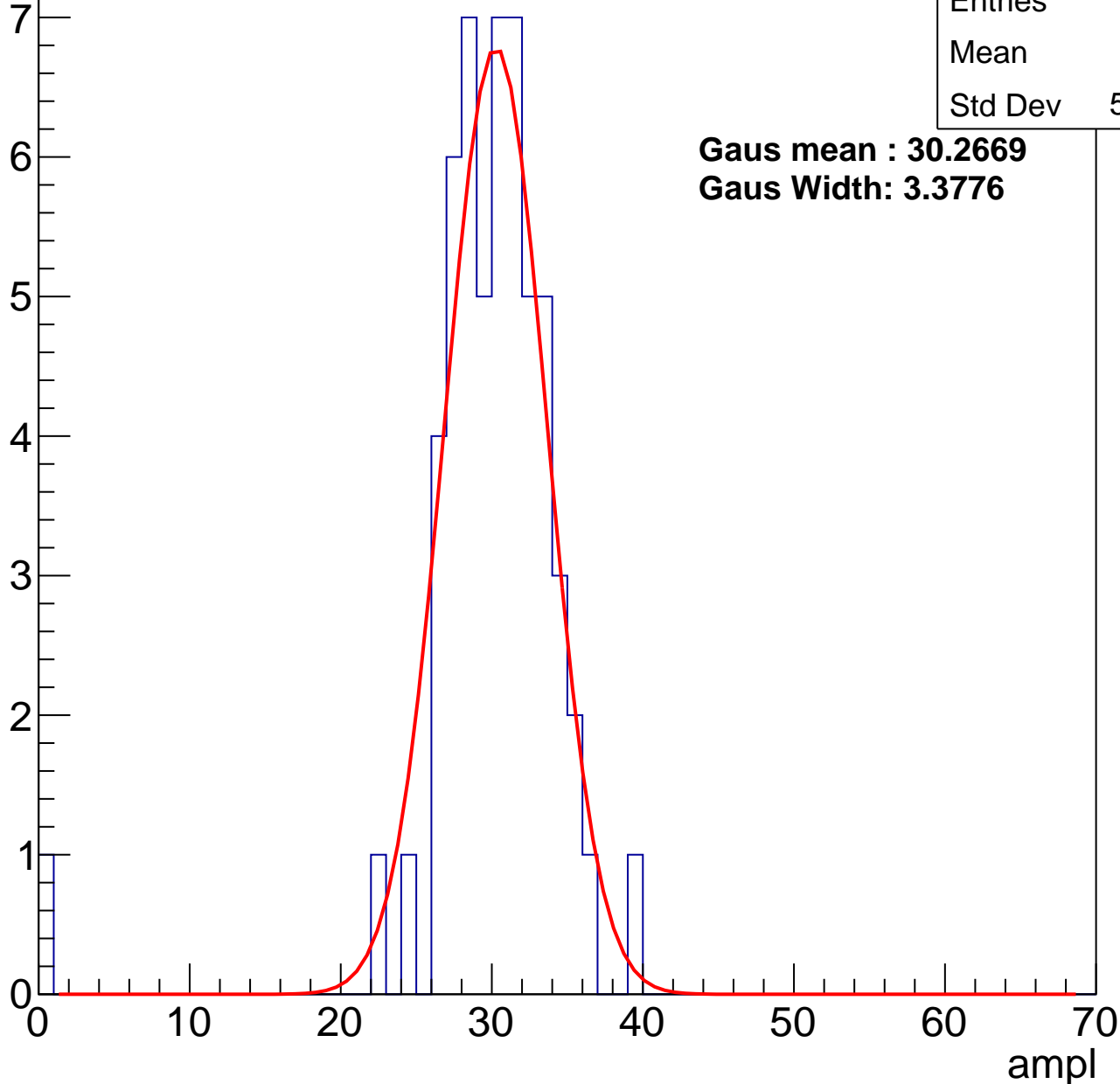
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	29.5
Std Dev	5.043

**Gaus mean : 30.2669**

**Gaus Width: 3.3776**



# B1L101S, U8-ch111, adc1

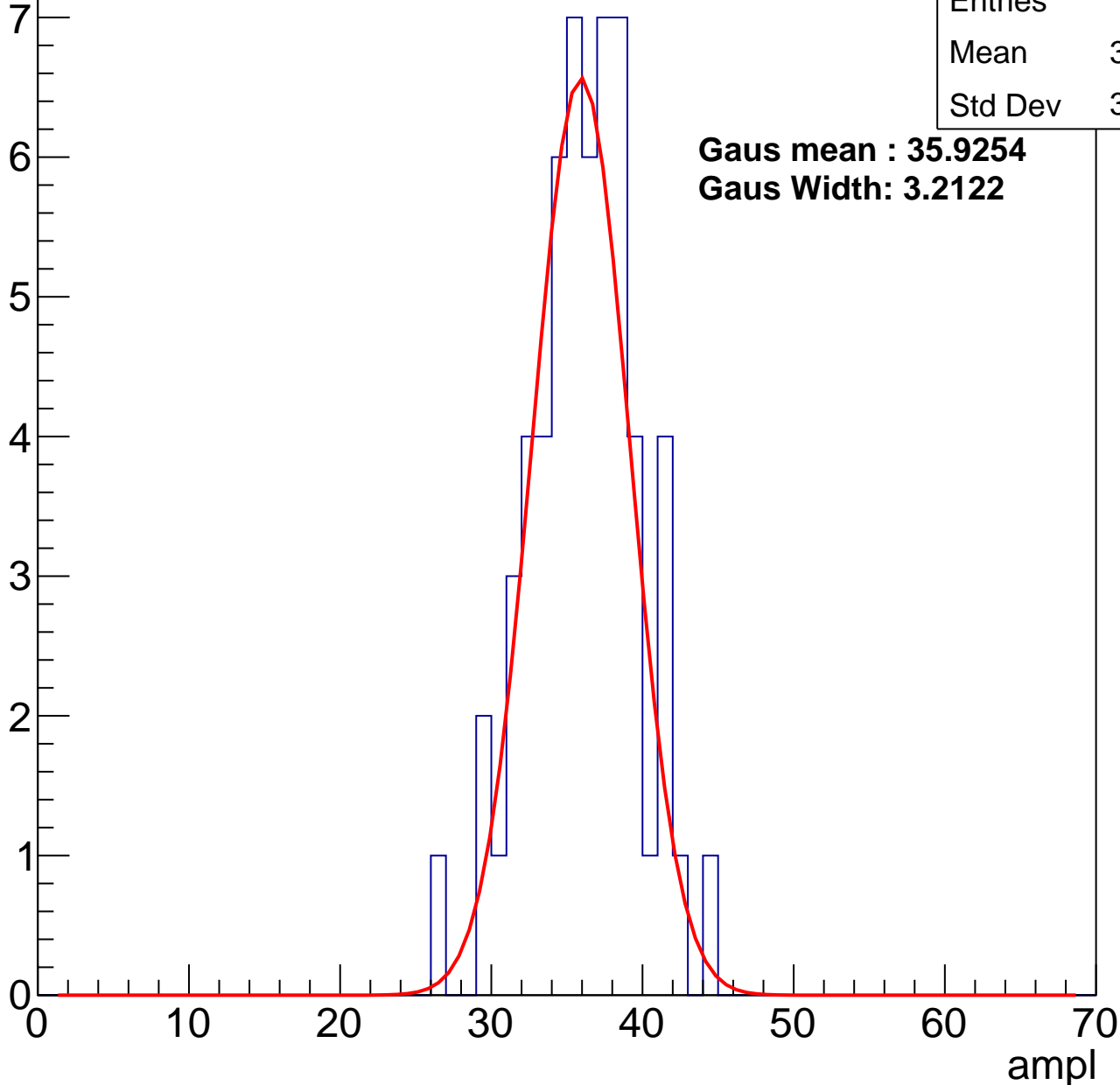
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	35.64
Std Dev	3.492

**Gaus mean : 35.9254**

**Gaus Width: 3.2122**



# B1L101S, U8-ch111, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	42.41
Std Dev	3.52

**Gaus mean : 43.4181**

**Gaus Width: 4.0247**

10

8

6

4

2

0

0

10

20

30

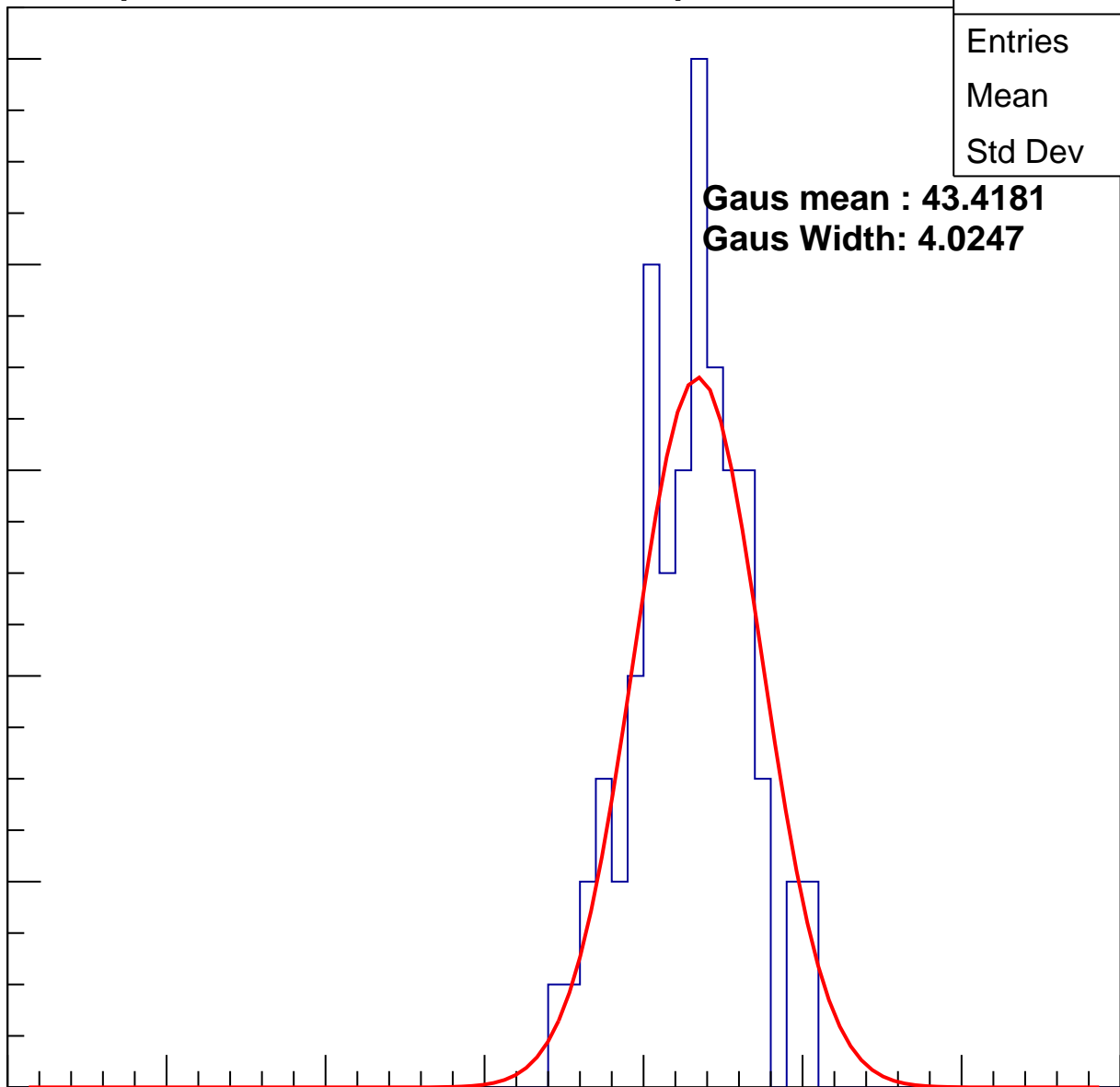
40

50

60

70

ampl

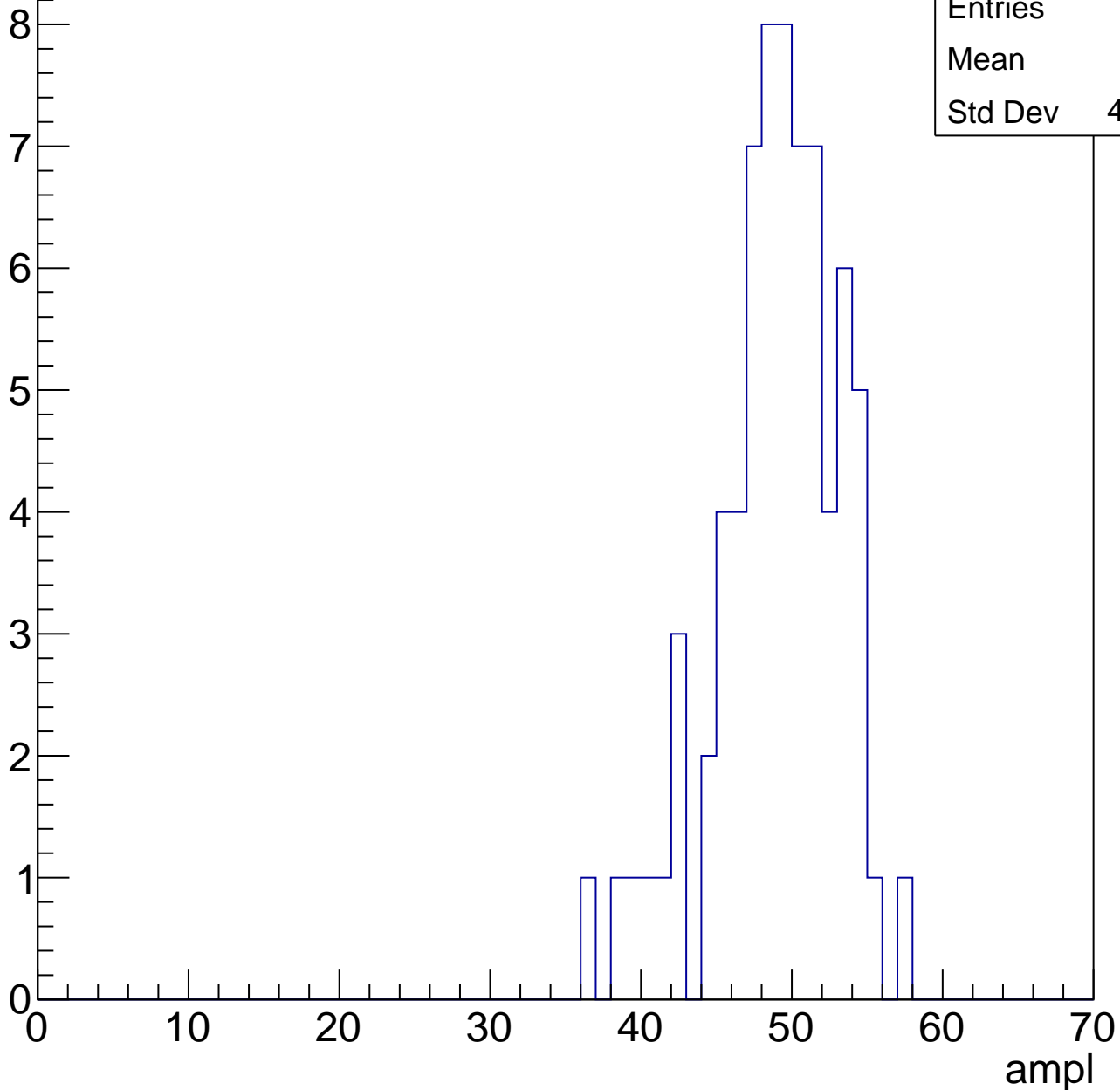


# B1L101S, U8-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	48.5
Std Dev	4.153

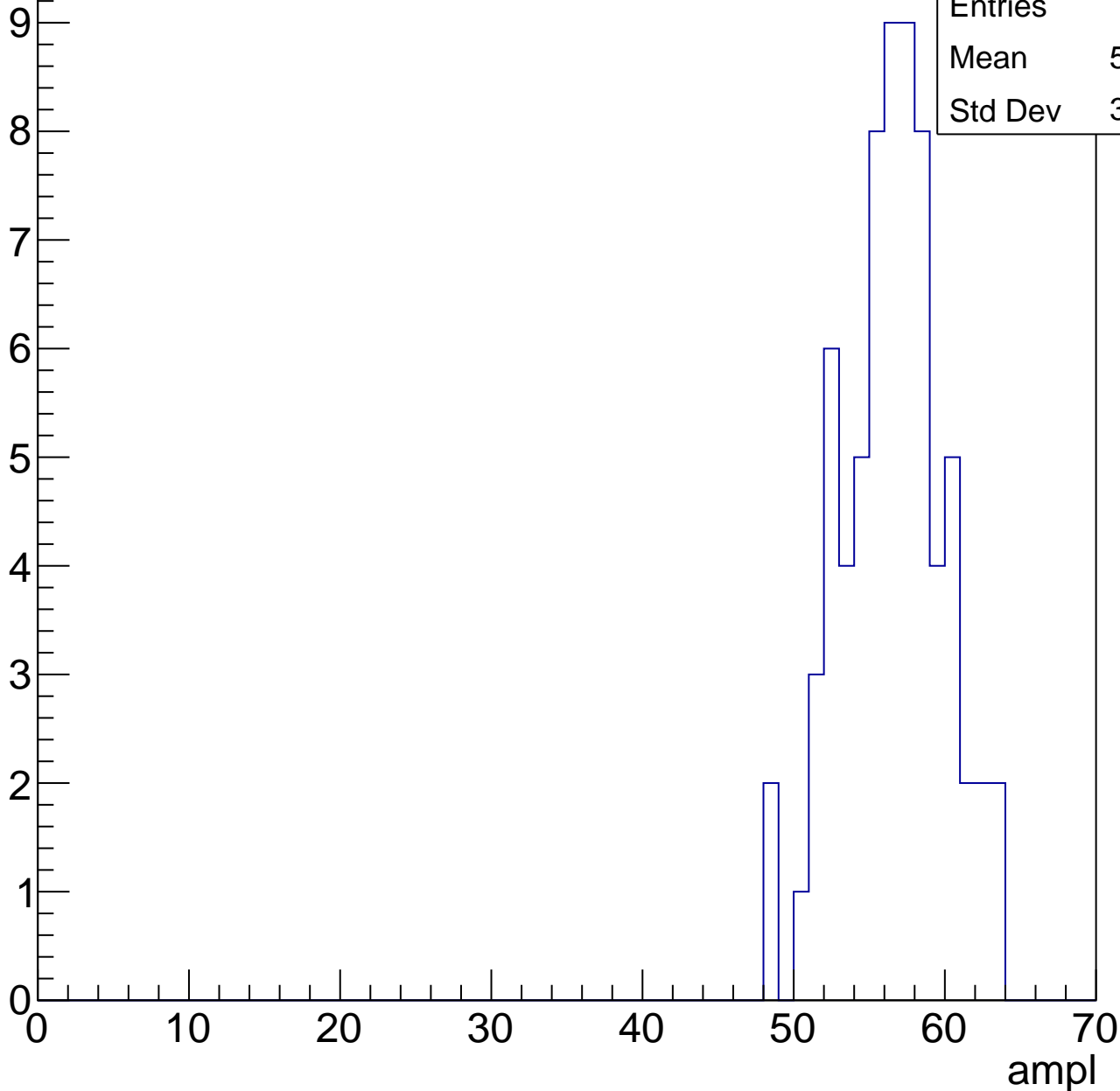


# B1L101S, U8-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	56.03
Std Dev	3.329

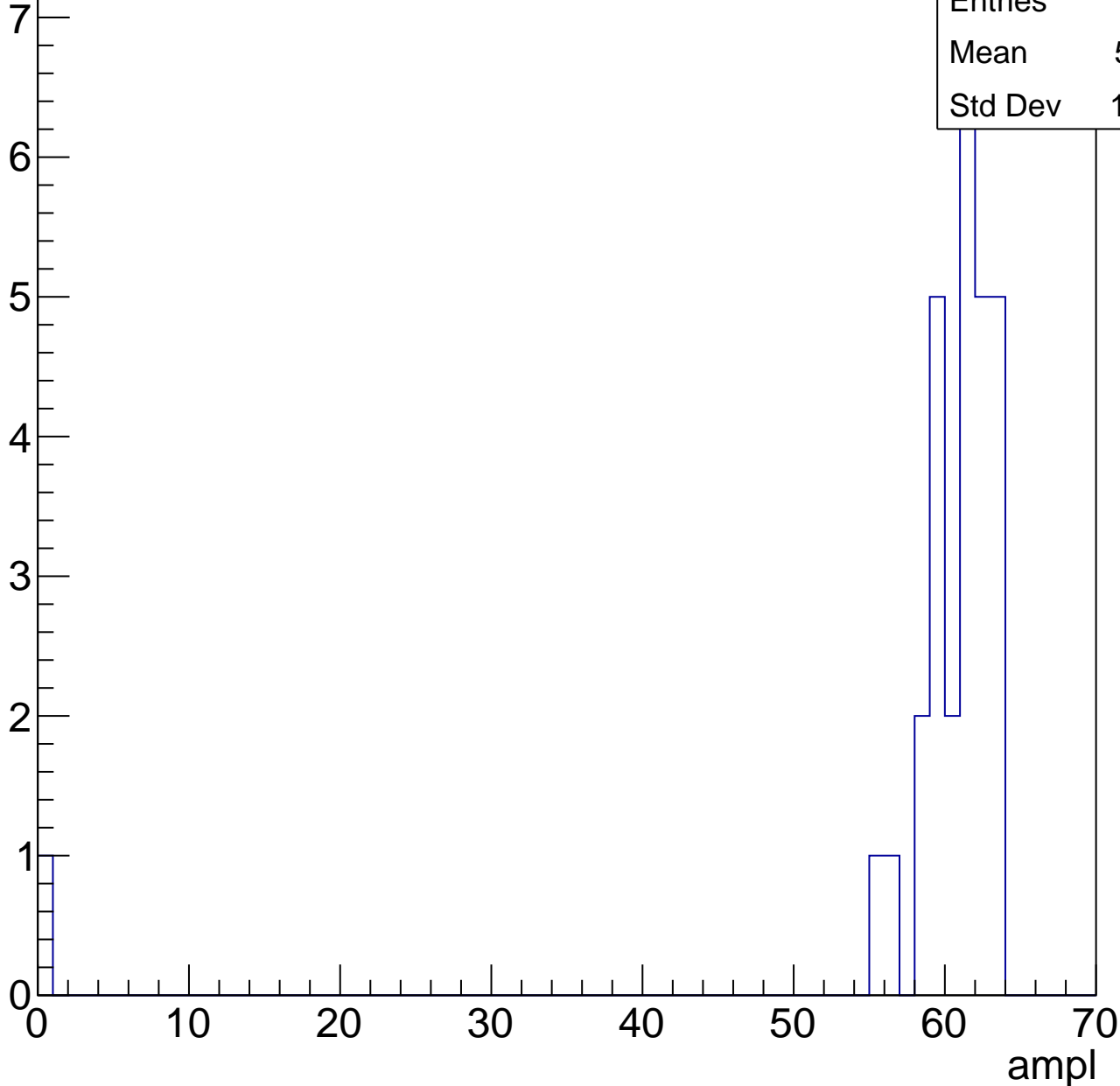


# B1L101S, U8-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

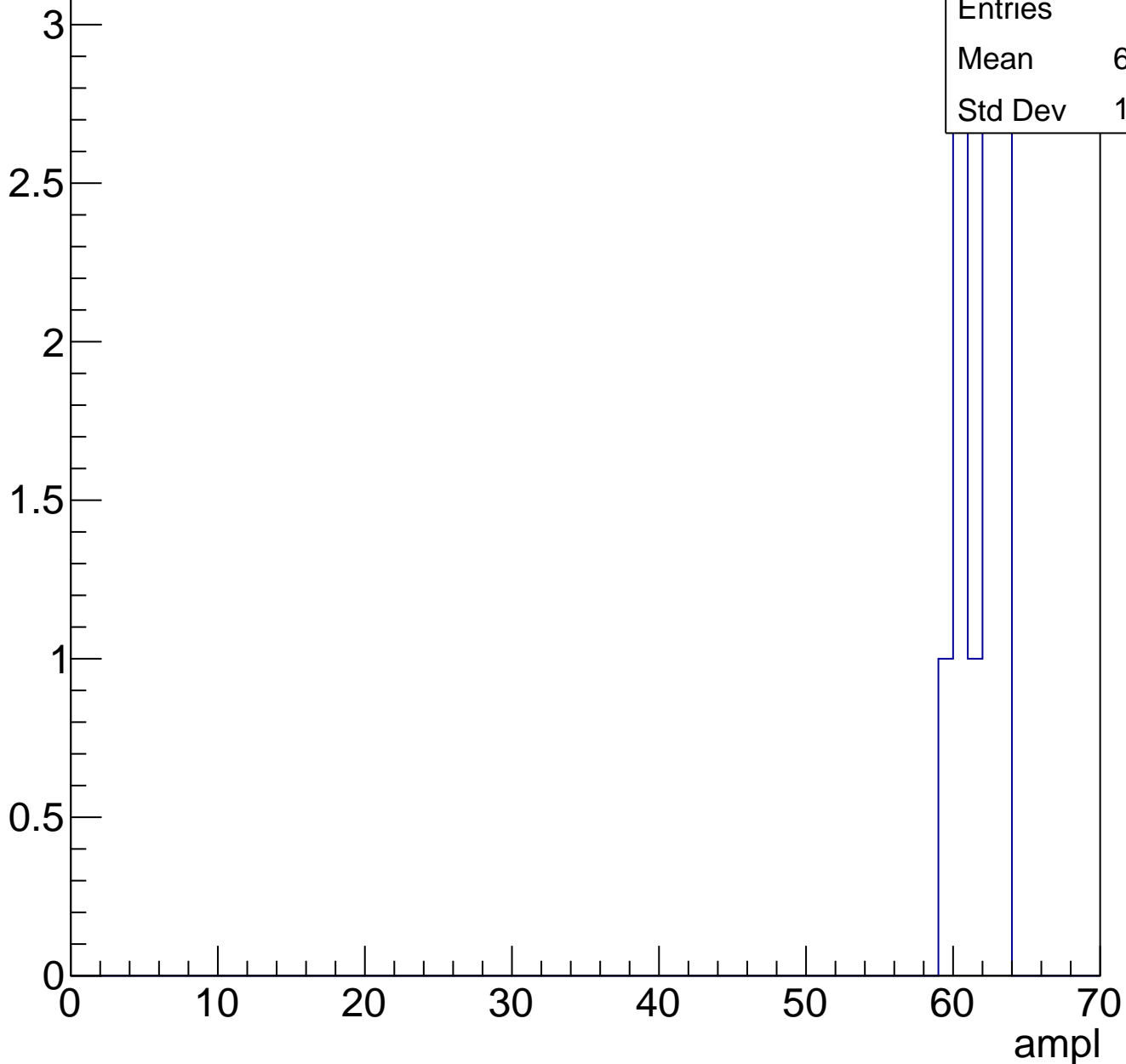
Entries	29
Mean	58.41
Std Dev	11.22



# B1L101S, U8-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U8-ch112, adc0

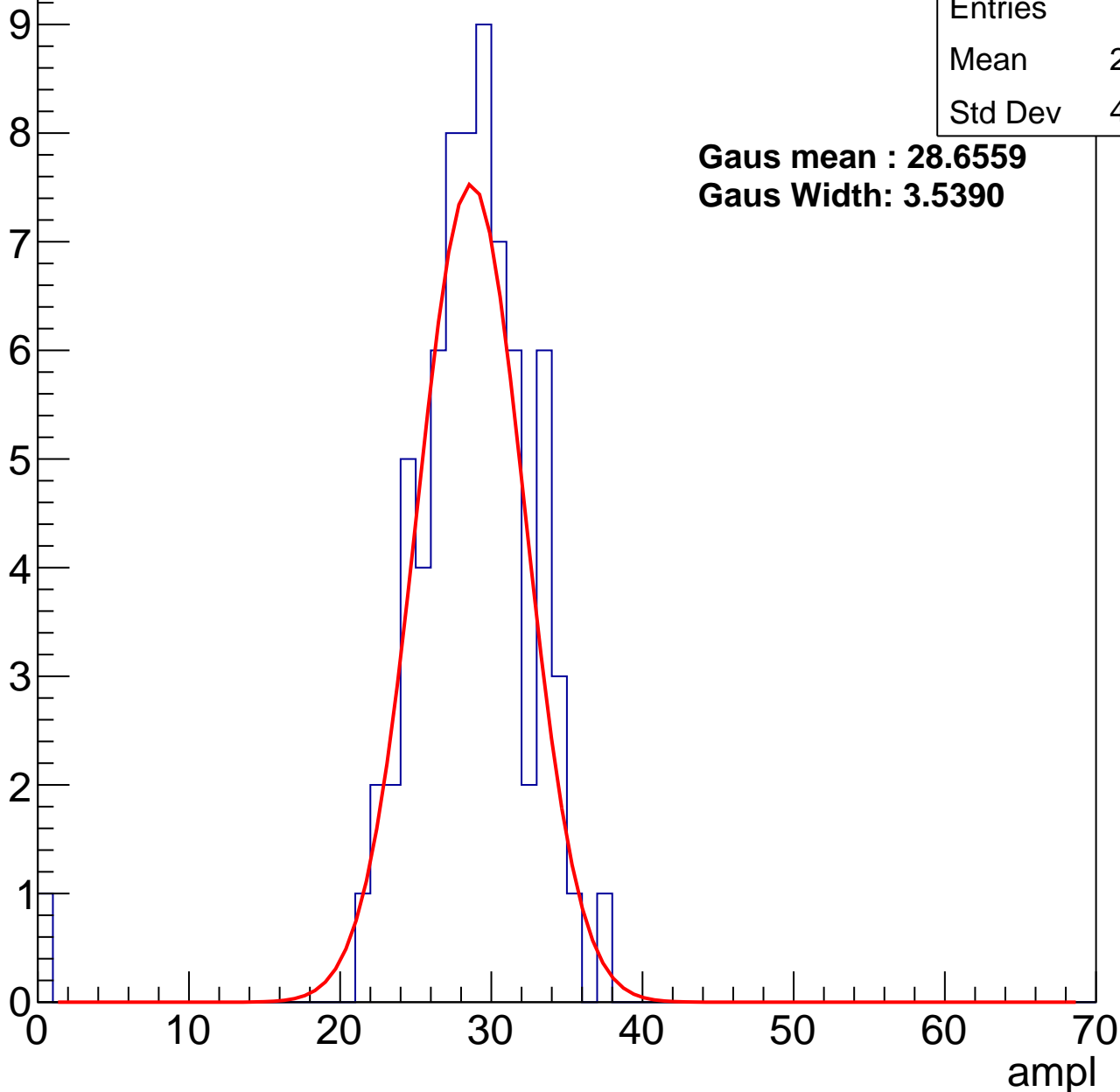
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	28.06
Std Dev	4.734

**Gaus mean : 28.6559**

**Gaus Width: 3.5390**



# B1L101S, U8-ch112, adc1

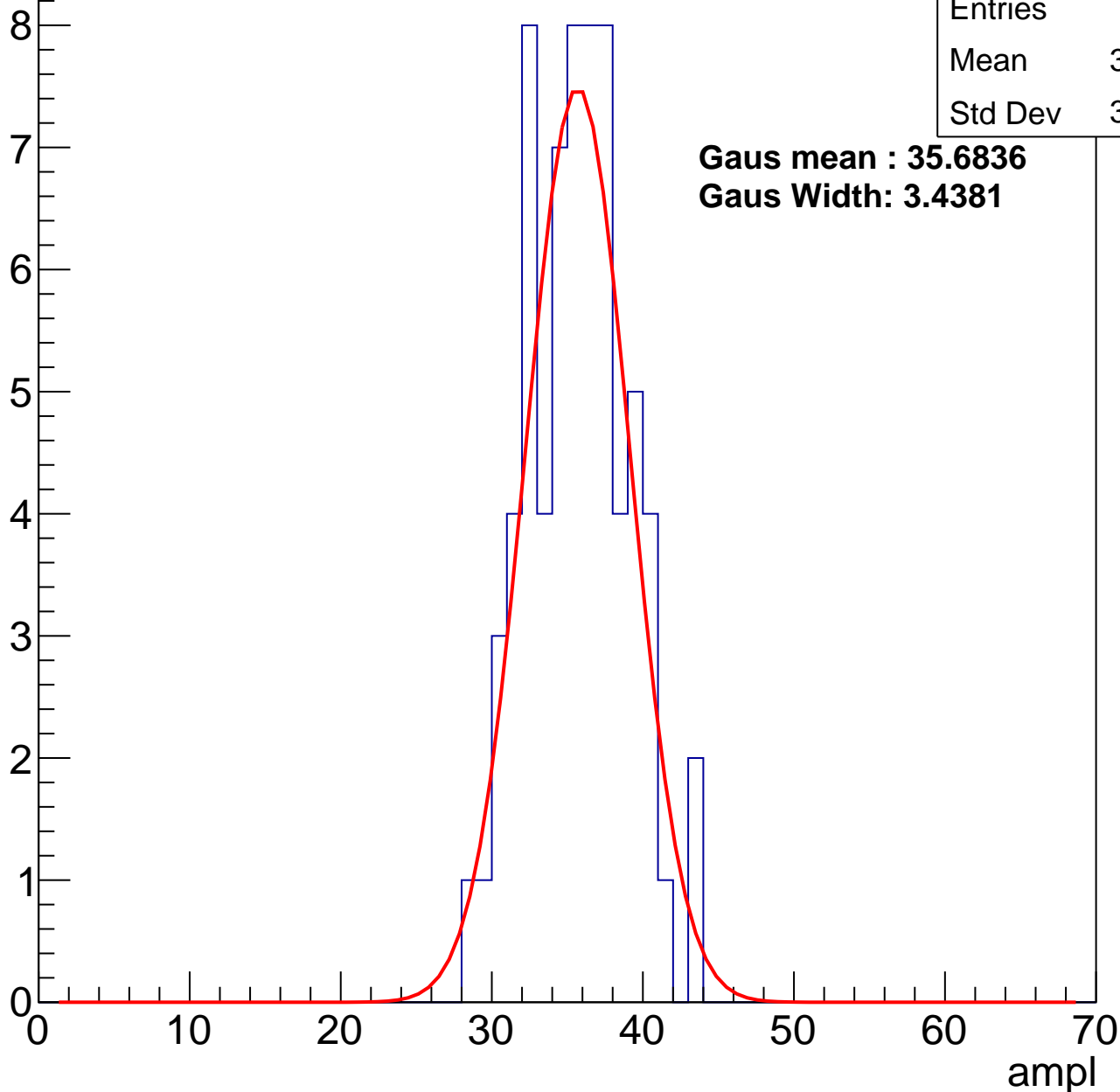
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	35.22
Std Dev	3.289

**Gaus mean : 35.6836**

**Gaus Width: 3.4381**



# B1L101S, U8-ch112, adc2

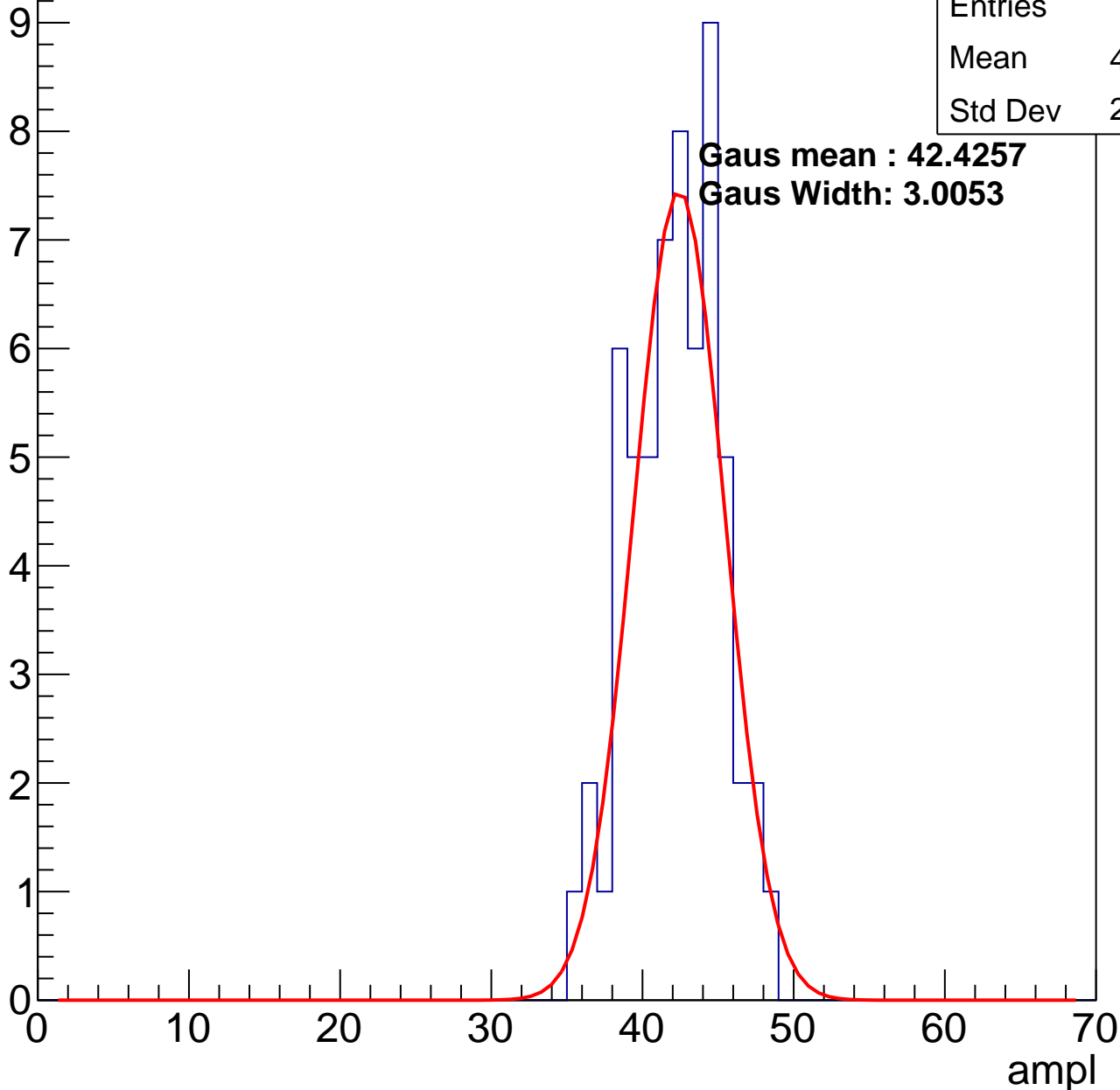
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	41.72
Std Dev	2.927

**Gaus mean : 42.4257**

**Gaus Width: 3.0053**



# B1L101S, U8-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

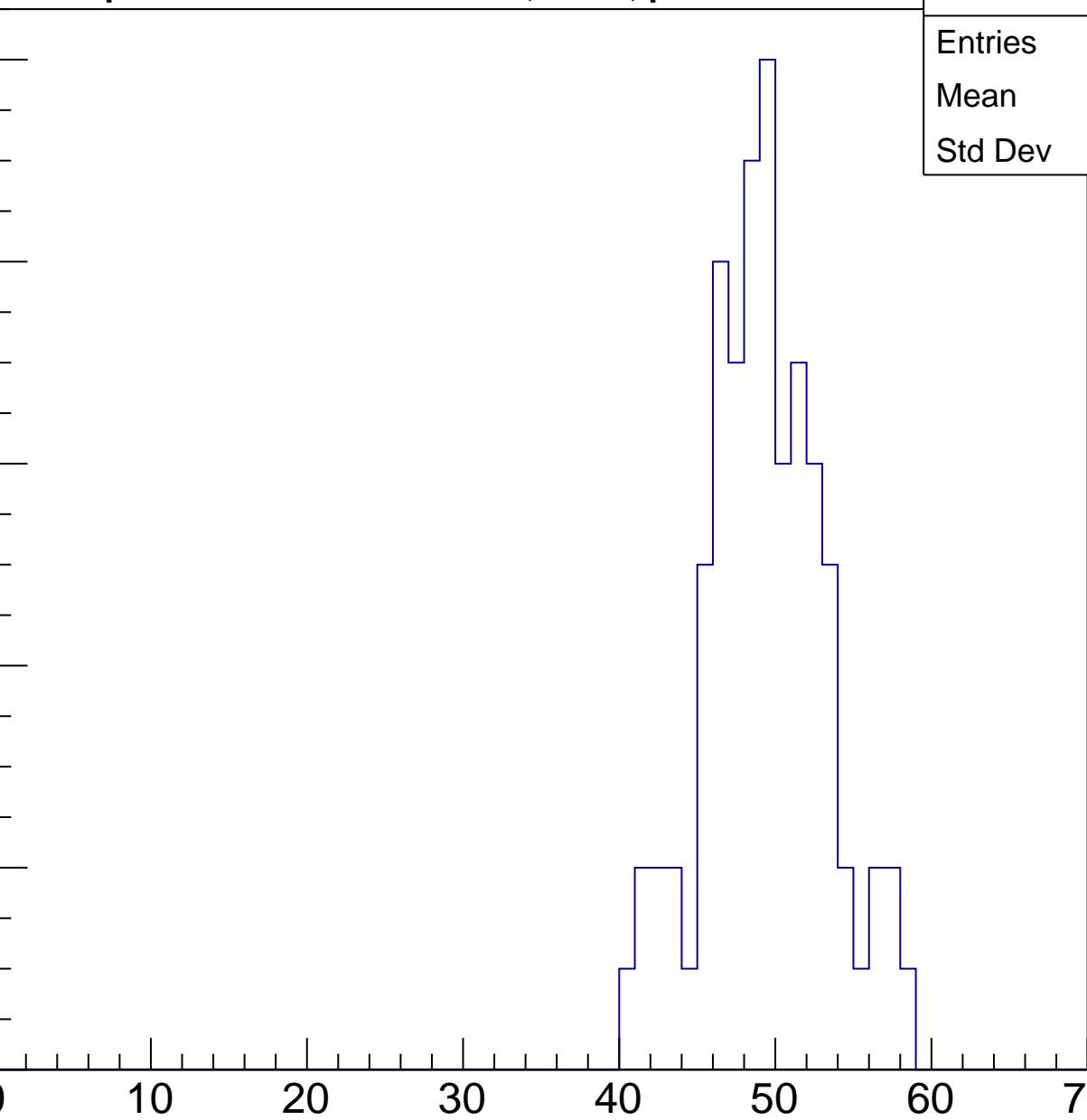
Entries	79
Mean	48.87
Std Dev	3.82

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

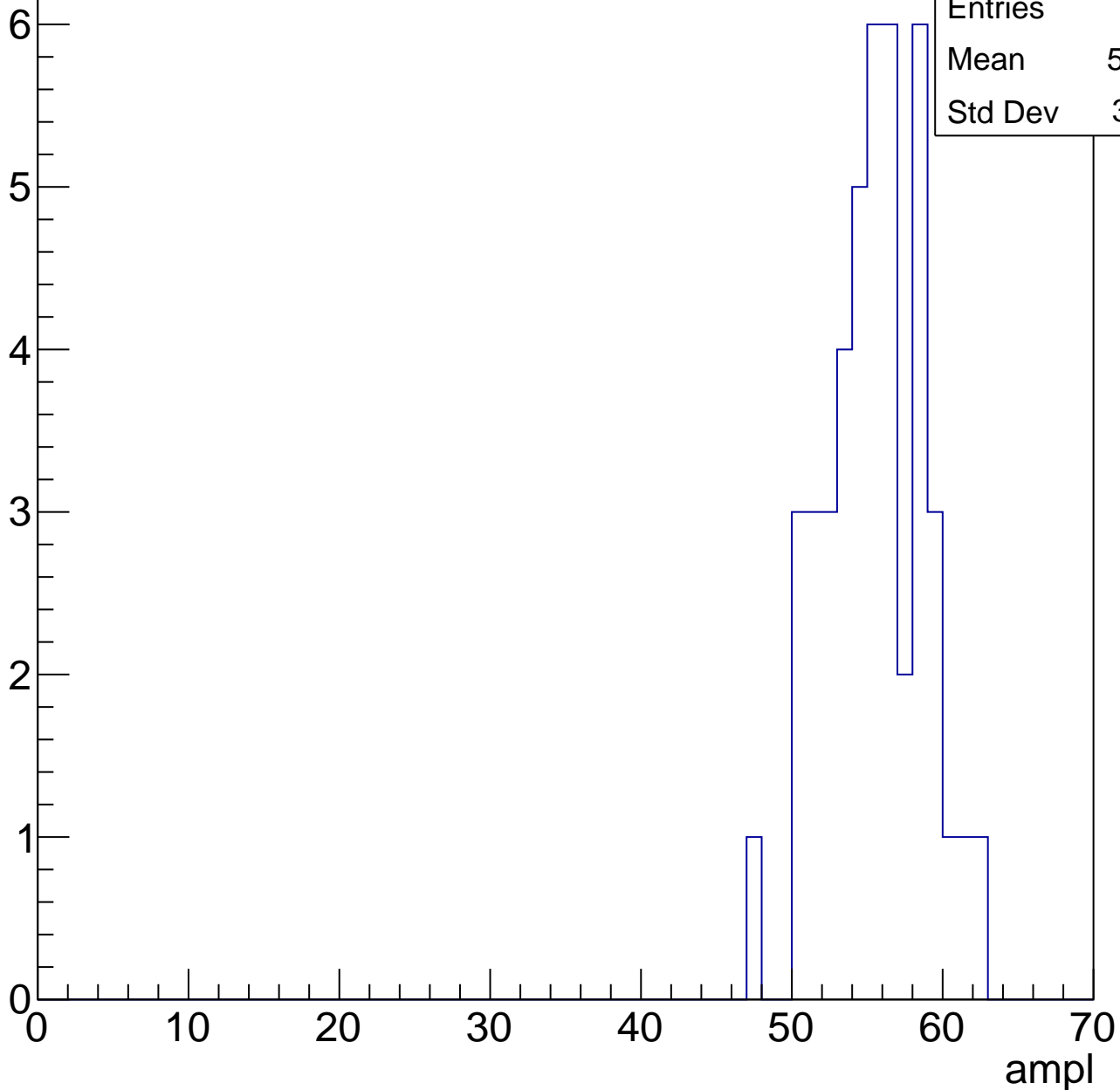


# B1L101S, U8-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	55.02
Std Dev	3.201

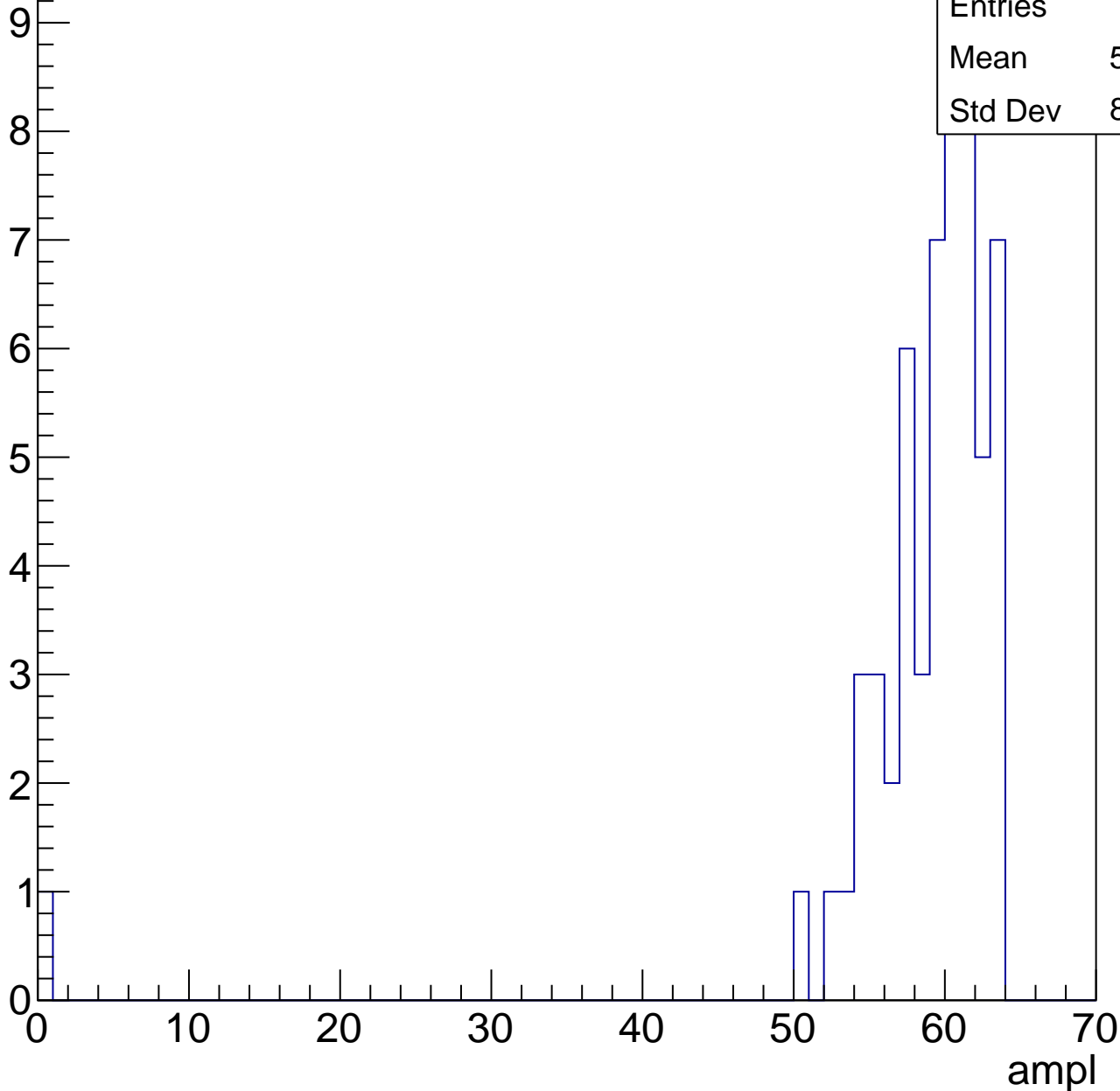


# B1L101S, U8-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

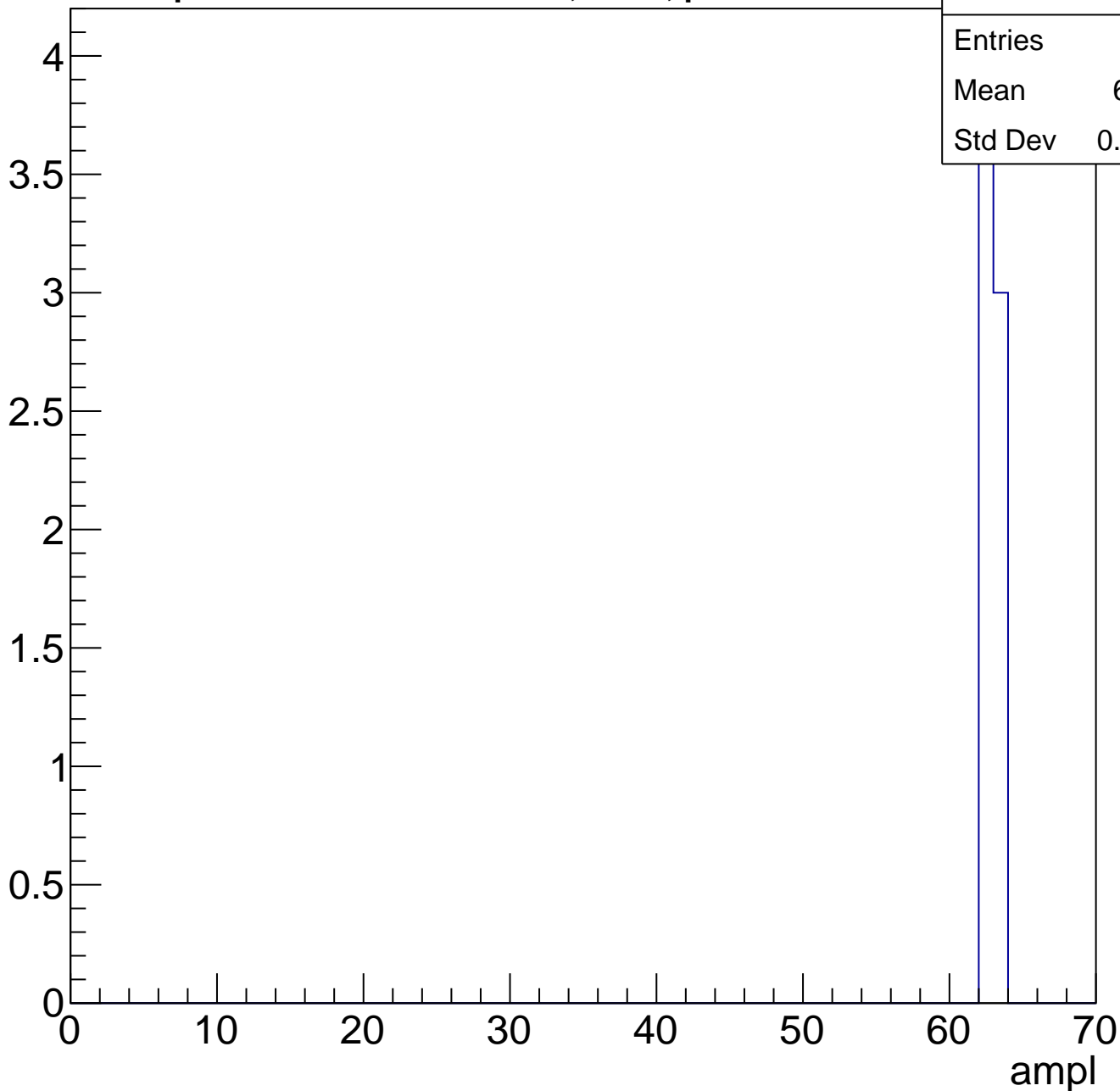
Entries	57
Mean	57.93
Std Dev	8.322



# B1L101S, U8-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch113, adc0

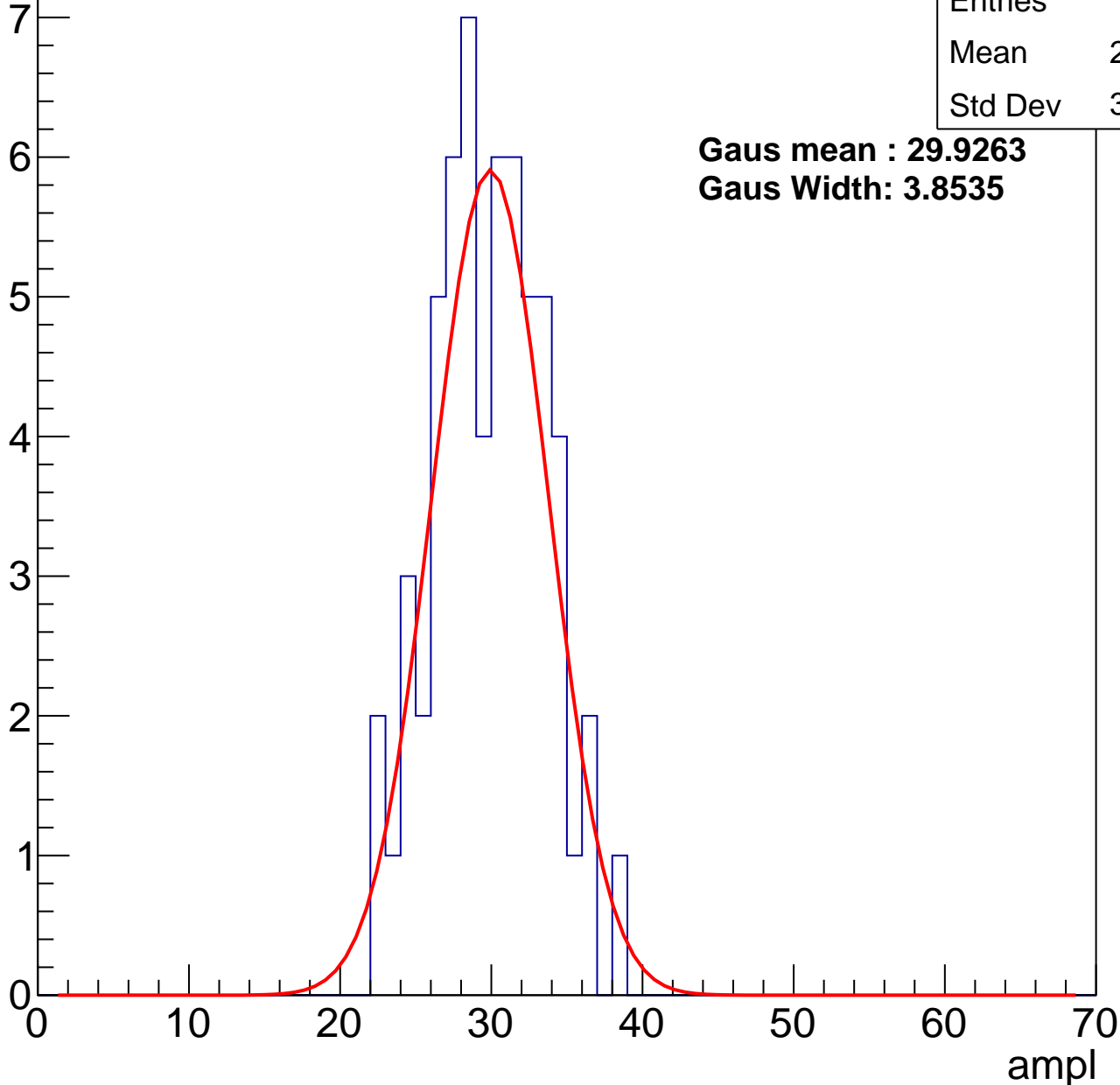
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	29.42
Std Dev	3.598

**Gaus mean : 29.9263**

**Gaus Width: 3.8535**



# B1L101S, U8-ch113, adc1

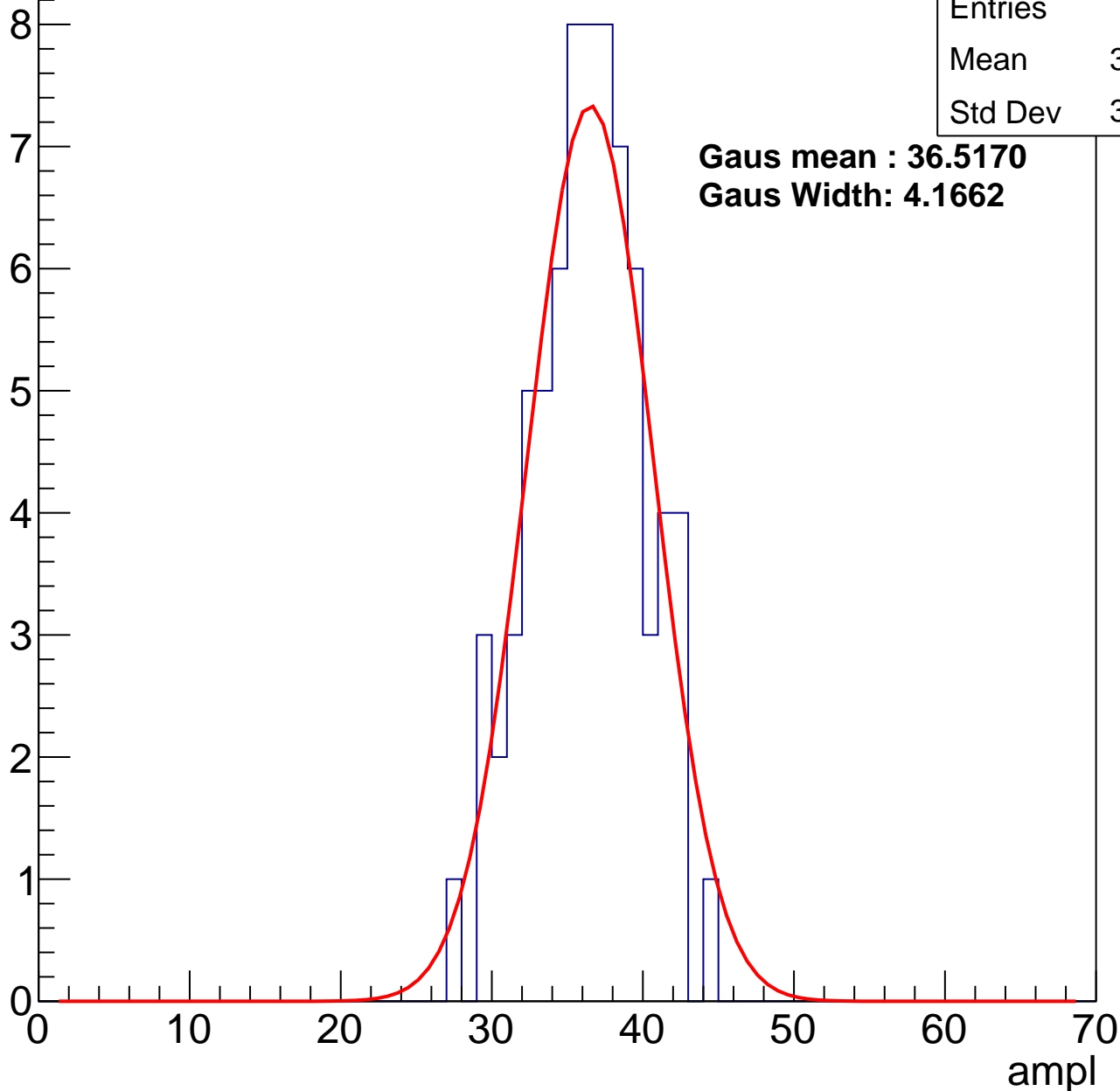
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	35.89
Std Dev	3.634

**Gaus mean : 36.5170**

**Gaus Width: 4.1662**



# B1L101S, U8-ch113, adc2

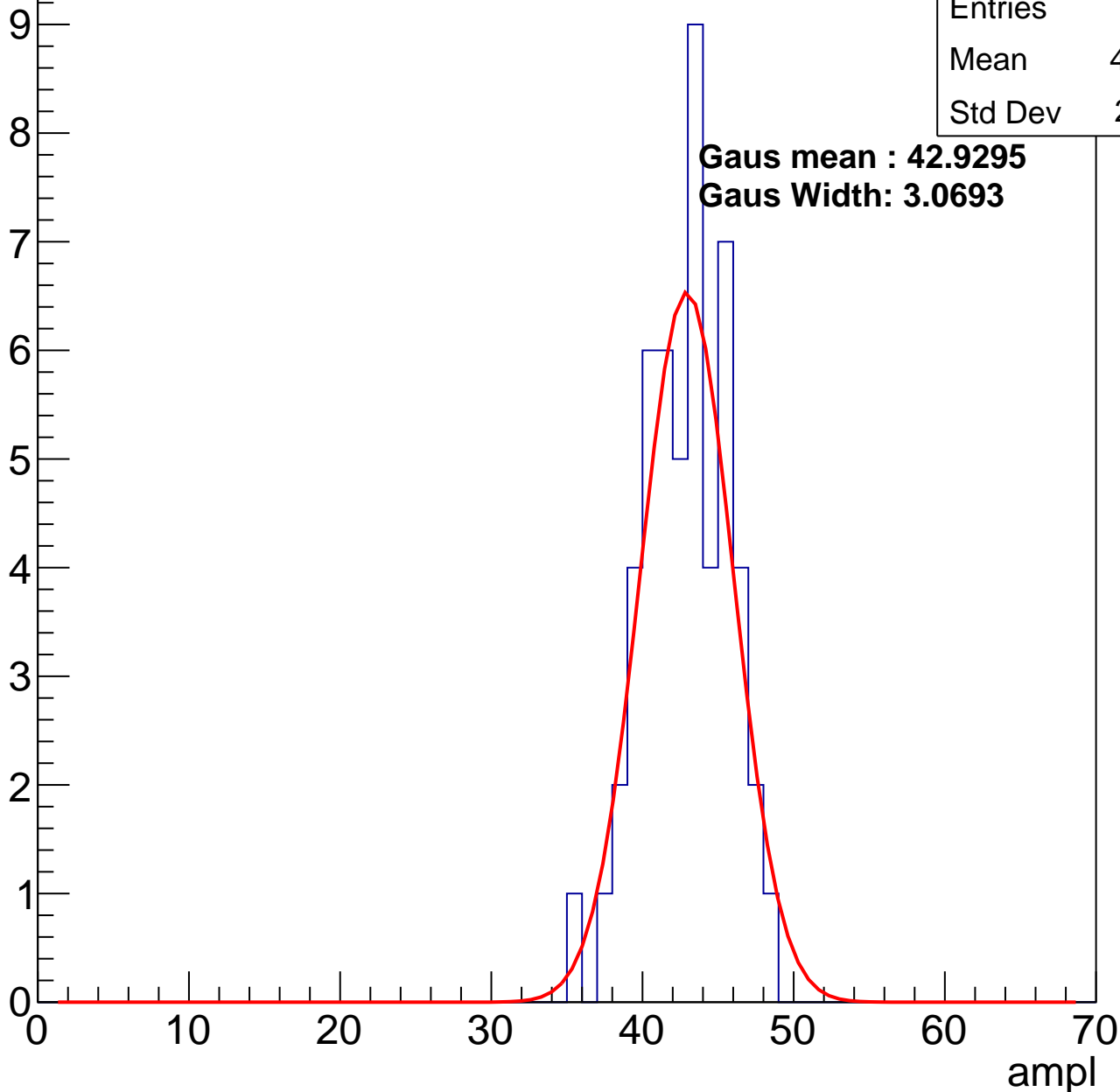
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	42.38
Std Dev	2.781

**Gaus mean : 42.9295**

**Gaus Width: 3.0693**

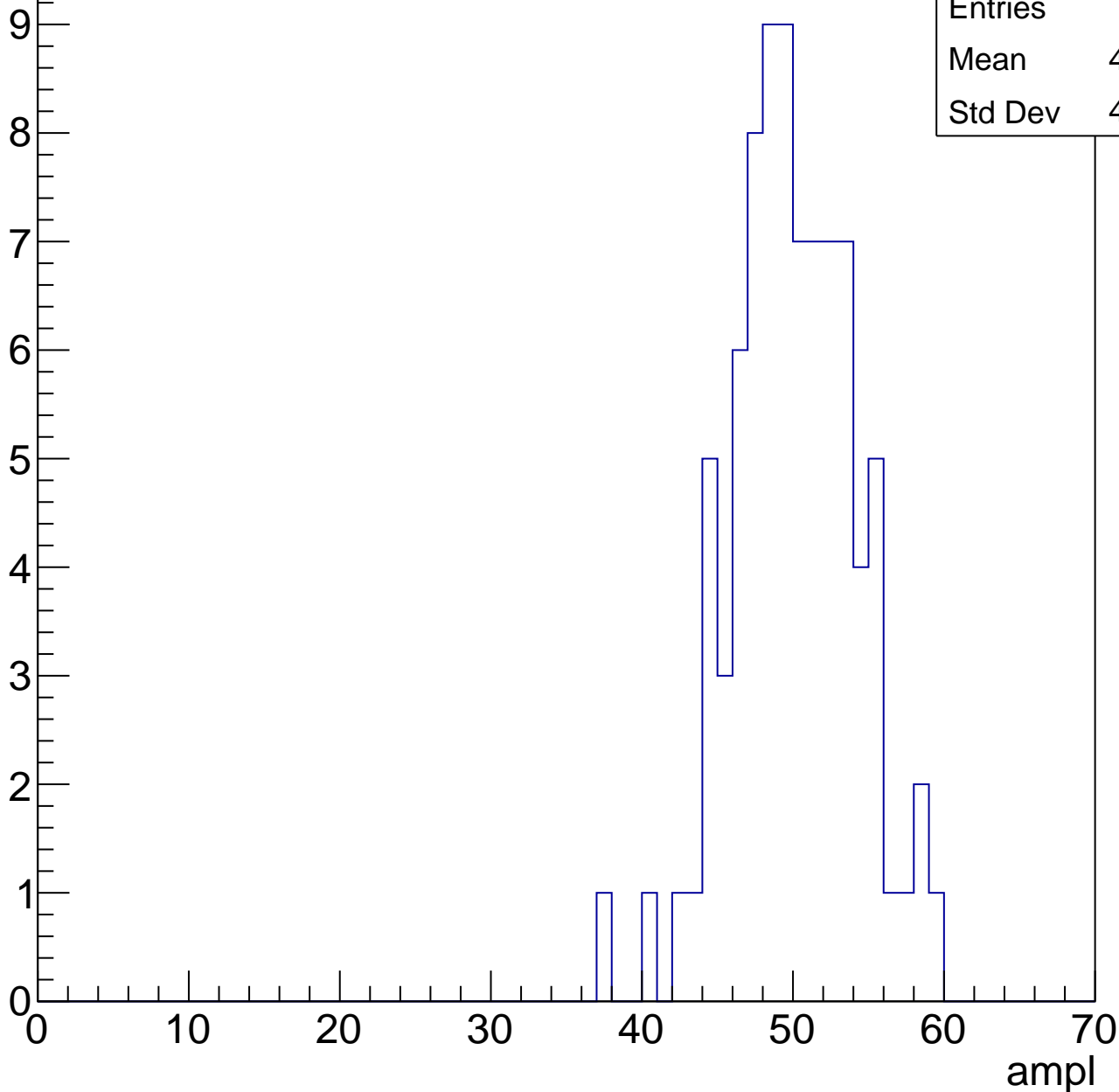


# B1L101S, U8-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

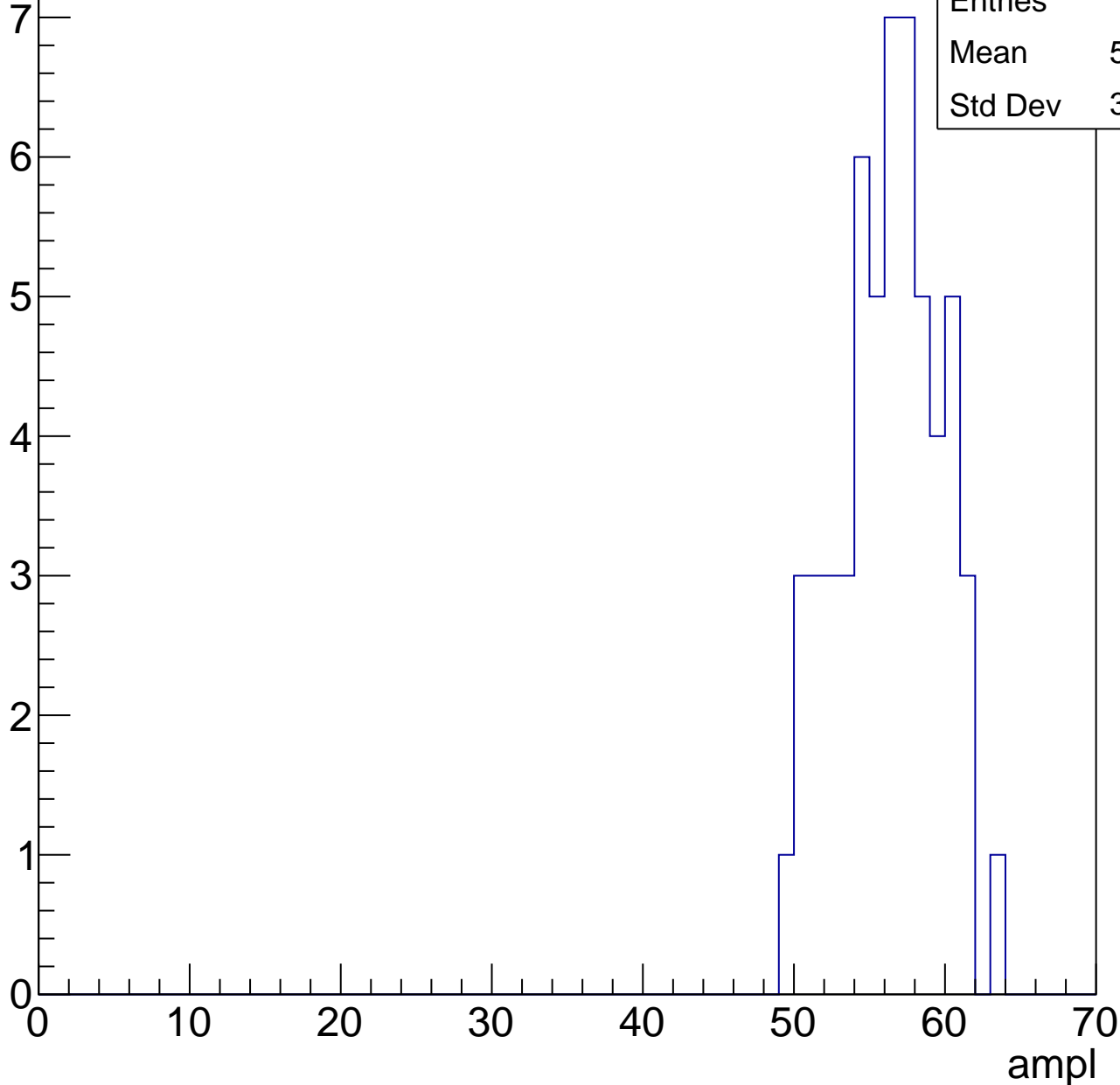
Entries	86
Mean	49.57
Std Dev	4.056



# B1L101S, U8-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

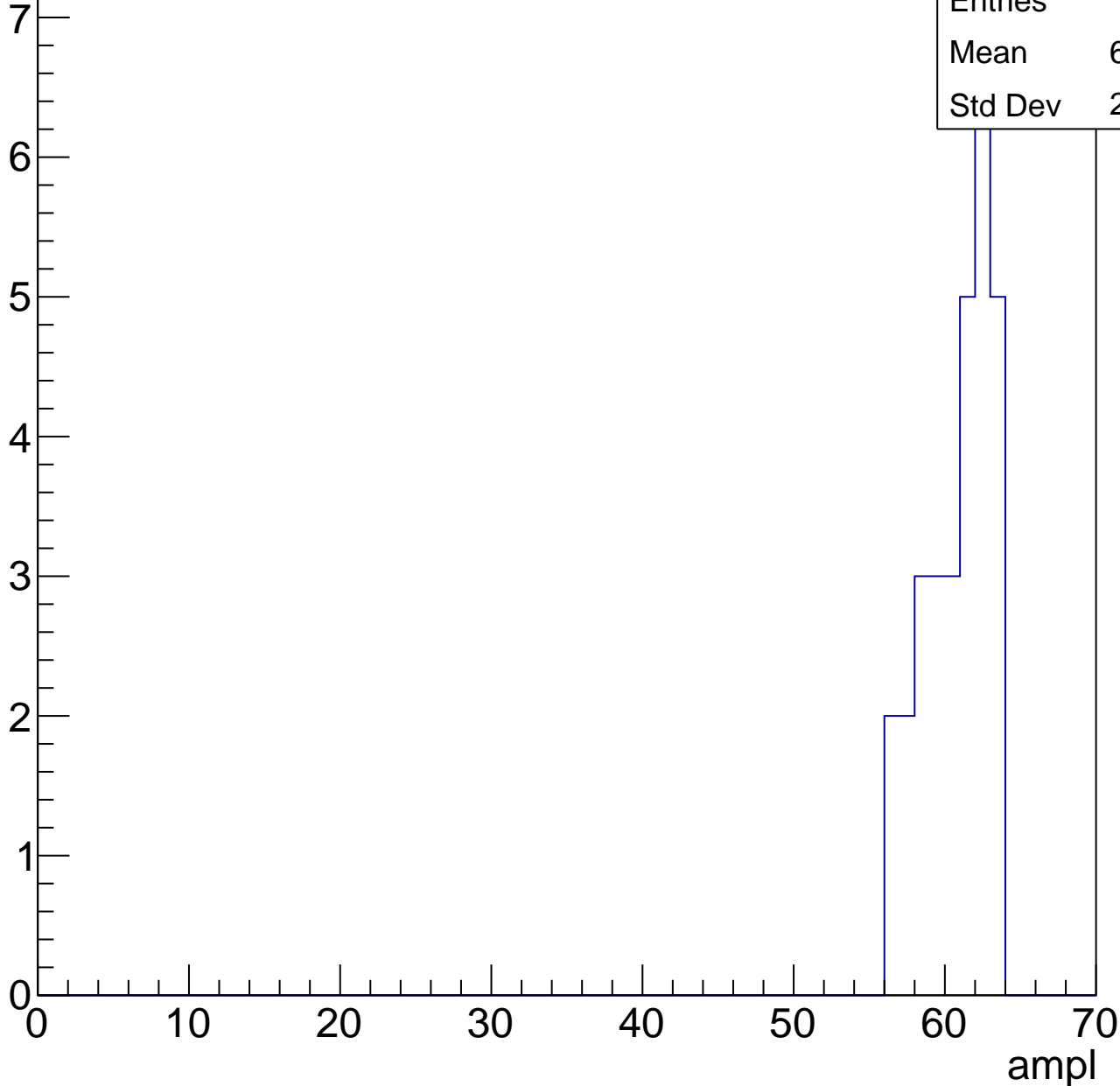


# B1L101S, U8-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

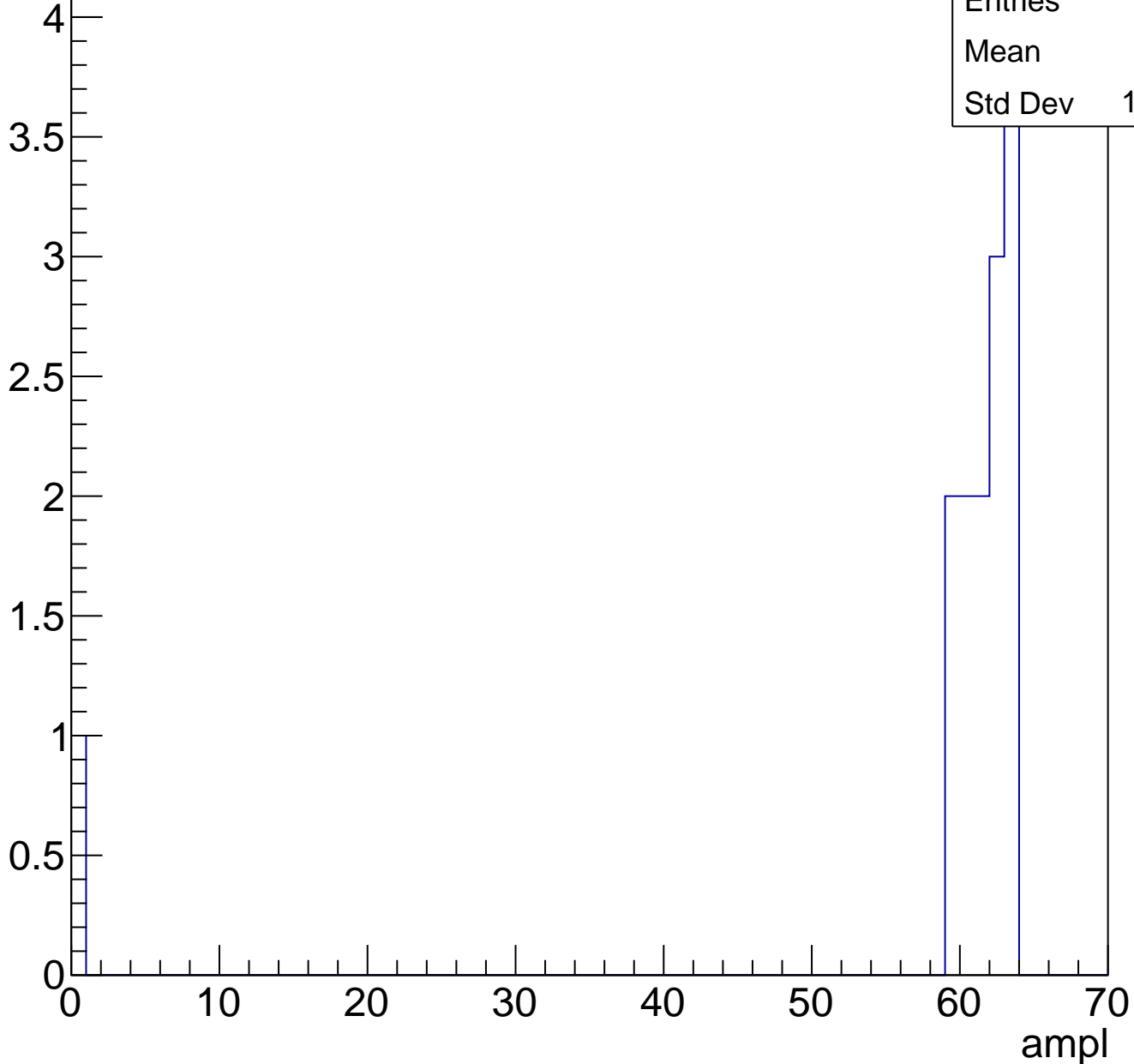
Entries	30
Mean	60.37
Std Dev	2.152



# B1L101S, U8-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch114, adc0

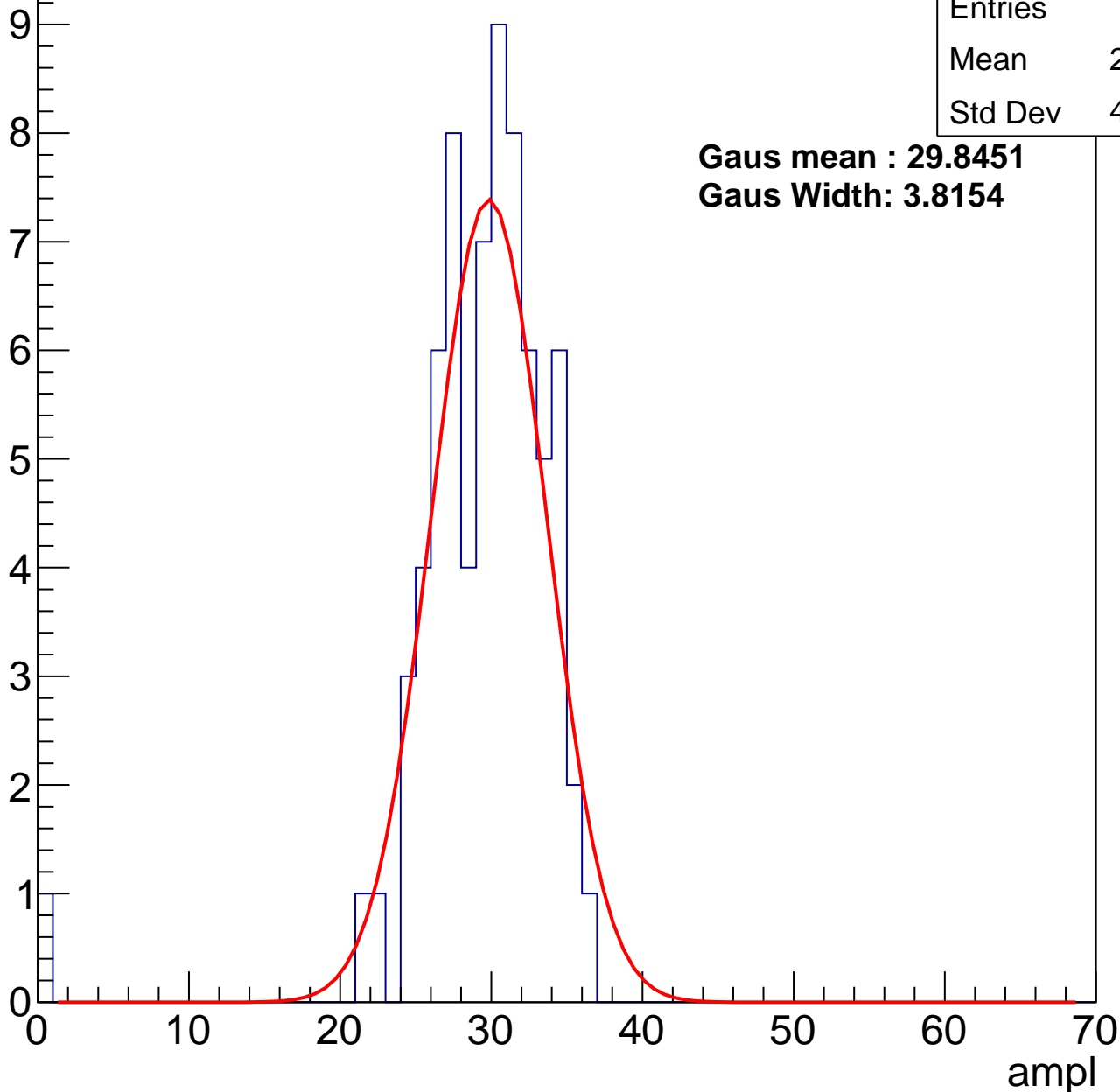
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	28.99
Std Dev	4.757

**Gaus mean : 29.8451**

**Gaus Width: 3.8154**



# B1L101S, U8-ch114, adc1

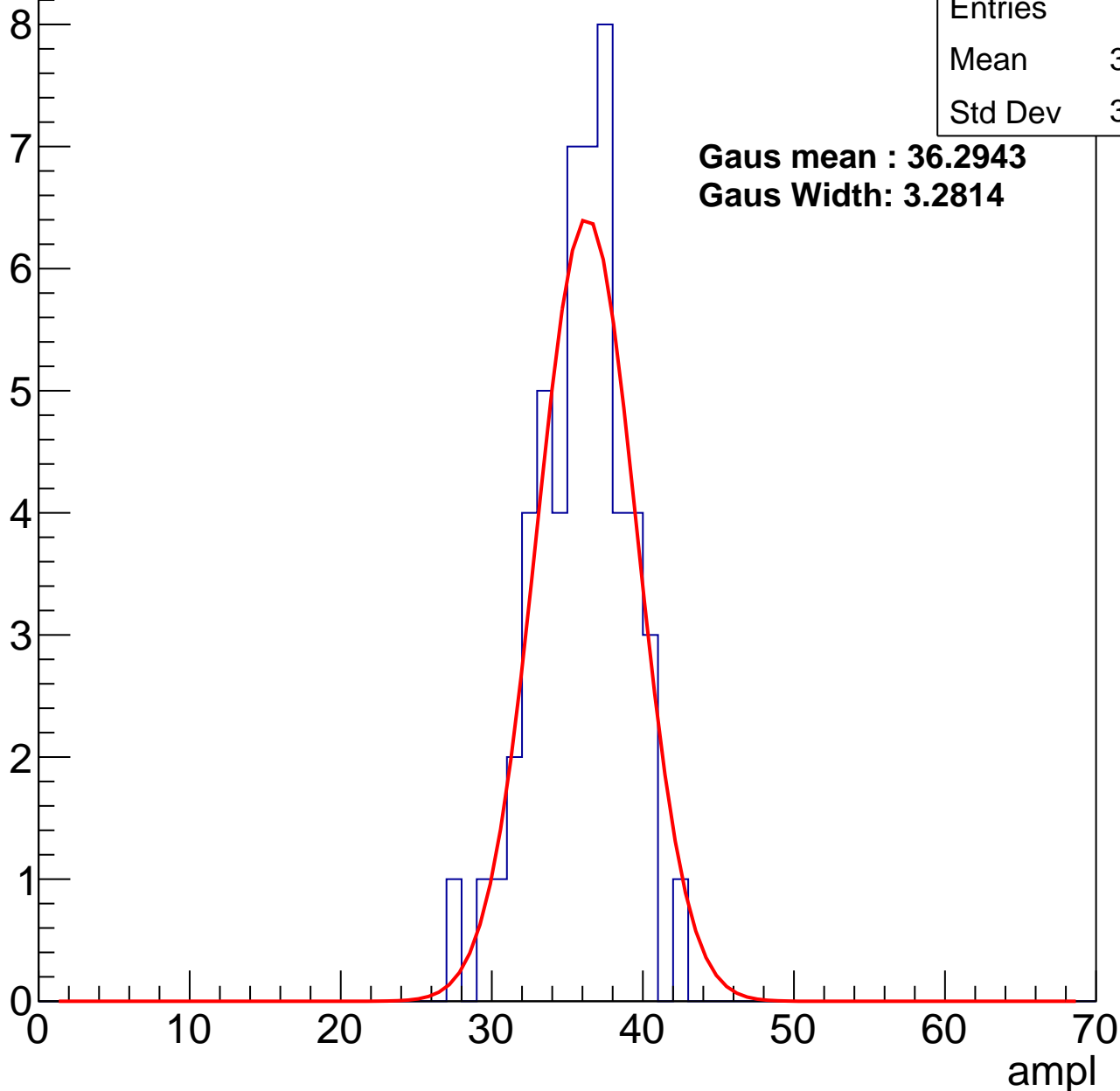
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	35.38
Std Dev	3.014

**Gaus mean : 36.2943**

**Gaus Width: 3.2814**



# B1L101S, U8-ch114, adc2

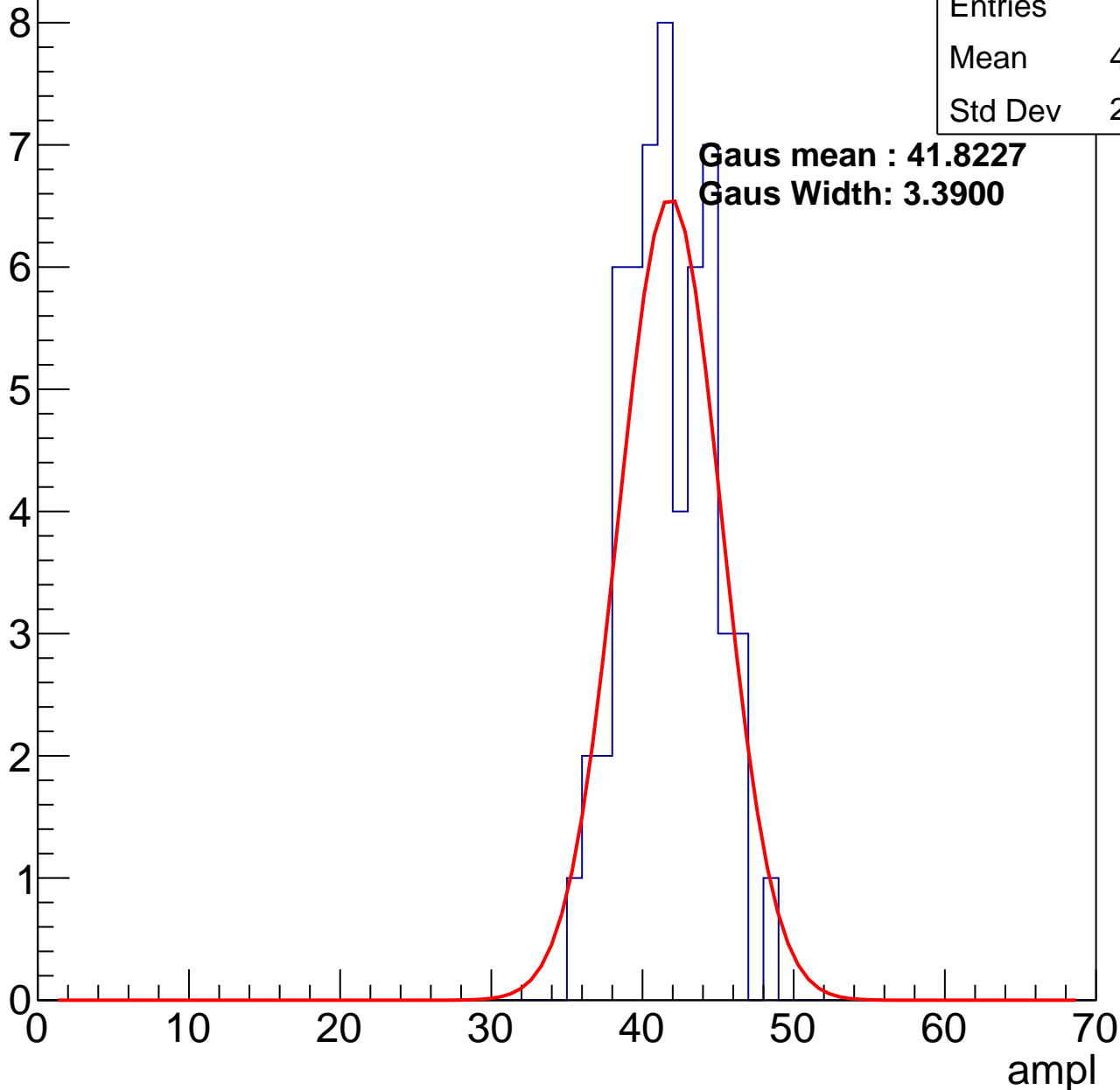
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	41.18
Std Dev	2.879

**Gaus mean : 41.8227**

**Gaus Width: 3.3900**



# B1L101S, U8-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	82
Mean	47.98
Std Dev	3.558

Entry

10

8

6

4

2

0

0

10

20

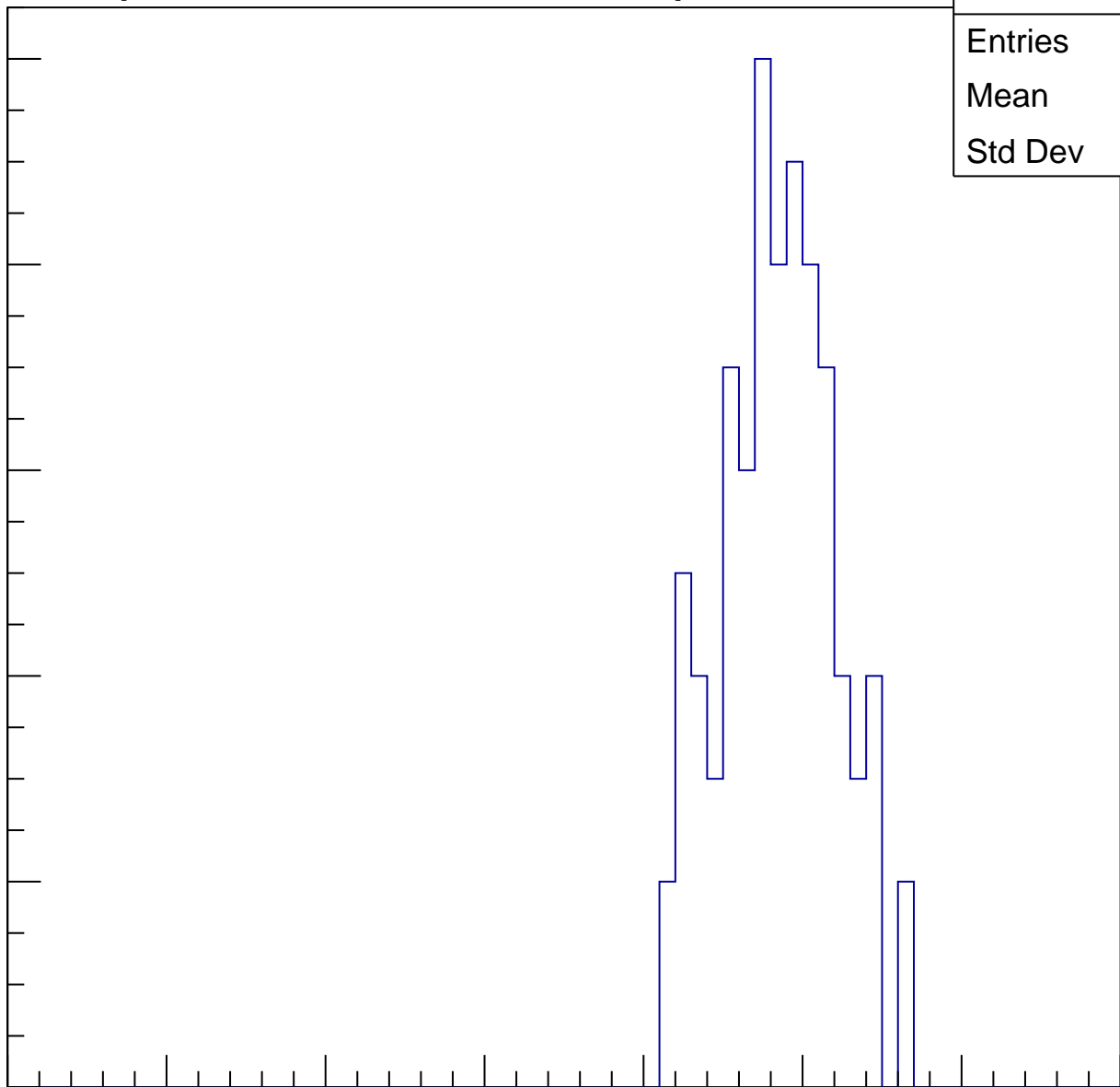
30

40

50

60

ampl

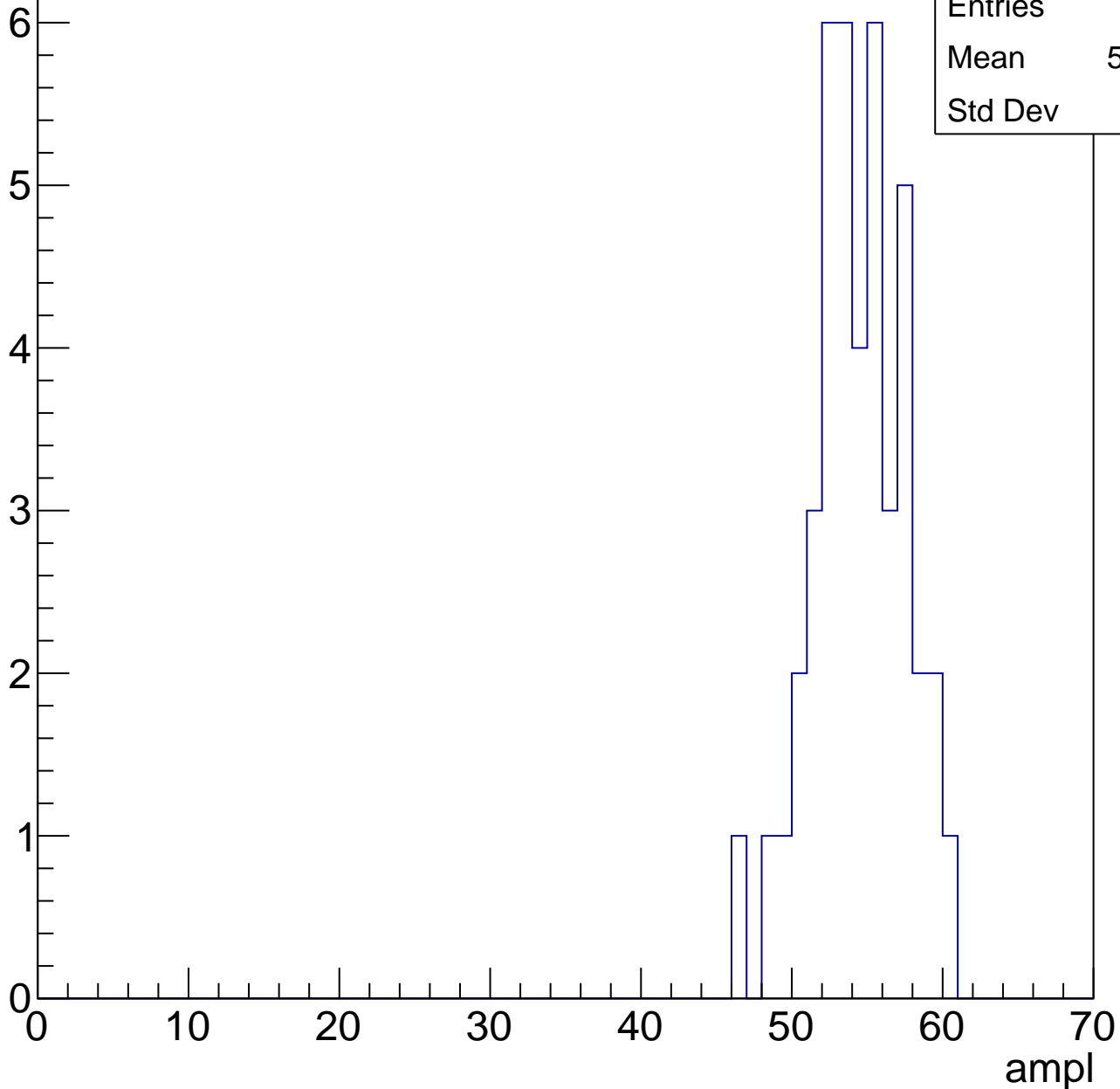


# B1L101S, U8-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

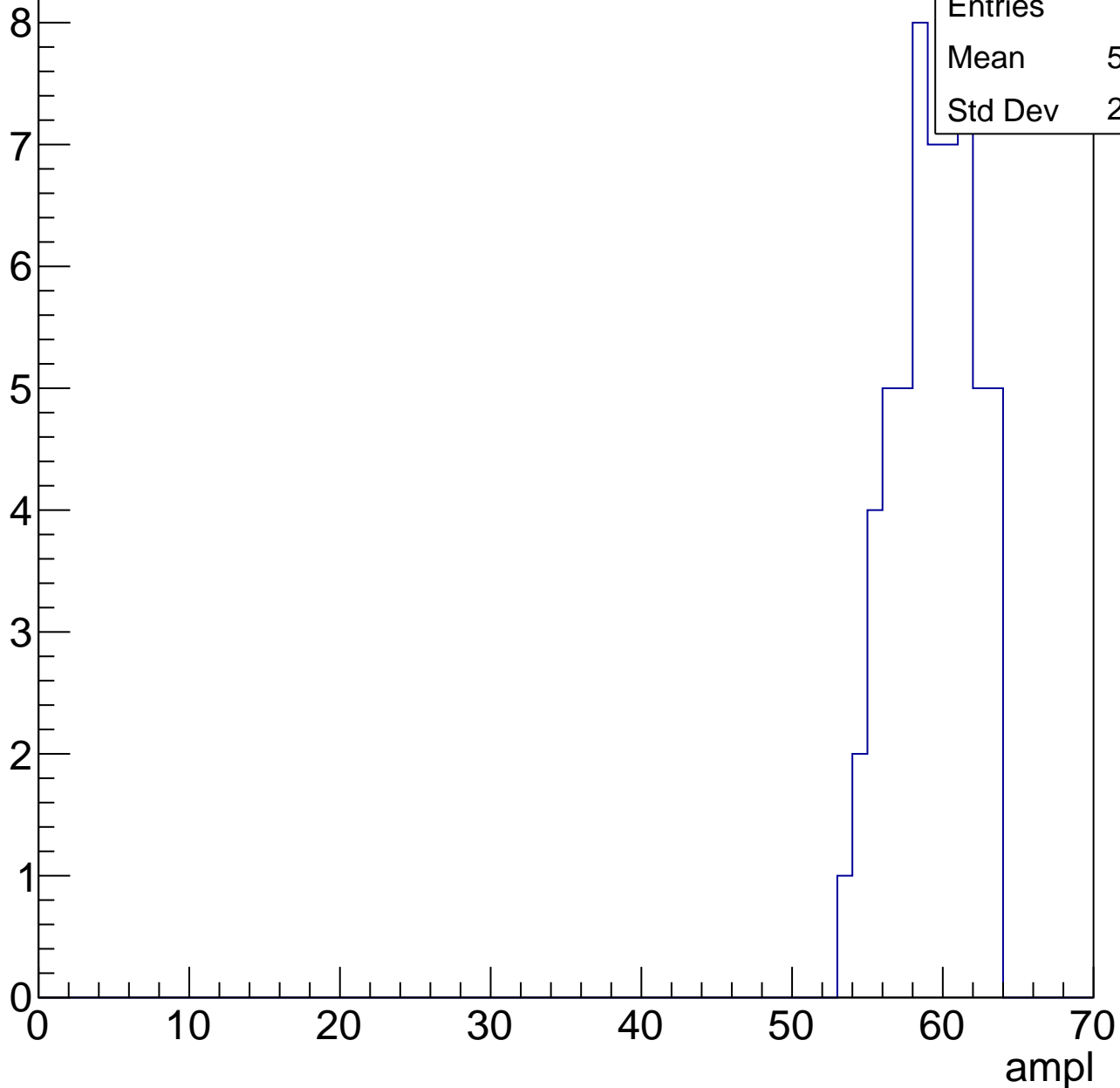
Entries	43
Mean	53.93
Std Dev	3.03



# B1L101S, U8-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



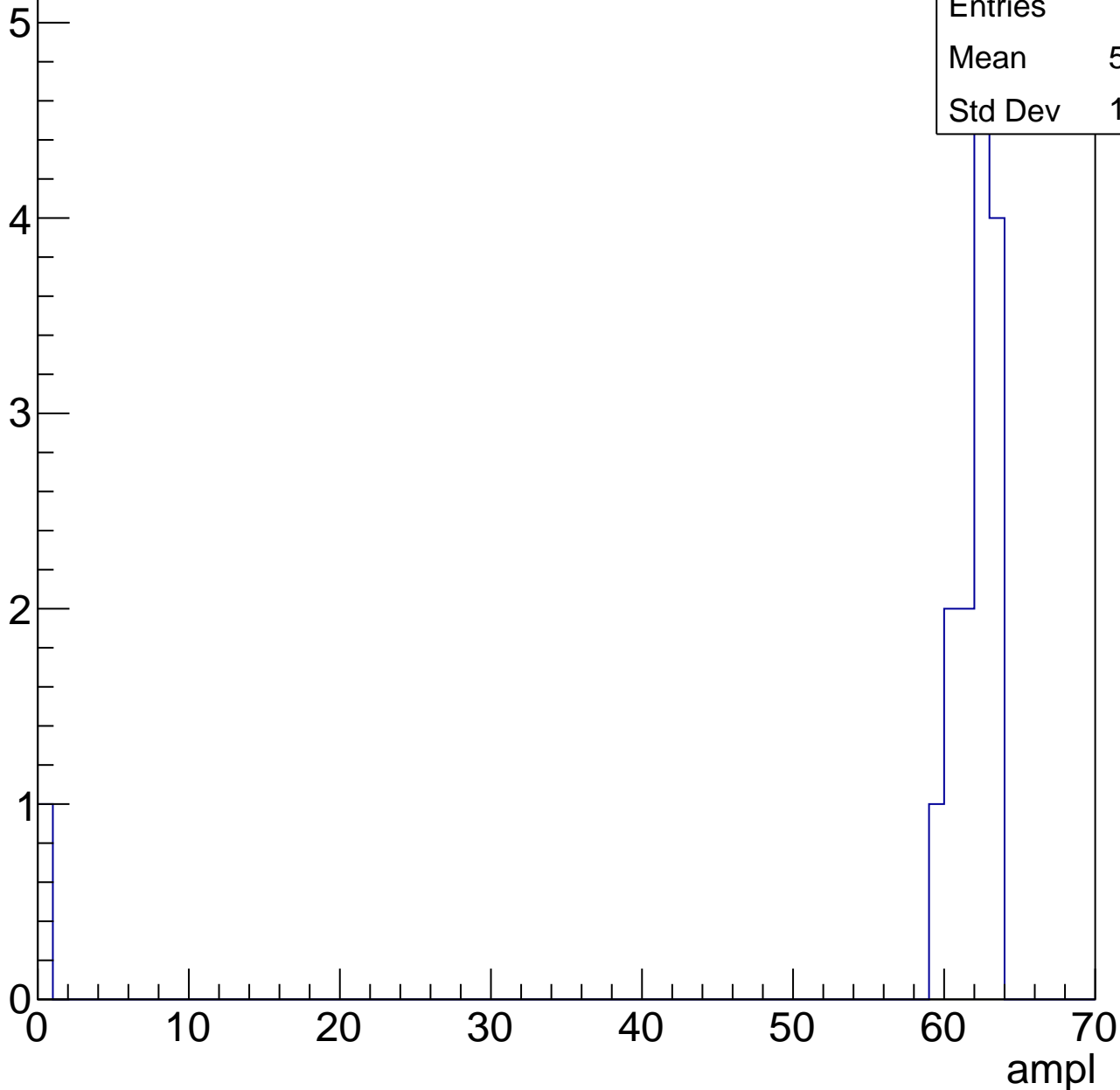
Entries	57
Mean	58.88
Std Dev	2.603

# B1L101S, U8-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	15
Mean	57.53
Std Dev	15.42





# B1L101S, U8-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L101S, U8-ch115, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	70
Mean	28.67
Std Dev	4.65

**Gaus mean : 29.7886**

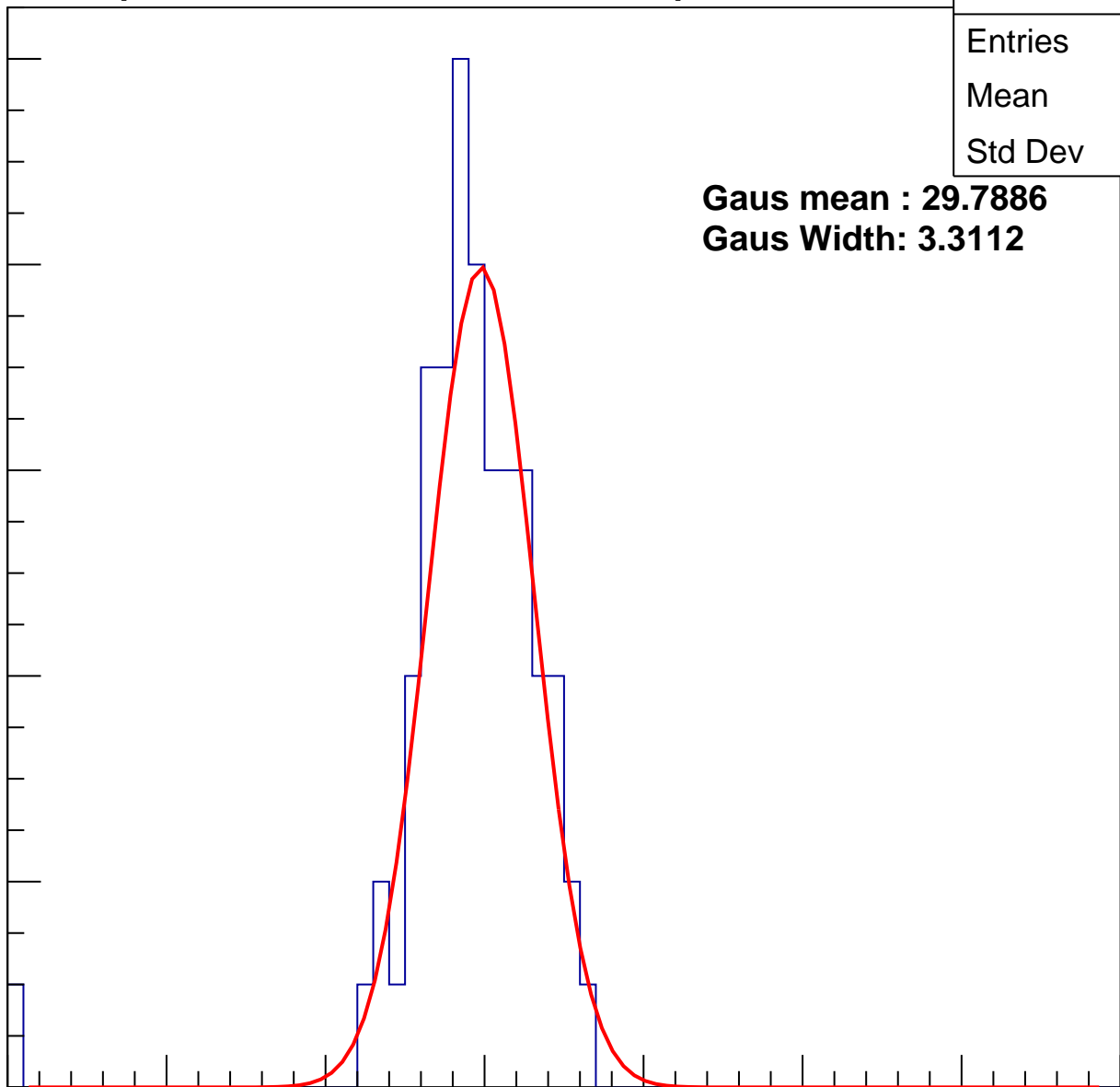
**Gaus Width: 3.3112**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



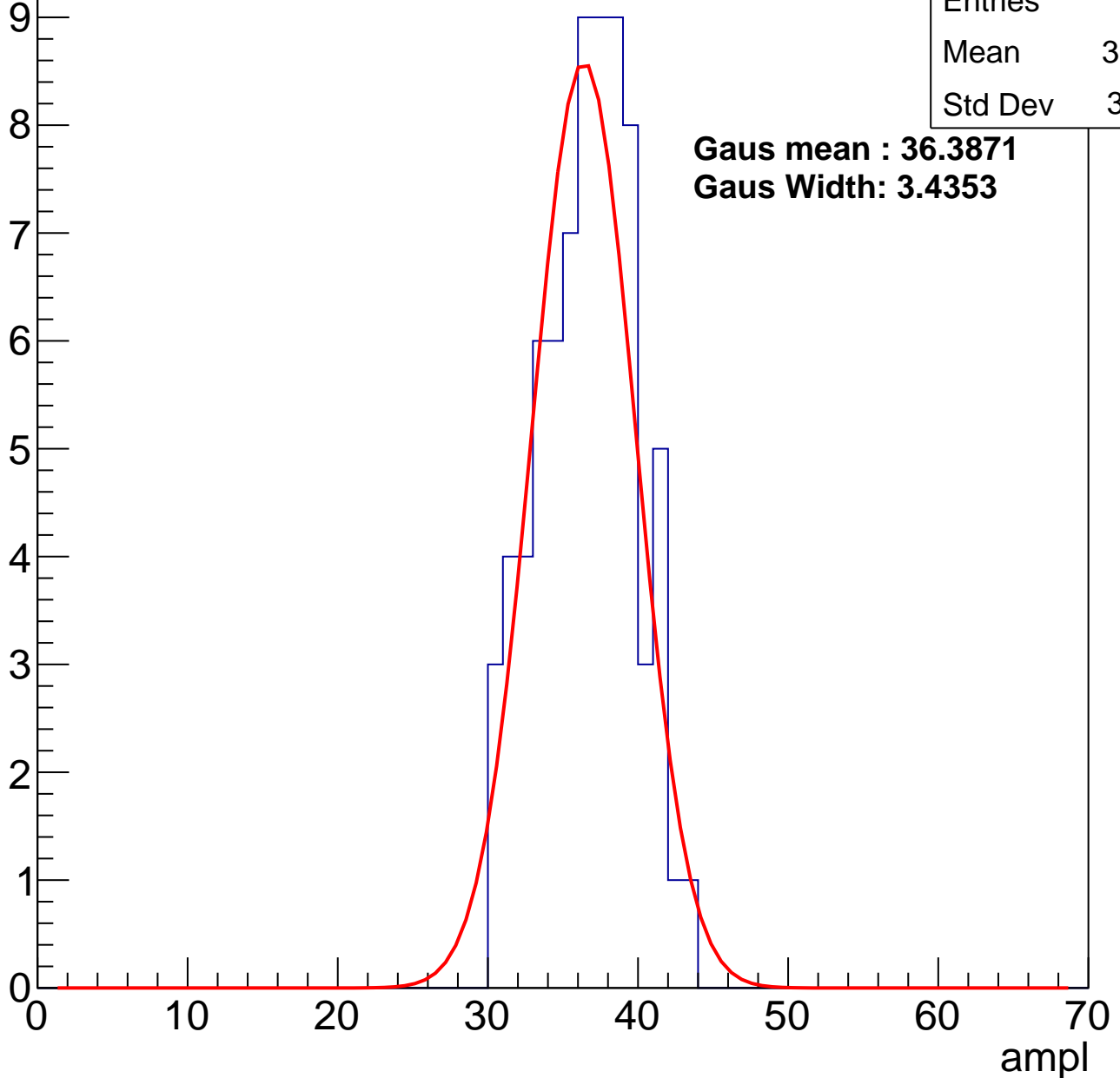
# B1L101S, U8-ch115, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	36.13
Std Dev	3.121

**Gaus mean : 36.3871**  
**Gaus Width: 3.4353**



# B1L101S, U8-ch115, adc2

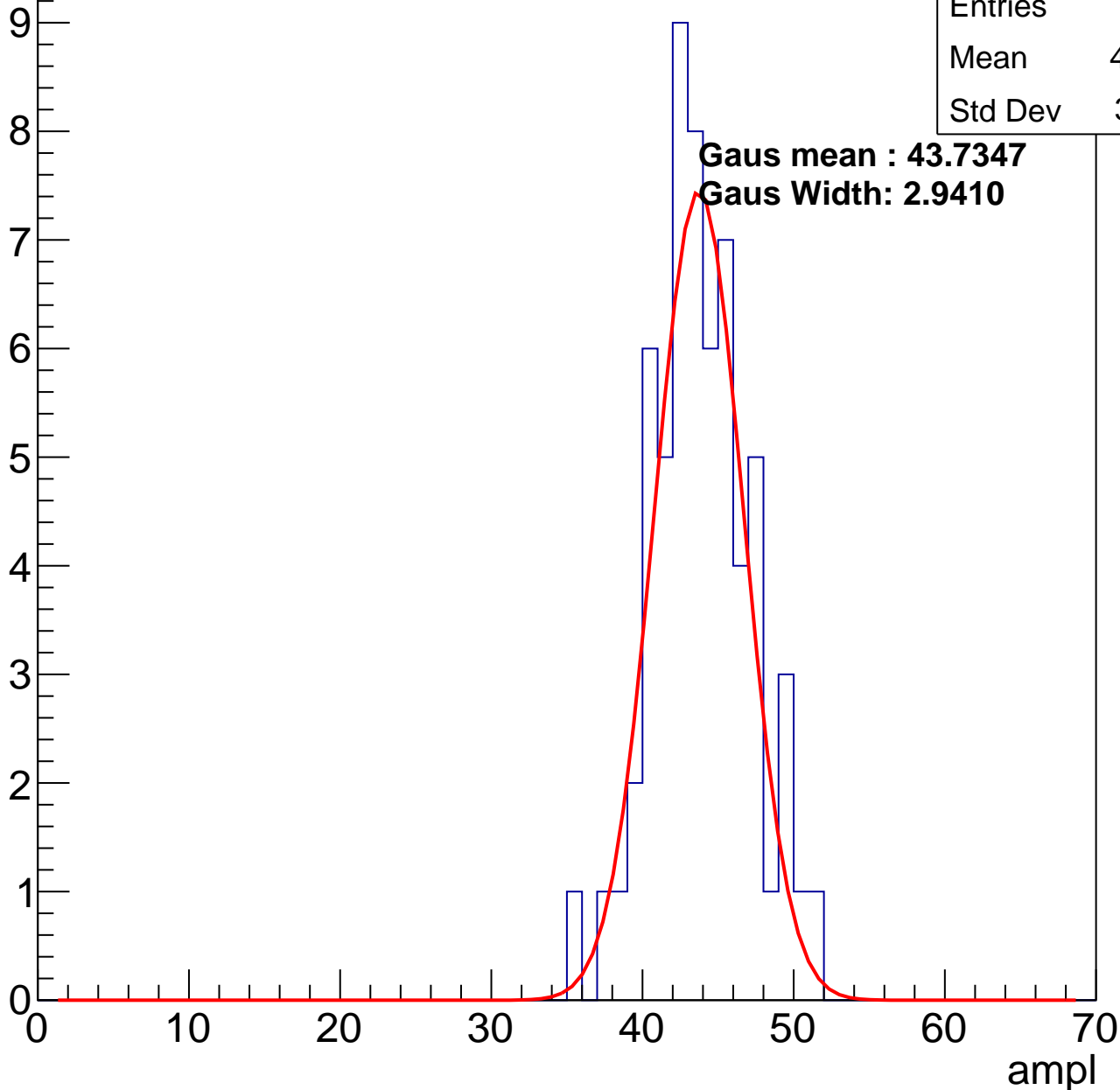
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	43.43
Std Dev	3.201

**Gaus mean : 43.7347**

**Gaus Width: 2.9410**

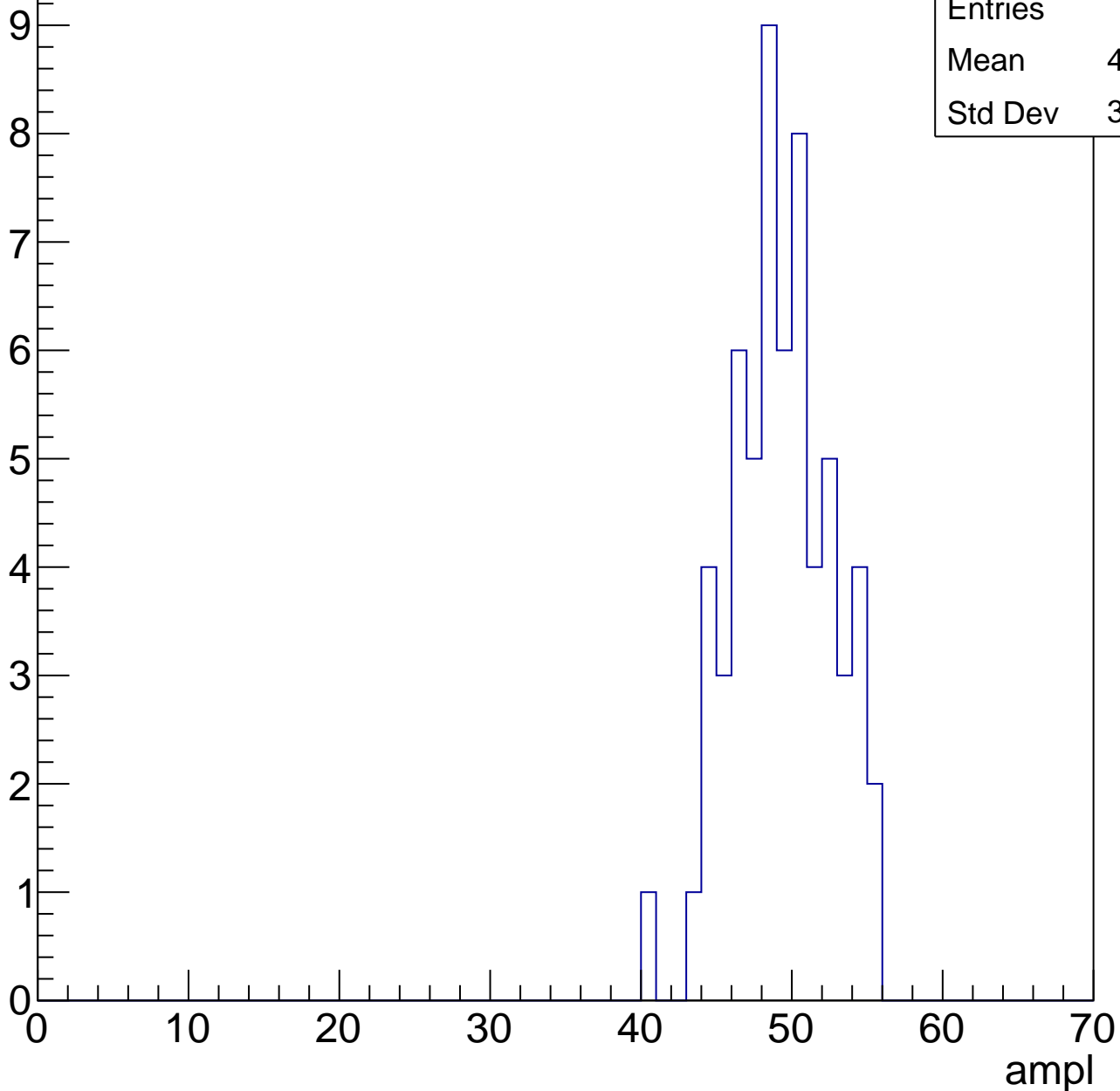


# B1L101S, U8-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	48.85
Std Dev	3.228

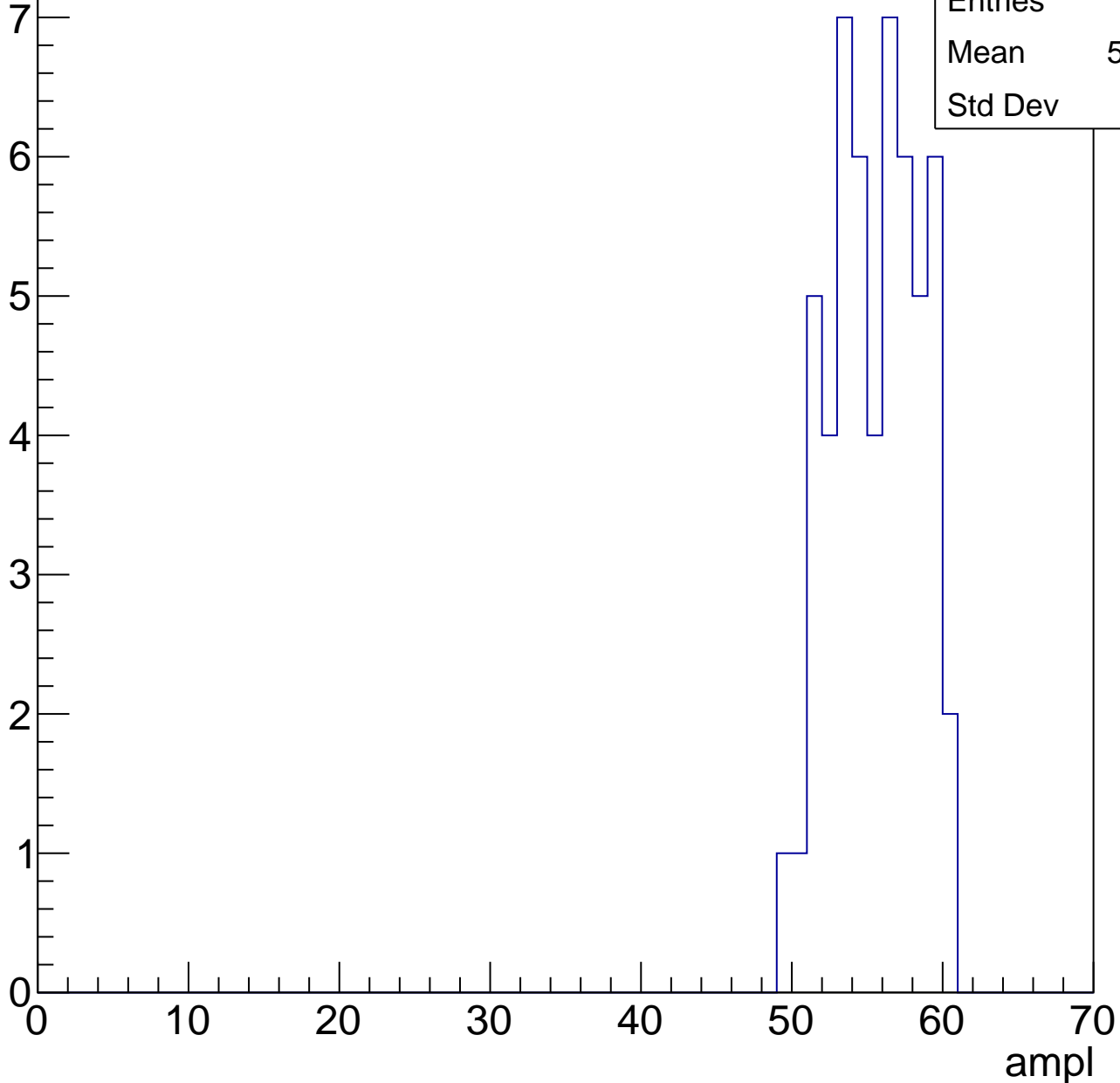


# B1L101S, U8-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	55.09
Std Dev	2.83



# B1L101S, U8-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	51
Mean	58.43
Std Dev	8.676

Entry

10

8

6

4

2

0

0

10

20

30

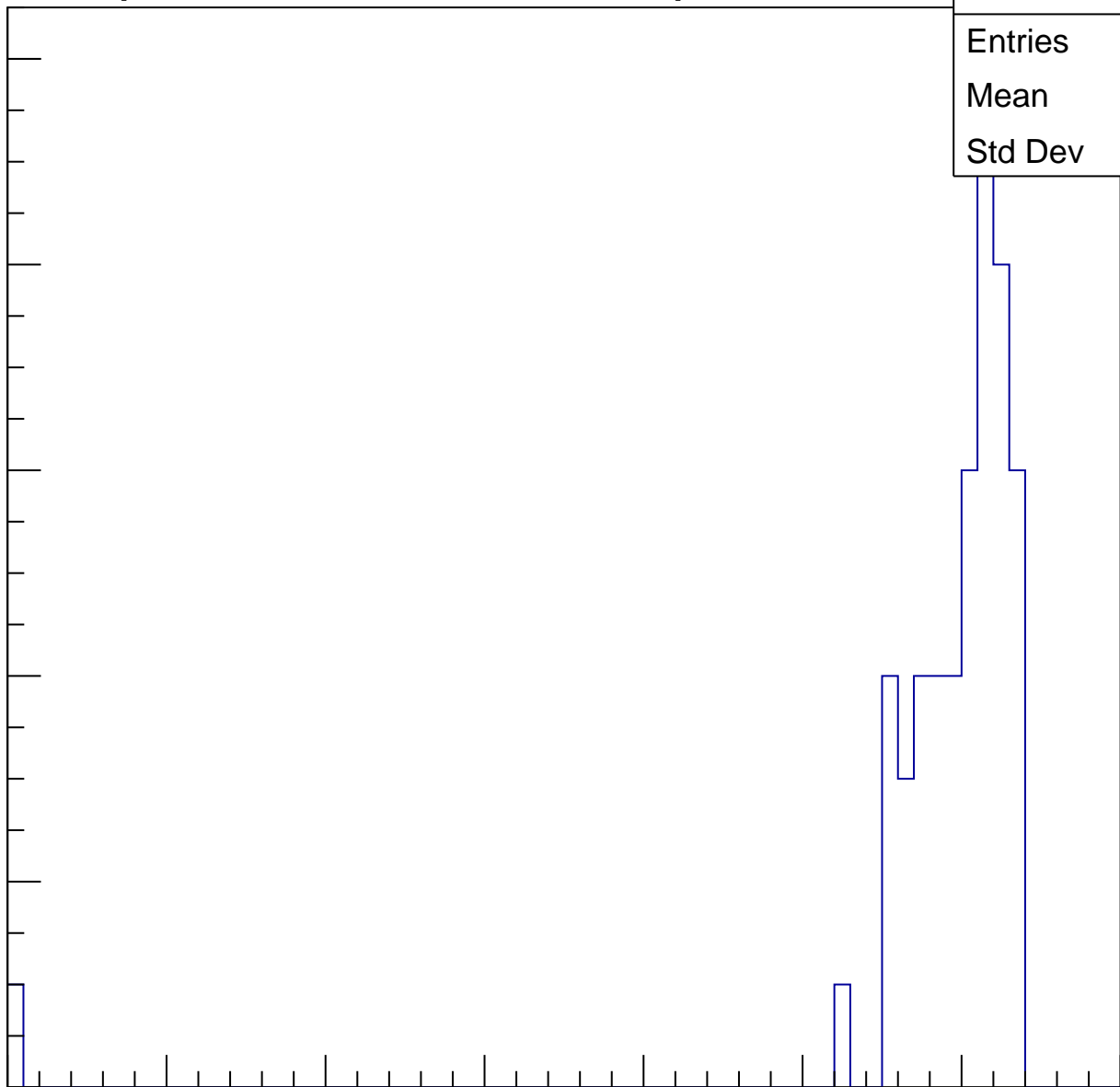
40

50

60

70

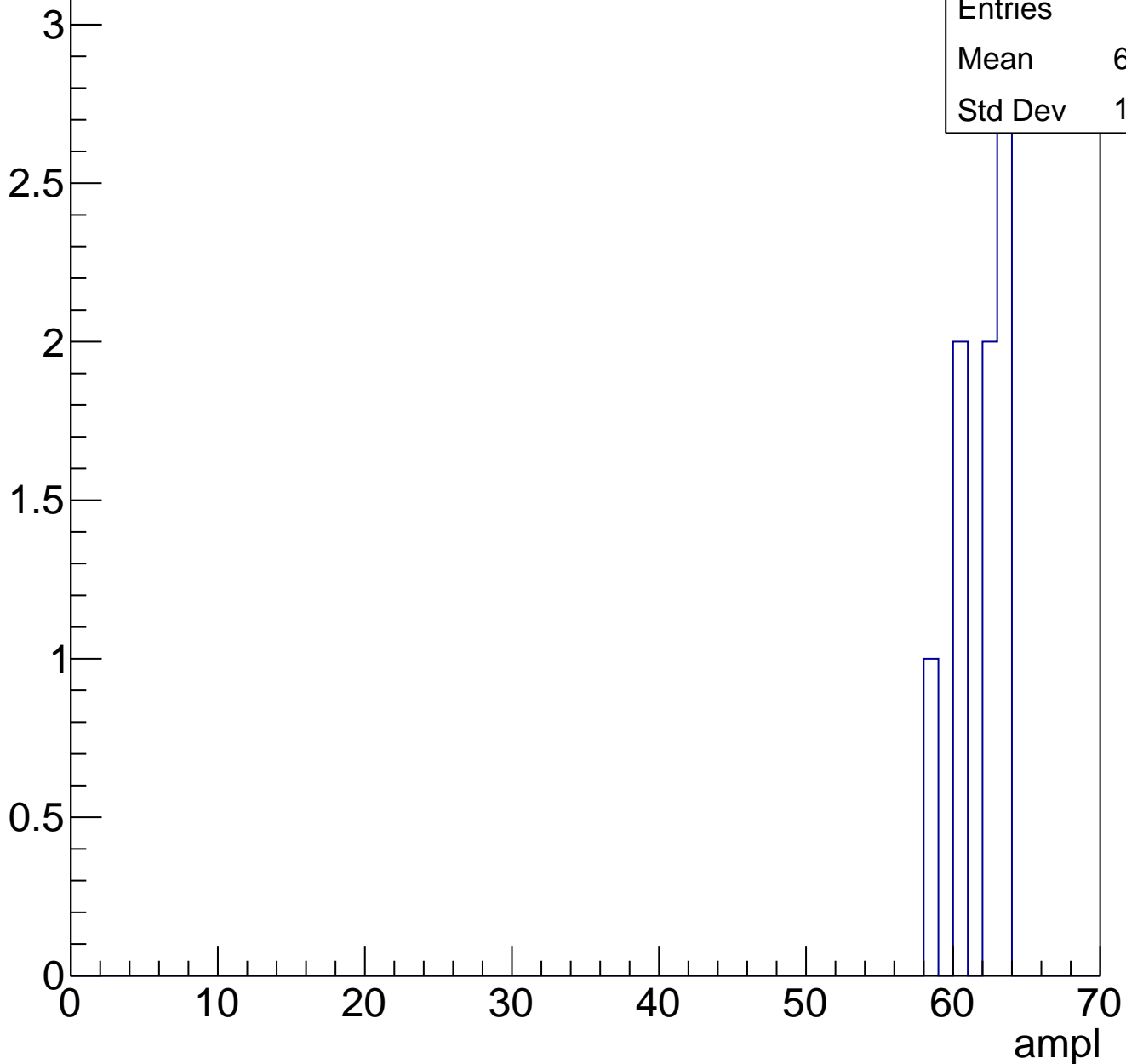
ampl



# B1L101S, U8-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch116, adc0

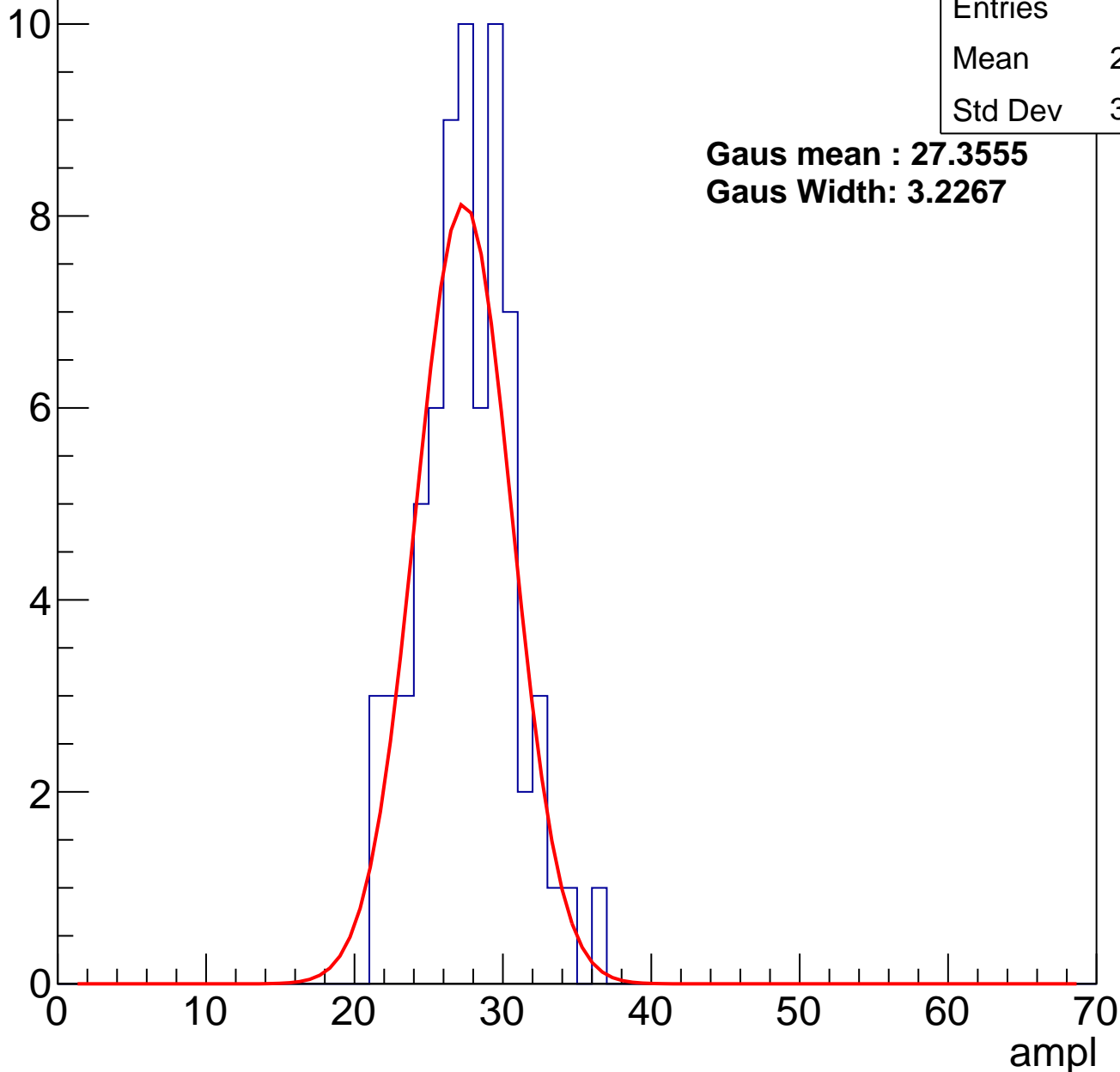
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	70
Mean	27.16
Std Dev	3.138

**Gaus mean : 27.3555**

**Gaus Width: 3.2267**

Entry



# B1L101S, U8-ch116, adc1

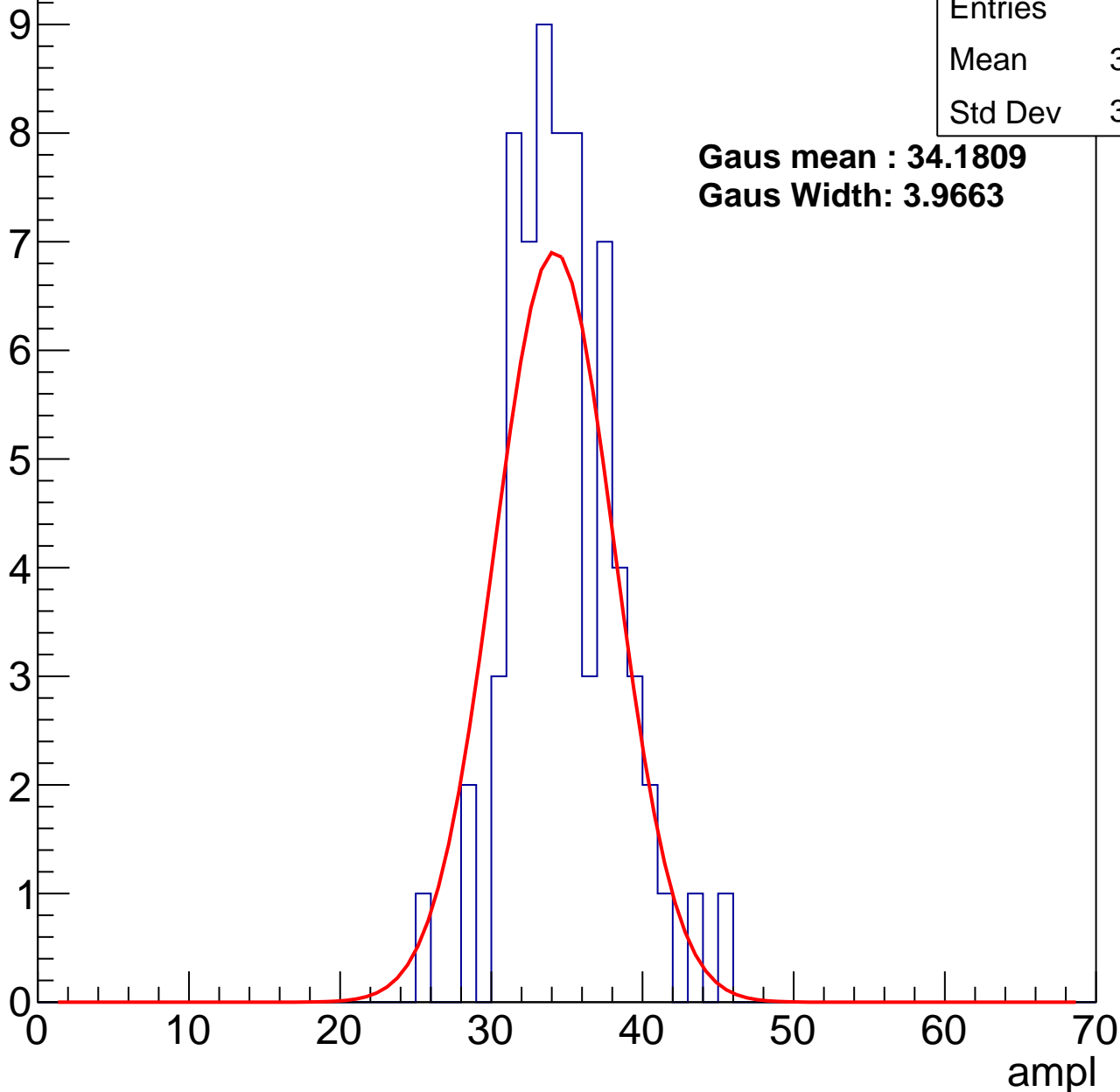
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	34.37
Std Dev	3.527

**Gaus mean : 34.1809**

**Gaus Width: 3.9663**



# B1L101S, U8-ch116, adc2

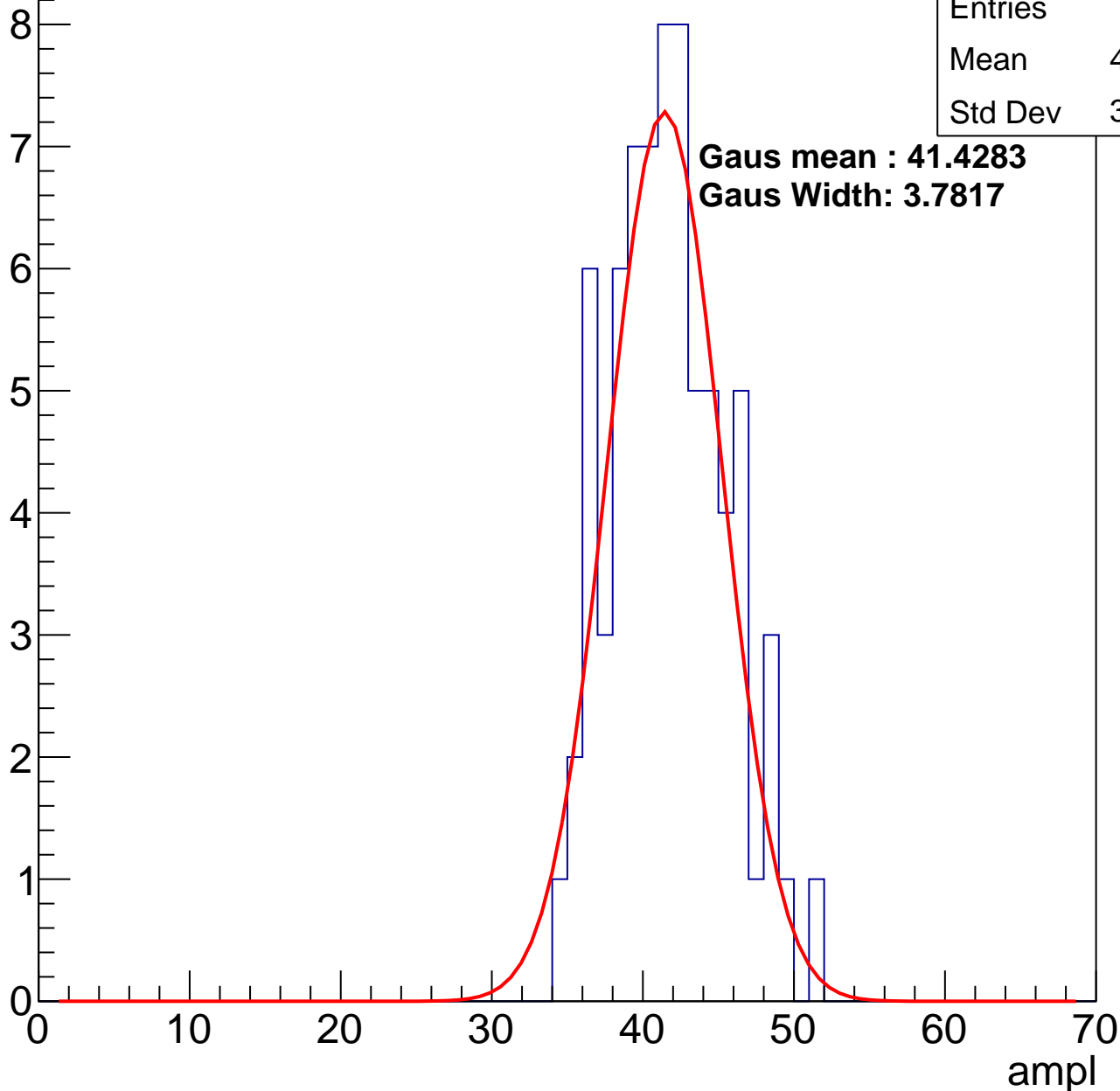
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	41.26
Std Dev	3.723

**Gaus mean : 41.4283**

**Gaus Width: 3.7817**

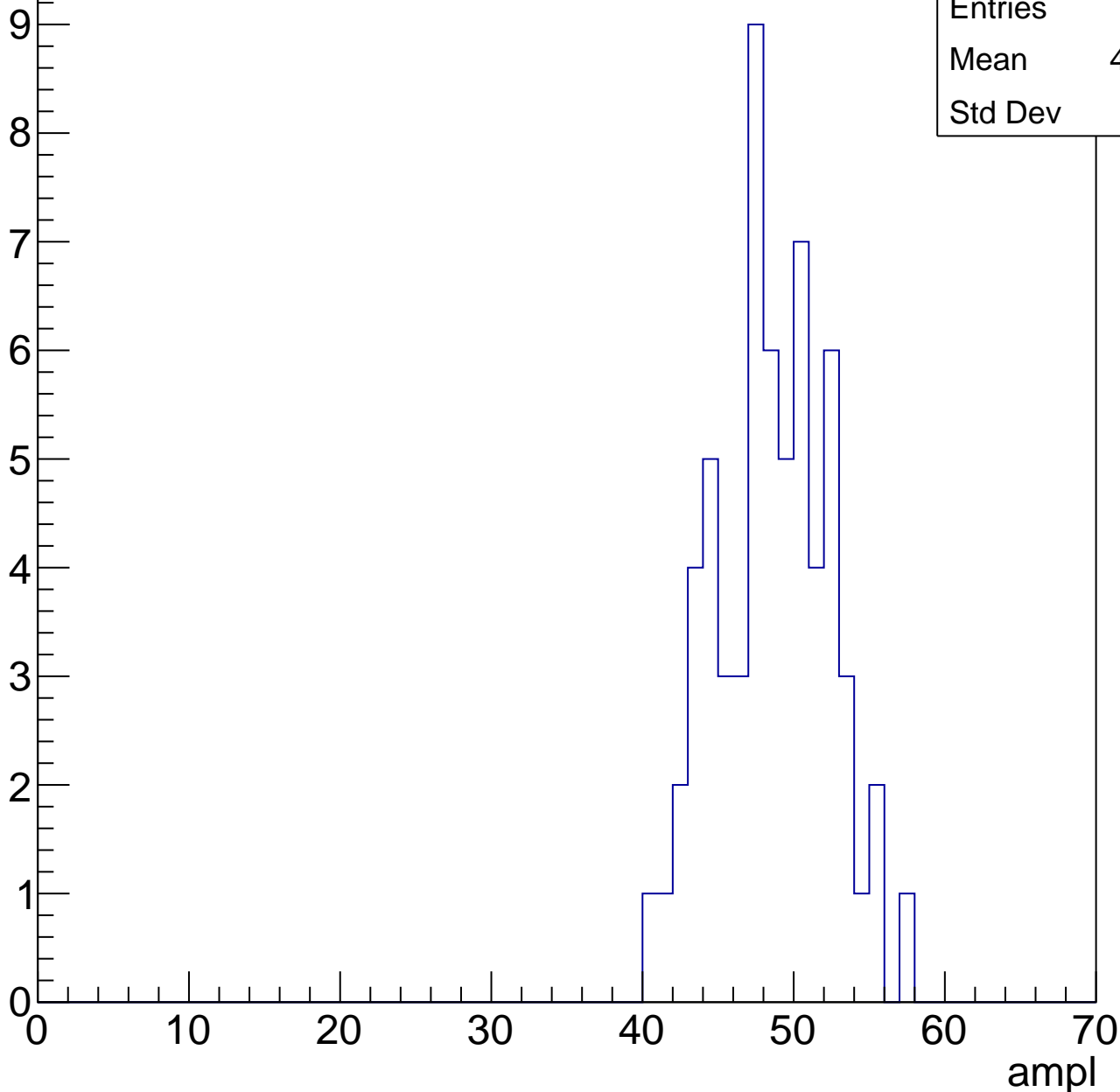


# B1L101S, U8-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	48.13
Std Dev	3.71

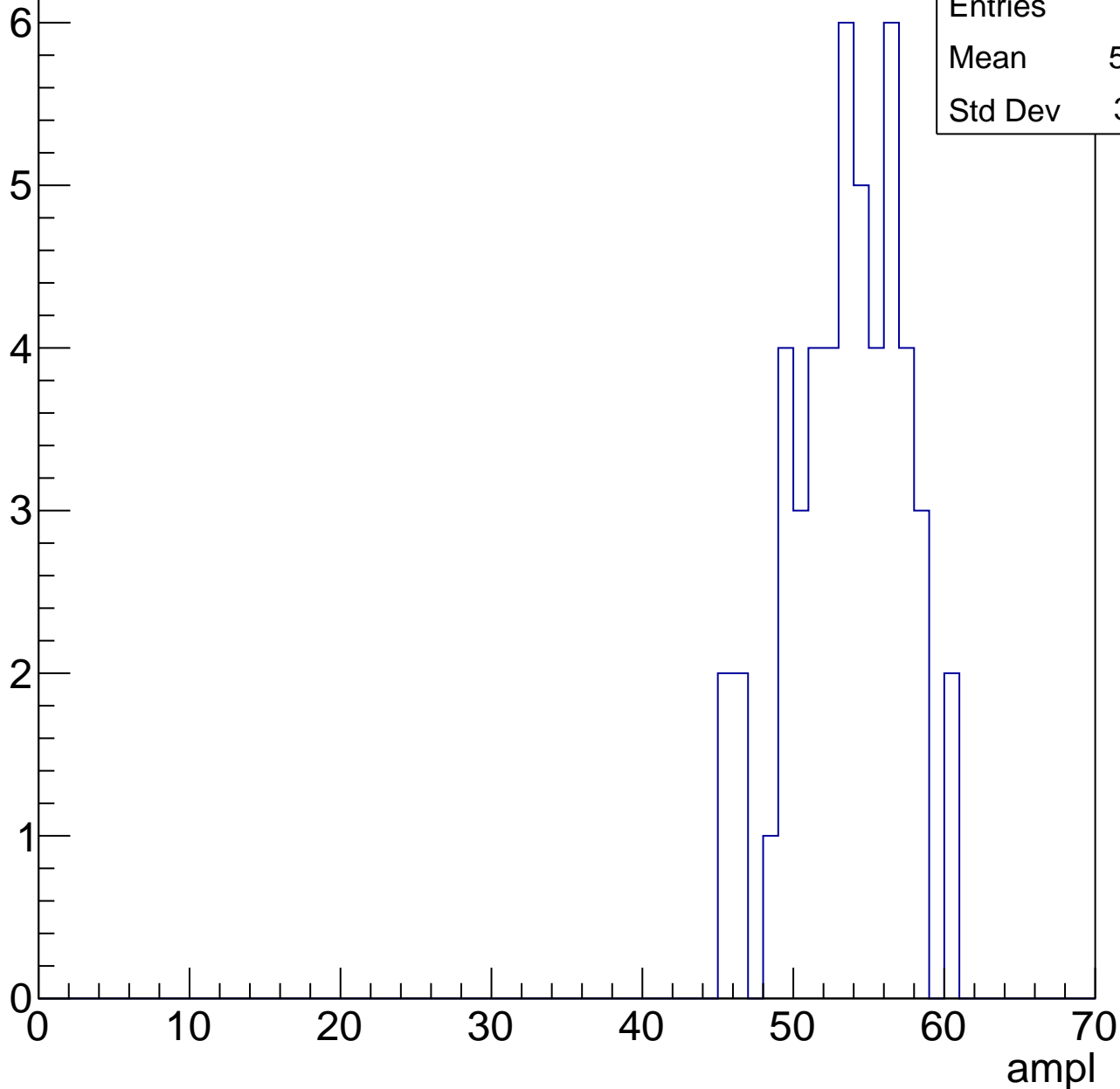


# B1L101S, U8-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	53.08
Std Dev	3.671

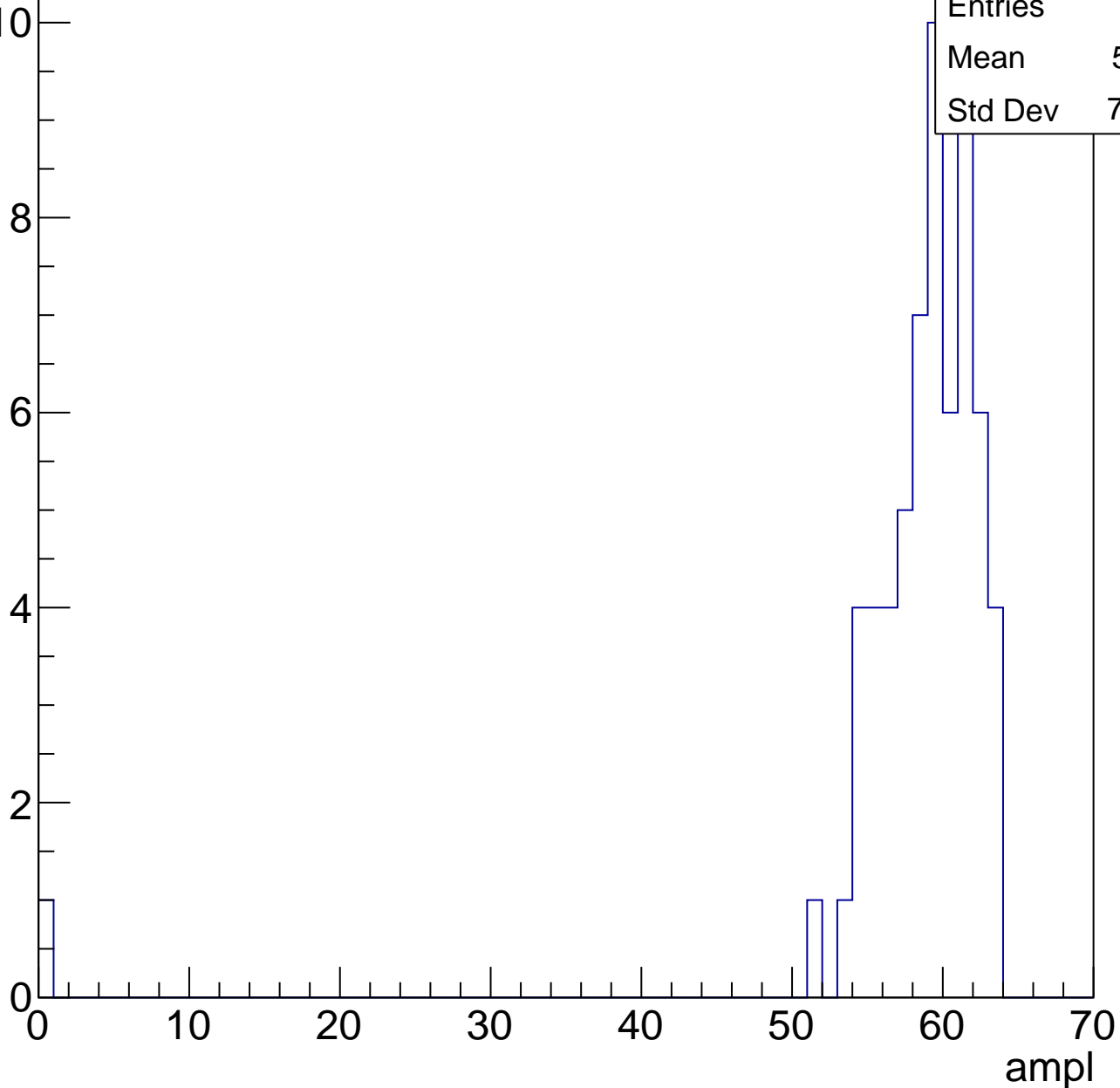


# B1L101S, U8-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	57.71
Std Dev	7.895

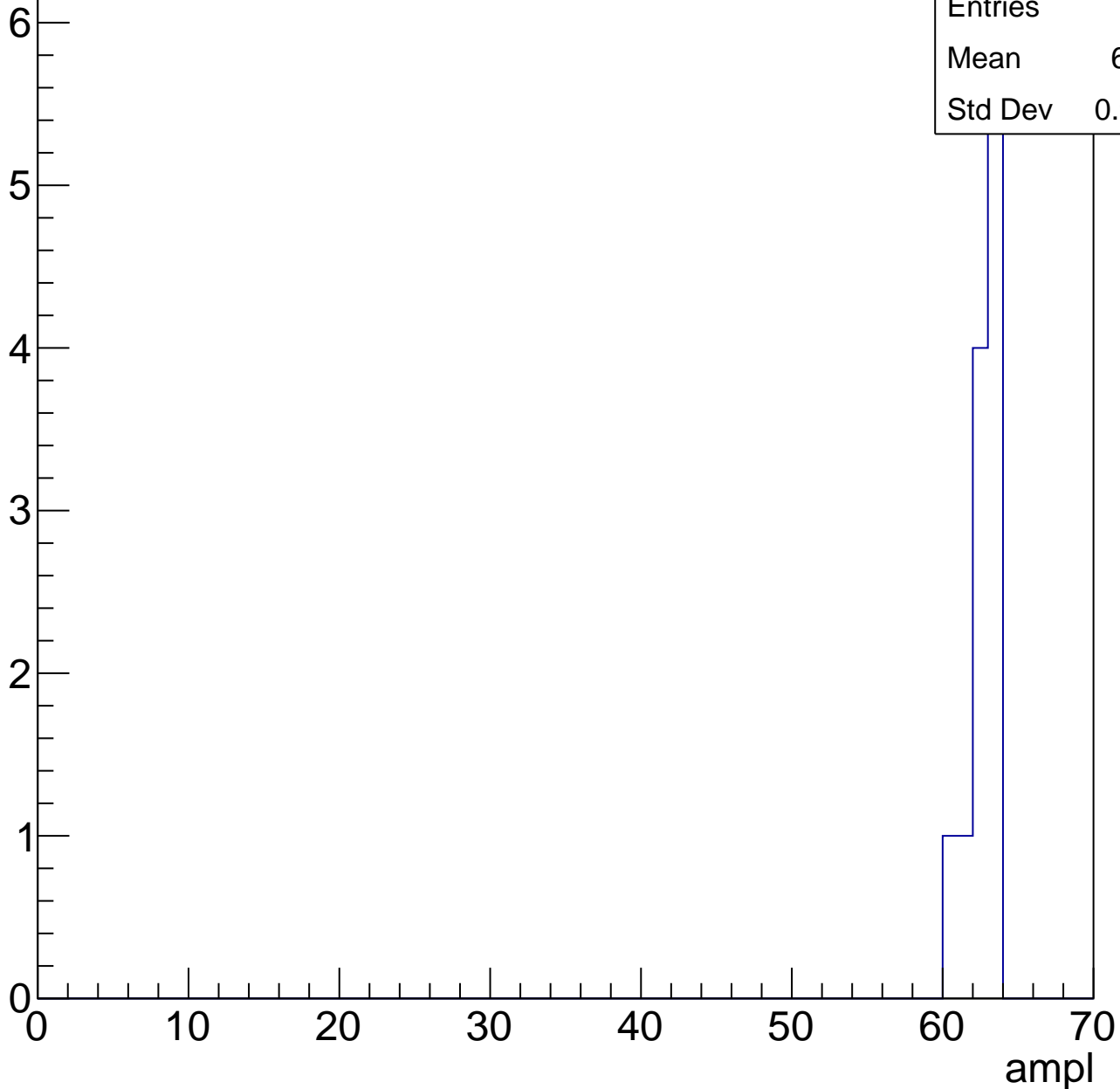


# B1L101S, U8-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	12
Mean	62.25
Std Dev	0.9242





# B1L101S, U8-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch117, adc0

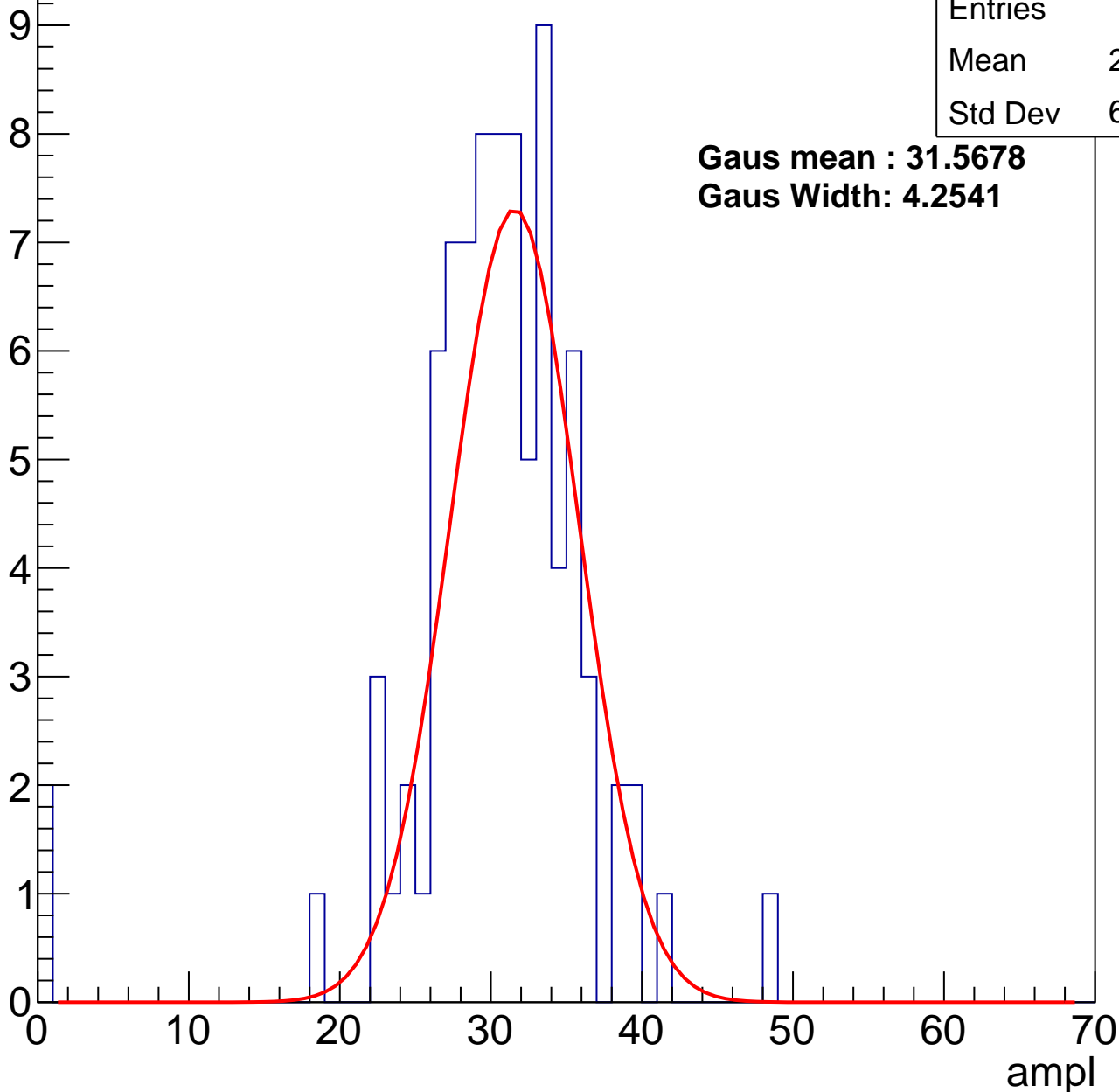
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	87
Mean	29.83
Std Dev	6.469

**Gaus mean : 31.5678**

**Gaus Width: 4.2541**



# B1L101S, U8-ch117, adc1

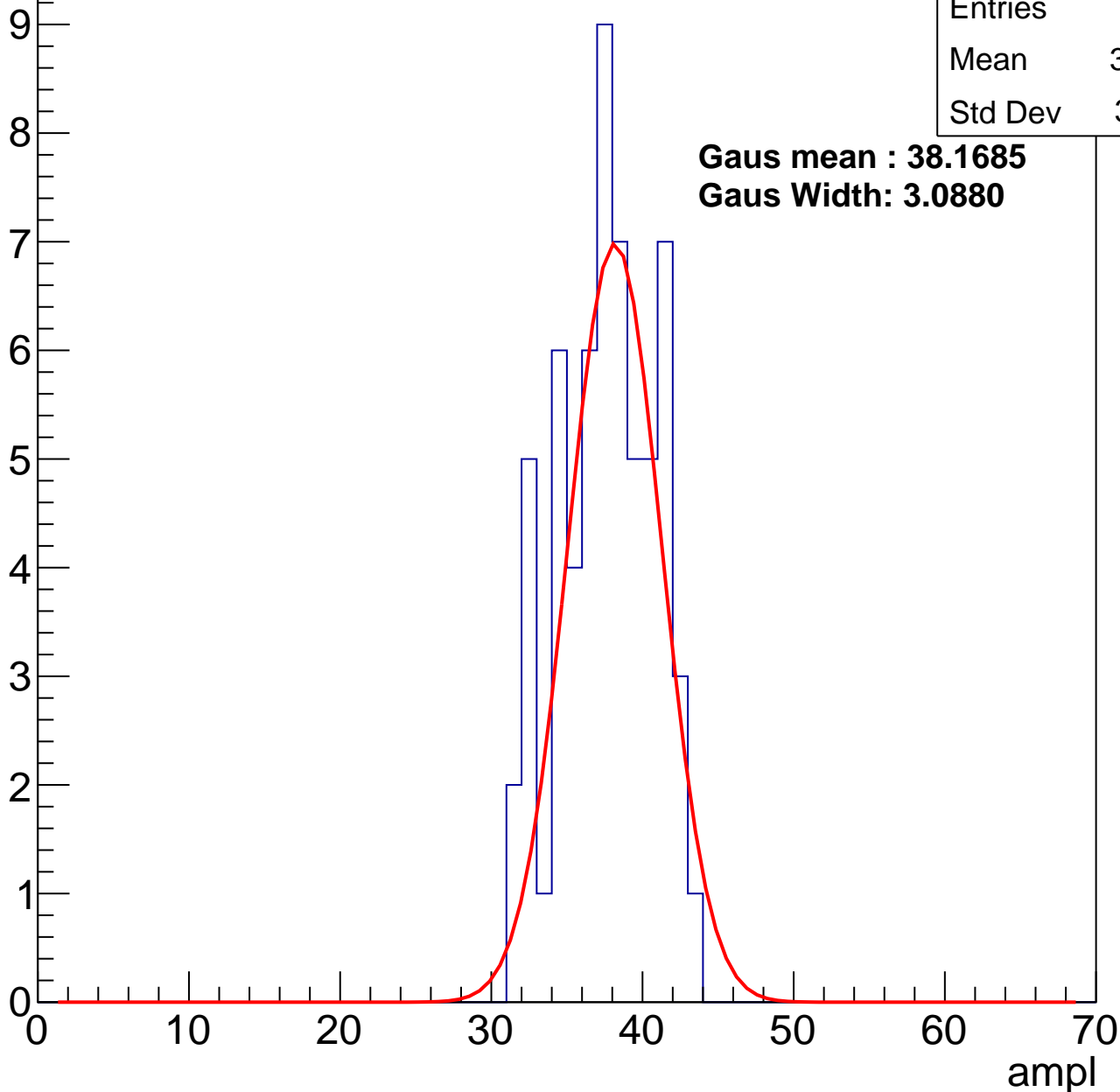
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	37.13
Std Dev	3.091

**Gaus mean : 38.1685**

**Gaus Width: 3.0880**



# B1L101S, U8-ch117, adc2

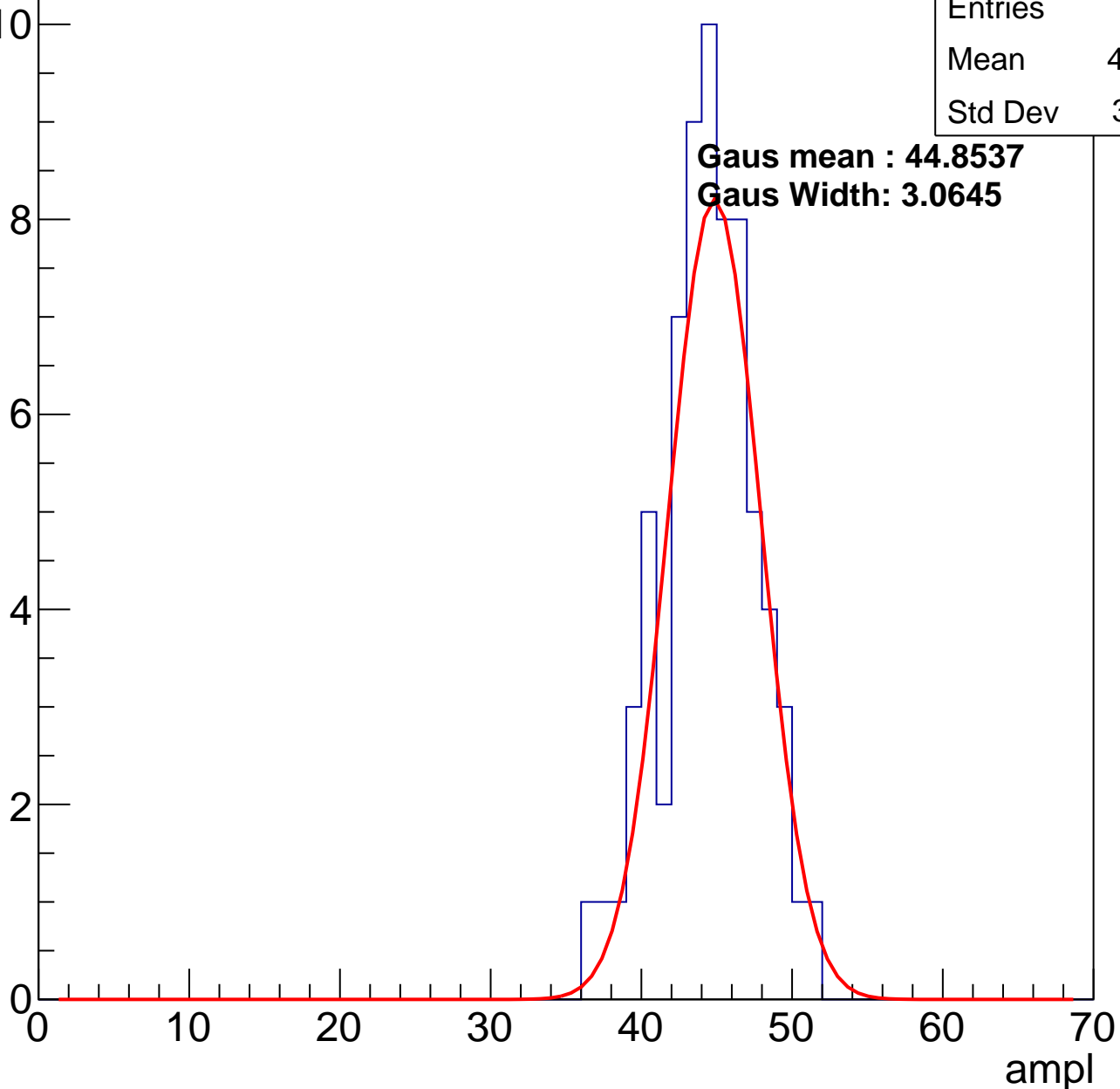
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	43.97
Std Dev	3.111

**Gaus mean : 44.8537**

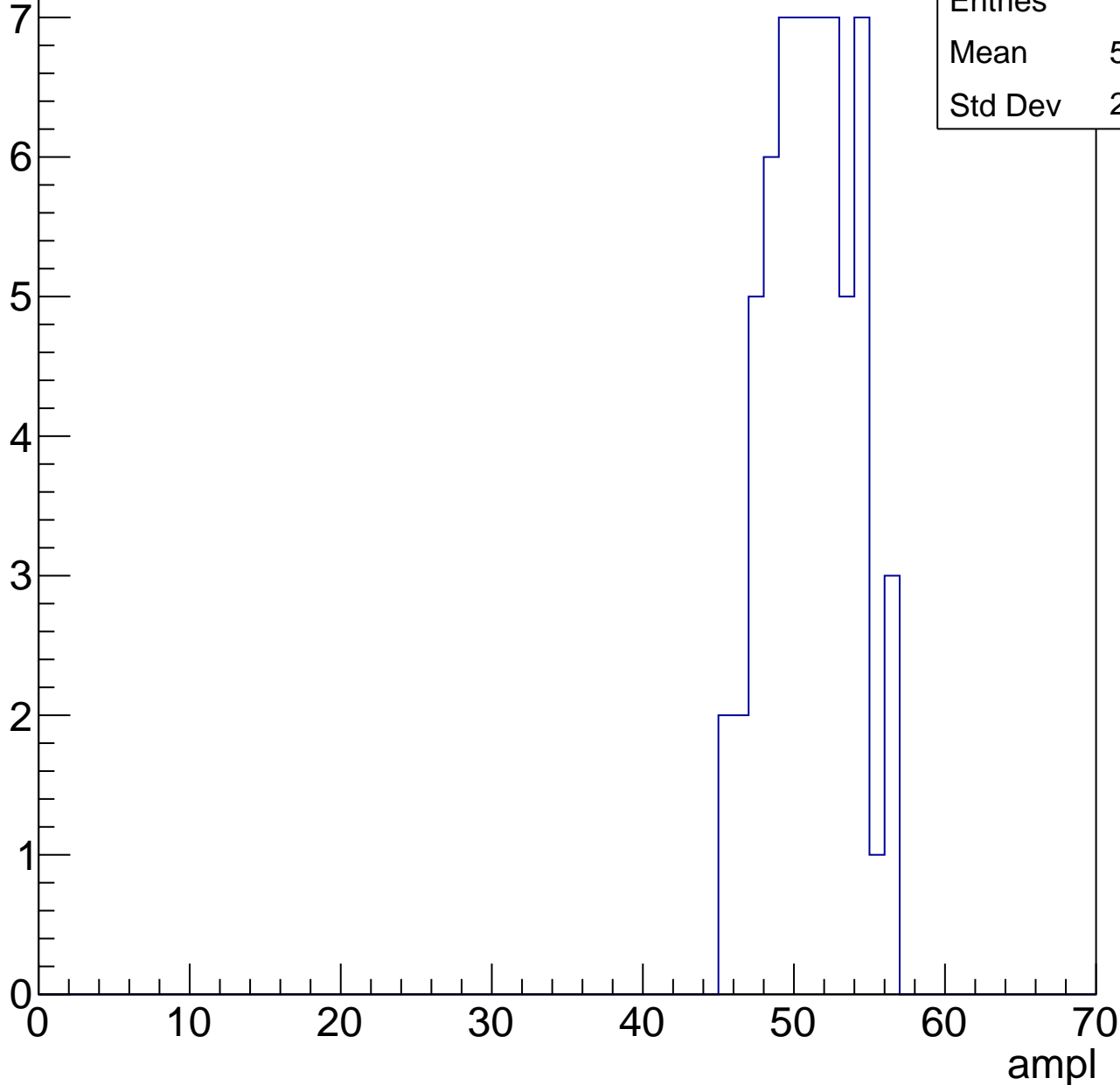
**Gaus Width: 3.0645**



# B1L101S, U8-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



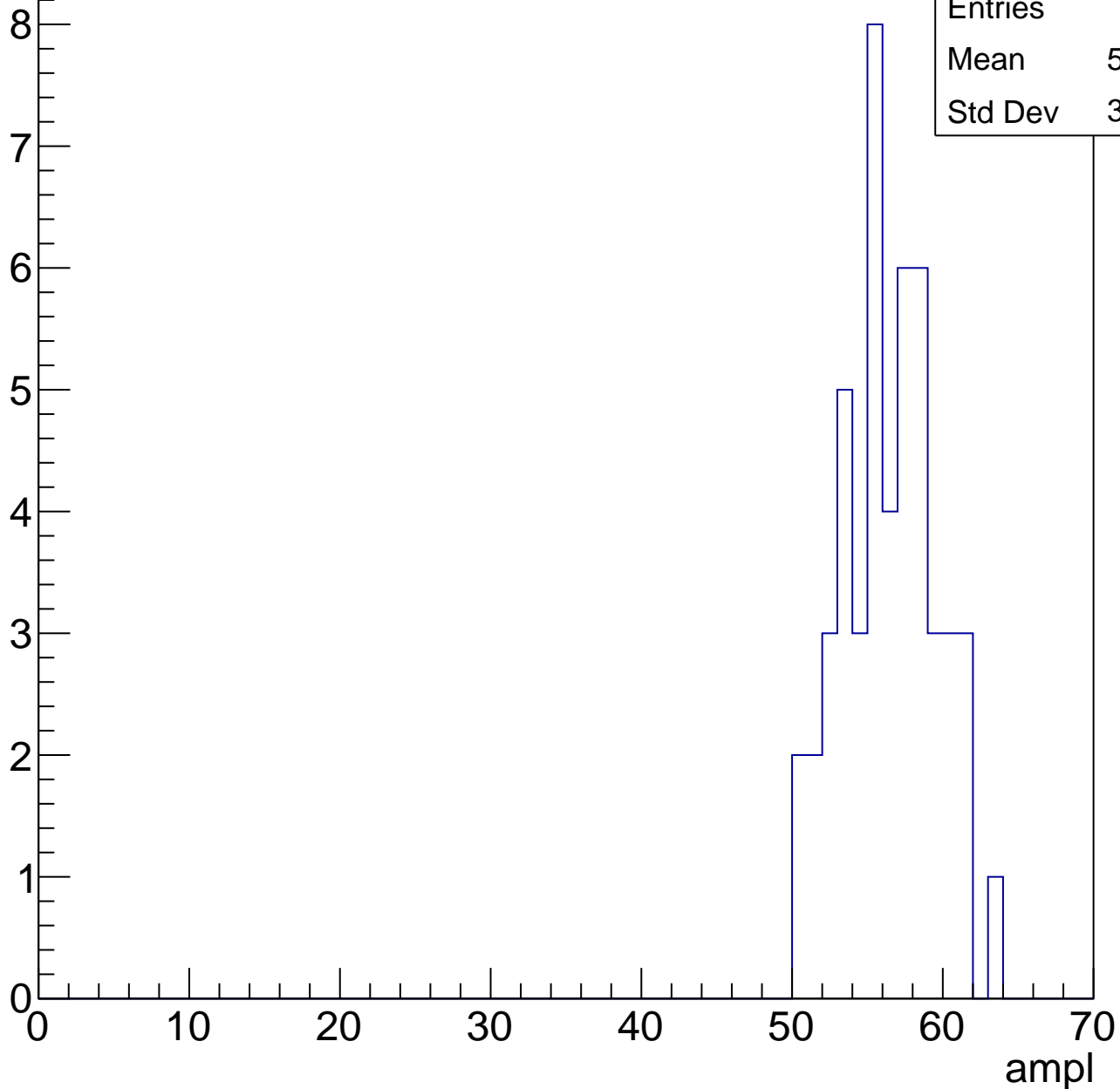
Entries	59
Mean	50.59
Std Dev	2.799

# B1L101S, U8-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	55.96
Std Dev	3.077

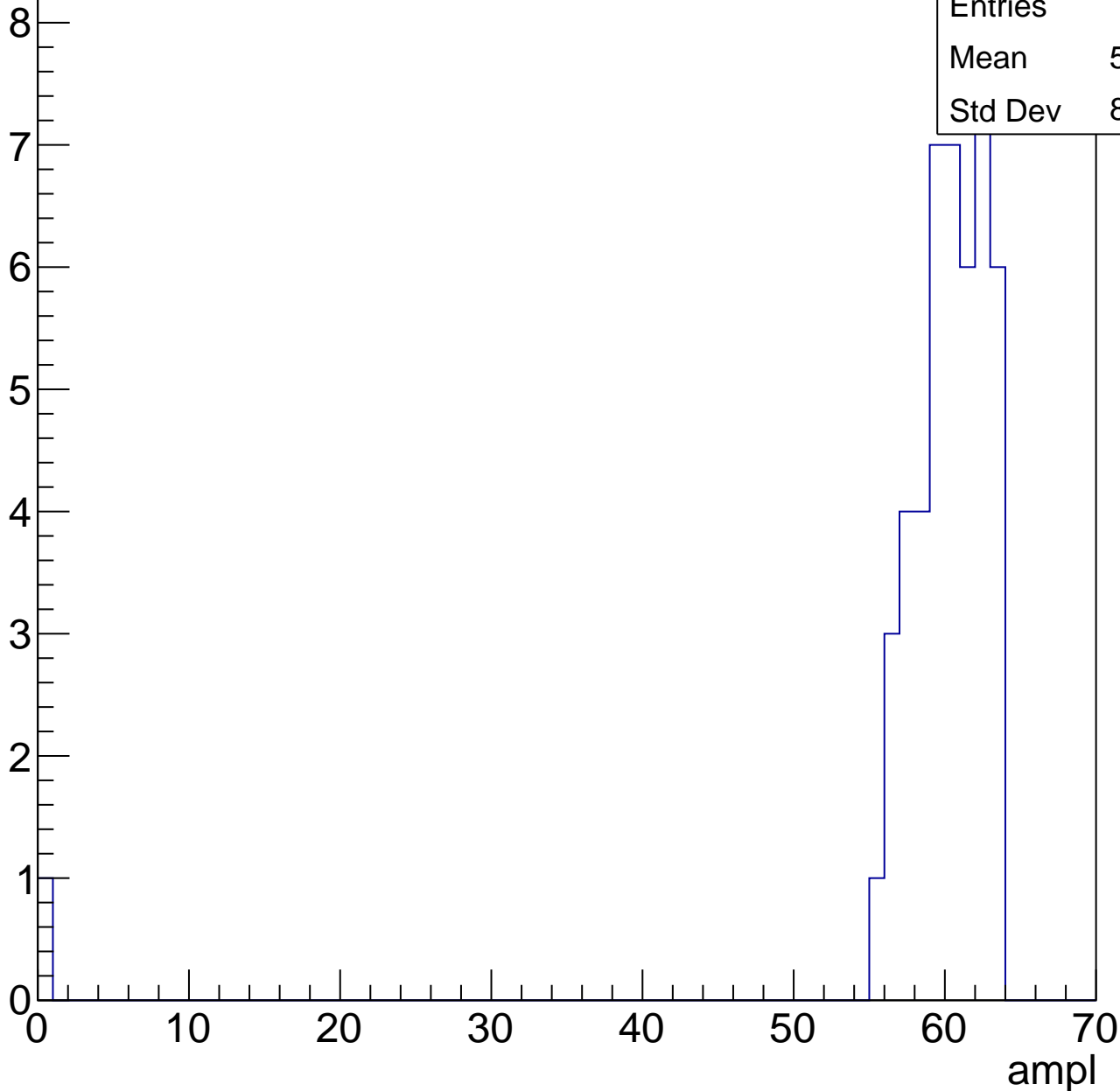


# B1L101S, U8-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	58.64
Std Dev	8.917



# B1L101S, U8-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U8-ch118, adc0

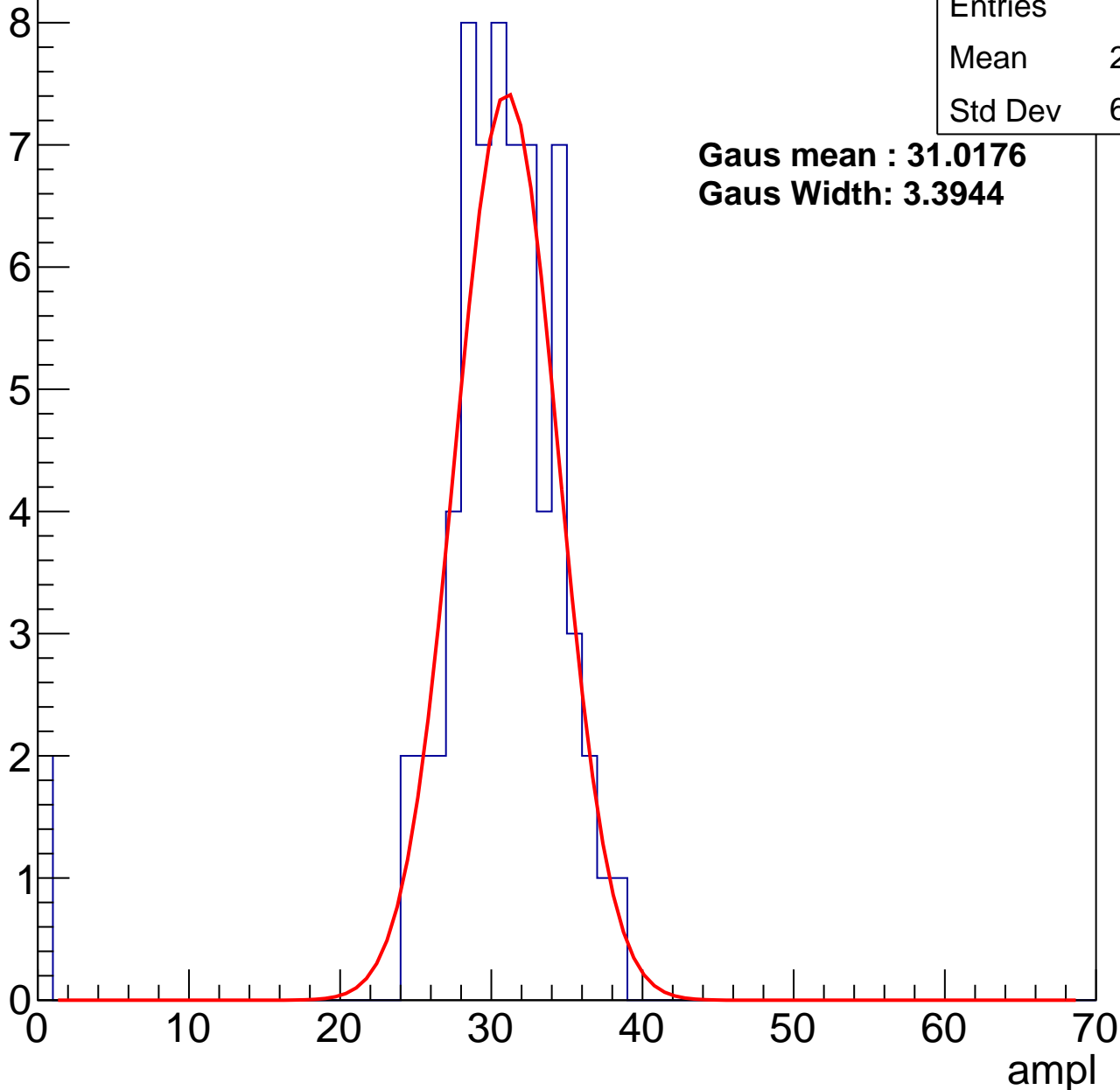
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	29.67
Std Dev	6.065

**Gaus mean : 31.0176**

**Gaus Width: 3.3944**



# B1L101S, U8-ch118, adc1

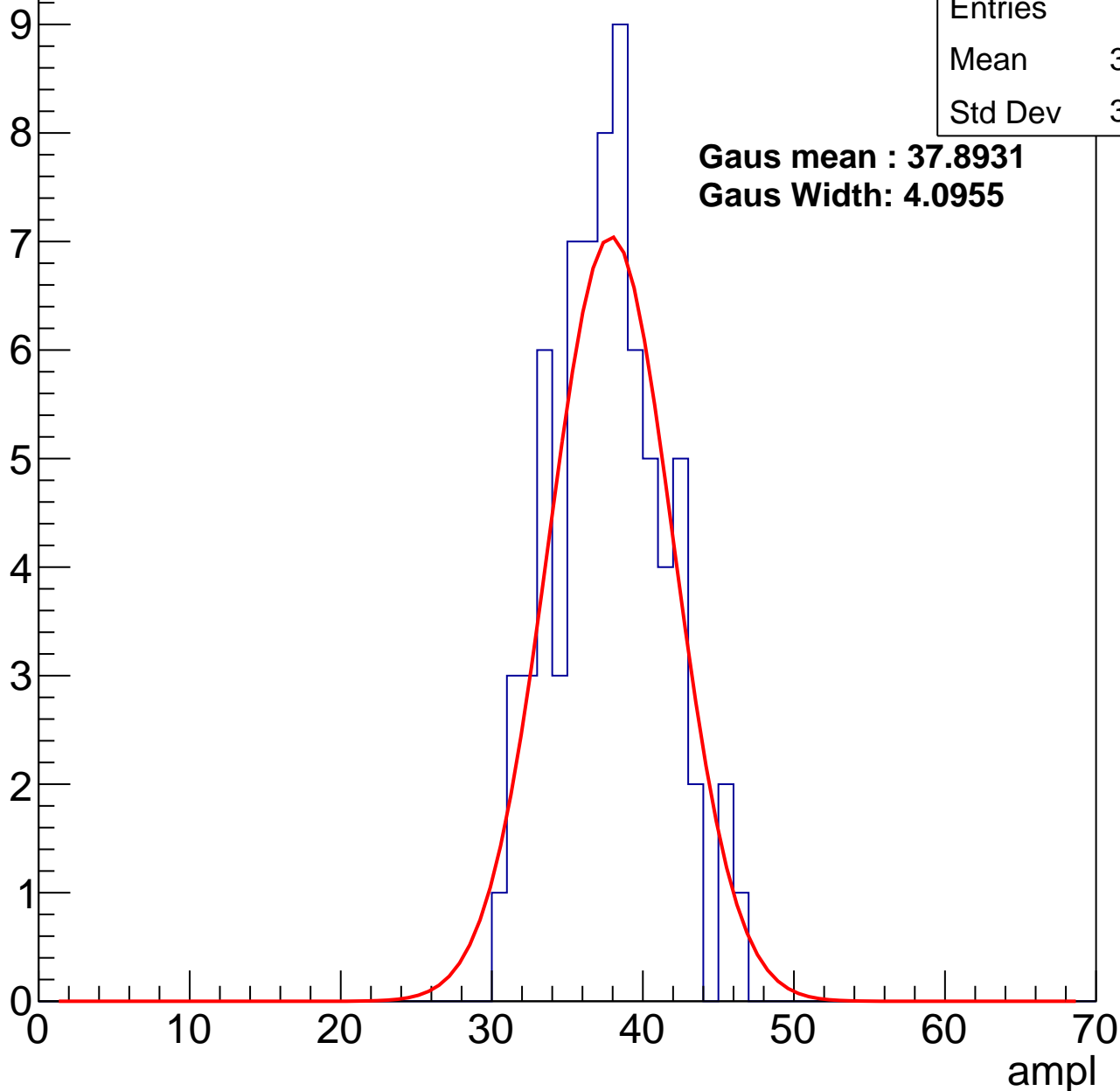
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	37.28
Std Dev	3.599

**Gaus mean : 37.8931**

**Gaus Width: 4.0955**



# B1L101S, U8-ch118, adc2

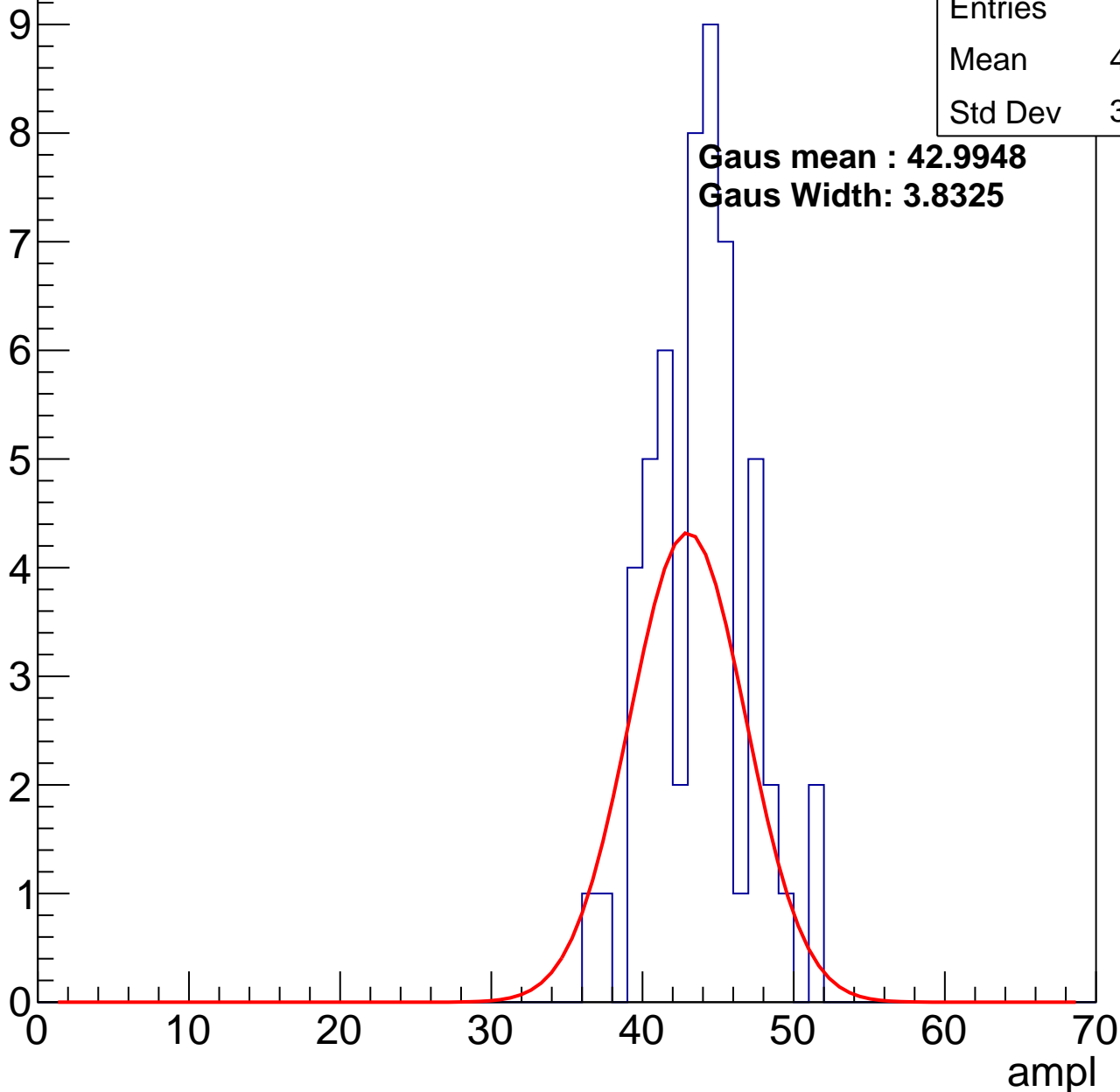
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	43.37
Std Dev	3.199

**Gaus mean : 42.9948**

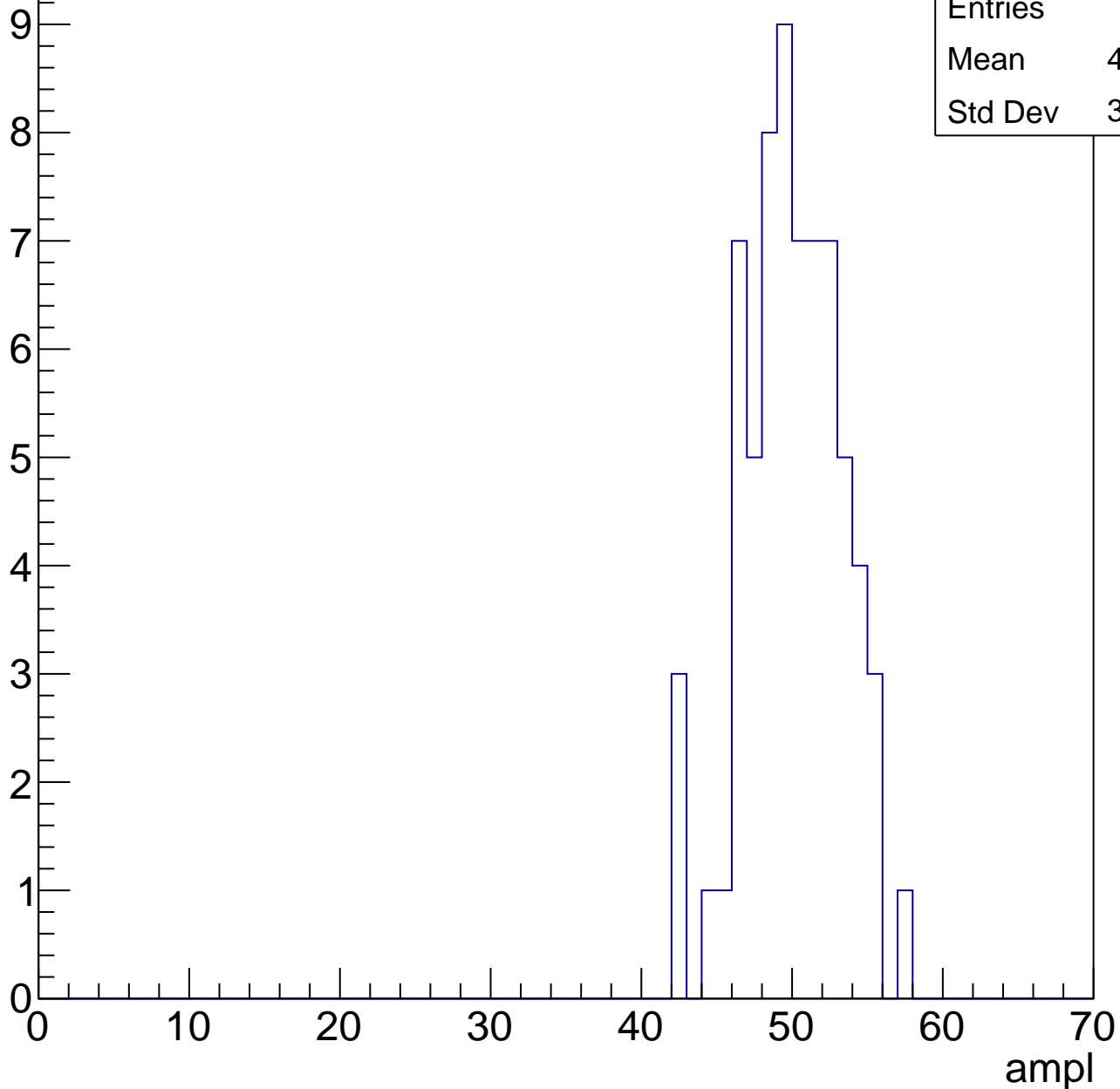
**Gaus Width: 3.8325**



# B1L101S, U8-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



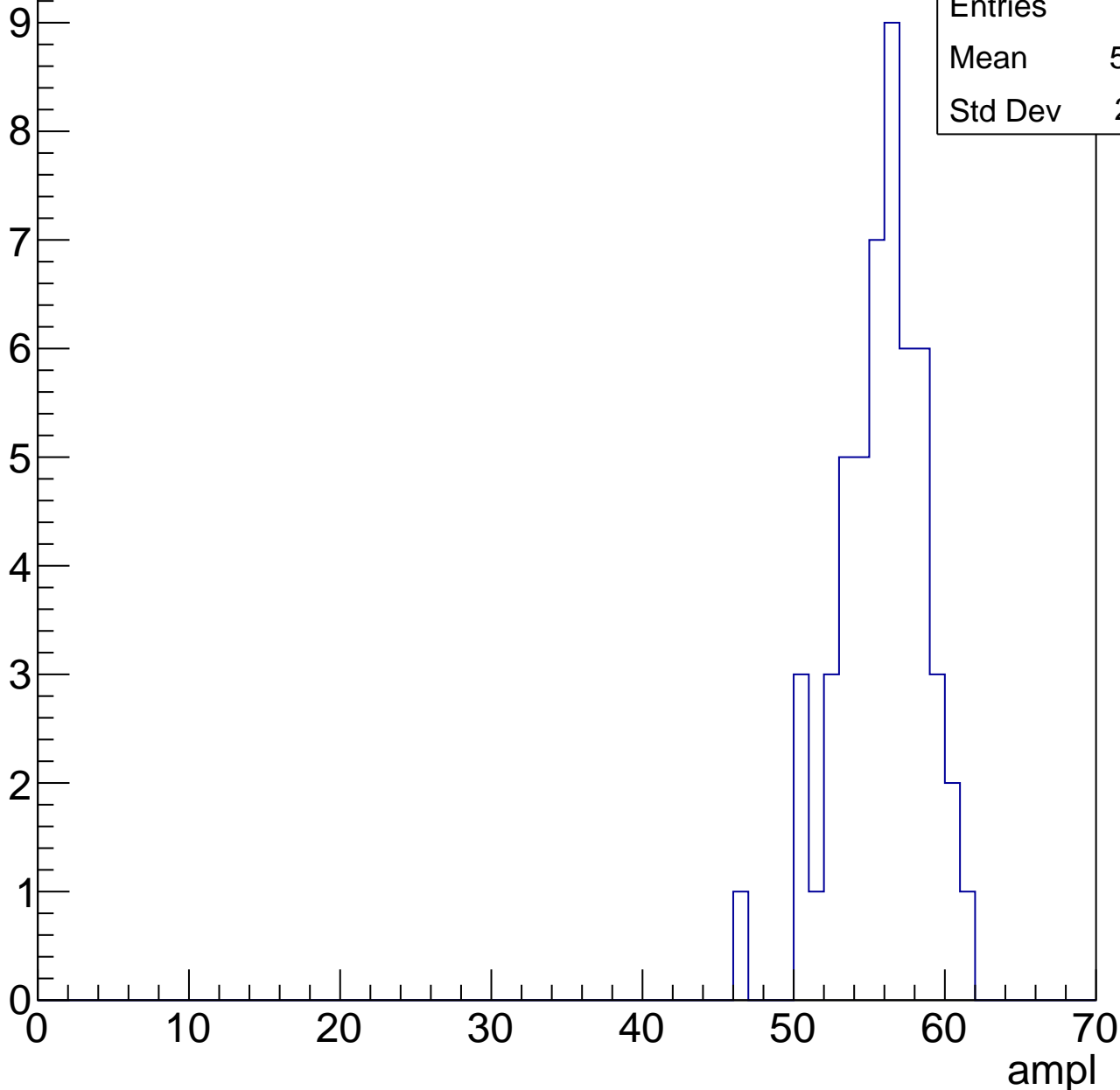
Entries	68
Mean	49.57
Std Dev	3.224

# B1L101S, U8-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	55.29
Std Dev	2.911

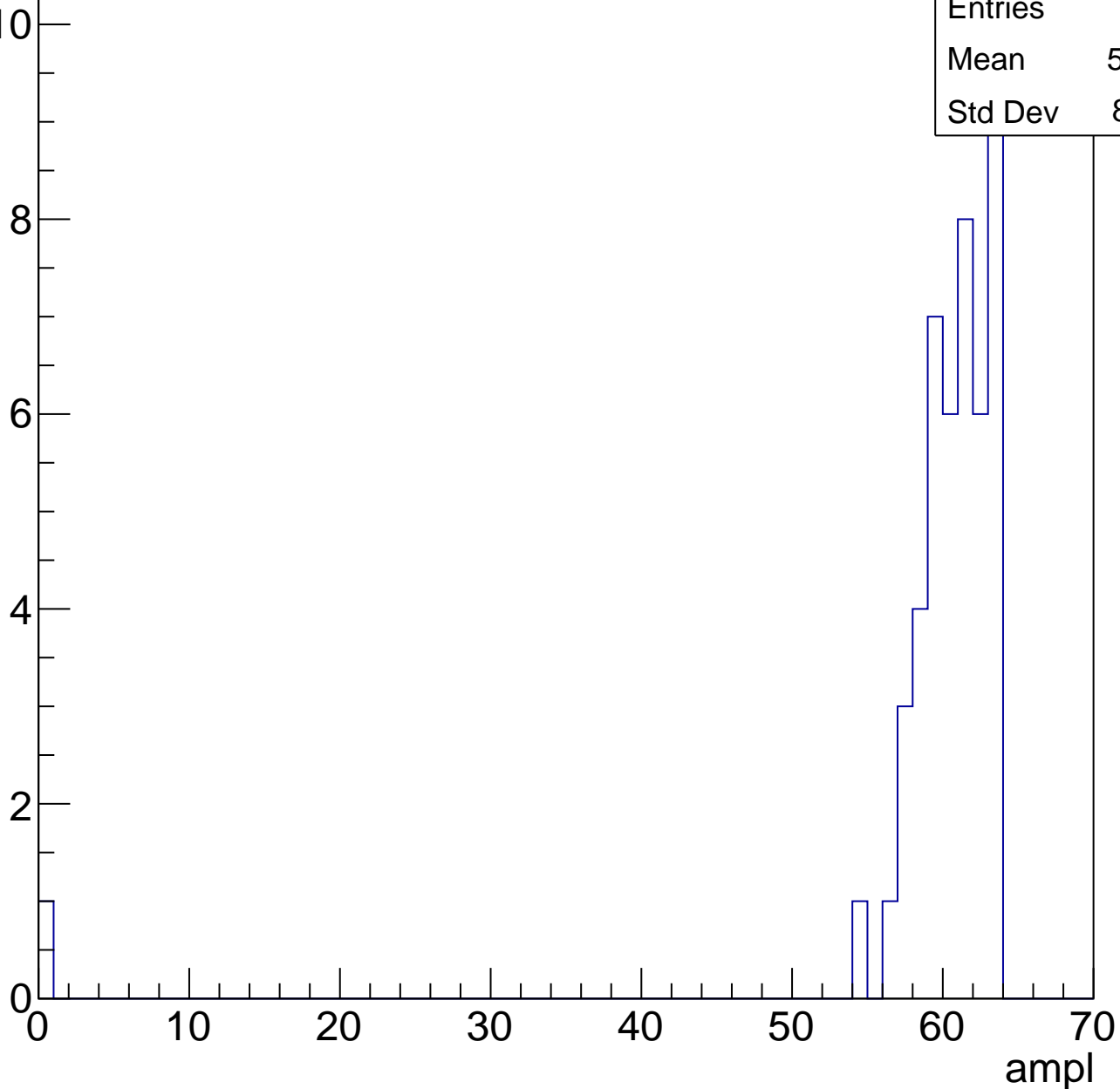


# B1L101S, U8-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

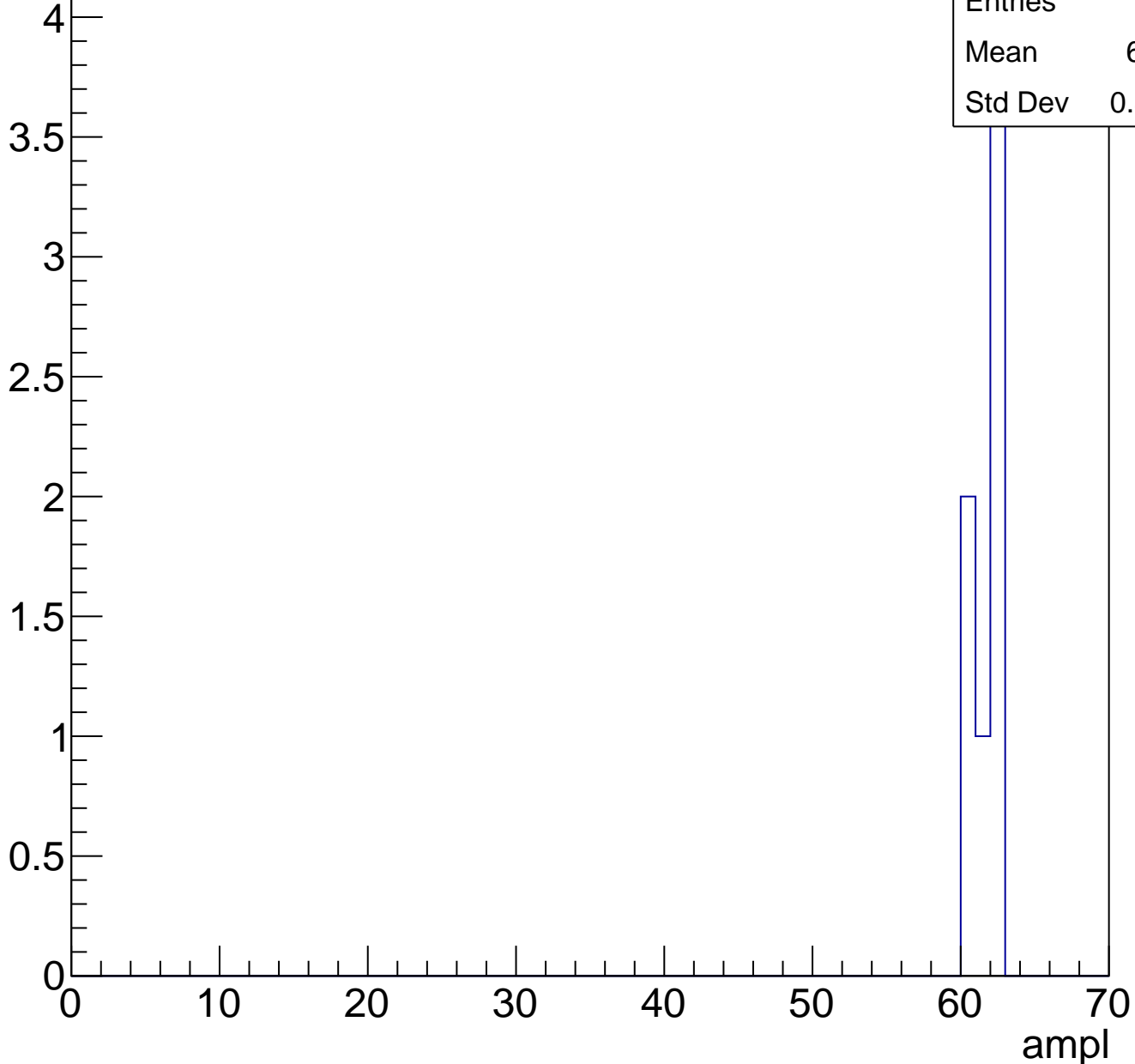
Entries	47
Mean	59.06
Std Dev	8.971



# B1L101S, U8-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U8-ch119, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	83
Mean	30.16
Std Dev	6.013

**Gaus mean : 31.7657**

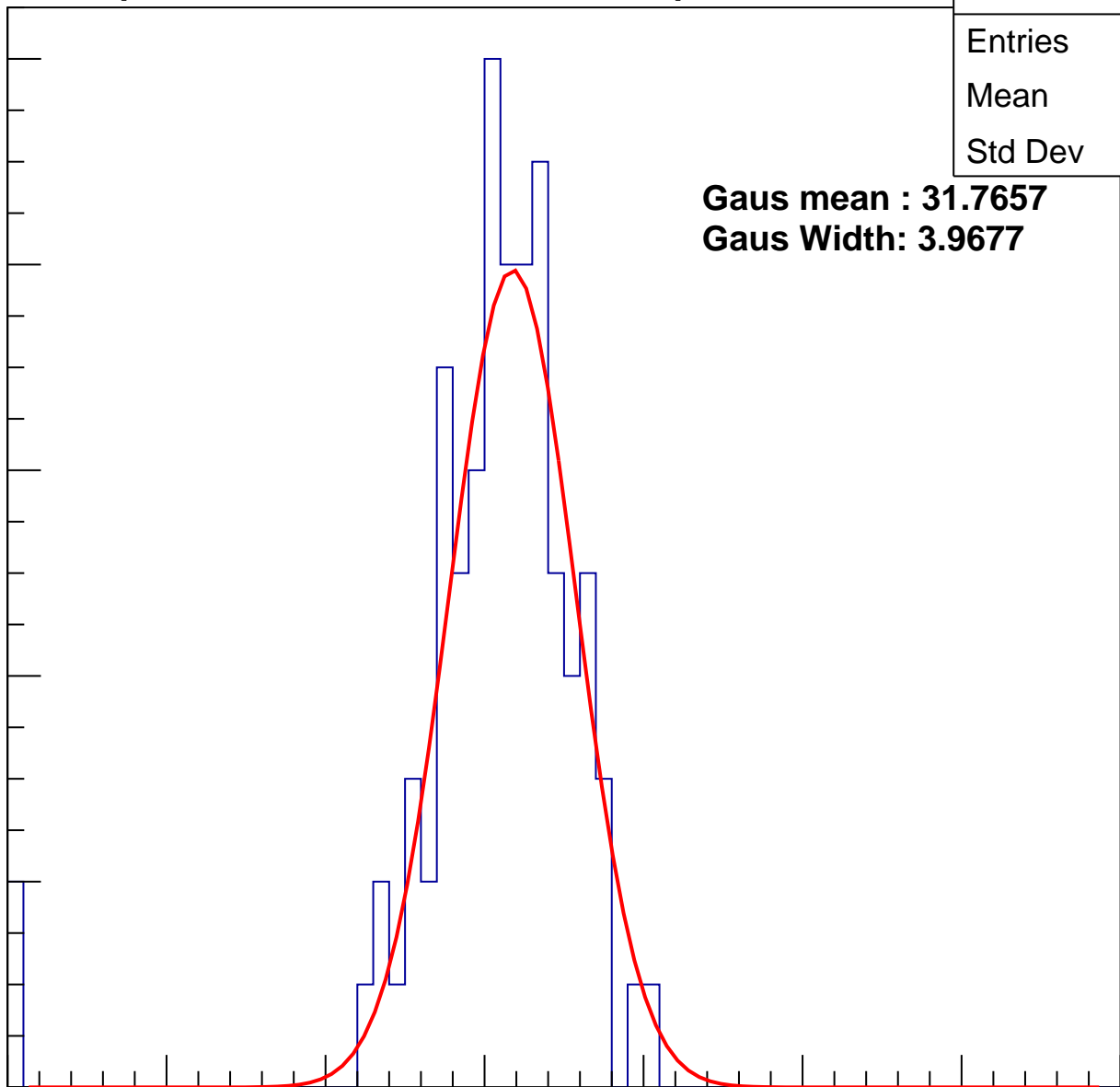
**Gaus Width: 3.9677**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U8-ch119, adc1

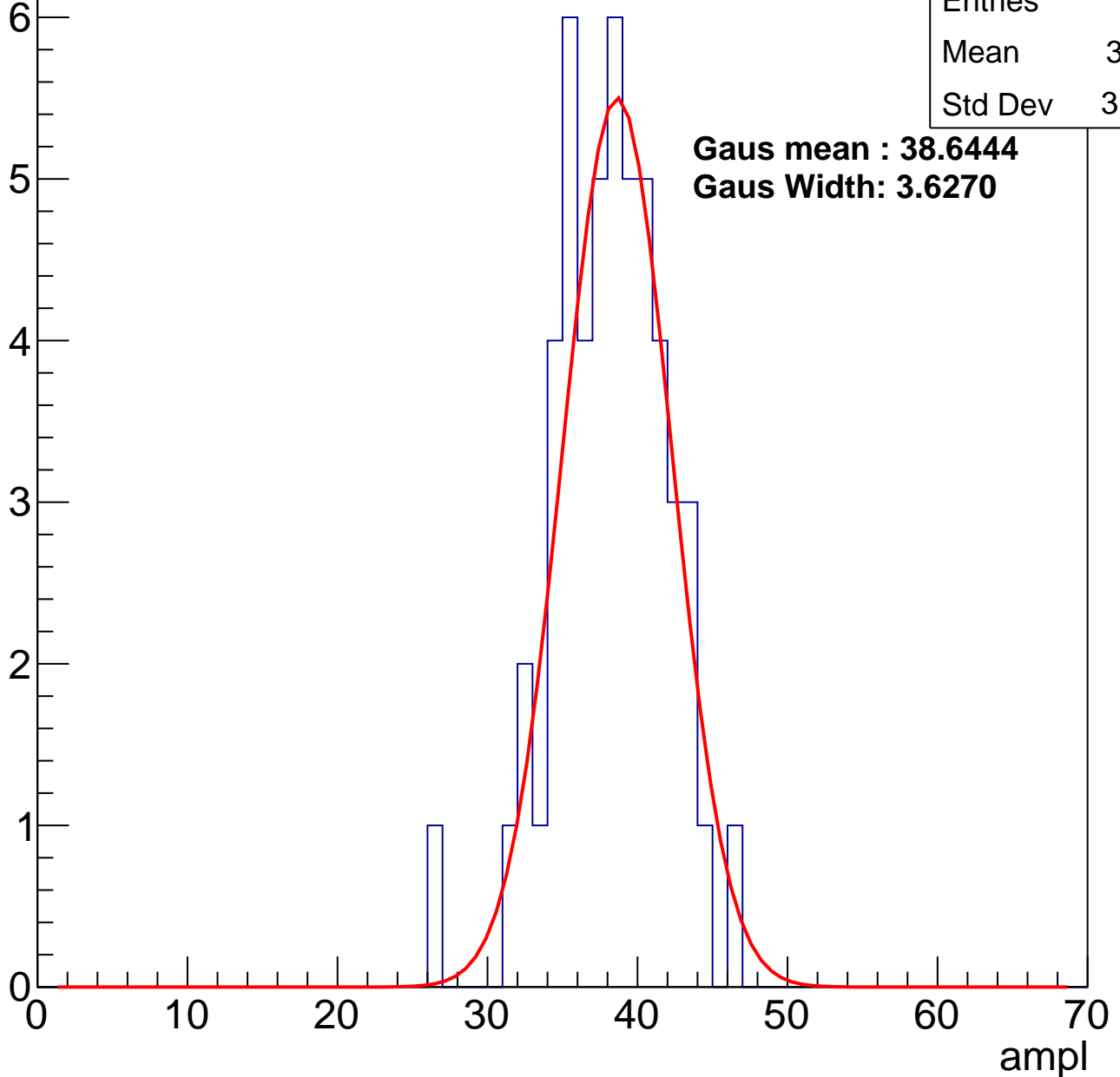
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	37.71
Std Dev	3.692

**Gaus mean : 38.6444**

**Gaus Width: 3.6270**



# B1L101S, U8-ch119, adc2

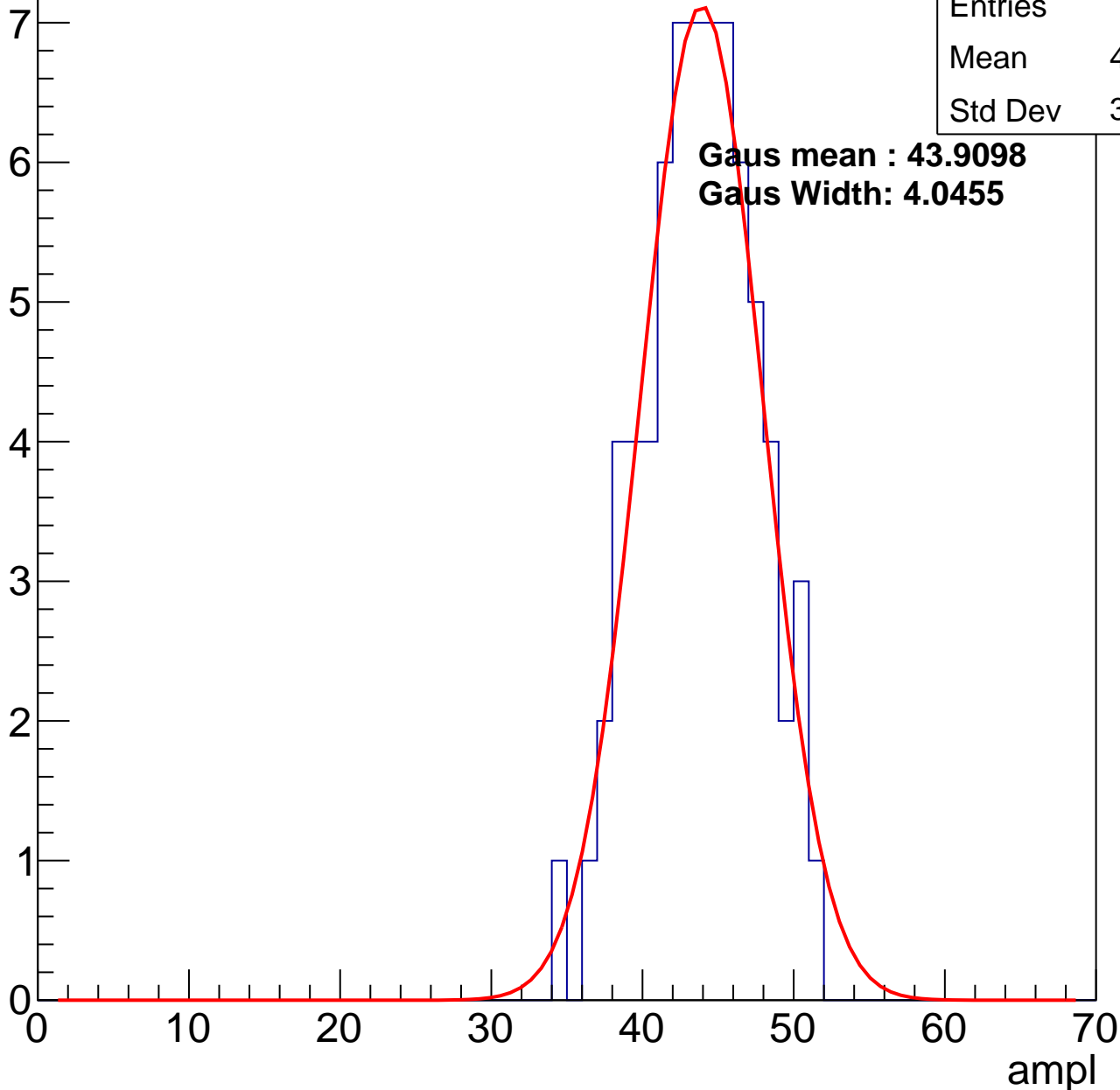
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	43.35
Std Dev	3.708

**Gaus mean : 43.9098**

**Gaus Width: 4.0455**

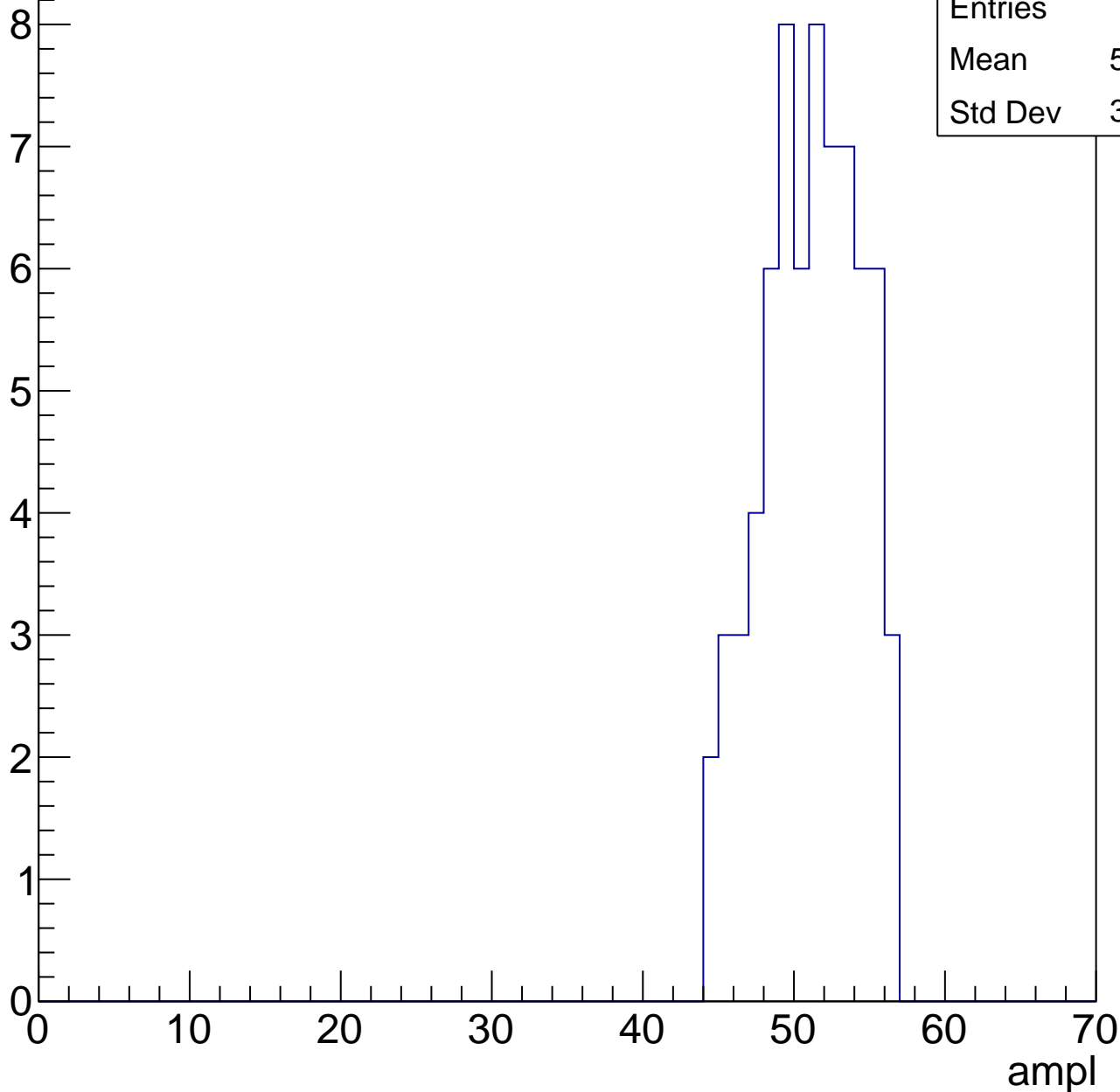


# B1L101S, U8-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

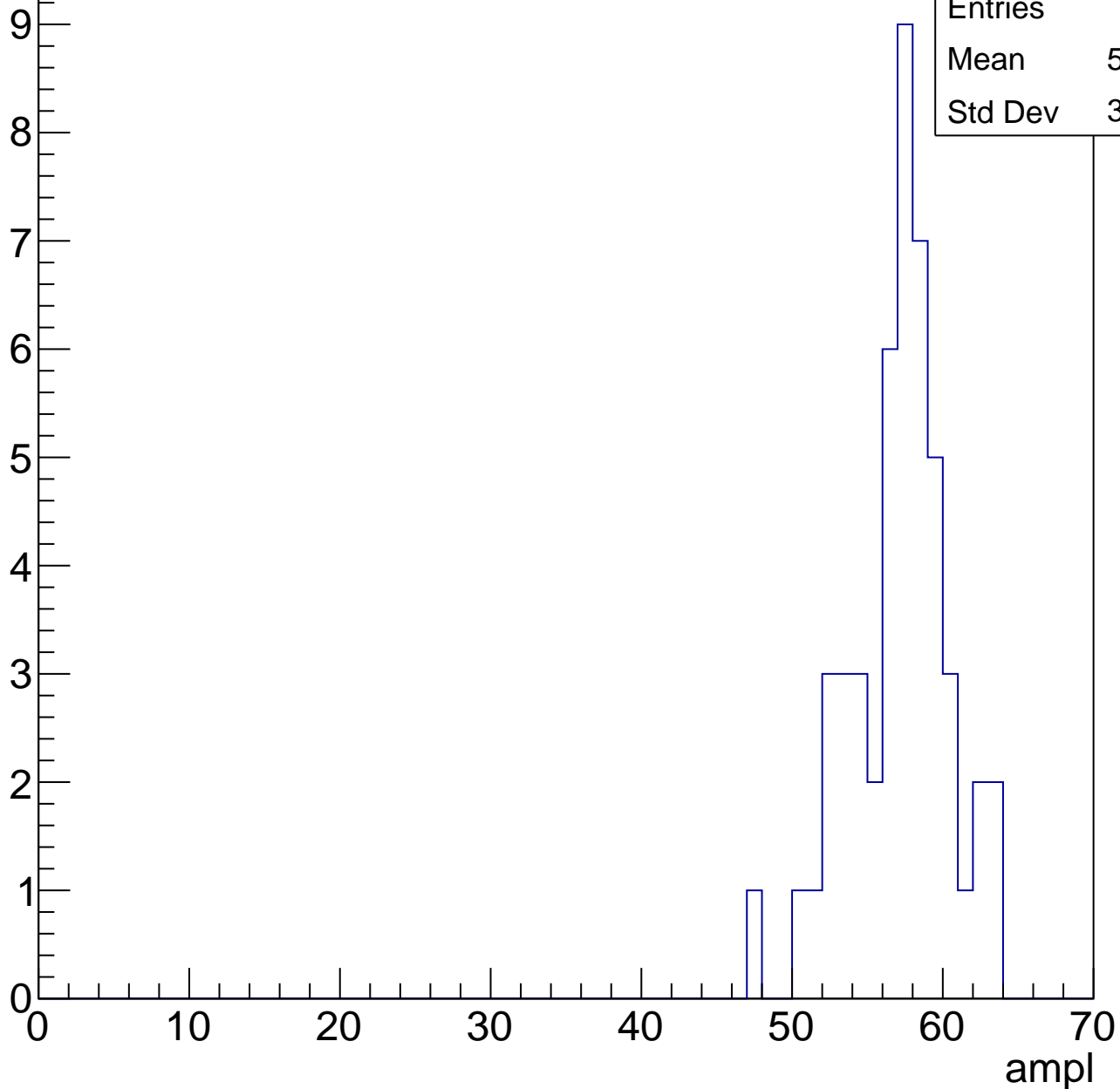
Entries	69
Mean	50.64
Std Dev	3.158



# B1L101S, U8-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

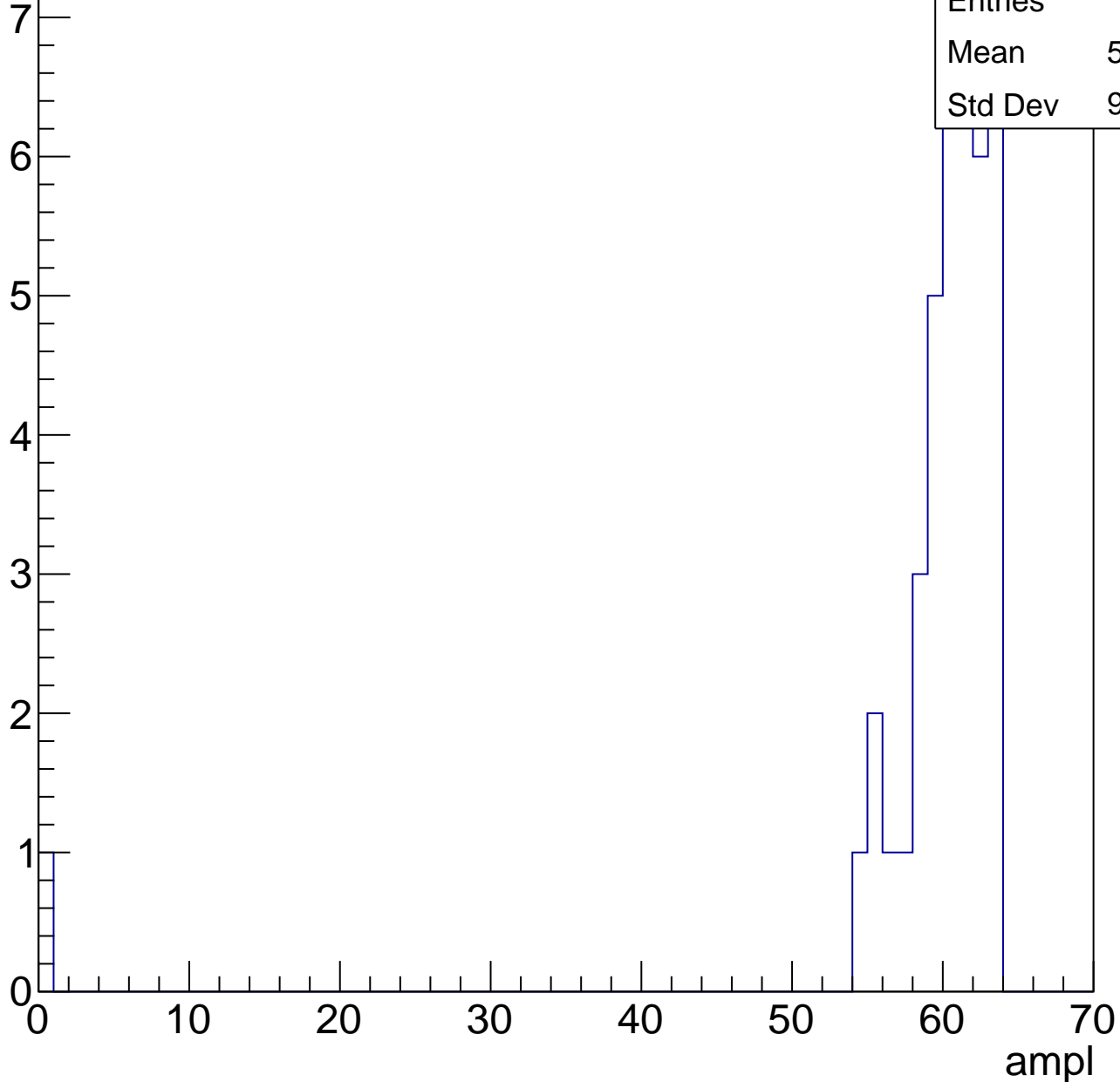
Entry



# B1L101S, U8-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.8
Std Dev	0.7483

ampl

0 10 20 30 40 50 60 70



# B1L101S, U8-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	22
Std Dev	0

# B1L101S, U8-ch120, adc0

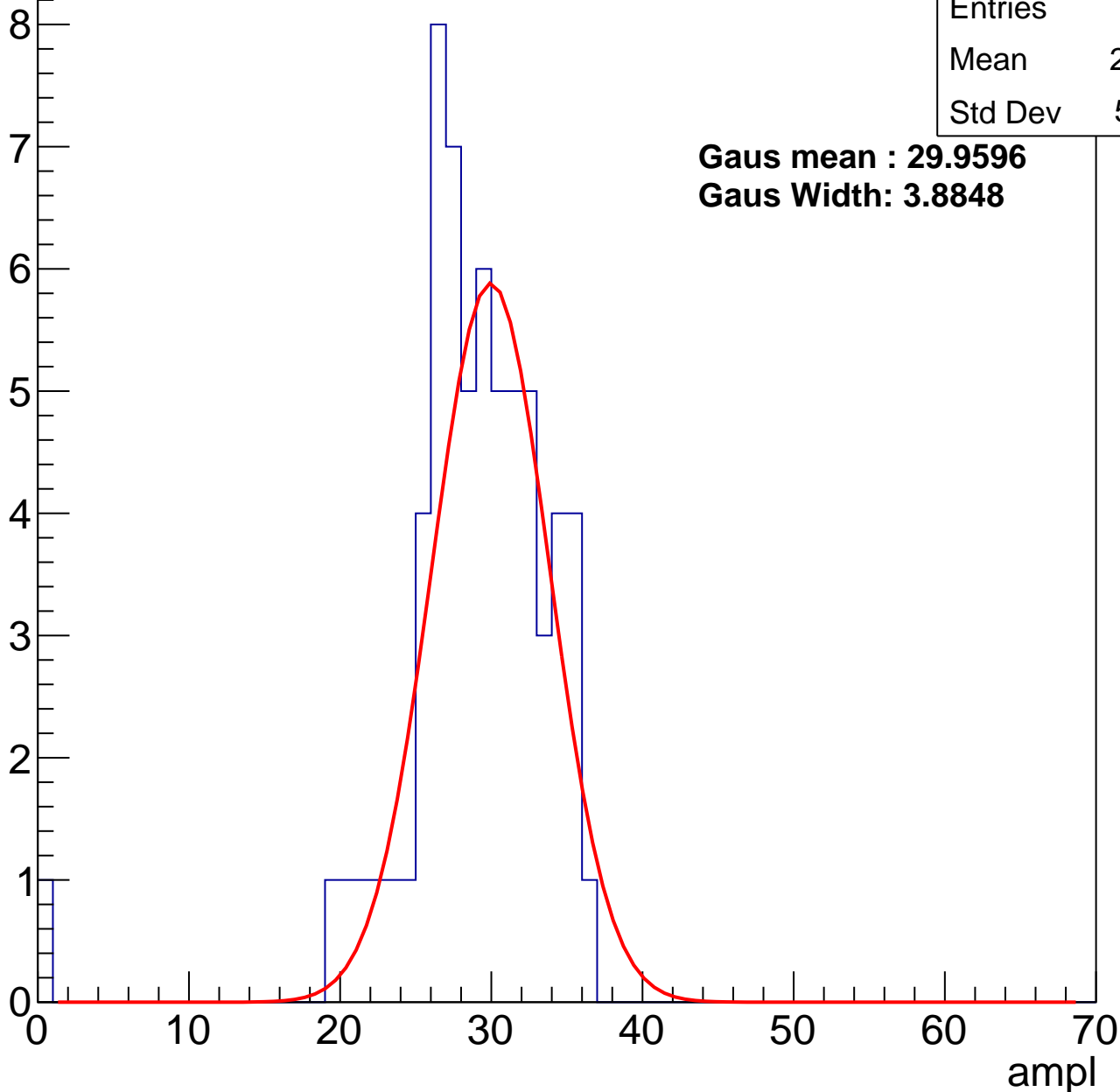
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	28.38
Std Dev	5.231

**Gaus mean : 29.9596**

**Gaus Width: 3.8848**



# B1L101S, U8-ch120, adc1

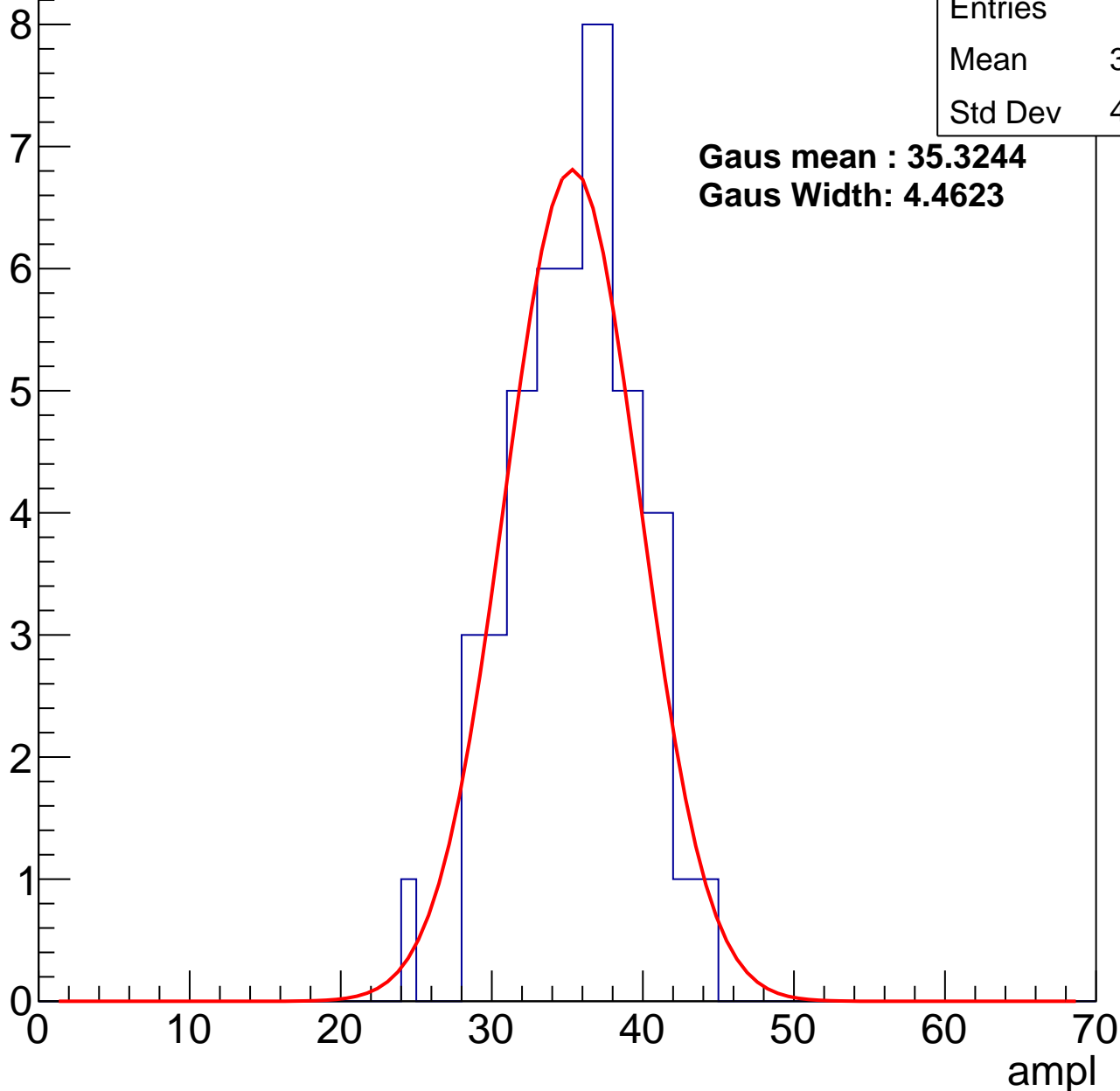
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	35.12
Std Dev	4.013

**Gaus mean : 35.3244**

**Gaus Width: 4.4623**



# B1L101S, U8-ch120, adc2

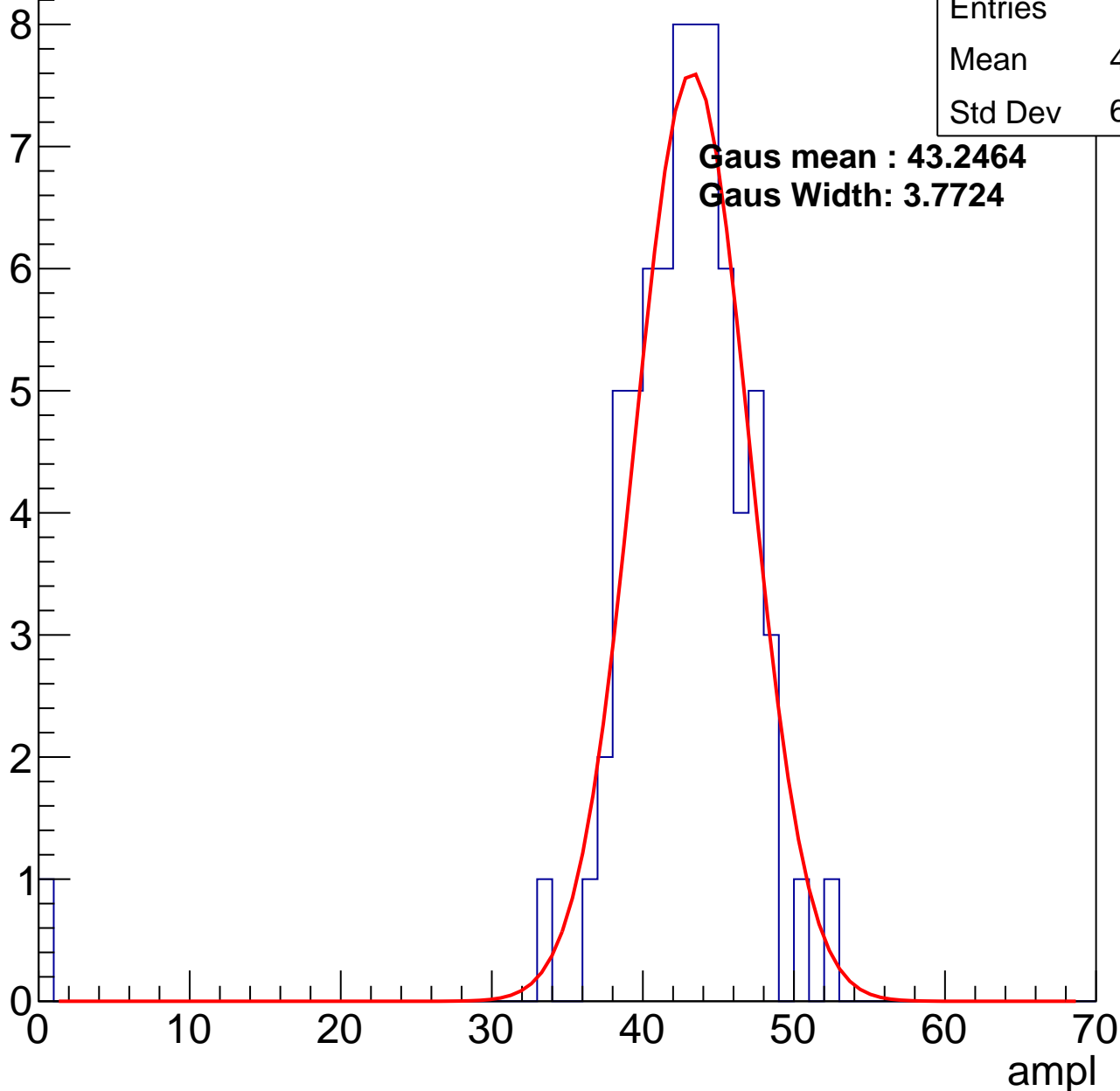
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	41.99
Std Dev	6.099

**Gaus mean : 43.2464**

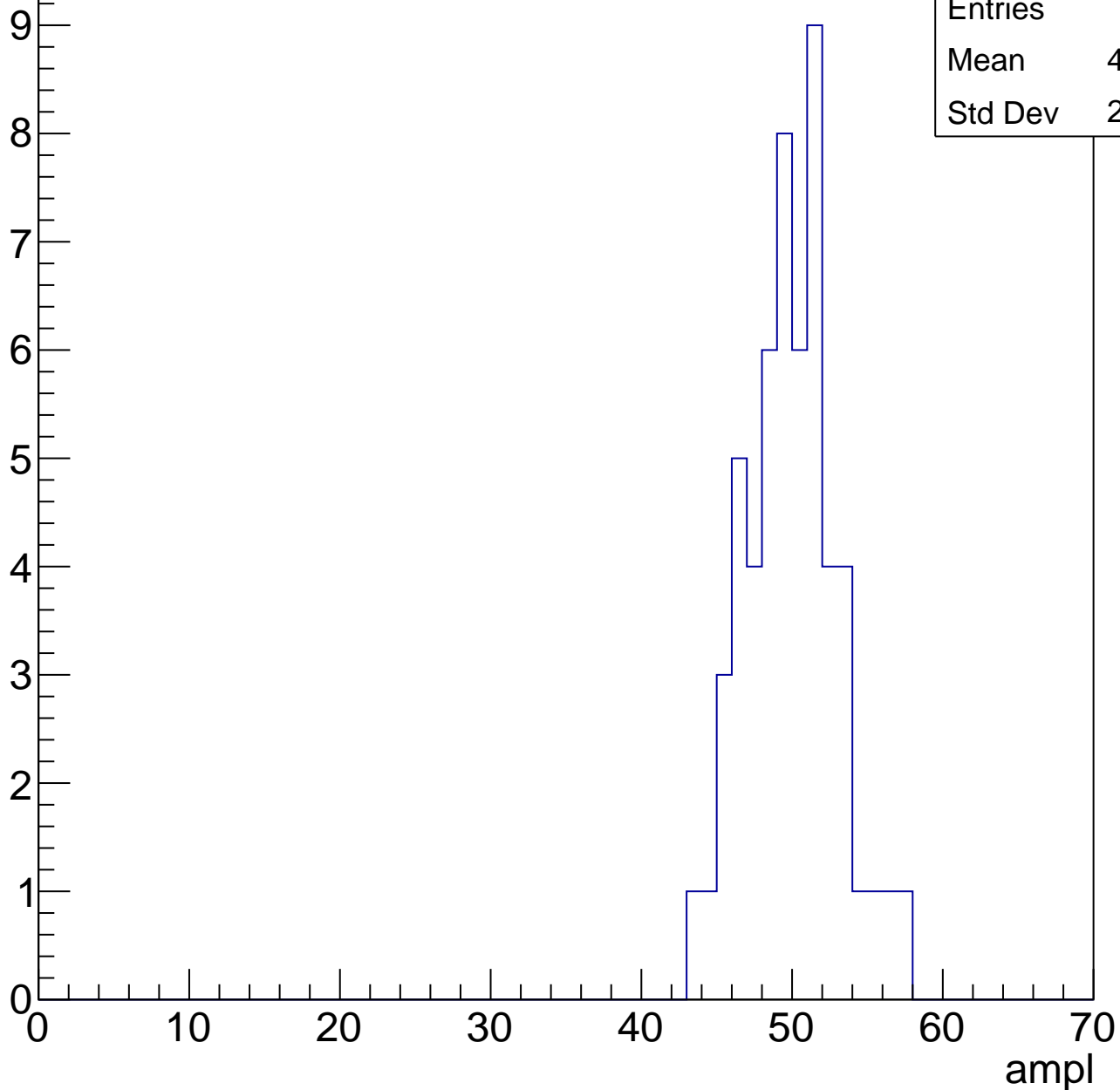
**Gaus Width: 3.7724**



# B1L101S, U8-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

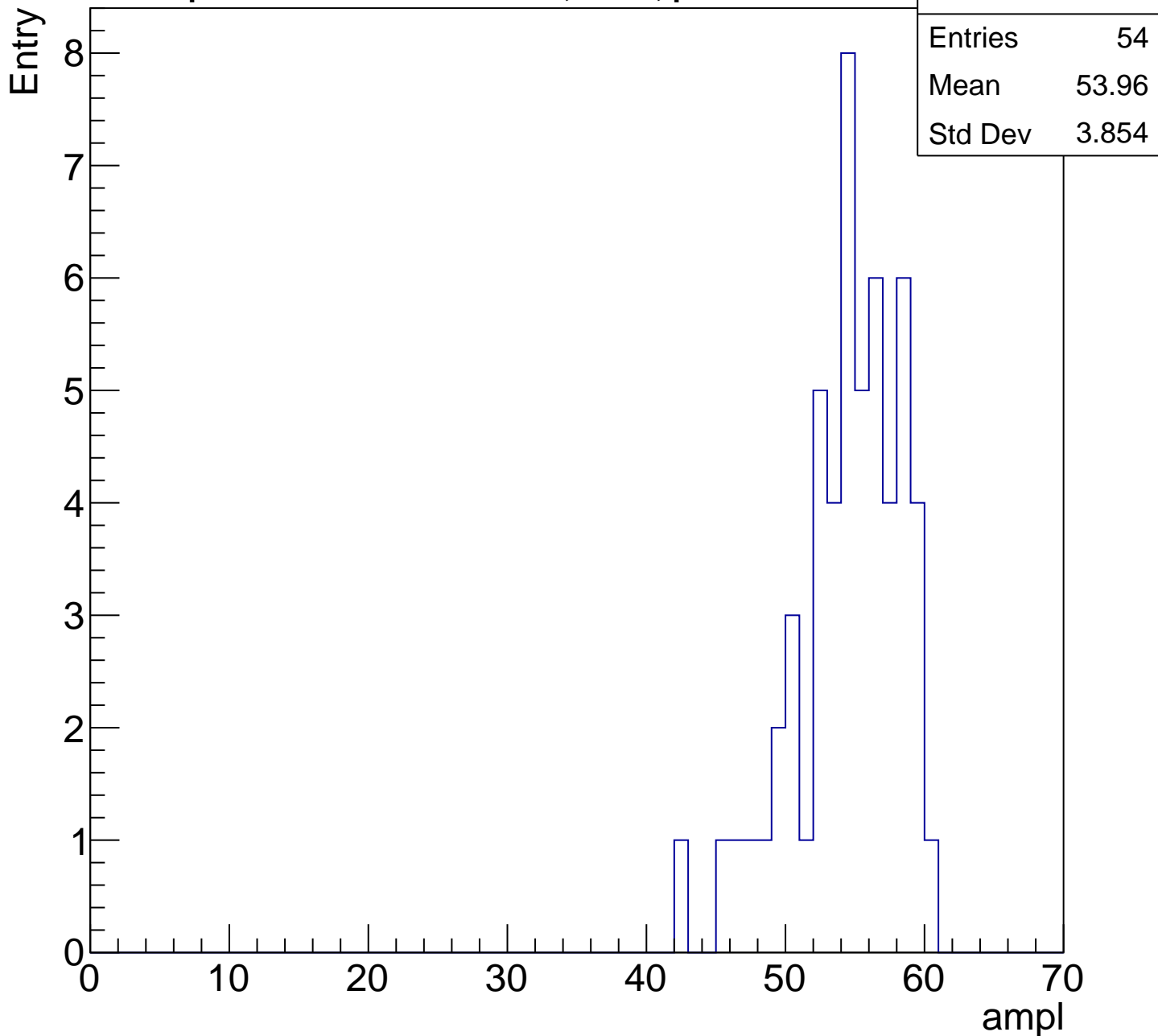
Entry



Entries	55
Mean	49.47
Std Dev	2.953

# B1L101S, U8-ch120, adc4

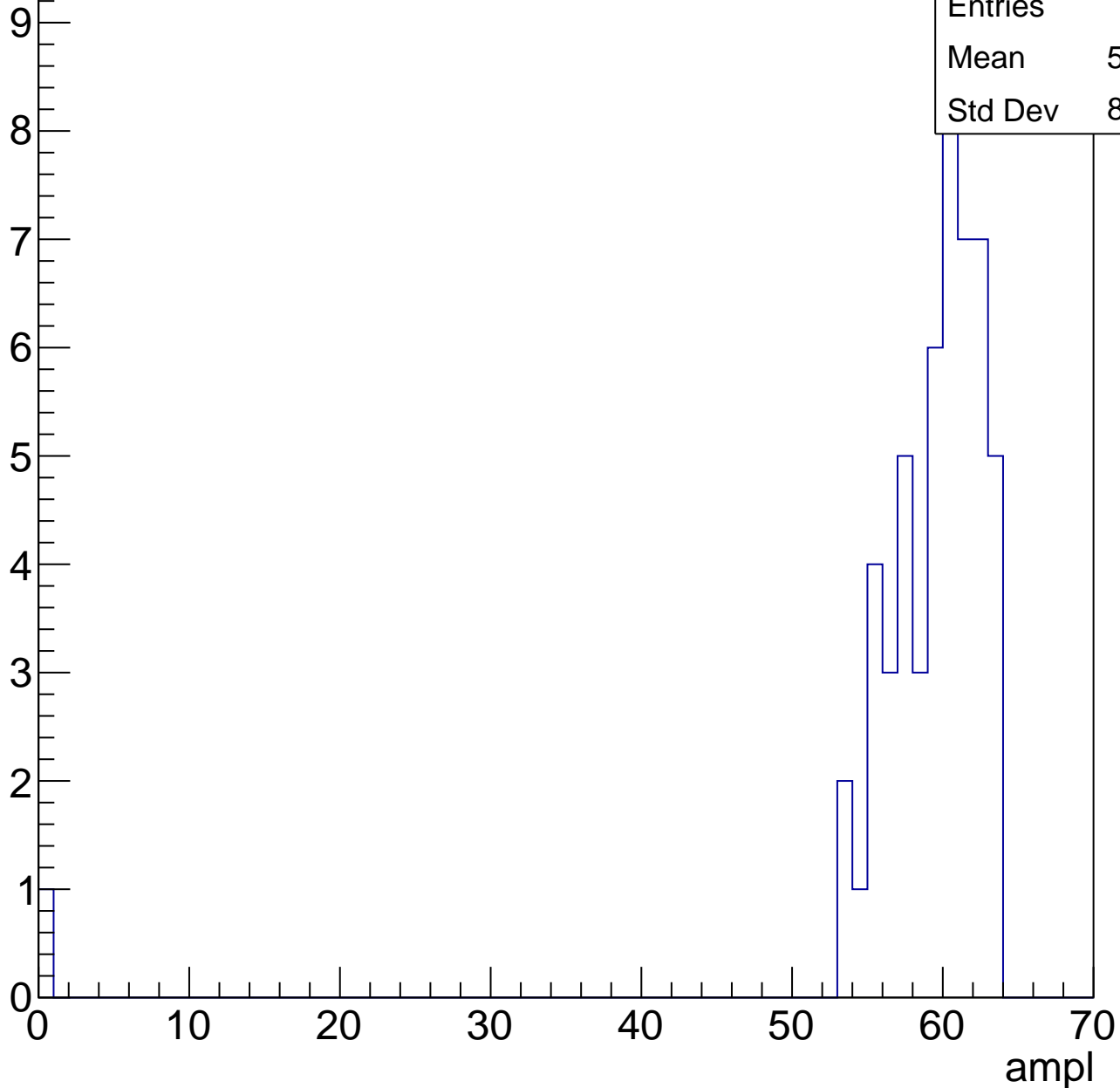
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U8-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

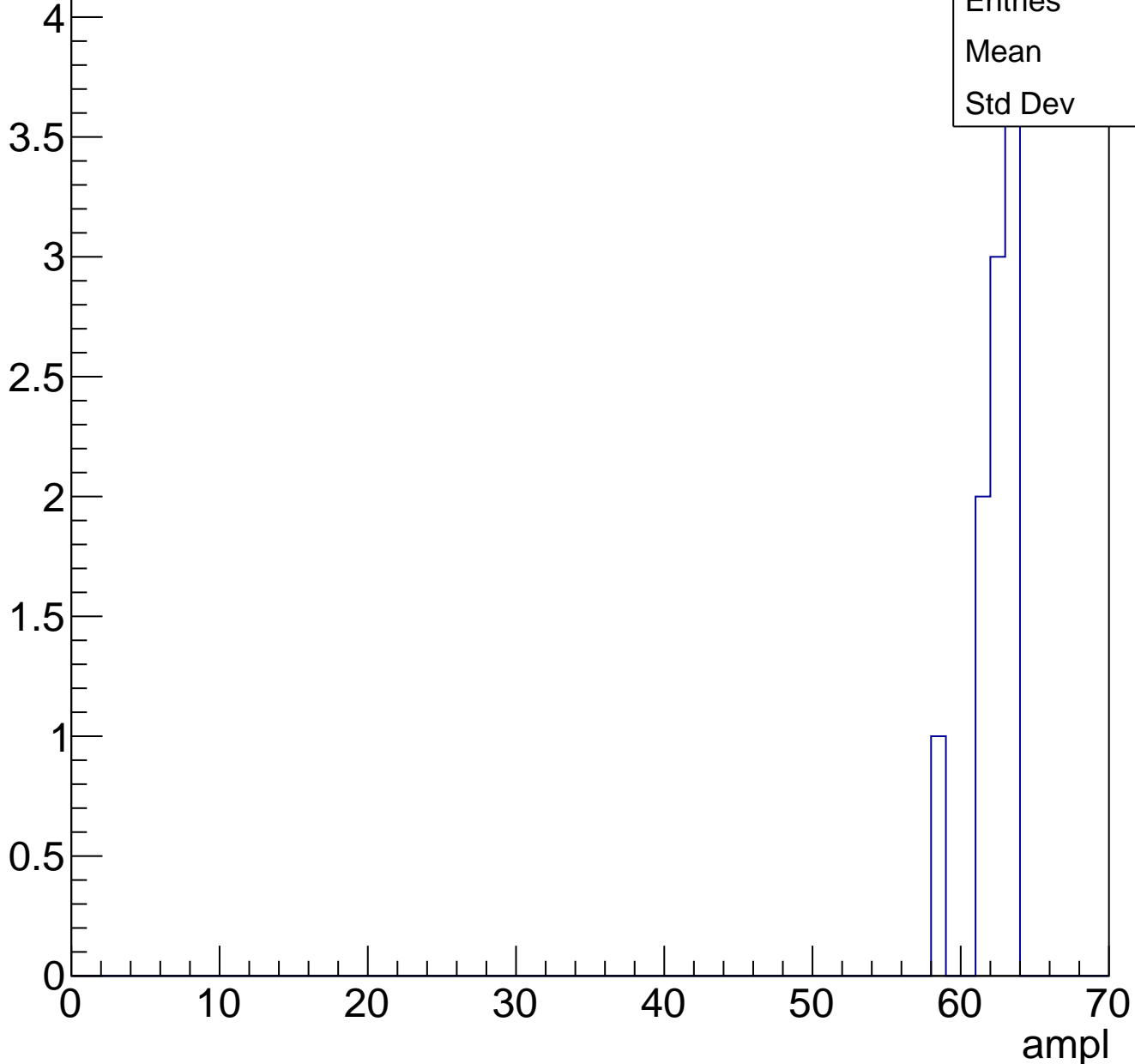
Entry



# B1L101S, U8-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



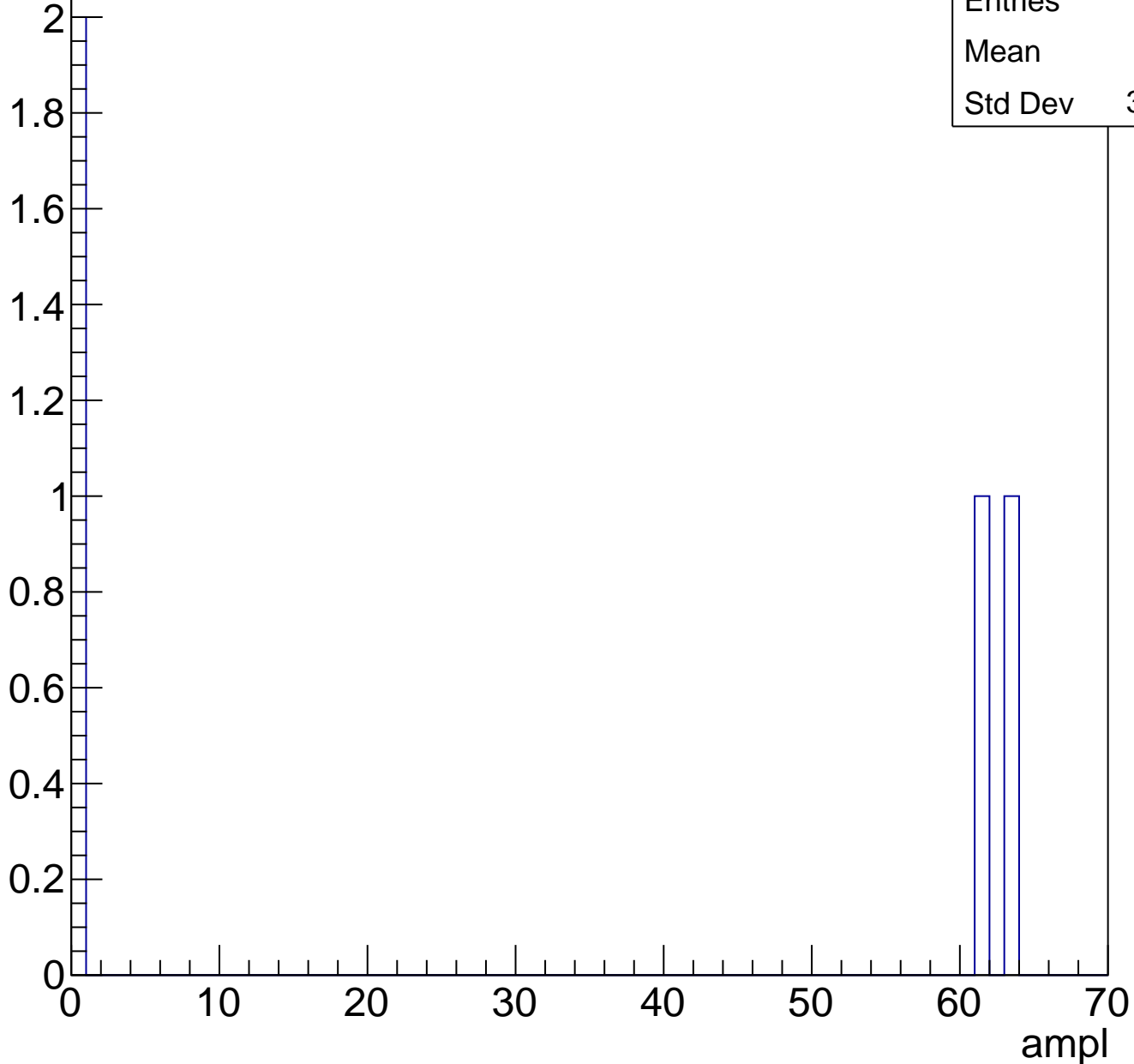
Entries	10
Mean	61.8
Std Dev	1.47



# B1L101S, U8-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	4
Mean	31
Std Dev	31.01

# B1L101S, U8-ch121, adc0

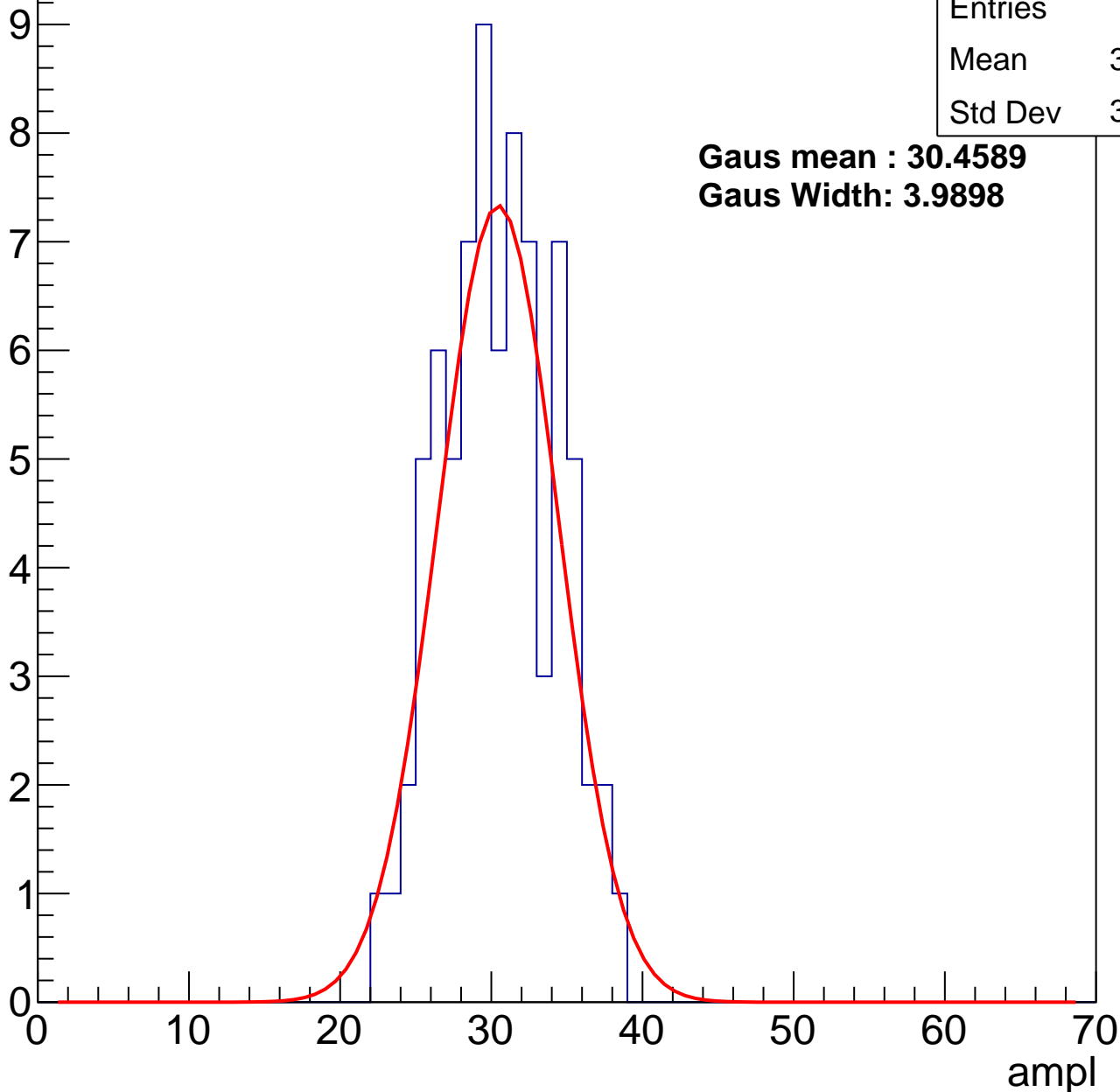
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	30.05
Std Dev	3.643

**Gaus mean : 30.4589**

**Gaus Width: 3.9898**



# B1L101S, U8-ch121, adc1

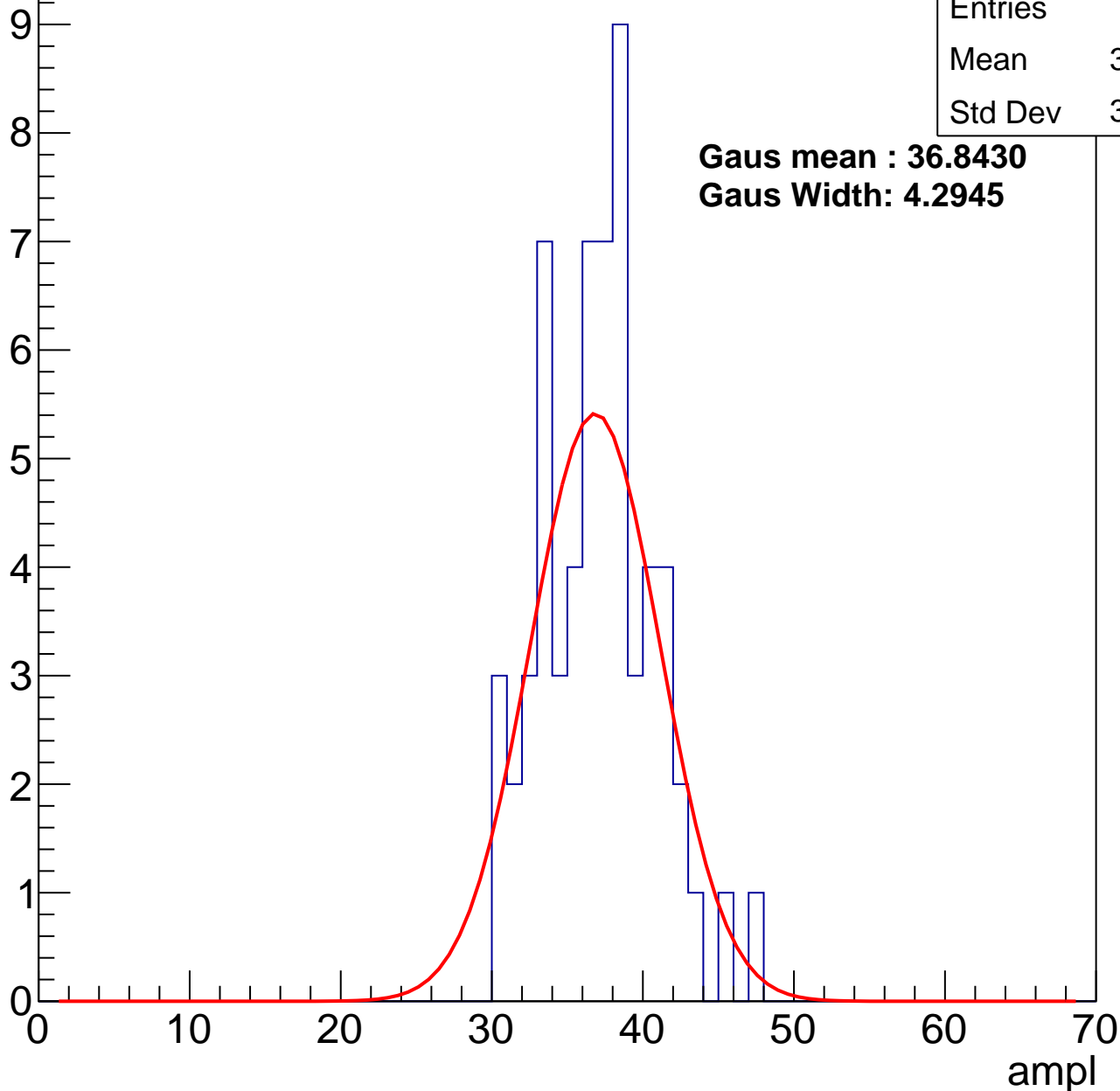
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	36.62
Std Dev	3.663

**Gaus mean : 36.8430**

**Gaus Width: 4.2945**



# B1L101S, U8-ch121, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	43.72
Std Dev	3.69

**Gaus mean : 43.8858**

**Gaus Width: 3.7617**

10

8

6

4

2

0

0

10

20

30

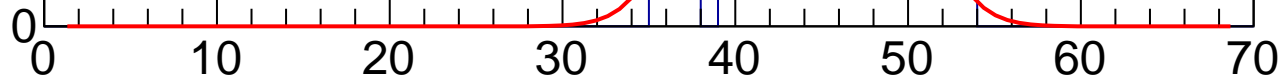
40

50

60

70

ampl

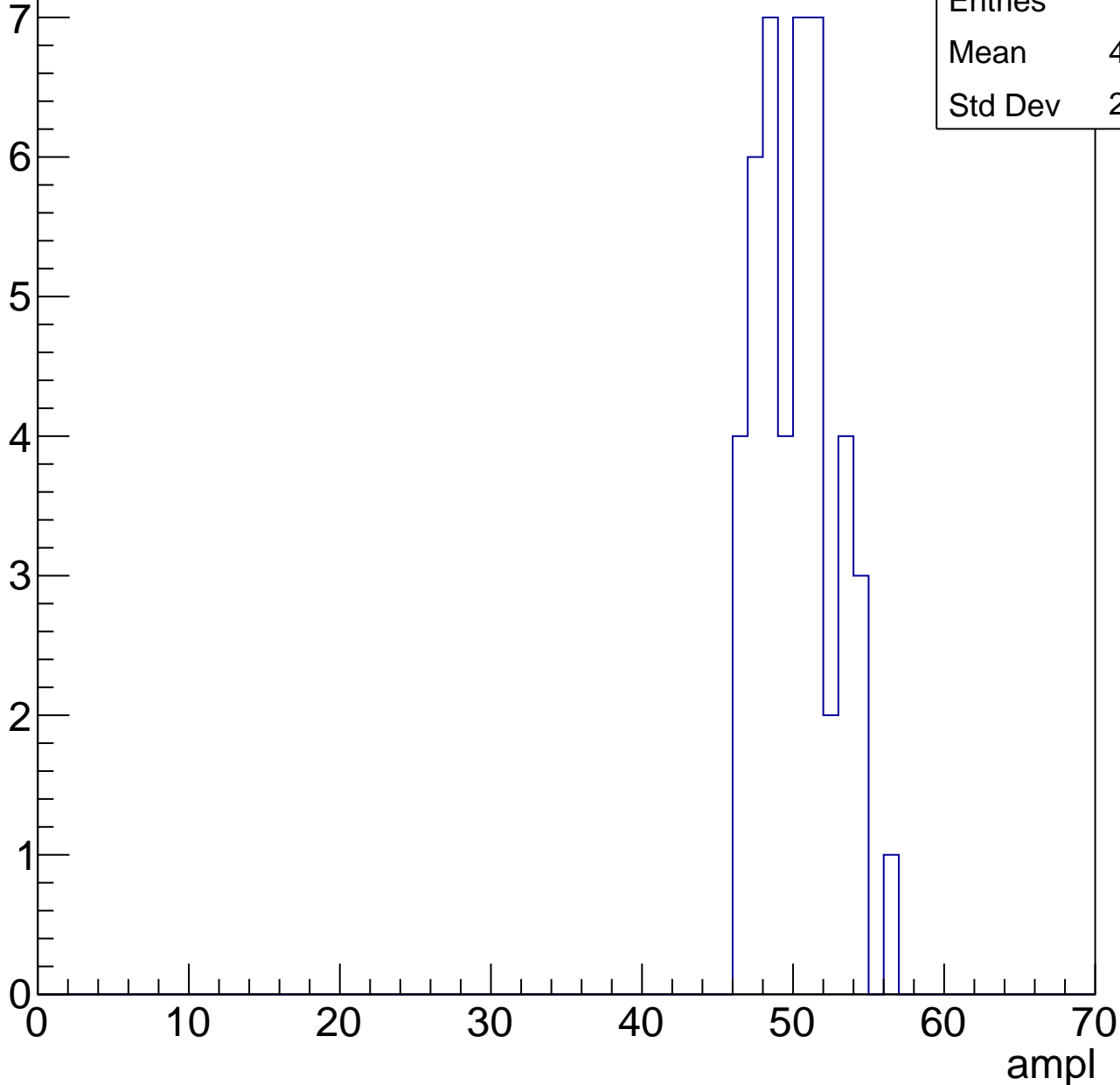


# B1L101S, U8-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

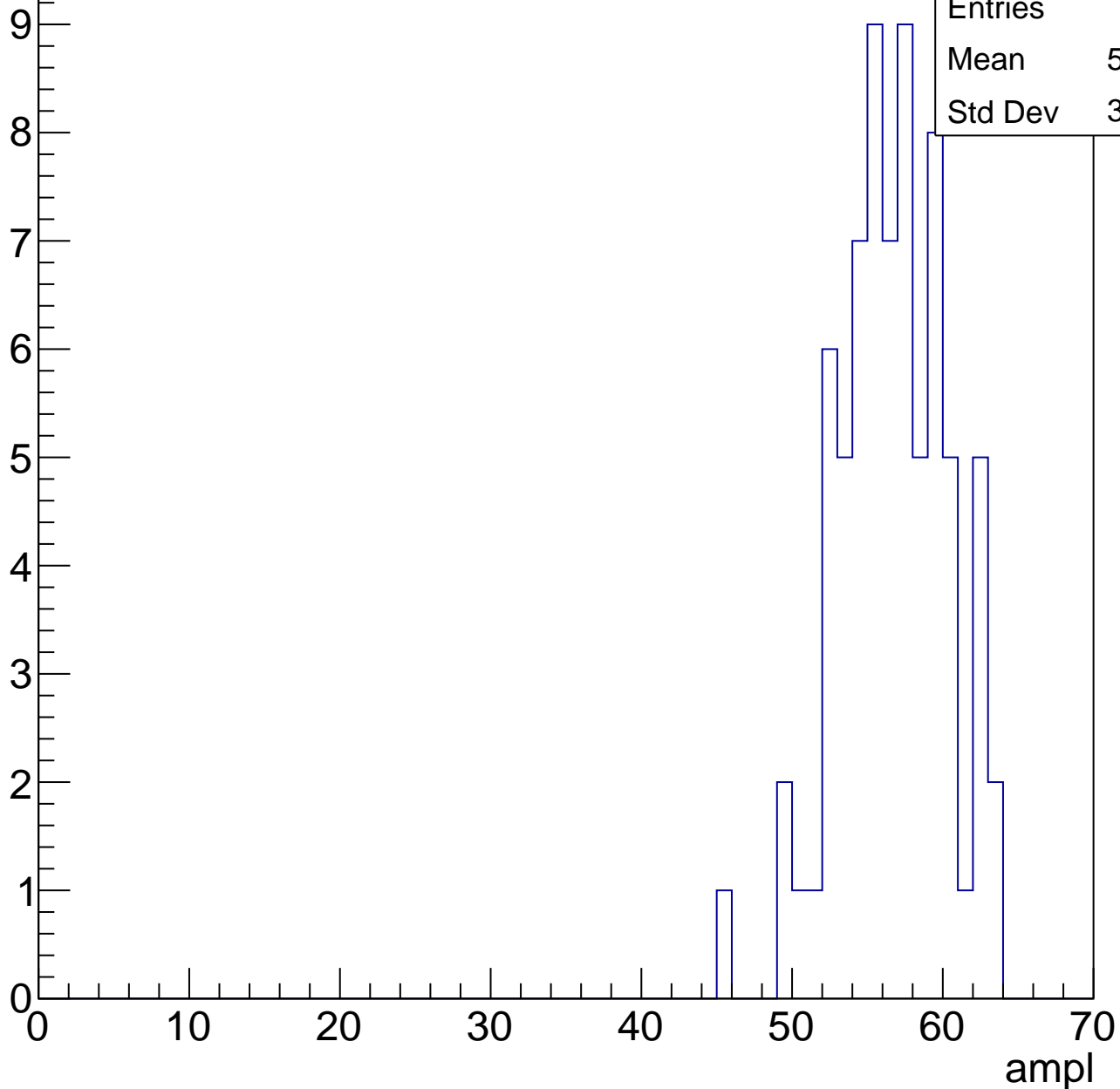
Entries	45
Mean	49.76
Std Dev	2.505



# B1L101S, U8-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



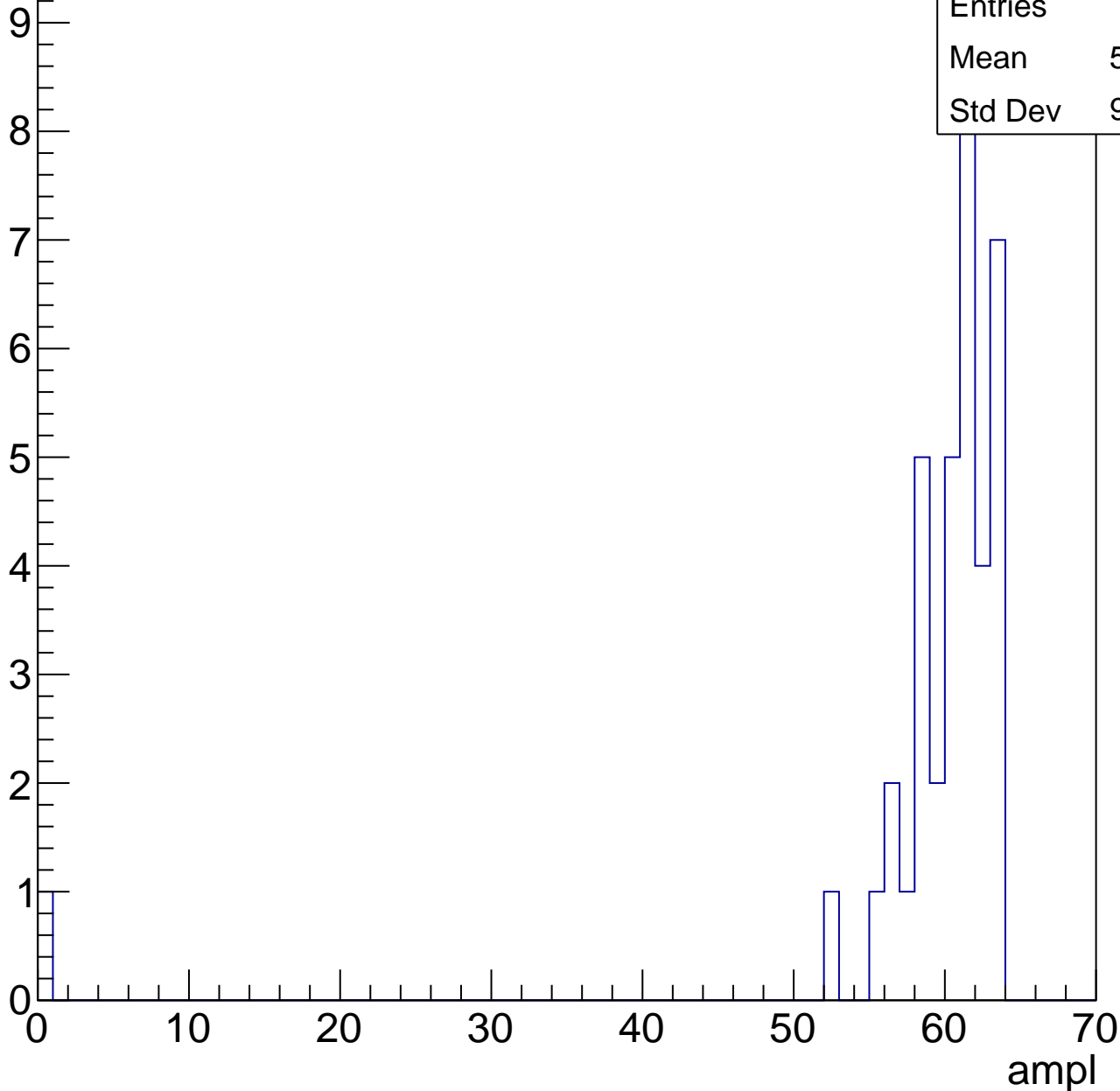
Entries	74
Mean	56.19
Std Dev	3.563

# B1L101S, U8-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	38
Mean	58.47
Std Dev	9.936



# B1L101S, U8-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U8-ch122, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	81
Mean	27.77
Std Dev	6.66

**Gaus mean : 29.0290**

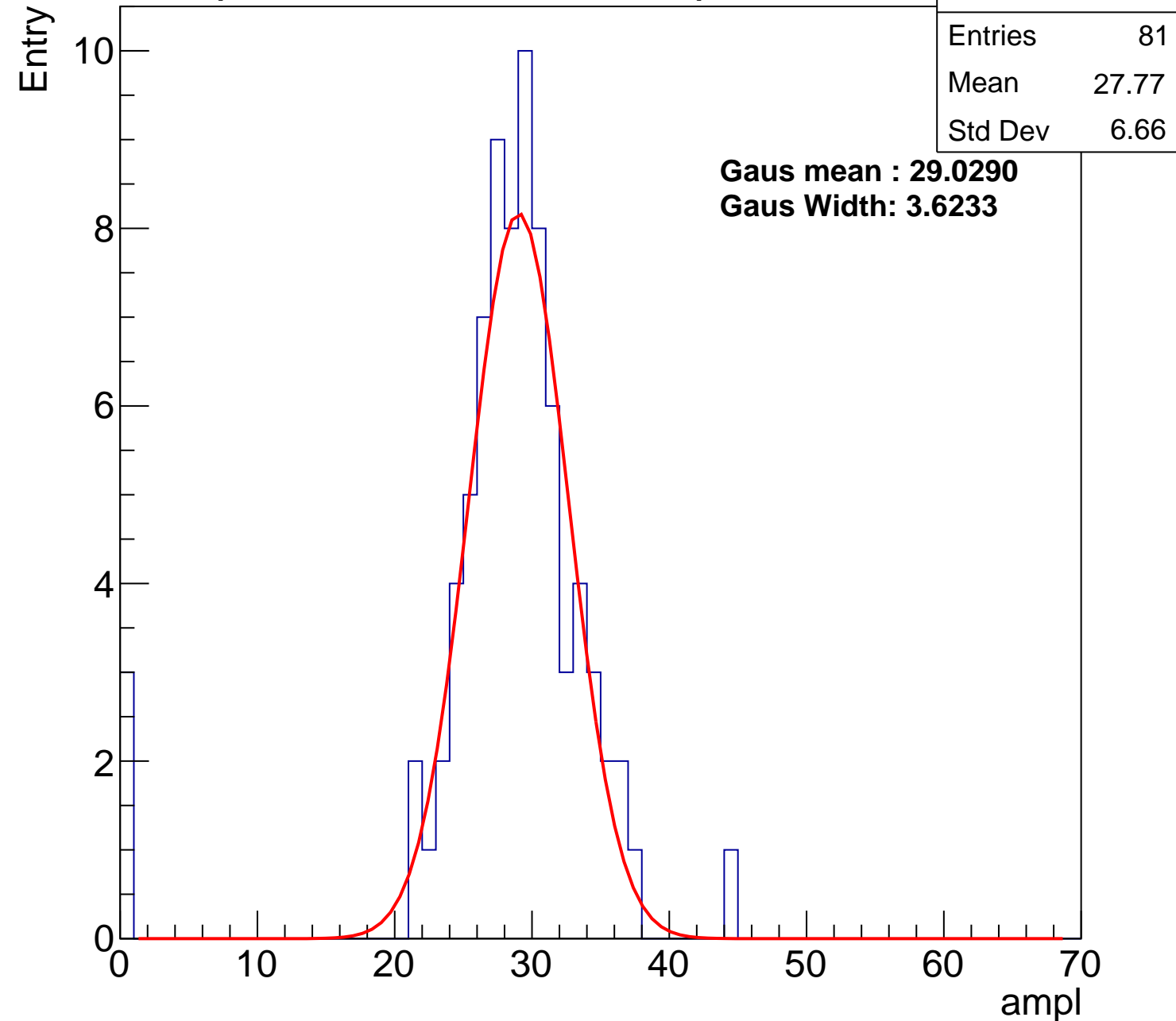
**Gaus Width: 3.6233**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



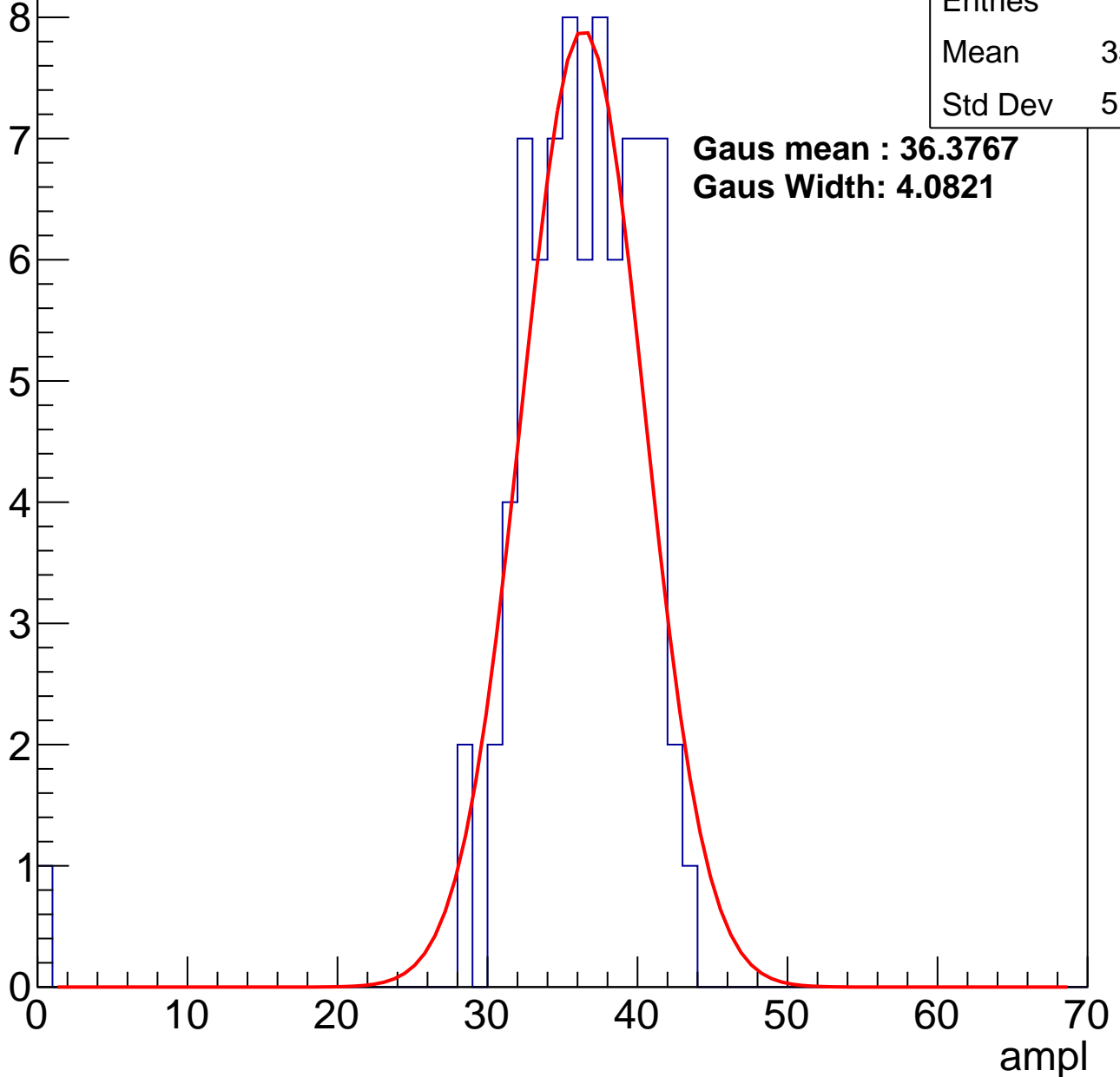
# B1L101S, U8-ch122, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	35.64
Std Dev	5.318

**Gaus mean : 36.3767**  
**Gaus Width: 4.0821**



# B1L101S, U8-ch122, adc2

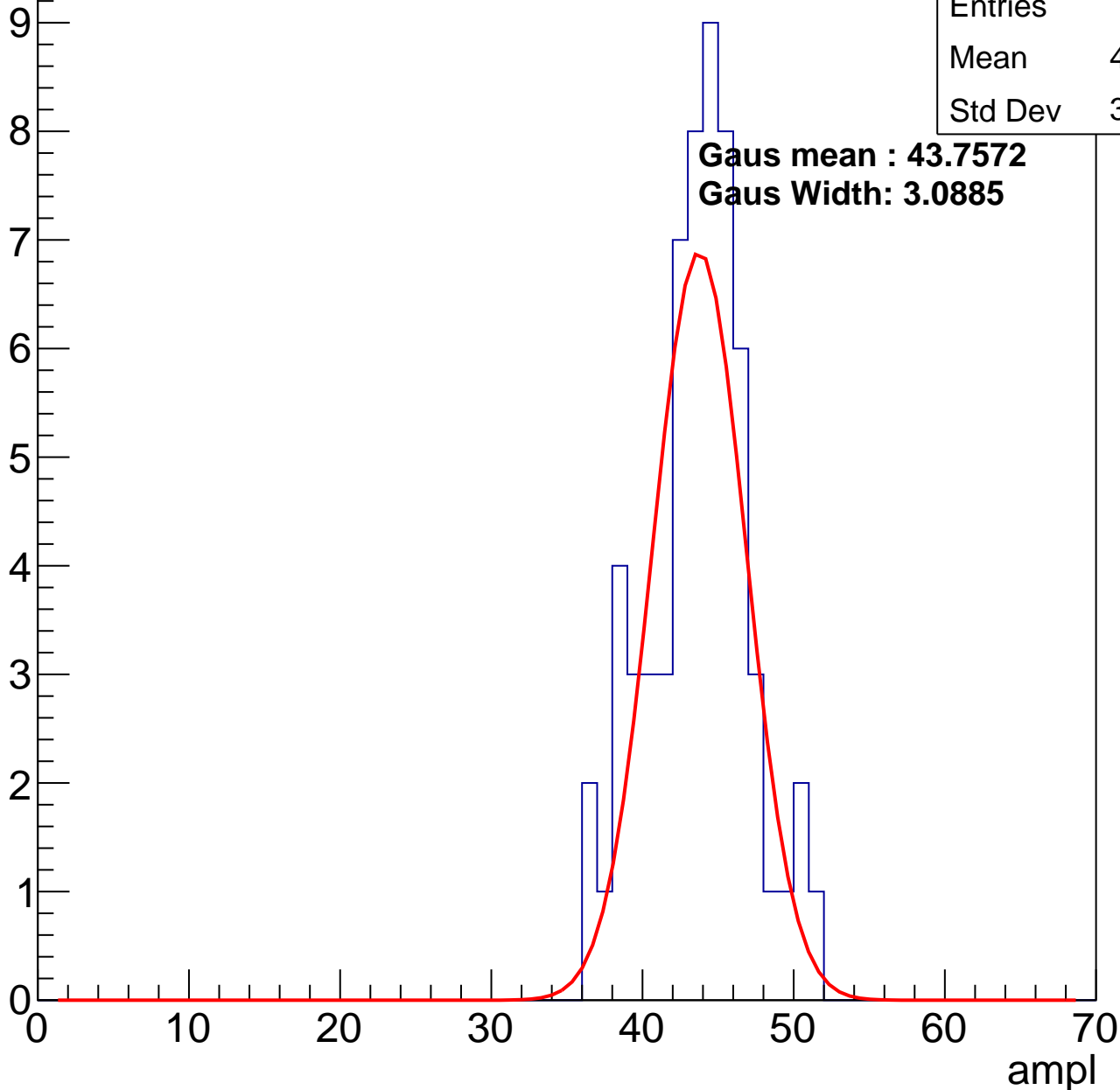
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	43.23
Std Dev	3.338

**Gaus mean : 43.7572**

**Gaus Width: 3.0885**

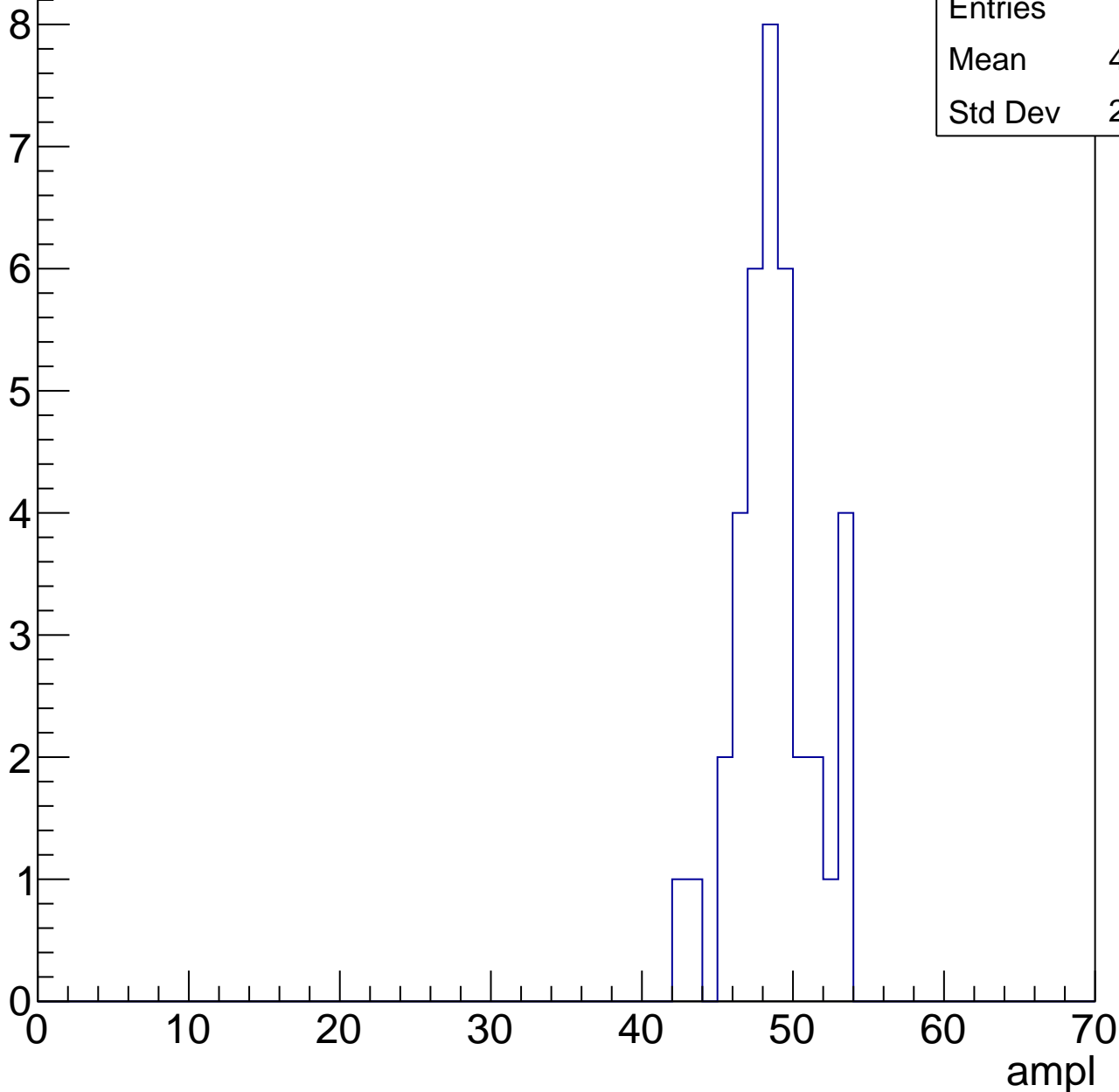


# B1L101S, U8-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	37
Mean	48.24
Std Dev	2.583



# B1L101S, U8-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	74
Mean	53.95
Std Dev	3.097

Entry

10

8

6

4

2

0

0

10

20

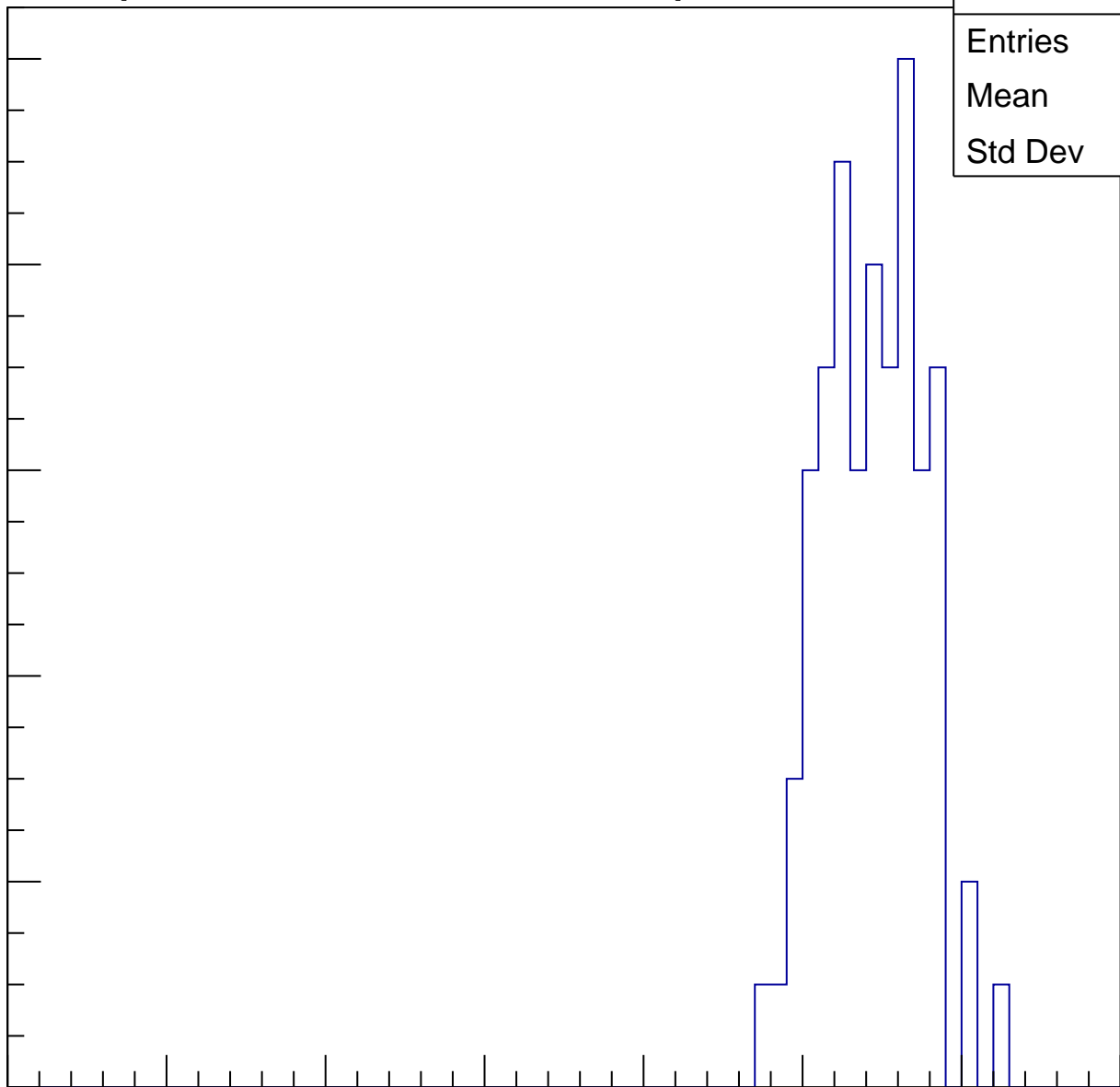
30

40

50

60

ampl



# B1L101S, U8-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

Entries	55
Mean	58.84
Std Dev	8.368



# B1L101S, U8-ch122, adc6

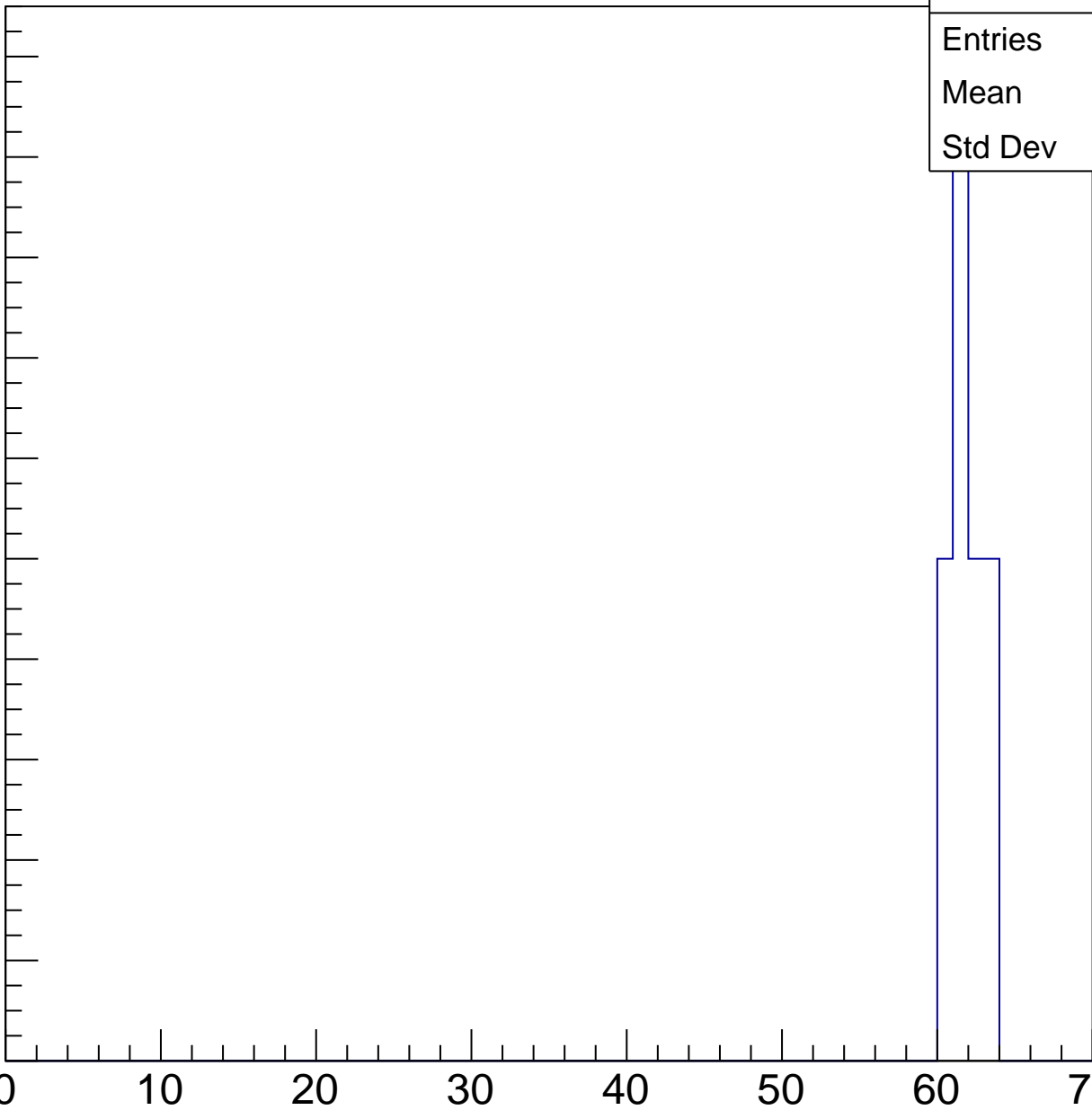
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.4
Std Dev	1.02

ampl





# B1L101S, U8-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U8-ch123, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	63
Mean	30.19
Std Dev	3.177

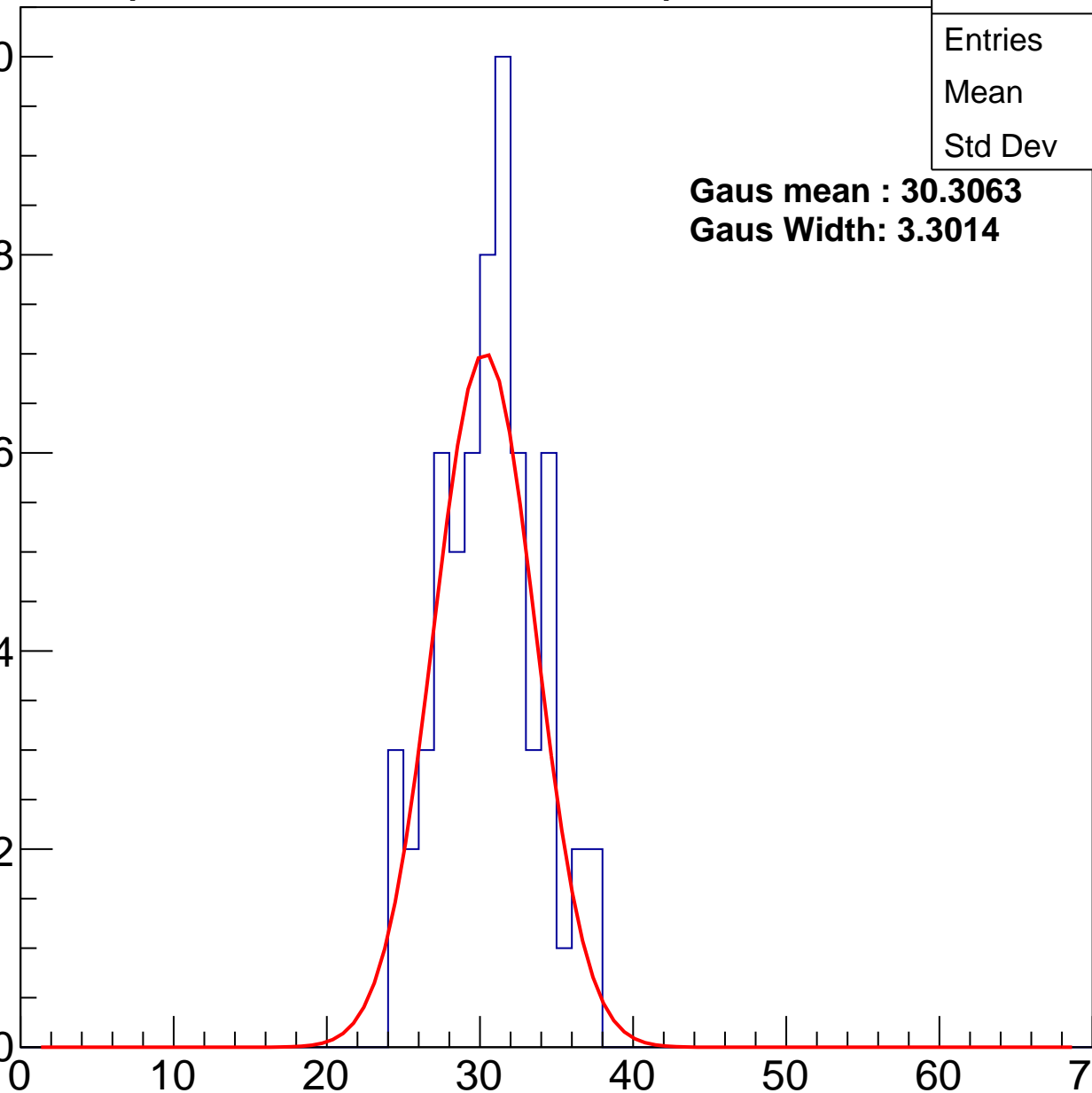
**Gaus mean : 30.3063**

**Gaus Width: 3.3014**

Entry

10  
8  
6  
4  
2  
0

ampl



# B1L101S, U8-ch123, adc1

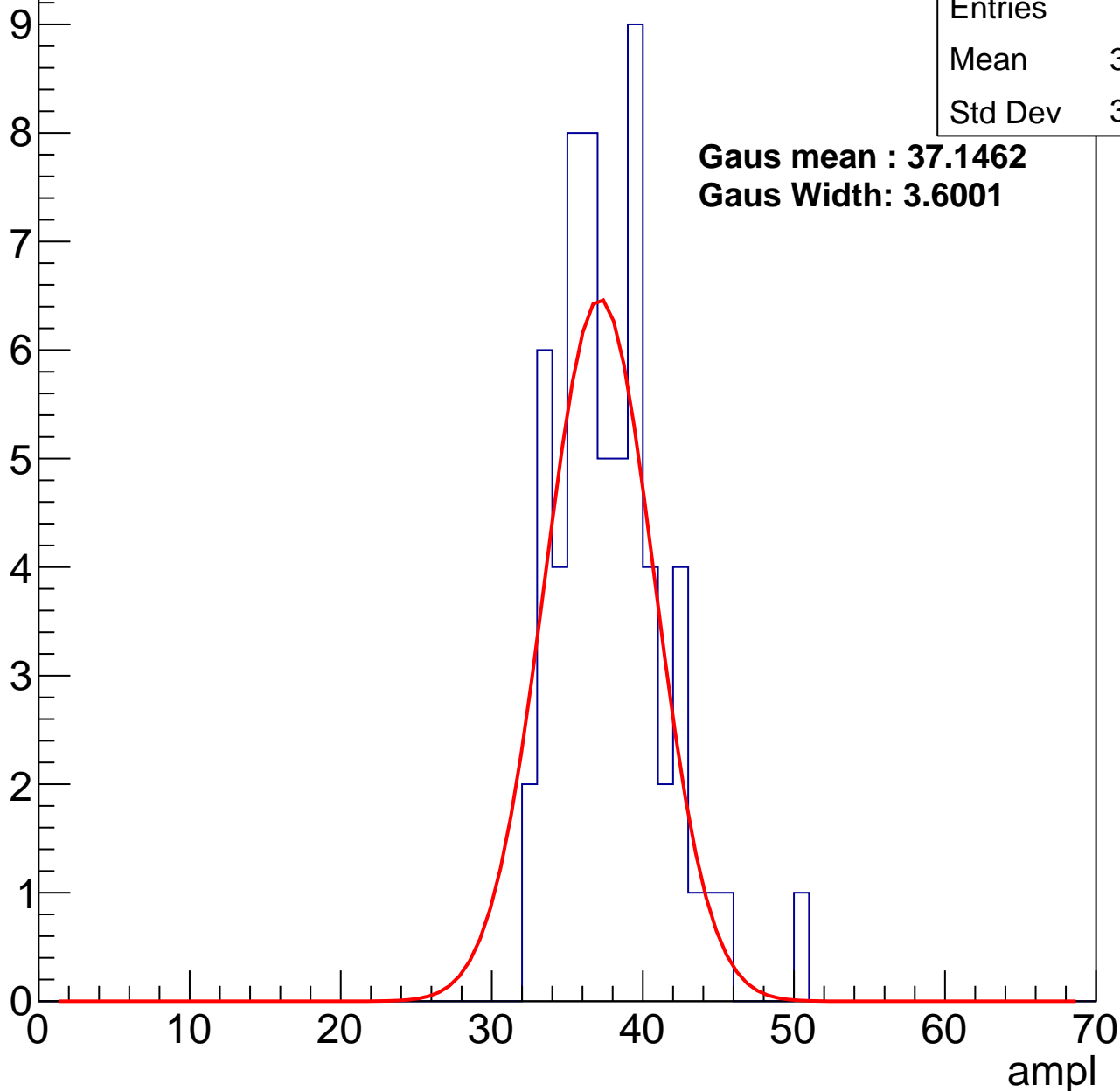
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	37.44
Std Dev	3.476

**Gaus mean : 37.1462**

**Gaus Width: 3.6001**



# B1L101S, U8-ch123, adc2

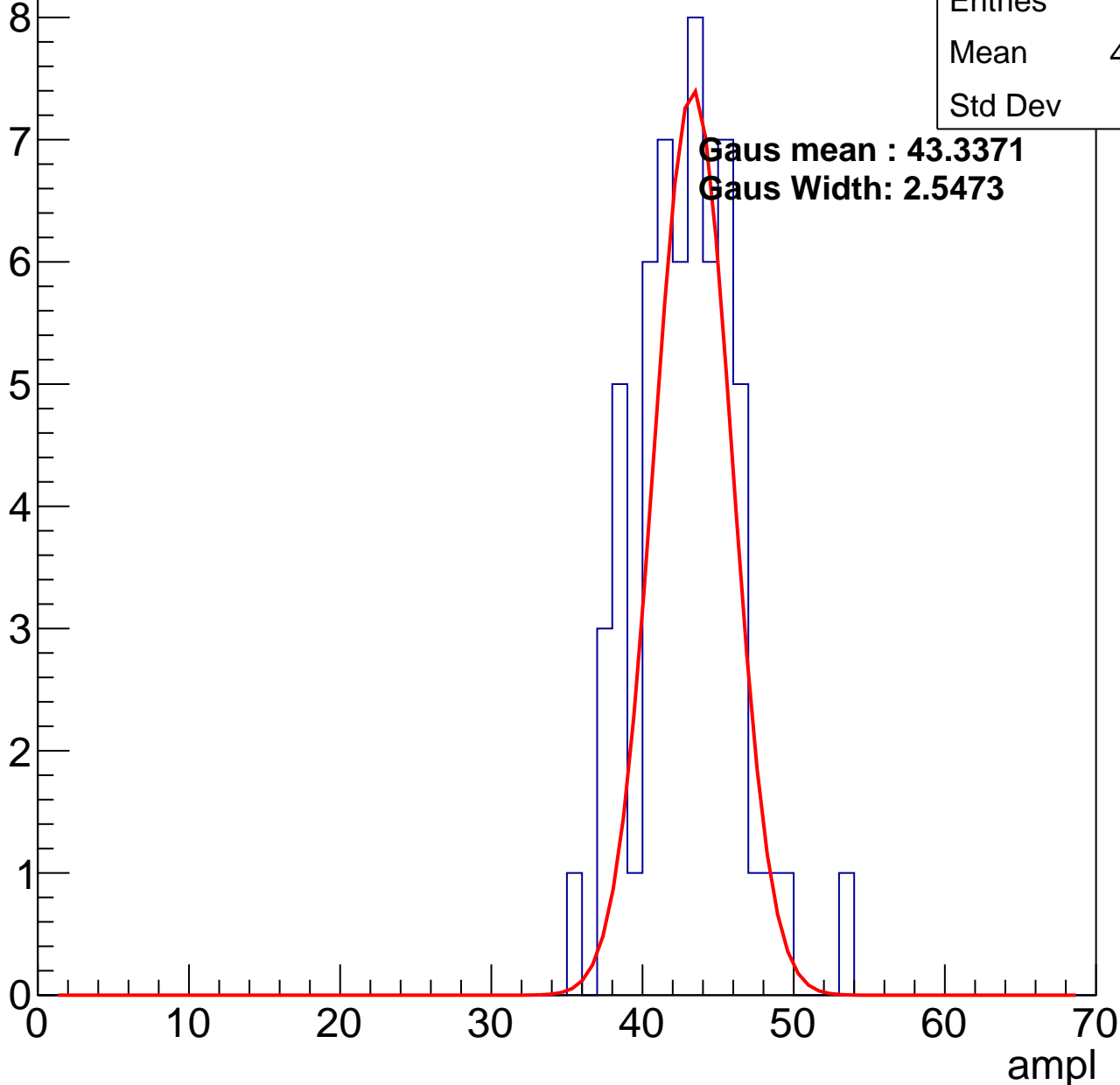
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	42.44
Std Dev	3.29

**Gaus mean : 43.3371**

**Gaus Width: 2.5473**

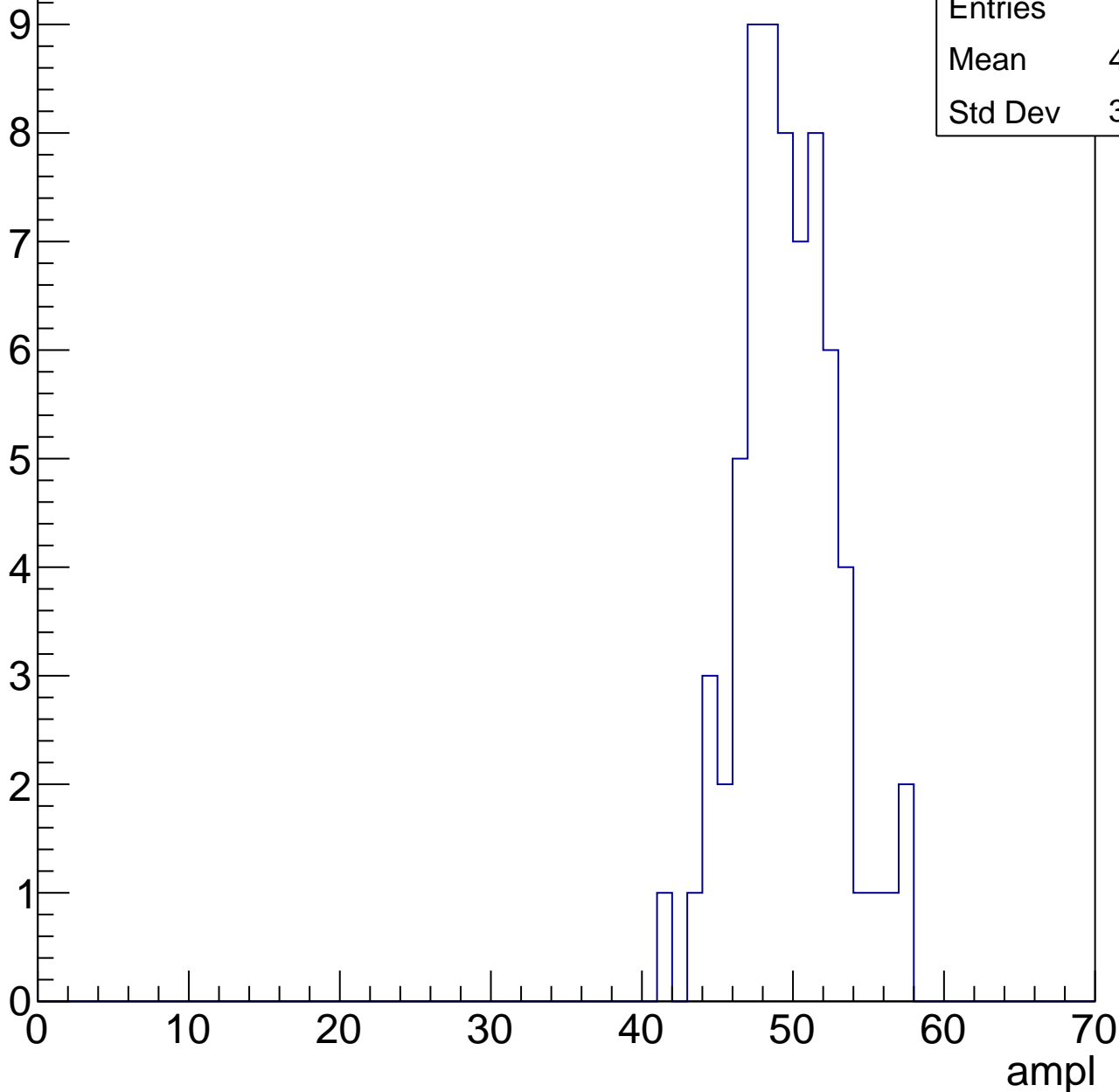


# B1L101S, U8-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	49.18
Std Dev	3.185

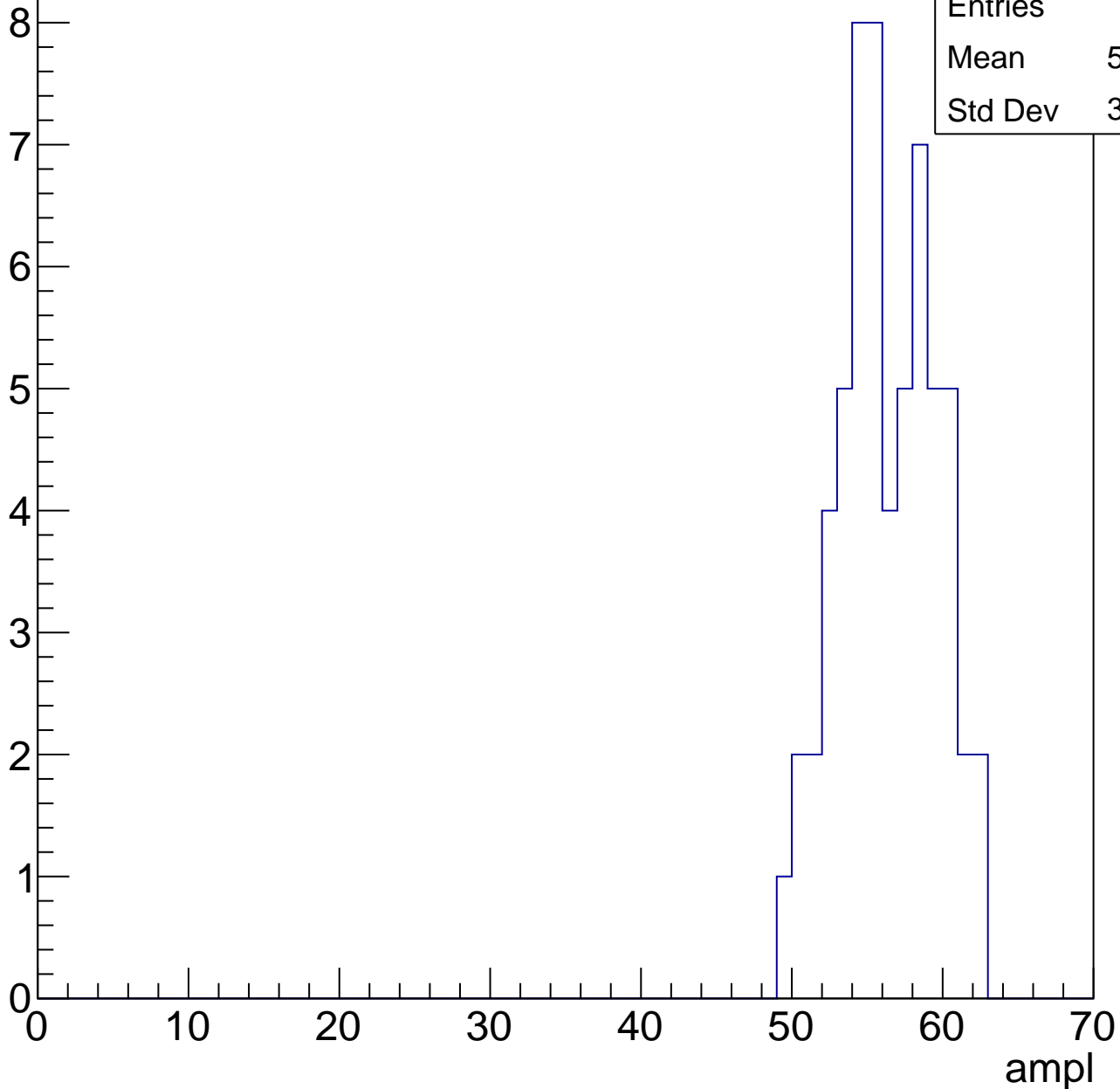


# B1L101S, U8-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	55.87
Std Dev	3.159

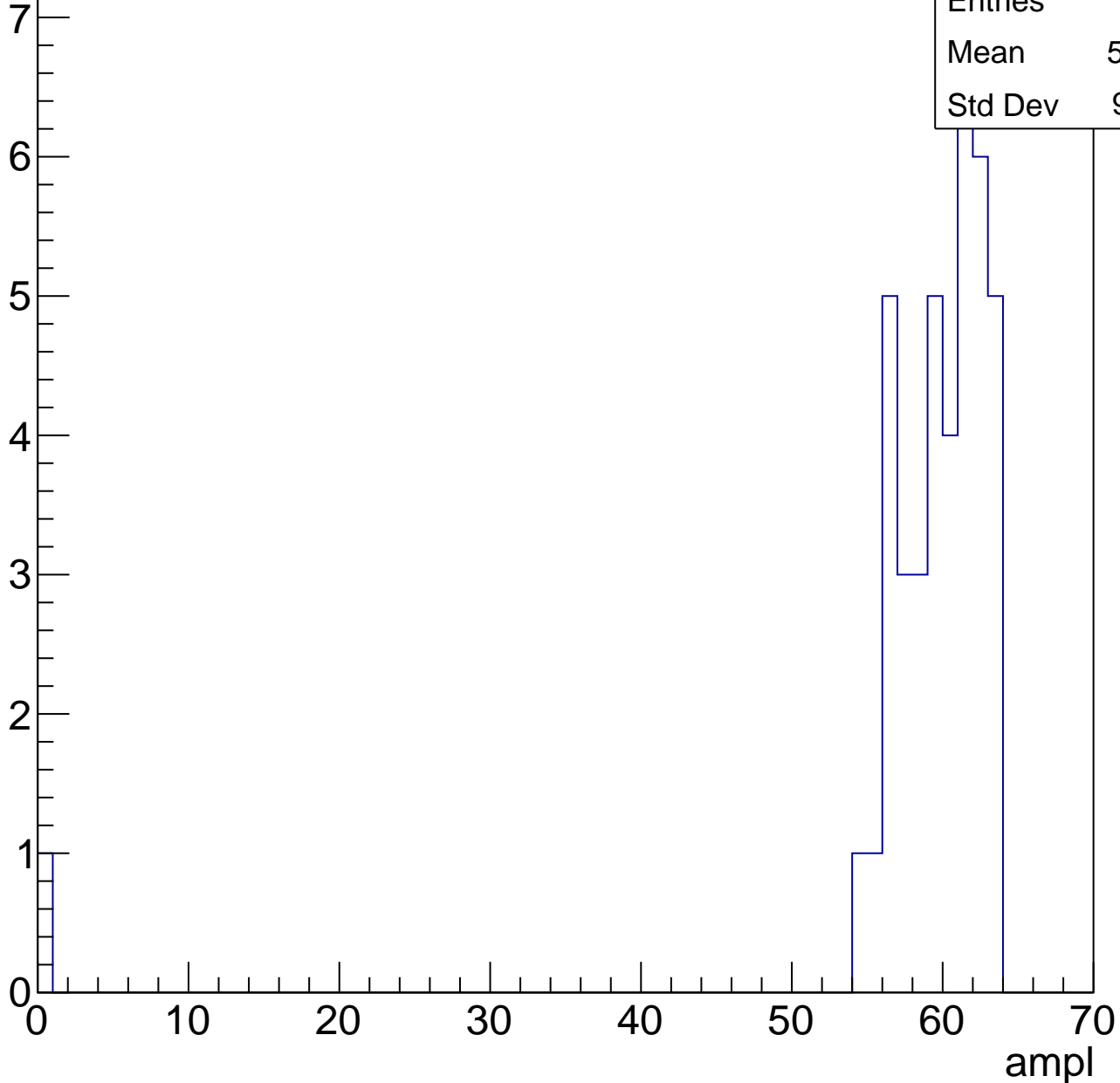


# B1L101S, U8-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	41
Mean	58.12
Std Dev	9.521

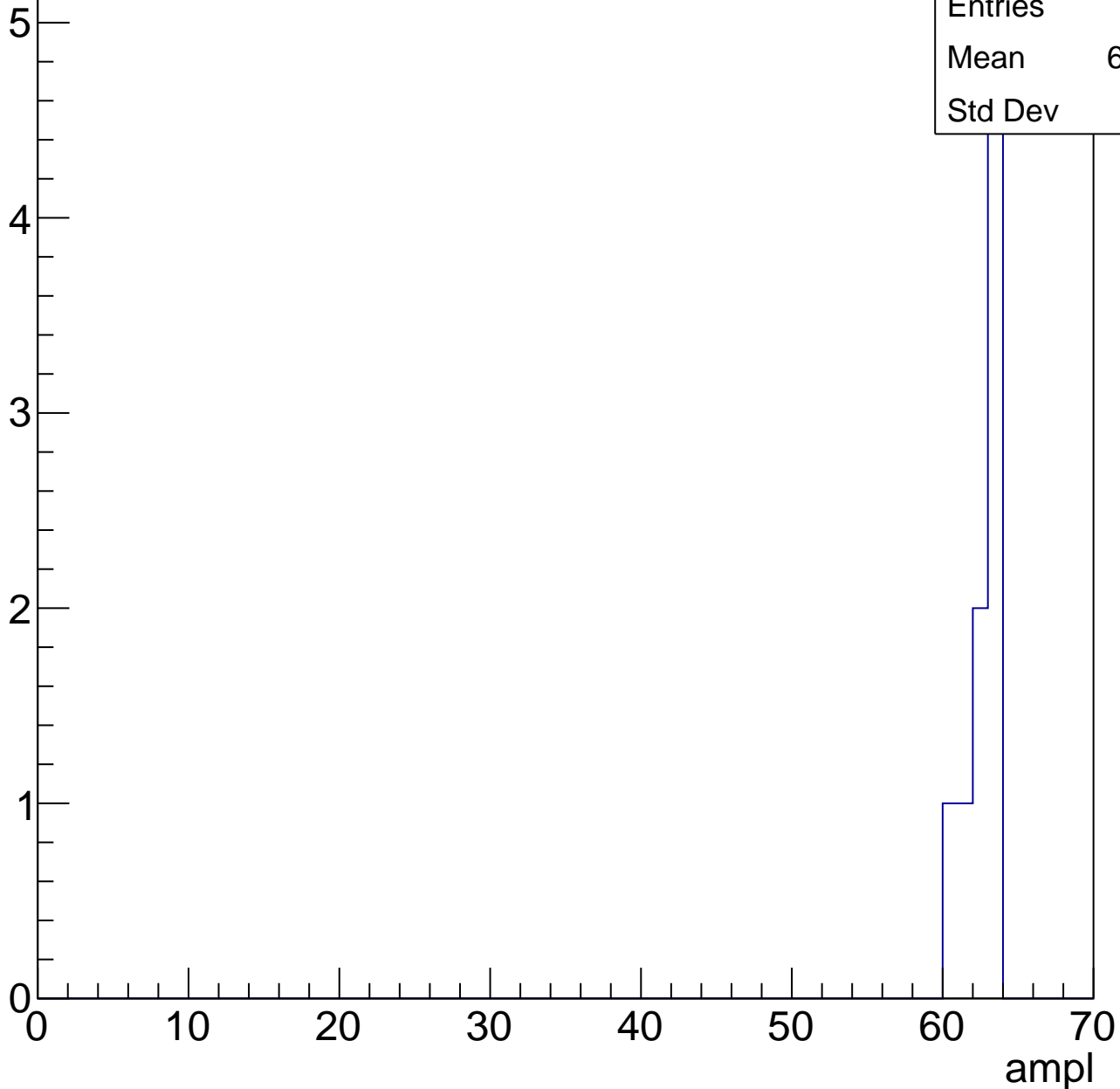


# B1L101S, U8-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	9
Mean	62.22
Std Dev	1.03





# B1L101S, U8-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch124, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	72
Mean	27.88
Std Dev	4.475

**Gaus mean : 28.8770**

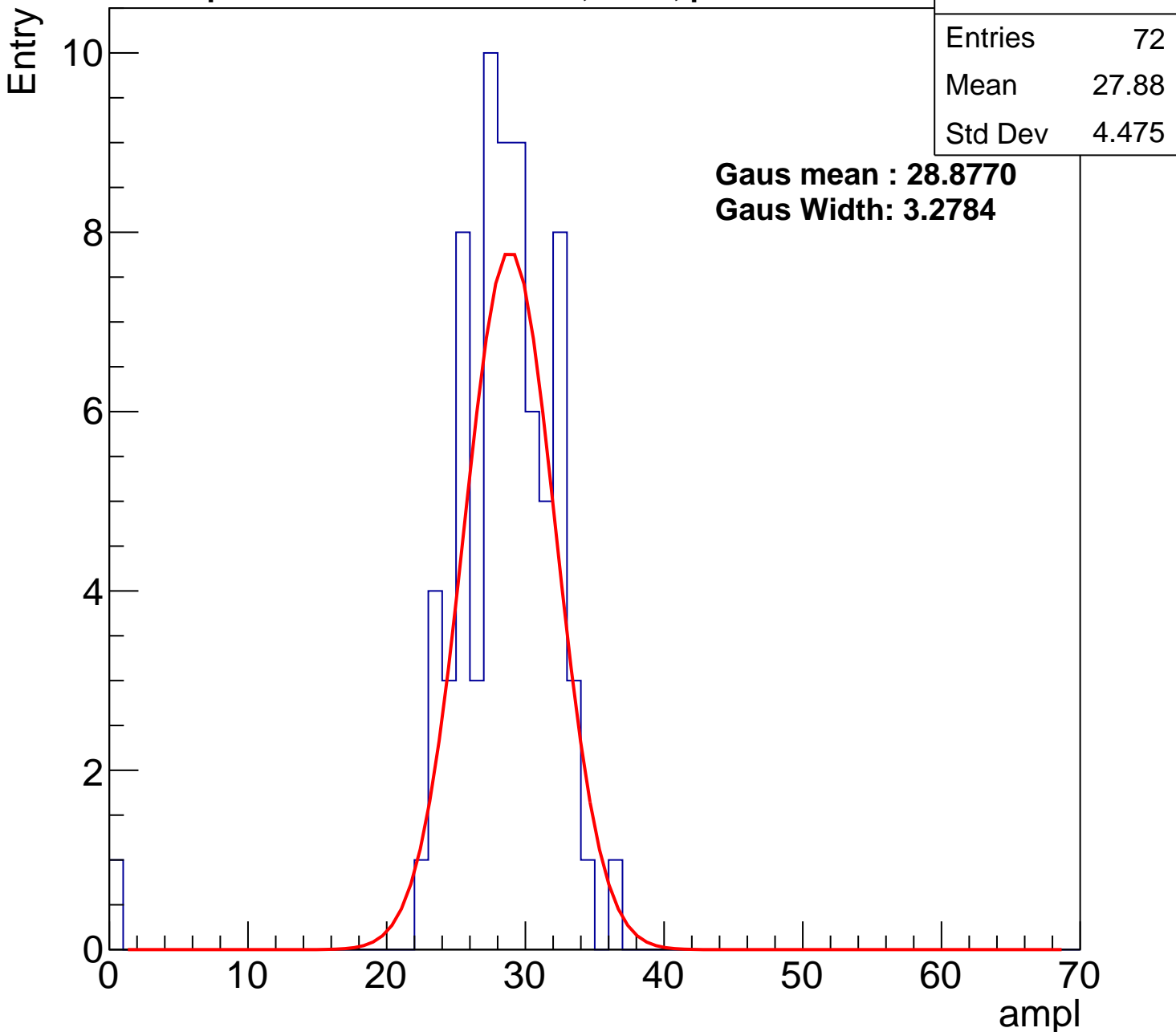
**Gaus Width: 3.2784**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U8-ch124, adc1

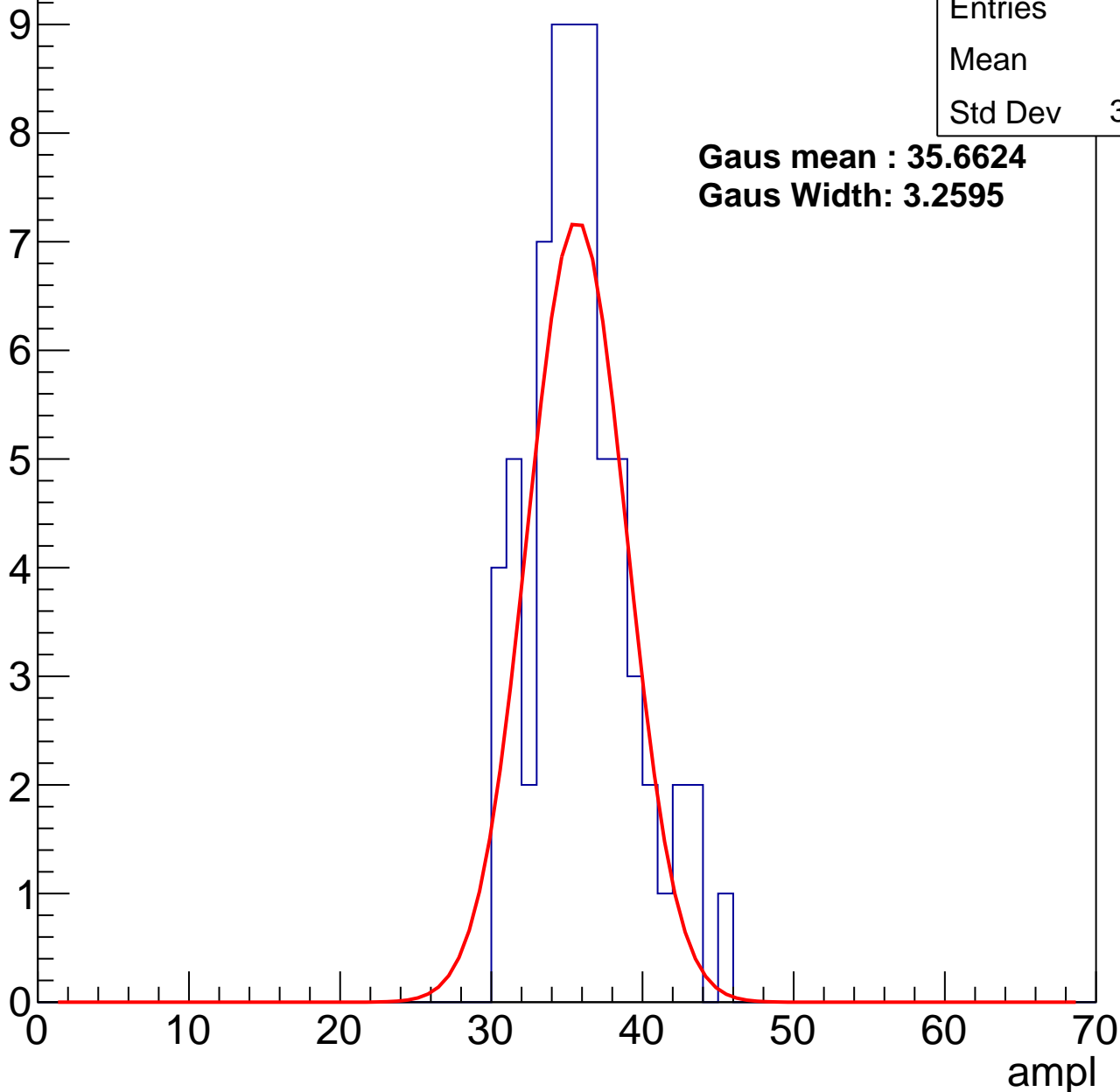
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	35.5
Std Dev	3.377

**Gaus mean : 35.6624**

**Gaus Width: 3.2595**



# B1L101S, U8-ch124, adc2

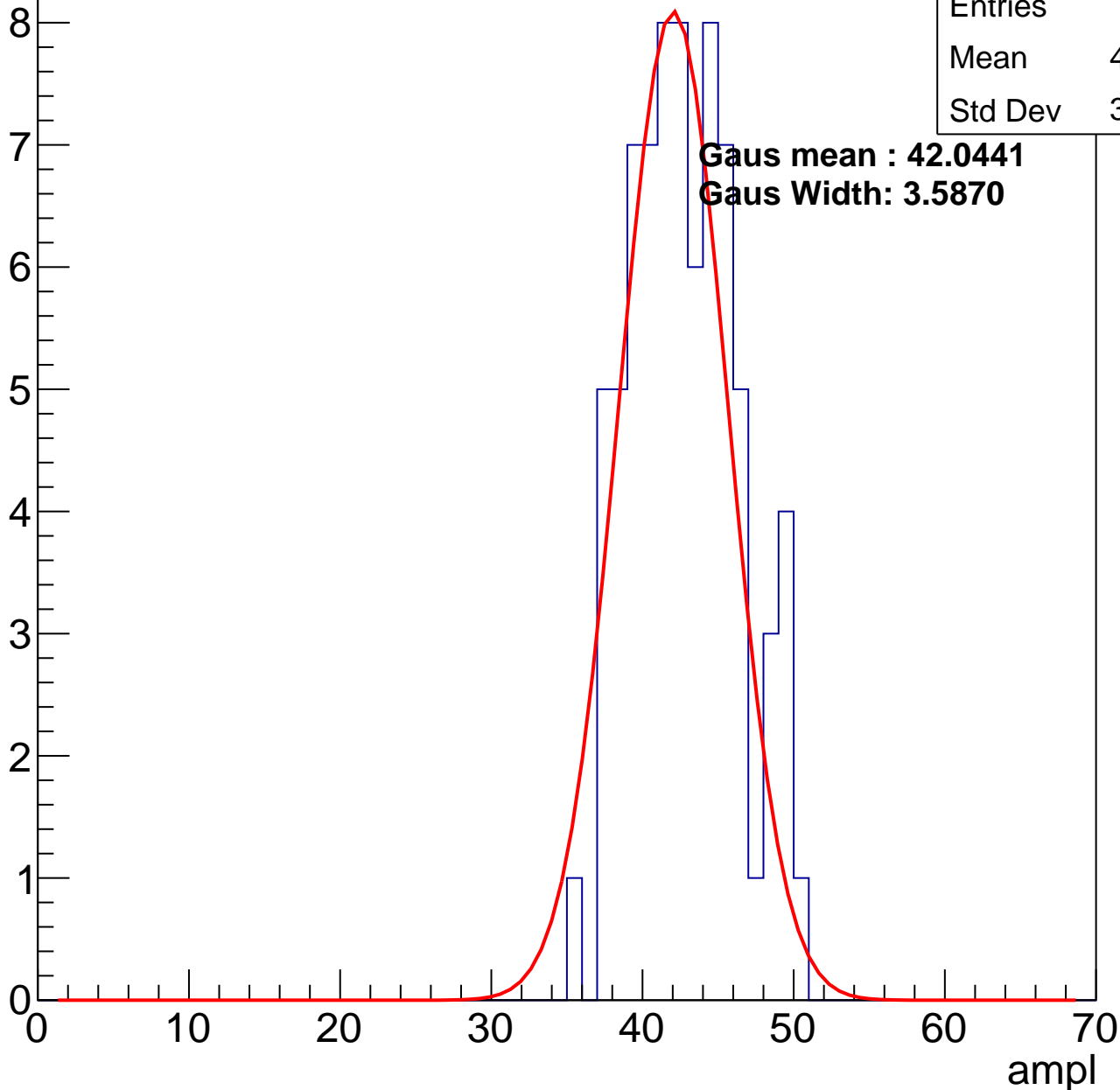
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	42.36
Std Dev	3.474

**Gaus mean : 42.0441**

**Gaus Width: 3.5870**

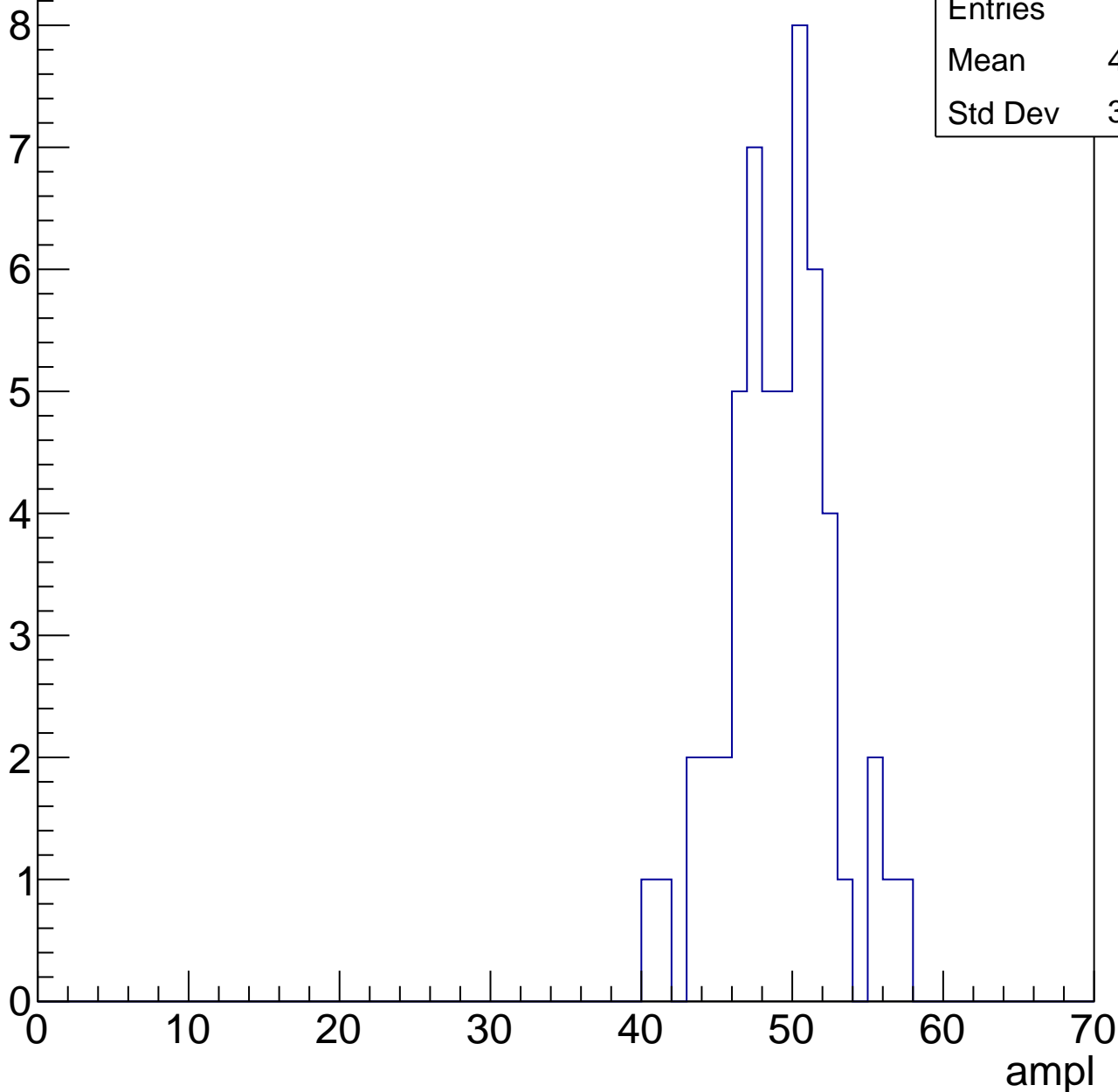


# B1L101S, U8-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	48.66
Std Dev	3.475

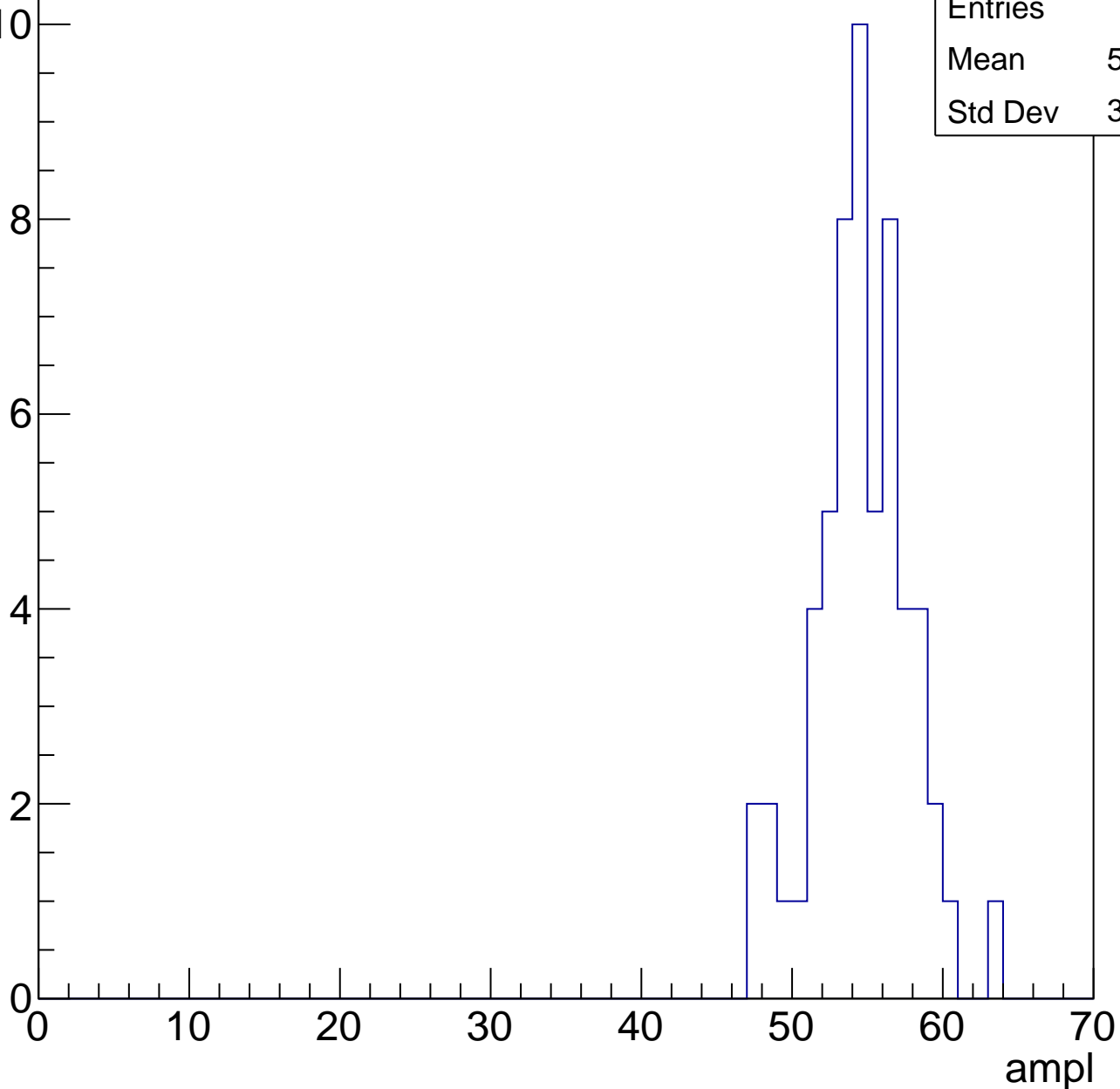


# B1L101S, U8-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	54.16
Std Dev	3.156



# B1L101S, U8-ch124, adc5

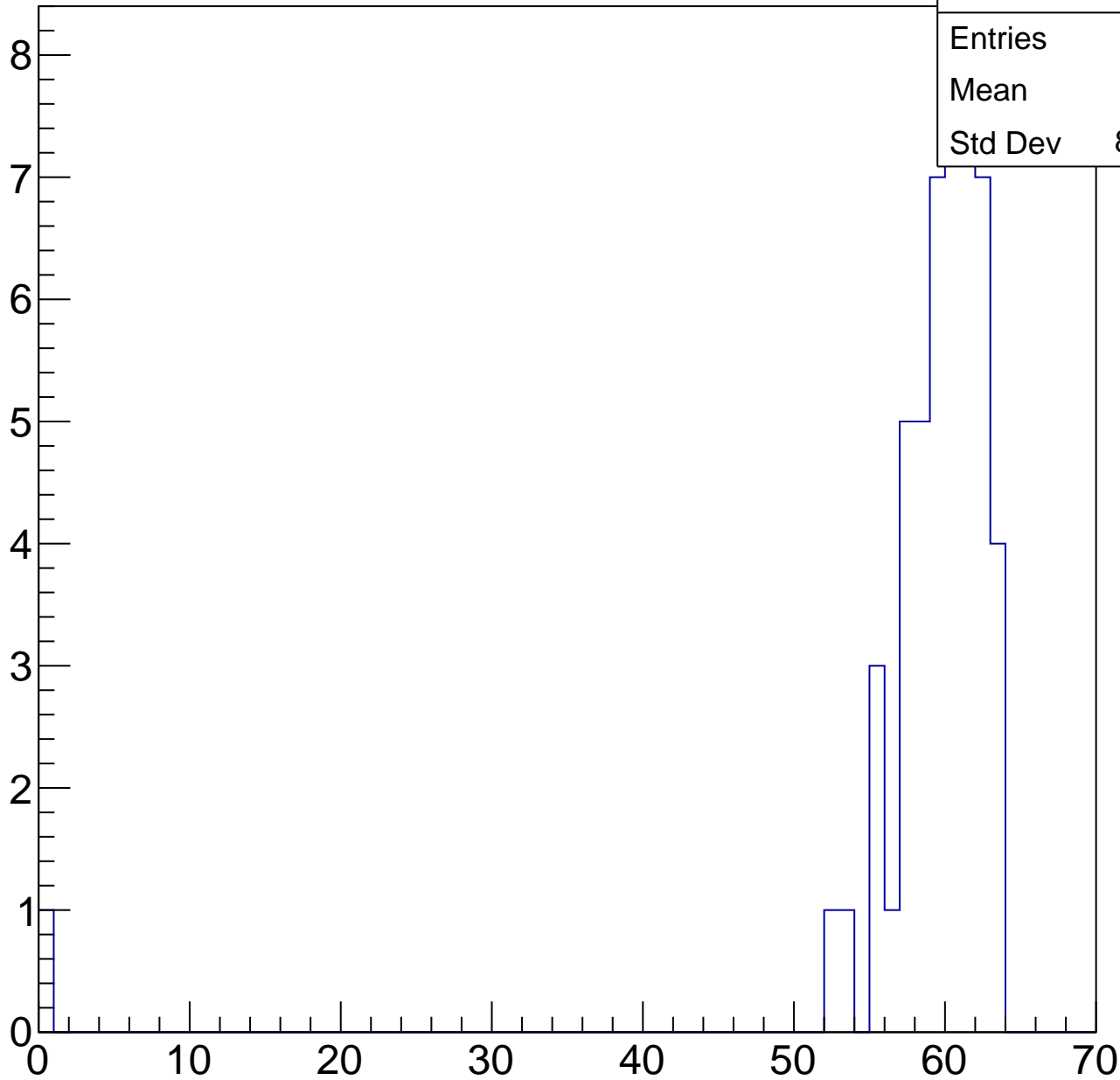
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	58.2
Std Dev	8.611

ampl

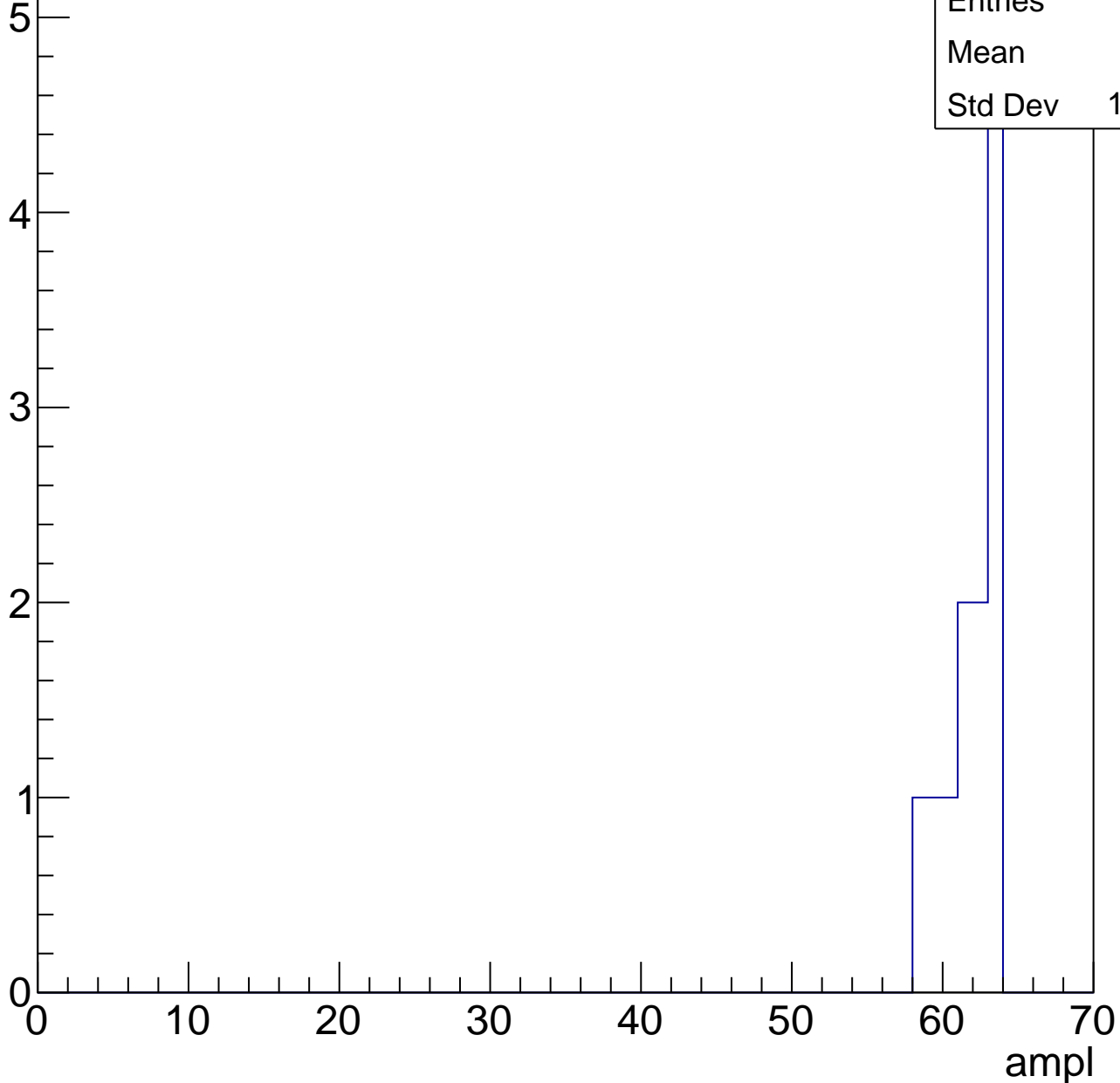


# B1L101S, U8-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	12
Mean	61.5
Std Dev	1.658





# B1L101S, U8-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	20.67
Std Dev	29.23

# B1L101S, U8-ch125, adc0

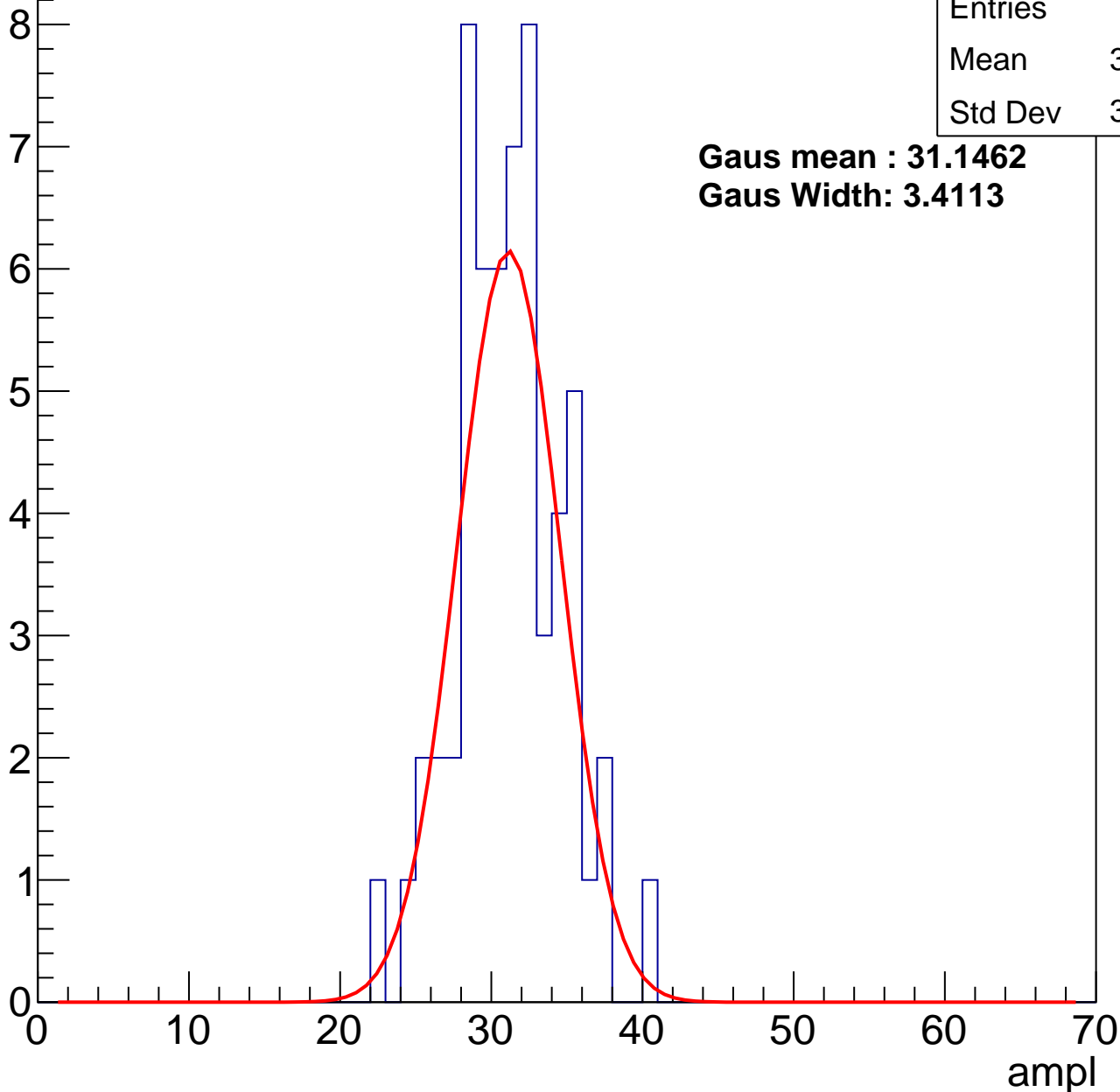
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	30.73
Std Dev	3.434

**Gaus mean : 31.1462**

**Gaus Width: 3.4113**



# B1L101S, U8-ch125, adc1

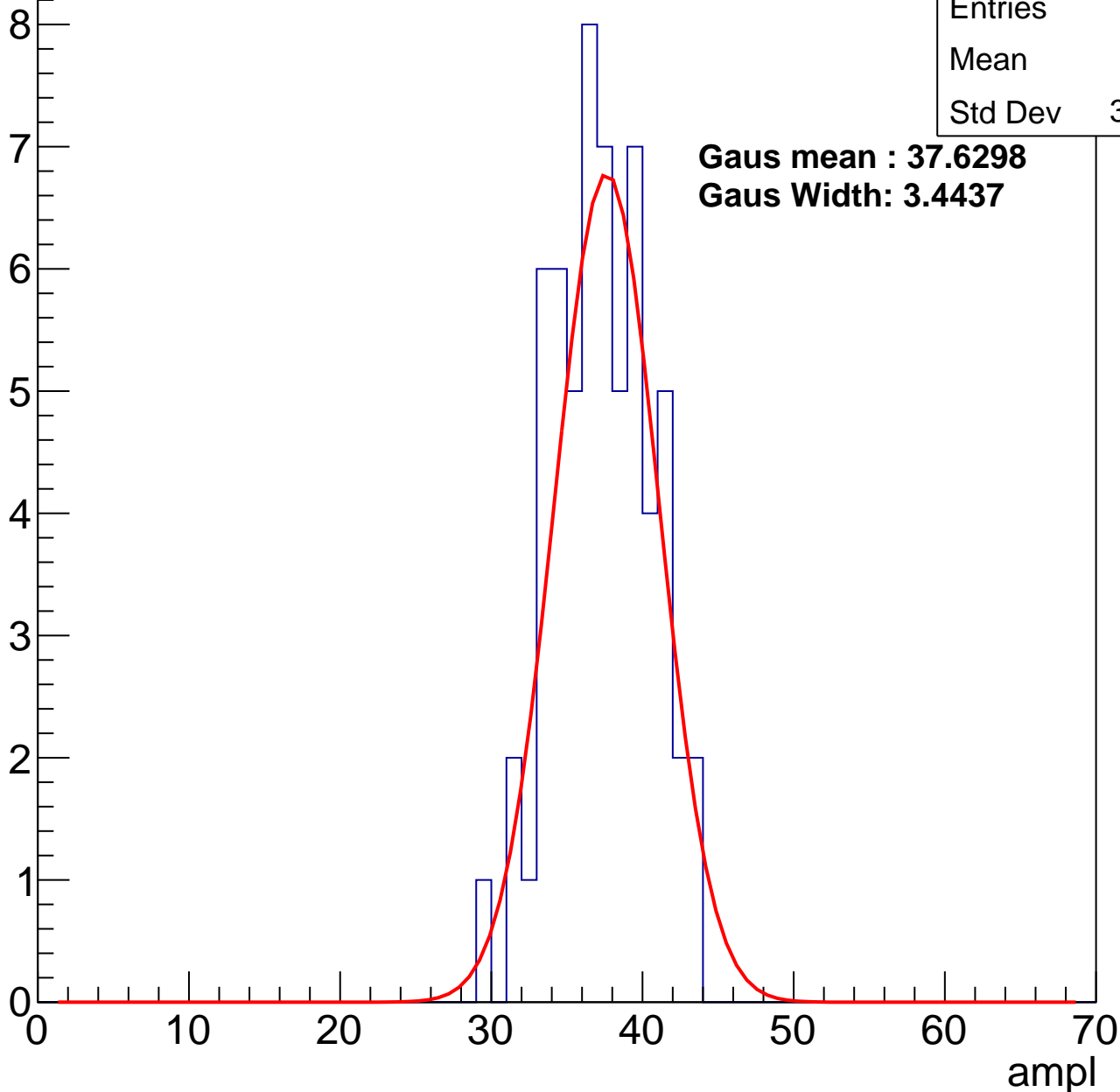
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	36.8
Std Dev	3.156

**Gaus mean : 37.6298**

**Gaus Width: 3.4437**



# B1L101S, U8-ch125, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	43.65
Std Dev	3.577

**Gaus mean : 44.6380**

**Gaus Width: 3.7552**

10

8

6

4

2

0

0

2

4

6

8

10

ampl

70

60

50

40

30

20

10

0

0

2

4

6

8

10

0

2

4

6

8

10

0

2

4

6

8

10

# B1L101S, U8-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	58
Mean	51
Std Dev	3.454

Entry

10

8

6

4

2

0

0

10

20

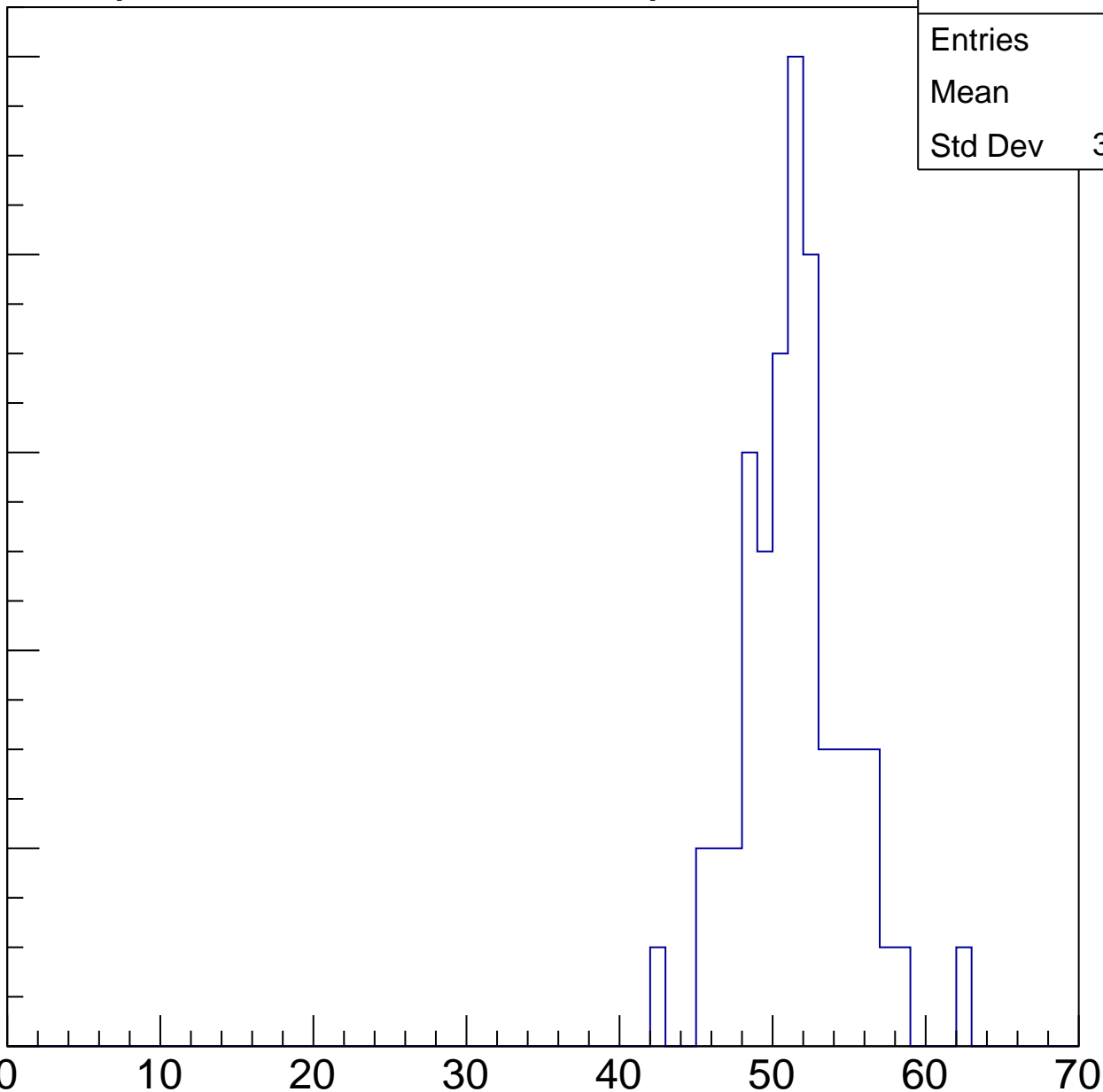
30

40

50

60

ampl

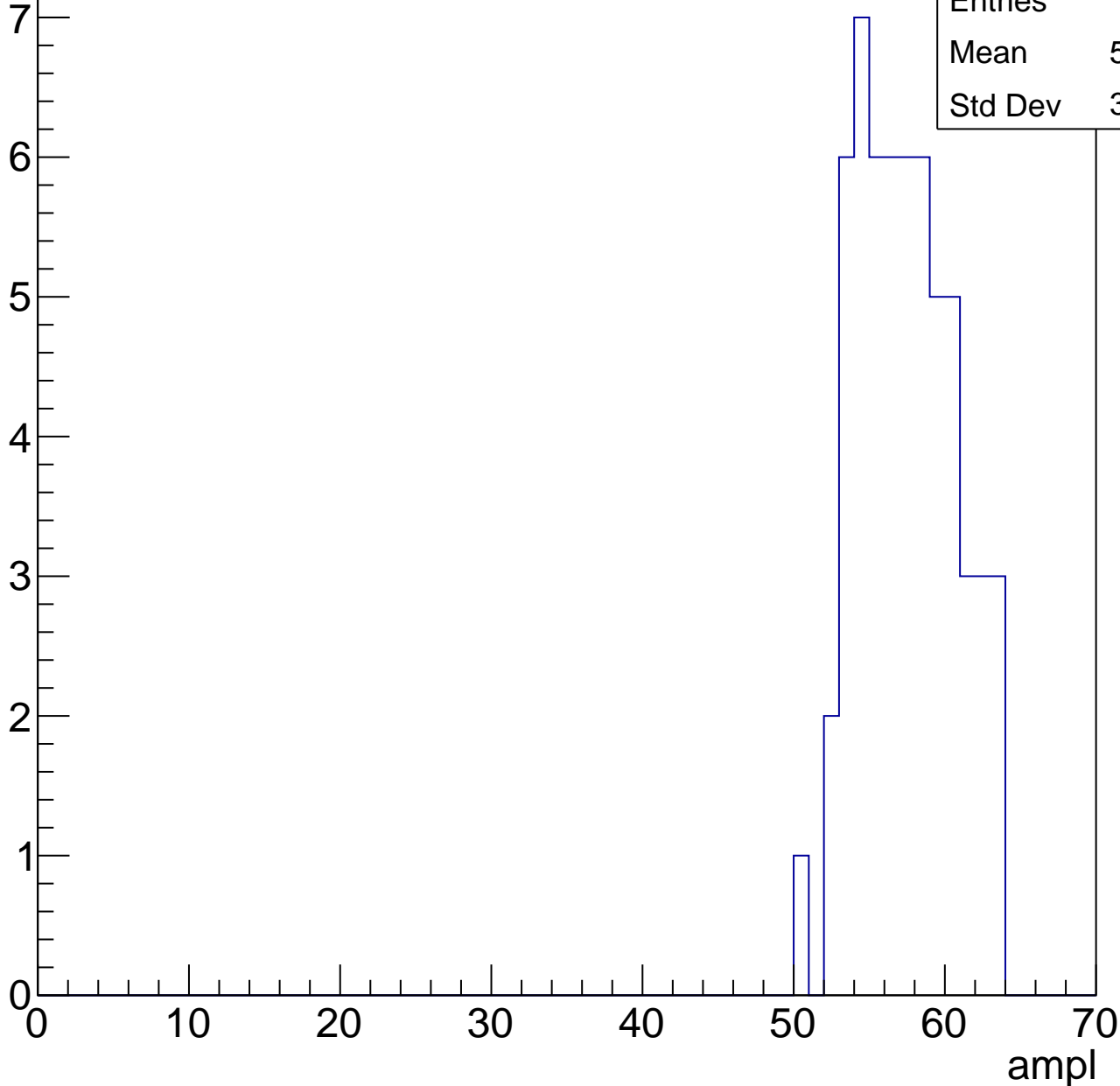


# B1L101S, U8-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	56.93
Std Dev	3.162

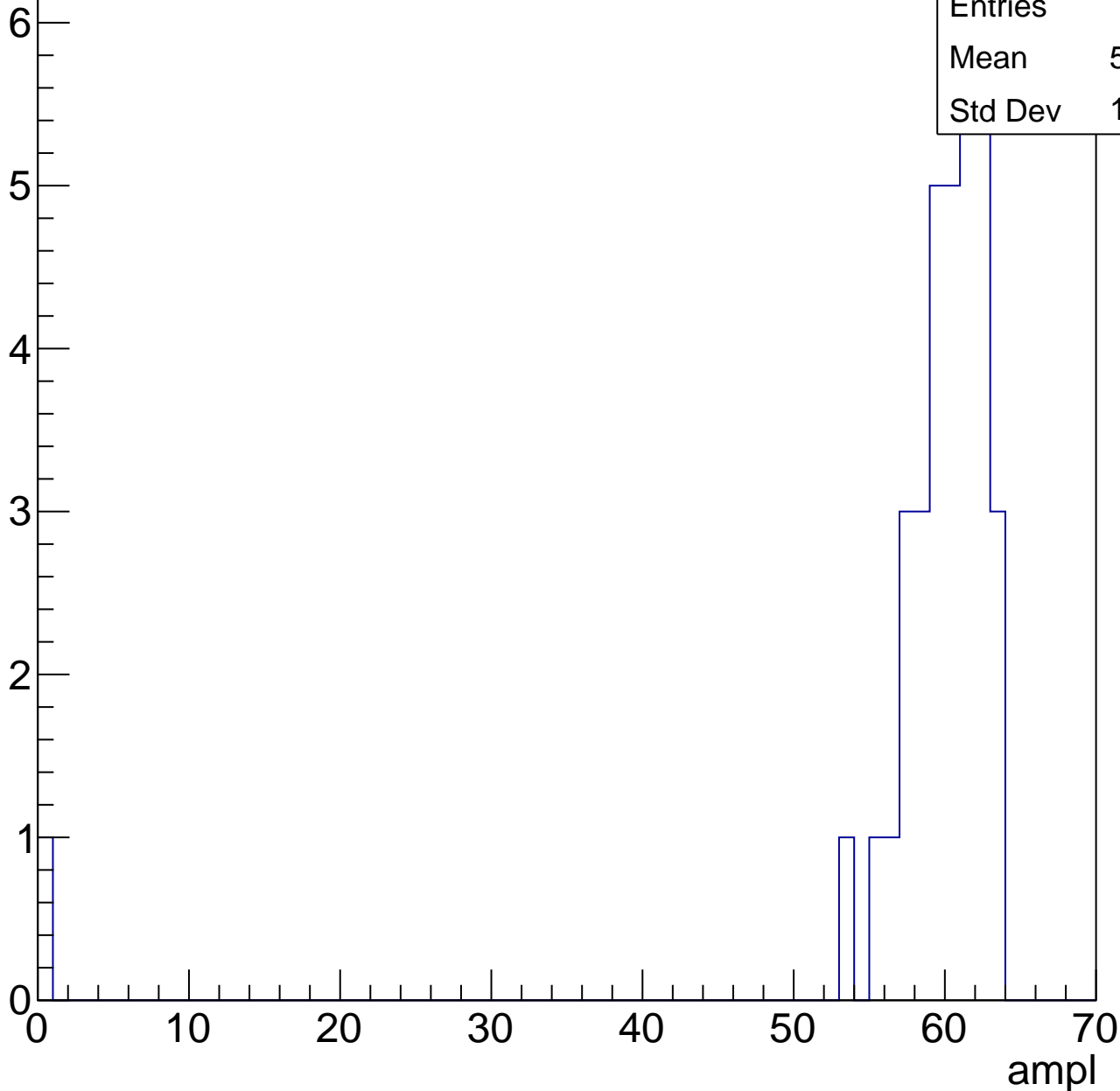


# B1L101S, U8-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

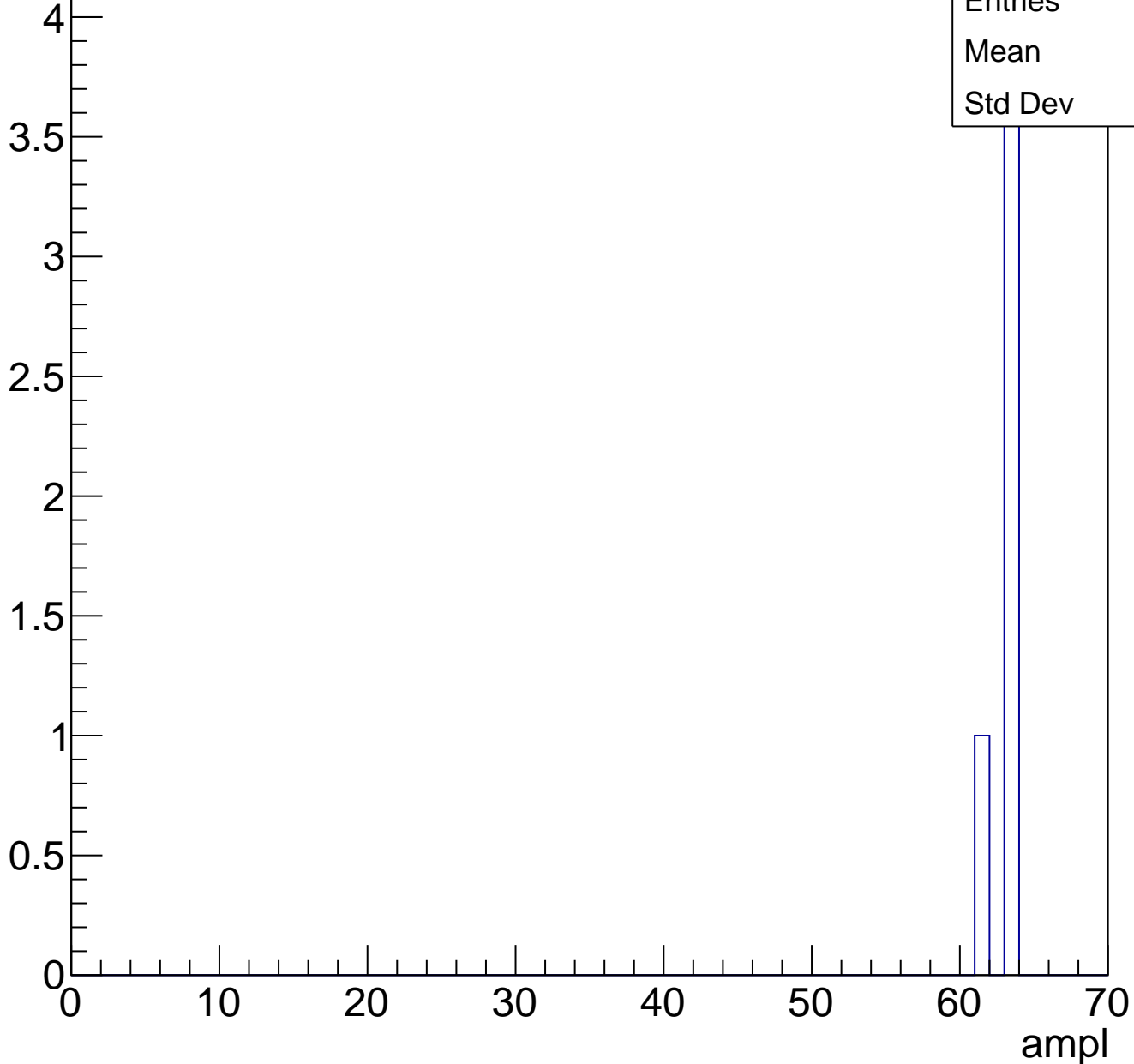
Entries	35
Mean	58.03
Std Dev	10.22



# B1L101S, U8-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U8-ch126, adc0

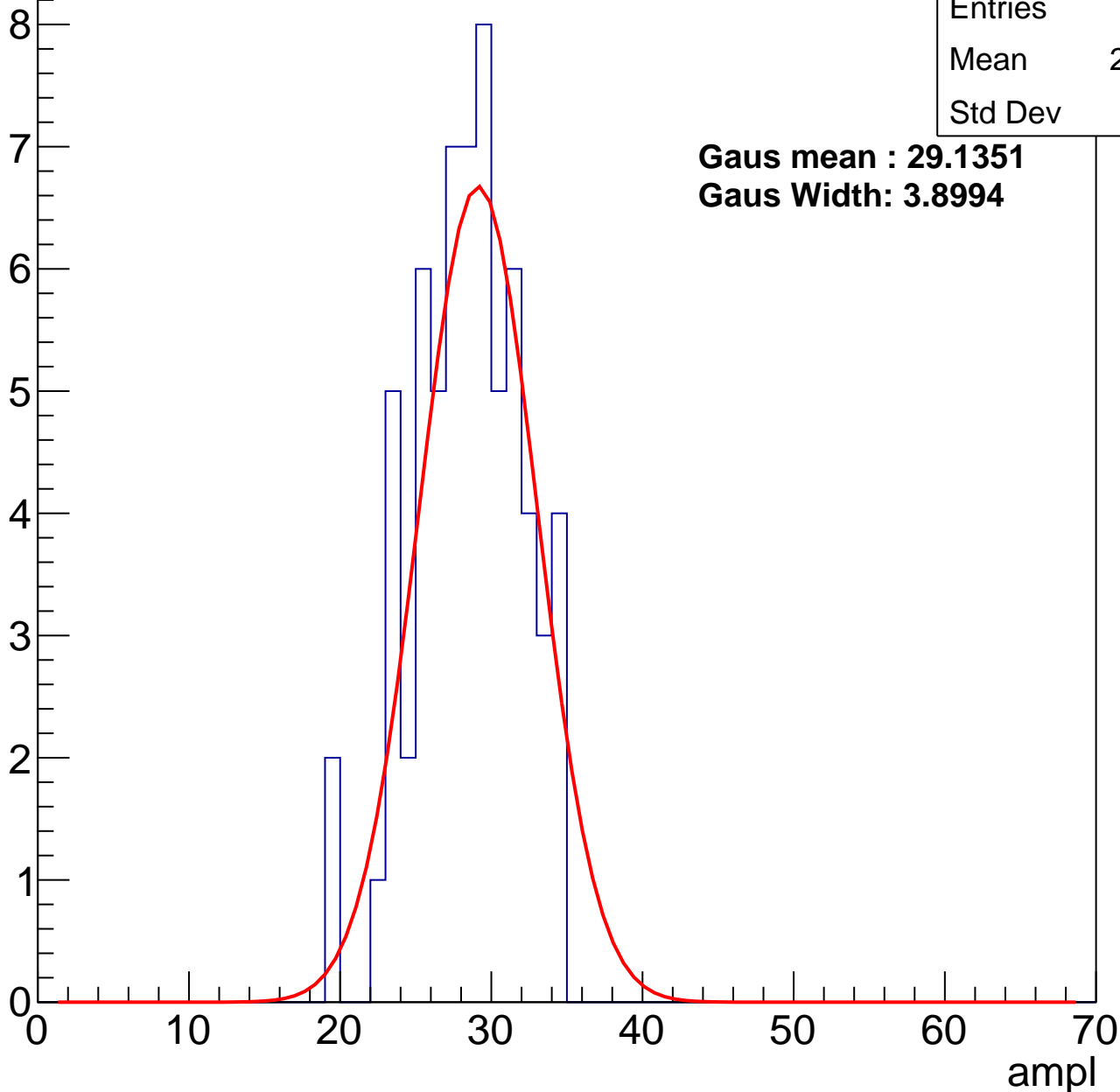
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	27.98
Std Dev	3.51

**Gaus mean : 29.1351**

**Gaus Width: 3.8994**



# B1L101S, U8-ch126, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	79
Mean	35.22
Std Dev	3.781

**Gaus mean : 36.2567**

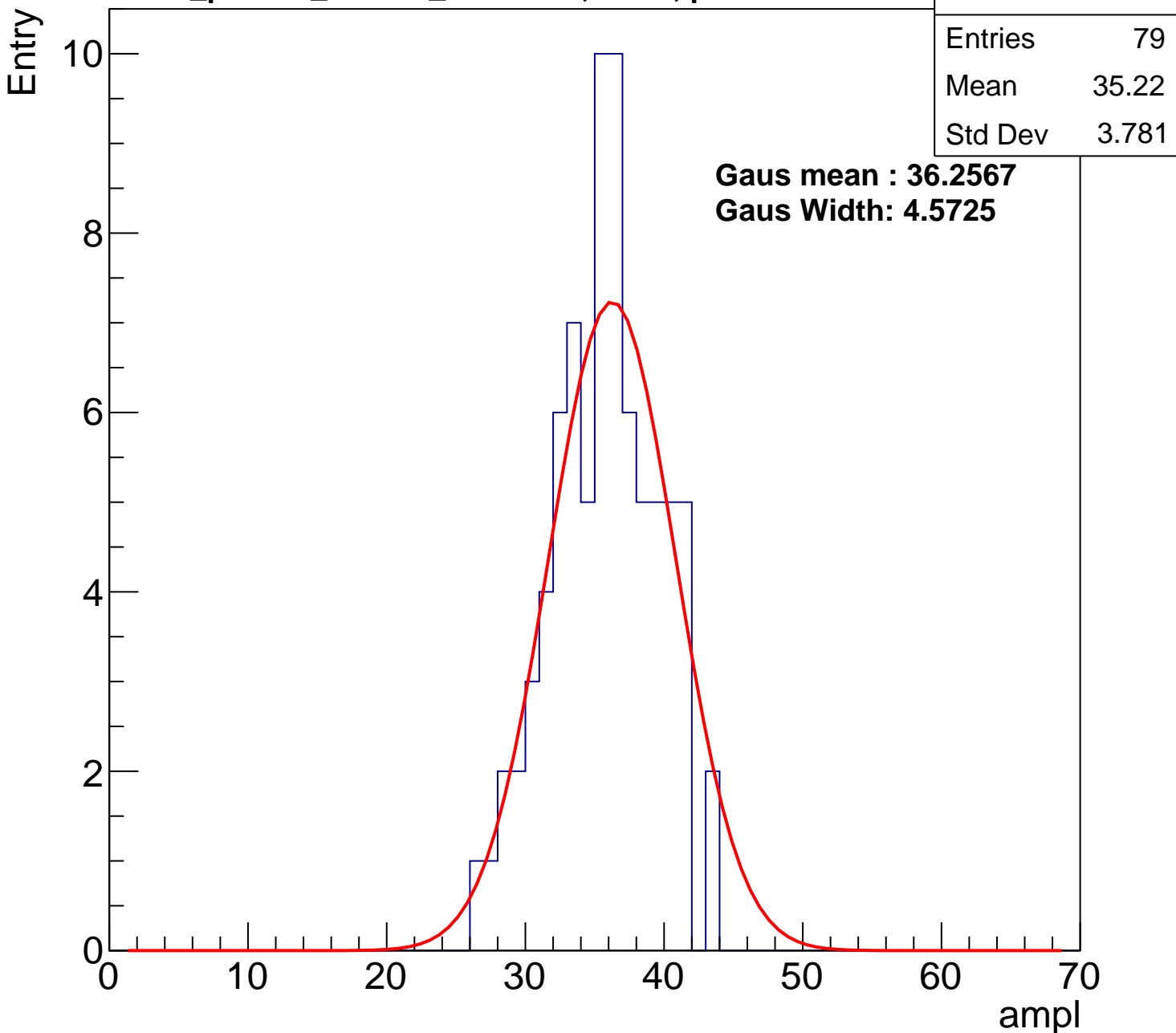
**Gaus Width: 4.5725**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U8-ch126, adc2

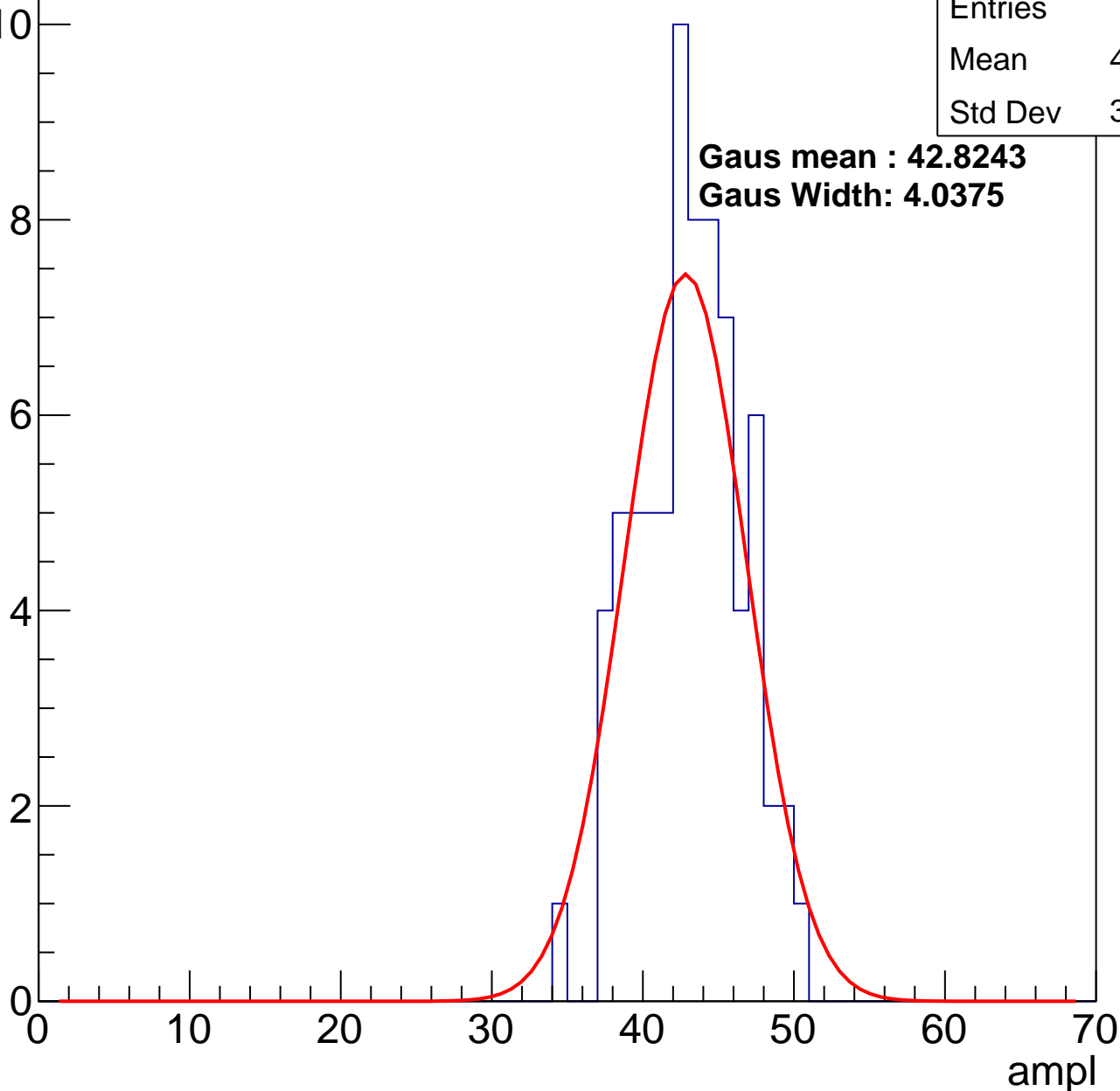
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	42.64
Std Dev	3.382

**Gaus mean : 42.8243**

**Gaus Width: 4.0375**

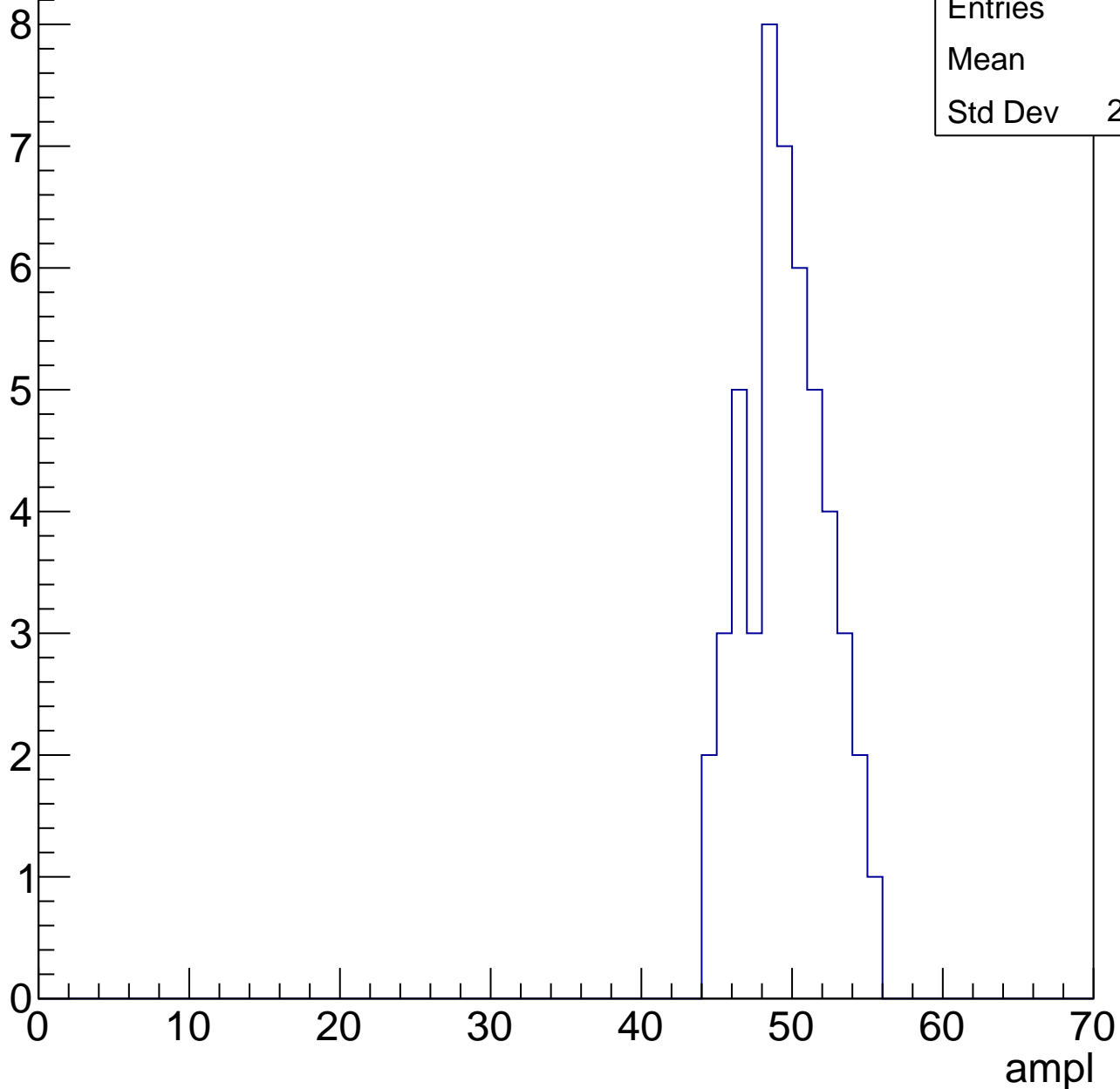


# B1L101S, U8-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	49.1
Std Dev	2.705

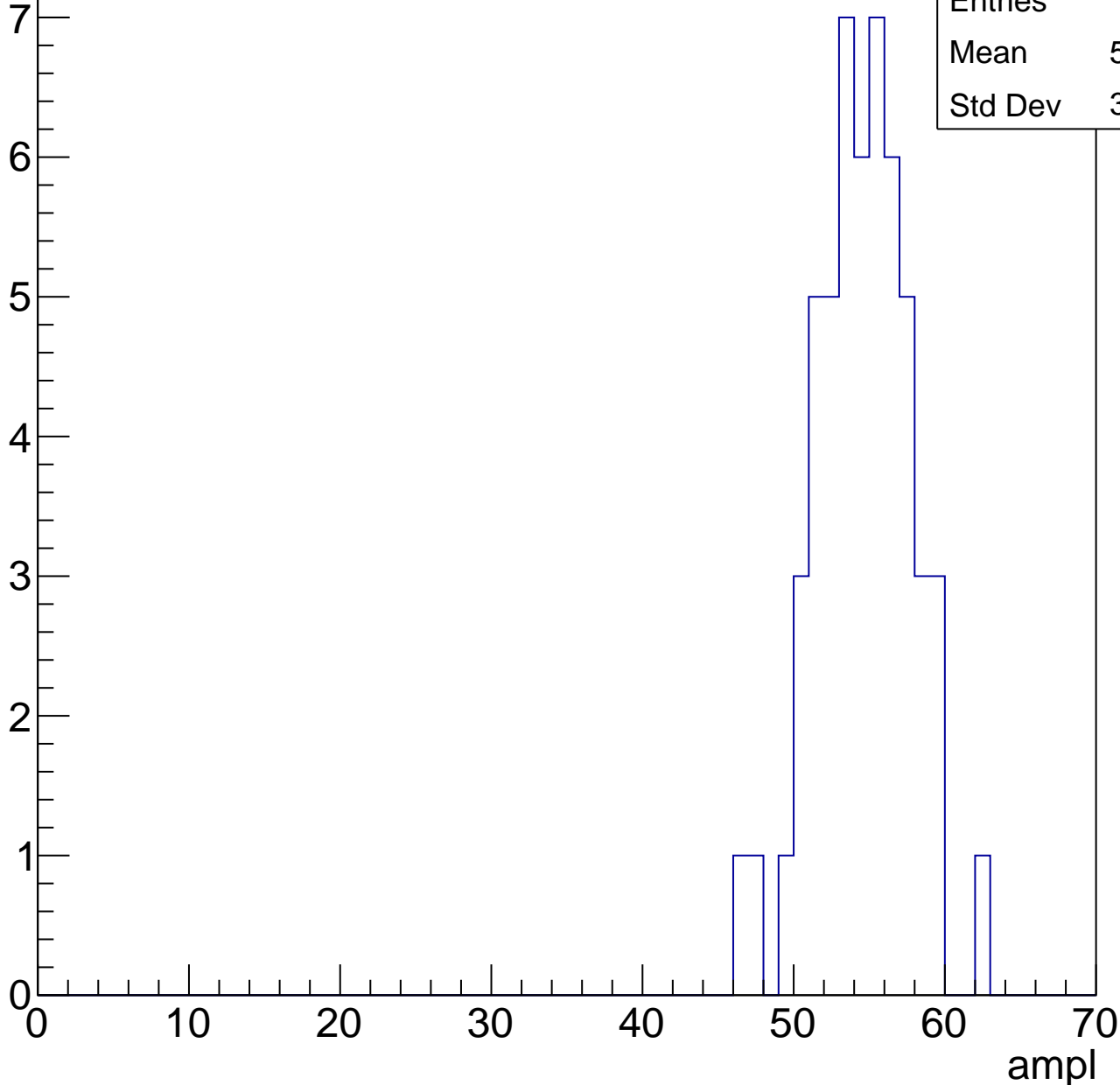


# B1L101S, U8-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	54.09
Std Dev	3.105



# B1L101S, U8-ch126, adc5

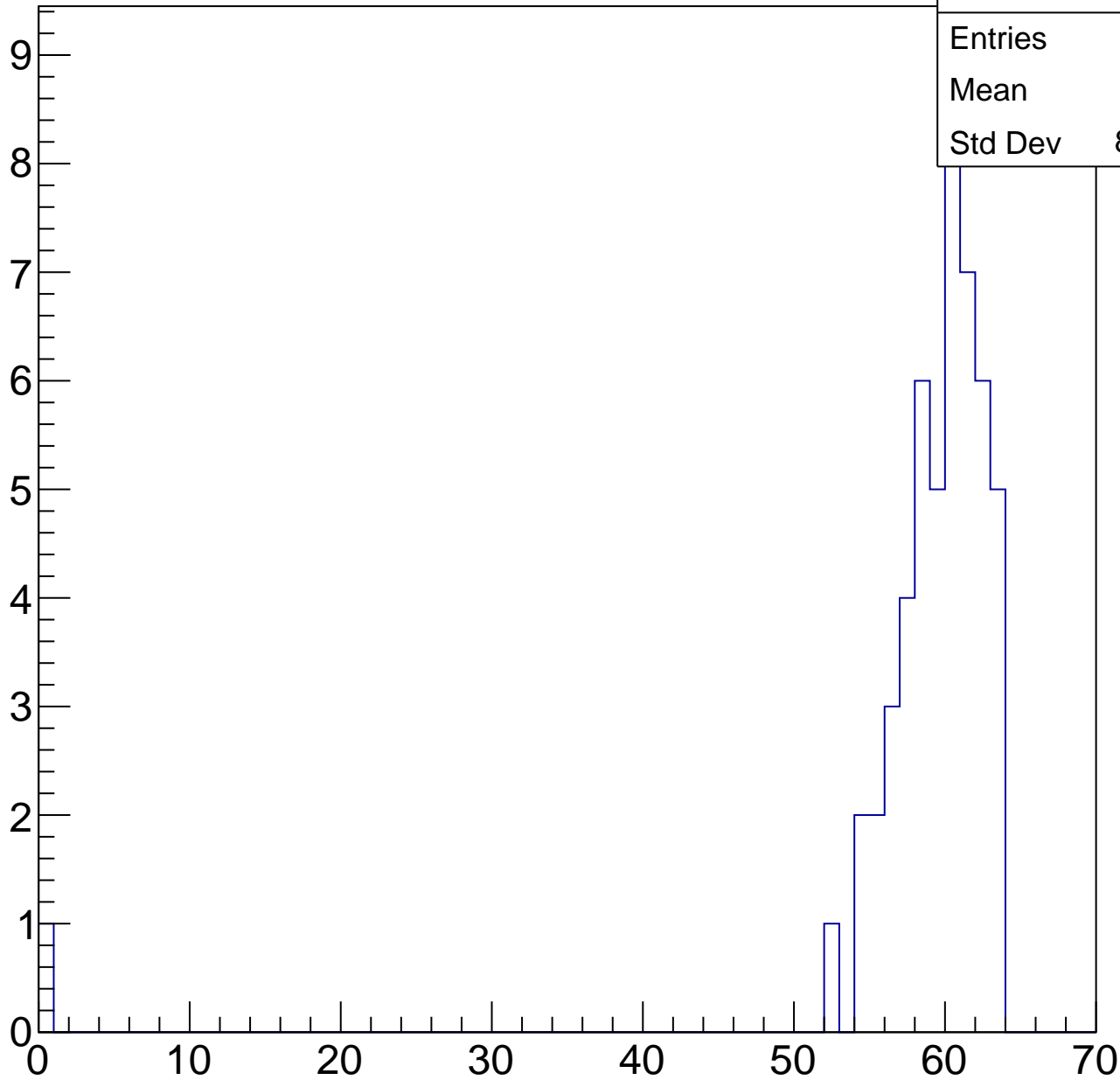
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	58.1
Std Dev	8.621

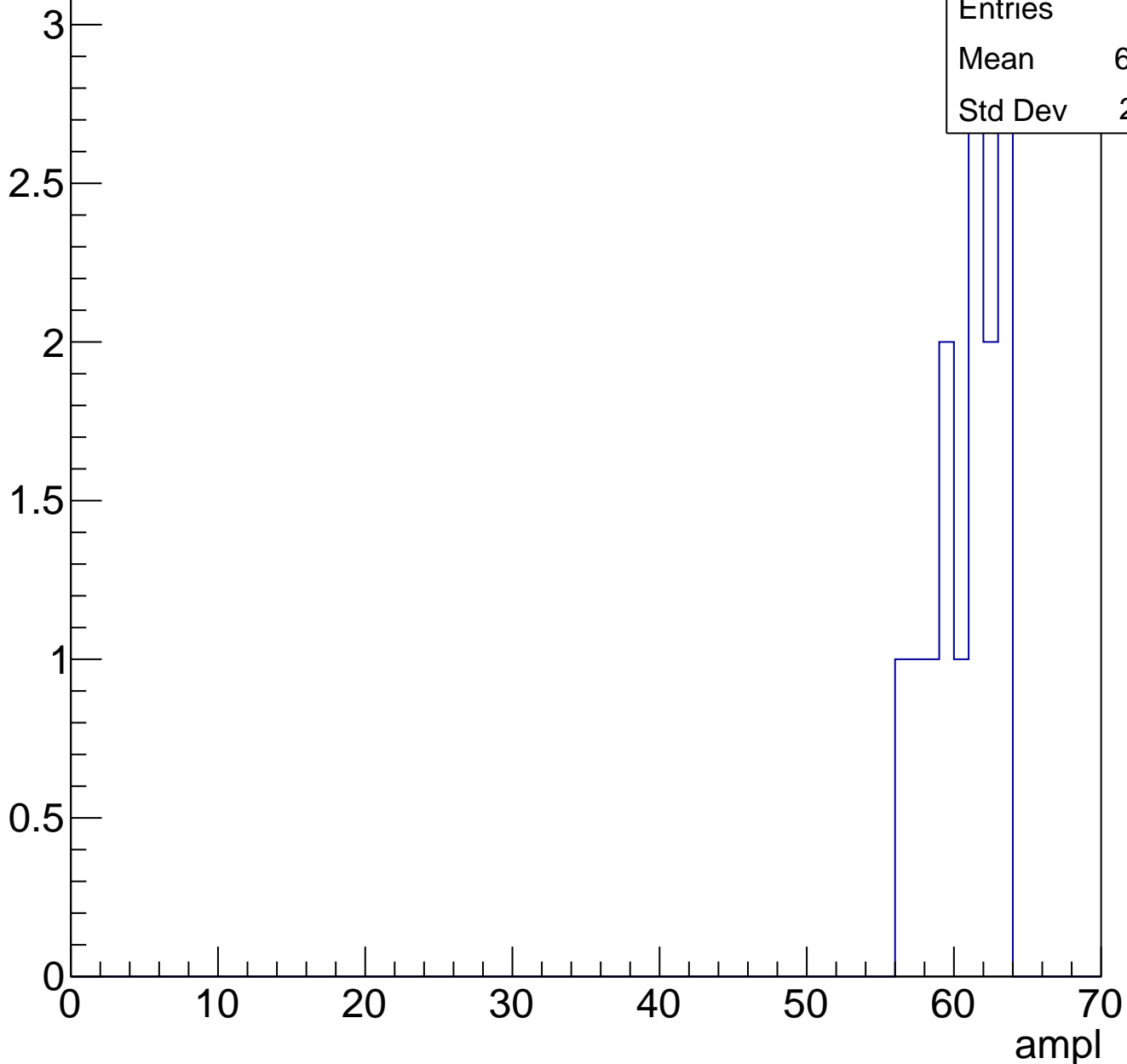
ampl



# B1L101S, U8-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U8-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U8-ch127, adc0

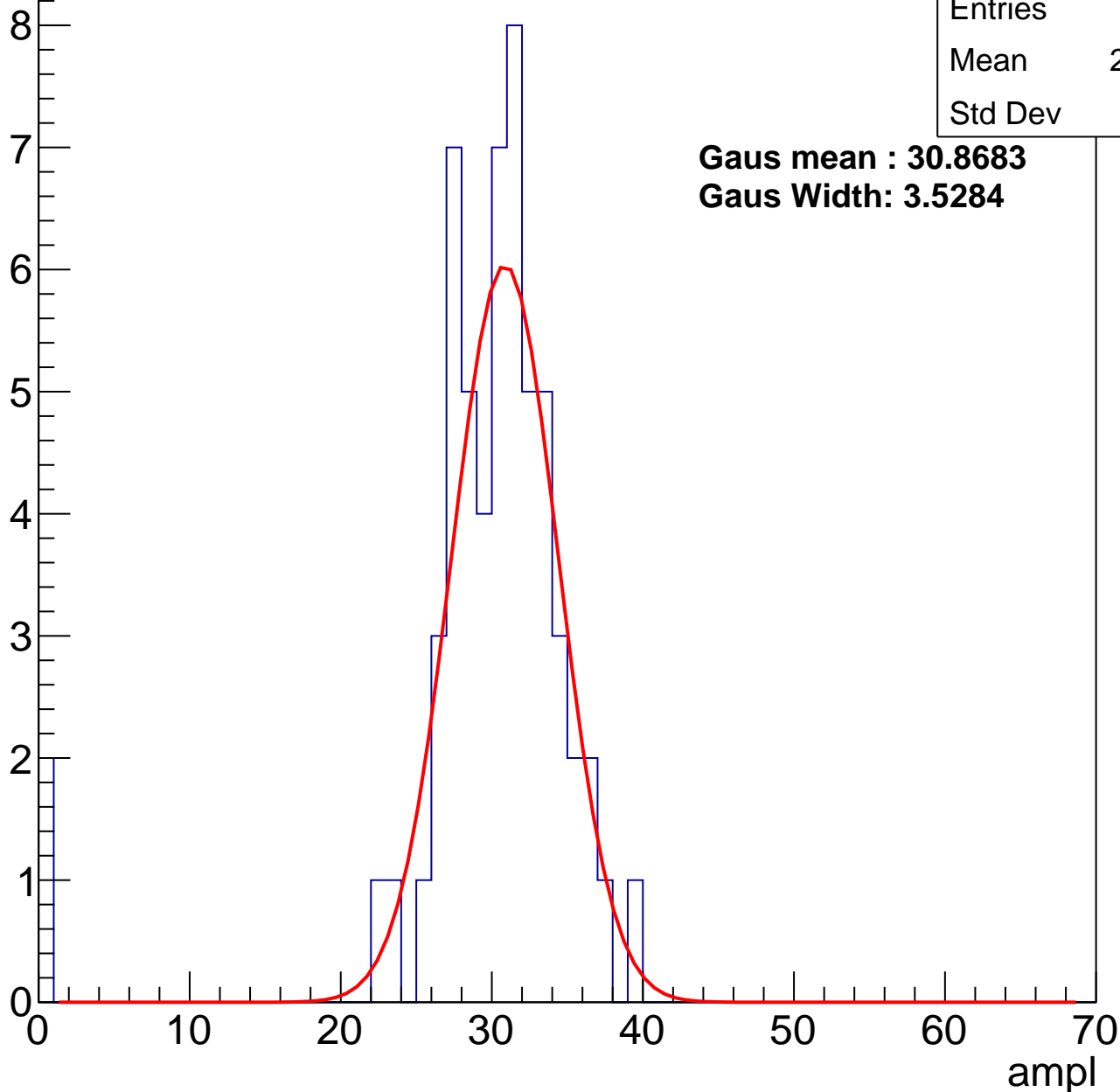
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	29.24
Std Dev	6.45

**Gaus mean : 30.8683**

**Gaus Width: 3.5284**



# B1L101S, U8-ch127, adc1

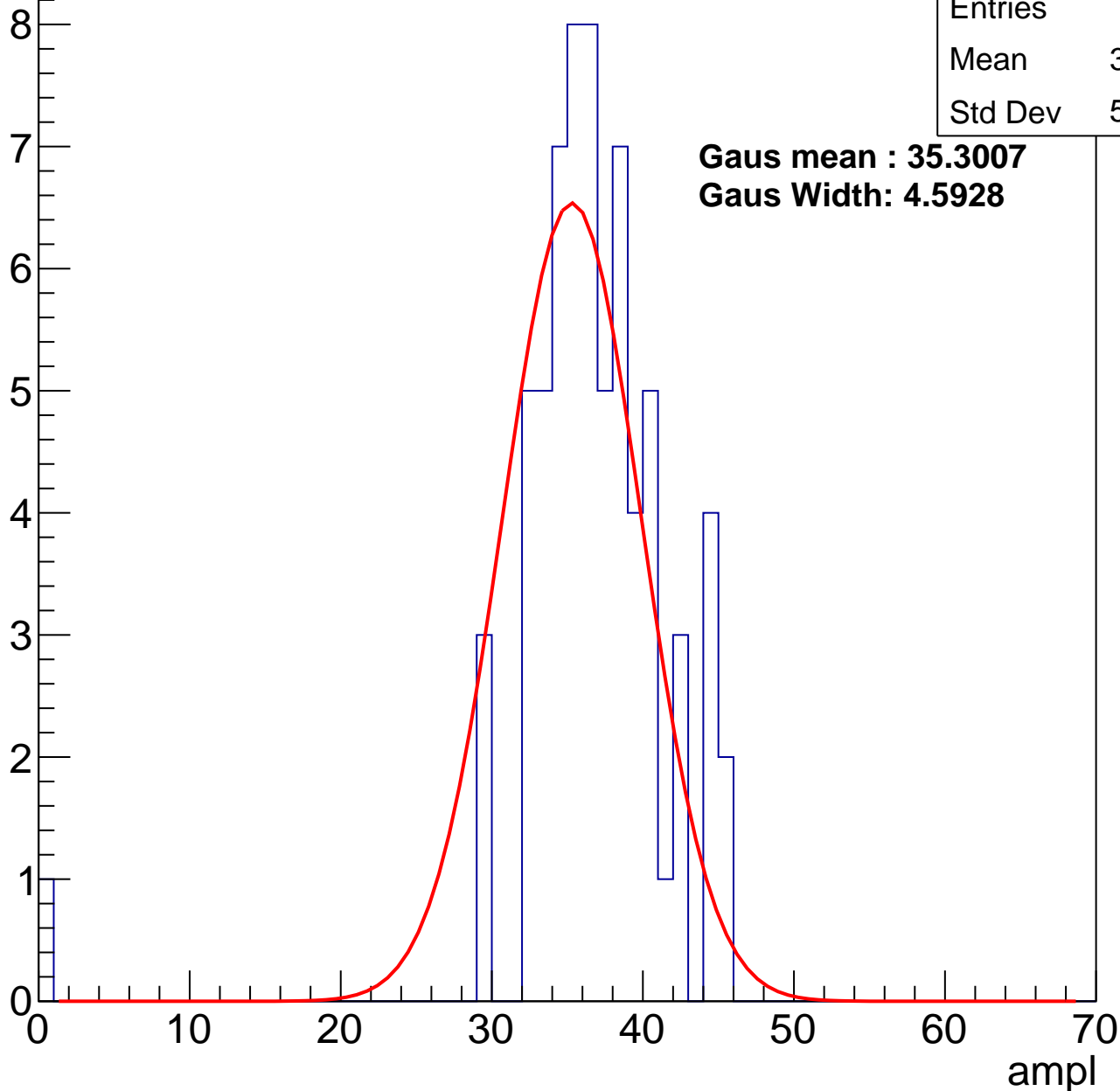
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	36.15
Std Dev	5.819

**Gaus mean : 35.3007**

**Gaus Width: 4.5928**



# B1L101S, U8-ch127, adc2

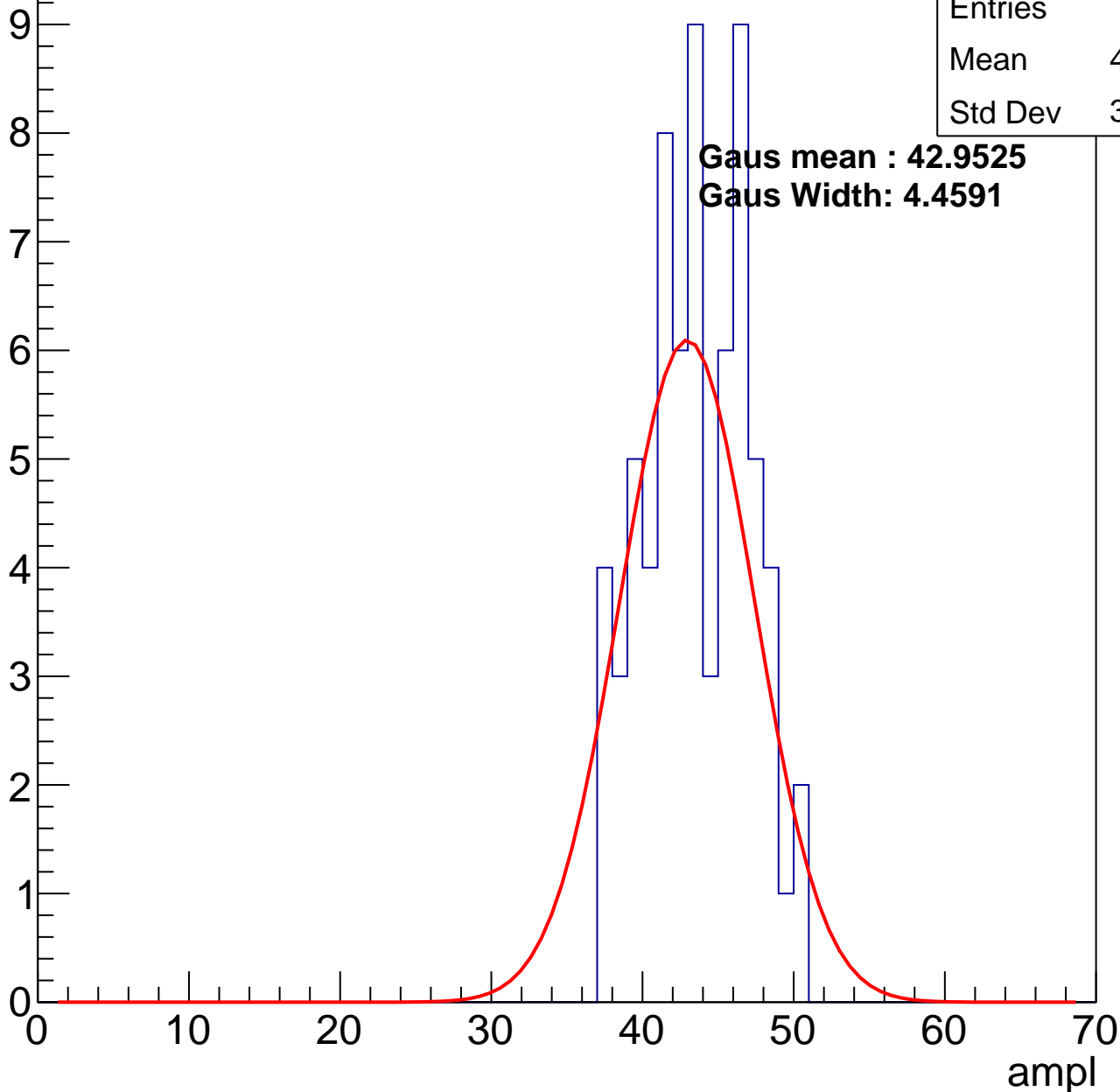
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	43.13
Std Dev	3.392

**Gaus mean : 42.9525**

**Gaus Width: 4.4591**

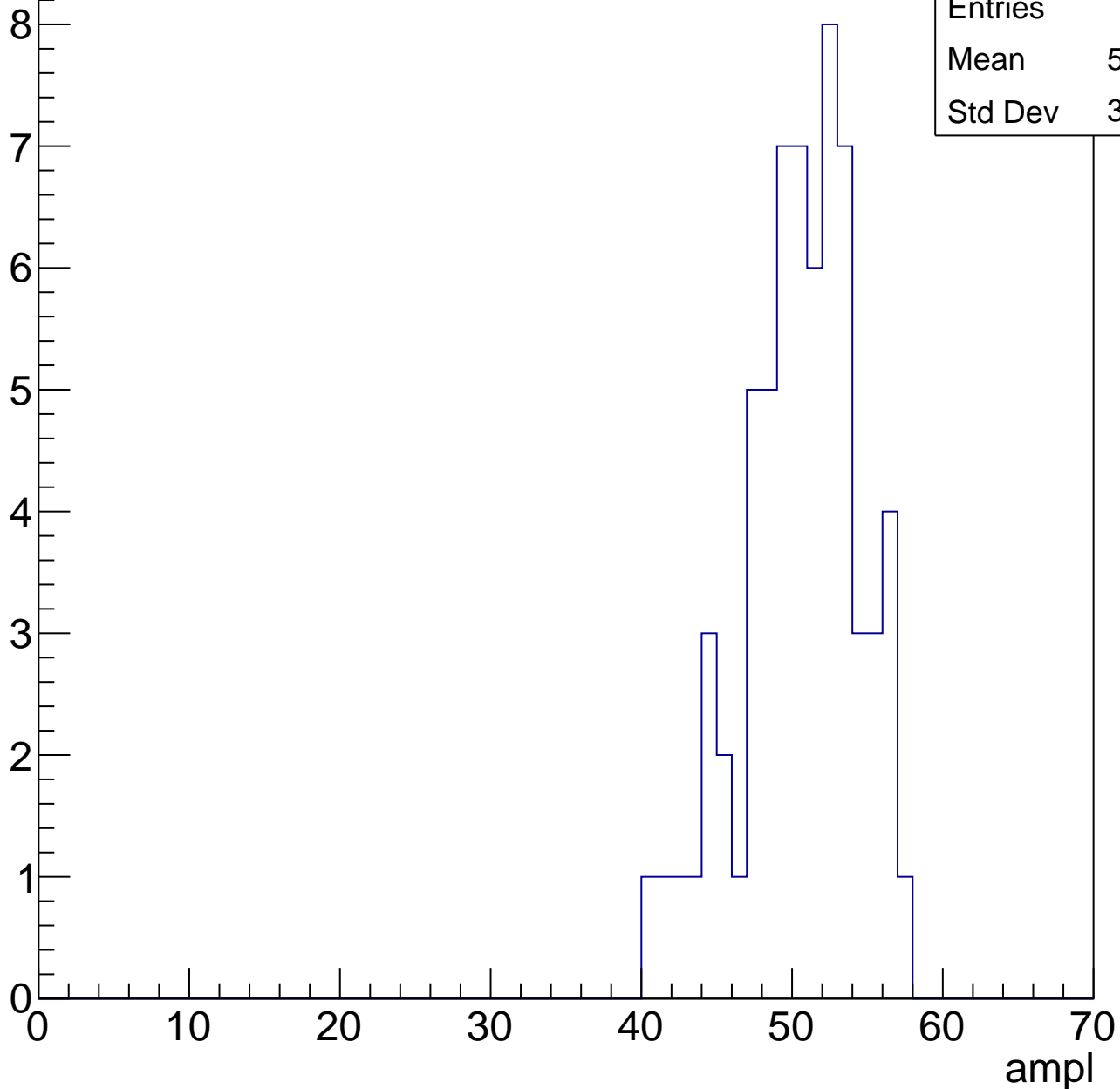


# B1L101S, U8-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	50.05
Std Dev	3.808

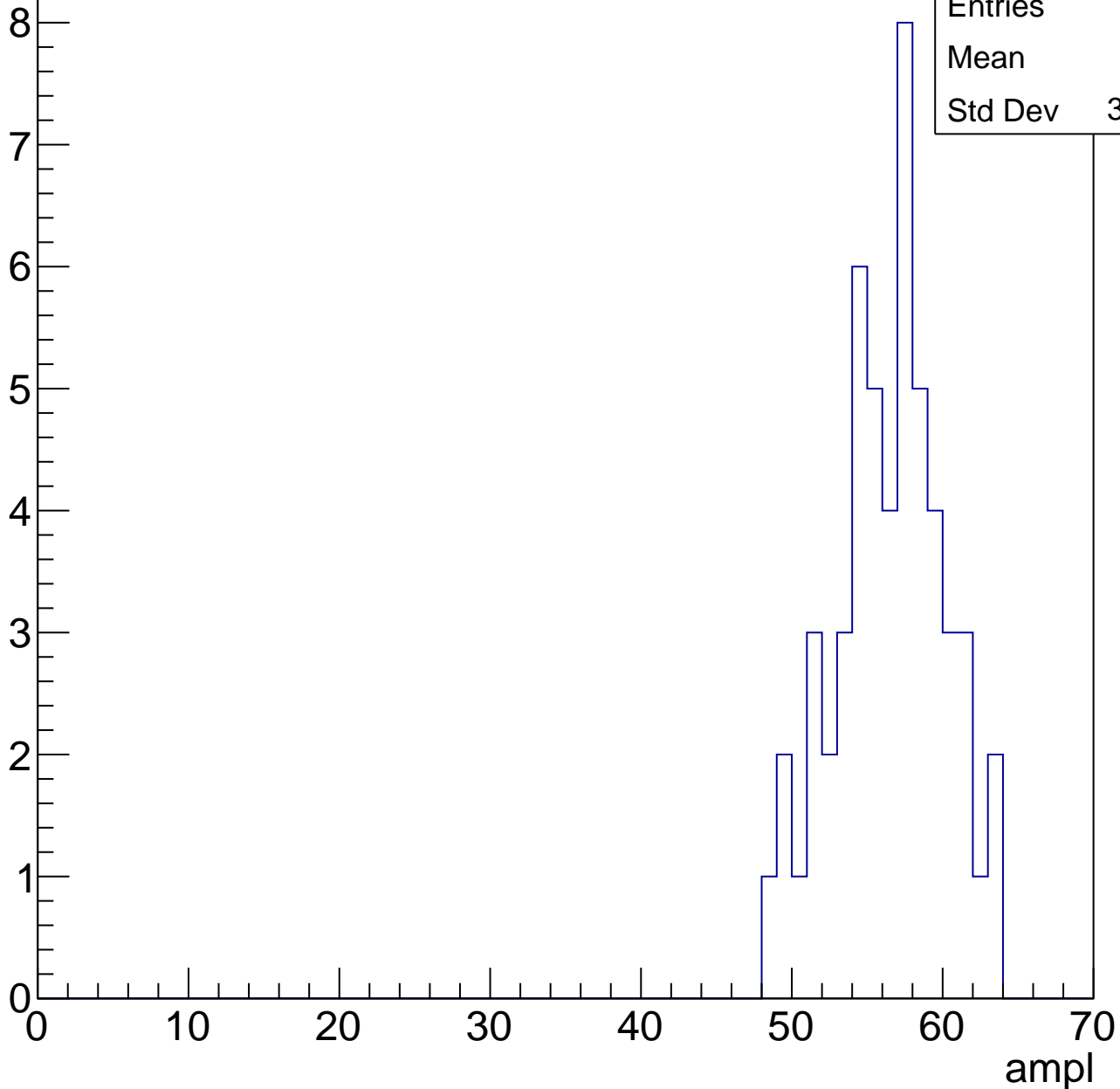


# B1L101S, U8-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	56
Std Dev	3.587

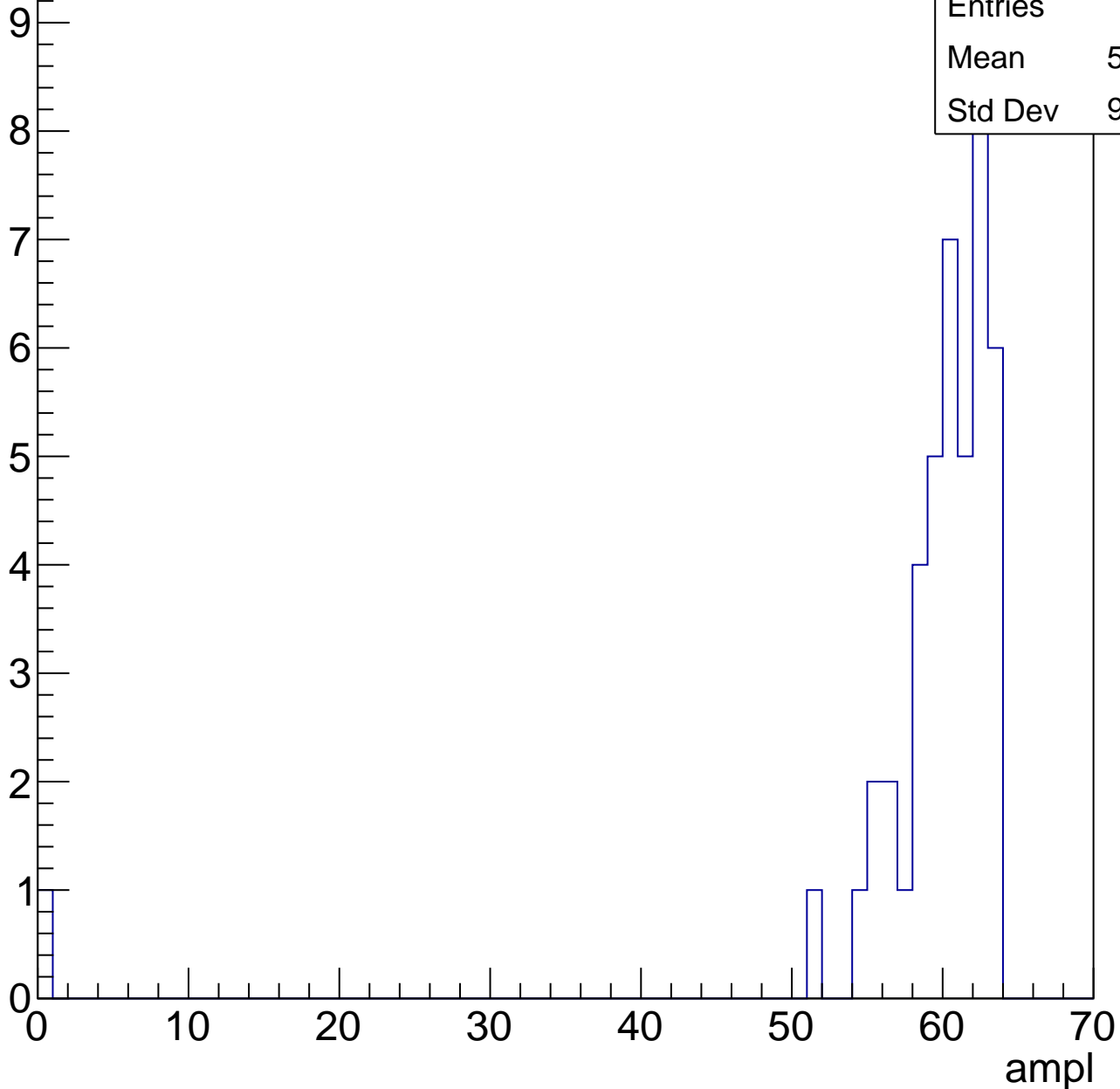


# B1L101S, U8-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	44
Mean	58.45
Std Dev	9.316



# B1L101S, U8-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	60.83
Std Dev	1.863

ampl

0 10 20 30 40 50 60 70

0



# B1L101S, U8-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

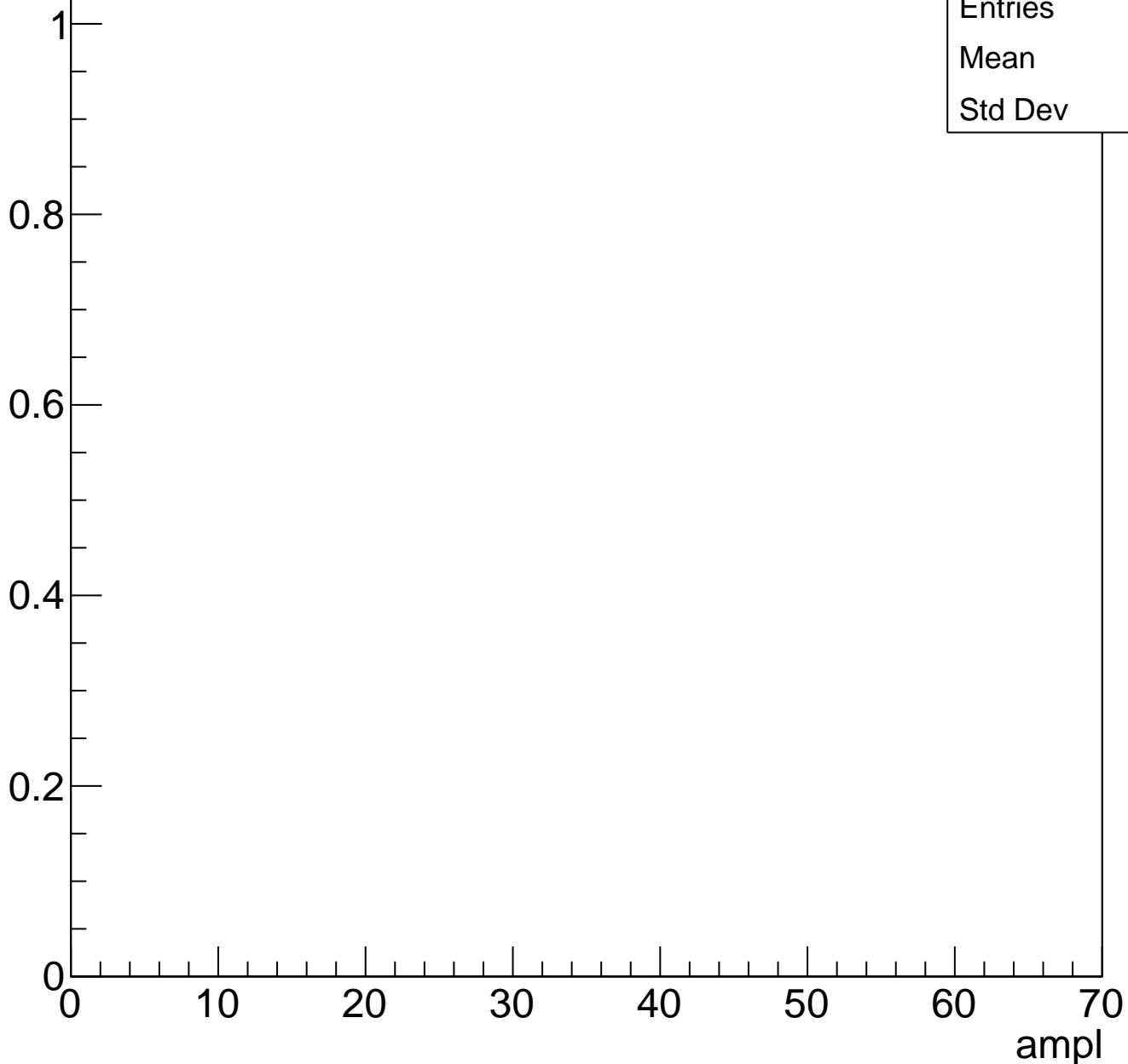


Entries	0
Mean	0
Std Dev	0

# B1L101S, U8-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0