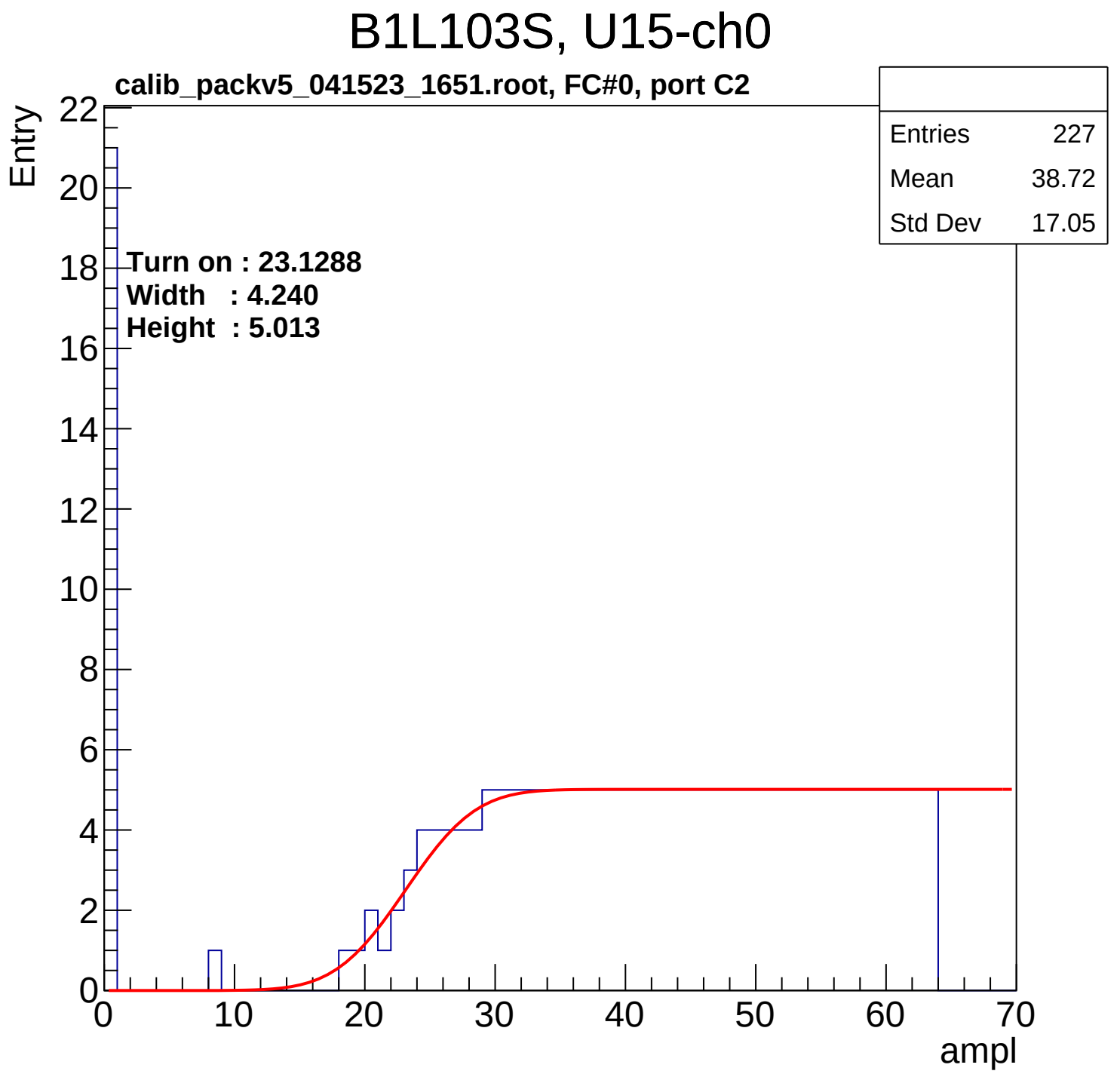
B1L103S, U15-ch0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 227
Mean 38.72
Std Dev 17.05
Turn on : 23.1288
Width : 4.240
Height : 5.013
Entry
ampl
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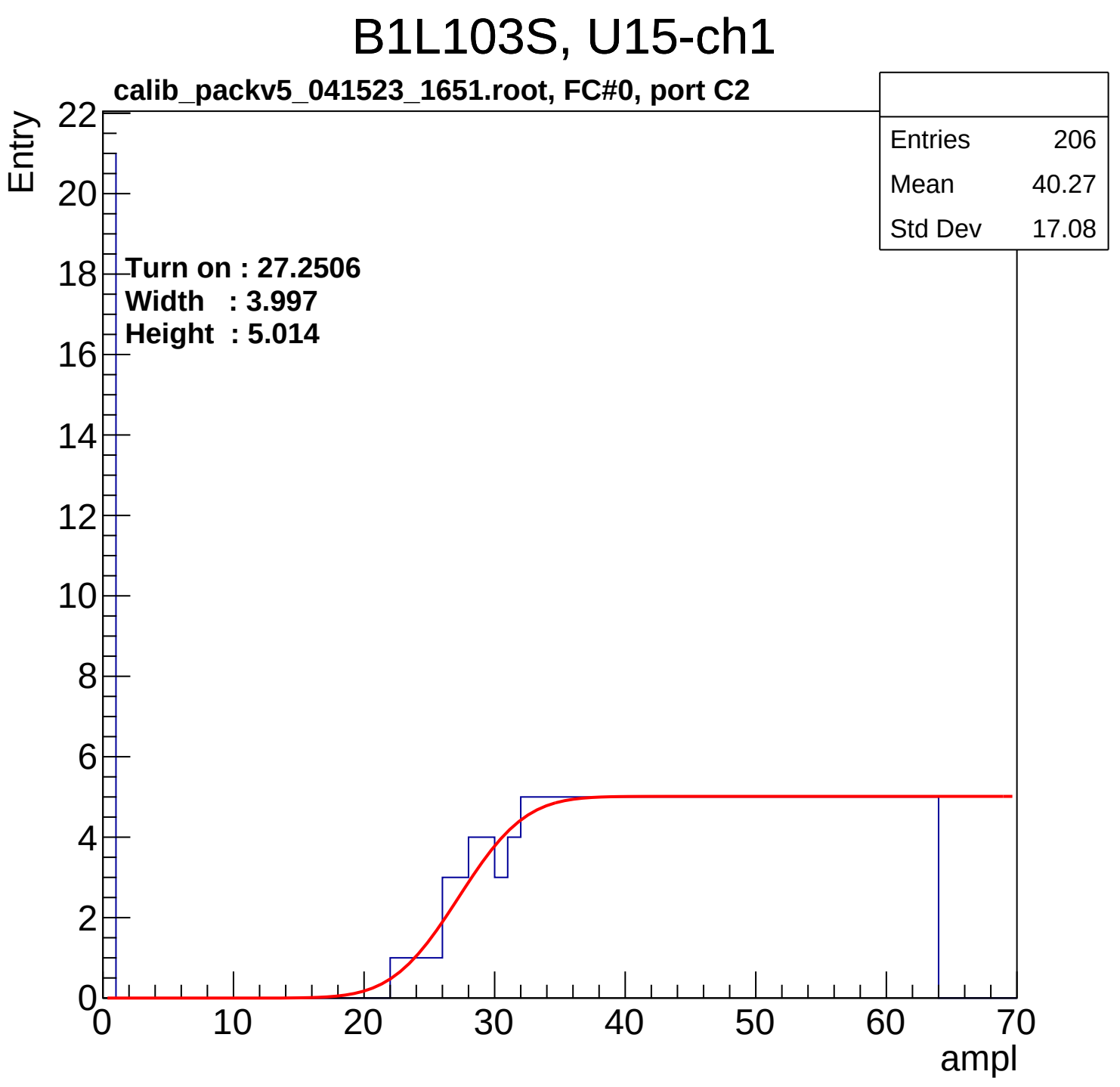
B1L103S, U15-ch1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 206
Mean 40.27
Std Dev 17.08
Turn on : 27.2506
Width : 3.997
Height : 5.014
Entry
ampl
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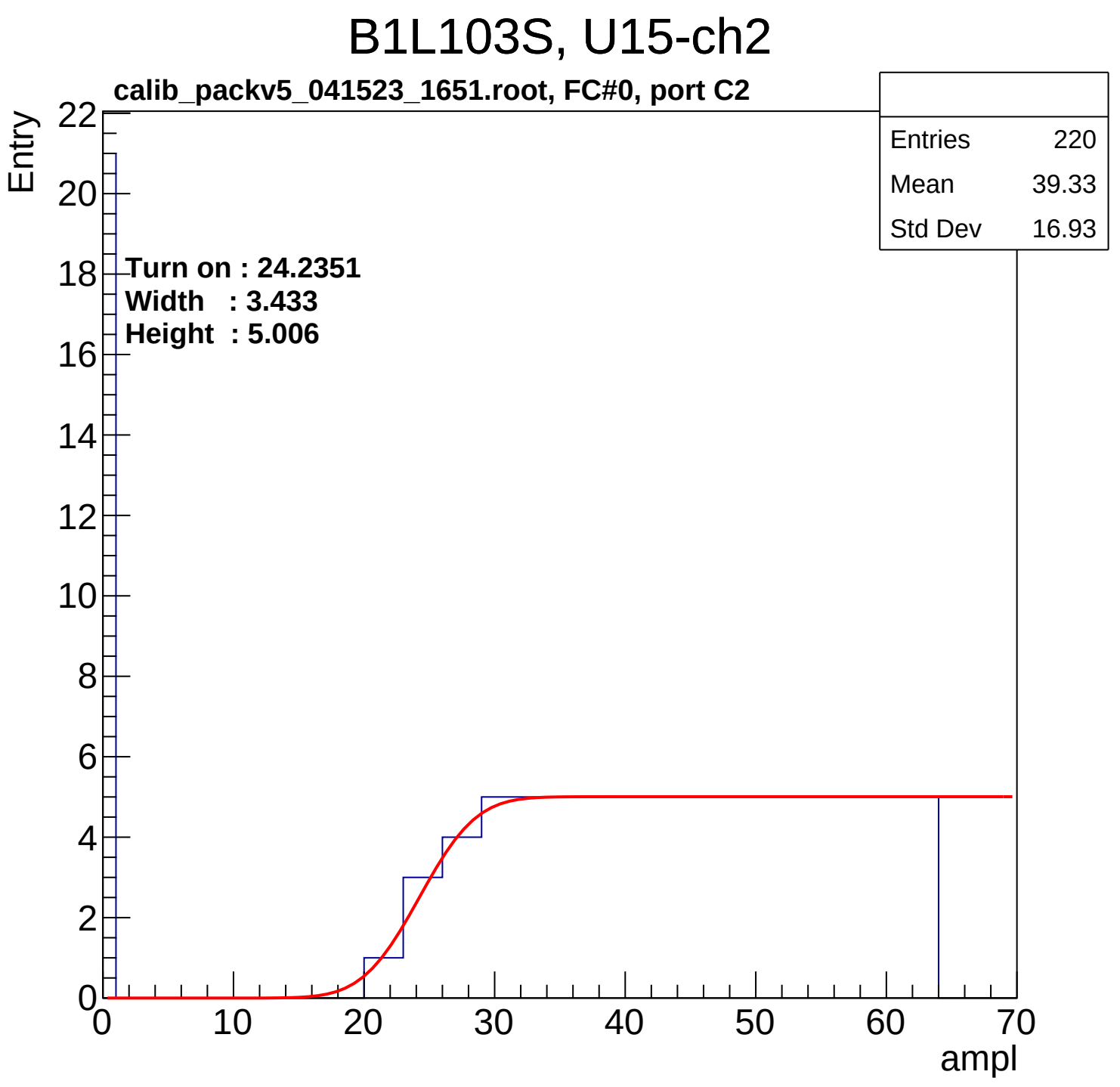
B1L103S, U15-ch2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 220
Mean 39.33
Std Dev 16.93
Turn on : 24.2351
Width : 3.433
Height : 5.006
Entry
ampl
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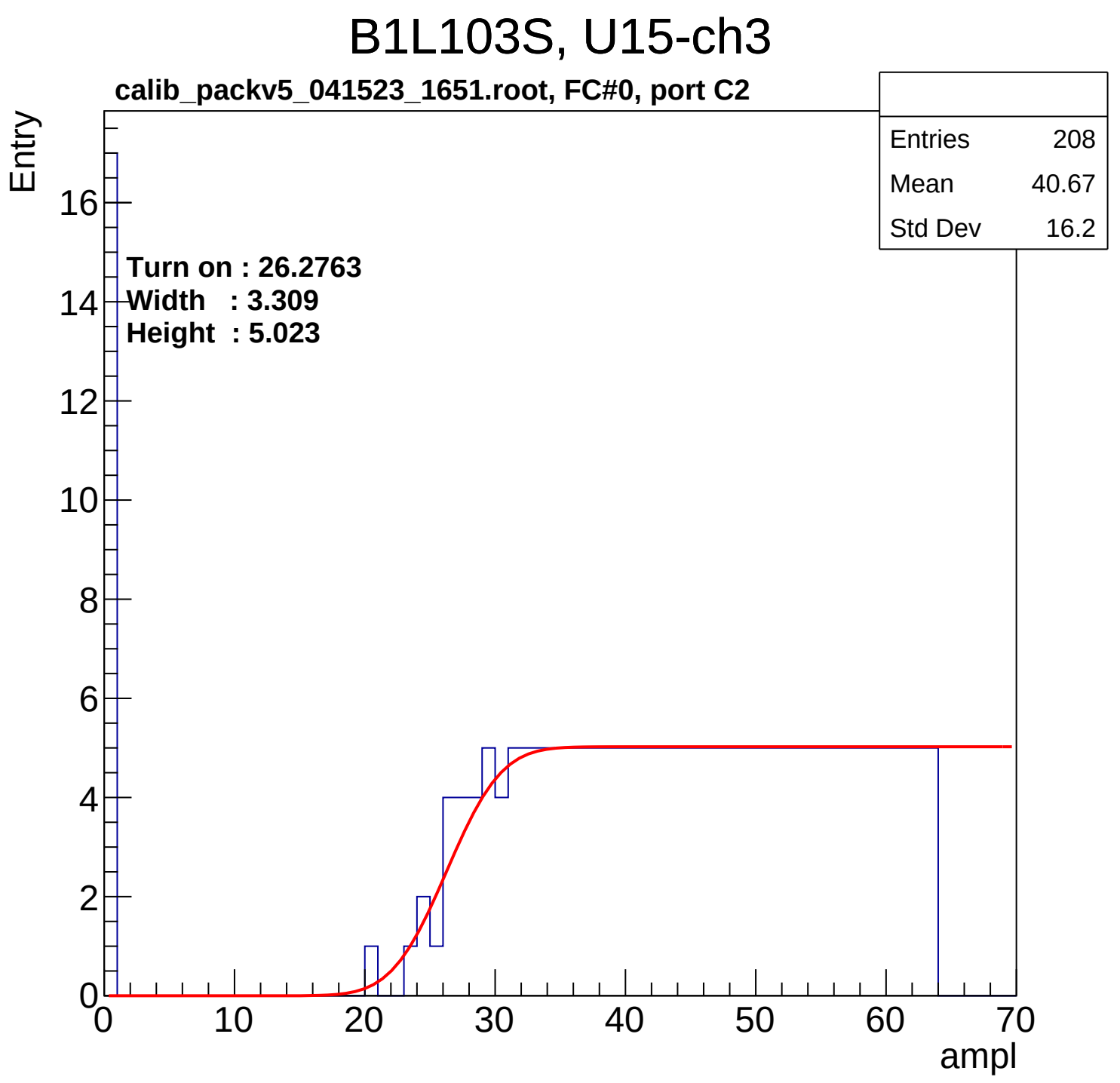
B1L103S, U15-ch3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 208
Mean 40.67
Std Dev 16.2
Turn on : 26.2763
Width : 3.309
Height : 5.023
Entry
ampl
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6
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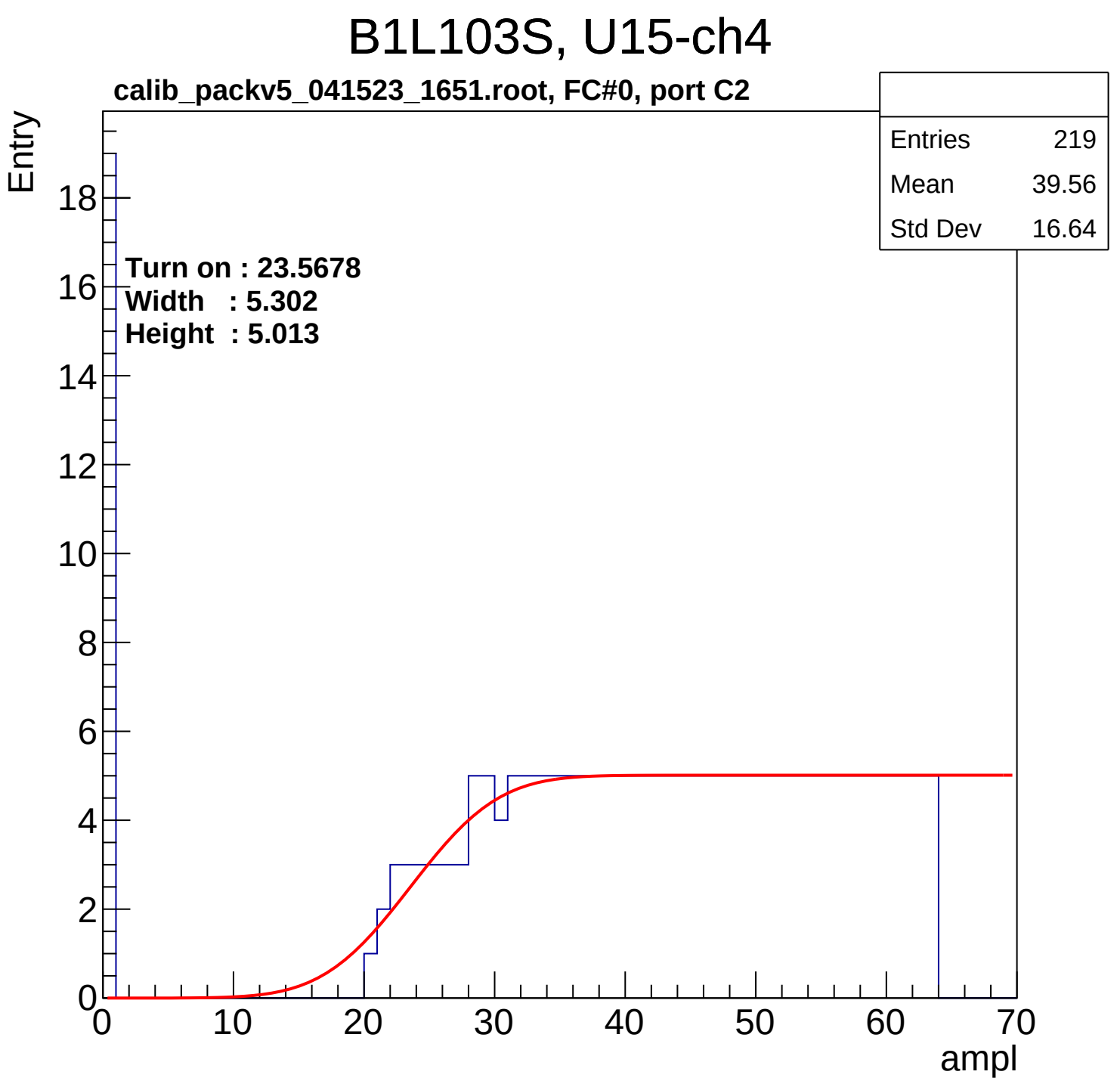
B1L103S, U15-ch4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 219
Mean 39.56
Std Dev 16.64
Turn on : 23.5678
Width : 5.302
Height : 5.013
Entry
ampl
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6
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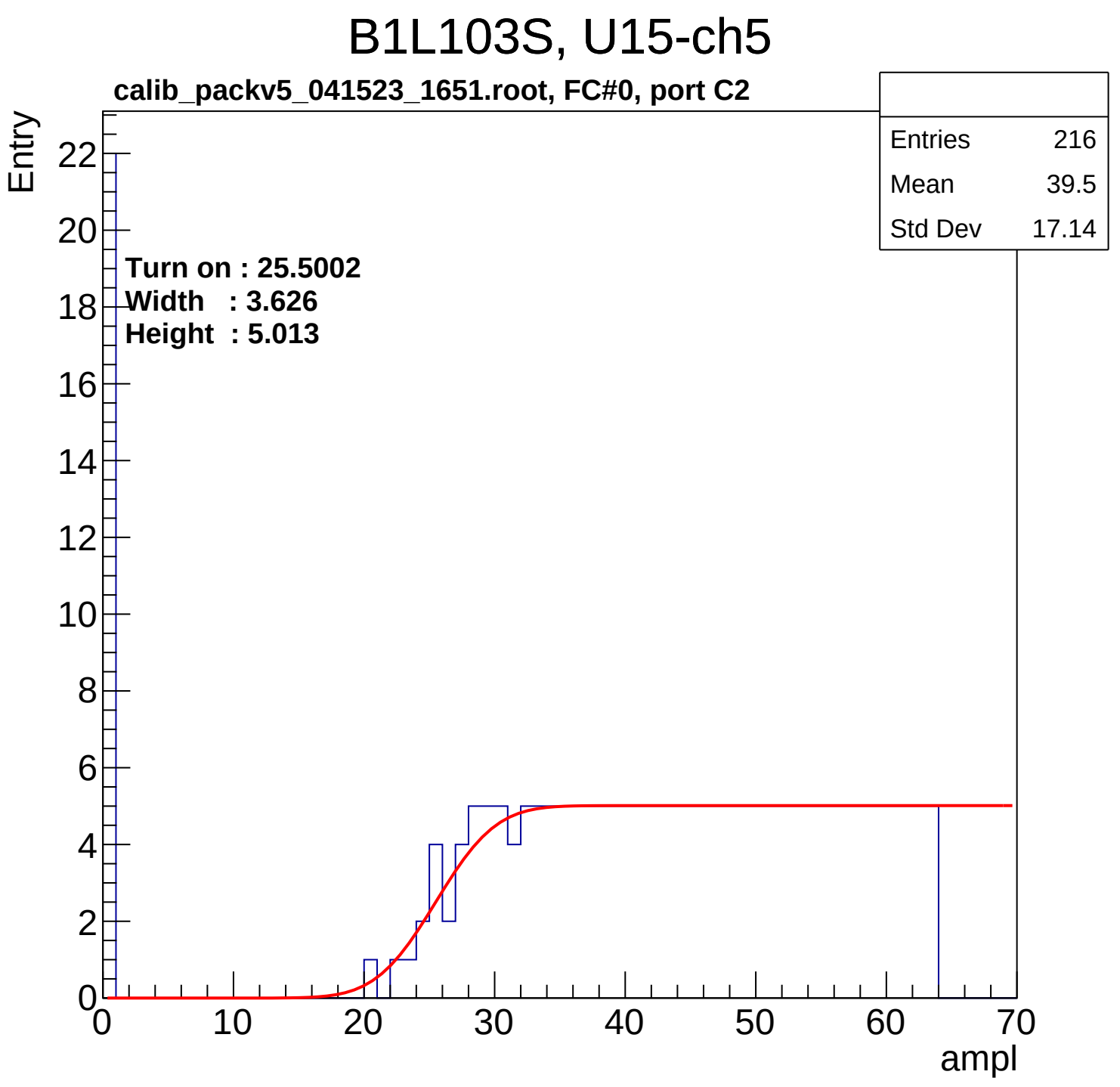
B1L103S, U15-ch5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 216
Mean 39.5
Std Dev 17.14
Turn on : 25.5002
Width : 3.626
Height : 5.013
Entry
ampl
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8
10
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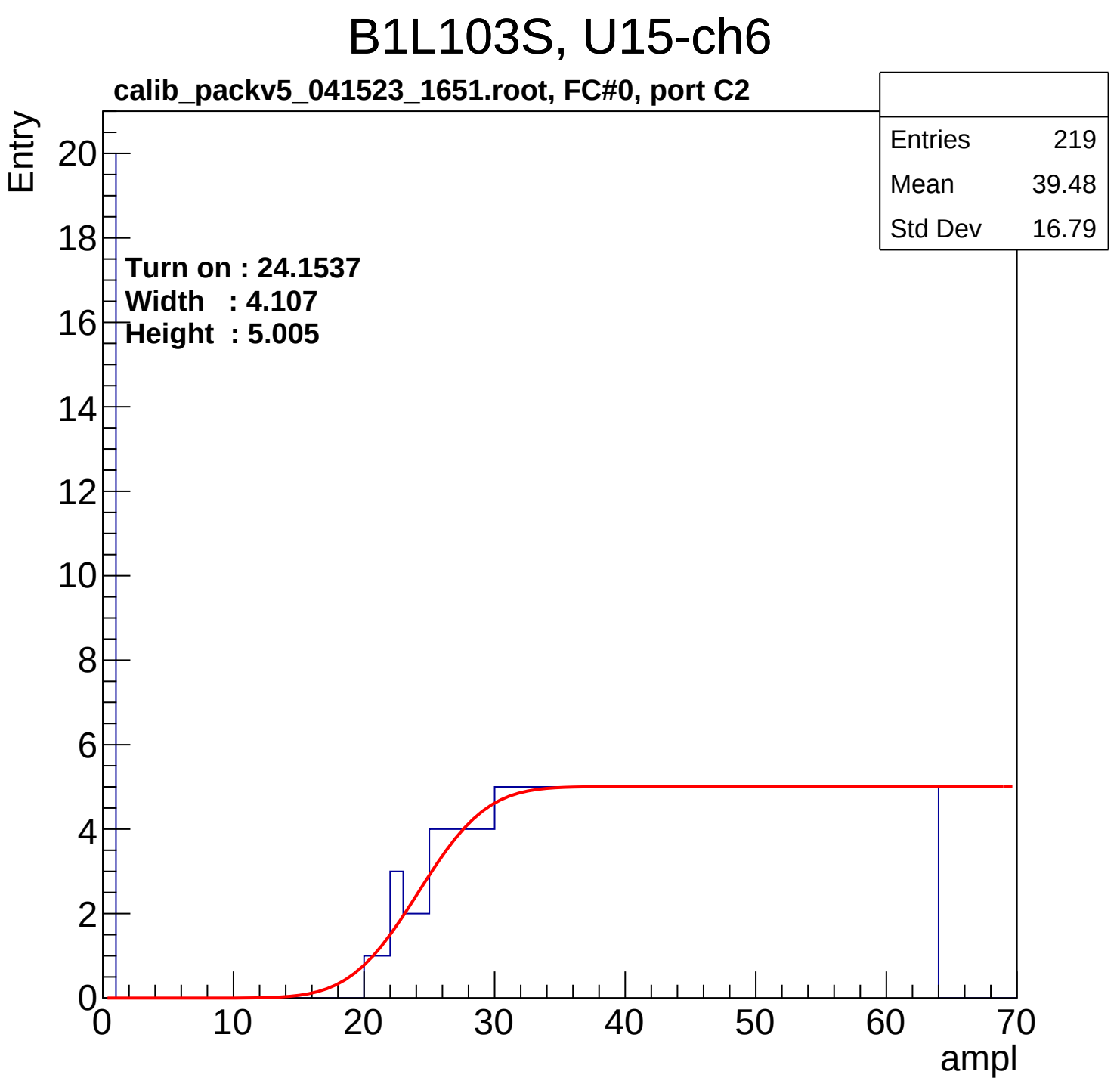
B1L103S, U15-ch6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 219
Mean 39.48
Std Dev 16.79
Turn on : 24.1537
Width : 4.107
Height : 5.005
Entry
ampl
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6
8
10
12
14
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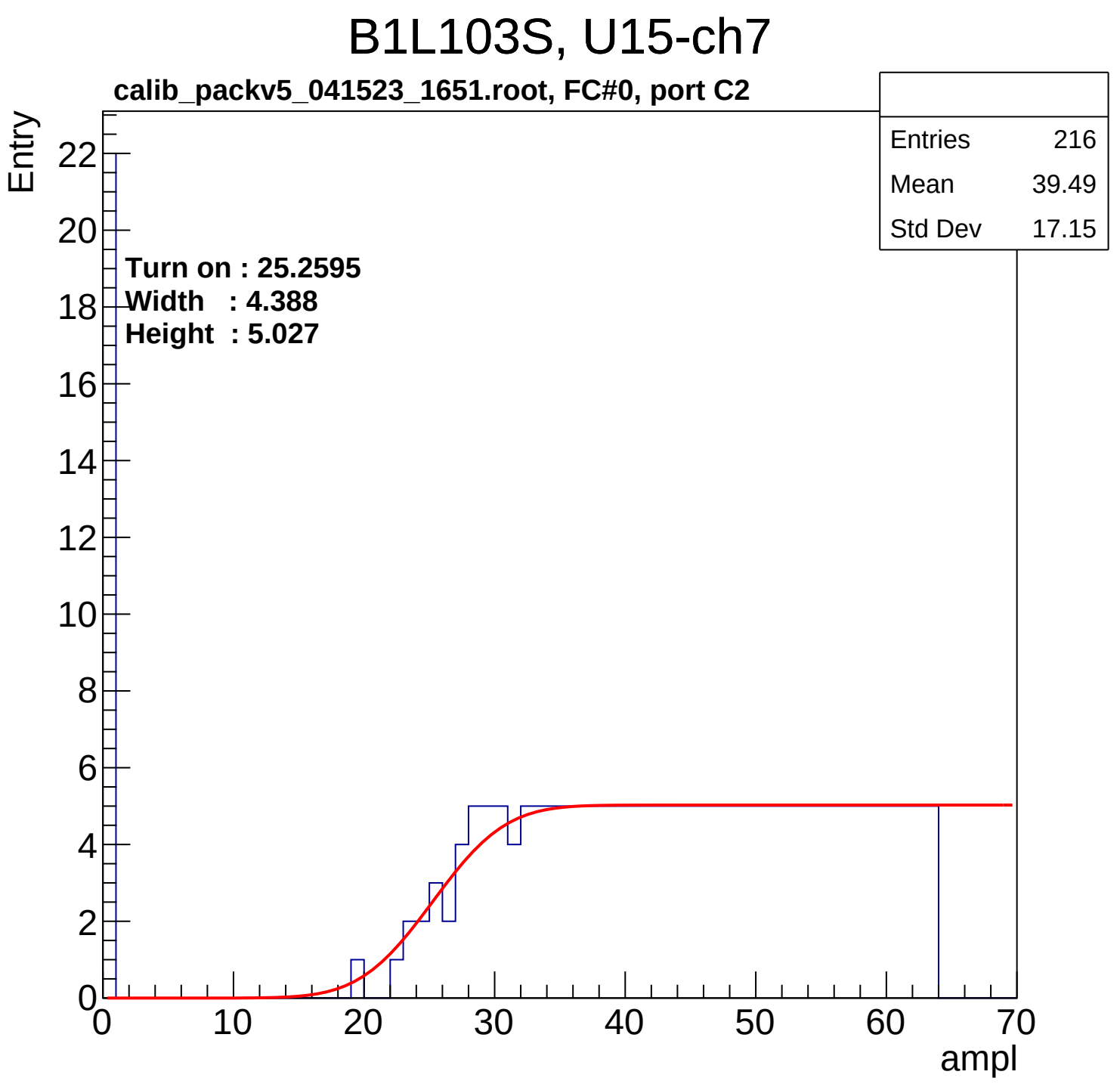
B1L103S, U15-ch7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 216
Mean 39.49
Std Dev 17.15
Turn on : 25.2595
Width : 4.388
Height : 5.027
Entry
ampl
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8
10
12
14
16
18
20
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0
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60
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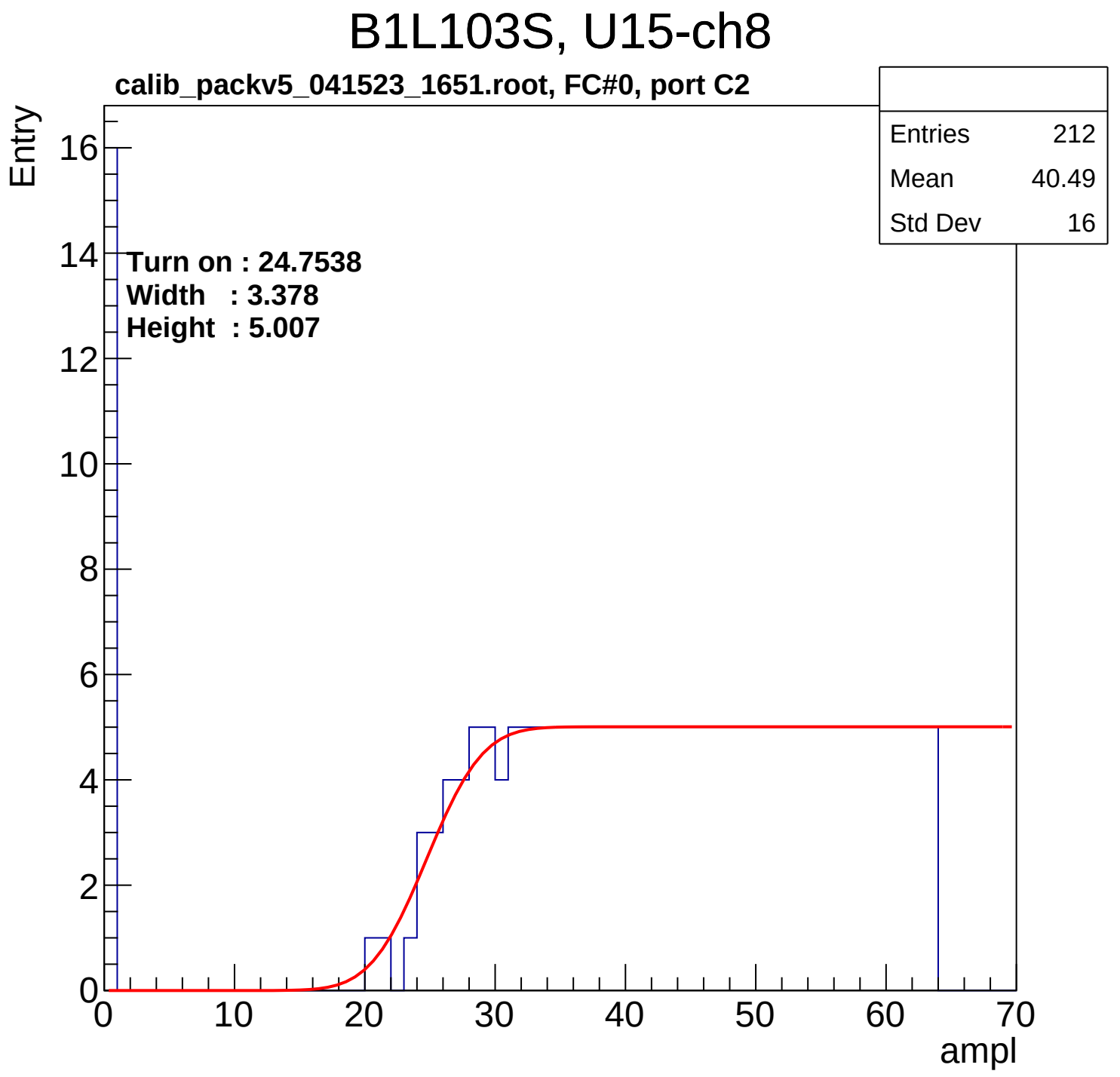
B1L103S, U15-ch8
calib_packv5_041523_1651.root, FC#0, port C2
Entries 212
Mean 40.49
Std Dev 16
Turn on : 24.7538
Width : 3.378
Height : 5.007
Entry
ampl
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4
6
8
10
12
14
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0
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60
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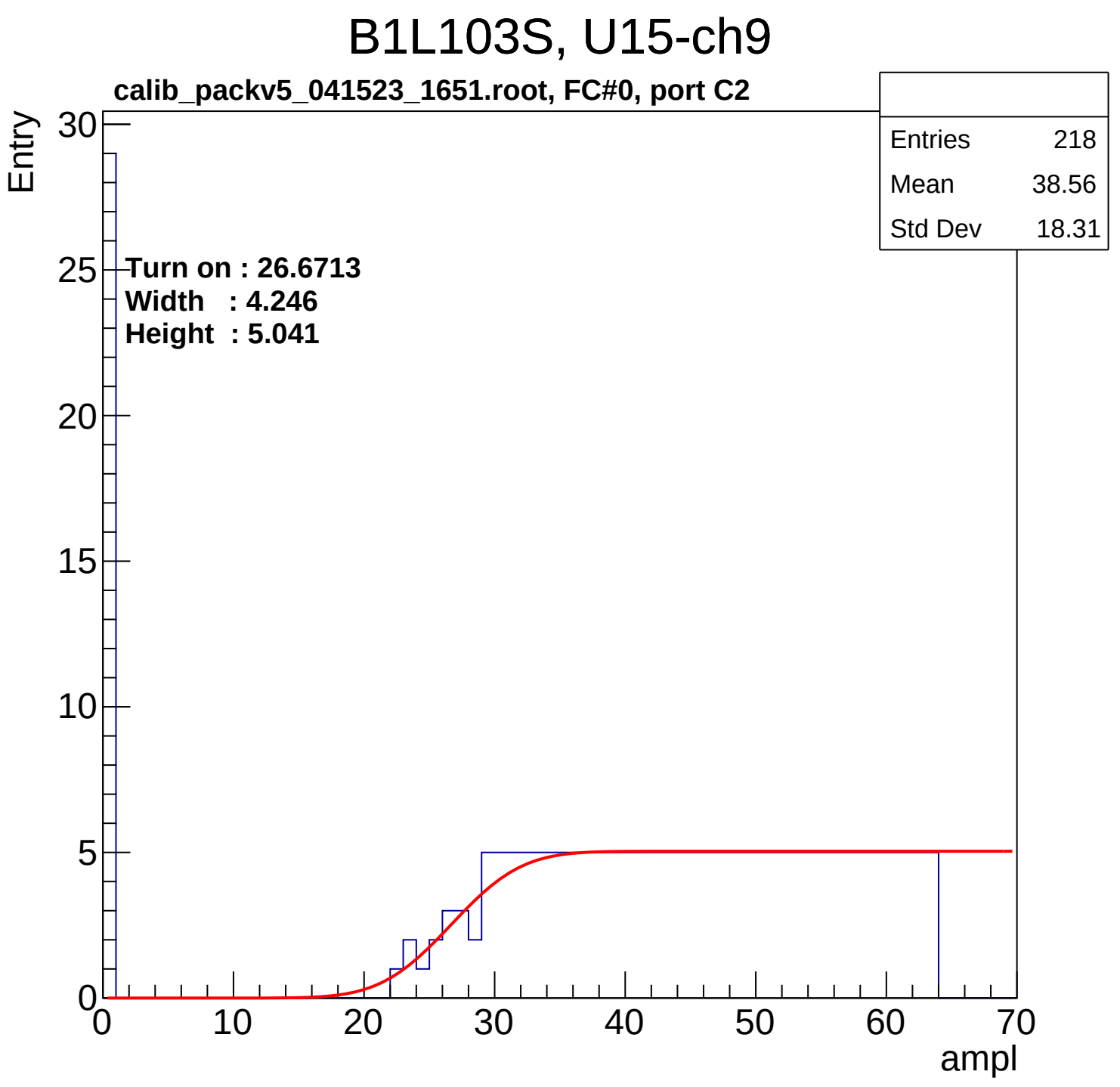
B1L103S, U15-ch9
calib_packv5_041523_1651.root, FC#0, port C2
Entries 218
Mean 38.56
Std Dev 18.31
Turn on : 26.6713
Width : 4.246
Height : 5.041
Entry
ampl
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5
10
15
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40
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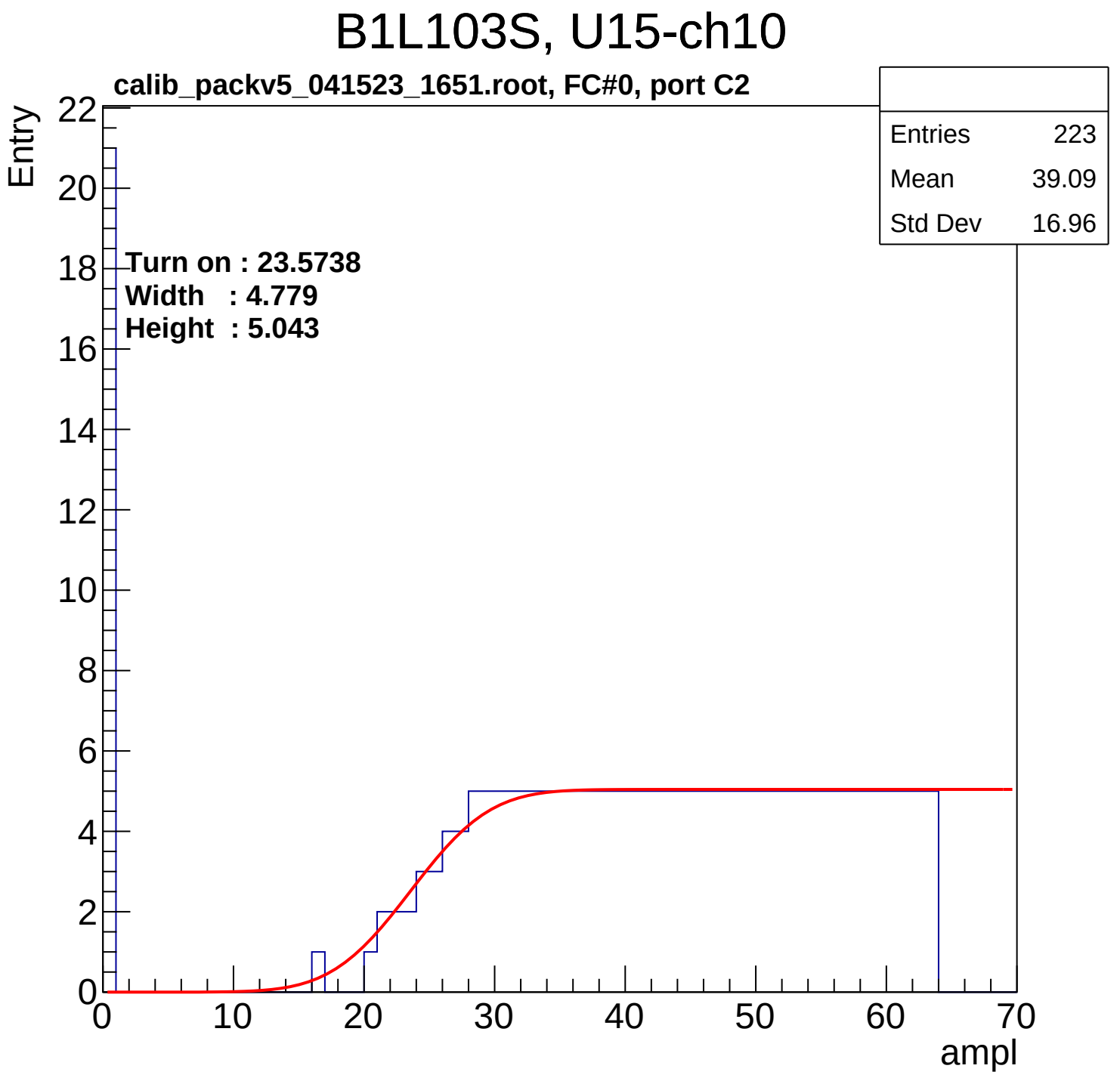
B1L103S, U15-ch10
calib_packv5_041523_1651.root, FC#0, port C2
Entries 223
Mean 39.09
Std Dev 16.96
Turn on : 23.5738
Width : 4.779
Height : 5.043
Entry
ampl
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8
10
12
14
16
18
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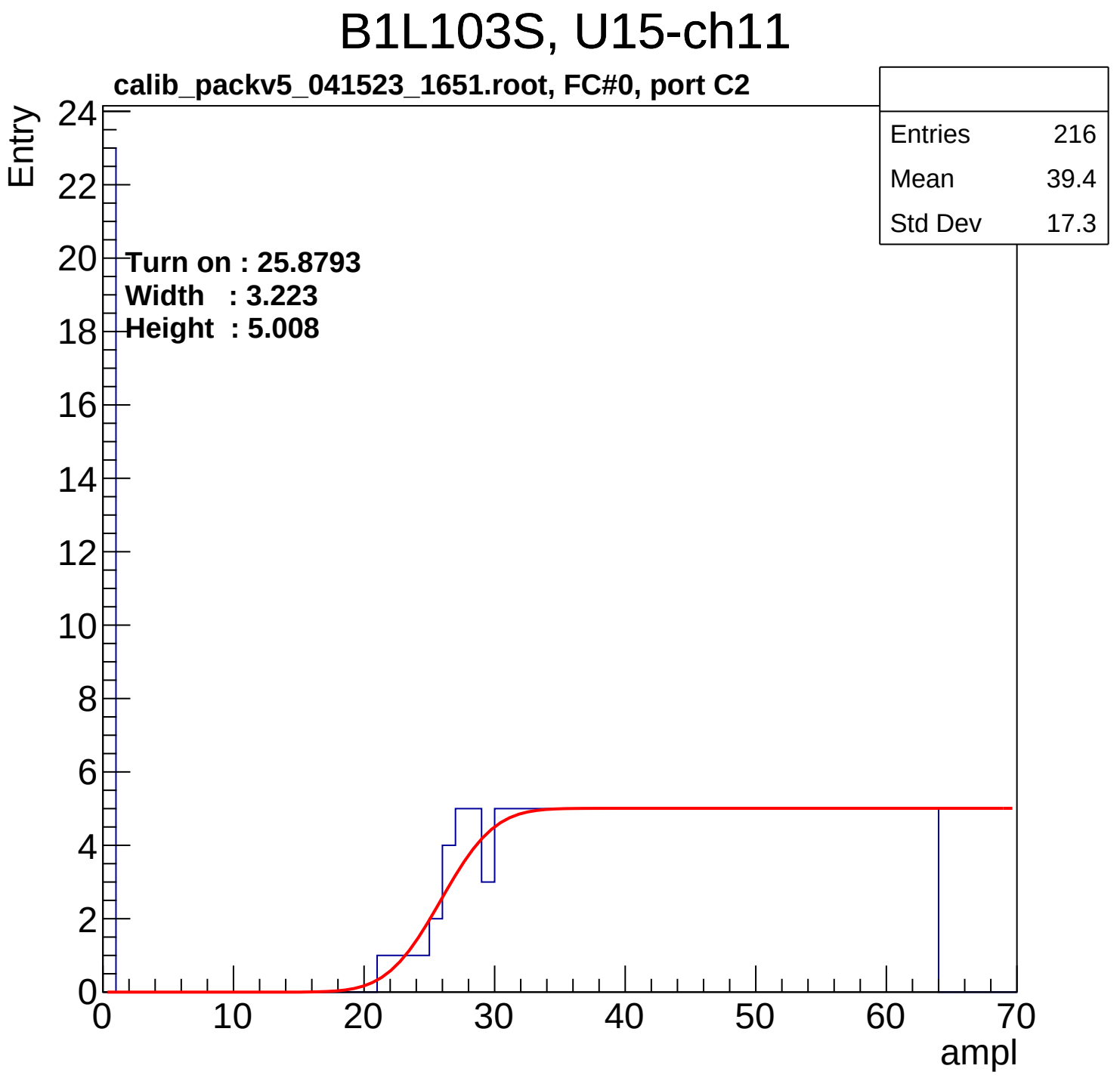
B1L103S, U15-ch11
calib_packv5_041523_1651.root, FC#0, port C2
Entries 216
Mean 39.4
Std Dev 17.3
Turn on : 25.8793
Width : 3.223
Height : 5.008
Entry
ampl
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12
14
16
18
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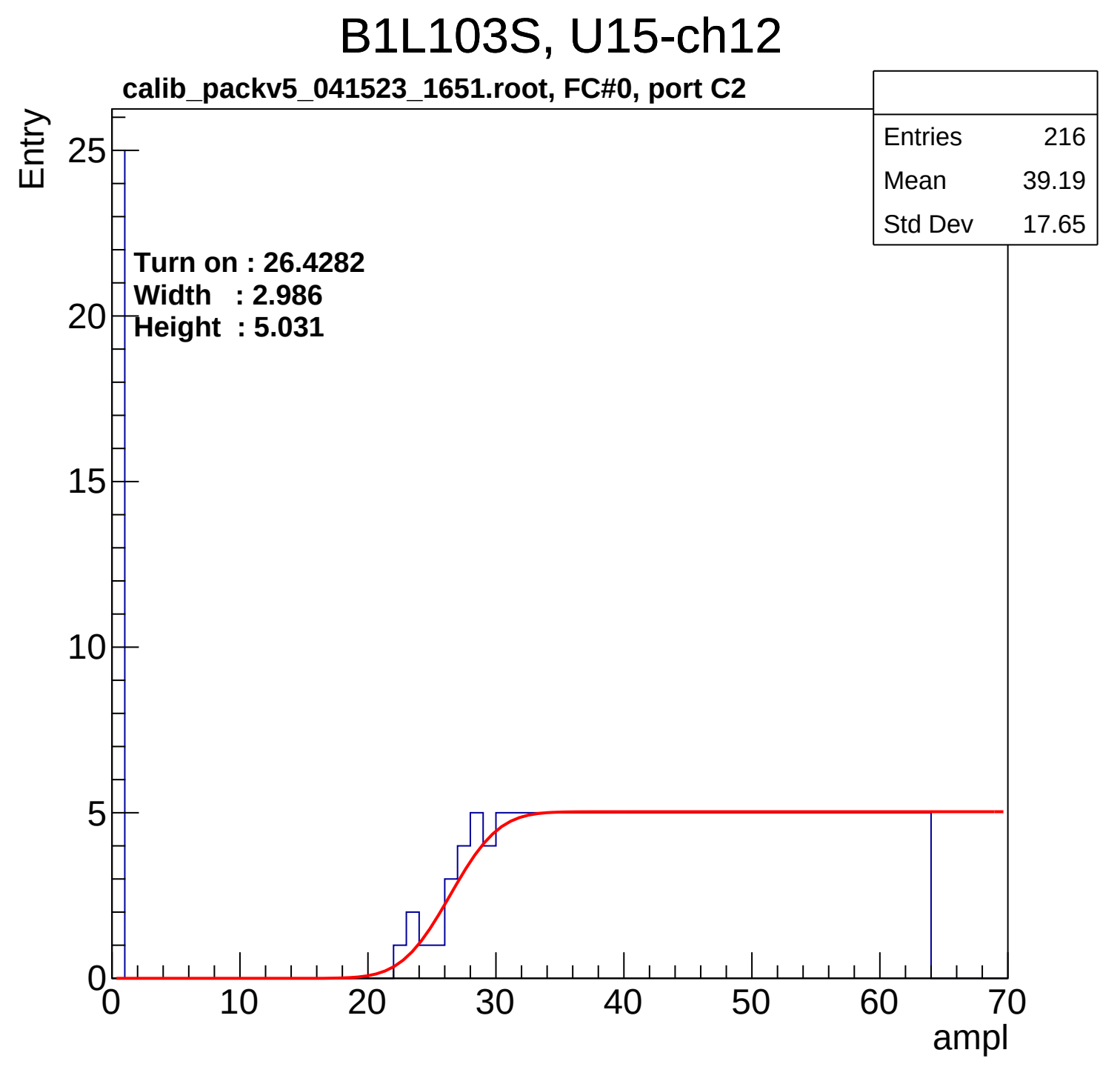
B1L103S, U15-ch12
calib_packv5_041523_1651.root, FC#0, port C2
Entries 216
Mean 39.19
Std Dev 17.65
Turn on : 26.4282
Width : 2.986
Height : 5.031
Entry
ampl
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5
10
15
20
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0
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40
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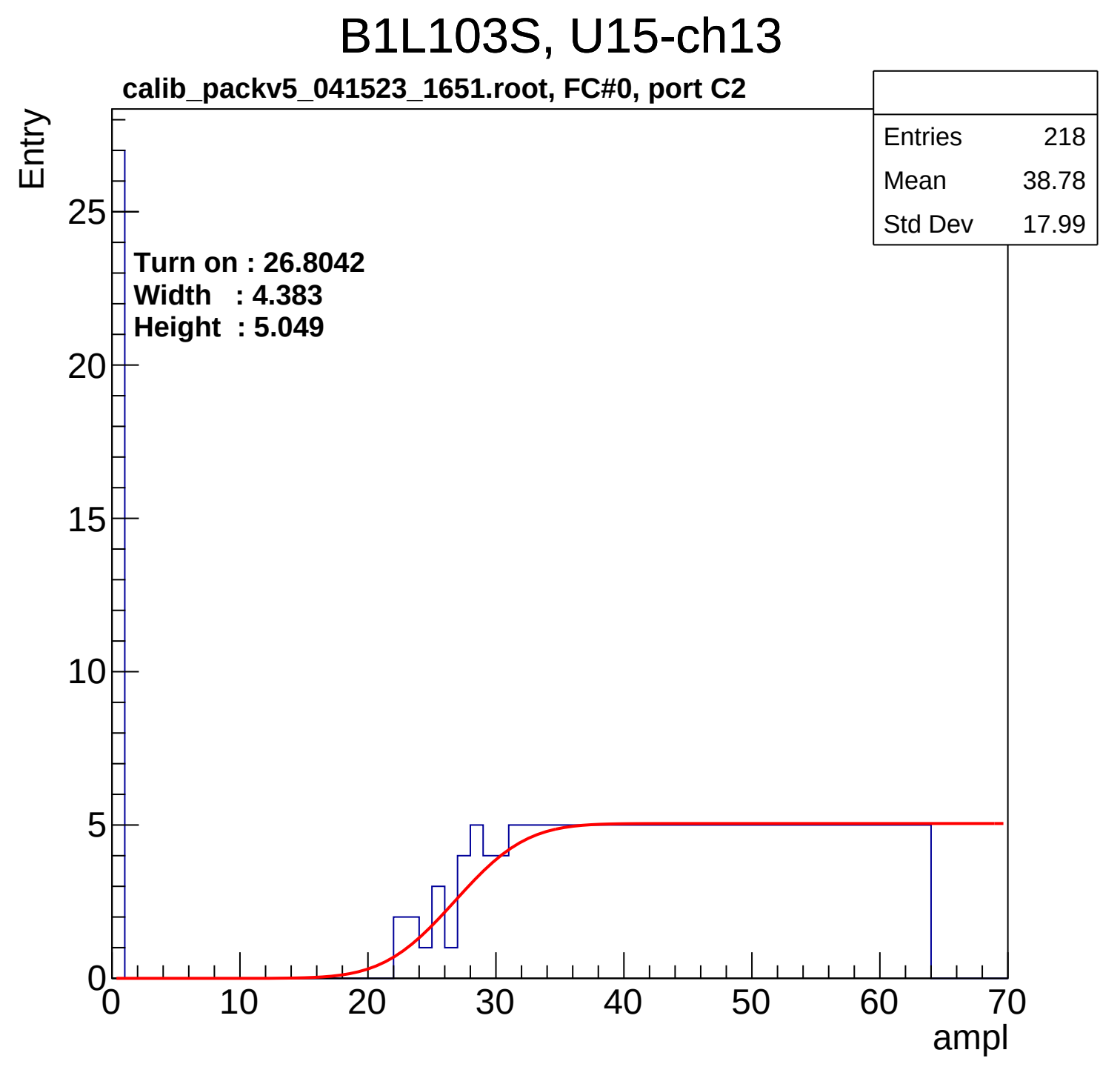
B1L103S, U15-ch13
calib_packv5_041523_1651.root, FC#0, port C2
Entries 218
Mean 38.78
Std Dev 17.99
Turn on : 26.8042
Width : 4.383
Height : 5.049
Entry
ampl
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10
15
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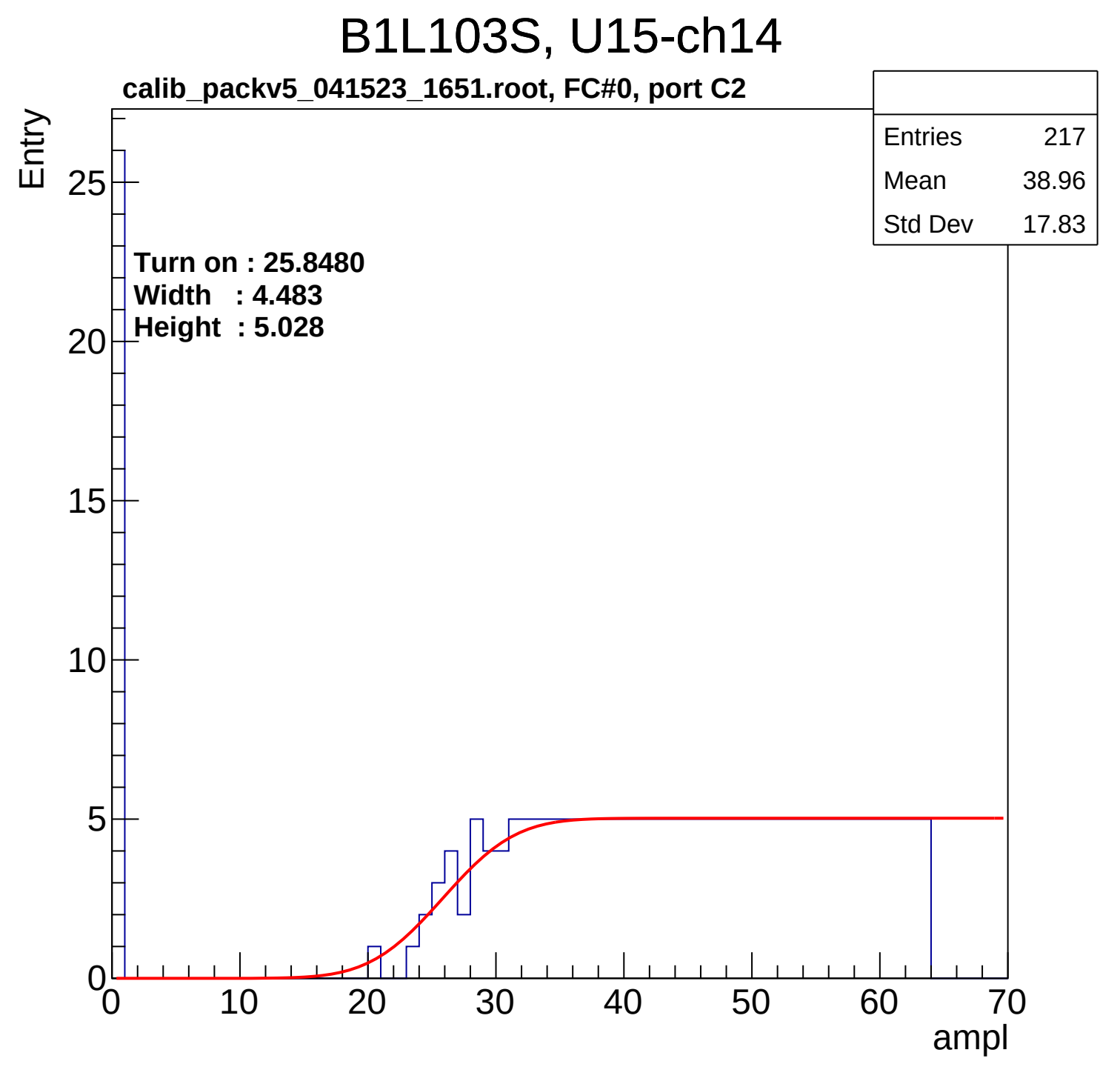
B1L103S, U15-ch14
calib_packv5_041523_1651.root, FC#0, port C2
Entries 217
Mean 38.96
Std Dev 17.83
Turn on : 25.8480
Width : 4.483
Height : 5.028
Entry
ampl
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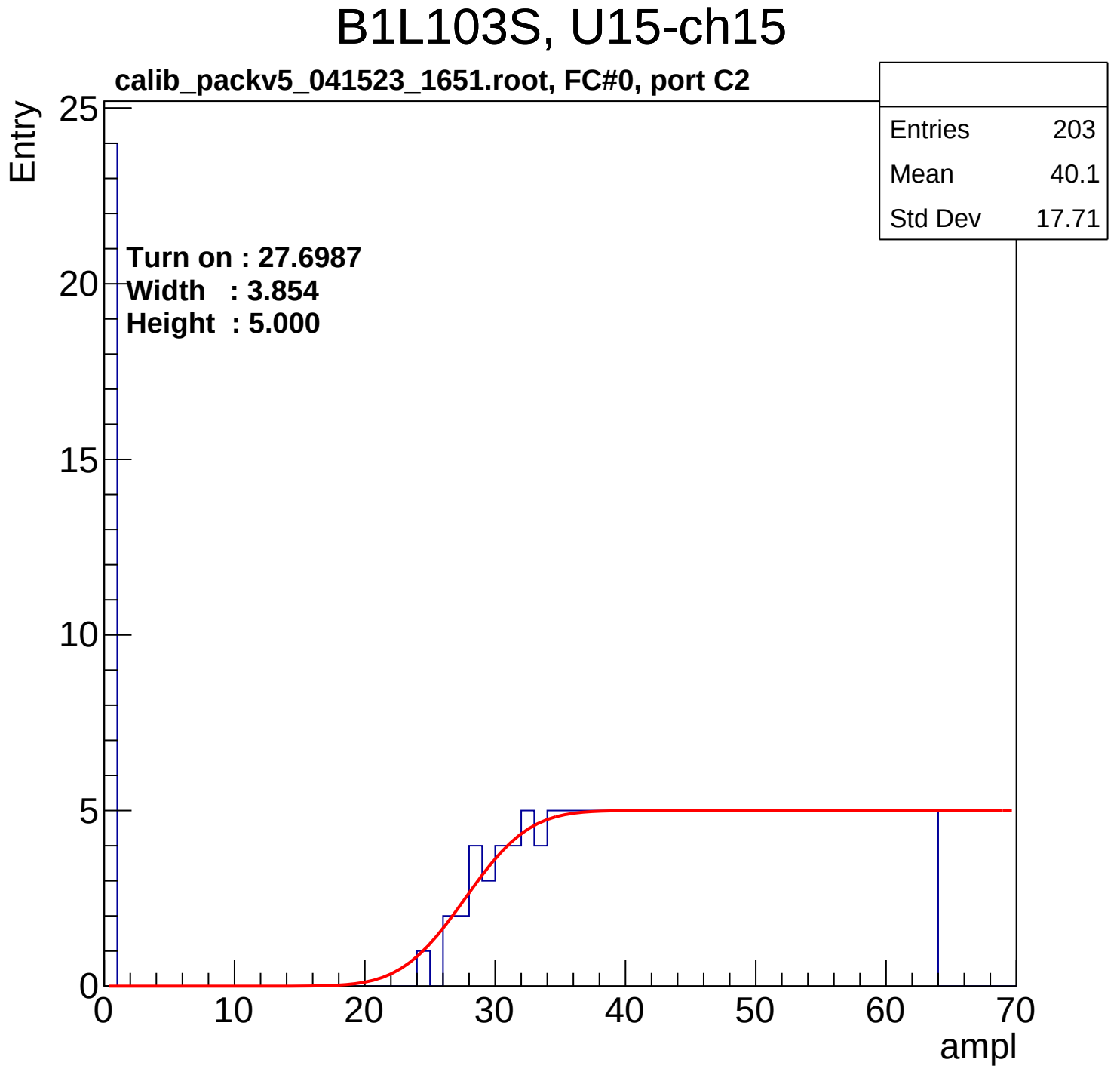
B1L103S, U15-ch15
calib_packv5_041523_1651.root, FC#0, port C2
Entries 203
Mean 40.1
Std Dev 17.71
Turn on : 27.6987
Width : 3.854
Height : 5.000
Entry
ampl
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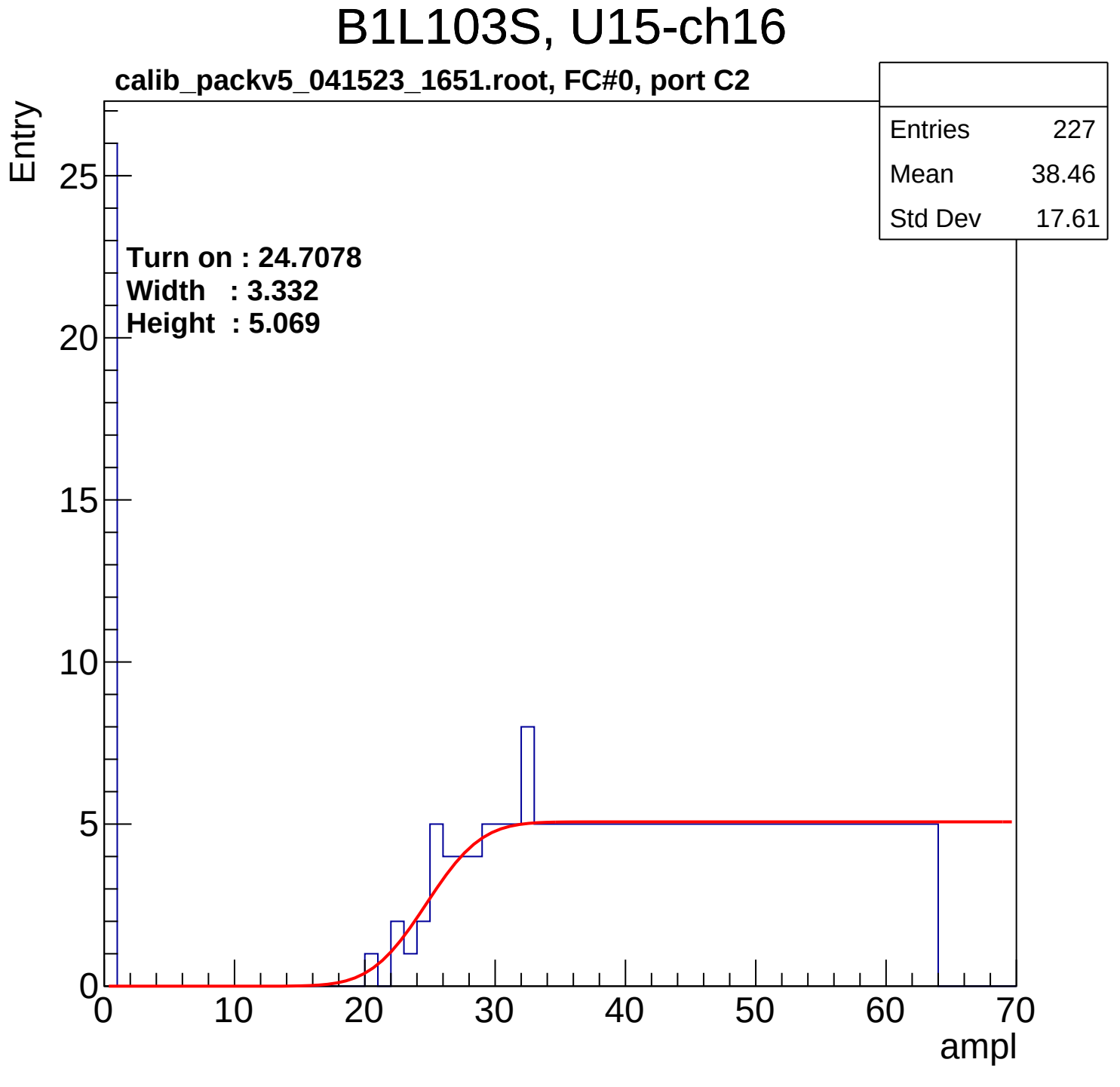
B1L103S, U15-ch16
calib_packv5_041523_1651.root, FC#0, port C2
Entries 227
Mean 38.46
Std Dev 17.61
Turn on : 24.7078
Width : 3.332
Height : 5.069
Entry
ampl
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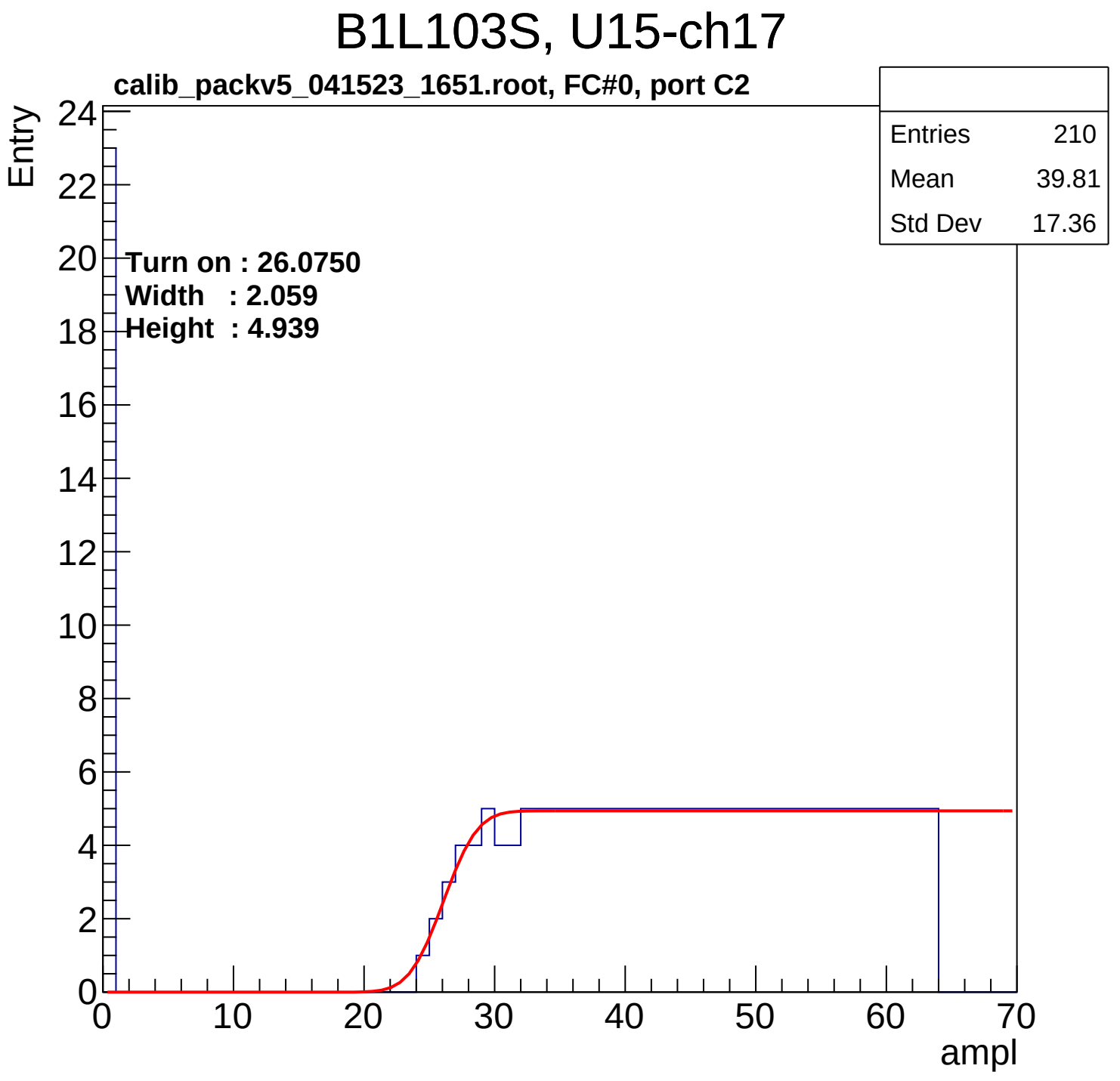
B1L103S, U15-ch17
calib_packv5_041523_1651.root, FC#0, port C2
Entries 210
Mean 39.81
Std Dev 17.36
Turn on : 26.0750
Width : 2.059
Height : 4.939
Entry
ampl
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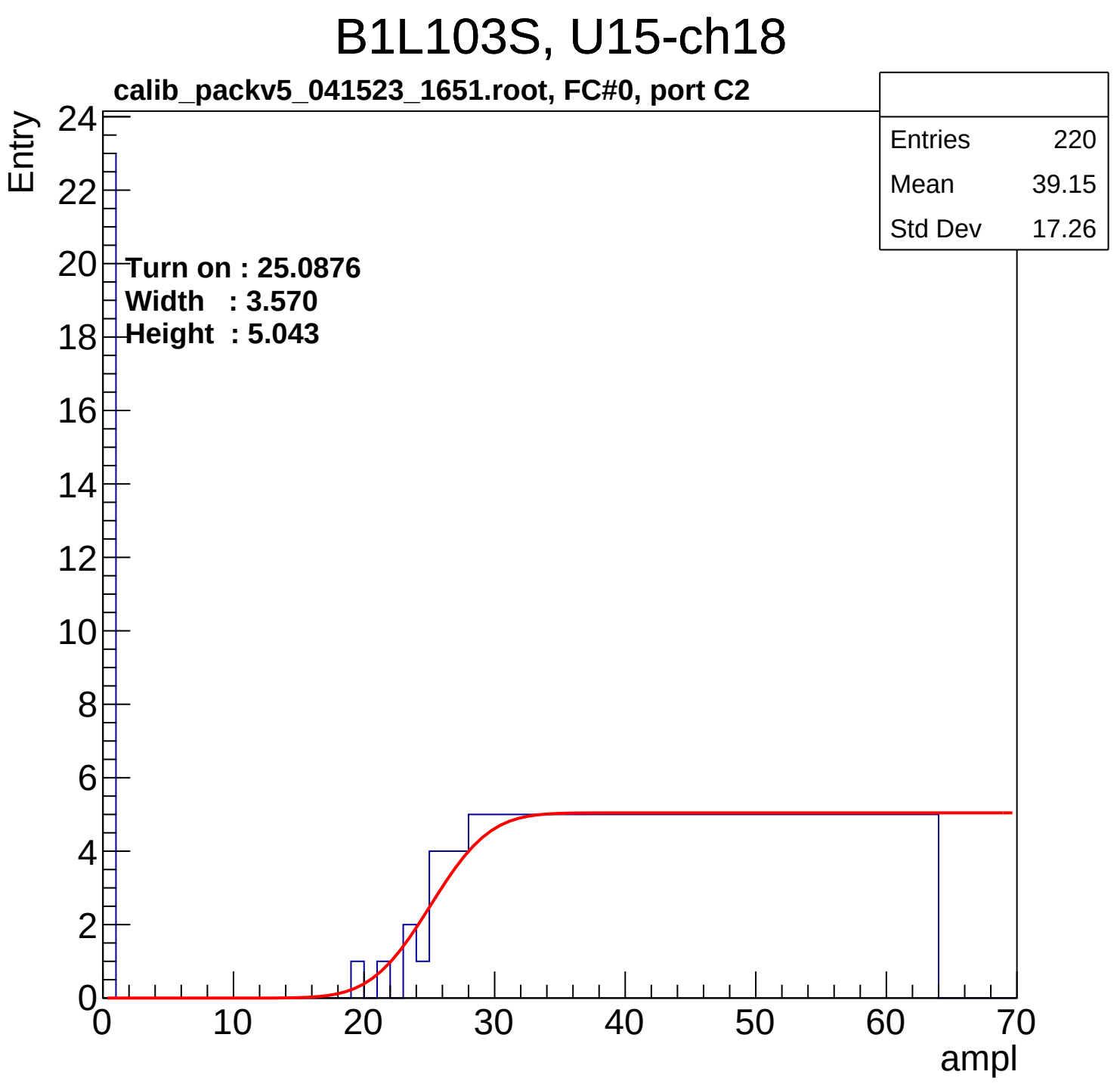
B1L103S, U15-ch18
calib_packv5_041523_1651.root, FC#0, port C2
Entries 220
Mean 39.15
Std Dev 17.26
Turn on : 25.0876
Width : 3.570
Height : 5.043
Entry
ampl
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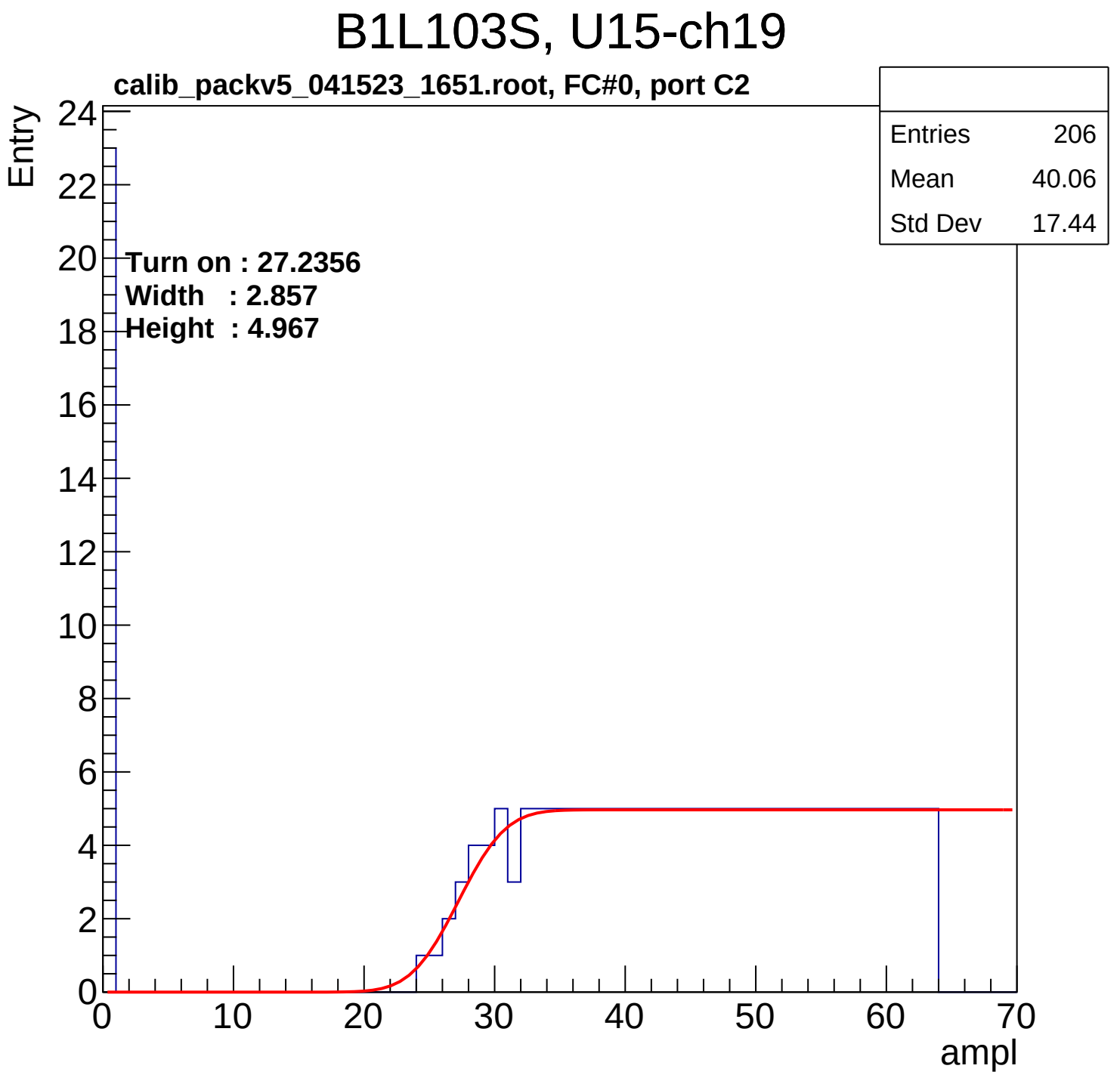
B1L103S, U15-ch19
calib_packv5_041523_1651.root, FC#0, port C2
Entries 206
Mean 40.06
Std Dev 17.44
Turn on : 27.2356
Width : 2.857
Height : 4.967
Entry
ampl
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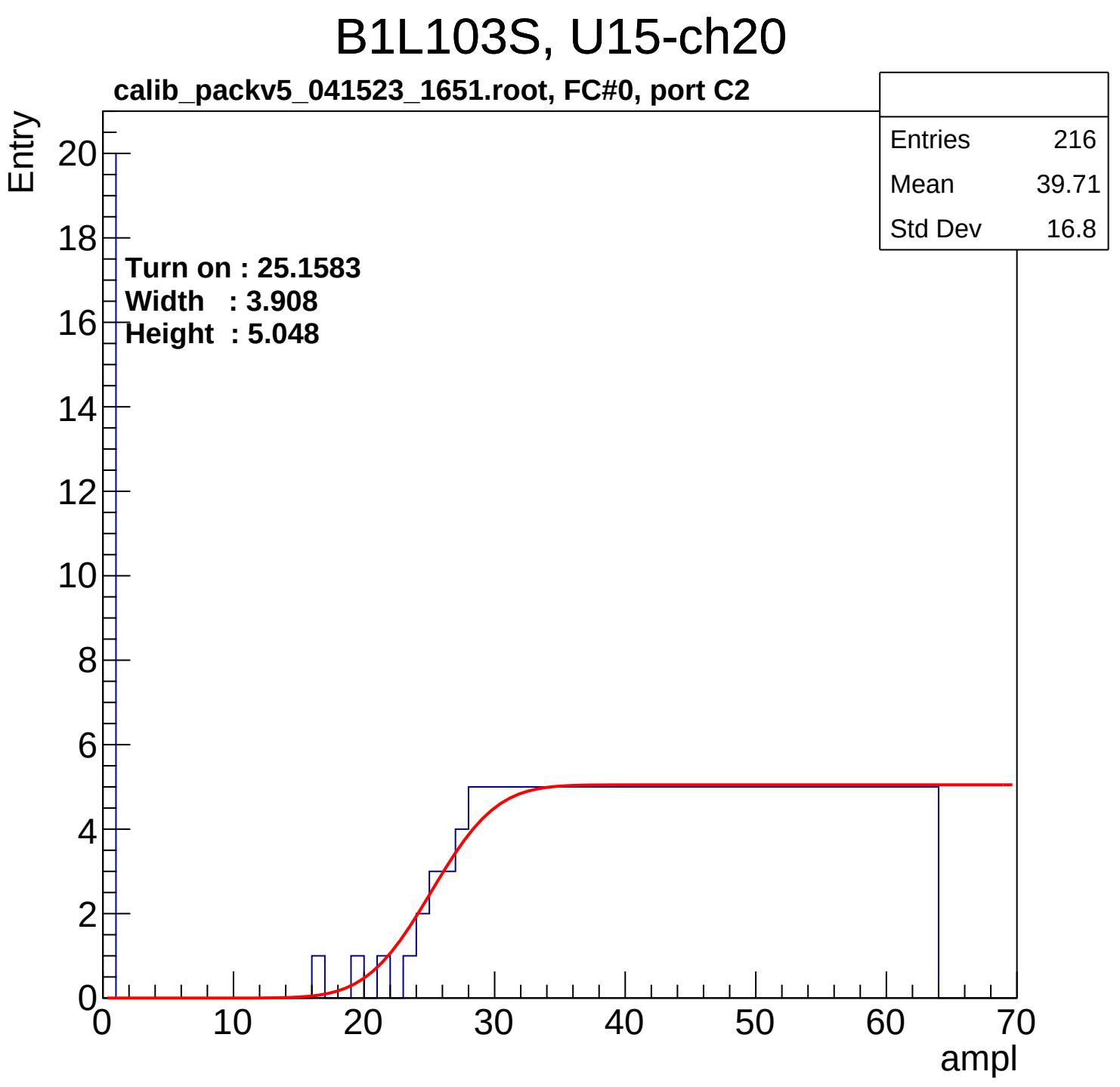
B1L103S, U15-ch20
calib_packv5_041523_1651.root, FC#0, port C2
Entries 216
Mean 39.71
Std Dev 16.8
Turn on : 25.1583
Width : 3.908
Height : 5.048
Entry
ampl
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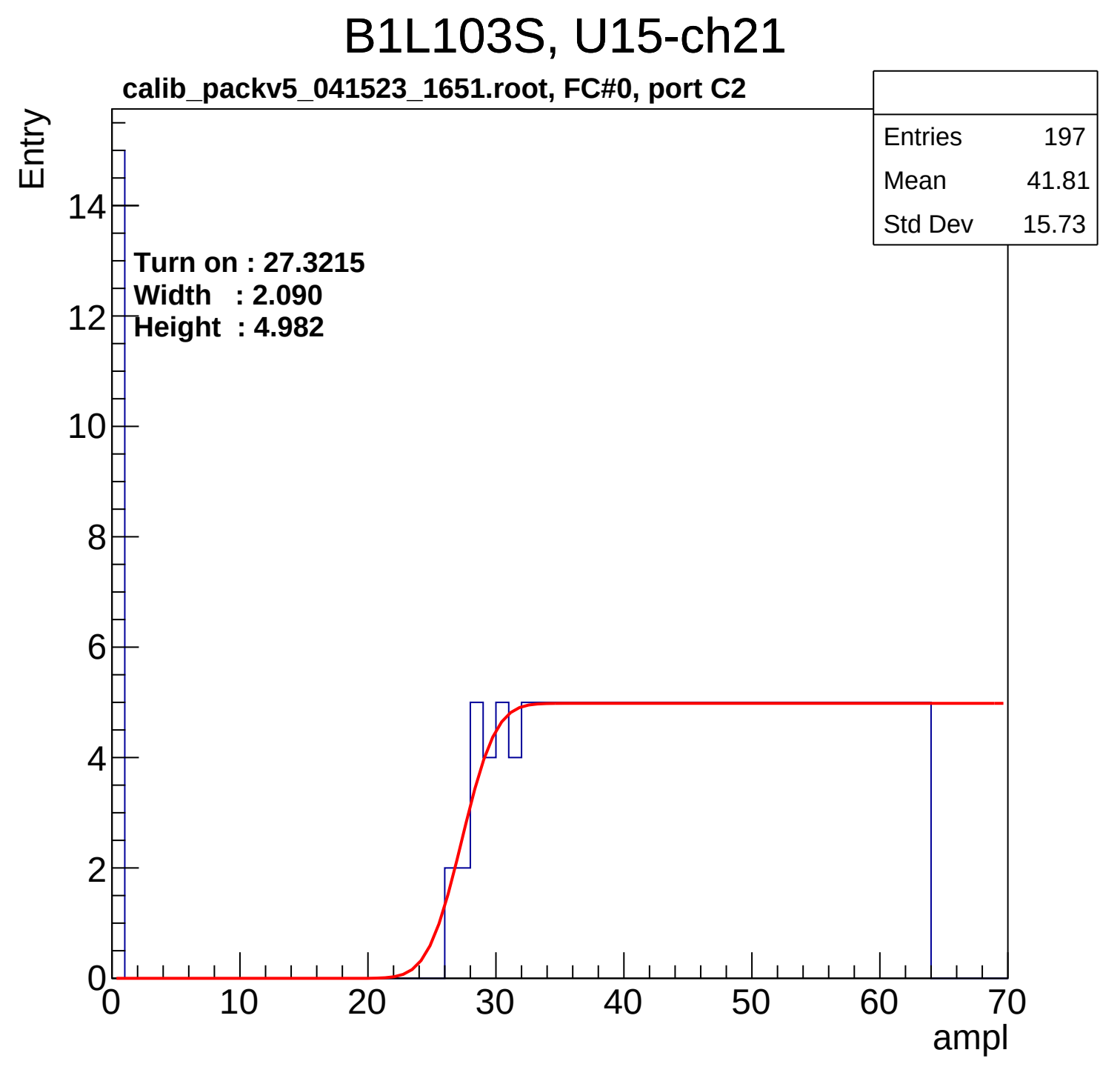
B1L103S, U15-ch21
calib_packv5_041523_1651.root, FC#0, port C2
Entries 197
Mean 41.81
Std Dev 15.73
Turn on : 27.3215
Width : 2.090
Height : 4.982
Entry
ampl
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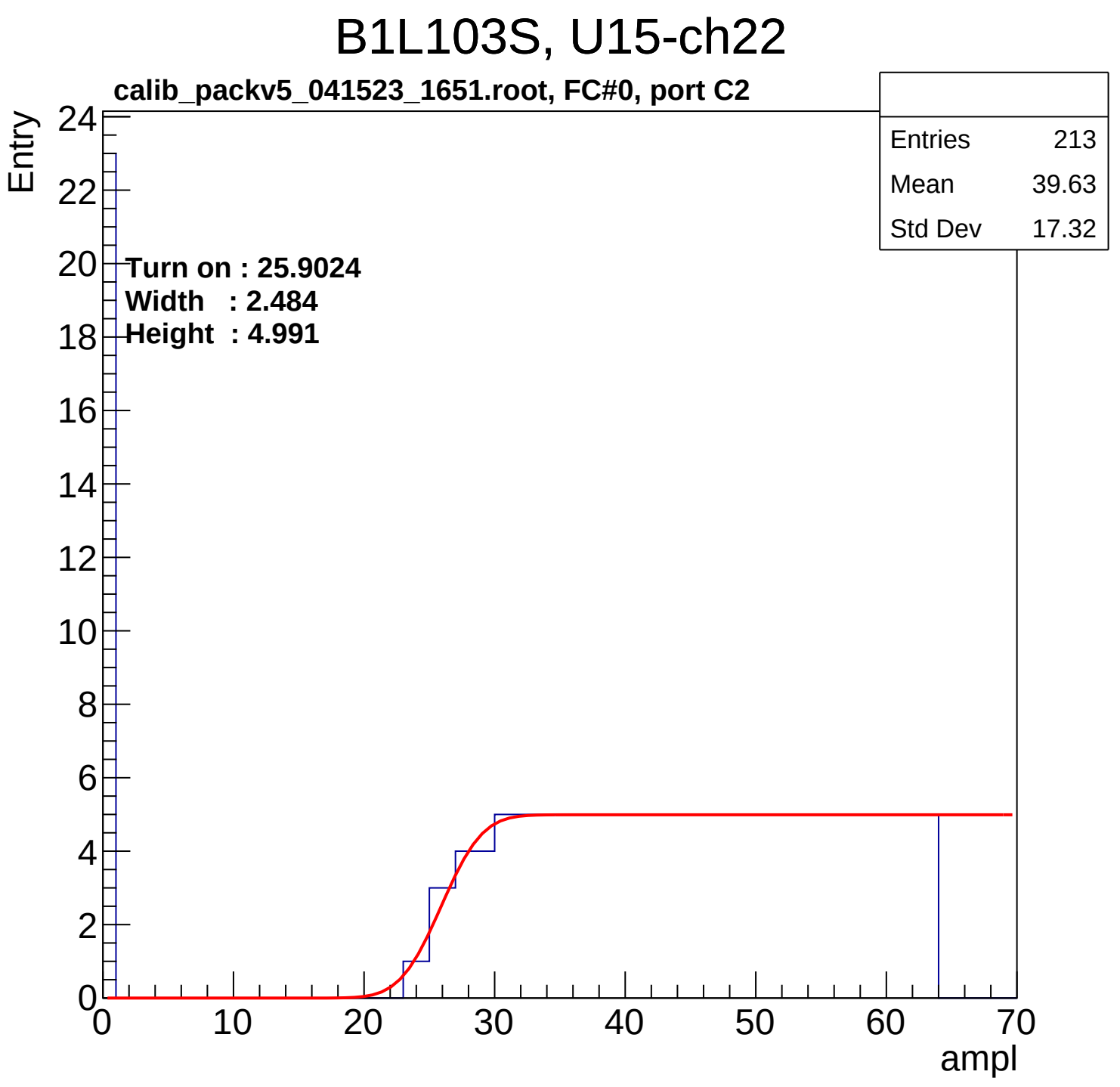
B1L103S, U15-ch22
calib_packv5_041523_1651.root, FC#0, port C2
Entries 213
Mean 39.63
Std Dev 17.32
Turn on : 25.9024
Width : 2.484
Height : 4.991
Entry
ampl
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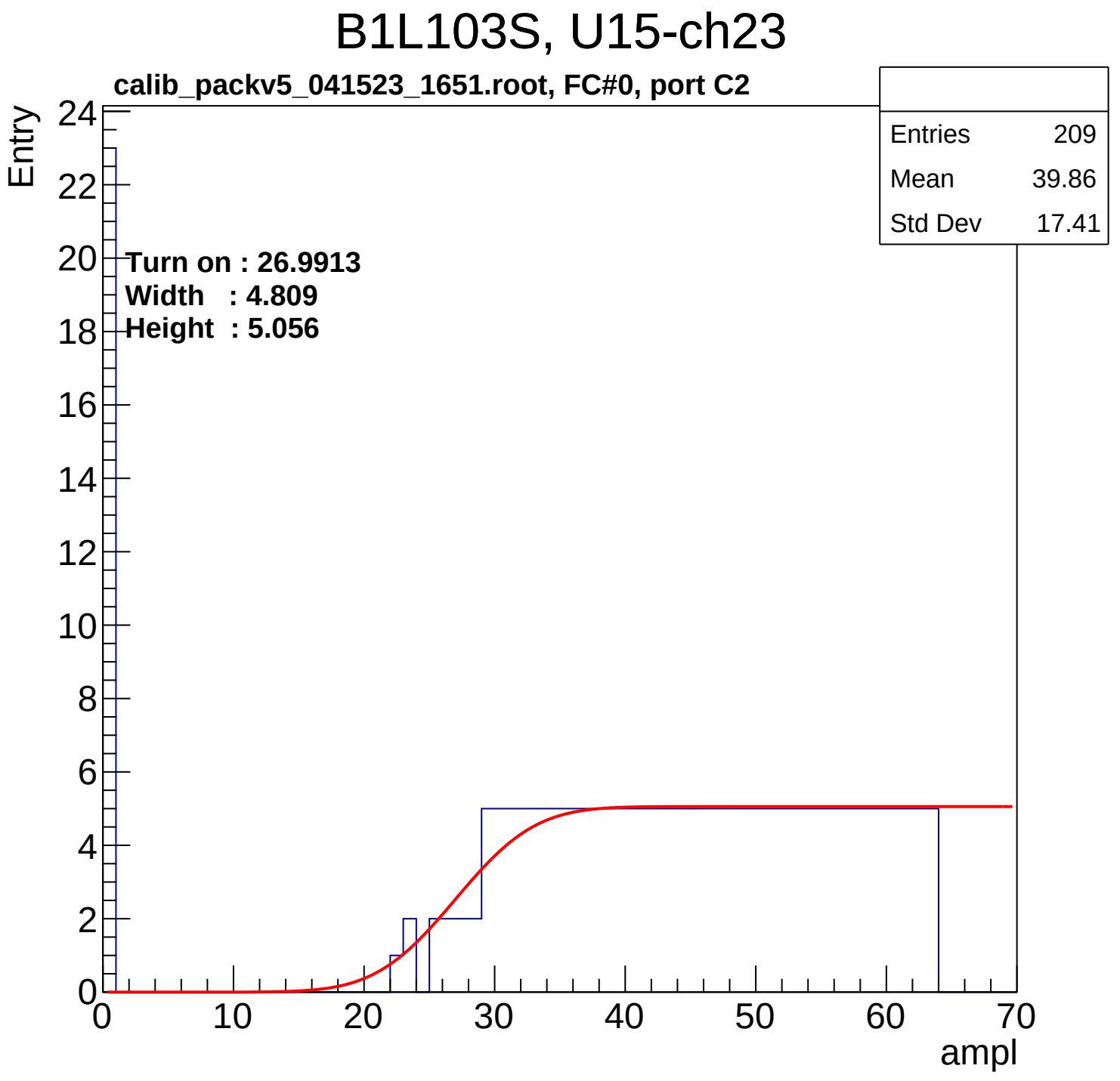
B1L103S, U15-ch23
calib_packv5_041523_1651.root, FC#0, port C2
Entries 209
Mean 39.86
Std Dev 17.41
Turn on : 26.9913
Width : 4.809
Height : 5.056
Entry
ampl
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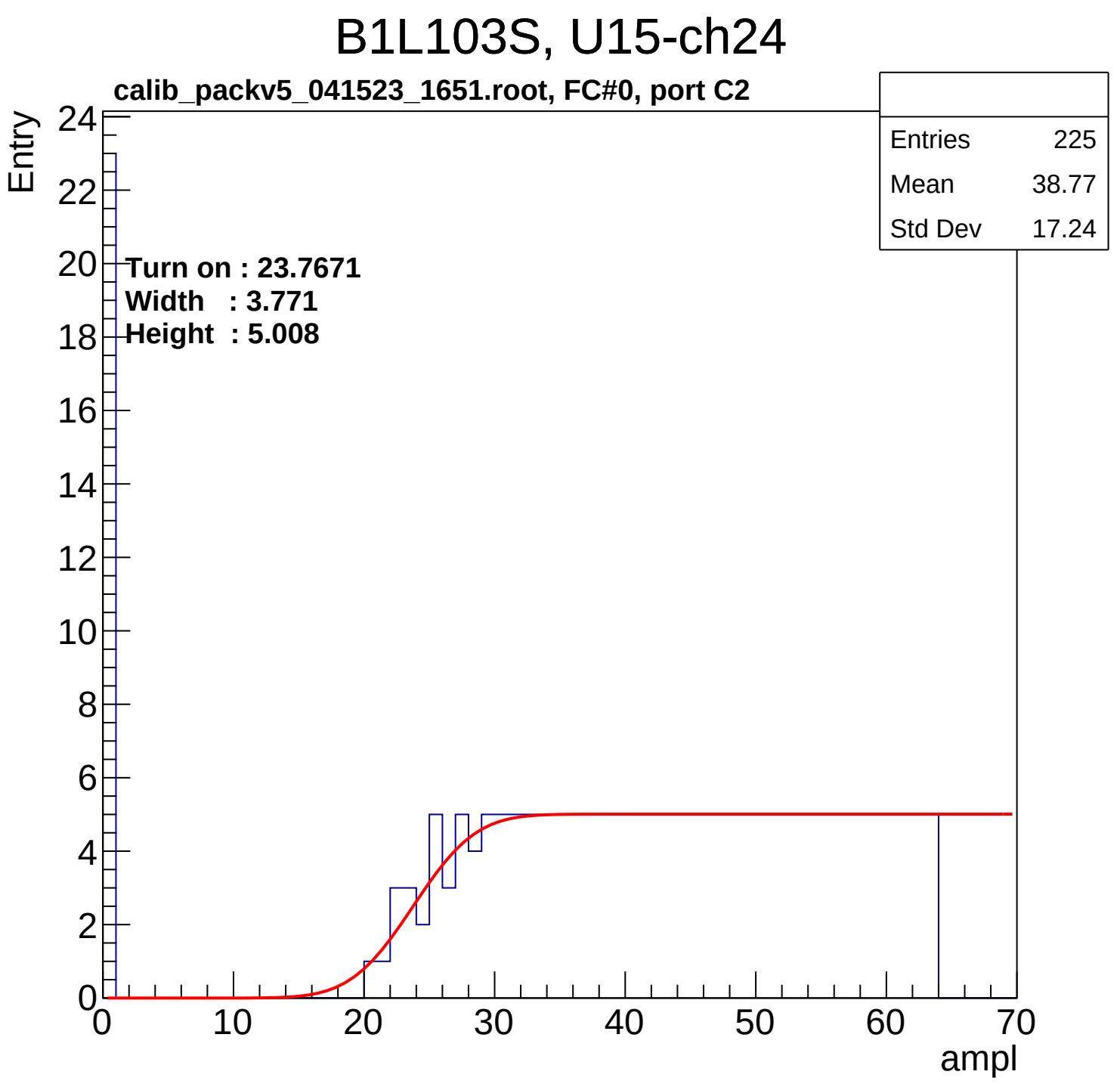
B1L103S, U15-ch24
calib_packv5_041523_1651.root, FC#0, port C2
Entries 225
Mean 38.77
Std Dev 17.24
Turn on : 23.7671
Width : 3.771
Height : 5.008
Entry
ampl
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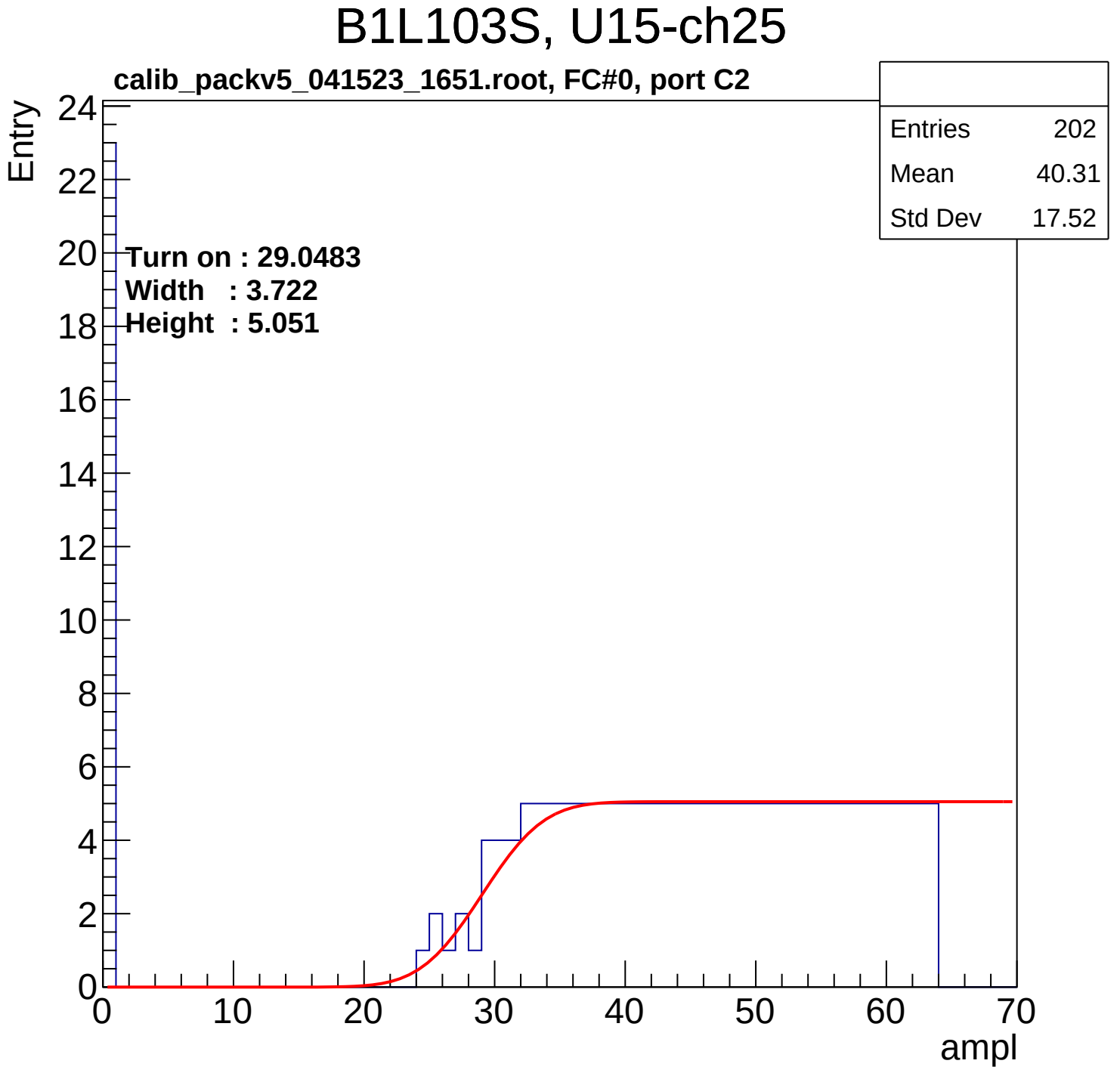
B1L103S, U15-ch25
calib_packv5_041523_1651.root, FC#0, port C2
Entries 202
Mean 40.31
Std Dev 17.52
Turn on : 29.0483
Width : 3.722
Height : 5.051
Entry
ampl
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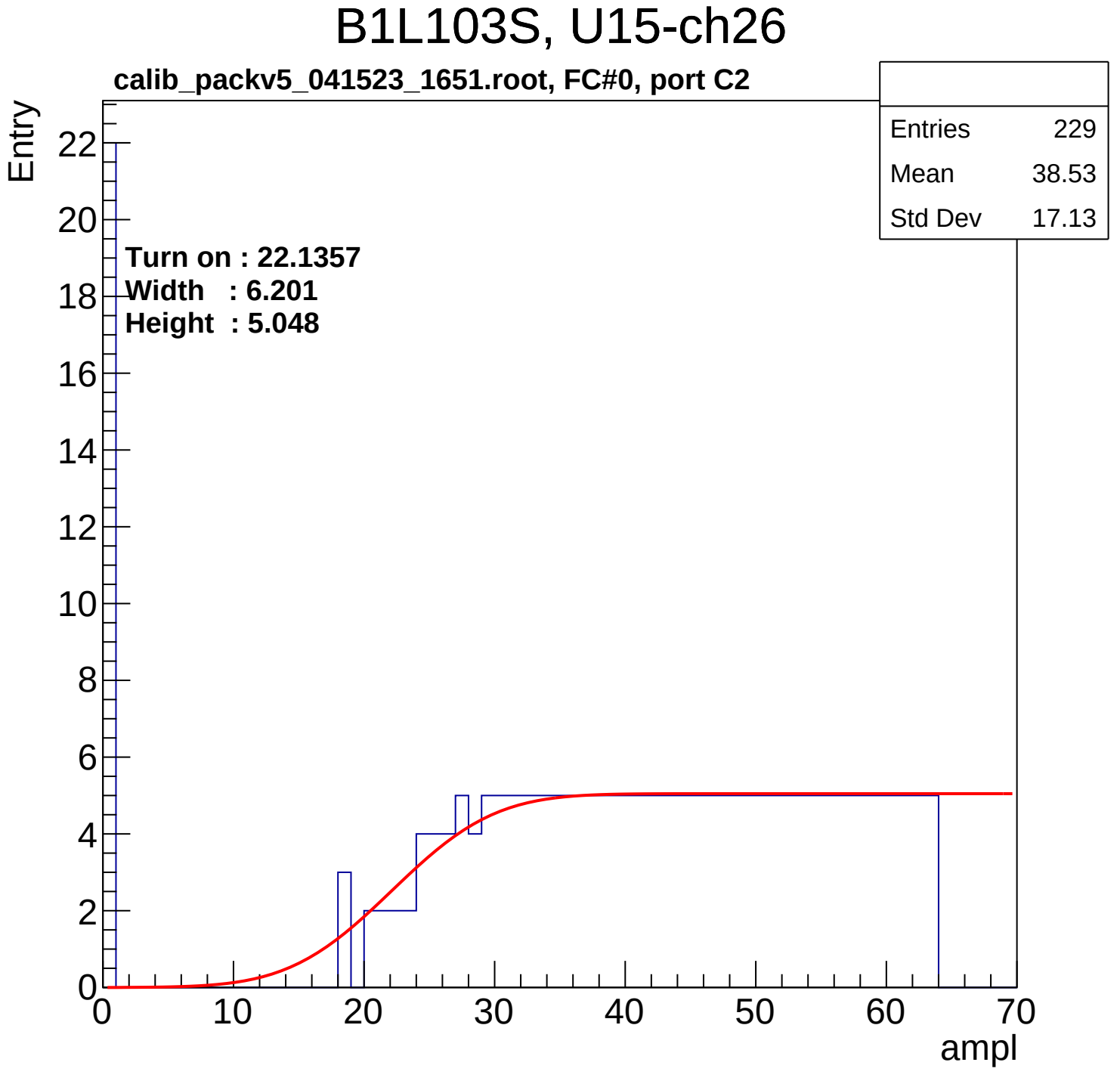
B1L103S, U15-ch26
calib_packv5_041523_1651.root, FC#0, port C2
Entries 229
Mean 38.53
Std Dev 17.13
Turn on : 22.1357
Width : 6.201
Height : 5.048
Entry
ampl
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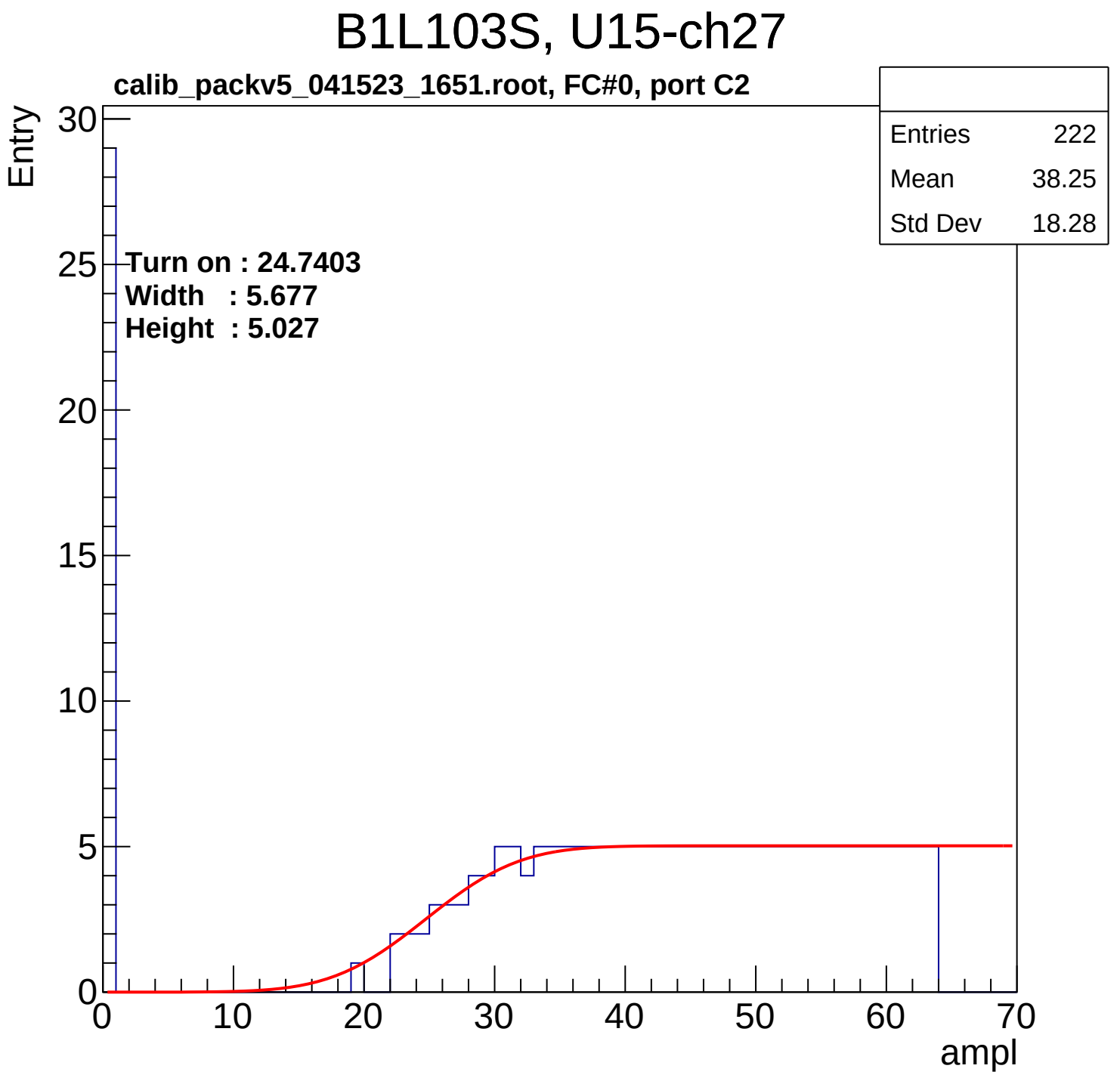
B1L103S, U15-ch27
calib_packv5_041523_1651.root, FC#0, port C2
Entries 222
Mean 38.25
Std Dev 18.28
Turn on : 24.7403
Width : 5.677
Height : 5.027
Entry
ampl
0
5
10
15
20
25
30
0
10
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30
40
50
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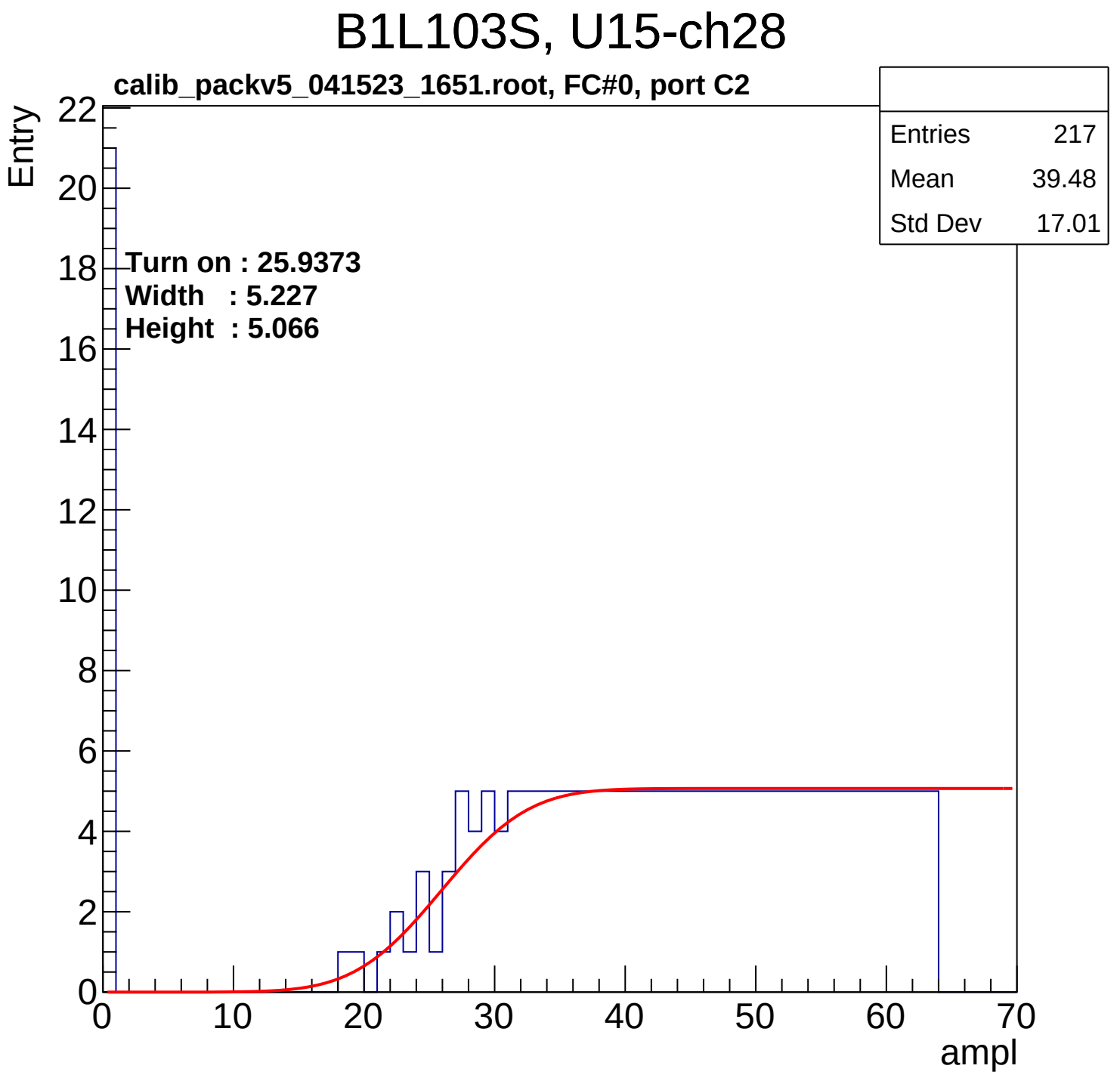
B1L103S, U15-ch28
calib_packv5_041523_1651.root, FC#0, port C2
Entries 217
Mean 39.48
Std Dev 17.01
Turn on : 25.9373
Width : 5.227
Height : 5.066
Entry
ampl
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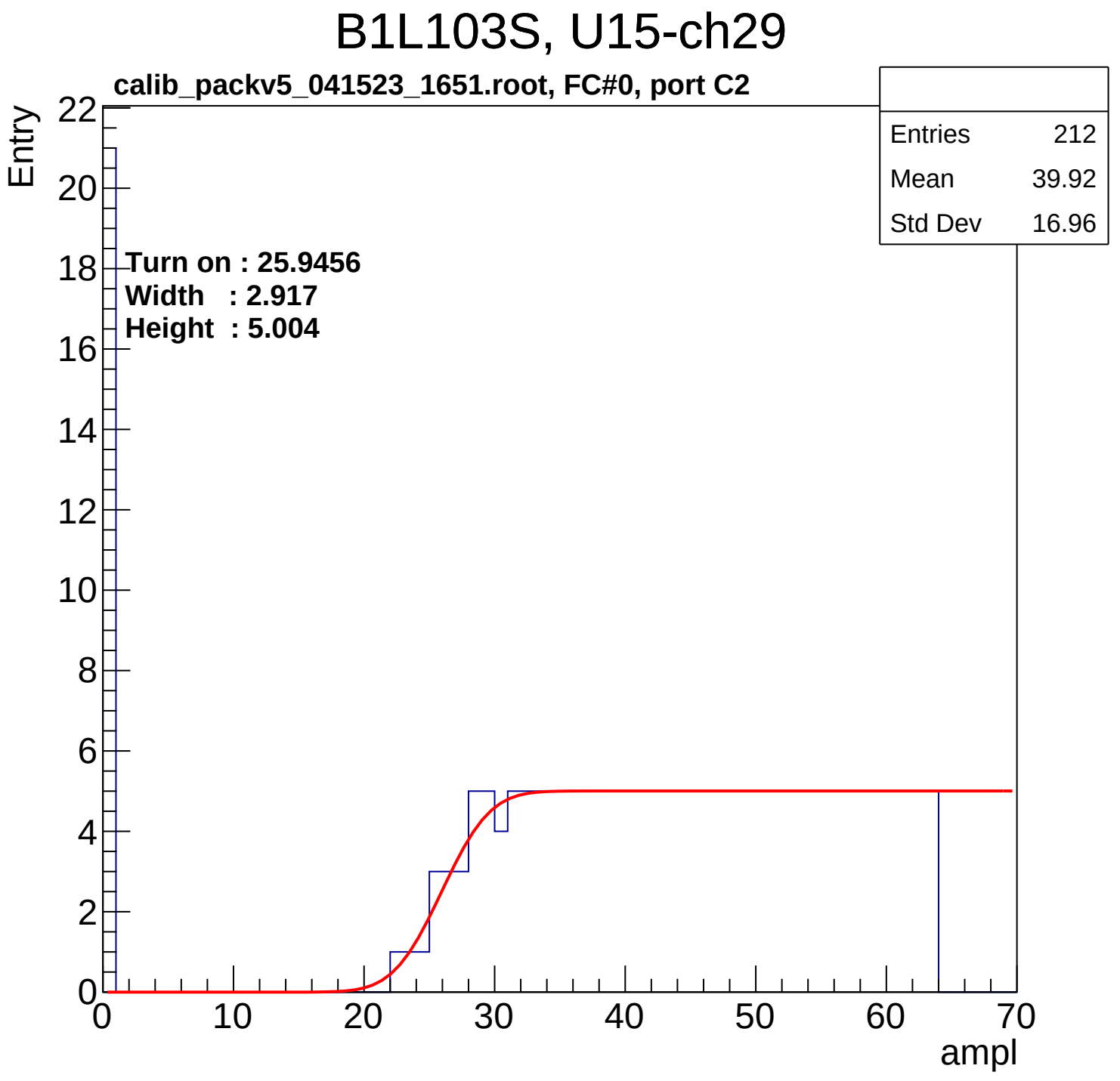
B1L103S, U15-ch29
calib_packv5_041523_1651.root, FC#0, port C2
Entries 212
Mean 39.92
Std Dev 16.96
Turn on : 25.9456
Width : 2.917
Height : 5.004
Entry
ampl
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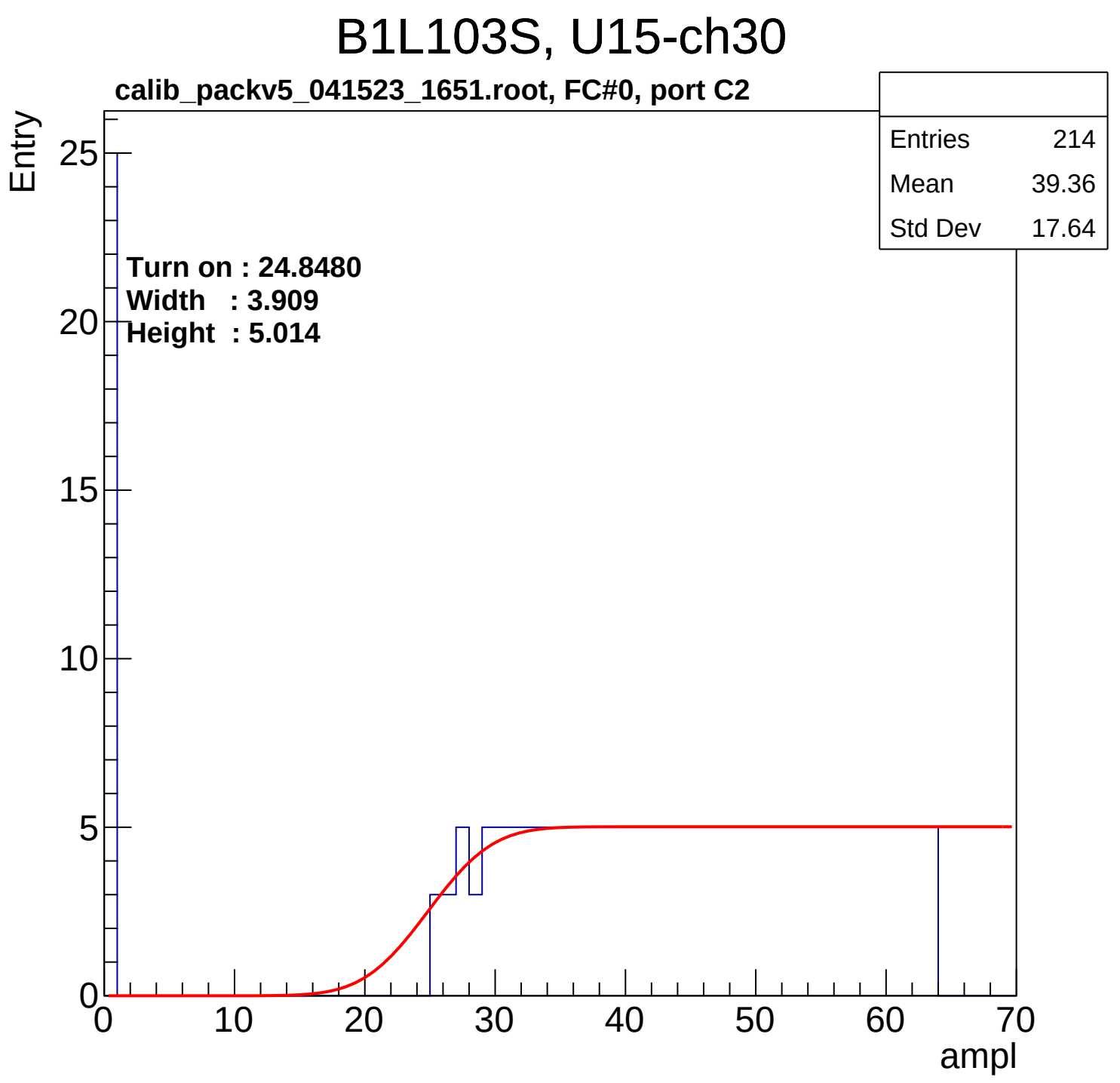
B1L103S, U15-ch30
calib_packv5_041523_1651.root, FC#0, port C2
Entries 214
Mean 39.36
Std Dev 17.64
Turn on : 24.8480
Width : 3.909
Height : 5.014
Entry
ampl
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10
15
20
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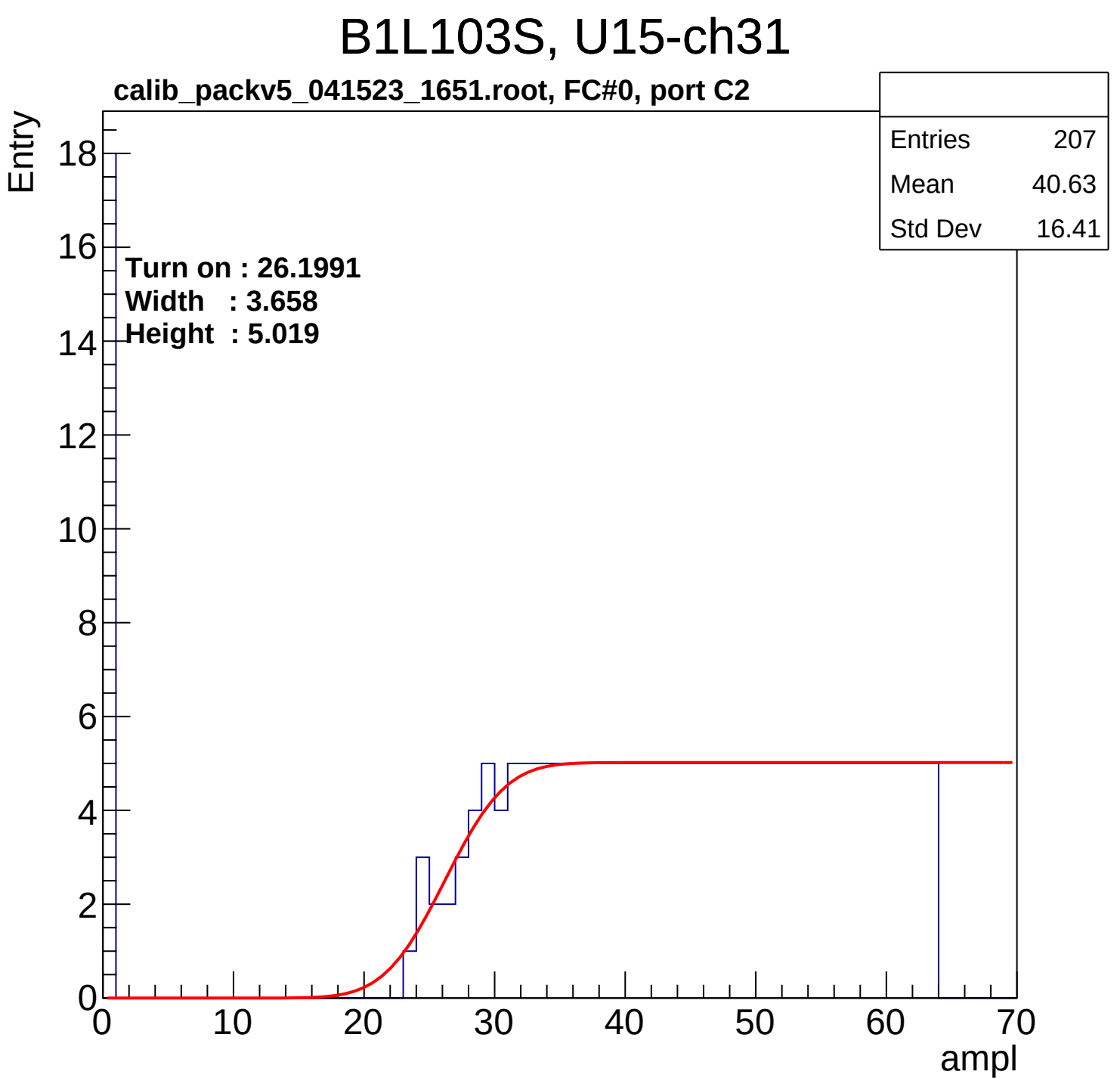
B1L103S, U15-ch31
calib_packv5_041523_1651.root, FC#0, port C2
Entries 207
Mean 40.63
Std Dev 16.41
Turn on : 26.1991
Width : 3.658
Height : 5.019
Entry
ampl
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4
6
8
10
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0
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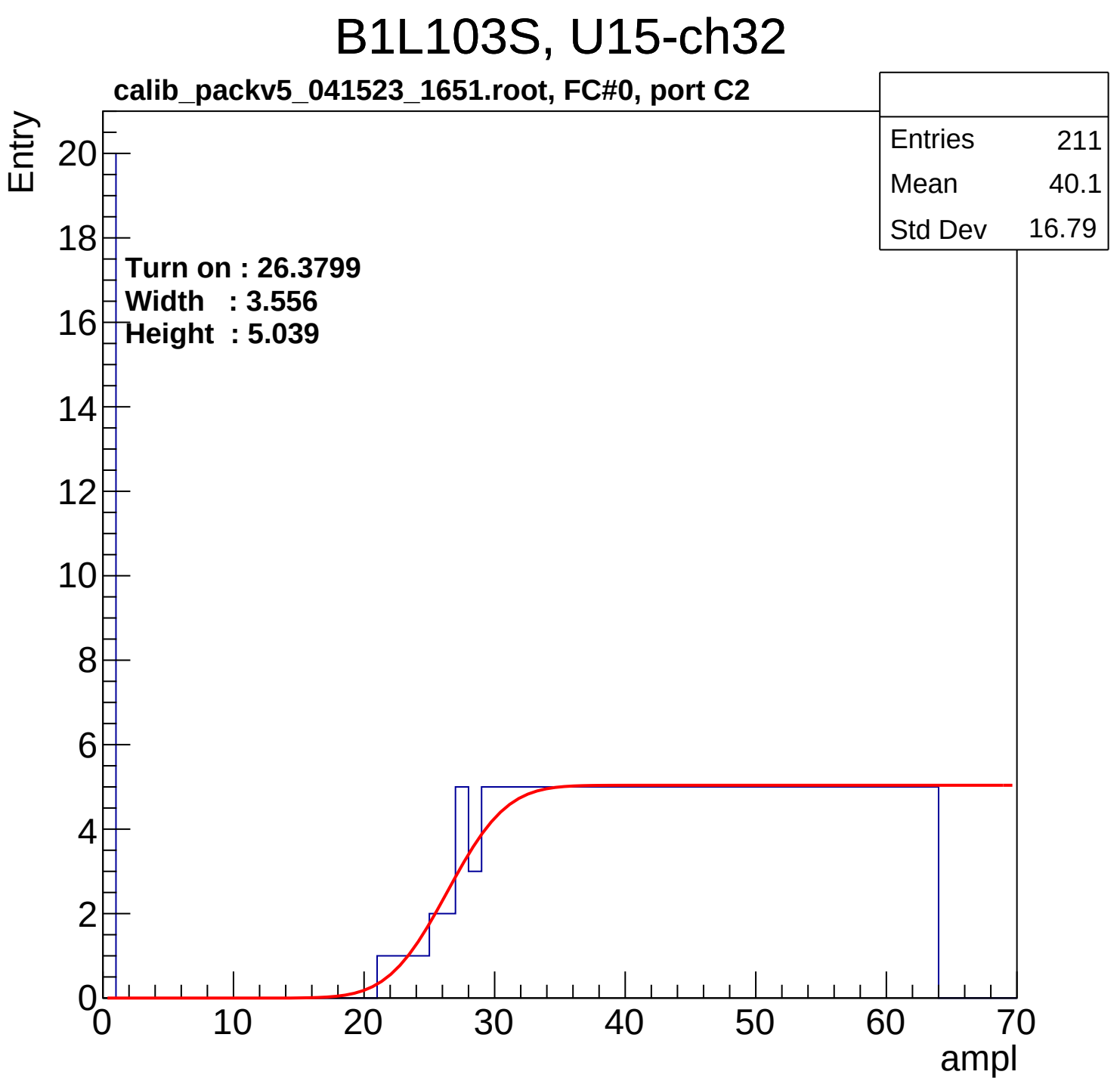
B1L103S, U15-ch32
calib_packv5_041523_1651.root, FC#0, port C2
Entries 211
Mean 40.1
Std Dev 16.79
Turn on : 26.3799
Width : 3.556
Height : 5.039
Entry
ampl
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6
8
10
12
14
16
18
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60
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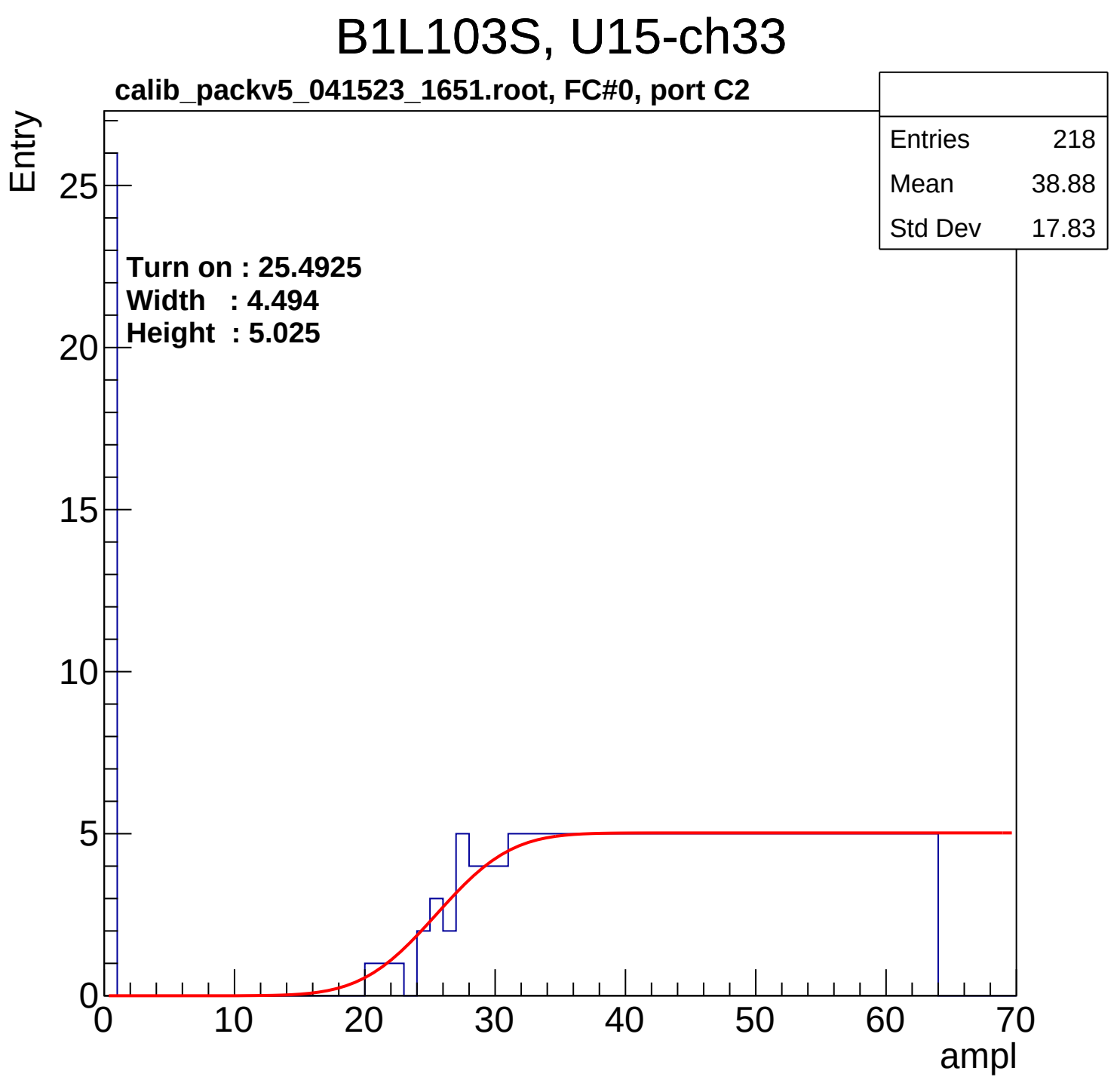
B1L103S, U15-ch33
calib_packv5_041523_1651.root, FC#0, port C2
Entries 218
Mean 38.88
Std Dev 17.83
Turn on : 25.4925
Width : 4.494
Height : 5.025
Entry
ampl
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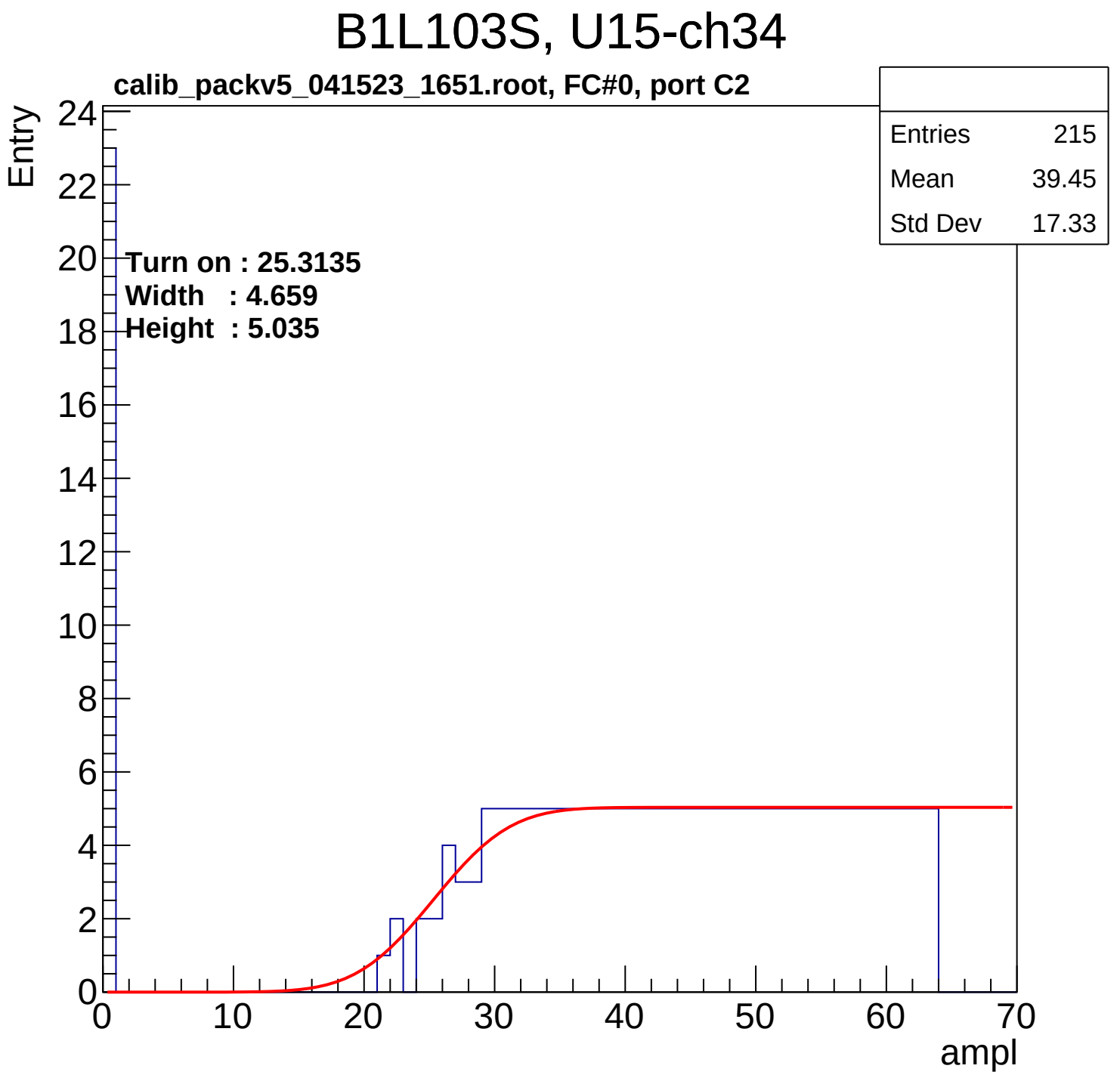
B1L103S, U15-ch34
calib_packv5_041523_1651.root, FC#0, port C2
Entries 215
Mean 39.45
Std Dev 17.33
Turn on : 25.3135
Width : 4.659
Height : 5.035
Entry
ampl
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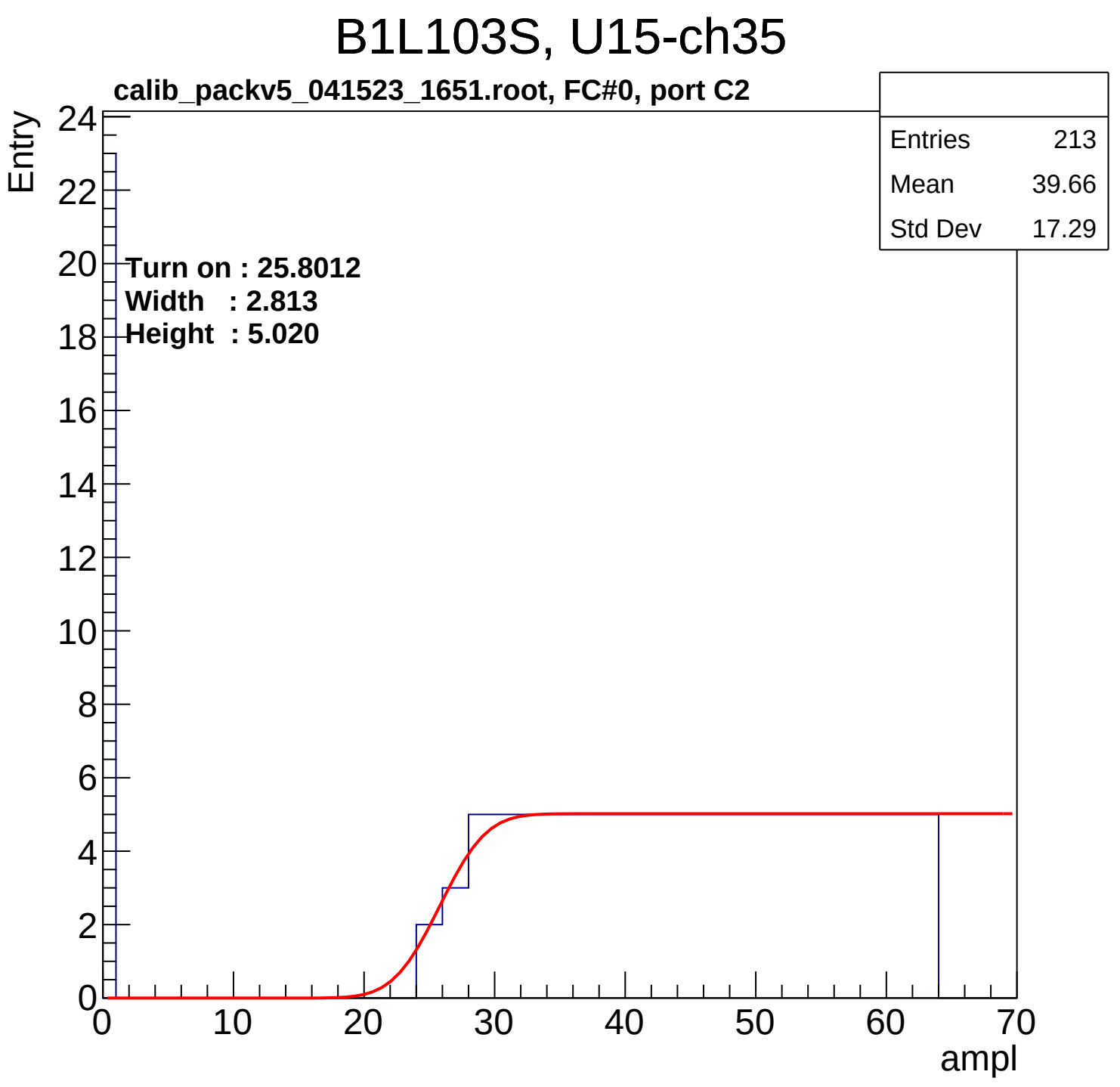
B1L103S, U15-ch35
calib_packv5_041523_1651.root, FC#0, port C2
Entries 213
Mean 39.66
Std Dev 17.29
Turn on : 25.8012
Width : 2.813
Height : 5.020
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
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20
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40
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60
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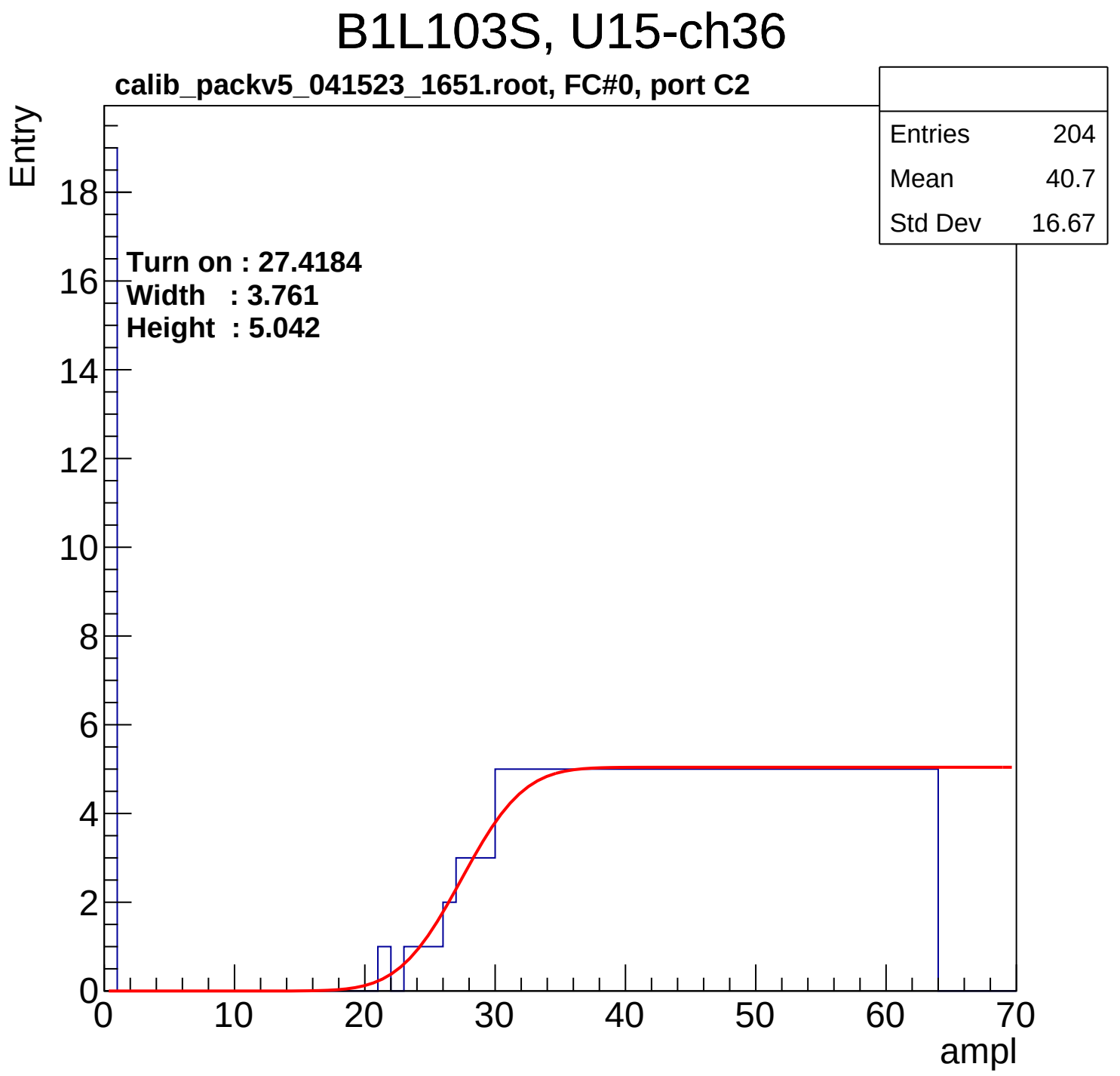
B1L103S, U15-ch36
calib_packv5_041523_1651.root, FC#0, port C2
Entries 204
Mean 40.7
Std Dev 16.67
Turn on : 27.4184
Width : 3.761
Height : 5.042
Entry
ampl
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4
6
8
10
12
14
16
18
0
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20
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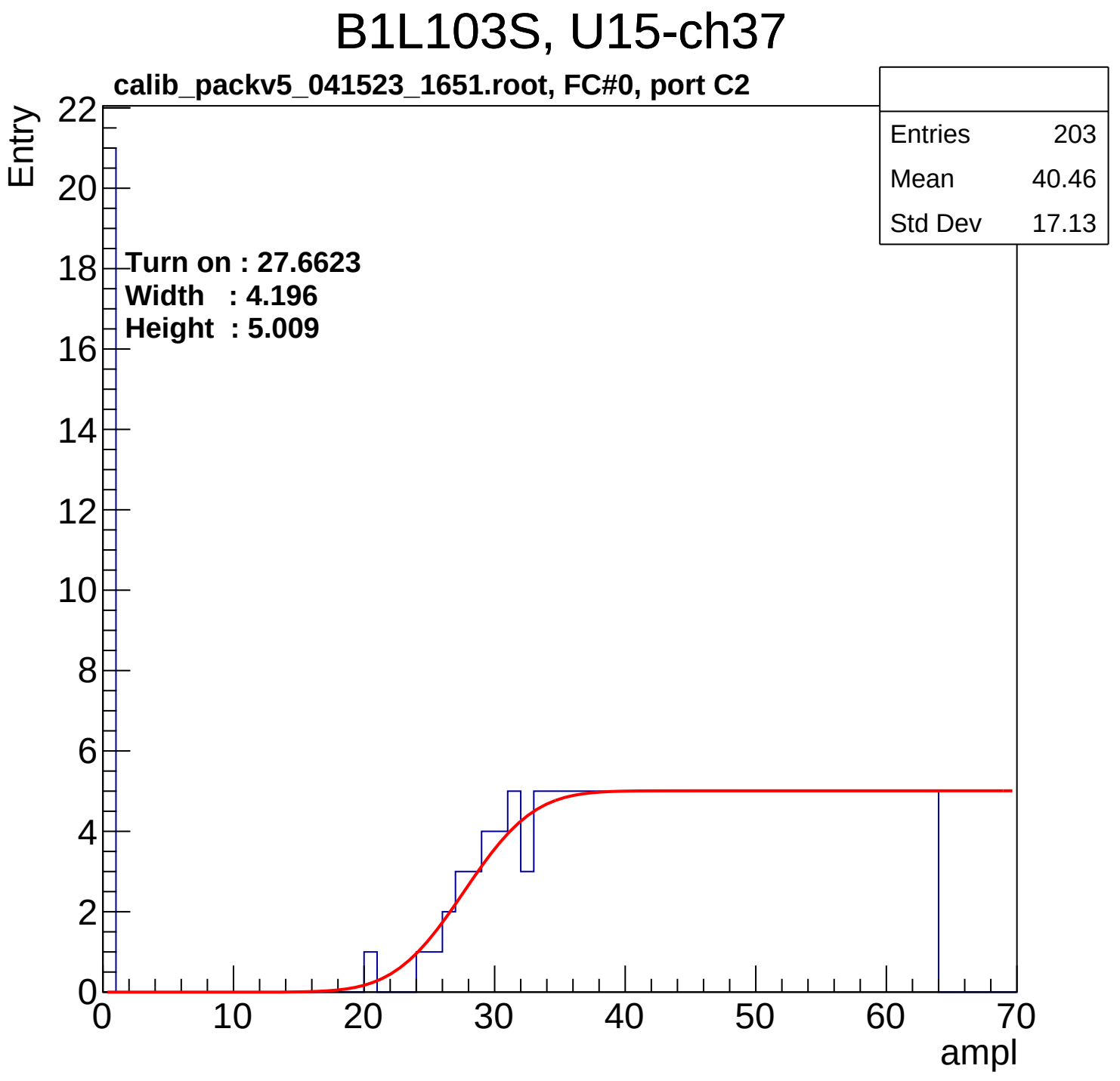
B1L103S, U15-ch37
calib_packv5_041523_1651.root, FC#0, port C2
Entries 203
Mean 40.46
Std Dev 17.13
Turn on : 27.6623
Width : 4.196
Height : 5.009
Entry
ampl
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8
10
12
14
16
18
20
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0
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20
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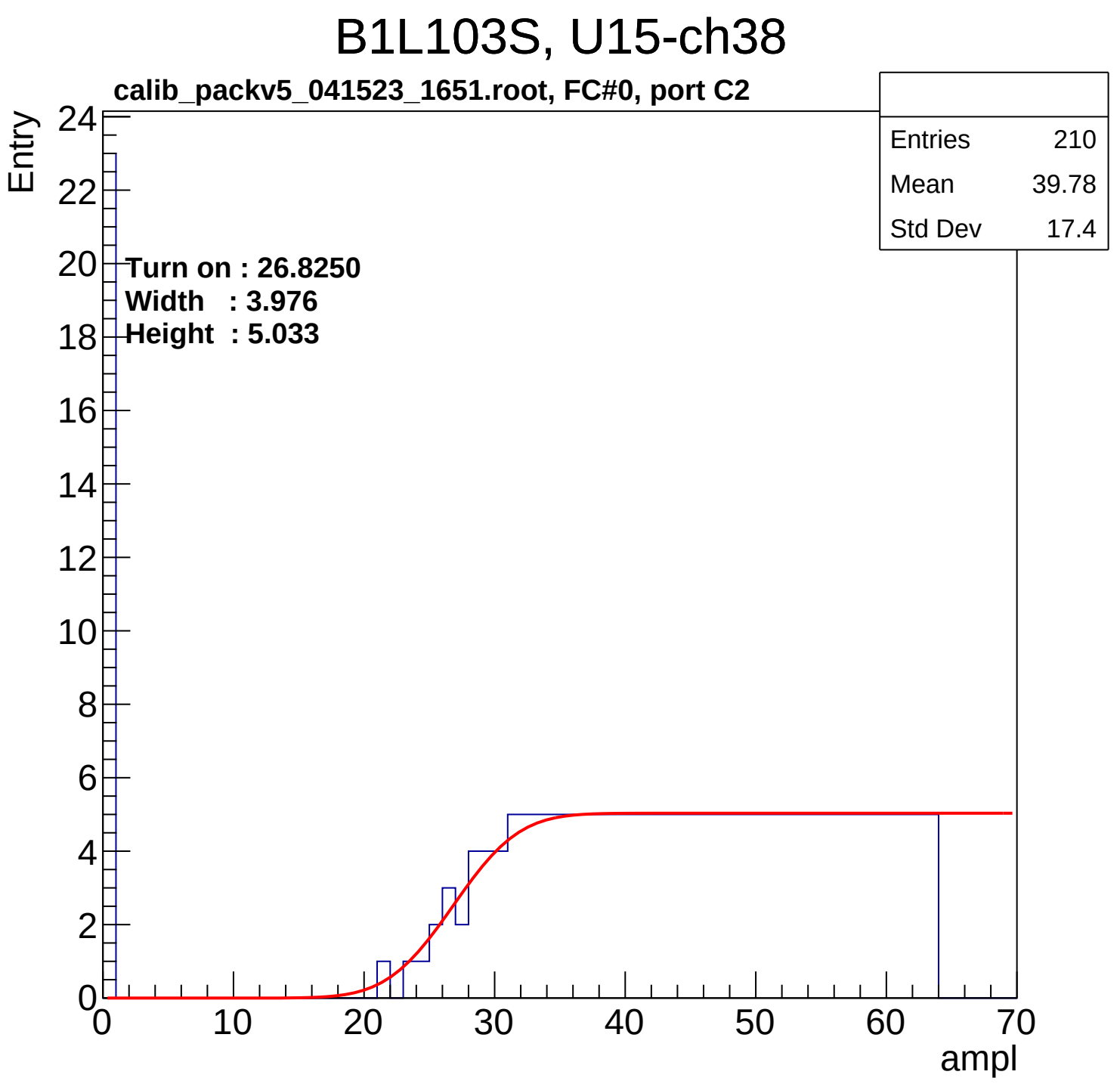
B1L103S, U15-ch38
calib_packv5_041523_1651.root, FC#0, port C2
Entries 210
Mean 39.78
Std Dev 17.4
Turn on : 26.8250
Width : 3.976
Height : 5.033
Entry
ampl
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10
12
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16
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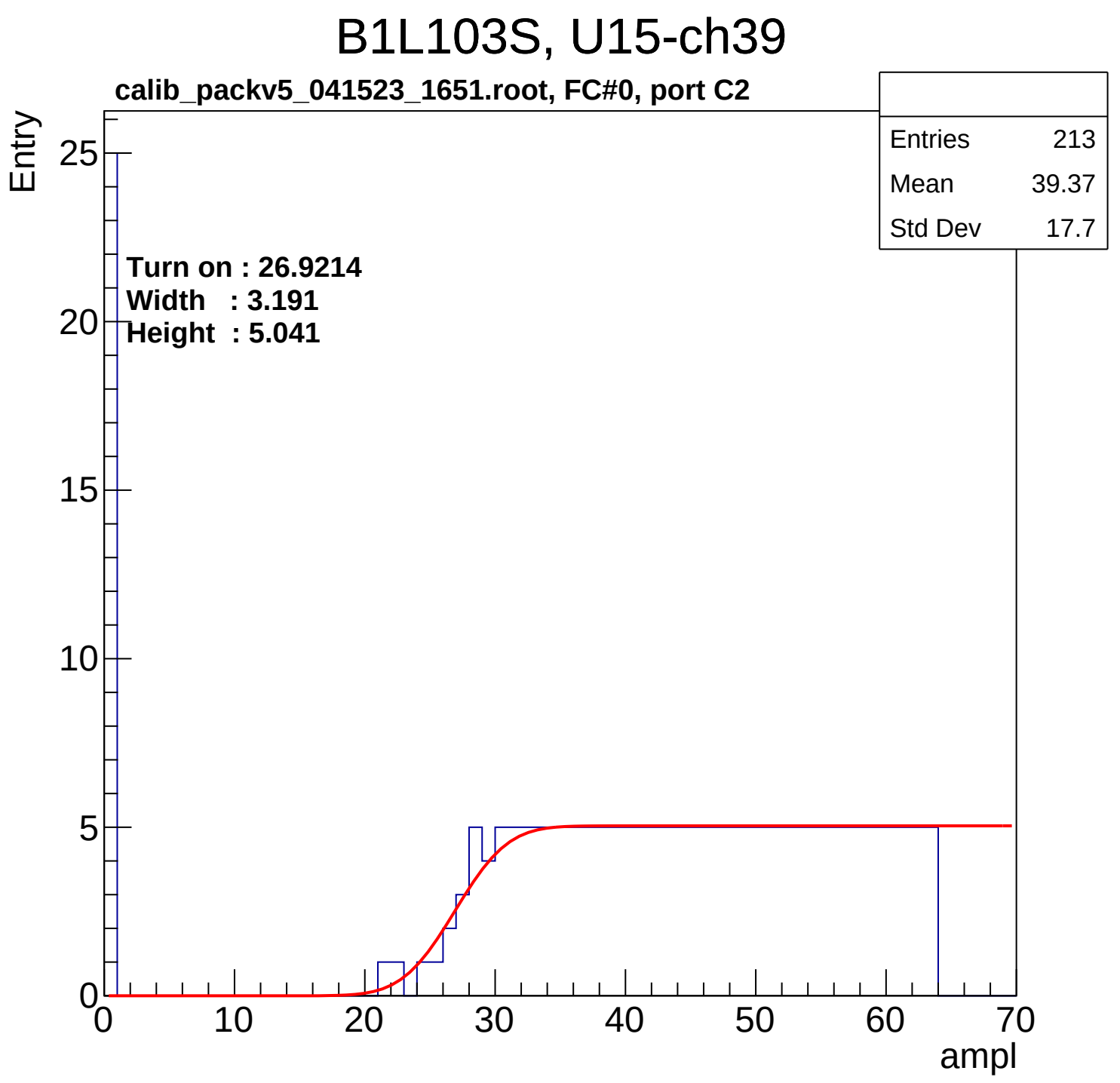
B1L103S, U15-ch39
calib_packv5_041523_1651.root, FC#0, port C2
Entries 213
Mean 39.37
Std Dev 17.7
Turn on : 26.9214
Width : 3.191
Height : 5.041
Entry
ampl
0
5
10
15
20
25
0
10
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40
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60
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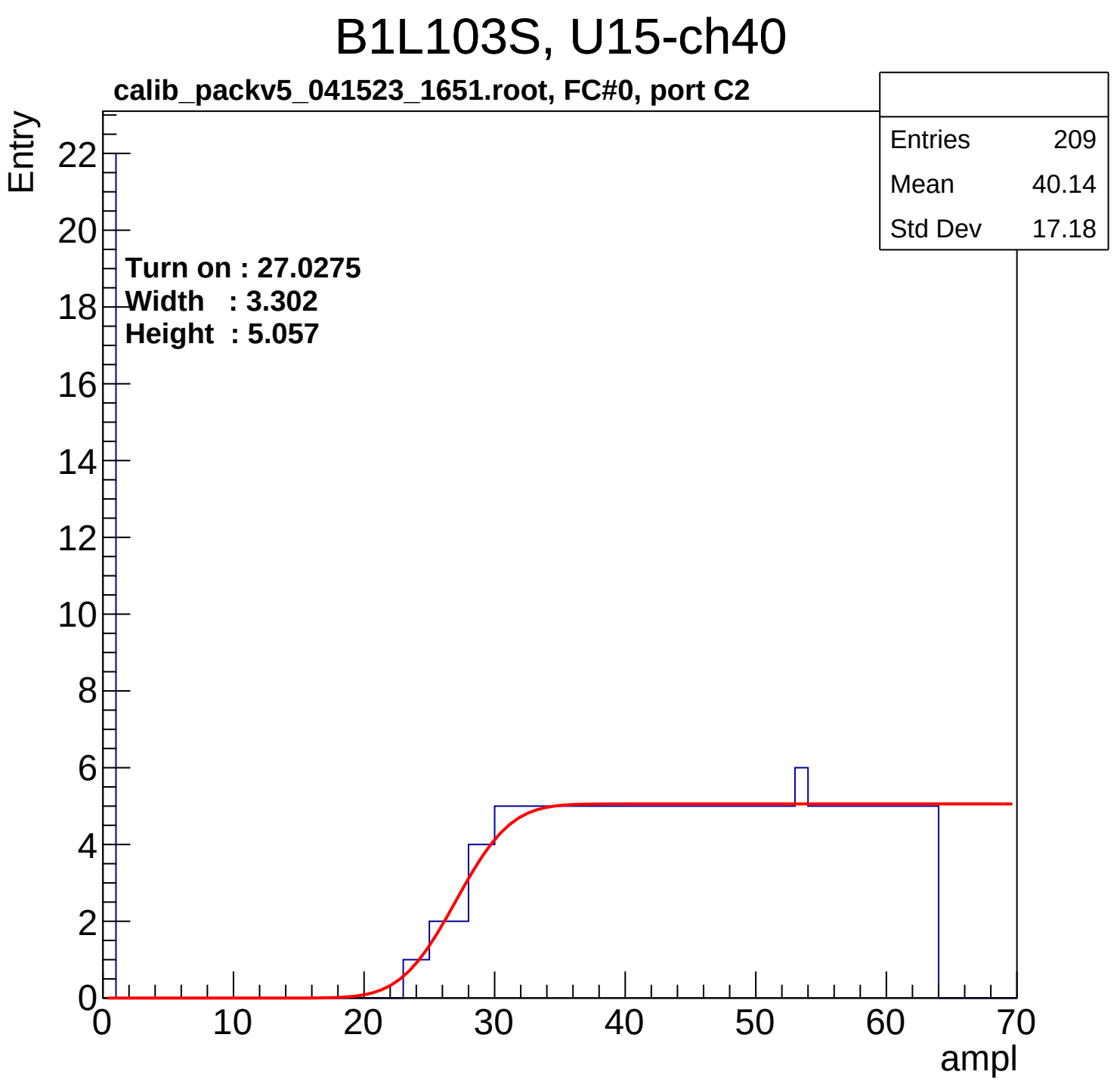
B1L103S, U15-ch40
calib_packv5_041523_1651.root, FC#0, port C2
Entries 209
Mean 40.14
Std Dev 17.18
Turn on : 27.0275
Width : 3.302
Height : 5.057
Entry
ampl
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18
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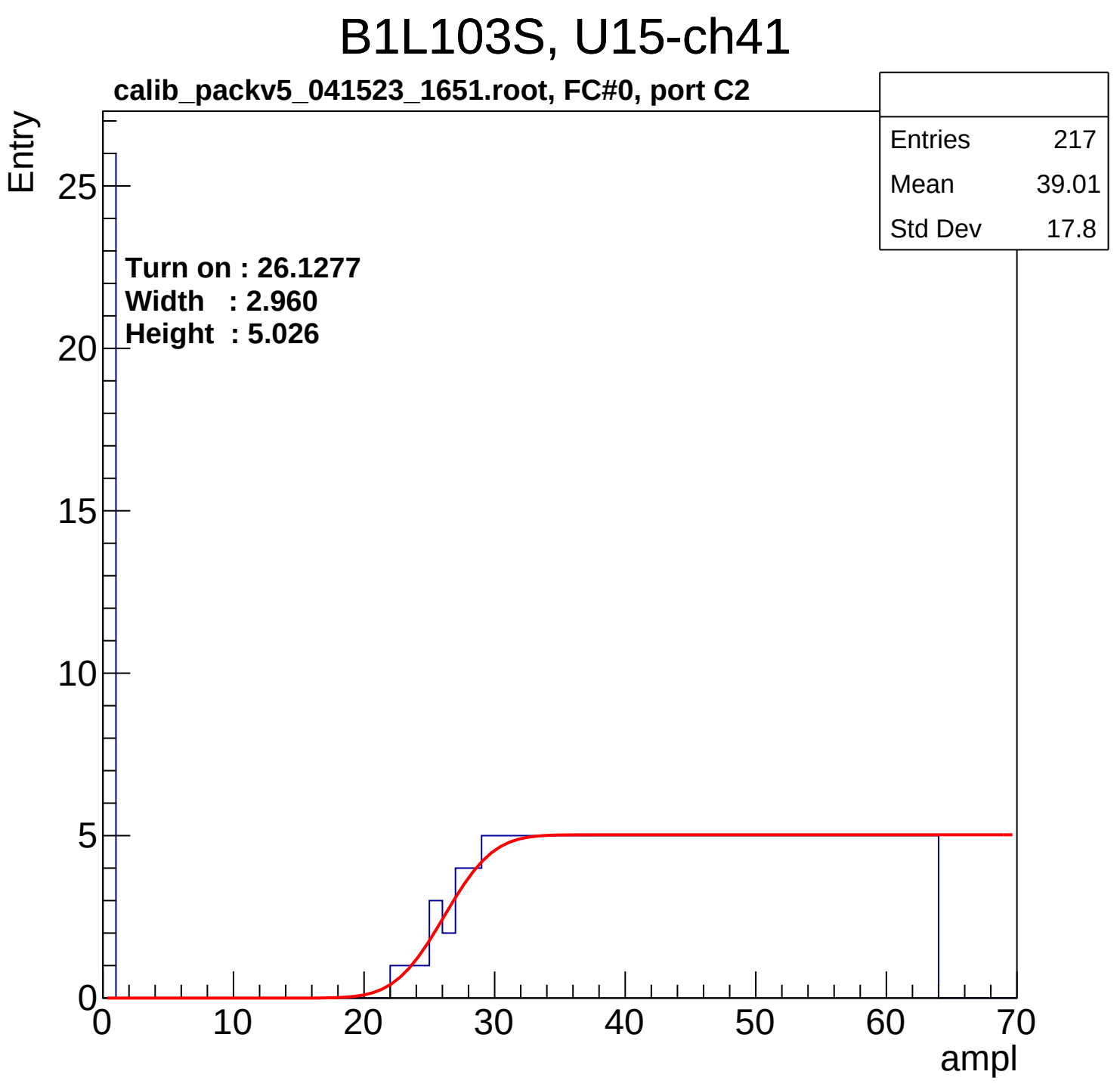
B1L103S, U15-ch41
calib_packv5_041523_1651.root, FC#0, port C2
Entries 217
Mean 39.01
Std Dev 17.8
Turn on : 26.1277
Width : 2.960
Height : 5.026
Entry
ampl
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20
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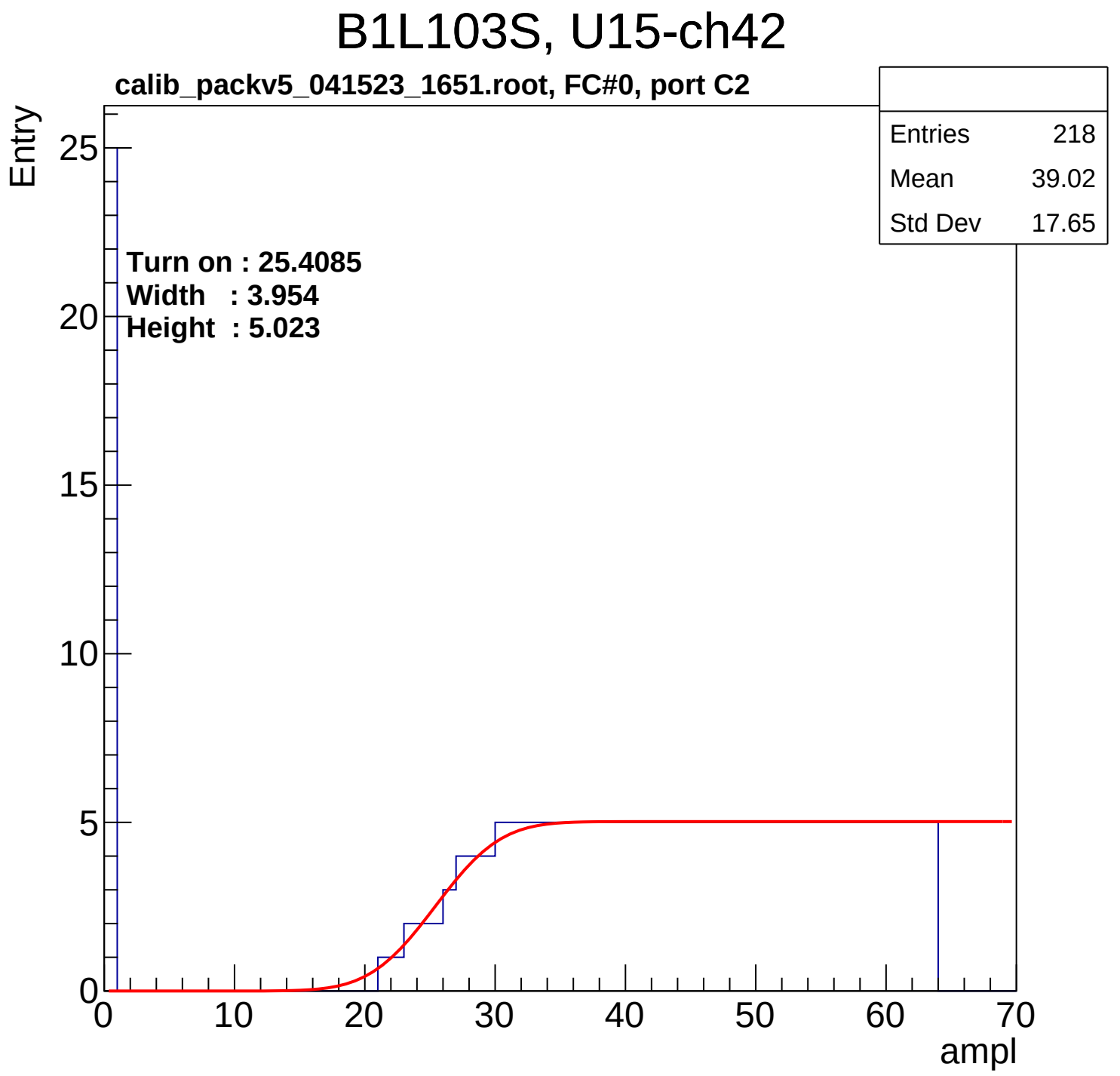
B1L103S, U15-ch42
calib_packv5_041523_1651.root, FC#0, port C2
Entries 218
Mean 39.02
Std Dev 17.65
Turn on : 25.4085
Width : 3.954
Height : 5.023
Entry
ampl
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10
15
20
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40
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60
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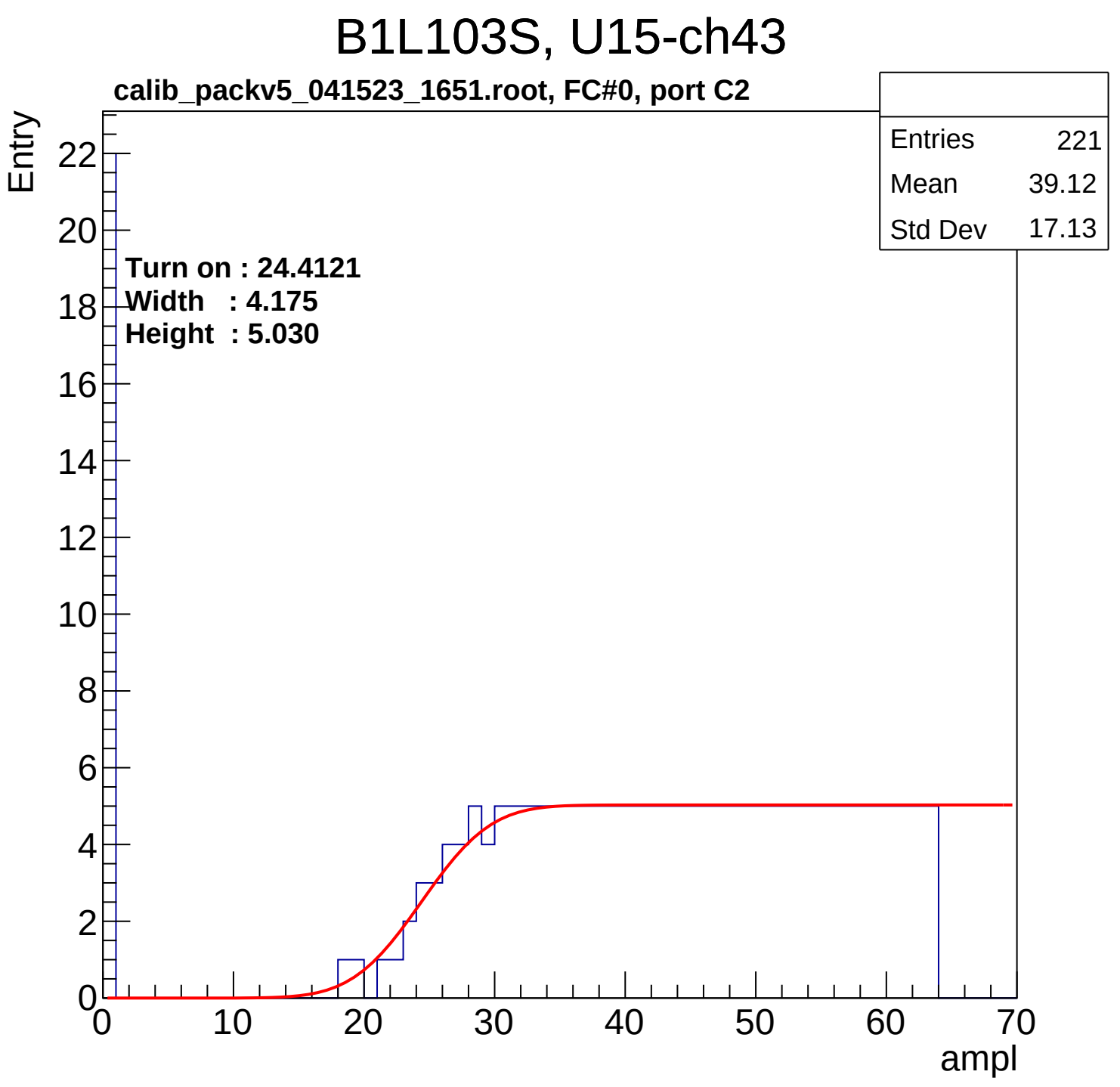
B1L103S, U15-ch43
calib_packv5_041523_1651.root, FC#0, port C2
Entries 221
Mean 39.12
Std Dev 17.13
Turn on : 24.4121
Width : 4.175
Height : 5.030
Entry
ampl
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8
10
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16
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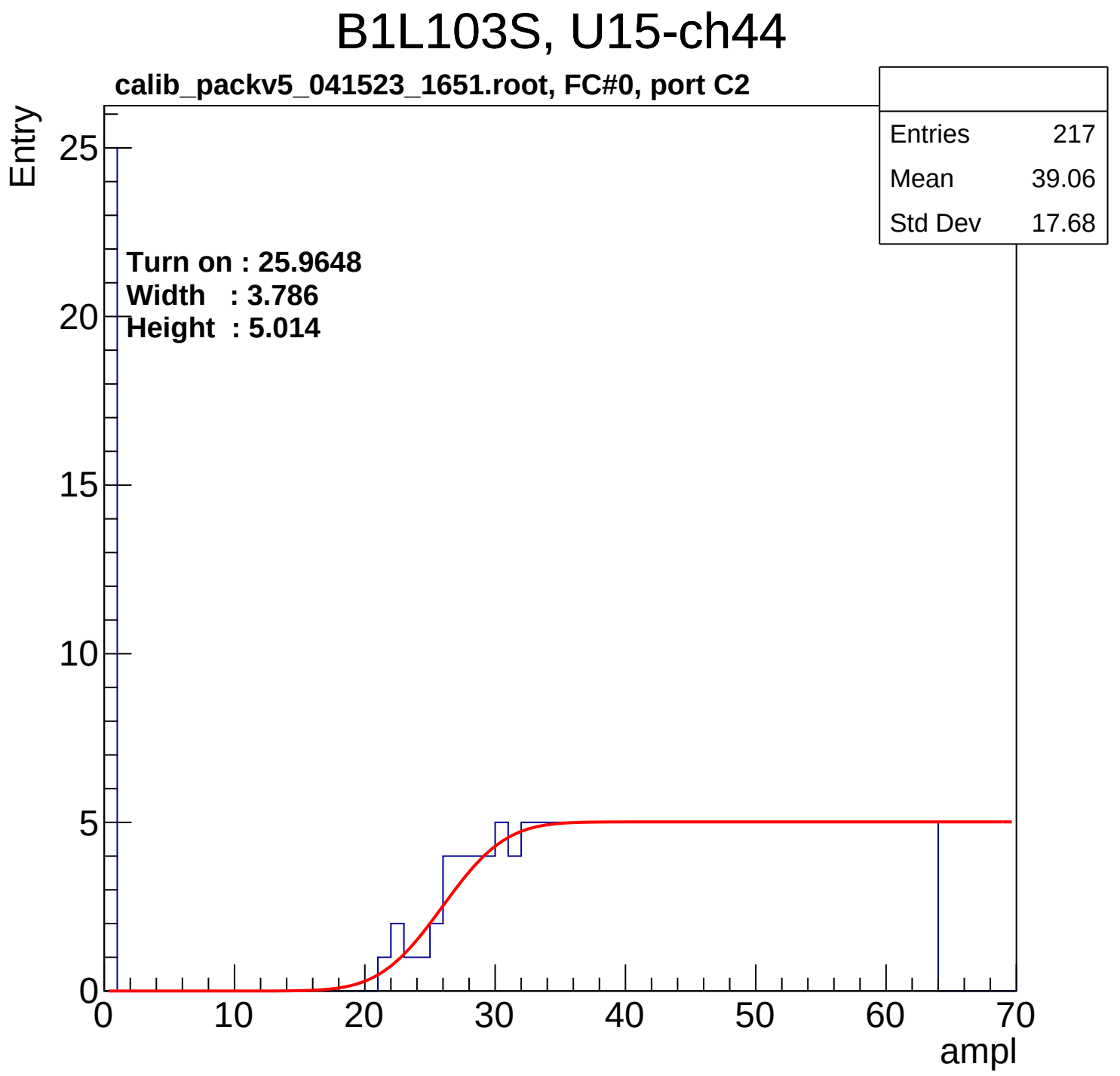
B1L103S, U15-ch44
calib_packv5_041523_1651.root, FC#0, port C2
Entries 217
Mean 39.06
Std Dev 17.68
Turn on : 25.9648
Width : 3.786
Height : 5.014
Entry
ampl
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10
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20
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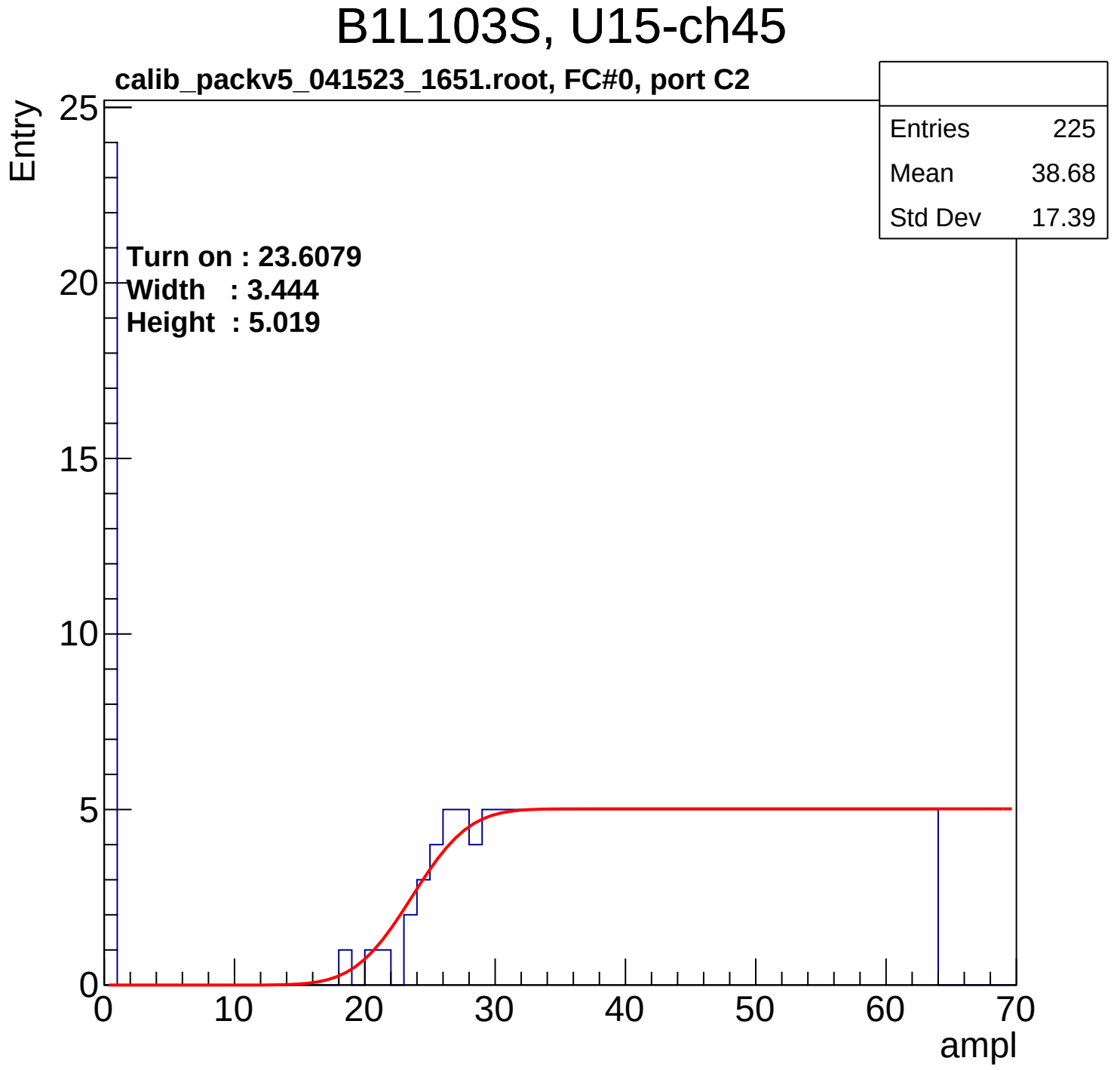
B1L103S, U15-ch45
calib_packv5_041523_1651.root, FC#0, port C2
Entries 225
Mean 38.68
Std Dev 17.39
Turn on : 23.6079
Width : 3.444
Height : 5.019
Entry
ampl
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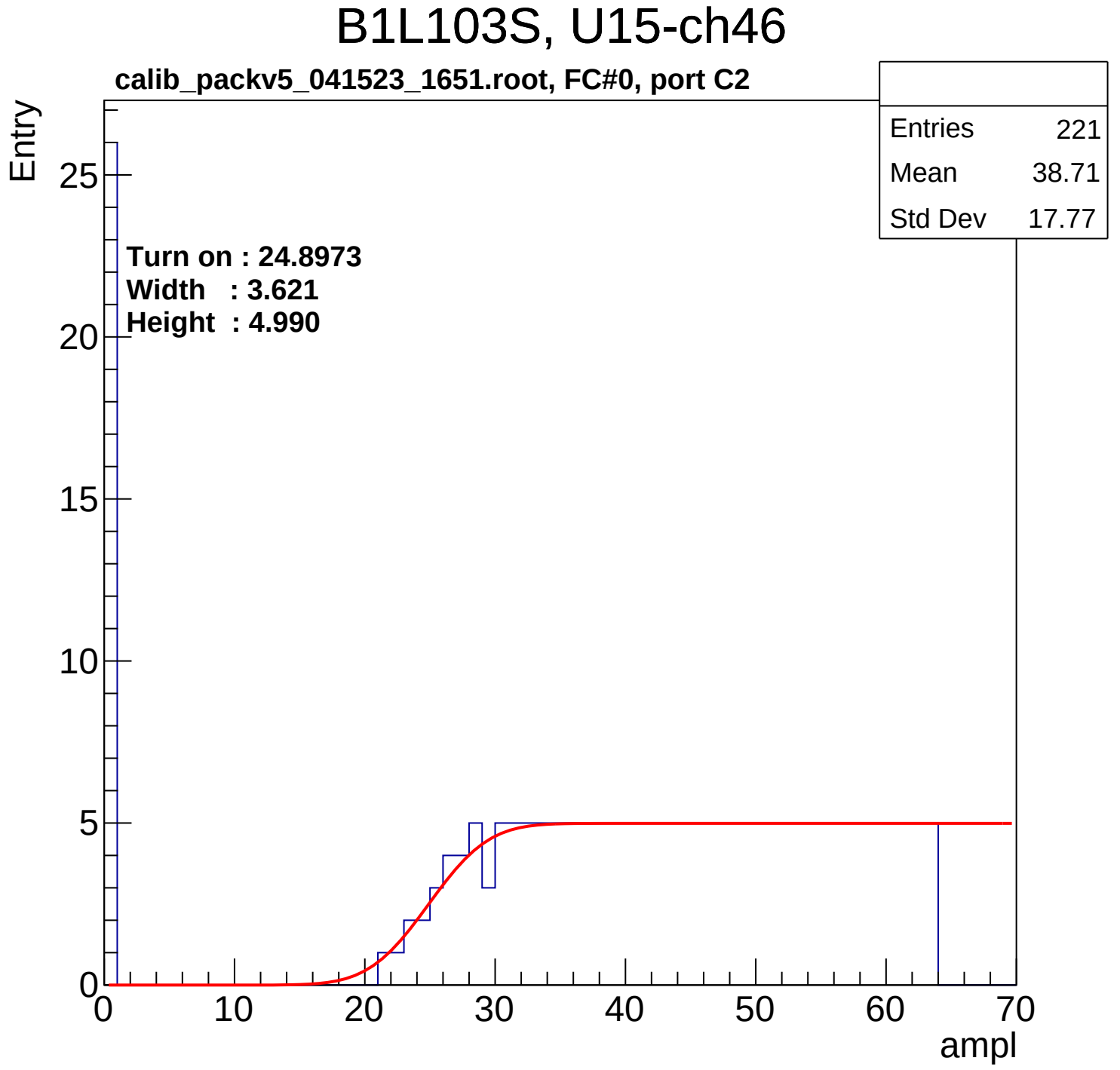
B1L103S, U15-ch46
calib_packv5_041523_1651.root, FC#0, port C2
Entries 221
Mean 38.71
Std Dev 17.77
Turn on : 24.8973
Width : 3.621
Height : 4.990
Entry
ampl
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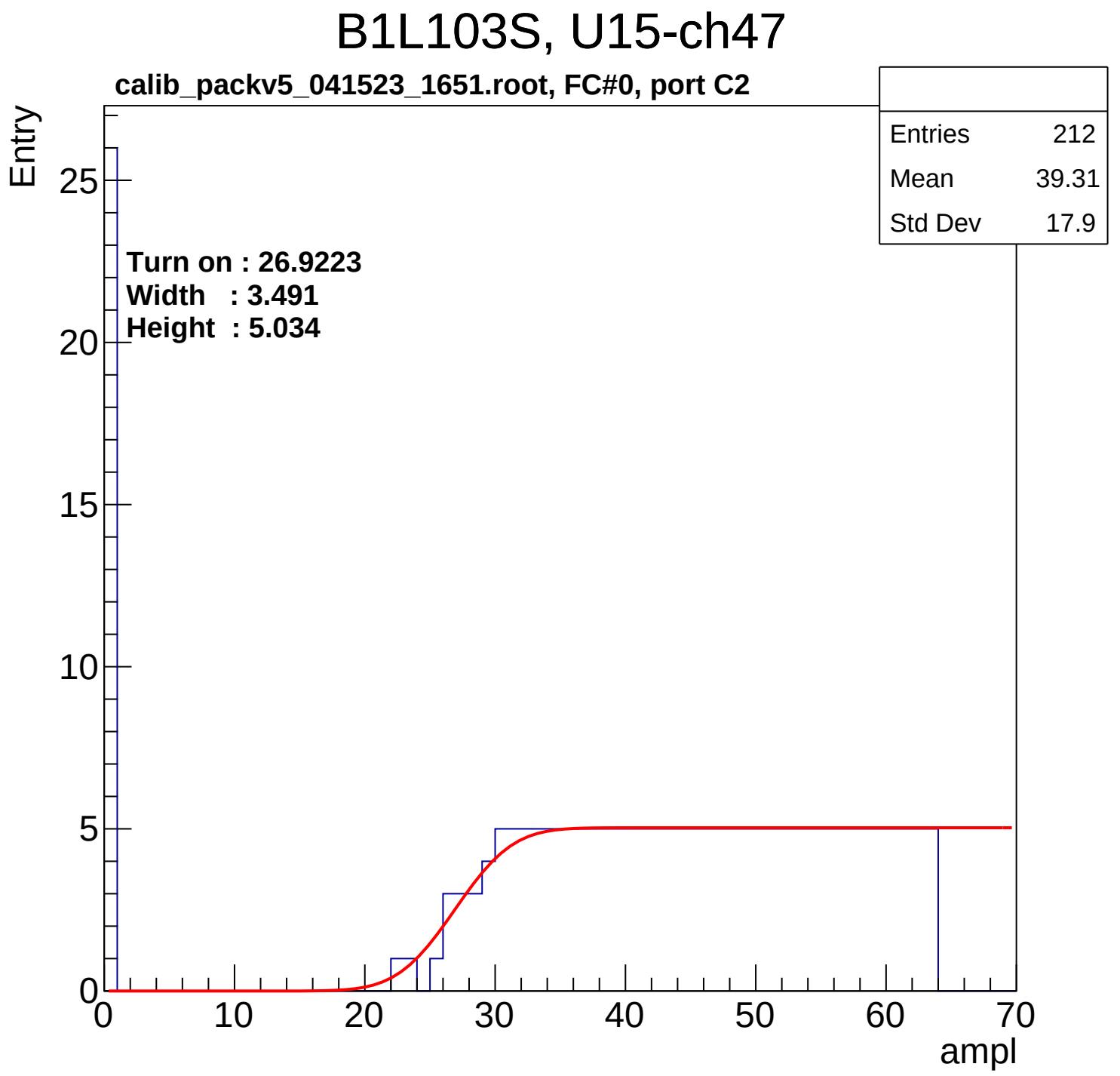
B1L103S, U15-ch47
calib_packv5_041523_1651.root, FC#0, port C2
Entries 212
Mean 39.31
Std Dev 17.9
Turn on : 26.9223
Width : 3.491
Height : 5.034
Entry
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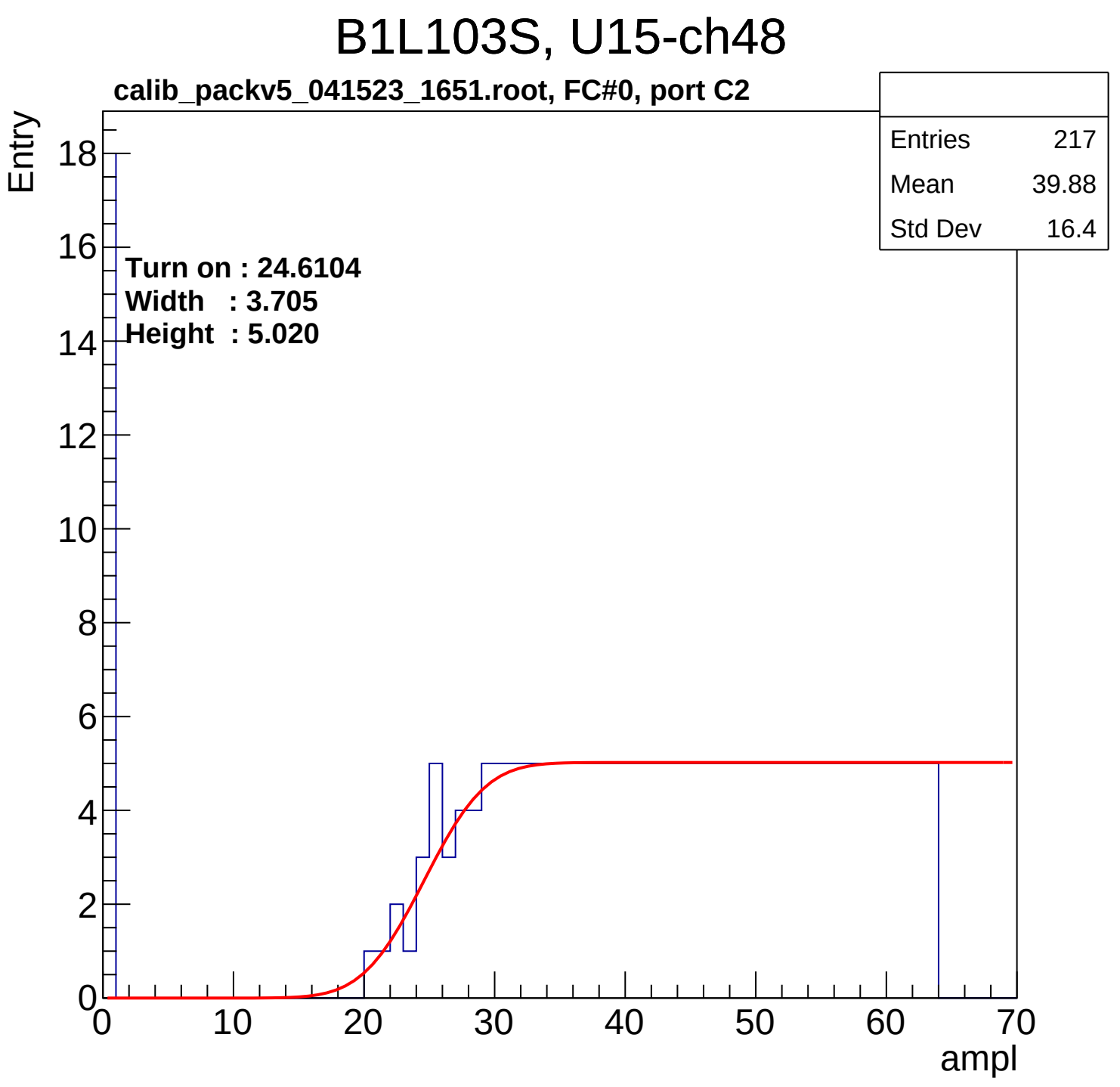
70
ampl


B1L103S, U15-ch48
calib_packv5_041523_1651.root, FC#0, port C2
Entries 217
Mean 39.88
Std Dev 16.4
Turn on : 24.6104
Width : 3.705
Height : 5.020
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ampl
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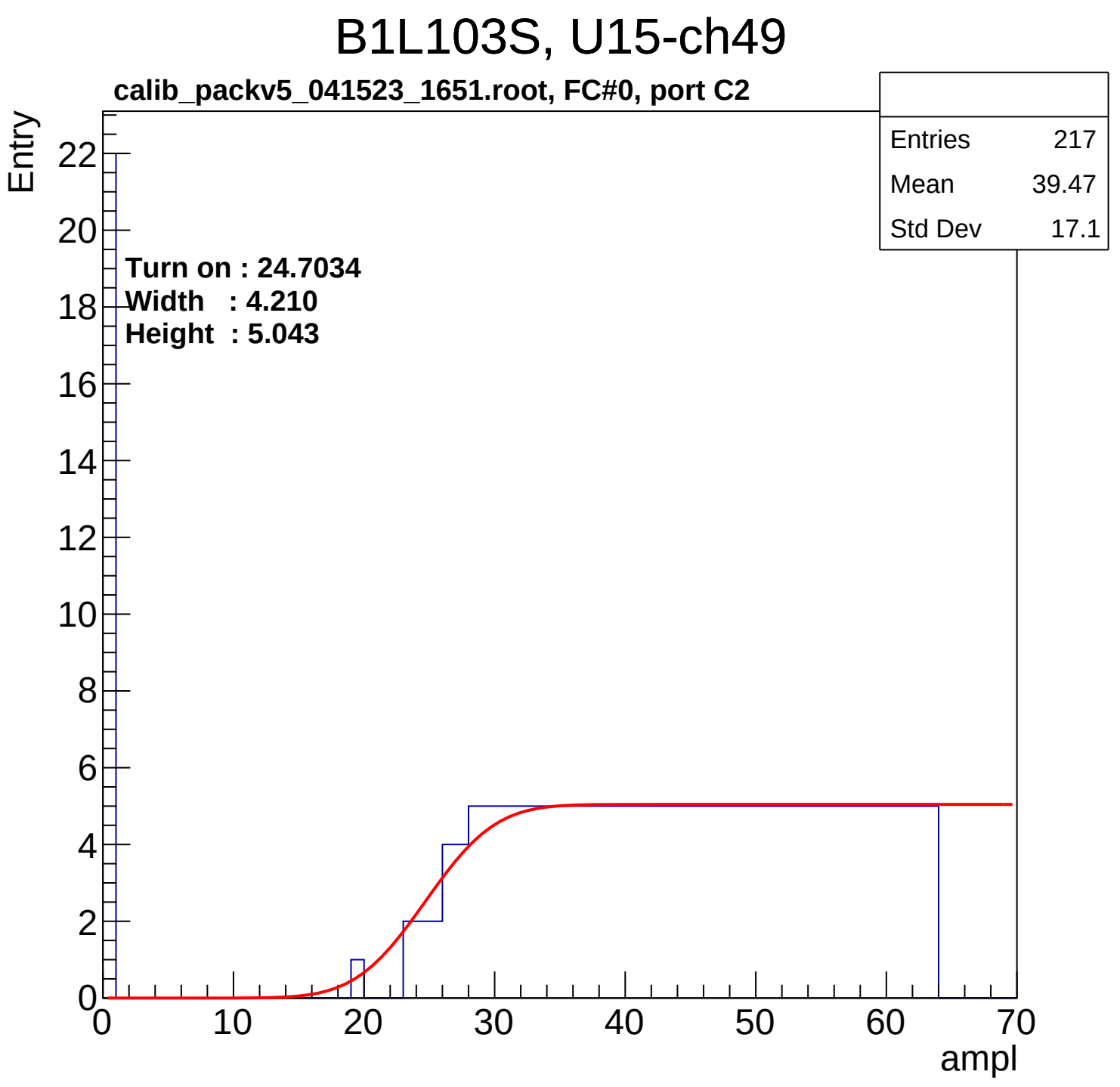
B1L103S, U15-ch49
calib_packv5_041523_1651.root, FC#0, port C2
Entries 217
Mean 39.47
Std Dev 17.1
Turn on : 24.7034
Width : 4.210
Height : 5.043
Entry
ampl
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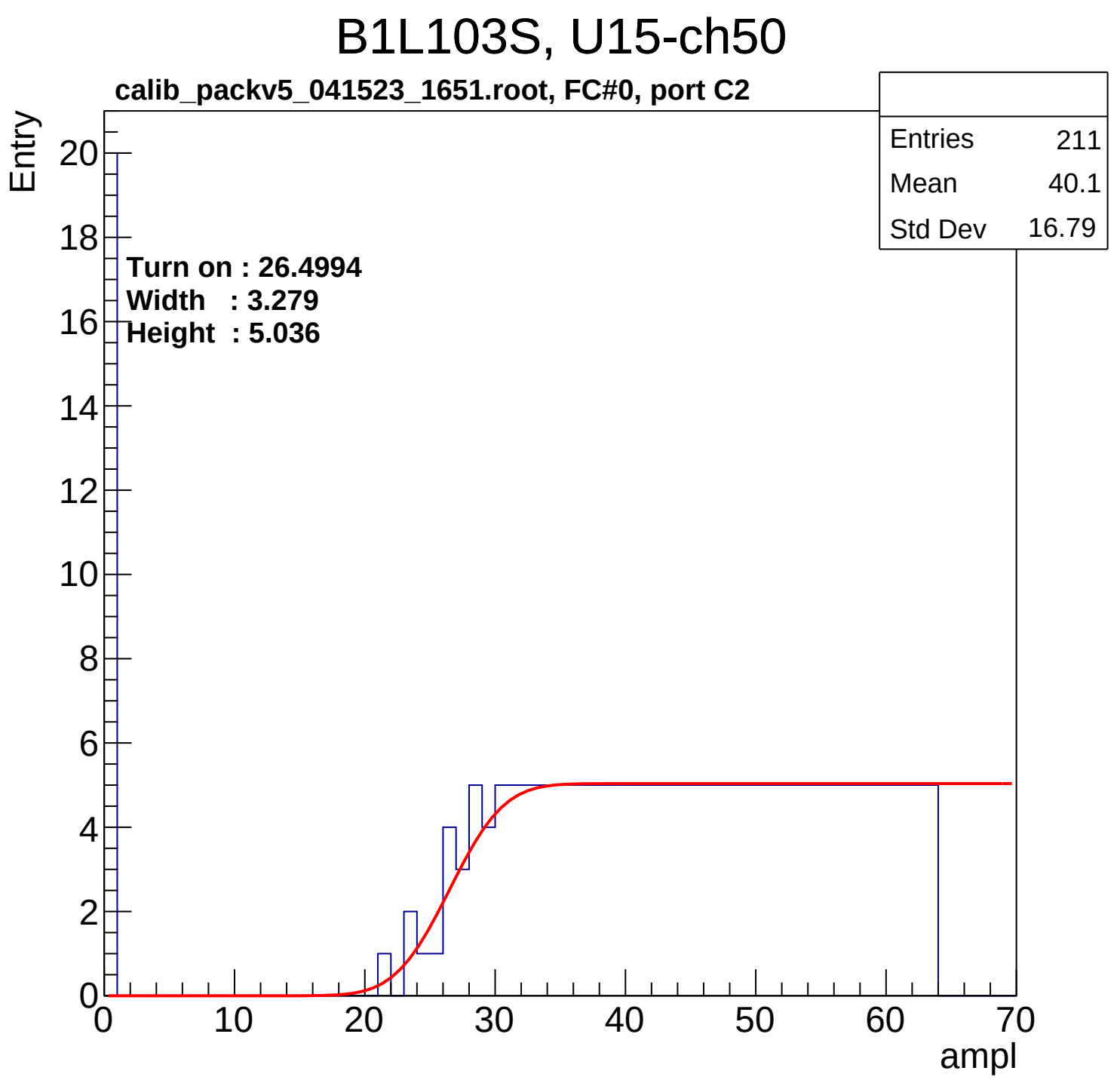
B1L103S, U15-ch50
calib_packv5_041523_1651.root, FC#0, port C2
Entries 211
Mean 40.1
Std Dev 16.79
Turn on : 26.4994
Width : 3.279
Height : 5.036
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ampl
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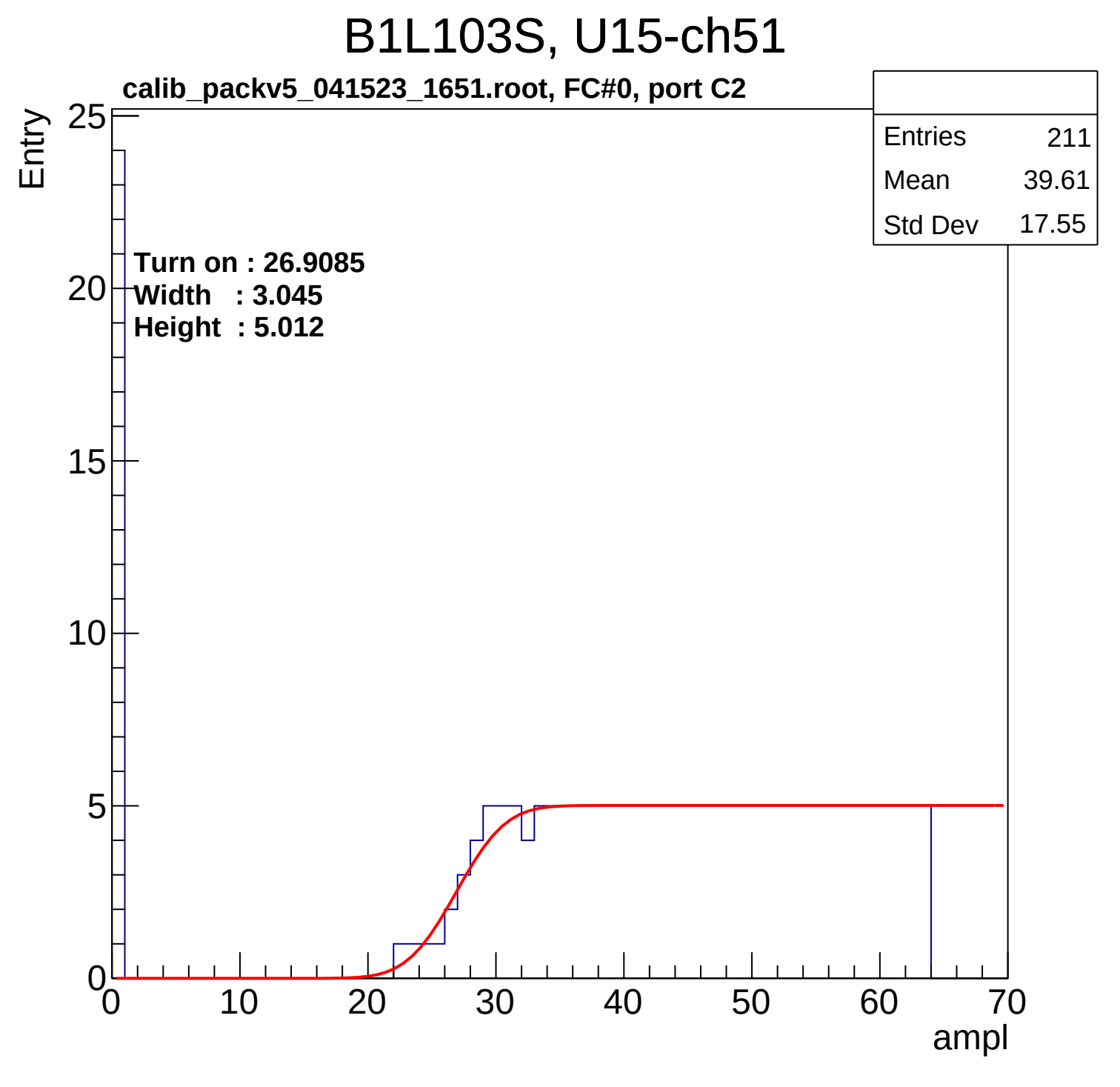
B1L103S, U15-ch51
calib_packv5_041523_1651.root, FC#0, port C2
Entries 211
Mean 39.61
Std Dev 17.55
Turn on : 26.9085
Width : 3.045
Height : 5.012
Entry
ampl
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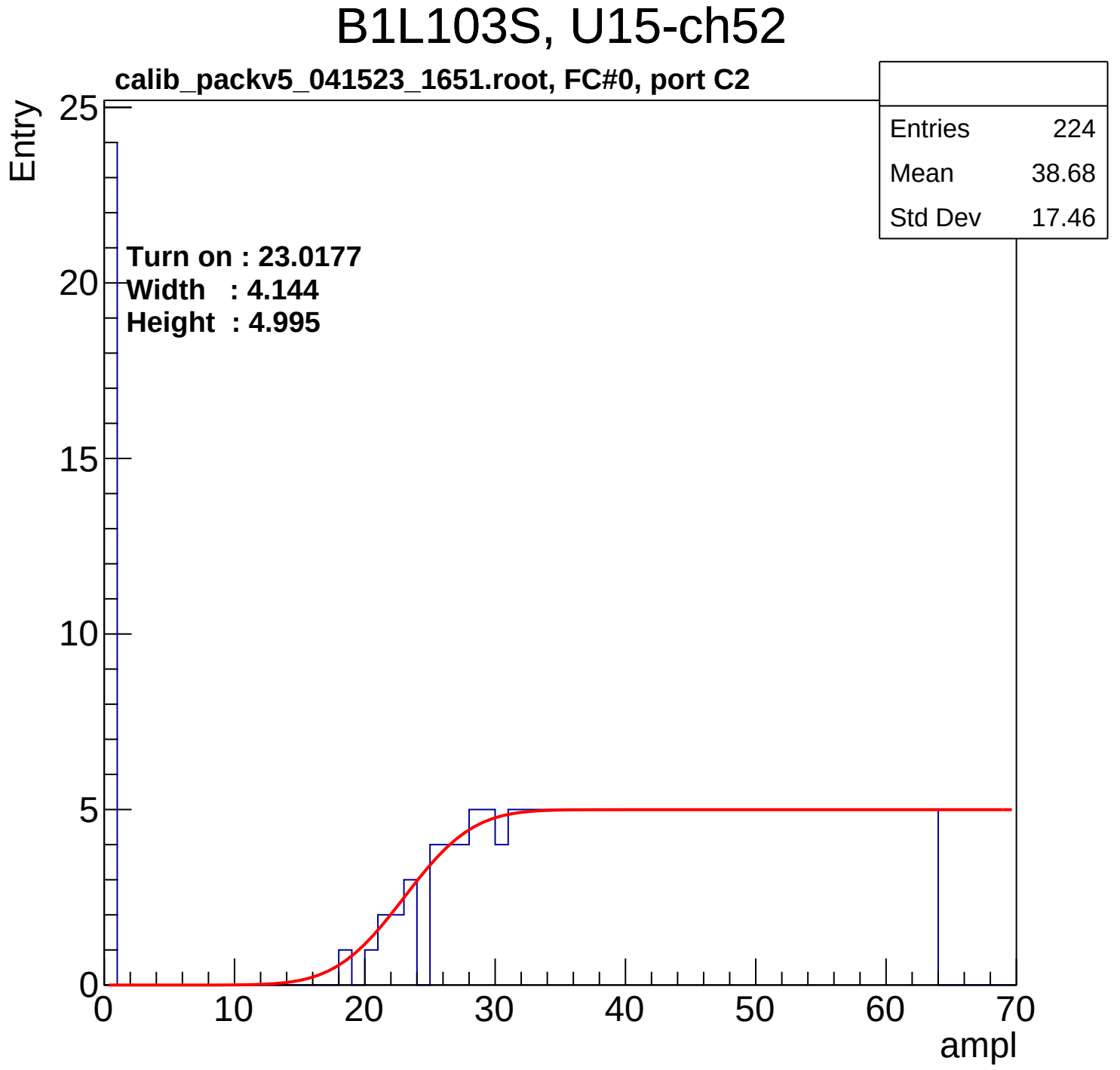
B1L103S, U15-ch52
calib_packv5_041523_1651.root, FC#0, port C2
Entries 224
Mean 38.68
Std Dev 17.46
Turn on : 23.0177
Width : 4.144
Height : 4.995
Entry
ampl
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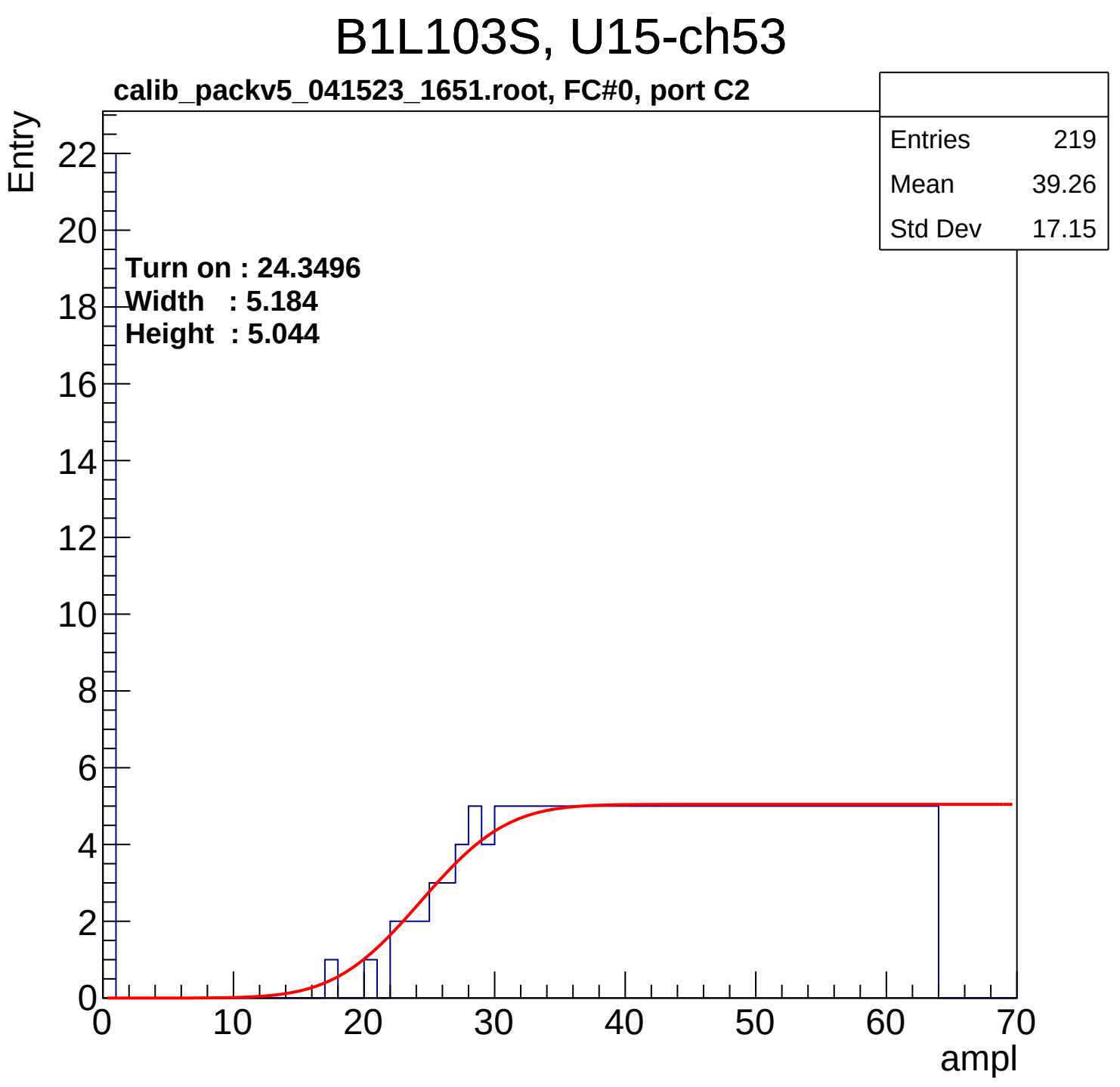
B1L103S, U15-ch53
calib_packv5_041523_1651.root, FC#0, port C2
Entries 219
Mean 39.26
Std Dev 17.15
Turn on : 24.3496
Width : 5.184
Height : 5.044
Entry
ampl
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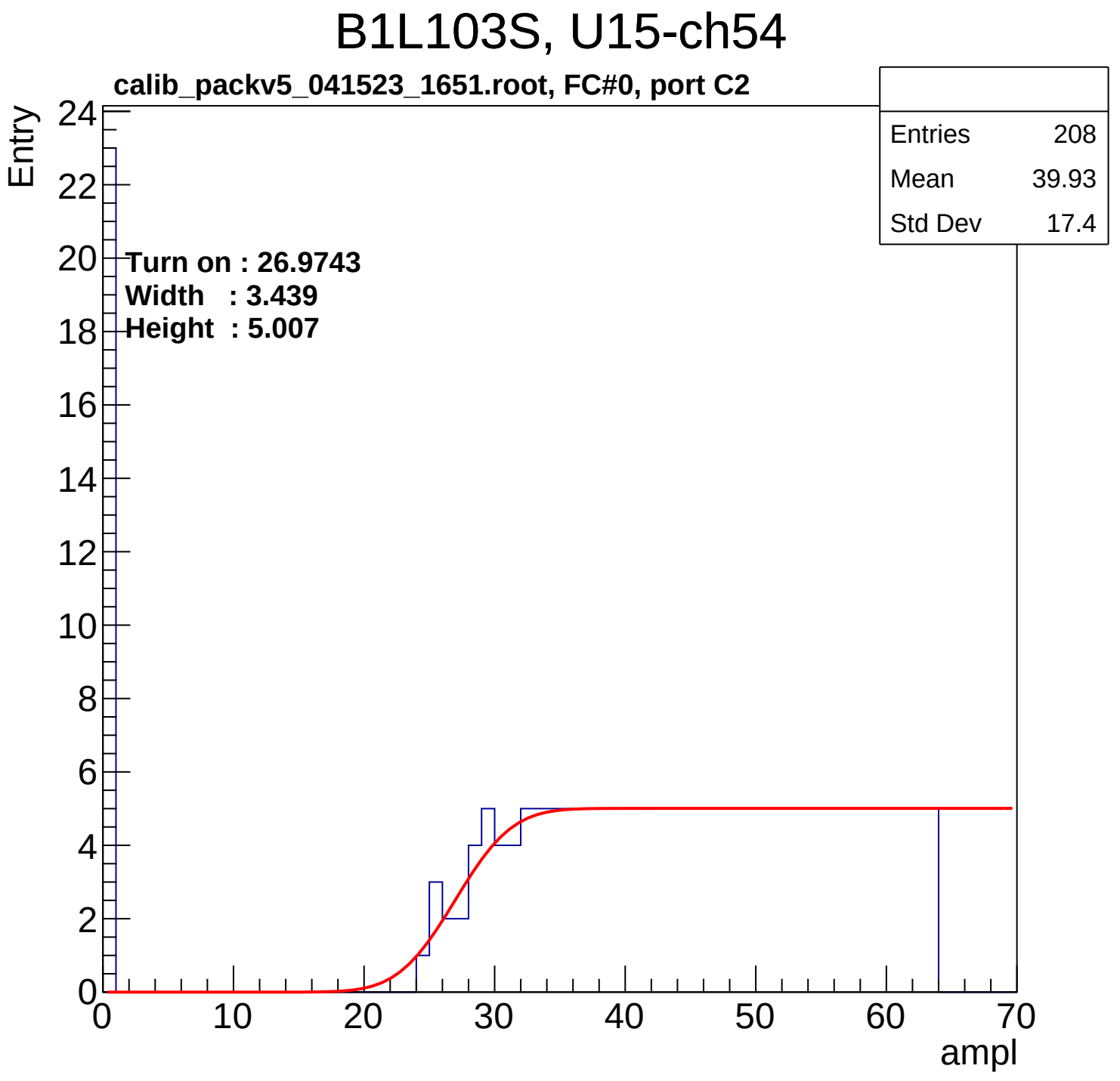
B1L103S, U15-ch54
calib_packv5_041523_1651.root, FC#0, port C2
Entries 208
Mean 39.93
Std Dev 17.4
Turn on : 26.9743
Width : 3.439
Height : 5.007
Entry
ampl
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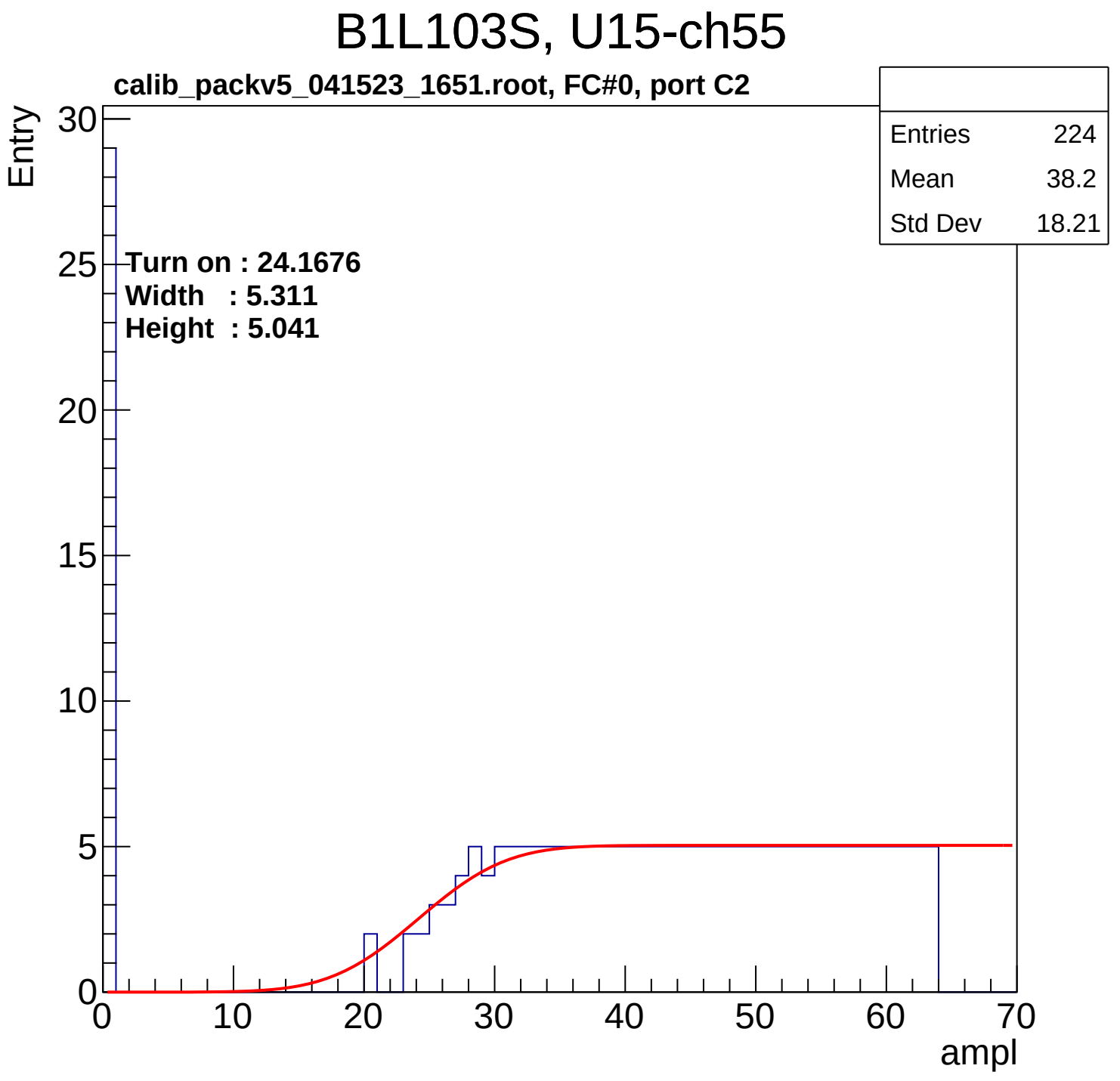
B1L103S, U15-ch55
calib_packv5_041523_1651.root, FC#0, port C2
Entries 224
Mean 38.2
Std Dev 18.21
Turn on : 24.1676
Width : 5.311
Height : 5.041
Entry
ampl
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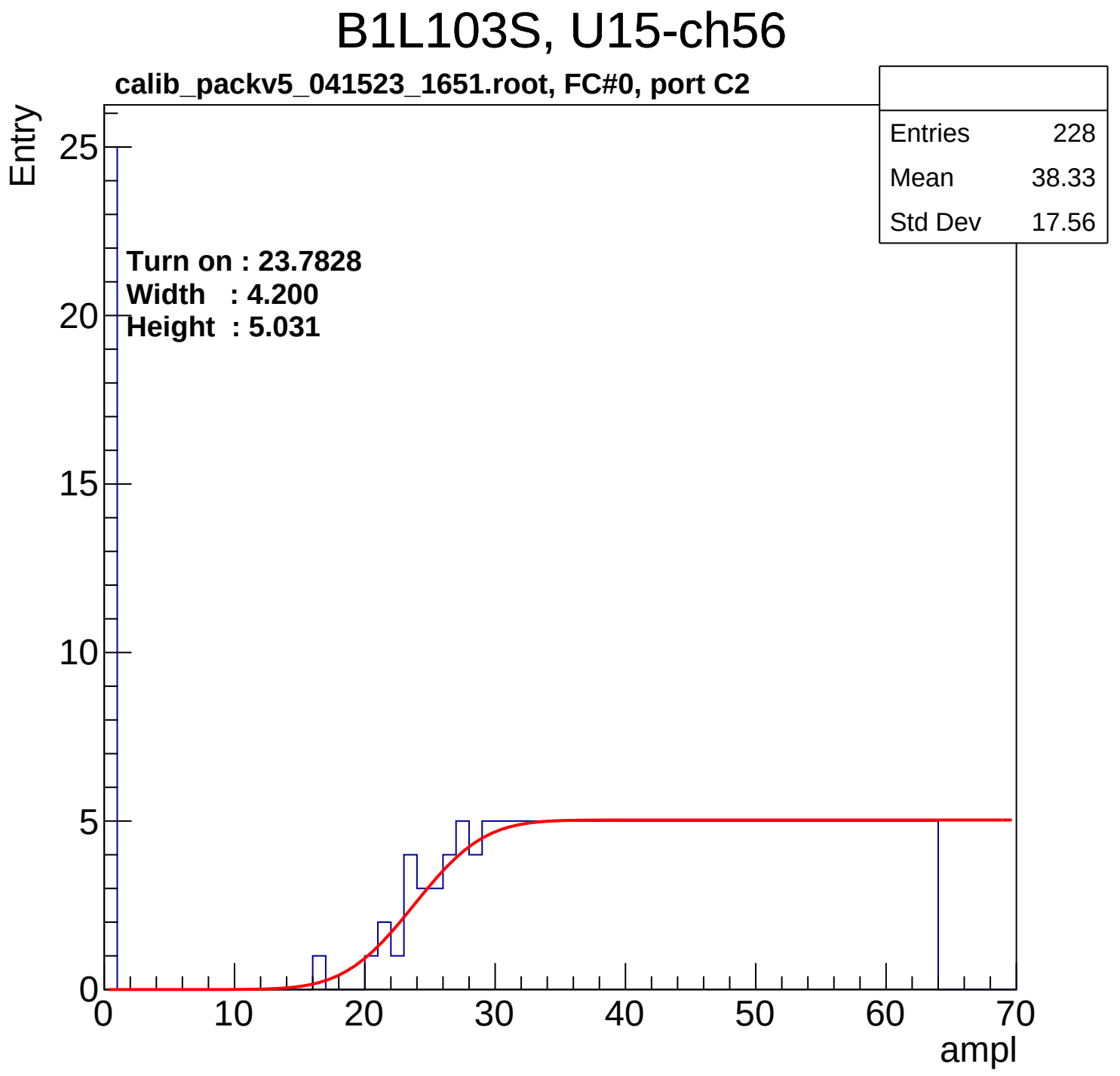
B1L103S, U15-ch56
calib_packv5_041523_1651.root, FC#0, port C2
Entries 228
Mean 38.33
Std Dev 17.56
Turn on : 23.7828
Width : 4.200
Height : 5.031
Entry
ampl
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0
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40
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60
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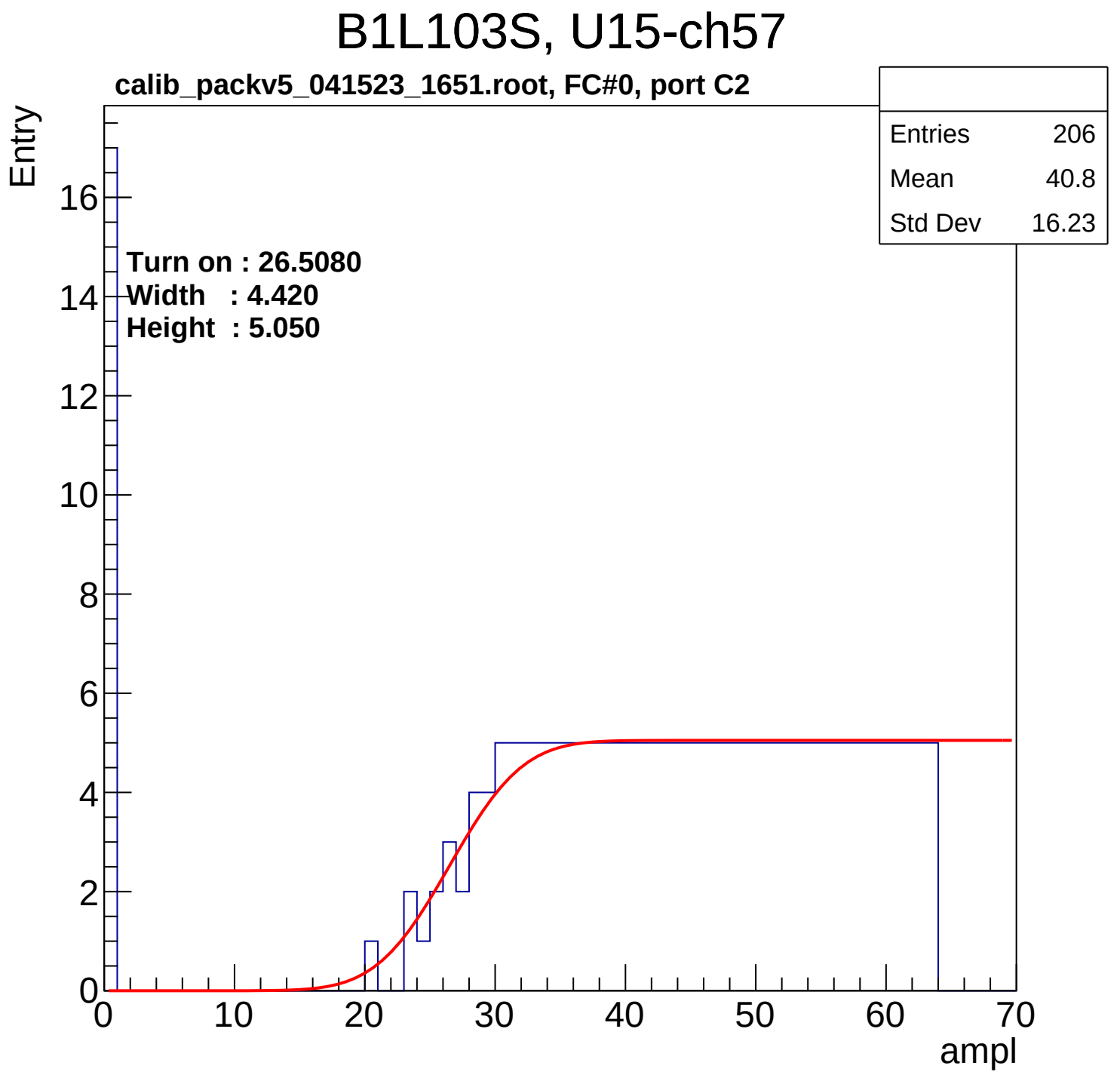
B1L103S, U15-ch57
calib_packv5_041523_1651.root, FC#0, port C2
Entries 206
Mean 40.8
Std Dev 16.23
Turn on : 26.5080
Width : 4.420
Height : 5.050
Entry
ampl
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6
8
10
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14
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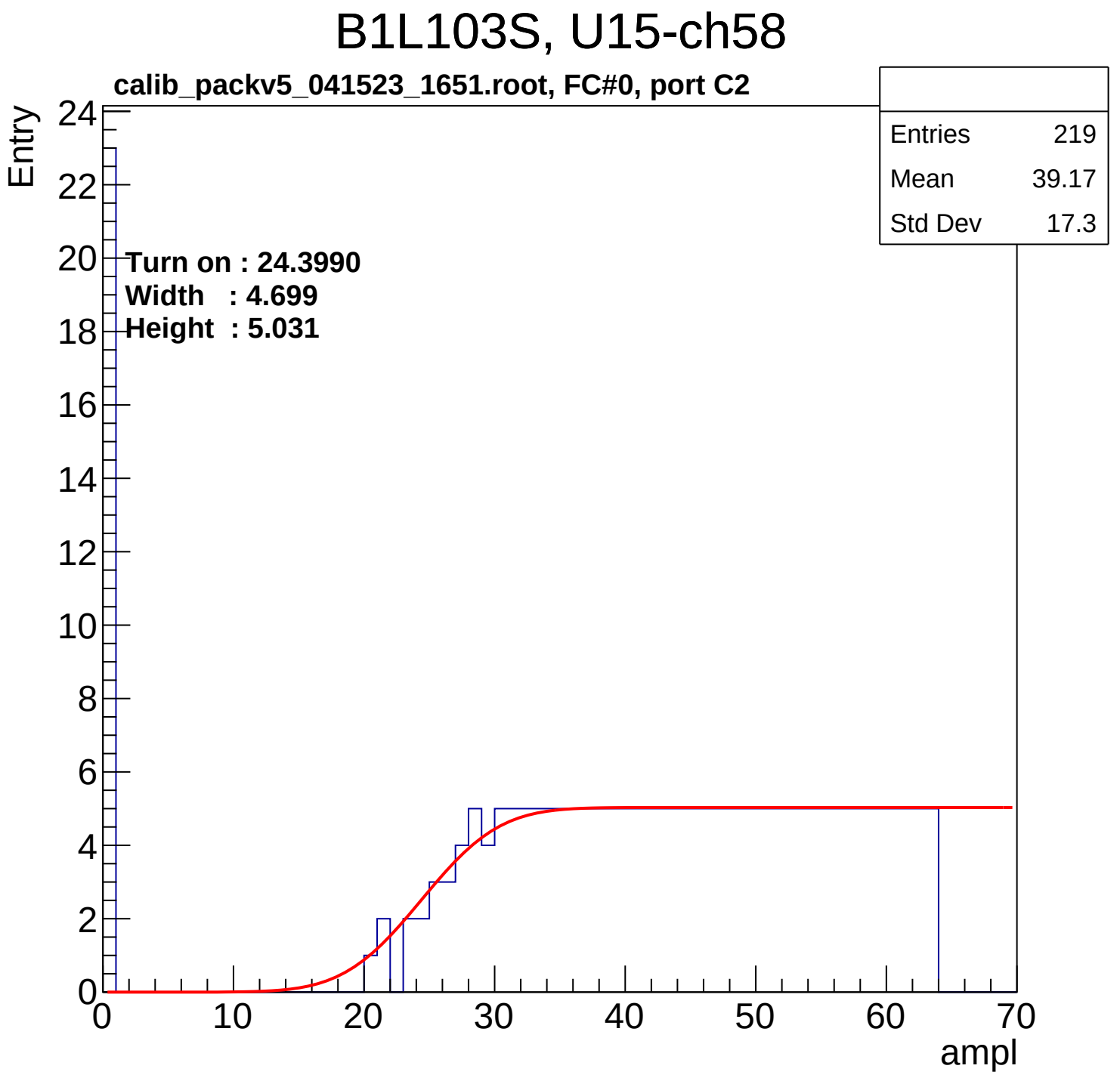
B1L103S, U15-ch58
calib_packv5_041523_1651.root, FC#0, port C2
Entries 219
Mean 39.17
Std Dev 17.3
Turn on : 24.3990
Width : 4.699
Height : 5.031
Entry
ampl
0
2
4
6
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10
12
14
16
18
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22
24
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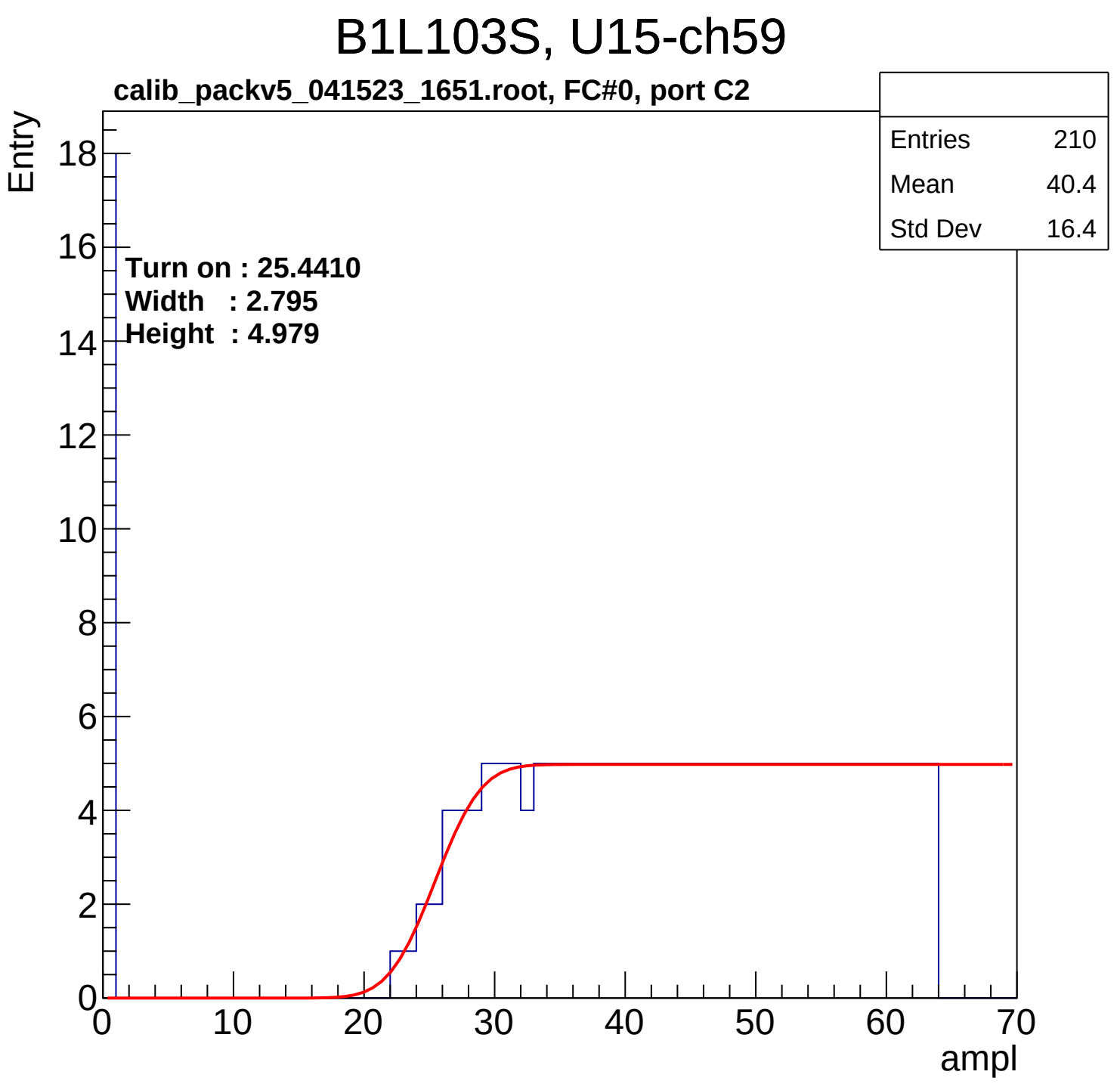
B1L103S, U15-ch59
calib_packv5_041523_1651.root, FC#0, port C2
Entries 210
Mean 40.4
Std Dev 16.4
Turn on : 25.4410
Width : 2.795
Height : 4.979
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
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30
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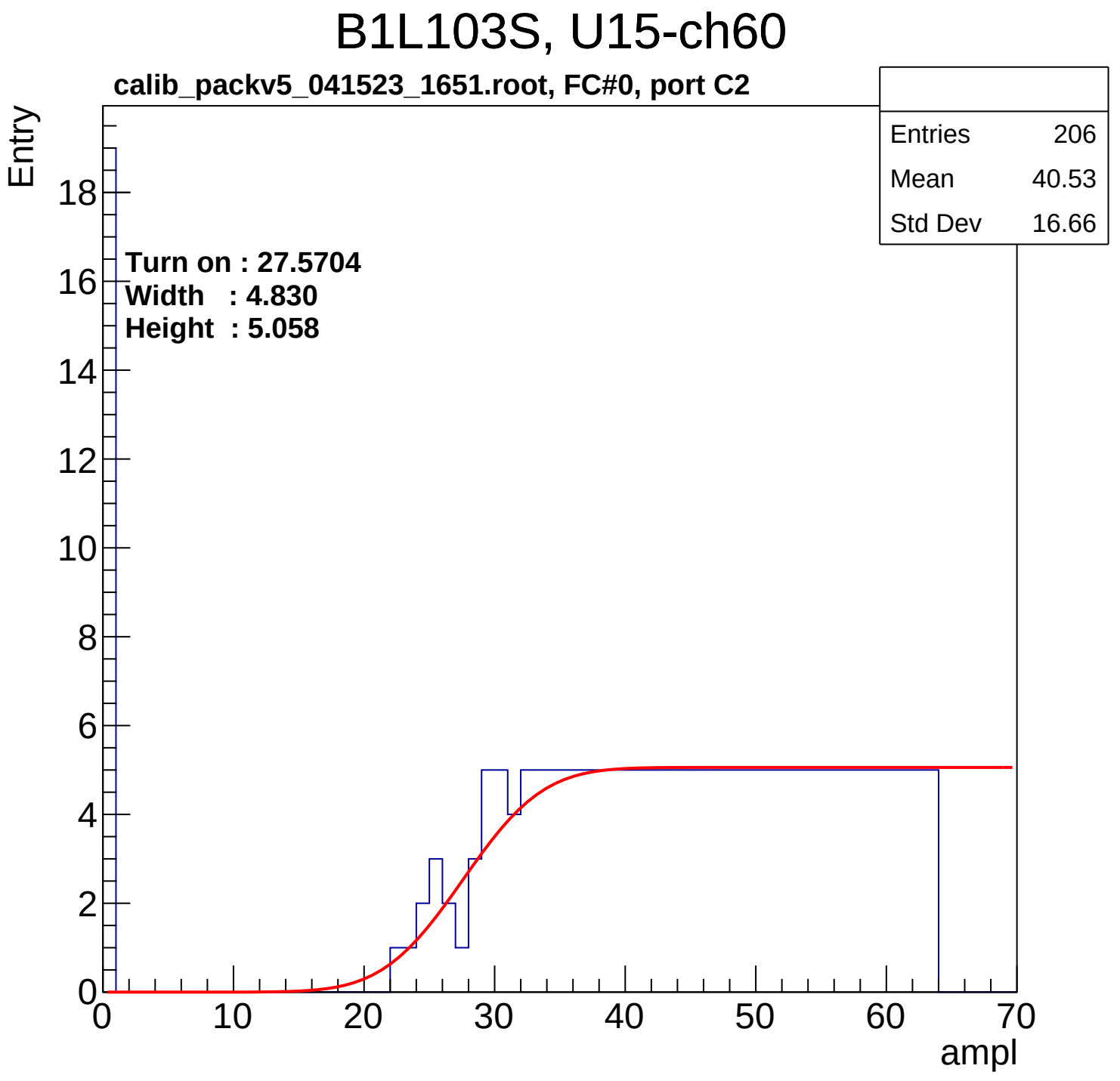
B1L103S, U15-ch60
calib_packv5_041523_1651.root, FC#0, port C2
Entries 206
Mean 40.53
Std Dev 16.66
Turn on : 27.5704
Width : 4.830
Height : 5.058
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
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20
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40
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60
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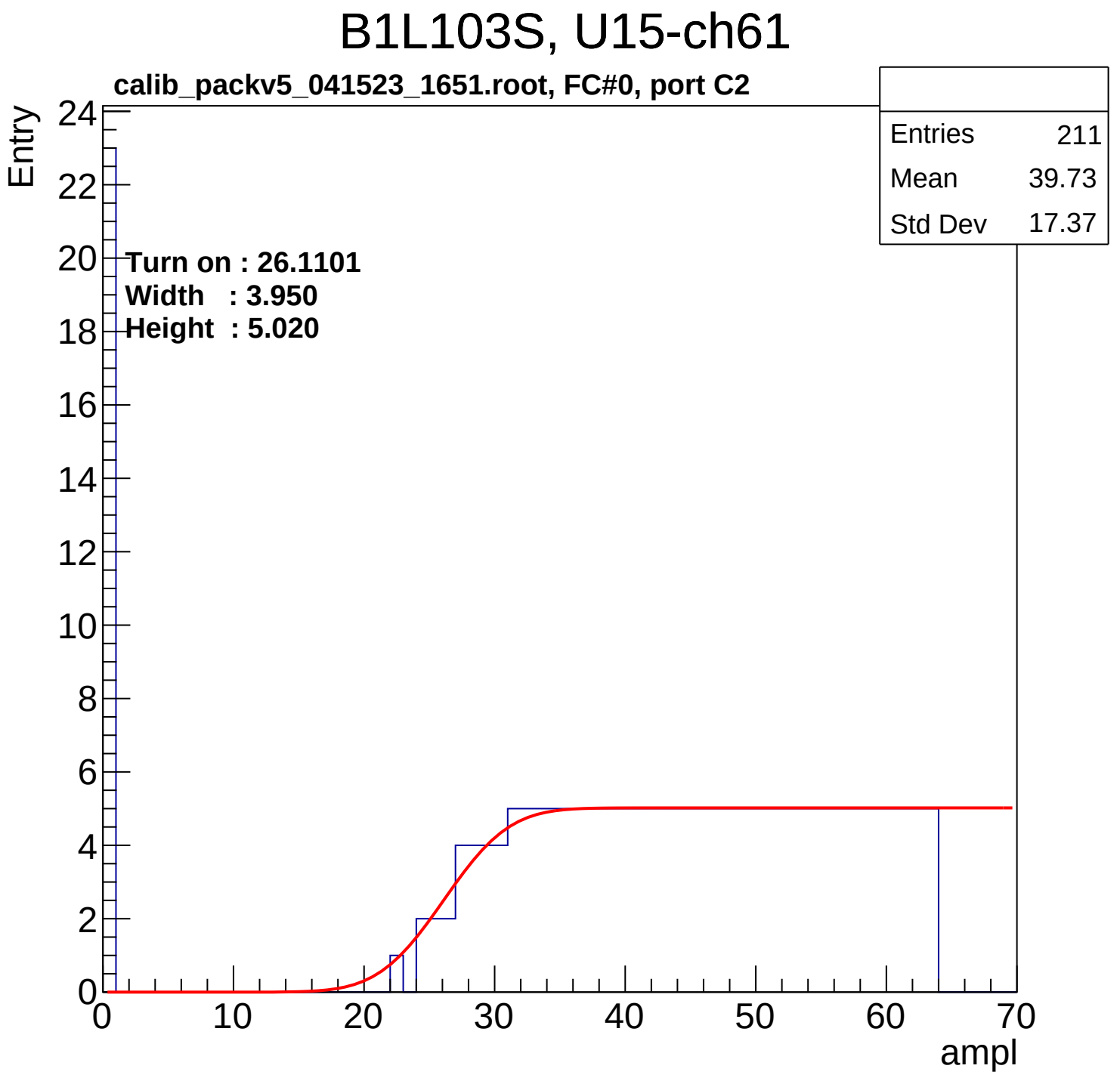
B1L103S, U15-ch61
calib_packv5_041523_1651.root, FC#0, port C2
Entries 211
Mean 39.73
Std Dev 17.37
Turn on : 26.1101
Width : 3.950
Height : 5.020
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
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60
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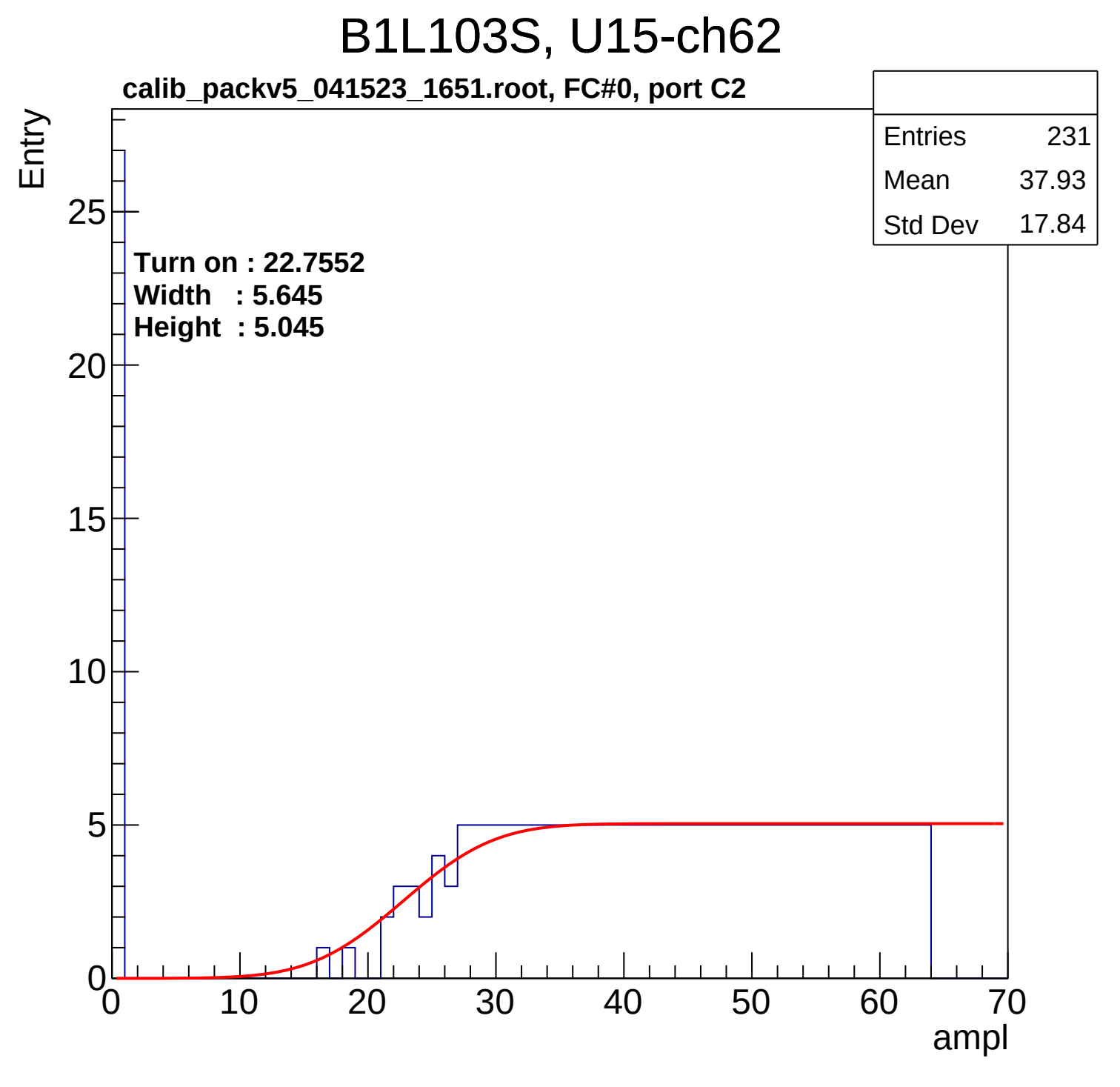
B1L103S, U15-ch62
calib_packv5_041523_1651.root, FC#0, port C2
Entries 231
Mean 37.93
Std Dev 17.84
Turn on : 22.7552
Width : 5.645
Height : 5.045
Entry
ampl
0
5
10
15
20
25
0
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40
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60
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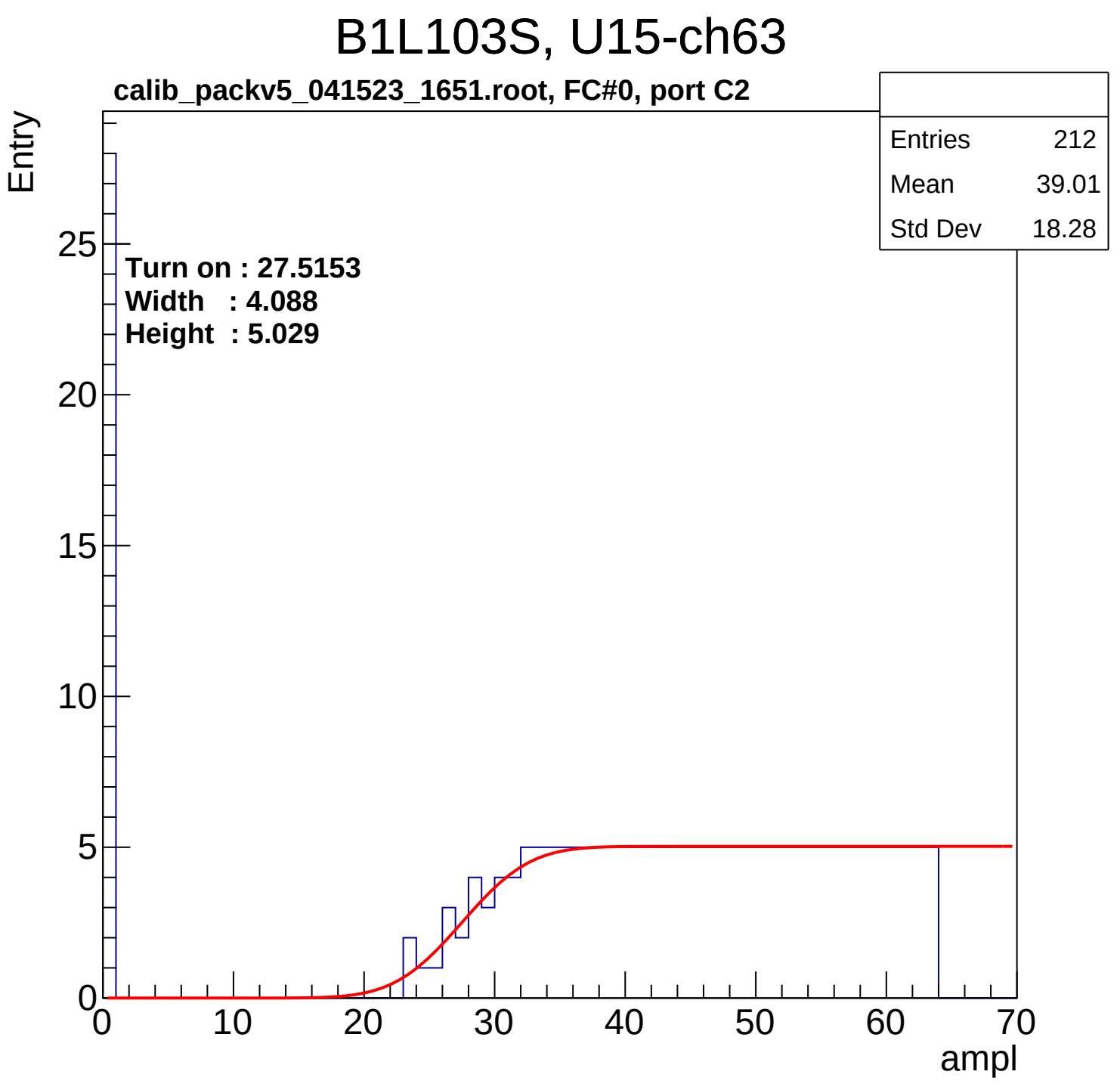
B1L103S, U15-ch63
calib_packv5_041523_1651.root, FC#0, port C2
Entries 212
Mean 39.01
Std Dev 18.28
Turn on : 27.5153
Width : 4.088
Height : 5.029
Entry
ampl
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5
10
15
20
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0
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20
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40
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60
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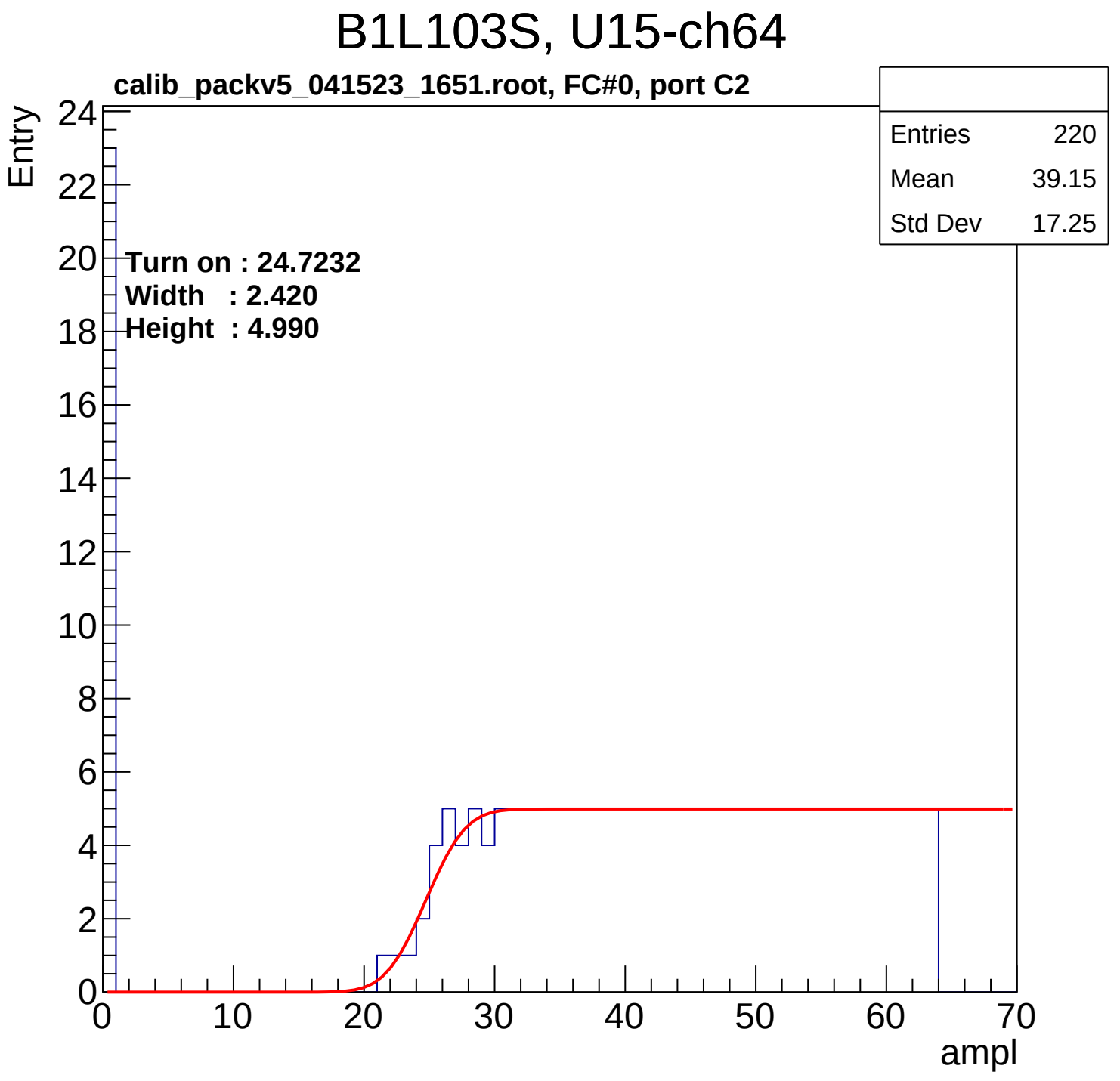
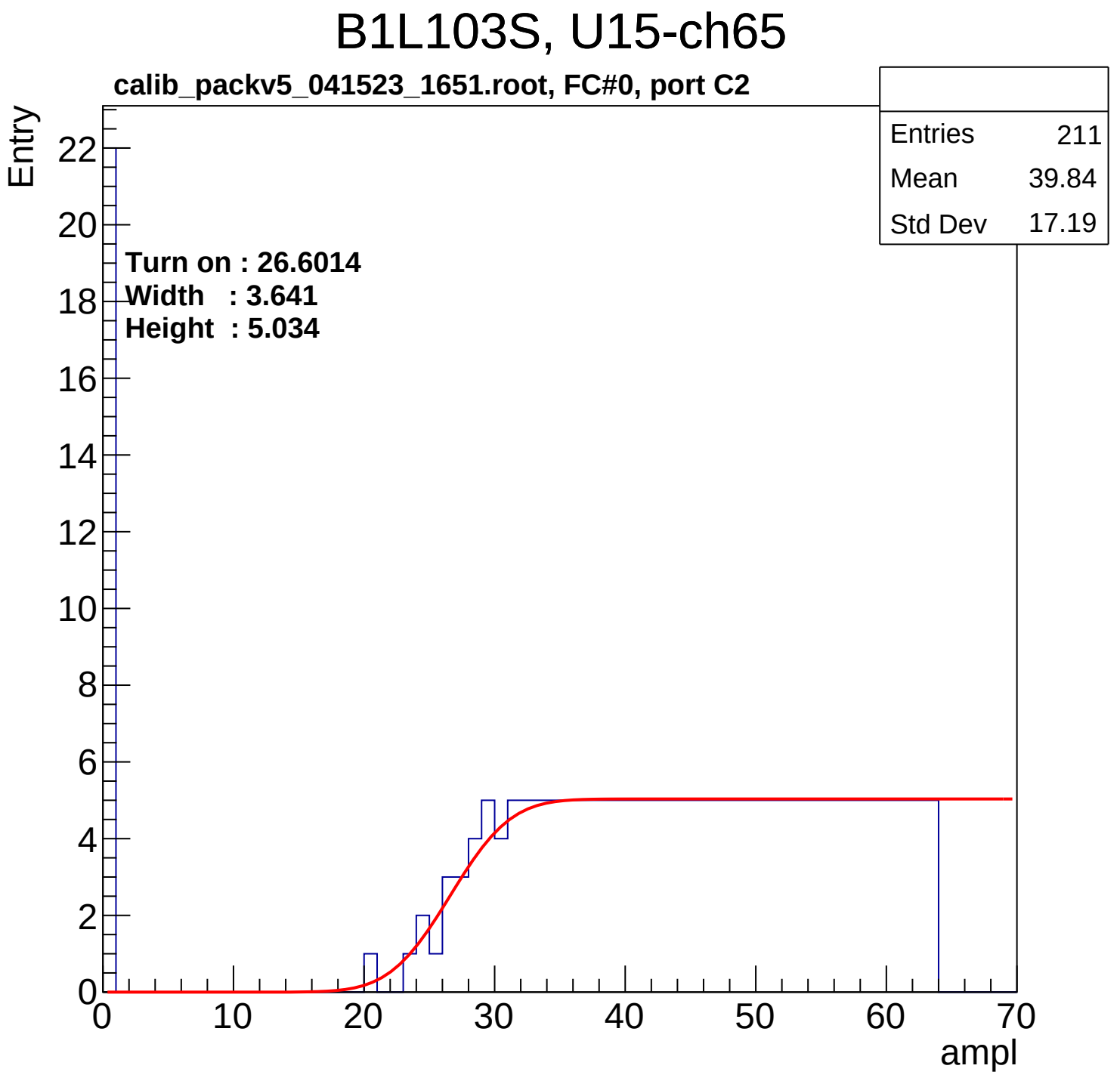

B1L103S, U15-ch64
calib_packv5_041523_1651.root, FC#0, port C2
Entries 220
Mean 39.15
Std Dev 17.25
Turn on : 24.7232
Width : 2.420
Height : 4.990
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70


B1L103S, U15-ch65
calib_packv5_041523_1651.root, FC#0, port C2
Entries 211
Mean 39.84
Std Dev 17.19
Turn on : 26.6014
Width : 3.641
Height : 5.034
Entry
ampl
0
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6
8
10
12
14
16
18
20
22
0
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20
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40
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60
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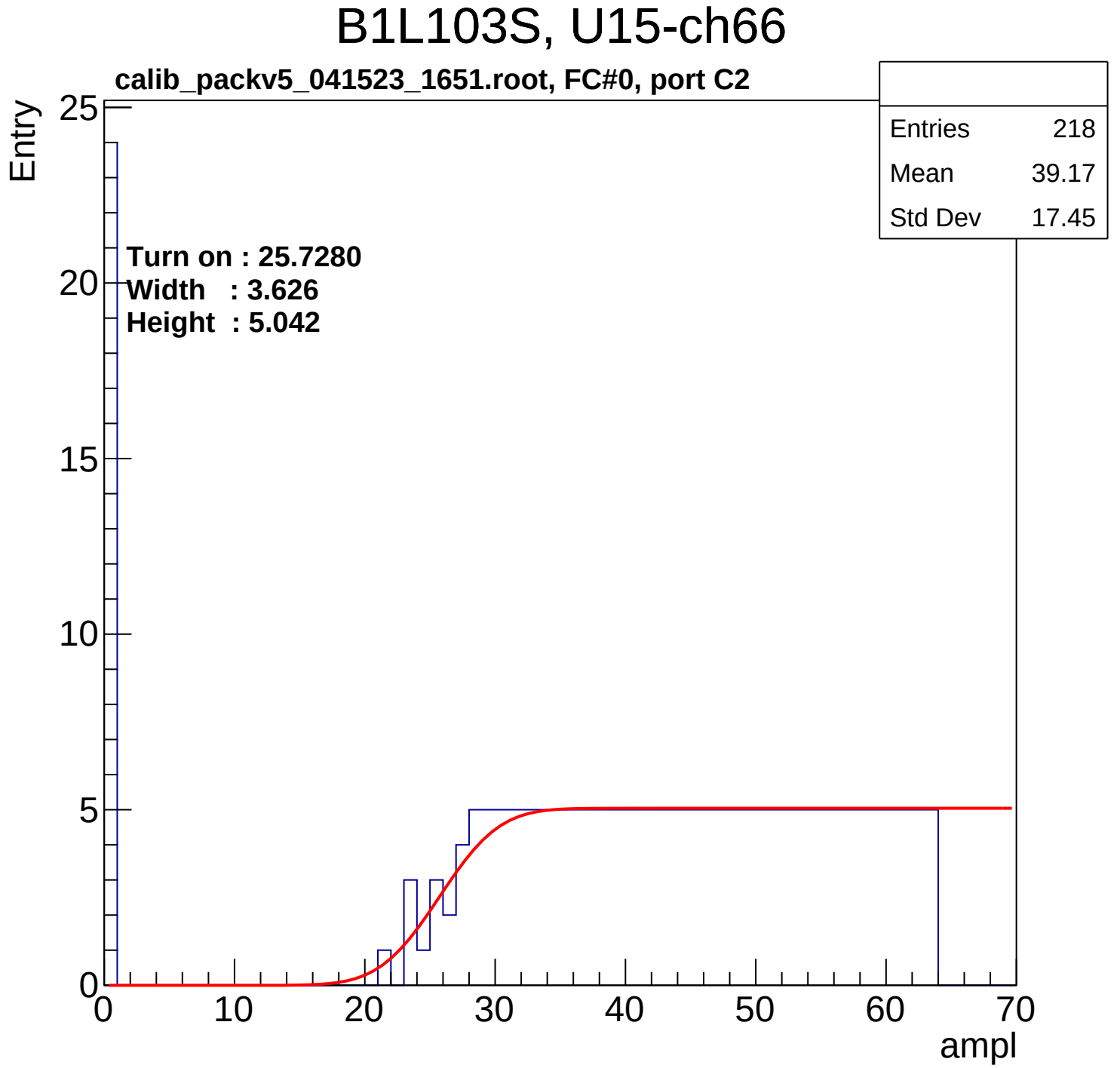
B1L103S, U15-ch66
calib_packv5_041523_1651.root, FC#0, port C2
Entries 218
Mean 39.17
Std Dev 17.45
Turn on : 25.7280
Width : 3.626
Height : 5.042
Entry
ampl
0
5
10
15
20
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0
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20
30
40
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60
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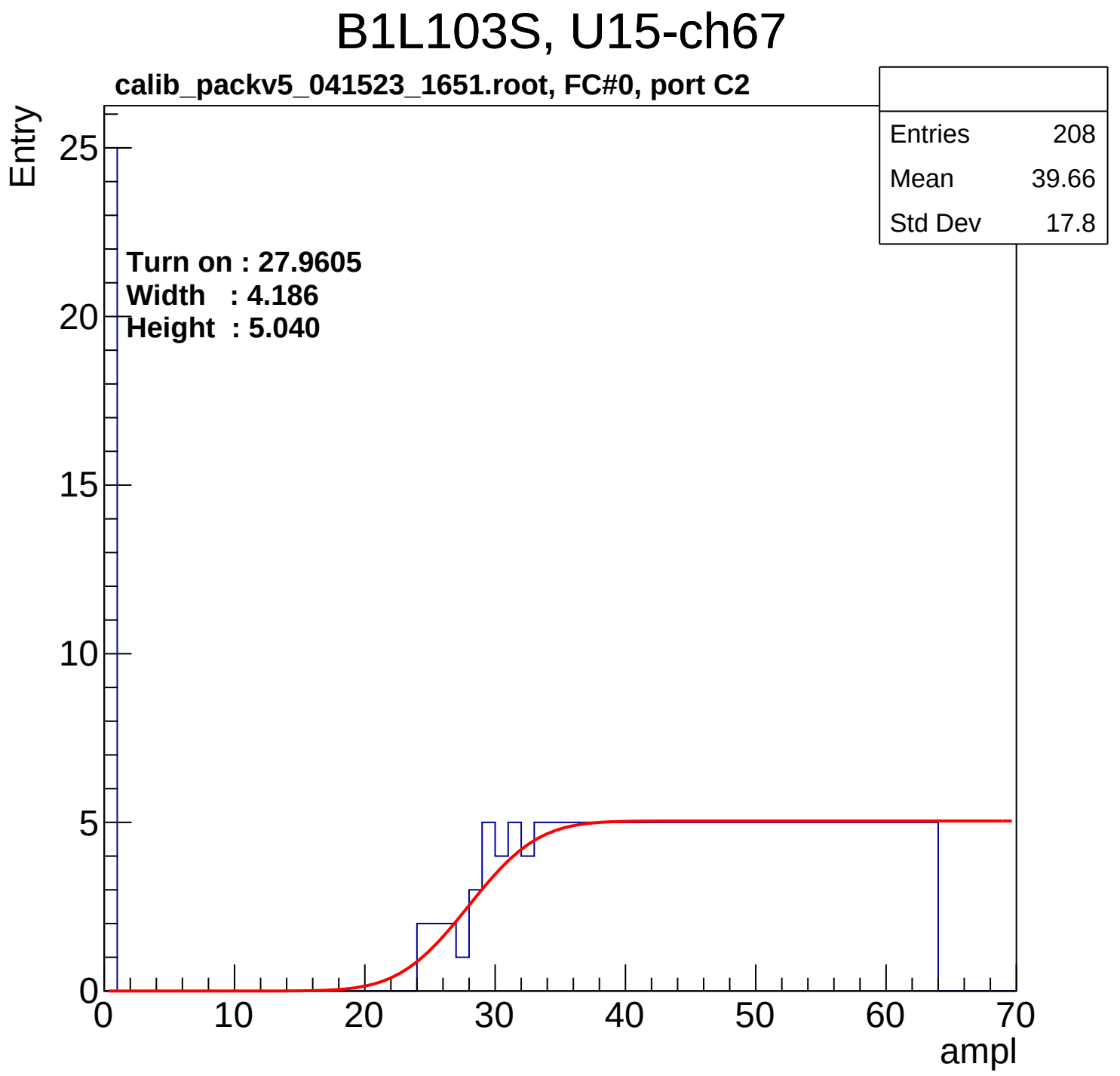
B1L103S, U15-ch67
calib_packv5_041523_1651.root, FC#0, port C2
Entries 208
Mean 39.66
Std Dev 17.8
Turn on : 27.9605
Width : 4.186
Height : 5.040
Entry
ampl
0
5
10
15
20
25
0
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20
30
40
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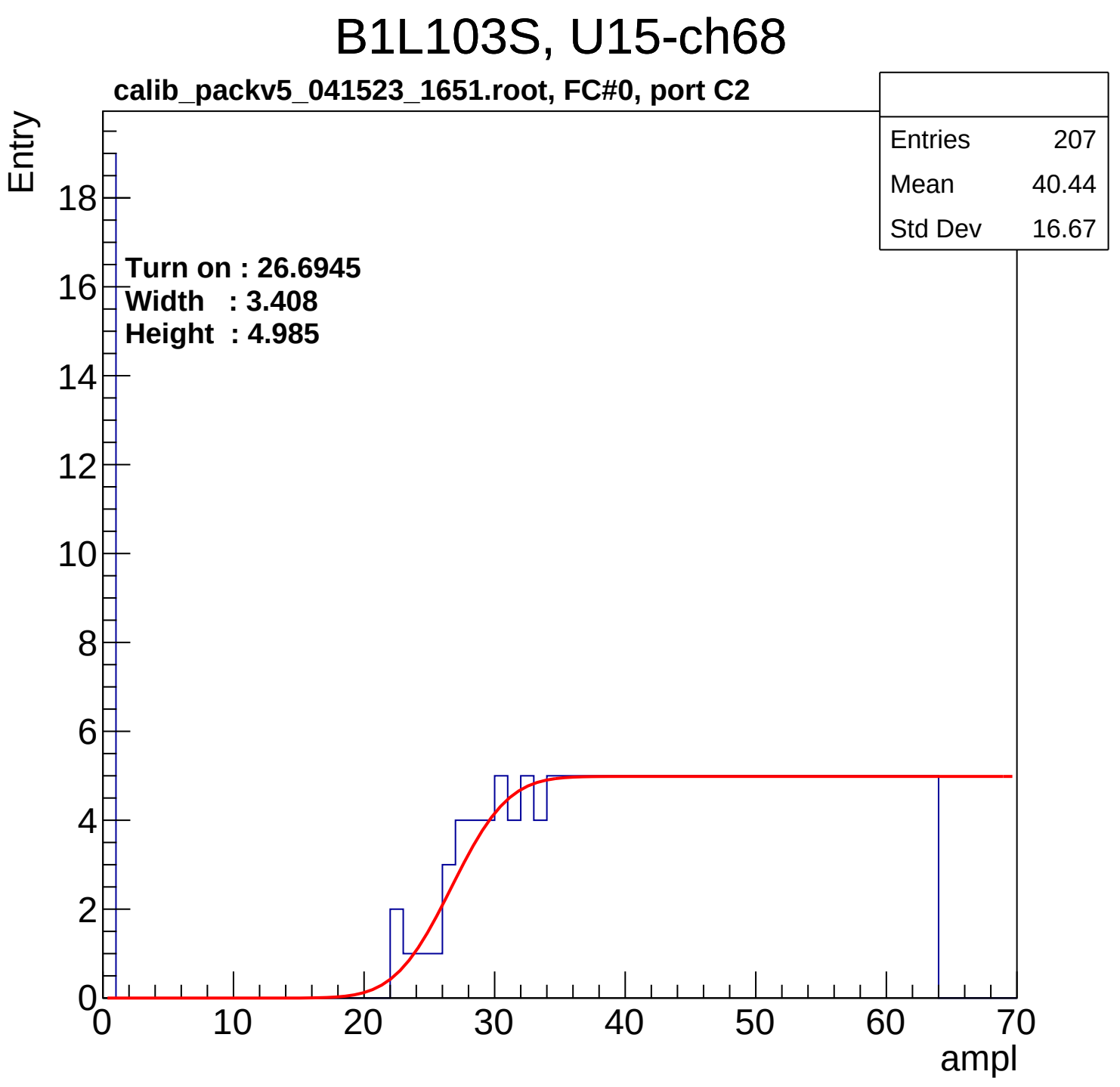
B1L103S, U15-ch68
calib_packv5_041523_1651.root, FC#0, port C2
Entries 207
Mean 40.44
Std Dev 16.67
Turn on : 26.6945
Width : 3.408
Height : 4.985
Entry
ampl
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4
6
8
10
12
14
16
18
0
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20
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60
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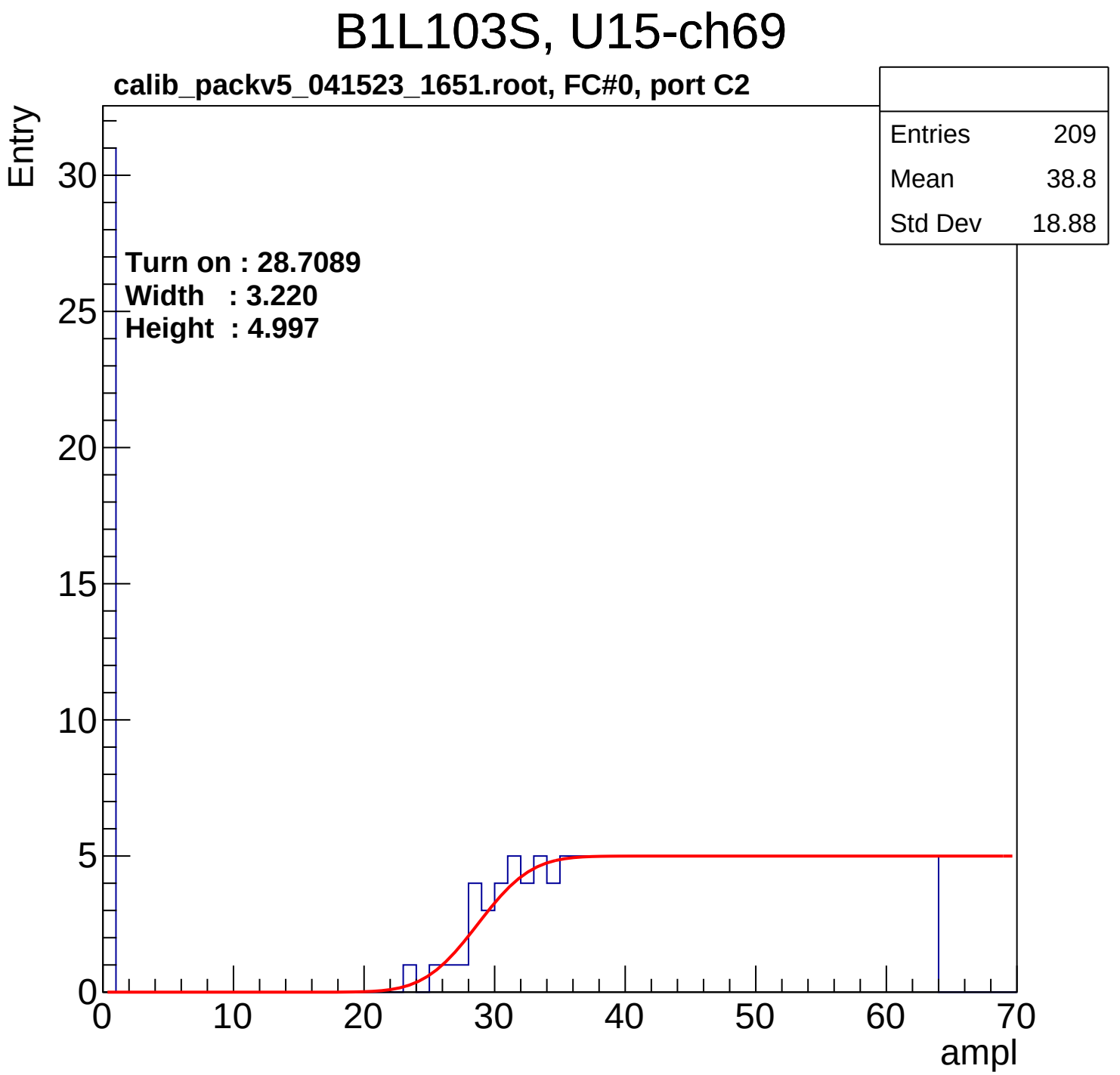
B1L103S, U15-ch69
calib_packv5_041523_1651.root, FC#0, port C2
Entries 209
Mean 38.8
Std Dev 18.88
Turn on : 28.7089
Width : 3.220
Height : 4.997
Entry
ampl
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5
10
15
20
25
30
0
10
20
30
40
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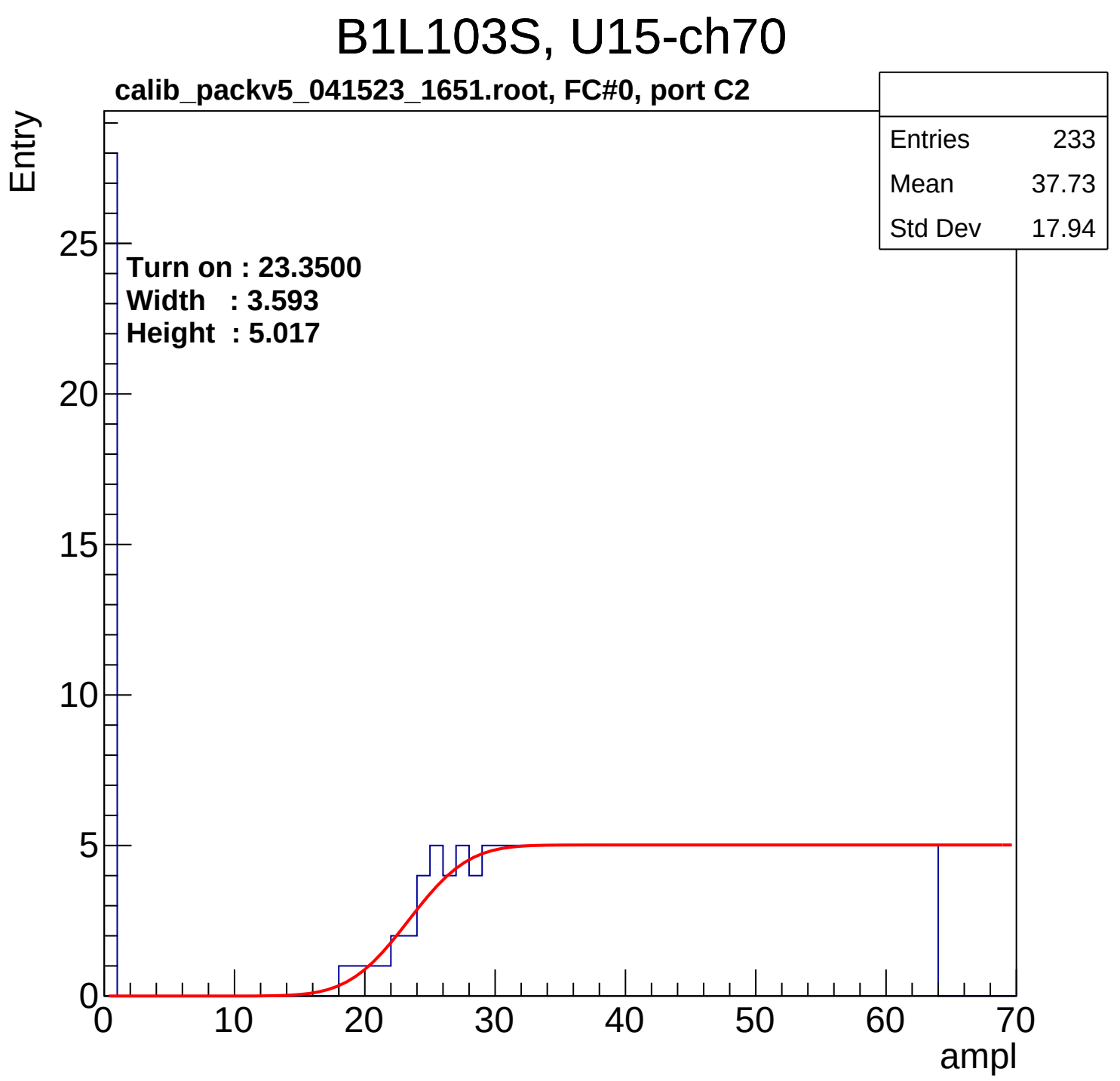
B1L103S, U15-ch70
calib_packv5_041523_1651.root, FC#0, port C2
Entries 233
Mean 37.73
Std Dev 17.94
Turn on : 23.3500
Width : 3.593
Height : 5.017
Entry
ampl
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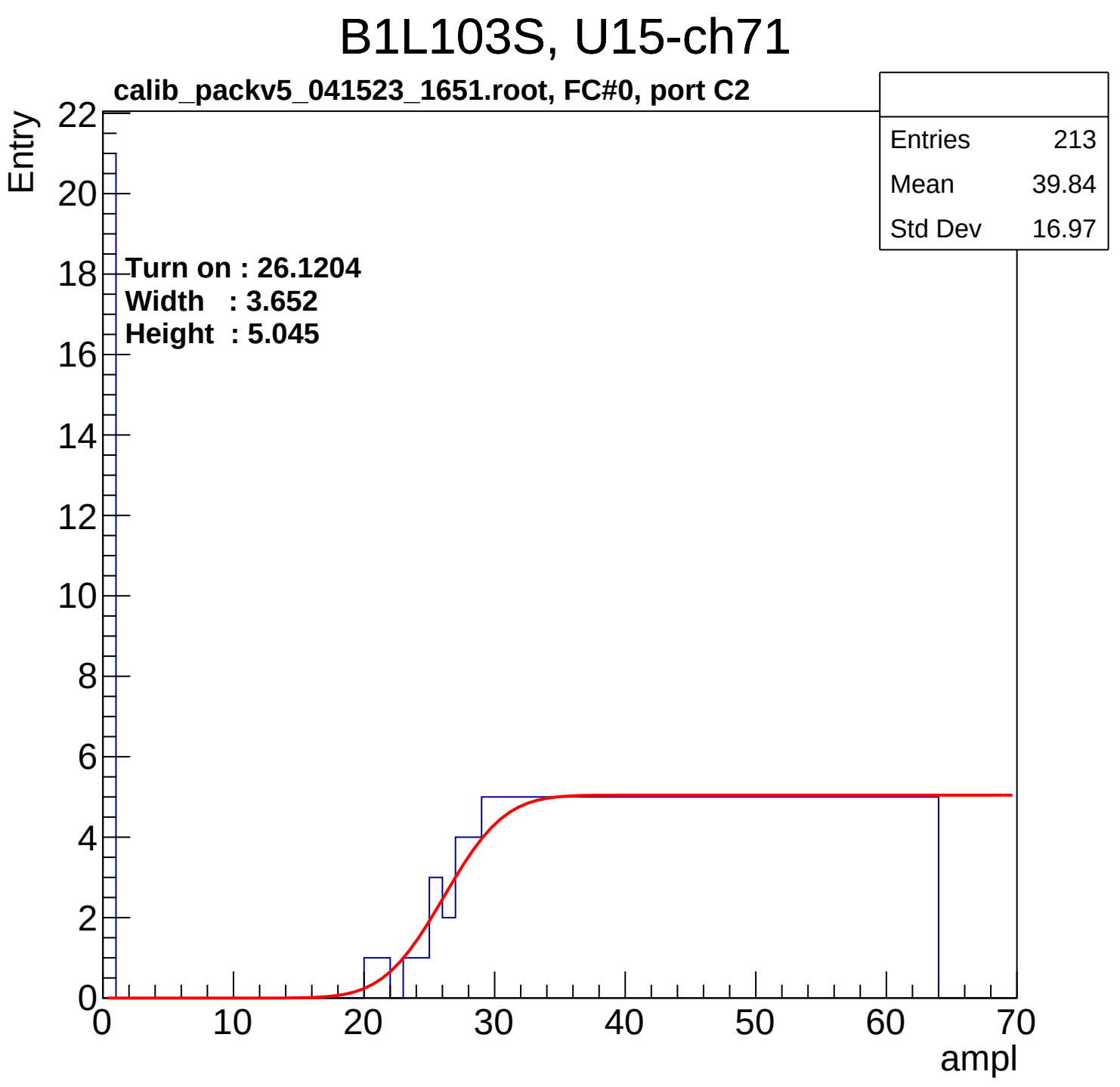
B1L103S, U15-ch71
calib_packv5_041523_1651.root, FC#0, port C2
Entries 213
Mean 39.84
Std Dev 16.97
Turn on : 26.1204
Width : 3.652
Height : 5.045
Entry
ampl
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8
10
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16
18
20
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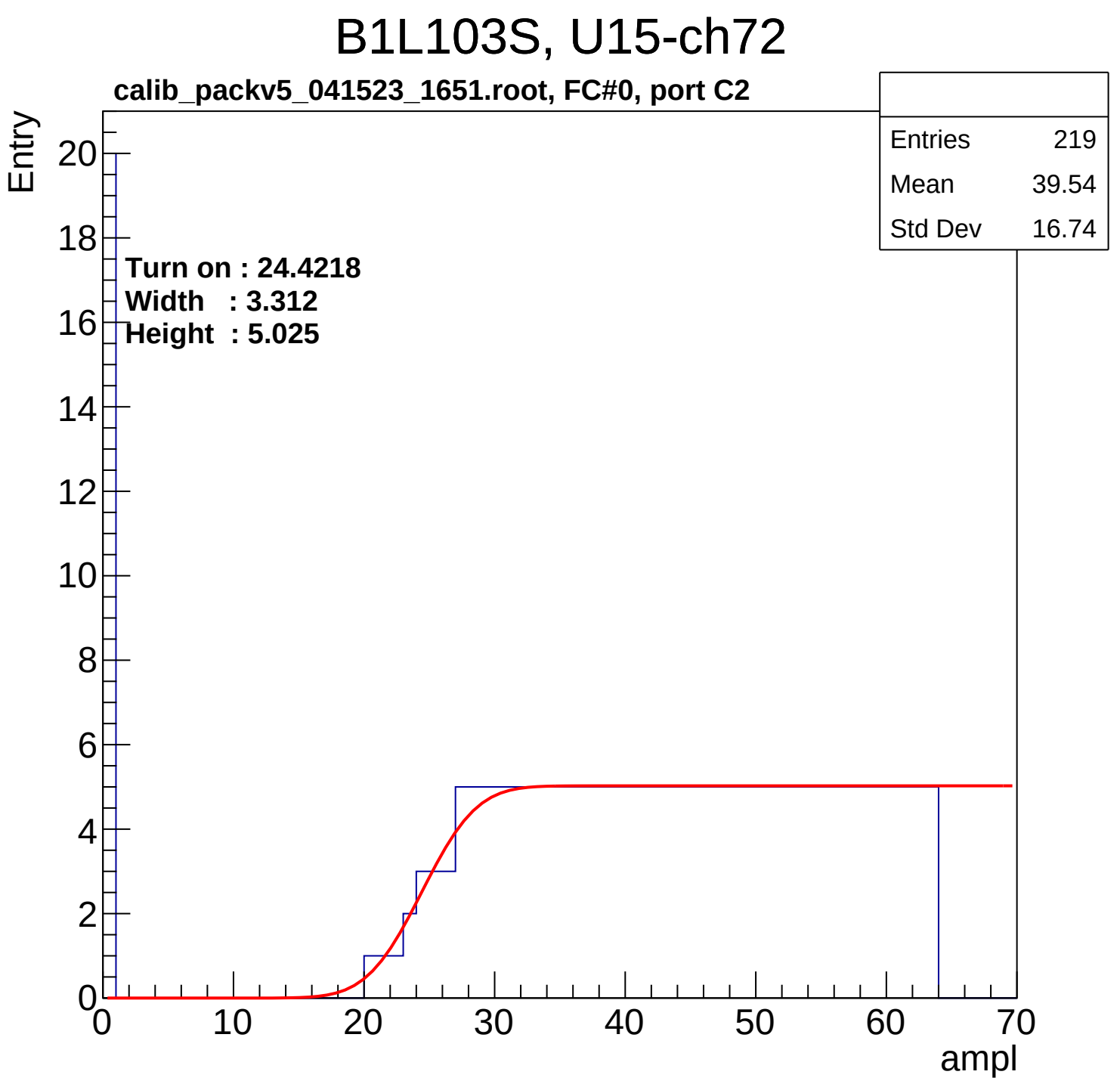
B1L103S, U15-ch72
calib_packv5_041523_1651.root, FC#0, port C2
Entries 219
Mean 39.54
Std Dev 16.74
Turn on : 24.4218
Width : 3.312
Height : 5.025
Entry
ampl
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6
8
10
12
14
16
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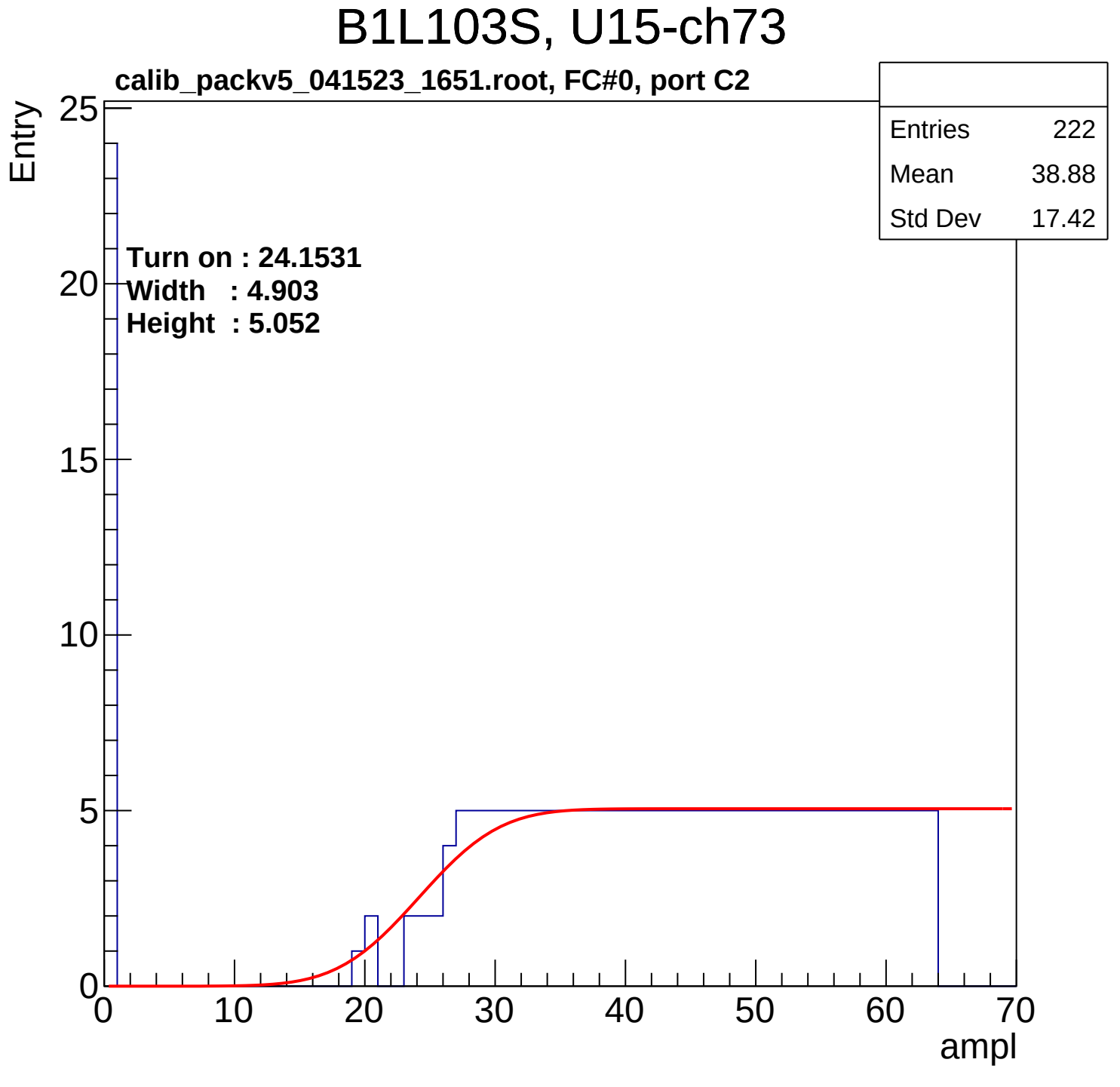
B1L103S, U15-ch73
calib_packv5_041523_1651.root, FC#0, port C2
Entries 222
Mean 38.88
Std Dev 17.42
Turn on : 24.1531
Width : 4.903
Height : 5.052
Entry
ampl
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5
10
15
20
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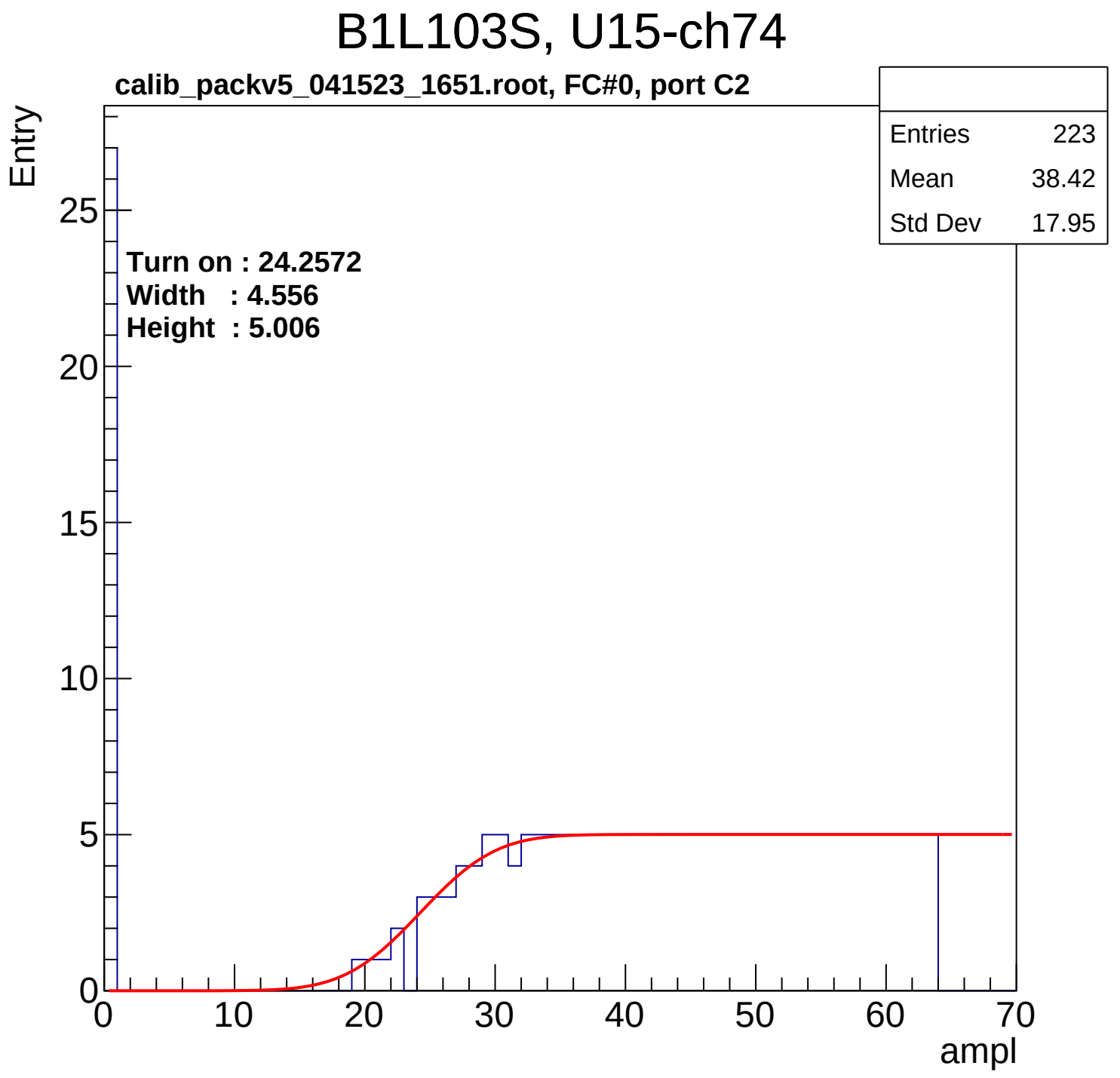
B1L103S, U15-ch74
calib_packv5_041523_1651.root, FC#0, port C2
Entries 223
Mean 38.42
Std Dev 17.95
Turn on : 24.2572
Width : 4.556
Height : 5.006
Entry
ampl
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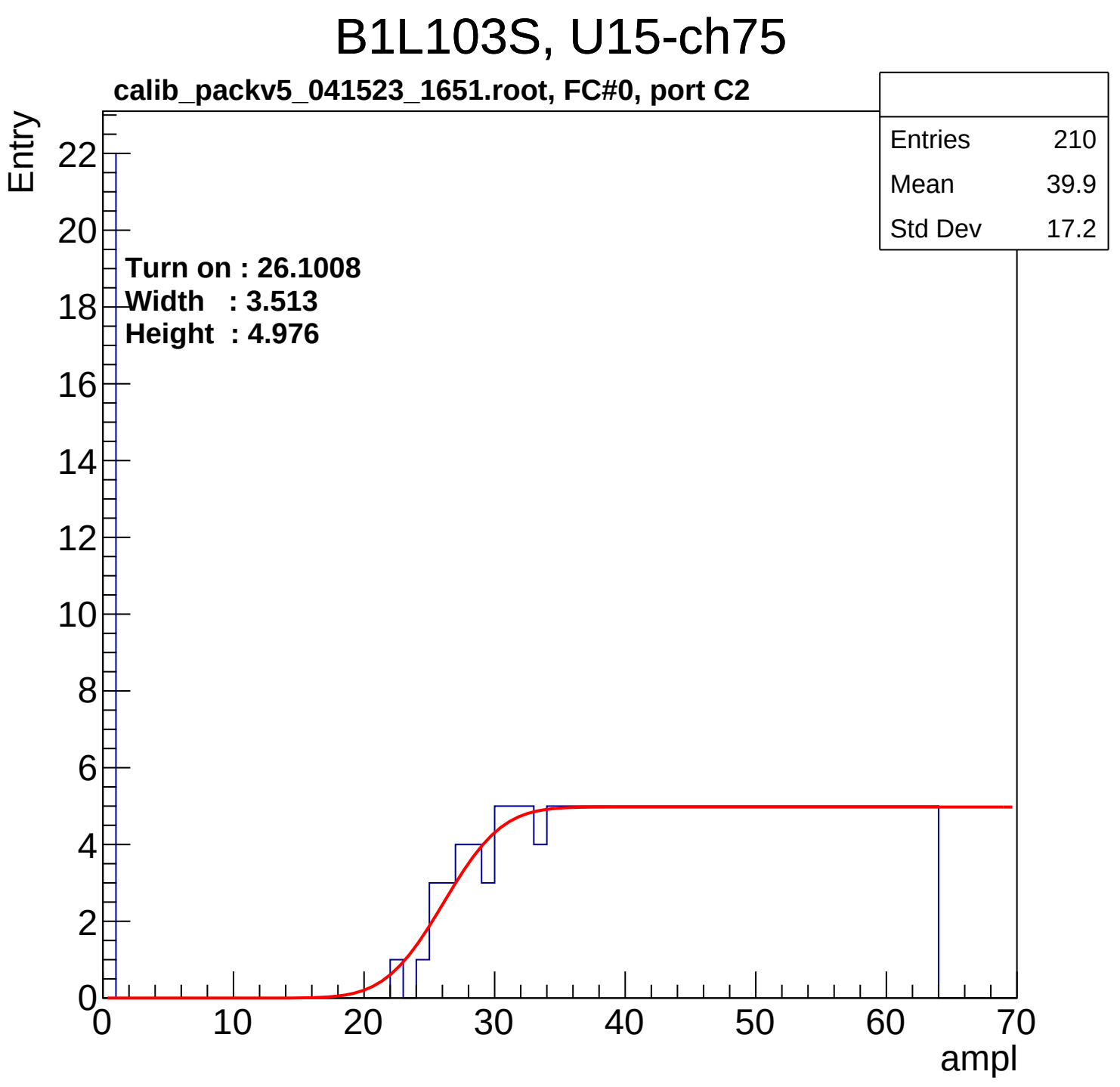
B1L103S, U15-ch75
calib_packv5_041523_1651.root, FC#0, port C2
Entries 210
Mean 39.9
Std Dev 17.2
Turn on : 26.1008
Width : 3.513
Height : 4.976
Entry
ampl
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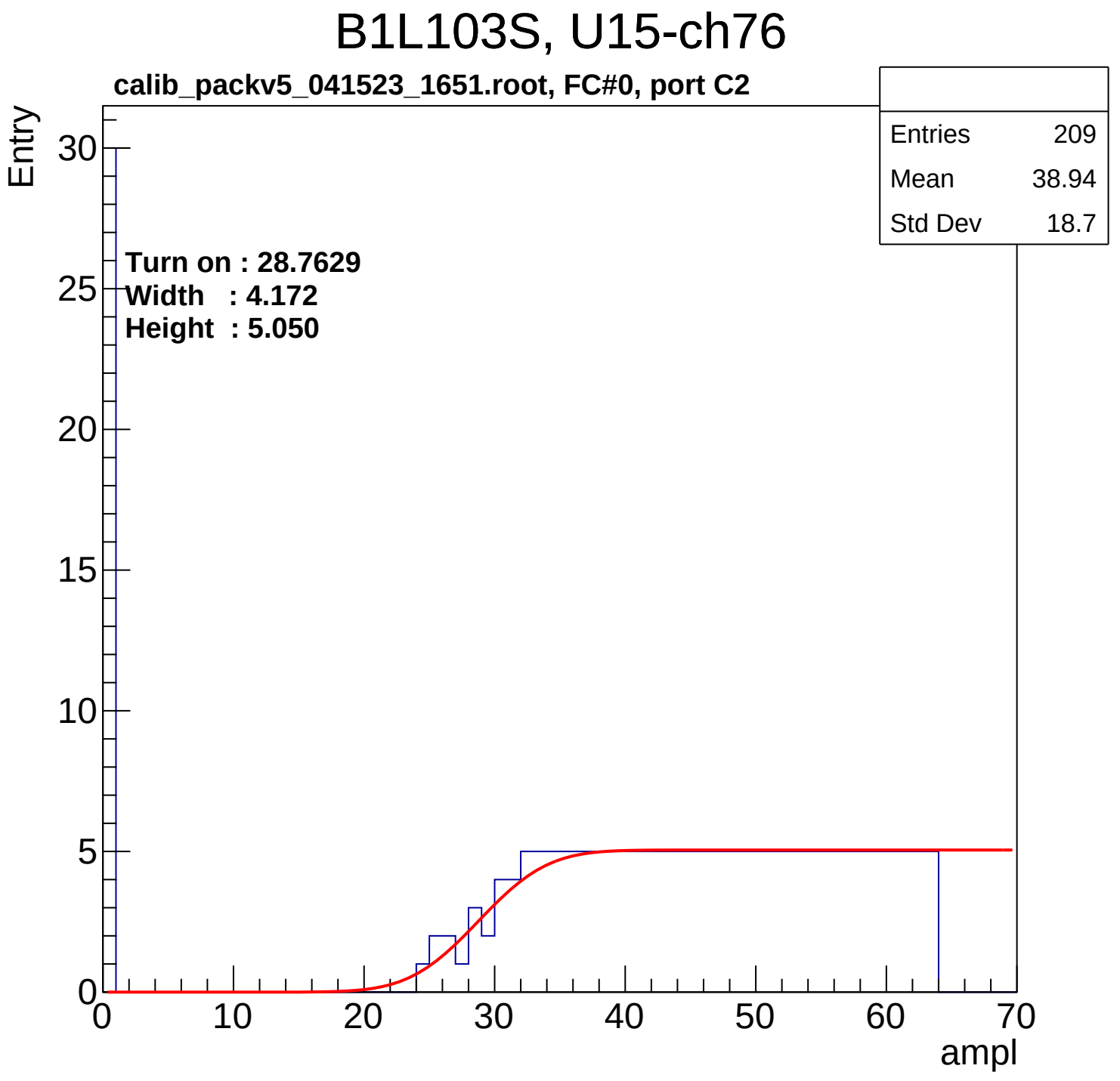
B1L103S, U15-ch76
calib_packv5_041523_1651.root, FC#0, port C2
Entries 209
Mean 38.94
Std Dev 18.7
Turn on : 28.7629
Width : 4.172
Height : 5.050
Entry
ampl
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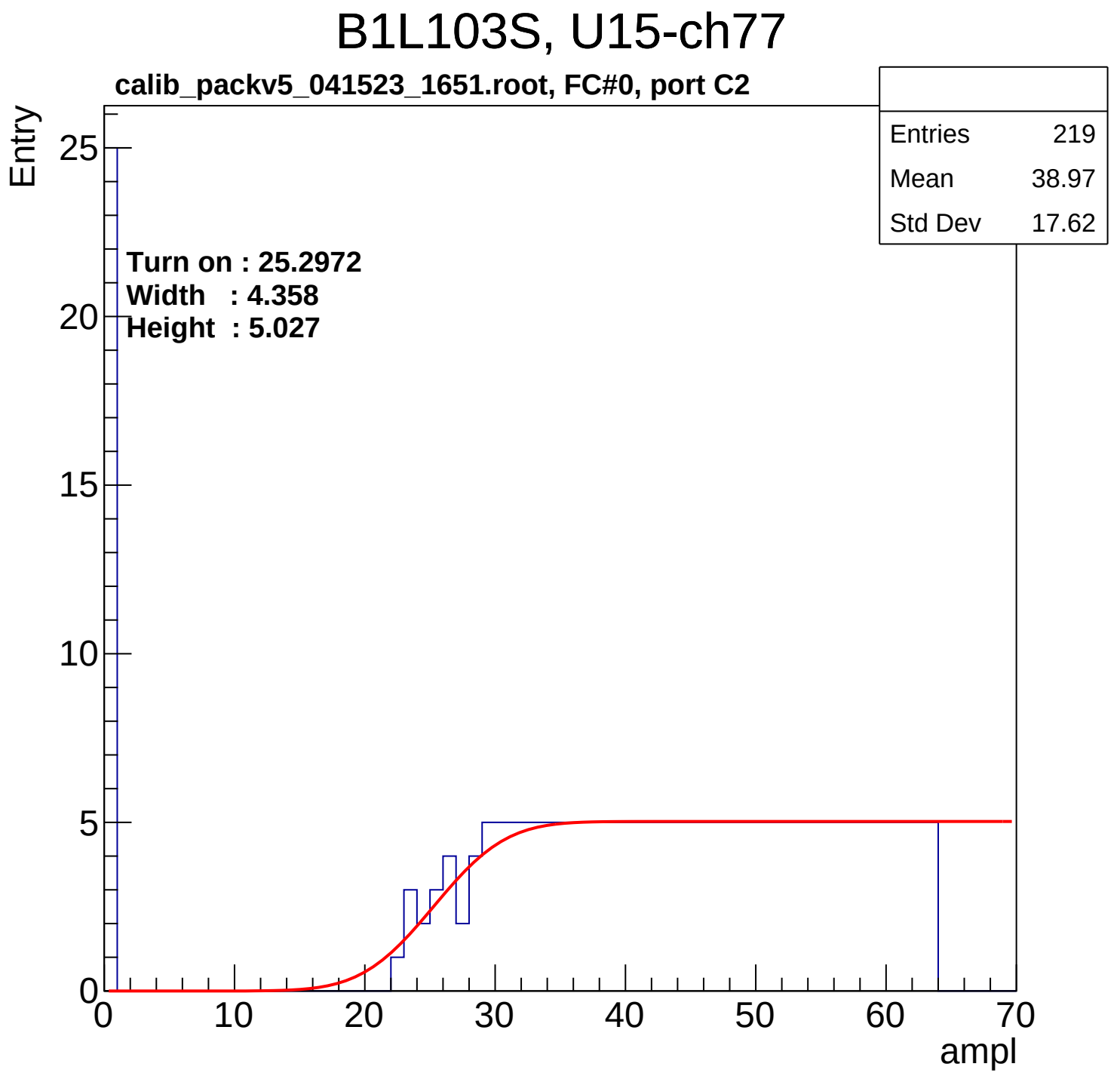
B1L103S, U15-ch77
calib_packv5_041523_1651.root, FC#0, port C2
Entries 219
Mean 38.97
Std Dev 17.62
Turn on : 25.2972
Width : 4.358
Height : 5.027
Entry
ampl
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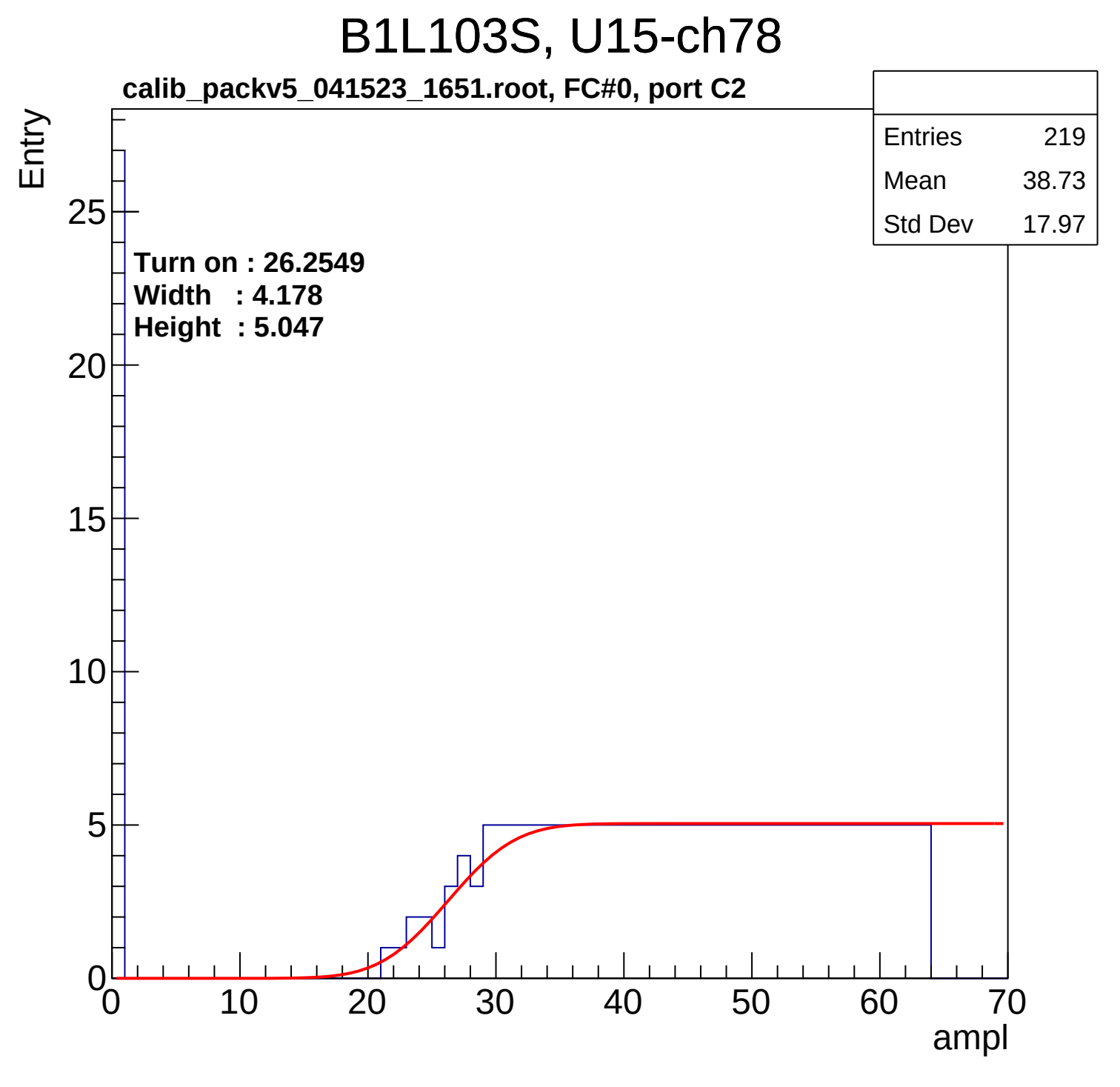
B1L103S, U15-ch78
calib_packv5_041523_1651.root, FC#0, port C2
Entries 219
Mean 38.73
Std Dev 17.97
Turn on : 26.2549
Width : 4.178
Height : 5.047
Entry
ampl
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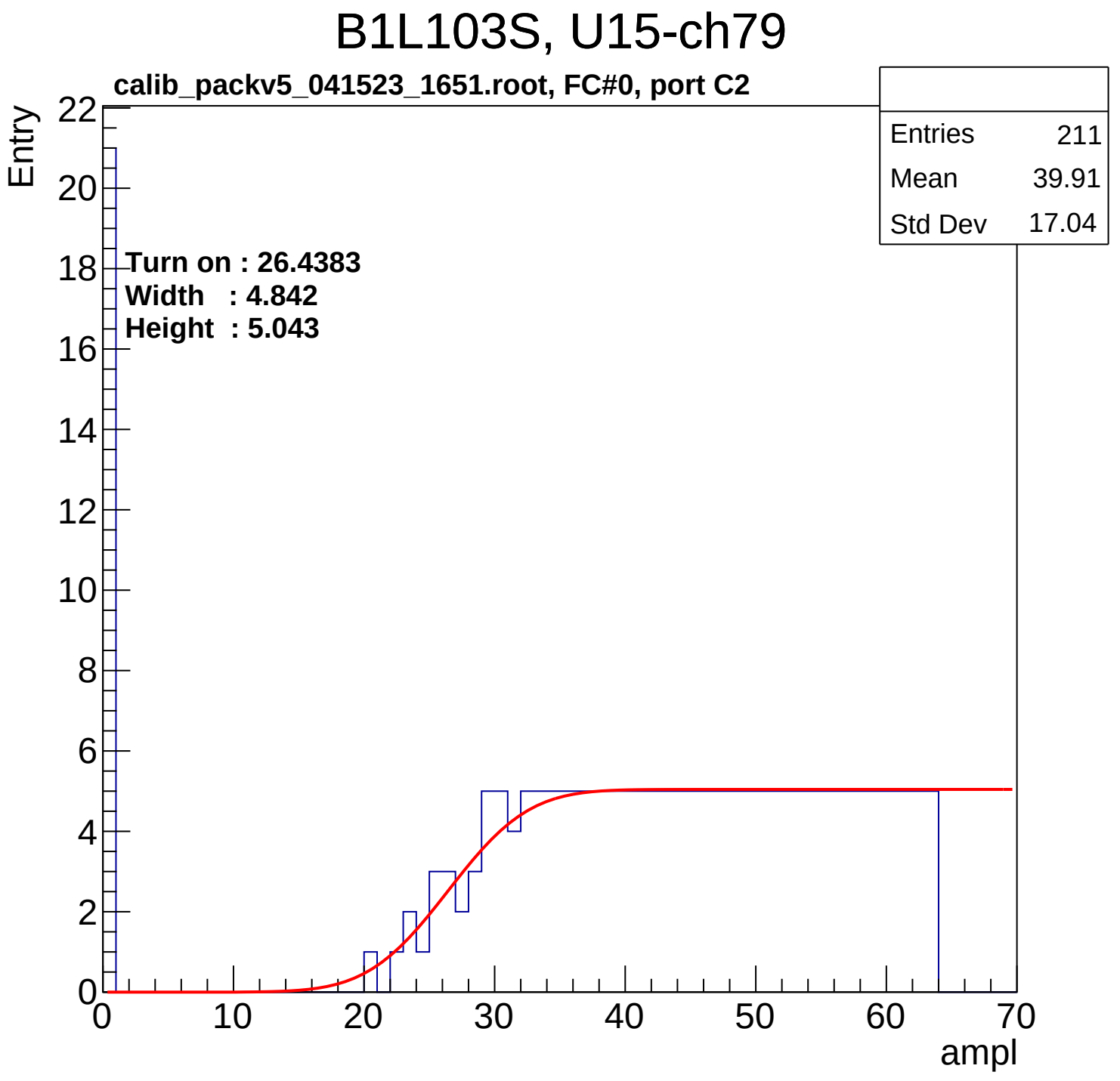
B1L103S, U15-ch79
calib_packv5_041523_1651.root, FC#0, port C2
Entries 211
Mean 39.91
Std Dev 17.04
Turn on : 26.4383
Width : 4.842
Height : 5.043
Entry
ampl
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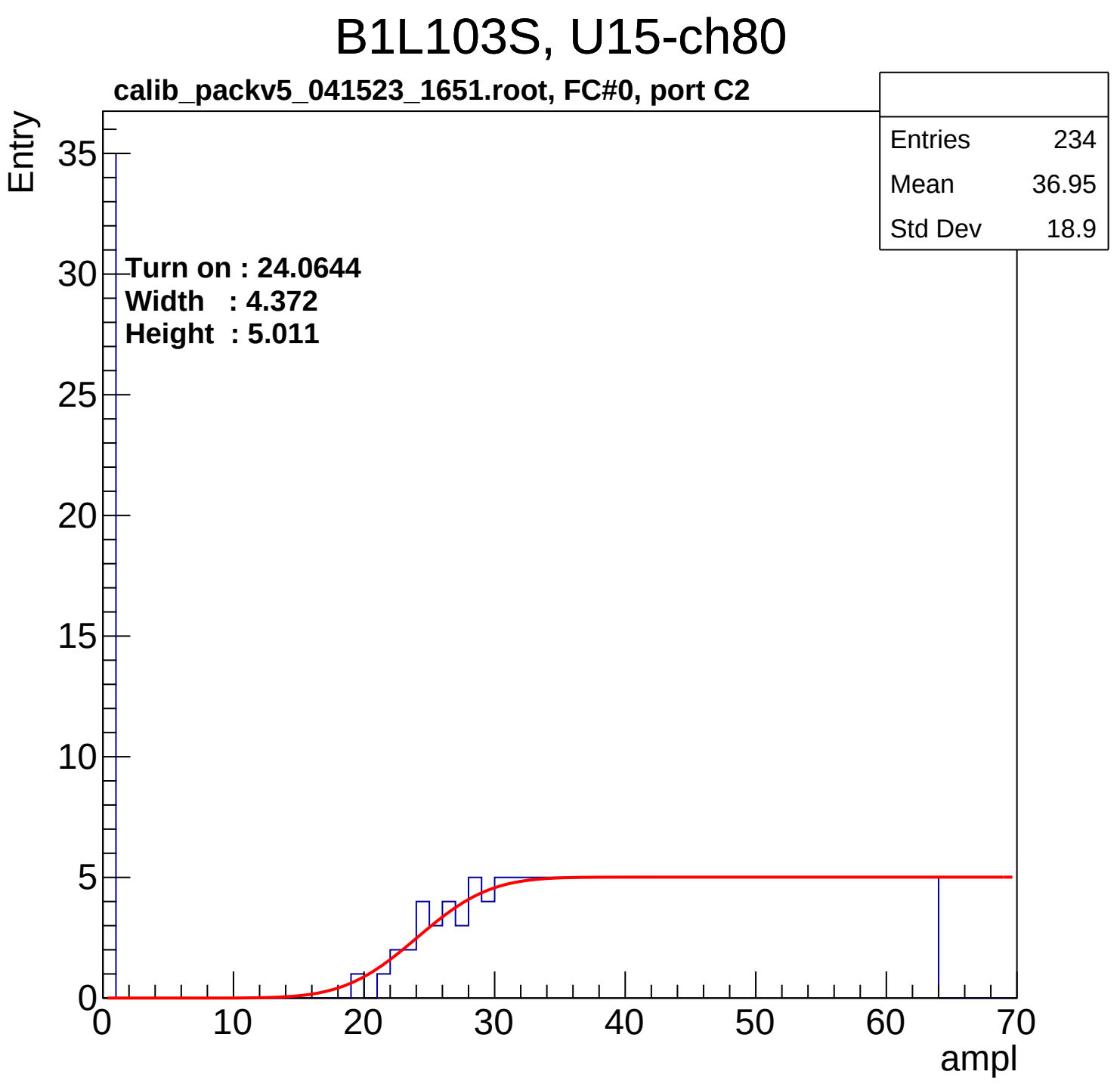
B1L103S, U15-ch80
calib_packv5_041523_1651.root, FC#0, port C2
Entries 234
Mean 36.95
Std Dev 18.9
Turn on : 24.0644
Width : 4.372
Height : 5.011
Entry
ampl
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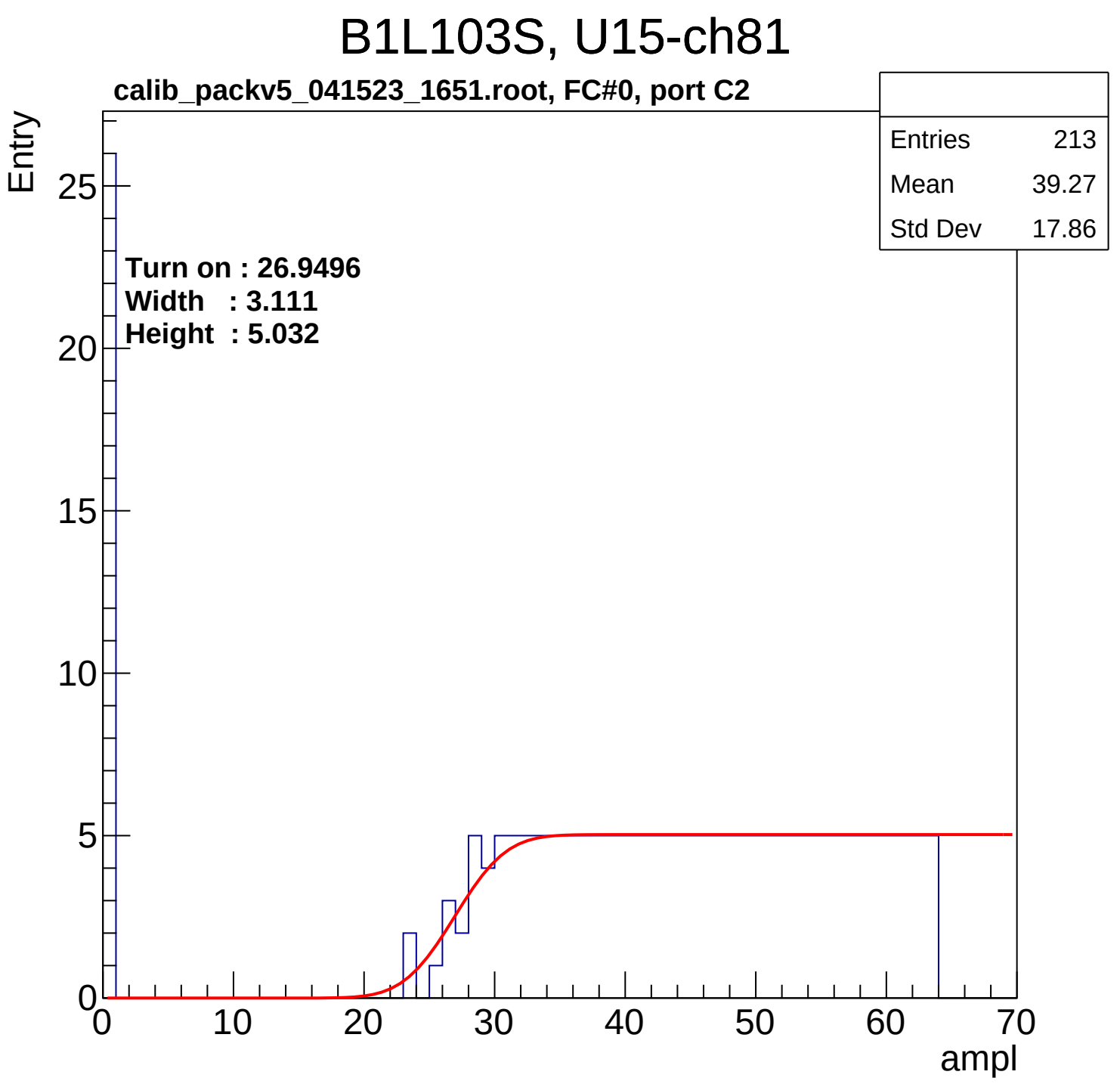
B1L103S, U15-ch81
calib_packv5_041523_1651.root, FC#0, port C2
Entries 213
Mean 39.27
Std Dev 17.86
Turn on : 26.9496
Width : 3.111
Height : 5.032
Entry
ampl
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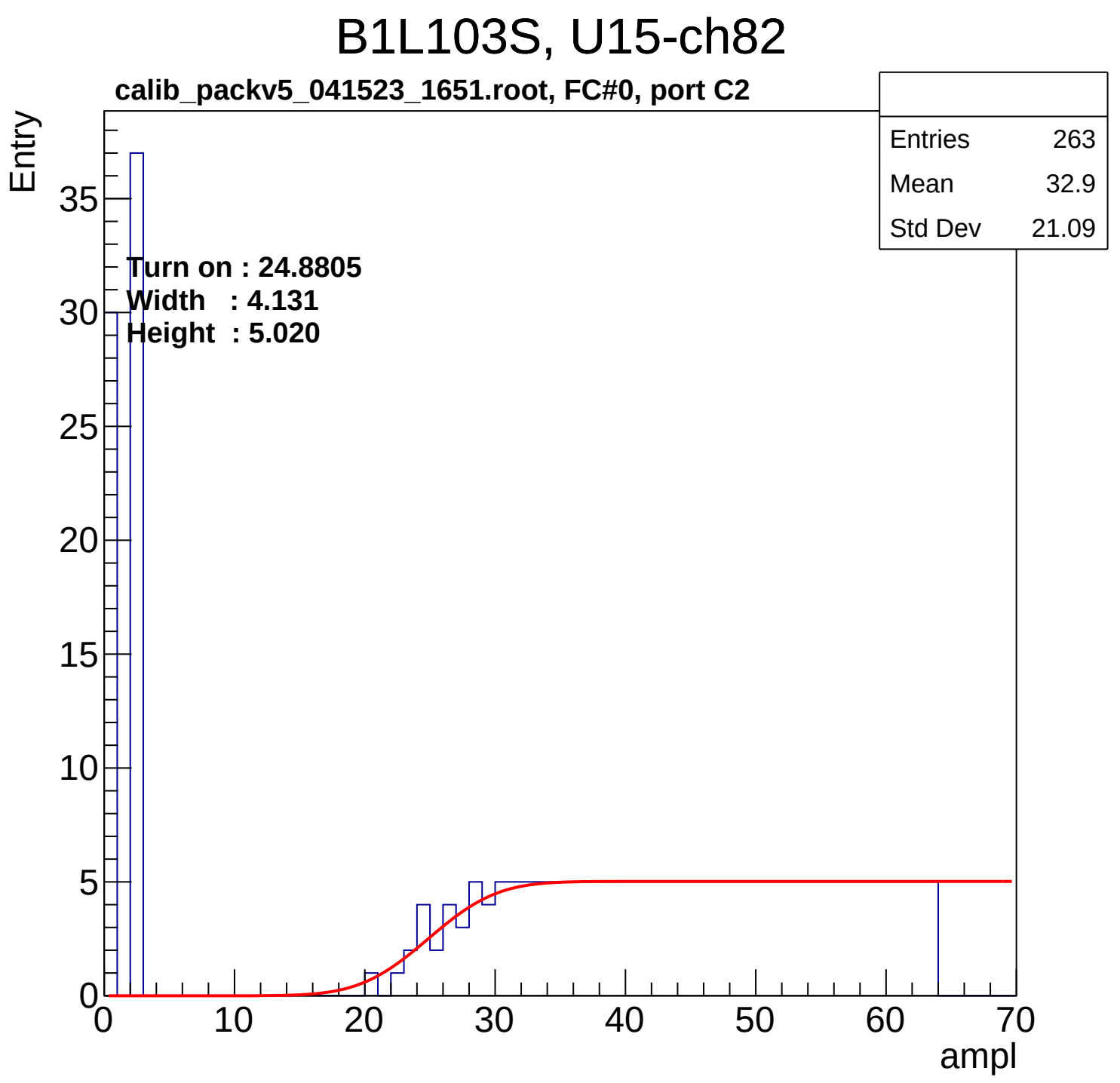
B1L103S, U15-ch82
calib_packv5_041523_1651.root, FC#0, port C2
Entries 263
Mean 32.9
Std Dev 21.09
Turn on : 24.8805
Width : 4.131
Height : 5.020
Entry
ampl
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5
10
15
20
25
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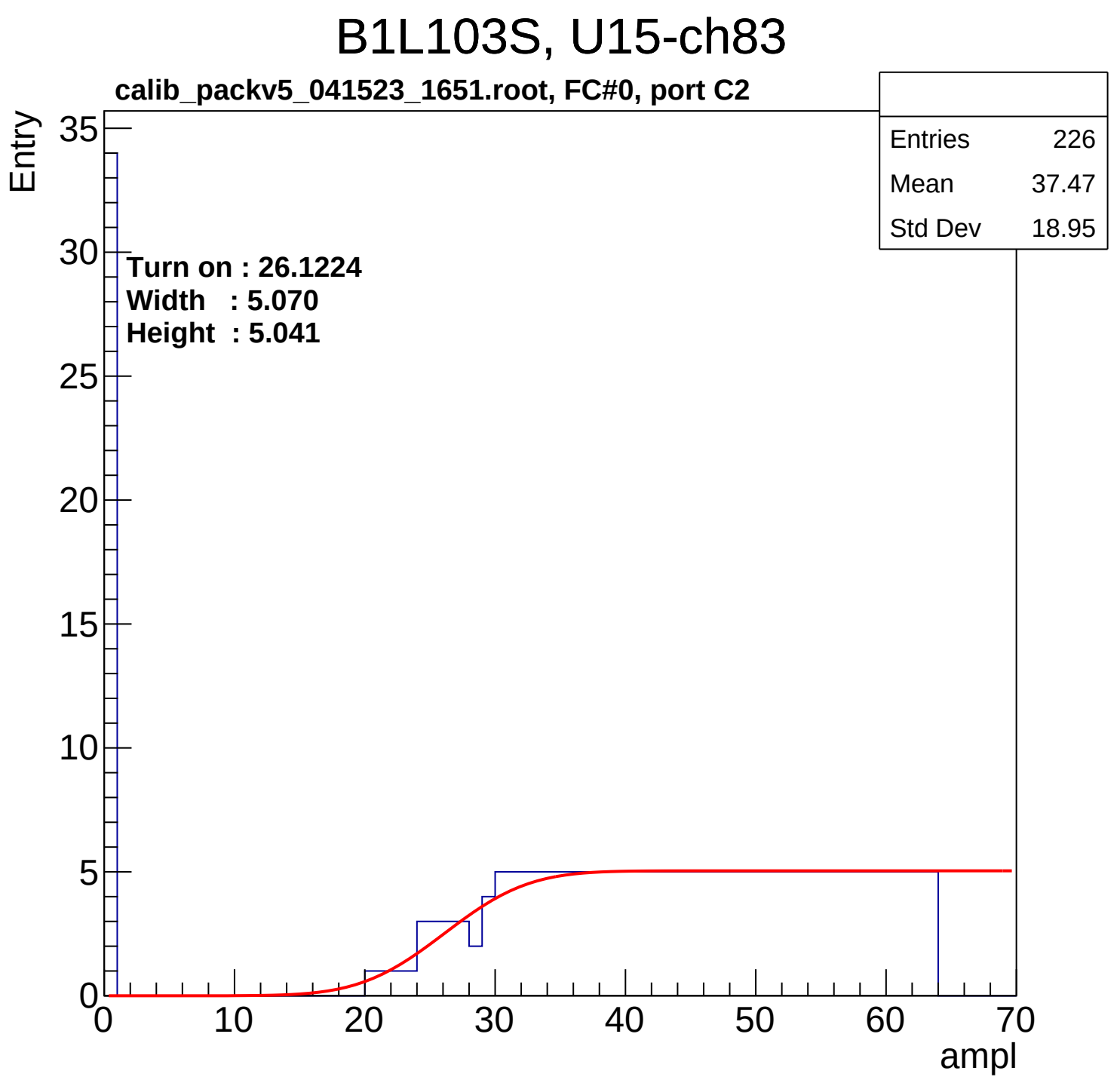
B1L103S, U15-ch83
calib_packv5_041523_1651.root, FC#0, port C2
Entries 226
Mean 37.47
Std Dev 18.95
Turn on : 26.1224
Width : 5.070
Height : 5.041
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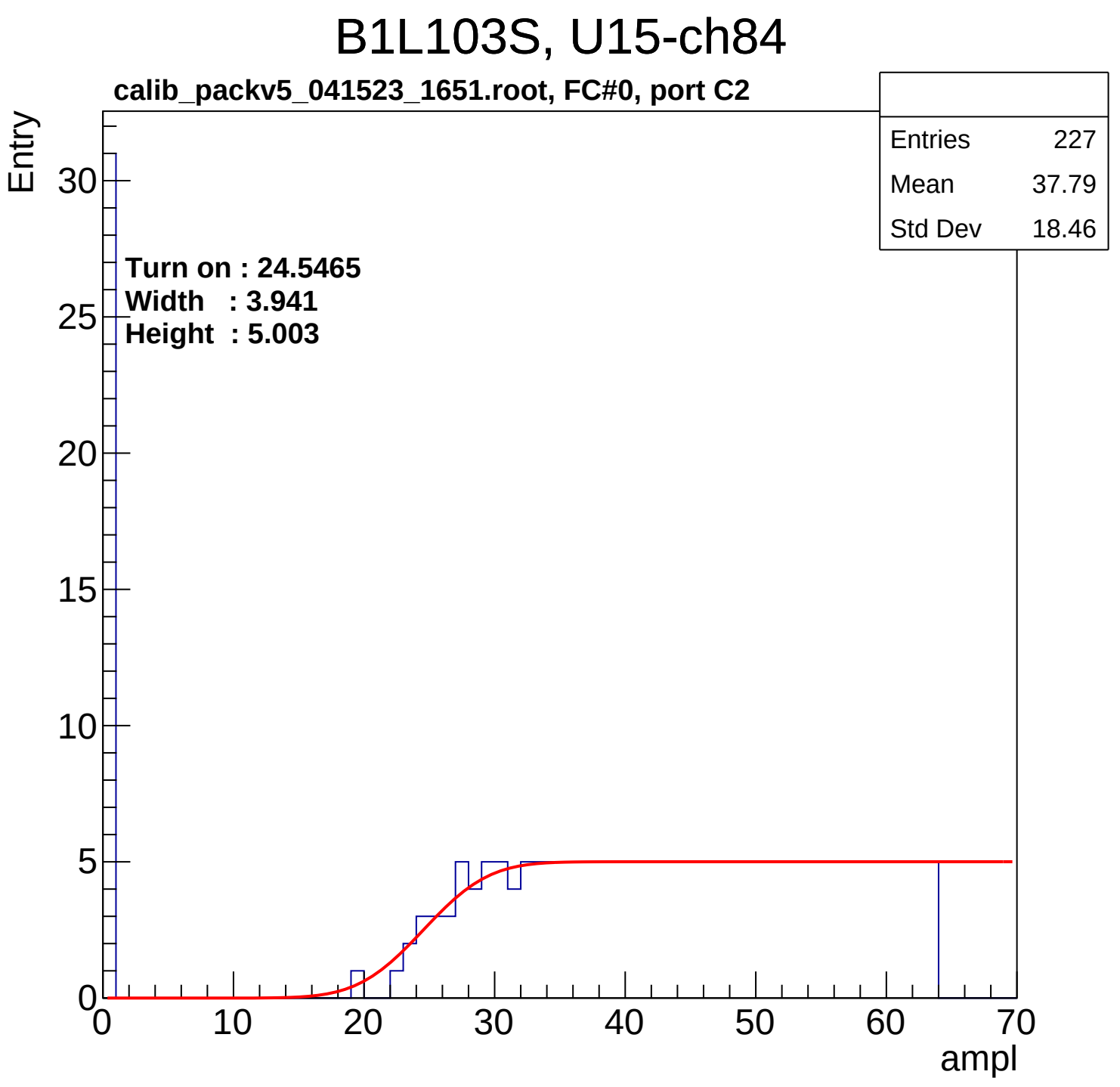
B1L103S, U15-ch84
calib_packv5_041523_1651.root, FC#0, port C2
Entries 227
Mean 37.79
Std Dev 18.46
Turn on : 24.5465
Width : 3.941
Height : 5.003
Entry
ampl
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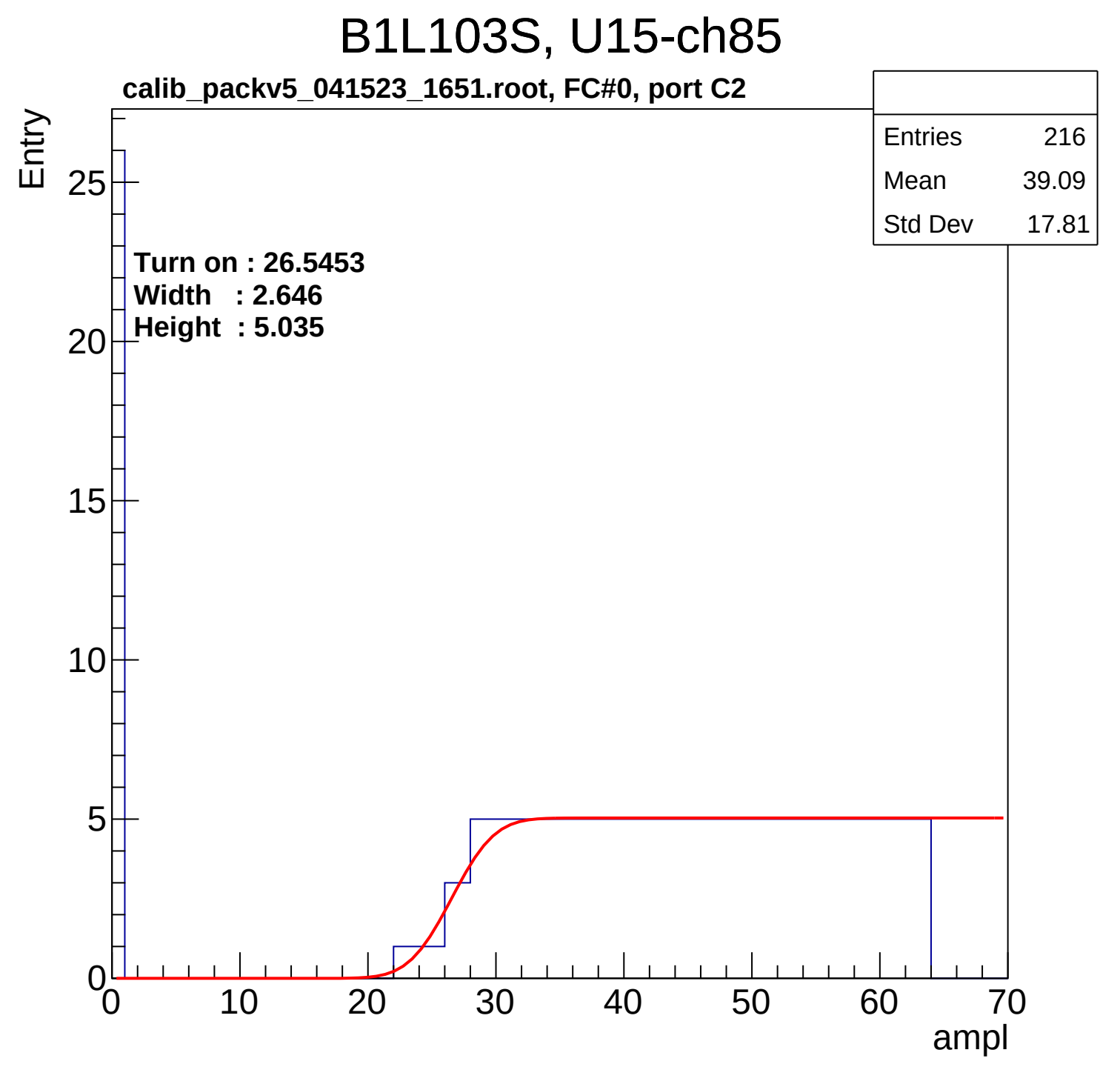
B1L103S, U15-ch85
calib_packv5_041523_1651.root, FC#0, port C2
Entries 216
Mean 39.09
Std Dev 17.81
Turn on : 26.5453
Width : 2.646
Height : 5.035
Entry
ampl
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5
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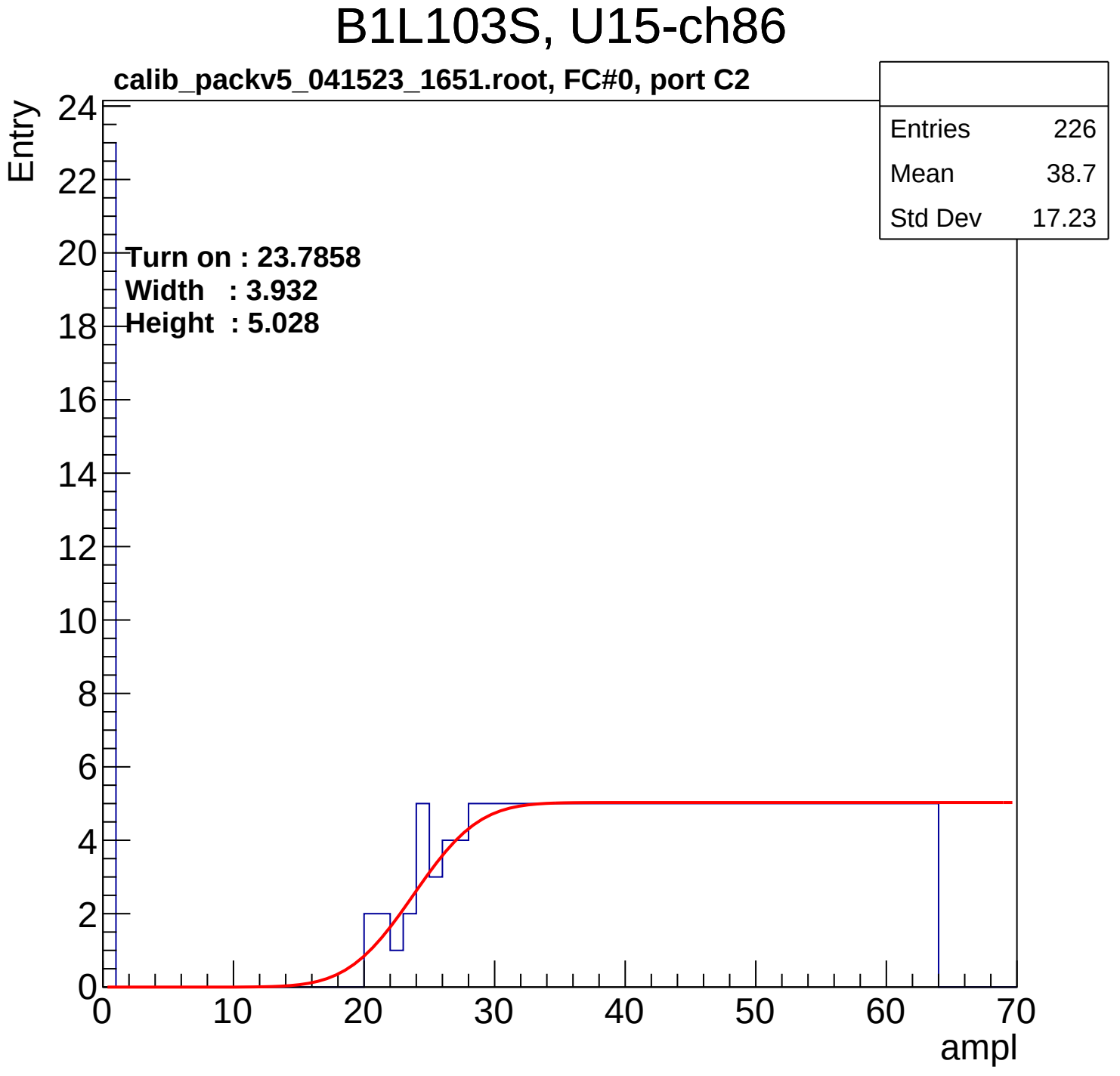
B1L103S, U15-ch86
calib_packv5_041523_1651.root, FC#0, port C2
Entries 226
Mean 38.7
Std Dev 17.23
Turn on : 23.7858
Width : 3.932
Height : 5.028
Entry
ampl
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2
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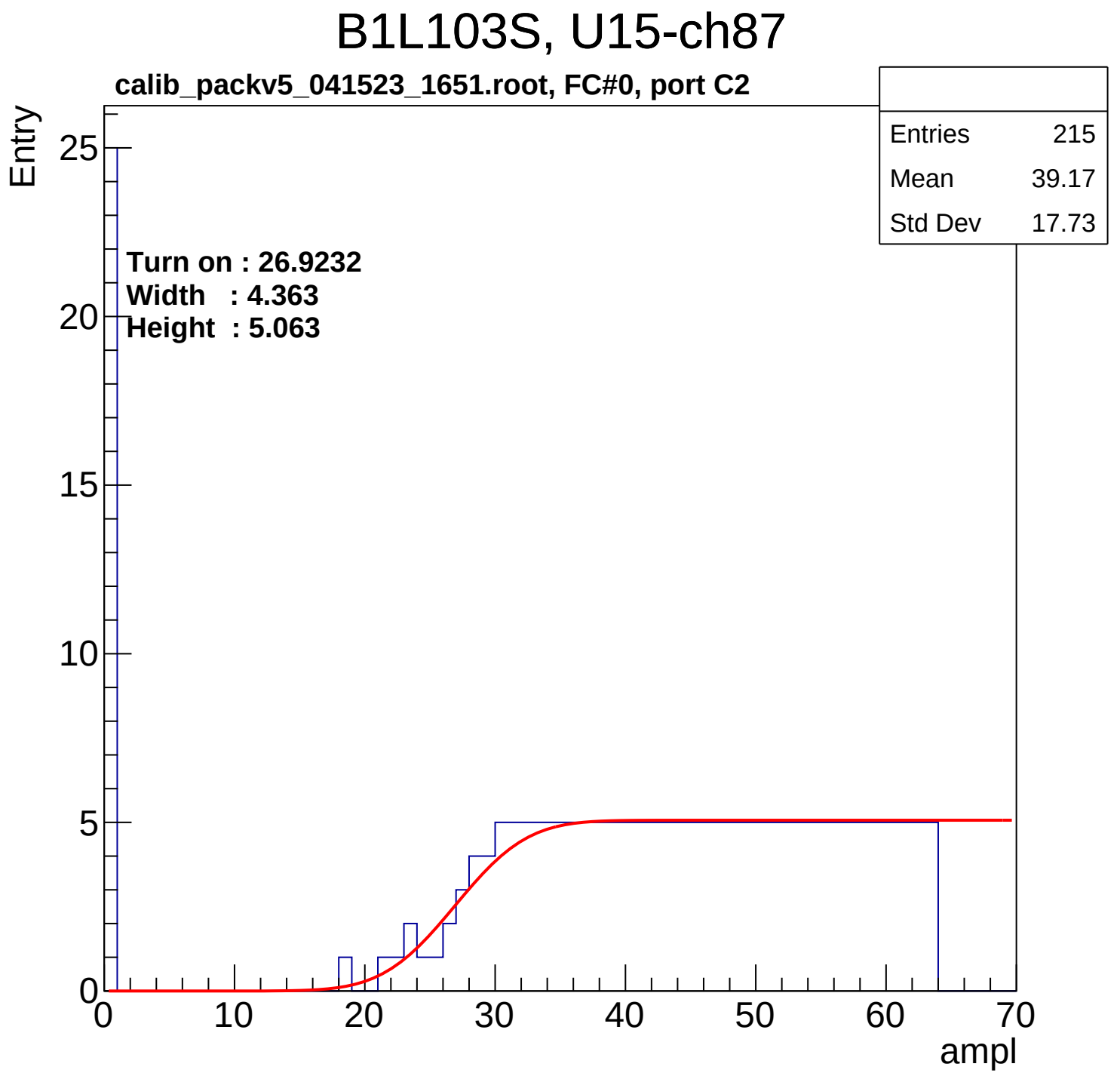
B1L103S, U15-ch87
calib_packv5_041523_1651.root, FC#0, port C2
Entries 215
Mean 39.17
Std Dev 17.73
Turn on : 26.9232
Width : 4.363
Height : 5.063
Entry
ampl
0
5
10
15
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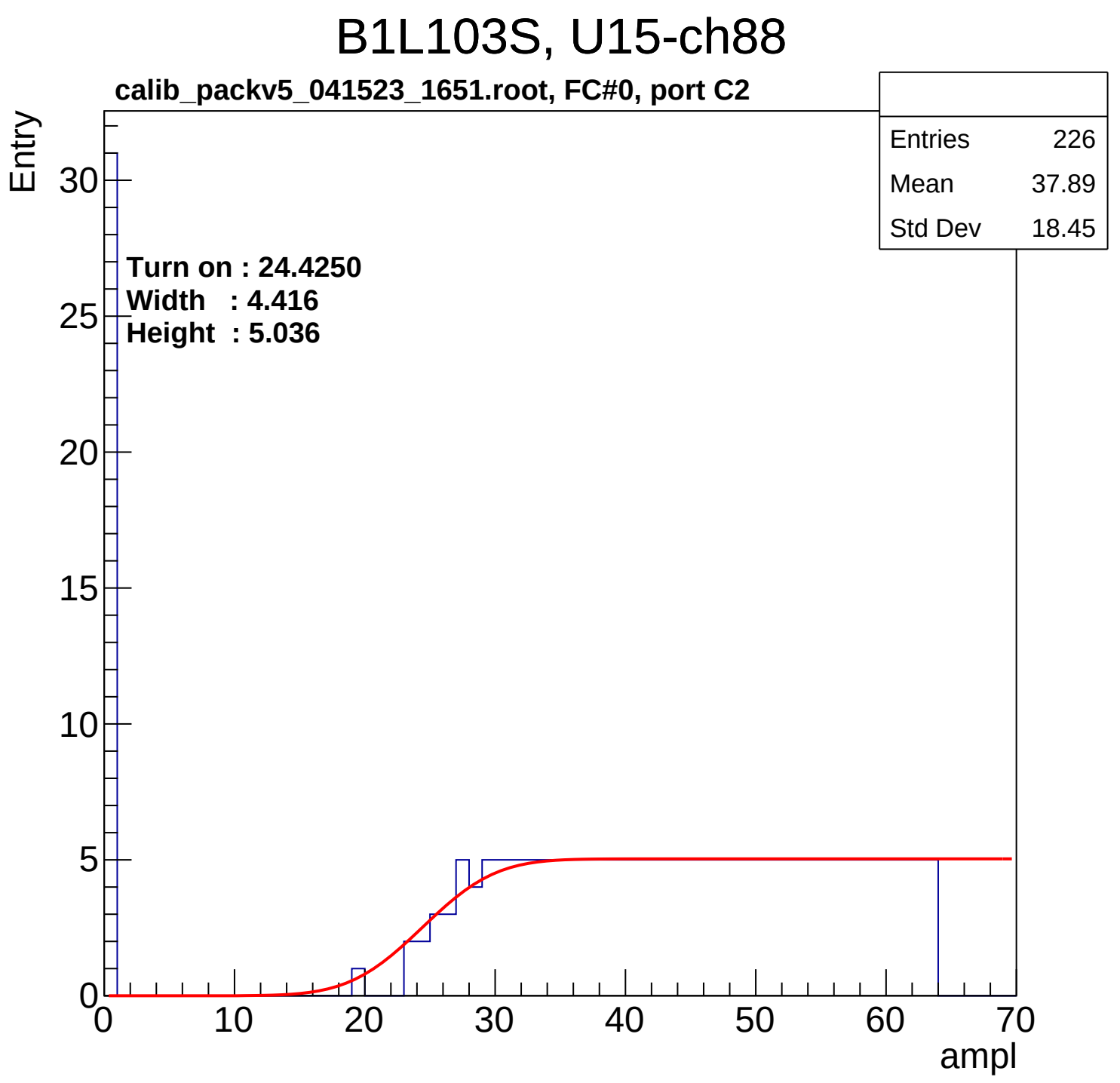
B1L103S, U15-ch88
calib_packv5_041523_1651.root, FC#0, port C2
Entries 226
Mean 37.89
Std Dev 18.45
Turn on : 24.4250
Width : 4.416
Height : 5.036
Entry
ampl
0
5
10
15
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0
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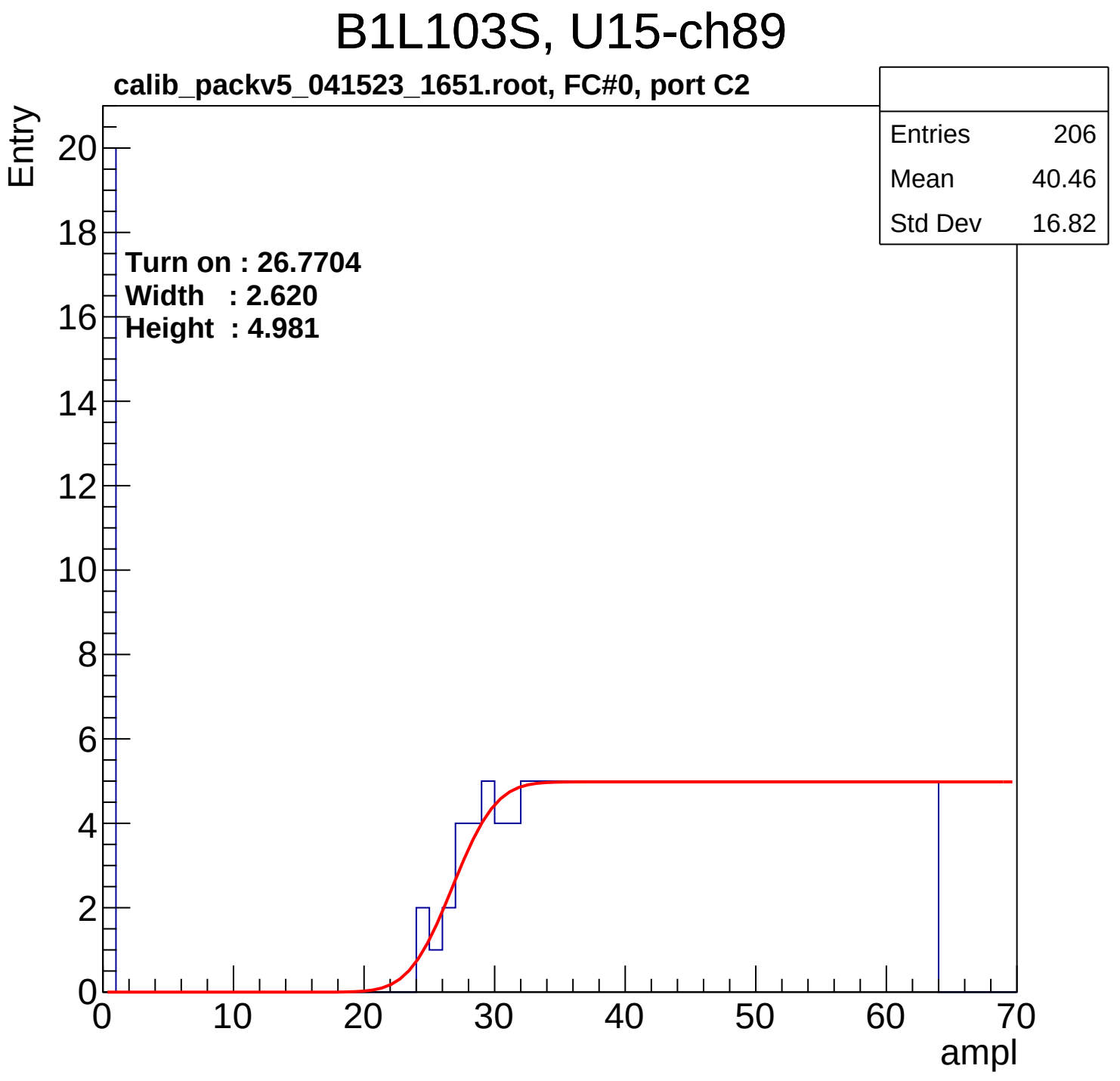
B1L103S, U15-ch89
calib_packv5_041523_1651.root, FC#0, port C2
Entries 206
Mean 40.46
Std Dev 16.82
Turn on : 26.7704
Width : 2.620
Height : 4.981
Entry
ampl
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6
8
10
12
14
16
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0
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60
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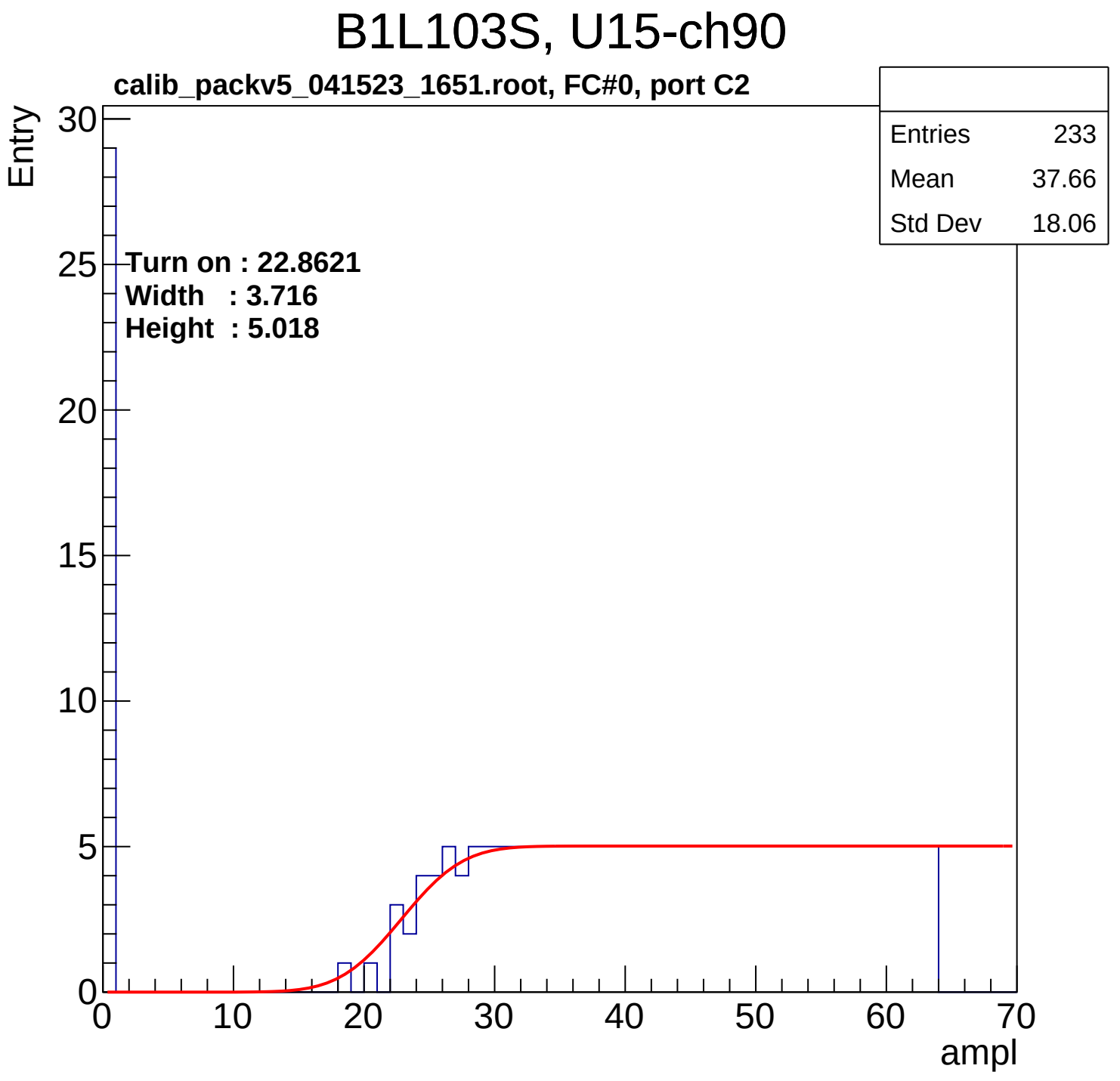
B1L103S, U15-ch90
calib_packv5_041523_1651.root, FC#0, port C2
Entries 233
Mean 37.66
Std Dev 18.06
Turn on : 22.8621
Width : 3.716
Height : 5.018
Entry
ampl
0
5
10
15
20
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0
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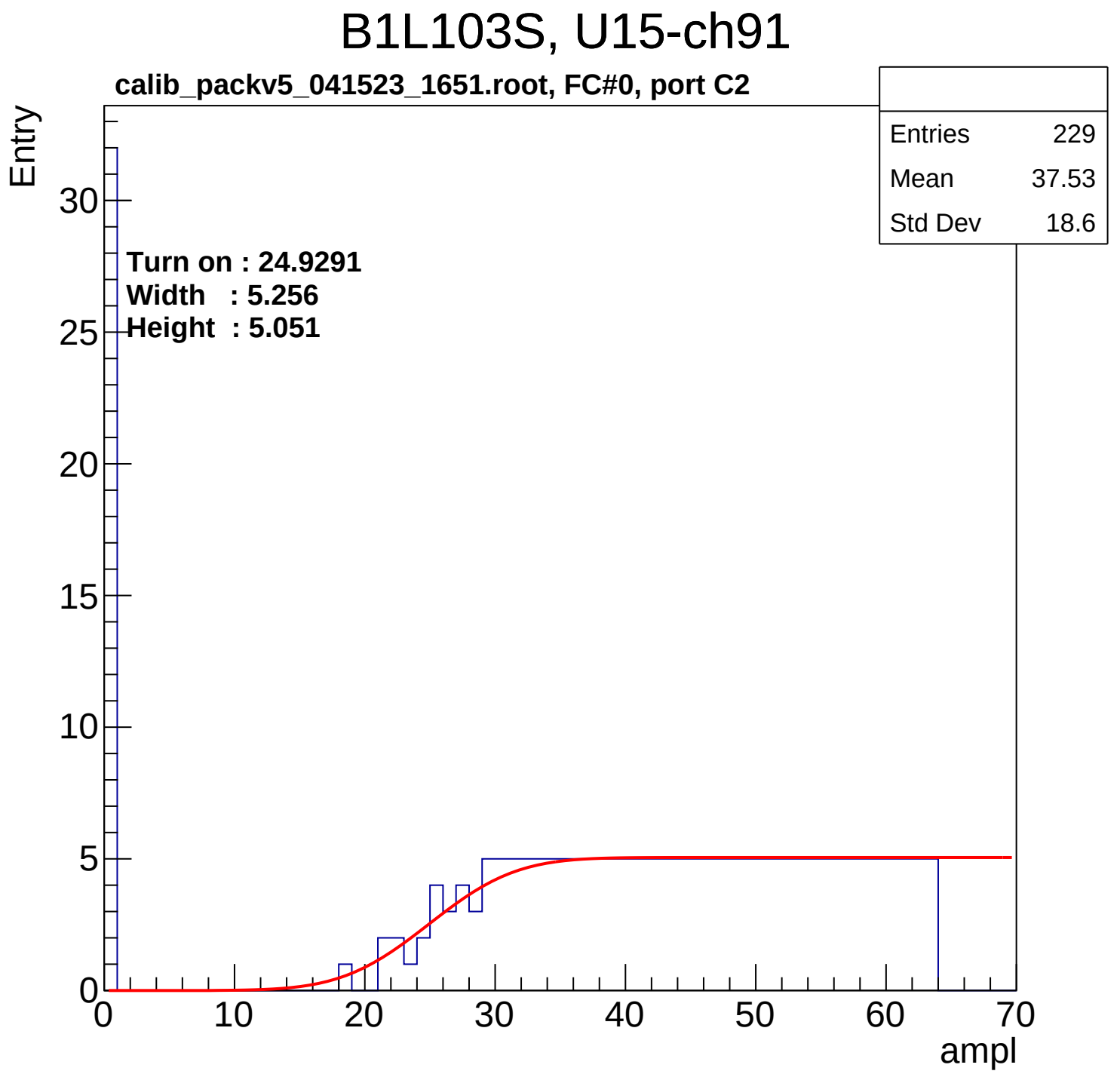
B1L103S, U15-ch91
calib_packv5_041523_1651.root, FC#0, port C2
Entries 229
Mean 37.53
Std Dev 18.6
Turn on : 24.9291
Width : 5.256
Height : 5.051
Entry
ampl
0
5
10
15
20
25
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0
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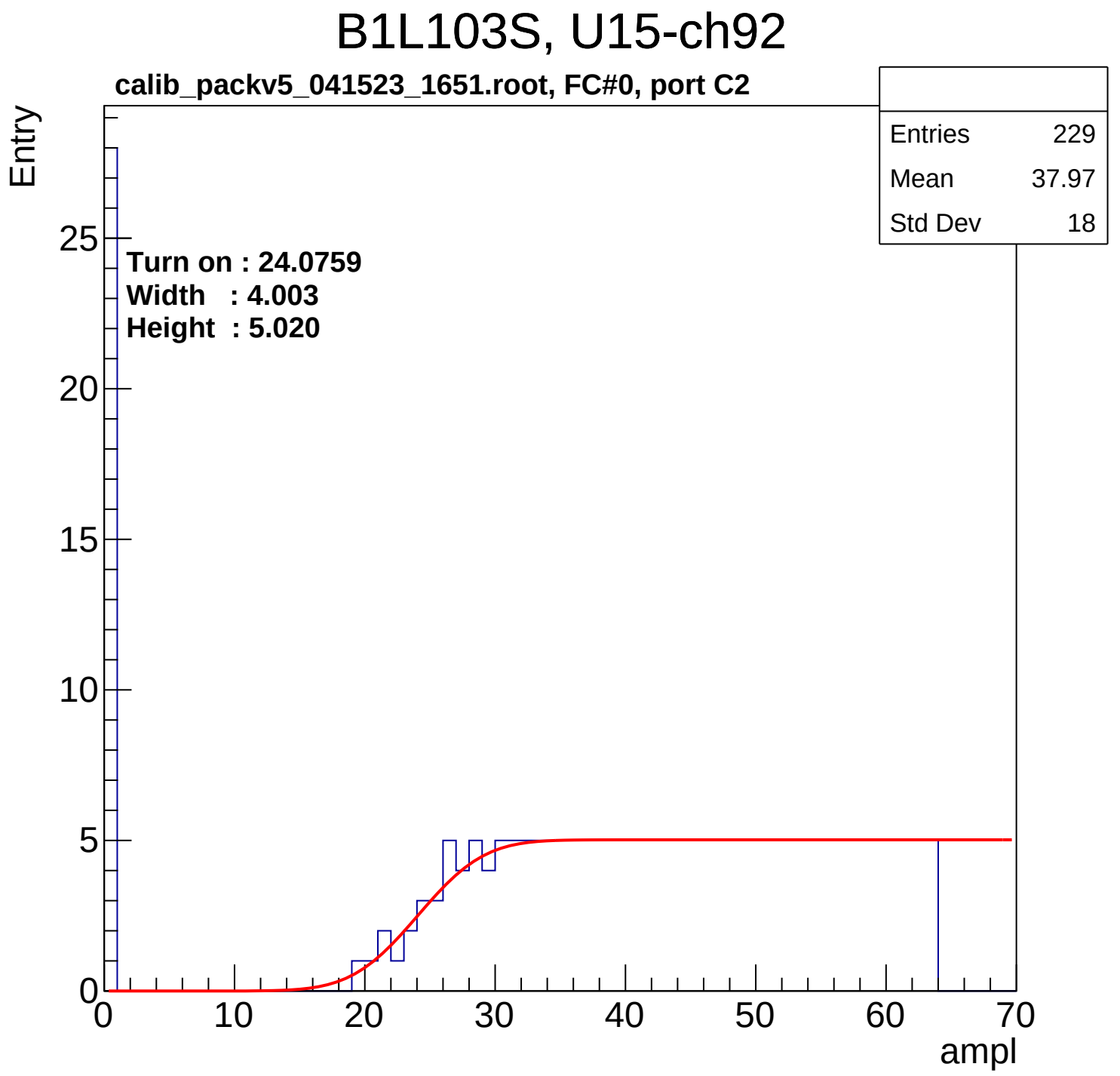
B1L103S, U15-ch92
calib_packv5_041523_1651.root, FC#0, port C2
Entries 229
Mean 37.97
Std Dev 18
Turn on : 24.0759
Width : 4.003
Height : 5.020
Entry
ampl
0
5
10
15
20
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0
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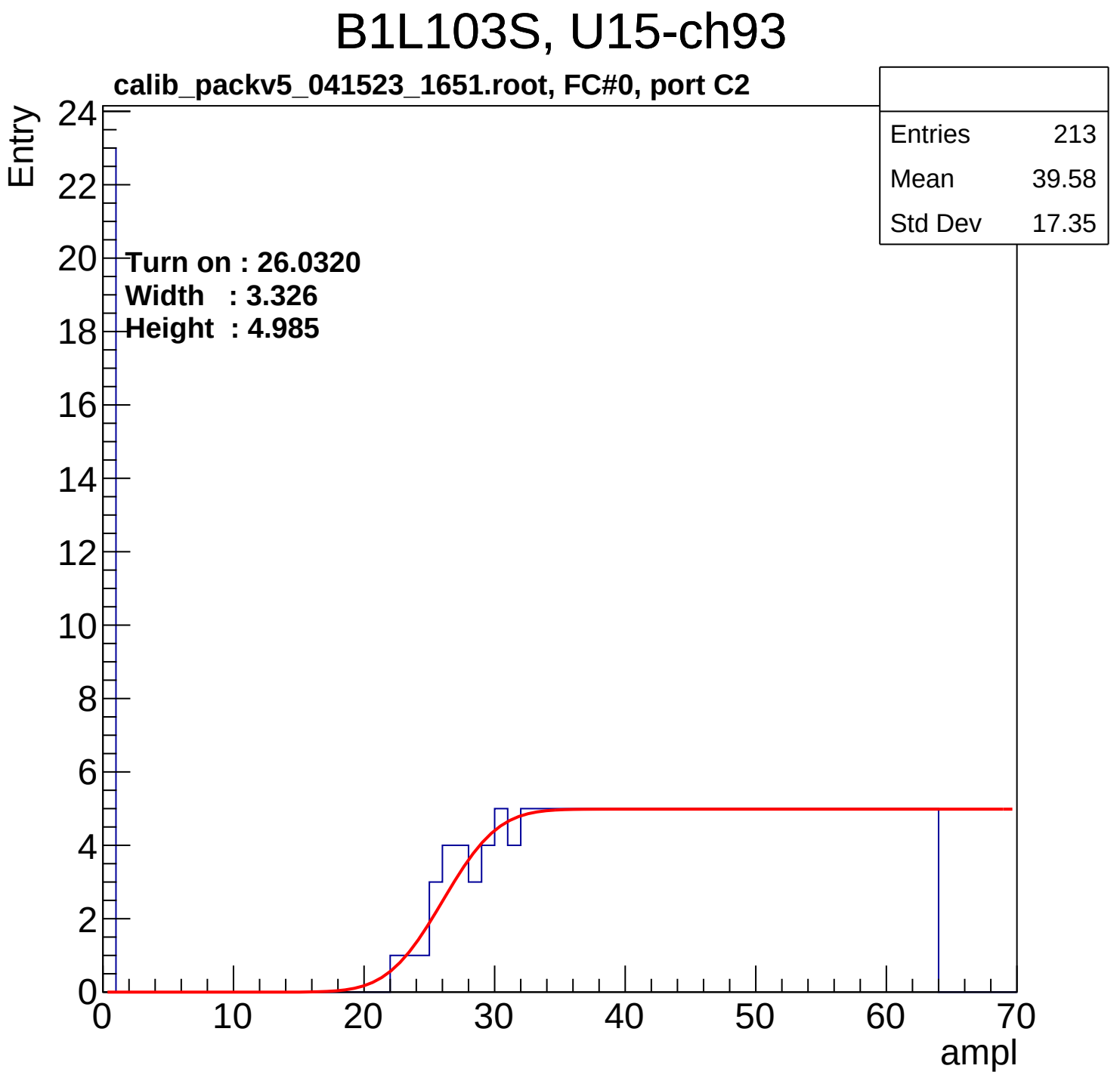
B1L103S, U15-ch93
calib_packv5_041523_1651.root, FC#0, port C2
Entries 213
Mean 39.58
Std Dev 17.35
Turn on : 26.0320
Width : 3.326
Height : 4.985
Entry
ampl
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2
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10
12
14
16
18
20
22
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0
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40
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60
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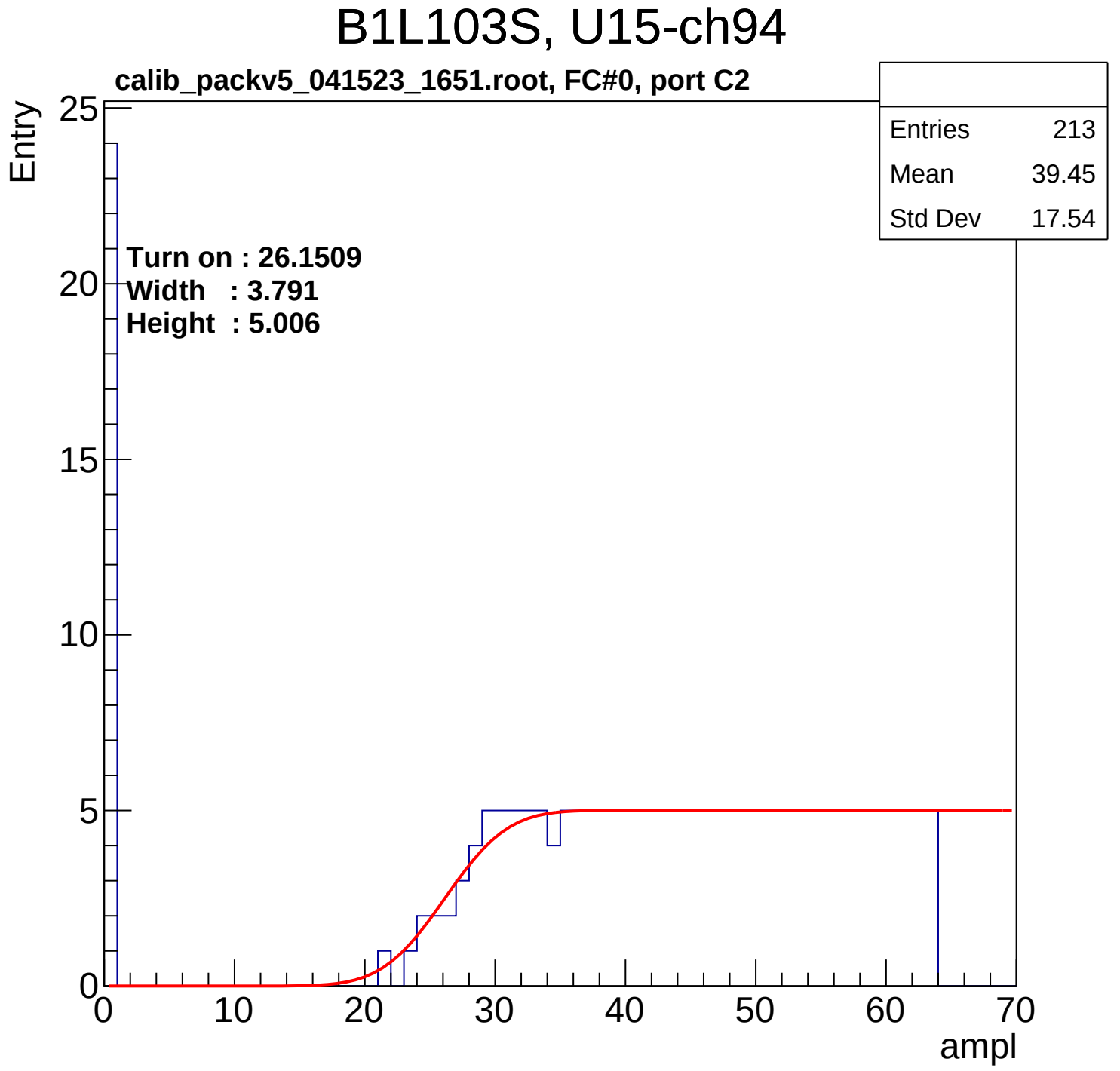
B1L103S, U15-ch94
calib_packv5_041523_1651.root, FC#0, port C2
Entries 213
Mean 39.45
Std Dev 17.54
Turn on : 26.1509
Width : 3.791
Height : 5.006
Entry
ampl
0
5
10
15
20
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0
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20
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40
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60
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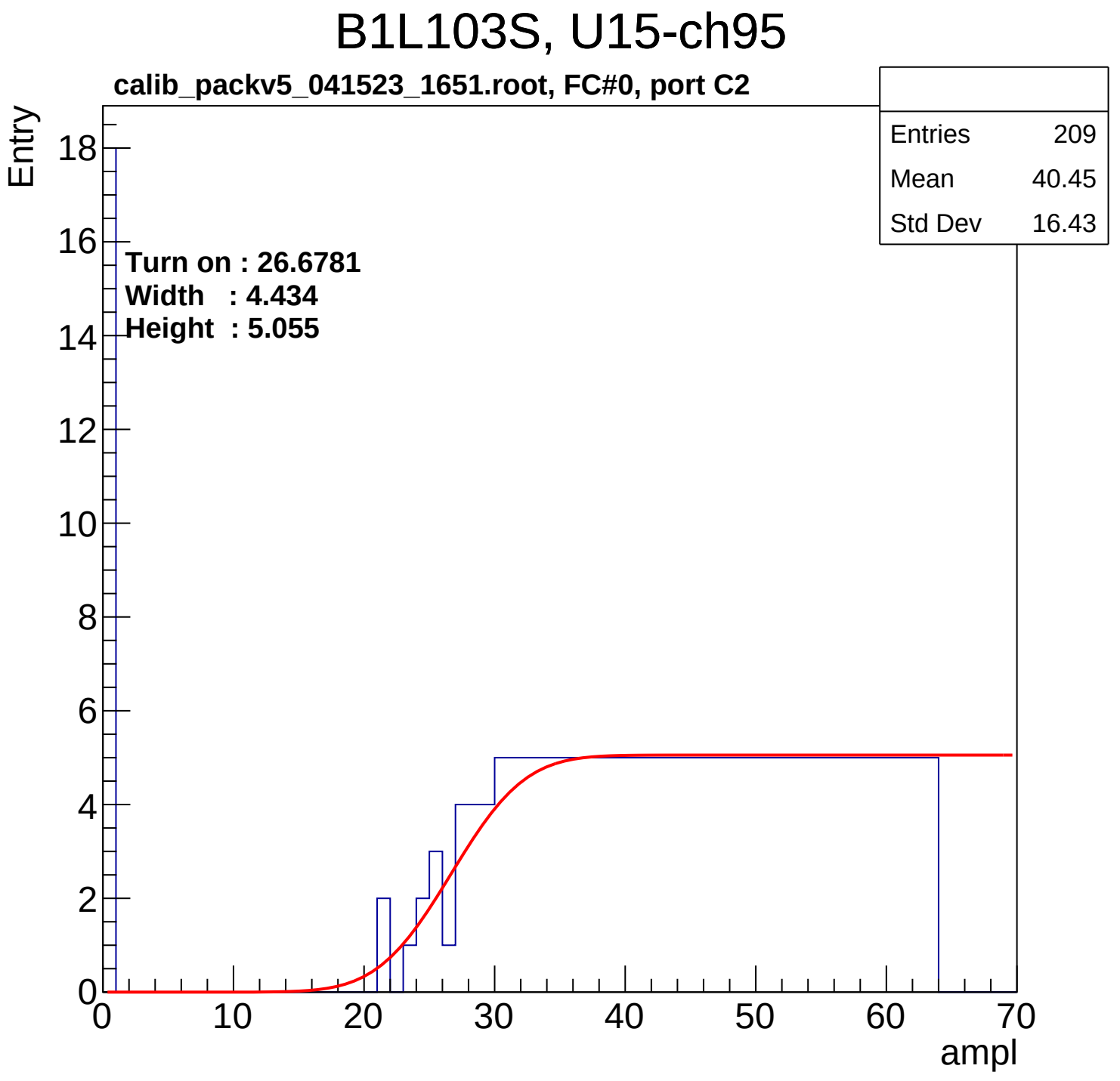
B1L103S, U15-ch95
calib_packv5_041523_1651.root, FC#0, port C2
Entries 209
Mean 40.45
Std Dev 16.43
Turn on : 26.6781
Width : 4.434
Height : 5.055
Entry
ampl
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4
6
8
10
12
14
16
18
0
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20
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40
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60
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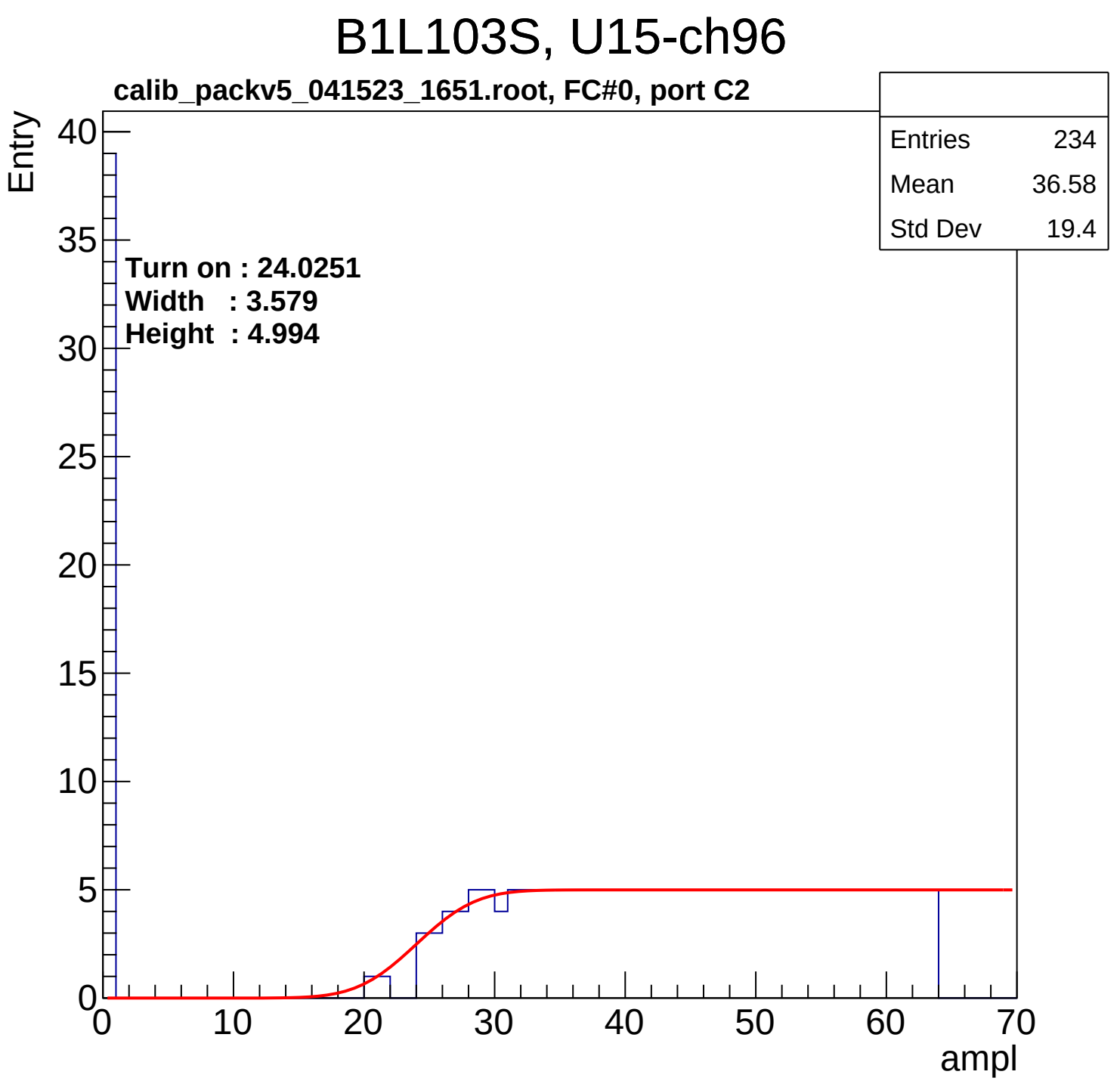
B1L103S, U15-ch96
calib_packv5_041523_1651.root, FC#0, port C2
Entries 234
Mean 36.58
Std Dev 19.4
Turn on : 24.0251
Width : 3.579
Height : 4.994
Entry
ampl
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5
10
15
20
25
30
35
40
0
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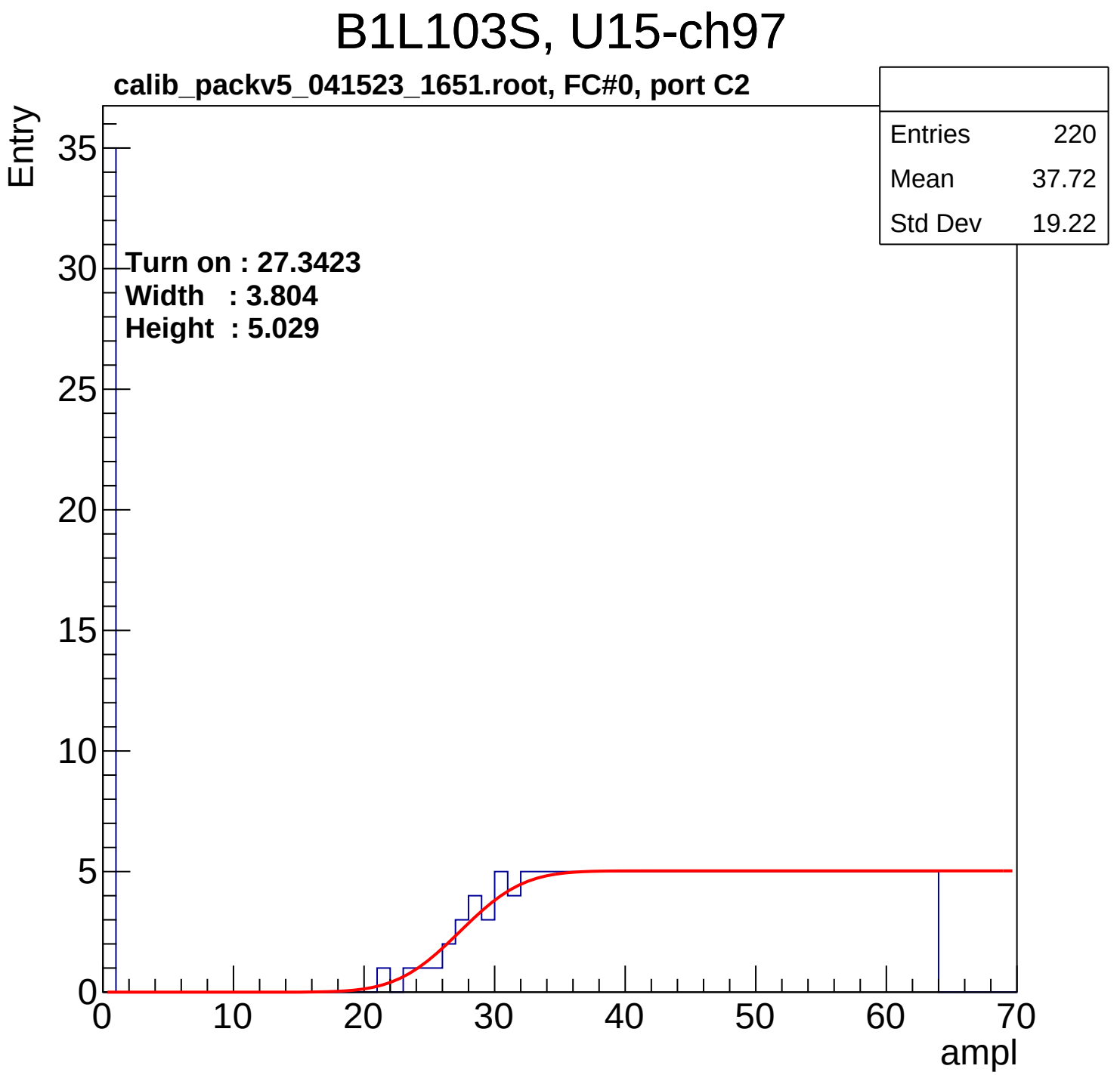
B1L103S, U15-ch97
calib_packv5_041523_1651.root, FC#0, port C2
Entries 220
Mean 37.72
Std Dev 19.22
Turn on : 27.3423
Width : 3.804
Height : 5.029
Entry
ampl
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5
10
15
20
25
30
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0
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60
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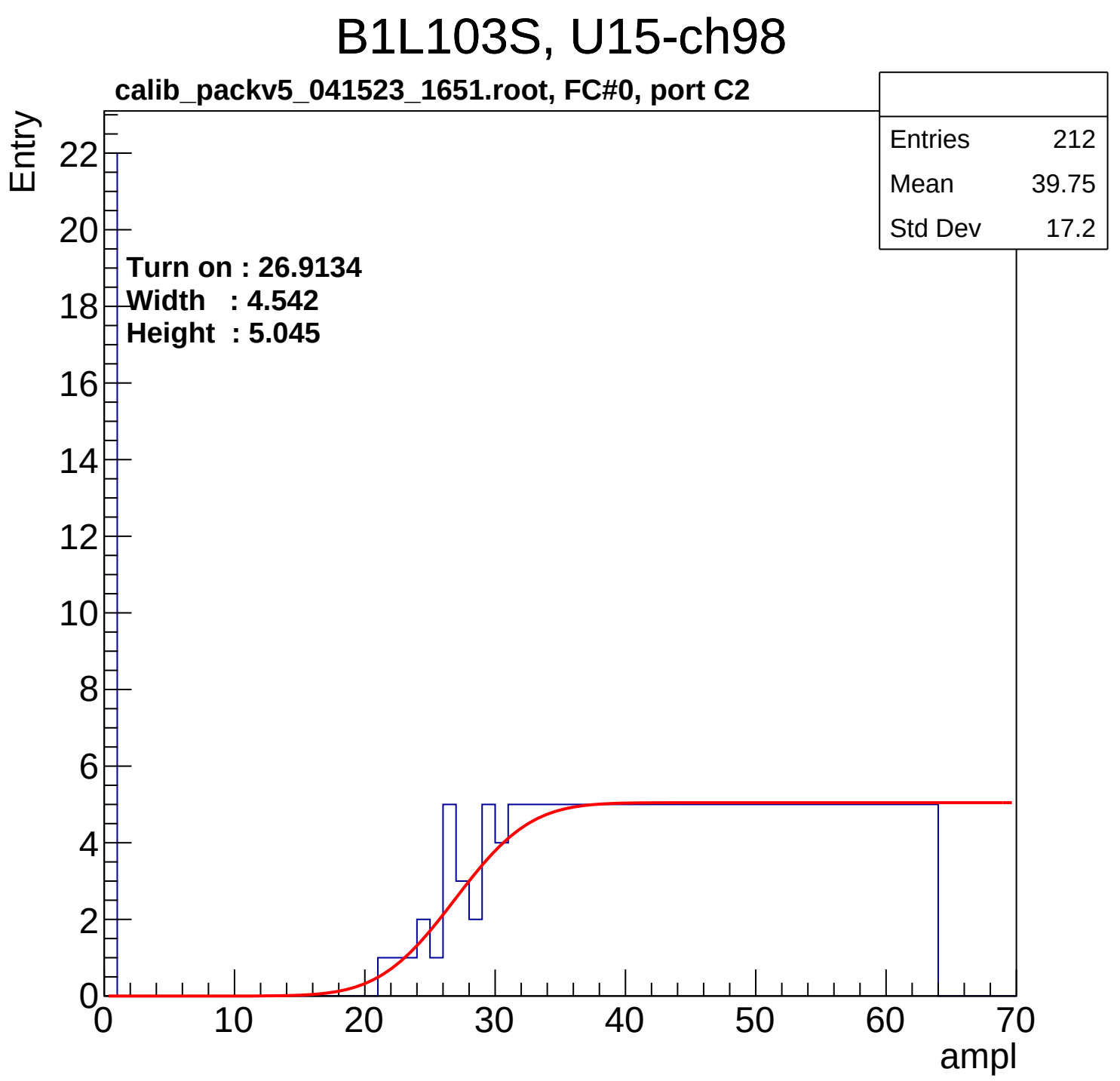
B1L103S, U15-ch98
calib_packv5_041523_1651.root, FC#0, port C2
Entries 212
Mean 39.75
Std Dev 17.2
Turn on : 26.9134
Width : 4.542
Height : 5.045
Entry
ampl
0
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6
8
10
12
14
16
18
20
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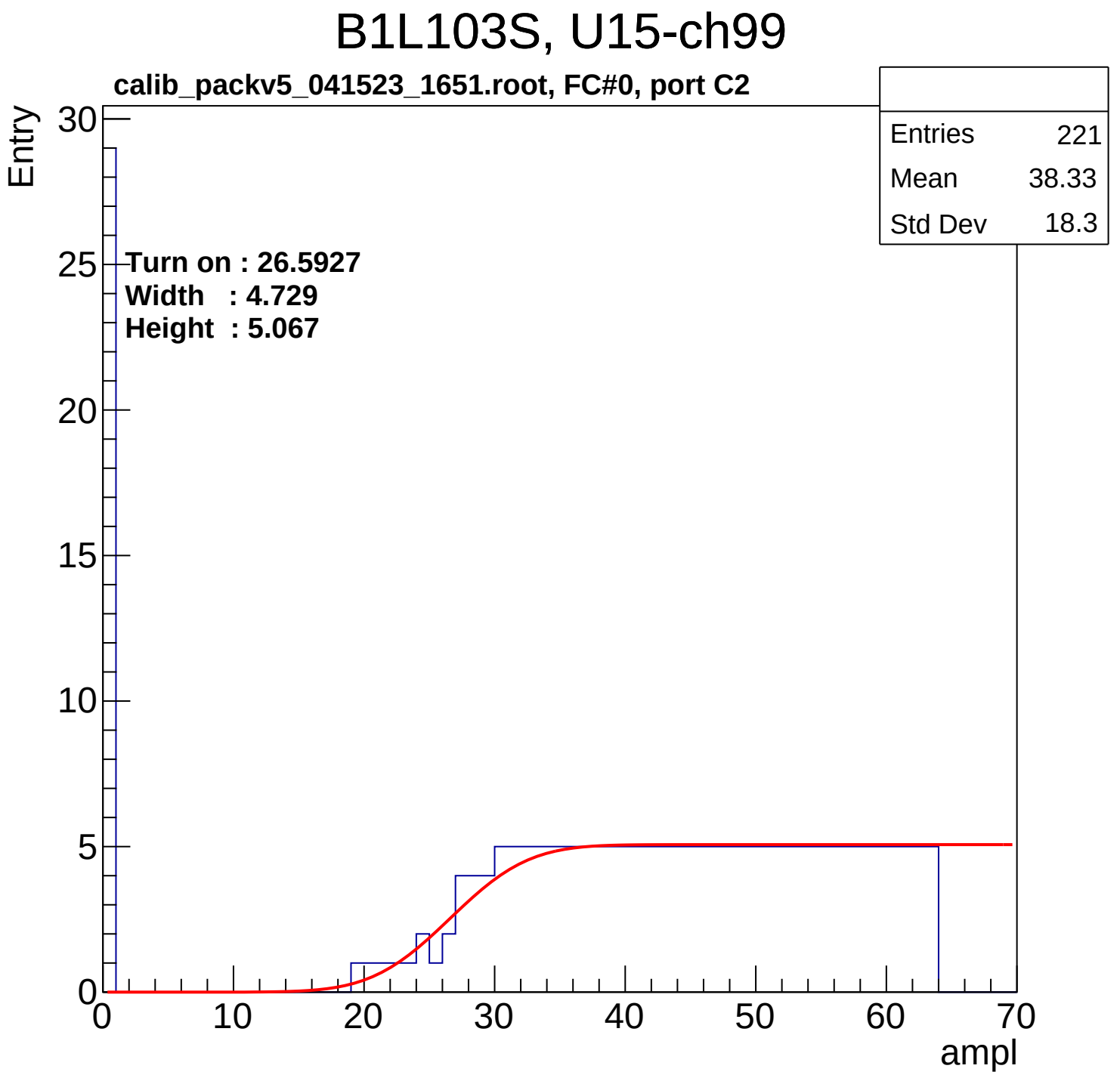
B1L103S, U15-ch99
calib_packv5_041523_1651.root, FC#0, port C2
Entries 221
Mean 38.33
Std Dev 18.3
Turn on : 26.5927
Width : 4.729
Height : 5.067
Entry
ampl
0
5
10
15
20
25
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0
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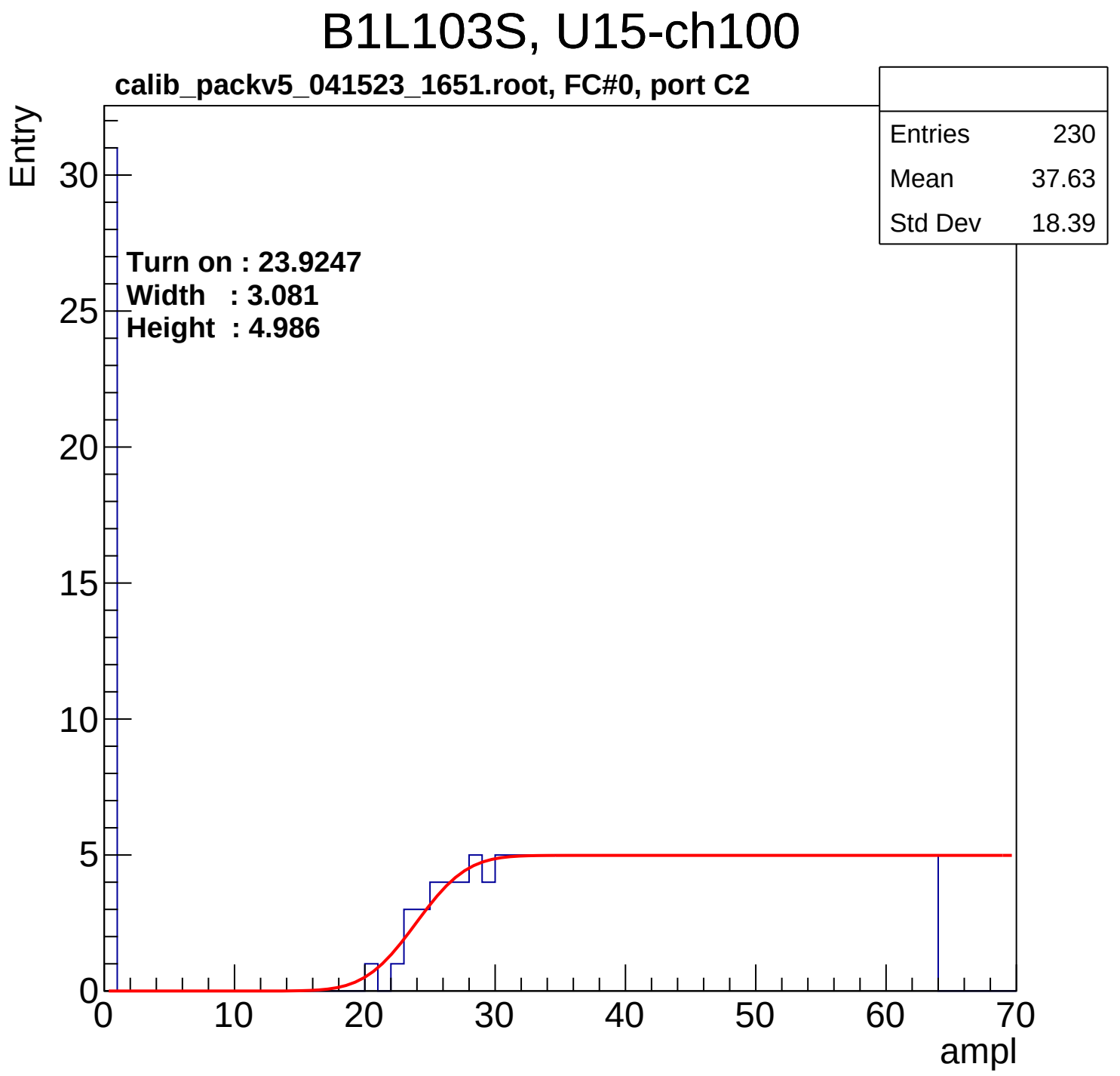
B1L103S, U15-ch100
calib_packv5_041523_1651.root, FC#0, port C2
Entries 230
Mean 37.63
Std Dev 18.39
Turn on : 23.9247
Width : 3.081
Height : 4.986
Entry
ampl
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15
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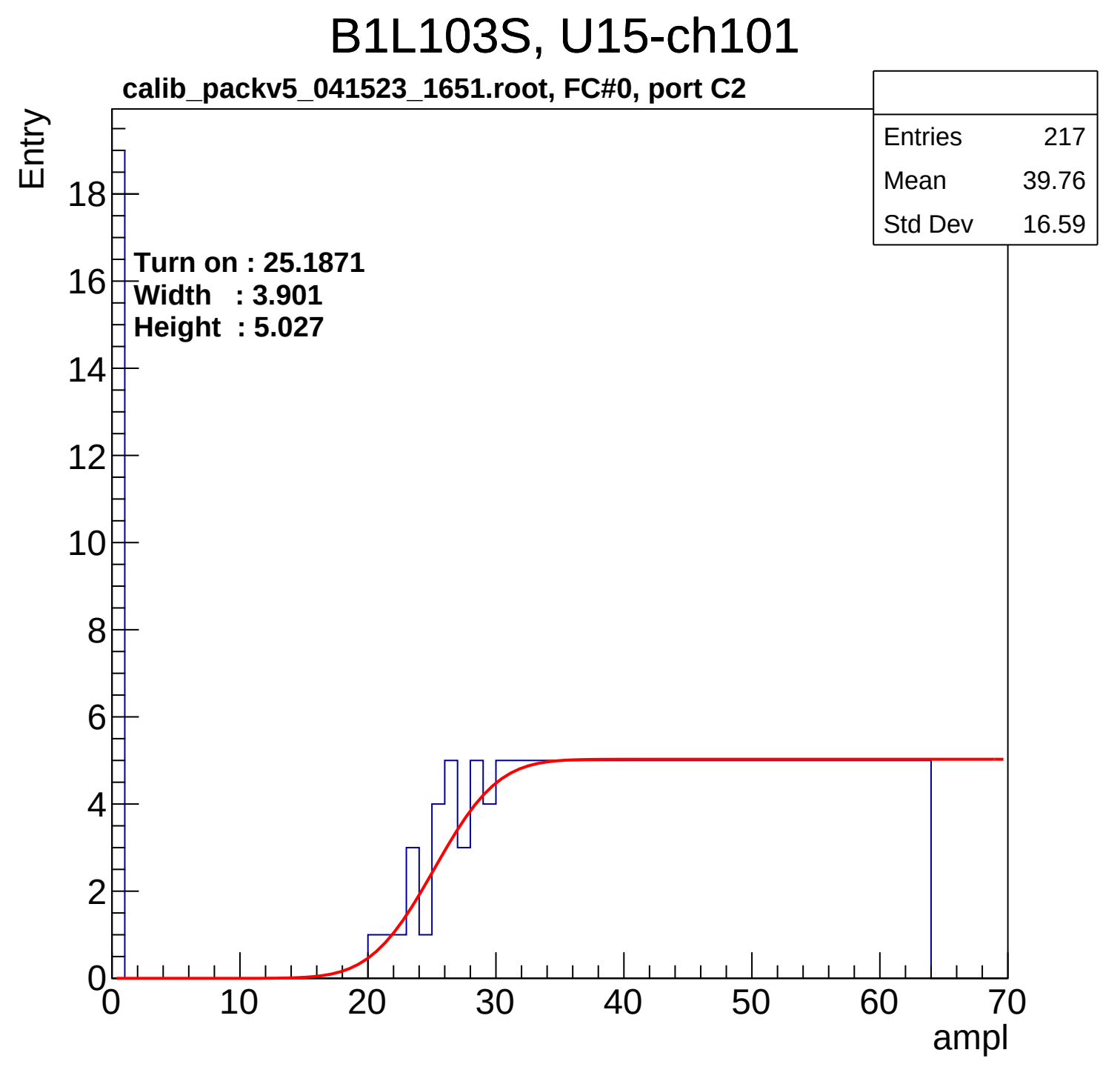
B1L103S, U15-ch101
calib_packv5_041523_1651.root, FC#0, port C2
Entries 217
Mean 39.76
Std Dev 16.59
Turn on : 25.1871
Width : 3.901
Height : 5.027
Entry
ampl
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4
6
8
10
12
14
16
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0
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60
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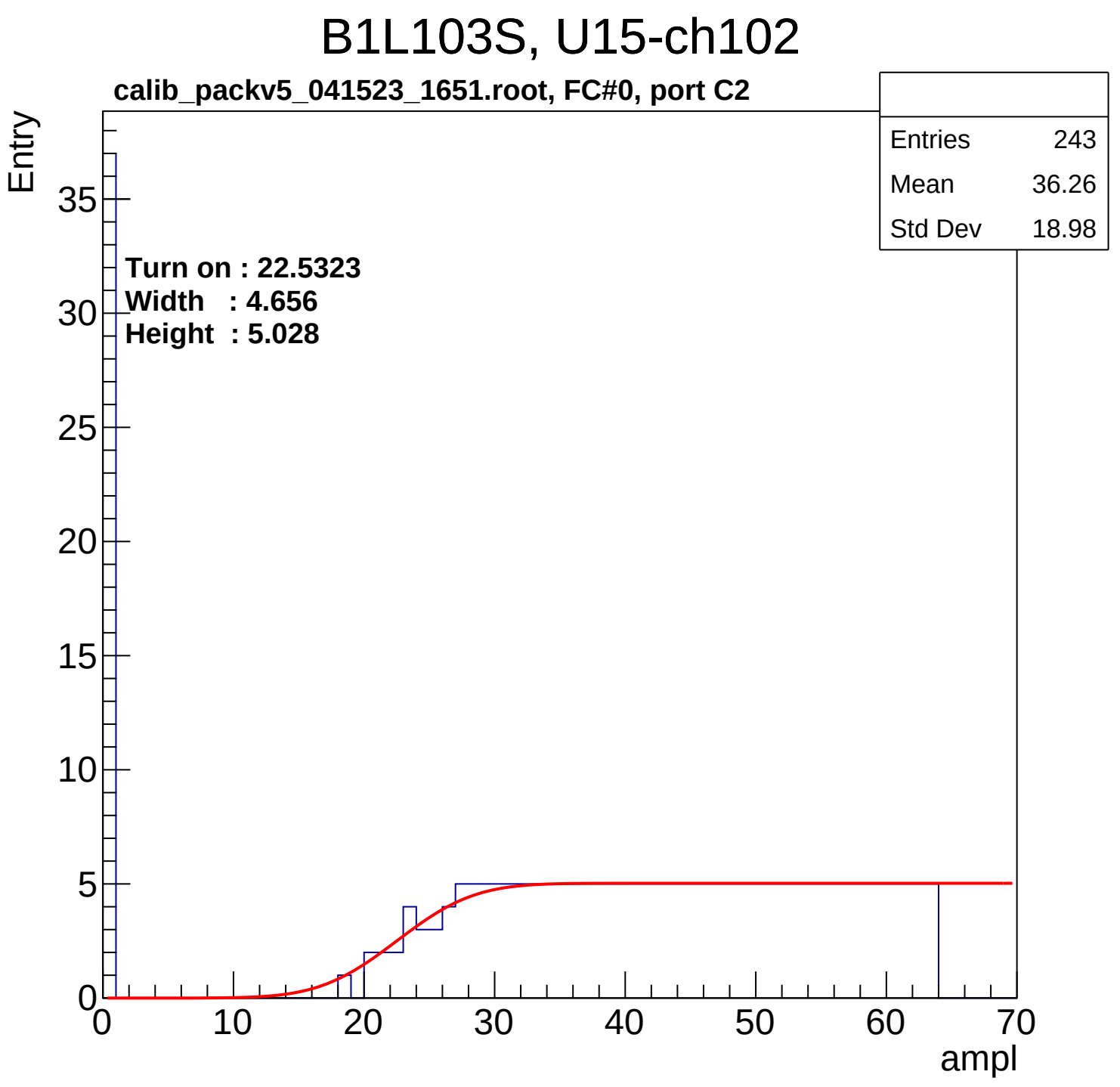
B1L103S, U15-ch102
calib_packv5_041523_1651.root, FC#0, port C2
Entries 243
Mean 36.26
Std Dev 18.98
Turn on : 22.5323
Width : 4.656
Height : 5.028
Entry
ampl
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10
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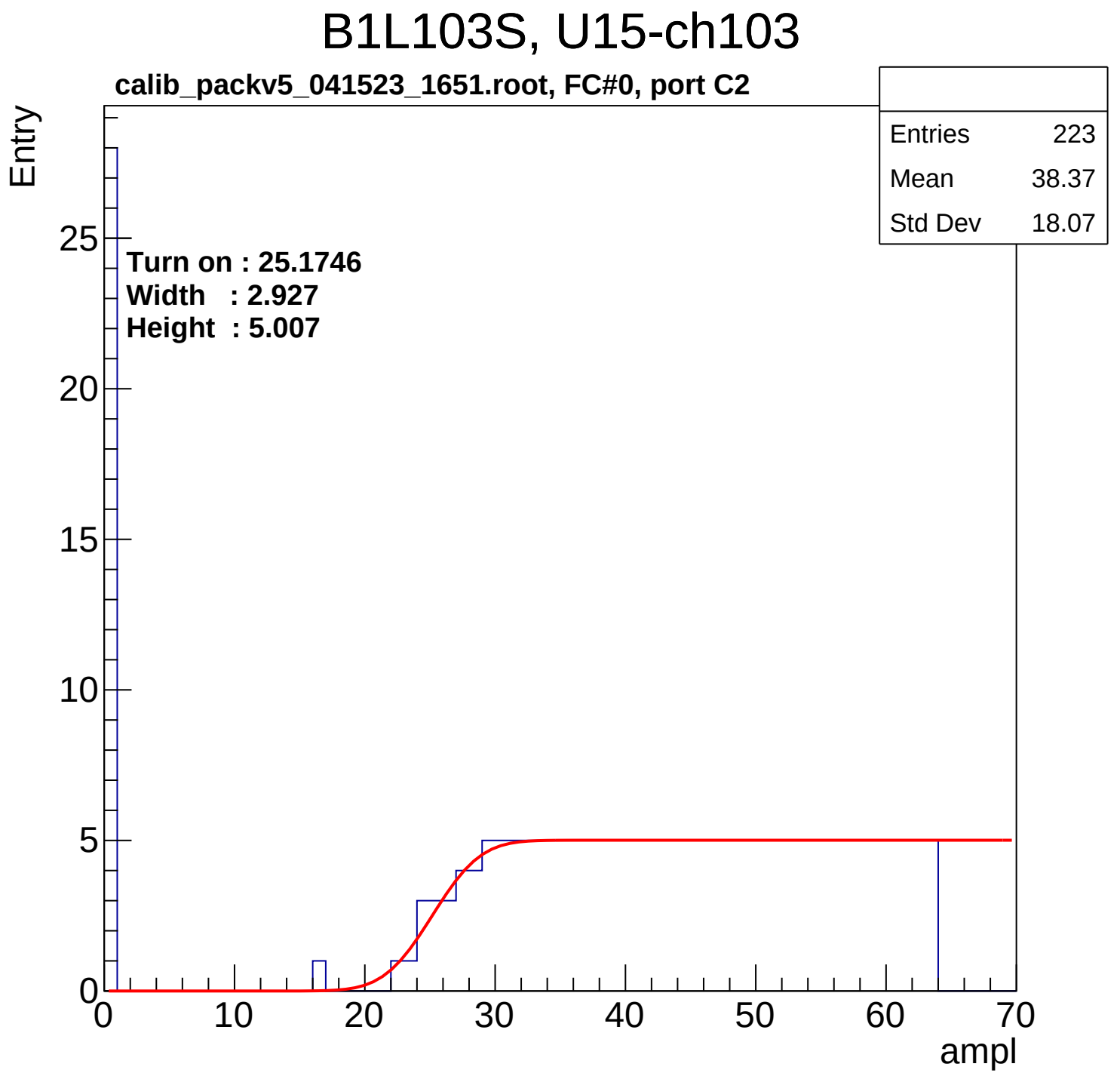
B1L103S, U15-ch103
calib_packv5_041523_1651.root, FC#0, port C2
Entries 223
Mean 38.37
Std Dev 18.07
Turn on : 25.1746
Width : 2.927
Height : 5.007
Entry
ampl
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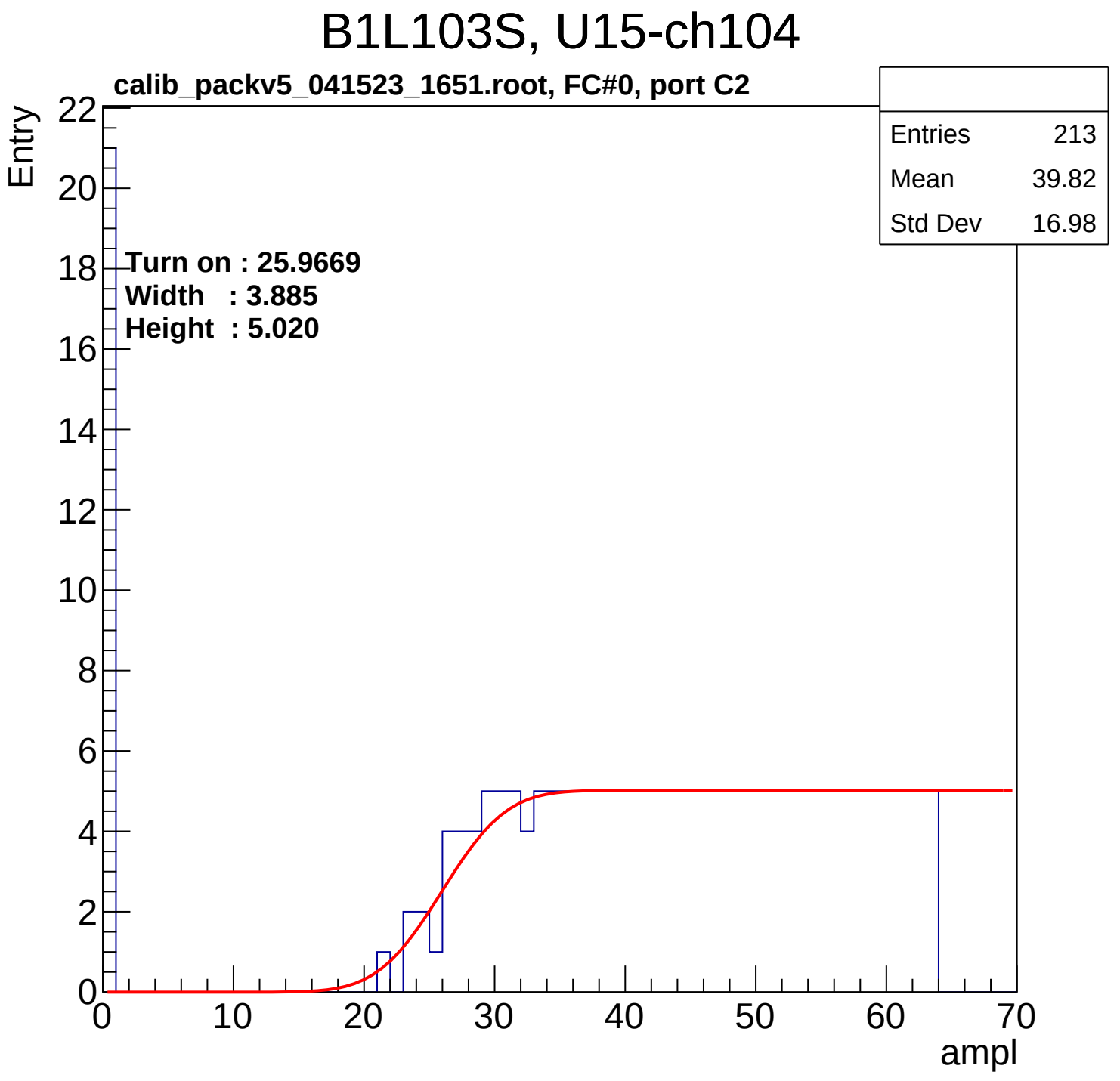
B1L103S, U15-ch104
calib_packv5_041523_1651.root, FC#0, port C2
Entries 213
Mean 39.82
Std Dev 16.98
Turn on : 25.9669
Width : 3.885
Height : 5.020
Entry
ampl
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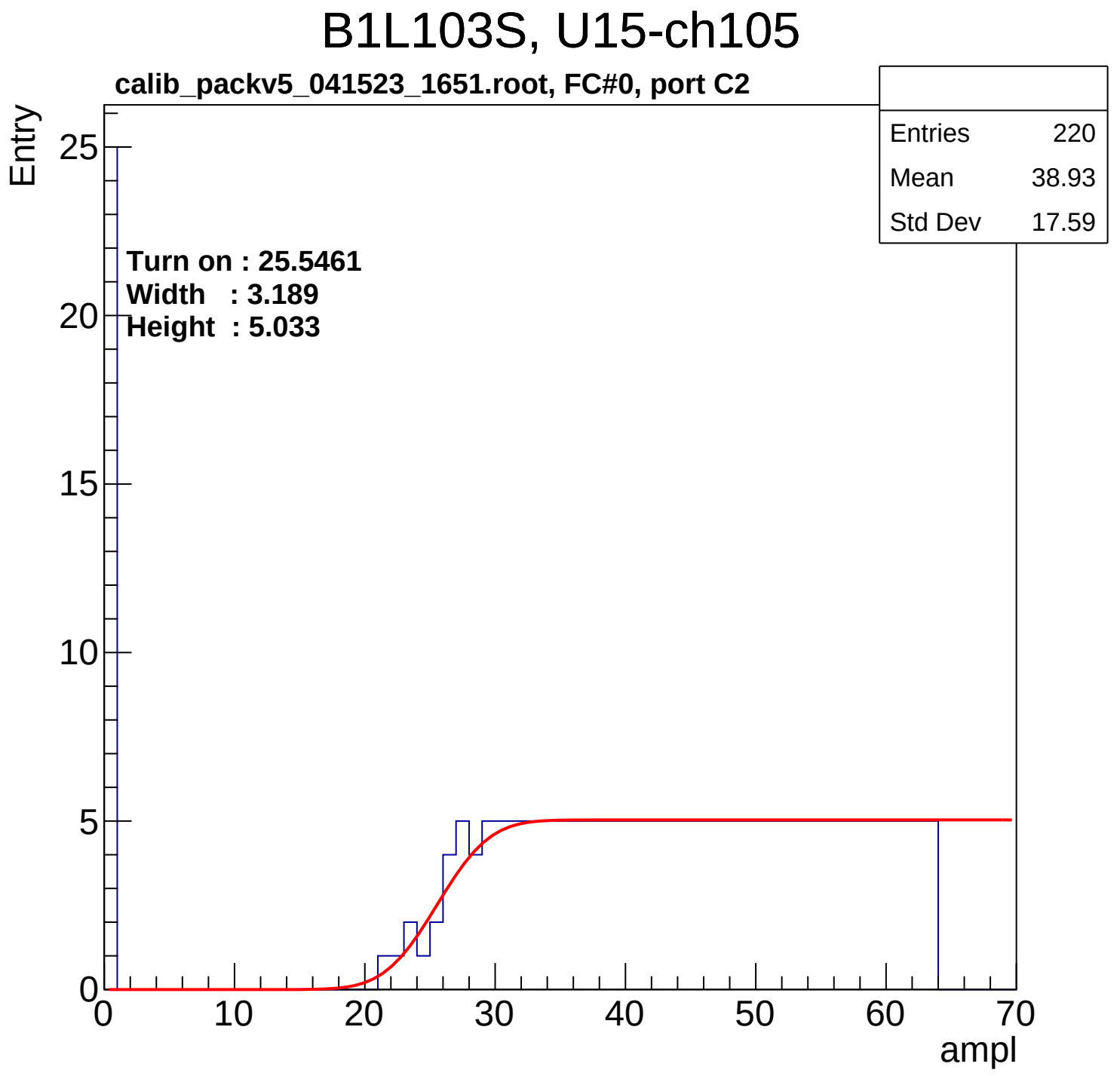
B1L103S, U15-ch105
calib_packv5_041523_1651.root, FC#0, port C2
Entries 220
Mean 38.93
Std Dev 17.59
Turn on : 25.5461
Width : 3.189
Height : 5.033
Entry
ampl
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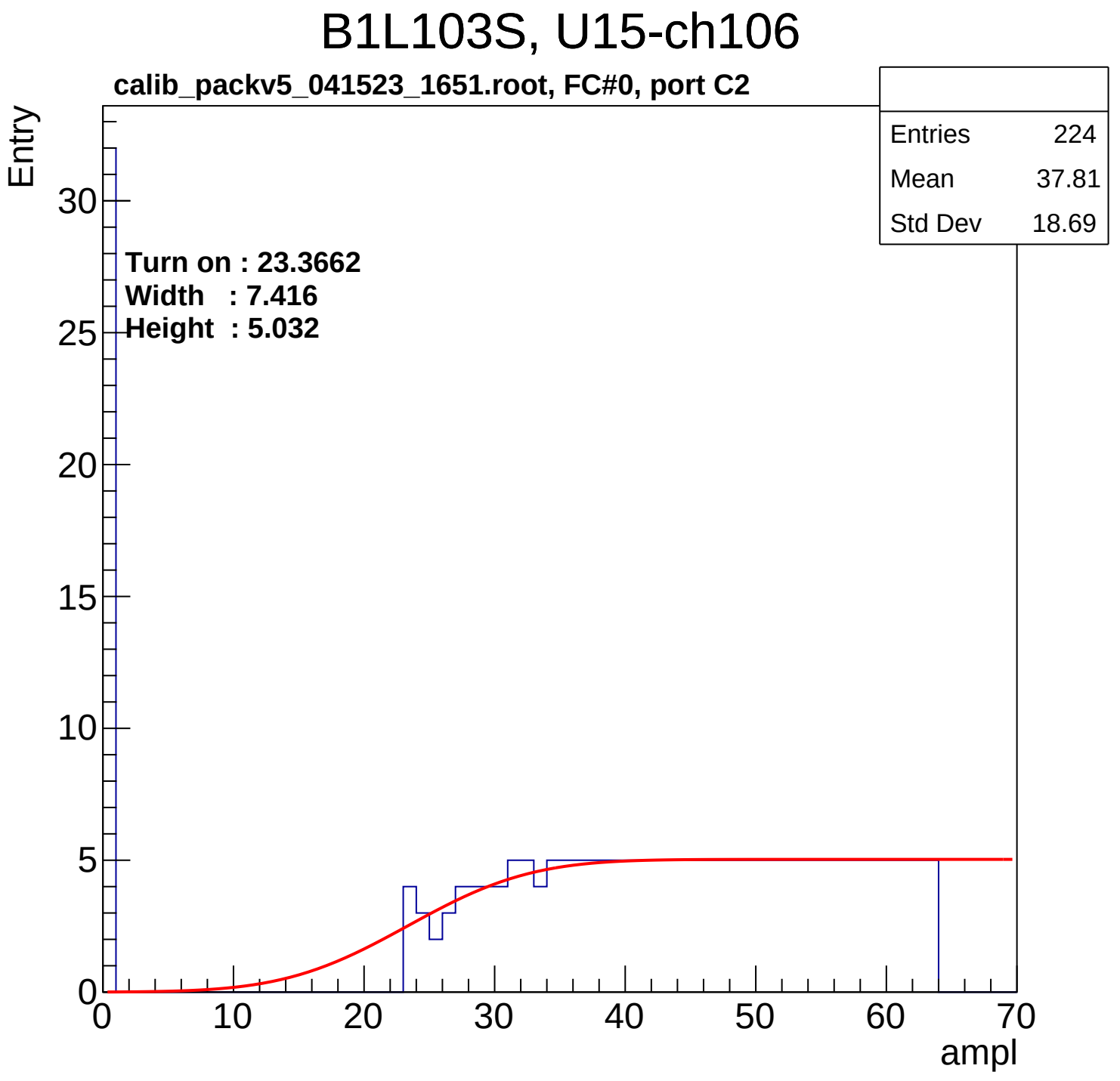
B1L103S, U15-ch106
calib_packv5_041523_1651.root, FC#0, port C2
Entries 224
Mean 37.81
Std Dev 18.69
Turn on : 23.3662
Width : 7.416
Height : 5.032
Entry
ampl
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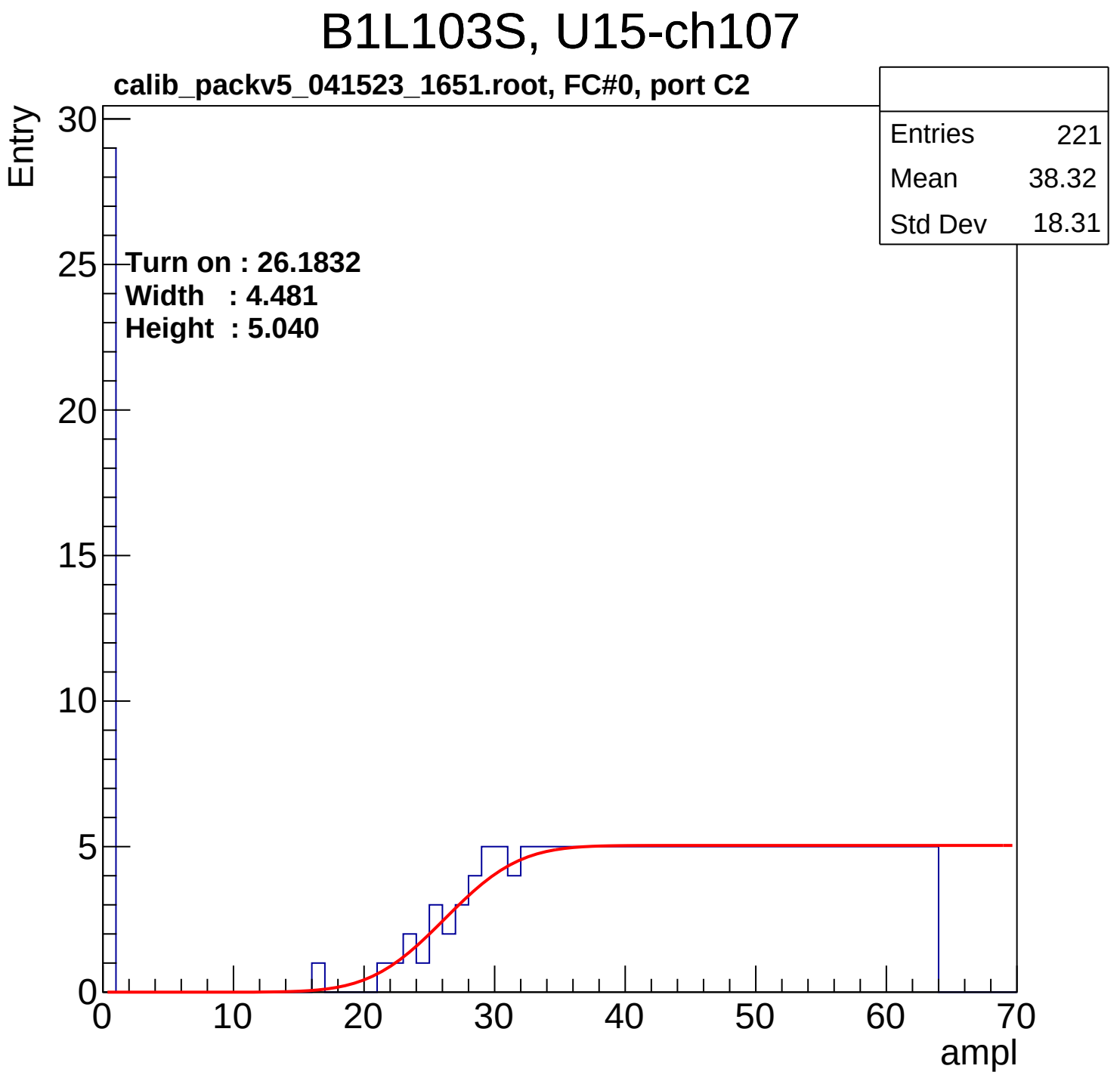
B1L103S, U15-ch107
calib_packv5_041523_1651.root, FC#0, port C2
Entries 221
Mean 38.32
Std Dev 18.31
Turn on : 26.1832
Width : 4.481
Height : 5.040
Entry
ampl
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15
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0
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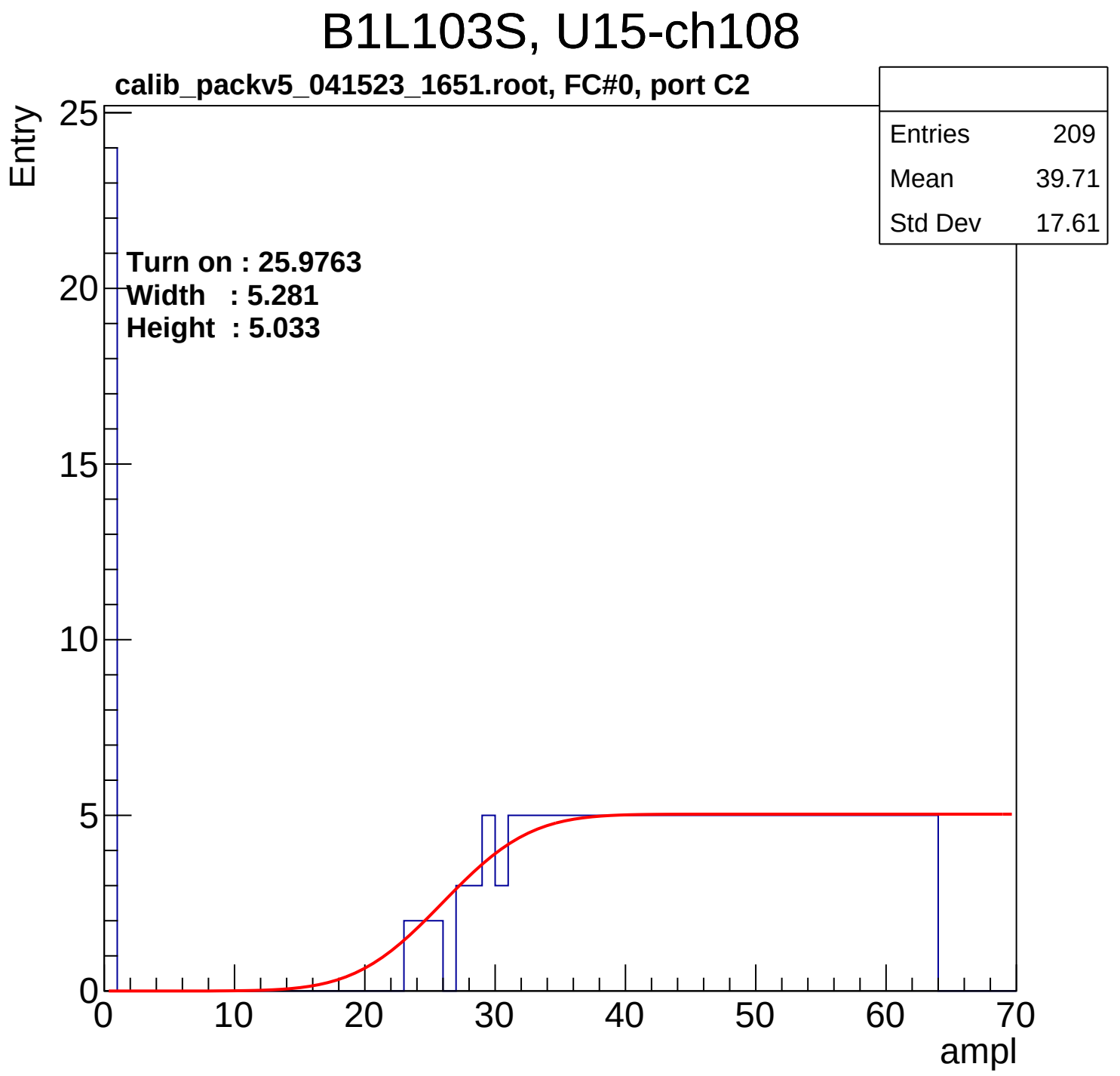
B1L103S, U15-ch108
calib_packv5_041523_1651.root, FC#0, port C2
Entries 209
Mean 39.71
Std Dev 17.61
Turn on : 25.9763
Width : 5.281
Height : 5.033
Entry
ampl
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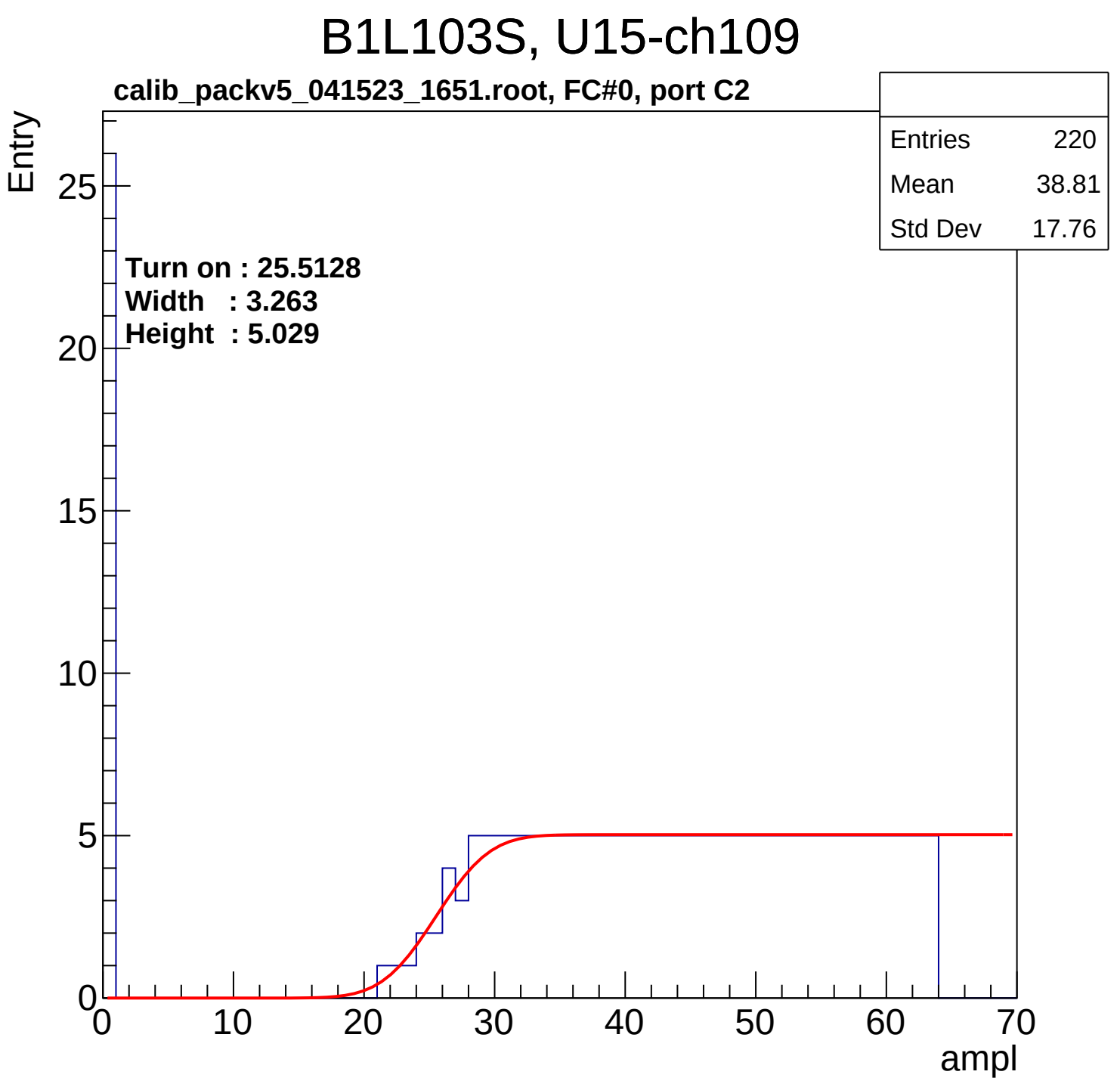
B1L103S, U15-ch109
calib_packv5_041523_1651.root, FC#0, port C2
Entries 220
Mean 38.81
Std Dev 17.76
Turn on : 25.5128
Width : 3.263
Height : 5.029
Entry
ampl
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10
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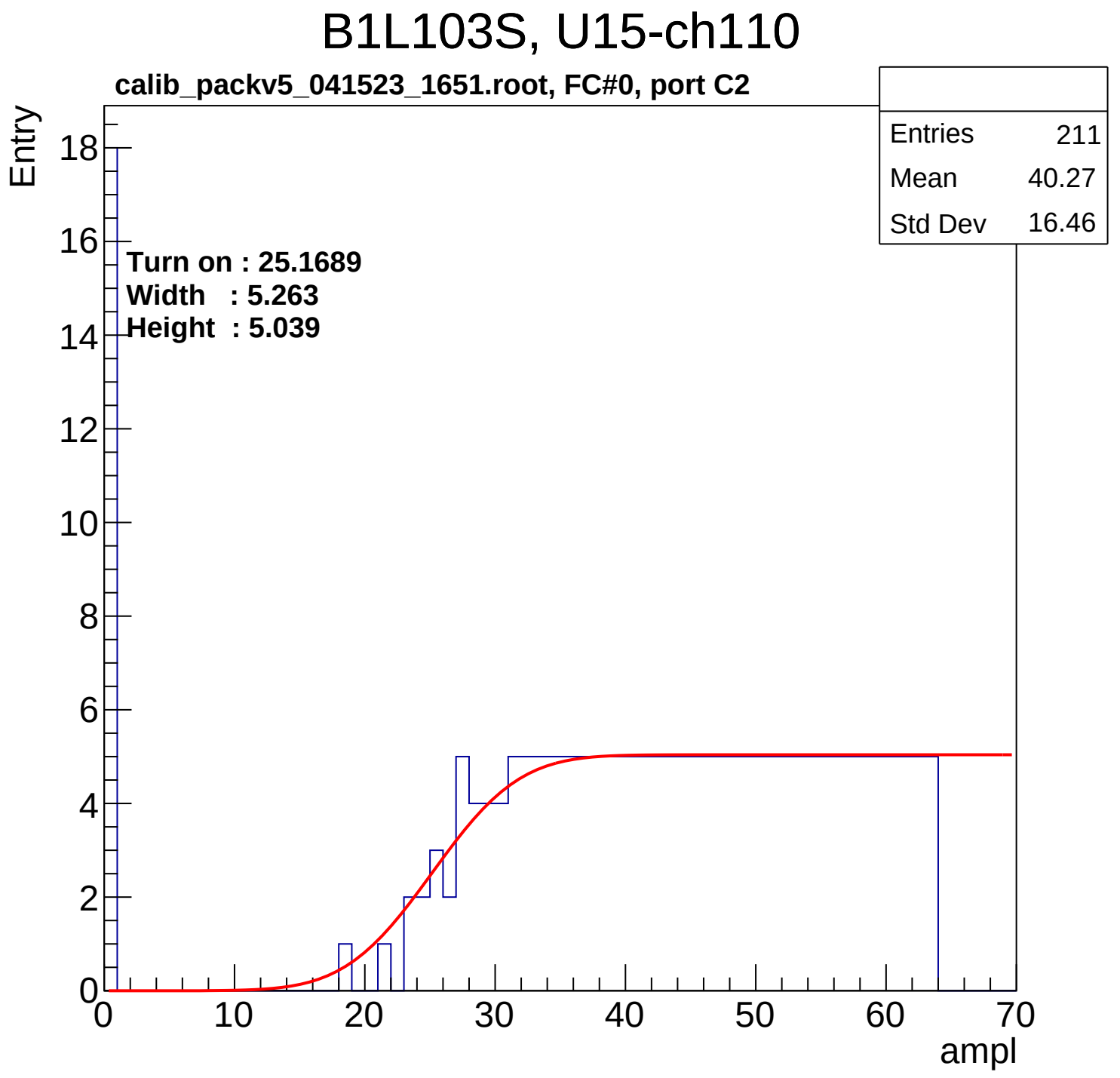
B1L103S, U15-ch110
calib_packv5_041523_1651.root, FC#0, port C2
Entries 211
Mean 40.27
Std Dev 16.46
Turn on : 25.1689
Width : 5.263
Height : 5.039
Entry
ampl
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6
8
10
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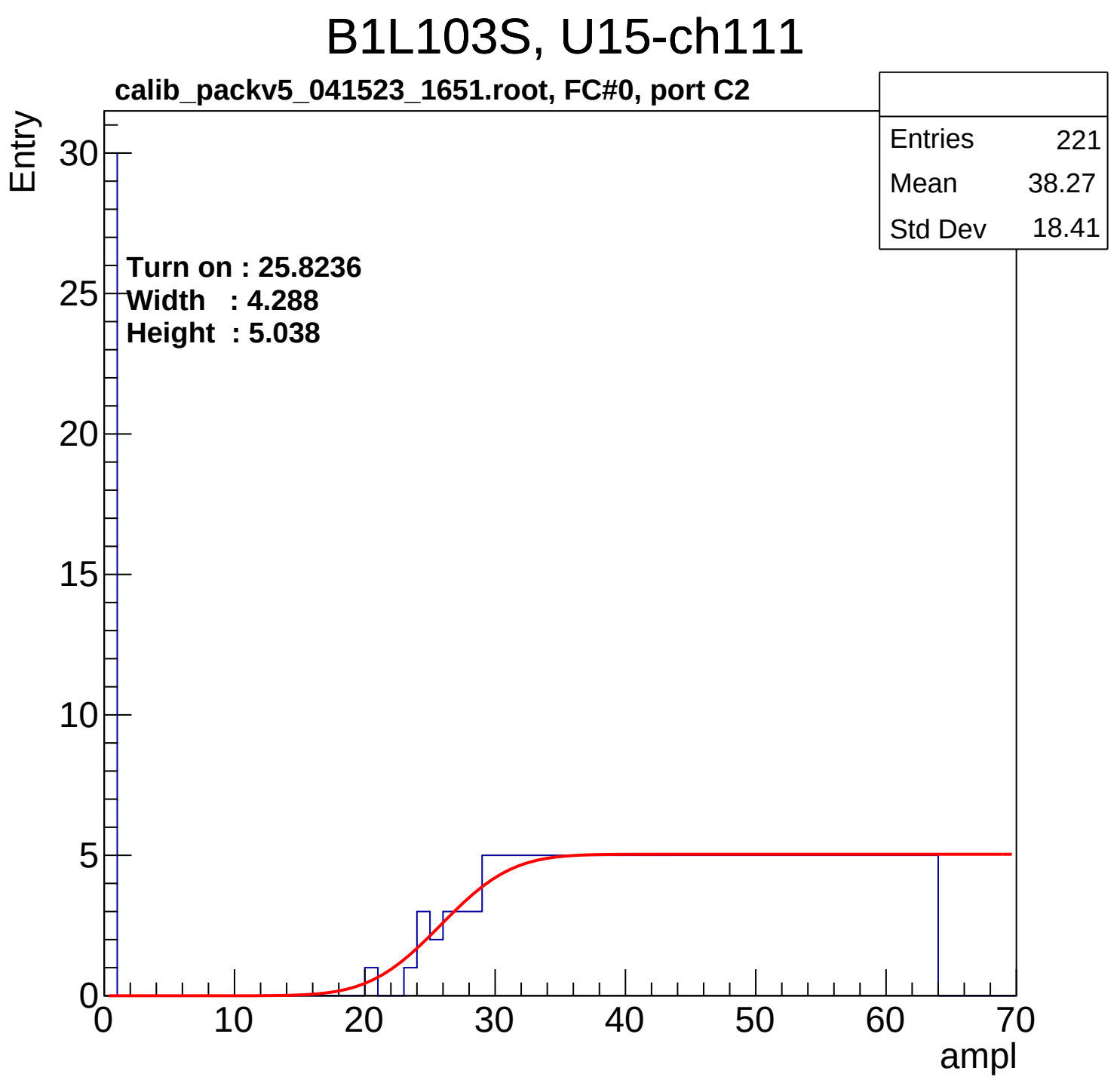
B1L103S, U15-ch111
calib_packv5_041523_1651.root, FC#0, port C2
Entries 221
Mean 38.27
Std Dev 18.41
Turn on : 25.8236
Width : 4.288
Height : 5.038
Entry
ampl
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10
15
20
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0
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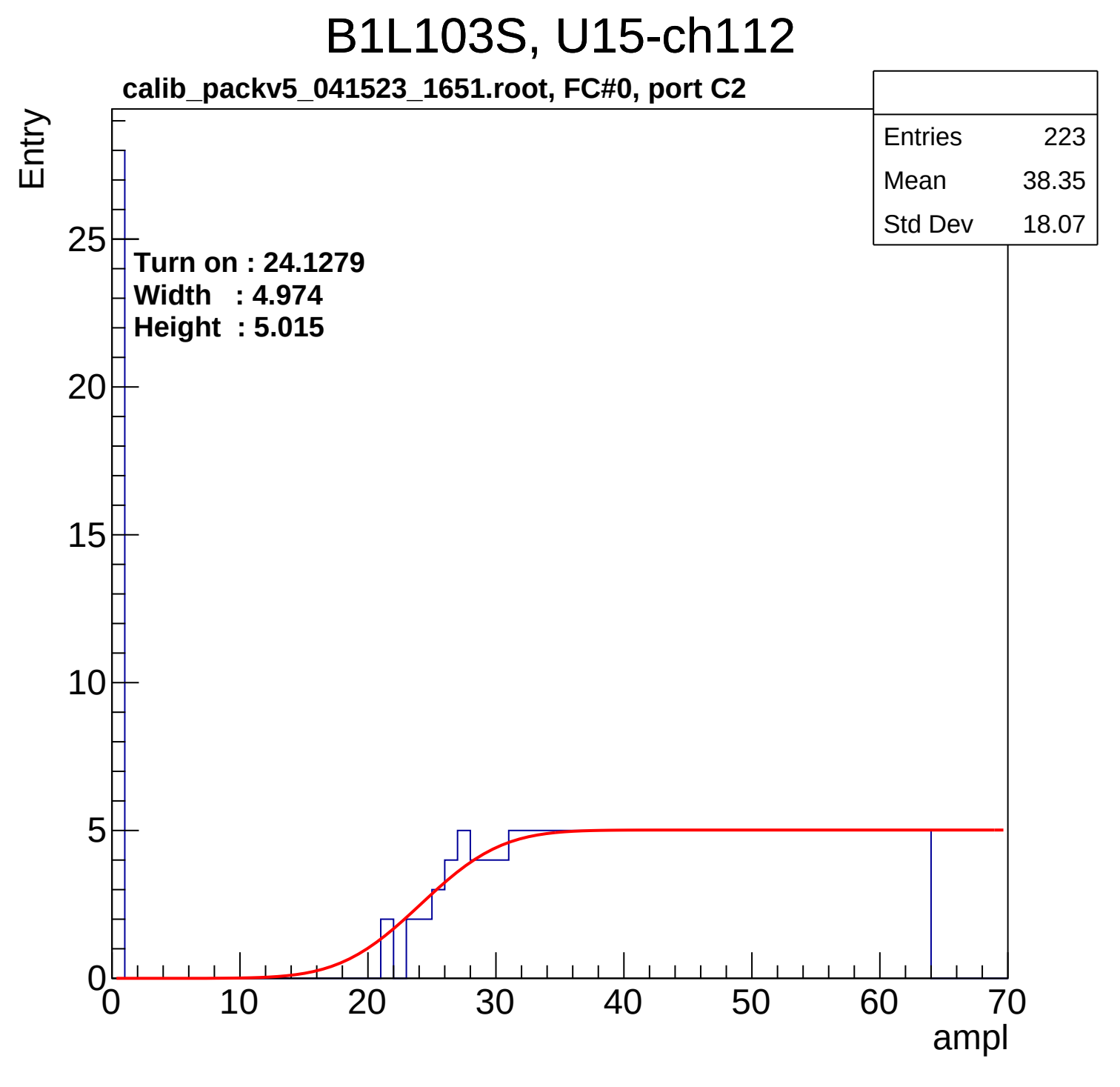
B1L103S, U15-ch112
calib_packv5_041523_1651.root, FC#0, port C2
Entries 223
Mean 38.35
Std Dev 18.07
Turn on : 24.1279
Width : 4.974
Height : 5.015
Entry
ampl
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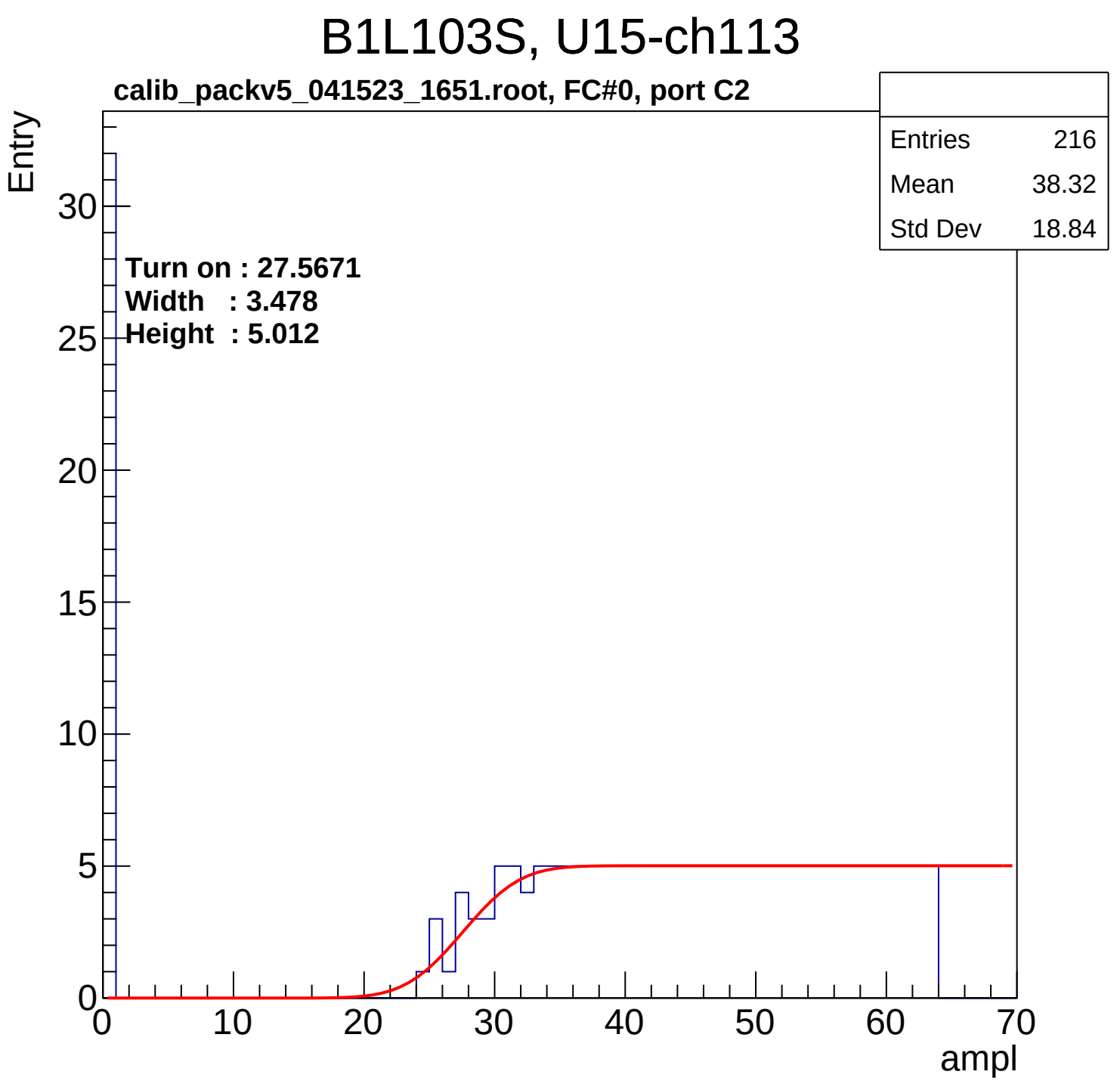
B1L103S, U15-ch113
calib_packv5_041523_1651.root, FC#0, port C2
Entries 216
Mean 38.32
Std Dev 18.84
Turn on : 27.5671
Width : 3.478
Height : 5.012
Entry
ampl
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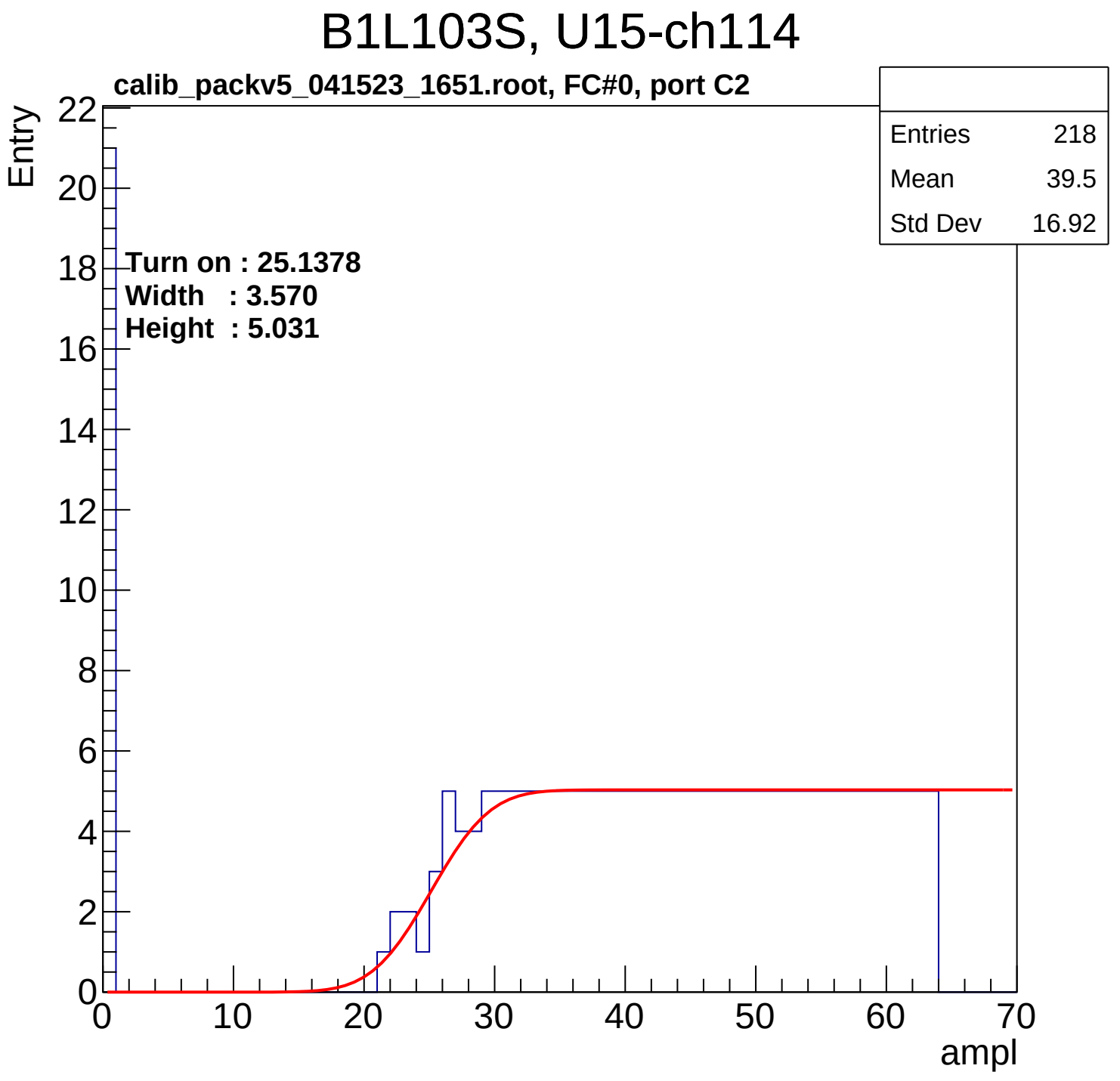
B1L103S, U15-ch114
calib_packv5_041523_1651.root, FC#0, port C2
Entries 218
Mean 39.5
Std Dev 16.92
Turn on : 25.1378
Width : 3.570
Height : 5.031
Entry
ampl
0
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4
6
8
10
12
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18
20
22
0
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20
30
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50
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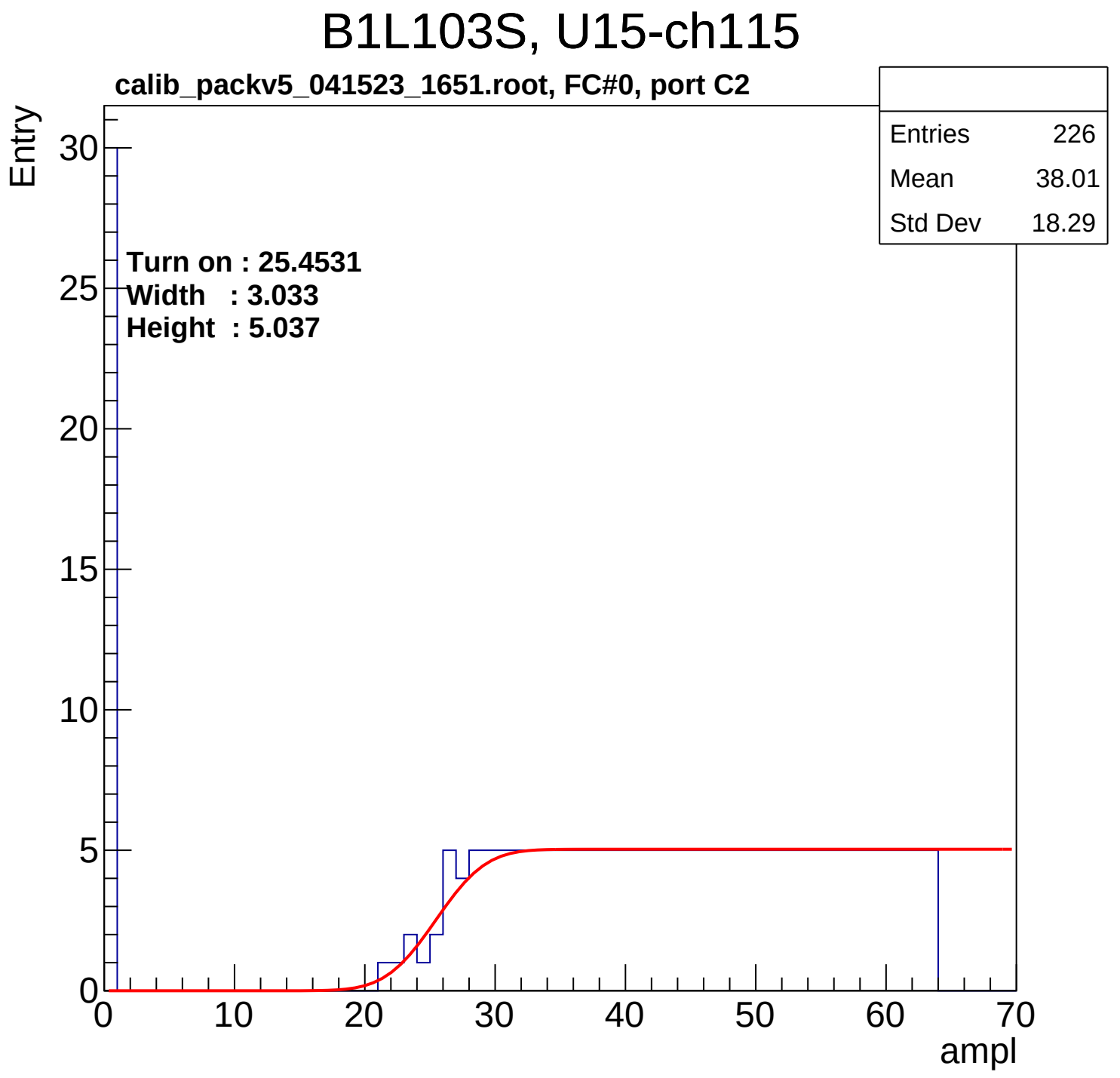
B1L103S, U15-ch115
calib_packv5_041523_1651.root, FC#0, port C2
Entries 226
Mean 38.01
Std Dev 18.29
Turn on : 25.4531
Width : 3.033
Height : 5.037
Entry
ampl
0
5
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15
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25
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0
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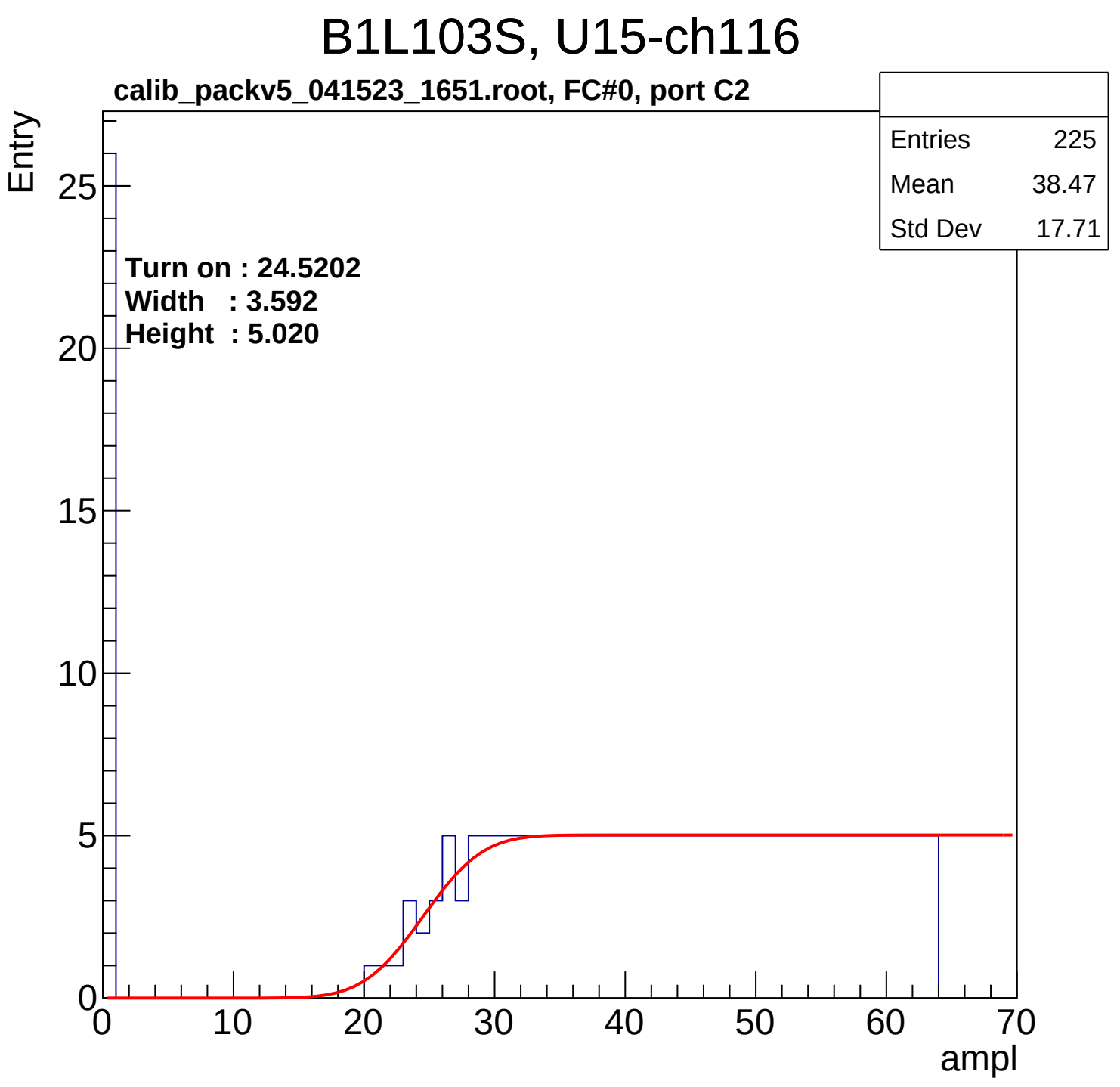
B1L103S, U15-ch116
calib_packv5_041523_1651.root, FC#0, port C2
Entries 225
Mean 38.47
Std Dev 17.71
Turn on : 24.5202
Width : 3.592
Height : 5.020
Entry
ampl
0
5
10
15
20
25
0
10
20
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40
50
60
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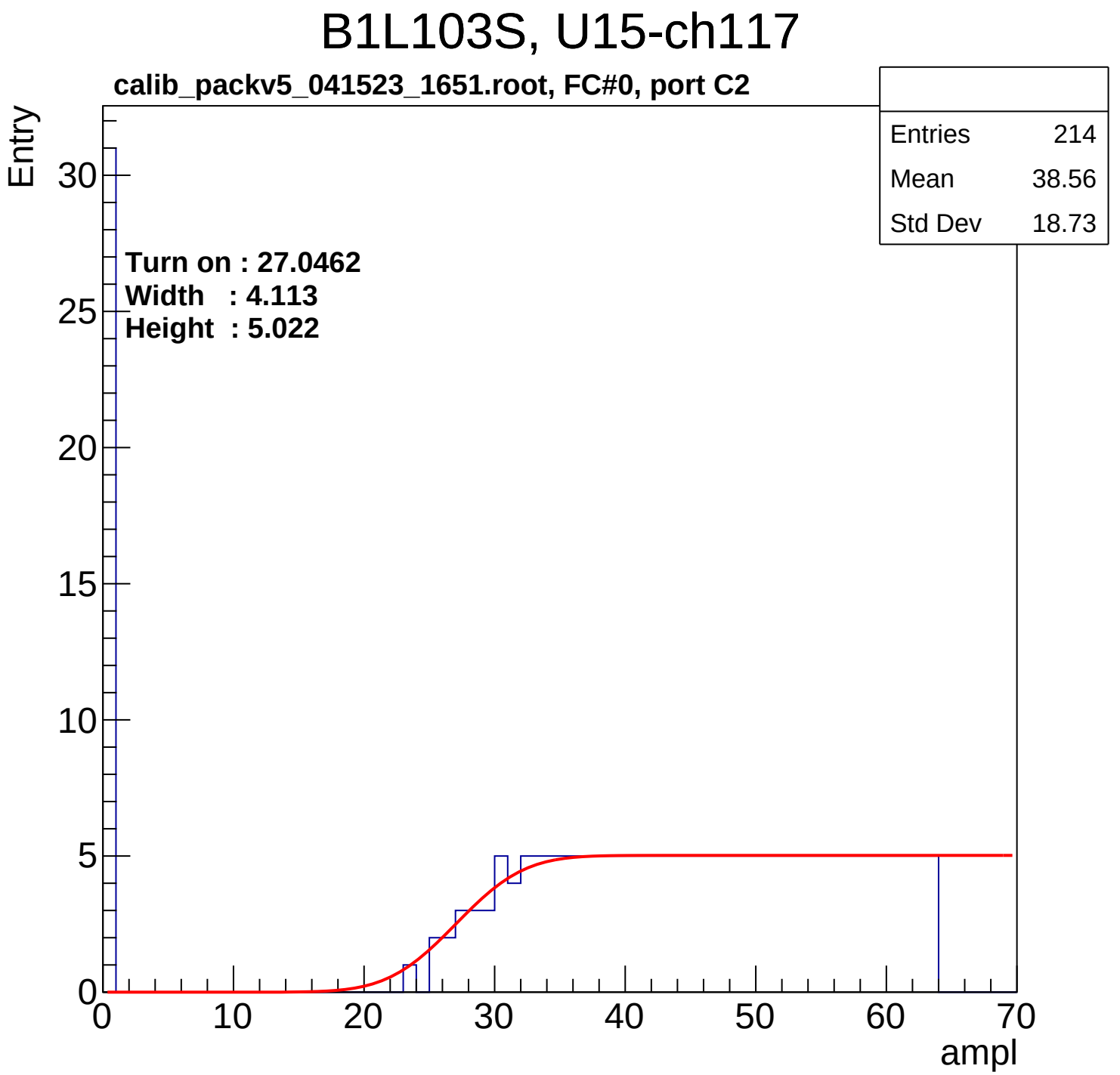
B1L103S, U15-ch117
calib_packv5_041523_1651.root, FC#0, port C2
Entries 214
Mean 38.56
Std Dev 18.73
Turn on : 27.0462
Width : 4.113
Height : 5.022
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
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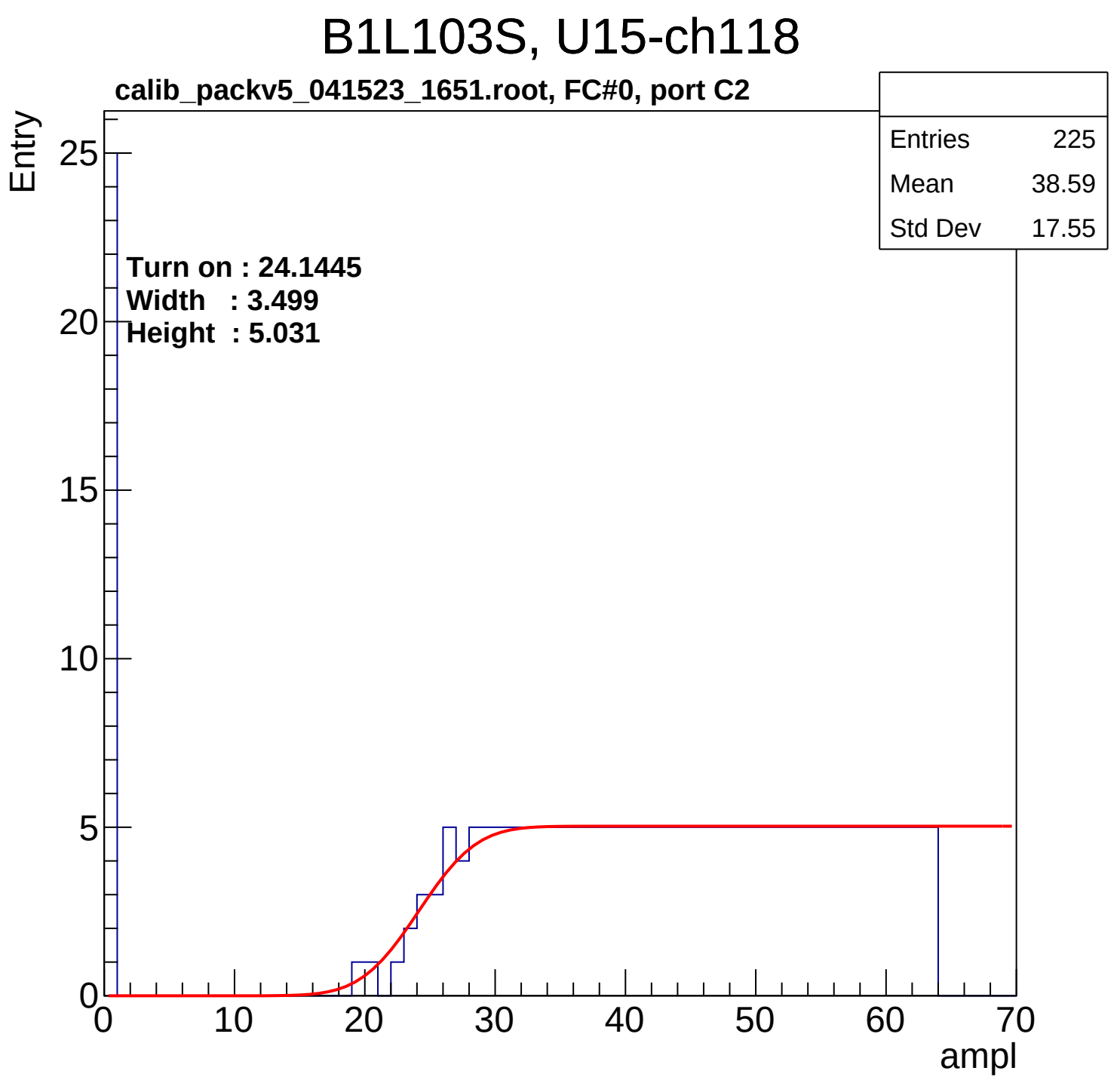
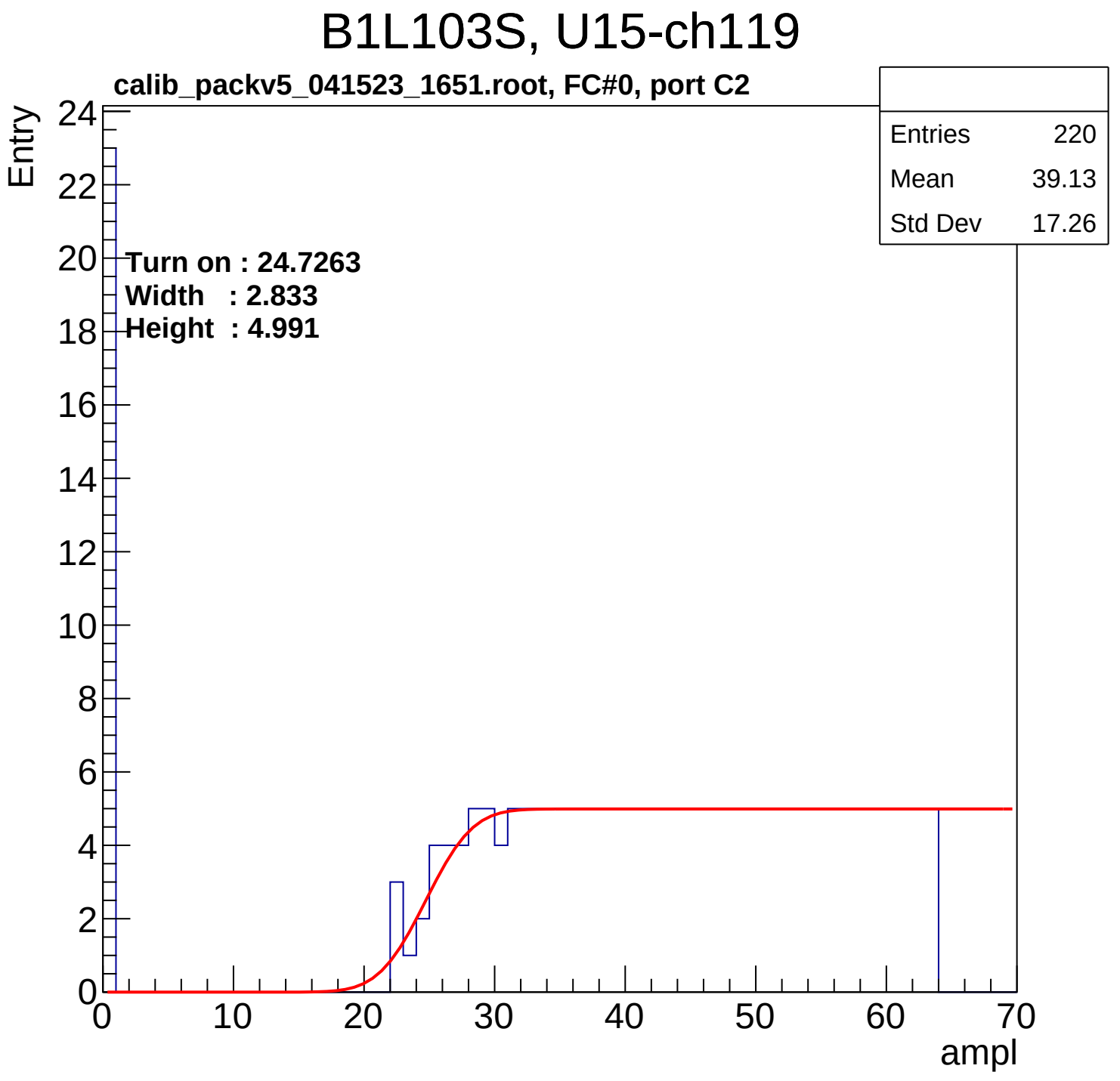

B1L103S, U15-ch118
calib_packv5_041523_1651.root, FC#0, port C2
Entries 225
Mean 38.59
Std Dev 17.55
Turn on : 24.1445
Width : 3.499
Height : 5.031
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U15-ch119
calib_packv5_041523_1651.root, FC#0, port C2
Entries 220
Mean 39.13
Std Dev 17.26
Turn on : 24.7263
Width : 2.833
Height : 4.991
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
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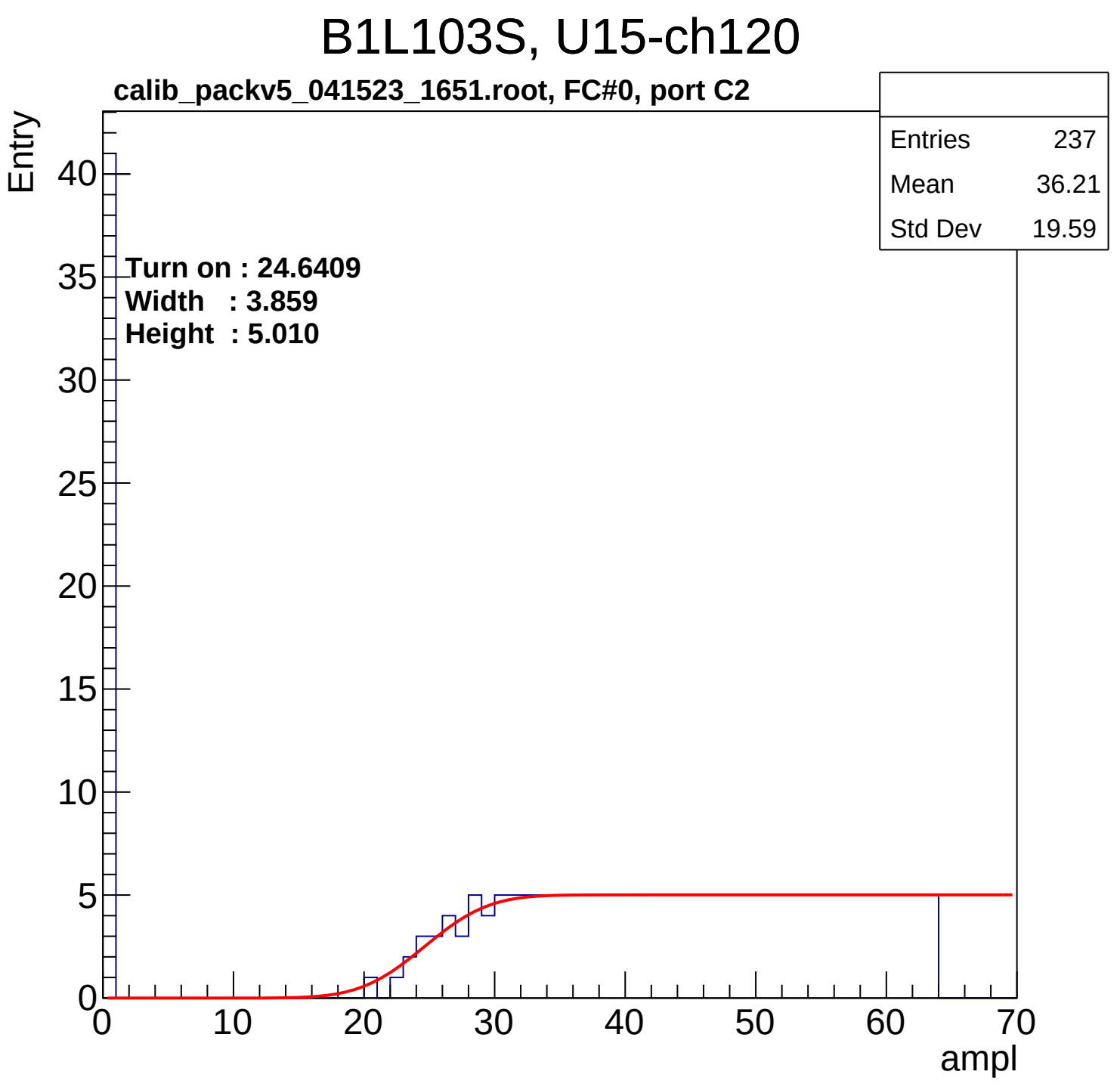
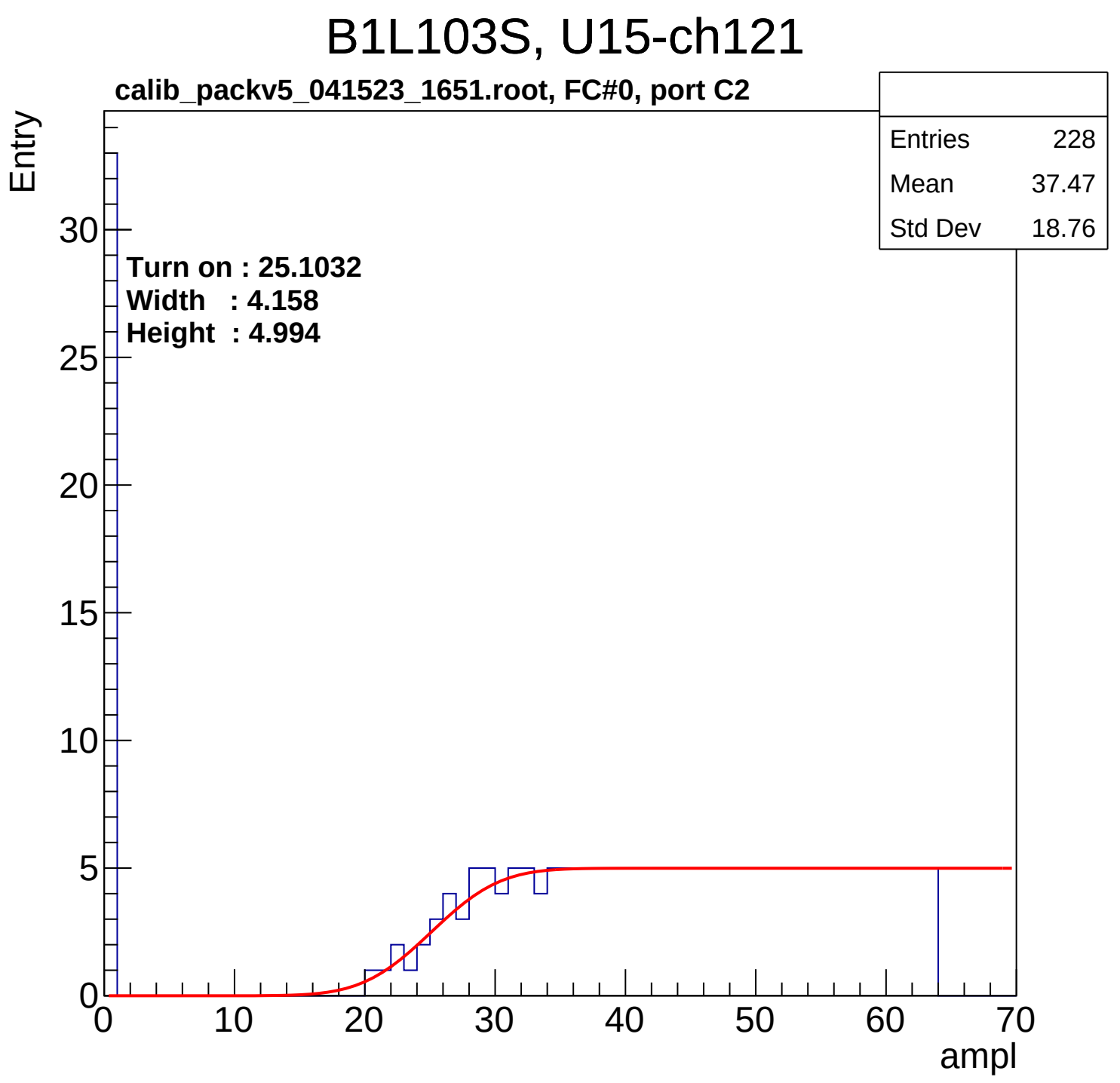
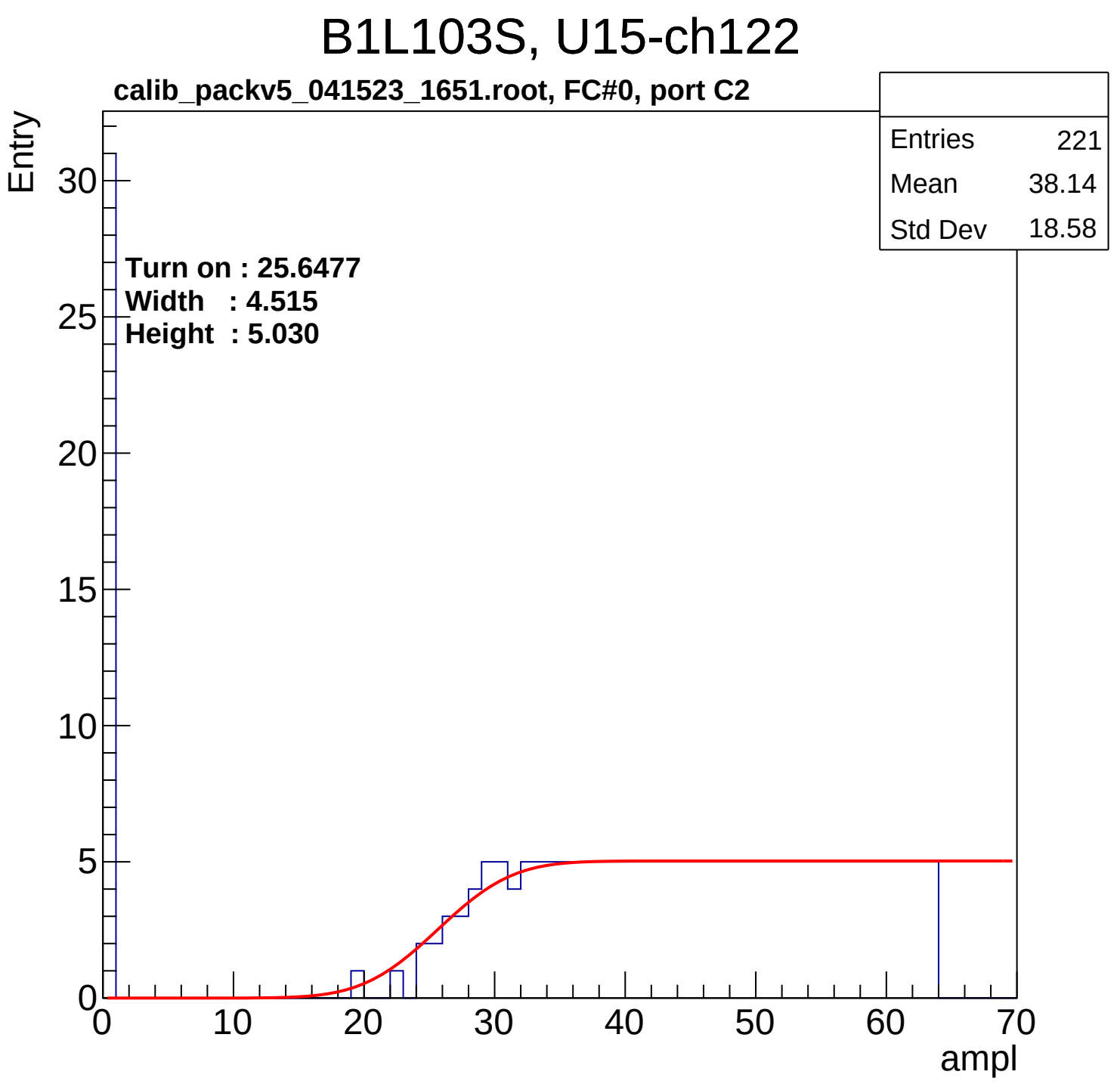
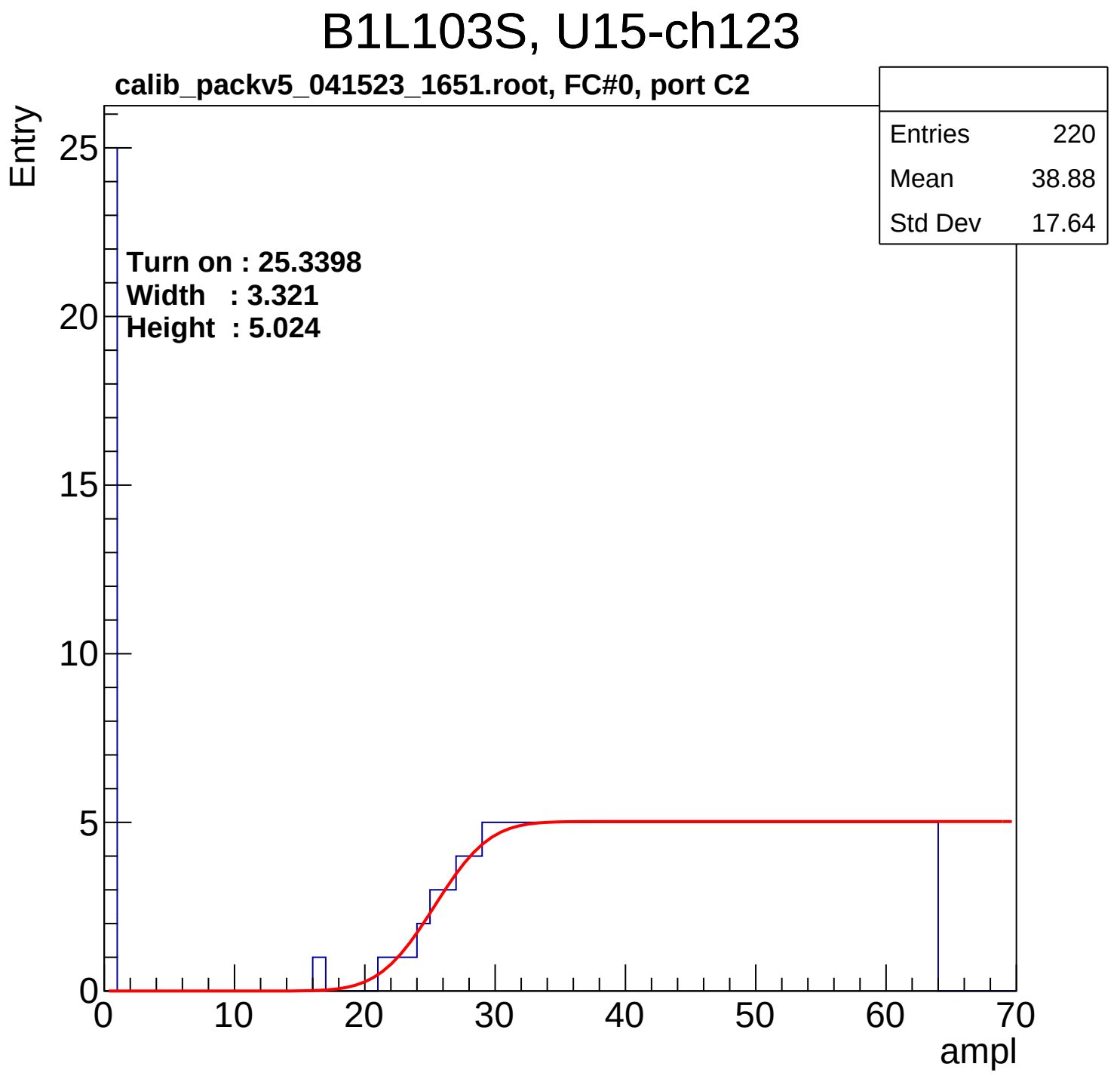
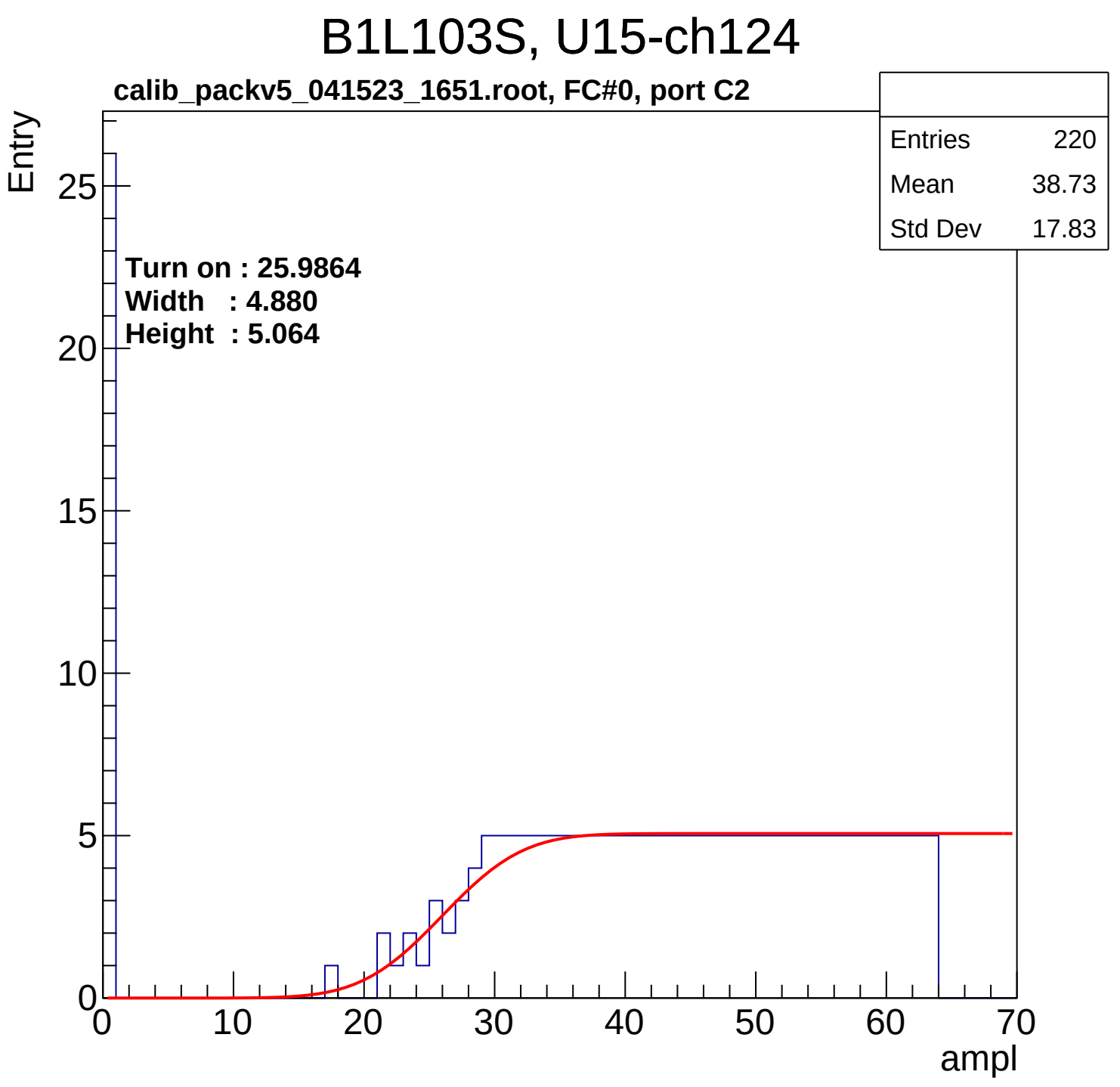
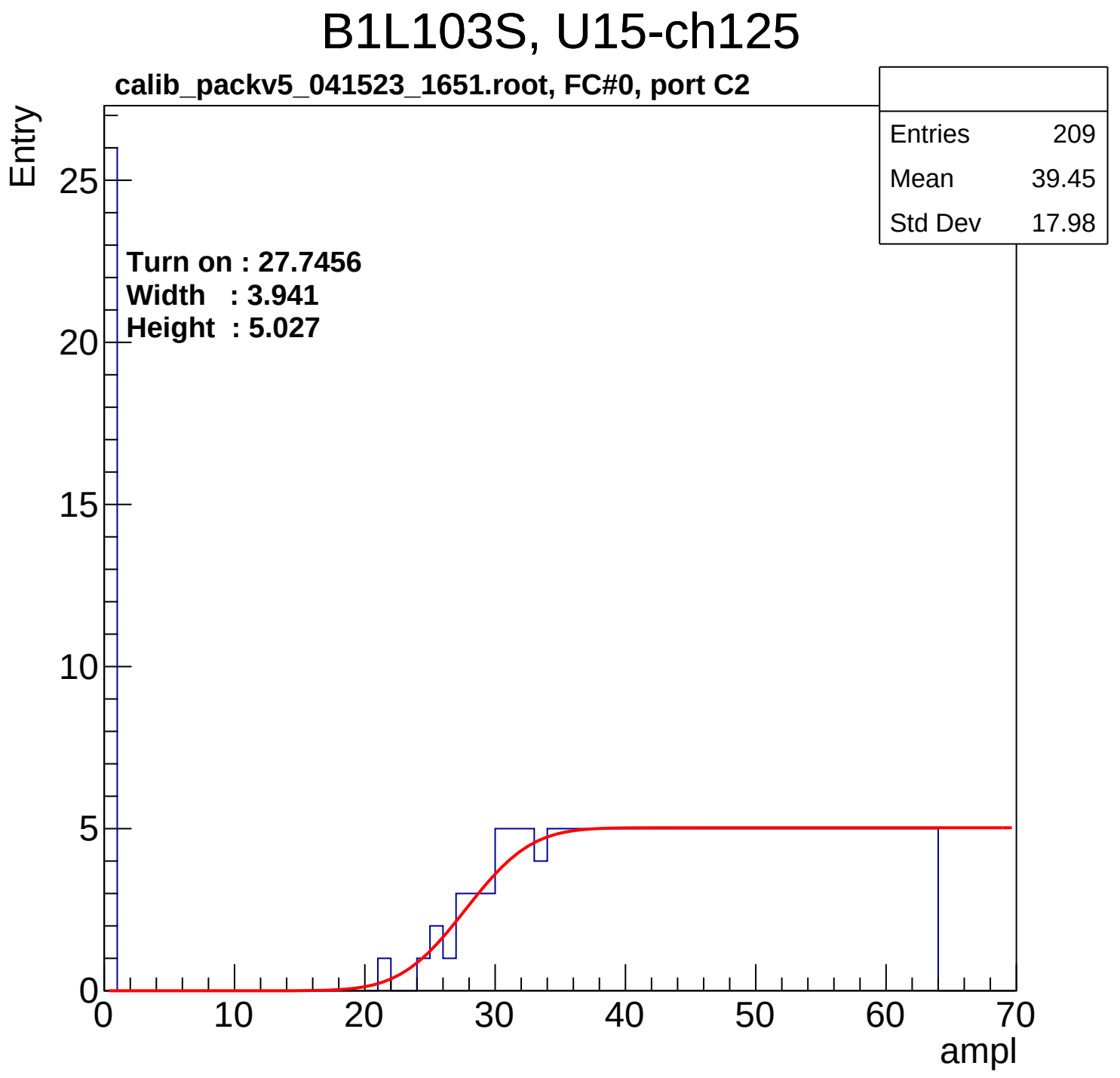

B1L103S, U15-ch120
calib_packv5_041523_1651.root, FC#0, port C2
Entries 237
Mean 36.21
Std Dev 19.59
Turn on : 24.6409
Width : 3.859
Height : 5.010
Entry
ampl
0
5
10
15
20
25
30
35
40
0
10
20
30
40
50
60
70

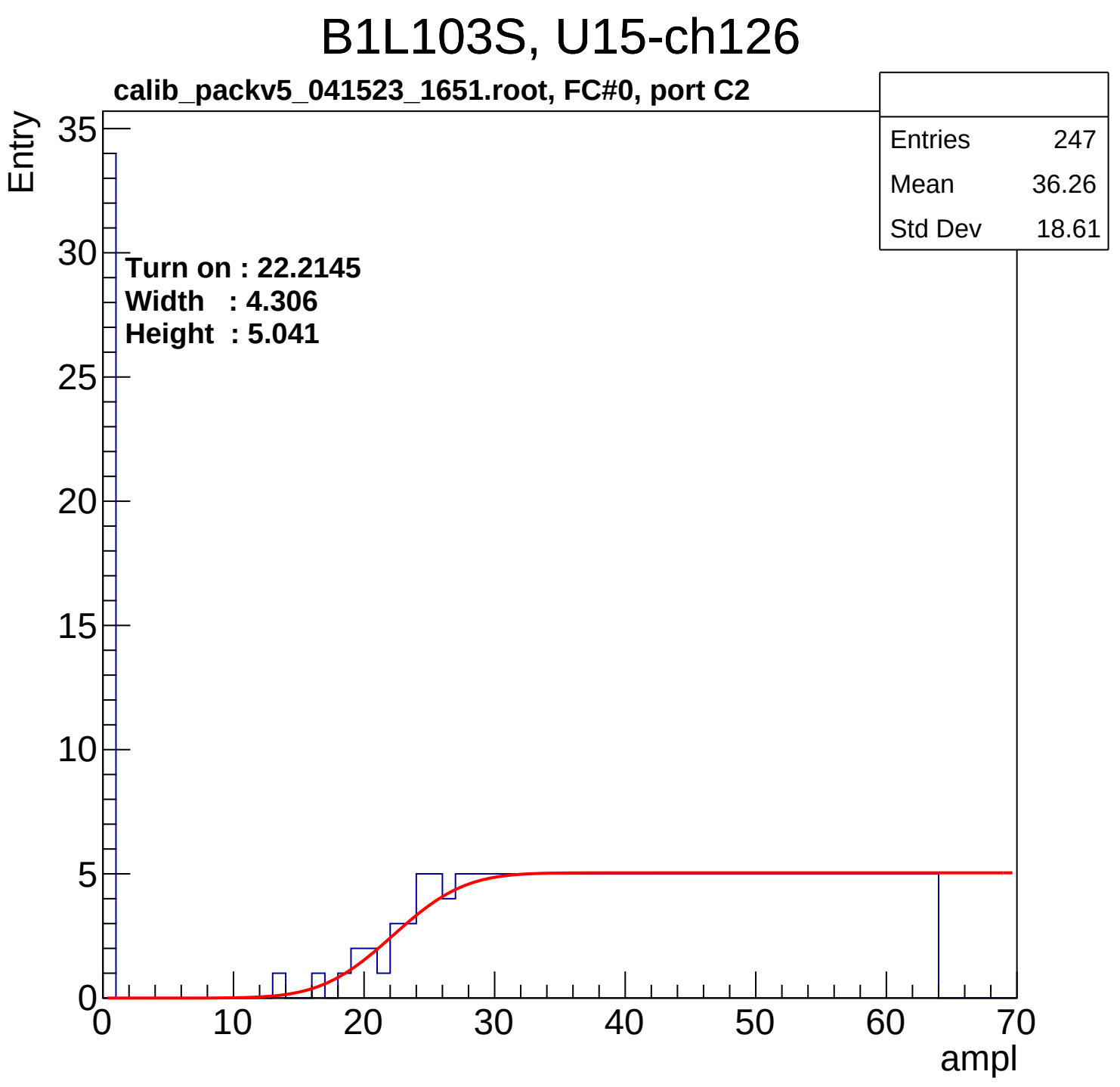

B1L103S, U15-ch121
calib_packv5_041523_1651.root, FC#0, port C2
Entries 228
Mean 37.47
Std Dev 18.76
Turn on : 25.1032
Width : 4.158
Height : 4.994
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70


B1L103S, U15-ch122
calib_packv5_041523_1651.root, FC#0, port C2
Entries 221
Mean 38.14
Std Dev 18.58
Turn on : 25.6477
Width : 4.515
Height : 5.030
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch123
calib_packv5_041523_1651.root, FC#0, port C2
Entries 220
Mean 38.88
Std Dev 17.64
Turn on : 25.3398
Width : 3.321
Height : 5.024
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U15-ch124
calib_packv5_041523_1651.root, FC#0, port C2
Entries 220
Mean 38.73
Std Dev 17.83
Turn on : 25.9864
Width : 4.880
Height : 5.064
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U15-ch125
calib_packv5_041523_1651.root, FC#0, port C2
Entries 209
Mean 39.45
Std Dev 17.98
Turn on : 27.7456
Width : 3.941
Height : 5.027
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U15-ch126
calib_packv5_041523_1651.root, FC#0, port C2
Entries 247
Mean 36.26
Std Dev 18.61
Turn on : 22.2145
Width : 4.306
Height : 5.041
Entry
ampl
0
5
10
15
20
25
30
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0
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20
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40
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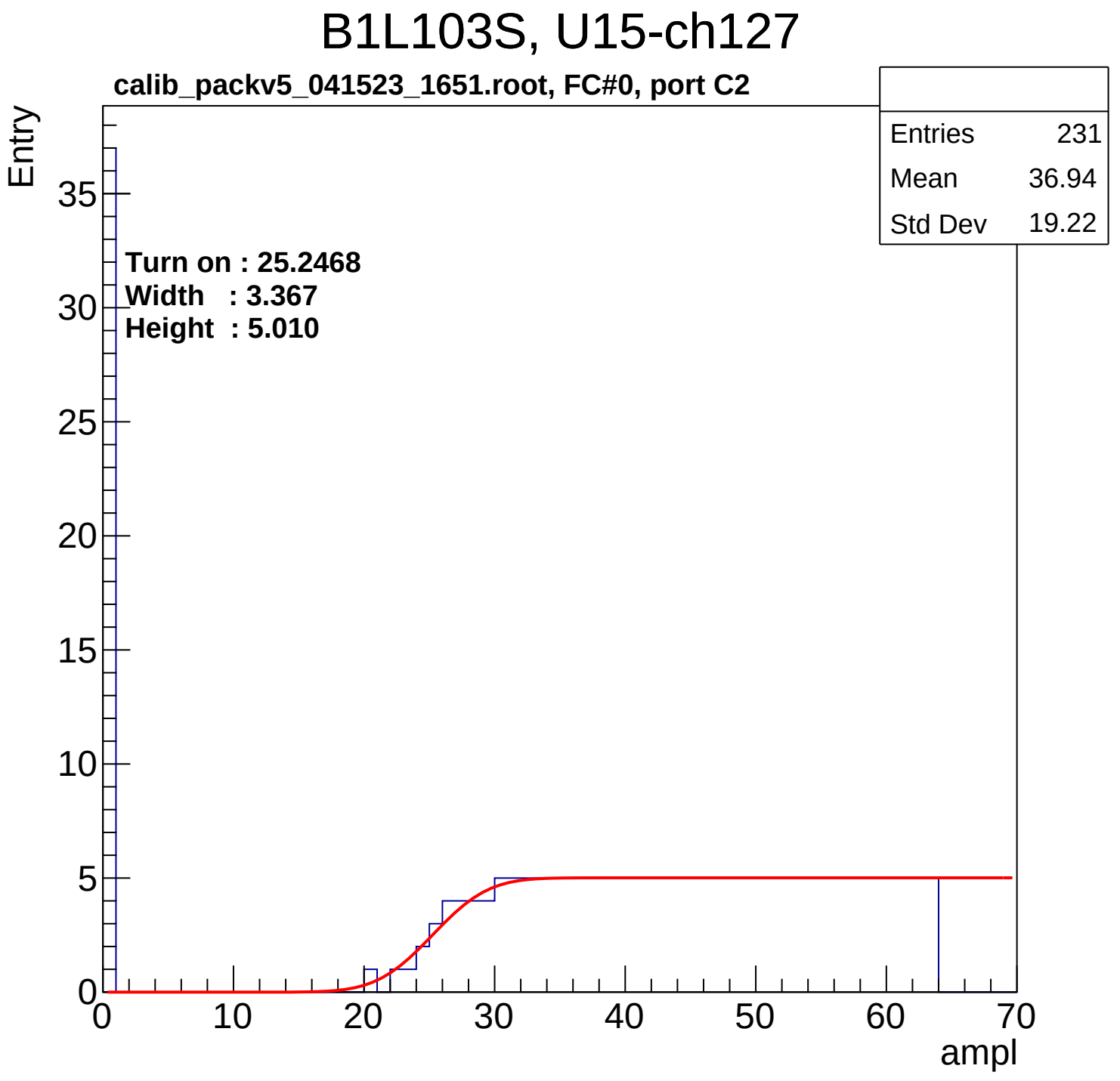
60
70


B1L103S, U15-ch127
calib_packv5_041523_1651.root, FC#0, port C2
Entries 231
Mean 36.94
Std Dev 19.22
Turn on : 25.2468
Width : 3.367
Height : 5.010
Entry
ampl
0
5
10
15
20
25
30
35
0
10
20
30
40
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60
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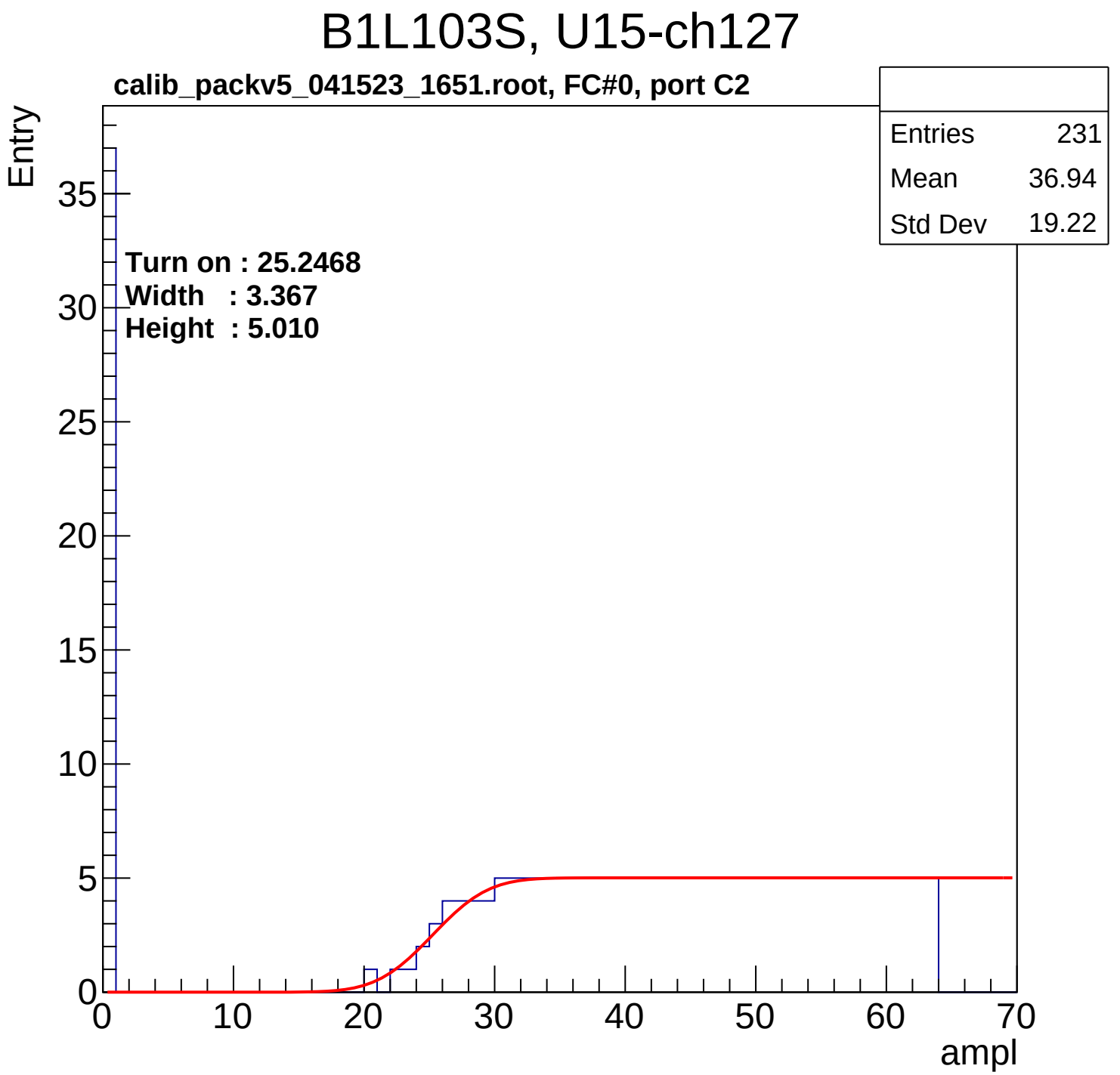
B1L103S, U15-ch127
calib_packv5_041523_1651.root, FC#0, port C2
Entries 231
Mean 36.94
Std Dev 19.22
Turn on : 25.2468
Width : 3.367
Height : 5.010
Entry
ampl
0
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70