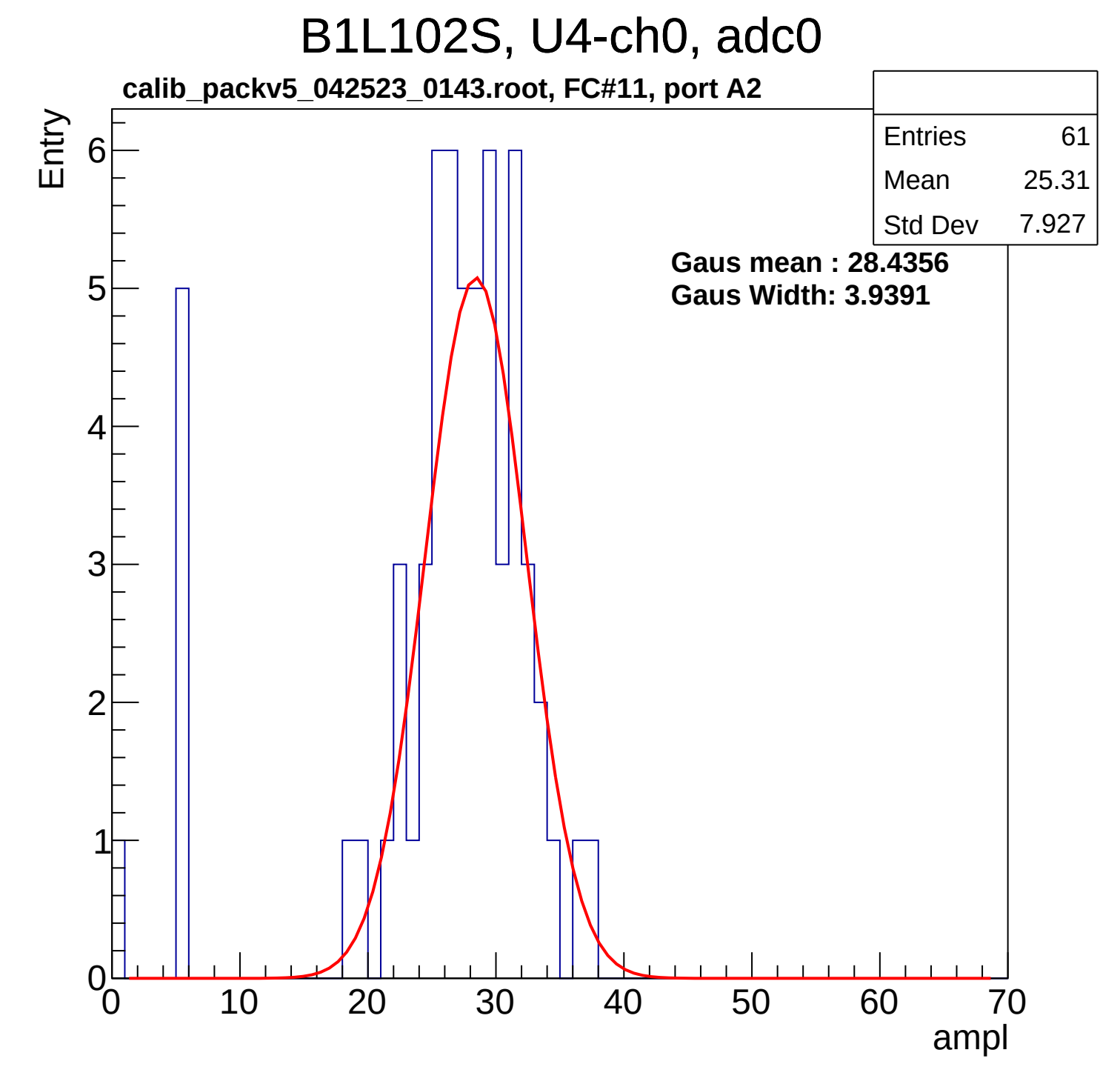
B1L102S, U4-ch0, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 25.31
Std Dev 7.927
Gaus mean : 28.4356
Gaus Width: 3.9391
Entry
ampl
0
1
2
3
4
5
6
0
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20
30
40
50
60
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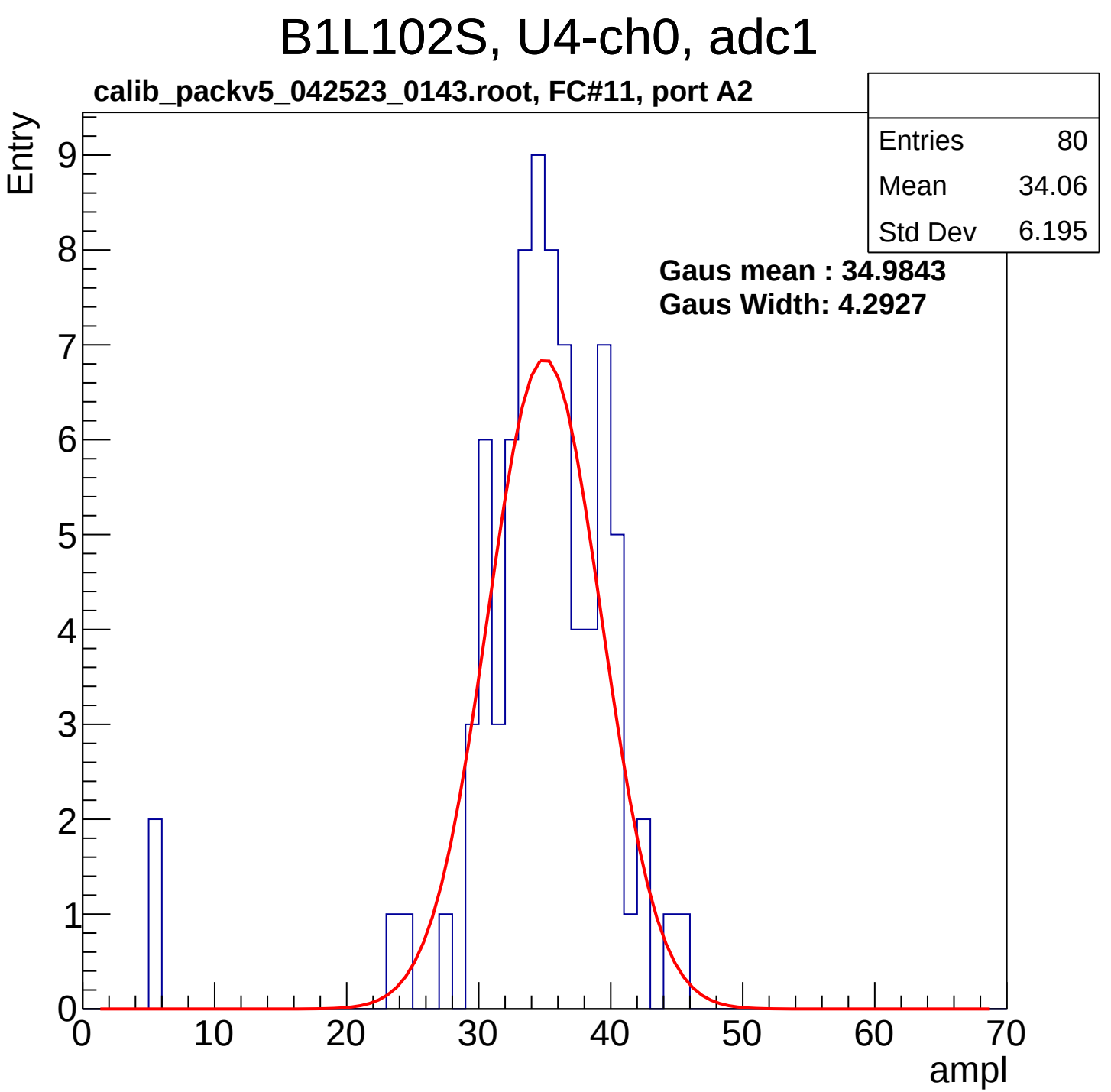
B1L102S, U4-ch0, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 80
Mean 34.06
Std Dev 6.195
Gaus mean : 34.9843
Gaus Width: 4.2927
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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40
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60
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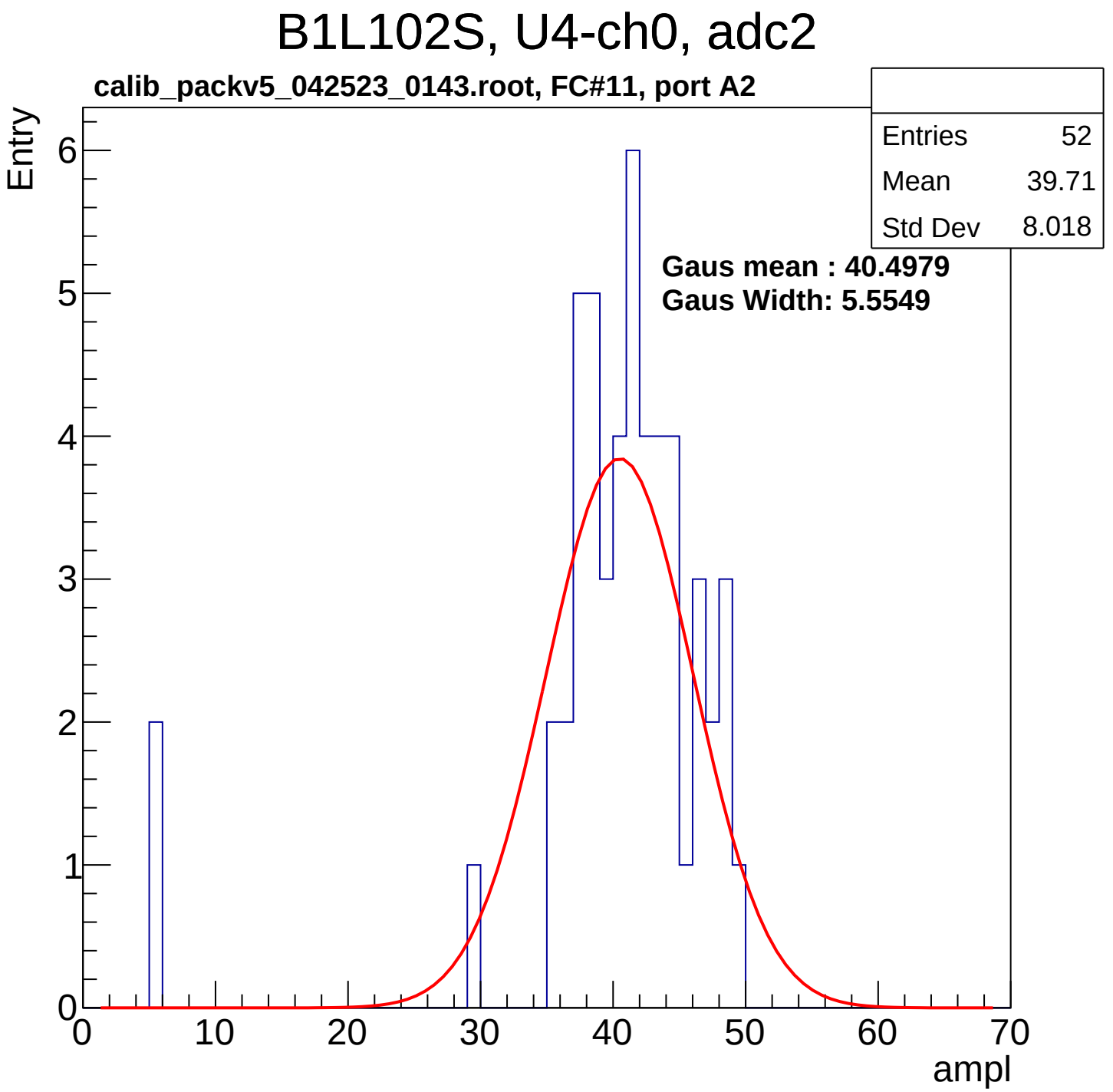
B1L102S, U4-ch0, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 52
Mean 39.71
Std Dev 8.018
Gaus mean : 40.4979
Gaus Width: 5.5549
Entry
ampl
0
1
2
3
4
5
6
0
10
20
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40
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60
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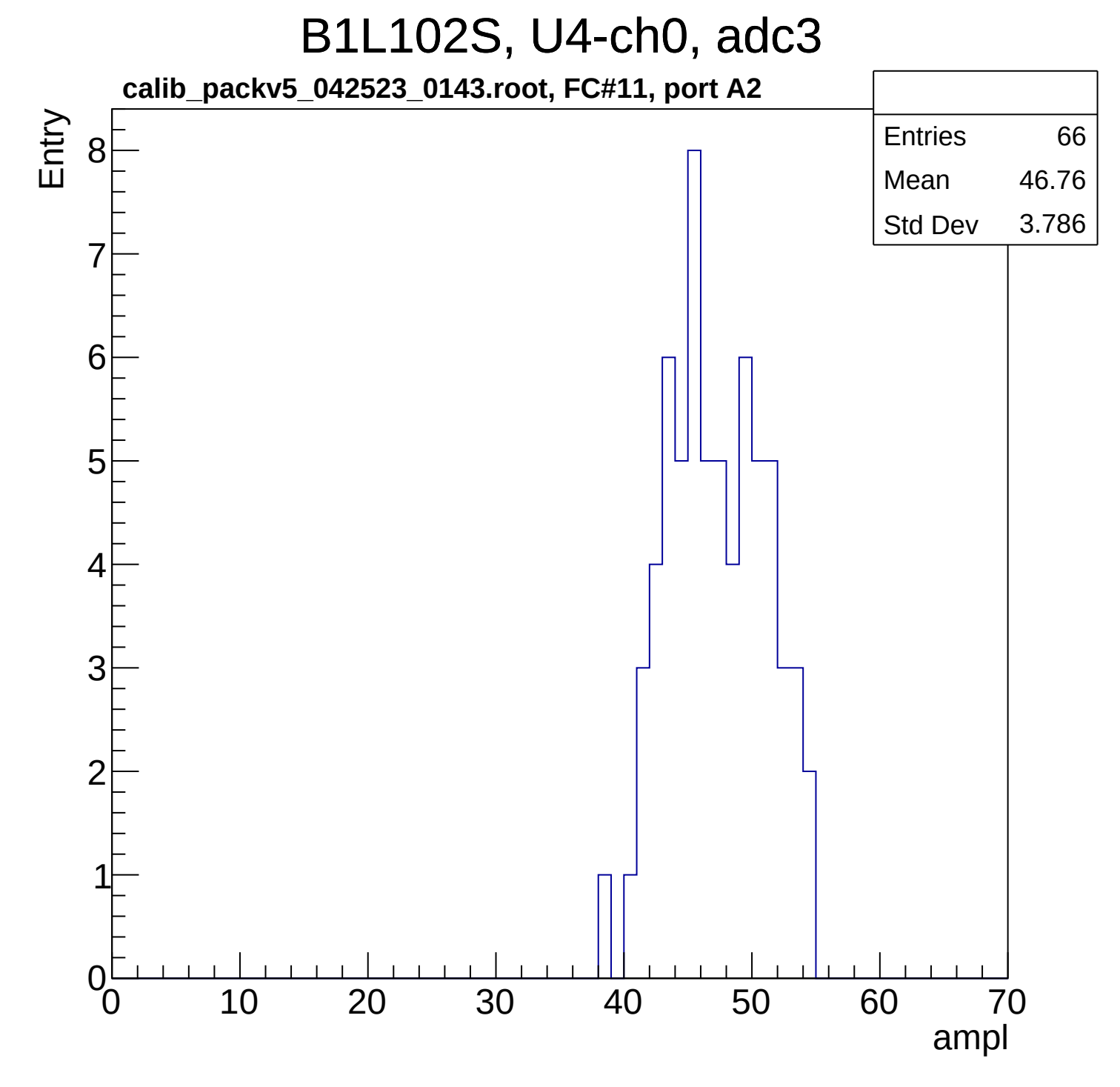
B1L102S, U4-ch0, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 46.76
Std Dev 3.786
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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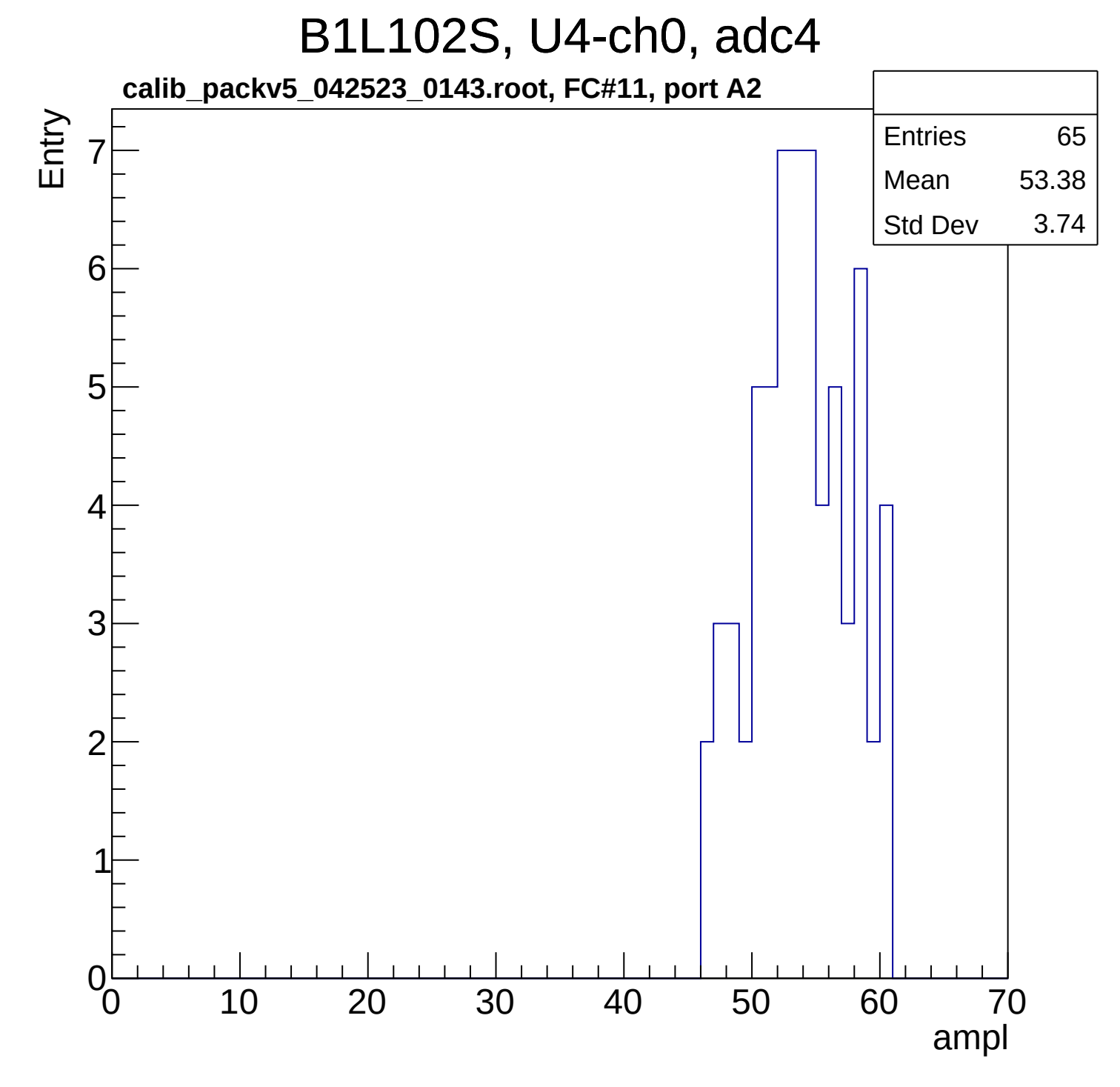
B1L102S, U4-ch0, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 53.38
Std Dev 3.74
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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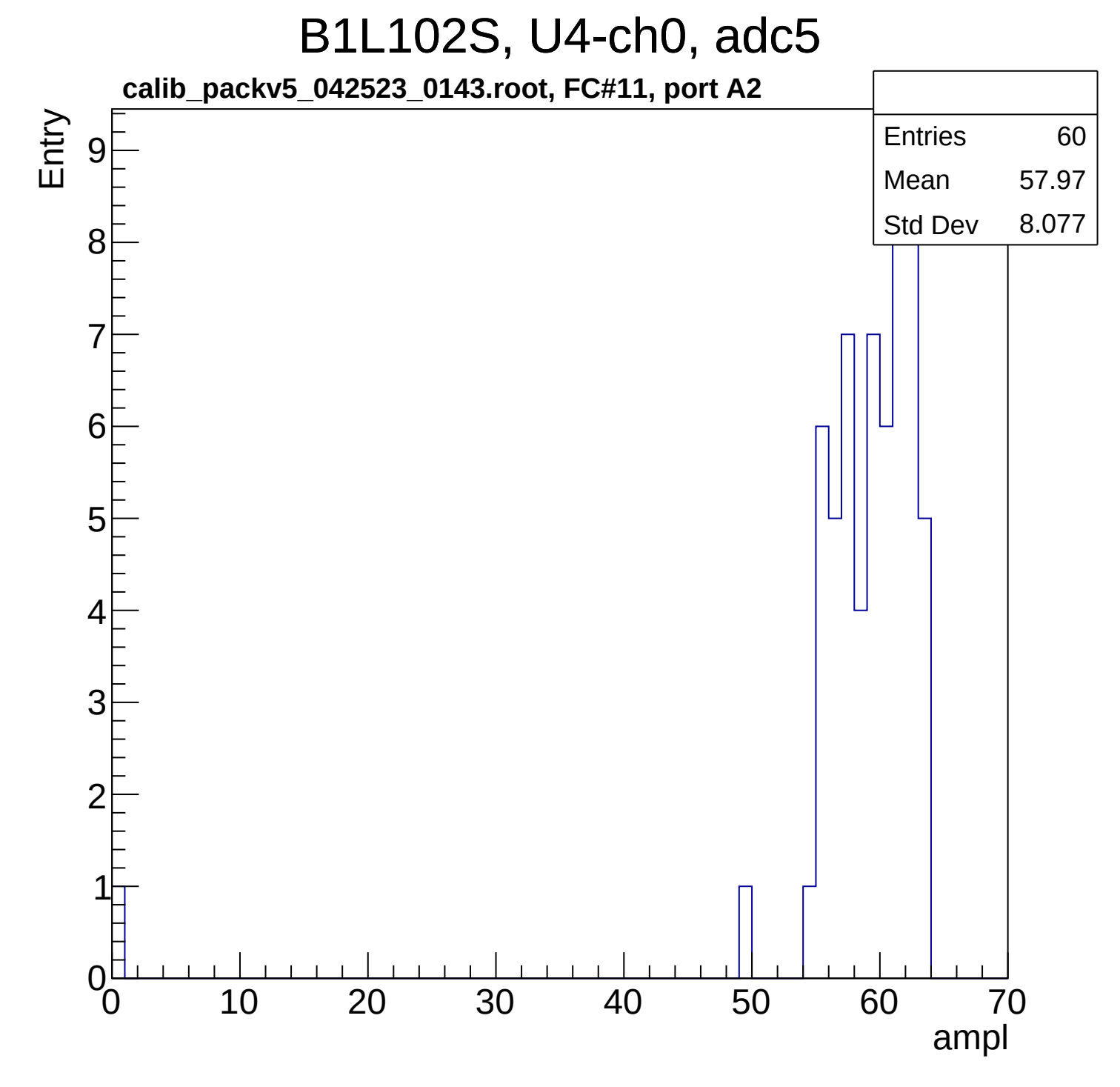
B1L102S, U4-ch0, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 57.97
Std Dev 8.077
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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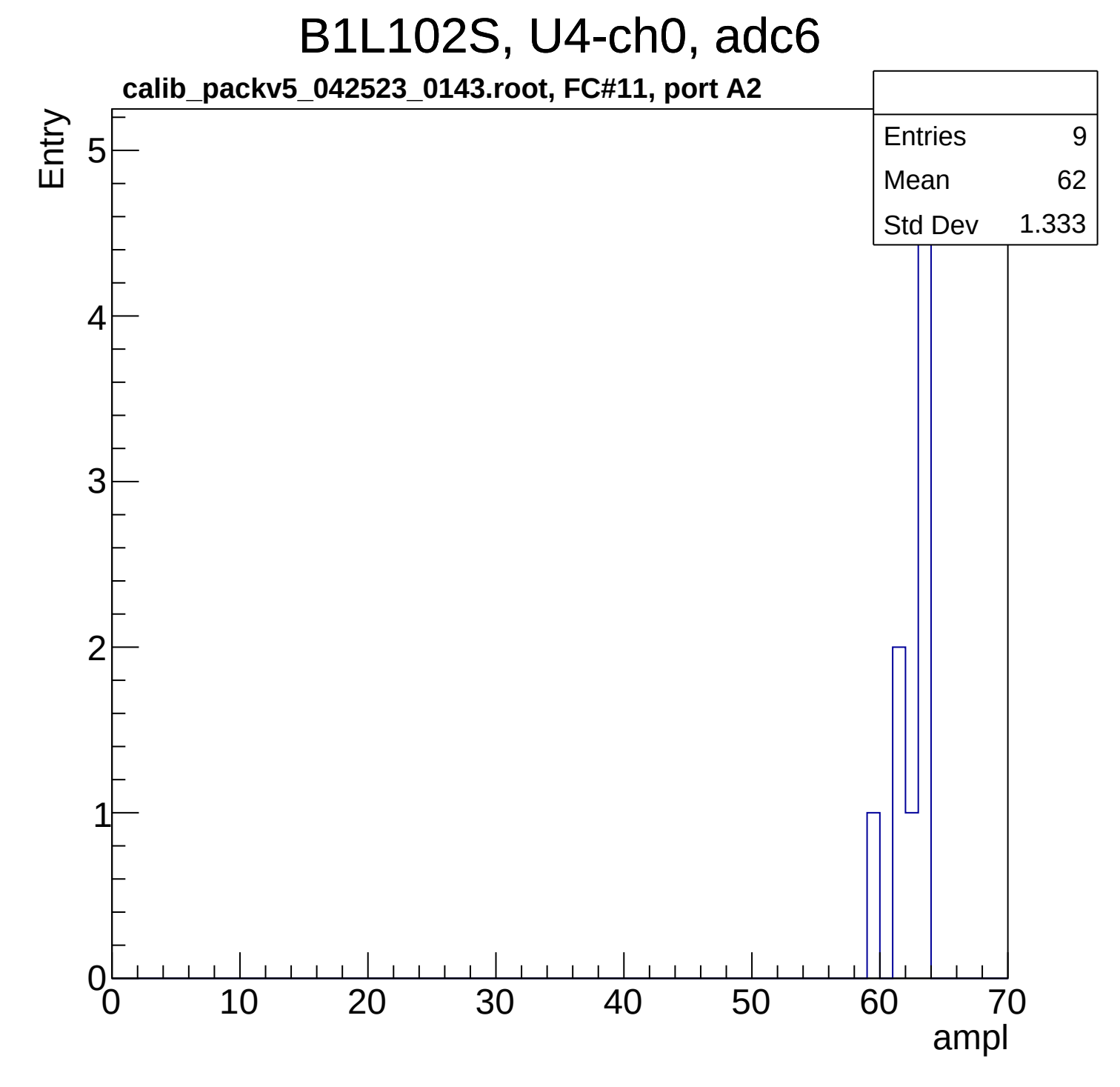
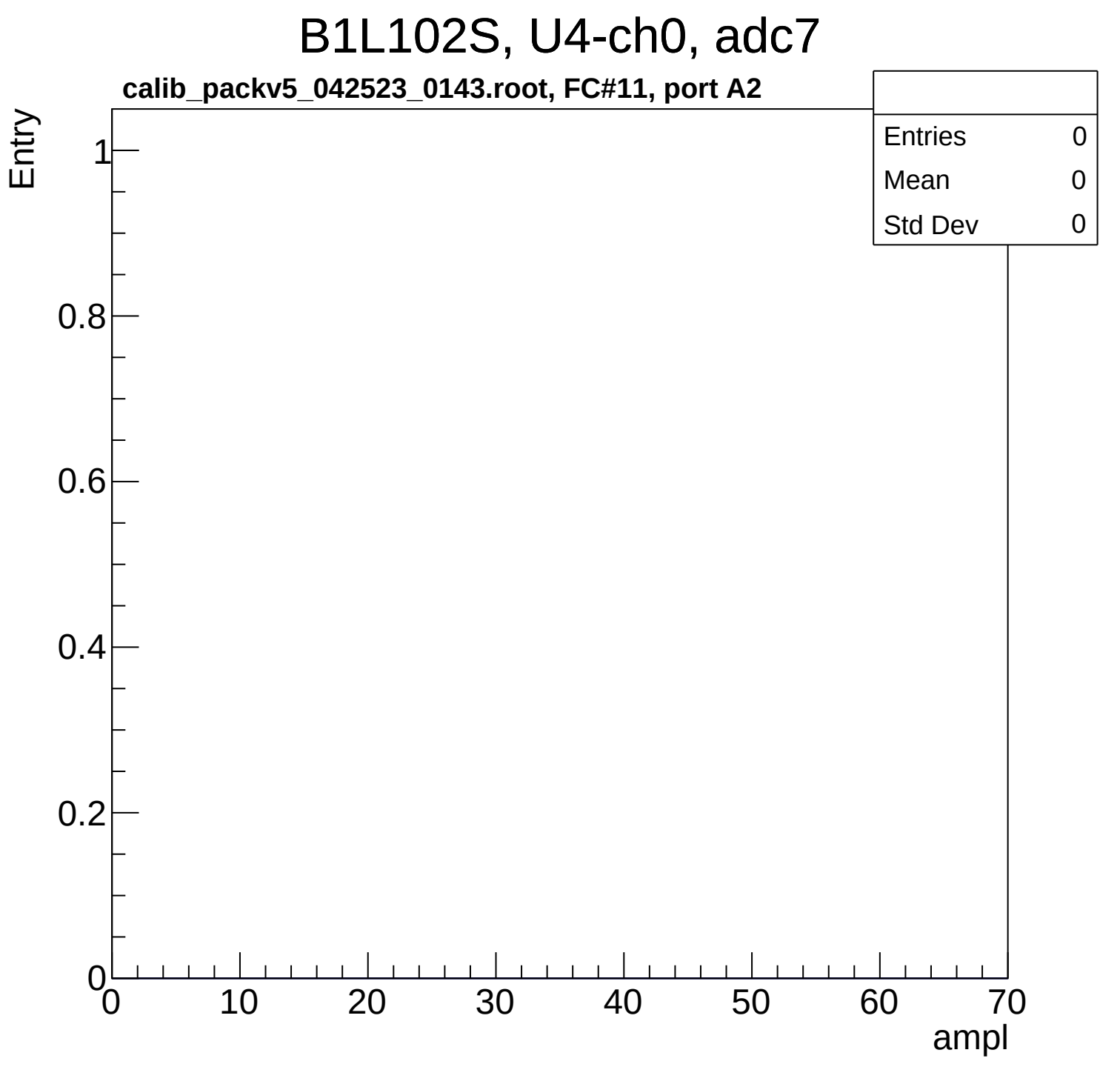
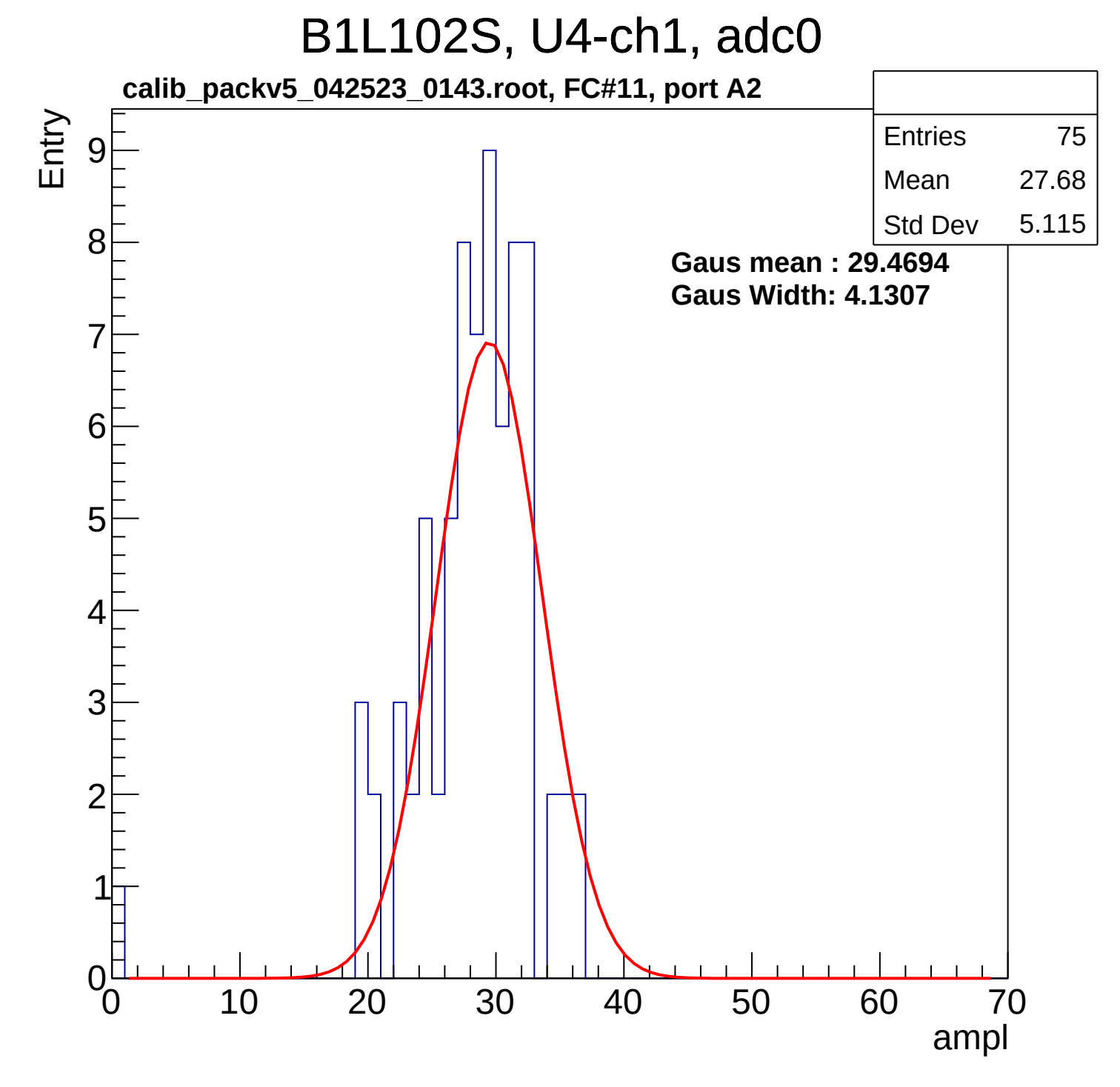
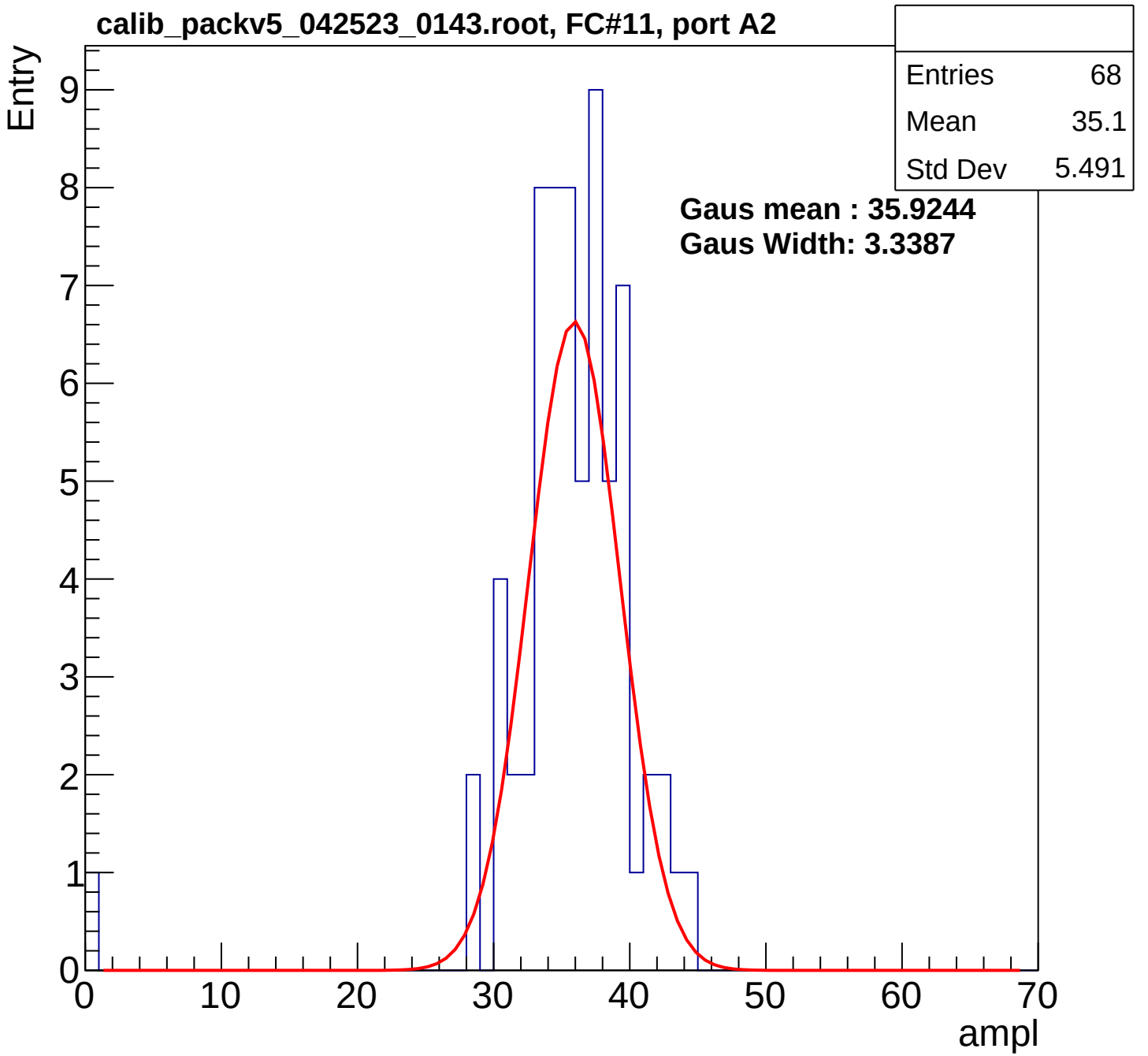

B1L102S, U4-ch0, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 9
Mean 62
Std Dev 1.333
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch0, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch1, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 27.68
Std Dev 5.115
Gaus mean : 29.4694
Gaus Width: 4.1307
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch1, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 35.1
Std Dev 5.491
Gaus mean : 35.9244
Gaus Width: 3.3387
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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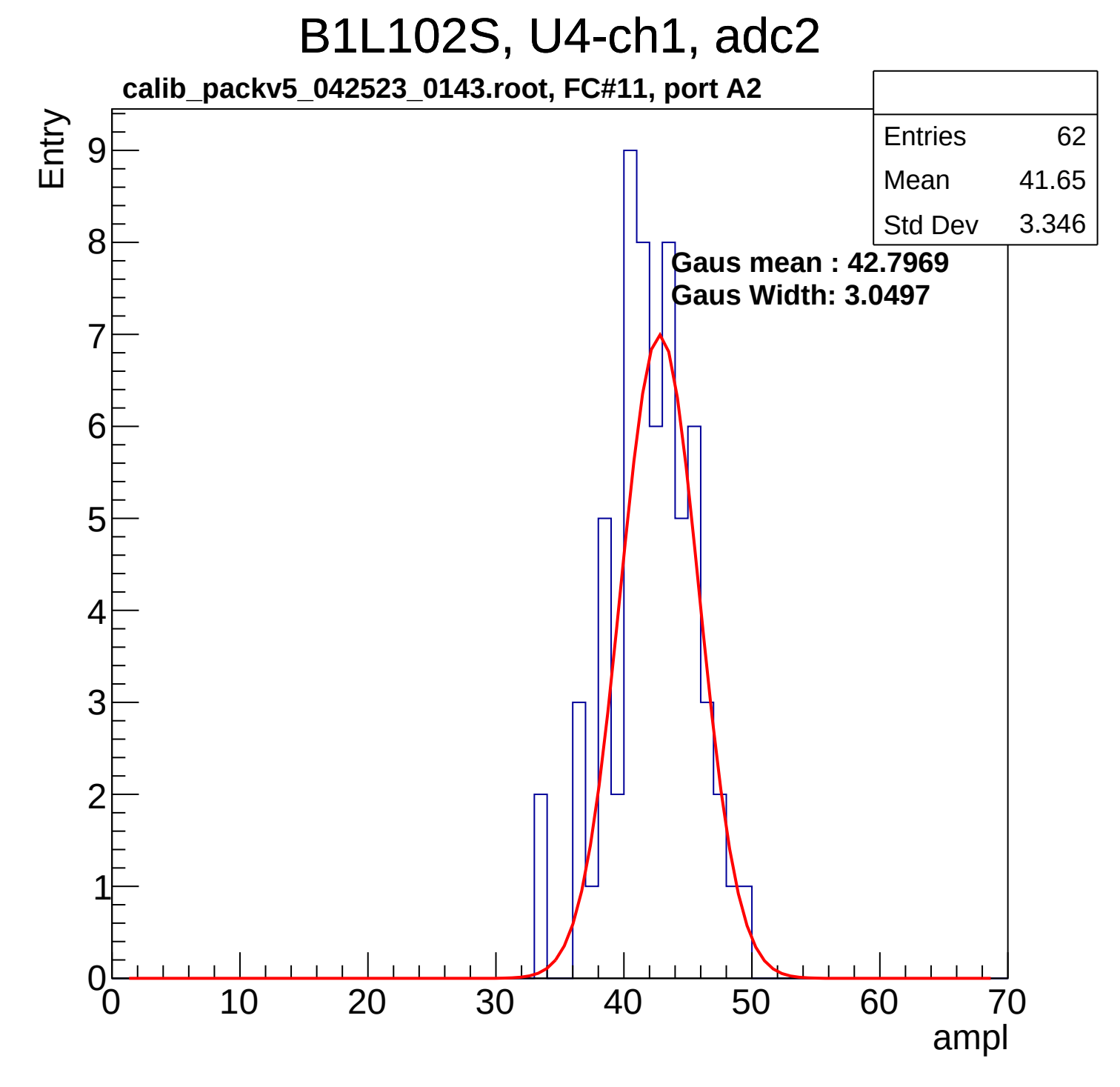
B1L102S, U4-ch1, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 41.65
Std Dev 3.346
Gaus mean : 42.7969
Gaus Width: 3.0497
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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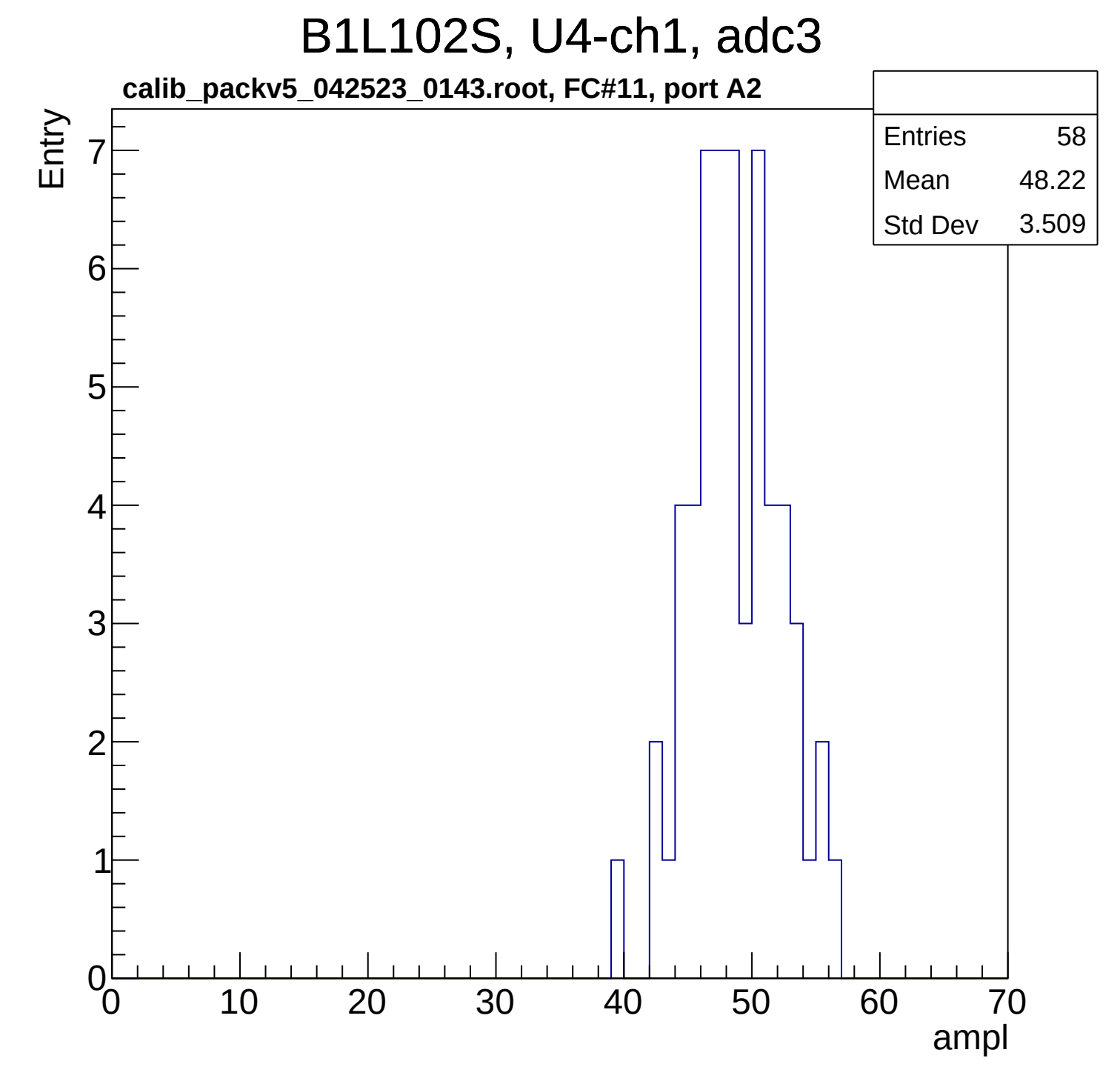
B1L102S, U4-ch1, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 48.22
Std Dev 3.509
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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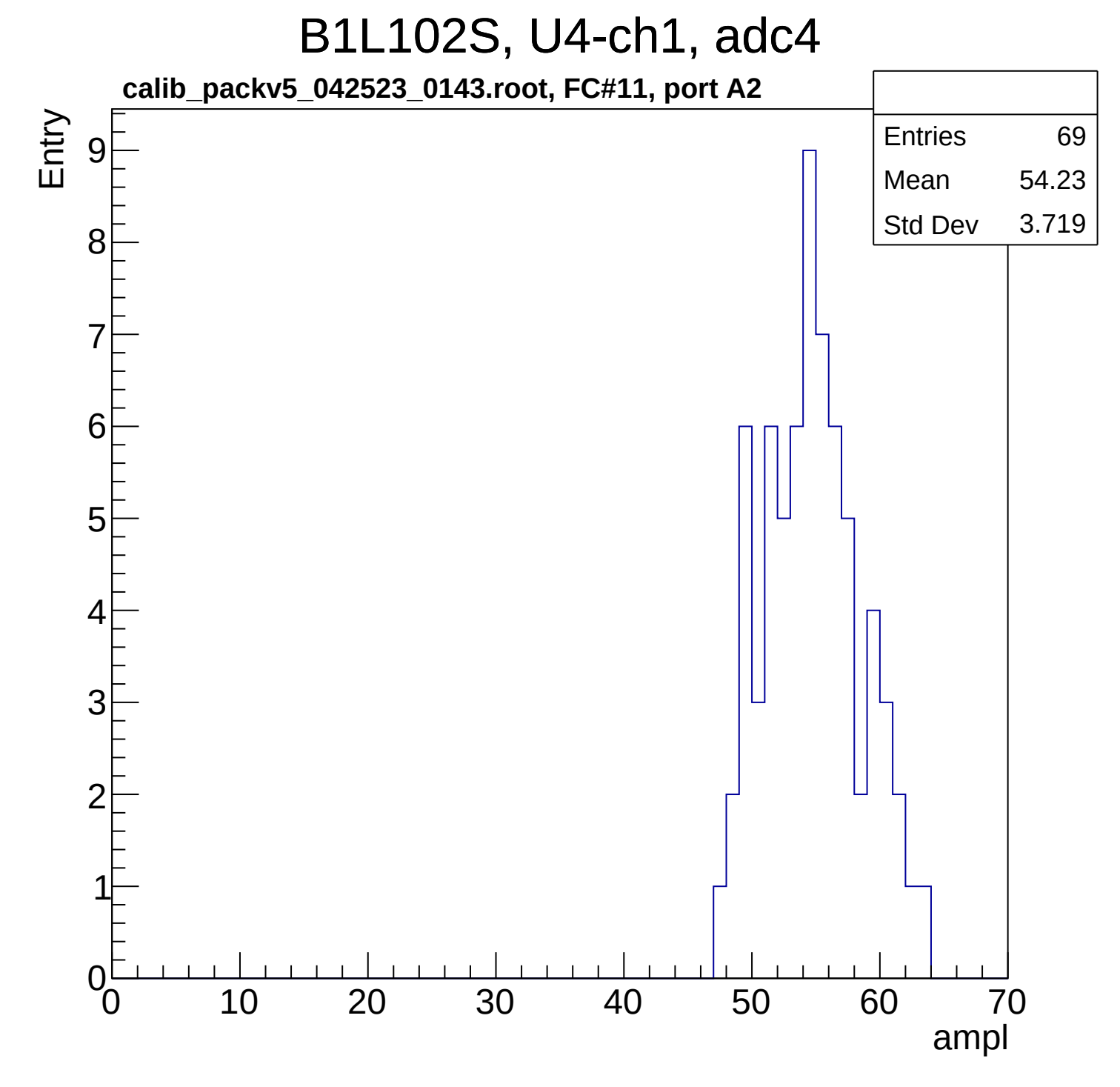
B1L102S, U4-ch1, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 54.23
Std Dev 3.719
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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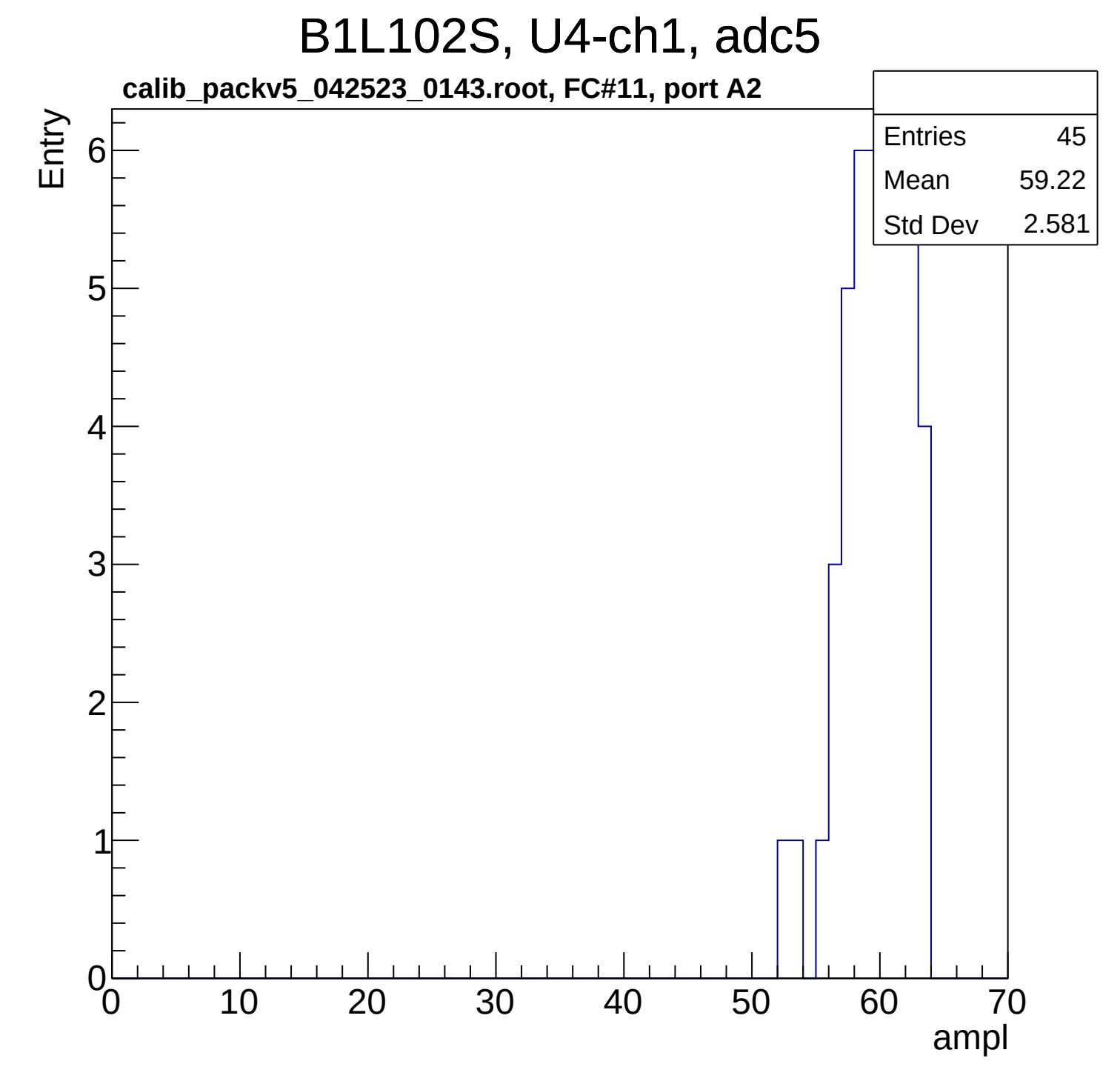
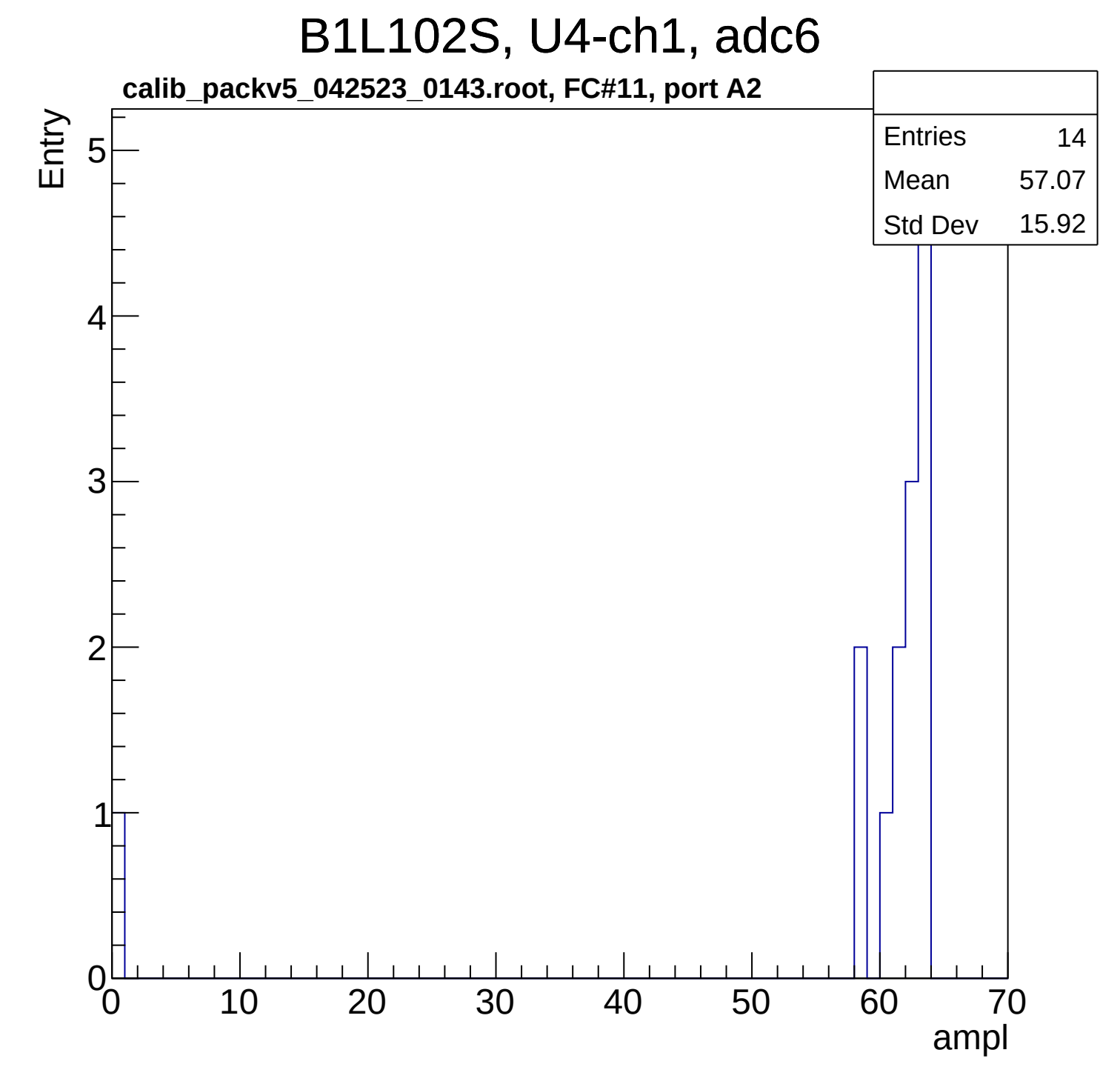
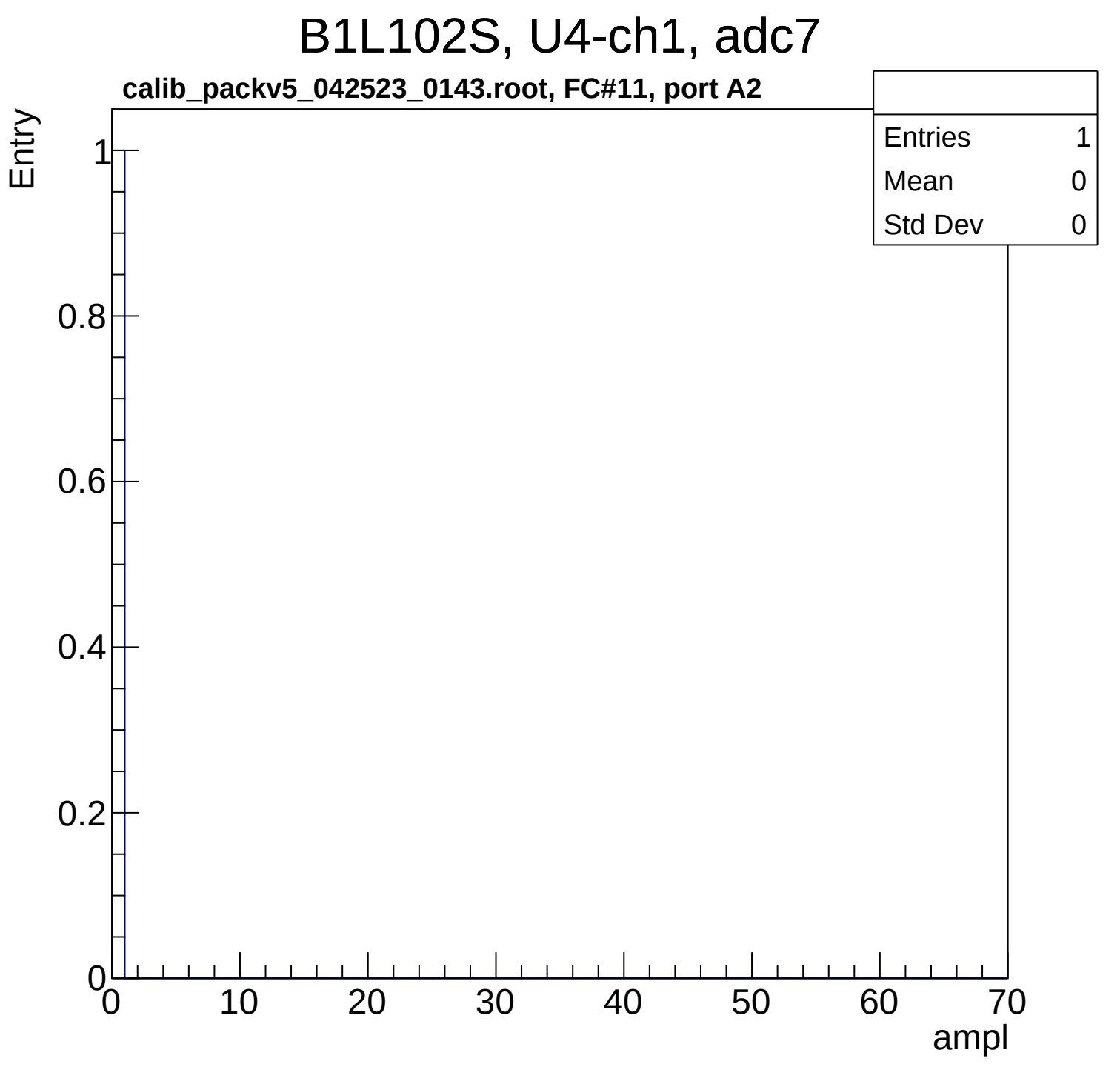
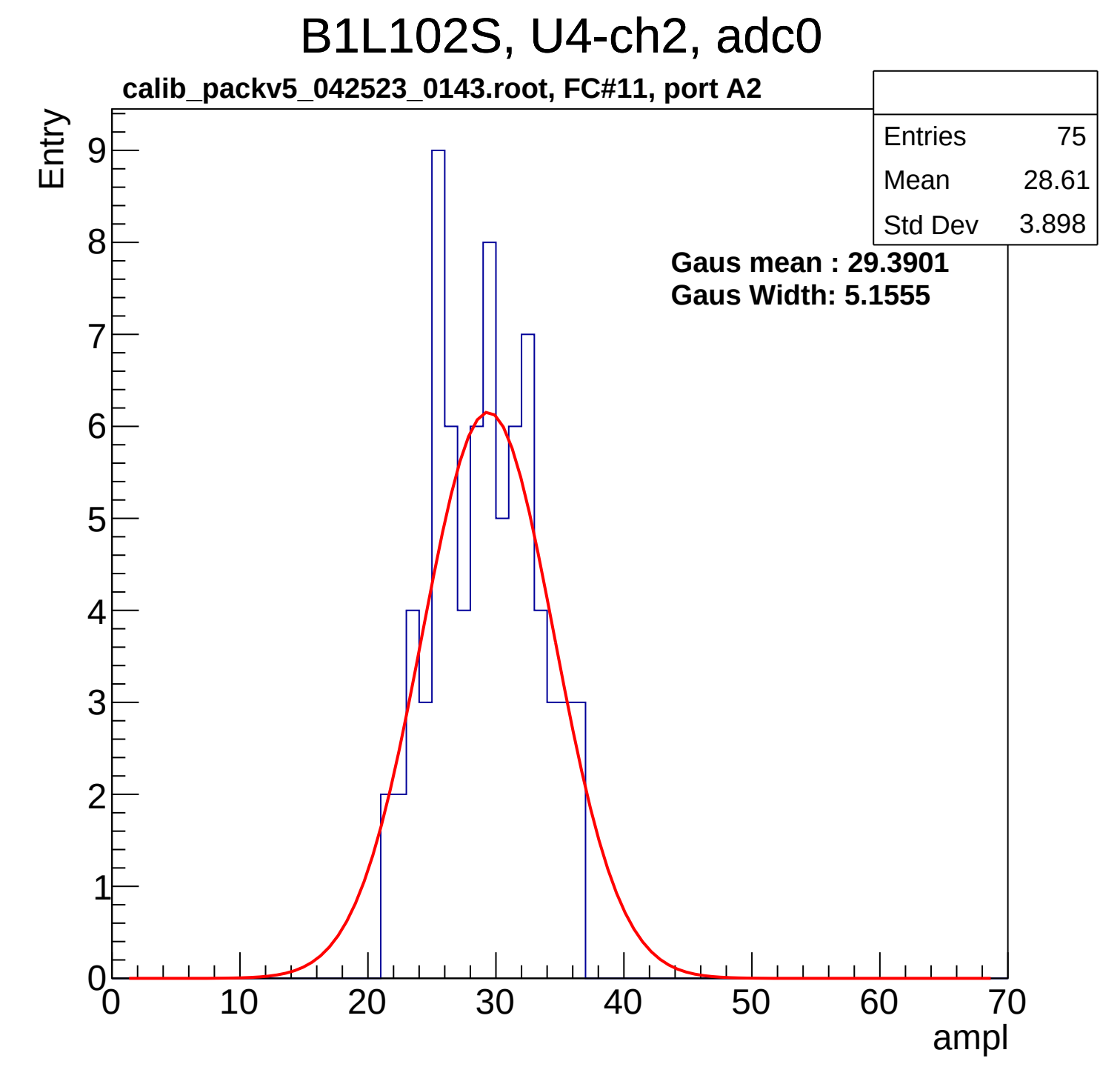

B1L102S, U4-ch1, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 45
Mean 59.22
Std Dev 2.581
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L102S, U4-ch1, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 14
Mean 57.07
Std Dev 15.92
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch1, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch2, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 28.61
Std Dev 3.898
Gaus mean : 29.3901
Gaus Width: 5.1555
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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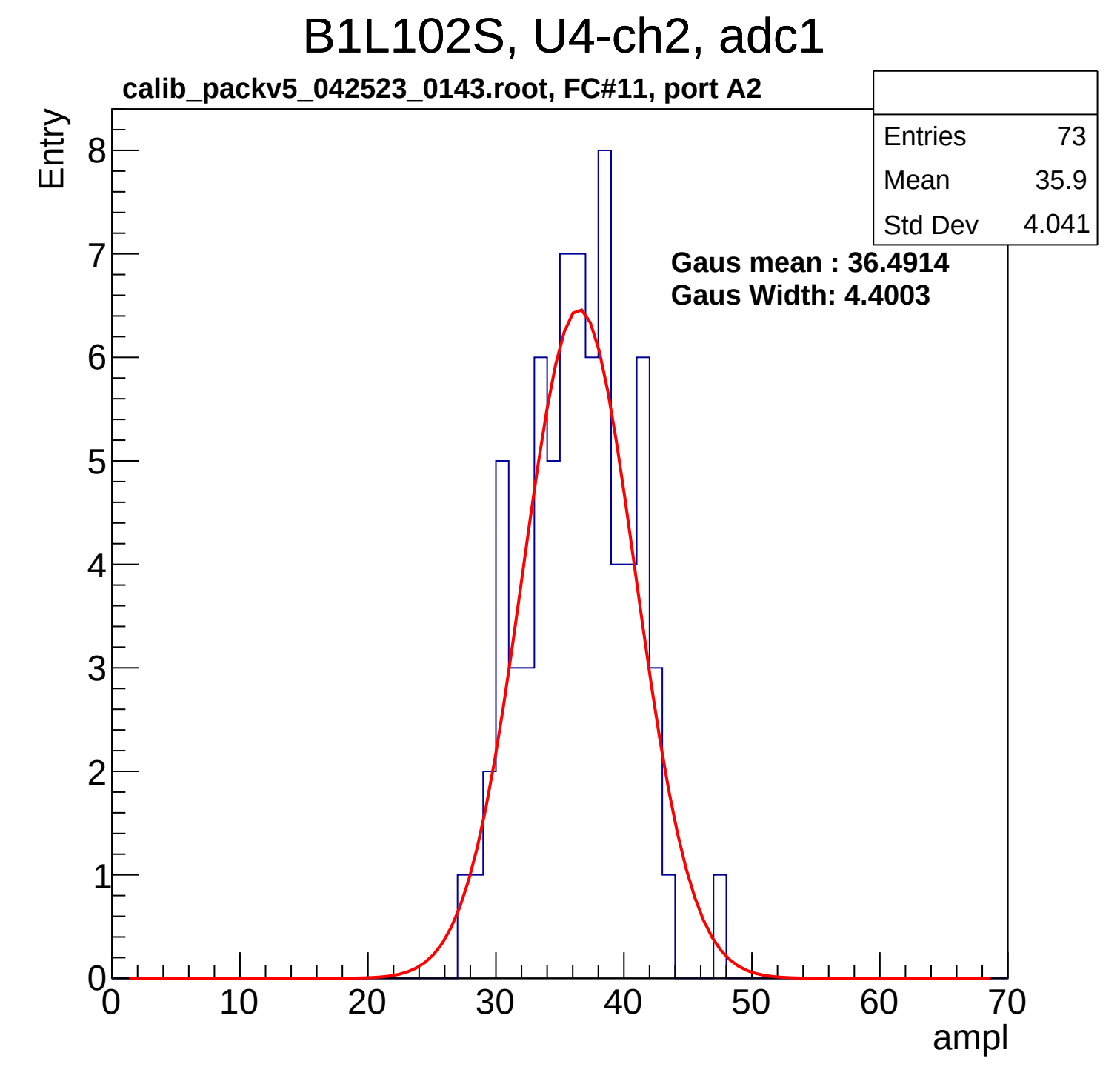
B1L102S, U4-ch2, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 35.9
Std Dev 4.041
Gaus mean : 36.4914
Gaus Width: 4.4003
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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20
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40
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60
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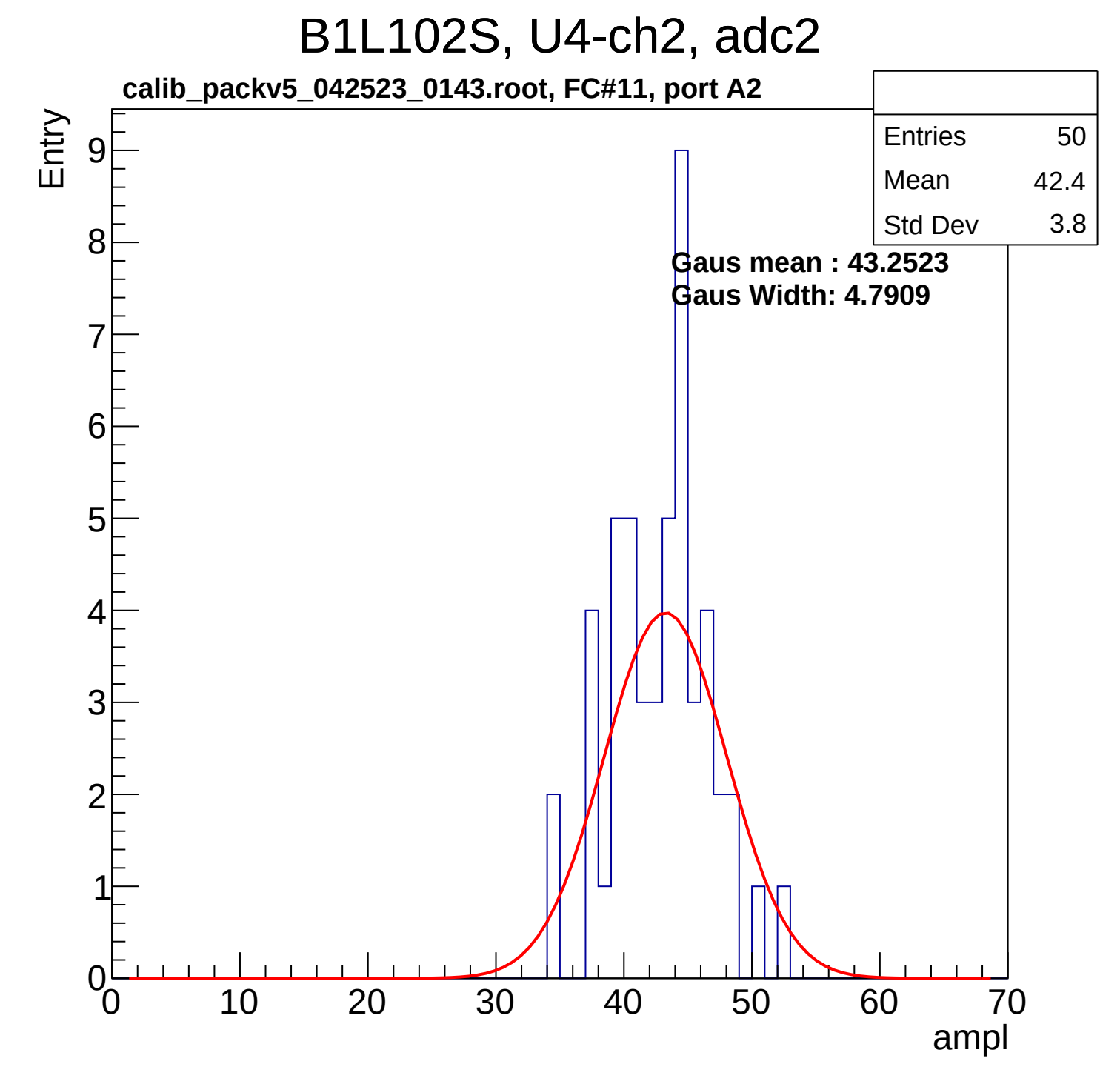
B1L102S, U4-ch2, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 50
Mean 42.4
Std Dev 3.8
Gaus mean : 43.2523
Gaus Width: 4.7909
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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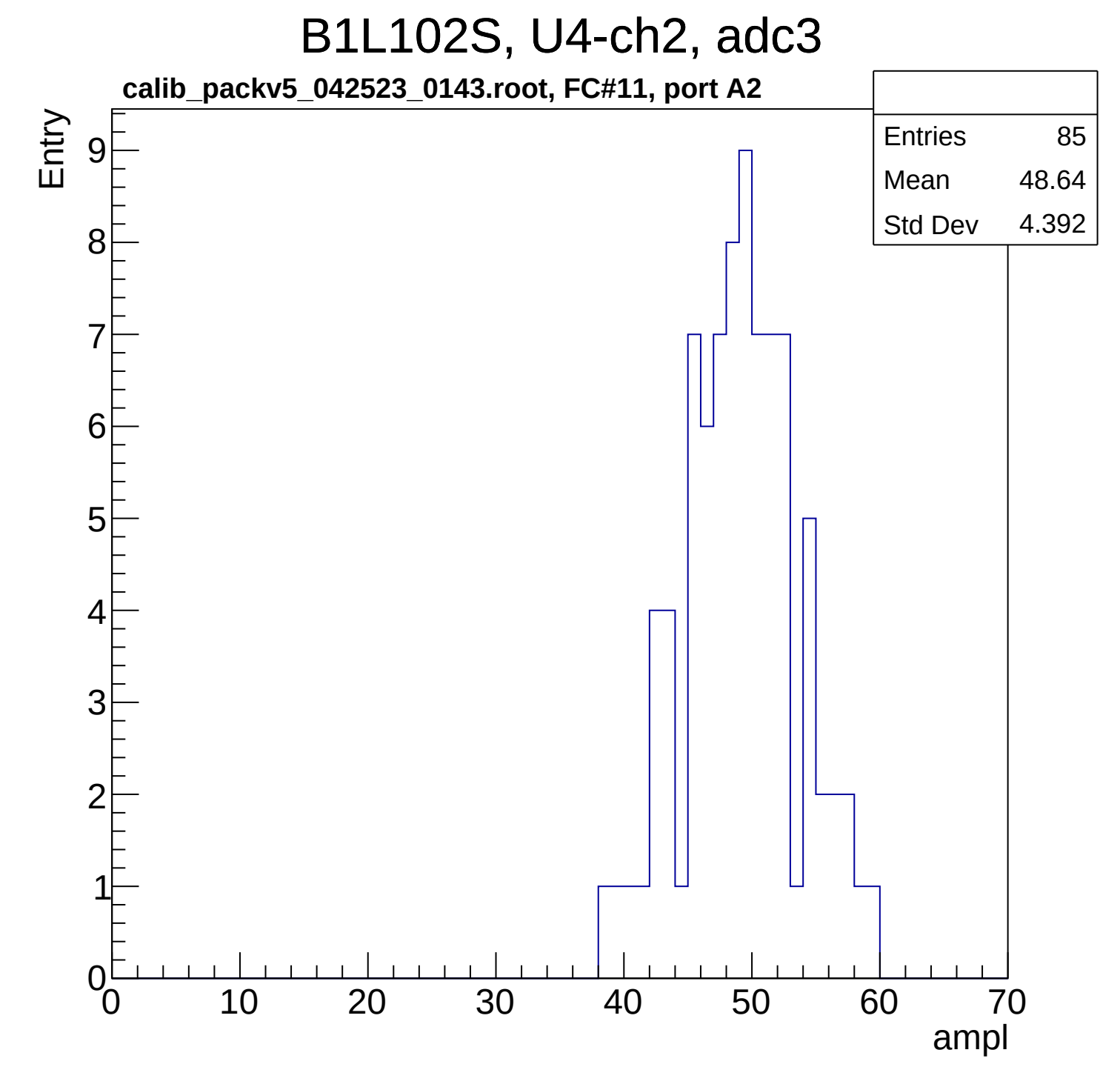
B1L102S, U4-ch2, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 85
Mean 48.64
Std Dev 4.392
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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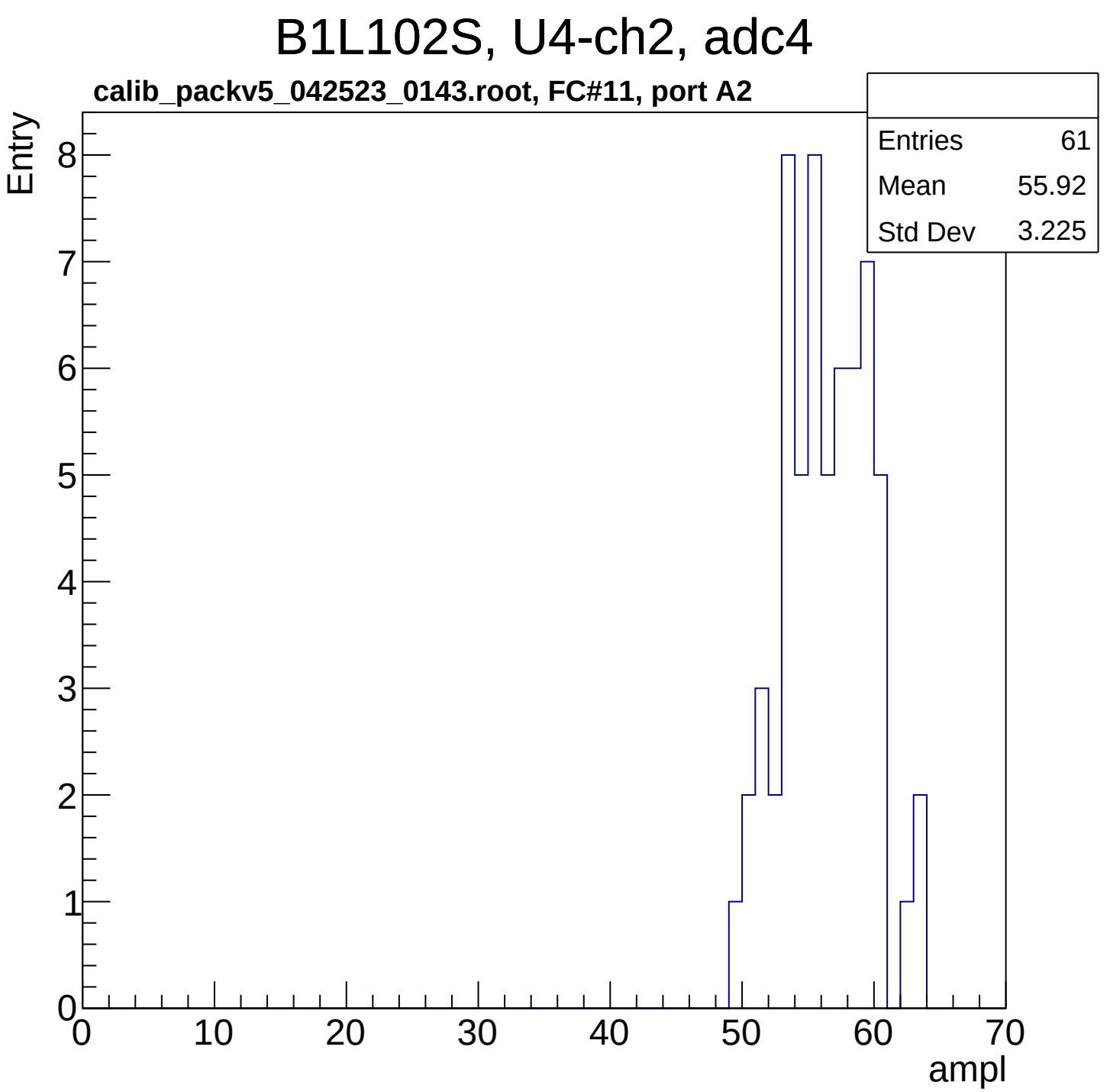
B1L102S, U4-ch2, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 55.92
Std Dev 3.225
Entry
ampl
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1
2
3
4
5
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7
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0
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40
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60
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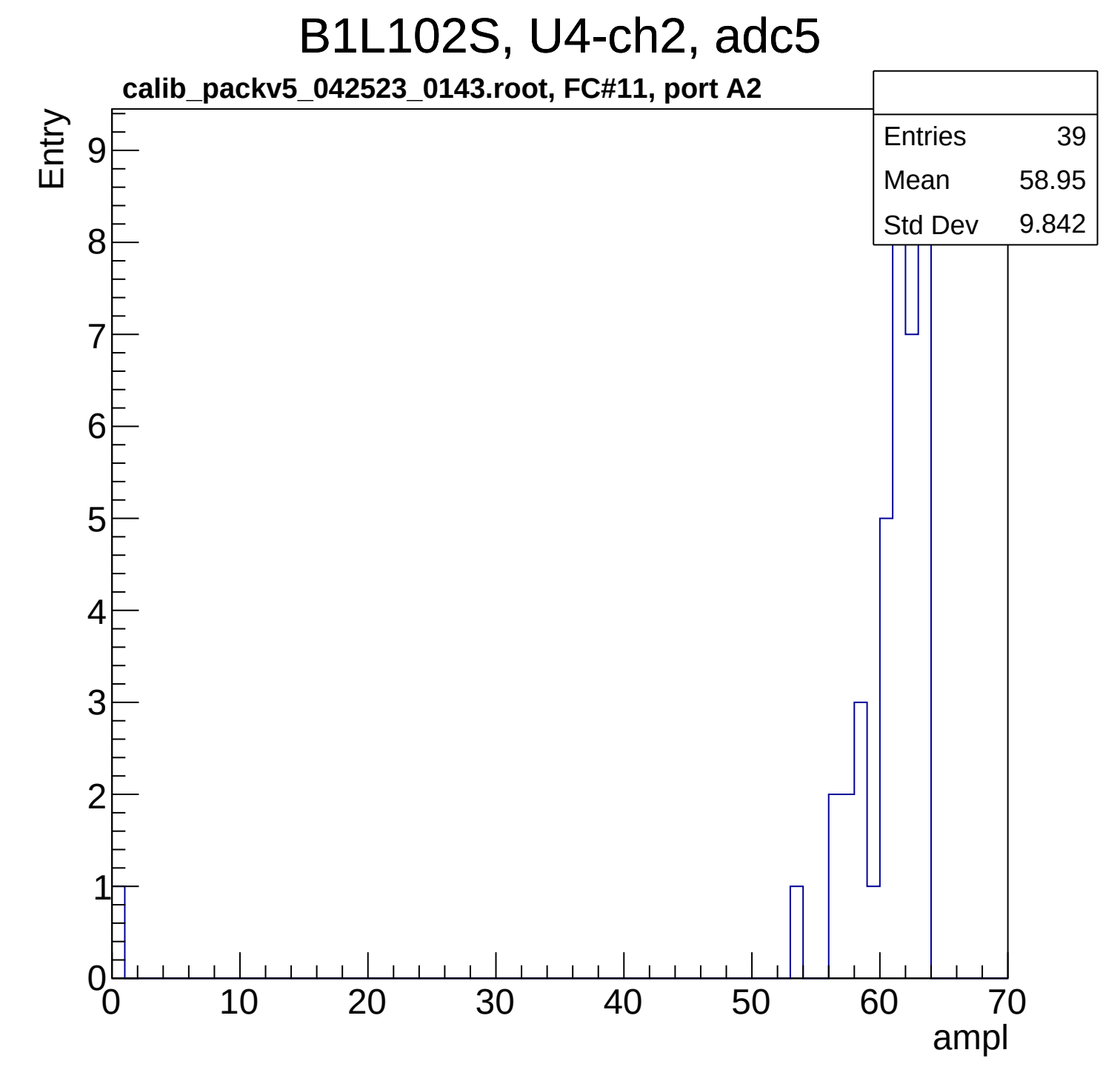
B1L102S, U4-ch2, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 39
Mean 58.95
Std Dev 9.842
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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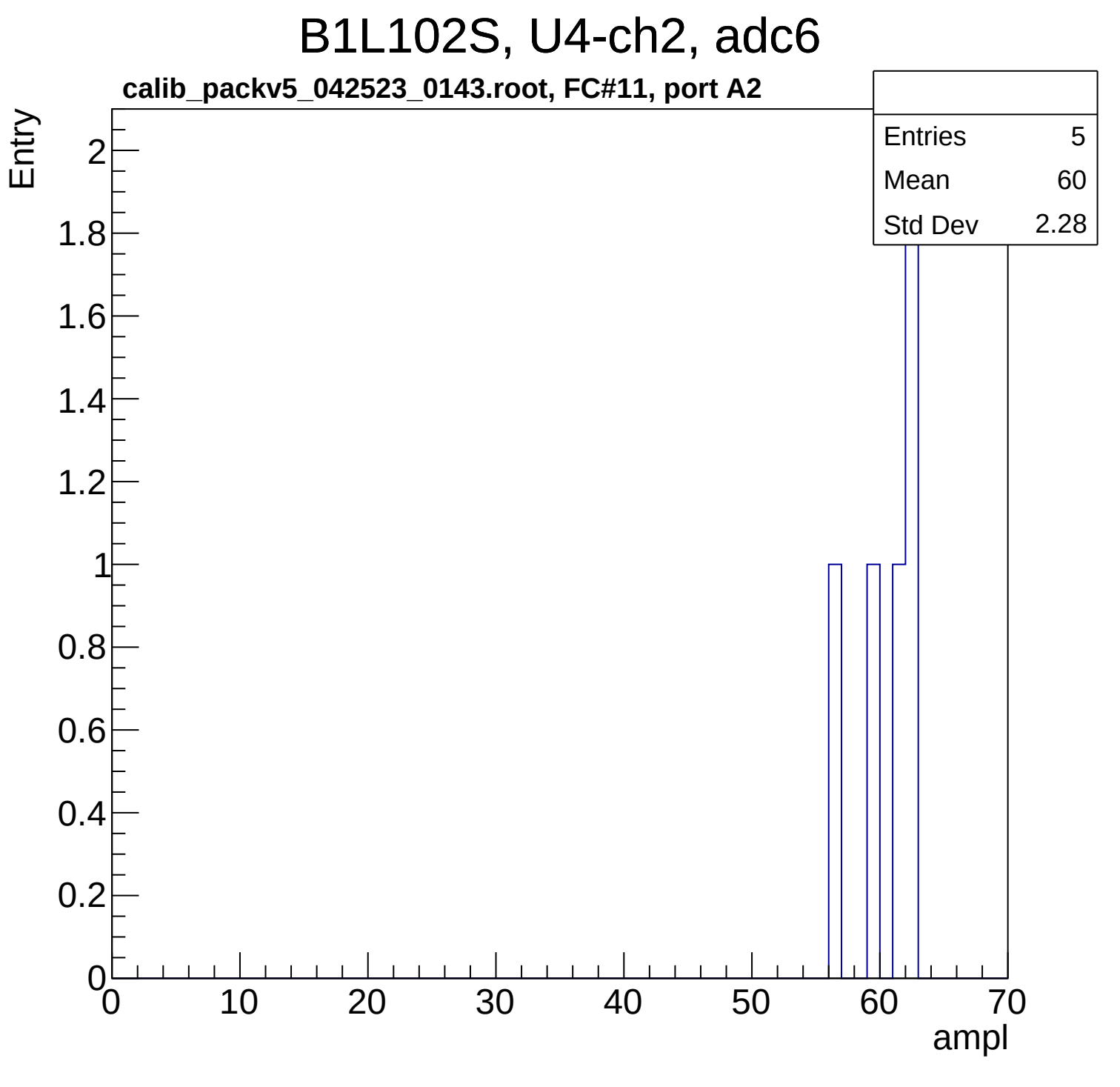
B1L102S, U4-ch2, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 5
Mean 60
Std Dev 2.28
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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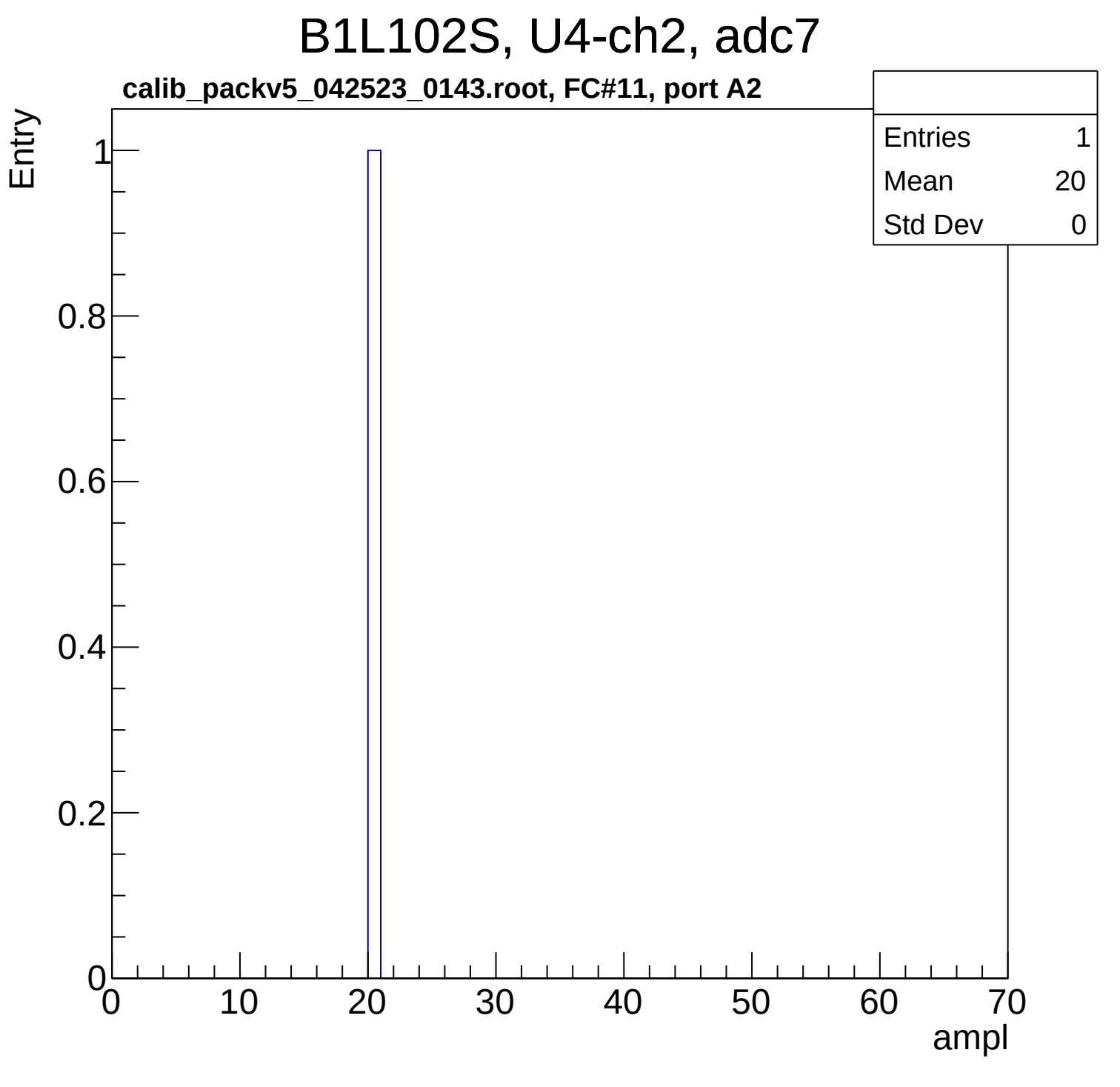
B1L102S, U4-ch2, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 20
Std Dev 0
Entry
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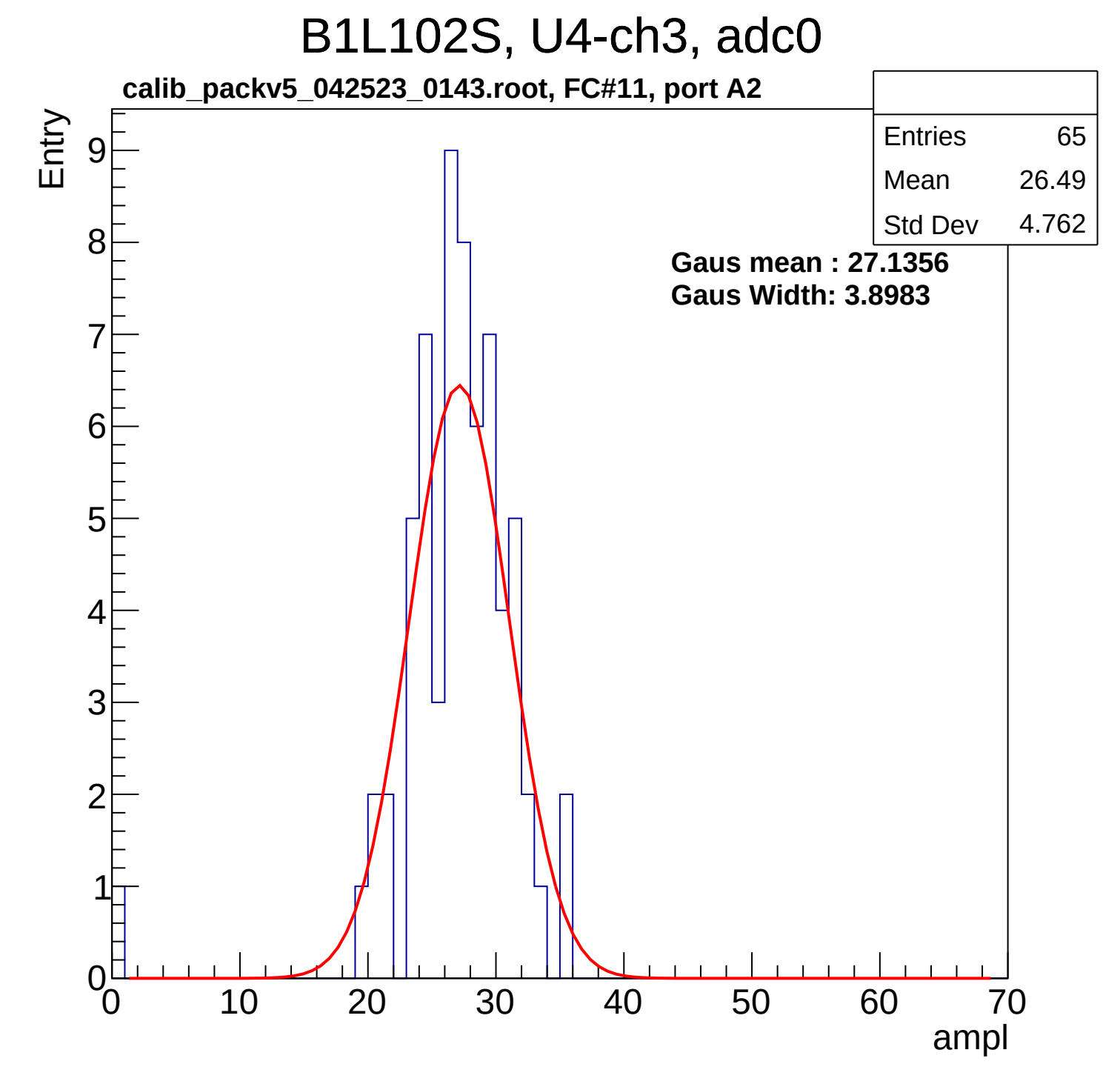
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch3, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 26.49
Std Dev 4.762
Gaus mean : 27.1356
Gaus Width: 3.8983
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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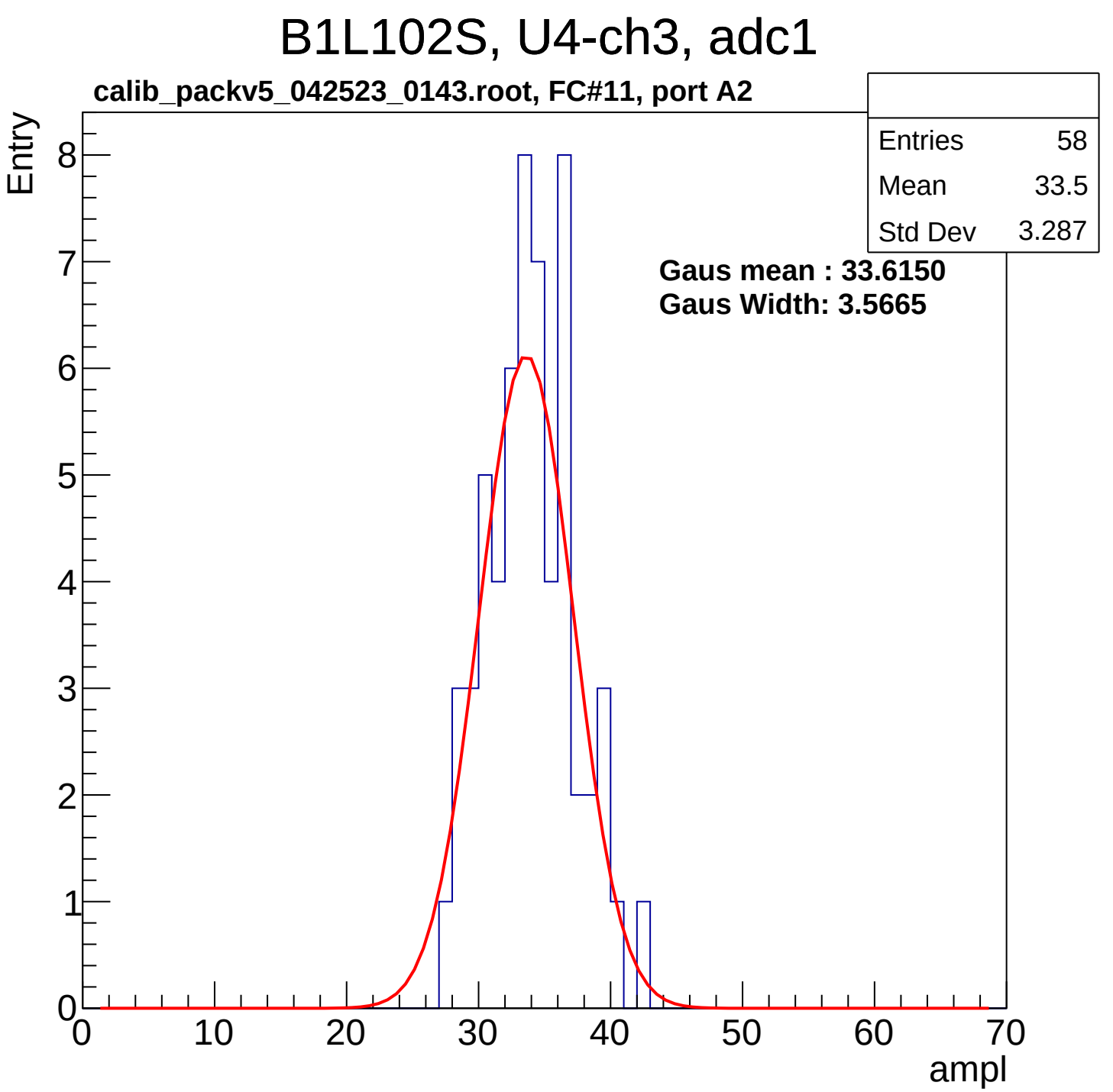
B1L102S, U4-ch3, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 33.5
Std Dev 3.287
Gaus mean : 33.6150
Gaus Width: 3.5665
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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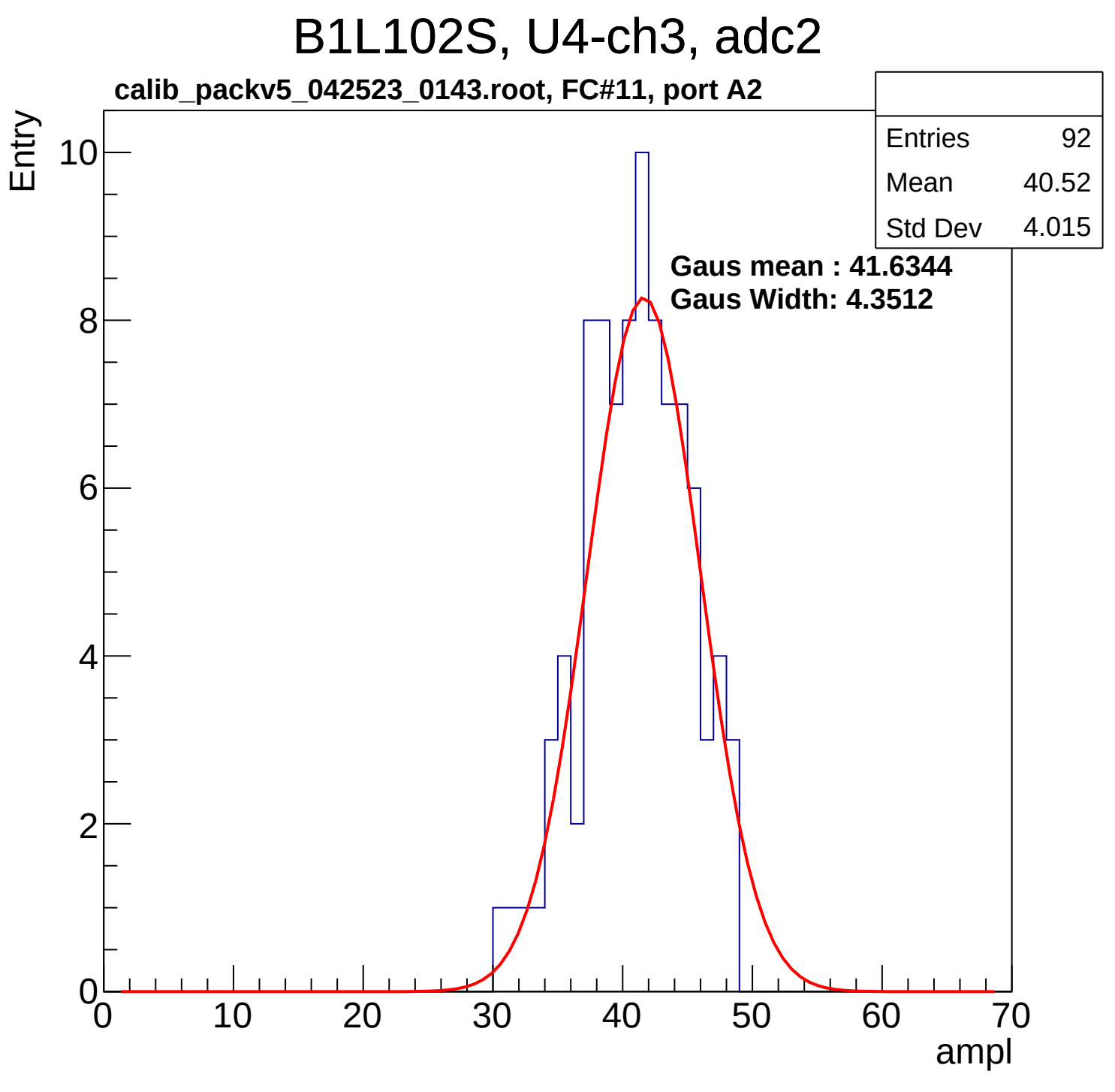
B1L102S, U4-ch3, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 92
Mean 40.52
Std Dev 4.015
Gaus mean : 41.6344
Gaus Width: 4.3512
Entry
ampl
0
2
4
6
8
10
0
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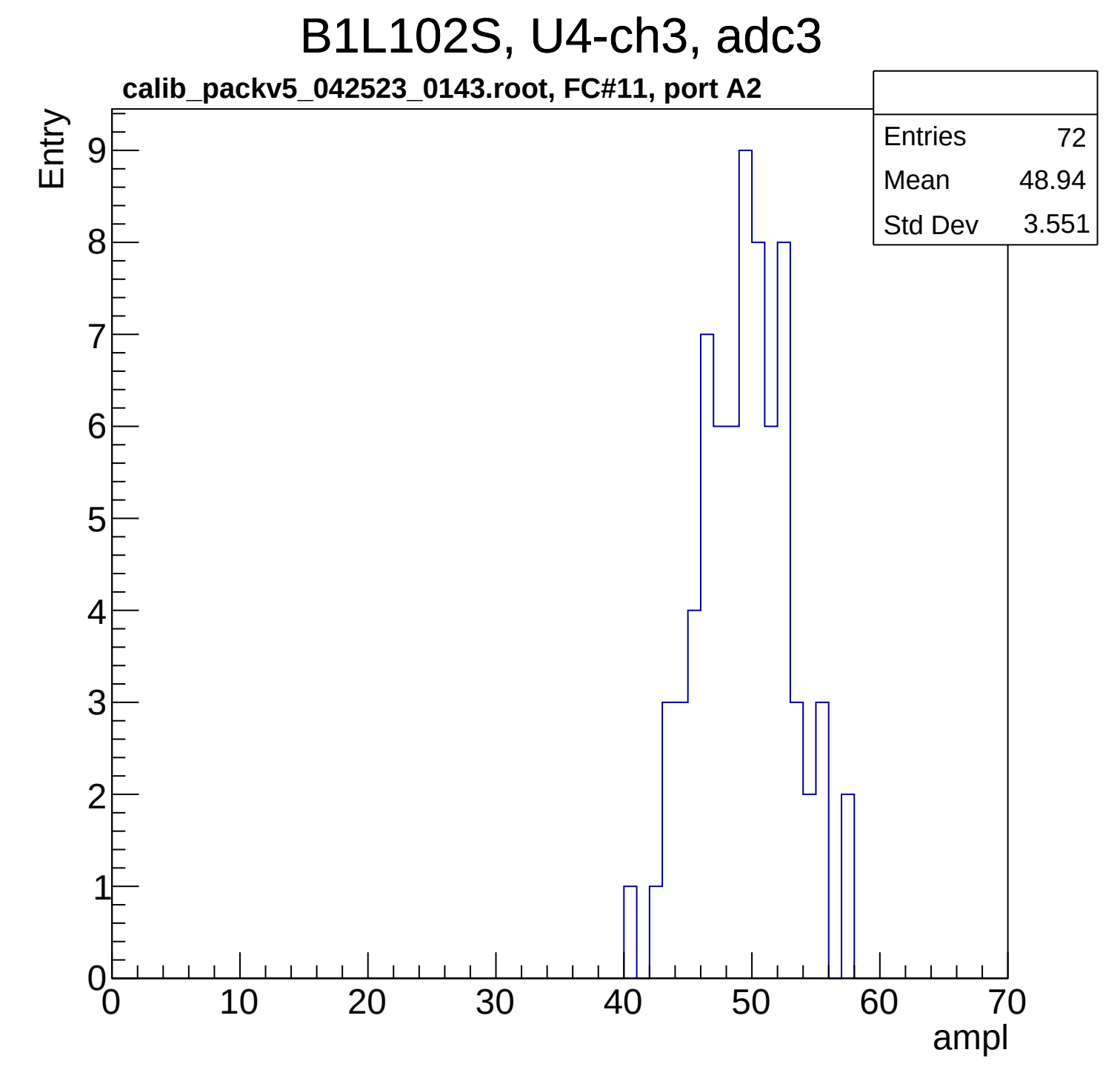
20
30
40
50
60
70


B1L102S, U4-ch3, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 72
Mean 48.94
Std Dev 3.551
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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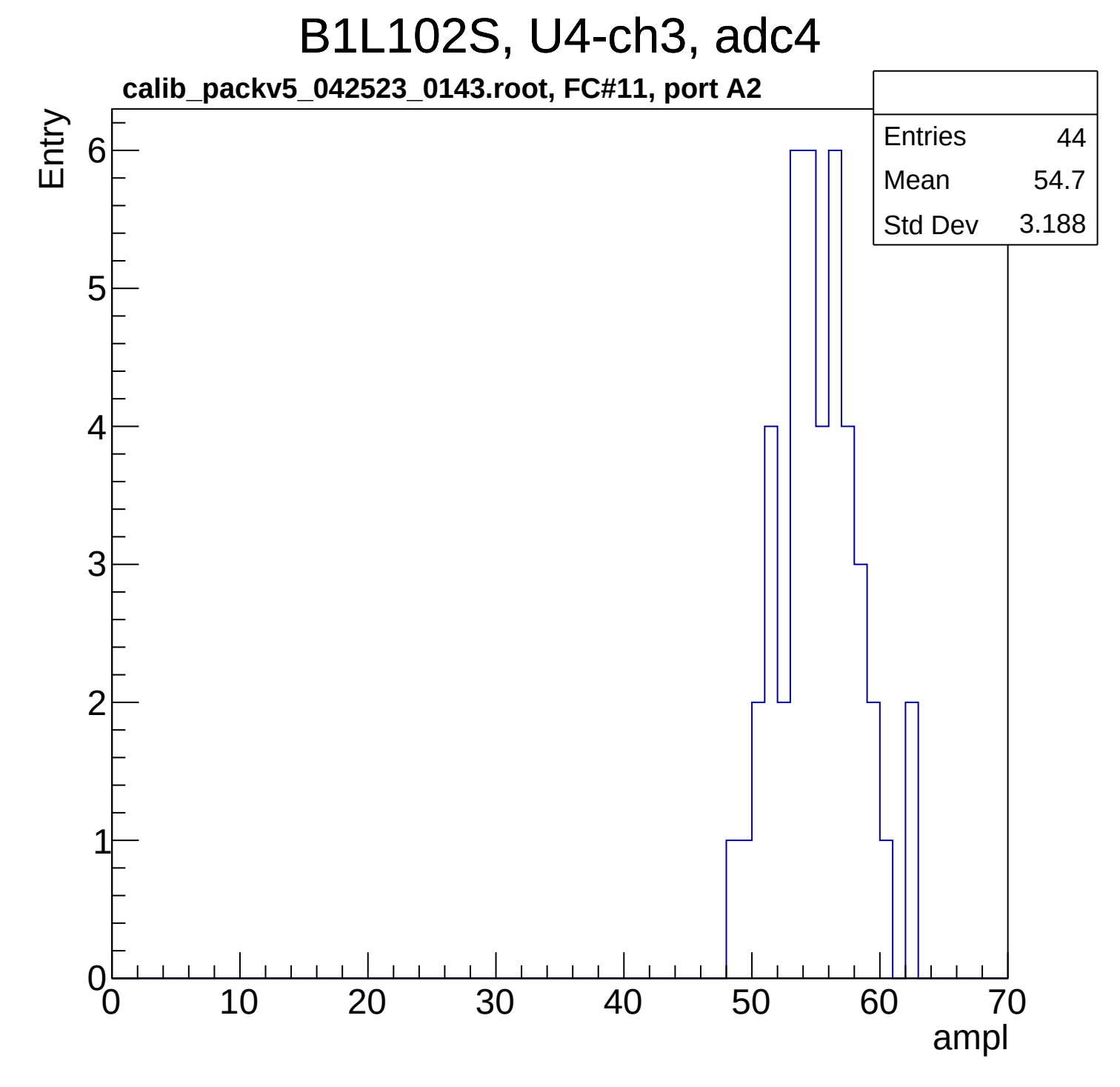
B1L102S, U4-ch3, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 44
Mean 54.7
Std Dev 3.188
Entry
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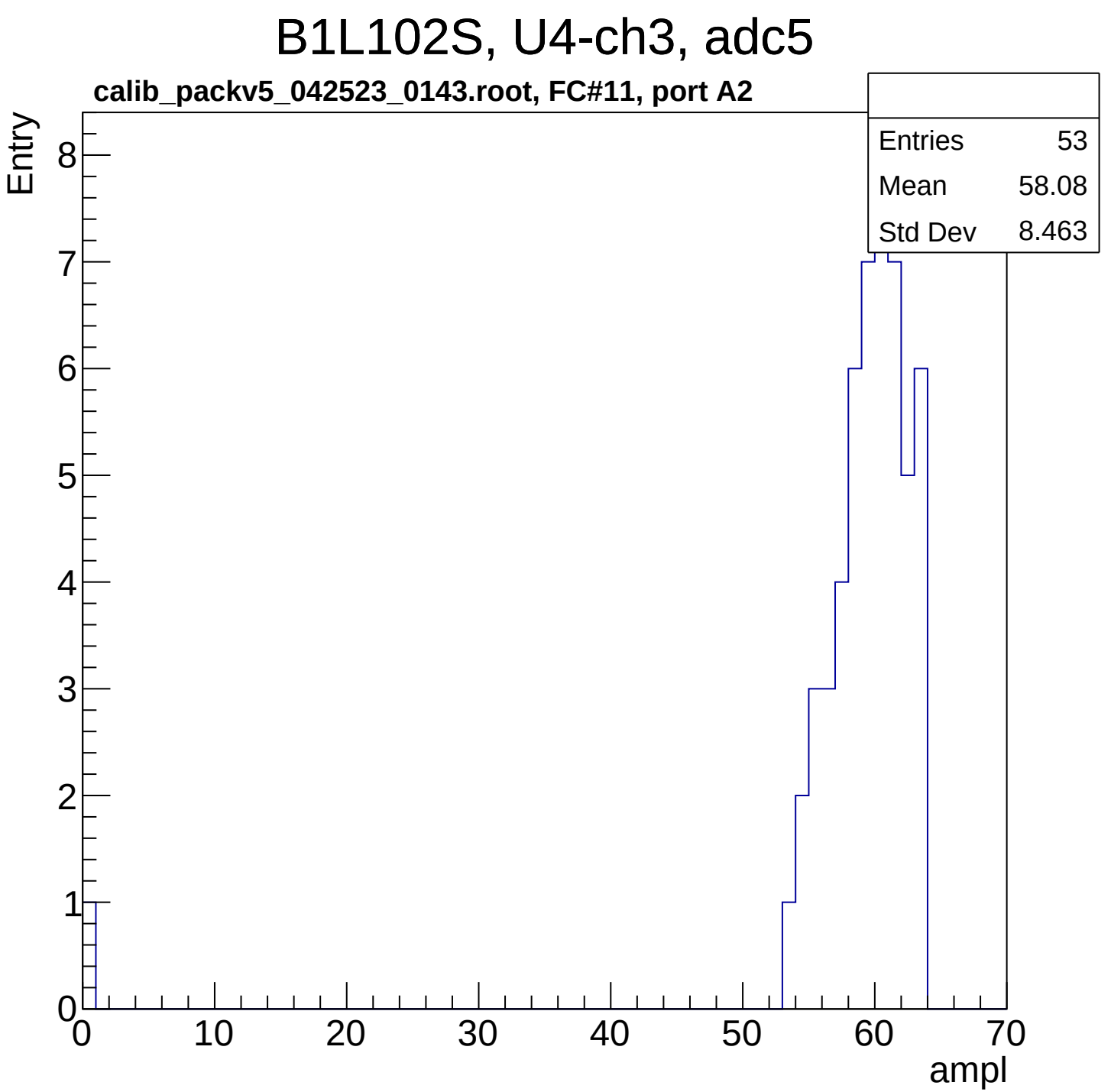
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch3, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 58.08
Std Dev 8.463
Entry
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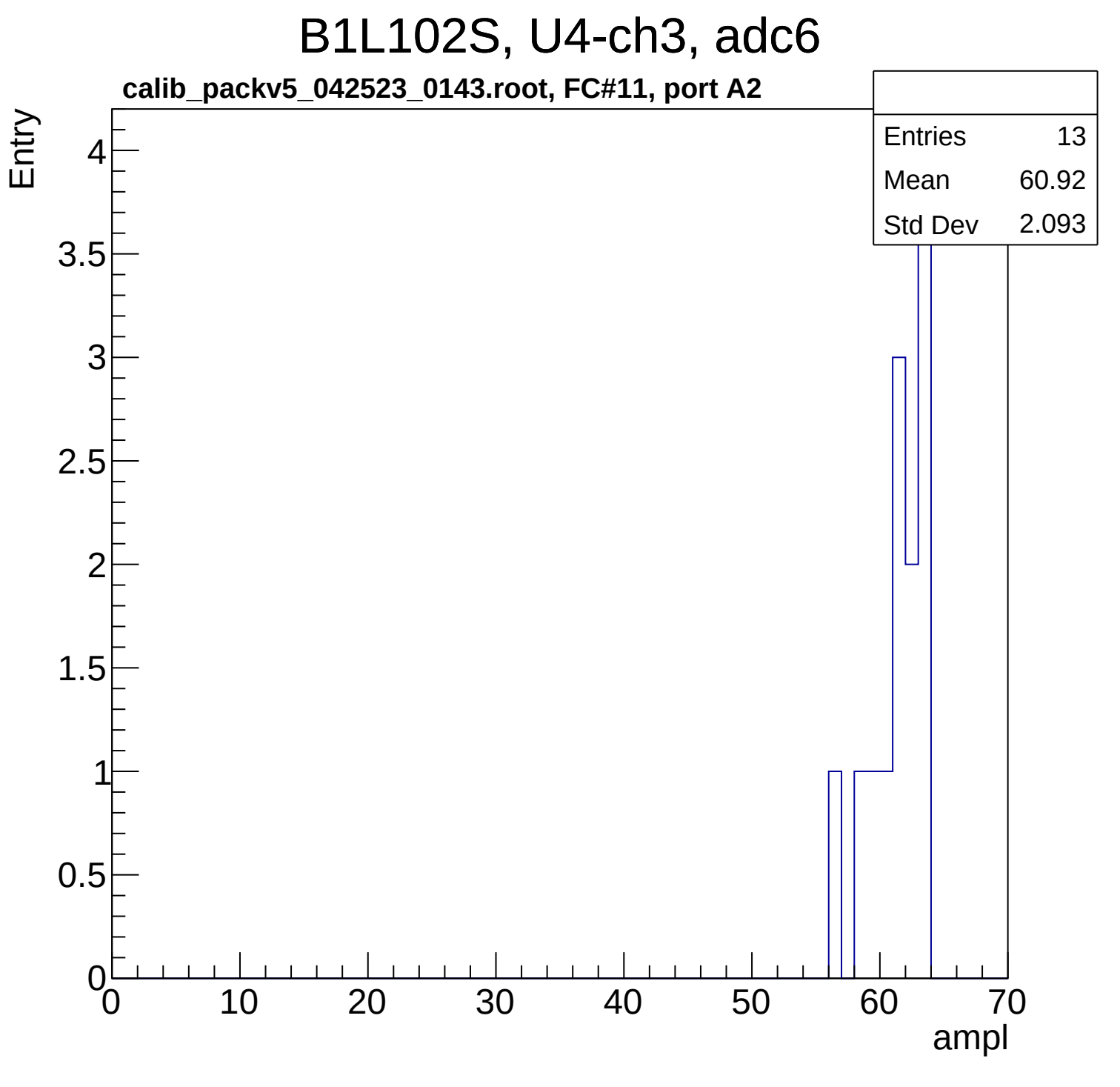
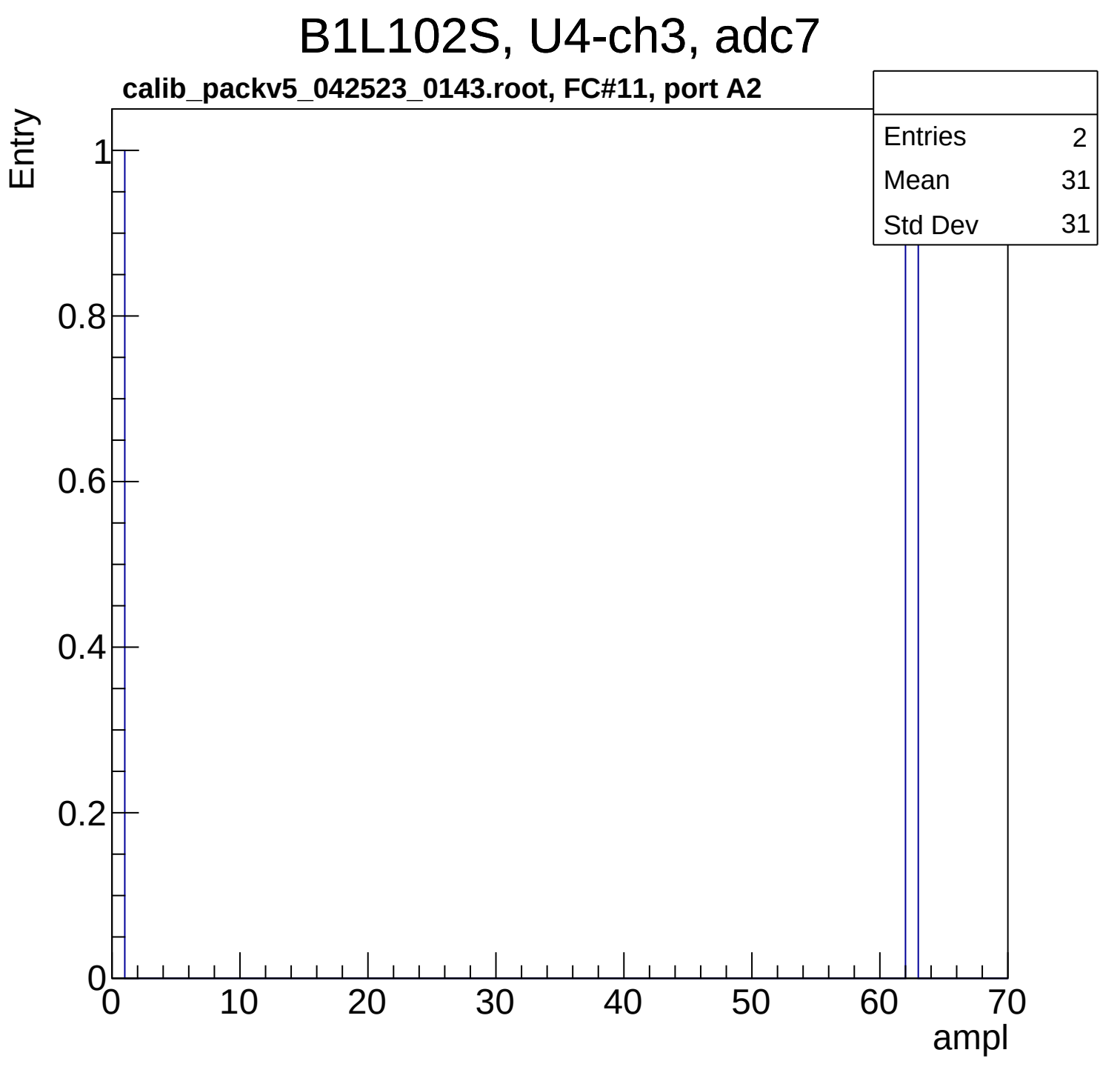
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch3, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 13
Mean 60.92
Std Dev 2.093
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U4-ch3, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 31
Std Dev 31
Entry
1
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0.6
0.4
0.2
0
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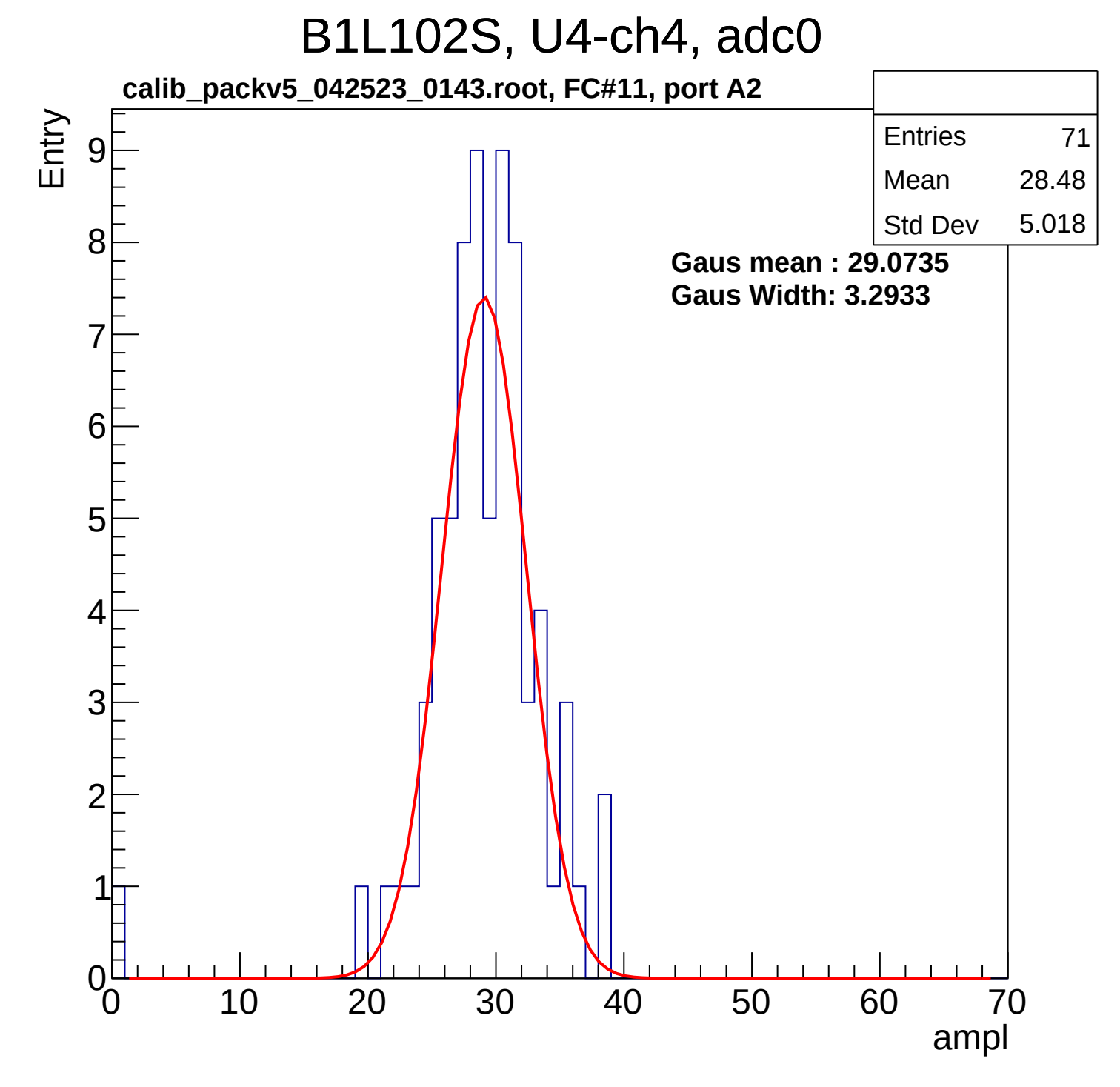
70
ampl


B1L102S, U4-ch4, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 28.48
Std Dev 5.018
Gaus mean : 29.0735
Gaus Width: 3.2933
Entry
ampl
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2
3
4
5
6
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8
9
0
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60
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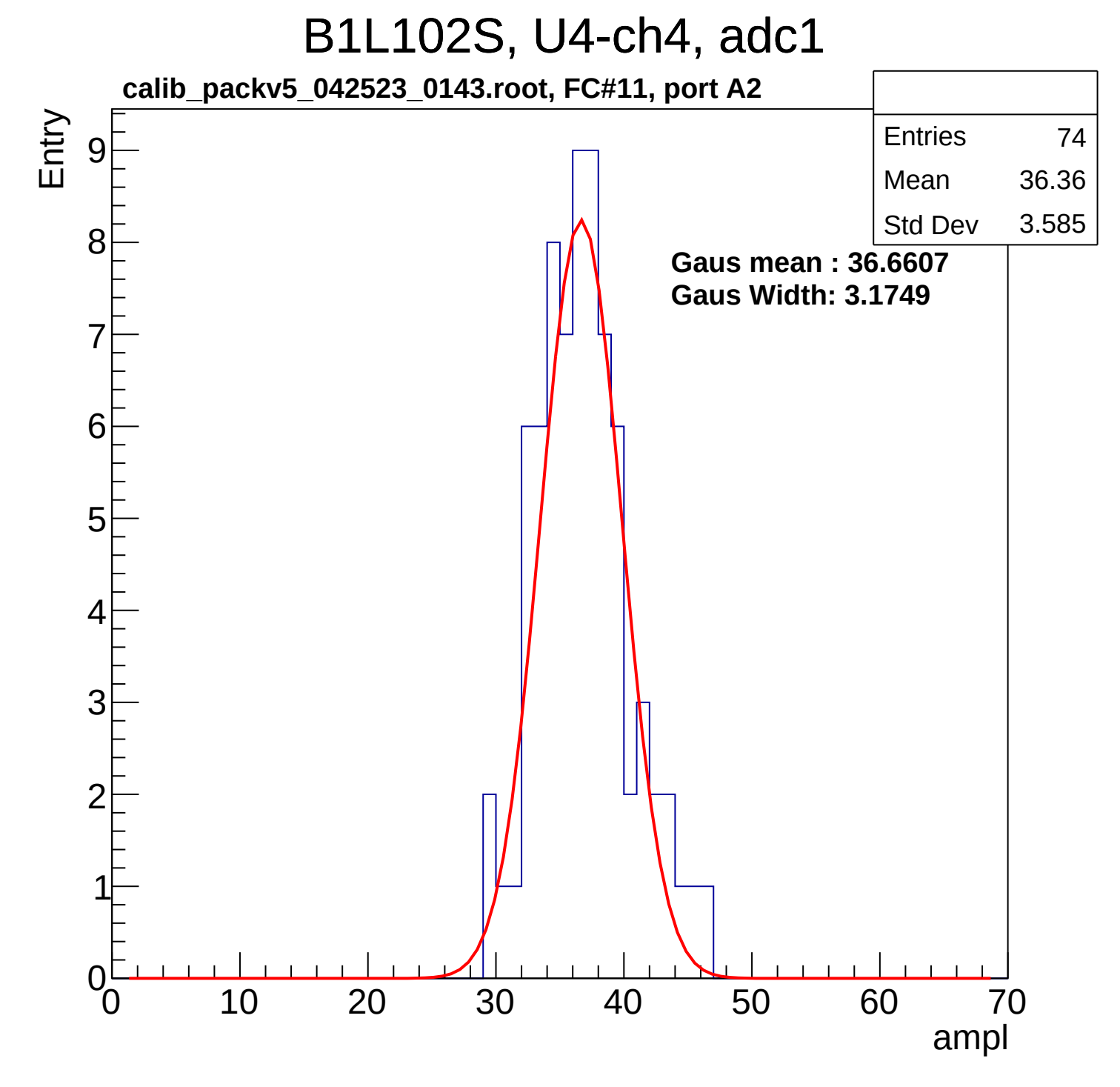
B1L102S, U4-ch4, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 36.36
Std Dev 3.585
Gaus mean : 36.6607
Gaus Width: 3.1749
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
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40
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60
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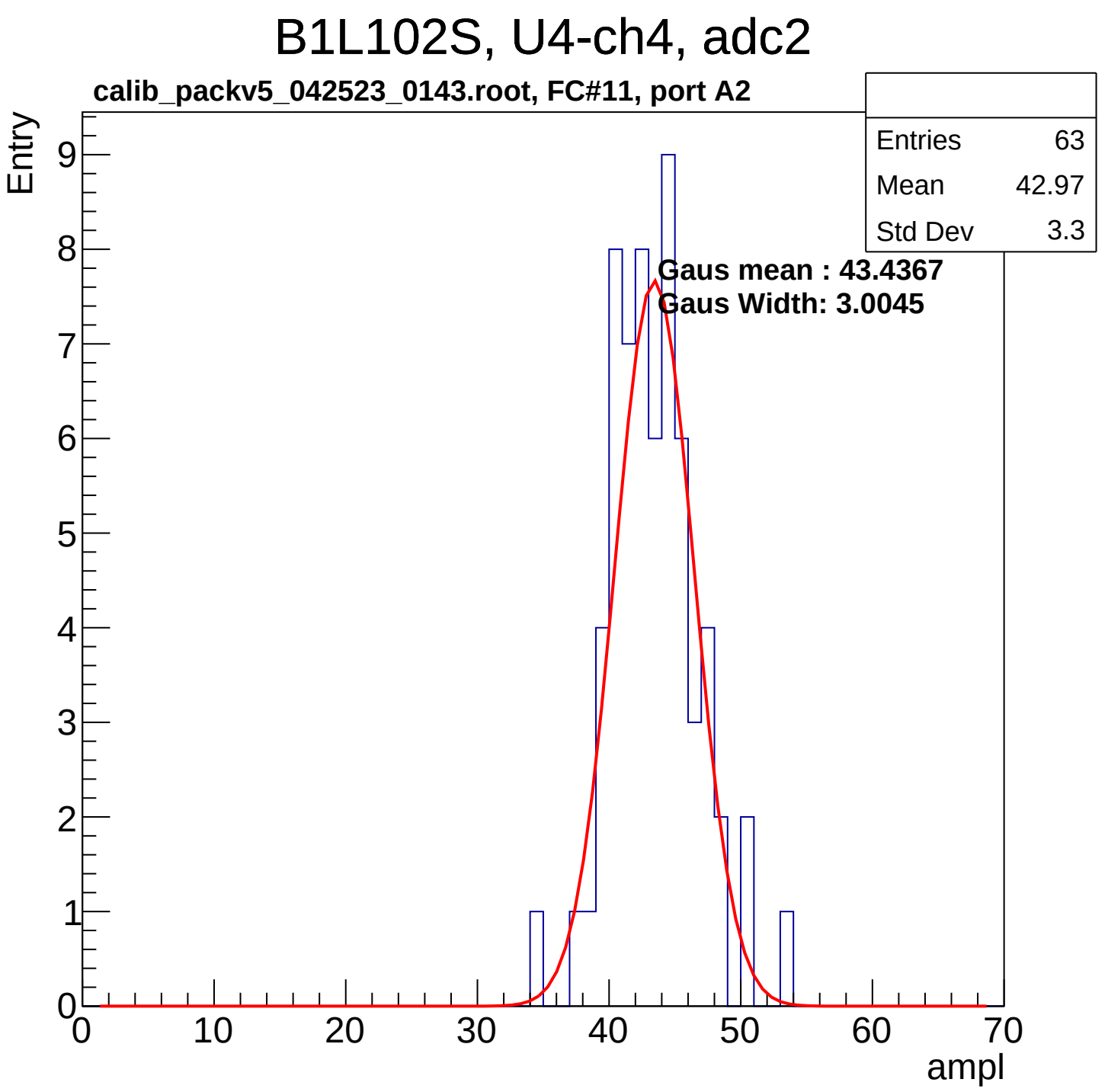
B1L102S, U4-ch4, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 42.97
Std Dev 3.3
Gaus mean : 43.4367
Gaus Width: 3.0045
Entry
ampl
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2
3
4
5
6
7
8
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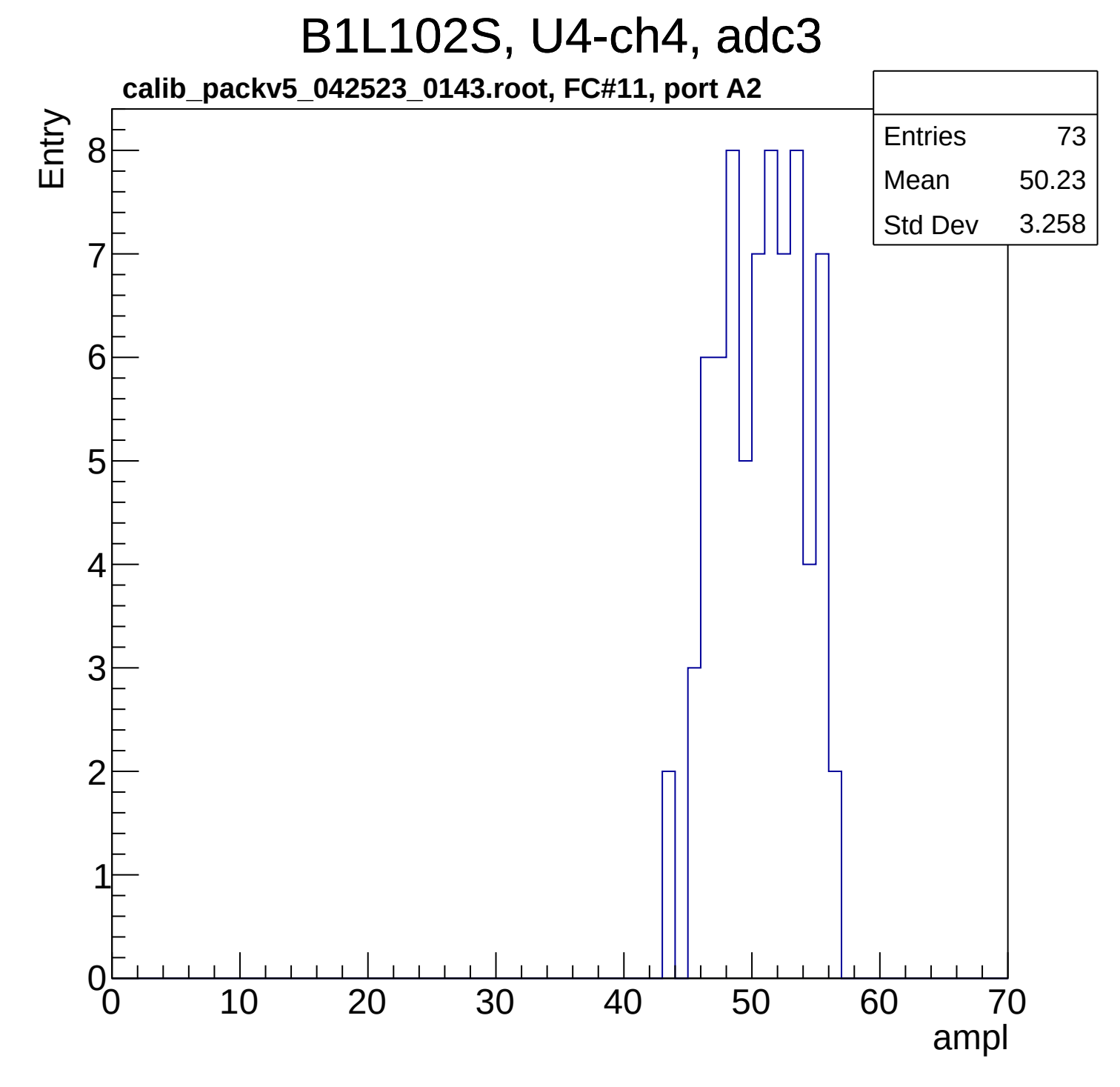
B1L102S, U4-ch4, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 50.23
Std Dev 3.258
Entry
ampl
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1
2
3
4
5
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0
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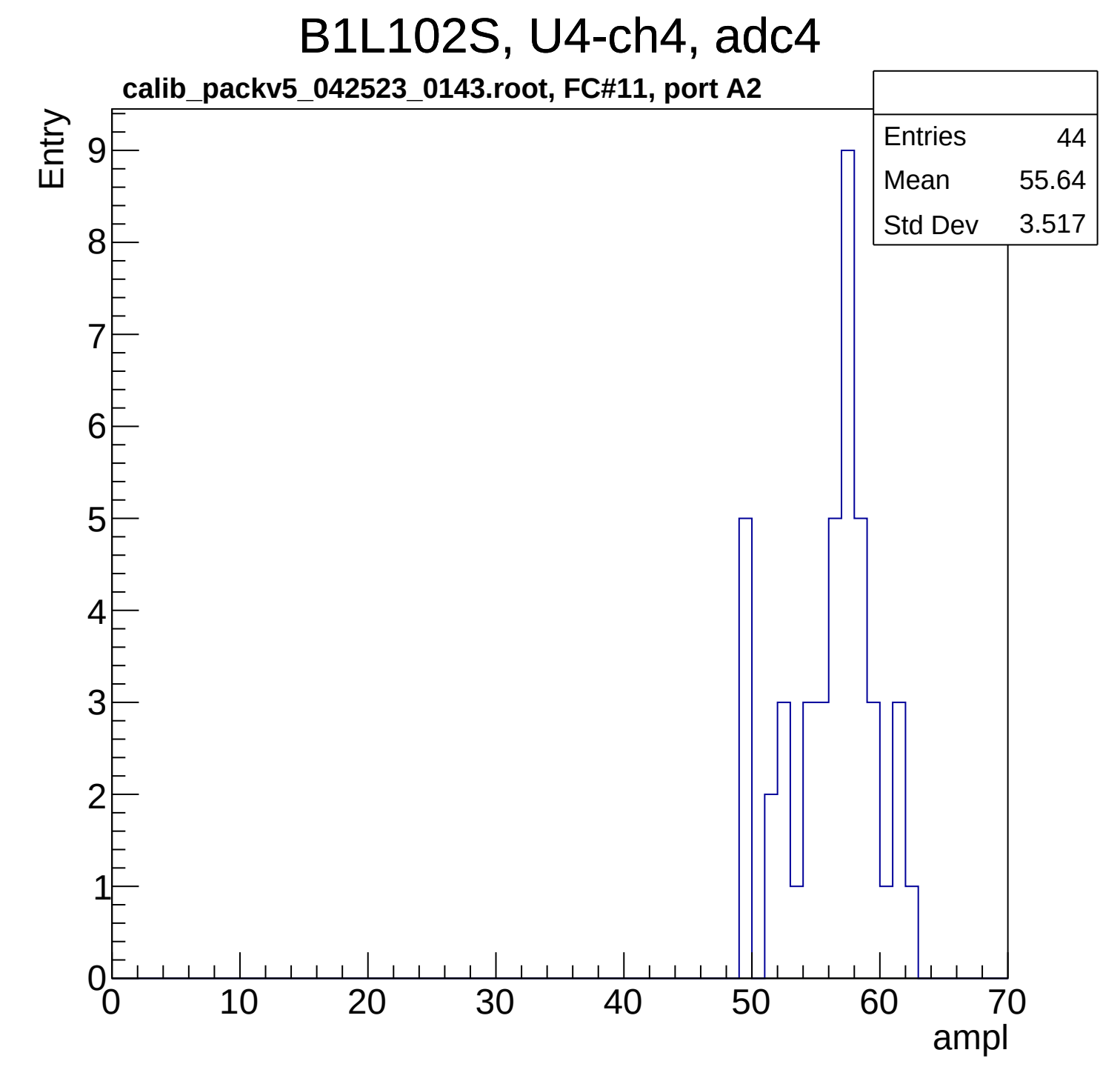
B1L102S, U4-ch4, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 44
Mean 55.64
Std Dev 3.517
Entry
ampl
0
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2
3
4
5
6
7
8
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0
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60
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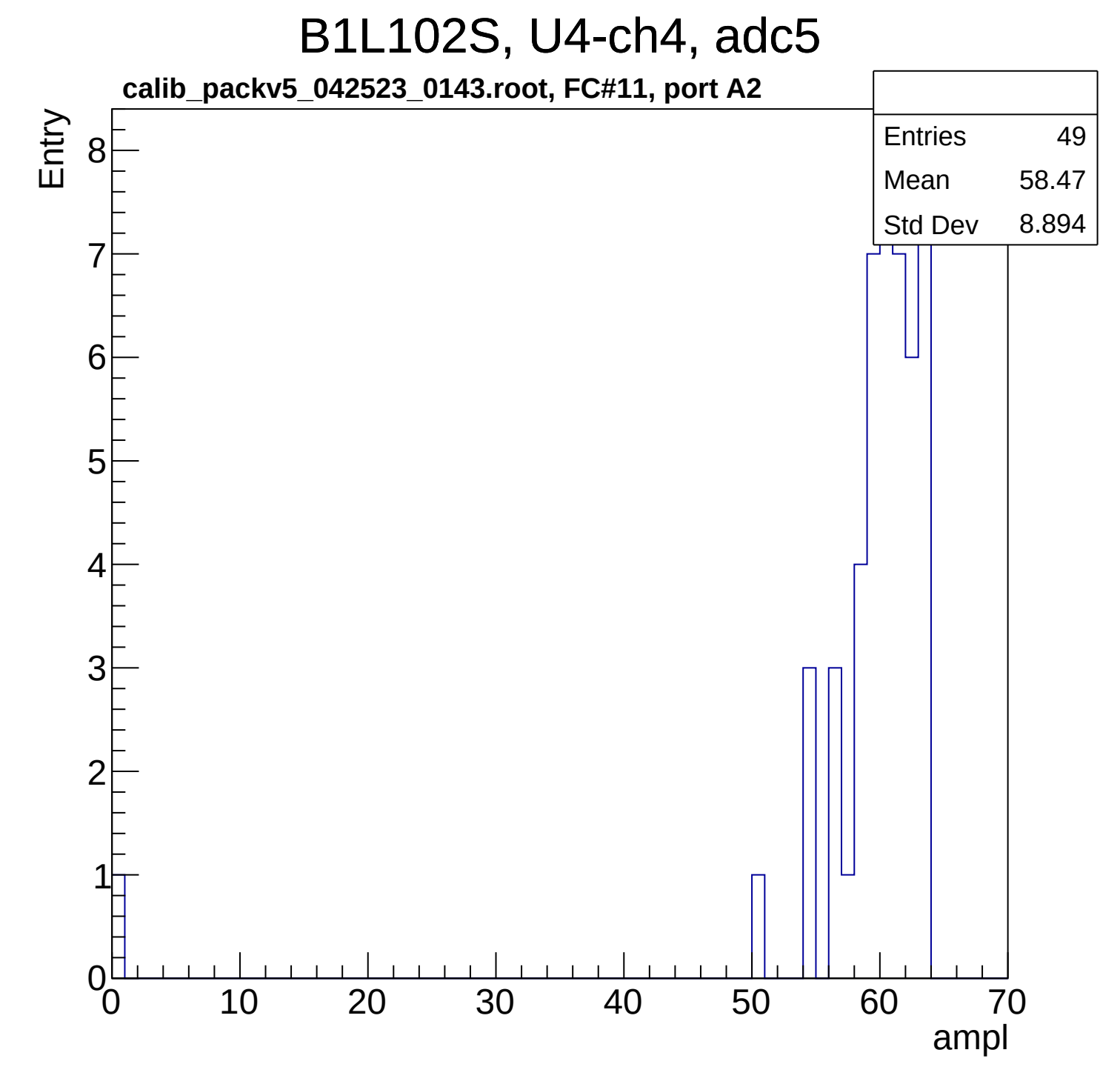
B1L102S, U4-ch4, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 58.47
Std Dev 8.894
Entry
ampl
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2
3
4
5
6
7
8
0
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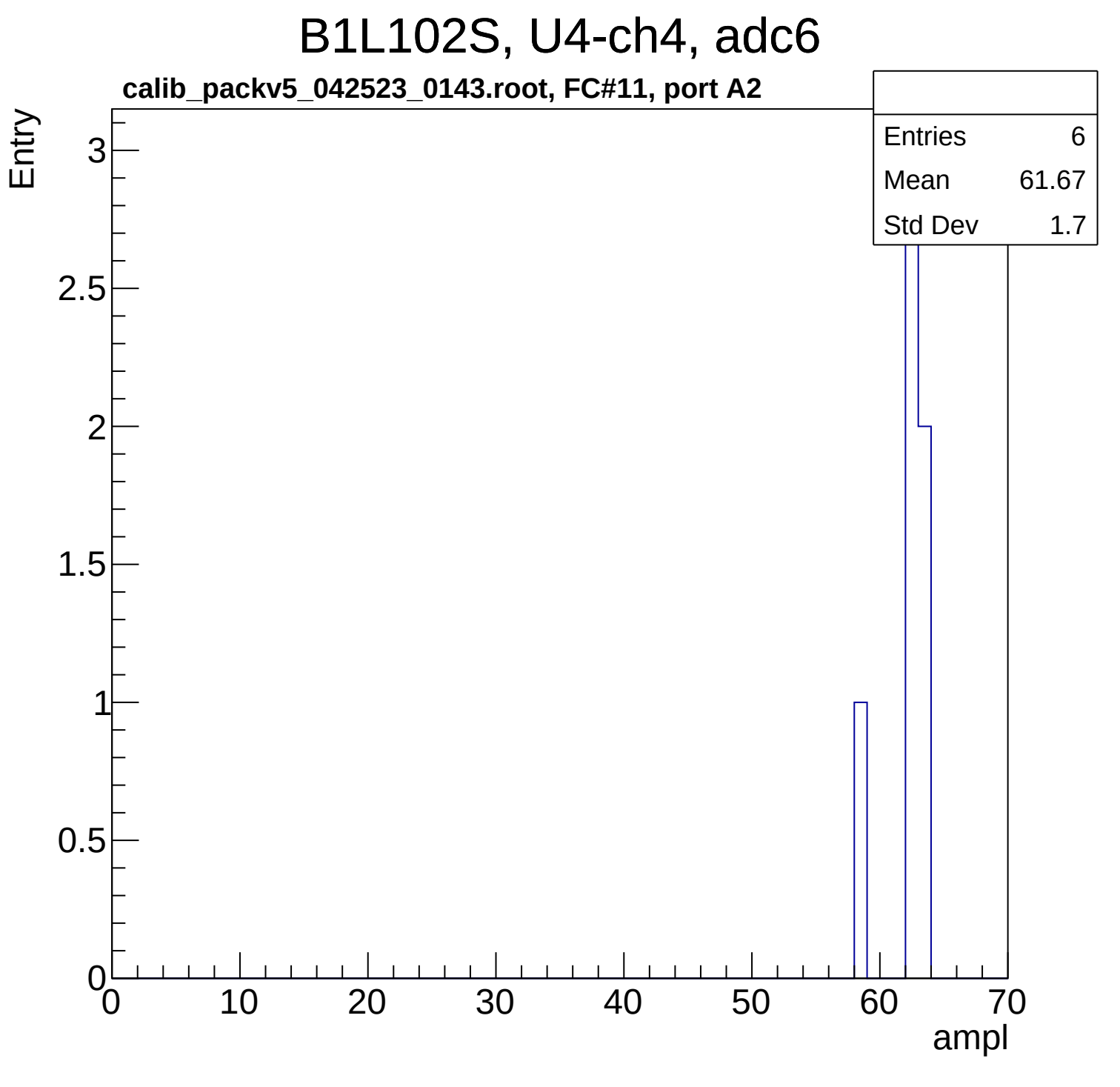
B1L102S, U4-ch4, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 6
Mean 61.67
Std Dev 1.7
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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40
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60
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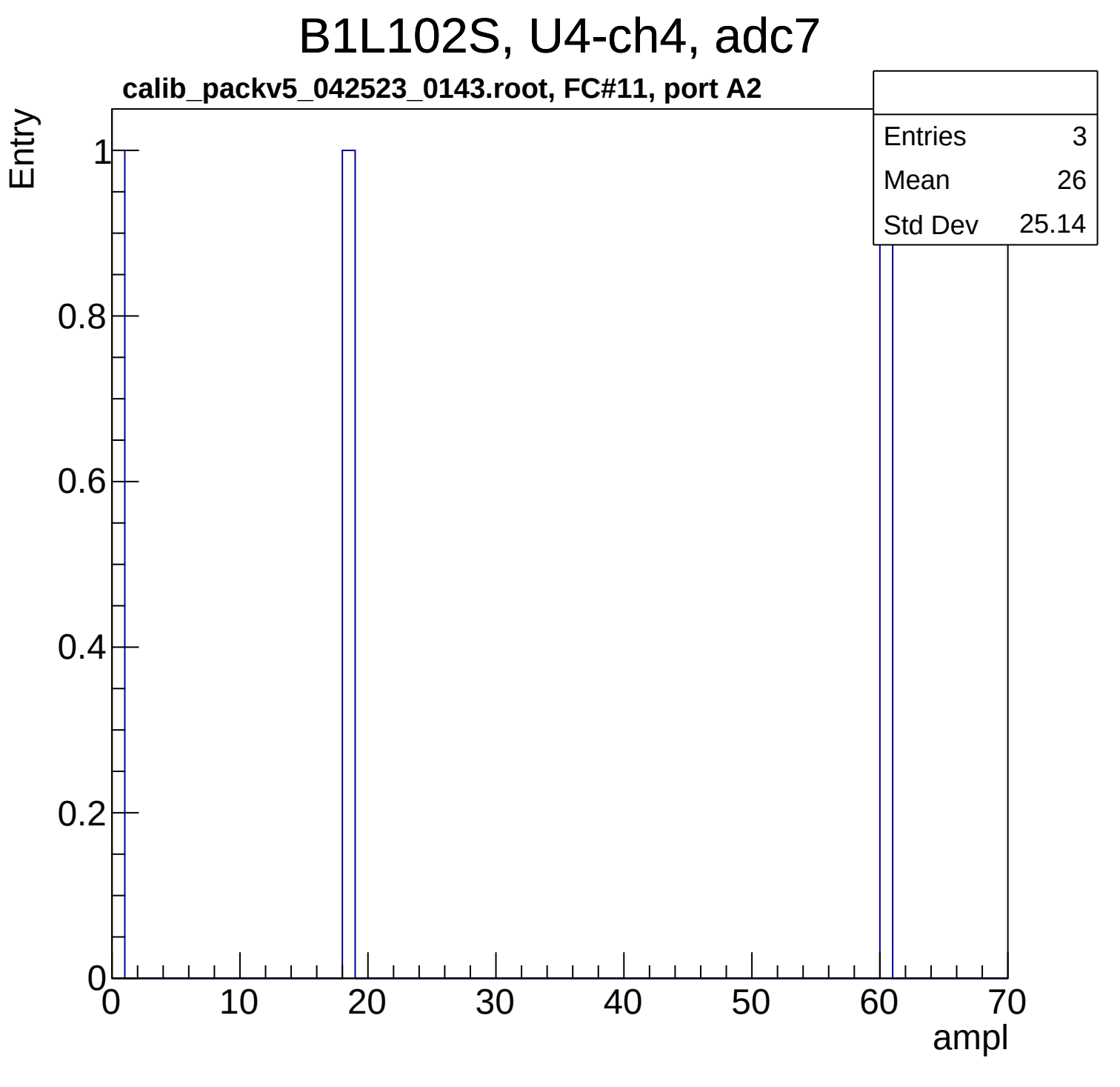
B1L102S, U4-ch4, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 26
Std Dev 25.14
Entry
ampl
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0.2
0.4
0.6
0.8
1
0
10
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30
40
50
60
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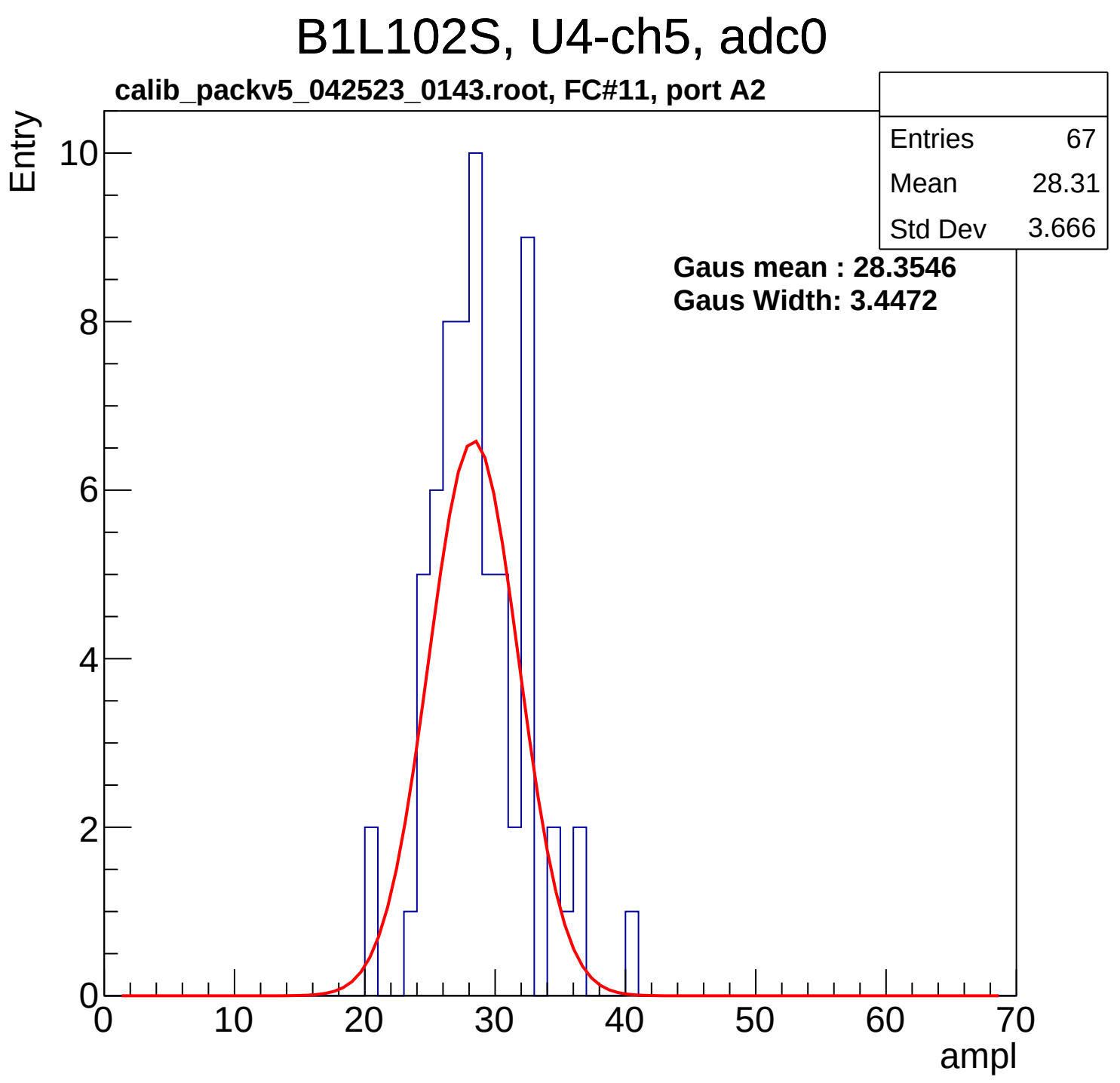
B1L102S, U4-ch5, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 28.31
Std Dev 3.666
Gaus mean : 28.3546
Gaus Width: 3.4472
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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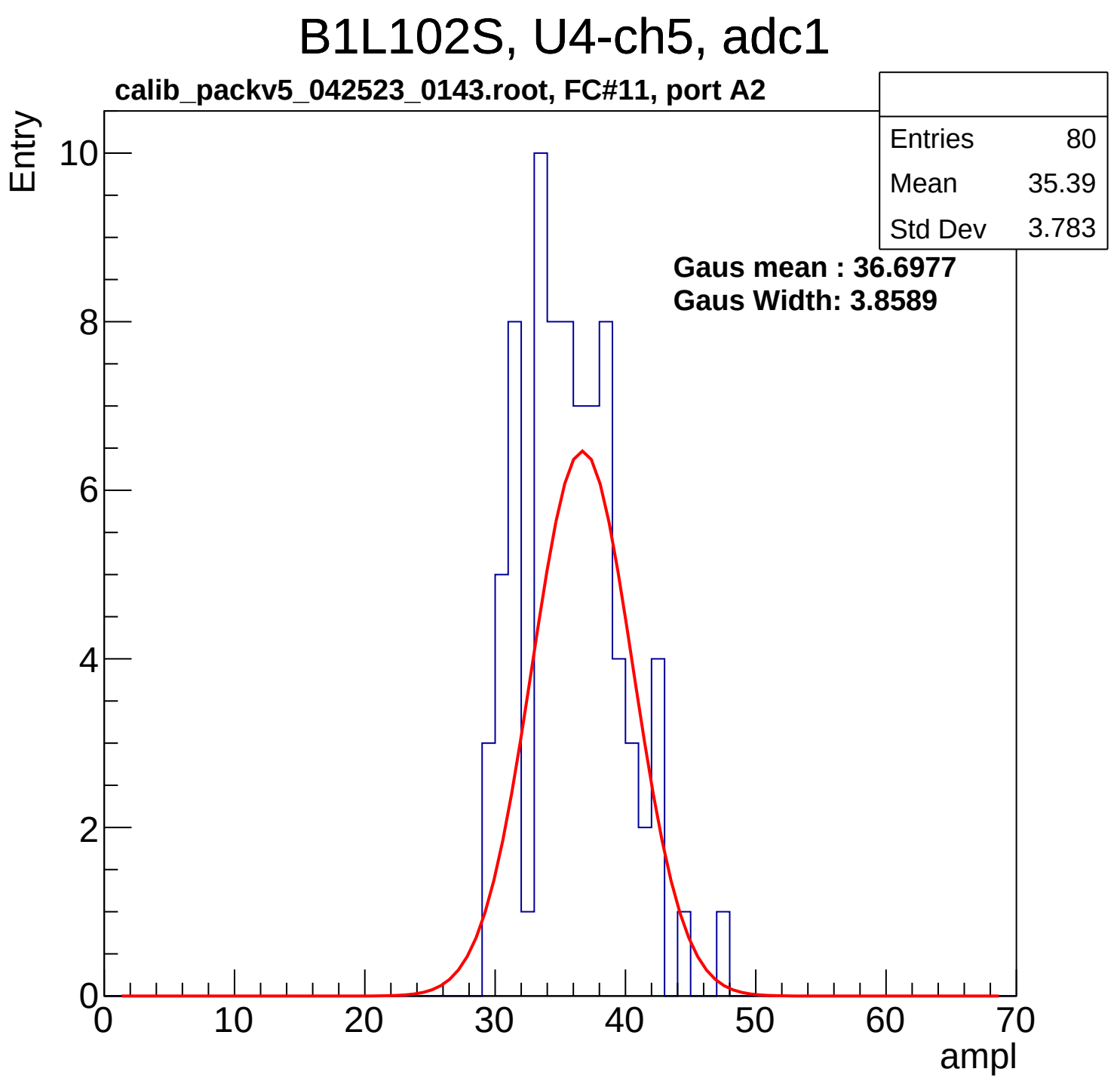
B1L102S, U4-ch5, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 80
Mean 35.39
Std Dev 3.783
Gaus mean : 36.6977
Gaus Width: 3.8589
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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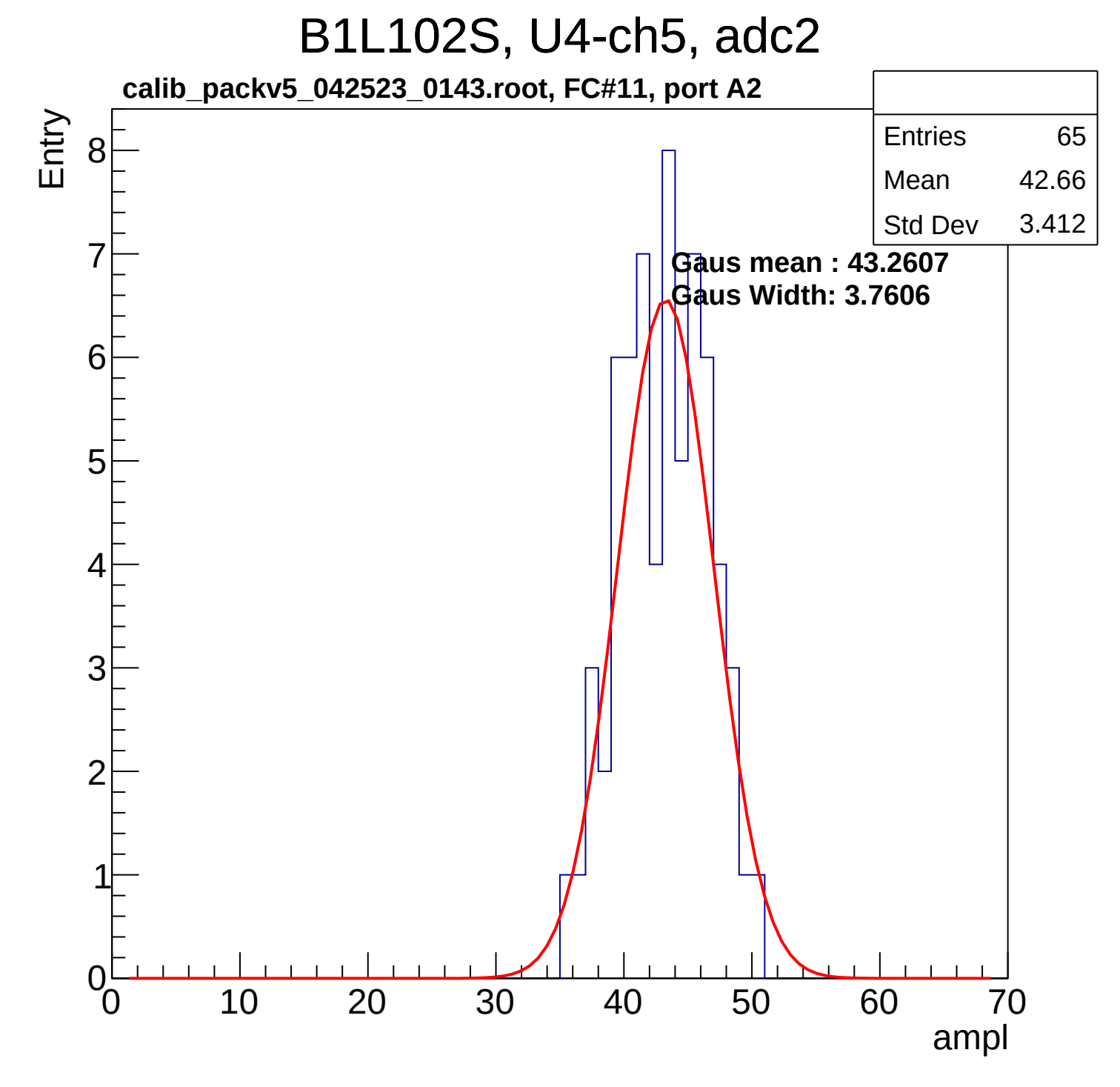
B1L102S, U4-ch5, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 42.66
Std Dev 3.412
Gaus mean : 43.2607
Gaus Width: 3.7606
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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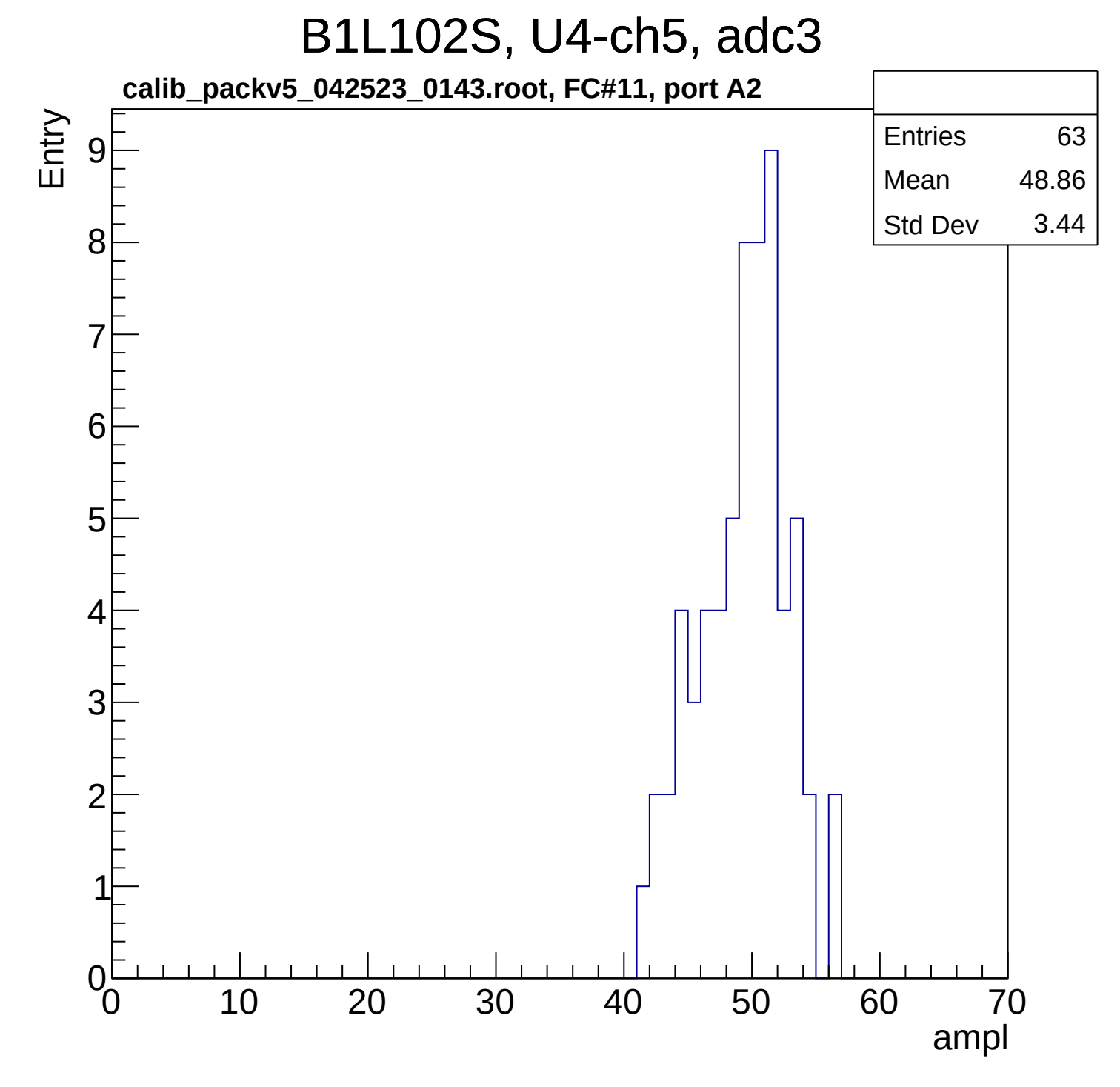
B1L102S, U4-ch5, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 48.86
Std Dev 3.44
Entry
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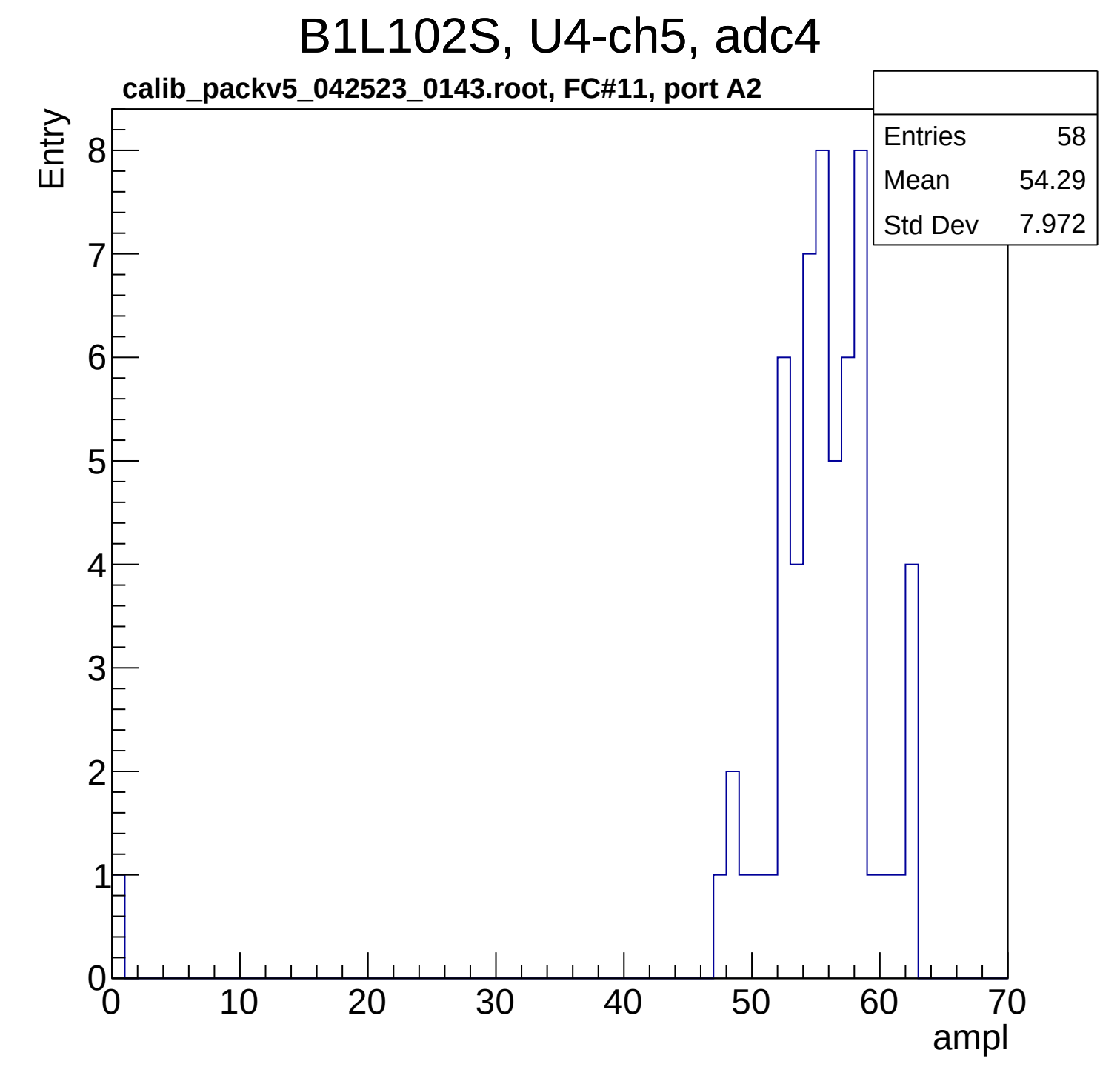
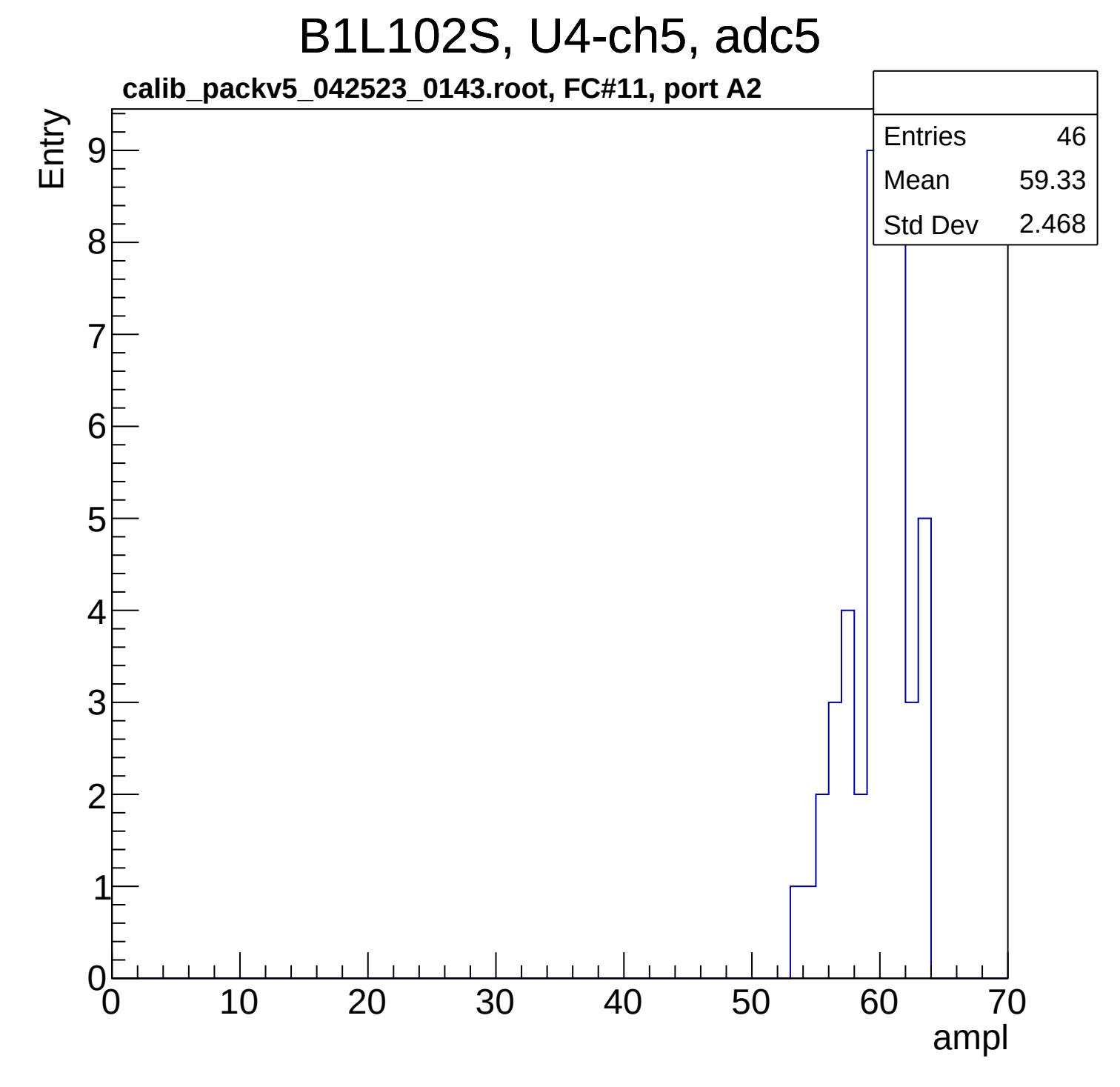
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch5, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 54.29
Std Dev 7.972
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch5, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 46
Mean 59.33
Std Dev 2.468
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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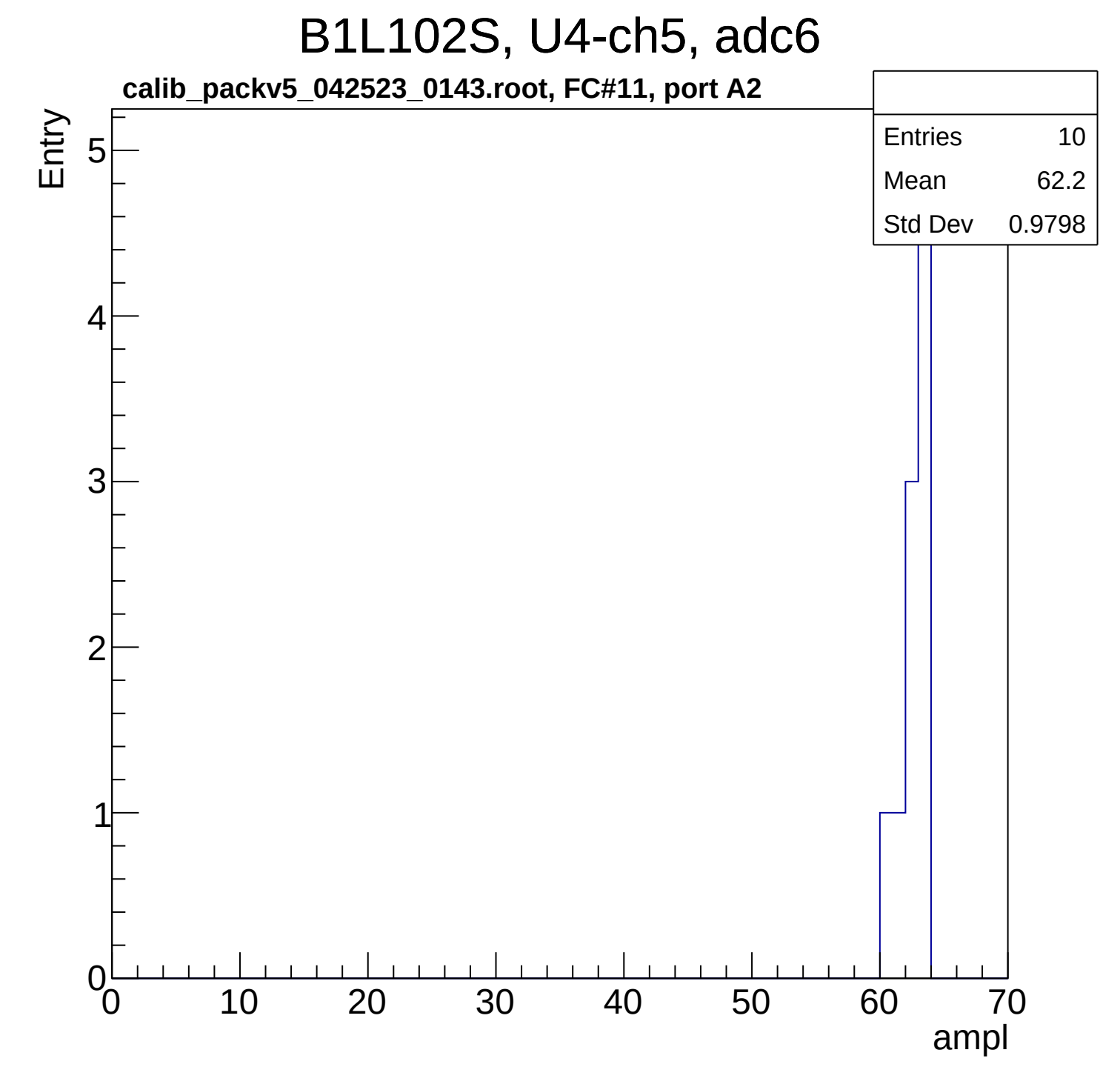
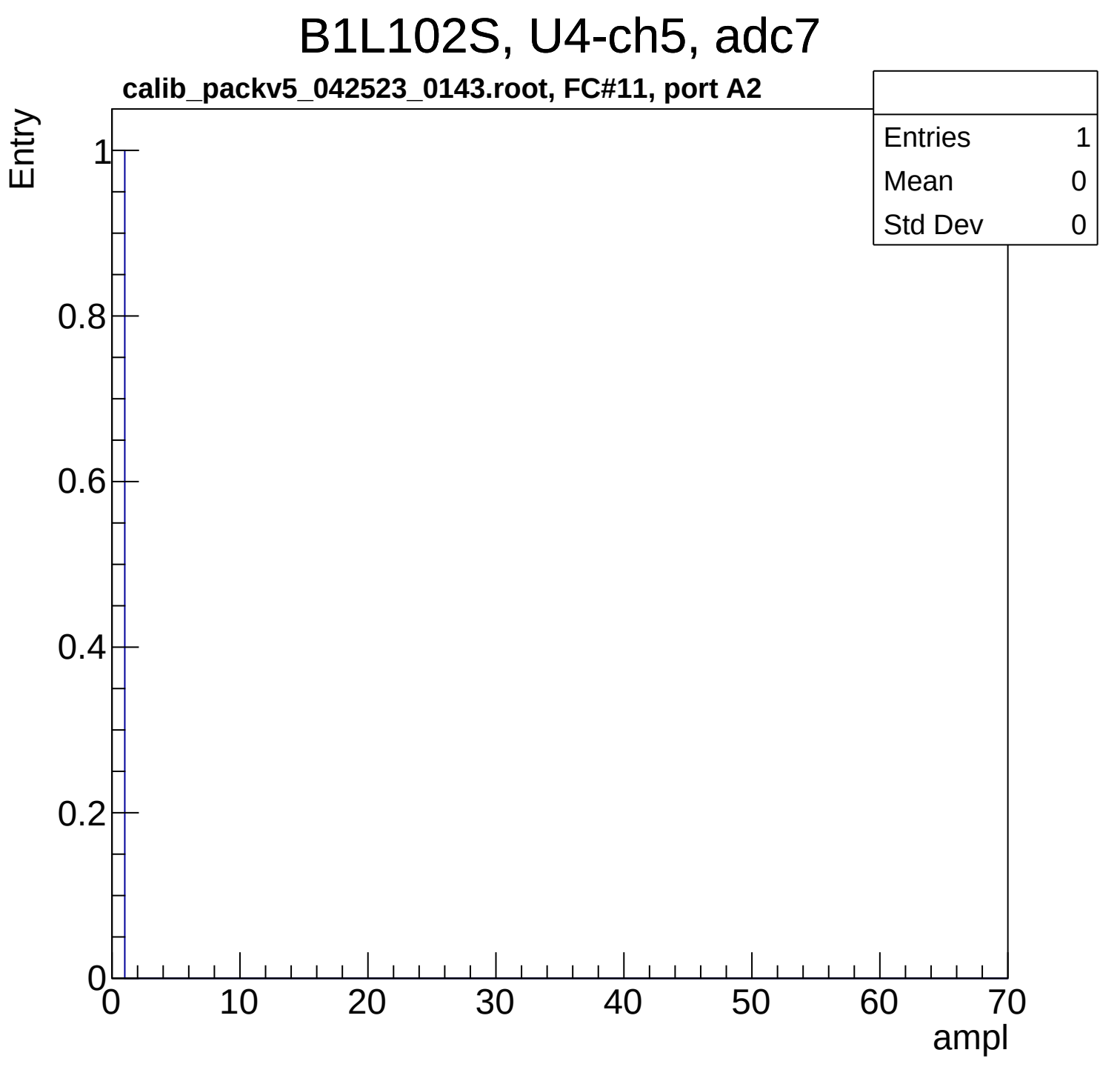
40
50
60
70


B1L102S, U4-ch5, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 10
Mean 62.2
Std Dev 0.9798
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch5, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
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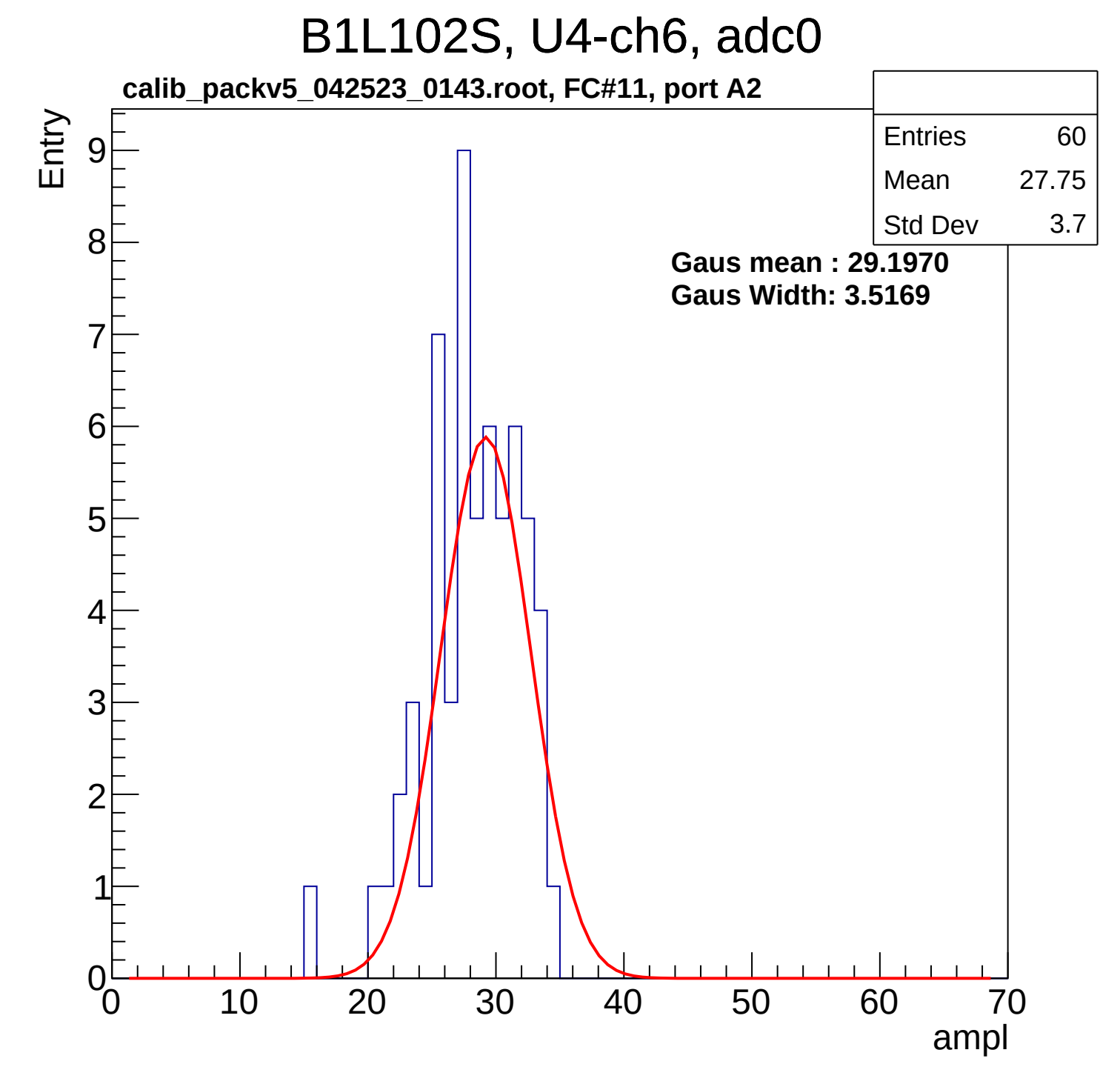
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch6, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 27.75
Std Dev 3.7
Gaus mean : 29.1970
Gaus Width: 3.5169
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
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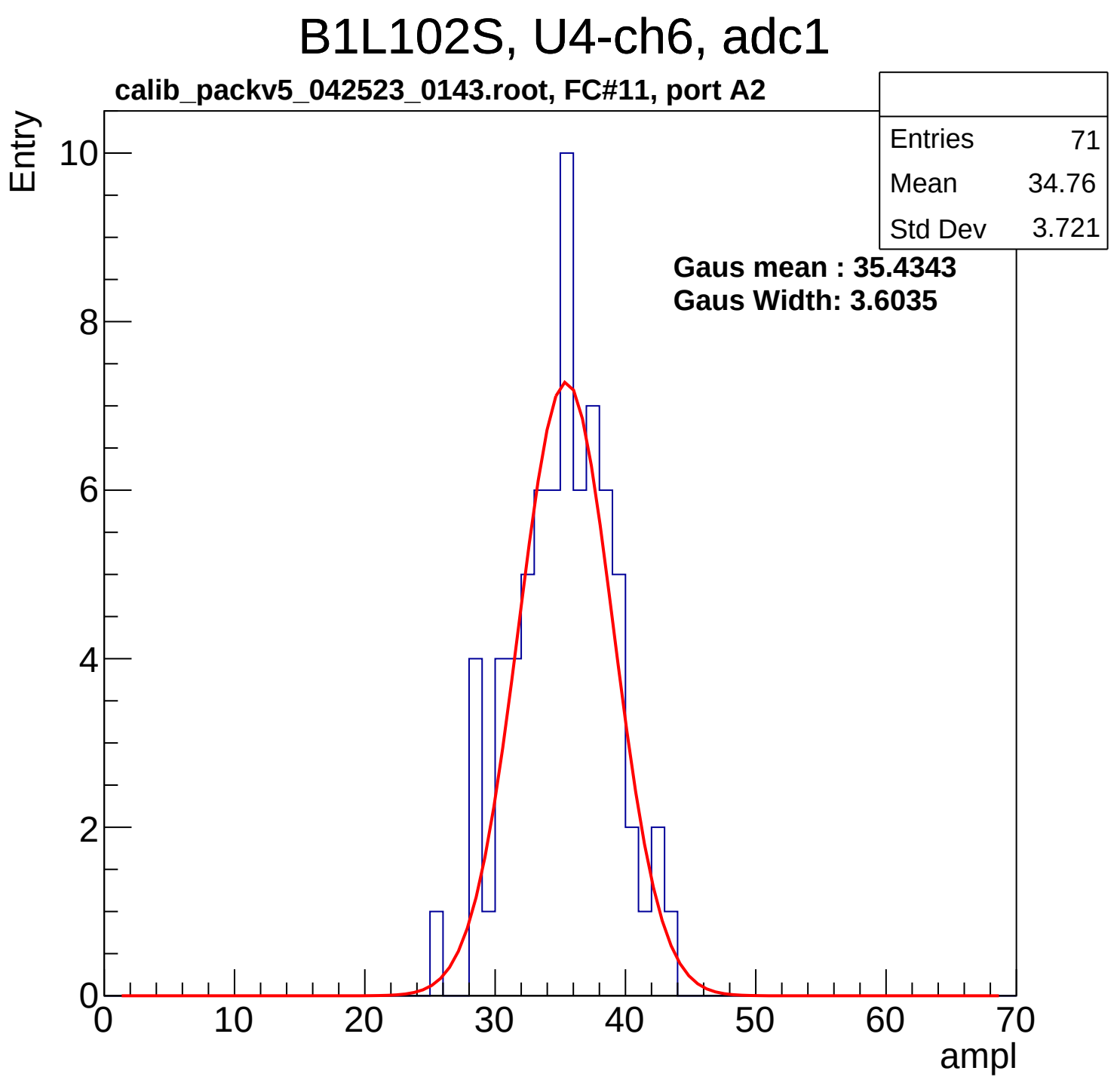
40
50
60
70


B1L102S, U4-ch6, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 34.76
Std Dev 3.721
Gaus mean : 35.4343
Gaus Width: 3.6035
Entry
ampl
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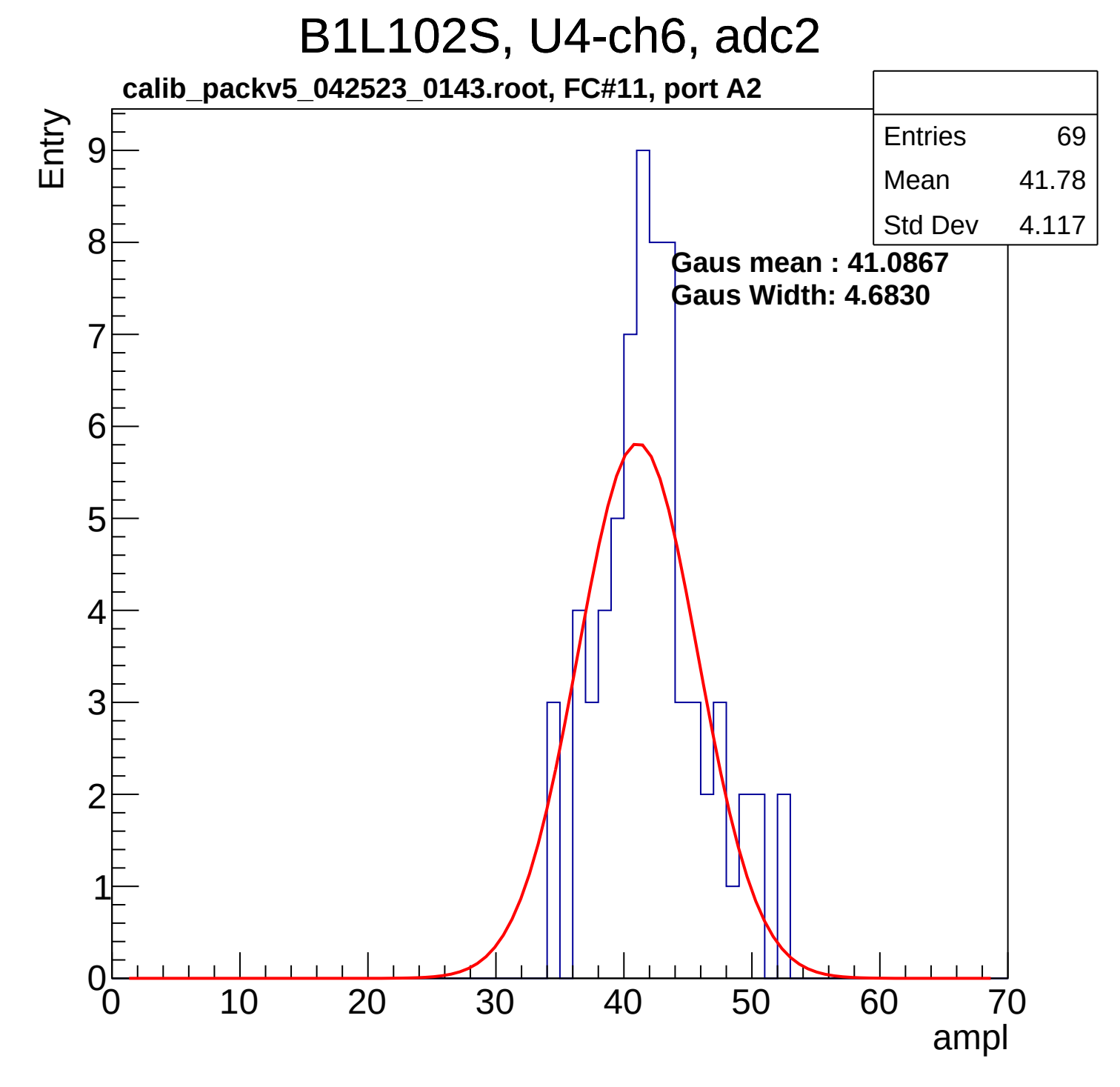
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch6, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 41.78
Std Dev 4.117
Gaus mean : 41.0867
Gaus Width: 4.6830
Entry
ampl
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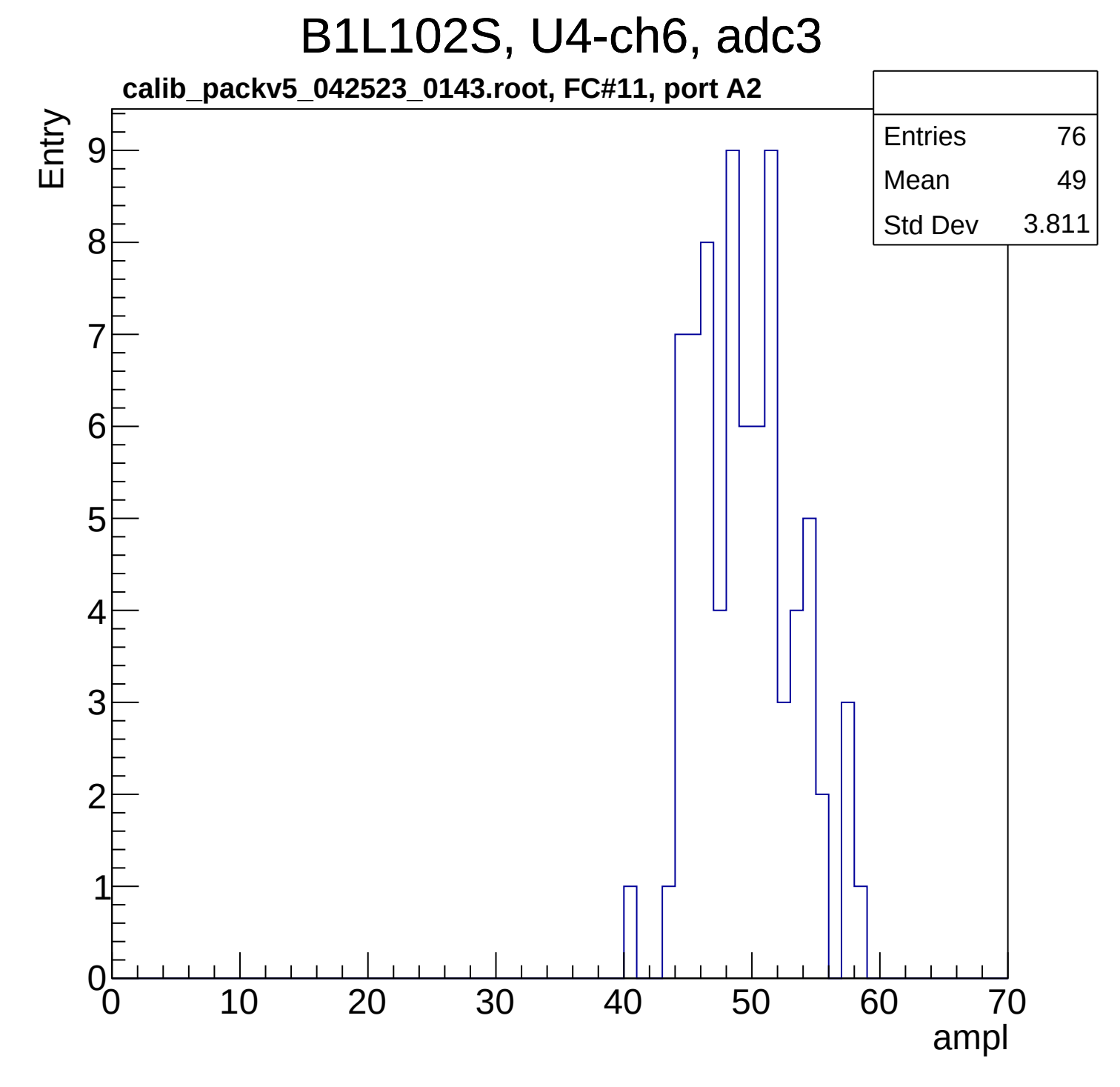
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L102S, U4-ch6, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 49
Std Dev 3.811
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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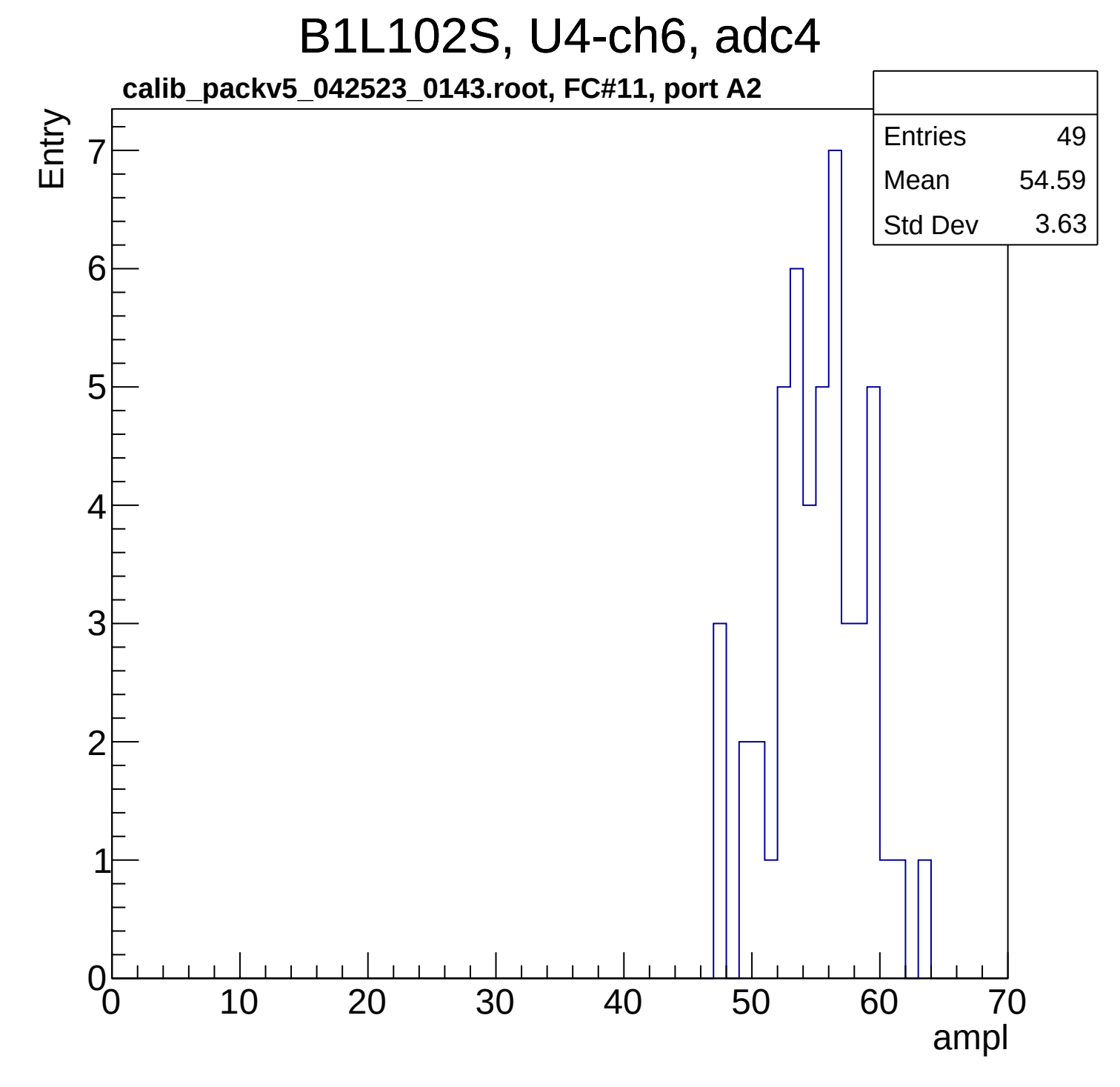
40
50
60
70


B1L102S, U4-ch6, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 54.59
Std Dev 3.63
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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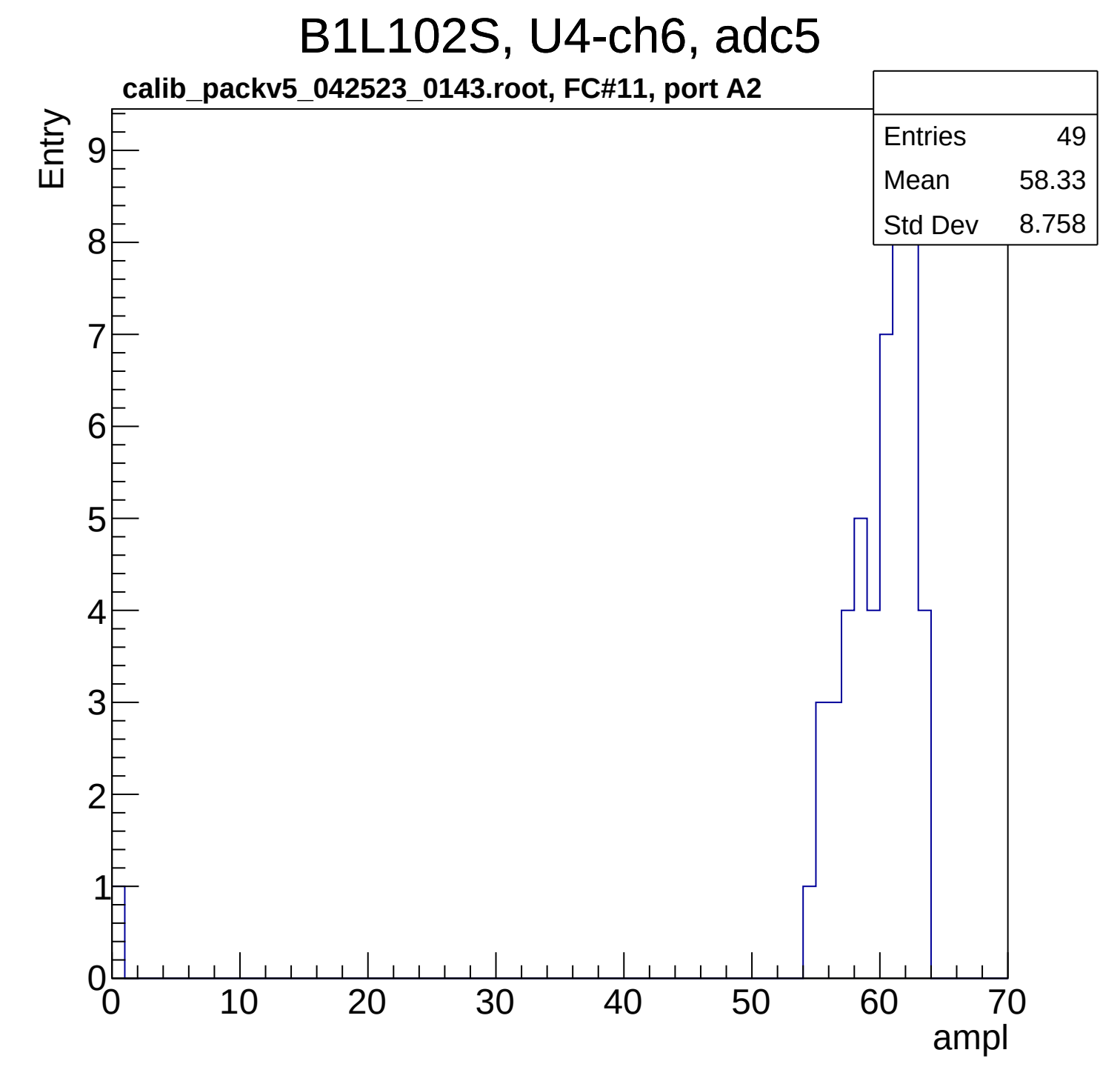
B1L102S, U4-ch6, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 58.33
Std Dev 8.758
Entry
ampl
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3
4
5
6
7
8
9
0
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60
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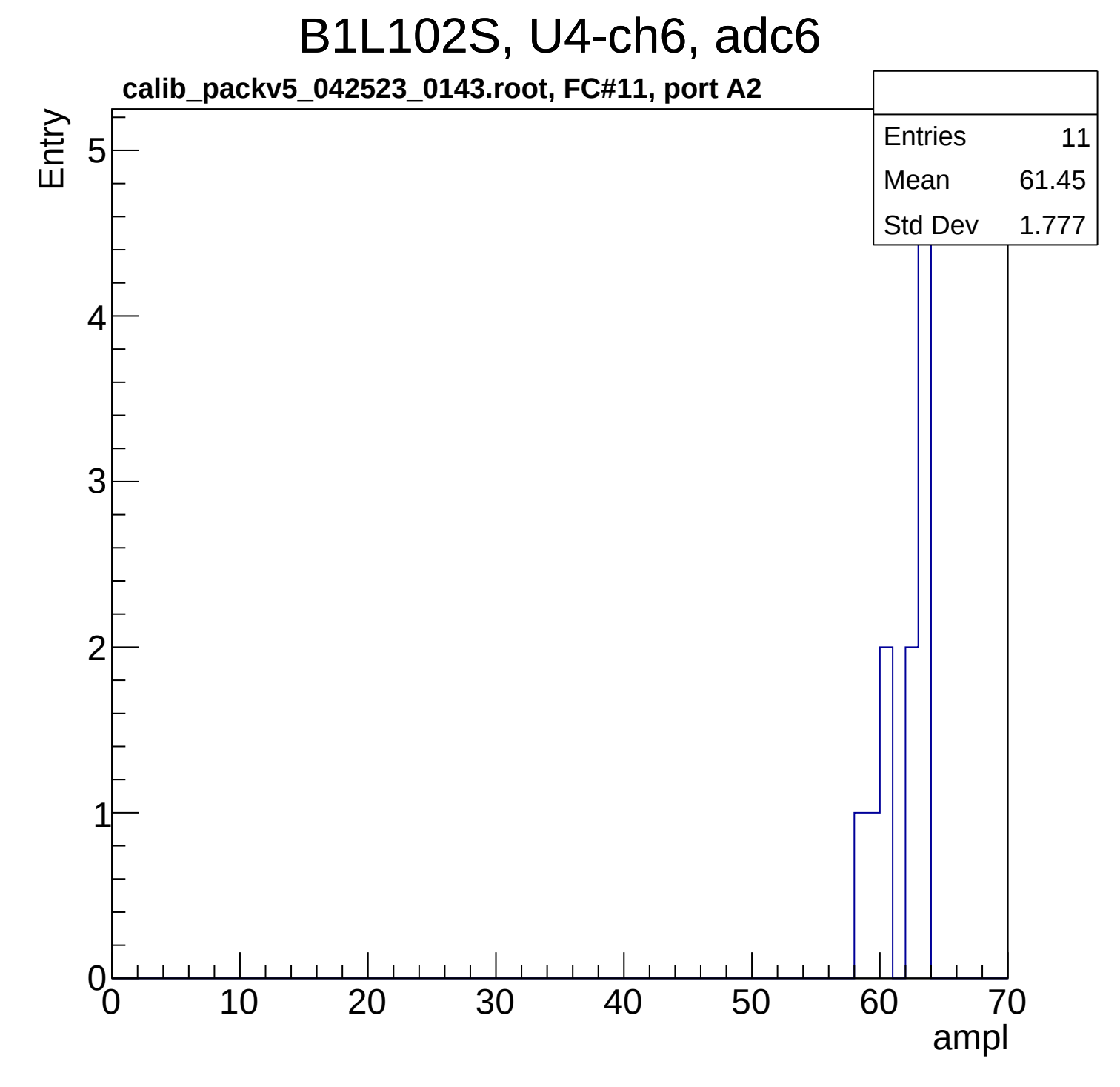
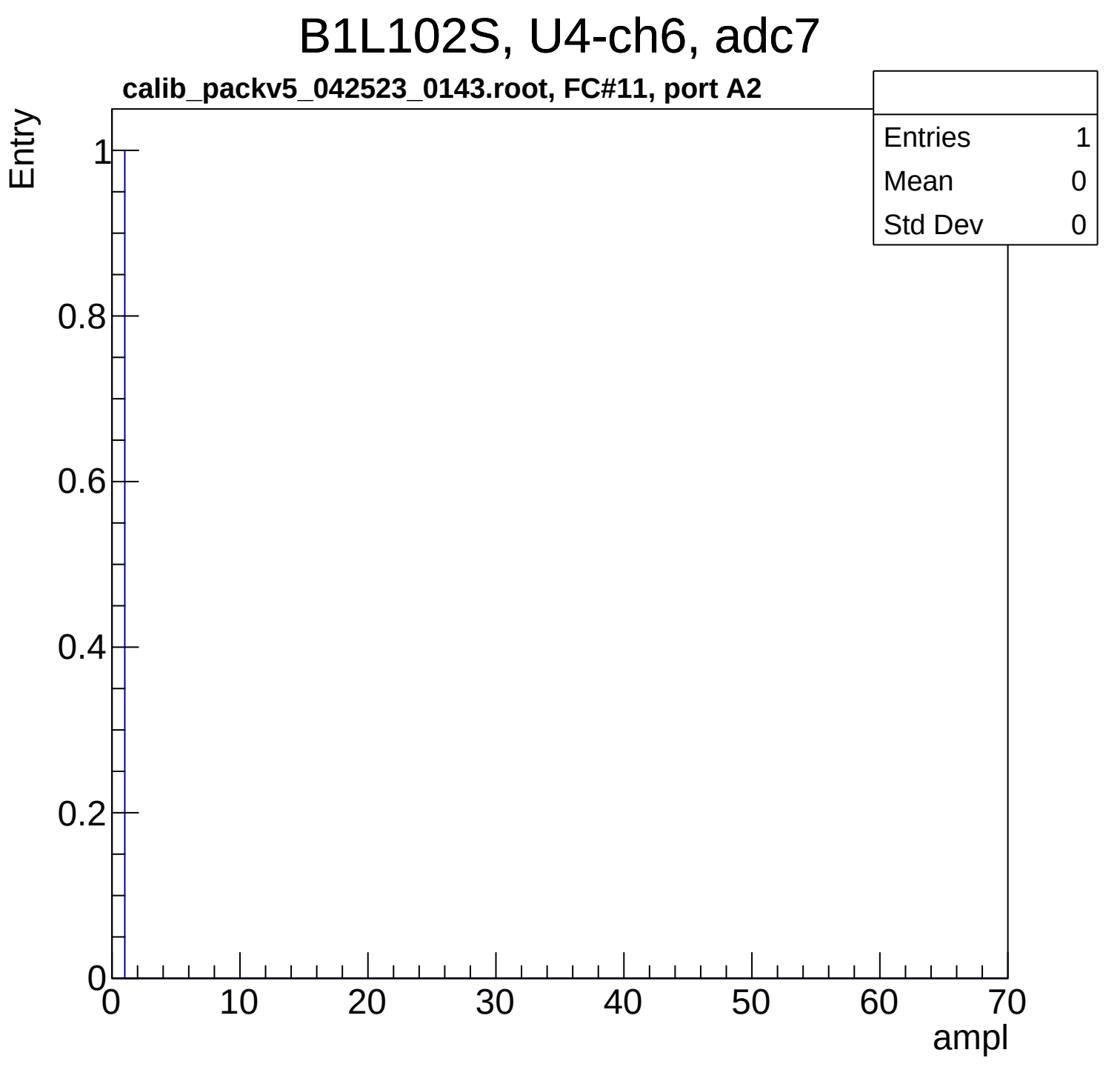

B1L102S, U4-ch6, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 11
Mean 61.45
Std Dev 1.777
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L102S, U4-ch6, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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0.6
0.4
0.2
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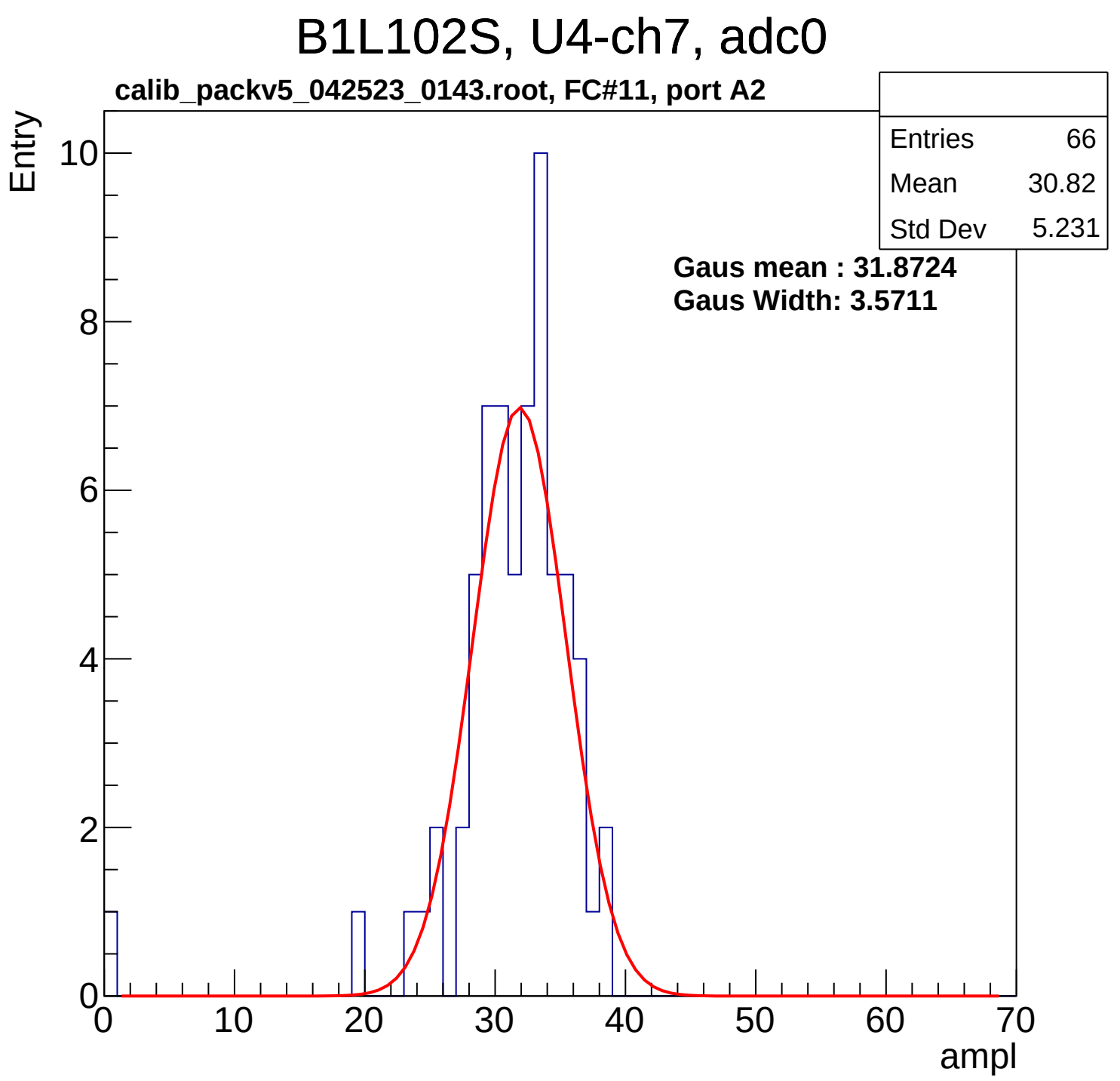
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch7, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 30.82
Std Dev 5.231
Gaus mean : 31.8724
Gaus Width: 3.5711
Entry
ampl
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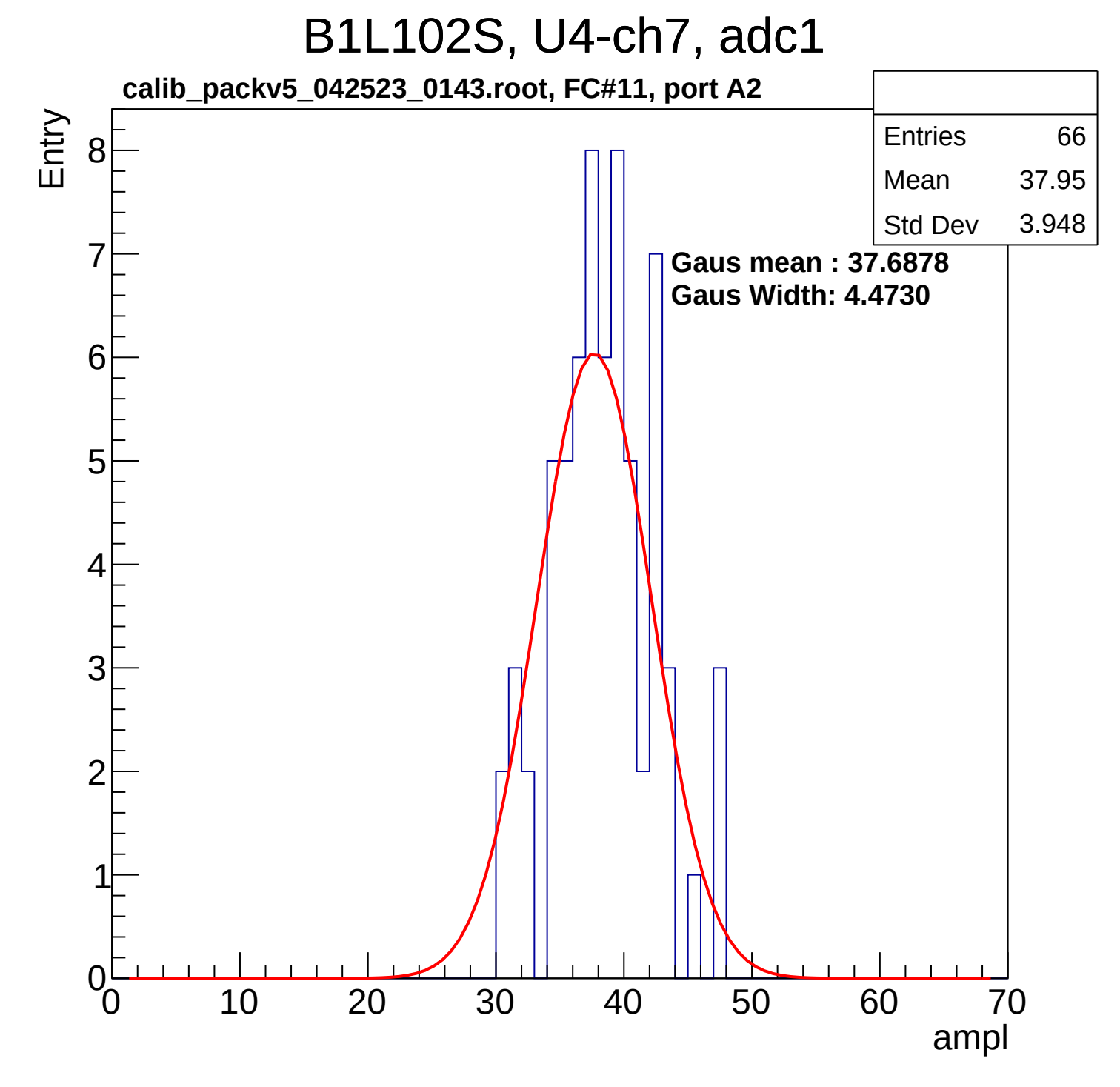
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch7, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 37.95
Std Dev 3.948
Gaus mean : 37.6878
Gaus Width: 4.4730
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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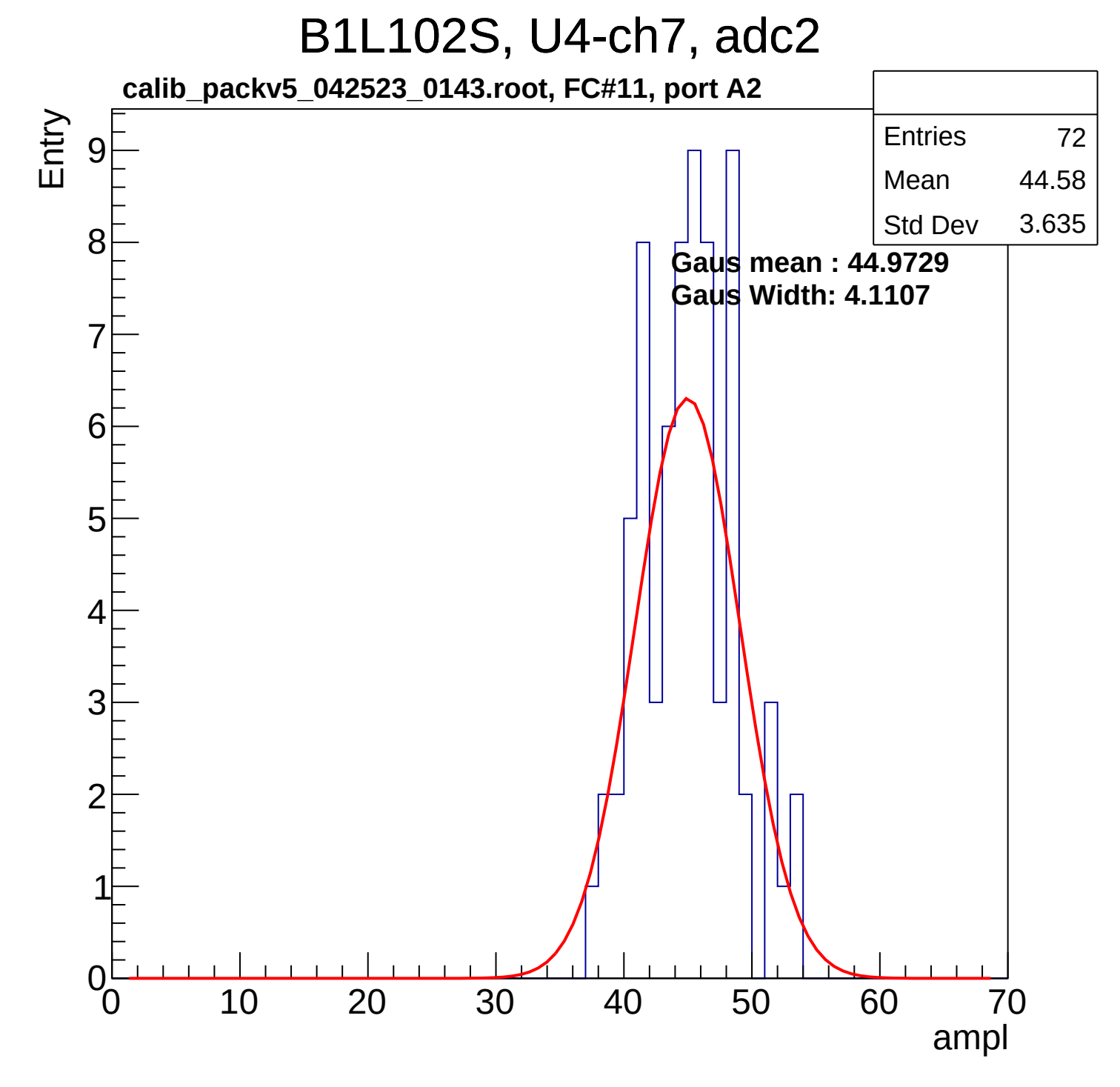
B1L102S, U4-ch7, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 72
Mean 44.58
Std Dev 3.635
Gaus mean : 44.9729
Gaus Width: 4.1107
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
50
60
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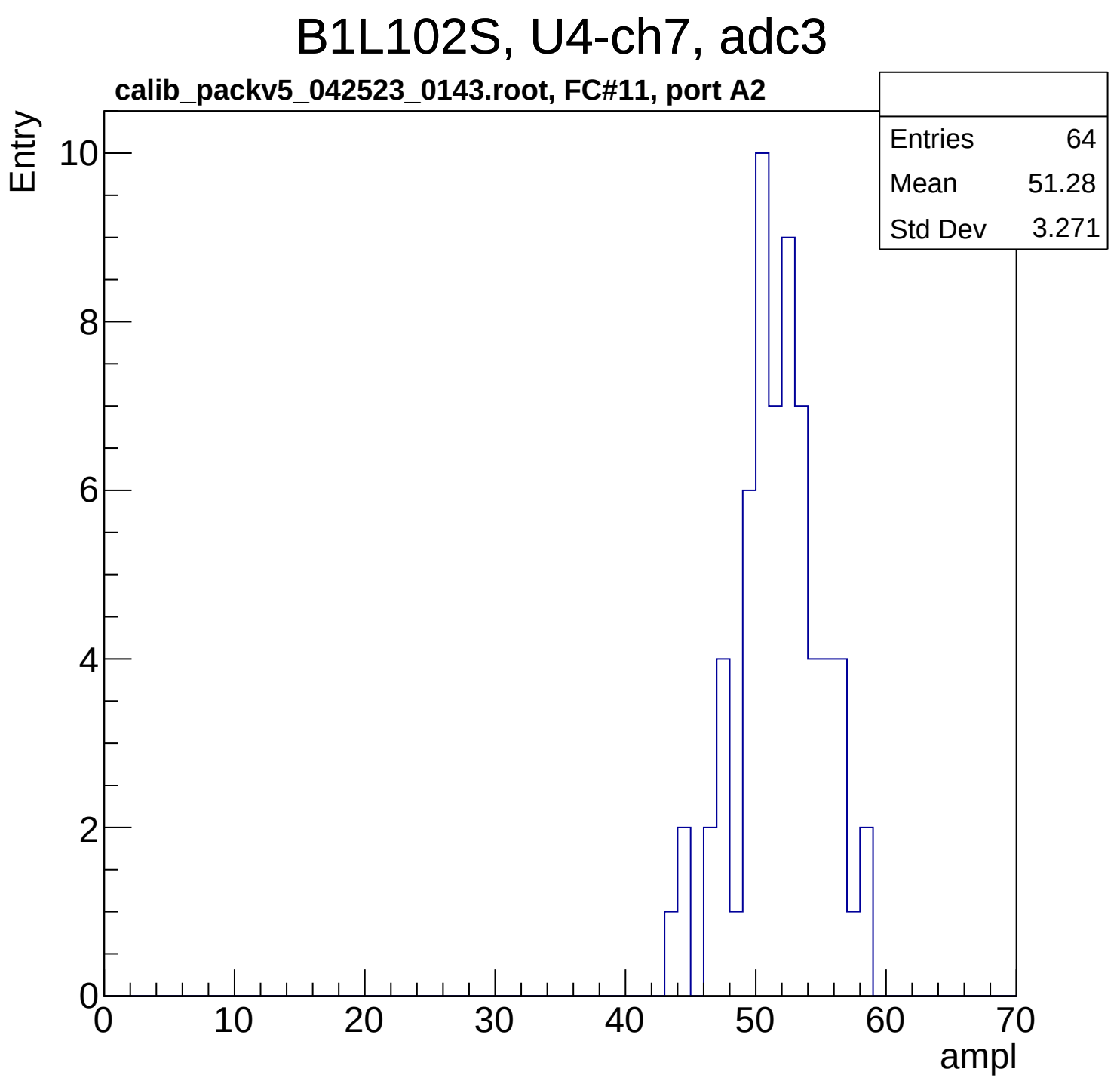
B1L102S, U4-ch7, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 51.28
Std Dev 3.271
Entry
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4
6
8
10
0
10
20
30
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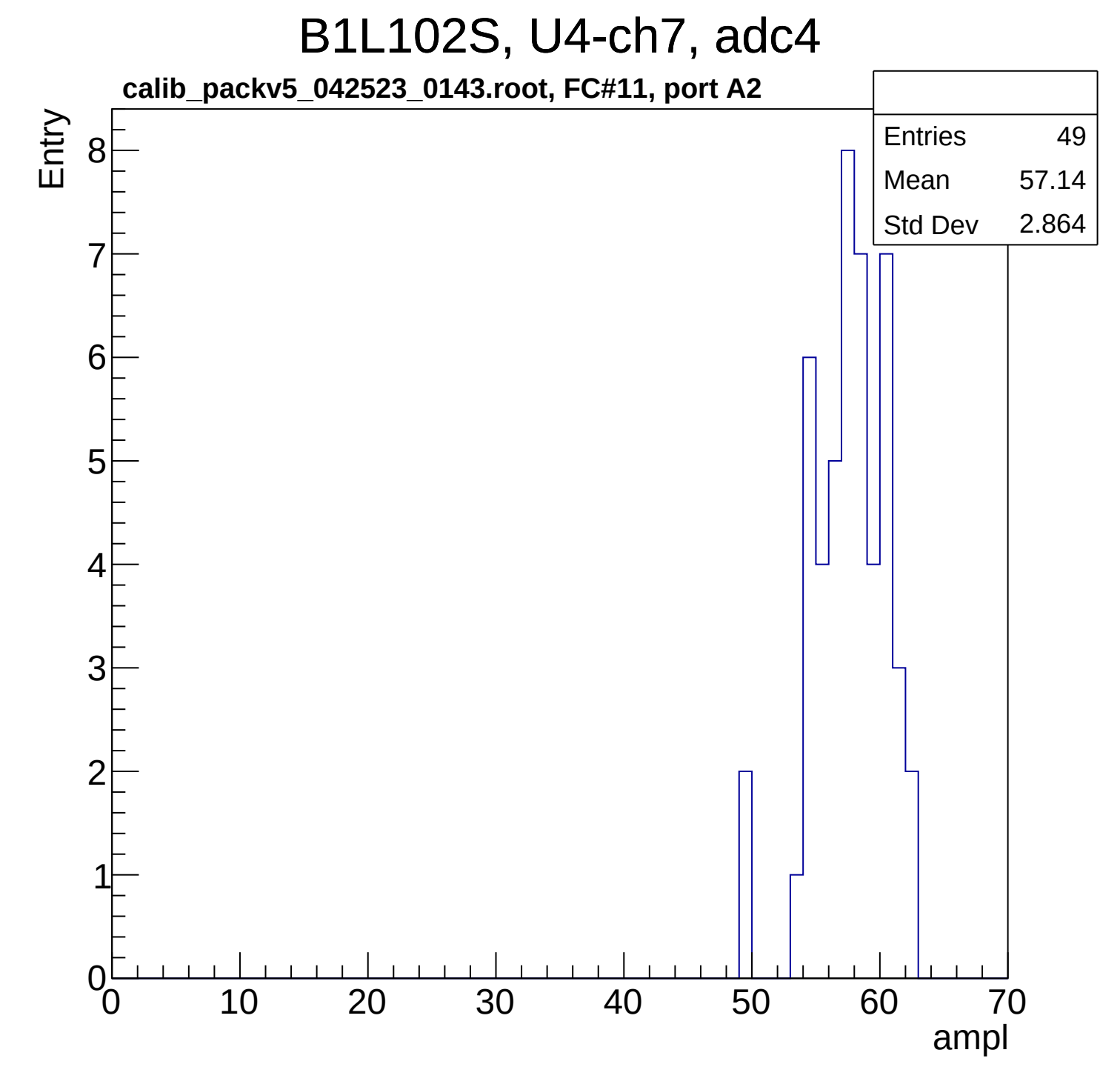
50
60
70
ampl


B1L102S, U4-ch7, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 57.14
Std Dev 2.864
Entry
ampl
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2
3
4
5
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7
8
0
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40
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60
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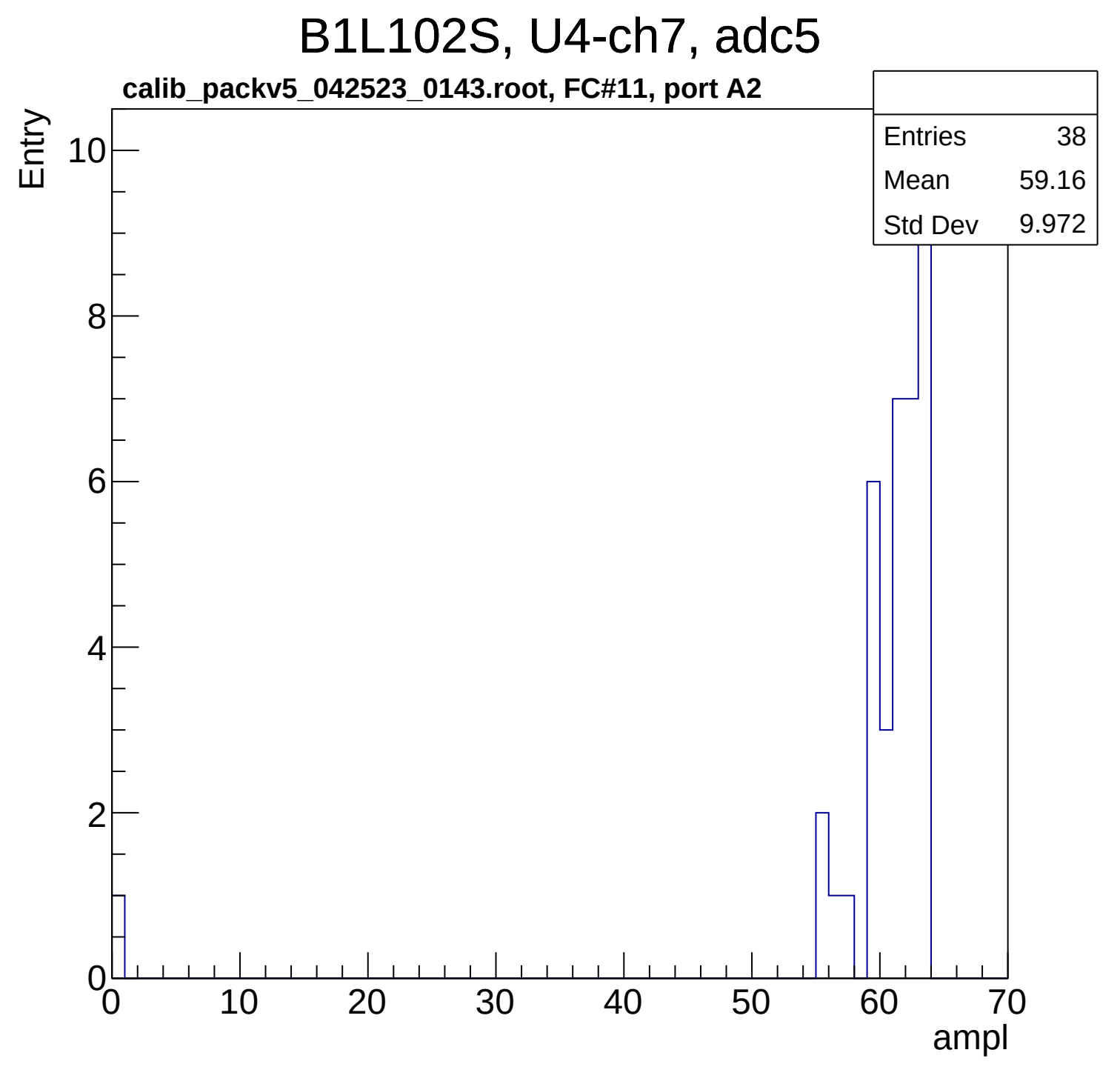
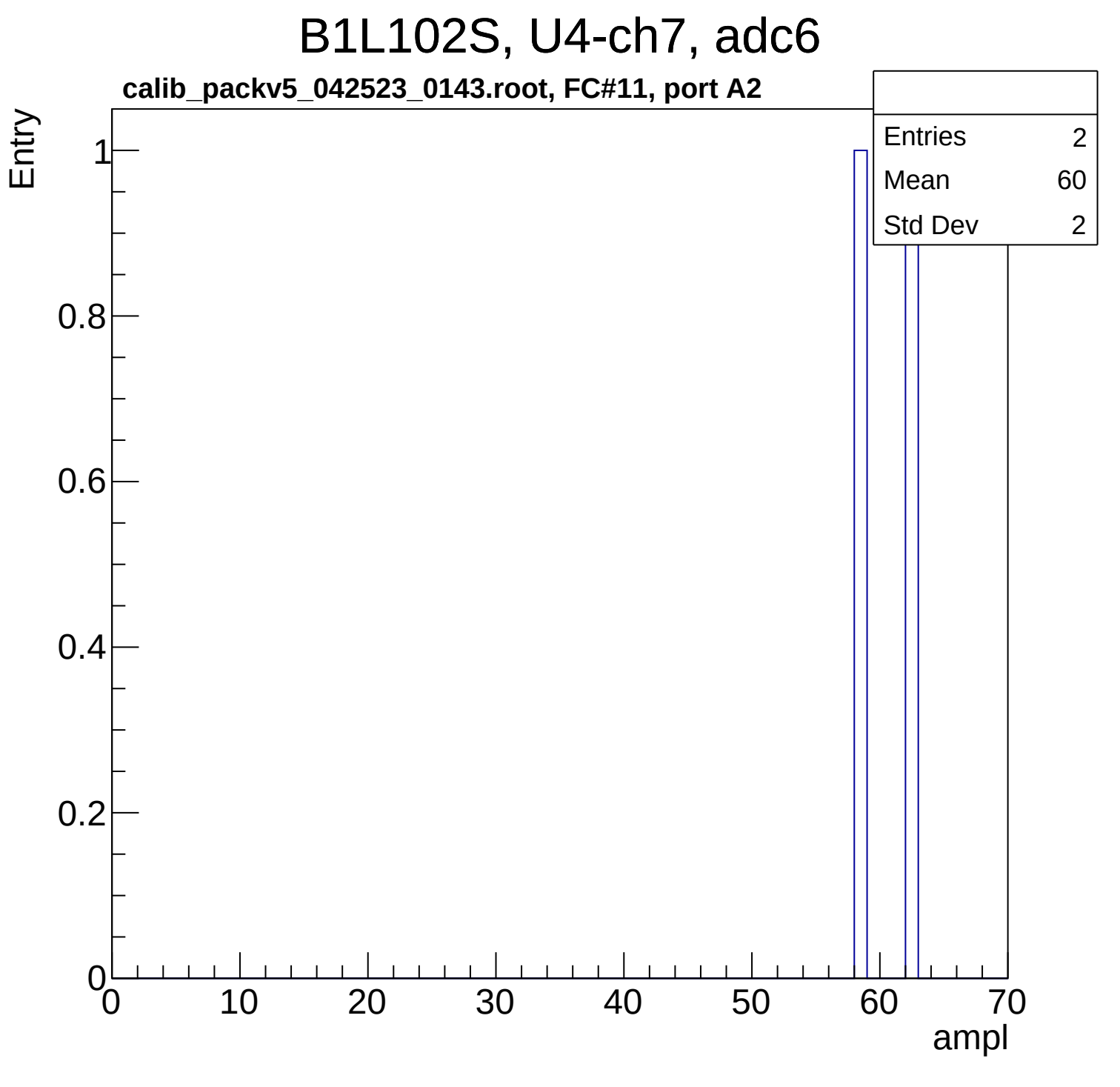

B1L102S, U4-ch7, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 38
Mean 59.16
Std Dev 9.972
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch7, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 60
Std Dev 2
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
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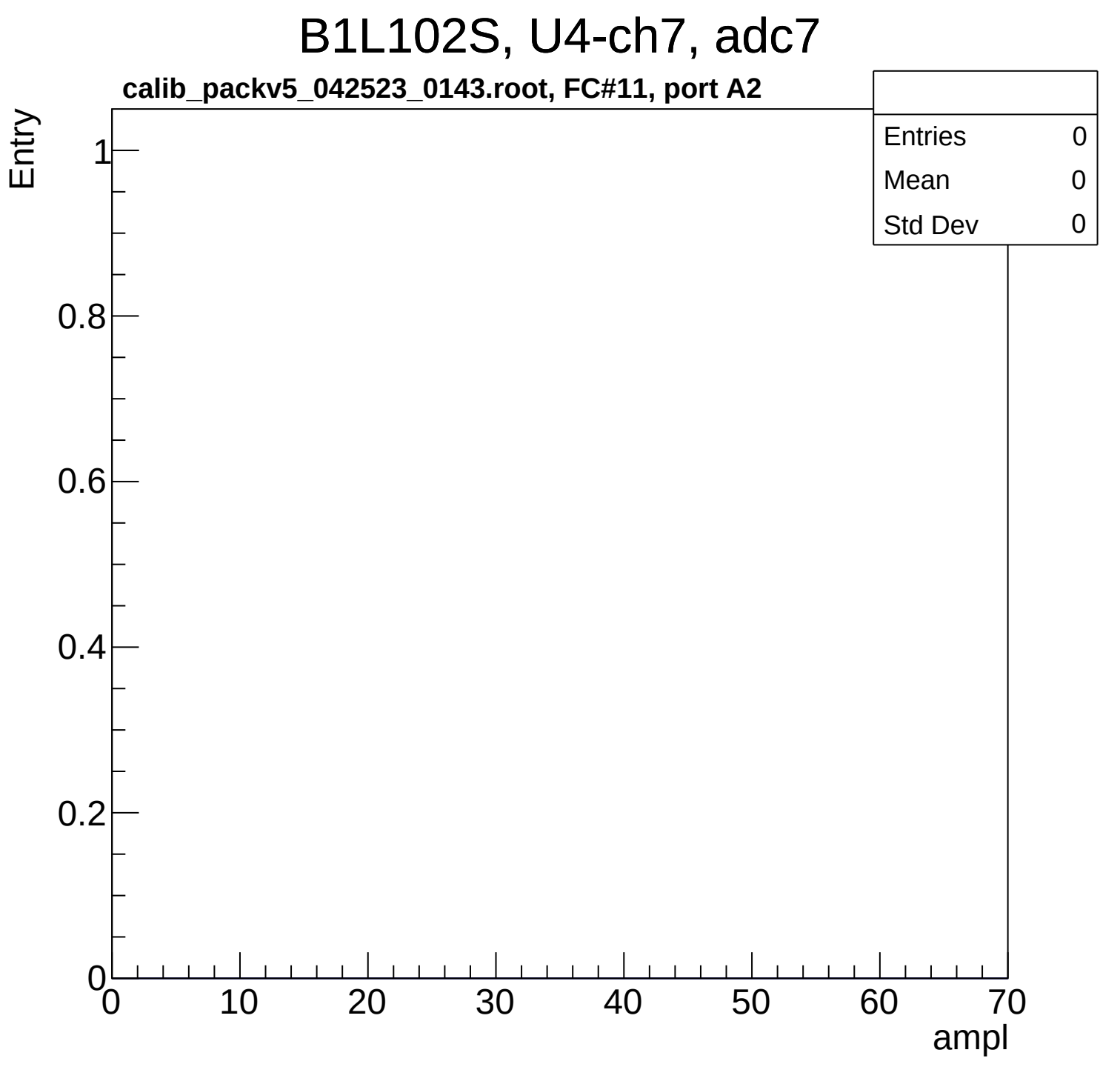
50
60
70
ampl


B1L102S, U4-ch7, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
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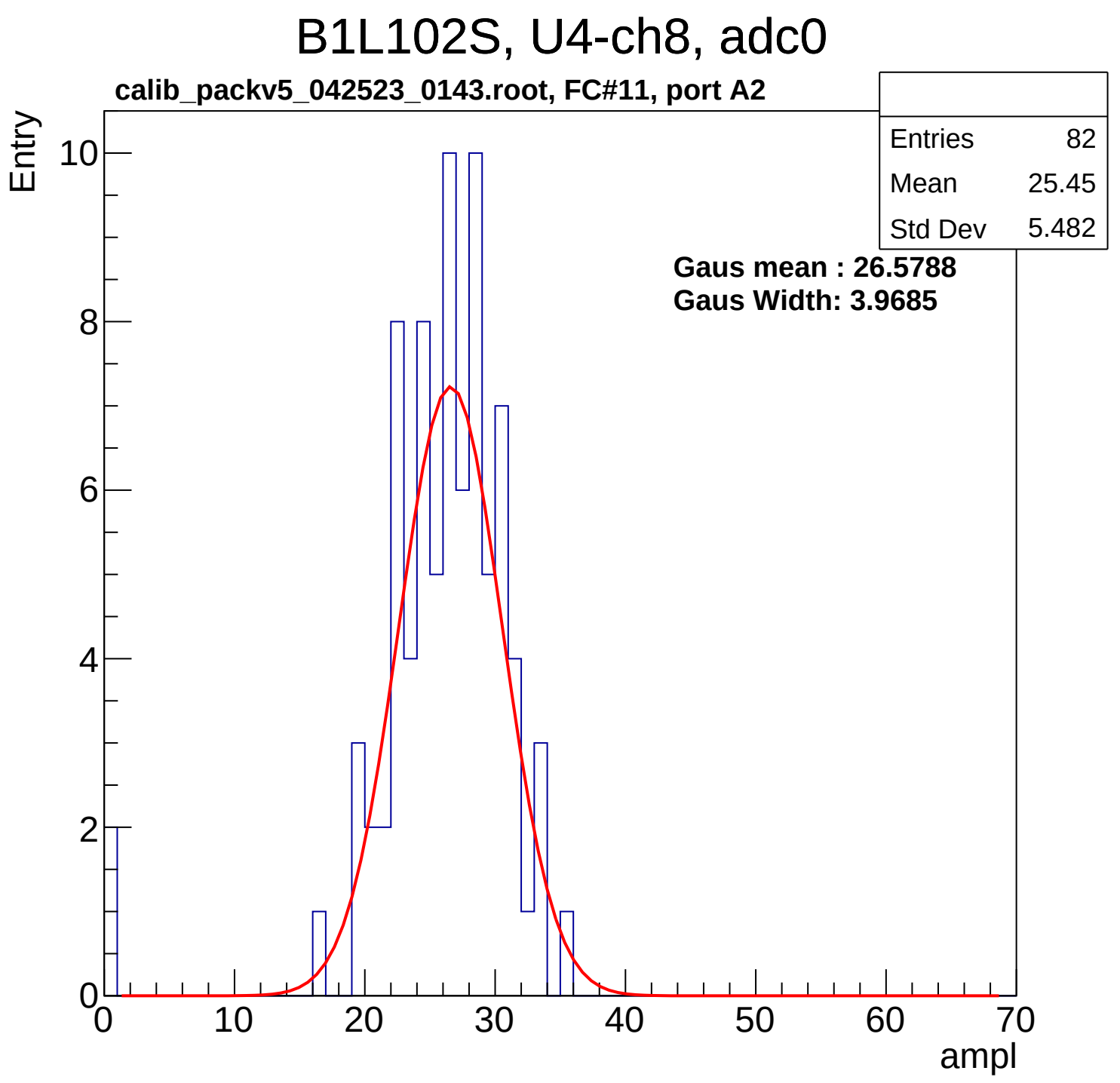
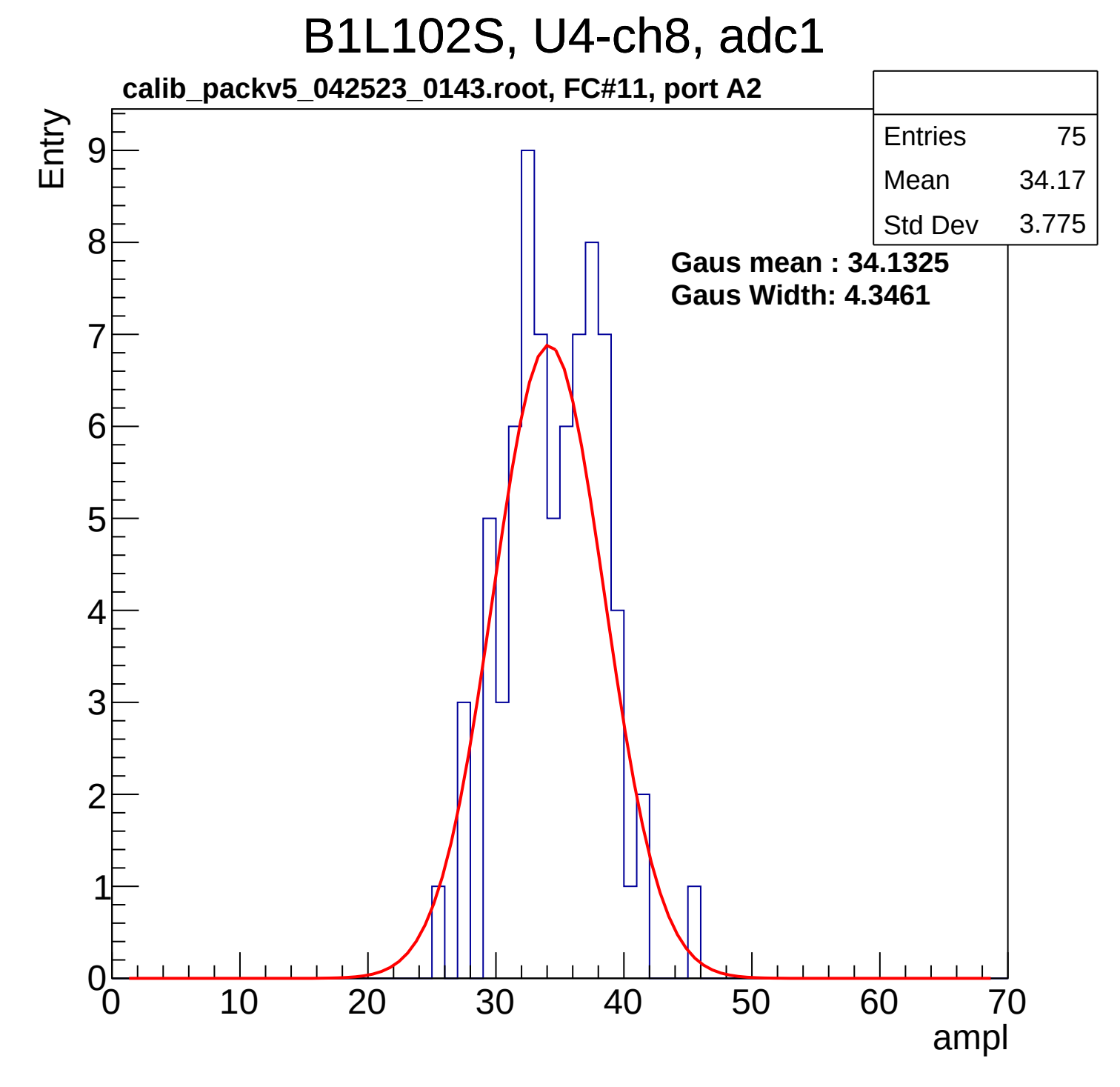
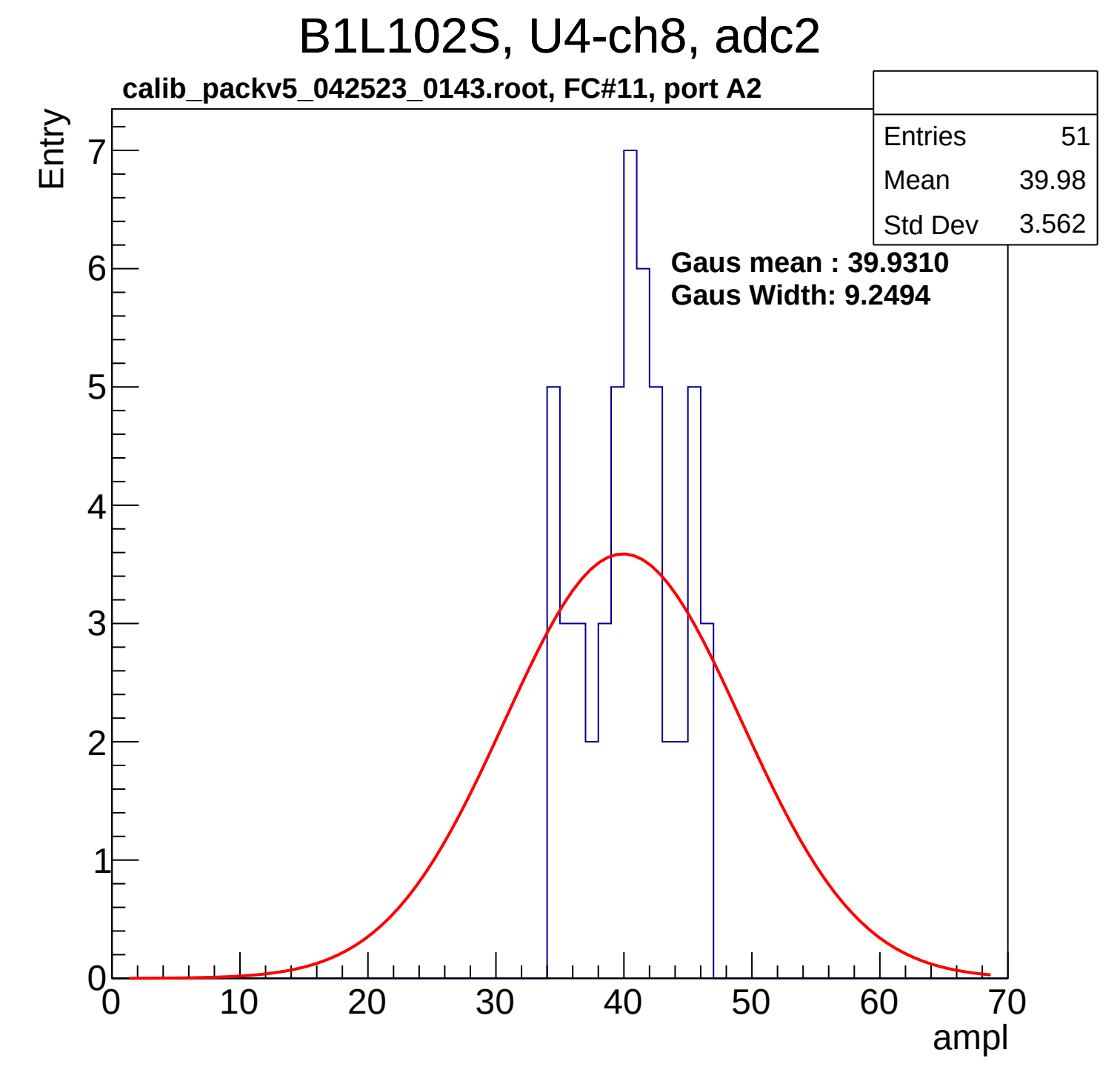
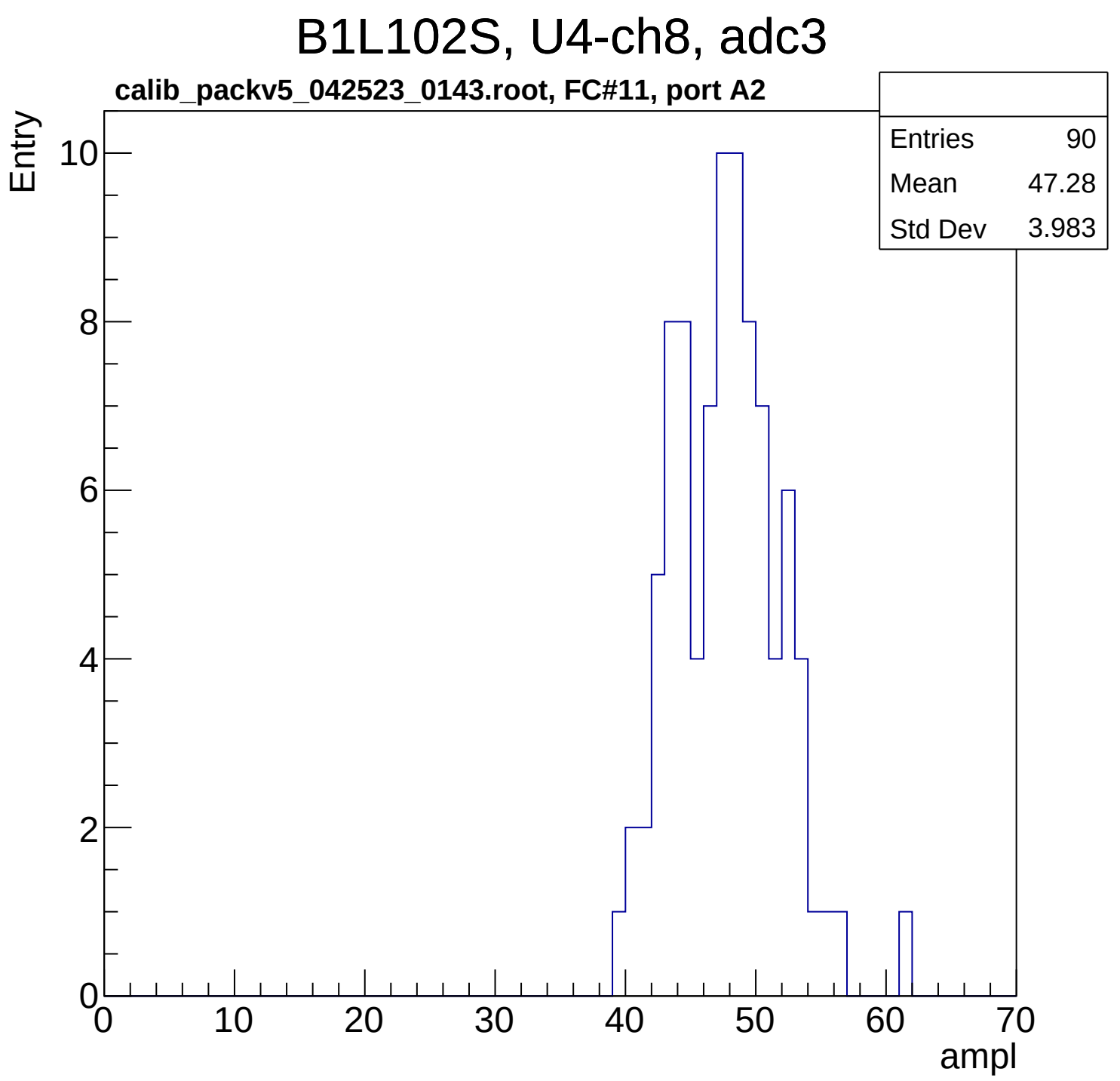
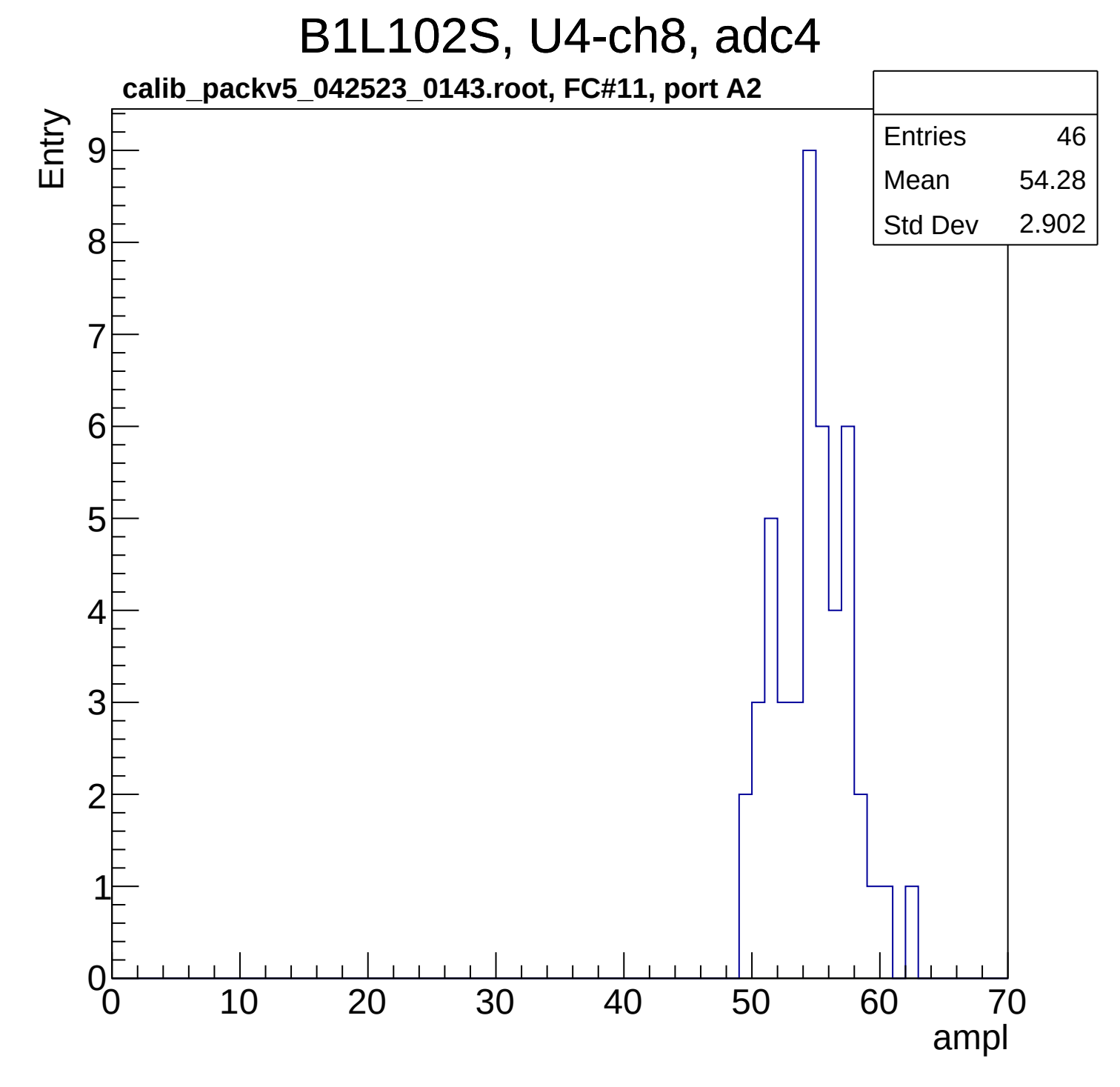
50
60
70
ampl

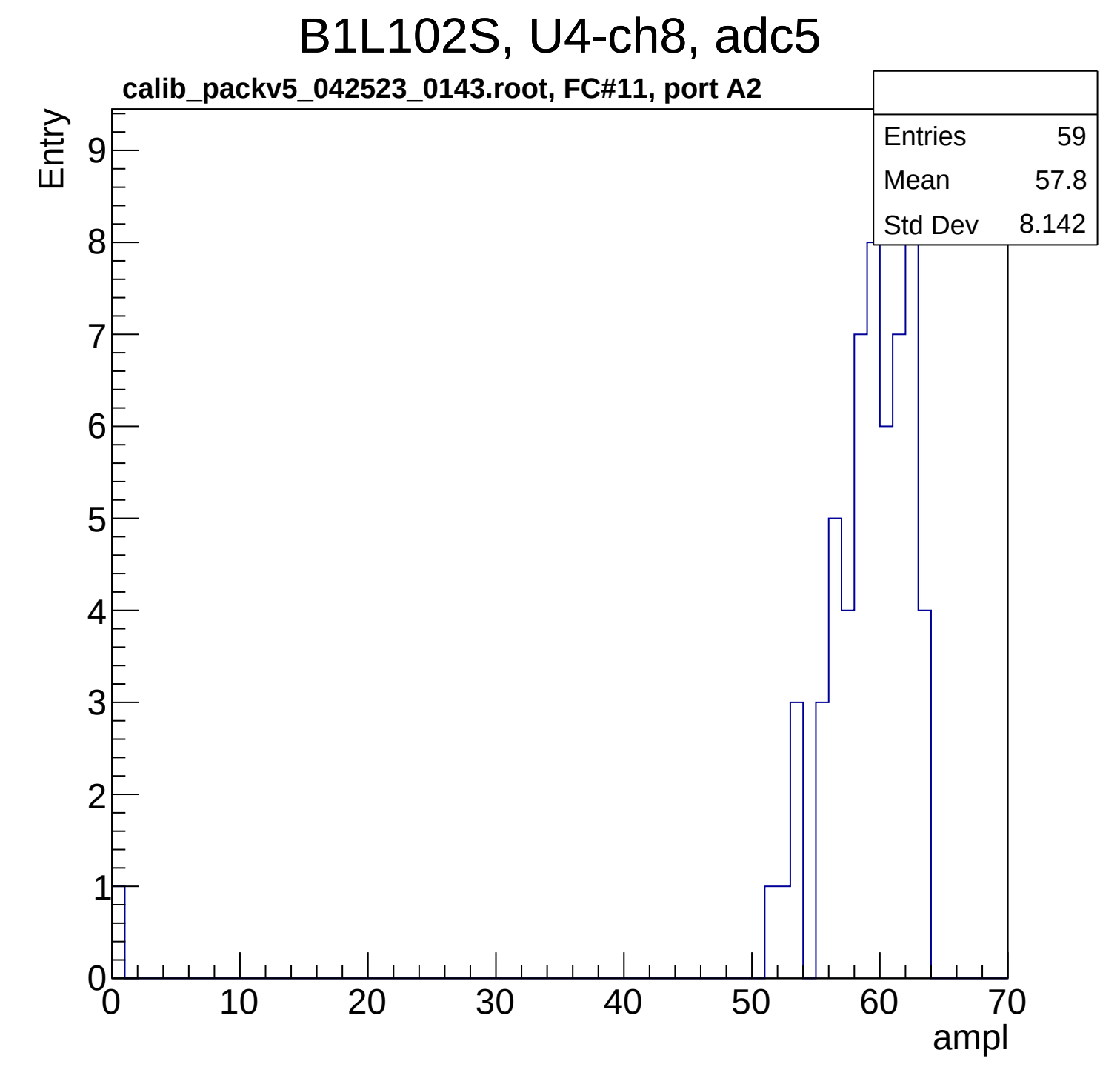

B1L102S, U4-ch8, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 82
Mean 25.45
Std Dev 5.482
Gaus mean : 26.5788
Gaus Width: 3.9685
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch8, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 34.17
Std Dev 3.775
Gaus mean : 34.1325
Gaus Width: 4.3461
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L102S, U4-ch8, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 39.98
Std Dev 3.562
Gaus mean : 39.9310
Gaus Width: 9.2494
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch8, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 90
Mean 47.28
Std Dev 3.983
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch8, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 46
Mean 54.28
Std Dev 2.902
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch8, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 57.8
Std Dev 8.142
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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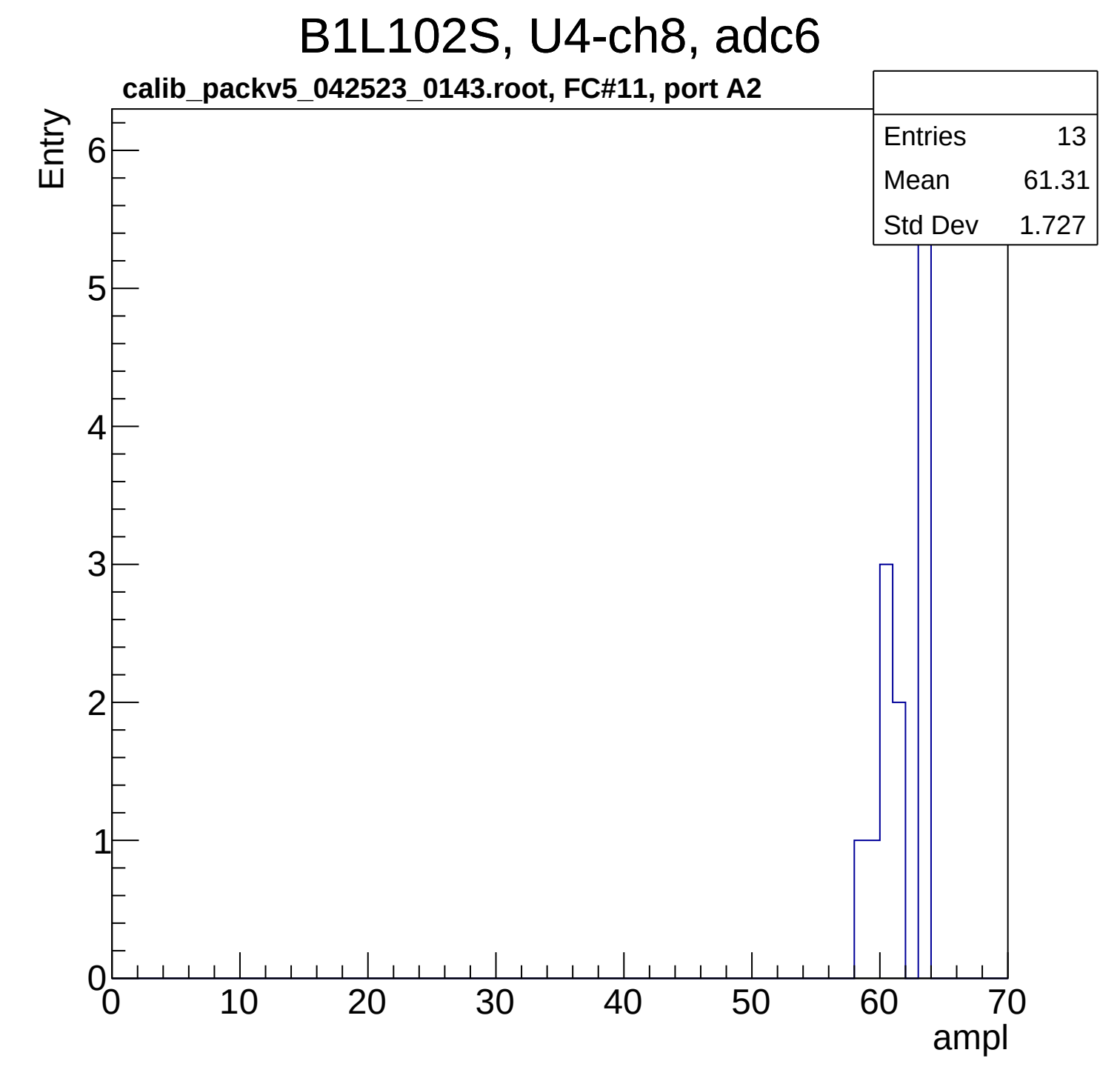
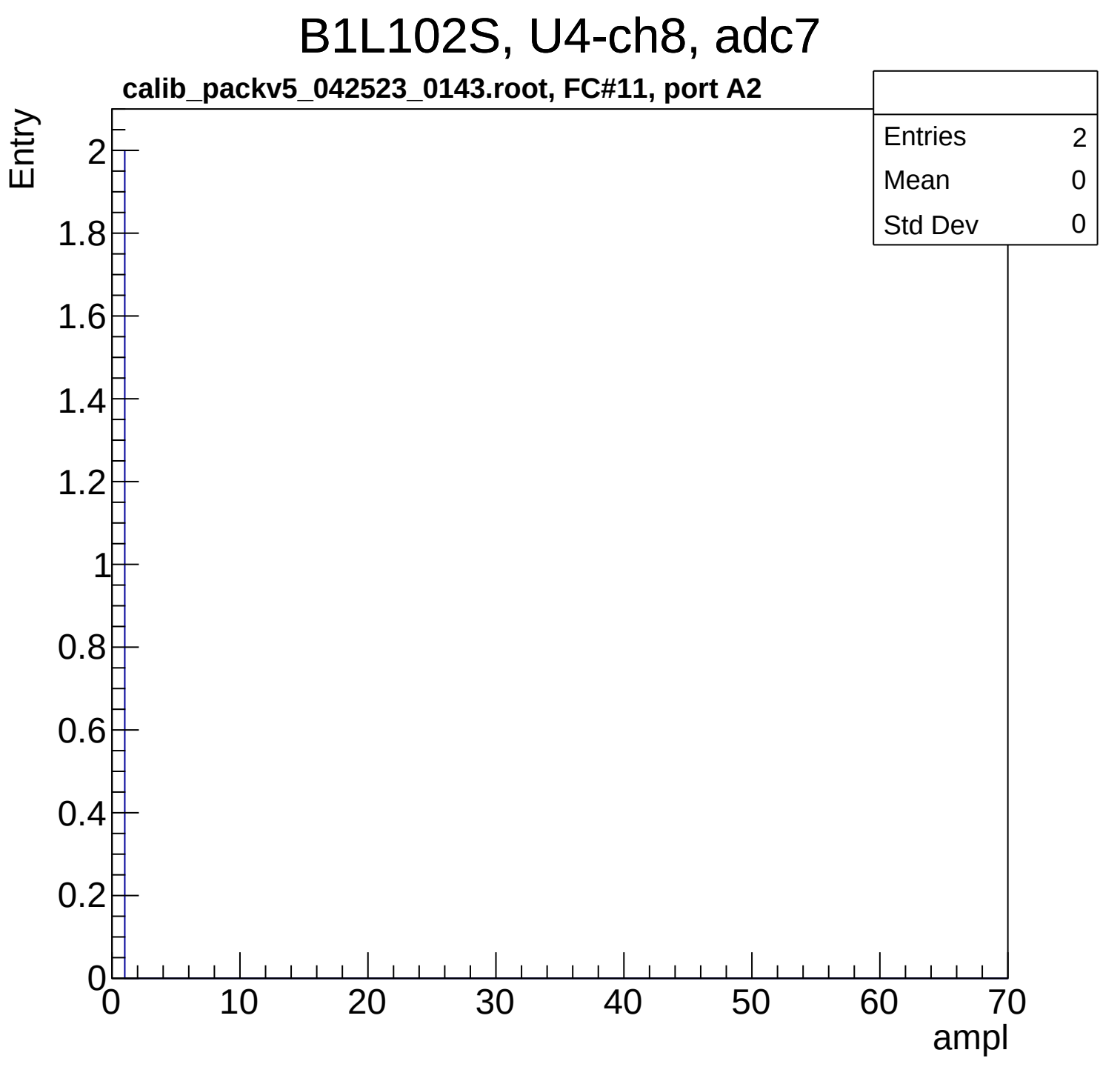
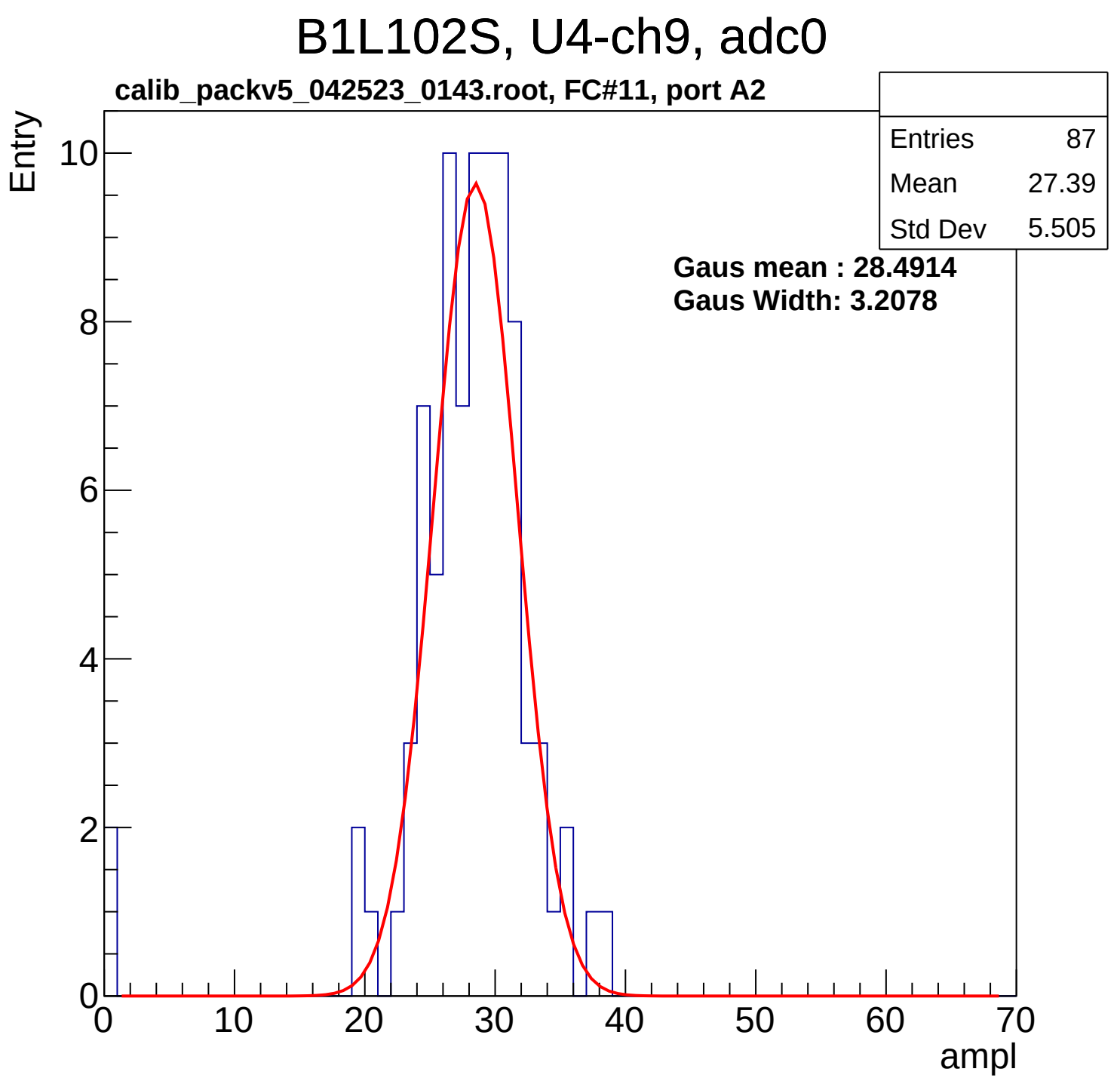
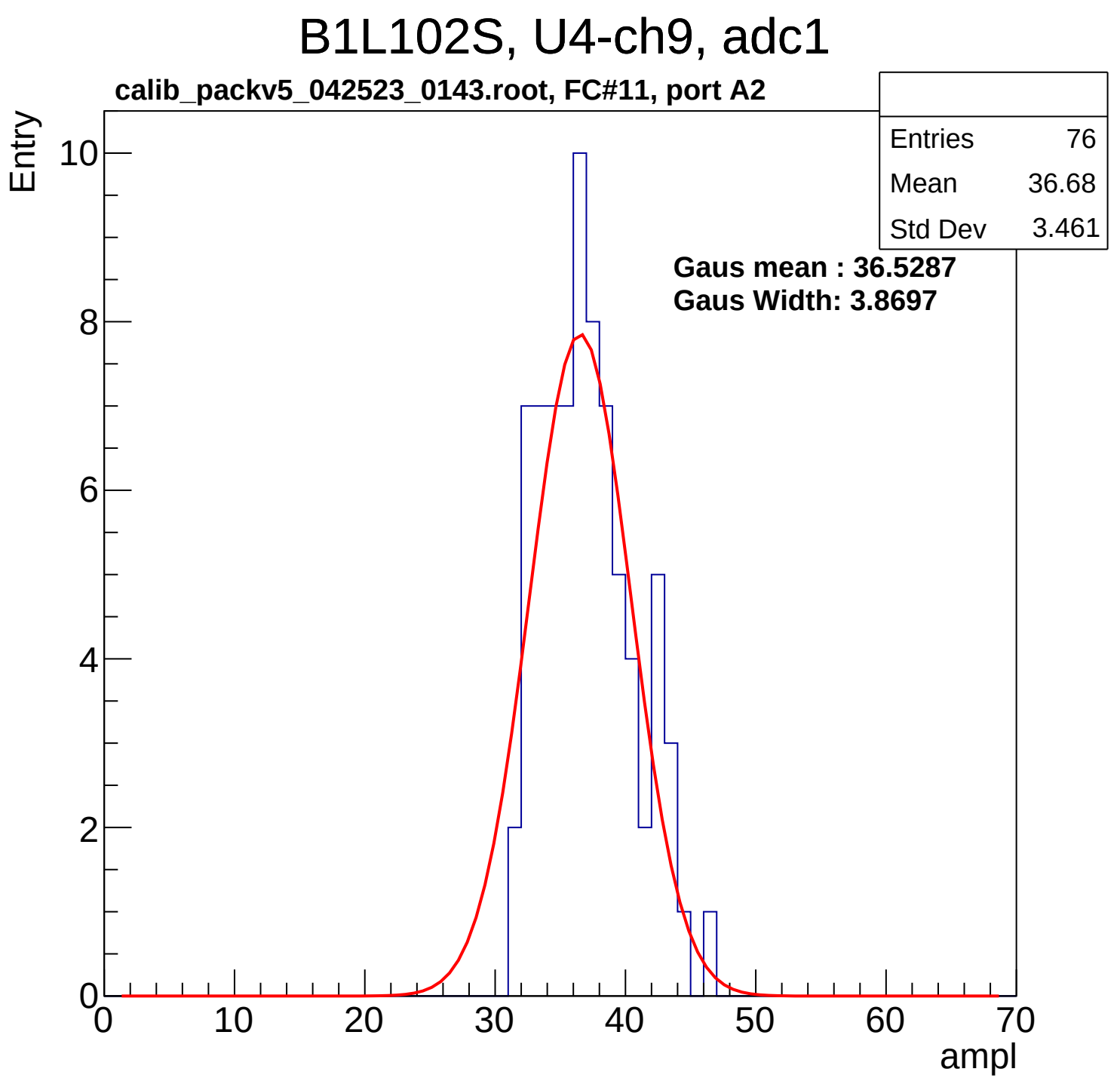
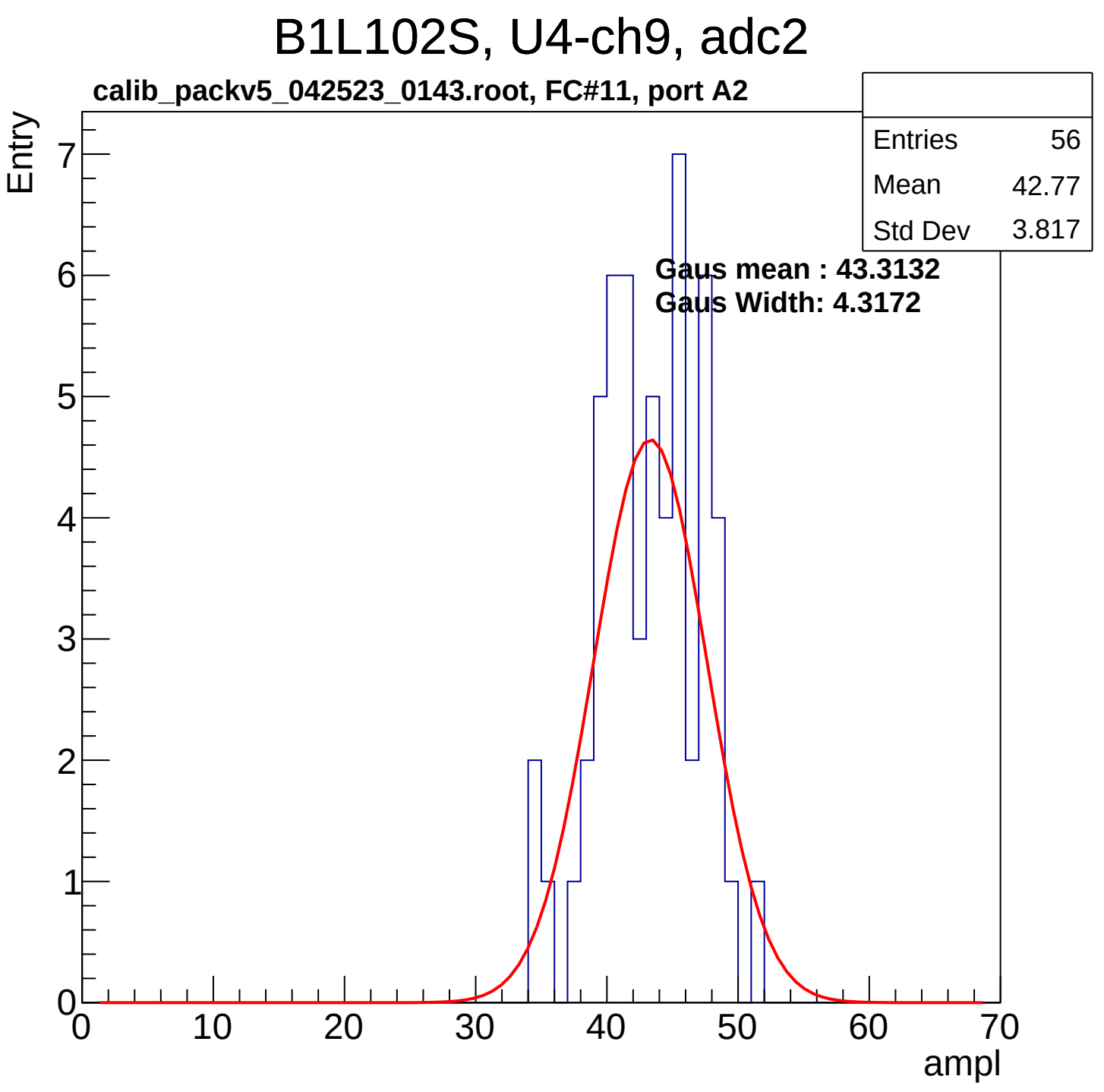
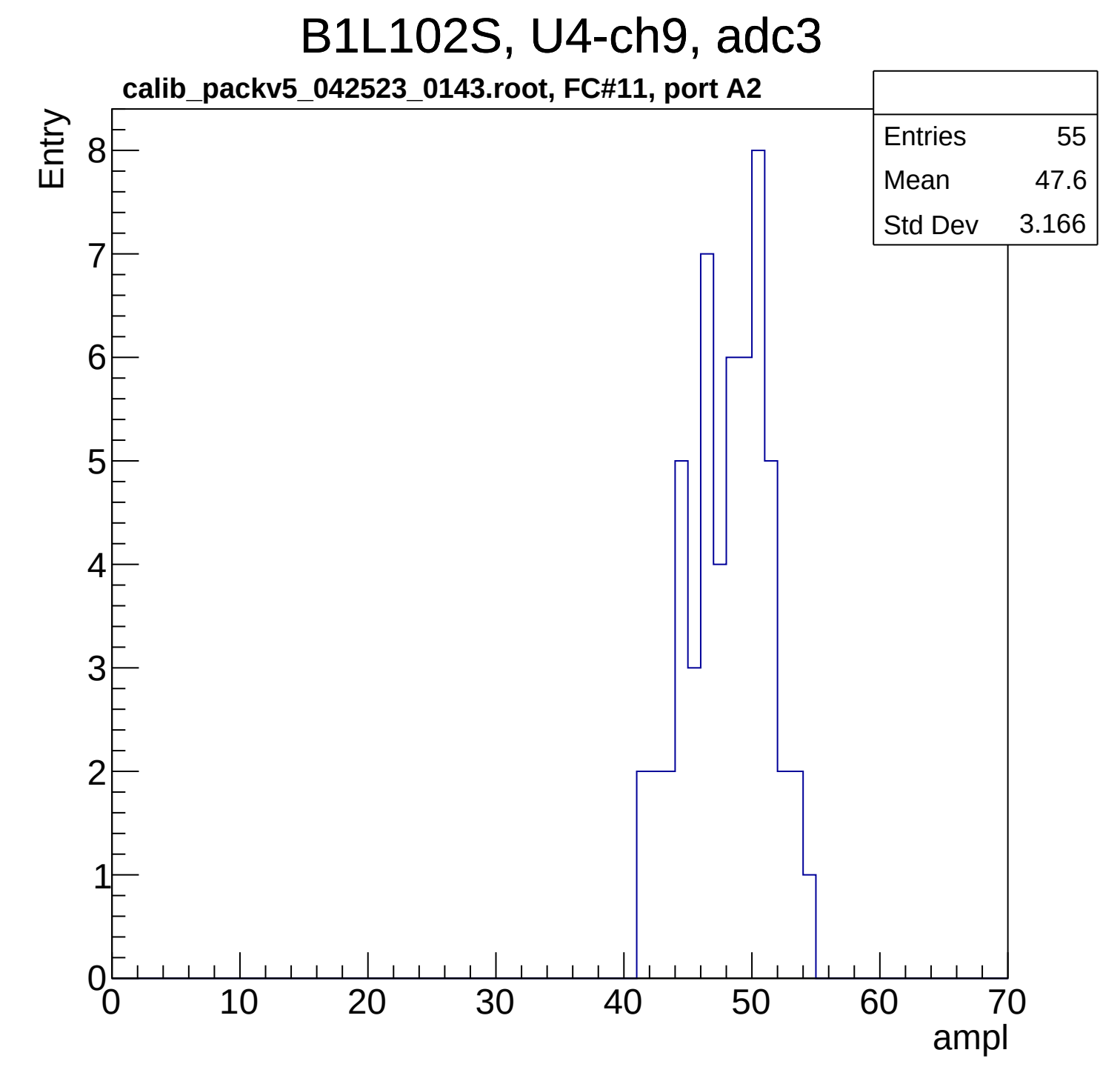

B1L102S, U4-ch8, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 13
Mean 61.31
Std Dev 1.727
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

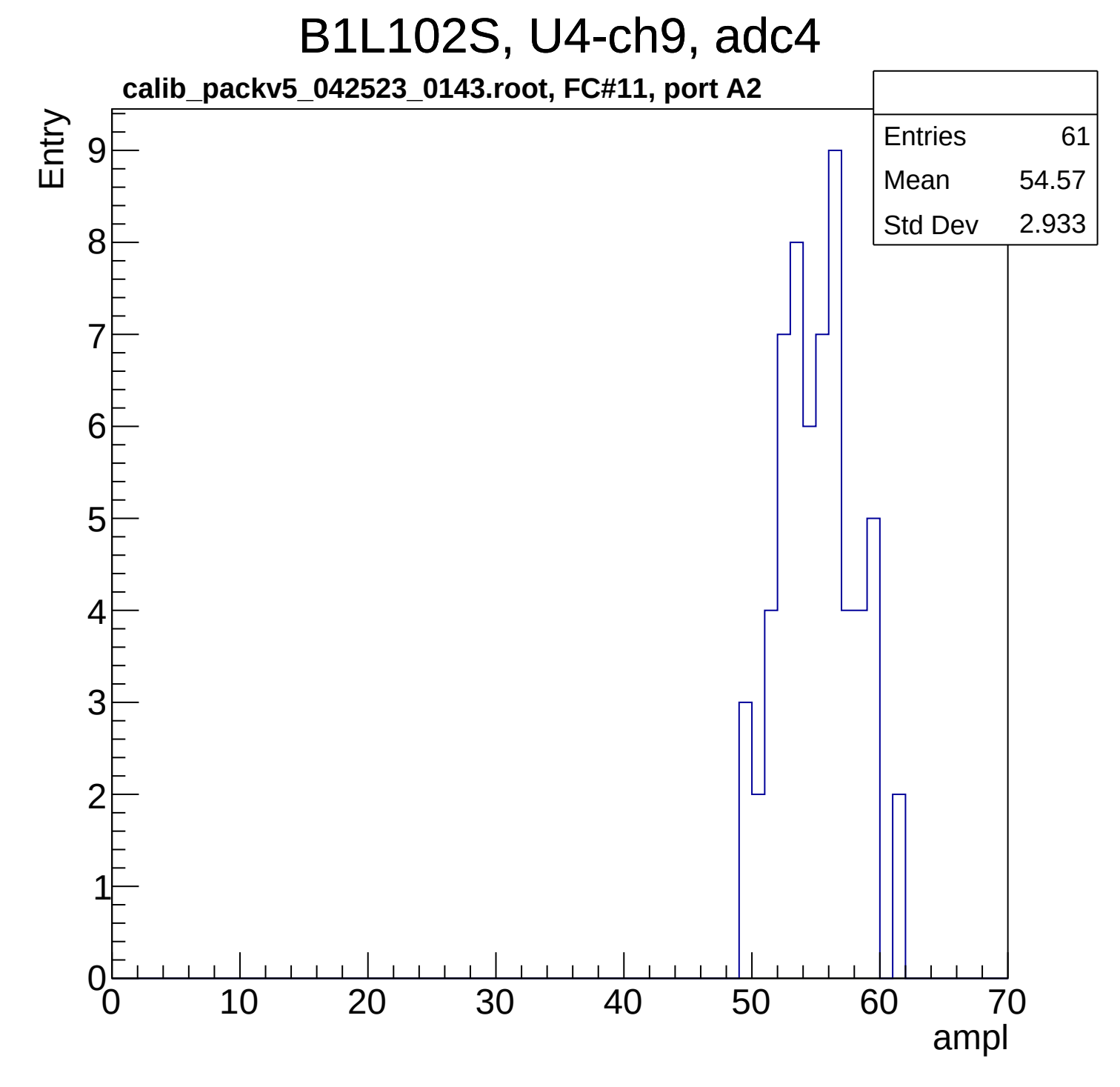

B1L102S, U4-ch8, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

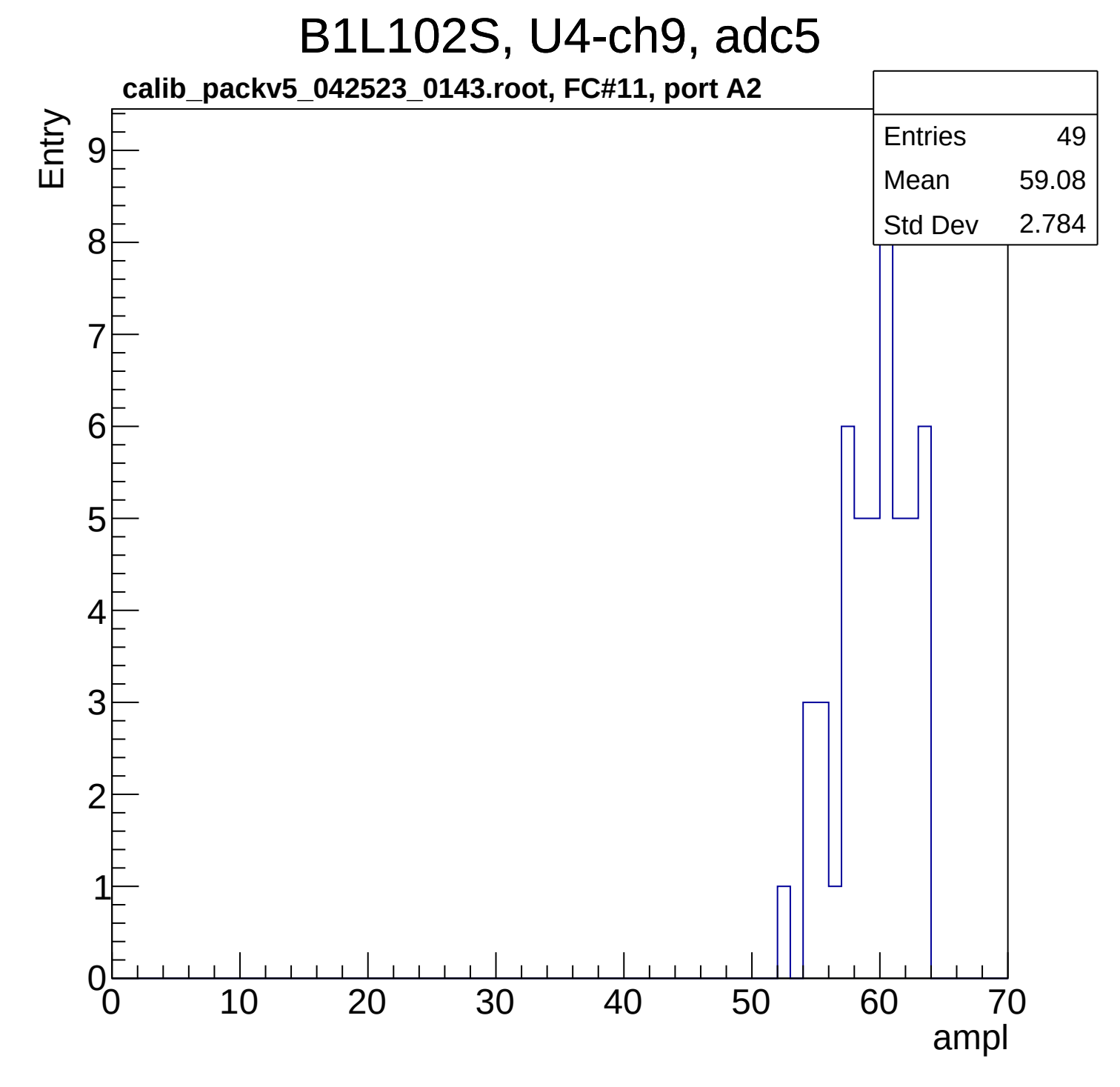

B1L102S, U4-ch9, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 87
Mean 27.39
Std Dev 5.505
Gaus mean : 28.4914
Gaus Width: 3.2078
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

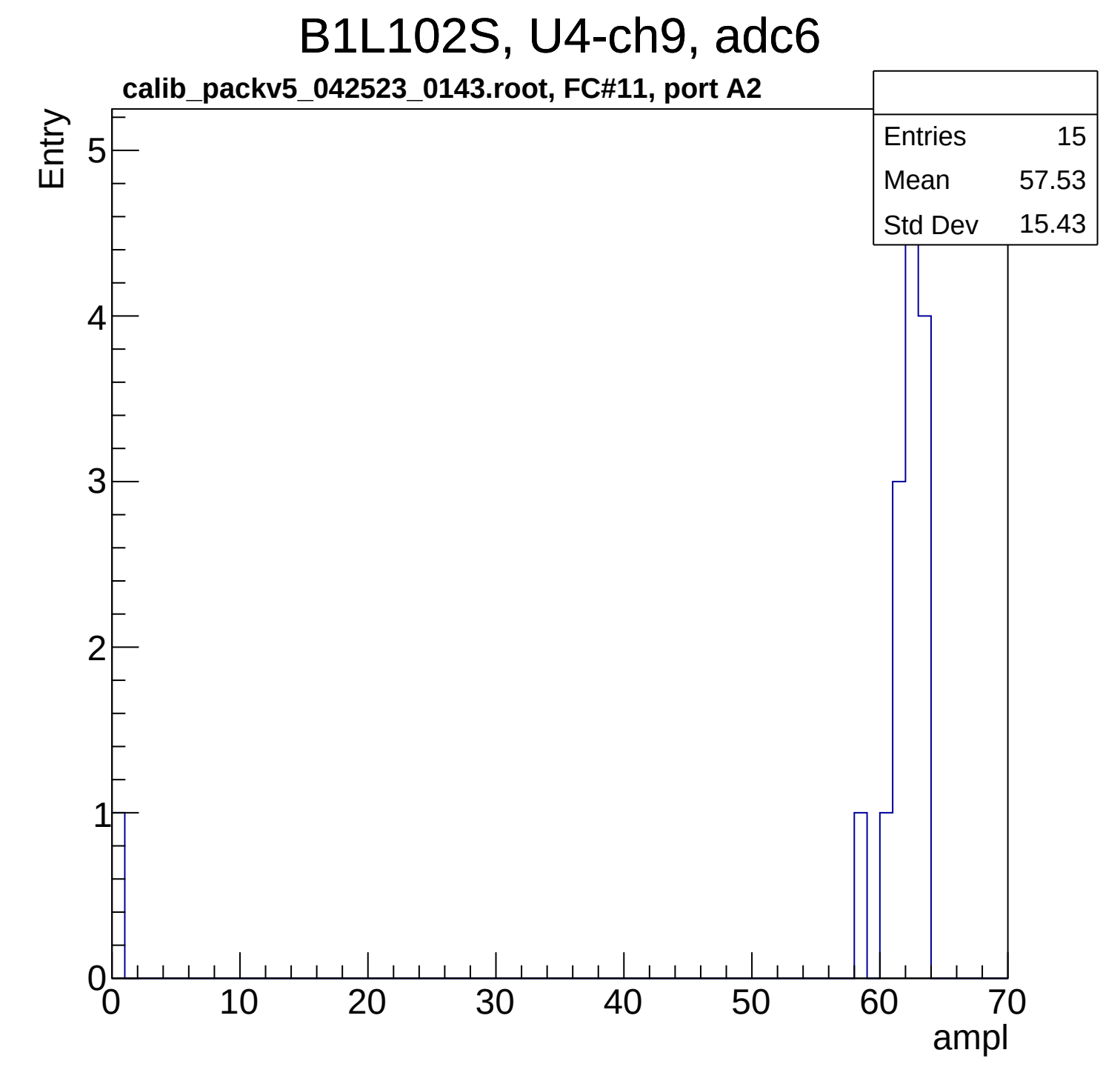

B1L102S, U4-ch9, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 36.68
Std Dev 3.461
Gaus mean : 36.5287
Gaus Width: 3.8697
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

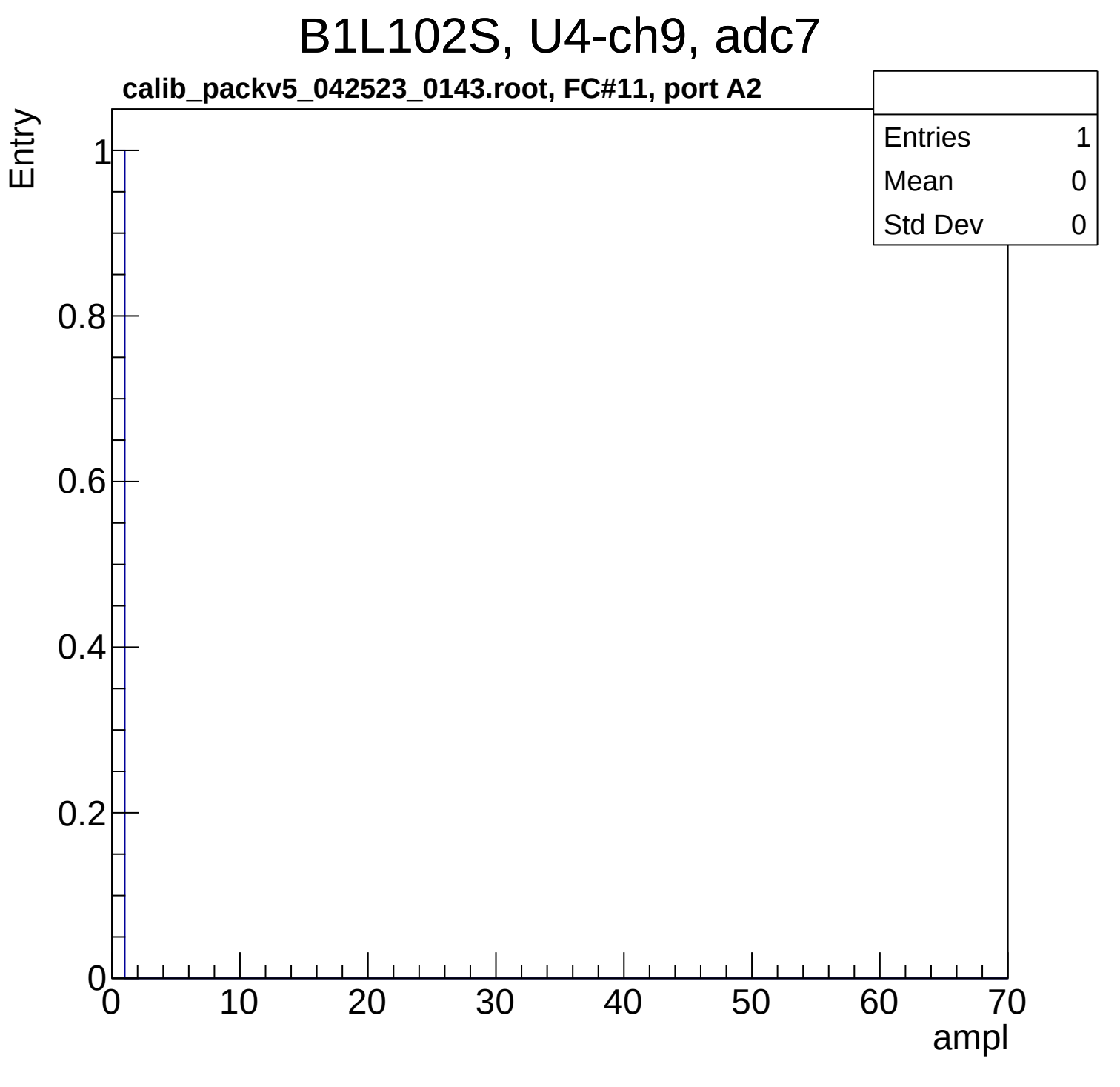

B1L102S, U4-ch9, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 42.77
Std Dev 3.817
Gaus mean : 43.3132
Gaus Width: 4.3172
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

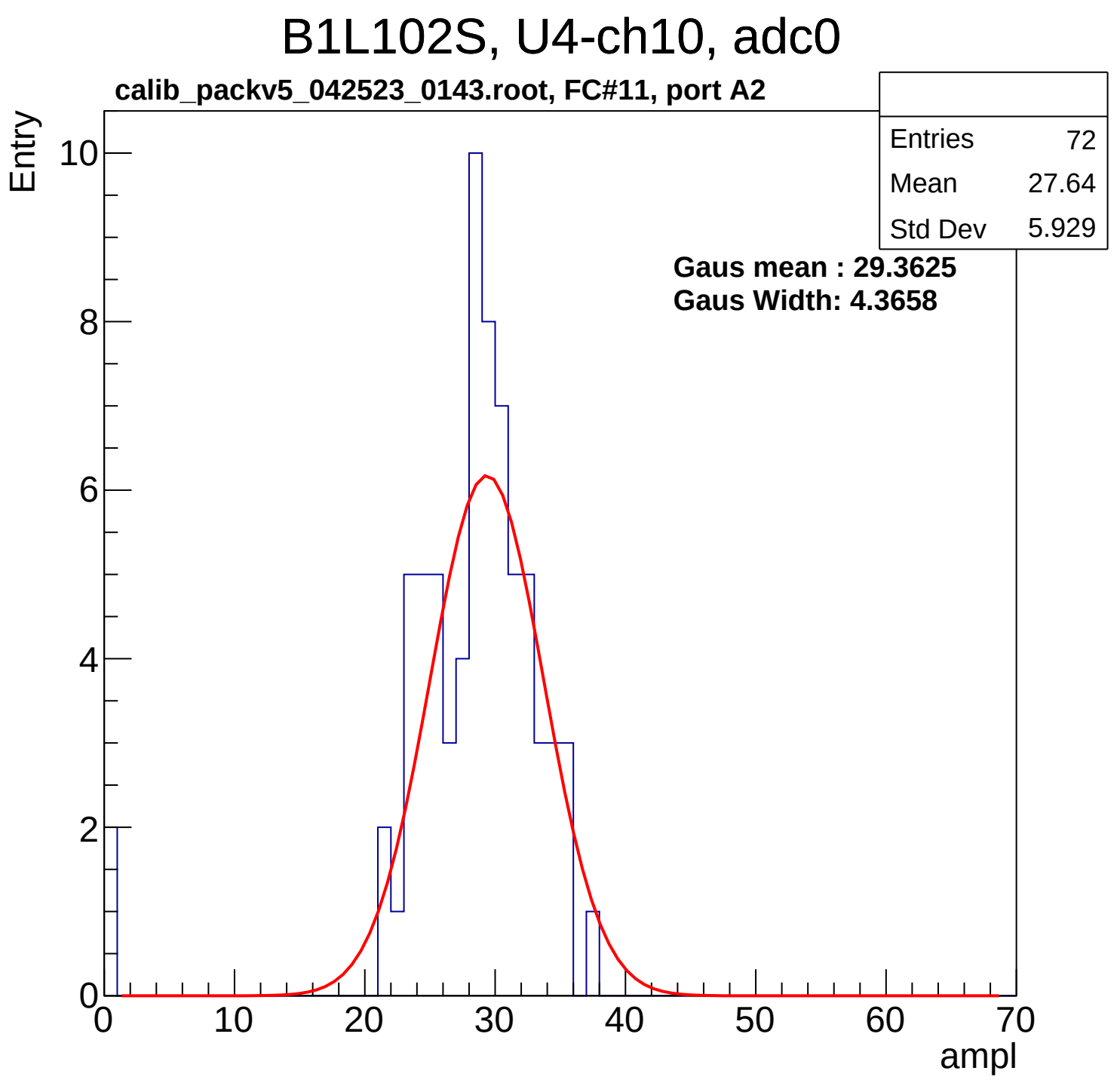

B1L102S, U4-ch9, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 47.6
Std Dev 3.166
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

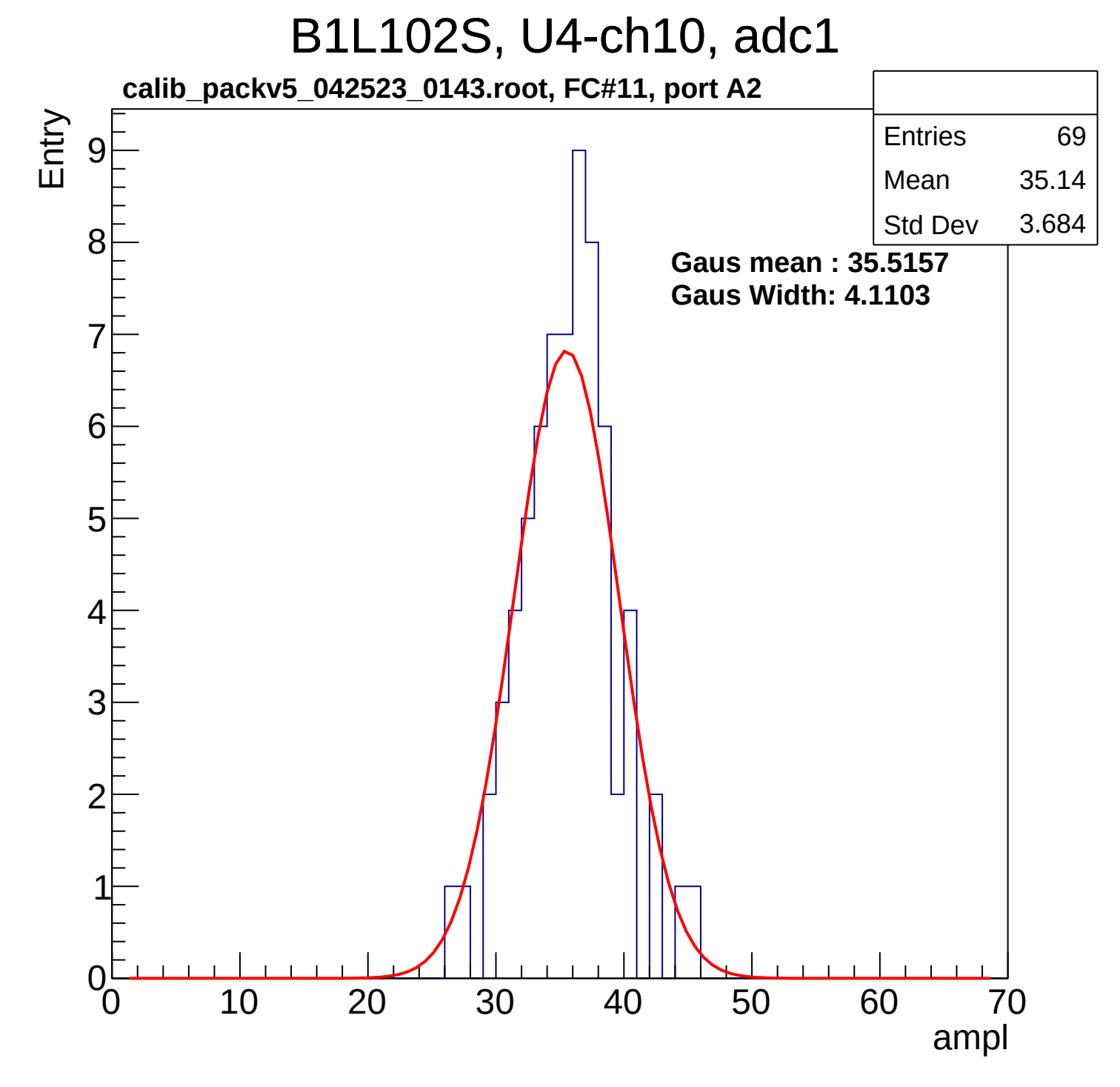

B1L102S, U4-ch9, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 54.57
Std Dev 2.933
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

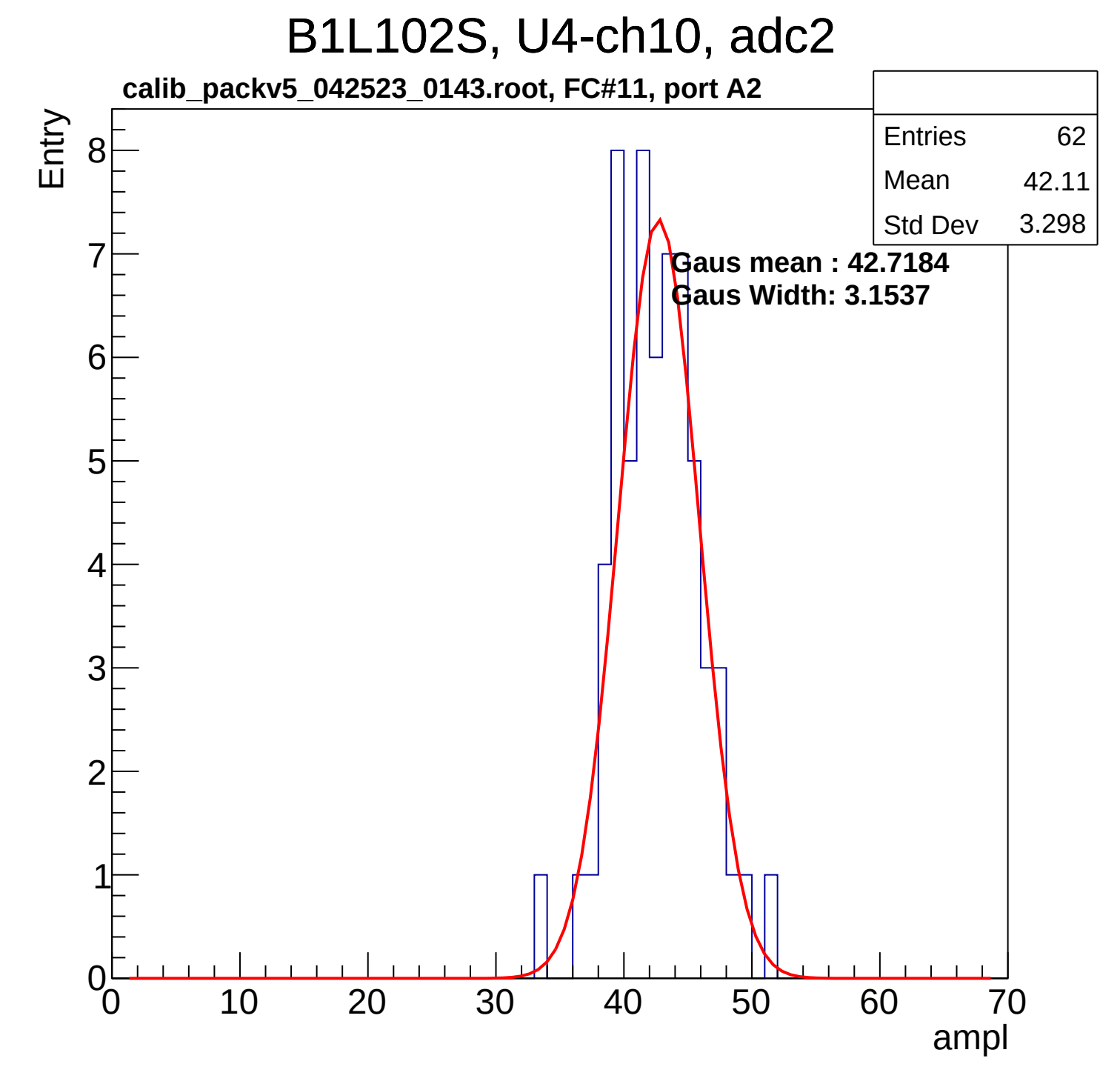

B1L102S, U4-ch9, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 59.08
Std Dev 2.784
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

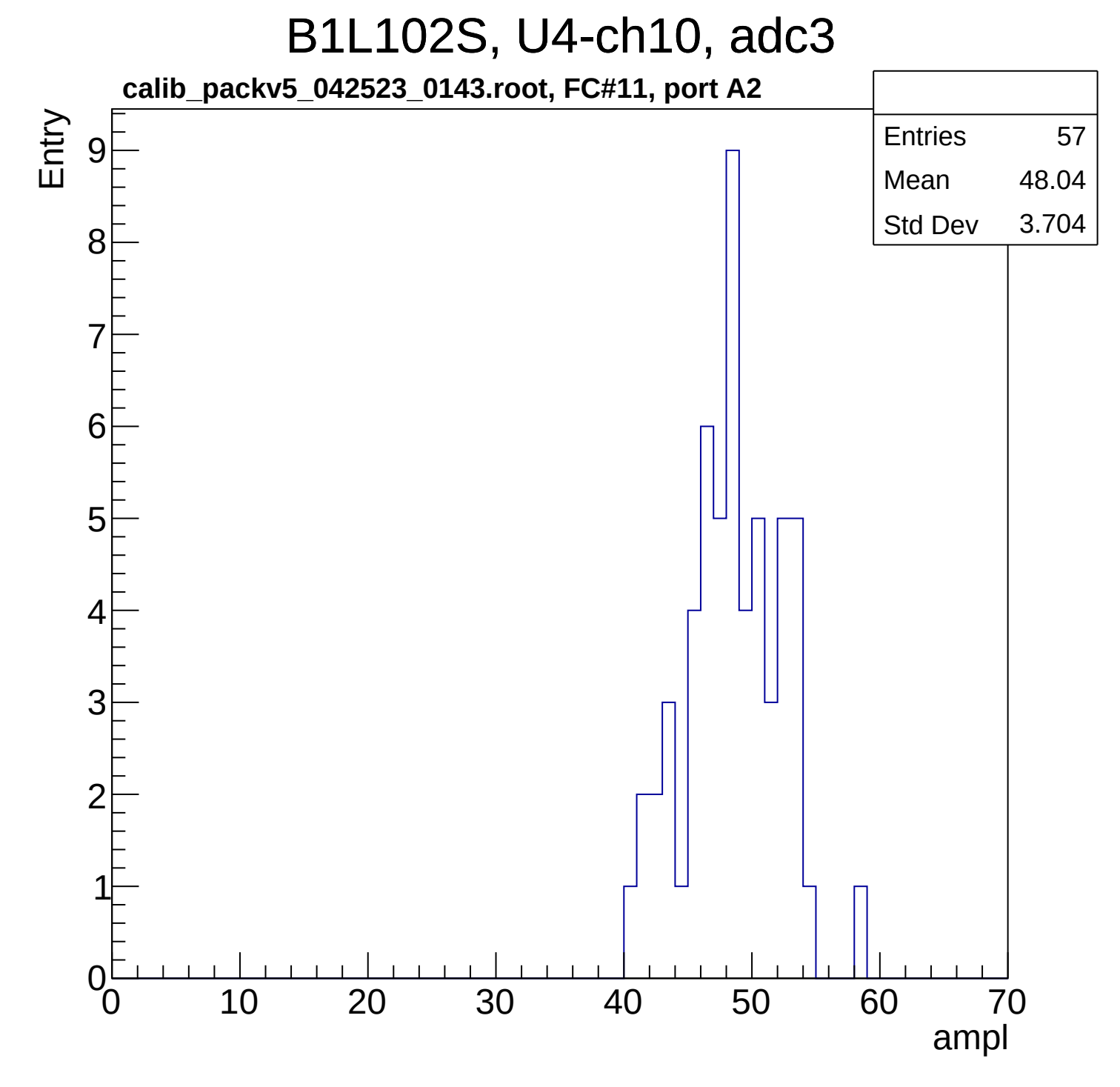

B1L102S, U4-ch9, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 15
Mean 57.53
Std Dev 15.43
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

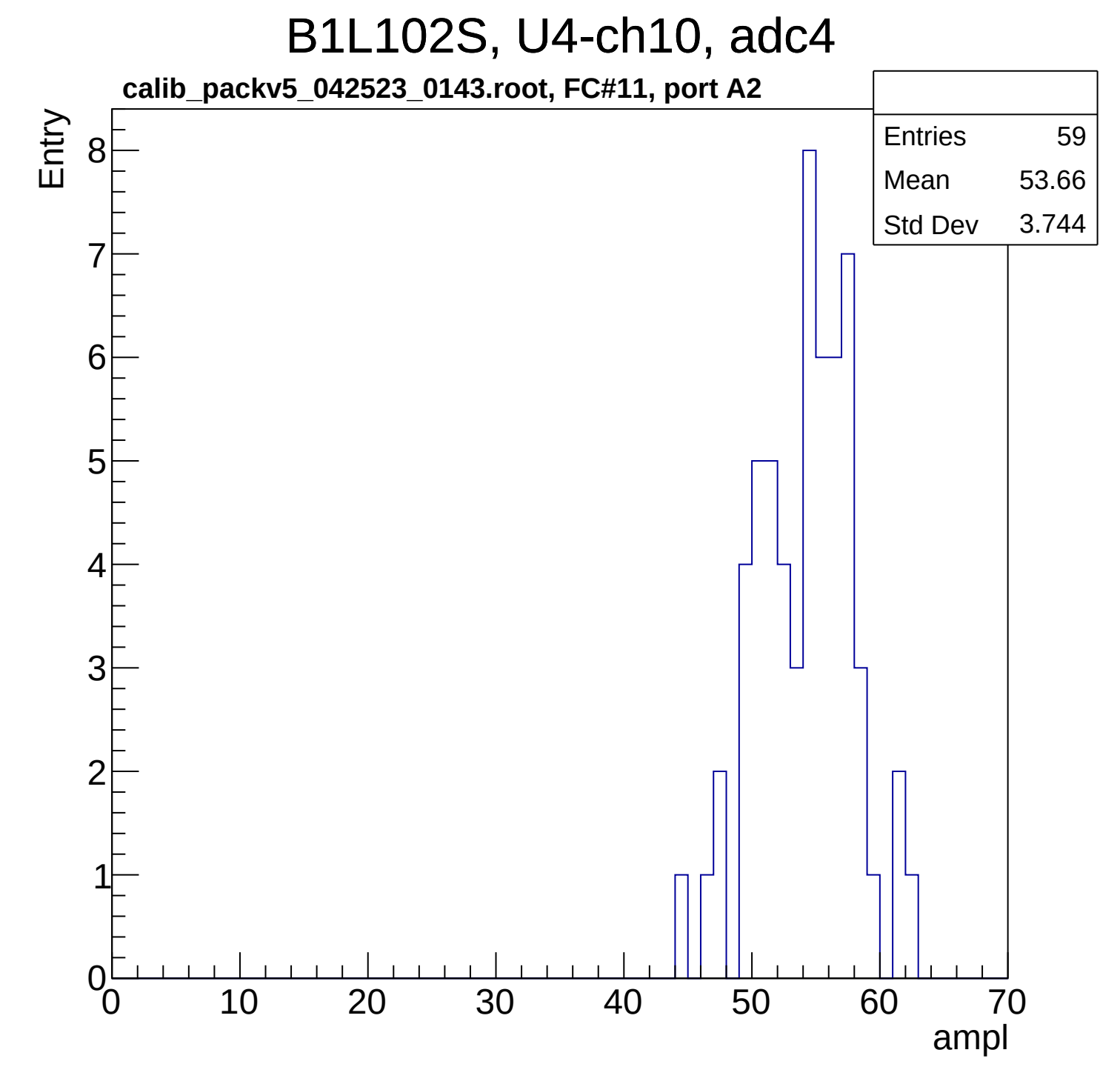

B1L102S, U4-ch9, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

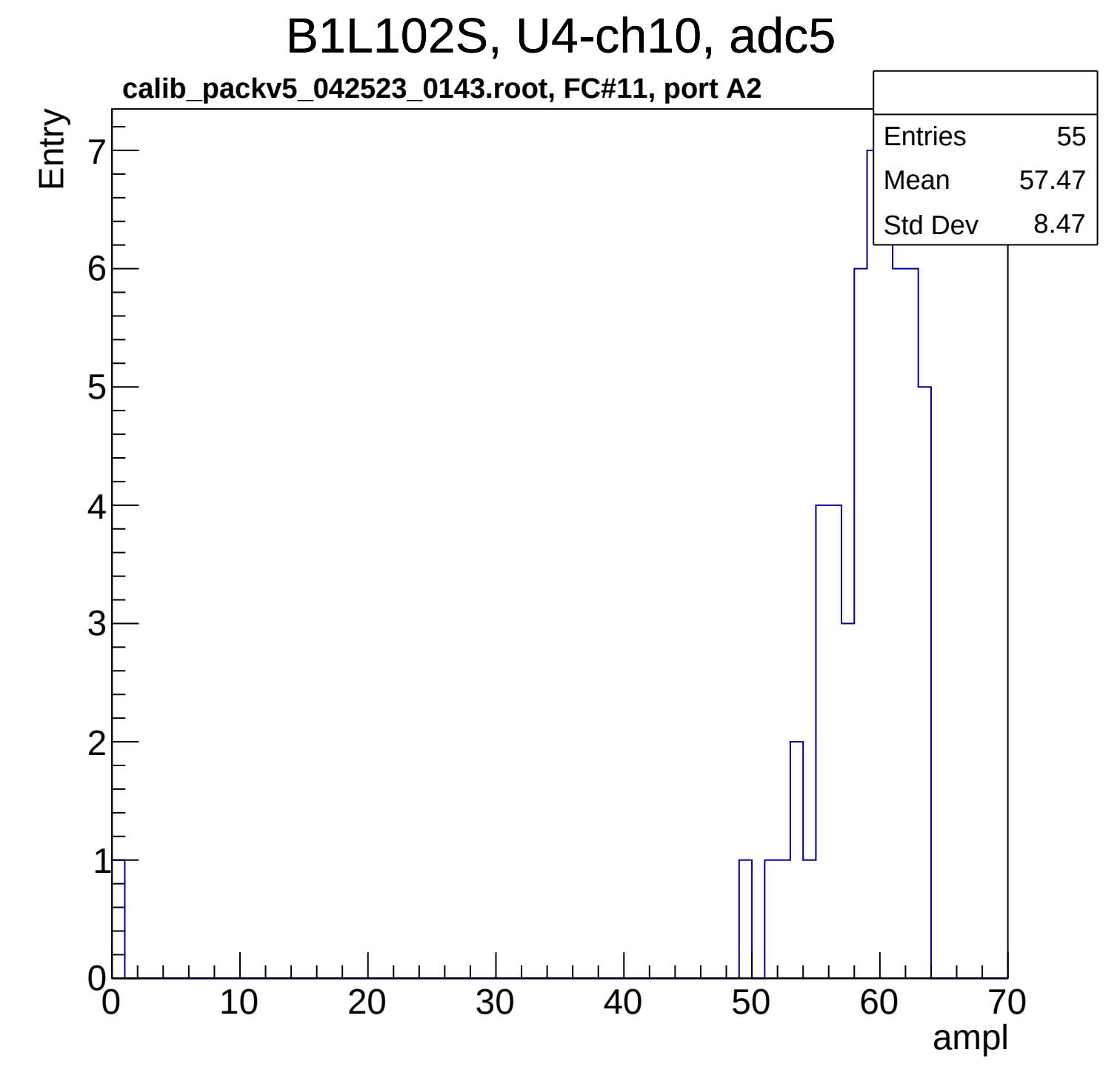

B1L102S, U4-ch10, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 72
Mean 27.64
Std Dev 5.929
Gaus mean : 29.3625
Gaus Width: 4.3658
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

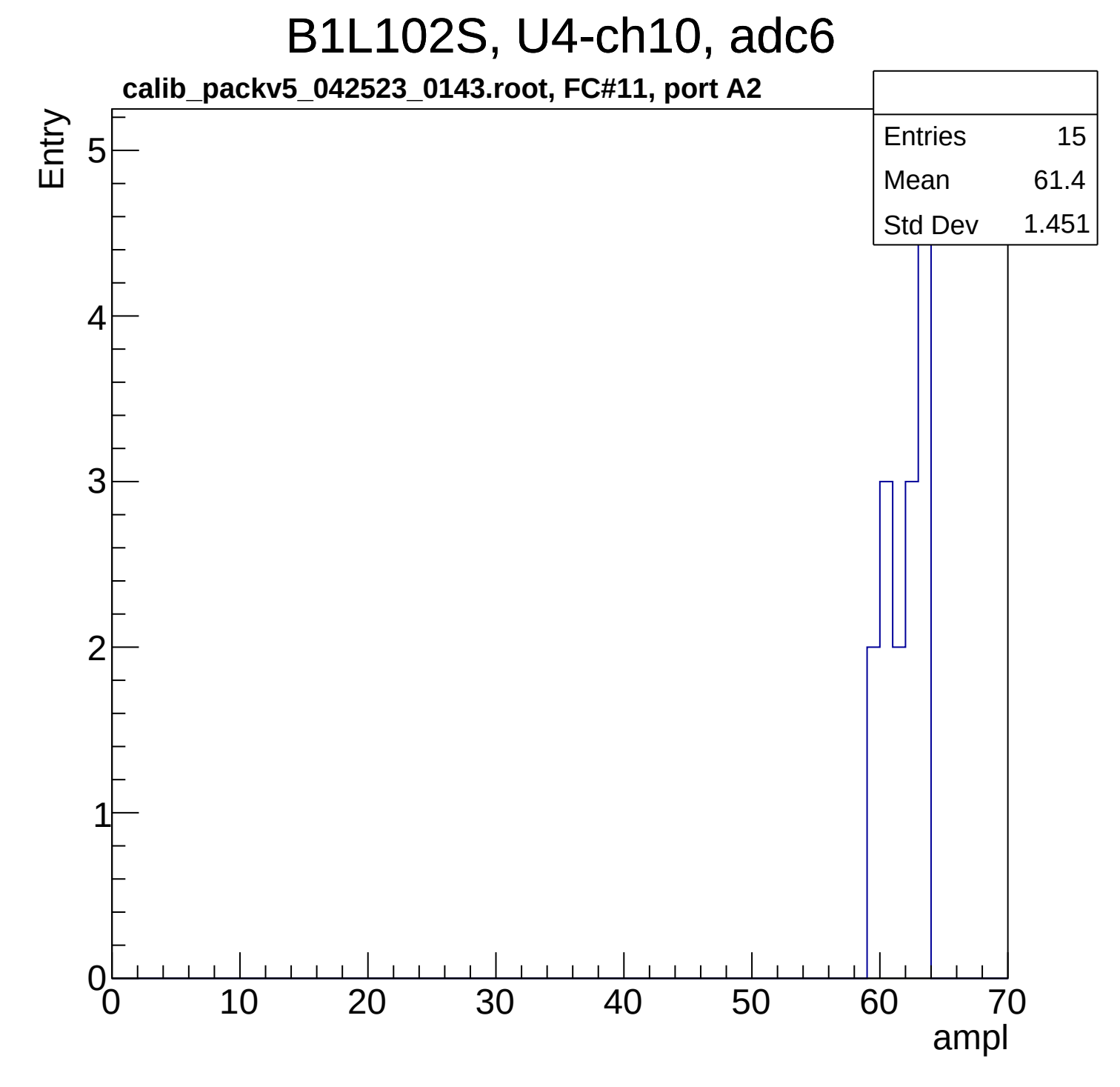

B1L102S, U4-ch10, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 35.14
Std Dev 3.684
Gaus mean : 35.5157
Gaus Width: 4.1103
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

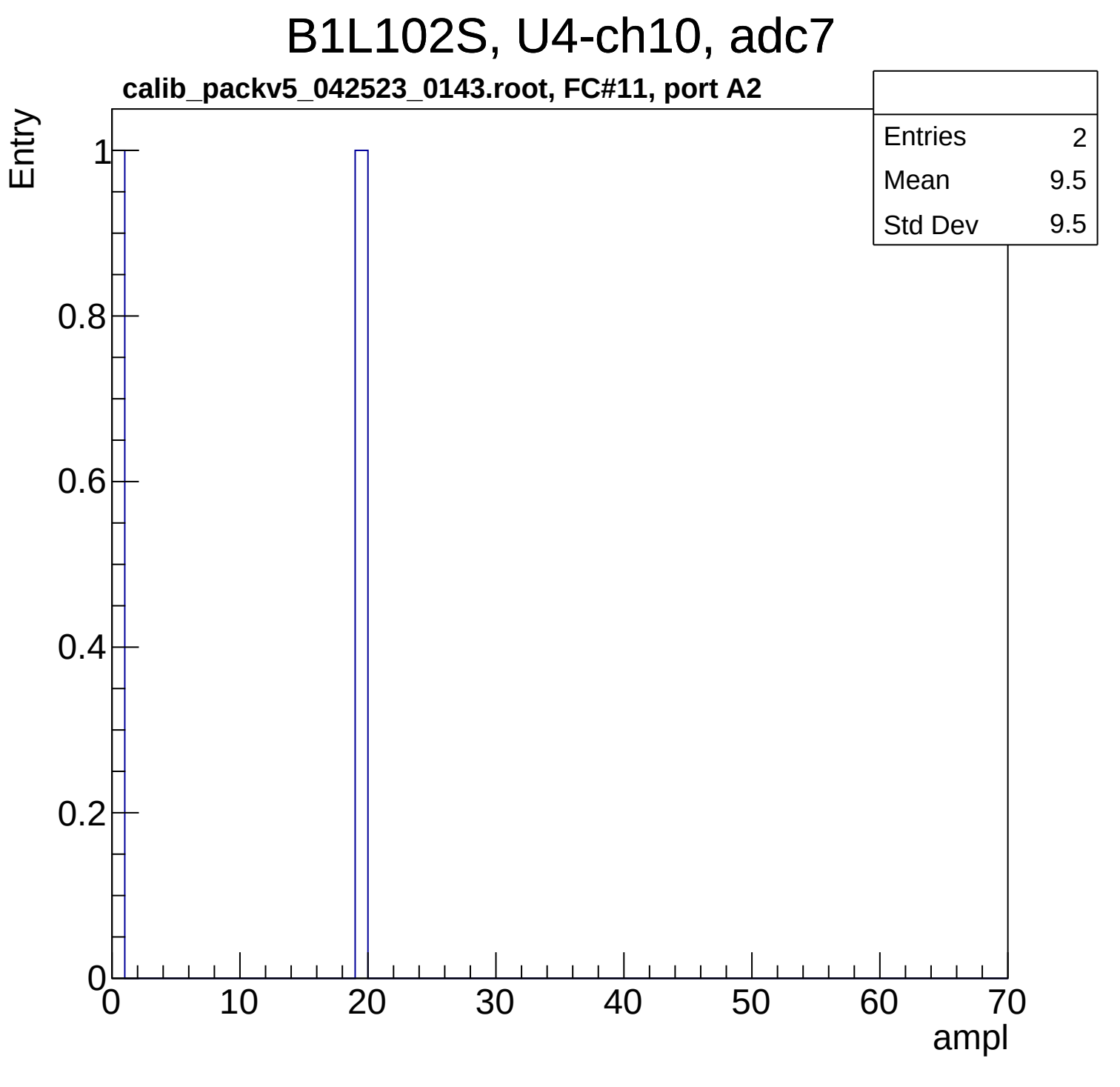

B1L102S, U4-ch10, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 42.11
Std Dev 3.298
Gaus mean : 42.7184
Gaus Width: 3.1537
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch10, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 57
Mean 48.04
Std Dev 3.704
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch10, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 53.66
Std Dev 3.744
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch10, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 57.47
Std Dev 8.47
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch10, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 15
Mean 61.4
Std Dev 1.451
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L102S, U4-ch10, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 9.5
Std Dev 9.5
Entry
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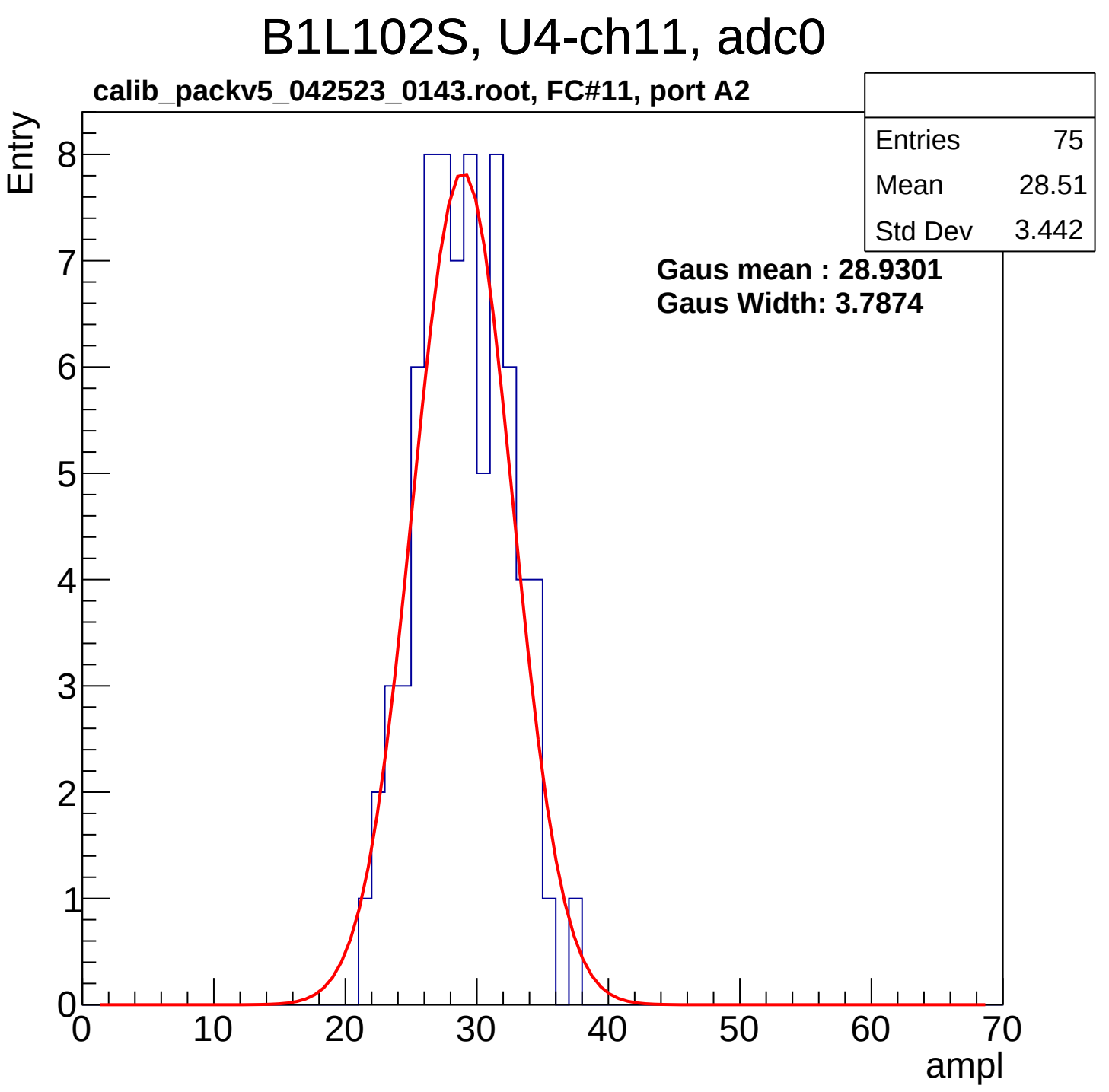
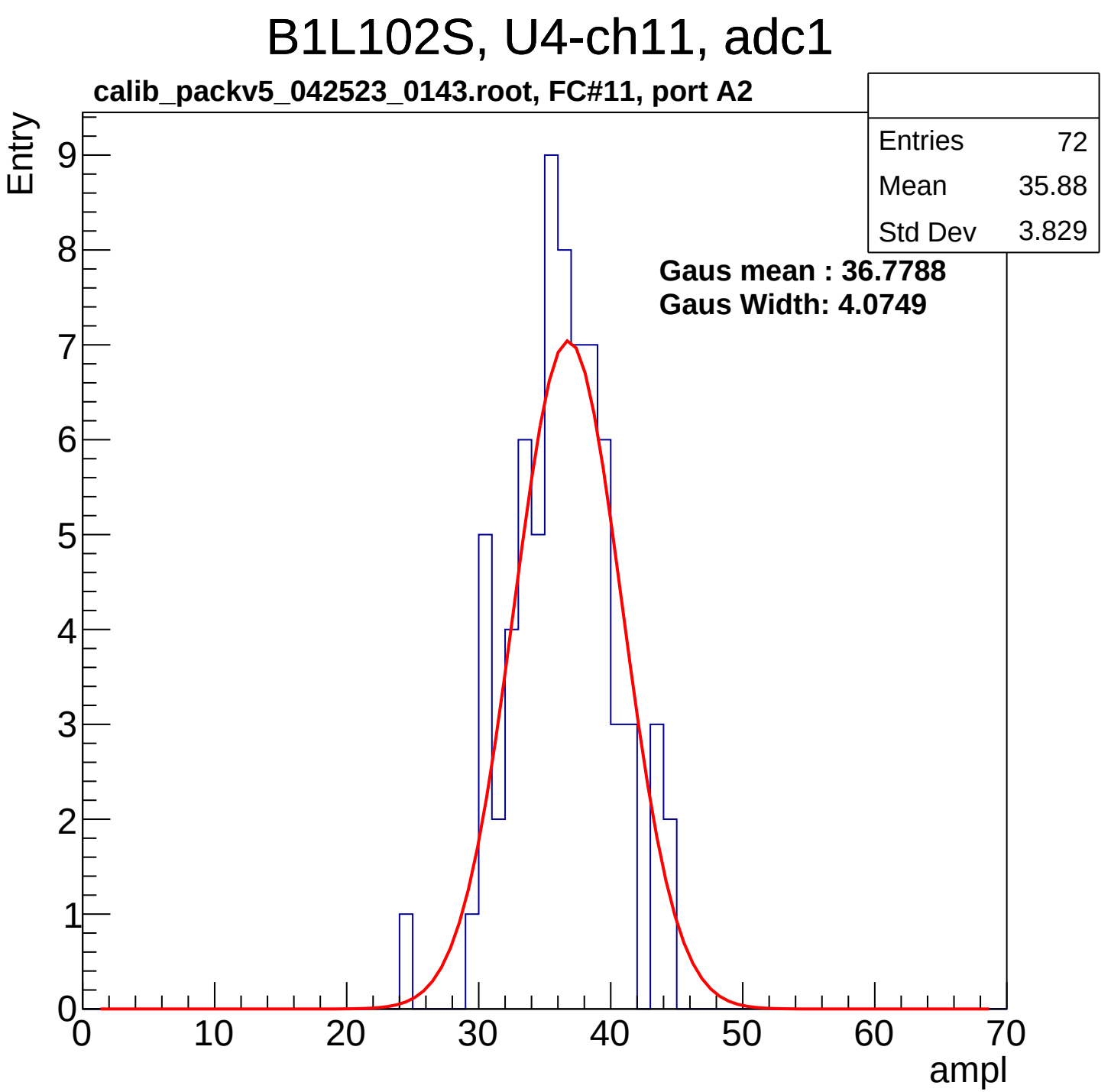
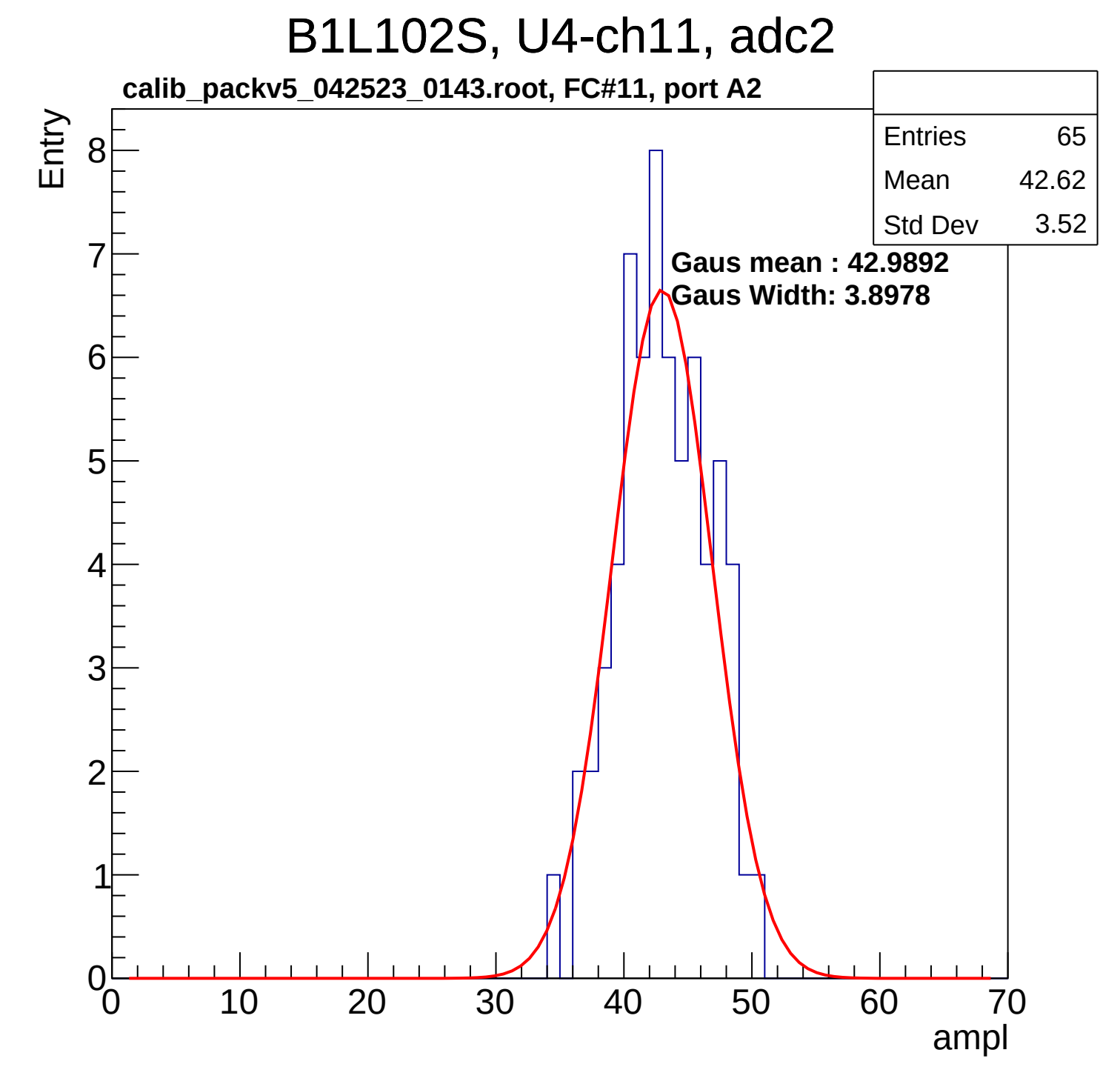
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch11, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 28.51
Std Dev 3.442
Gaus mean : 28.9301
Gaus Width: 3.7874
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch11, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 72
Mean 35.88
Std Dev 3.829
Gaus mean : 36.7788
Gaus Width: 4.0749
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch11, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 42.62
Std Dev 3.52
Gaus mean : 42.9892
Gaus Width: 3.8978
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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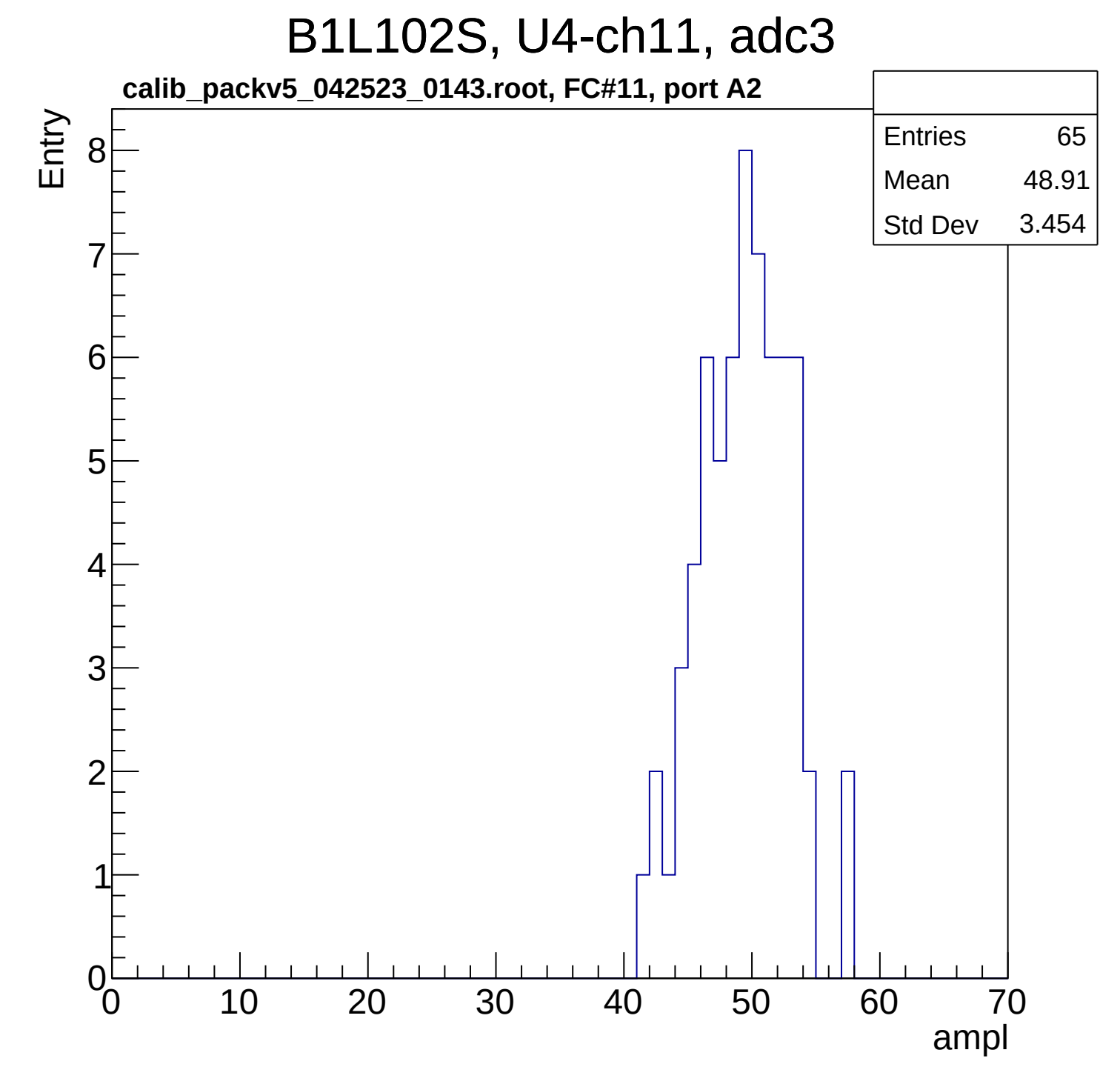
B1L102S, U4-ch11, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 48.91
Std Dev 3.454
Entry
ampl
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1
2
3
4
5
6
7
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0
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60
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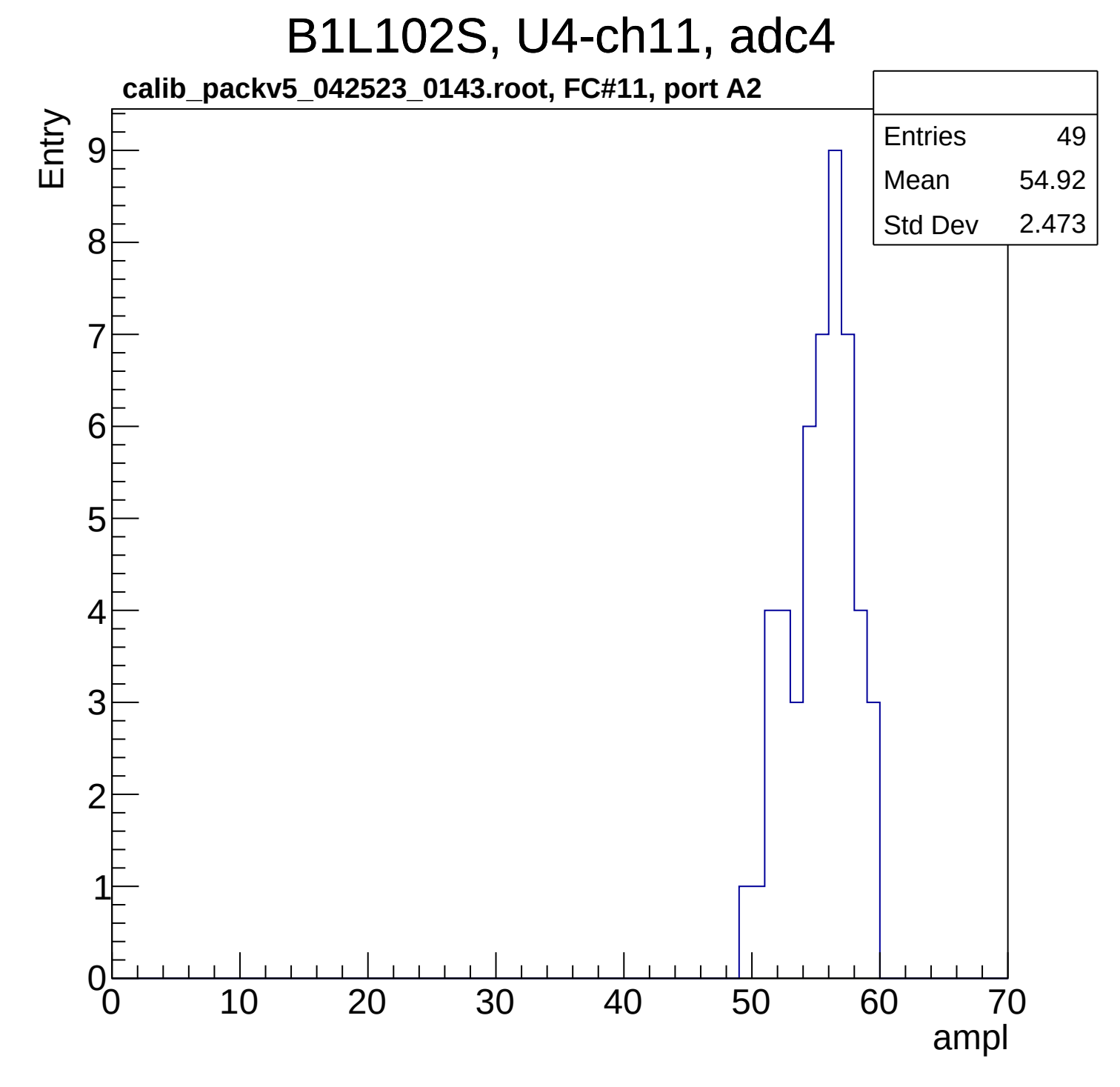
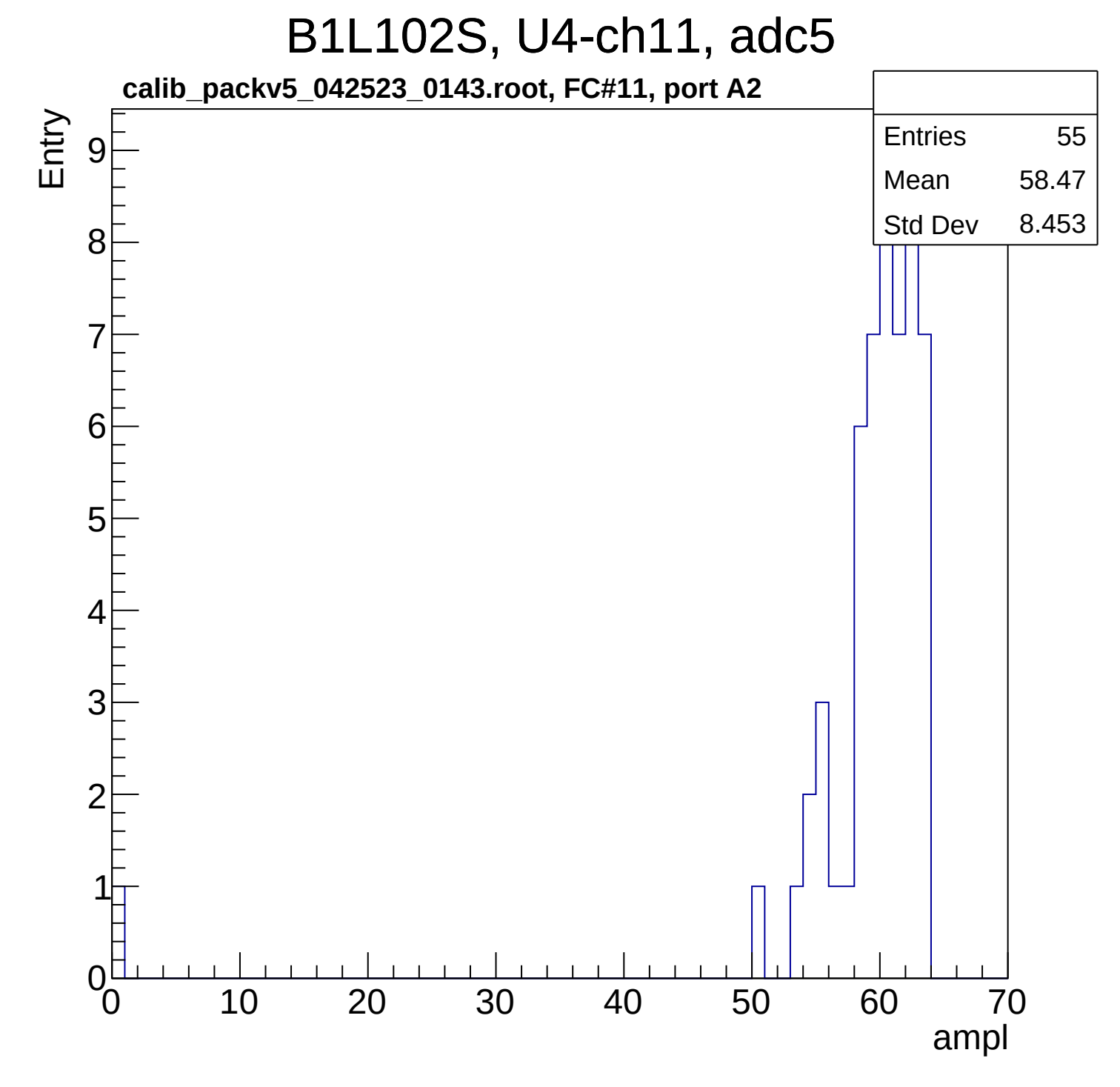

B1L102S, U4-ch11, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 54.92
Std Dev 2.473
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch11, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 58.47
Std Dev 8.453
Entry
ampl
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3
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0
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60
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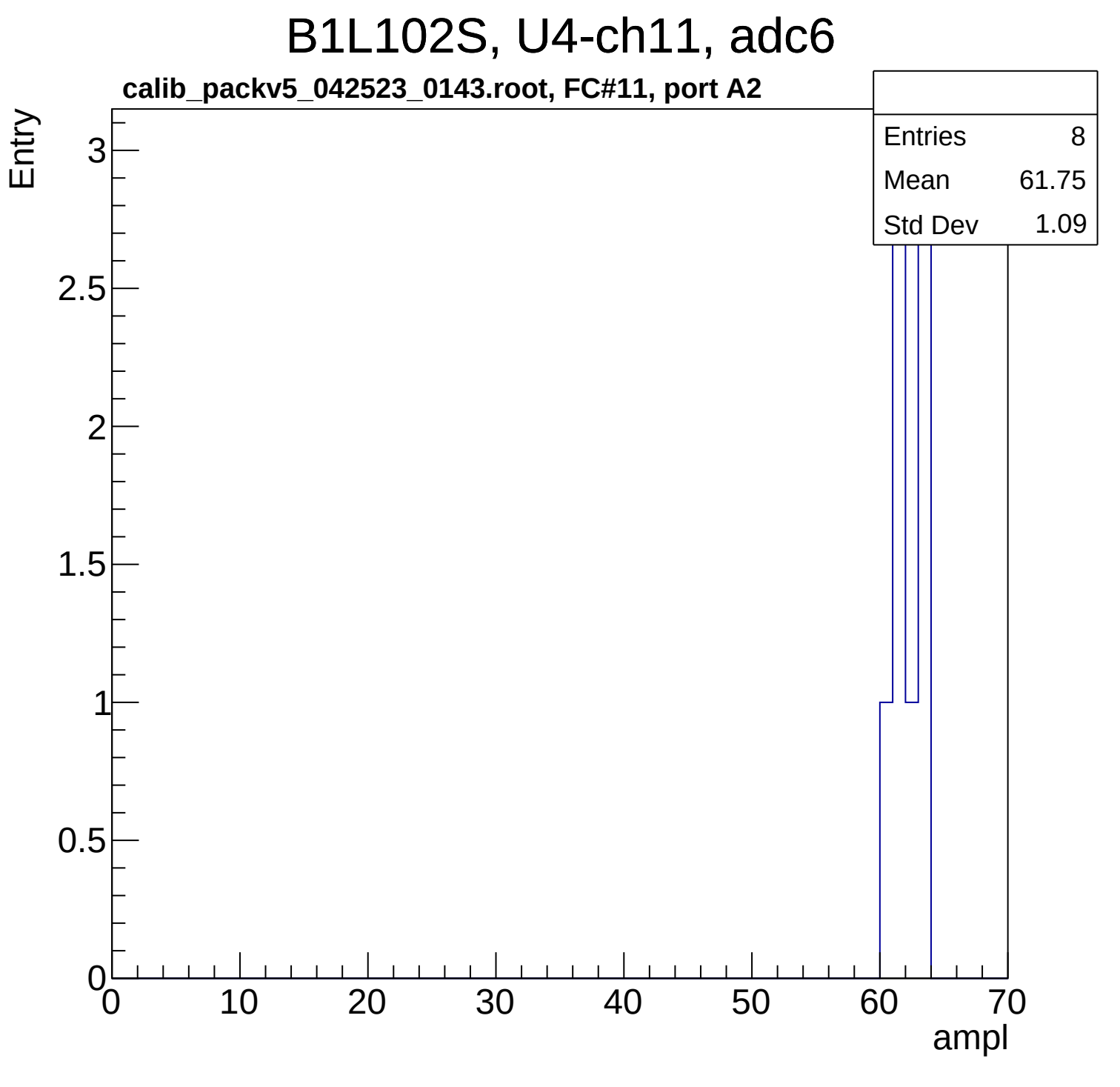
B1L102S, U4-ch11, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 8
Mean 61.75
Std Dev 1.09
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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40
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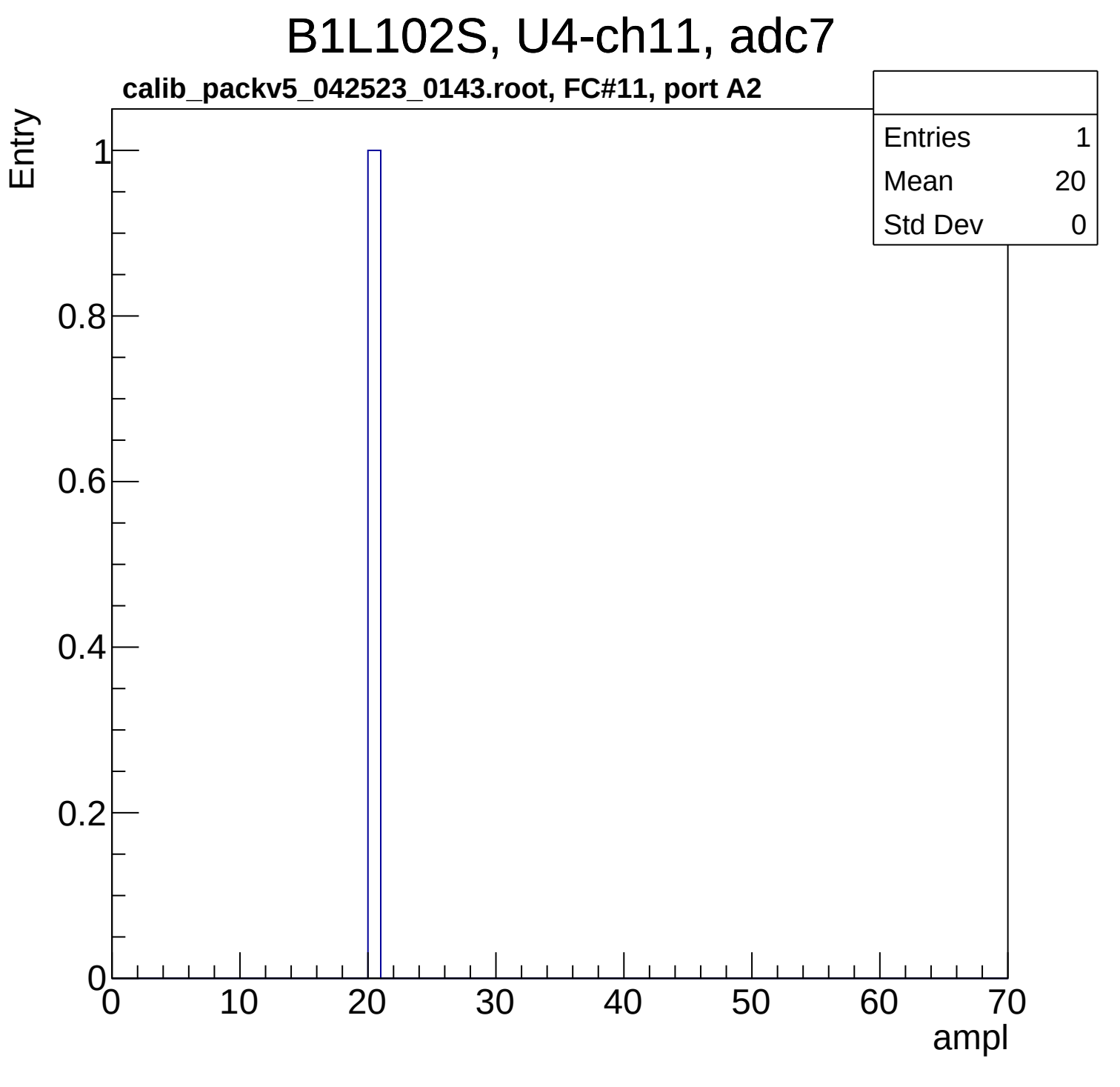
B1L102S, U4-ch11, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 20
Std Dev 0
Entry
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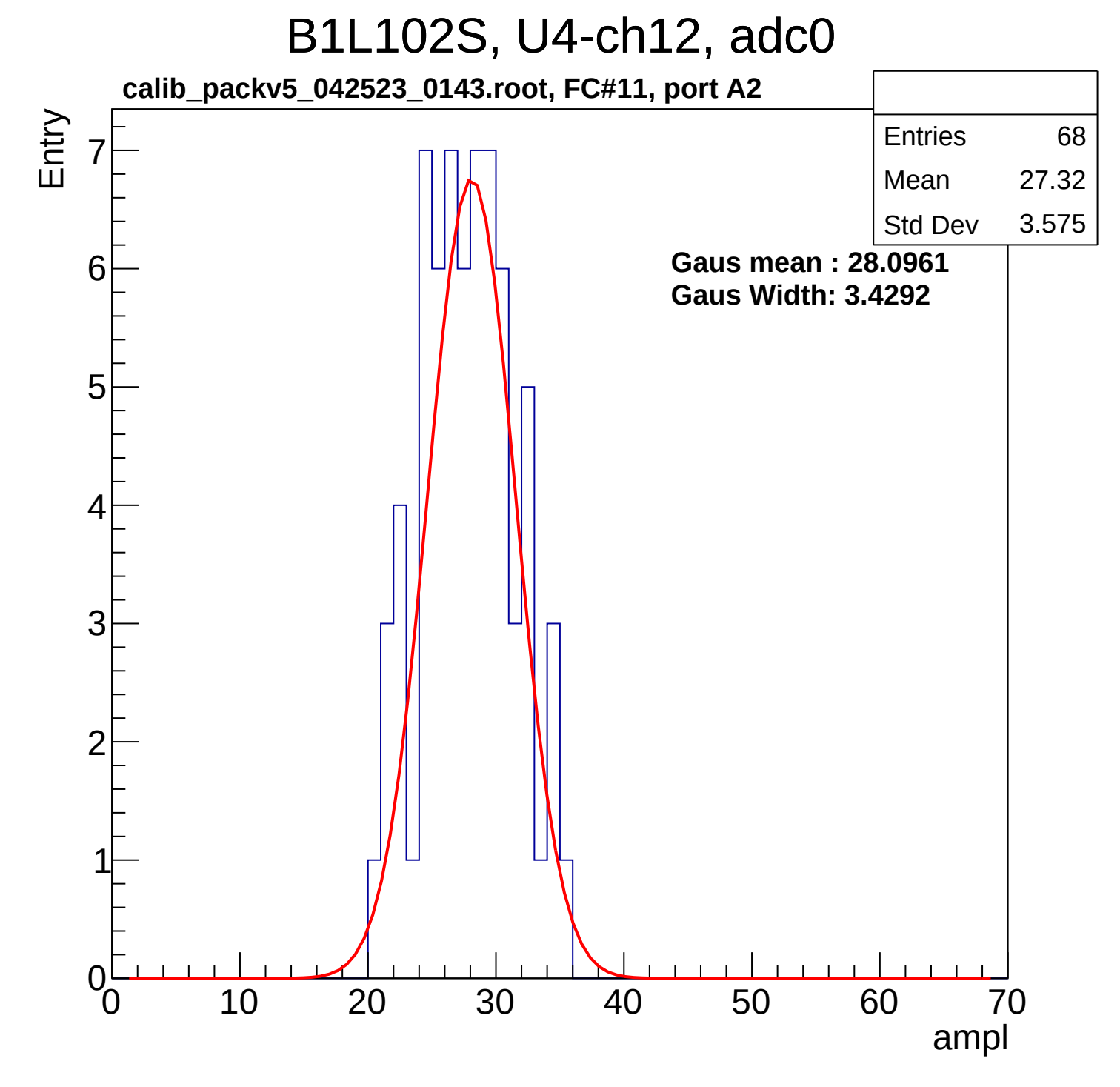
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch12, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 27.32
Std Dev 3.575
Gaus mean : 28.0961
Gaus Width: 3.4292
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
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60
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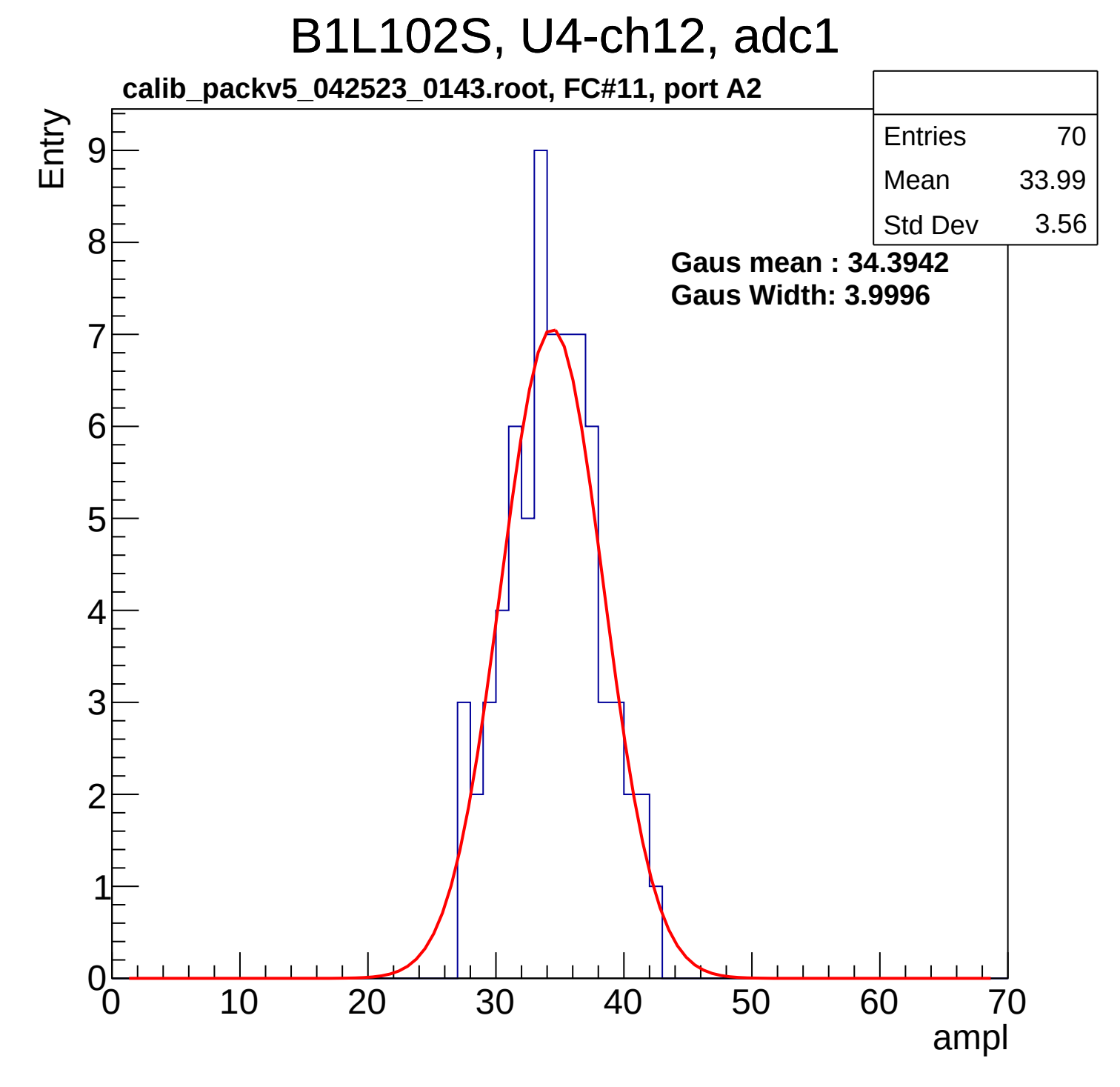
B1L102S, U4-ch12, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 33.99
Std Dev 3.56
Gaus mean : 34.3942
Gaus Width: 3.9996
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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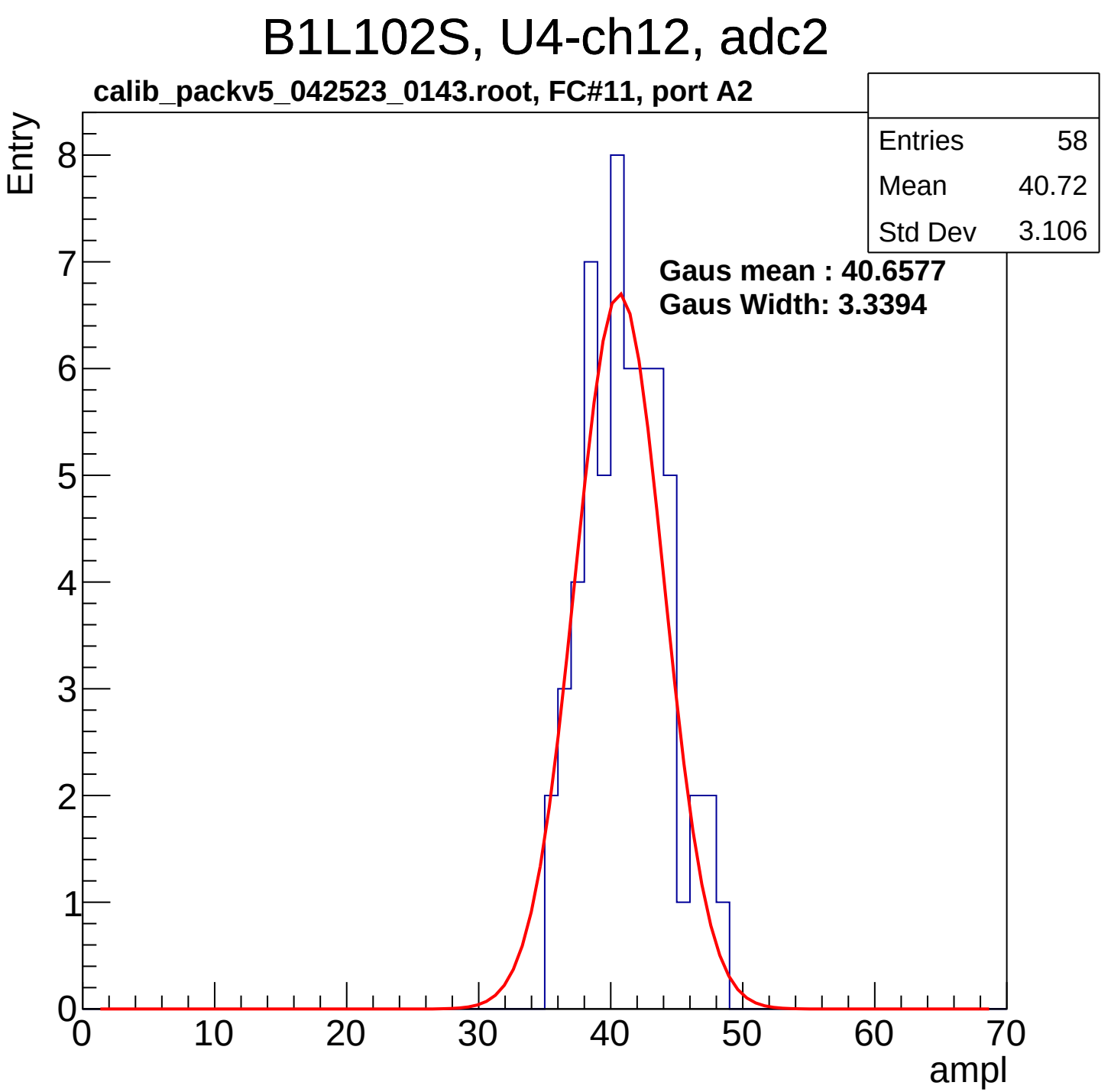
B1L102S, U4-ch12, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 40.72
Std Dev 3.106
Gaus mean : 40.6577
Gaus Width: 3.3394
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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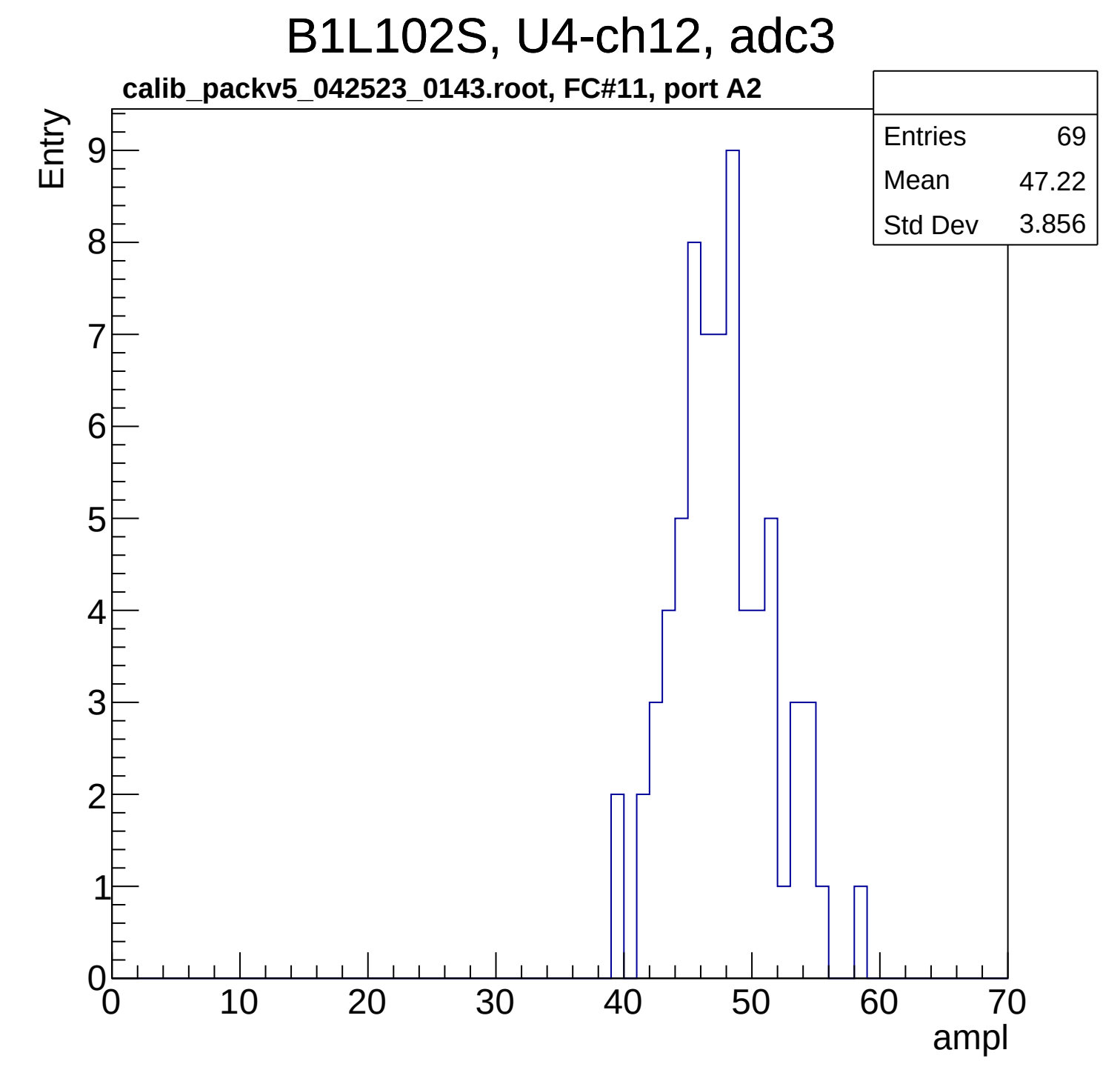
B1L102S, U4-ch12, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 47.22
Std Dev 3.856
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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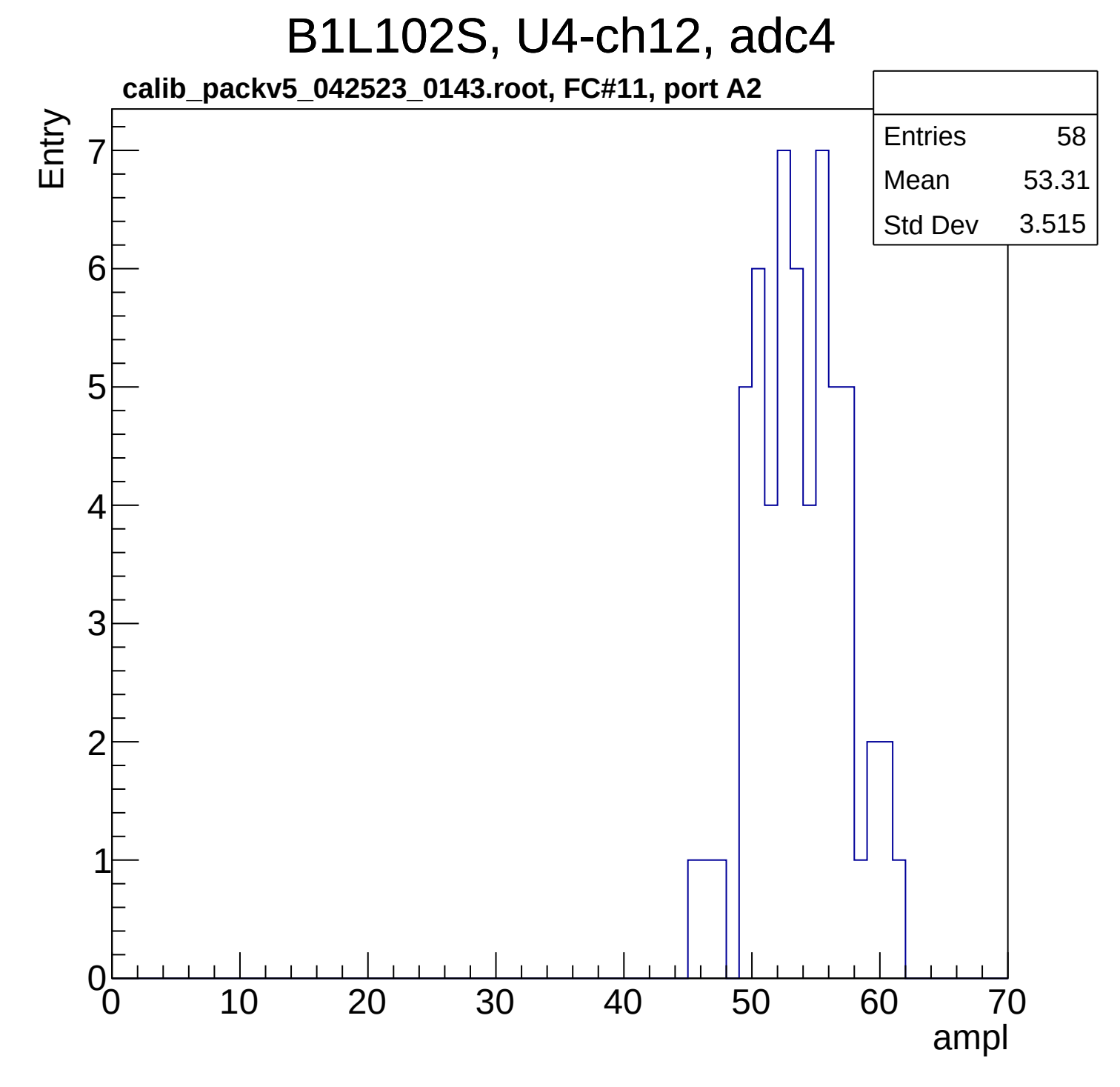
B1L102S, U4-ch12, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 53.31
Std Dev 3.515
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
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60
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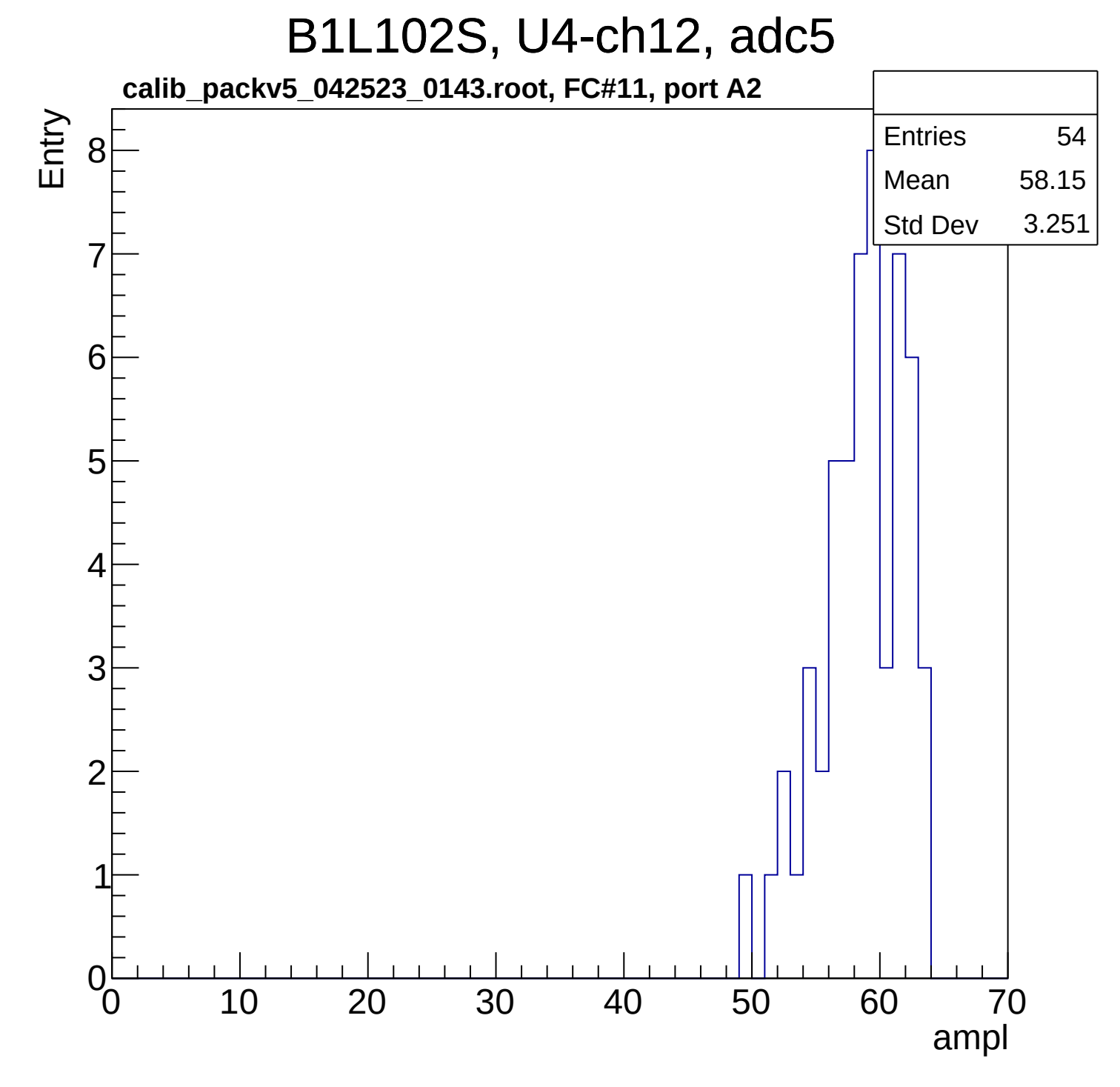
B1L102S, U4-ch12, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 58.15
Std Dev 3.251
Entry
ampl
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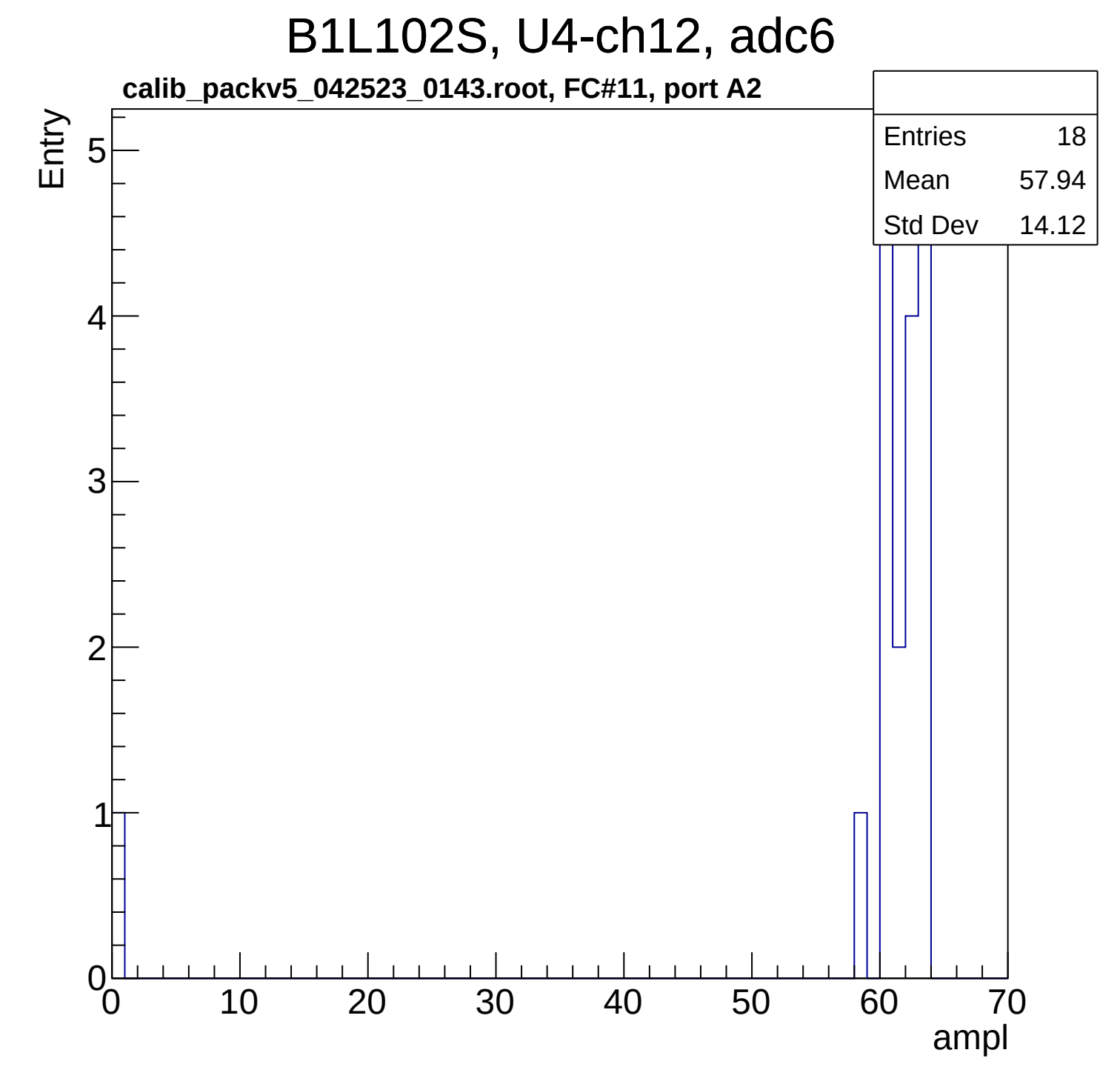
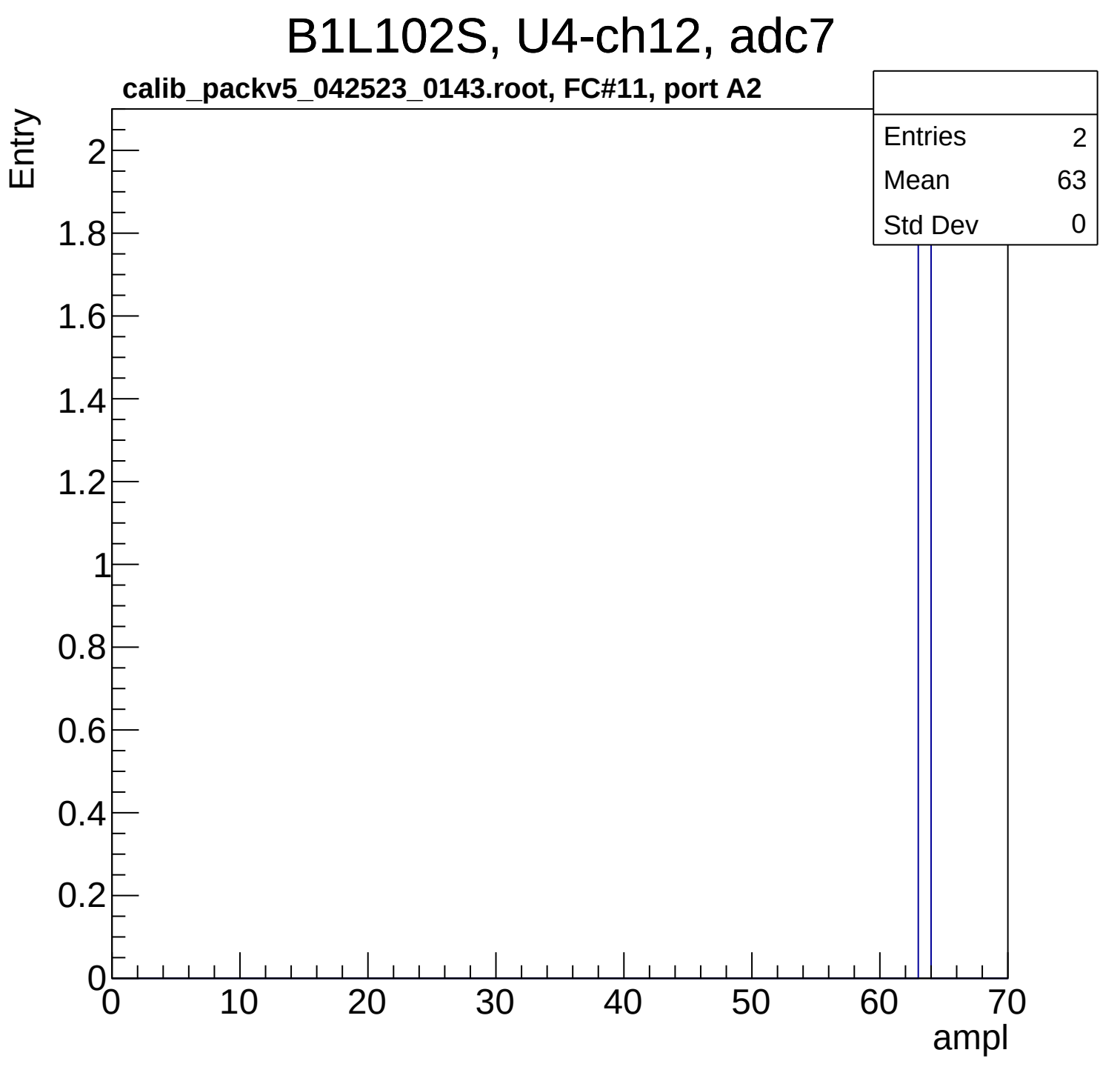
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch12, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 18
Mean 57.94
Std Dev 14.12
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L102S, U4-ch12, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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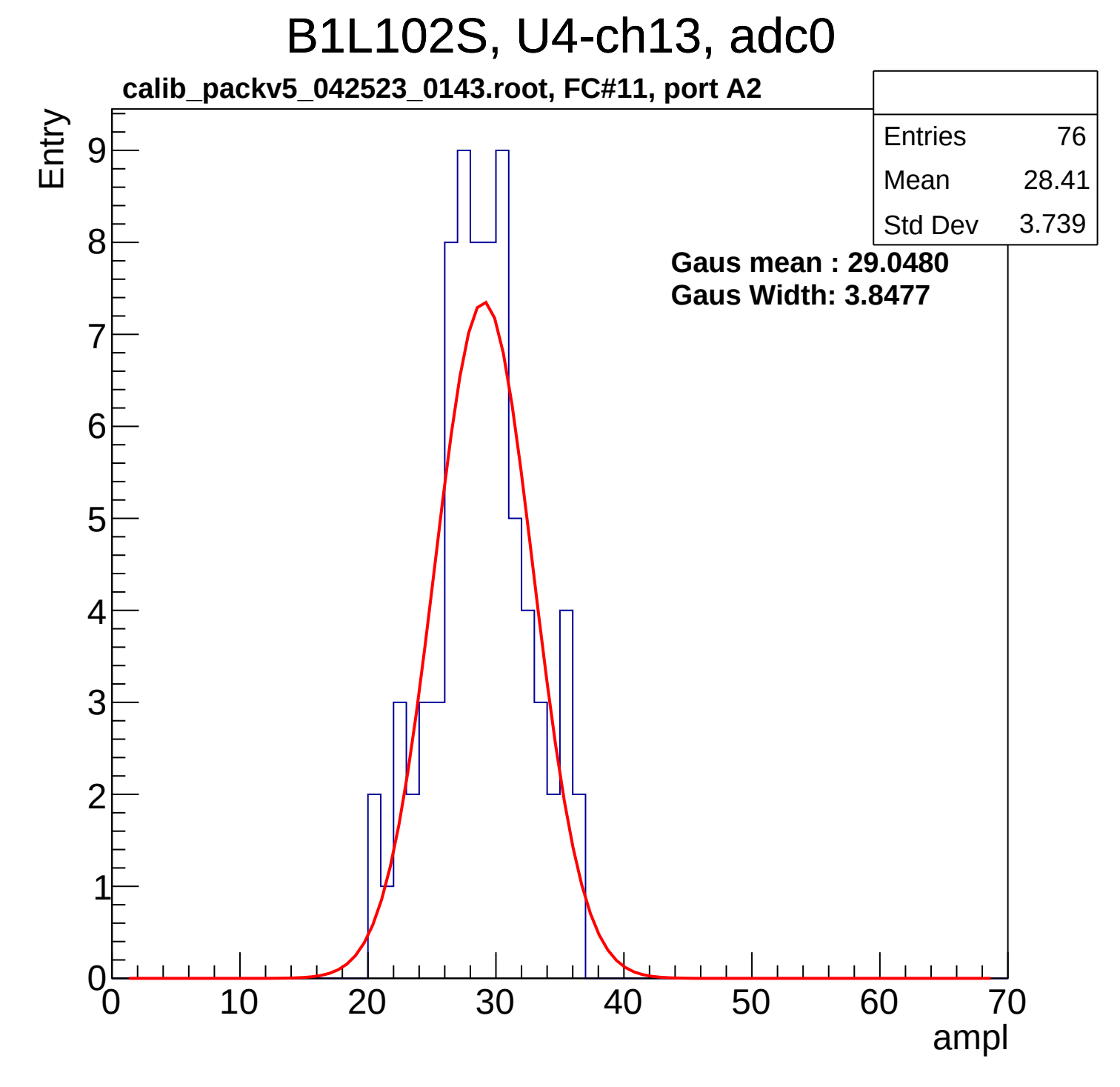
B1L102S, U4-ch13, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 28.41
Std Dev 3.739
Gaus mean : 29.0480
Gaus Width: 3.8477
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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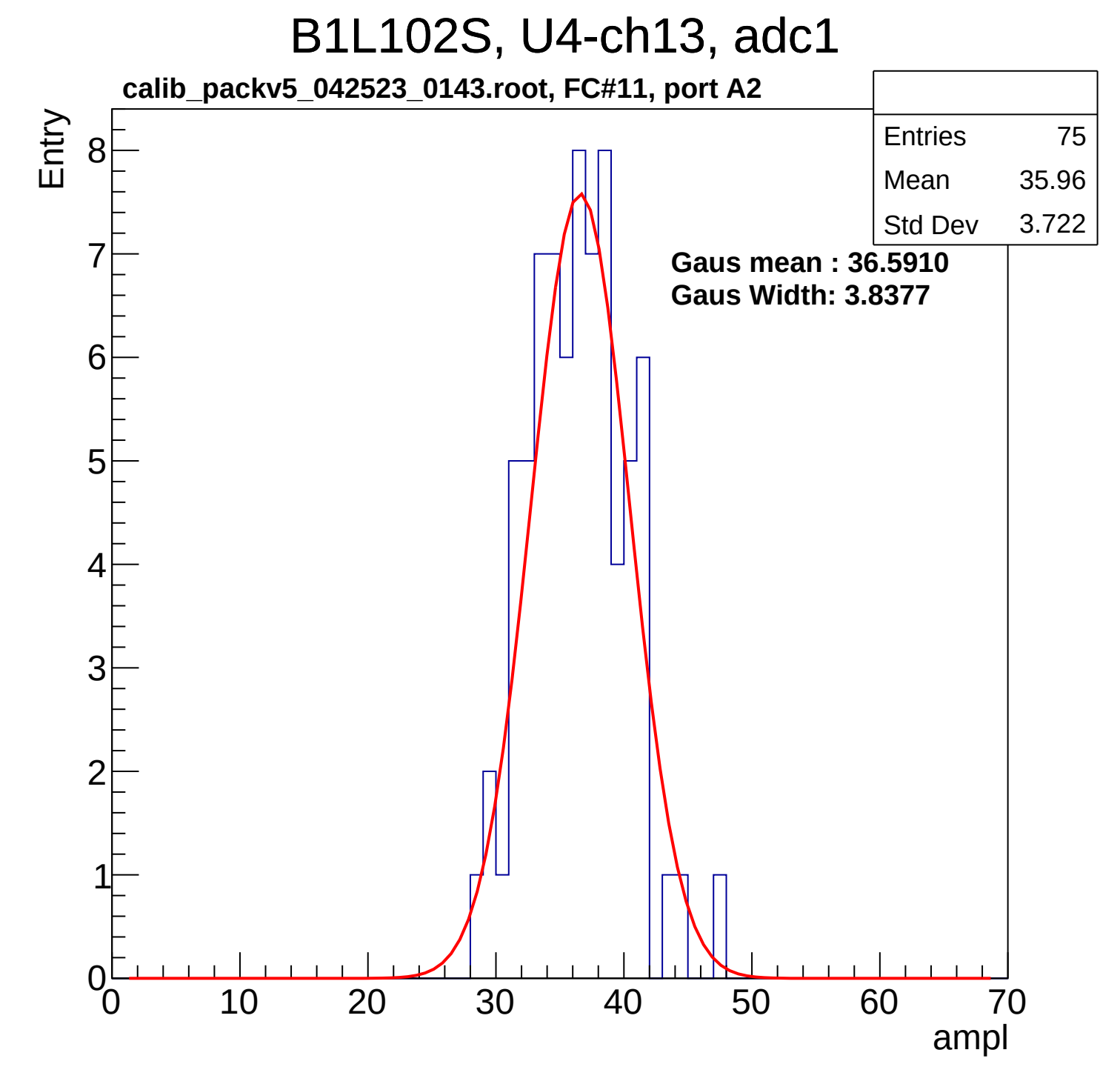
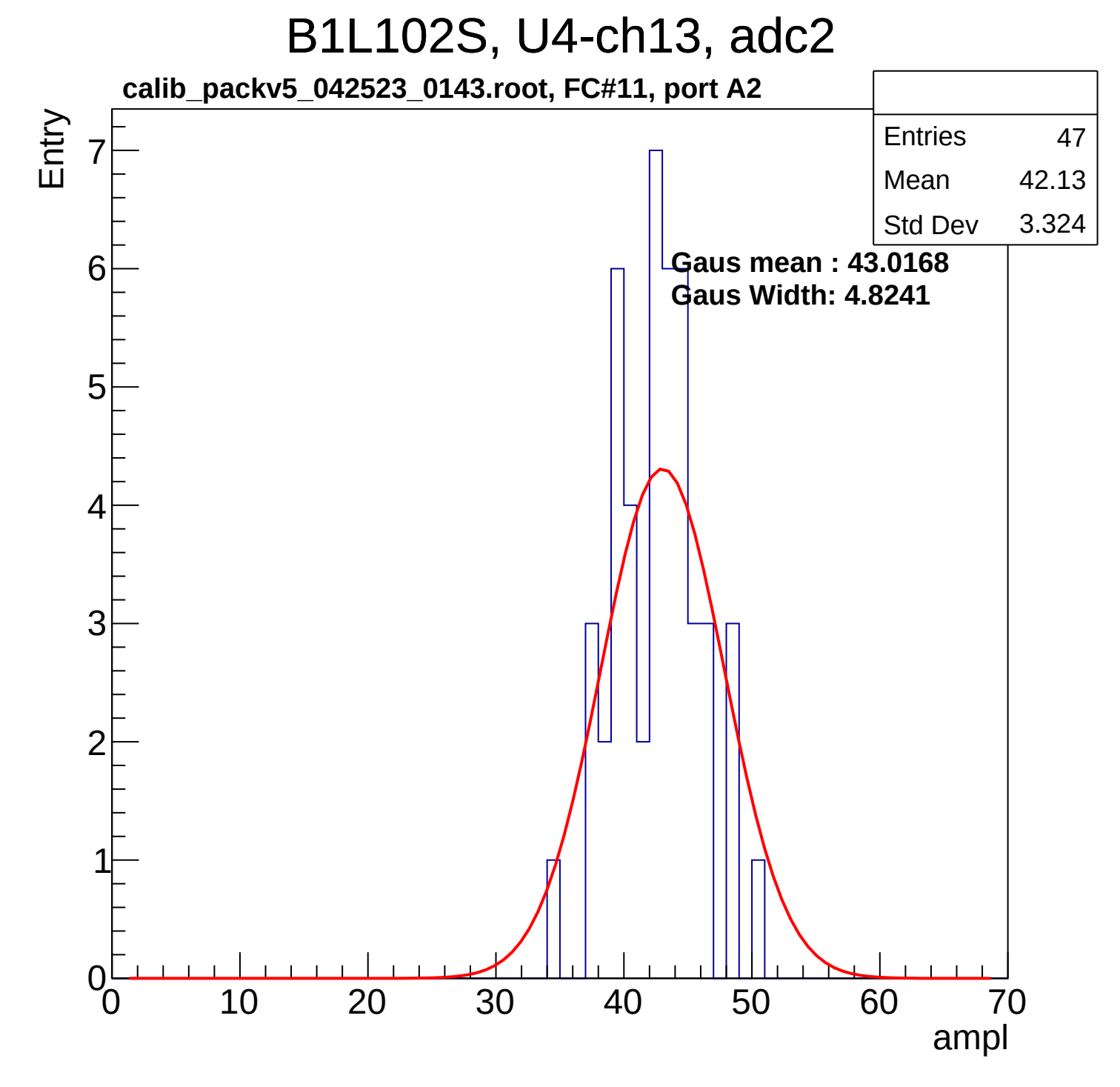

B1L102S, U4-ch13, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 35.96
Std Dev 3.722
Gaus mean : 36.5910
Gaus Width: 3.8377
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch13, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 47
Mean 42.13
Std Dev 3.324
Gaus mean : 43.0168
Gaus Width: 4.8241
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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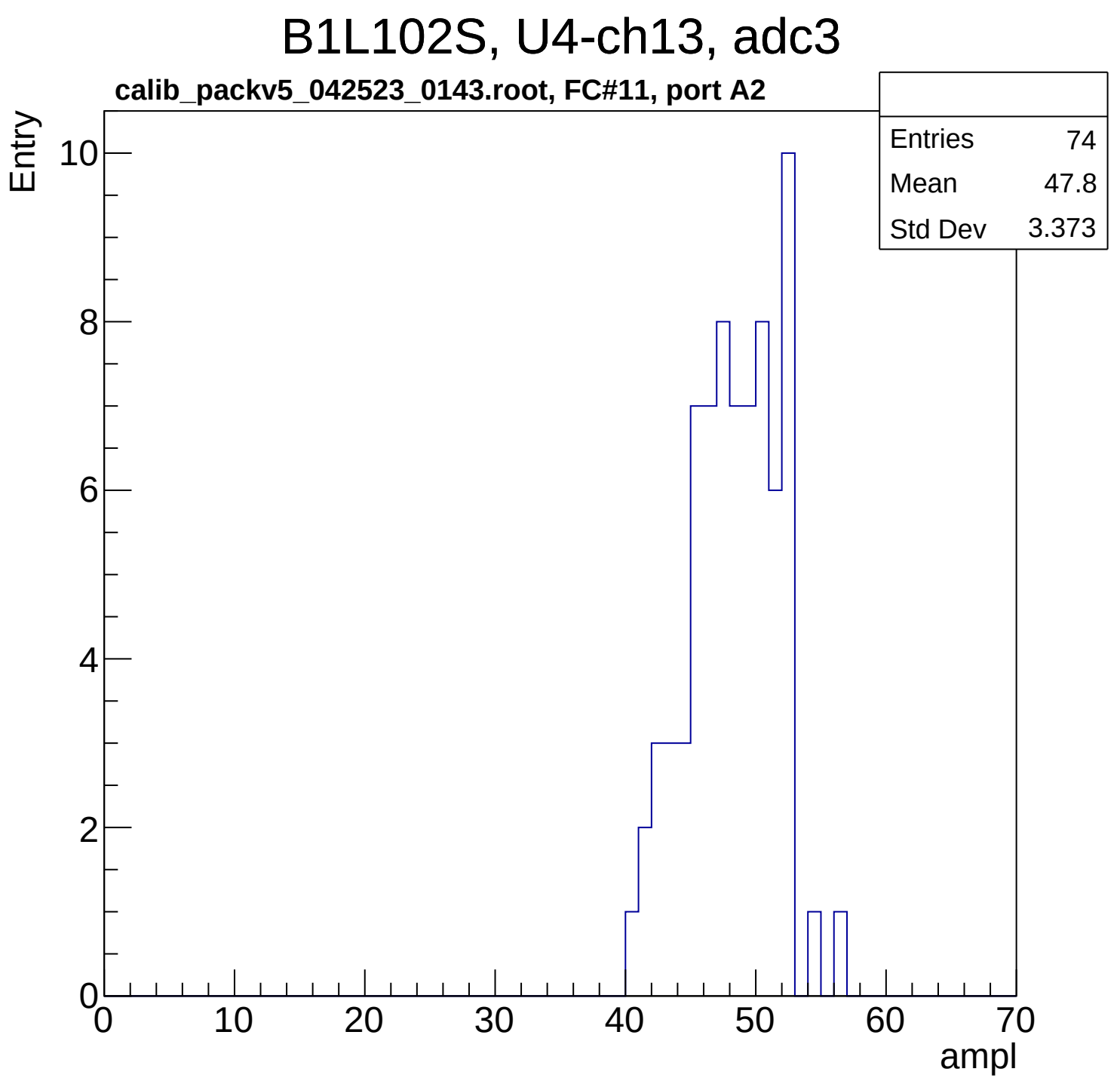
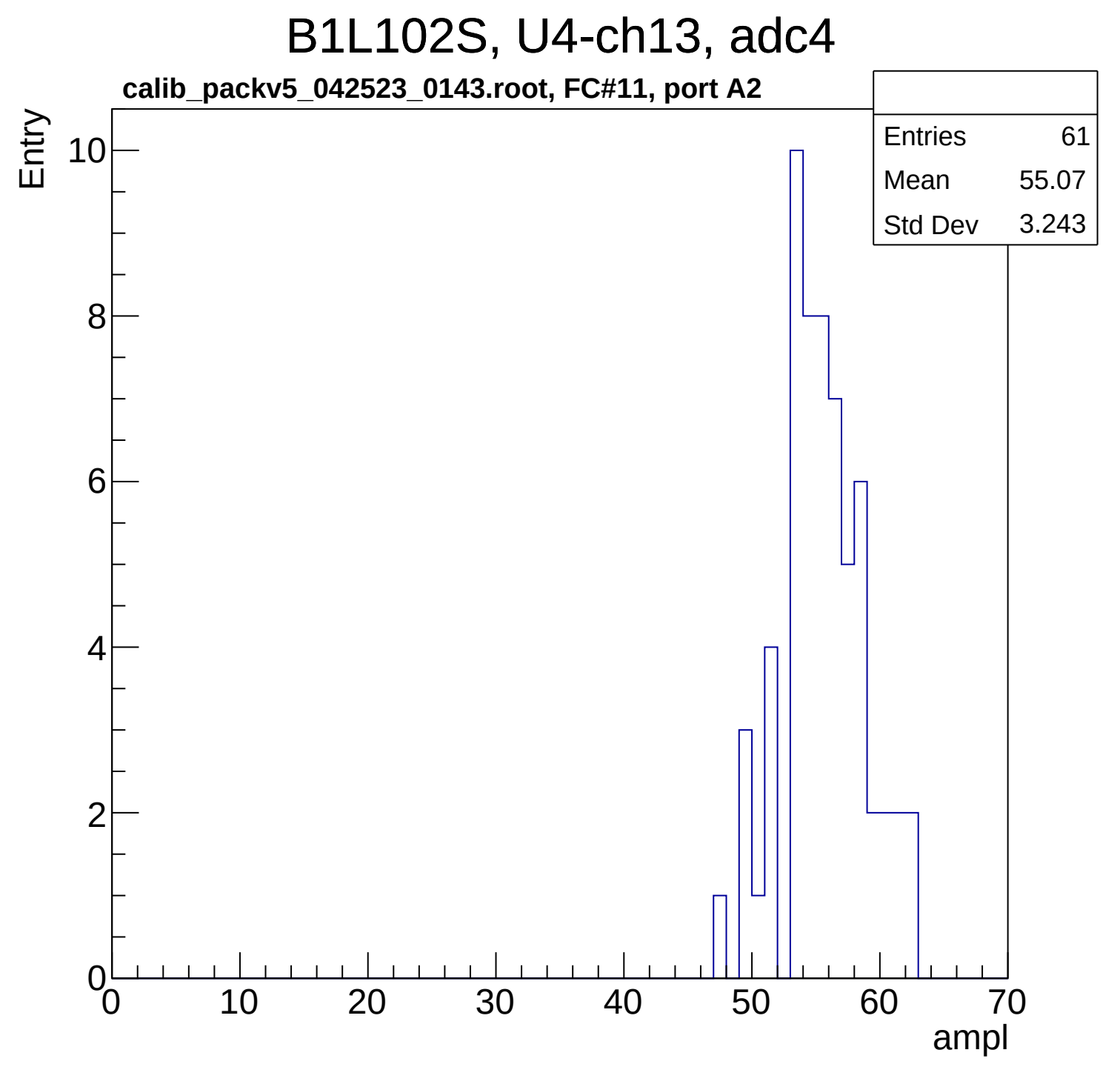
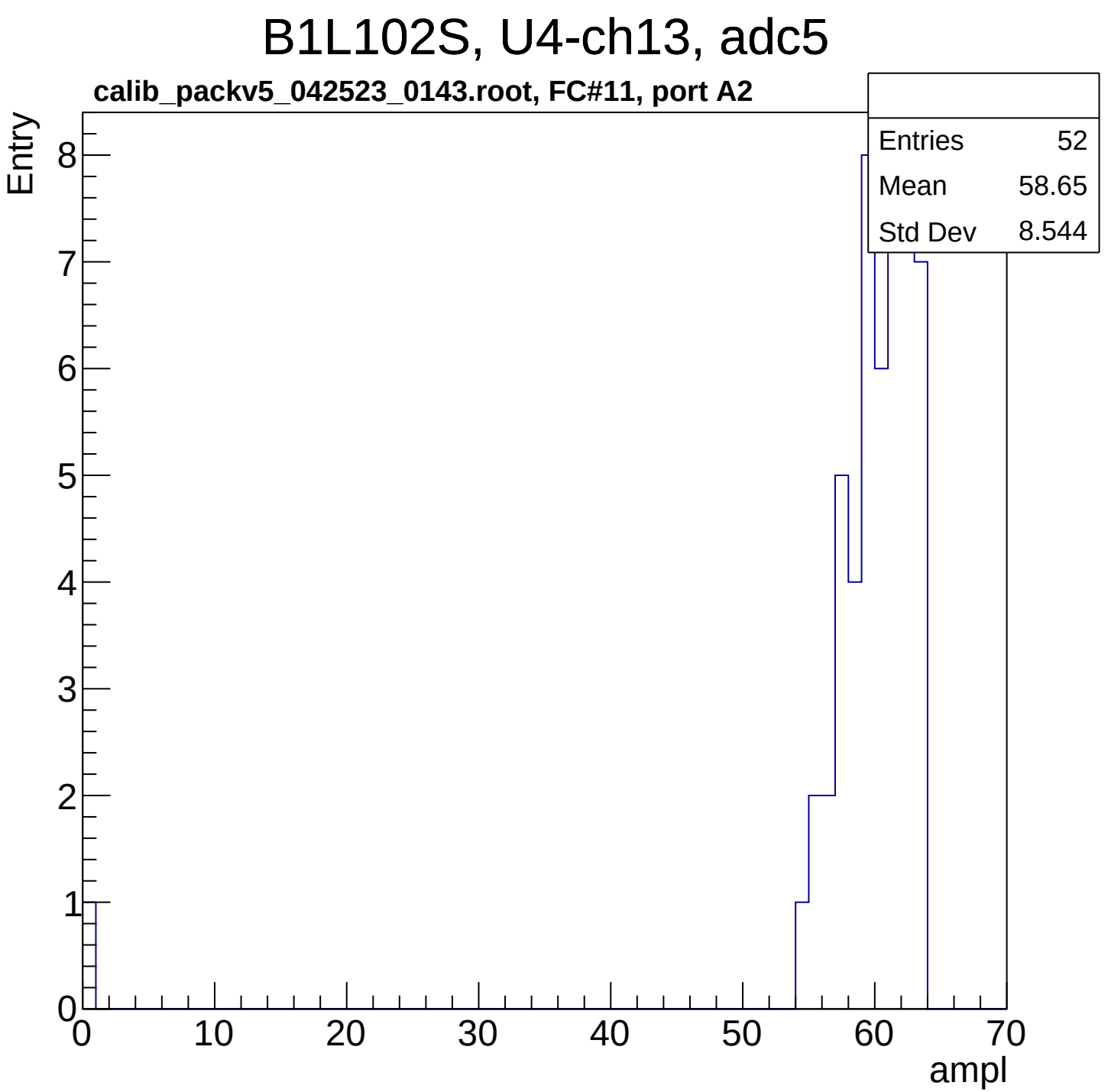

B1L102S, U4-ch13, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 47.8
Std Dev 3.373
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch13, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 55.07
Std Dev 3.243
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch13, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 52
Mean 58.65
Std Dev 8.544
Entry
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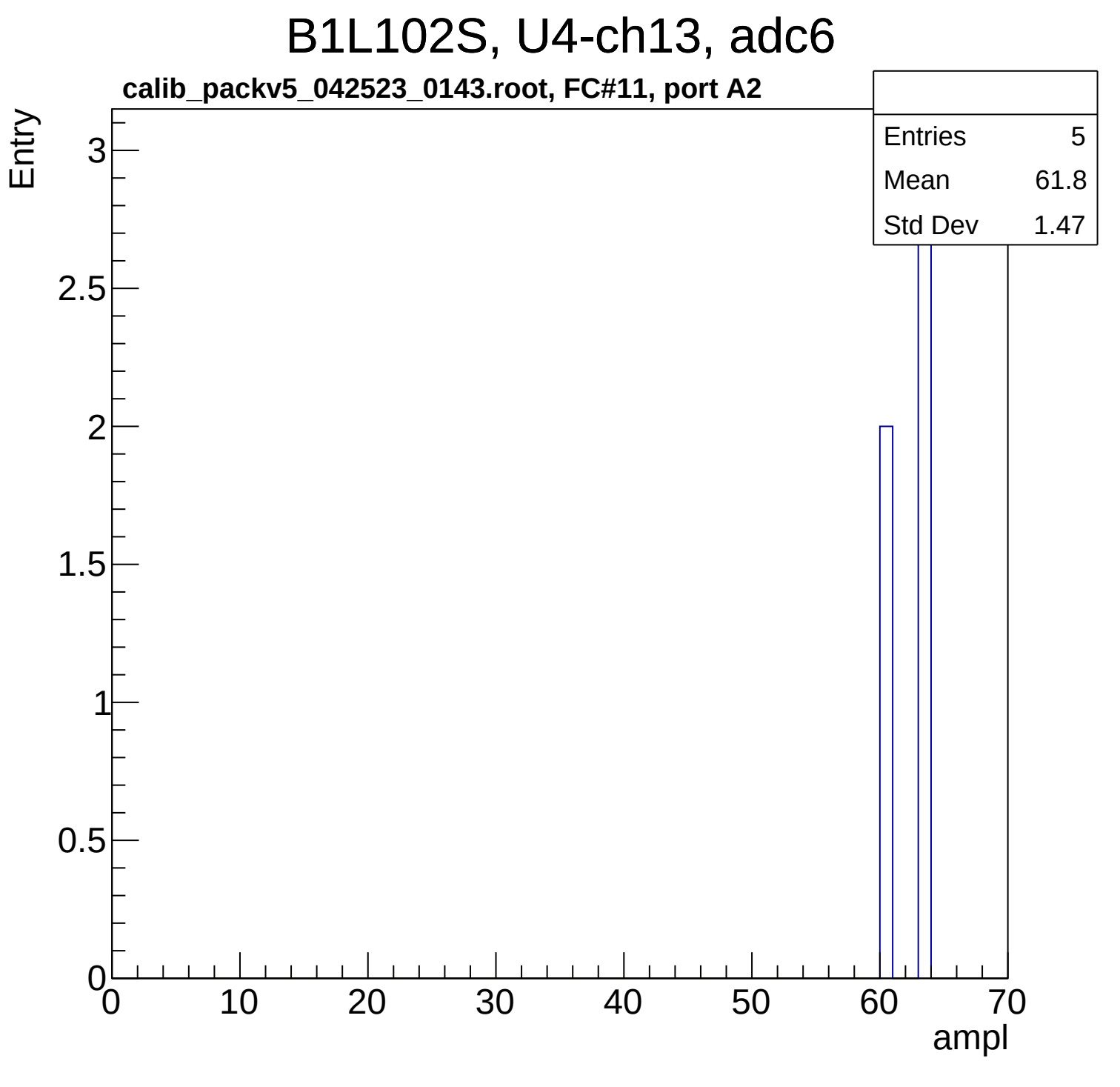
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch13, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 5
Mean 61.8
Std Dev 1.47
Entry
ampl
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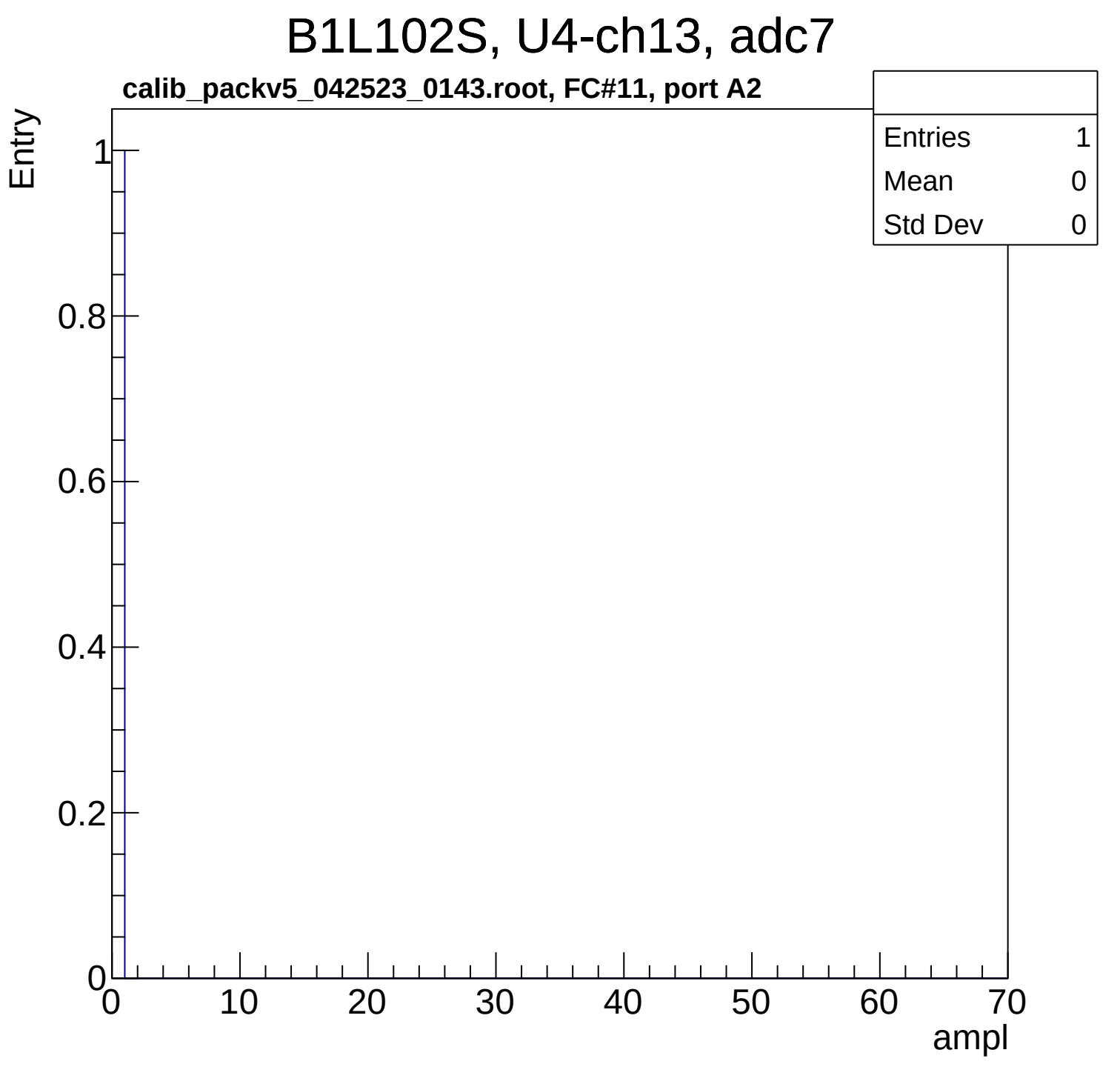
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U4-ch13, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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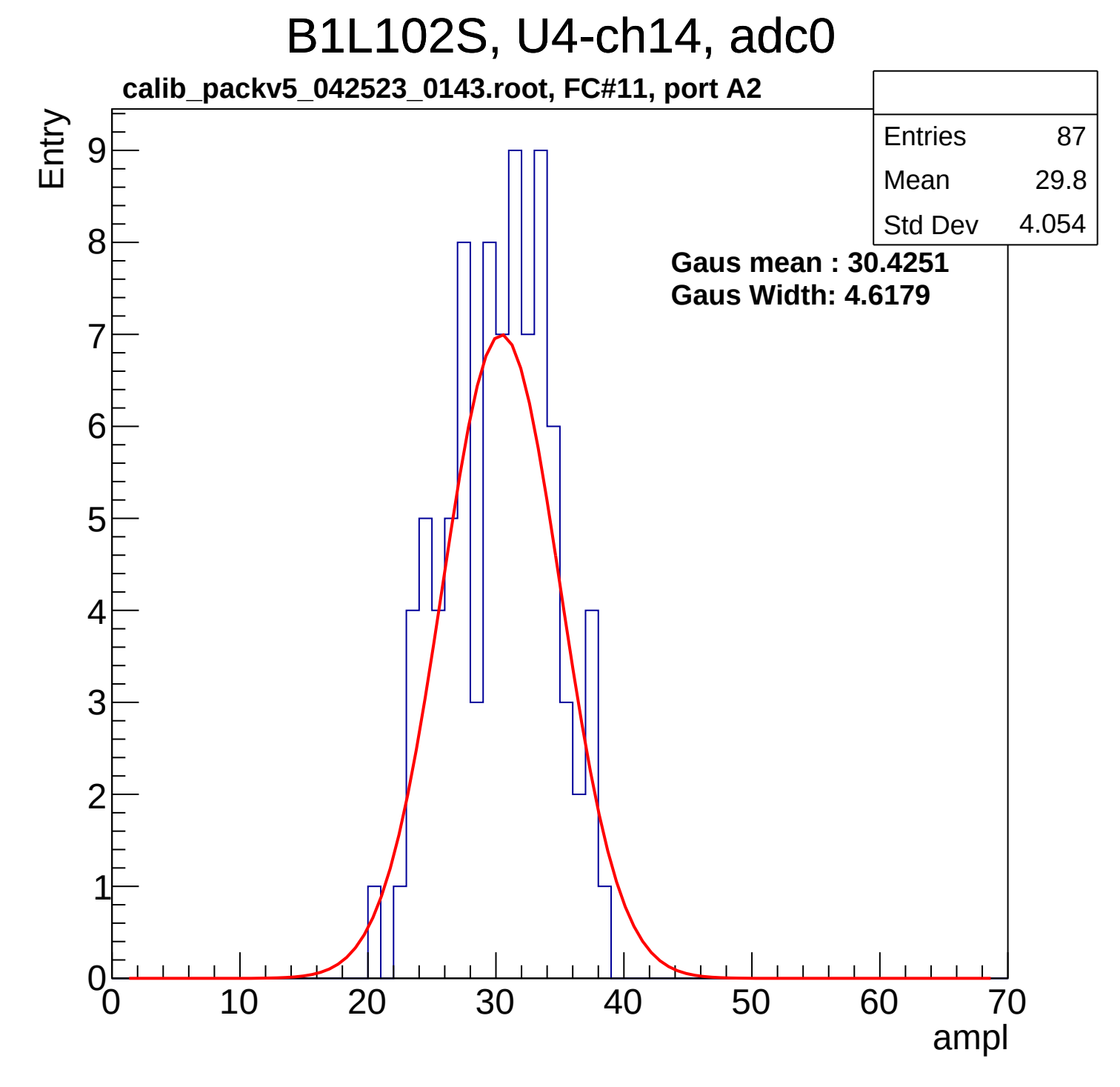
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch14, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 87
Mean 29.8
Std Dev 4.054
Gaus mean : 30.4251
Gaus Width: 4.6179
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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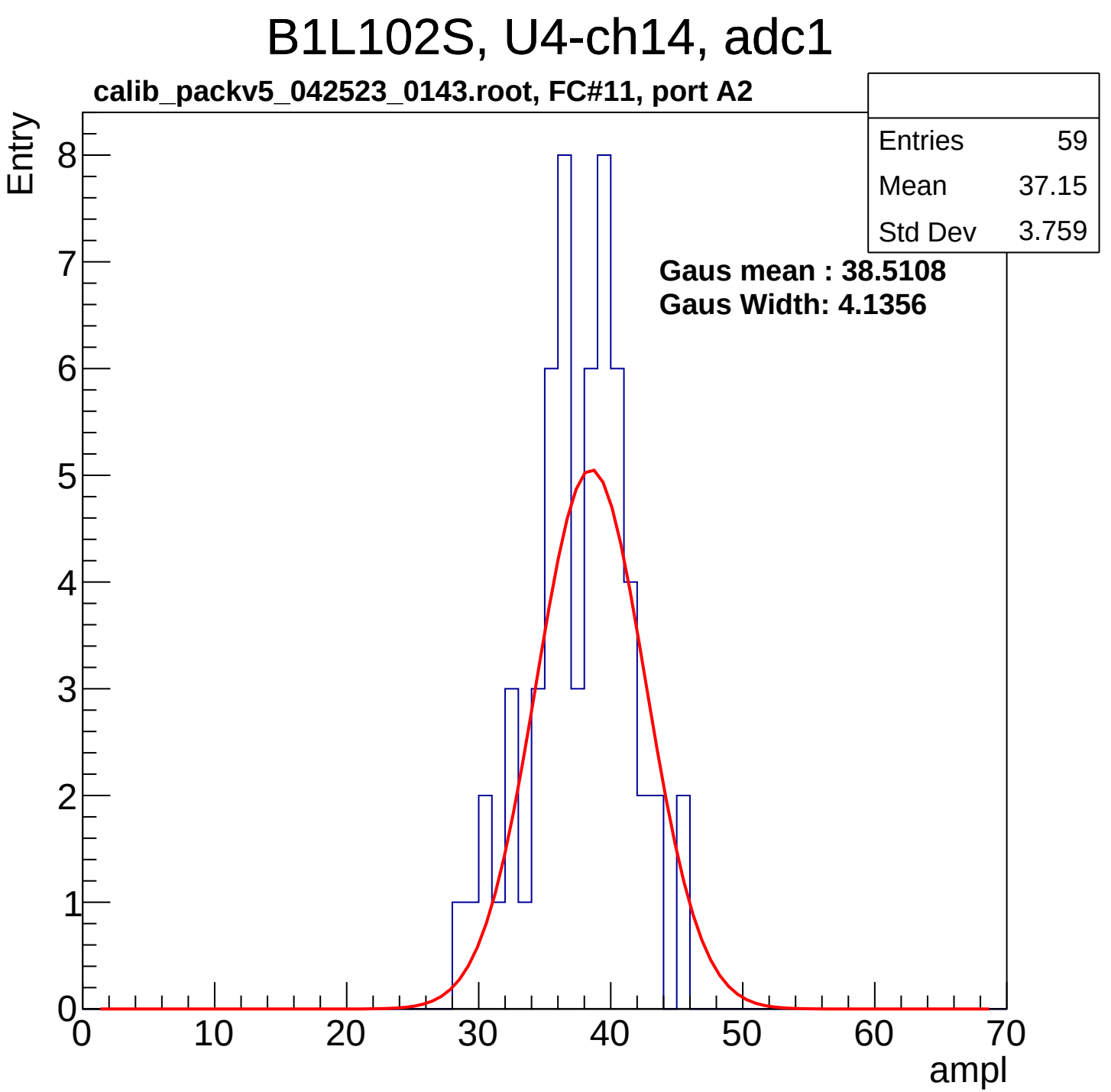
60
70


B1L102S, U4-ch14, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 37.15
Std Dev 3.759
Gaus mean : 38.5108
Gaus Width: 4.1356
Entry
ampl
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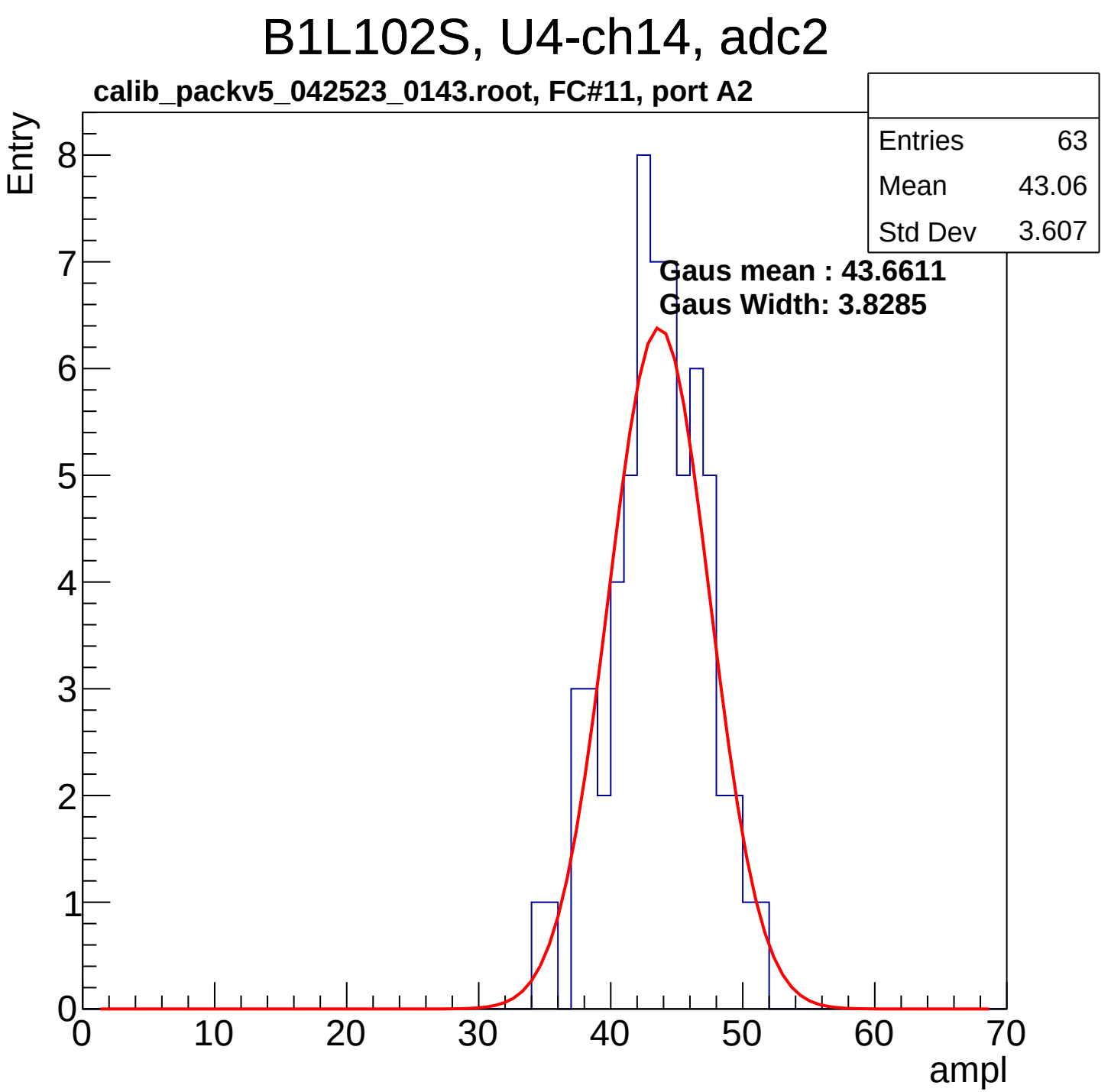
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch14, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 43.06
Std Dev 3.607
Gaus mean : 43.6611
Gaus Width: 3.8285
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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40
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60
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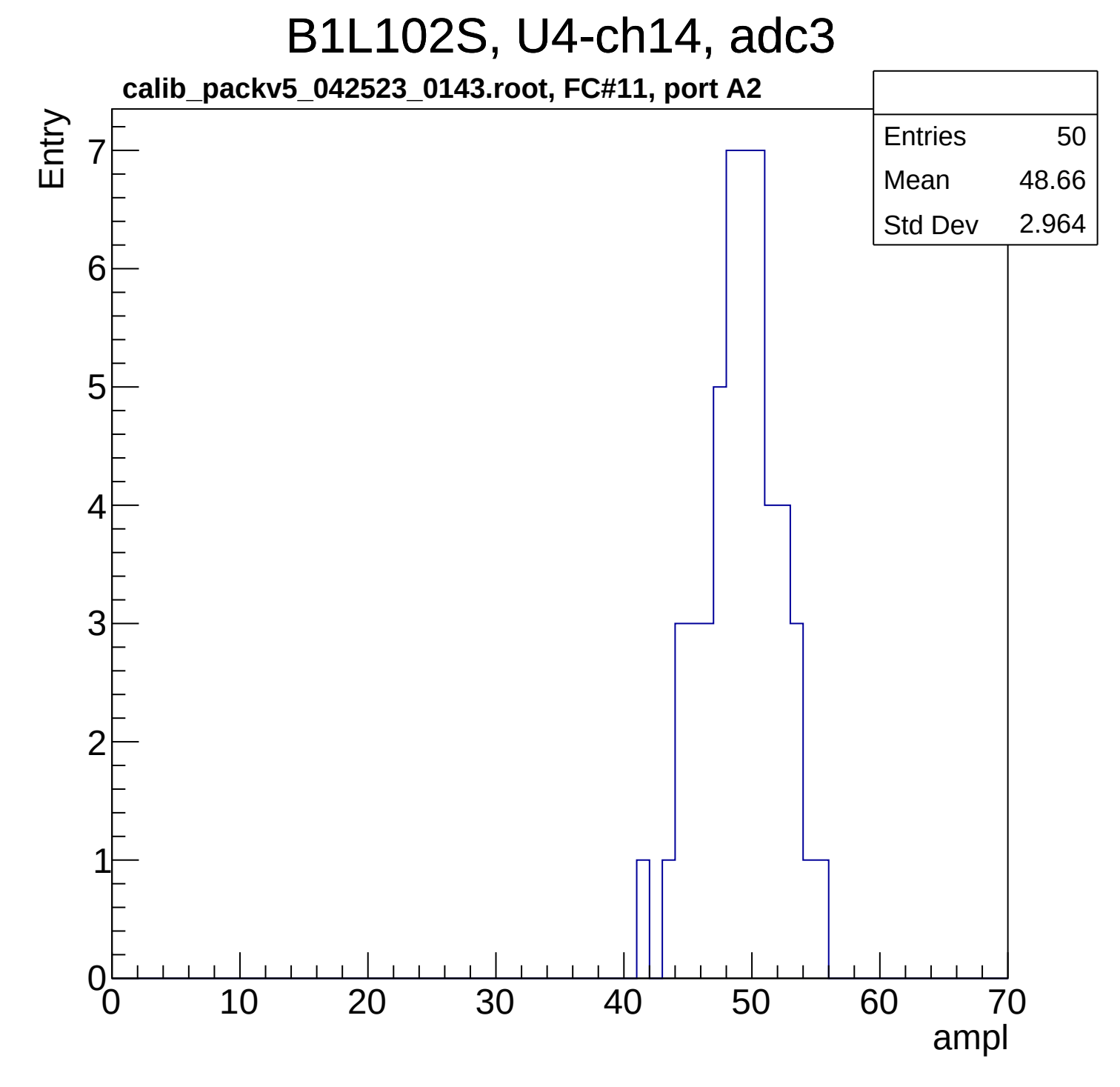
B1L102S, U4-ch14, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 50
Mean 48.66
Std Dev 2.964
Entry
ampl
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4
5
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7
0
10
20
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40
50
60
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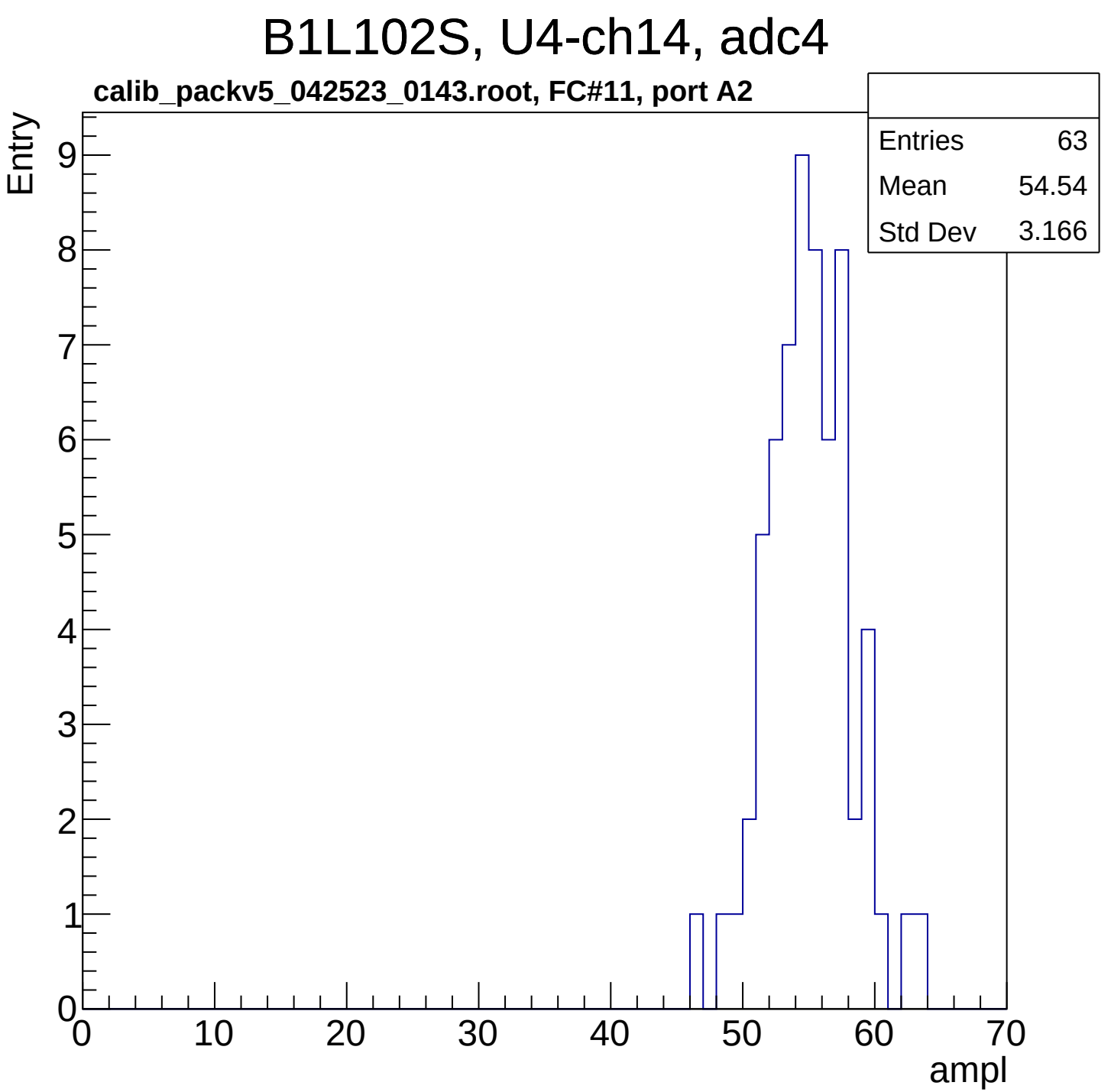
B1L102S, U4-ch14, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 54.54
Std Dev 3.166
Entry
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3
4
5
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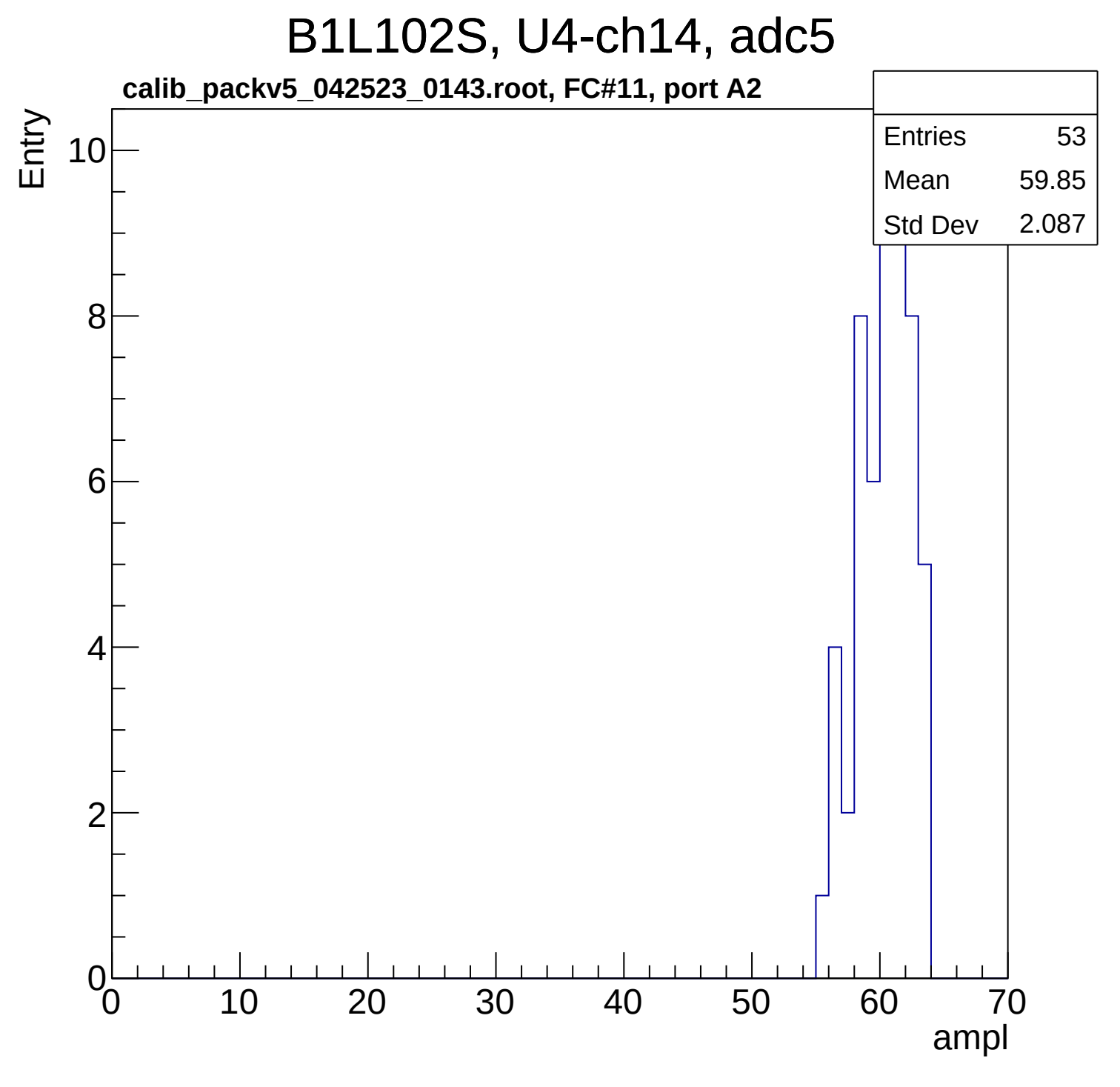
7
8
9
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch14, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 59.85
Std Dev 2.087
Entry
ampl
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4
6
8
10
0
10
20
30
40
50
60
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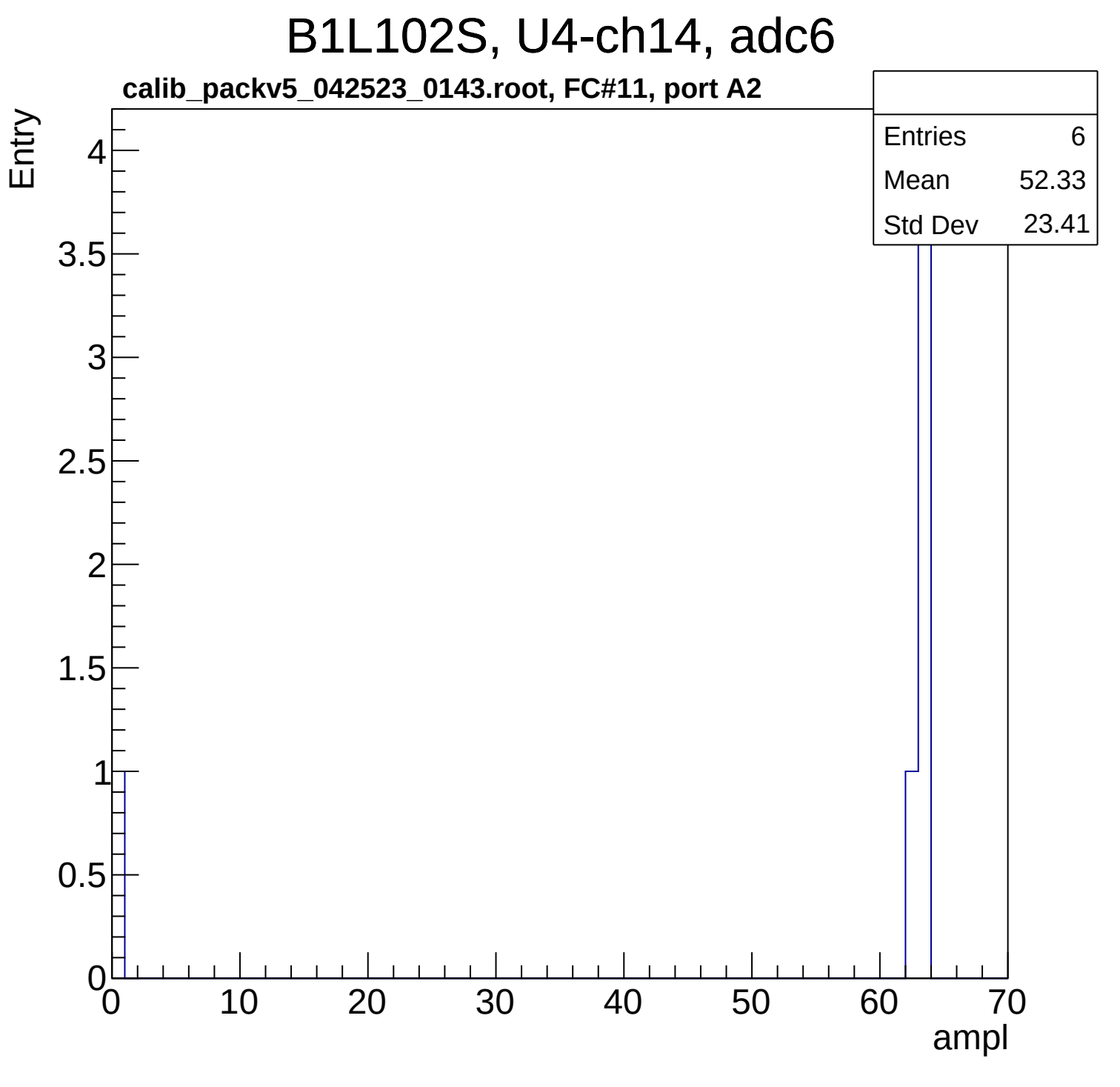
B1L102S, U4-ch14, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 6
Mean 52.33
Std Dev 23.41
Entry
ampl
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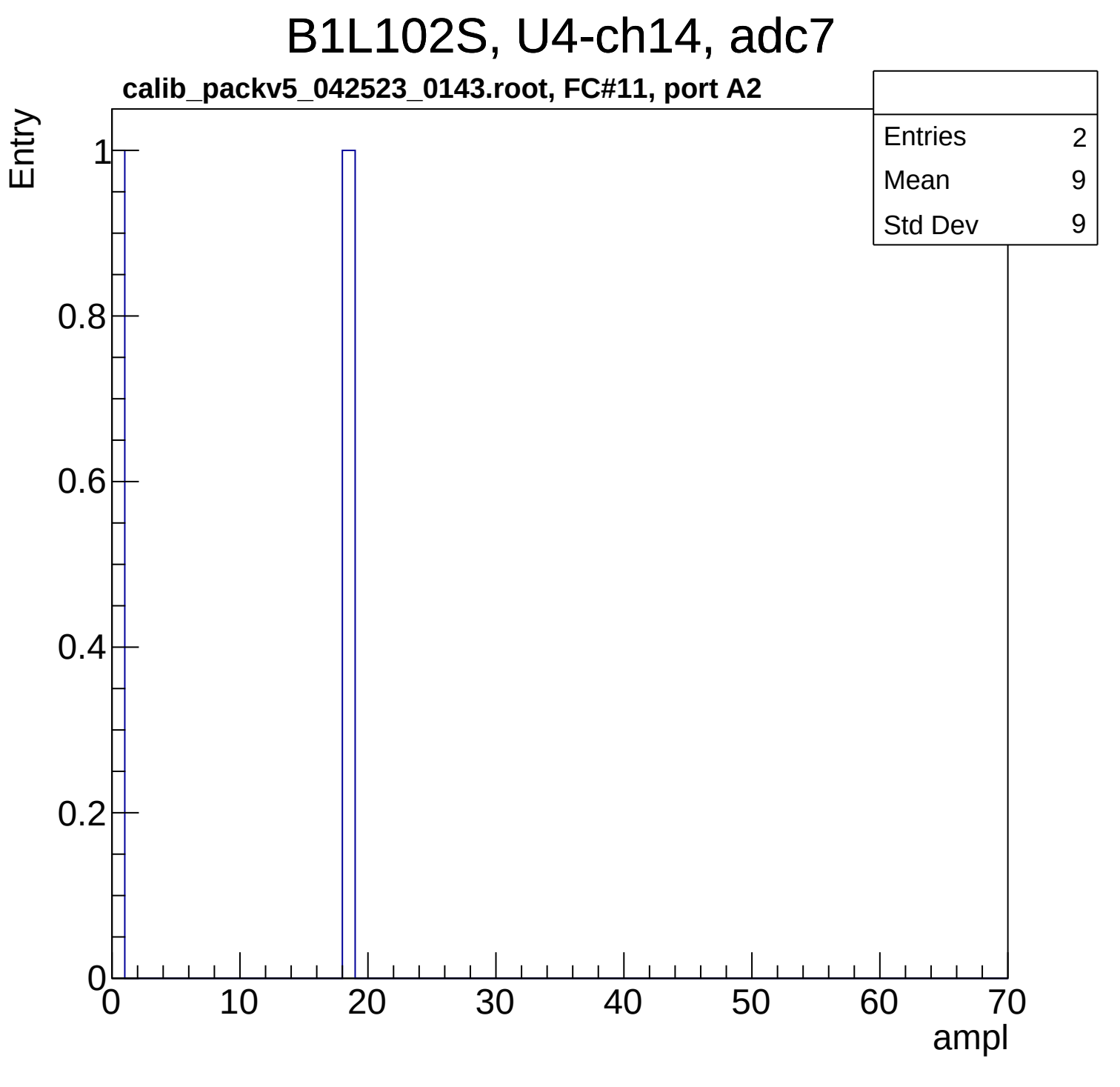
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U4-ch14, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 9
Std Dev 9
Entry
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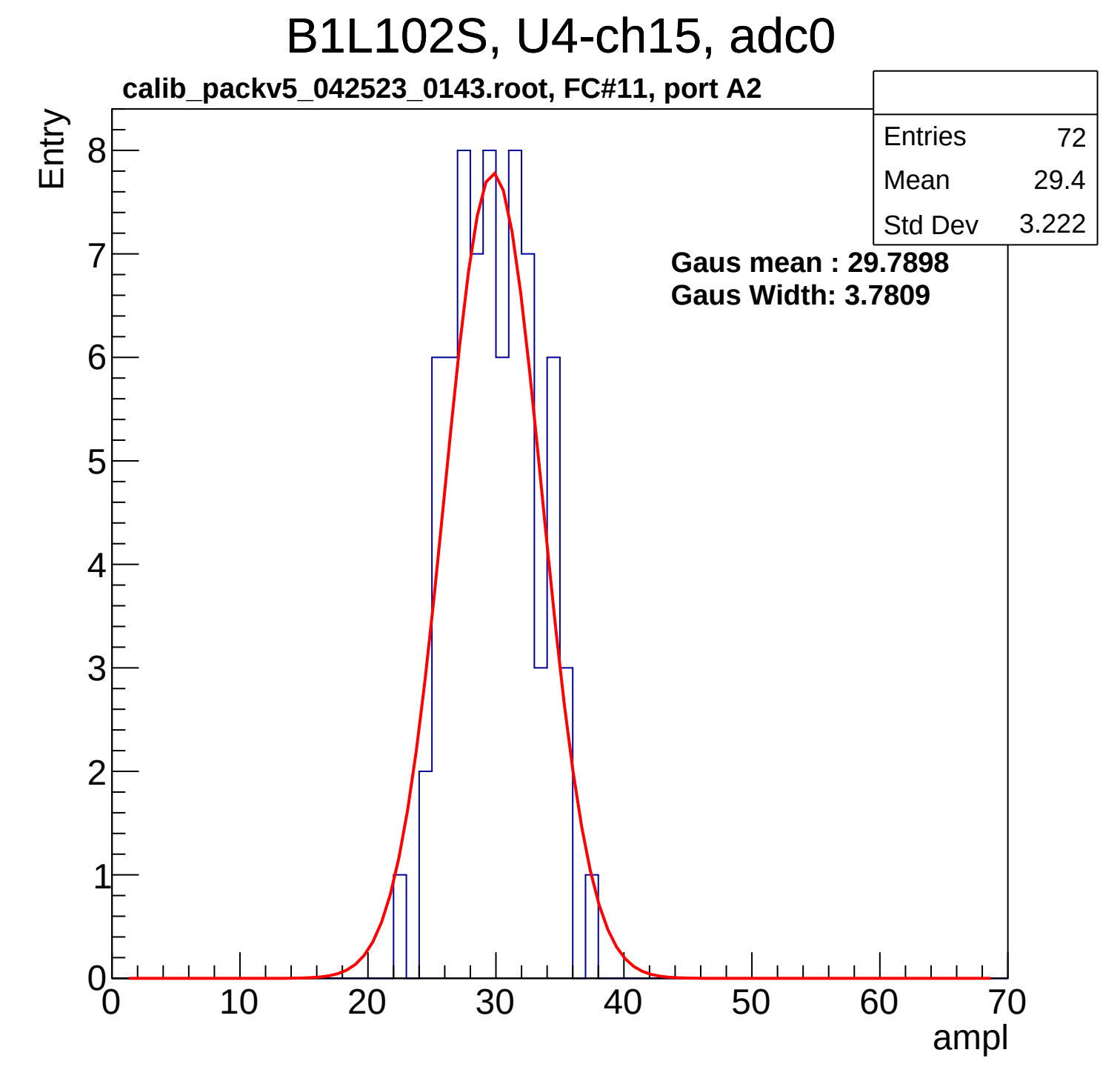
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch15, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 72
Mean 29.4
Std Dev 3.222
Gaus mean : 29.7898
Gaus Width: 3.7809
Entry
ampl
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1
2
3
4
5
6
7
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0
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30
40
50
60
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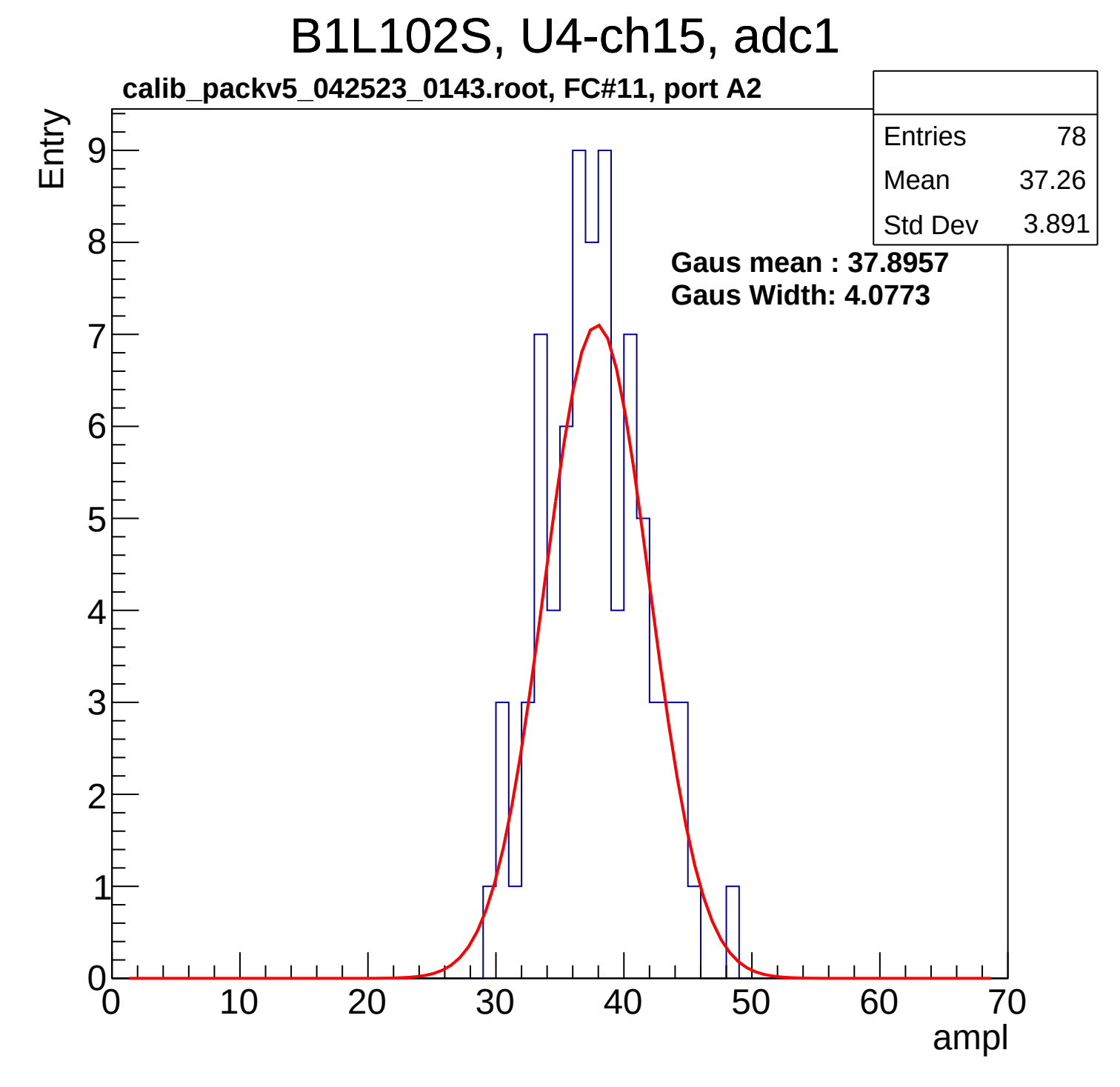
B1L102S, U4-ch15, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 78
Mean 37.26
Std Dev 3.891
Gaus mean : 37.8957
Gaus Width: 4.0773
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
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40
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60
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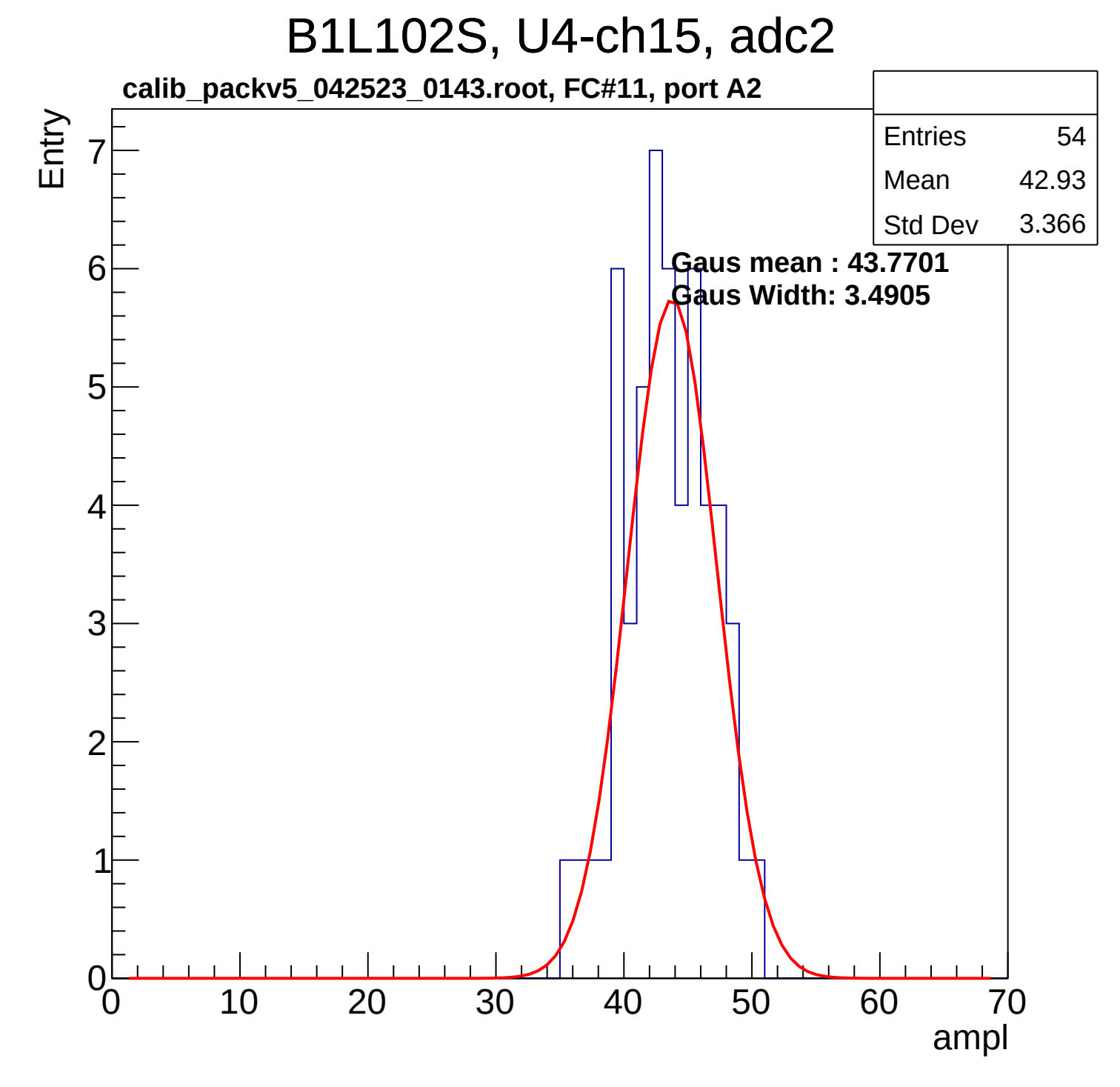
B1L102S, U4-ch15, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 42.93
Std Dev 3.366
Gaus mean : 43.7701
Gaus Width: 3.4905
Entry
ampl
0
1
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3
4
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0
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60
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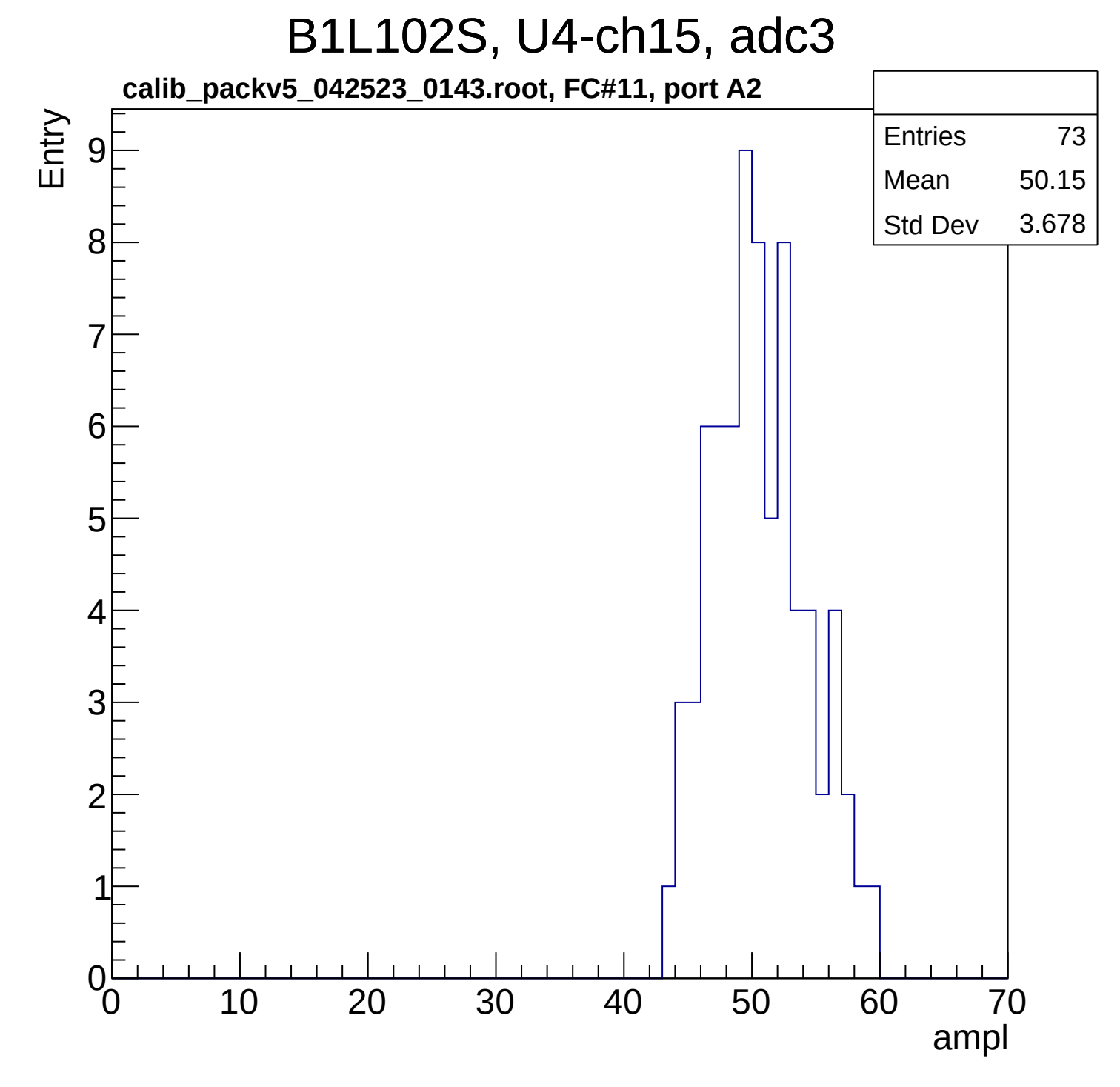
B1L102S, U4-ch15, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 50.15
Std Dev 3.678
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
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60
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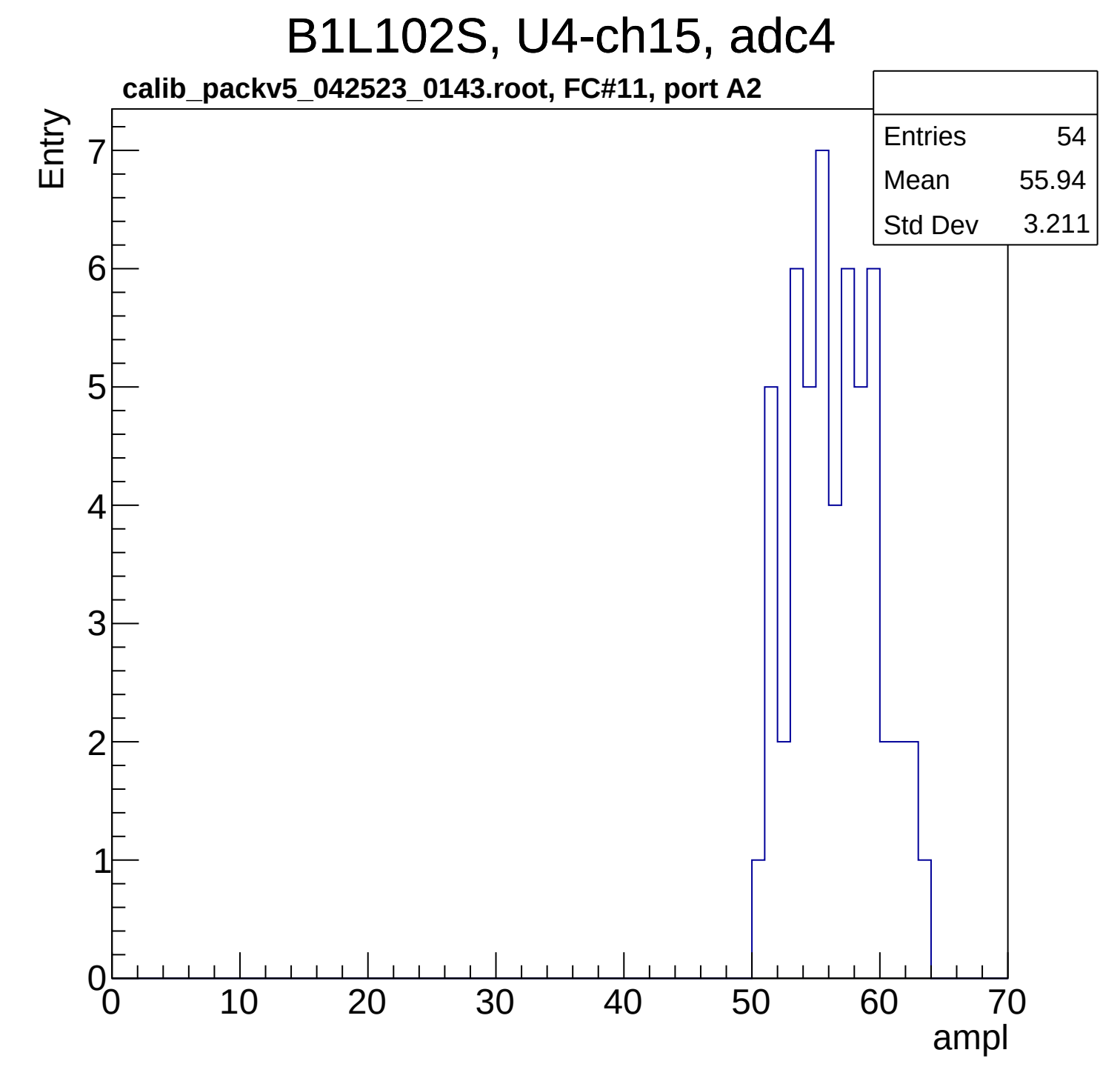
B1L102S, U4-ch15, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 55.94
Std Dev 3.211
Entry
ampl
0
1
2
3
4
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0
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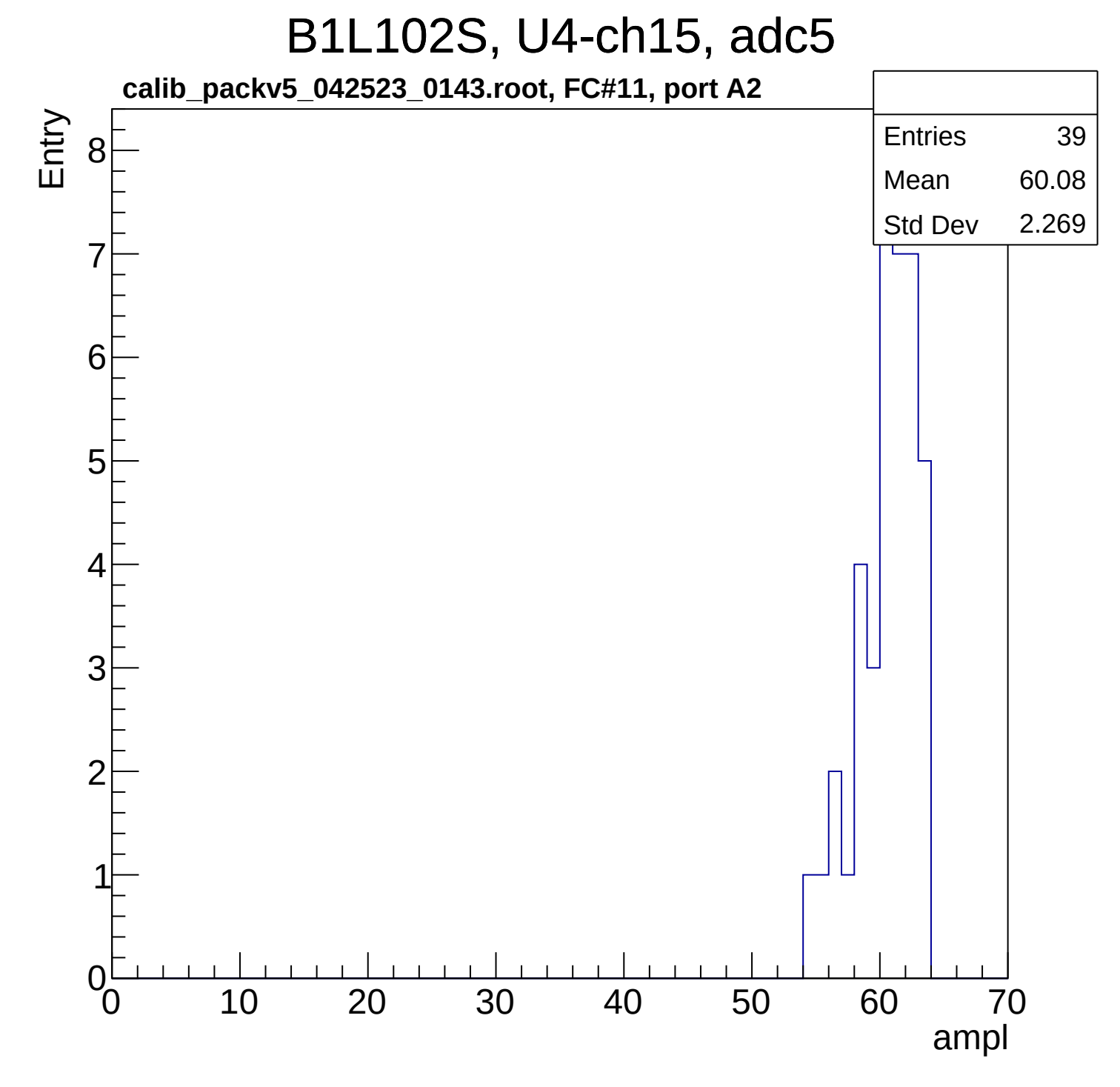
B1L102S, U4-ch15, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 39
Mean 60.08
Std Dev 2.269
Entry
ampl
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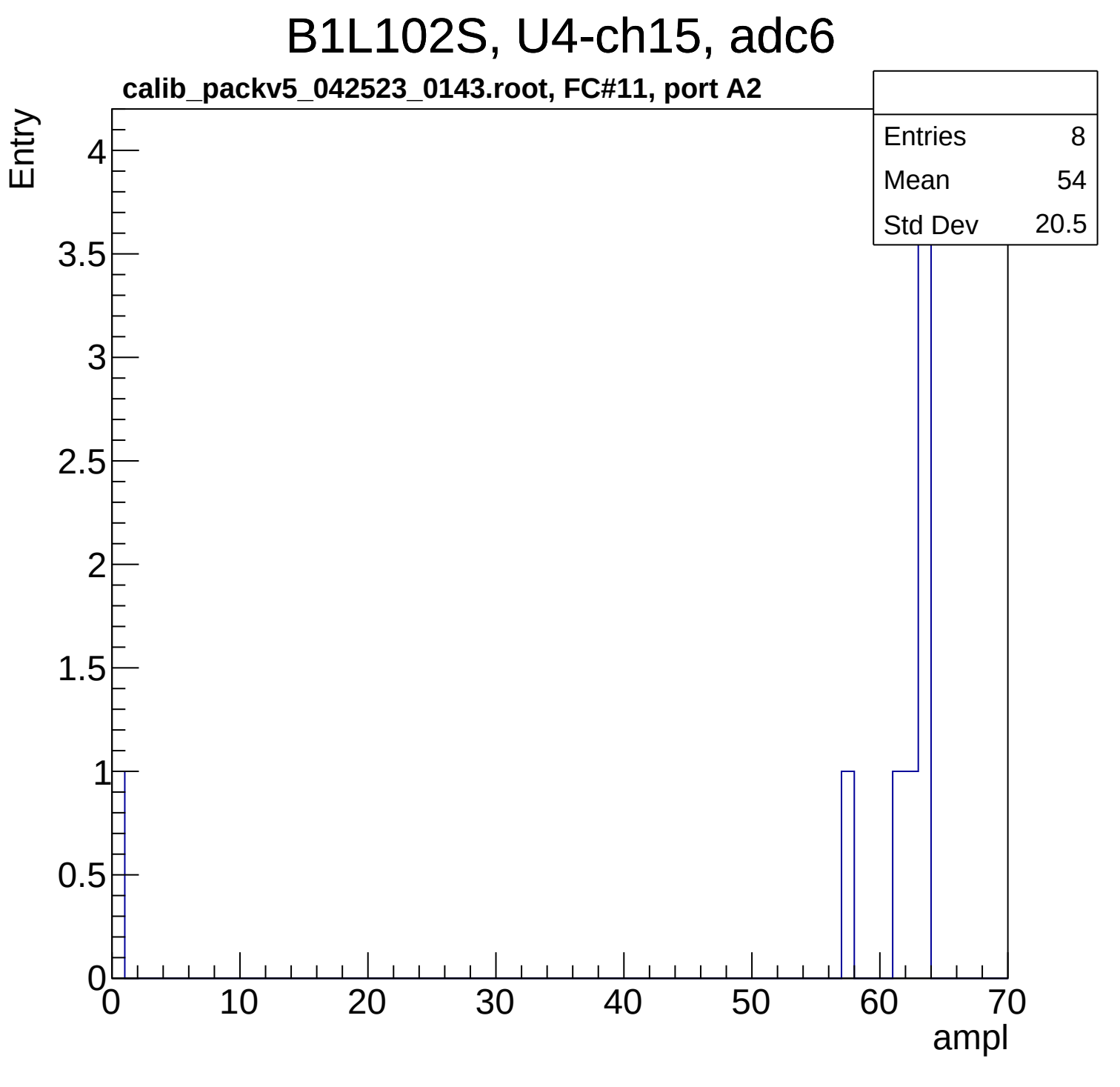
B1L102S, U4-ch15, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 8
Mean 54
Std Dev 20.5
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
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20
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40
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60
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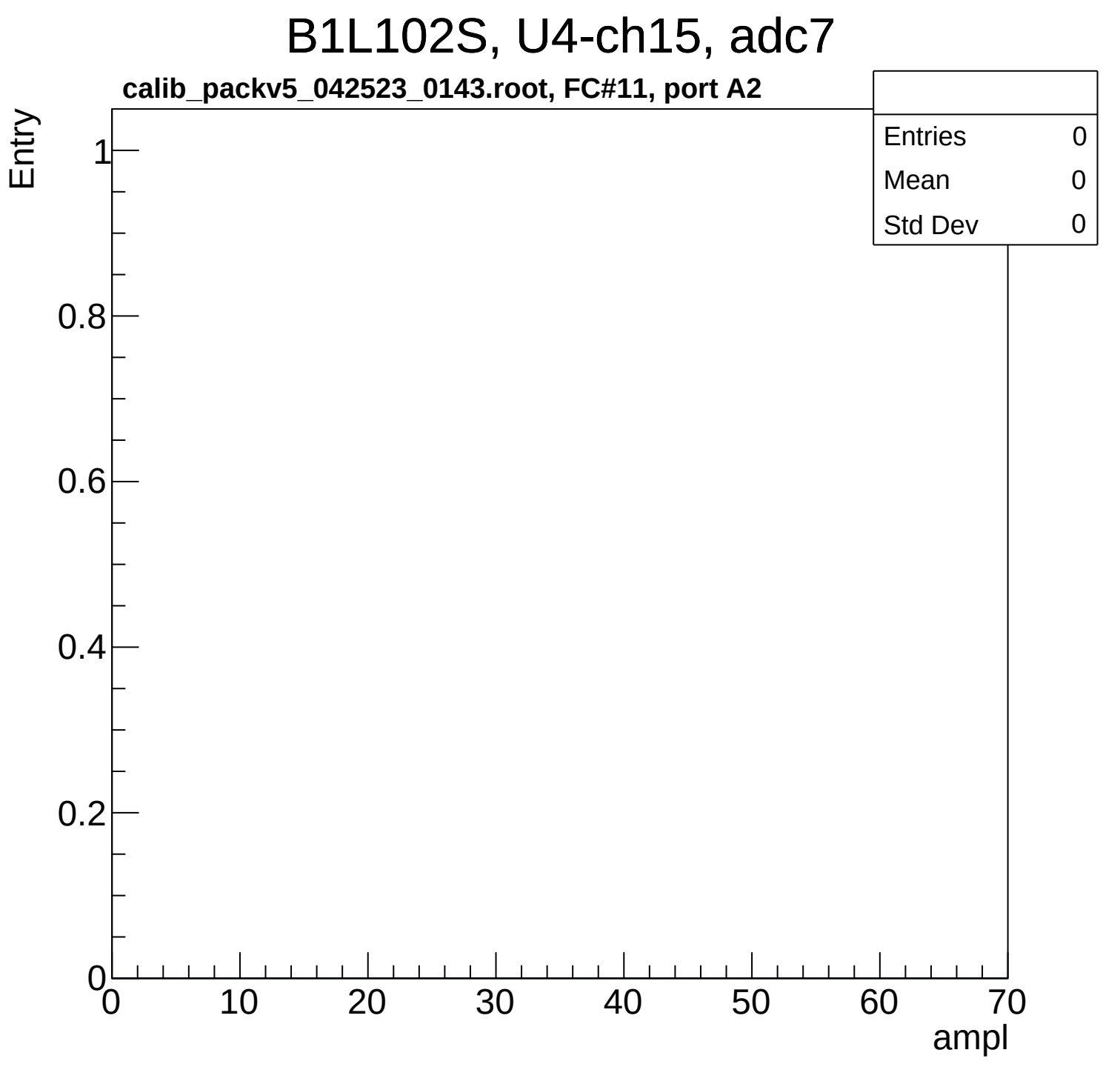
B1L102S, U4-ch15, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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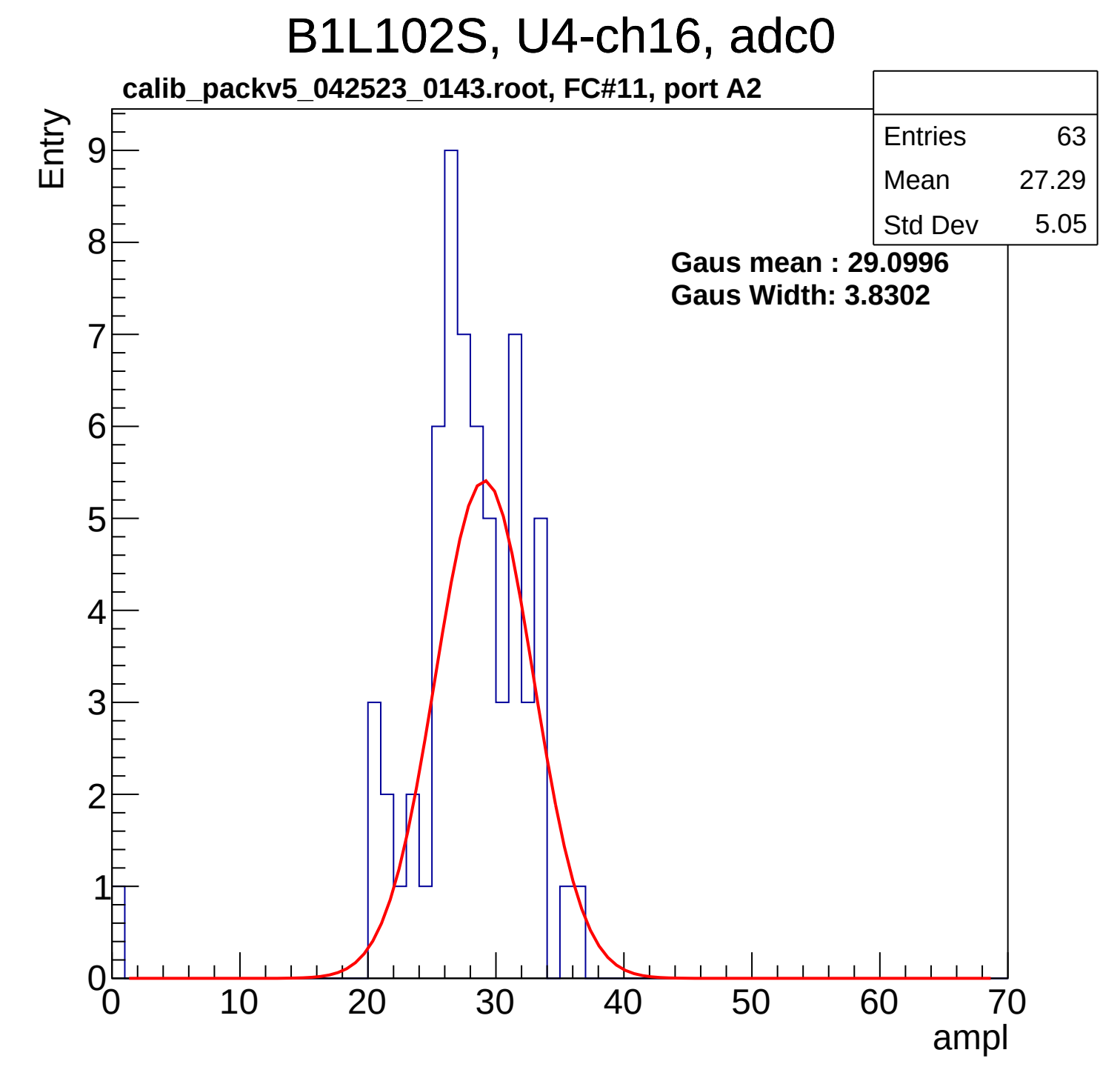
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch16, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 27.29
Std Dev 5.05
Gaus mean : 29.0996
Gaus Width: 3.8302
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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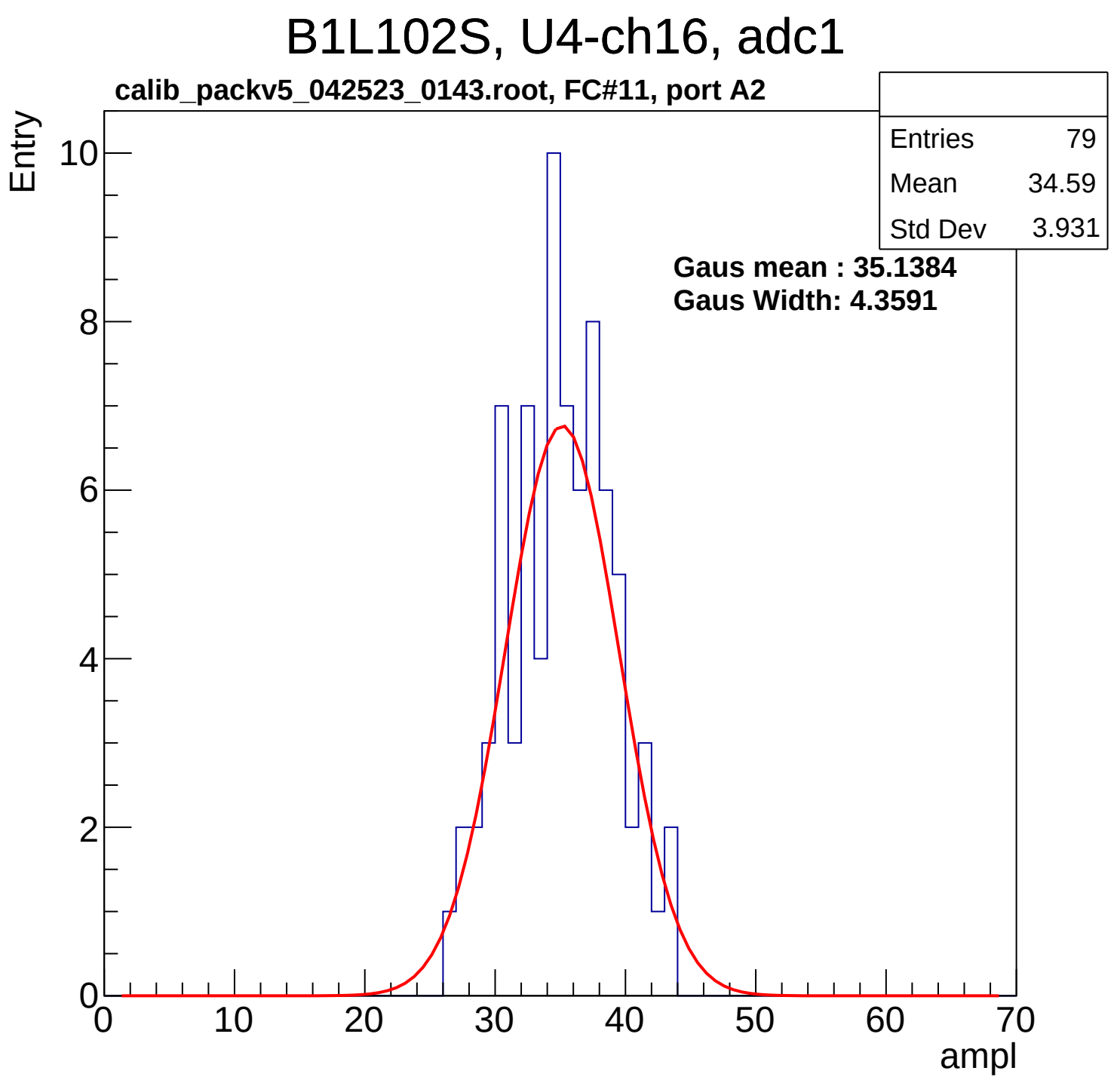
B1L102S, U4-ch16, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 79
Mean 34.59
Std Dev 3.931
Gaus mean : 35.1384
Gaus Width: 4.3591
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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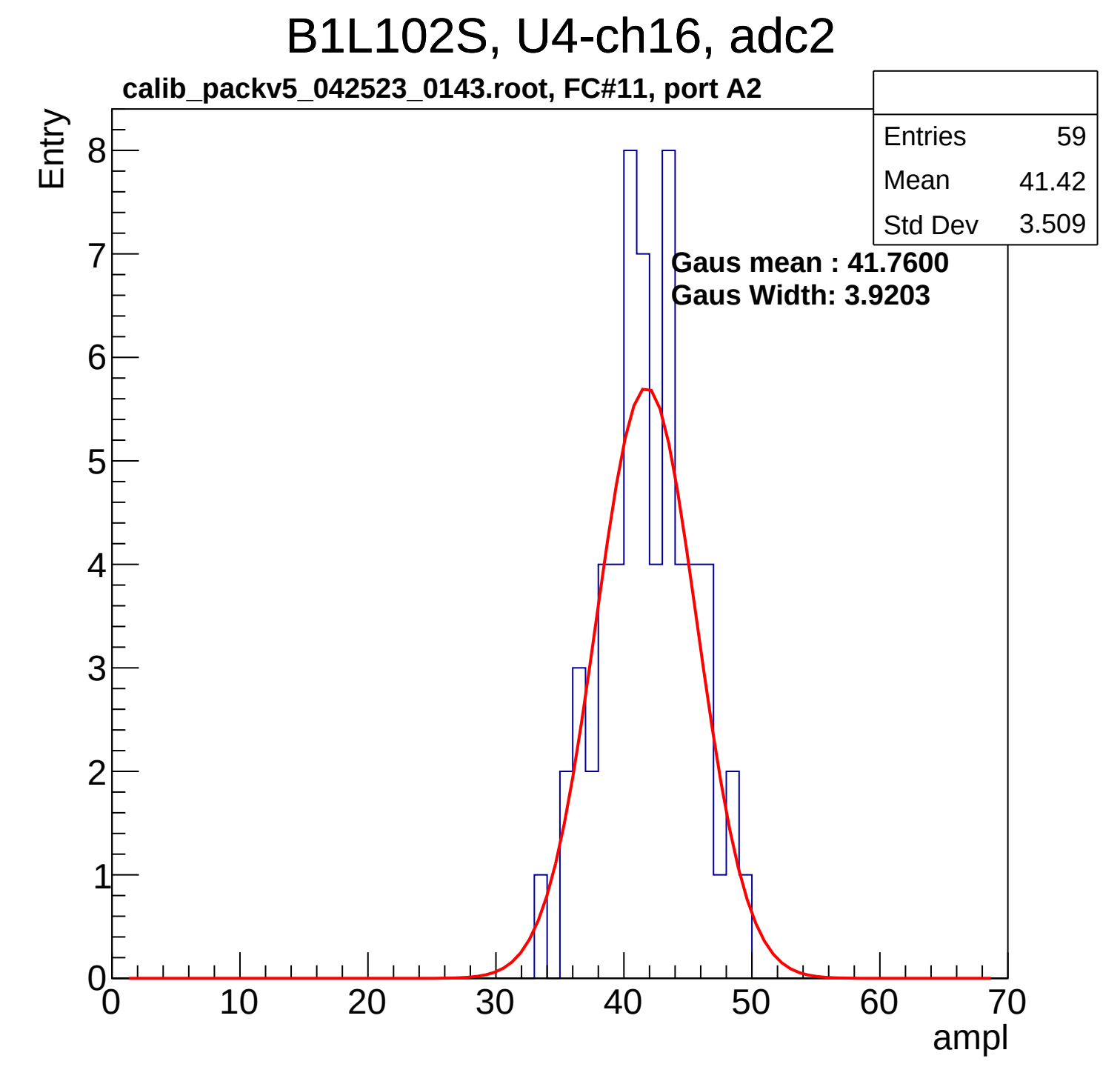
B1L102S, U4-ch16, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 41.42
Std Dev 3.509
Gaus mean : 41.7600
Gaus Width: 3.9203
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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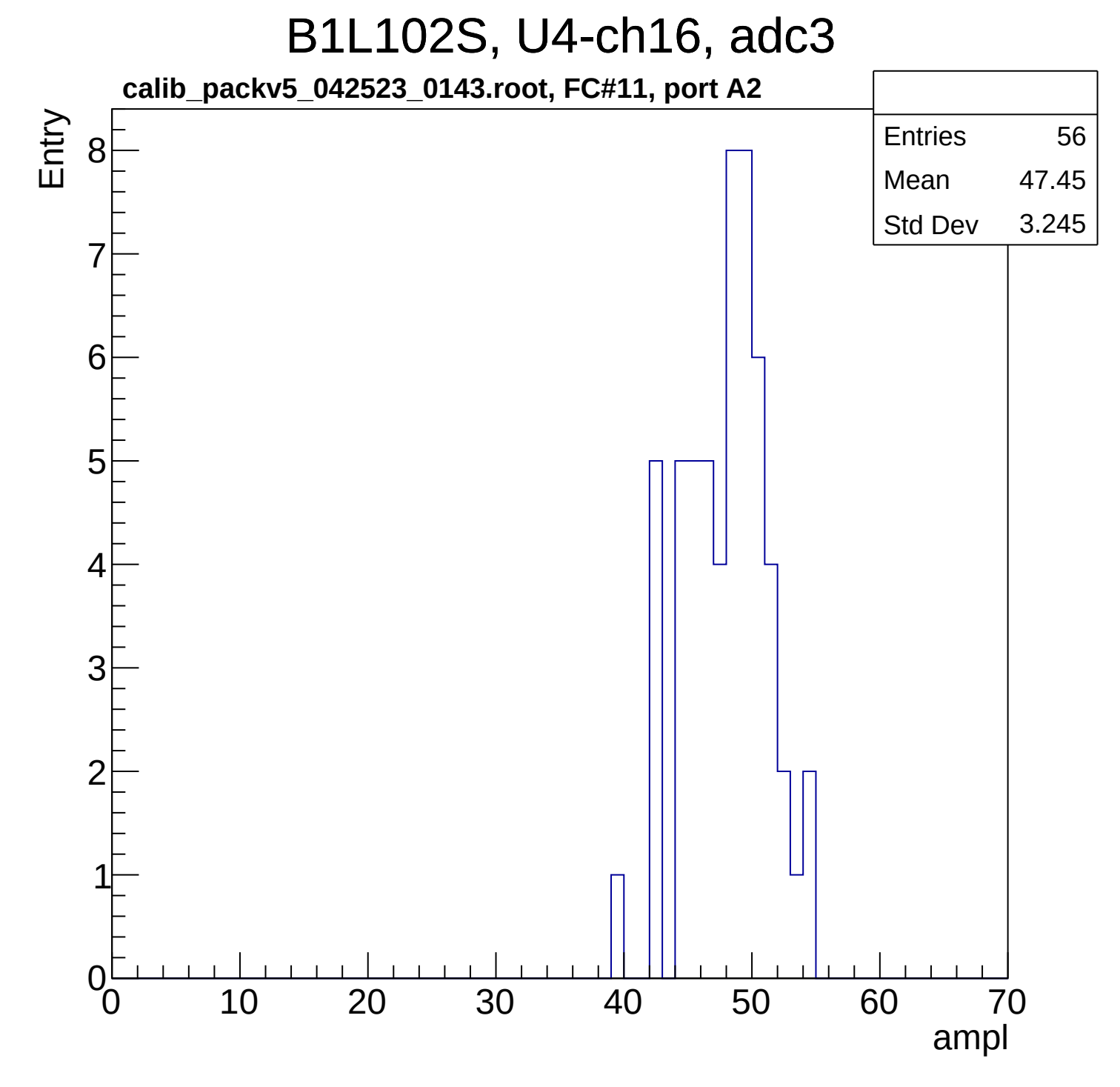
B1L102S, U4-ch16, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 47.45
Std Dev 3.245
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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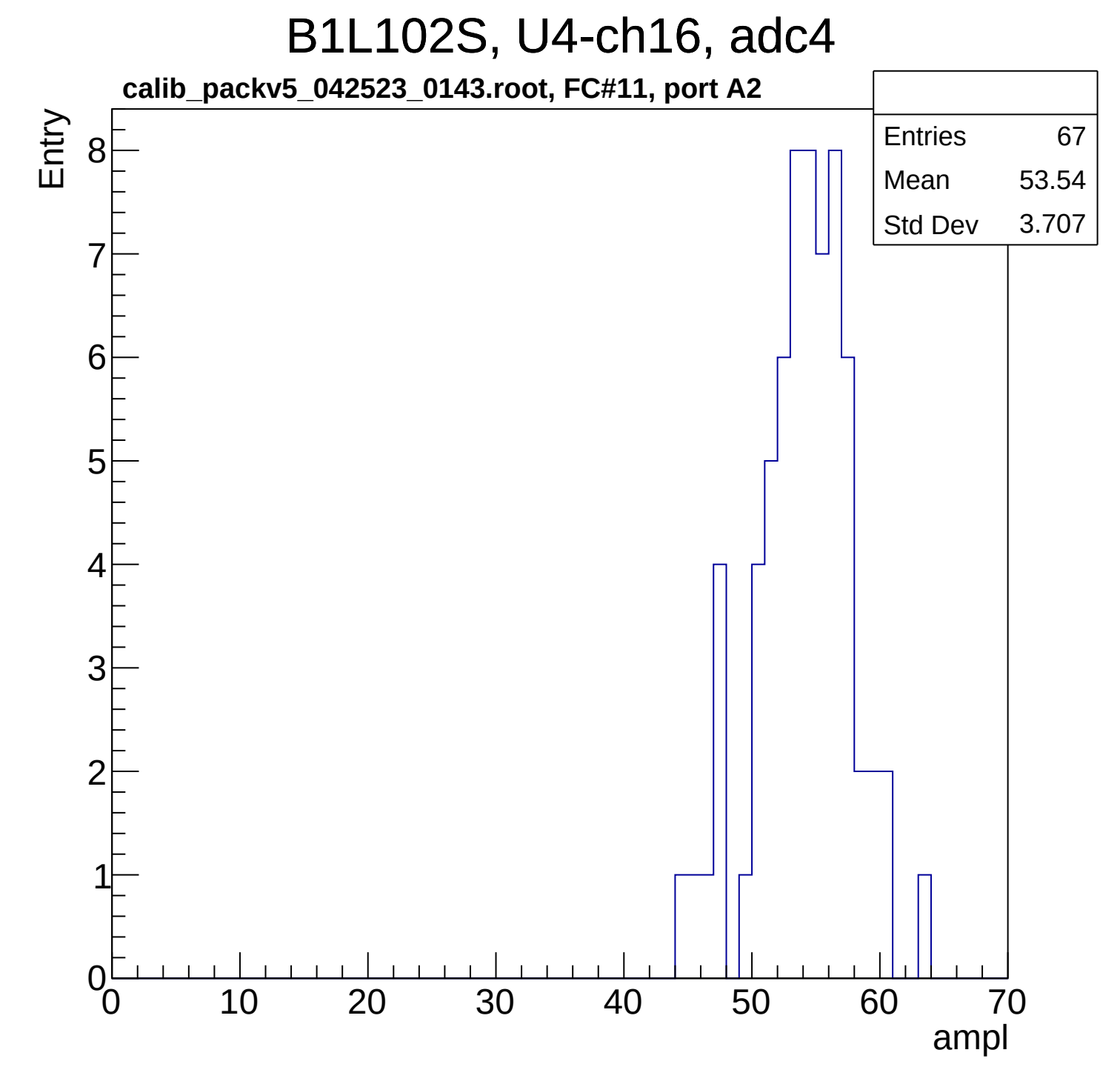
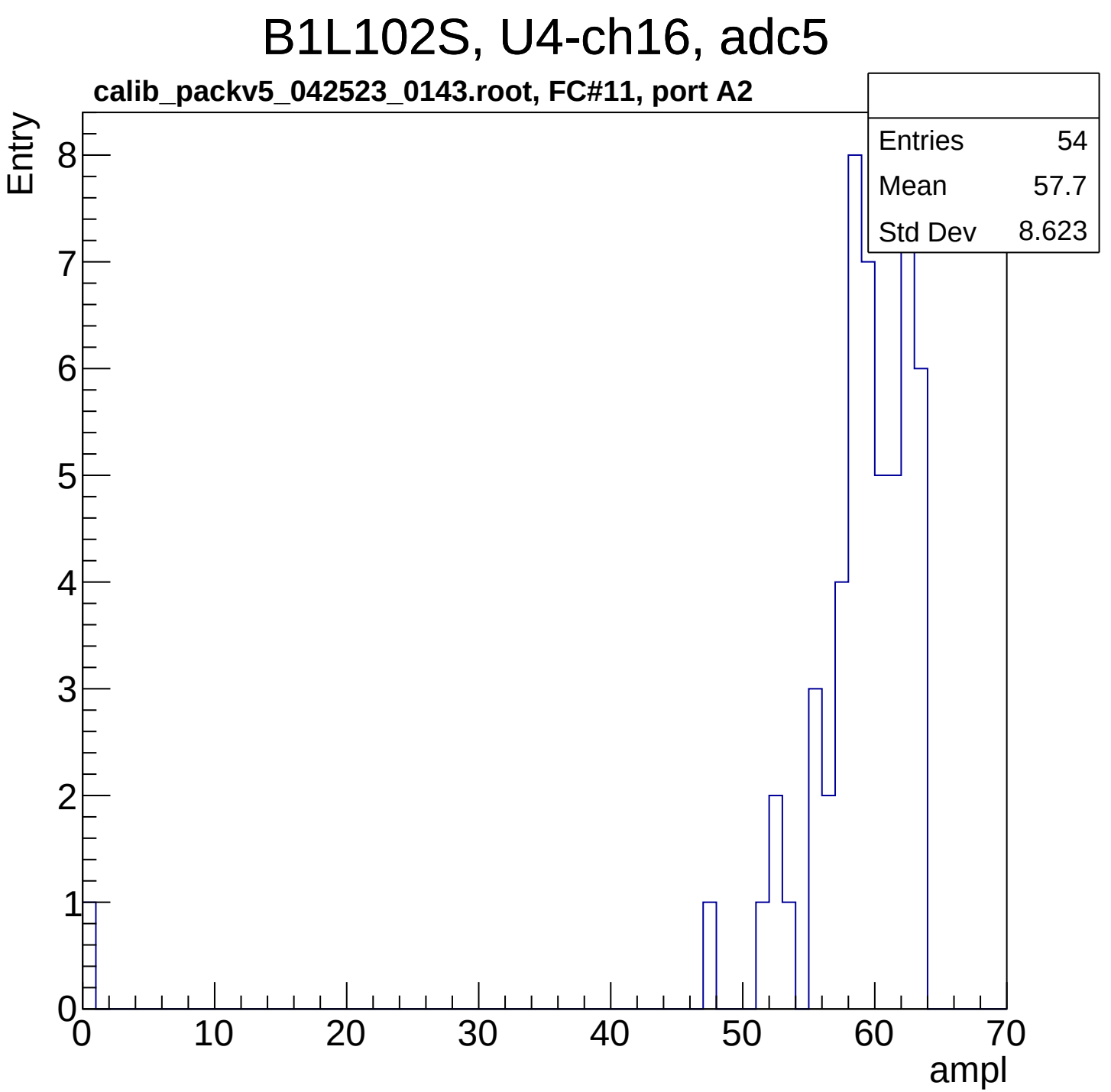

B1L102S, U4-ch16, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 53.54
Std Dev 3.707
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch16, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 57.7
Std Dev 8.623
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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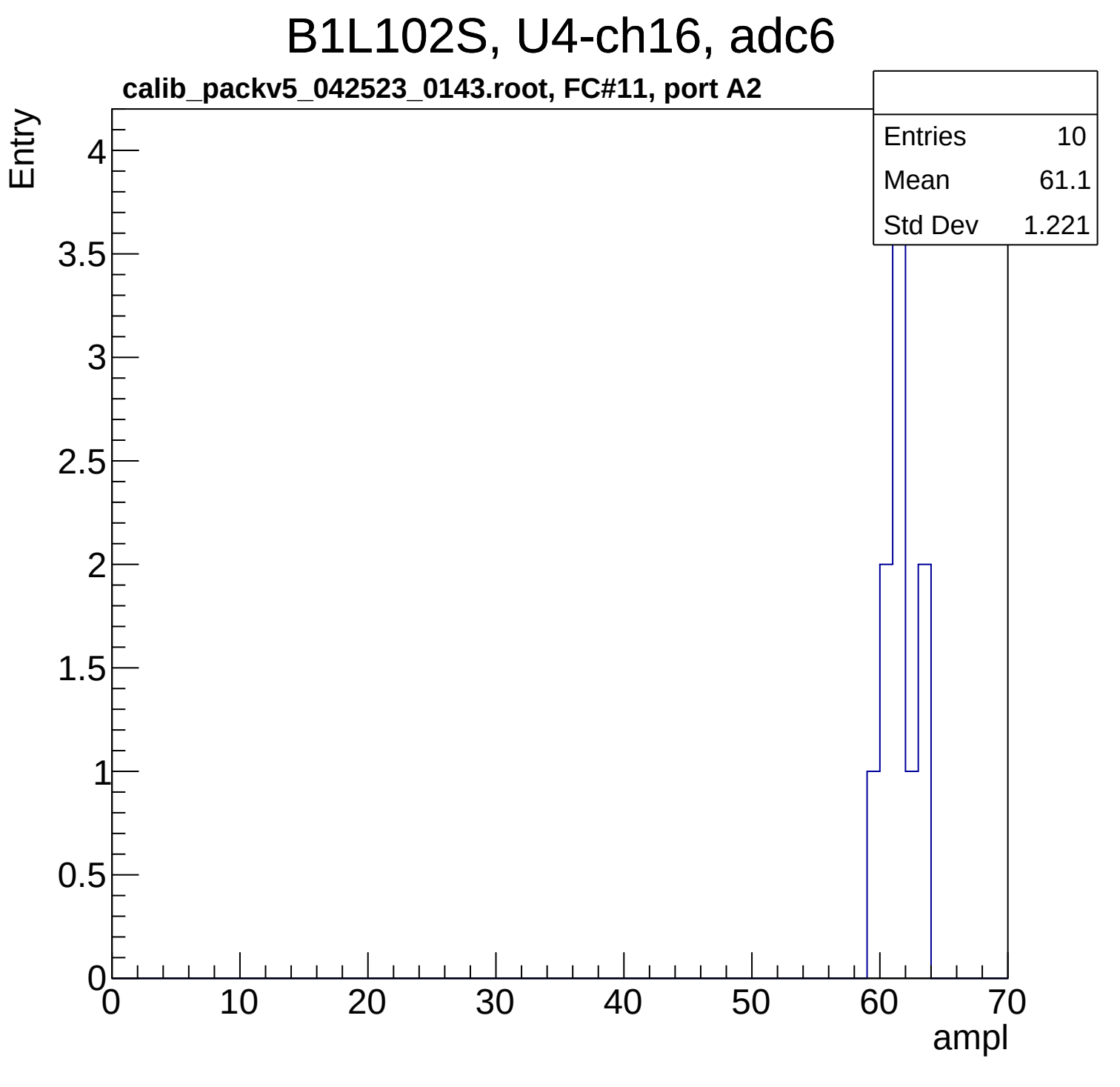
B1L102S, U4-ch16, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 10
Mean 61.1
Std Dev 1.221
Entry
ampl
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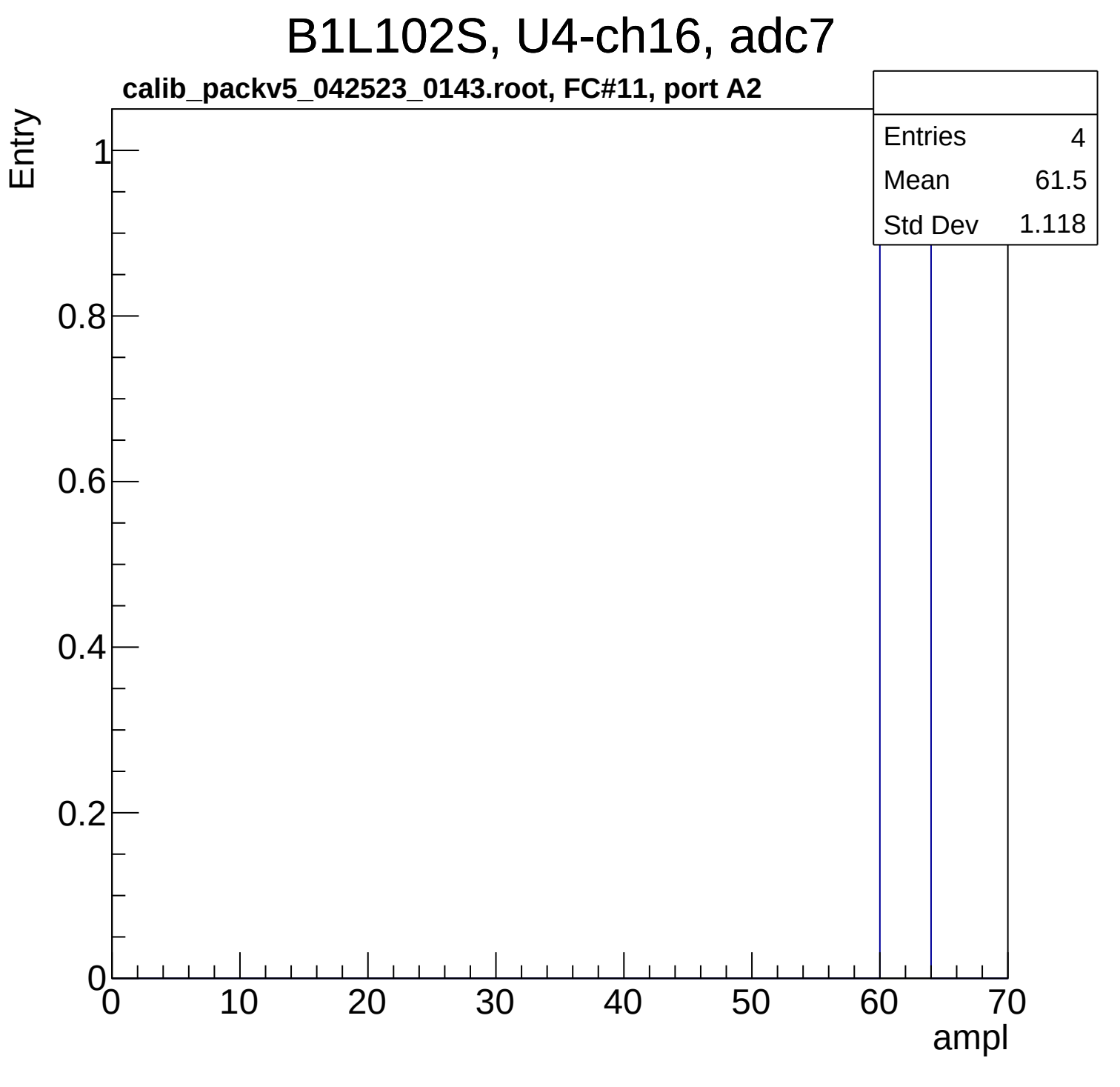
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U4-ch16, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 4
Mean 61.5
Std Dev 1.118
Entry
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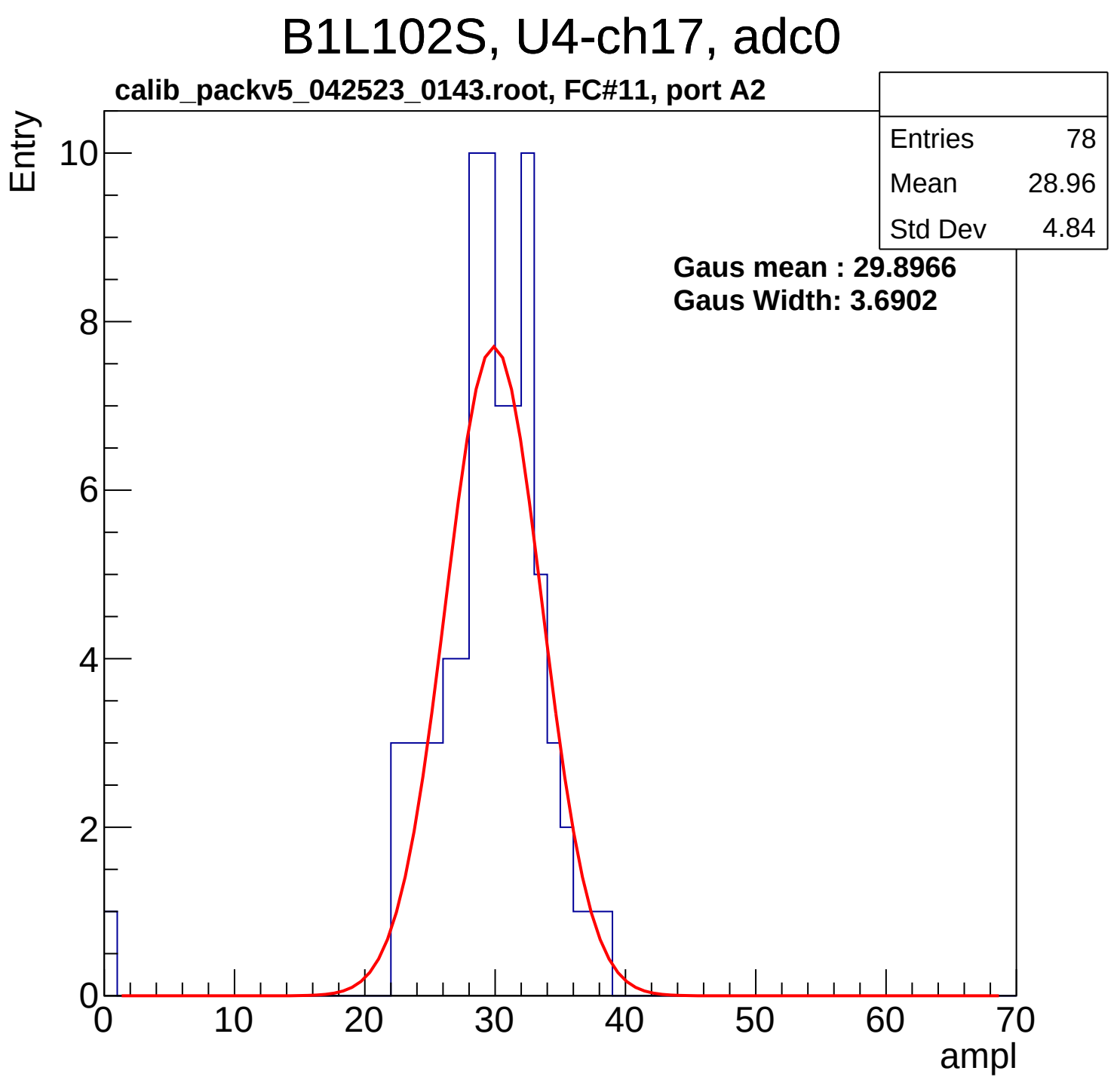
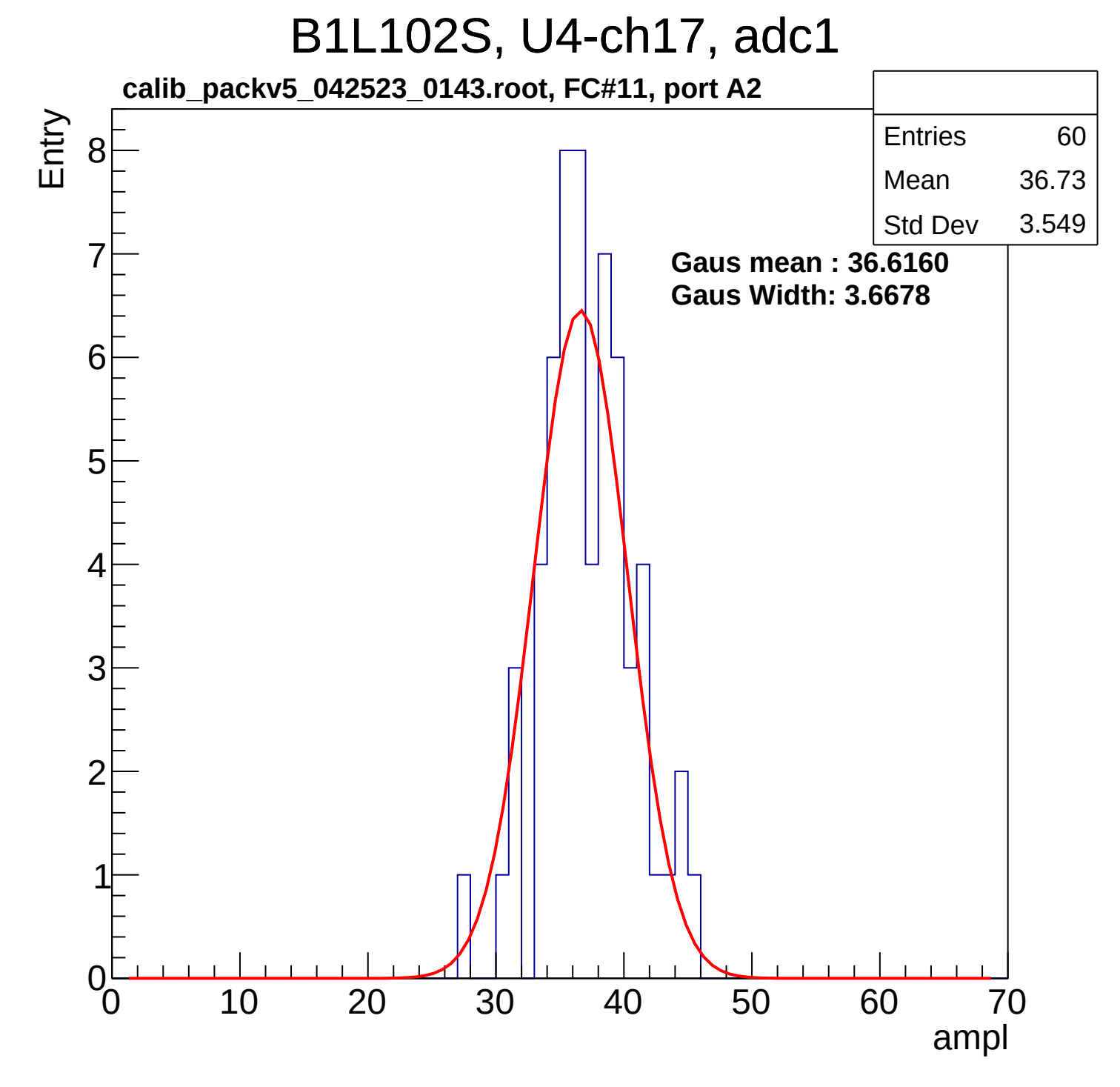
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch17, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 78
Mean 28.96
Std Dev 4.84
Gaus mean : 29.8966
Gaus Width: 3.6902
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch17, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 36.73
Std Dev 3.549
Gaus mean : 36.6160
Gaus Width: 3.6678
Entry
ampl
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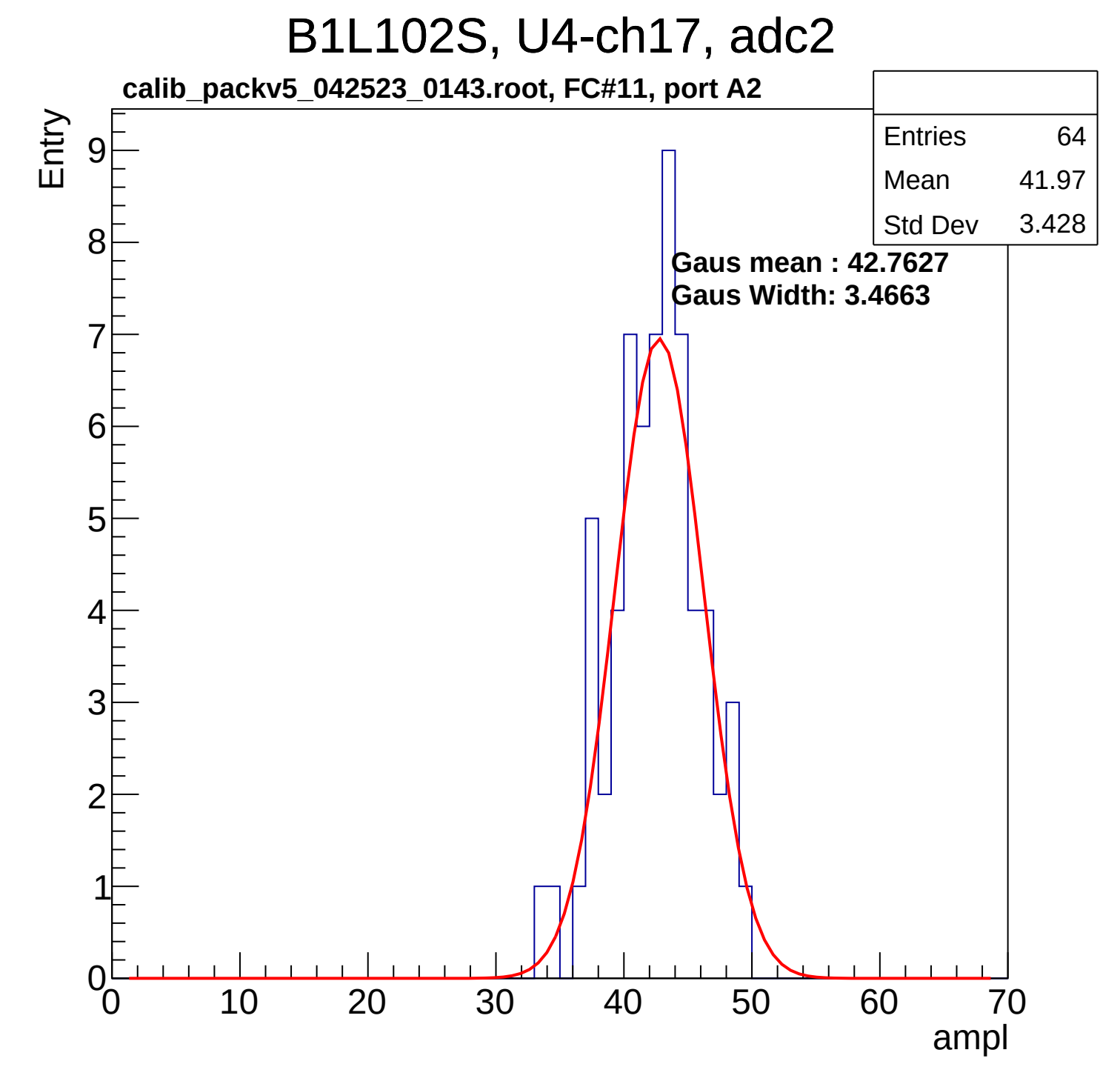
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch17, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 41.97
Std Dev 3.428
Gaus mean : 42.7627
Gaus Width: 3.4663
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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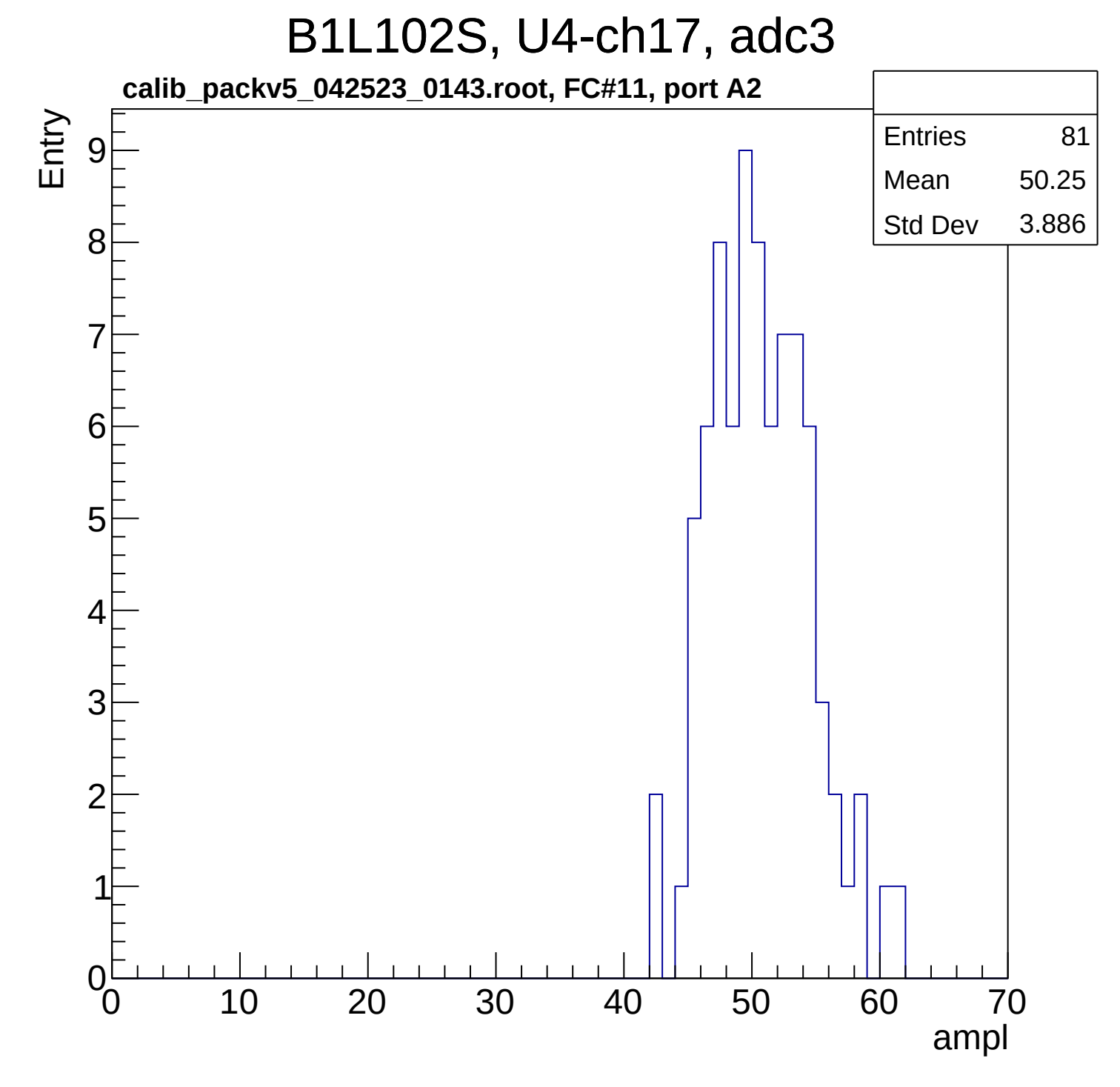
B1L102S, U4-ch17, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 81
Mean 50.25
Std Dev 3.886
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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60
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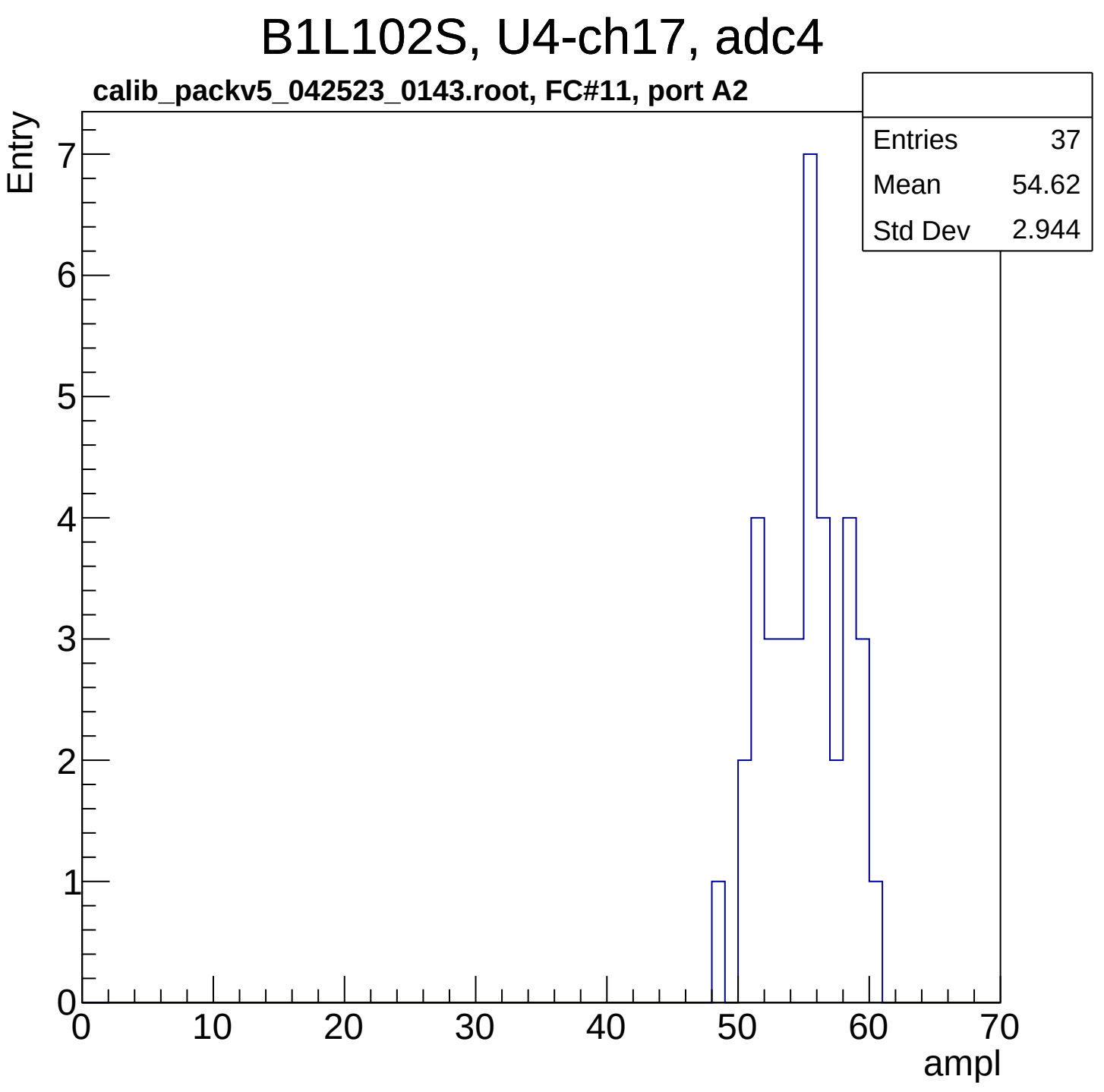
B1L102S, U4-ch17, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 37
Mean 54.62
Std Dev 2.944
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
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60
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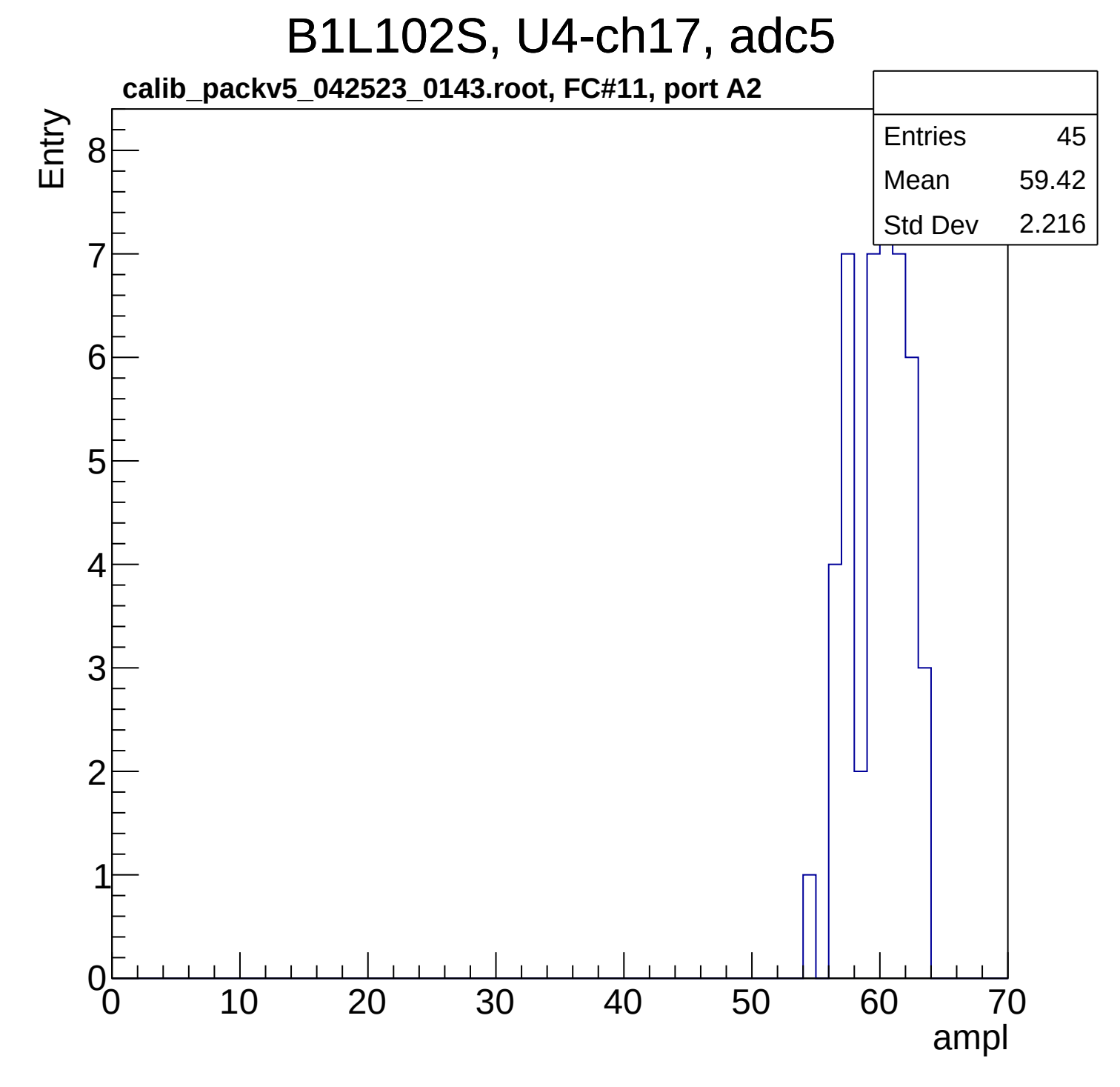
B1L102S, U4-ch17, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 45
Mean 59.42
Std Dev 2.216
Entry
ampl
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4
5
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7
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0
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60
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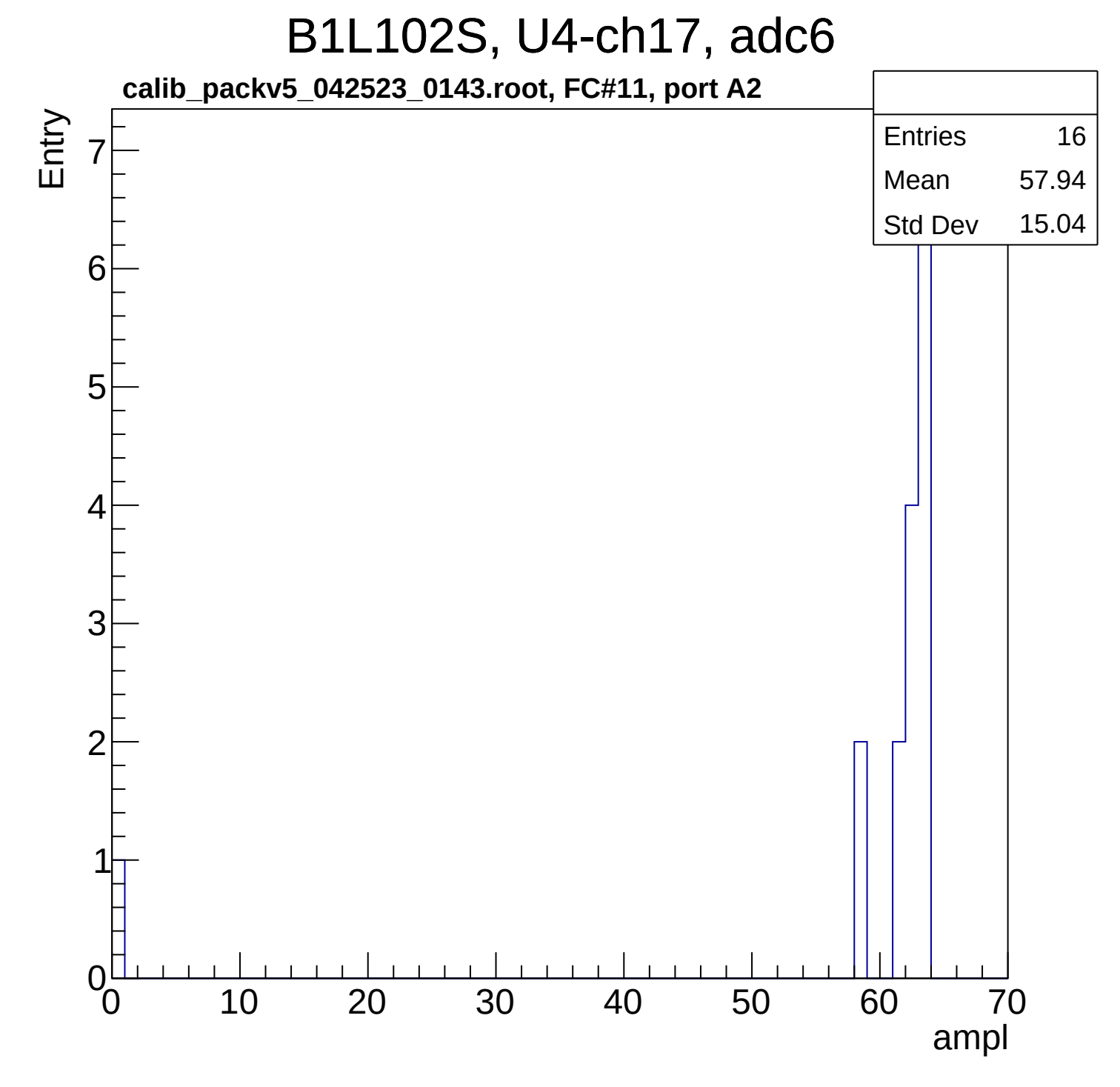
B1L102S, U4-ch17, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 16
Mean 57.94
Std Dev 15.04
Entry
ampl
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1
2
3
4
5
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0
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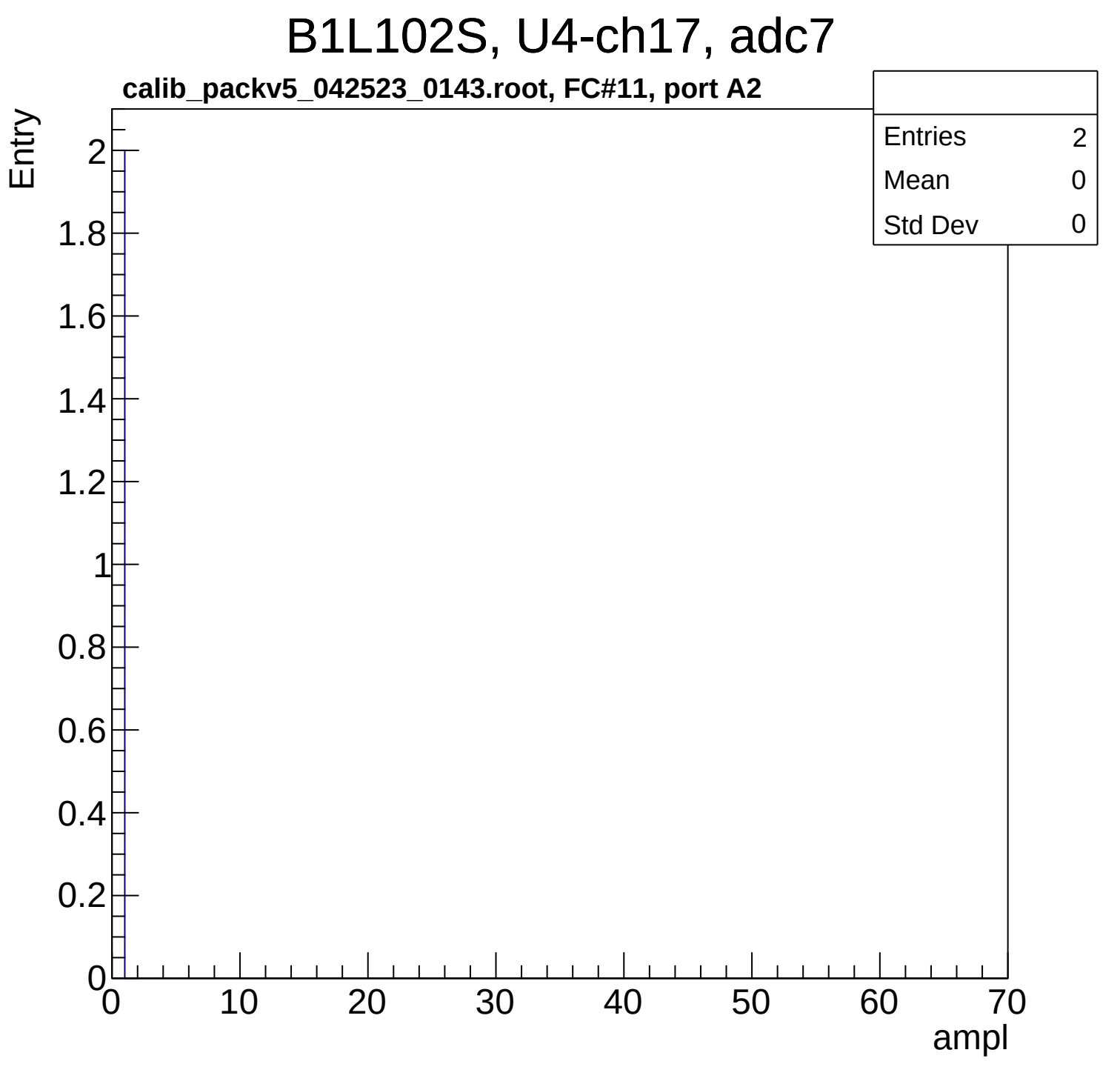
B1L102S, U4-ch17, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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60
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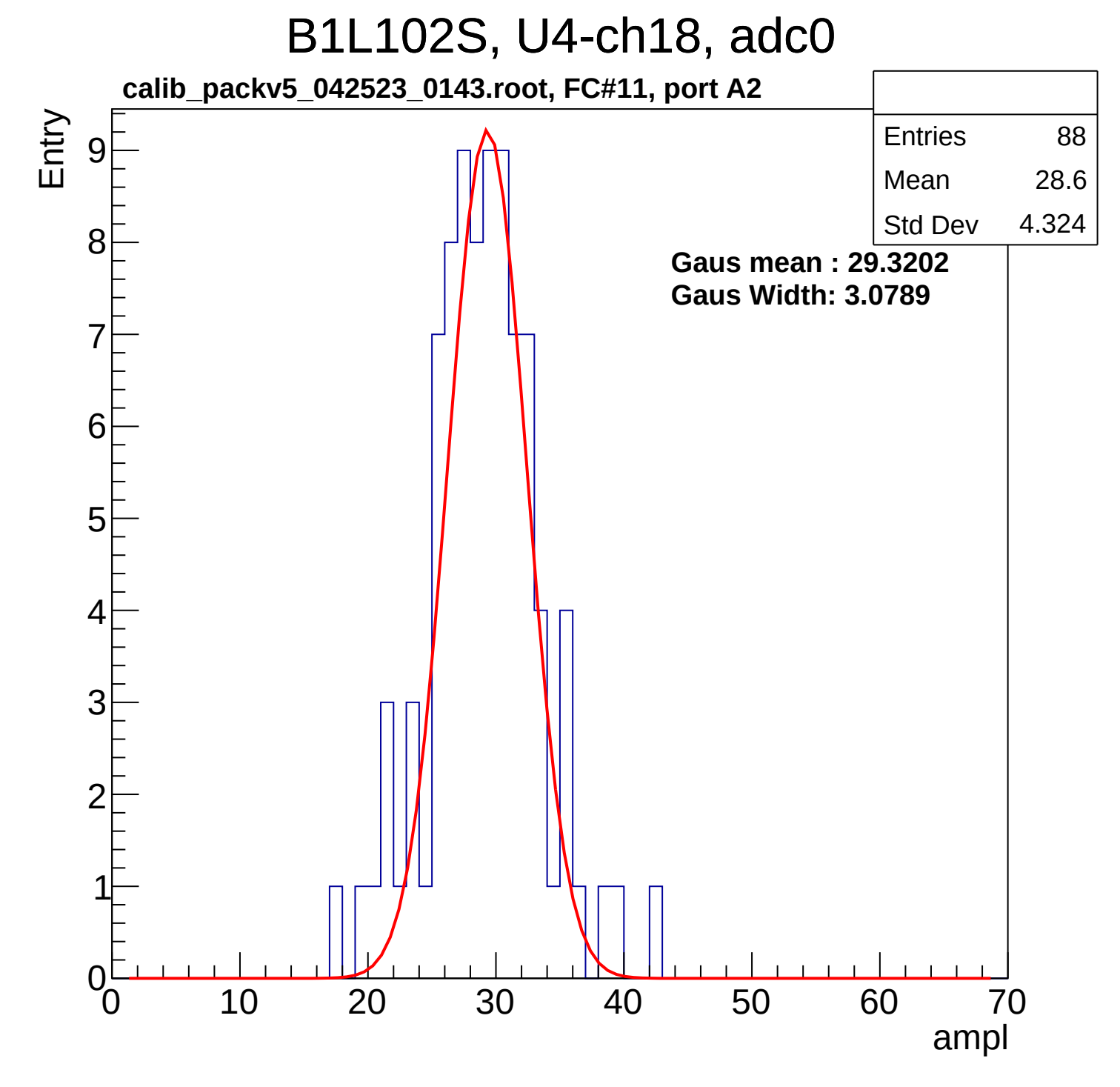
B1L102S, U4-ch18, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 88
Mean 28.6
Std Dev 4.324
Gaus mean : 29.3202
Gaus Width: 3.0789
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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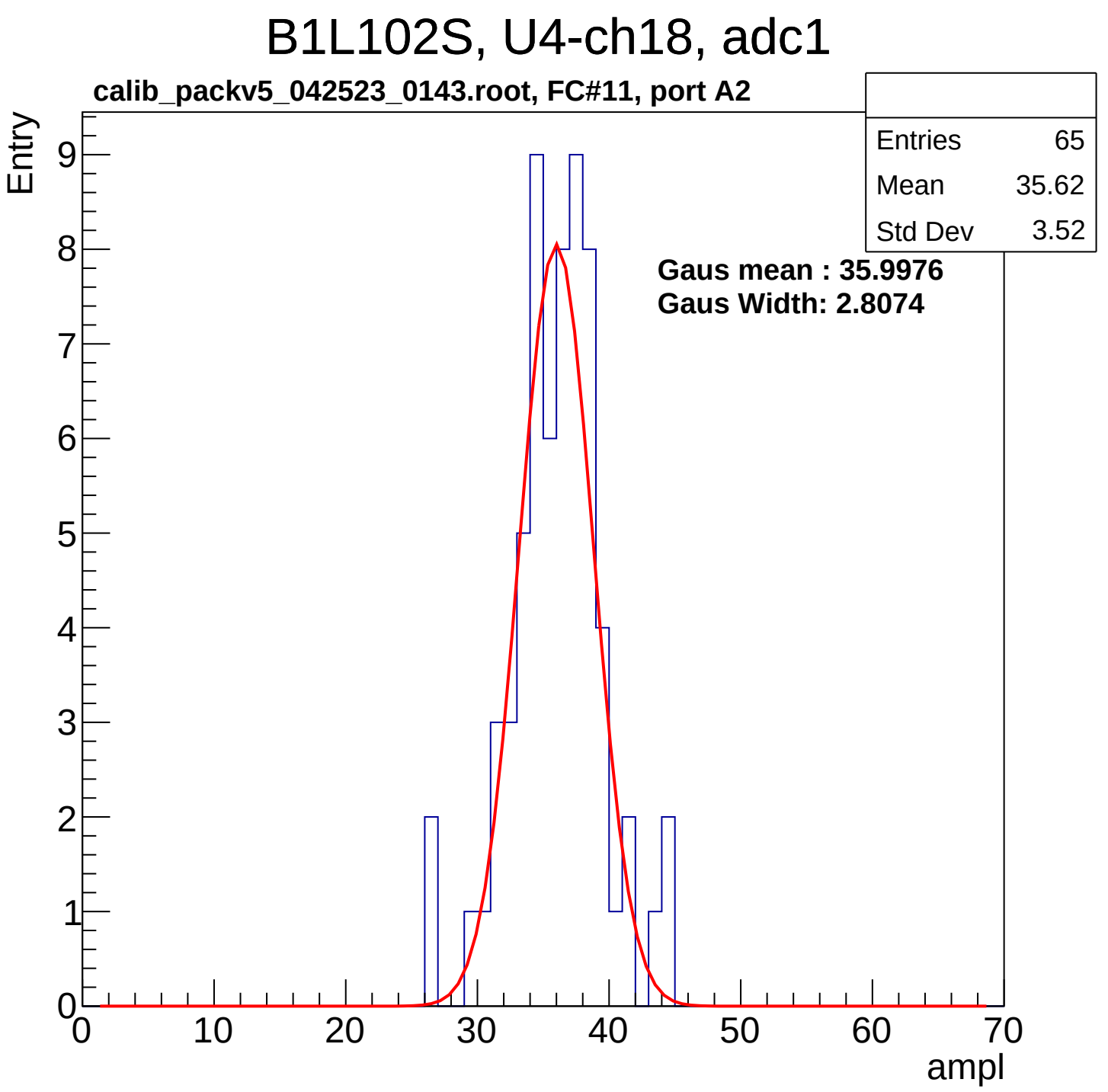
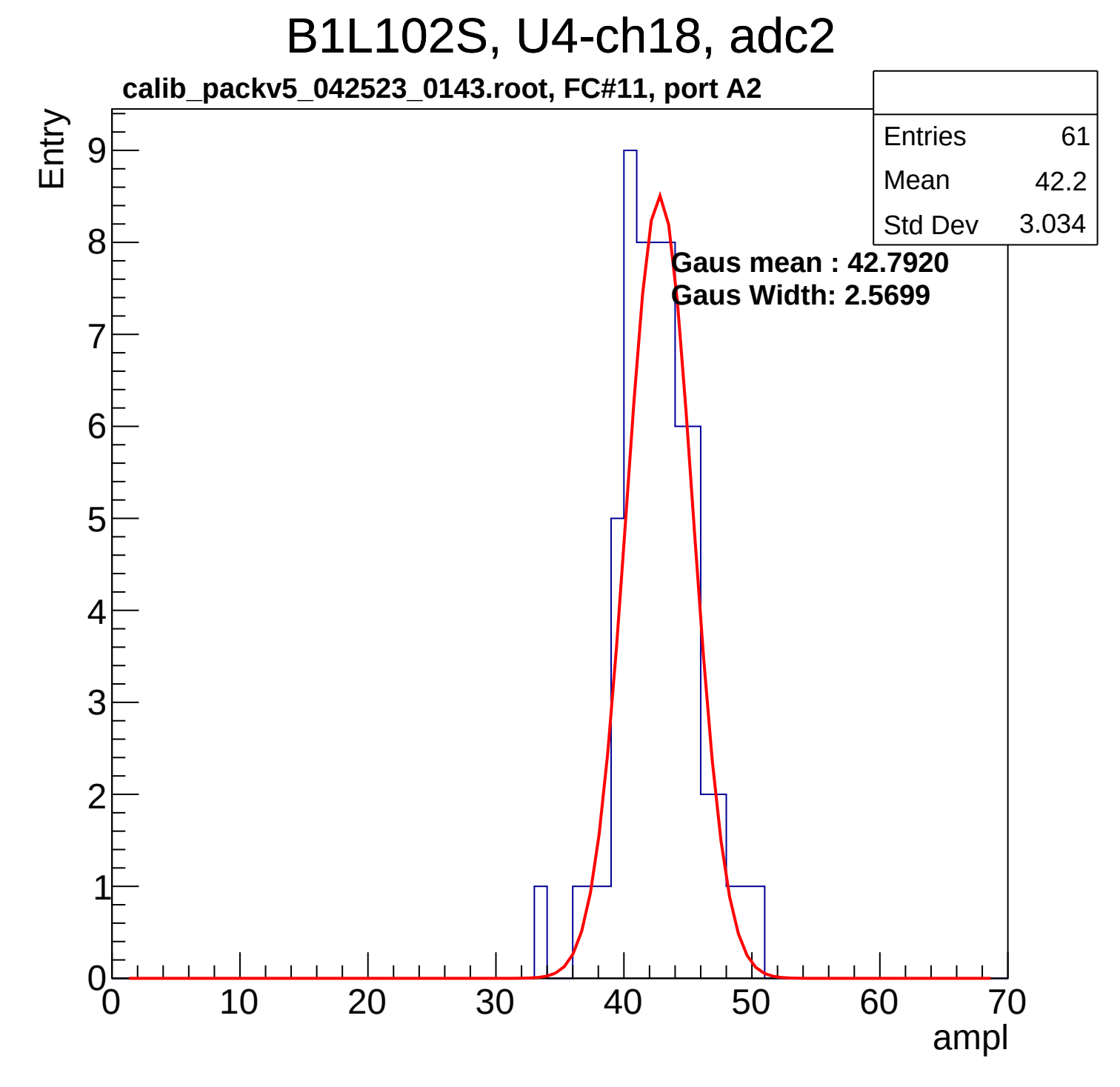

B1L102S, U4-ch18, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 35.62
Std Dev 3.52
Gaus mean : 35.9976
Gaus Width: 2.8074
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch18, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 42.2
Std Dev 3.034
Gaus mean : 42.7920
Gaus Width: 2.5699
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
30
40
50
60
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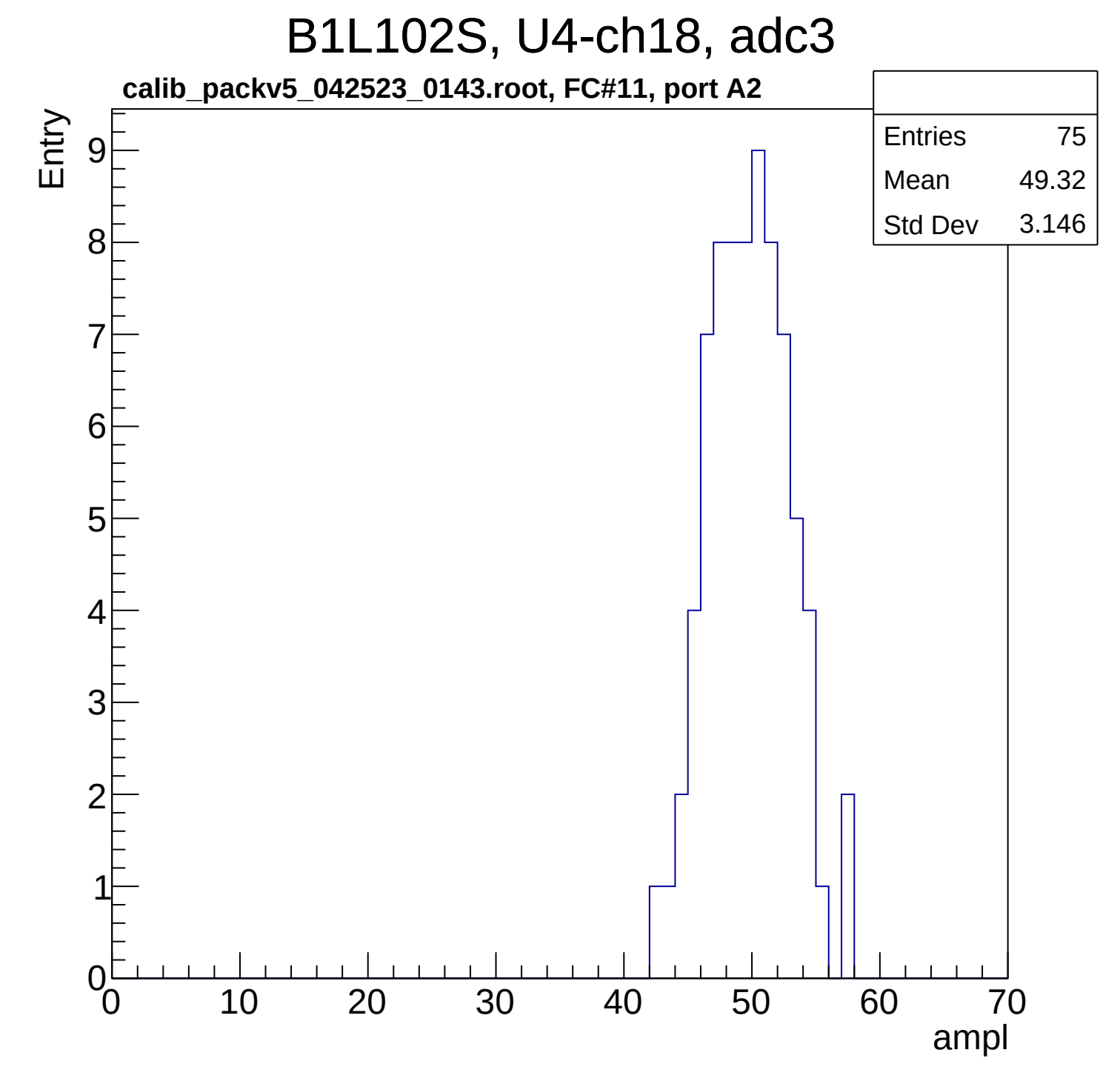
B1L102S, U4-ch18, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 49.32
Std Dev 3.146
Entry
ampl
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3
4
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6
7
8
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0
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20
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60
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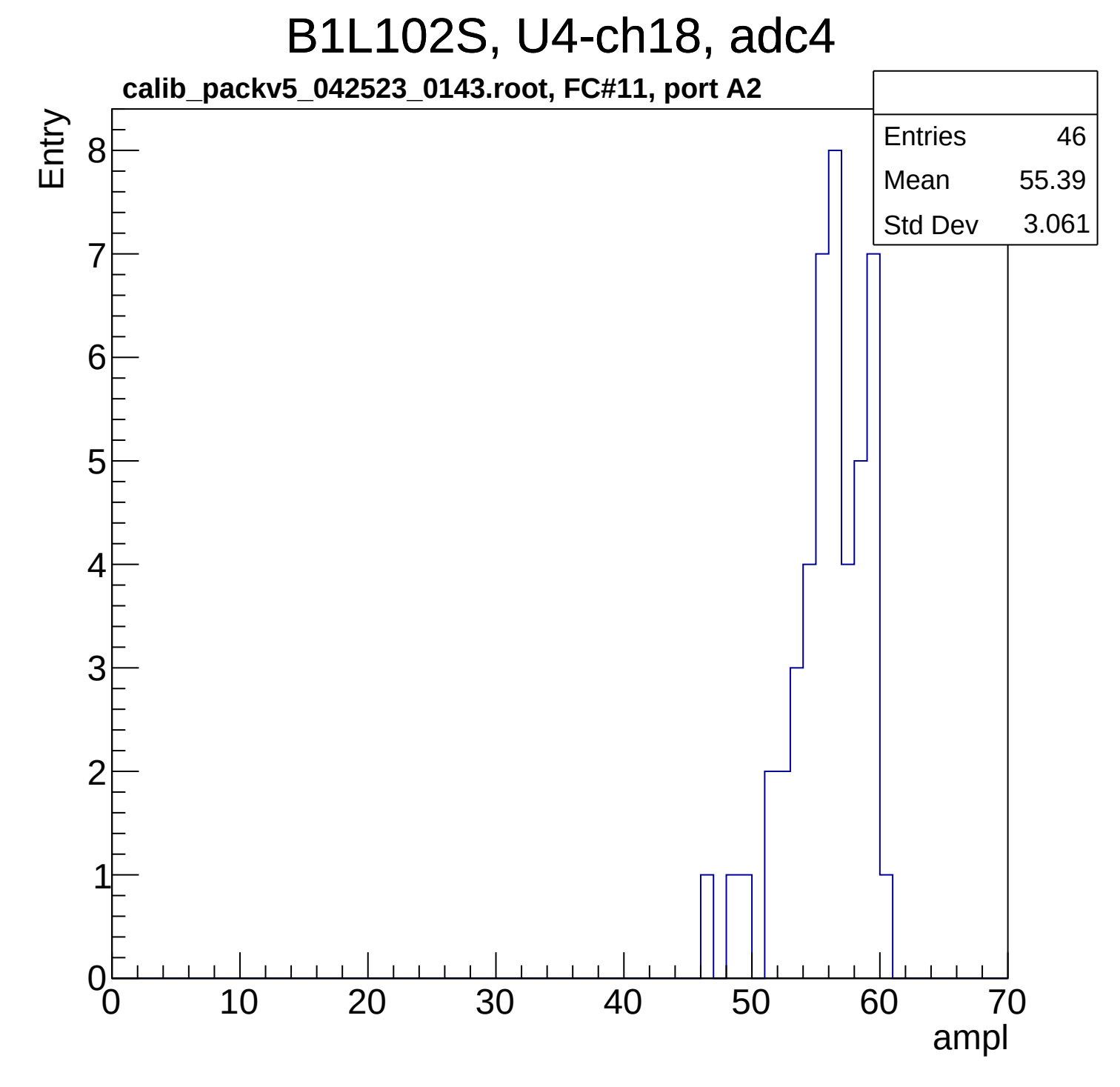
B1L102S, U4-ch18, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 46
Mean 55.39
Std Dev 3.061
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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60
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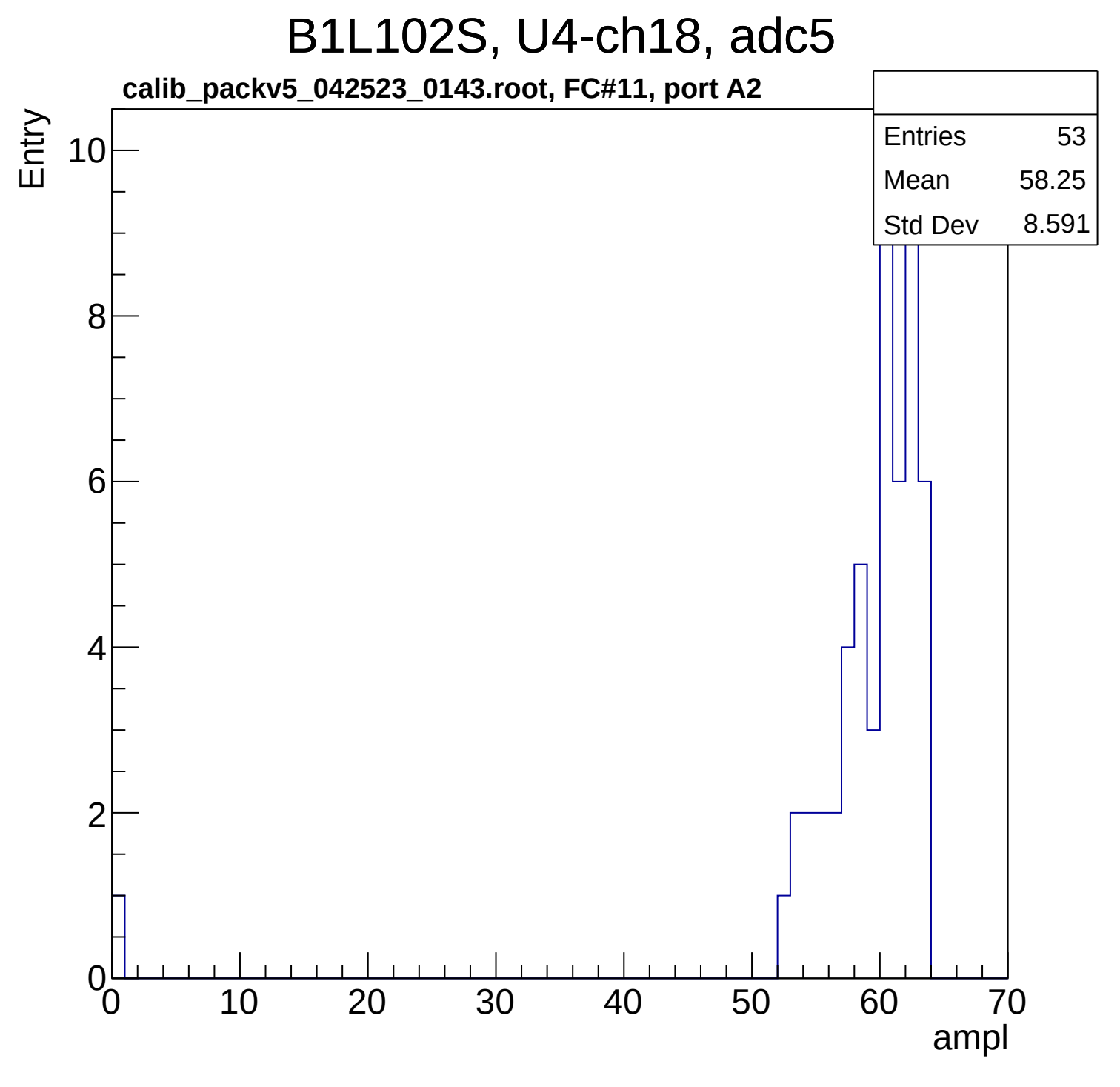
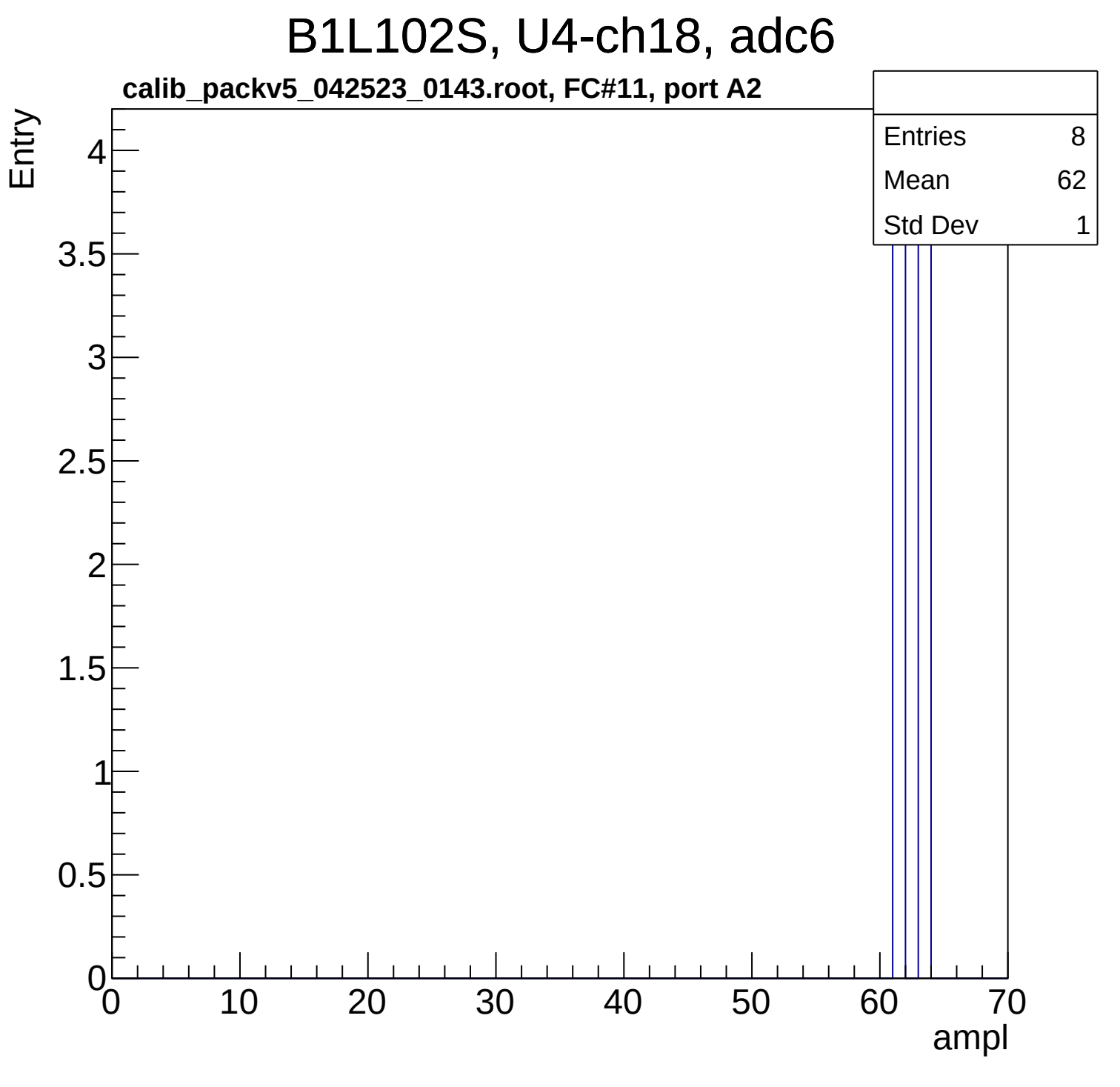
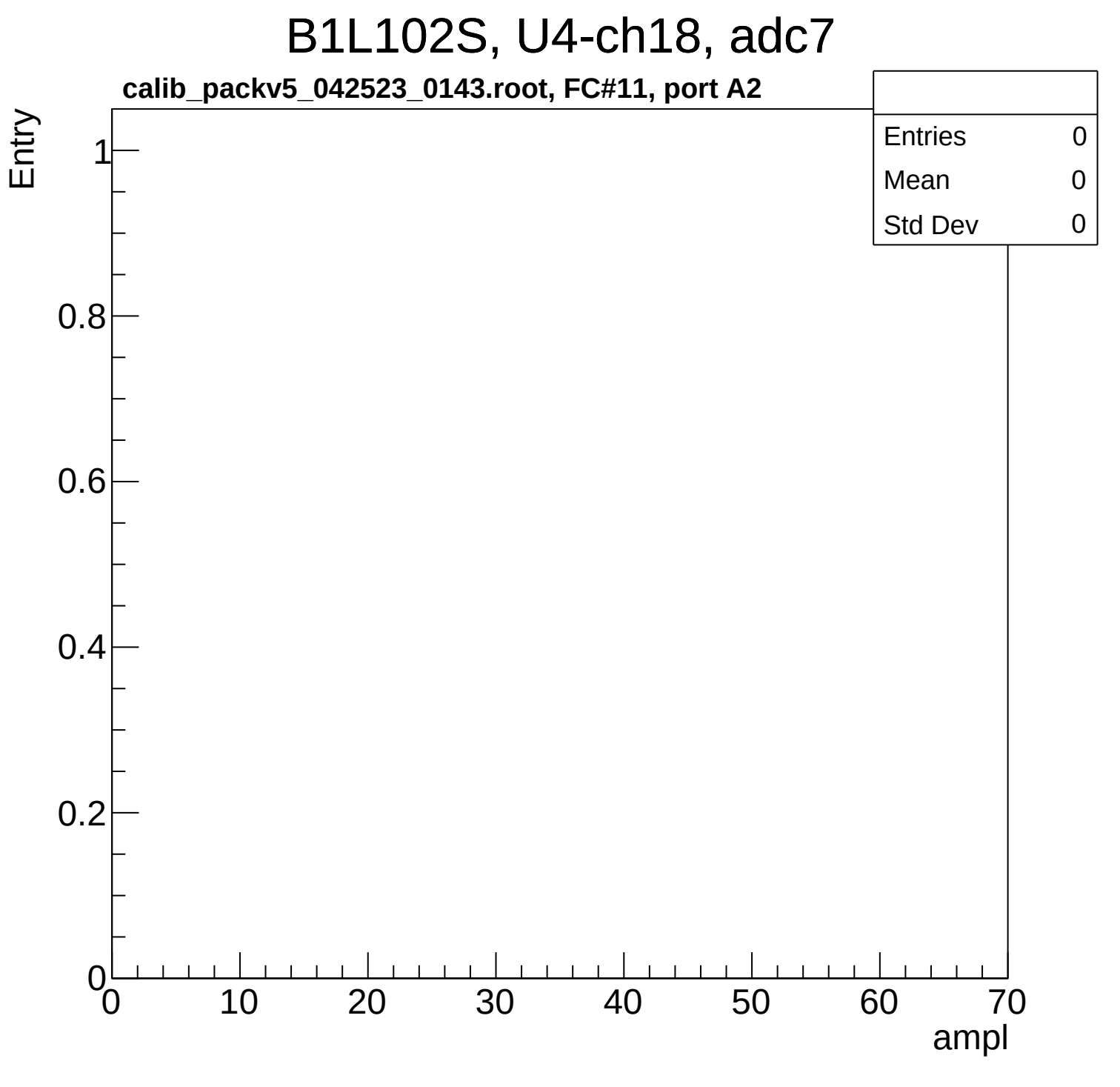

B1L102S, U4-ch18, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 58.25
Std Dev 8.591
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch18, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 8
Mean 62
Std Dev 1
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U4-ch18, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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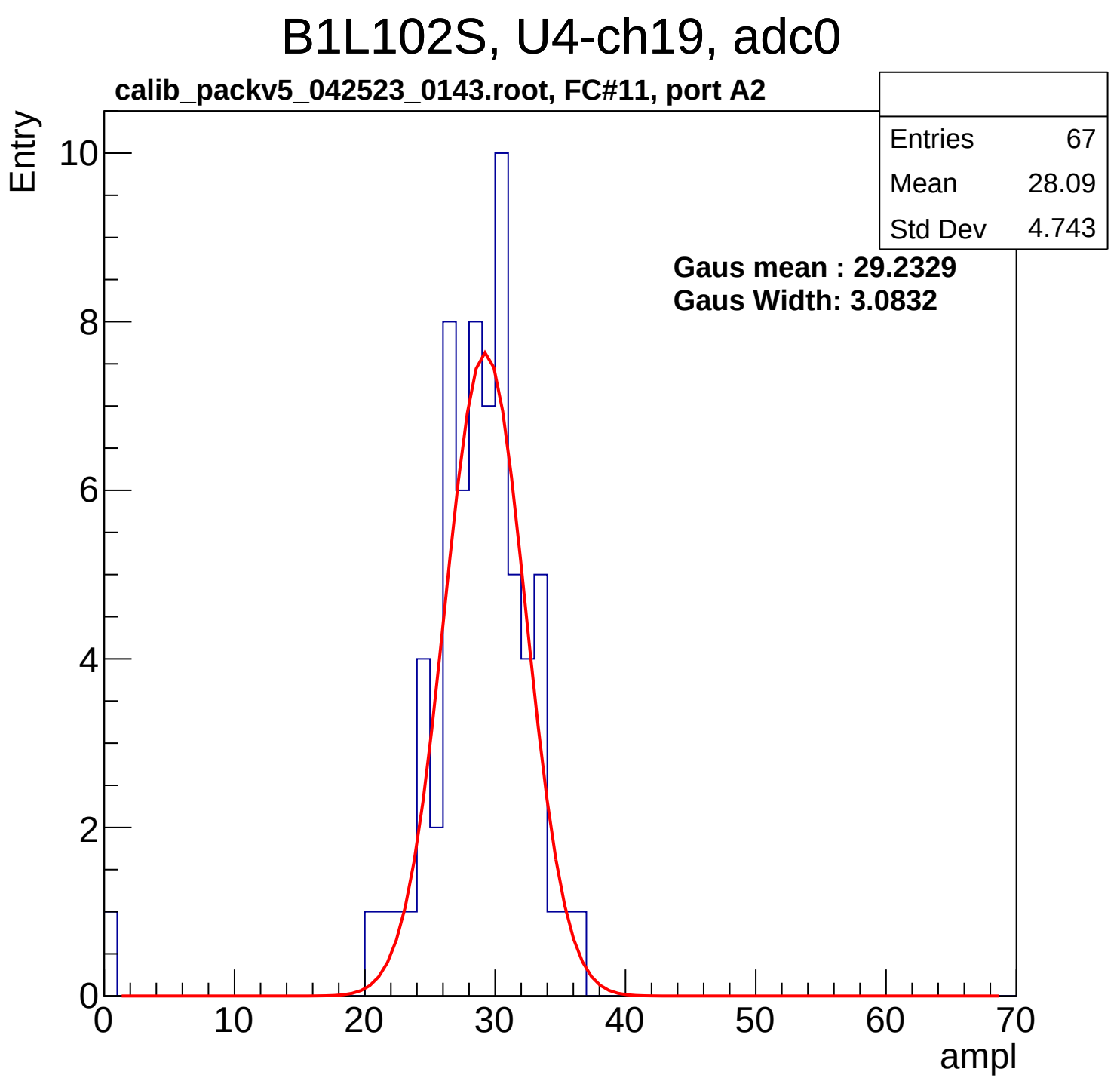
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch19, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 28.09
Std Dev 4.743
Gaus mean : 29.2329
Gaus Width: 3.0832
Entry
ampl
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2
4
6
8
10
0
10
20
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40
50
60
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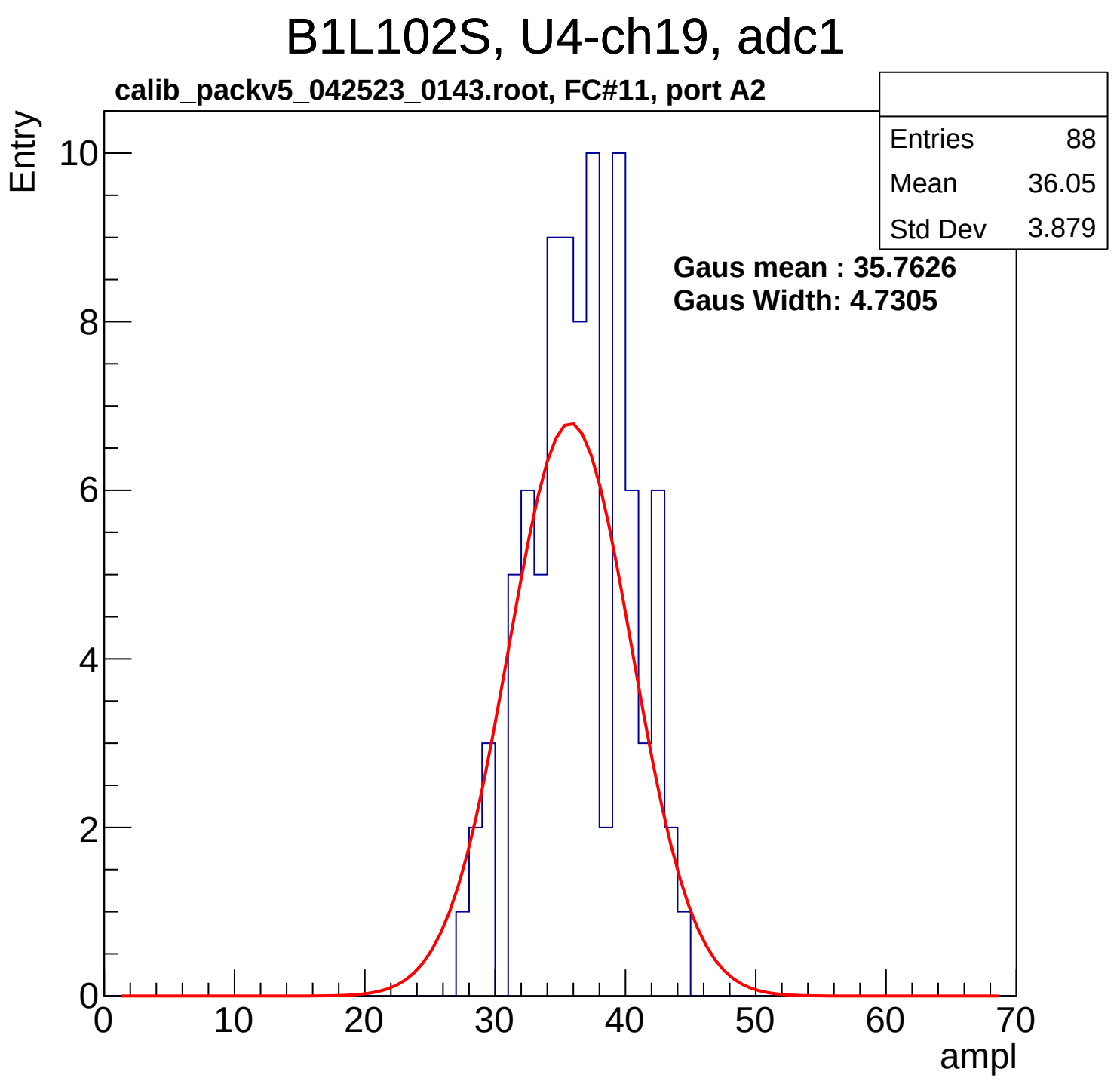
B1L102S, U4-ch19, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 88
Mean 36.05
Std Dev 3.879
Gaus mean : 35.7626
Gaus Width: 4.7305
Entry
ampl
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2
4
6
8
10
0
10
20
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40
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60
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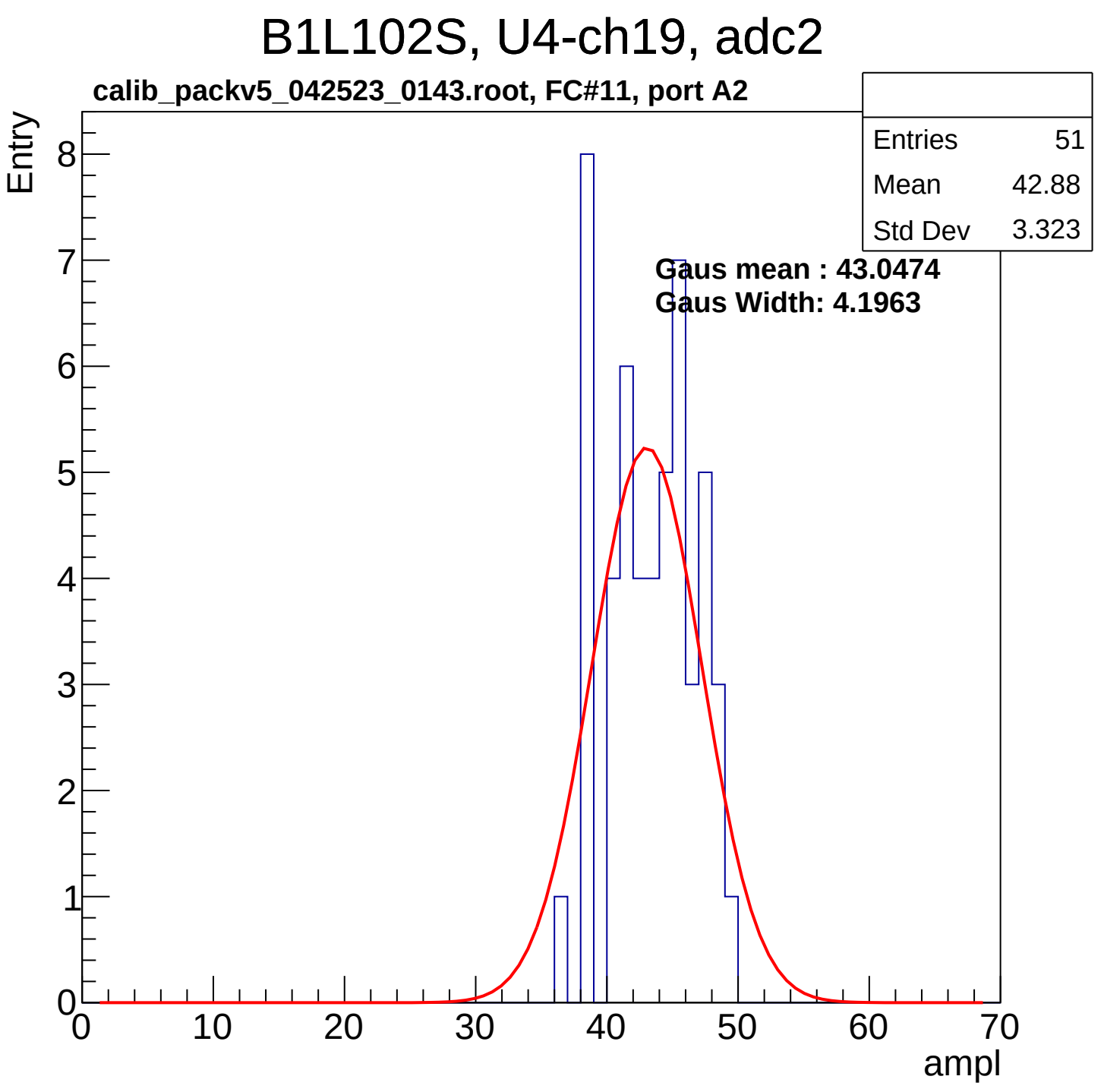
B1L102S, U4-ch19, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 42.88
Std Dev 3.323
Gaus mean : 43.0474
Gaus Width: 4.1963
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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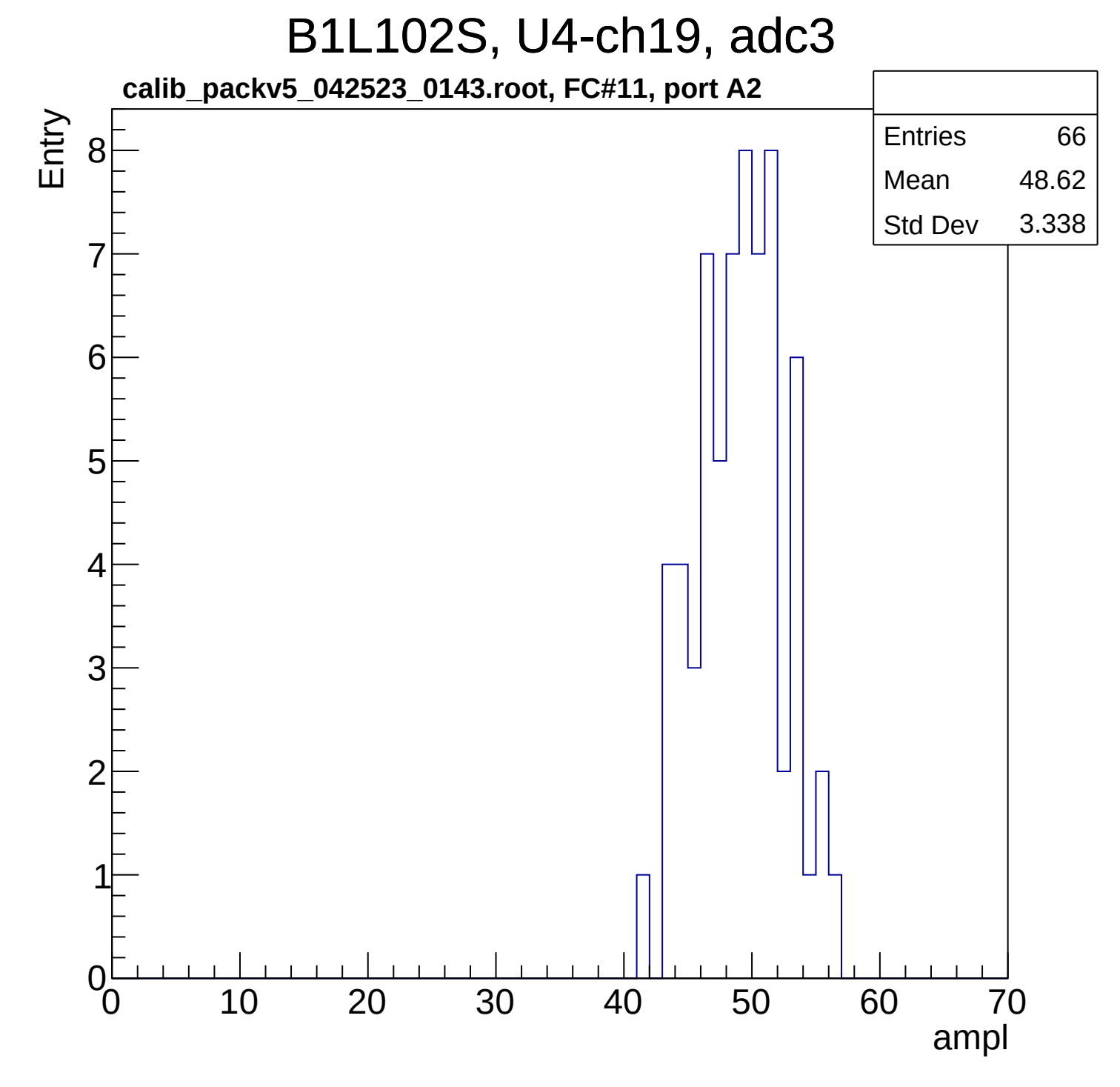
B1L102S, U4-ch19, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 48.62
Std Dev 3.338
Entry
ampl
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2
3
4
5
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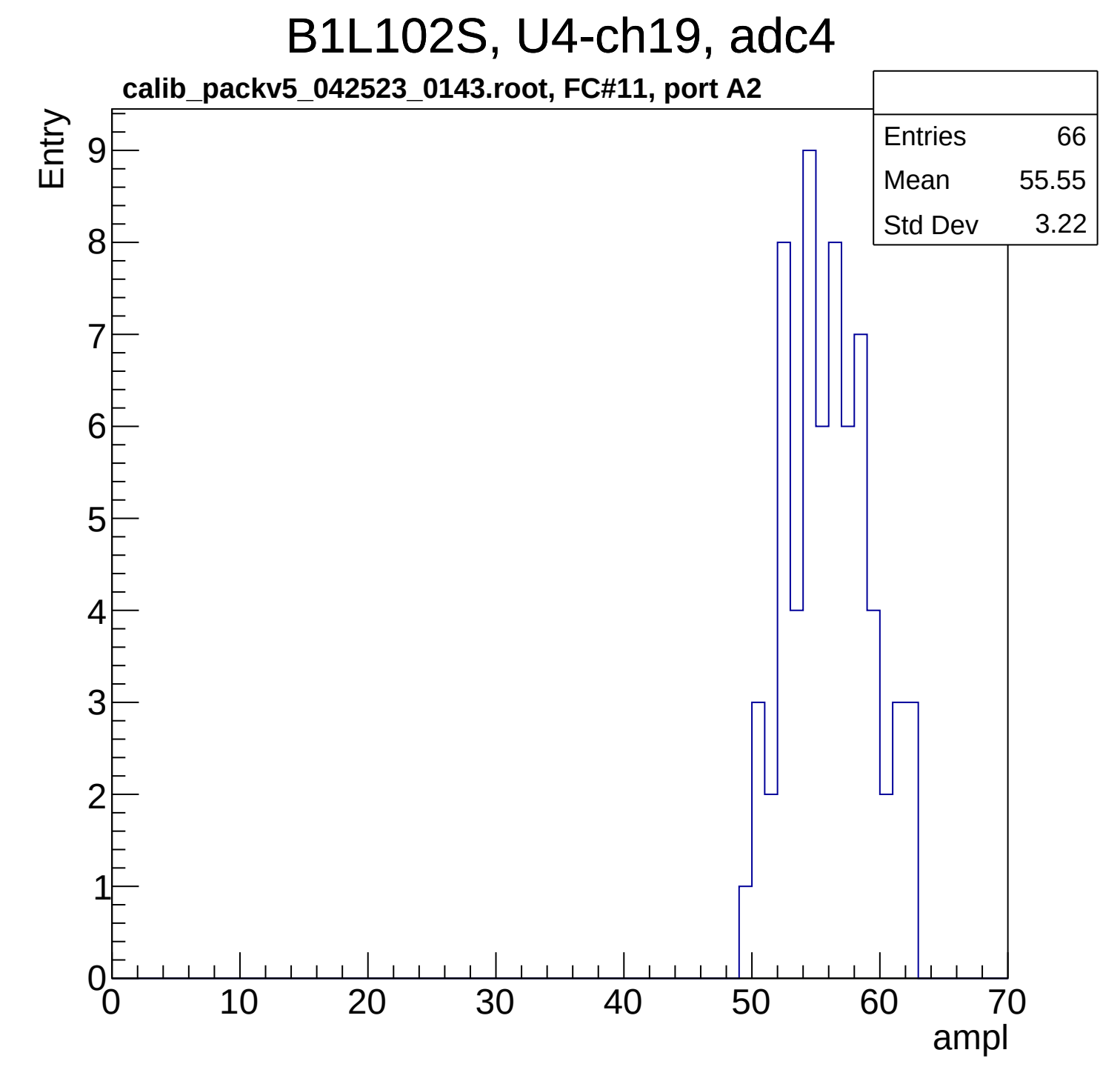
B1L102S, U4-ch19, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 55.55
Std Dev 3.22
Entry
ampl
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2
3
4
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6
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0
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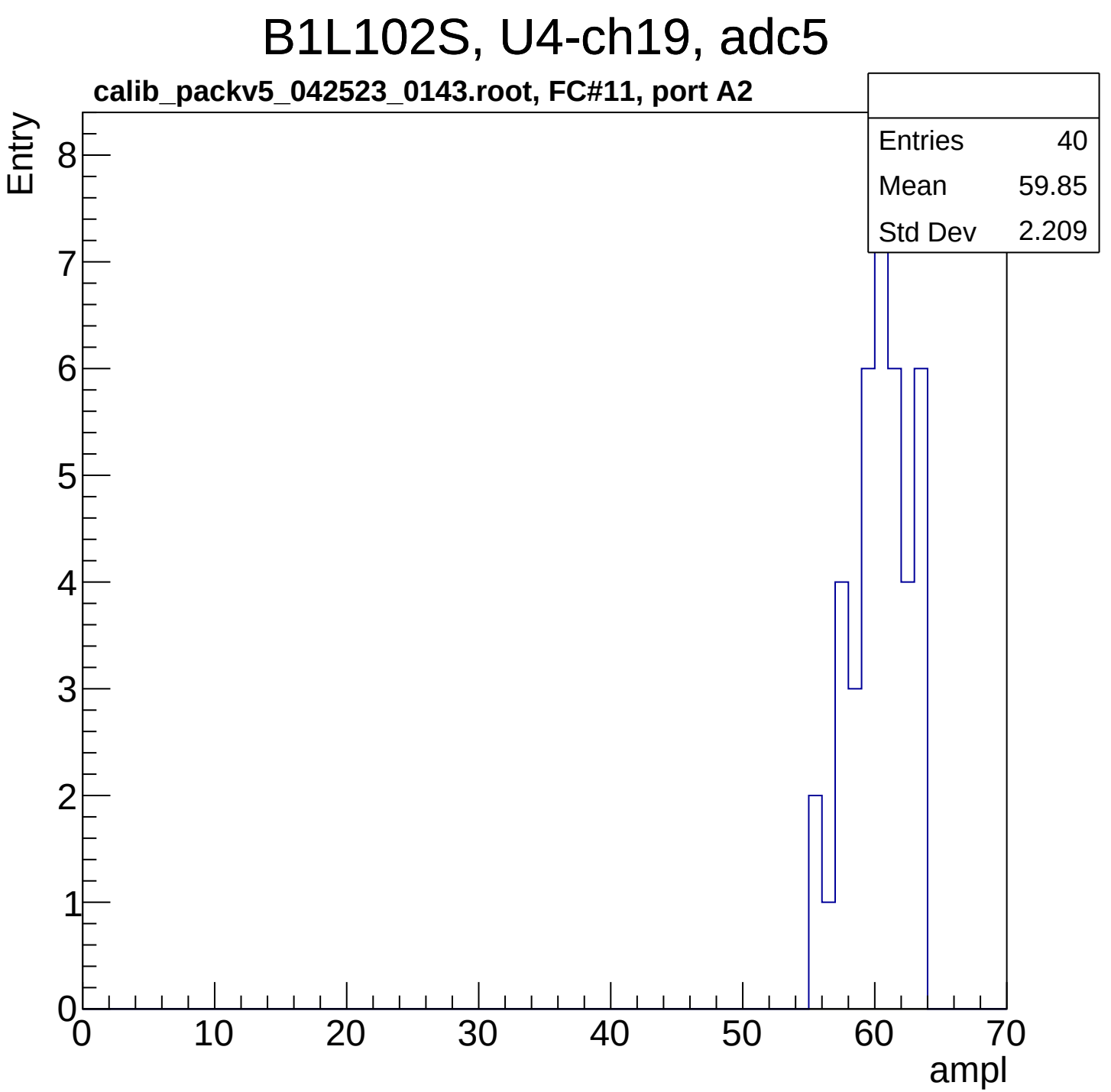
B1L102S, U4-ch19, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 40
Mean 59.85
Std Dev 2.209
Entry
ampl
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2
3
4
5
6
7
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0
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40
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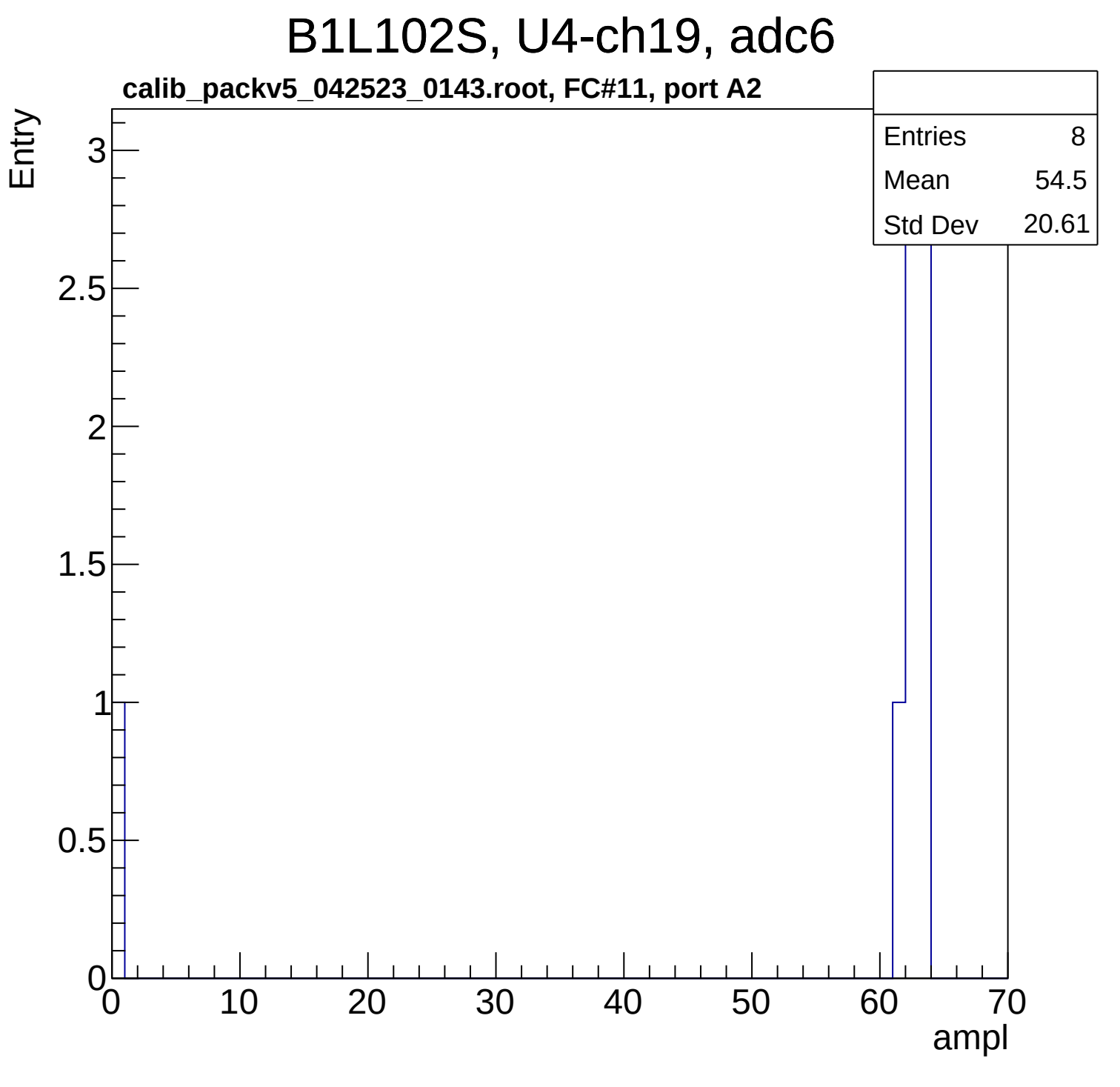
B1L102S, U4-ch19, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 8
Mean 54.5
Std Dev 20.61
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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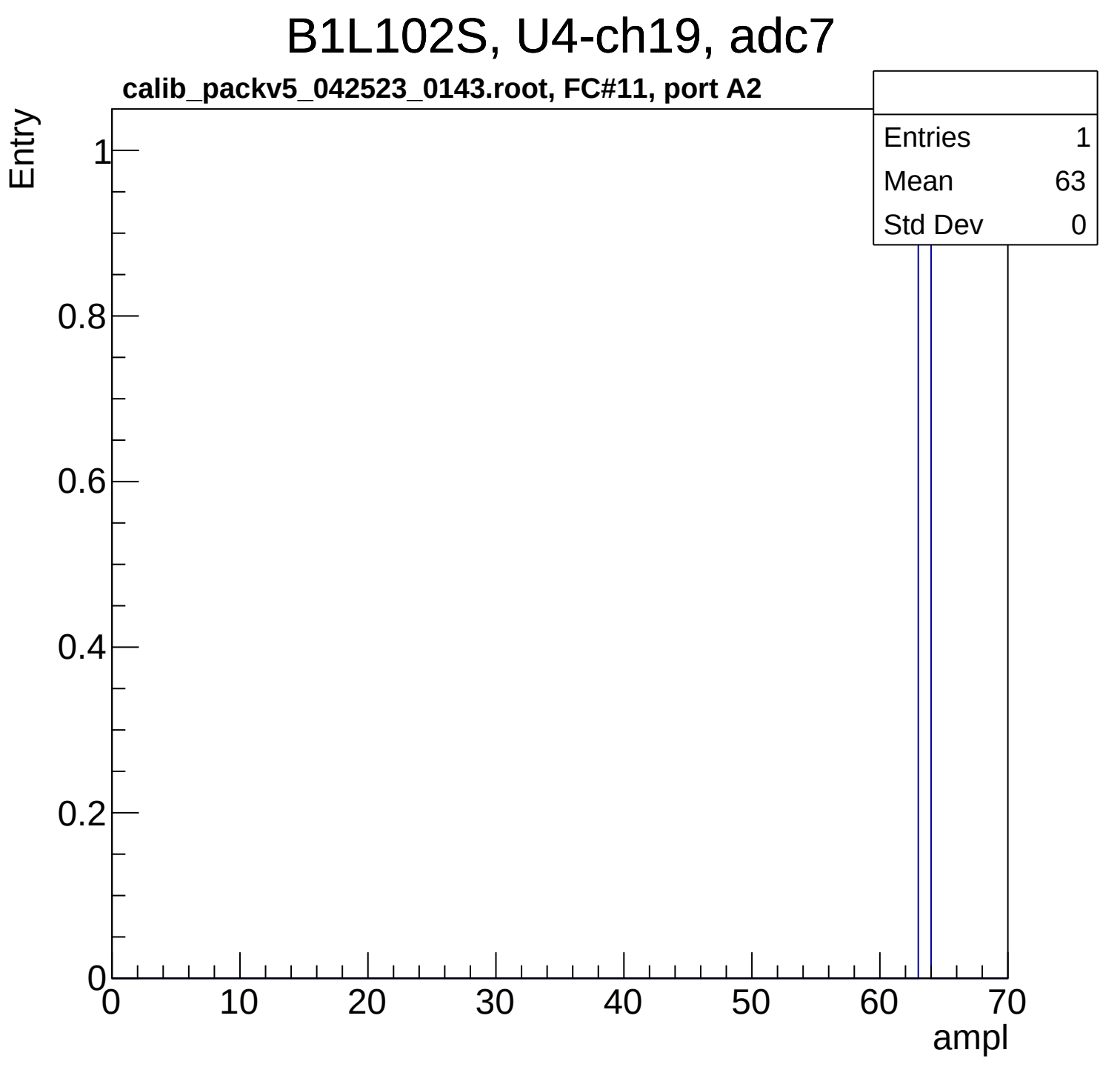
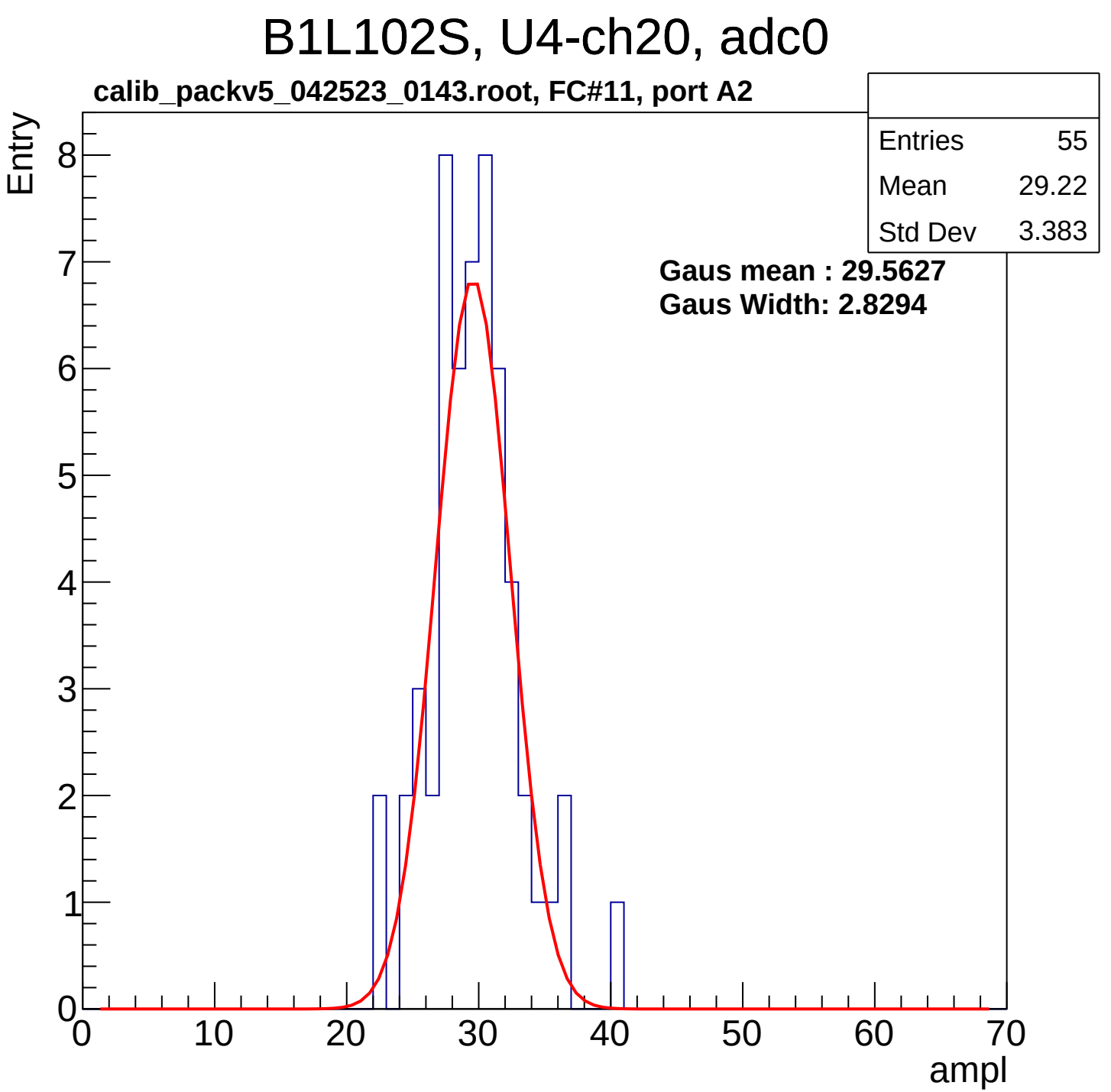

B1L102S, U4-ch19, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch20, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 29.22
Std Dev 3.383
Gaus mean : 29.5627
Gaus Width: 2.8294
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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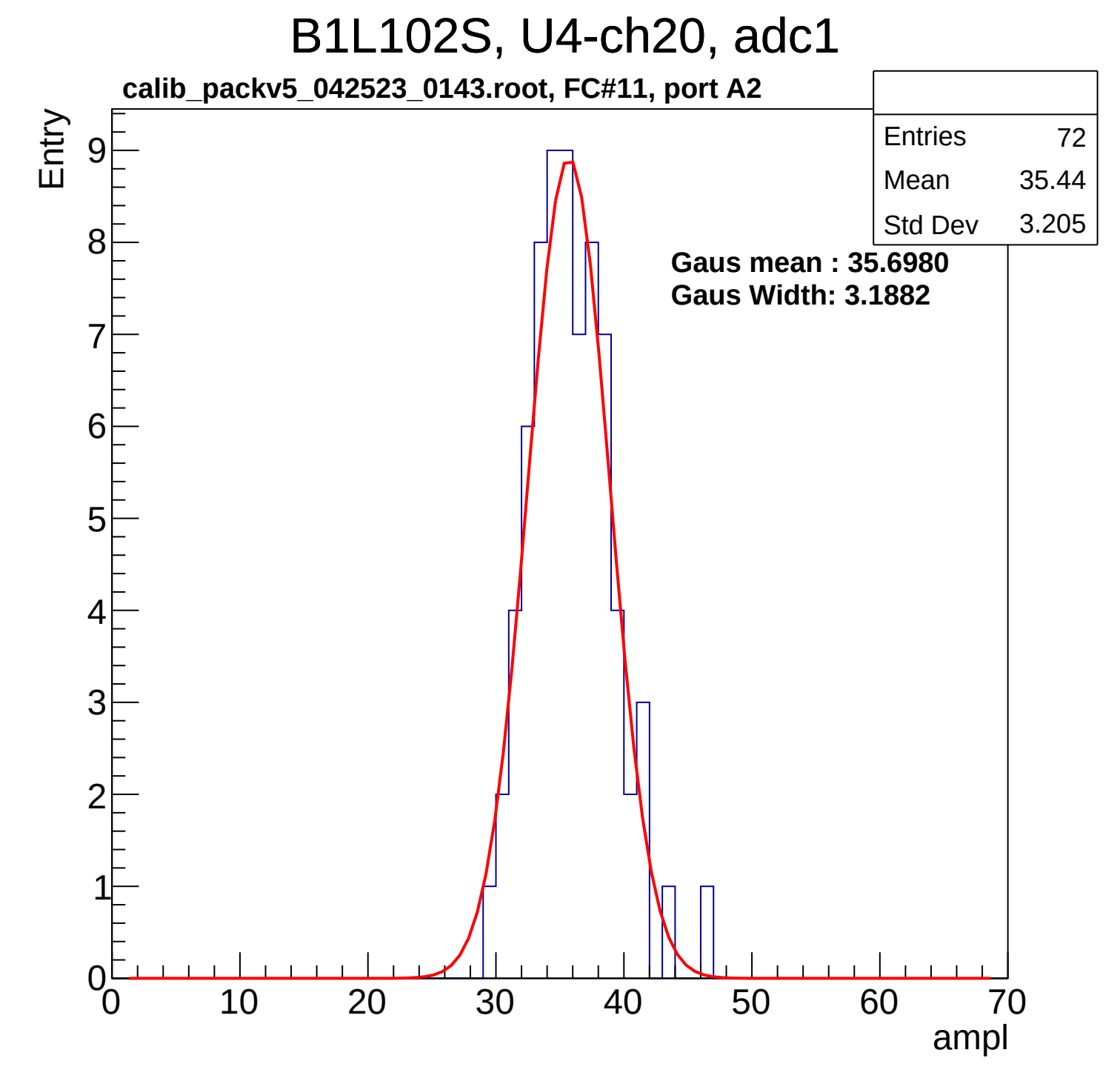
B1L102S, U4-ch20, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 72
Mean 35.44
Std Dev 3.205
Gaus mean : 35.6980
Gaus Width: 3.1882
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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60
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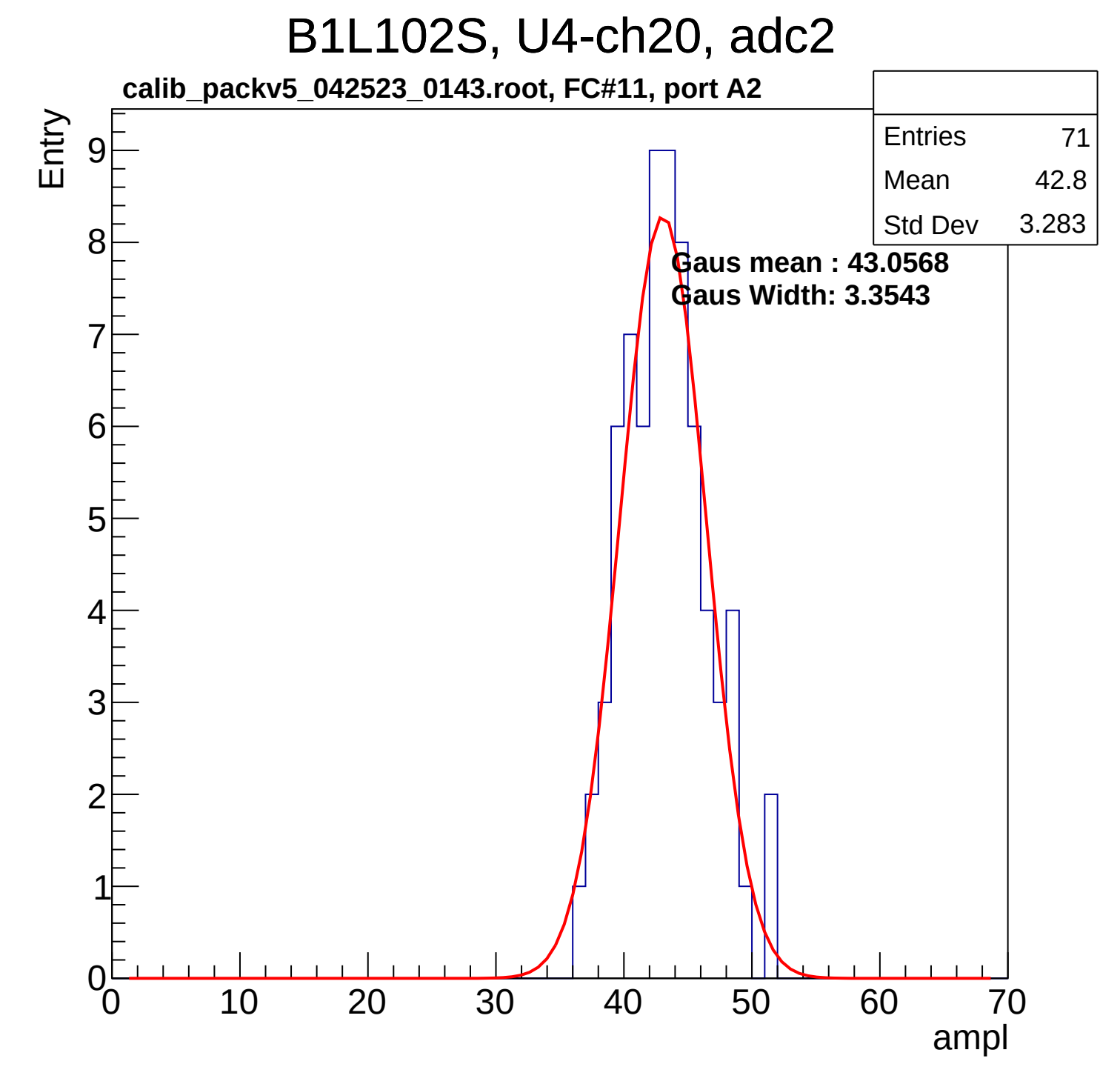
B1L102S, U4-ch20, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 42.8
Std Dev 3.283
Gaus mean : 43.0568
Gaus Width: 3.3543
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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40
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60
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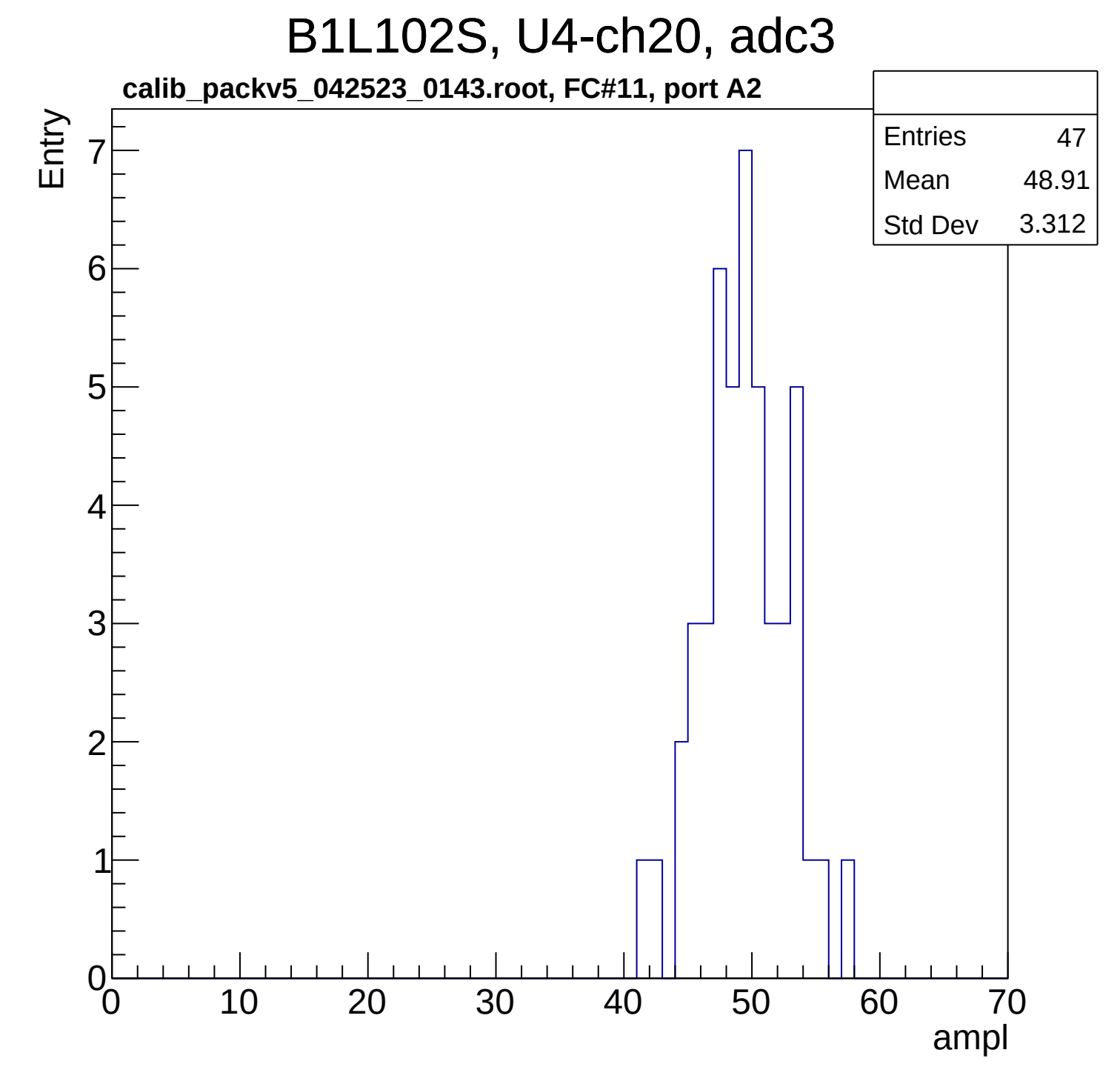
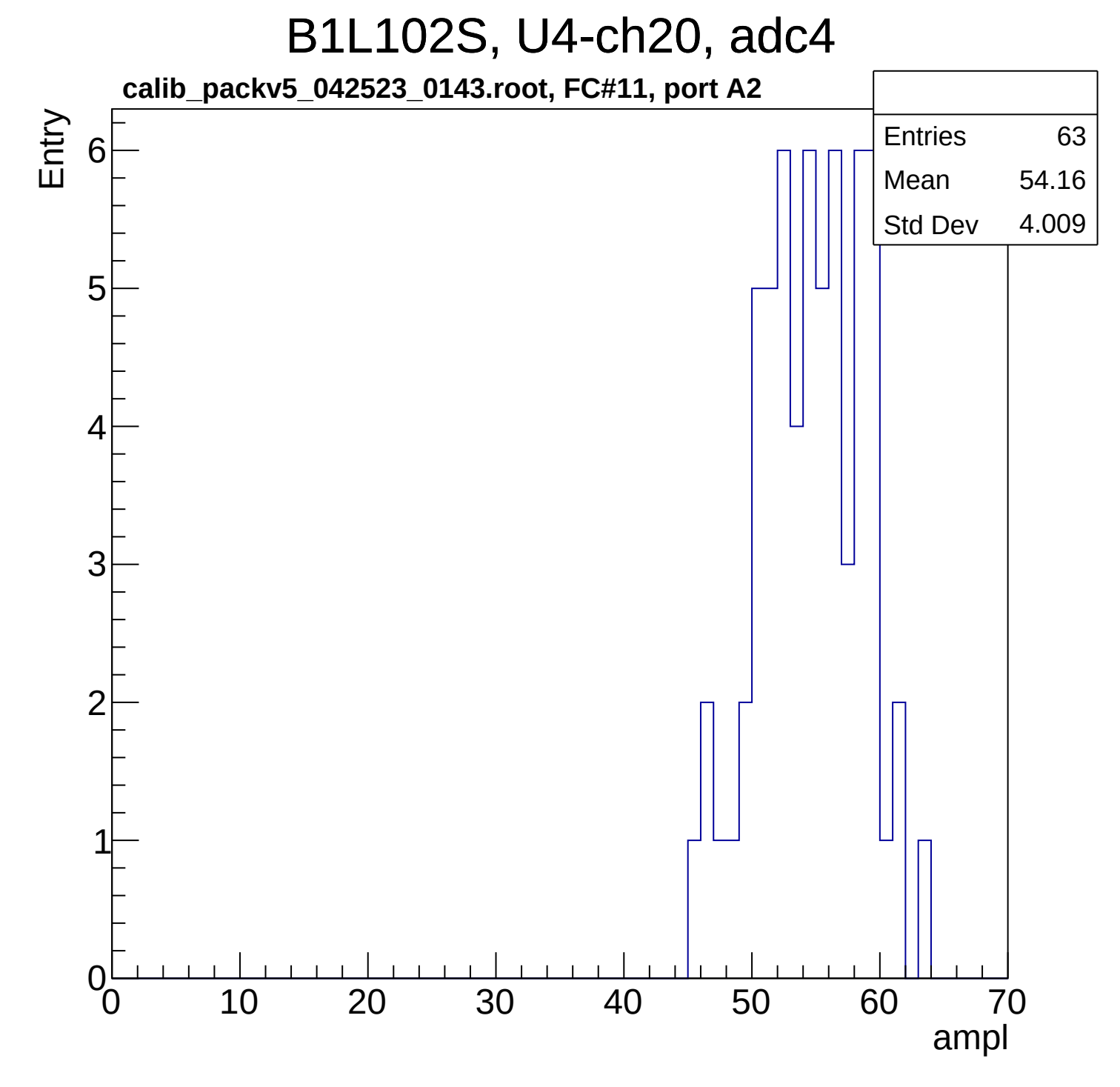
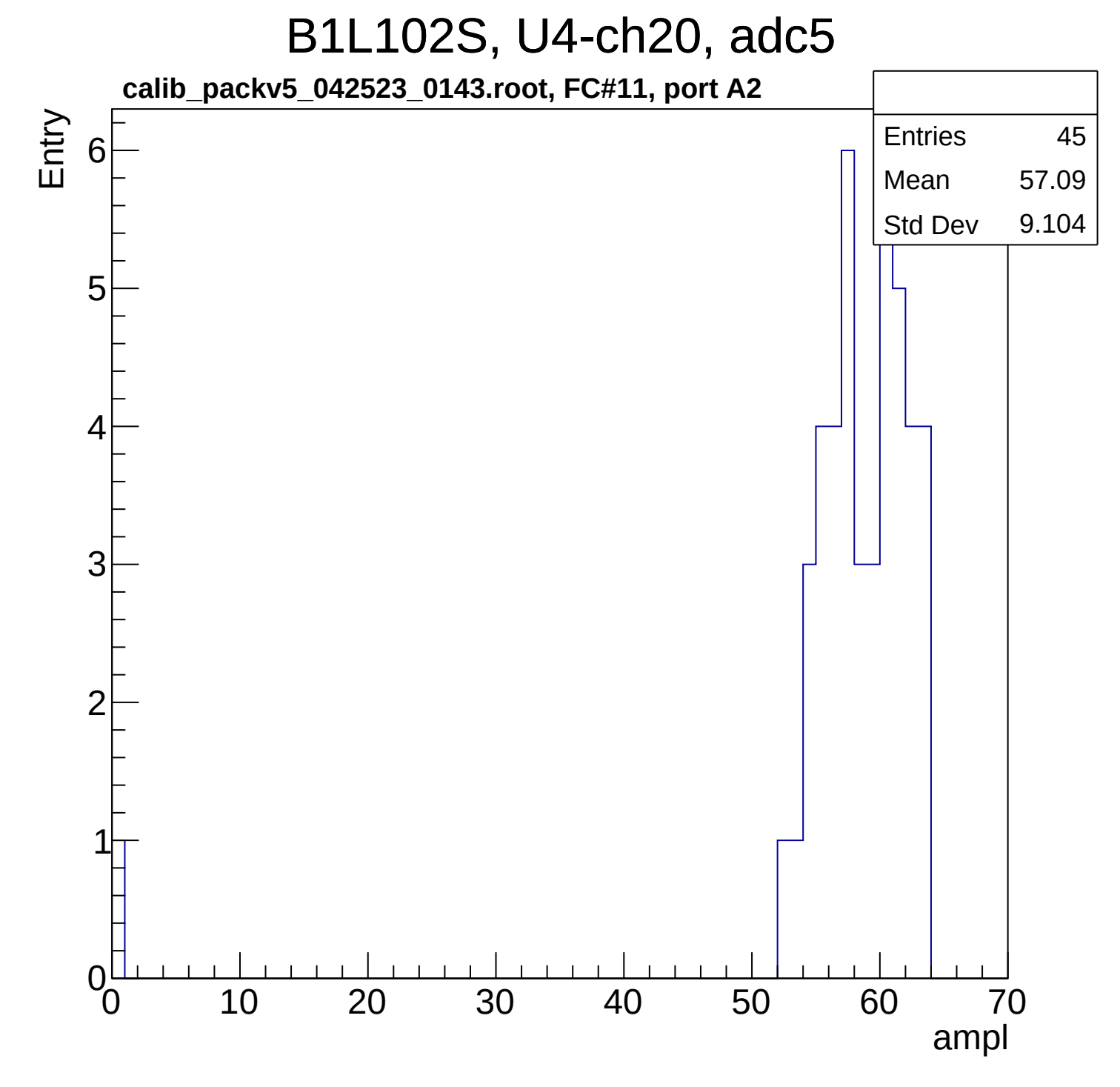
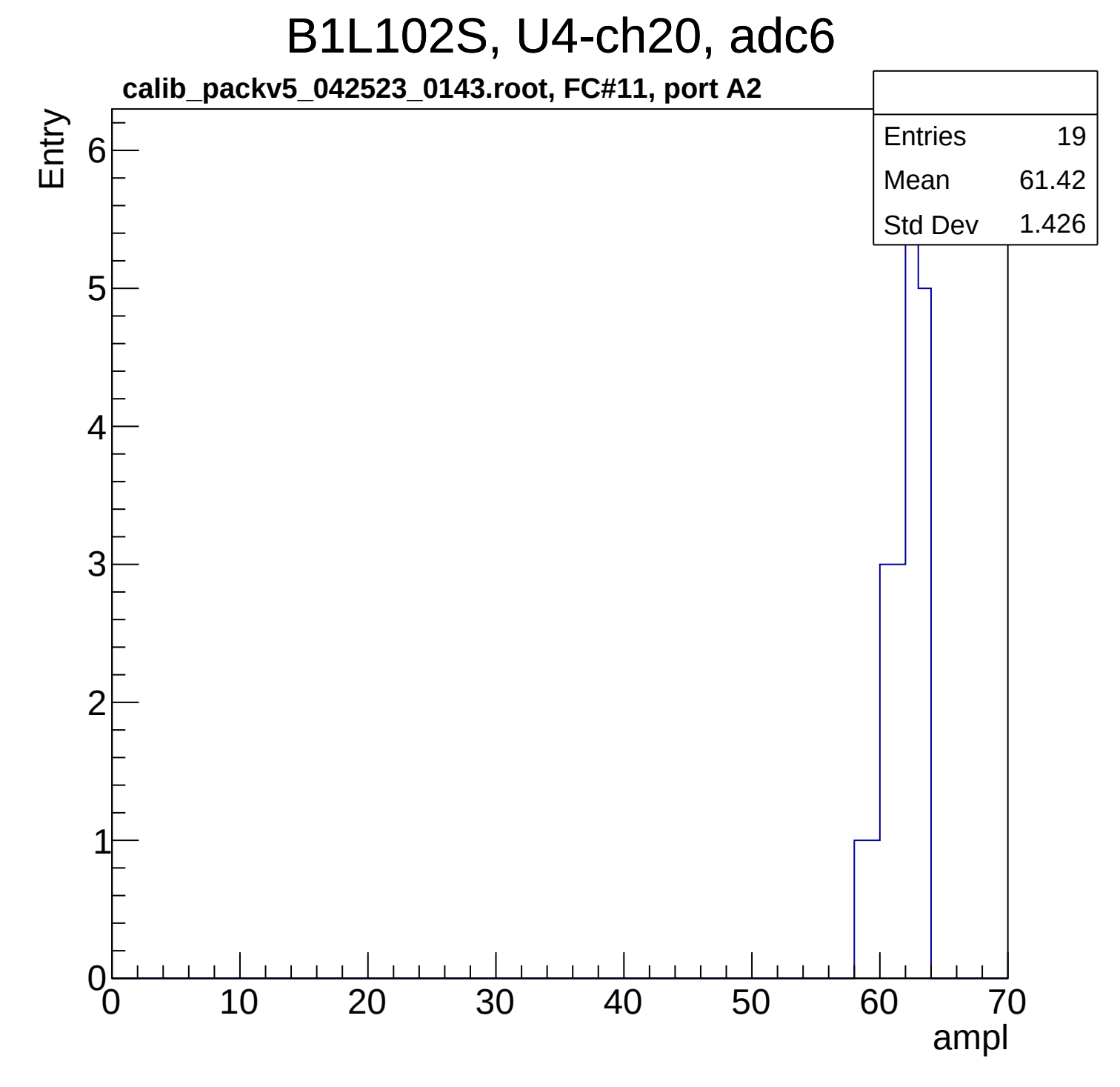

B1L102S, U4-ch20, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 47
Mean 48.91
Std Dev 3.312
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch20, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 54.16
Std Dev 4.009
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch20, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 45
Mean 57.09
Std Dev 9.104
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L102S, U4-ch20, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 19
Mean 61.42
Std Dev 1.426
Entry
ampl
0
1
2
3
4
5
6
0
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20
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40
50
60
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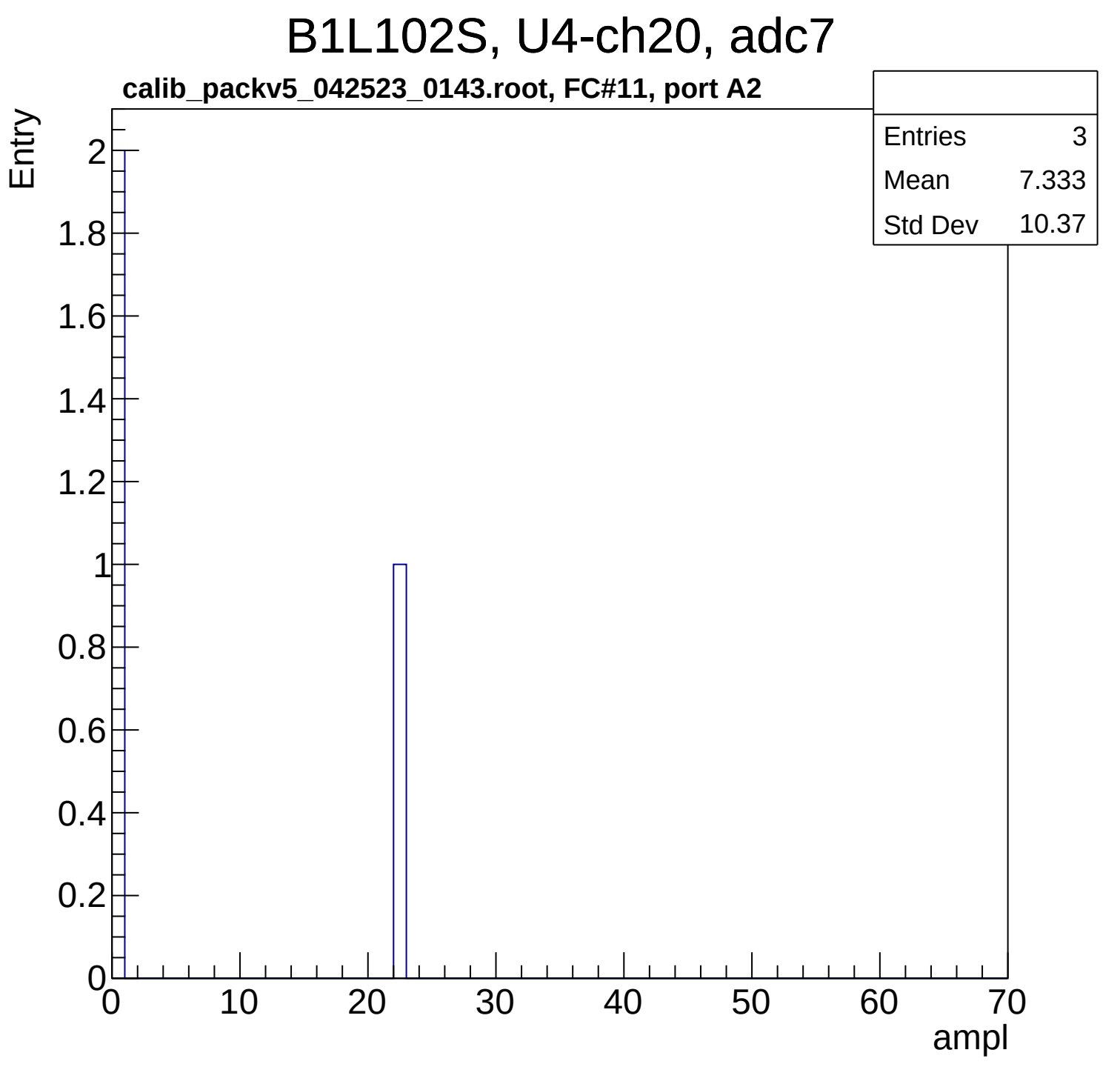
B1L102S, U4-ch20, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 7.333
Std Dev 10.37
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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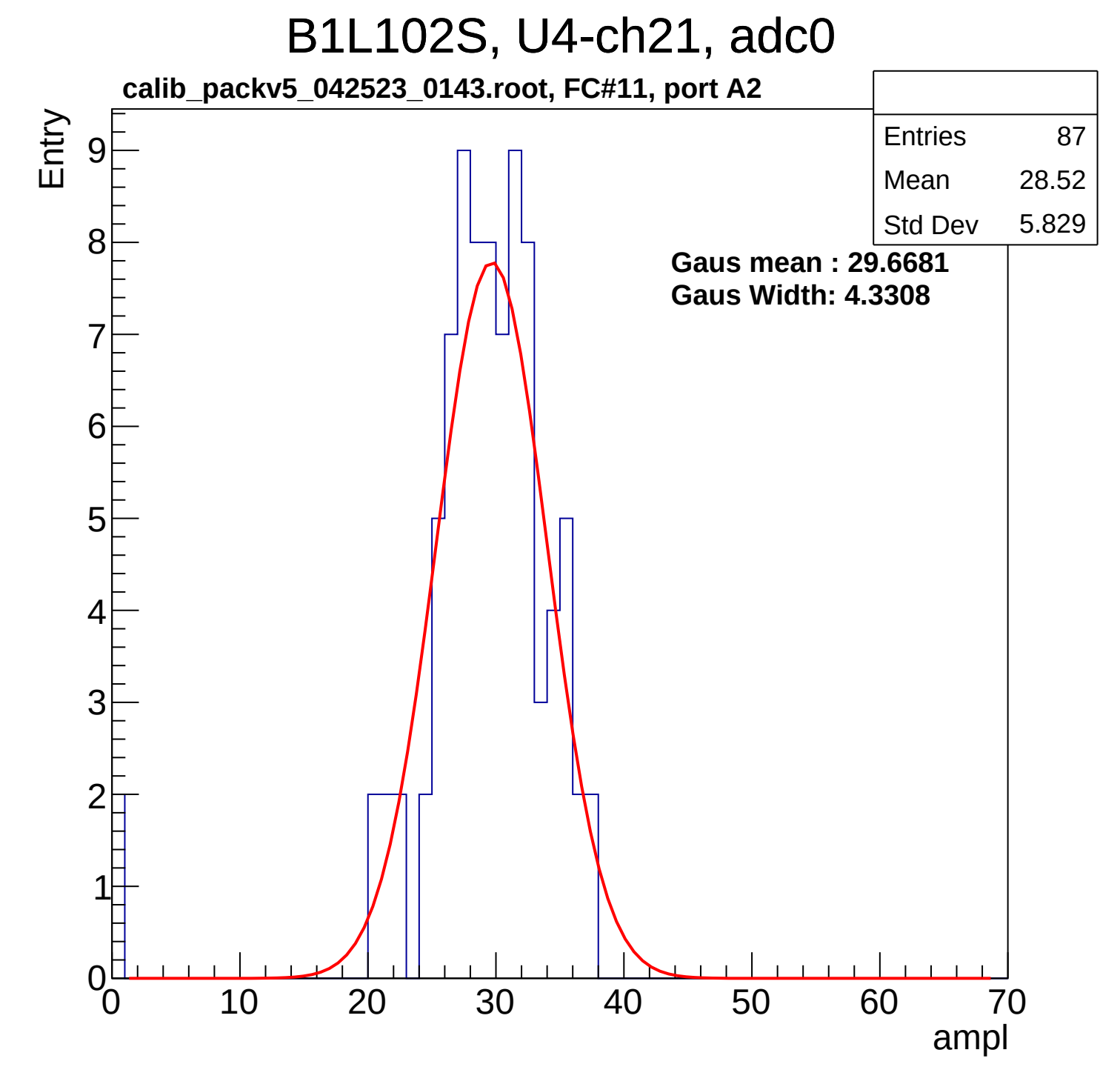
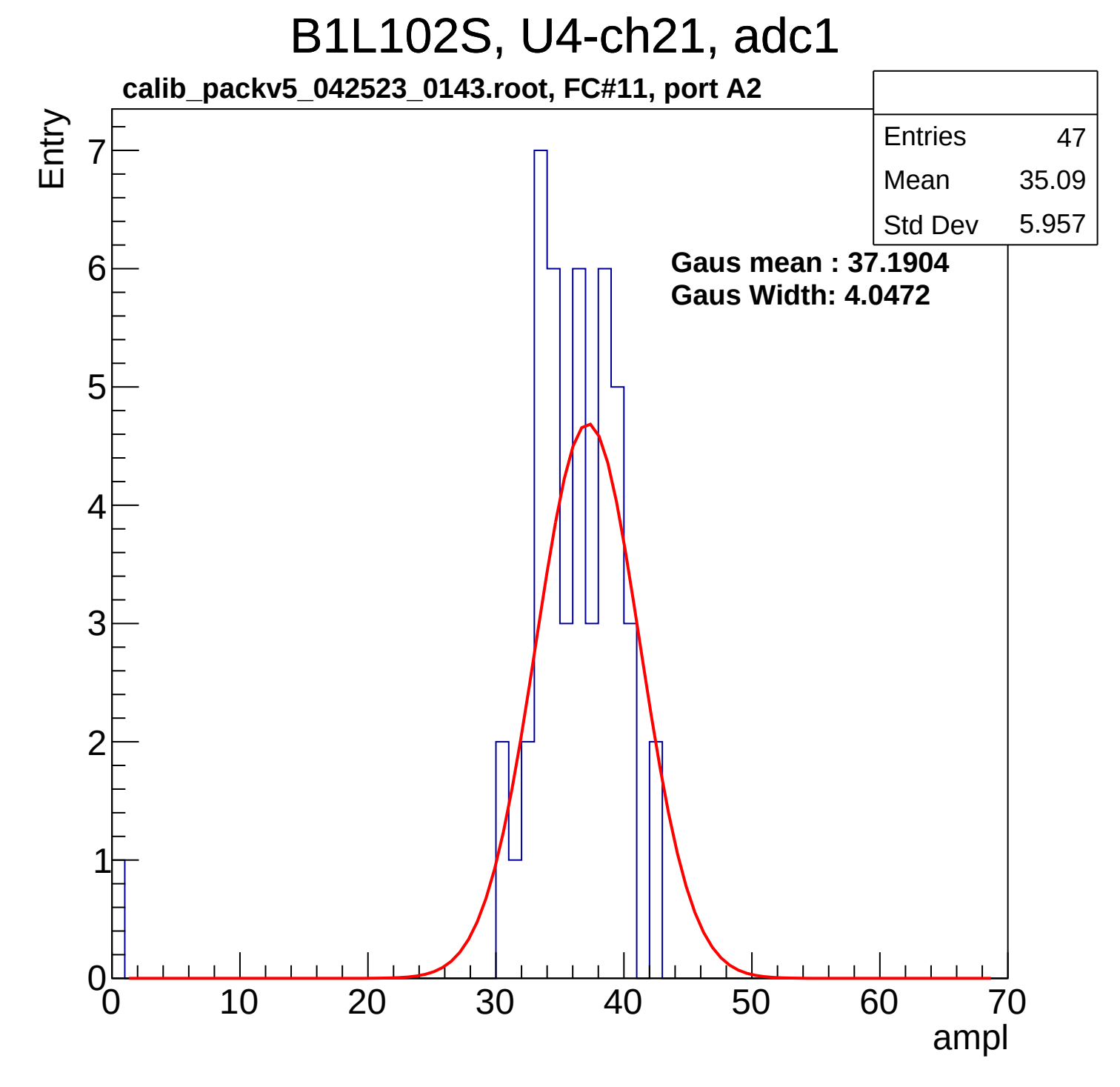

B1L102S, U4-ch21, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 87
Mean 28.52
Std Dev 5.829
Gaus mean : 29.6681
Gaus Width: 4.3308
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch21, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 47
Mean 35.09
Std Dev 5.957
Gaus mean : 37.1904
Gaus Width: 4.0472
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
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60
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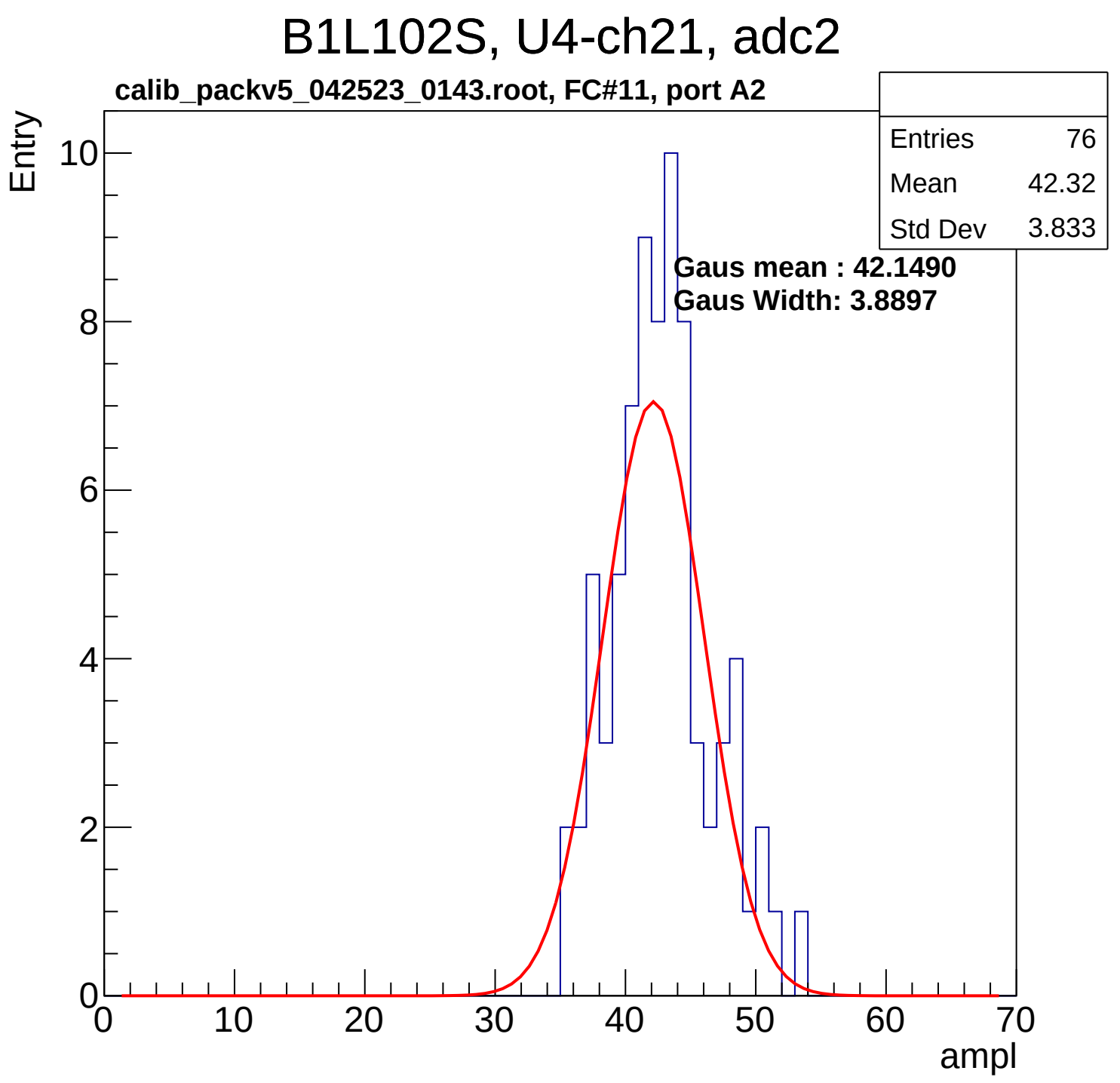
B1L102S, U4-ch21, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 42.32
Std Dev 3.833
Gaus mean : 42.1490
Gaus Width: 3.8897
Entry
ampl
0
2
4
6
8
10
0
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20
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40
50
60
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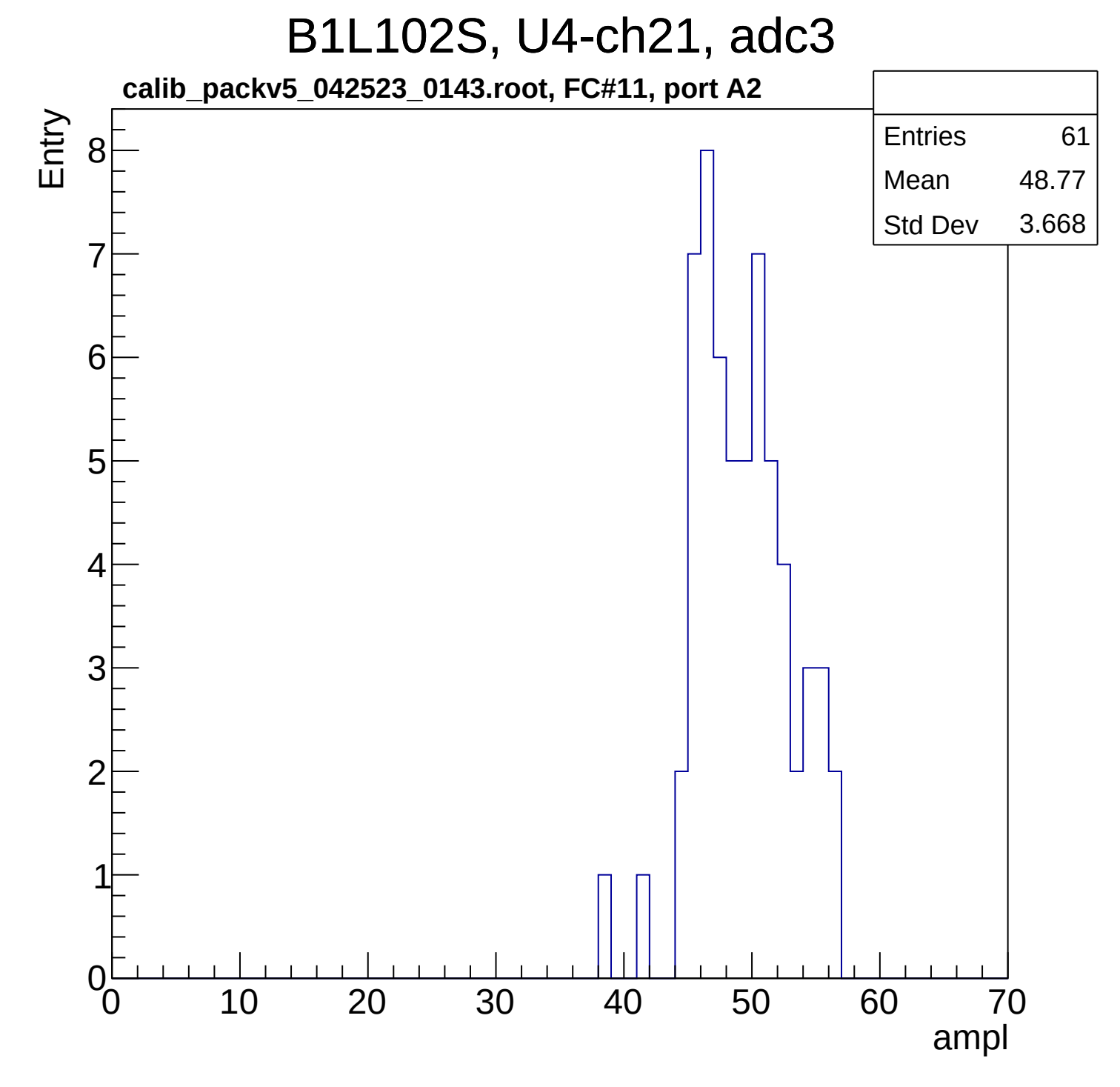
B1L102S, U4-ch21, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 48.77
Std Dev 3.668
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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40
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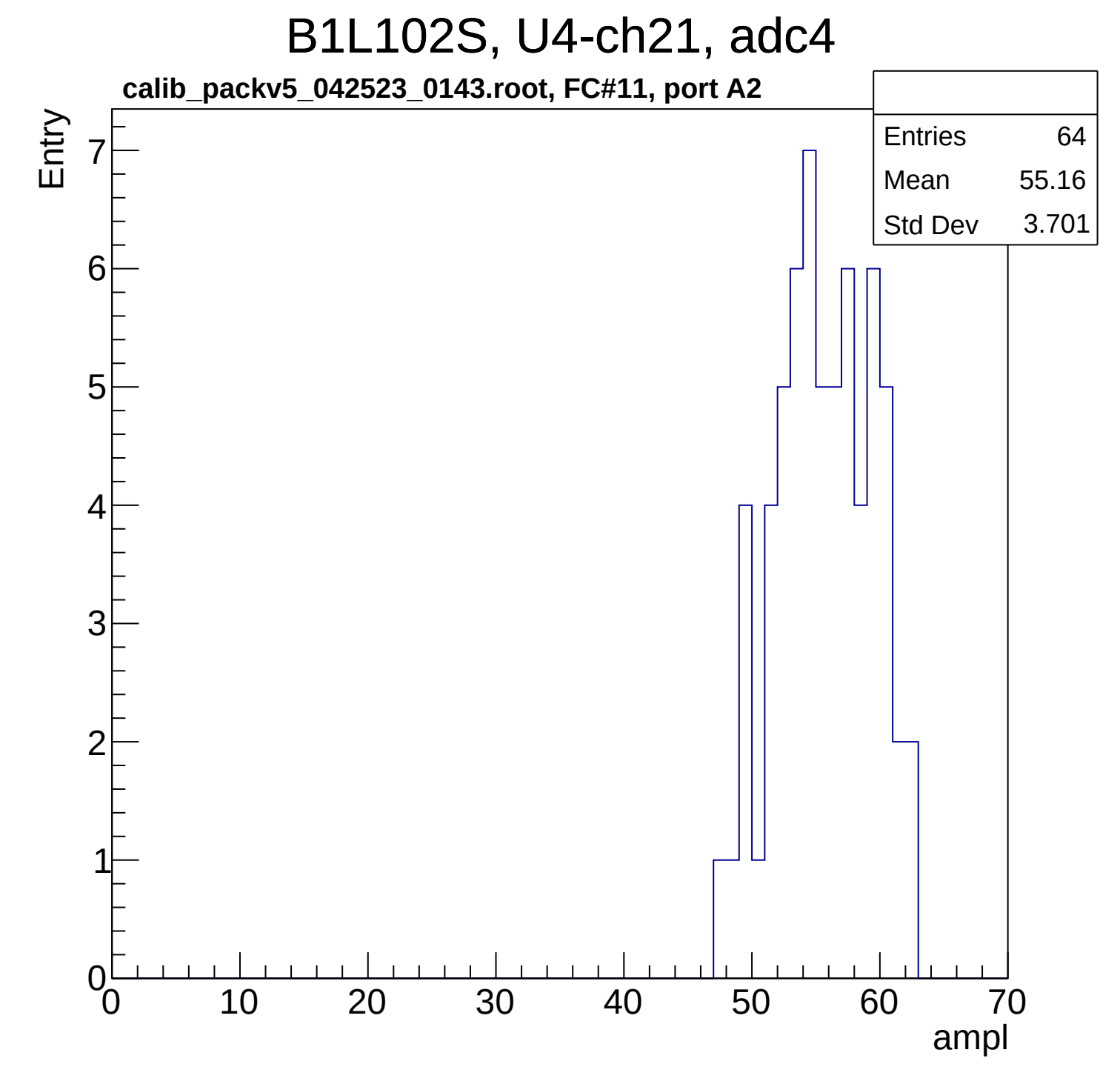
60
70


B1L102S, U4-ch21, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 55.16
Std Dev 3.701
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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40
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60
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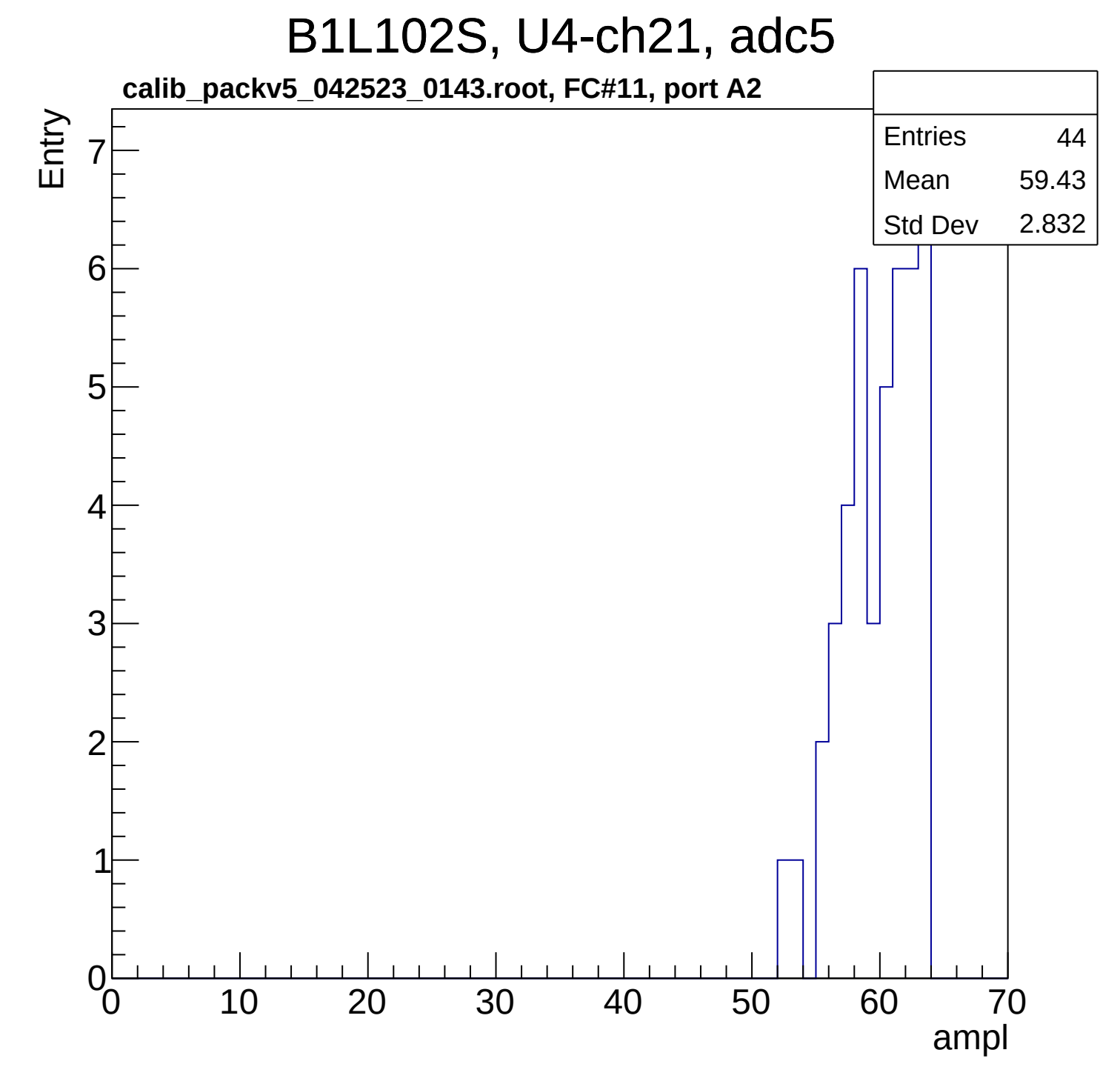
B1L102S, U4-ch21, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 44
Mean 59.43
Std Dev 2.832
Entry
ampl
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1
2
3
4
5
6
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0
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20
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40
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60
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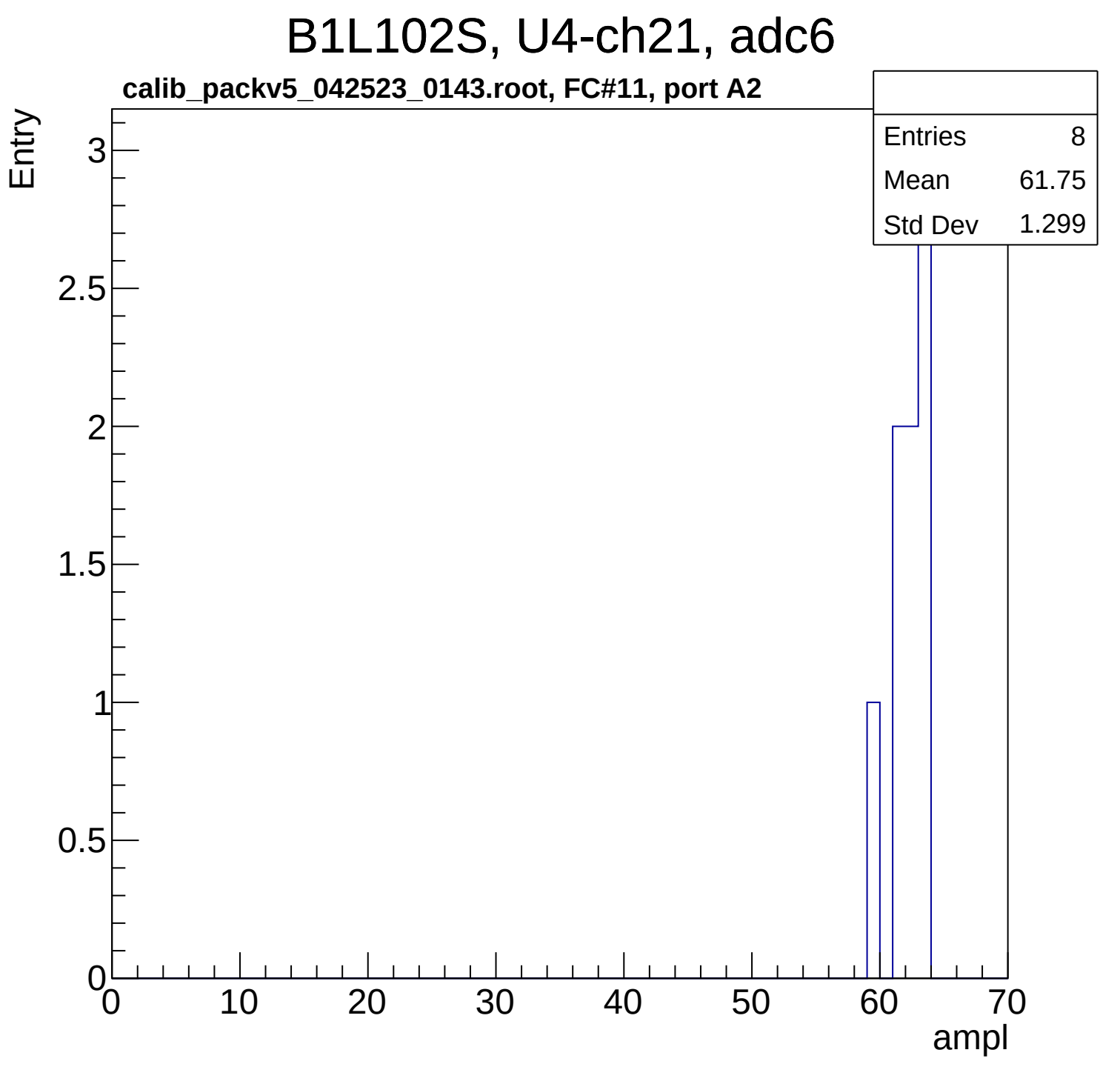
B1L102S, U4-ch21, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 8
Mean 61.75
Std Dev 1.299
Entry
ampl
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0.5
1
1.5
2
2.5
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0
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20
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60
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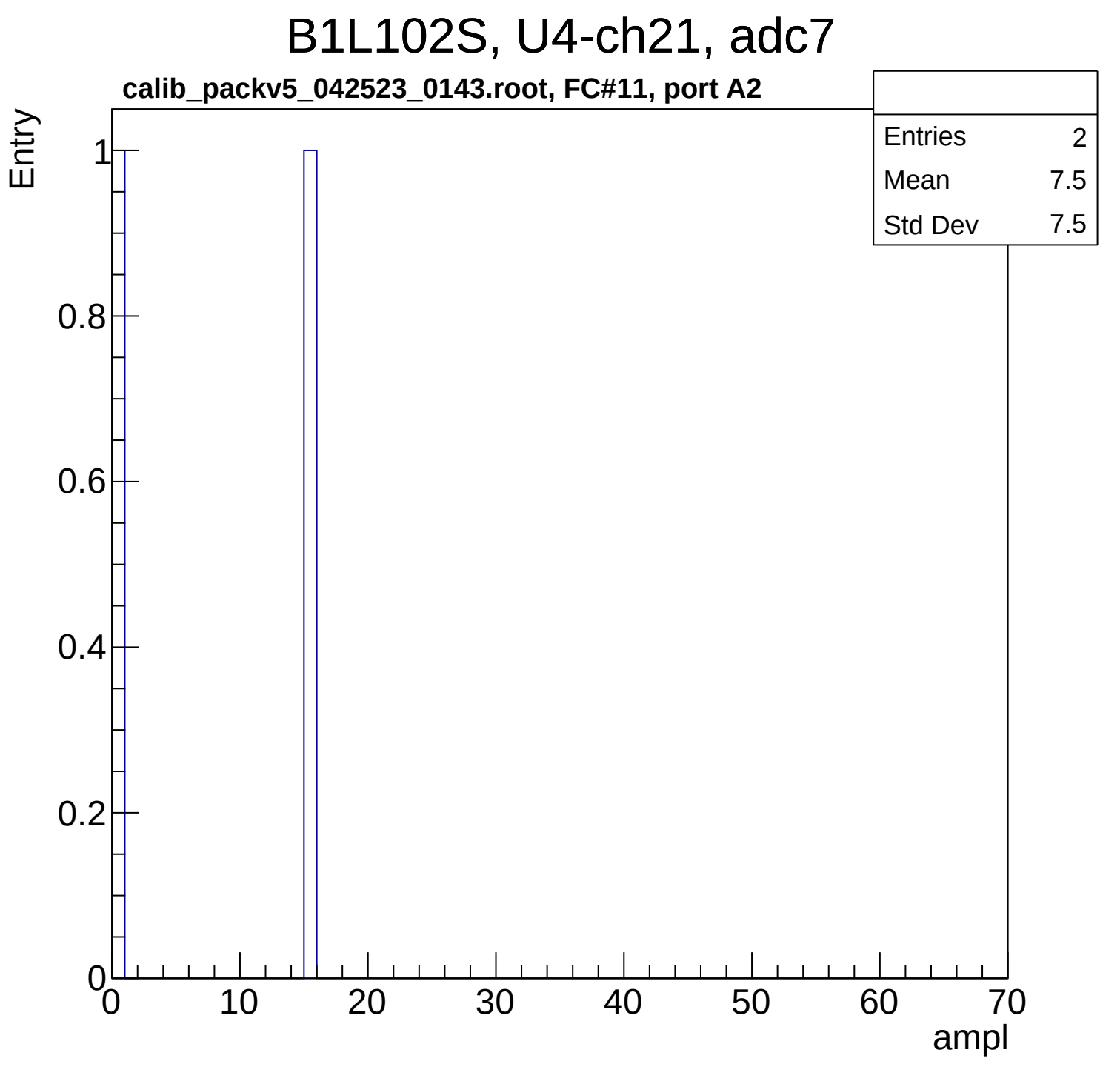
B1L102S, U4-ch21, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 7.5
Std Dev 7.5
Entry
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0.6
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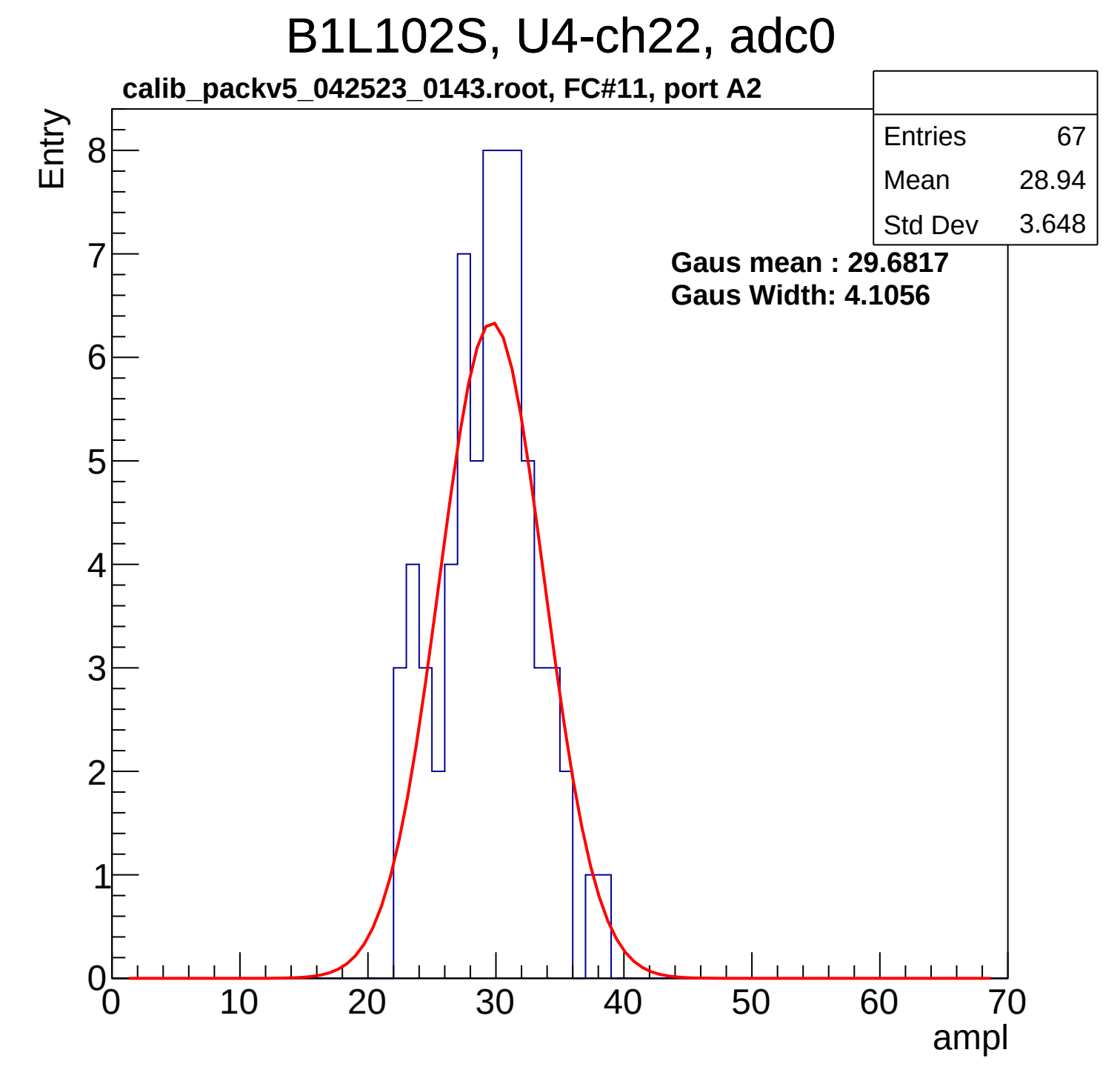
50
60
70
ampl


B1L102S, U4-ch22, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 28.94
Std Dev 3.648
Gaus mean : 29.6817
Gaus Width: 4.1056
Entry
ampl
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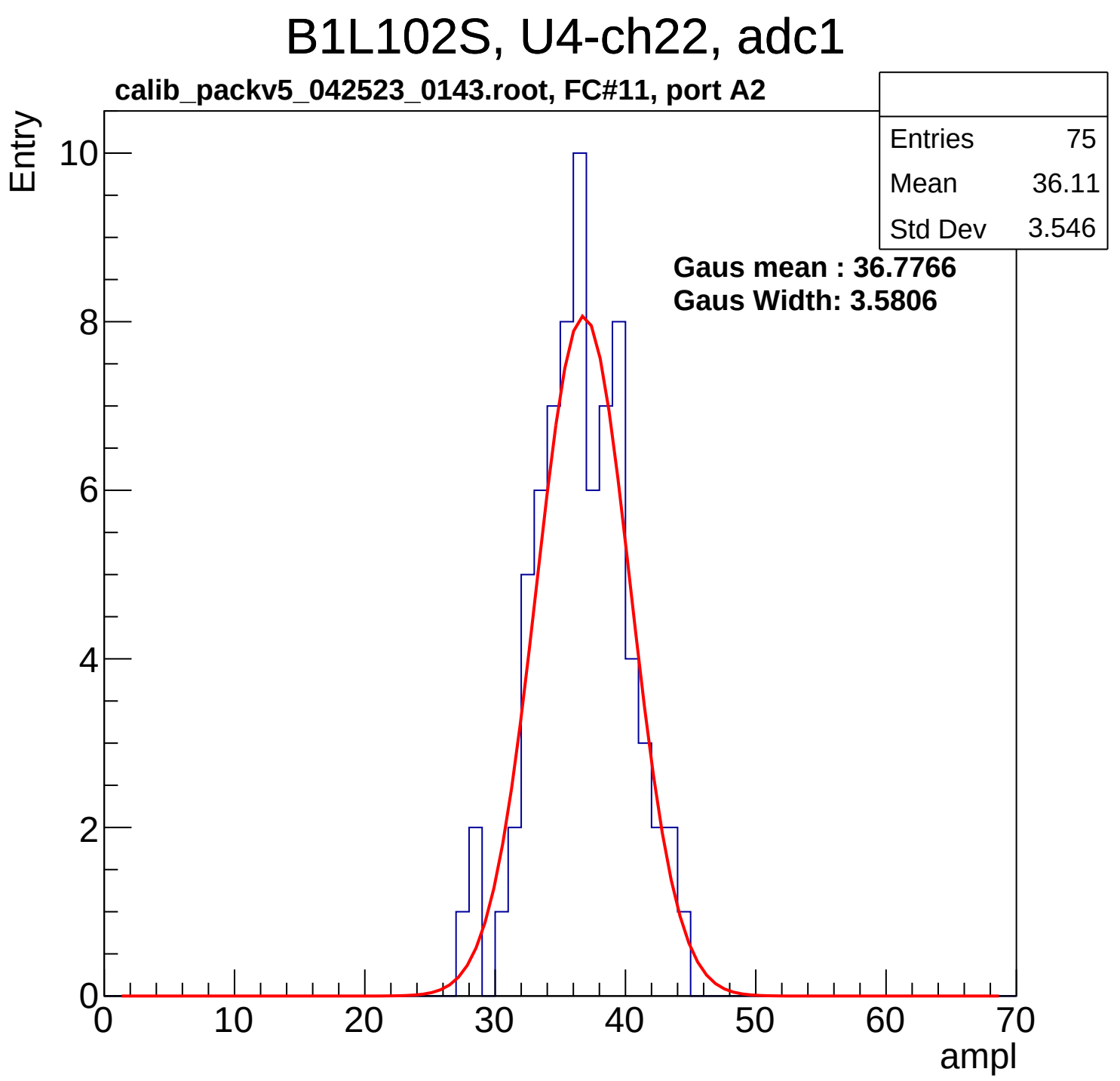
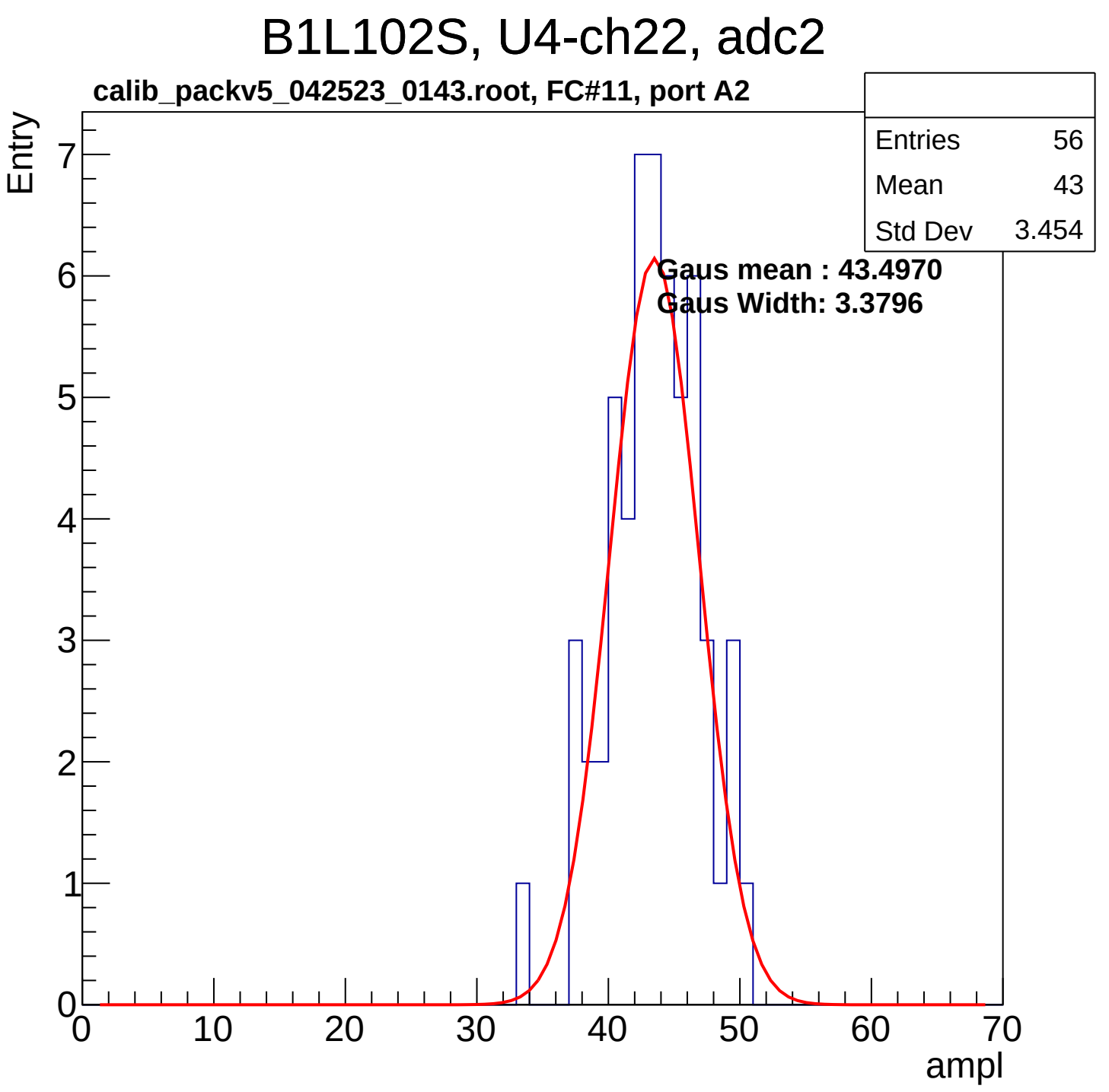
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch22, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 36.11
Std Dev 3.546
Gaus mean : 36.7766
Gaus Width: 3.5806
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch22, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 43
Std Dev 3.454
Gaus mean : 43.4970
Gaus Width: 3.3796
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
30
40
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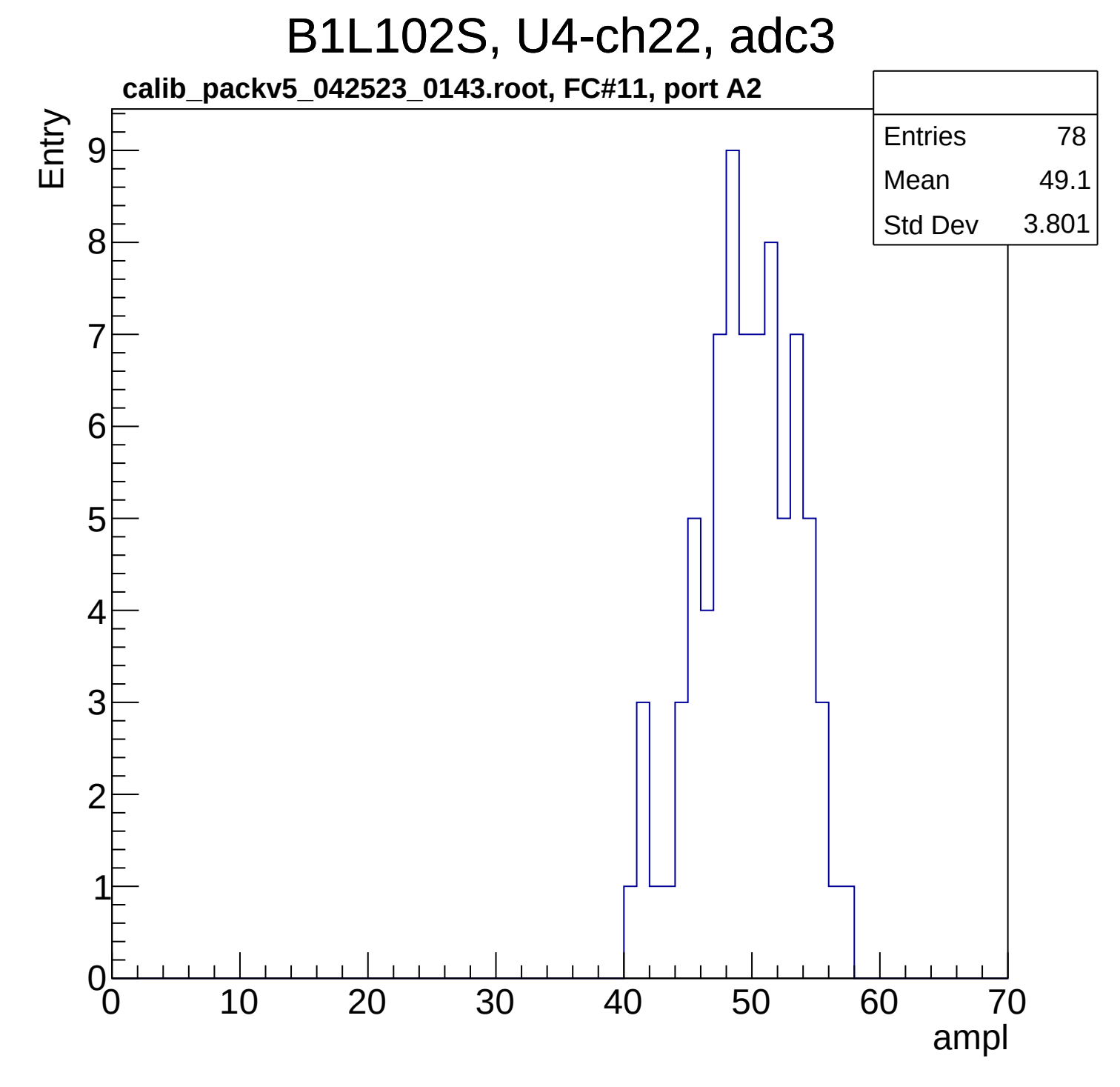
60
70


B1L102S, U4-ch22, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 78
Mean 49.1
Std Dev 3.801
Entry
ampl
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3
4
5
6
7
8
9
0
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60
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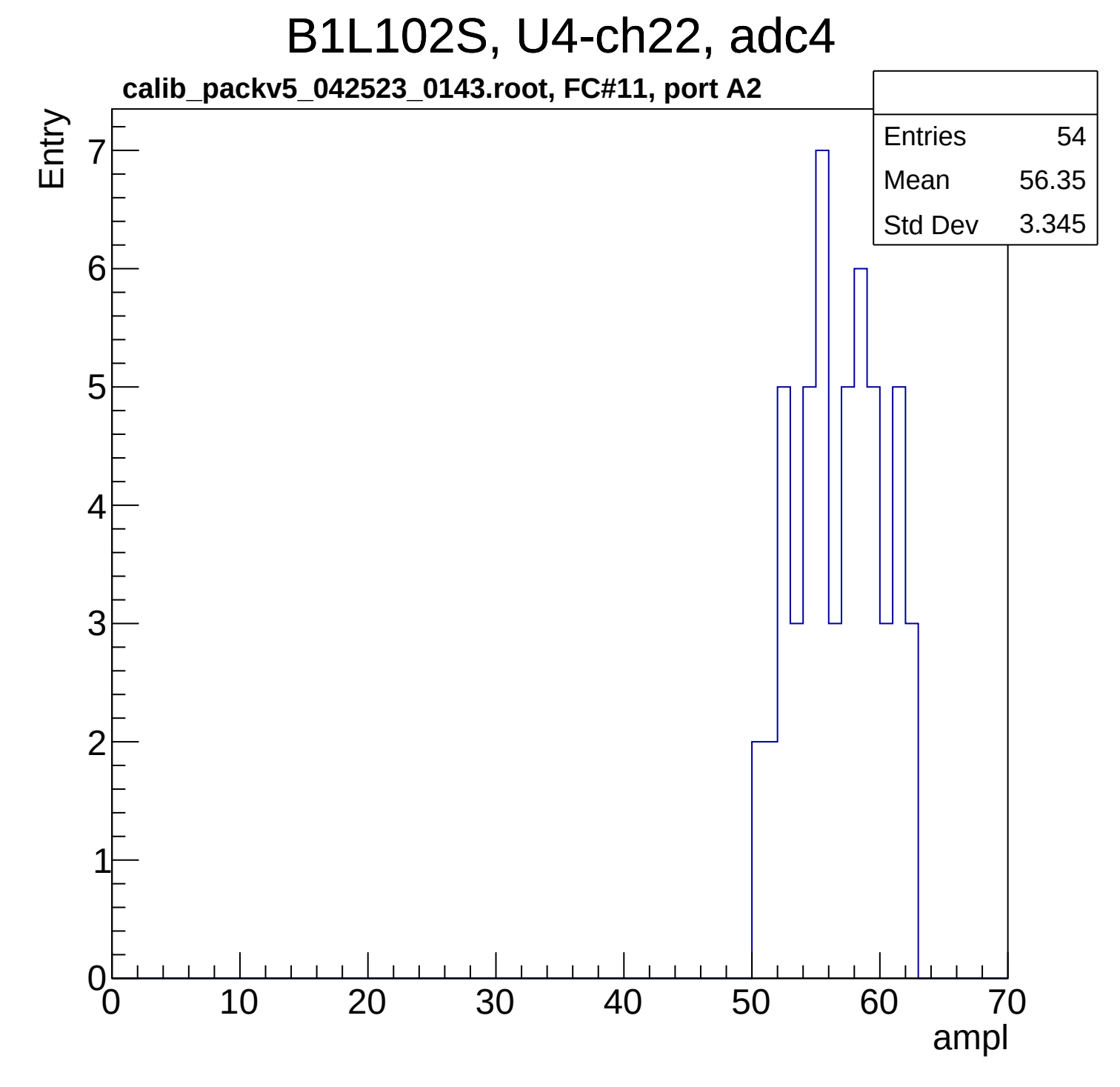
B1L102S, U4-ch22, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 56.35
Std Dev 3.345
Entry
ampl
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1
2
3
4
5
6
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0
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60
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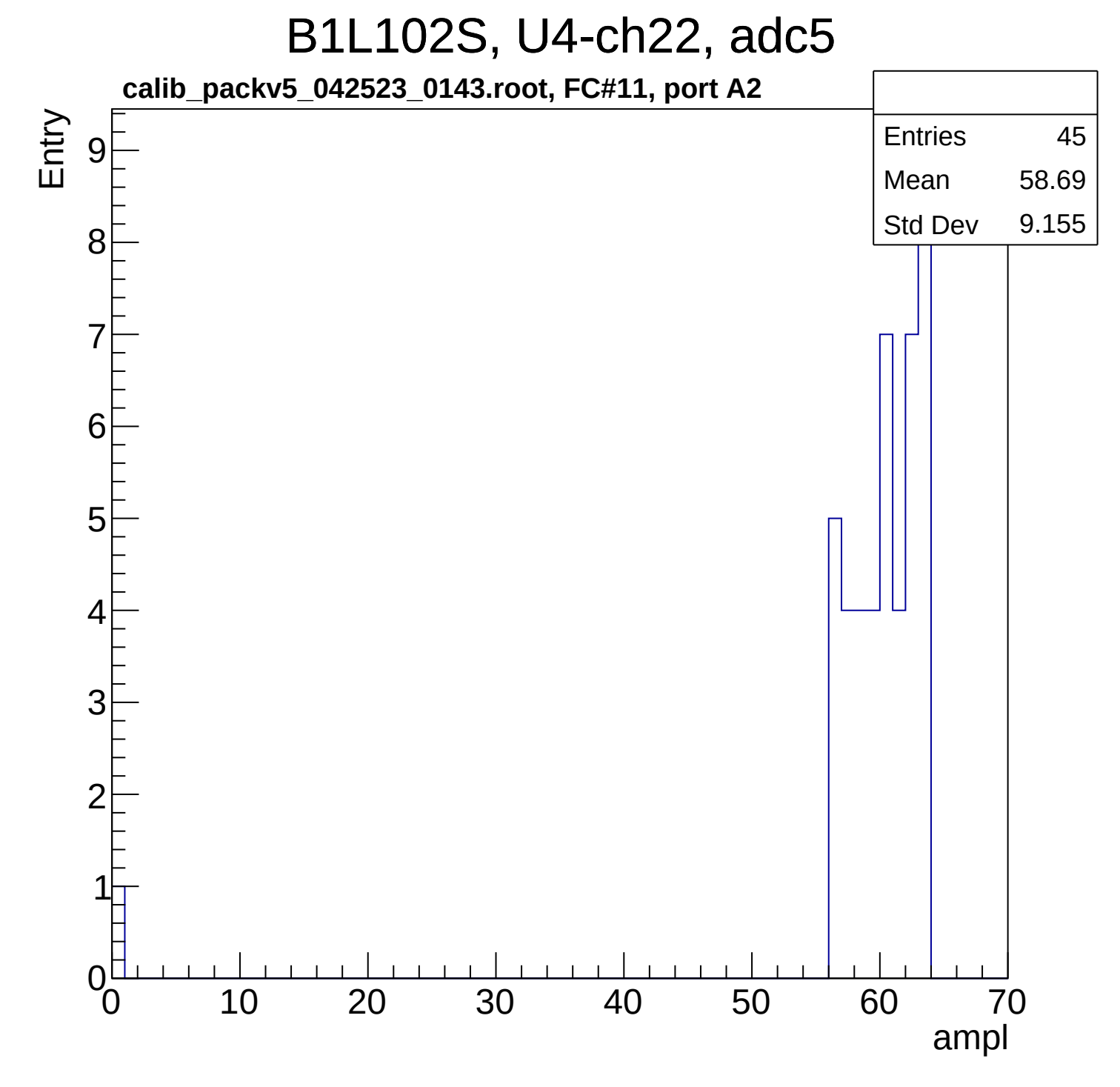
B1L102S, U4-ch22, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 45
Mean 58.69
Std Dev 9.155
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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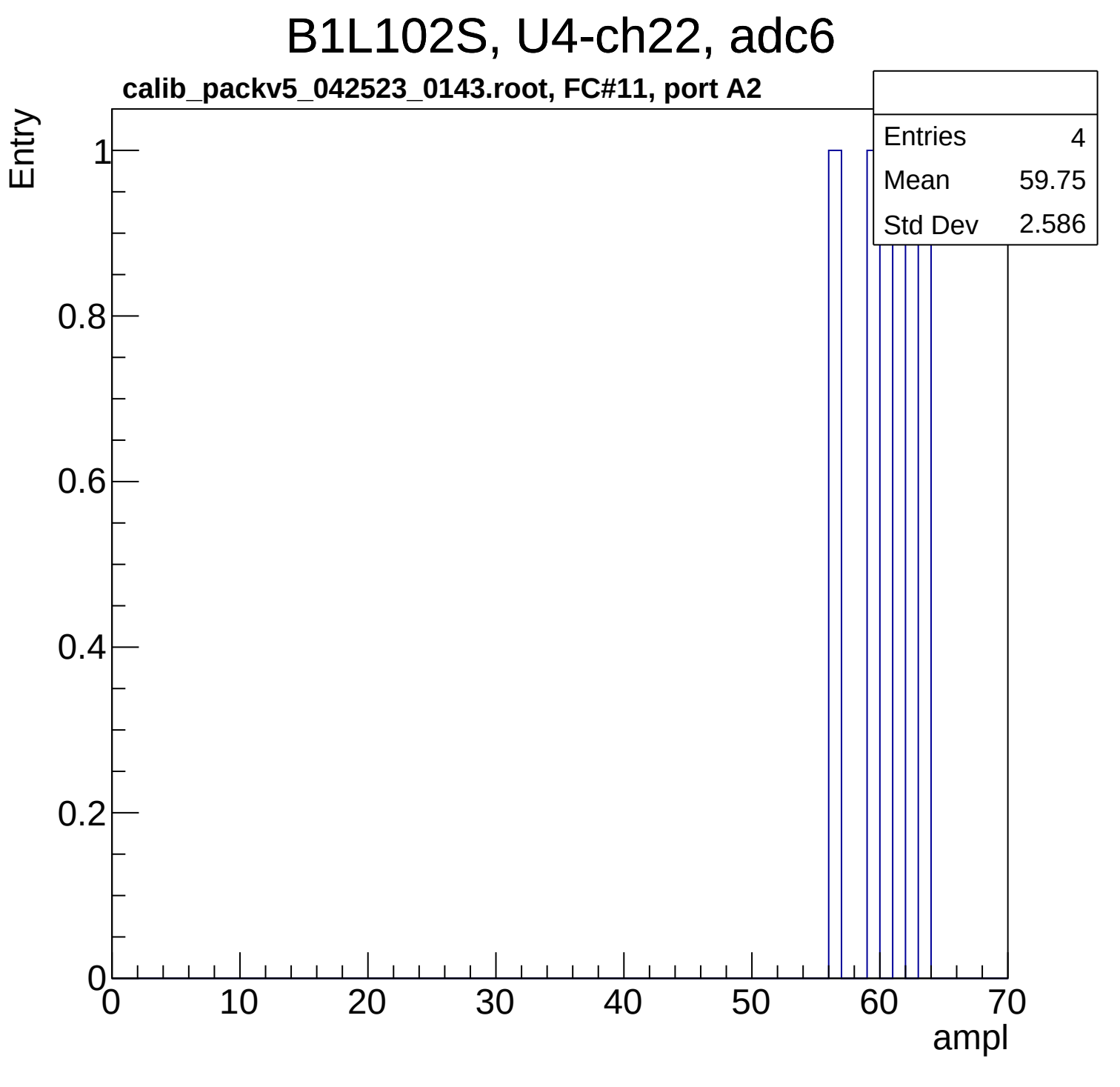
B1L102S, U4-ch22, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 4
Mean 59.75
Std Dev 2.586
Entry
ampl
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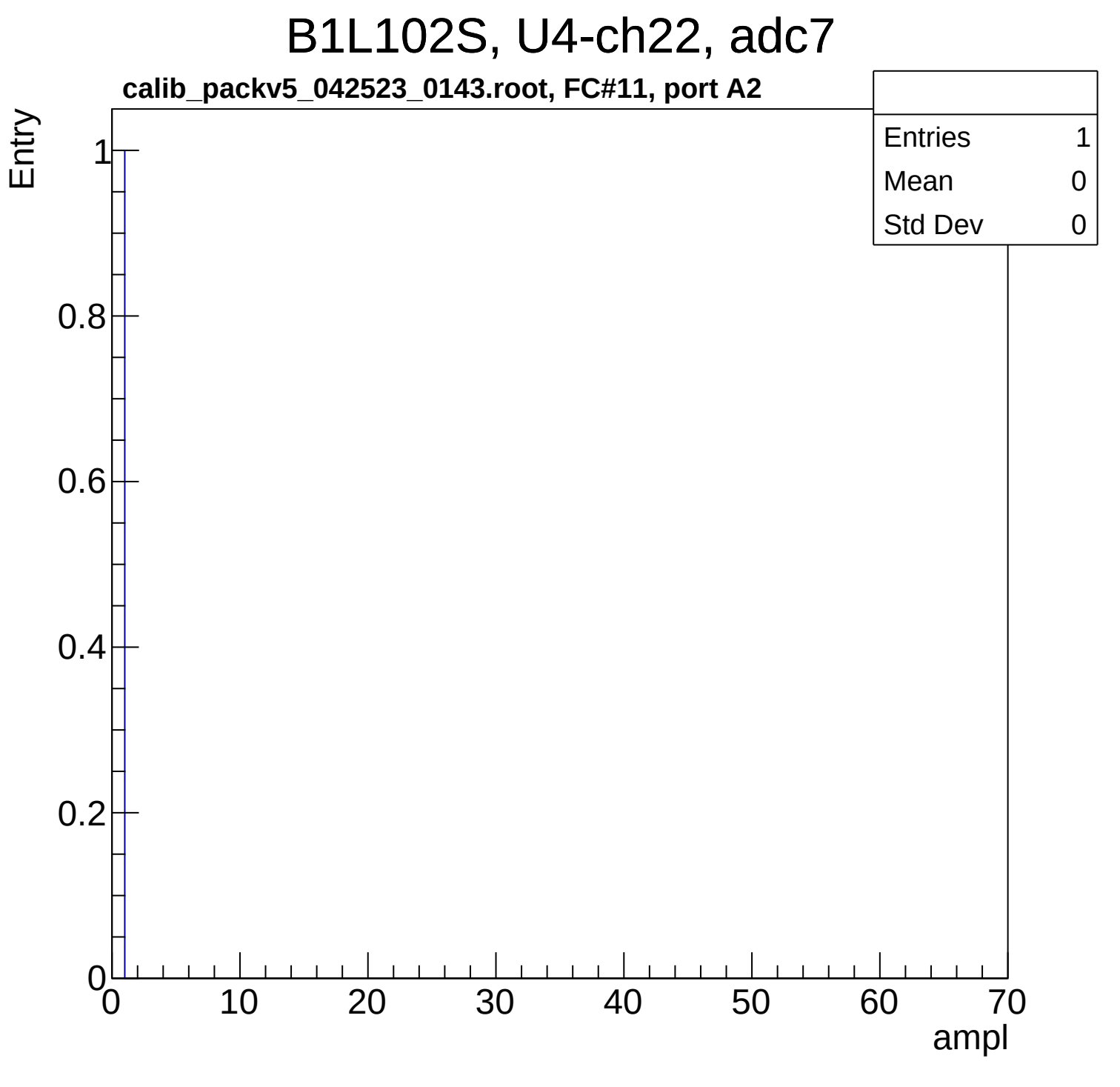
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L102S, U4-ch22, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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0.6
0.4
0.2
0
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10
20
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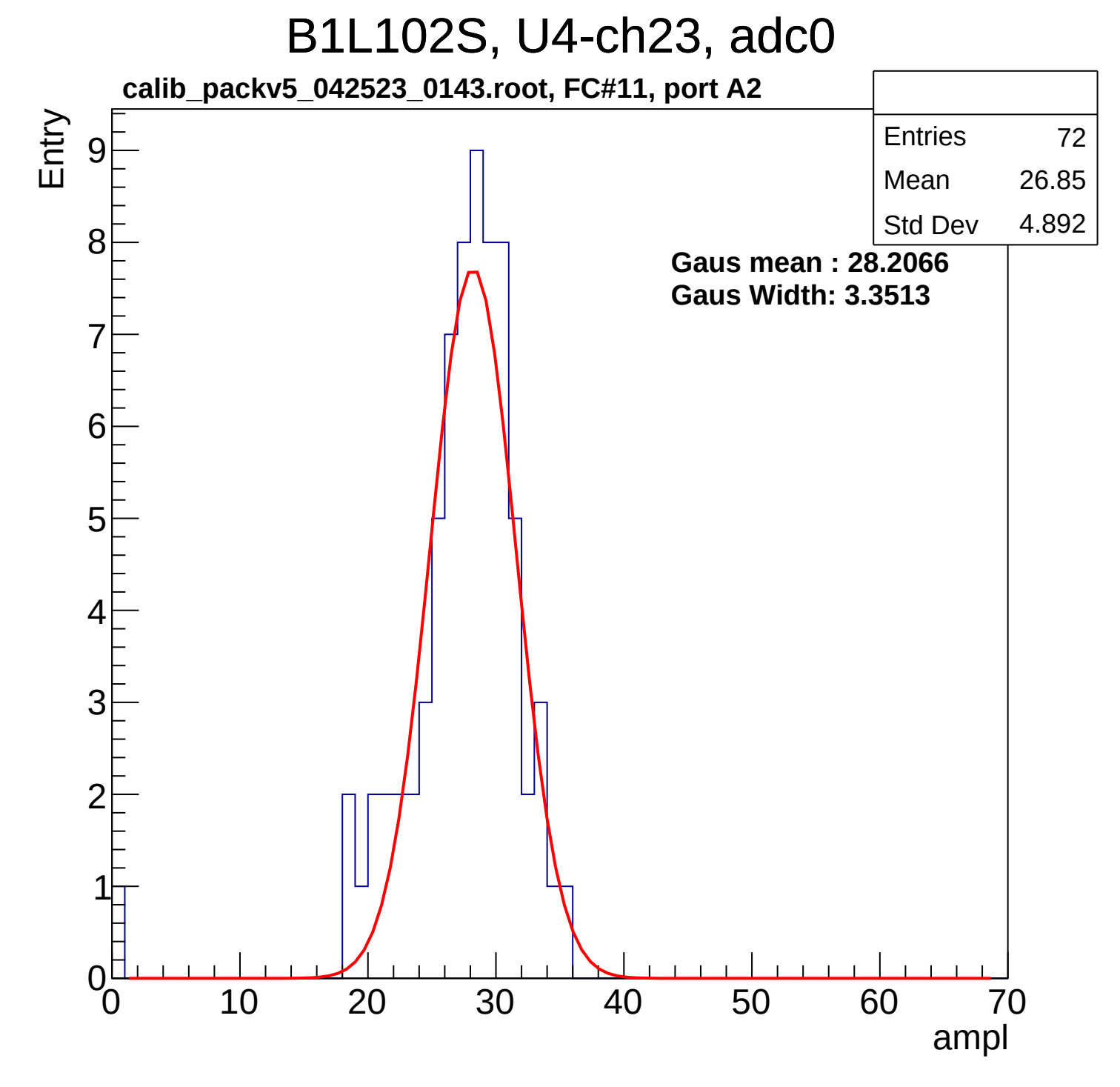
50
60
70
ampl


B1L102S, U4-ch23, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 72
Mean 26.85
Std Dev 4.892
Gaus mean : 28.2066
Gaus Width: 3.3513
Entry
ampl
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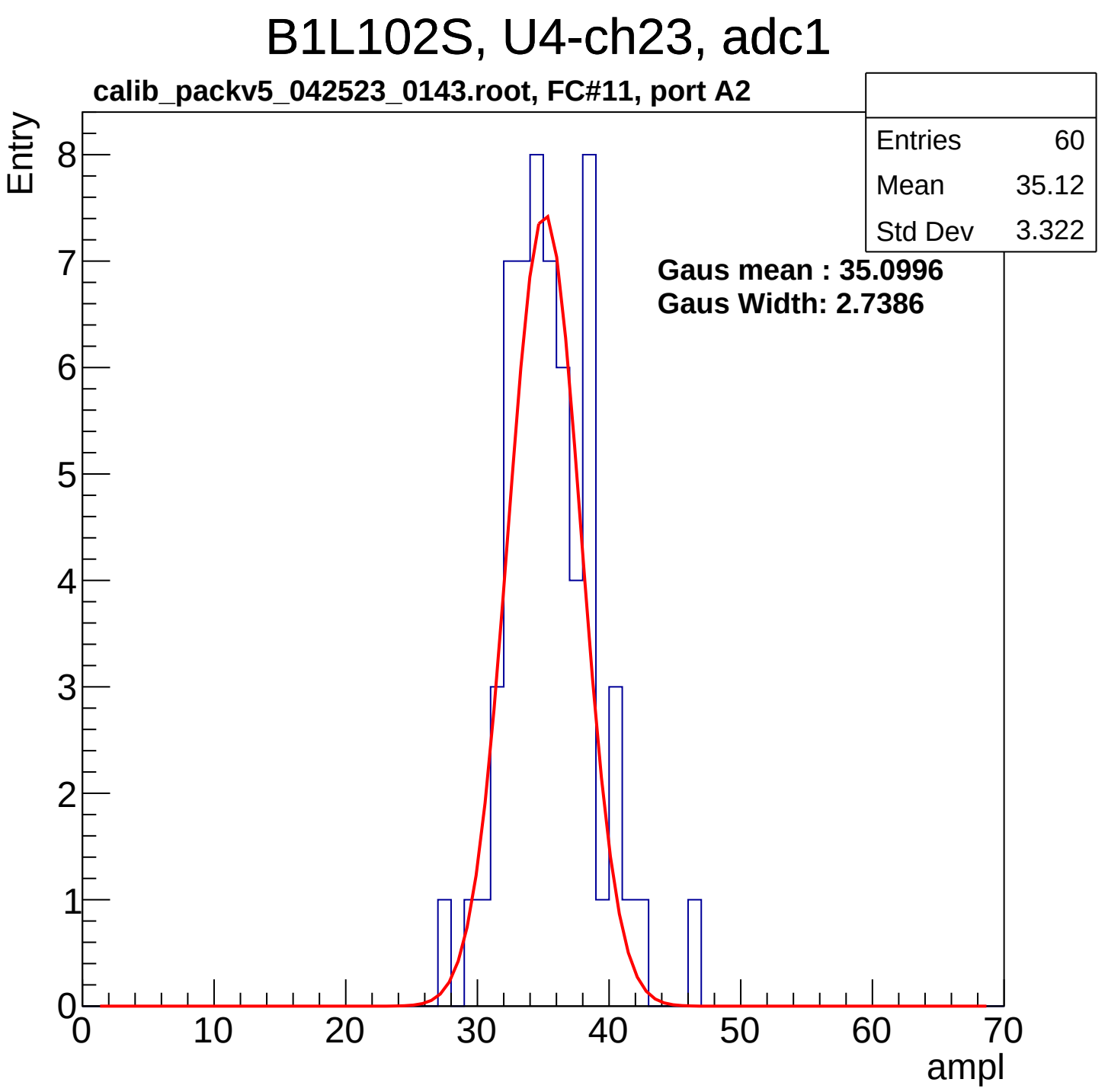
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L102S, U4-ch23, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 35.12
Std Dev 3.322
Gaus mean : 35.0996
Gaus Width: 2.7386
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
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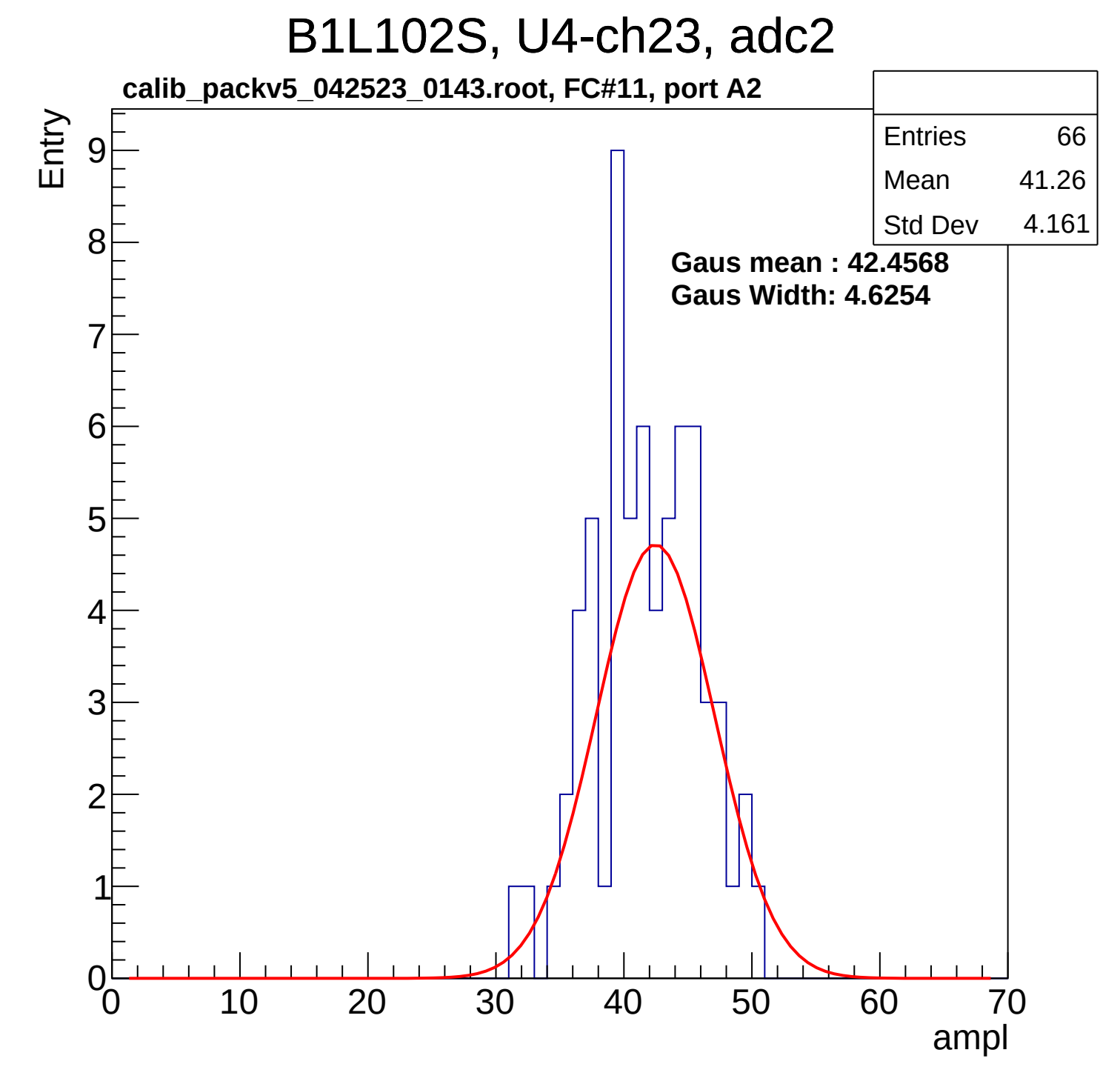
B1L102S, U4-ch23, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 41.26
Std Dev 4.161
Gaus mean : 42.4568
Gaus Width: 4.6254
Entry
ampl
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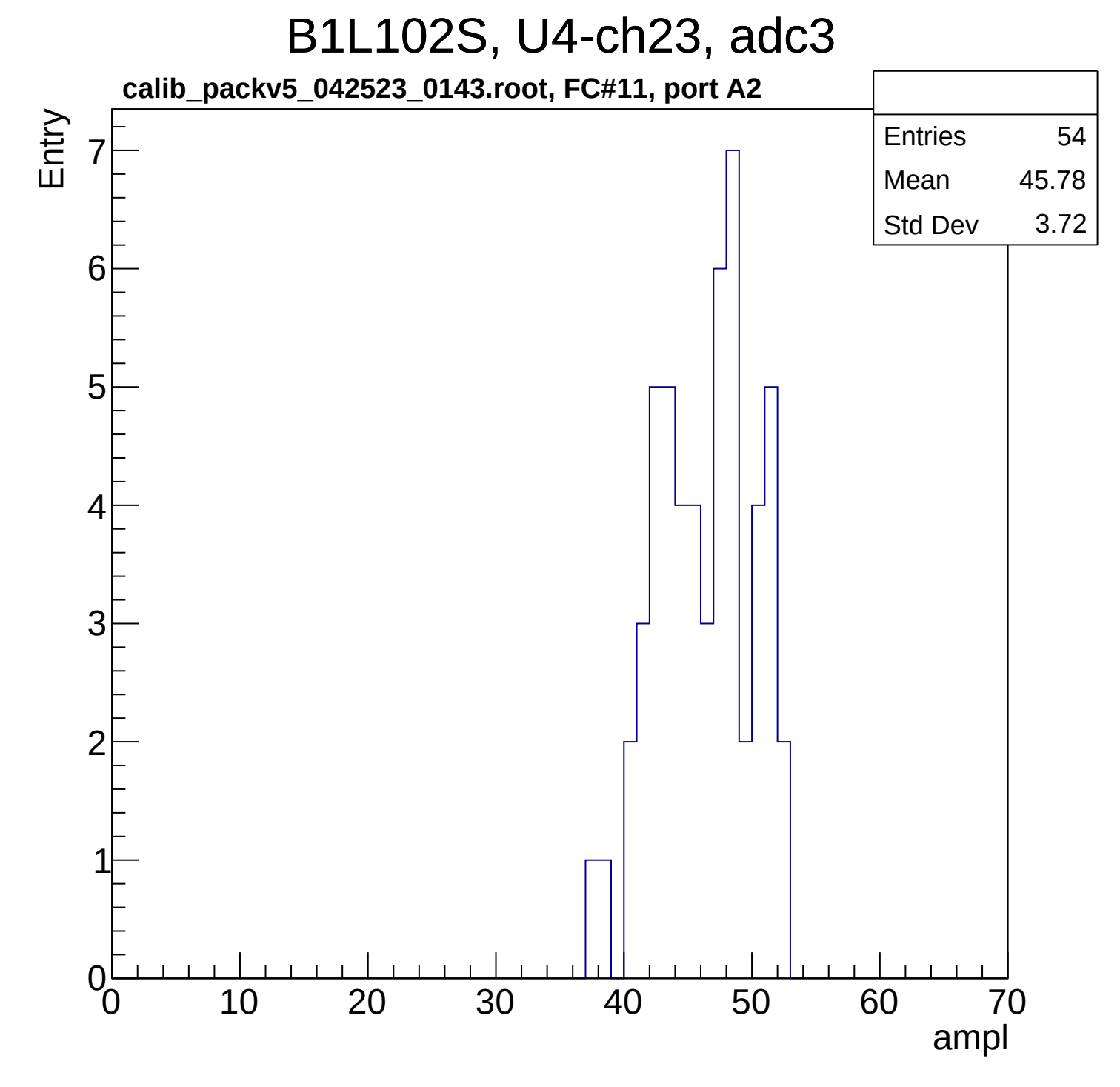
B1L102S, U4-ch23, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 45.78
Std Dev 3.72
Entry
ampl
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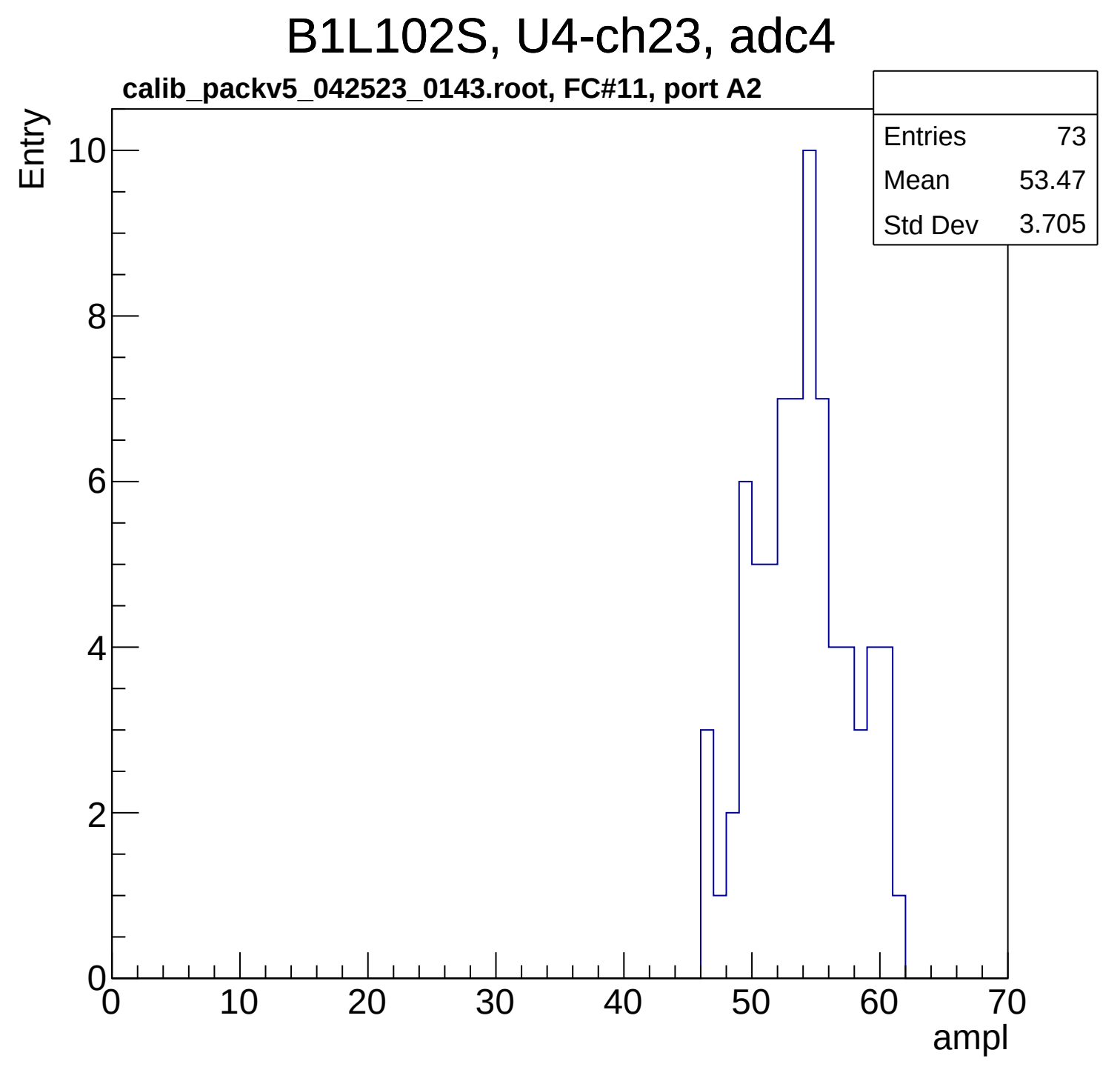
B1L102S, U4-ch23, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 53.47
Std Dev 3.705
Entry
ampl
0
2
4
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8
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0
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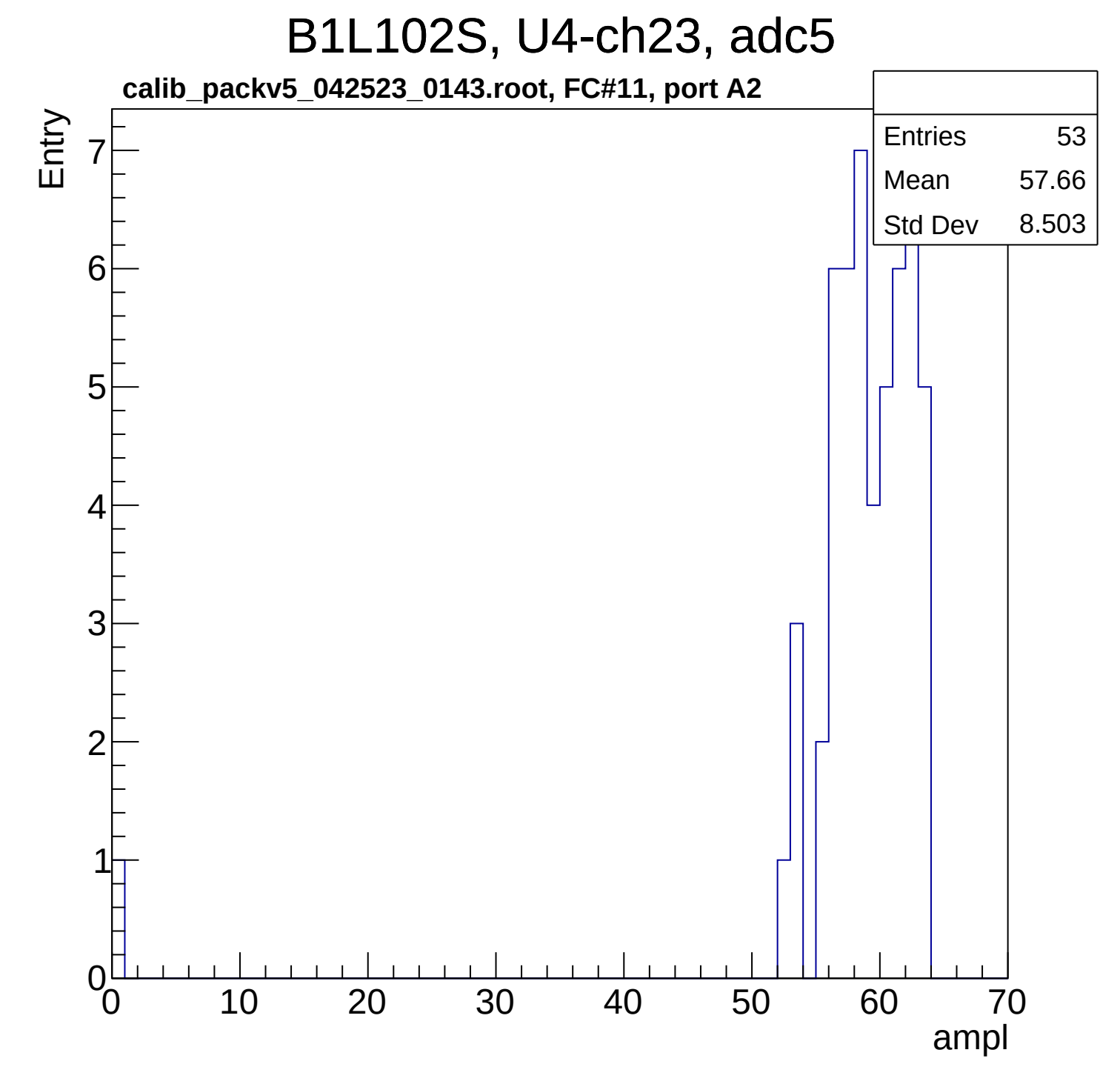
B1L102S, U4-ch23, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 57.66
Std Dev 8.503
Entry
ampl
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3
4
5
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0
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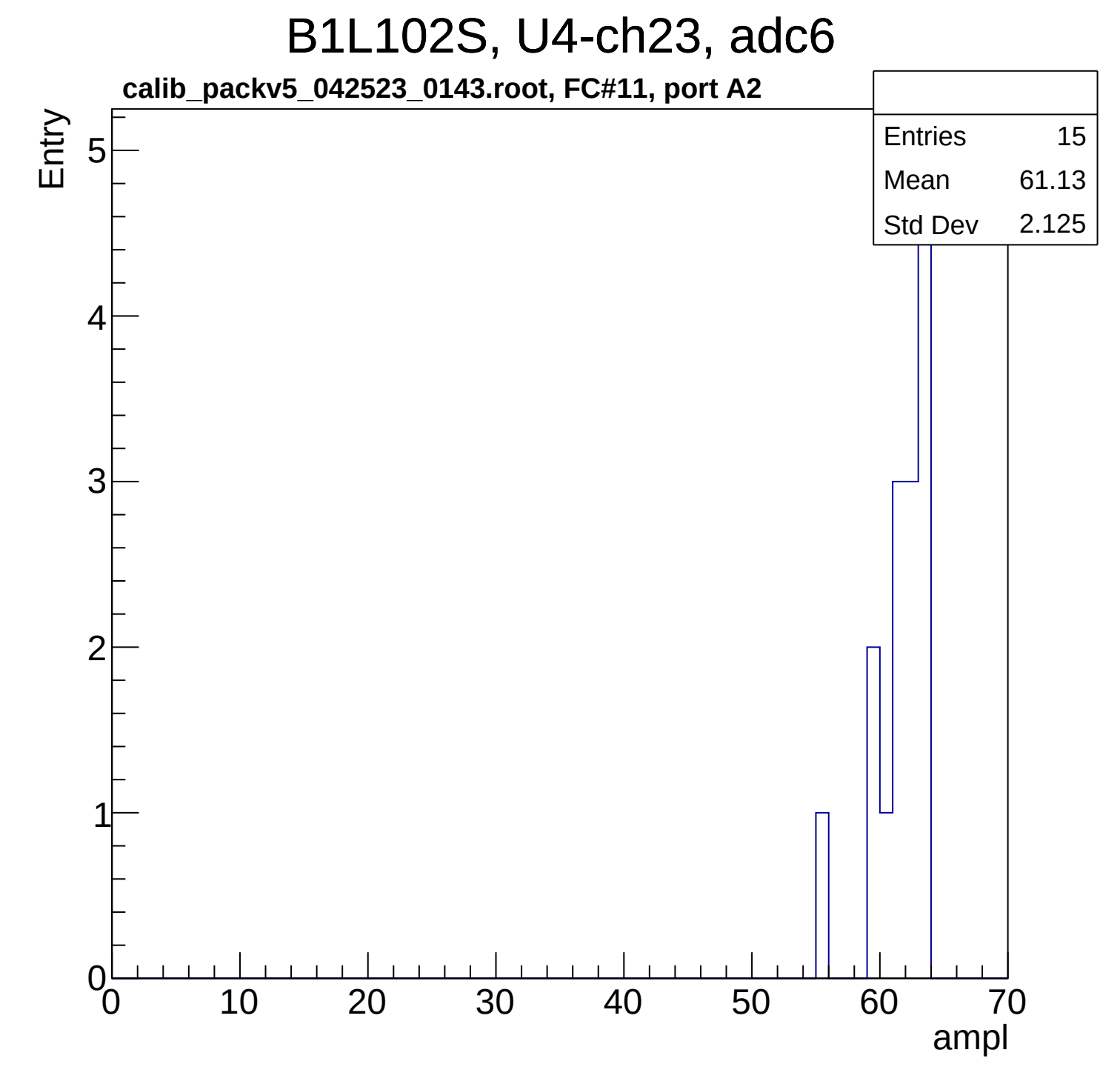
B1L102S, U4-ch23, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 15
Mean 61.13
Std Dev 2.125
Entry
ampl
0
1
2
3
4
5
0
10
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40
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60
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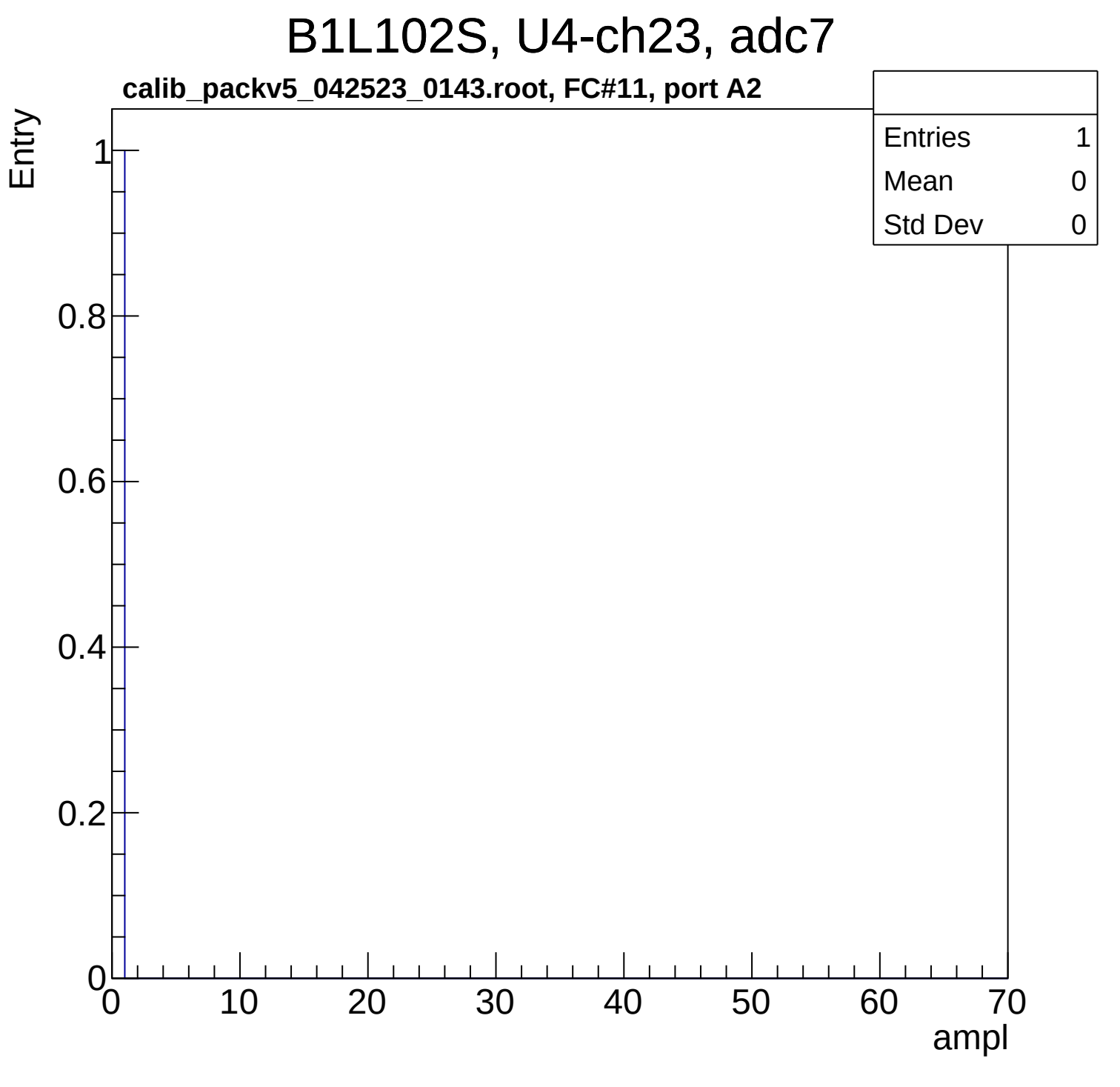
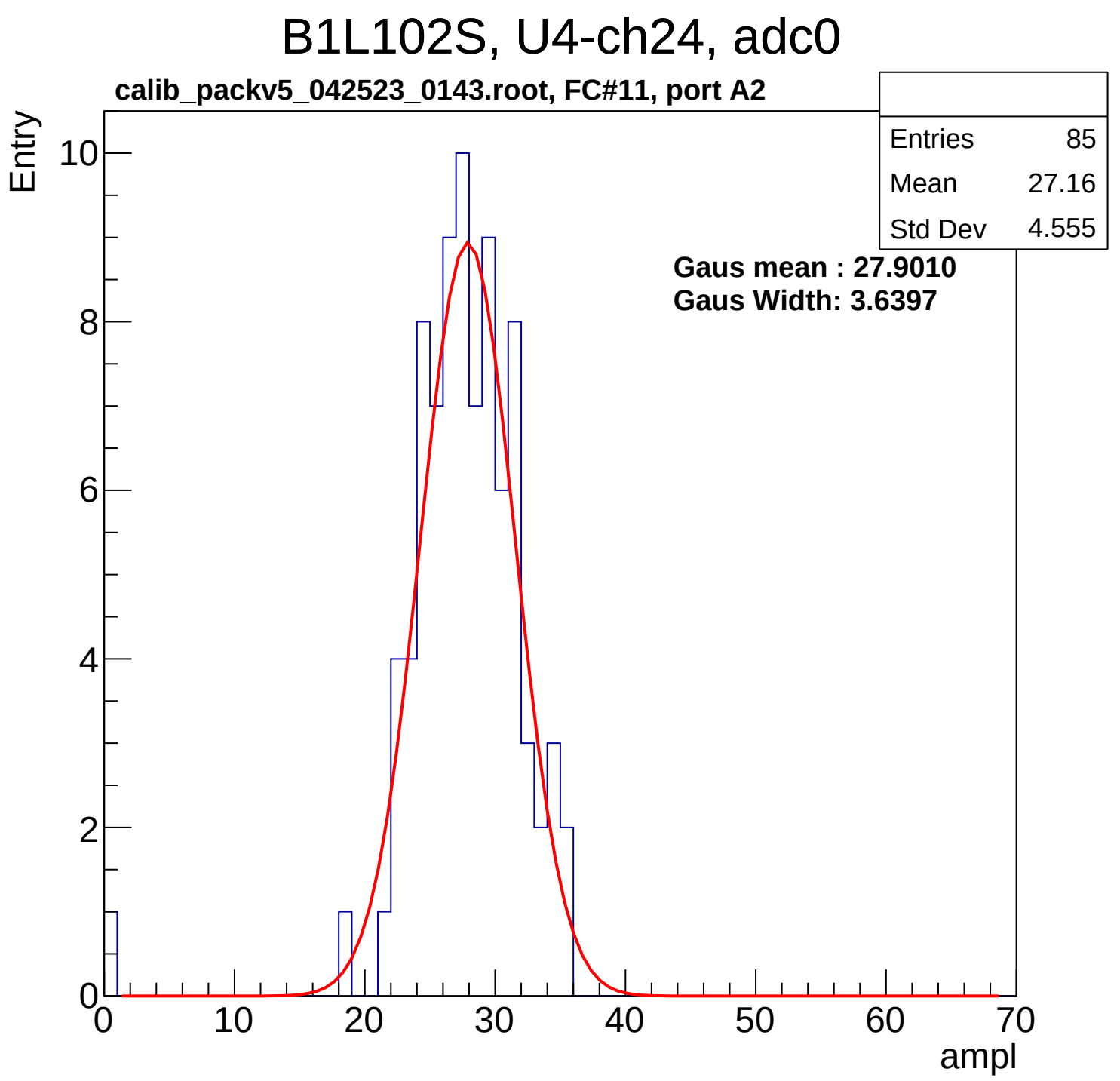
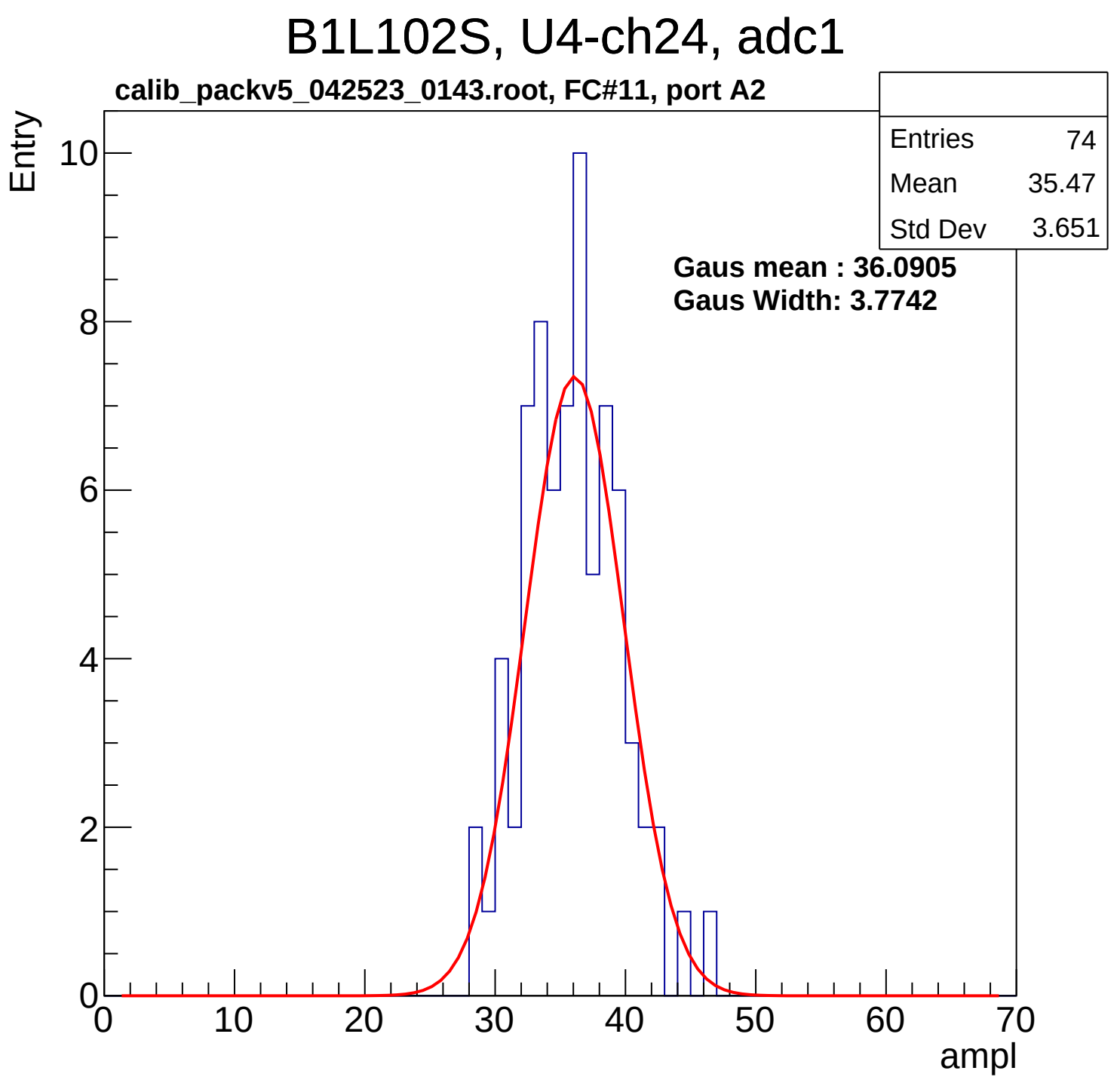

B1L102S, U4-ch23, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch24, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 85
Mean 27.16
Std Dev 4.555
Gaus mean : 27.9010
Gaus Width: 3.6397
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch24, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 35.47
Std Dev 3.651
Gaus mean : 36.0905
Gaus Width: 3.7742
Entry
ampl
0
2
4
6
8
10
0
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20
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40
50
60
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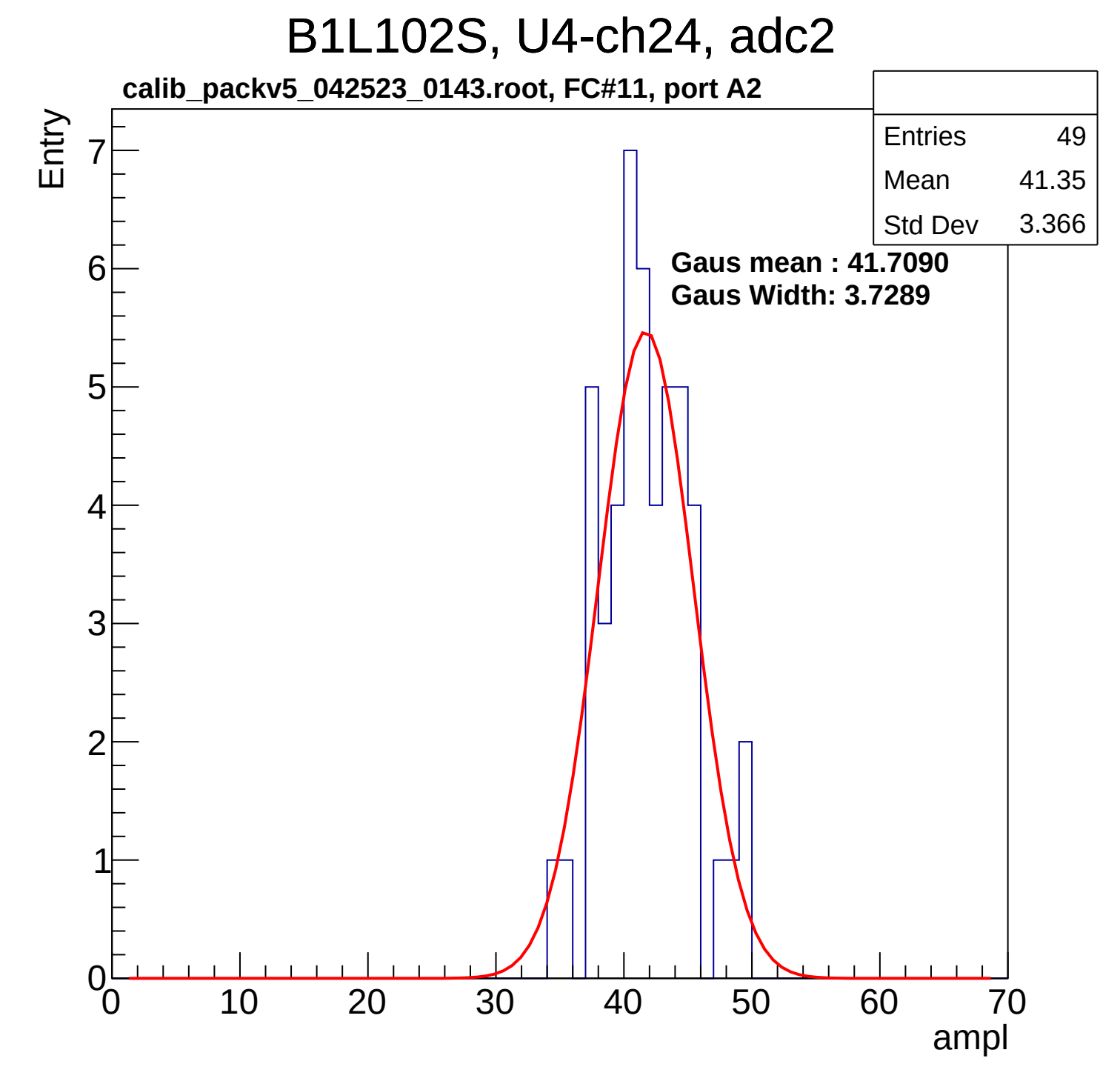
B1L102S, U4-ch24, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 41.35
Std Dev 3.366
Gaus mean : 41.7090
Gaus Width: 3.7289
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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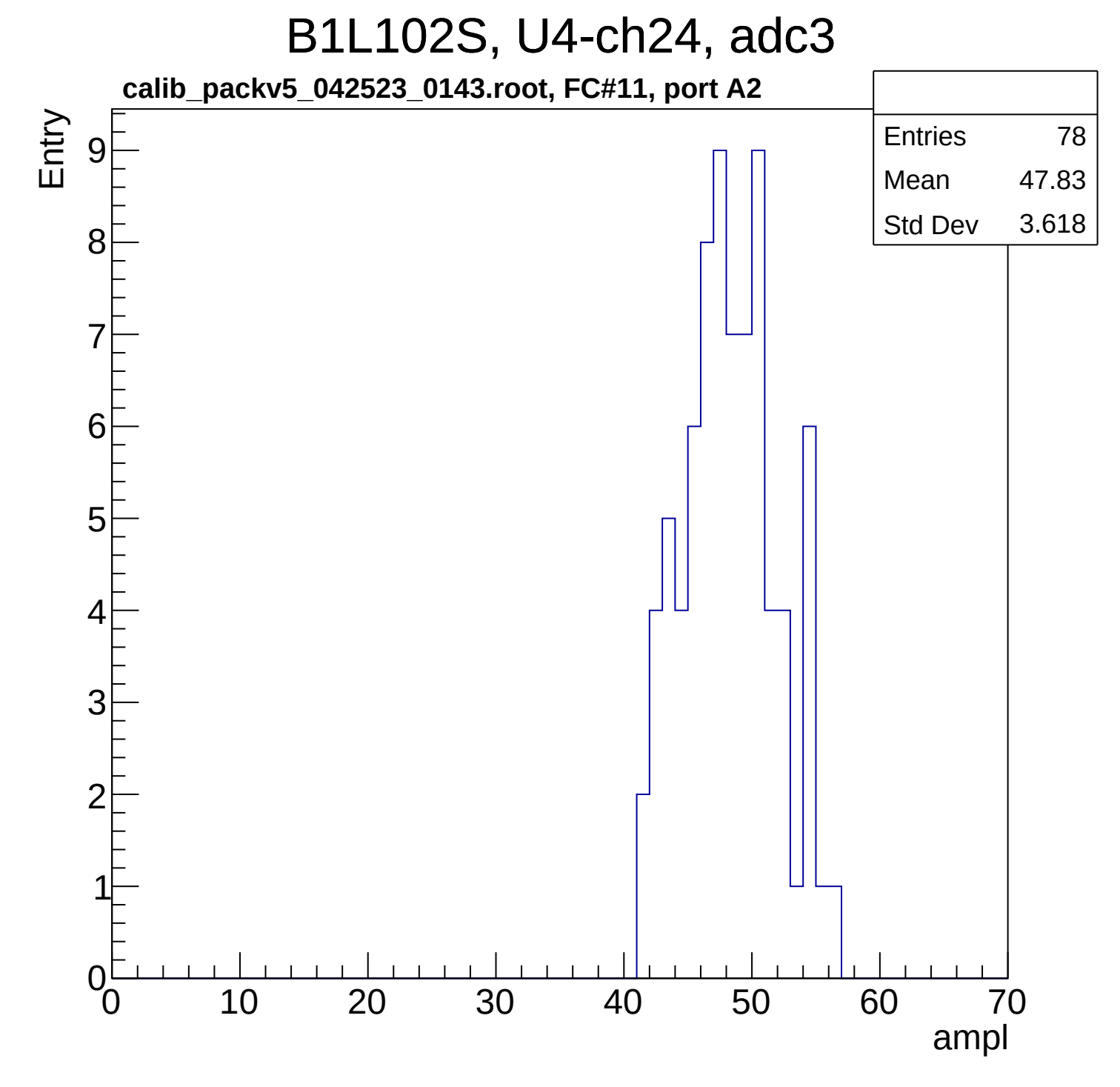
B1L102S, U4-ch24, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 78
Mean 47.83
Std Dev 3.618
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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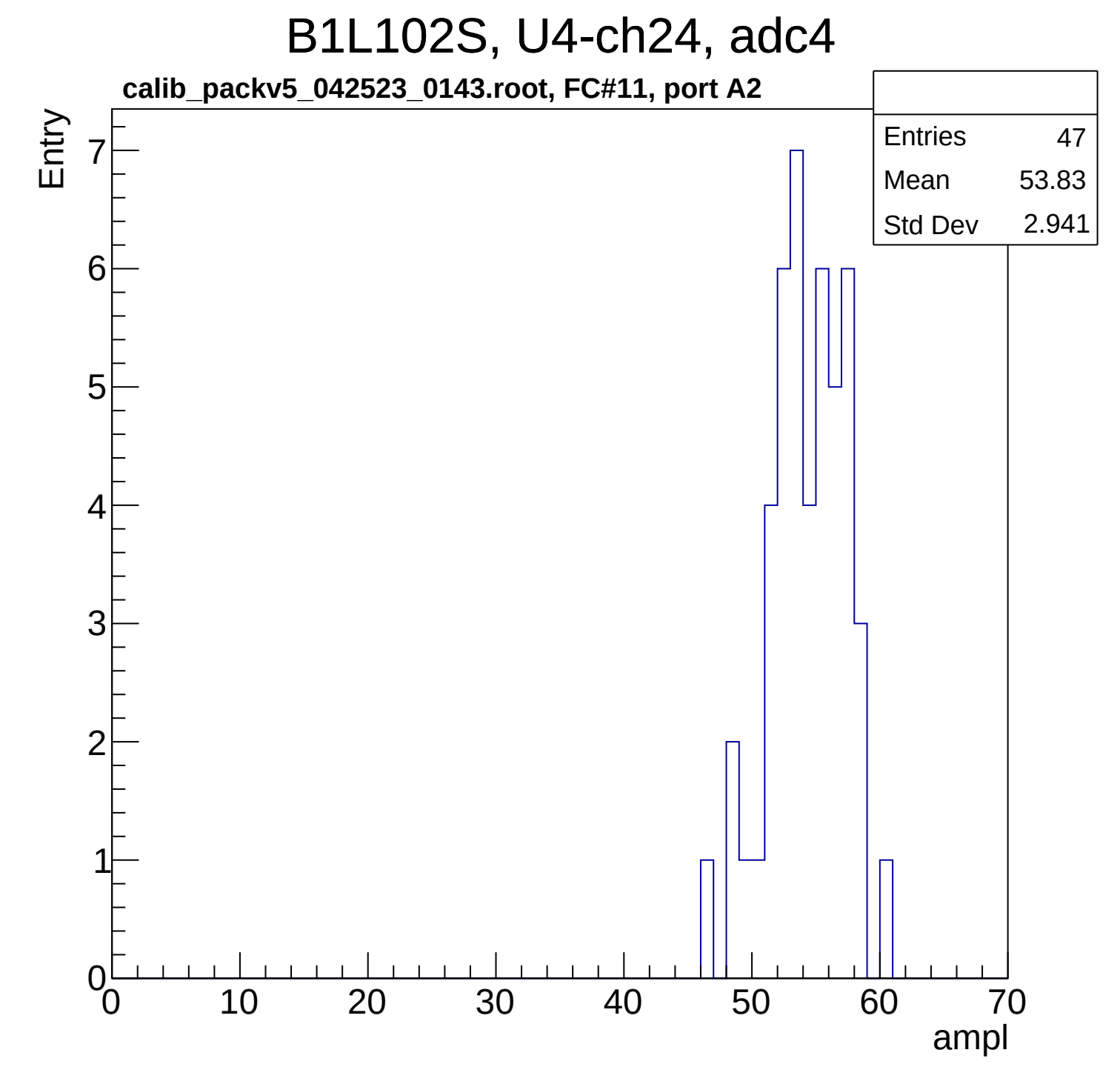
B1L102S, U4-ch24, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 47
Mean 53.83
Std Dev 2.941
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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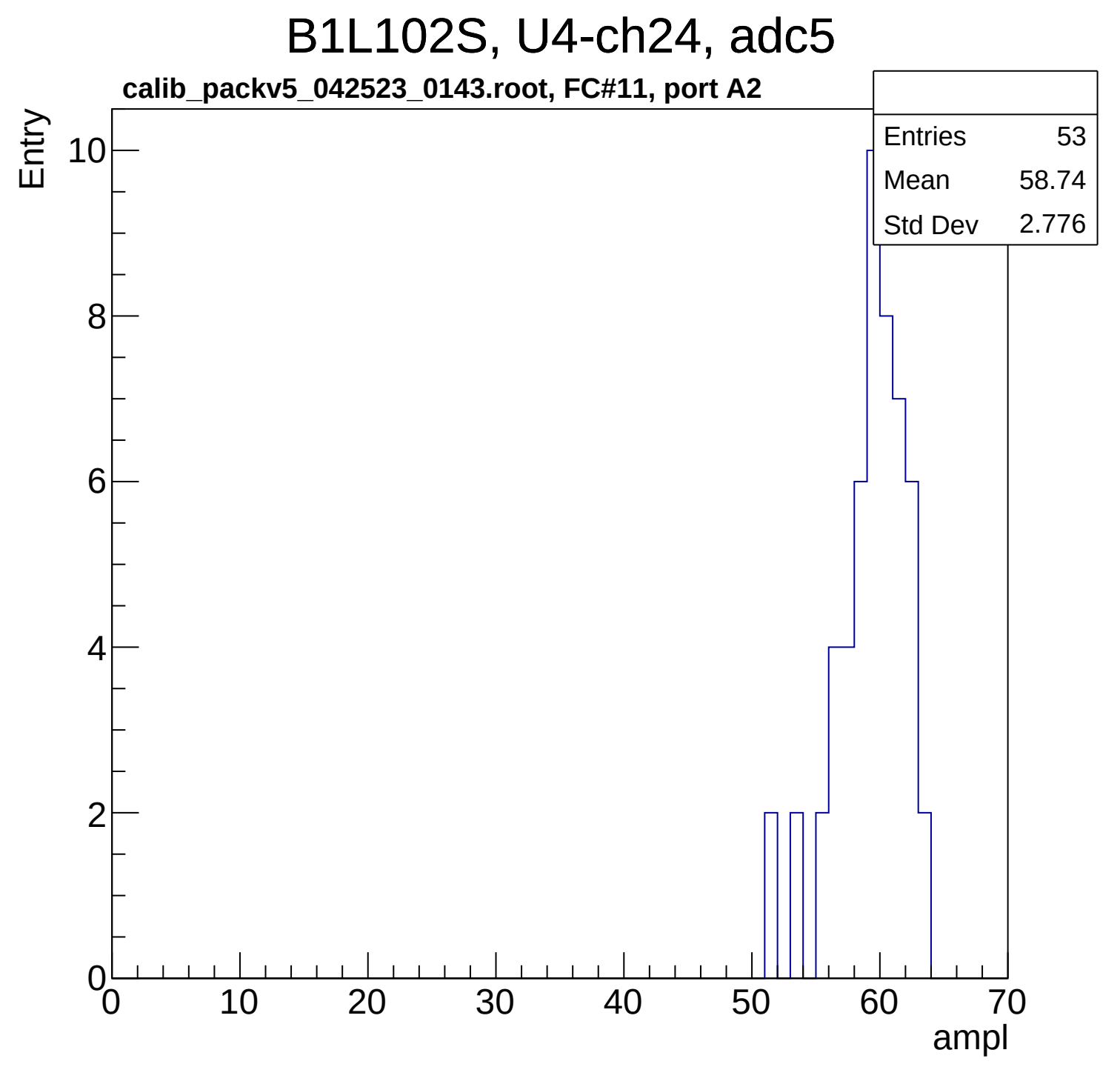
B1L102S, U4-ch24, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 58.74
Std Dev 2.776
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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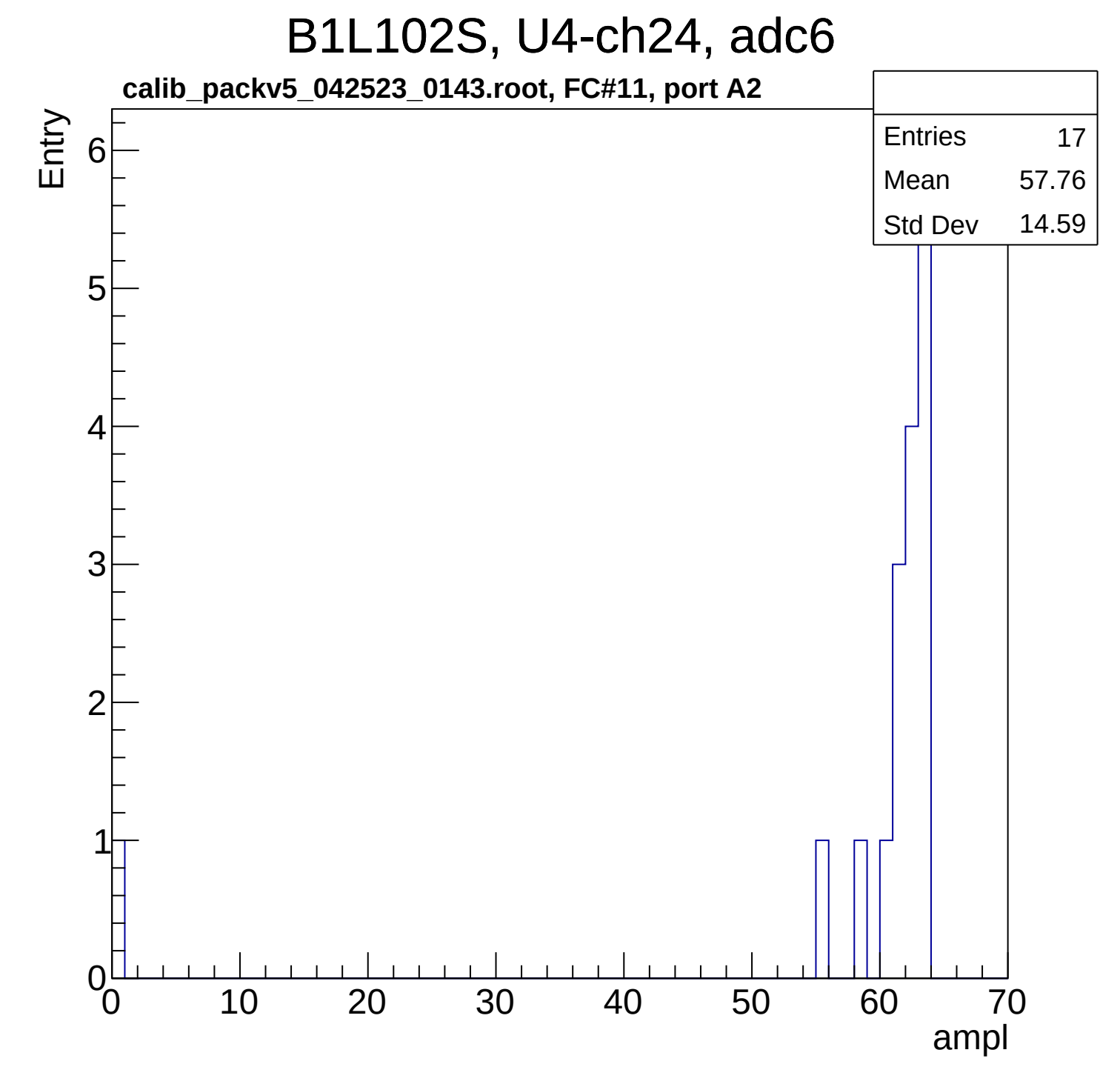
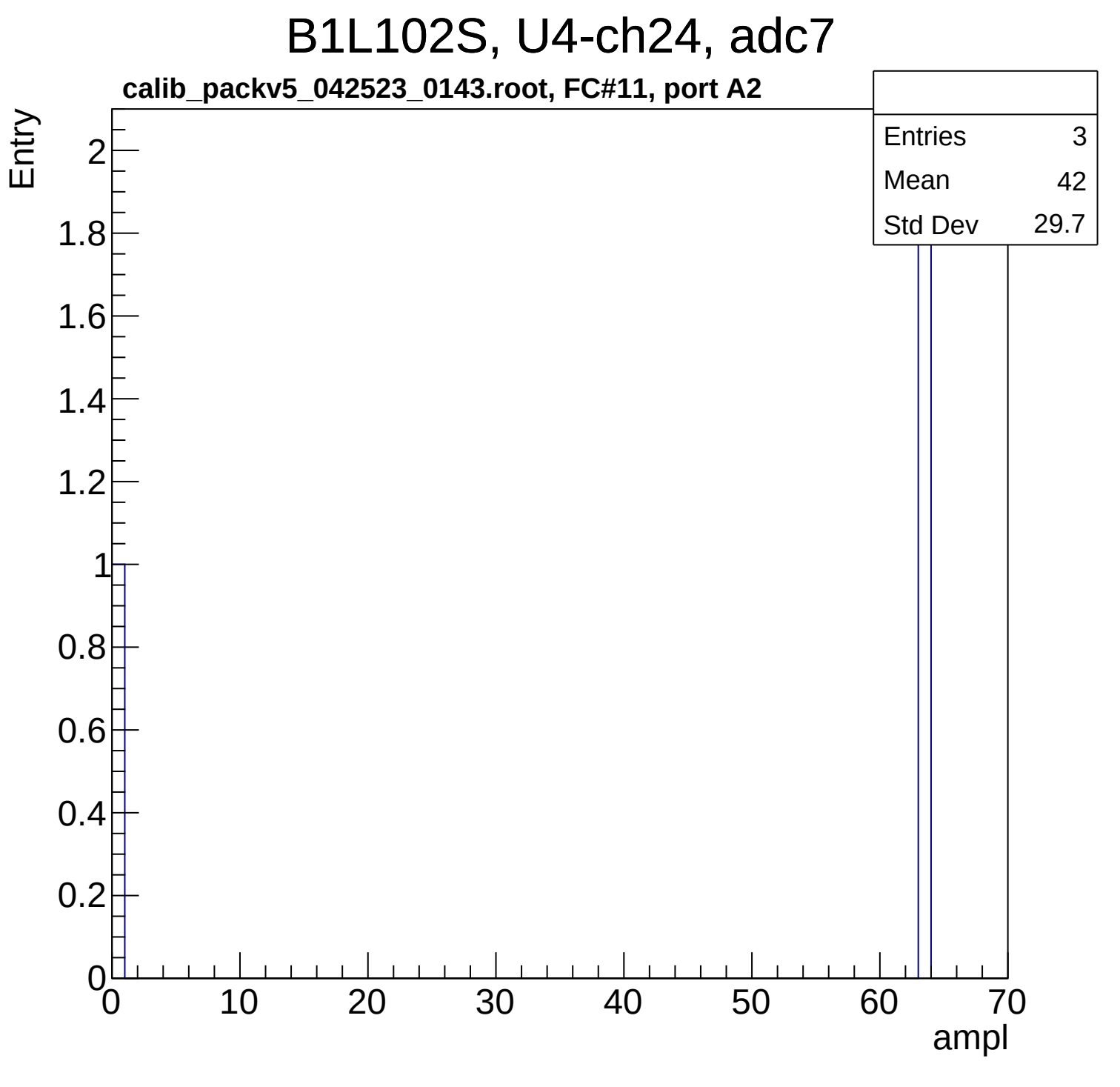

B1L102S, U4-ch24, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 17
Mean 57.76
Std Dev 14.59
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch24, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 42
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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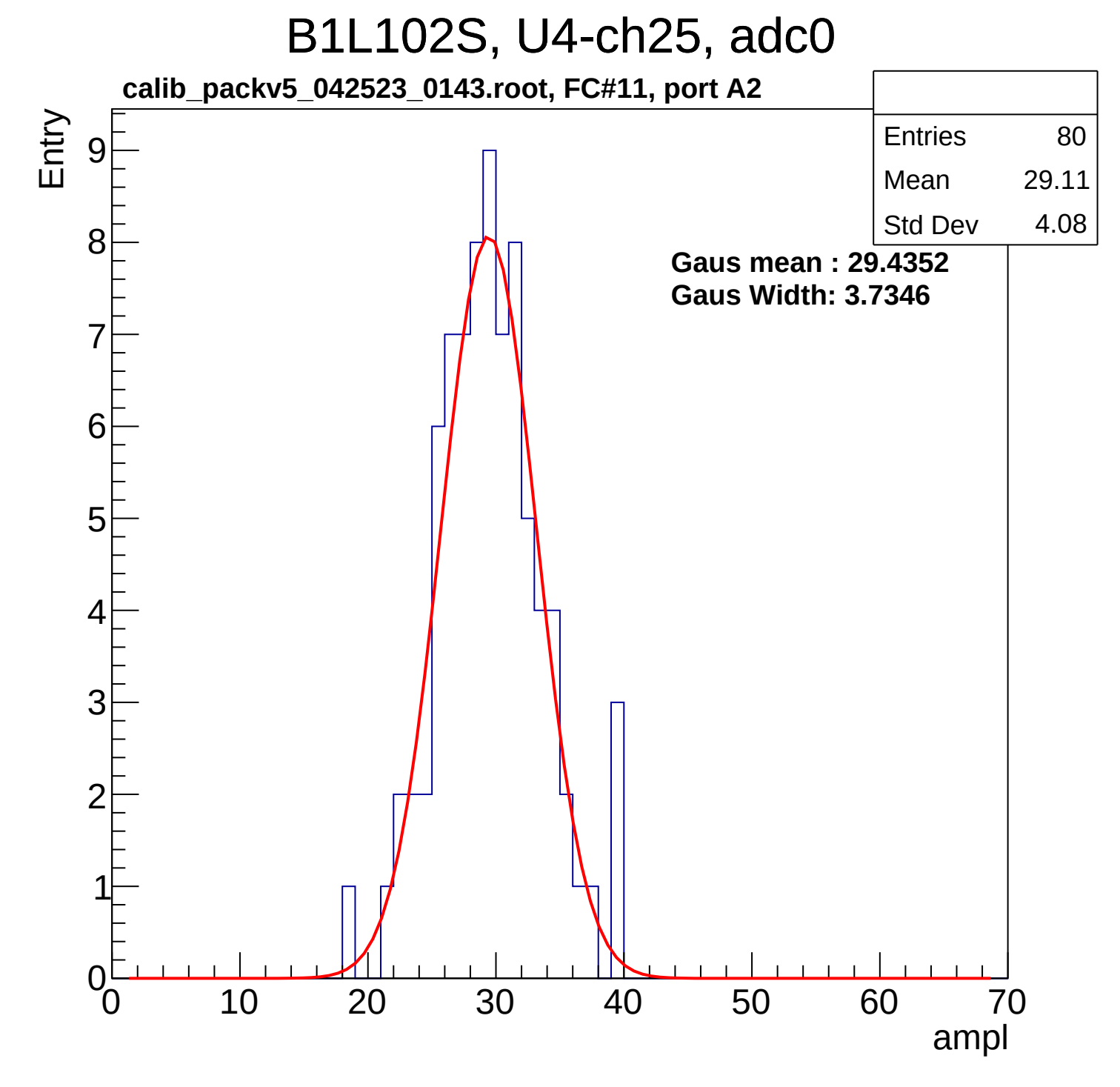
B1L102S, U4-ch25, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 80
Mean 29.11
Std Dev 4.08
Gaus mean : 29.4352
Gaus Width: 3.7346
Entry
ampl
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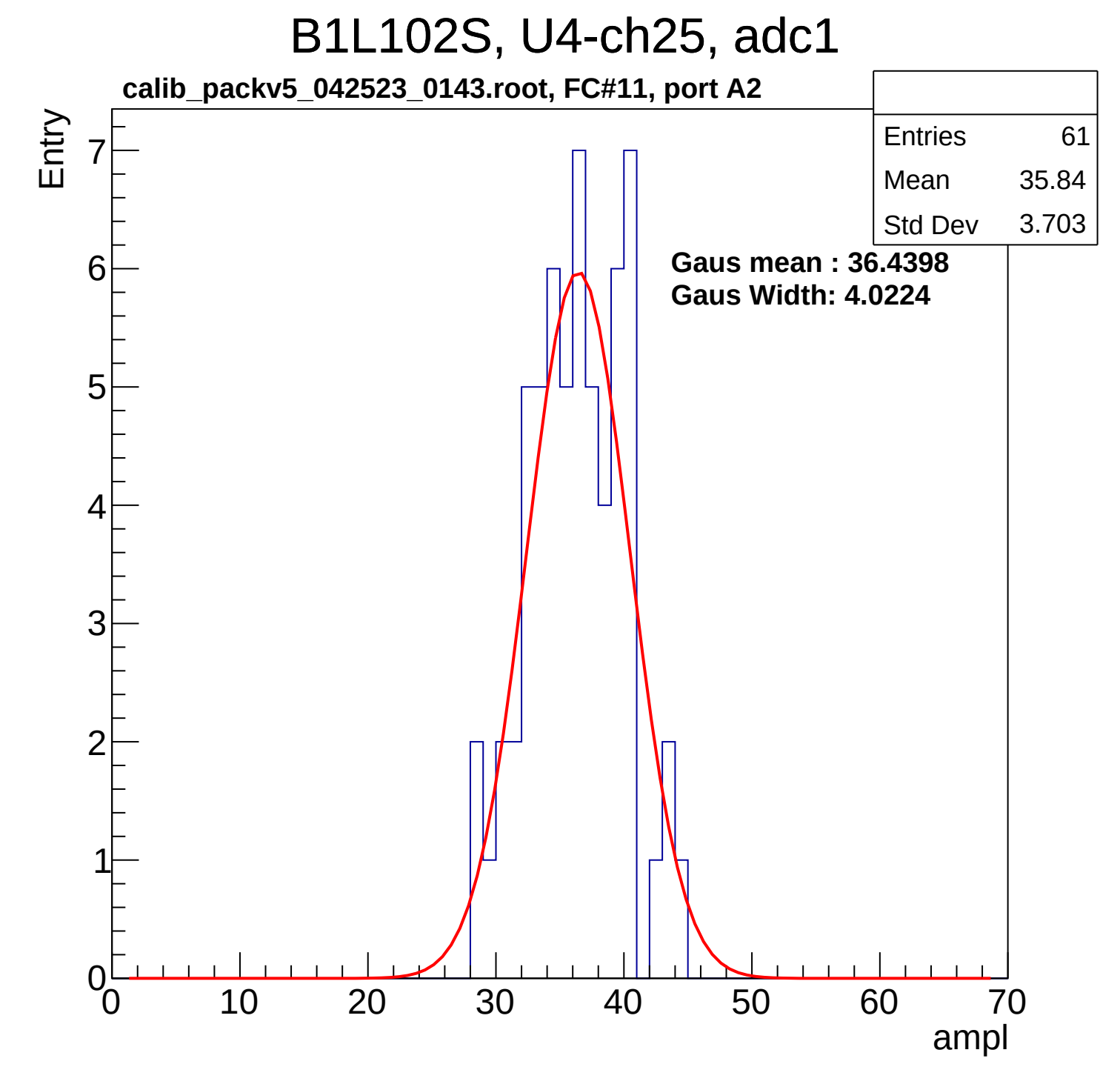
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch25, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 35.84
Std Dev 3.703
Gaus mean : 36.4398
Gaus Width: 4.0224
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
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60
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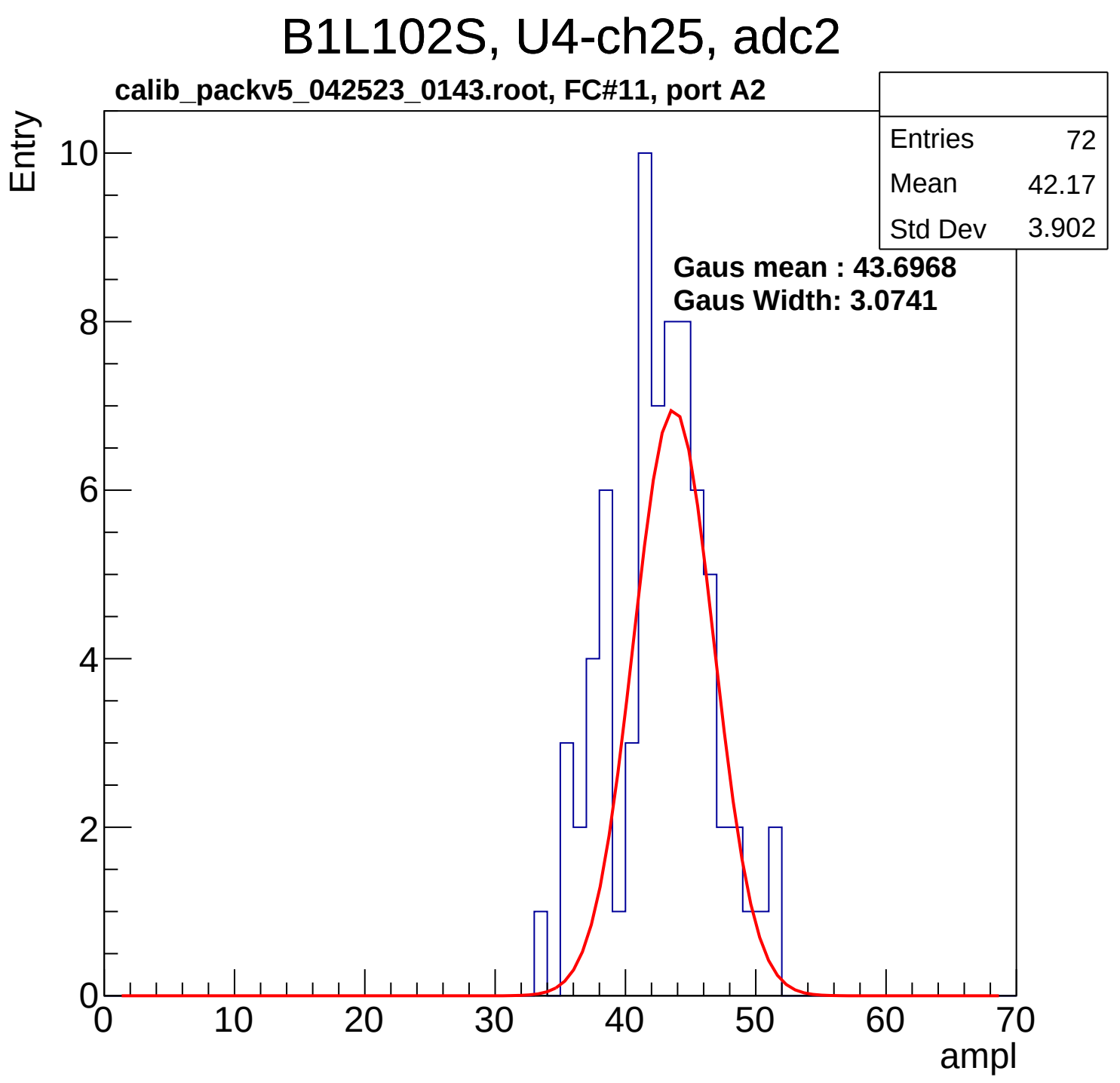
B1L102S, U4-ch25, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 72
Mean 42.17
Std Dev 3.902
Gaus mean : 43.6968
Gaus Width: 3.0741
Entry
ampl
0
2
4
6
8
10
0
10
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40
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60
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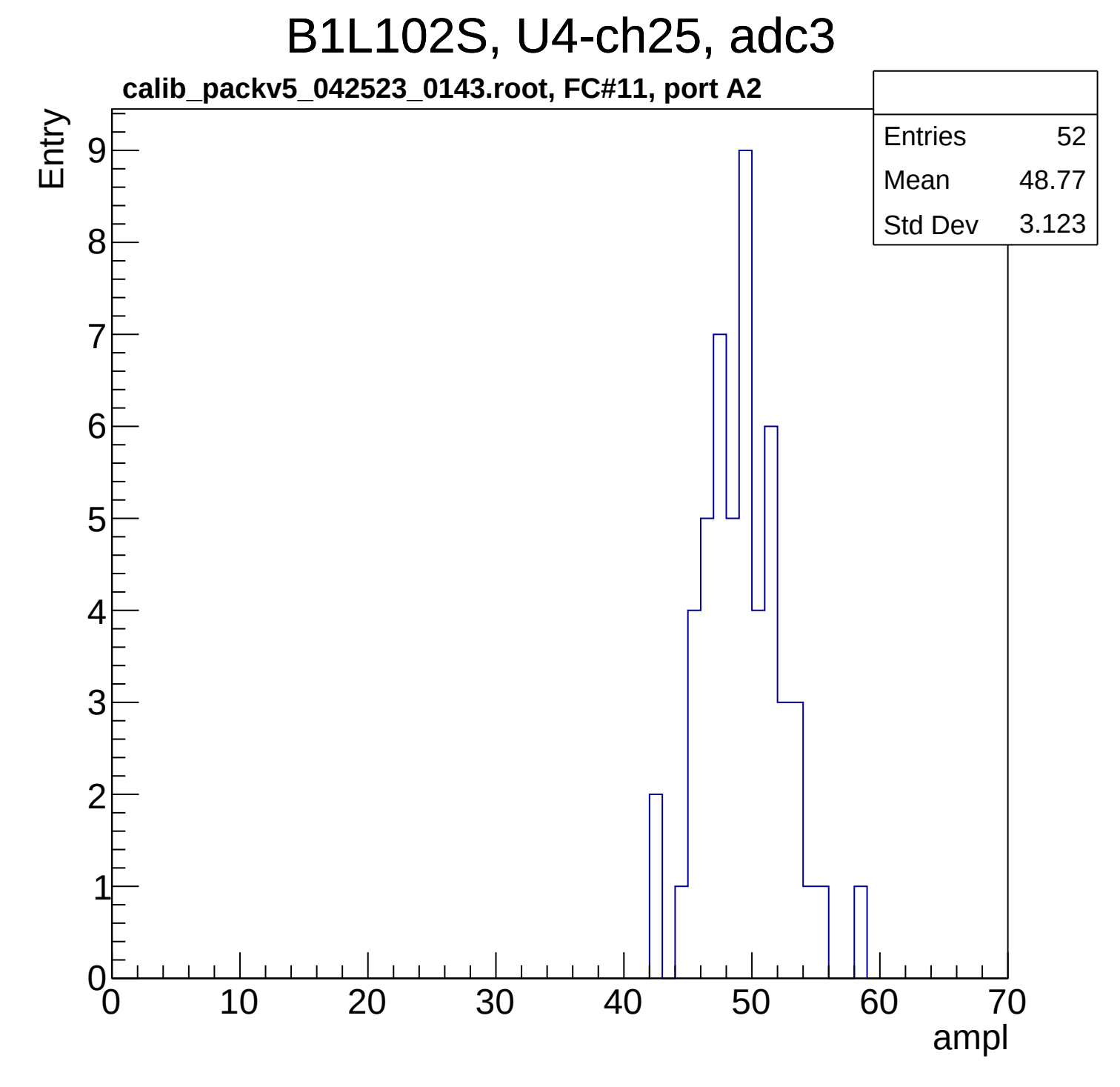
B1L102S, U4-ch25, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 52
Mean 48.77
Std Dev 3.123
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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60
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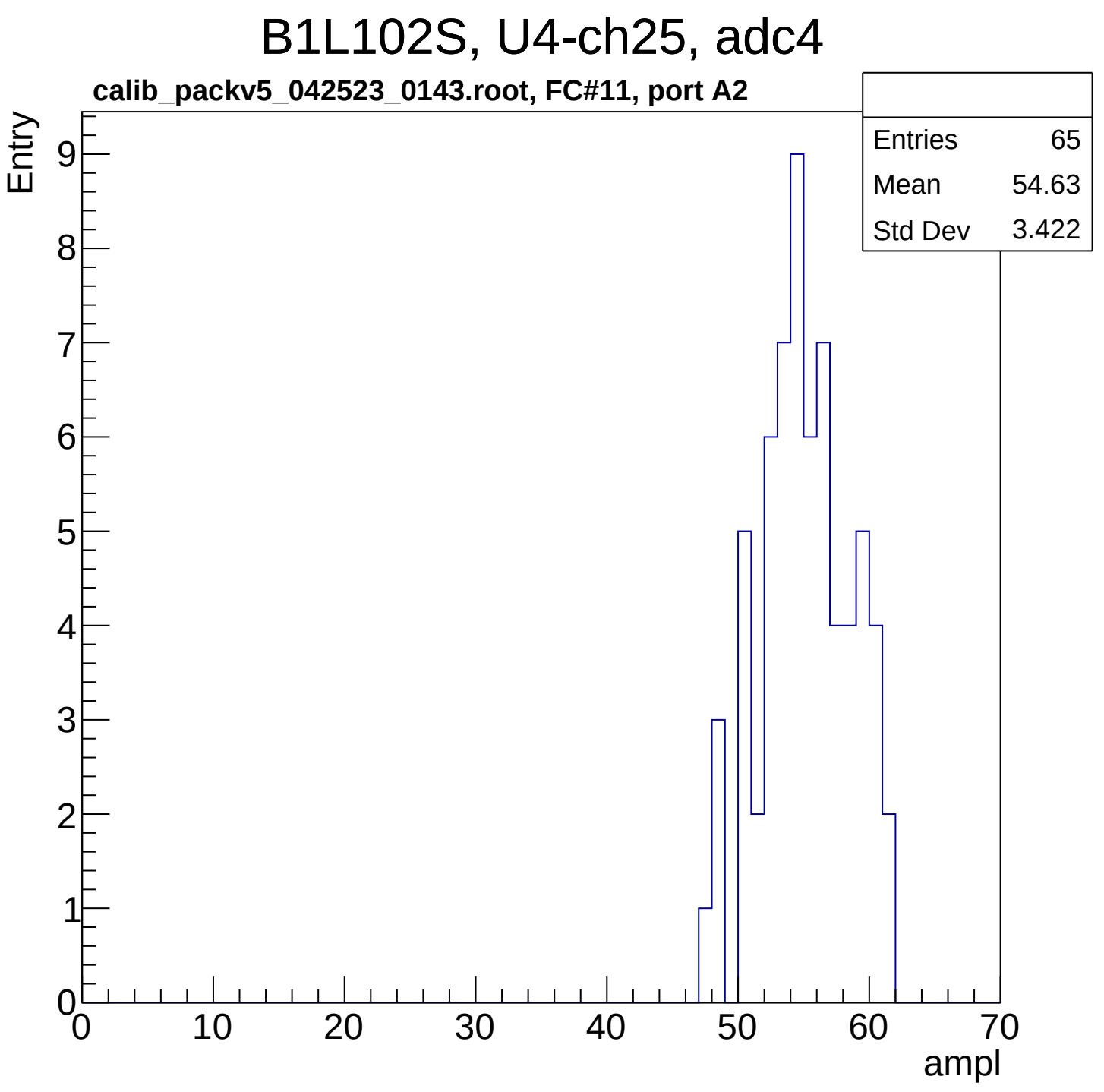
B1L102S, U4-ch25, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 54.63
Std Dev 3.422
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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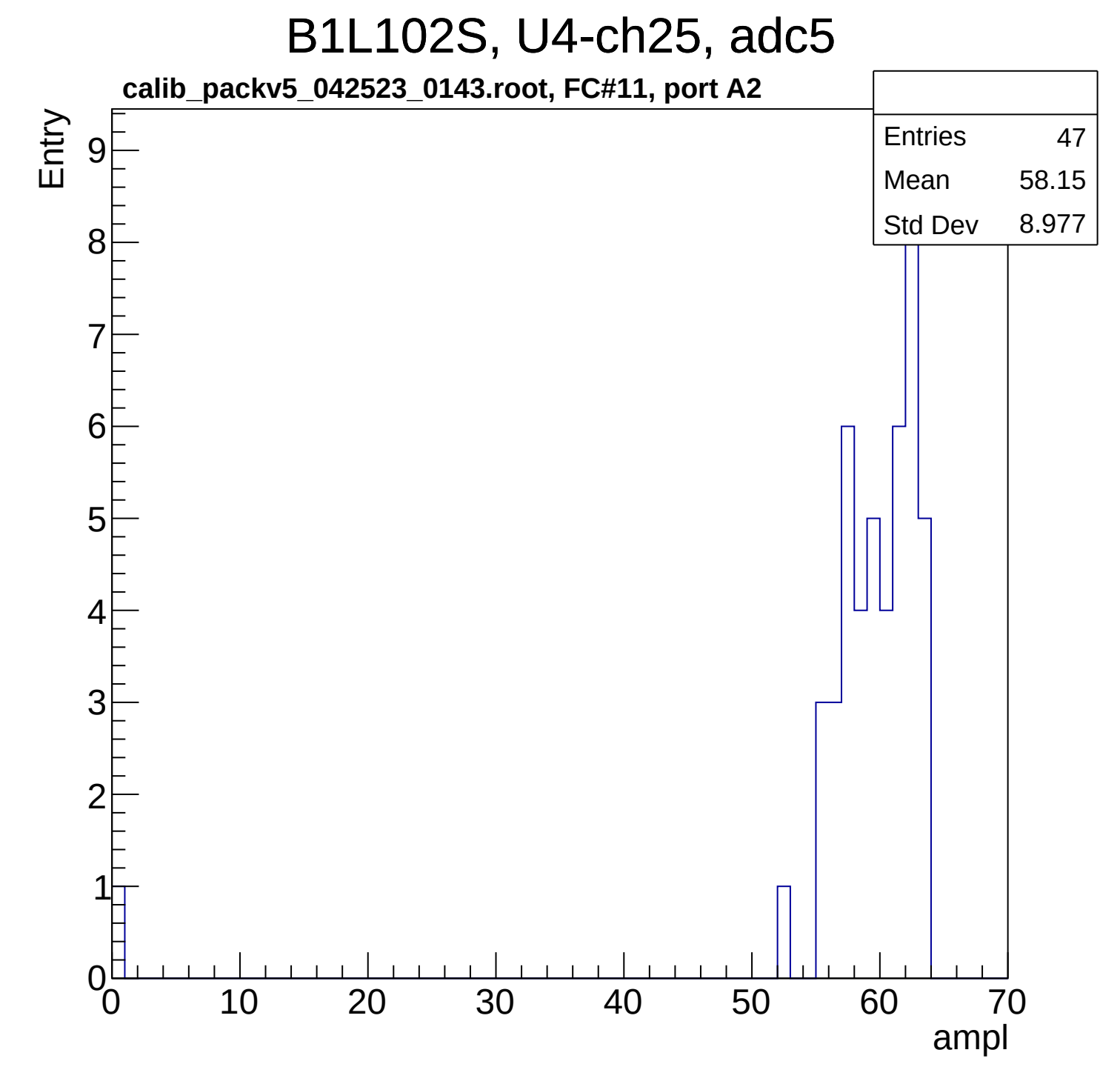
B1L102S, U4-ch25, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 47
Mean 58.15
Std Dev 8.977
Entry
ampl
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2
3
4
5
6
7
8
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0
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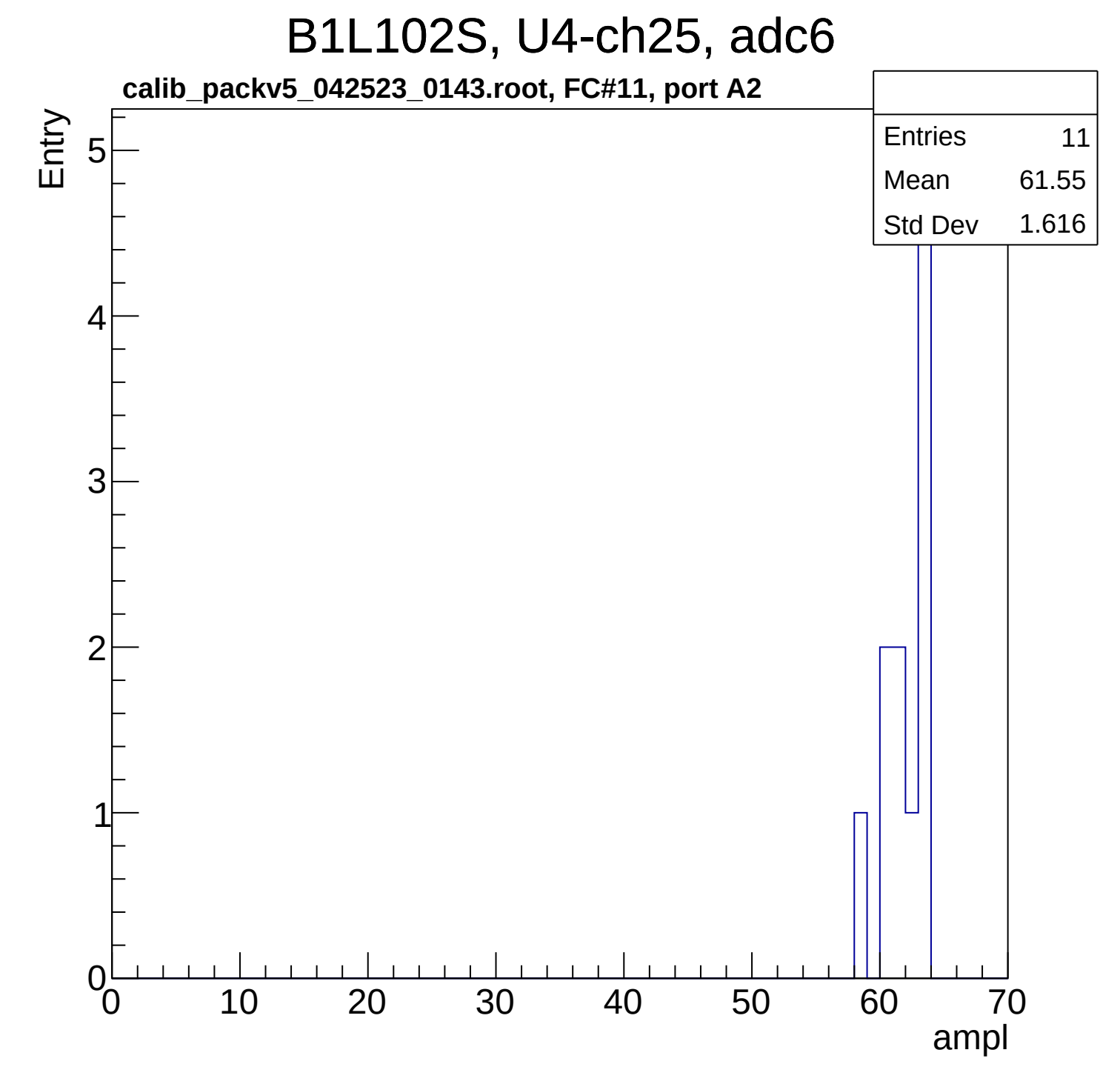
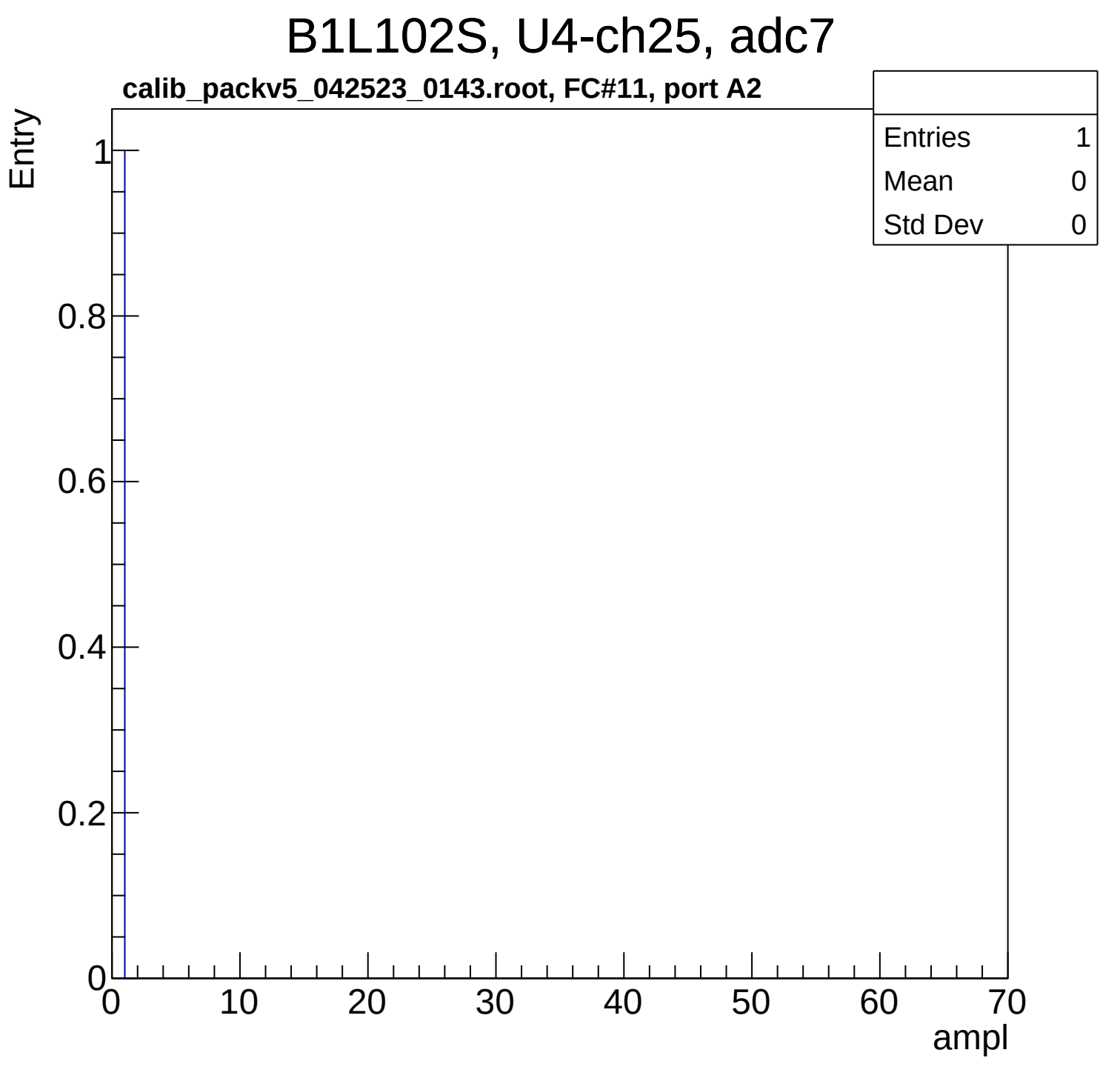

B1L102S, U4-ch25, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 11
Mean 61.55
Std Dev 1.616
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch25, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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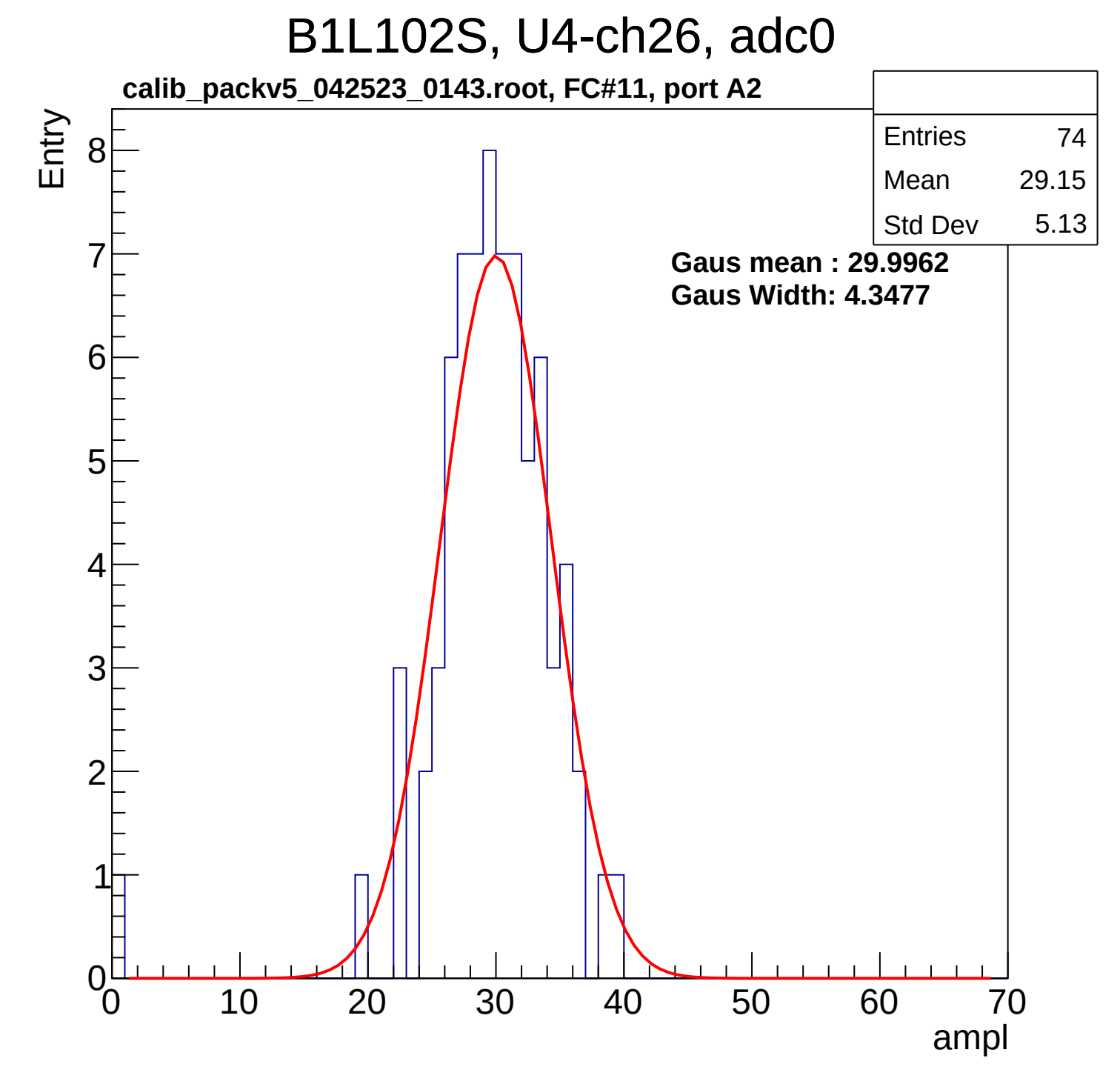
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch26, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 29.15
Std Dev 5.13
Gaus mean : 29.9962
Gaus Width: 4.3477
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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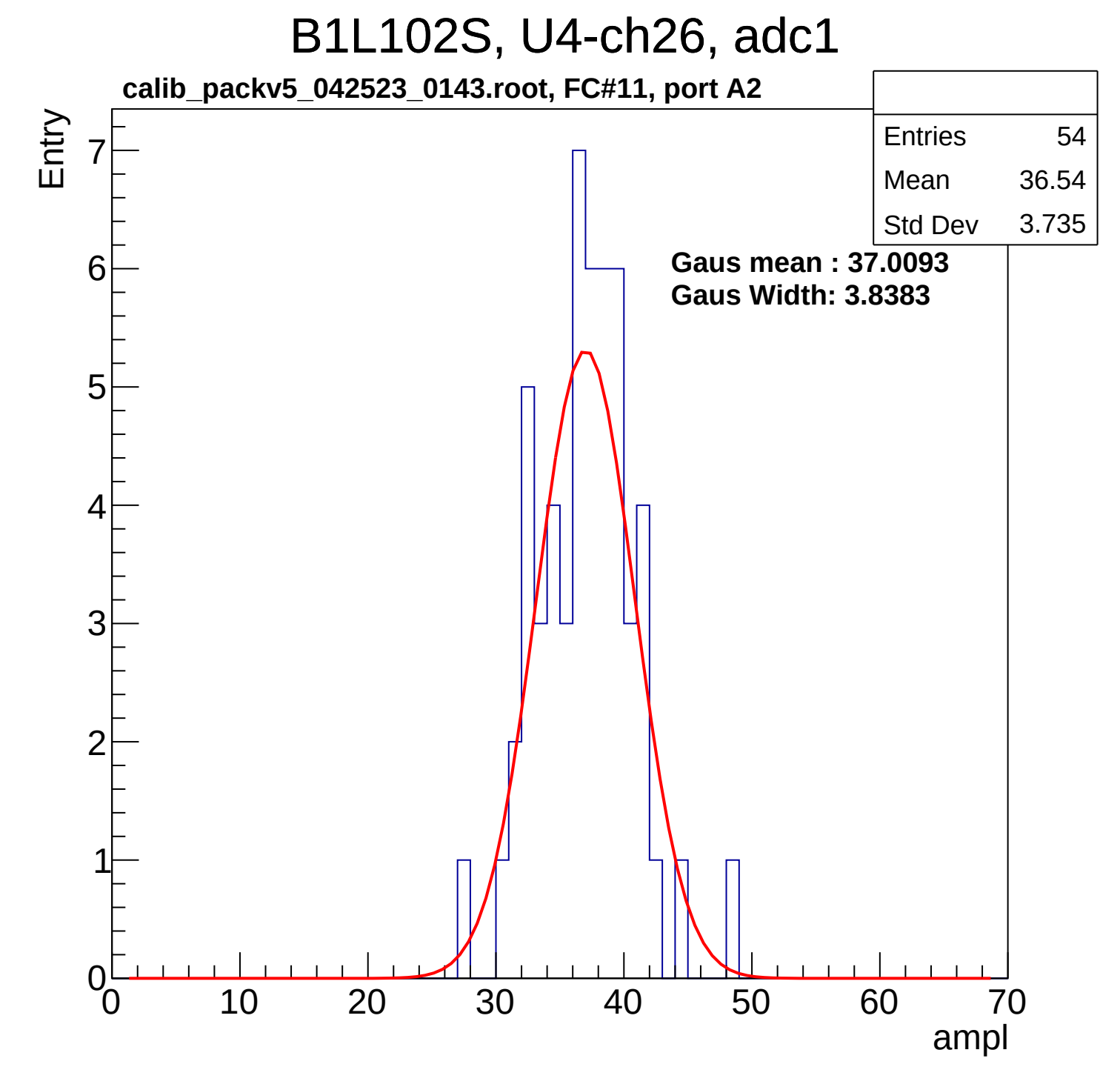
B1L102S, U4-ch26, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 36.54
Std Dev 3.735
Gaus mean : 37.0093
Gaus Width: 3.8383
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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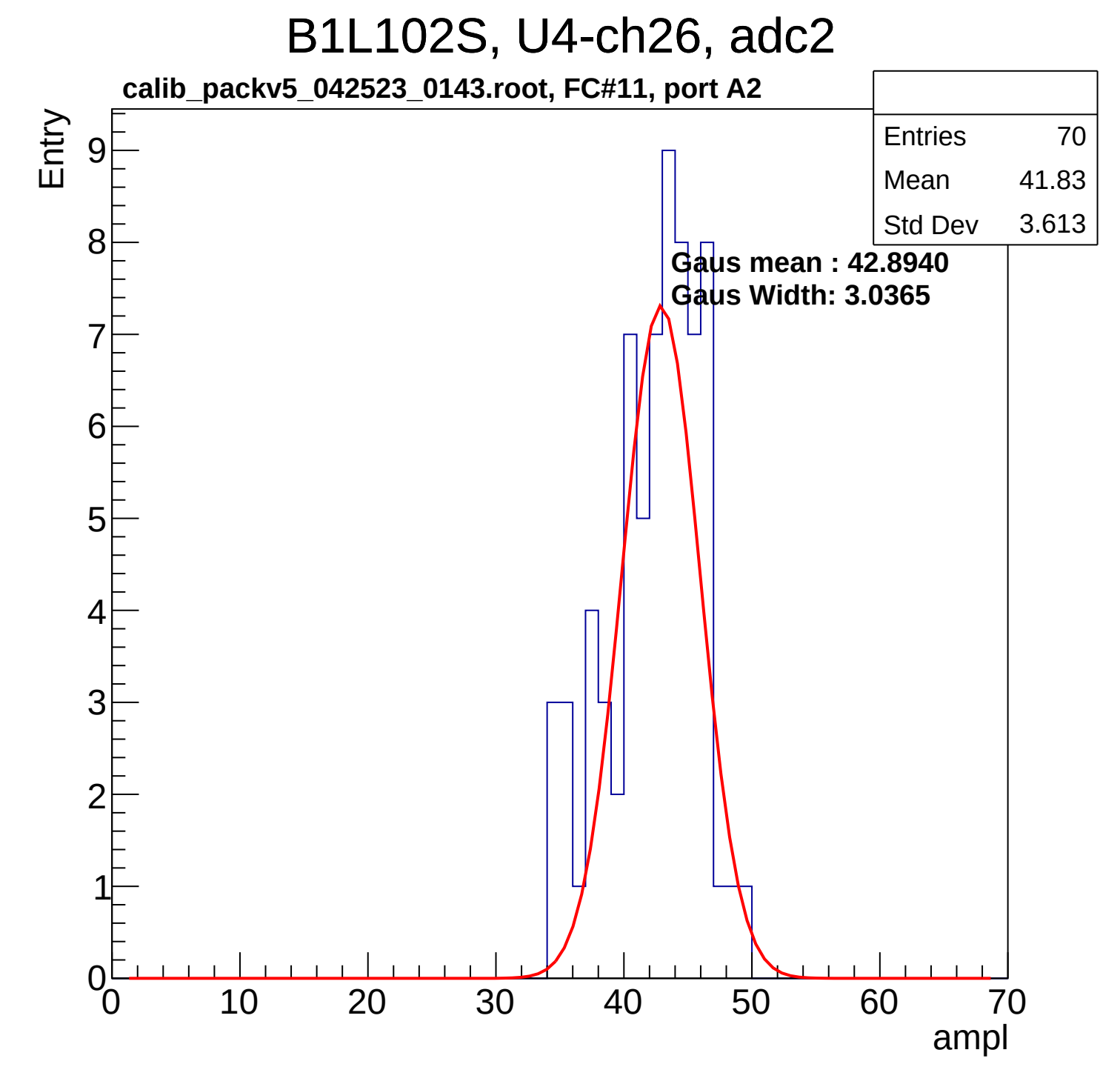
B1L102S, U4-ch26, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 41.83
Std Dev 3.613
Gaus mean : 42.8940
Gaus Width: 3.0365
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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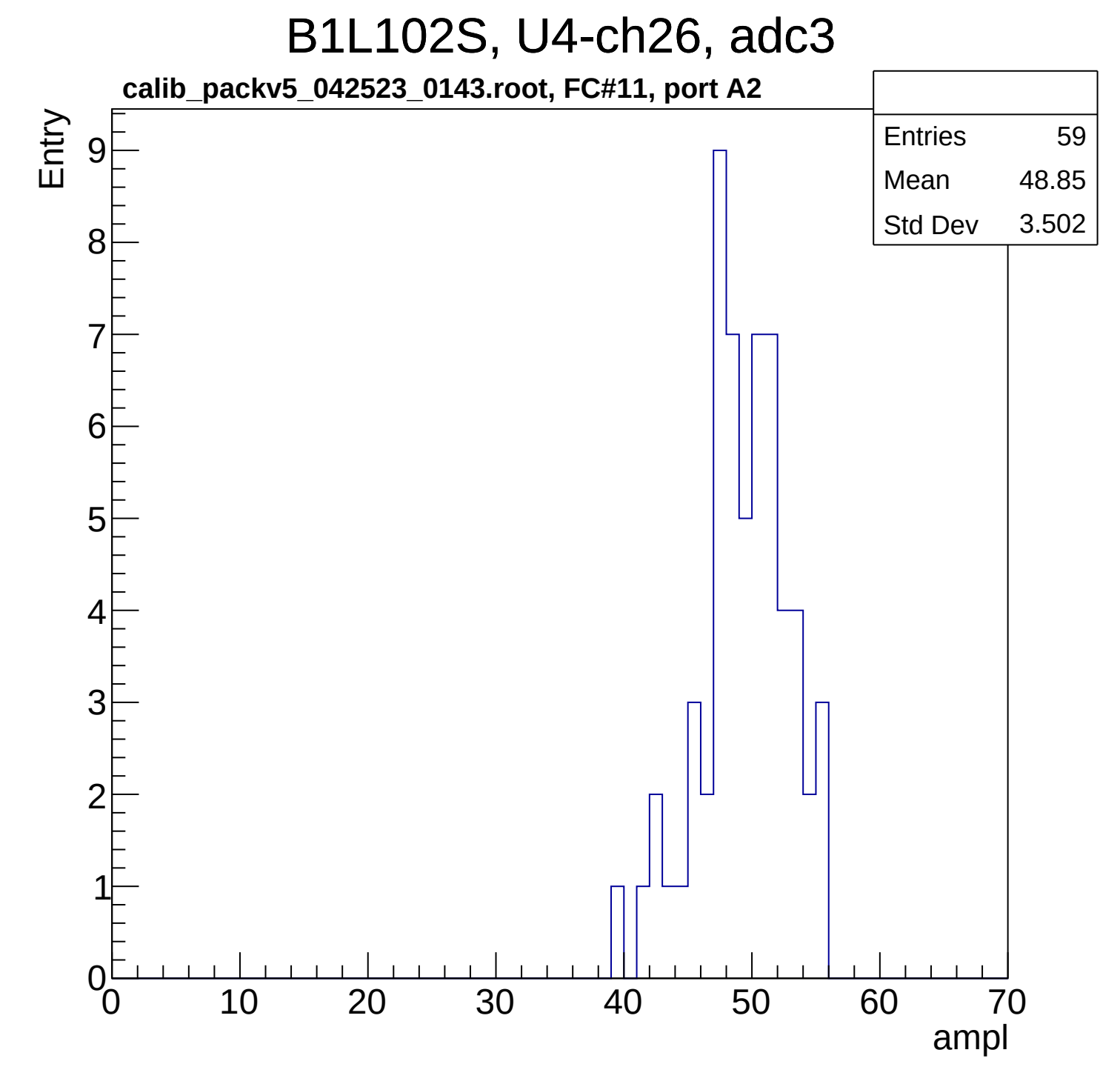
B1L102S, U4-ch26, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 48.85
Std Dev 3.502
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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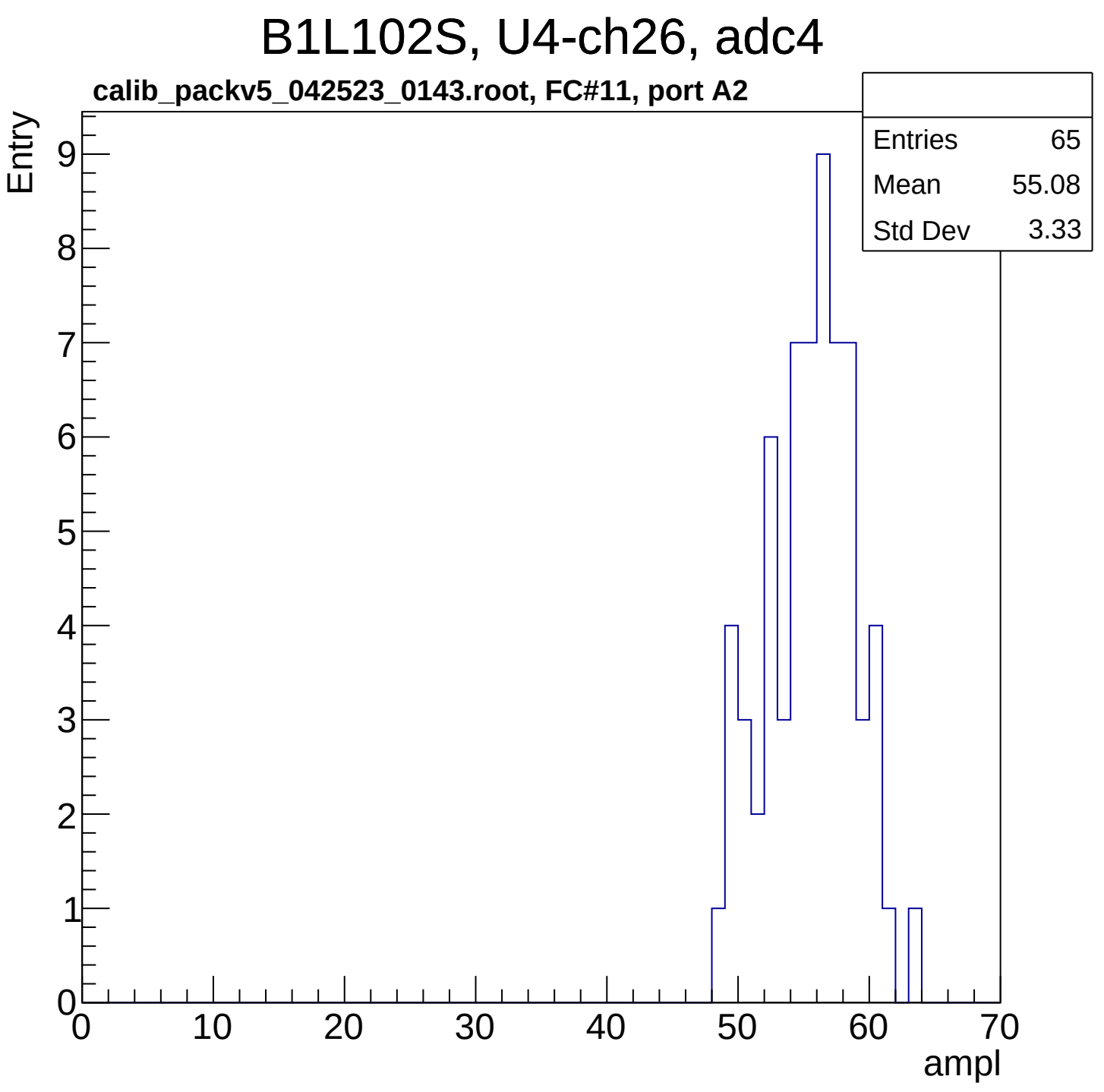
B1L102S, U4-ch26, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 55.08
Std Dev 3.33
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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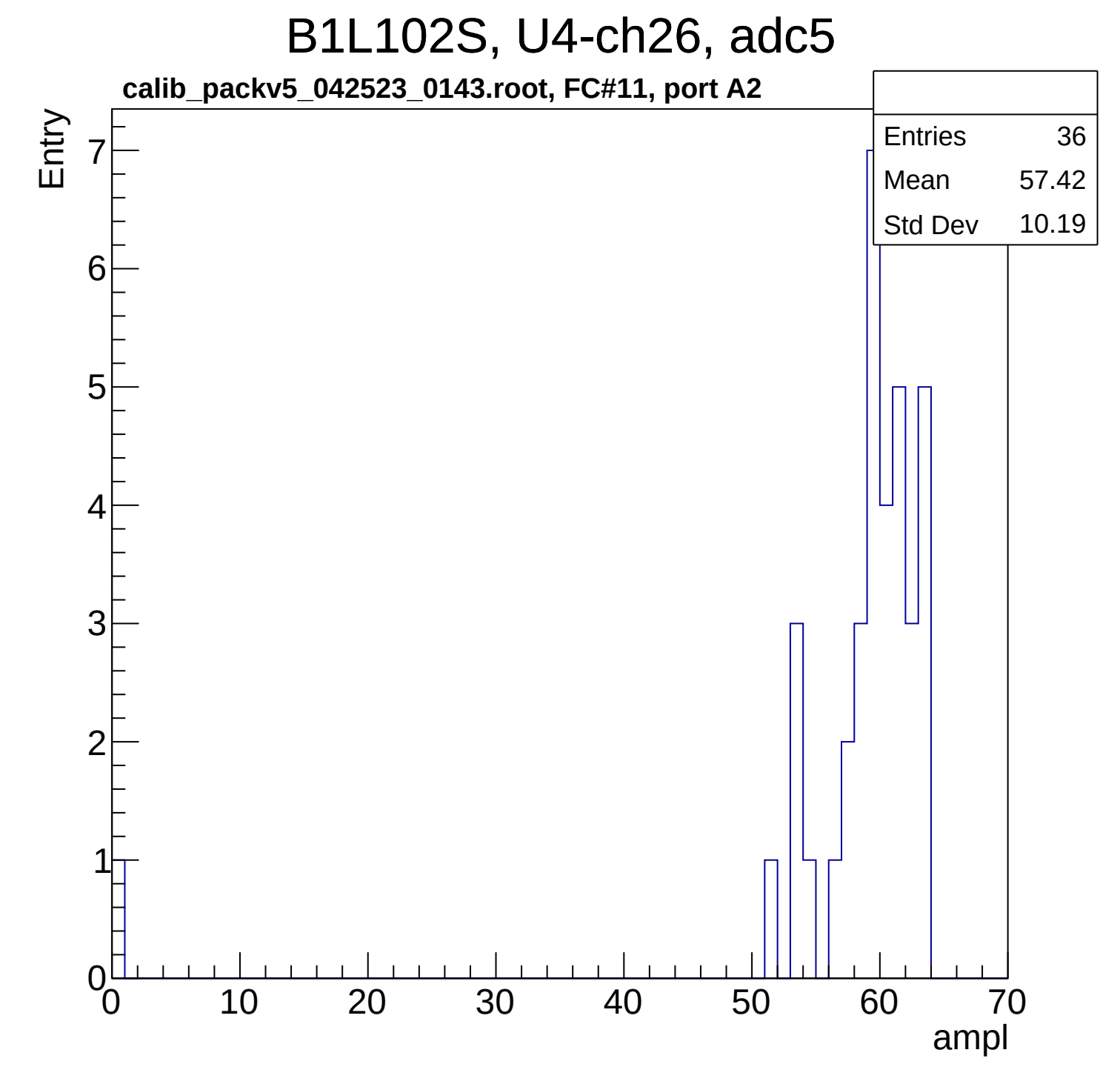
B1L102S, U4-ch26, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 36
Mean 57.42
Std Dev 10.19
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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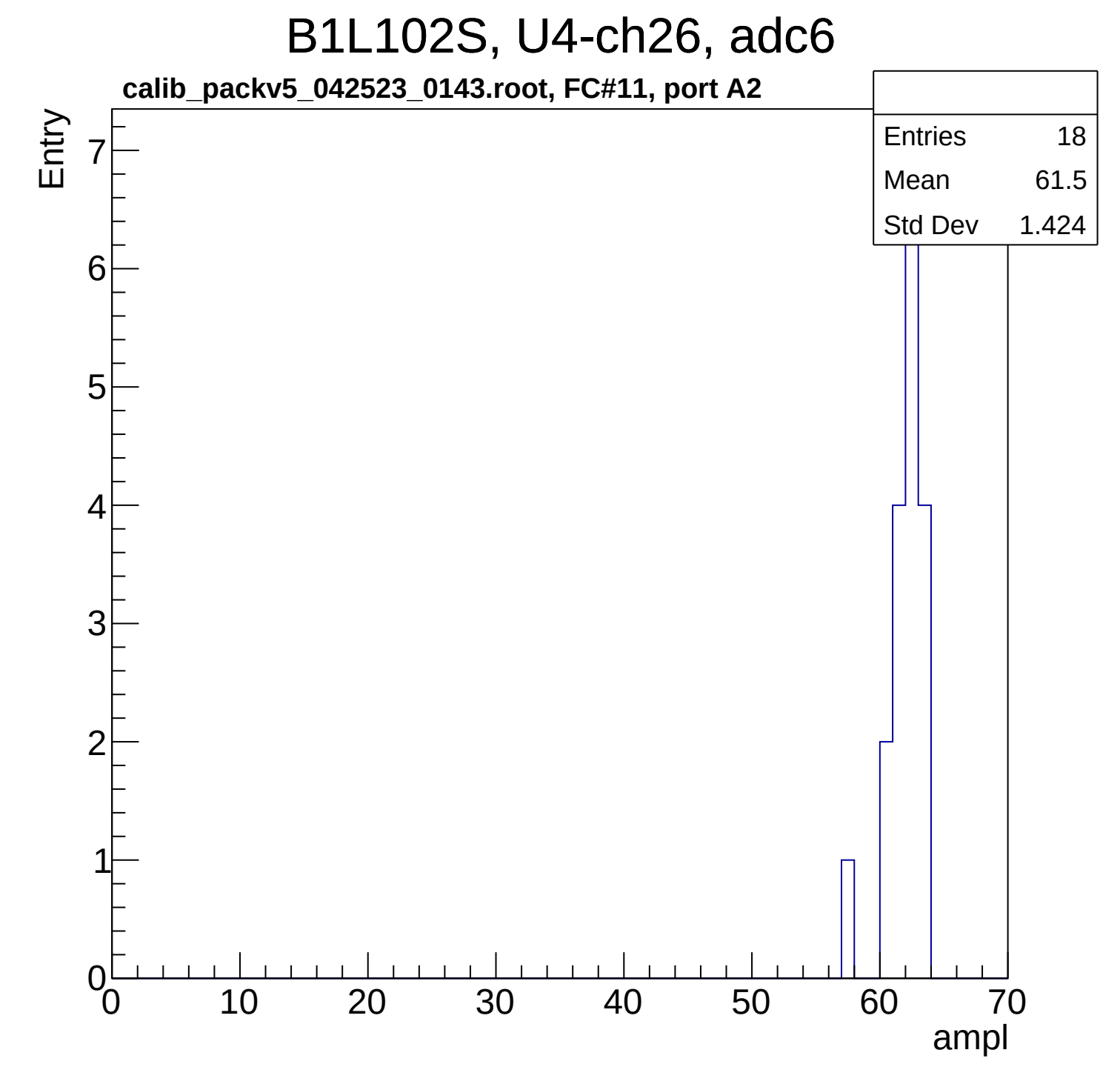
B1L102S, U4-ch26, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 18
Mean 61.5
Std Dev 1.424
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
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60
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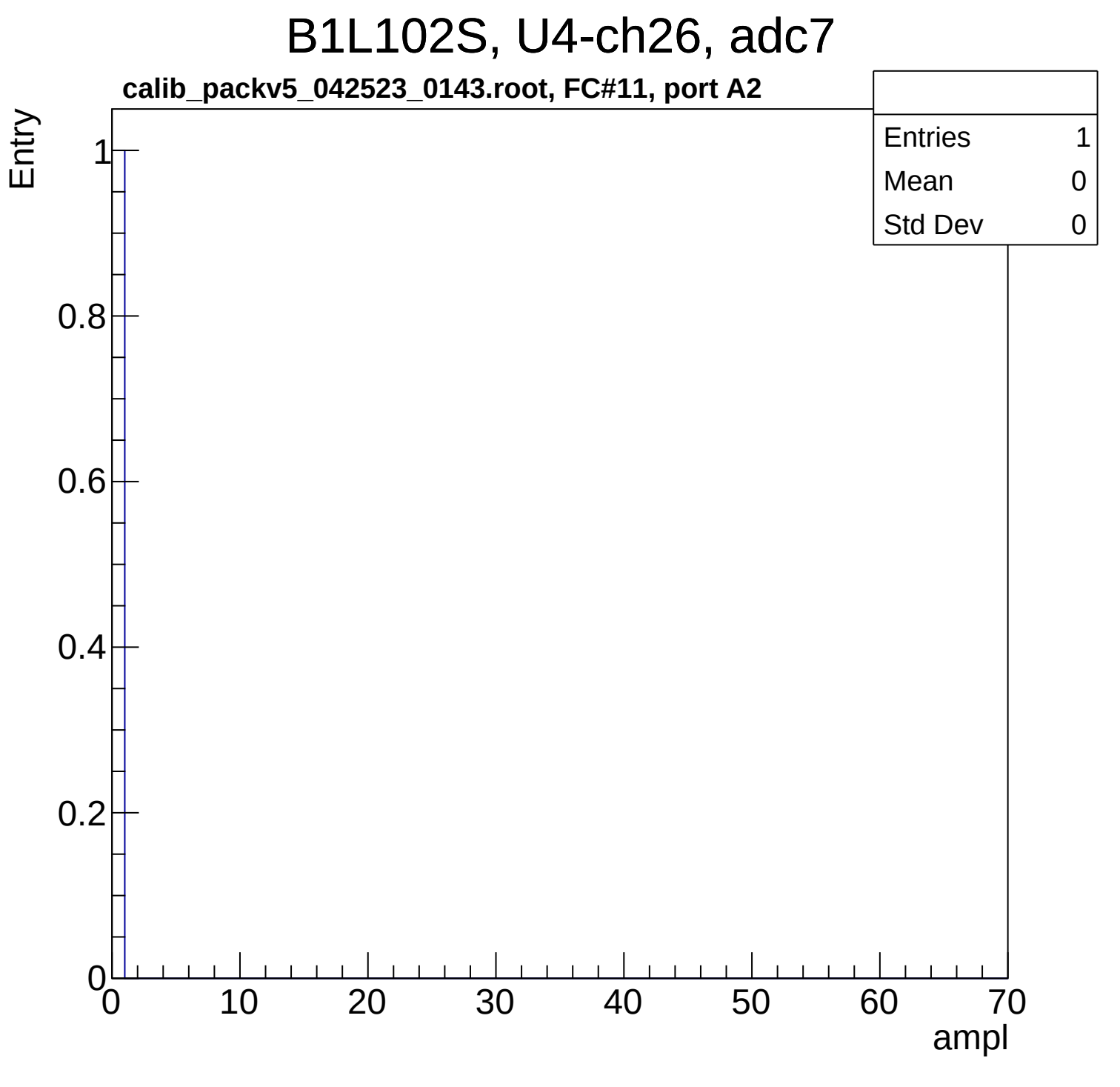
B1L102S, U4-ch26, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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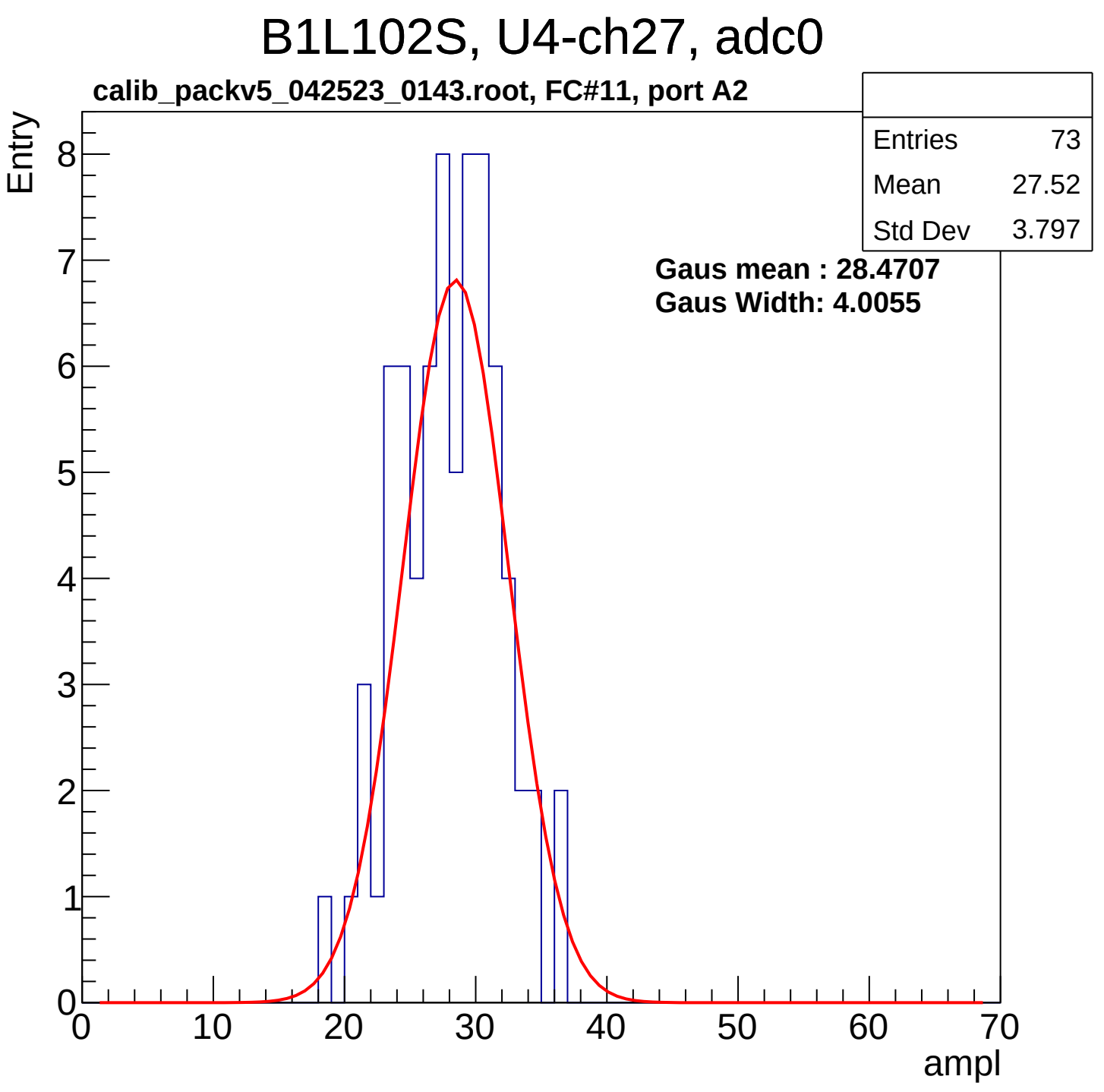
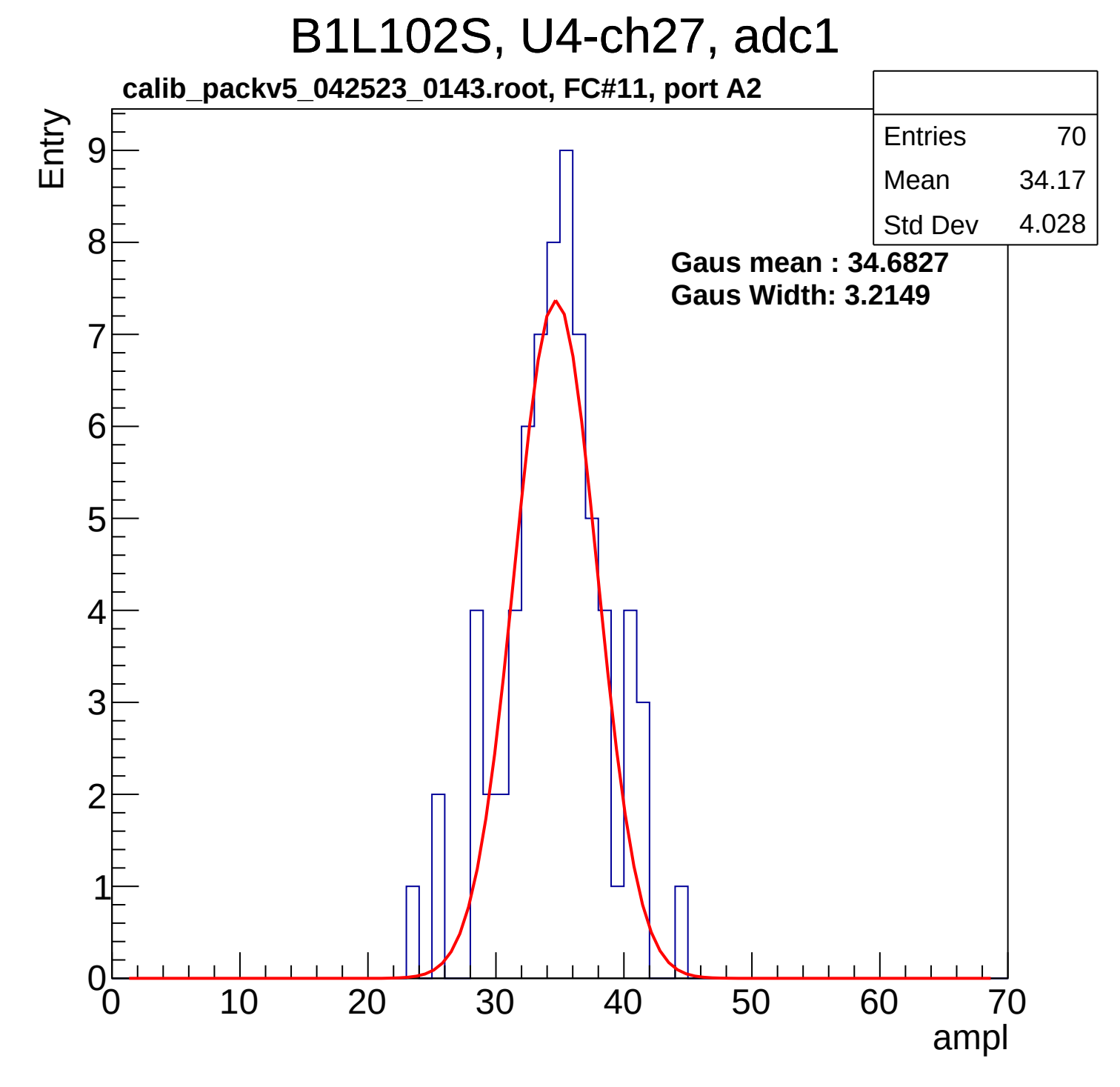
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch27, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 27.52
Std Dev 3.797
Gaus mean : 28.4707
Gaus Width: 4.0055
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch27, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 34.17
Std Dev 4.028
Gaus mean : 34.6827
Gaus Width: 3.2149
Entry
ampl
0
1
2
3
4
5
6
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8
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0
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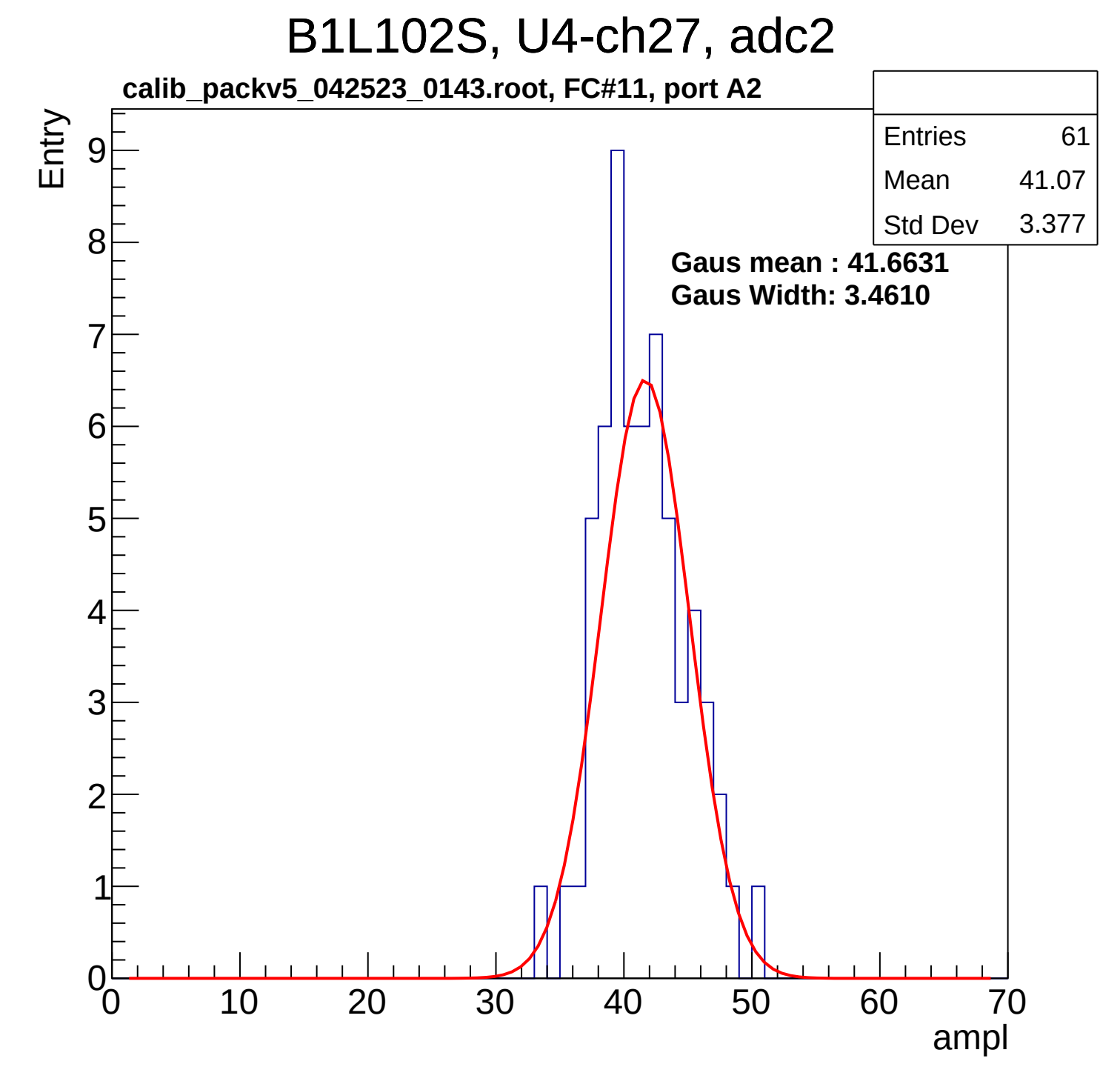
B1L102S, U4-ch27, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 41.07
Std Dev 3.377
Gaus mean : 41.6631
Gaus Width: 3.4610
Entry
ampl
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2
3
4
5
6
7
8
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0
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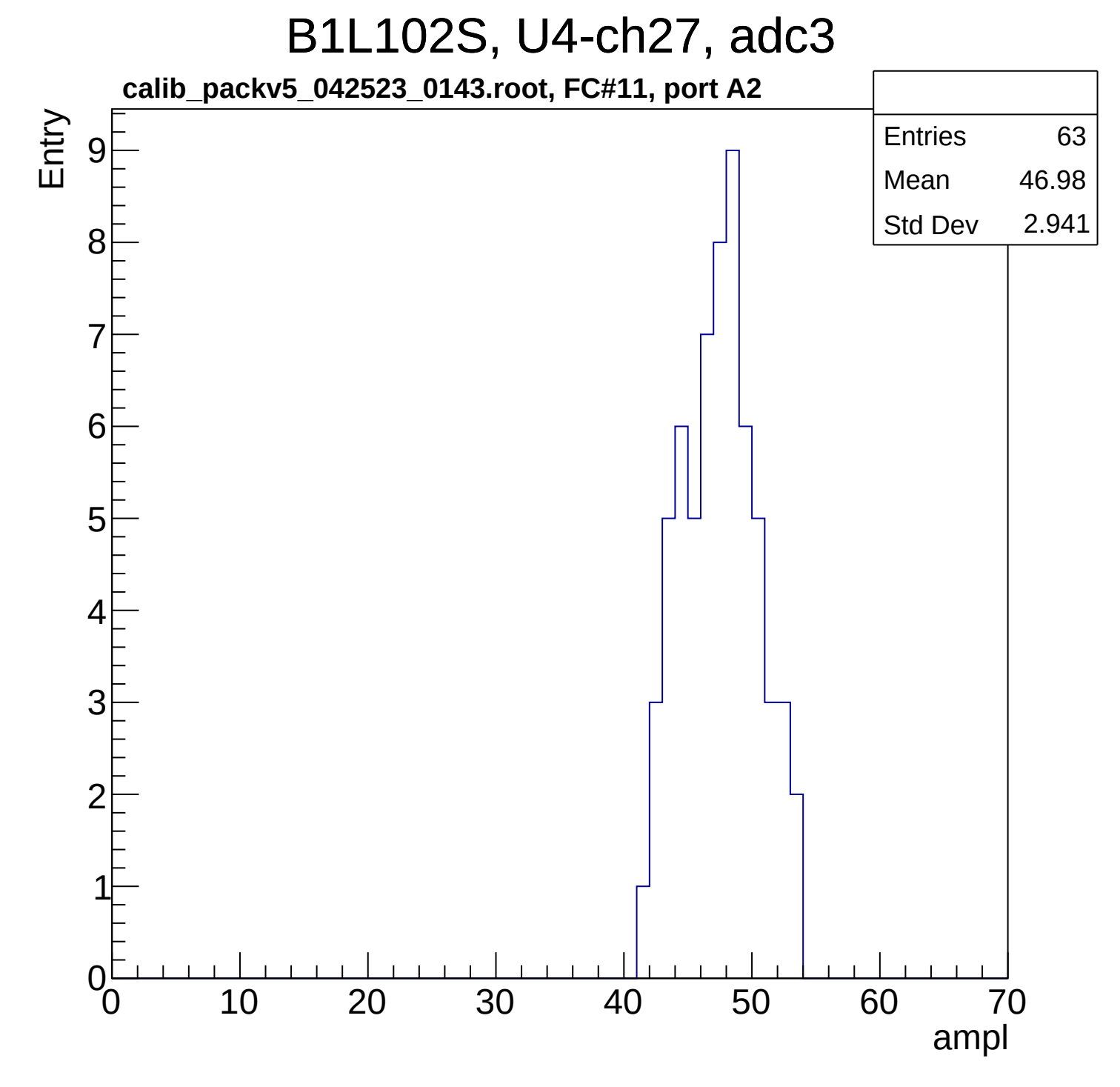
B1L102S, U4-ch27, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 46.98
Std Dev 2.941
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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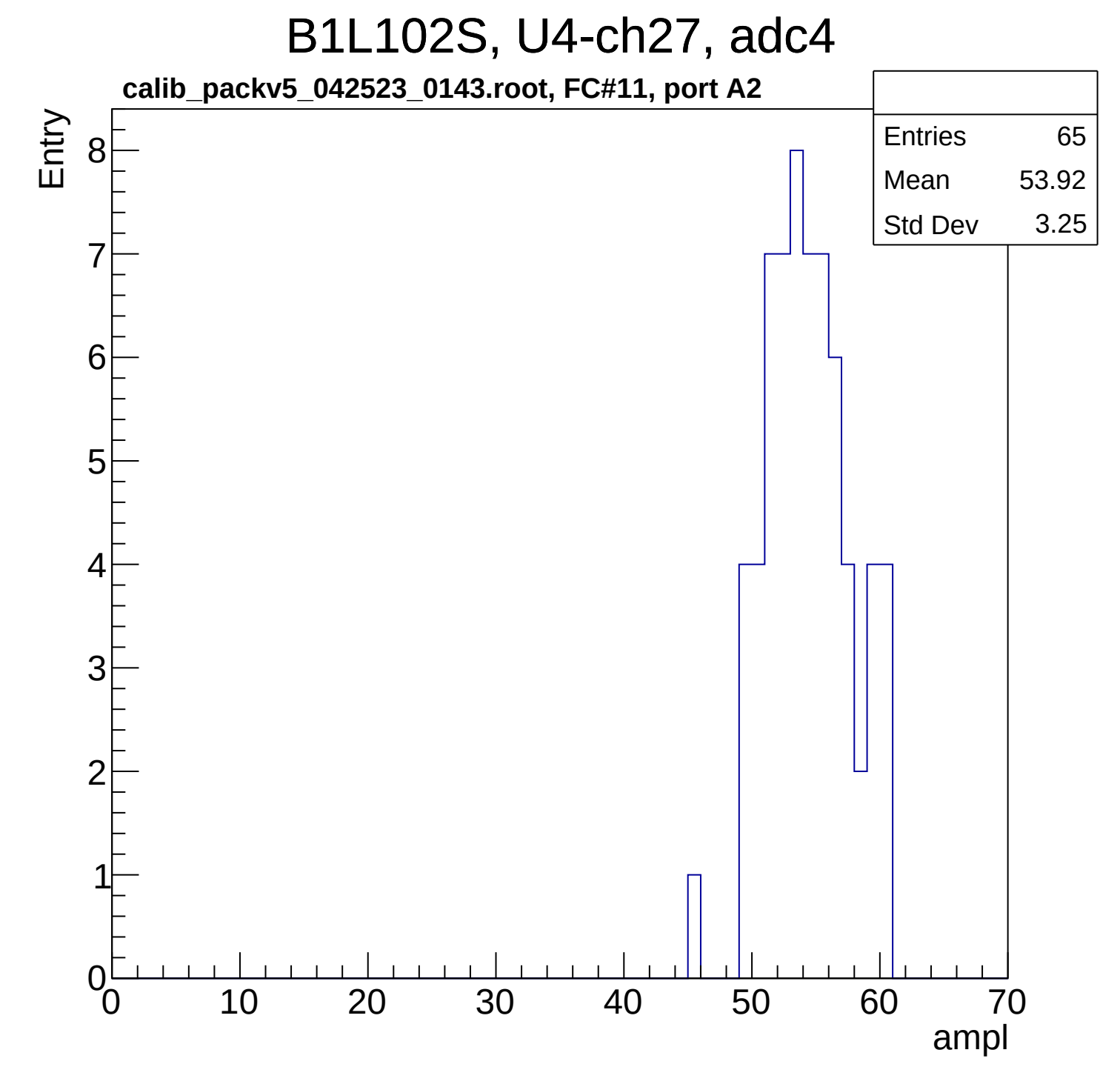
B1L102S, U4-ch27, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 53.92
Std Dev 3.25
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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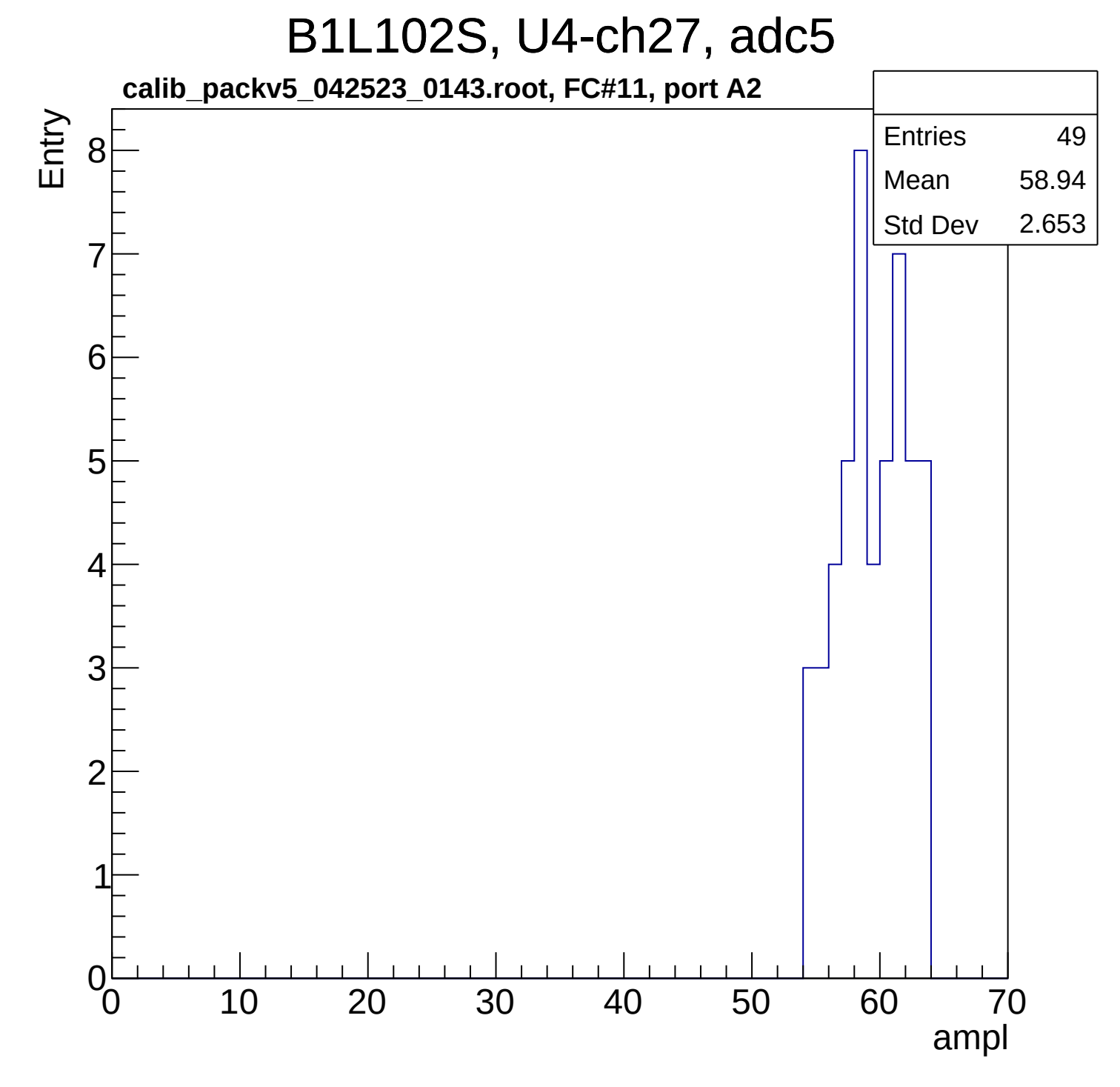
B1L102S, U4-ch27, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 58.94
Std Dev 2.653
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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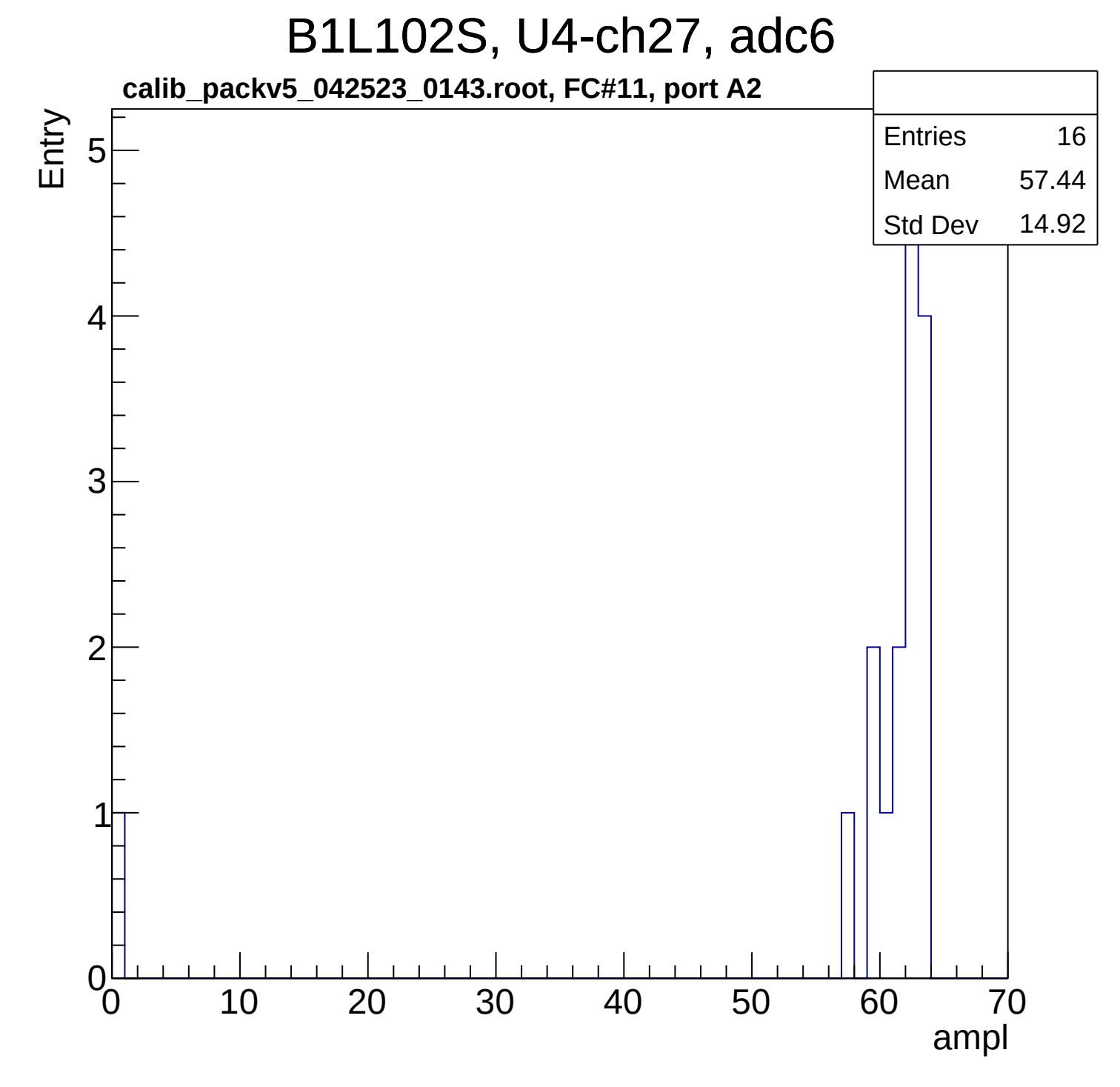
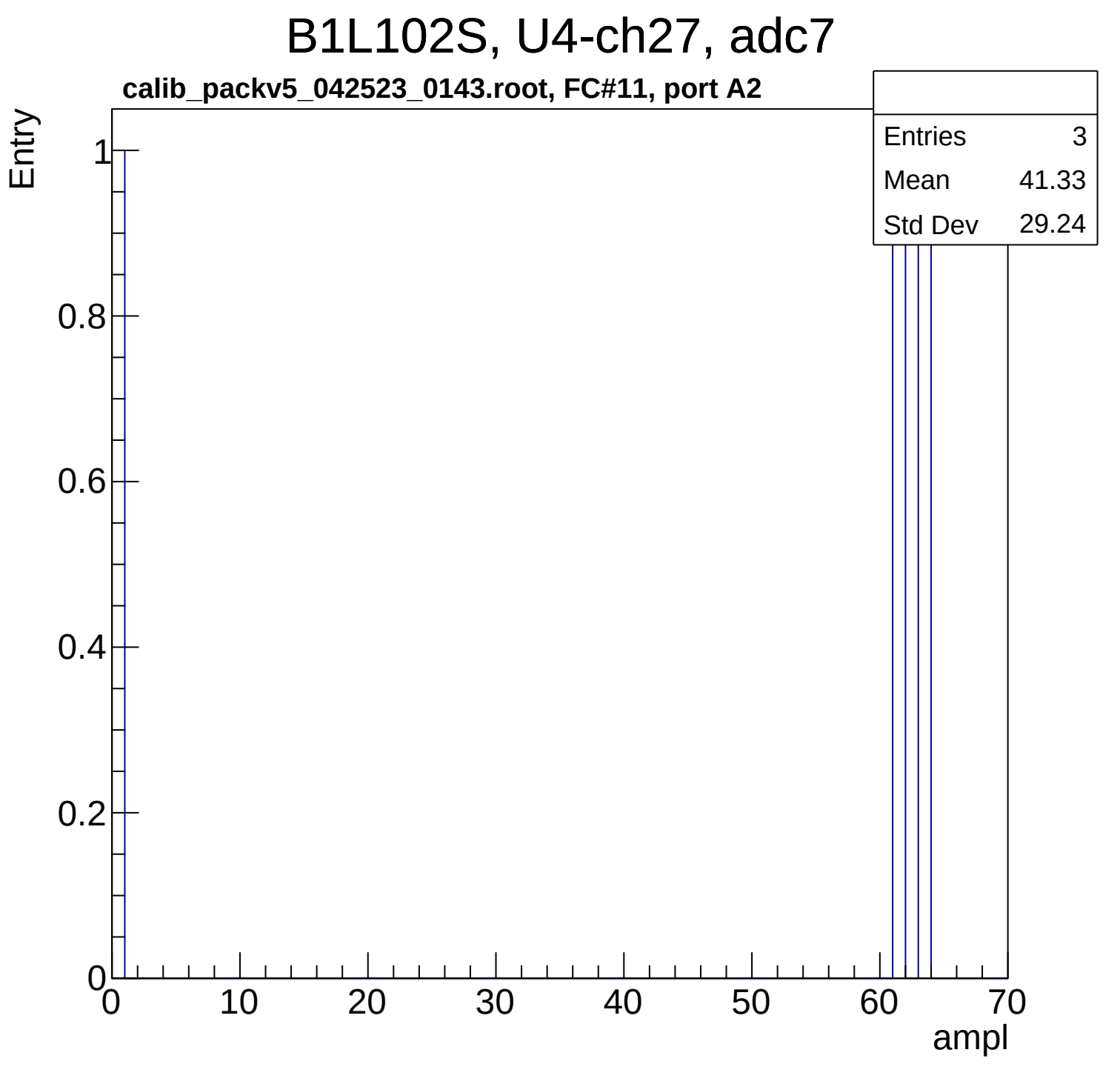
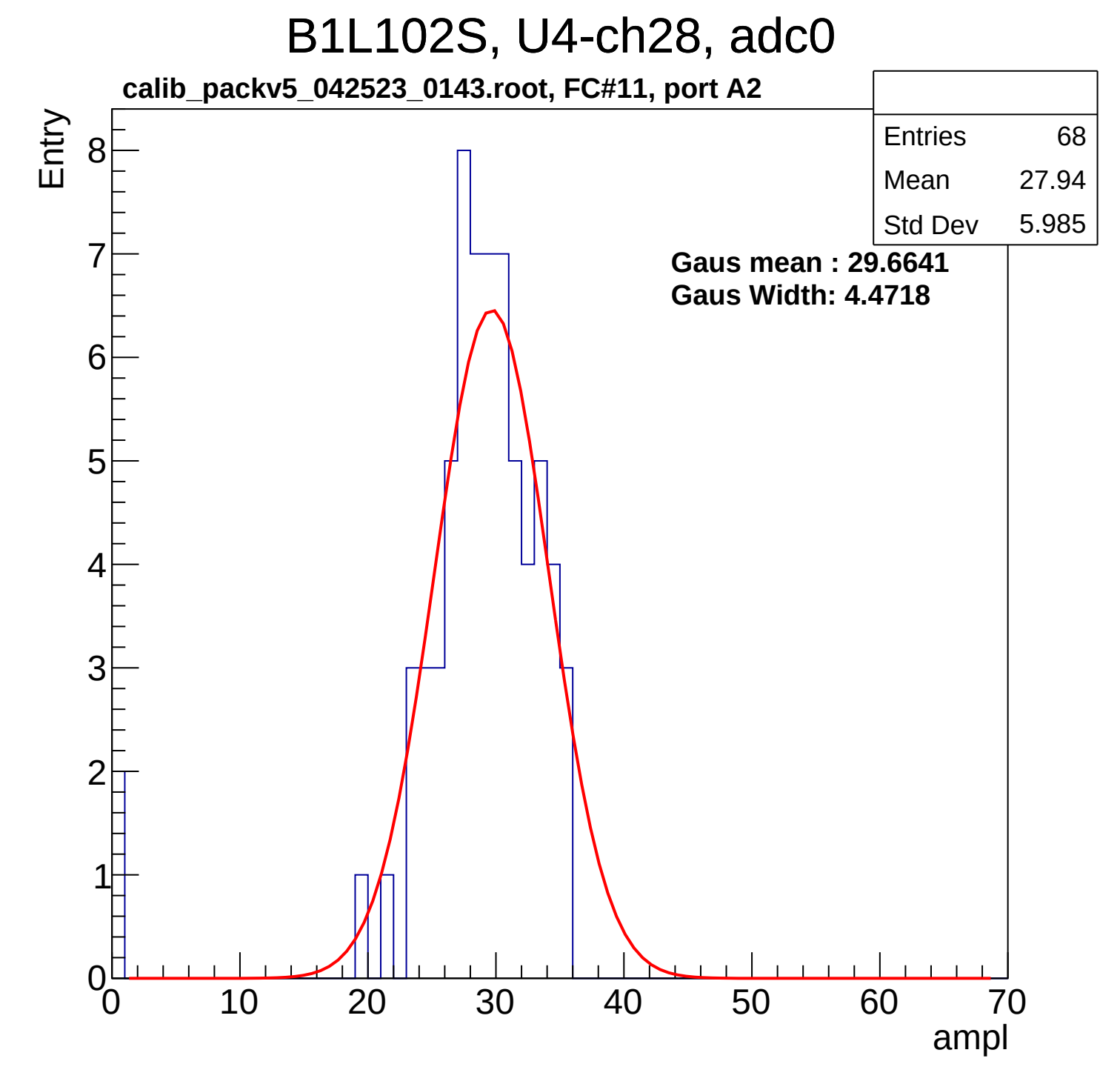

B1L102S, U4-ch27, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 16
Mean 57.44
Std Dev 14.92
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch27, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 41.33
Std Dev 29.24
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch28, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 27.94
Std Dev 5.985
Gaus mean : 29.6641
Gaus Width: 4.4718
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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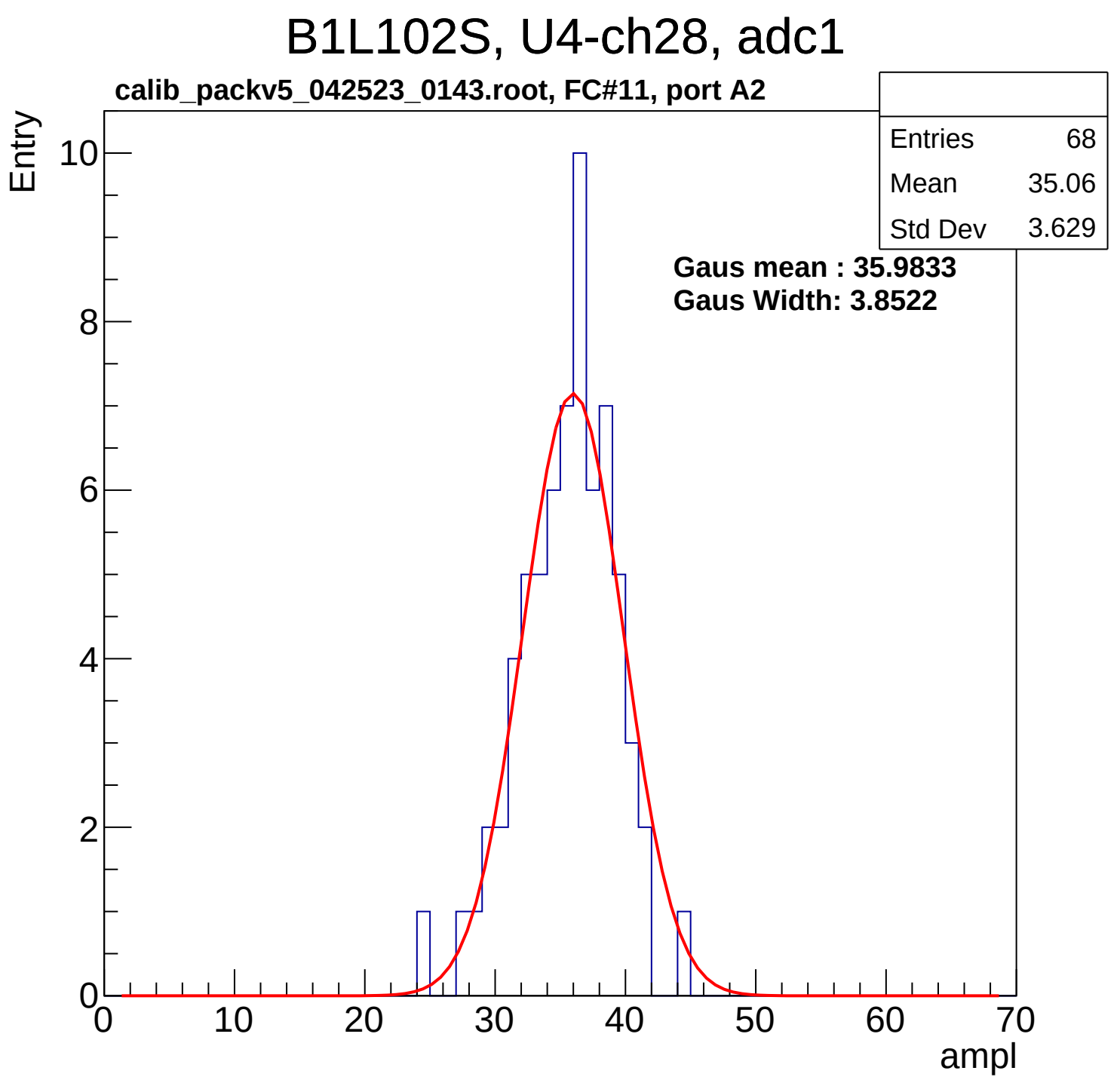
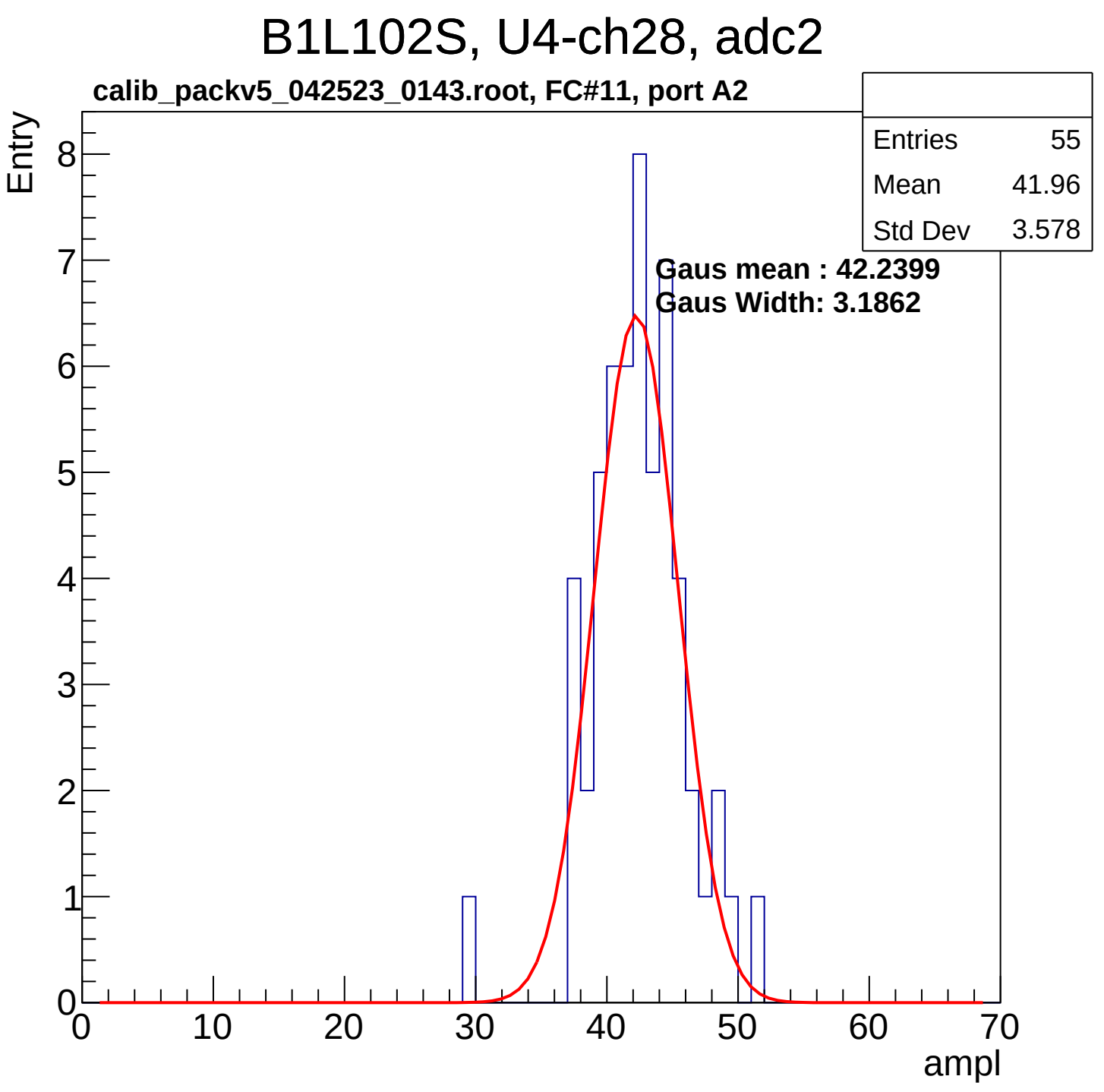

B1L102S, U4-ch28, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 35.06
Std Dev 3.629
Gaus mean : 35.9833
Gaus Width: 3.8522
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch28, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 41.96
Std Dev 3.578
Gaus mean : 42.2399
Gaus Width: 3.1862
Entry
ampl
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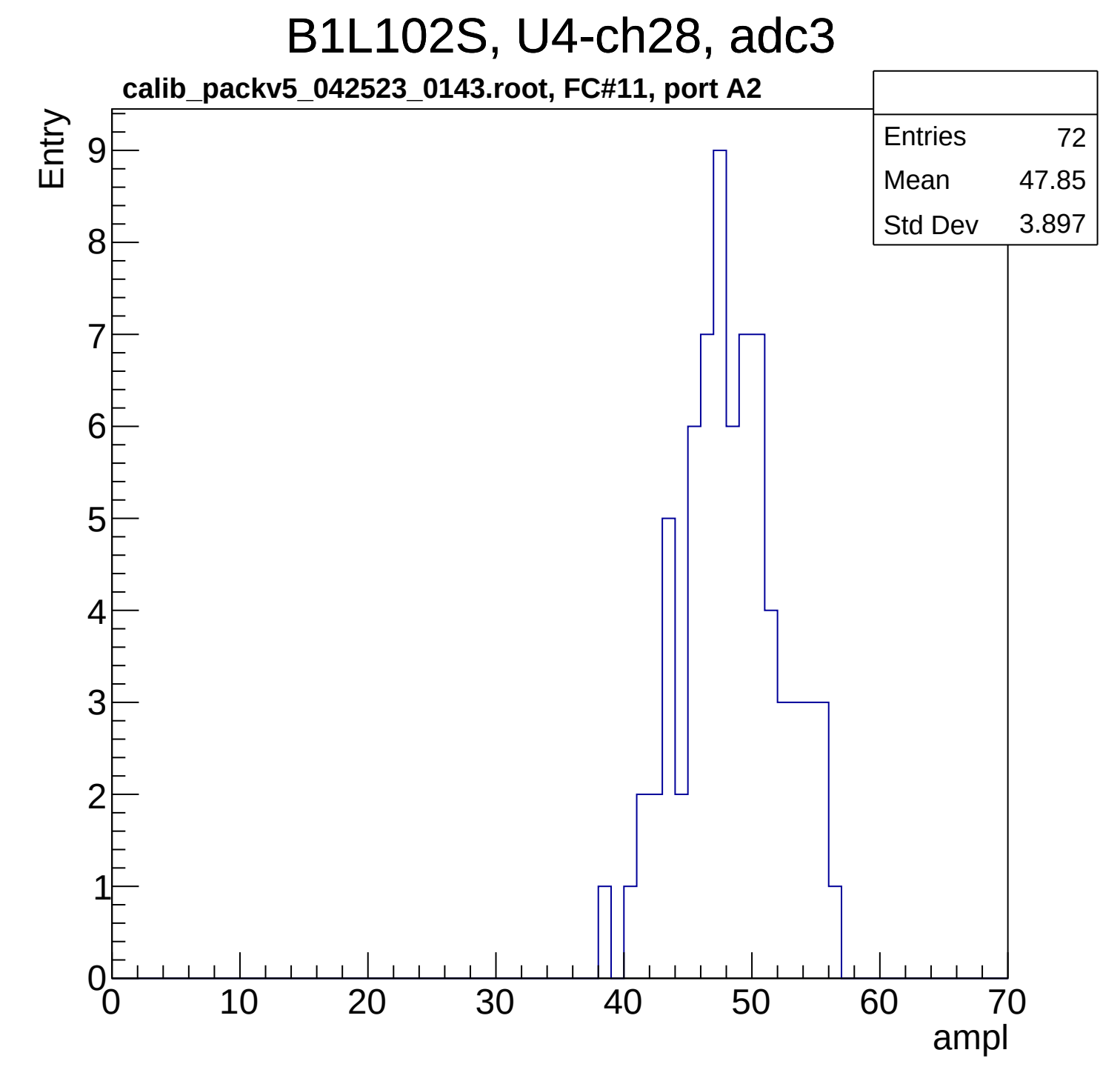
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch28, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 72
Mean 47.85
Std Dev 3.897
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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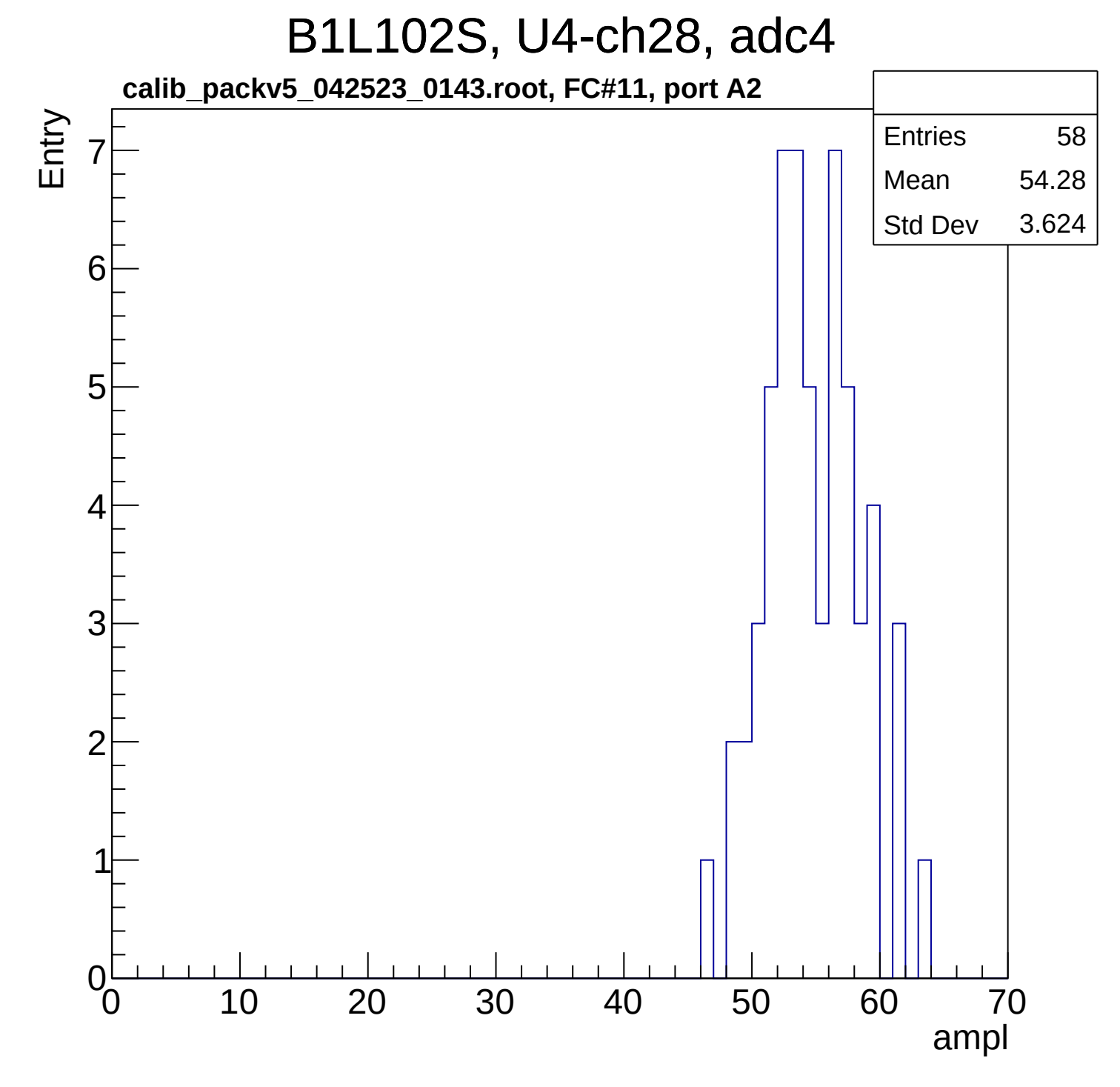
B1L102S, U4-ch28, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 54.28
Std Dev 3.624
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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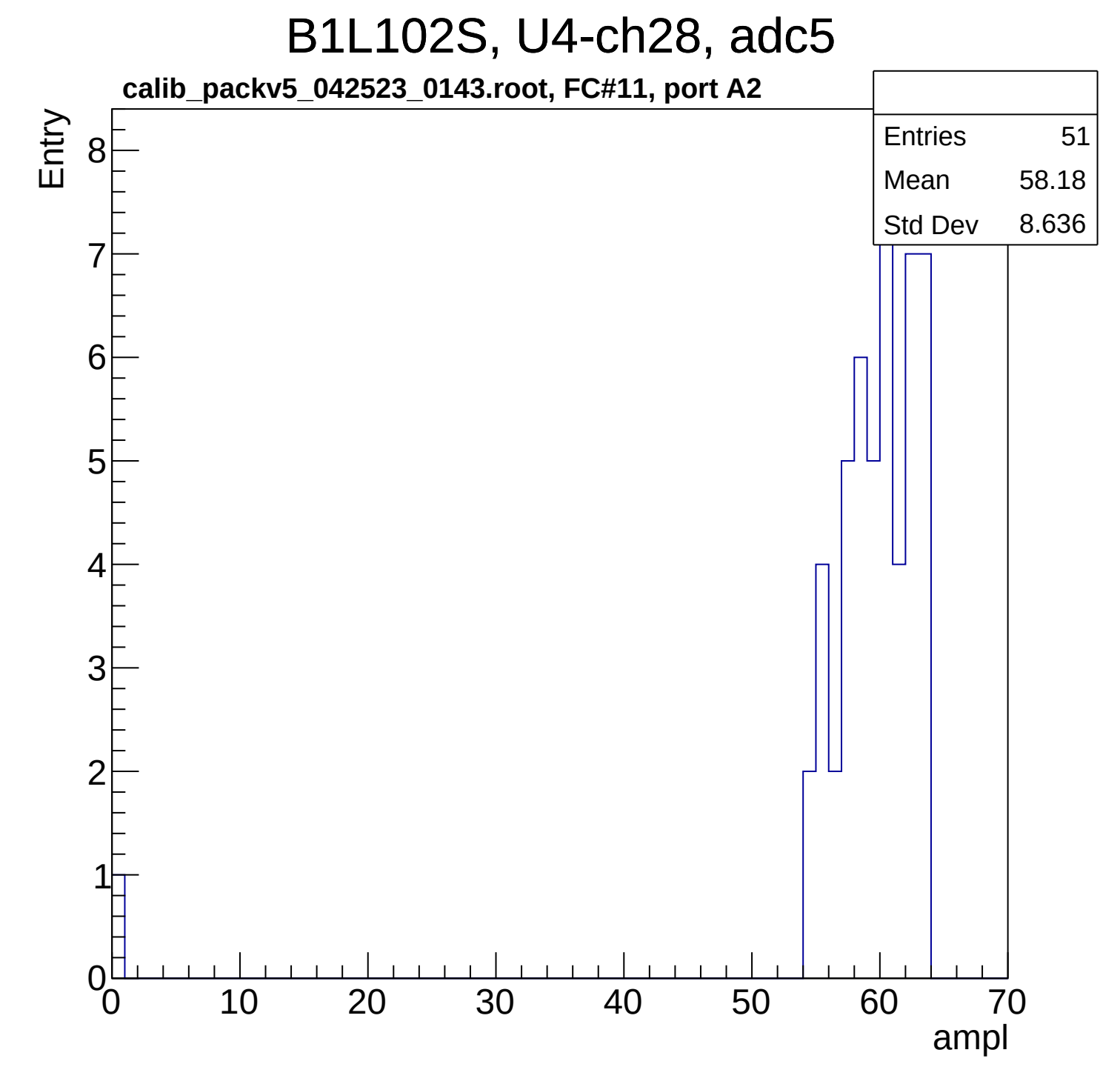
B1L102S, U4-ch28, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 58.18
Std Dev 8.636
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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60
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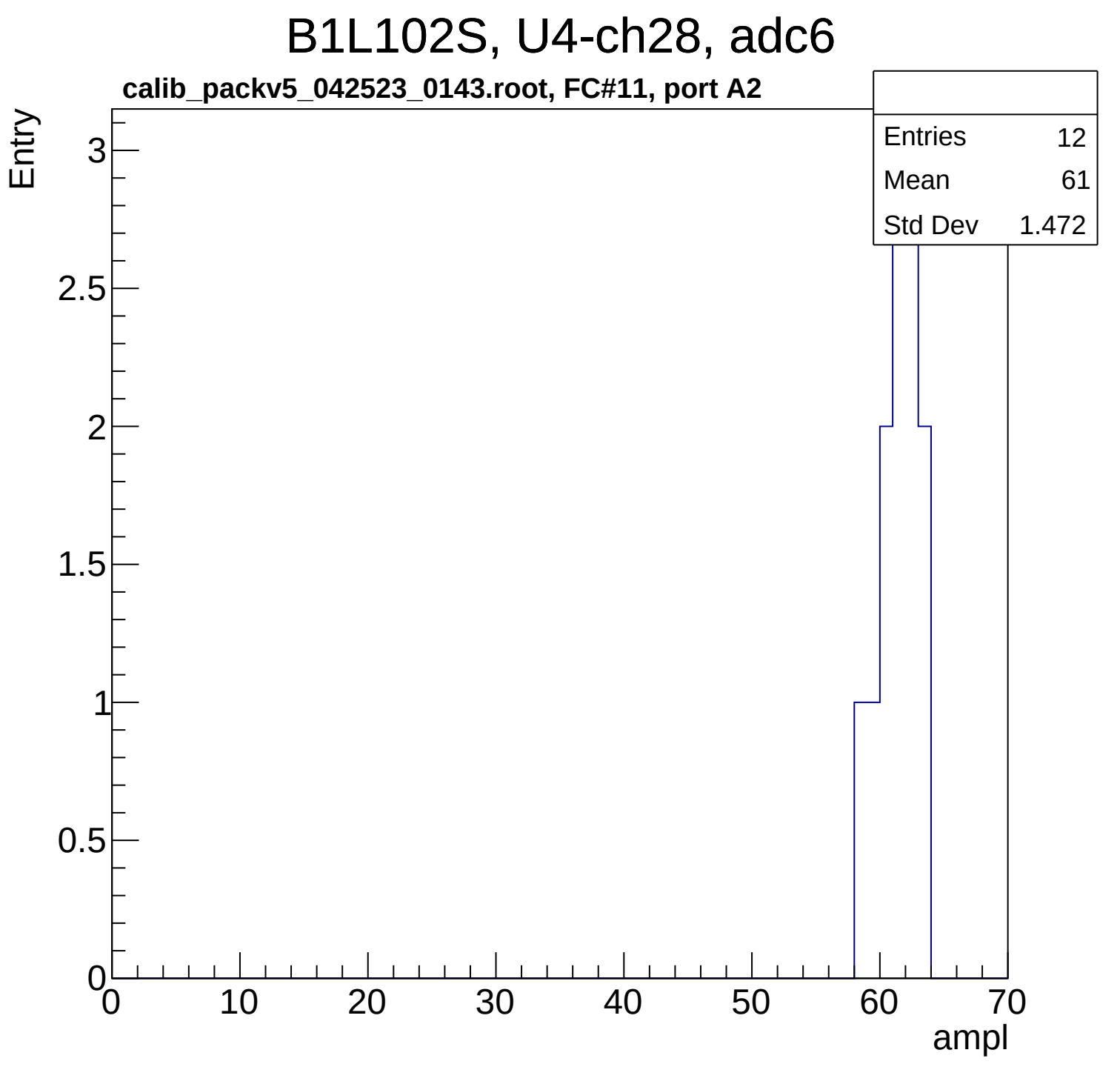
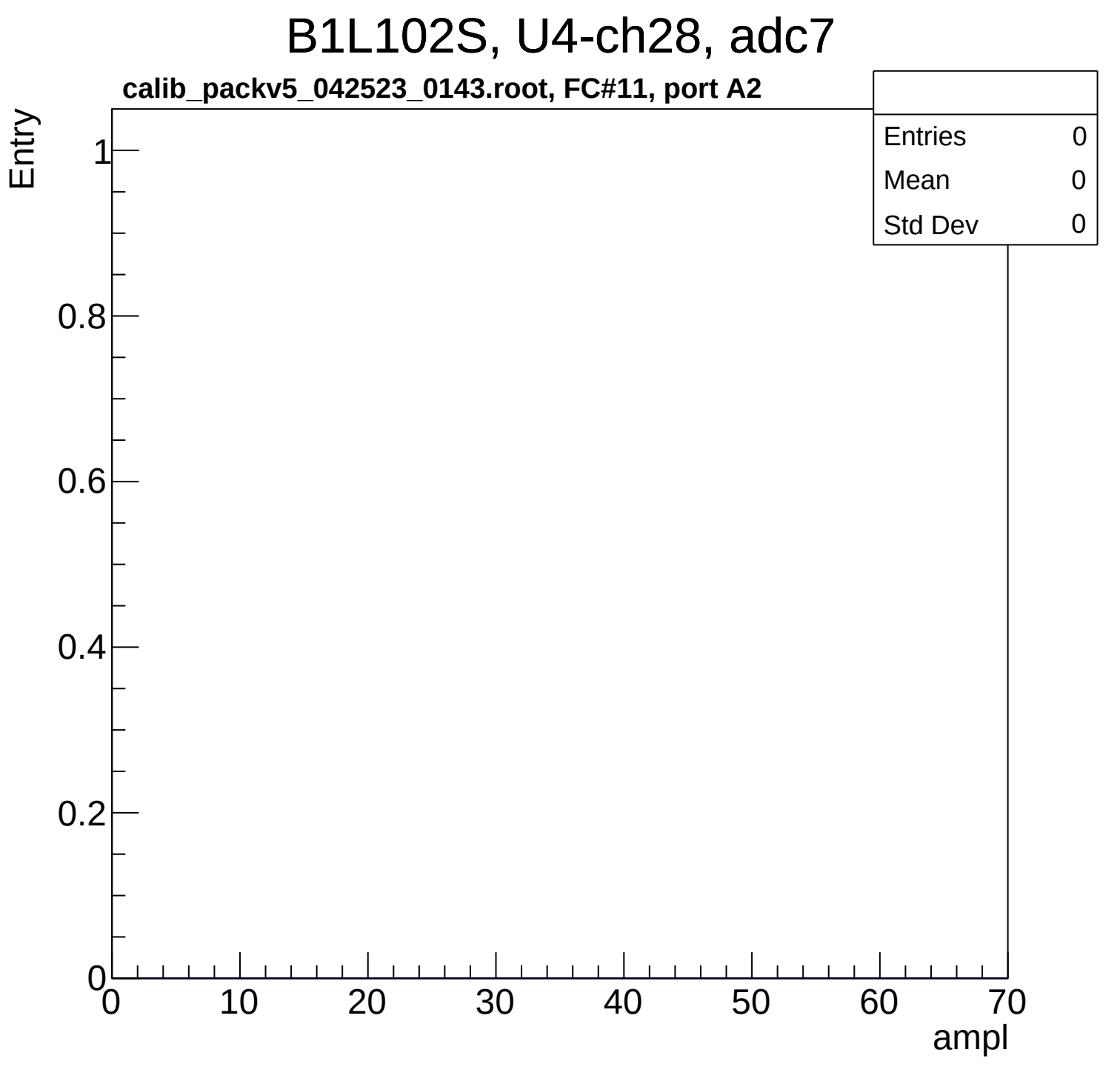
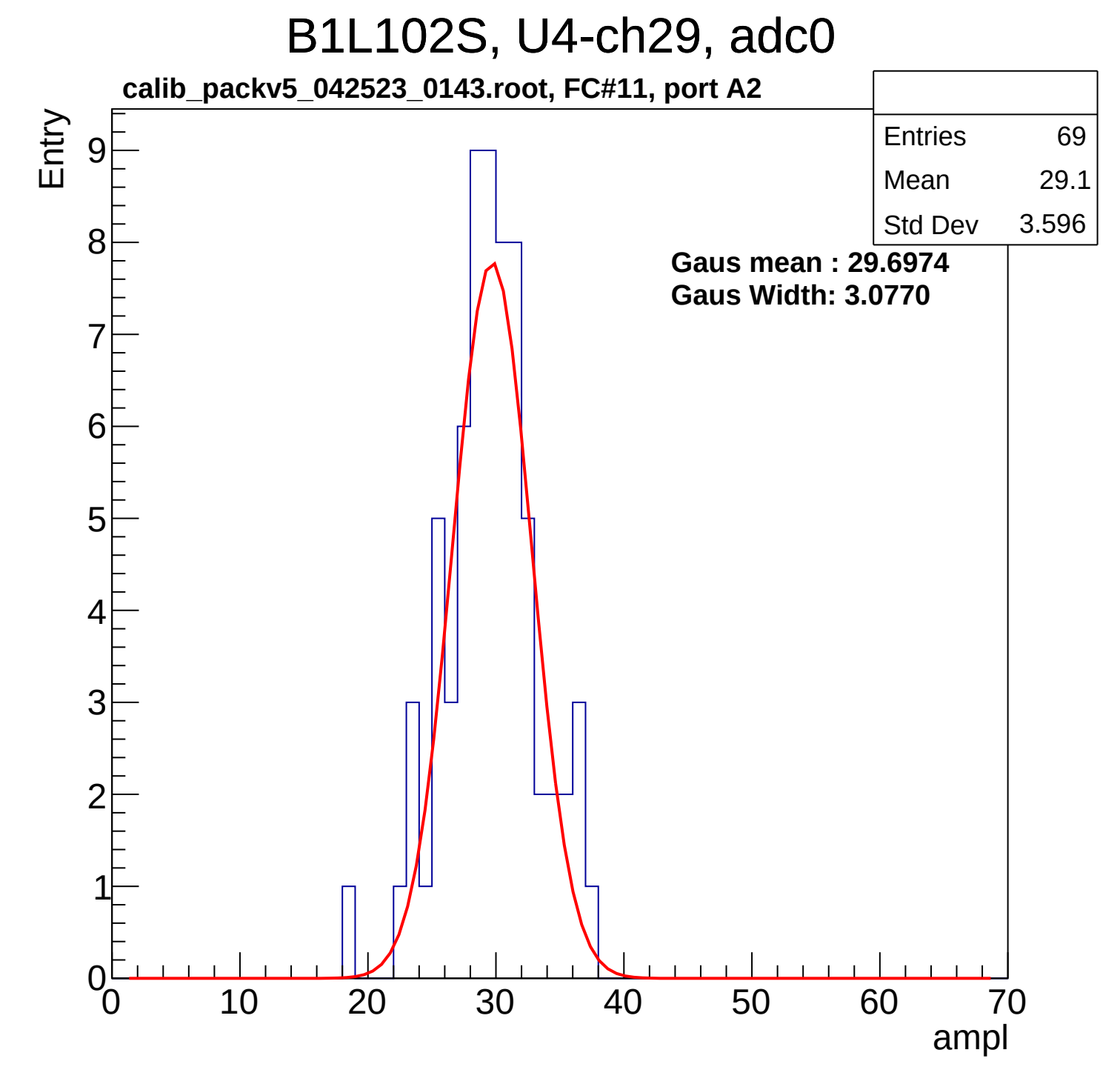

B1L102S, U4-ch28, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 12
Mean 61
Std Dev 1.472
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch28, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch29, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 29.1
Std Dev 3.596
Gaus mean : 29.6974
Gaus Width: 3.0770
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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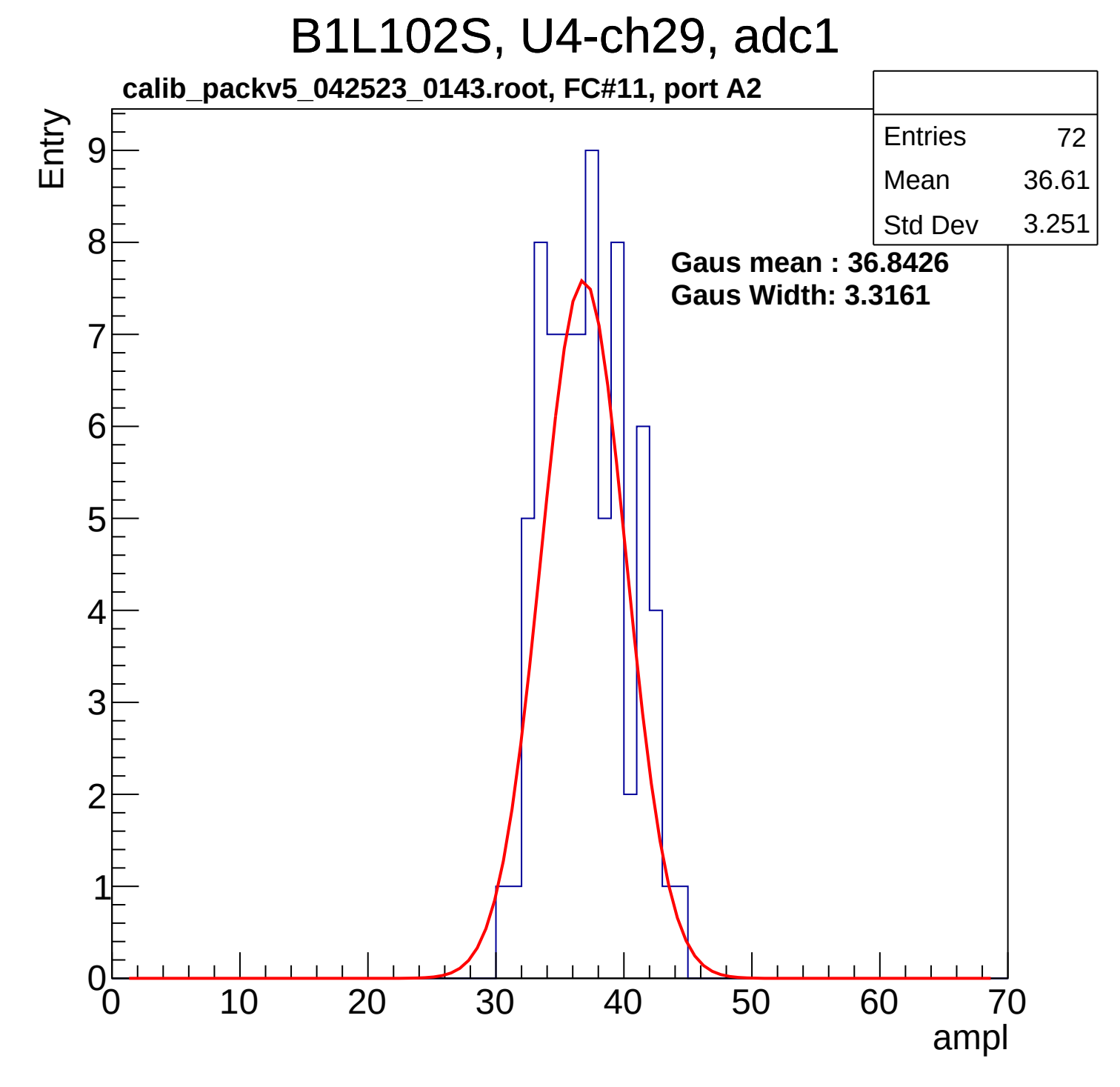
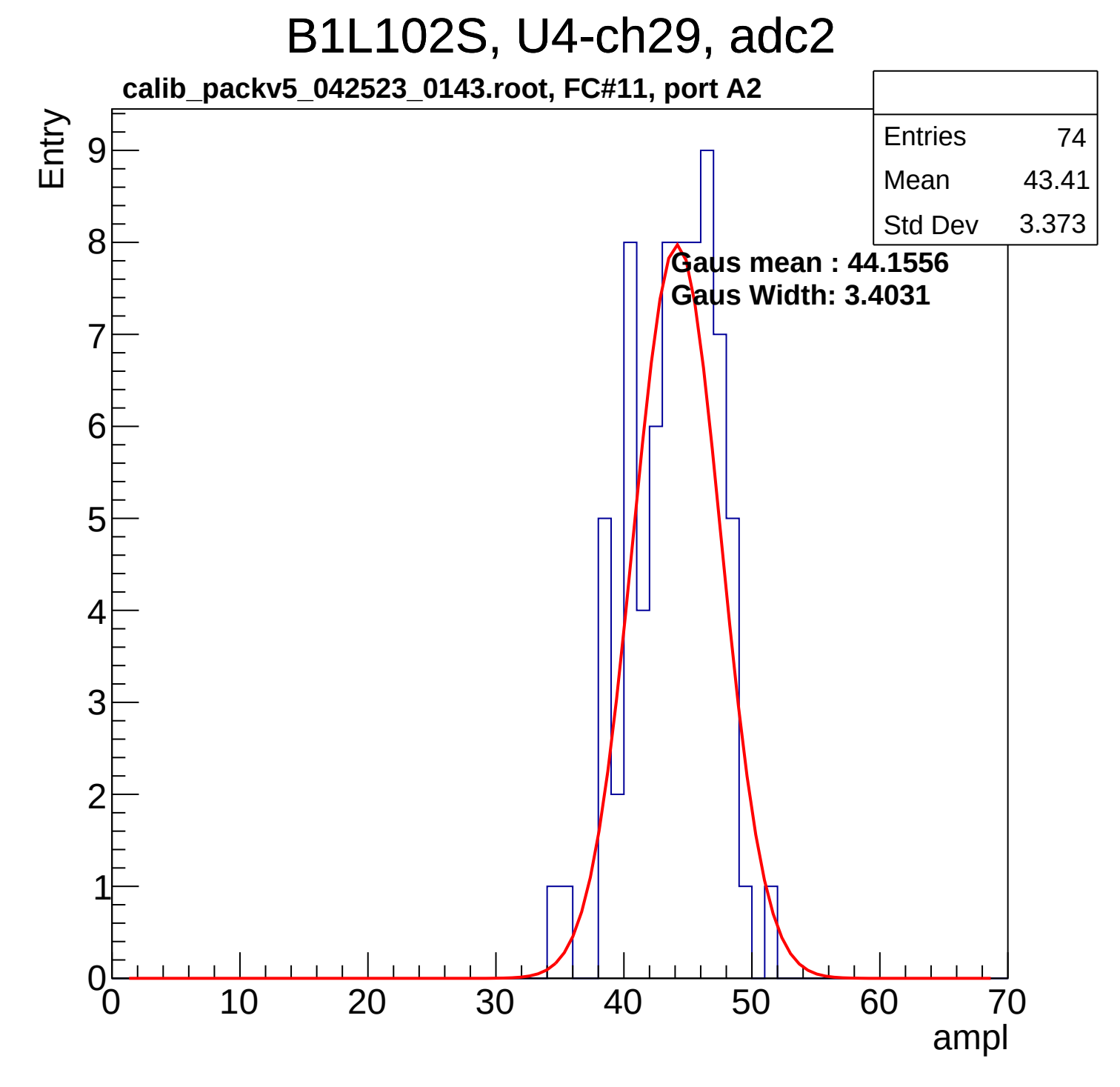
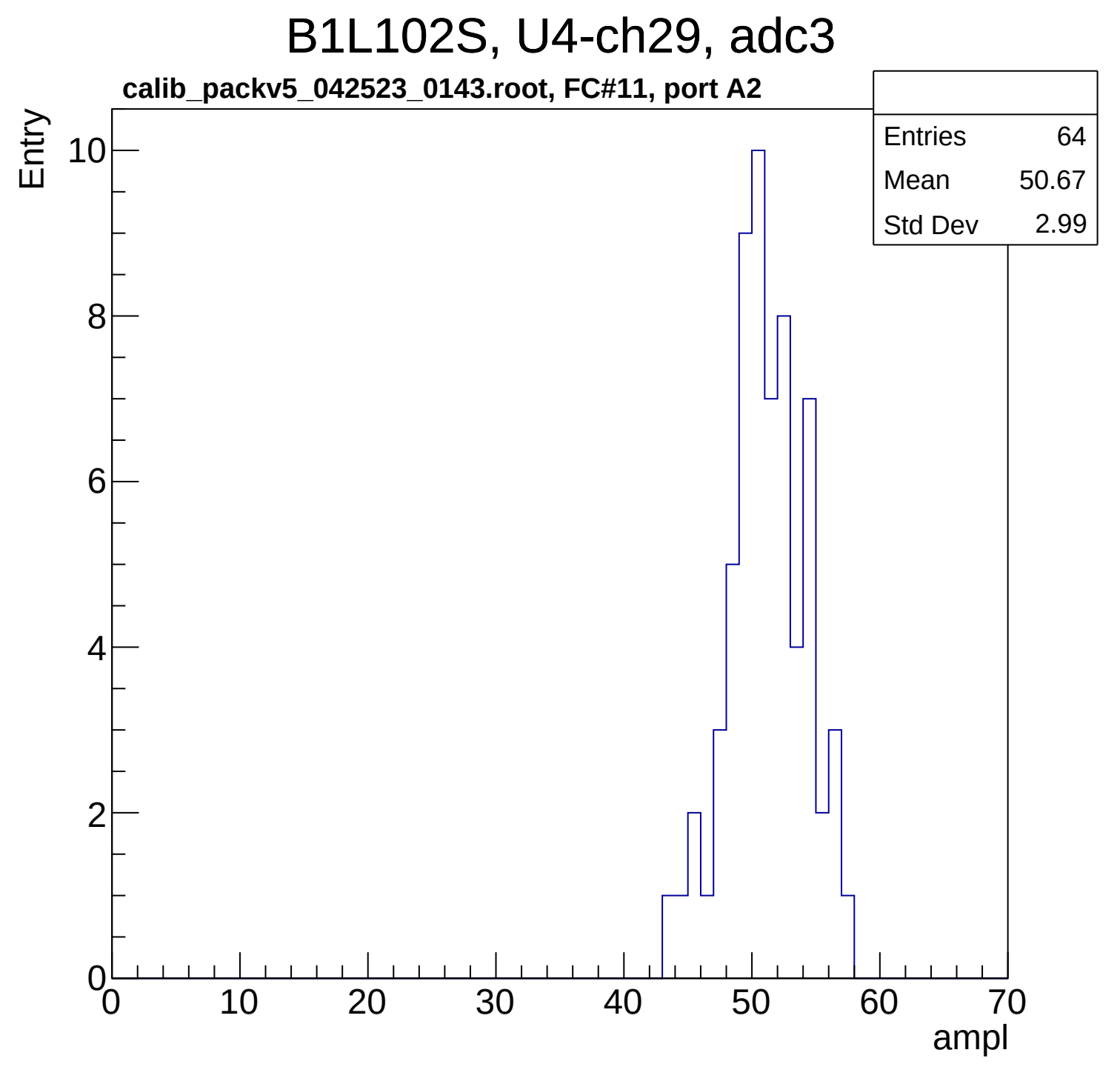
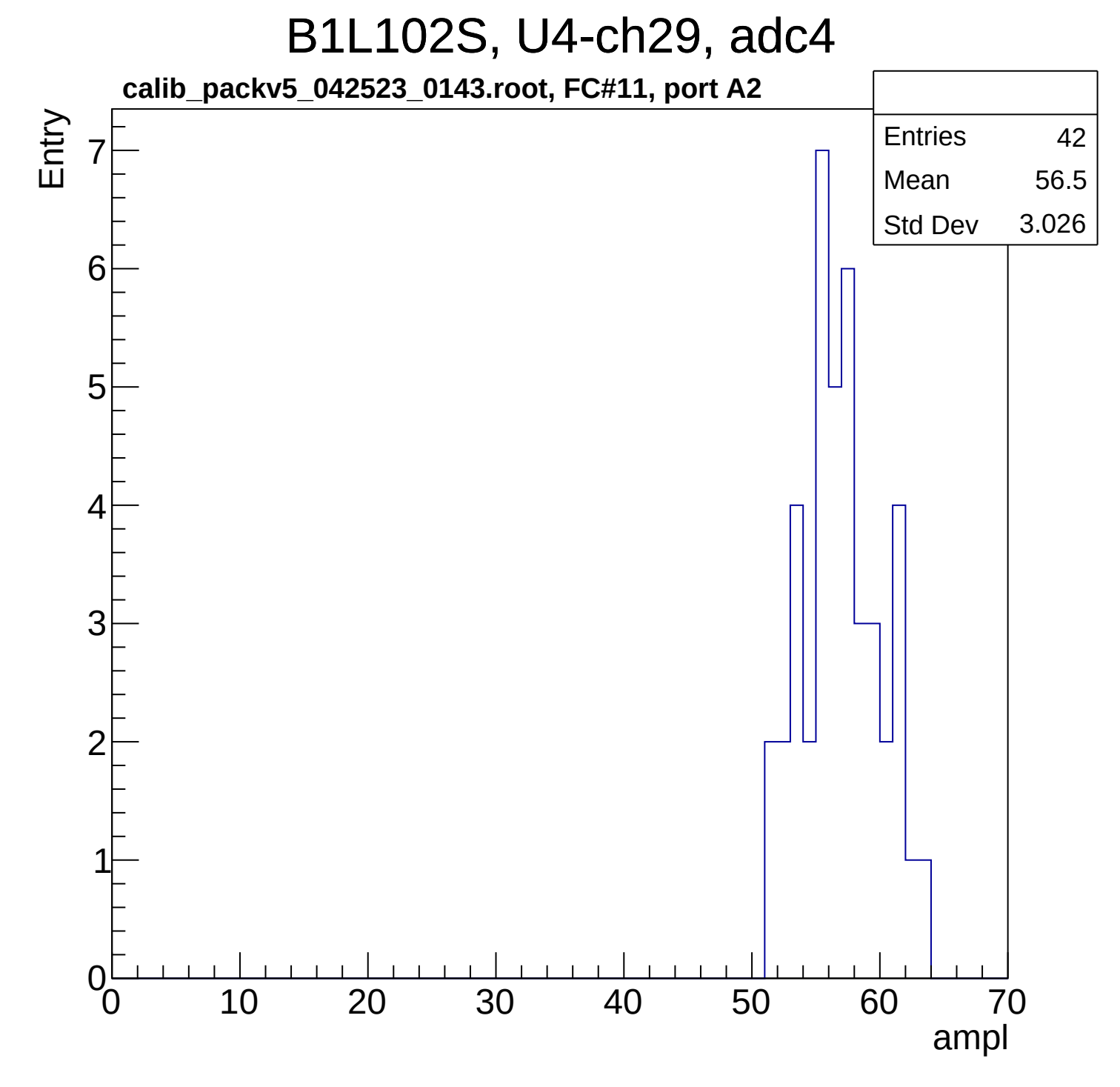

B1L102S, U4-ch29, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 72
Mean 36.61
Std Dev 3.251
Gaus mean : 36.8426
Gaus Width: 3.3161
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch29, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 43.41
Std Dev 3.373
Gaus mean : 44.1556
Gaus Width: 3.4031
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch29, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 50.67
Std Dev 2.99
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch29, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 42
Mean 56.5
Std Dev 3.026
Entry
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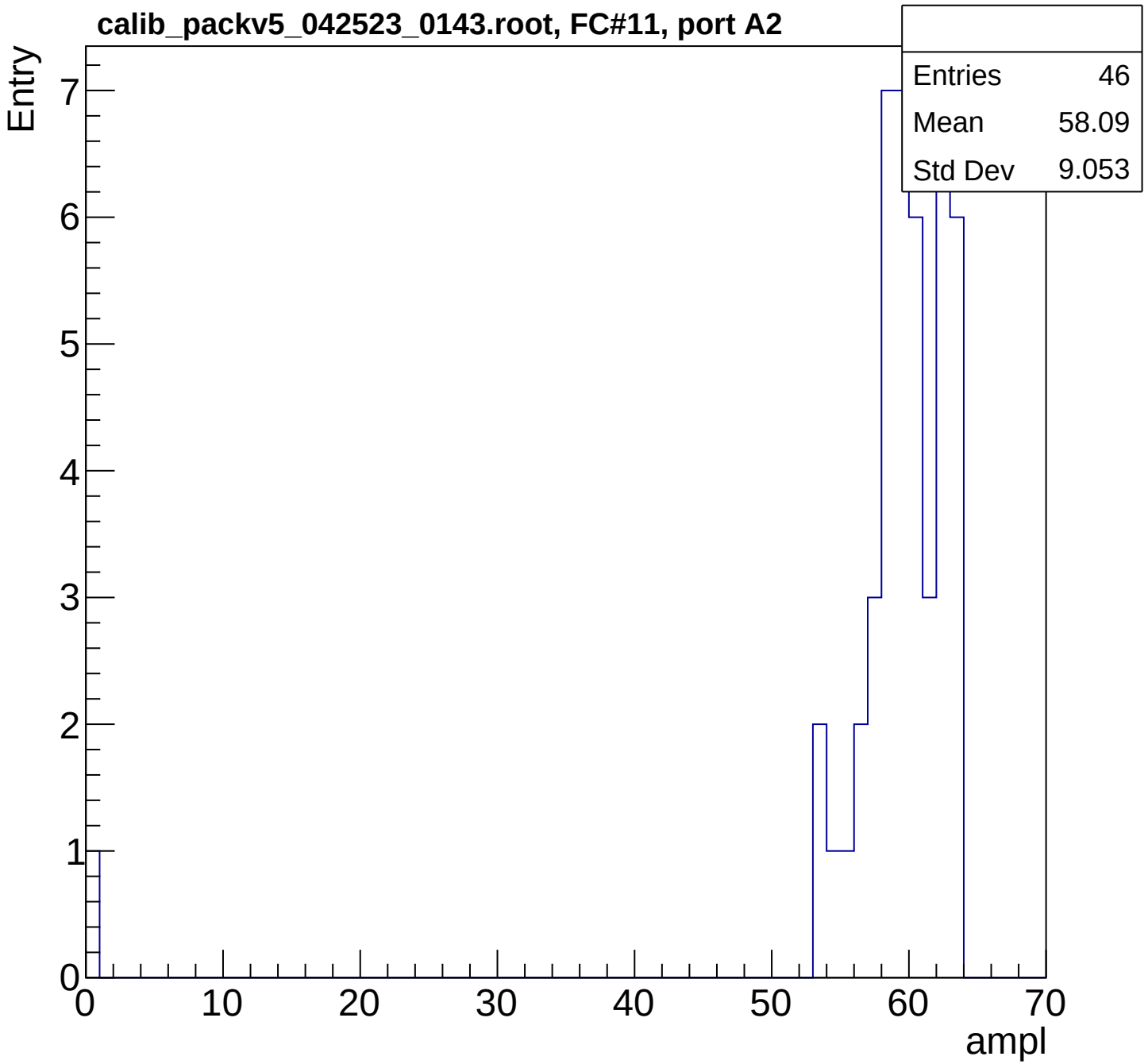
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch29, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 46
Mean 58.09
Std Dev 9.053
Entry
ampl
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1
2
3
4
5
6
7
0
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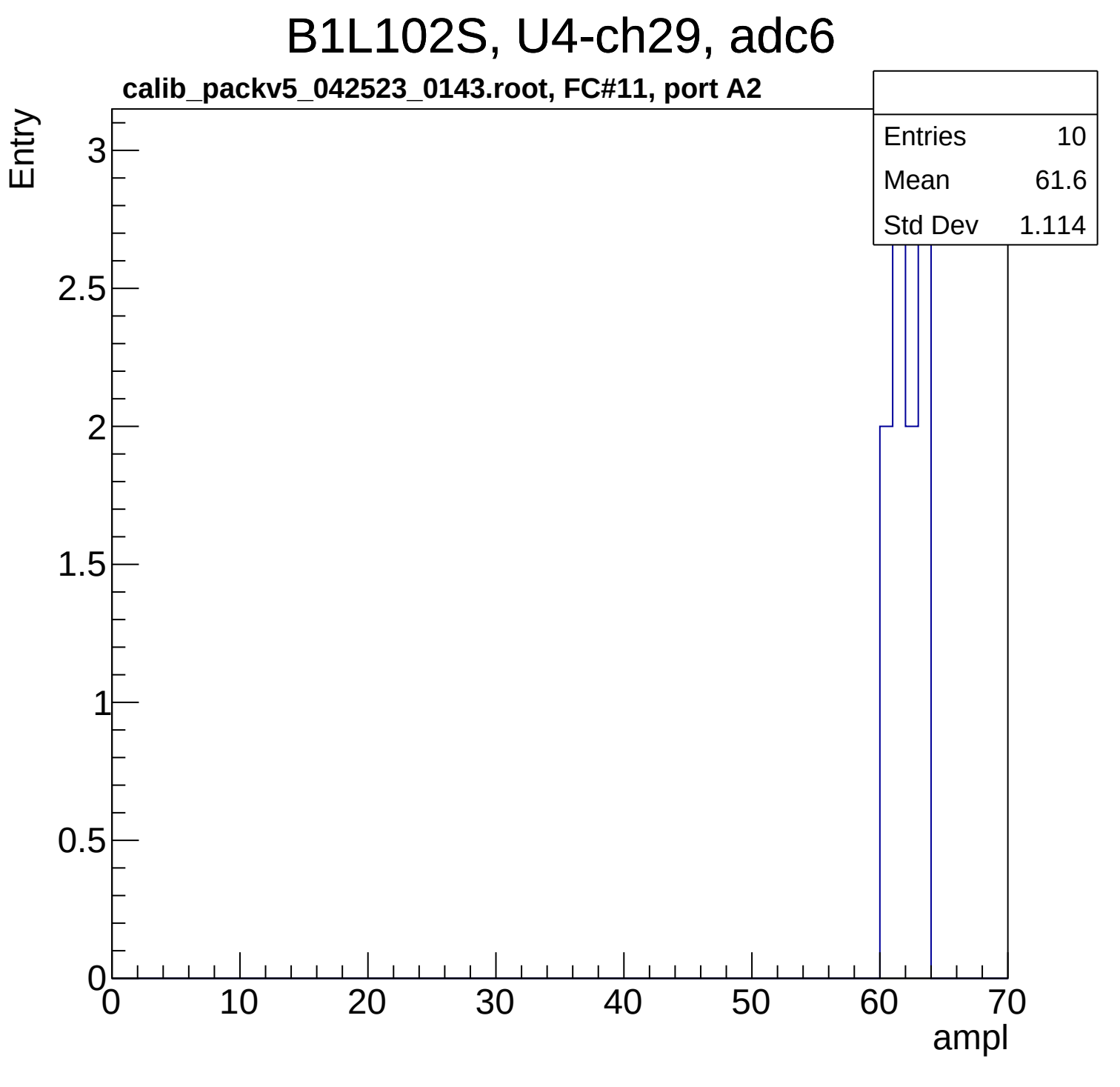
20
30
40
50
60
70


B1L102S, U4-ch29, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 10
Mean 61.6
Std Dev 1.114
Entry
ampl
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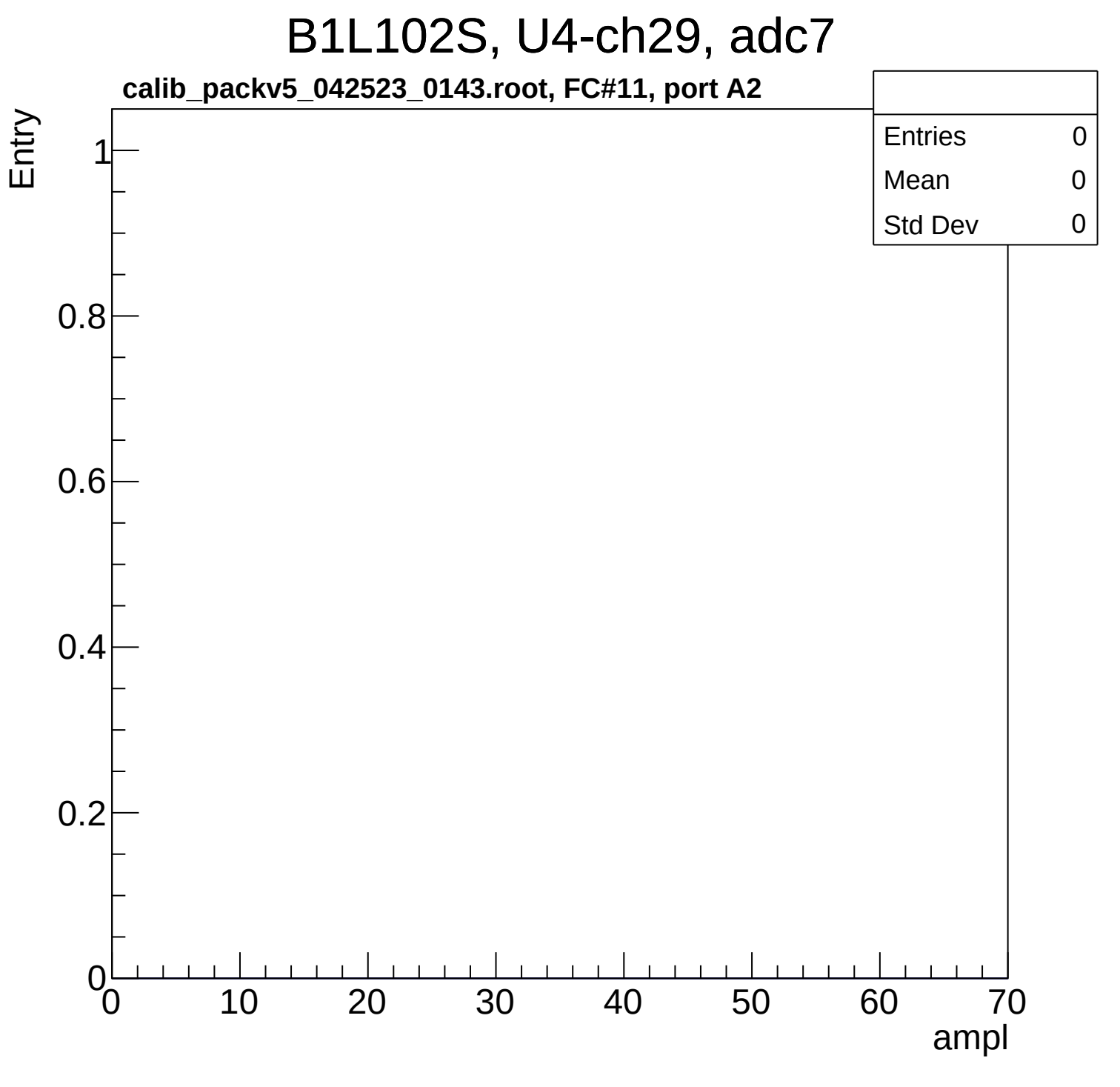
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U4-ch29, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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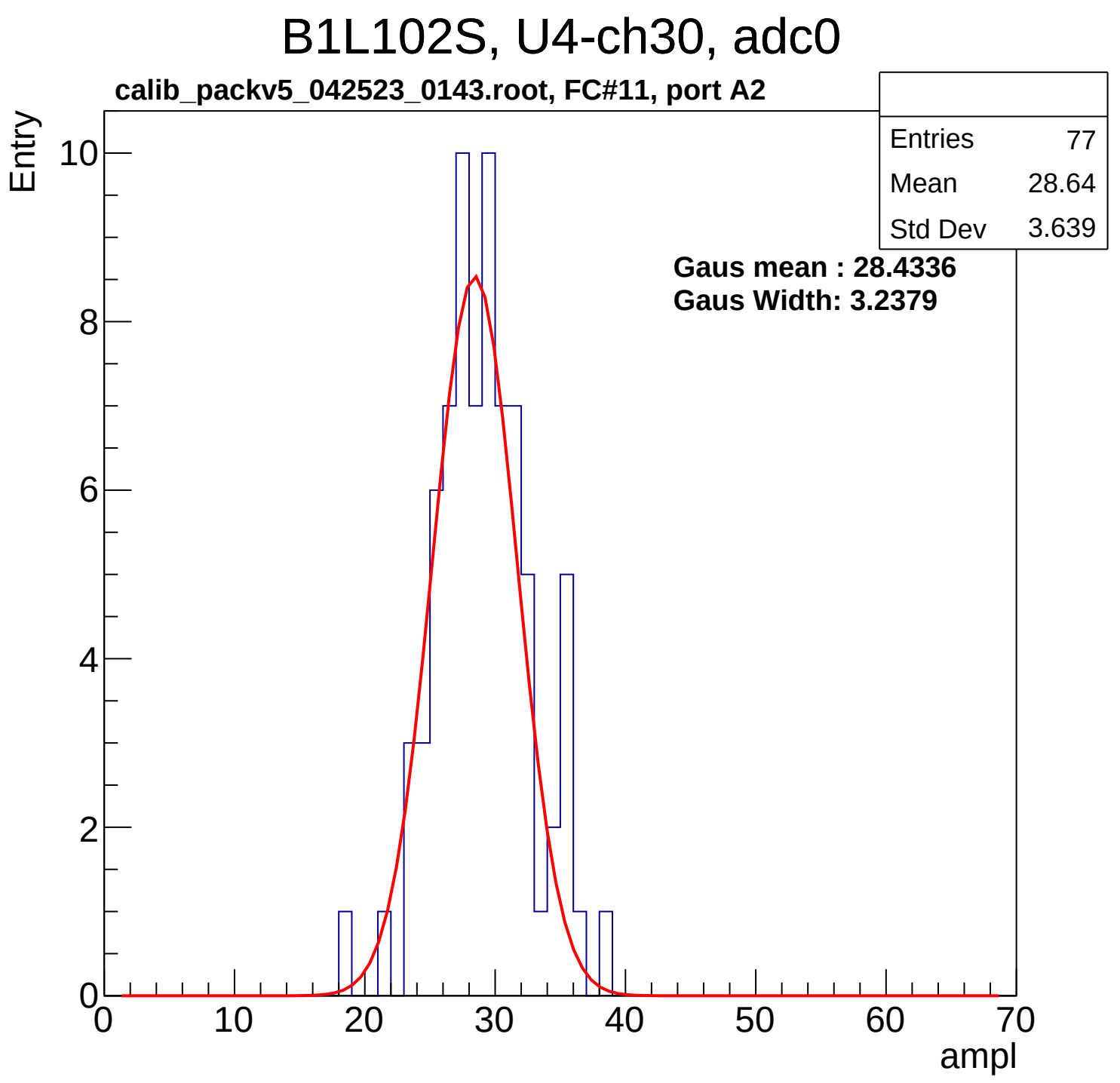
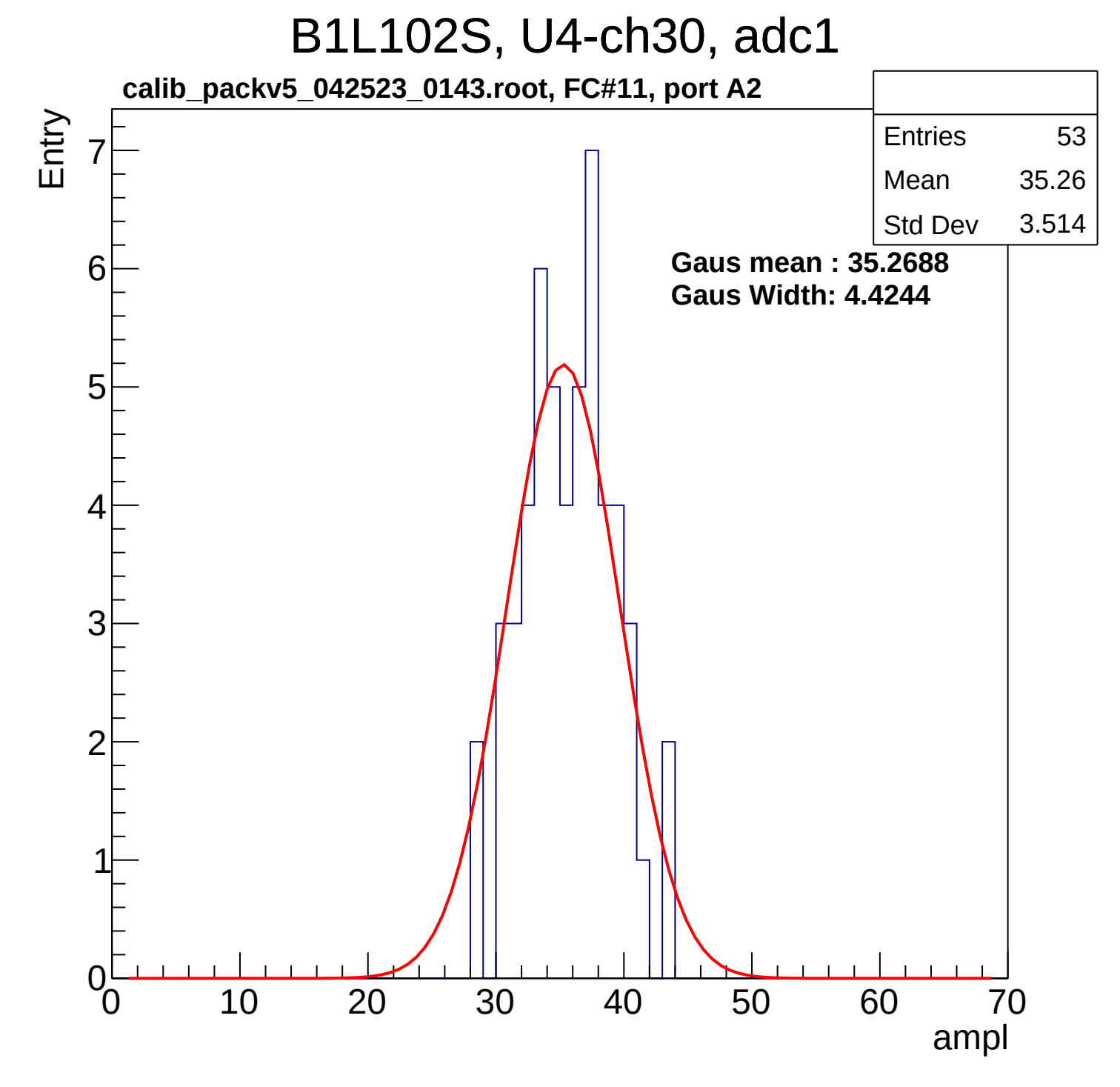
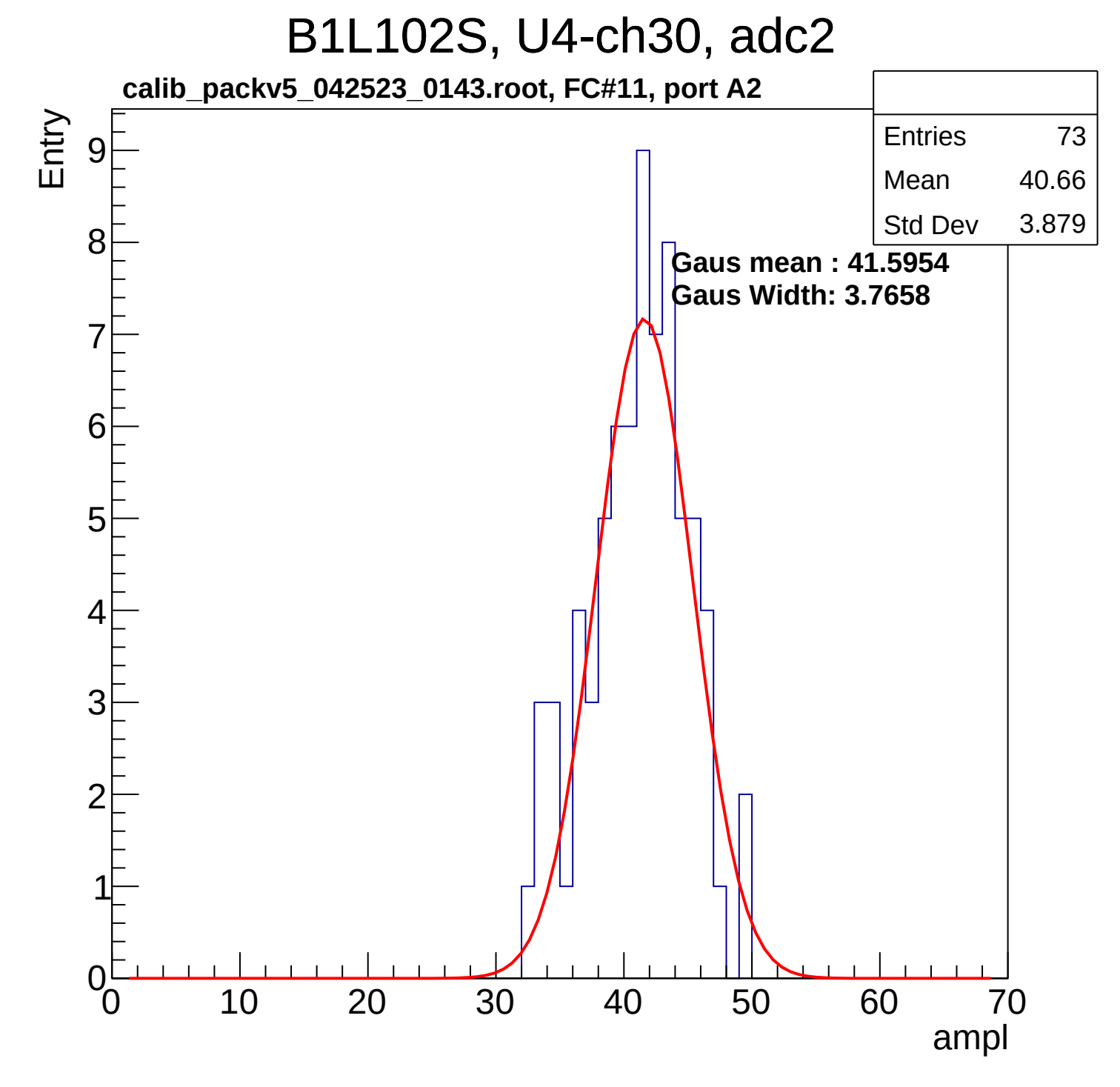
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch30, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 77
Mean 28.64
Std Dev 3.639
Gaus mean : 28.4336
Gaus Width: 3.2379
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch30, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 35.26
Std Dev 3.514
Gaus mean : 35.2688
Gaus Width: 4.4244
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch30, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 40.66
Std Dev 3.879
Gaus mean : 41.5954
Gaus Width: 3.7658
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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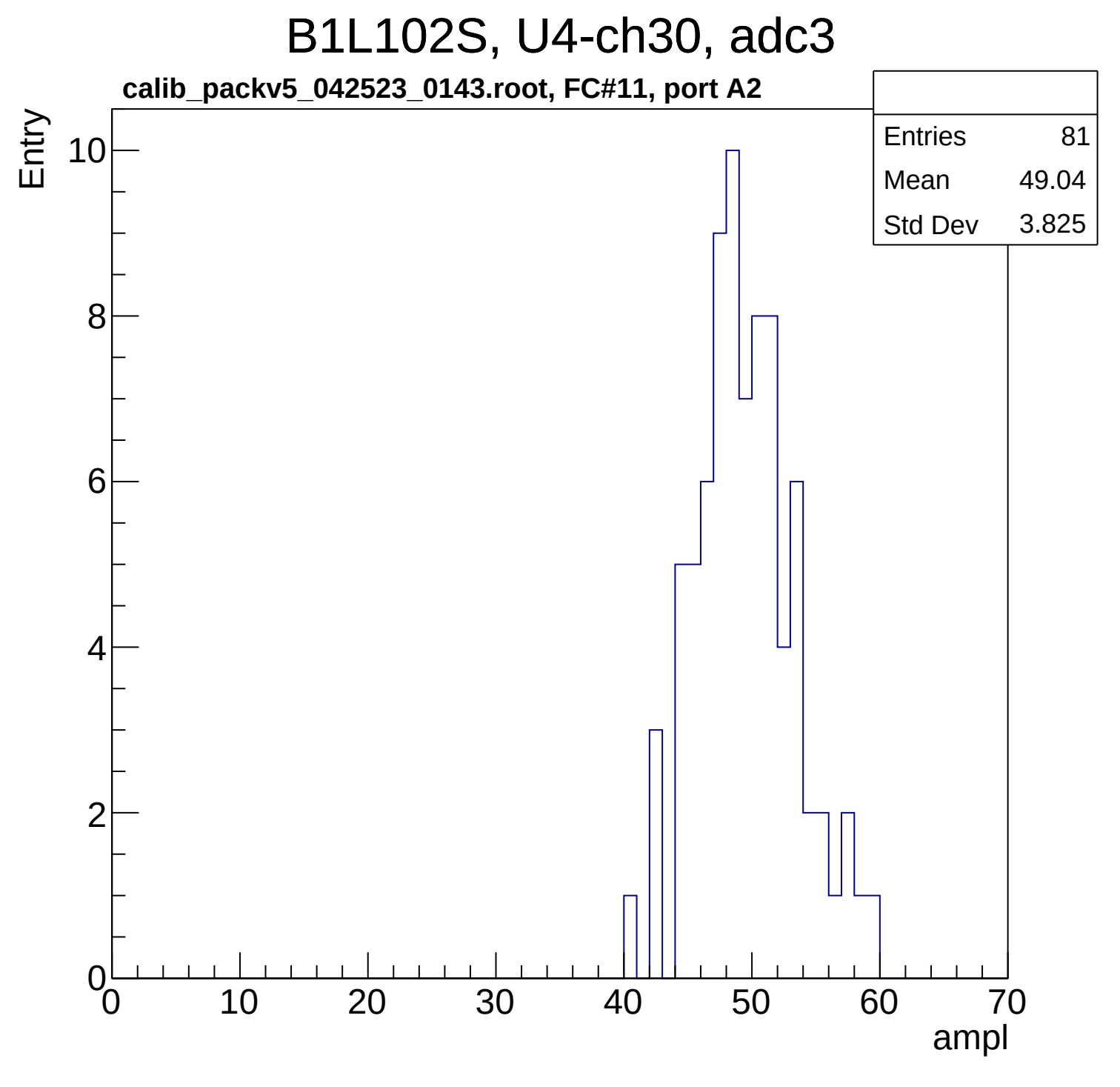
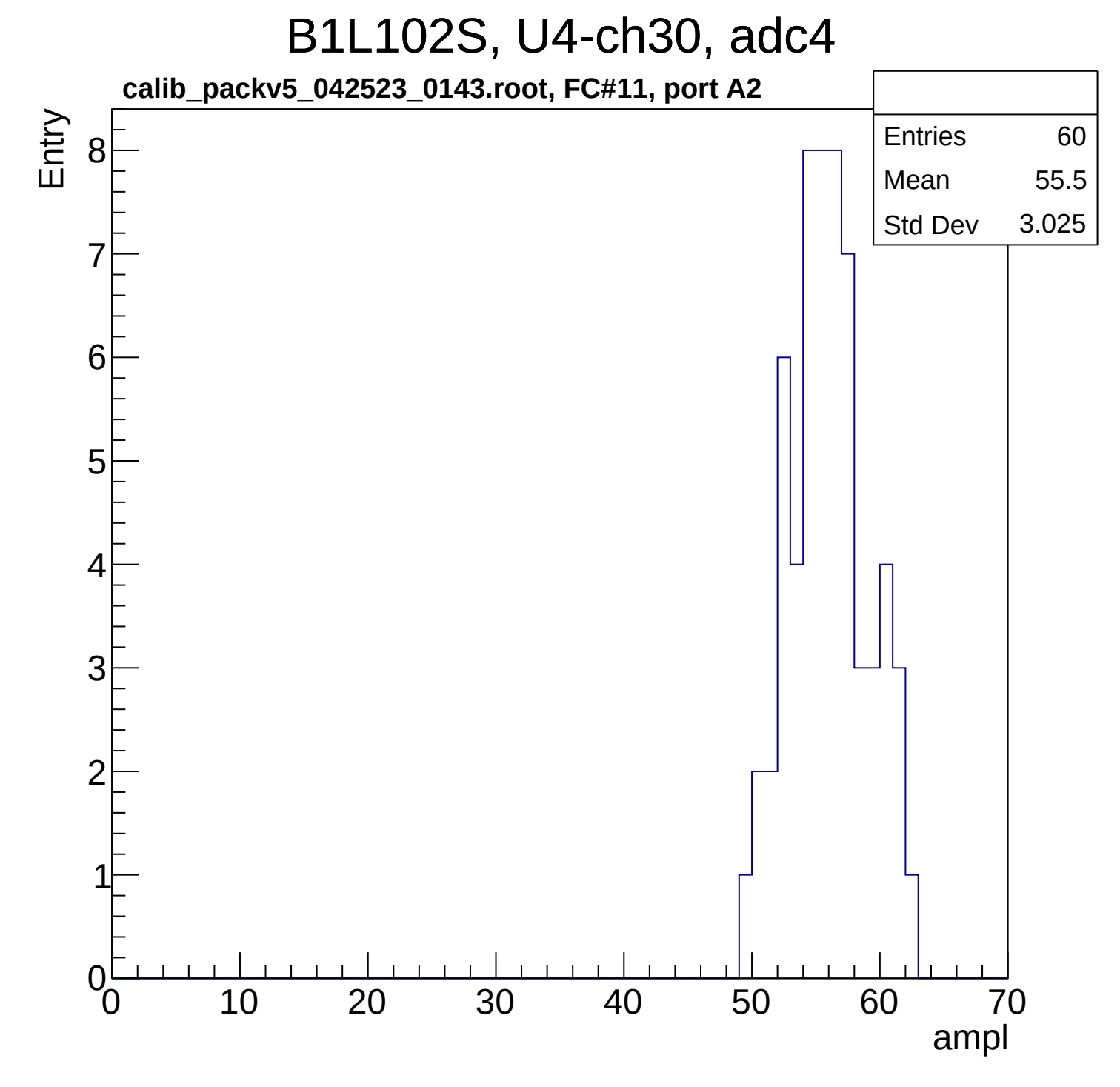

B1L102S, U4-ch30, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 81
Mean 49.04
Std Dev 3.825
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch30, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 55.5
Std Dev 3.025
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
50
60
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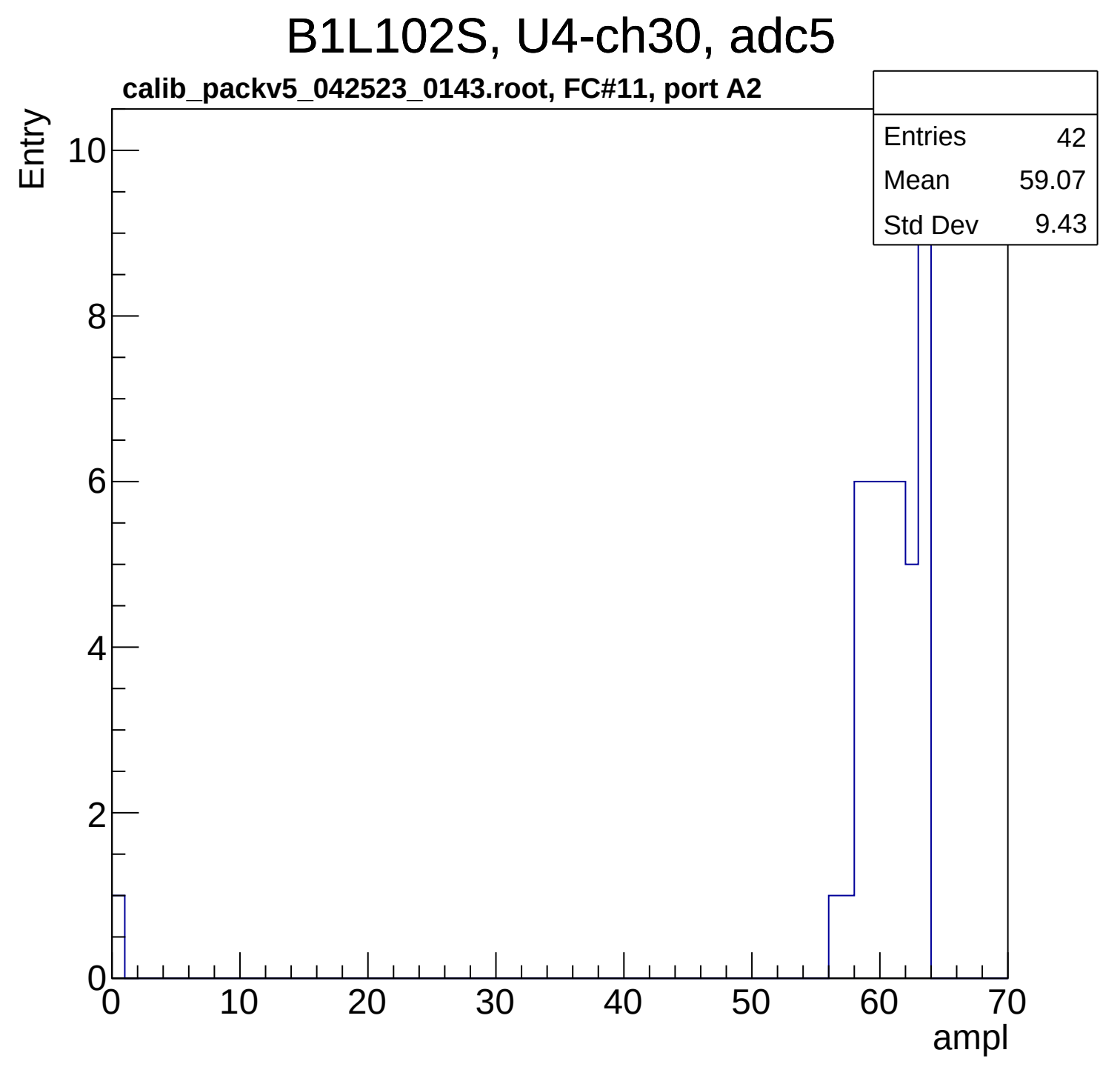
B1L102S, U4-ch30, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 42
Mean 59.07
Std Dev 9.43
Entry
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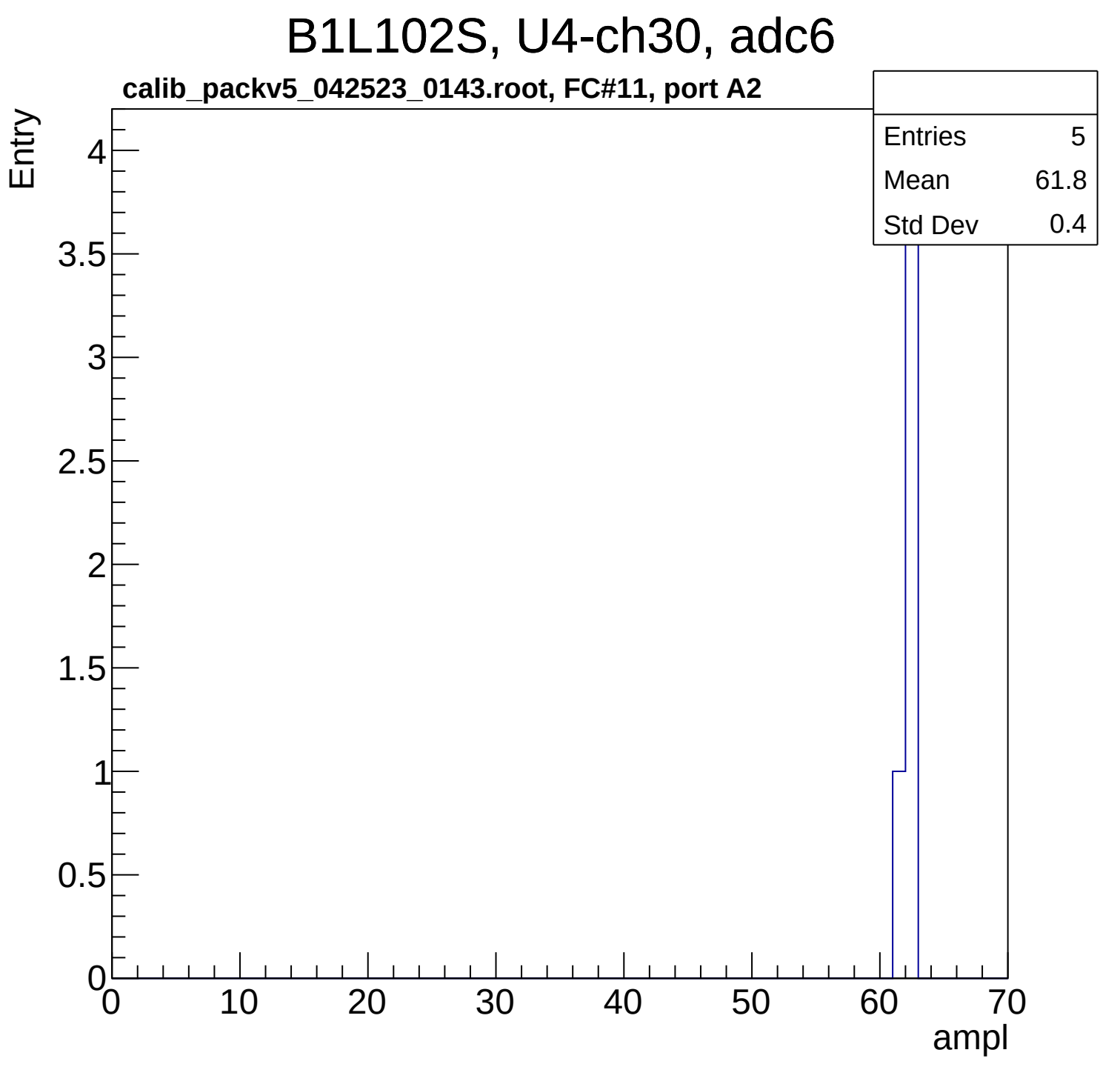
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch30, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 5
Mean 61.8
Std Dev 0.4
Entry
ampl
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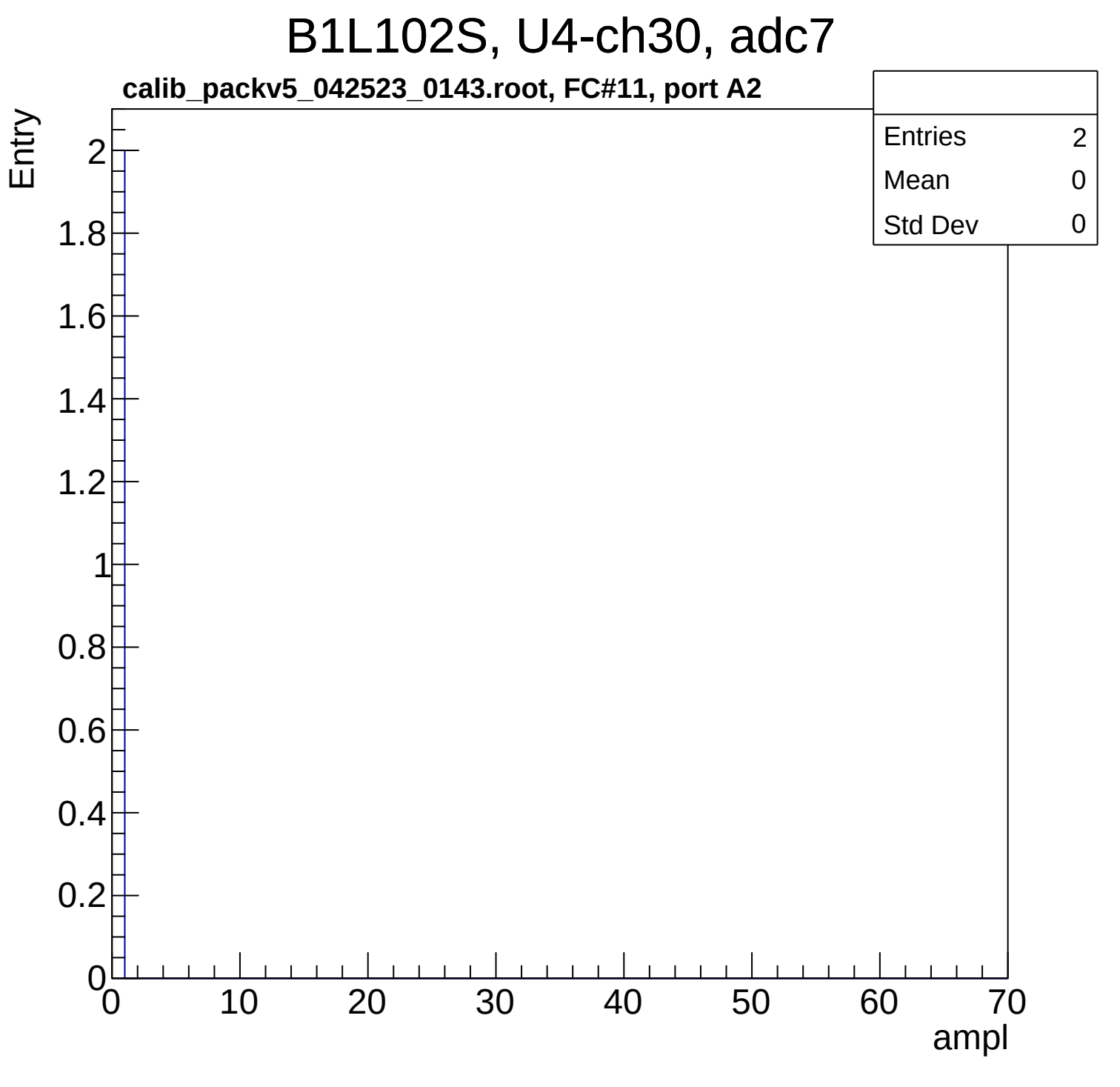
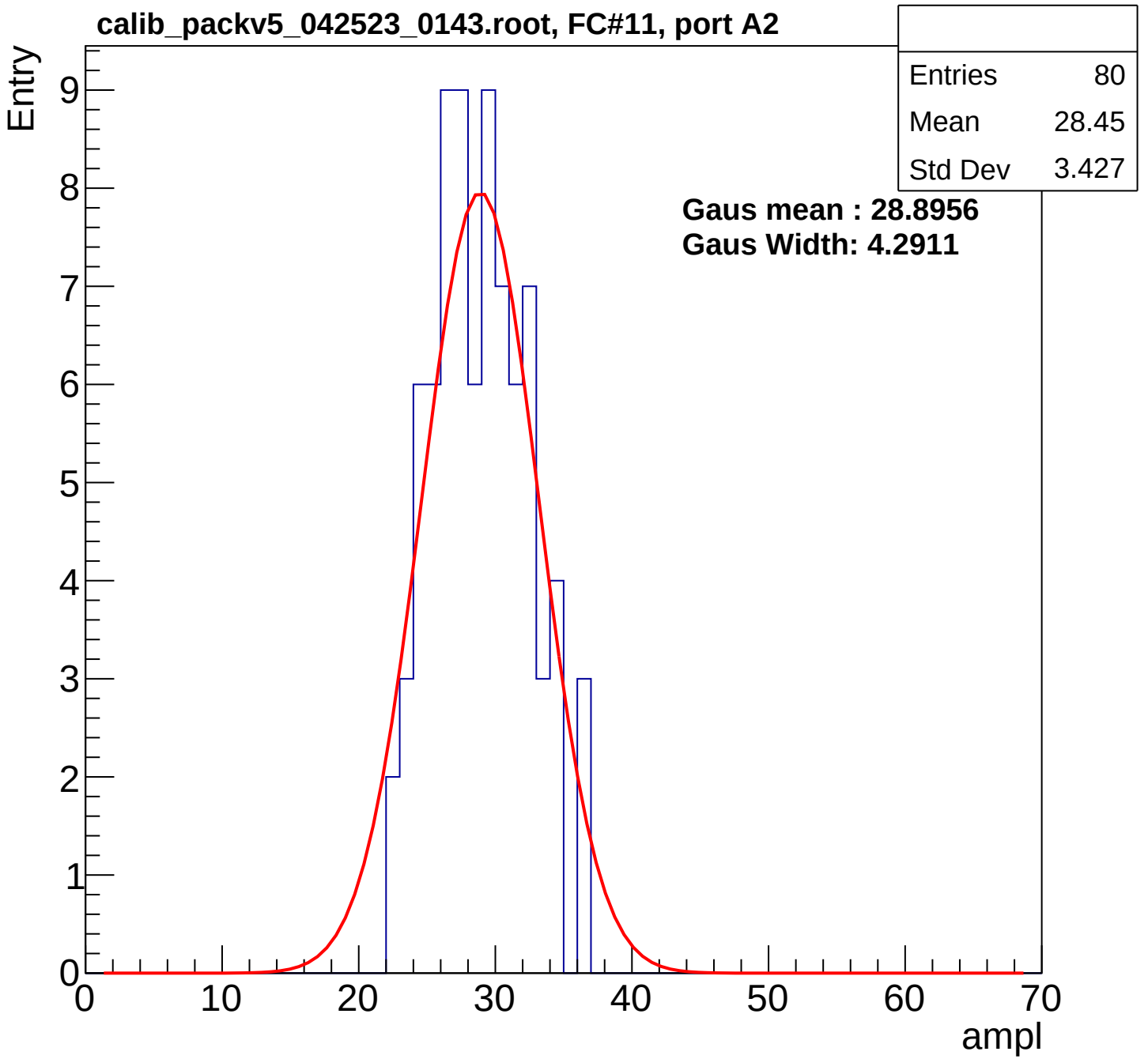
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U4-ch30, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L102S, U4-ch31, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 80
Mean 28.45
Std Dev 3.427
Gaus mean : 28.8956
Gaus Width: 4.2911
Entry
ampl
0
1
2
3
4
5
6
7
8
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0
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40
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60
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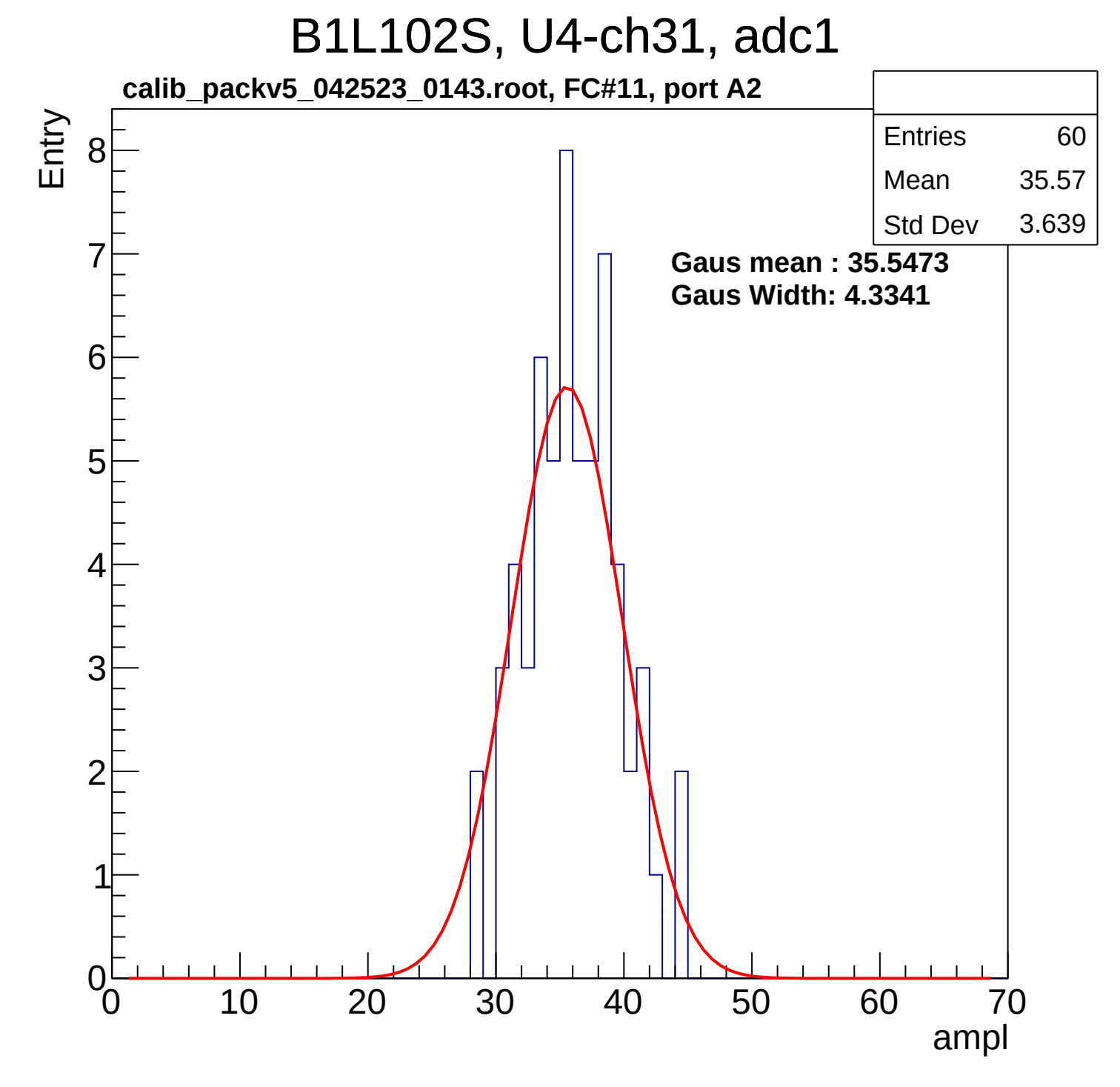
B1L102S, U4-ch31, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 35.57
Std Dev 3.639
Gaus mean : 35.5473
Gaus Width: 4.3341
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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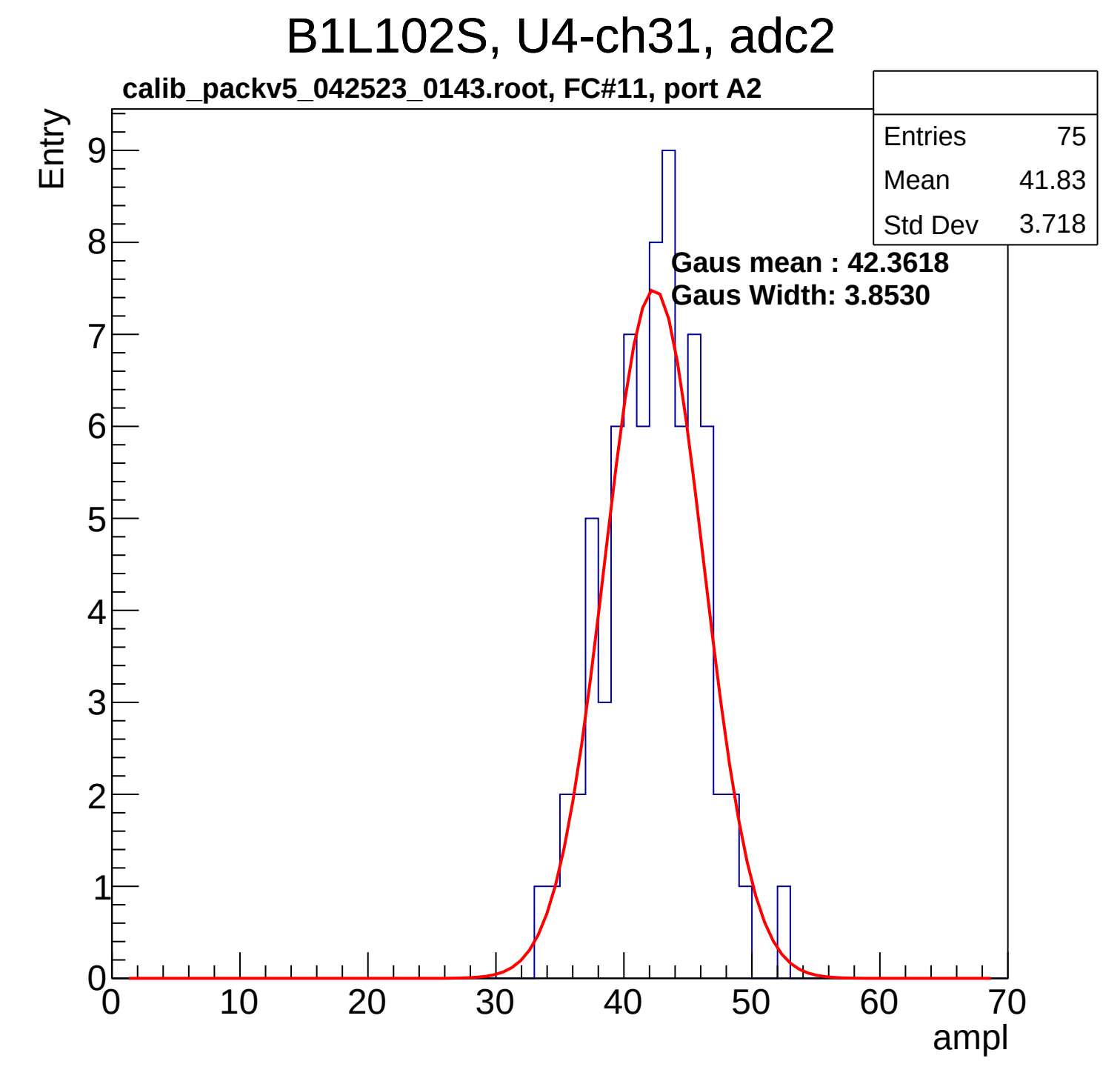
B1L102S, U4-ch31, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 41.83
Std Dev 3.718
Gaus mean : 42.3618
Gaus Width: 3.8530
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
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40
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60
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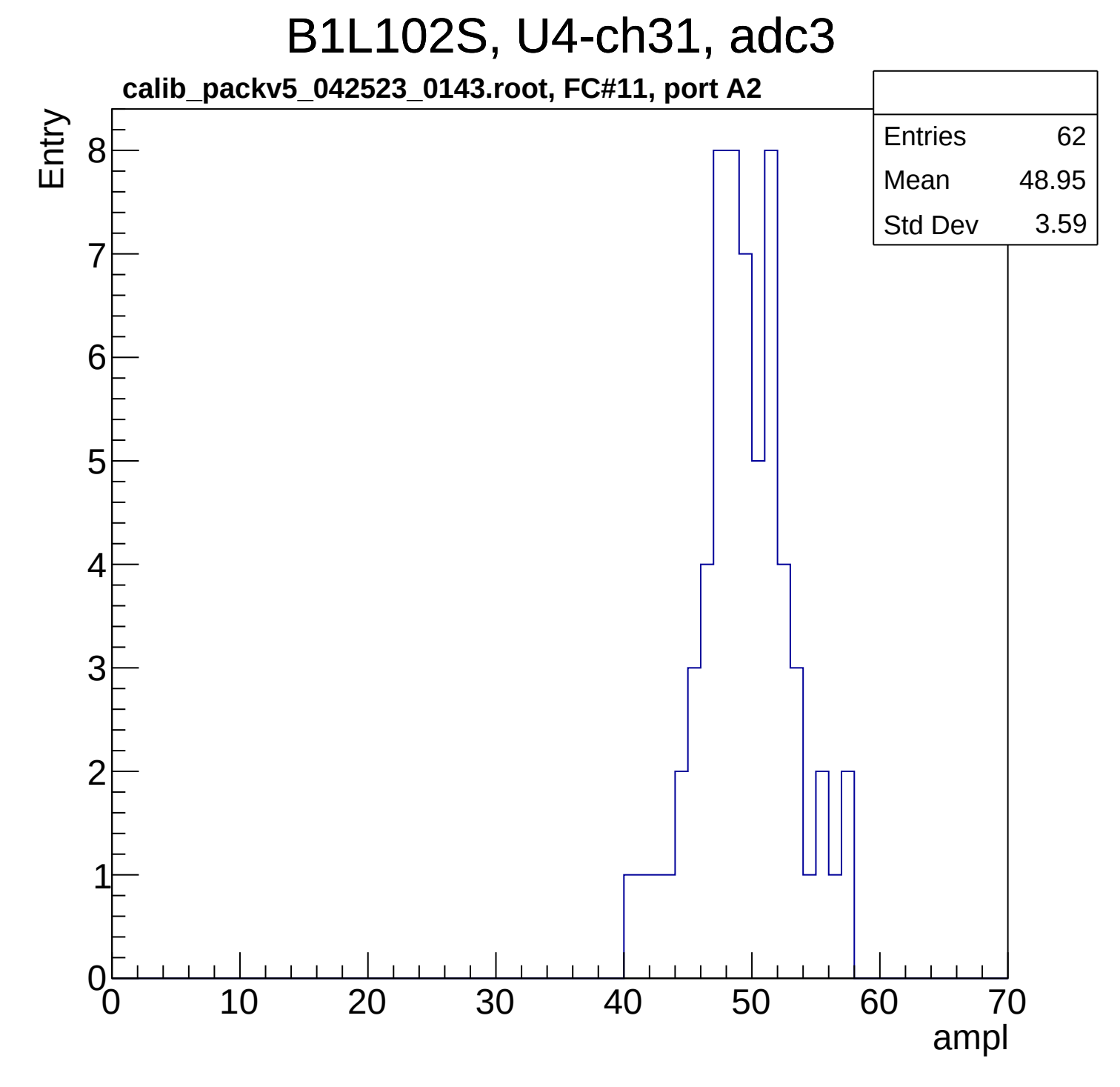
B1L102S, U4-ch31, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 48.95
Std Dev 3.59
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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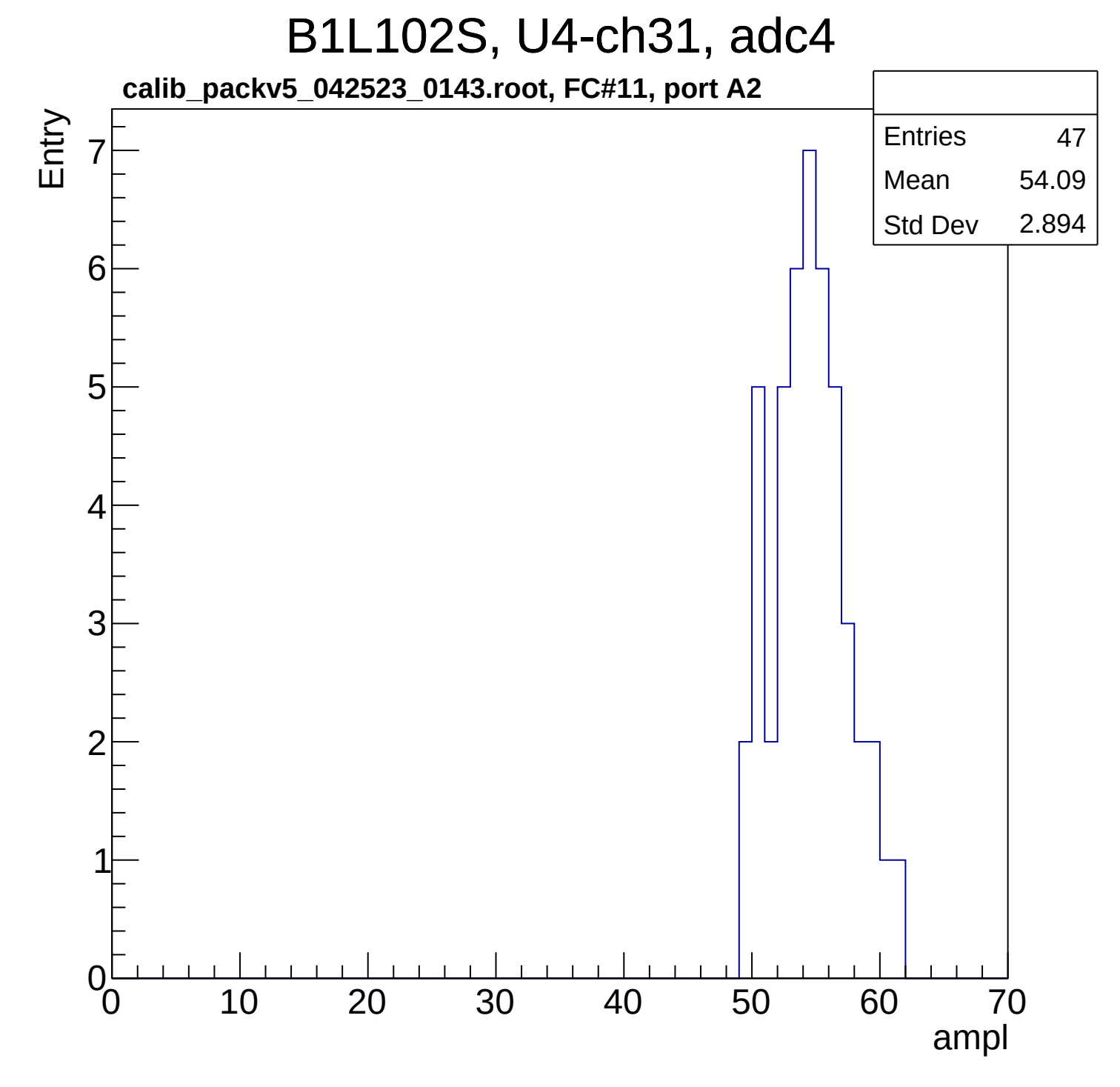
B1L102S, U4-ch31, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 47
Mean 54.09
Std Dev 2.894
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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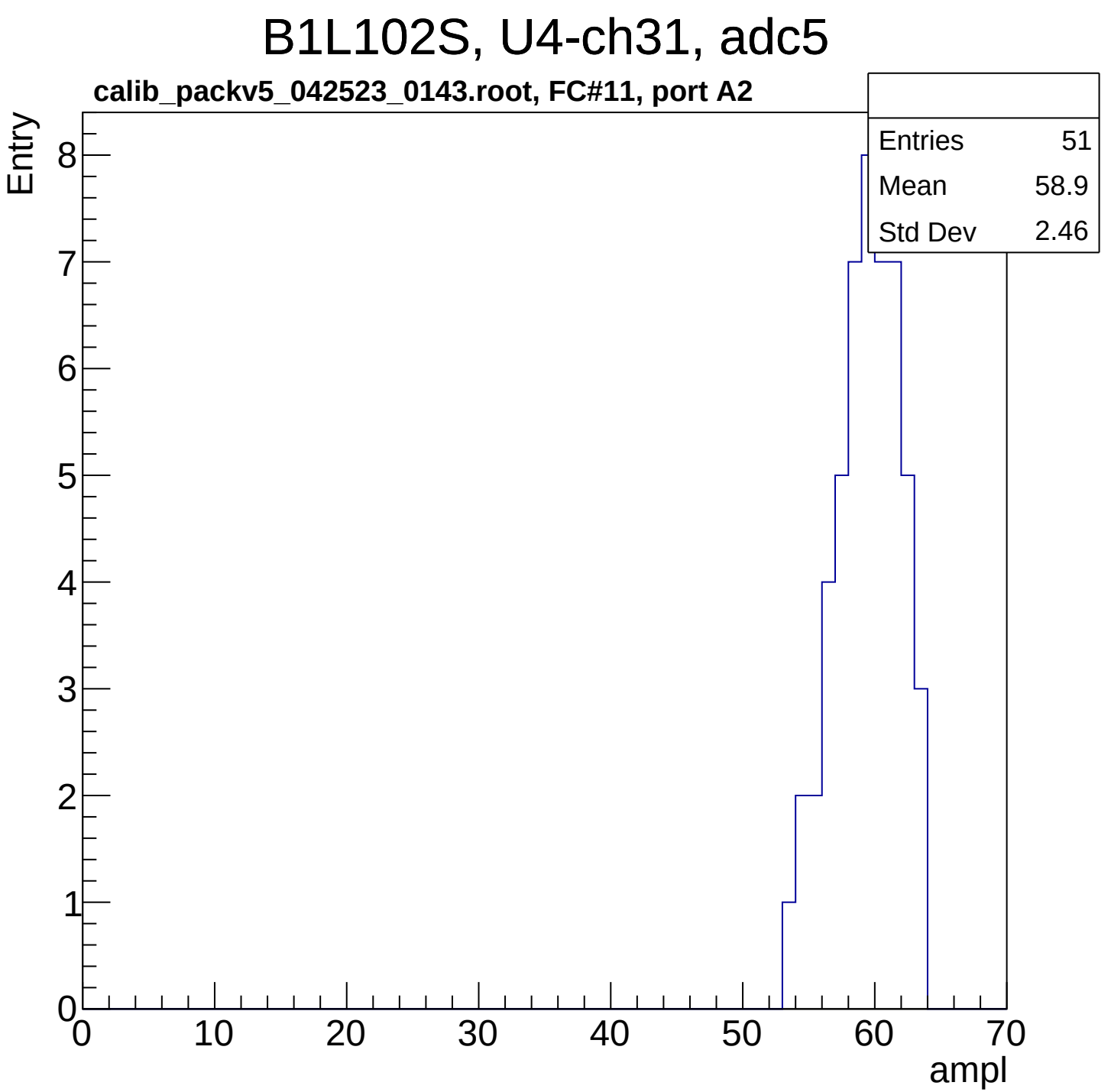
B1L102S, U4-ch31, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 58.9
Std Dev 2.46
Entry
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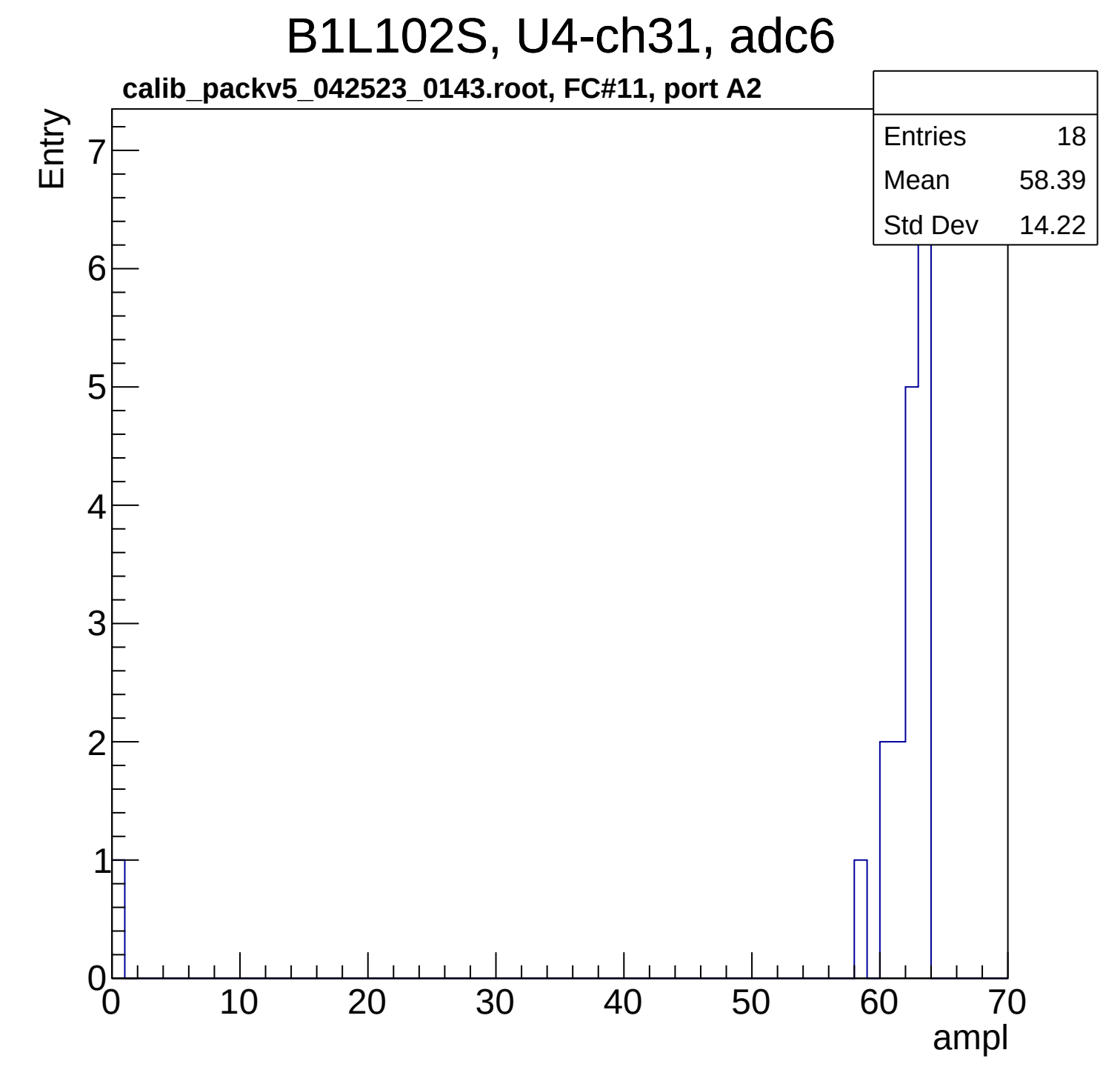
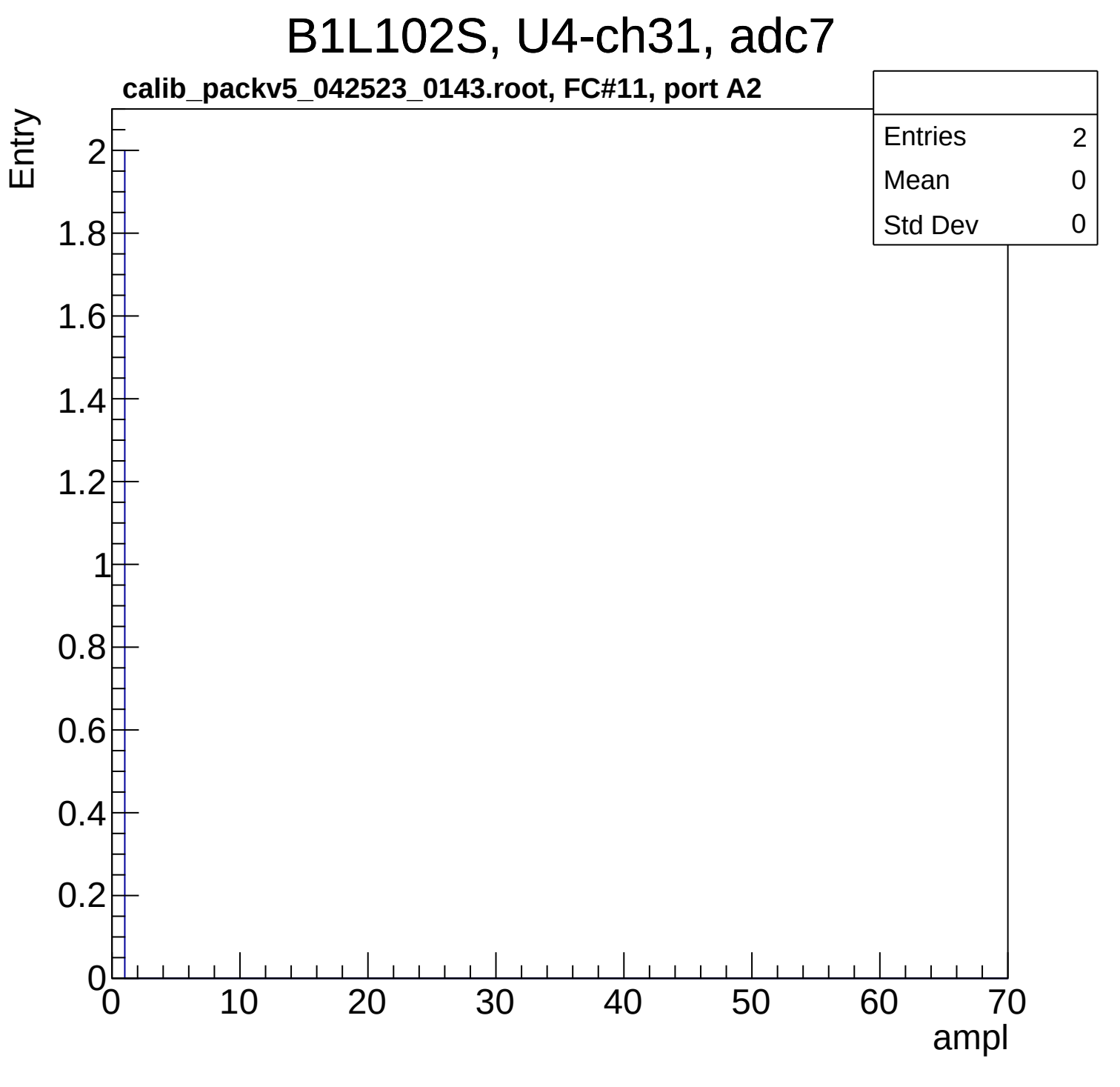
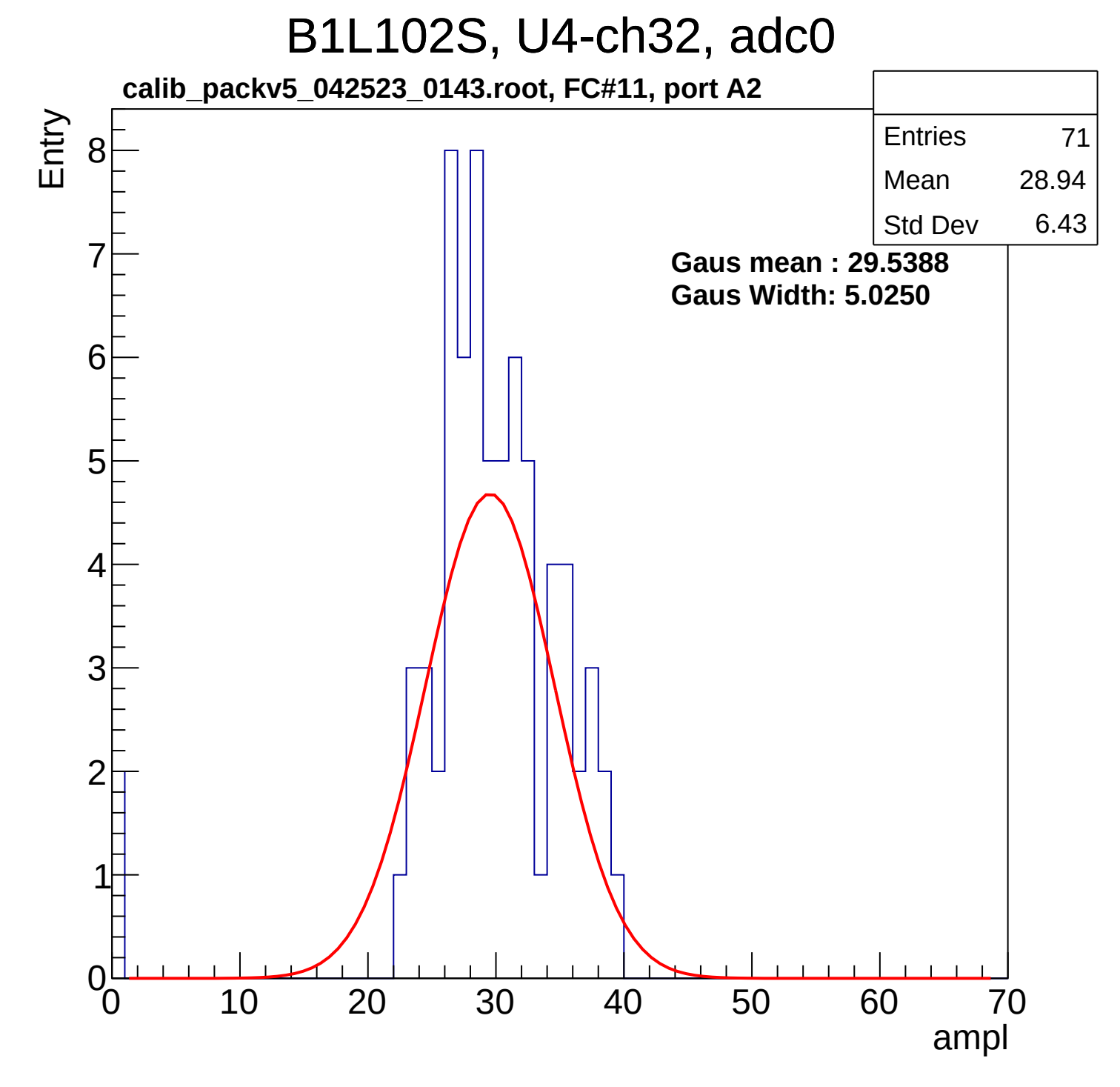
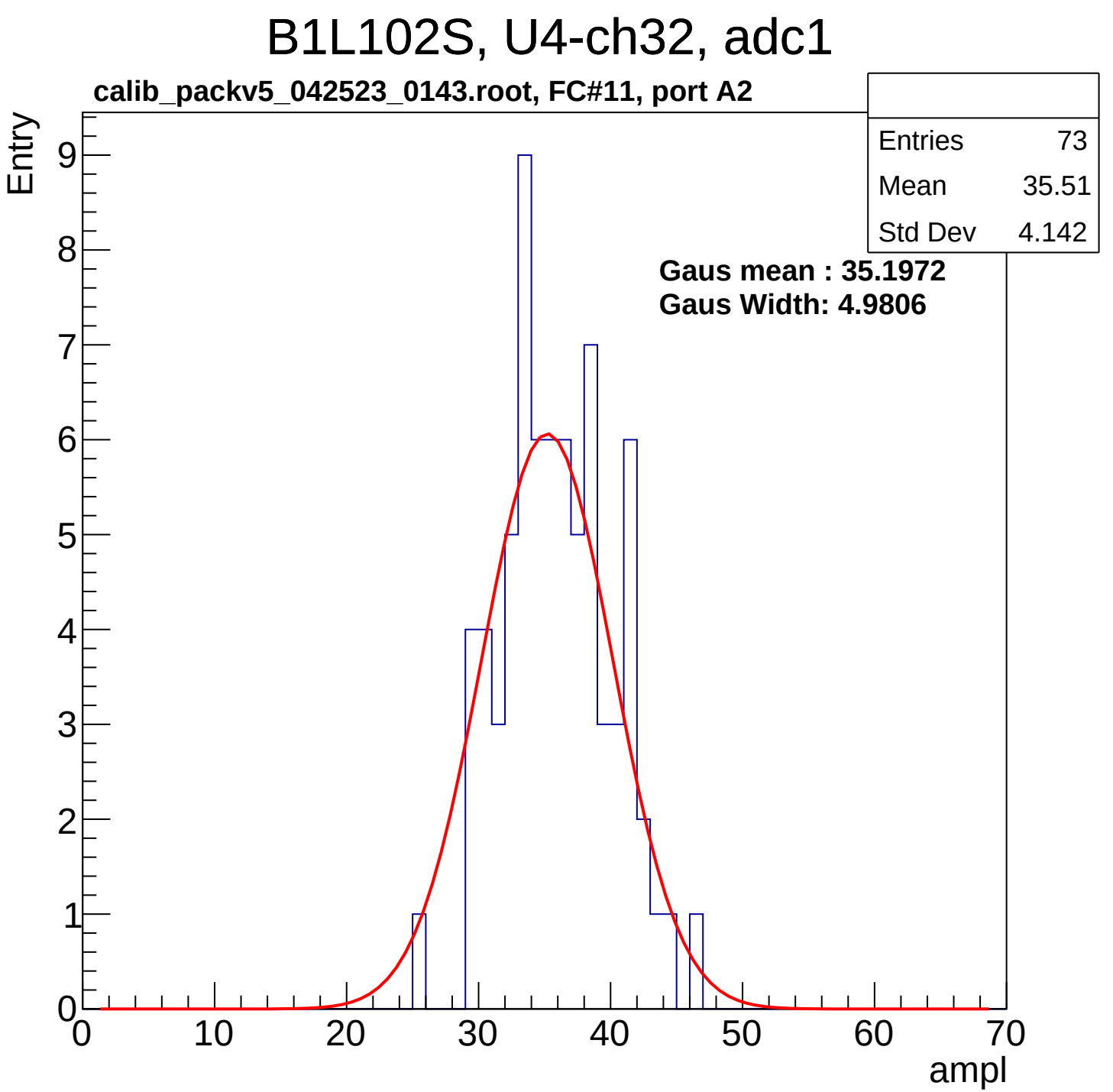
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch31, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 18
Mean 58.39
Std Dev 14.22
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch31, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch32, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 28.94
Std Dev 6.43
Gaus mean : 29.5388
Gaus Width: 5.0250
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch32, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 35.51
Std Dev 4.142
Gaus mean : 35.1972
Gaus Width: 4.9806
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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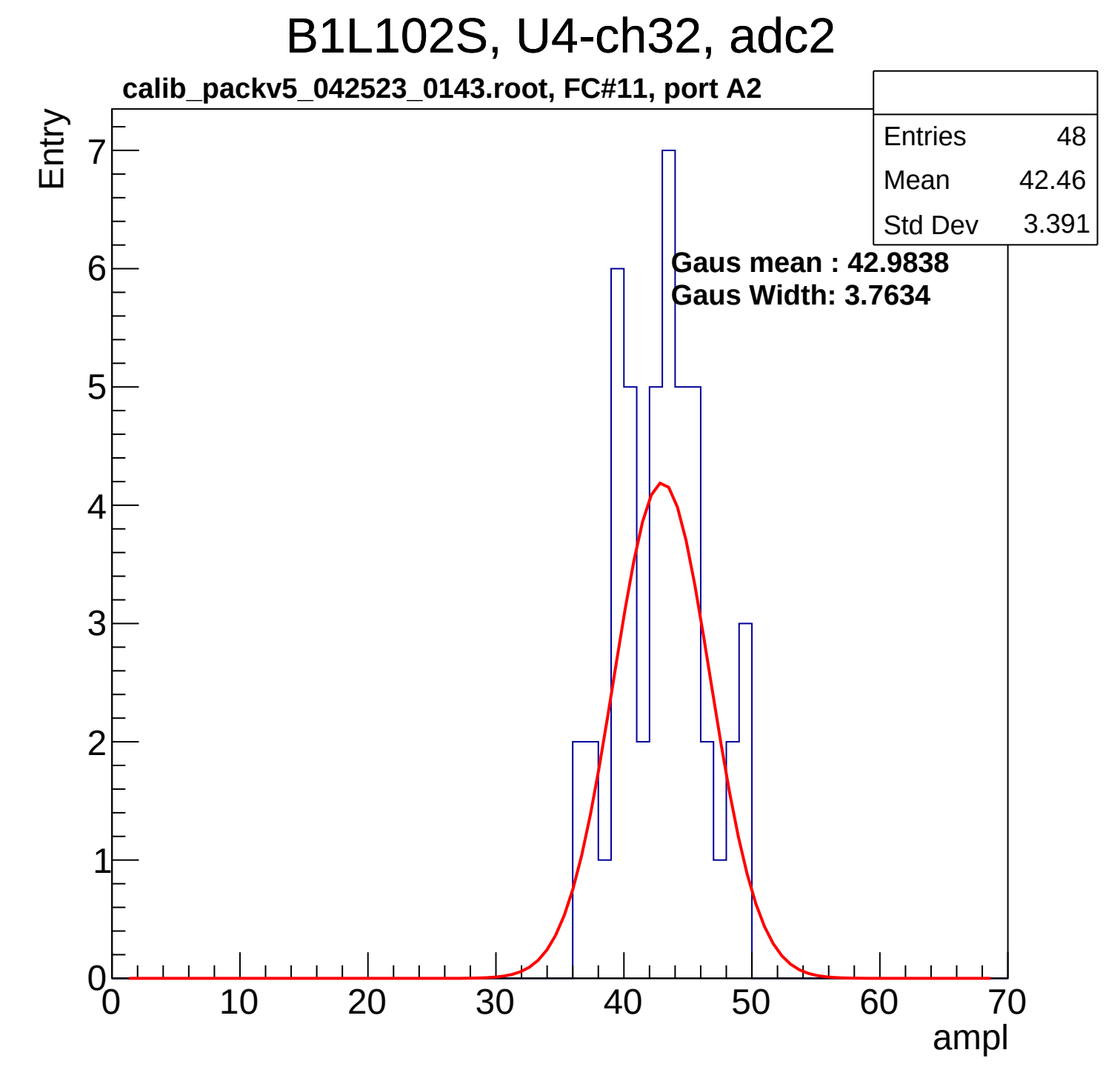
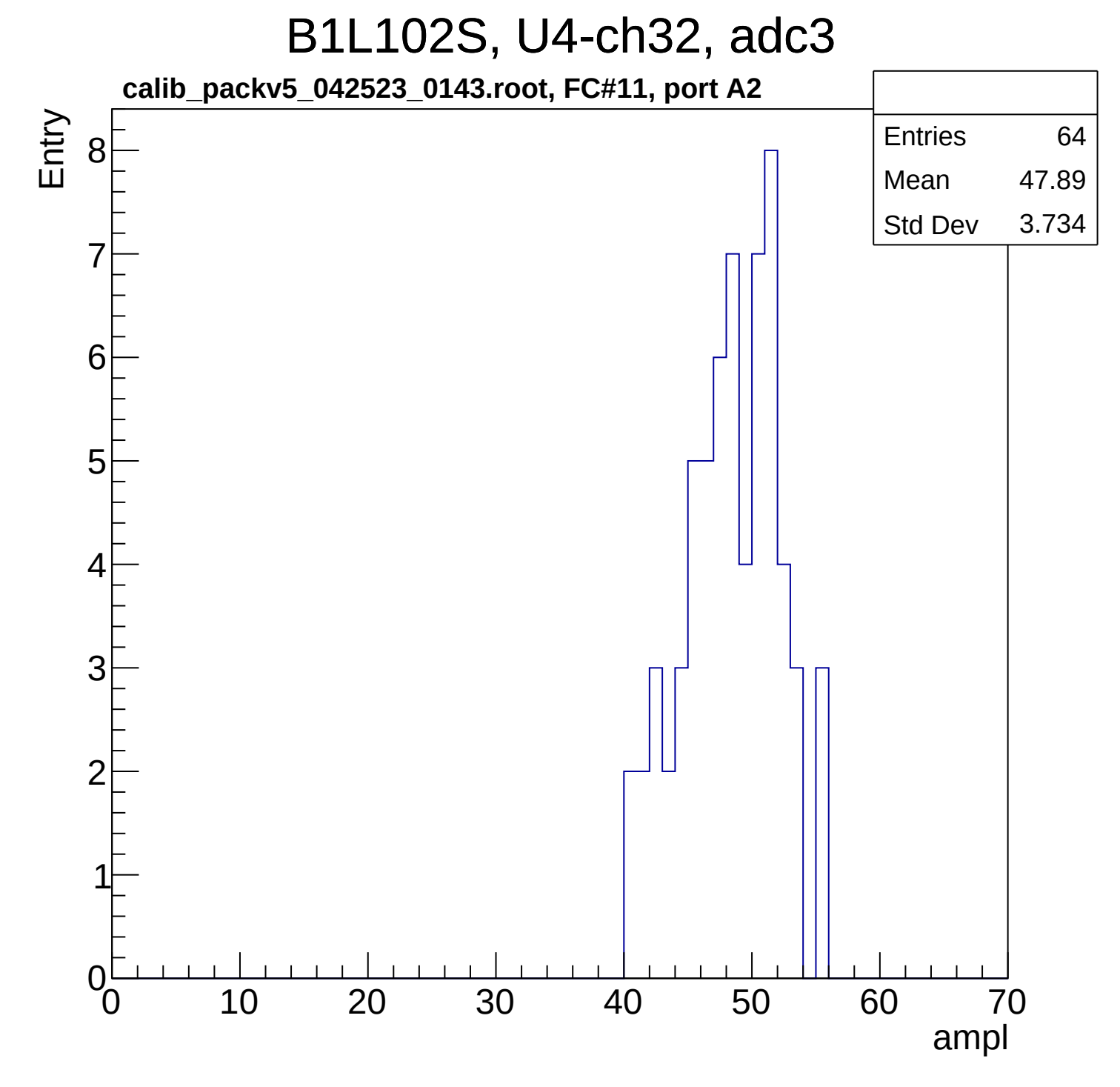

B1L102S, U4-ch32, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 48
Mean 42.46
Std Dev 3.391
Gaus mean : 42.9838
Gaus Width: 3.7634
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch32, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 47.89
Std Dev 3.734
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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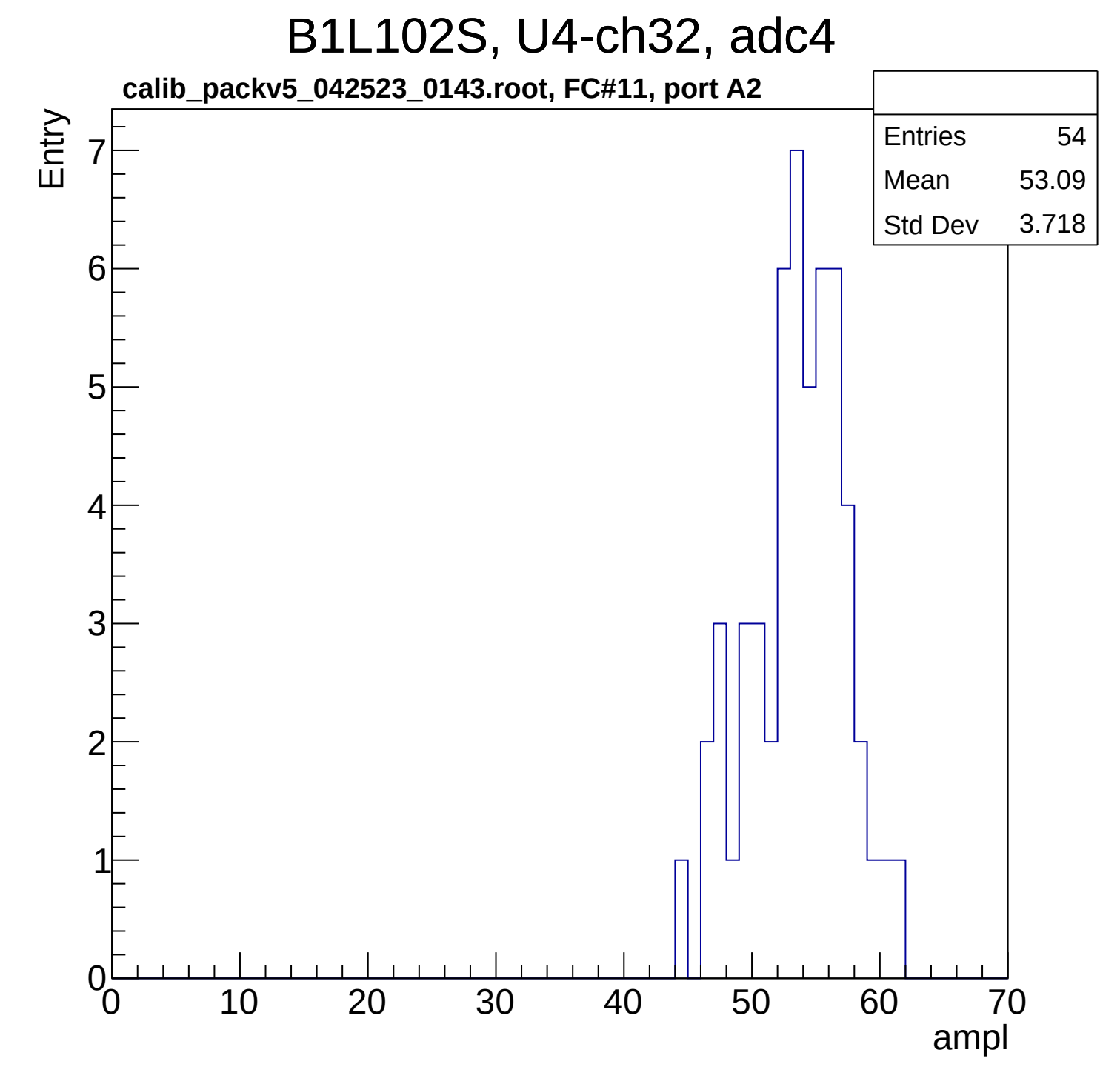
B1L102S, U4-ch32, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 53.09
Std Dev 3.718
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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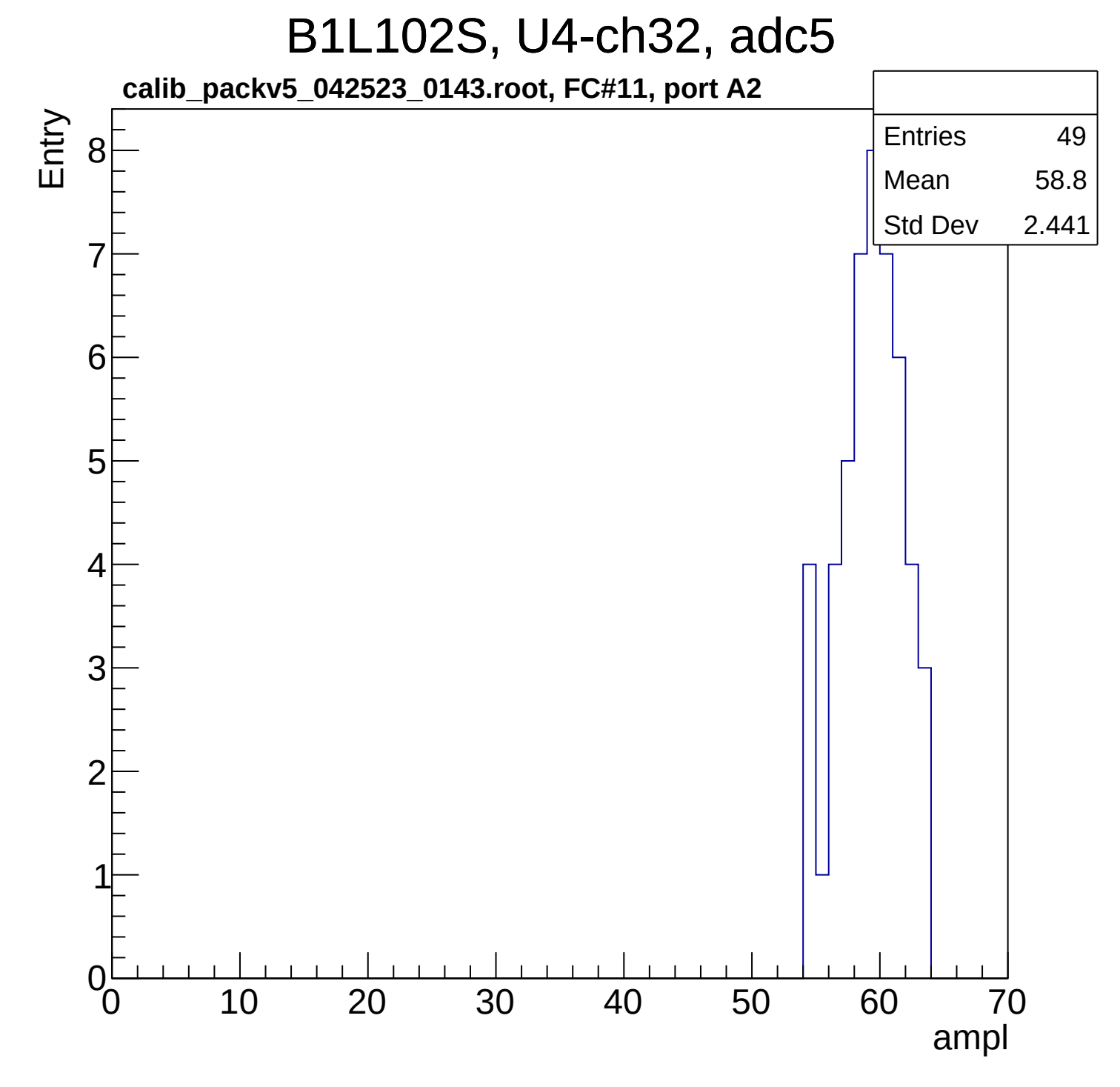
B1L102S, U4-ch32, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 58.8
Std Dev 2.441
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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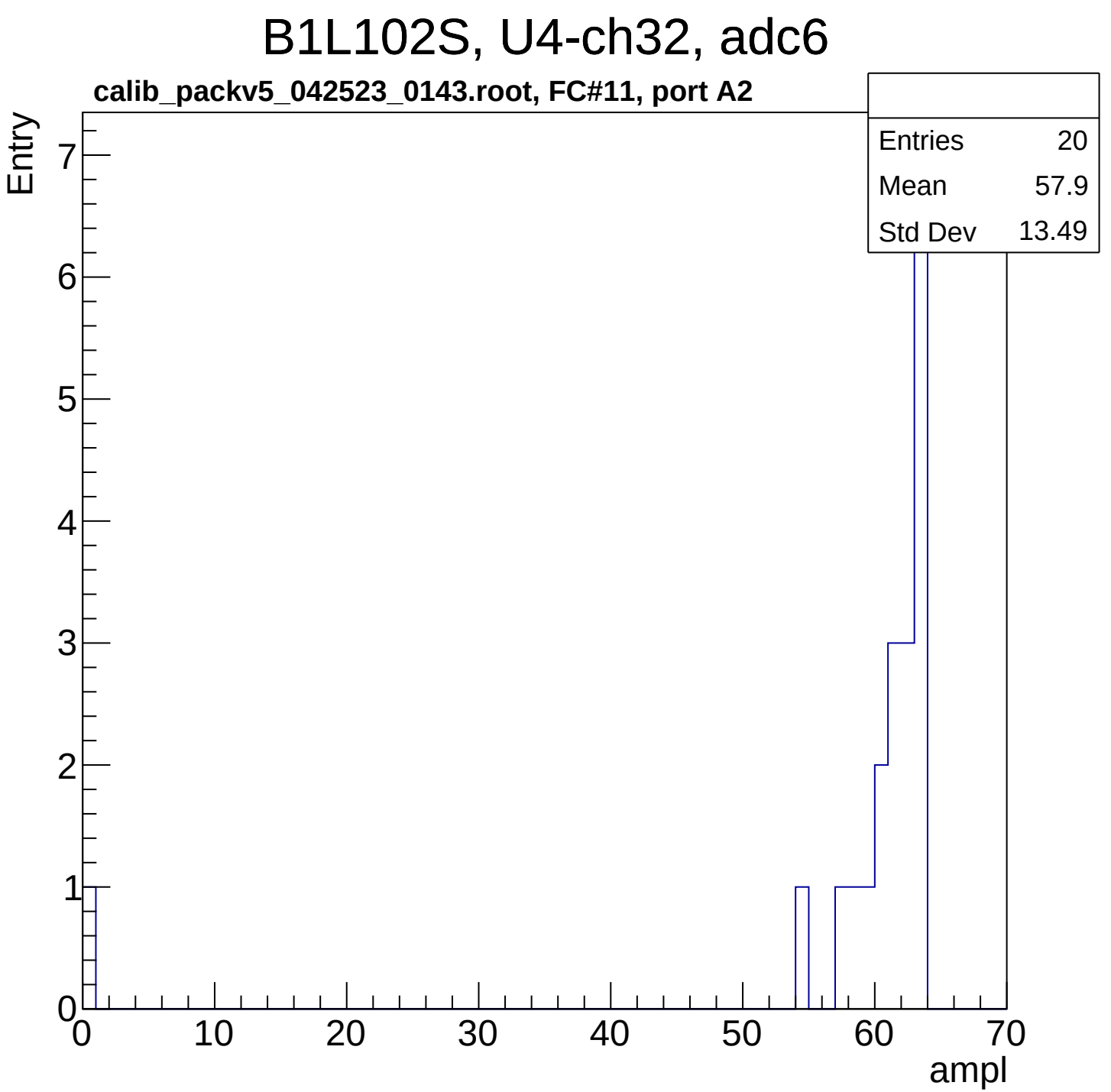
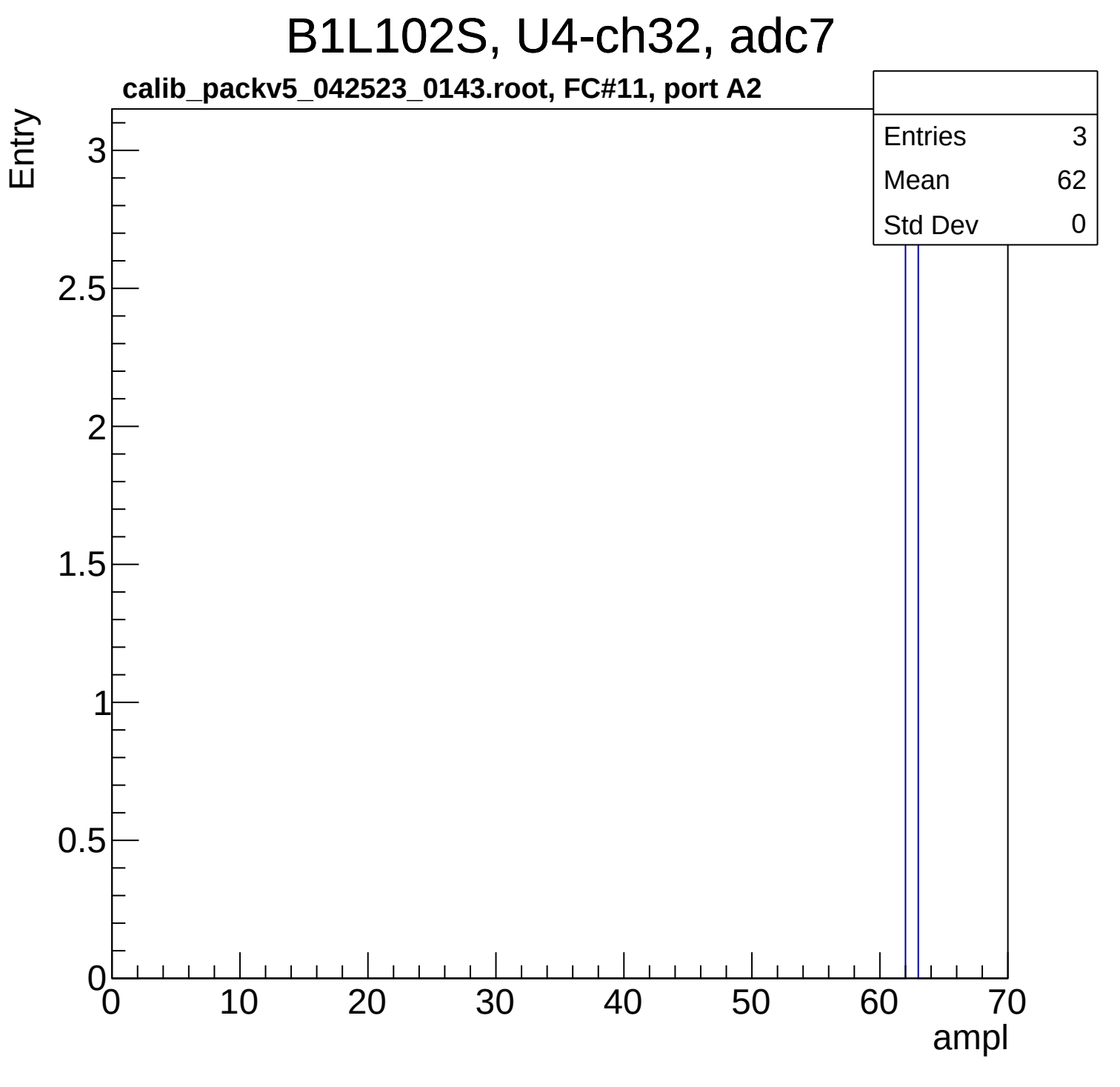

B1L102S, U4-ch32, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 20
Mean 57.9
Std Dev 13.49
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch32, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 62
Std Dev 0
Entry
ampl
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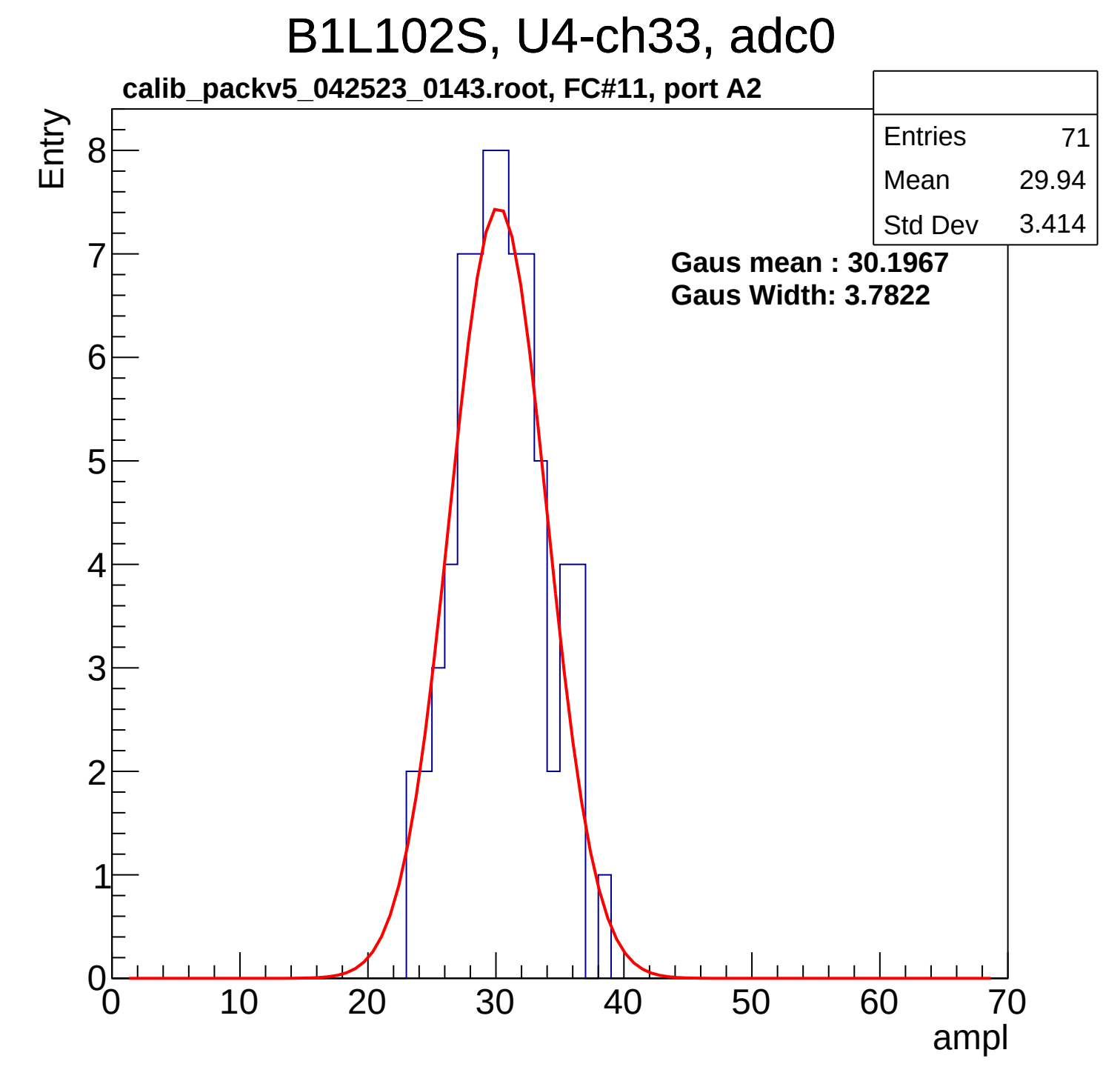
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U4-ch33, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 29.94
Std Dev 3.414
Gaus mean : 30.1967
Gaus Width: 3.7822
Entry
ampl
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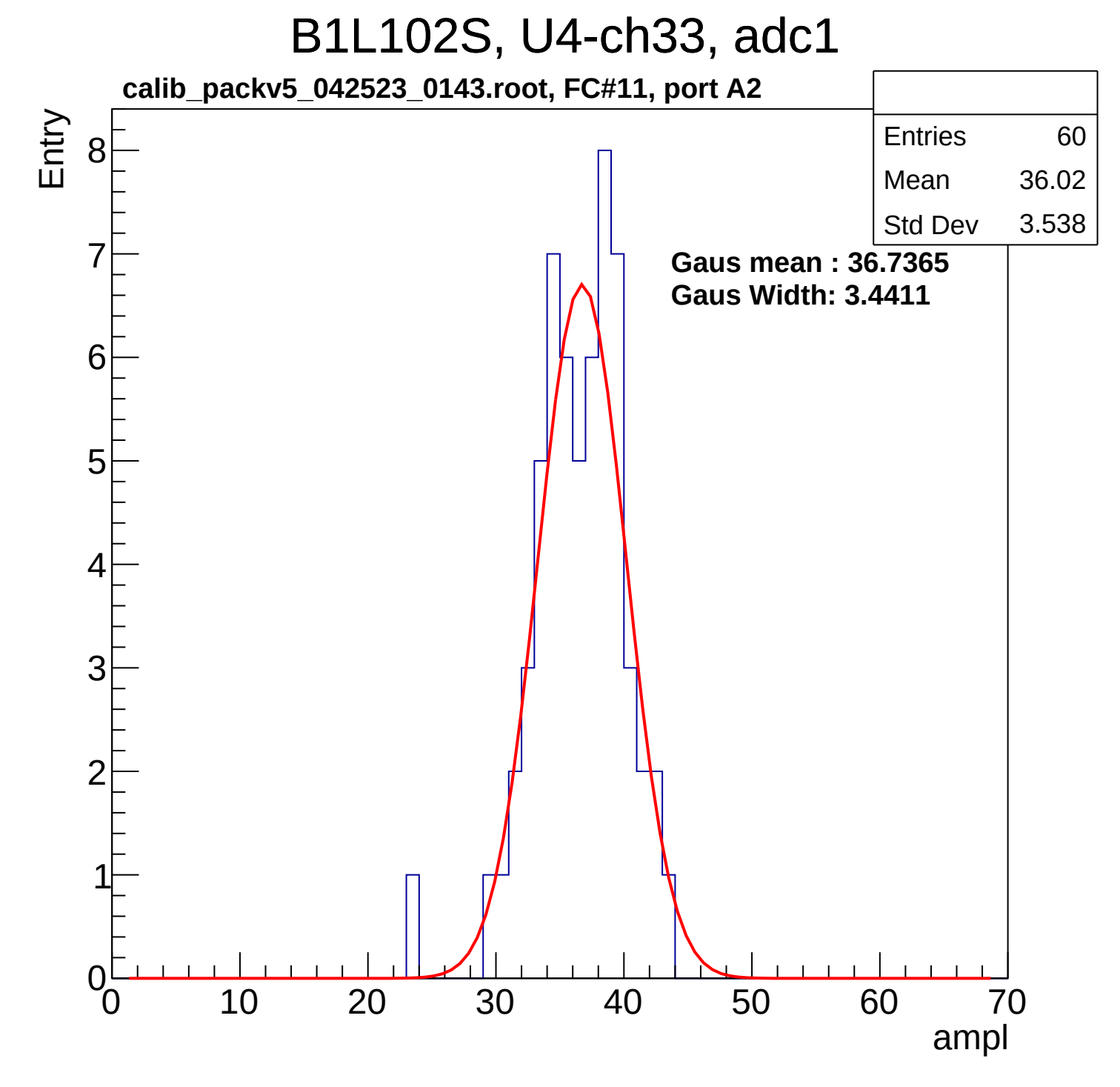
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch33, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 36.02
Std Dev 3.538
Gaus mean : 36.7365
Gaus Width: 3.4411
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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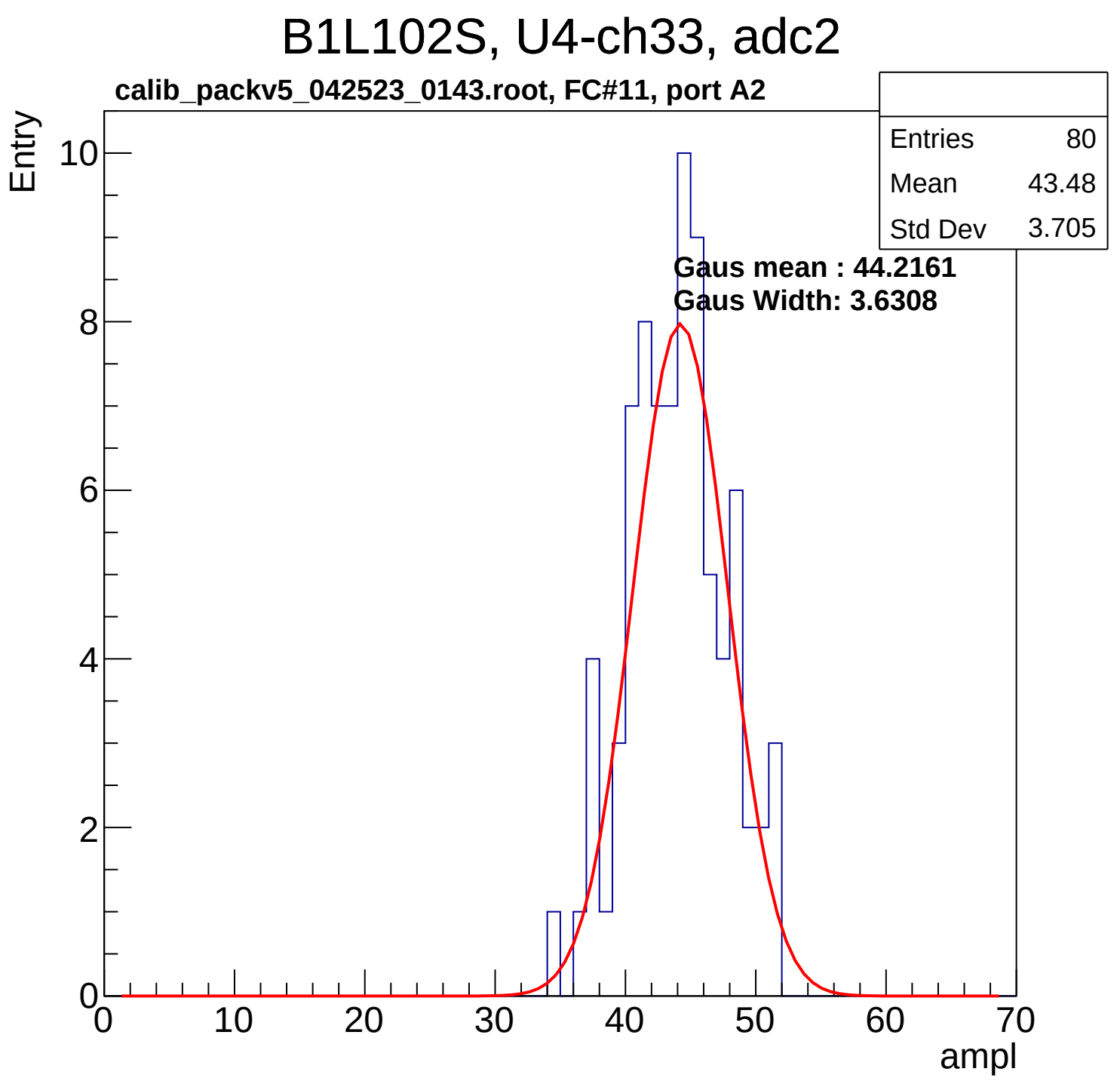
B1L102S, U4-ch33, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 80
Mean 43.48
Std Dev 3.705
Gaus mean : 44.2161
Gaus Width: 3.6308
Entry
ampl
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2
4
6
8
10
0
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20
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40
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60
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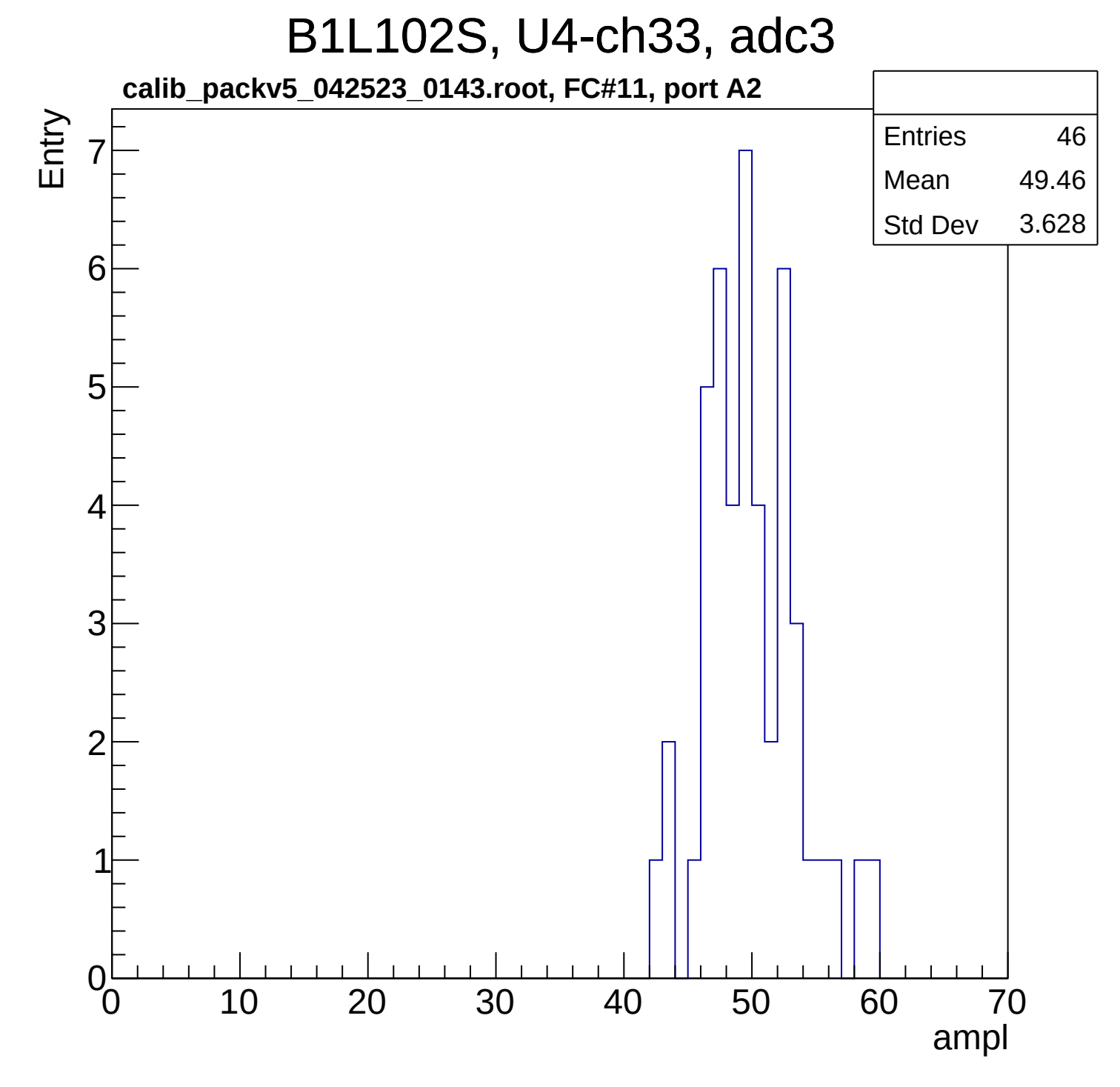
B1L102S, U4-ch33, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 46
Mean 49.46
Std Dev 3.628
Entry
ampl
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3
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0
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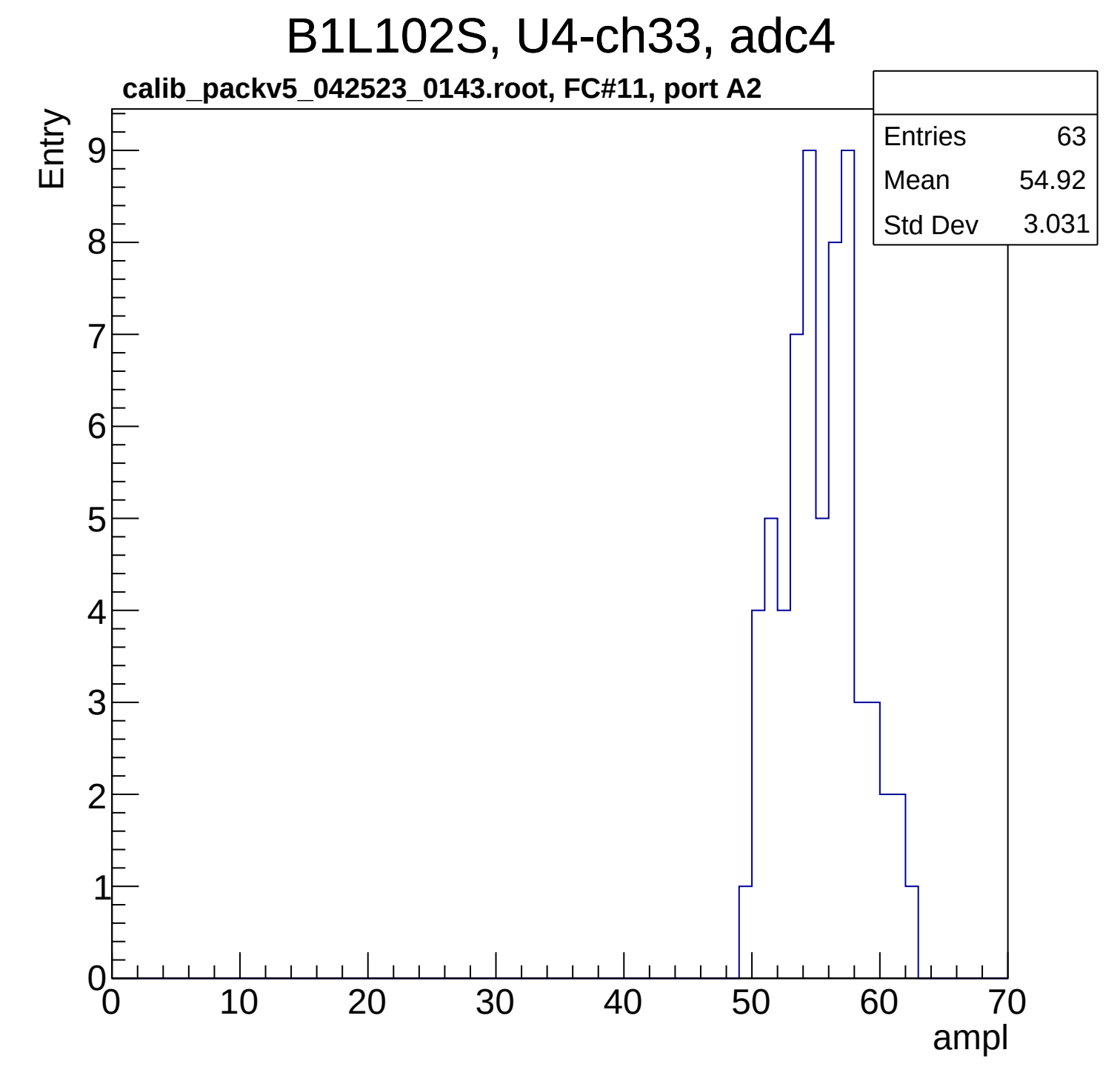
B1L102S, U4-ch33, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 54.92
Std Dev 3.031
Entry
ampl
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7
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0
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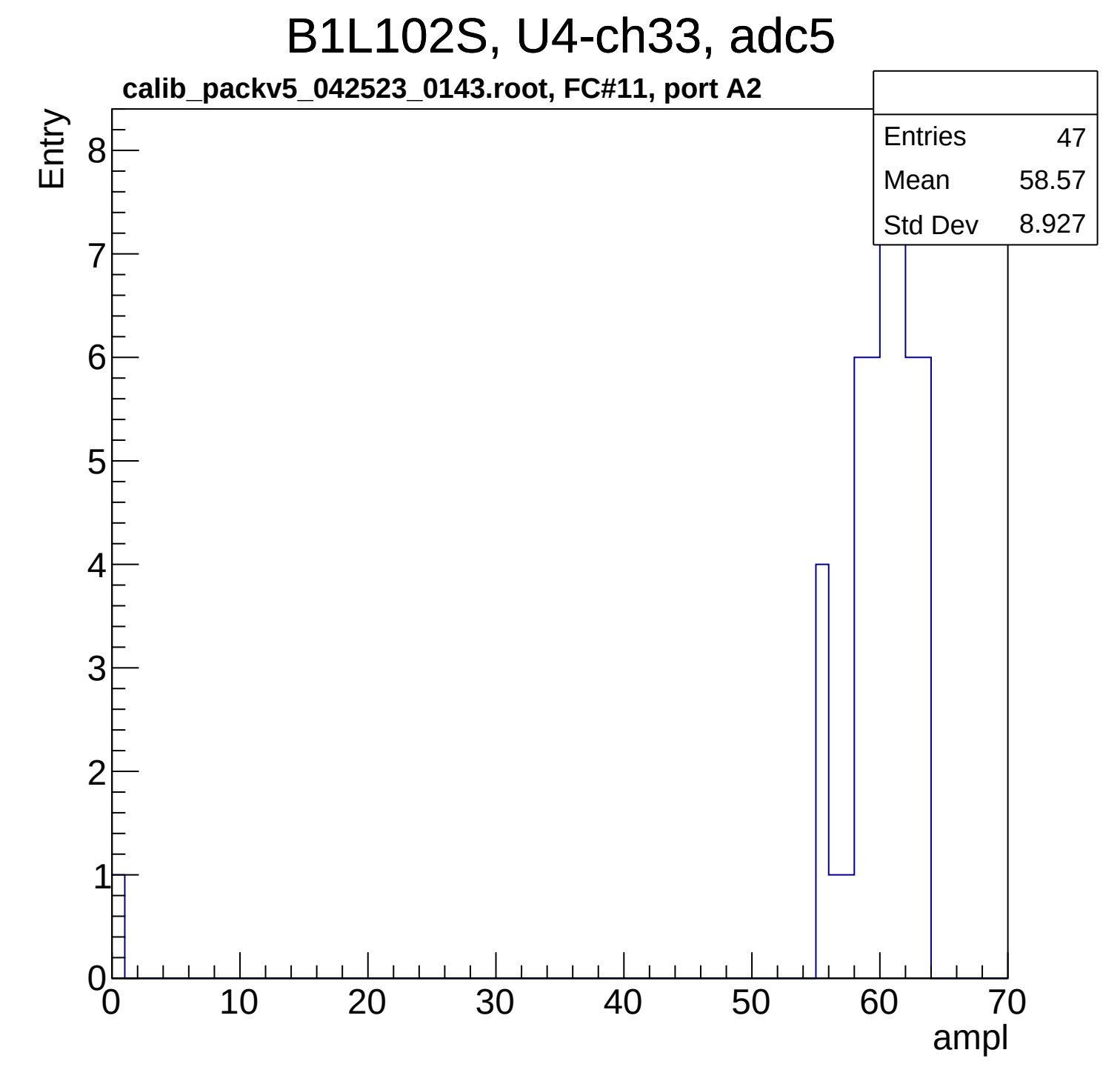
B1L102S, U4-ch33, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 47
Mean 58.57
Std Dev 8.927
Entry
ampl
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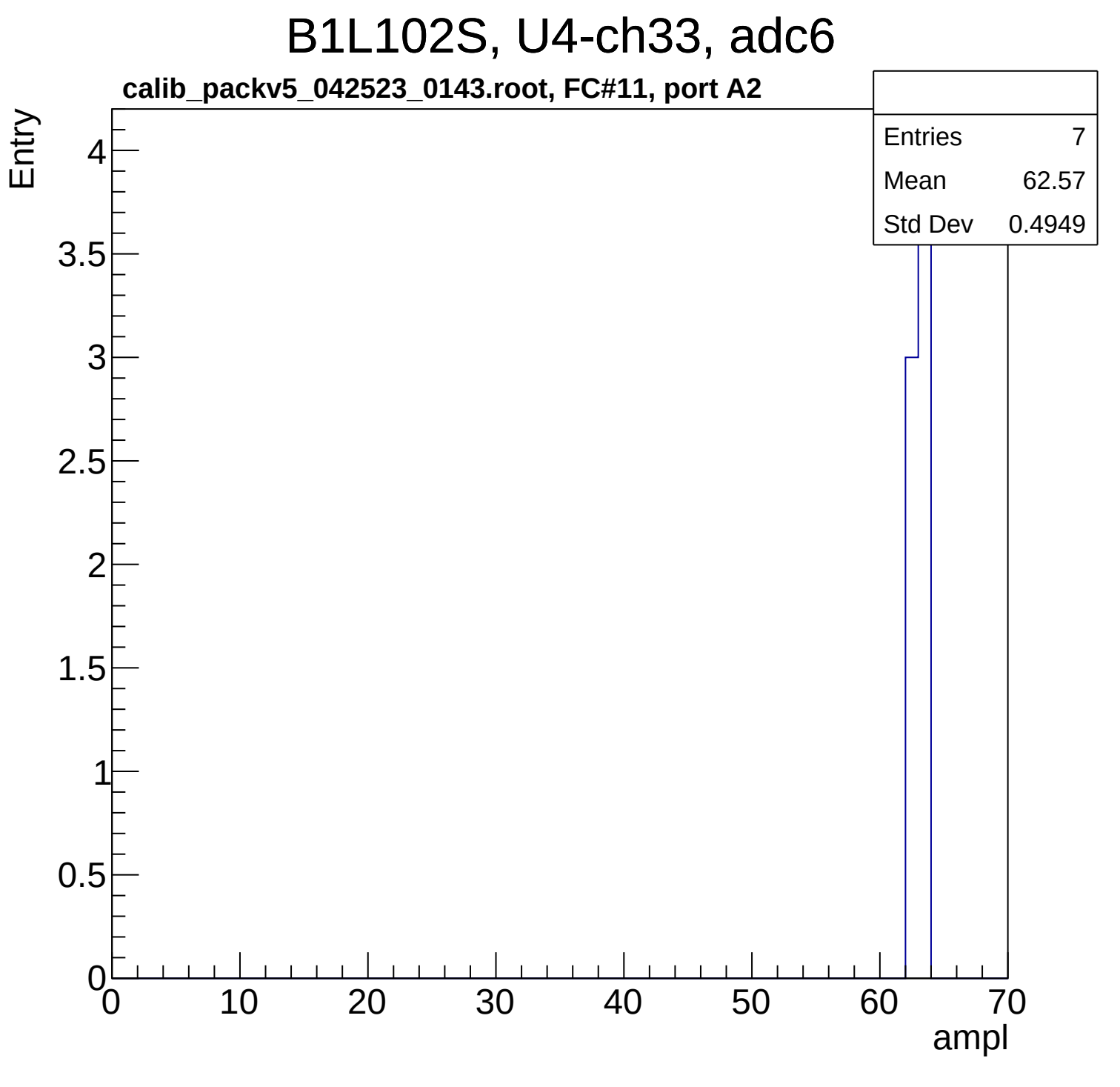
B1L102S, U4-ch33, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 7
Mean 62.57
Std Dev 0.4949
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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40
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60
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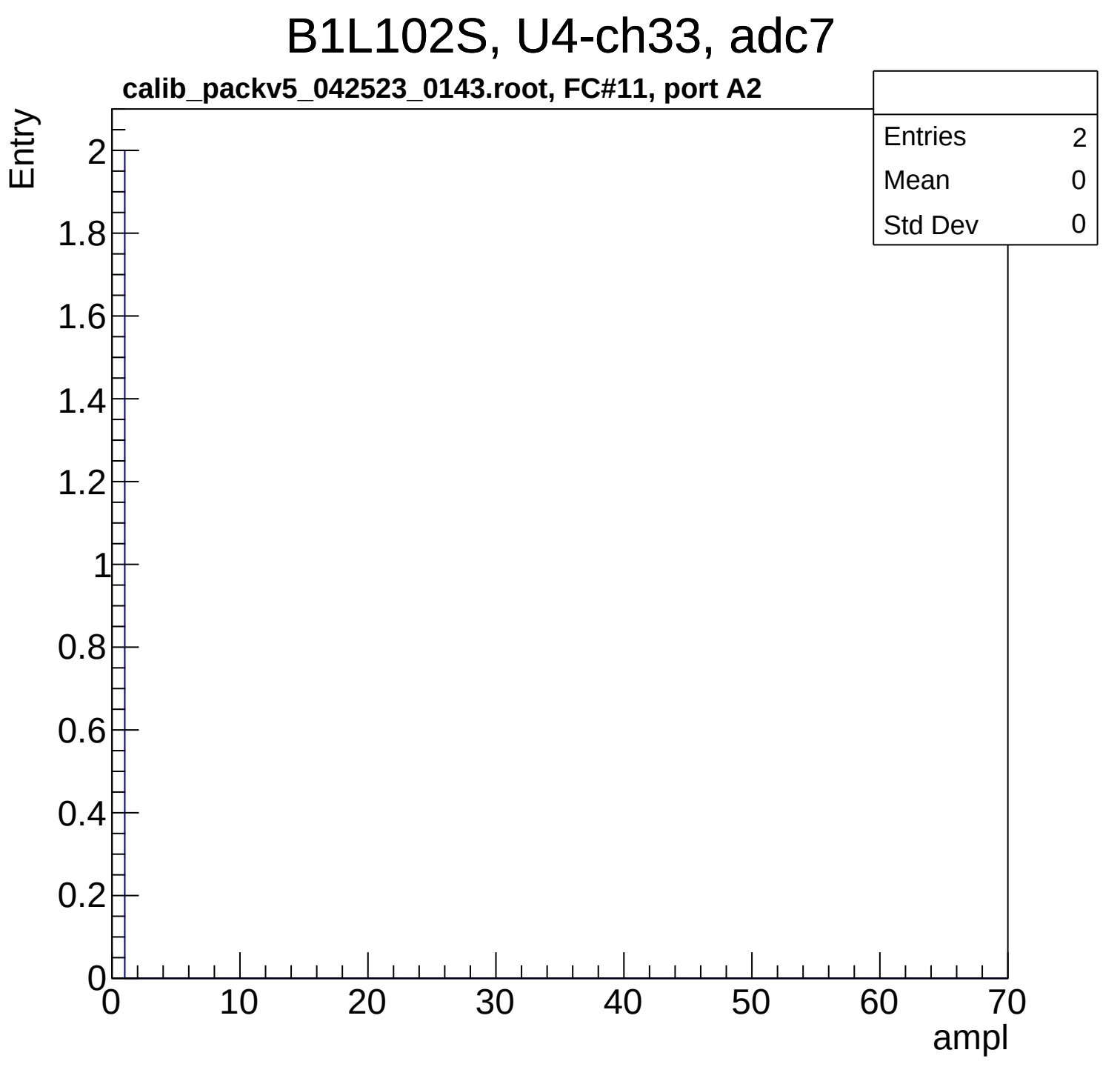
B1L102S, U4-ch33, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
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1
1.2
1.4
1.6
1.8
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0
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40
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60
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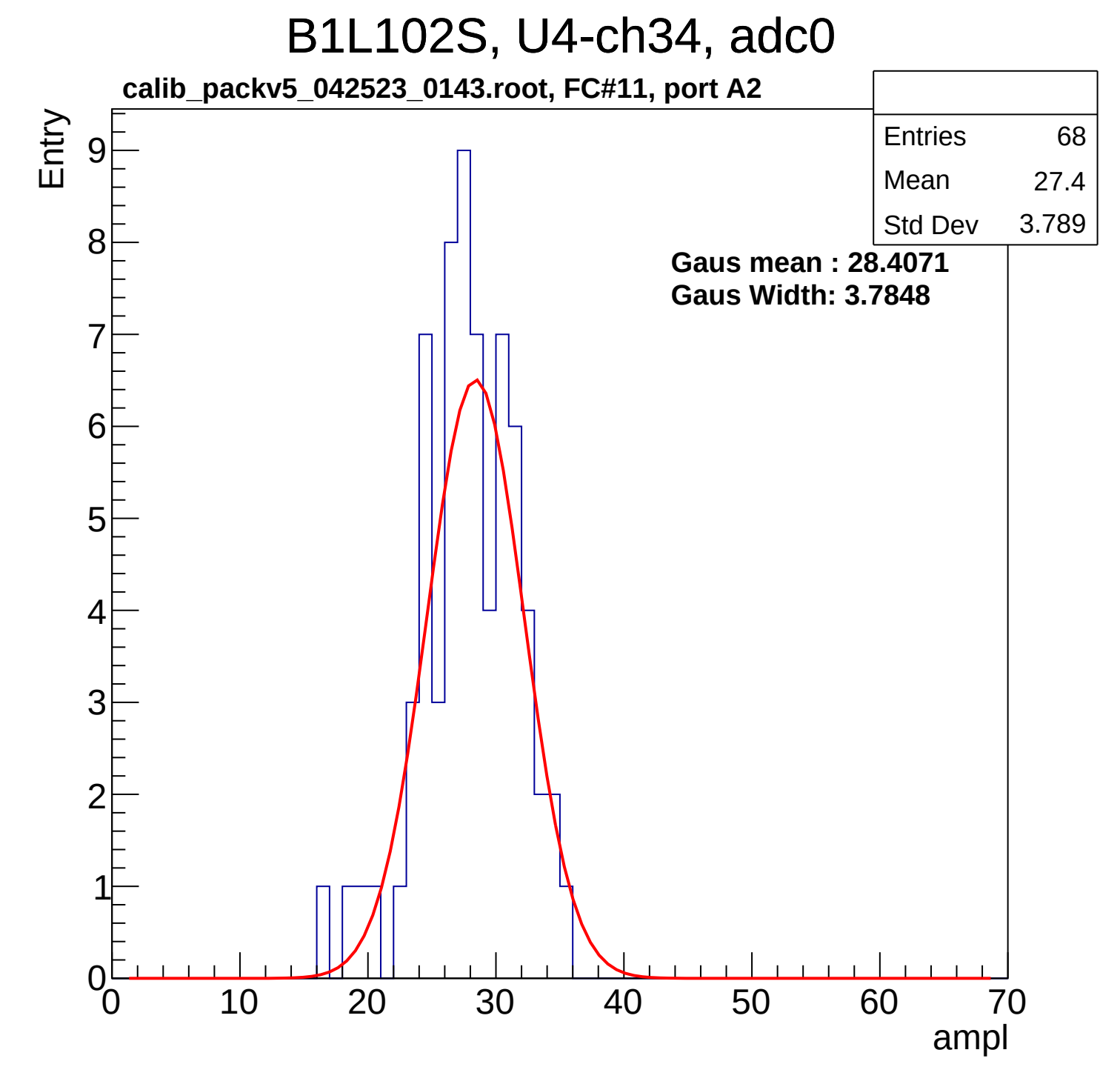
B1L102S, U4-ch34, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 27.4
Std Dev 3.789
Gaus mean : 28.4071
Gaus Width: 3.7848
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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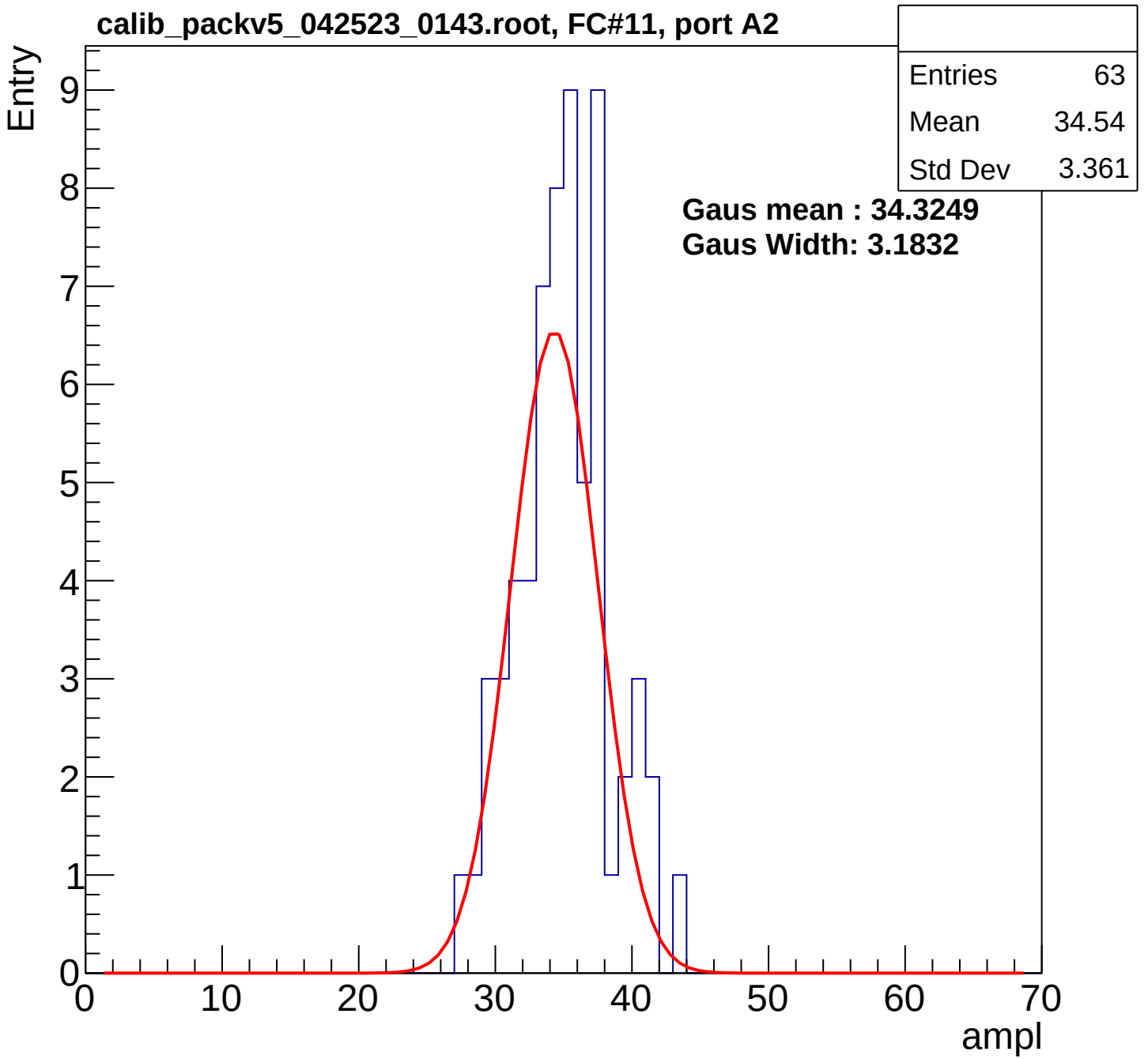
B1L102S, U4-ch34, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 34.54
Std Dev 3.361
Gaus mean : 34.3249
Gaus Width: 3.1832
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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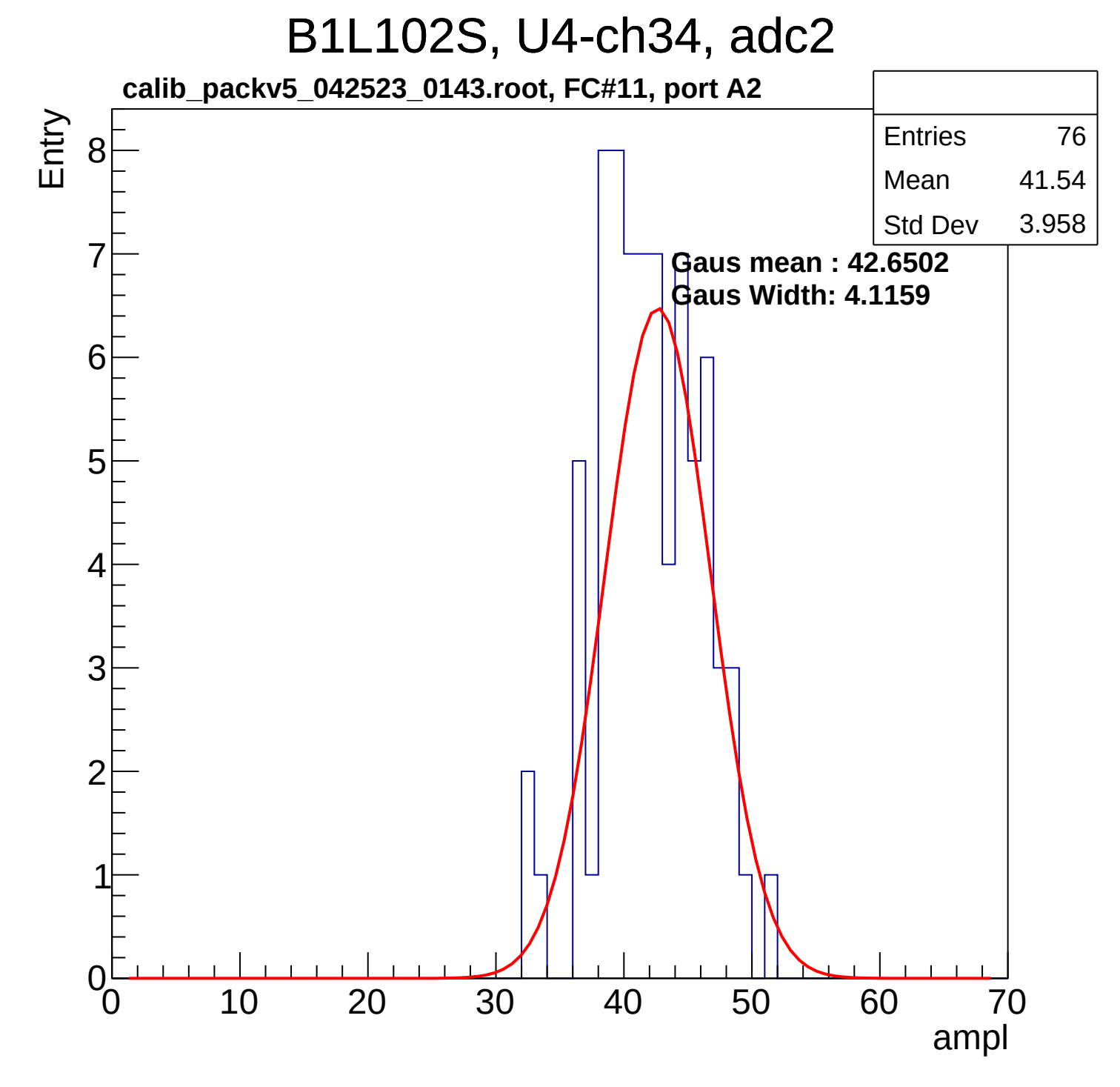
B1L102S, U4-ch34, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 41.54
Std Dev 3.958
Gaus mean : 42.6502
Gaus Width: 4.1159
Entry
ampl
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1
2
3
4
5
6
7
8
0
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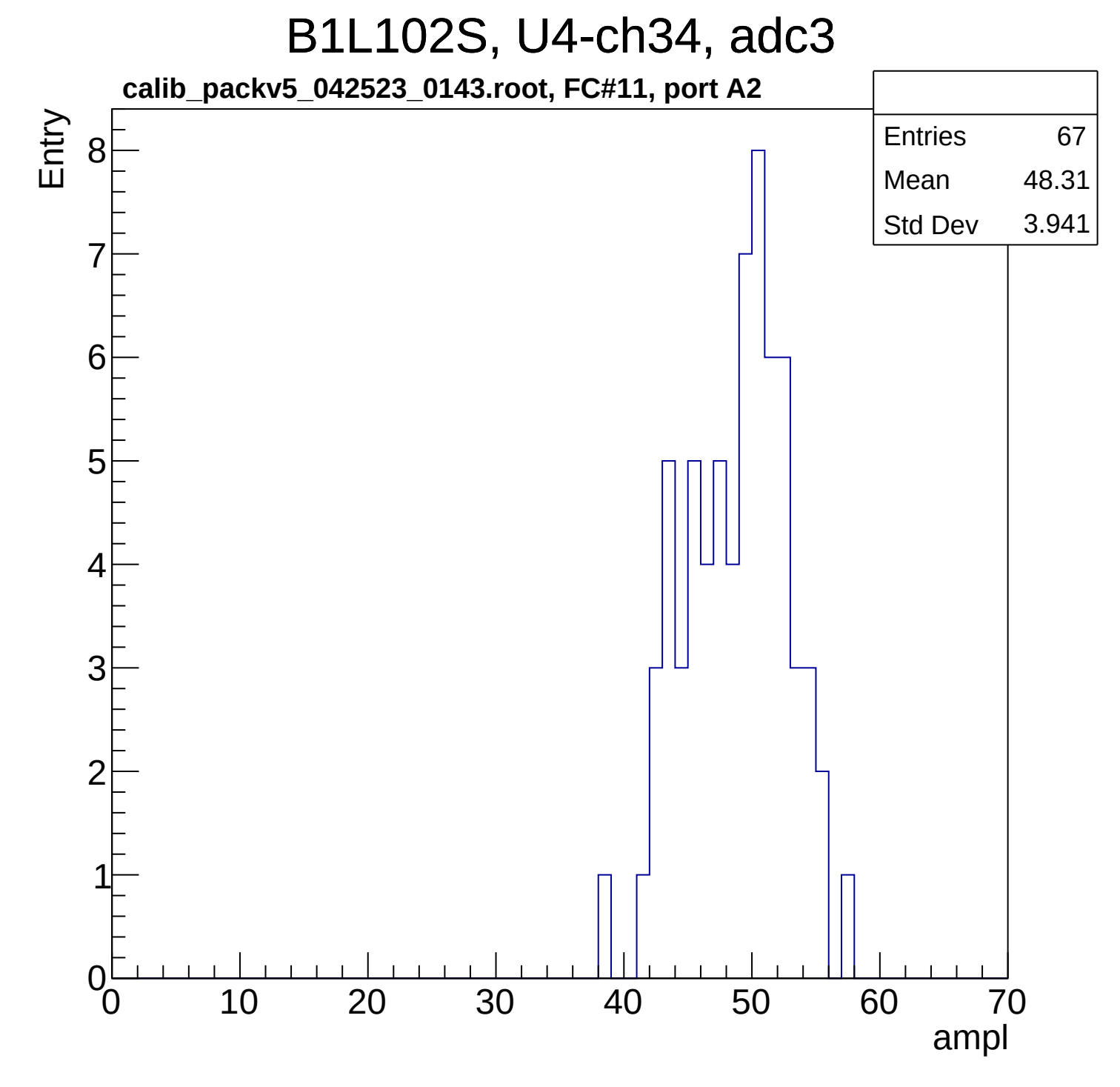
B1L102S, U4-ch34, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 48.31
Std Dev 3.941
Entry
ampl
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7
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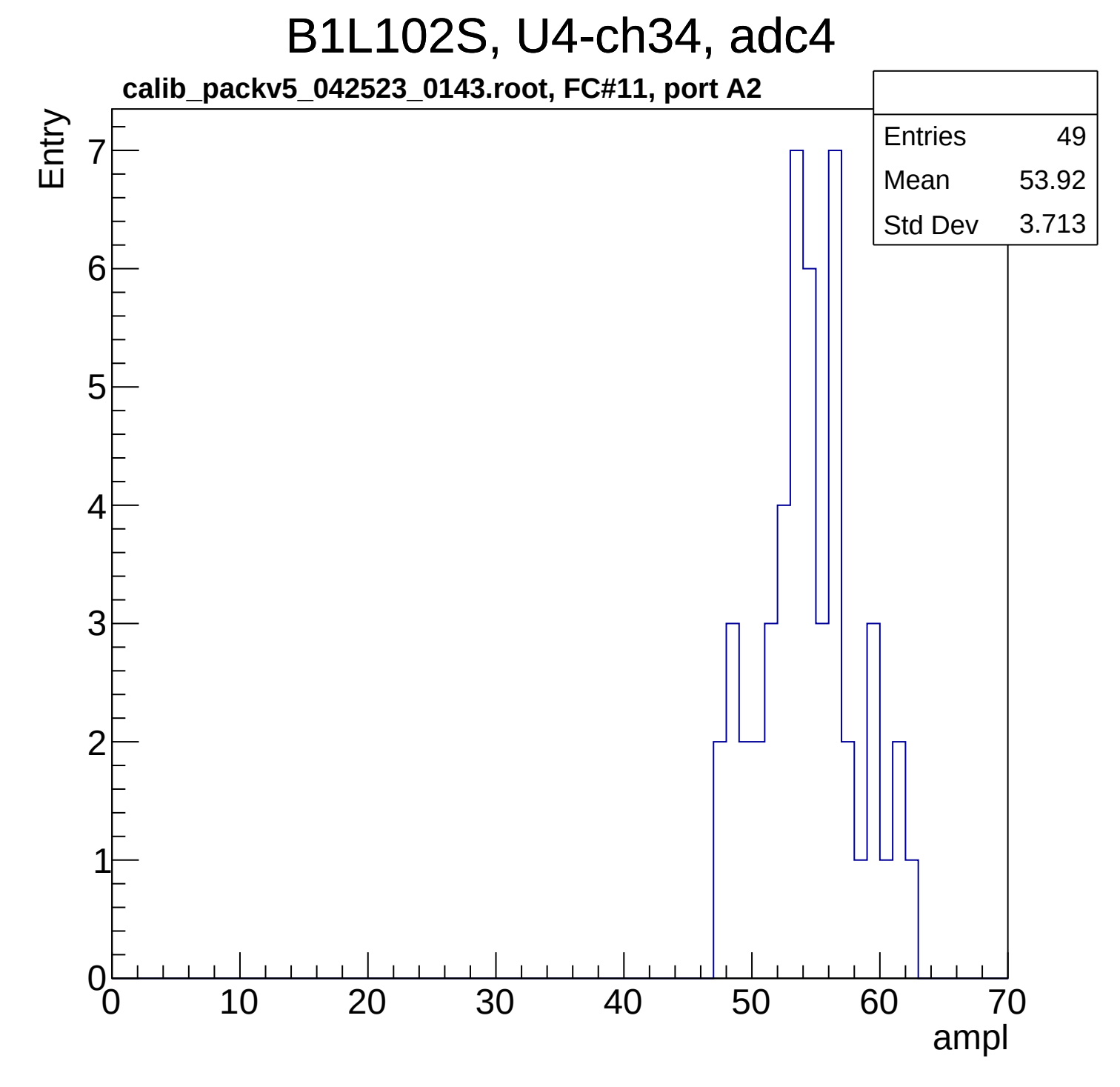
B1L102S, U4-ch34, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 53.92
Std Dev 3.713
Entry
ampl
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3
4
5
6
7
0
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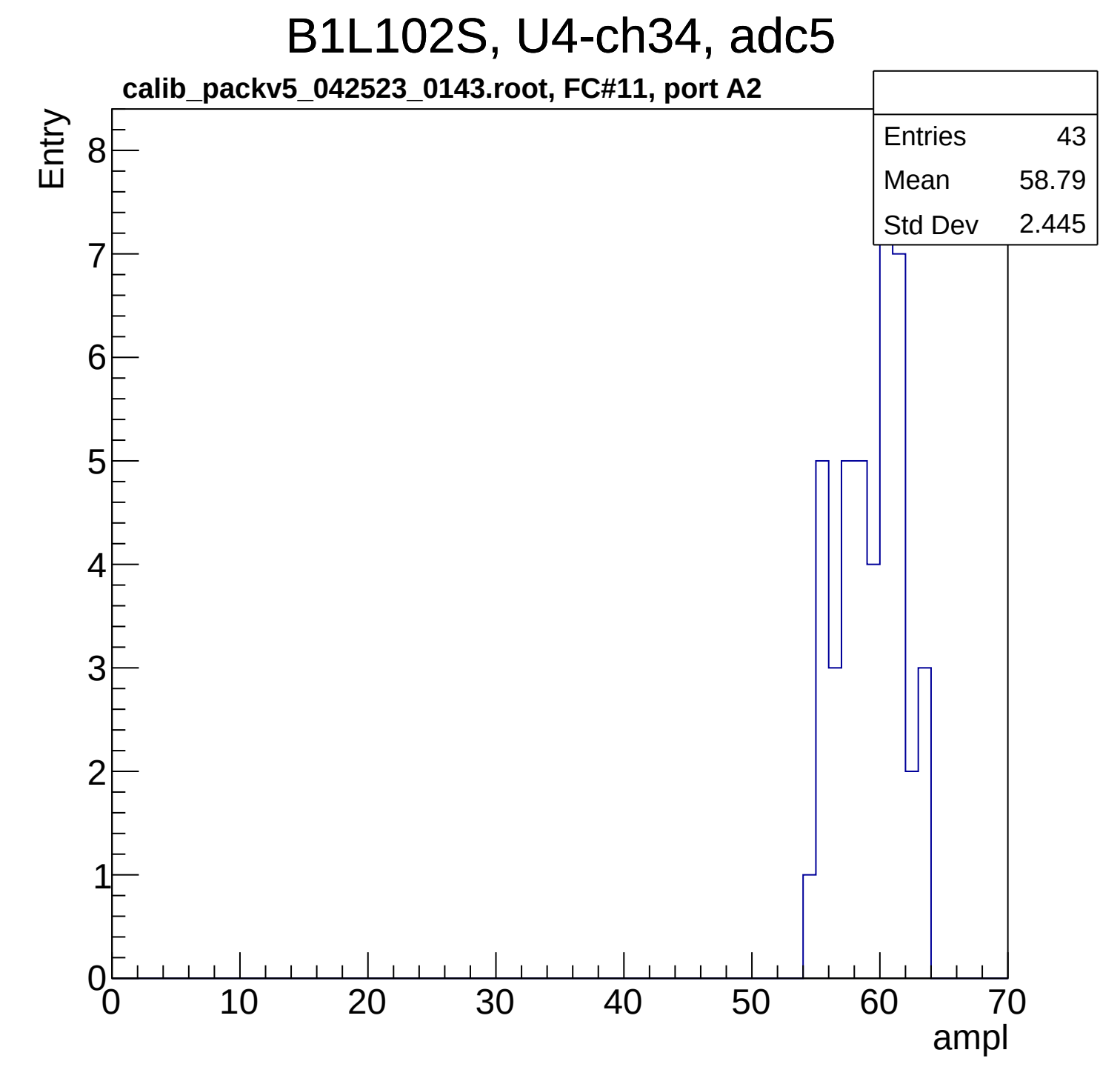
B1L102S, U4-ch34, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 43
Mean 58.79
Std Dev 2.445
Entry
ampl
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4
5
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0
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40
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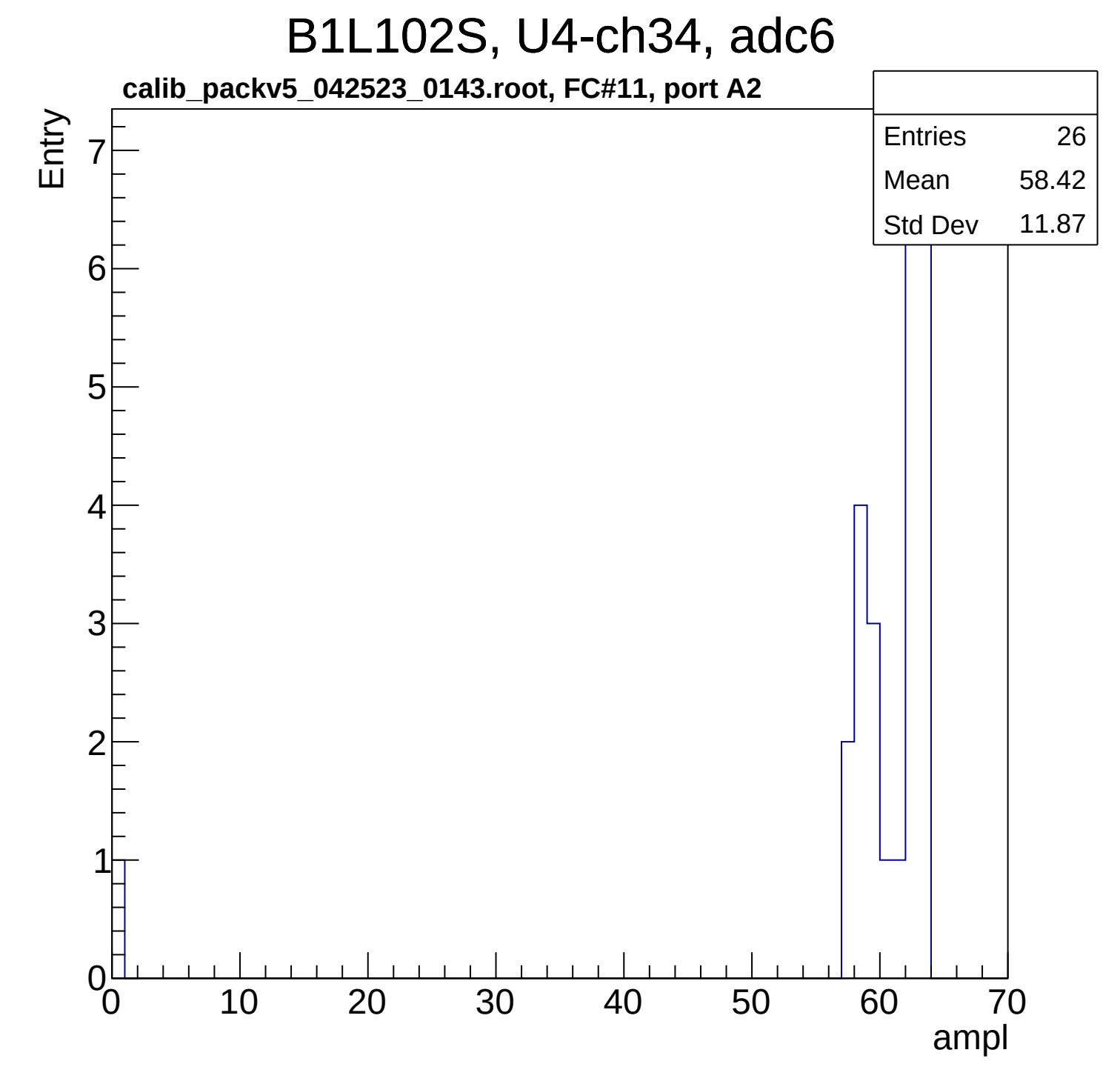
B1L102S, U4-ch34, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 26
Mean 58.42
Std Dev 11.87
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
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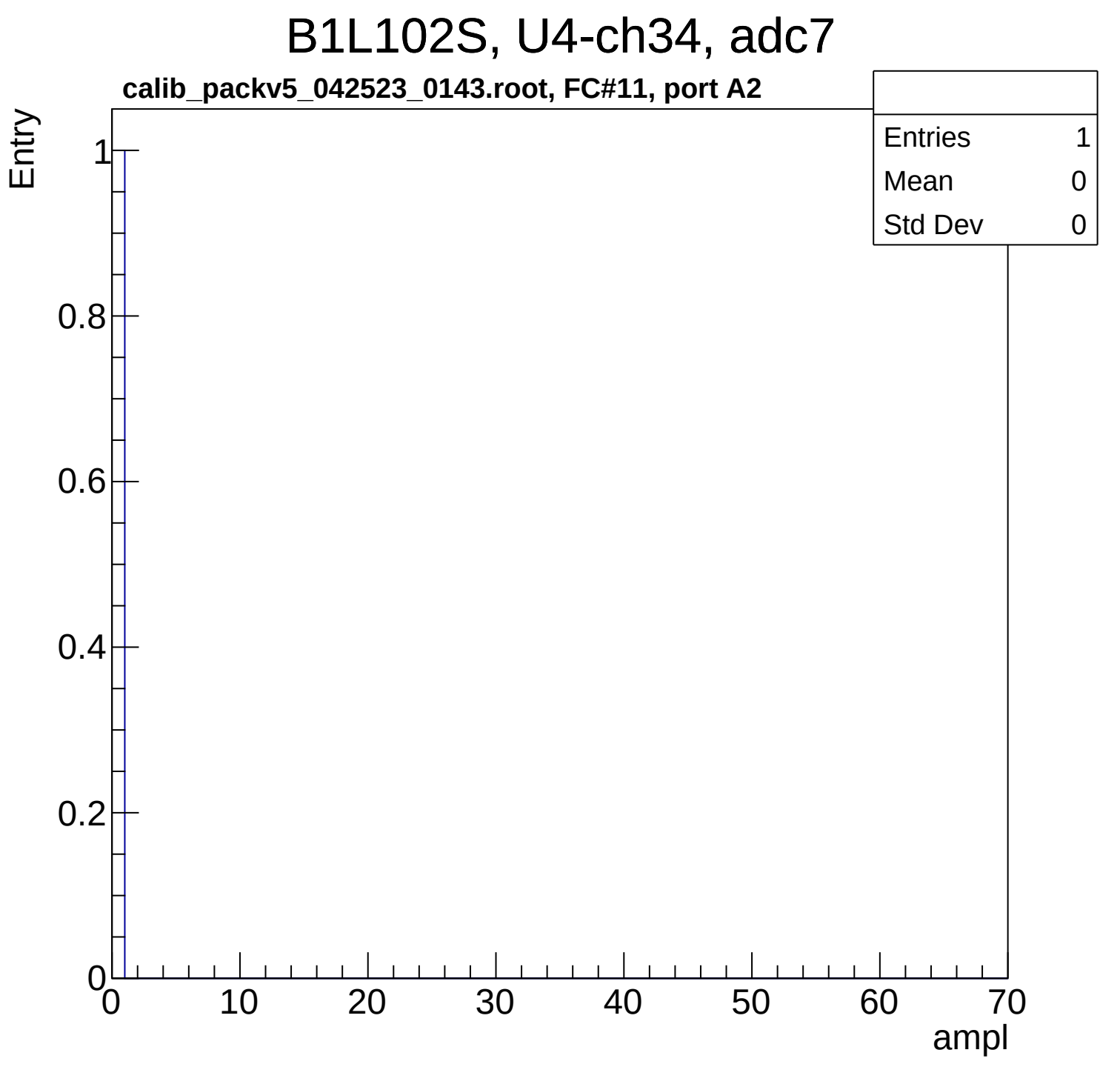
60
70


B1L102S, U4-ch34, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
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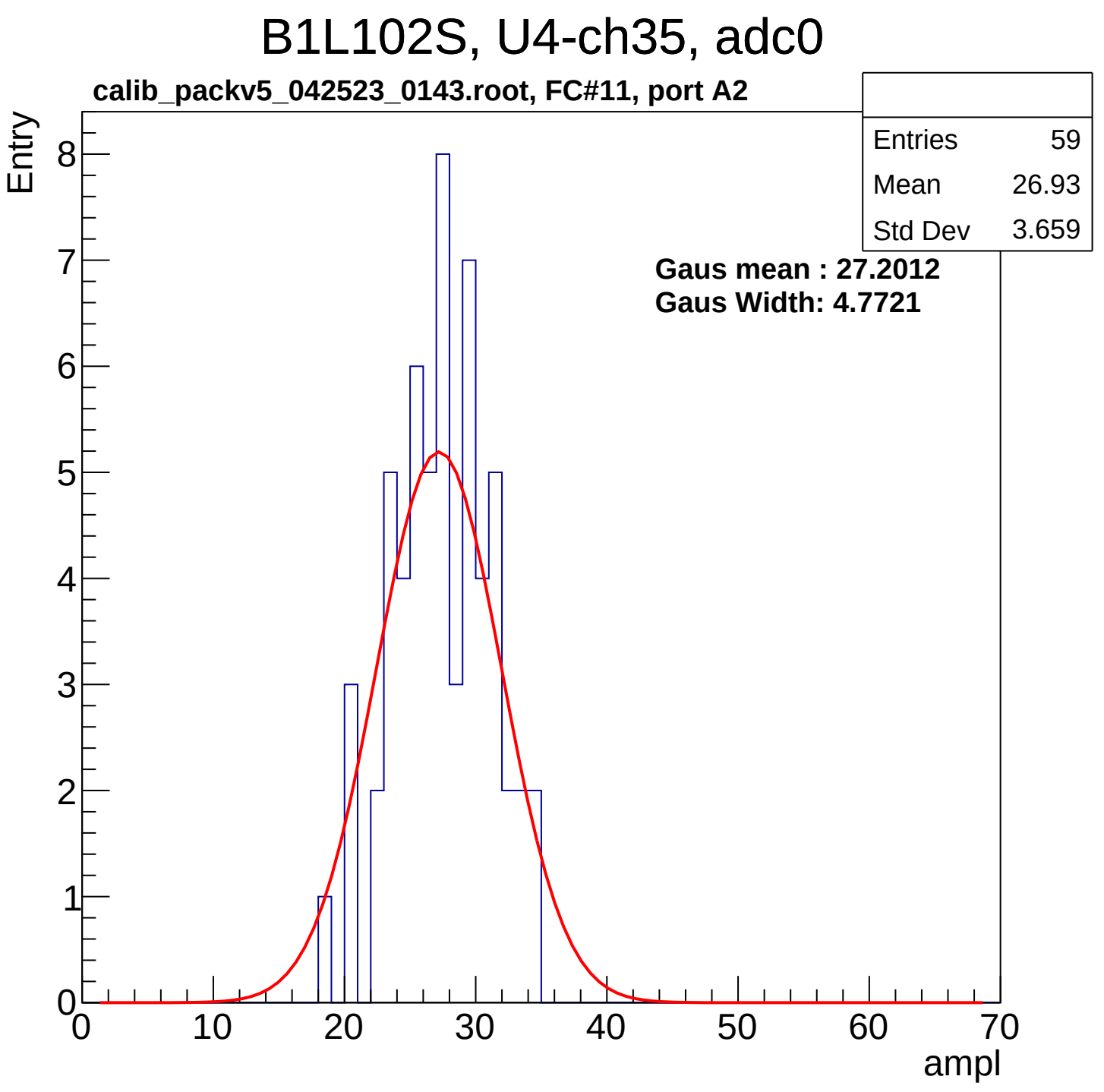
50
60
70
ampl


B1L102S, U4-ch35, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 26.93
Std Dev 3.659
Gaus mean : 27.2012
Gaus Width: 4.7721
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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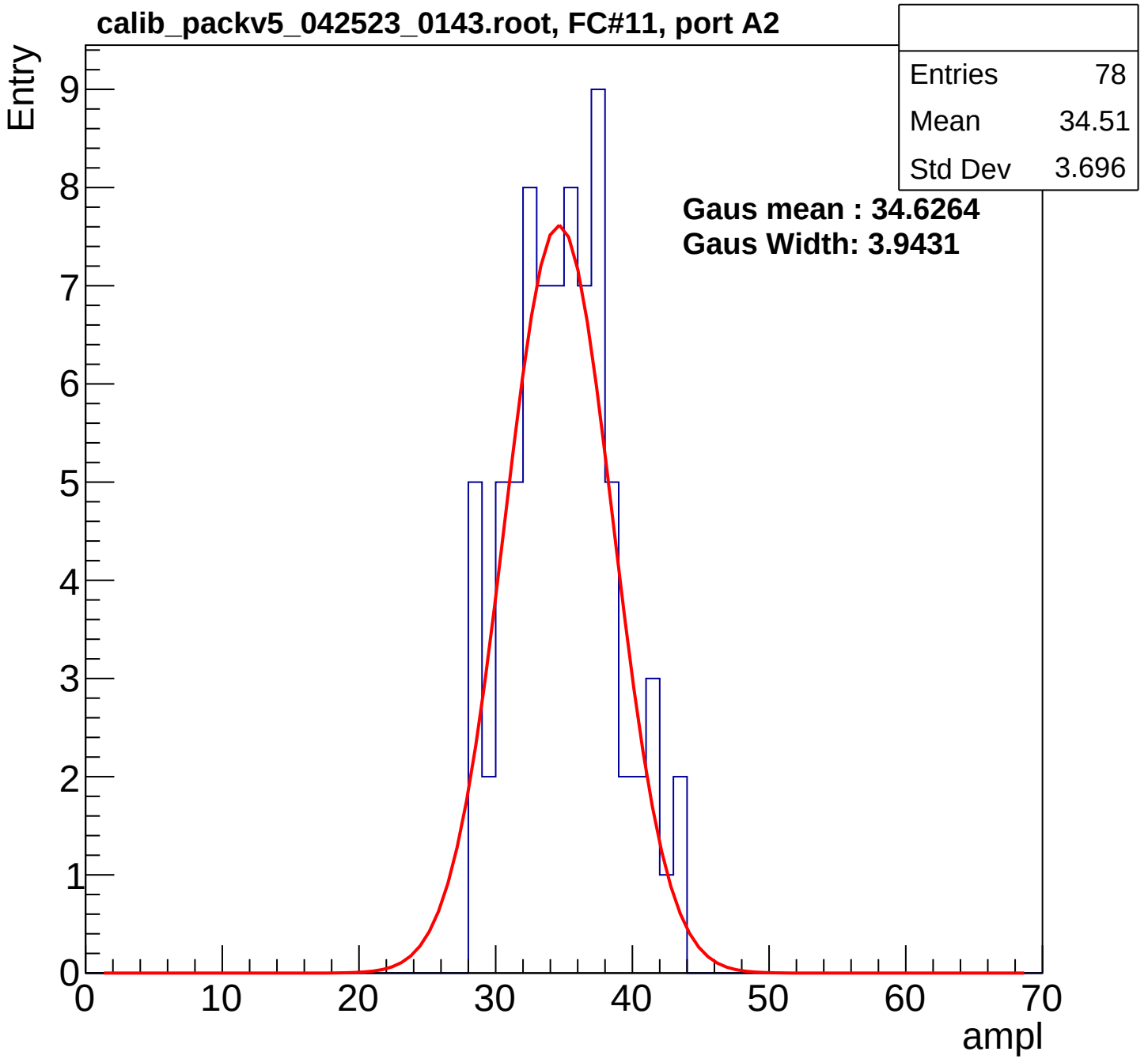
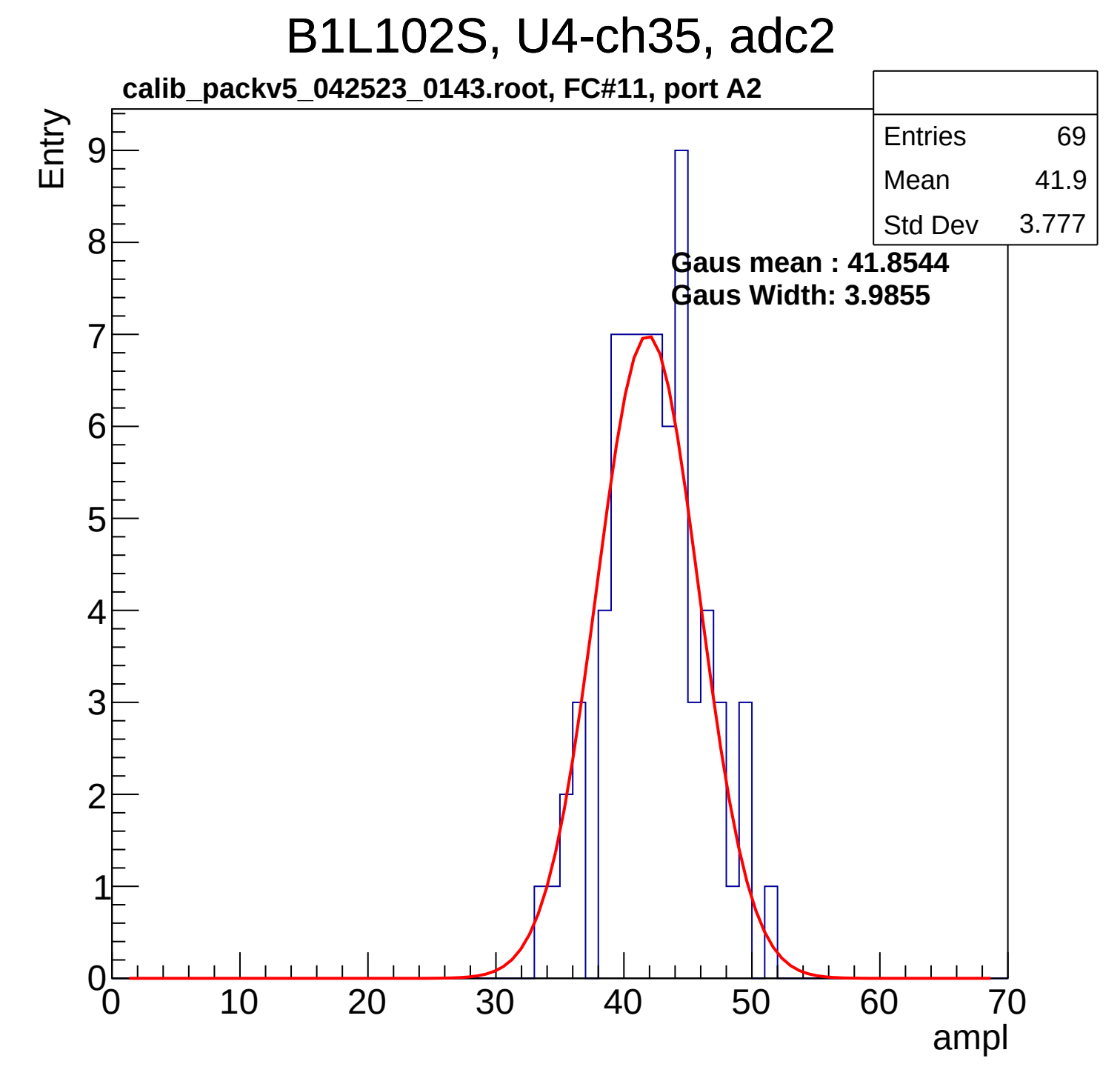

B1L102S, U4-ch35, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 78
Mean 34.51
Std Dev 3.696
Gaus mean : 34.6264
Gaus Width: 3.9431
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L102S, U4-ch35, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 41.9
Std Dev 3.777
Gaus mean : 41.8544
Gaus Width: 3.9855
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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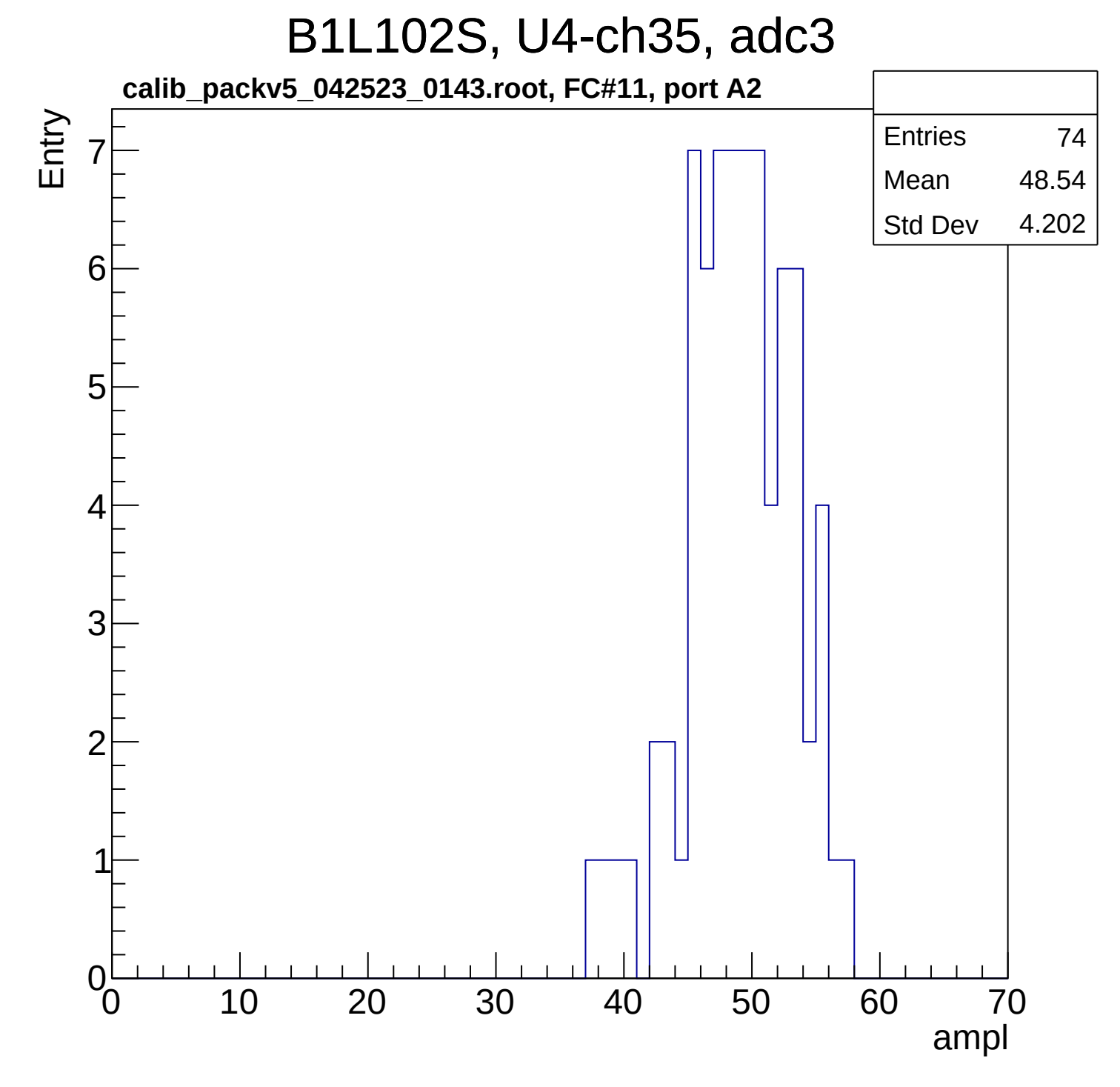
B1L102S, U4-ch35, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 48.54
Std Dev 4.202
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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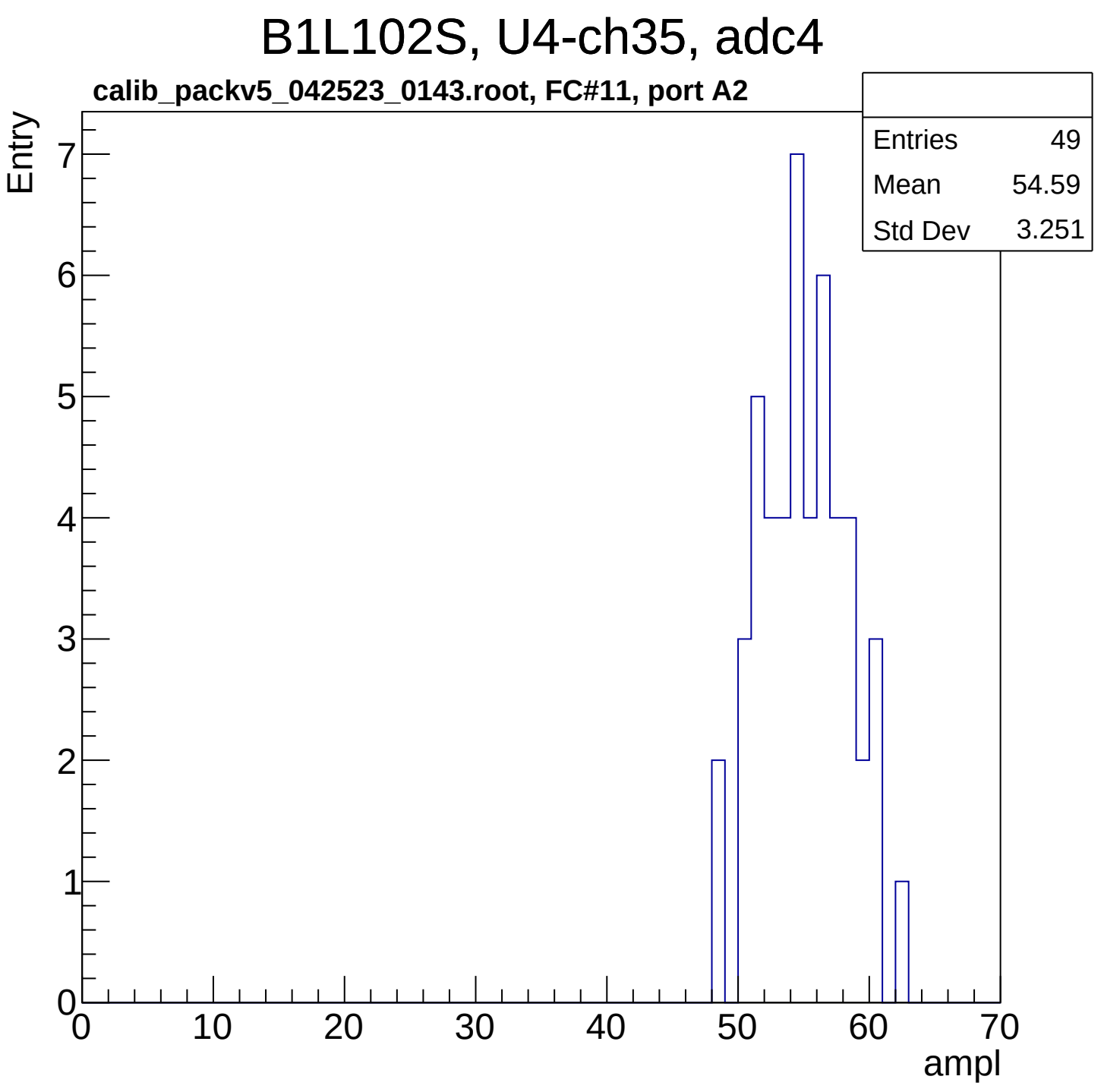
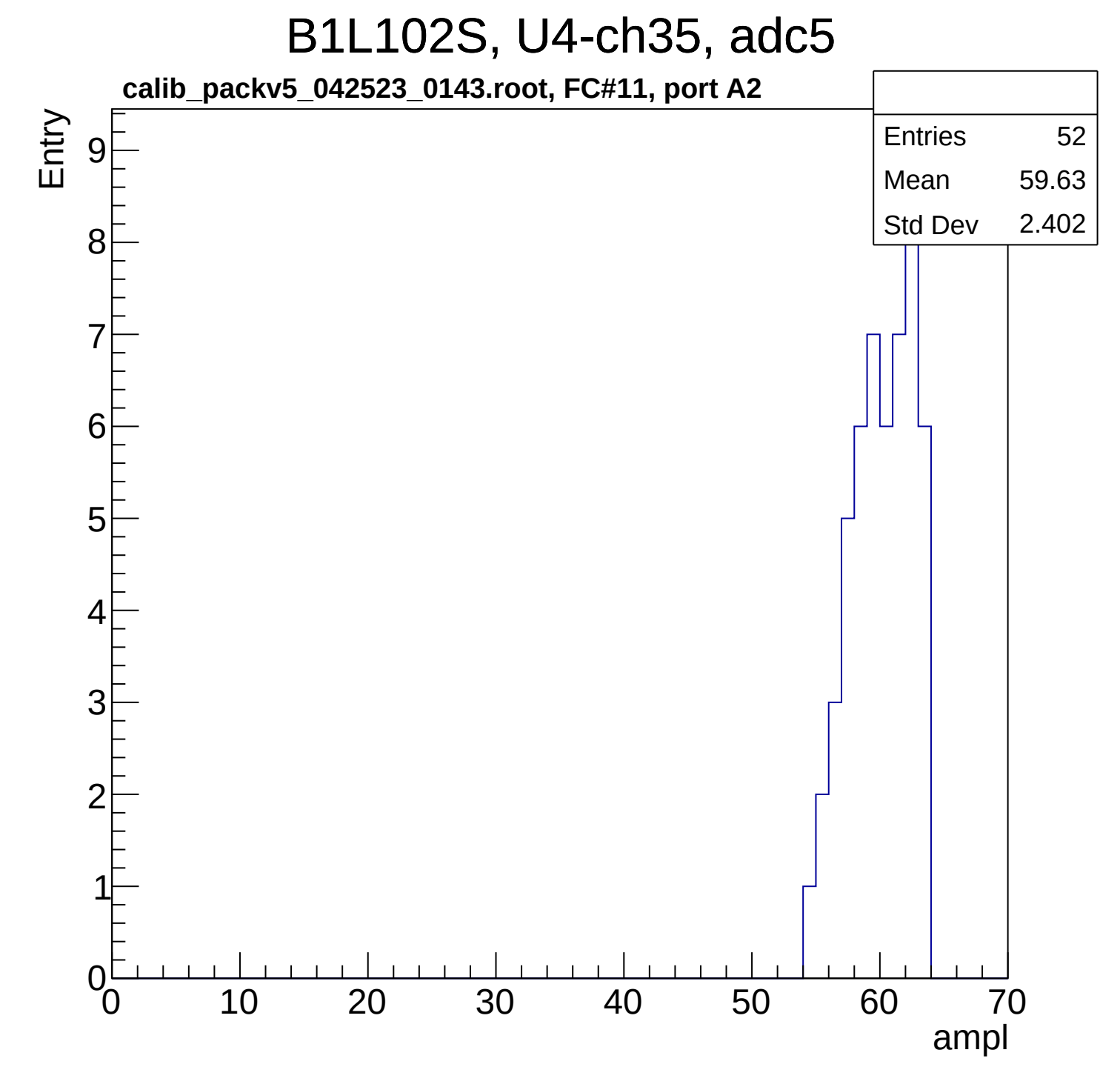
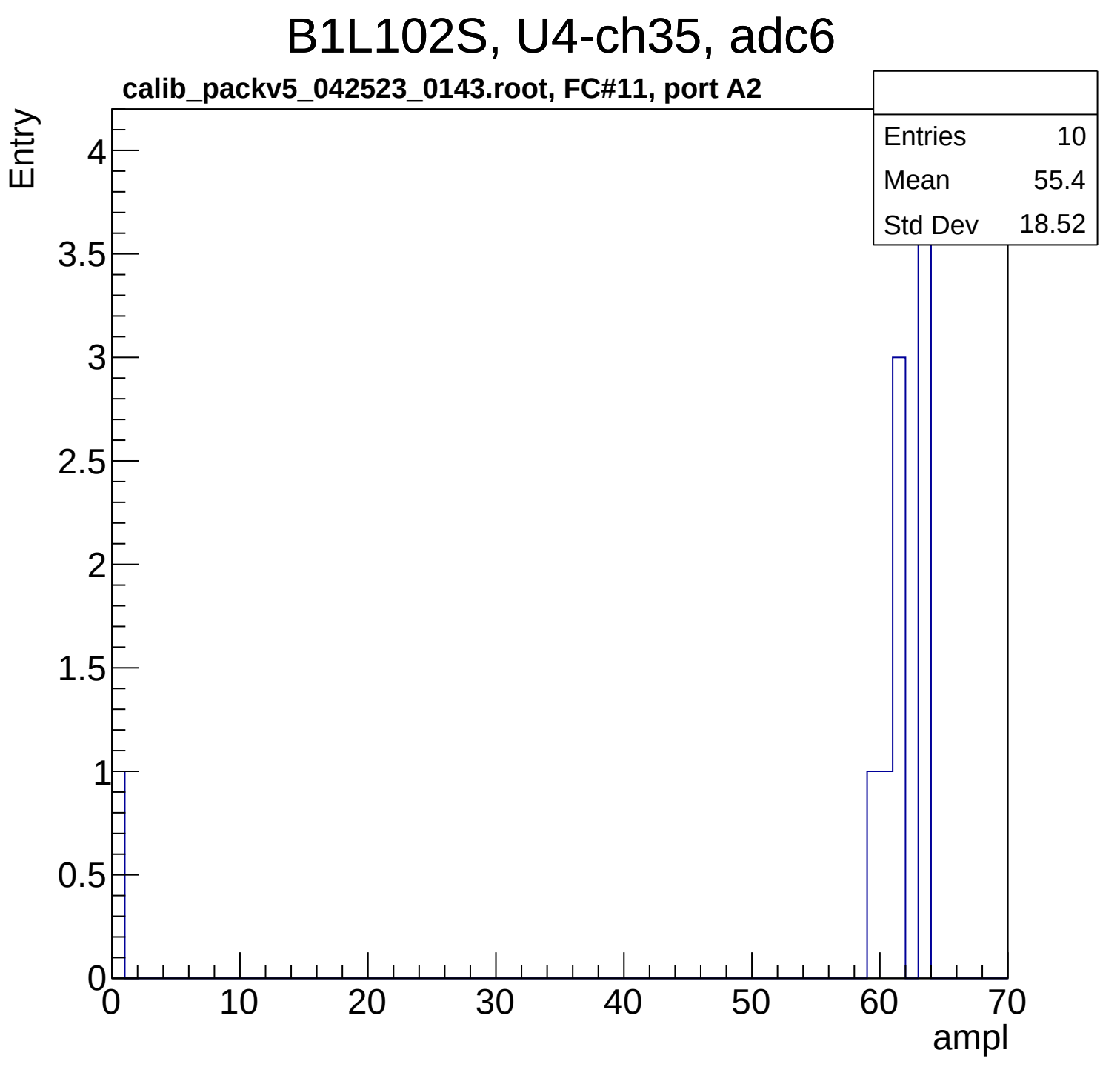

B1L102S, U4-ch35, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 54.59
Std Dev 3.251
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch35, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 52
Mean 59.63
Std Dev 2.402
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch35, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 10
Mean 55.4
Std Dev 18.52
Entry
ampl
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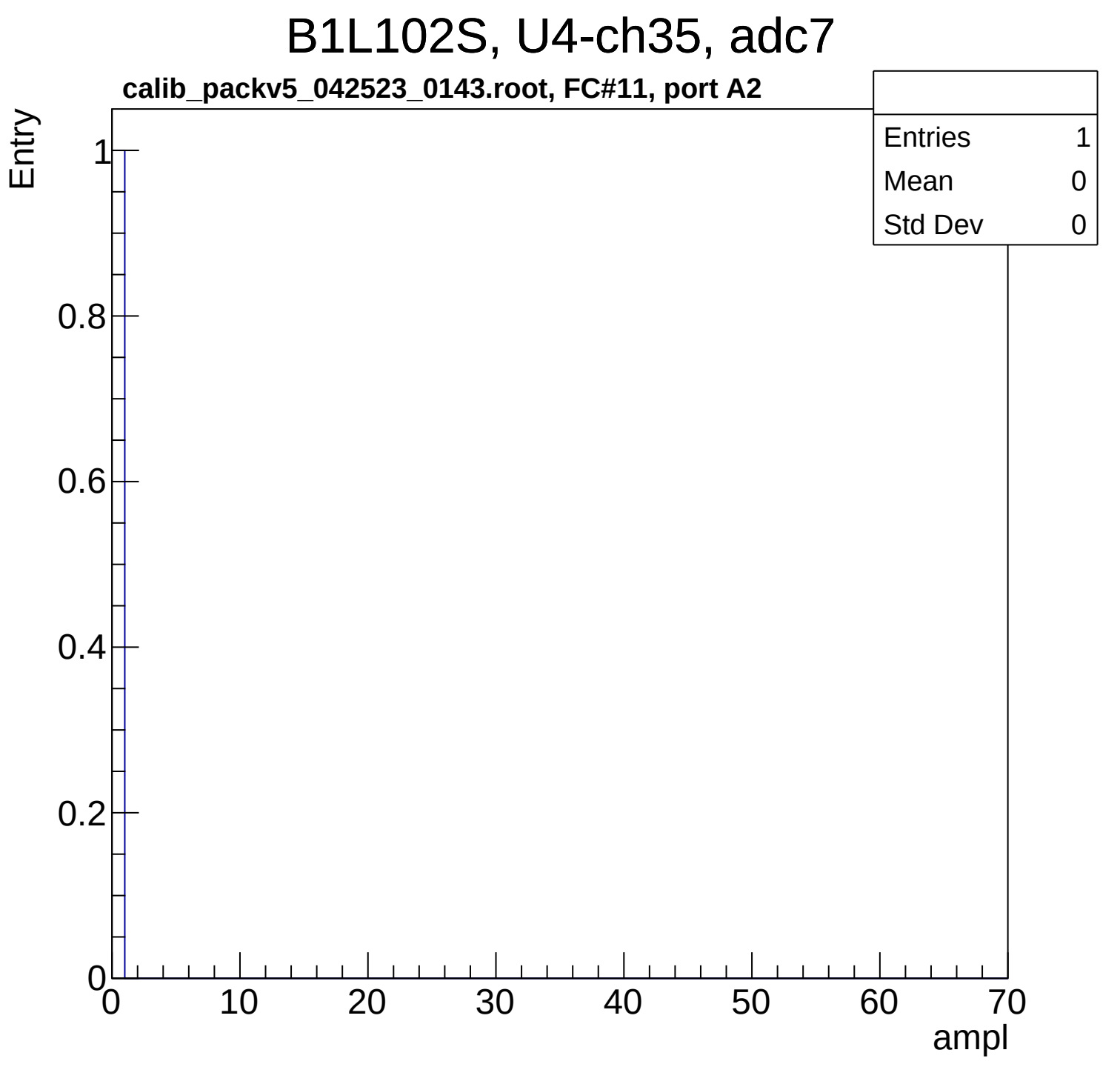
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U4-ch35, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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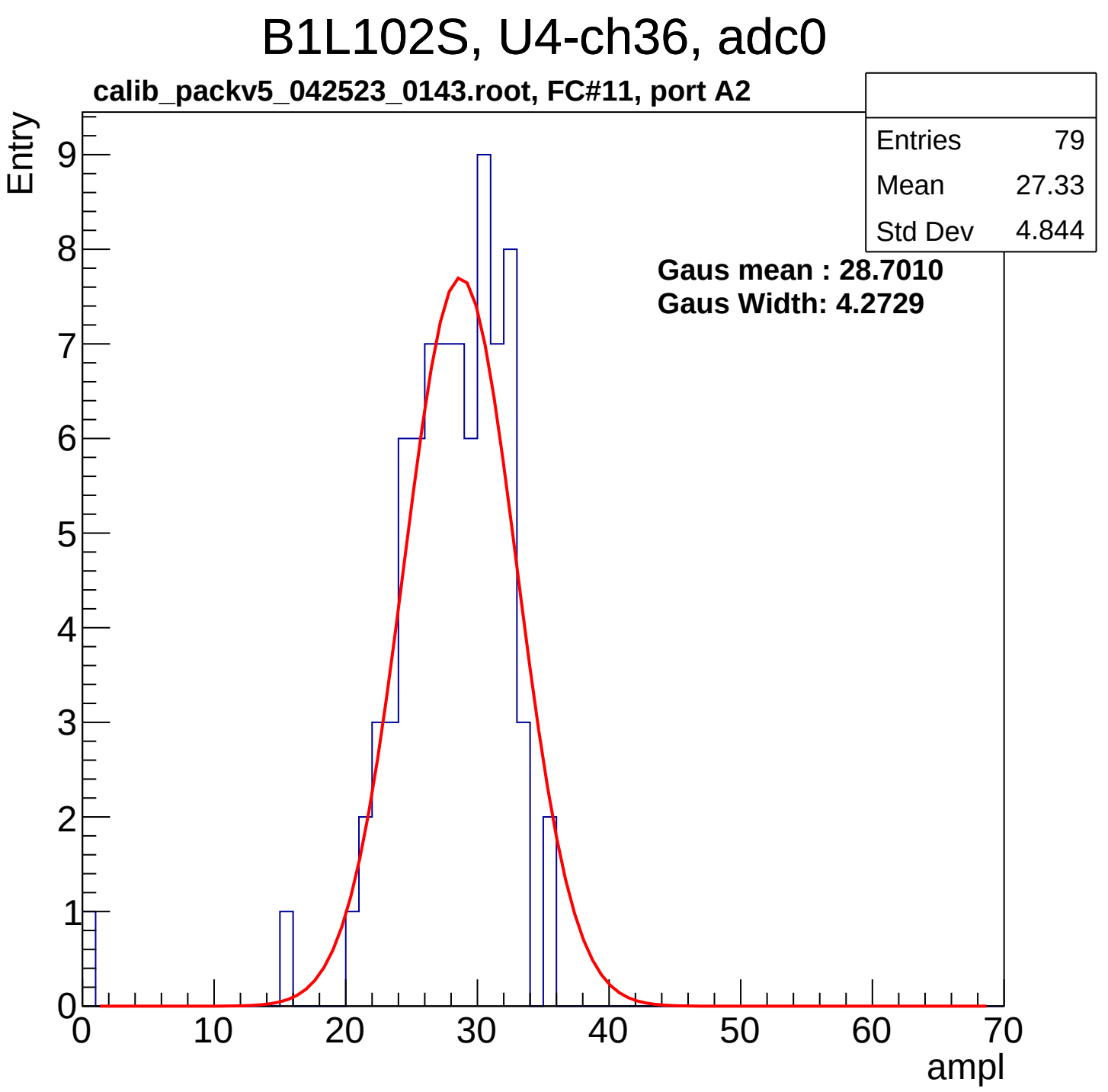
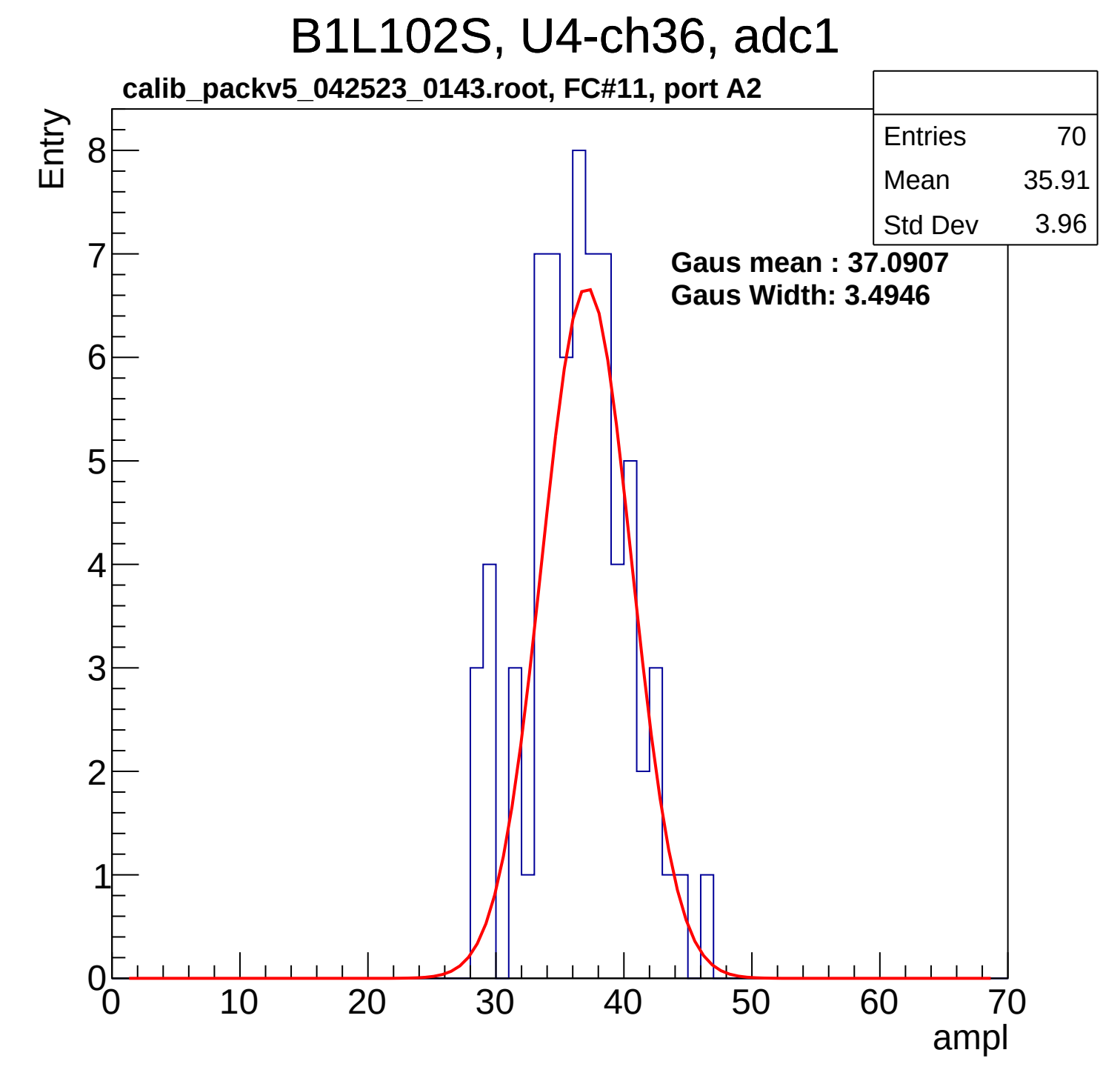
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch36, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 79
Mean 27.33
Std Dev 4.844
Gaus mean : 28.7010
Gaus Width: 4.2729
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch36, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 35.91
Std Dev 3.96
Gaus mean : 37.0907
Gaus Width: 3.4946
Entry
ampl
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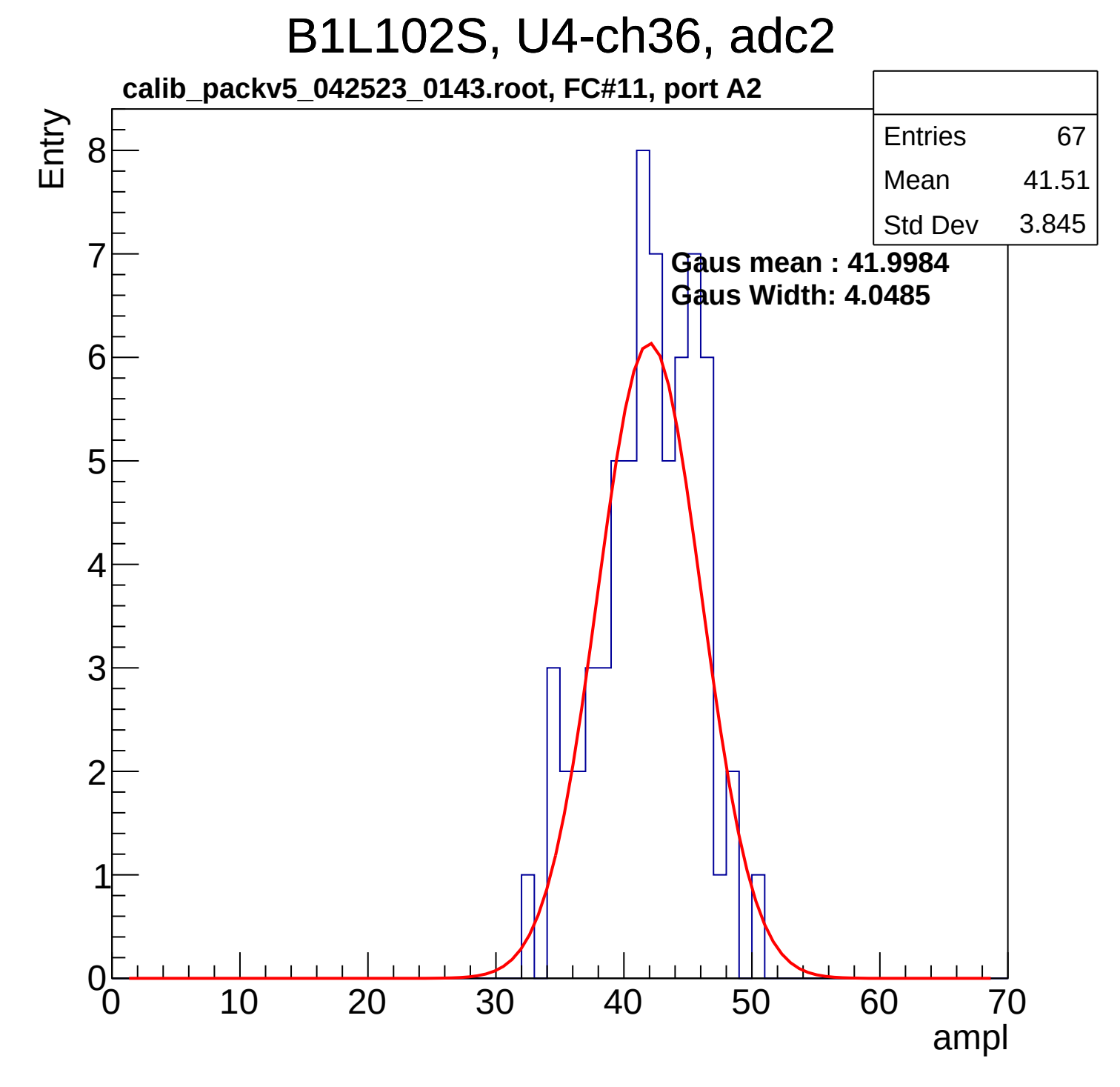
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch36, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 41.51
Std Dev 3.845
Gaus mean : 41.9984
Gaus Width: 4.0485
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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60
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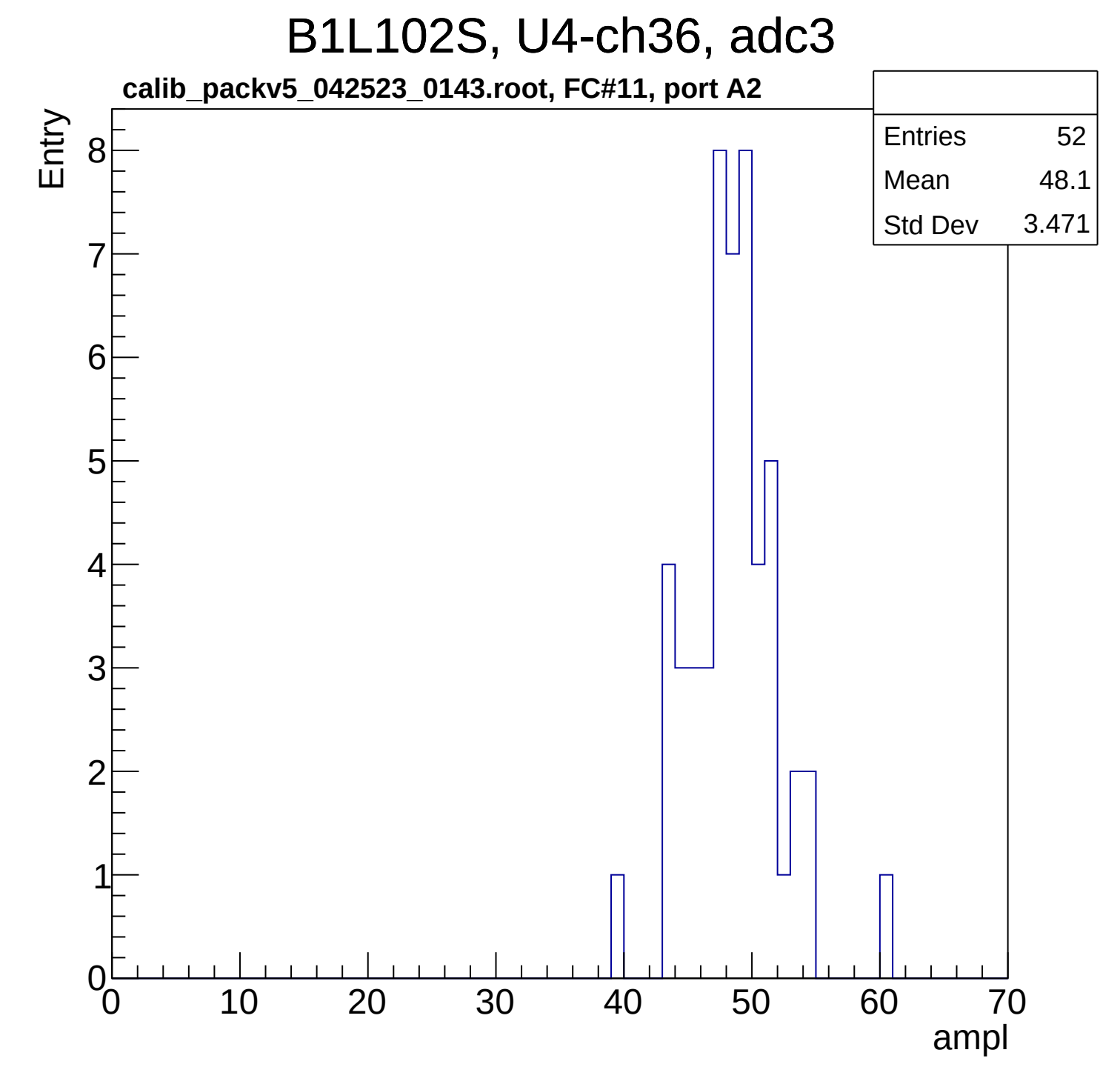
B1L102S, U4-ch36, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 52
Mean 48.1
Std Dev 3.471
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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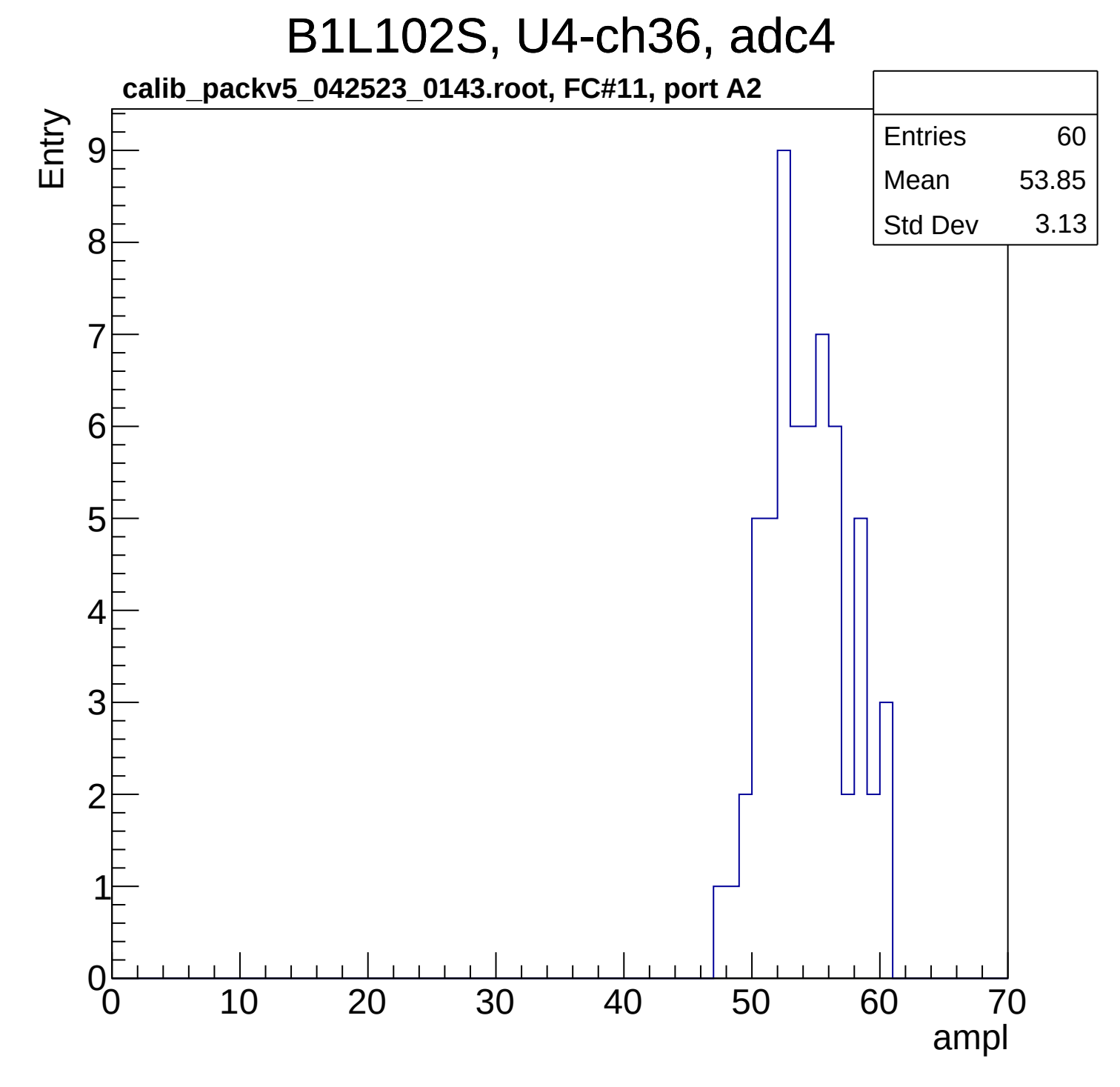
B1L102S, U4-ch36, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 53.85
Std Dev 3.13
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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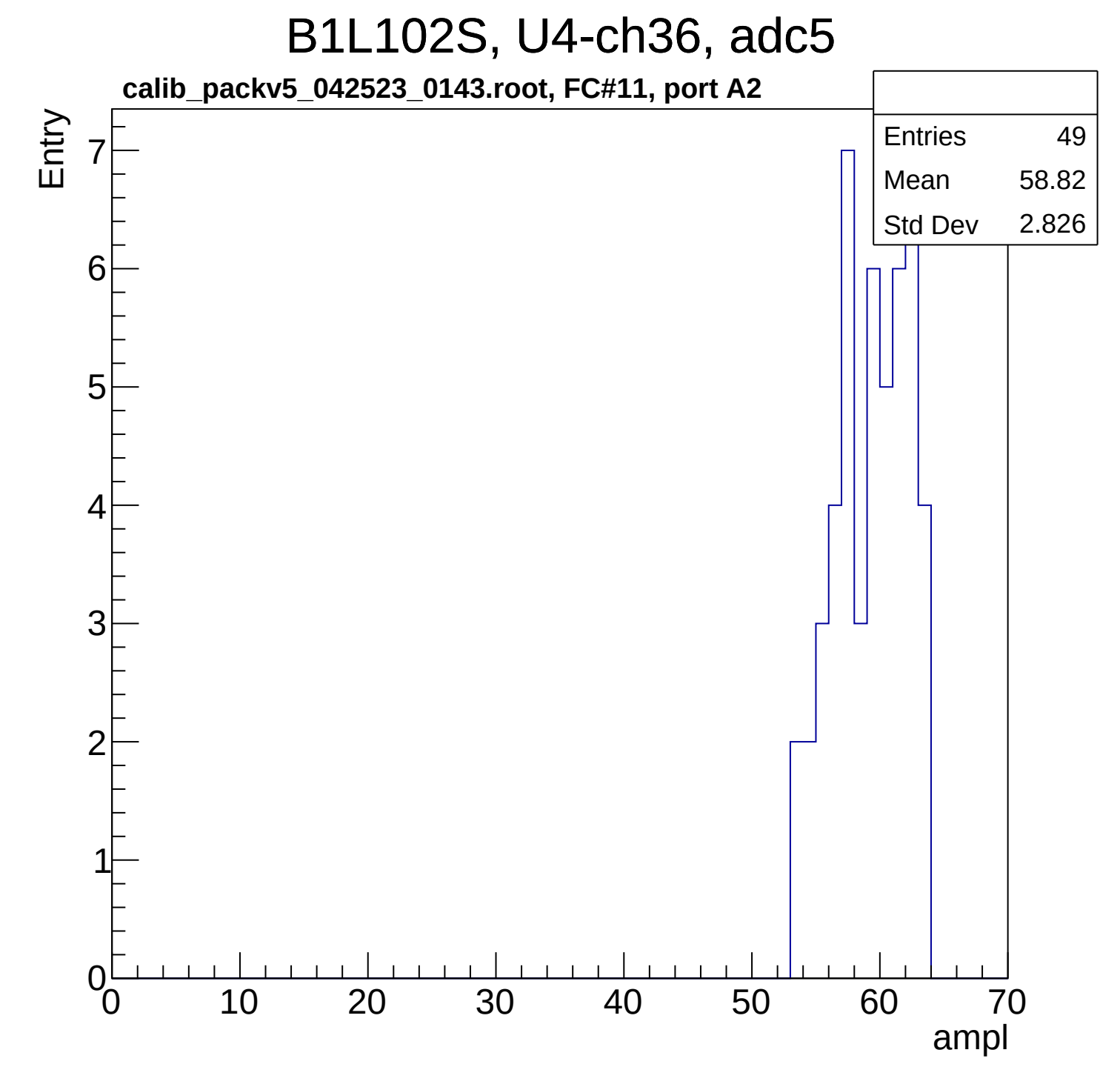
B1L102S, U4-ch36, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 58.82
Std Dev 2.826
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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60
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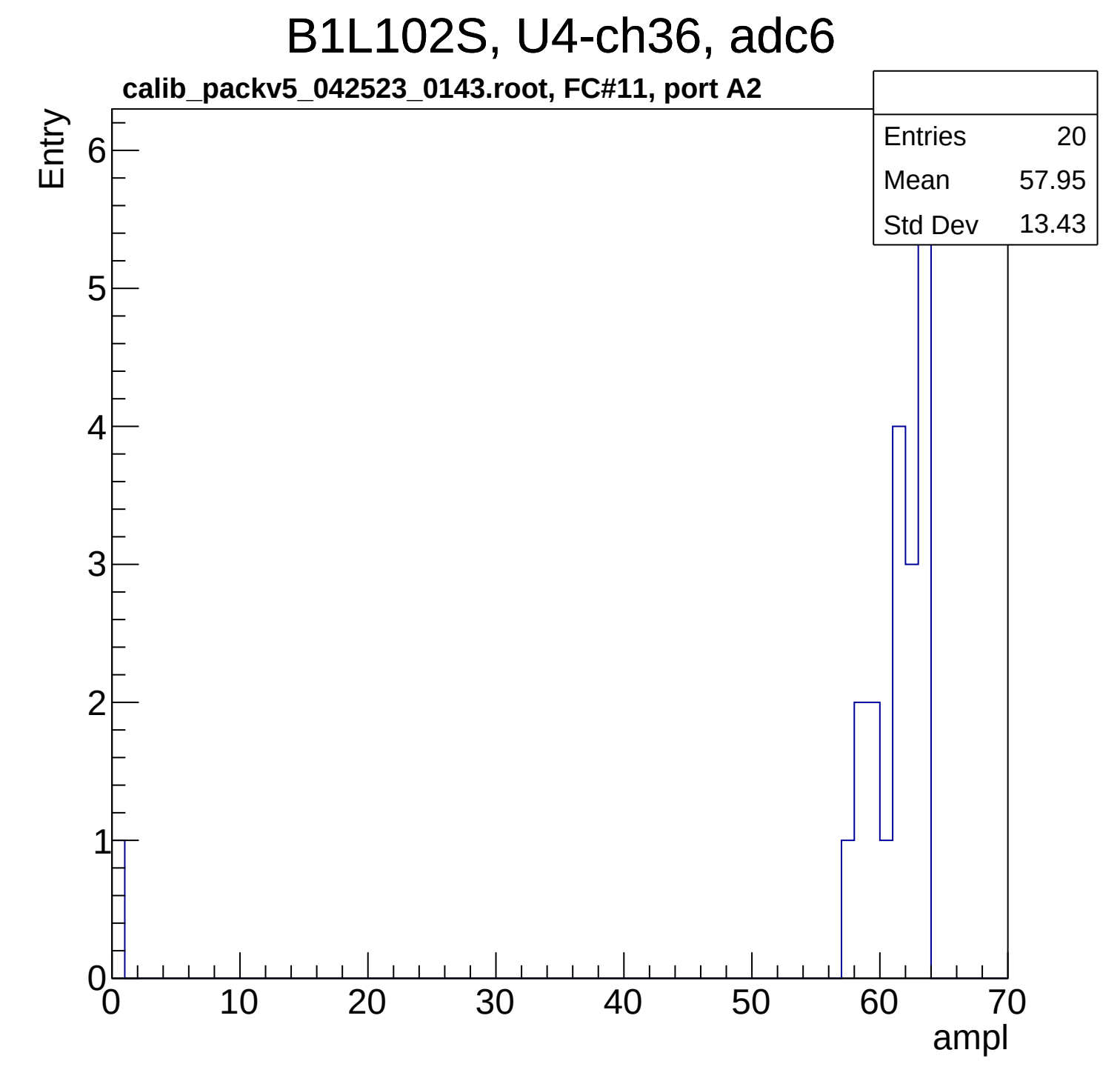
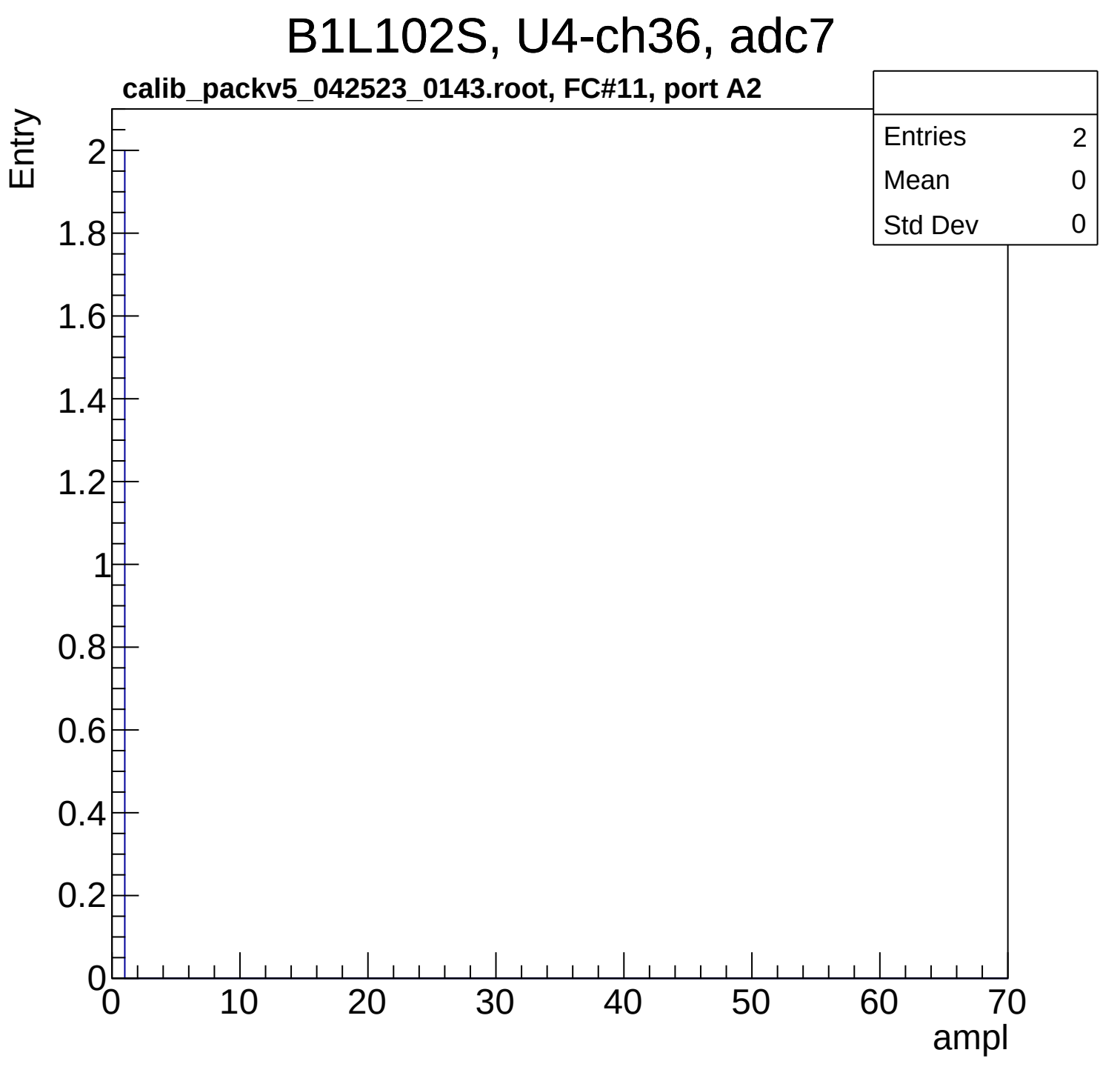

B1L102S, U4-ch36, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 20
Mean 57.95
Std Dev 13.43
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L102S, U4-ch36, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
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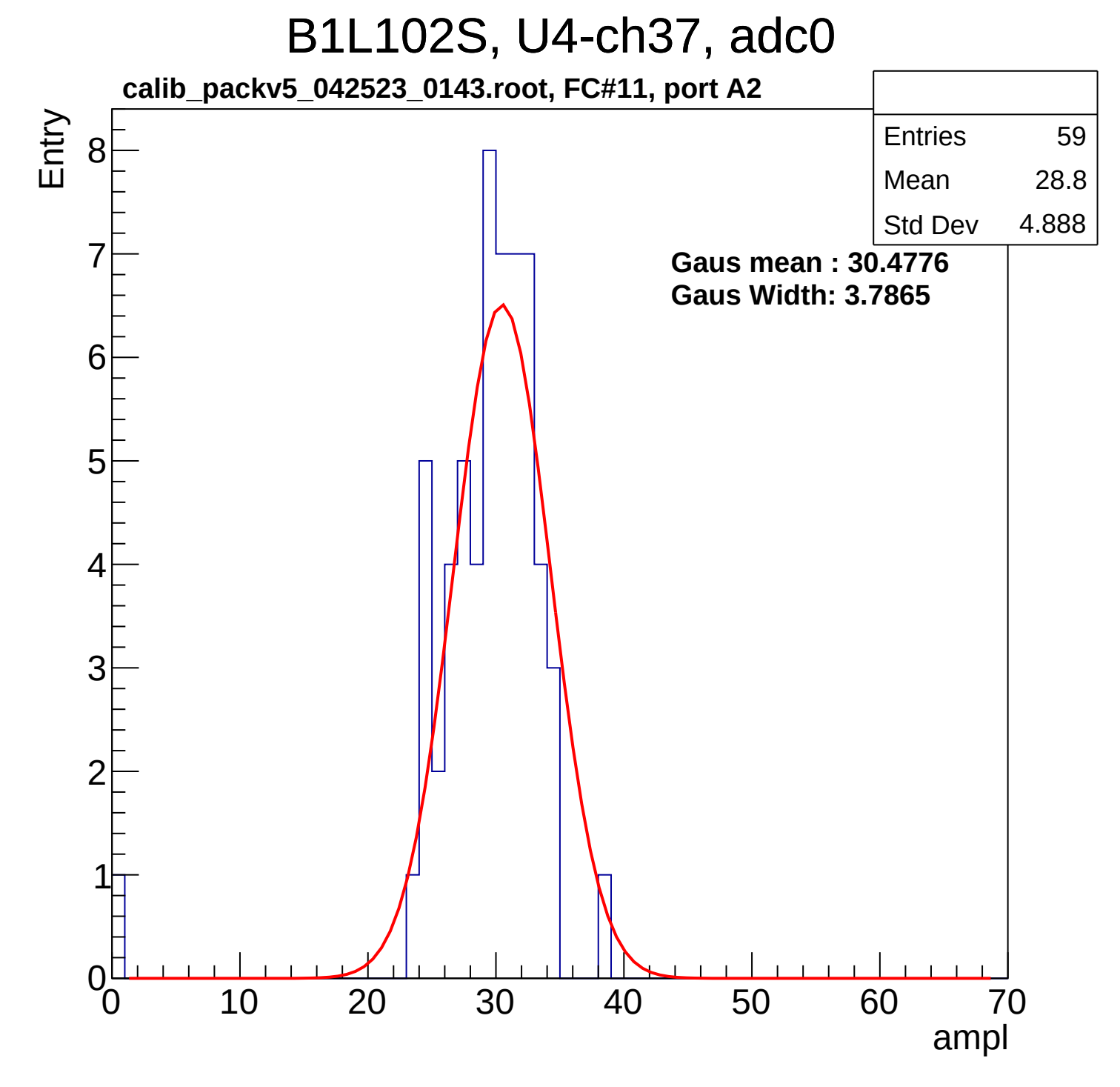
60
70


B1L102S, U4-ch37, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 28.8
Std Dev 4.888
Gaus mean : 30.4776
Gaus Width: 3.7865
Entry
ampl
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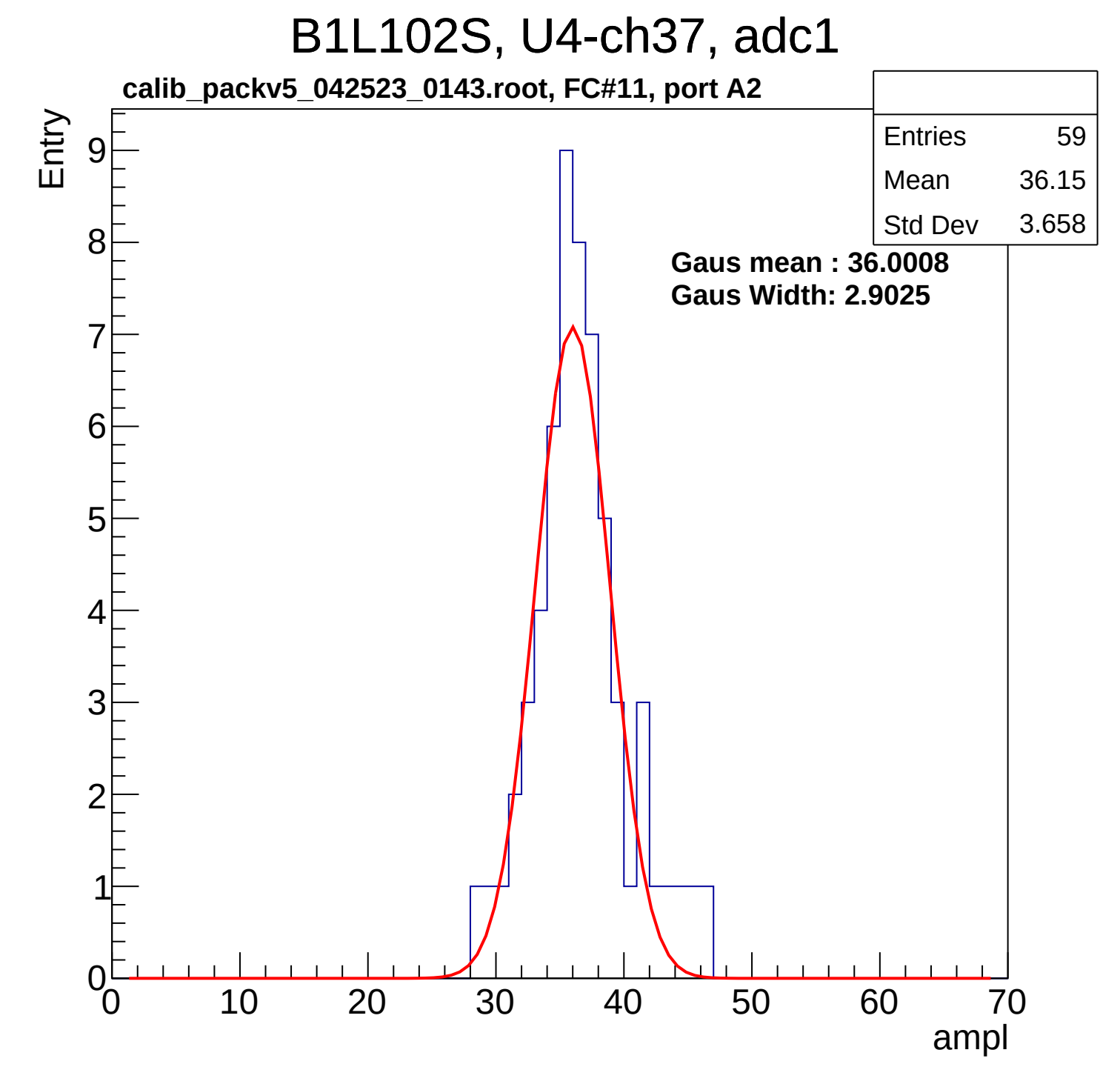
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch37, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 36.15
Std Dev 3.658
Gaus mean : 36.0008
Gaus Width: 2.9025
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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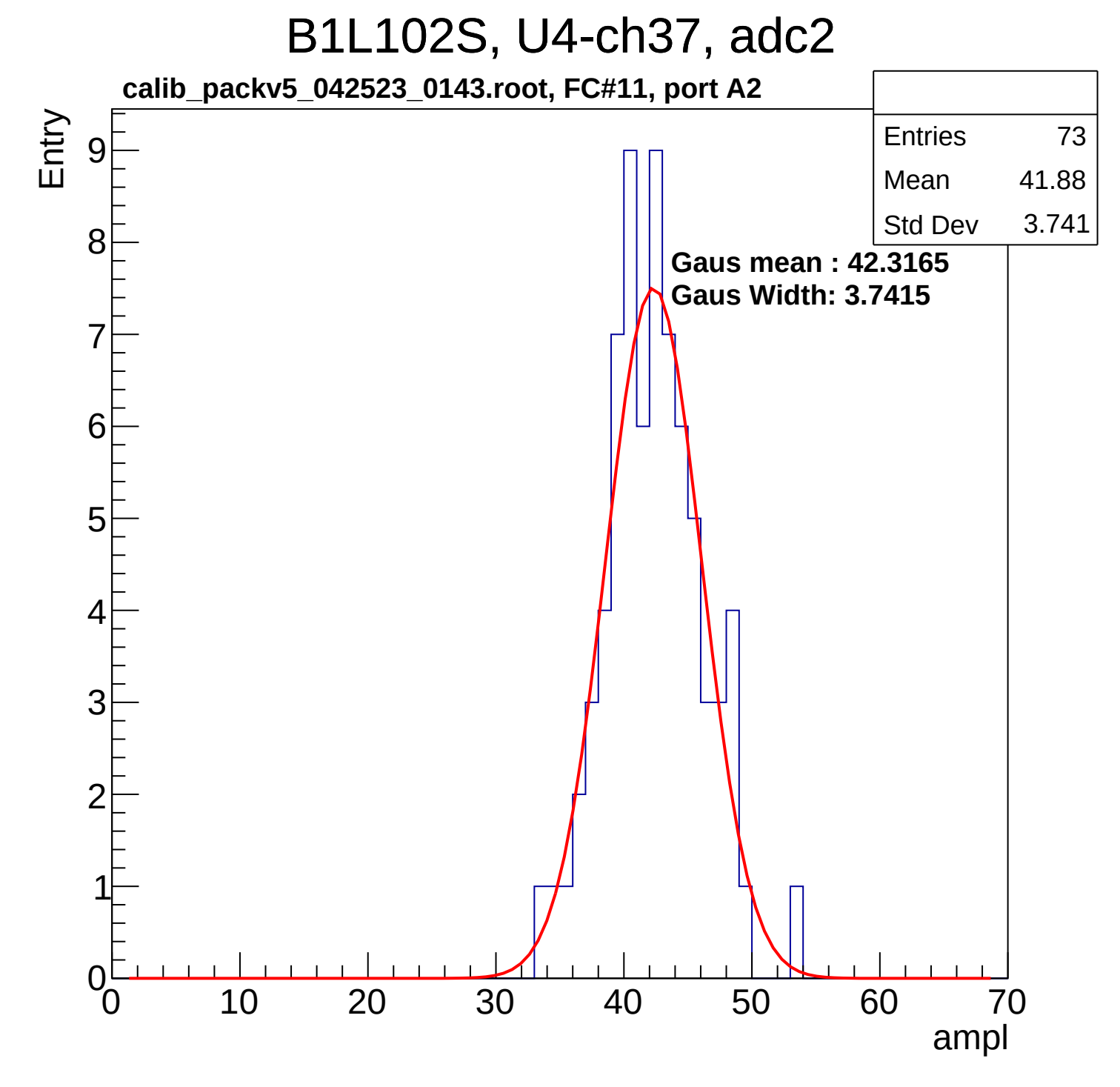
60
70


B1L102S, U4-ch37, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 41.88
Std Dev 3.741
Gaus mean : 42.3165
Gaus Width: 3.7415
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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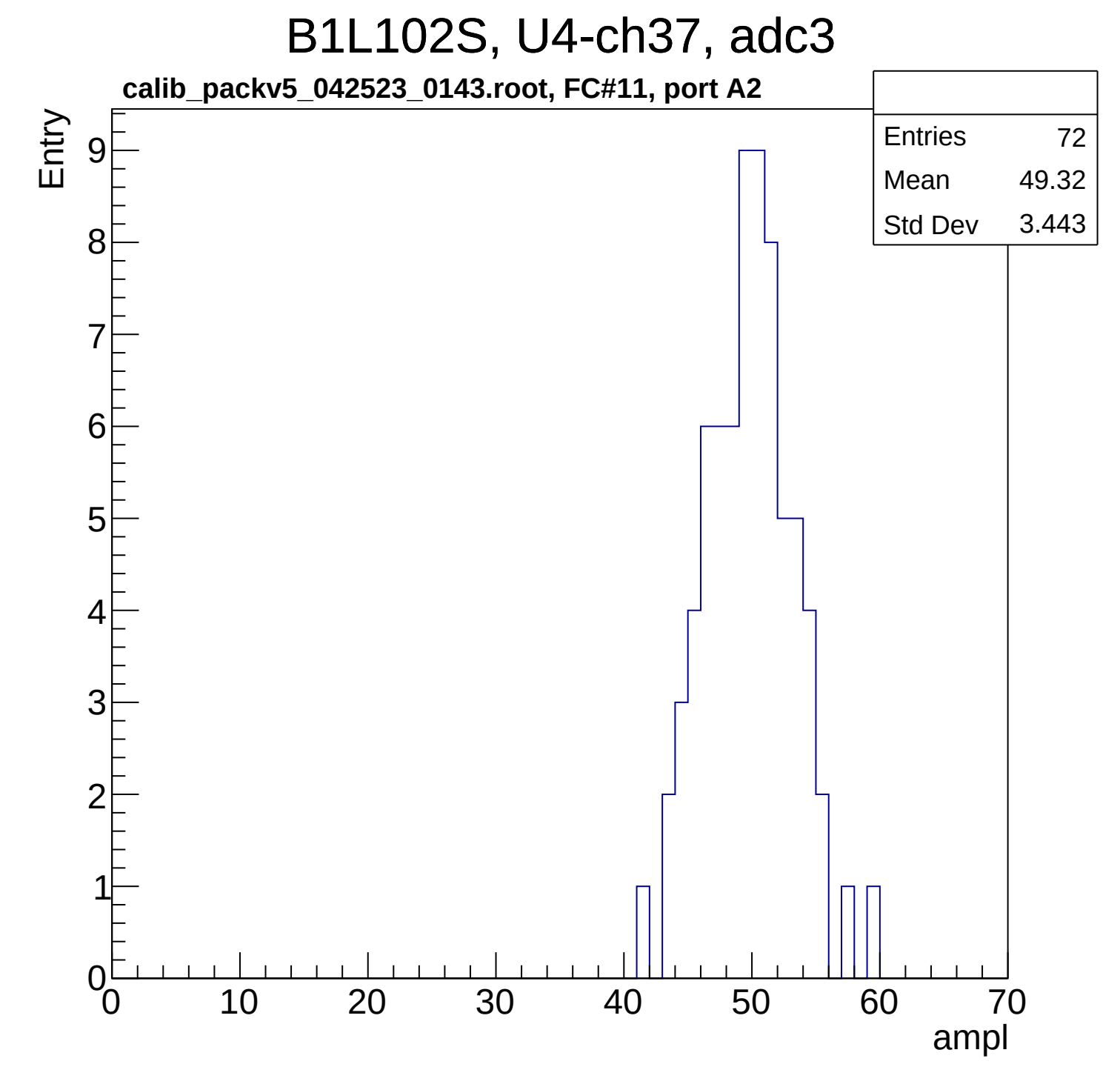
B1L102S, U4-ch37, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 72
Mean 49.32
Std Dev 3.443
Entry
ampl
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5
6
7
8
9
0
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40
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60
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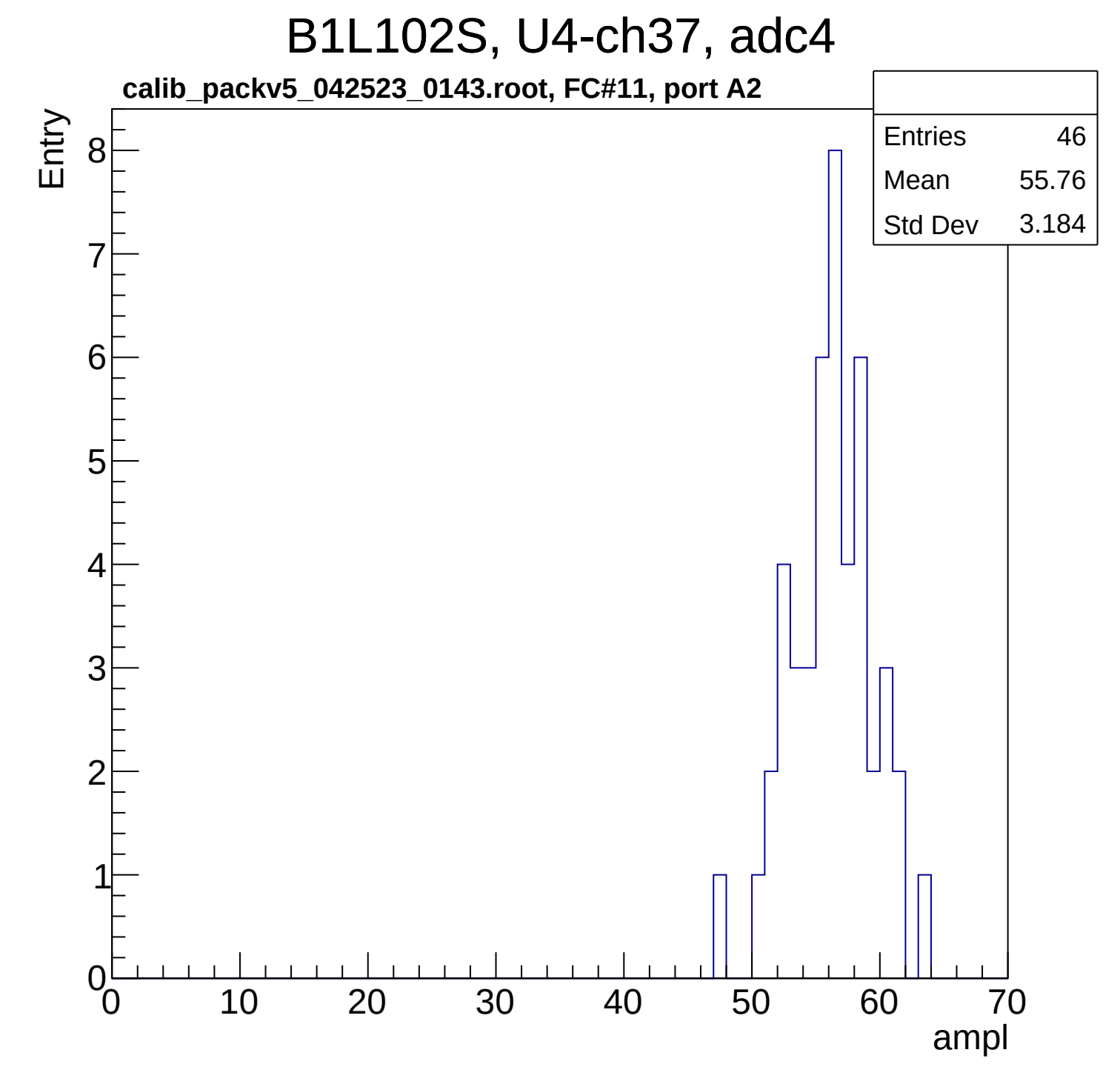
B1L102S, U4-ch37, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 46
Mean 55.76
Std Dev 3.184
Entry
ampl
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6
7
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0
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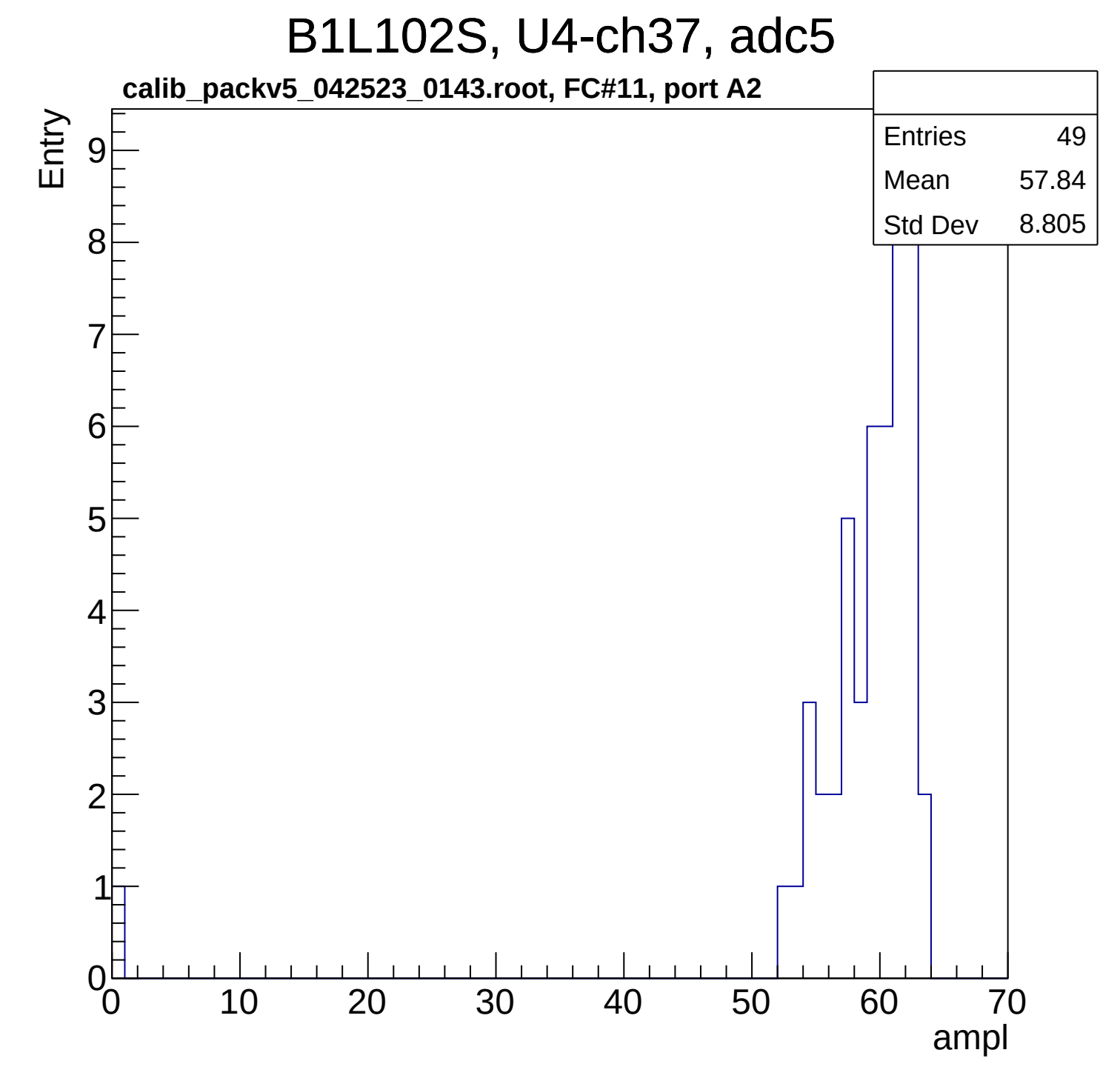
B1L102S, U4-ch37, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 57.84
Std Dev 8.805
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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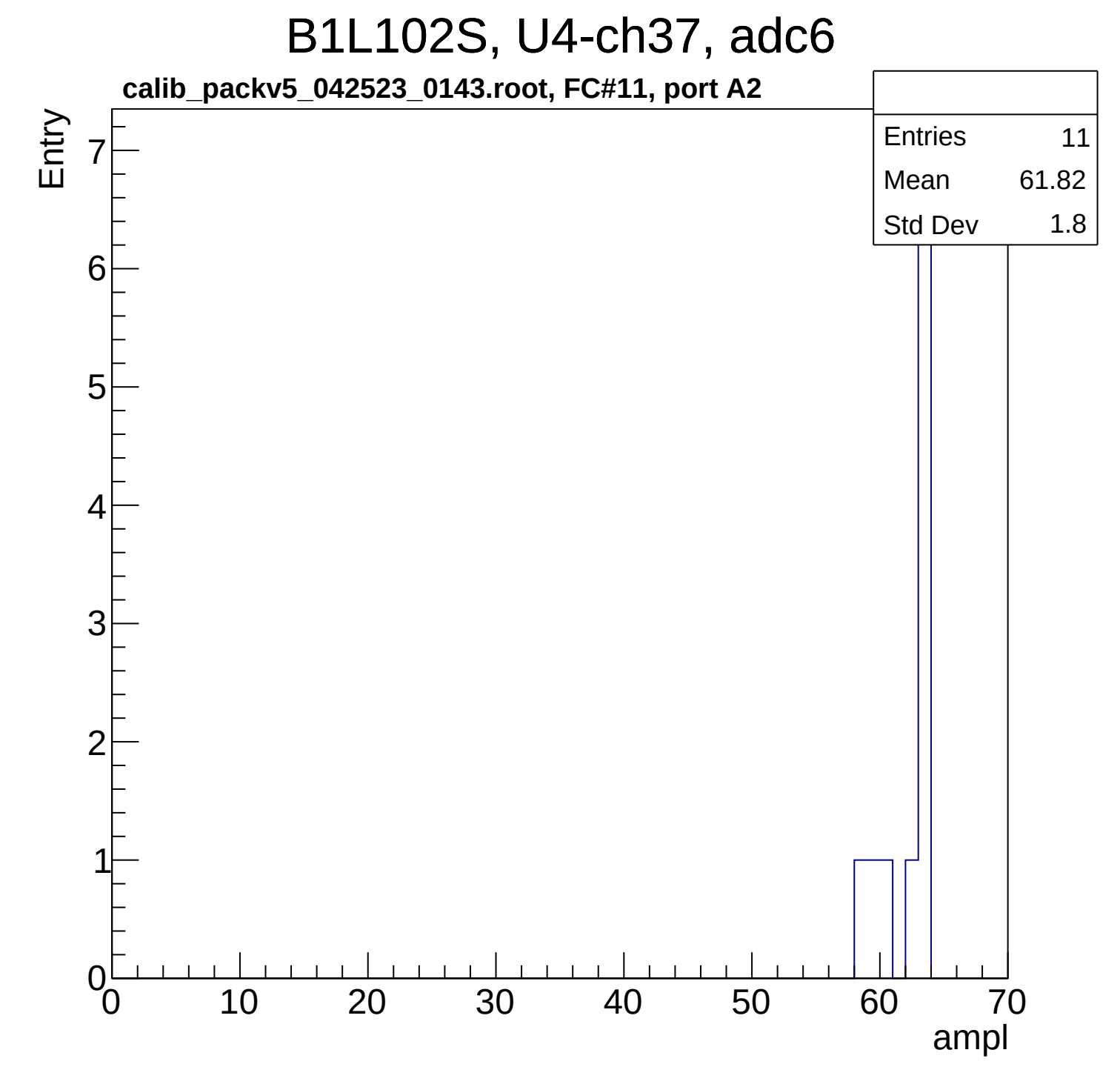
60
70


B1L102S, U4-ch37, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 11
Mean 61.82
Std Dev 1.8
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
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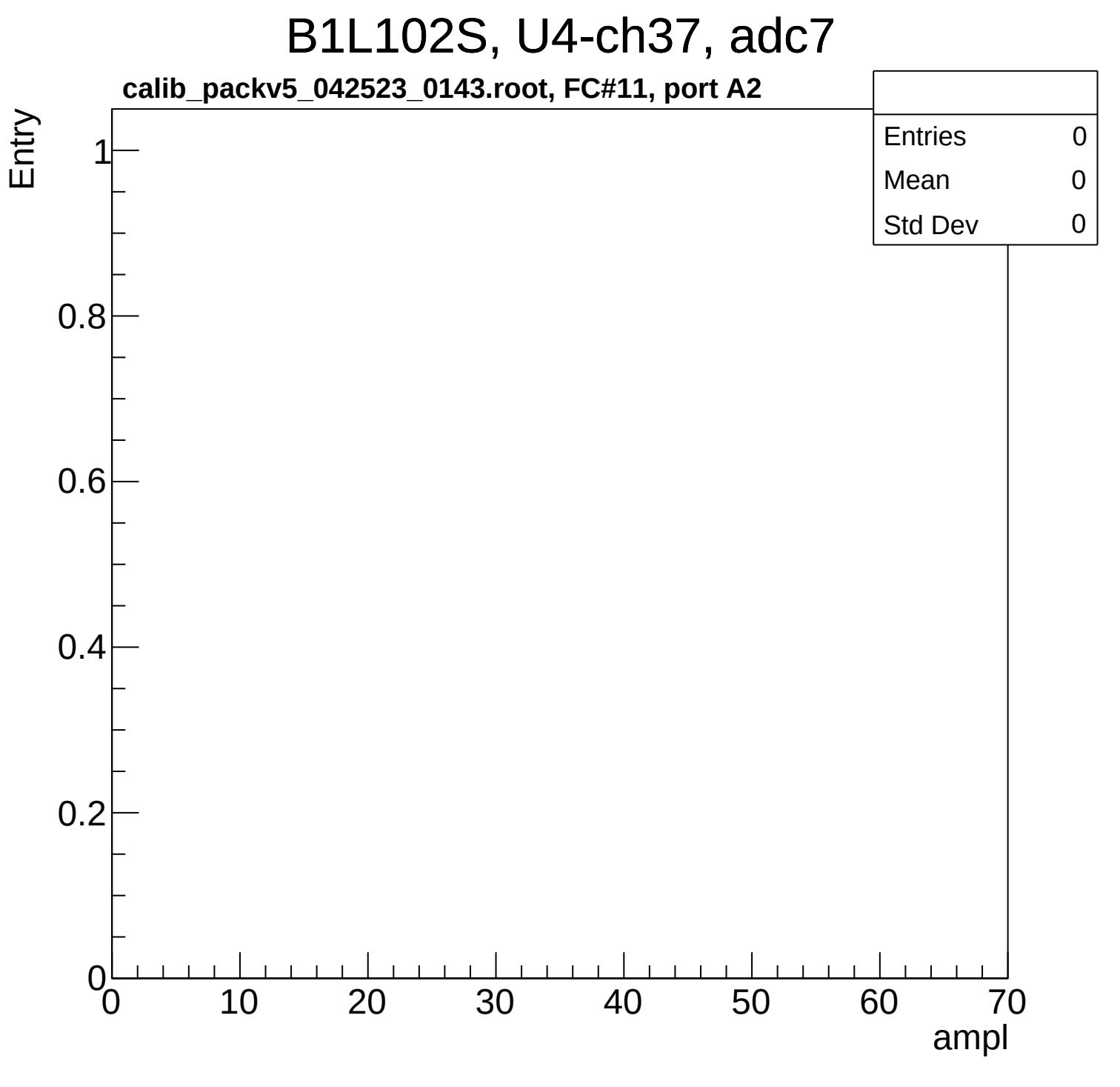
60
70


B1L102S, U4-ch37, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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0.6
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10
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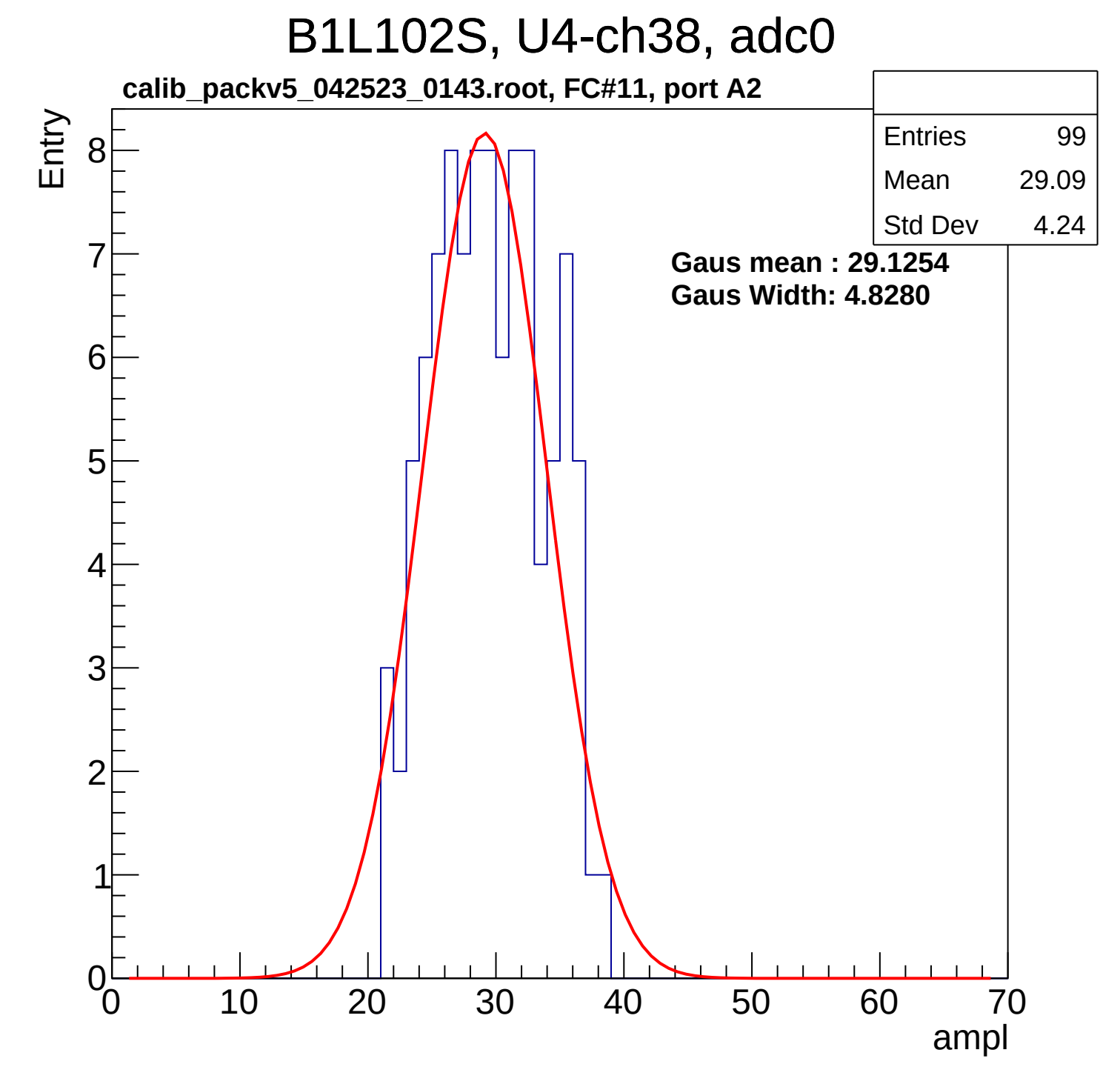
50
60
70
ampl


B1L102S, U4-ch38, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 99
Mean 29.09
Std Dev 4.24
Gaus mean : 29.1254
Gaus Width: 4.8280
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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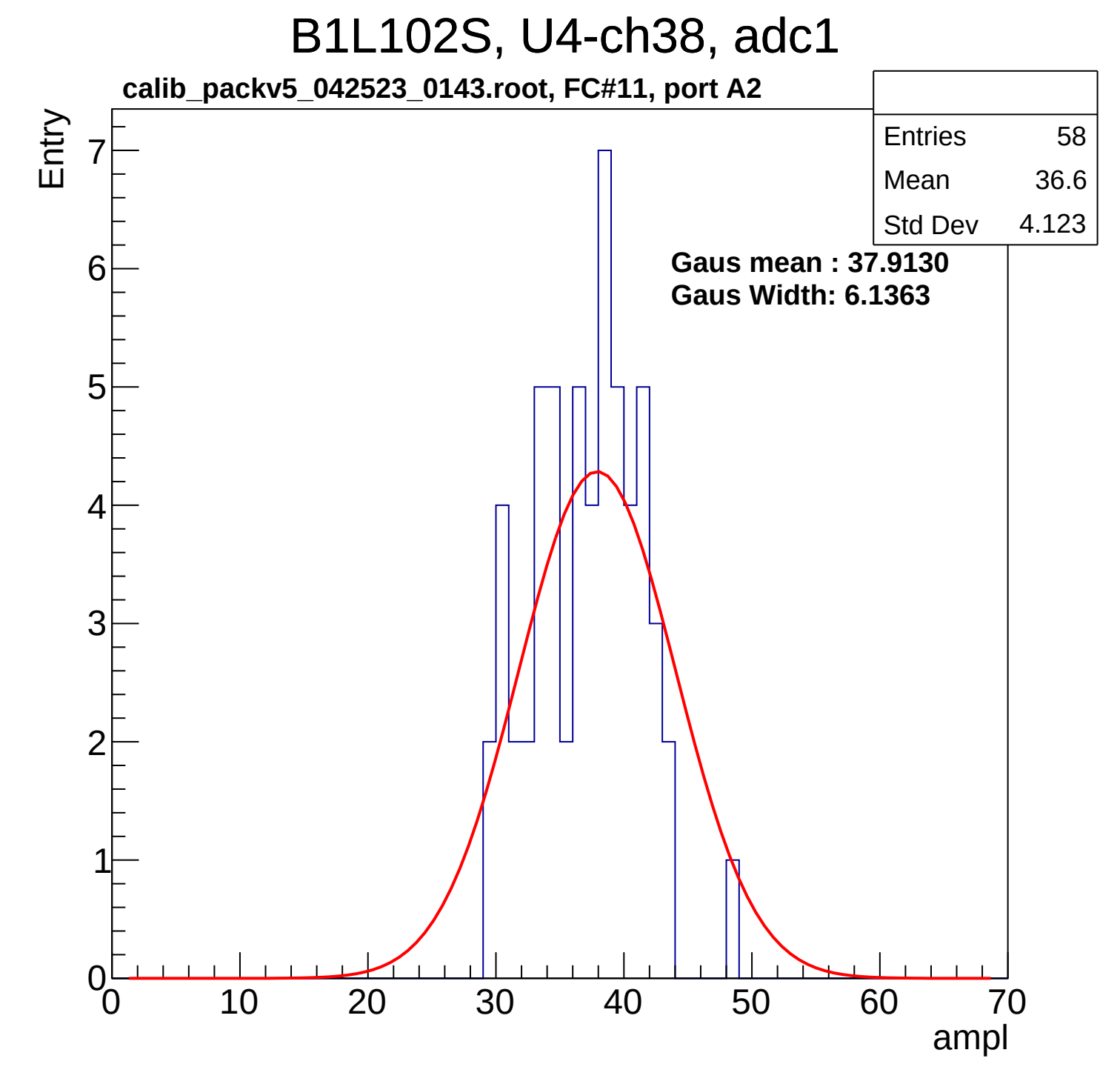
40
50
60
70


B1L102S, U4-ch38, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 36.6
Std Dev 4.123
Gaus mean : 37.9130
Gaus Width: 6.1363
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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50
60
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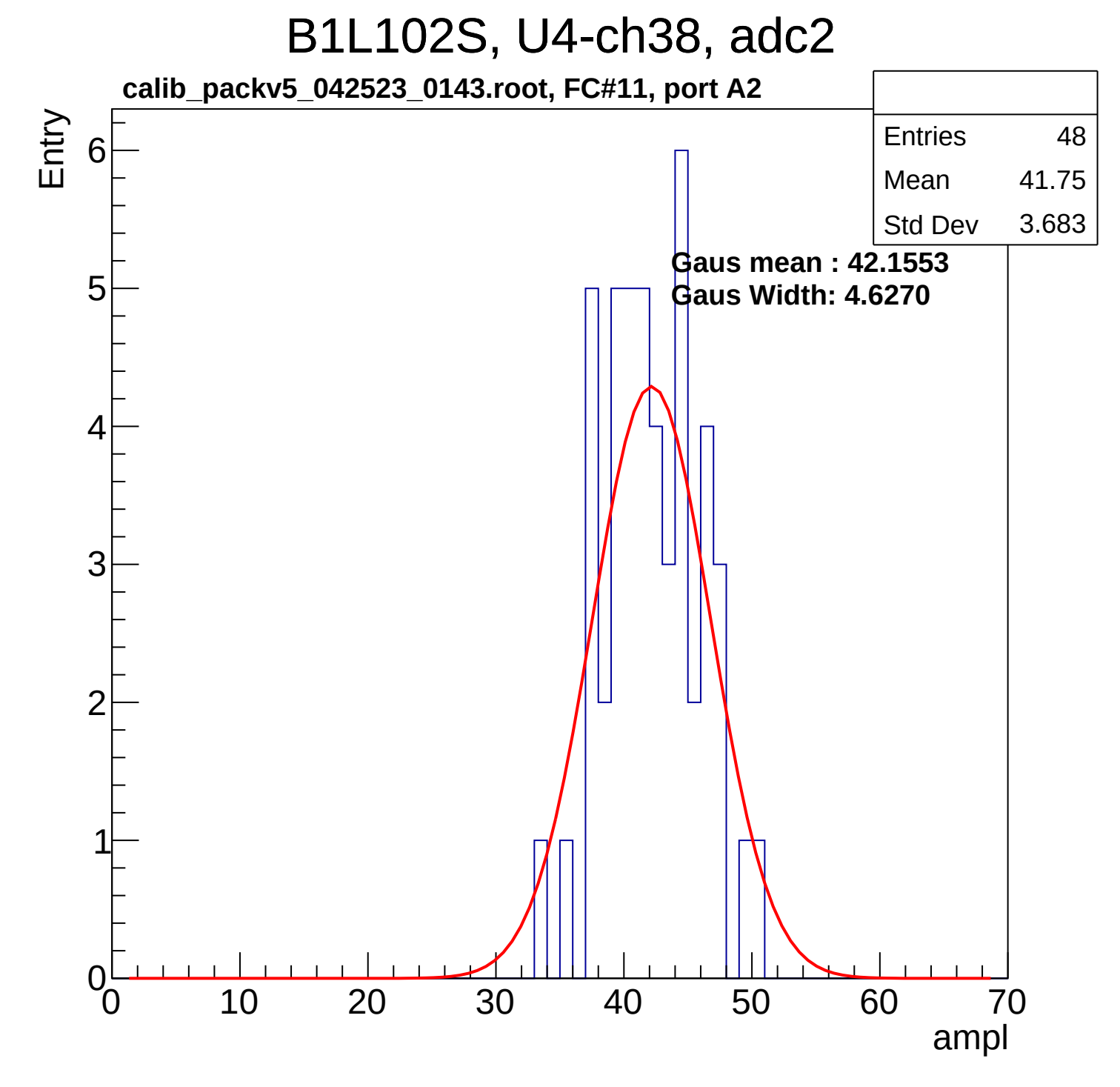
B1L102S, U4-ch38, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 48
Mean 41.75
Std Dev 3.683
Gaus mean : 42.1553
Gaus Width: 4.6270
Entry
ampl
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2
3
4
5
6
0
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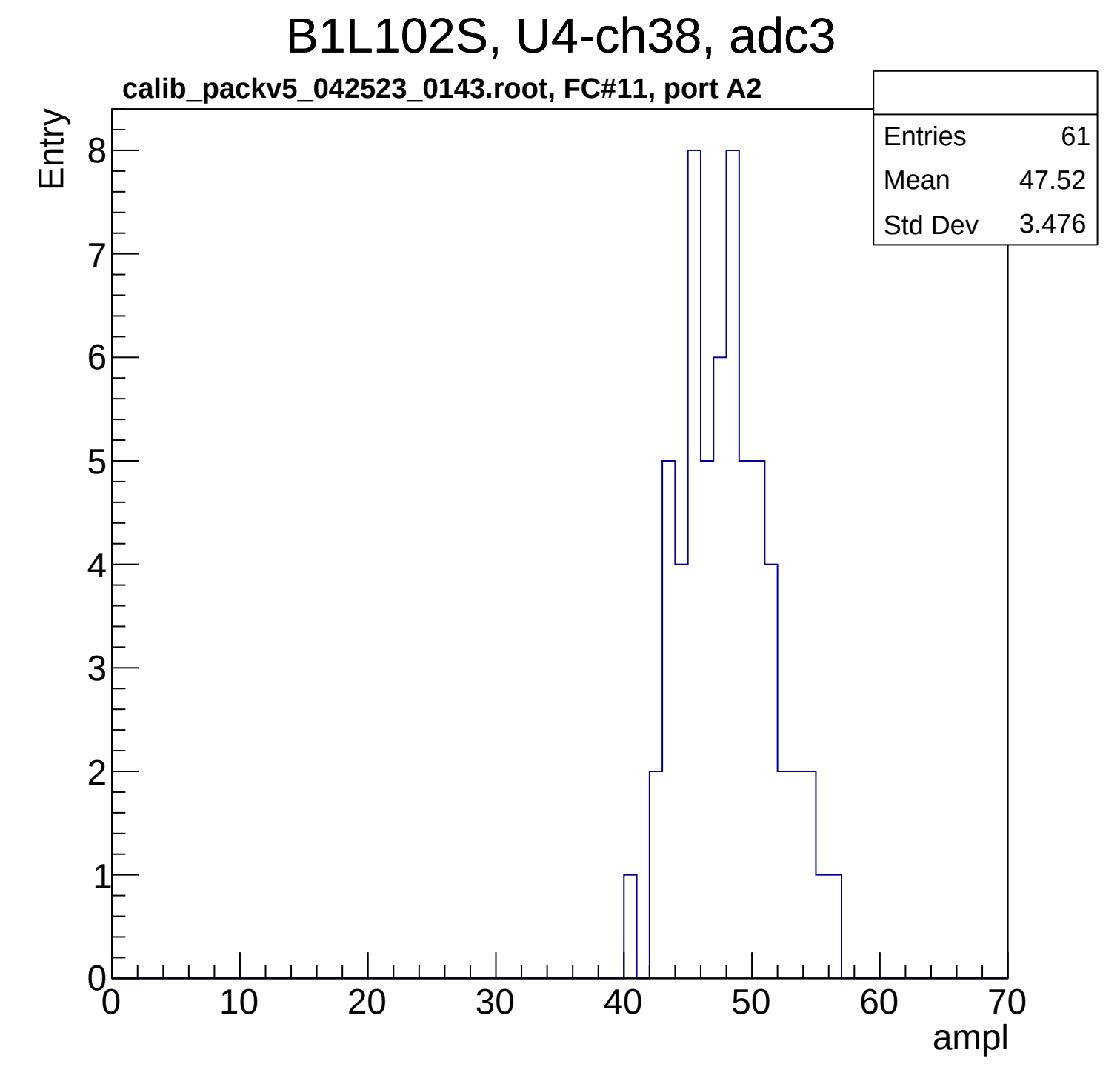
B1L102S, U4-ch38, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 47.52
Std Dev 3.476
Entry
ampl
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4
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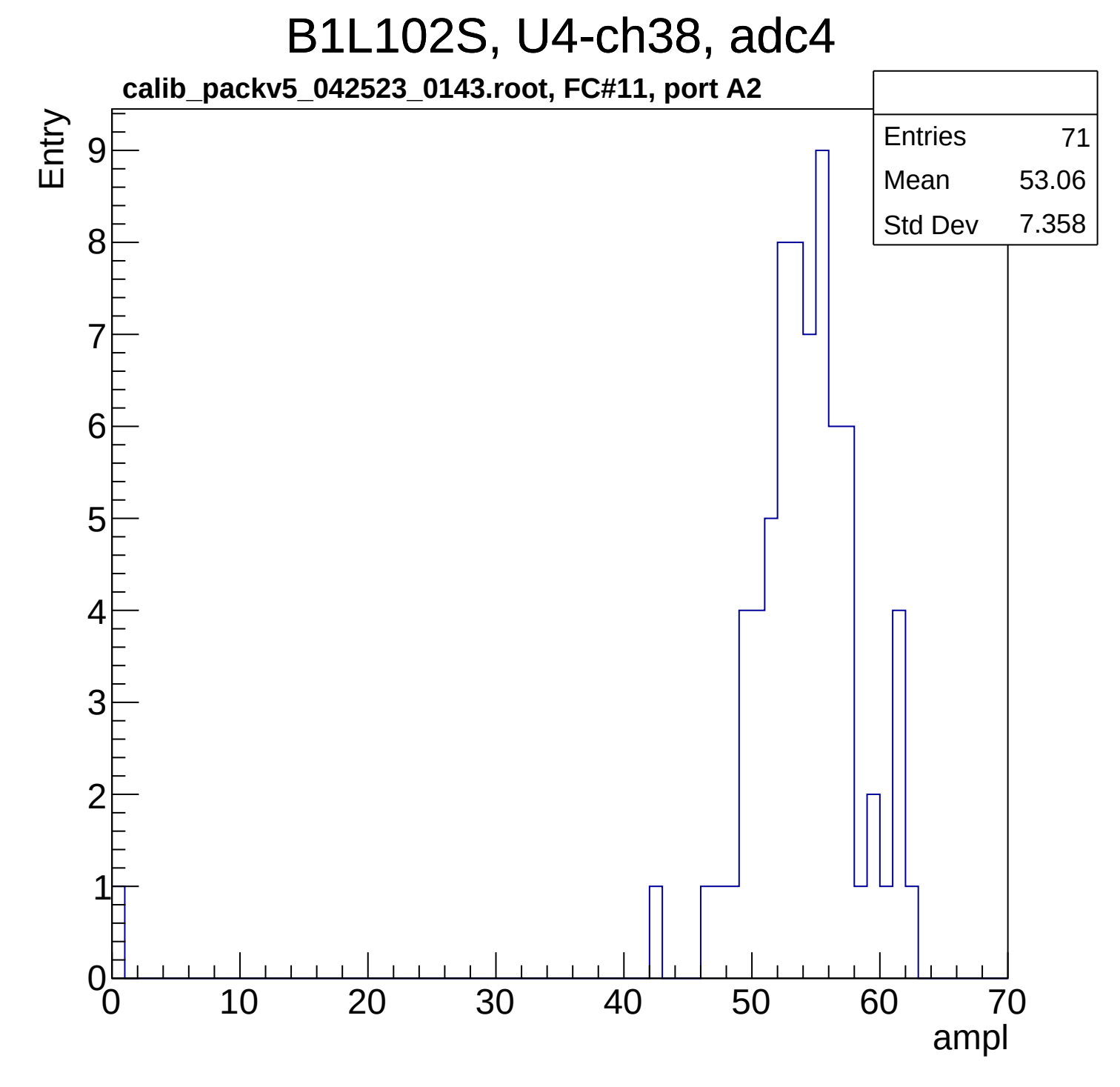
B1L102S, U4-ch38, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 53.06
Std Dev 7.358
Entry
ampl
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8
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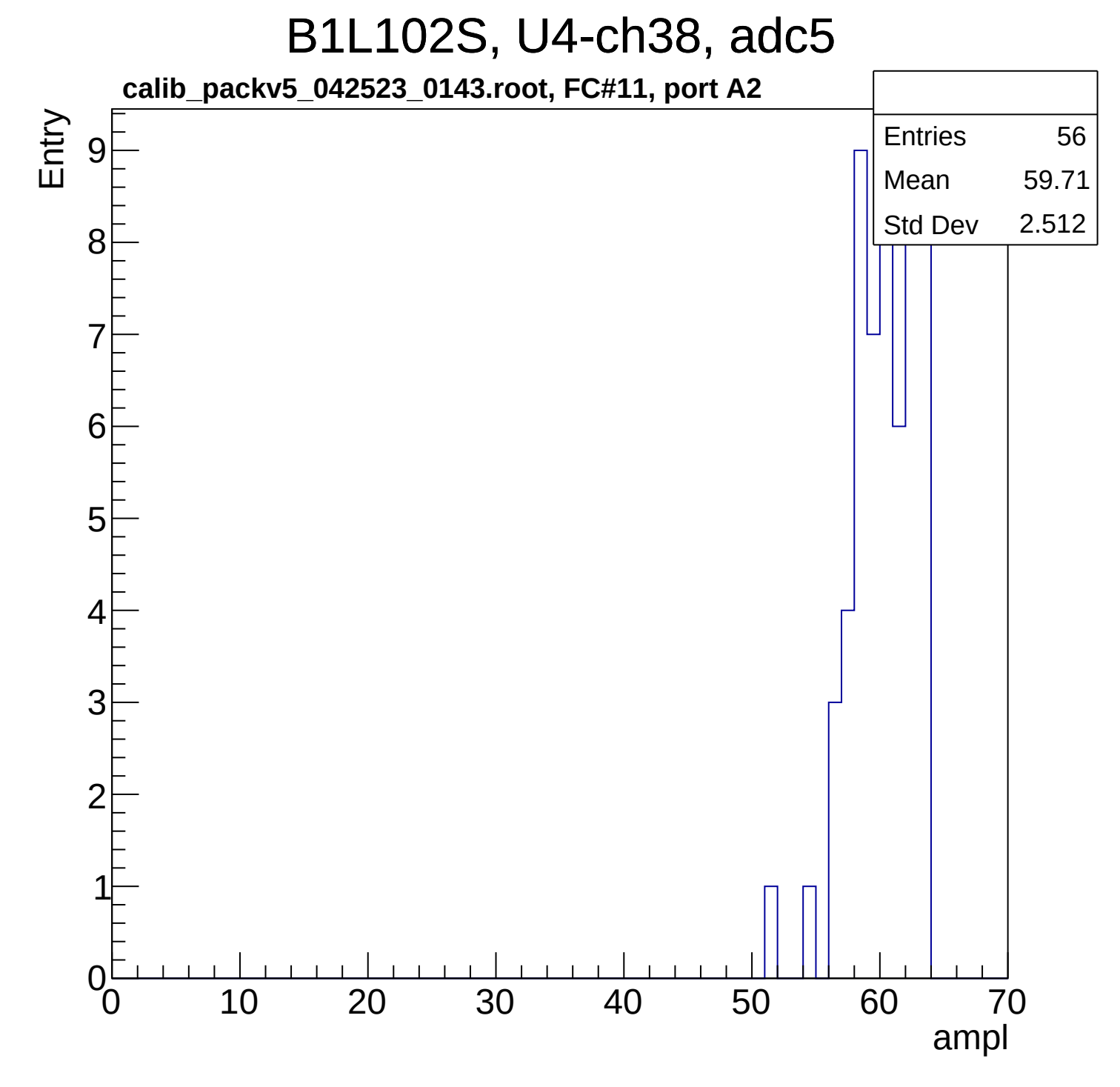
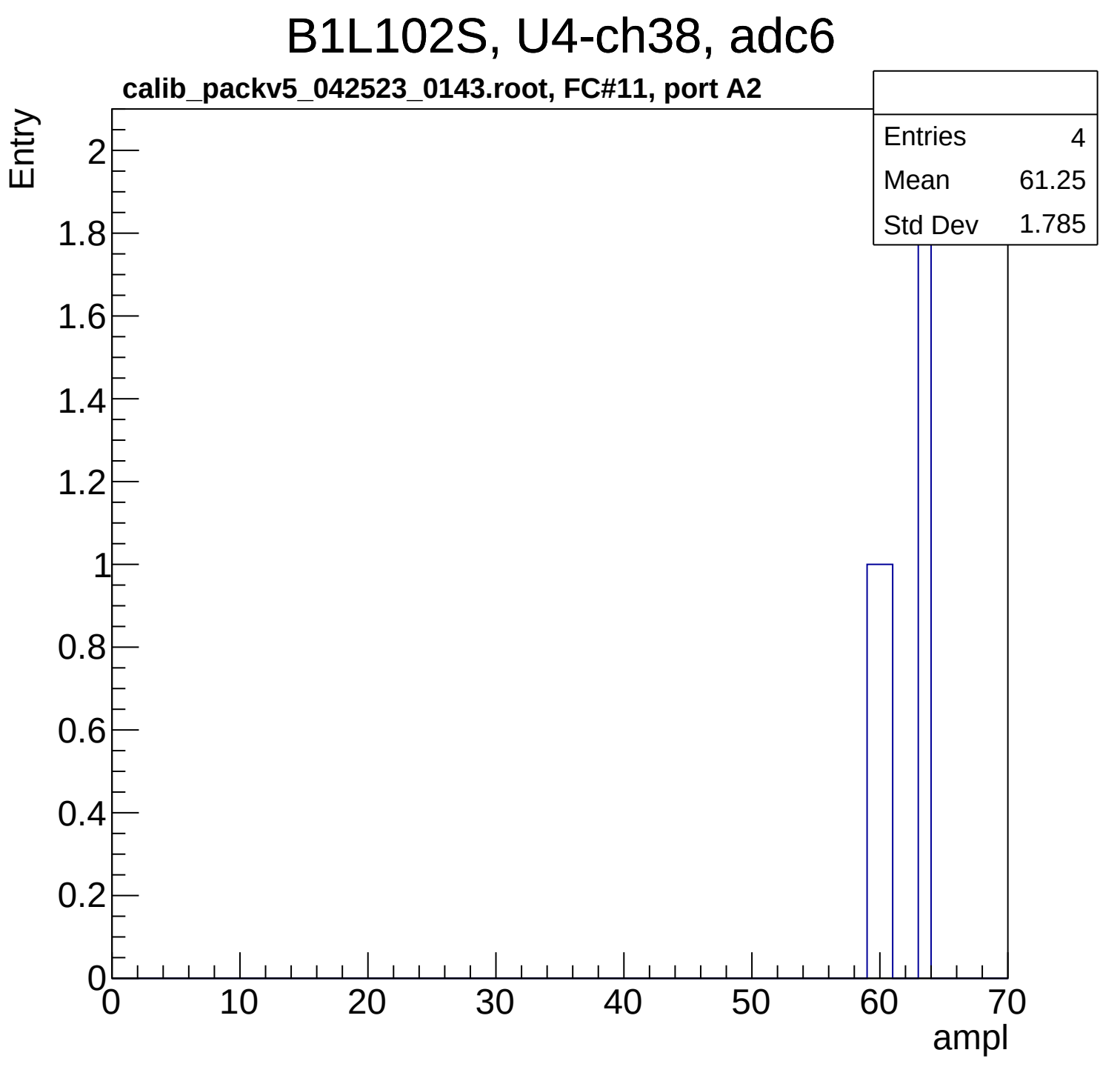
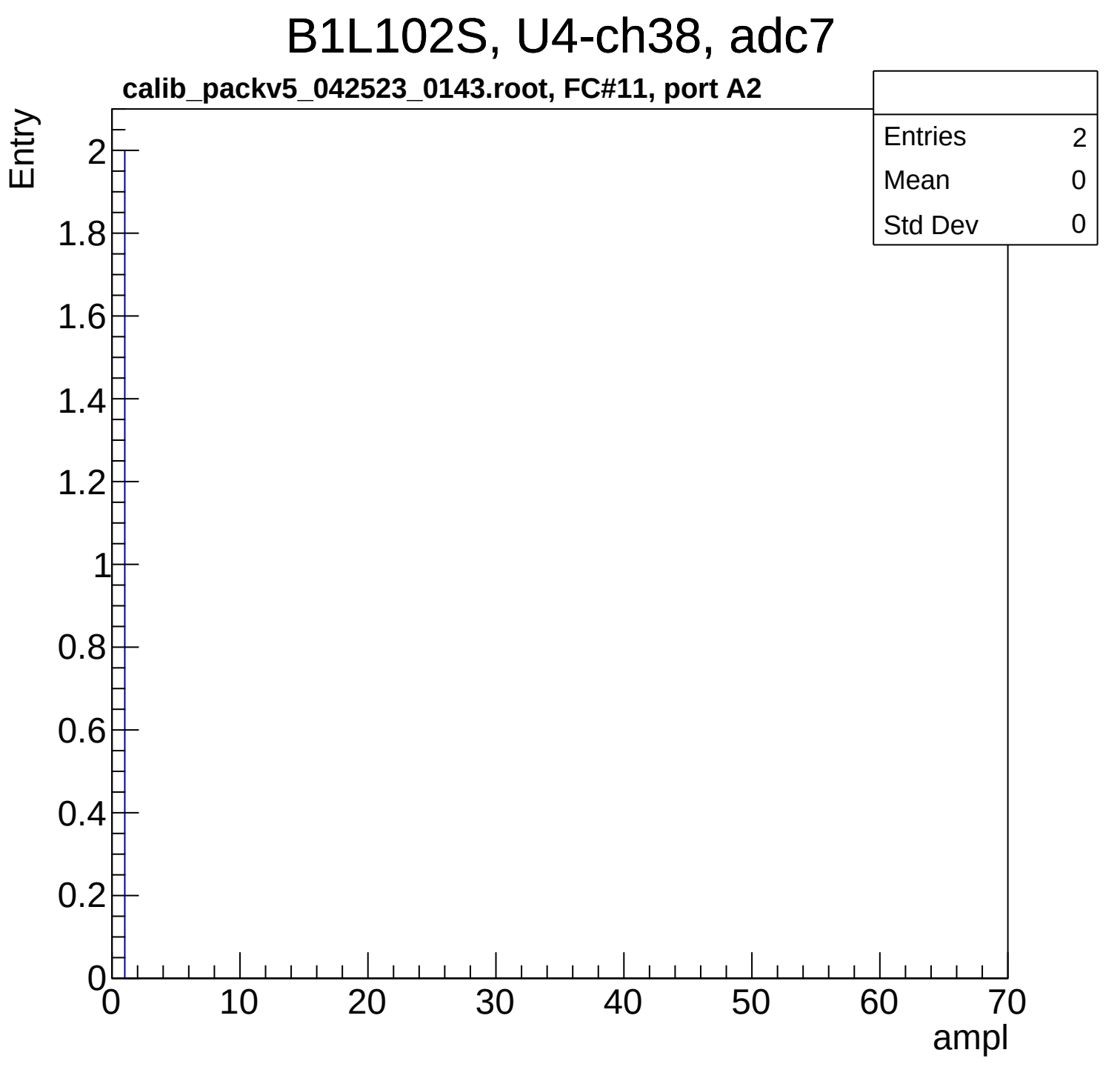
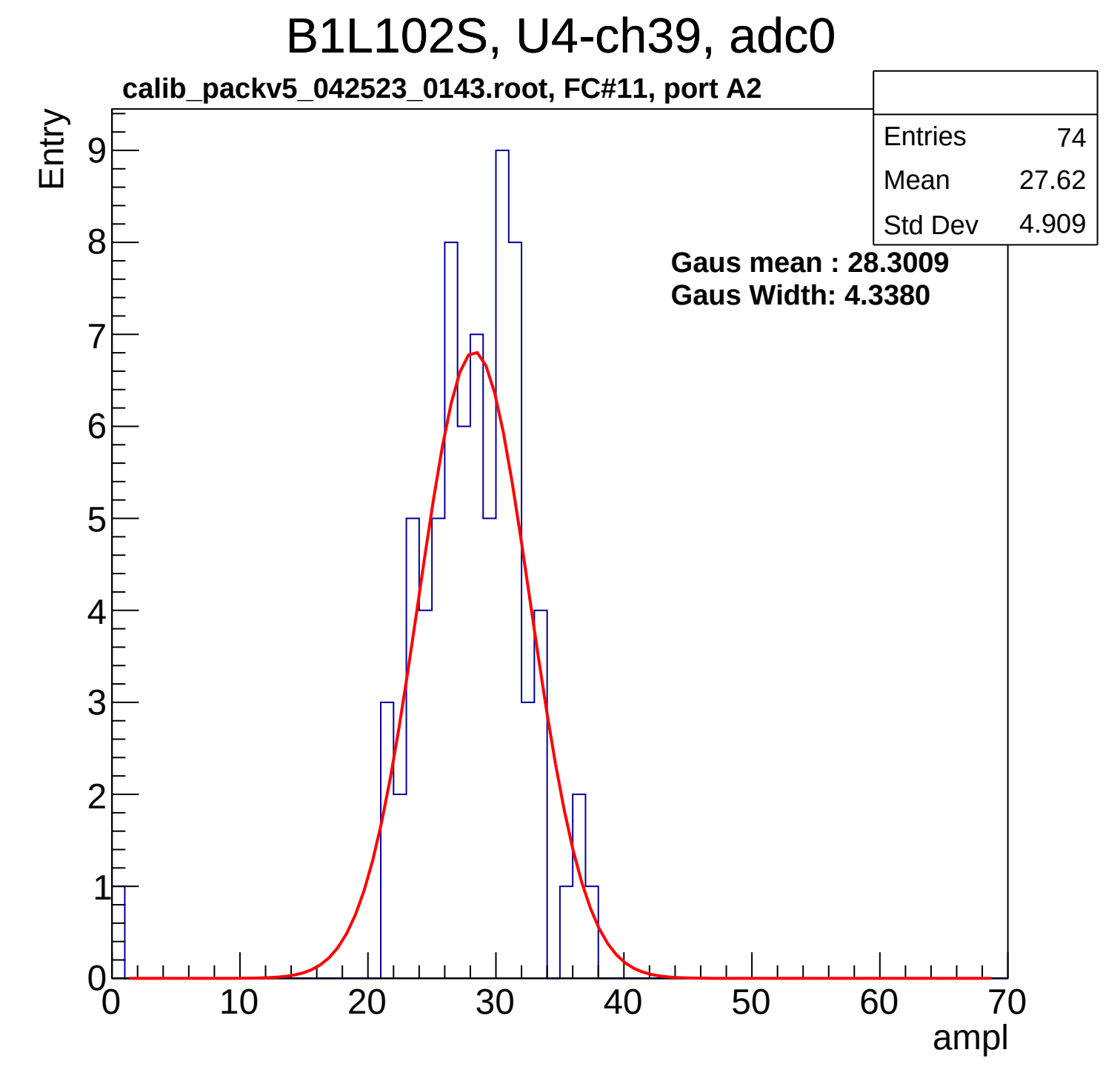
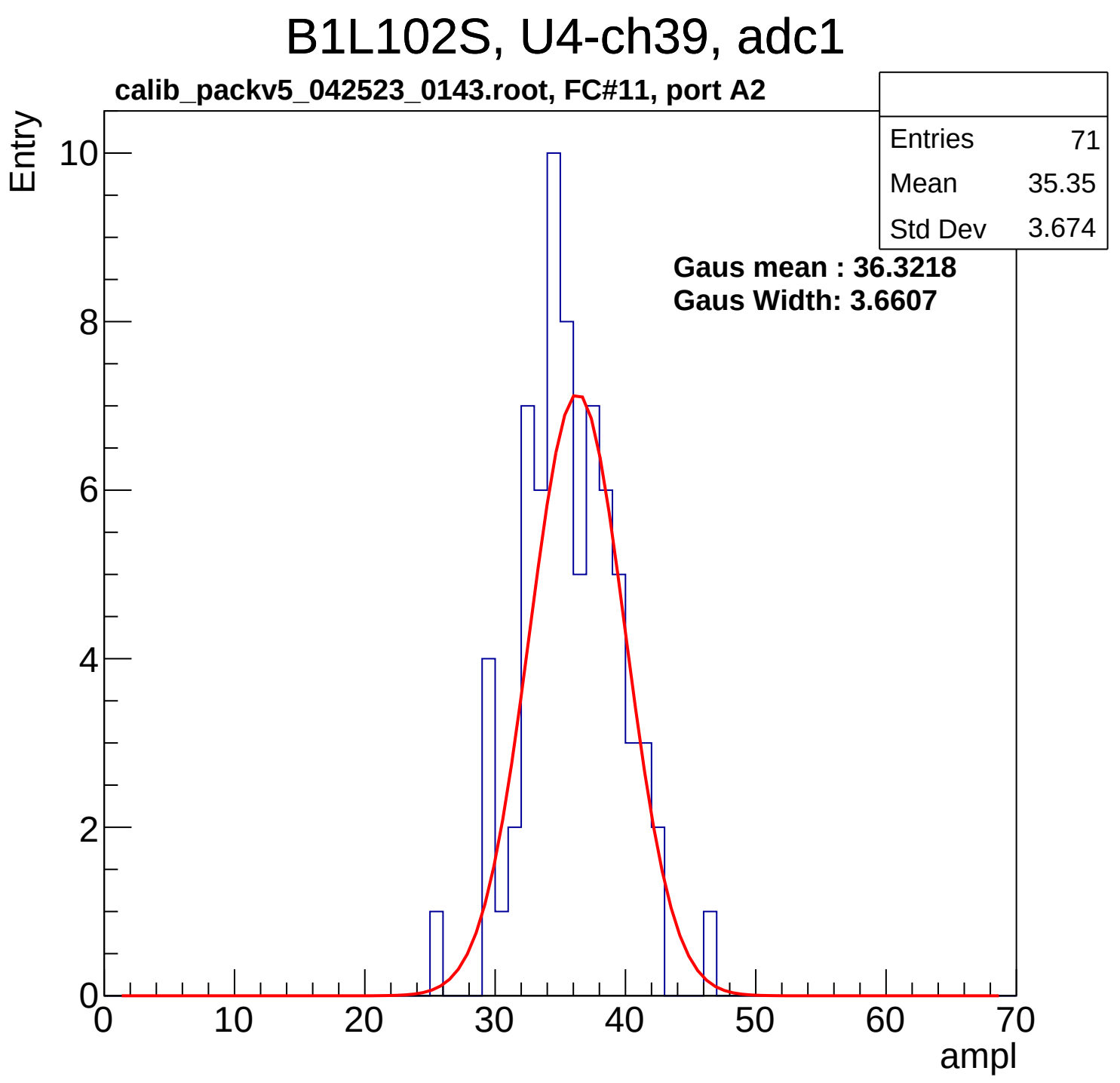
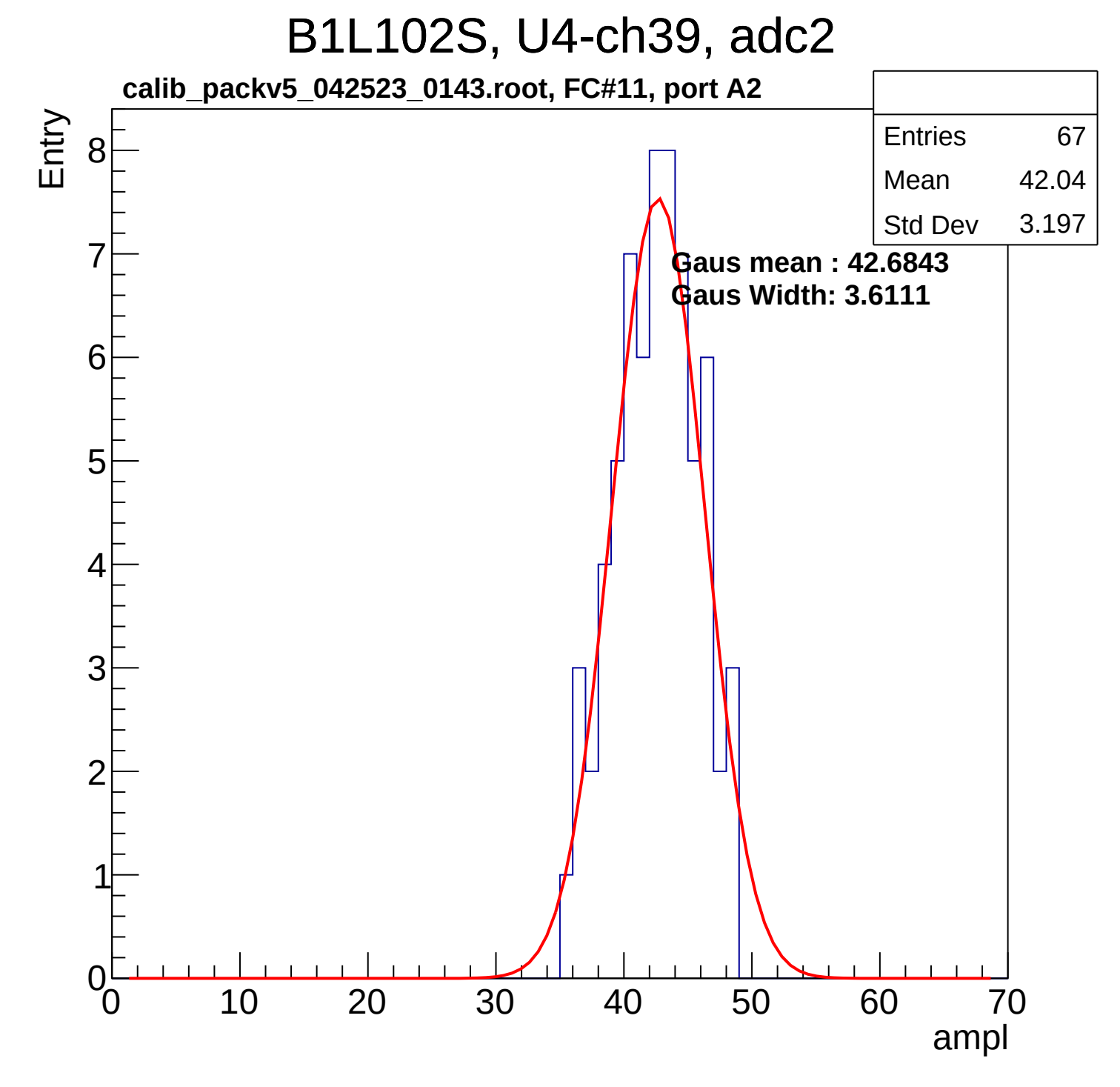

B1L102S, U4-ch38, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 59.71
Std Dev 2.512
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

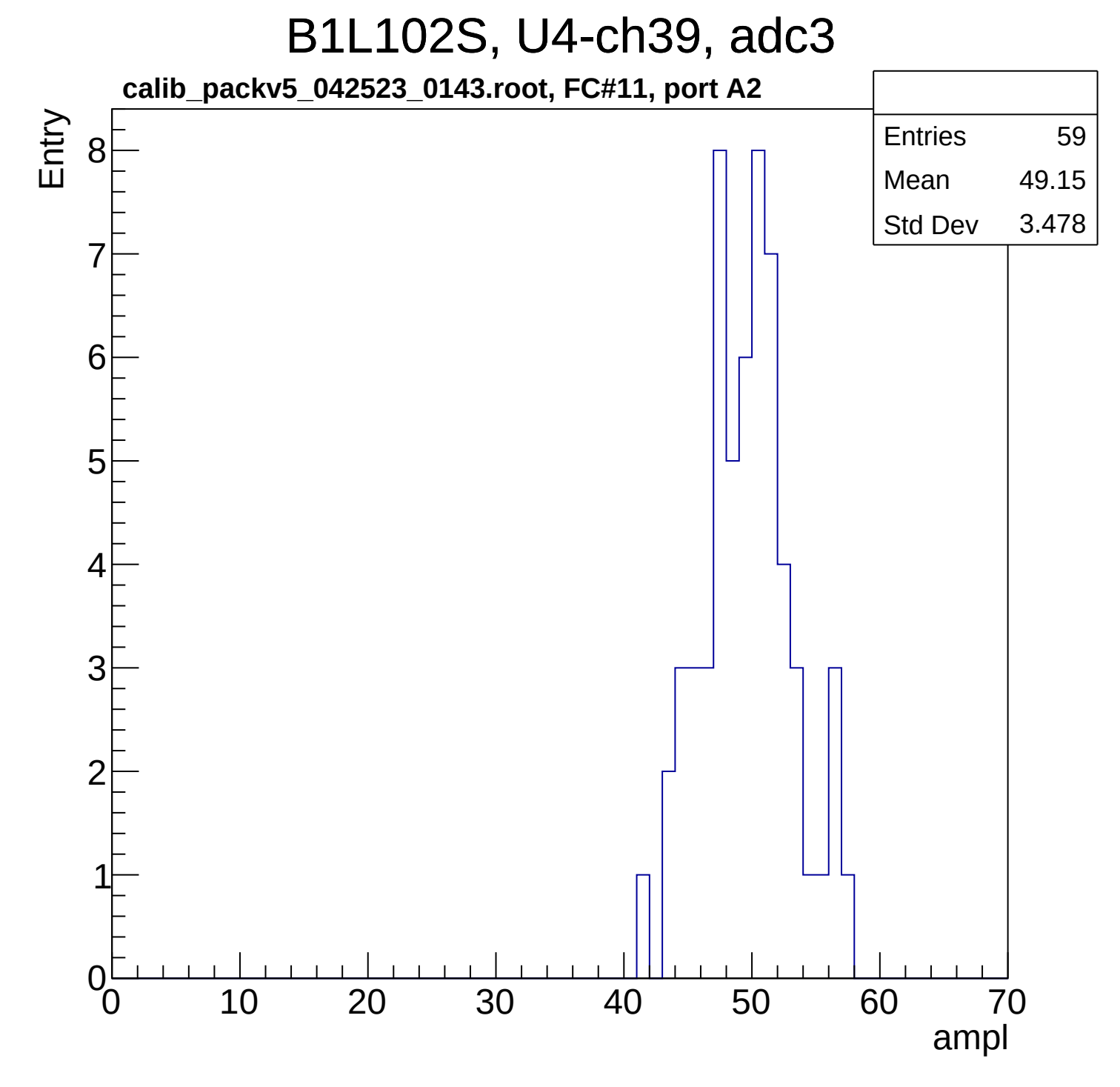

B1L102S, U4-ch38, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 4
Mean 61.25
Std Dev 1.785
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

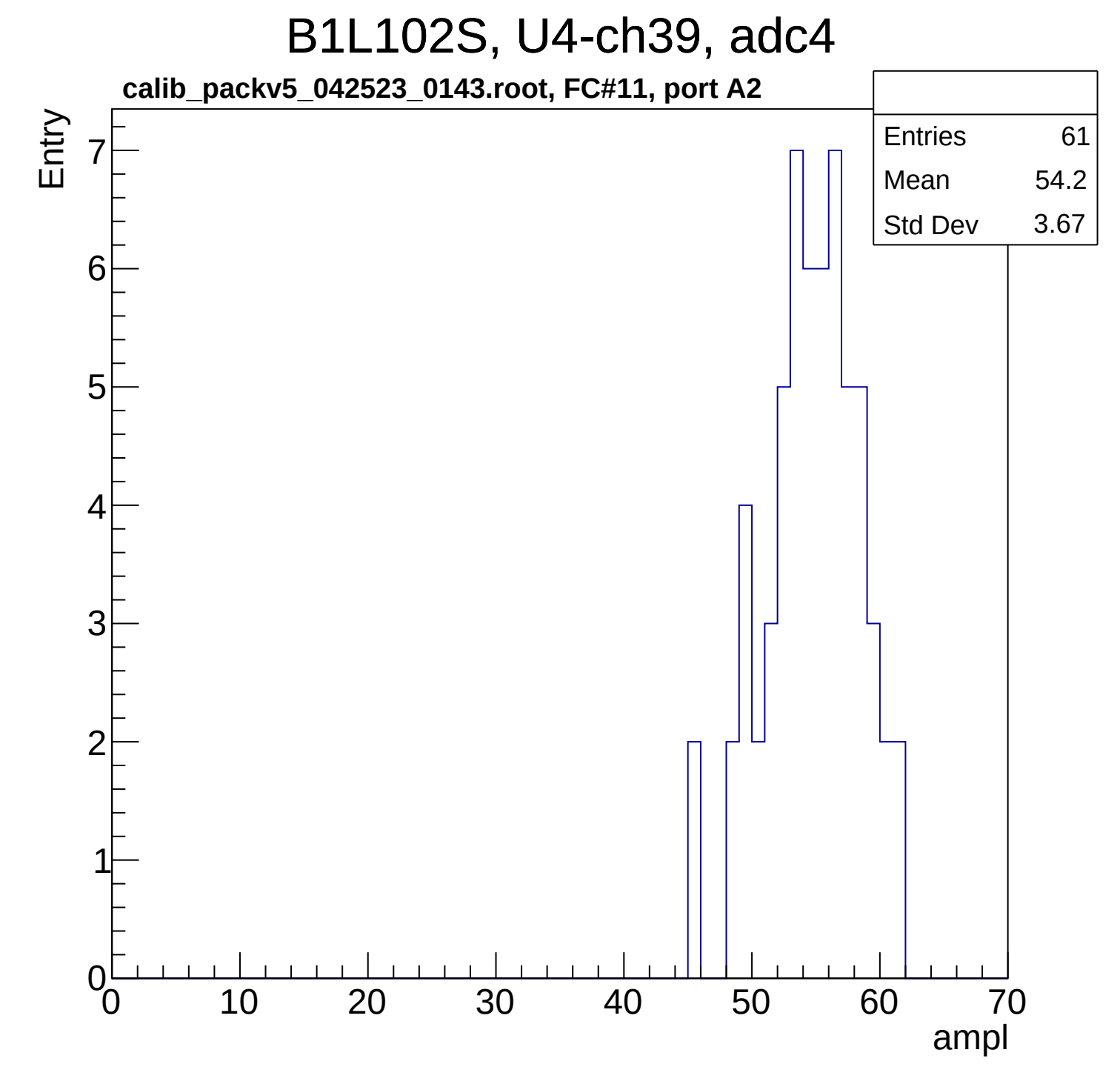

B1L102S, U4-ch38, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

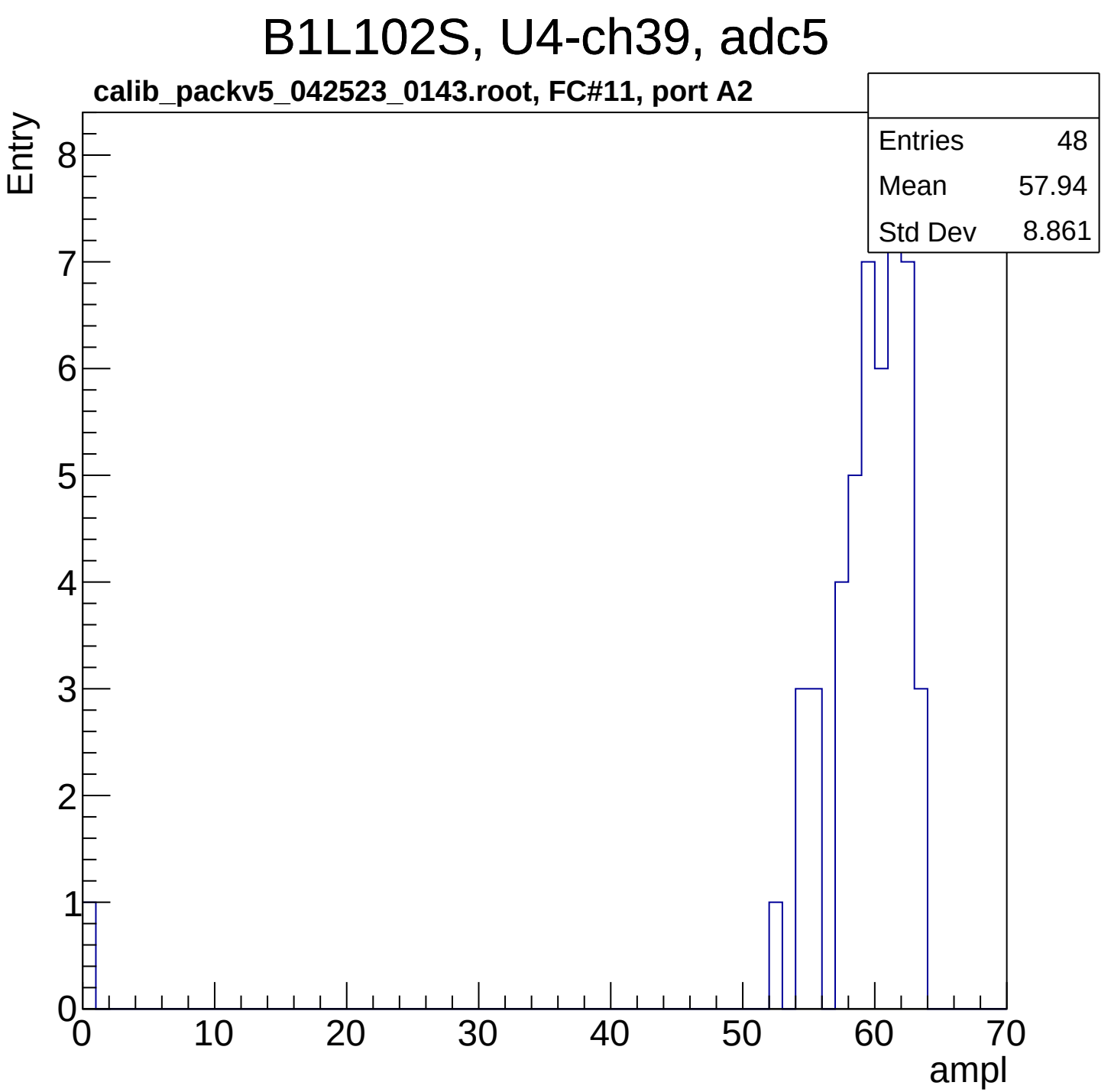

B1L102S, U4-ch39, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 27.62
Std Dev 4.909
Gaus mean : 28.3009
Gaus Width: 4.3380
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

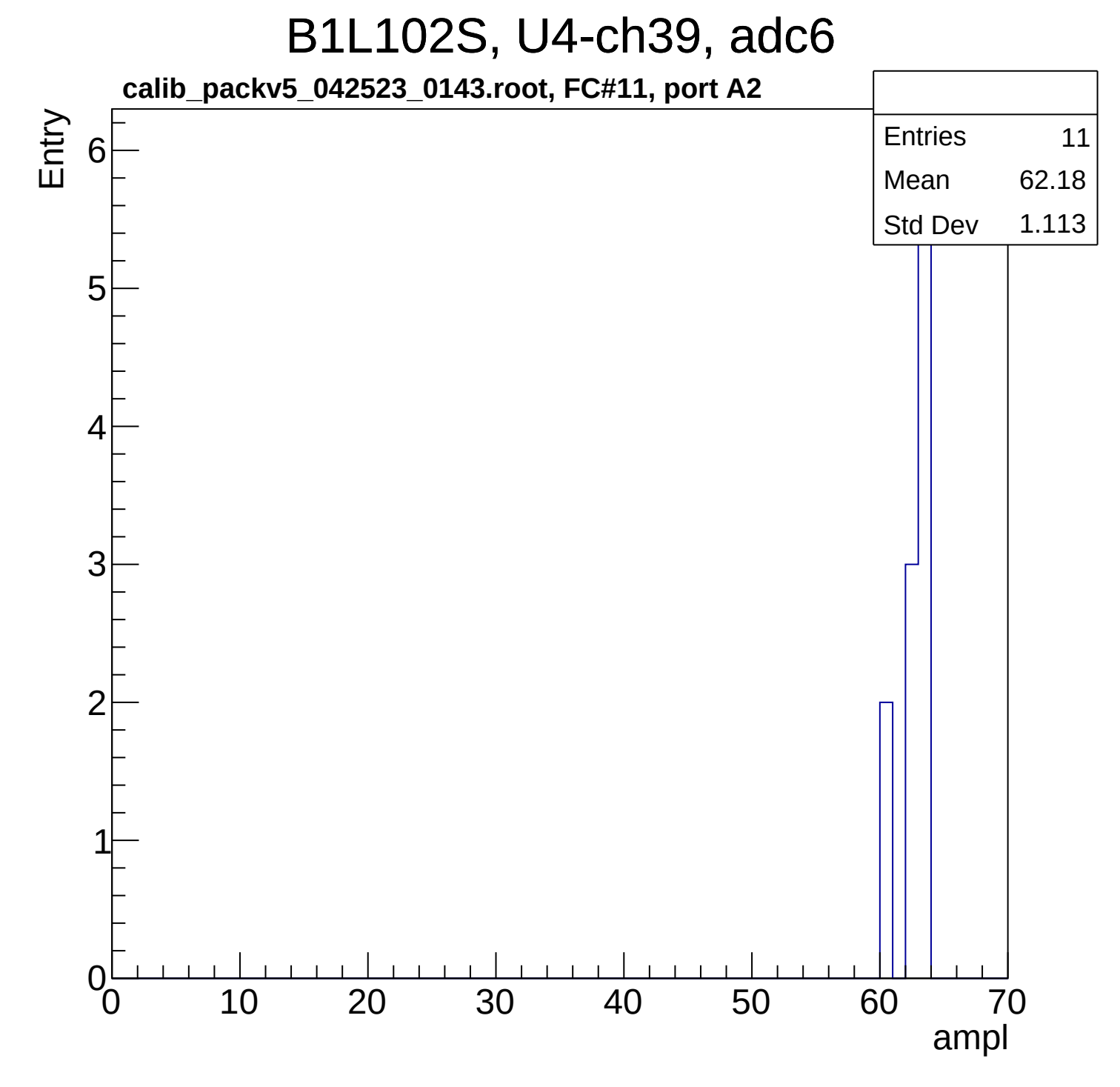

B1L102S, U4-ch39, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 35.35
Std Dev 3.674
Gaus mean : 36.3218
Gaus Width: 3.6607
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

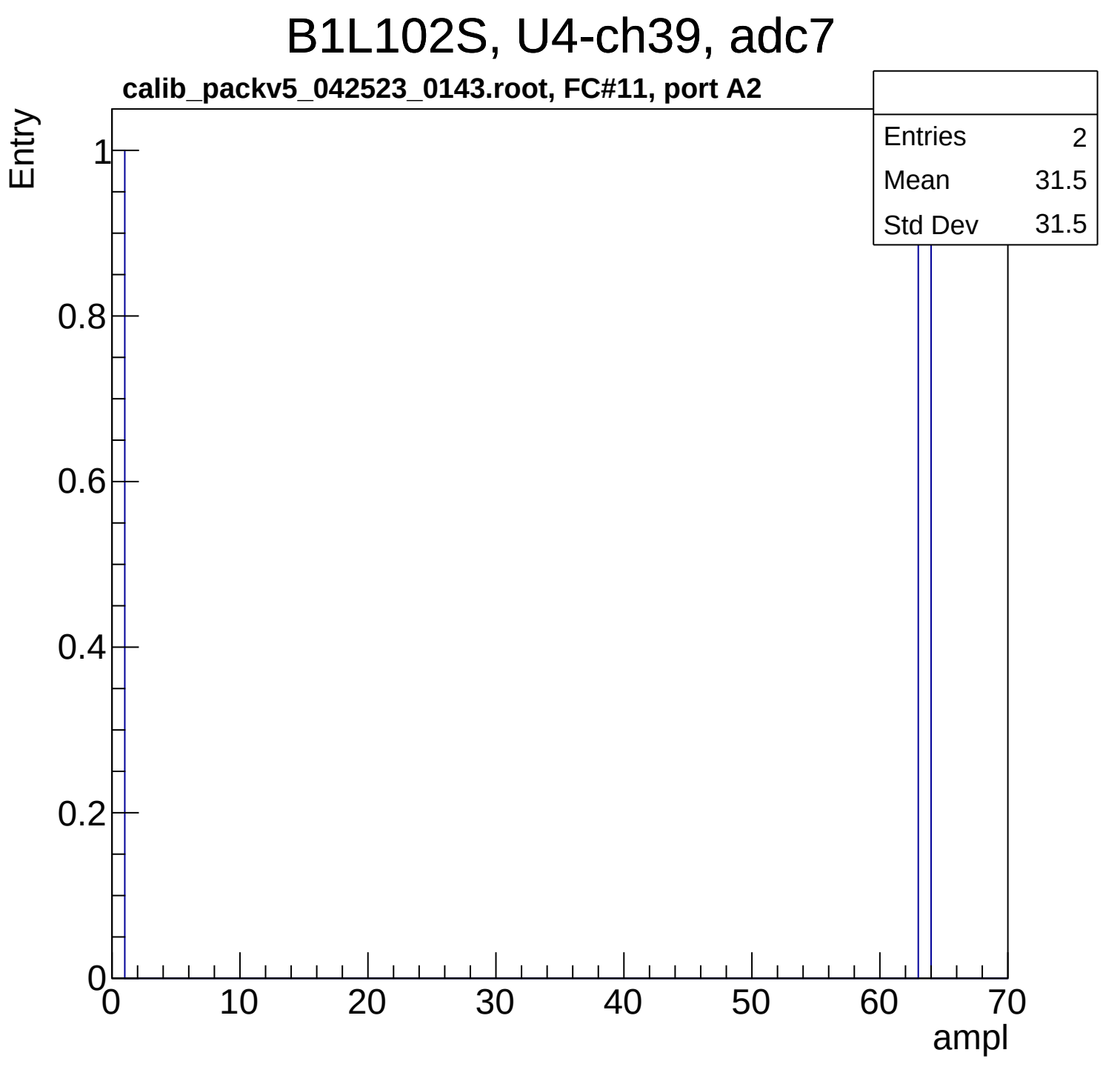

B1L102S, U4-ch39, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 42.04
Std Dev 3.197
Gaus mean : 42.6843
Gaus Width: 3.6111
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

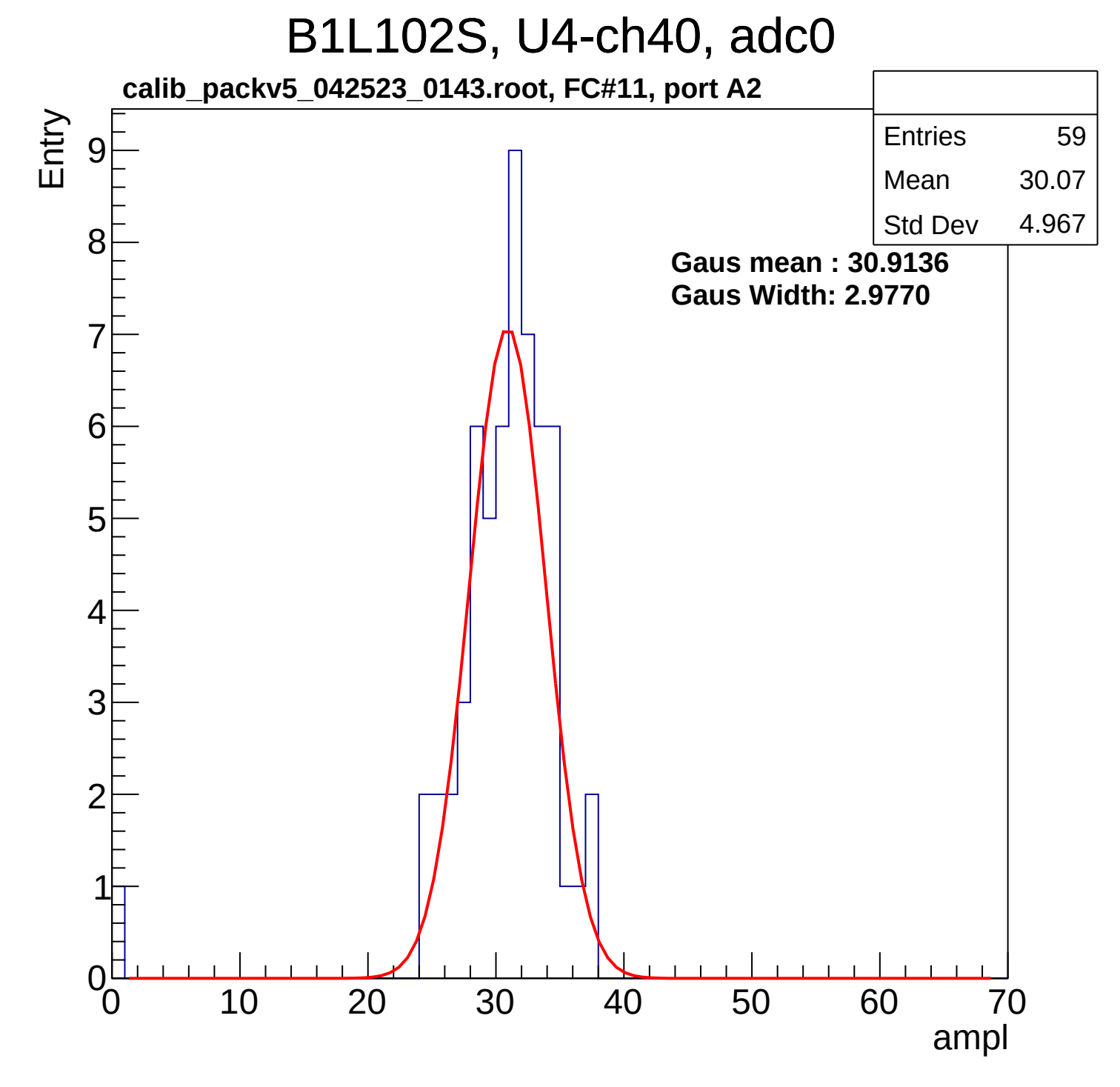

B1L102S, U4-ch39, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 49.15
Std Dev 3.478
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

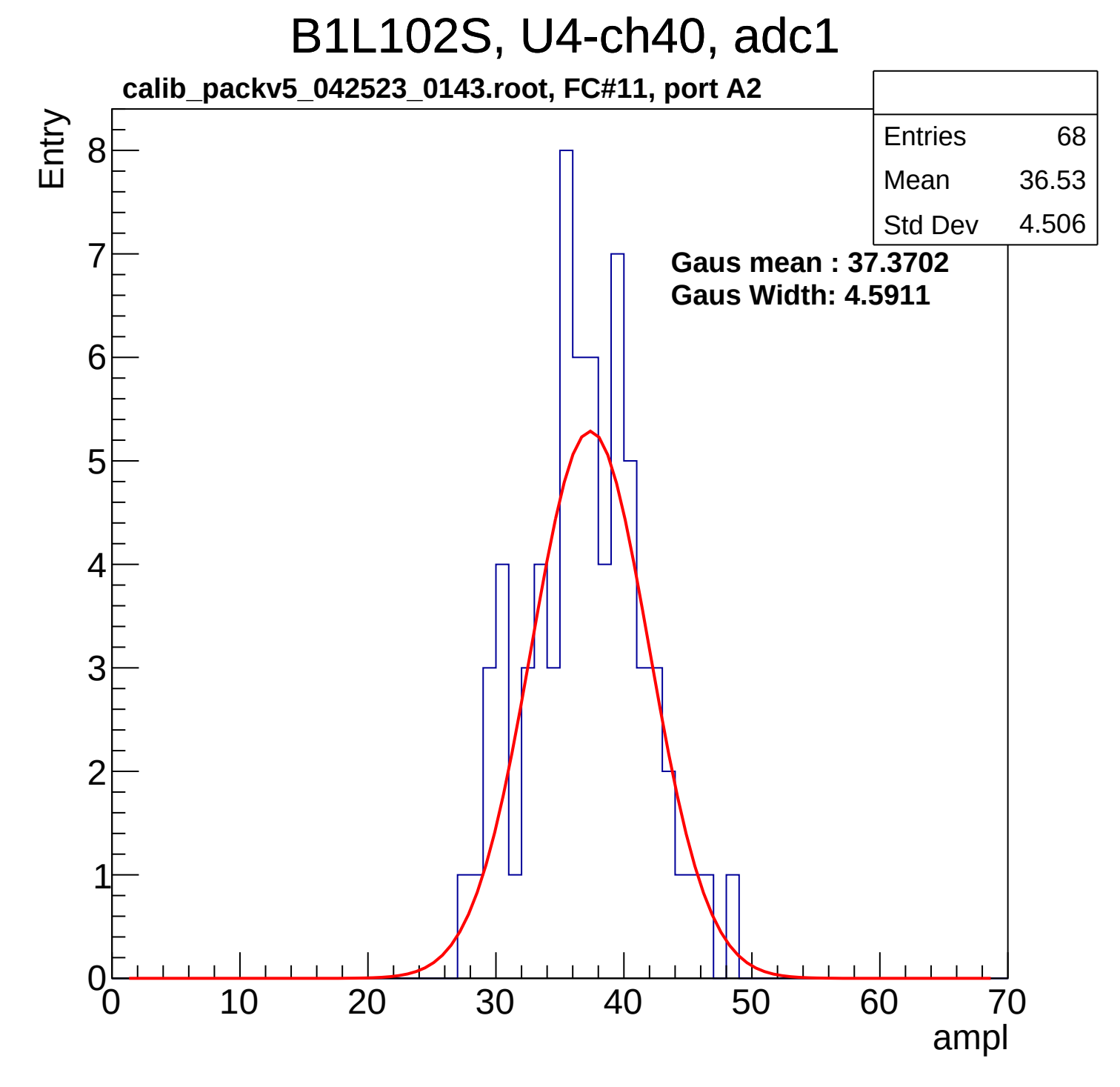

B1L102S, U4-ch39, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 54.2
Std Dev 3.67
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

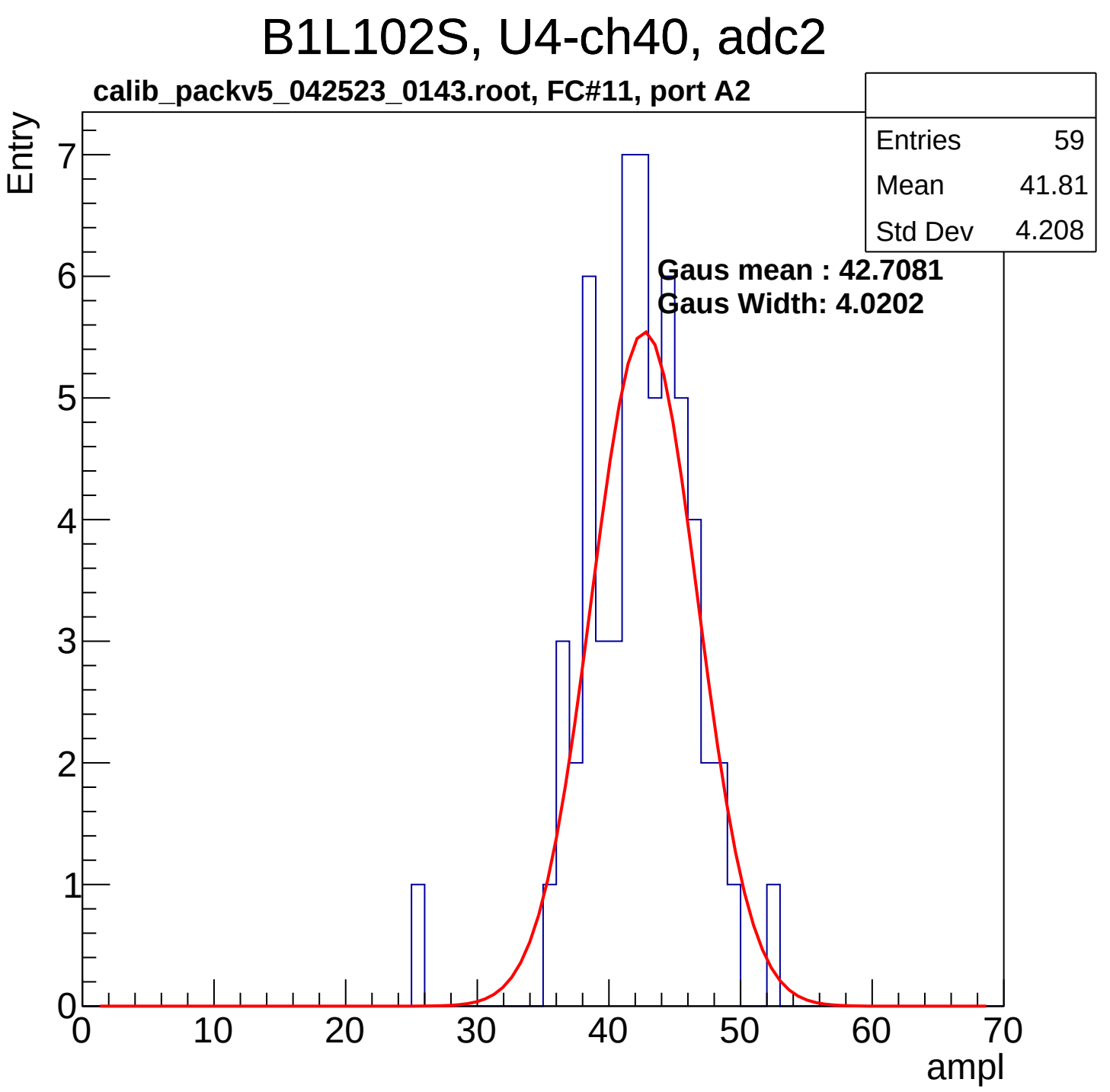

B1L102S, U4-ch39, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 48
Mean 57.94
Std Dev 8.861
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

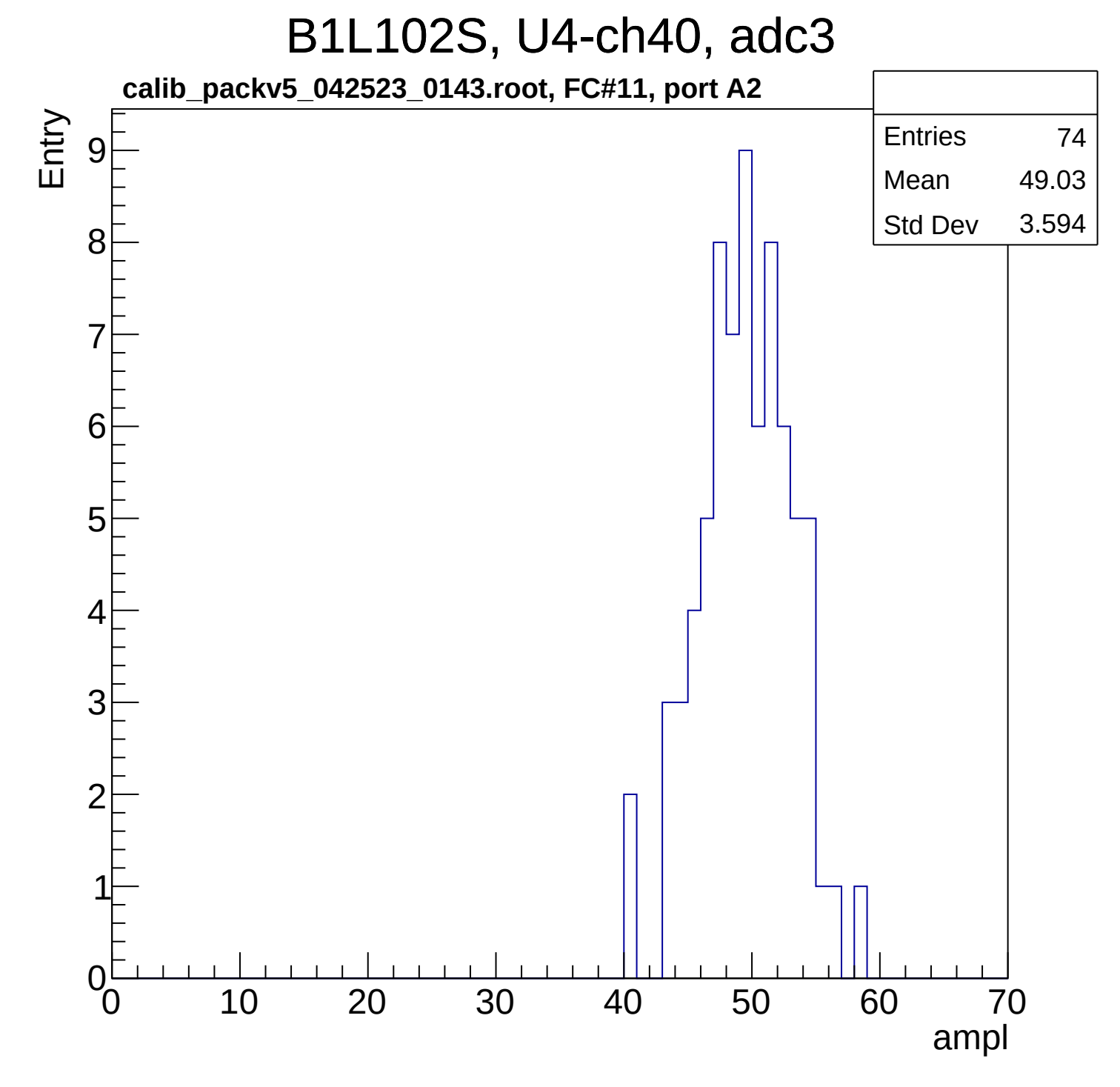

B1L102S, U4-ch39, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 11
Mean 62.18
Std Dev 1.113
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

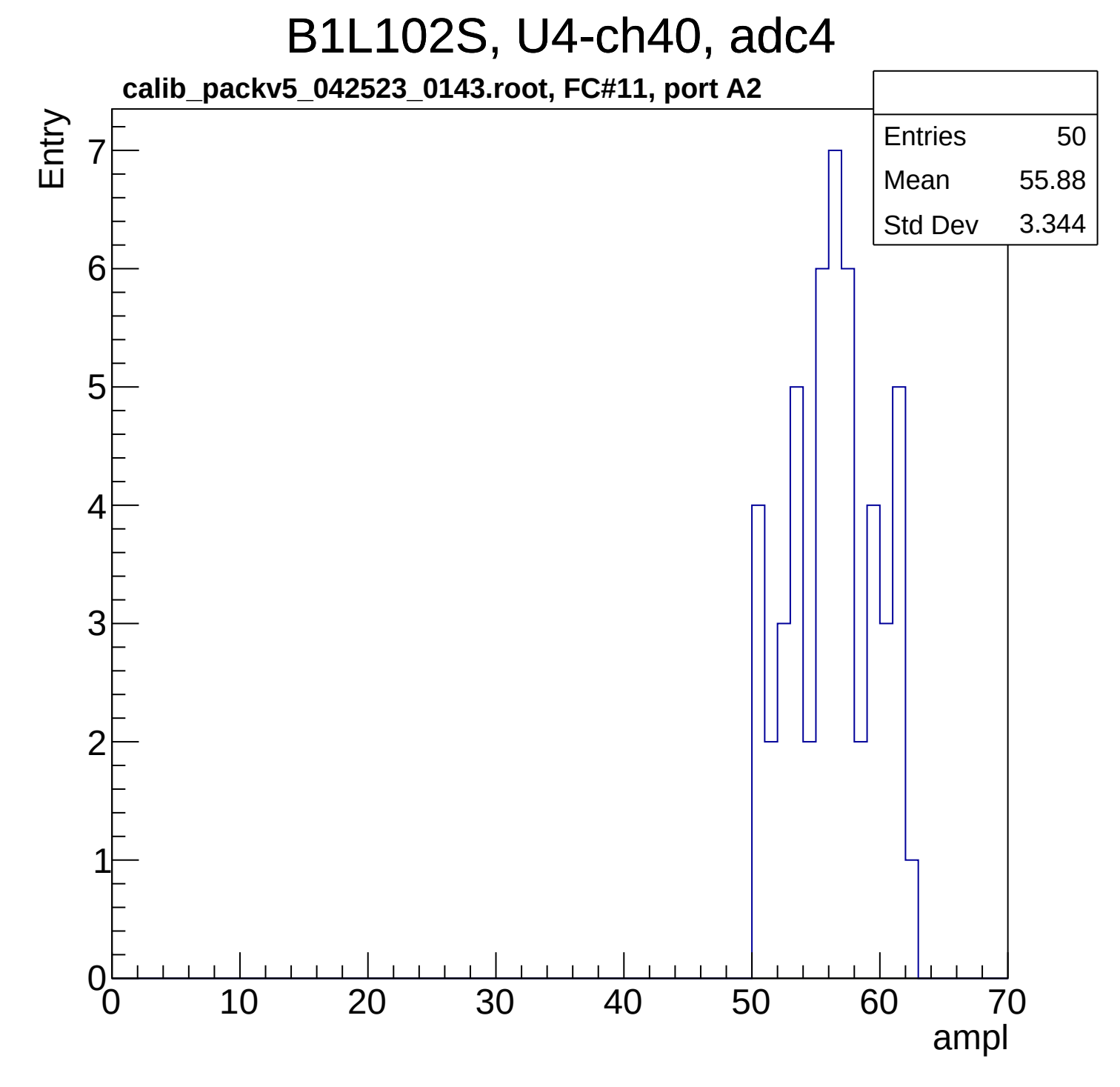

B1L102S, U4-ch39, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

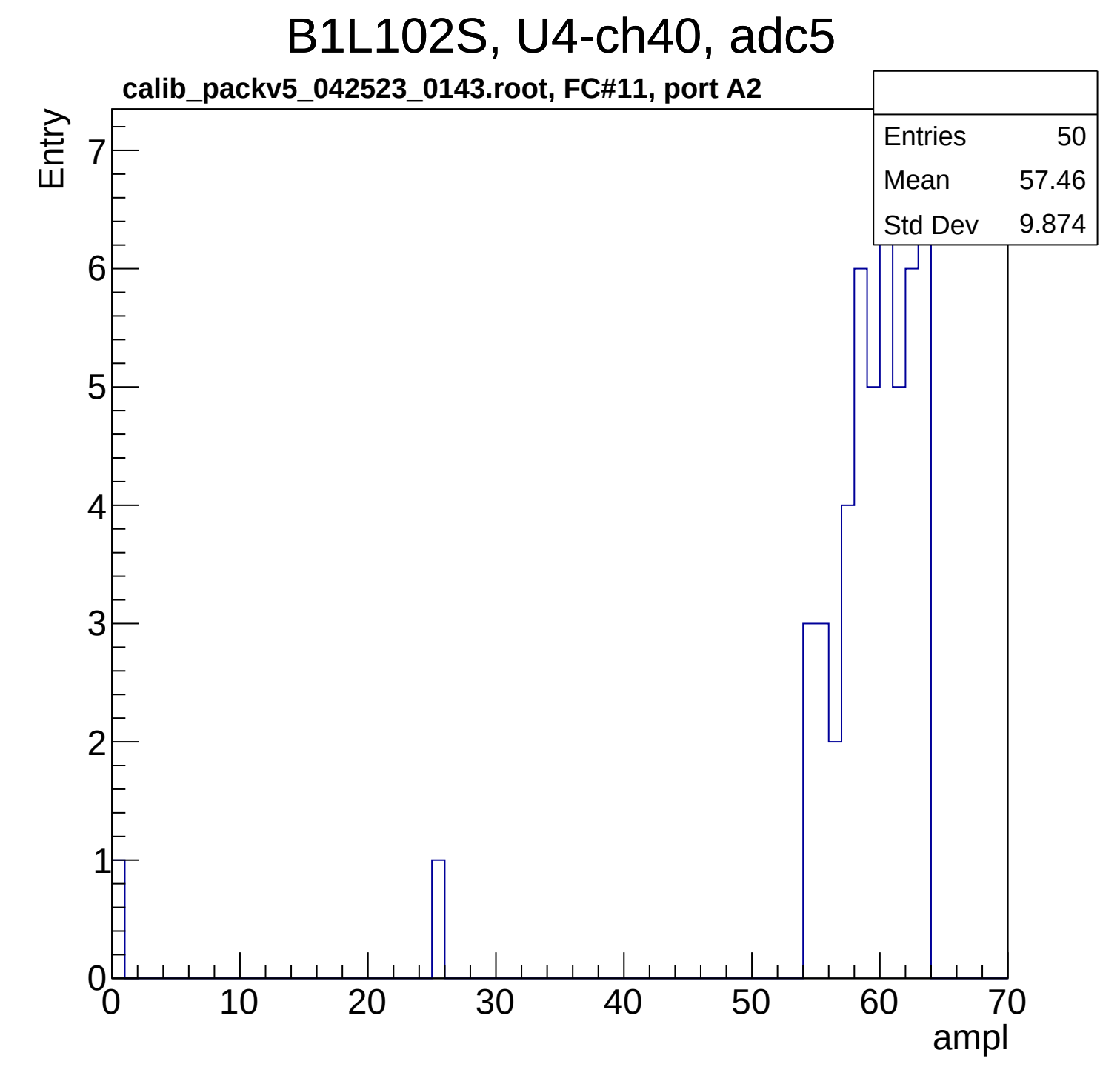

B1L102S, U4-ch40, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 30.07
Std Dev 4.967
Gaus mean : 30.9136
Gaus Width: 2.9770
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

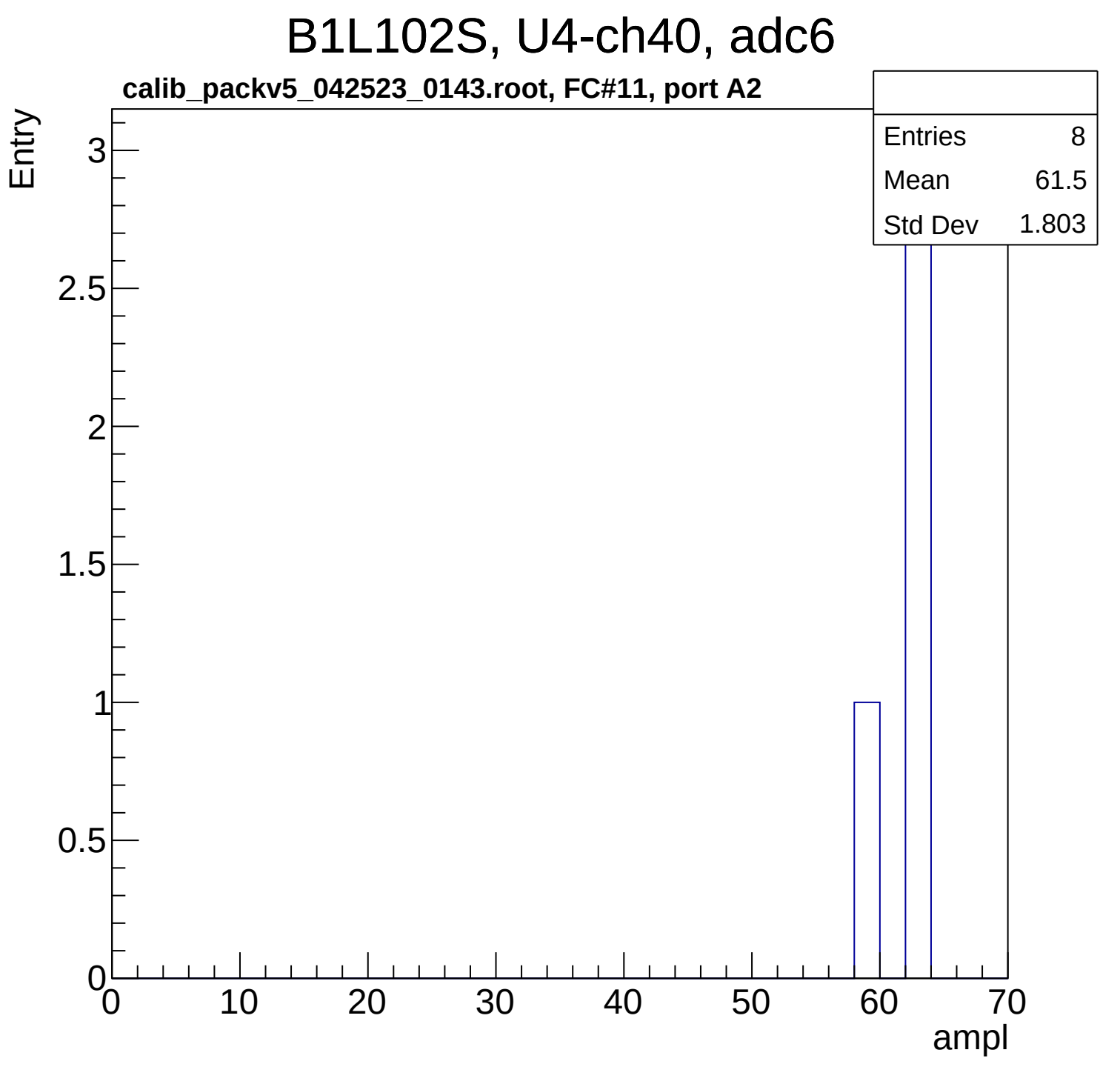

B1L102S, U4-ch40, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 36.53
Std Dev 4.506
Gaus mean : 37.3702
Gaus Width: 4.5911
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

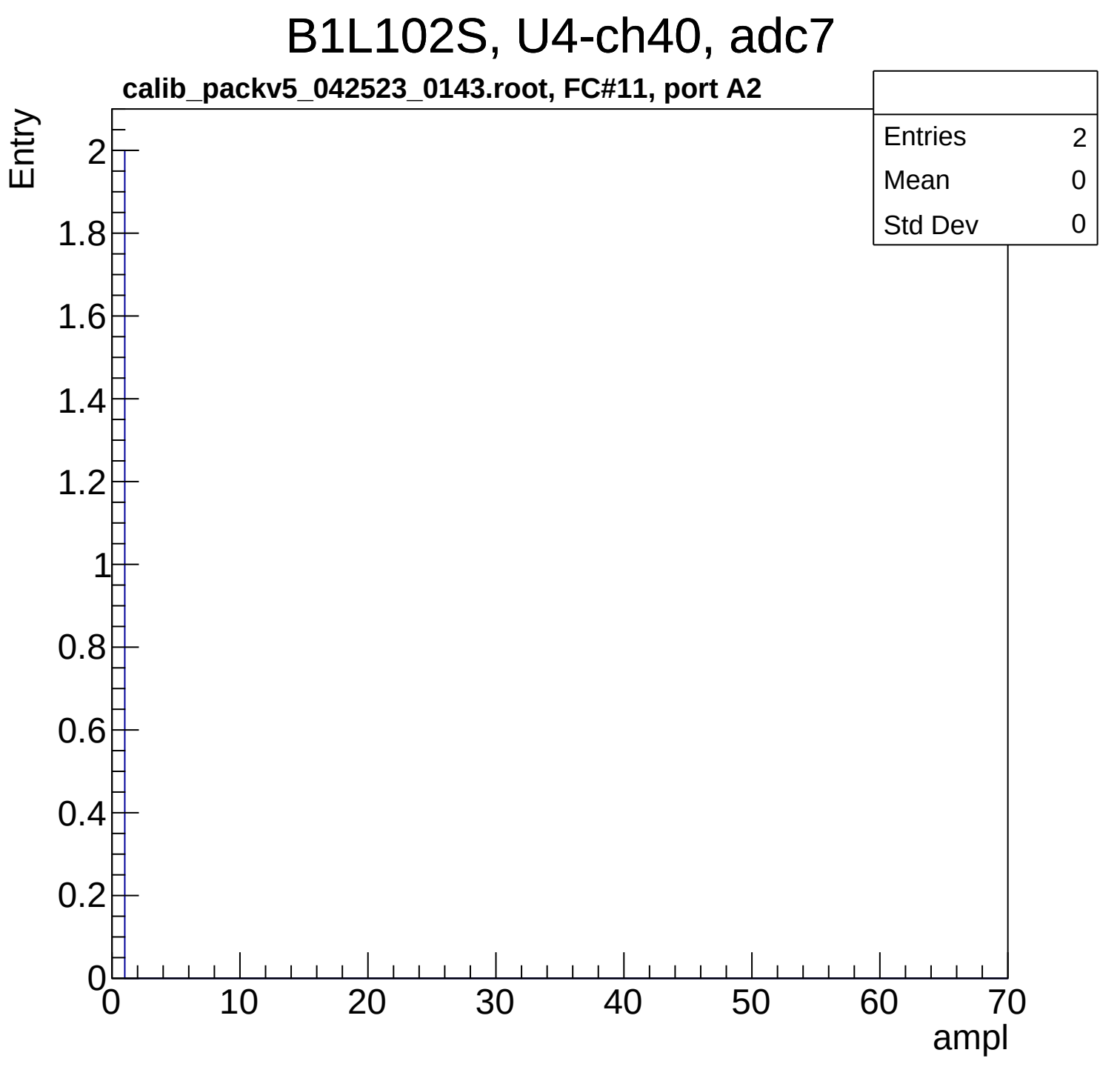

B1L102S, U4-ch40, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 41.81
Std Dev 4.208
Gaus mean : 42.7081
Gaus Width: 4.0202
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch40, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 49.03
Std Dev 3.594
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch40, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 50
Mean 55.88
Std Dev 3.344
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch40, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 50
Mean 57.46
Std Dev 9.874
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch40, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 8
Mean 61.5
Std Dev 1.803
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U4-ch40, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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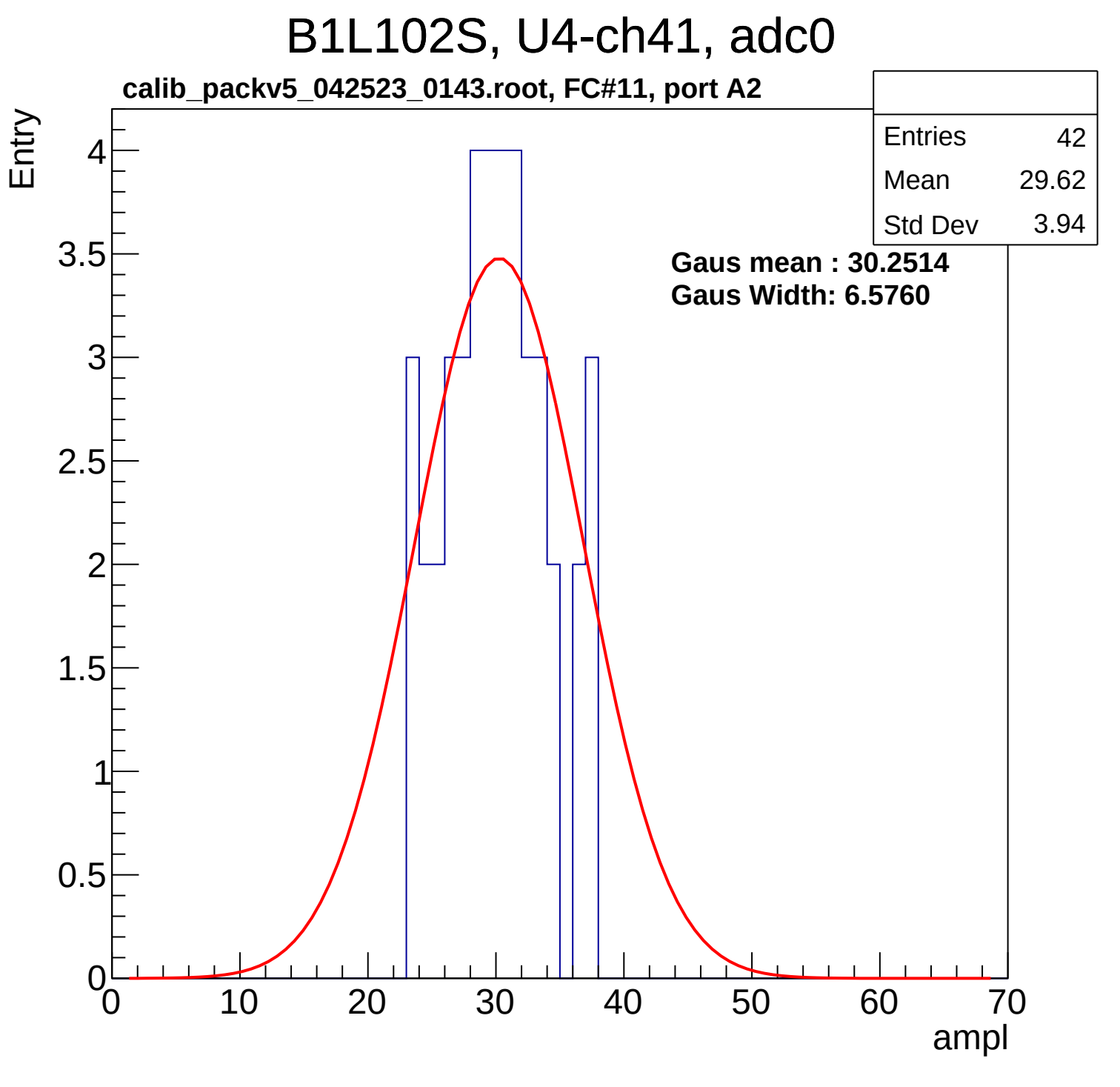
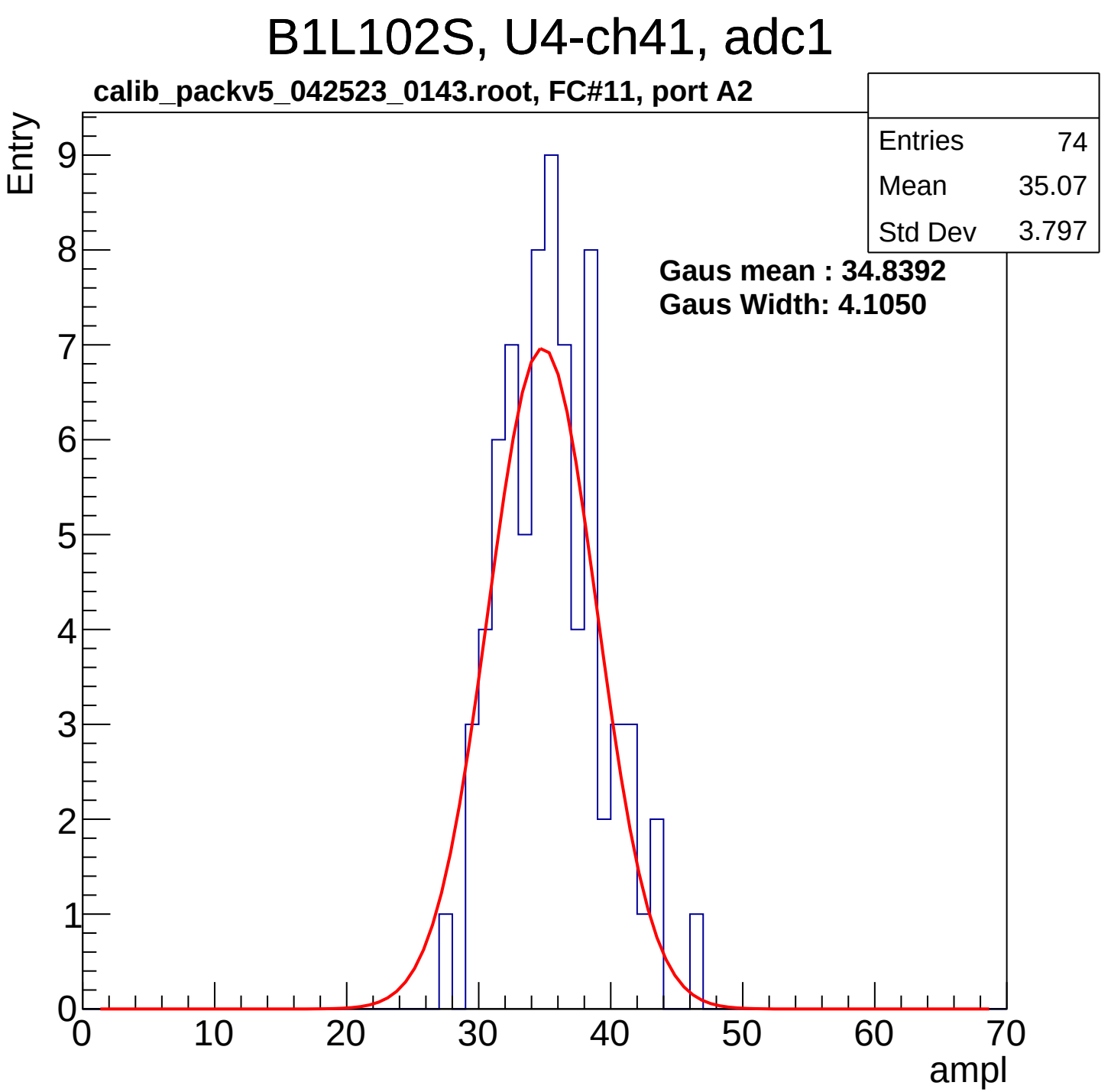
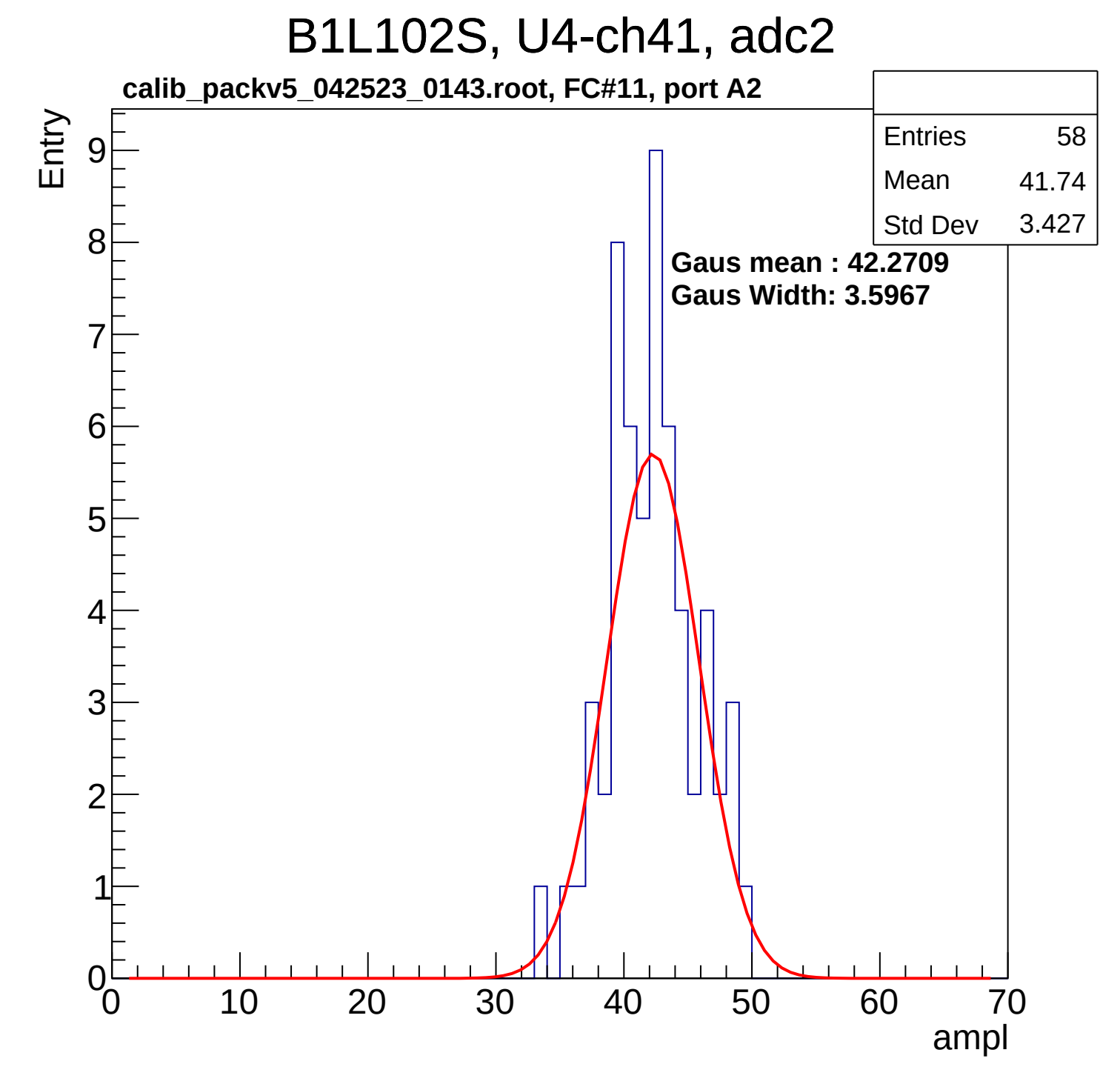

B1L102S, U4-ch41, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 42
Mean 29.62
Std Dev 3.94
Gaus mean : 30.2514
Gaus Width: 6.5760
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U4-ch41, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 35.07
Std Dev 3.797
Gaus mean : 34.8392
Gaus Width: 4.1050
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch41, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 41.74
Std Dev 3.427
Gaus mean : 42.2709
Gaus Width: 3.5967
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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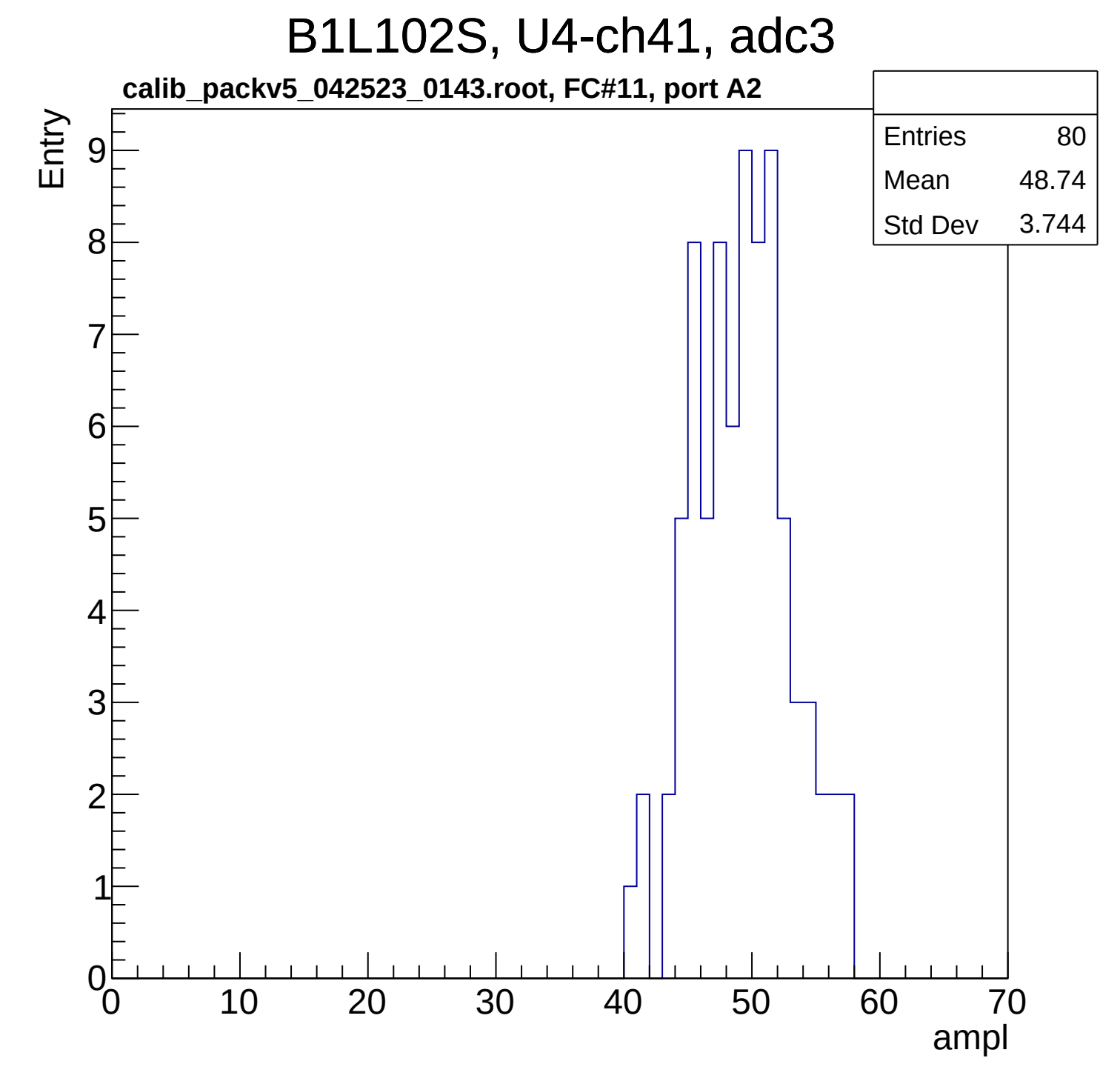
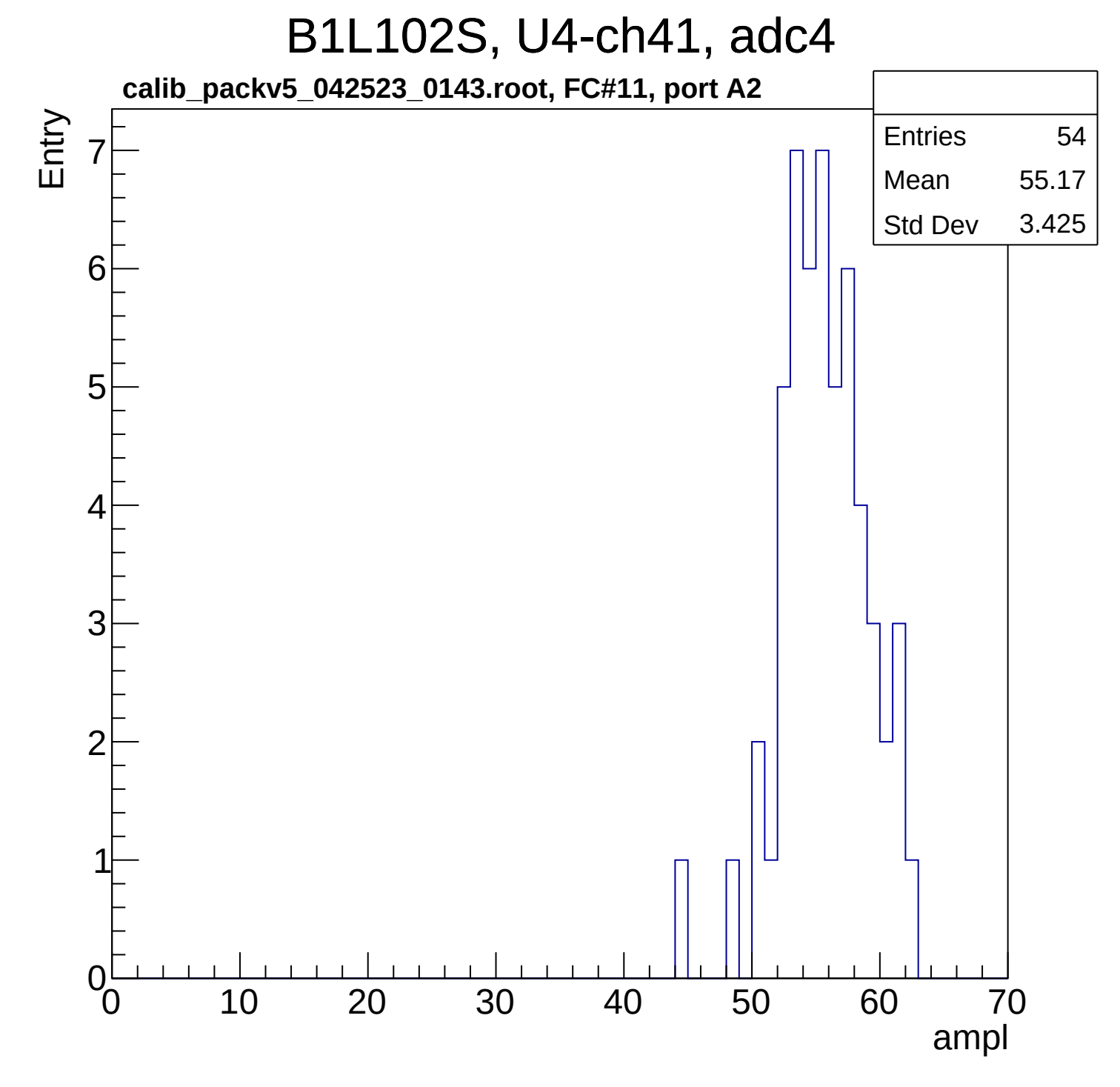
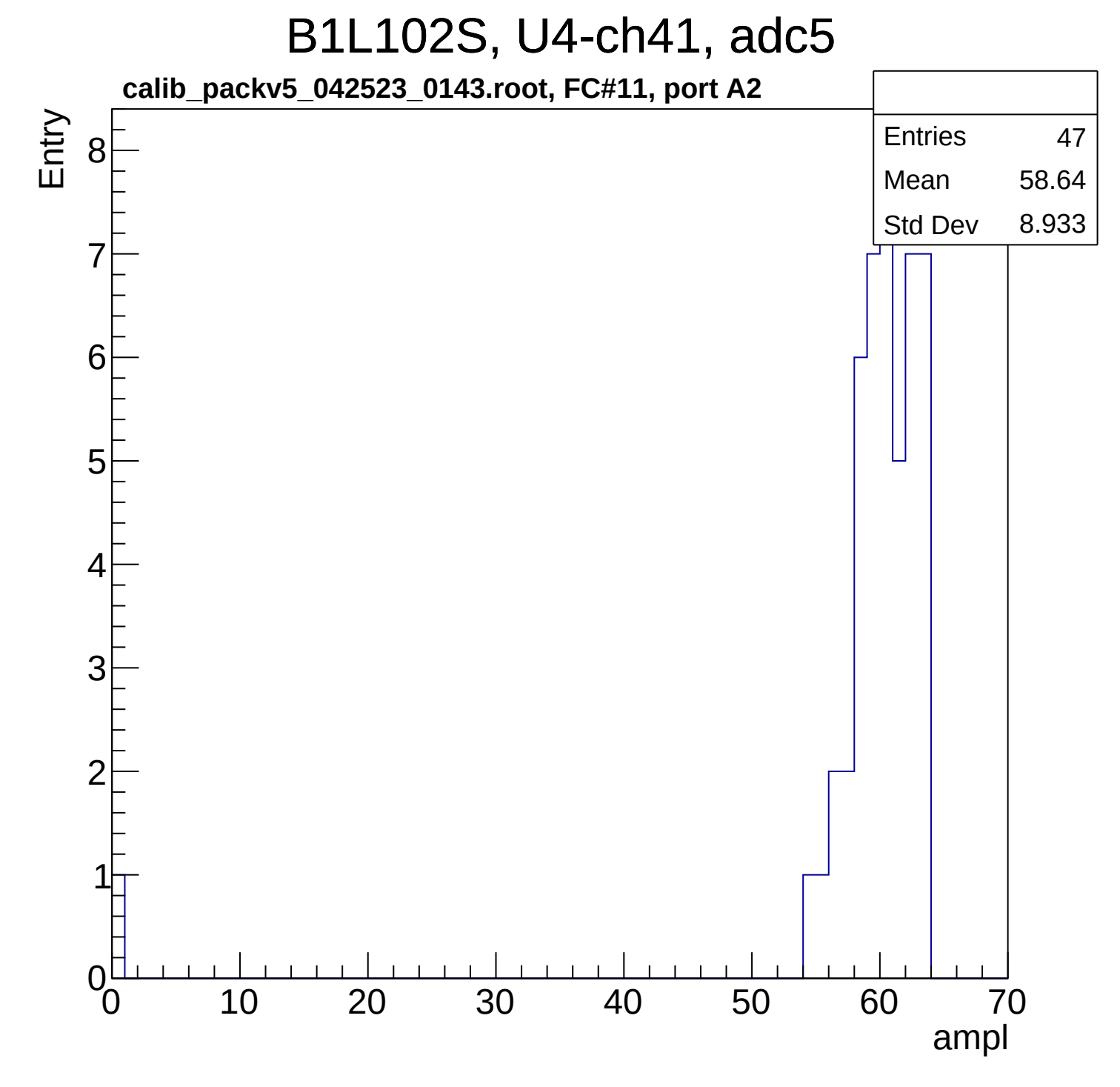
40
50
60
70


B1L102S, U4-ch41, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 80
Mean 48.74
Std Dev 3.744
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch41, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 55.17
Std Dev 3.425
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch41, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 47
Mean 58.64
Std Dev 8.933
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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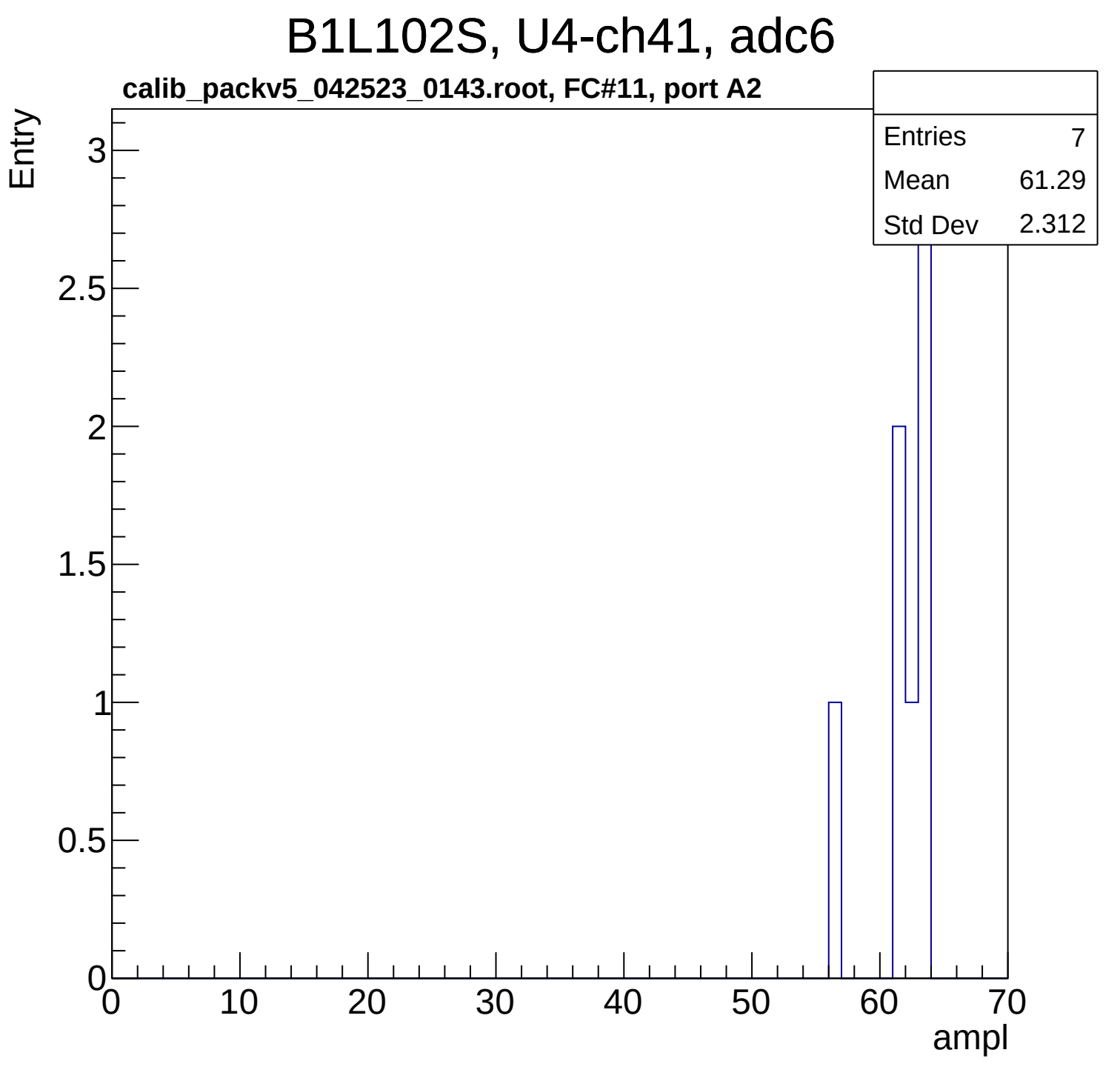
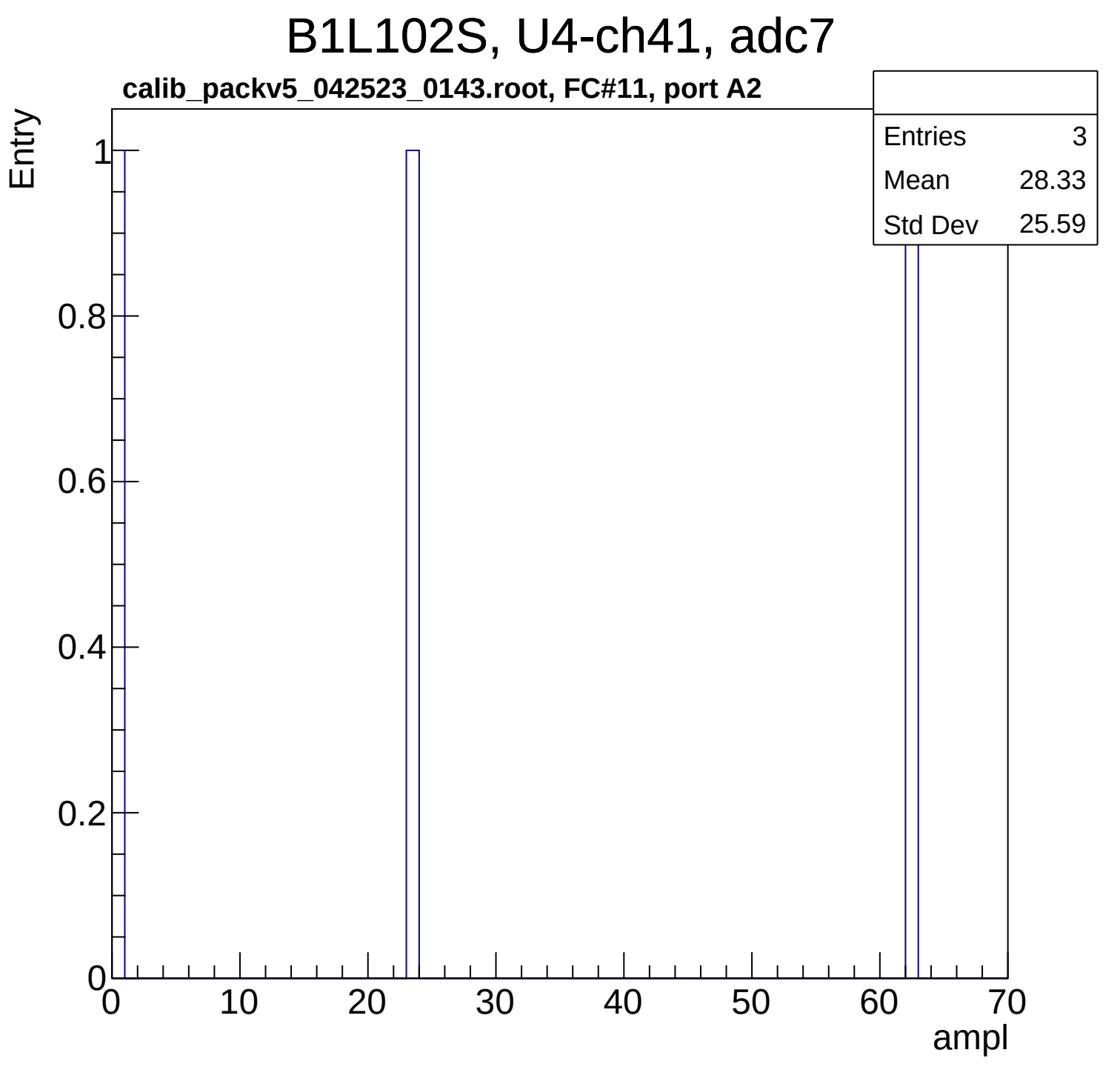

B1L102S, U4-ch41, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 7
Mean 61.29
Std Dev 2.312
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U4-ch41, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 28.33
Std Dev 25.59
Entry
ampl
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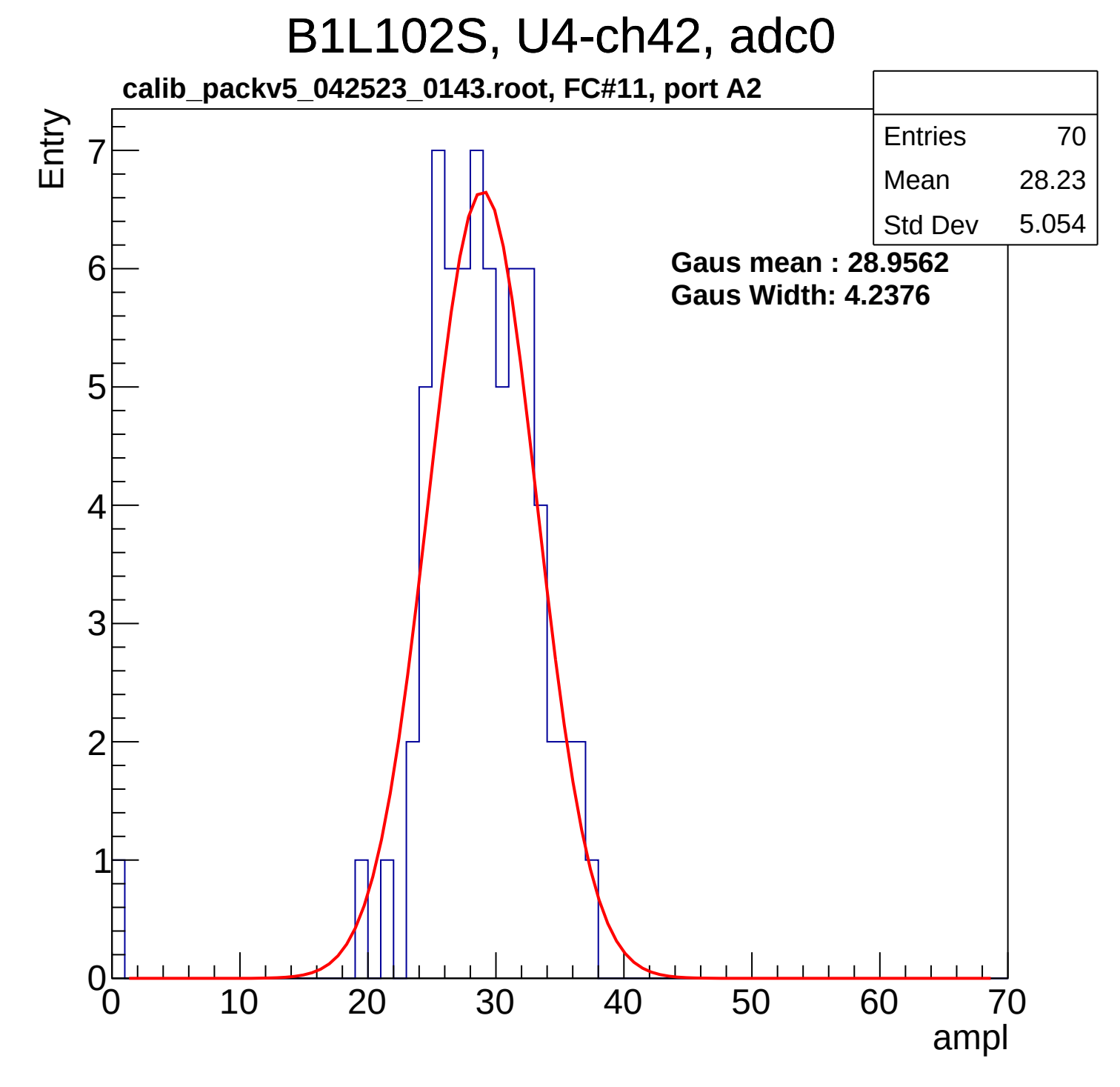
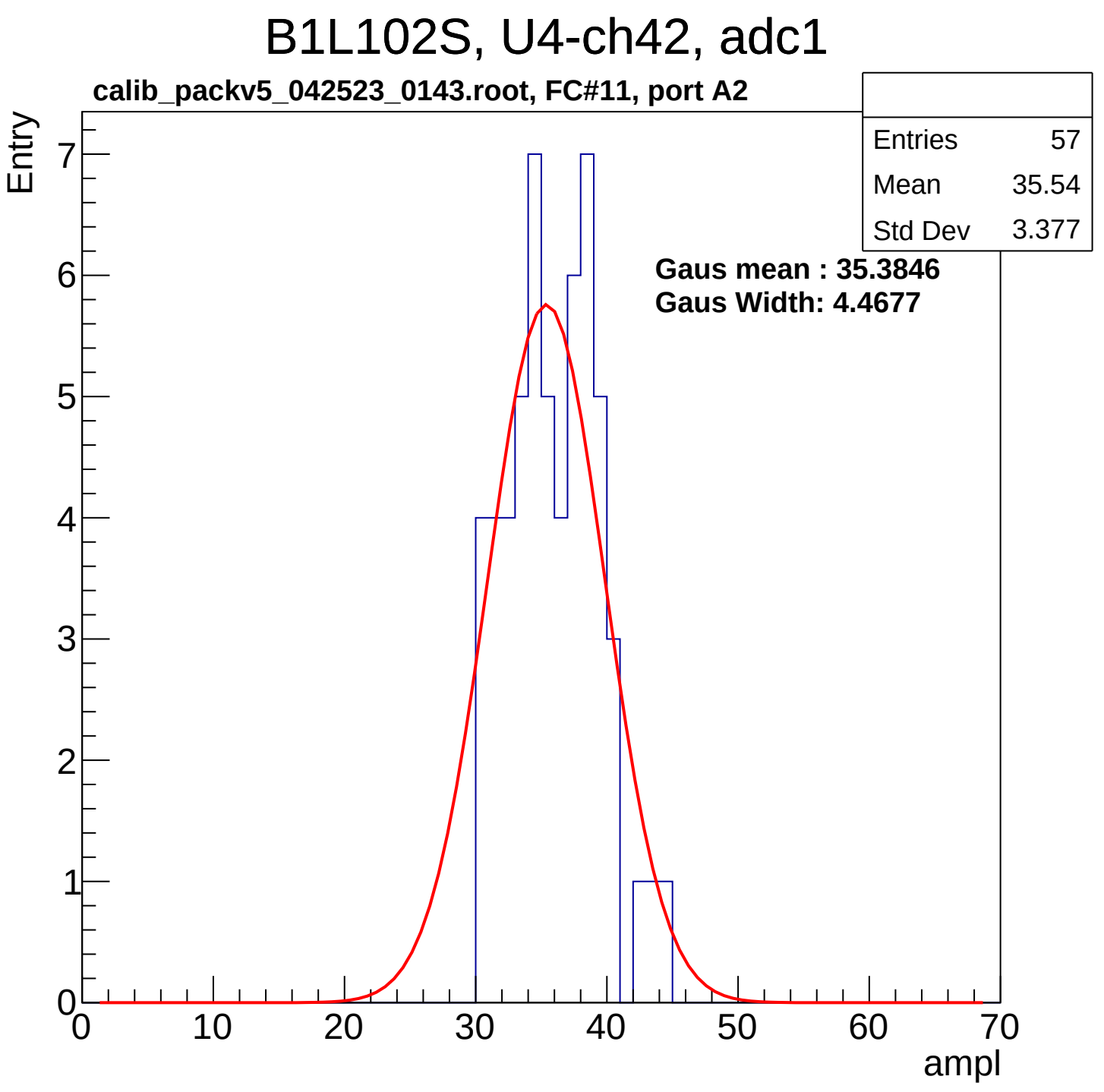
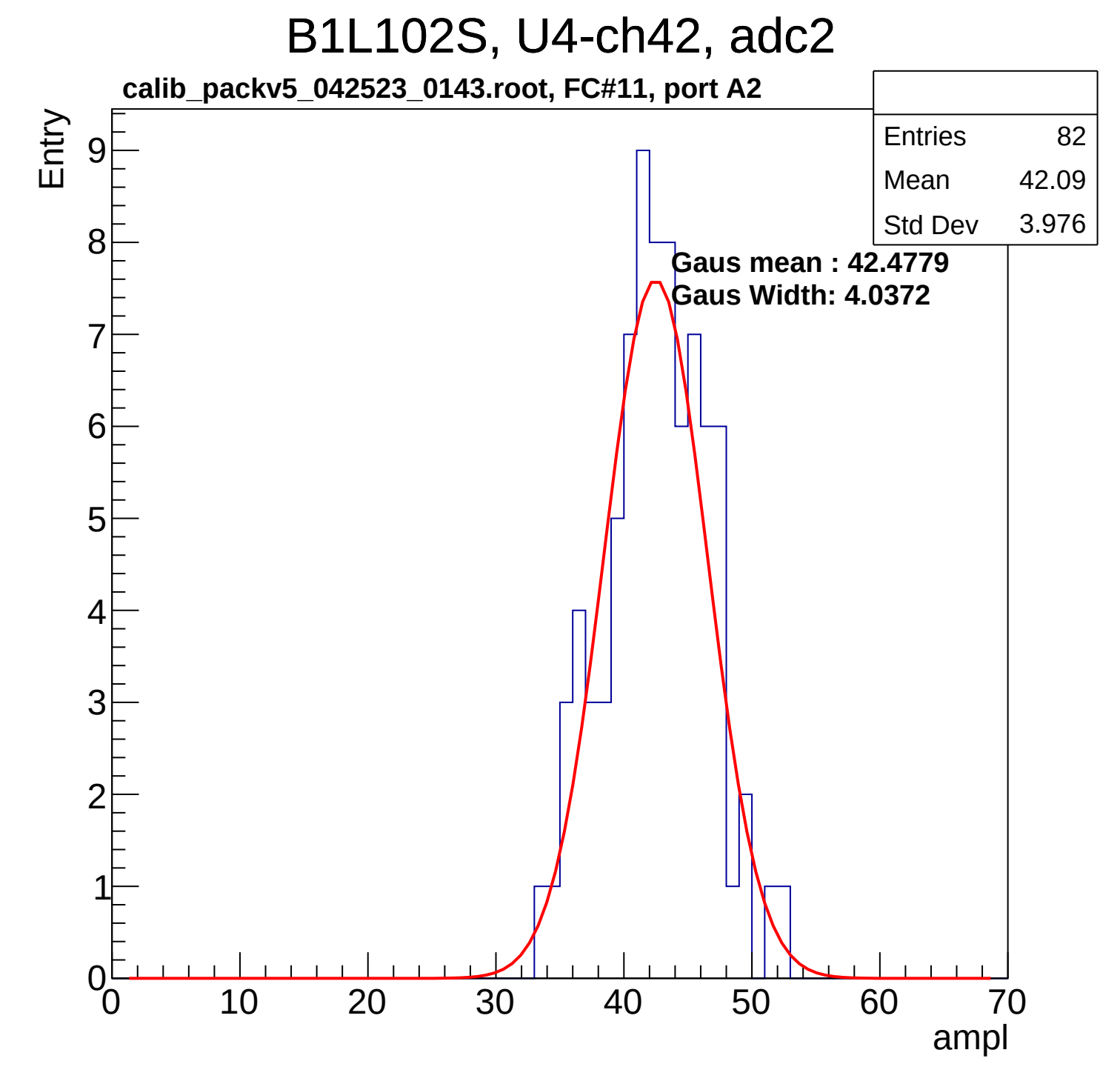
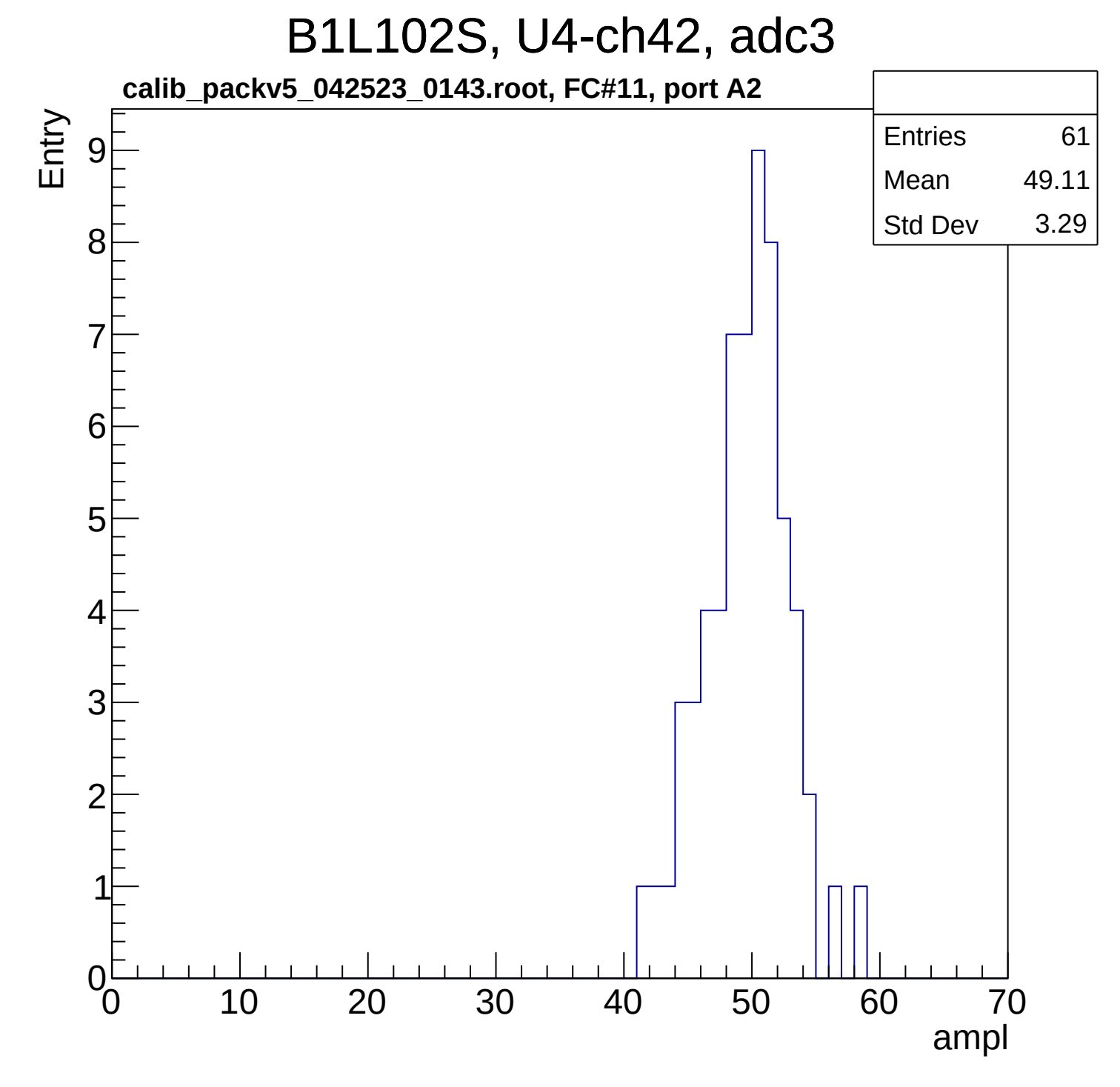
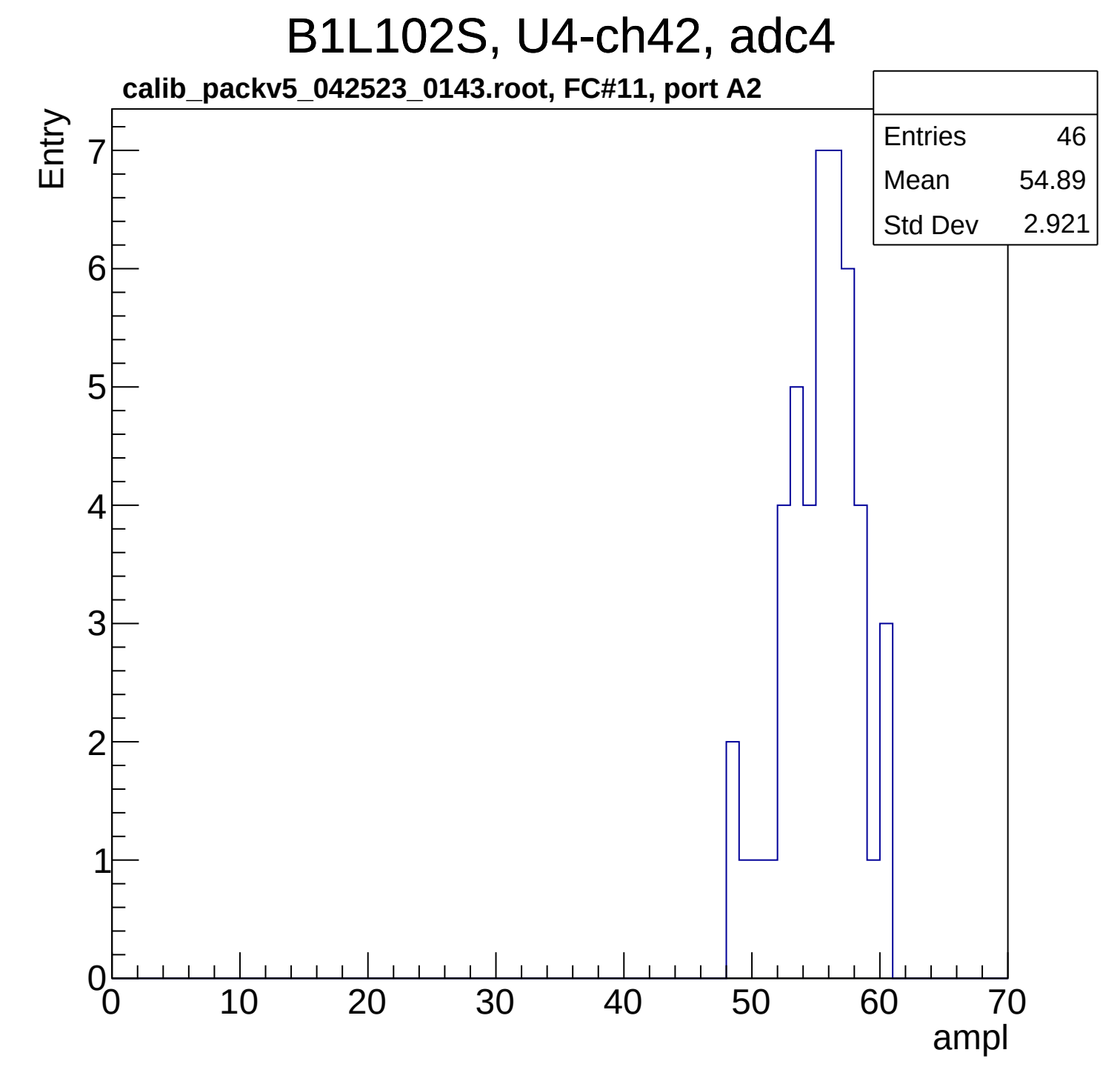
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L102S, U4-ch42, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 28.23
Std Dev 5.054
Gaus mean : 28.9562
Gaus Width: 4.2376
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch42, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 57
Mean 35.54
Std Dev 3.377
Gaus mean : 35.3846
Gaus Width: 4.4677
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch42, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 82
Mean 42.09
Std Dev 3.976
Gaus mean : 42.4779
Gaus Width: 4.0372
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch42, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 49.11
Std Dev 3.29
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch42, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 46
Mean 54.89
Std Dev 2.921
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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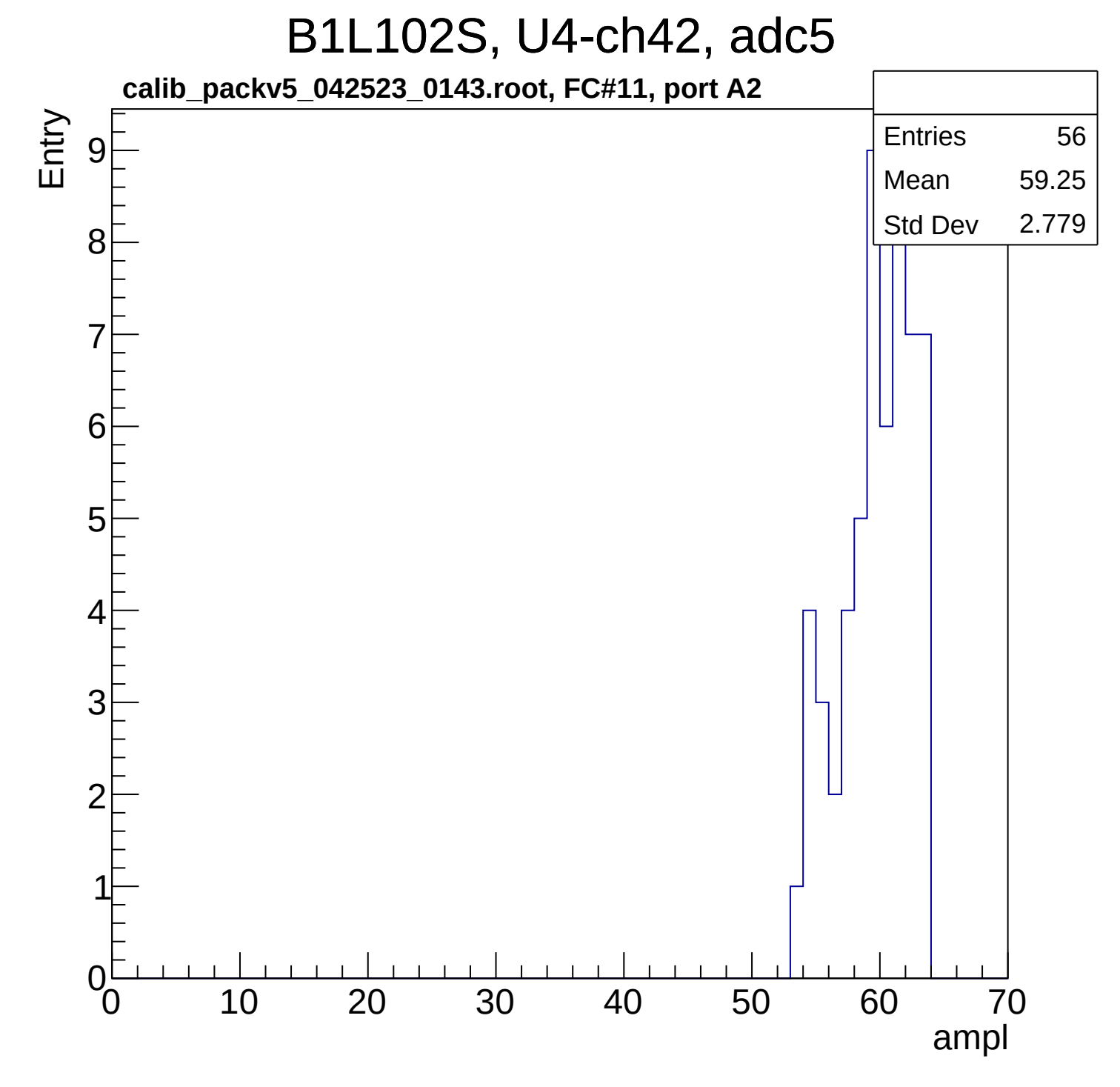
B1L102S, U4-ch42, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 59.25
Std Dev 2.779
Entry
ampl
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2
3
4
5
6
7
8
9
0
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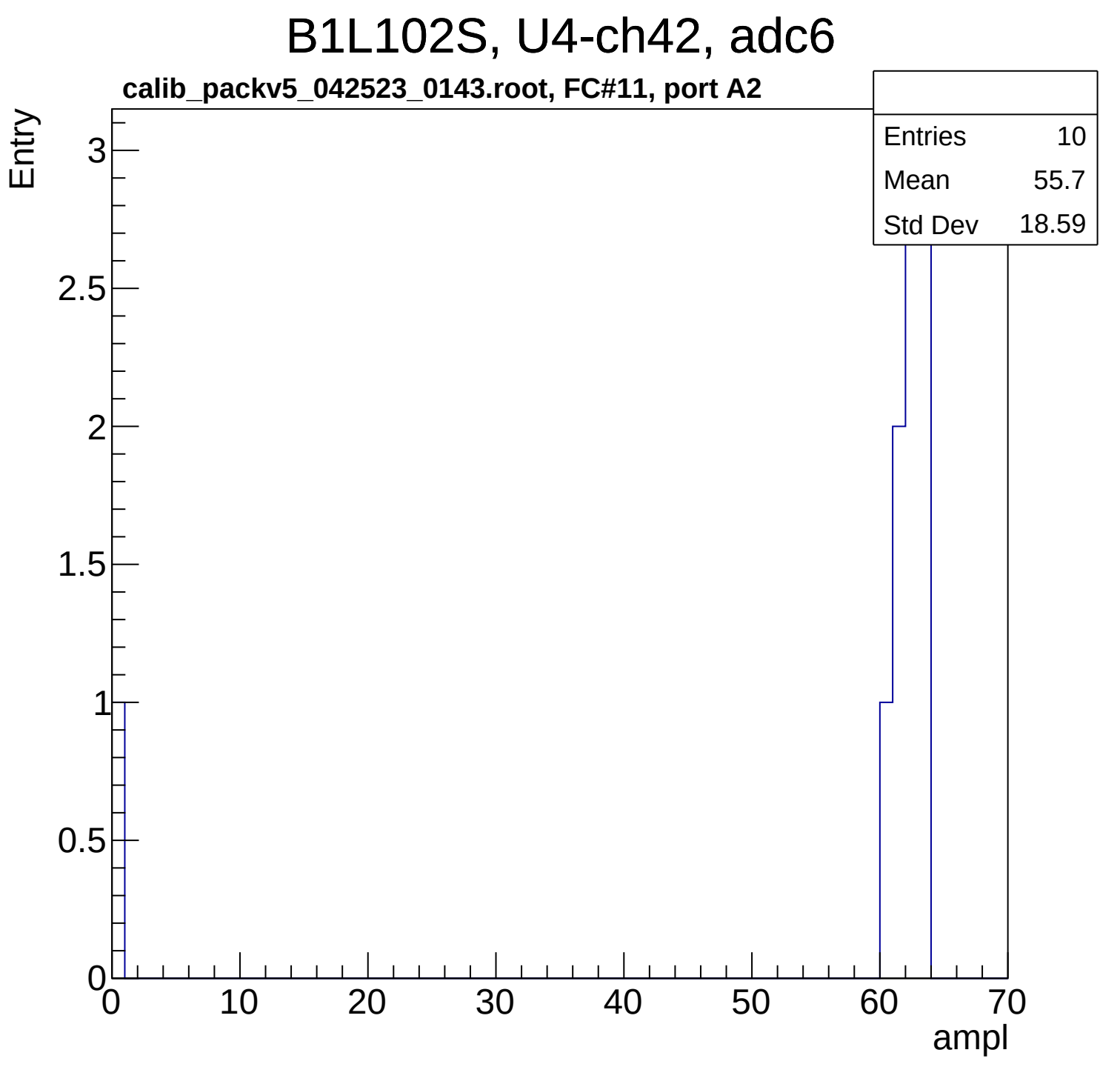
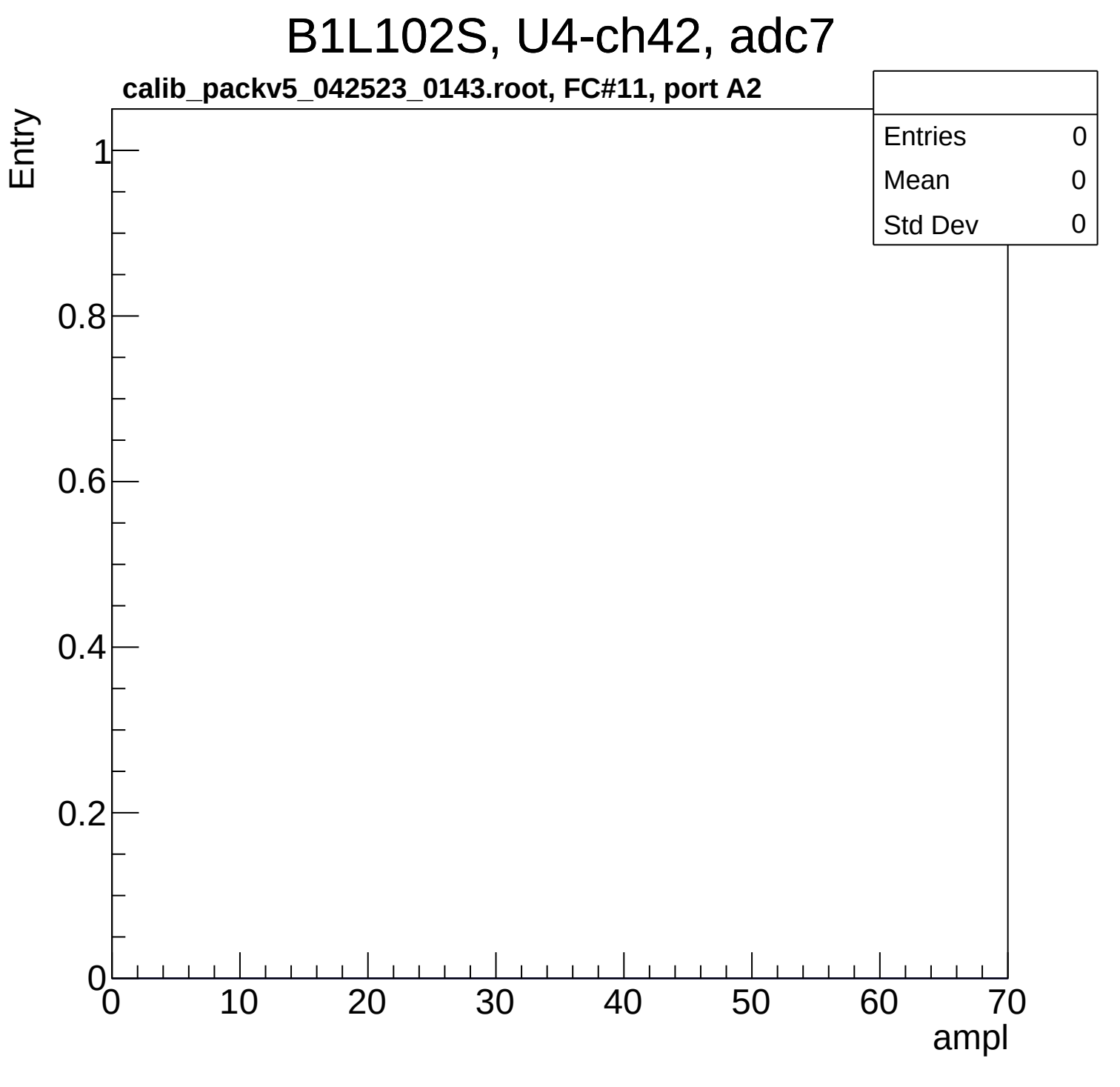
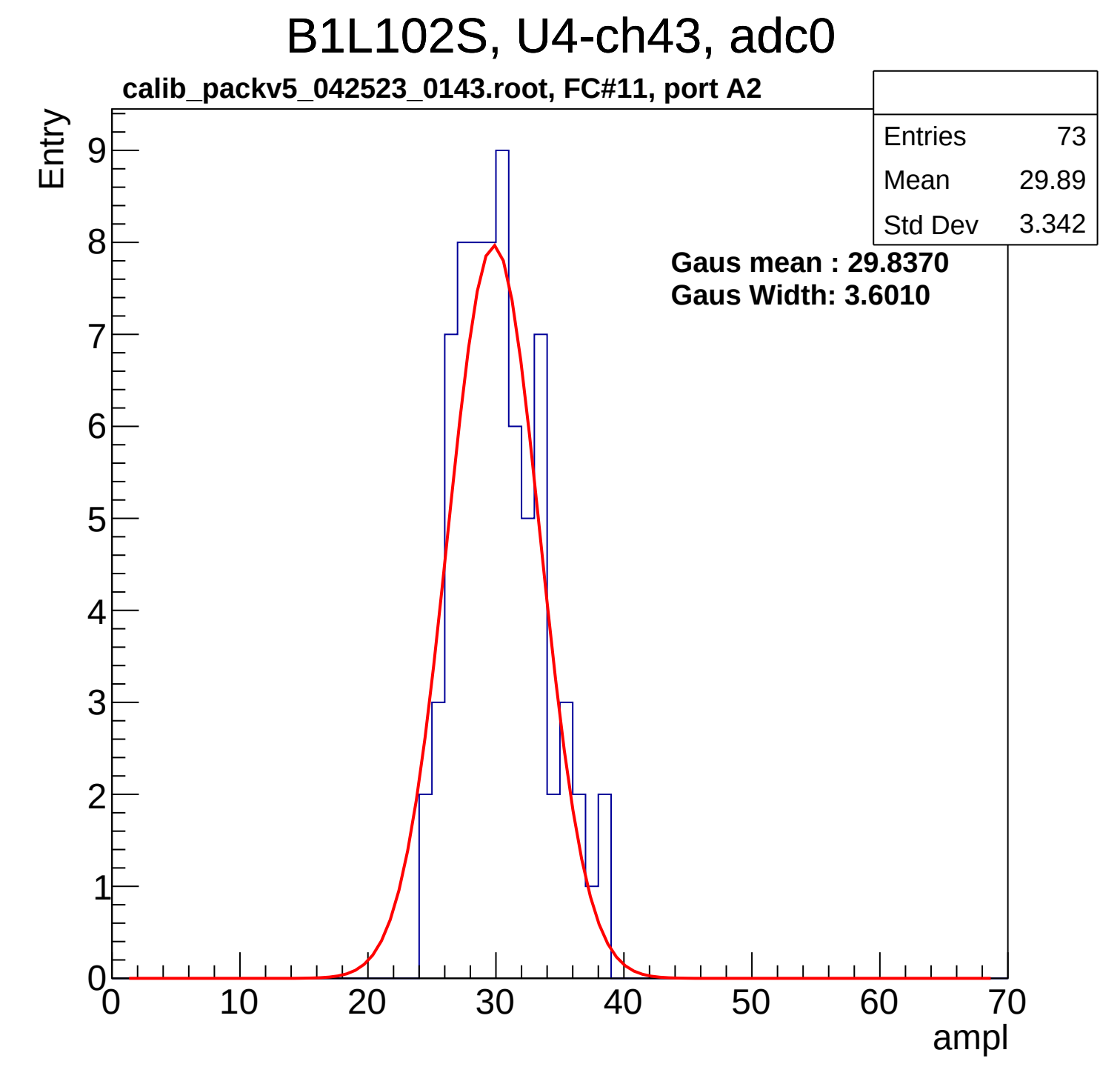

B1L102S, U4-ch42, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 10
Mean 55.7
Std Dev 18.59
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch42, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch43, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 29.89
Std Dev 3.342
Gaus mean : 29.8370
Gaus Width: 3.6010
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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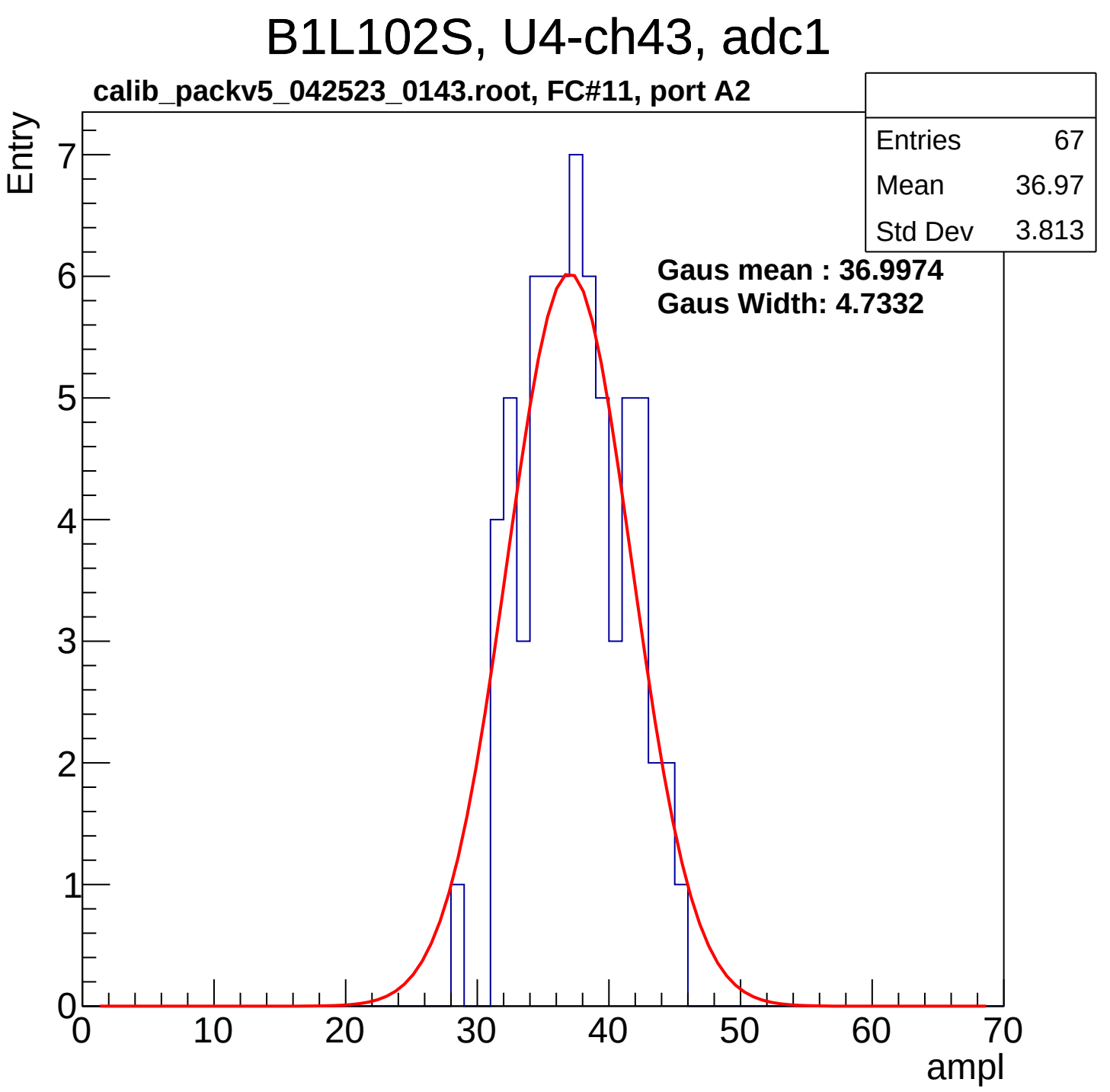
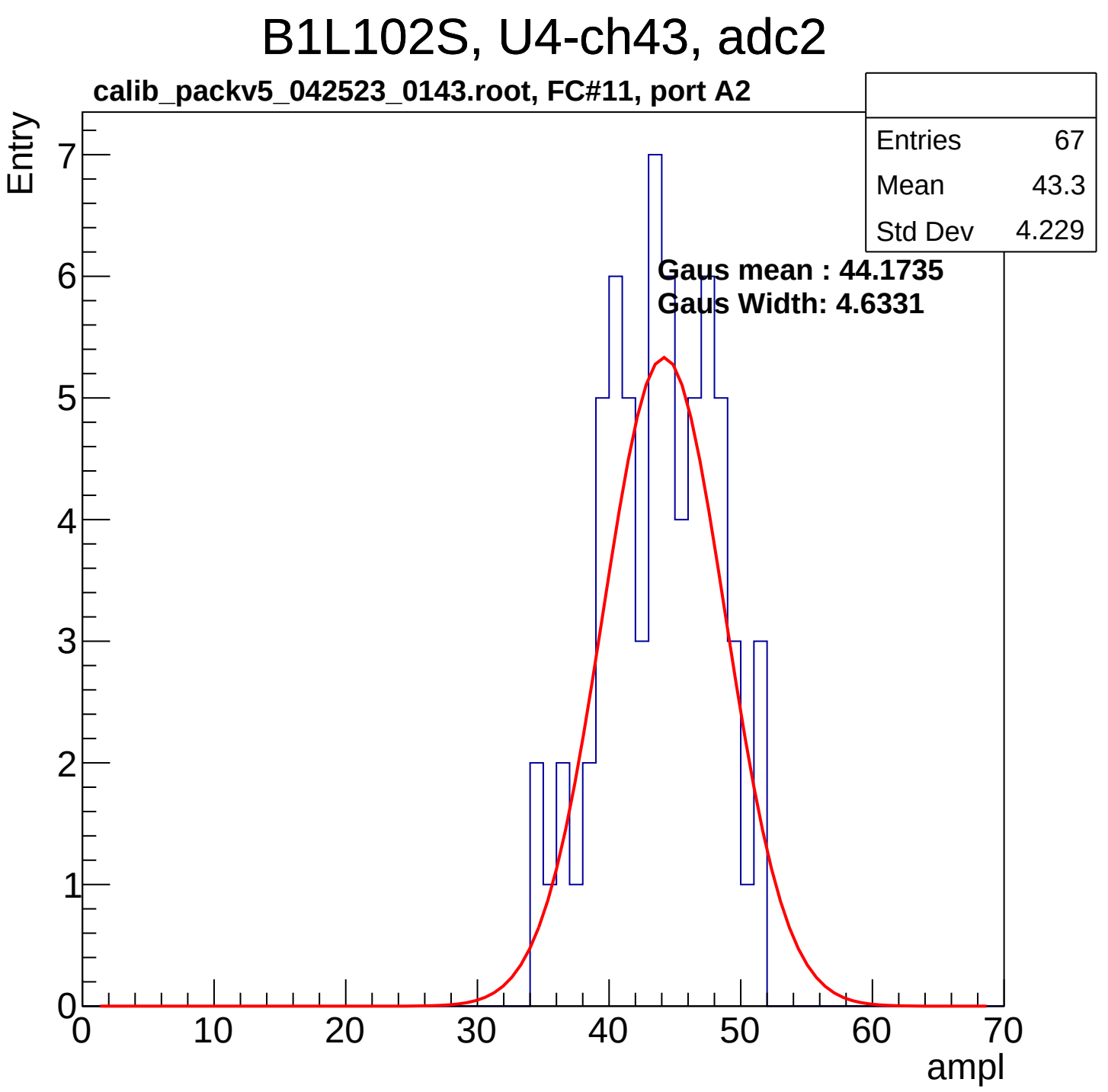

B1L102S, U4-ch43, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 36.97
Std Dev 3.813
Gaus mean : 36.9974
Gaus Width: 4.7332
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch43, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 43.3
Std Dev 4.229
Gaus mean : 44.1735
Gaus Width: 4.6331
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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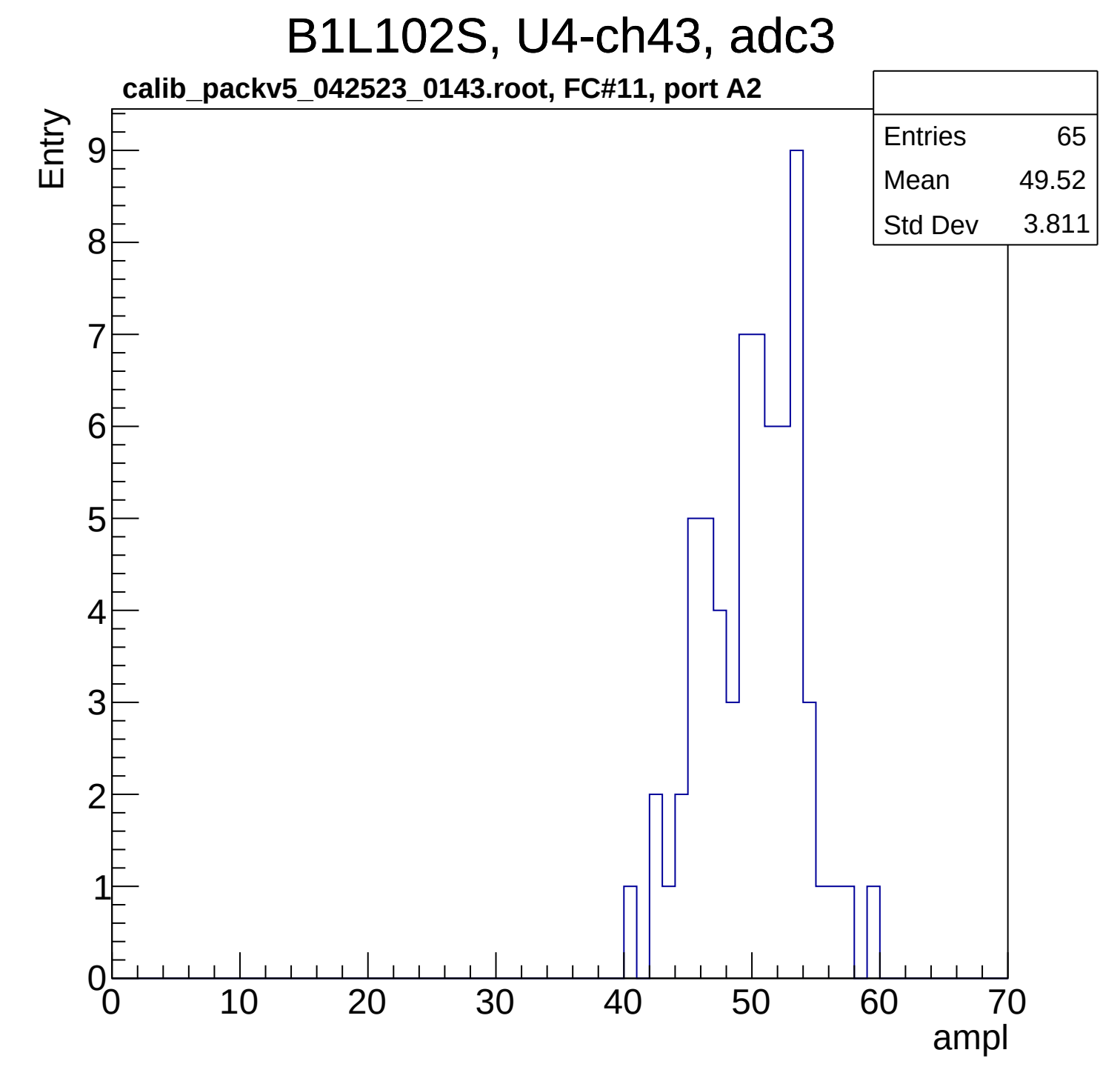
B1L102S, U4-ch43, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 49.52
Std Dev 3.811
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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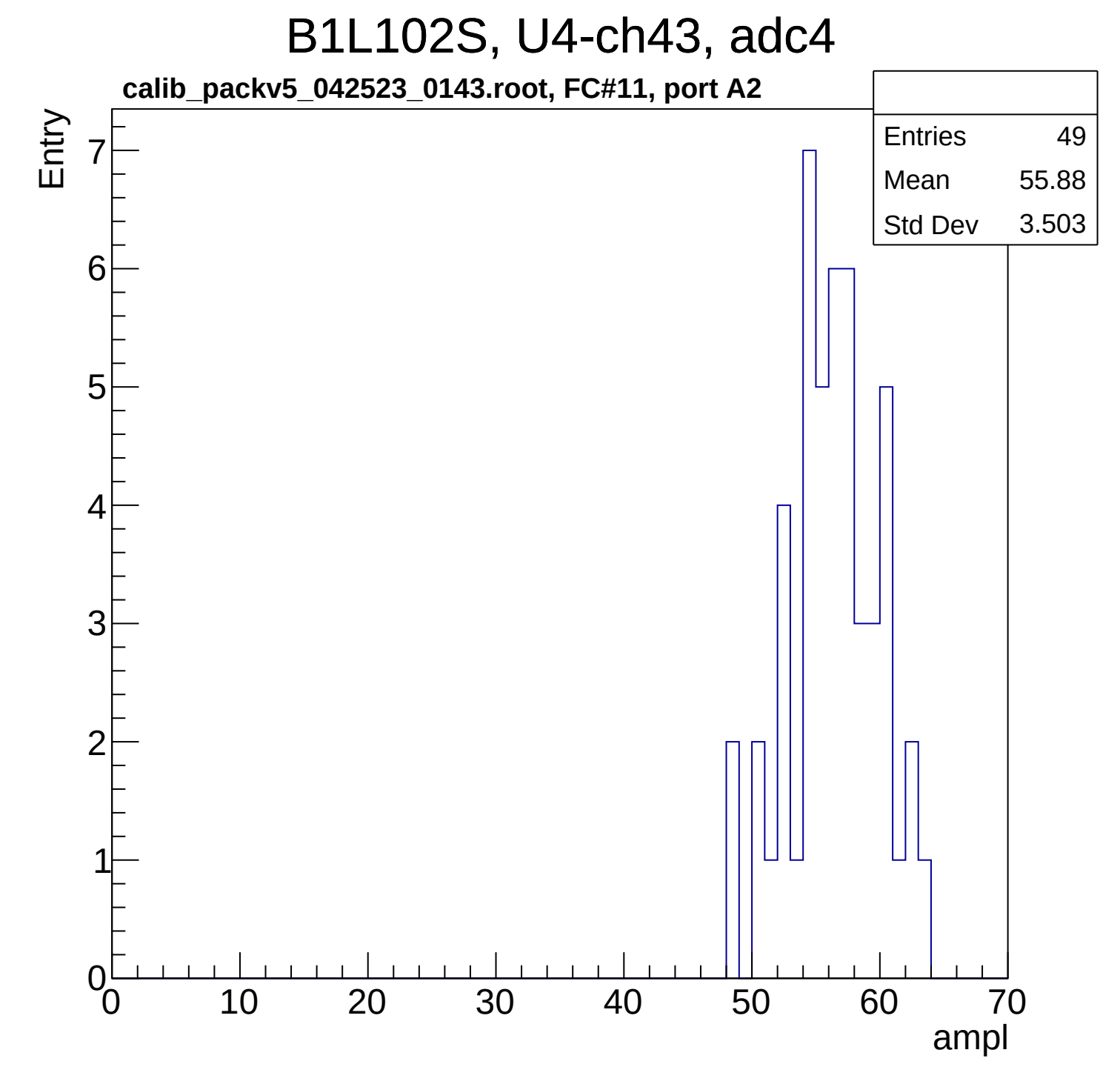
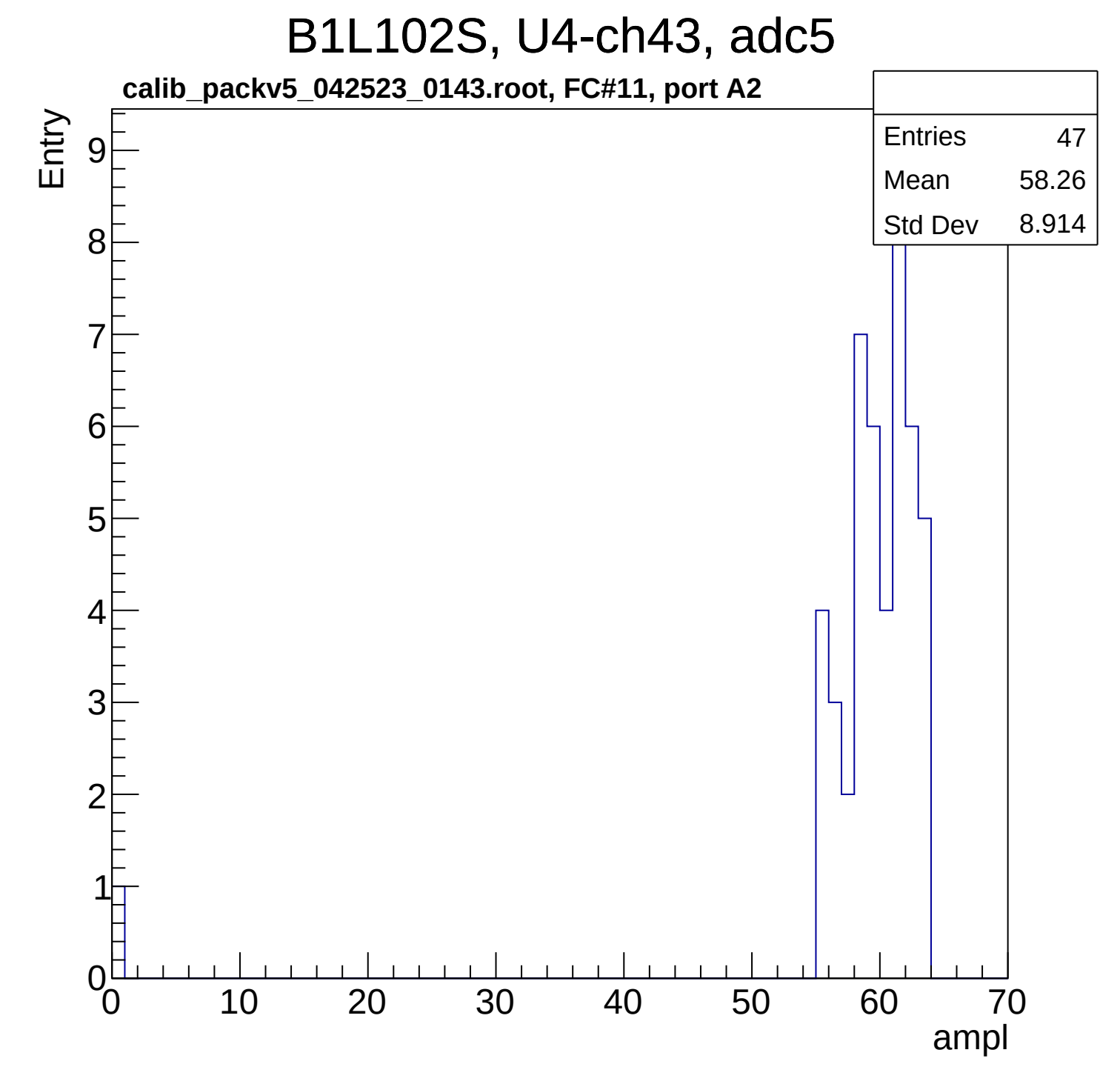

B1L102S, U4-ch43, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 55.88
Std Dev 3.503
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch43, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 47
Mean 58.26
Std Dev 8.914
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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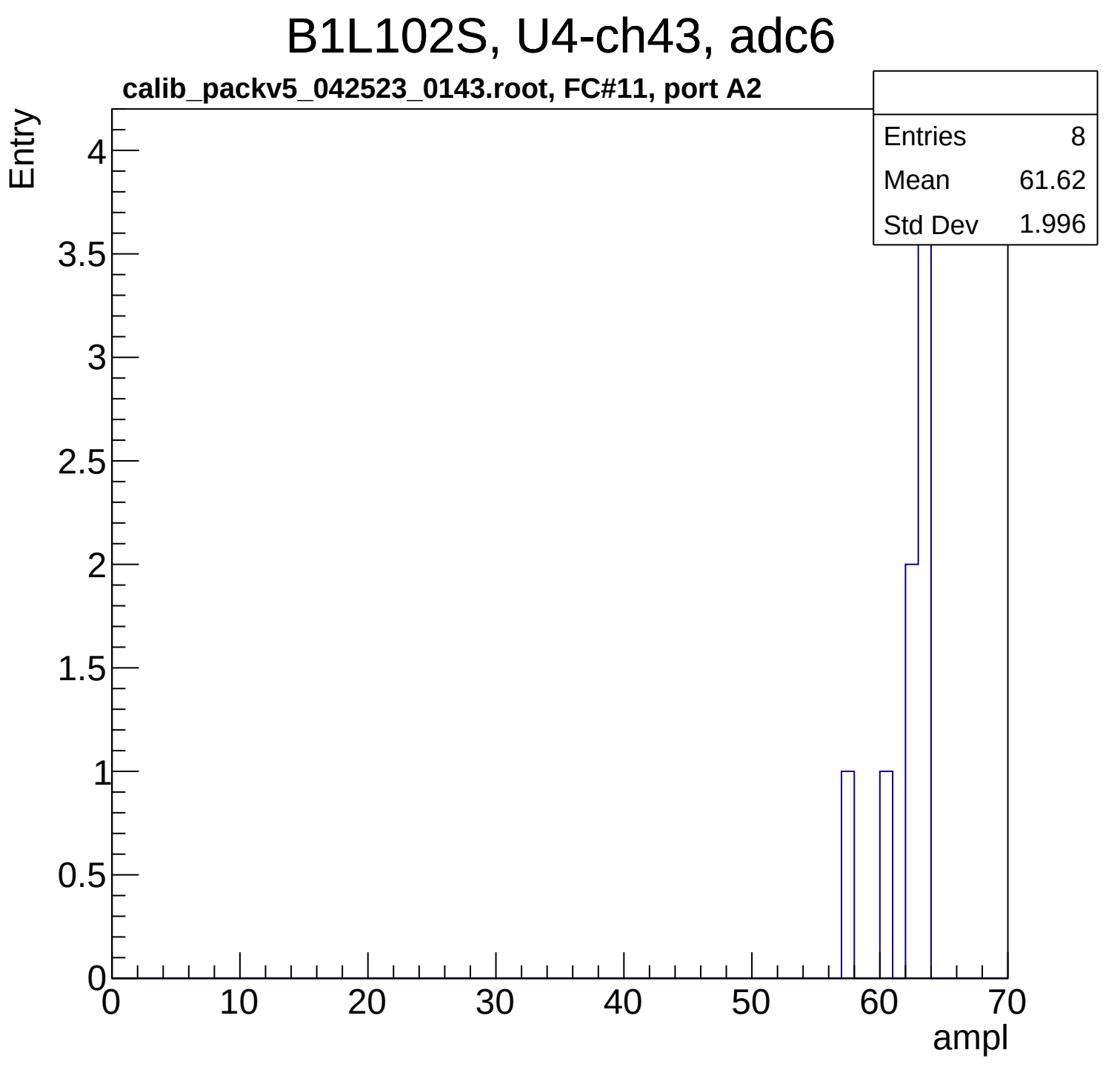
B1L102S, U4-ch43, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 8
Mean 61.62
Std Dev 1.996
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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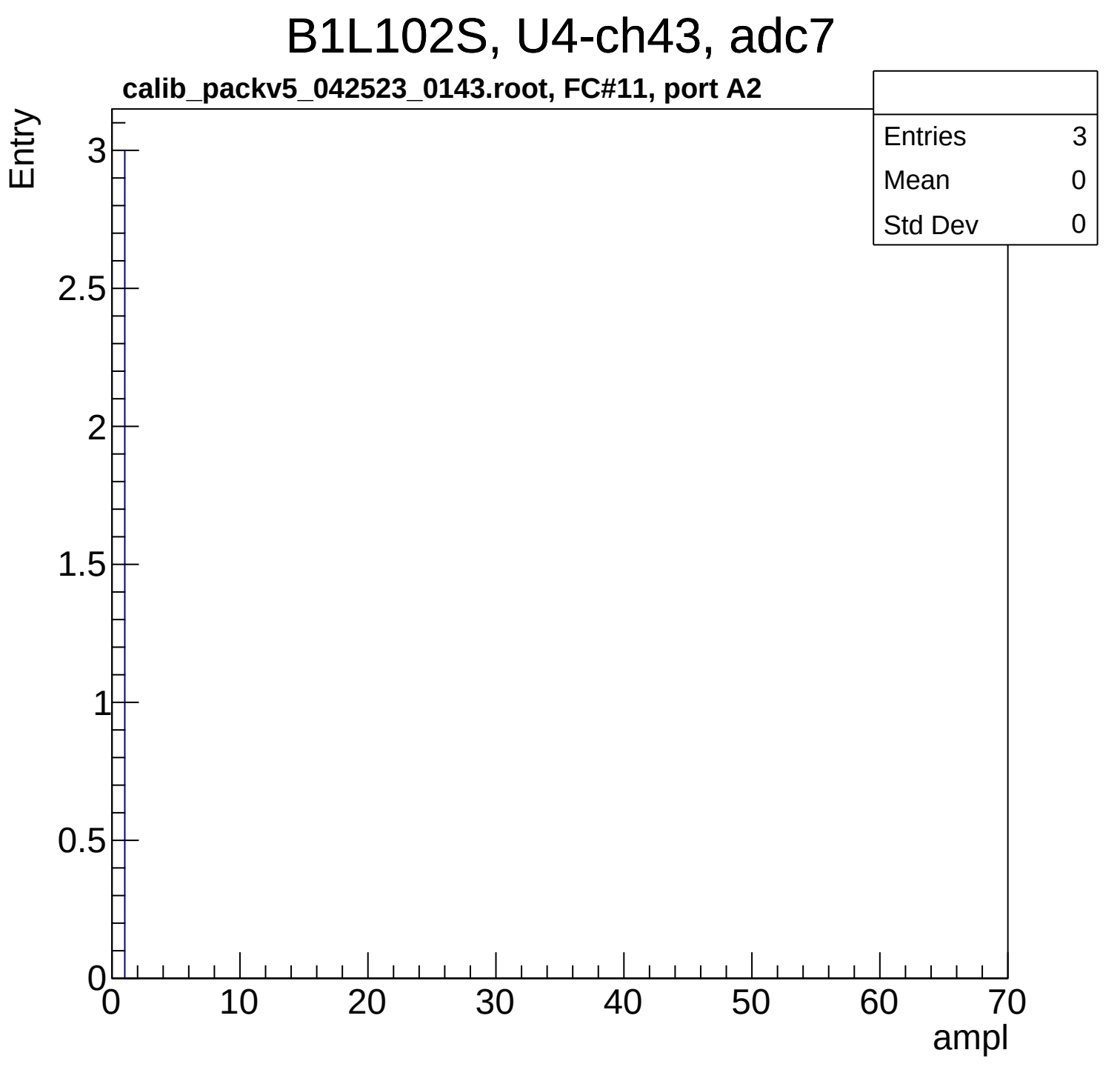
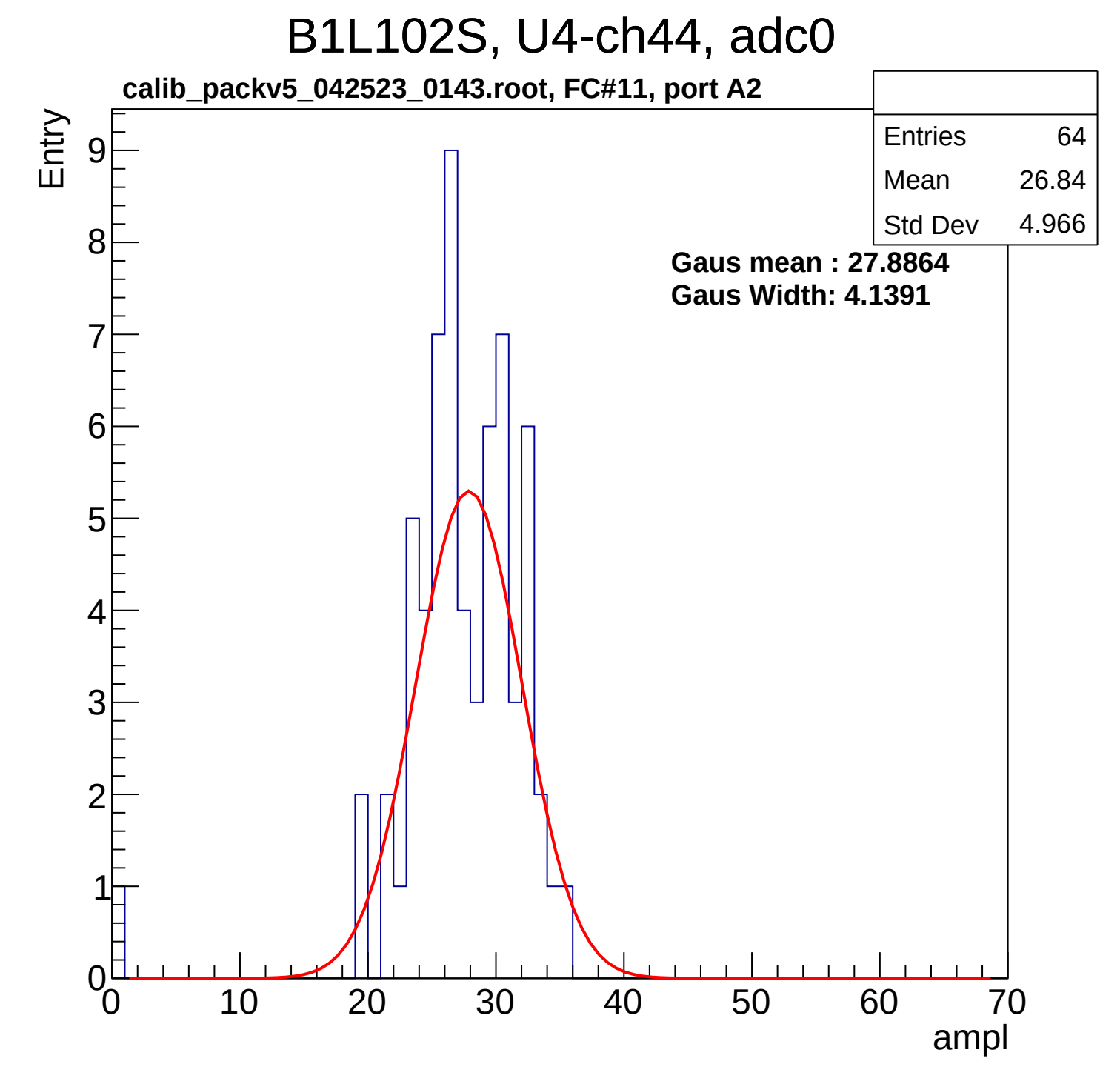
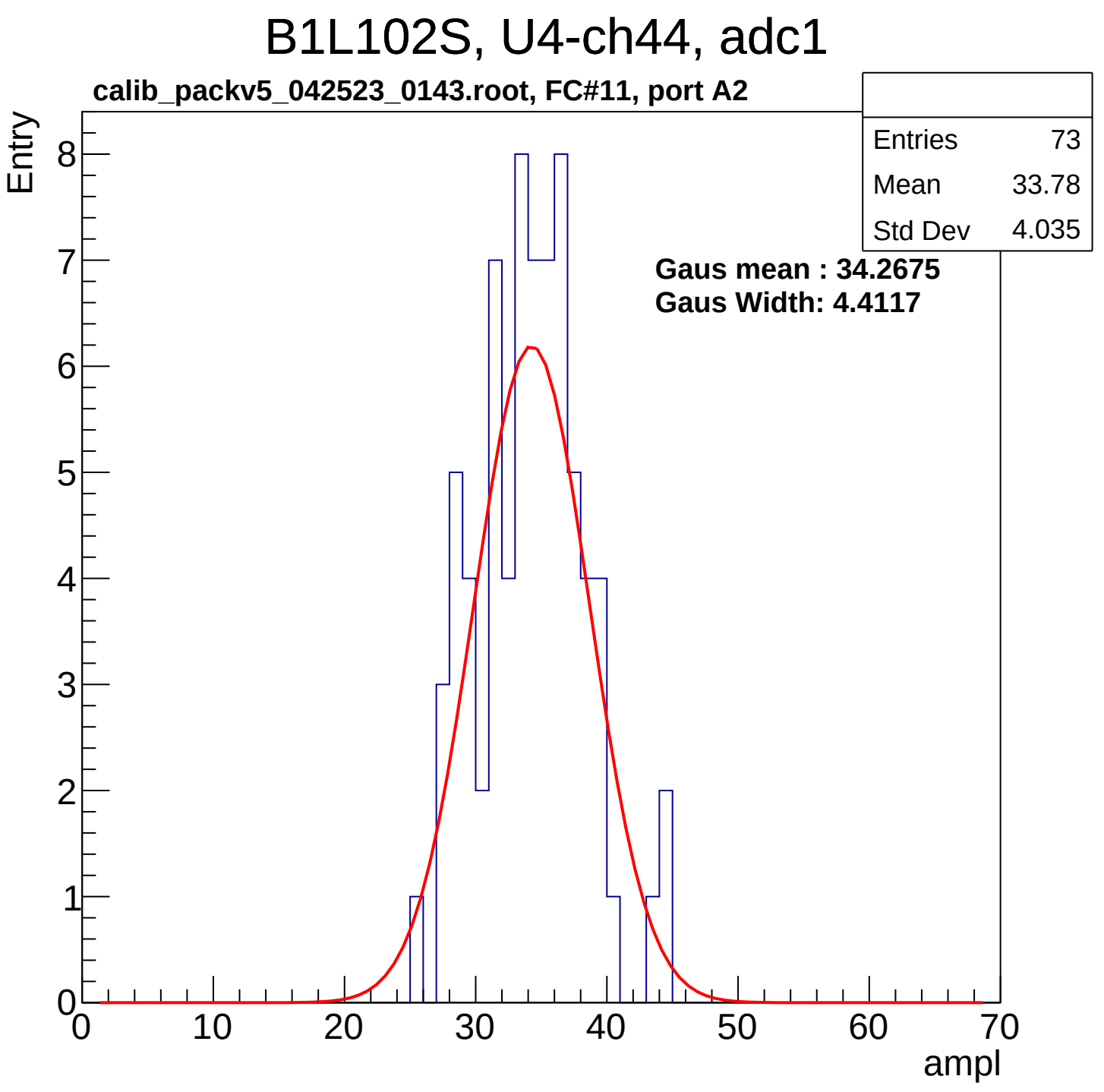
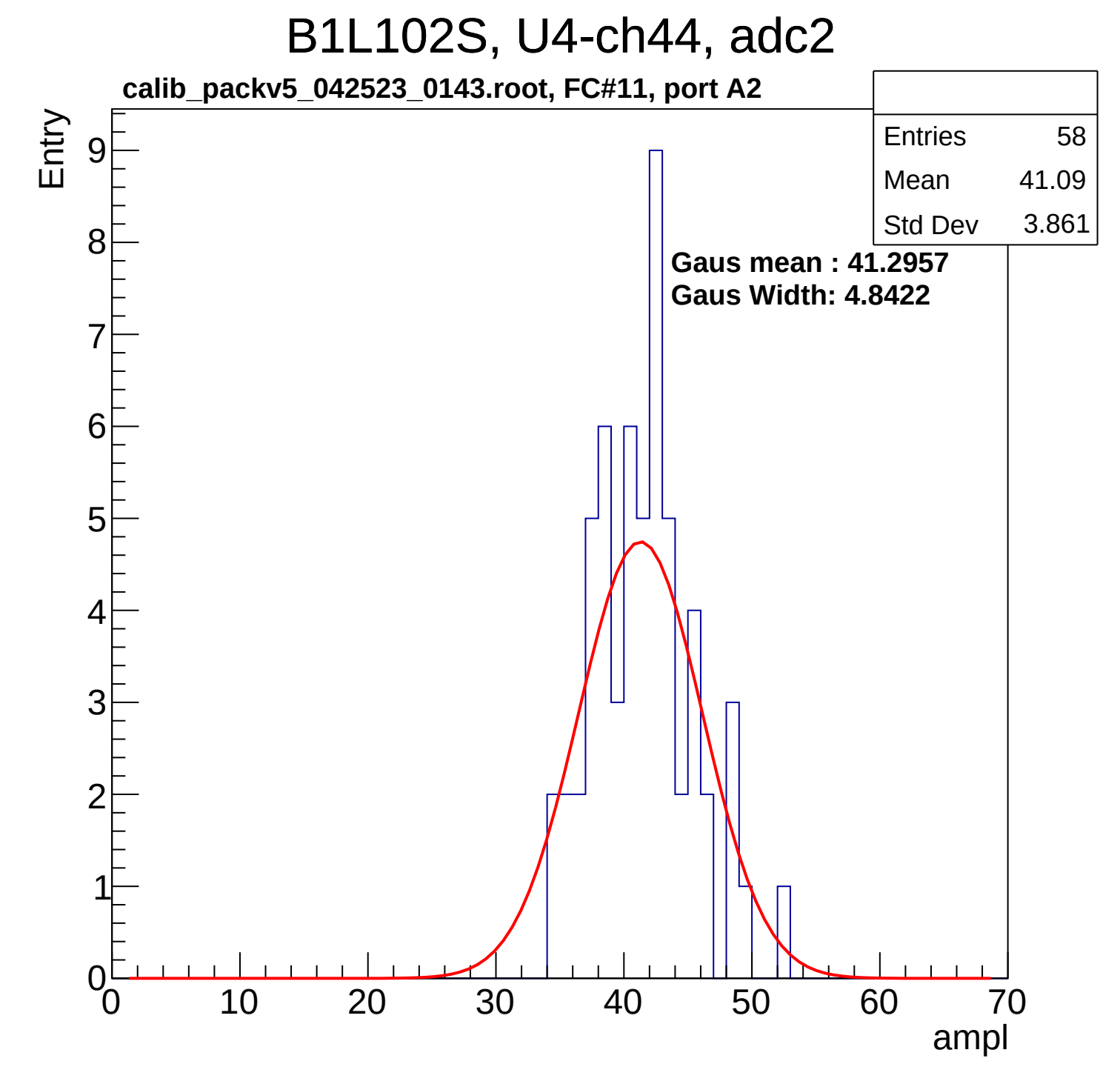
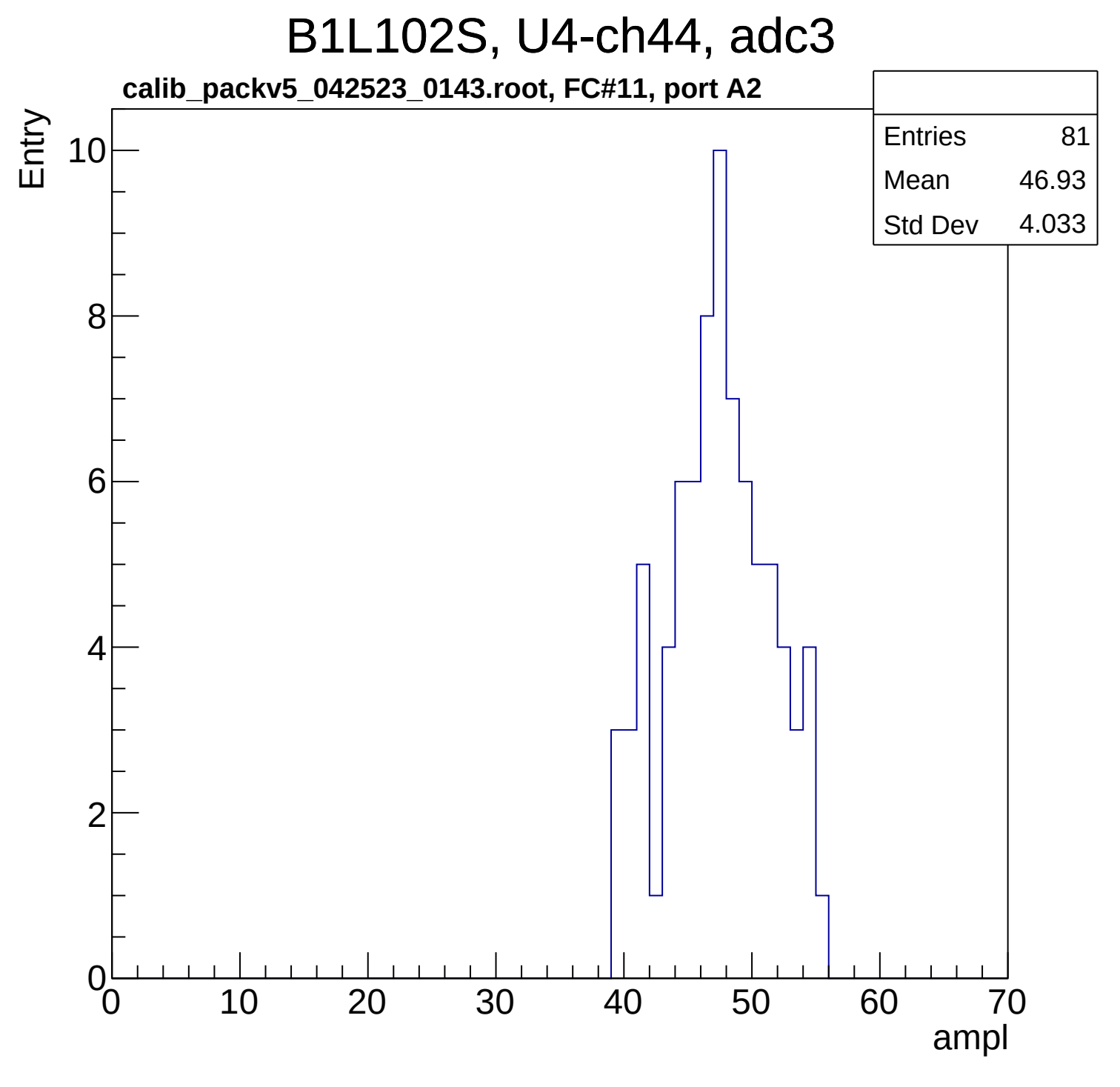
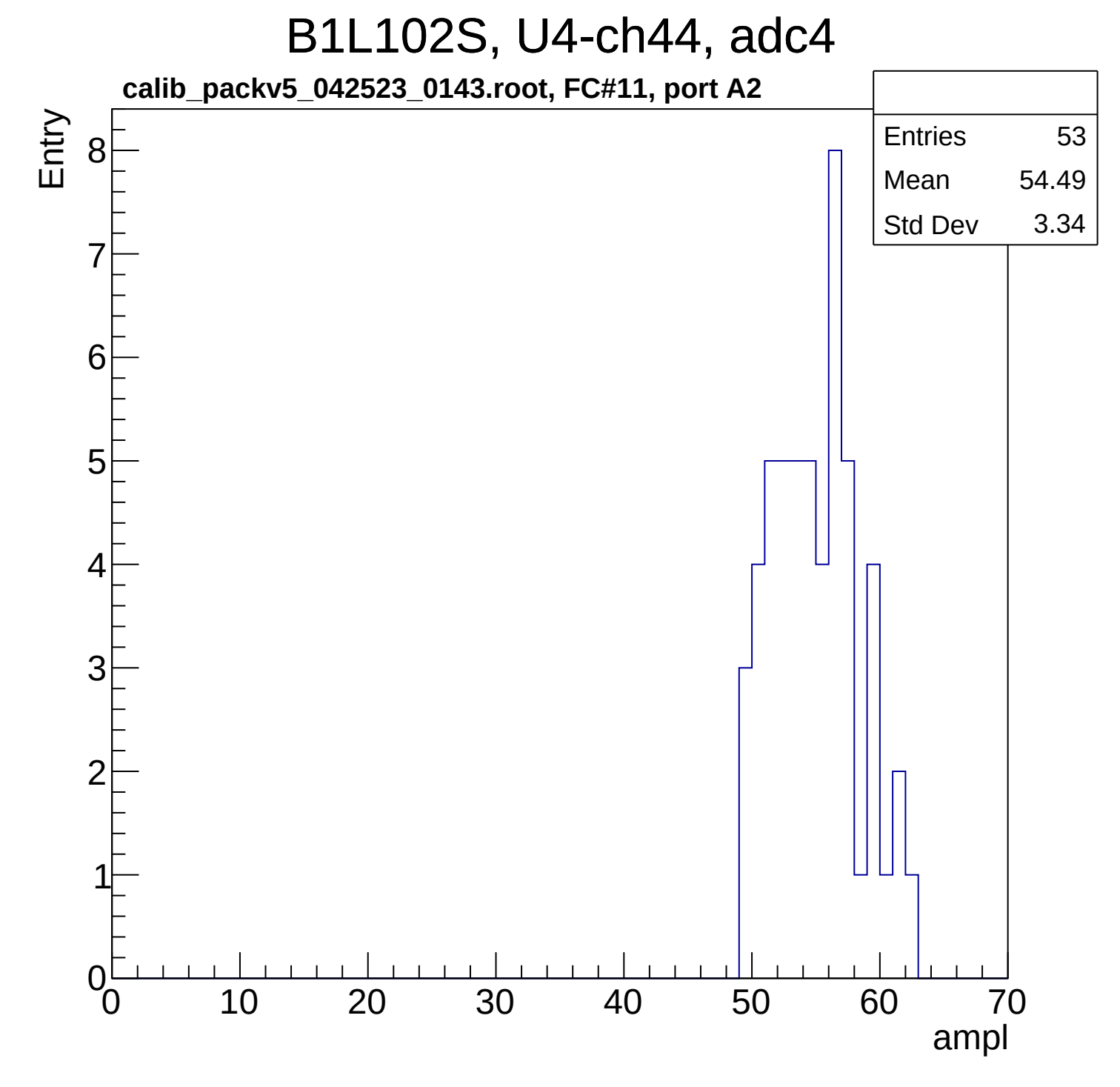

B1L102S, U4-ch43, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 0
Std Dev 0
Entry
3
2.5
2
1.5
1
0.5
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch44, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 26.84
Std Dev 4.966
Gaus mean : 27.8864
Gaus Width: 4.1391
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch44, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 33.78
Std Dev 4.035
Gaus mean : 34.2675
Gaus Width: 4.4117
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch44, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 41.09
Std Dev 3.861
Gaus mean : 41.2957
Gaus Width: 4.8422
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch44, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 81
Mean 46.93
Std Dev 4.033
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch44, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 54.49
Std Dev 3.34
Entry
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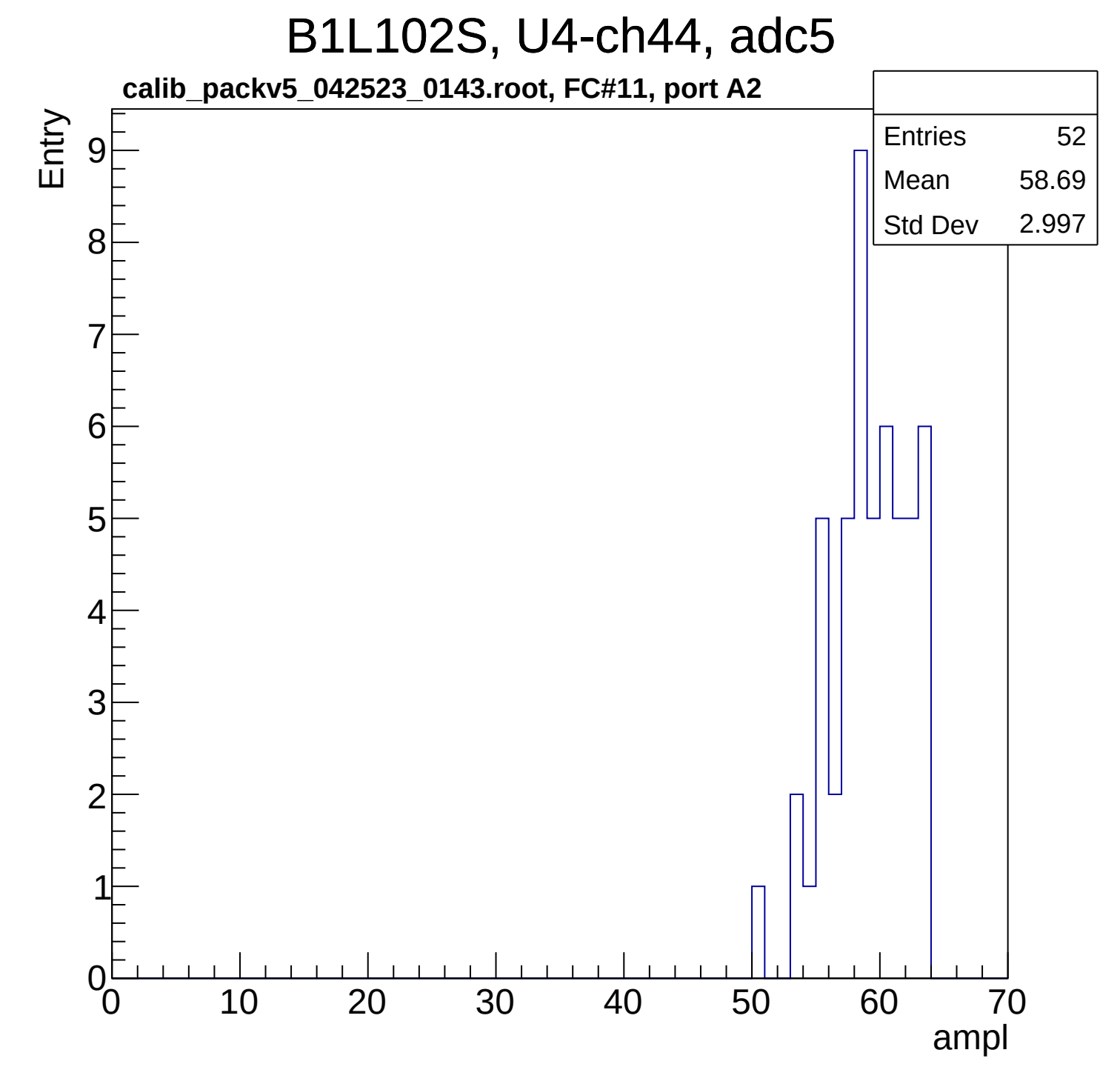
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch44, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 52
Mean 58.69
Std Dev 2.997
Entry
ampl
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2
3
4
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6
7
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0
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60
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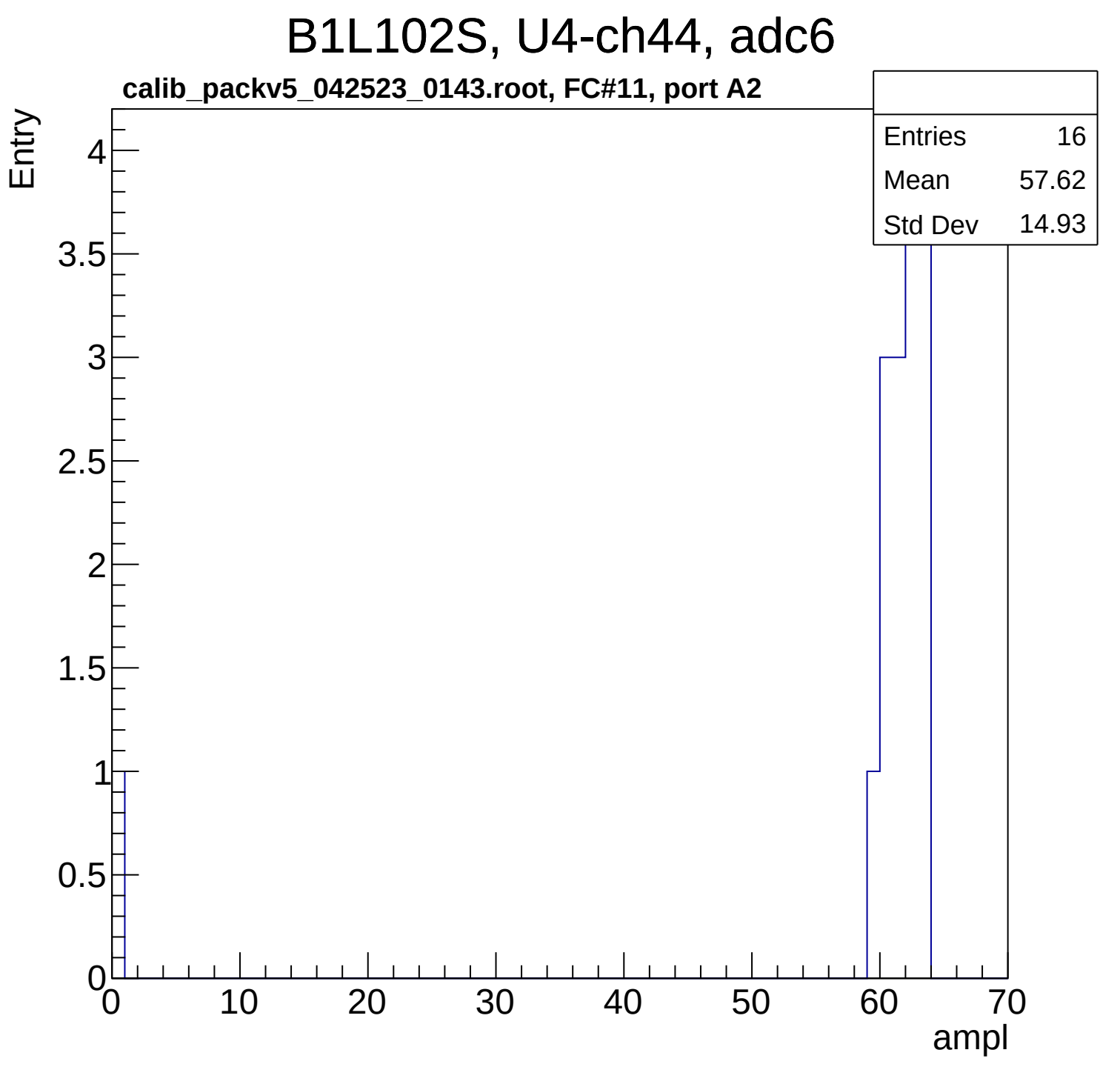
B1L102S, U4-ch44, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 16
Mean 57.62
Std Dev 14.93
Entry
ampl
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0.5
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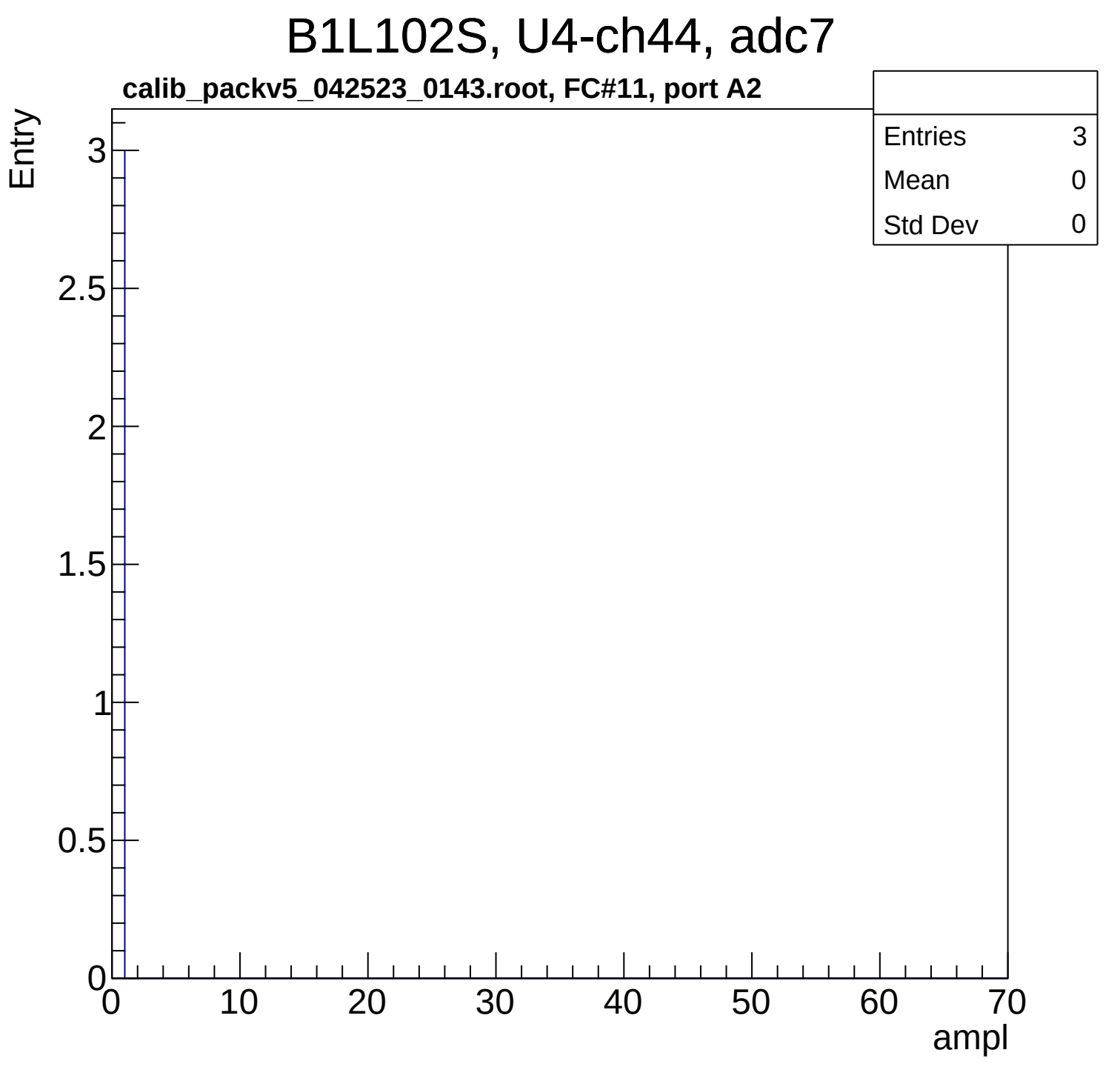
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U4-ch44, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 0
Std Dev 0
Entry
3
2.5
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1.5
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0.5
0
0
10
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30
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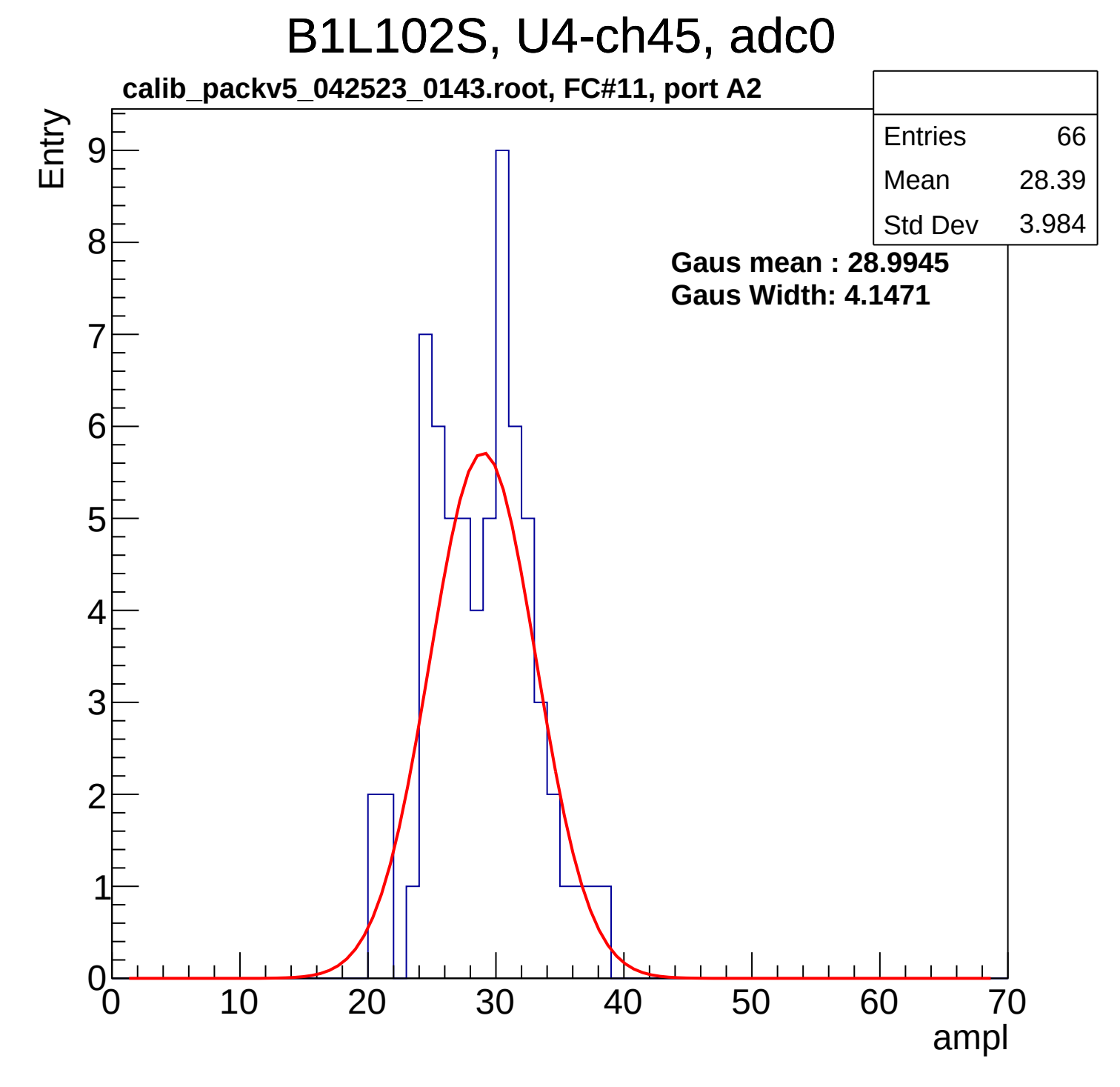
50
60
70
ampl


B1L102S, U4-ch45, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 28.39
Std Dev 3.984
Gaus mean : 28.9945
Gaus Width: 4.1471
Entry
ampl
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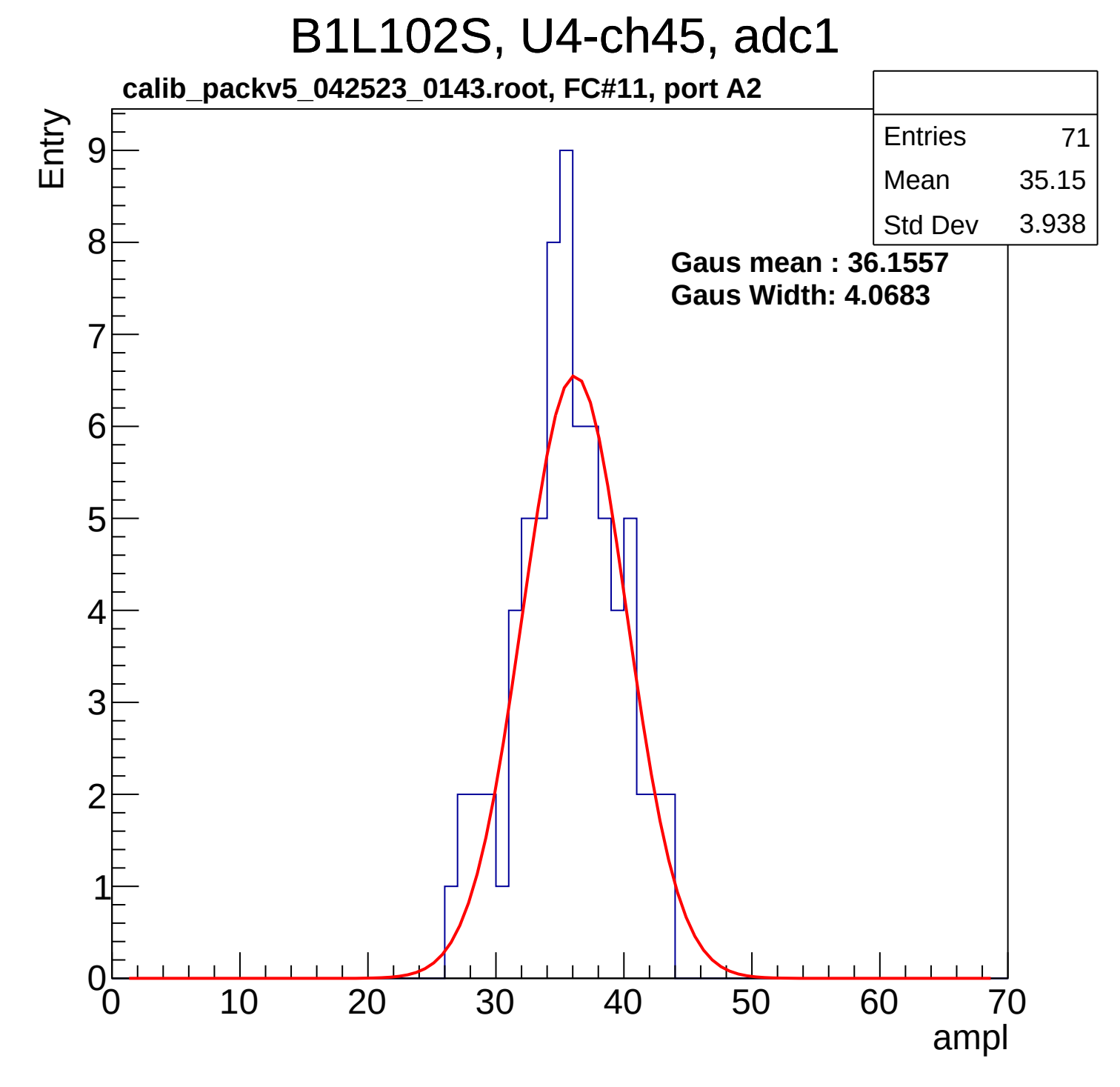
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch45, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 35.15
Std Dev 3.938
Gaus mean : 36.1557
Gaus Width: 4.0683
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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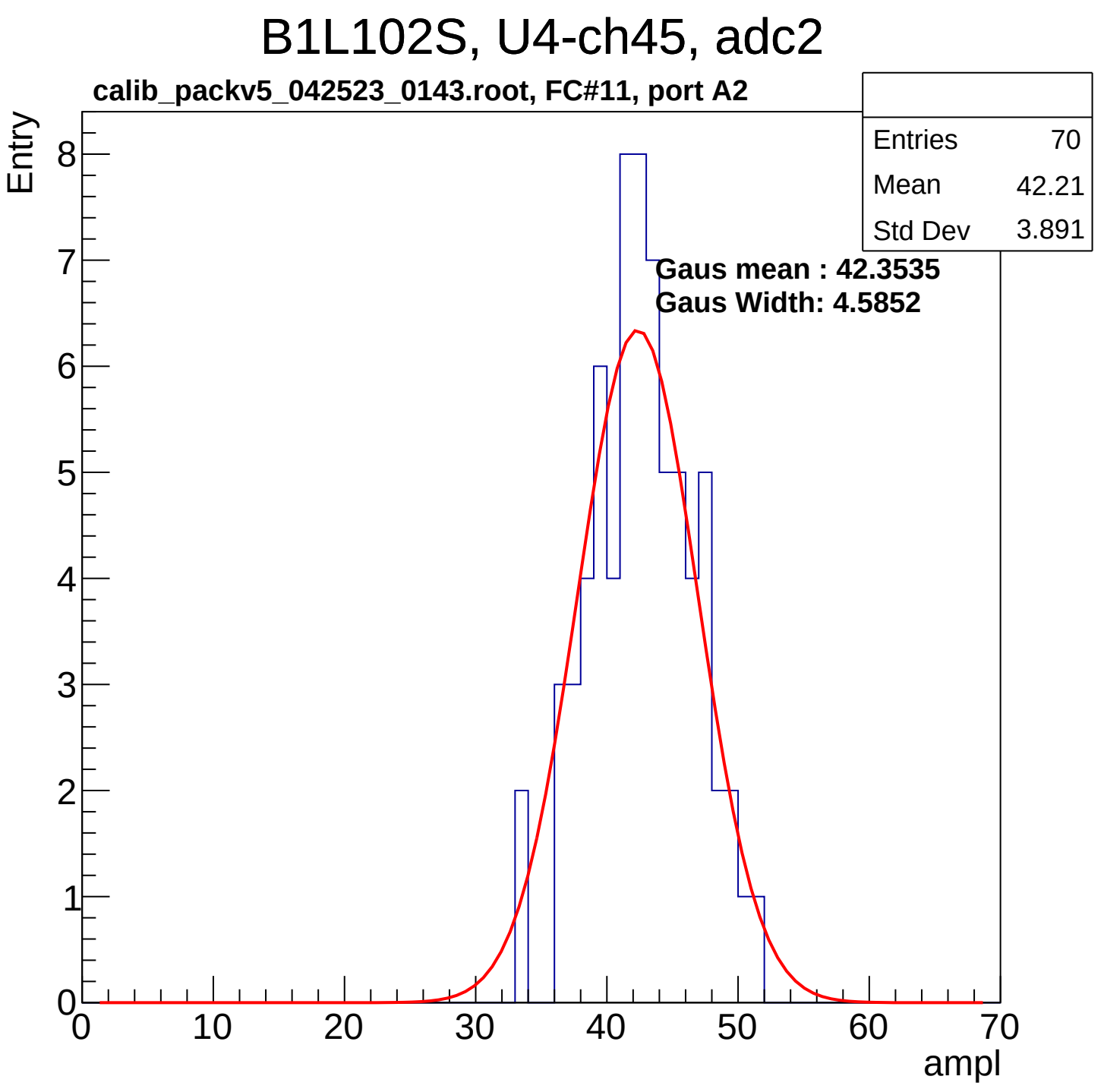
B1L102S, U4-ch45, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 42.21
Std Dev 3.891
Gaus mean : 42.3535
Gaus Width: 4.5852
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
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60
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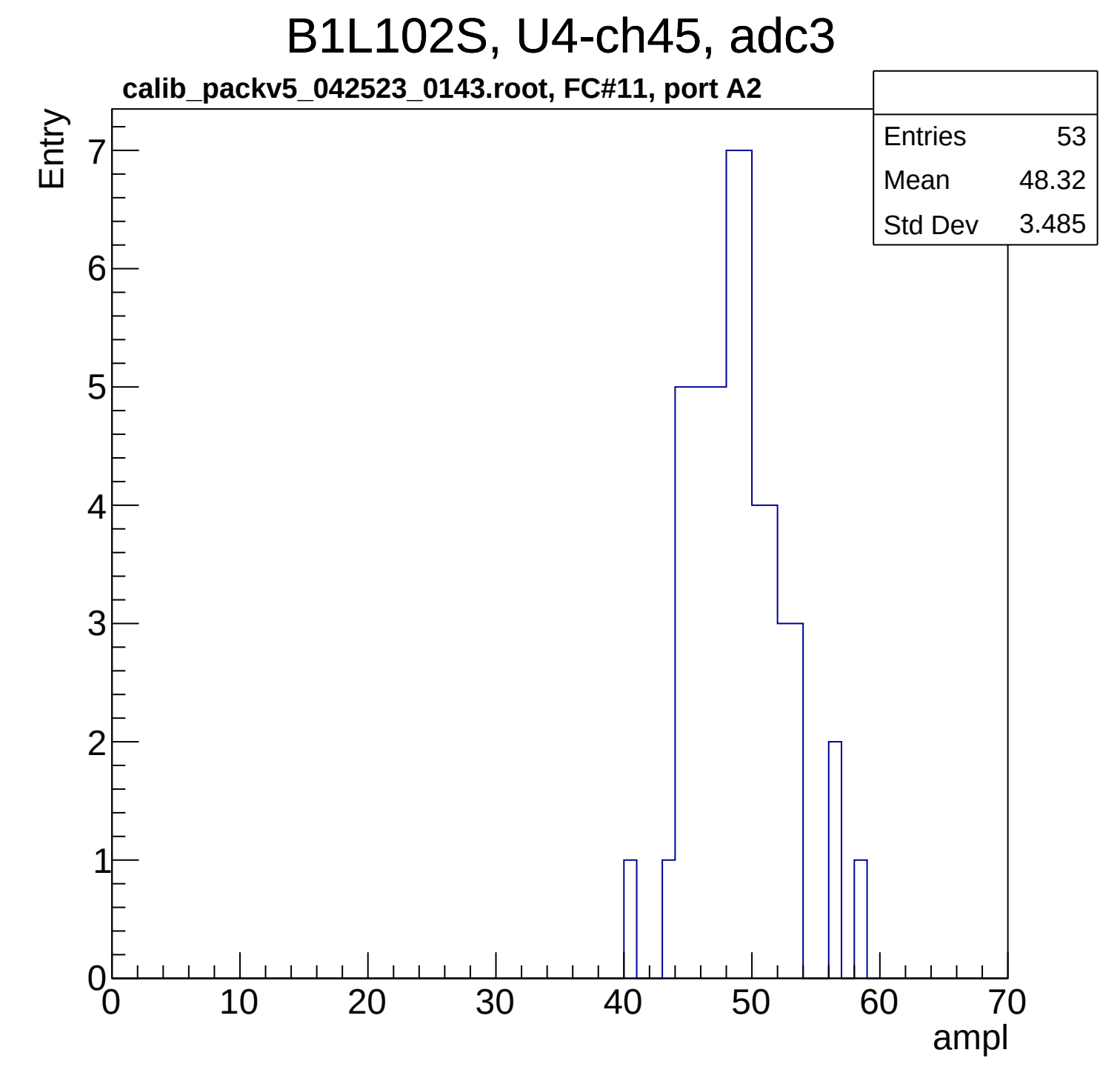
B1L102S, U4-ch45, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 48.32
Std Dev 3.485
Entry
ampl
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4
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0
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20
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60
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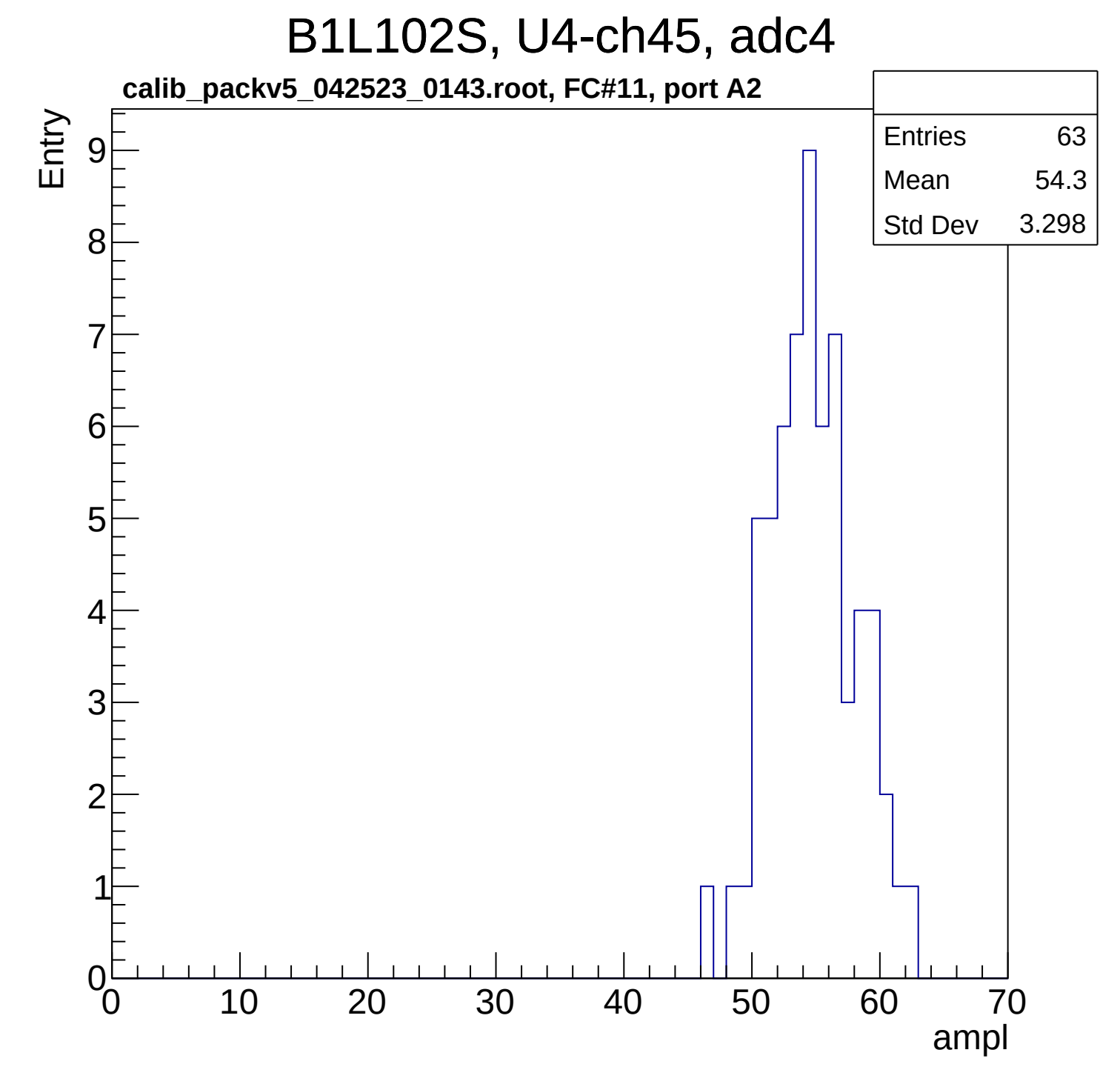
B1L102S, U4-ch45, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 54.3
Std Dev 3.298
Entry
ampl
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3
4
5
6
7
8
9
0
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60
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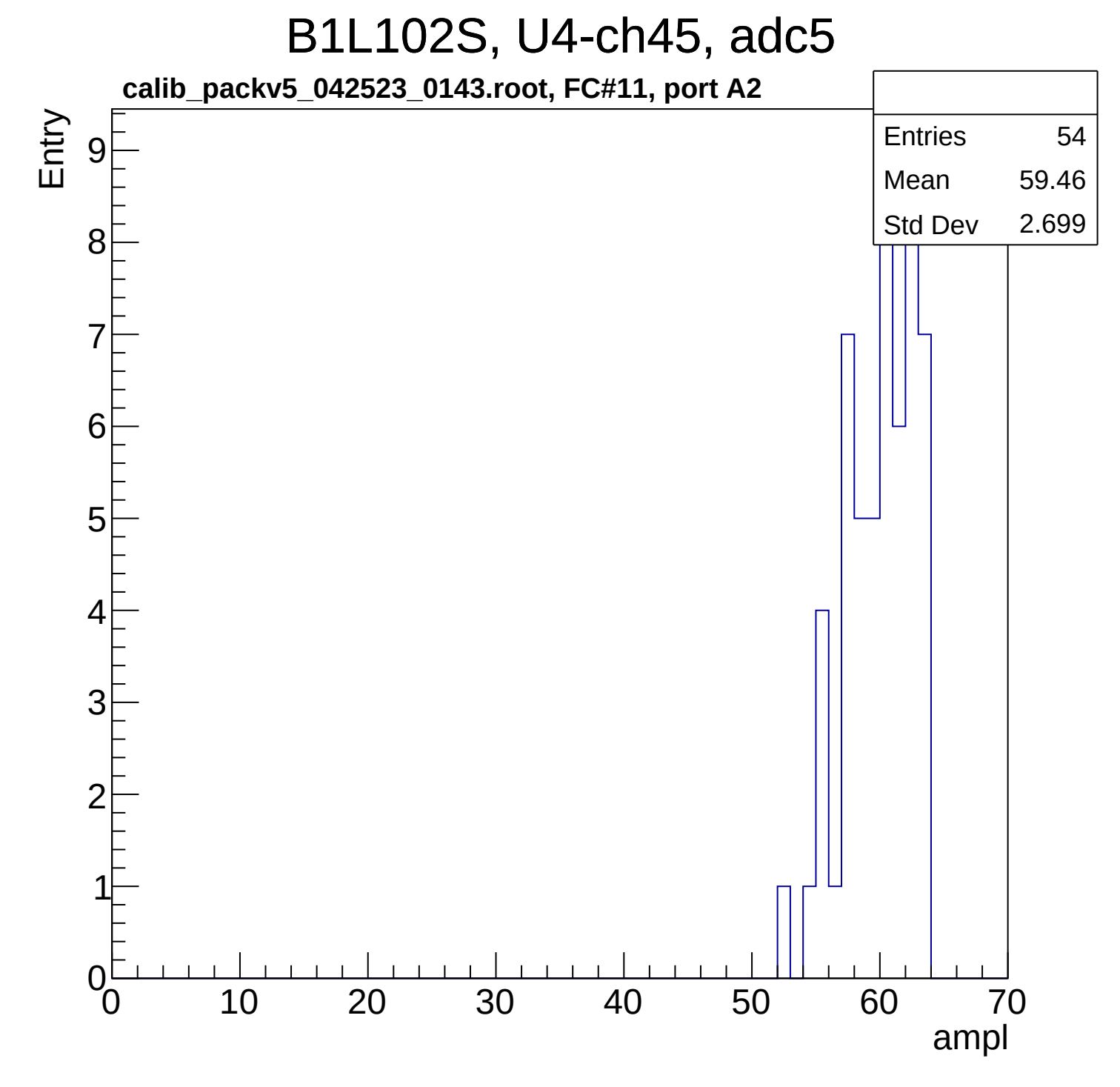
B1L102S, U4-ch45, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 59.46
Std Dev 2.699
Entry
ampl
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2
3
4
5
6
7
8
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0
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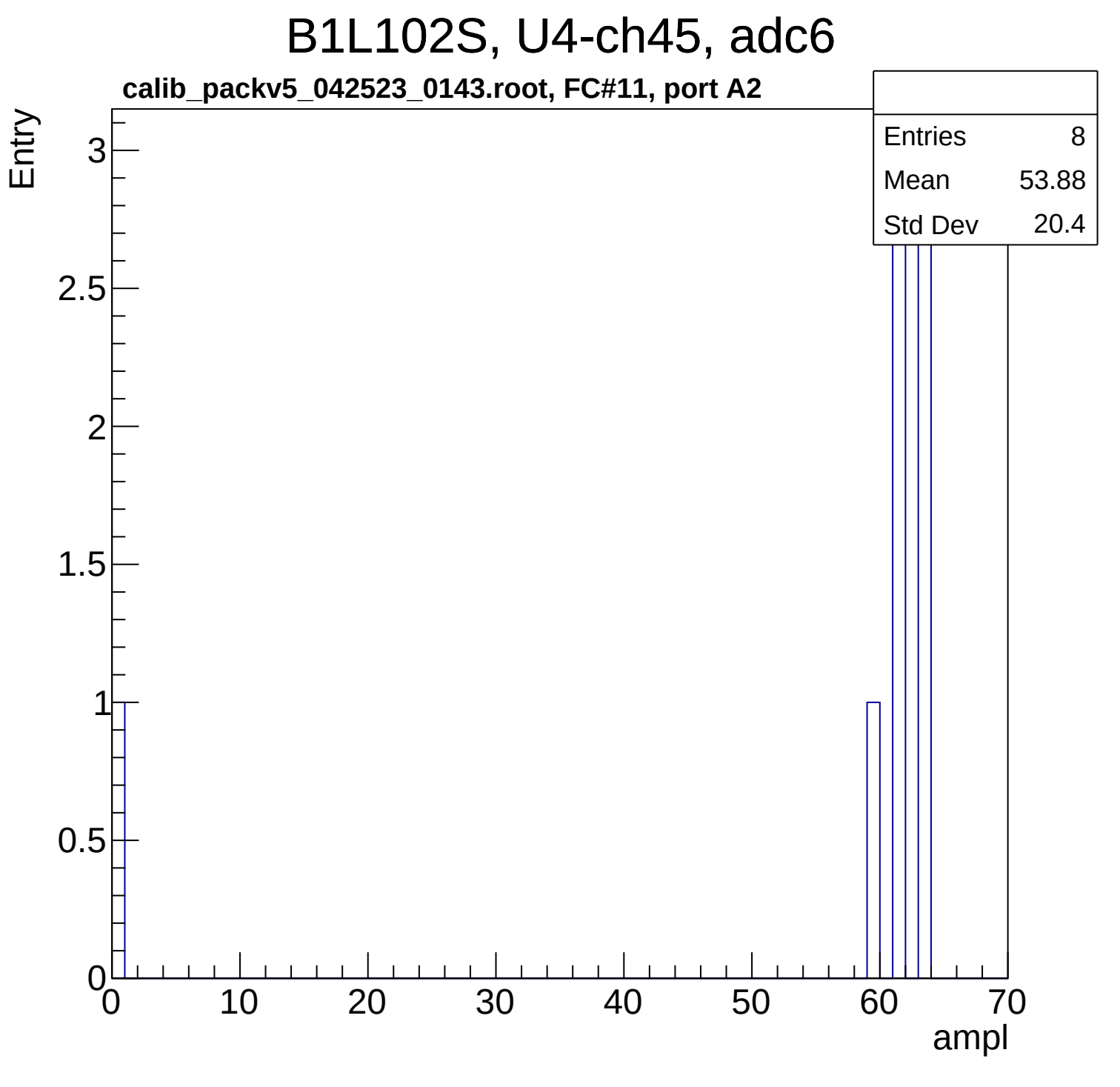
B1L102S, U4-ch45, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 8
Mean 53.88
Std Dev 20.4
Entry
ampl
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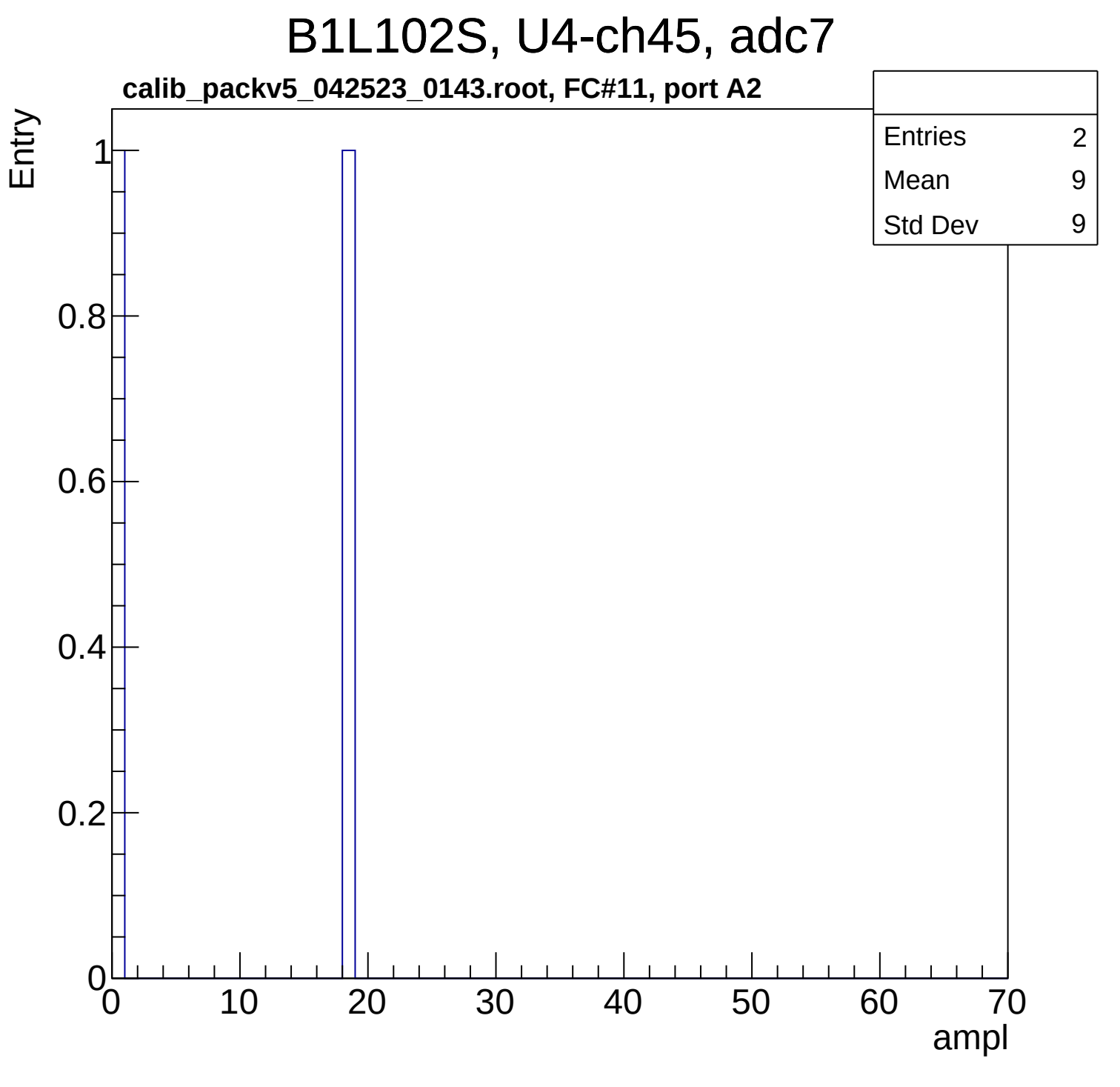
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U4-ch45, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 9
Std Dev 9
Entry
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0.6
0.4
0.2
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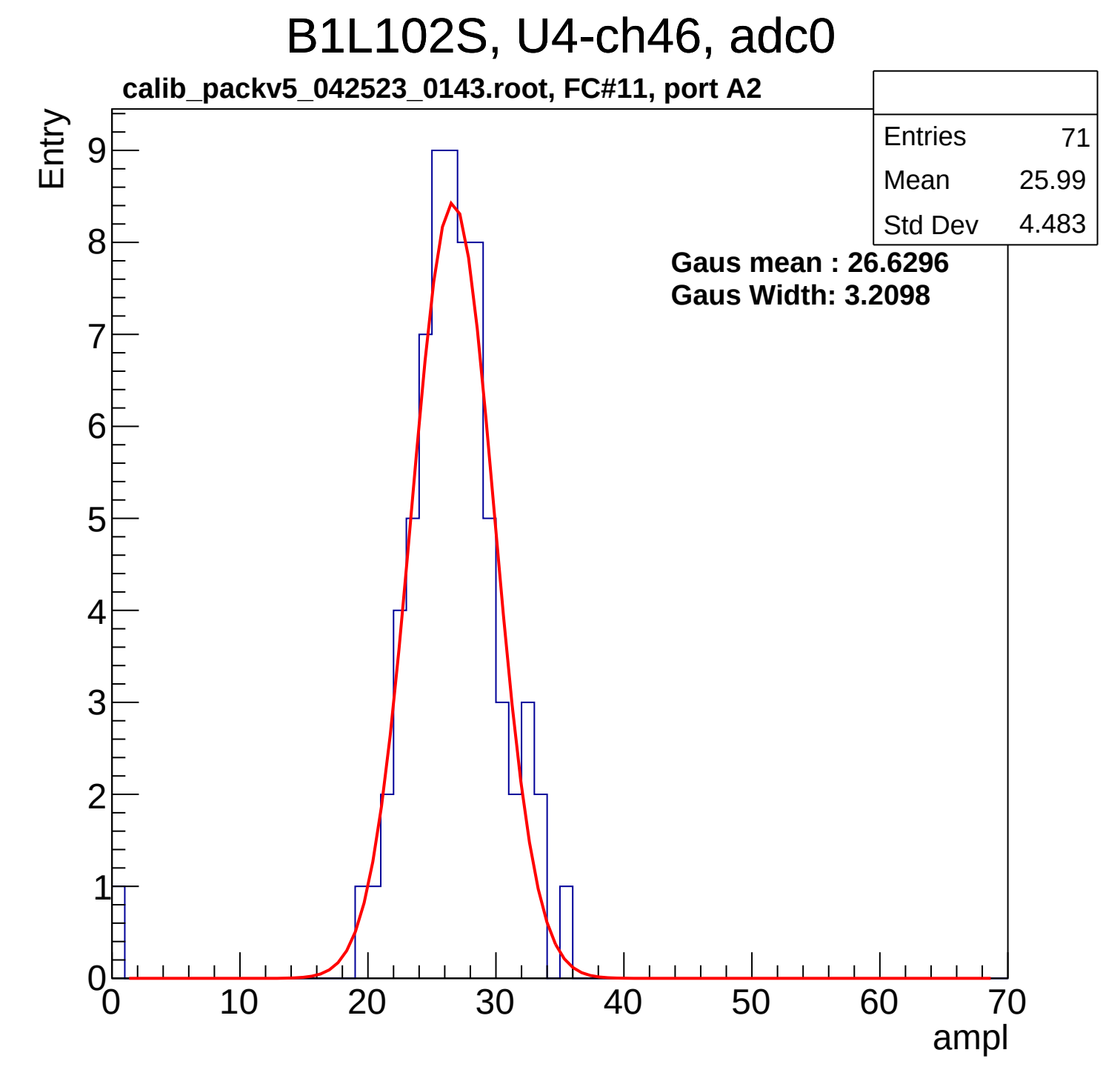
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch46, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 25.99
Std Dev 4.483
Gaus mean : 26.6296
Gaus Width: 3.2098
Entry
ampl
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3
4
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6
7
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0
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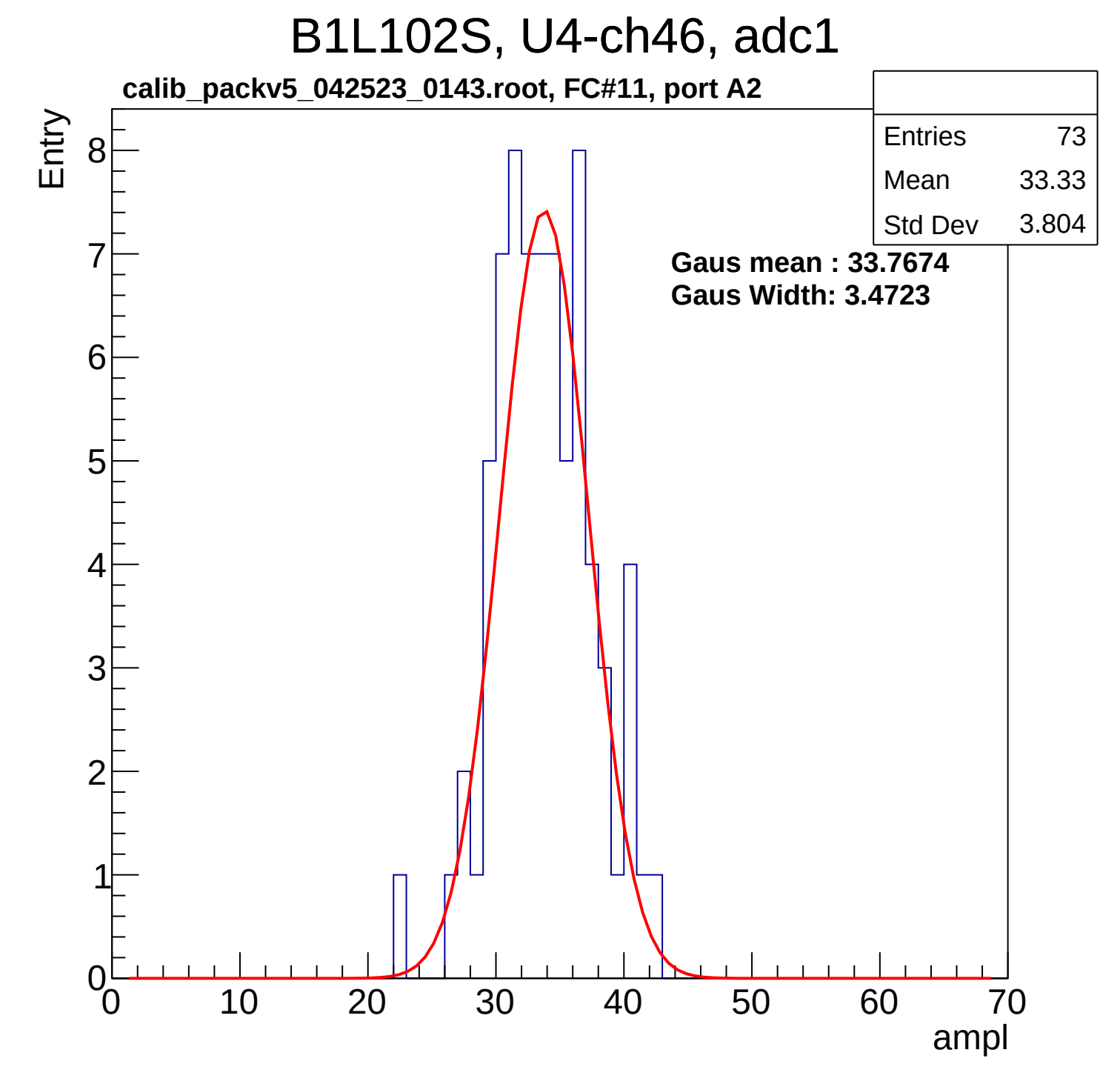
B1L102S, U4-ch46, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 33.33
Std Dev 3.804
Gaus mean : 33.7674
Gaus Width: 3.4723
Entry
ampl
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2
3
4
5
6
7
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0
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40
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60
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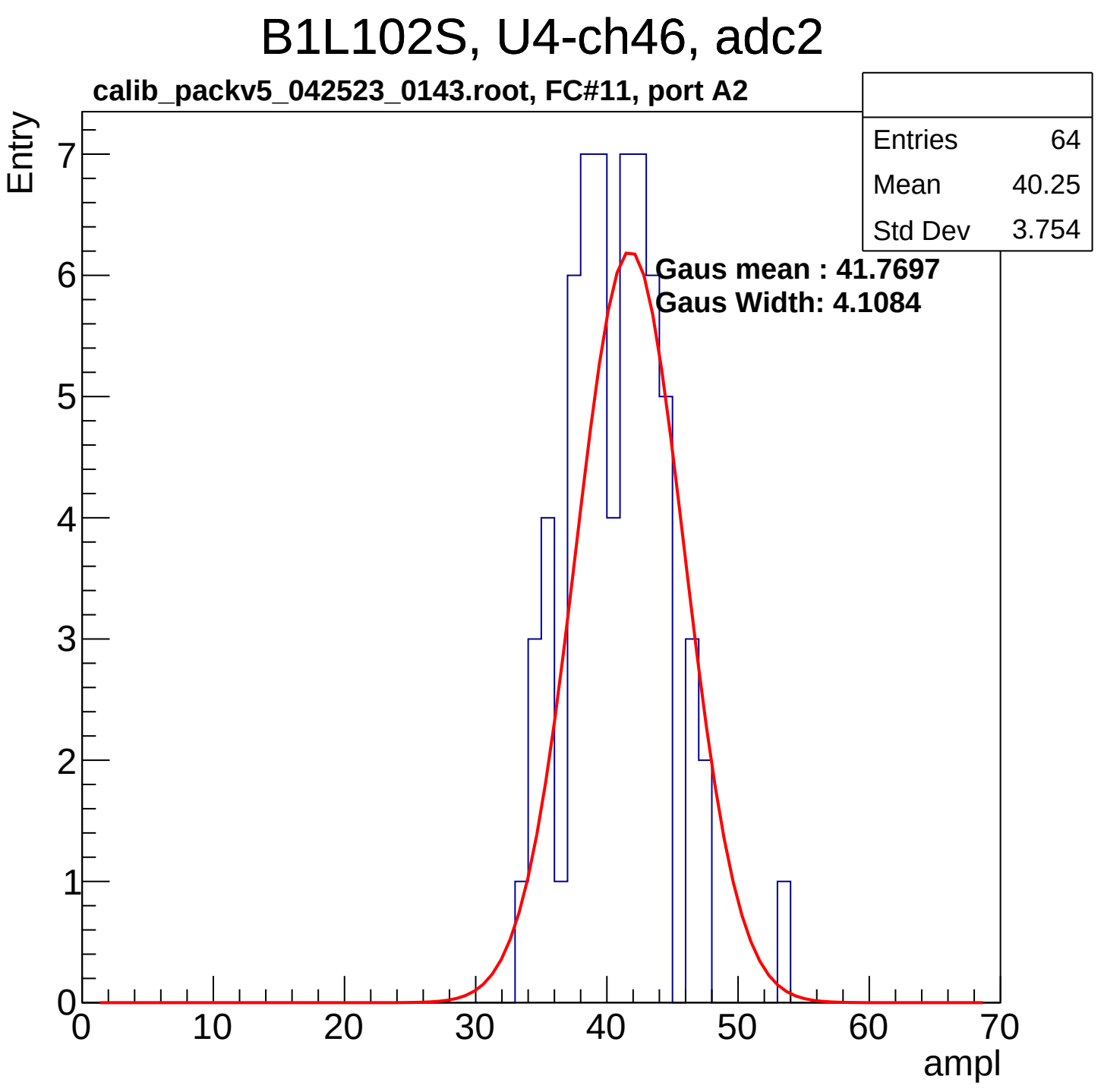
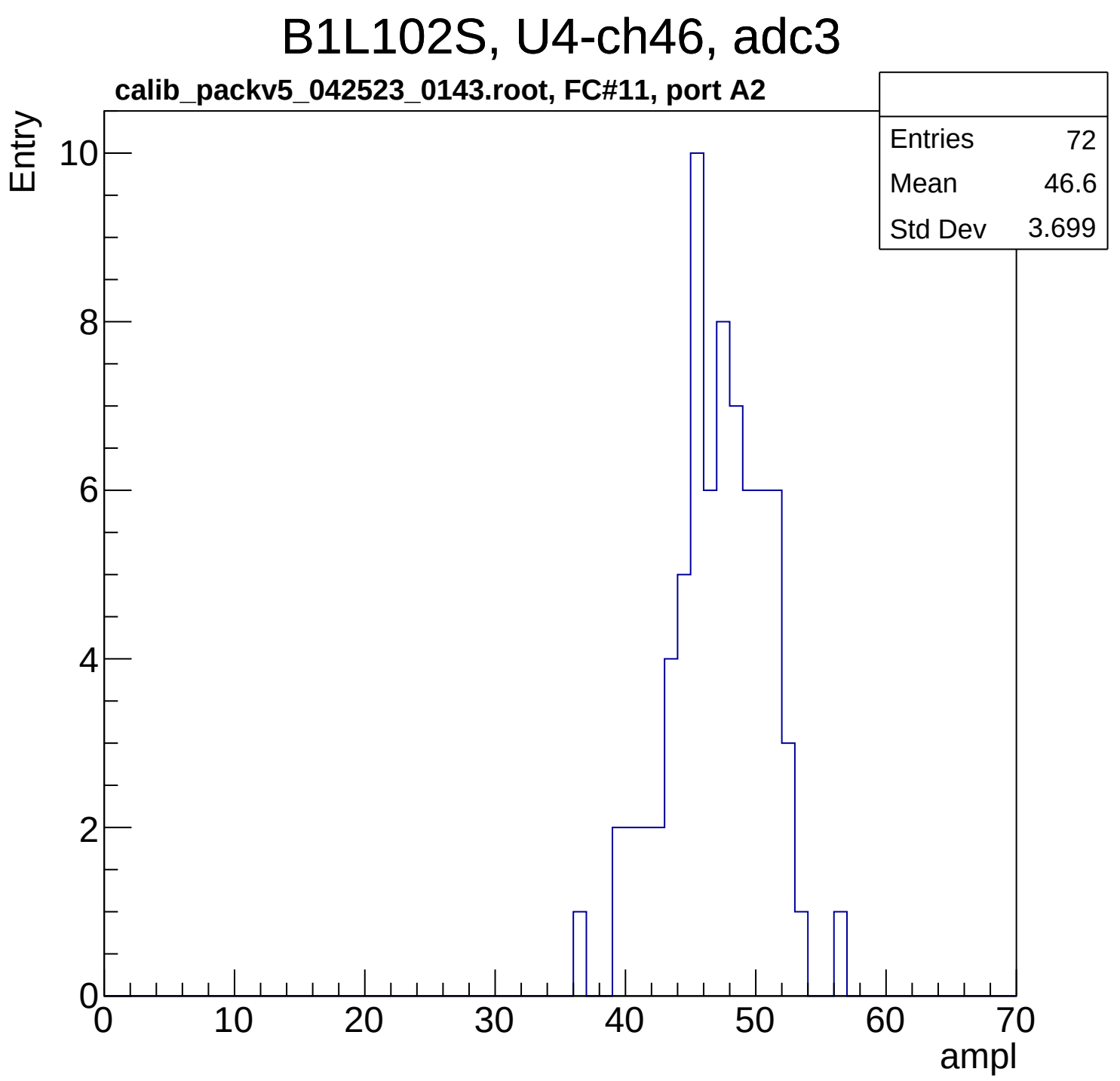
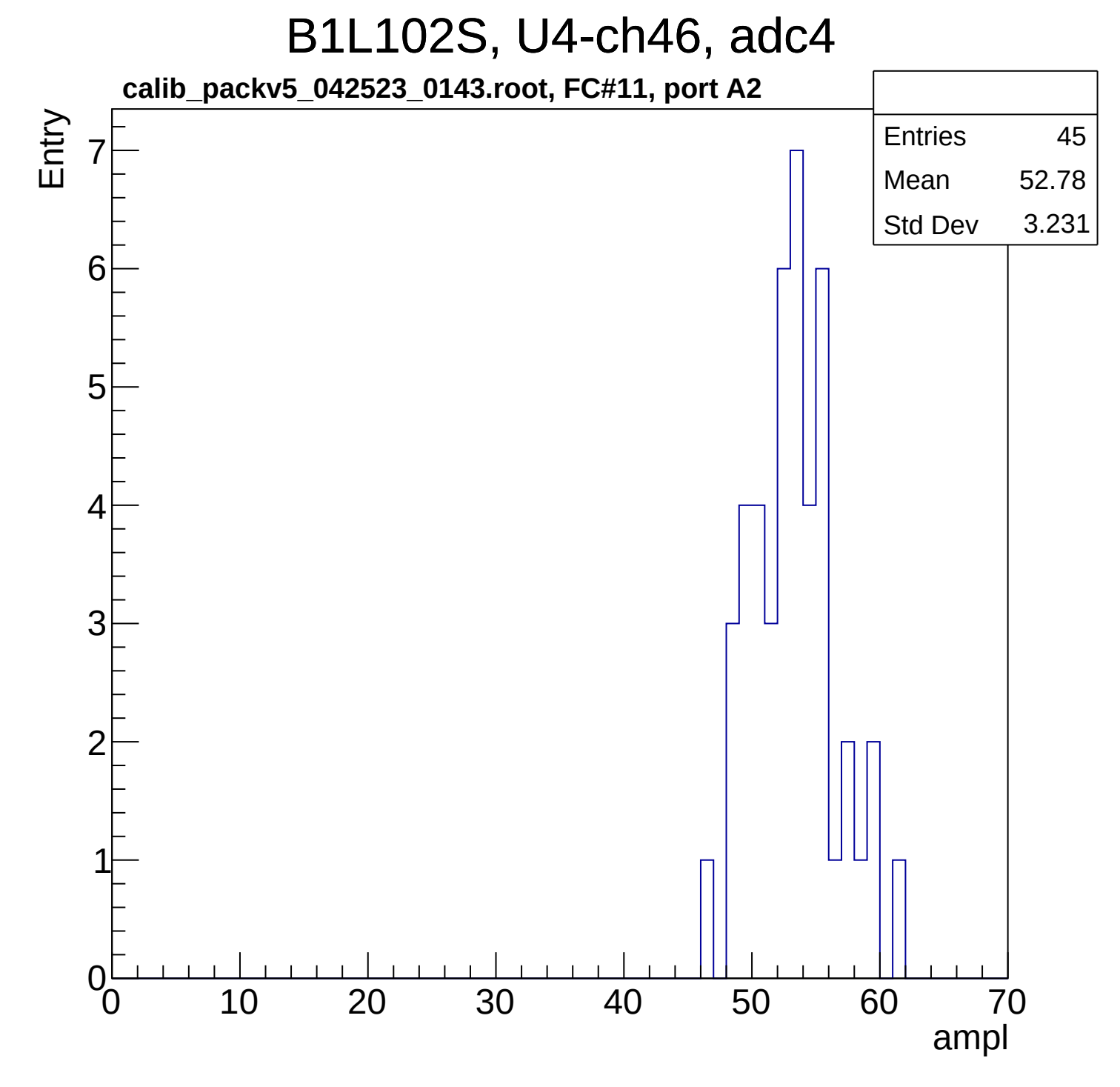
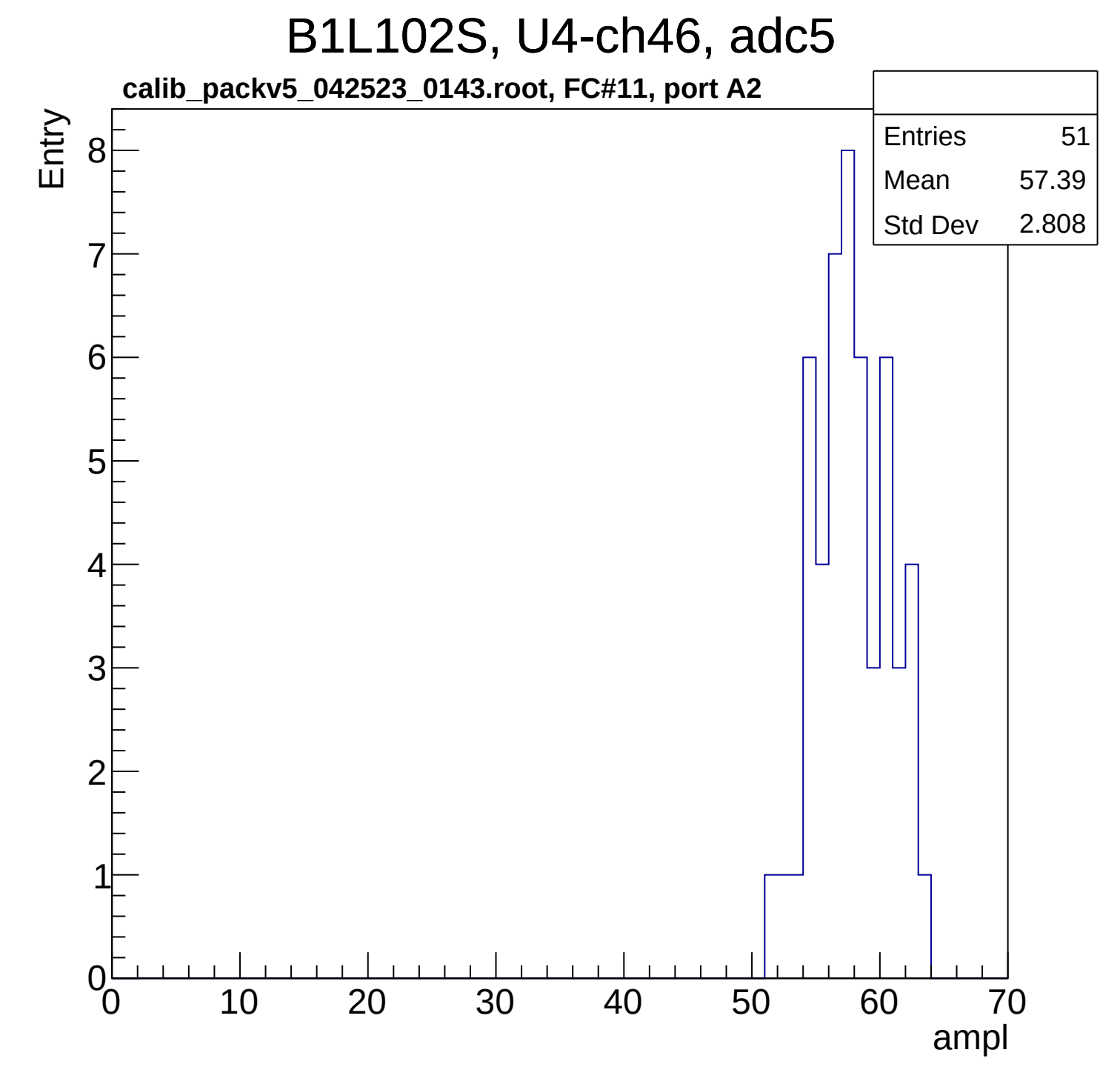
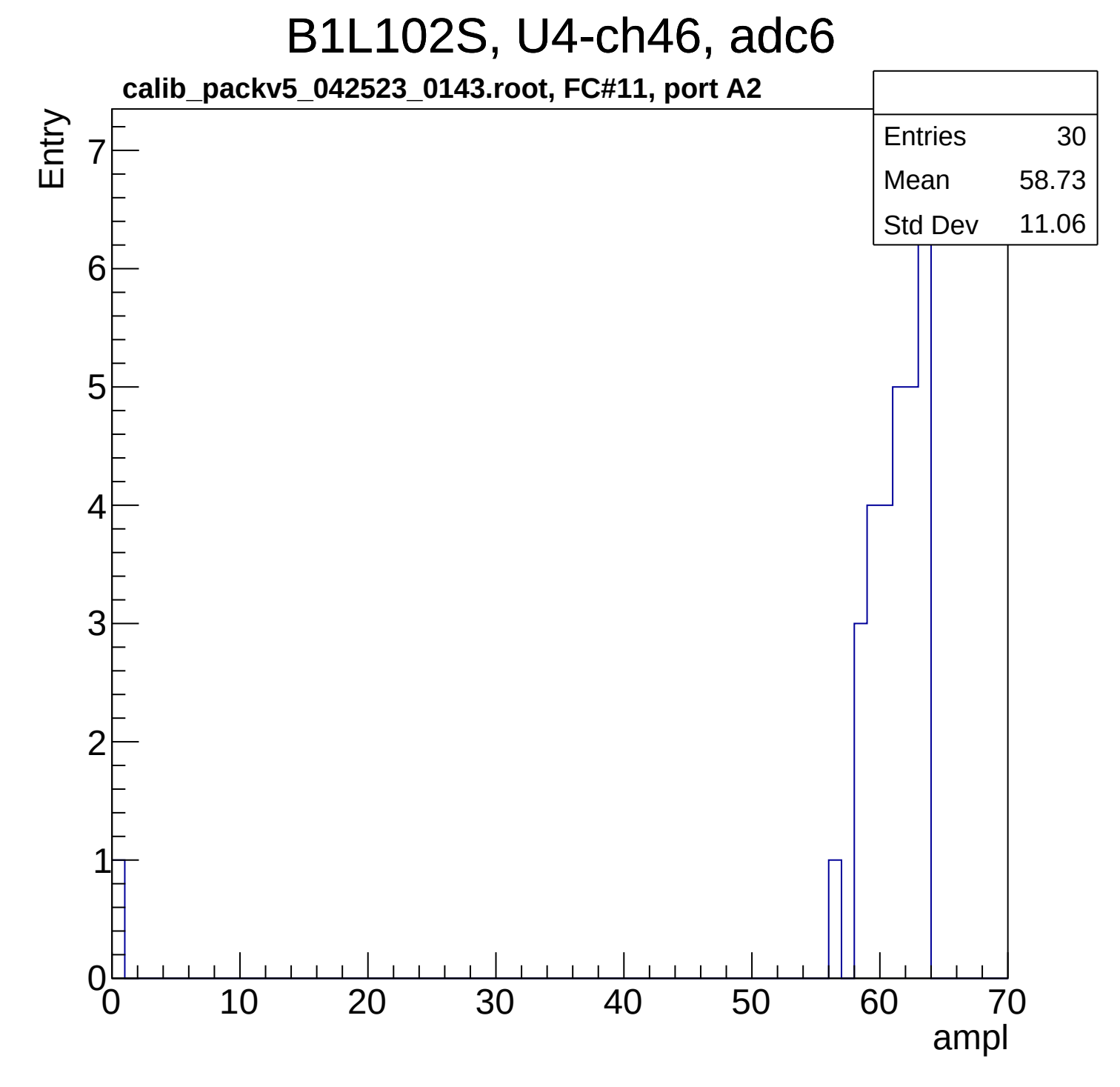
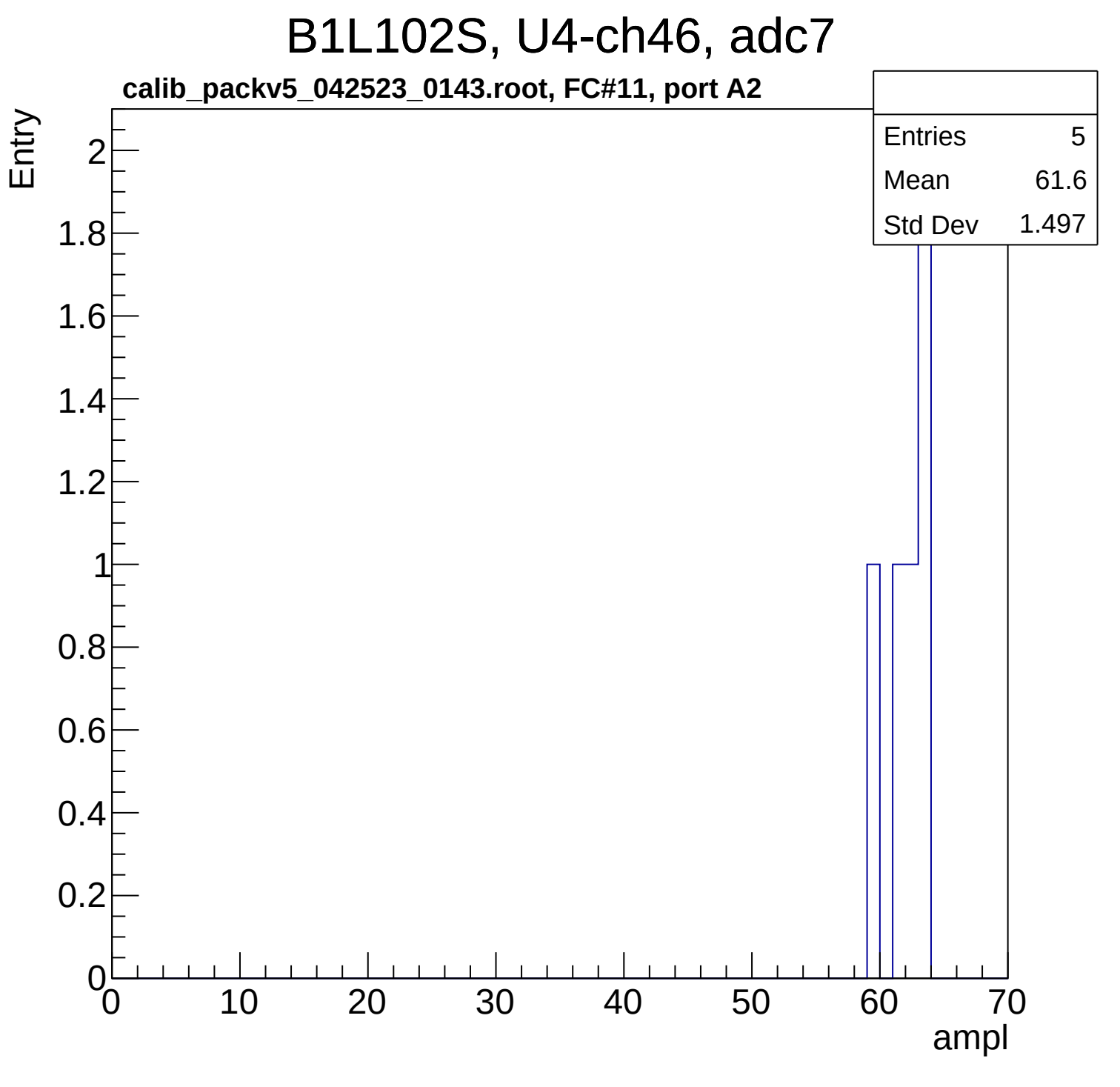

B1L102S, U4-ch46, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 40.25
Std Dev 3.754
Gaus mean : 41.7697
Gaus Width: 4.1084
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch46, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 72
Mean 46.6
Std Dev 3.699
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch46, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 45
Mean 52.78
Std Dev 3.231
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch46, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 57.39
Std Dev 2.808
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch46, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 30
Mean 58.73
Std Dev 11.06
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch46, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 5
Mean 61.6
Std Dev 1.497
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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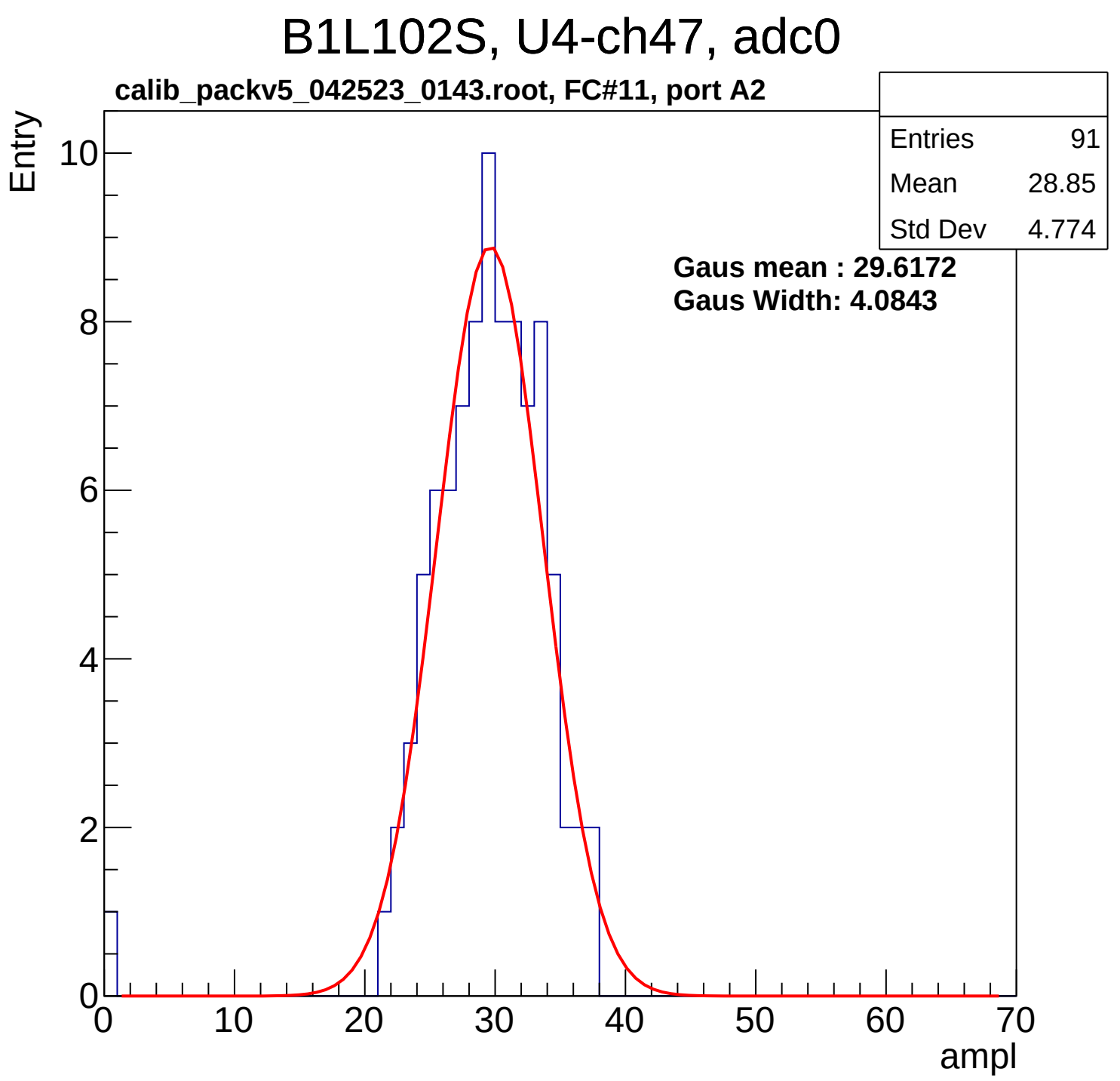
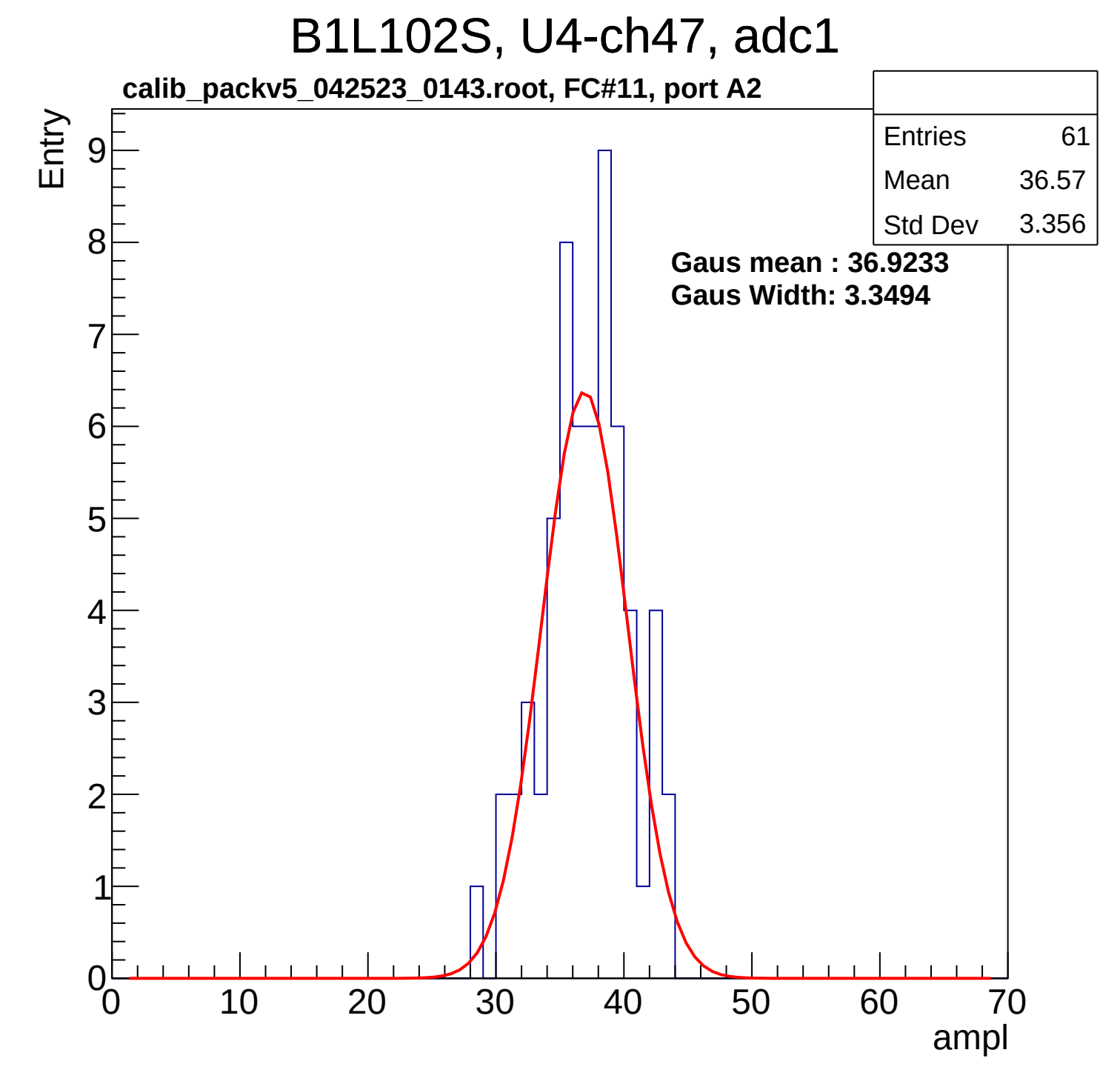

B1L102S, U4-ch47, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 91
Mean 28.85
Std Dev 4.774
Gaus mean : 29.6172
Gaus Width: 4.0843
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch47, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 36.57
Std Dev 3.356
Gaus mean : 36.9233
Gaus Width: 3.3494
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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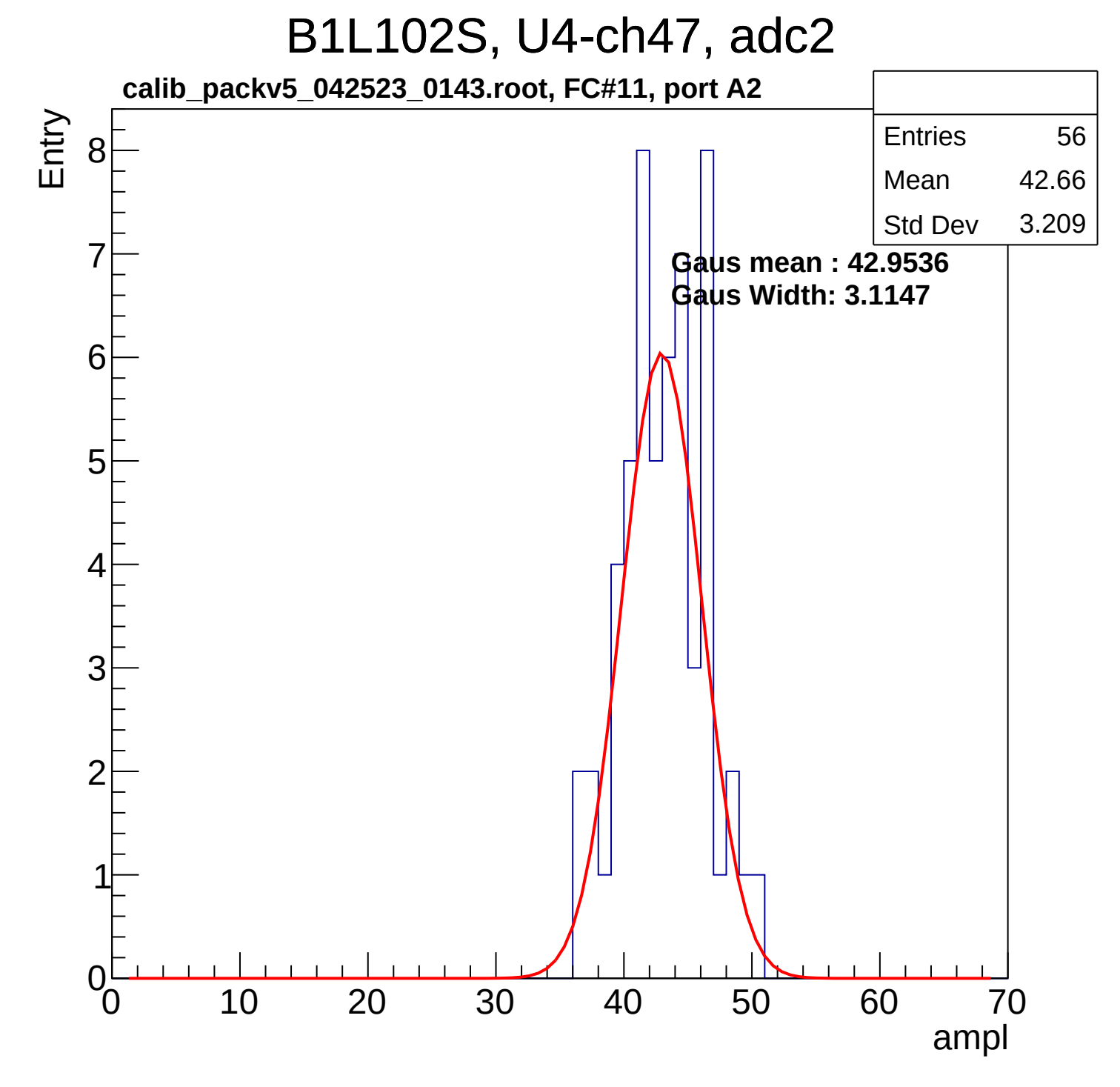
B1L102S, U4-ch47, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 42.66
Std Dev 3.209
Gaus mean : 42.9536
Gaus Width: 3.1147
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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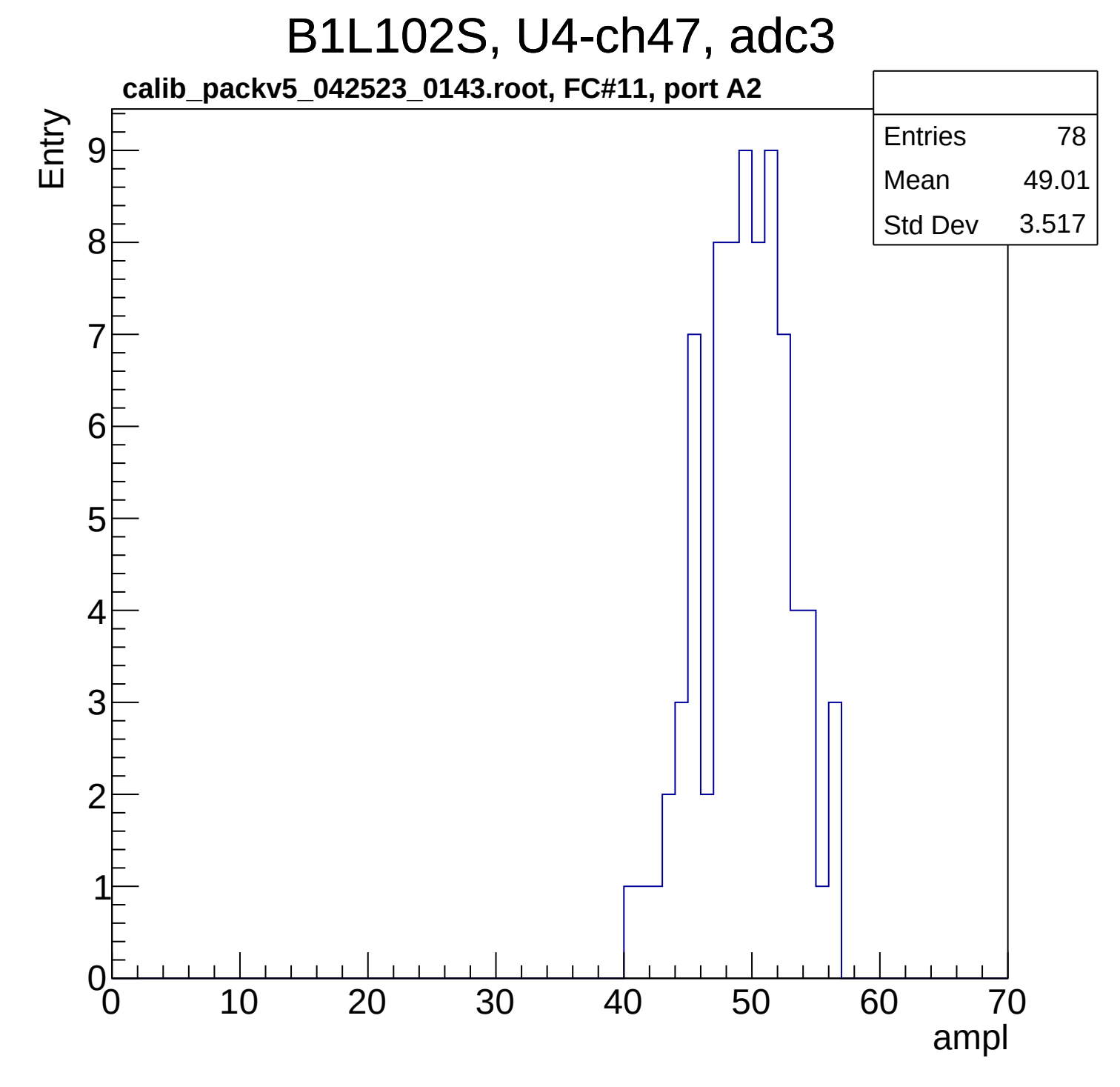
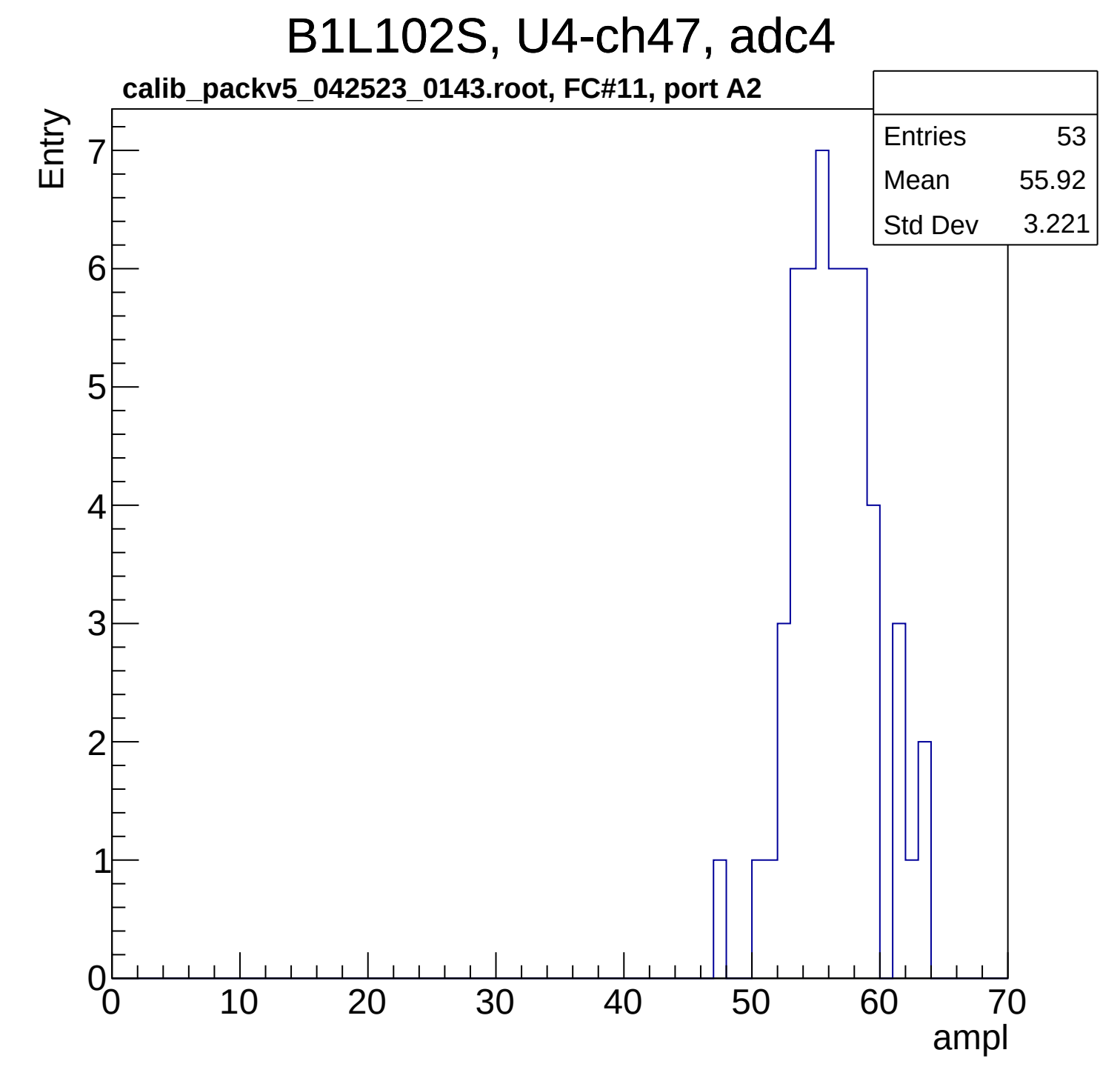
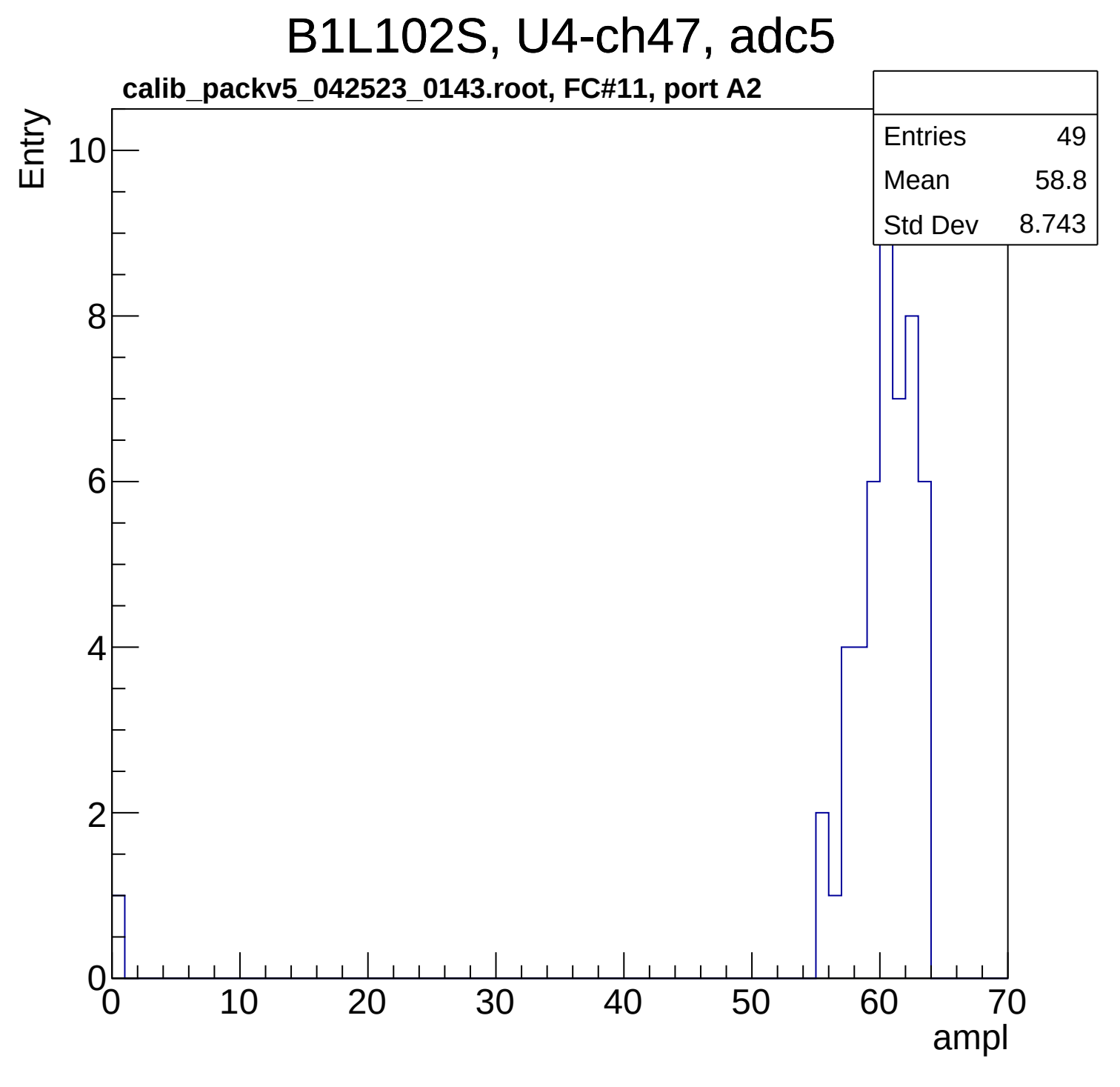
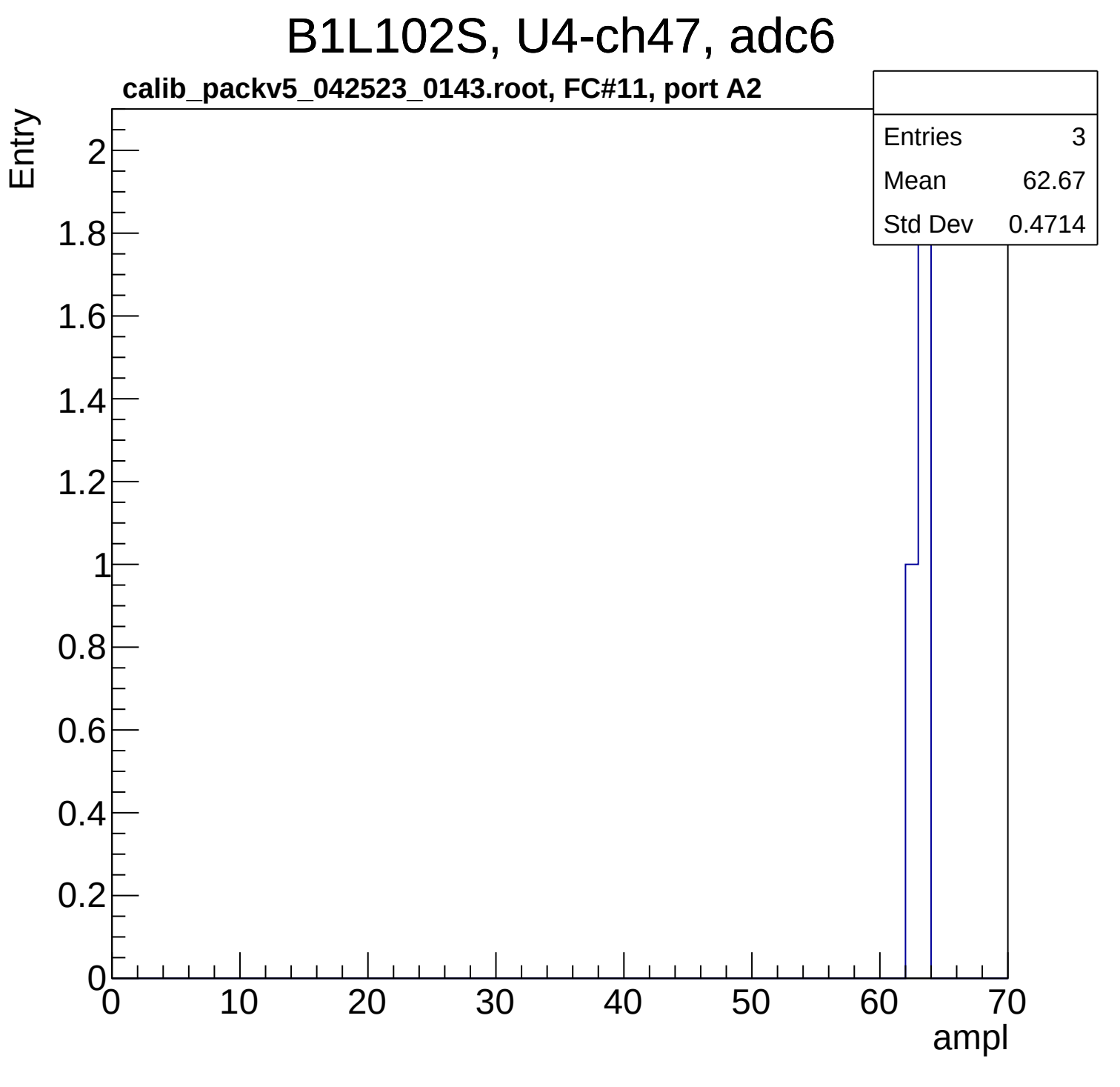
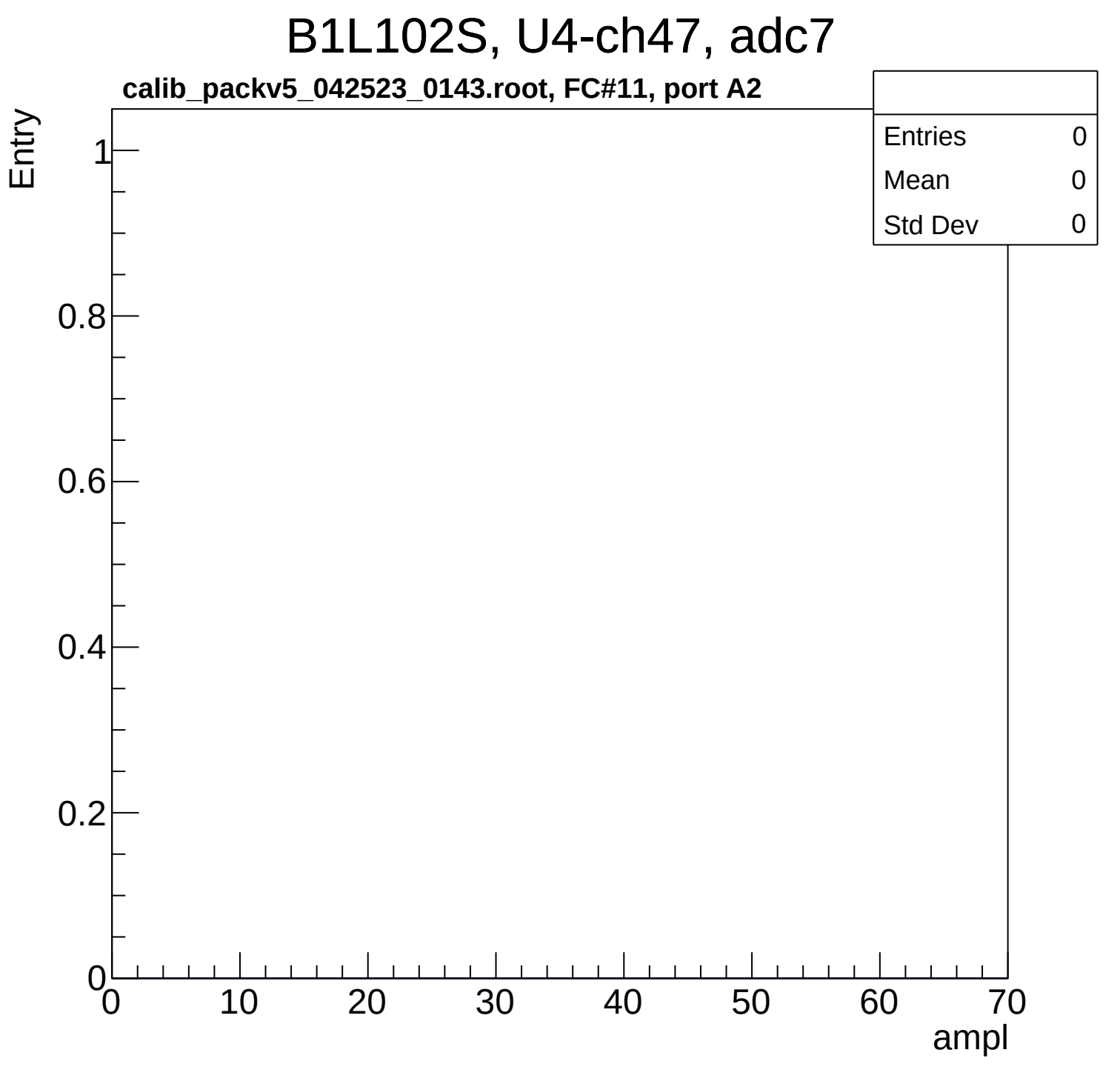
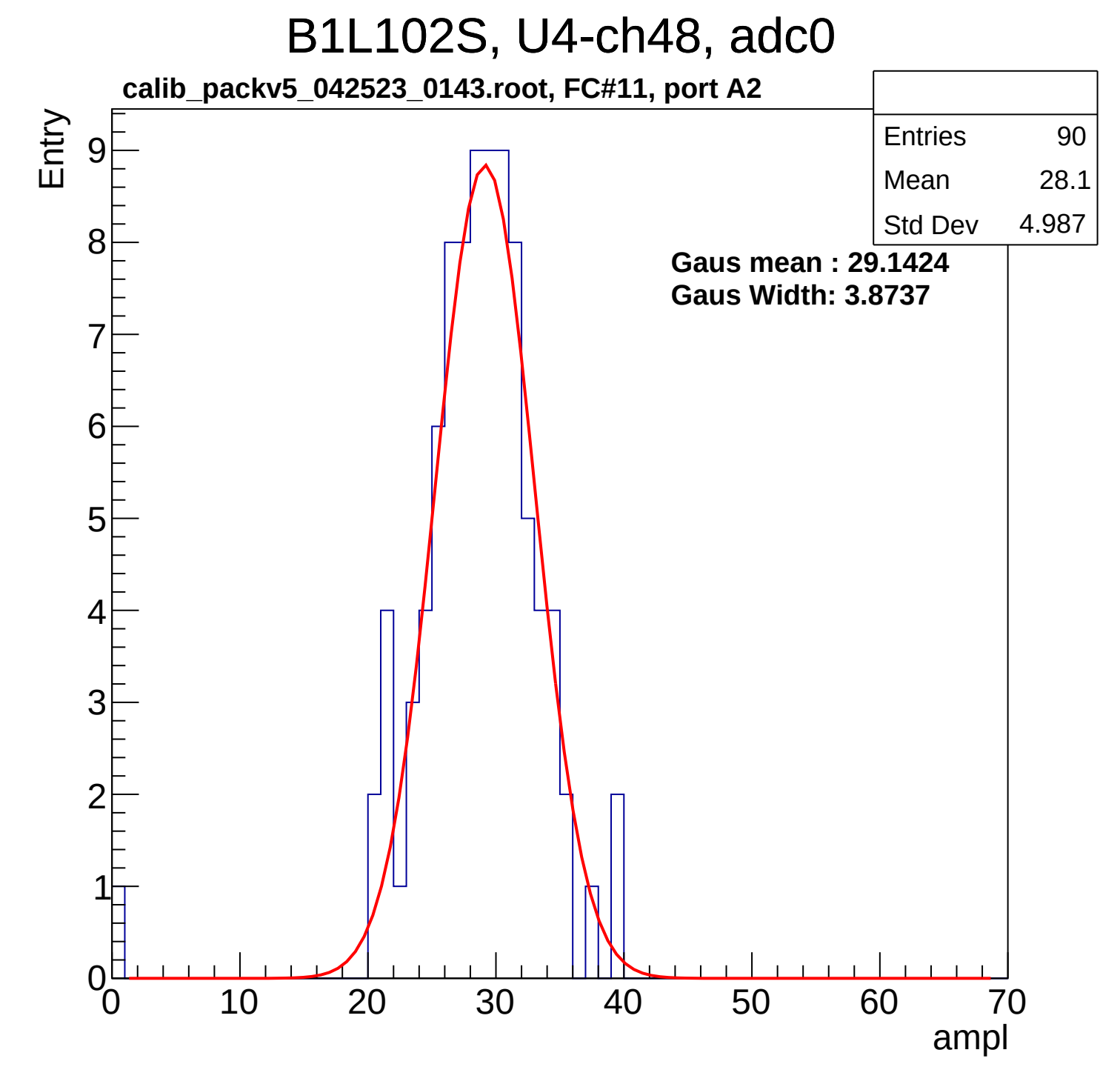

B1L102S, U4-ch47, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 78
Mean 49.01
Std Dev 3.517
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

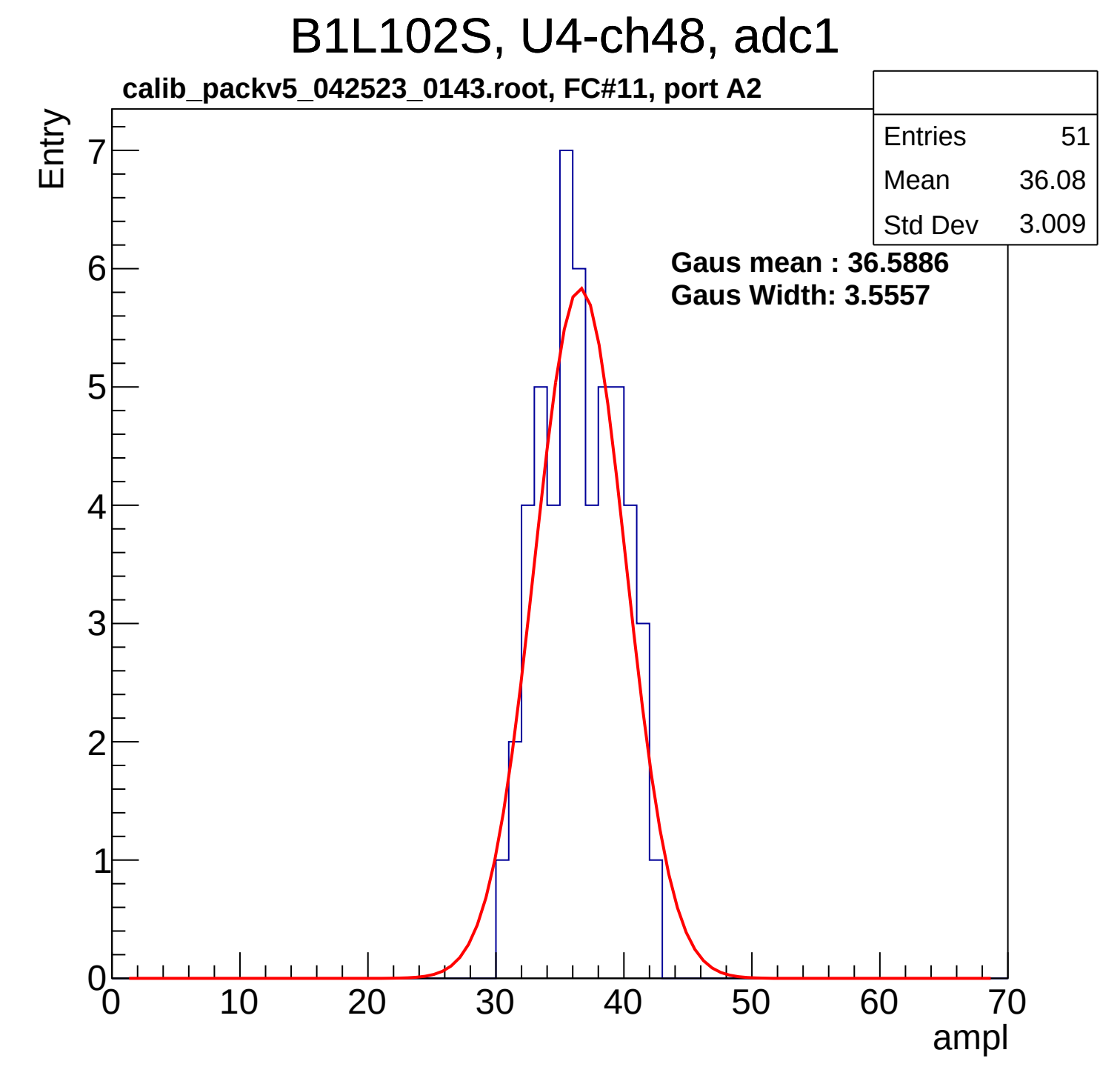

B1L102S, U4-ch47, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 55.92
Std Dev 3.221
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

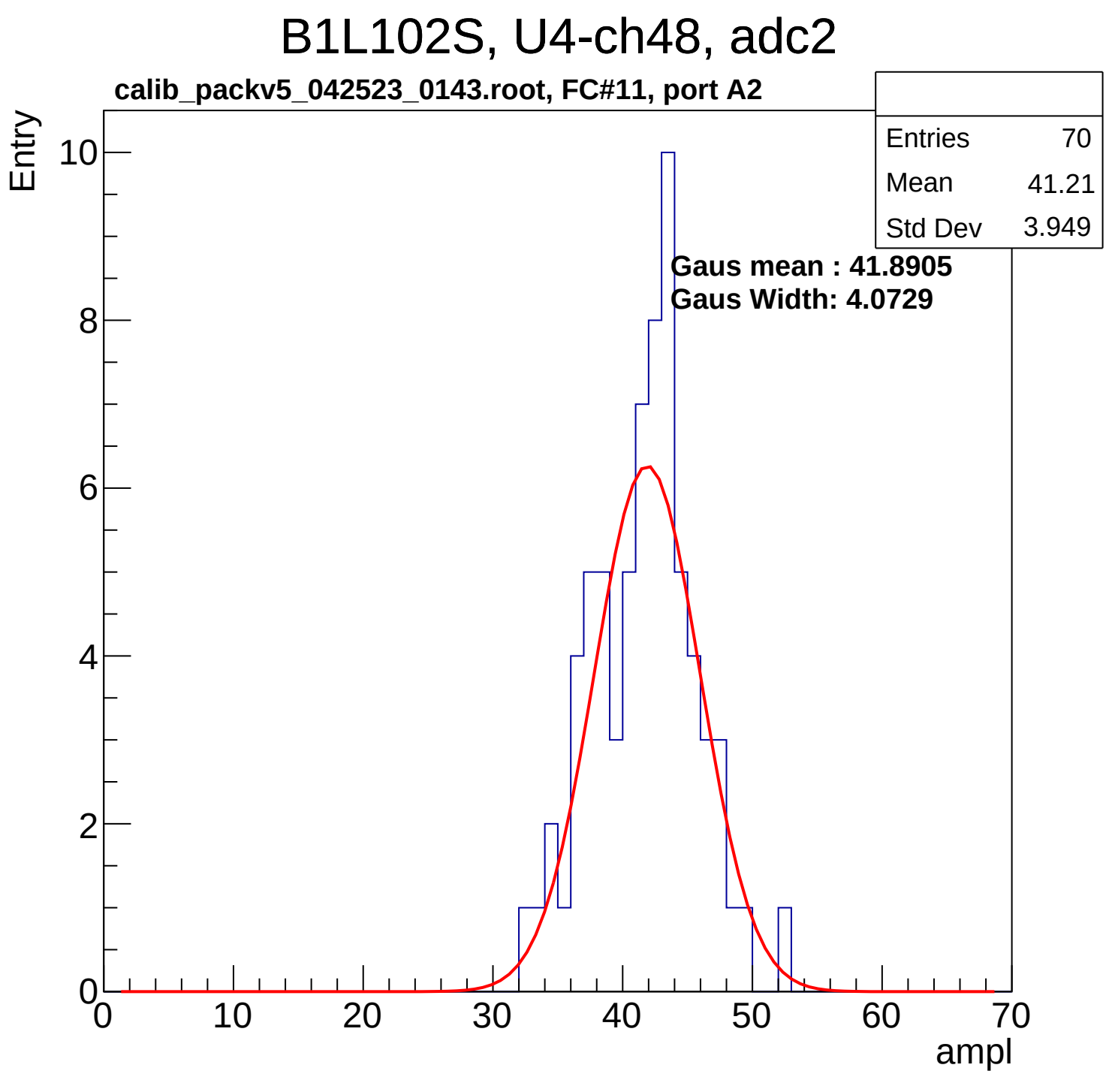

B1L102S, U4-ch47, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 58.8
Std Dev 8.743
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

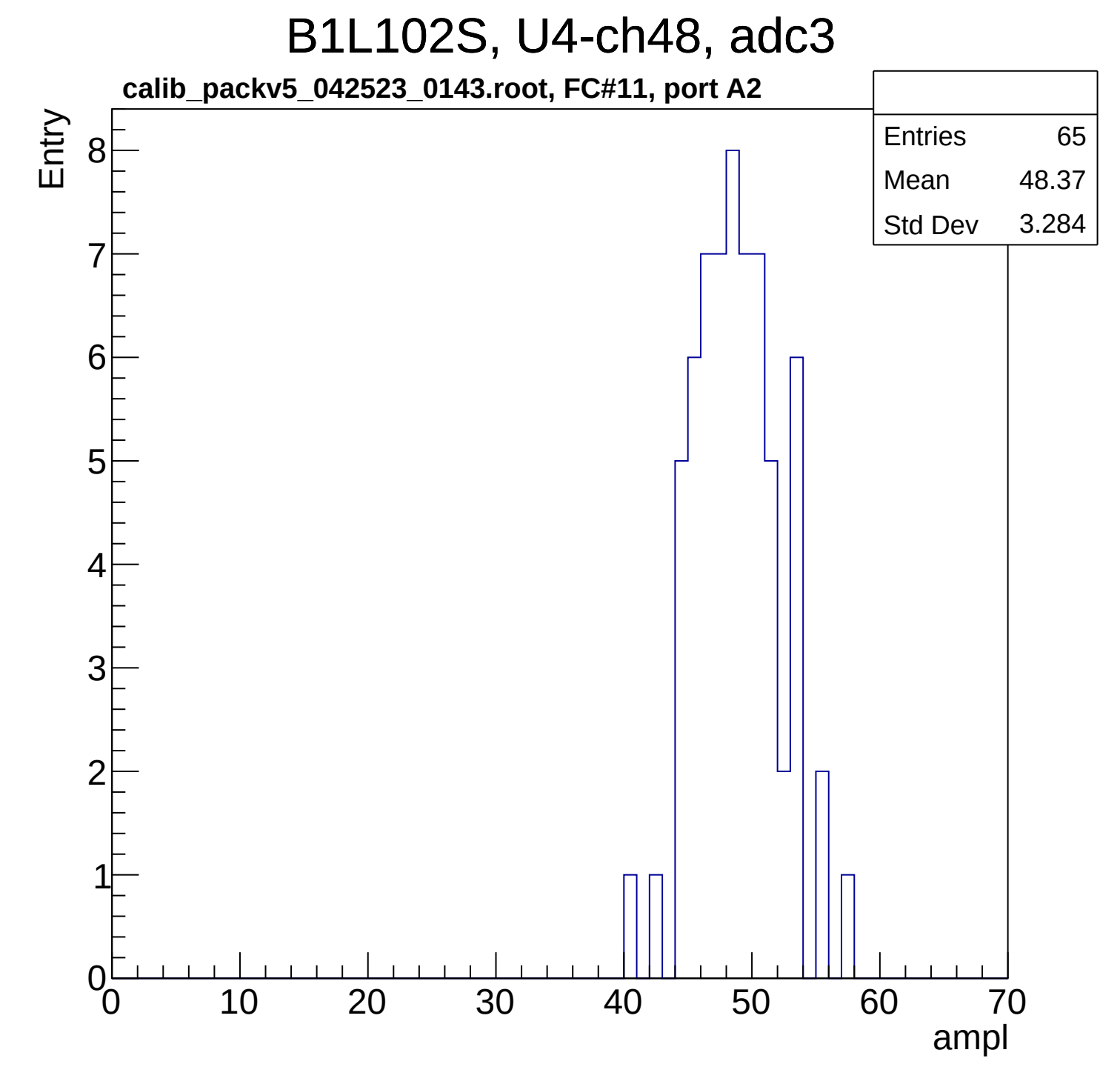

B1L102S, U4-ch47, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

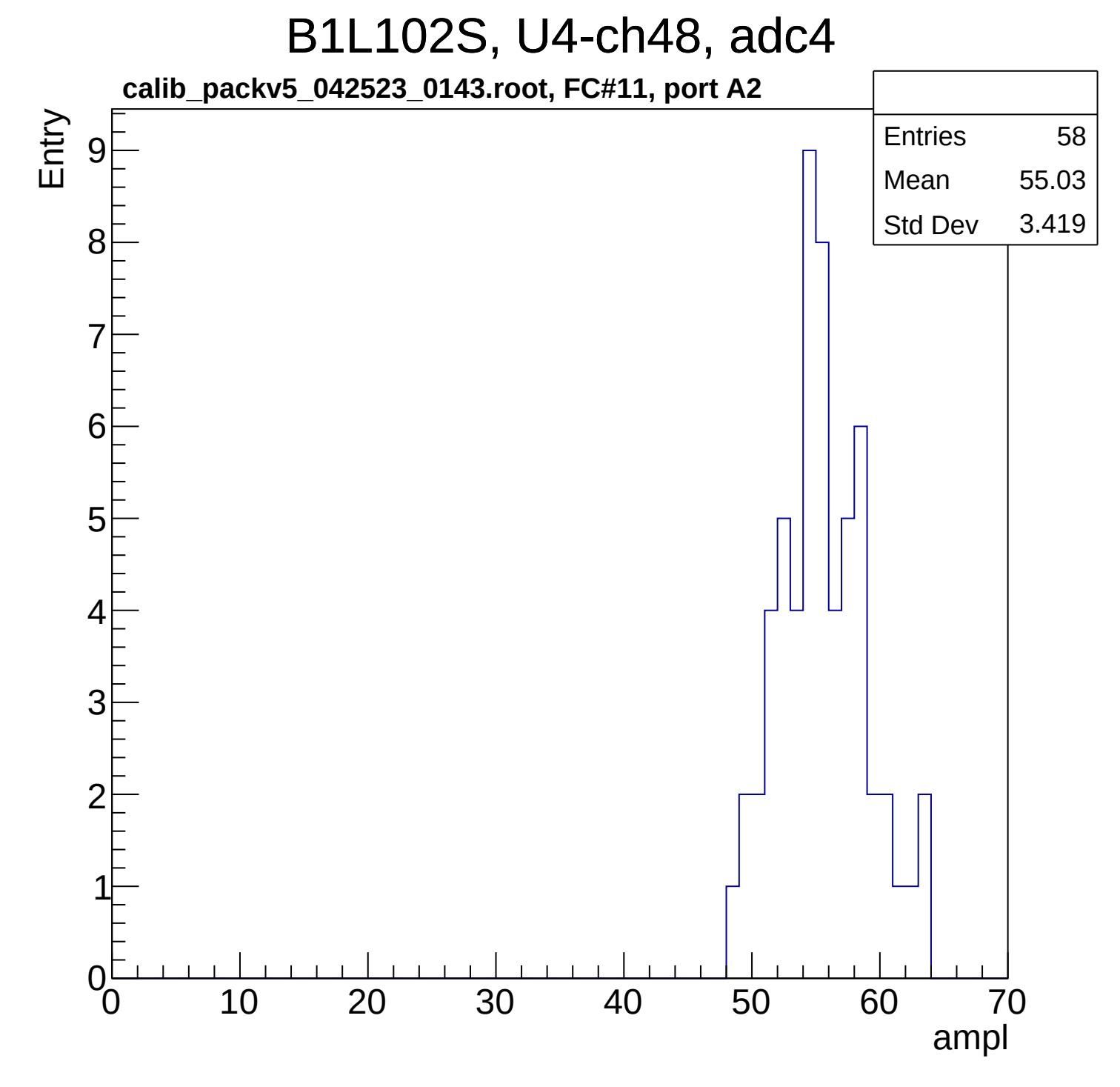

B1L102S, U4-ch47, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

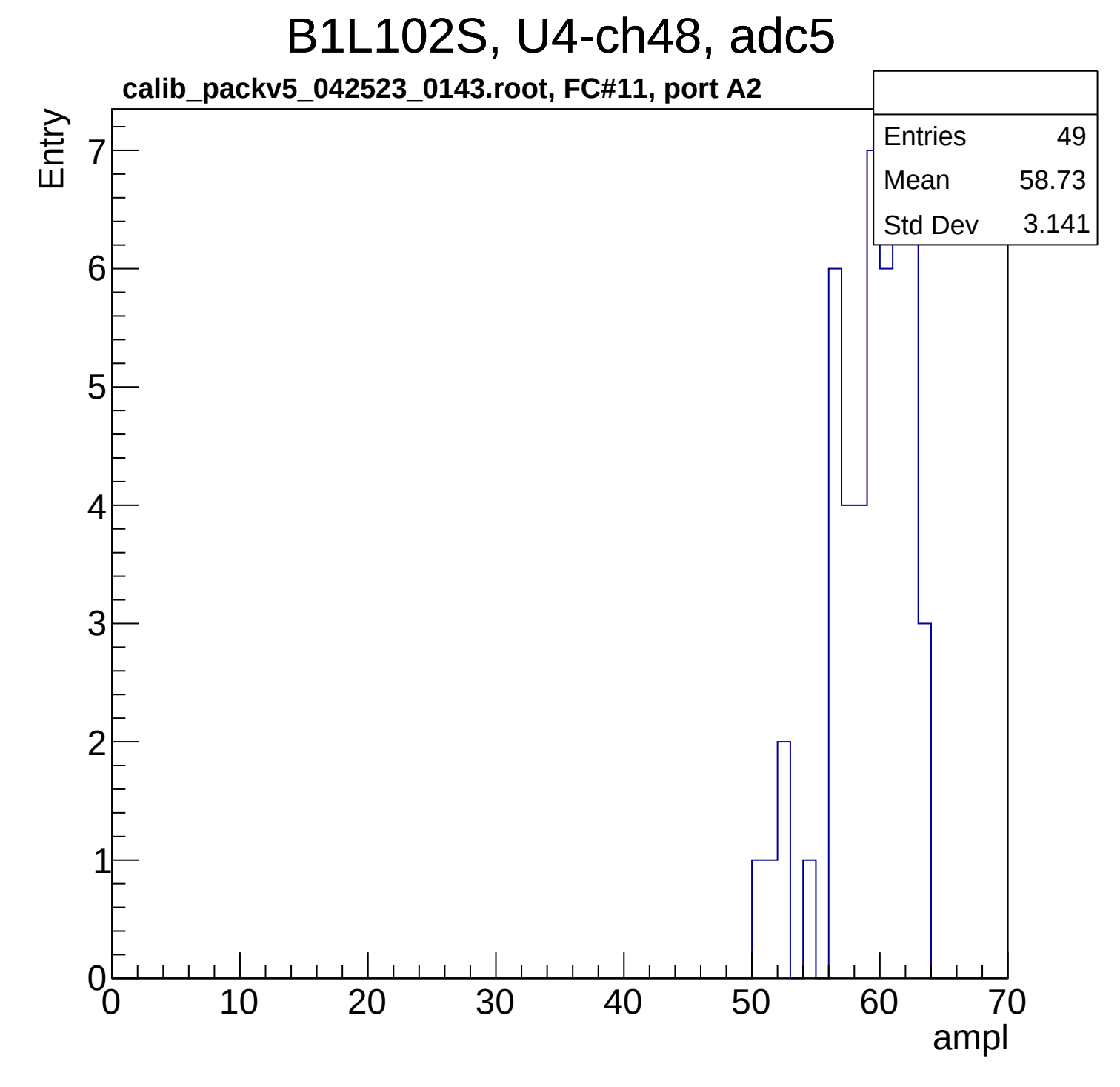

B1L102S, U4-ch48, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 90
Mean 28.1
Std Dev 4.987
Gaus mean : 29.1424
Gaus Width: 3.8737
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L102S, U4-ch48, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 36.08
Std Dev 3.009
Gaus mean : 36.5886
Gaus Width: 3.5557
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch48, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 41.21
Std Dev 3.949
Gaus mean : 41.8905
Gaus Width: 4.0729
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch48, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 48.37
Std Dev 3.284
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch48, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 55.03
Std Dev 3.419
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch48, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 58.73
Std Dev 3.141
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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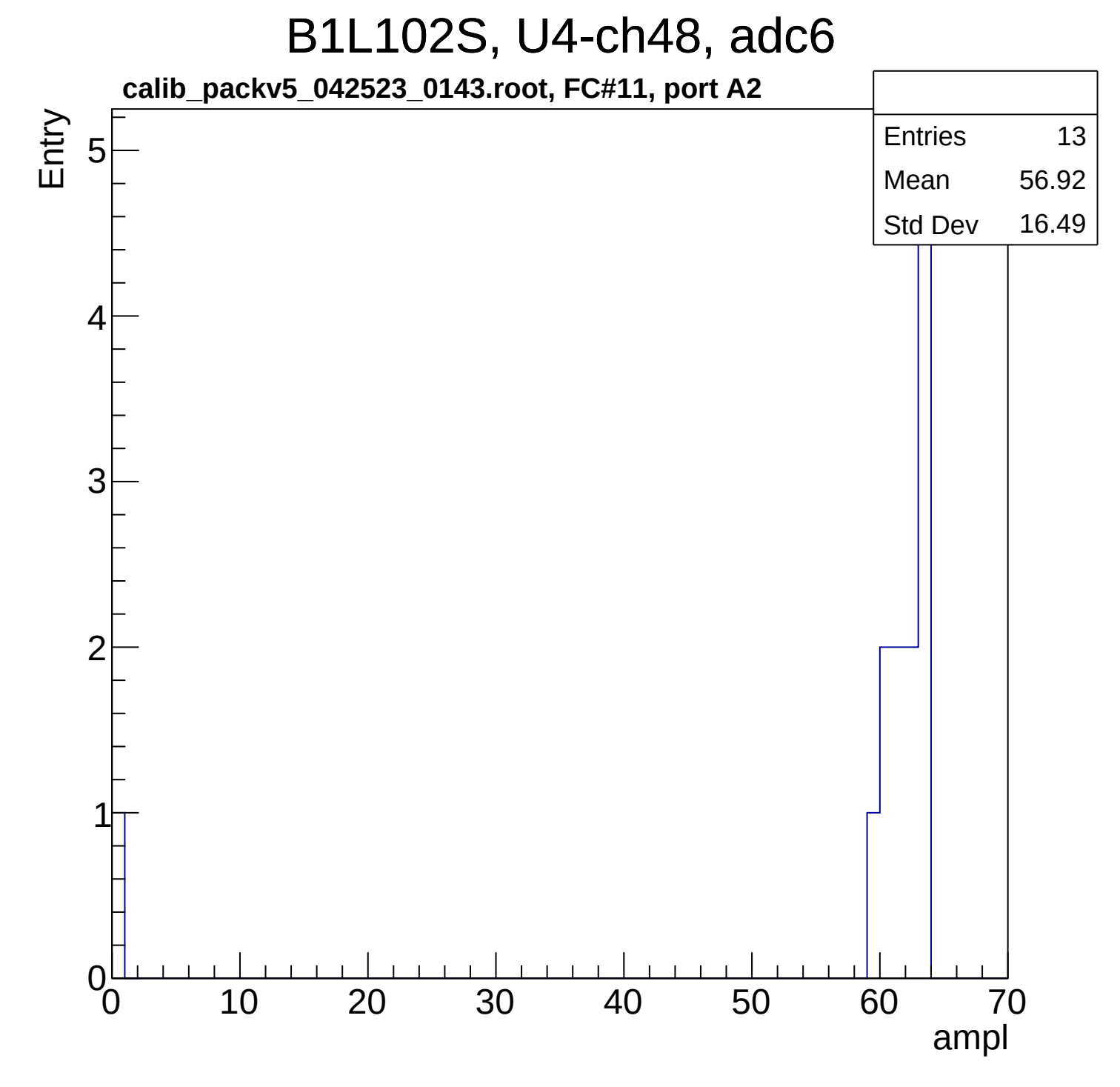
40
50
60
70


B1L102S, U4-ch48, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 13
Mean 56.92
Std Dev 16.49
Entry
0
1
2
3
4
5
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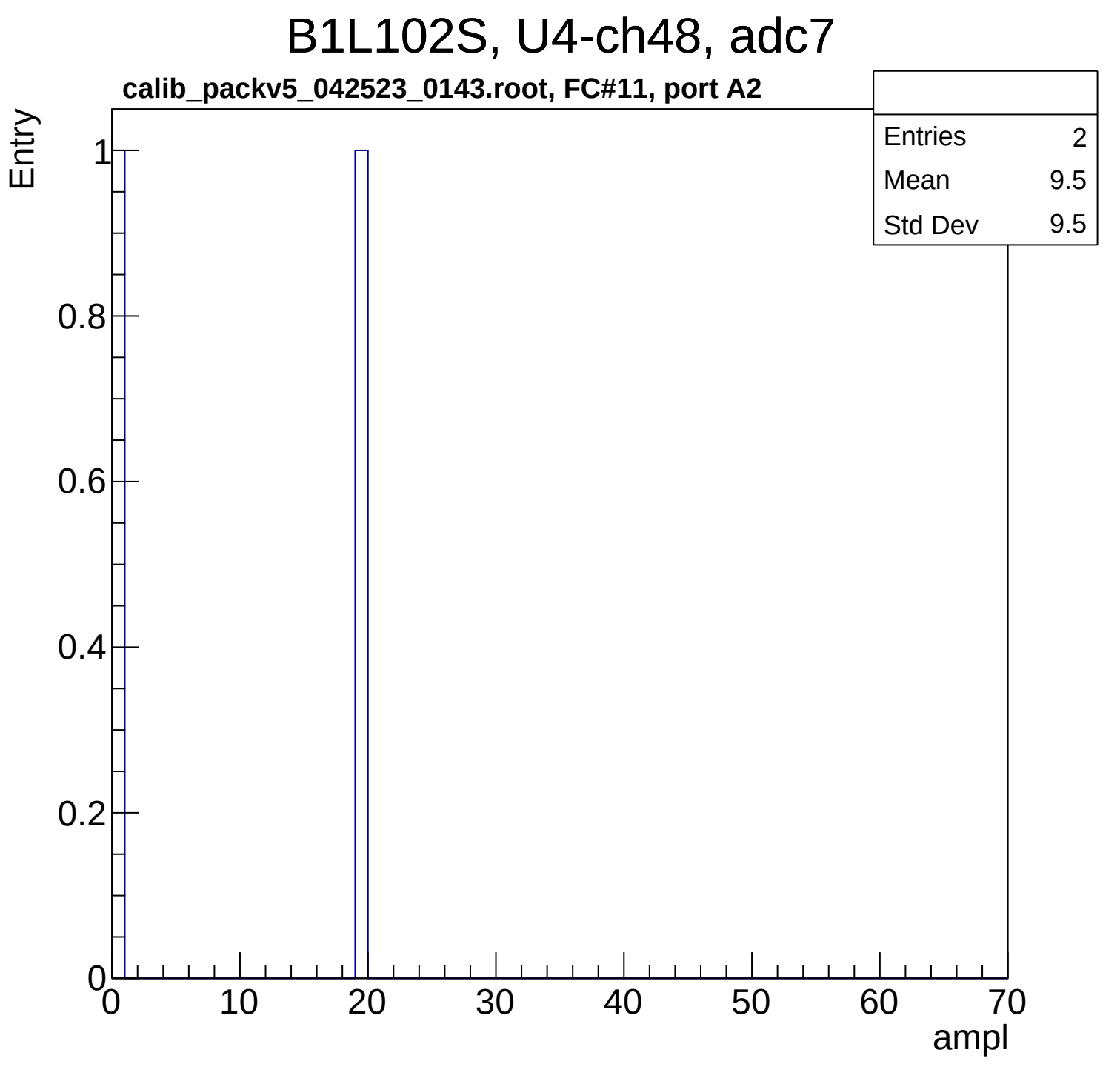
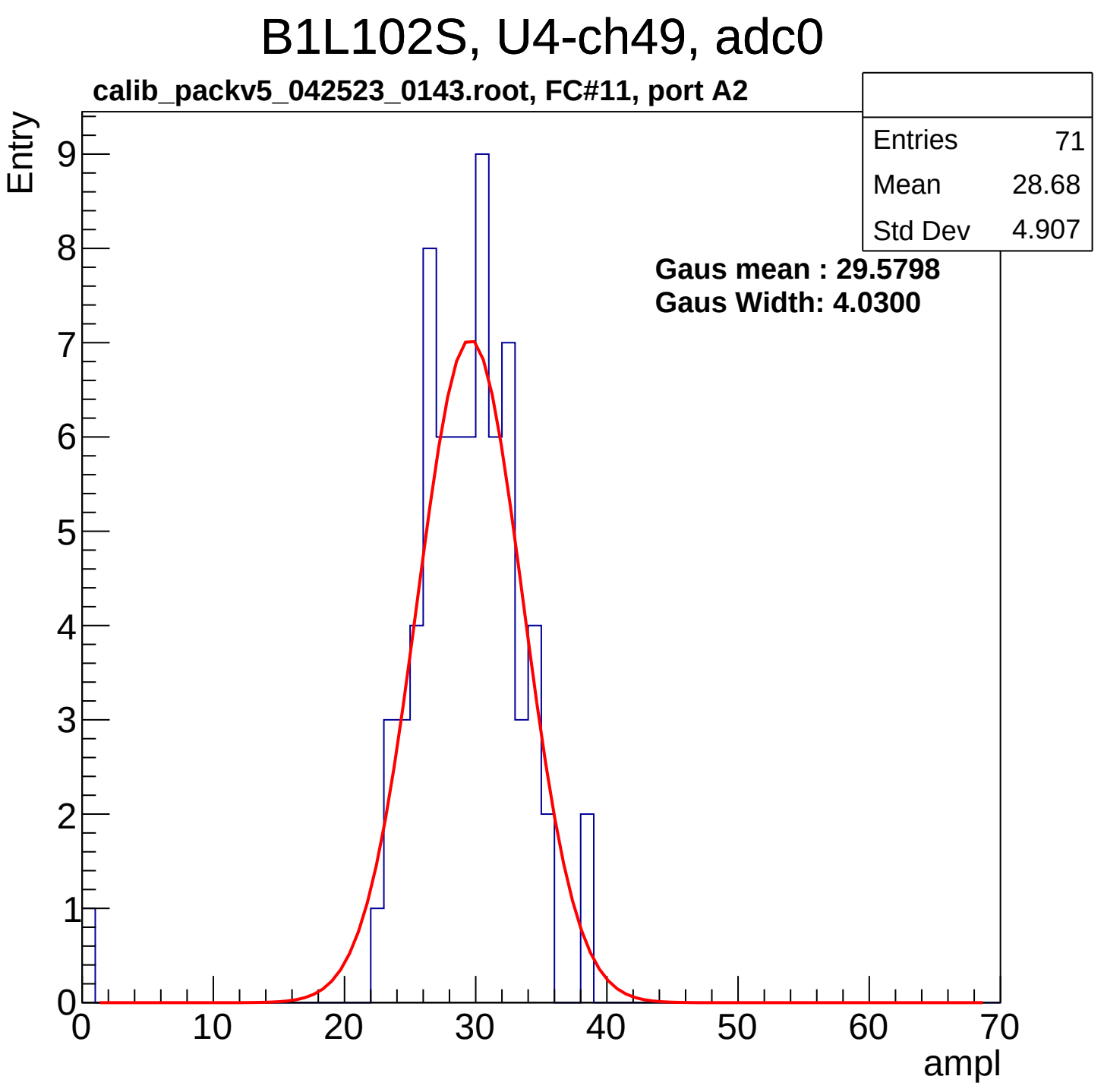
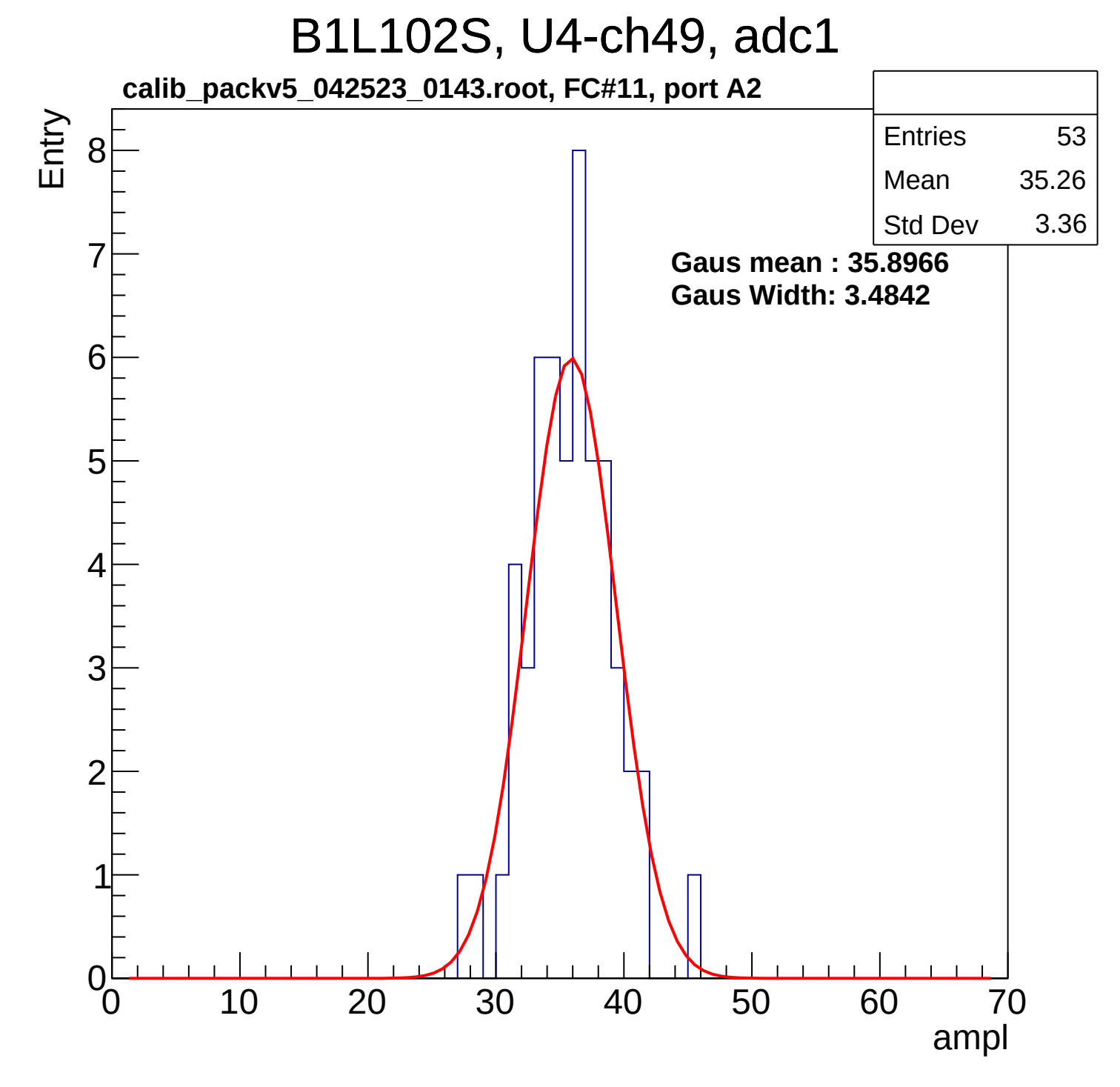
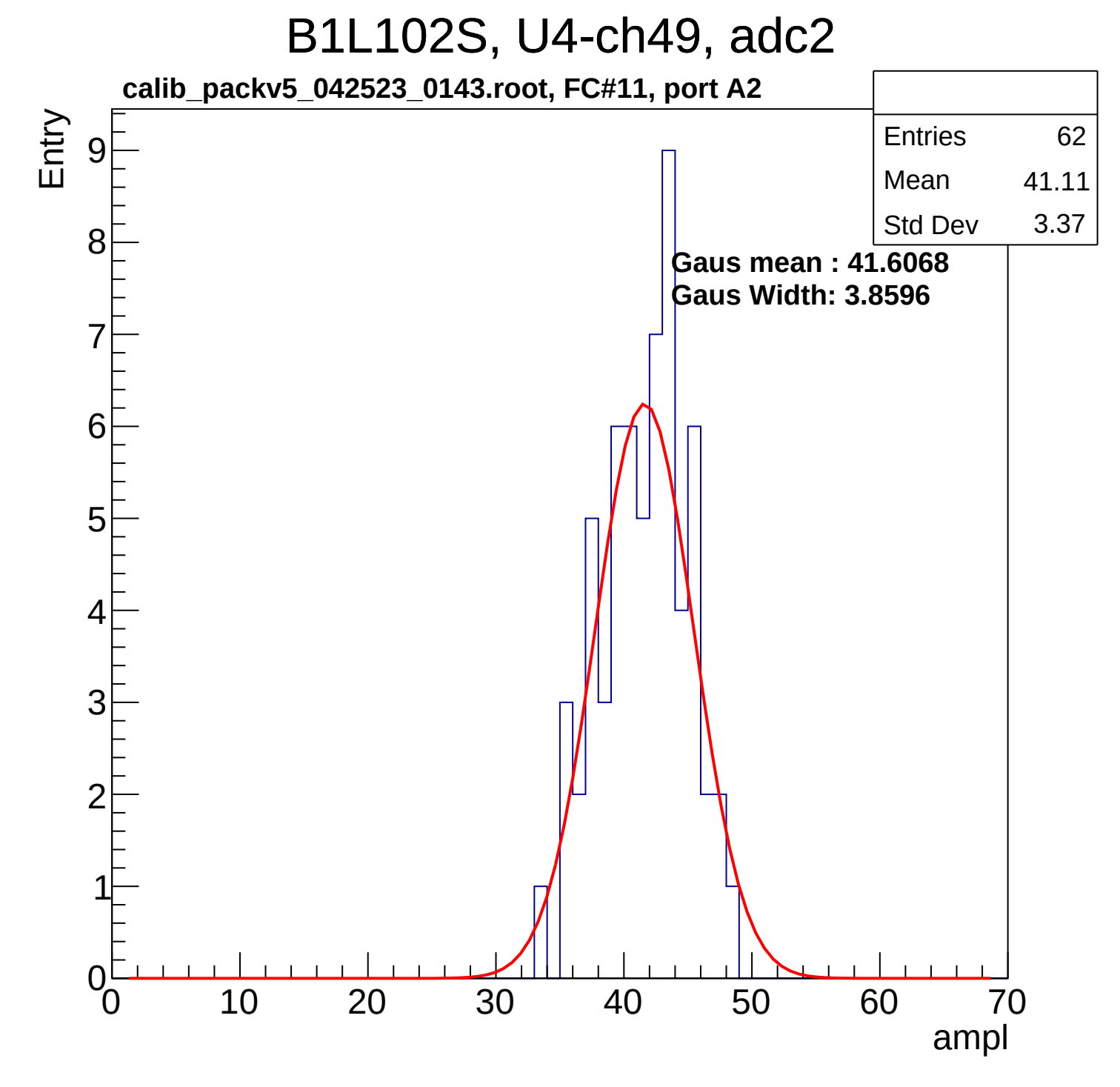
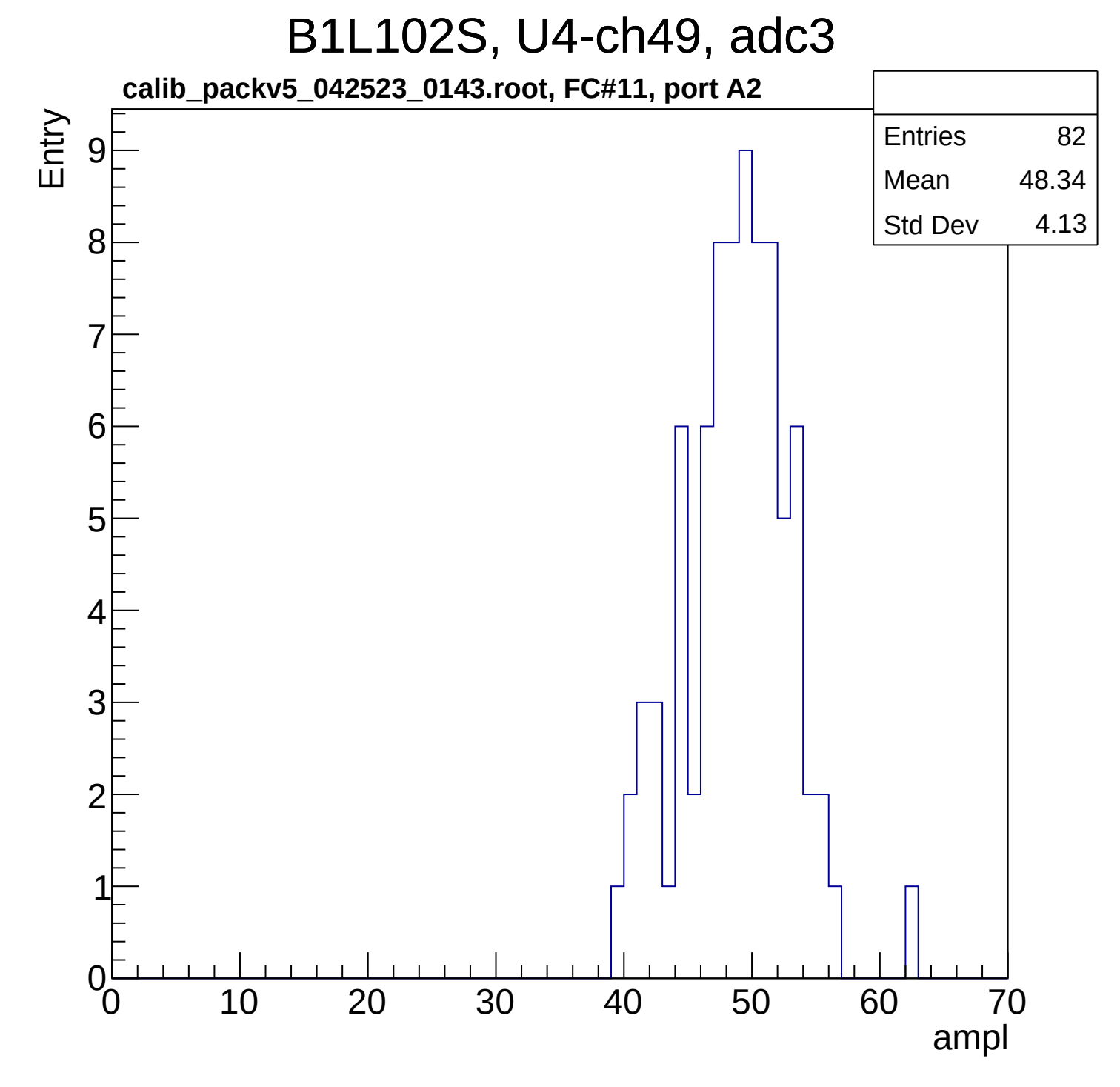
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch48, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 9.5
Std Dev 9.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch49, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 28.68
Std Dev 4.907
Gaus mean : 29.5798
Gaus Width: 4.0300
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch49, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 35.26
Std Dev 3.36
Gaus mean : 35.8966
Gaus Width: 3.4842
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch49, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 41.11
Std Dev 3.37
Gaus mean : 41.6068
Gaus Width: 3.8596
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch49, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 82
Mean 48.34
Std Dev 4.13
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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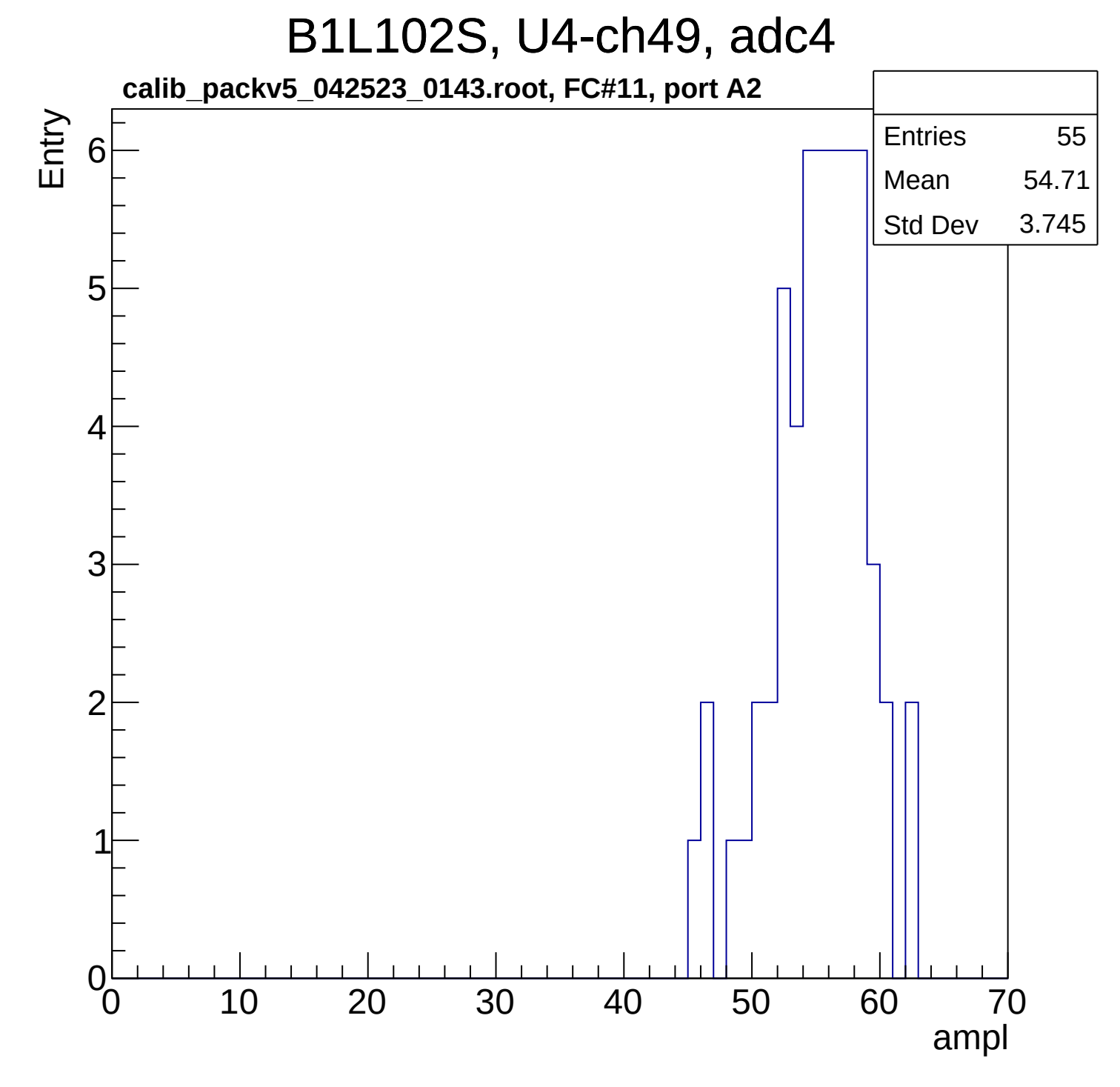
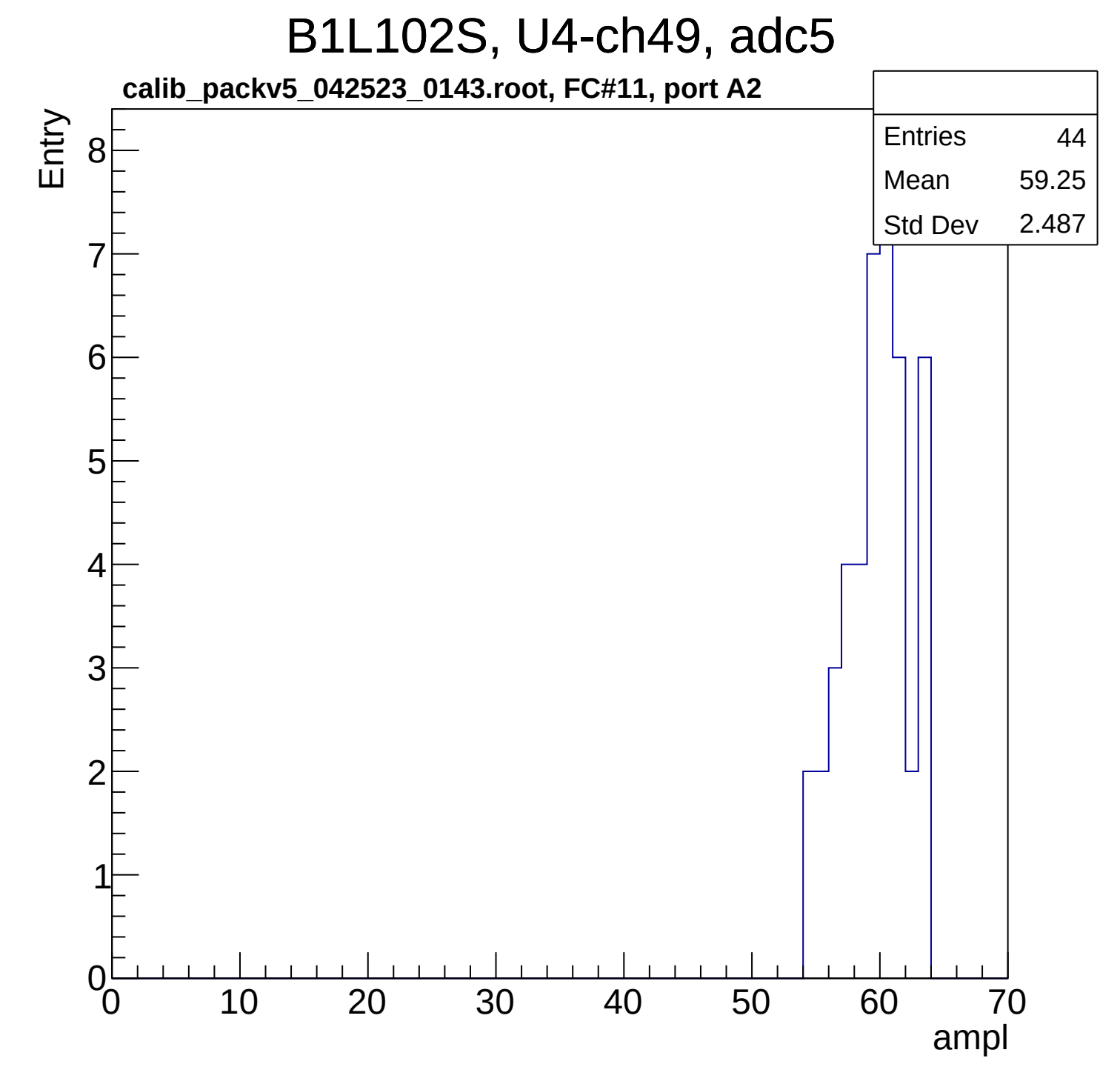
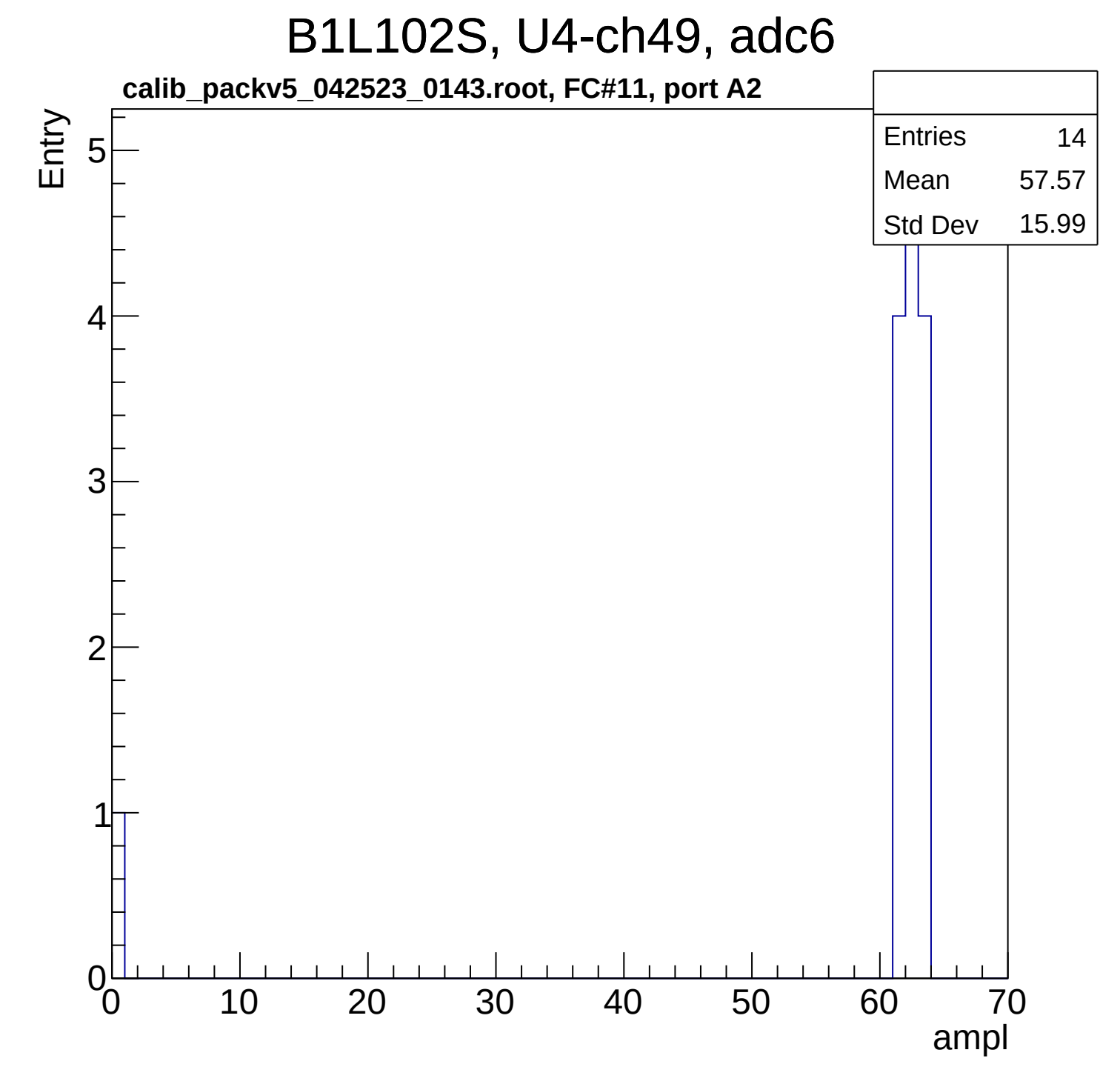
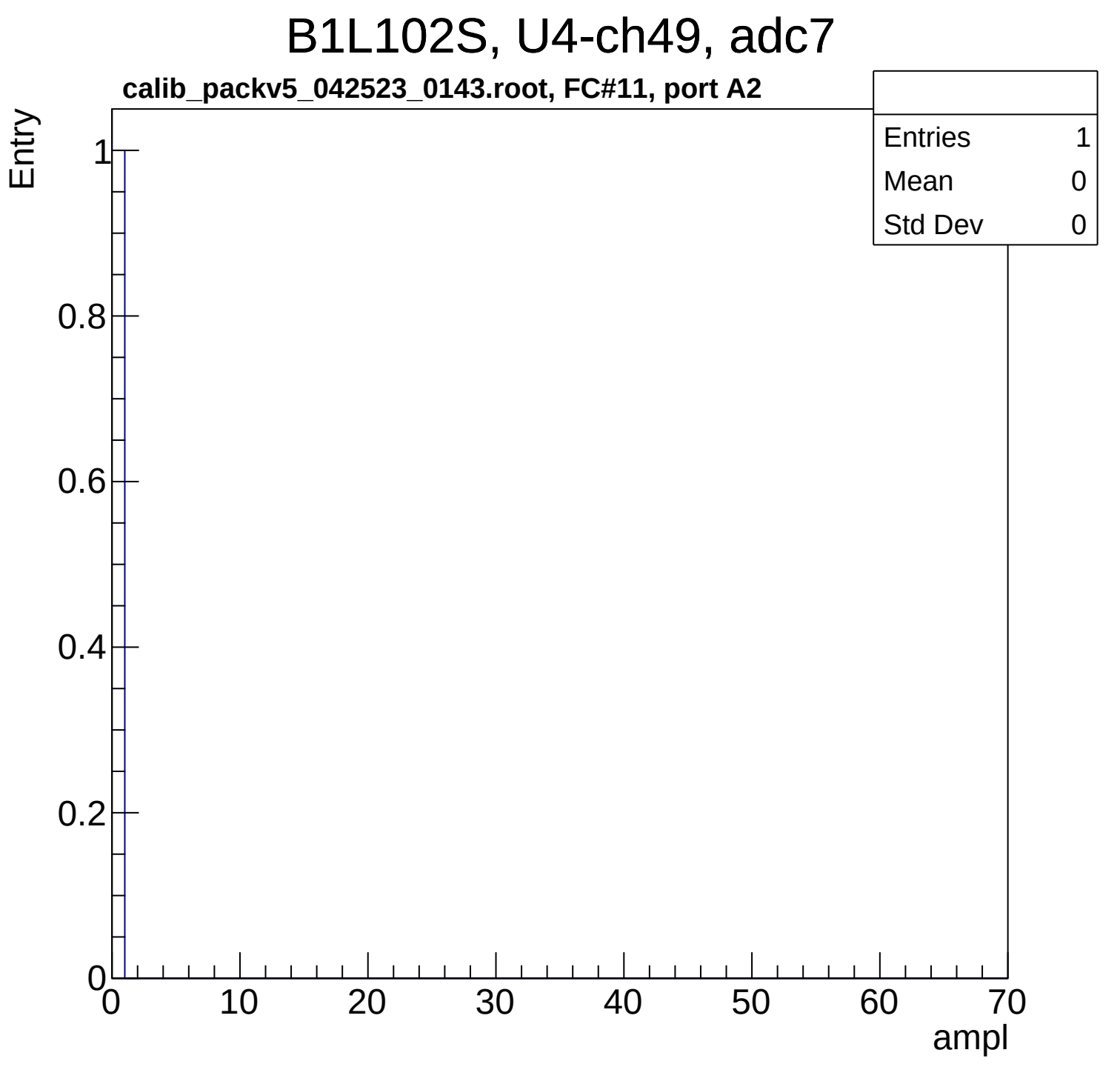

B1L102S, U4-ch49, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 54.71
Std Dev 3.745
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L102S, U4-ch49, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 44
Mean 59.25
Std Dev 2.487
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch49, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 14
Mean 57.57
Std Dev 15.99
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch49, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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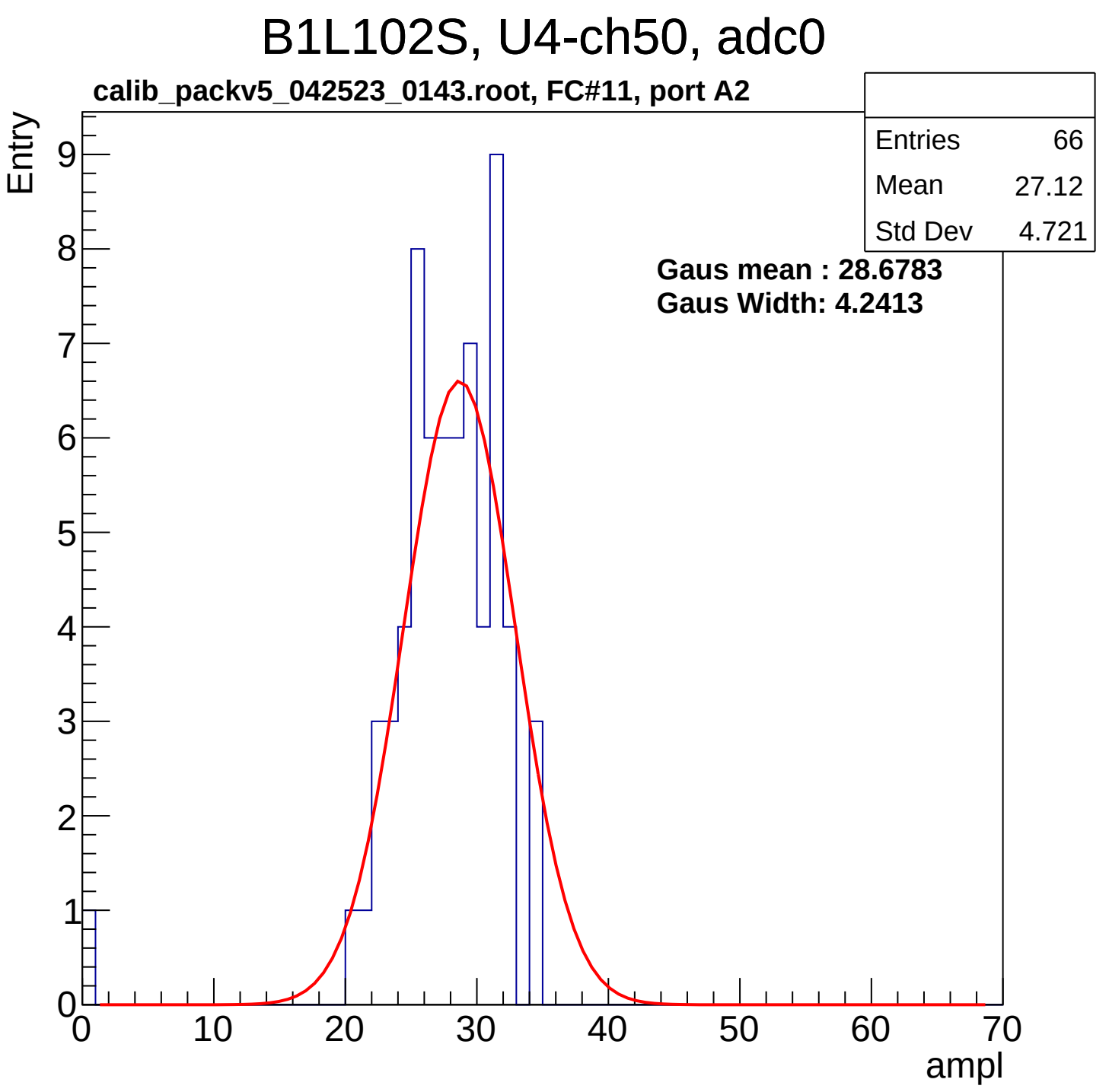
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch50, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 27.12
Std Dev 4.721
Gaus mean : 28.6783
Gaus Width: 4.2413
Entry
ampl
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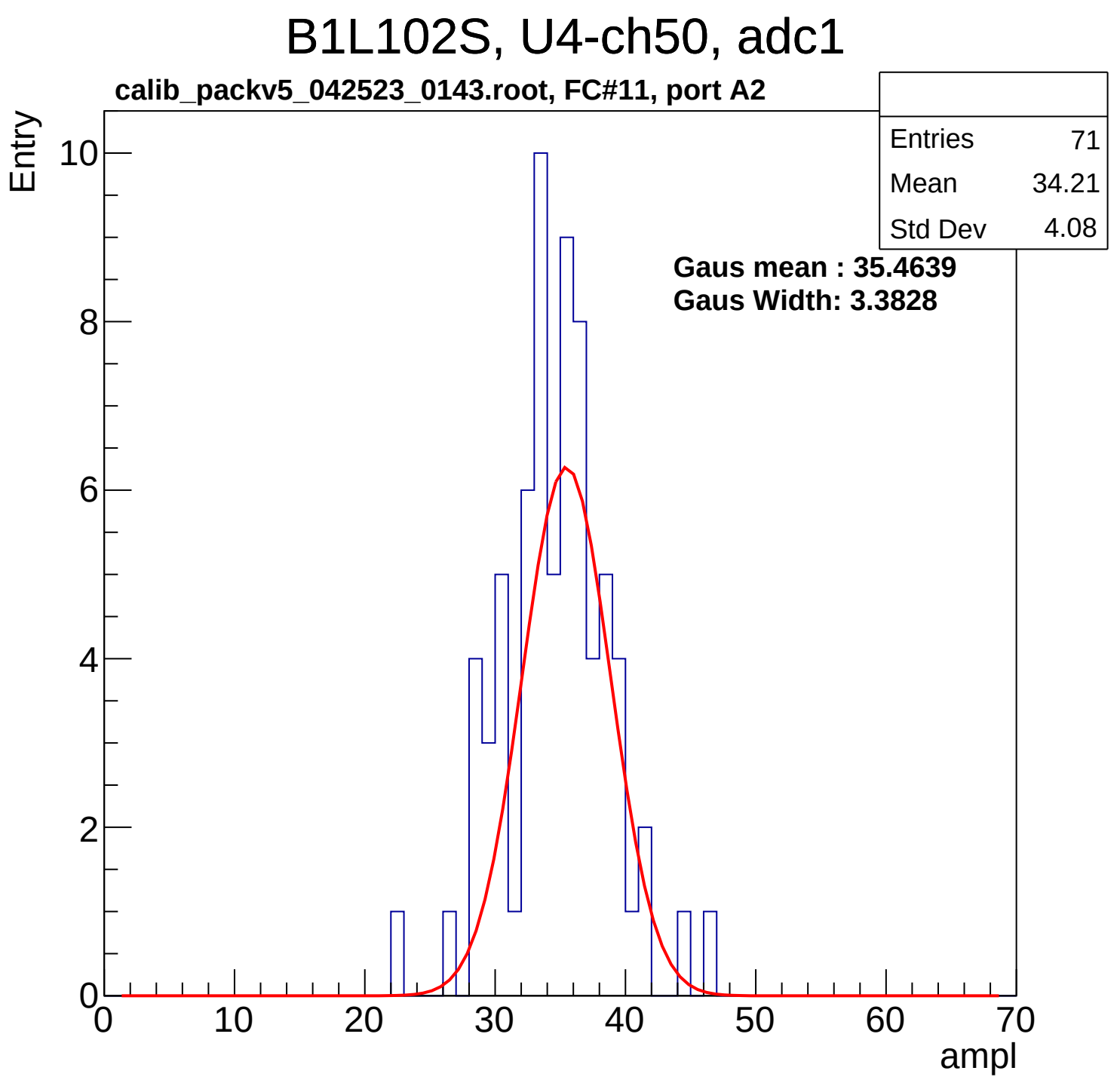
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch50, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 34.21
Std Dev 4.08
Gaus mean : 35.4639
Gaus Width: 3.3828
Entry
ampl
0
2
4
6
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0
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60
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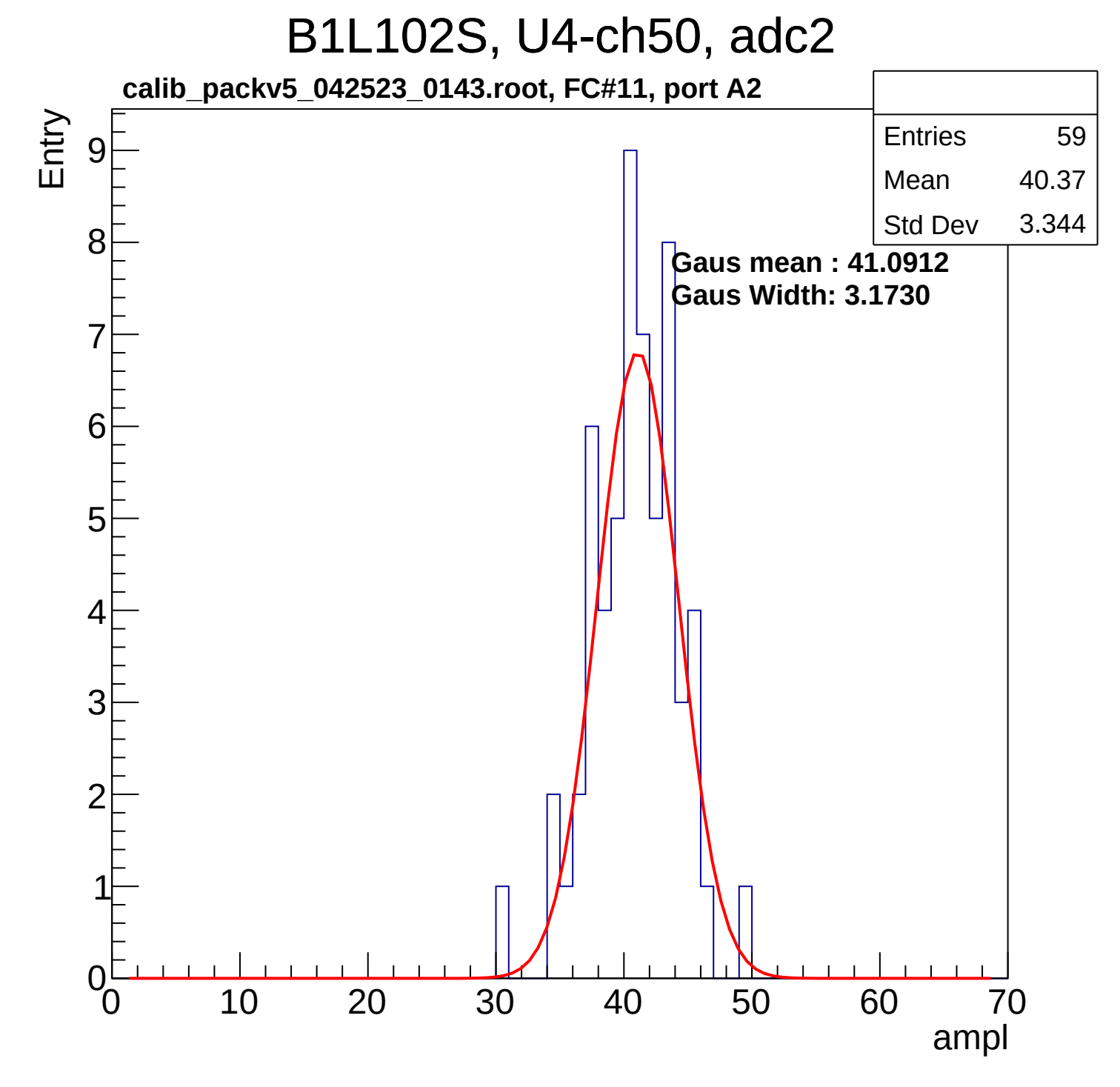
B1L102S, U4-ch50, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 40.37
Std Dev 3.344
Gaus mean : 41.0912
Gaus Width: 3.1730
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
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60
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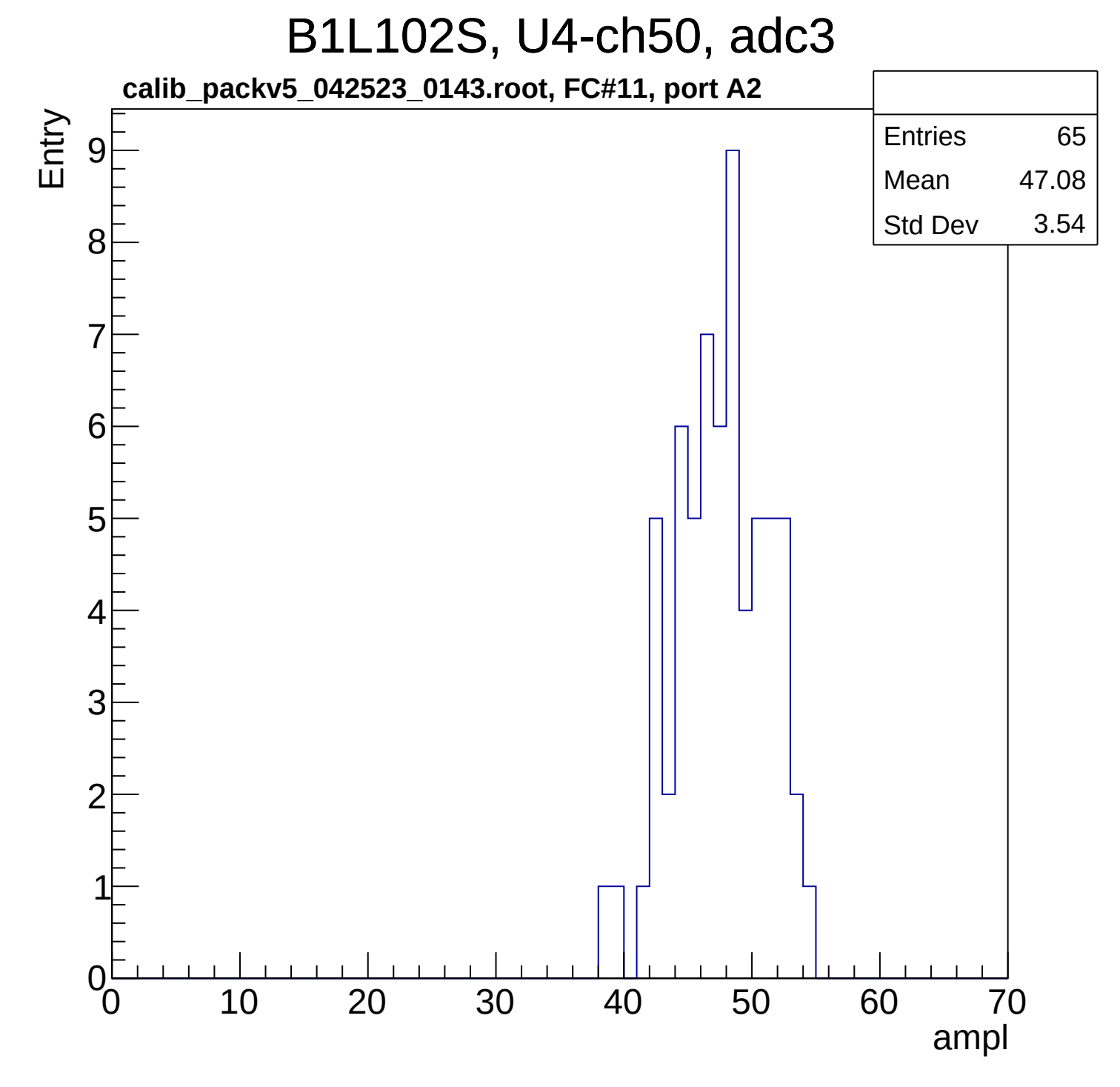
B1L102S, U4-ch50, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 47.08
Std Dev 3.54
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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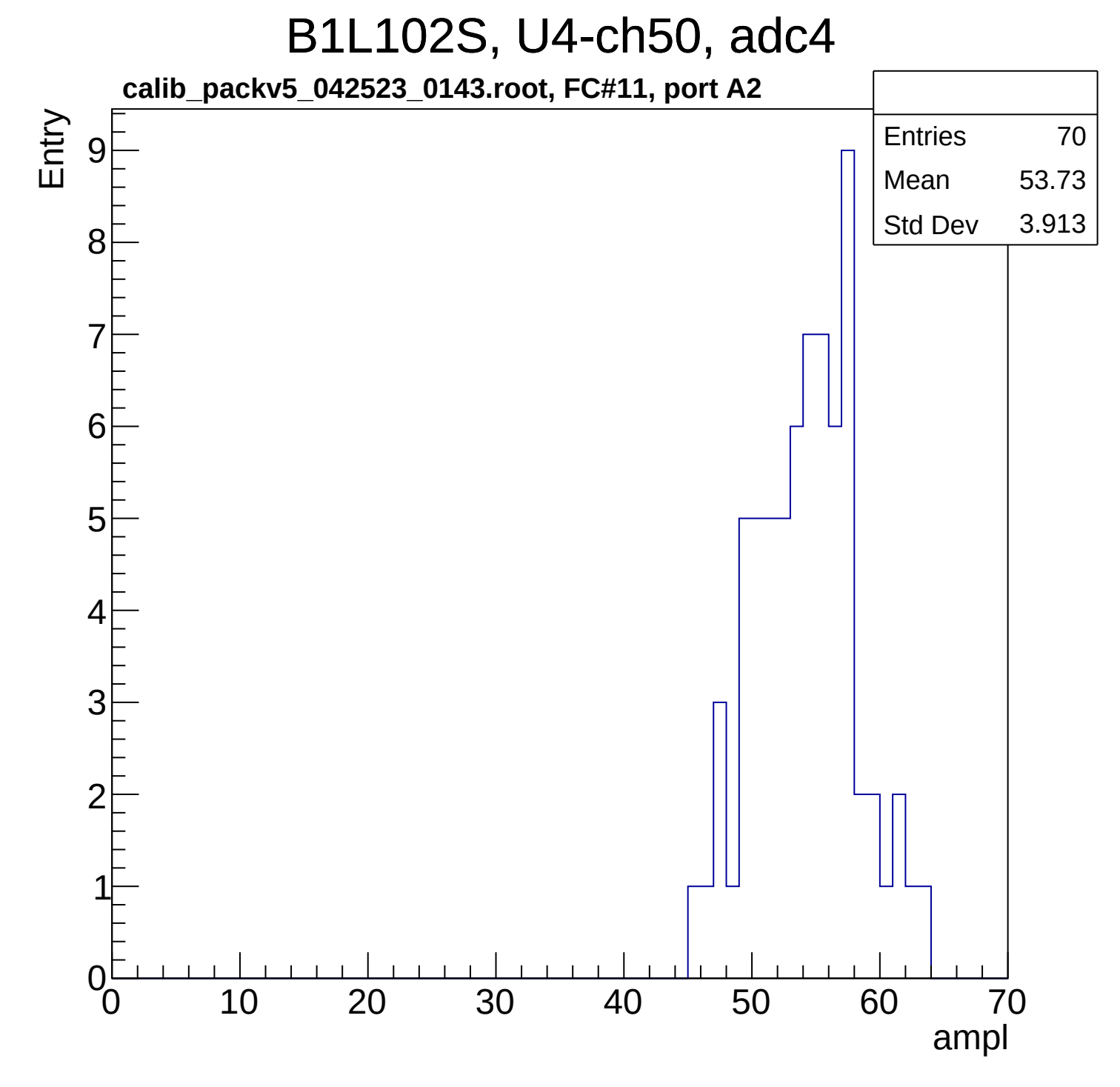
B1L102S, U4-ch50, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 53.73
Std Dev 3.913
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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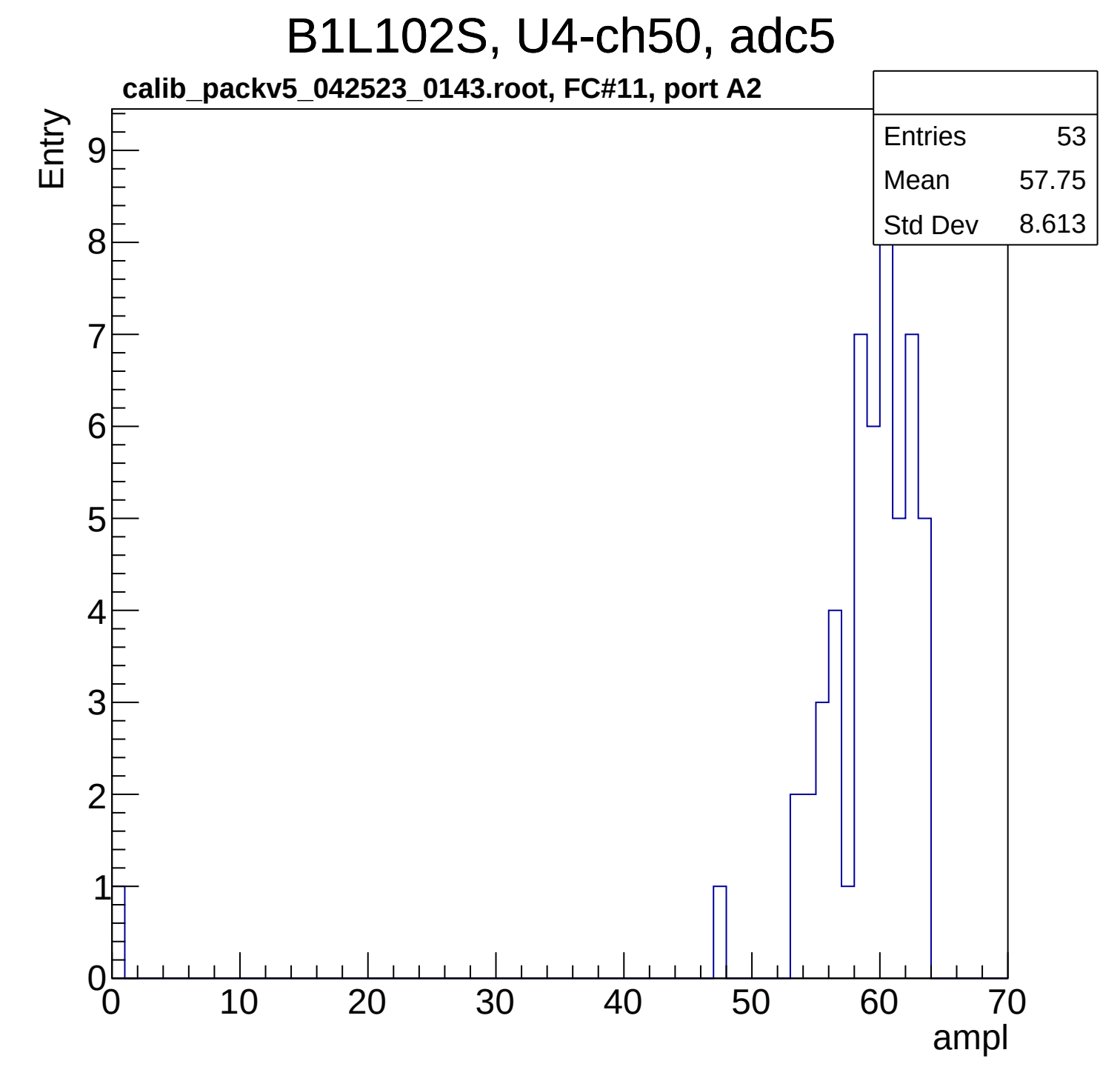
B1L102S, U4-ch50, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 57.75
Std Dev 8.613
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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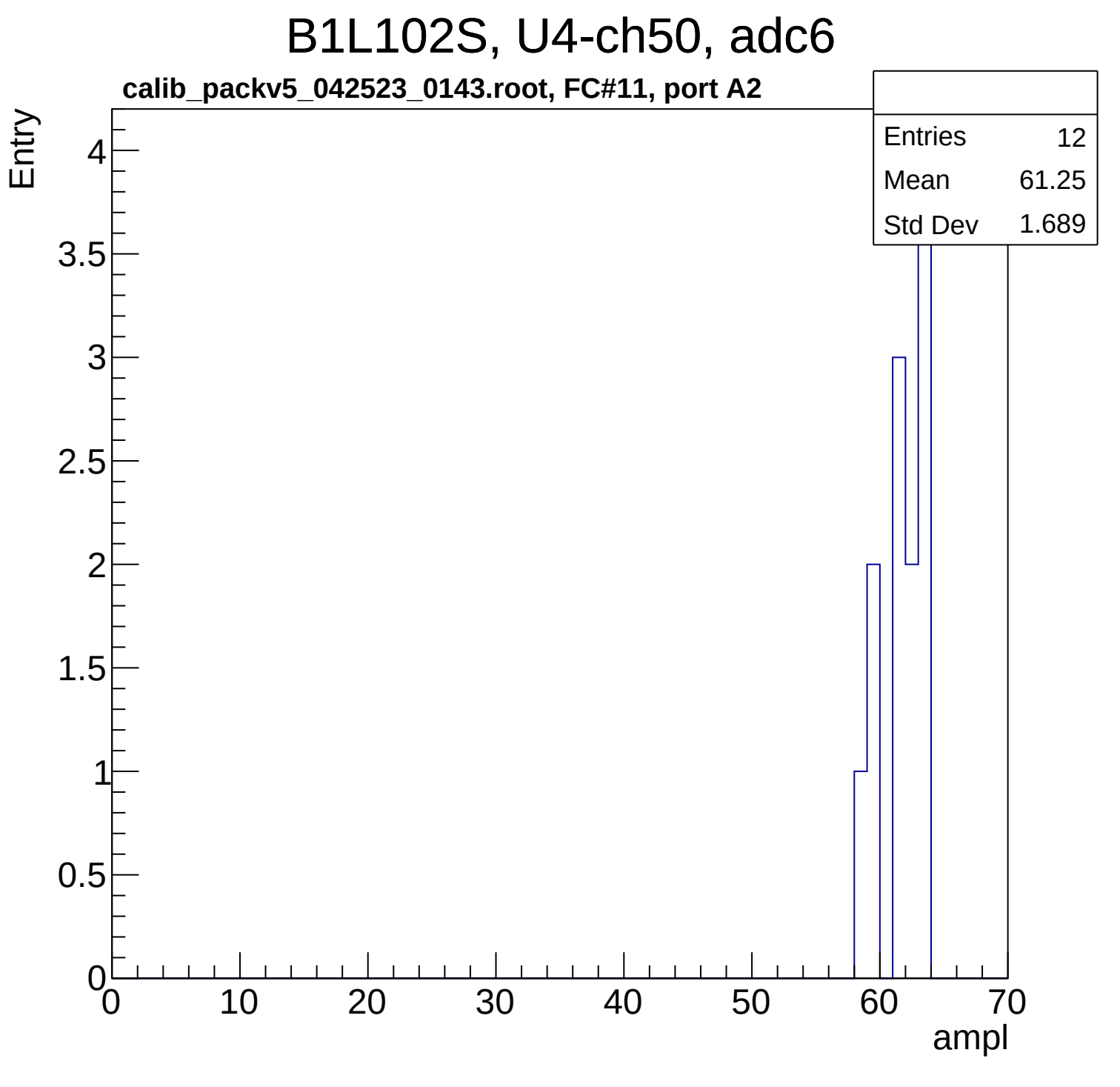
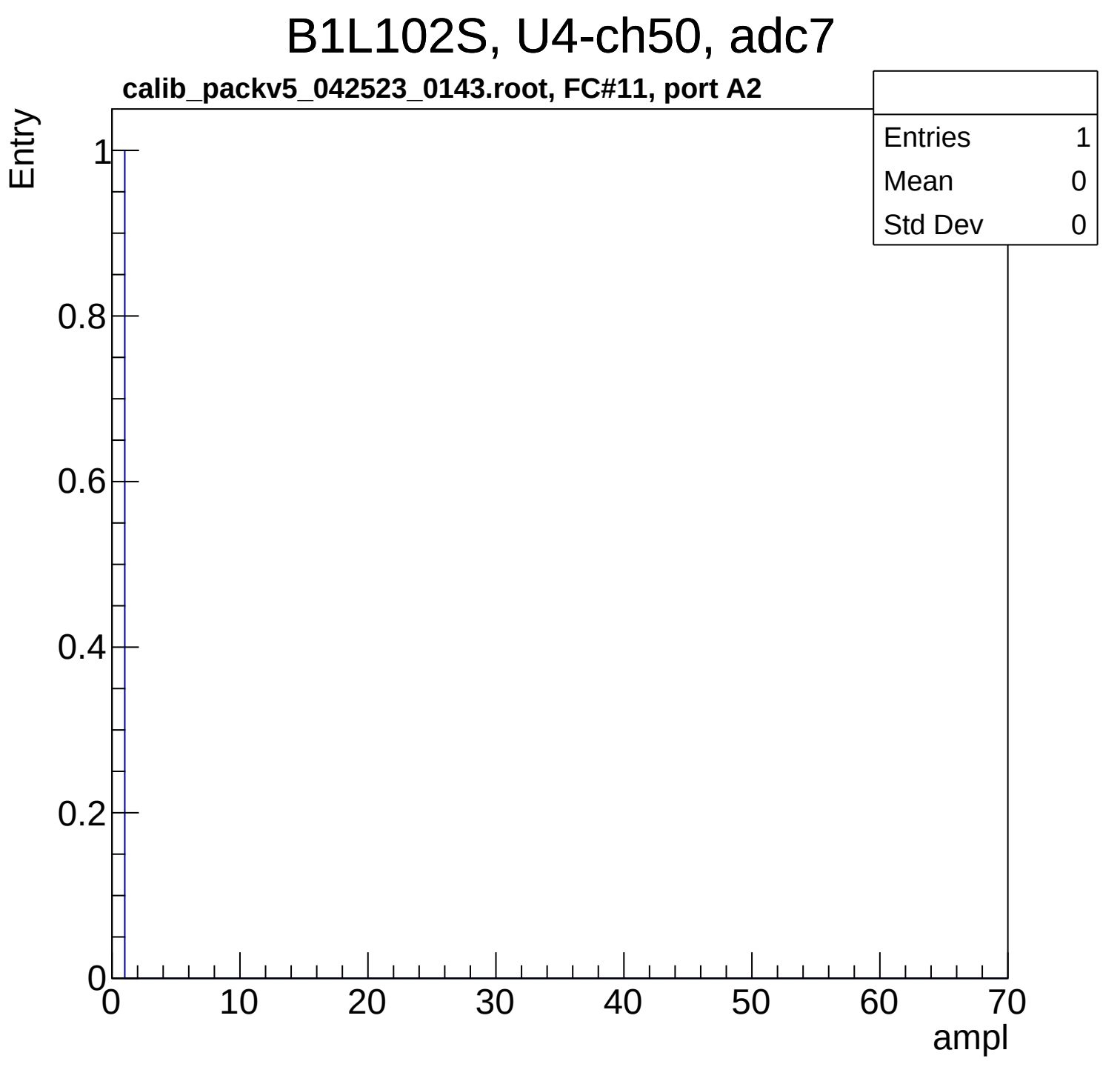
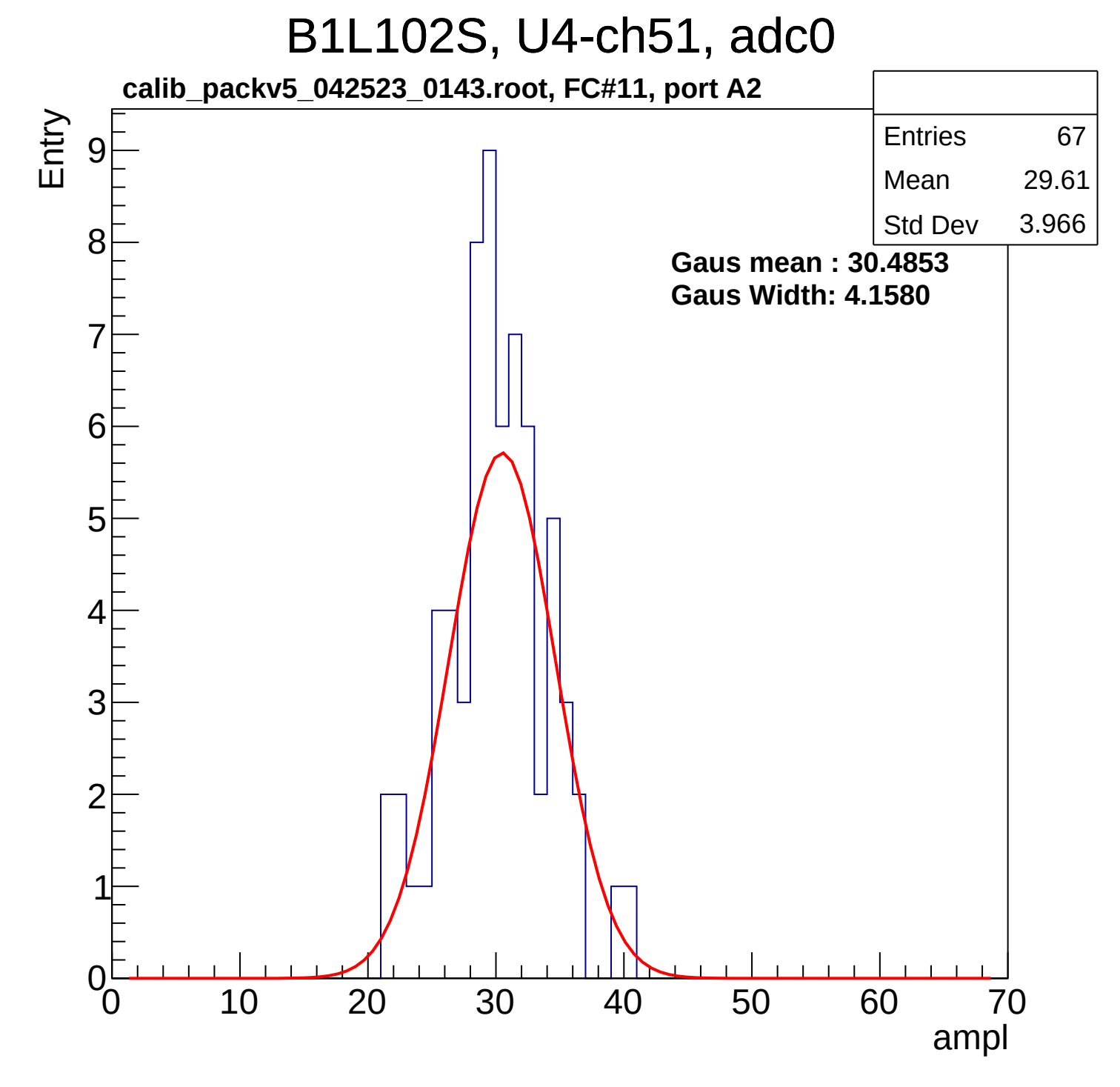
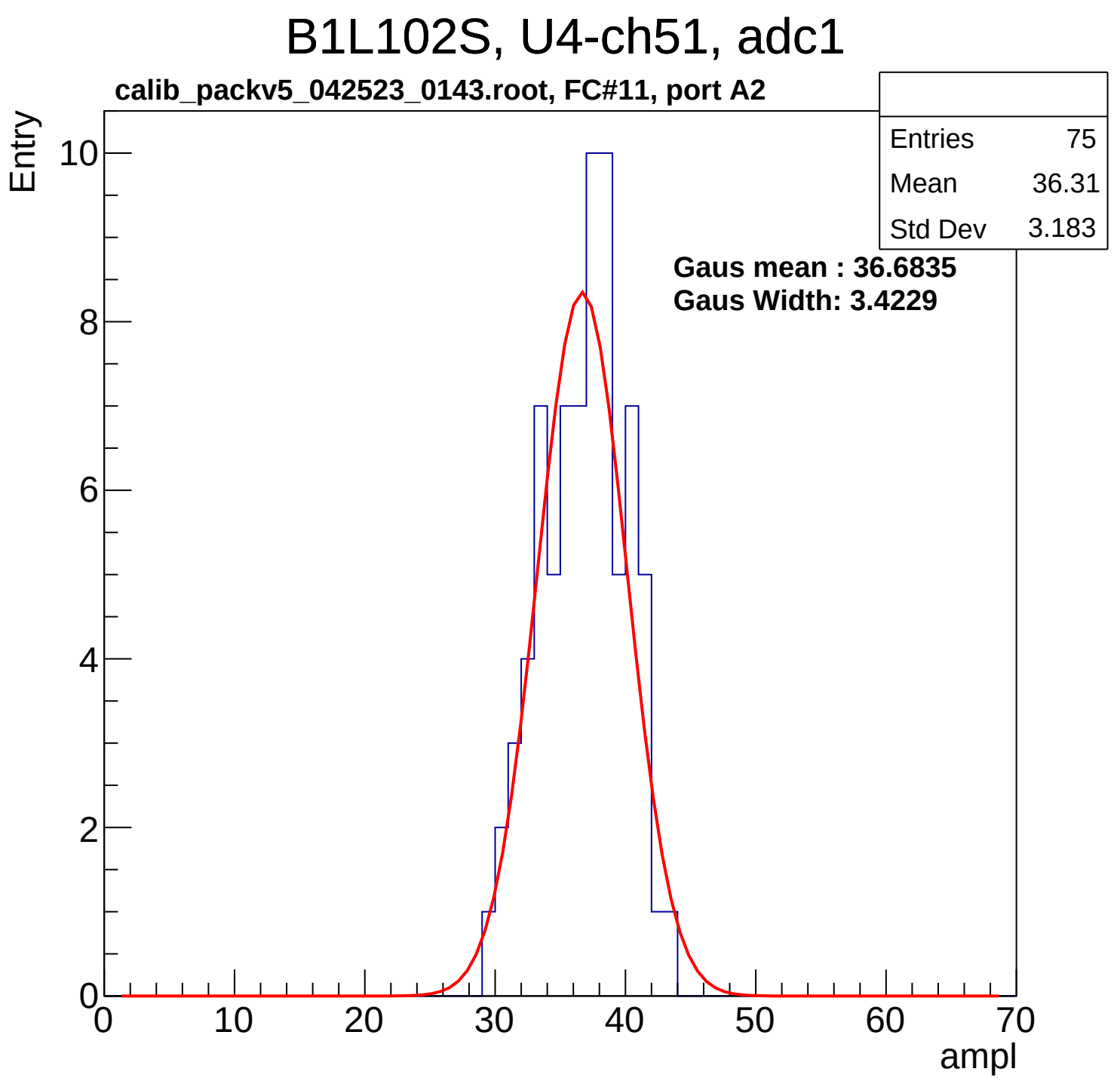

B1L102S, U4-ch50, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 12
Mean 61.25
Std Dev 1.689
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U4-ch50, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch51, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 29.61
Std Dev 3.966
Gaus mean : 30.4853
Gaus Width: 4.1580
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch51, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 36.31
Std Dev 3.183
Gaus mean : 36.6835
Gaus Width: 3.4229
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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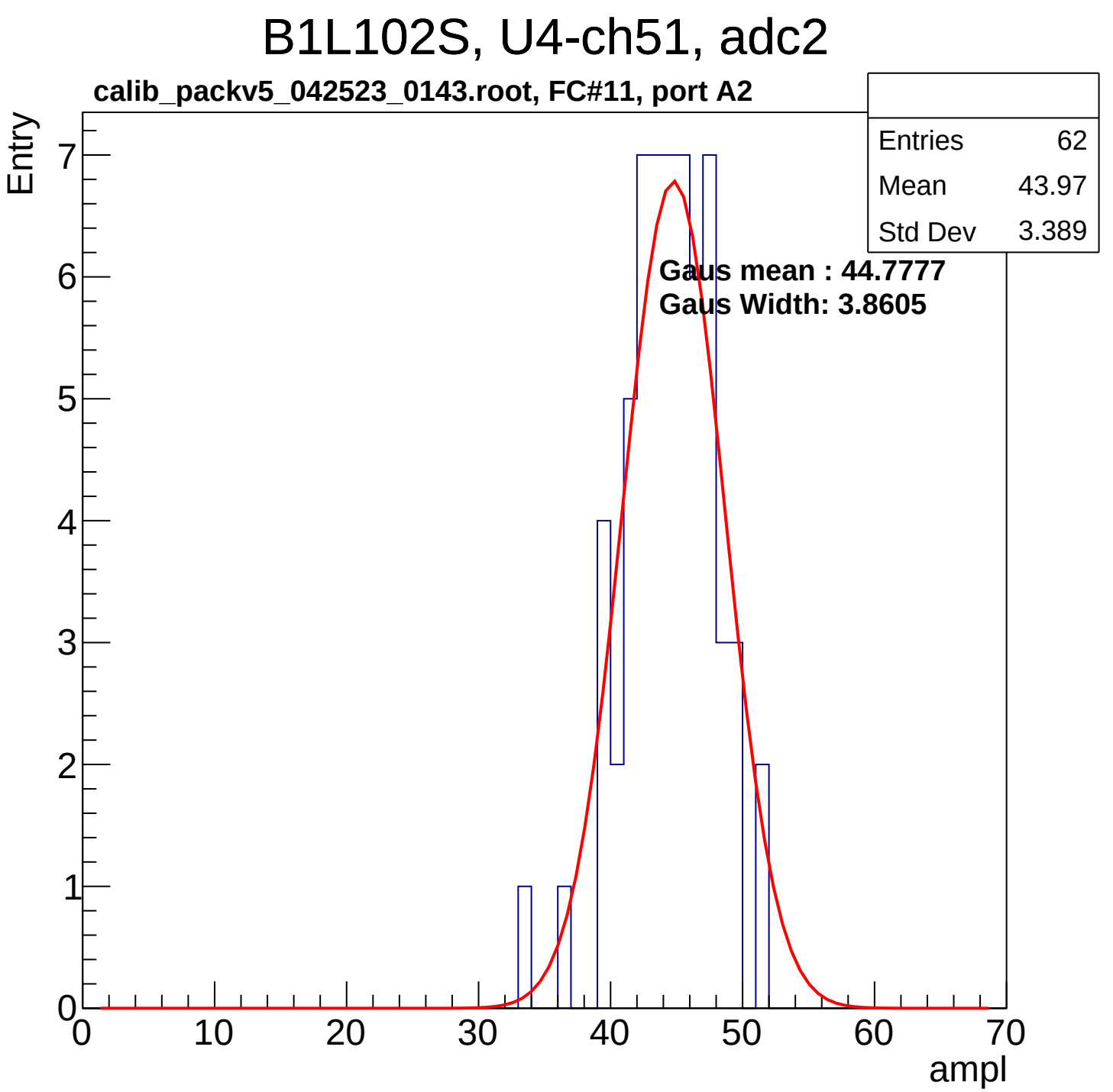
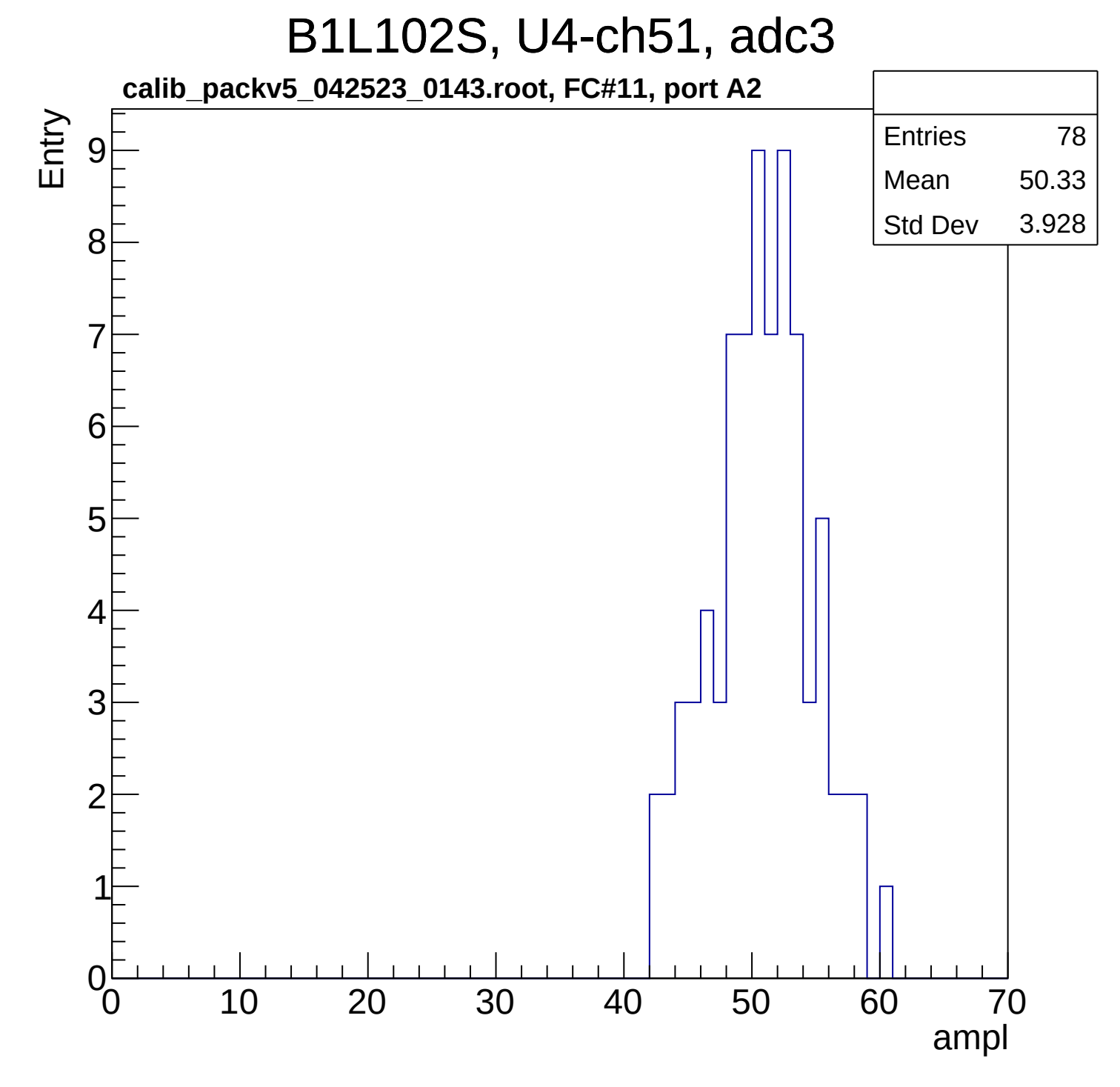

B1L102S, U4-ch51, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 43.97
Std Dev 3.389
Gaus mean : 44.7777
Gaus Width: 3.8605
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch51, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 78
Mean 50.33
Std Dev 3.928
Entry
ampl
0
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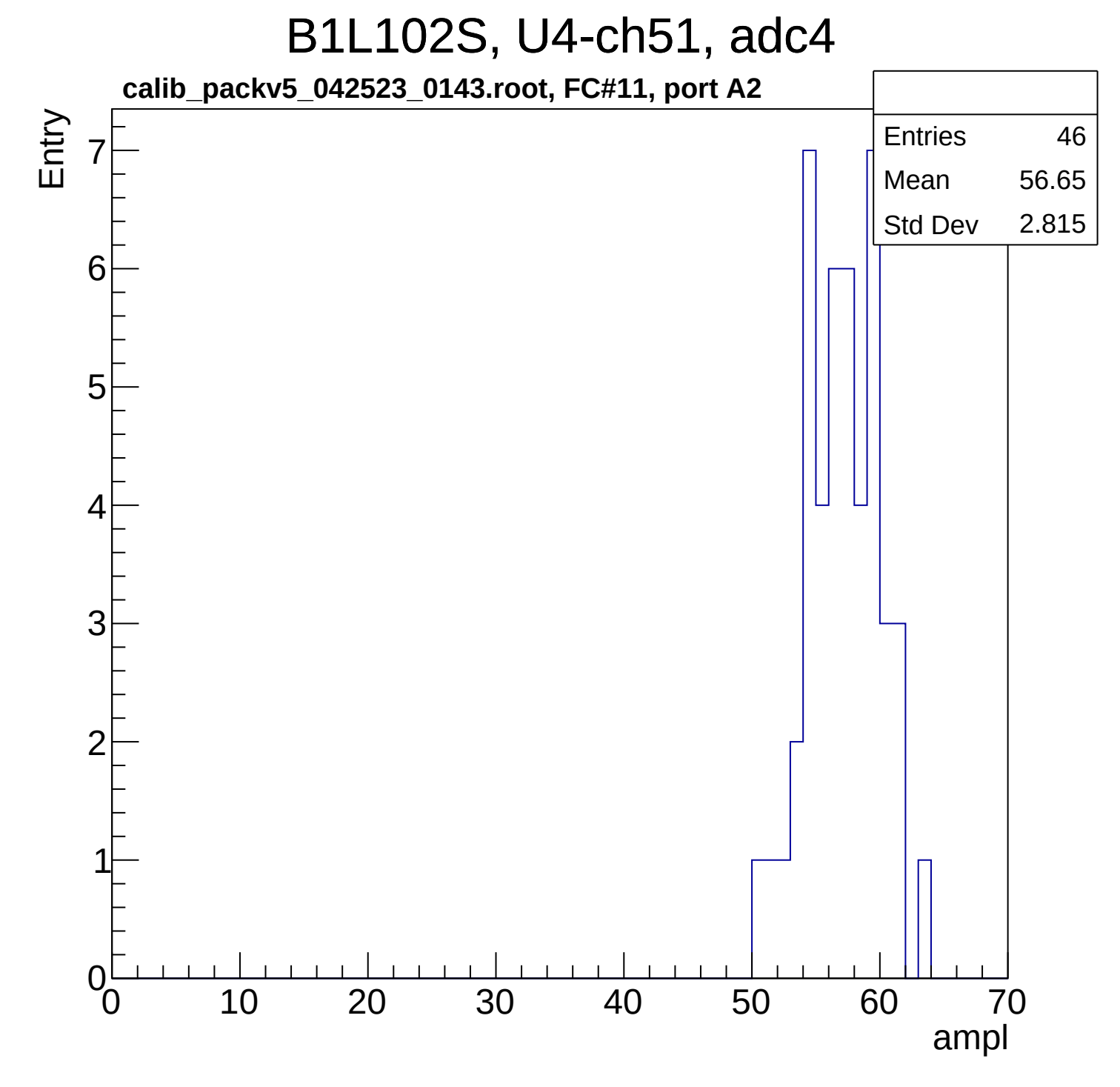
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch51, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 46
Mean 56.65
Std Dev 2.815
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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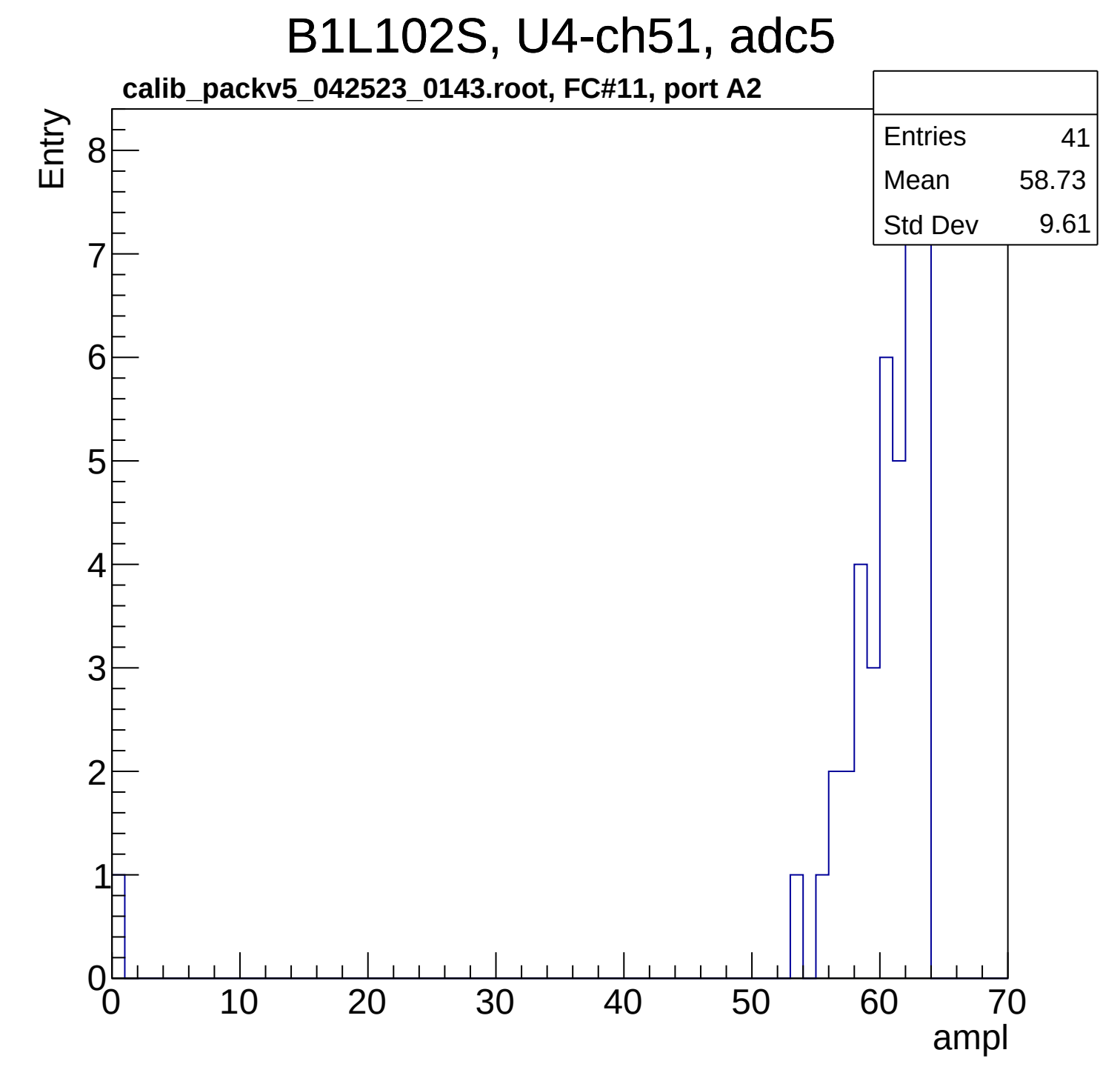
B1L102S, U4-ch51, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 41
Mean 58.73
Std Dev 9.61
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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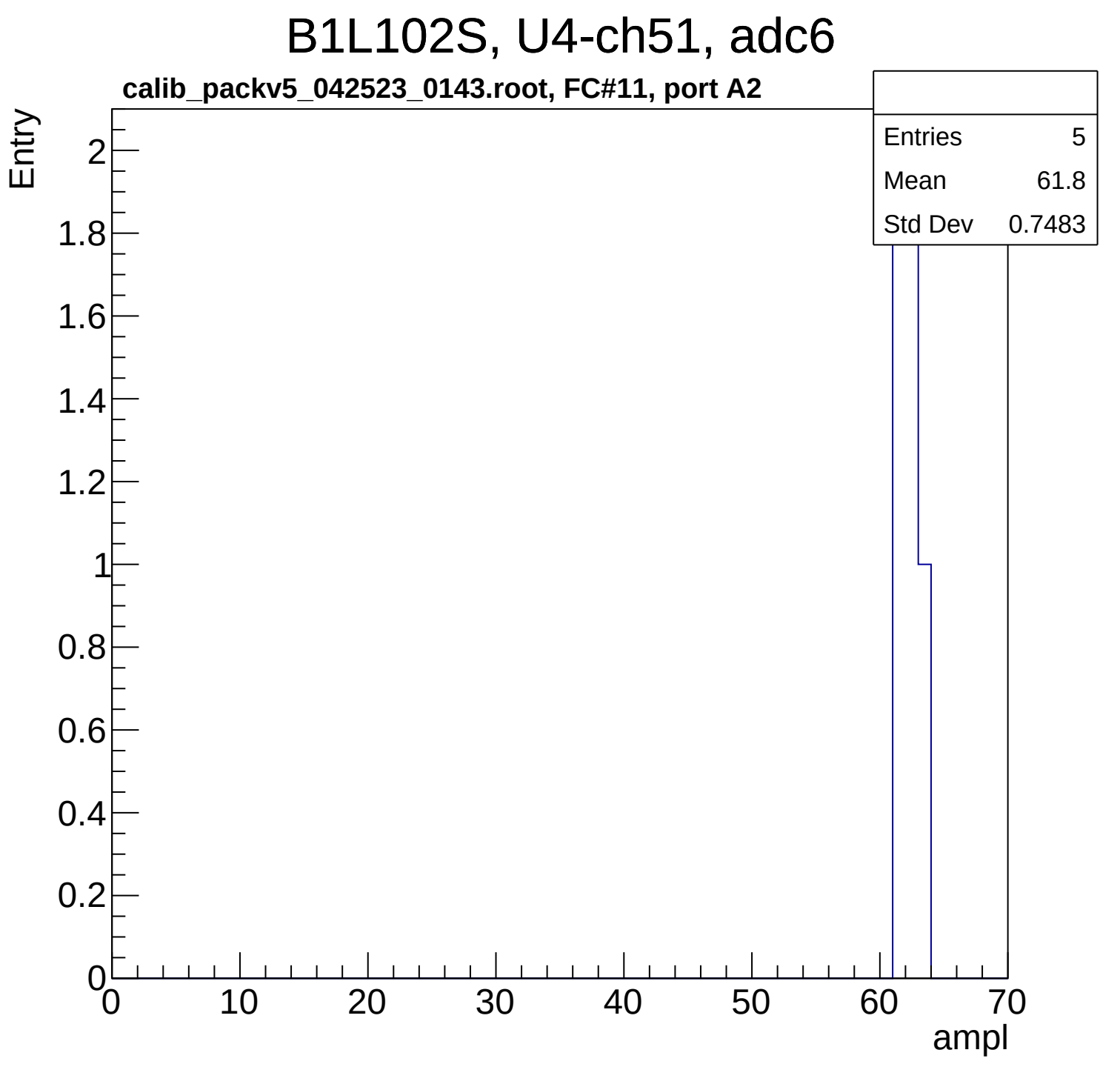
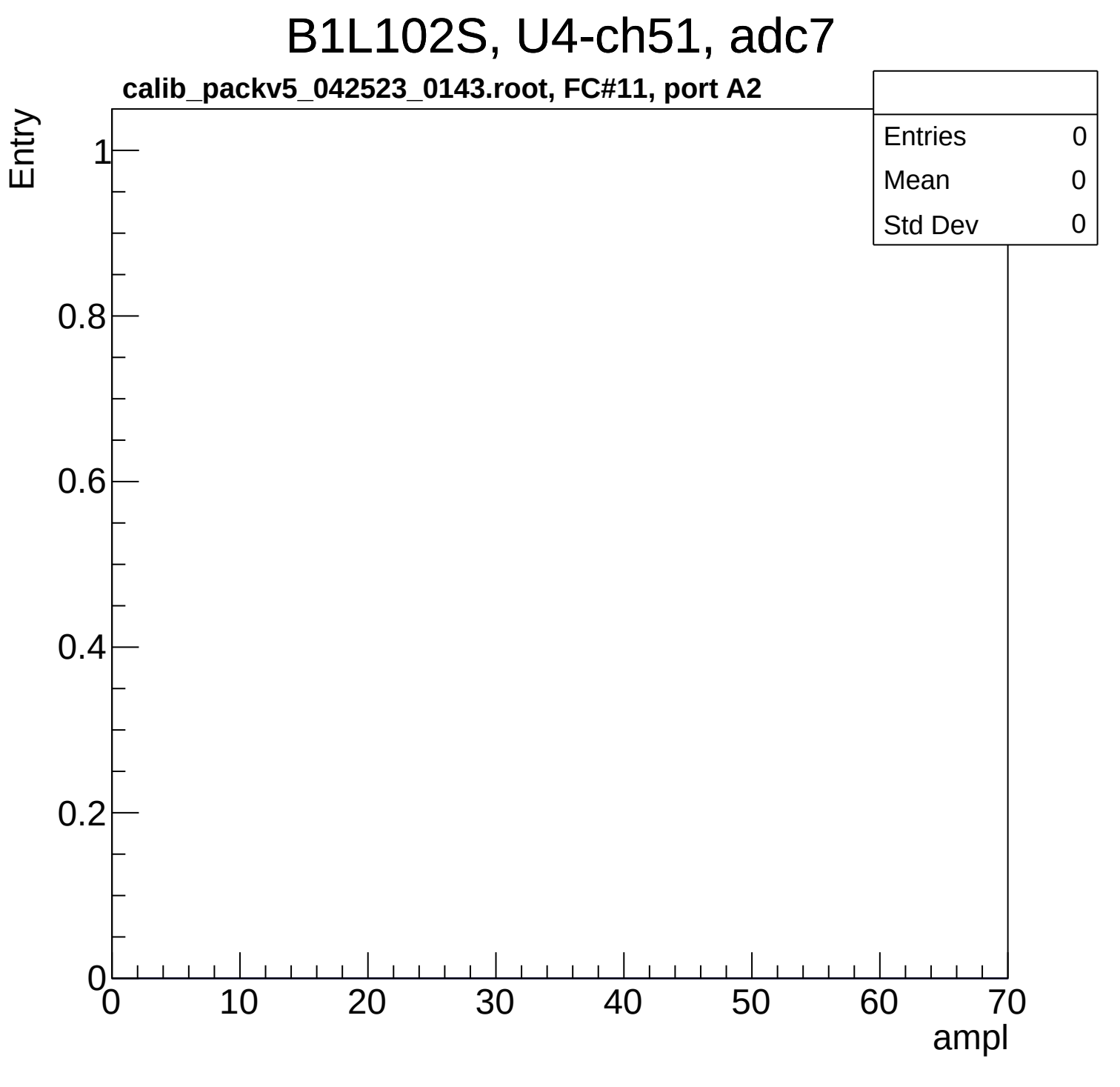
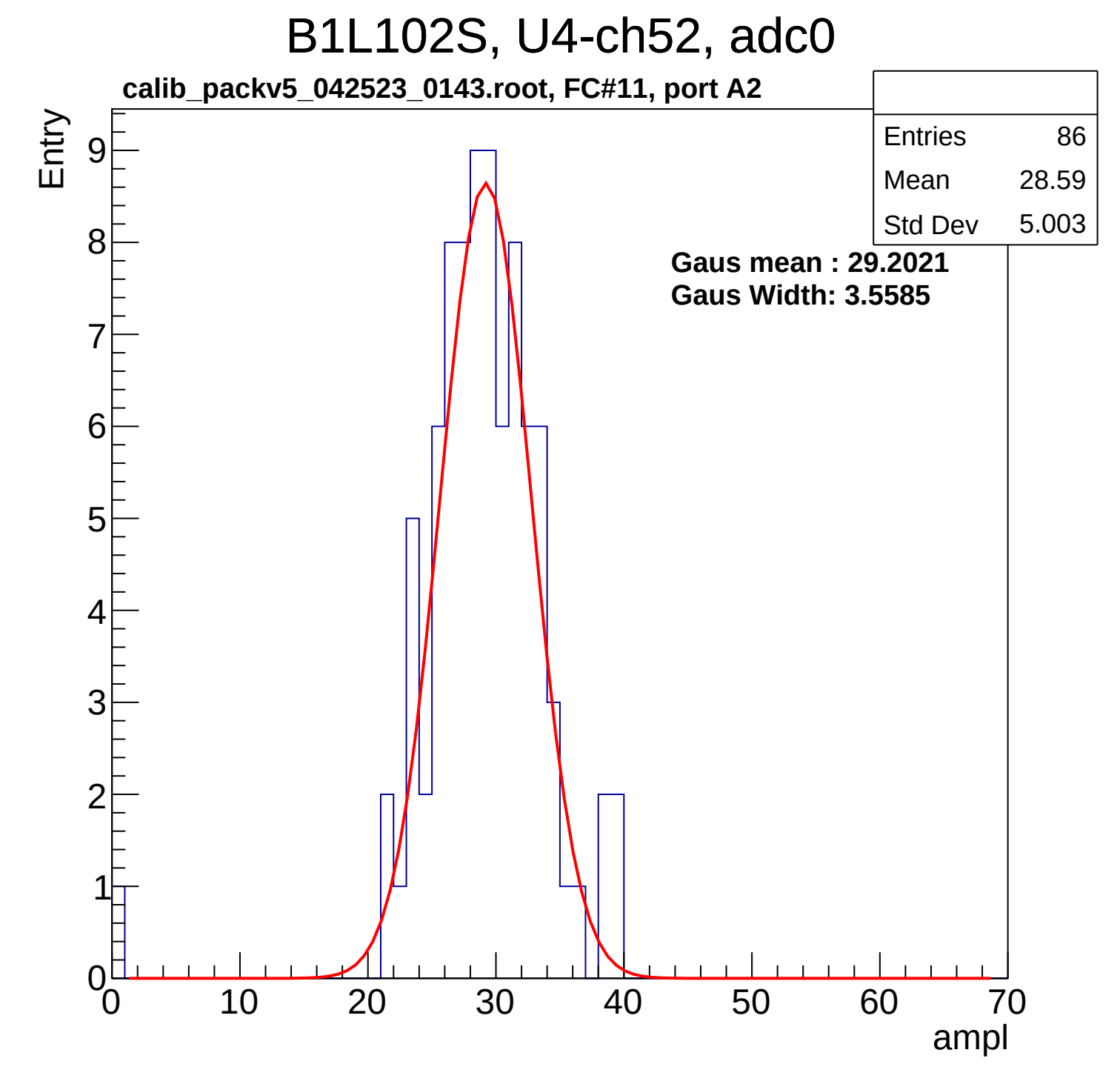

B1L102S, U4-ch51, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 5
Mean 61.8
Std Dev 0.7483
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L102S, U4-ch51, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch52, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 86
Mean 28.59
Std Dev 5.003
Gaus mean : 29.2021
Gaus Width: 3.5585
Entry
ampl
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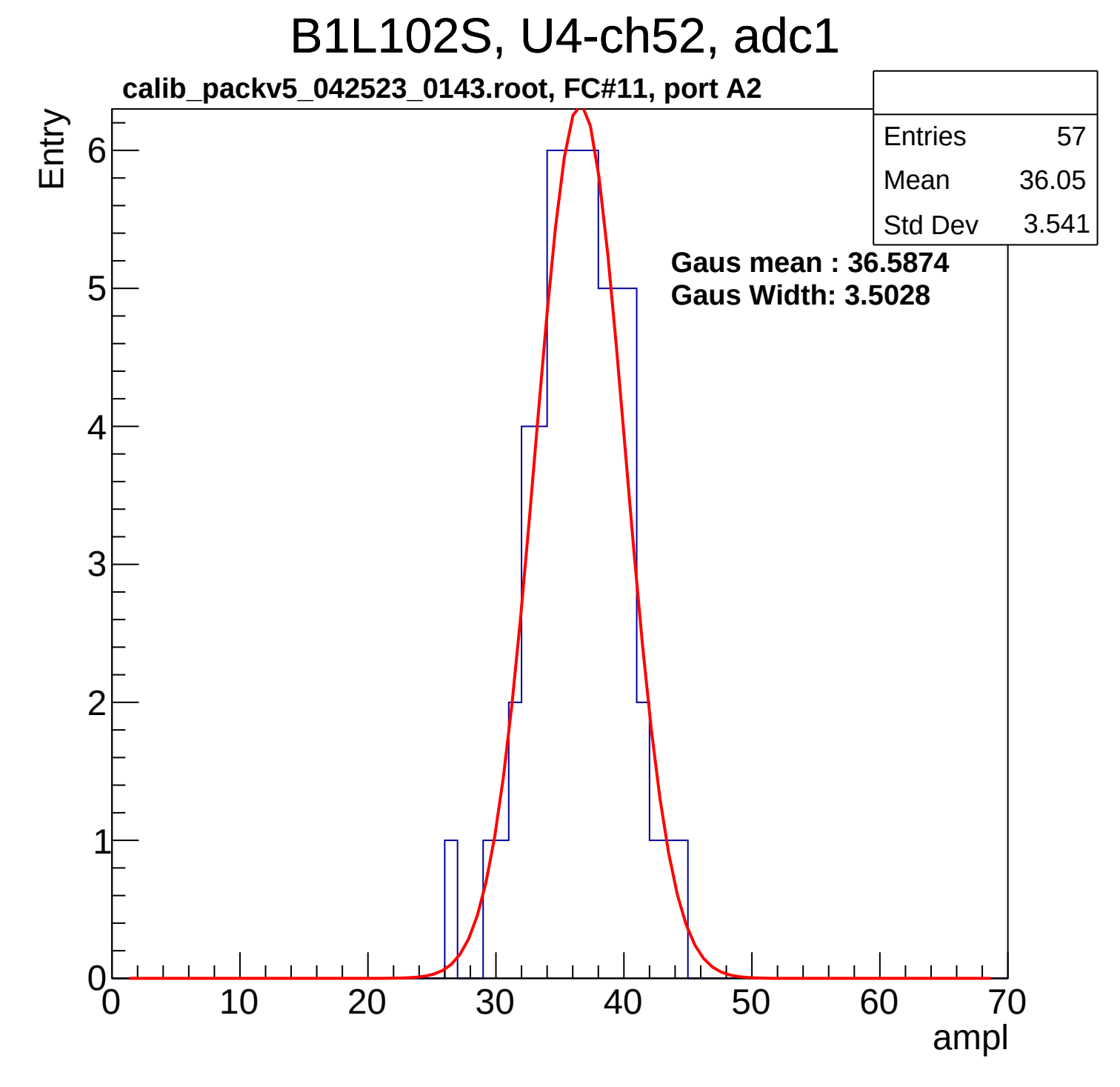
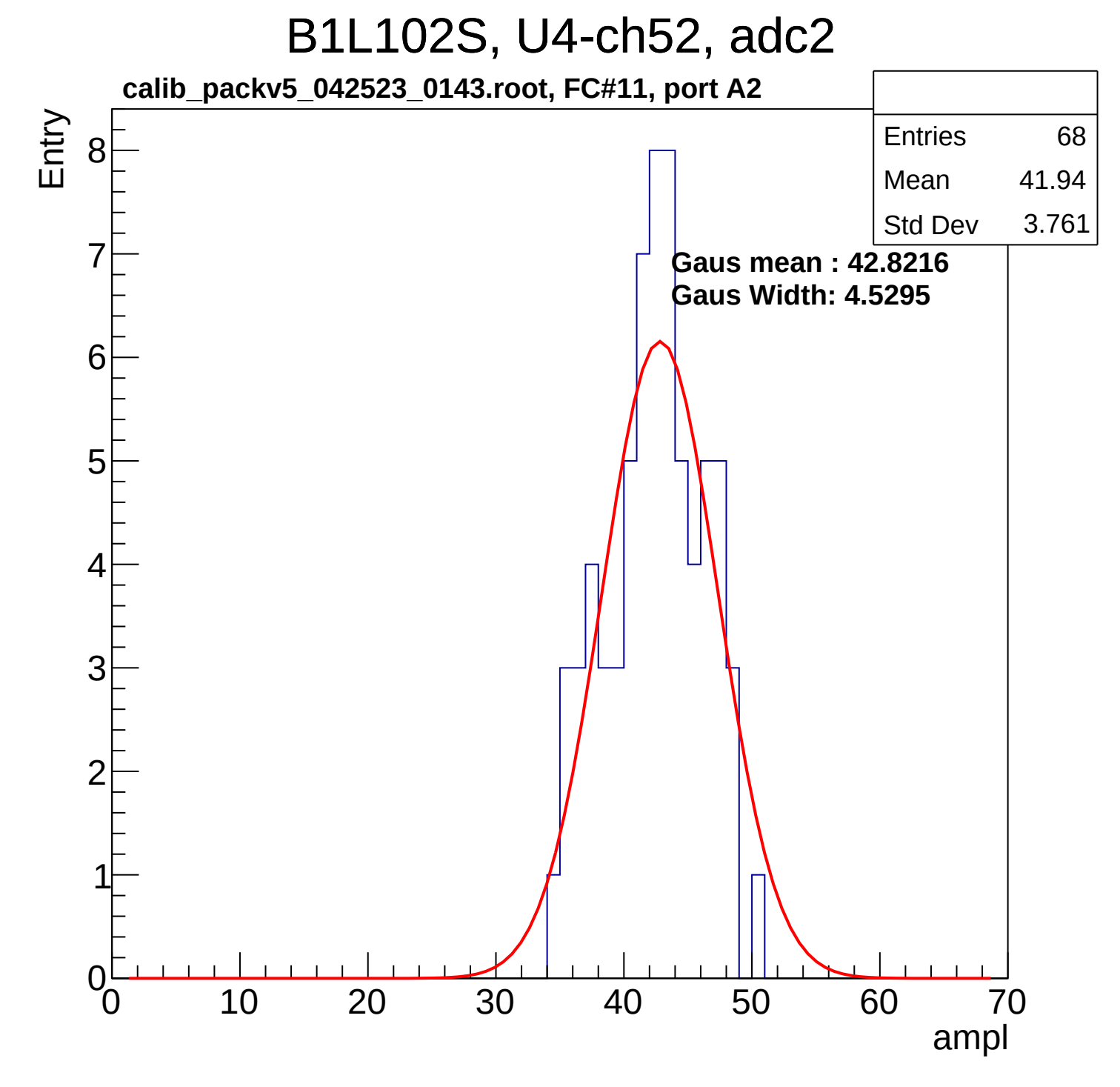
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch52, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 57
Mean 36.05
Std Dev 3.541
Gaus mean : 36.5874
Gaus Width: 3.5028
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L102S, U4-ch52, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 41.94
Std Dev 3.761
Gaus mean : 42.8216
Gaus Width: 4.5295
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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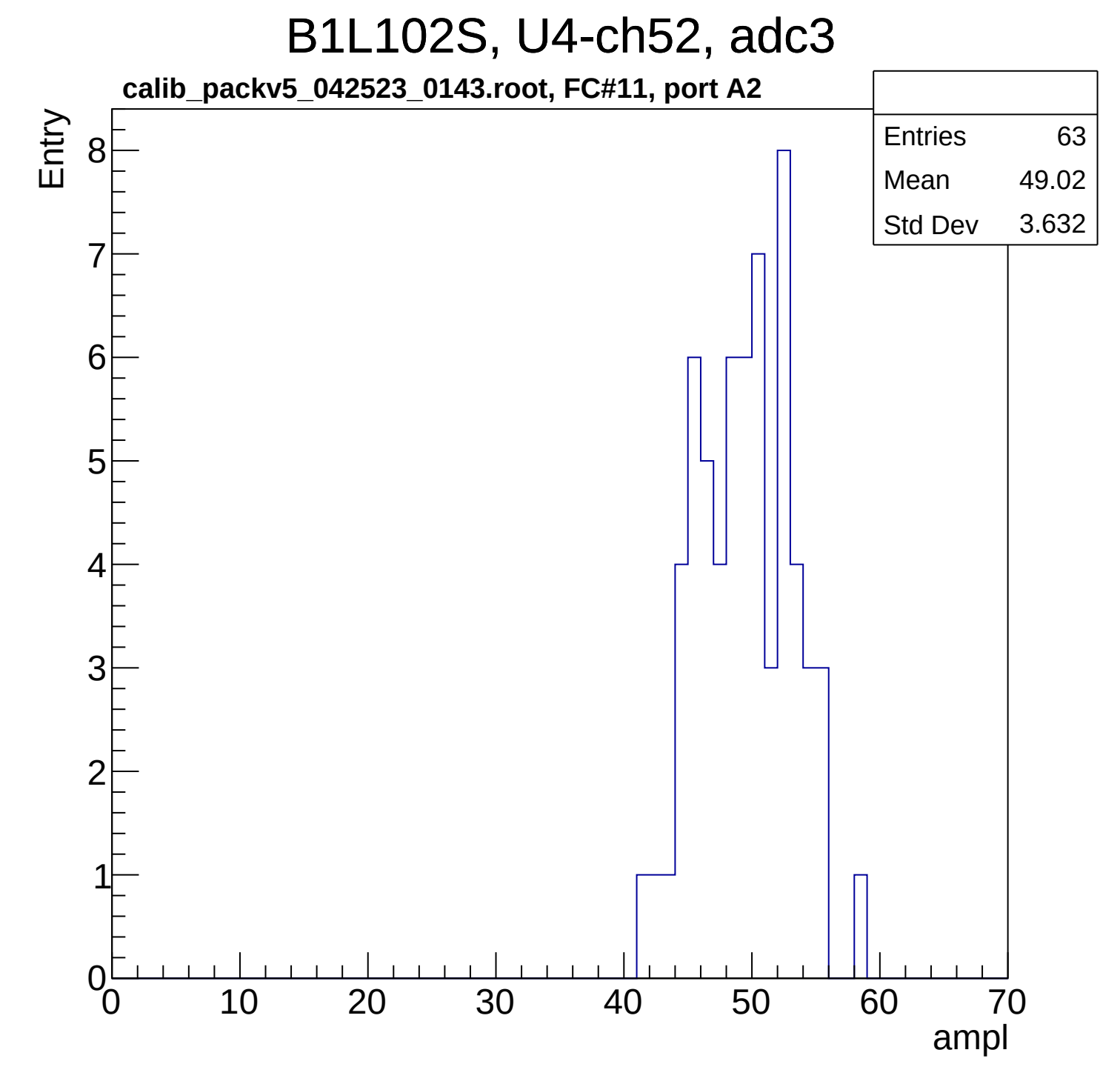
B1L102S, U4-ch52, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 49.02
Std Dev 3.632
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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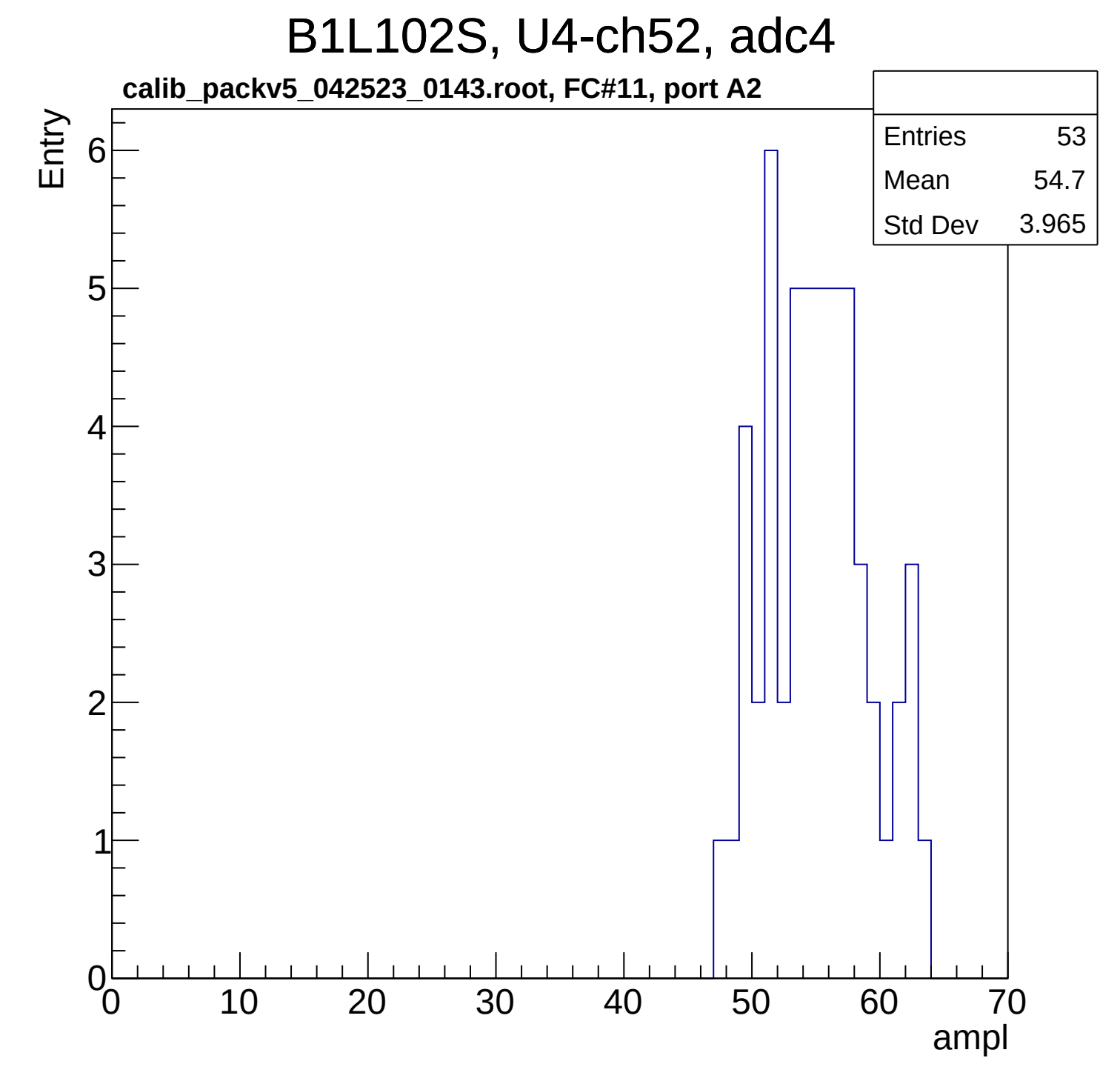
B1L102S, U4-ch52, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 54.7
Std Dev 3.965
Entry
ampl
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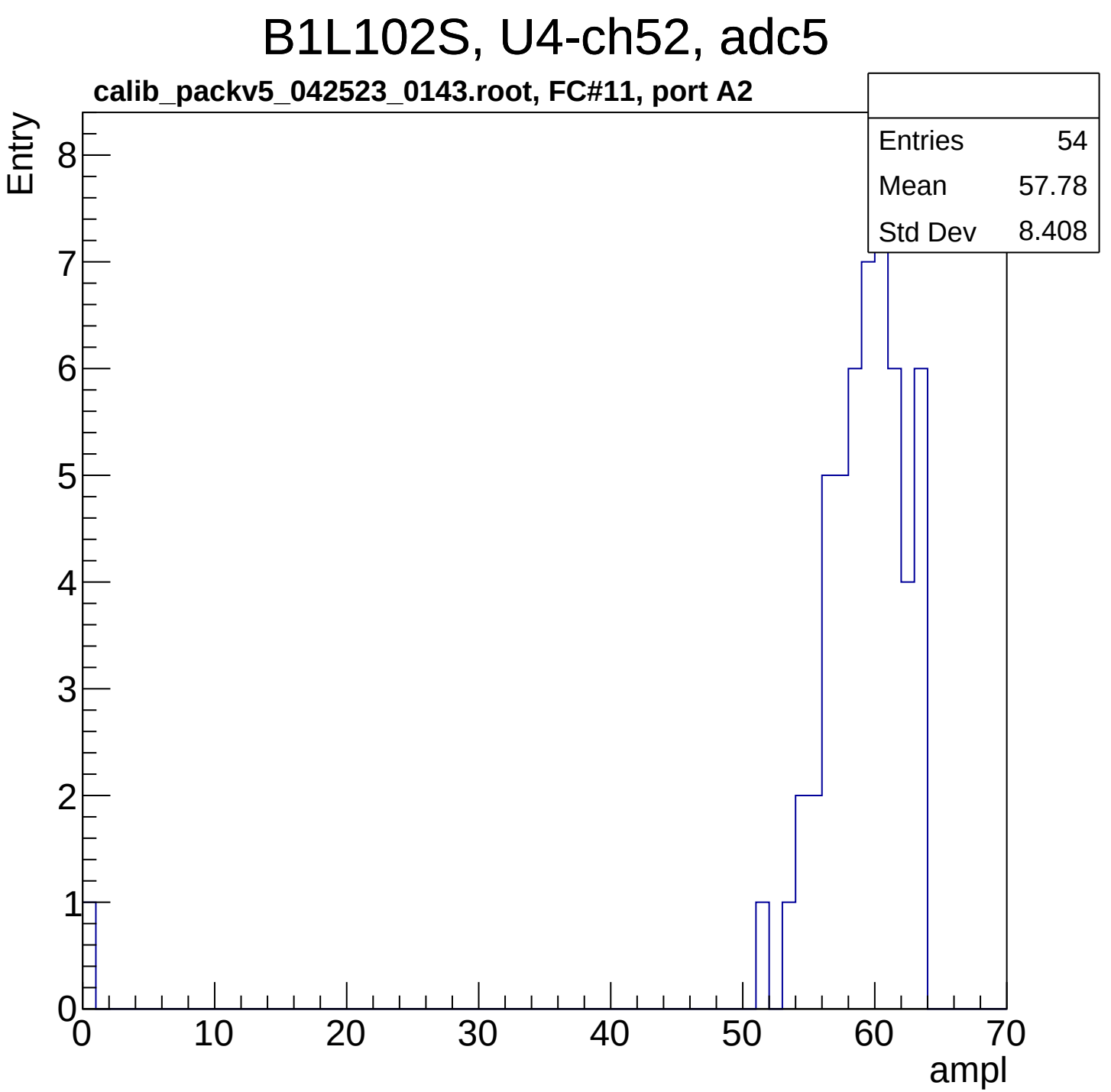
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L102S, U4-ch52, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 57.78
Std Dev 8.408
Entry
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8
0
10
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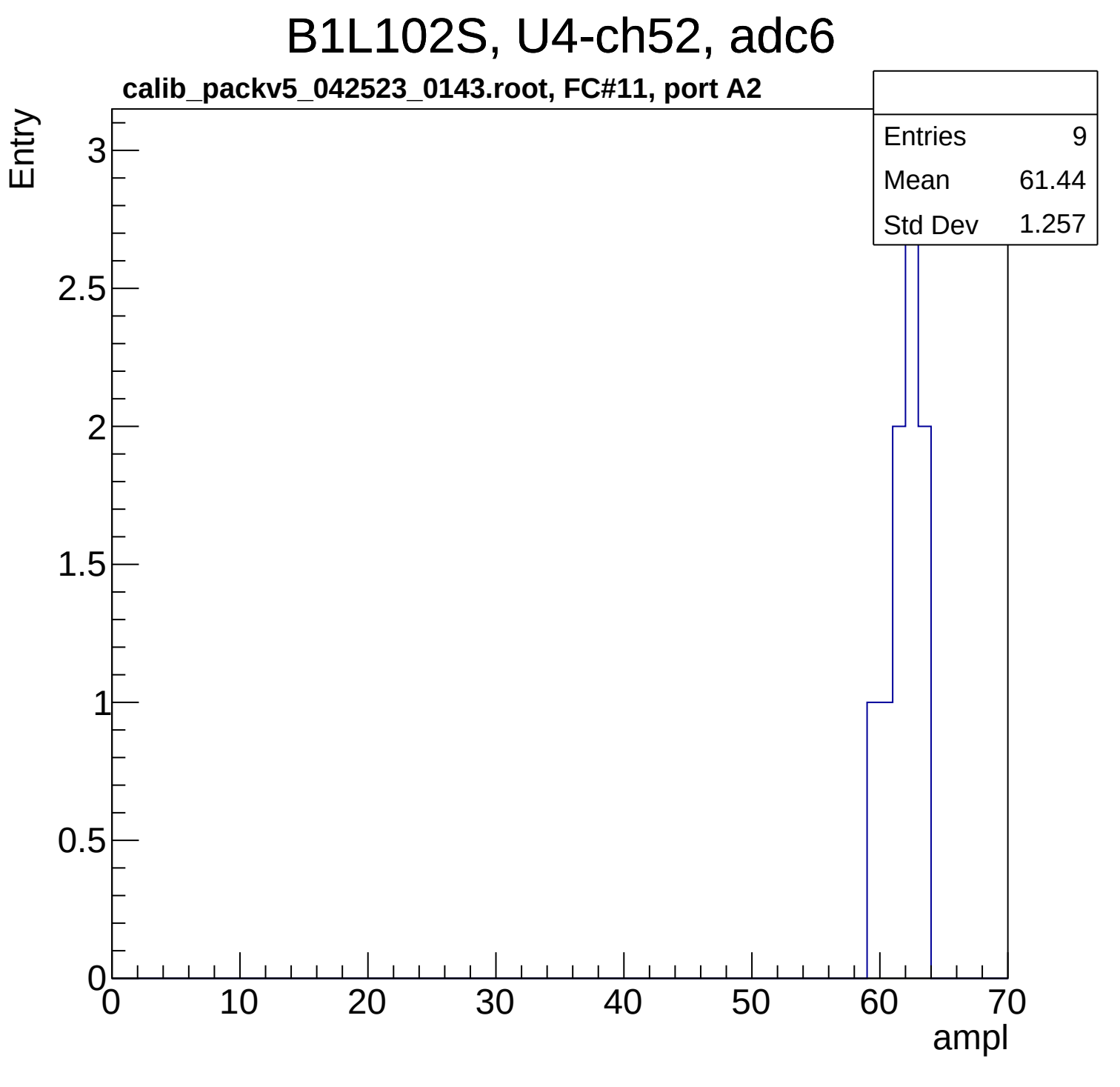
30
40
50
60
70
ampl


B1L102S, U4-ch52, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 9
Mean 61.44
Std Dev 1.257
Entry
ampl
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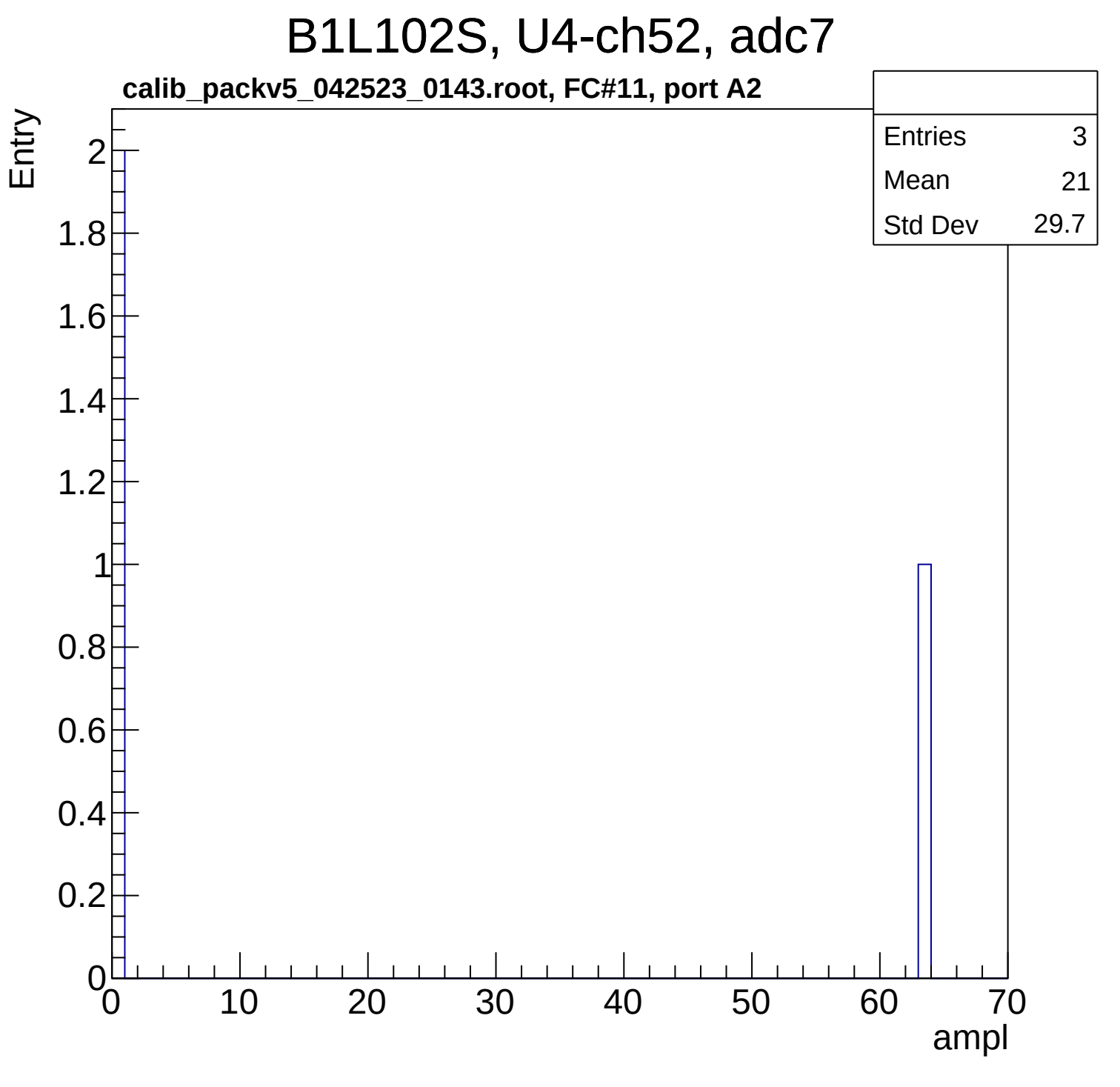
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U4-ch52, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 21
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
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40
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60
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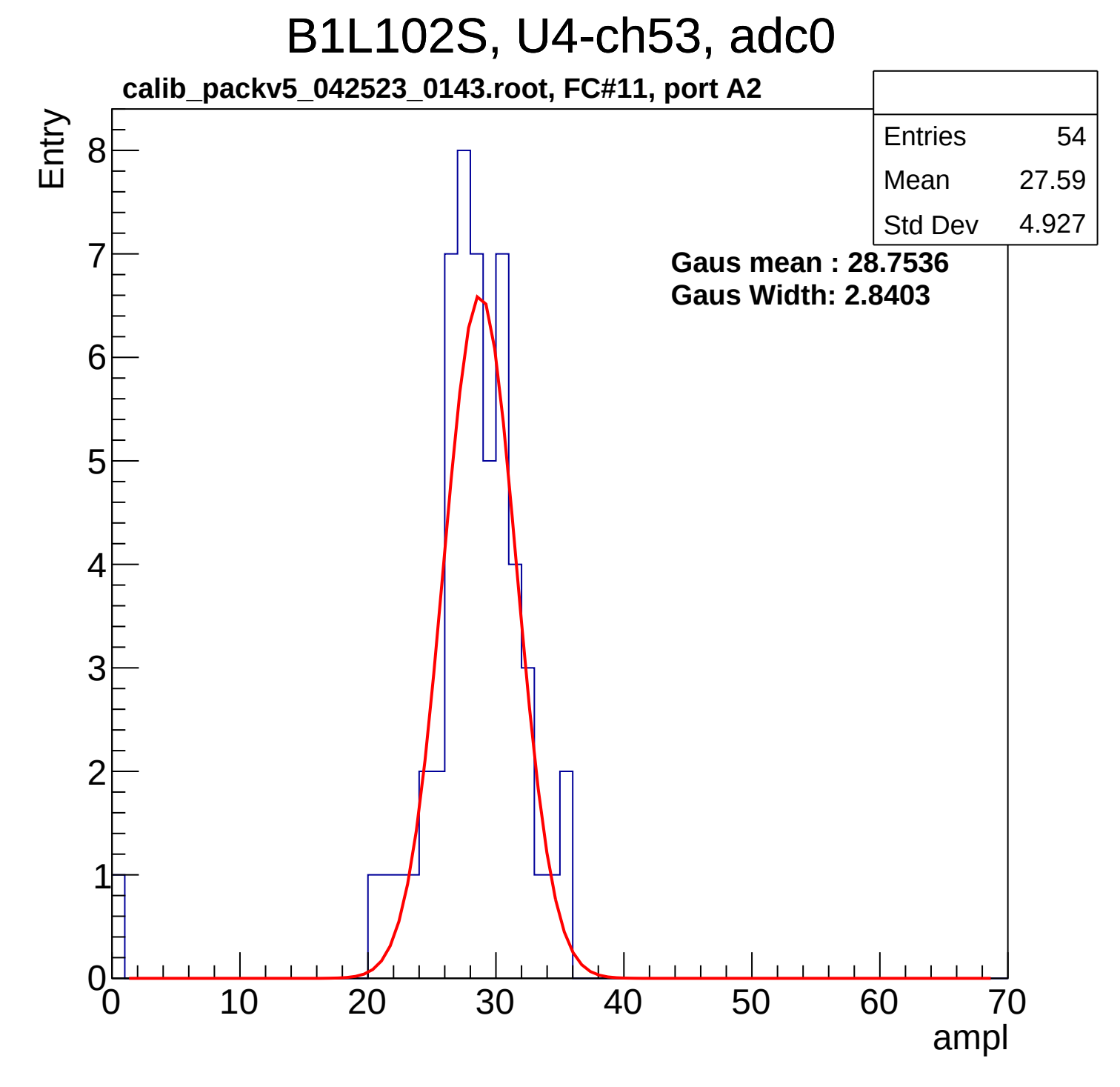
B1L102S, U4-ch53, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 27.59
Std Dev 4.927
Gaus mean : 28.7536
Gaus Width: 2.8403
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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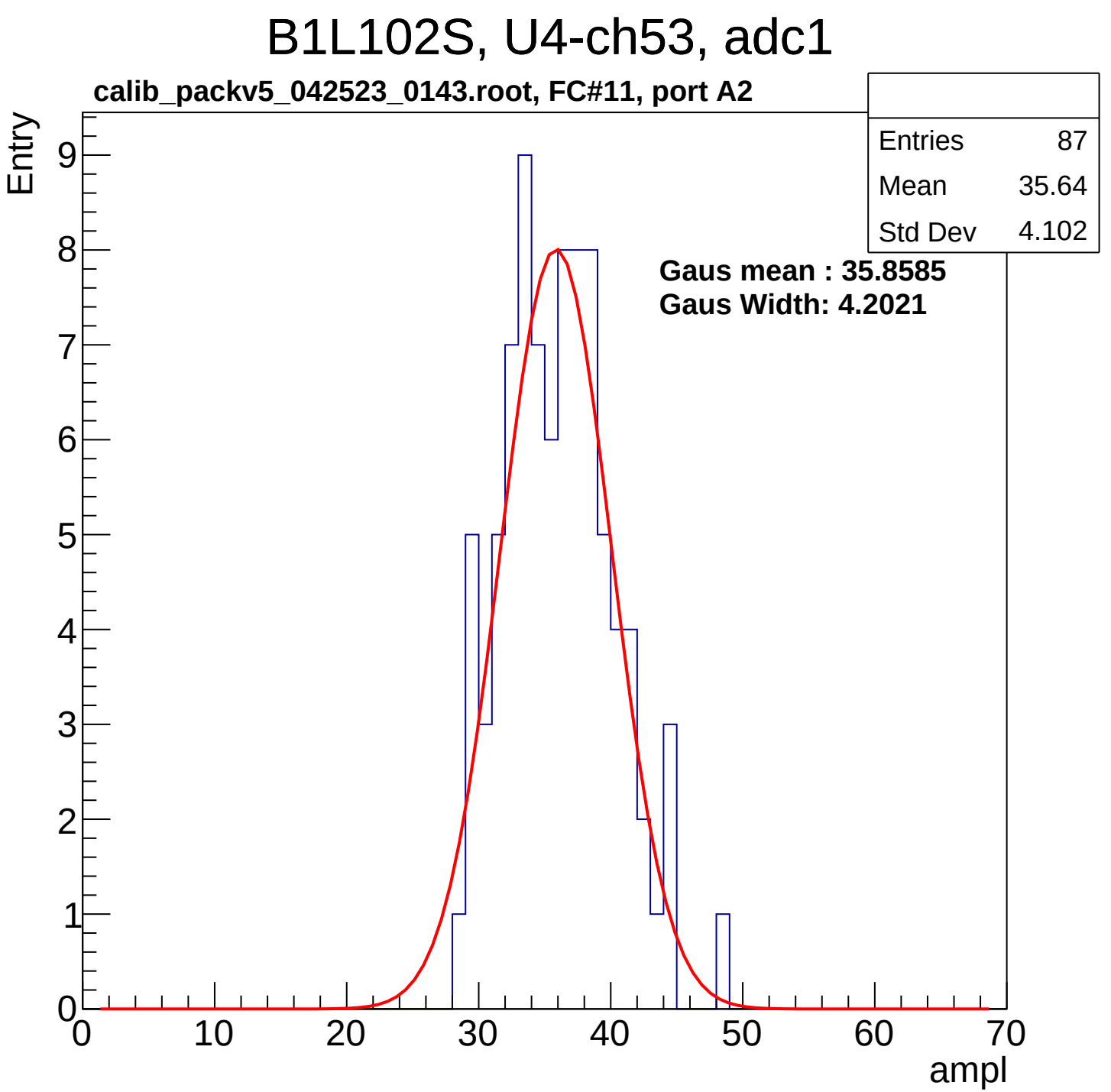
B1L102S, U4-ch53, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 87
Mean 35.64
Std Dev 4.102
Gaus mean : 35.8585
Gaus Width: 4.2021
Entry
ampl
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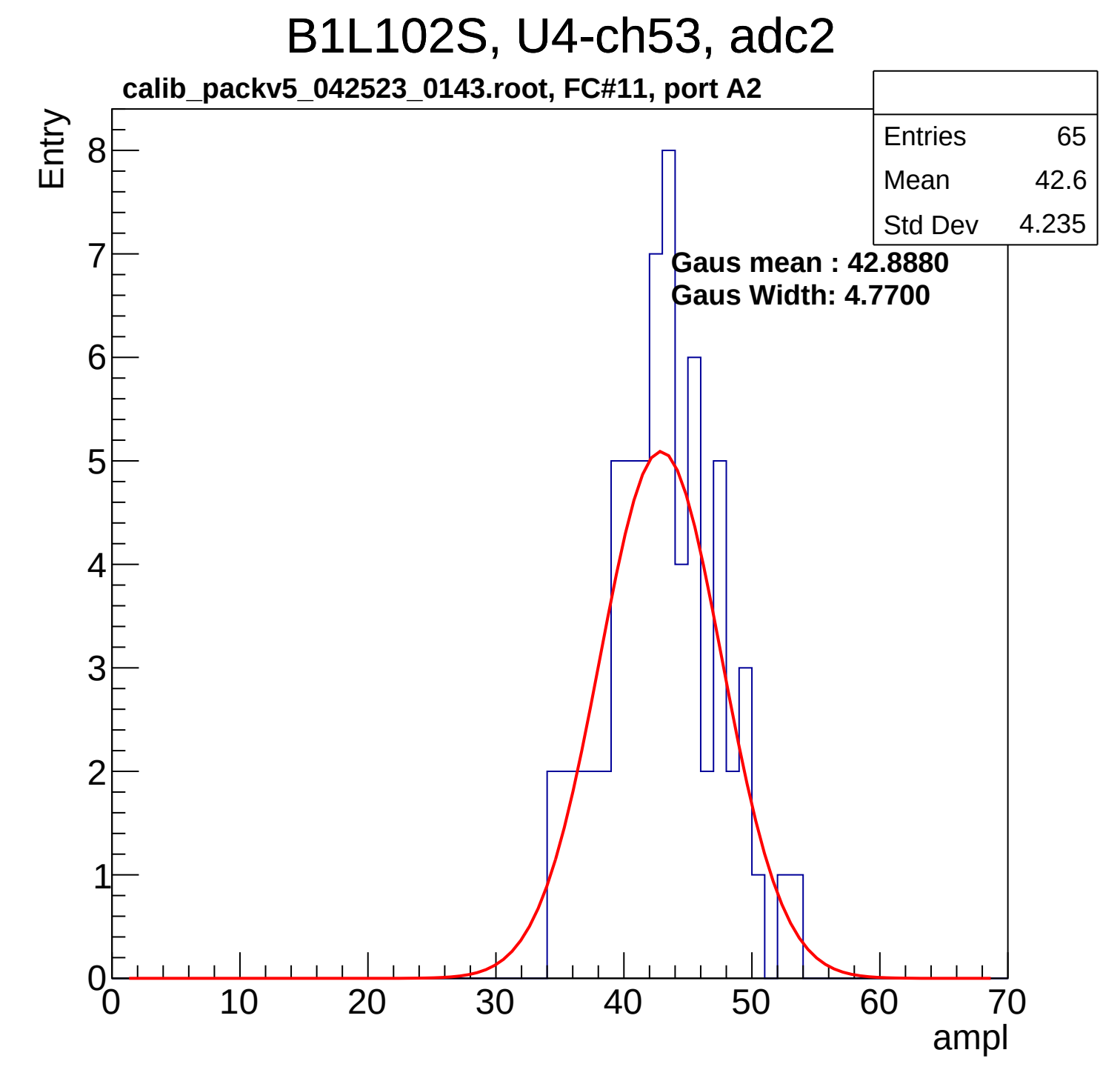
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch53, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 42.6
Std Dev 4.235
Gaus mean : 42.8880
Gaus Width: 4.7700
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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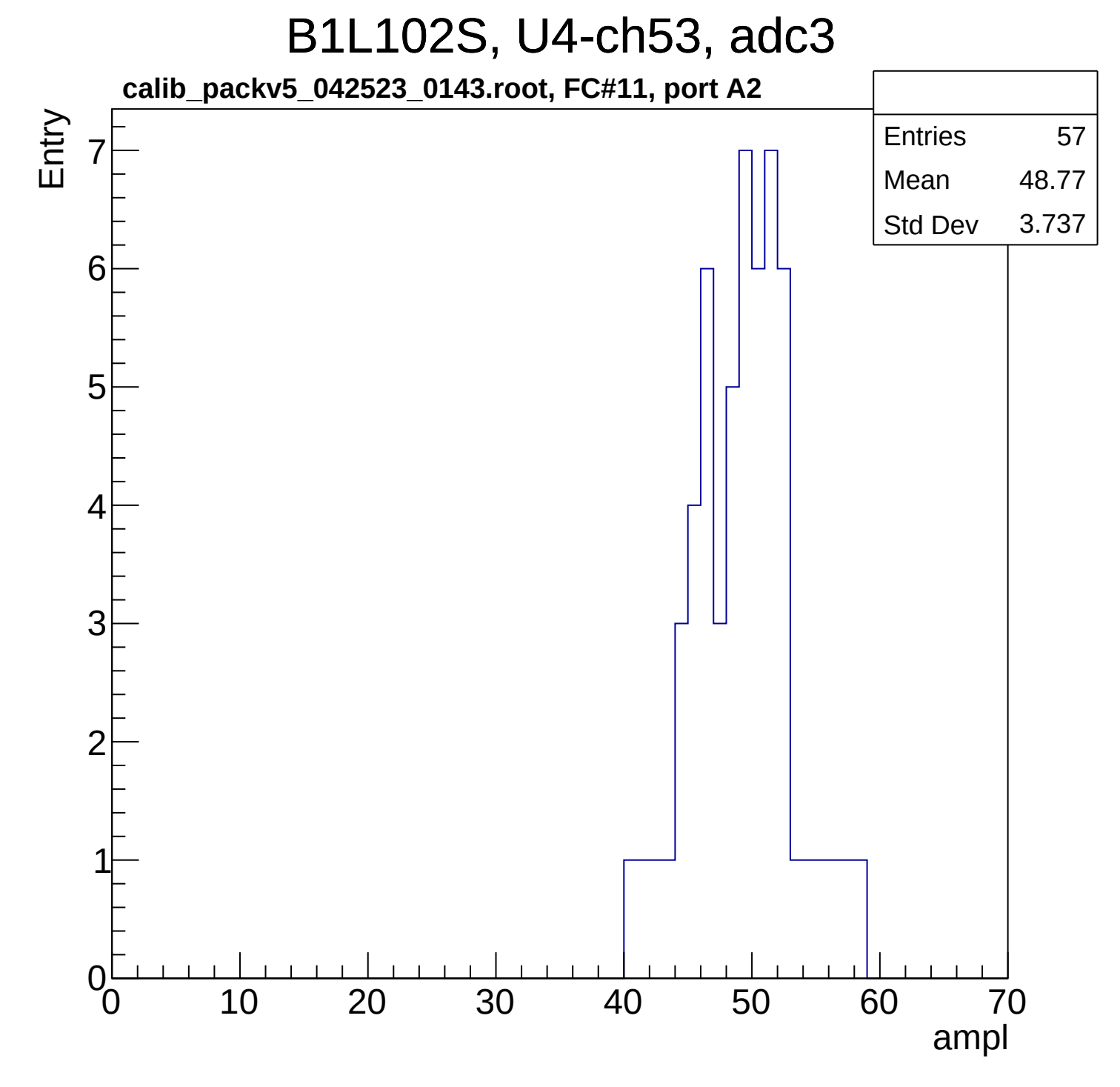
B1L102S, U4-ch53, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 57
Mean 48.77
Std Dev 3.737
Entry
ampl
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2
3
4
5
6
7
0
10
20
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40
50
60
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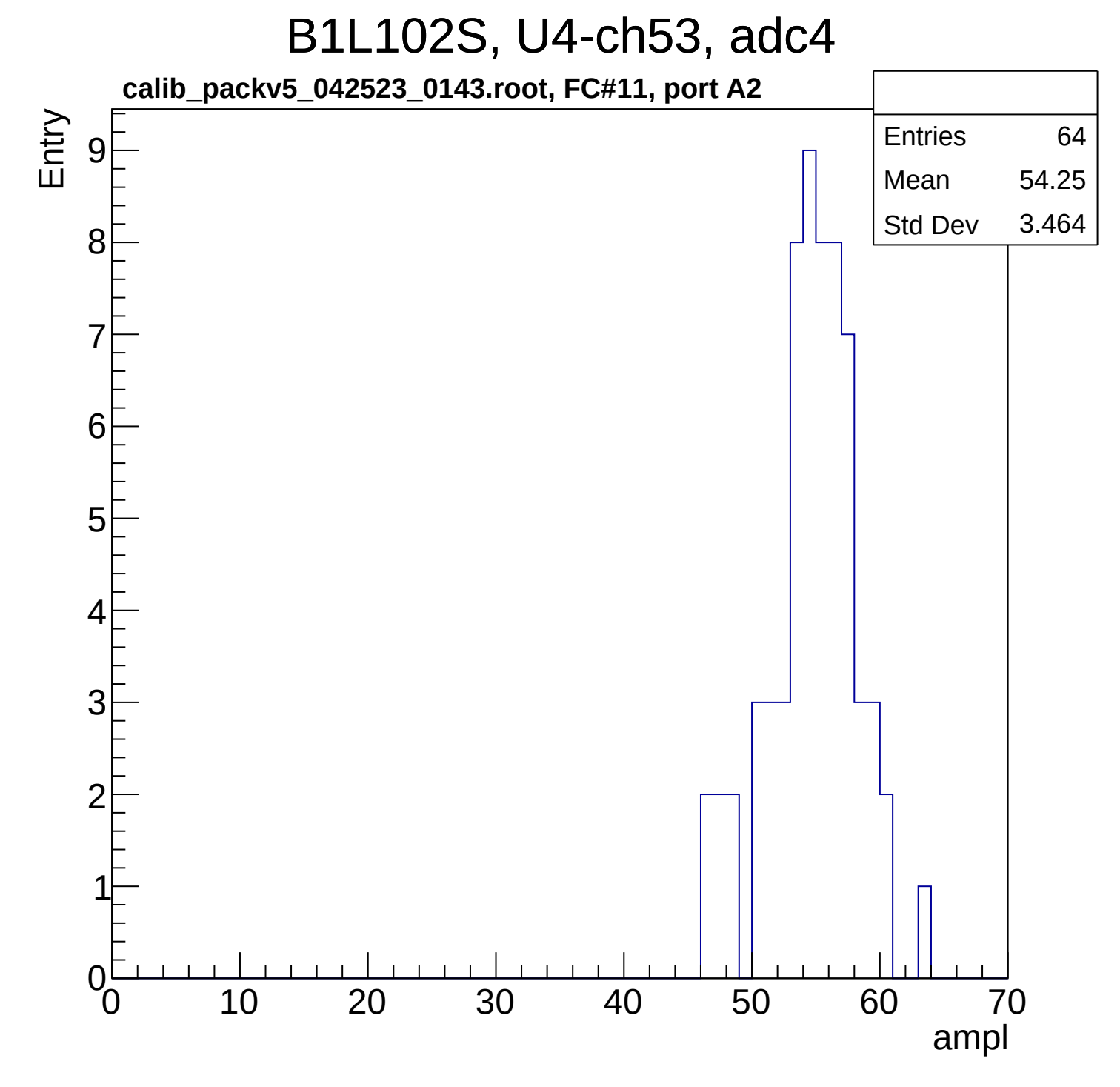
B1L102S, U4-ch53, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 54.25
Std Dev 3.464
Entry
ampl
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3
4
5
6
7
8
9
0
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20
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40
50
60
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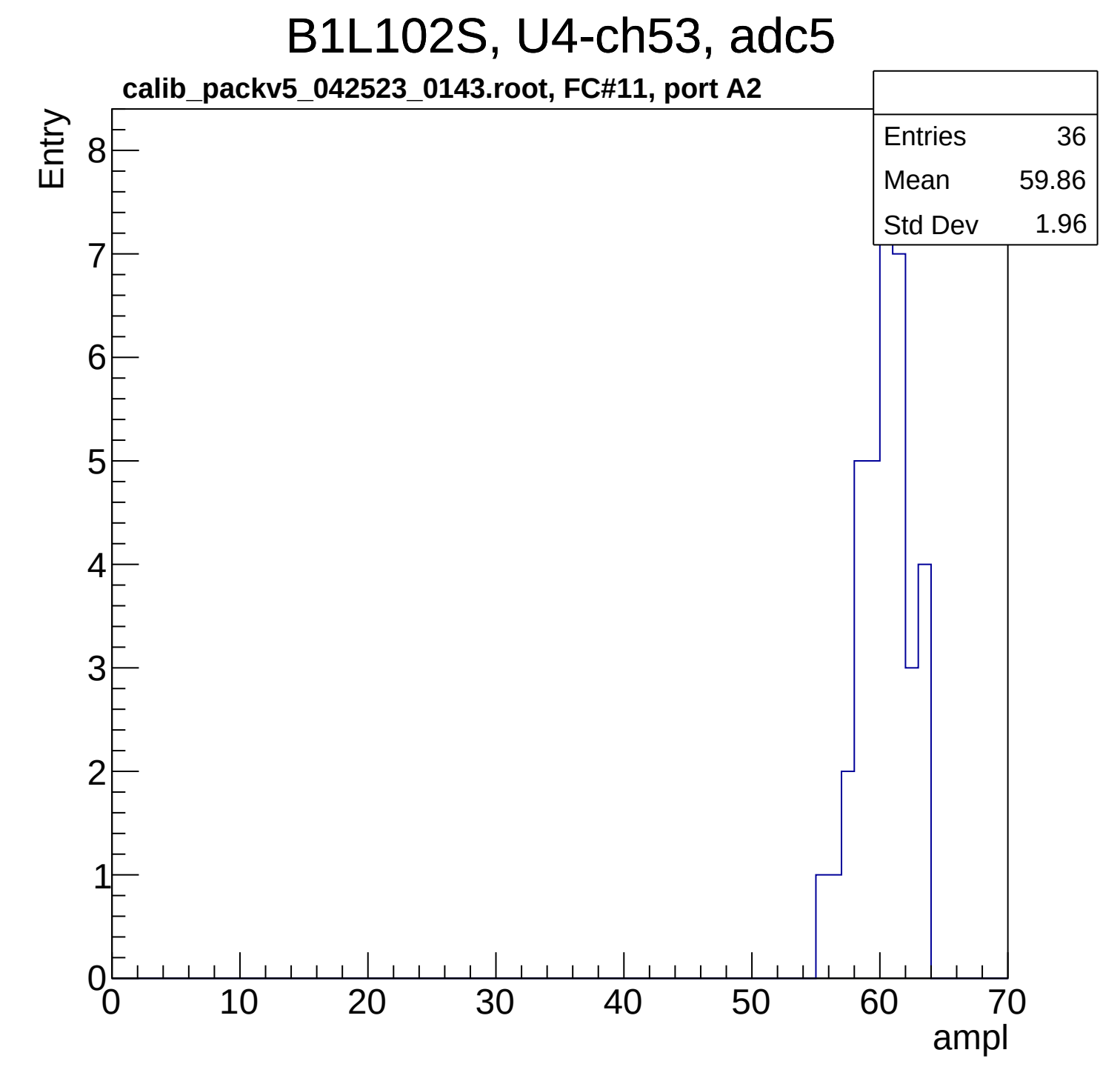
B1L102S, U4-ch53, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 36
Mean 59.86
Std Dev 1.96
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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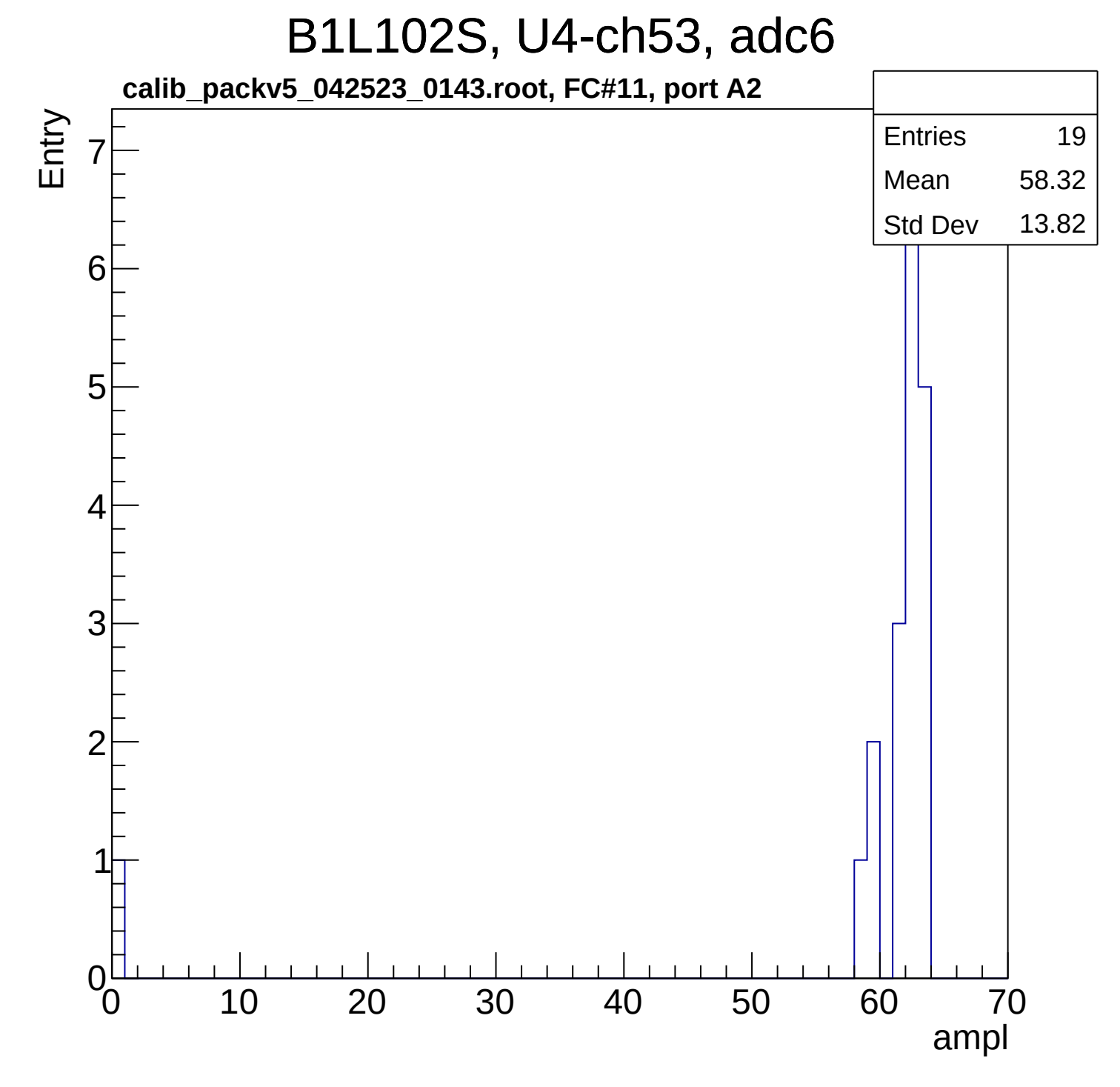
B1L102S, U4-ch53, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 19
Mean 58.32
Std Dev 13.82
Entry
ampl
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1
2
3
4
5
6
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0
10
20
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40
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60
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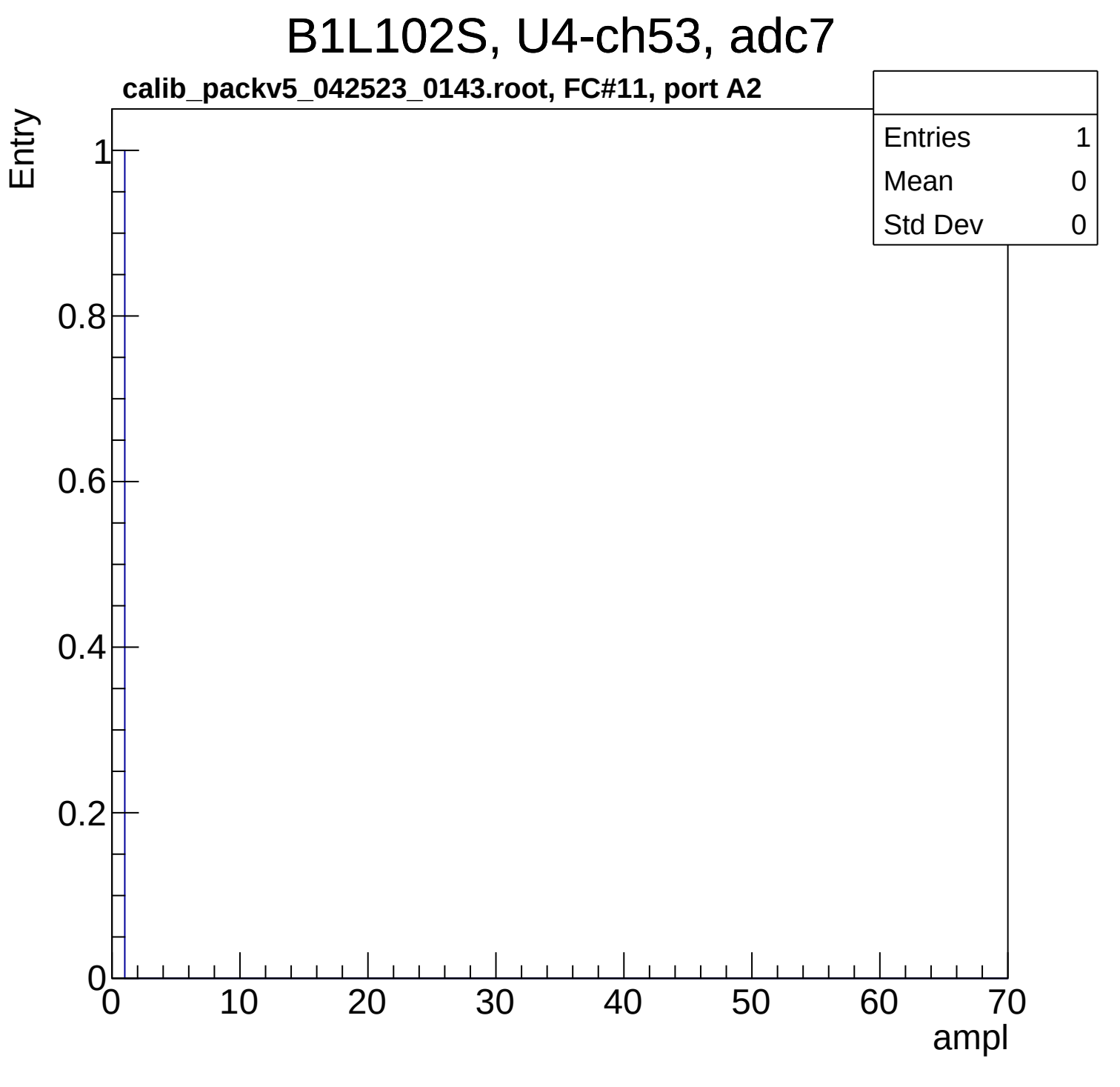
B1L102S, U4-ch53, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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0.6
0.4
0.2
0
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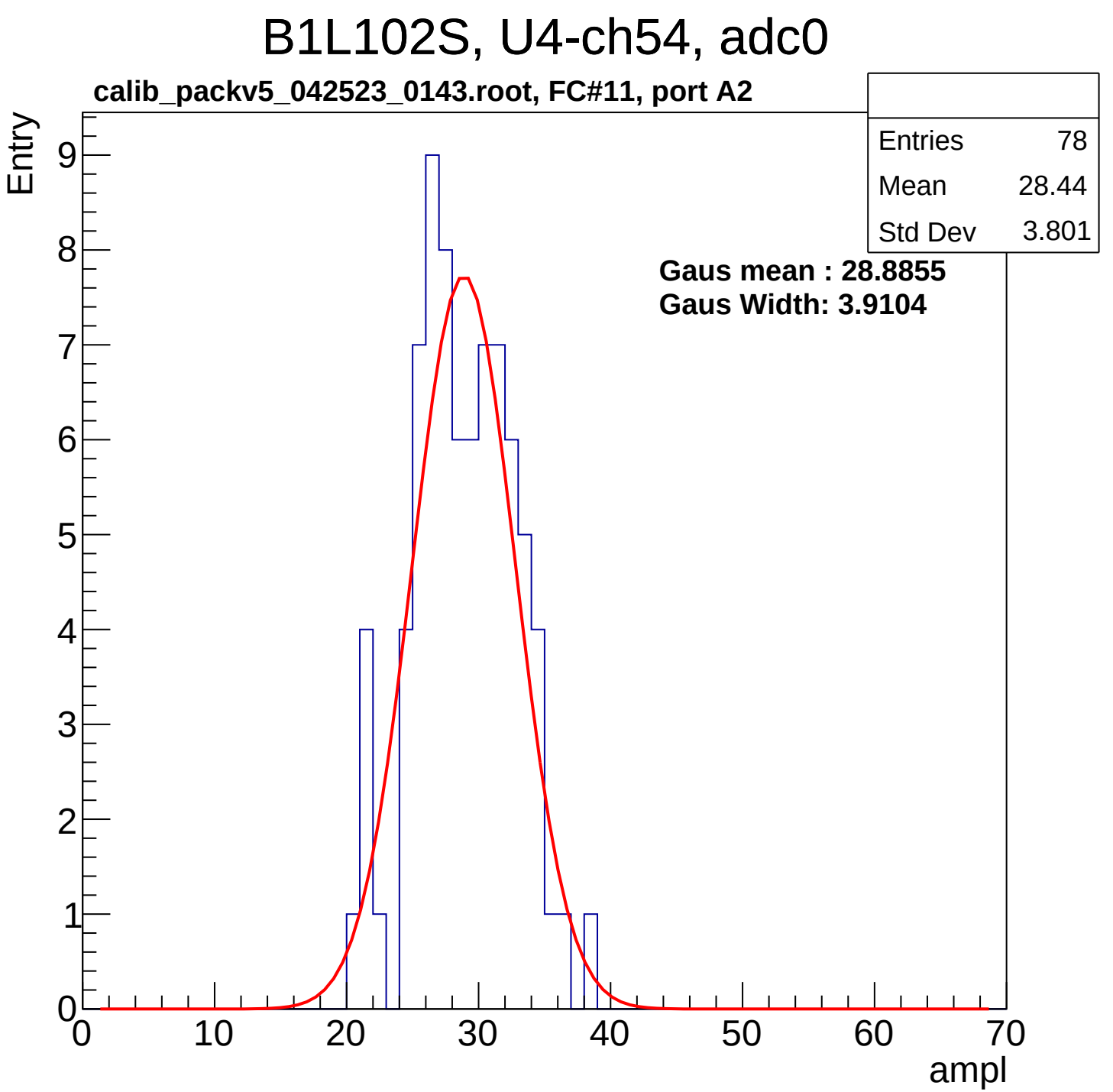
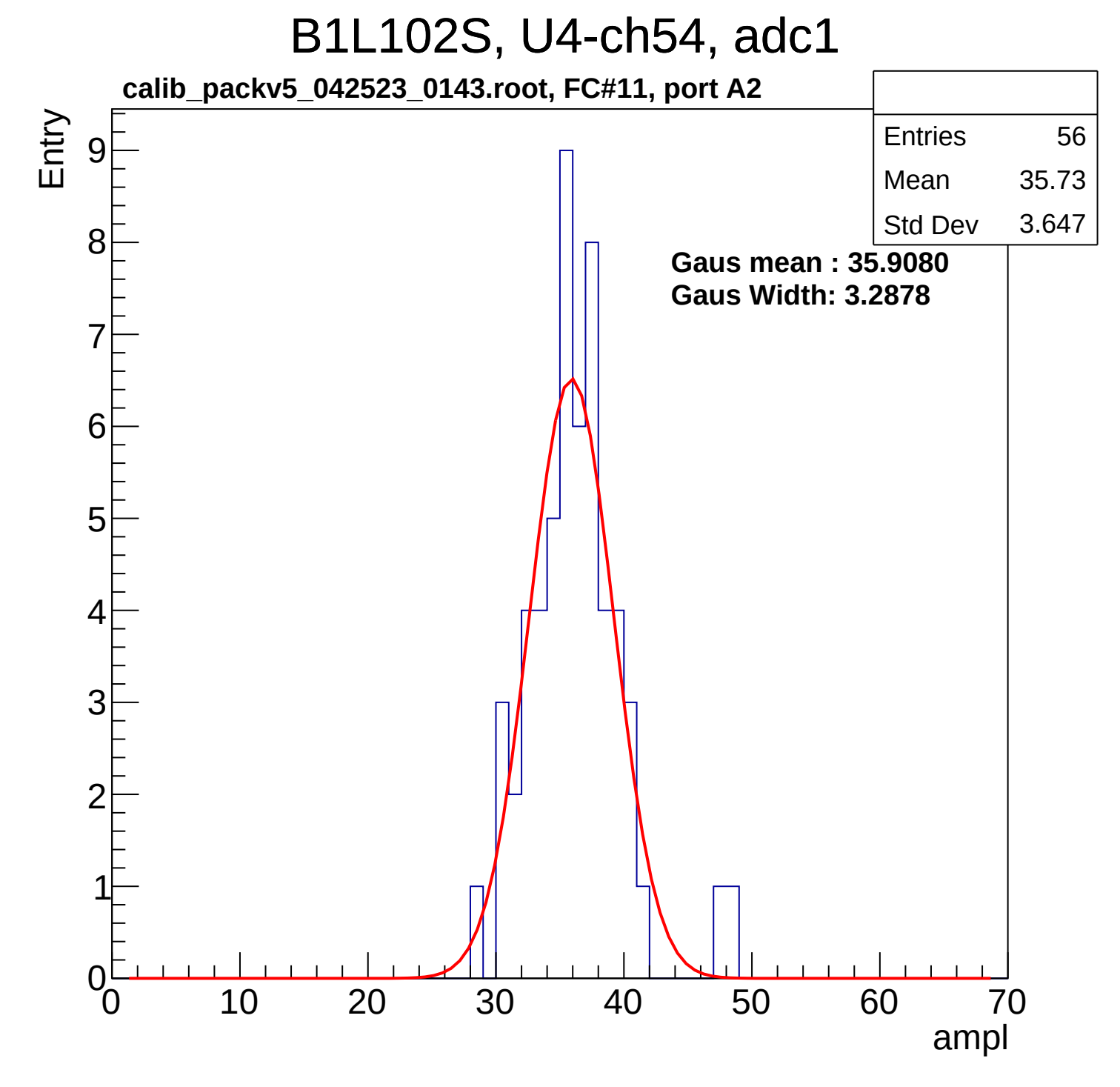
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch54, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 78
Mean 28.44
Std Dev 3.801
Gaus mean : 28.8855
Gaus Width: 3.9104
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch54, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 35.73
Std Dev 3.647
Gaus mean : 35.9080
Gaus Width: 3.2878
Entry
ampl
0
1
2
3
4
5
6
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8
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0
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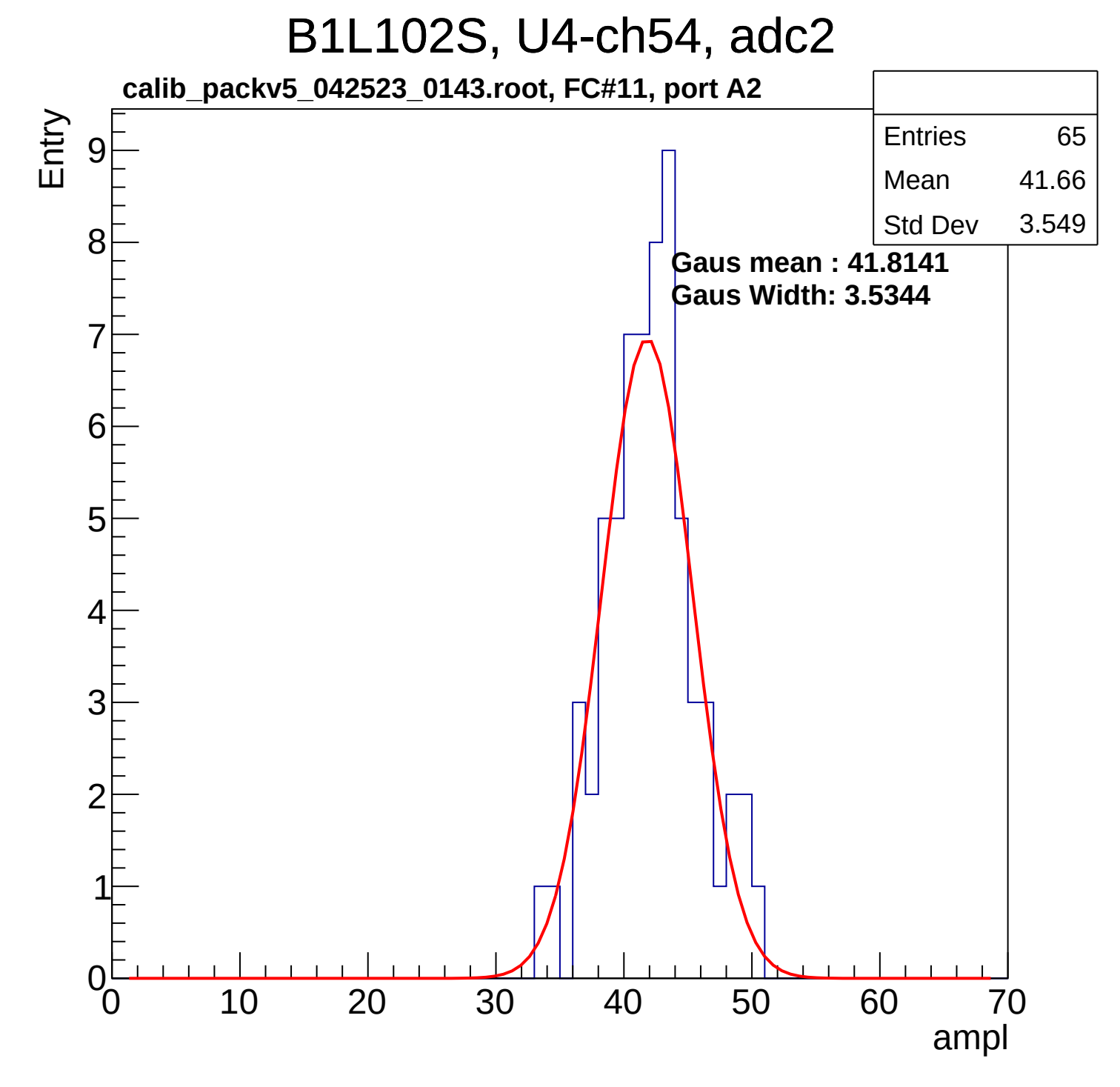
B1L102S, U4-ch54, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 41.66
Std Dev 3.549
Gaus mean : 41.8141
Gaus Width: 3.5344
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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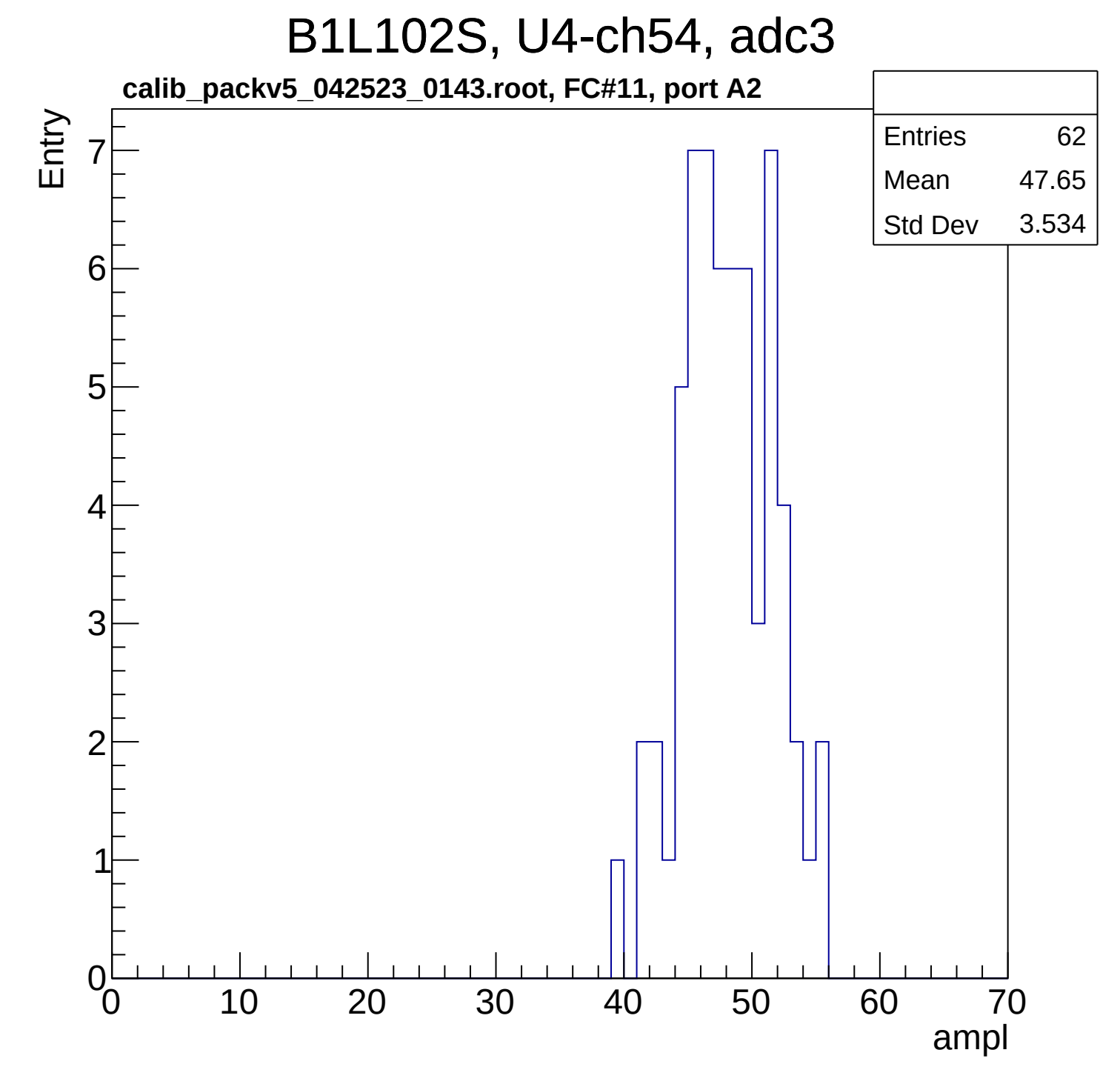
B1L102S, U4-ch54, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 47.65
Std Dev 3.534
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
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60
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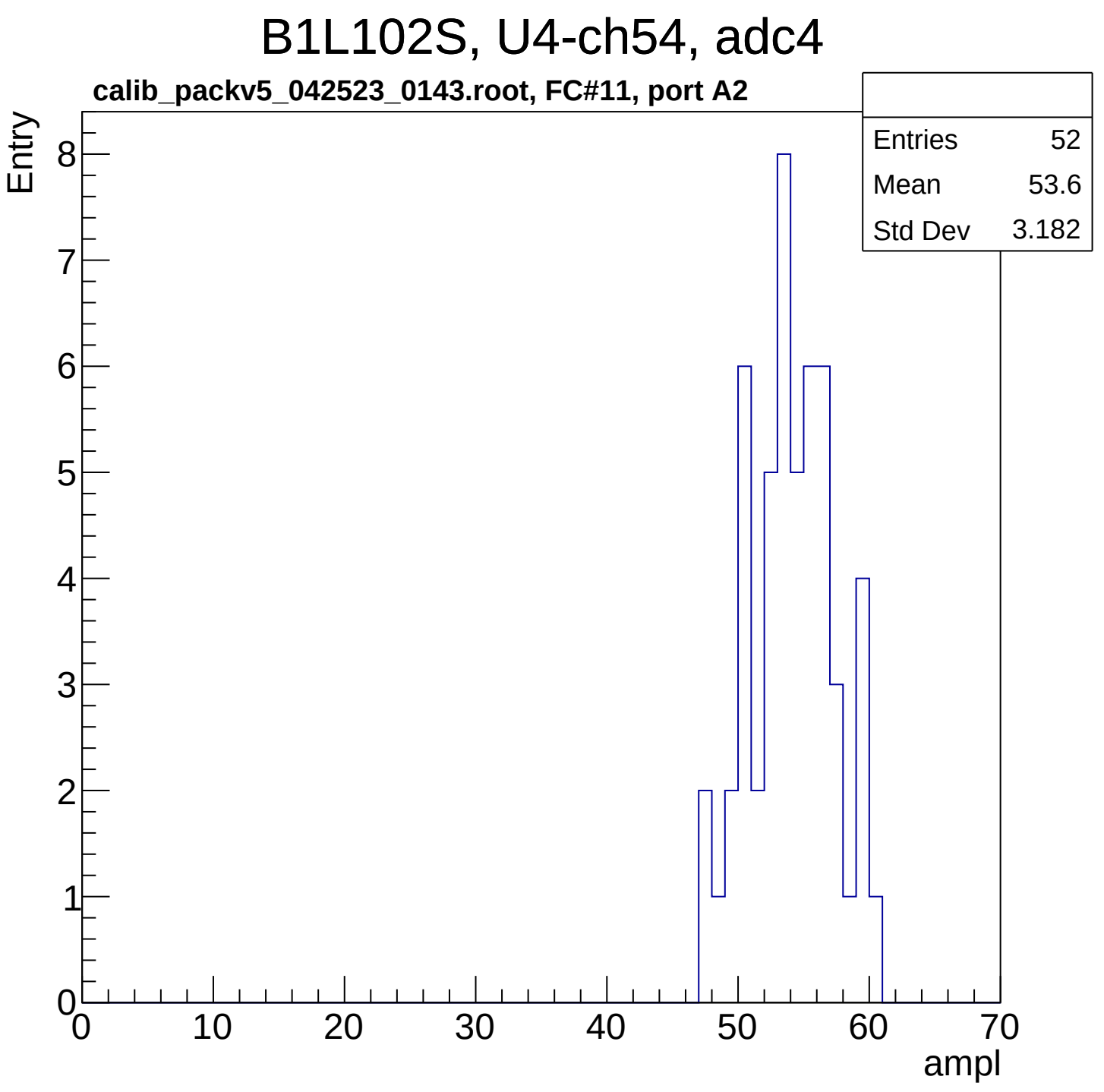
B1L102S, U4-ch54, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 52
Mean 53.6
Std Dev 3.182
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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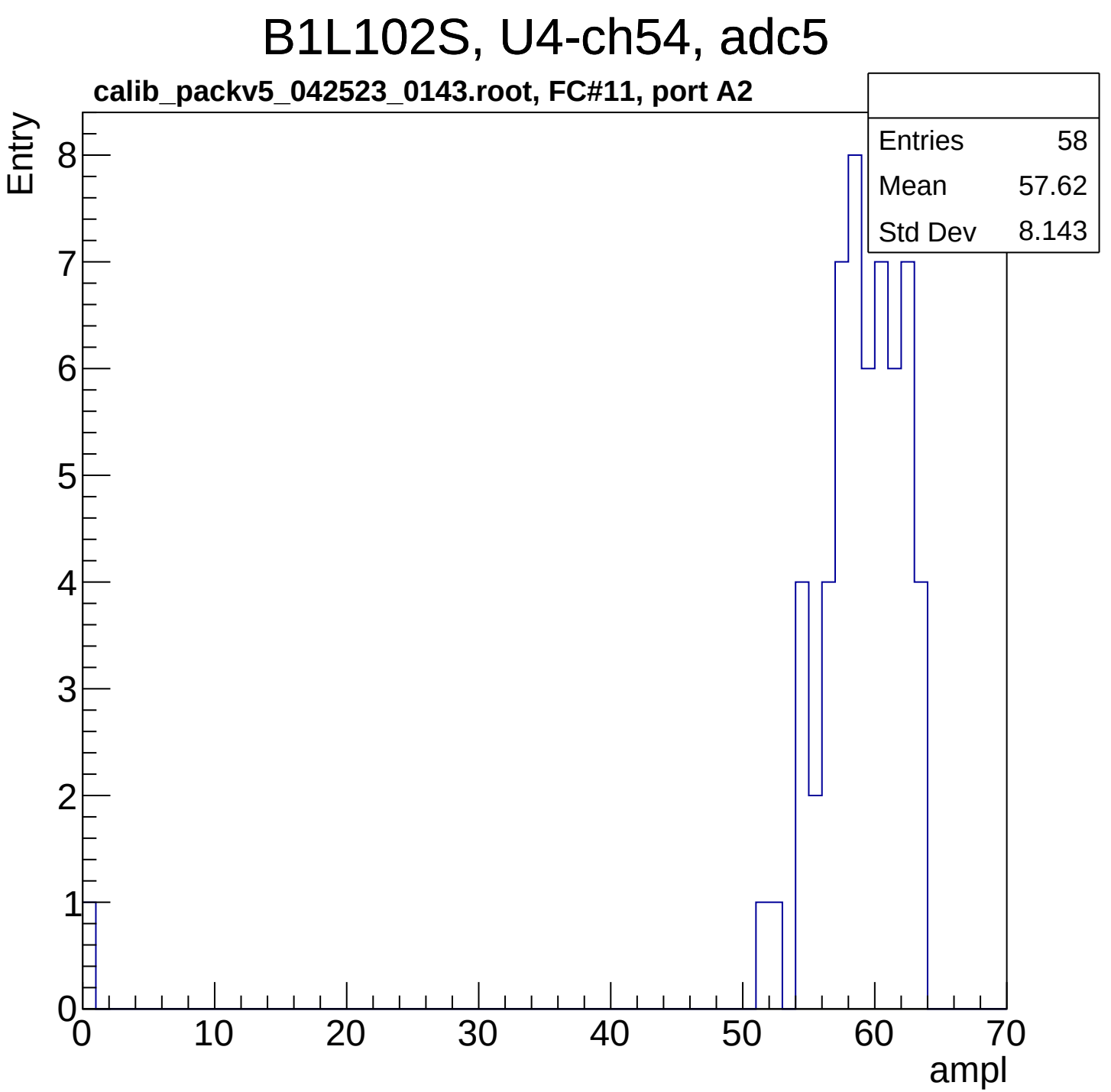
B1L102S, U4-ch54, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 57.62
Std Dev 8.143
Entry
ampl
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1
2
3
4
5
6
7
8
0
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30
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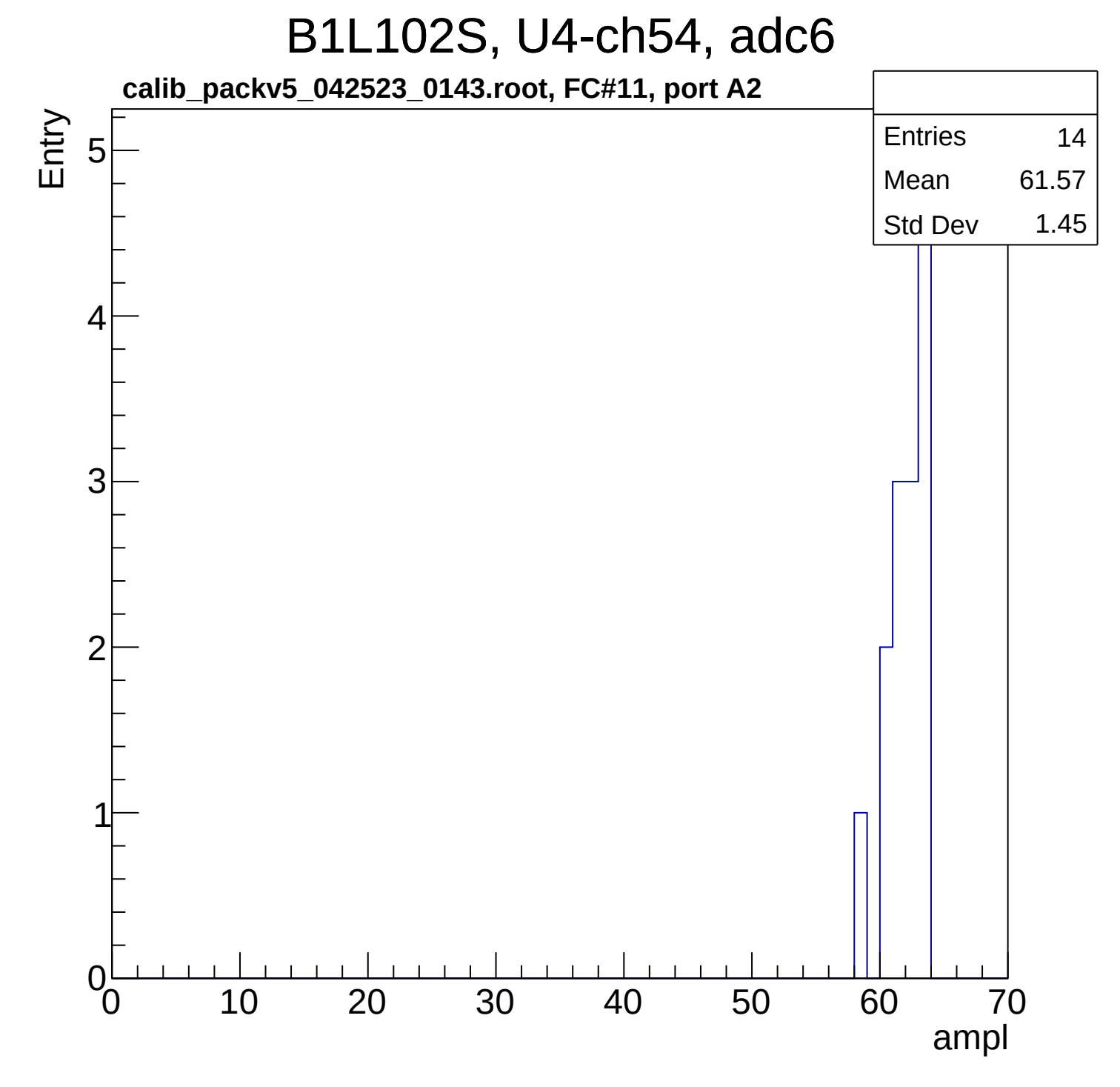
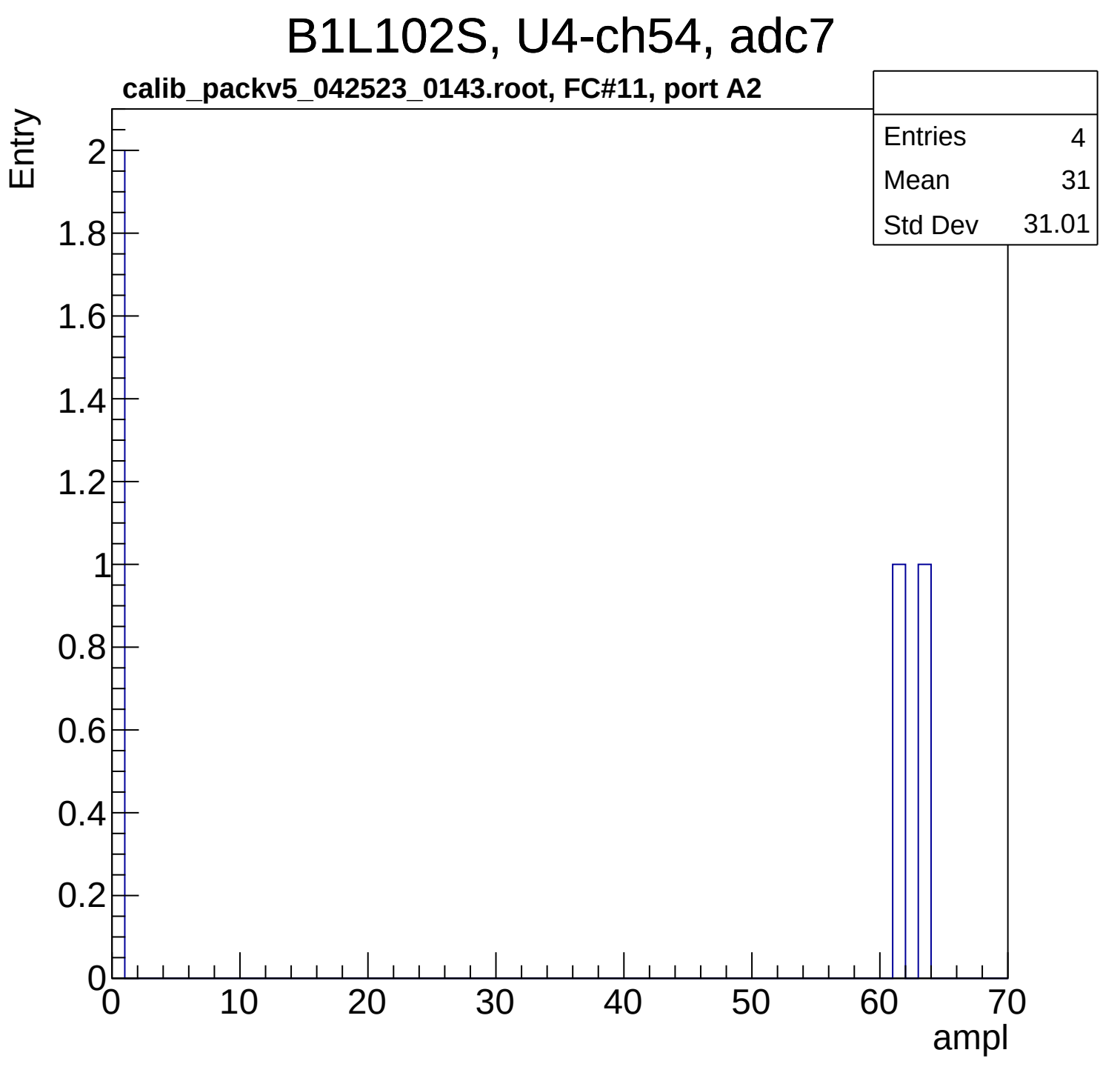

B1L102S, U4-ch54, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 14
Mean 61.57
Std Dev 1.45
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch54, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 4
Mean 31
Std Dev 31.01
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
50
60
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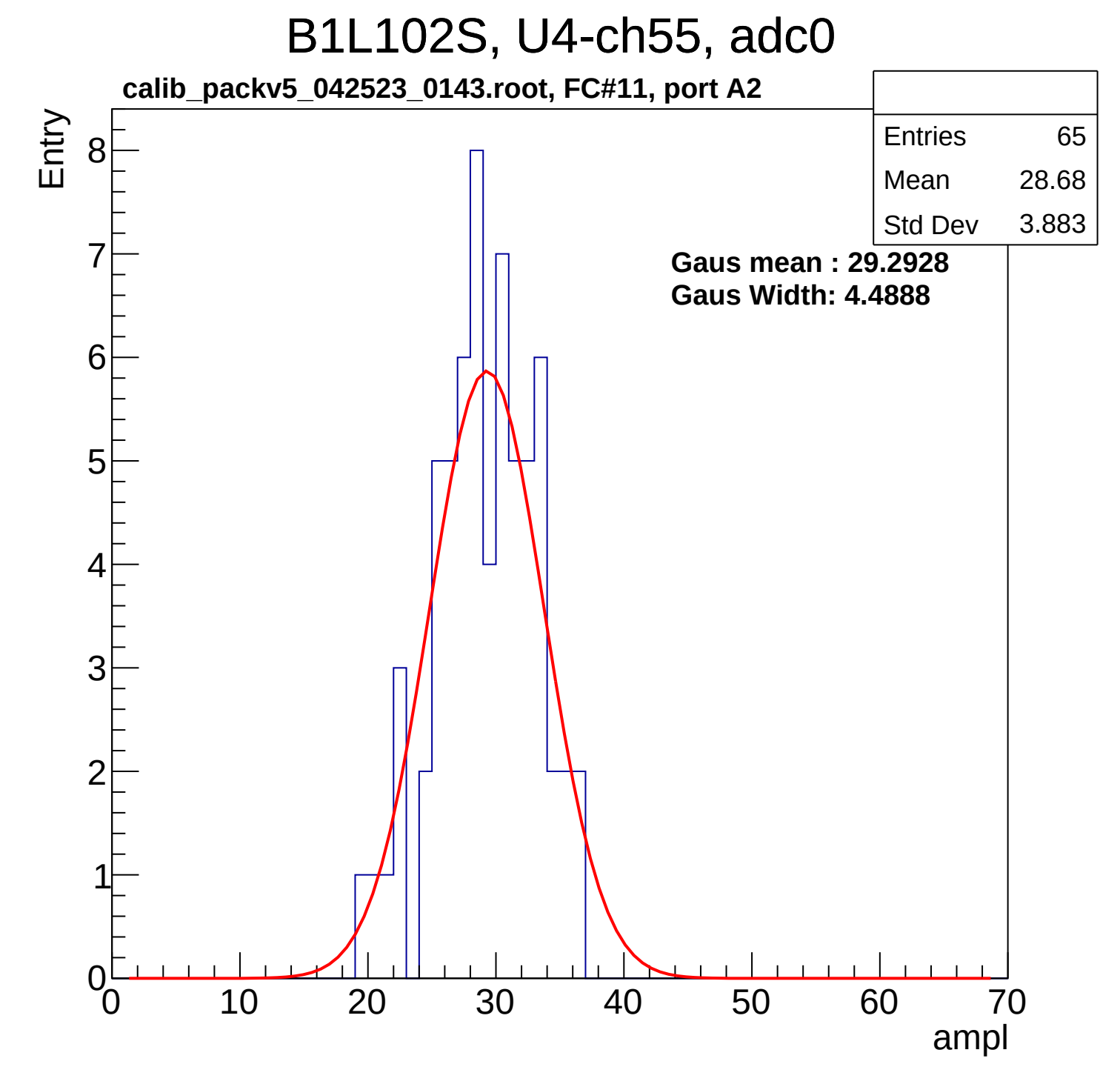
B1L102S, U4-ch55, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 28.68
Std Dev 3.883
Gaus mean : 29.2928
Gaus Width: 4.4888
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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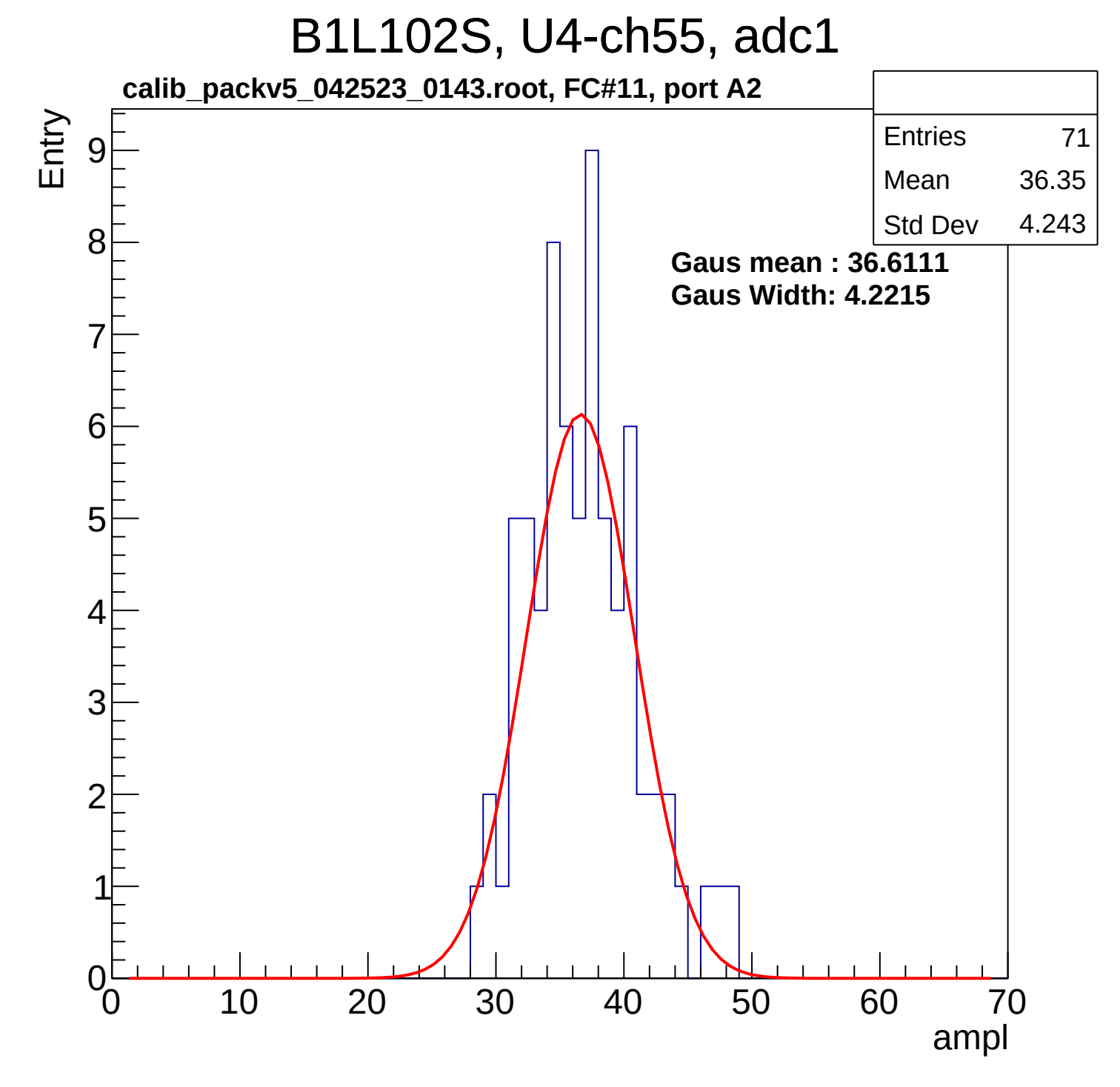
B1L102S, U4-ch55, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 36.35
Std Dev 4.243
Gaus mean : 36.6111
Gaus Width: 4.2215
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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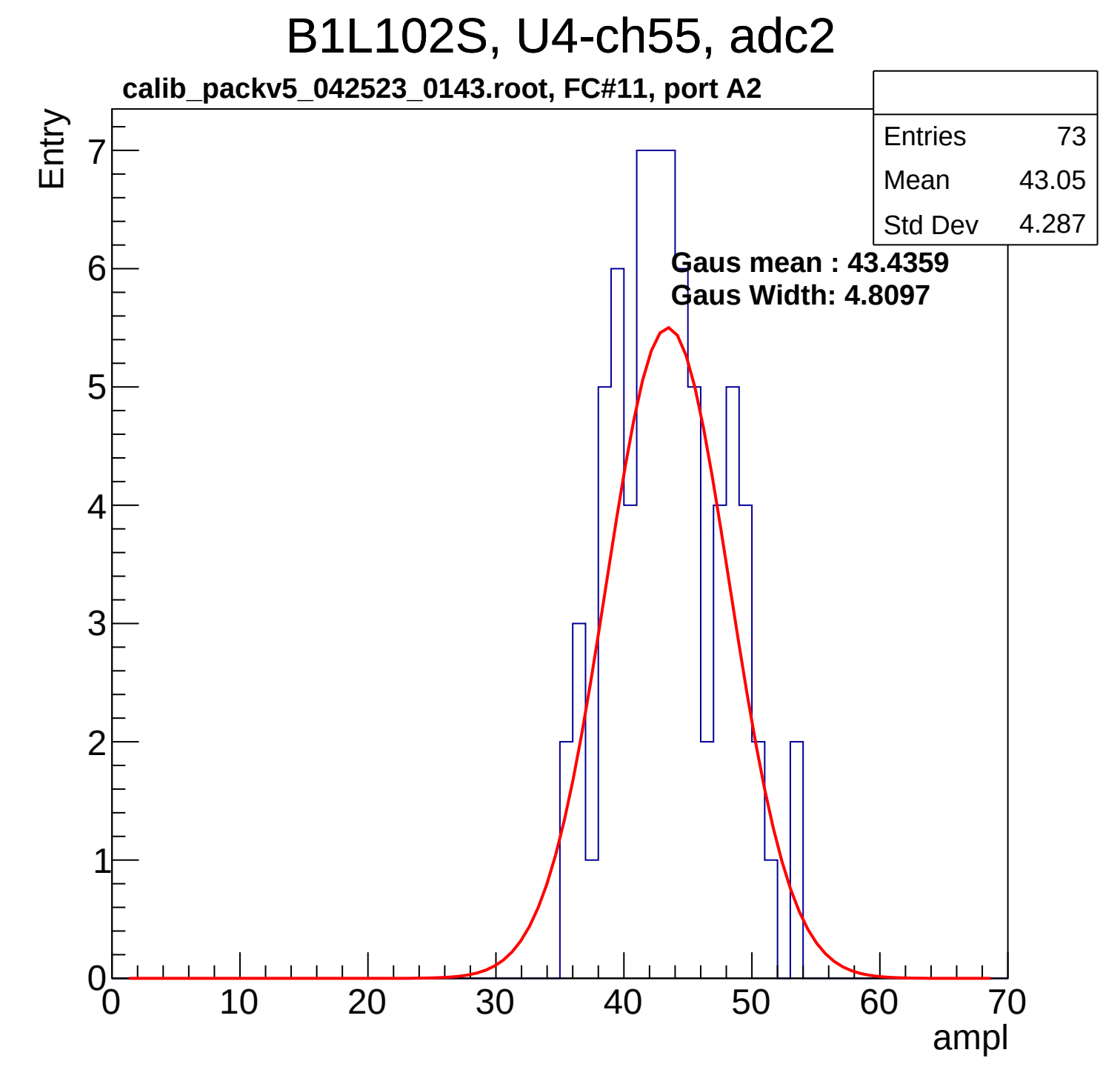
B1L102S, U4-ch55, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 43.05
Std Dev 4.287
Gaus mean : 43.4359
Gaus Width: 4.8097
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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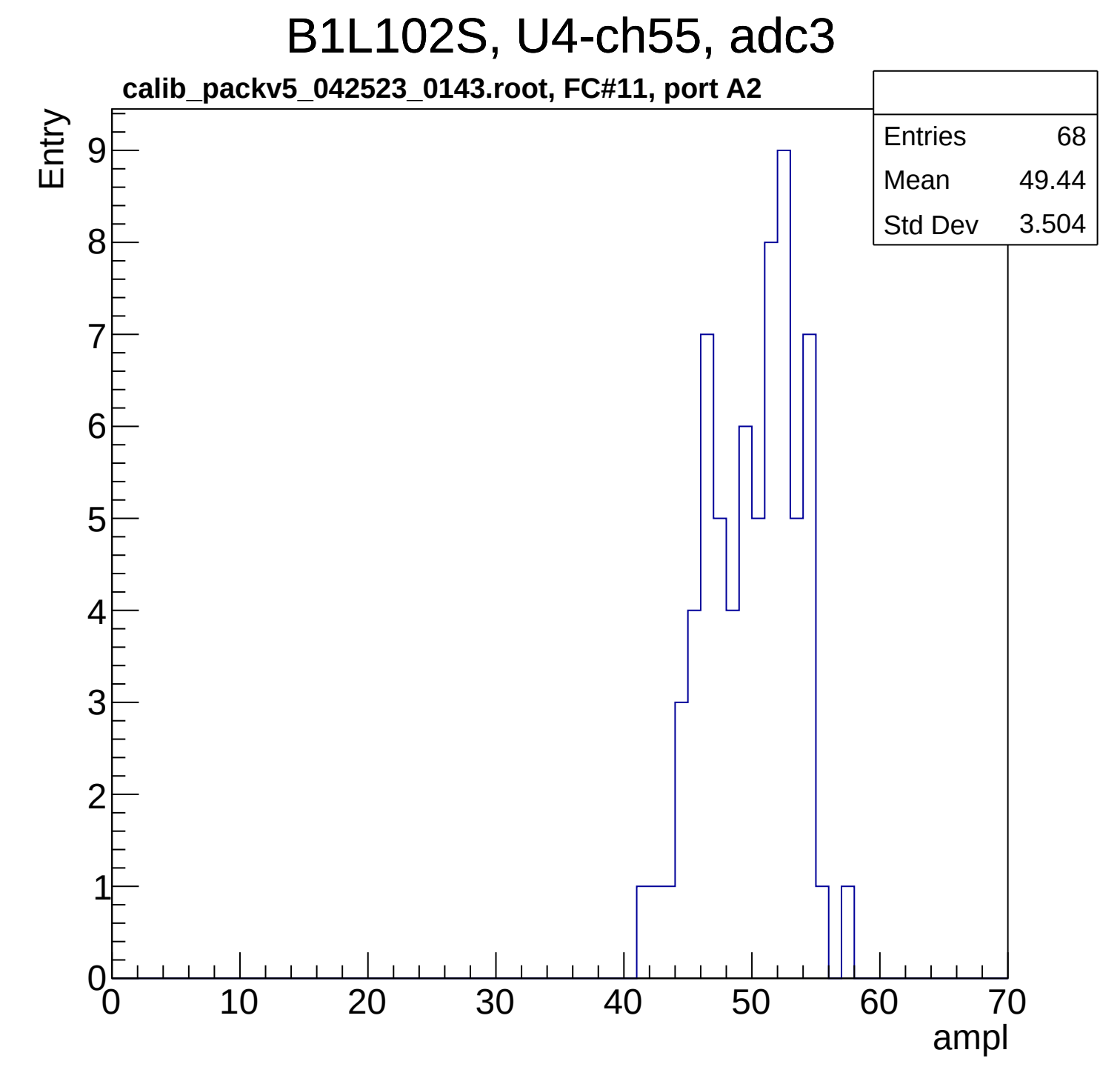
B1L102S, U4-ch55, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 49.44
Std Dev 3.504
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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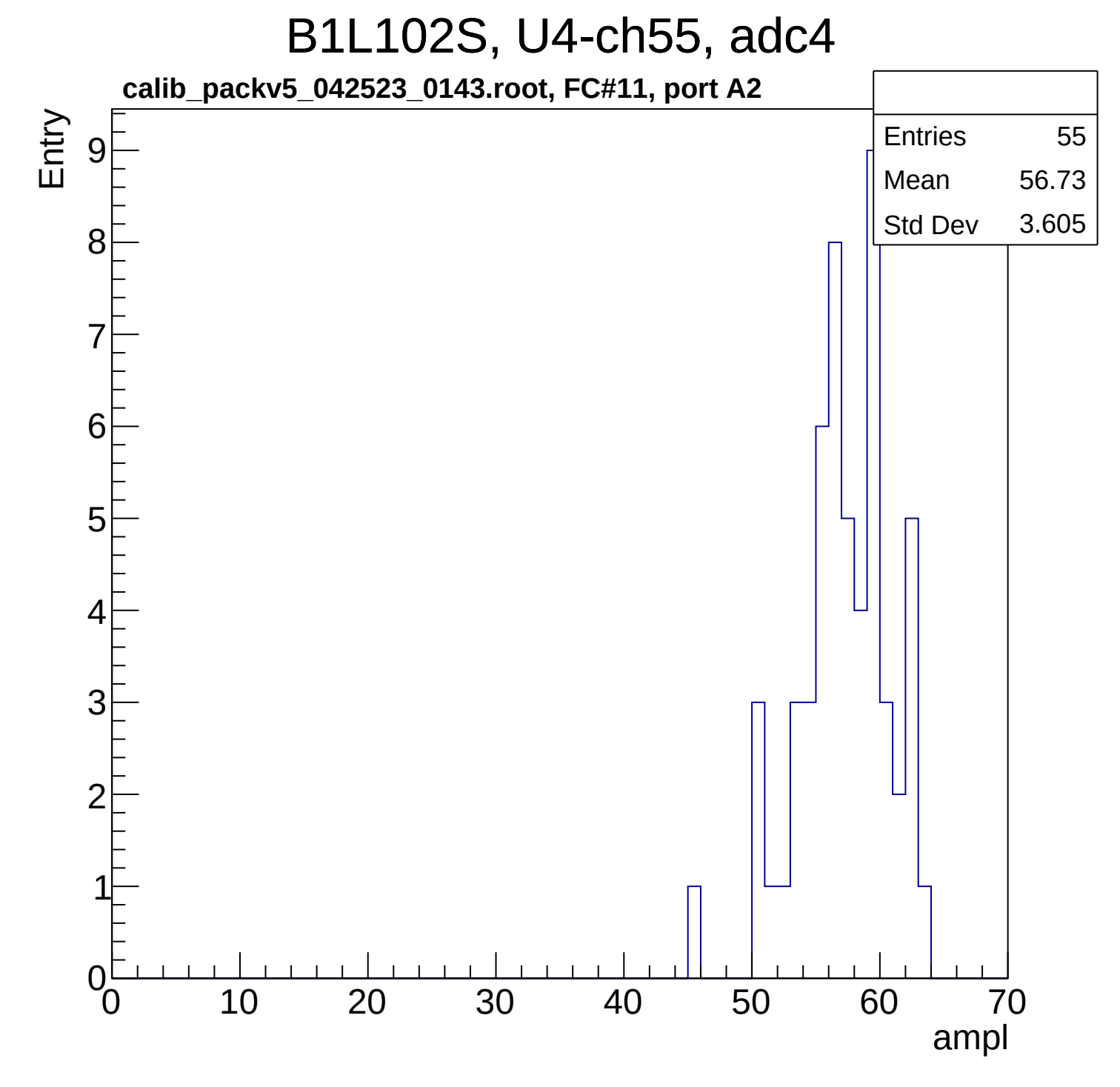
B1L102S, U4-ch55, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 56.73
Std Dev 3.605
Entry
ampl
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2
3
4
5
6
7
8
9
0
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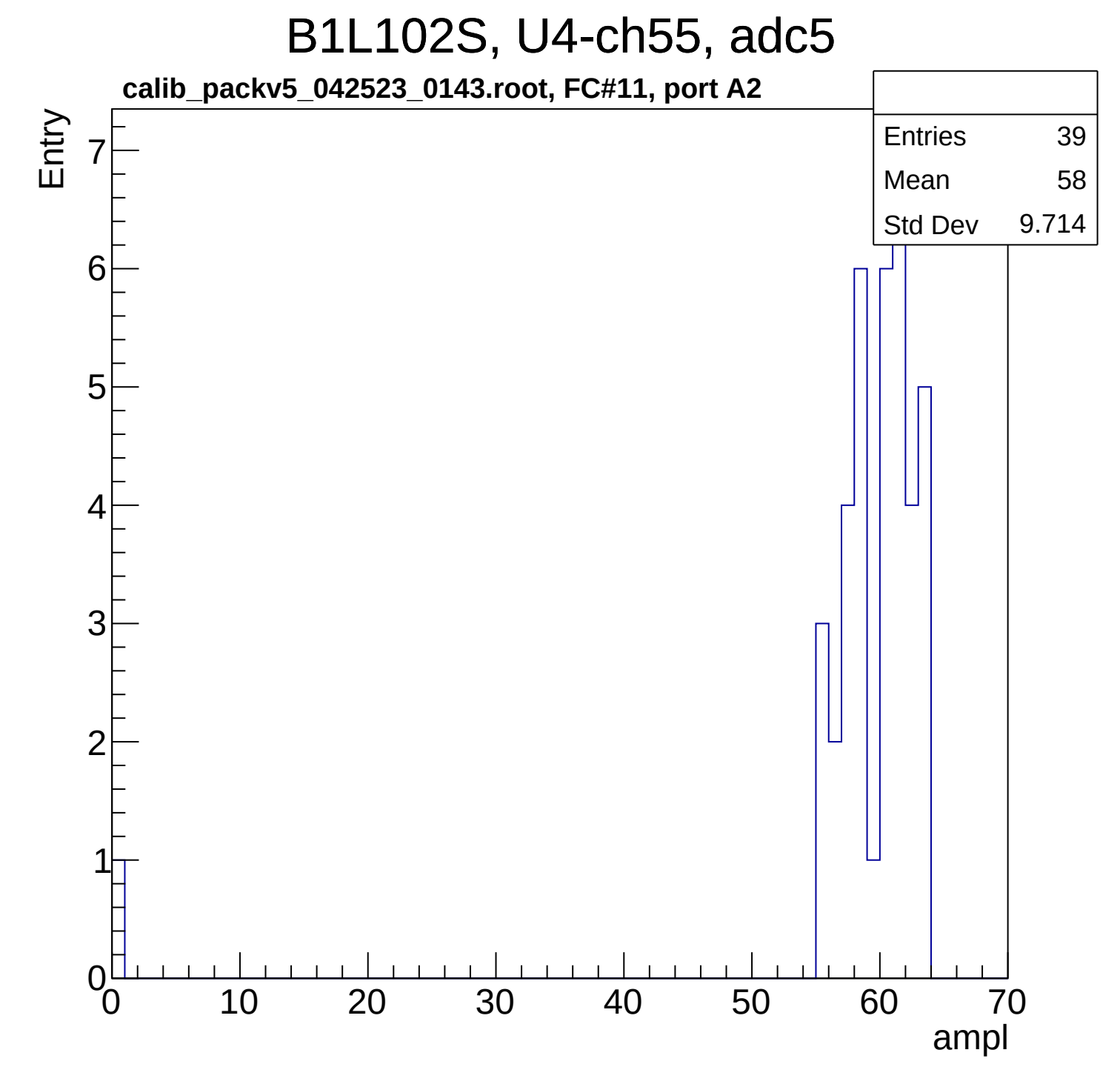
B1L102S, U4-ch55, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 39
Mean 58
Std Dev 9.714
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
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60
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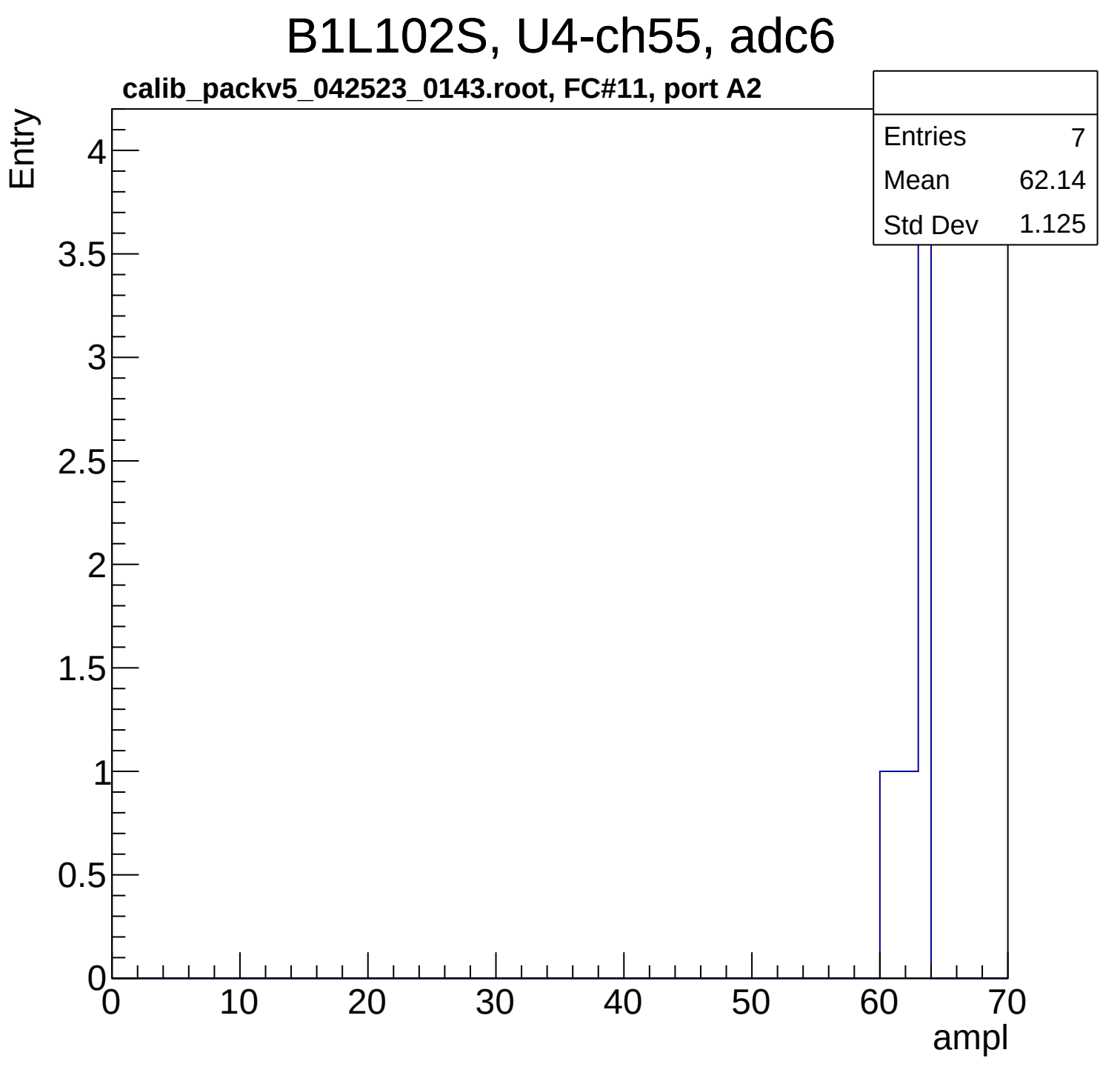
B1L102S, U4-ch55, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 7
Mean 62.14
Std Dev 1.125
Entry
ampl
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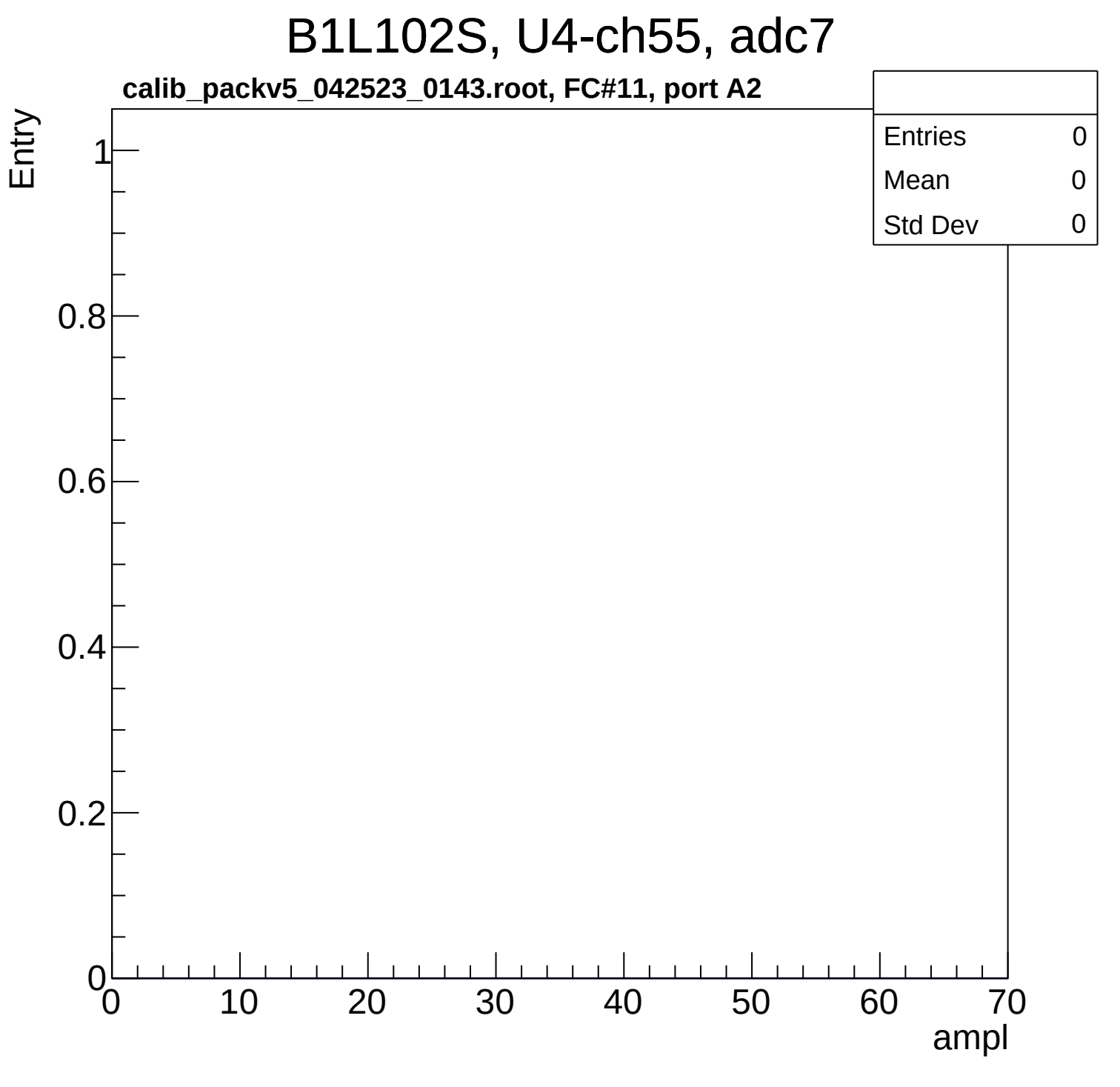
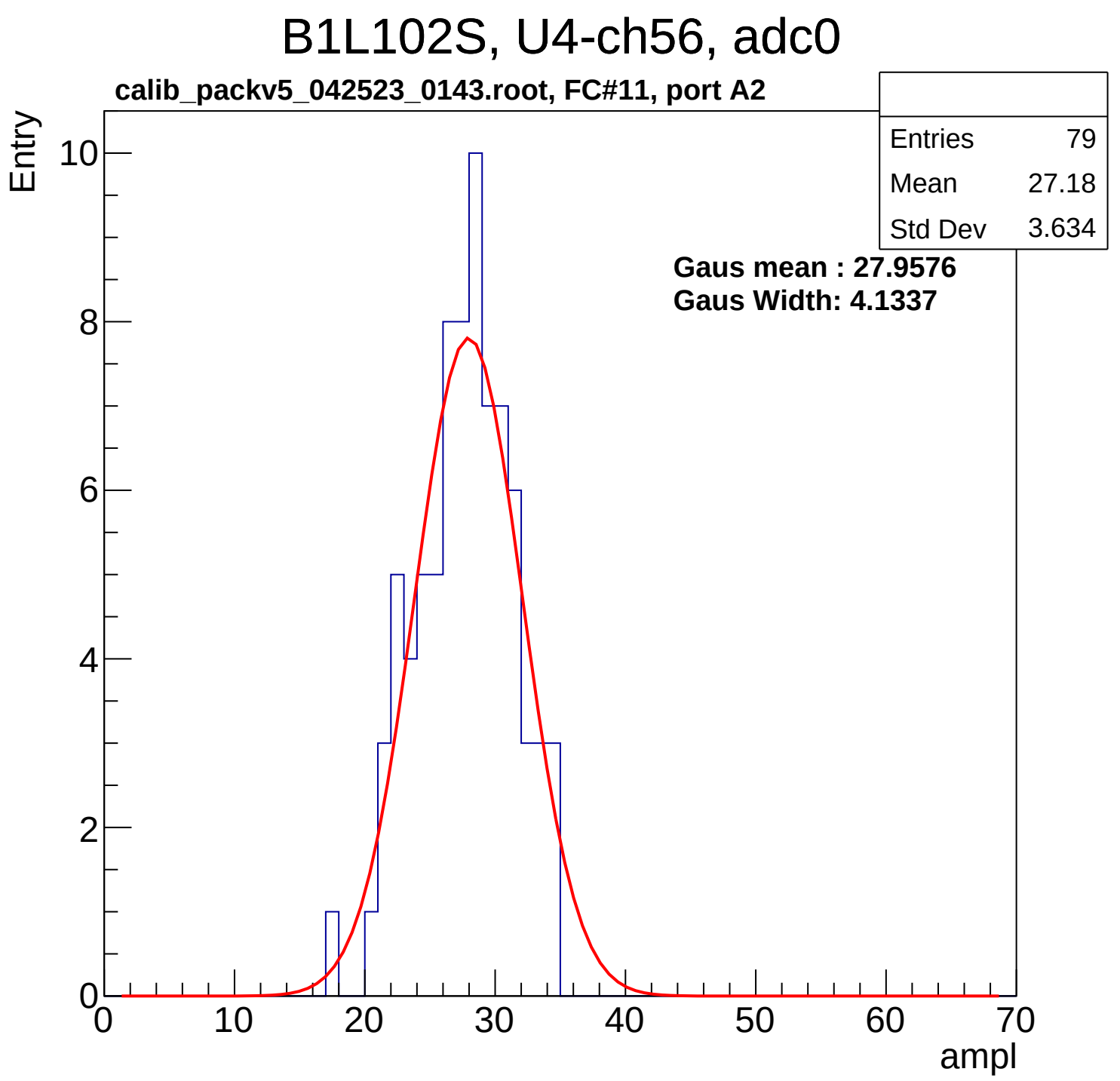
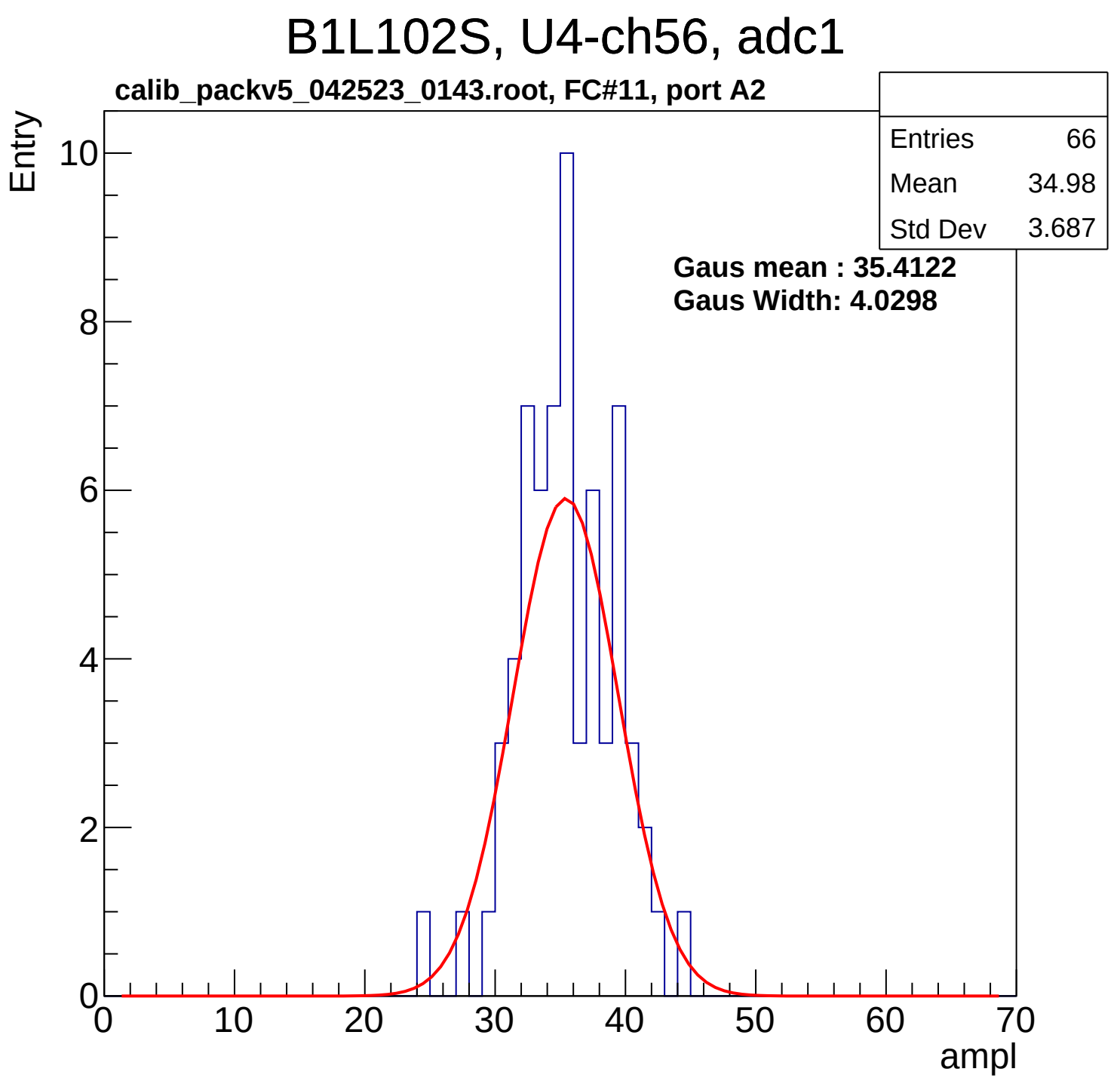
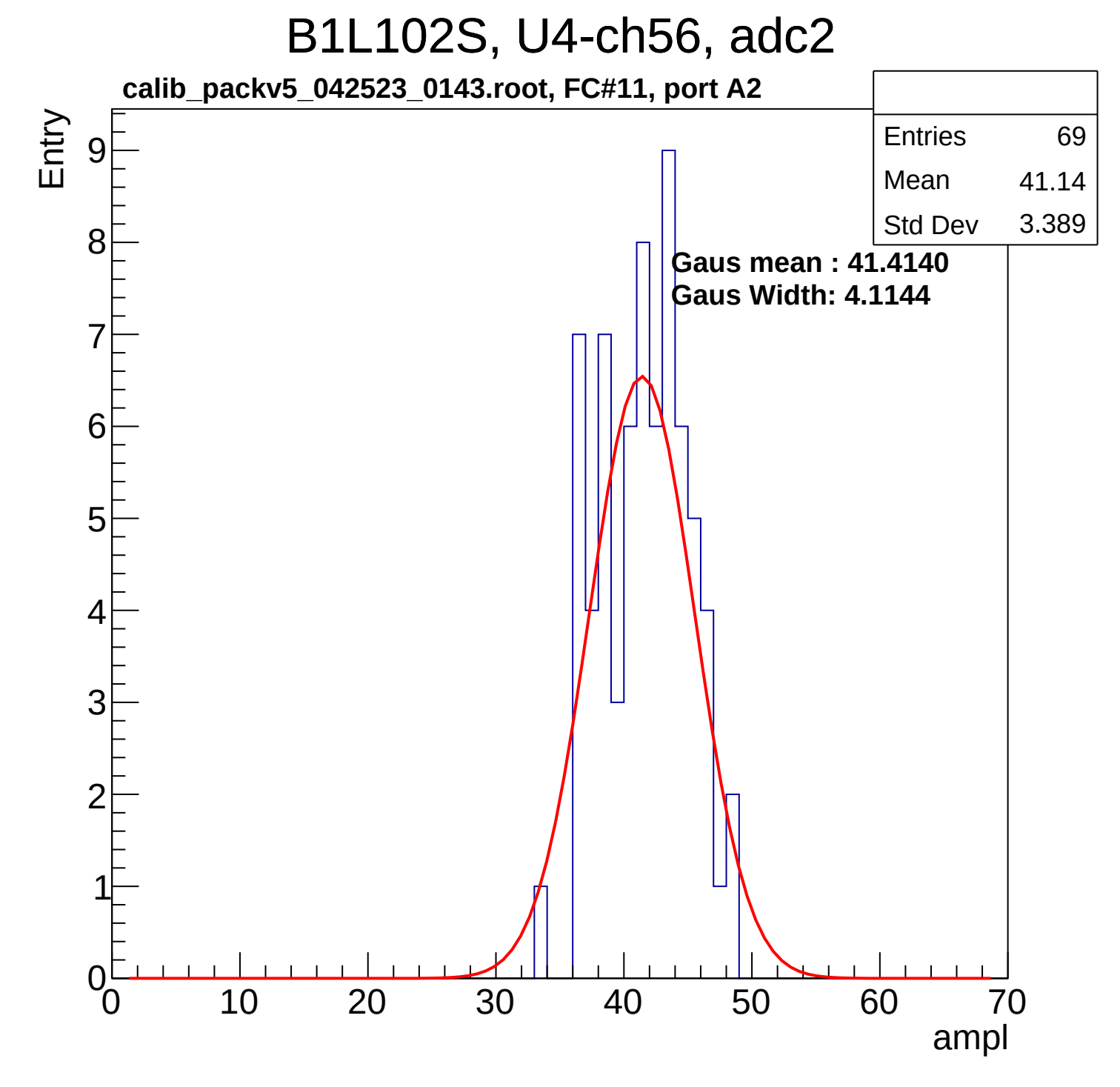
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U4-ch55, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch56, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 79
Mean 27.18
Std Dev 3.634
Gaus mean : 27.9576
Gaus Width: 4.1337
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch56, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 34.98
Std Dev 3.687
Gaus mean : 35.4122
Gaus Width: 4.0298
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch56, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 41.14
Std Dev 3.389
Gaus mean : 41.4140
Gaus Width: 4.1144
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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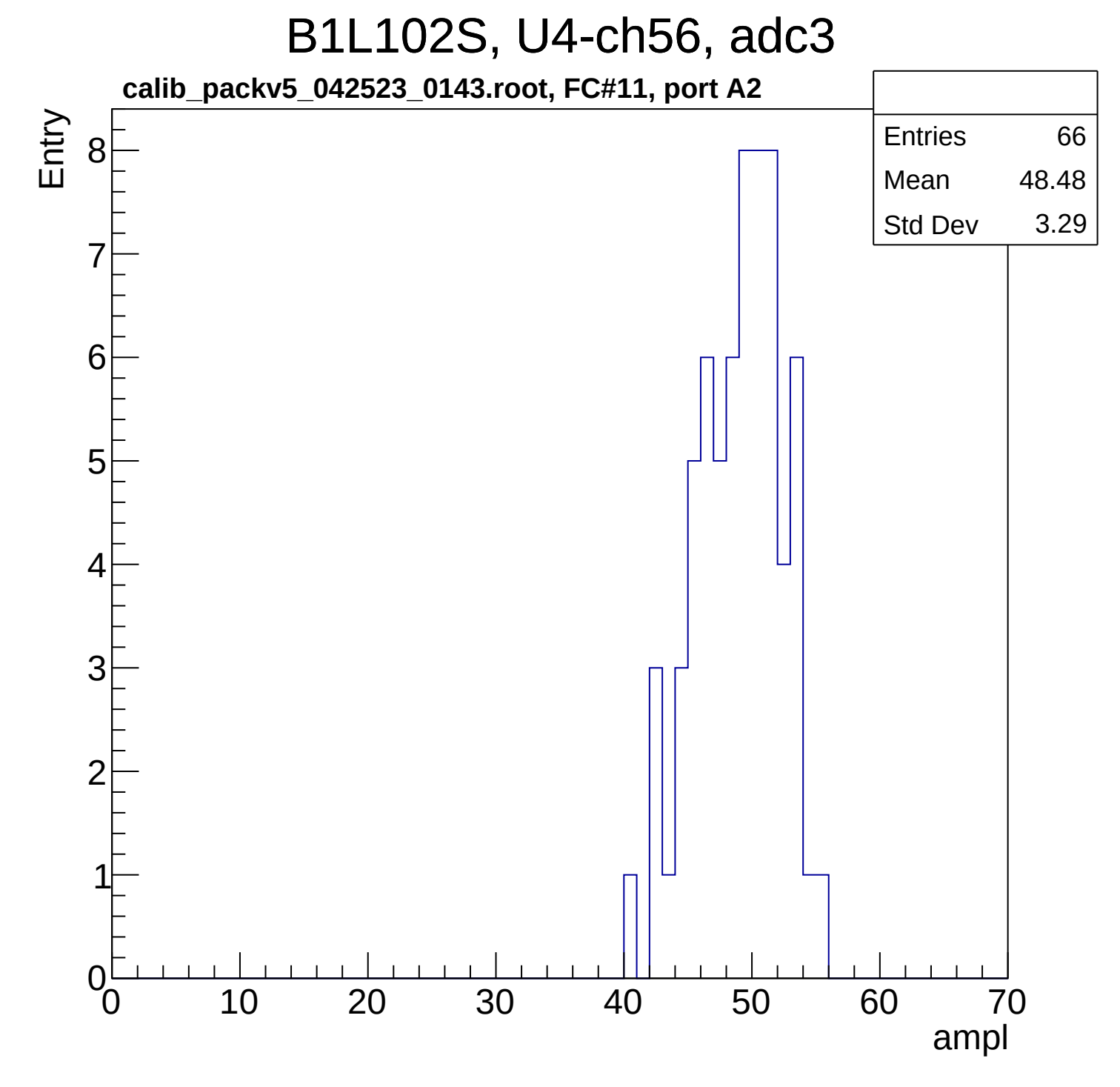
B1L102S, U4-ch56, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 48.48
Std Dev 3.29
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
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60
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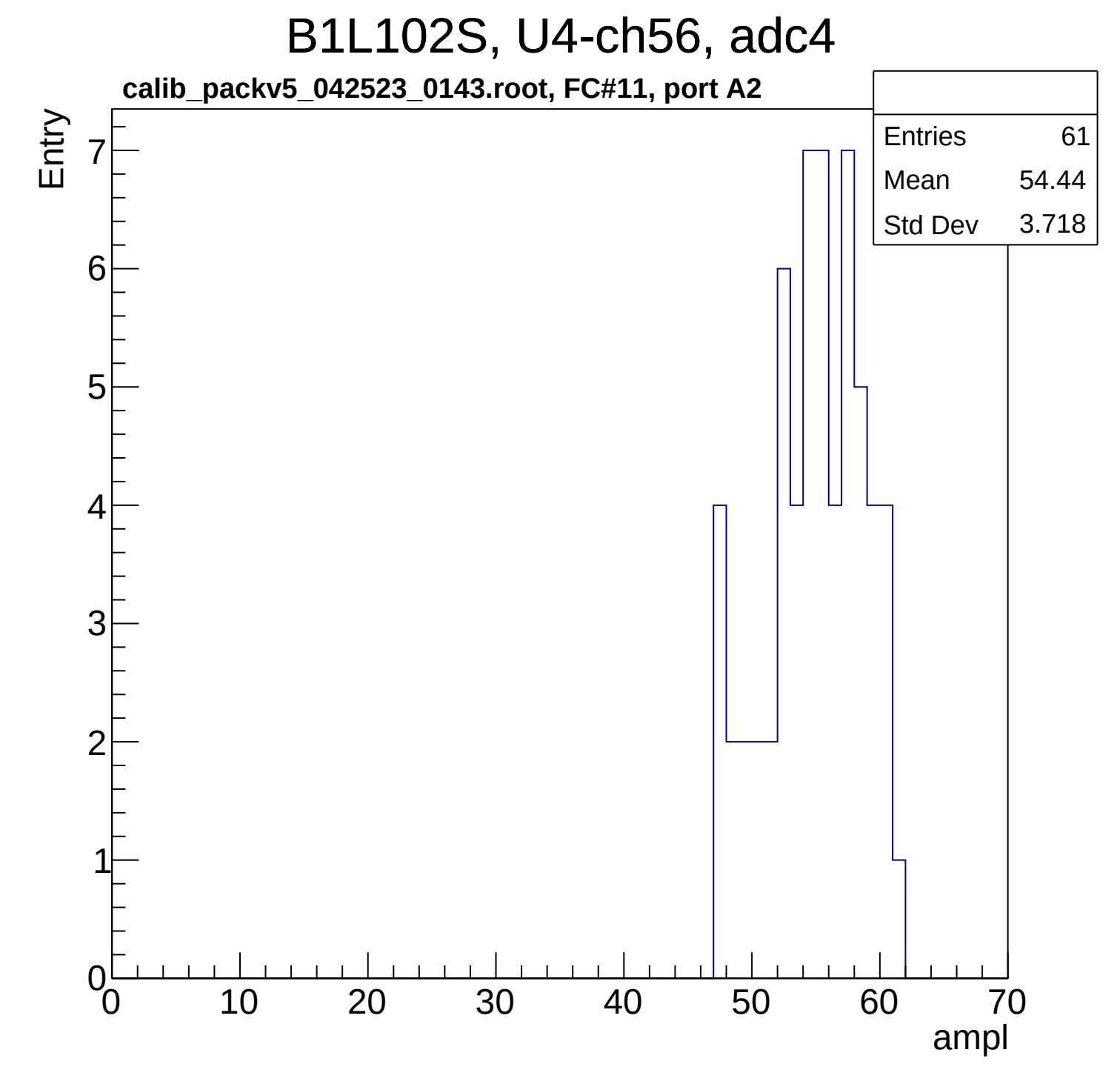
B1L102S, U4-ch56, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 54.44
Std Dev 3.718
Entry
ampl
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1
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4
5
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7
0
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60
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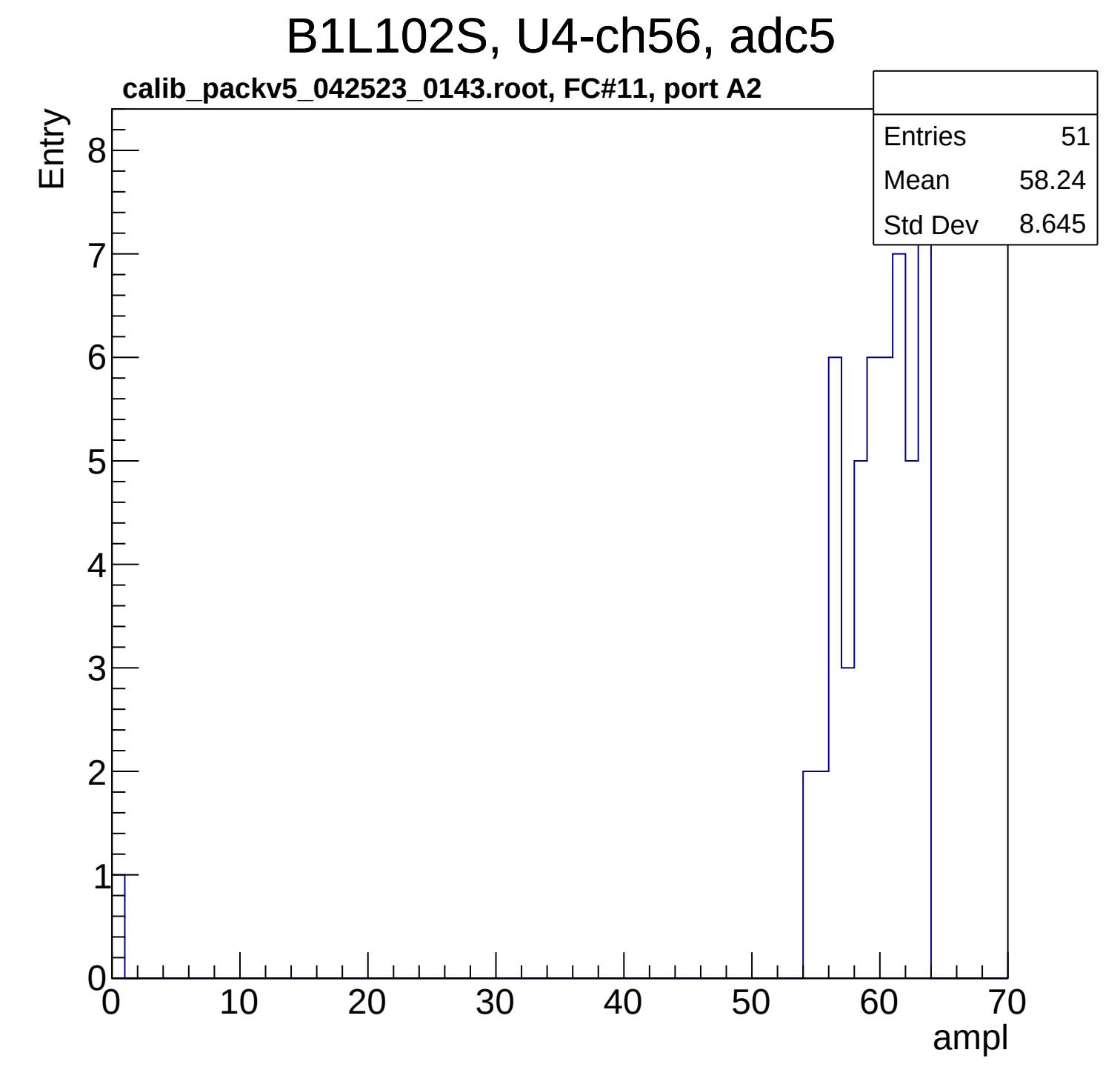
B1L102S, U4-ch56, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 58.24
Std Dev 8.645
Entry
ampl
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4
5
6
7
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0
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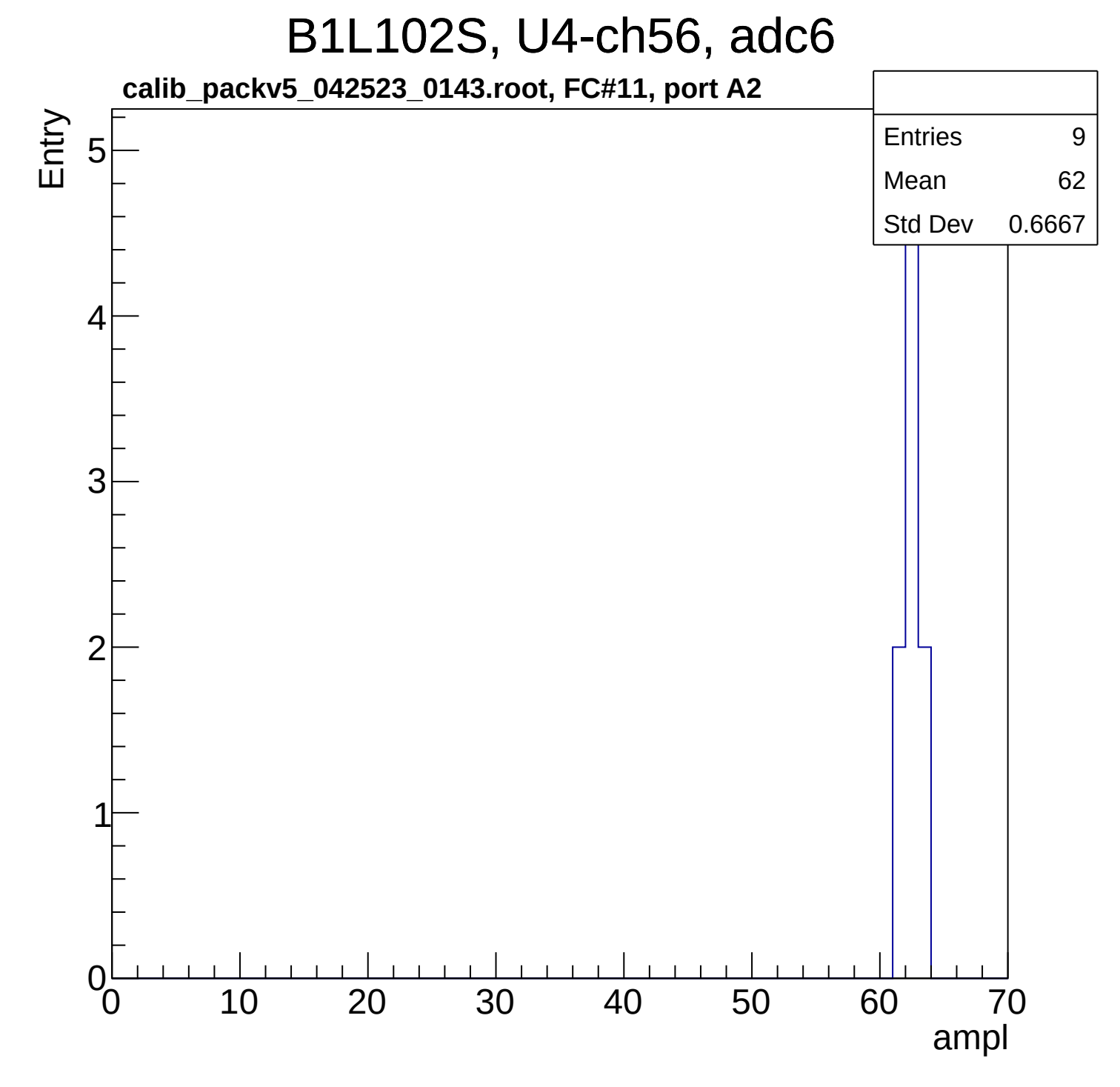
B1L102S, U4-ch56, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 9
Mean 62
Std Dev 0.6667
Entry
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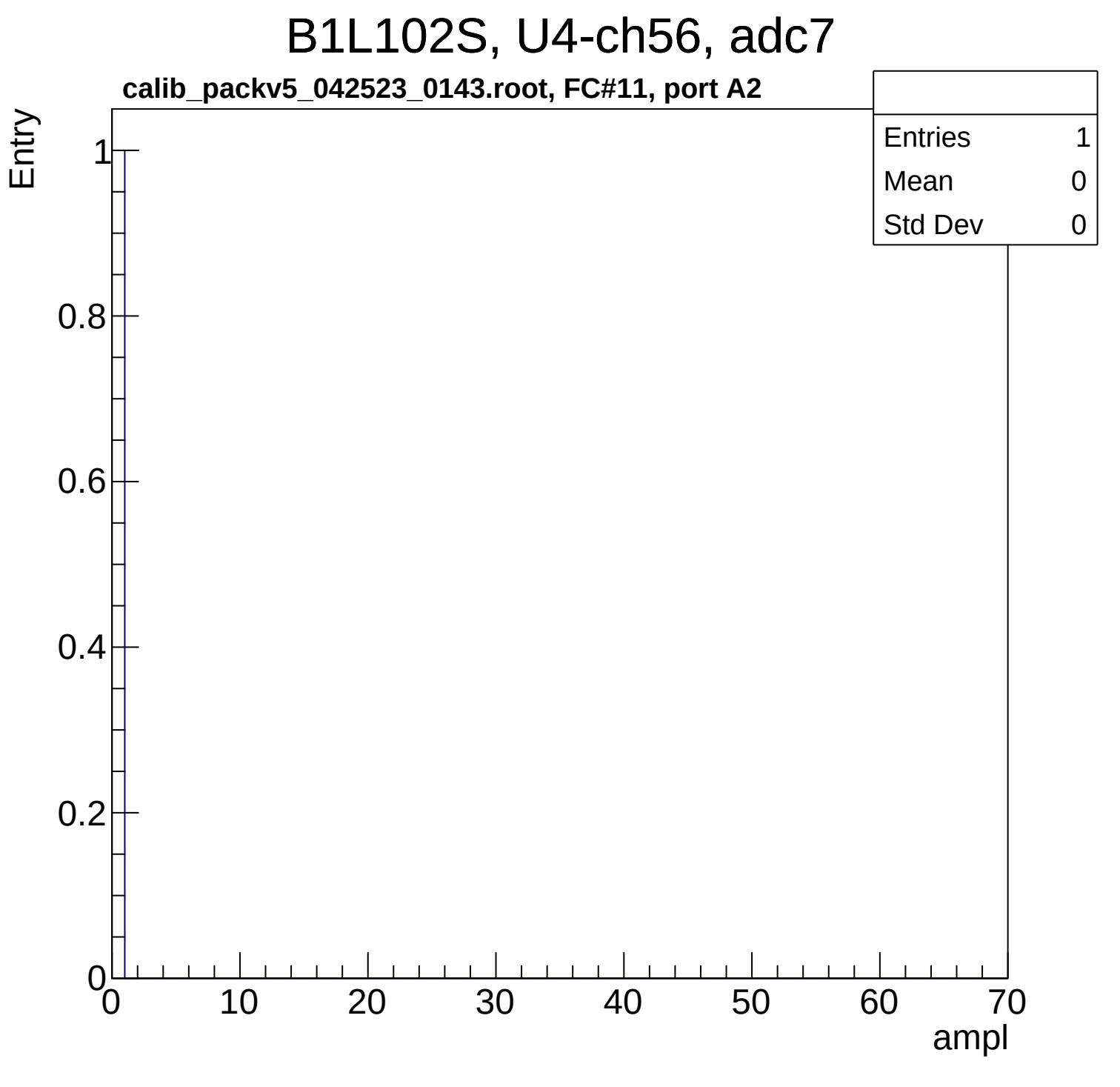
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch56, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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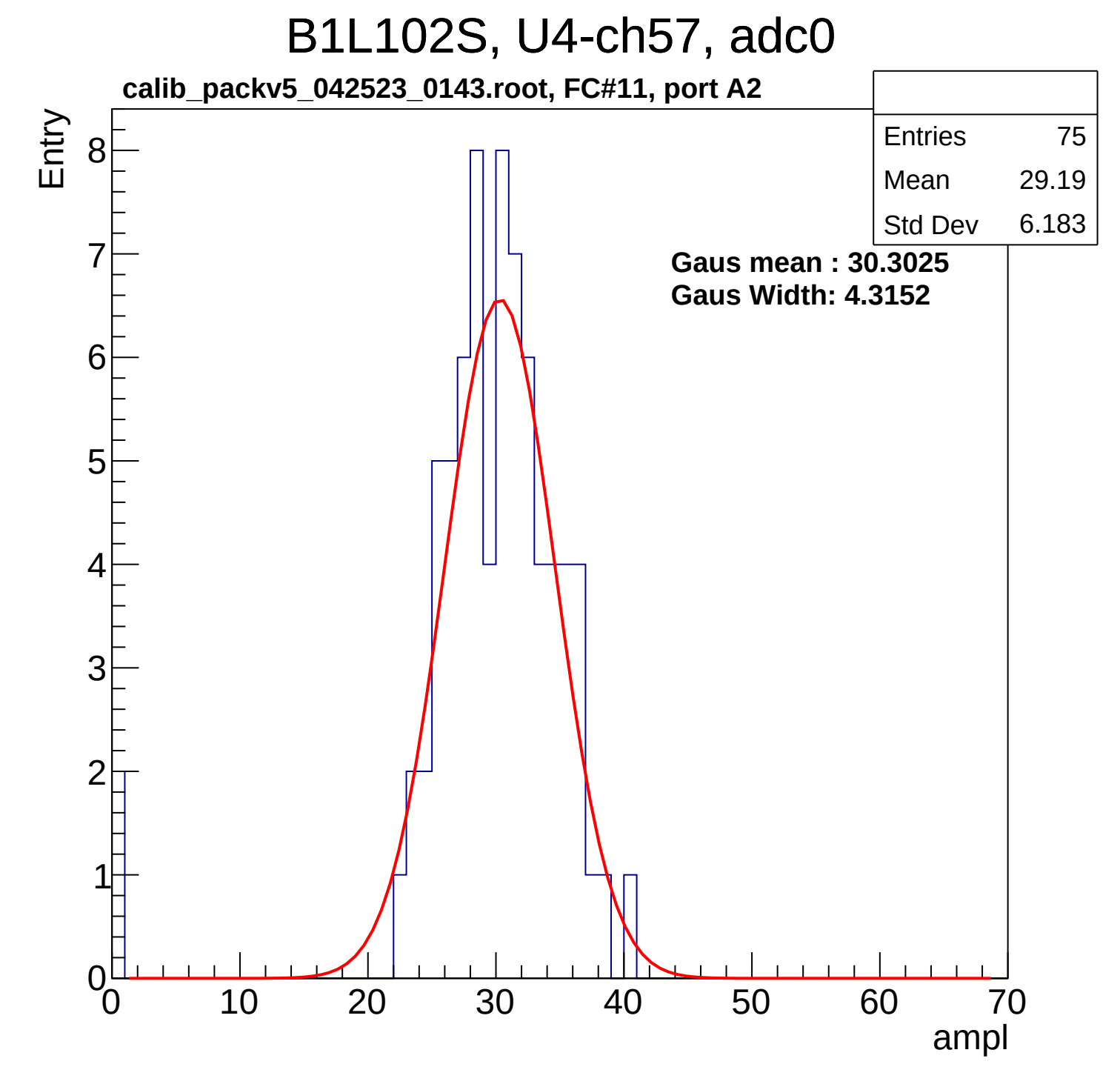
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch57, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 29.19
Std Dev 6.183
Gaus mean : 30.3025
Gaus Width: 4.3152
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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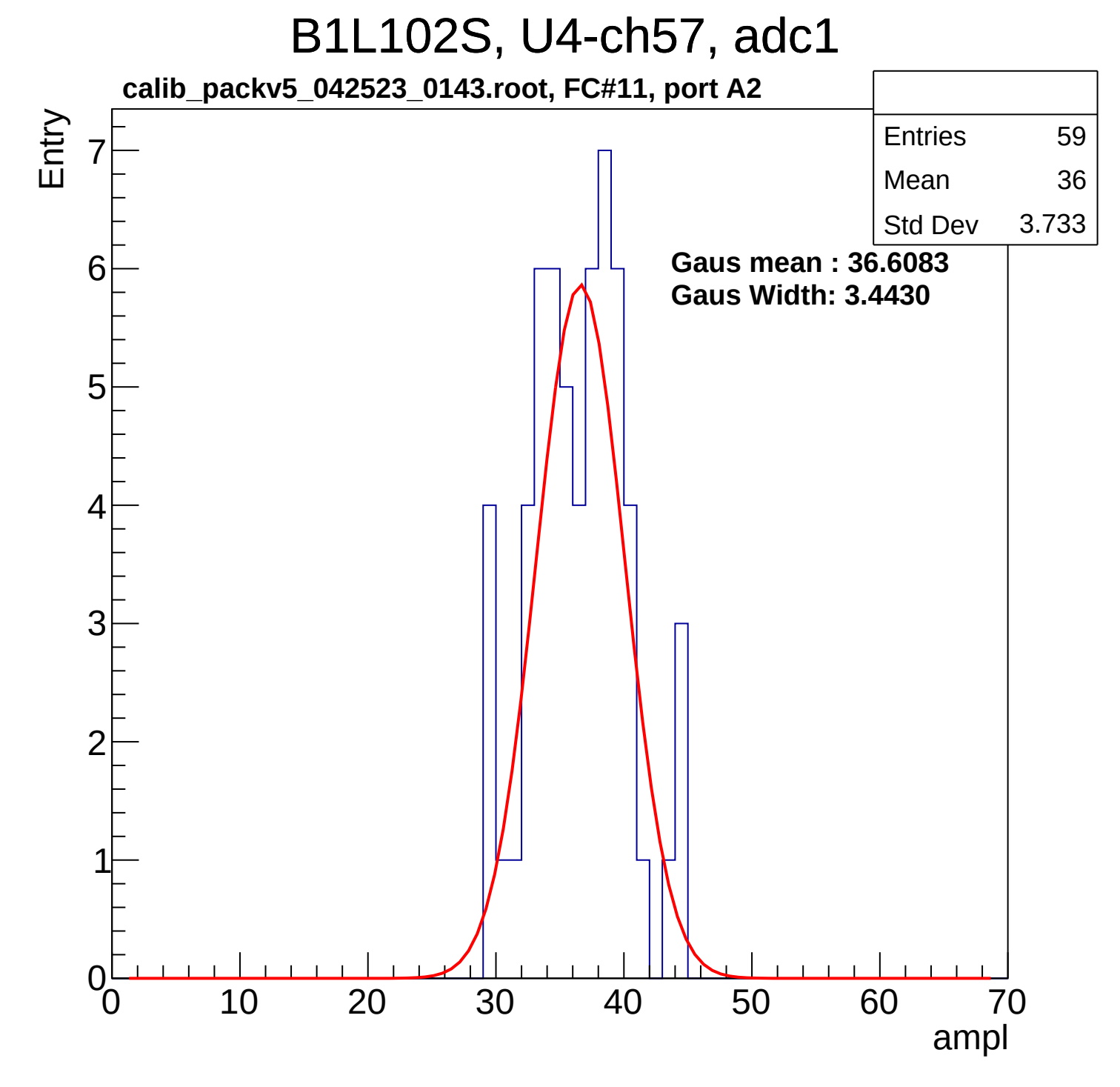
B1L102S, U4-ch57, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 36
Std Dev 3.733
Gaus mean : 36.6083
Gaus Width: 3.4430
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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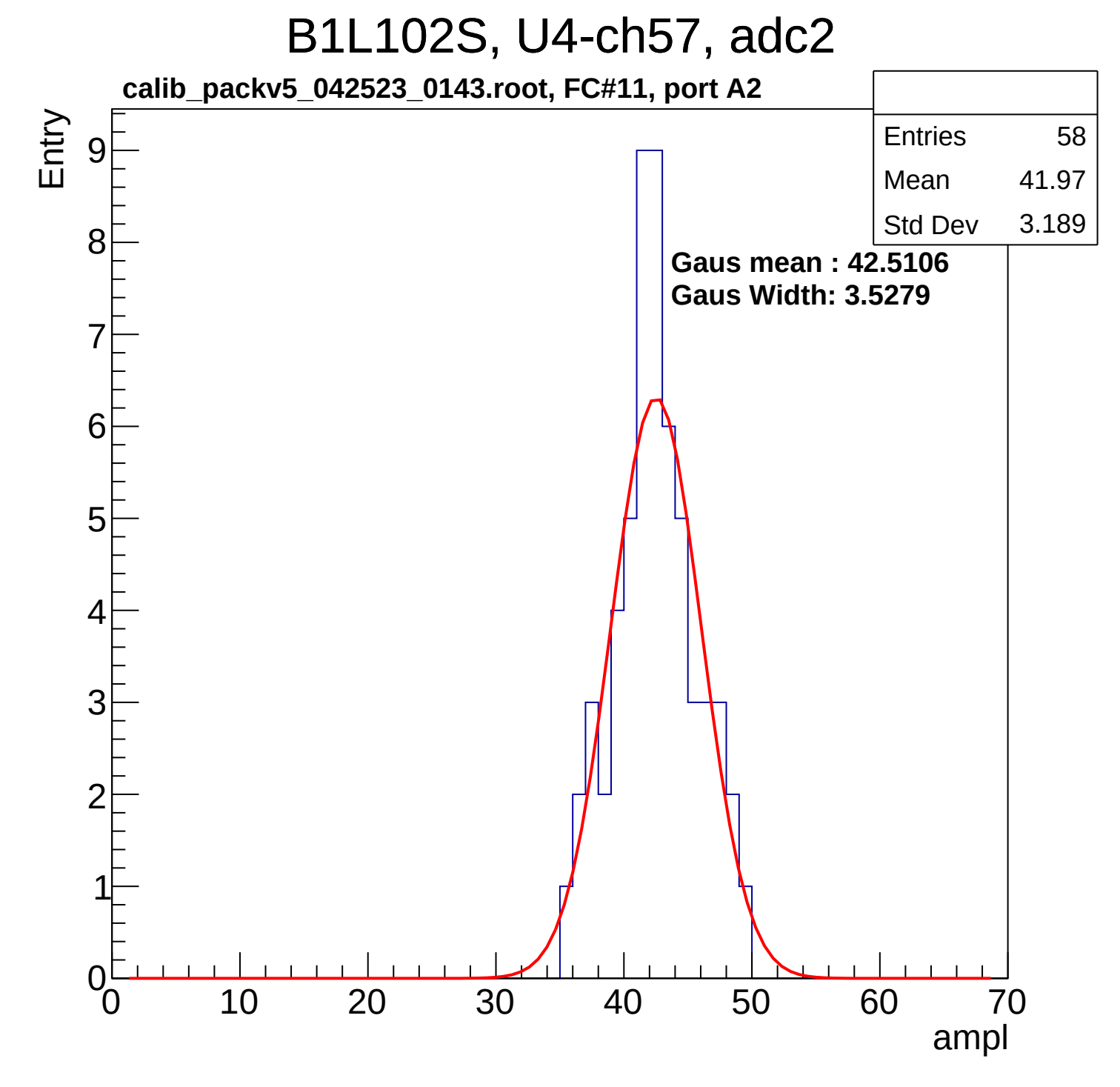
B1L102S, U4-ch57, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 41.97
Std Dev 3.189
Gaus mean : 42.5106
Gaus Width: 3.5279
Entry
ampl
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3
4
5
6
7
8
9
0
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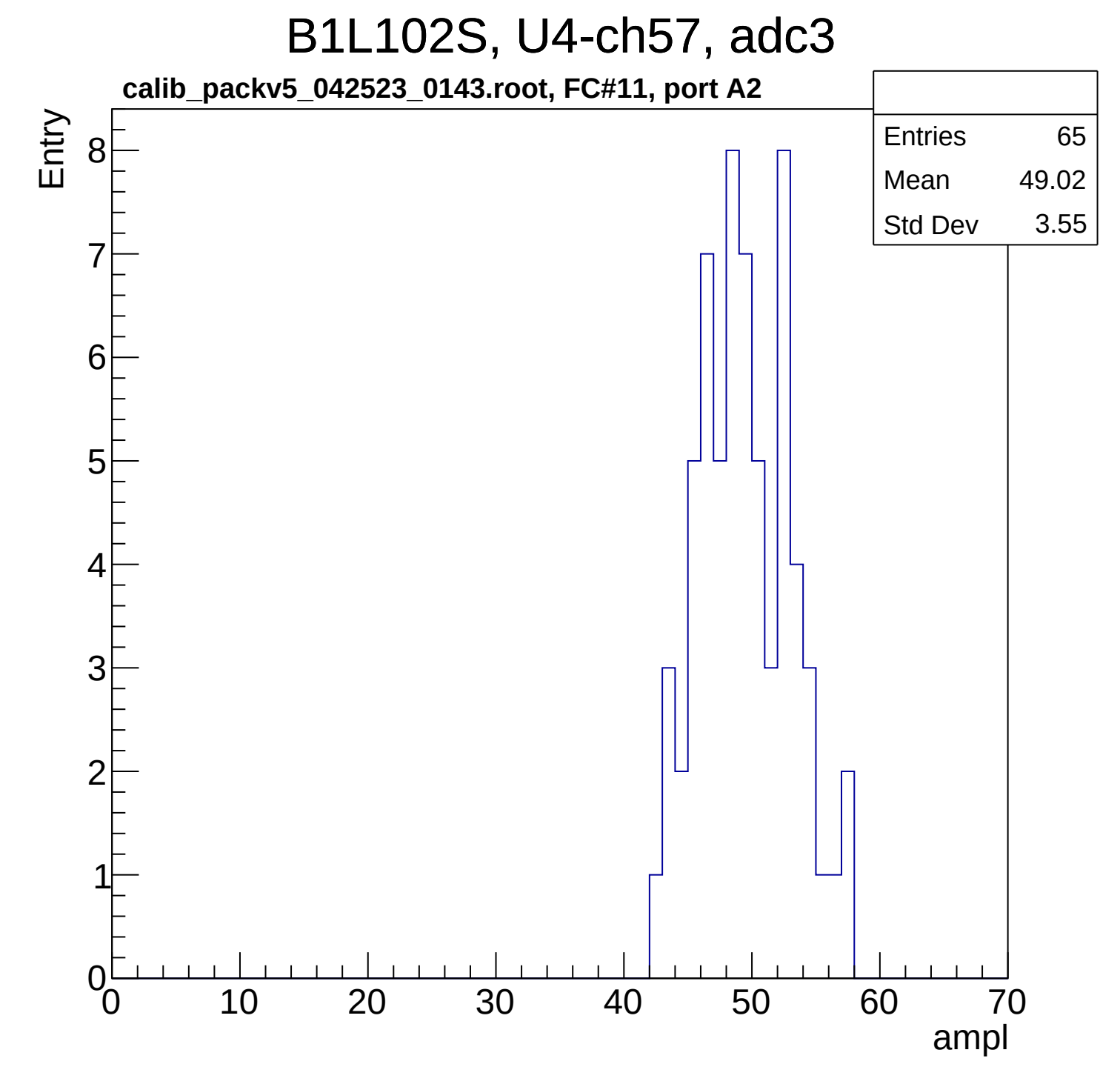
B1L102S, U4-ch57, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 49.02
Std Dev 3.55
Entry
ampl
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3
4
5
6
7
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10
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60
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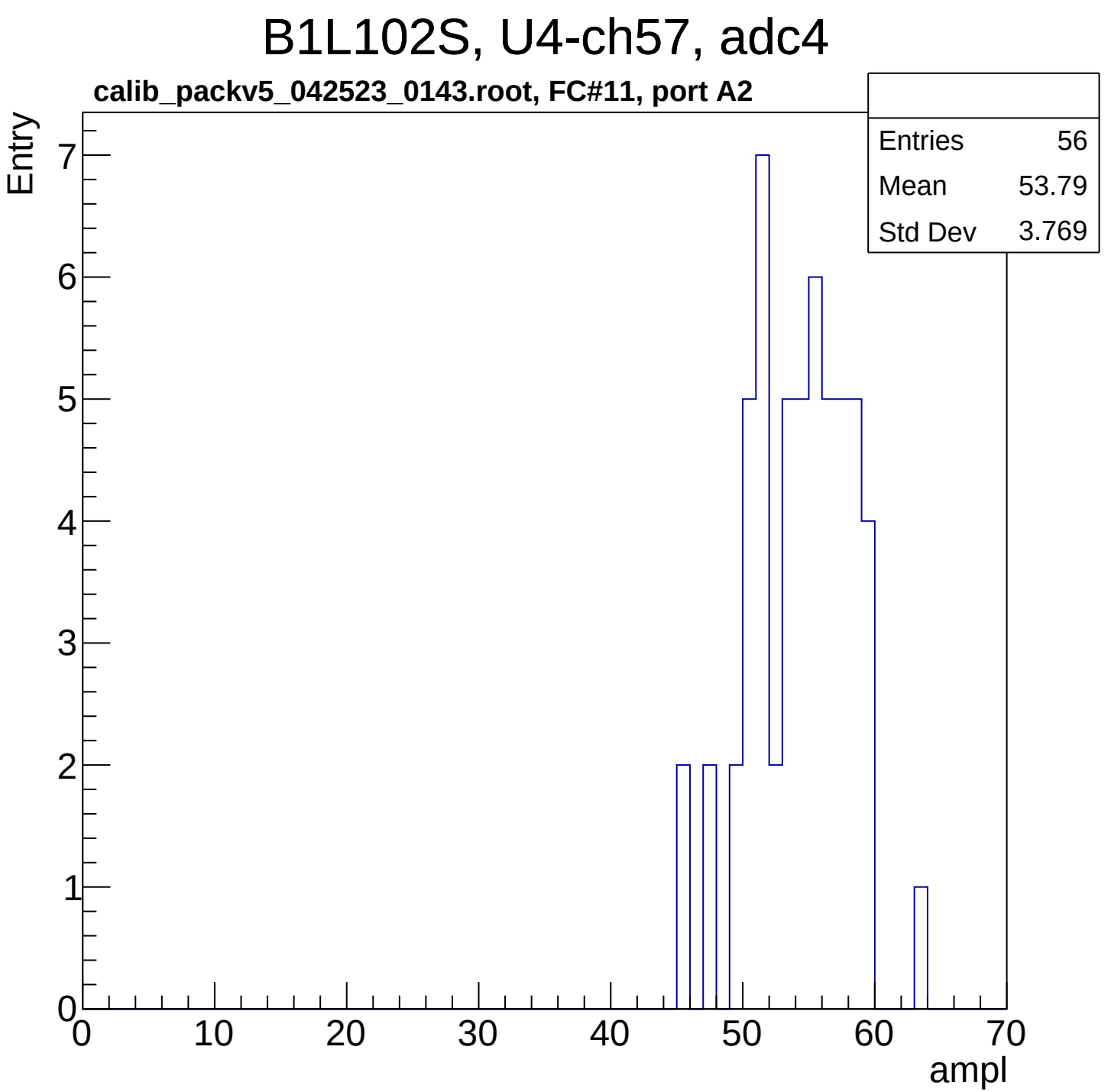
B1L102S, U4-ch57, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 53.79
Std Dev 3.769
Entry
ampl
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3
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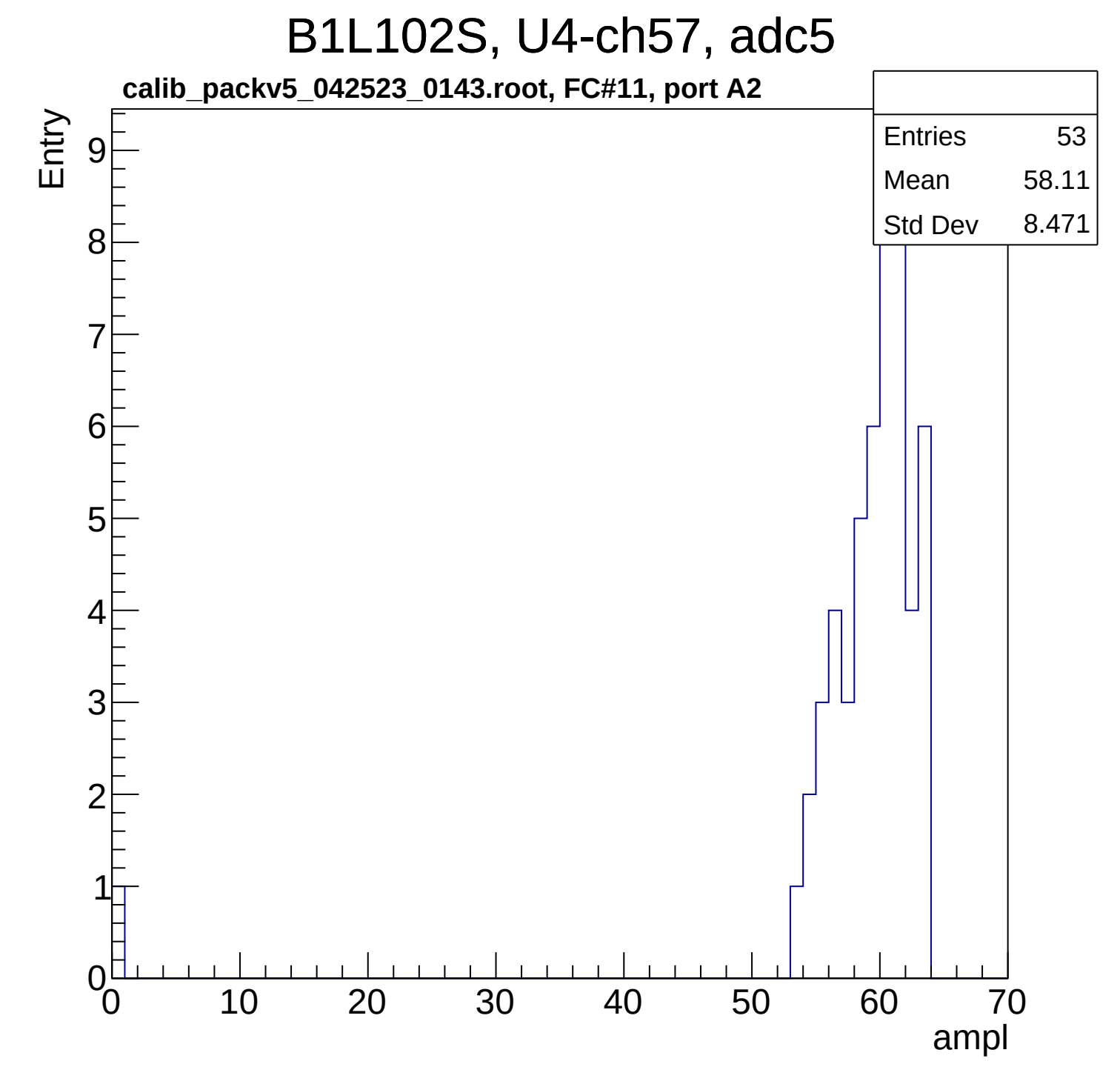
B1L102S, U4-ch57, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 58.11
Std Dev 8.471
Entry
ampl
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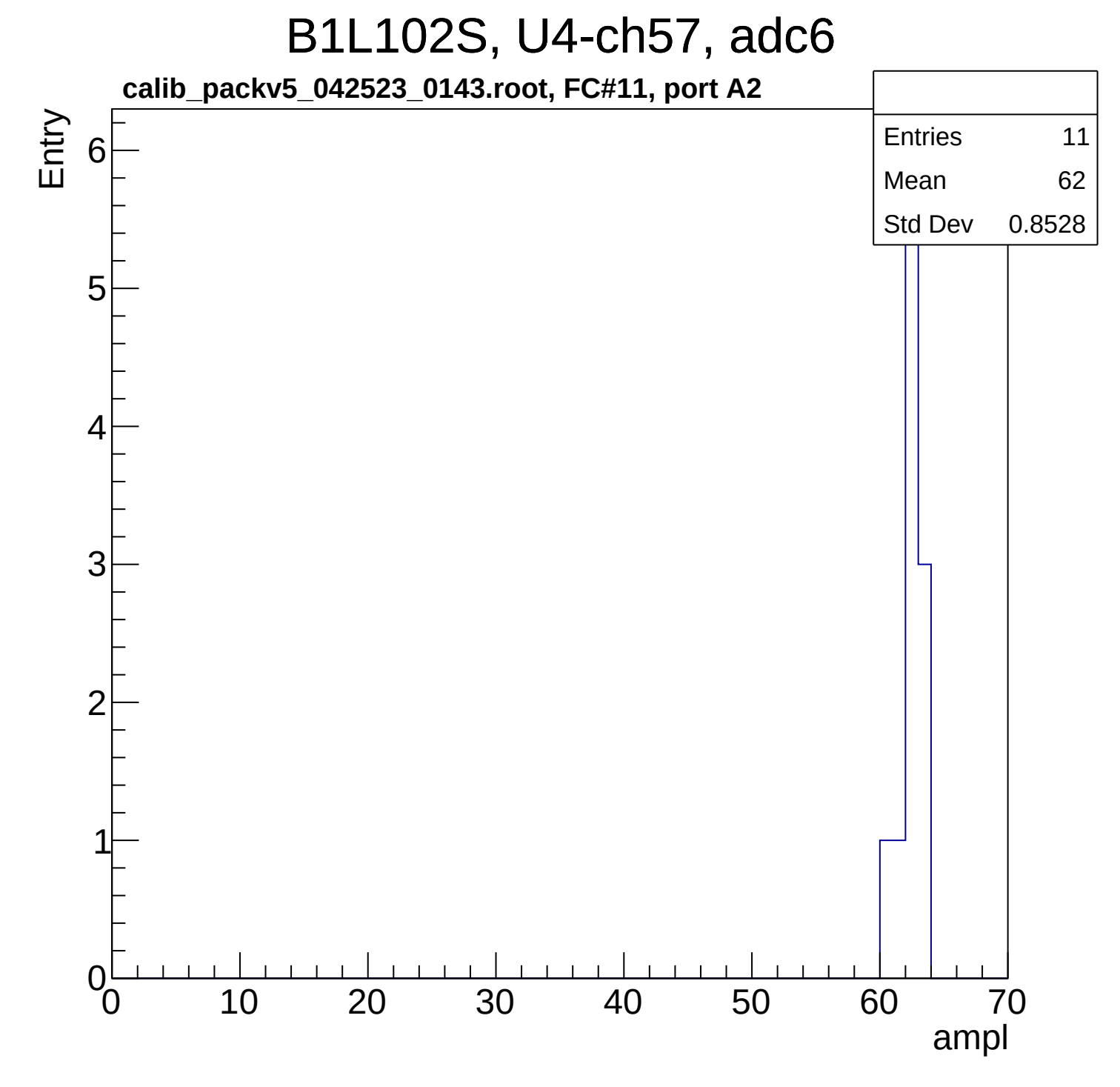
B1L102S, U4-ch57, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 11
Mean 62
Std Dev 0.8528
Entry
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3
4
5
6
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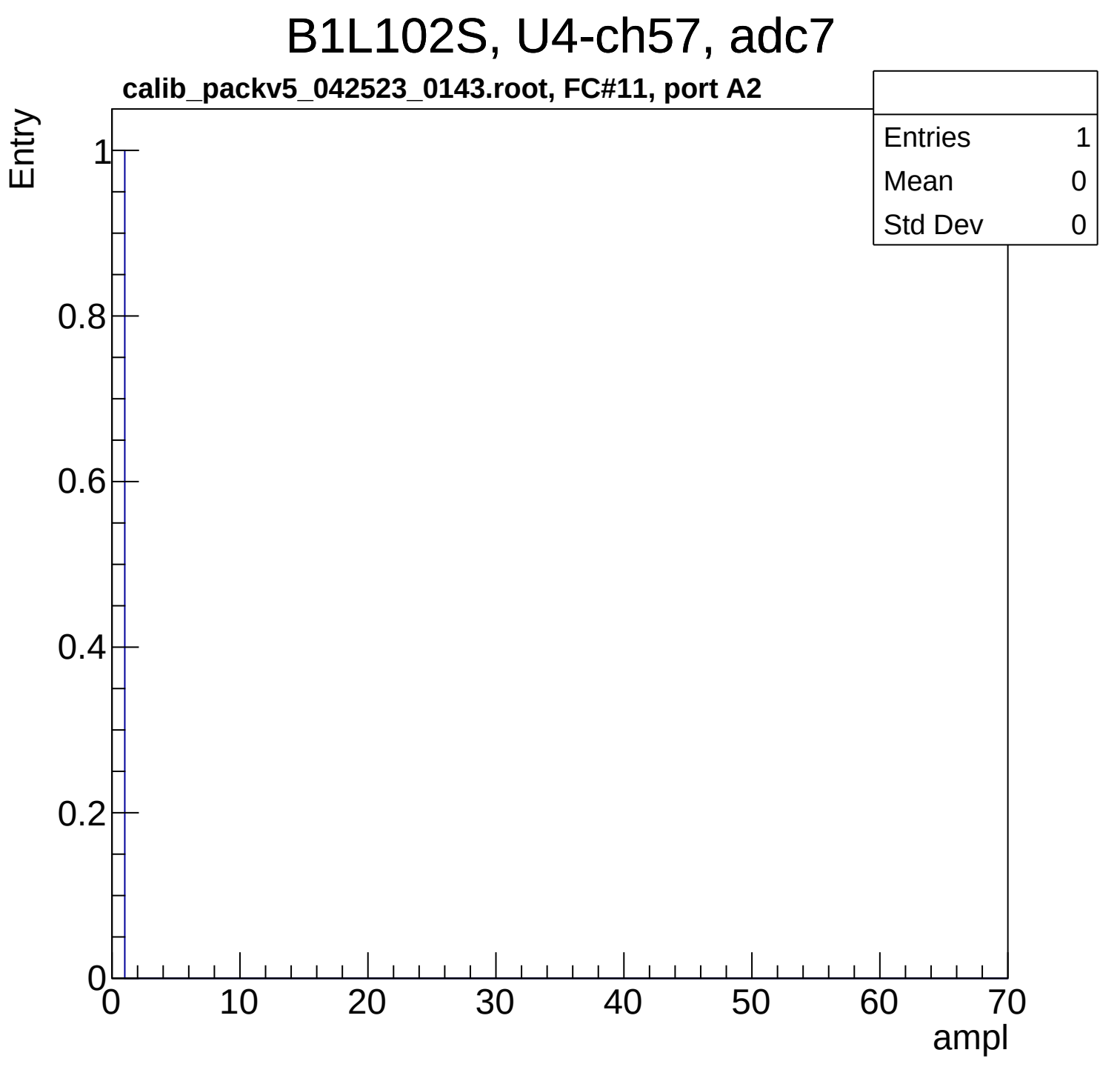
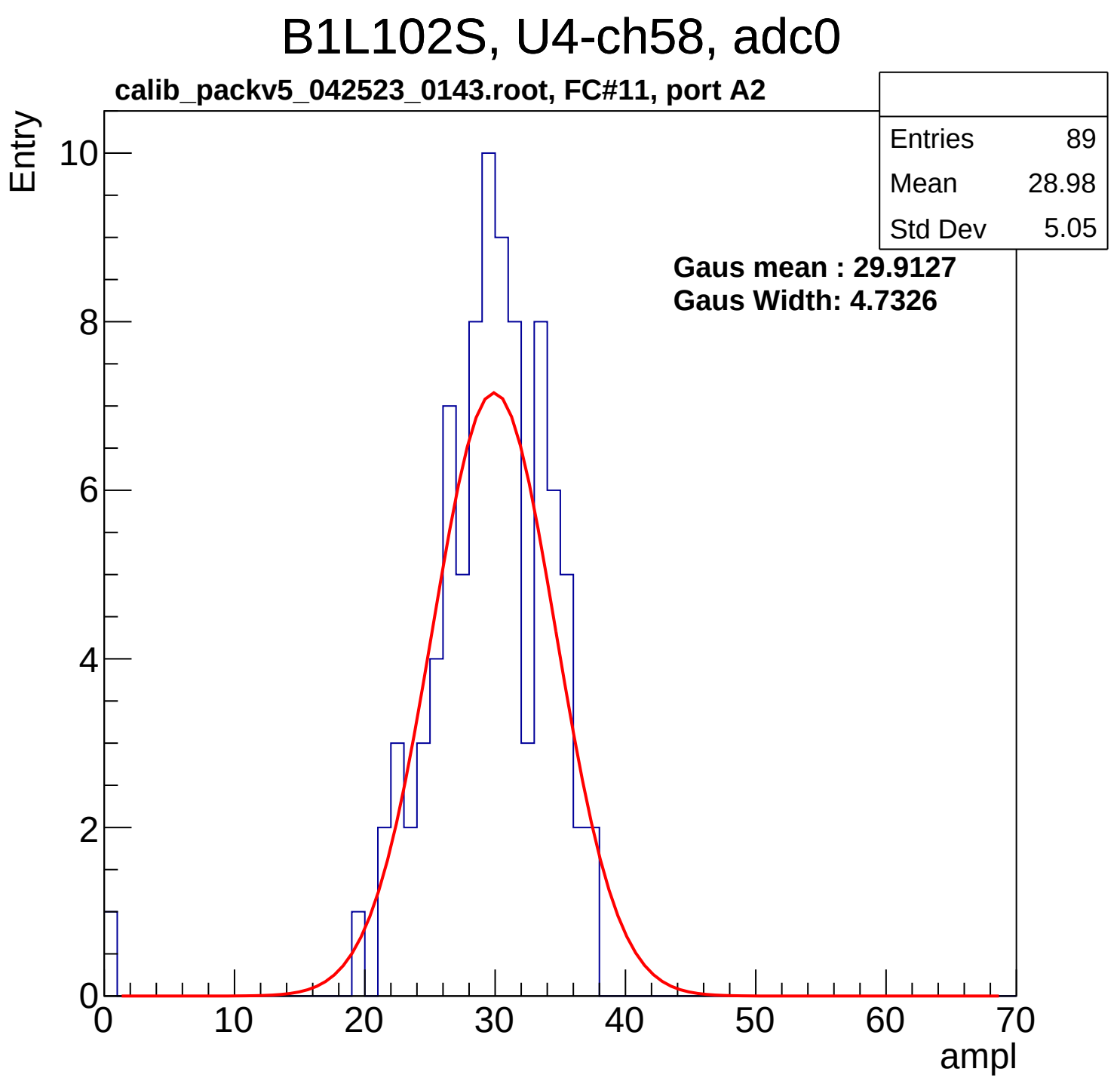
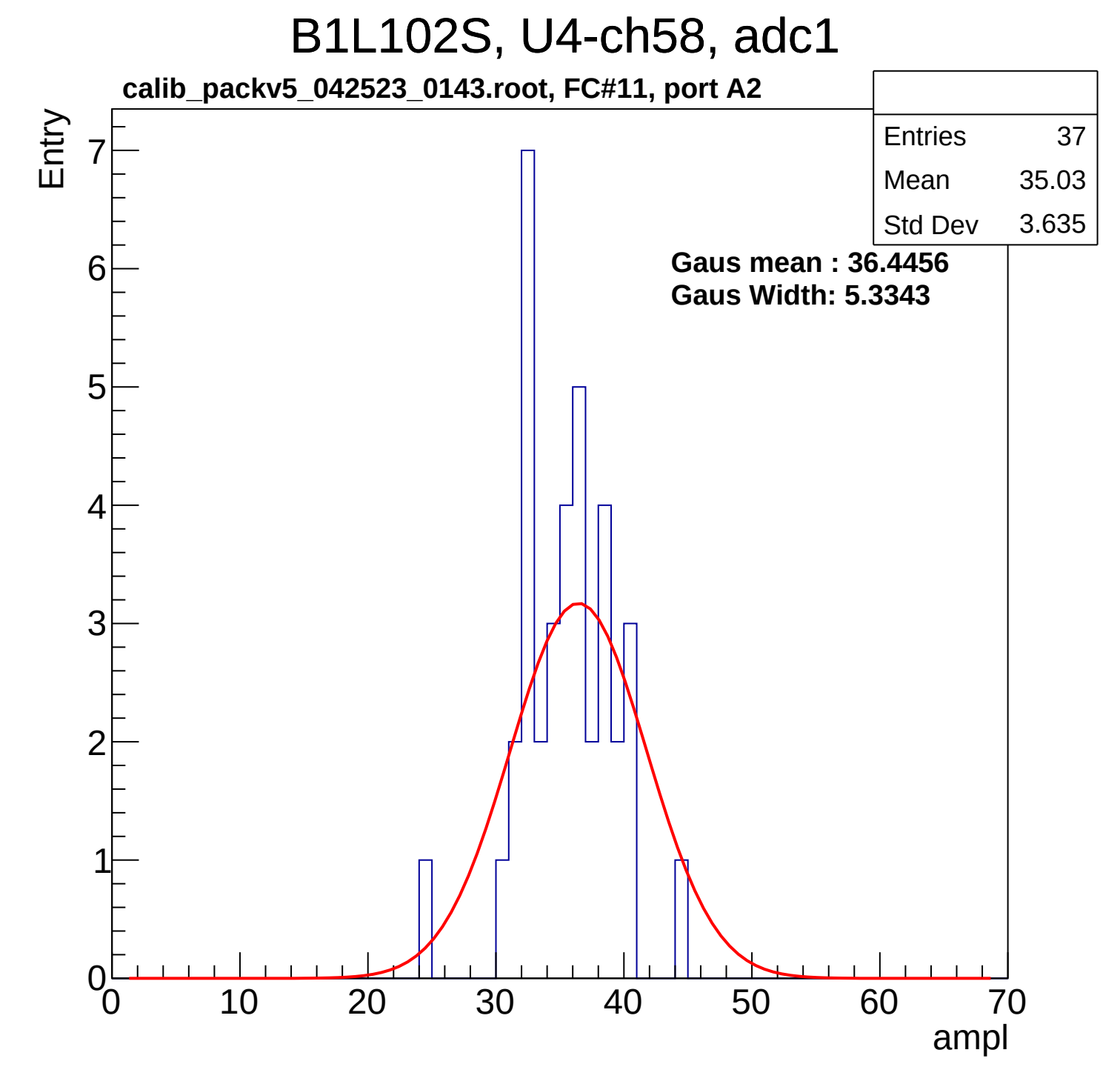
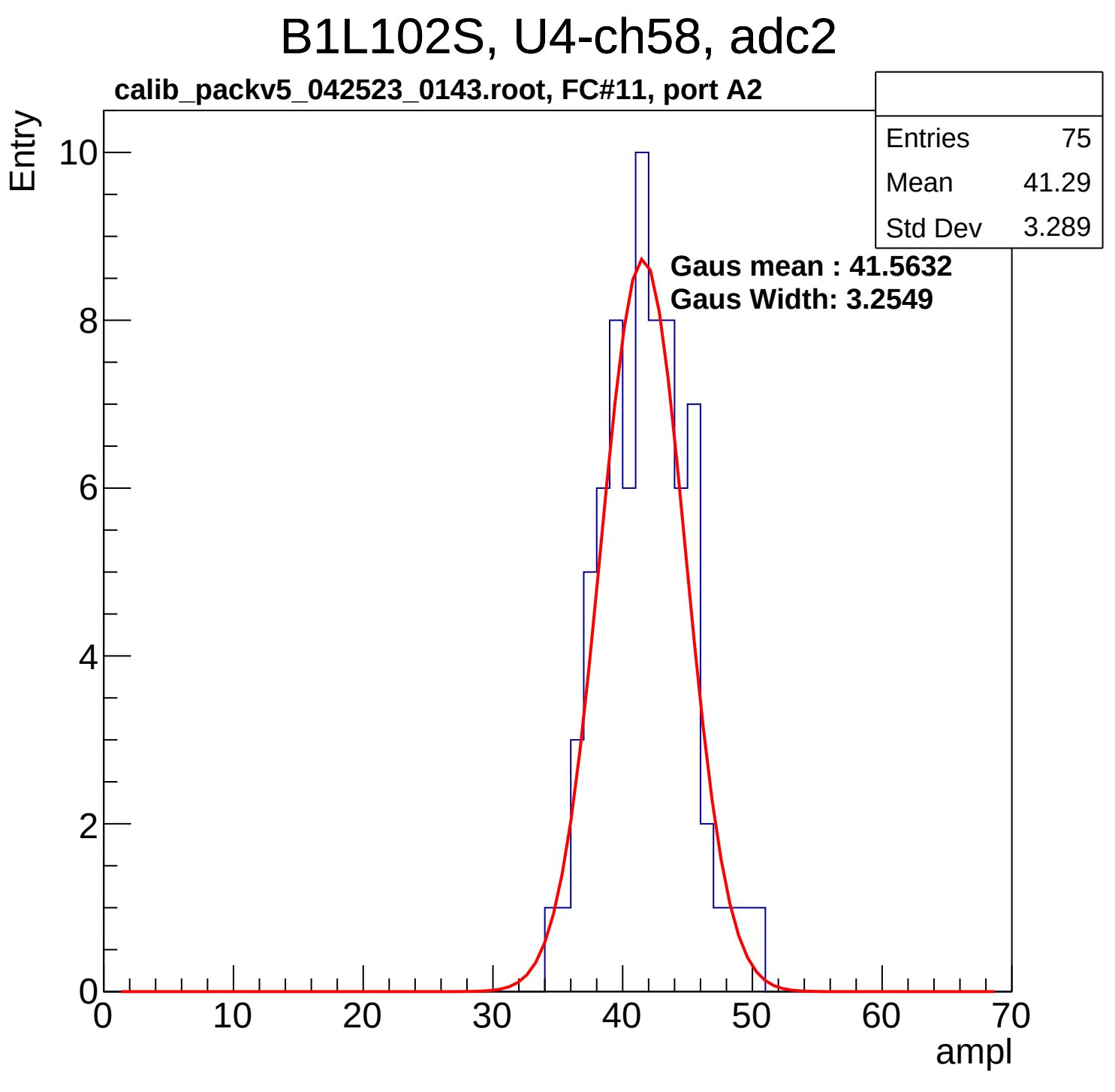
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch57, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch58, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 89
Mean 28.98
Std Dev 5.05
Gaus mean : 29.9127
Gaus Width: 4.7326
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch58, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 37
Mean 35.03
Std Dev 3.635
Gaus mean : 36.4456
Gaus Width: 5.3343
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch58, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 41.29
Std Dev 3.289
Gaus mean : 41.5632
Gaus Width: 3.2549
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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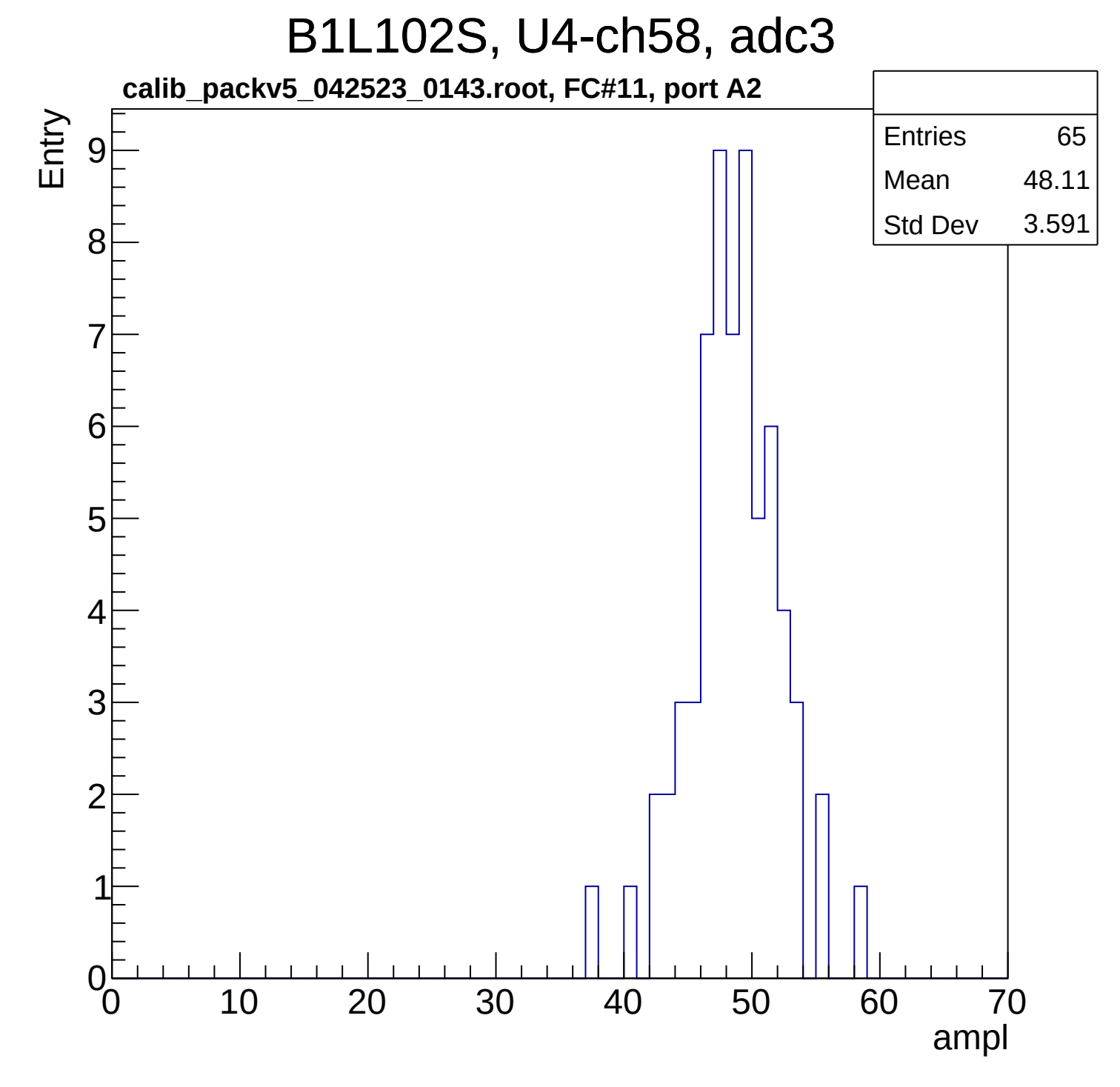
B1L102S, U4-ch58, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 48.11
Std Dev 3.591
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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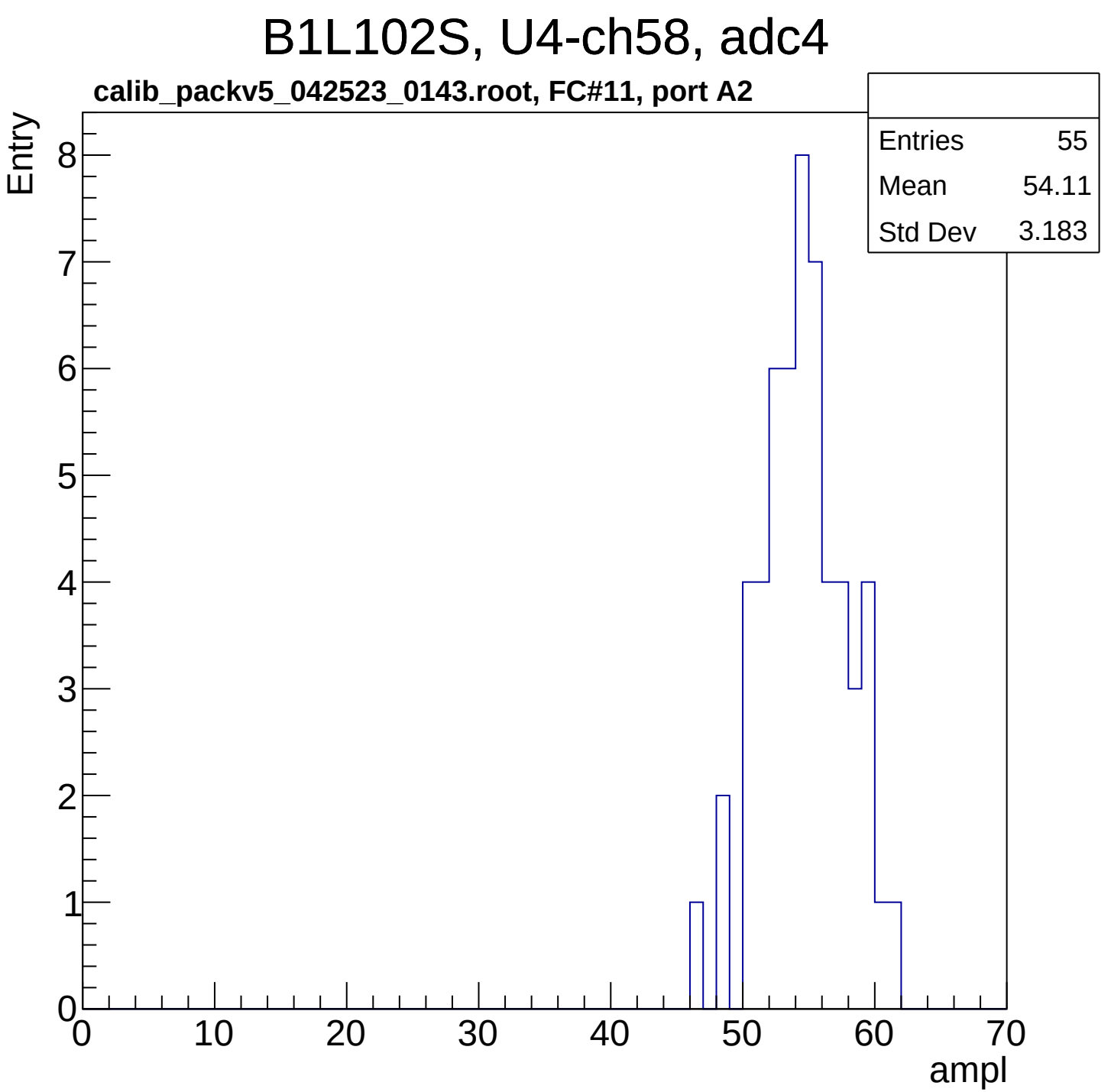
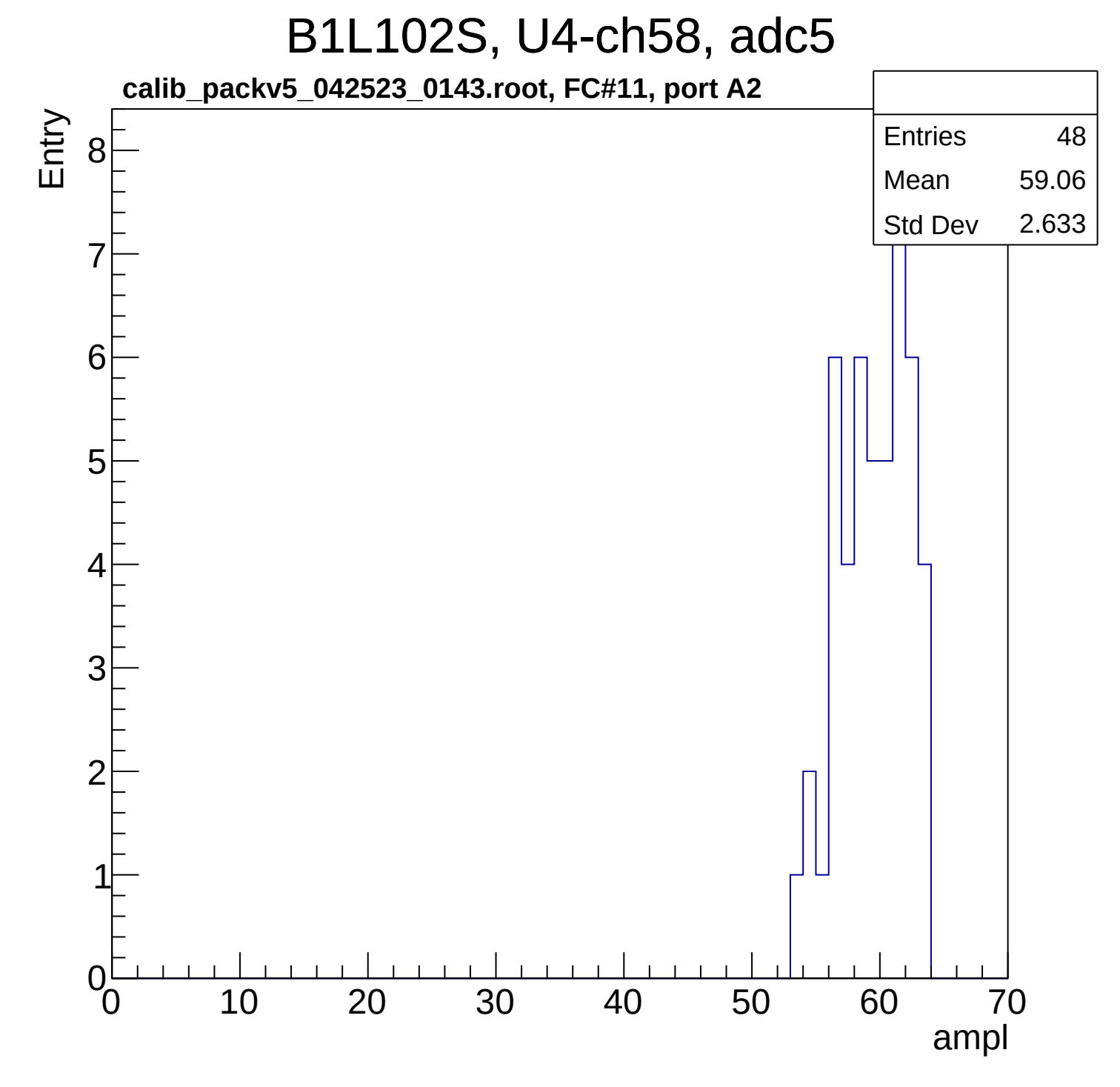

B1L102S, U4-ch58, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 54.11
Std Dev 3.183
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch58, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 48
Mean 59.06
Std Dev 2.633
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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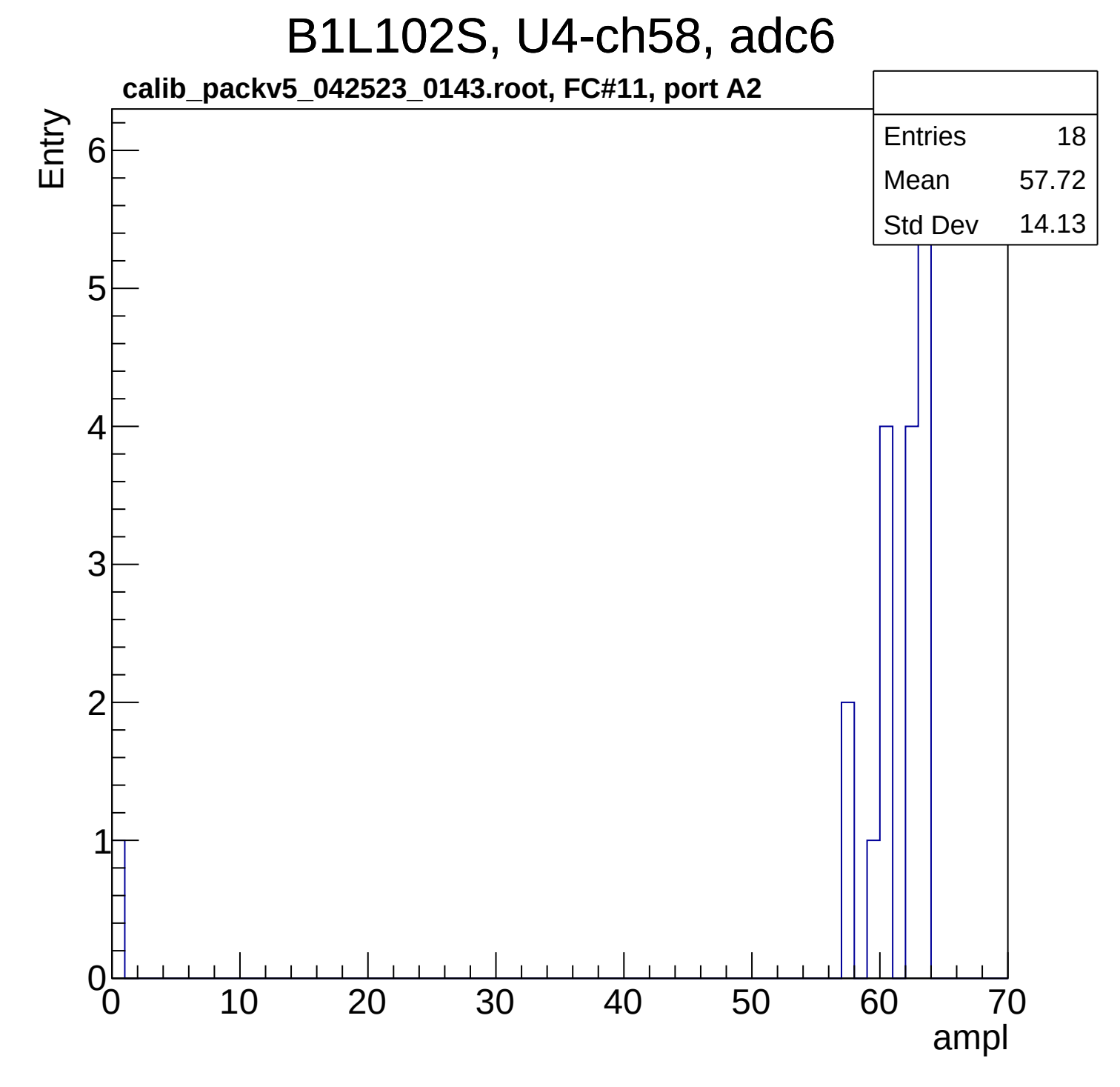
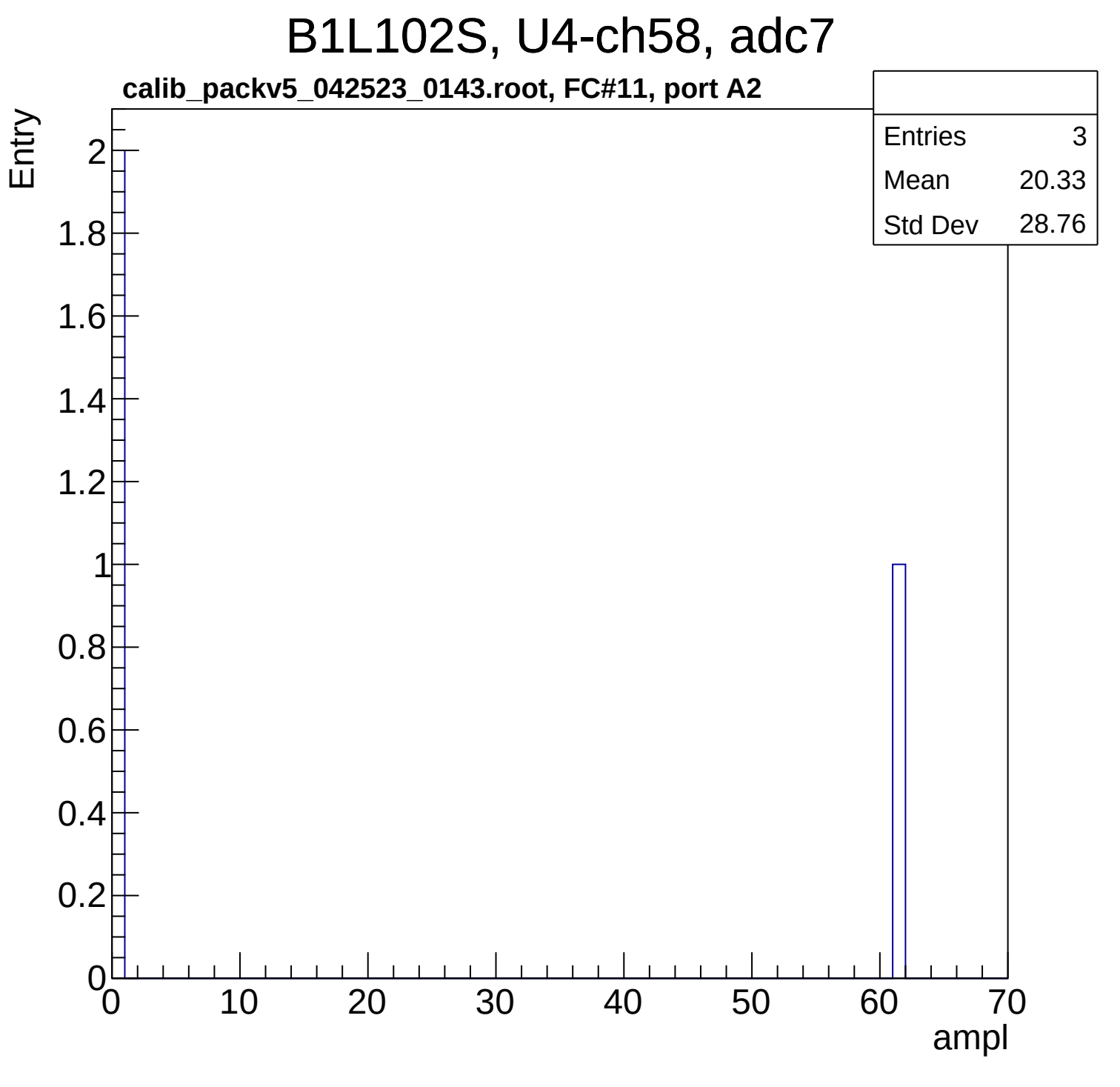
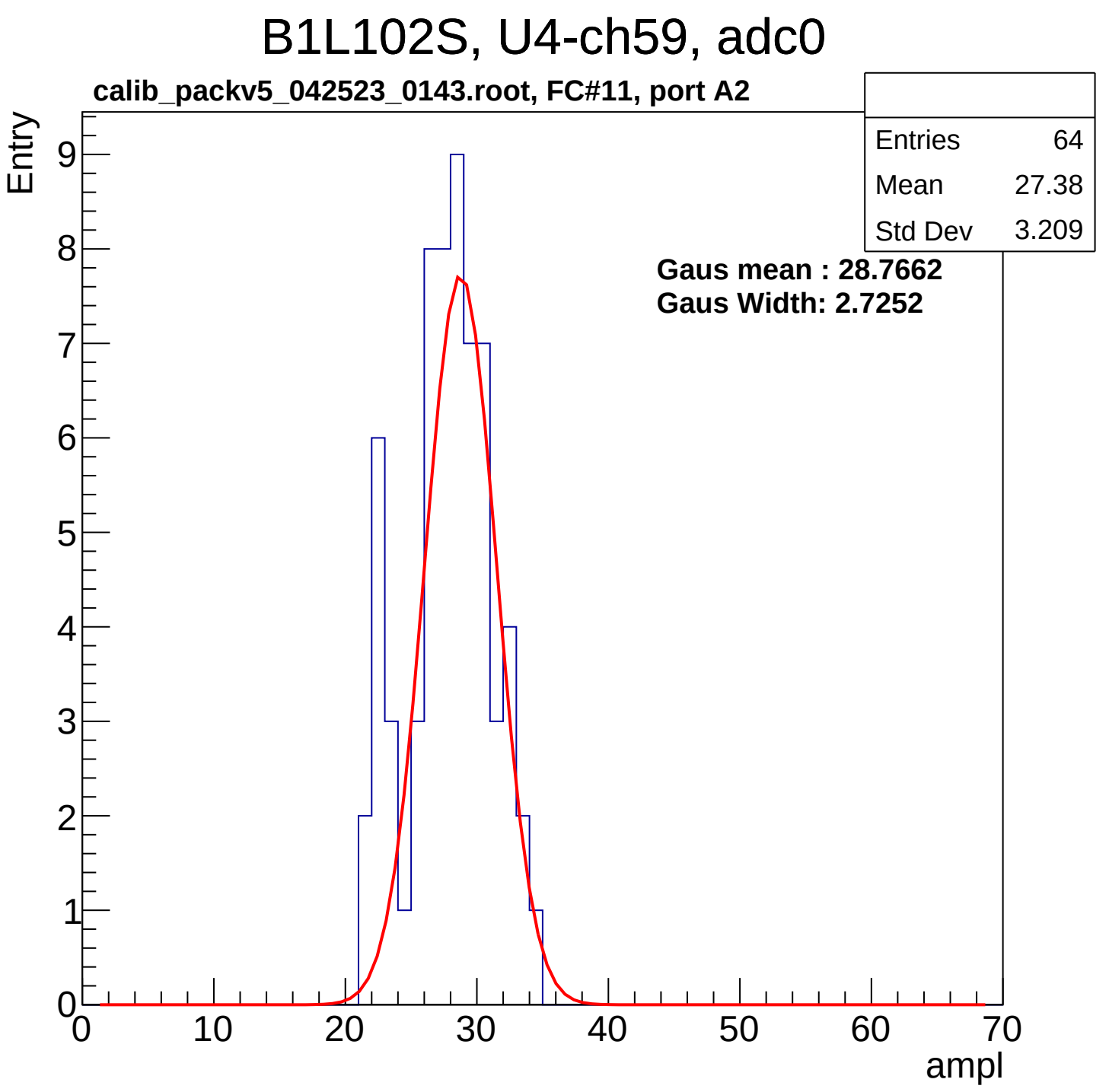
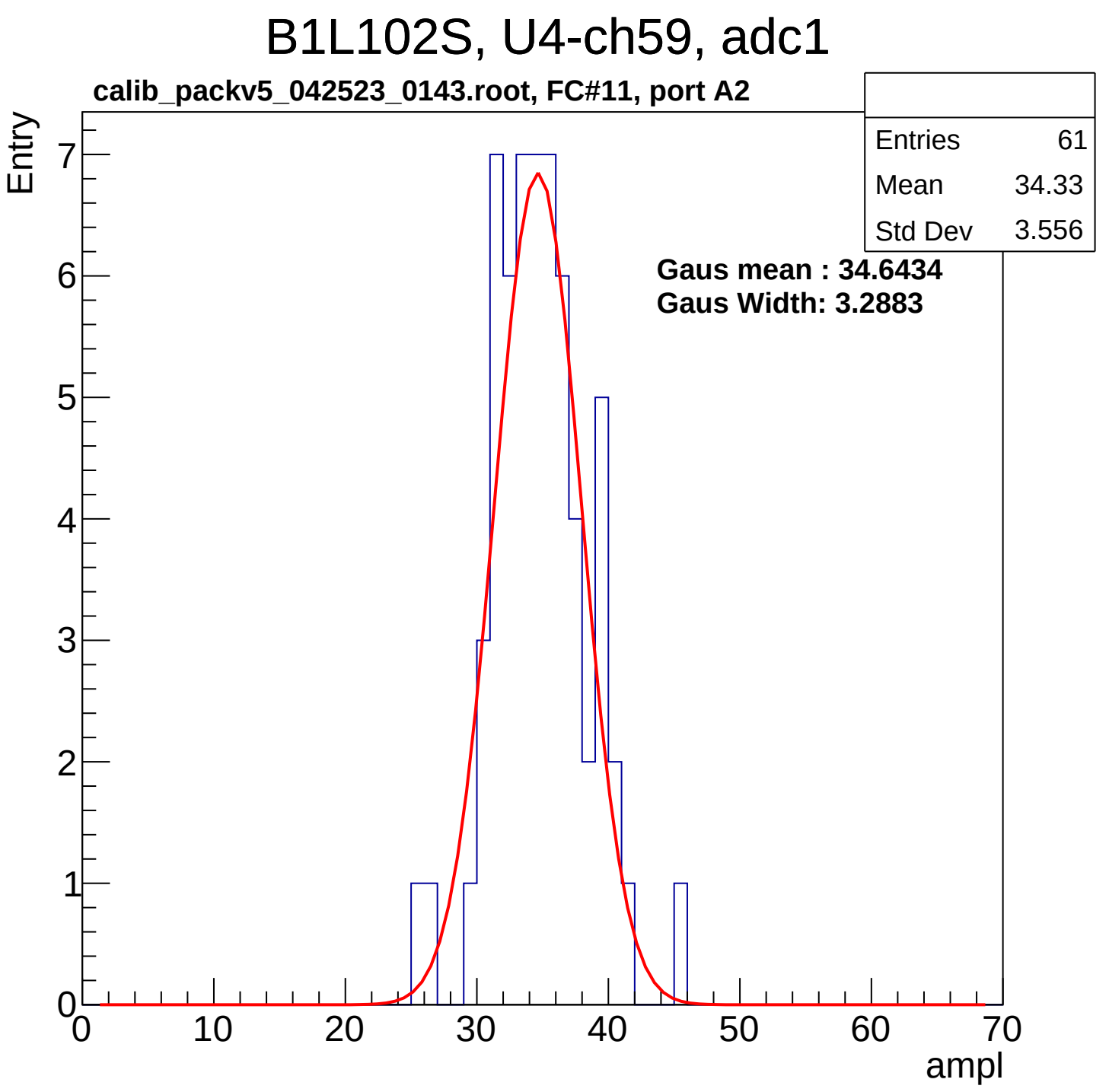
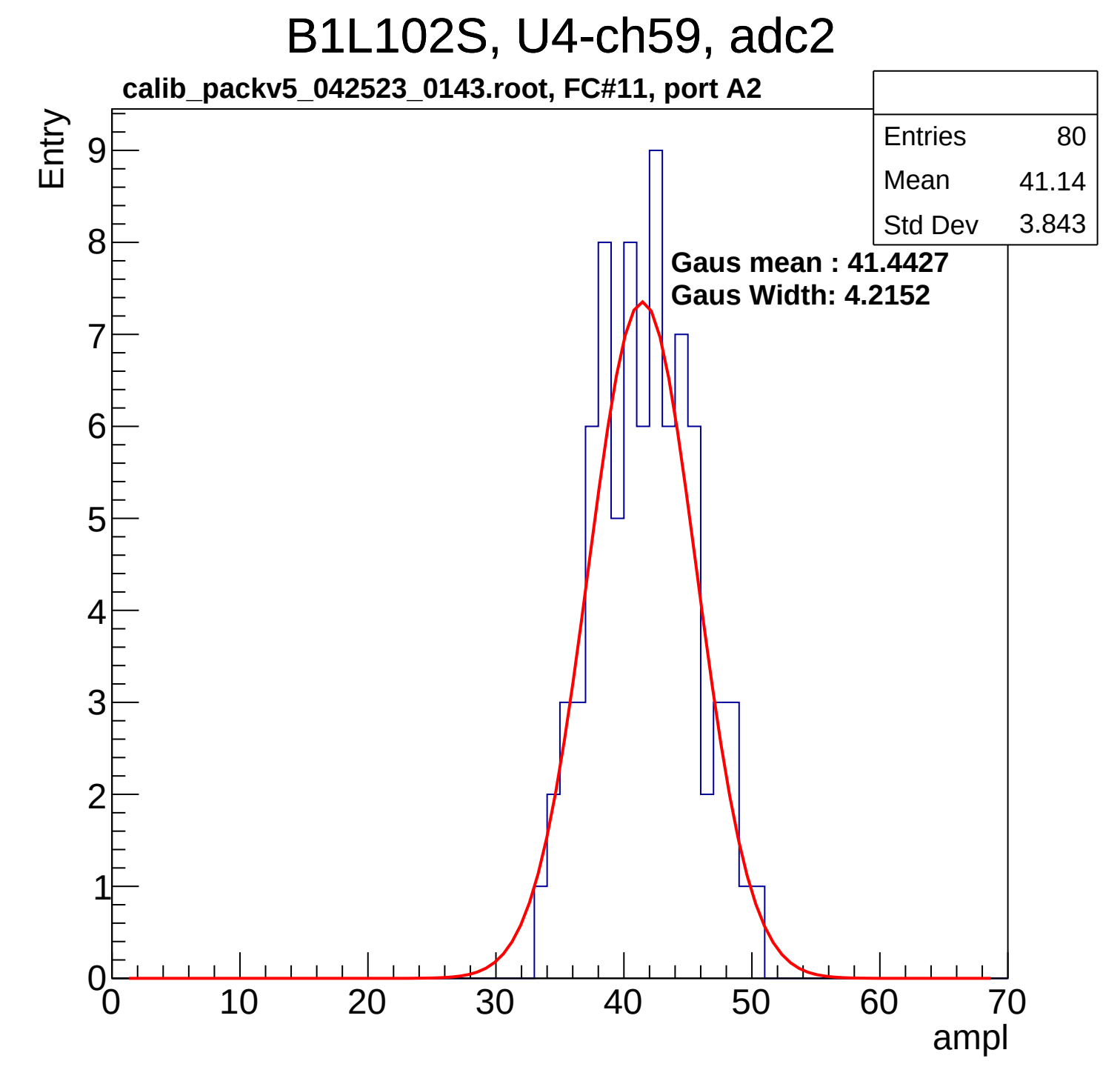
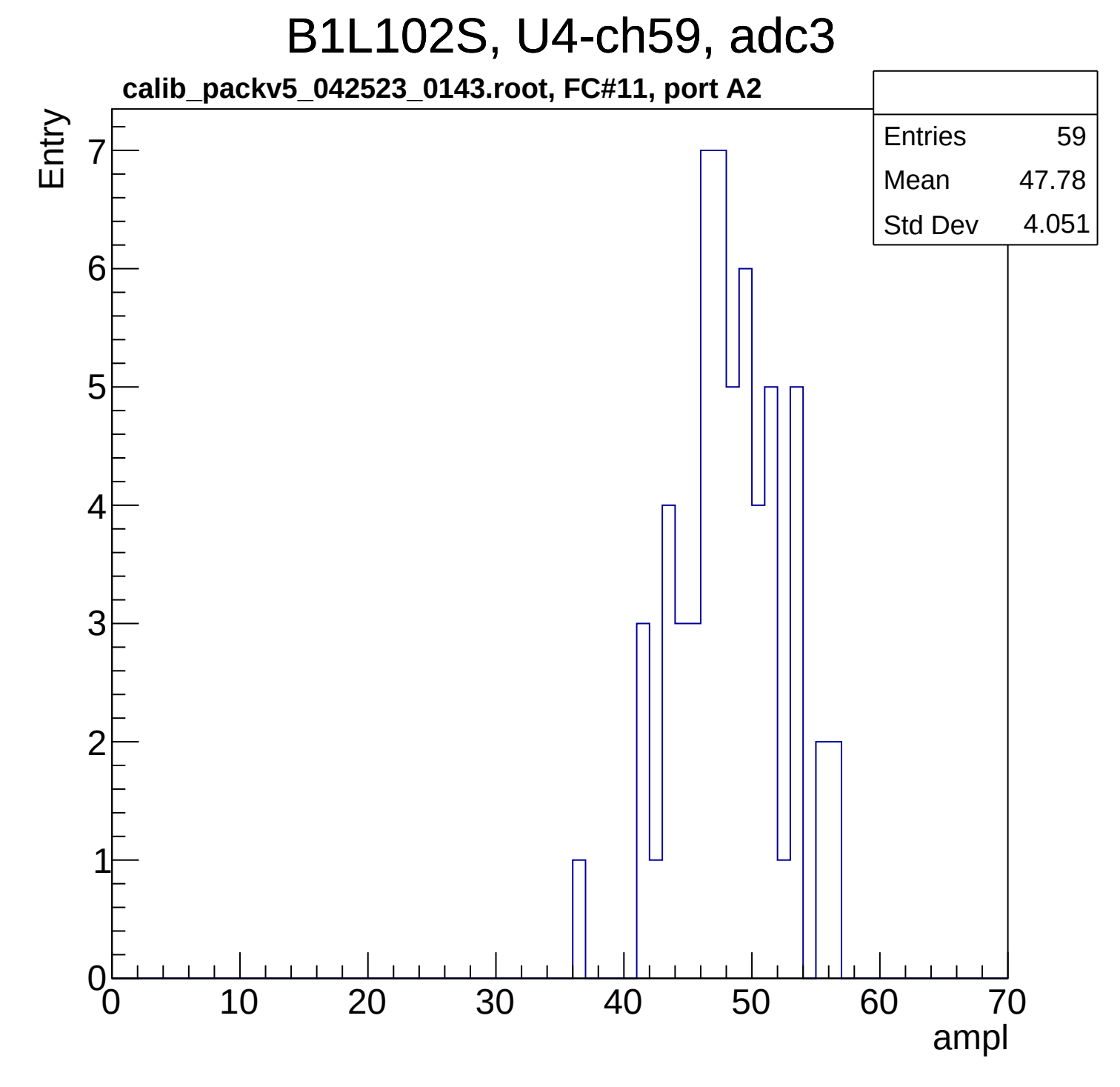

B1L102S, U4-ch58, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 18
Mean 57.72
Std Dev 14.13
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

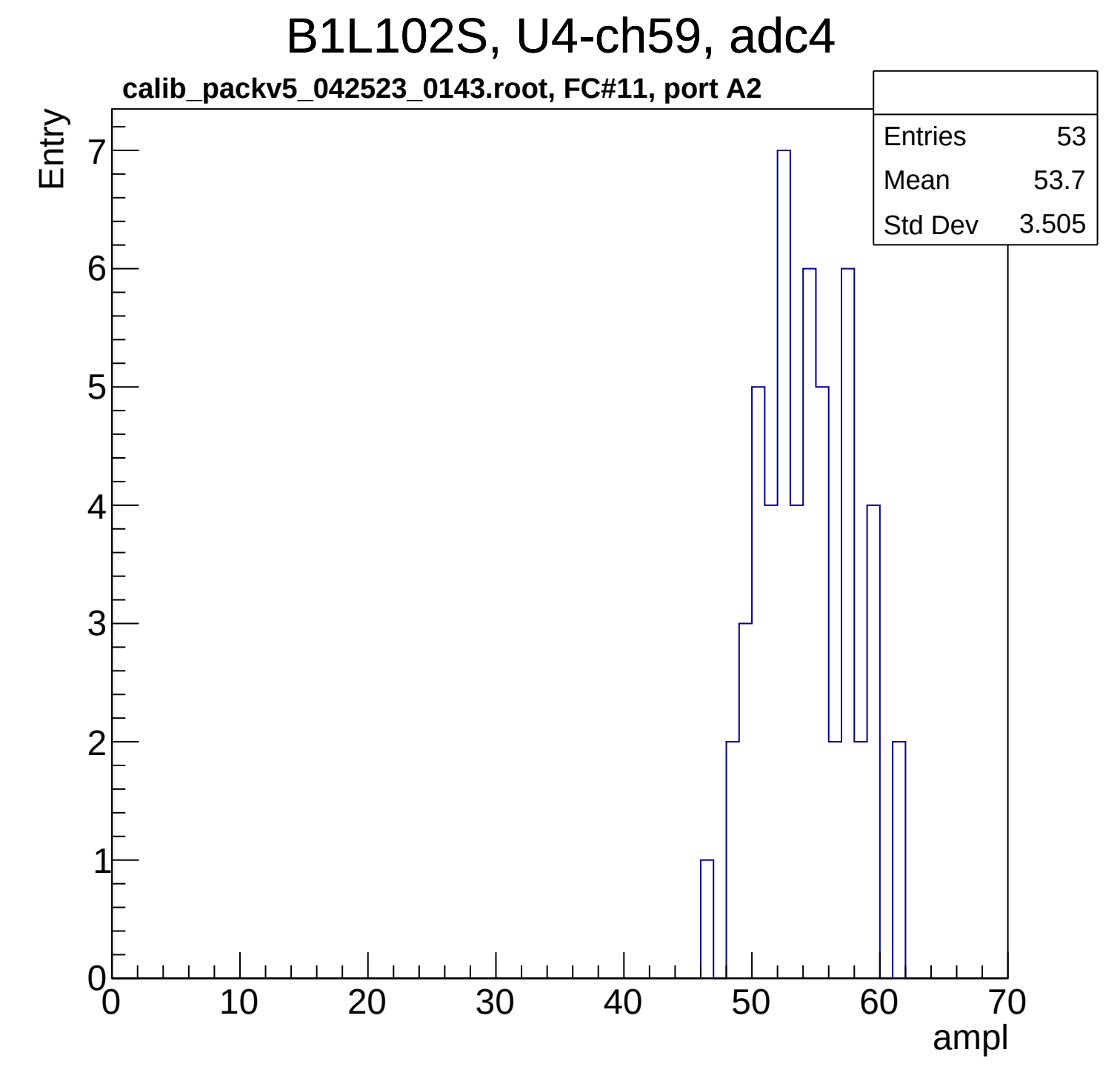

B1L102S, U4-ch58, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 20.33
Std Dev 28.76
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

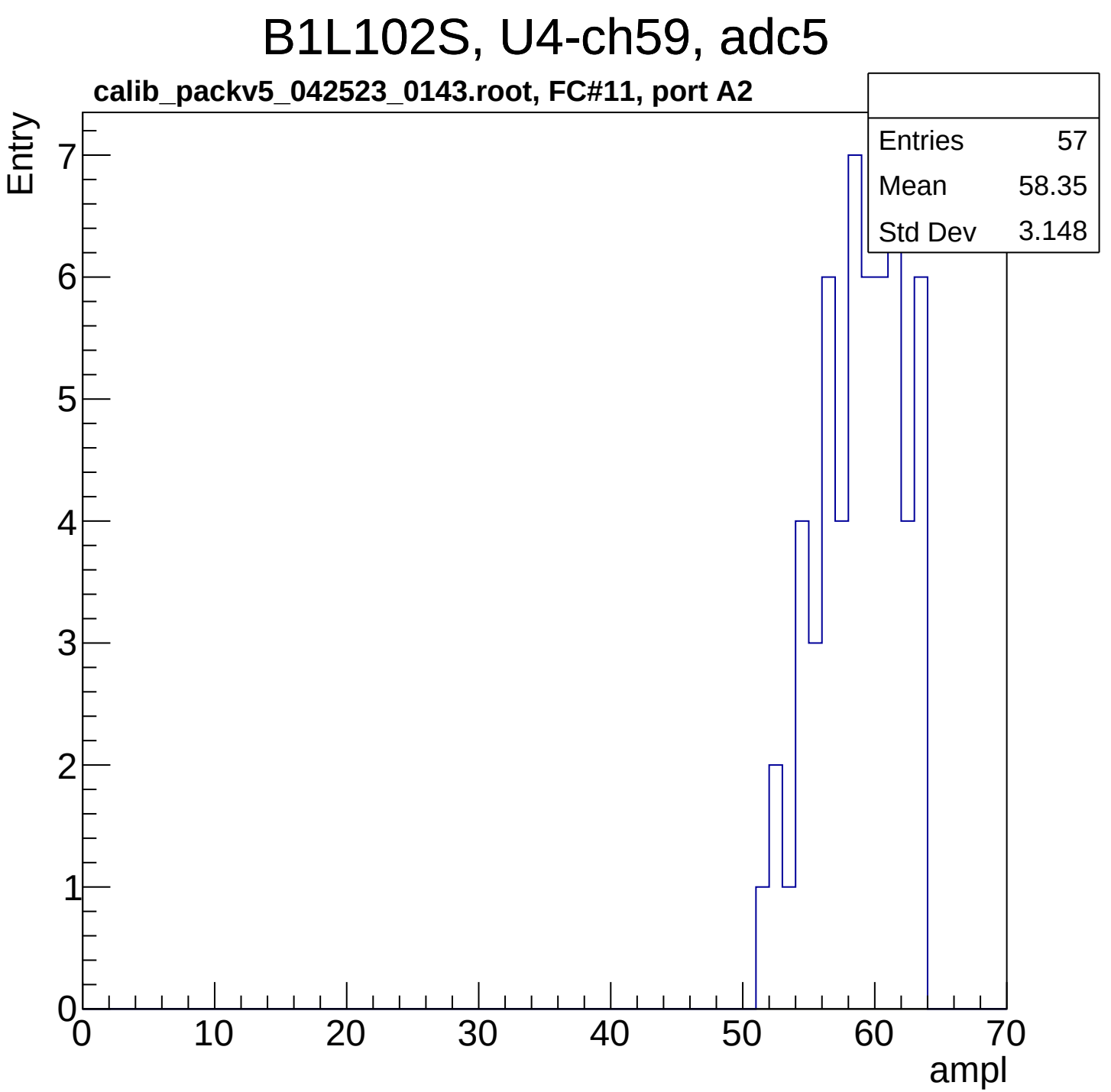

B1L102S, U4-ch59, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 27.38
Std Dev 3.209
Gaus mean : 28.7662
Gaus Width: 2.7252
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

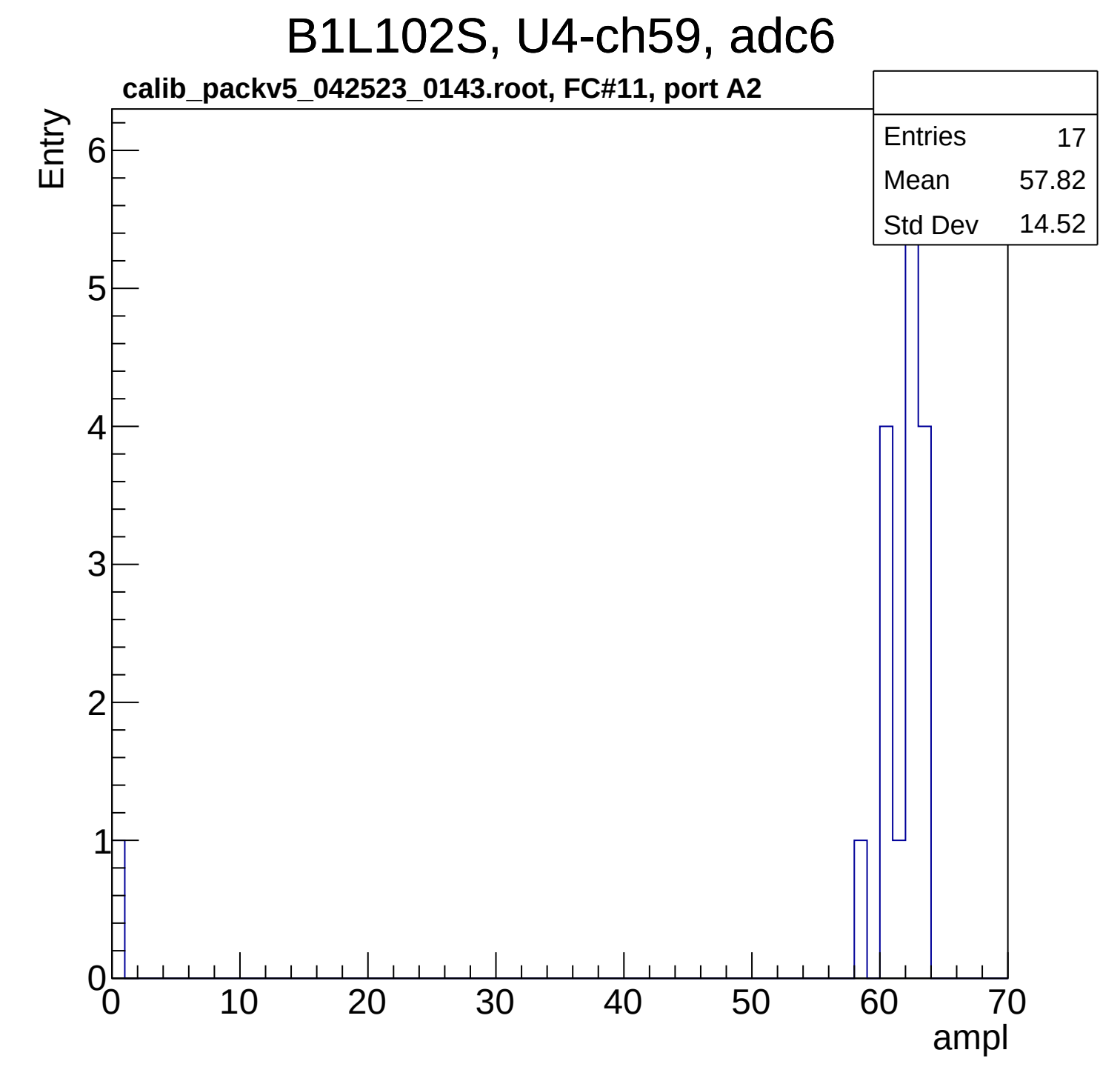

B1L102S, U4-ch59, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 34.33
Std Dev 3.556
Gaus mean : 34.6434
Gaus Width: 3.2883
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

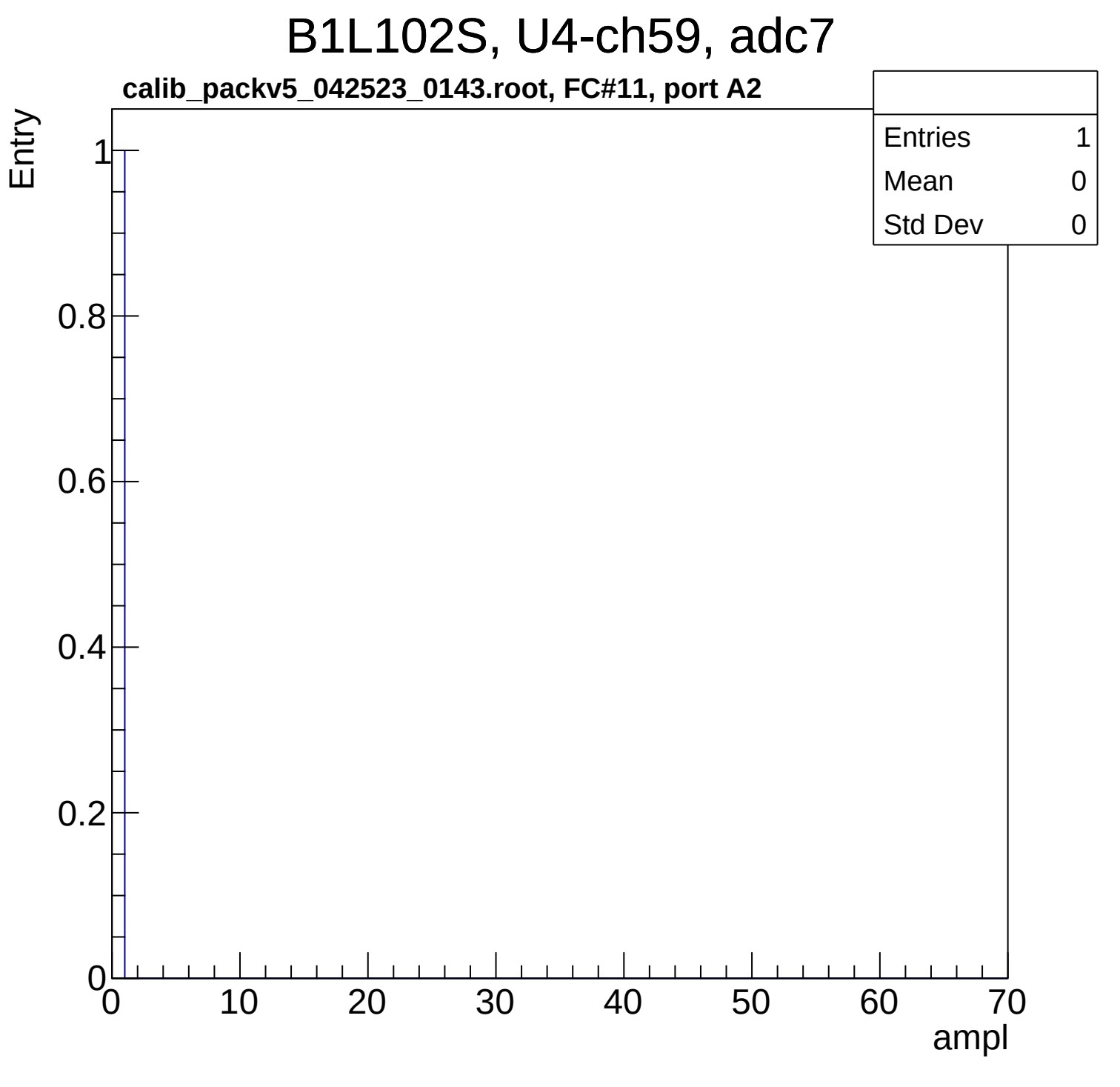

B1L102S, U4-ch59, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 80
Mean 41.14
Std Dev 3.843
Gaus mean : 41.4427
Gaus Width: 4.2152
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

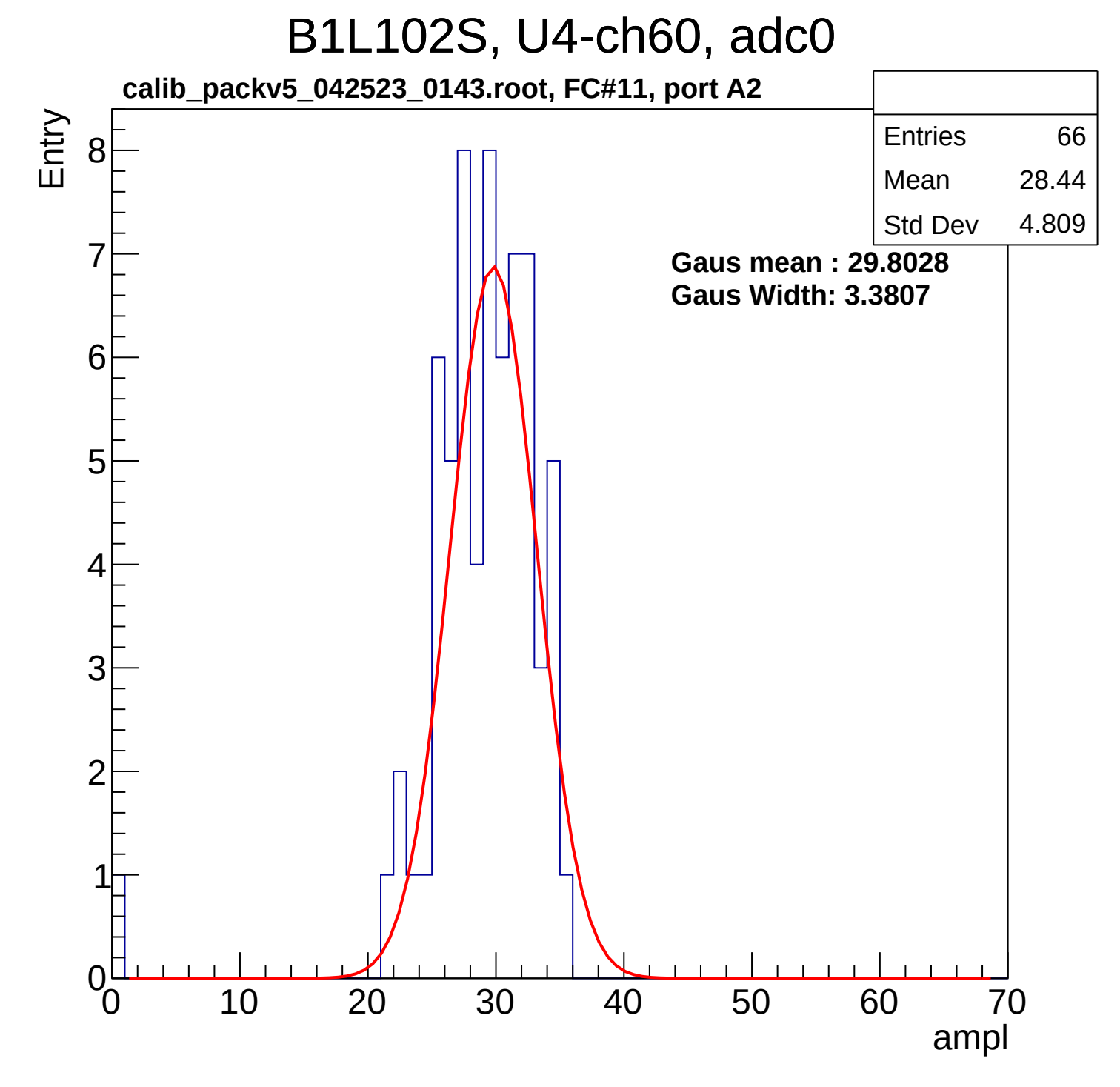

B1L102S, U4-ch59, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 47.78
Std Dev 4.051
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

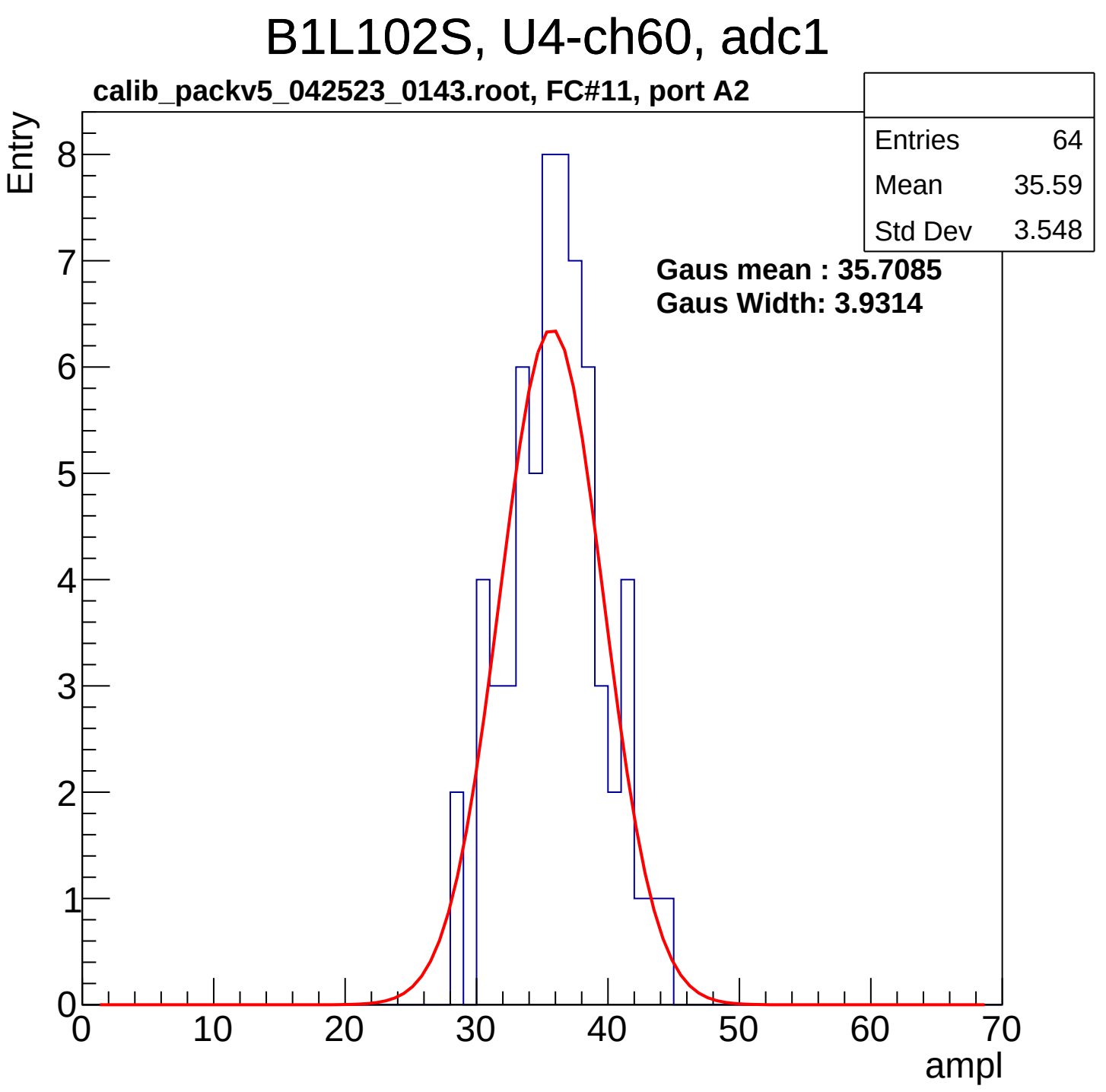

B1L102S, U4-ch59, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 53.7
Std Dev 3.505
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

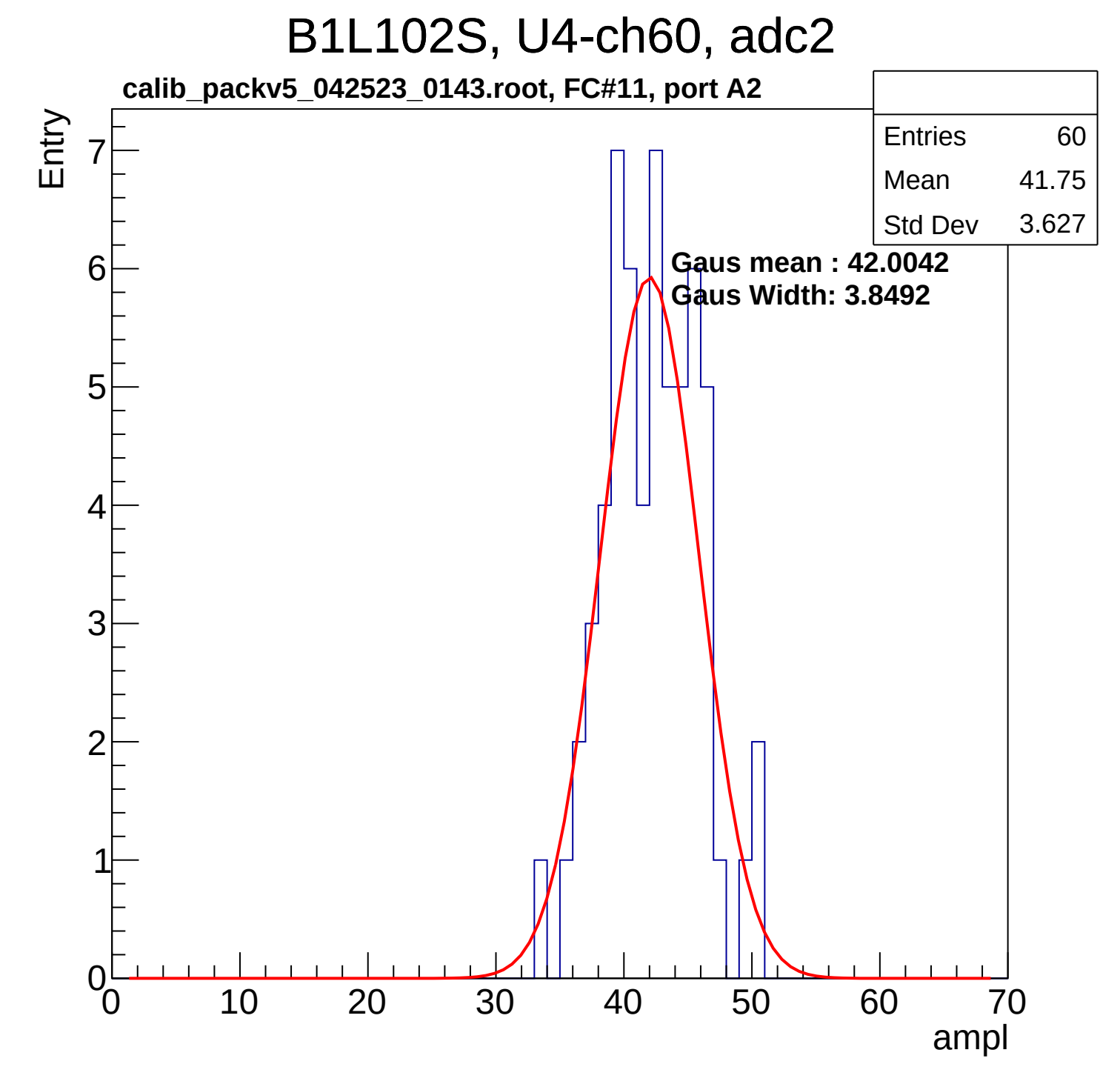

B1L102S, U4-ch59, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 57
Mean 58.35
Std Dev 3.148
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

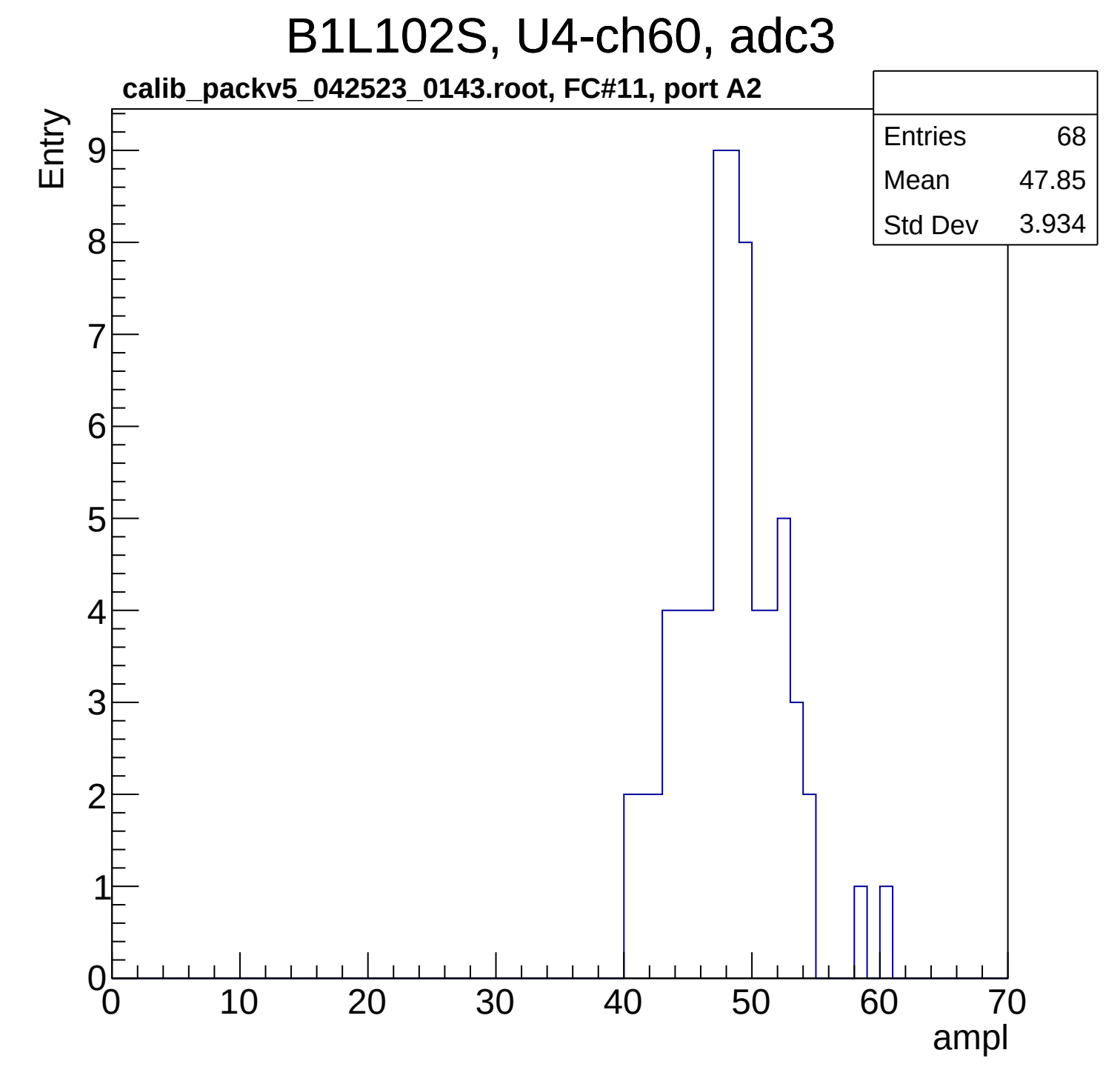

B1L102S, U4-ch59, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 17
Mean 57.82
Std Dev 14.52
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch59, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch60, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 28.44
Std Dev 4.809
Gaus mean : 29.8028
Gaus Width: 3.3807
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch60, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 35.59
Std Dev 3.548
Gaus mean : 35.7085
Gaus Width: 3.9314
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch60, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 41.75
Std Dev 3.627
Gaus mean : 42.0042
Gaus Width: 3.8492
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch60, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 47.85
Std Dev 3.934
Entry
ampl
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2
3
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5
6
7
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9
0
10
20
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40
50
60
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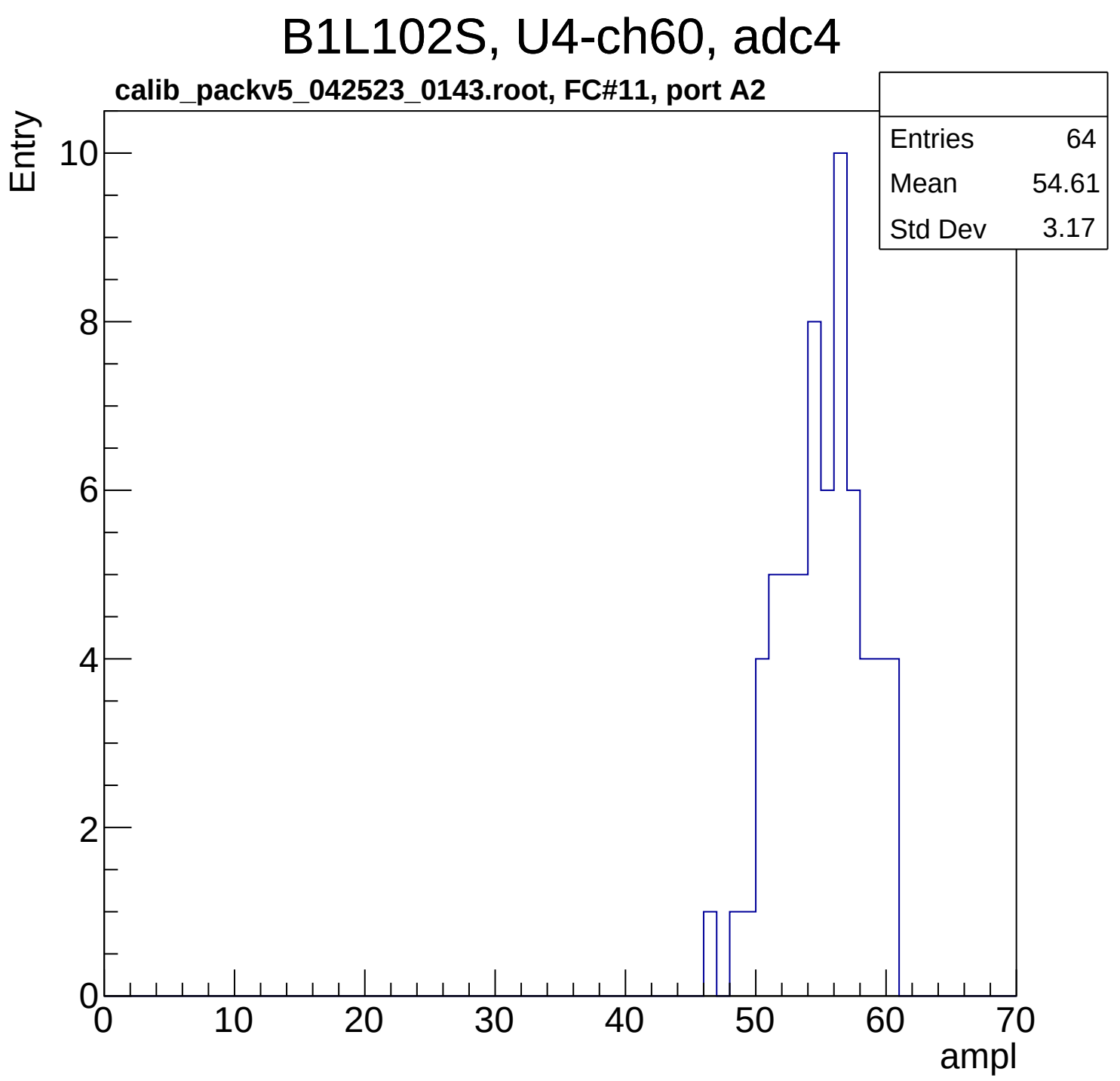
B1L102S, U4-ch60, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 54.61
Std Dev 3.17
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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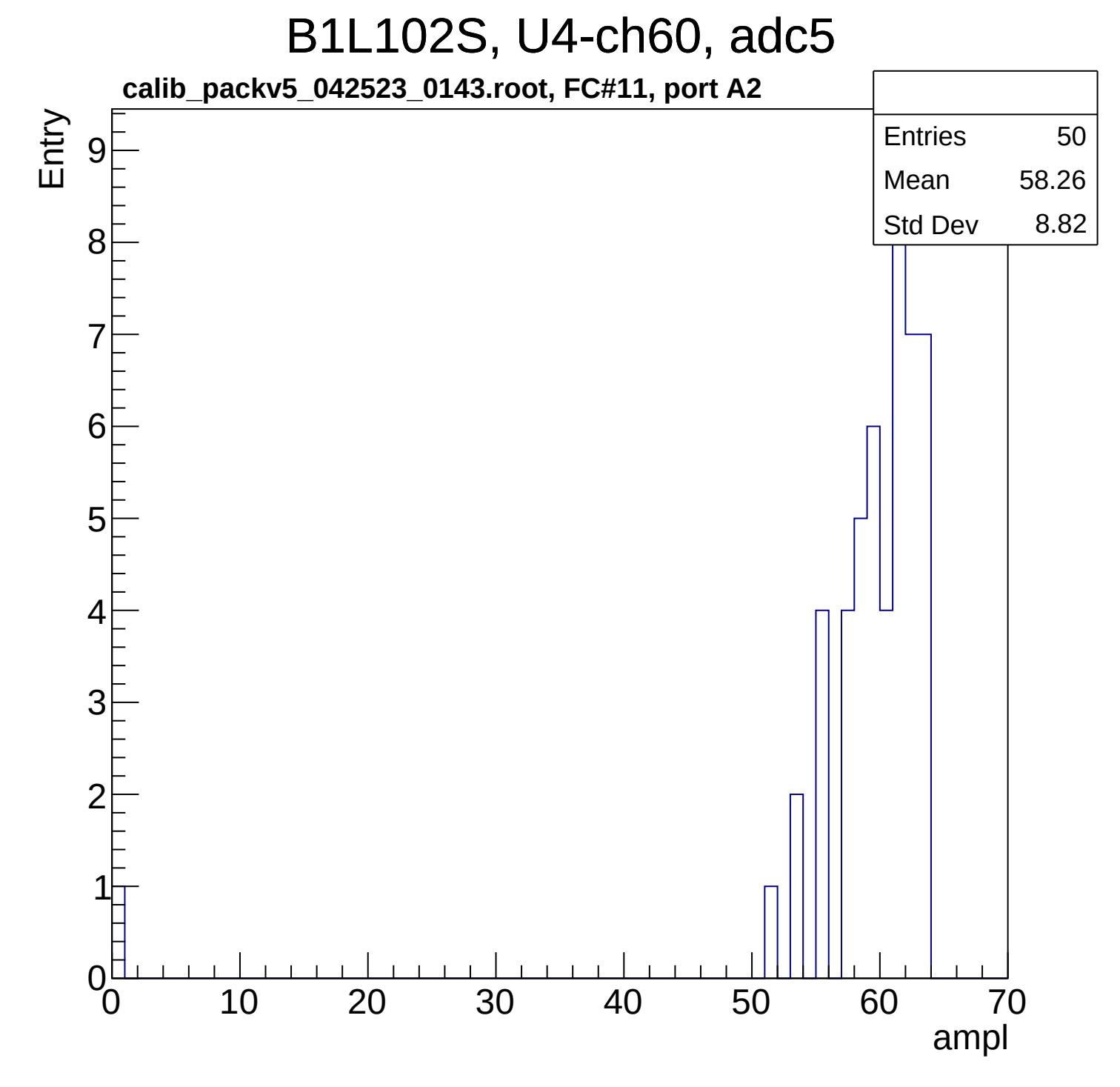
B1L102S, U4-ch60, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 50
Mean 58.26
Std Dev 8.82
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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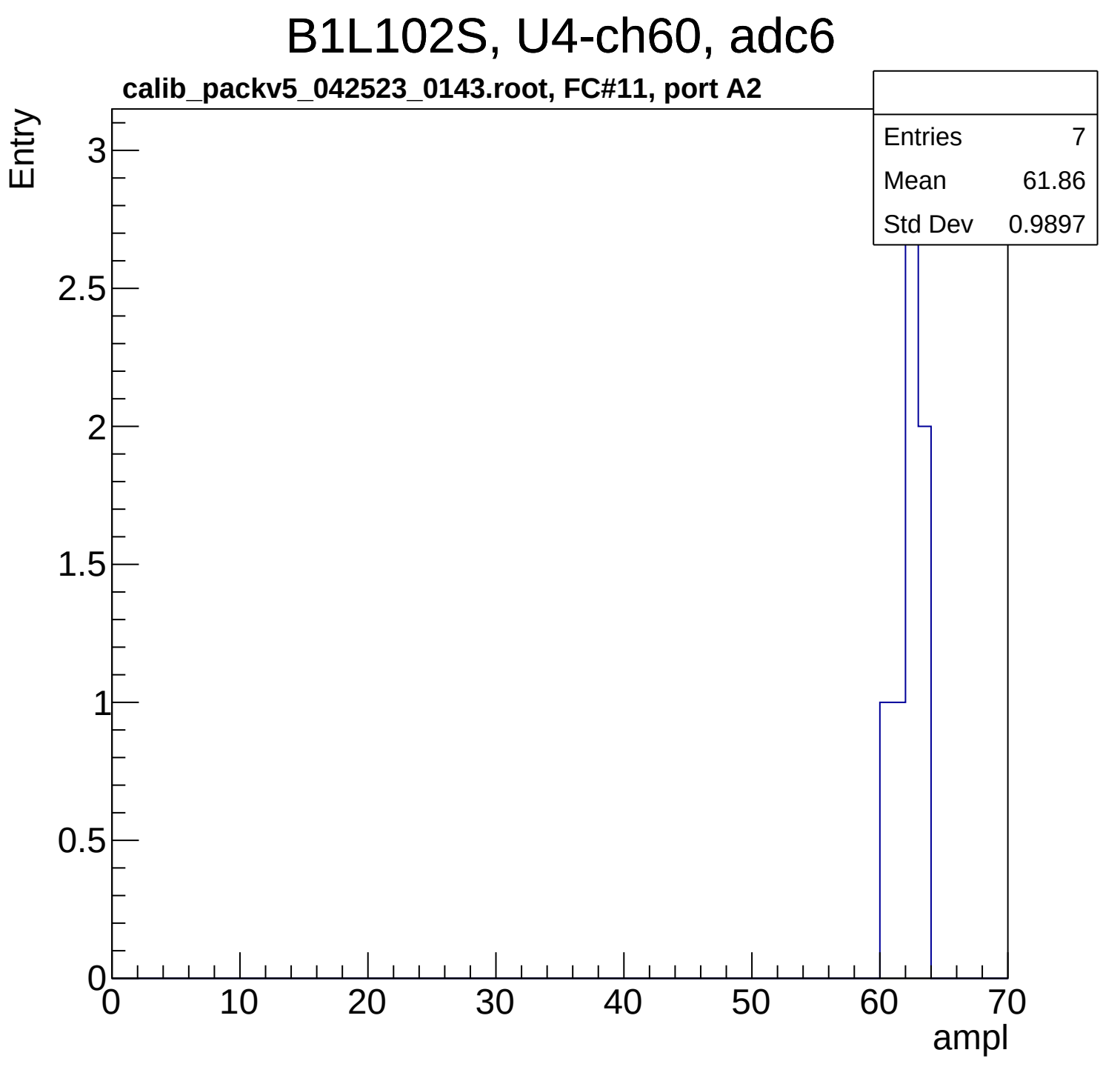
B1L102S, U4-ch60, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 7
Mean 61.86
Std Dev 0.9897
Entry
ampl
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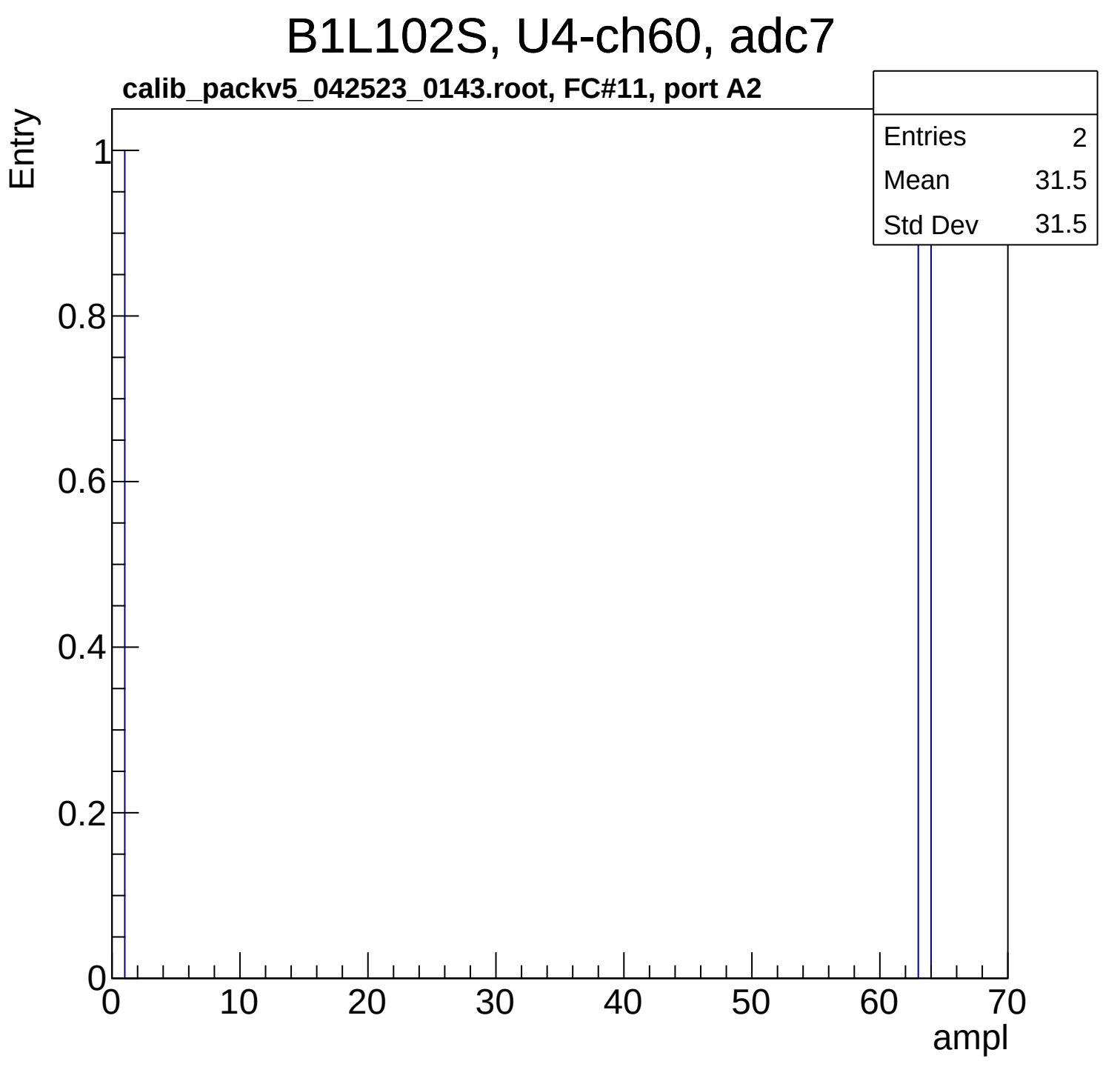
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U4-ch60, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
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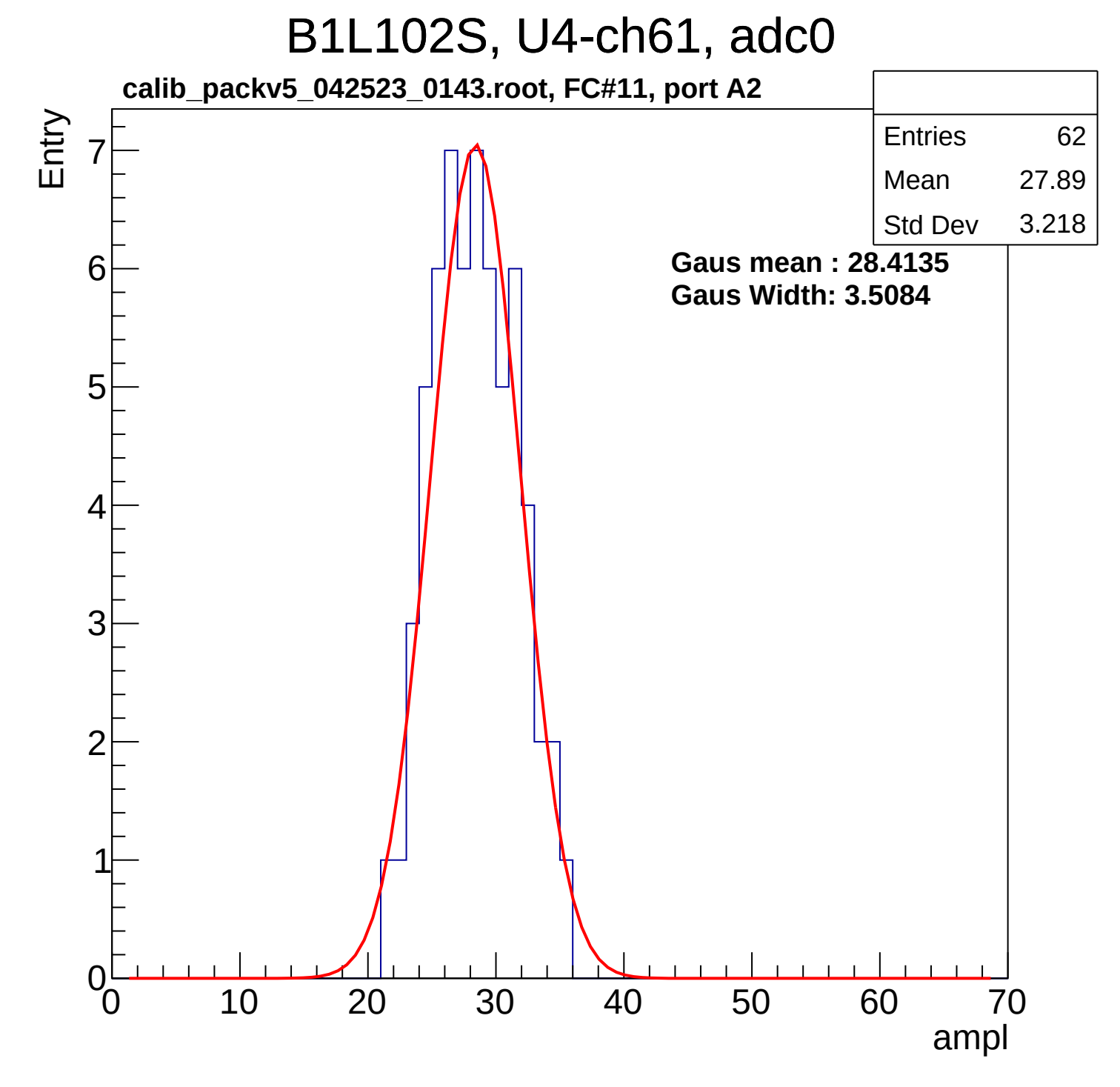
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch61, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 27.89
Std Dev 3.218
Gaus mean : 28.4135
Gaus Width: 3.5084
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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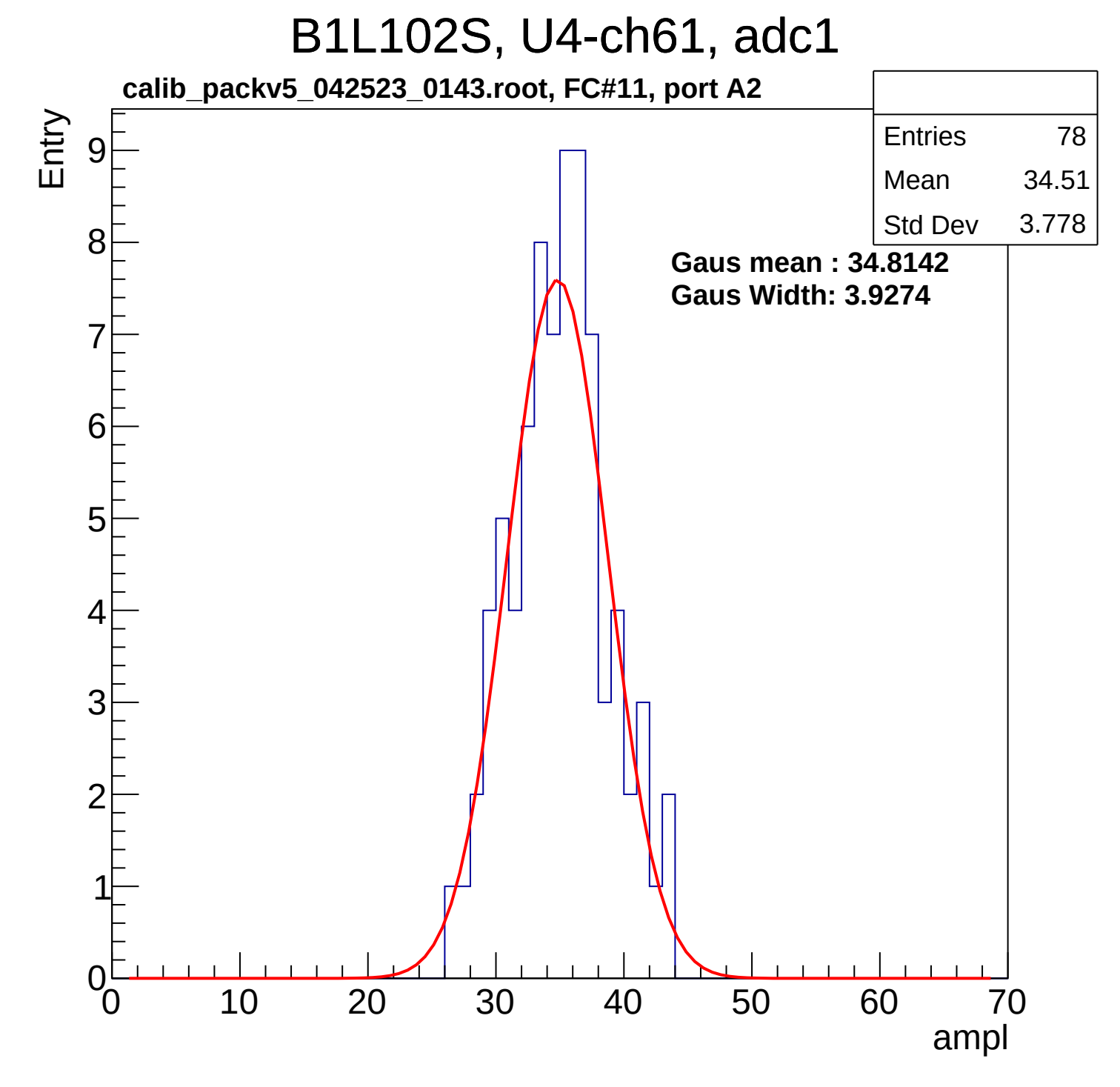
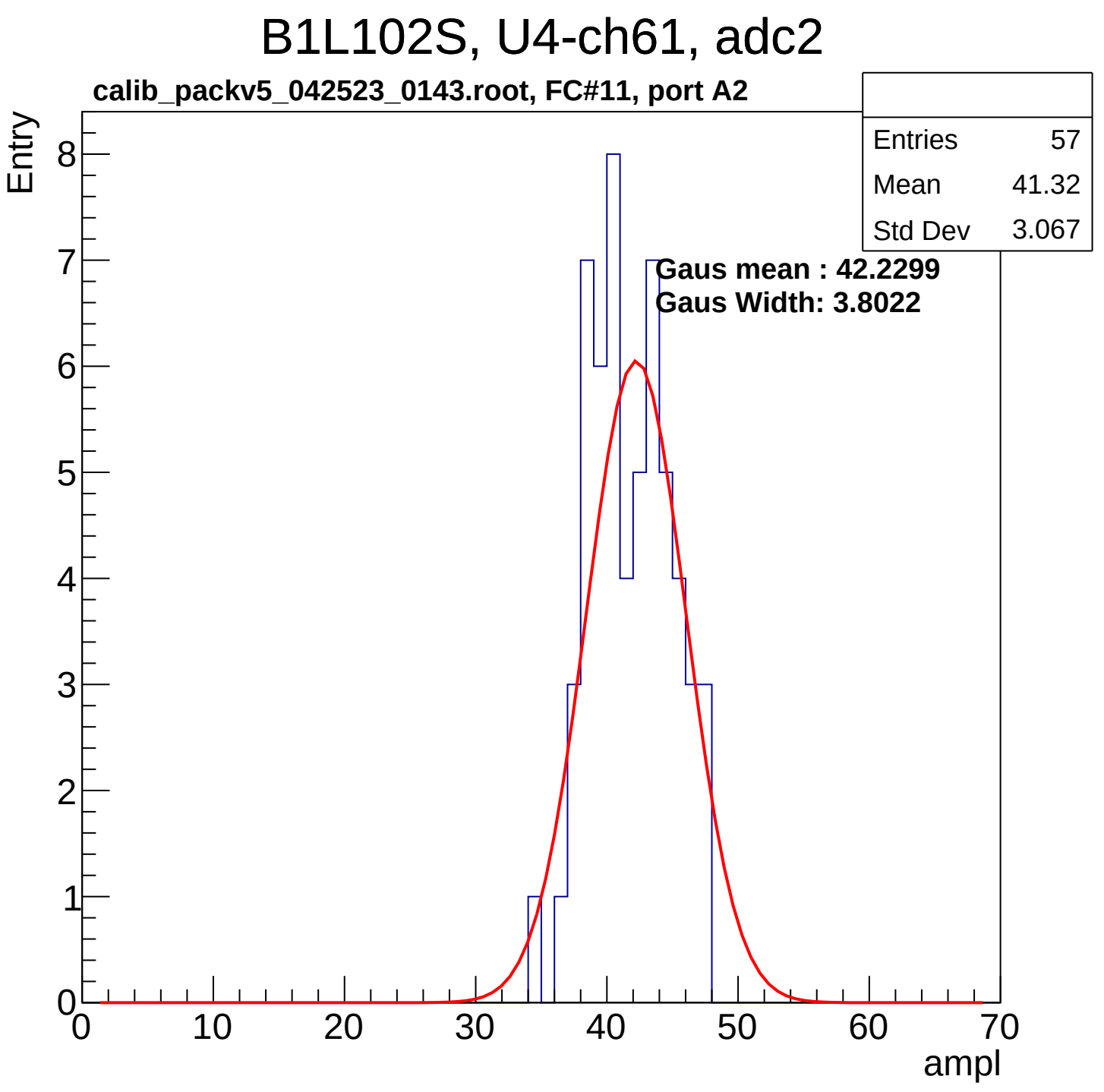
40
50
60
70


B1L102S, U4-ch61, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 78
Mean 34.51
Std Dev 3.778
Gaus mean : 34.8142
Gaus Width: 3.9274
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L102S, U4-ch61, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 57
Mean 41.32
Std Dev 3.067
Gaus mean : 42.2299
Gaus Width: 3.8022
Entry
ampl
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1
2
3
4
5
6
7
8
0
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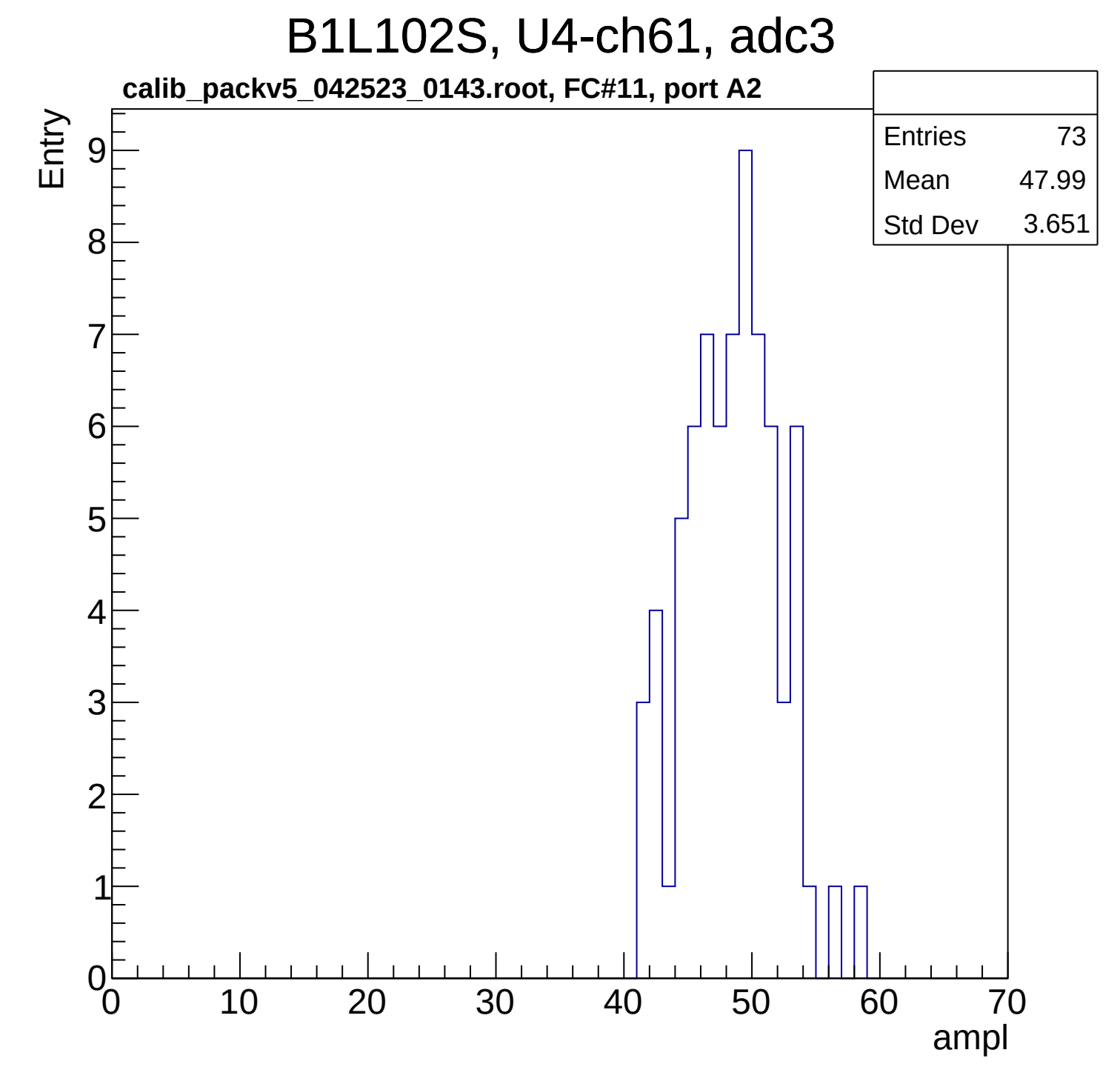
B1L102S, U4-ch61, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 47.99
Std Dev 3.651
Entry
ampl
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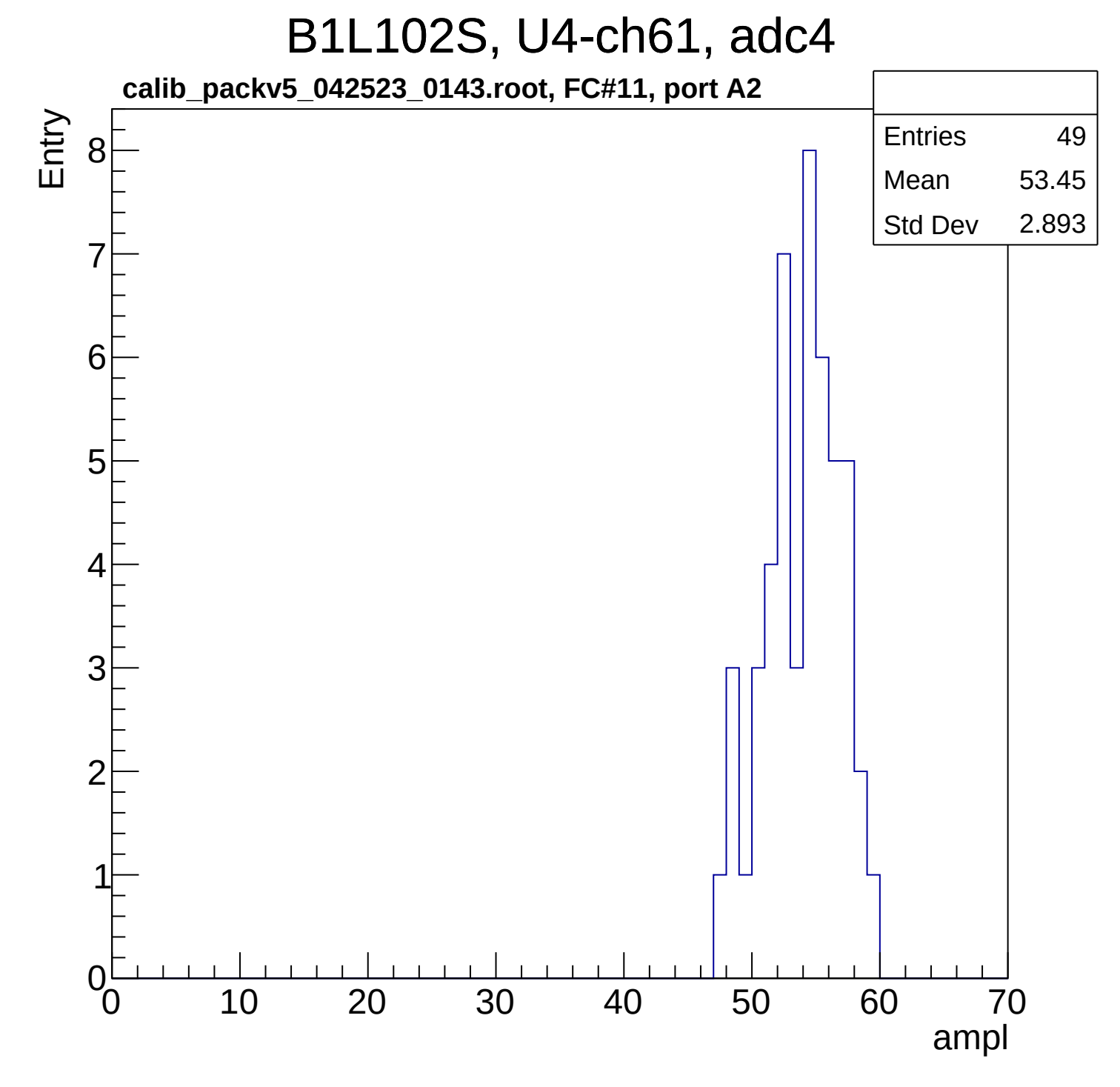
B1L102S, U4-ch61, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 53.45
Std Dev 2.893
Entry
ampl
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60
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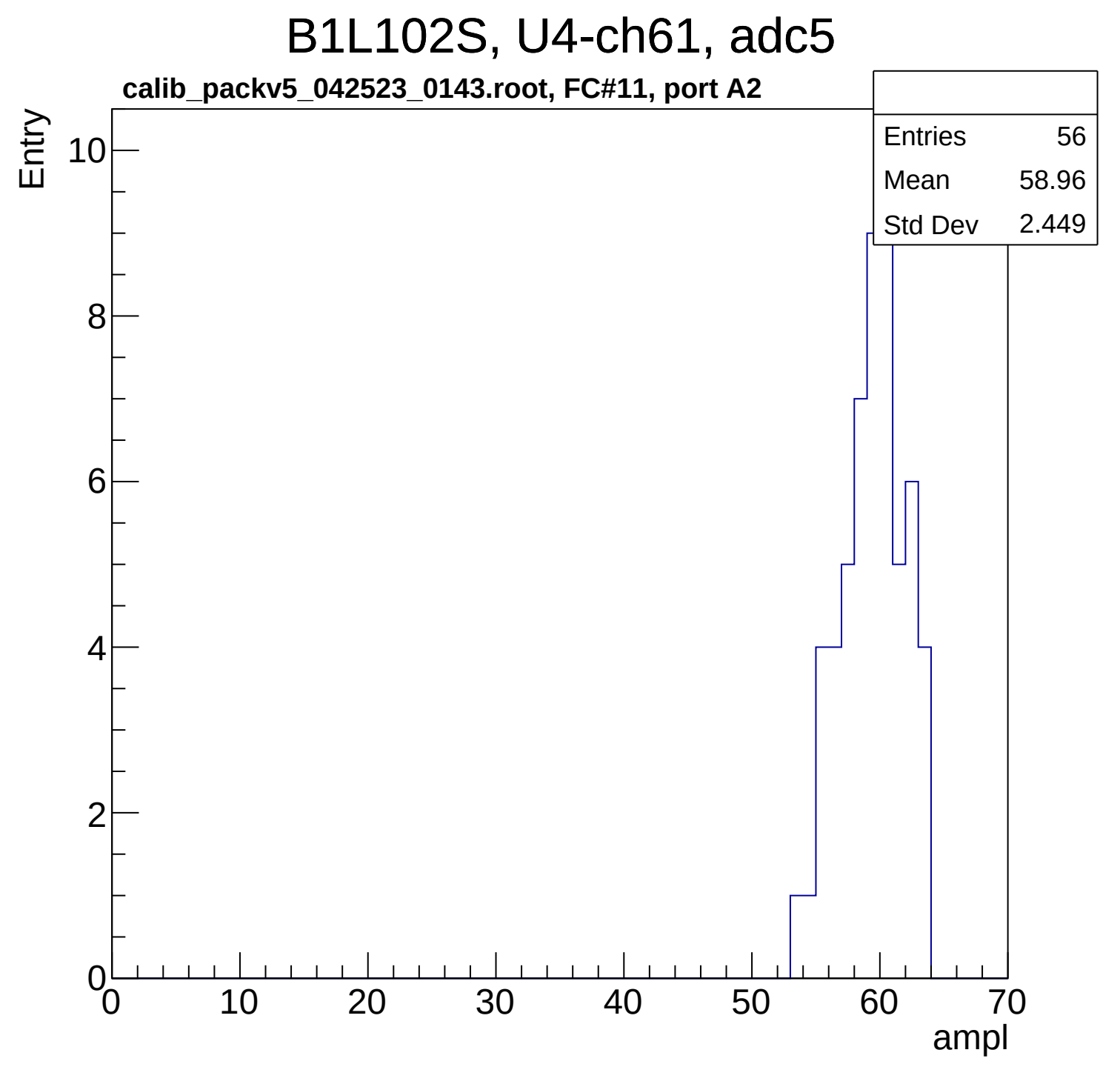
B1L102S, U4-ch61, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 58.96
Std Dev 2.449
Entry
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4
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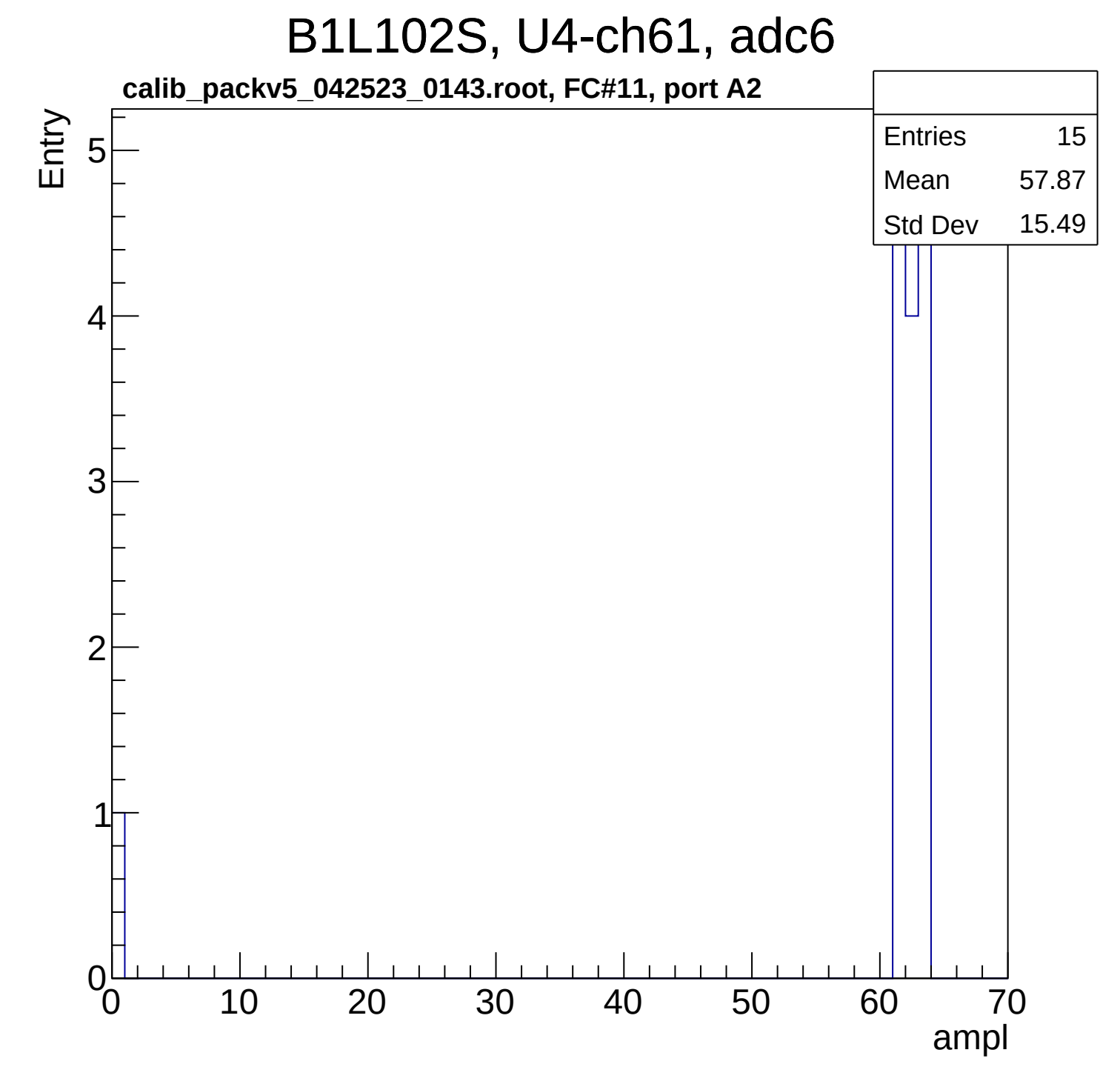
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch61, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 15
Mean 57.87
Std Dev 15.49
Entry
0
1
2
3
4
5
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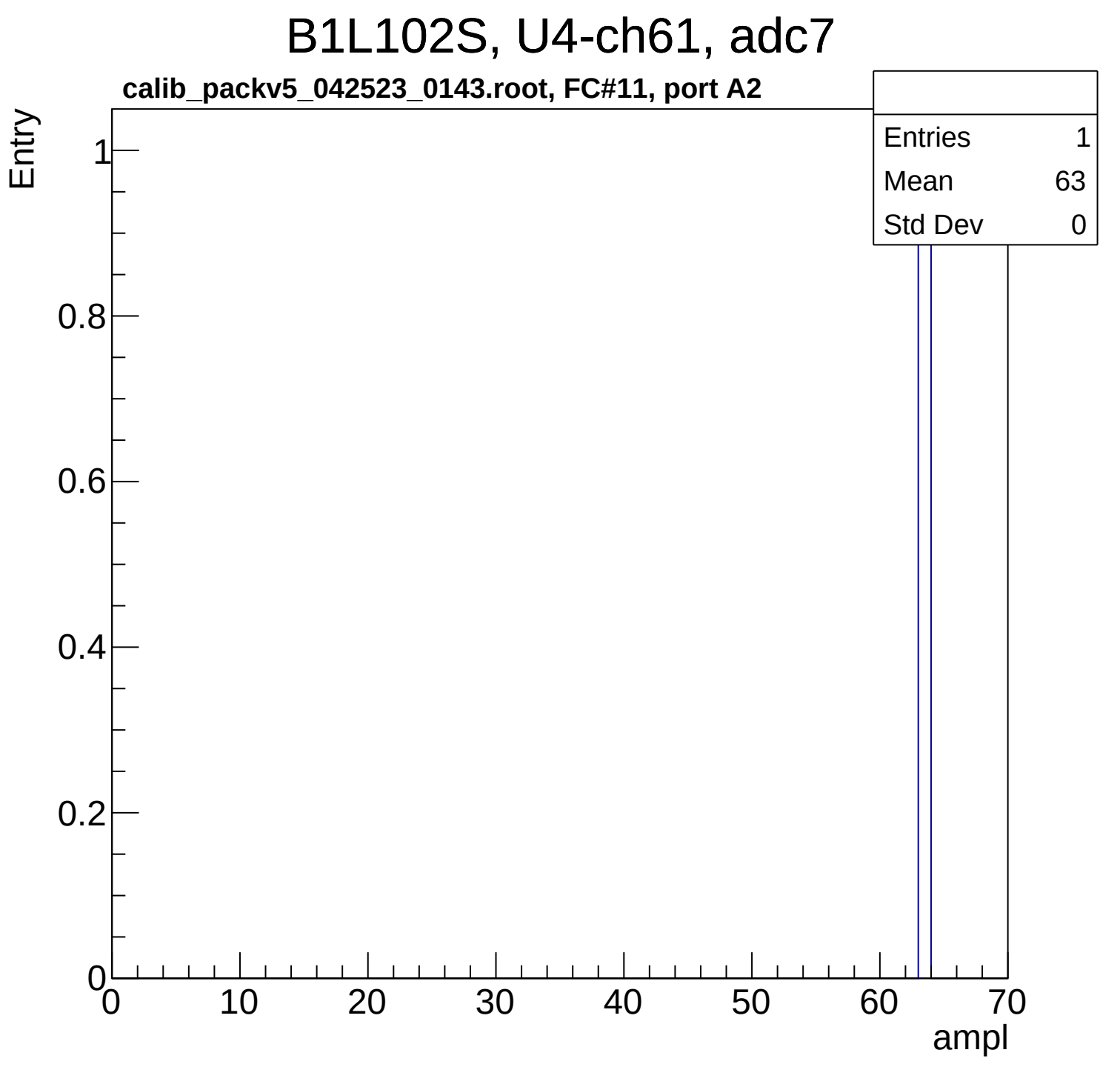
50
60
70
ampl


B1L102S, U4-ch61, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
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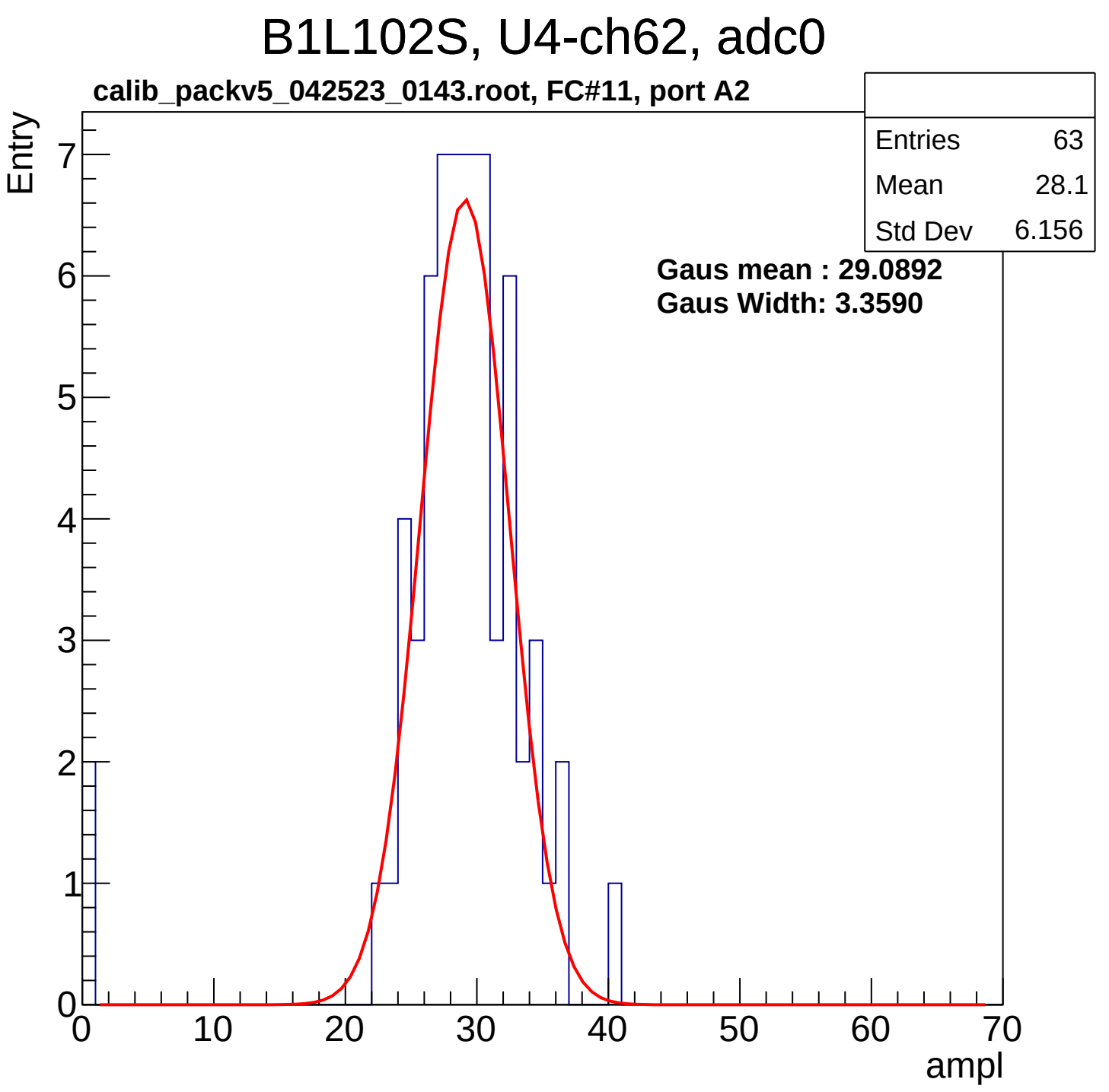
70
ampl


B1L102S, U4-ch62, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 28.1
Std Dev 6.156
Gaus mean : 29.0892
Gaus Width: 3.3590
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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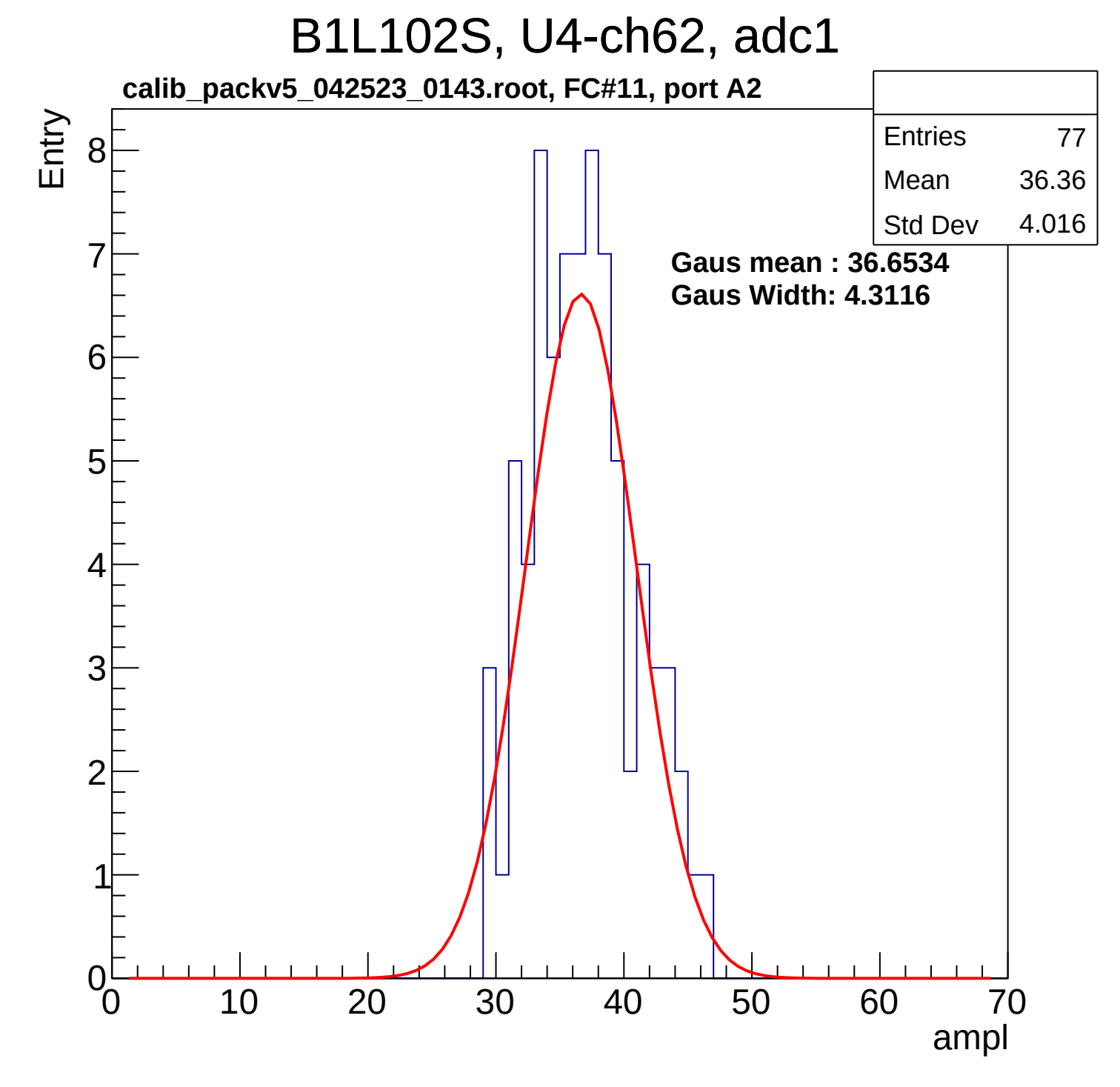
B1L102S, U4-ch62, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 77
Mean 36.36
Std Dev 4.016
Gaus mean : 36.6534
Gaus Width: 4.3116
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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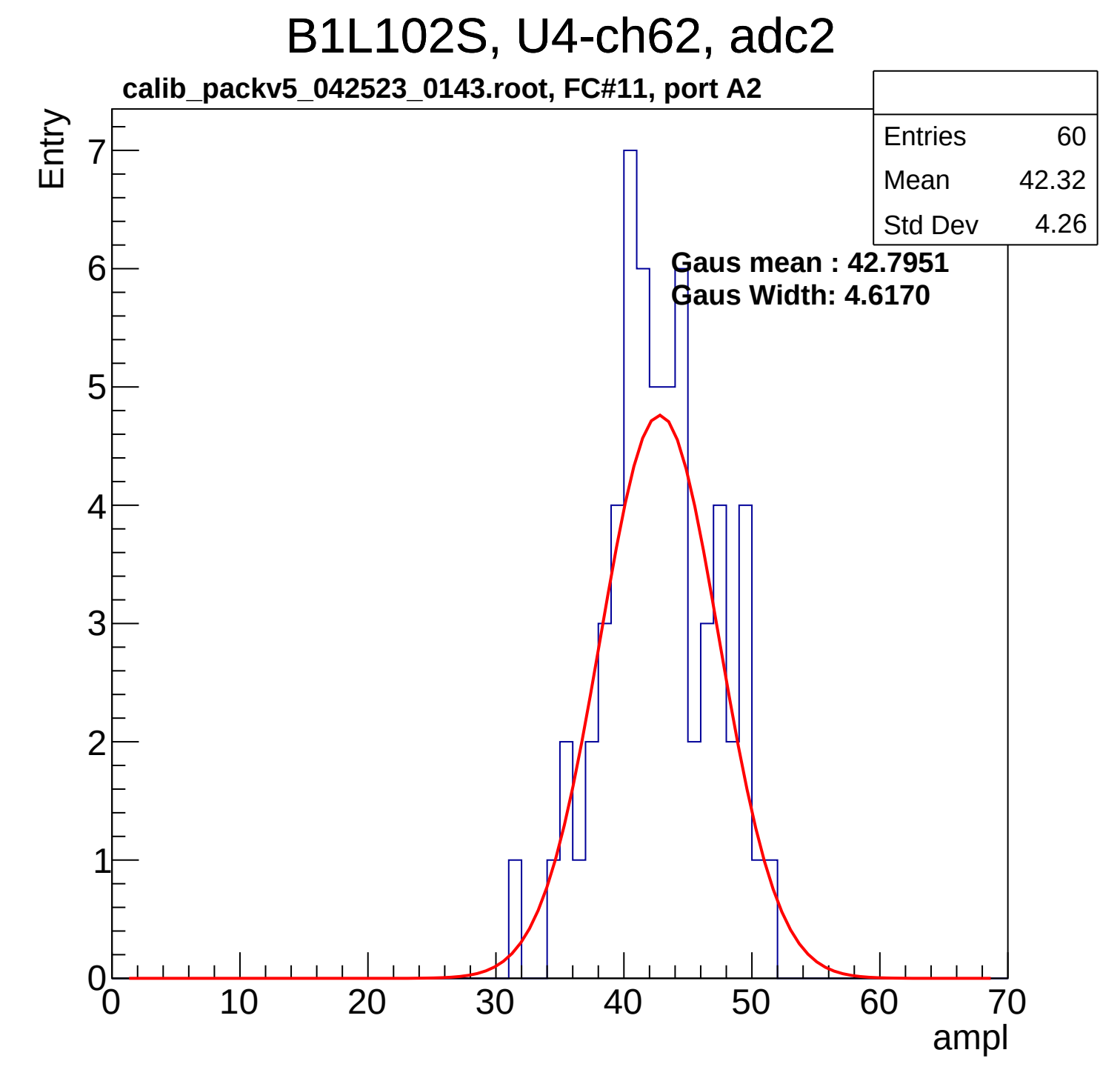
B1L102S, U4-ch62, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 42.32
Std Dev 4.26
Gaus mean : 42.7951
Gaus Width: 4.6170
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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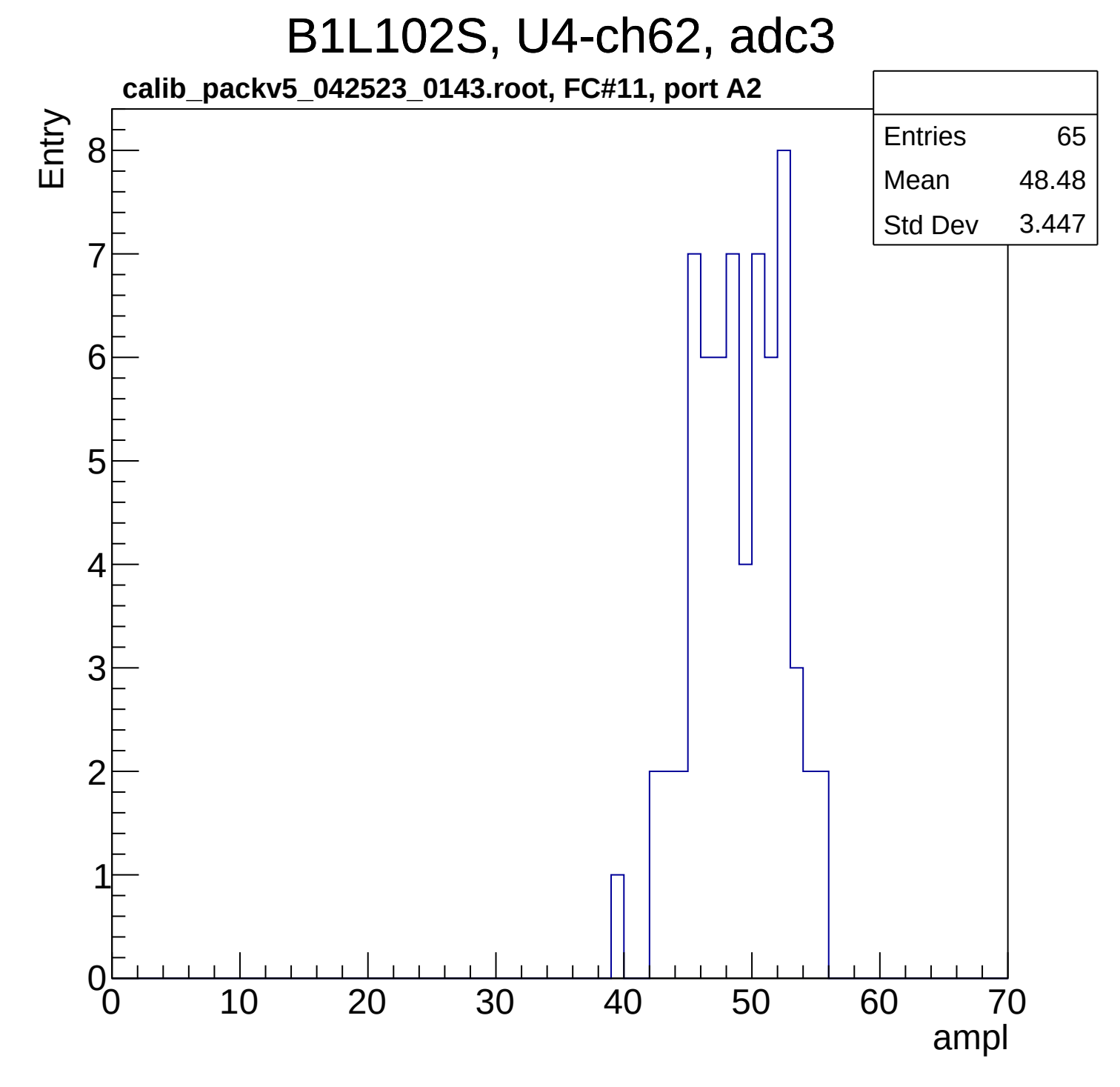
B1L102S, U4-ch62, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 48.48
Std Dev 3.447
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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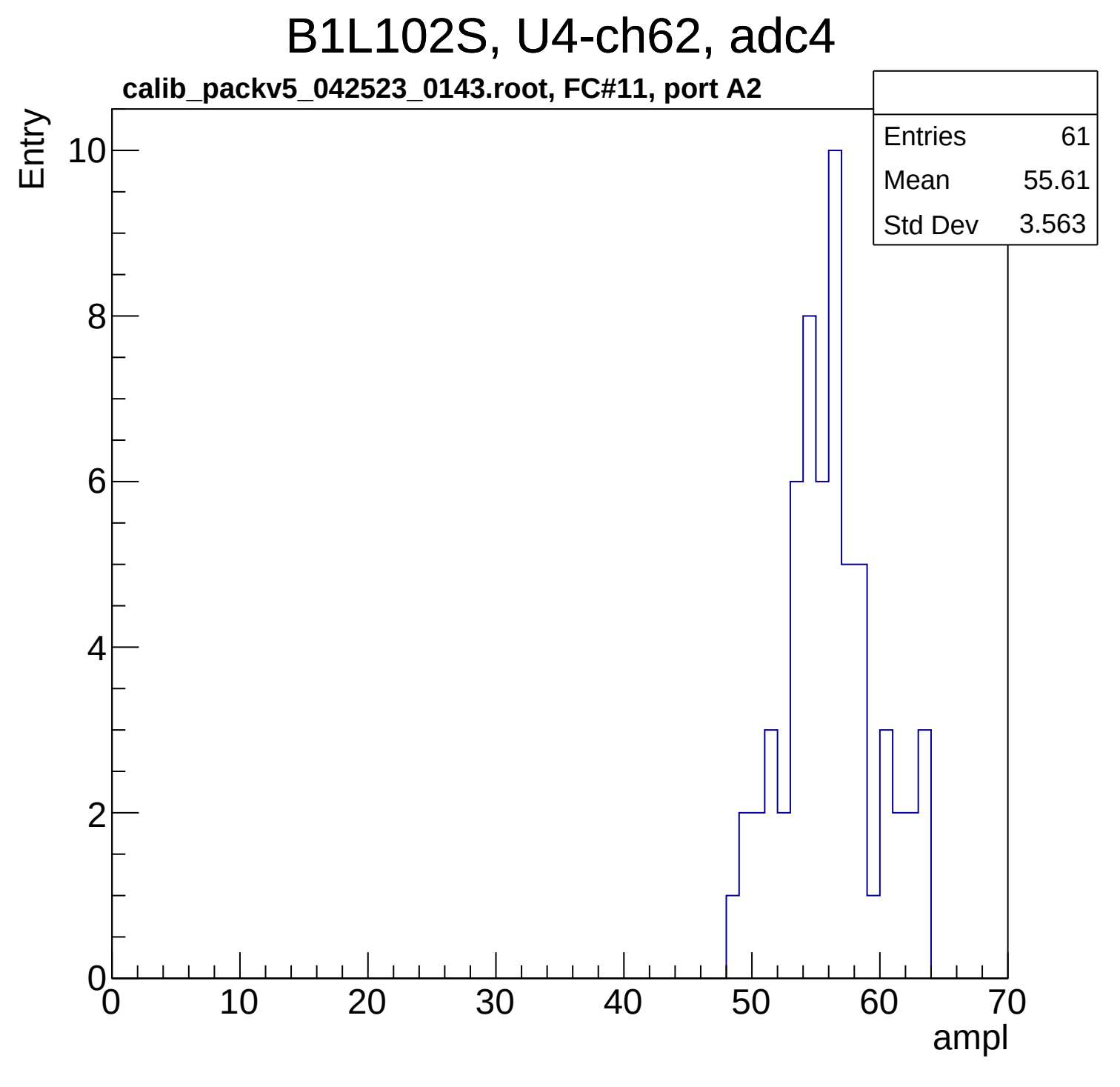
B1L102S, U4-ch62, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 55.61
Std Dev 3.563
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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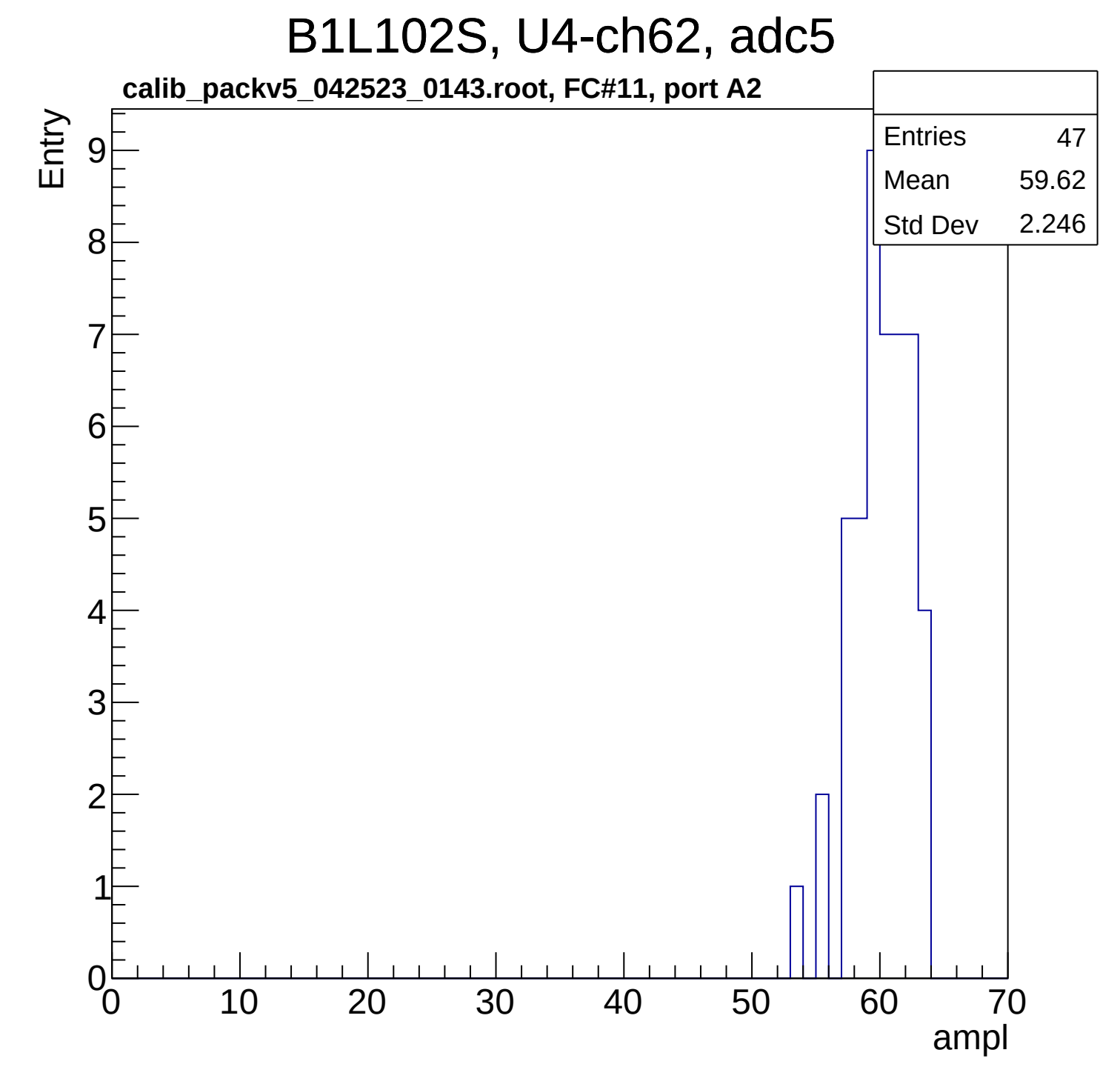
B1L102S, U4-ch62, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 47
Mean 59.62
Std Dev 2.246
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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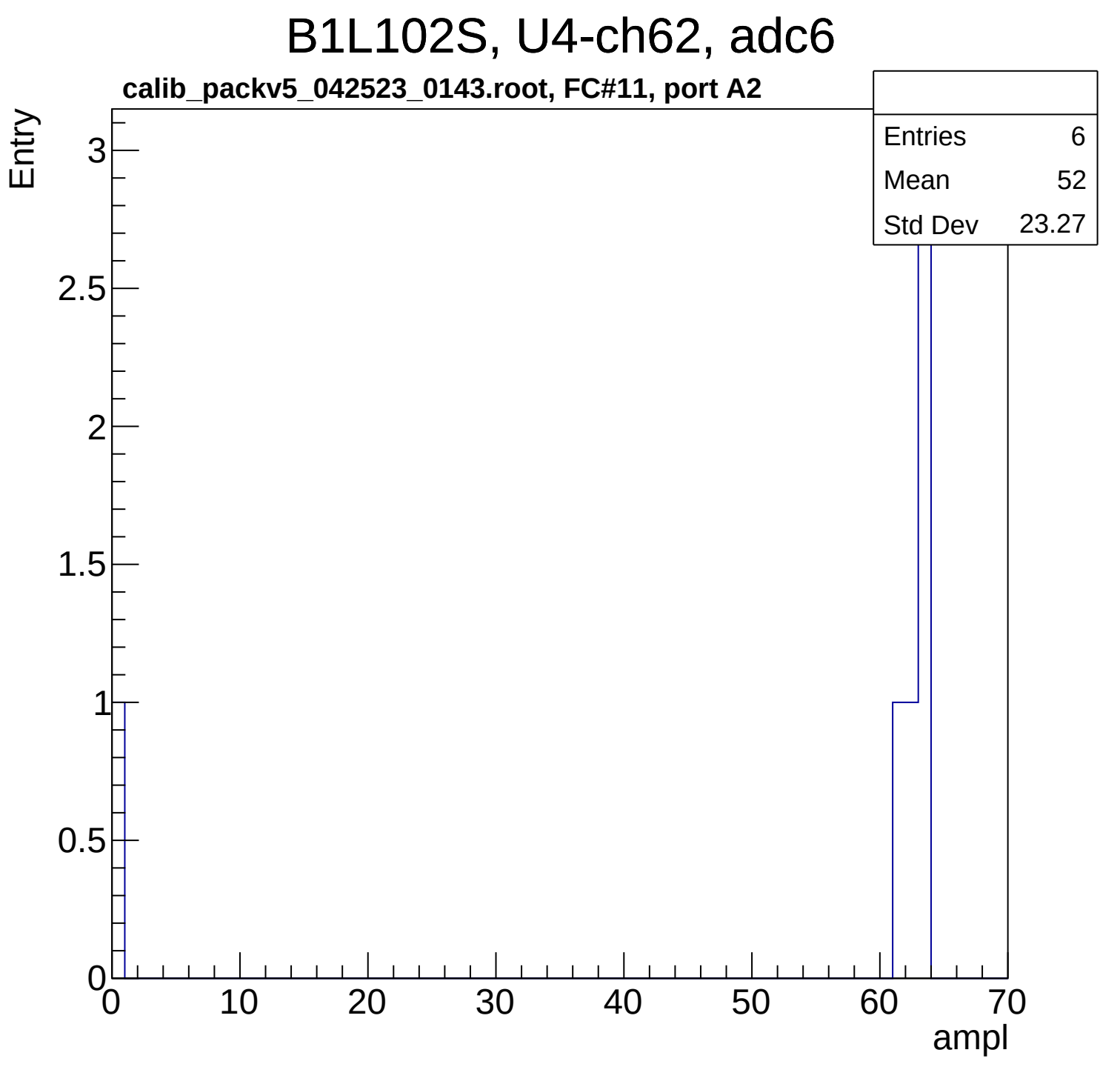
B1L102S, U4-ch62, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 6
Mean 52
Std Dev 23.27
Entry
ampl
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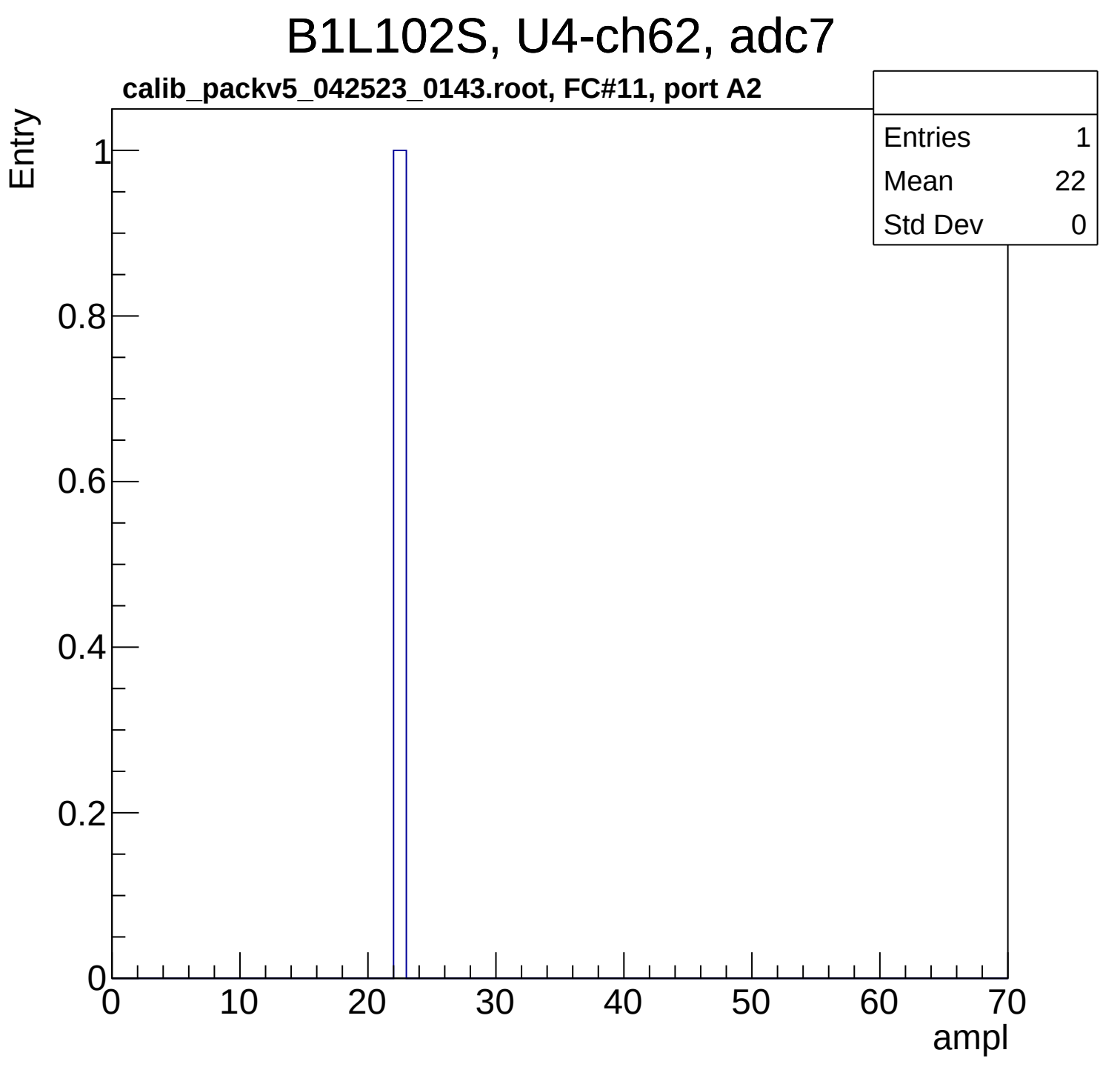
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U4-ch62, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 22
Std Dev 0
Entry
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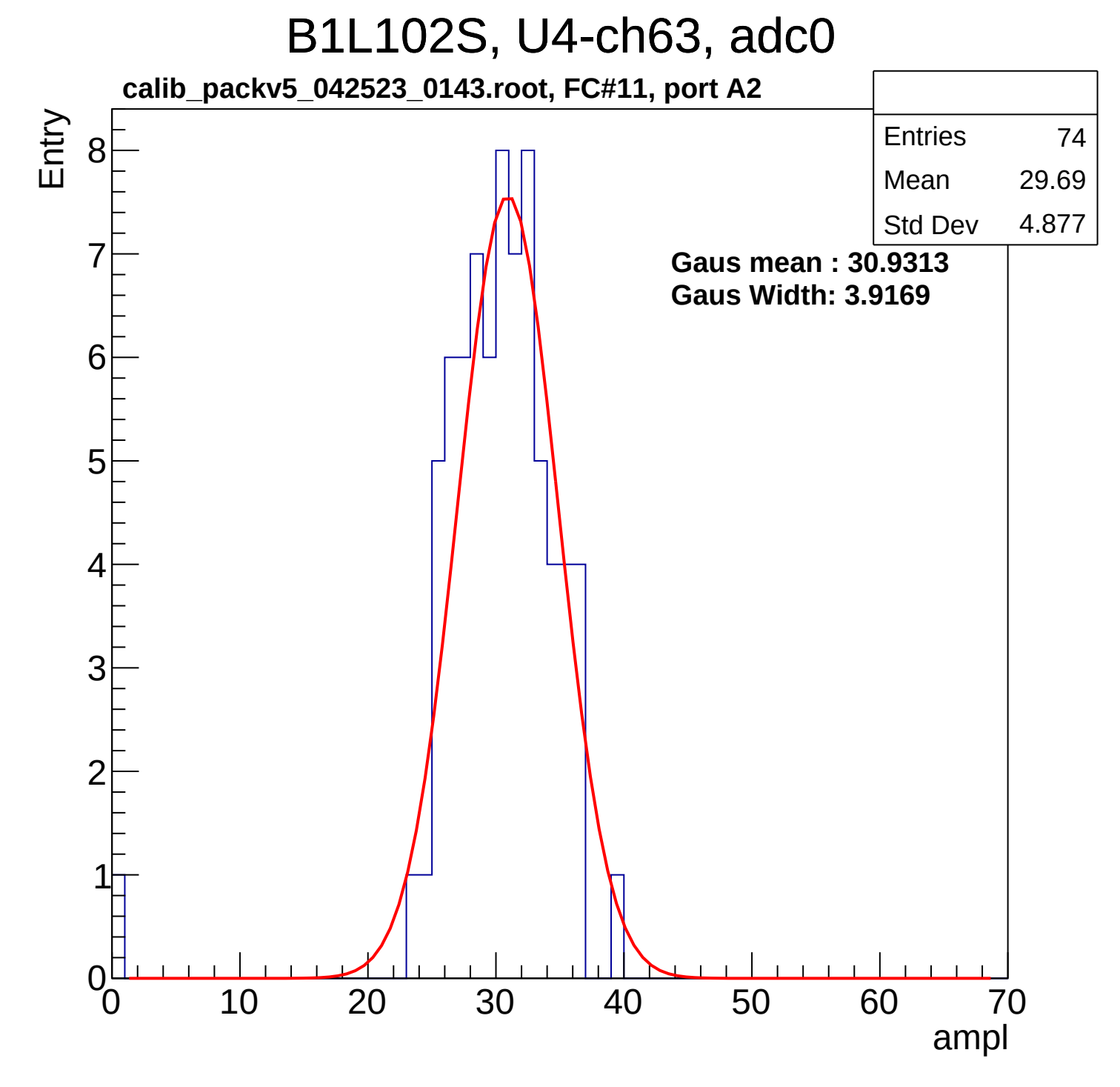
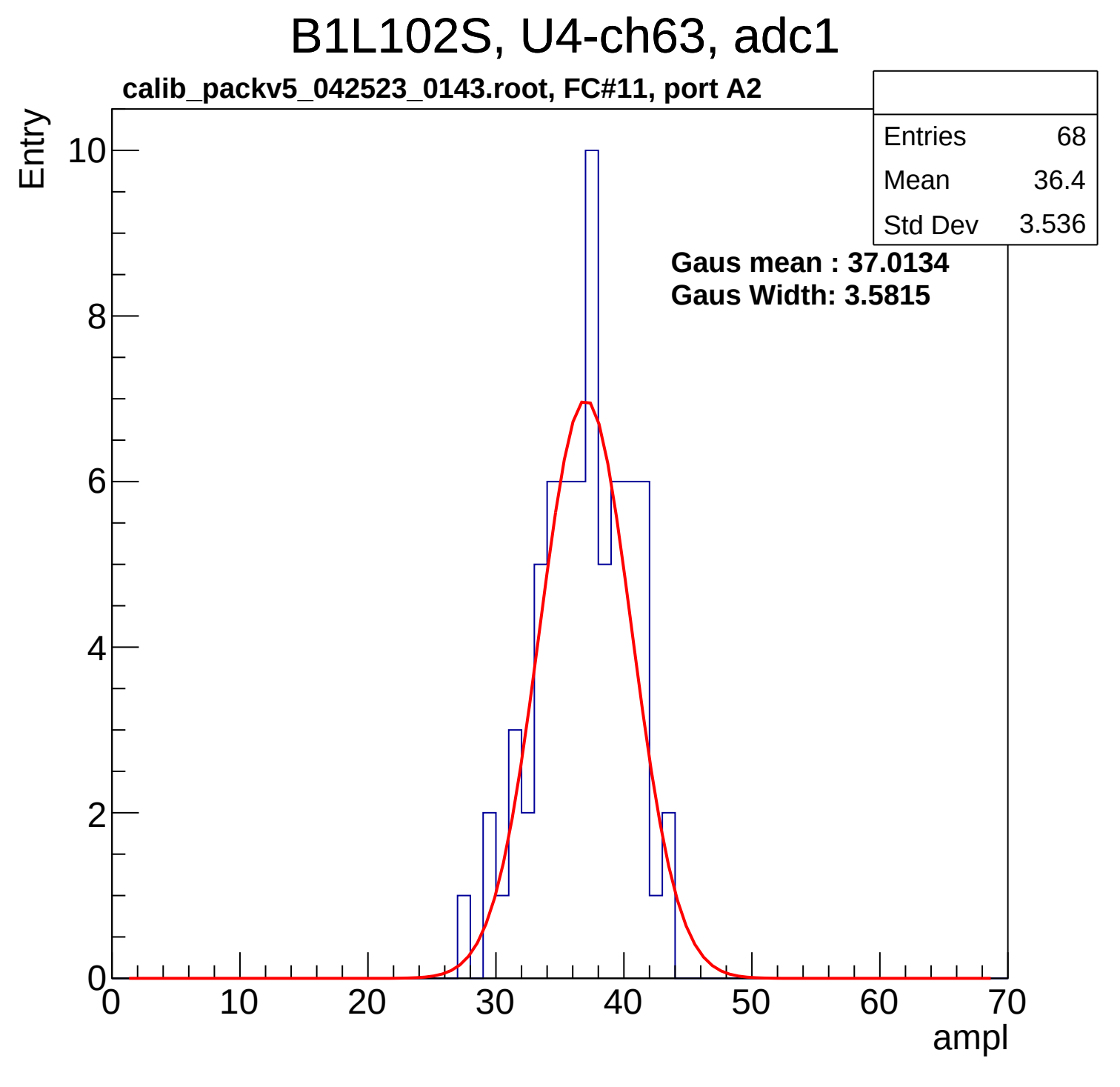
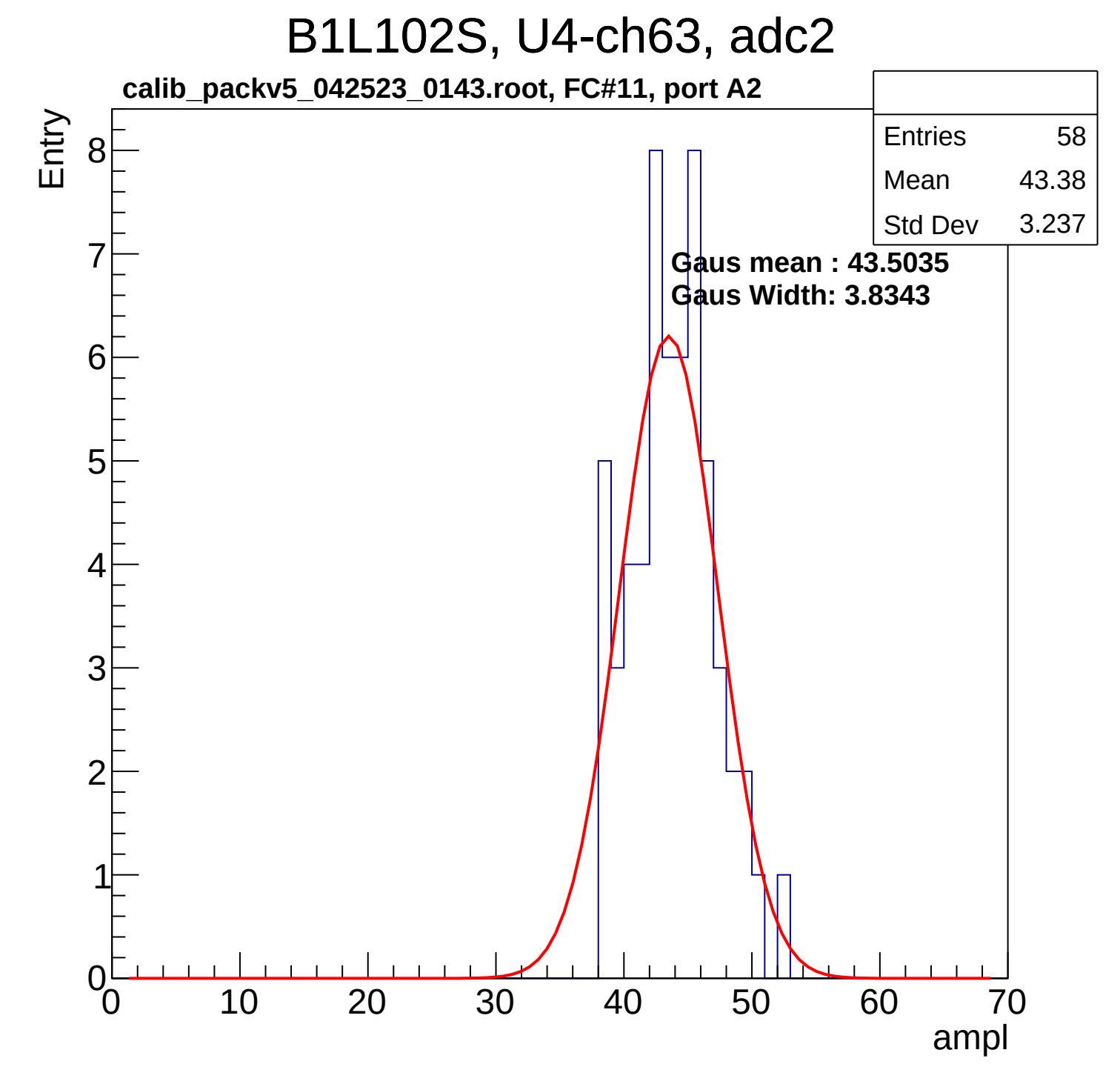
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch63, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 29.69
Std Dev 4.877
Gaus mean : 30.9313
Gaus Width: 3.9169
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch63, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 36.4
Std Dev 3.536
Gaus mean : 37.0134
Gaus Width: 3.5815
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch63, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 43.38
Std Dev 3.237
Gaus mean : 43.5035
Gaus Width: 3.8343
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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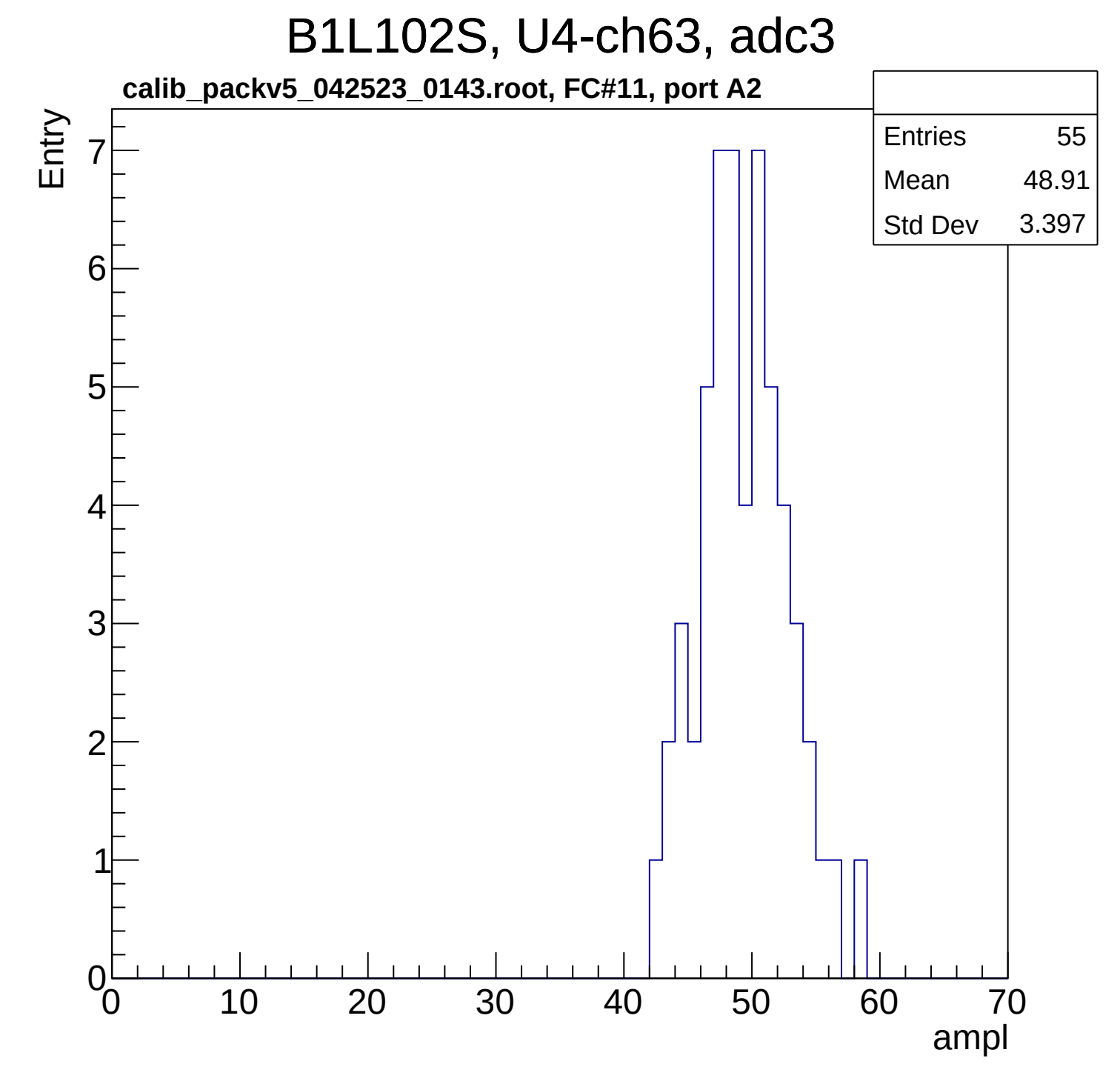
B1L102S, U4-ch63, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 48.91
Std Dev 3.397
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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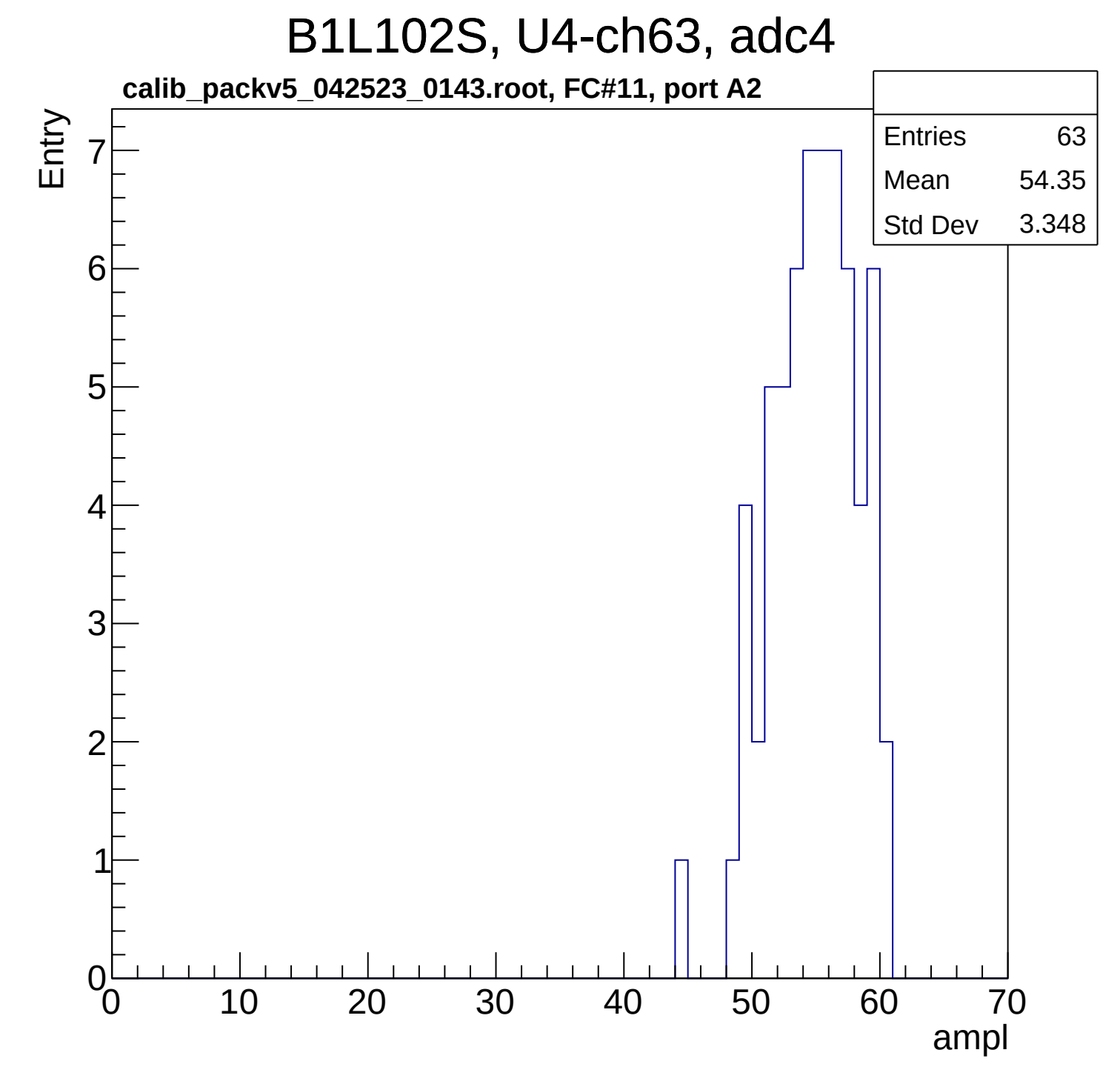
B1L102S, U4-ch63, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 54.35
Std Dev 3.348
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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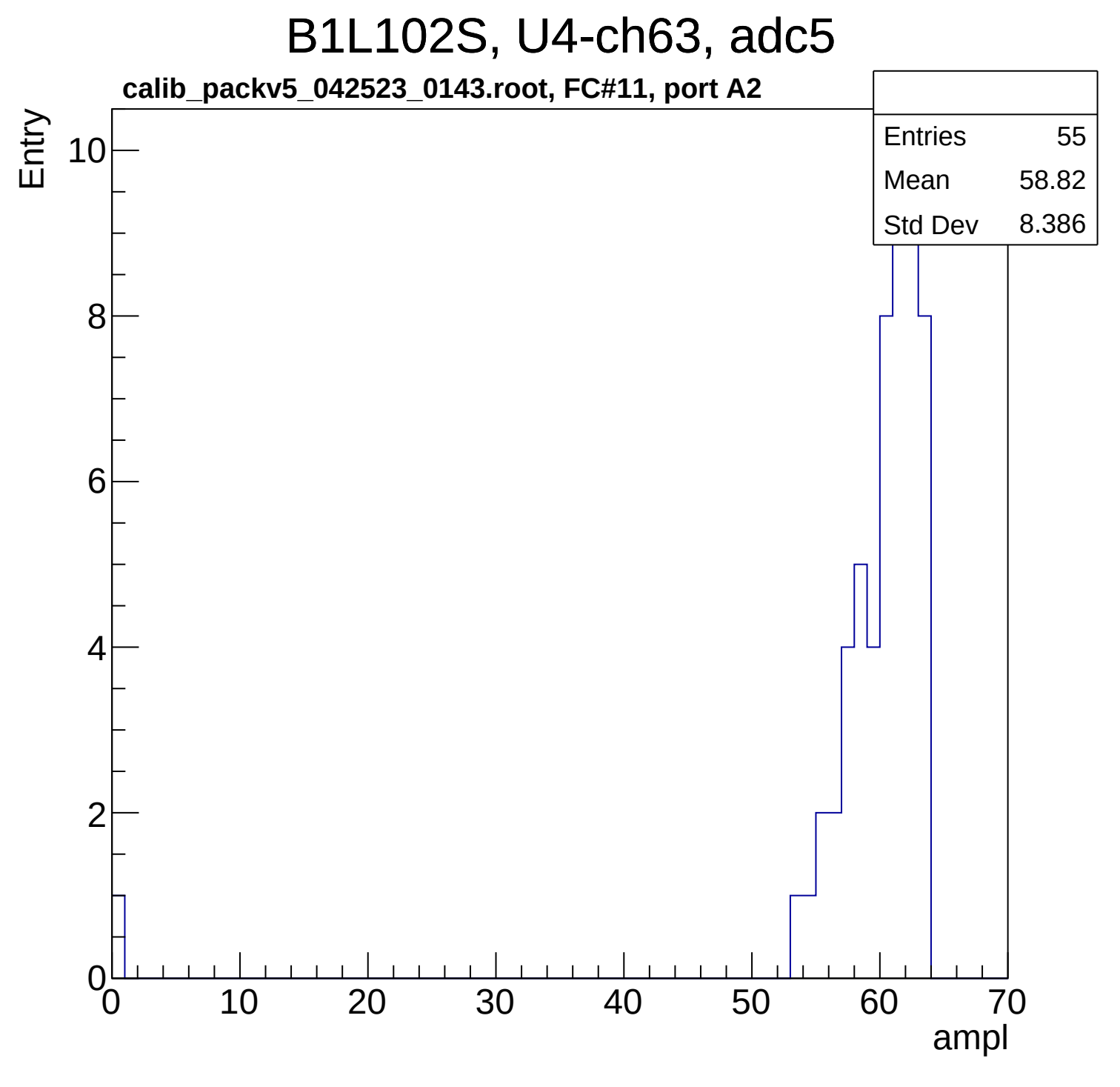
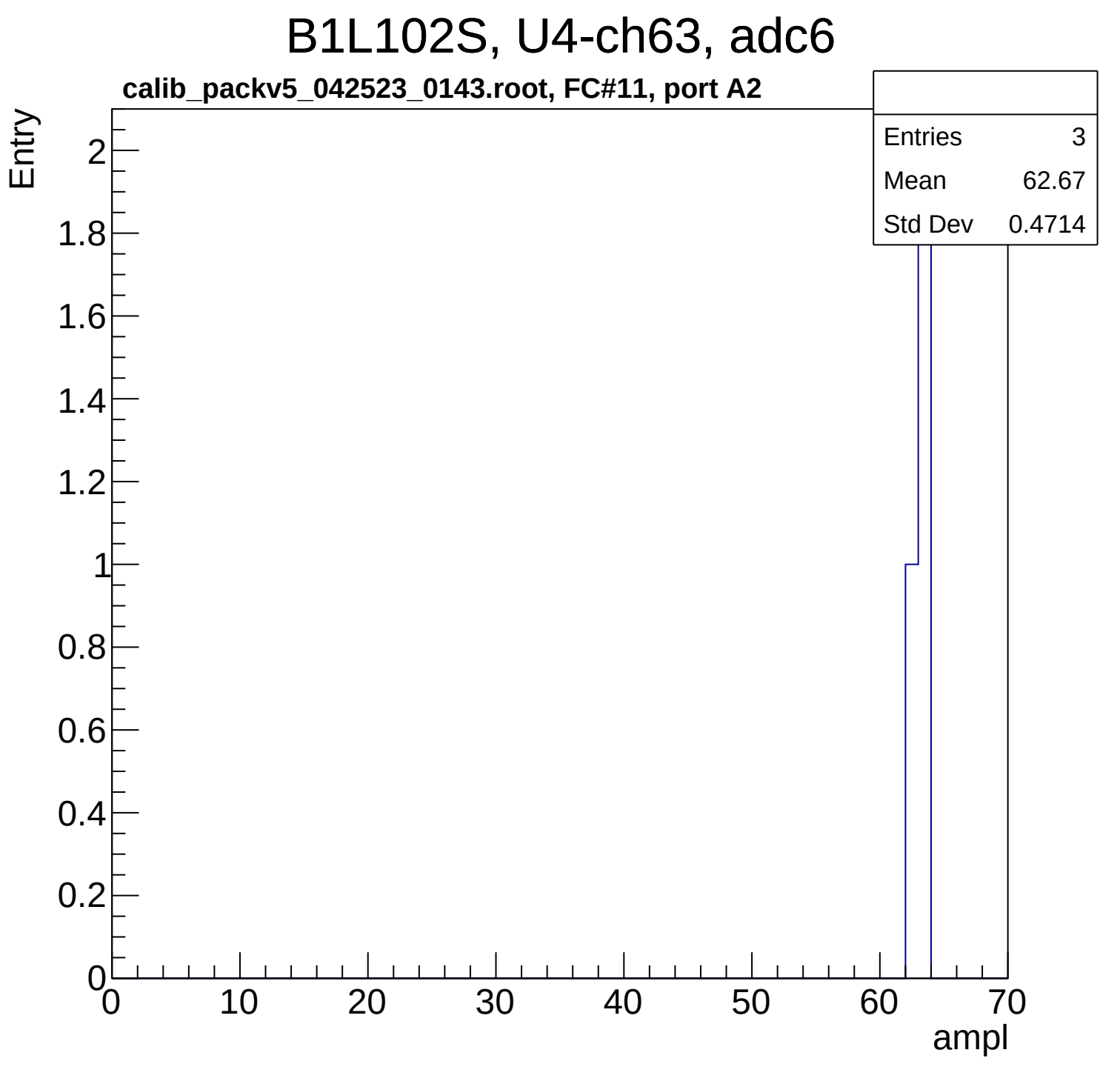
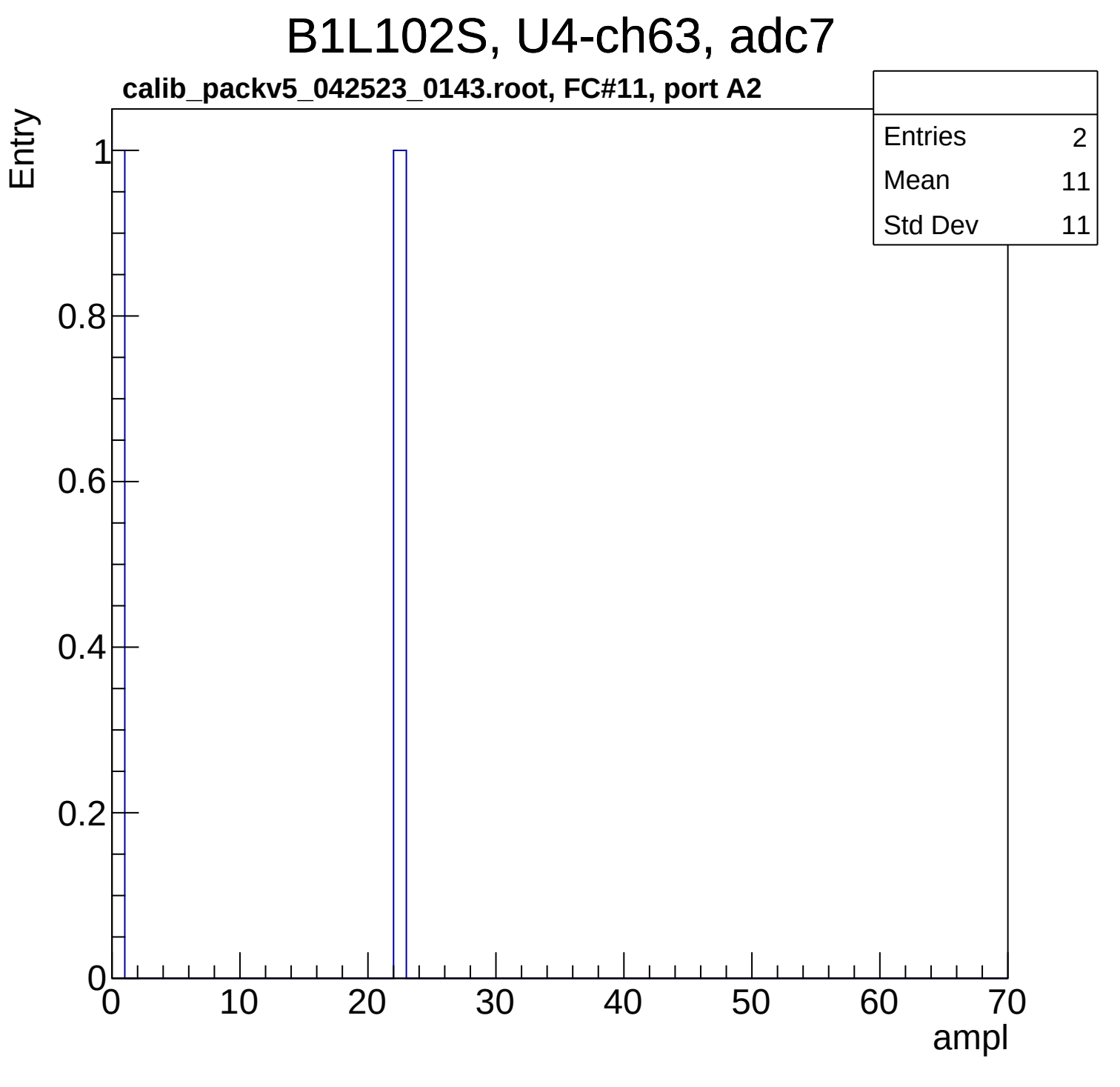

B1L102S, U4-ch63, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 58.82
Std Dev 8.386
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch63, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L102S, U4-ch63, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 11
Std Dev 11
Entry
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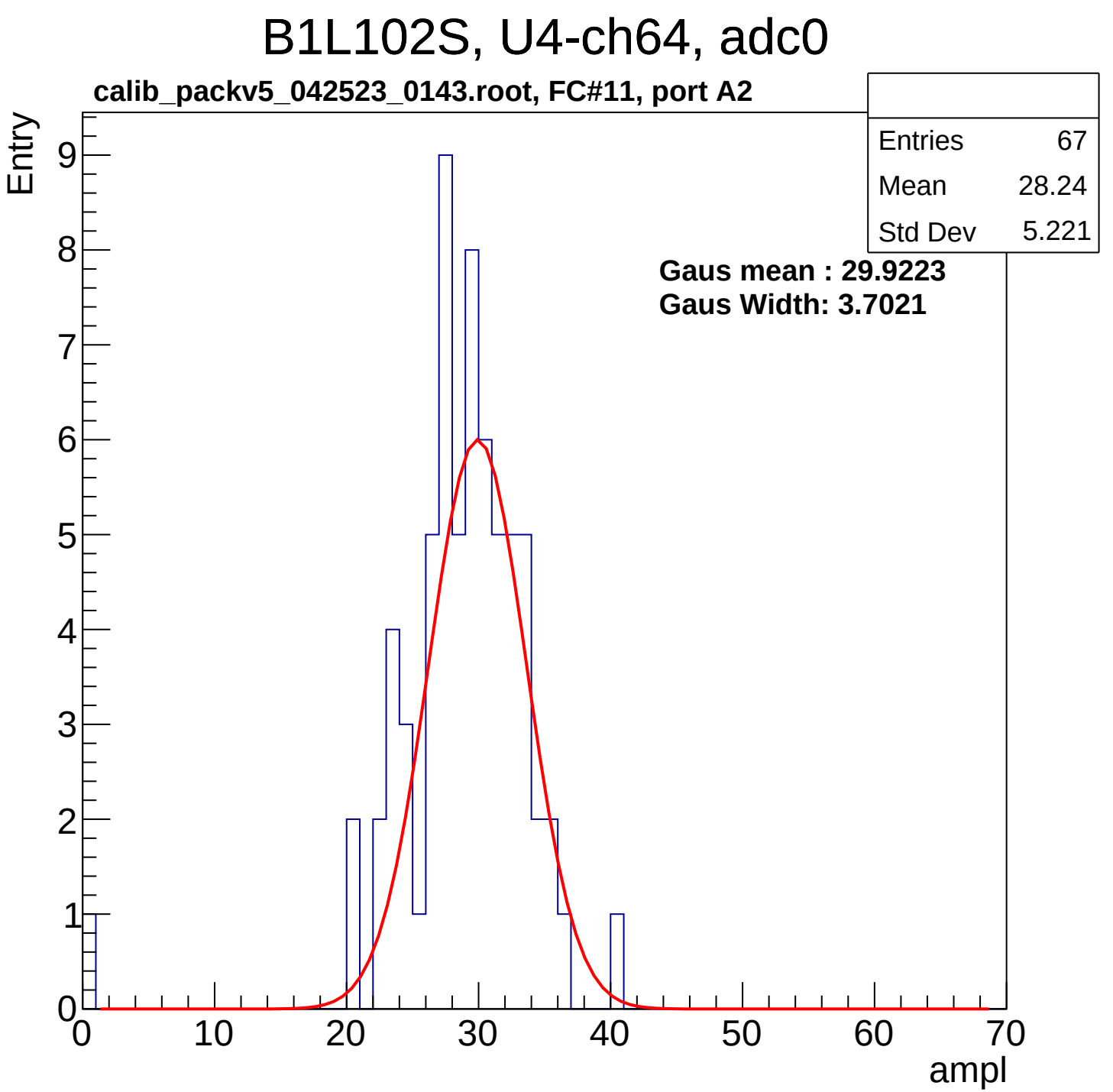
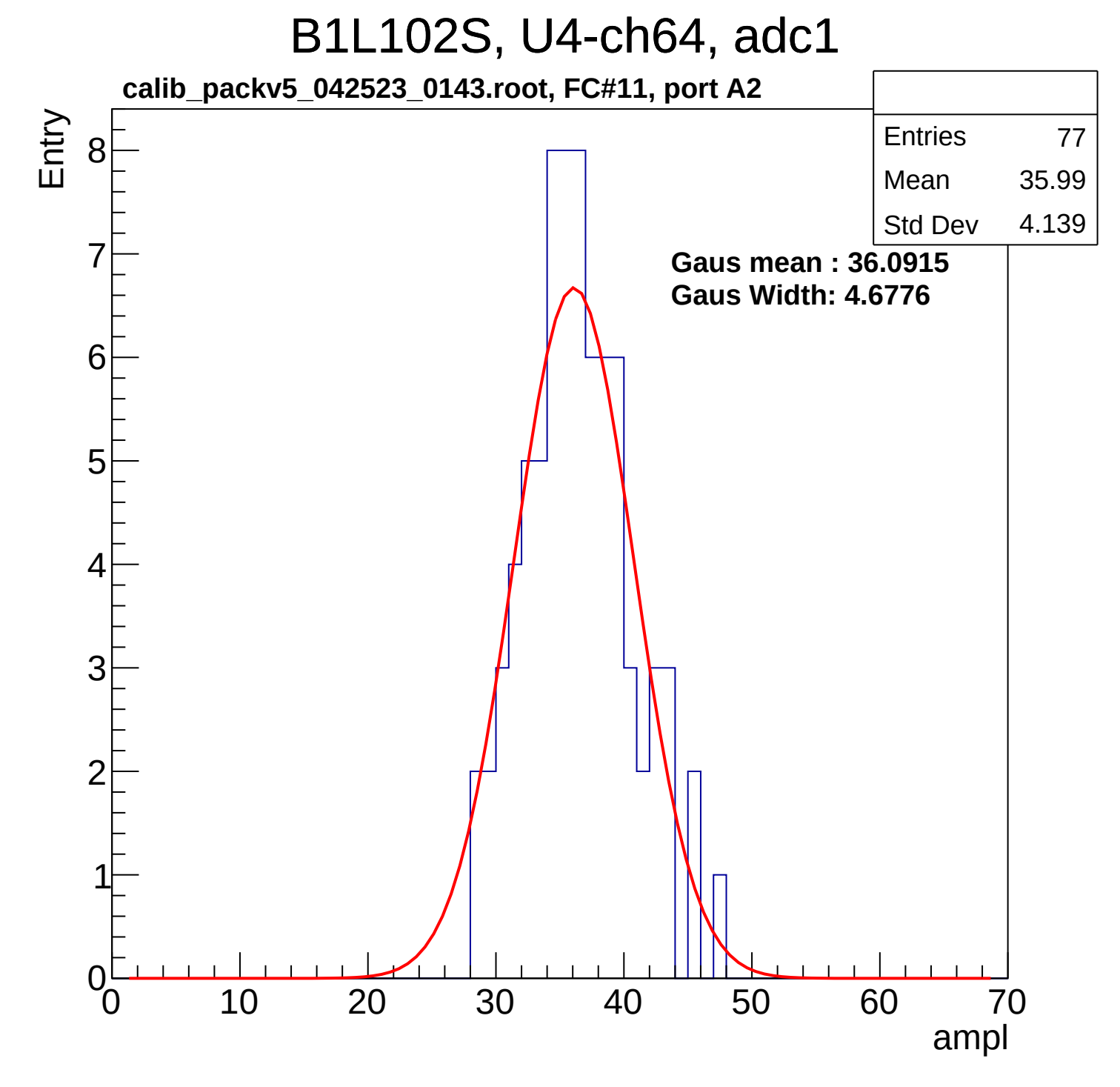
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch64, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 28.24
Std Dev 5.221
Gaus mean : 29.9223
Gaus Width: 3.7021
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch64, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 77
Mean 35.99
Std Dev 4.139
Gaus mean : 36.0915
Gaus Width: 4.6776
Entry
ampl
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1
2
3
4
5
6
7
8
0
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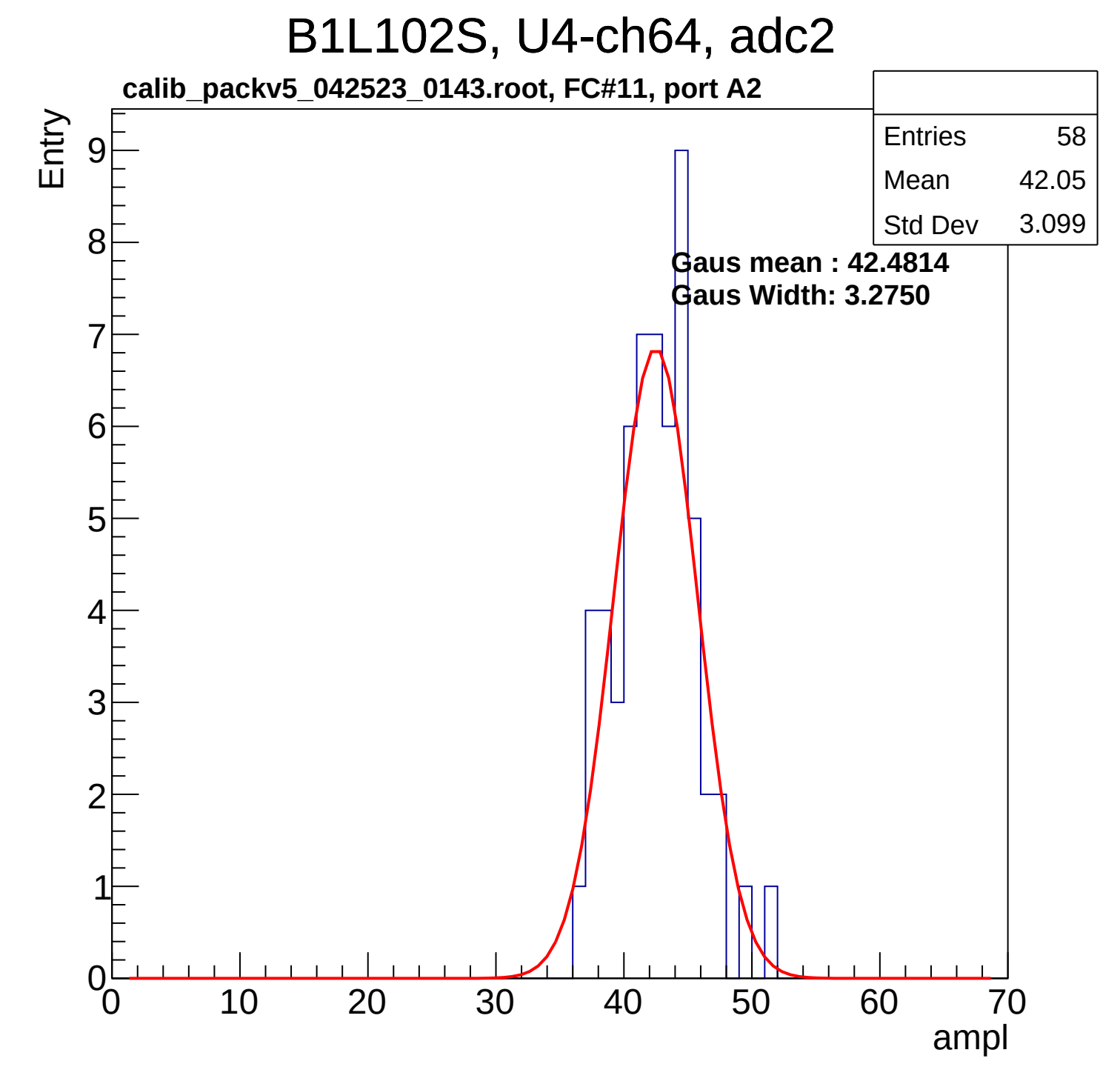
20
30
40
50
60
70


B1L102S, U4-ch64, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 42.05
Std Dev 3.099
Gaus mean : 42.4814
Gaus Width: 3.2750
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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40
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60
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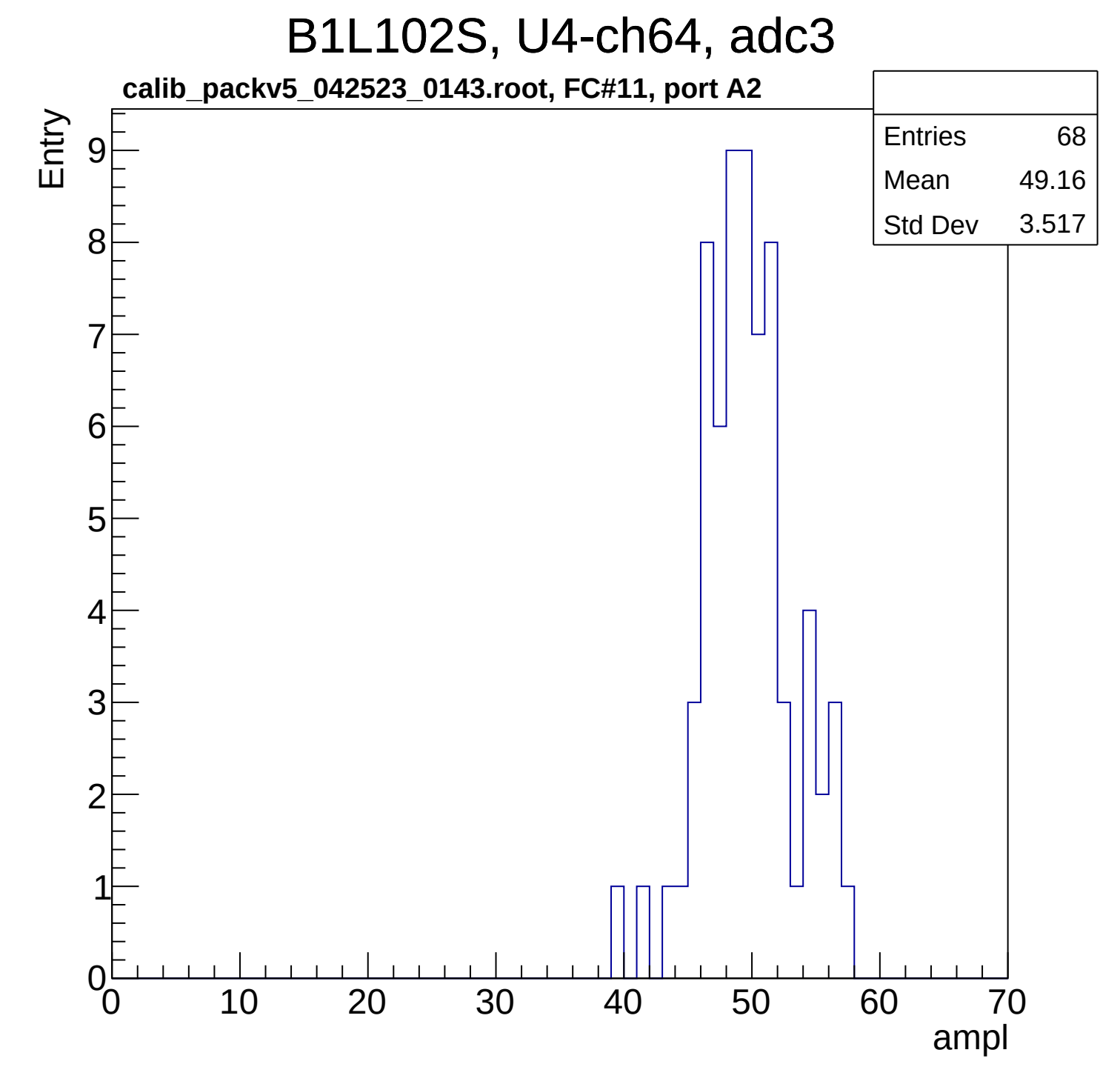
B1L102S, U4-ch64, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 49.16
Std Dev 3.517
Entry
ampl
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4
5
6
7
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0
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60
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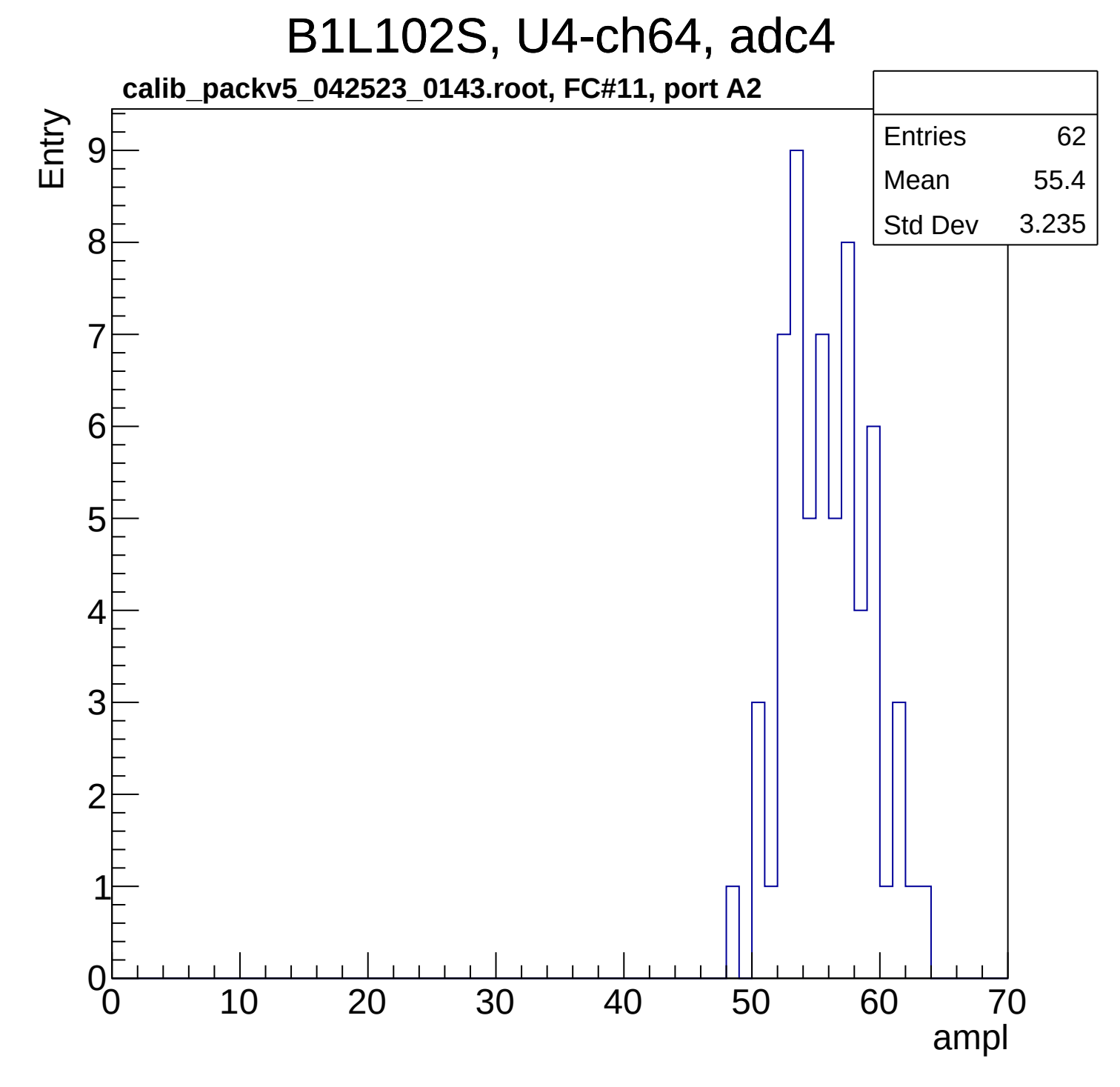
B1L102S, U4-ch64, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 55.4
Std Dev 3.235
Entry
ampl
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3
4
5
6
7
8
9
0
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40
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60
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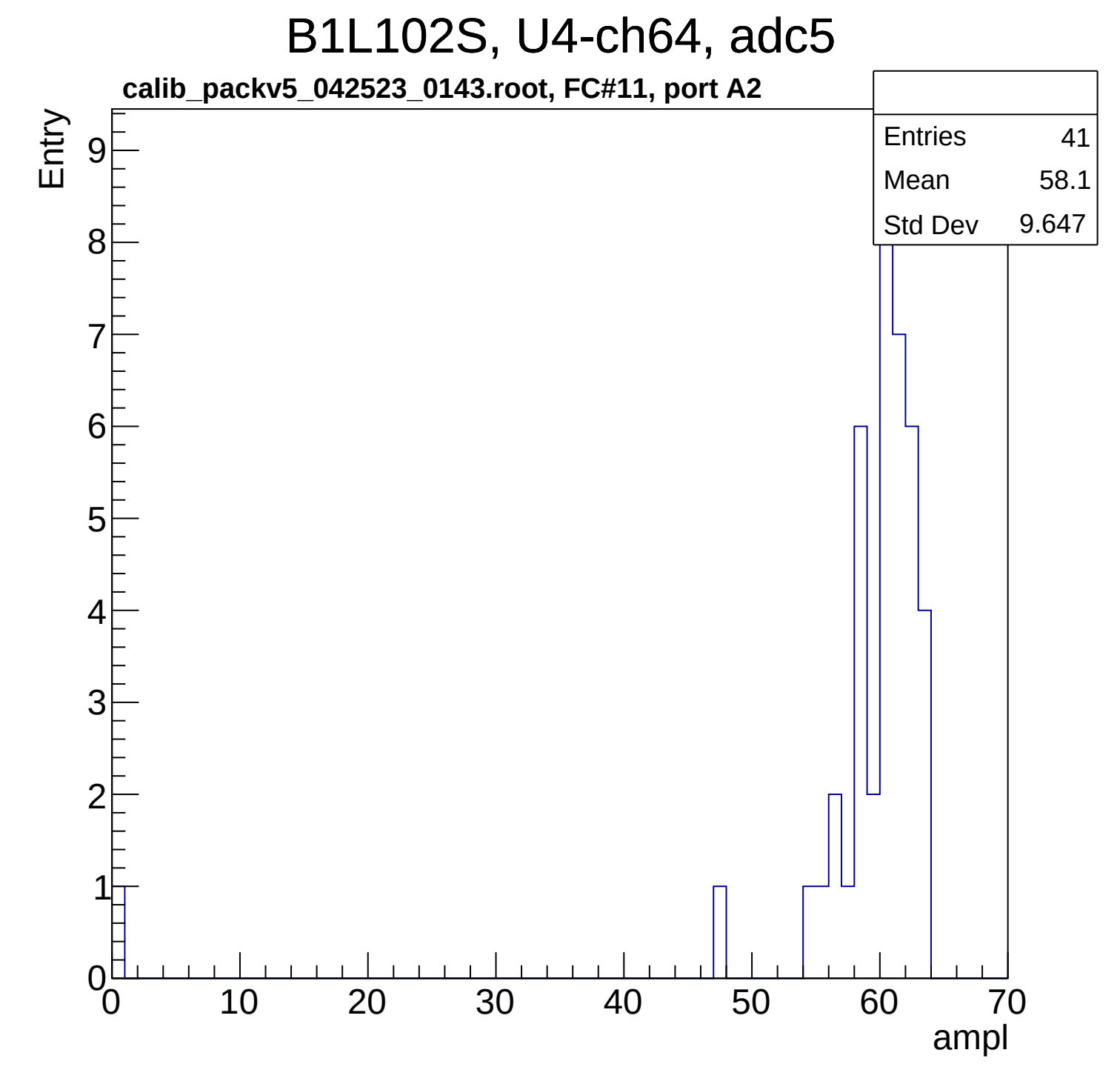
B1L102S, U4-ch64, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 41
Mean 58.1
Std Dev 9.647
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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60
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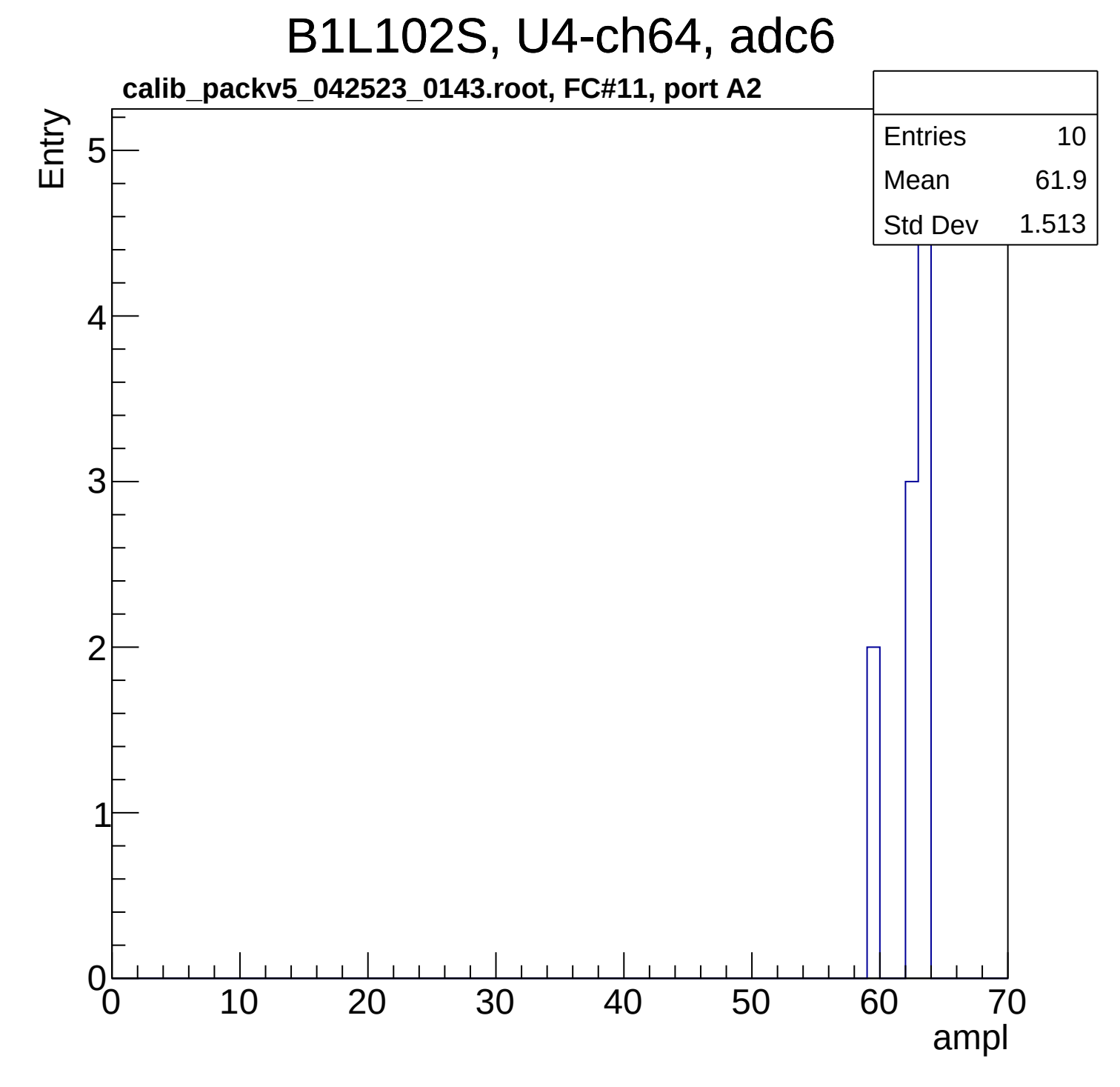
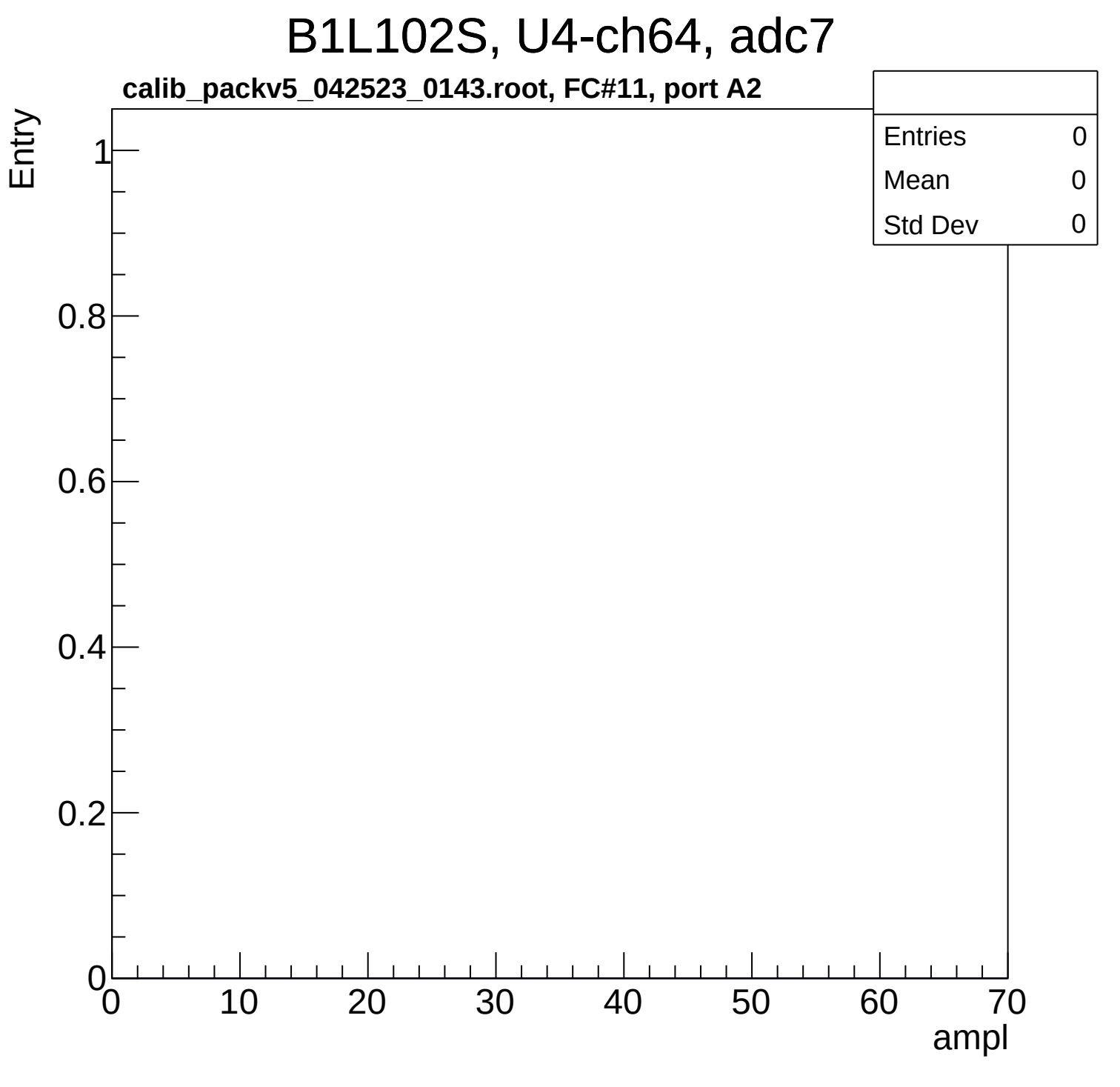

B1L102S, U4-ch64, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 10
Mean 61.9
Std Dev 1.513
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L102S, U4-ch64, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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0.6
0.4
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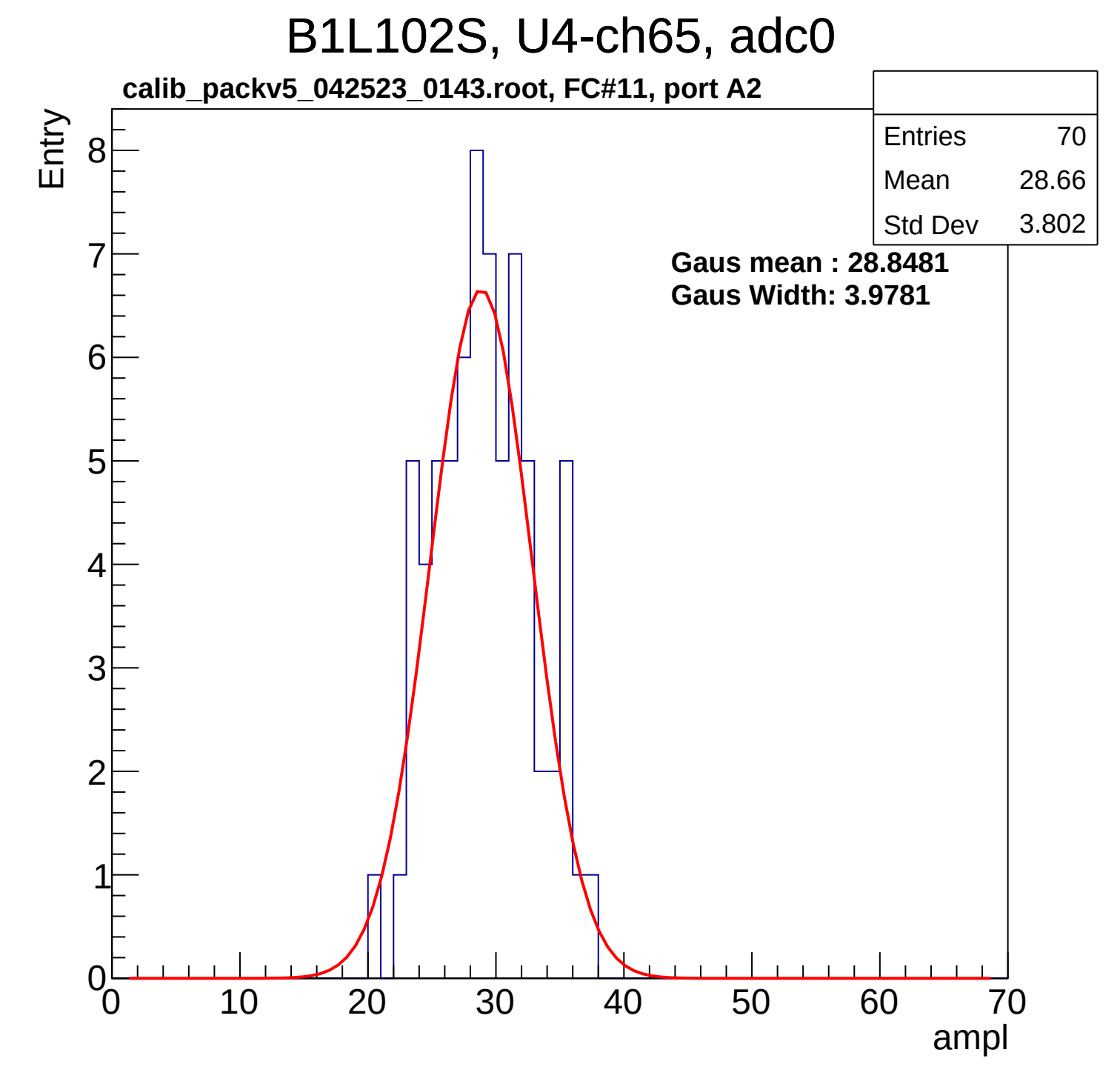
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch65, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 28.66
Std Dev 3.802
Gaus mean : 28.8481
Gaus Width: 3.9781
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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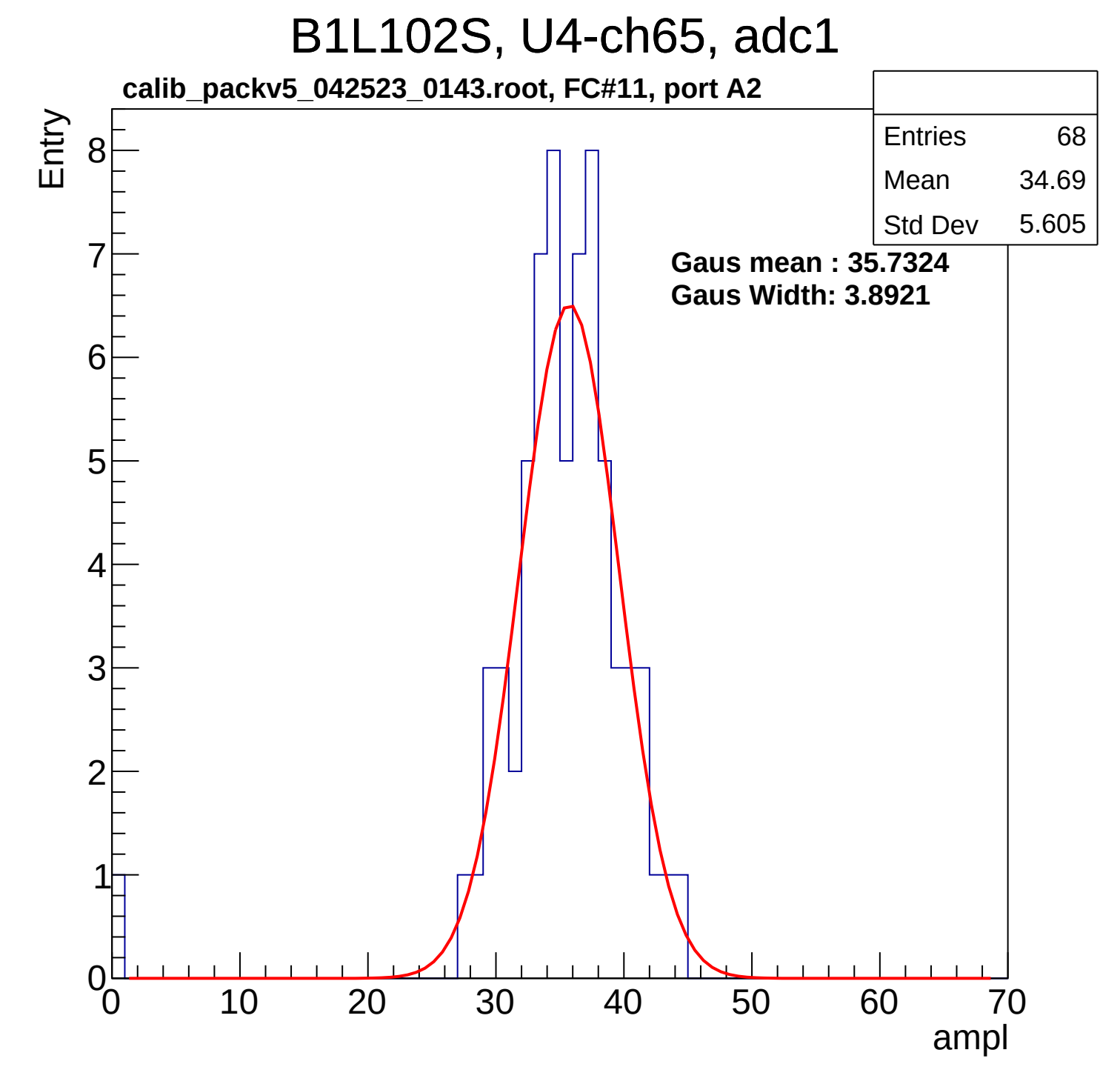
40
50
60
70


B1L102S, U4-ch65, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 34.69
Std Dev 5.605
Gaus mean : 35.7324
Gaus Width: 3.8921
Entry
ampl
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2
3
4
5
6
7
8
0
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40
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60
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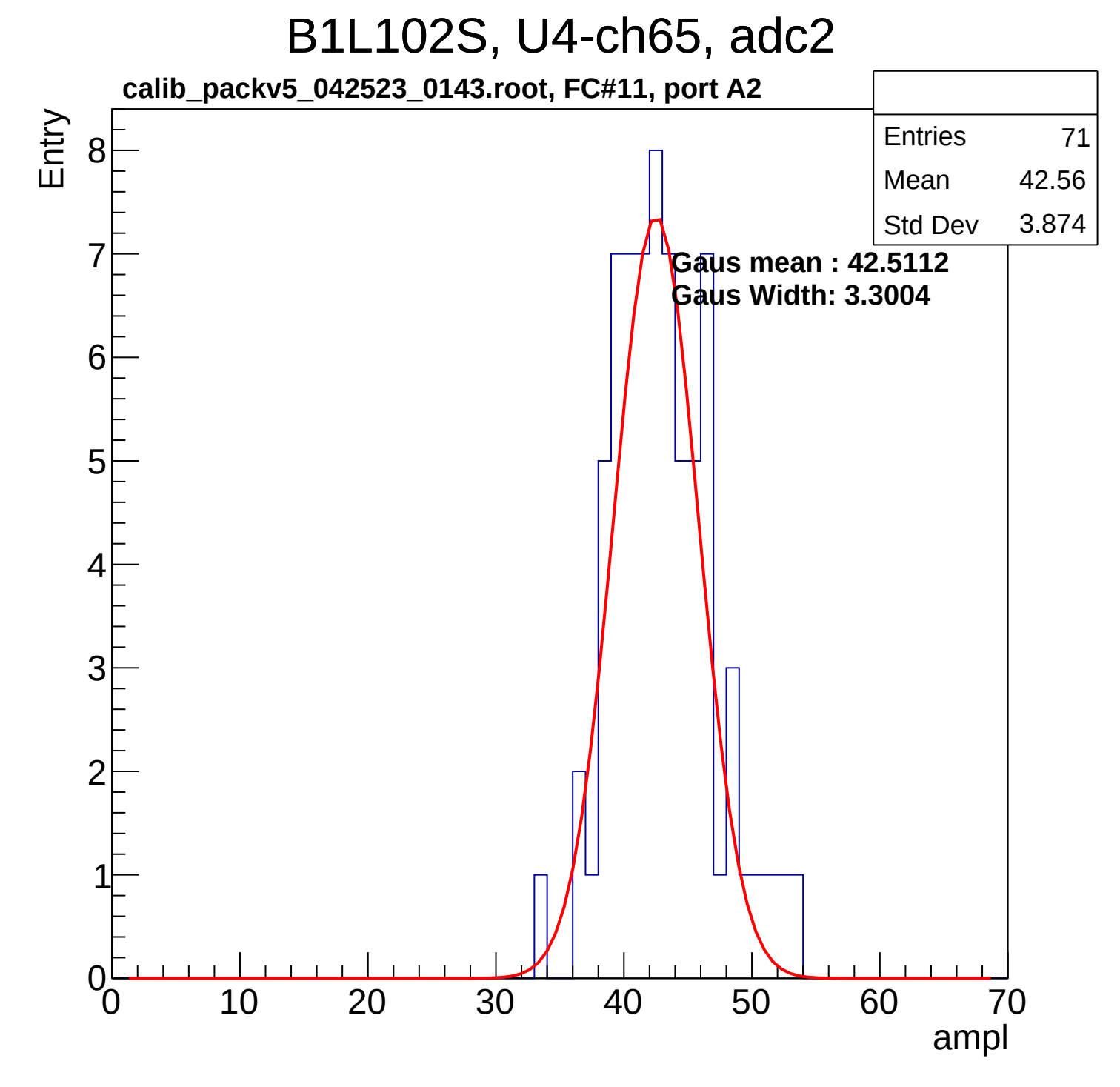
B1L102S, U4-ch65, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 42.56
Std Dev 3.874
Gaus mean : 42.5112
Gaus Width: 3.3004
Entry
ampl
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1
2
3
4
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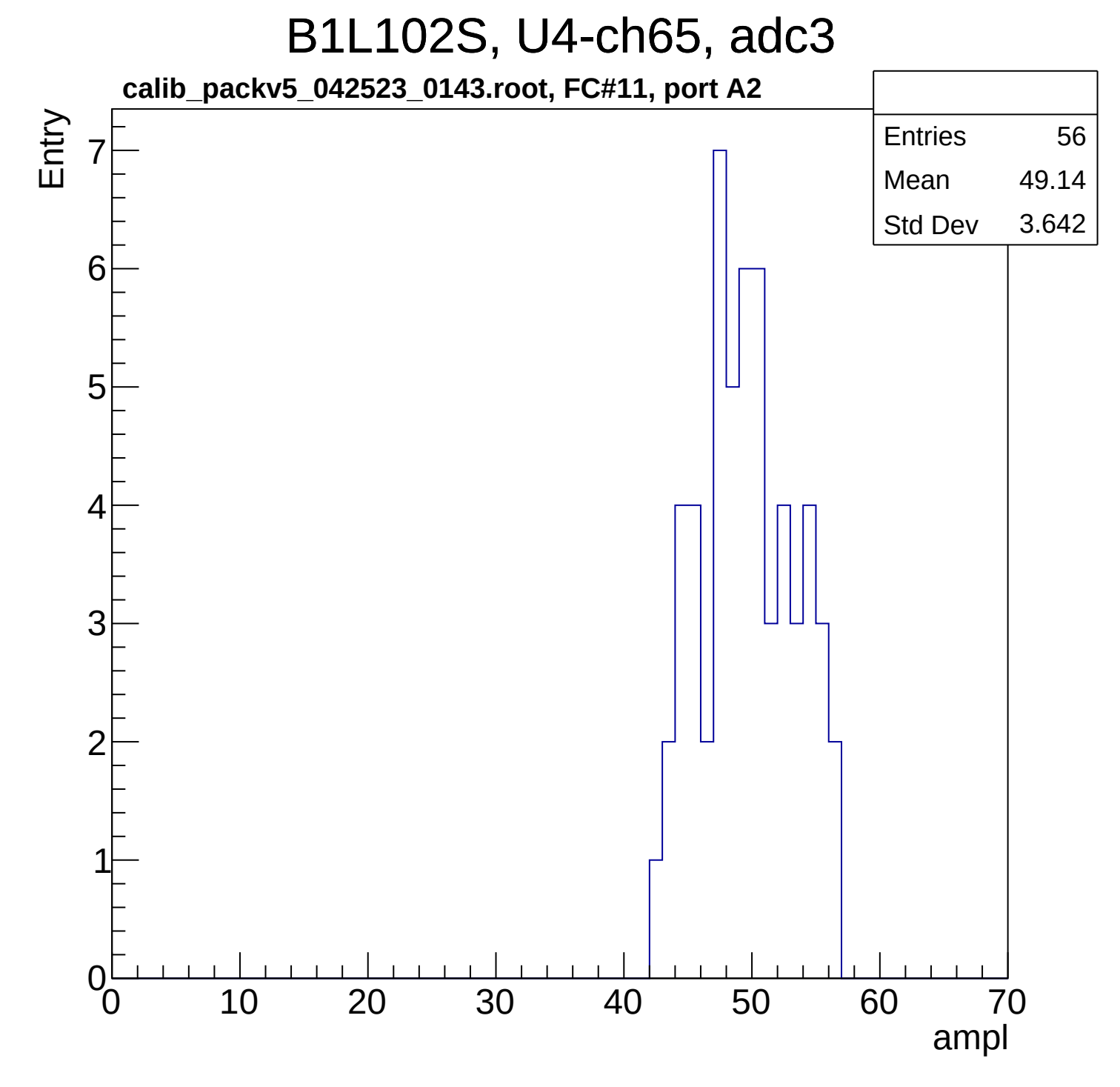
B1L102S, U4-ch65, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 49.14
Std Dev 3.642
Entry
ampl
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3
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5
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10
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40
50
60
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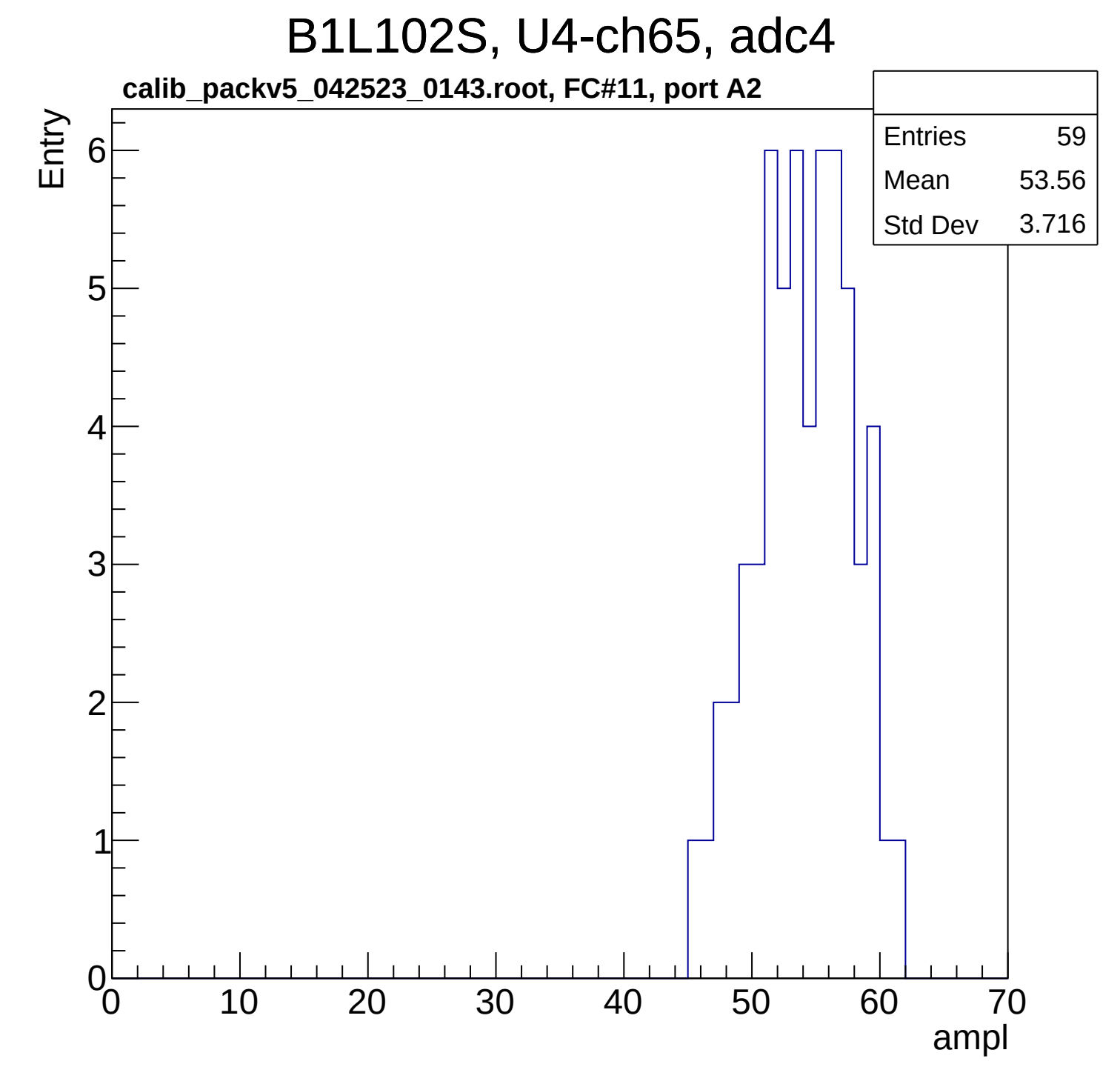
B1L102S, U4-ch65, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 53.56
Std Dev 3.716
Entry
ampl
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1
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3
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6
0
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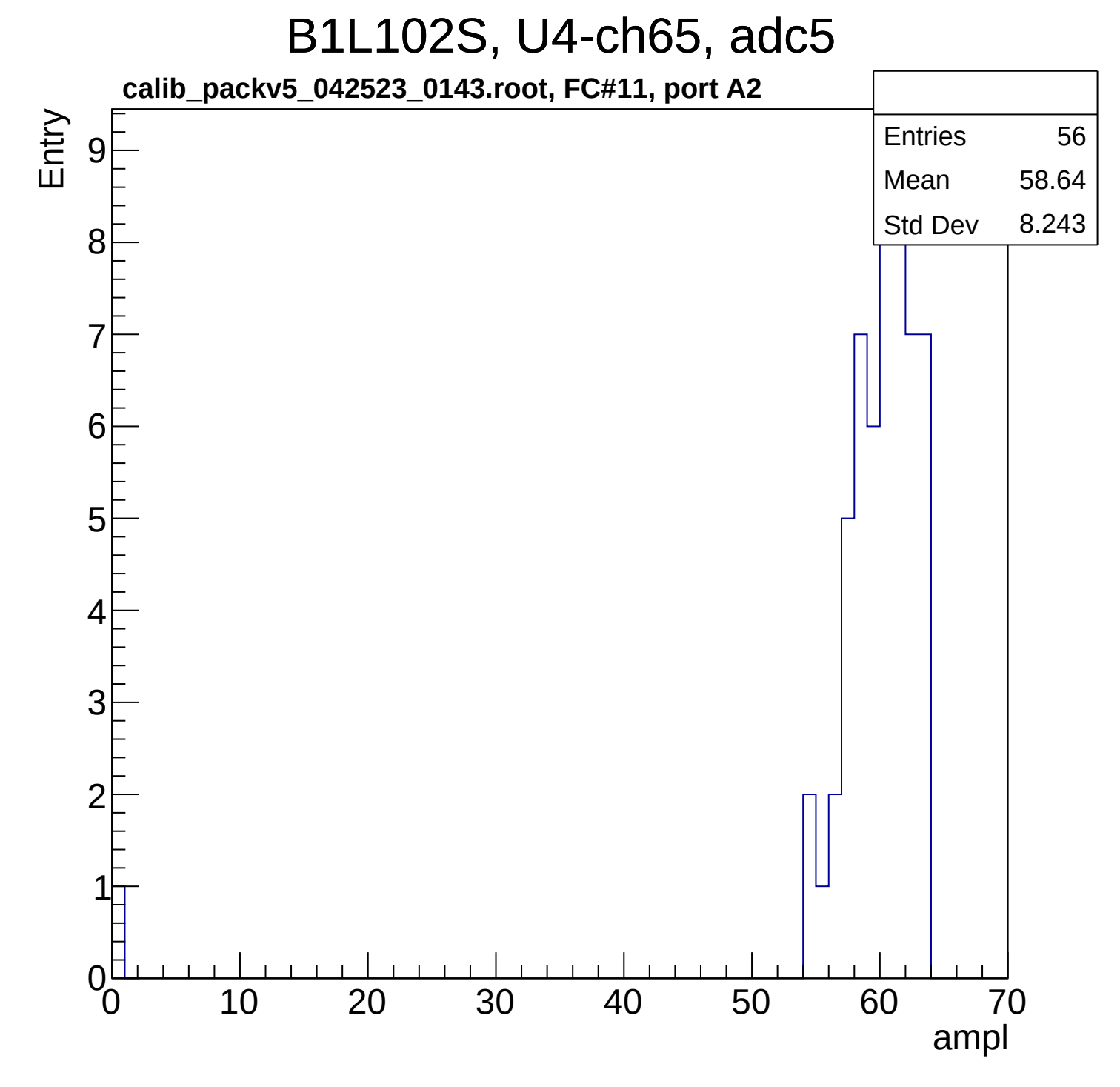
30
40
50
60
70


B1L102S, U4-ch65, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 58.64
Std Dev 8.243
Entry
ampl
0
1
2
3
4
5
6
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9
0
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60
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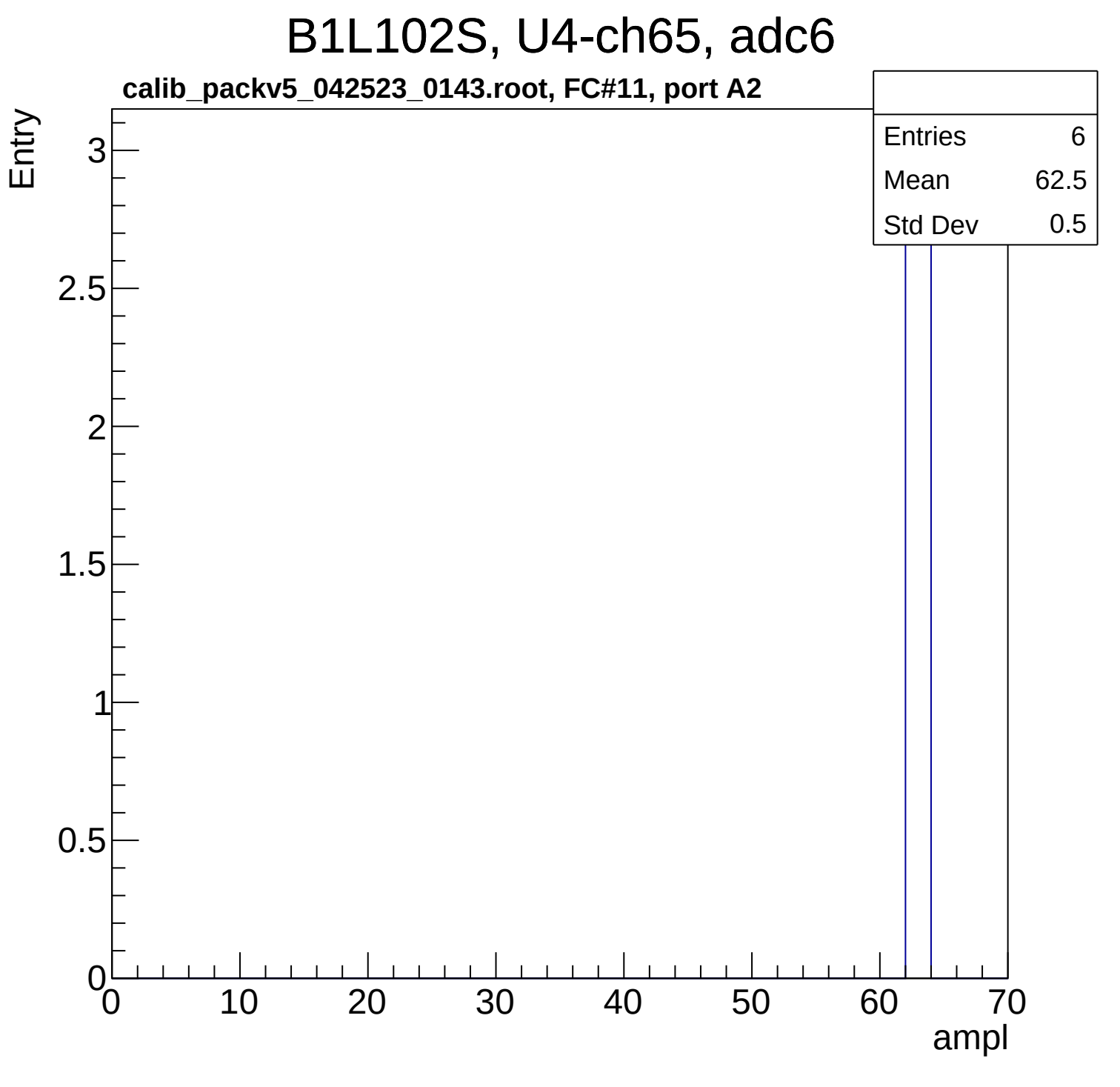
B1L102S, U4-ch65, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 6
Mean 62.5
Std Dev 0.5
Entry
ampl
0
0.5
1
1.5
2
2.5
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0
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40
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60
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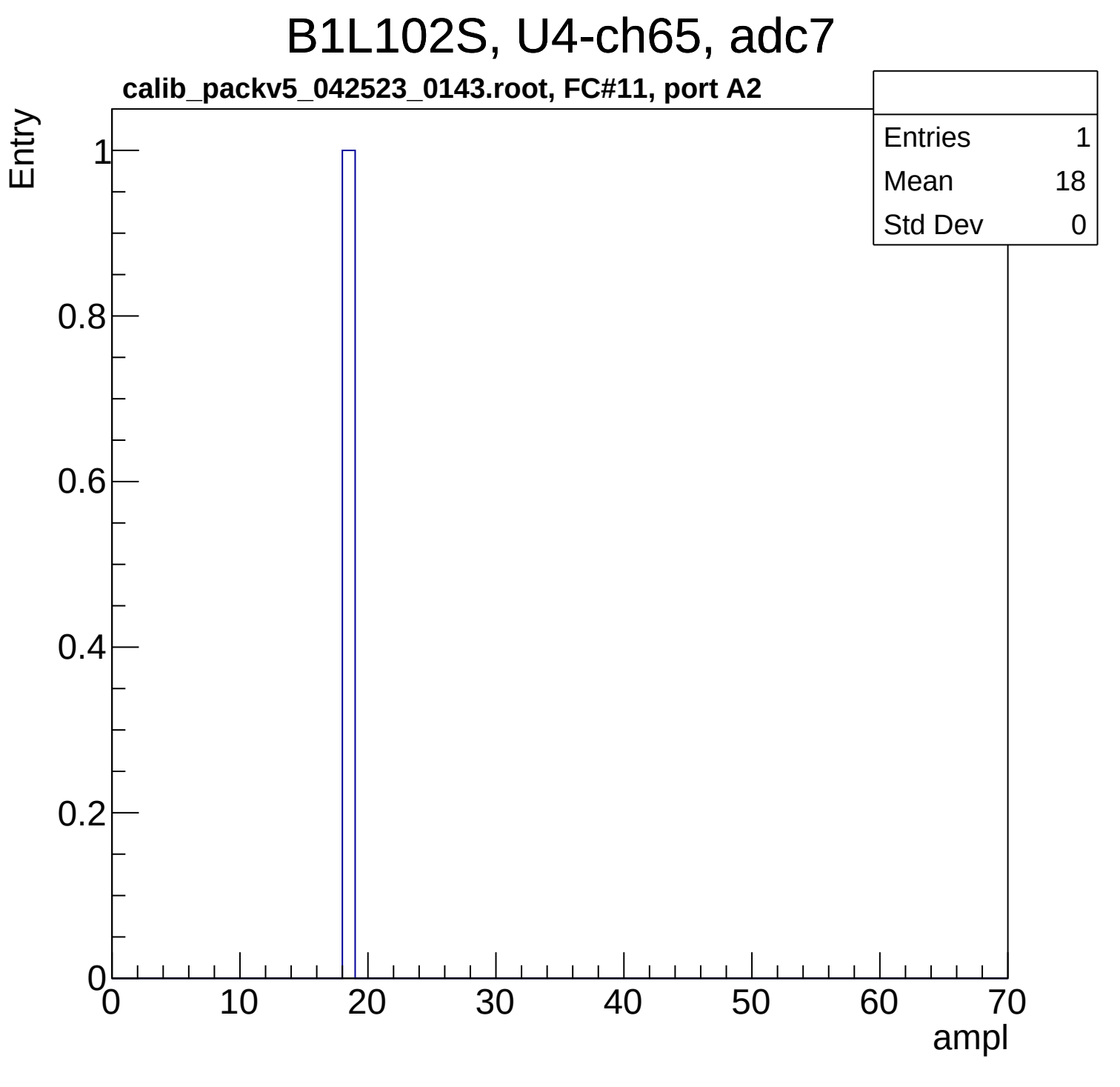
B1L102S, U4-ch65, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 18
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
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20
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40
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60
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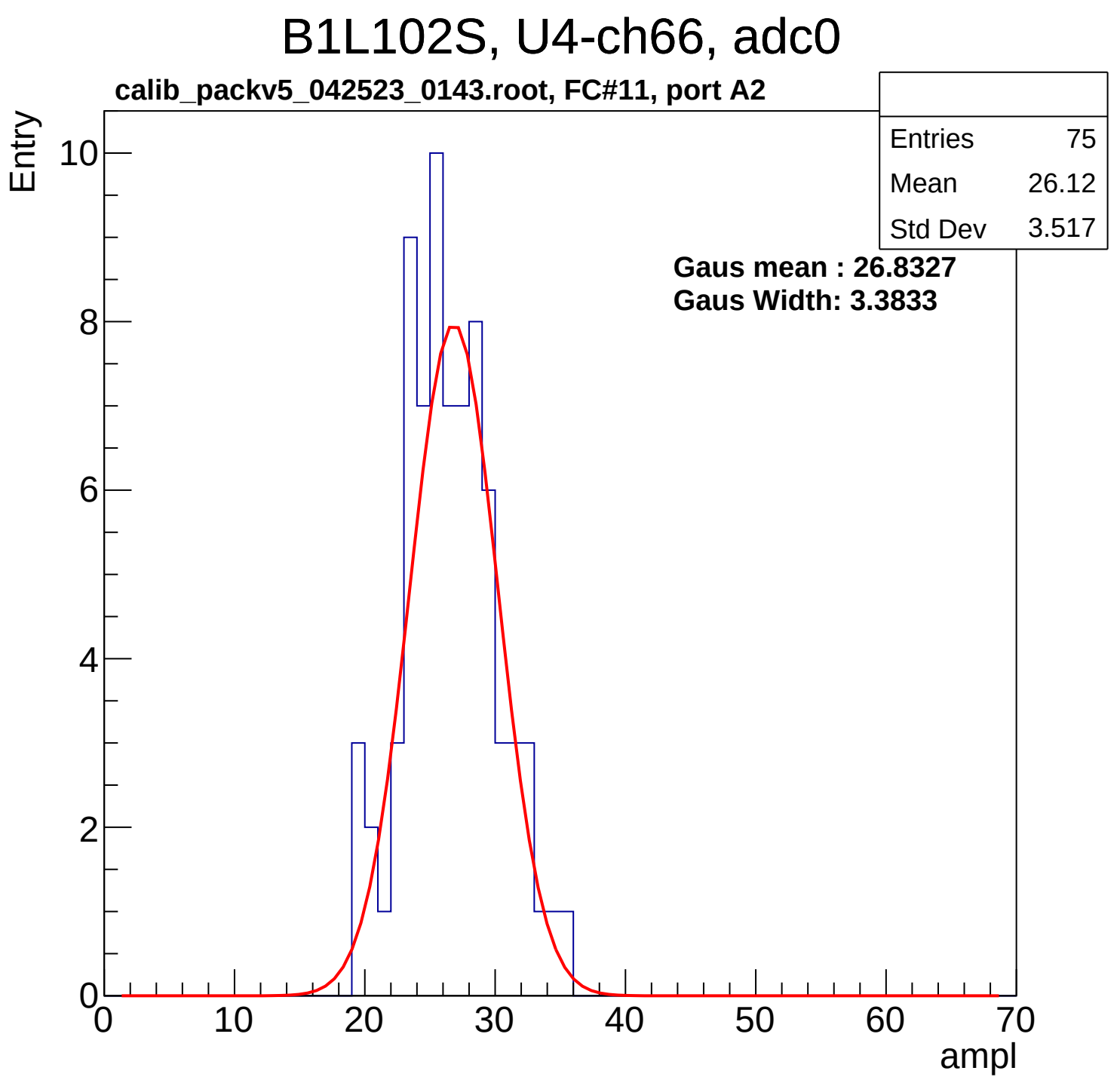
B1L102S, U4-ch66, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 26.12
Std Dev 3.517
Gaus mean : 26.8327
Gaus Width: 3.3833
Entry
ampl
0
2
4
6
8
10
0
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20
30
40
50
60
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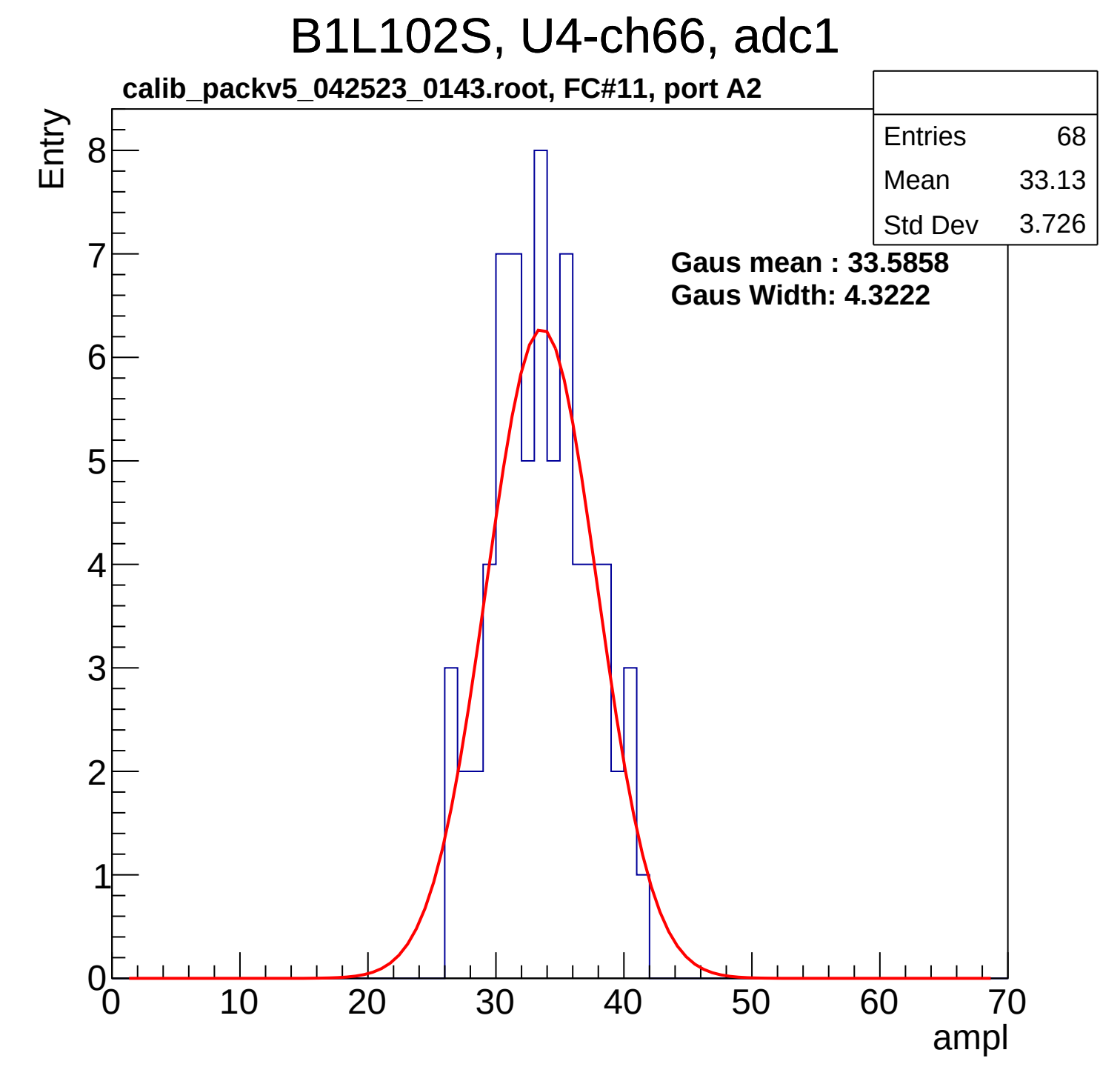
B1L102S, U4-ch66, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 33.13
Std Dev 3.726
Gaus mean : 33.5858
Gaus Width: 4.3222
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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20
30
40
50
60
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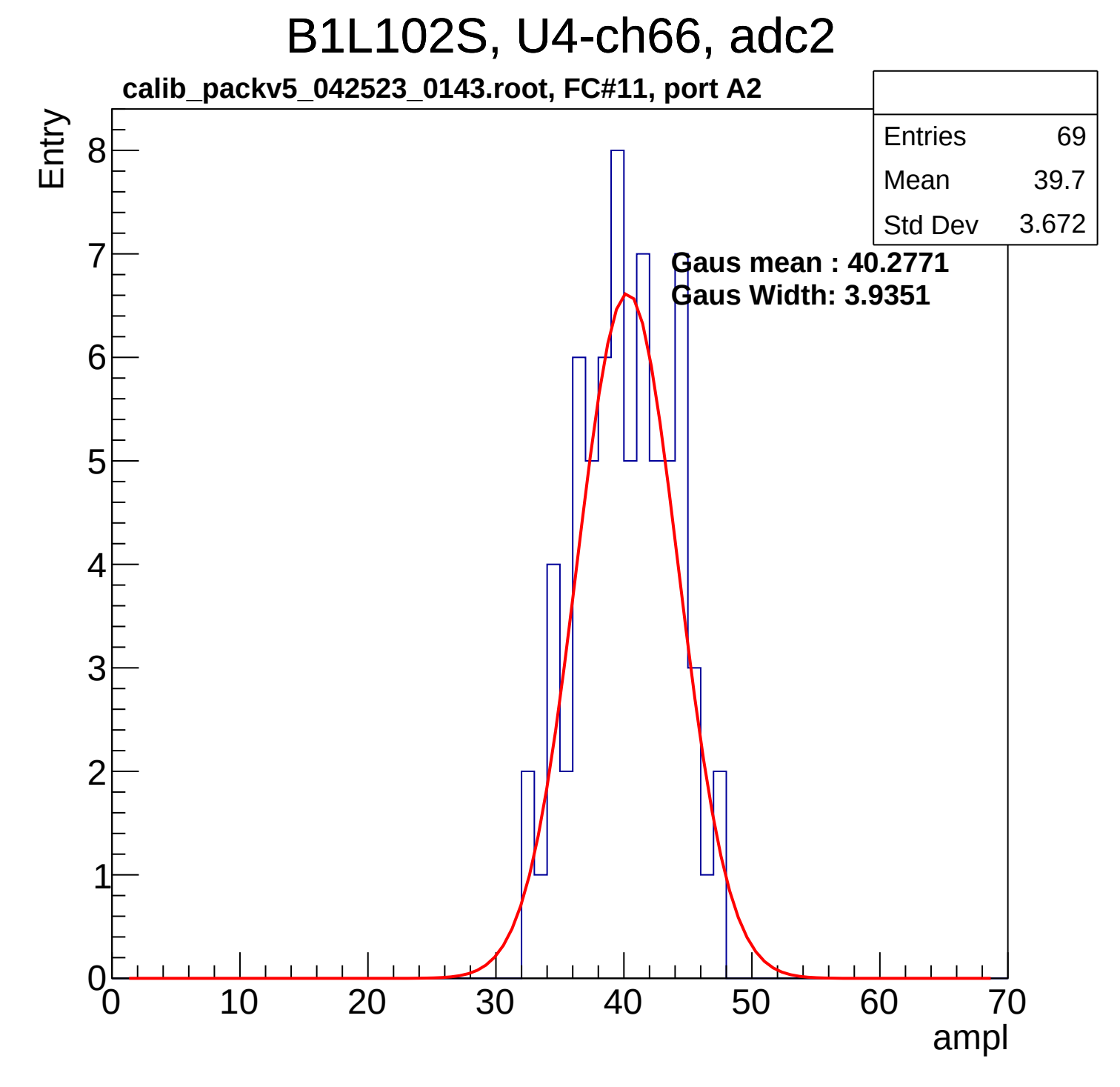
B1L102S, U4-ch66, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 39.7
Std Dev 3.672
Gaus mean : 40.2771
Gaus Width: 3.9351
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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40
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60
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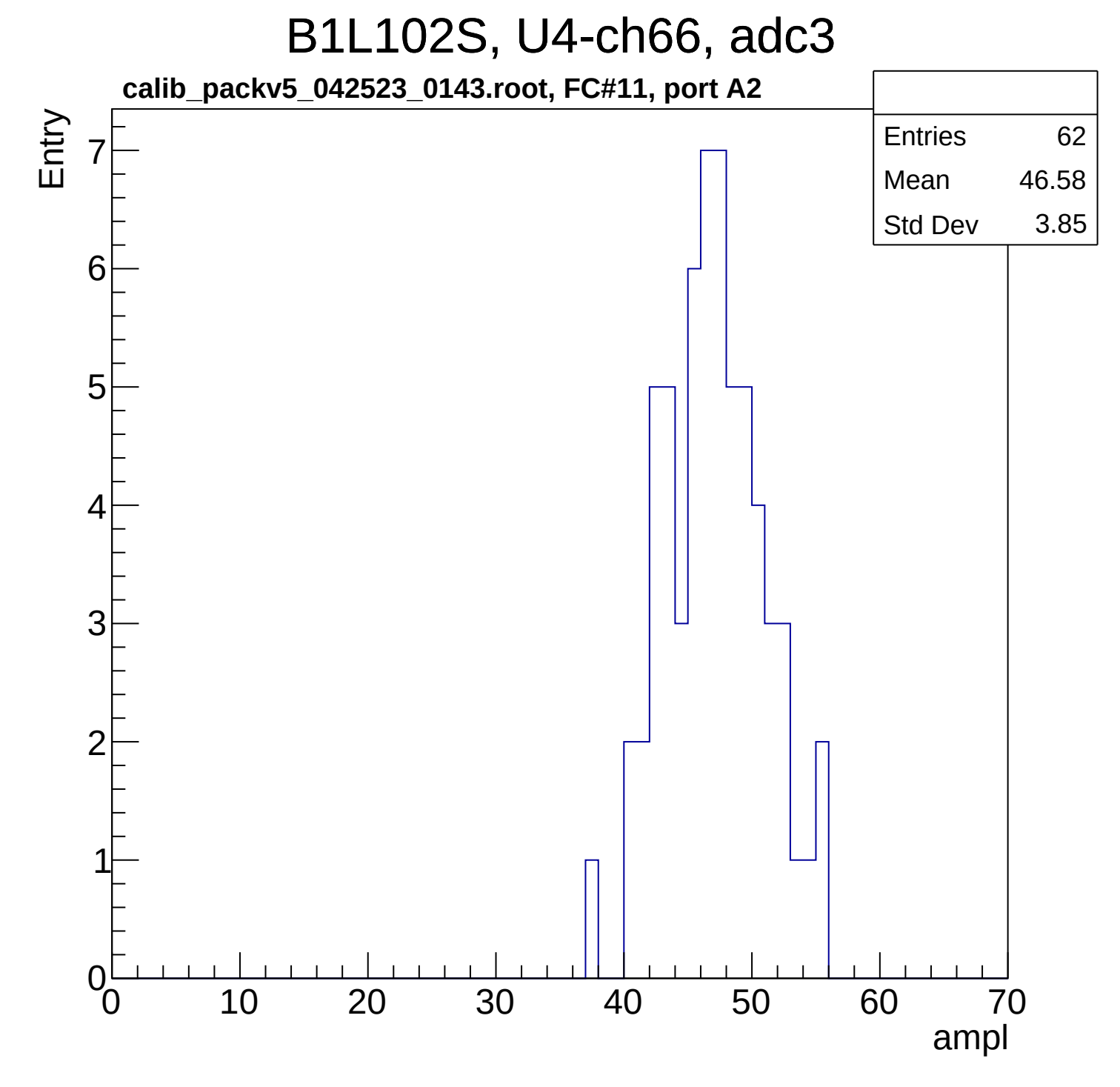
B1L102S, U4-ch66, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 46.58
Std Dev 3.85
Entry
ampl
0
1
2
3
4
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0
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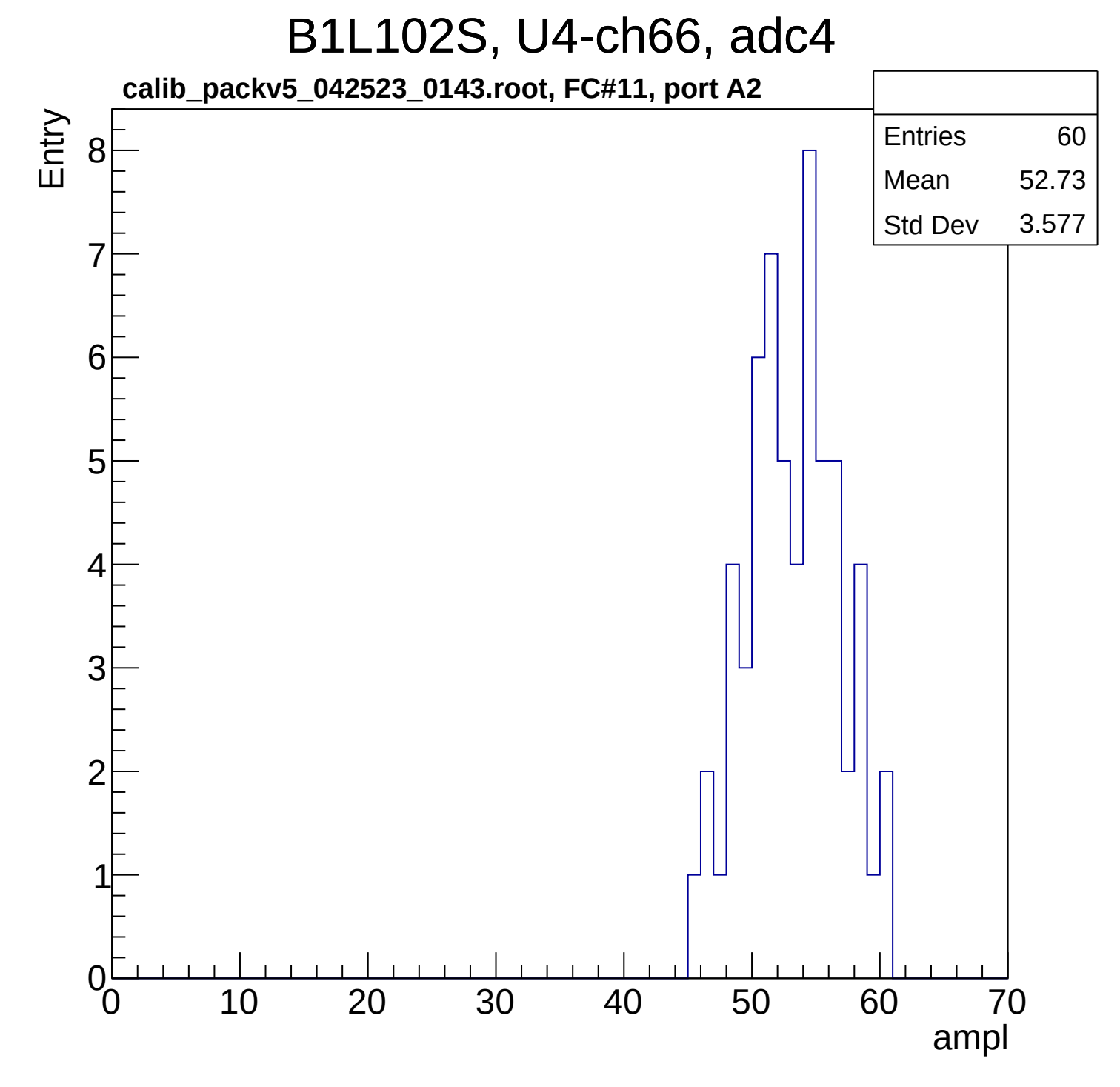
B1L102S, U4-ch66, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 52.73
Std Dev 3.577
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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40
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60
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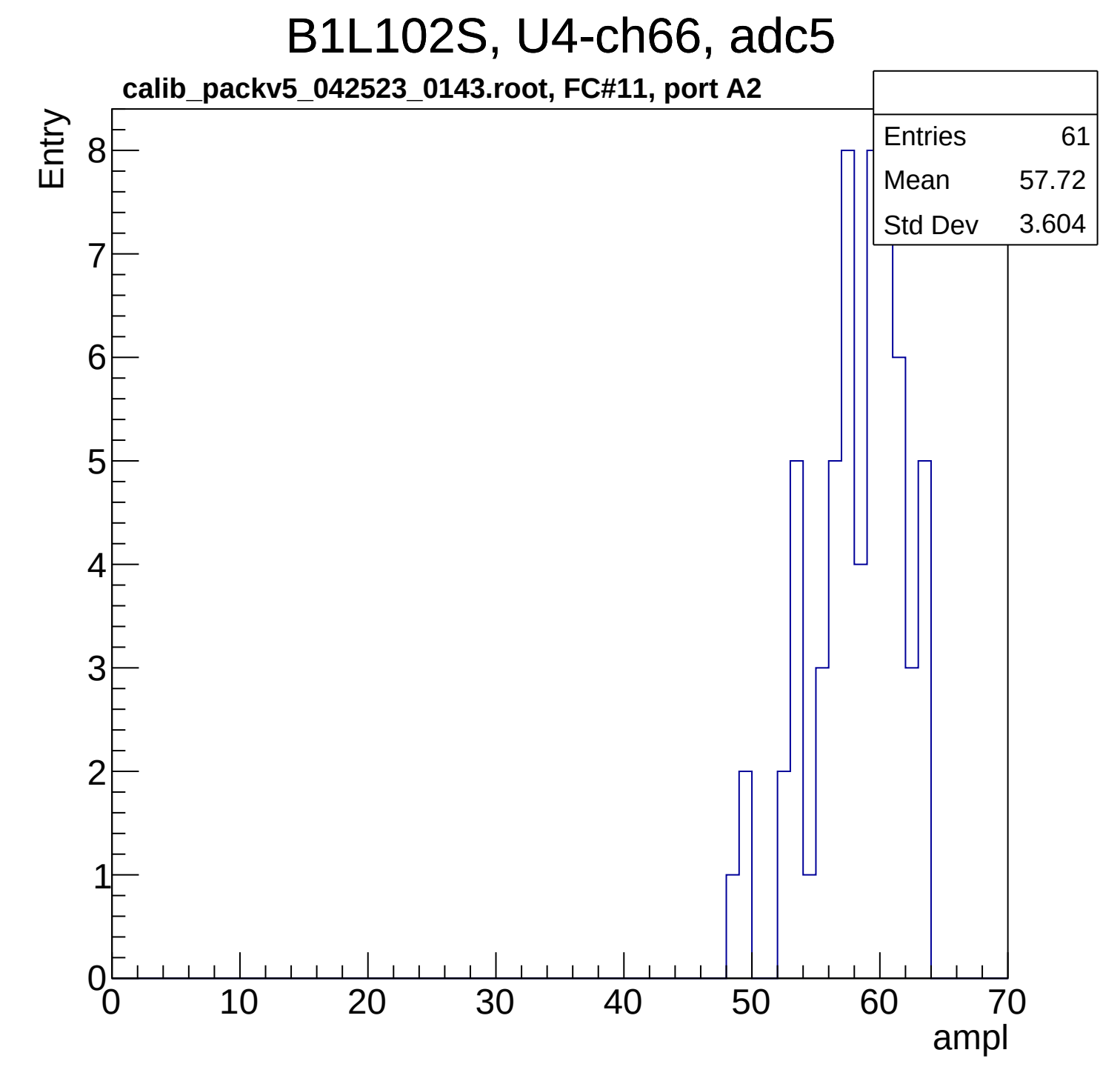
B1L102S, U4-ch66, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 57.72
Std Dev 3.604
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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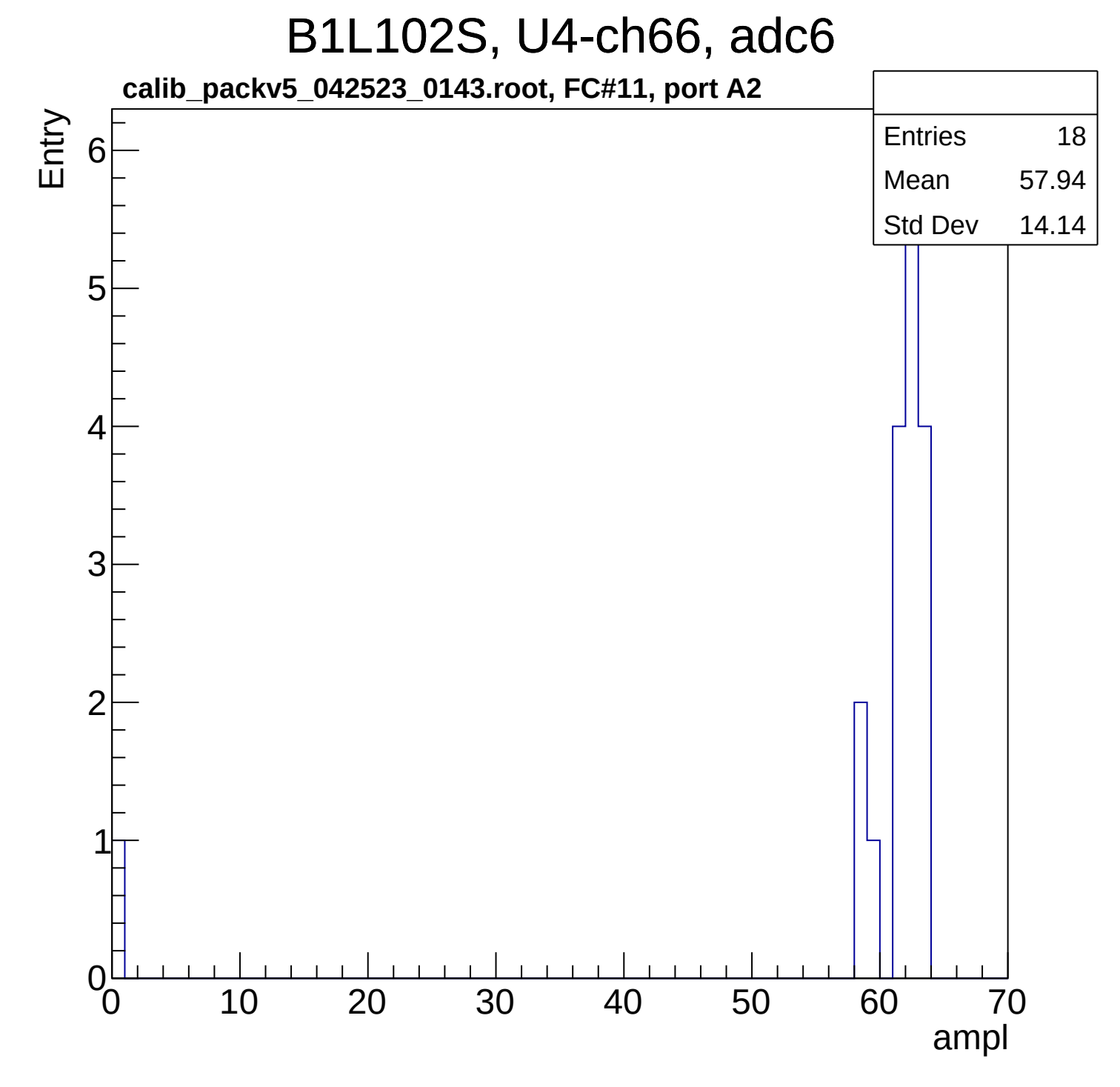
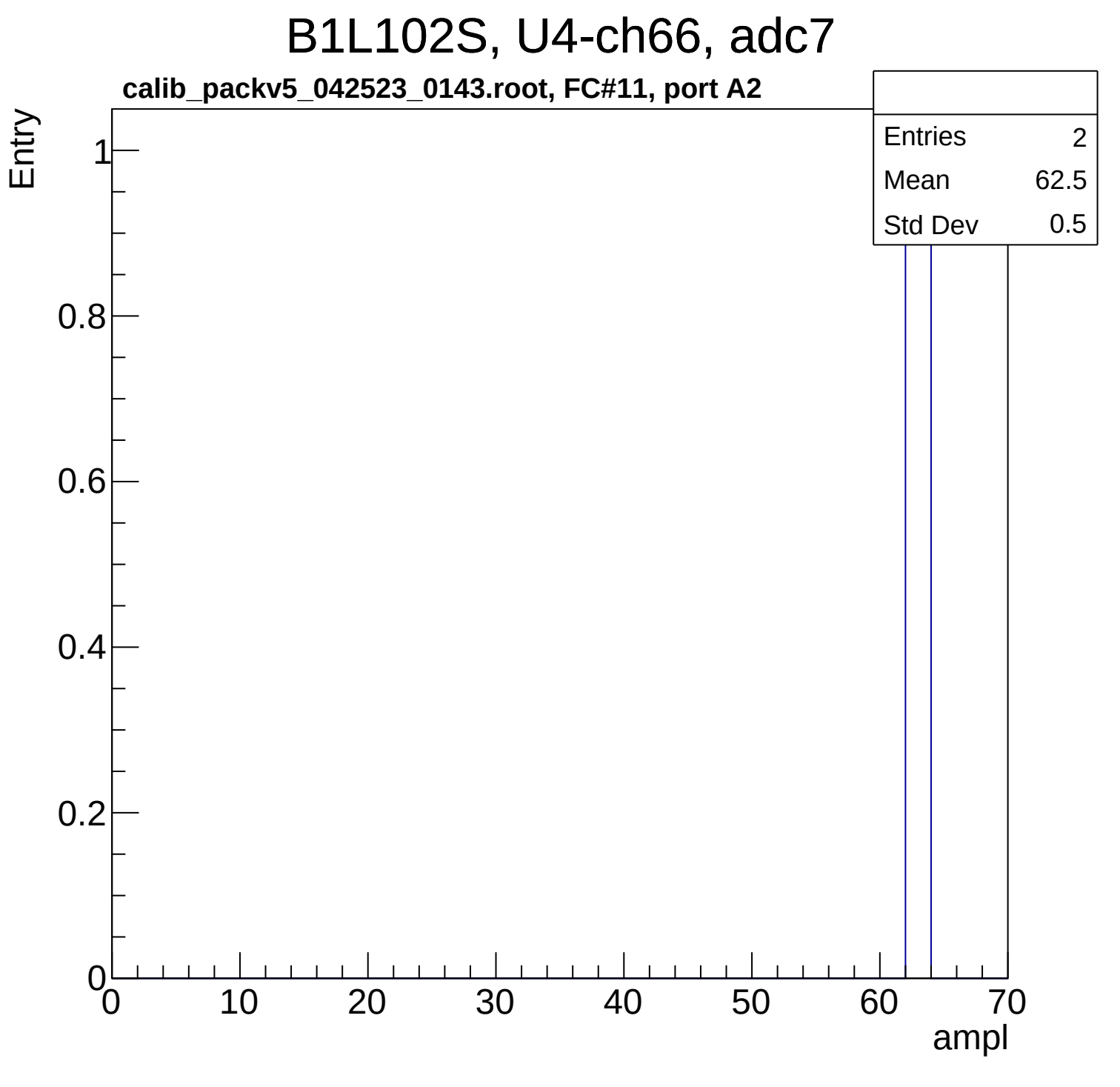
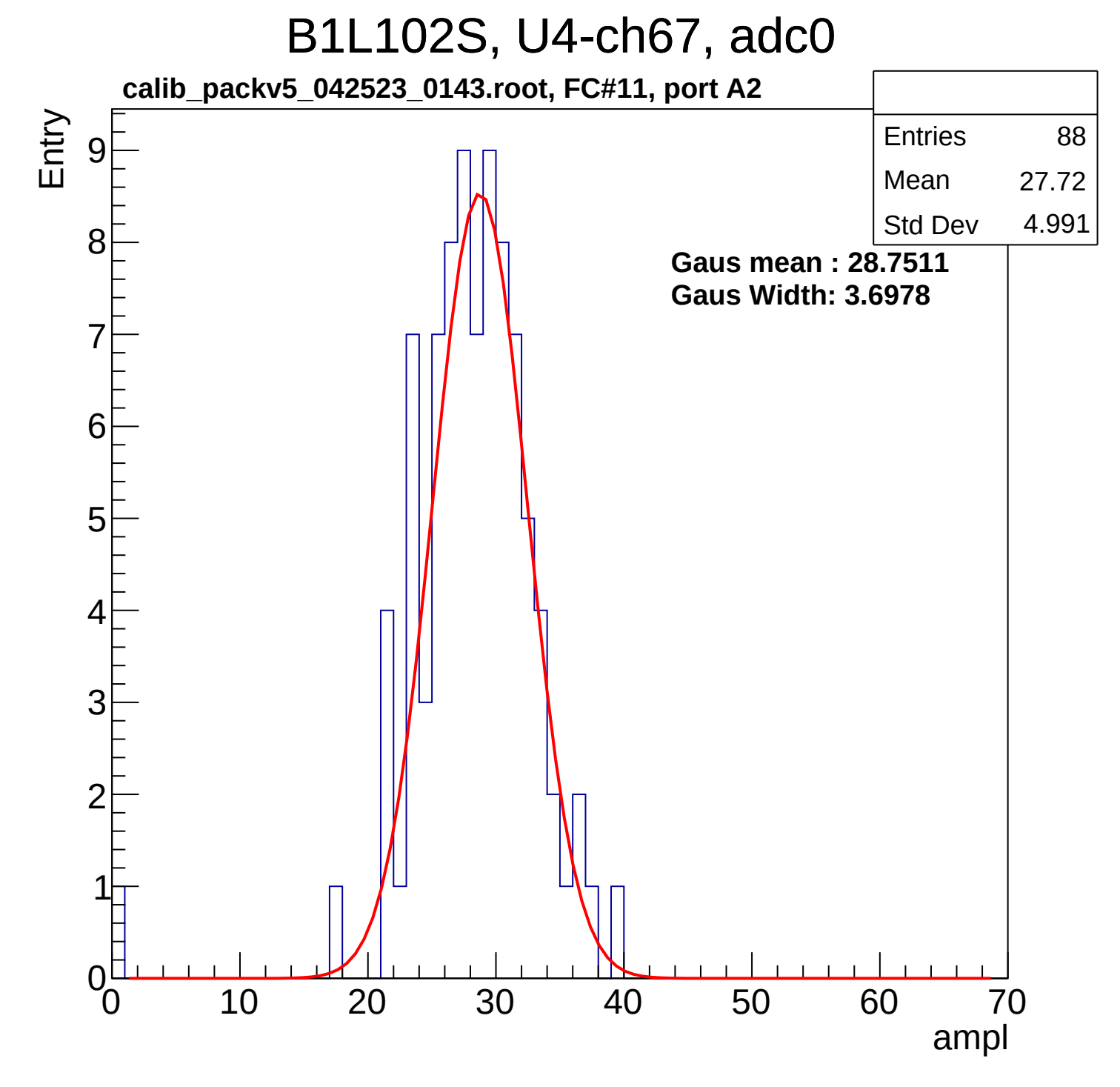
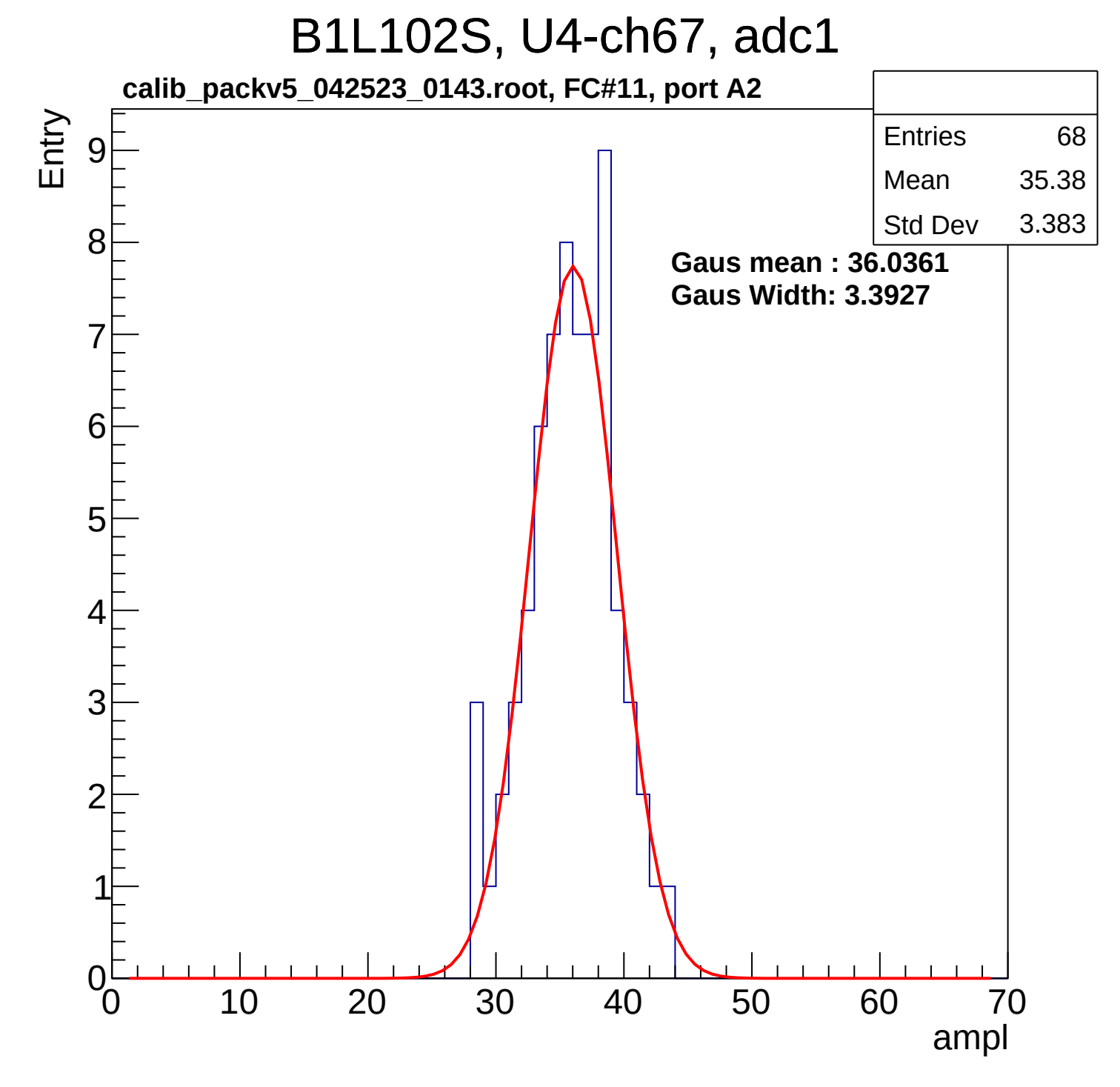

B1L102S, U4-ch66, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 18
Mean 57.94
Std Dev 14.14
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L102S, U4-ch66, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch67, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 88
Mean 27.72
Std Dev 4.991
Gaus mean : 28.7511
Gaus Width: 3.6978
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch67, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 35.38
Std Dev 3.383
Gaus mean : 36.0361
Gaus Width: 3.3927
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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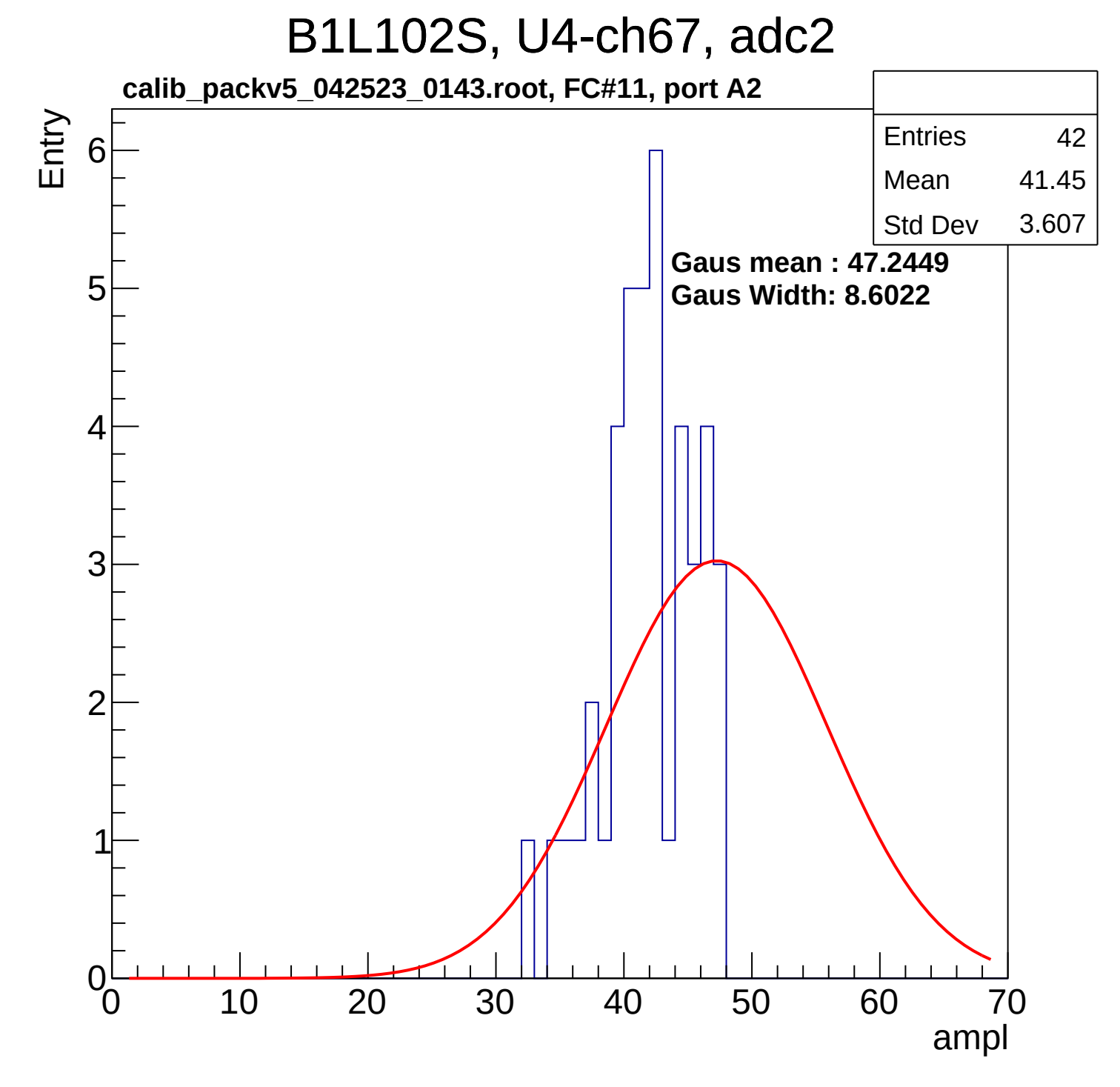
B1L102S, U4-ch67, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 42
Mean 41.45
Std Dev 3.607
Gaus mean : 47.2449
Gaus Width: 8.6022
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
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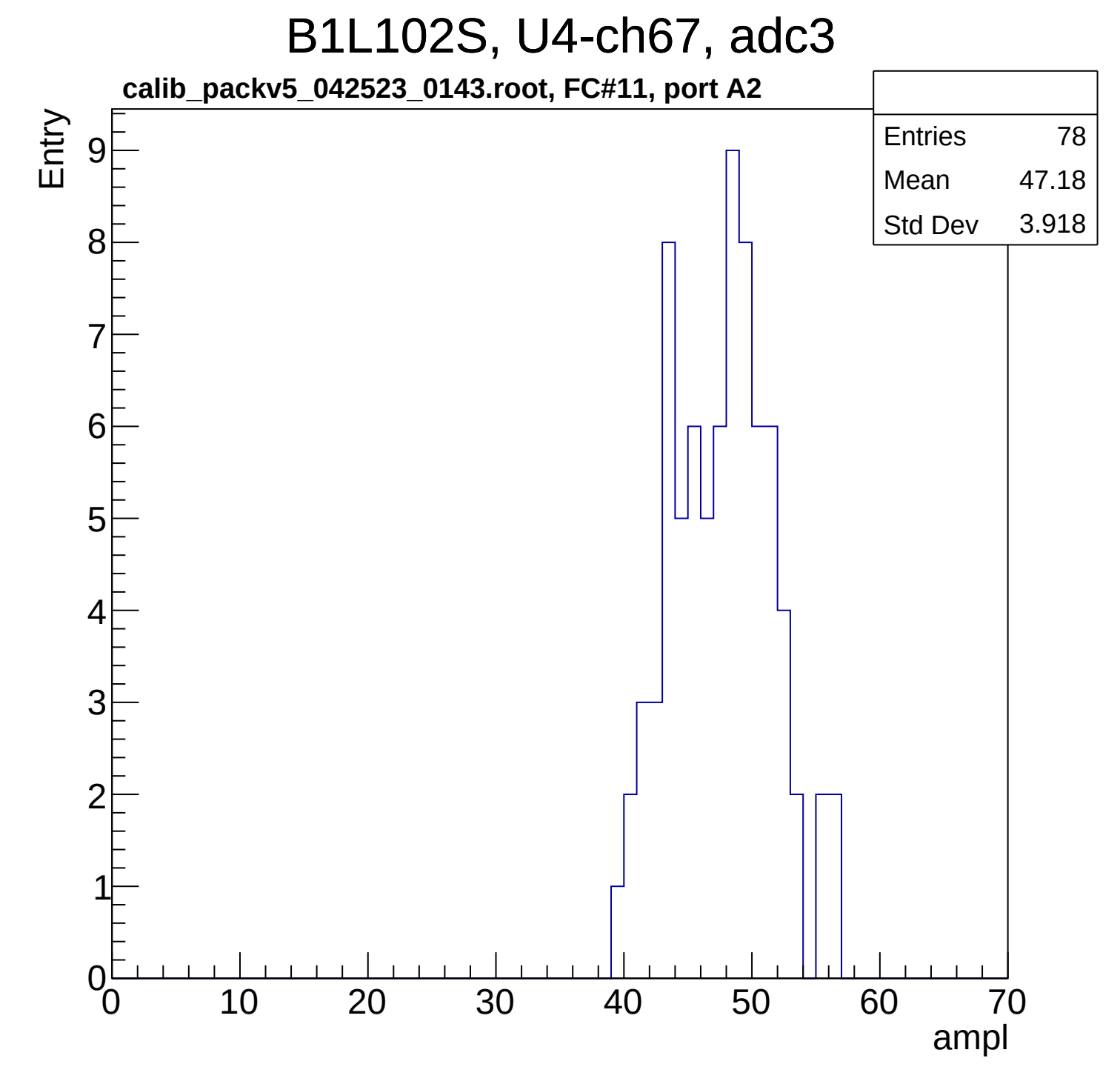
60
70


B1L102S, U4-ch67, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 78
Mean 47.18
Std Dev 3.918
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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60
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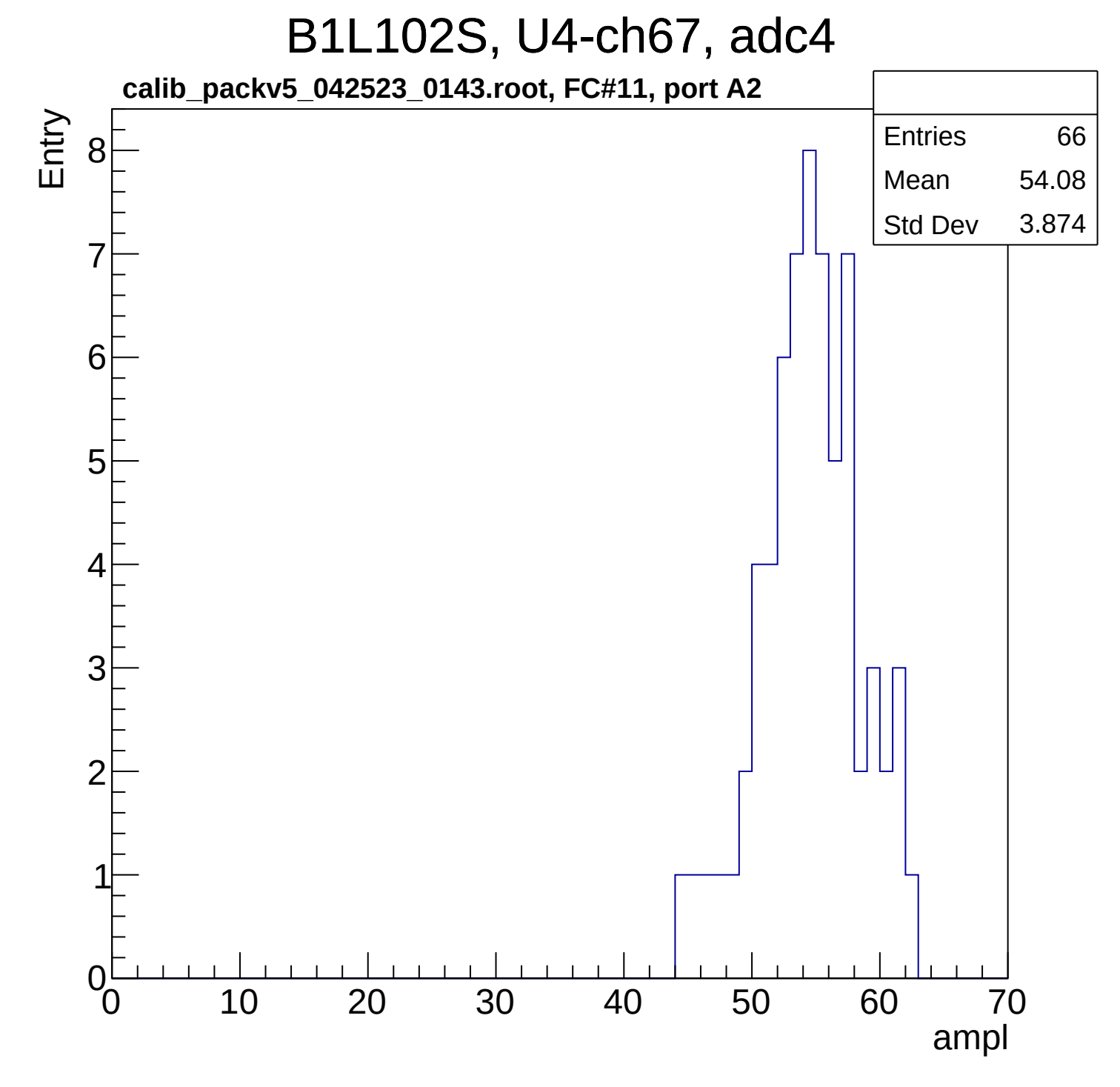
B1L102S, U4-ch67, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 54.08
Std Dev 3.874
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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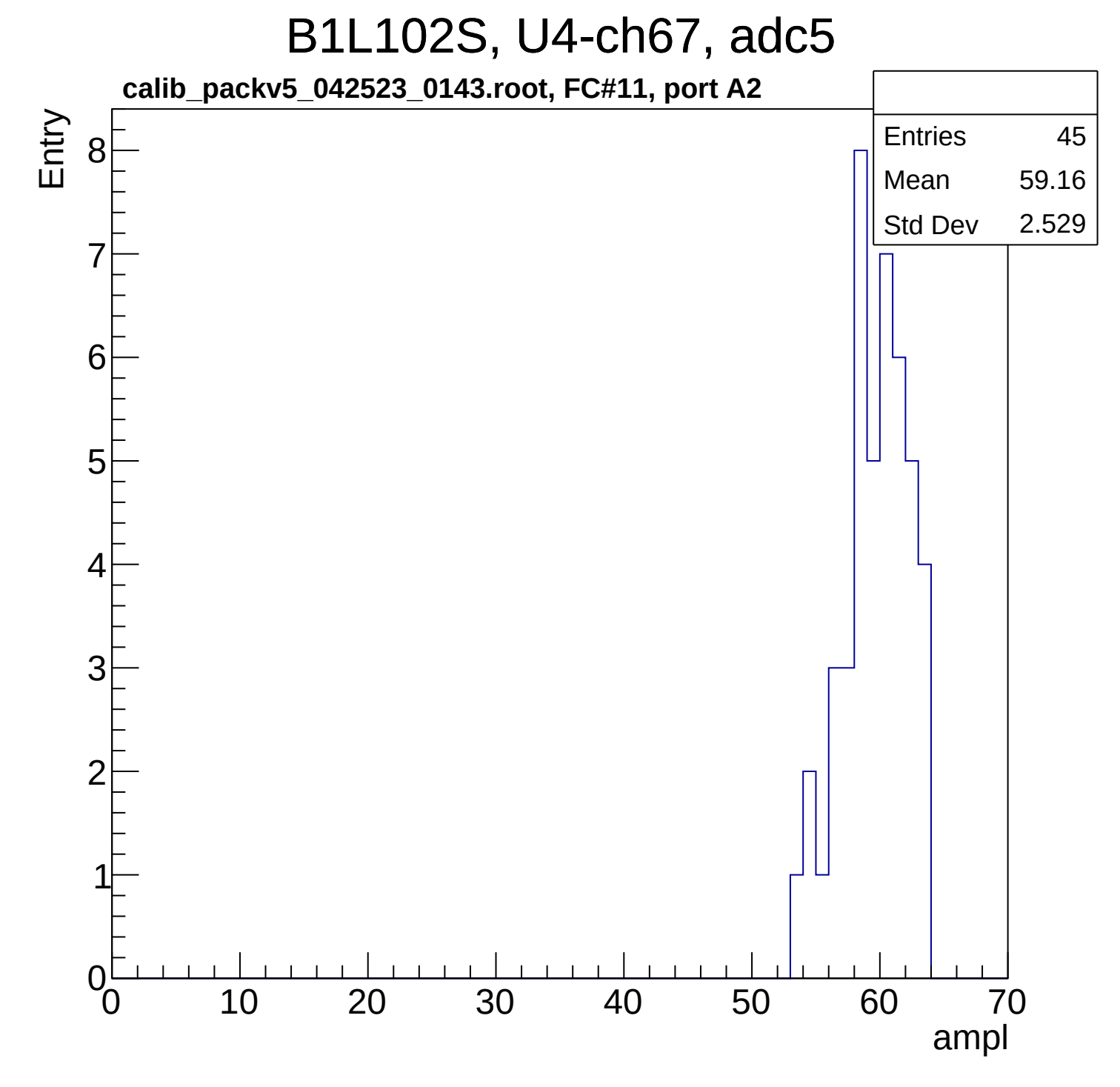
B1L102S, U4-ch67, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 45
Mean 59.16
Std Dev 2.529
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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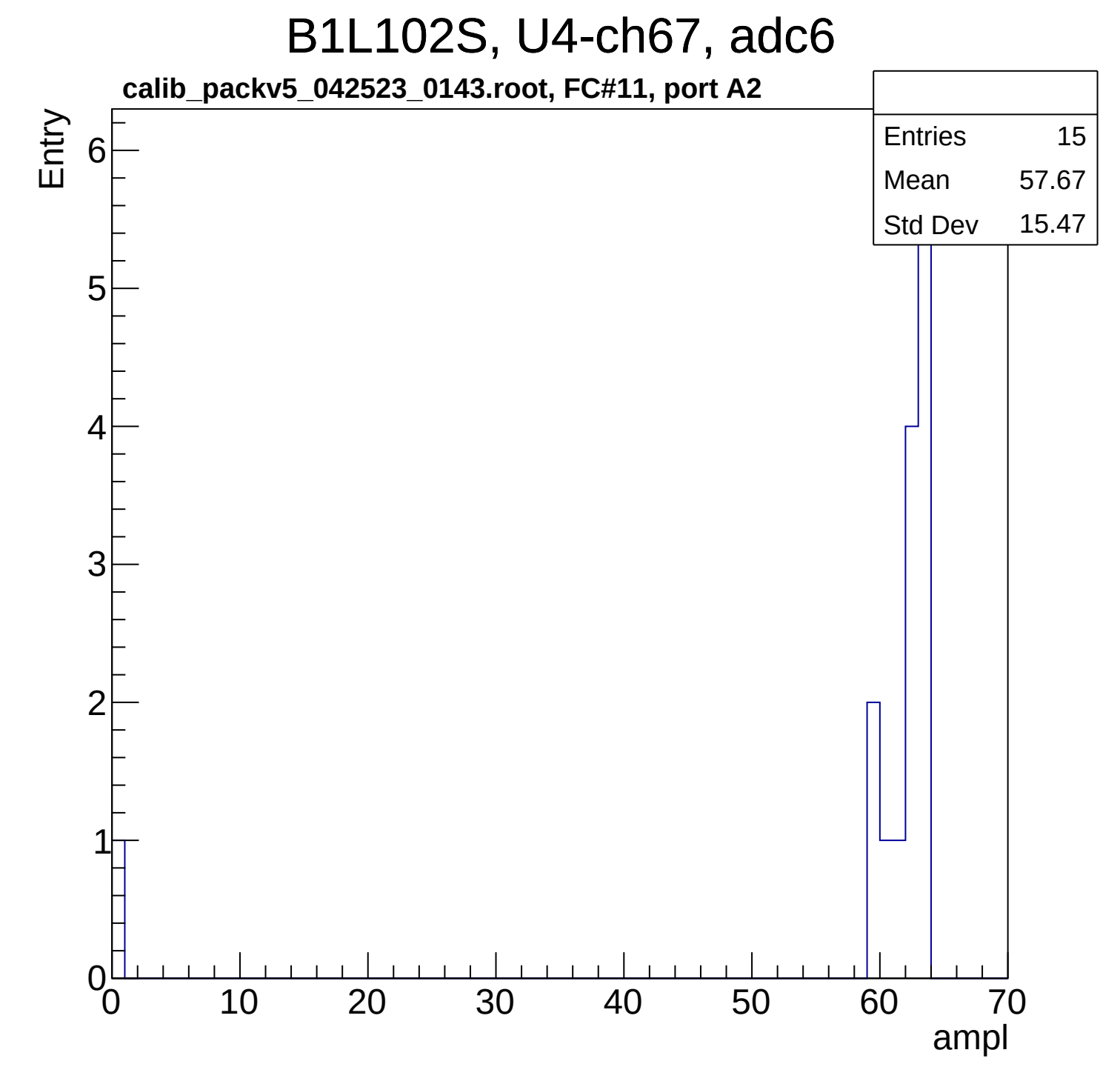
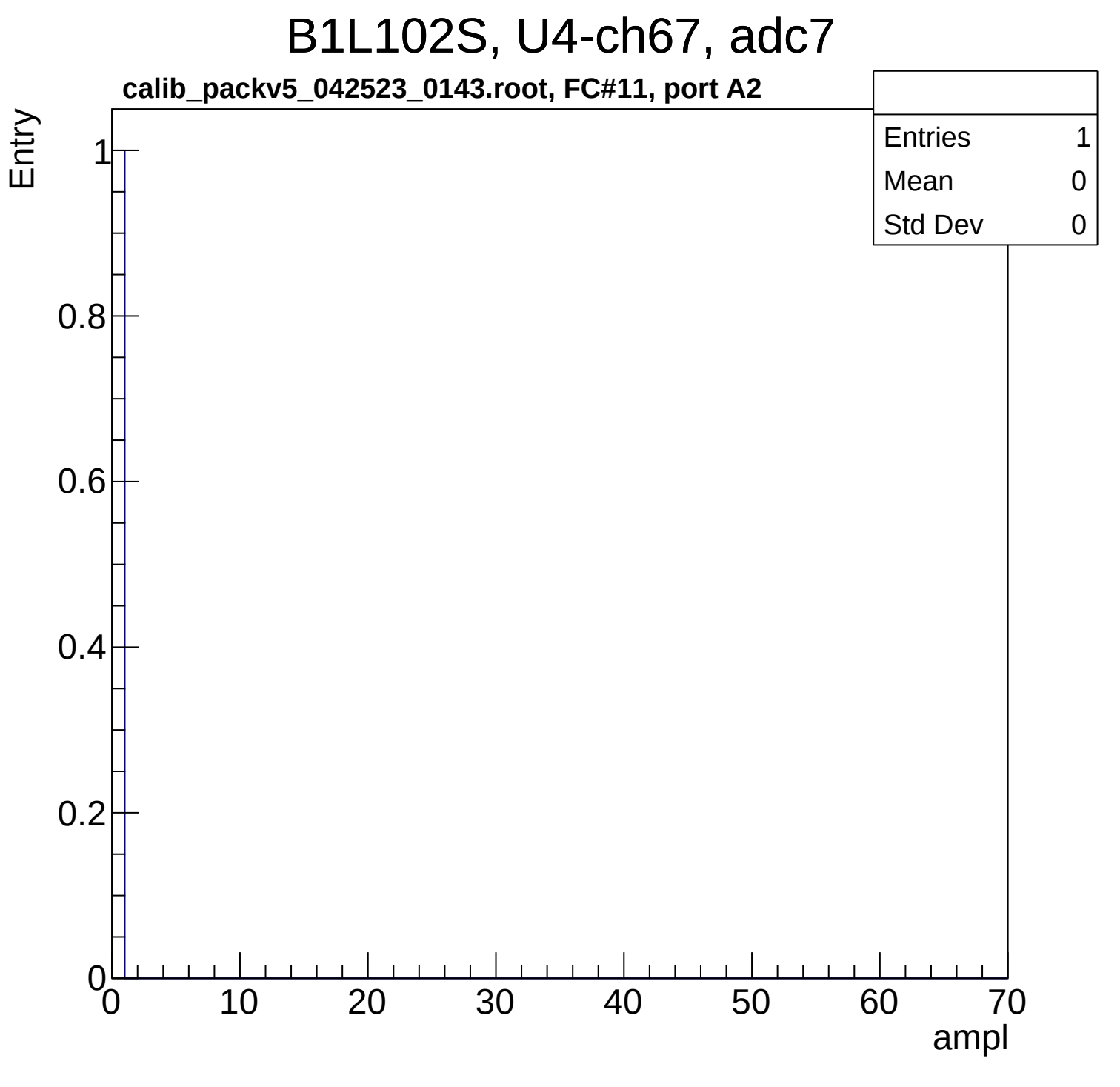

B1L102S, U4-ch67, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 15
Mean 57.67
Std Dev 15.47
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch67, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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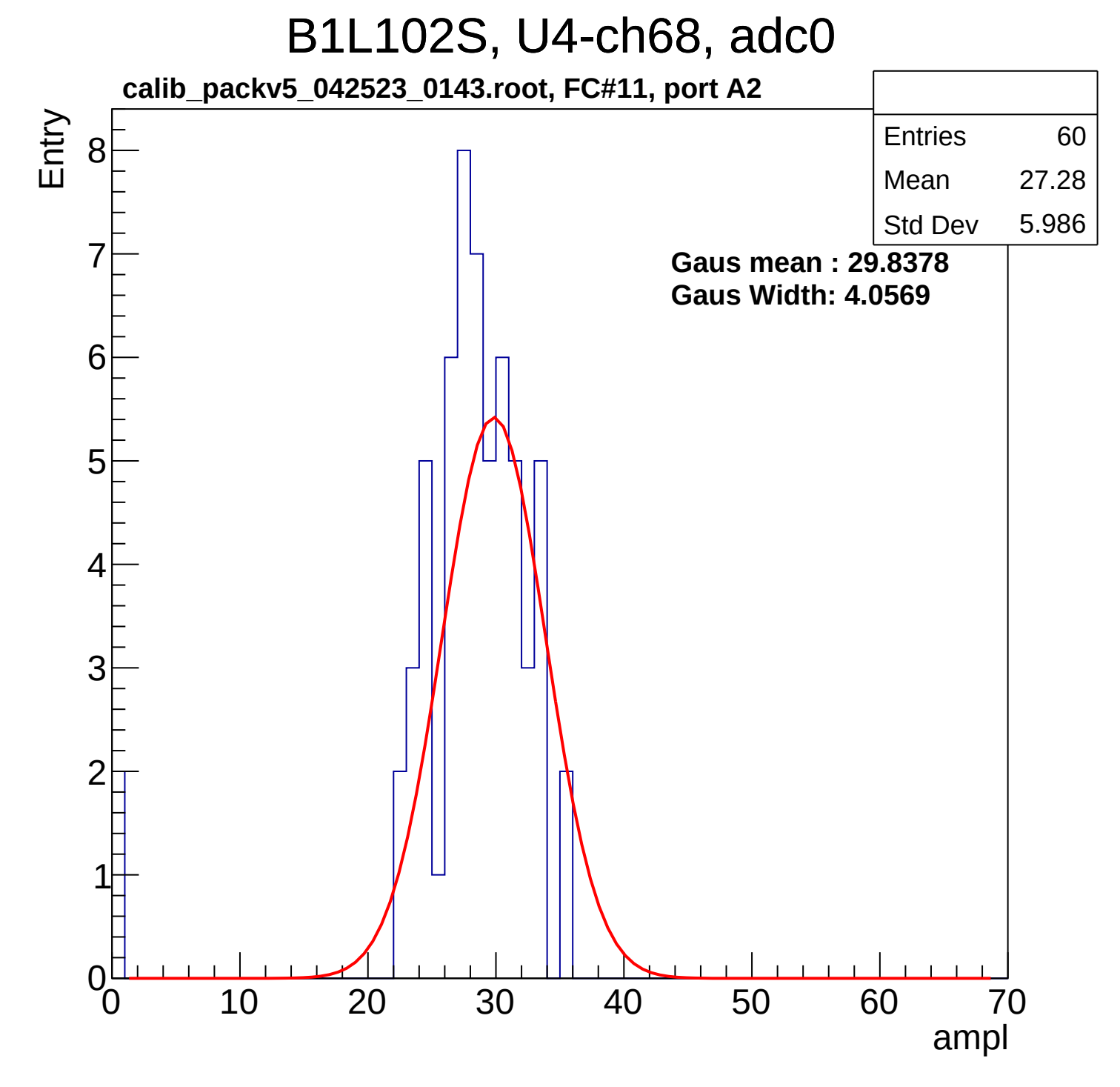
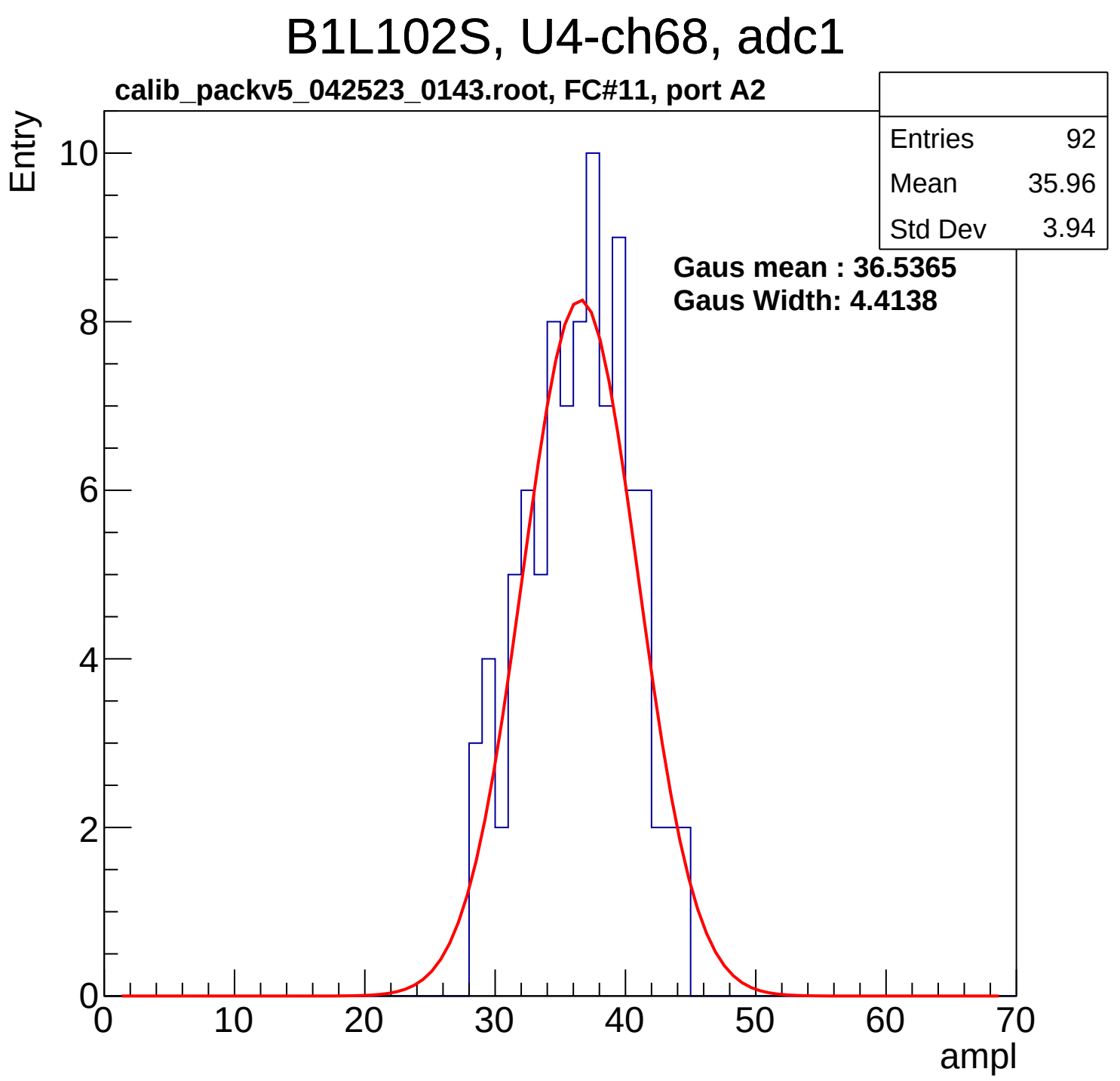
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch68, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 27.28
Std Dev 5.986
Gaus mean : 29.8378
Gaus Width: 4.0569
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch68, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 92
Mean 35.96
Std Dev 3.94
Gaus mean : 36.5365
Gaus Width: 4.4138
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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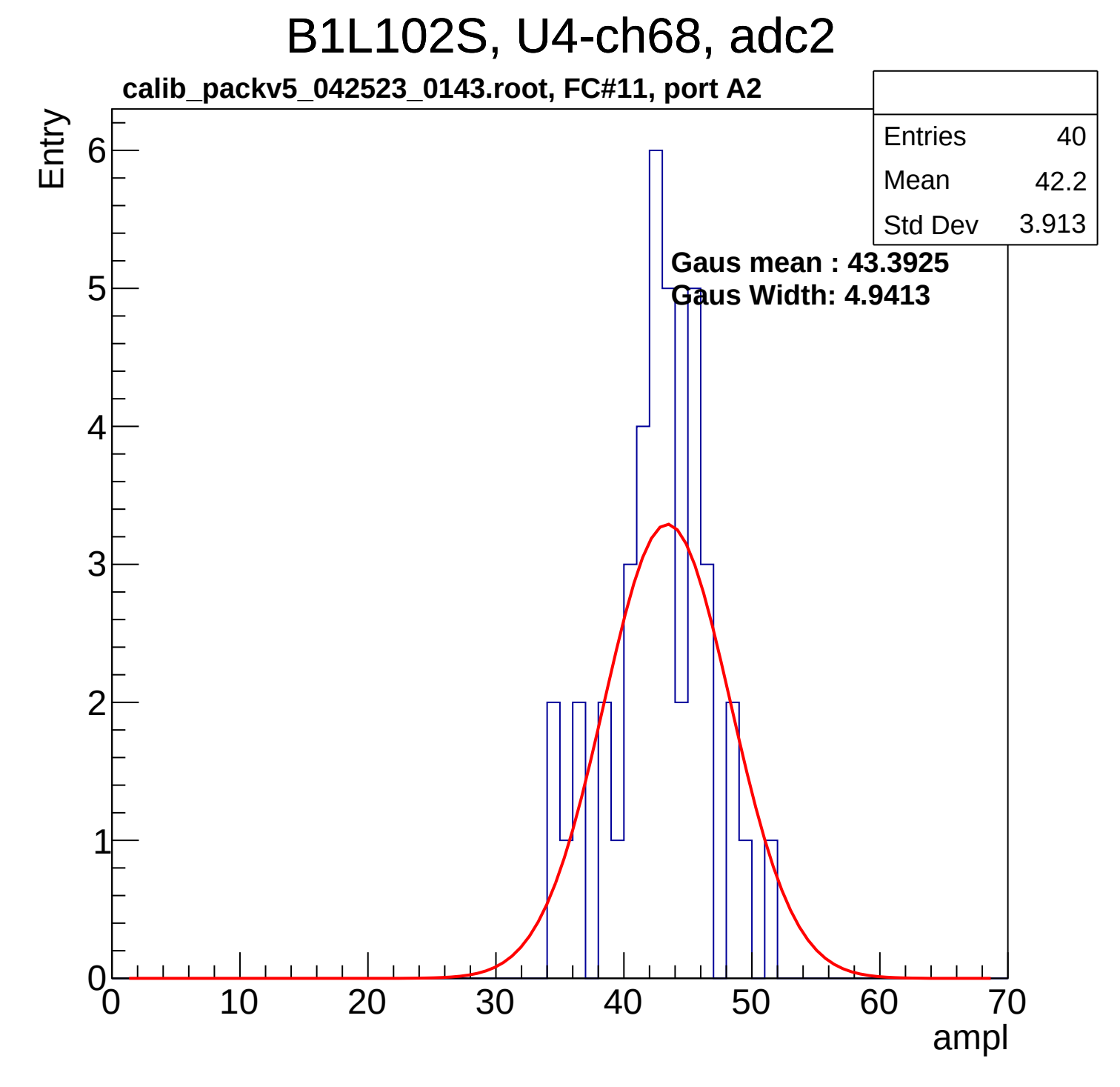
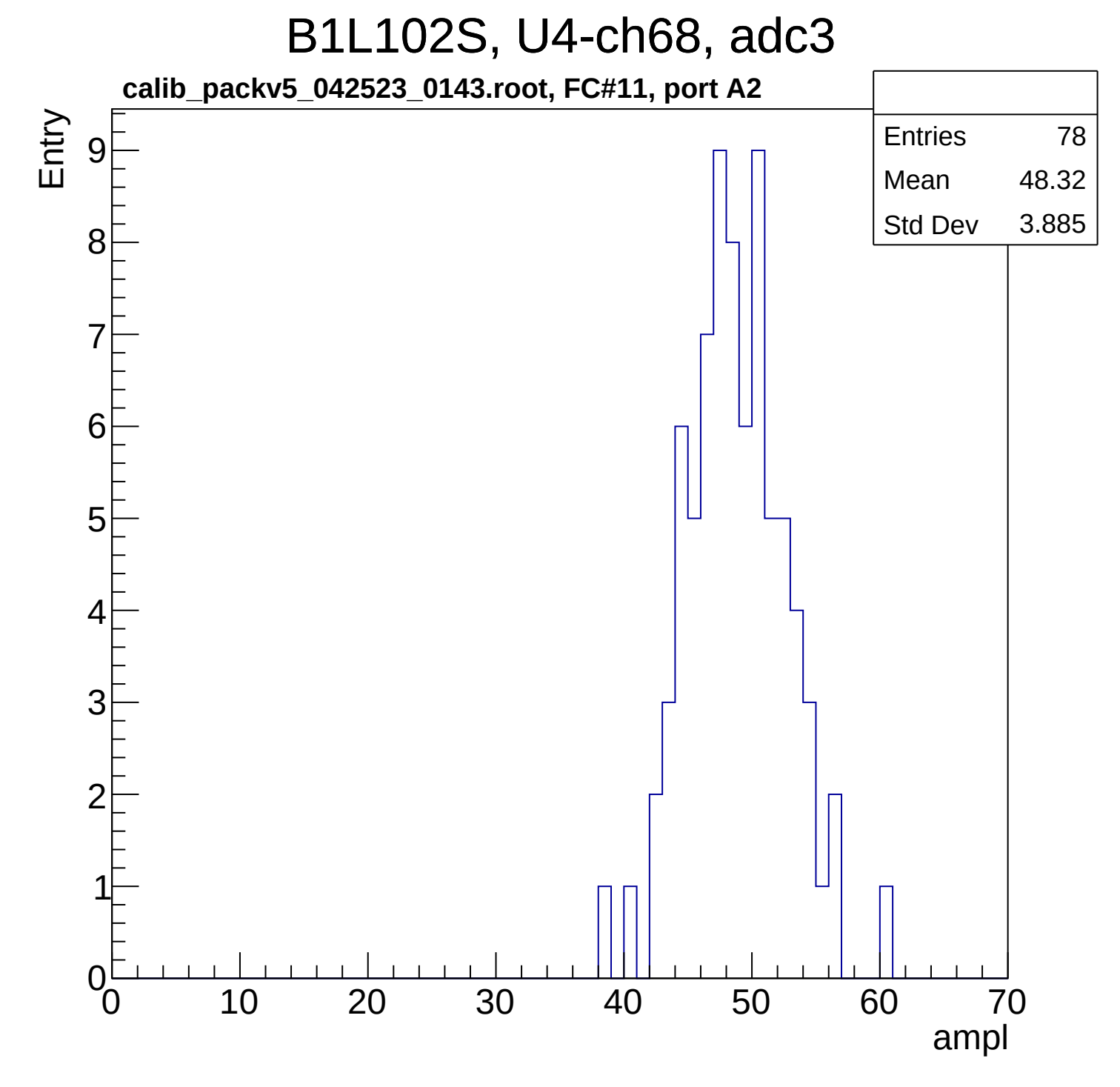

B1L102S, U4-ch68, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 40
Mean 42.2
Std Dev 3.913
Gaus mean : 43.3925
Gaus Width: 4.9413
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L102S, U4-ch68, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 78
Mean 48.32
Std Dev 3.885
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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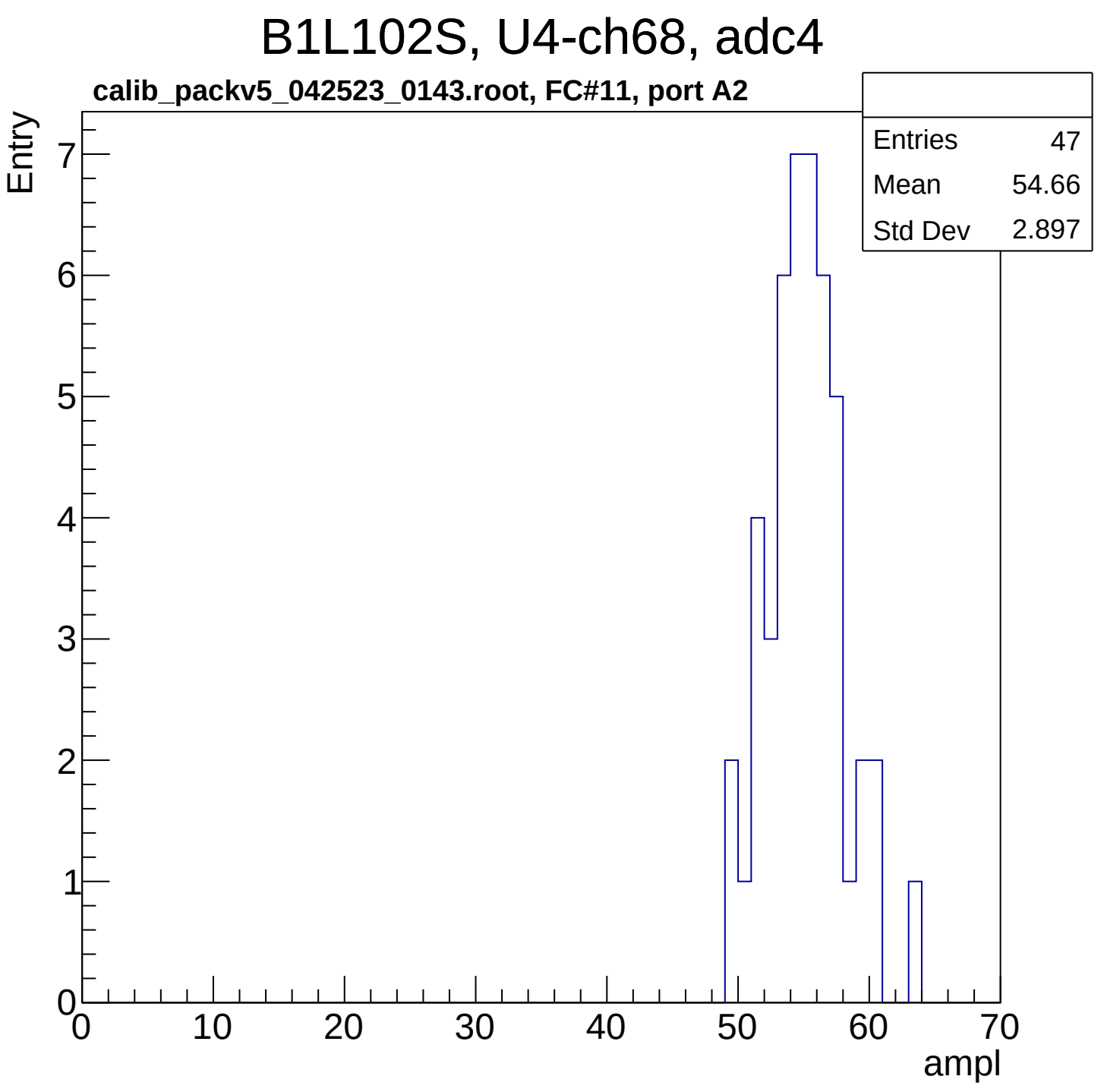
B1L102S, U4-ch68, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 47
Mean 54.66
Std Dev 2.897
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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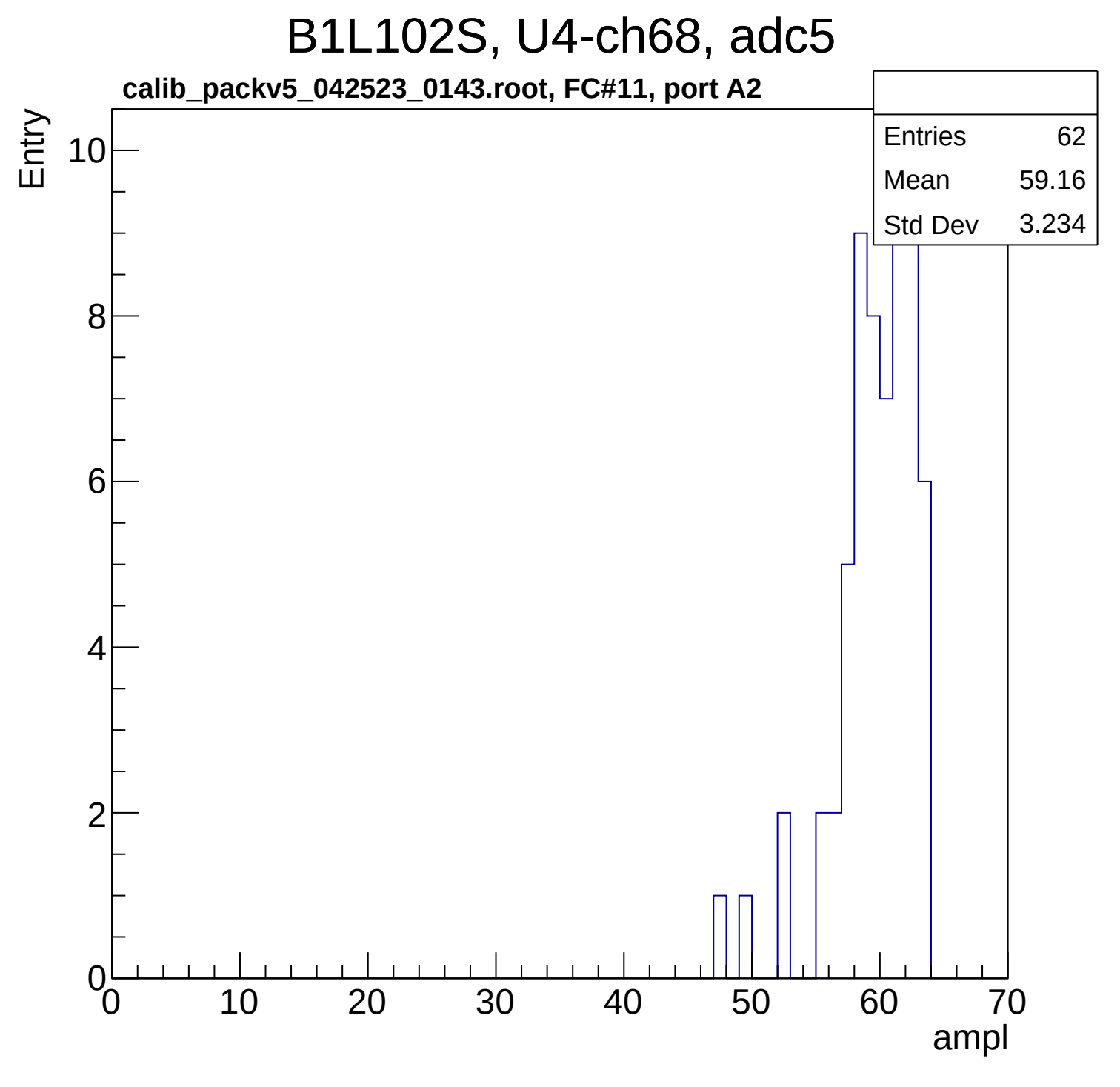
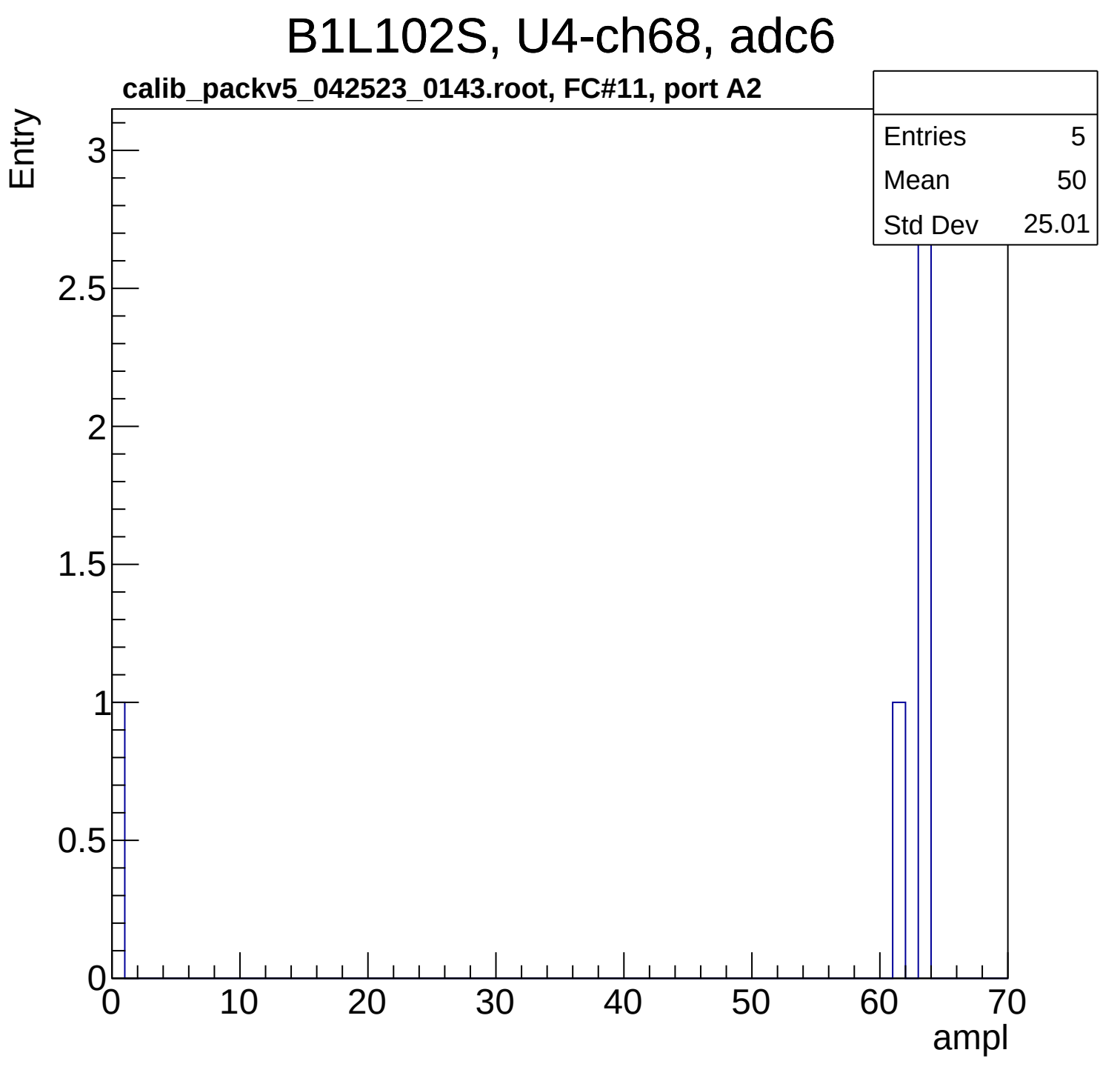

B1L102S, U4-ch68, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 59.16
Std Dev 3.234
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch68, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 5
Mean 50
Std Dev 25.01
Entry
ampl
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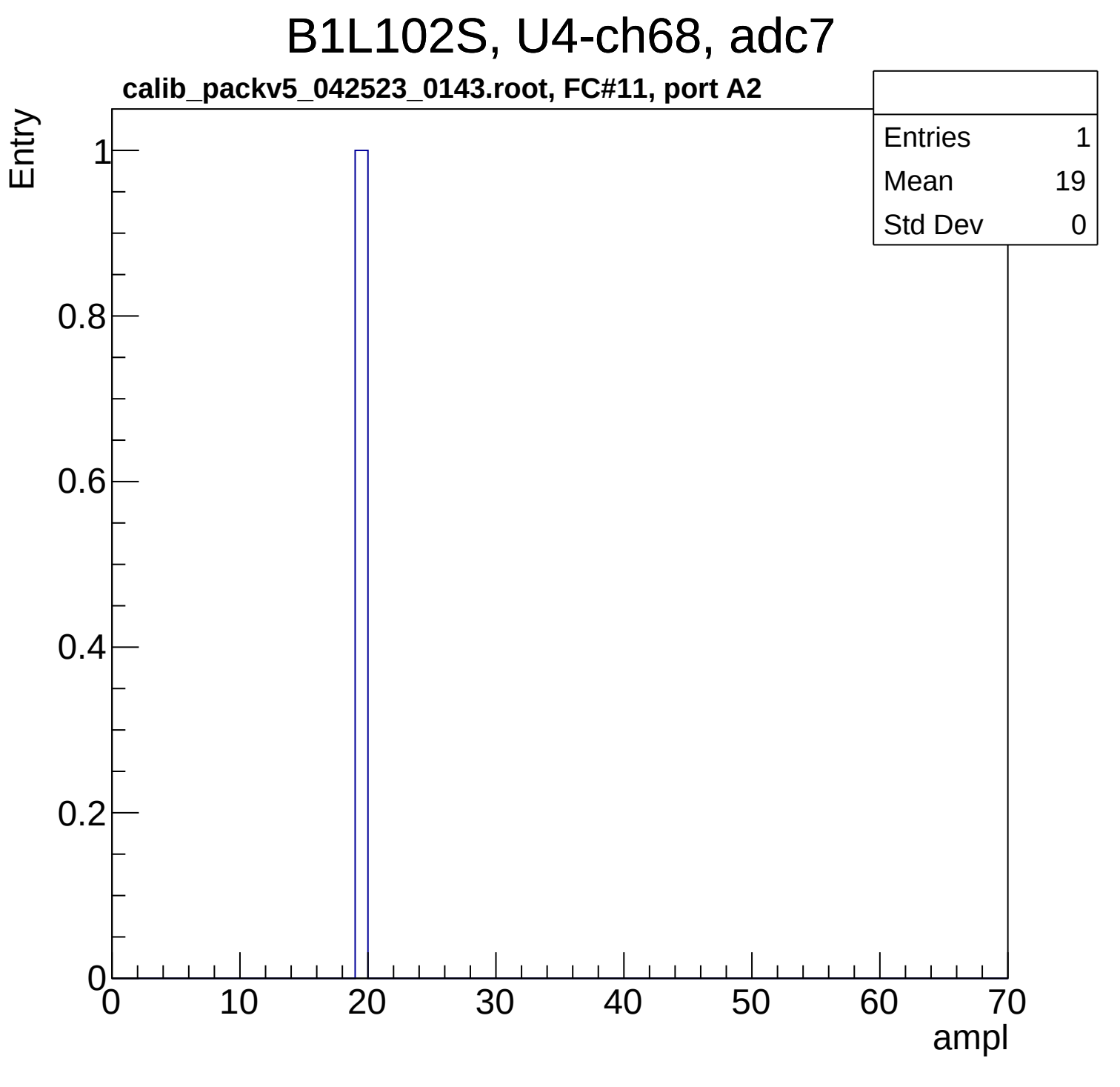
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U4-ch68, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 19
Std Dev 0
Entry
ampl
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0.4
0.6
0.8
1
0
10
20
30
40
50
60
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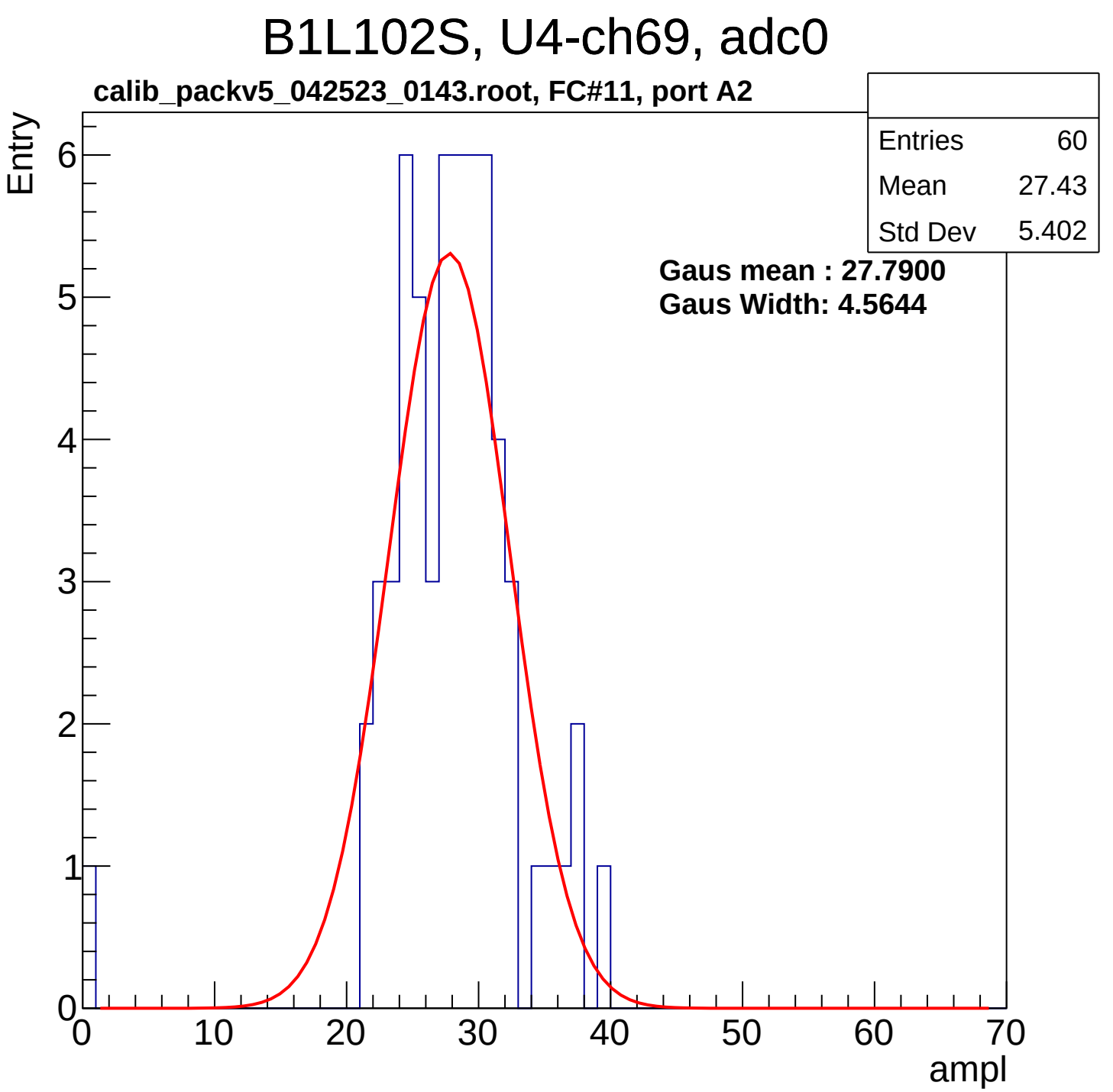
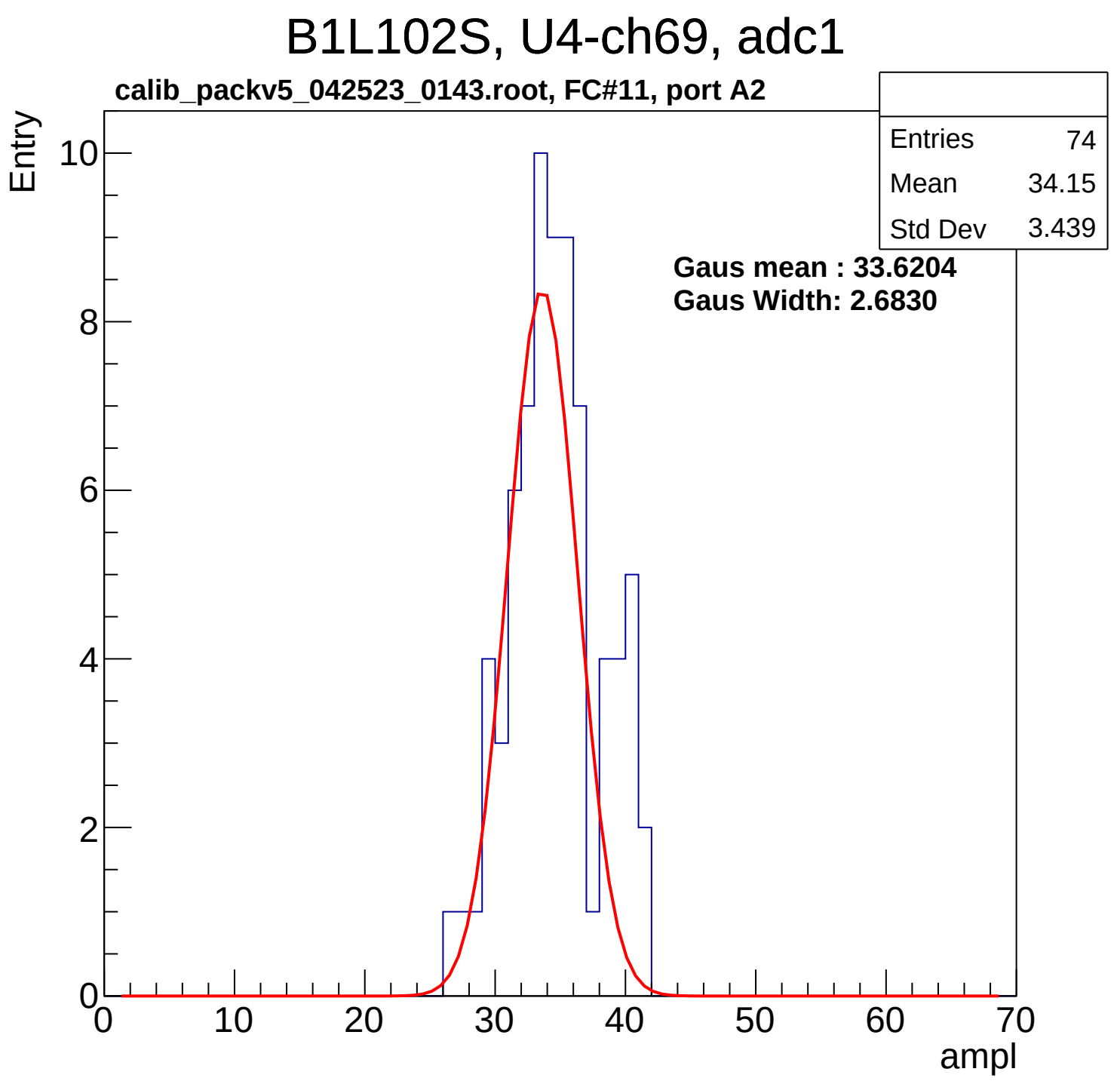
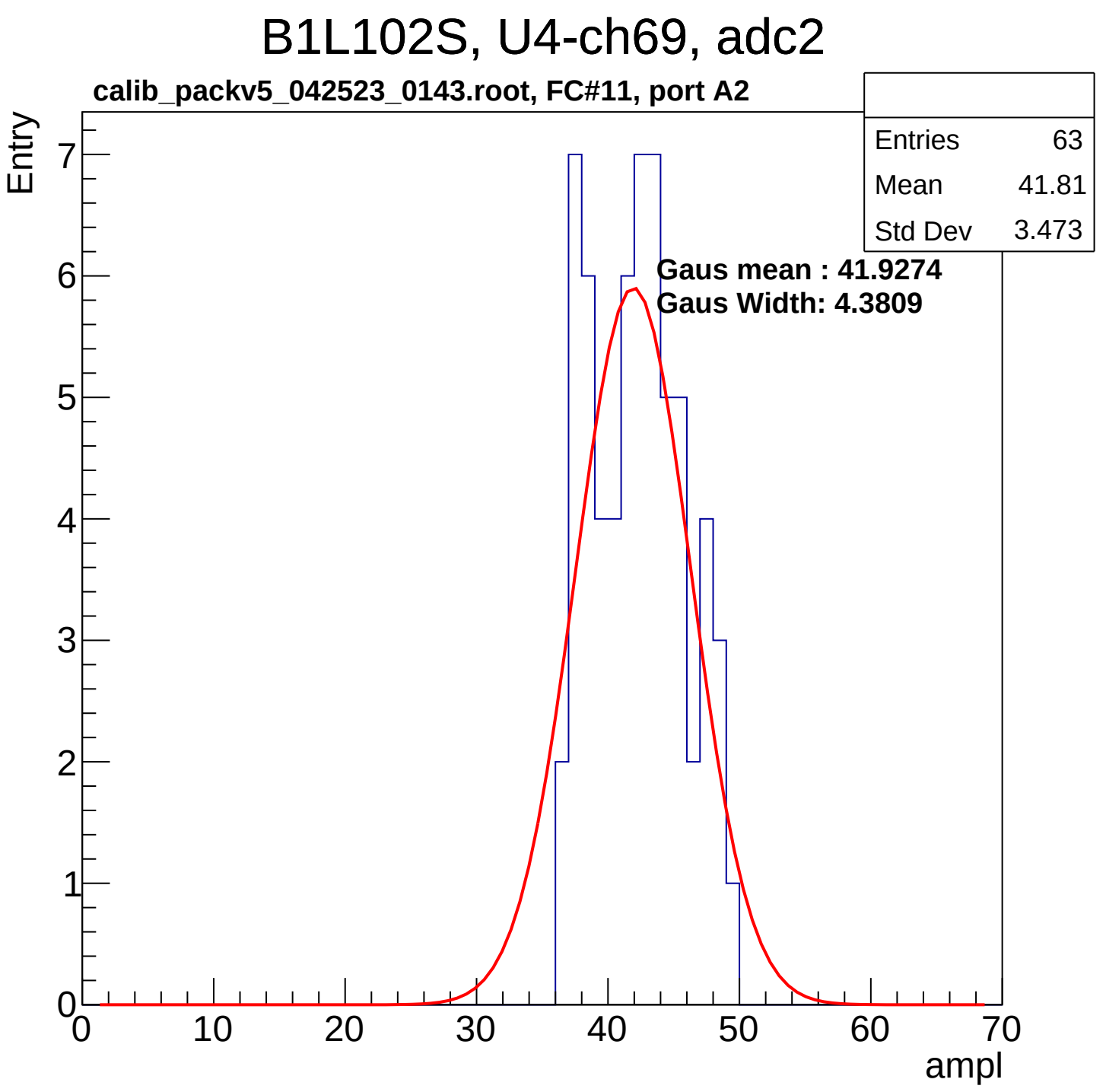

B1L102S, U4-ch69, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 27.43
Std Dev 5.402
Gaus mean : 27.7900
Gaus Width: 4.5644
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L102S, U4-ch69, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 34.15
Std Dev 3.439
Gaus mean : 33.6204
Gaus Width: 2.6830
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch69, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 41.81
Std Dev 3.473
Gaus mean : 41.9274
Gaus Width: 4.3809
Entry
ampl
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4
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7
0
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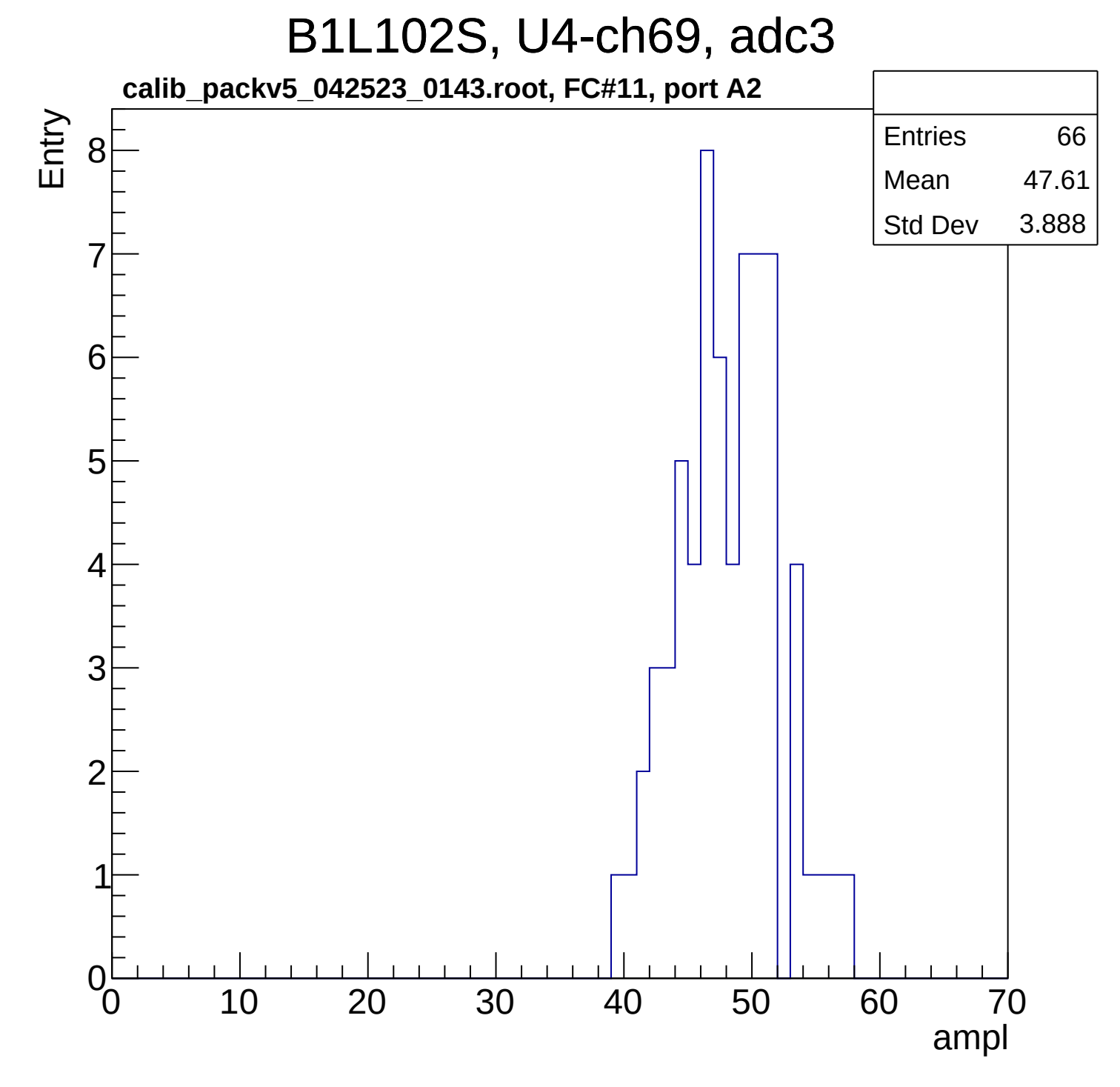
B1L102S, U4-ch69, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 47.61
Std Dev 3.888
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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60
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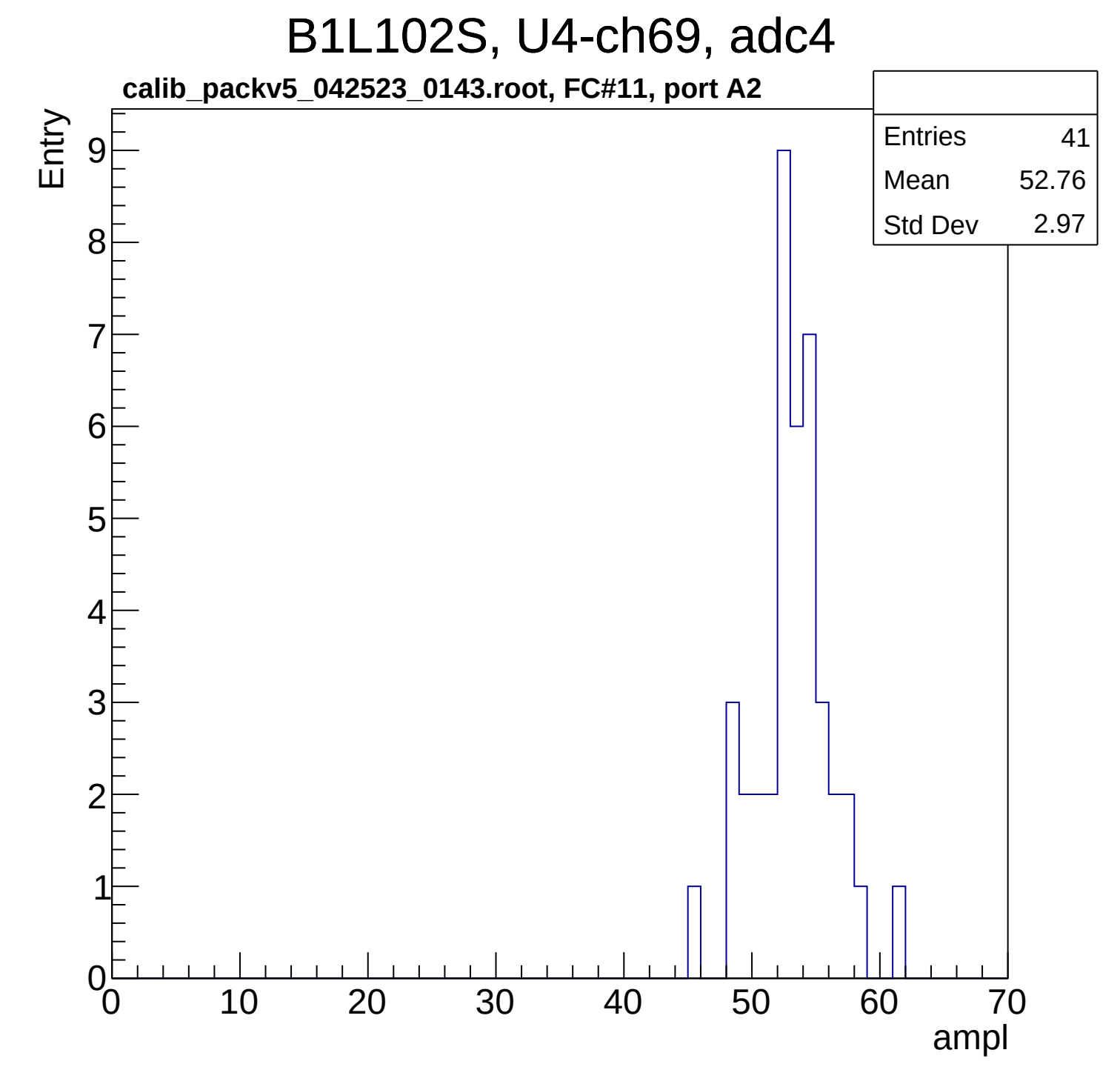
B1L102S, U4-ch69, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 41
Mean 52.76
Std Dev 2.97
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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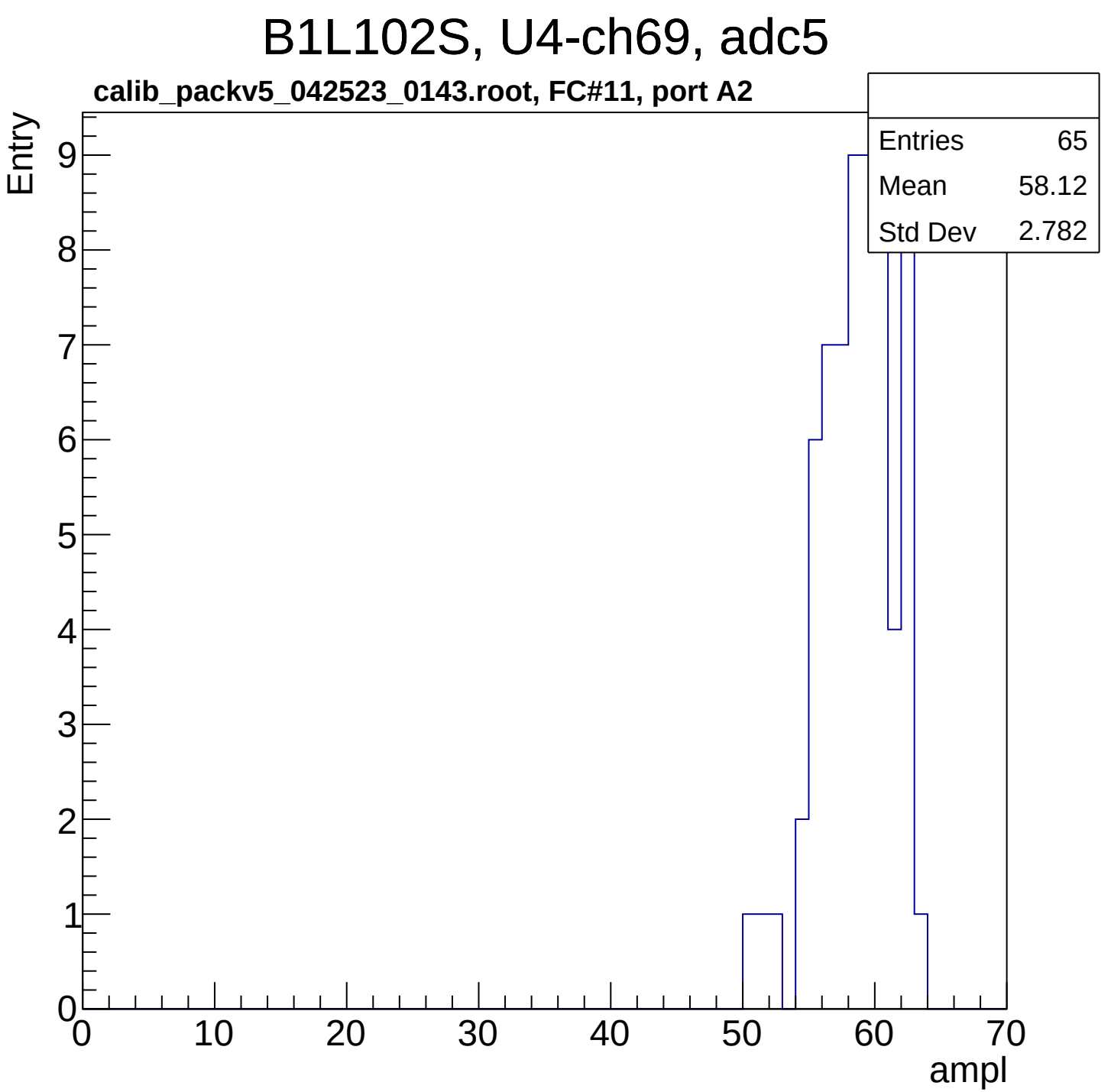
B1L102S, U4-ch69, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 58.12
Std Dev 2.782
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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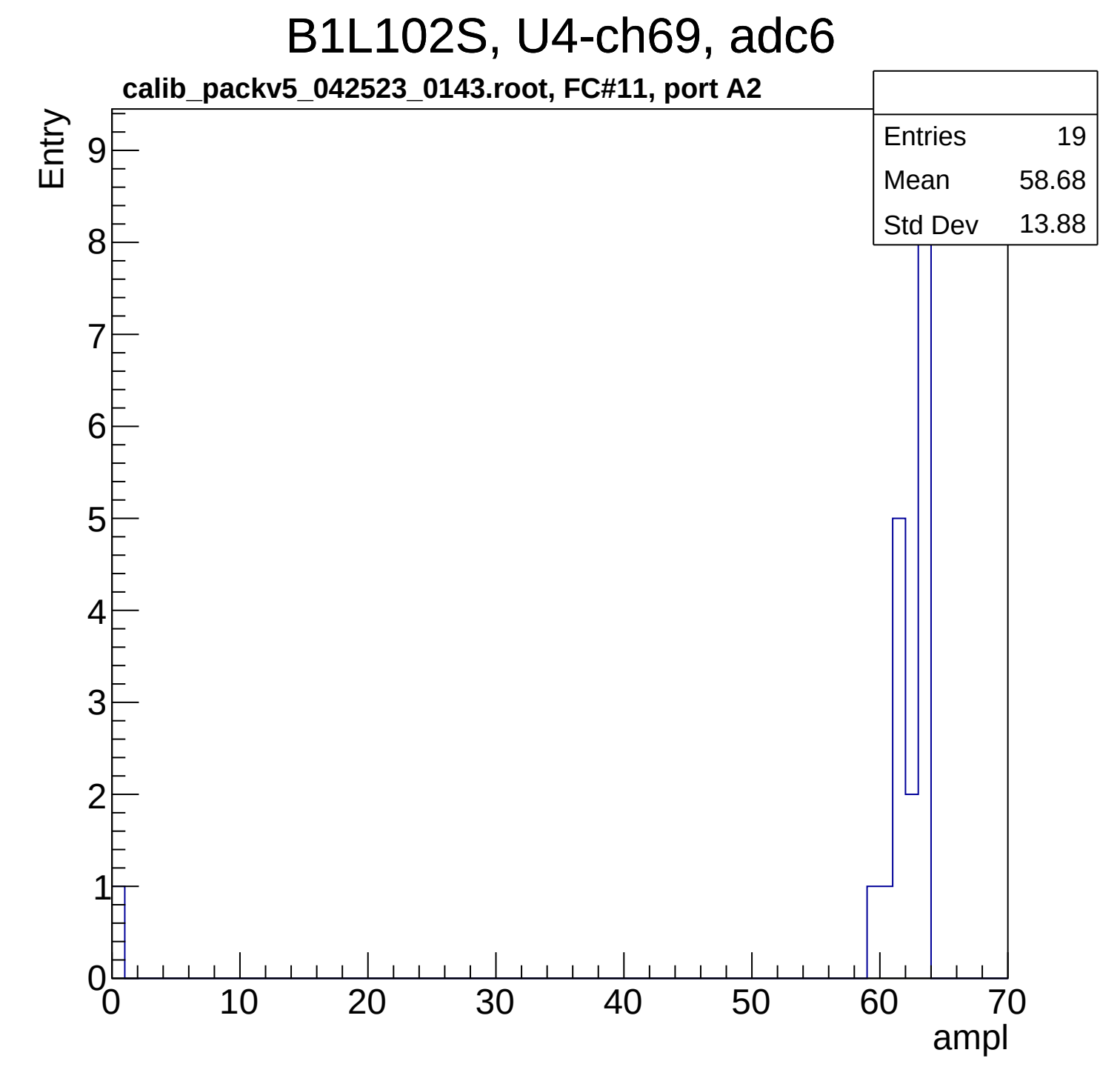
B1L102S, U4-ch69, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 19
Mean 58.68
Std Dev 13.88
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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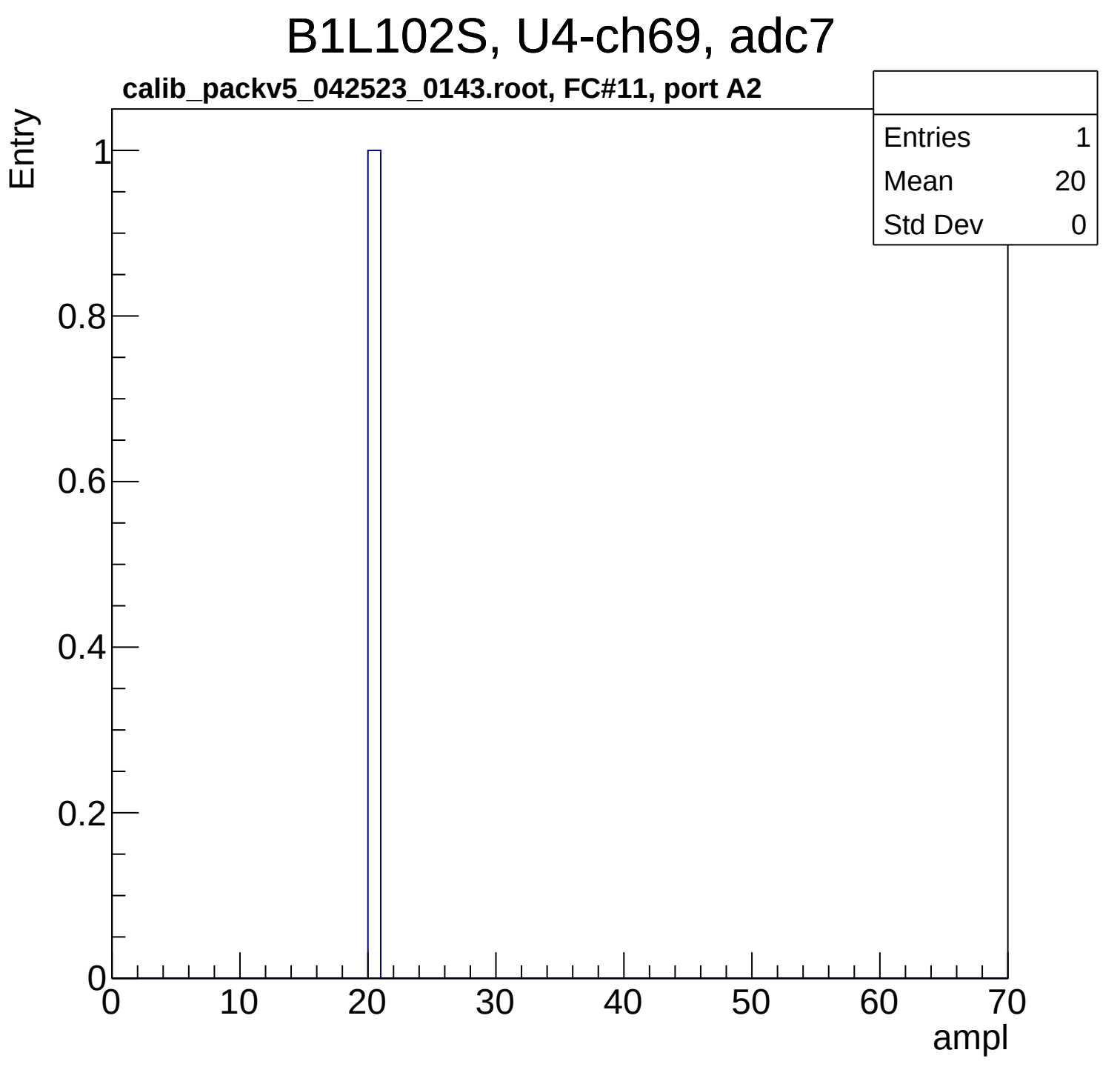
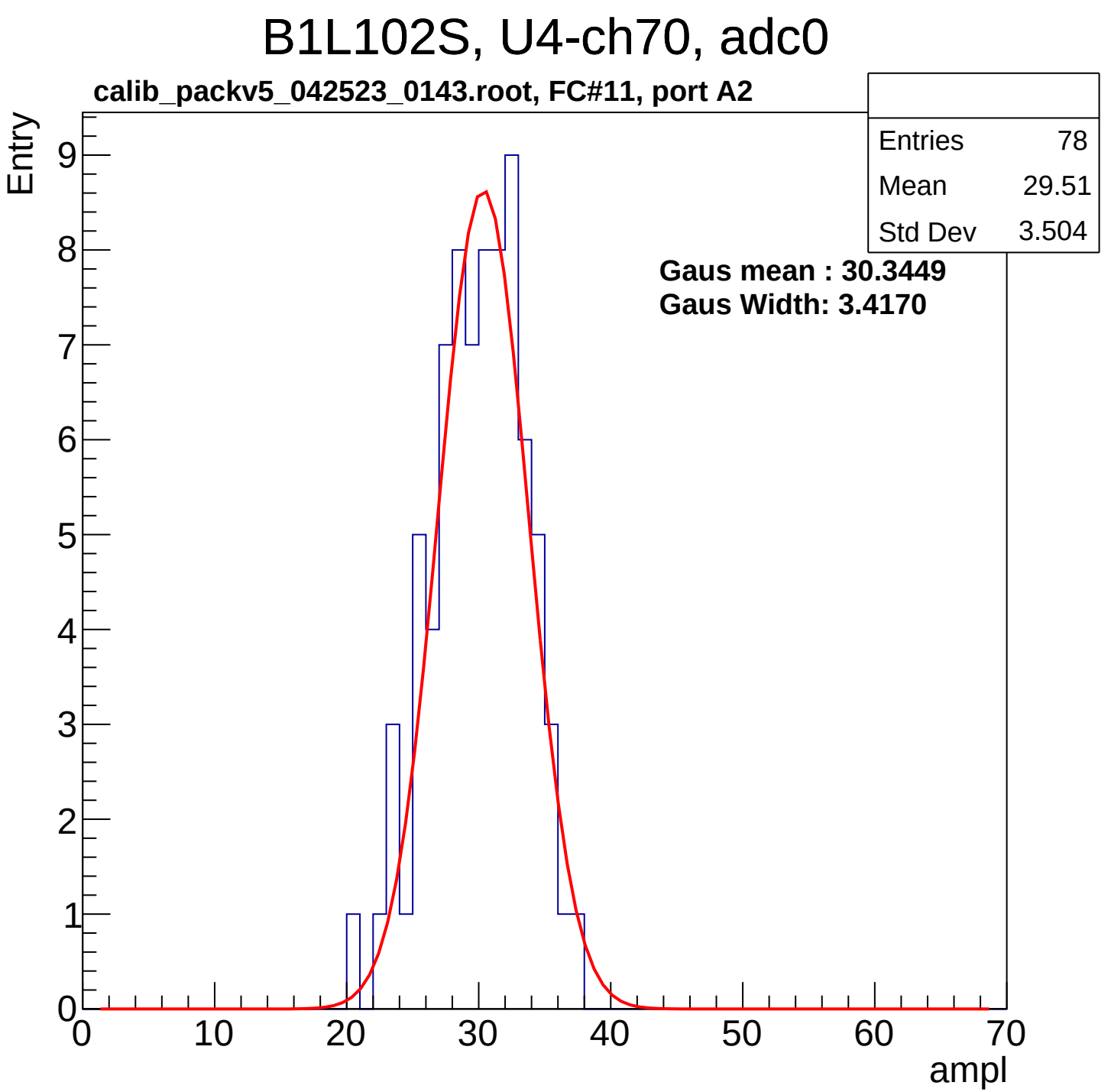
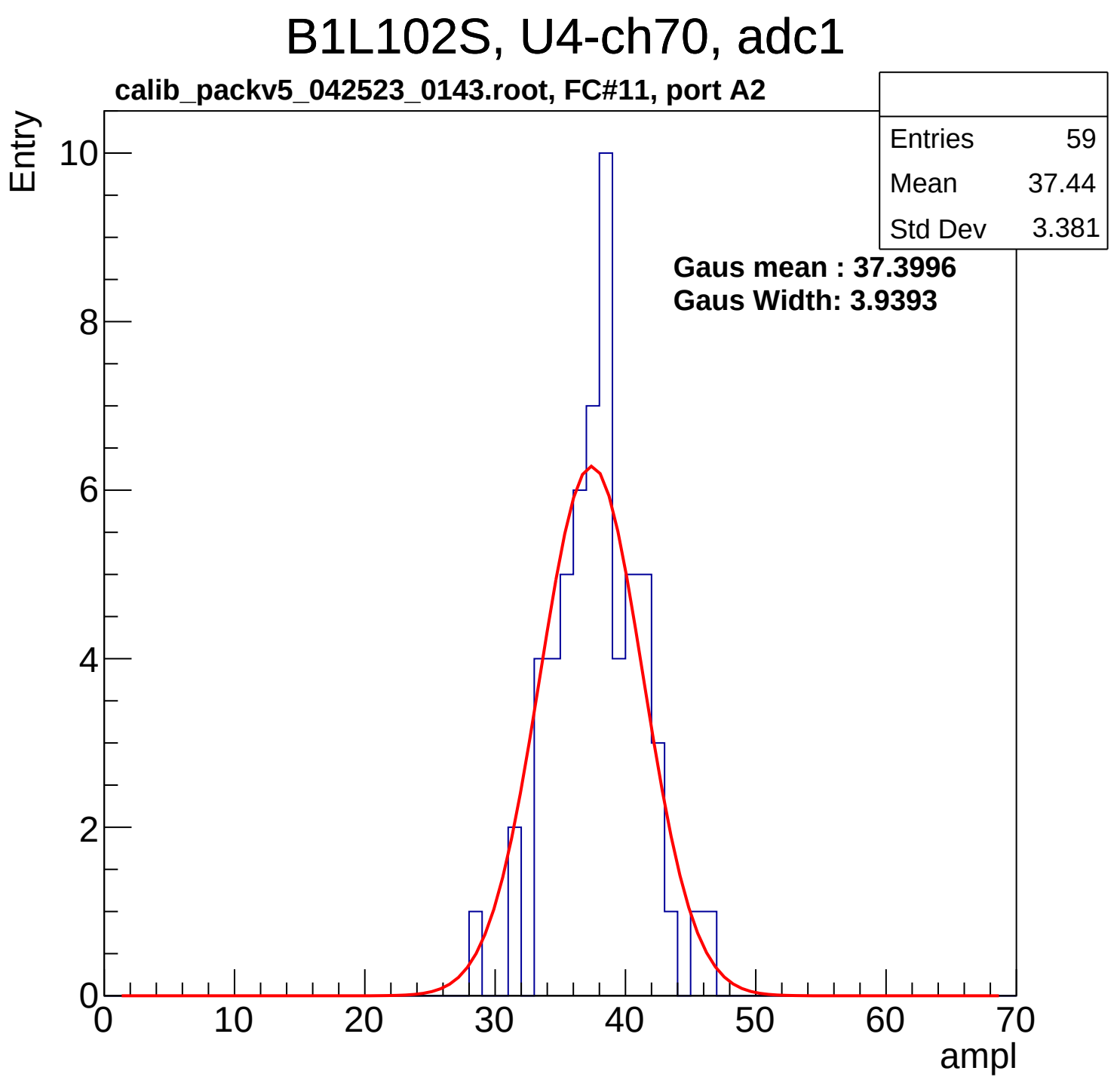
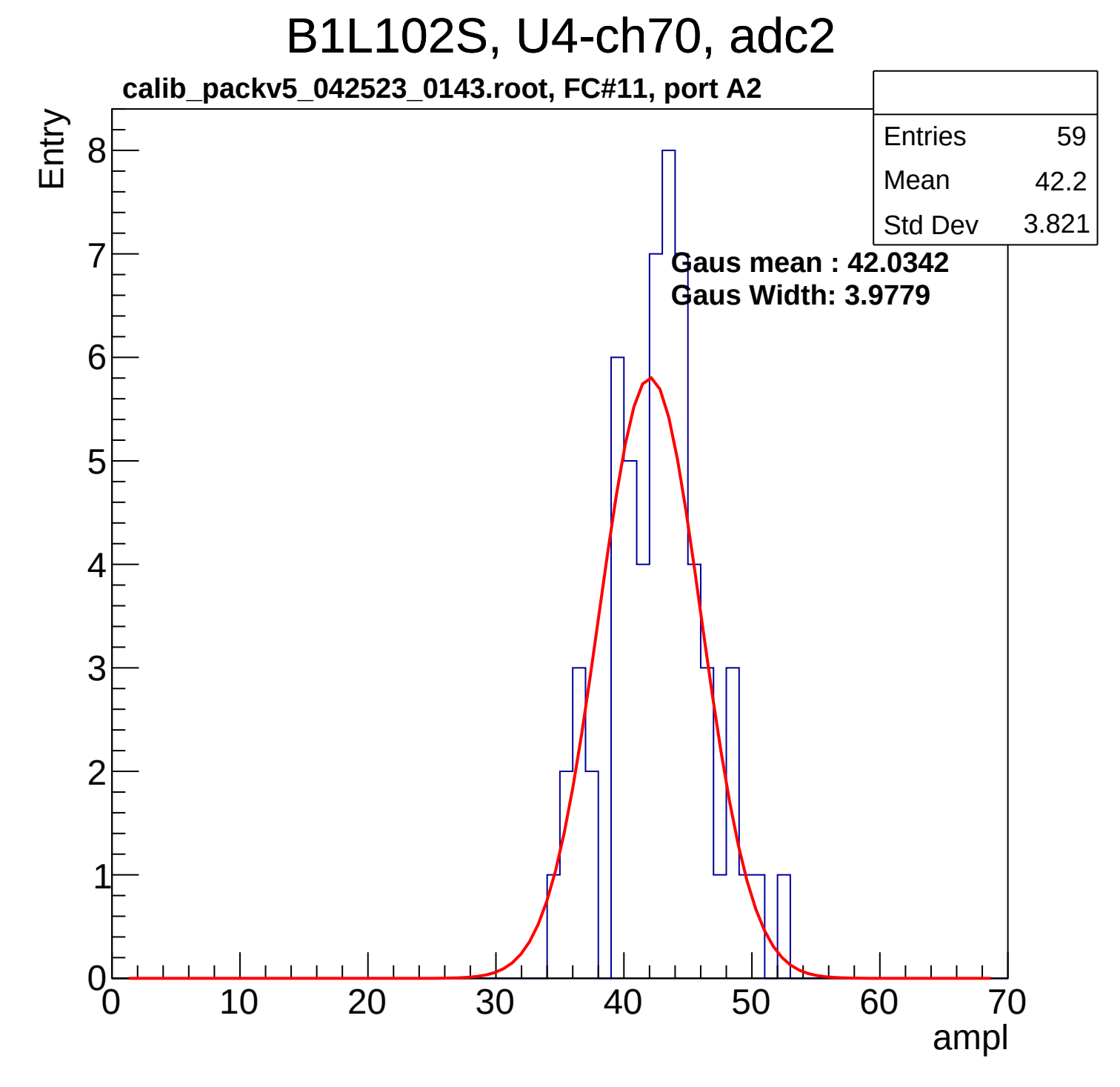

B1L102S, U4-ch69, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 20
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch70, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 78
Mean 29.51
Std Dev 3.504
Gaus mean : 30.3449
Gaus Width: 3.4170
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch70, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 37.44
Std Dev 3.381
Gaus mean : 37.3996
Gaus Width: 3.9393
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch70, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 42.2
Std Dev 3.821
Gaus mean : 42.0342
Gaus Width: 3.9779
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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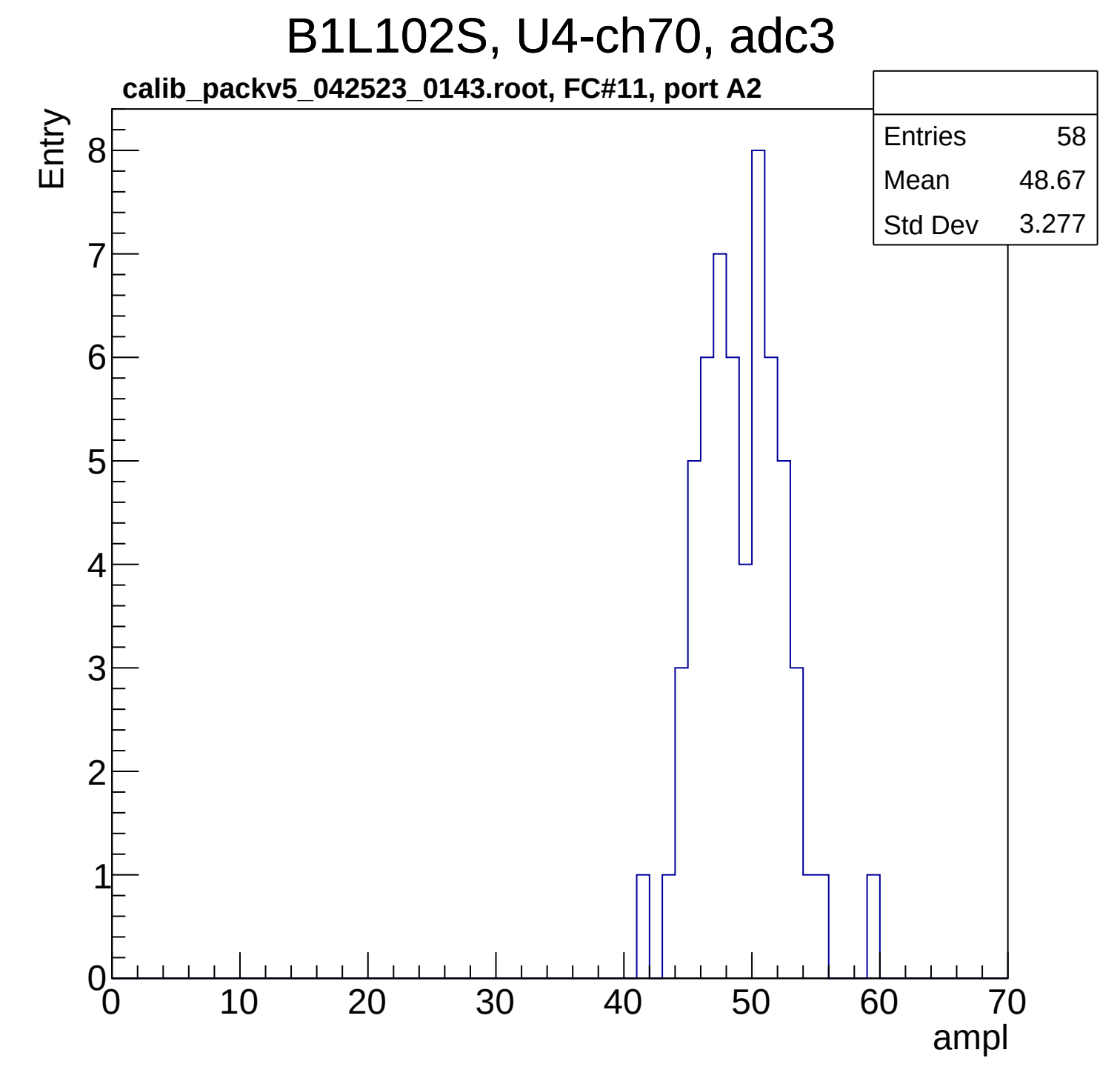
B1L102S, U4-ch70, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 48.67
Std Dev 3.277
Entry
ampl
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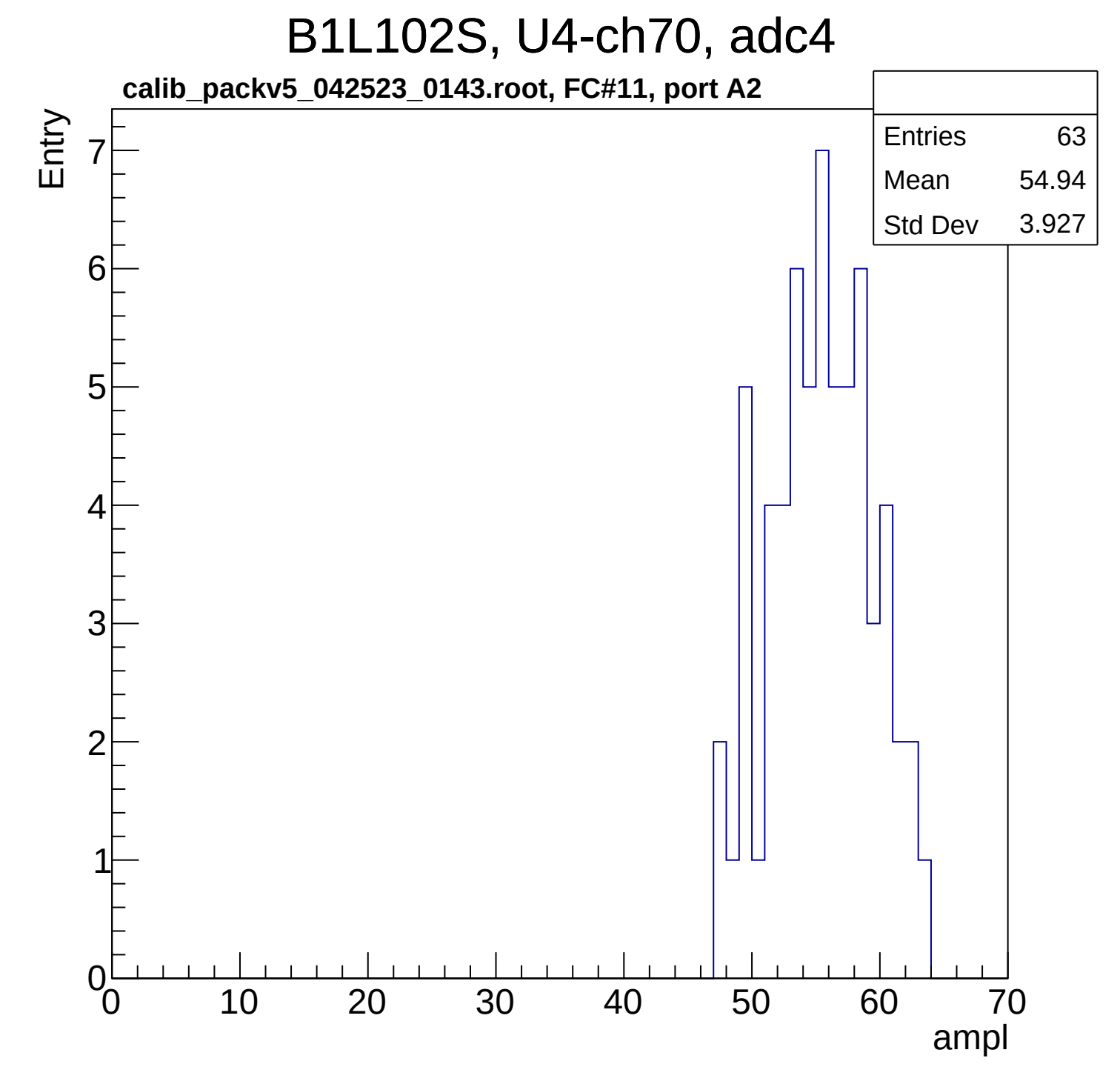
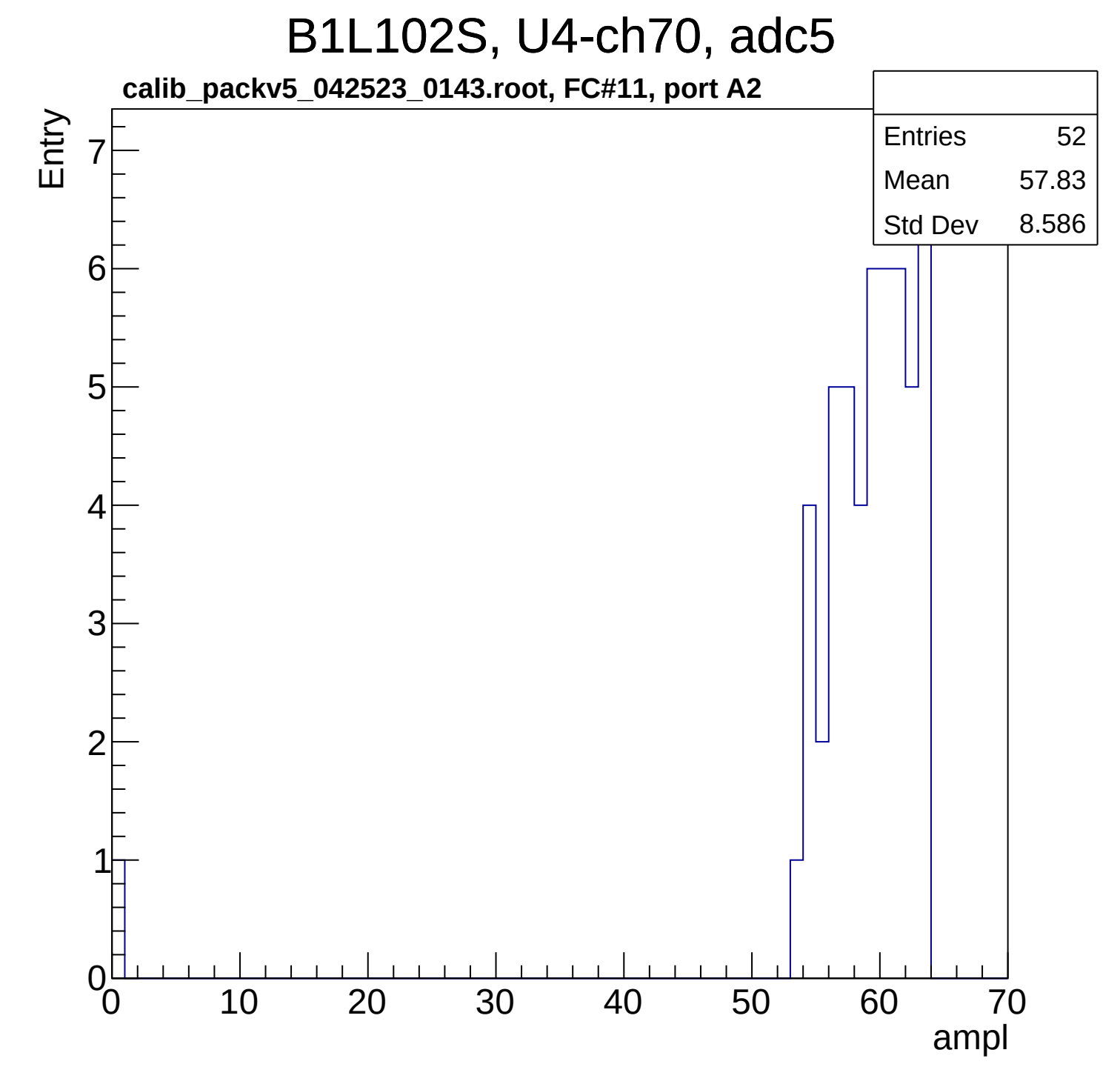
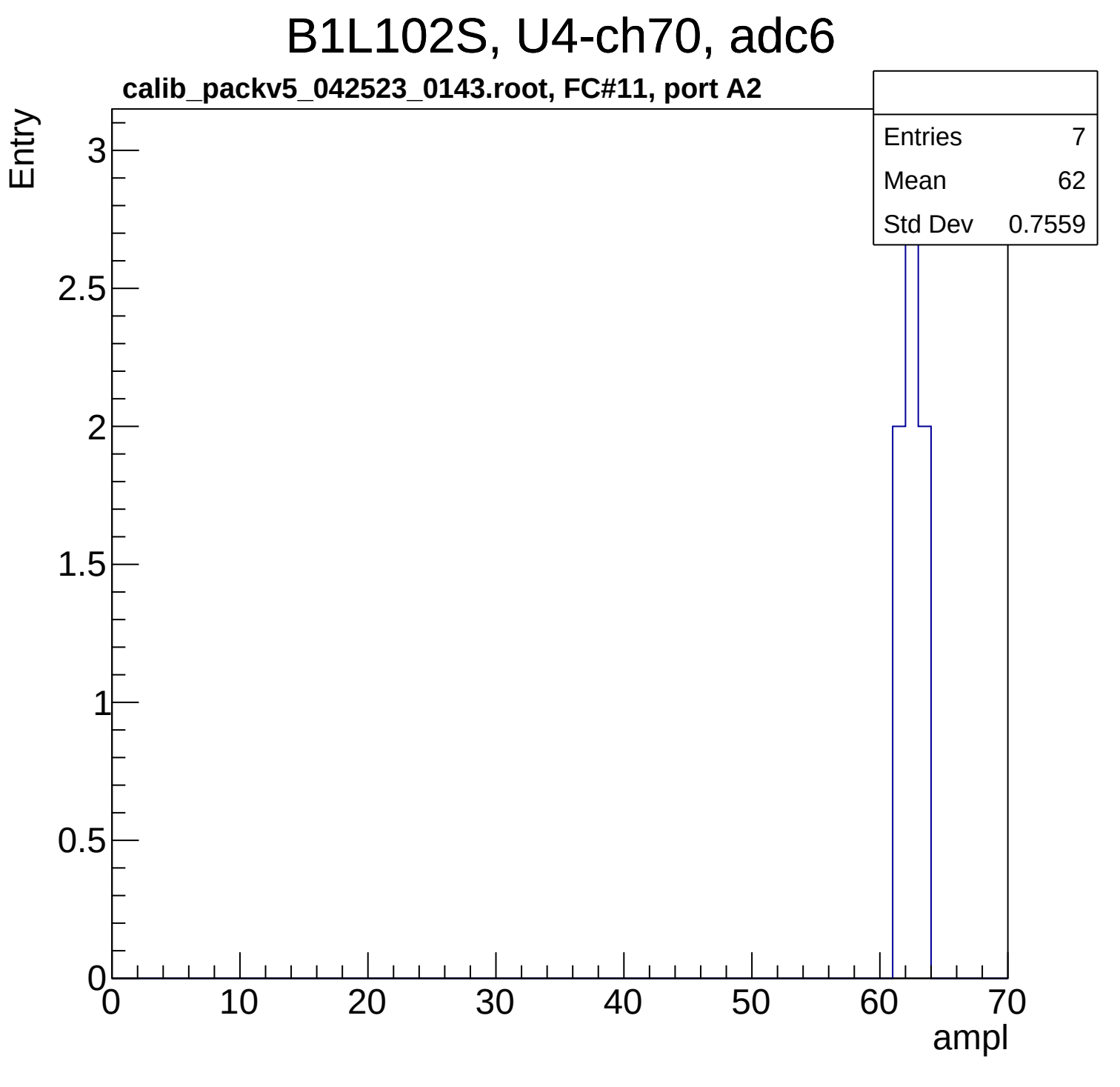
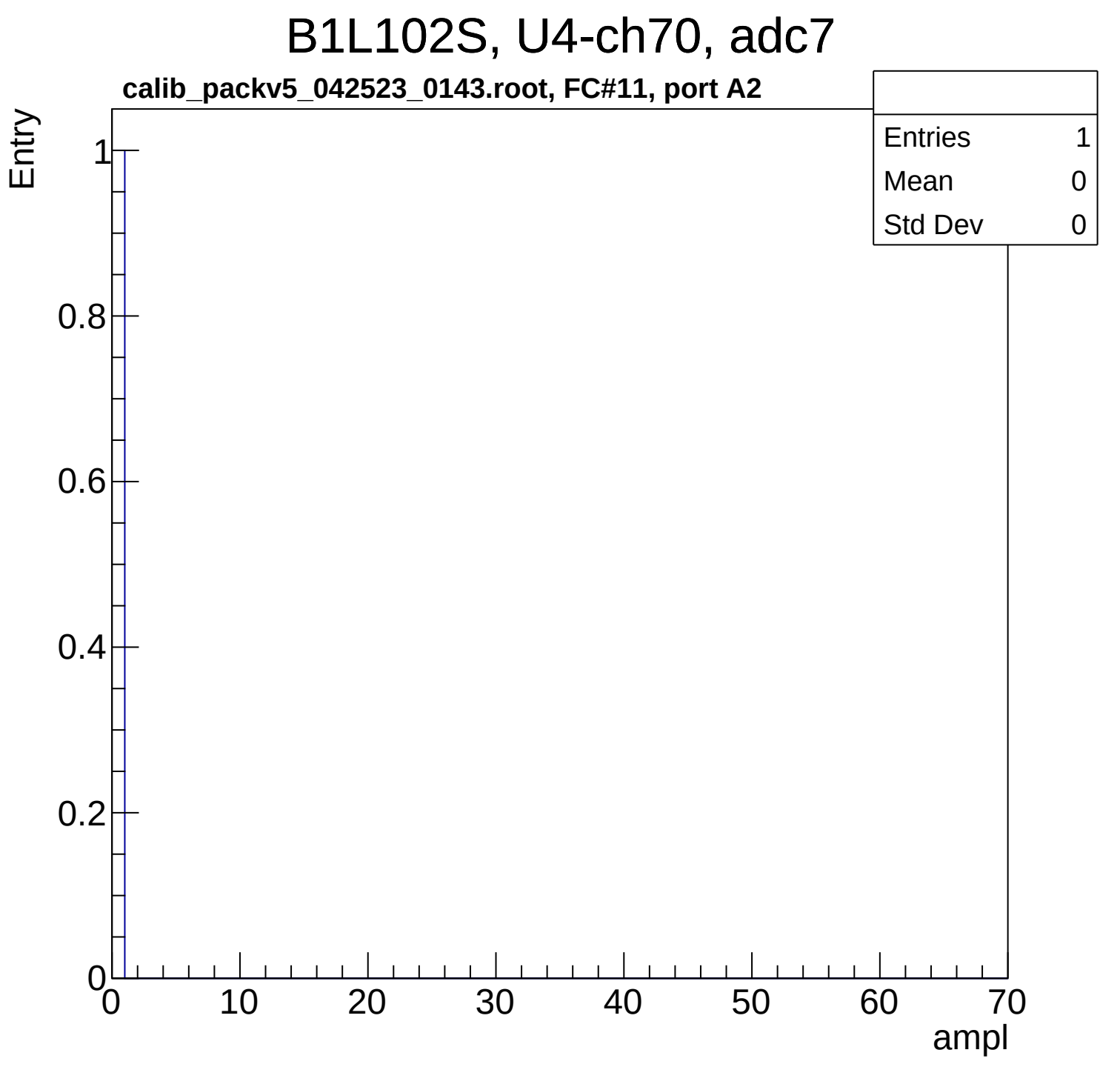
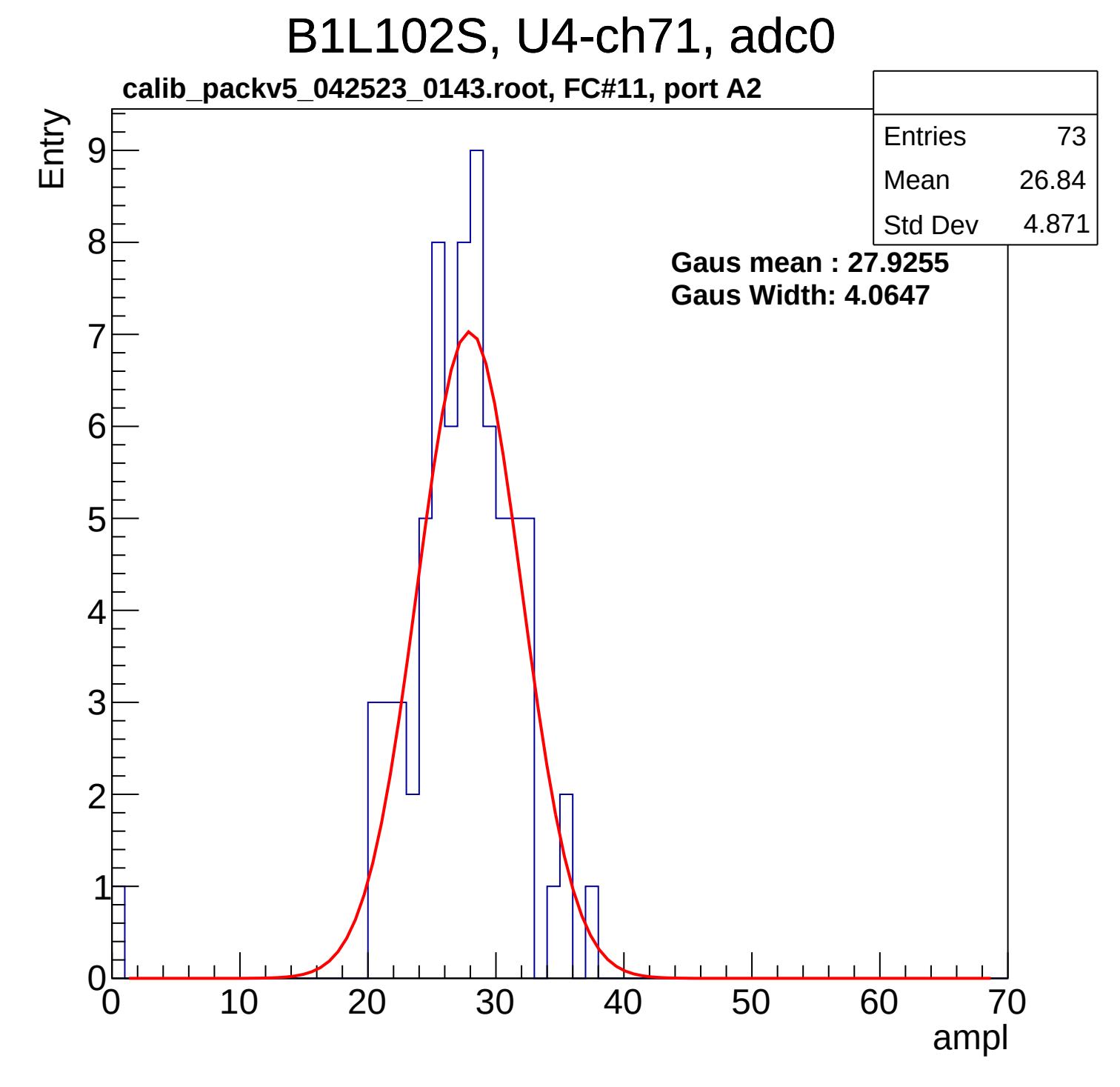
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

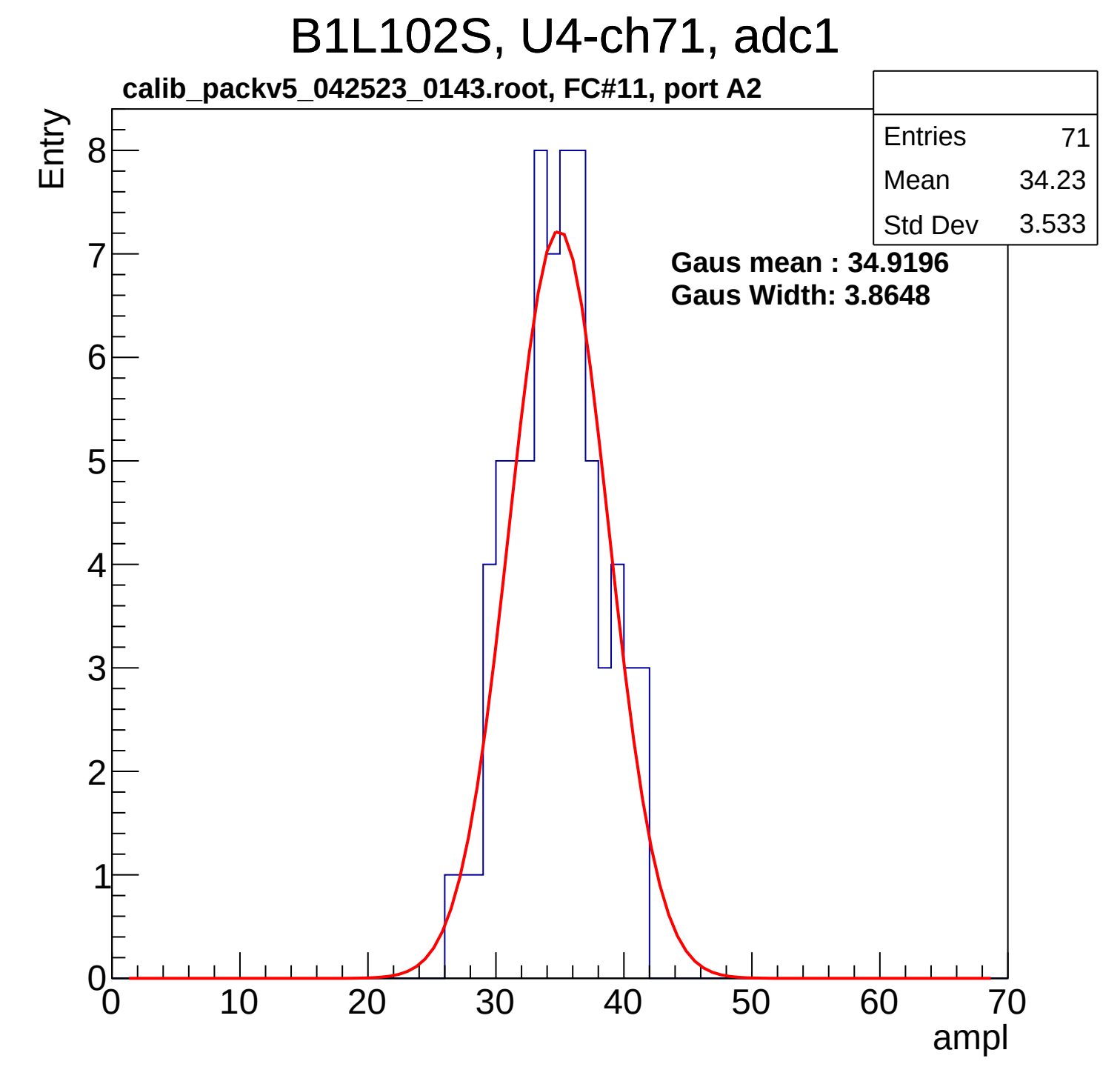

B1L102S, U4-ch70, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 54.94
Std Dev 3.927
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

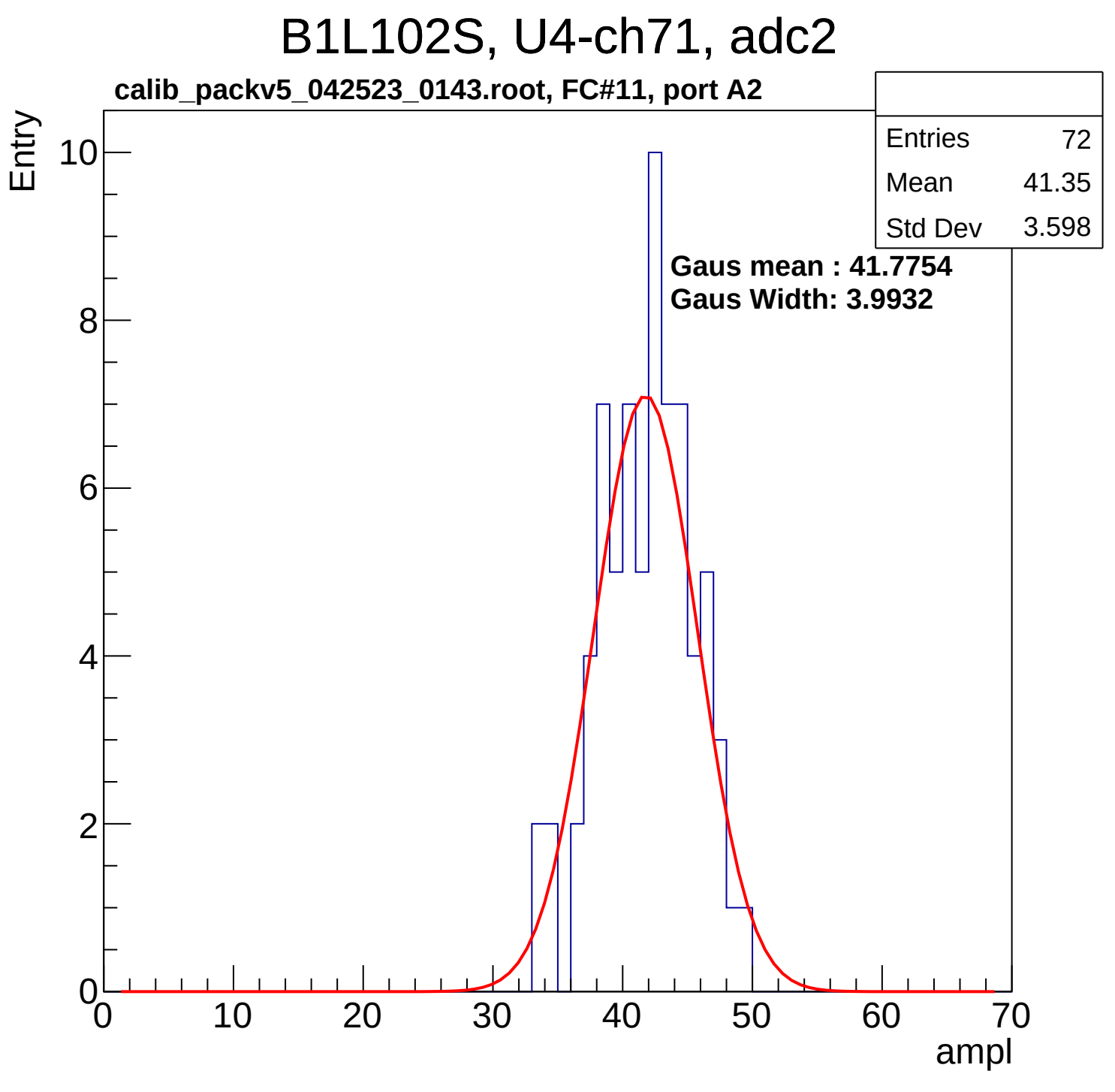

B1L102S, U4-ch70, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 52
Mean 57.83
Std Dev 8.586
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

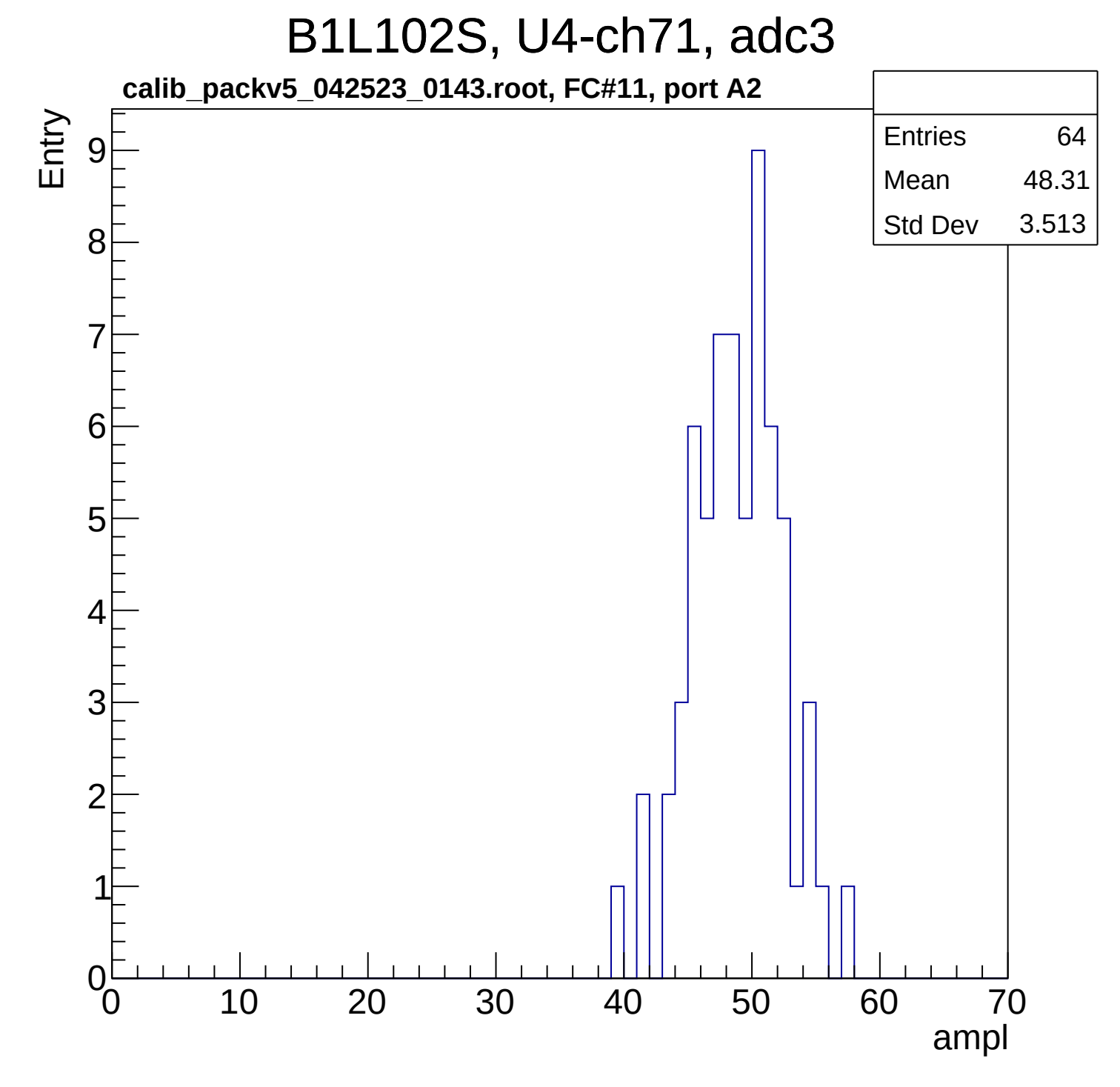

B1L102S, U4-ch70, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 7
Mean 62
Std Dev 0.7559
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U4-ch70, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch71, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 26.84
Std Dev 4.871
Gaus mean : 27.9255
Gaus Width: 4.0647
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch71, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 34.23
Std Dev 3.533
Gaus mean : 34.9196
Gaus Width: 3.8648
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch71, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 72
Mean 41.35
Std Dev 3.598
Gaus mean : 41.7754
Gaus Width: 3.9932
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch71, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 48.31
Std Dev 3.513
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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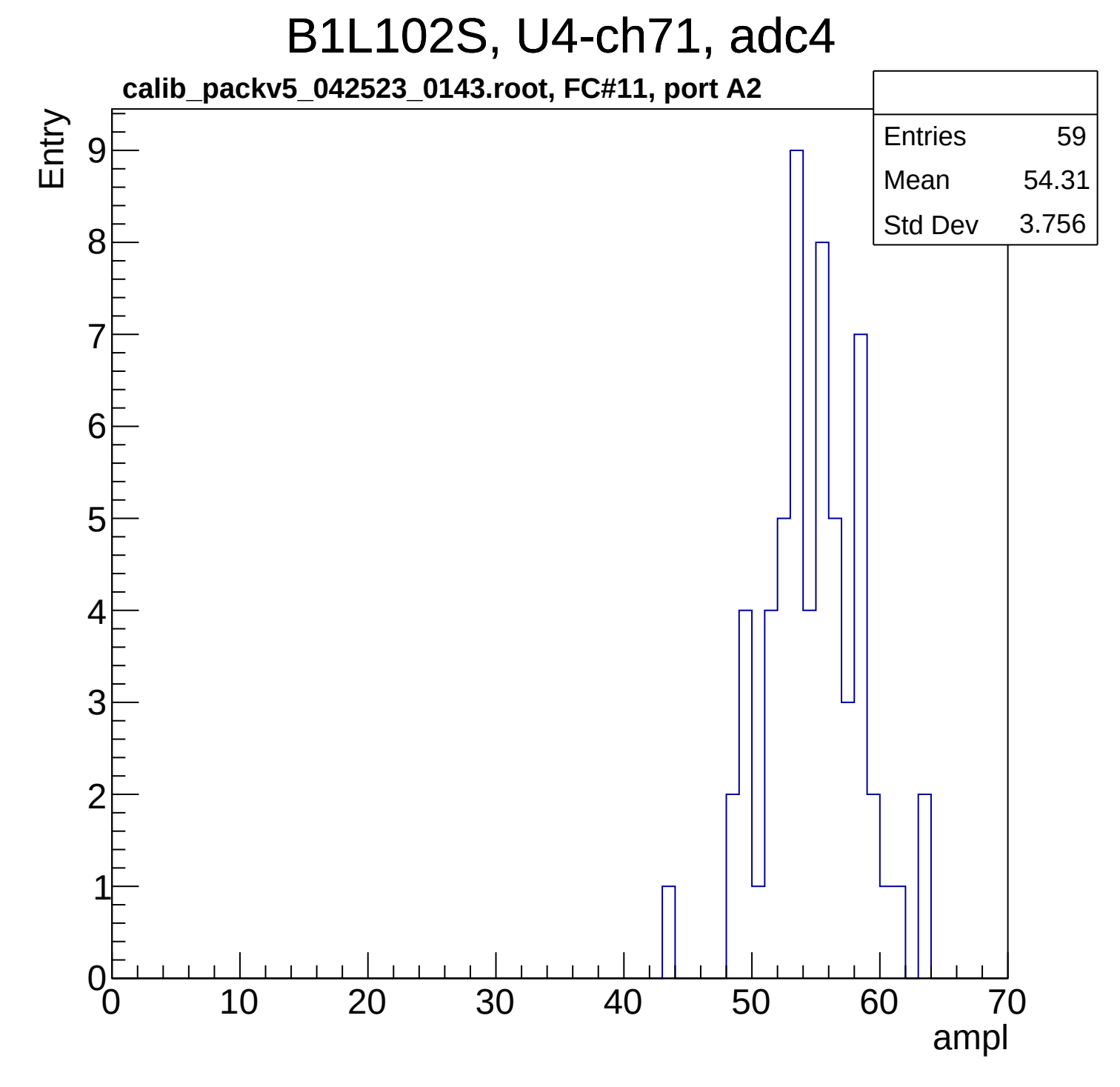
B1L102S, U4-ch71, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 54.31
Std Dev 3.756
Entry
ampl
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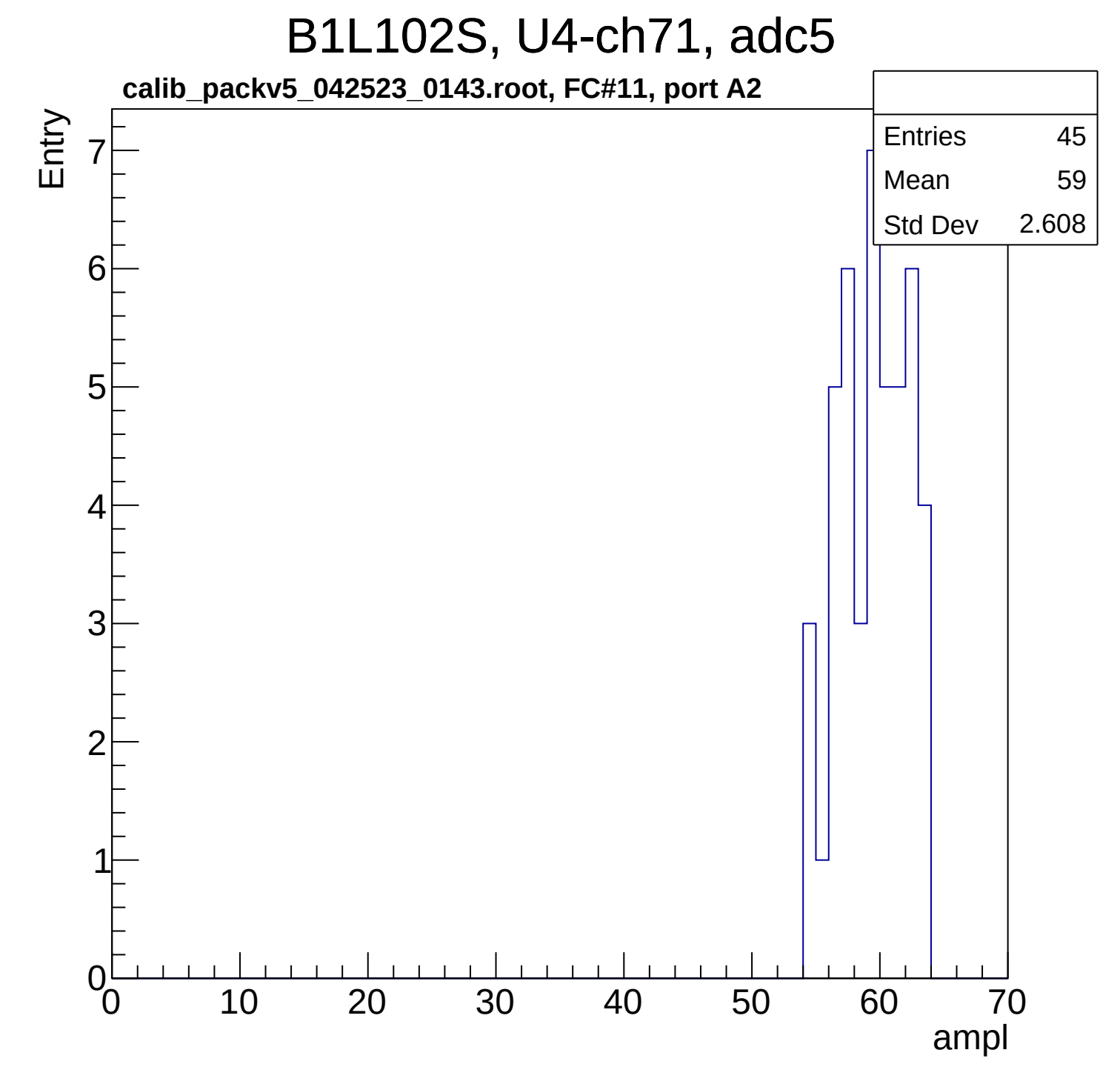
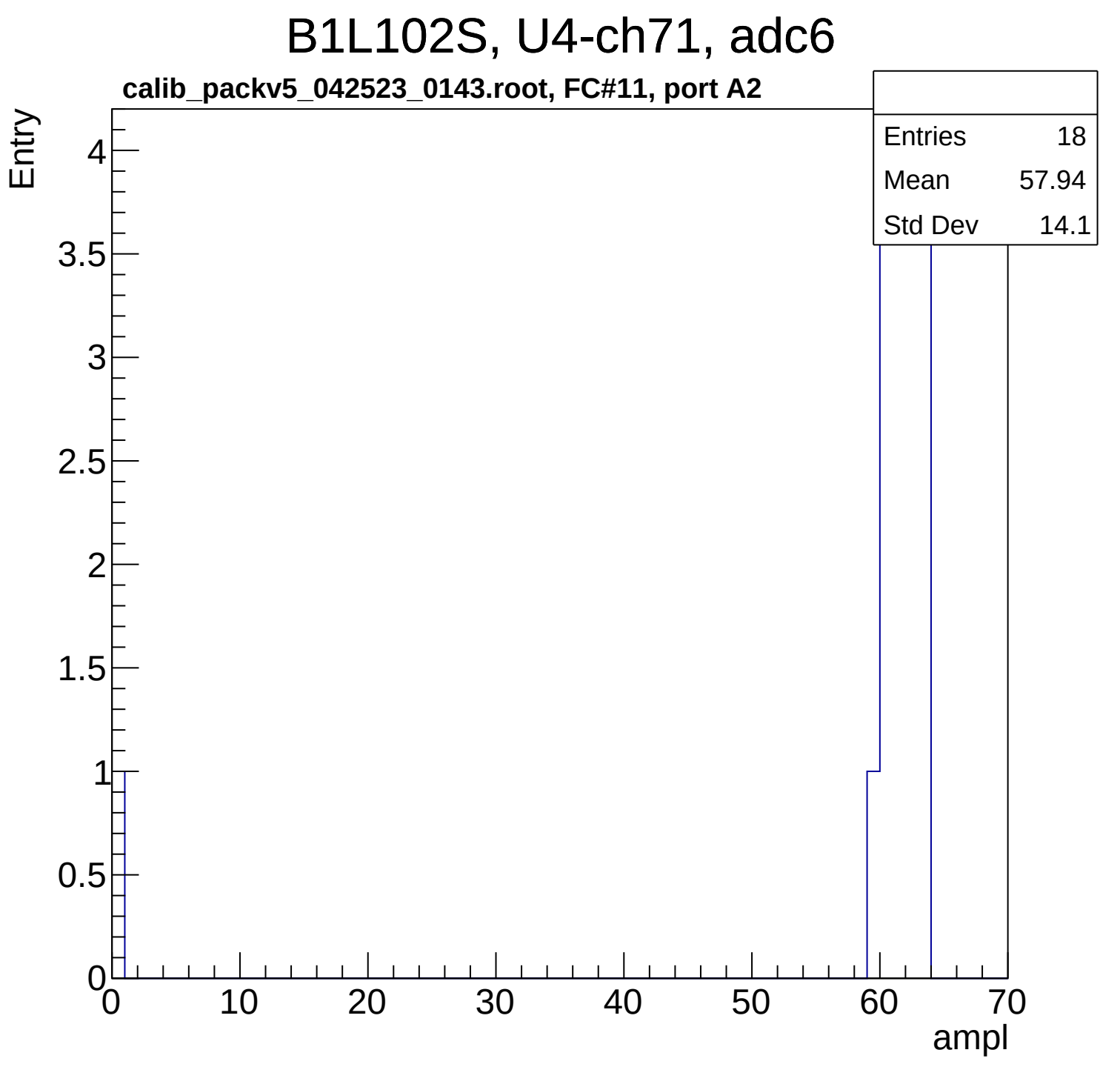
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch71, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 45
Mean 59
Std Dev 2.608
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch71, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 18
Mean 57.94
Std Dev 14.1
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
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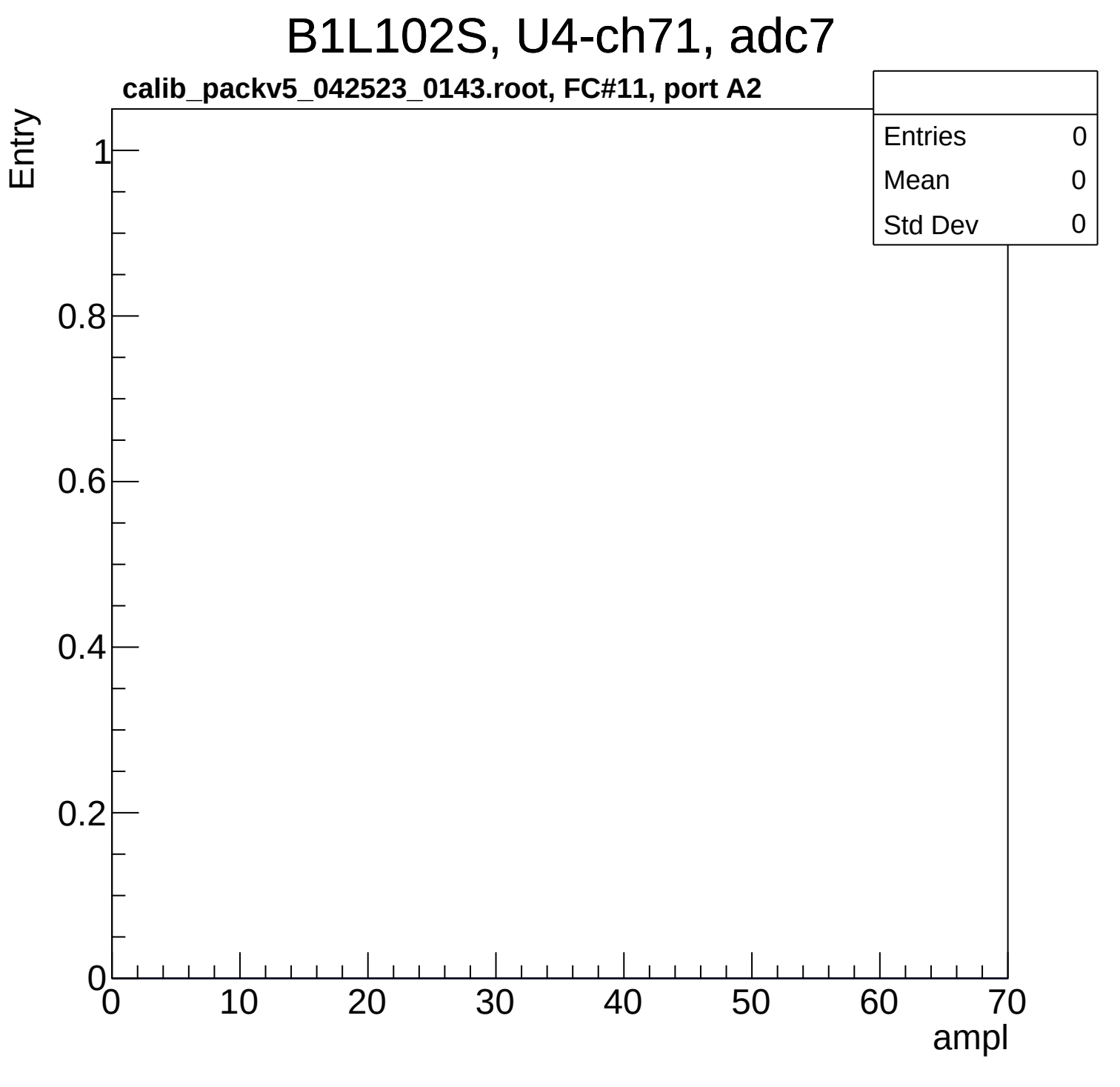
20
30
40
50
60
70


B1L102S, U4-ch71, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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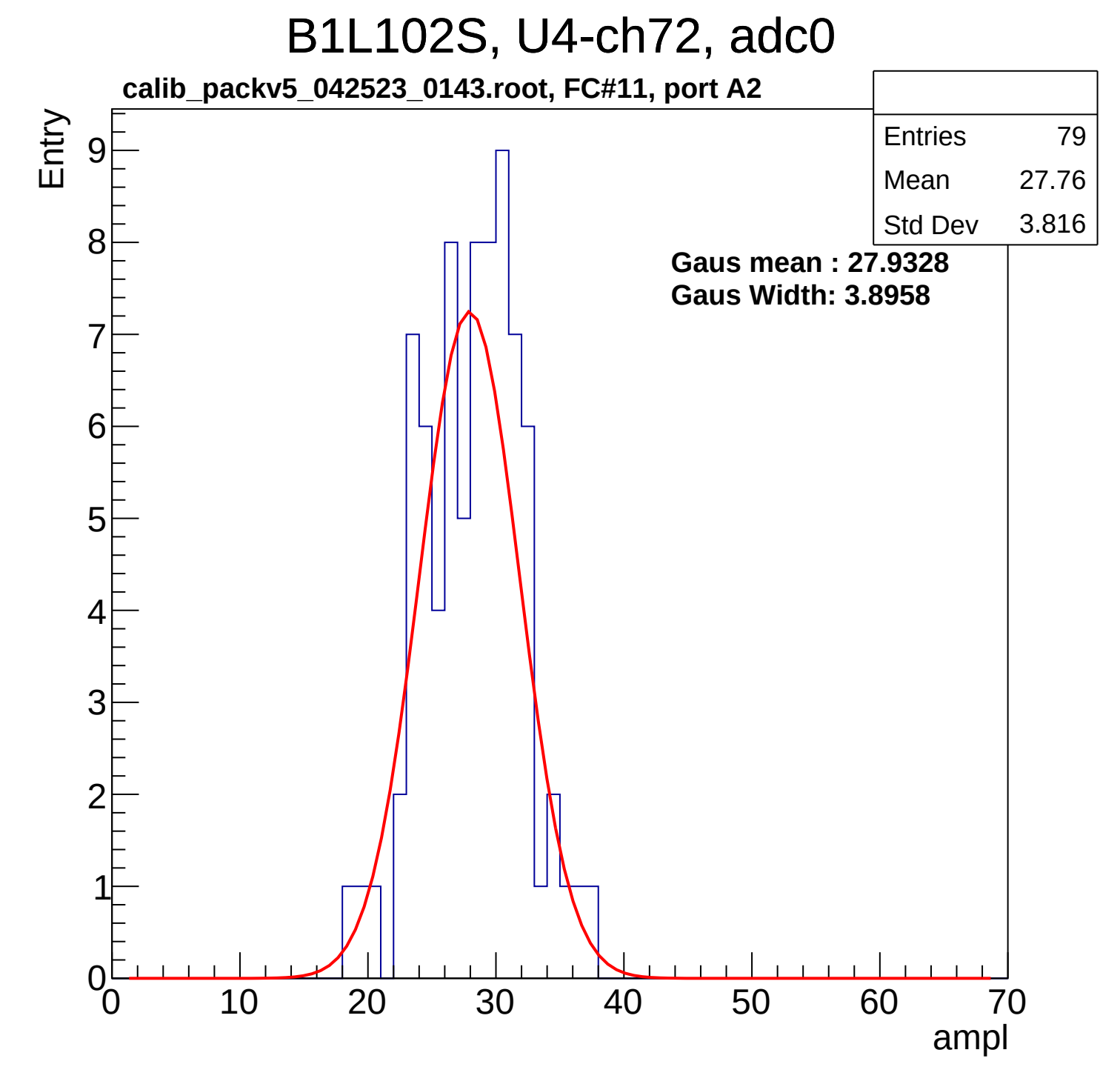
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch72, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 79
Mean 27.76
Std Dev 3.816
Gaus mean : 27.9328
Gaus Width: 3.8958
Entry
ampl
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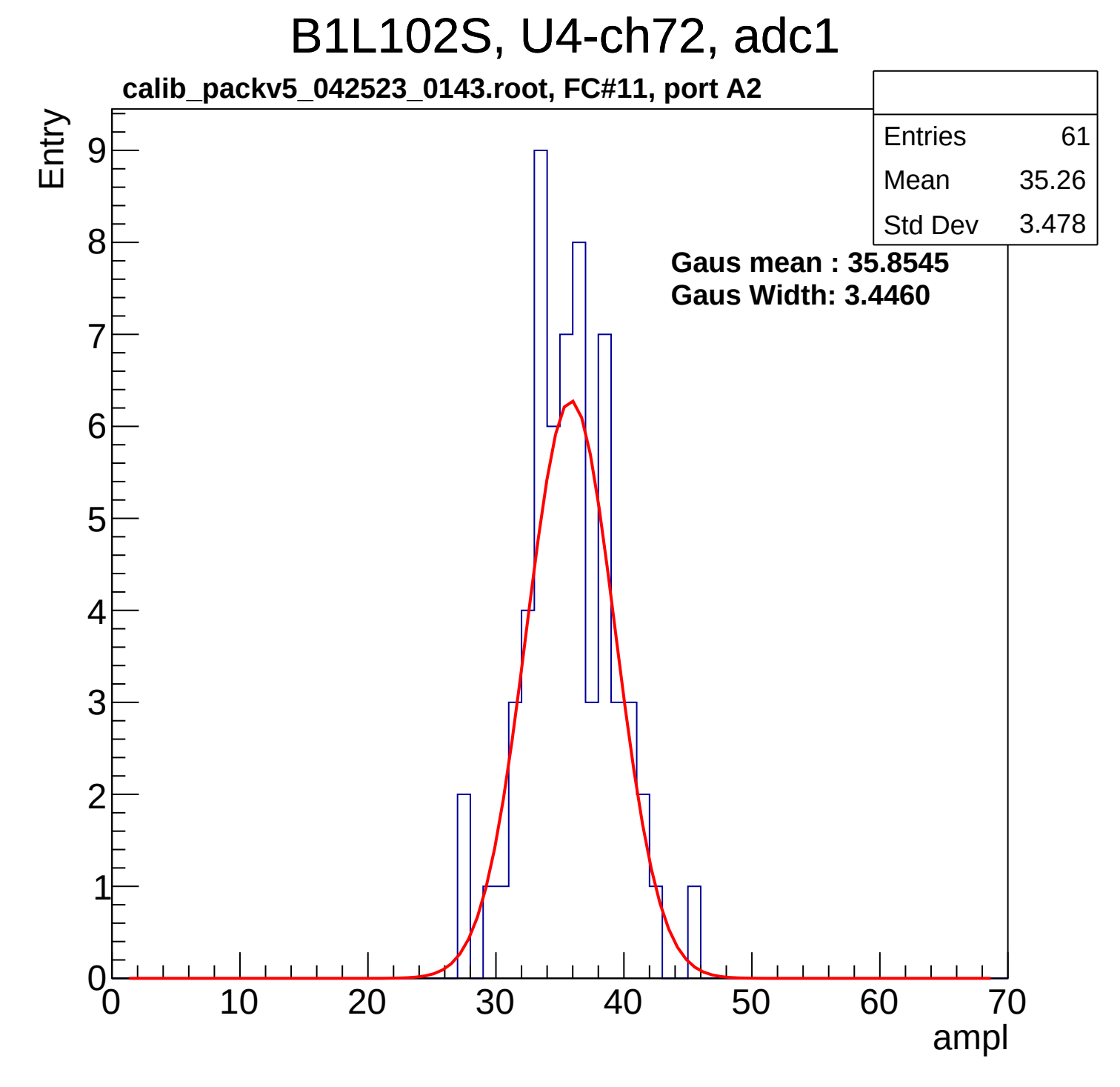
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch72, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 35.26
Std Dev 3.478
Gaus mean : 35.8545
Gaus Width: 3.4460
Entry
ampl
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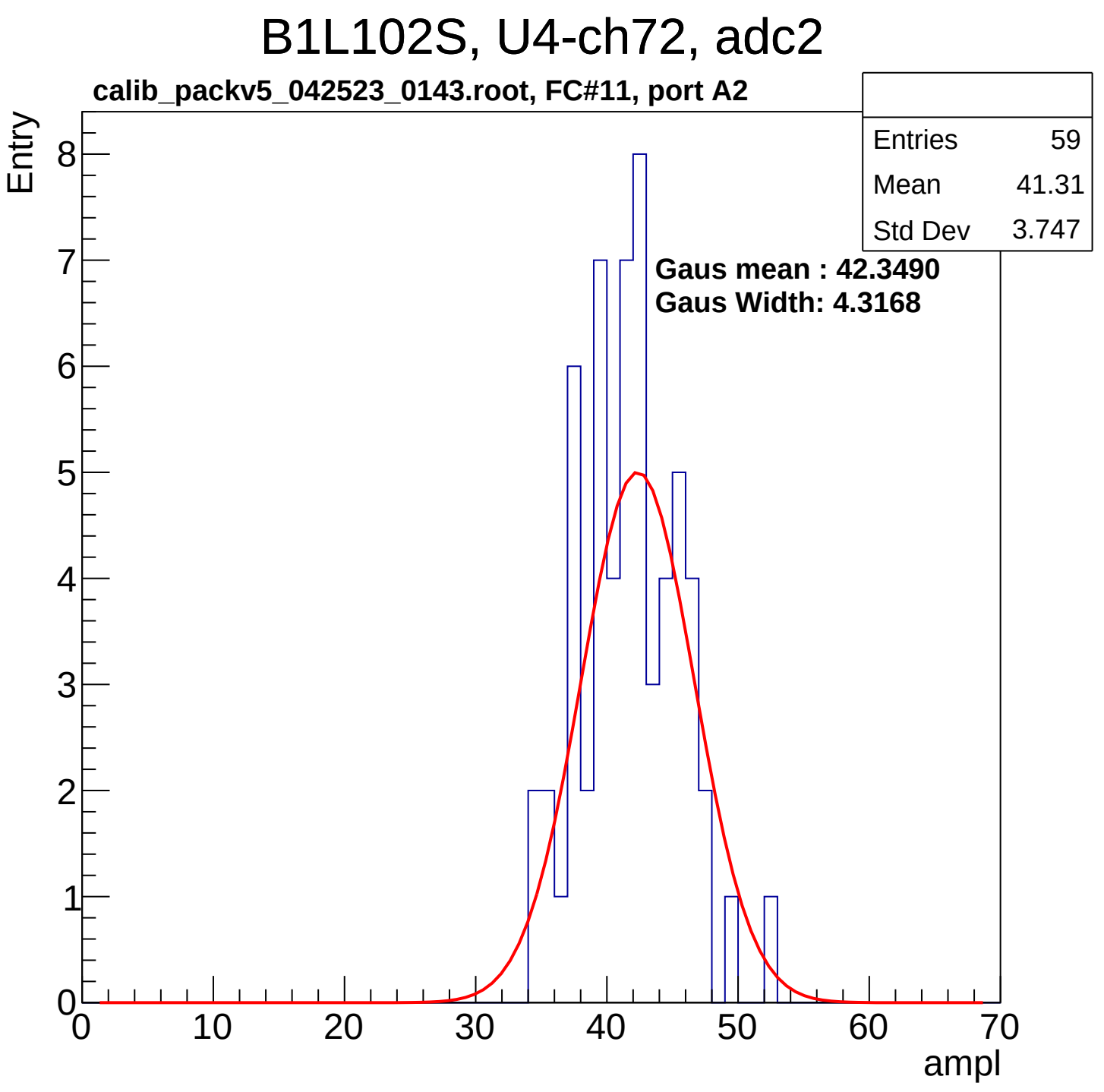
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch72, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 41.31
Std Dev 3.747
Gaus mean : 42.3490
Gaus Width: 4.3168
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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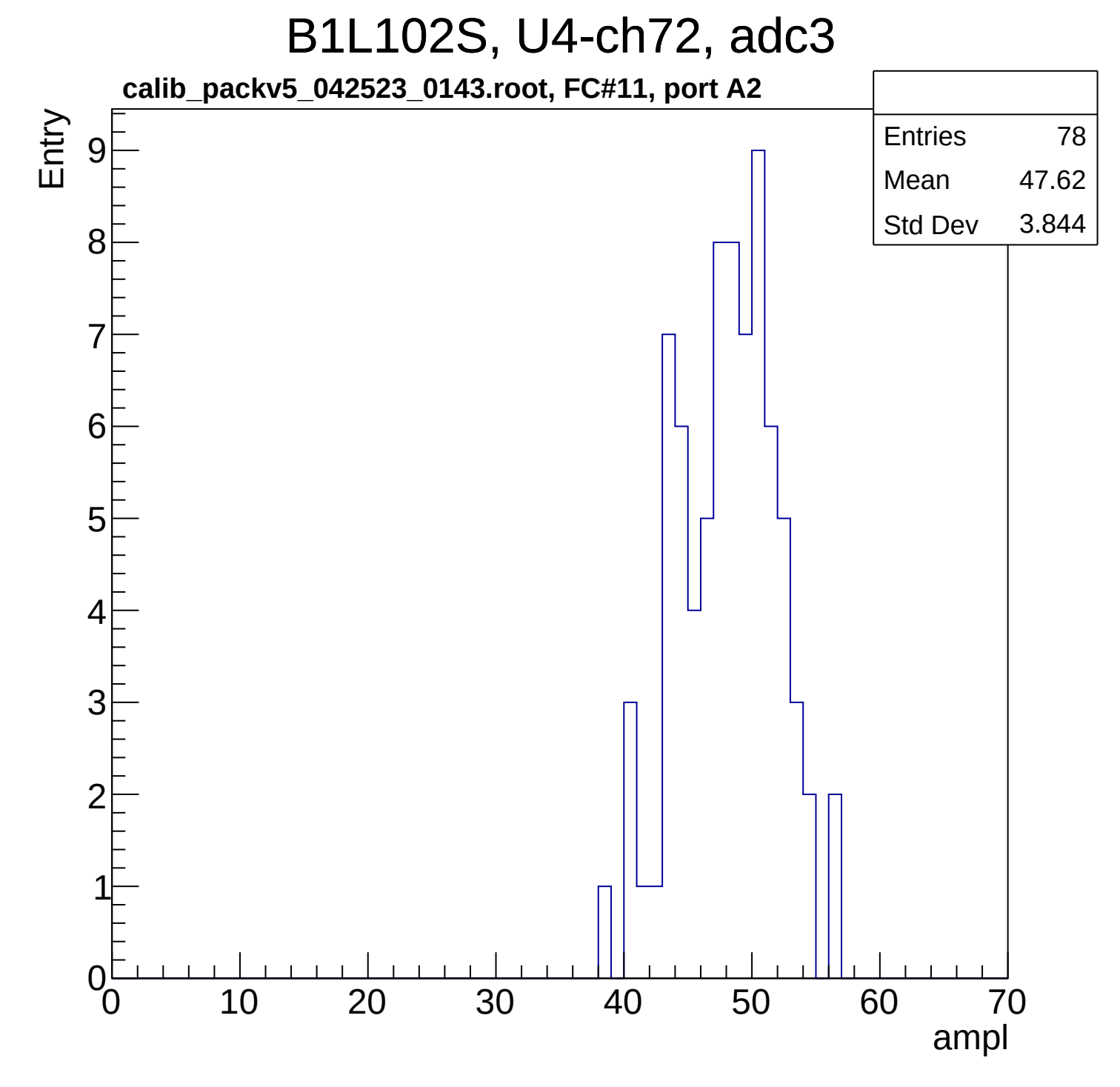
40
50
60
70


B1L102S, U4-ch72, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 78
Mean 47.62
Std Dev 3.844
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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60
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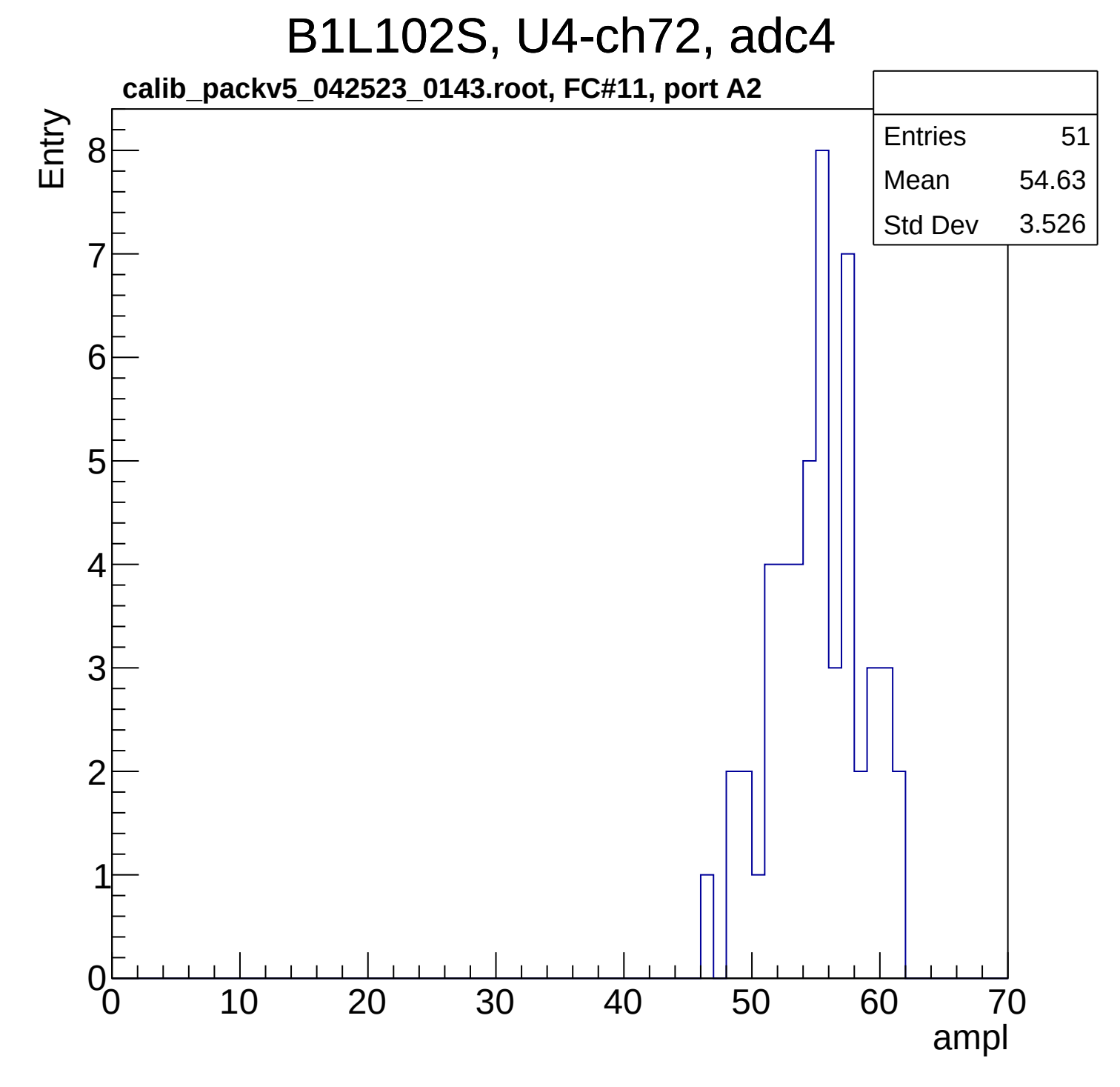
B1L102S, U4-ch72, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 54.63
Std Dev 3.526
Entry
ampl
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2
3
4
5
6
7
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0
10
20
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40
50
60
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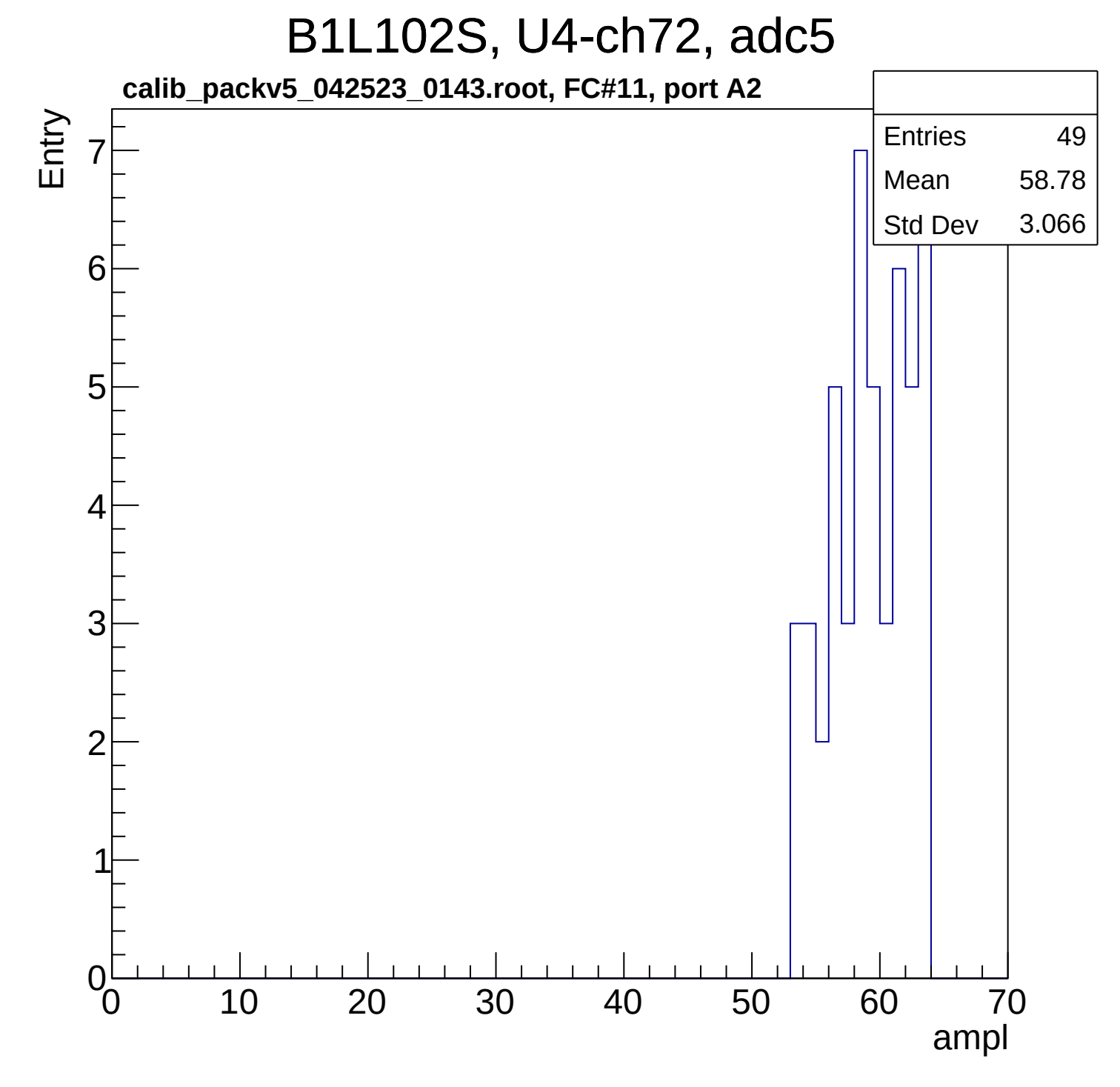
B1L102S, U4-ch72, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 58.78
Std Dev 3.066
Entry
ampl
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4
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6
7
0
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40
50
60
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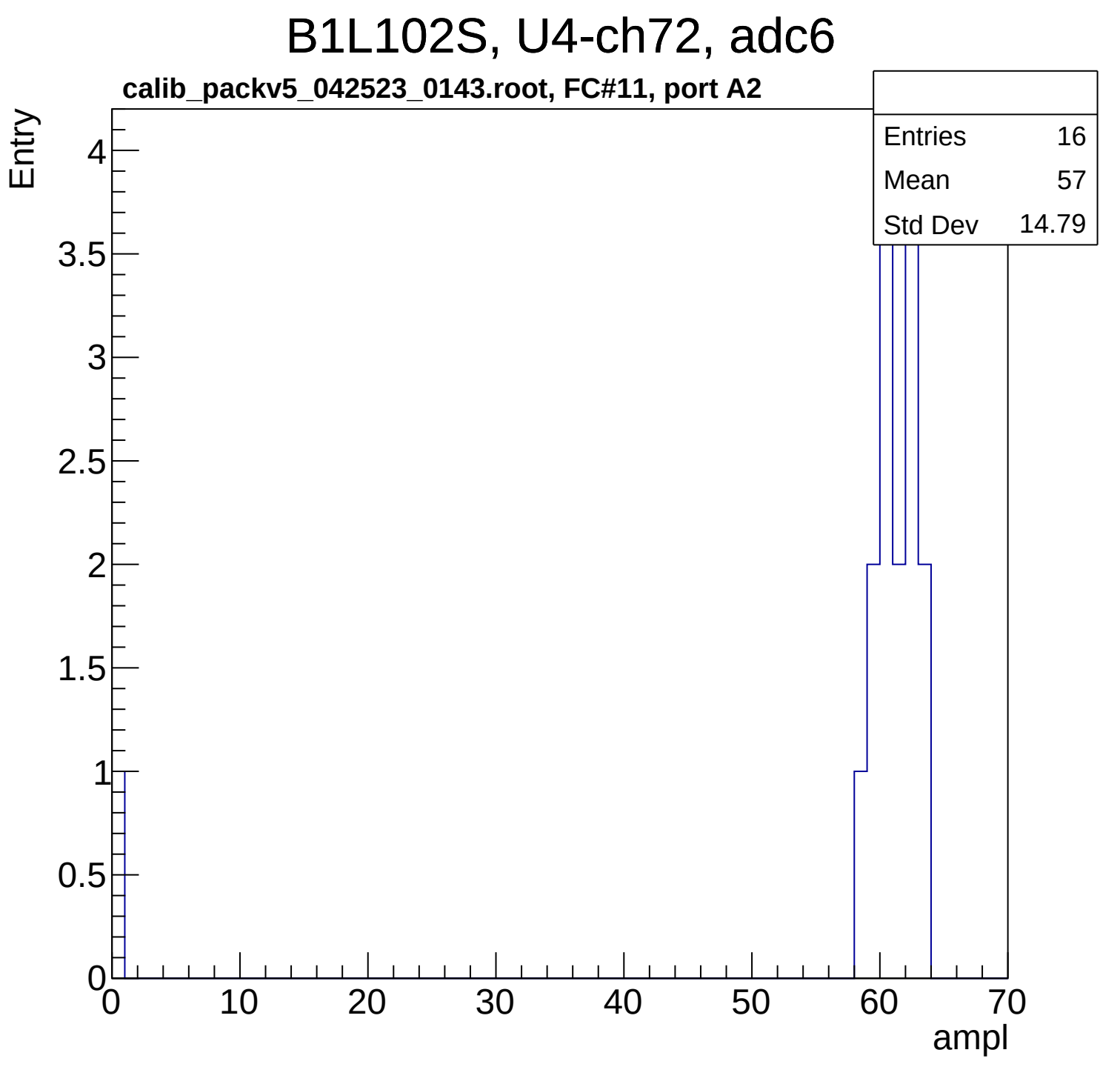
B1L102S, U4-ch72, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 16
Mean 57
Std Dev 14.79
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
10
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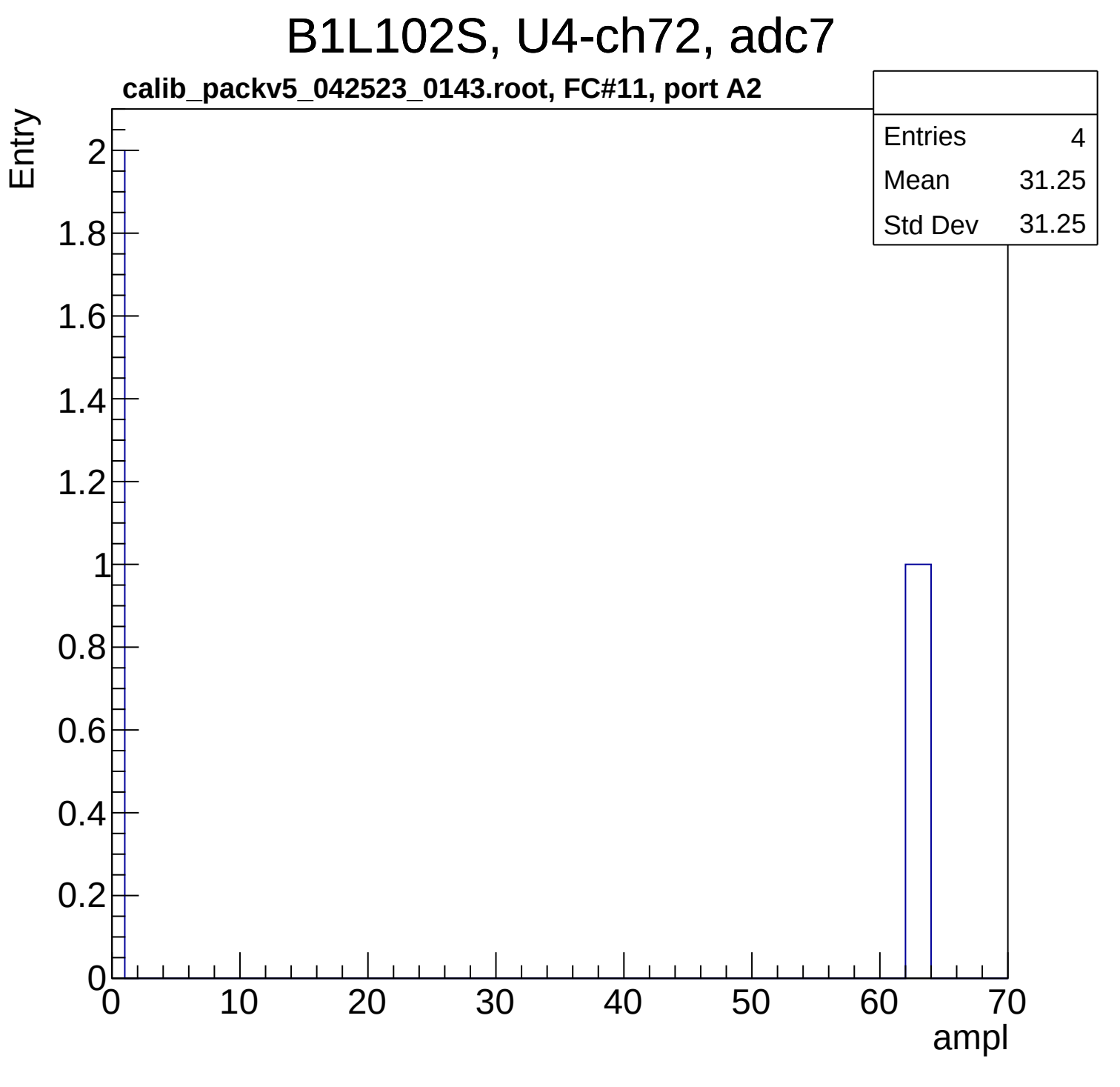
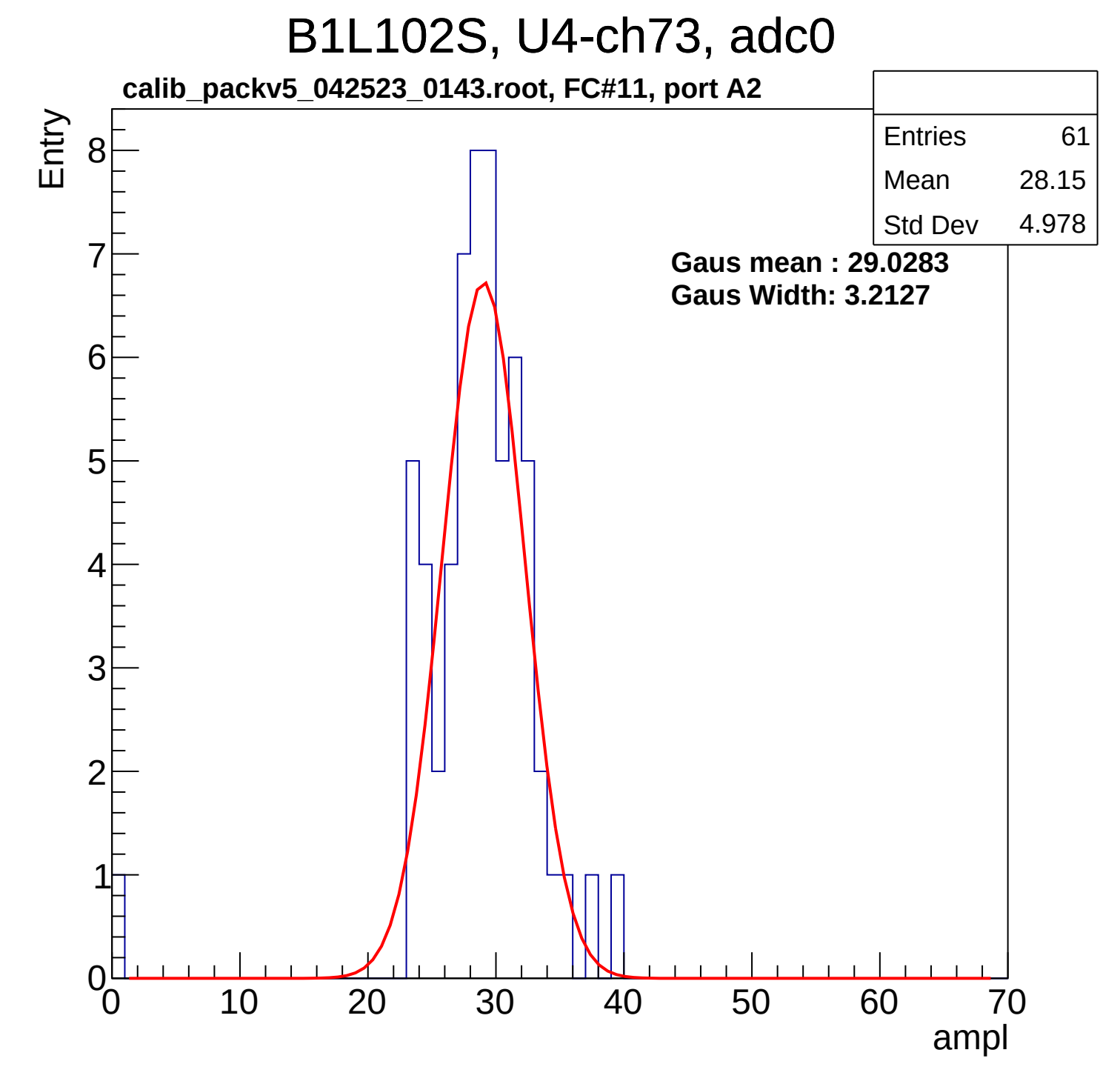
40
50
60
70


B1L102S, U4-ch72, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 4
Mean 31.25
Std Dev 31.25
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L102S, U4-ch73, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 28.15
Std Dev 4.978
Gaus mean : 29.0283
Gaus Width: 3.2127
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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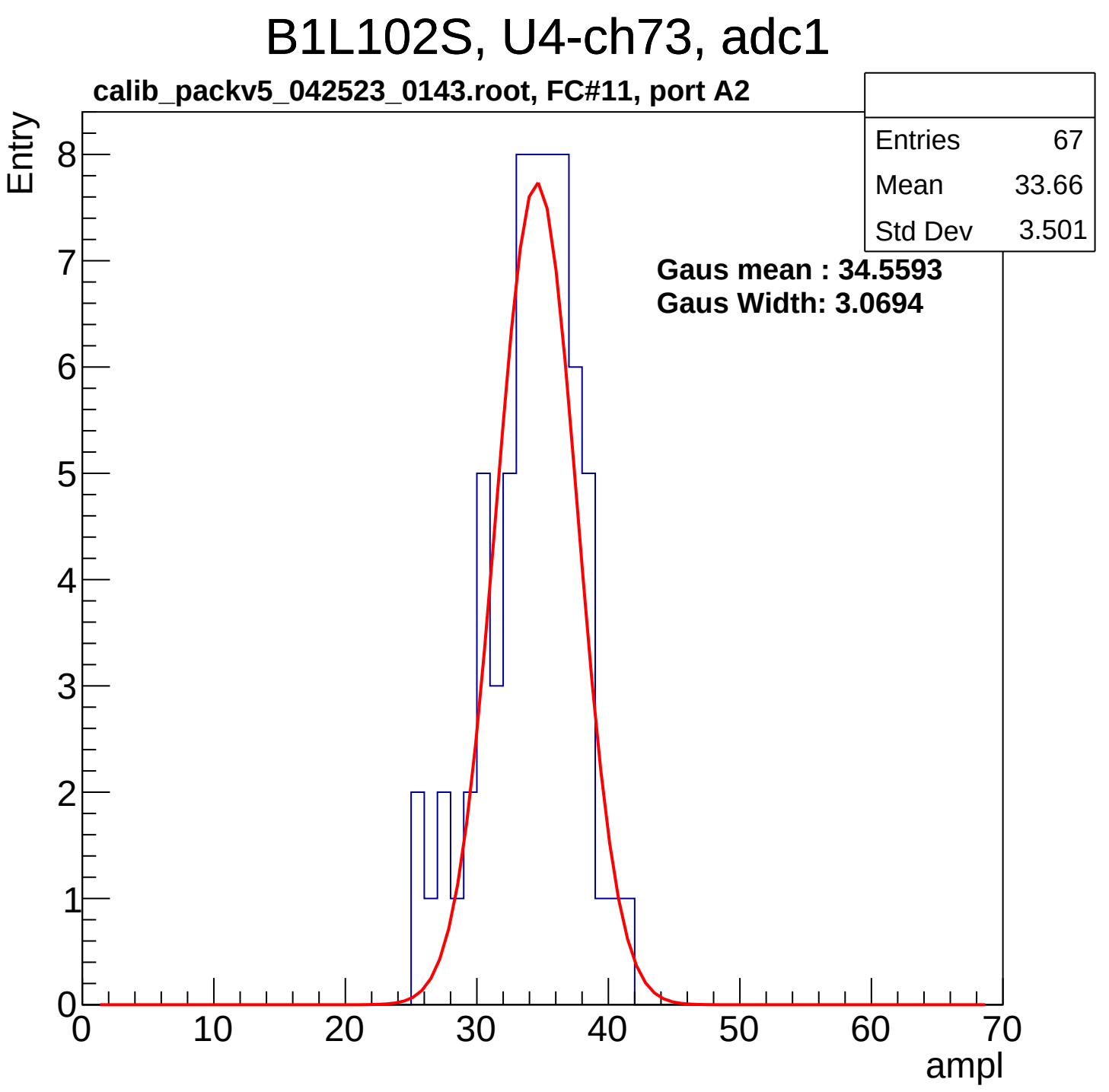
B1L102S, U4-ch73, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 33.66
Std Dev 3.501
Gaus mean : 34.5593
Gaus Width: 3.0694
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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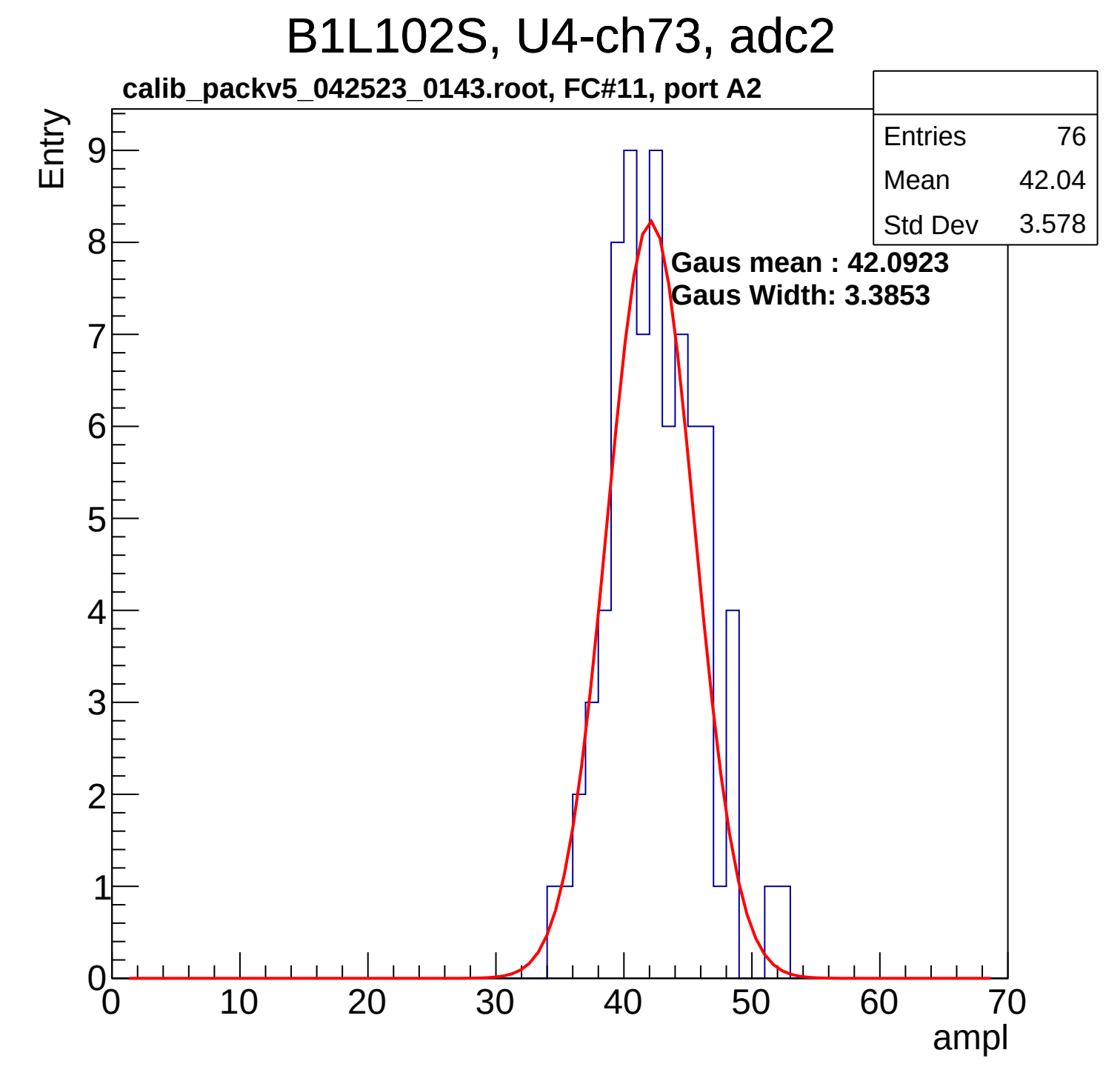
B1L102S, U4-ch73, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 42.04
Std Dev 3.578
Gaus mean : 42.0923
Gaus Width: 3.3853
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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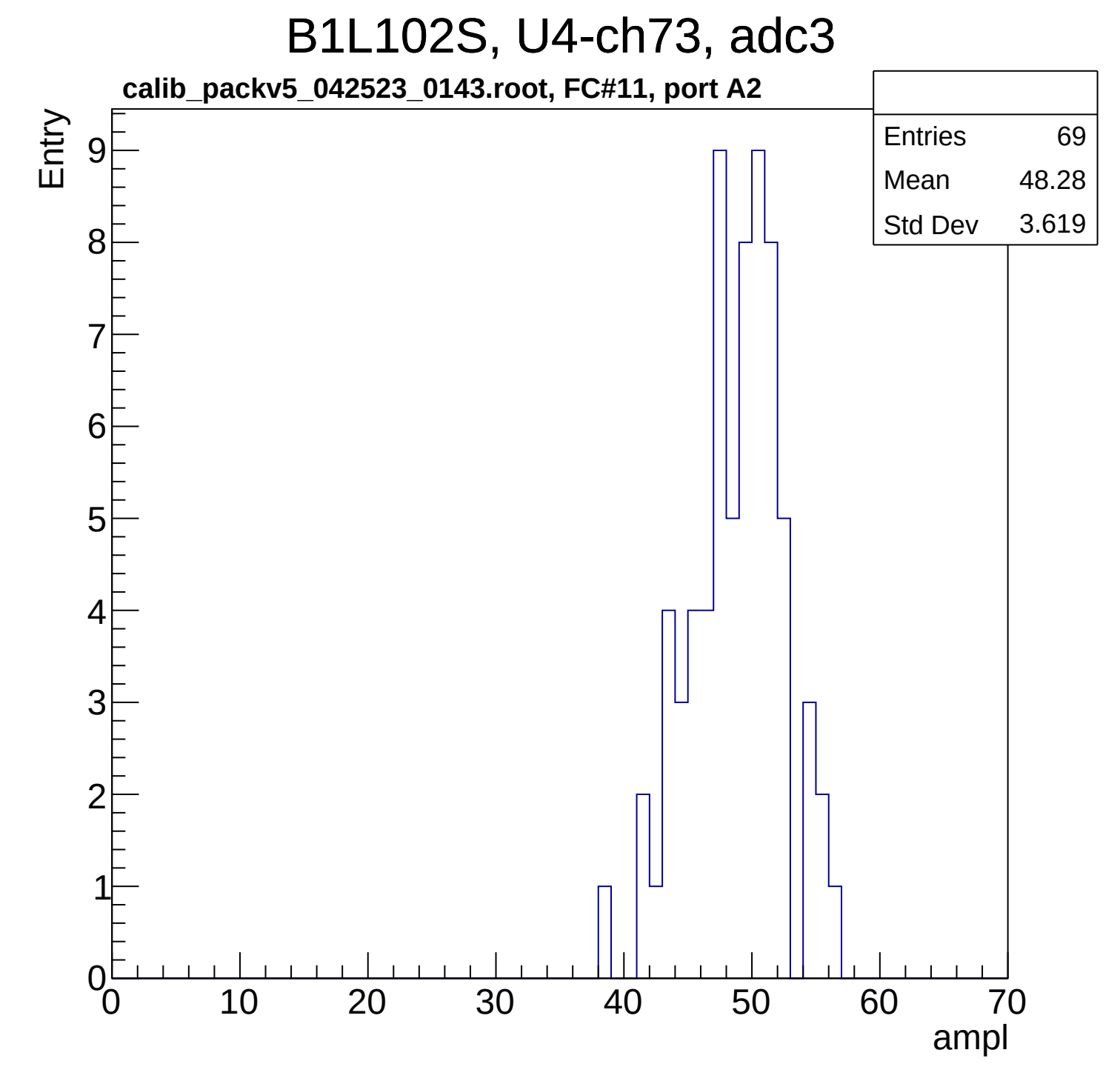
B1L102S, U4-ch73, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 48.28
Std Dev 3.619
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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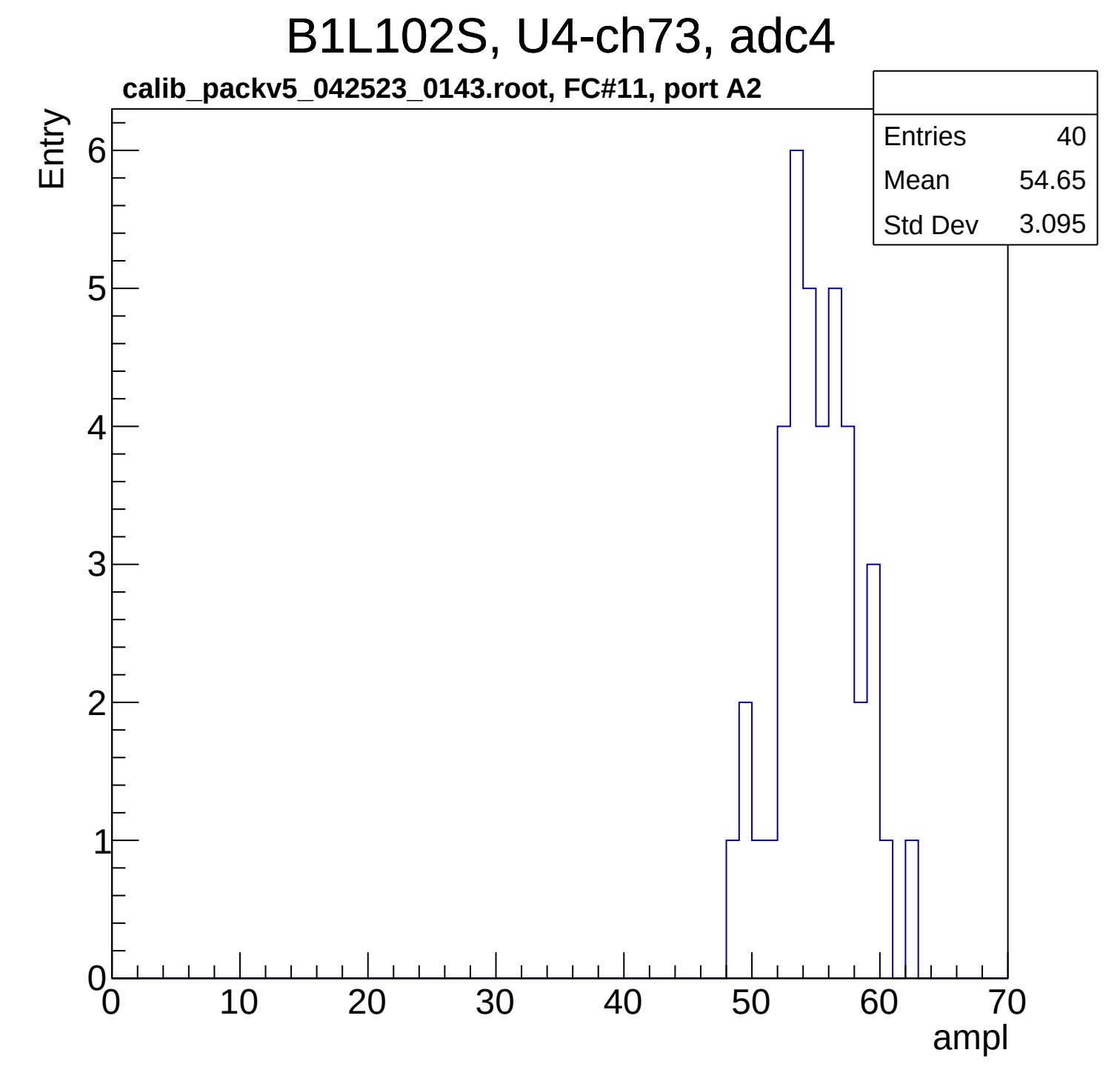
40
50
60
70


B1L102S, U4-ch73, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 40
Mean 54.65
Std Dev 3.095
Entry
0
1
2
3
4
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6
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10
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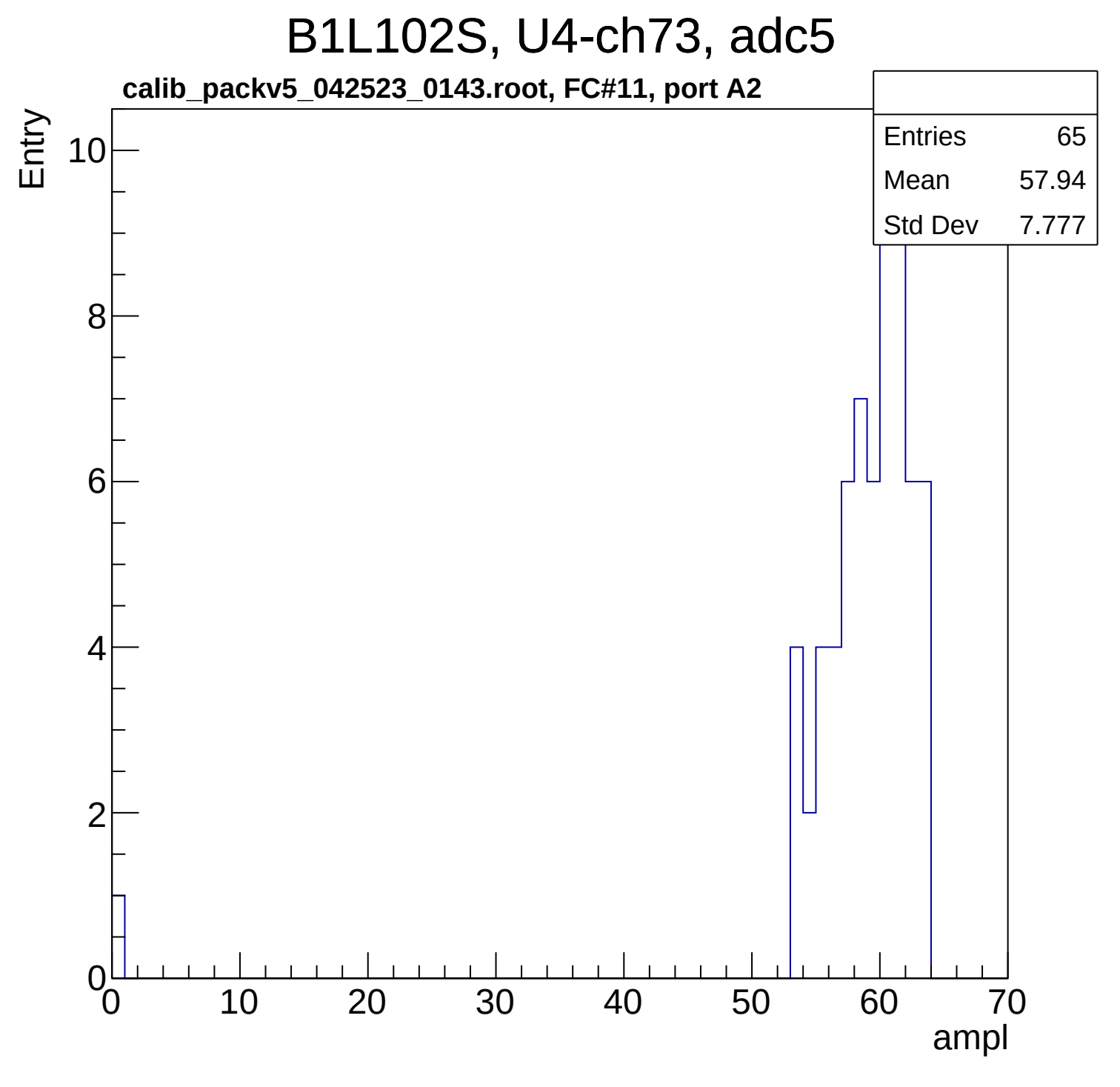
70
ampl


B1L102S, U4-ch73, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 57.94
Std Dev 7.777
Entry
ampl
0
2
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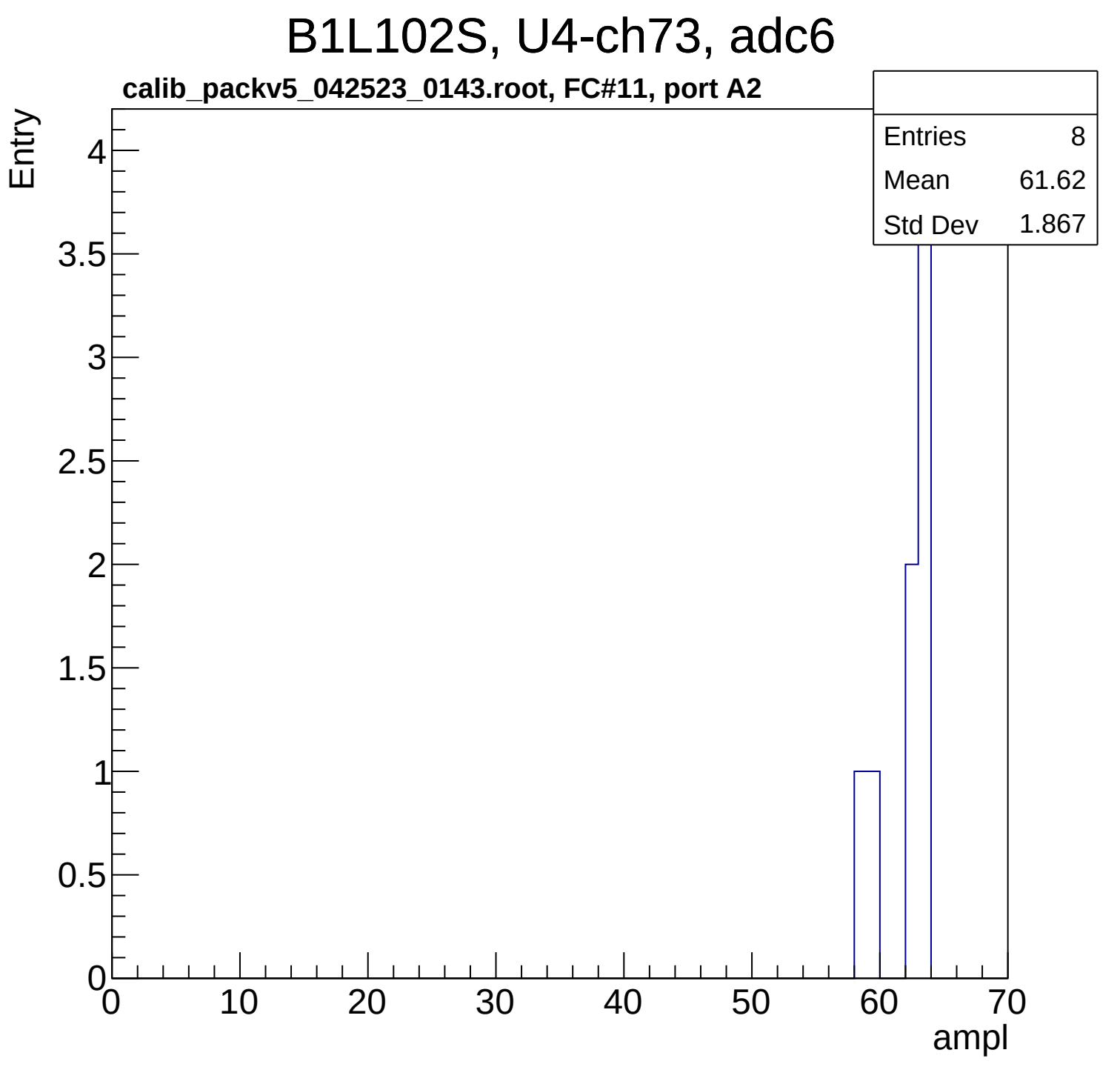
B1L102S, U4-ch73, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 8
Mean 61.62
Std Dev 1.867
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
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40
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60
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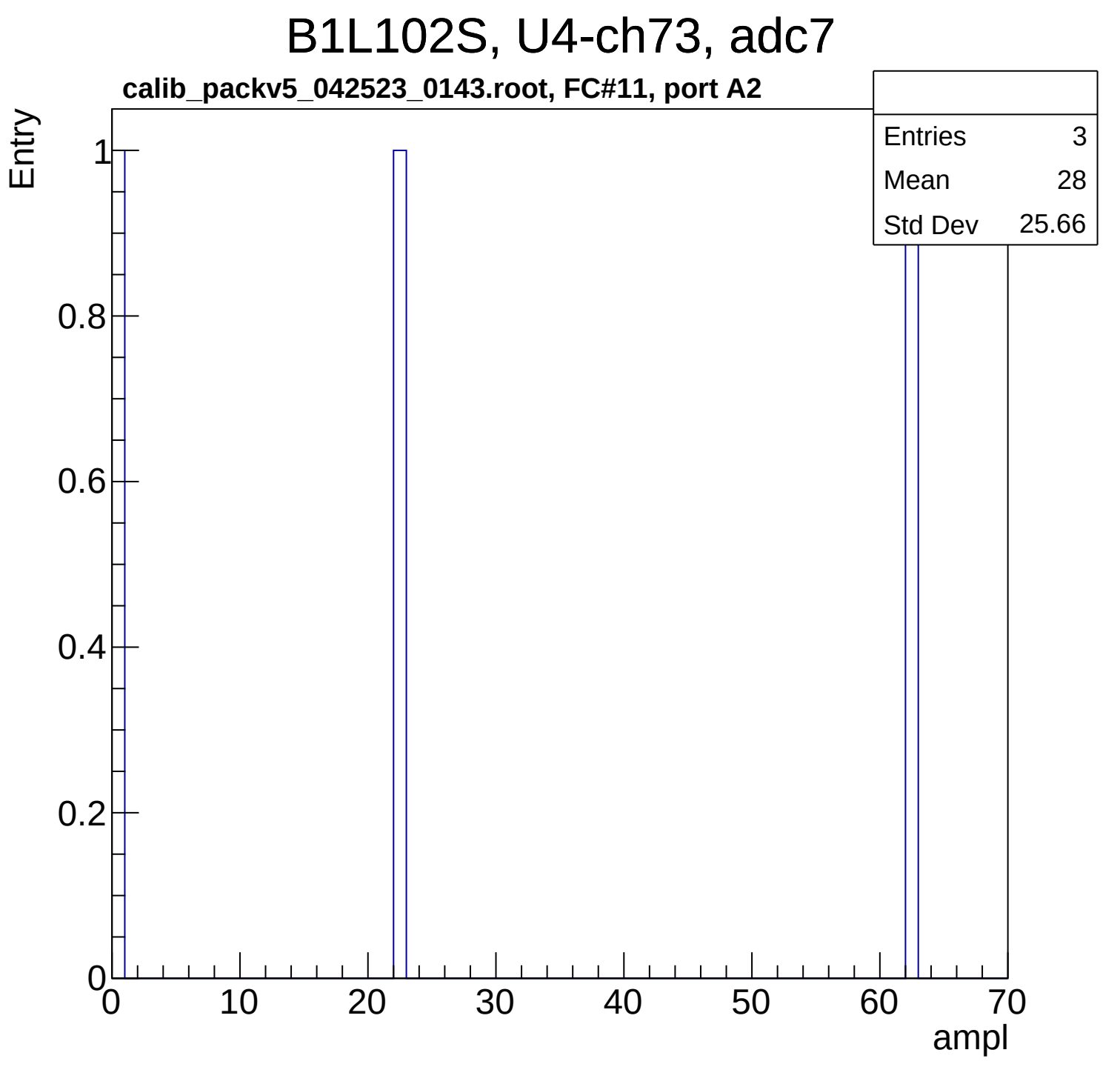
B1L102S, U4-ch73, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 28
Std Dev 25.66
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
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60
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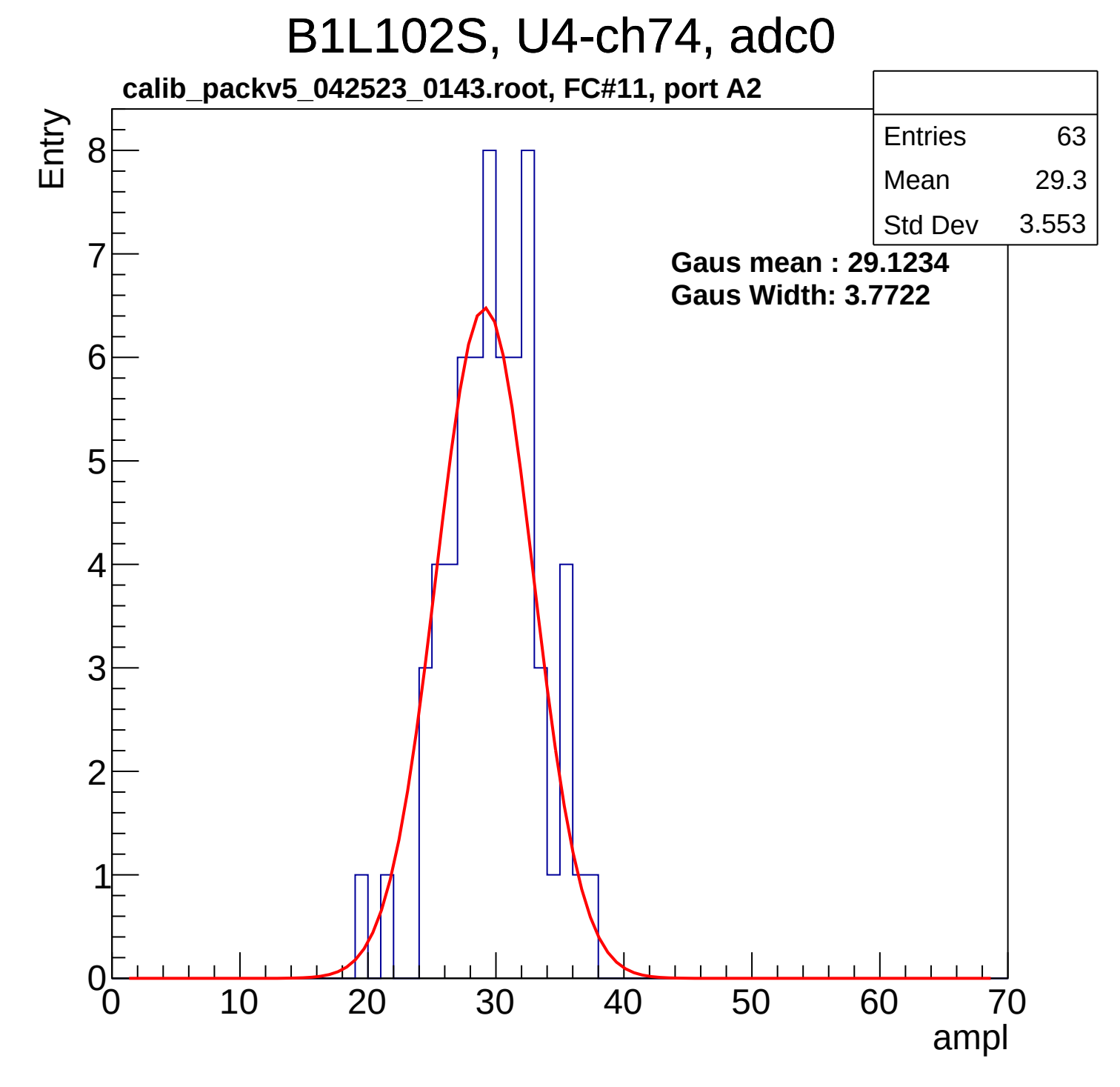
B1L102S, U4-ch74, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 29.3
Std Dev 3.553
Gaus mean : 29.1234
Gaus Width: 3.7722
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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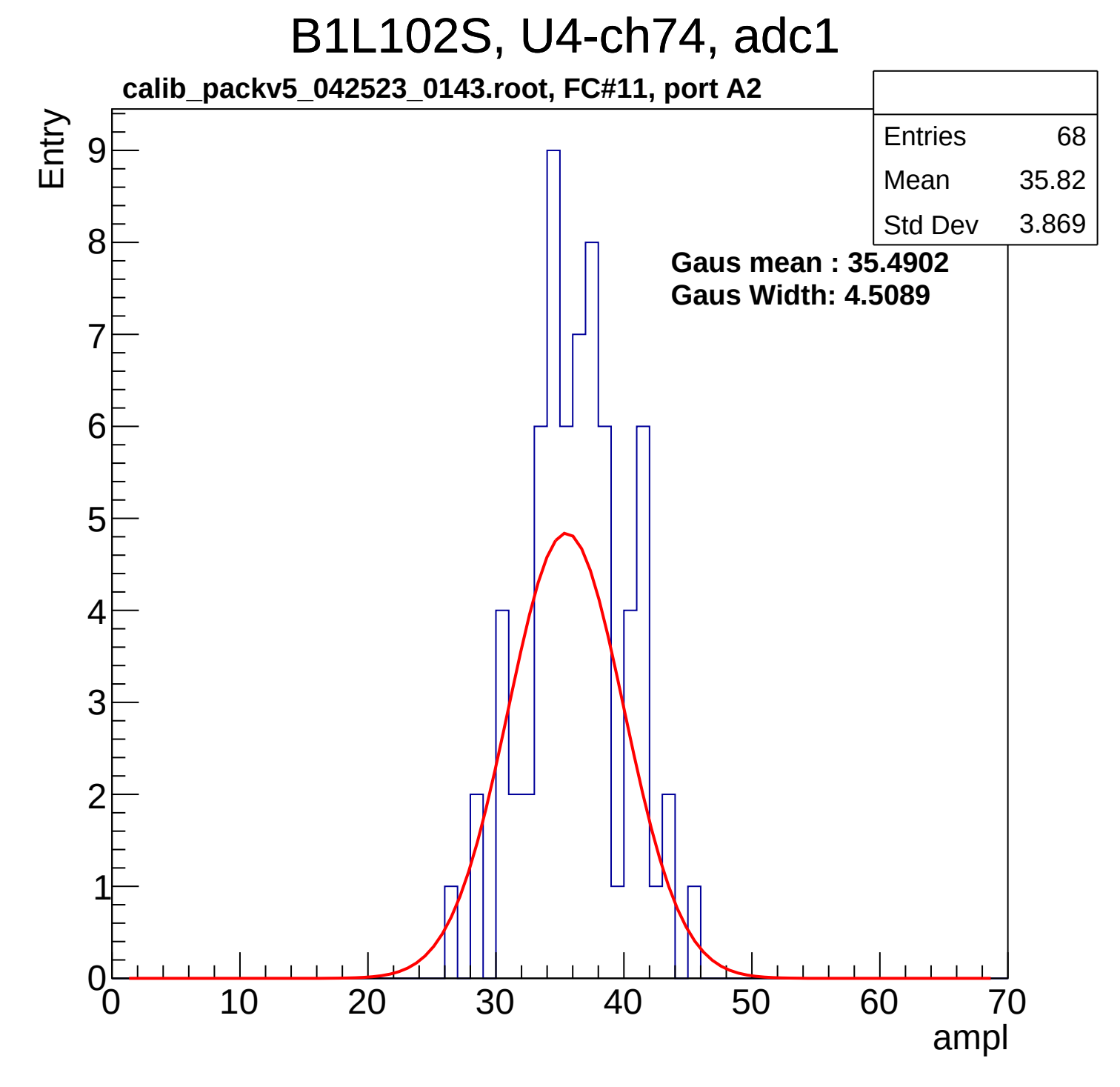
B1L102S, U4-ch74, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 35.82
Std Dev 3.869
Gaus mean : 35.4902
Gaus Width: 4.5089
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
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40
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60
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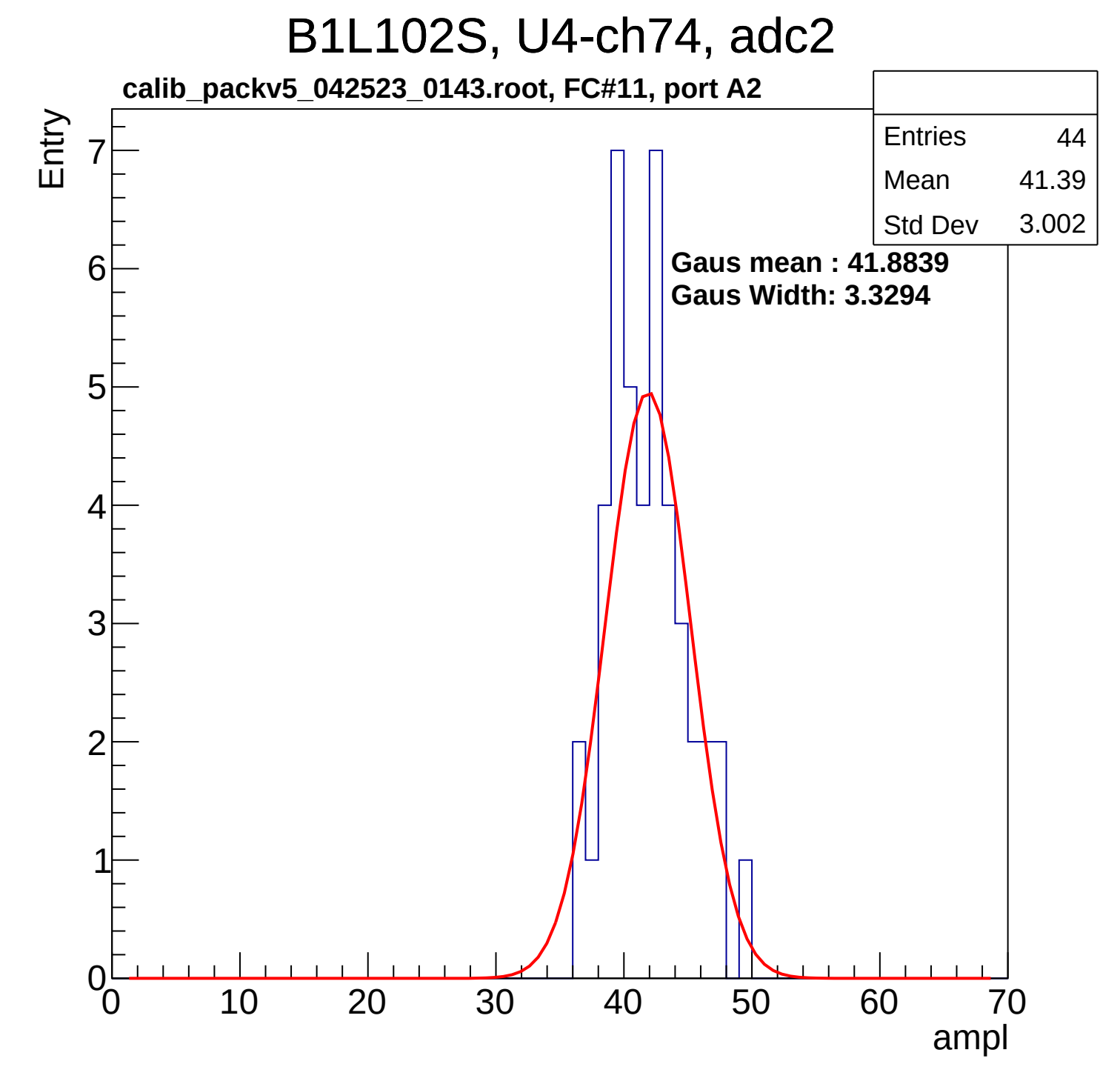
B1L102S, U4-ch74, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 44
Mean 41.39
Std Dev 3.002
Gaus mean : 41.8839
Gaus Width: 3.3294
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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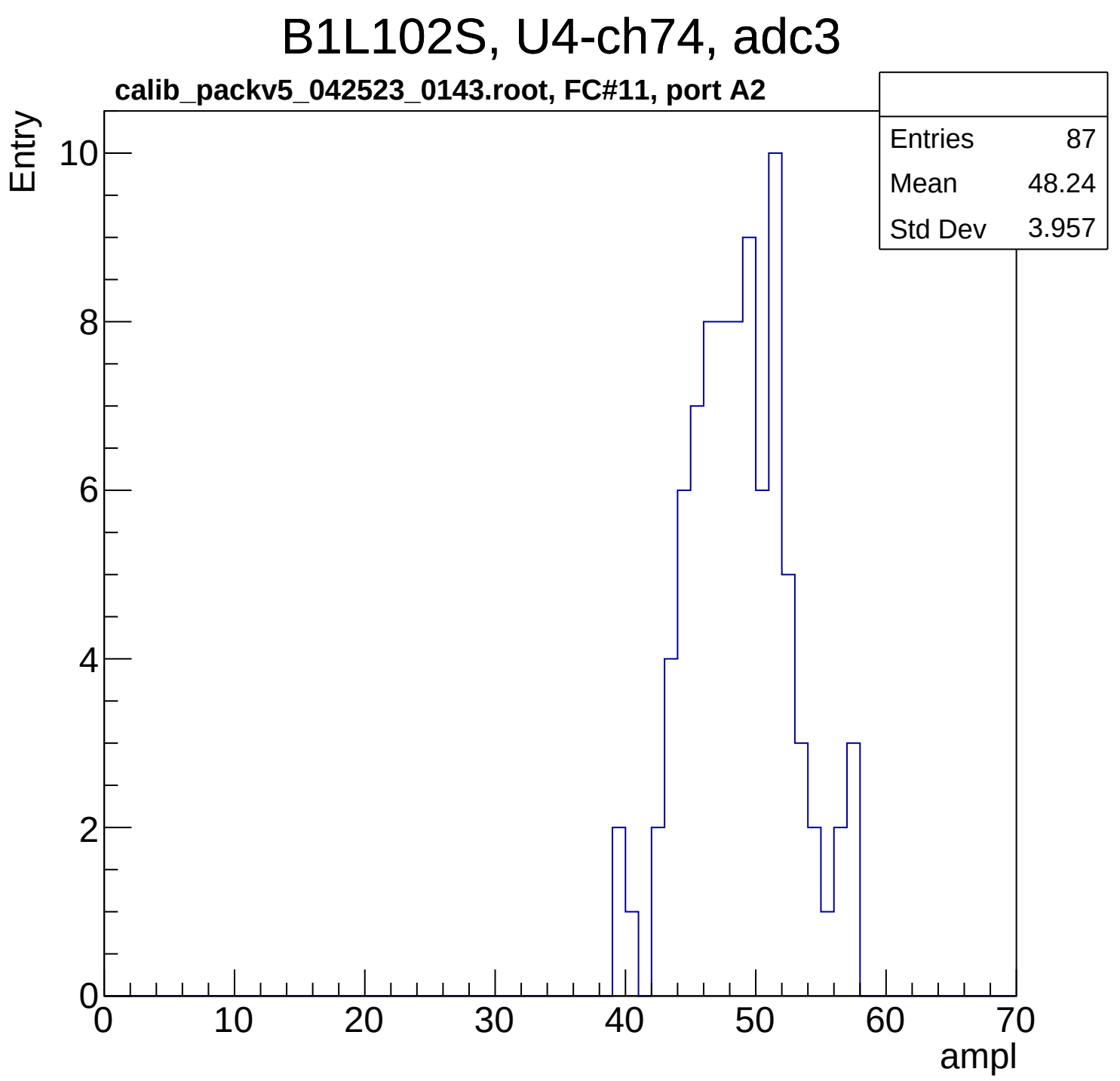
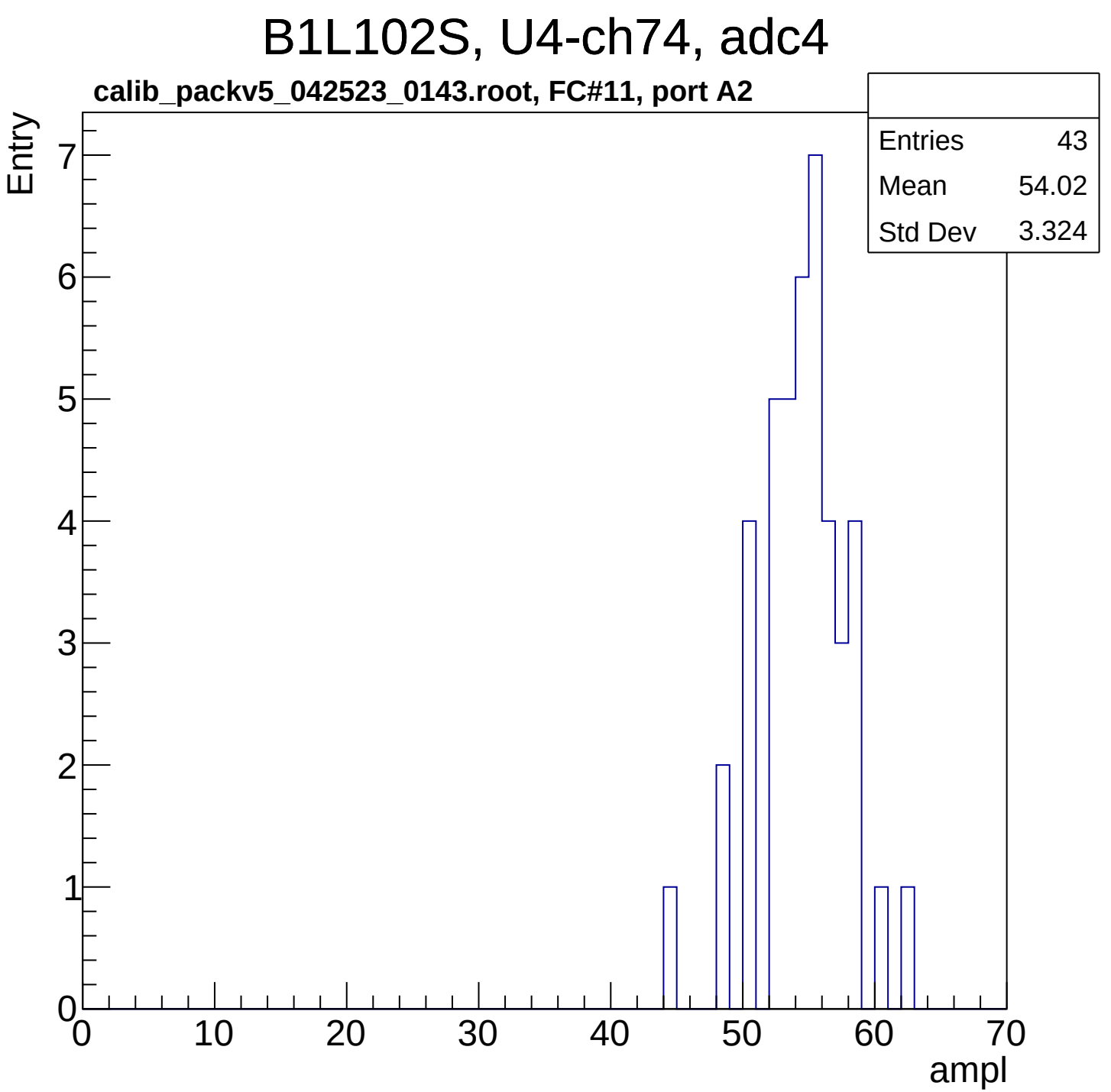
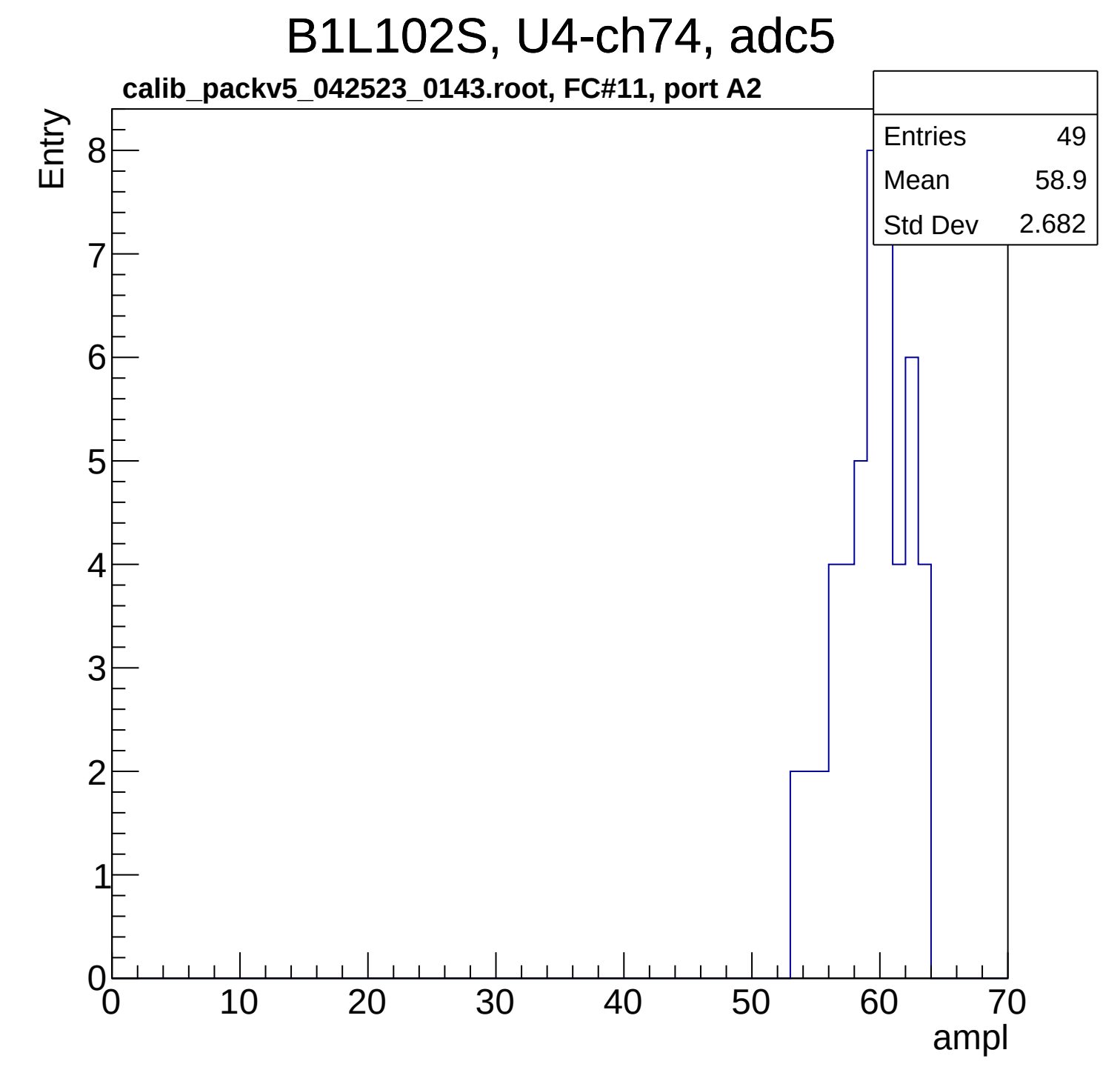

B1L102S, U4-ch74, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 87
Mean 48.24
Std Dev 3.957
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch74, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 43
Mean 54.02
Std Dev 3.324
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch74, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 58.9
Std Dev 2.682
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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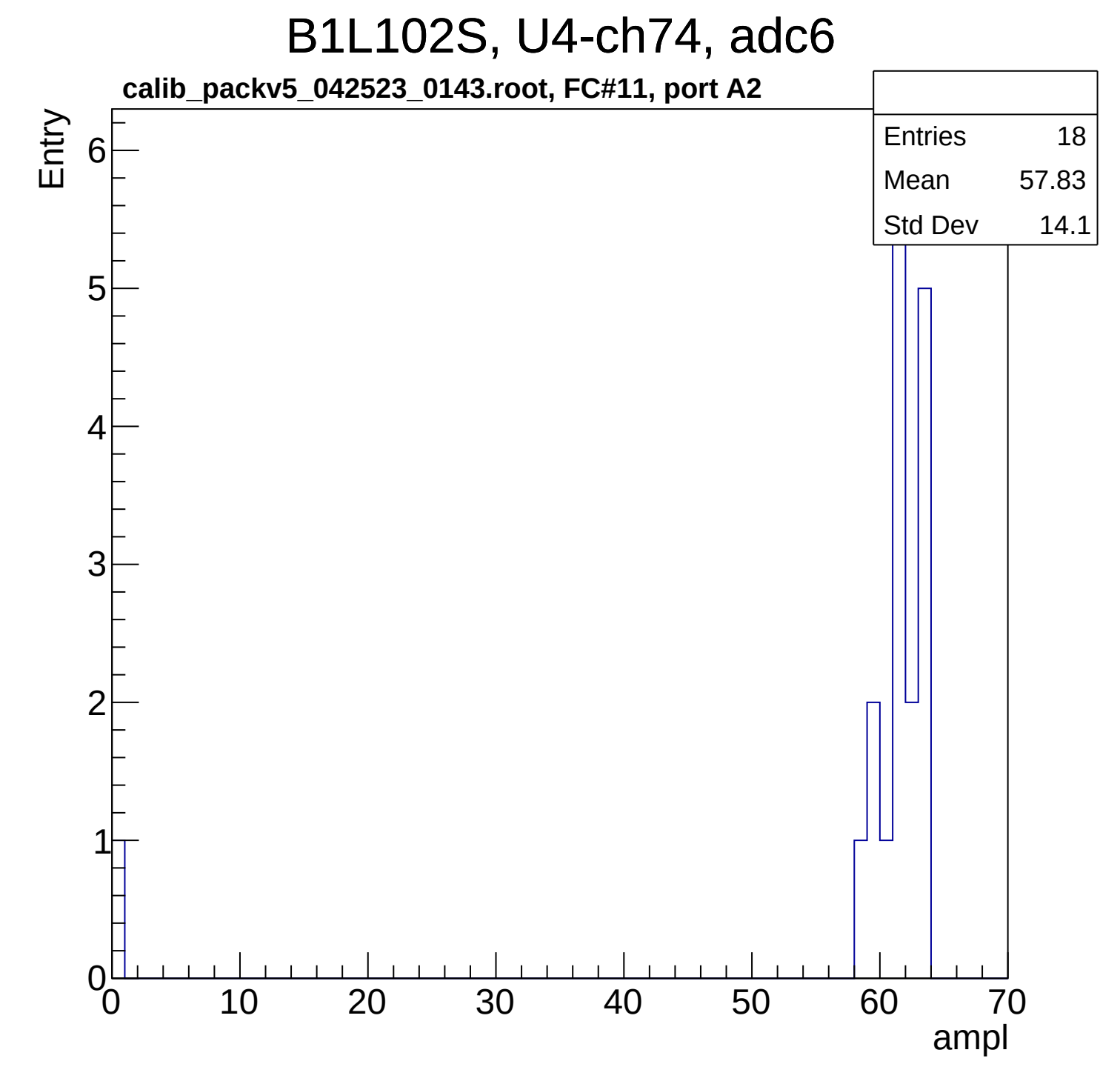
B1L102S, U4-ch74, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 18
Mean 57.83
Std Dev 14.1
Entry
ampl
0
1
2
3
4
5
6
0
10
20
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40
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60
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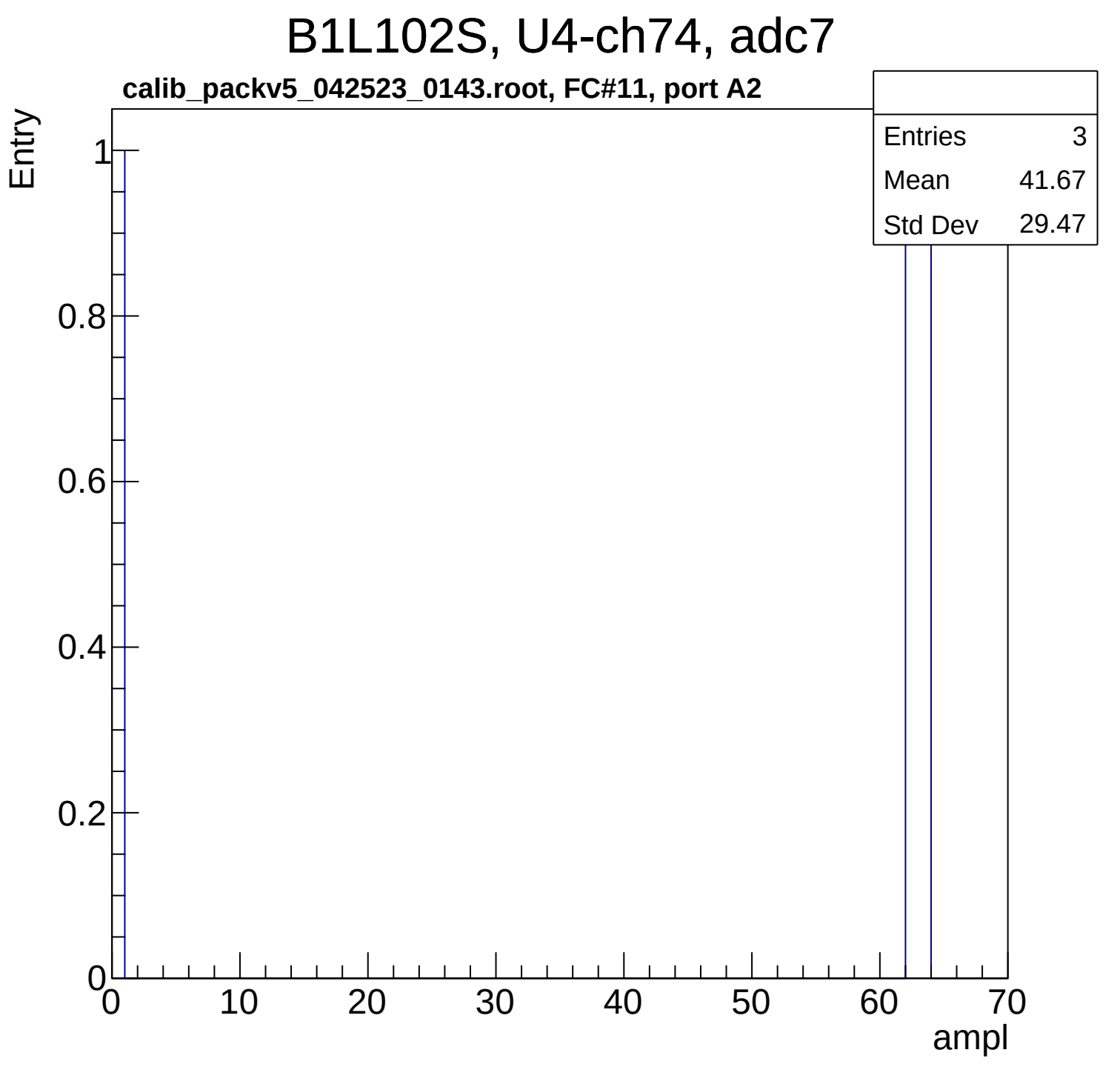
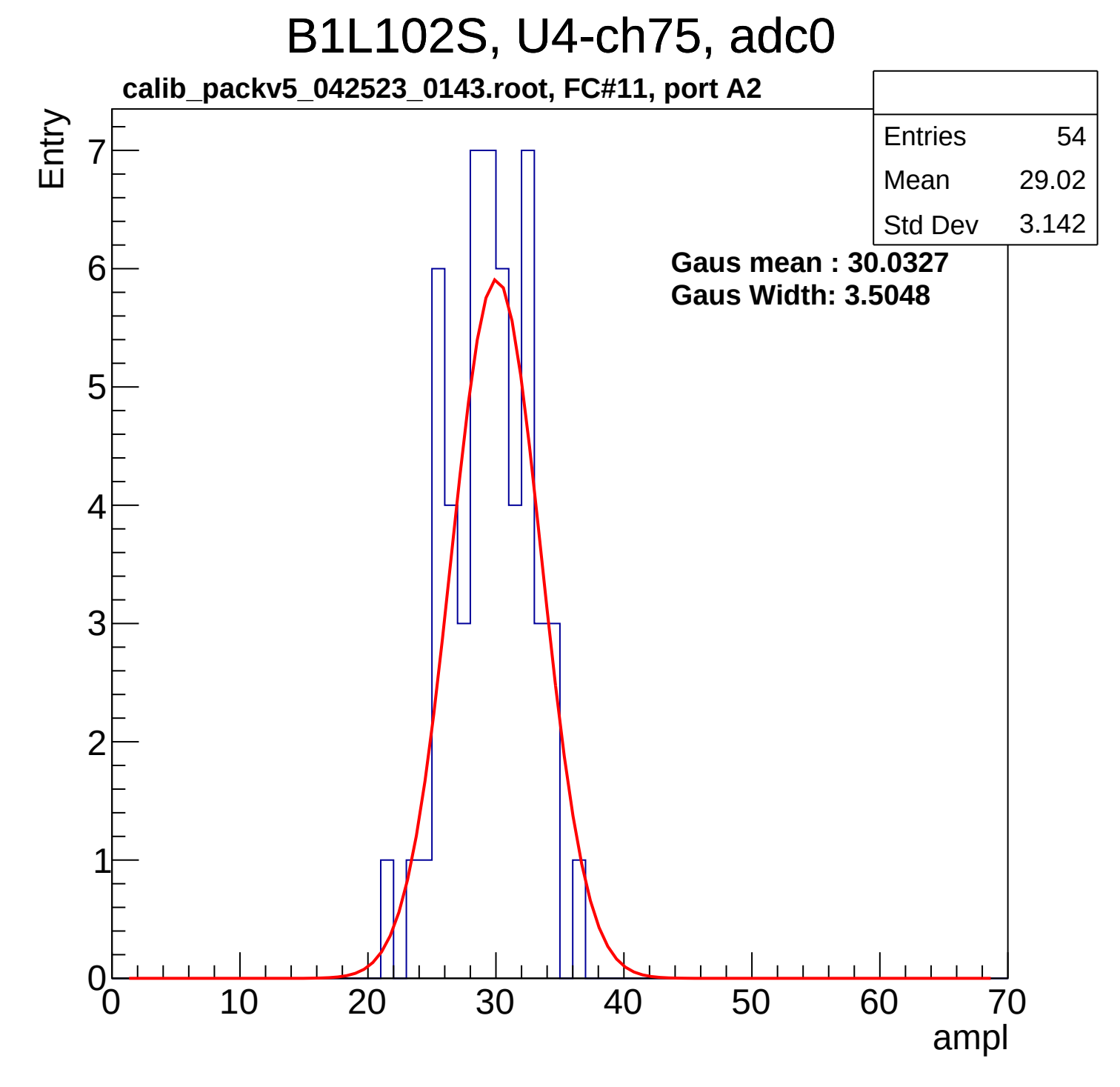
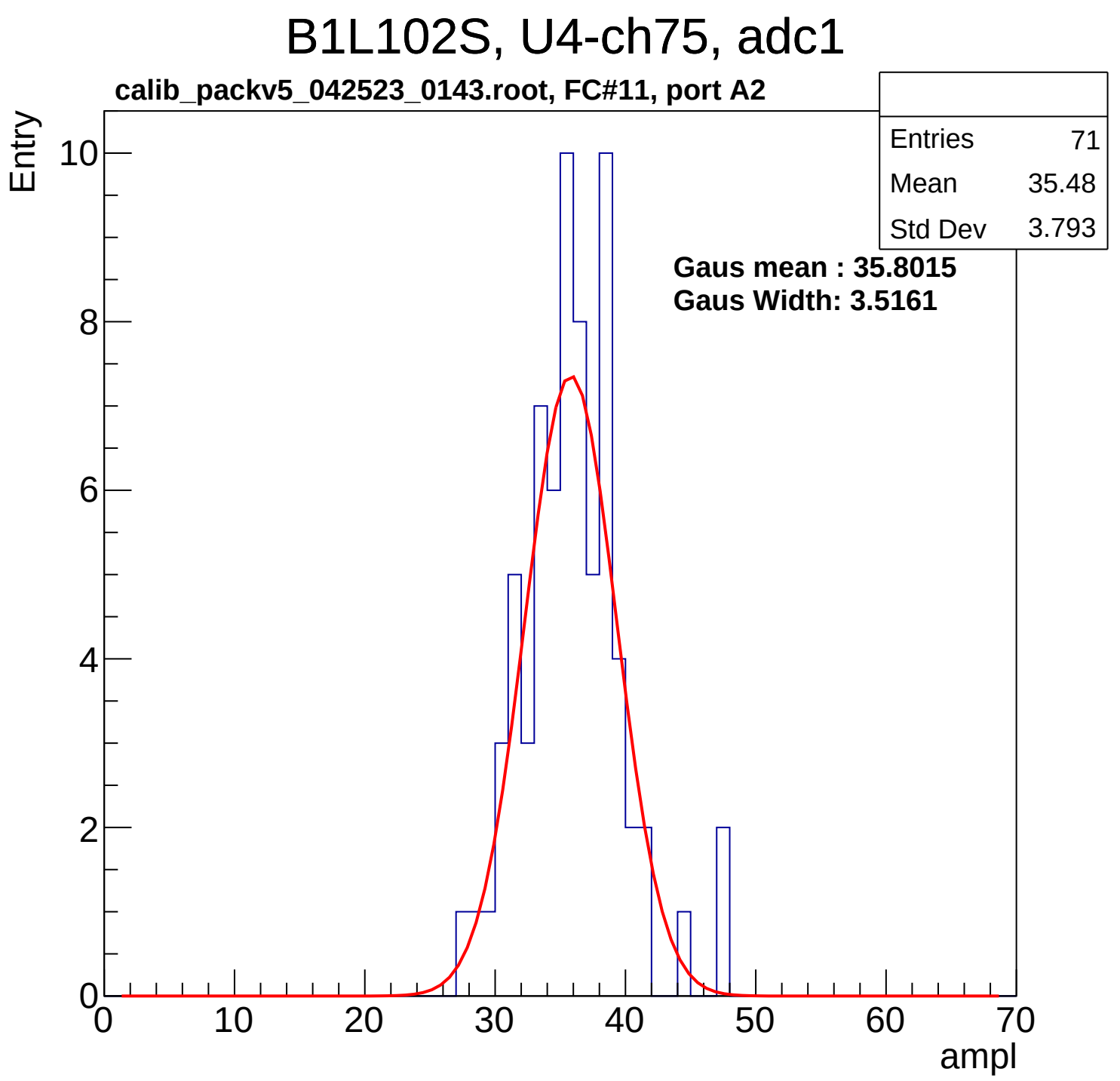

B1L102S, U4-ch74, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 41.67
Std Dev 29.47
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch75, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 29.02
Std Dev 3.142
Gaus mean : 30.0327
Gaus Width: 3.5048
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch75, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 35.48
Std Dev 3.793
Gaus mean : 35.8015
Gaus Width: 3.5161
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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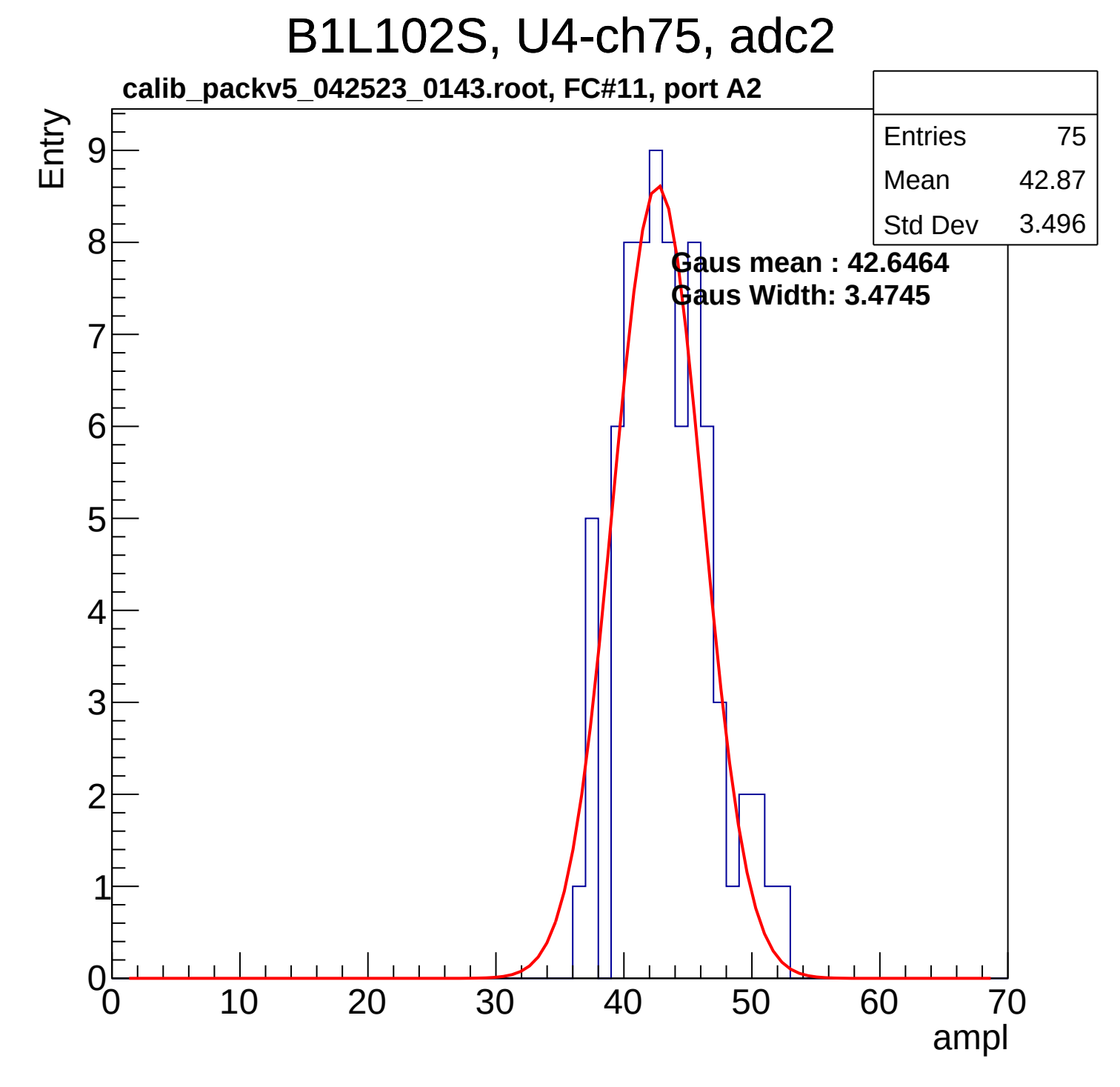
B1L102S, U4-ch75, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 42.87
Std Dev 3.496
Gaus mean : 42.6464
Gaus Width: 3.4745
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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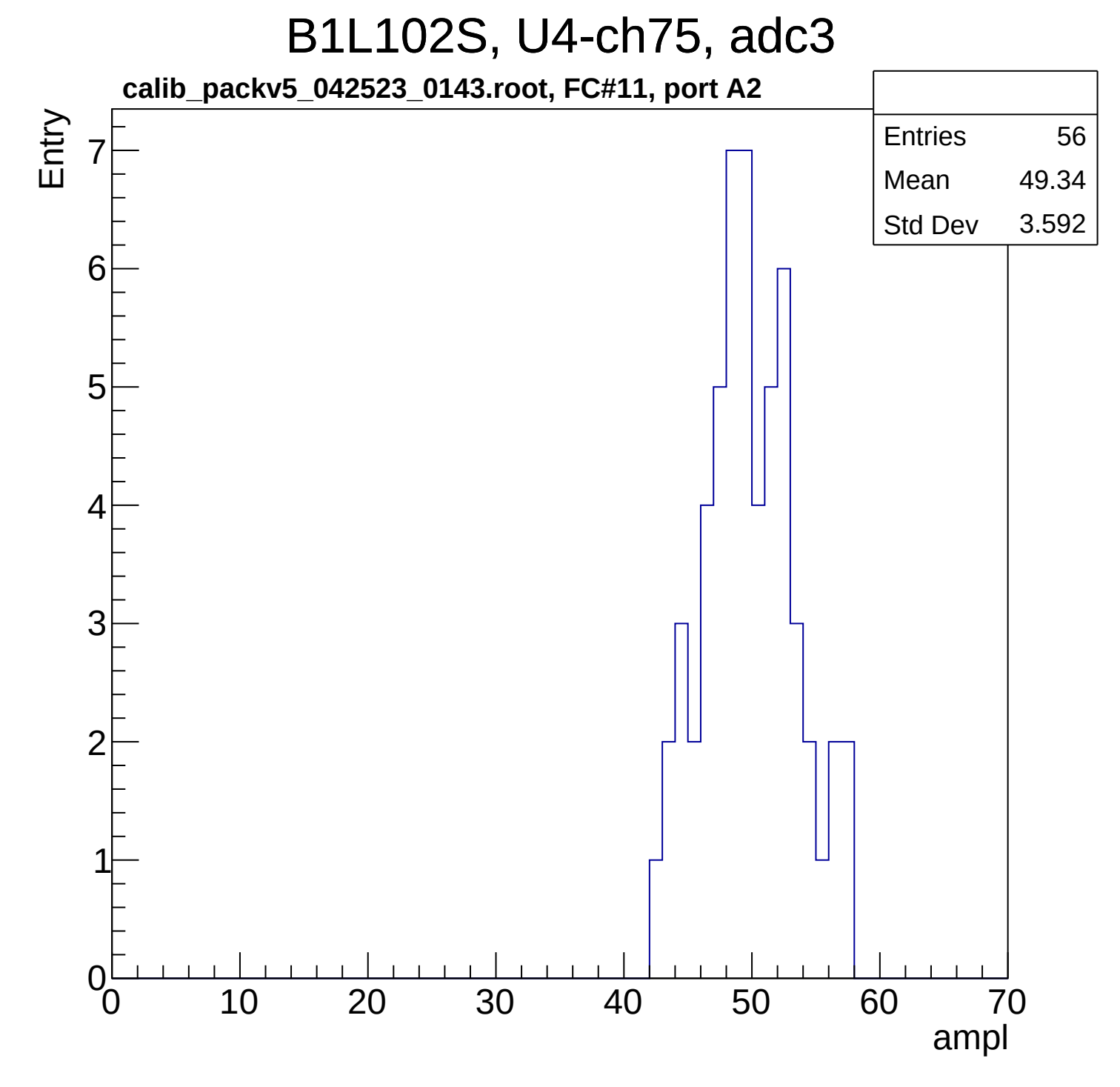
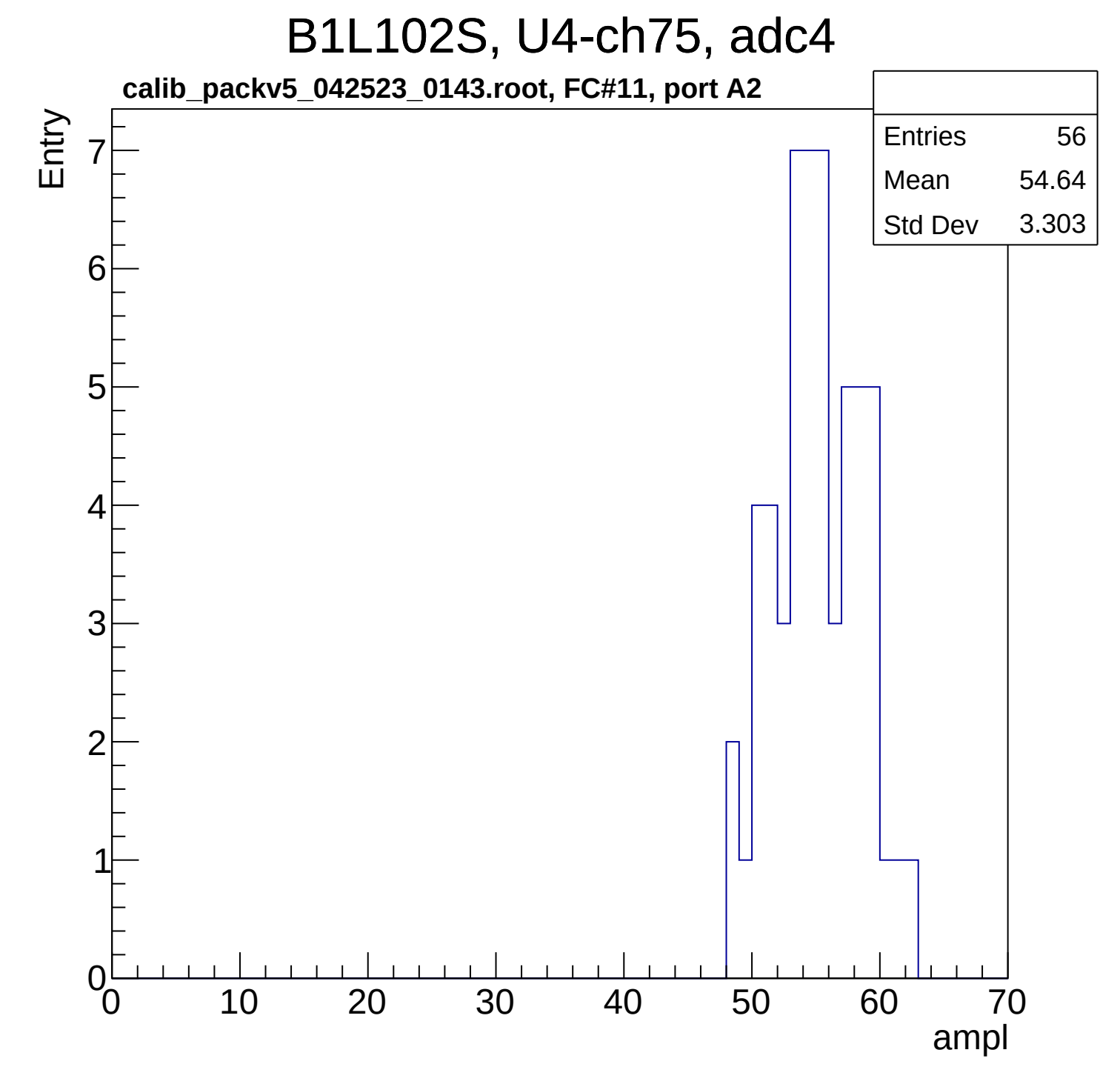

B1L102S, U4-ch75, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 49.34
Std Dev 3.592
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch75, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 54.64
Std Dev 3.303
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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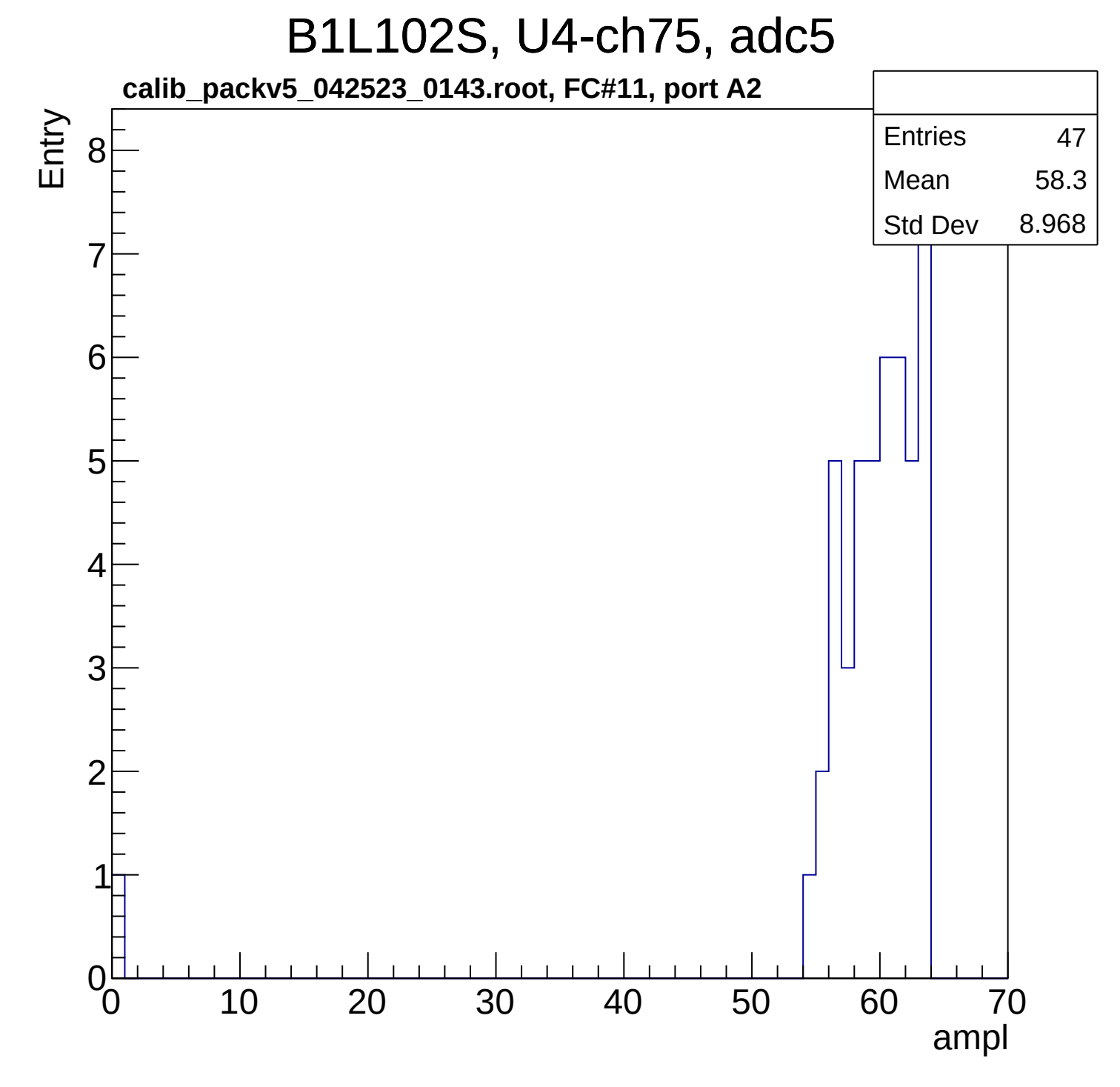
B1L102S, U4-ch75, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 47
Mean 58.3
Std Dev 8.968
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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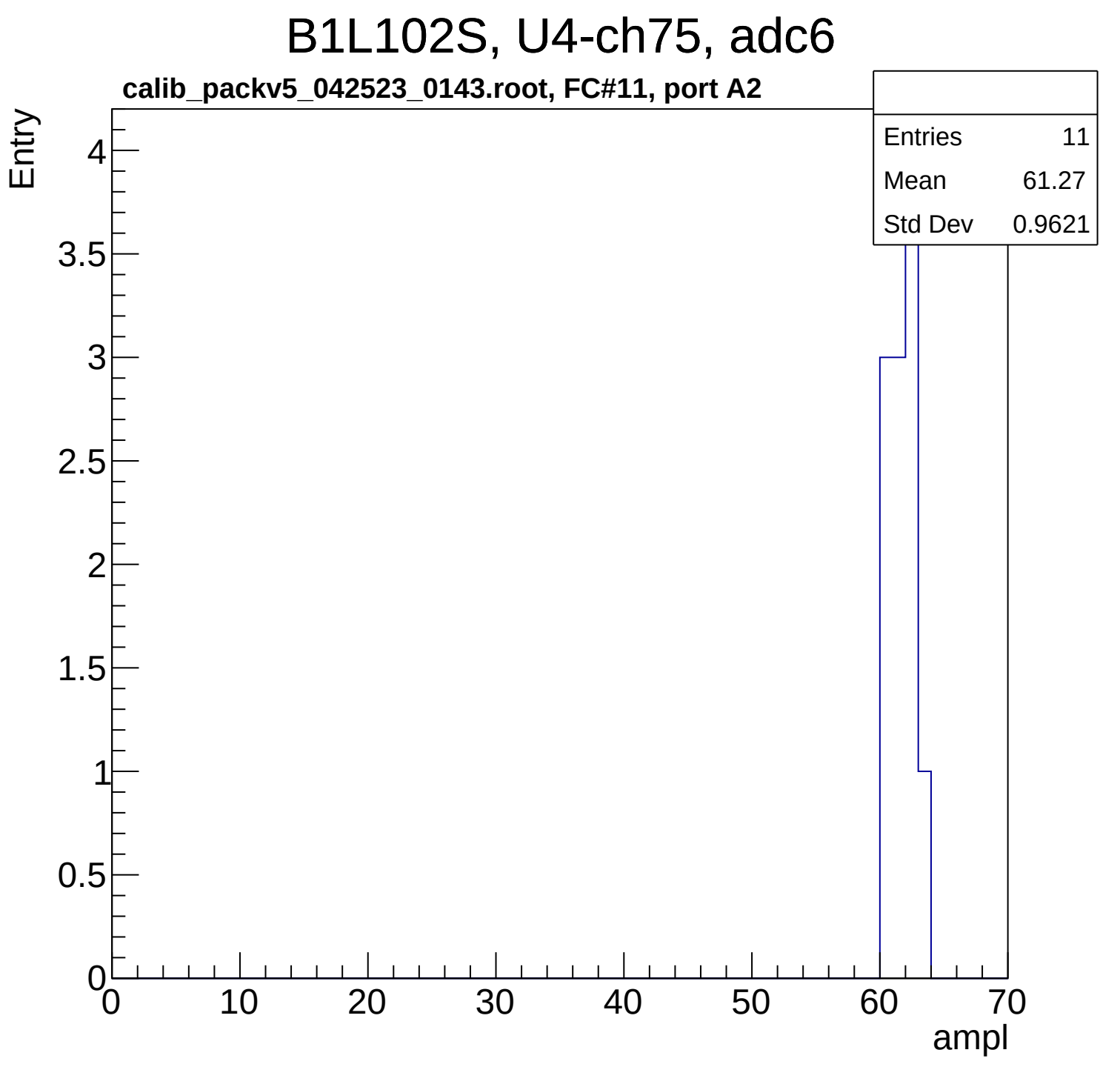
B1L102S, U4-ch75, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 11
Mean 61.27
Std Dev 0.9621
Entry
ampl
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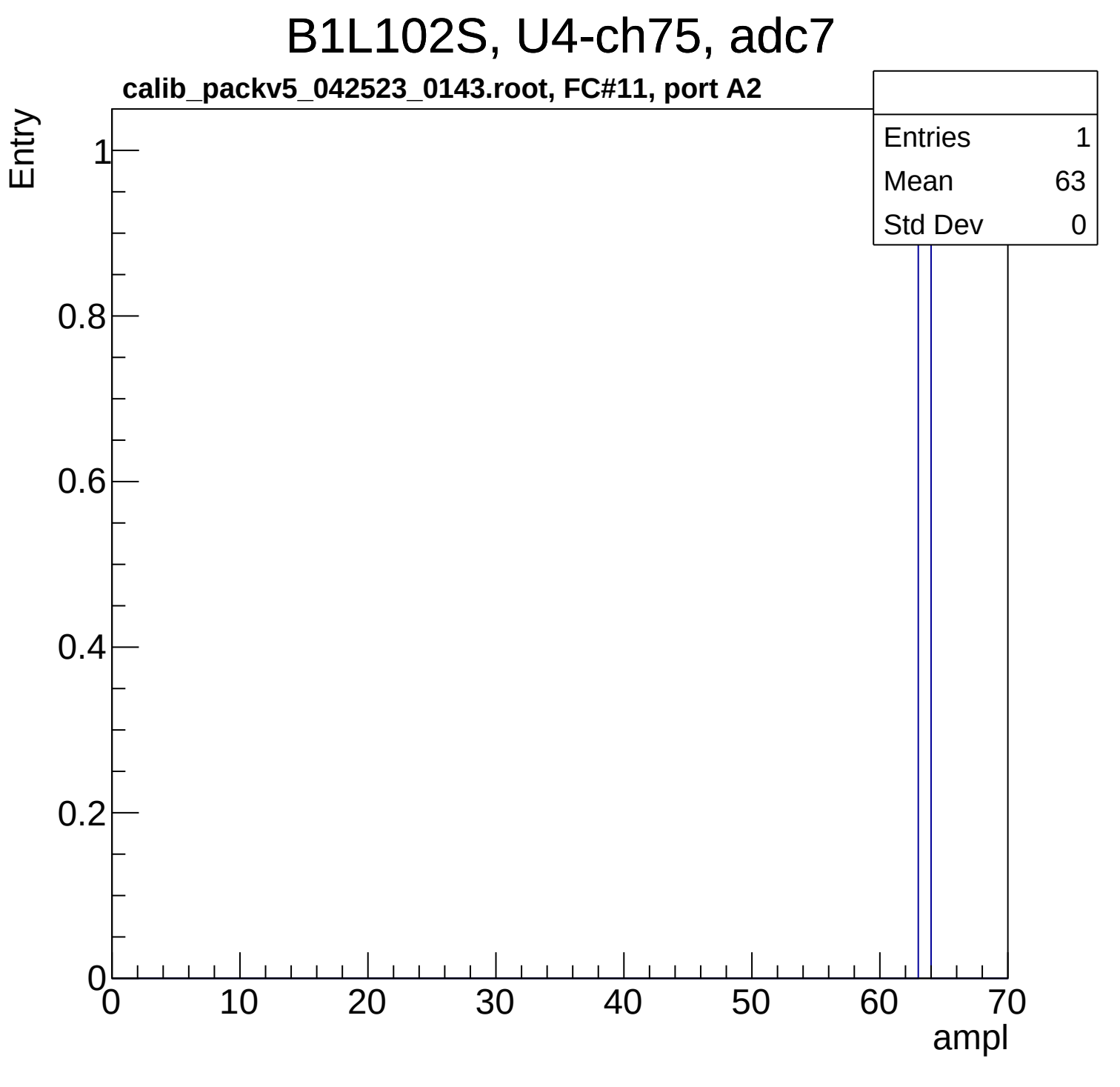
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U4-ch75, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
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10
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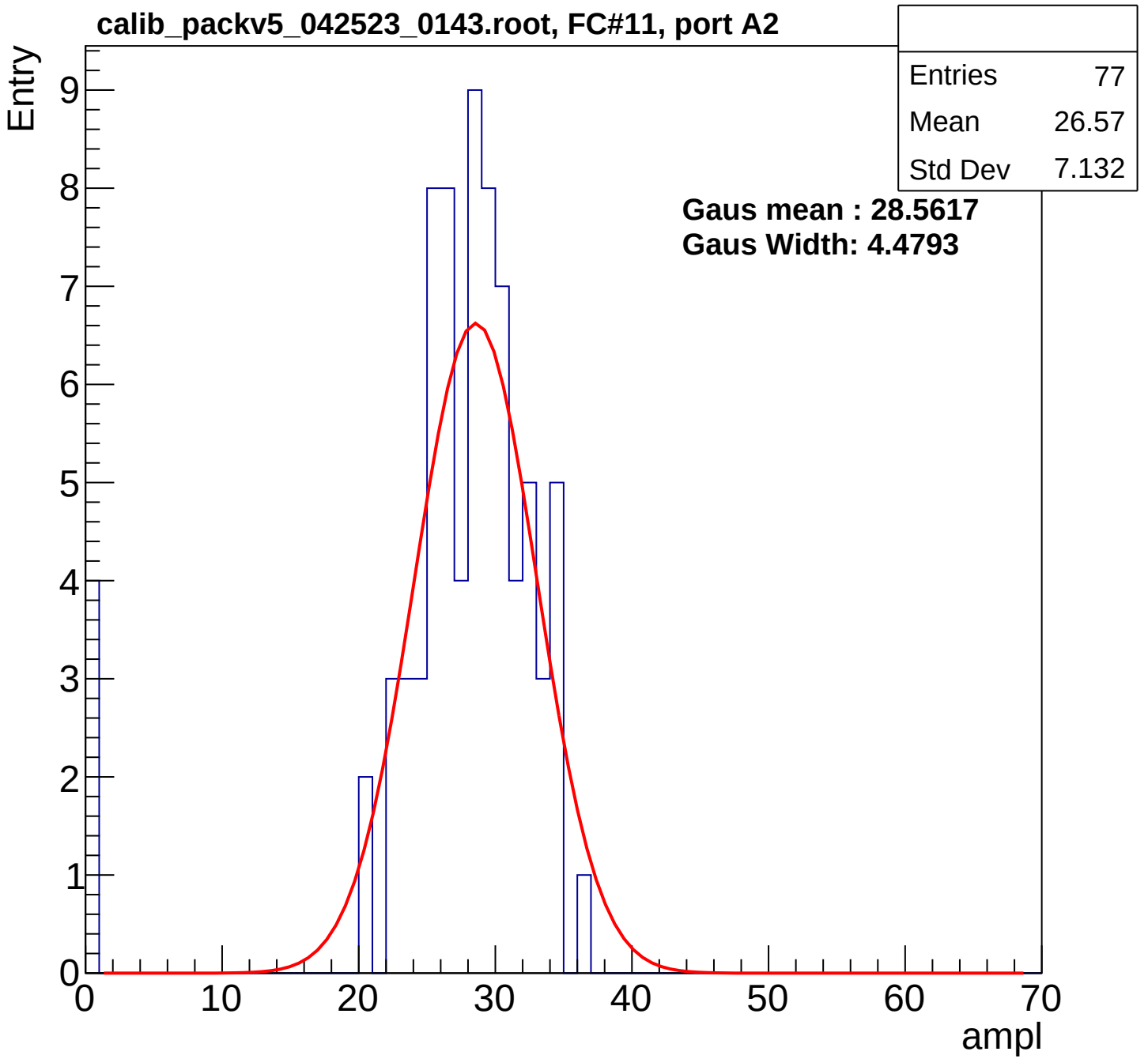
50
60
70
ampl


B1L102S, U4-ch76, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 77
Mean 26.57
Std Dev 7.132
Gaus mean : 28.5617
Gaus Width: 4.4793
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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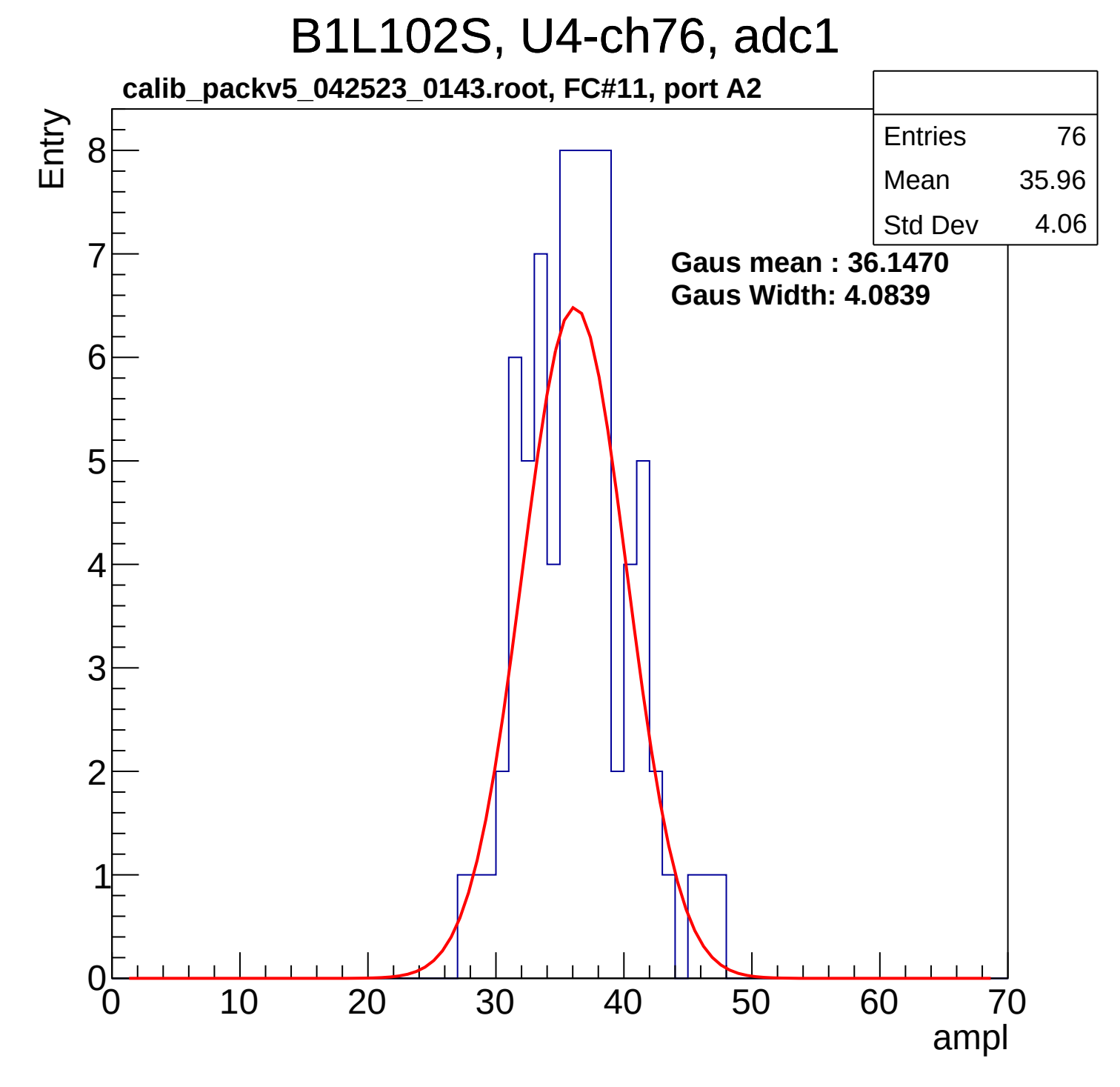
B1L102S, U4-ch76, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 35.96
Std Dev 4.06
Gaus mean : 36.1470
Gaus Width: 4.0839
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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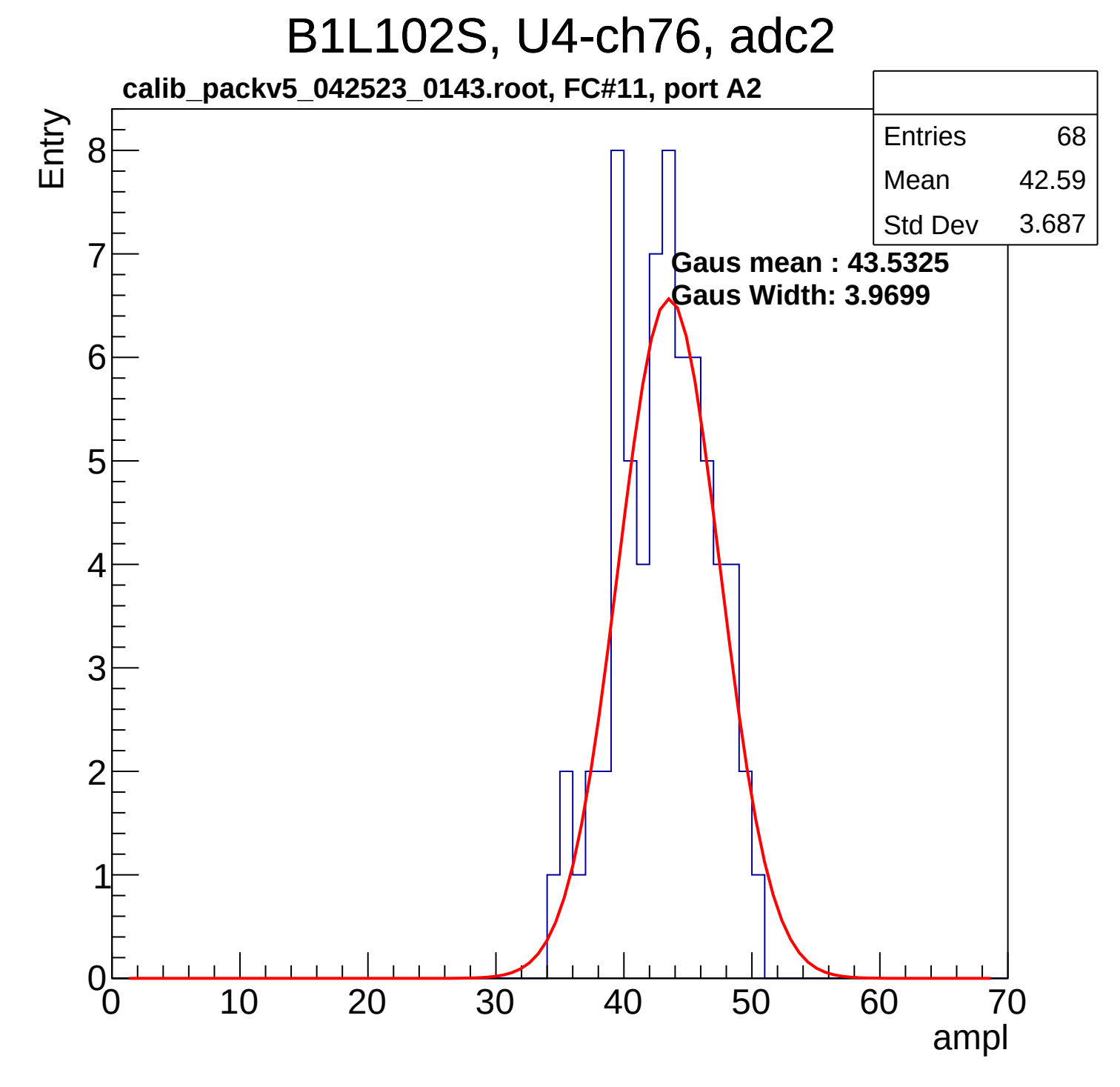
B1L102S, U4-ch76, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 42.59
Std Dev 3.687
Gaus mean : 43.5325
Gaus Width: 3.9699
Entry
ampl
0
1
2
3
4
5
6
7
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0
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20
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40
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60
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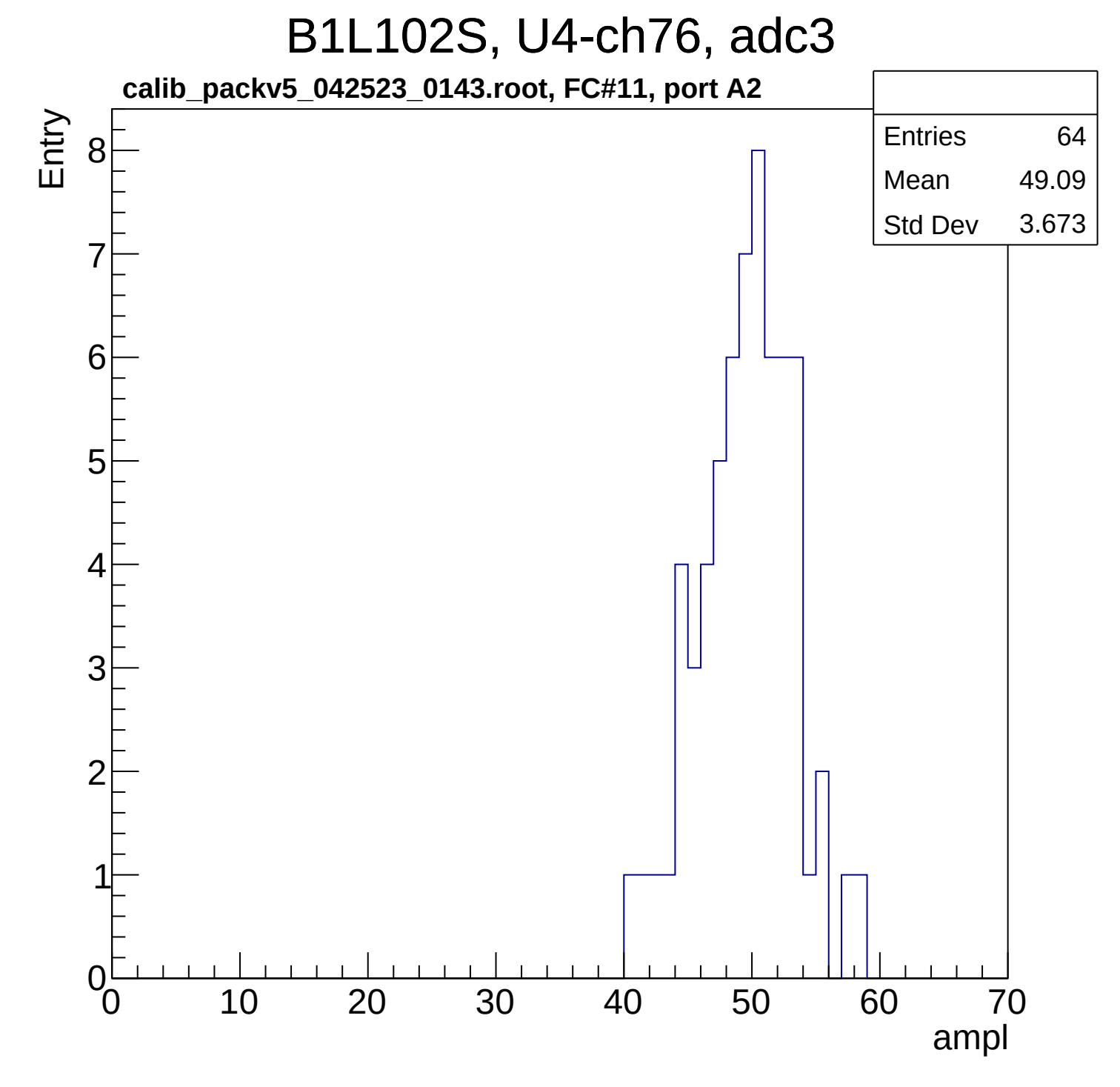
B1L102S, U4-ch76, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 49.09
Std Dev 3.673
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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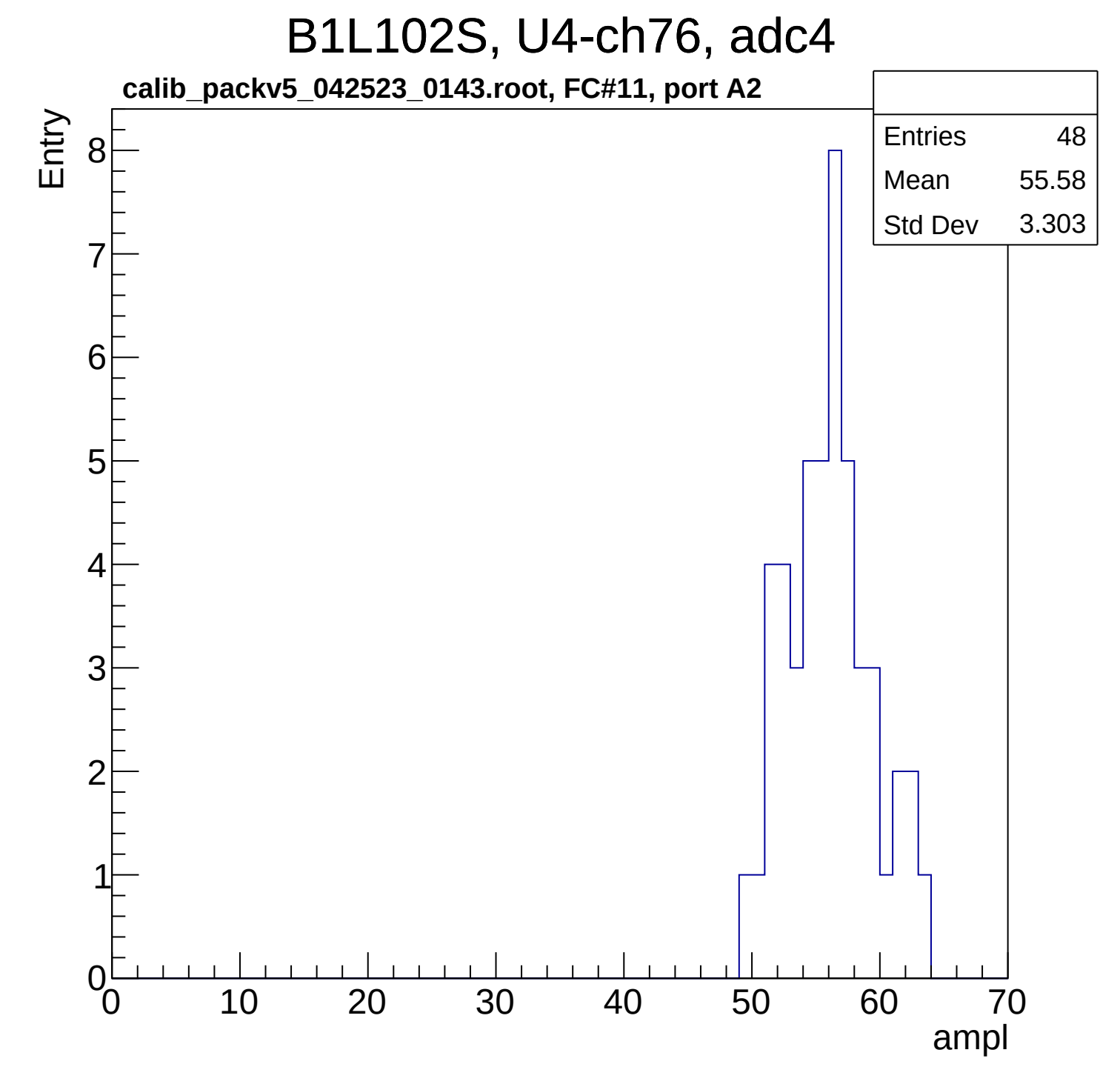
40
50
60
70


B1L102S, U4-ch76, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 48
Mean 55.58
Std Dev 3.303
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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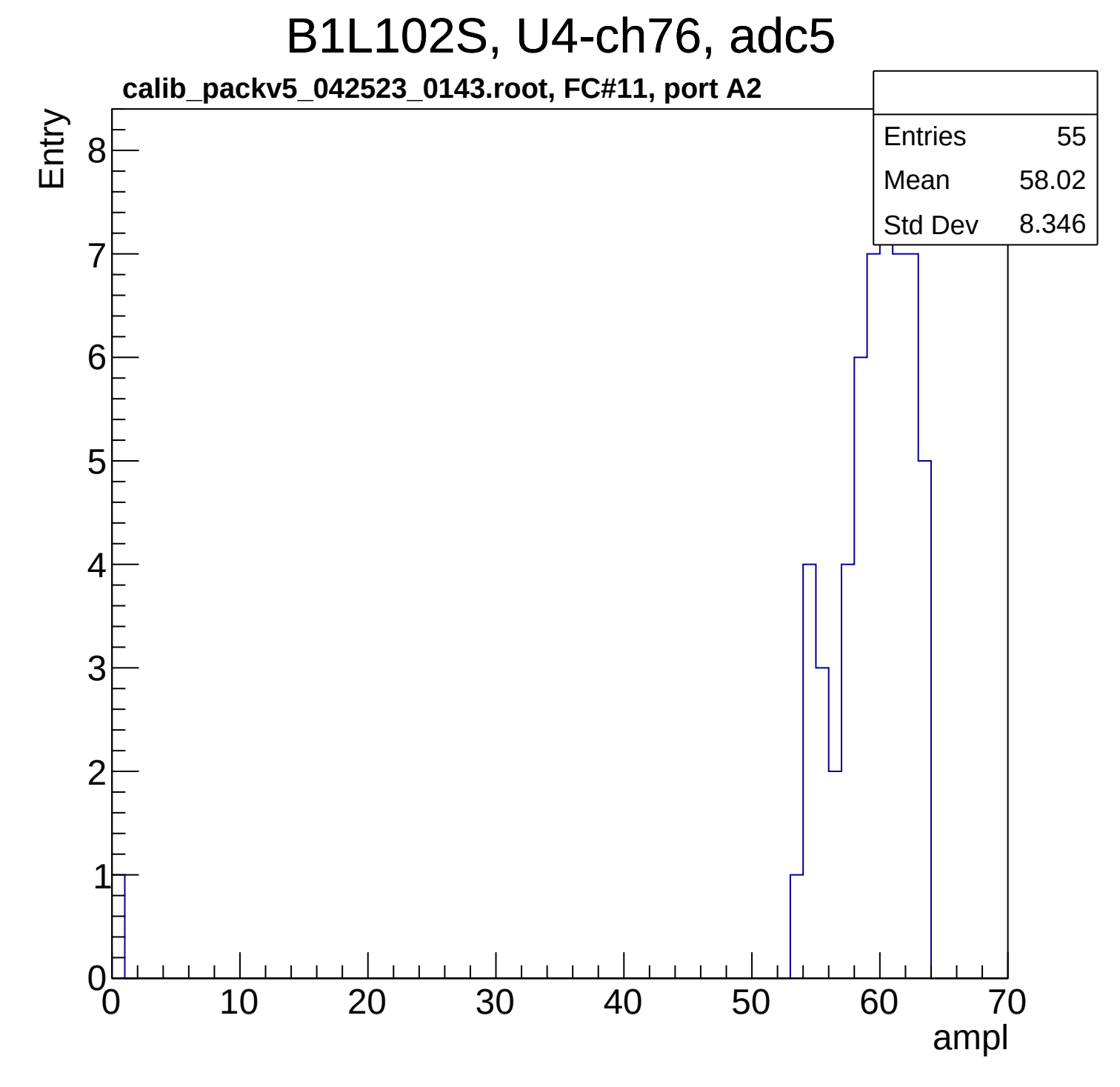
B1L102S, U4-ch76, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 58.02
Std Dev 8.346
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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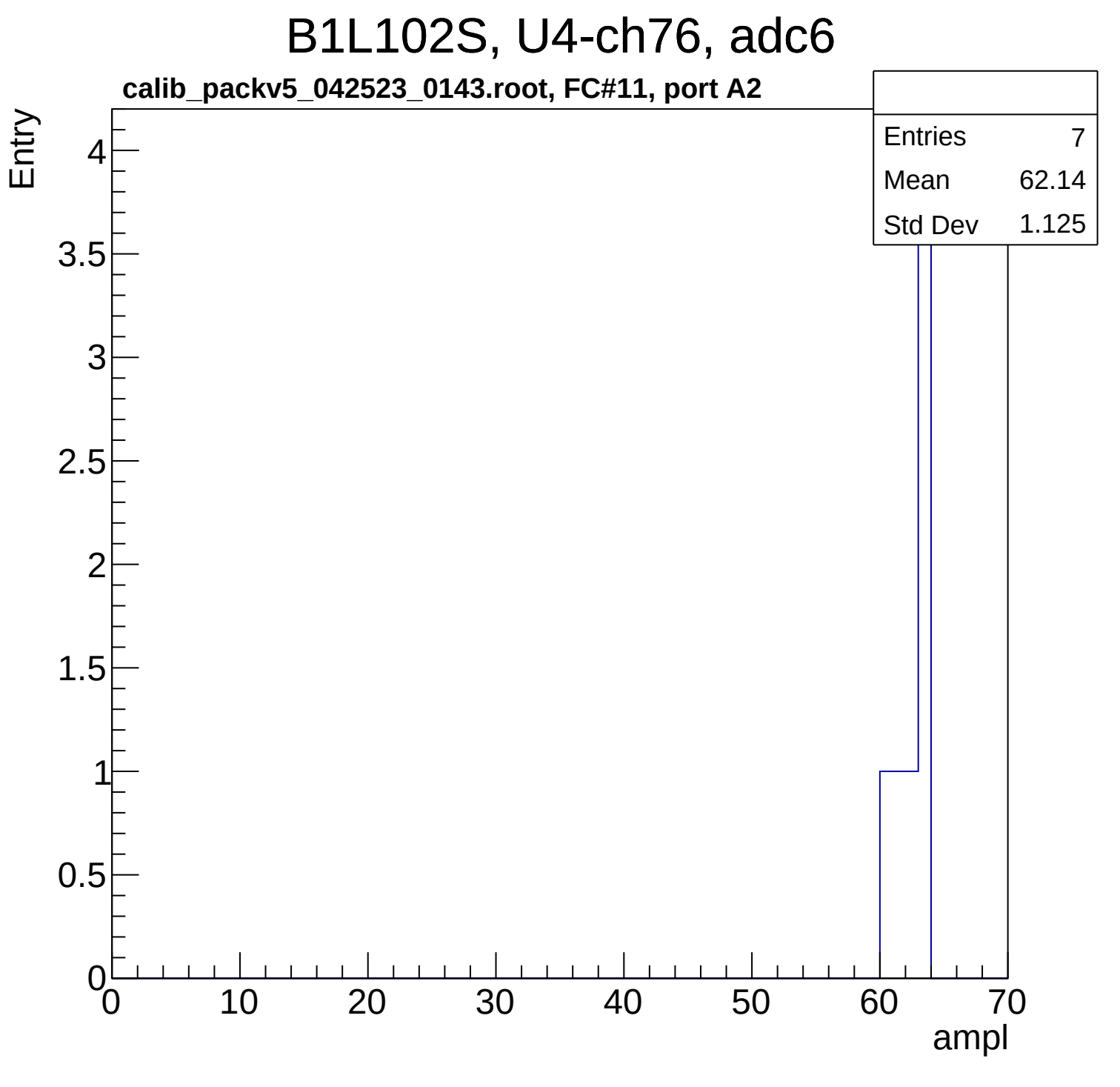
B1L102S, U4-ch76, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 7
Mean 62.14
Std Dev 1.125
Entry
ampl
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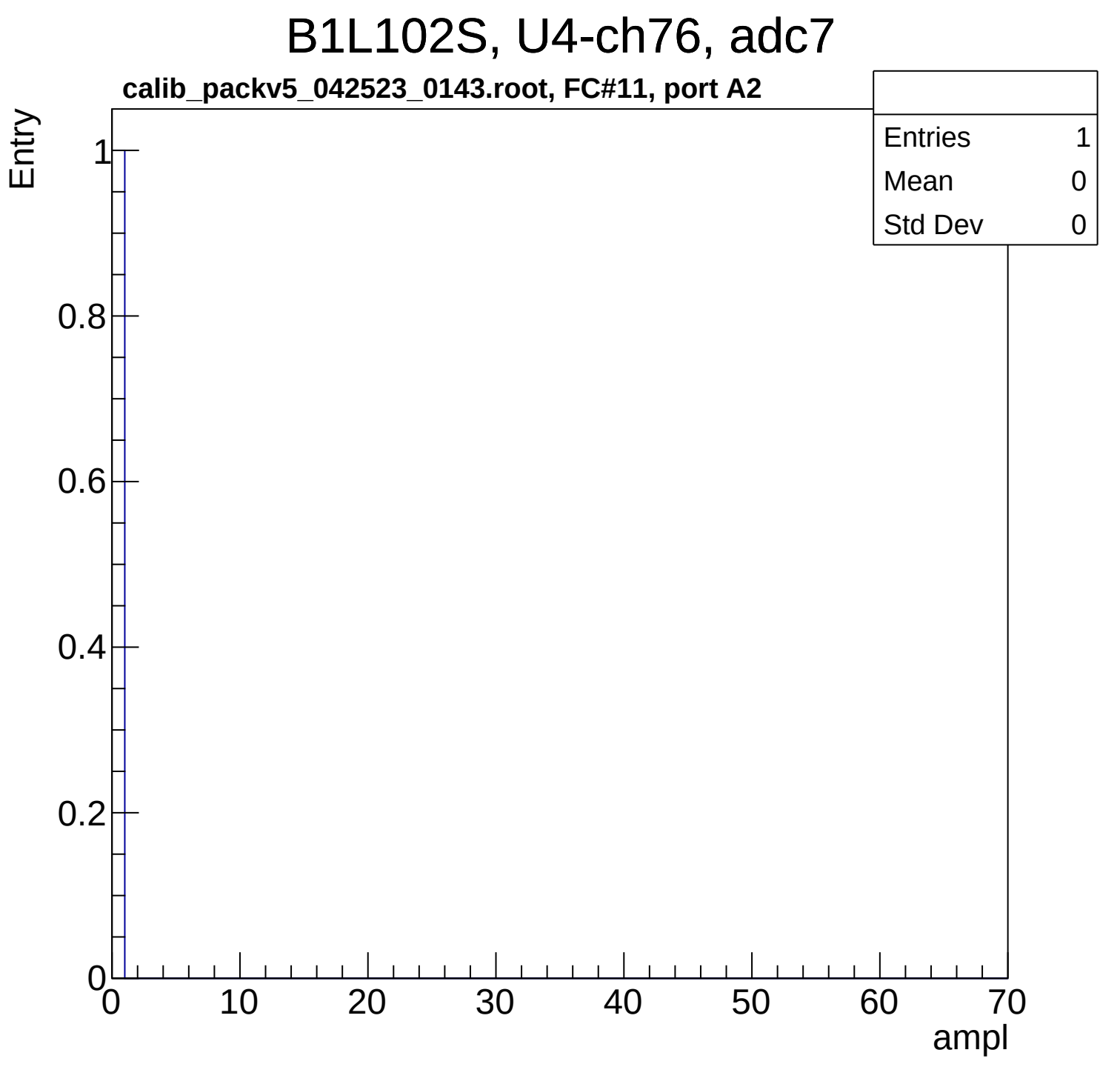
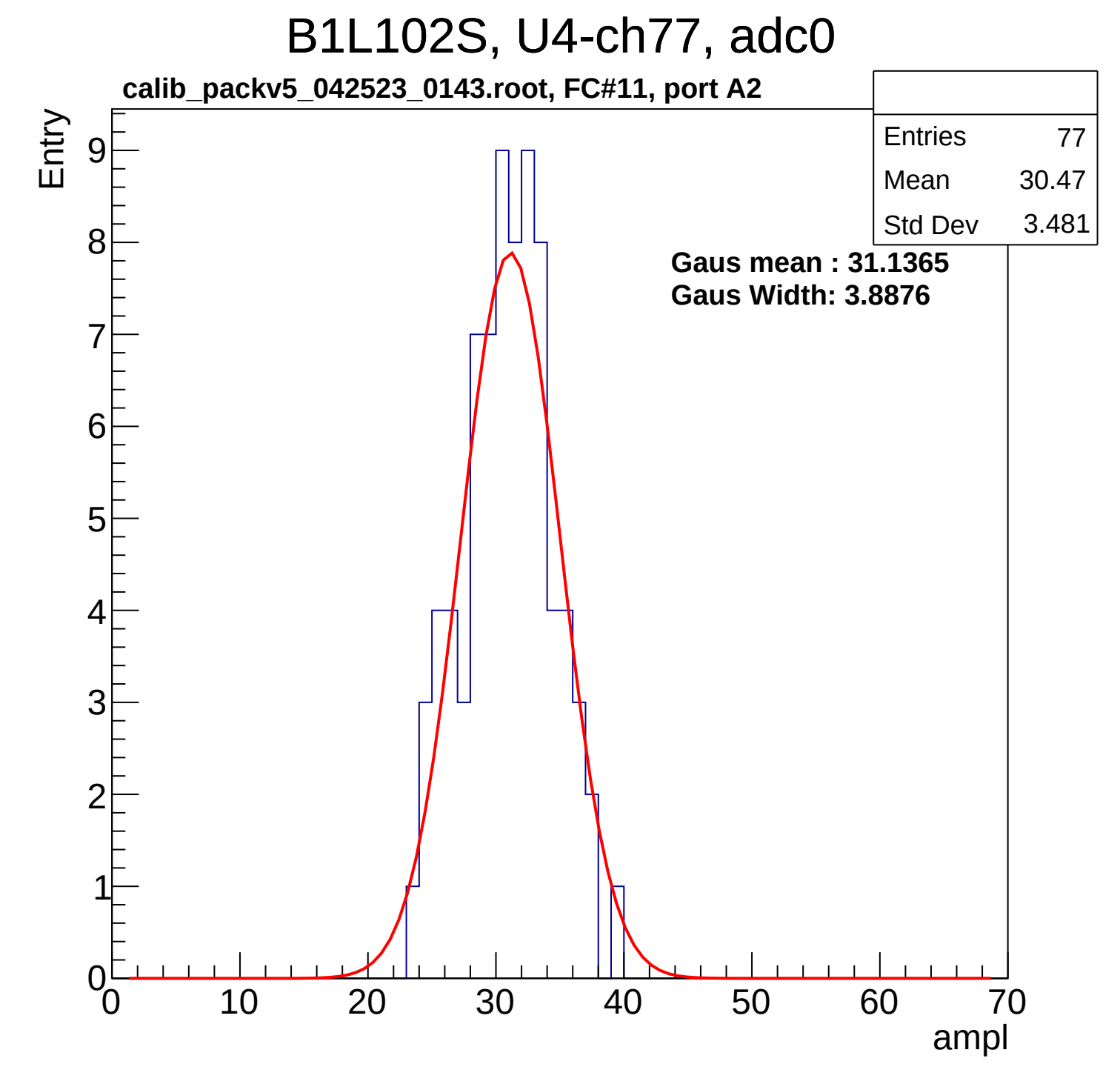
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U4-ch76, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch77, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 77
Mean 30.47
Std Dev 3.481
Gaus mean : 31.1365
Gaus Width: 3.8876
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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60
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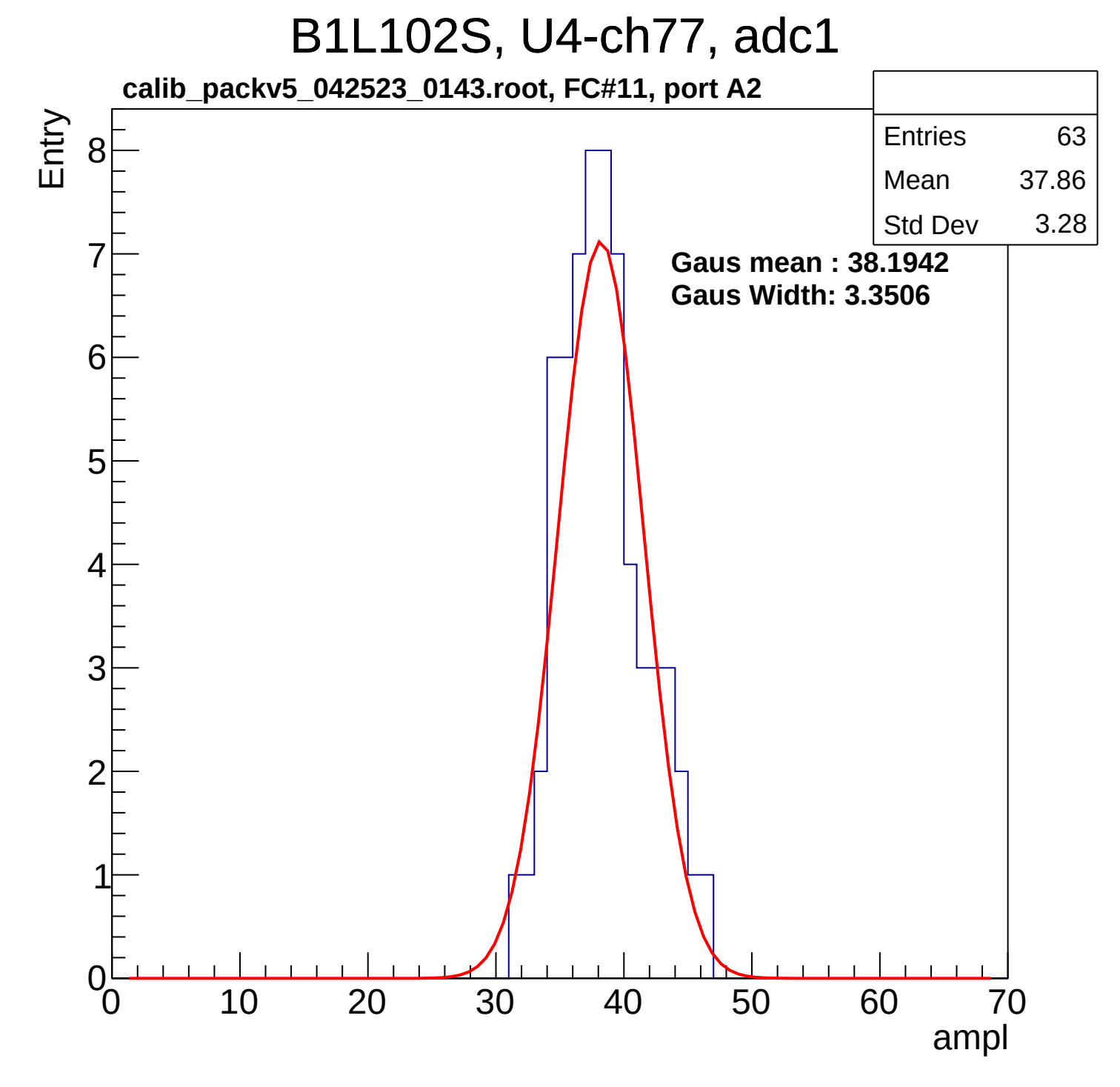
B1L102S, U4-ch77, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 37.86
Std Dev 3.28
Gaus mean : 38.1942
Gaus Width: 3.3506
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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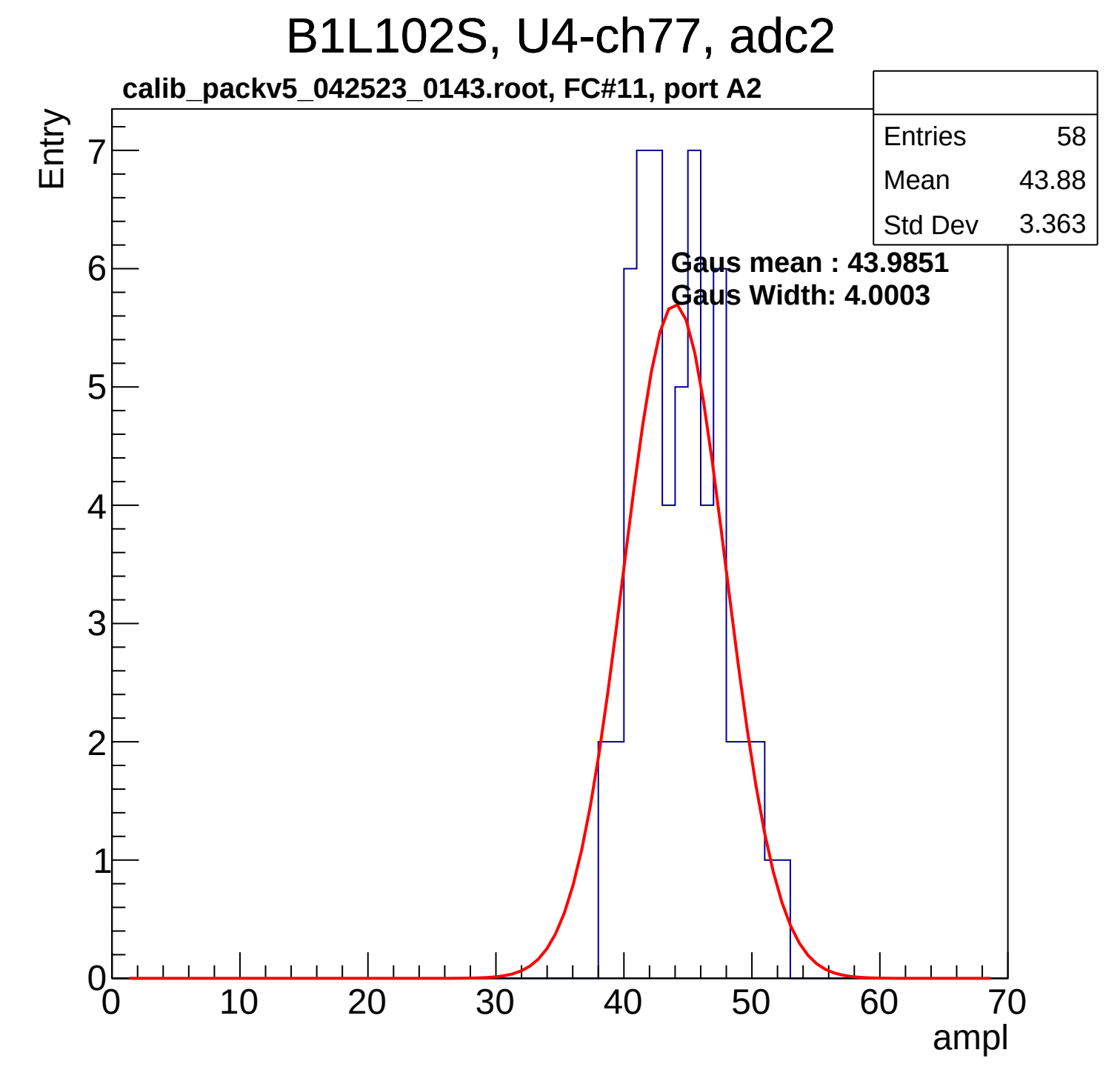
40
50
60
70


B1L102S, U4-ch77, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 43.88
Std Dev 3.363
Gaus mean : 43.9851
Gaus Width: 4.0003
Entry
ampl
0
1
2
3
4
5
6
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0
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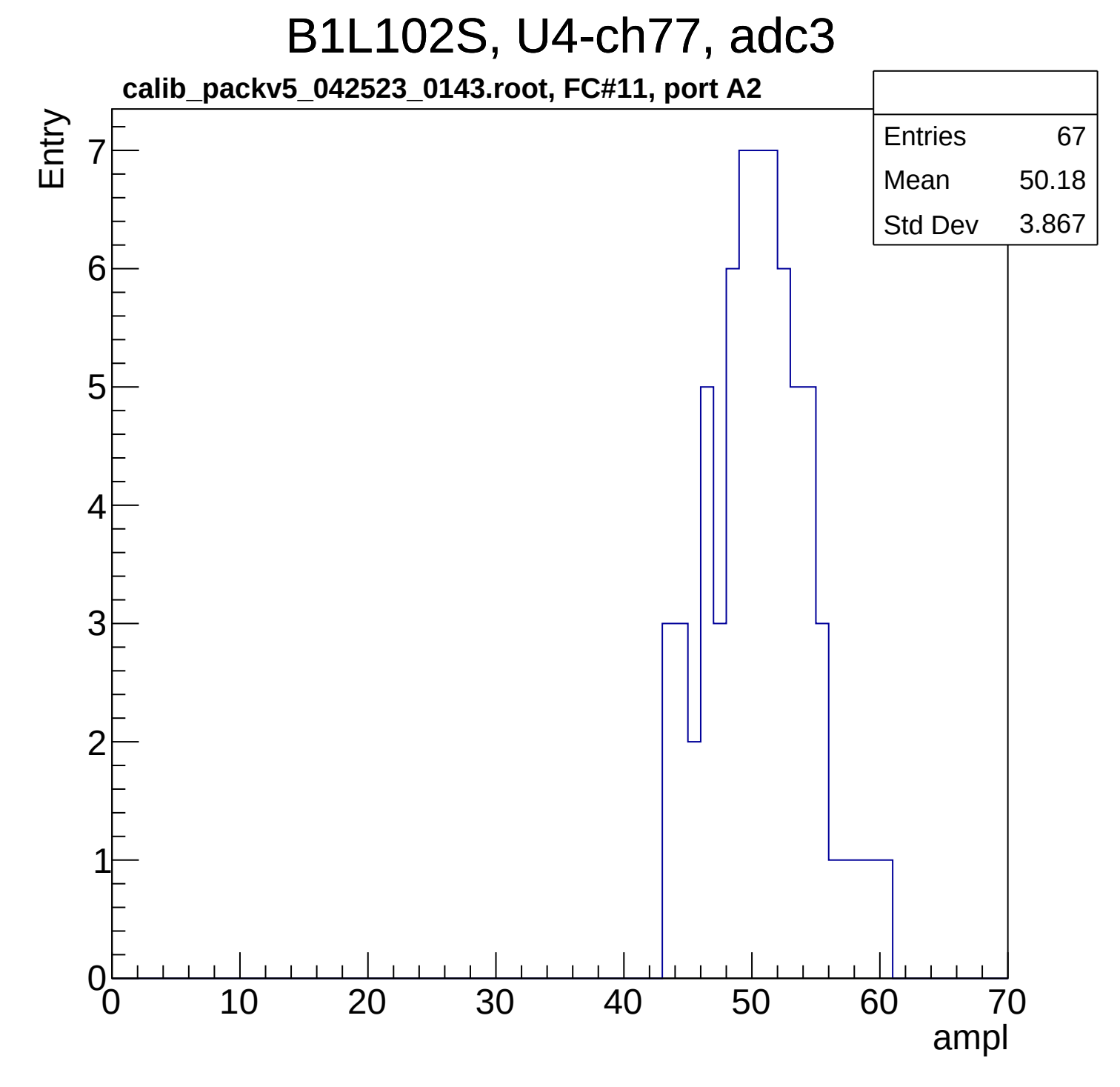
B1L102S, U4-ch77, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 50.18
Std Dev 3.867
Entry
ampl
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1
2
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4
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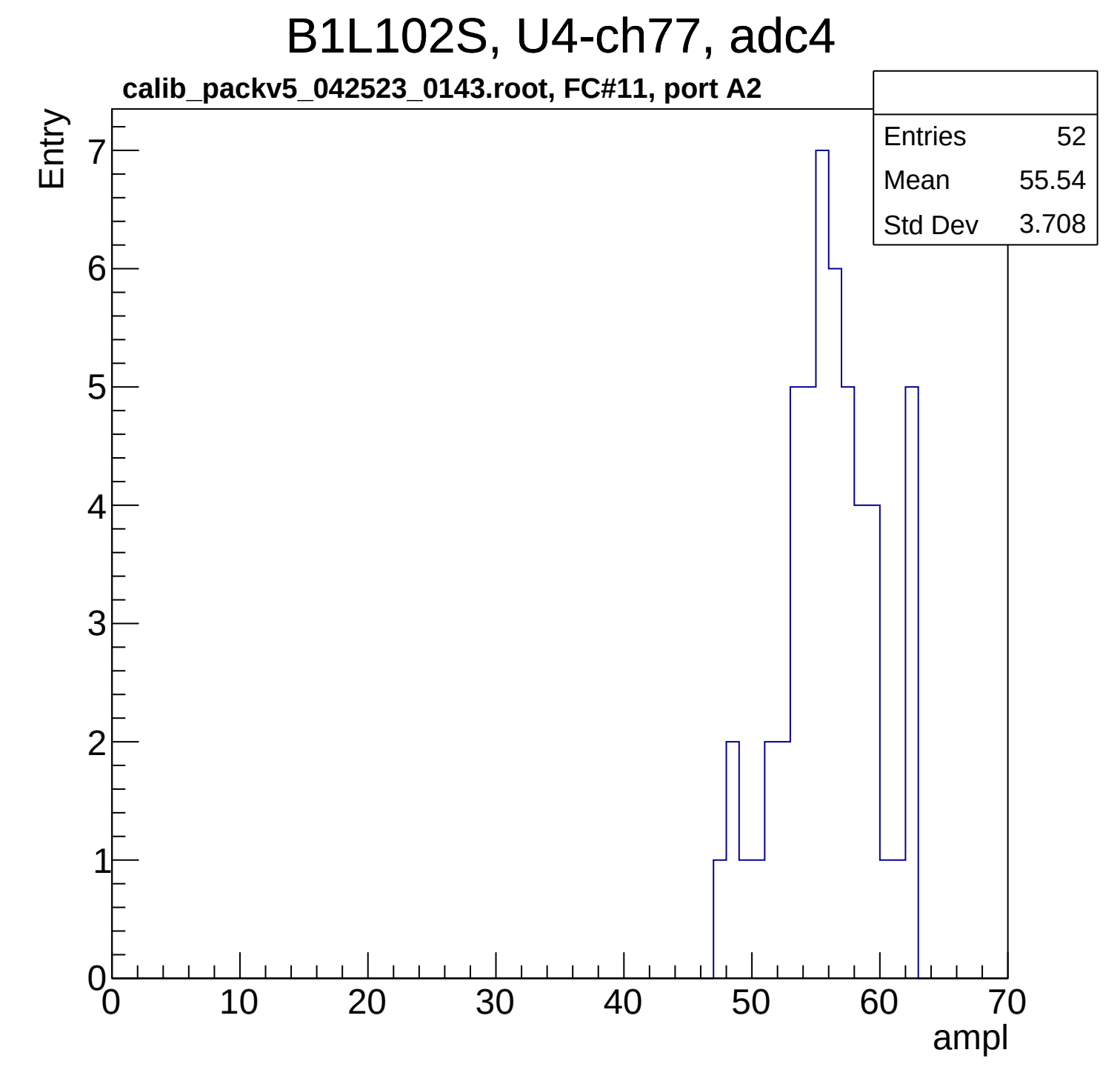
B1L102S, U4-ch77, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 52
Mean 55.54
Std Dev 3.708
Entry
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1
2
3
4
5
6
7
0
10
20
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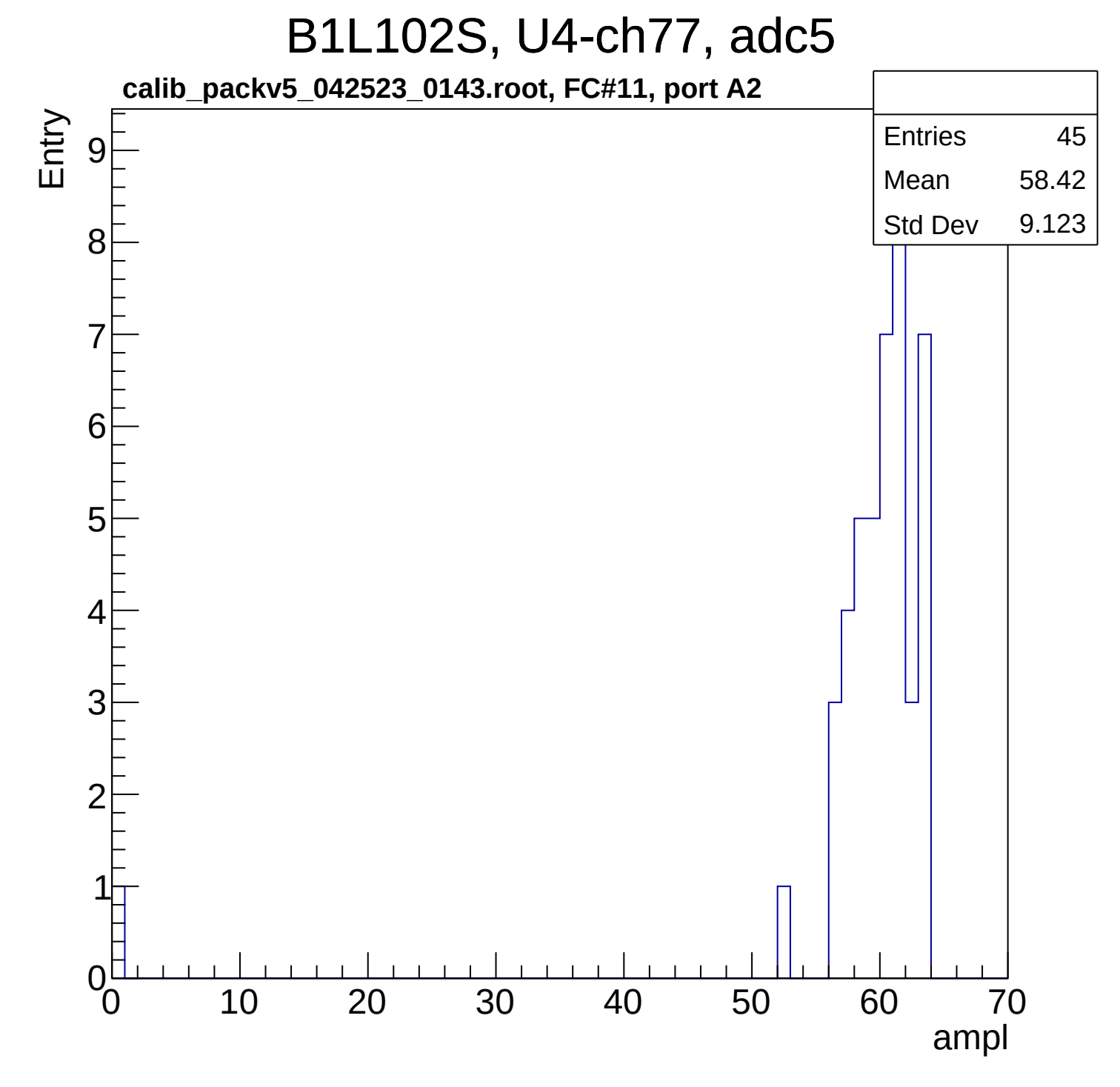
50
60
70
ampl


B1L102S, U4-ch77, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 45
Mean 58.42
Std Dev 9.123
Entry
0
1
2
3
4
5
6
7
8
9
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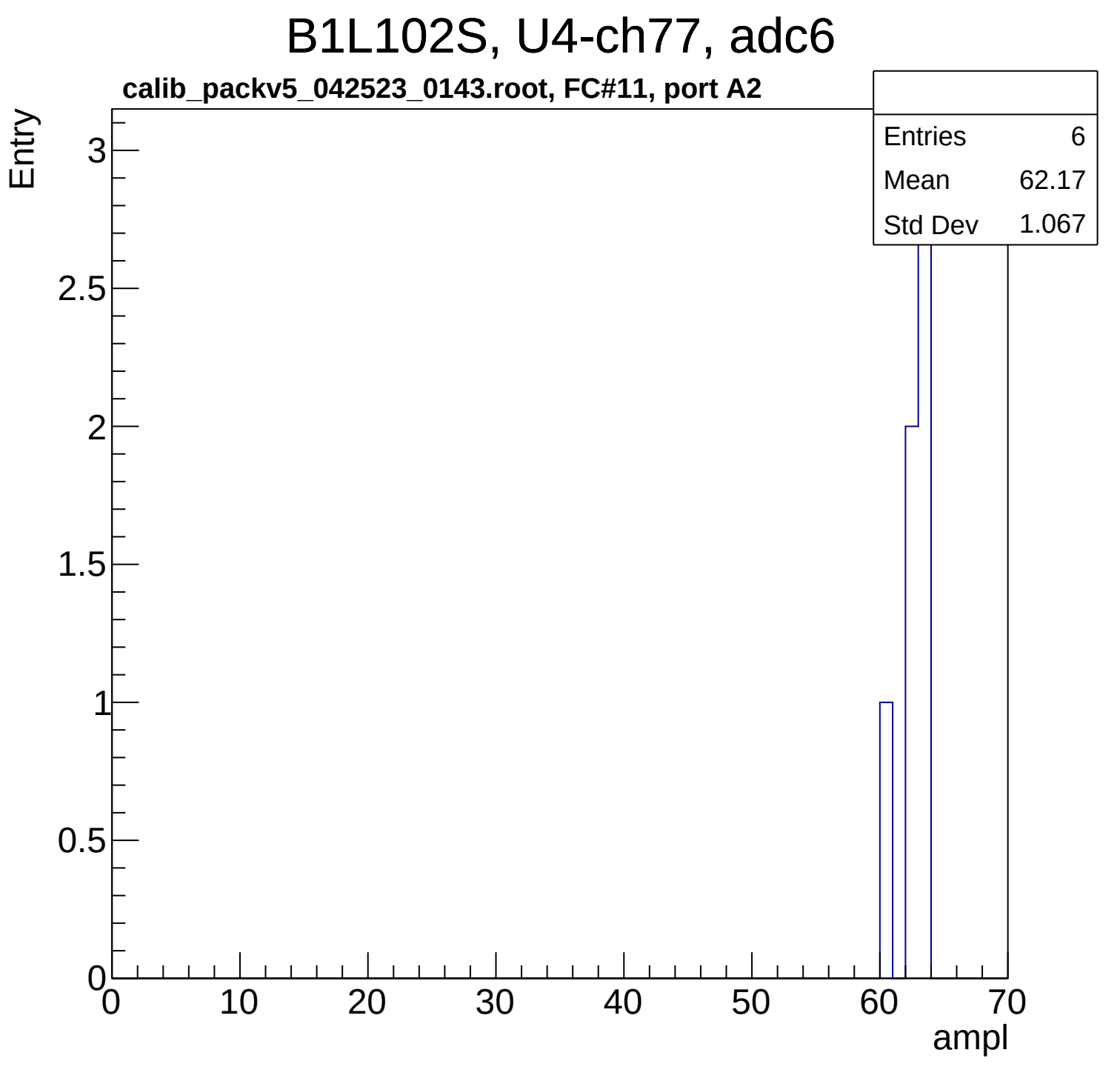
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch77, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 6
Mean 62.17
Std Dev 1.067
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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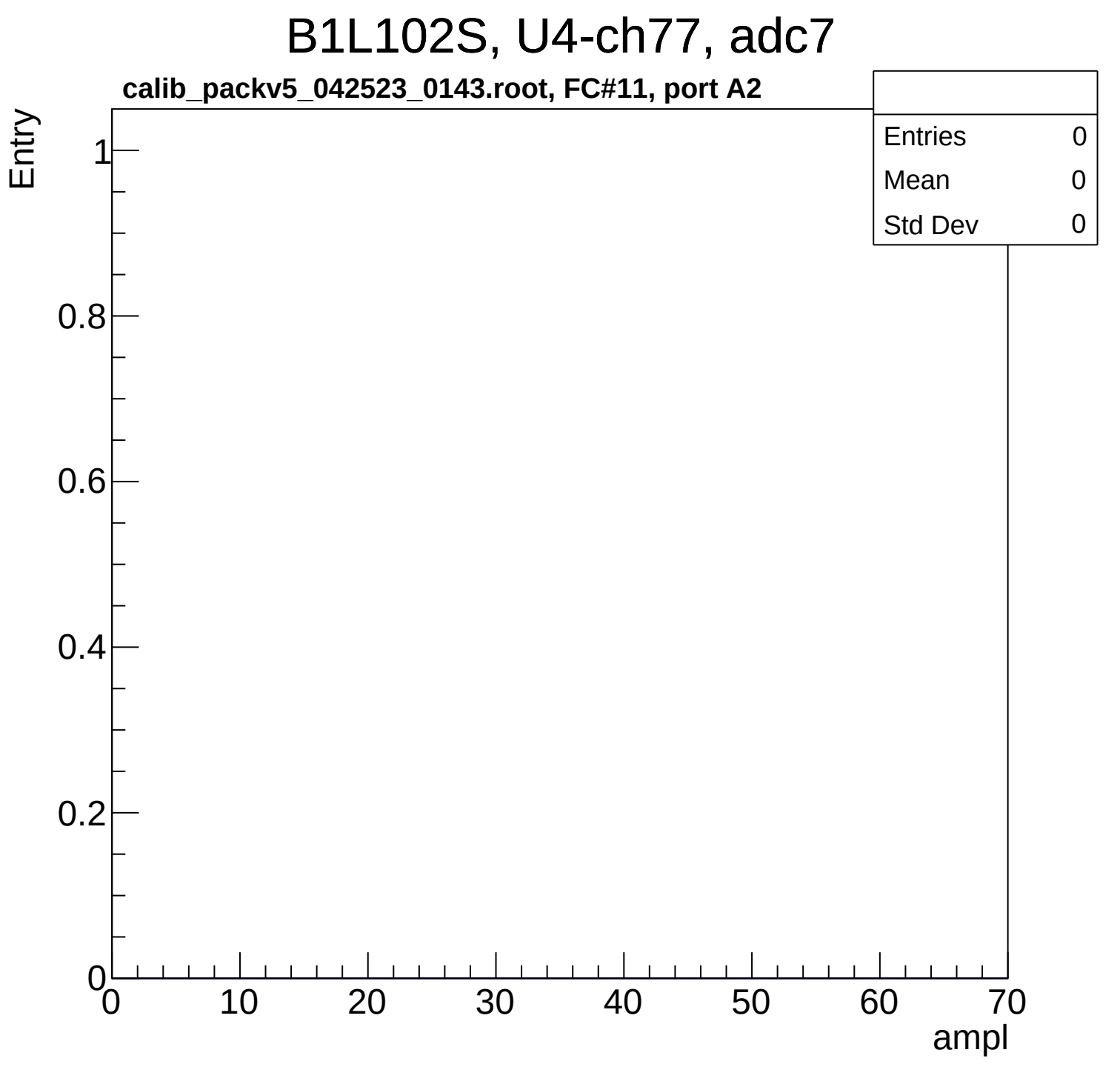
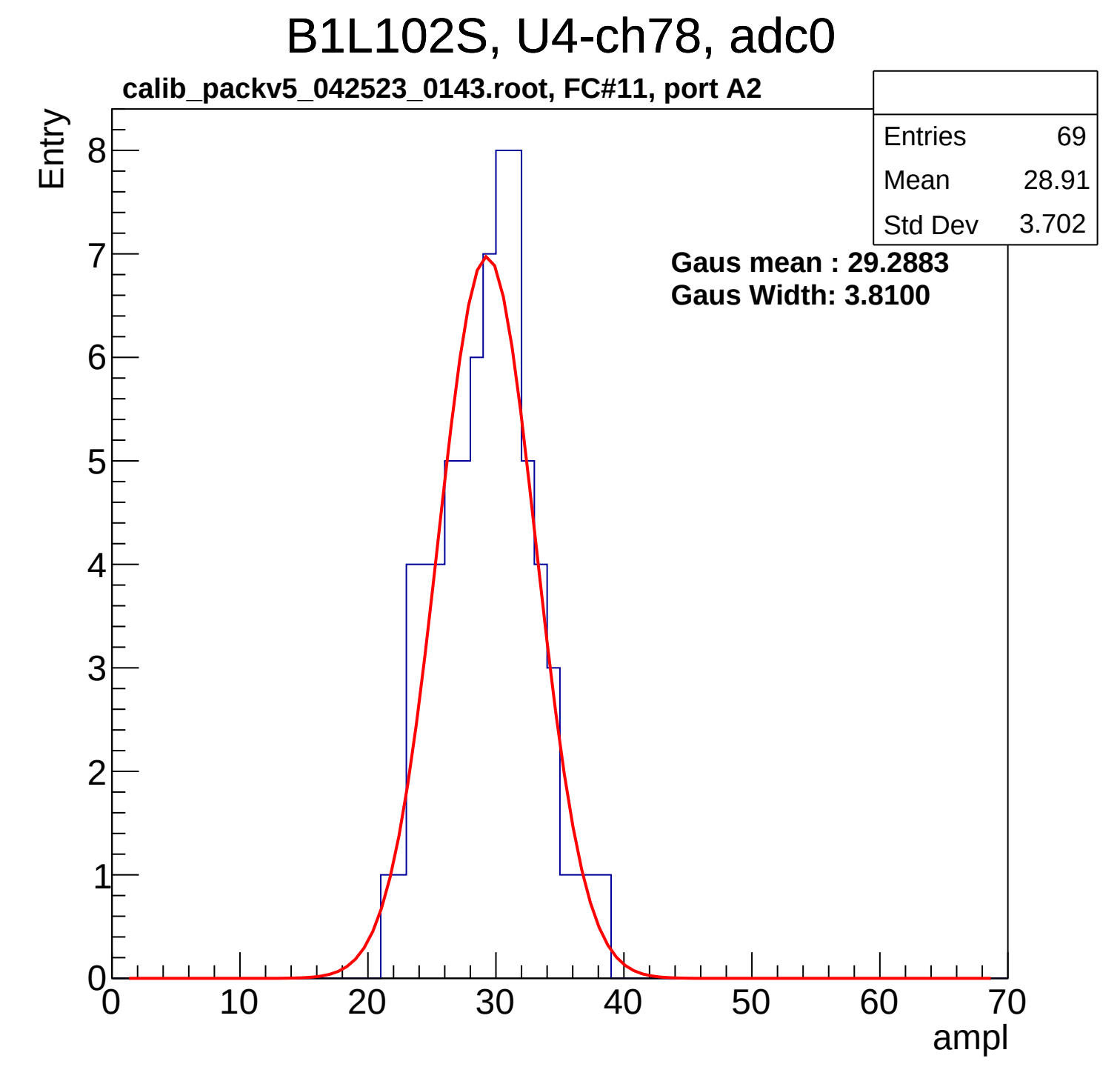

B1L102S, U4-ch77, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch78, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 28.91
Std Dev 3.702
Gaus mean : 29.2883
Gaus Width: 3.8100
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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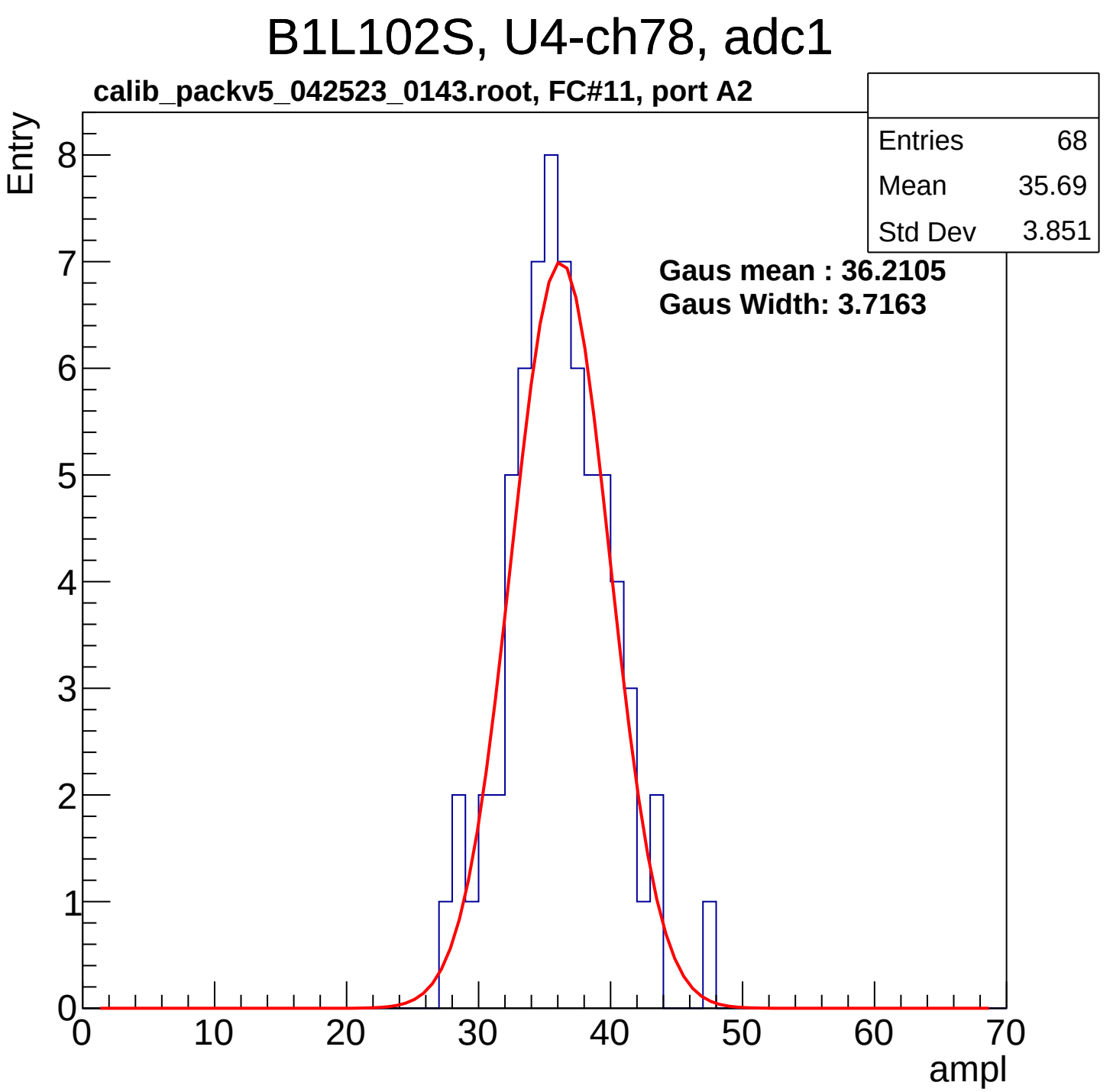
B1L102S, U4-ch78, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 35.69
Std Dev 3.851
Gaus mean : 36.2105
Gaus Width: 3.7163
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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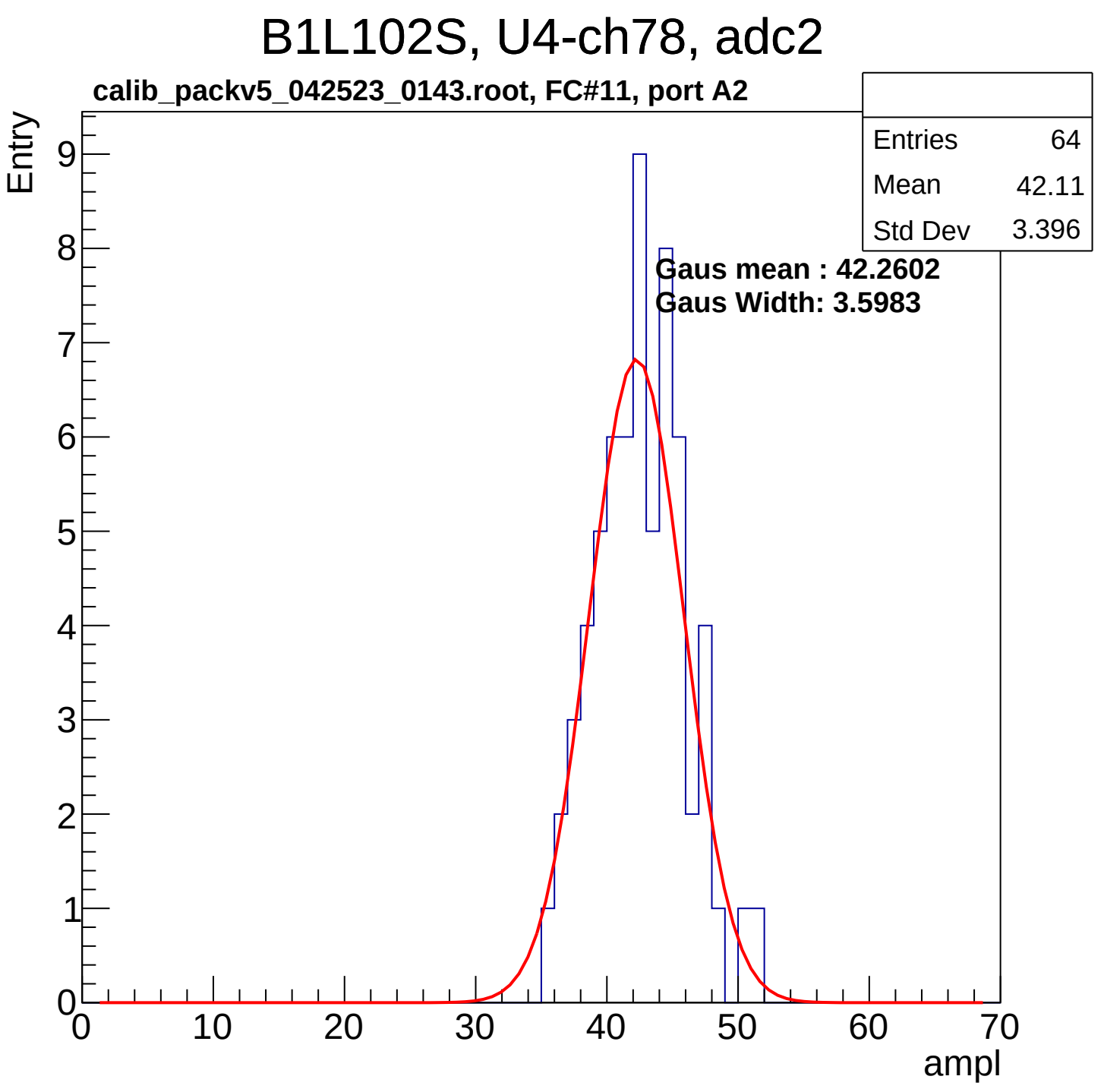
B1L102S, U4-ch78, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 42.11
Std Dev 3.396
Gaus mean : 42.2602
Gaus Width: 3.5983
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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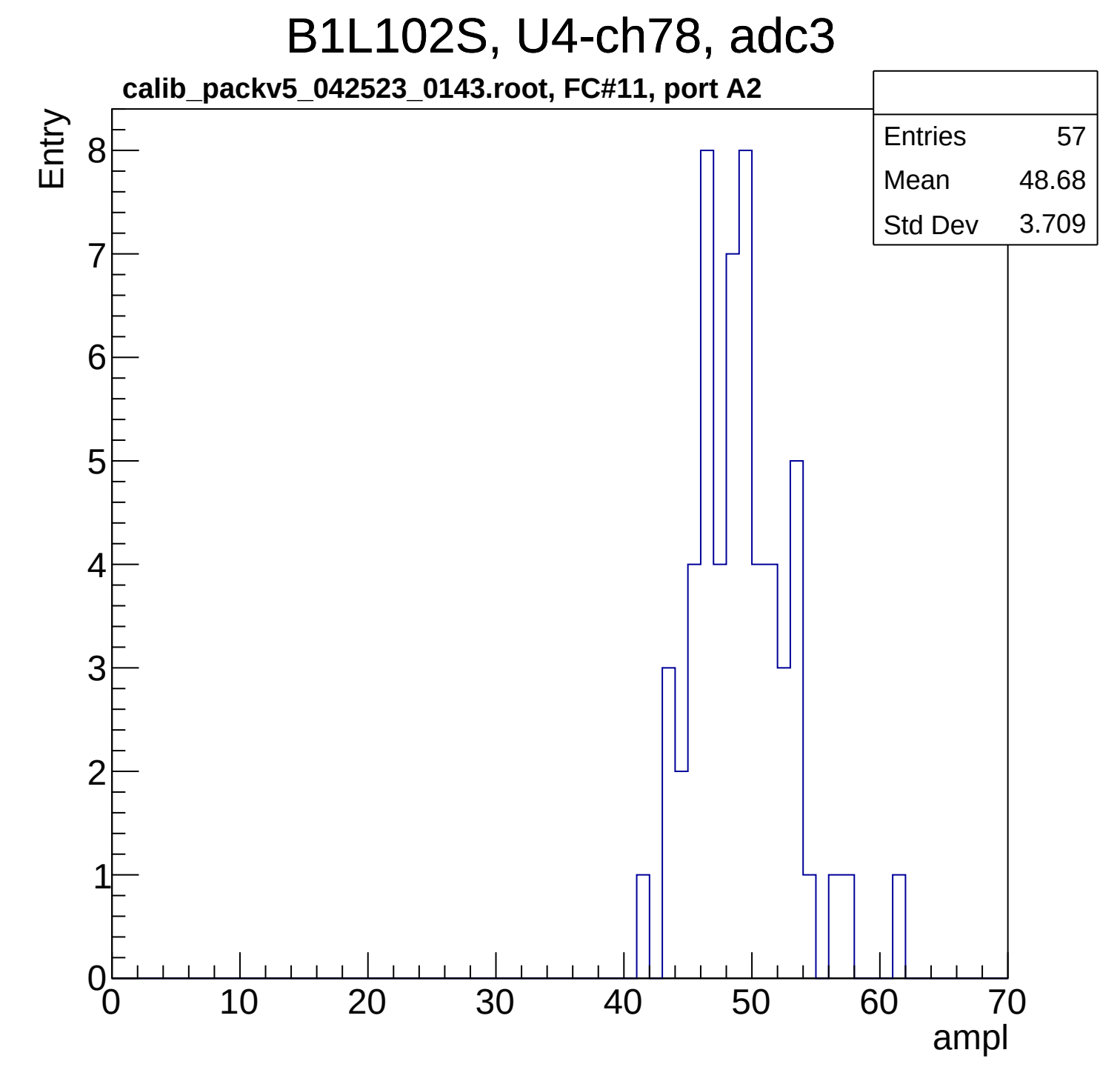
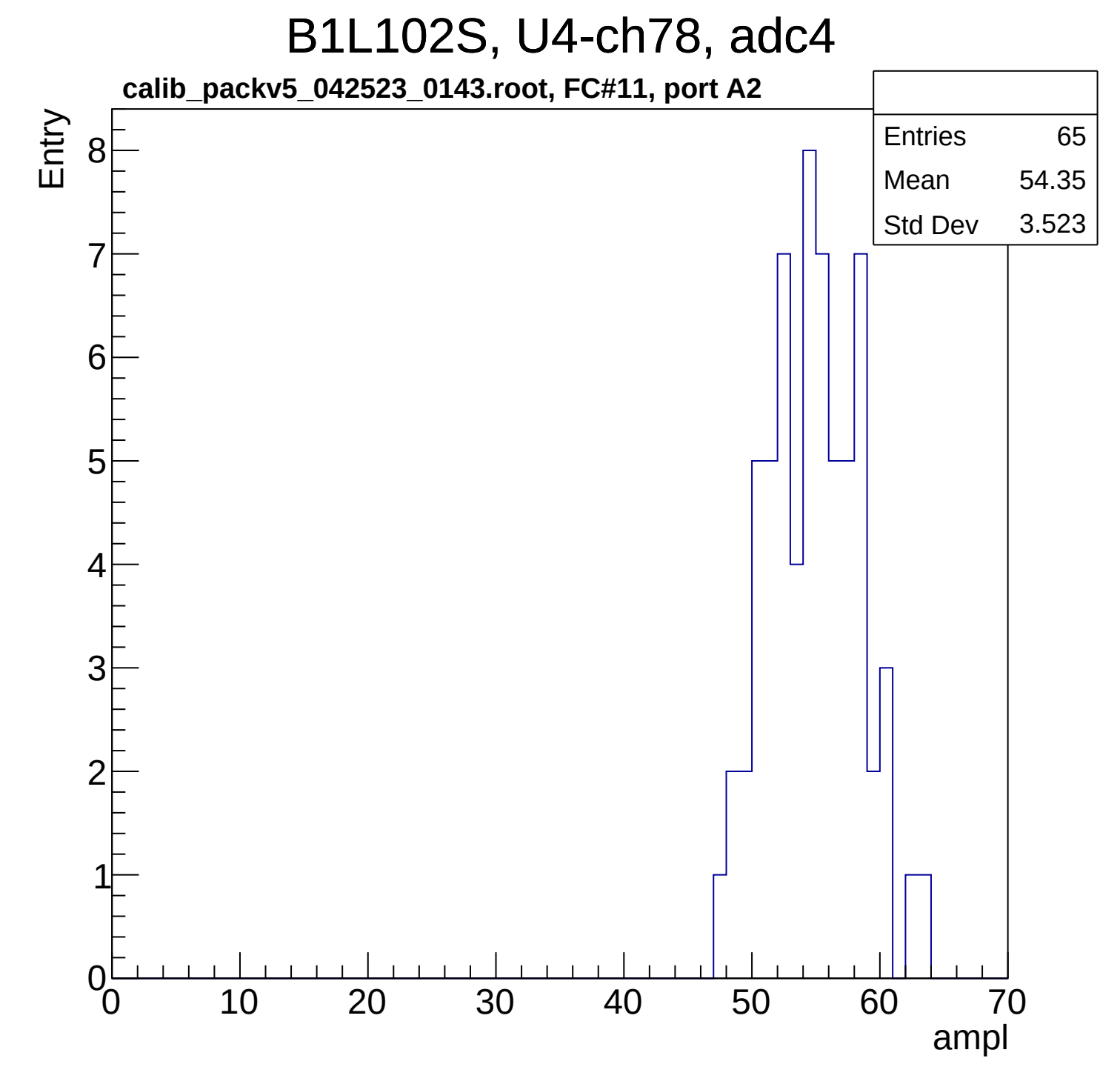

B1L102S, U4-ch78, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 57
Mean 48.68
Std Dev 3.709
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch78, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 54.35
Std Dev 3.523
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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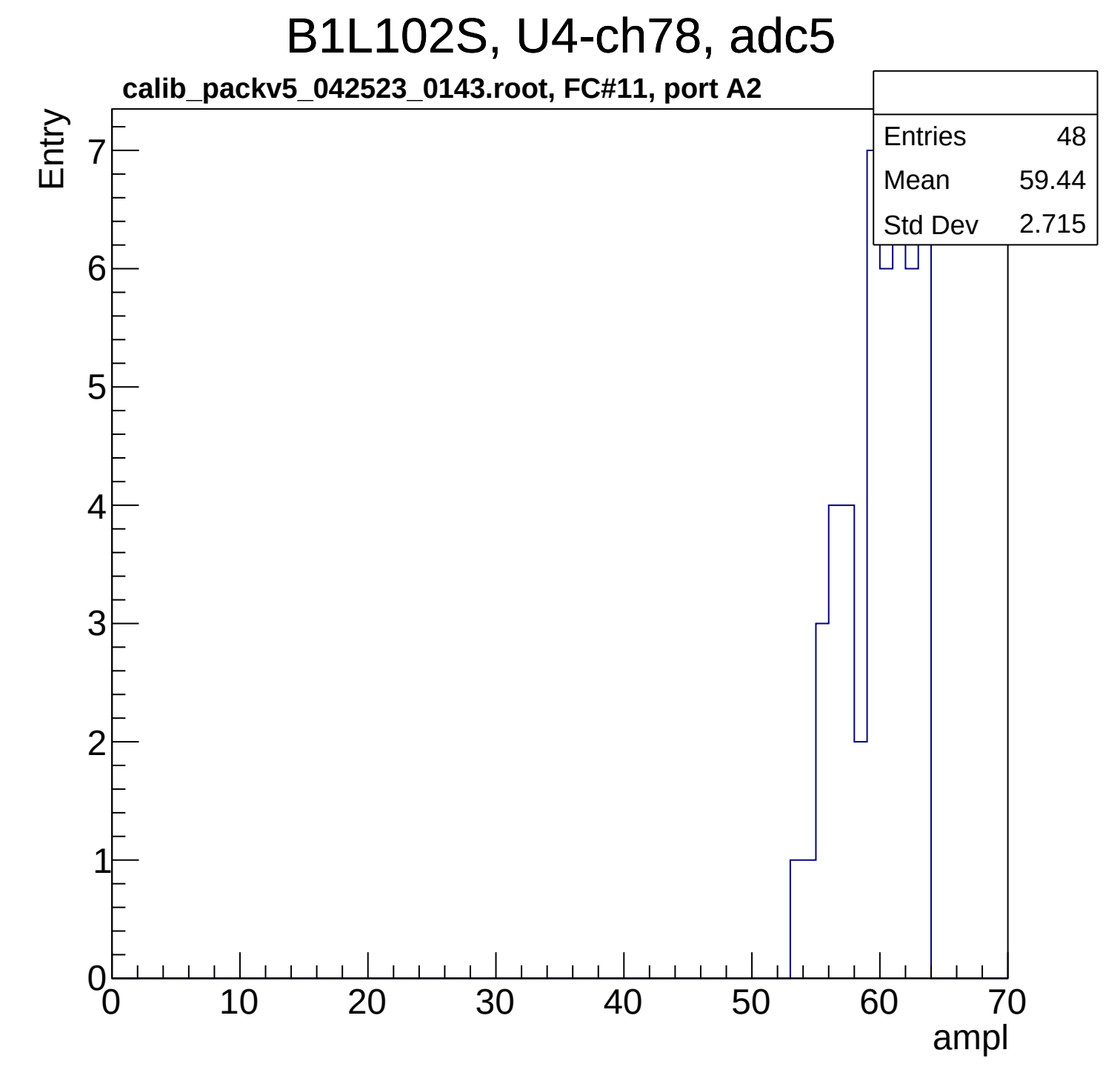
B1L102S, U4-ch78, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 48
Mean 59.44
Std Dev 2.715
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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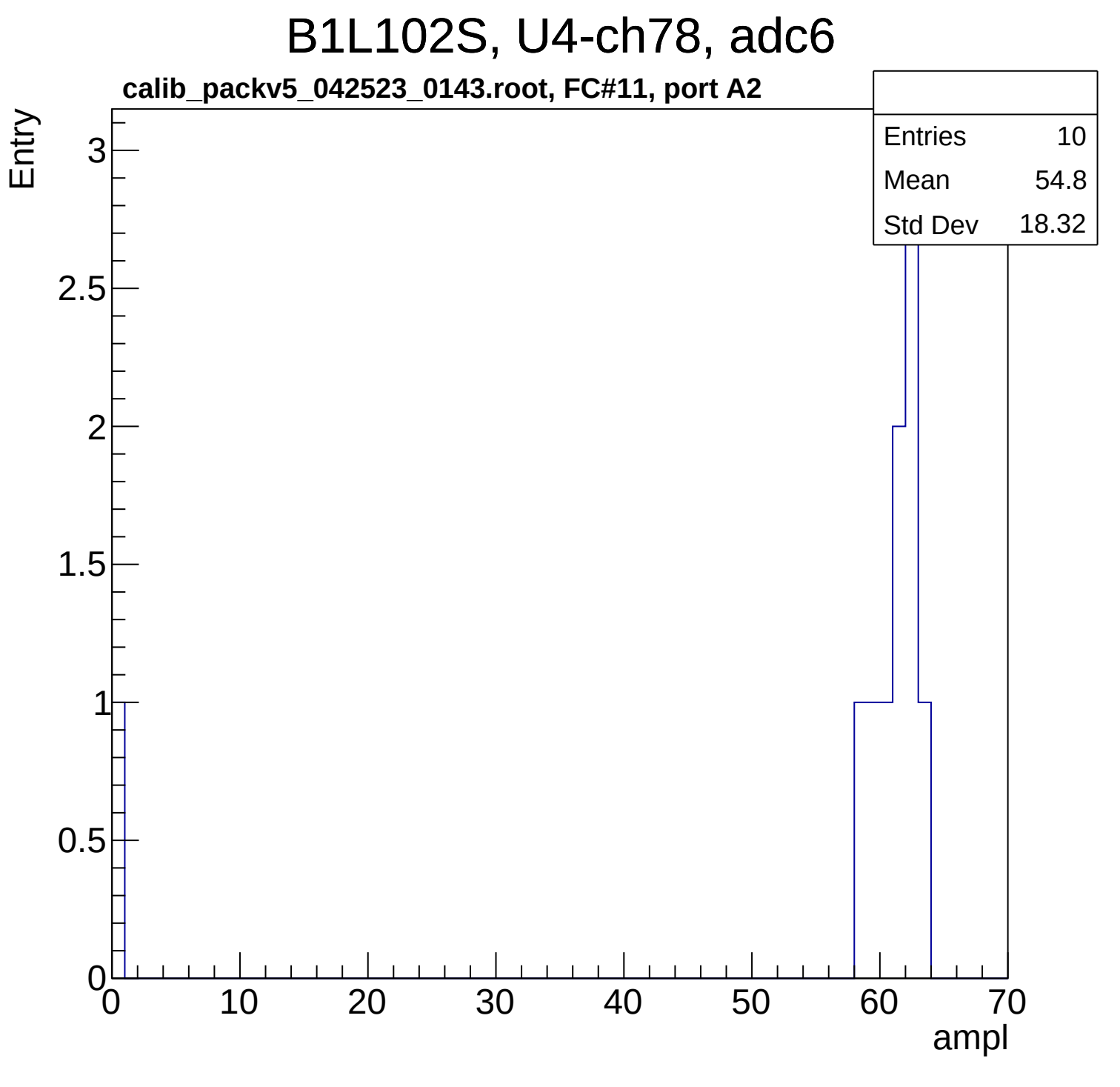
B1L102S, U4-ch78, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 10
Mean 54.8
Std Dev 18.32
Entry
ampl
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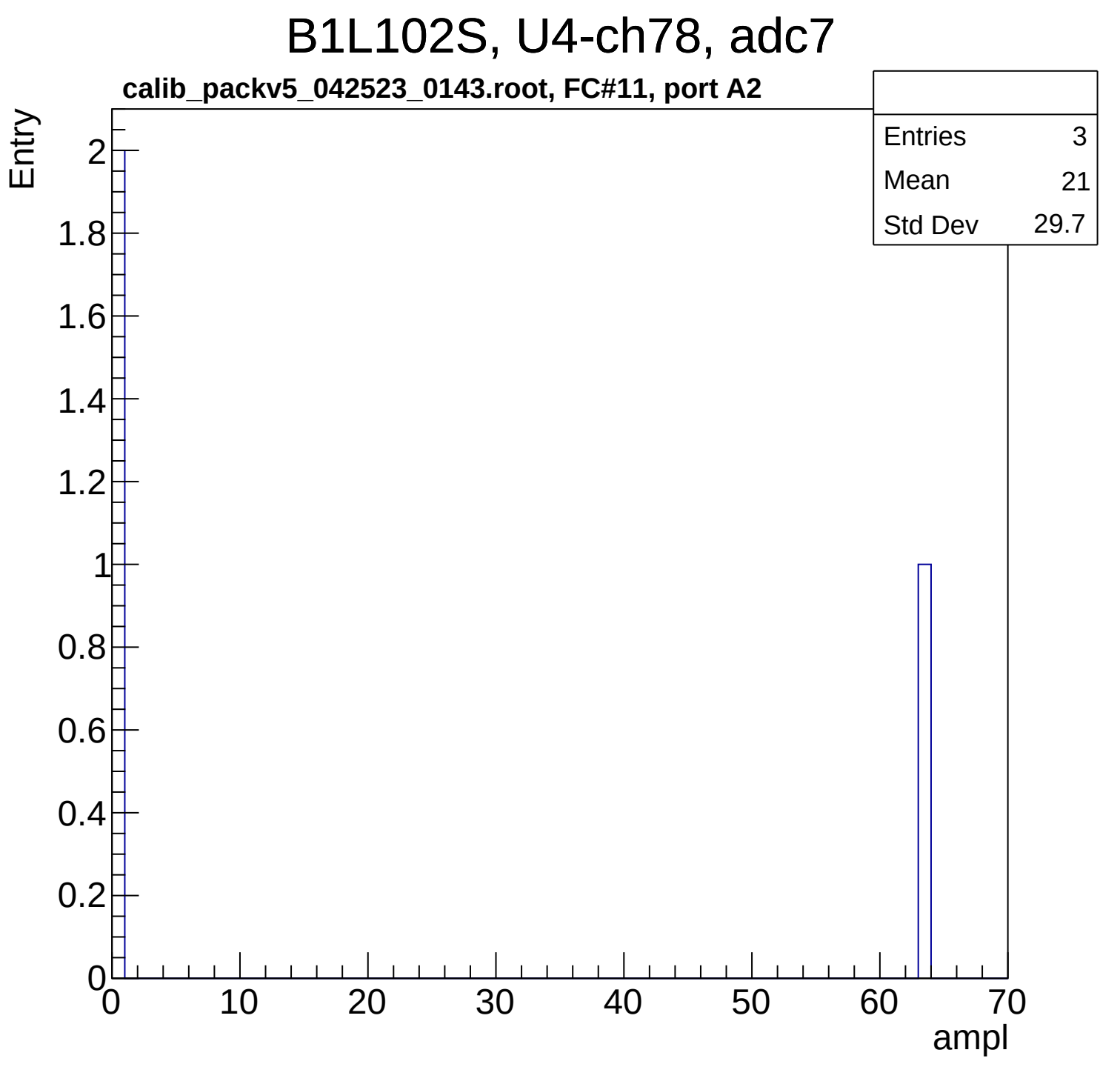
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U4-ch78, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 21
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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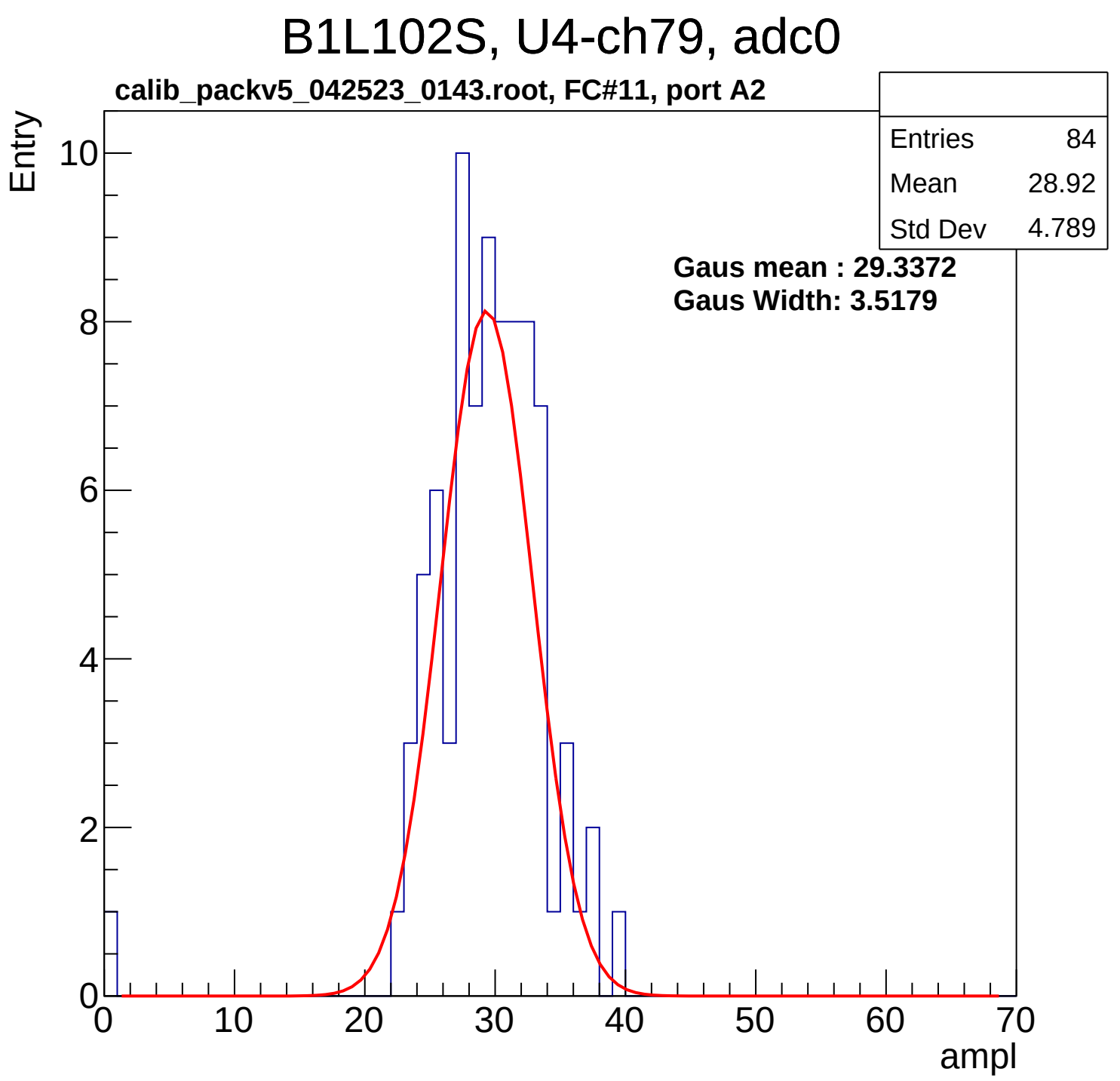
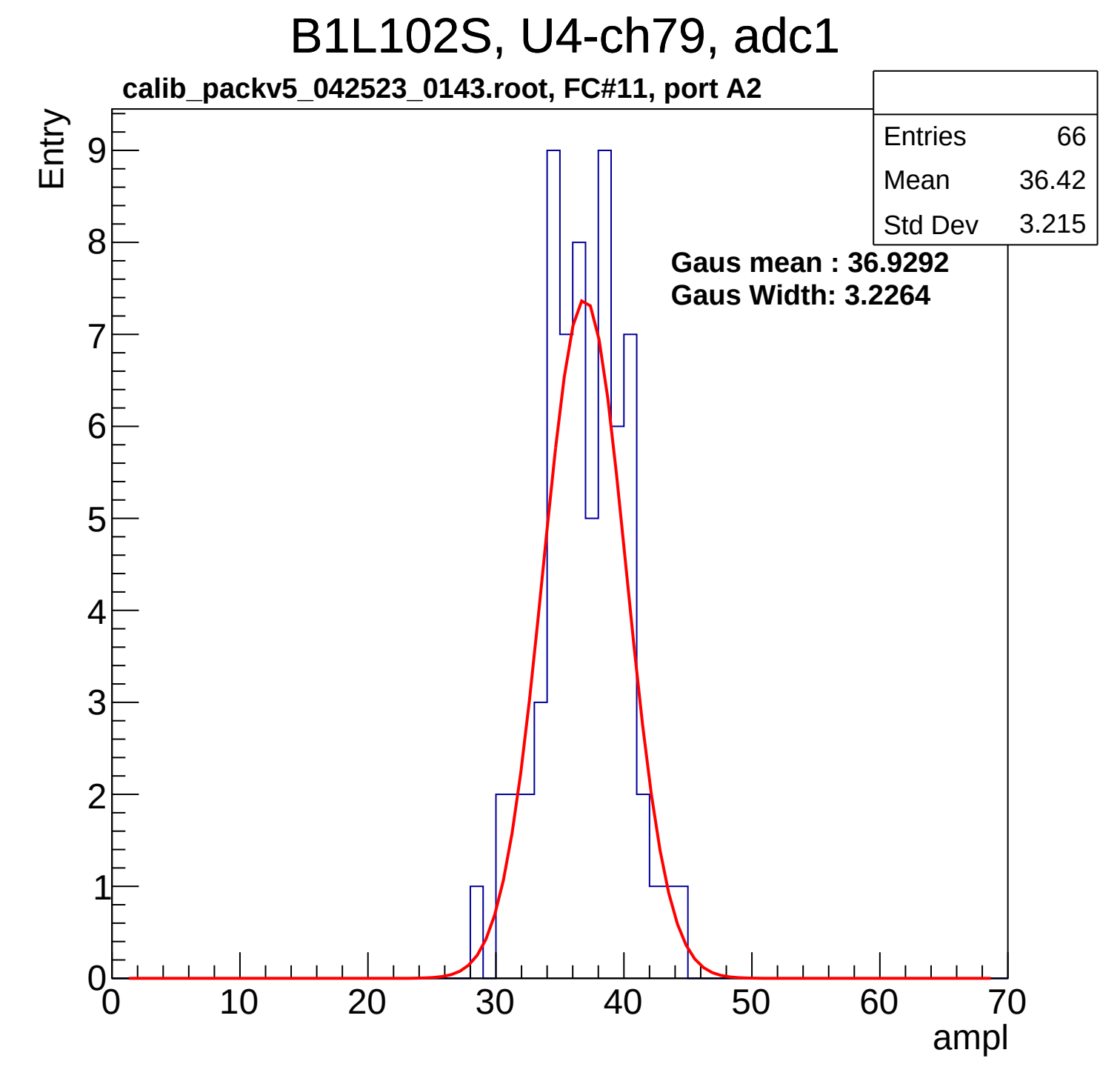

B1L102S, U4-ch79, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 84
Mean 28.92
Std Dev 4.789
Gaus mean : 29.3372
Gaus Width: 3.5179
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch79, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 36.42
Std Dev 3.215
Gaus mean : 36.9292
Gaus Width: 3.2264
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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40
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60
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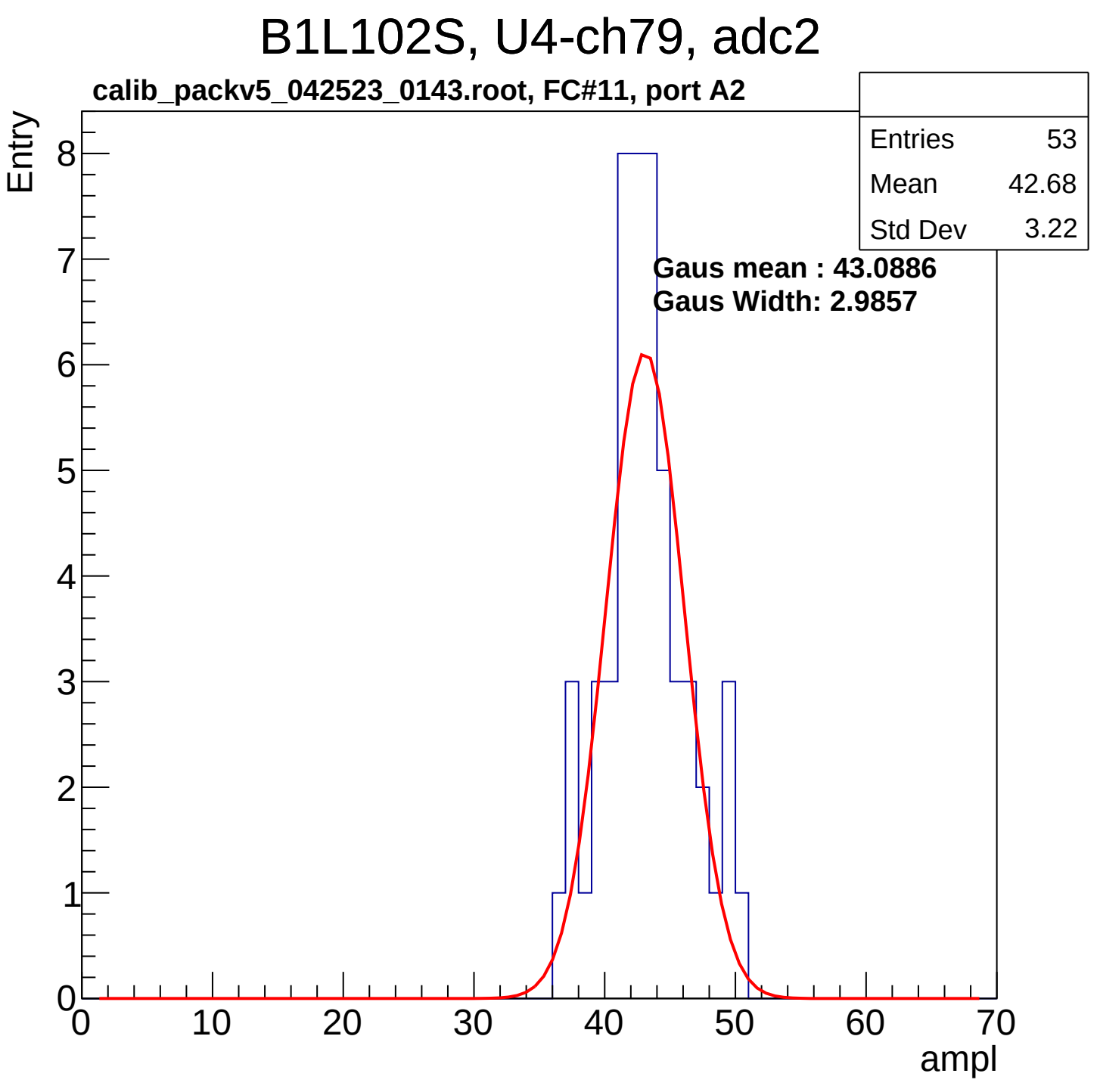
B1L102S, U4-ch79, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 42.68
Std Dev 3.22
Gaus mean : 43.0886
Gaus Width: 2.9857
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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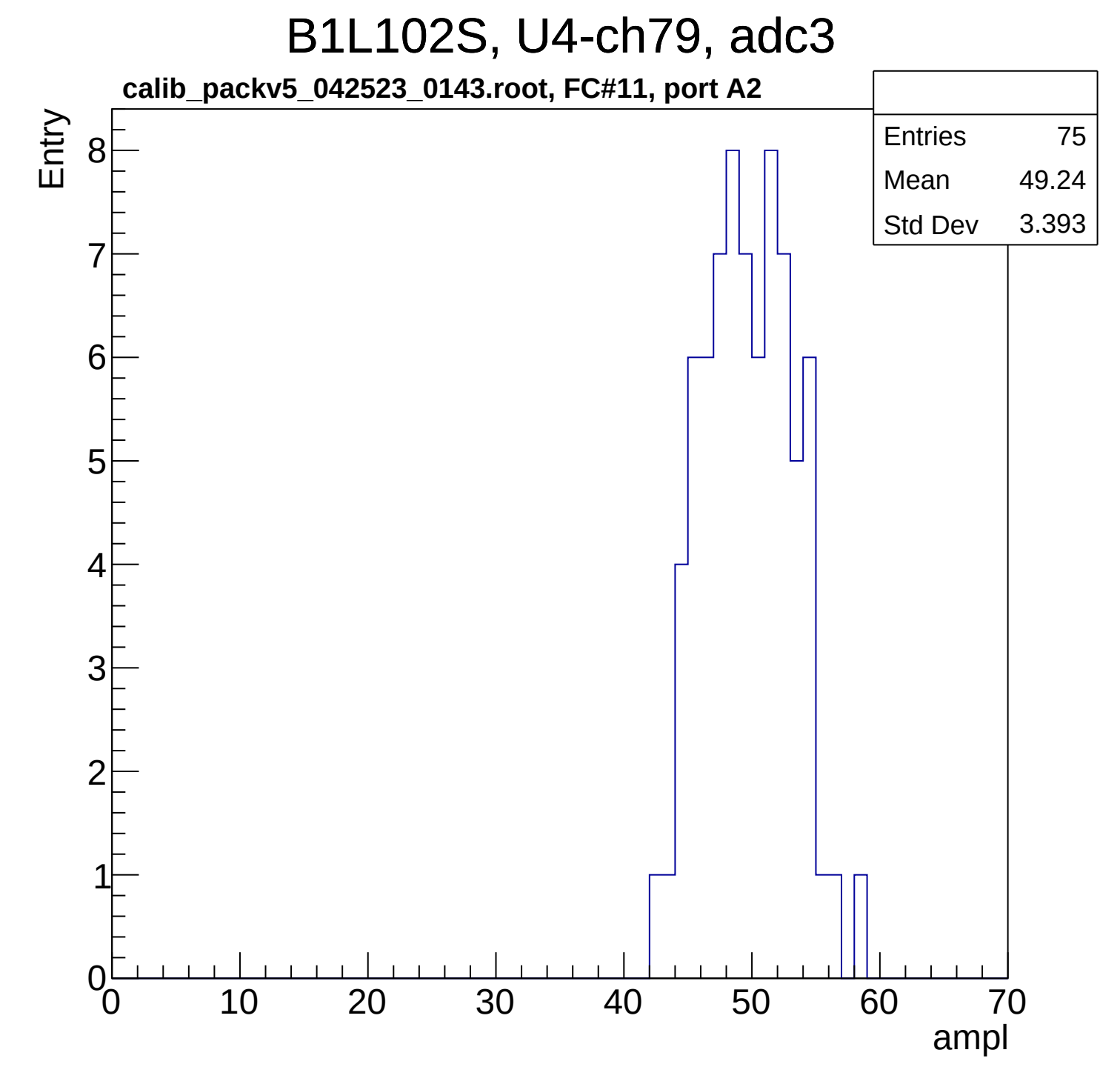
B1L102S, U4-ch79, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 49.24
Std Dev 3.393
Entry
ampl
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1
2
3
4
5
6
7
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0
10
20
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40
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60
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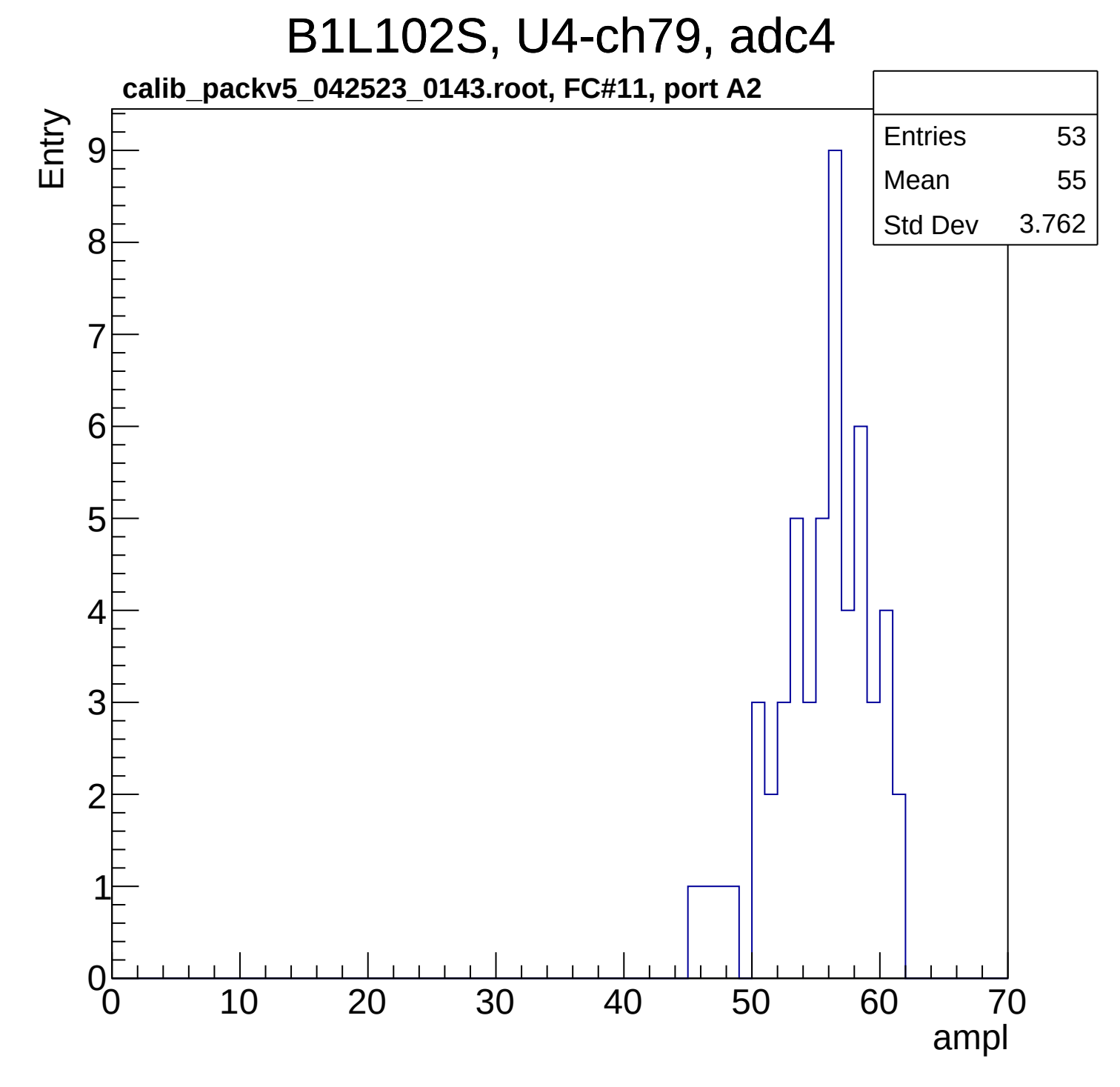
B1L102S, U4-ch79, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 55
Std Dev 3.762
Entry
ampl
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3
4
5
6
7
8
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0
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20
30
40
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60
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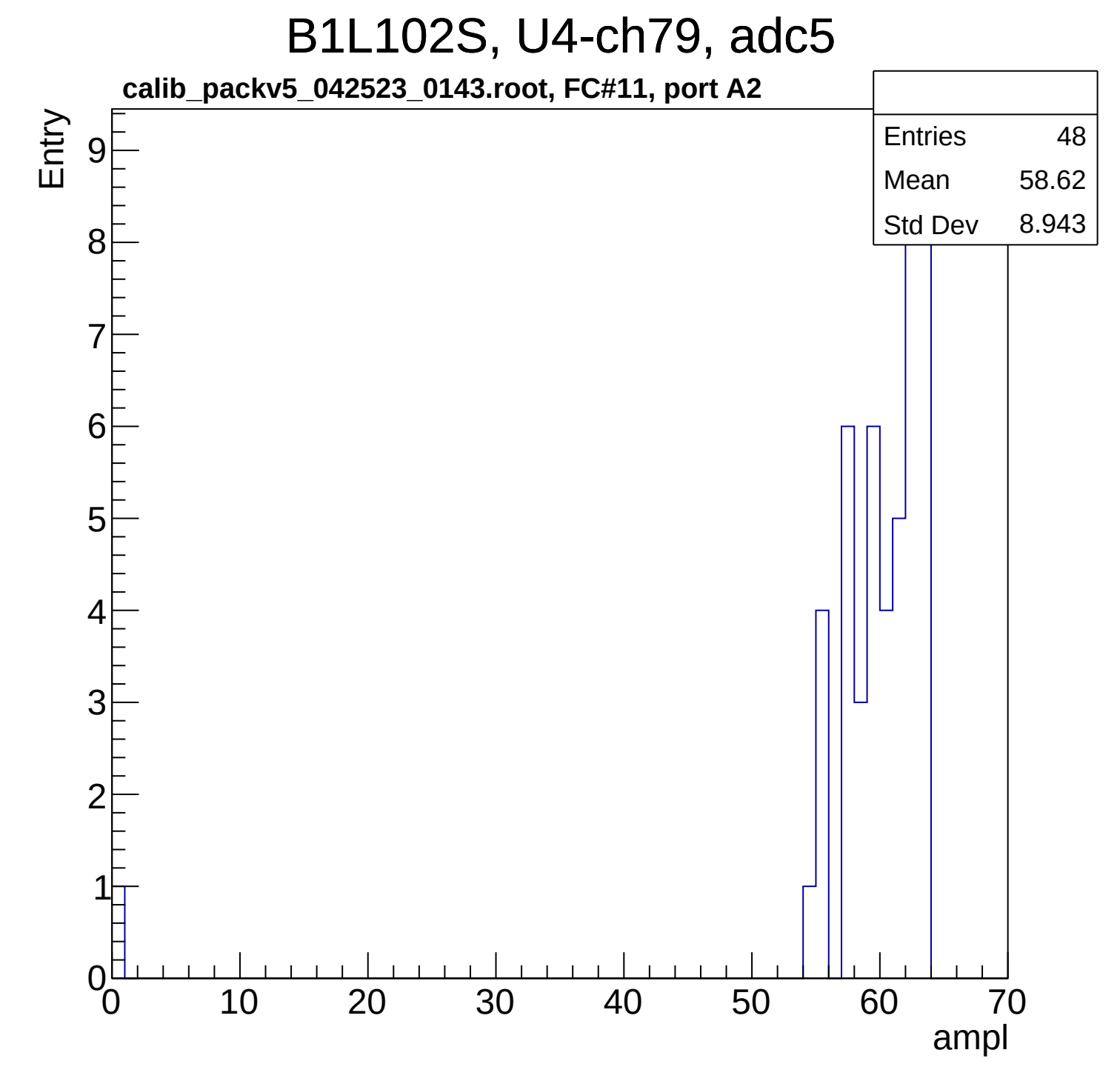
B1L102S, U4-ch79, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 48
Mean 58.62
Std Dev 8.943
Entry
ampl
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5
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0
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60
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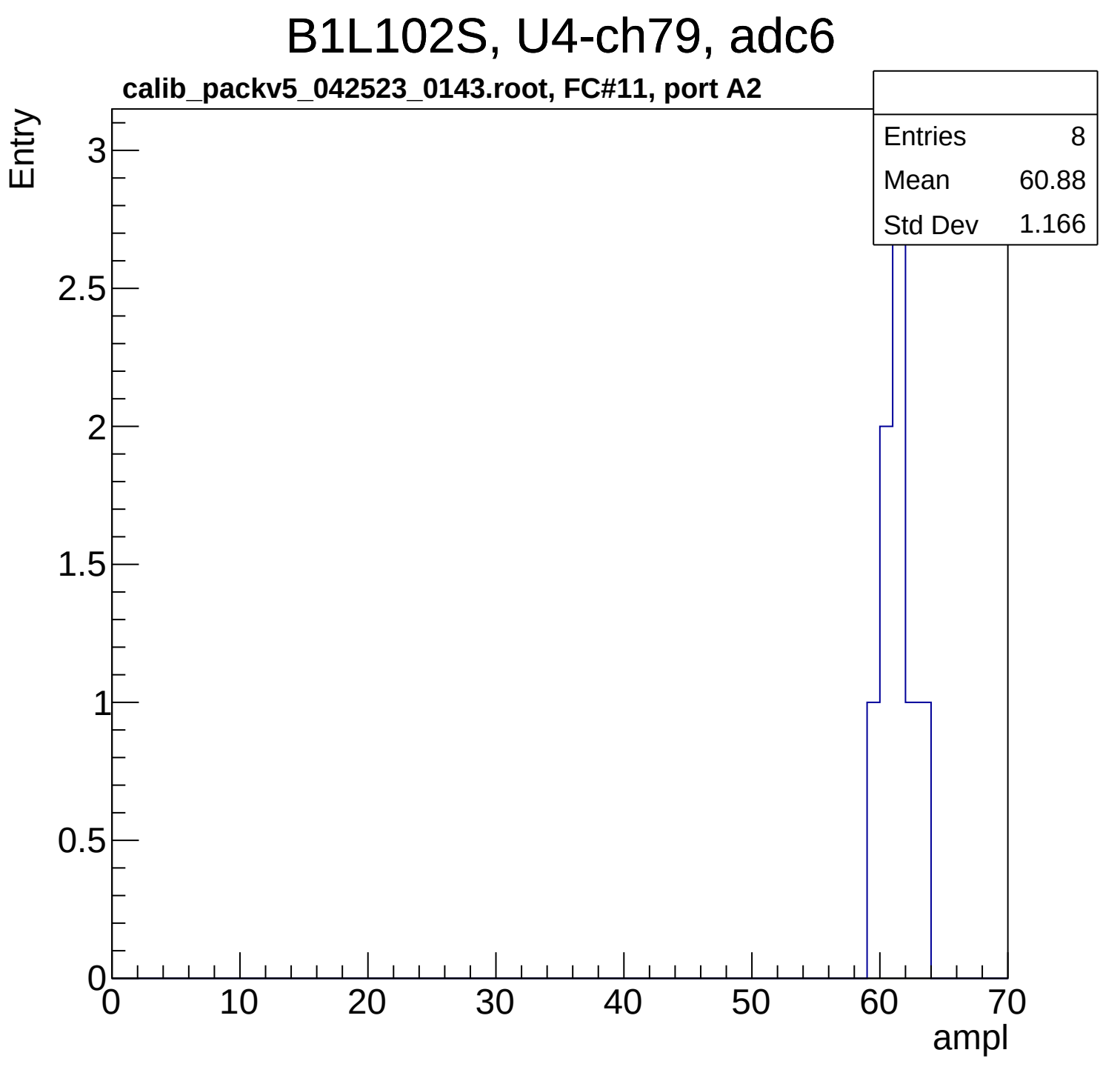
B1L102S, U4-ch79, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 8
Mean 60.88
Std Dev 1.166
Entry
ampl
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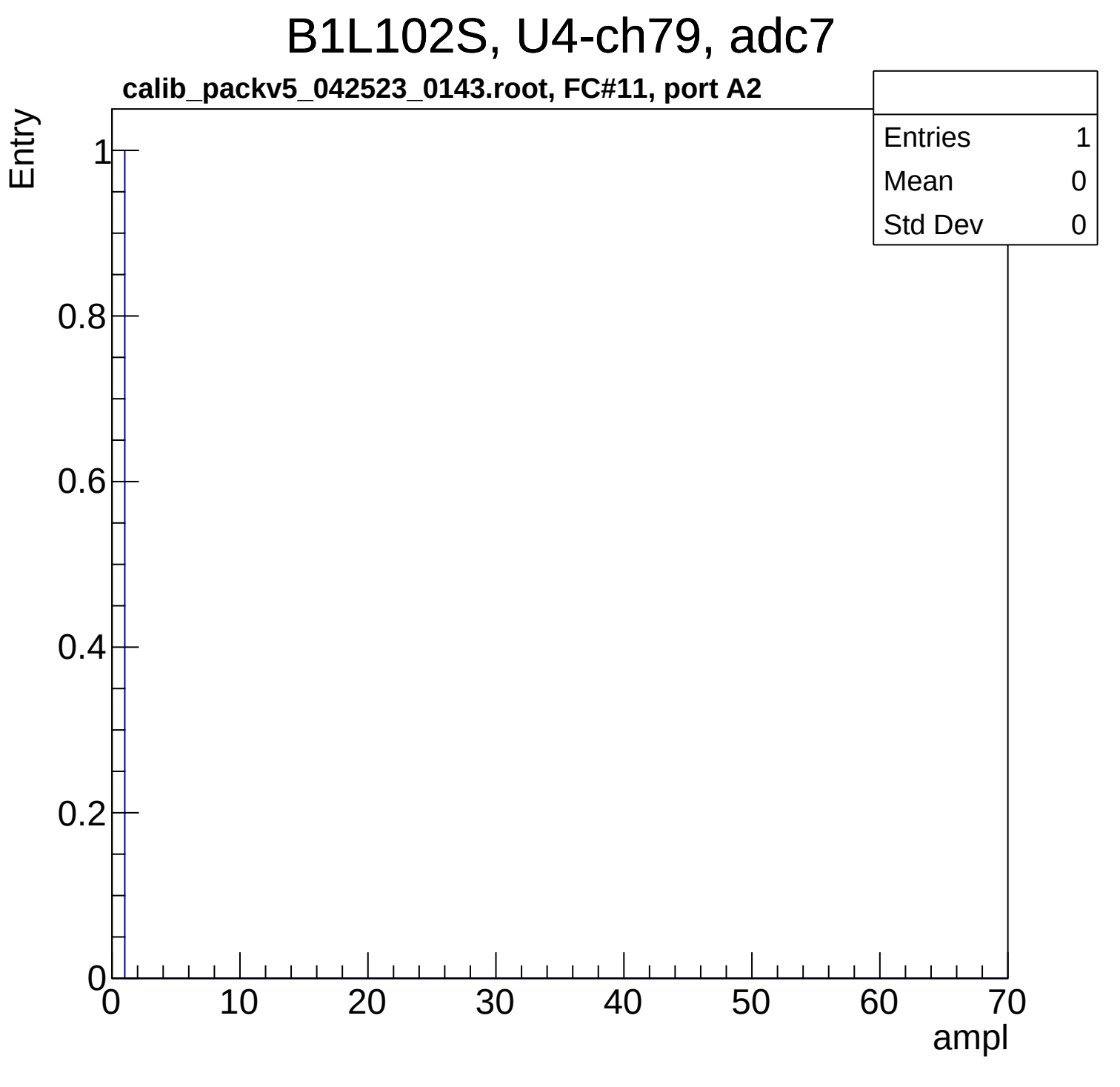
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U4-ch79, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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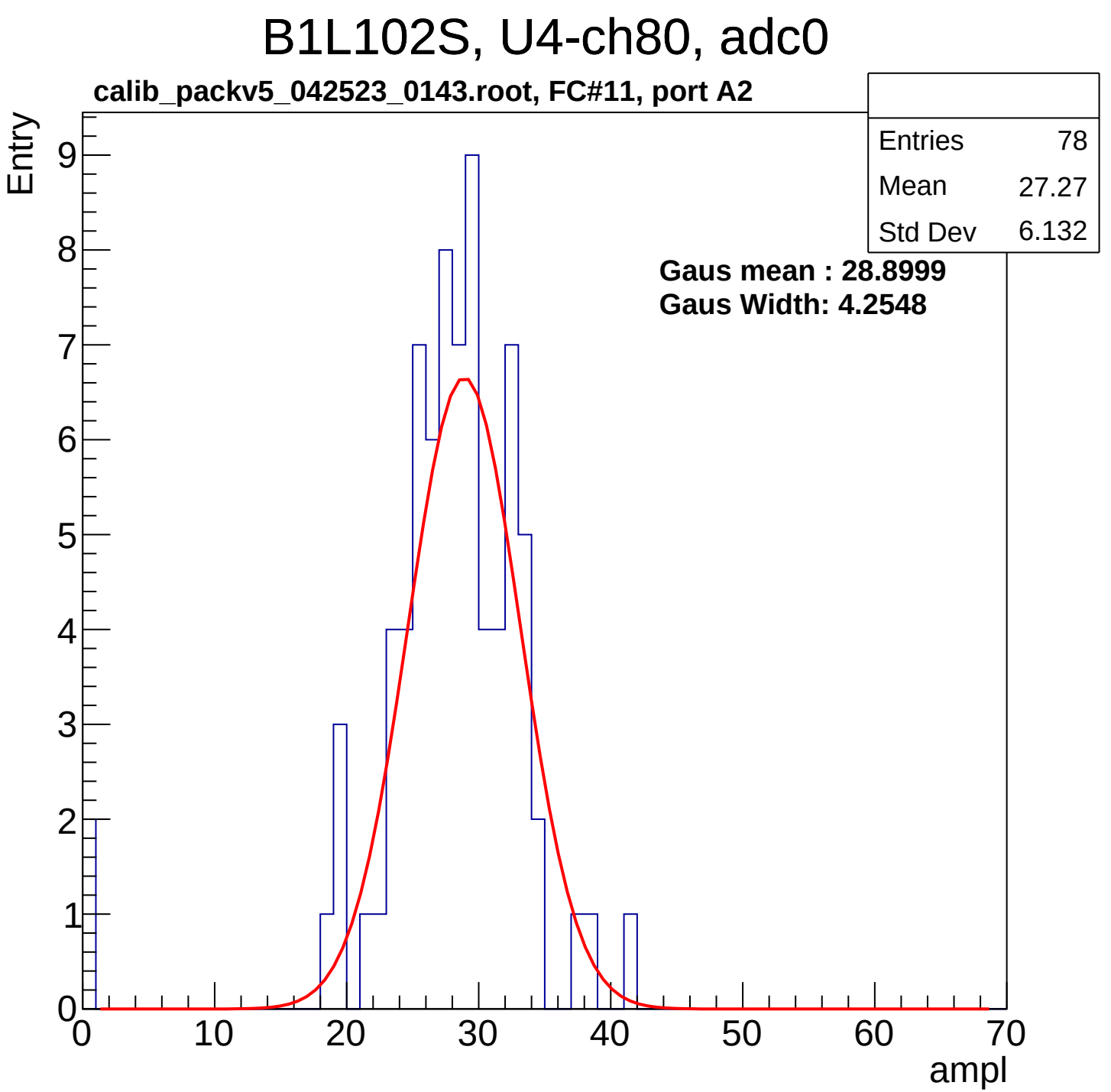
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch80, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 78
Mean 27.27
Std Dev 6.132
Gaus mean : 28.8999
Gaus Width: 4.2548
Entry
ampl
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1
2
3
4
5
6
7
8
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0
10
20
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40
50
60
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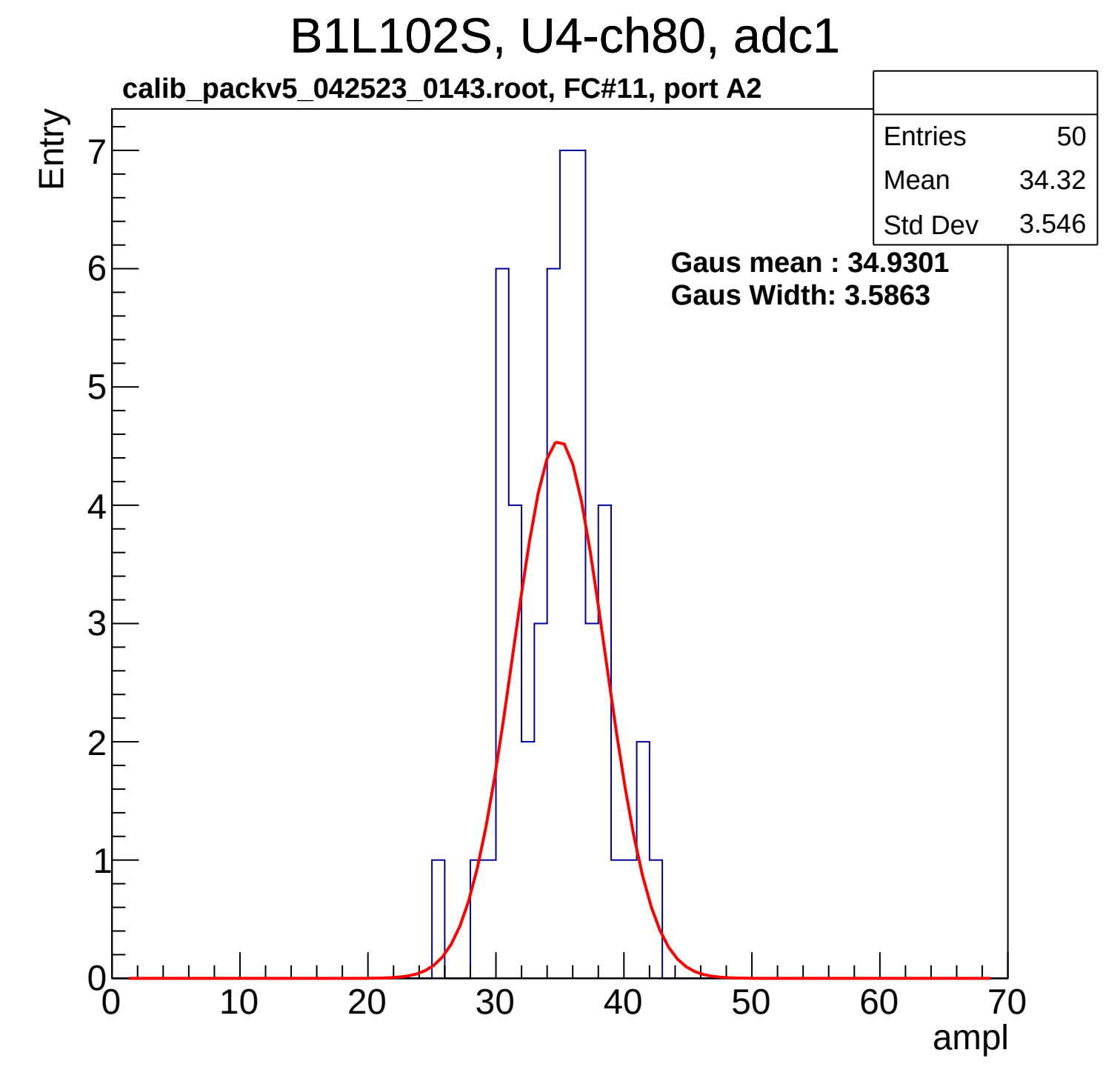
B1L102S, U4-ch80, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 50
Mean 34.32
Std Dev 3.546
Gaus mean : 34.9301
Gaus Width: 3.5863
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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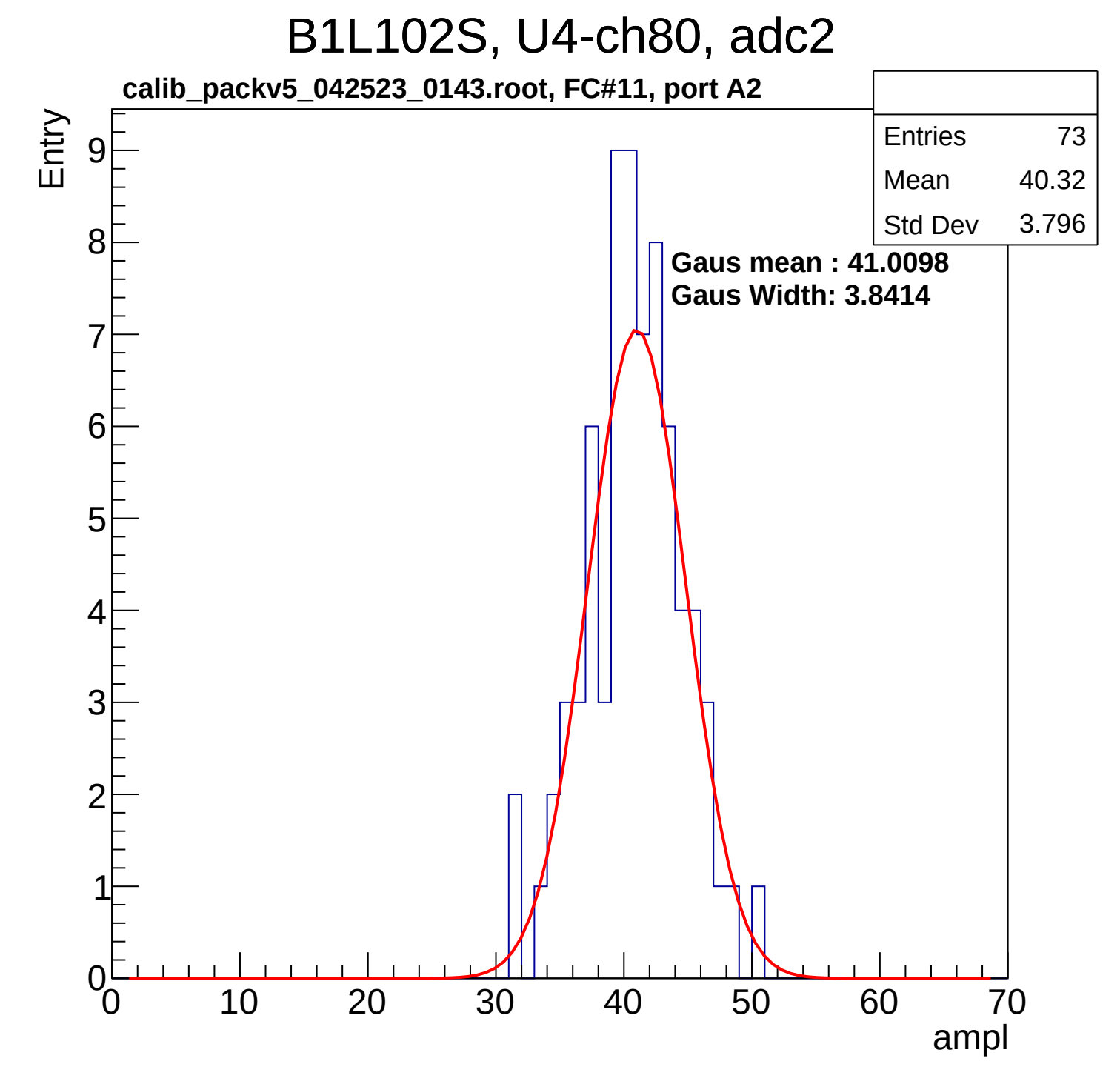
B1L102S, U4-ch80, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 40.32
Std Dev 3.796
Gaus mean : 41.0098
Gaus Width: 3.8414
Entry
ampl
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2
3
4
5
6
7
8
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0
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20
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40
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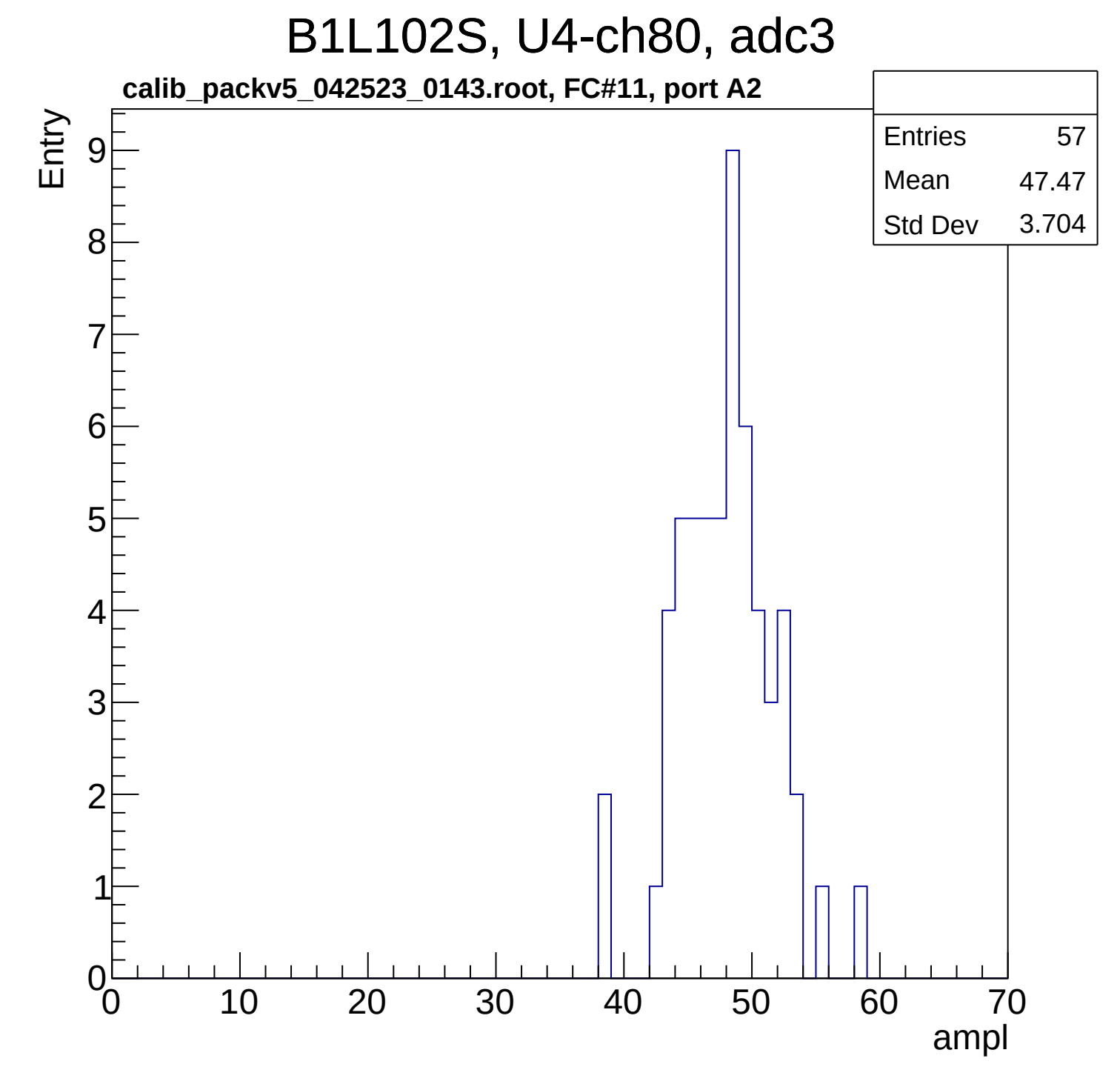
B1L102S, U4-ch80, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 57
Mean 47.47
Std Dev 3.704
Entry
ampl
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6
7
8
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0
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40
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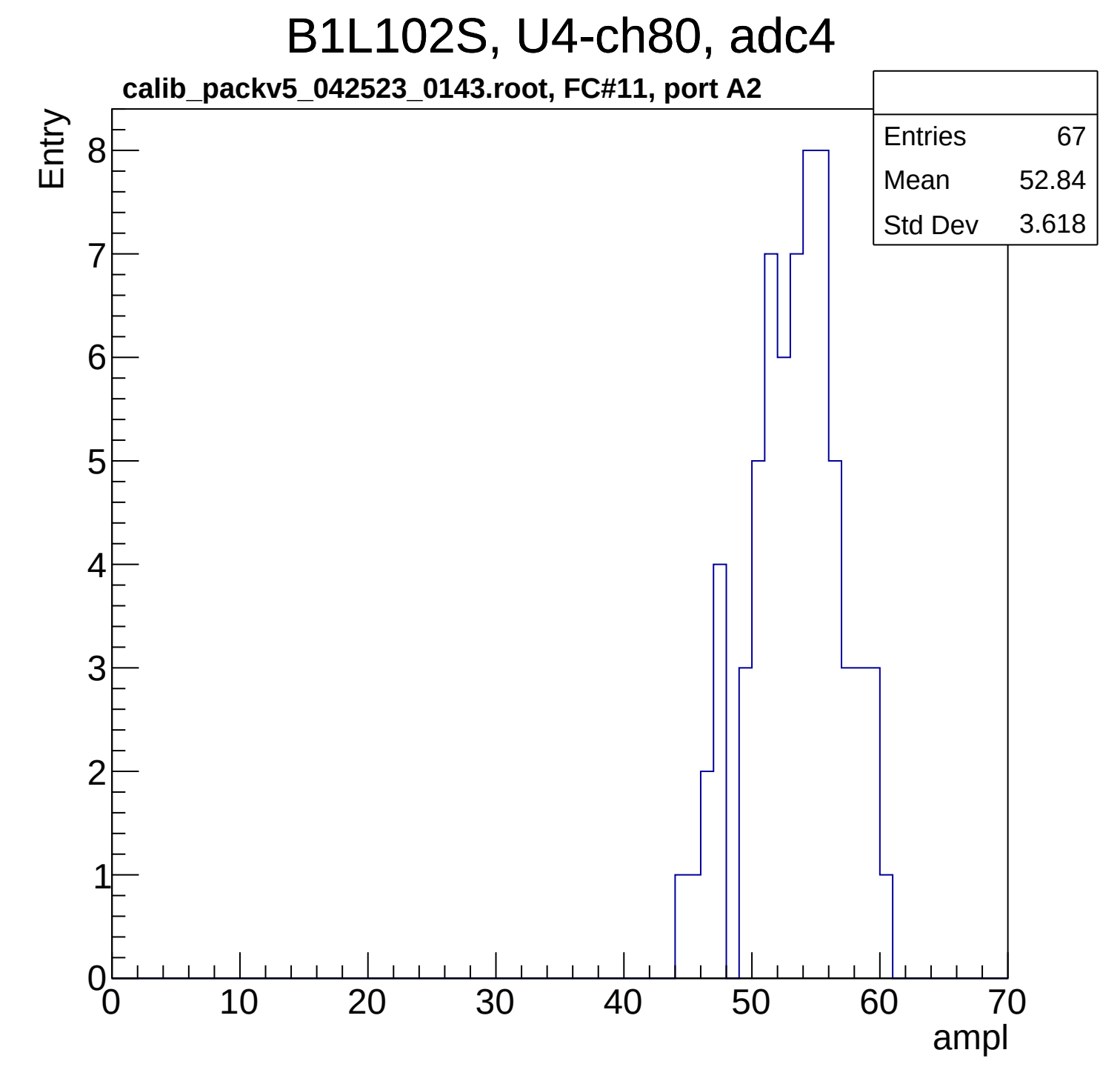
B1L102S, U4-ch80, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 52.84
Std Dev 3.618
Entry
ampl
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0
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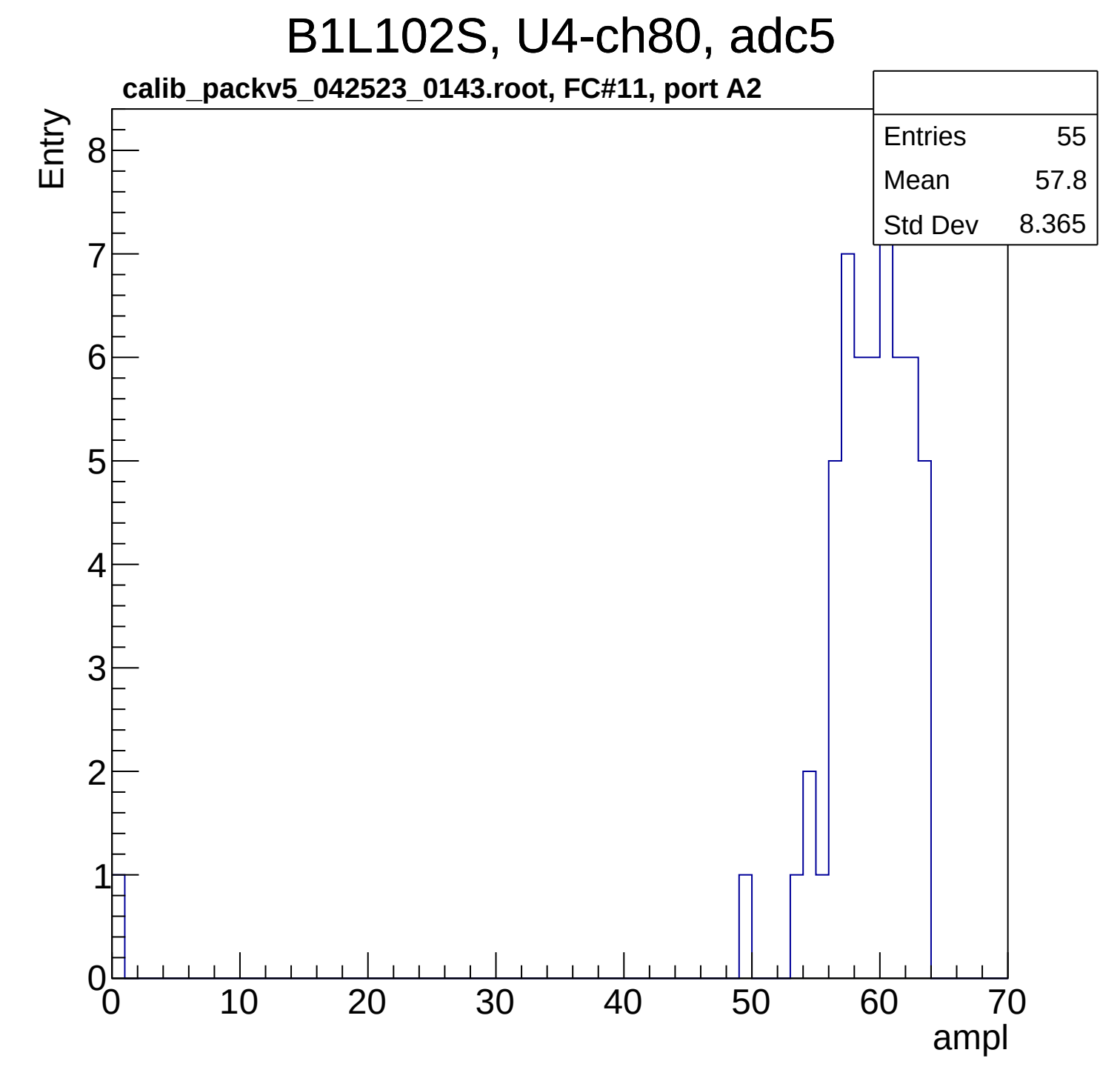
B1L102S, U4-ch80, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 57.8
Std Dev 8.365
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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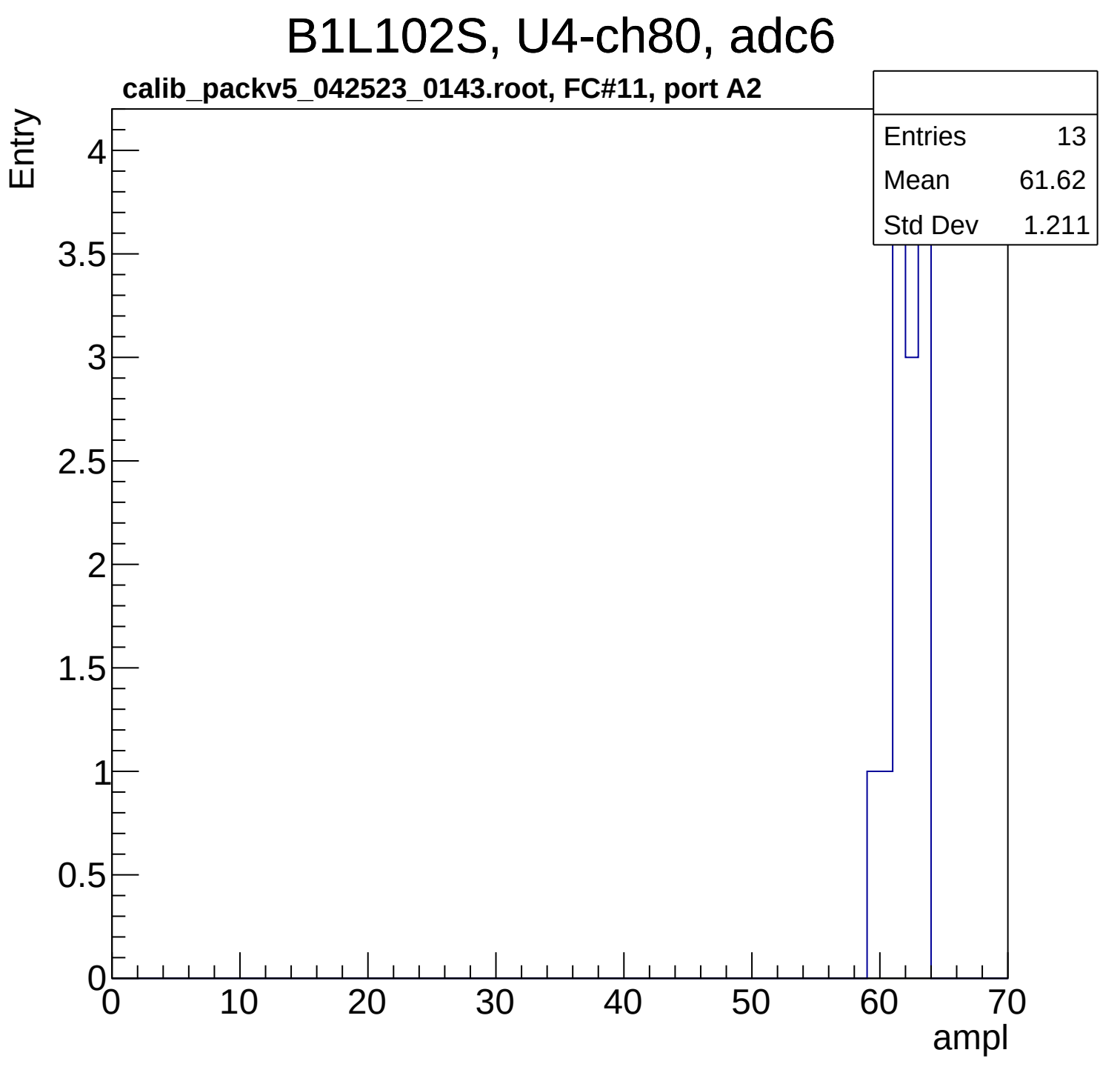
B1L102S, U4-ch80, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 13
Mean 61.62
Std Dev 1.211
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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60
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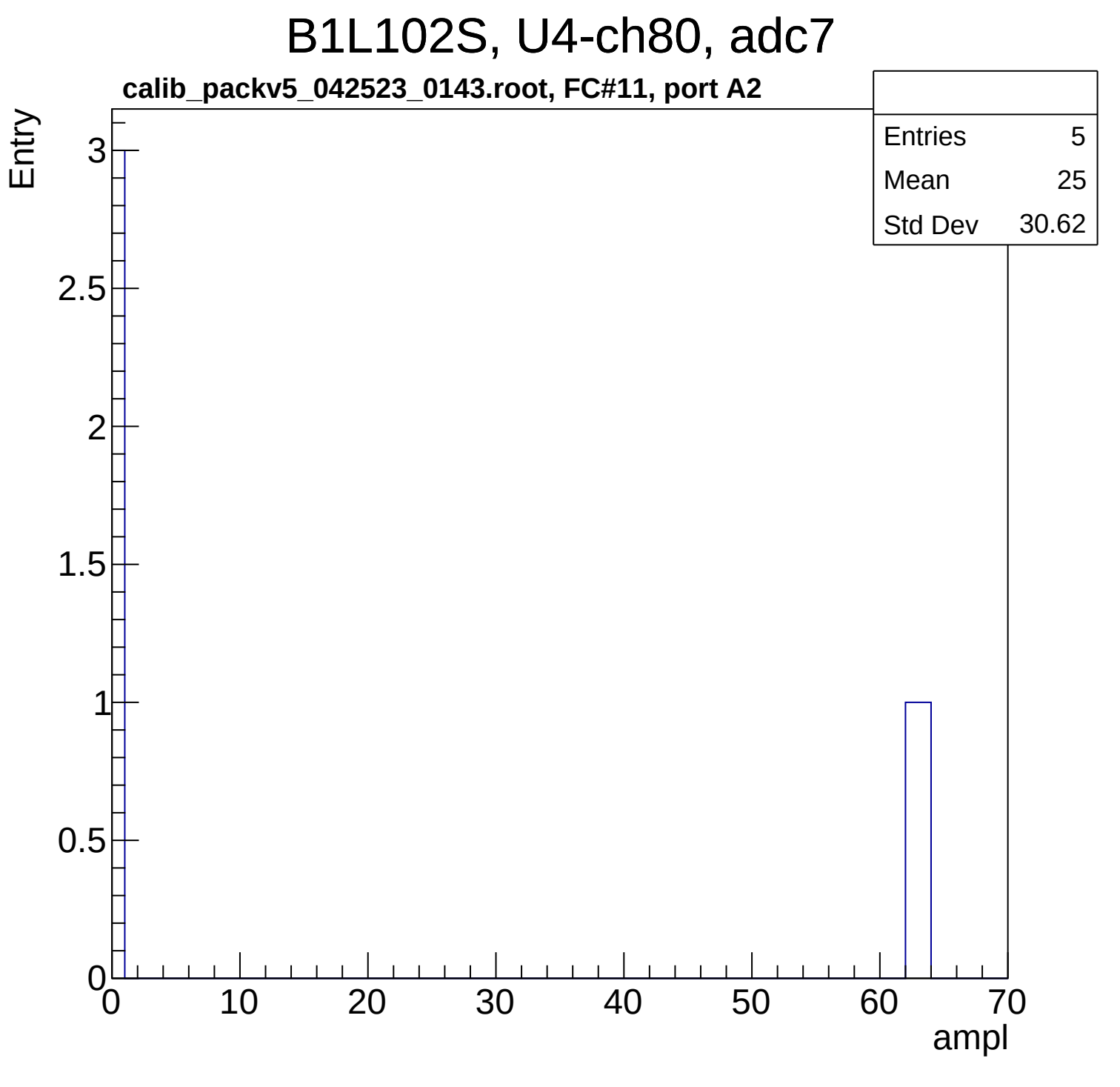
B1L102S, U4-ch80, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 5
Mean 25
Std Dev 30.62
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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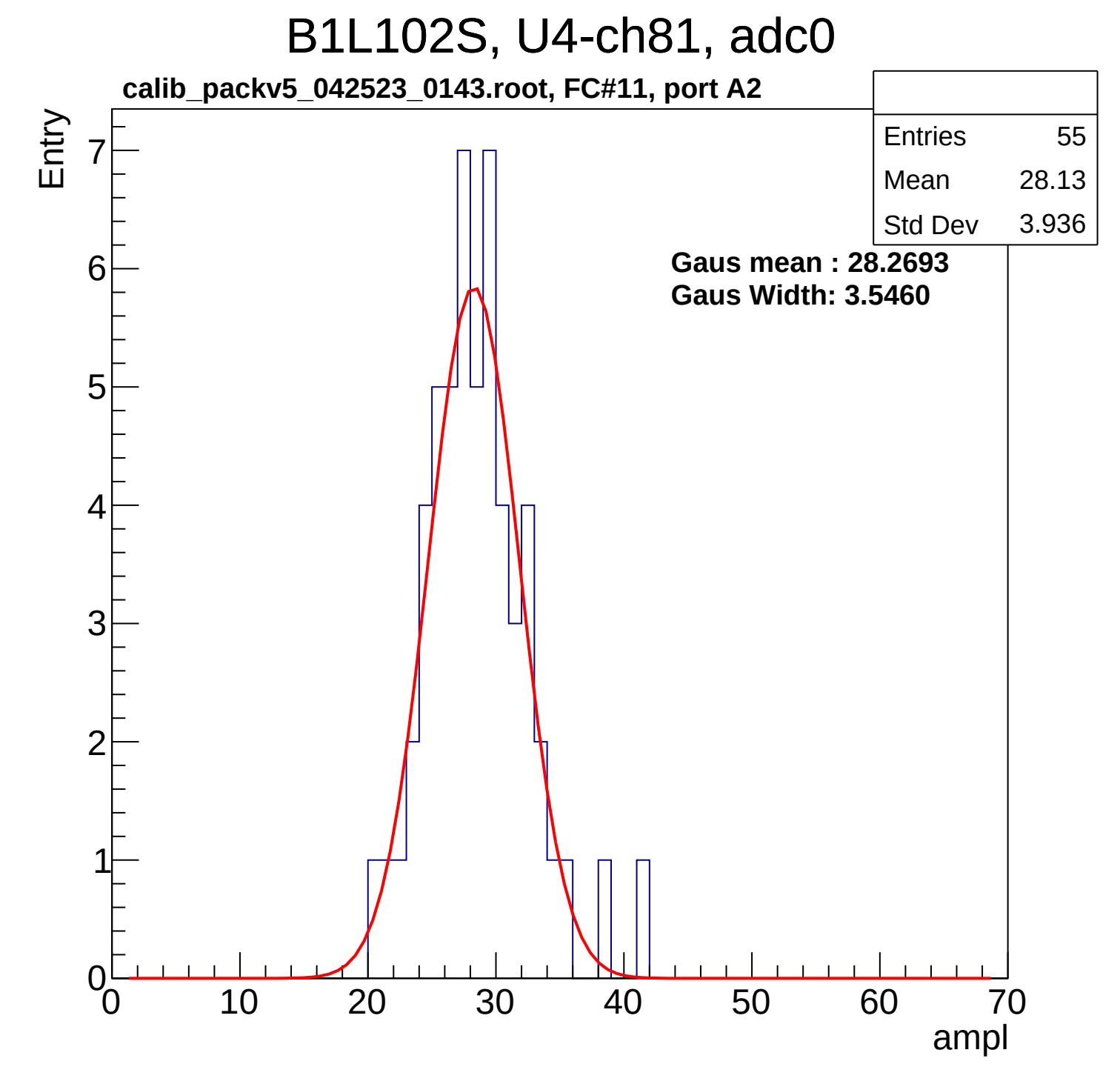
B1L102S, U4-ch81, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 28.13
Std Dev 3.936
Gaus mean : 28.2693
Gaus Width: 3.5460
Entry
ampl
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1
2
3
4
5
6
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0
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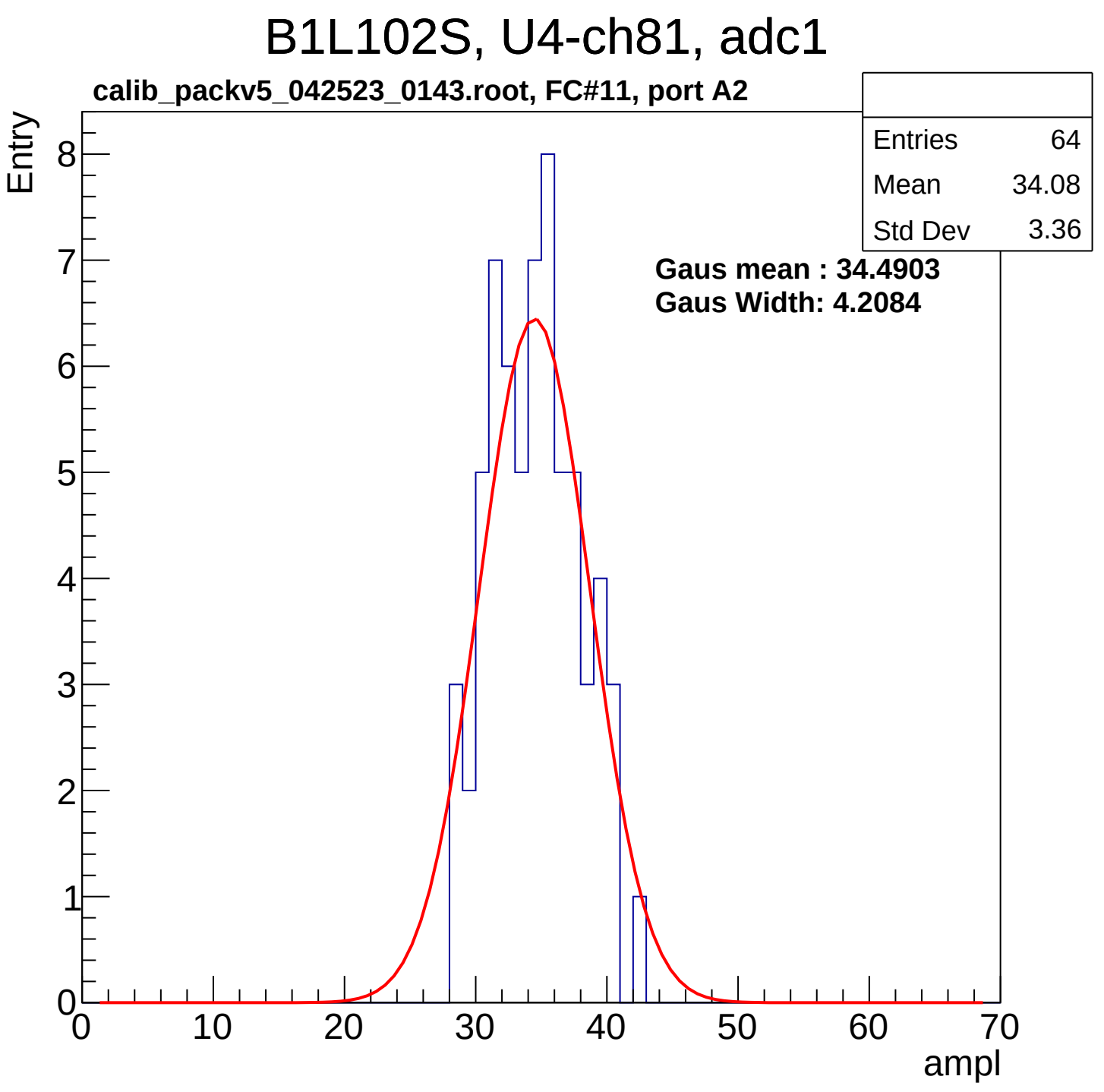
B1L102S, U4-ch81, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 34.08
Std Dev 3.36
Gaus mean : 34.4903
Gaus Width: 4.2084
Entry
ampl
0
1
2
3
4
5
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7
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0
10
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40
50
60
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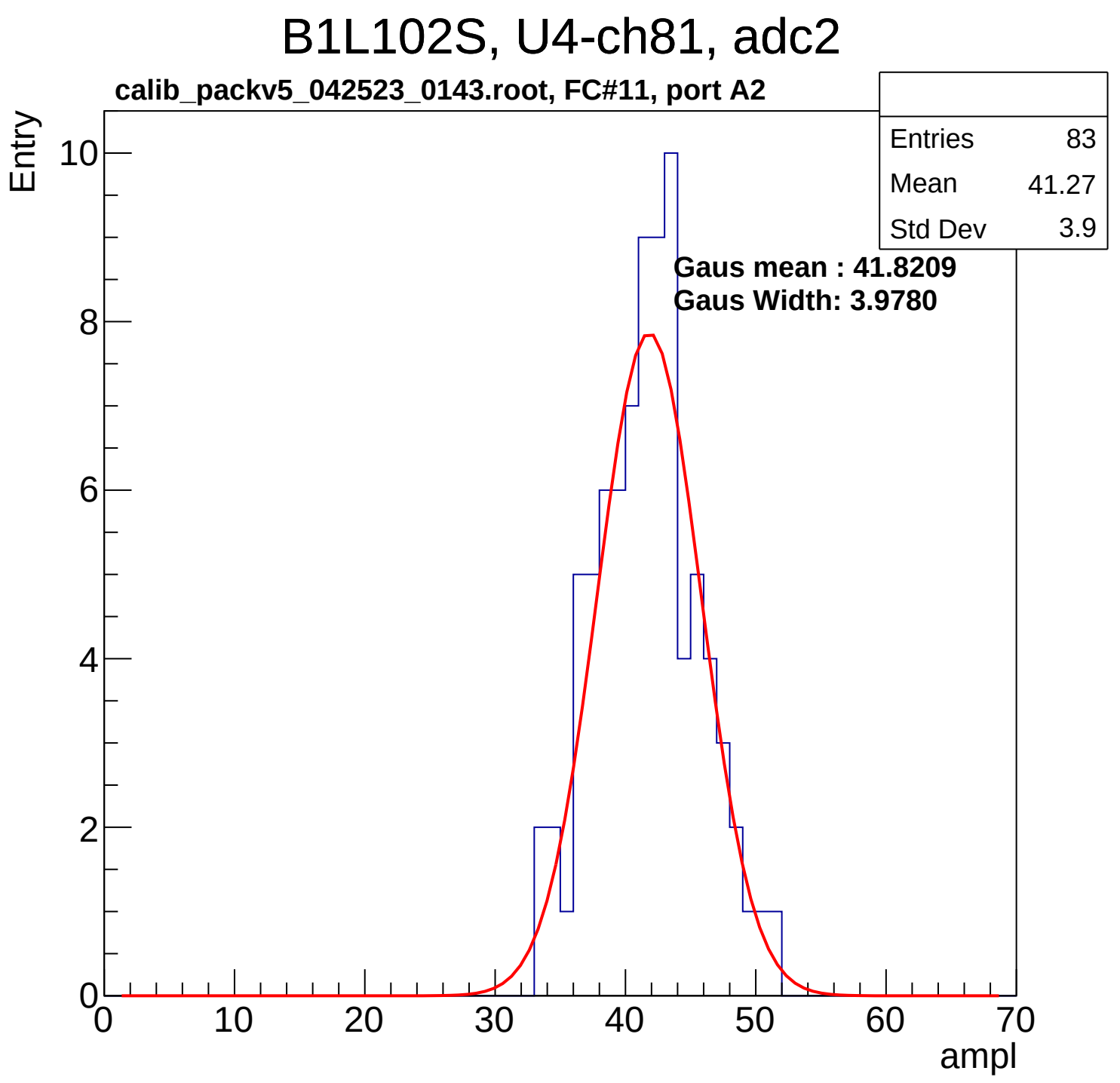
B1L102S, U4-ch81, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 83
Mean 41.27
Std Dev 3.9
Gaus mean : 41.8209
Gaus Width: 3.9780
Entry
ampl
0
2
4
6
8
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0
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60
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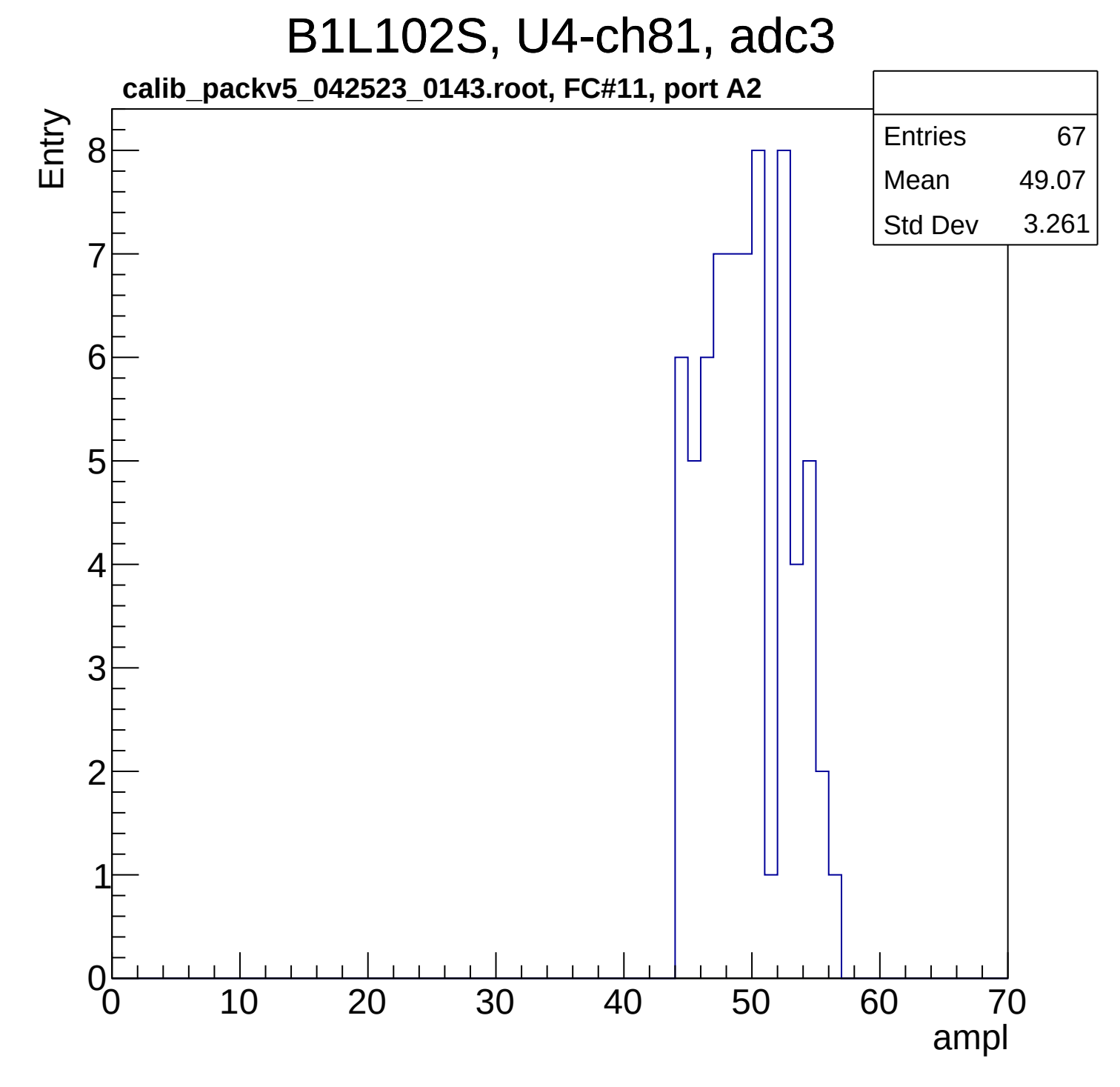
B1L102S, U4-ch81, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 49.07
Std Dev 3.261
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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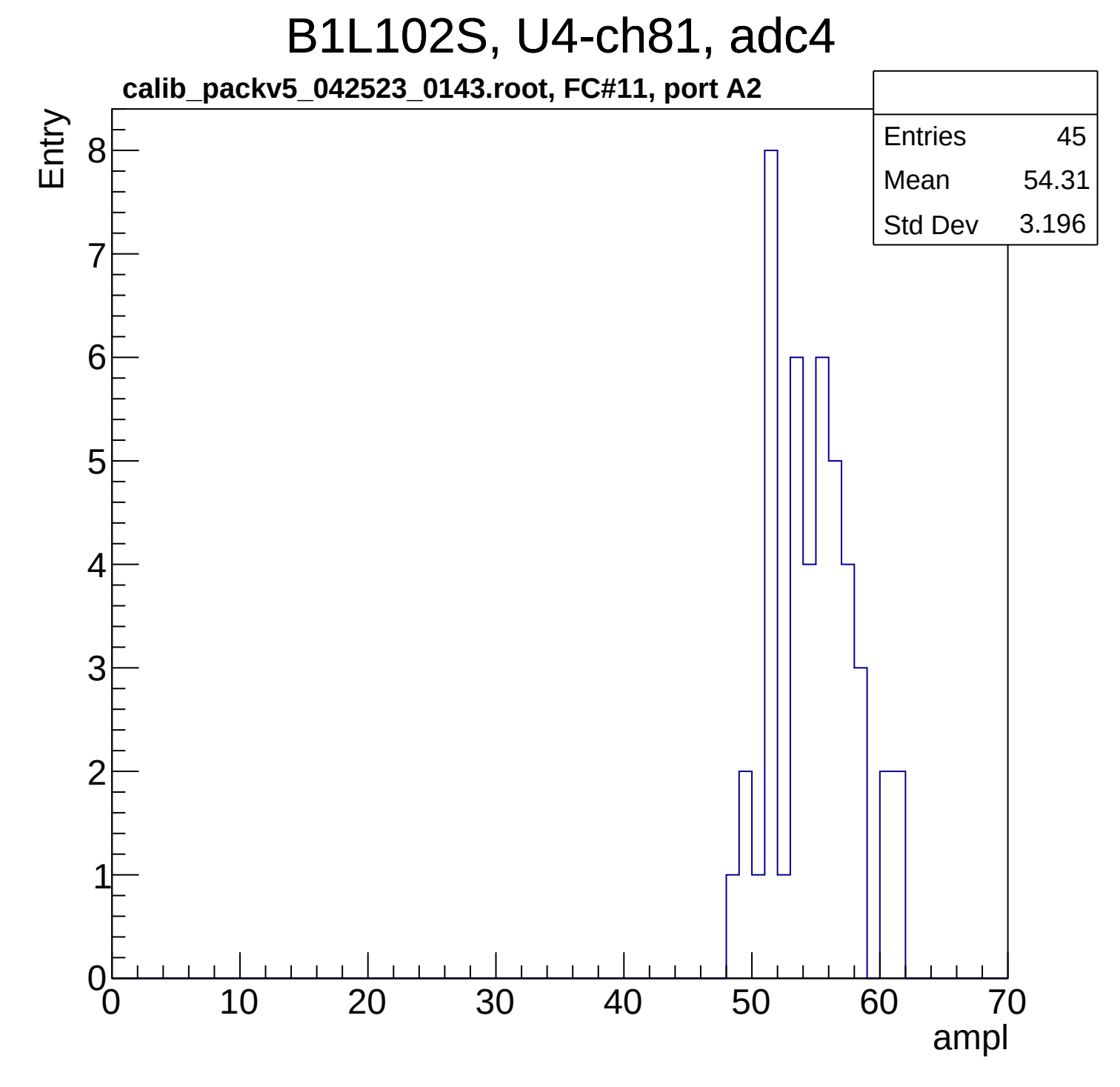
B1L102S, U4-ch81, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 45
Mean 54.31
Std Dev 3.196
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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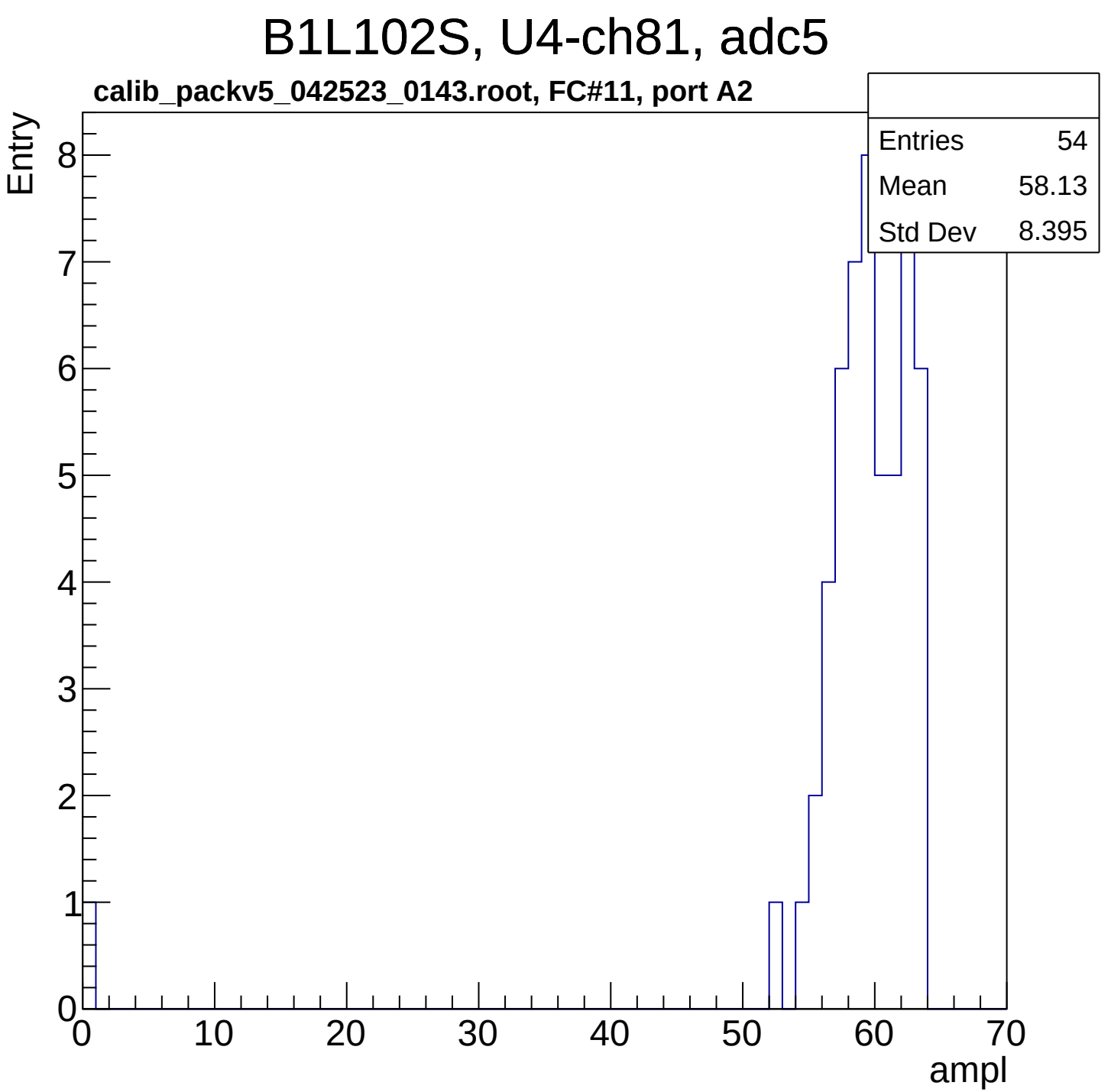
B1L102S, U4-ch81, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 58.13
Std Dev 8.395
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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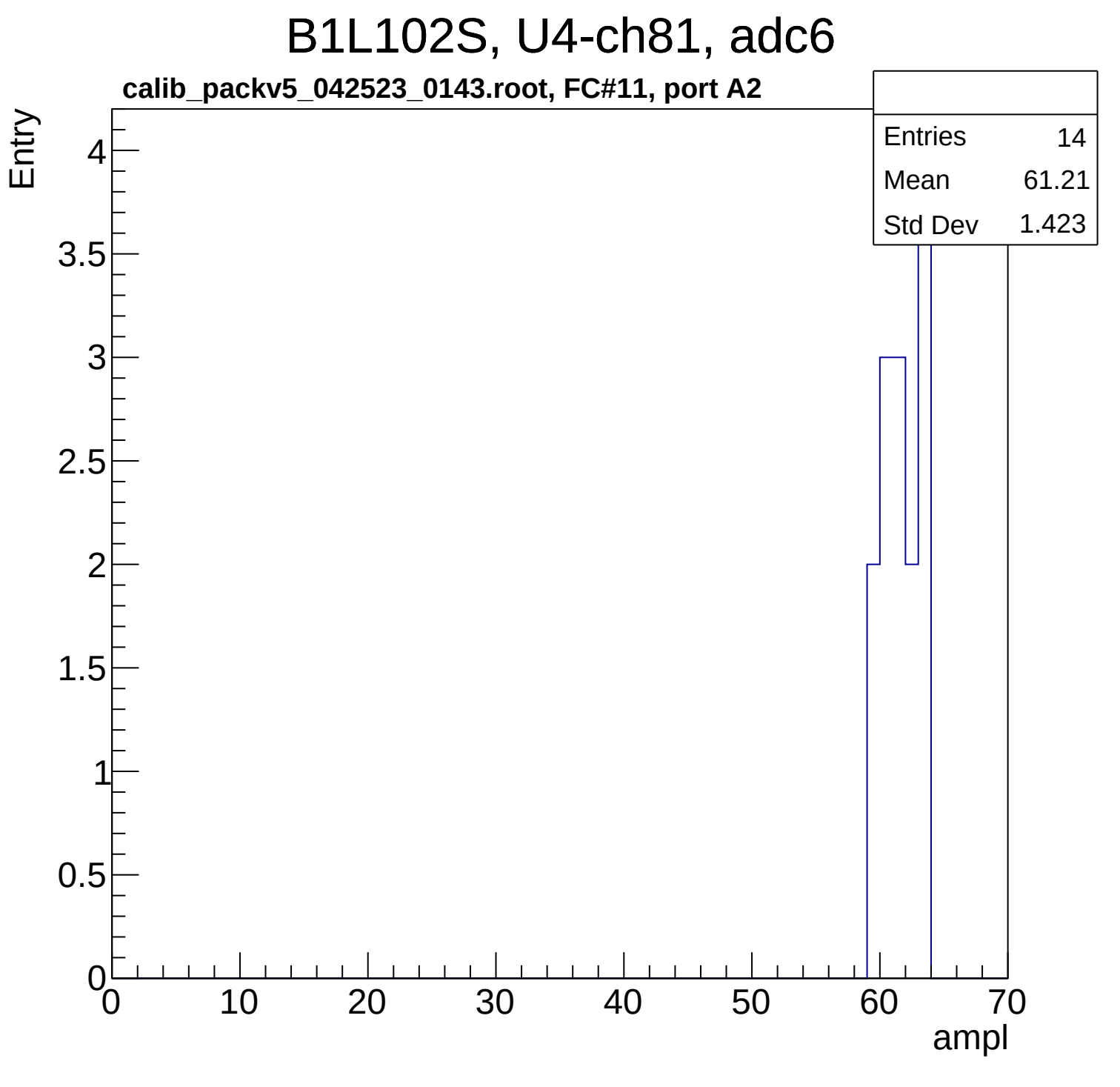
B1L102S, U4-ch81, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 14
Mean 61.21
Std Dev 1.423
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
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60
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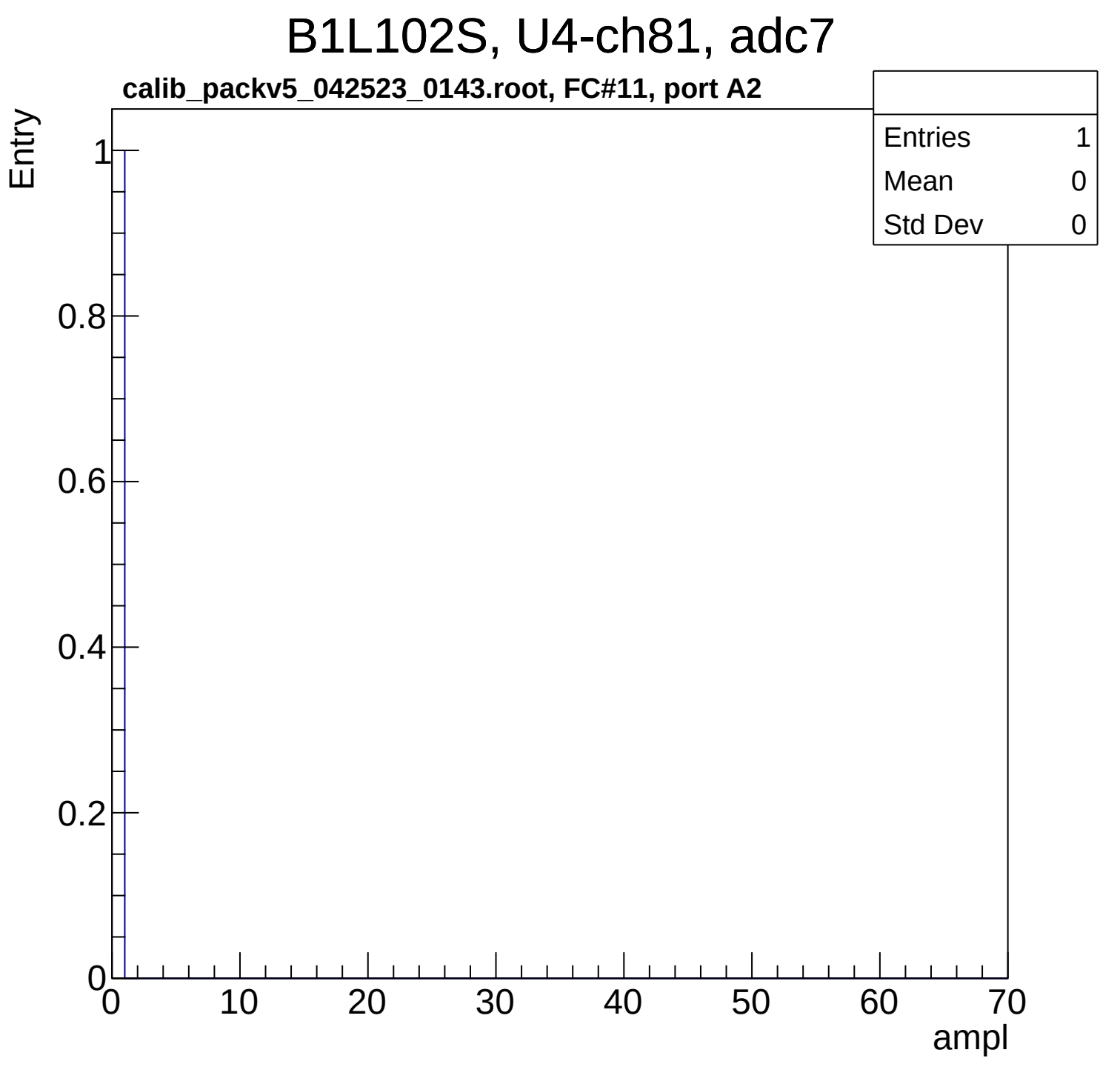
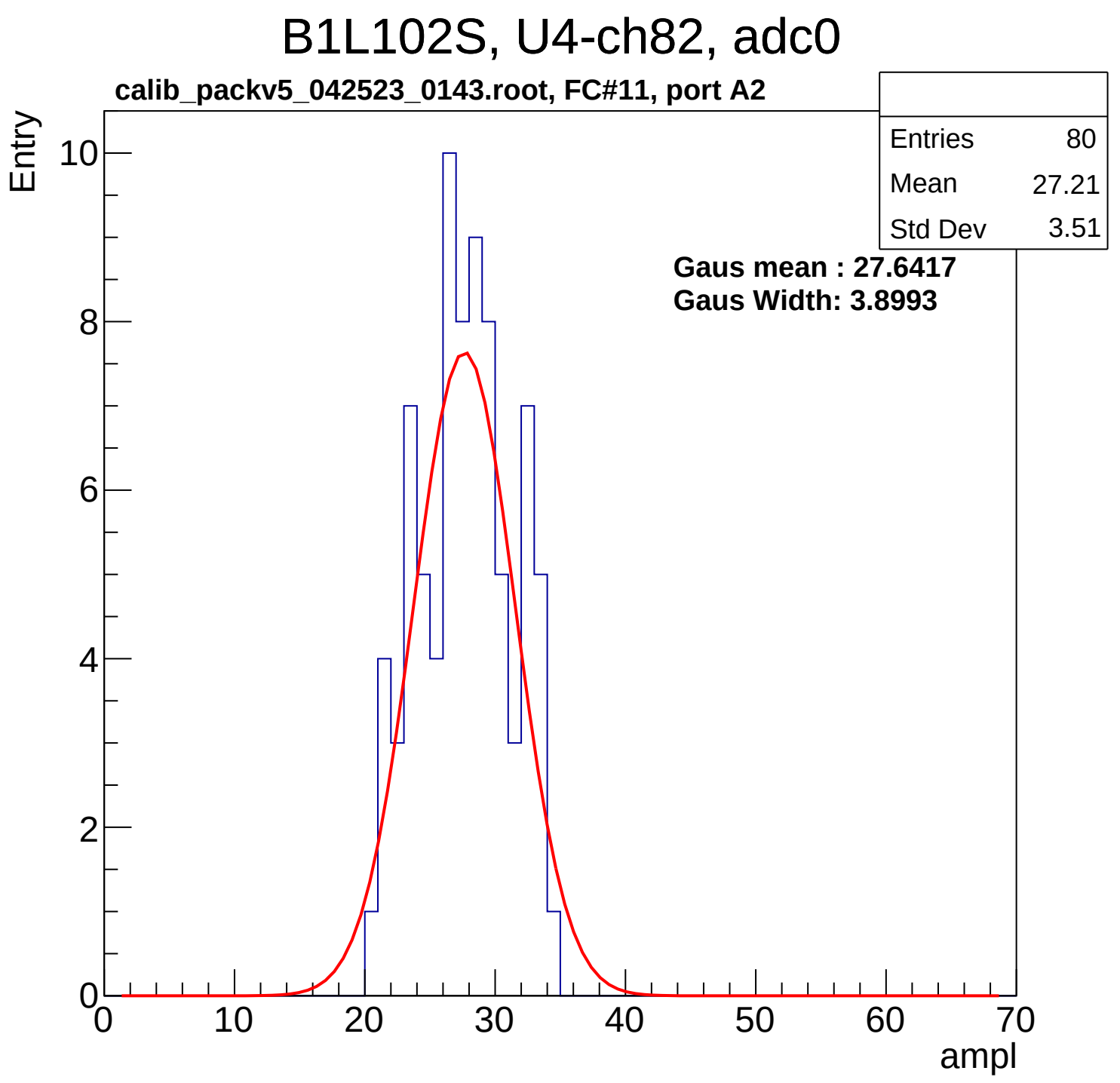
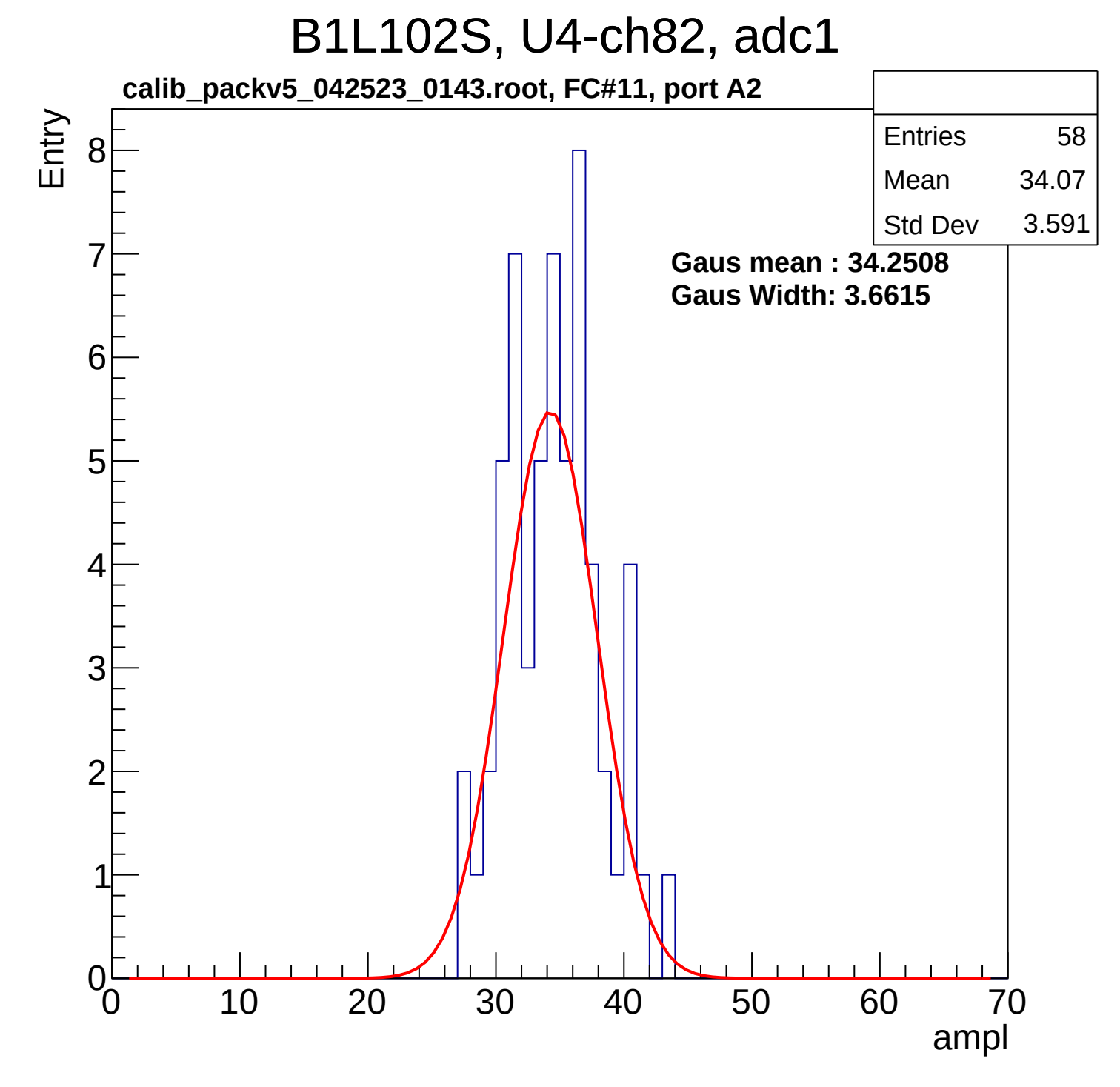

B1L102S, U4-ch81, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch82, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 80
Mean 27.21
Std Dev 3.51
Gaus mean : 27.6417
Gaus Width: 3.8993
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch82, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 34.07
Std Dev 3.591
Gaus mean : 34.2508
Gaus Width: 3.6615
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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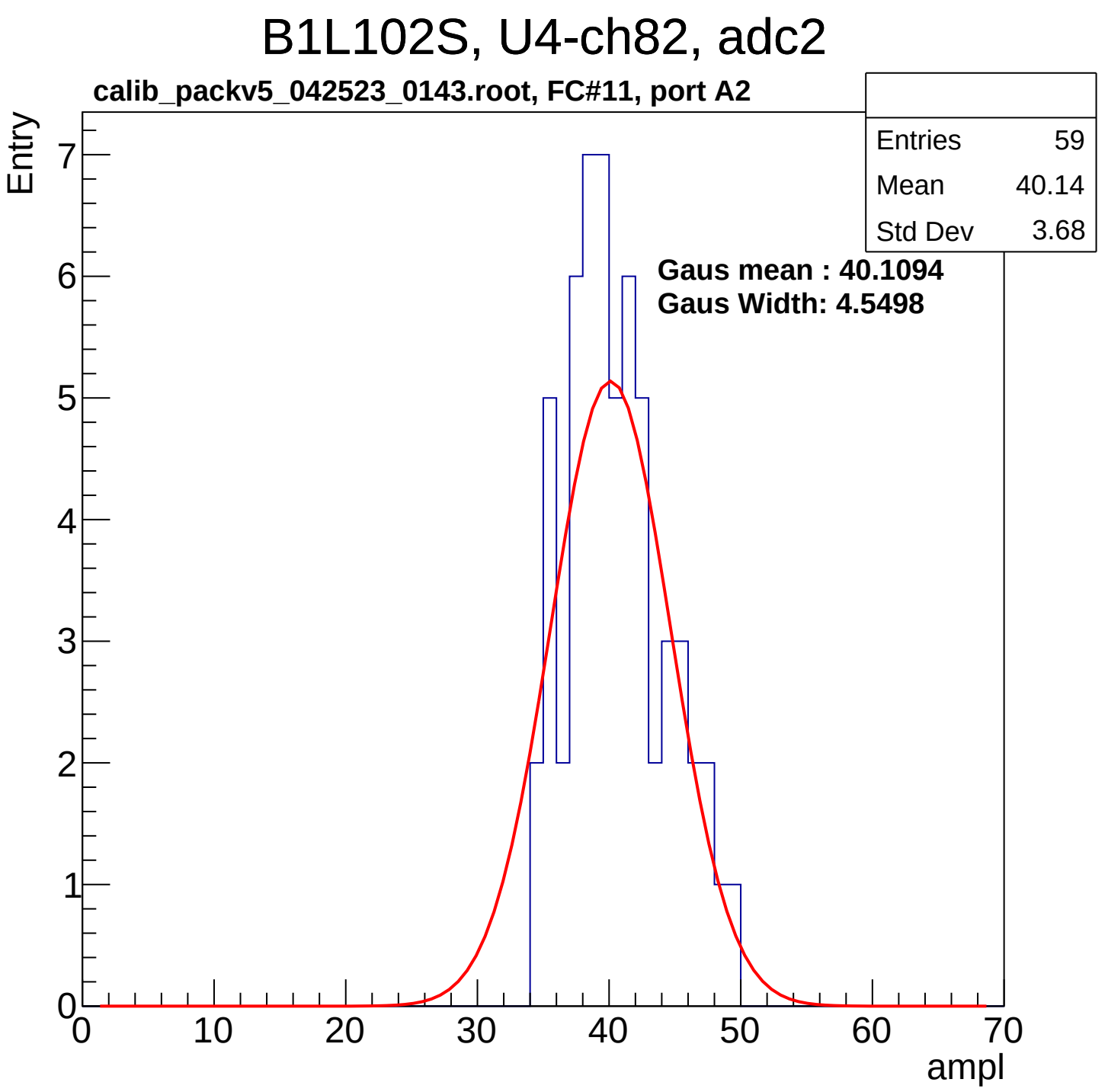
B1L102S, U4-ch82, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 40.14
Std Dev 3.68
Gaus mean : 40.1094
Gaus Width: 4.5498
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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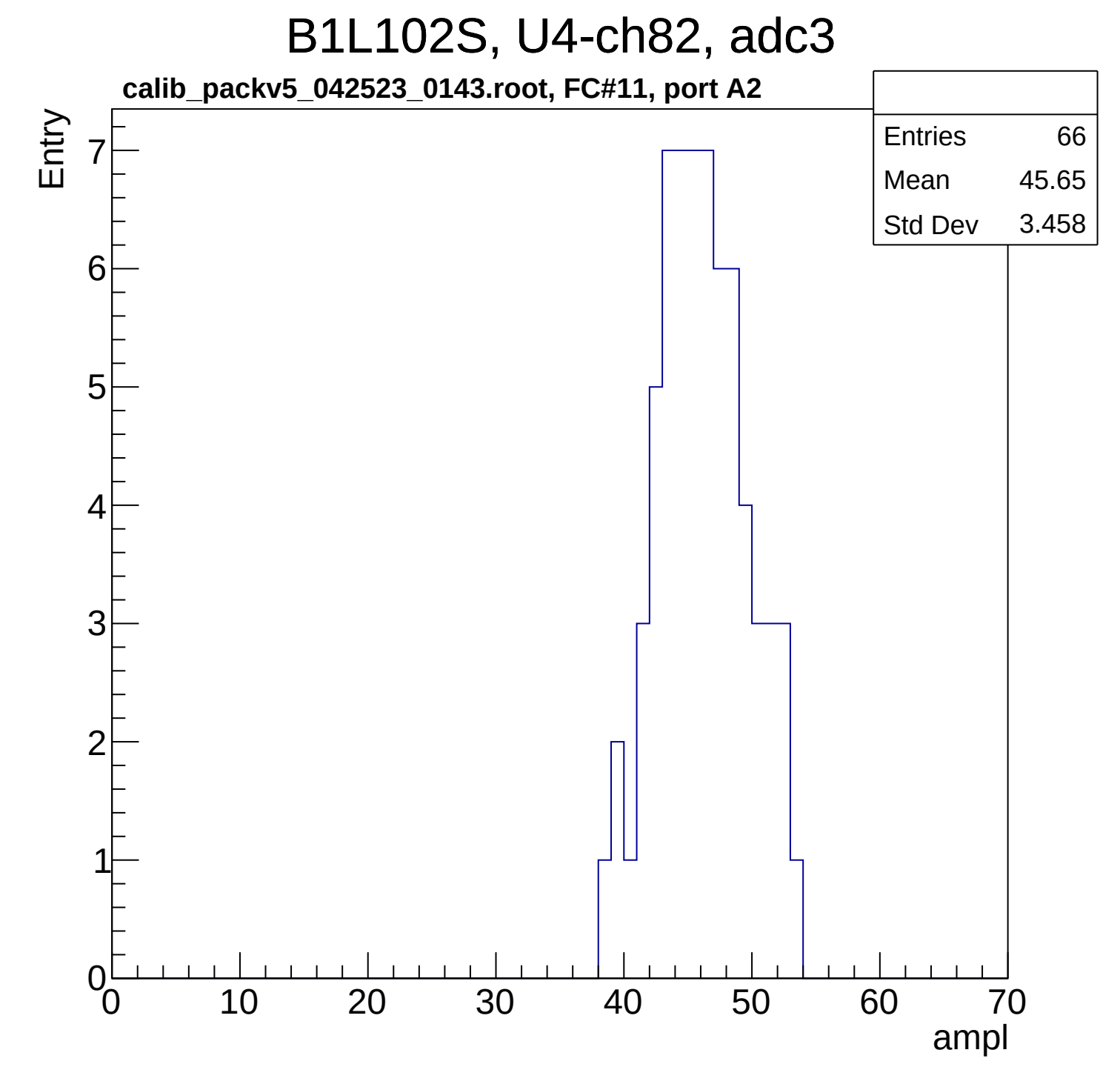
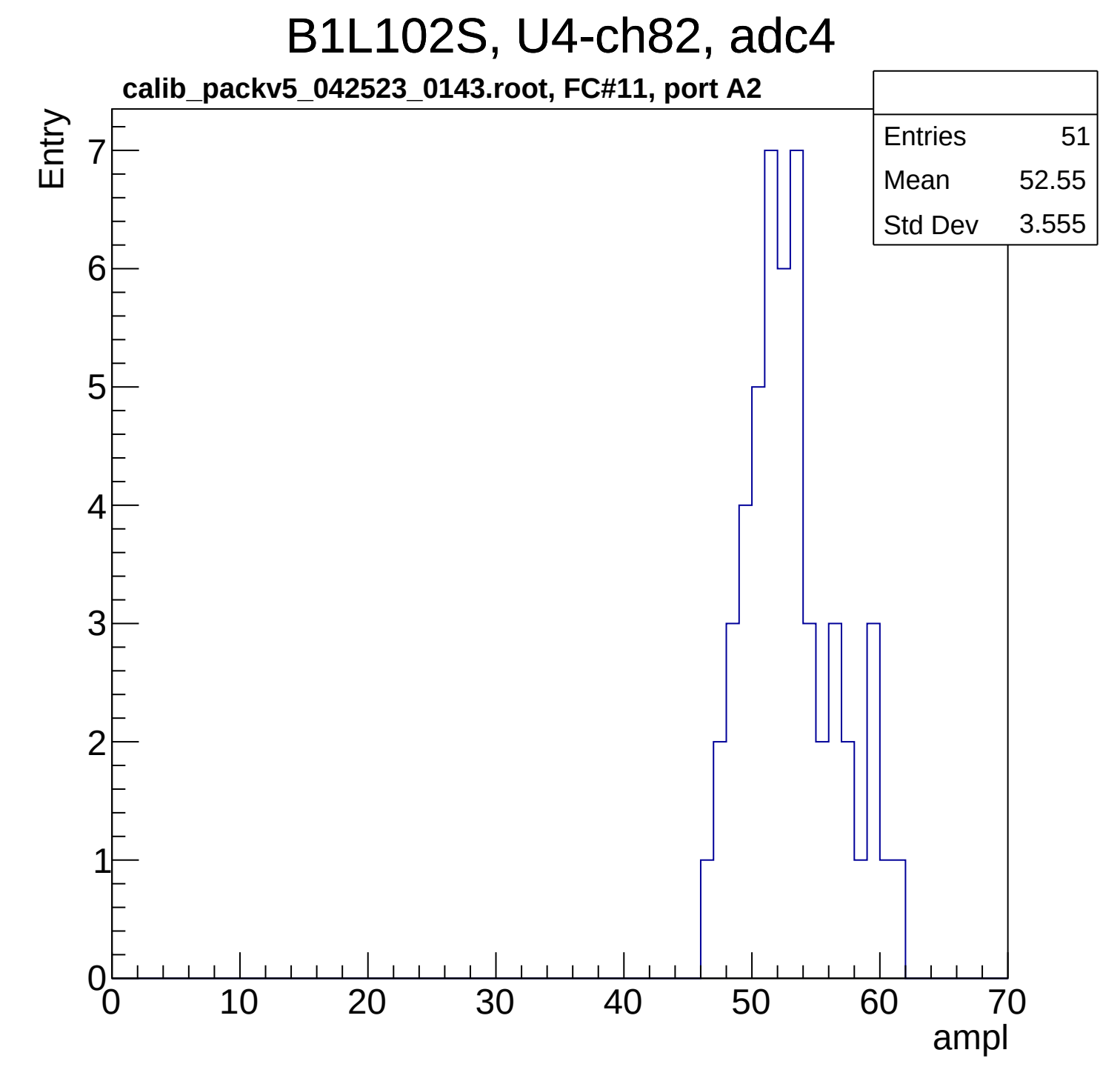

B1L102S, U4-ch82, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 45.65
Std Dev 3.458
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch82, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 52.55
Std Dev 3.555
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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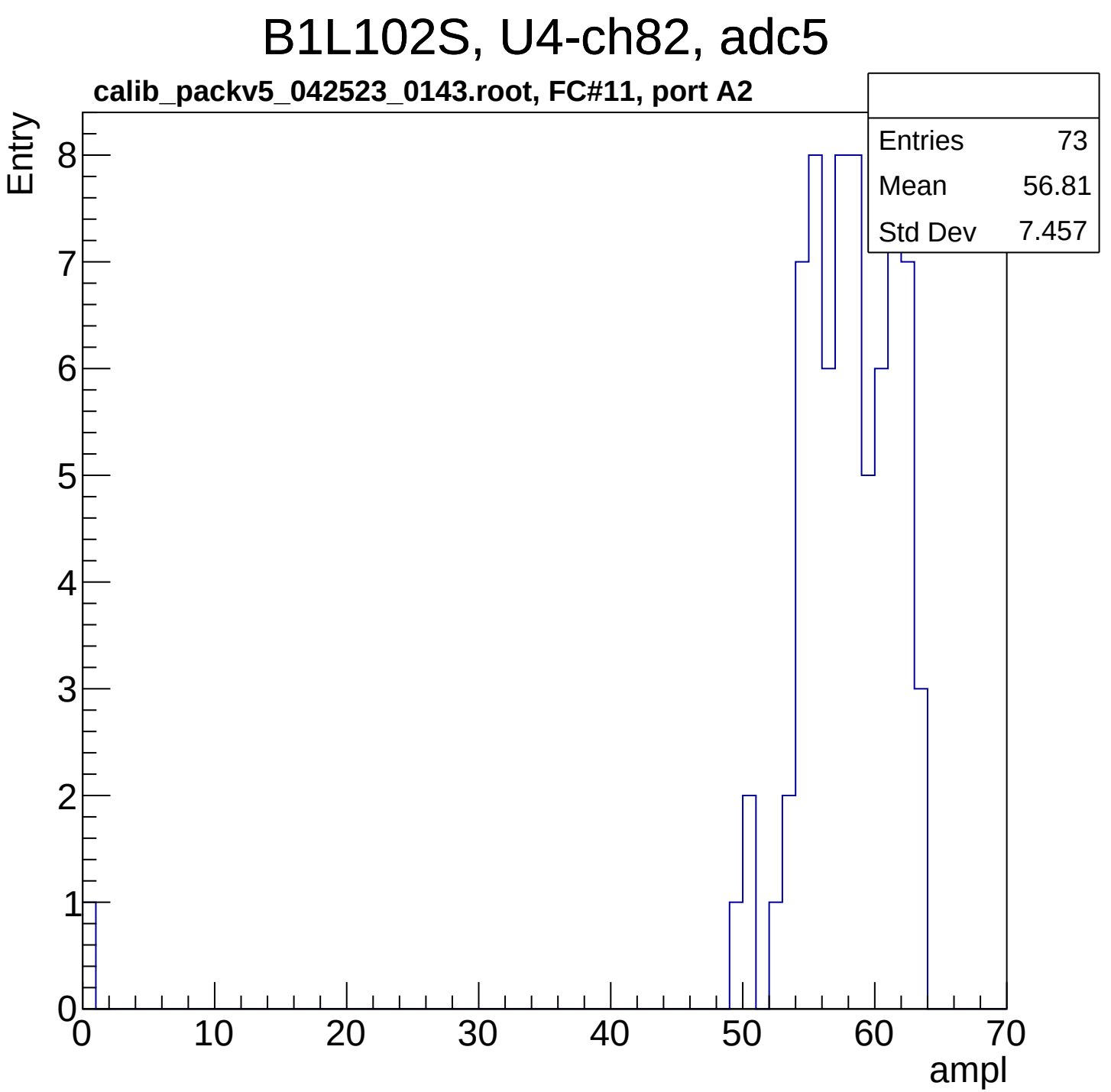
B1L102S, U4-ch82, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 56.81
Std Dev 7.457
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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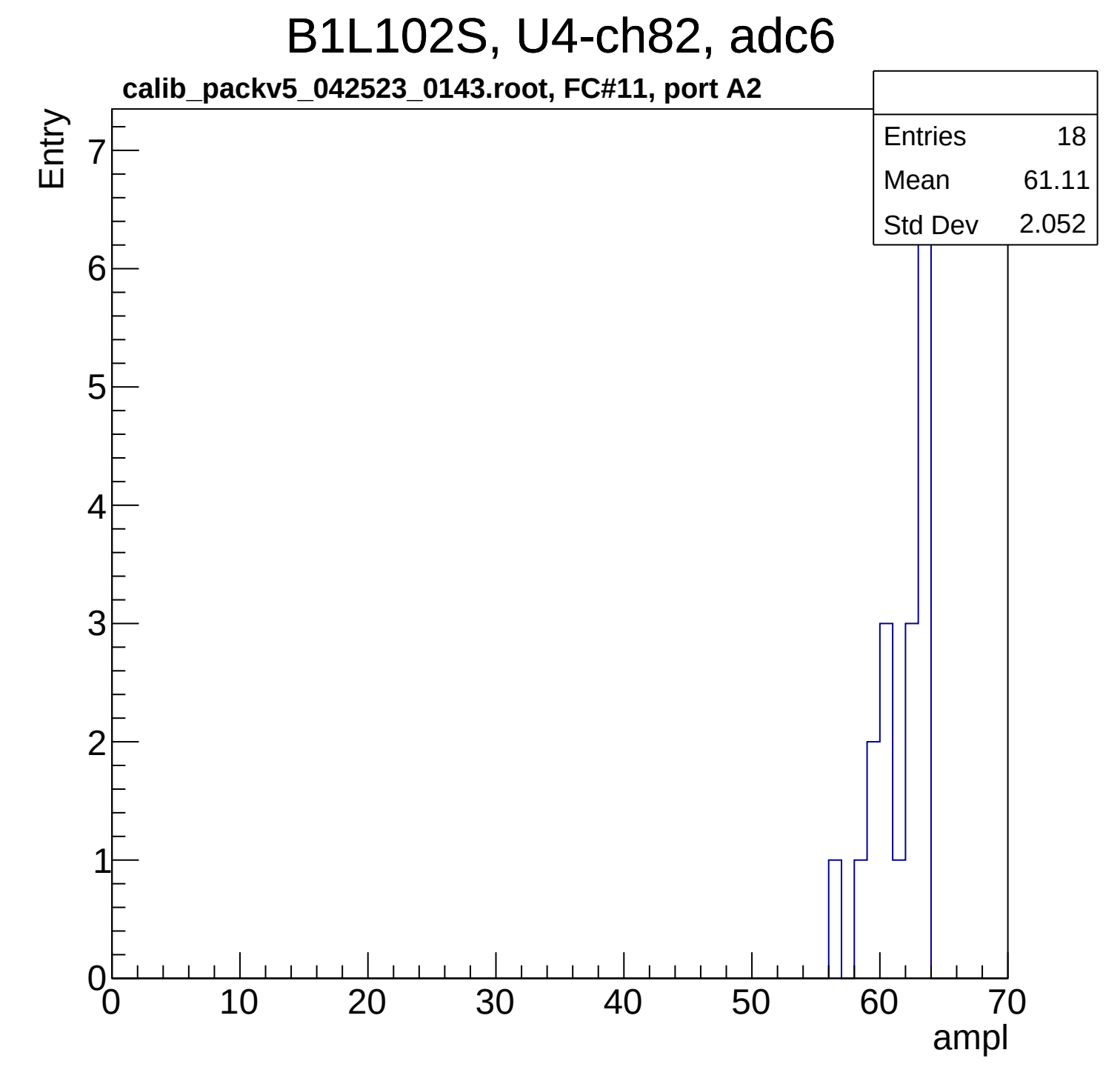
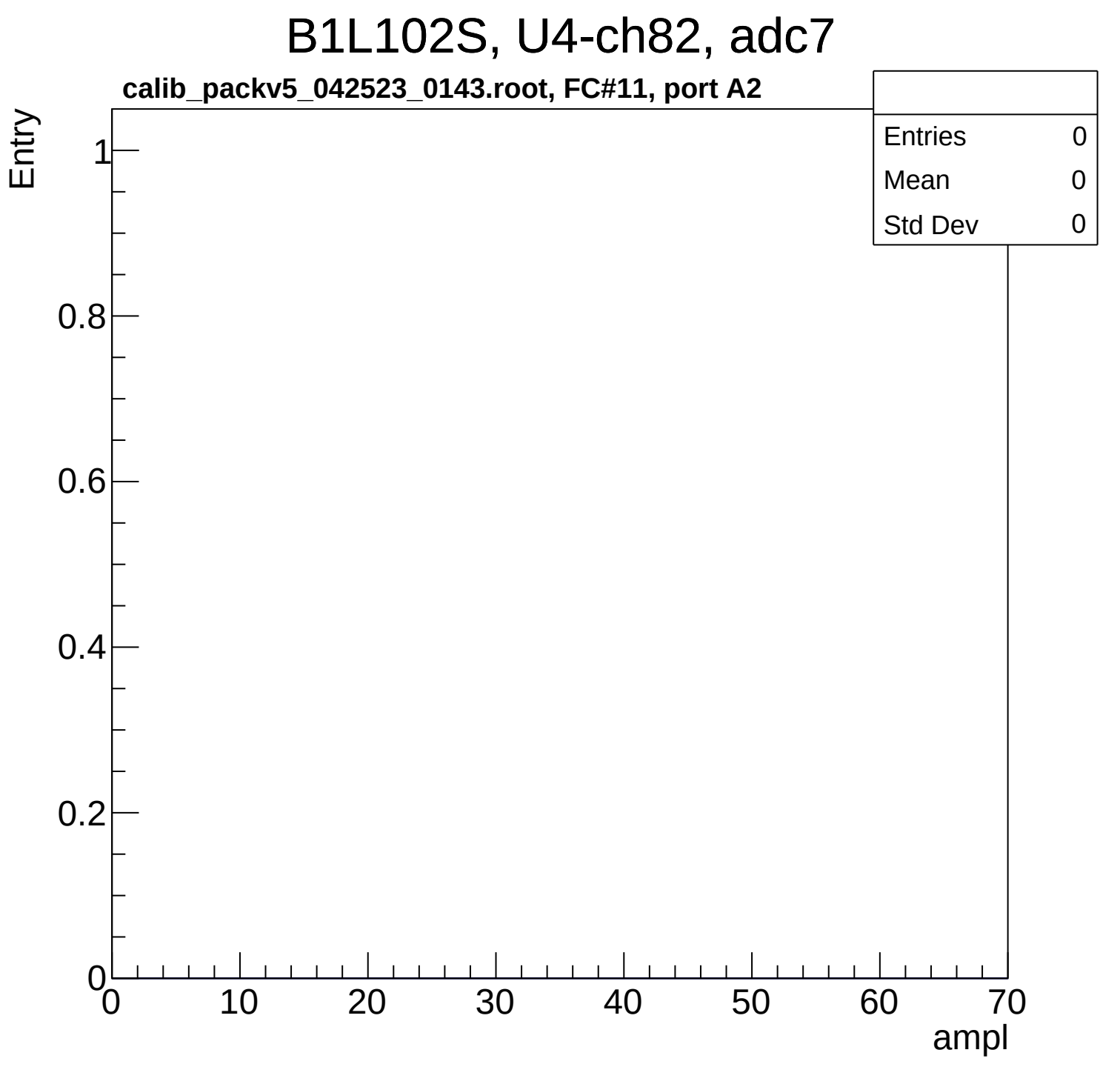
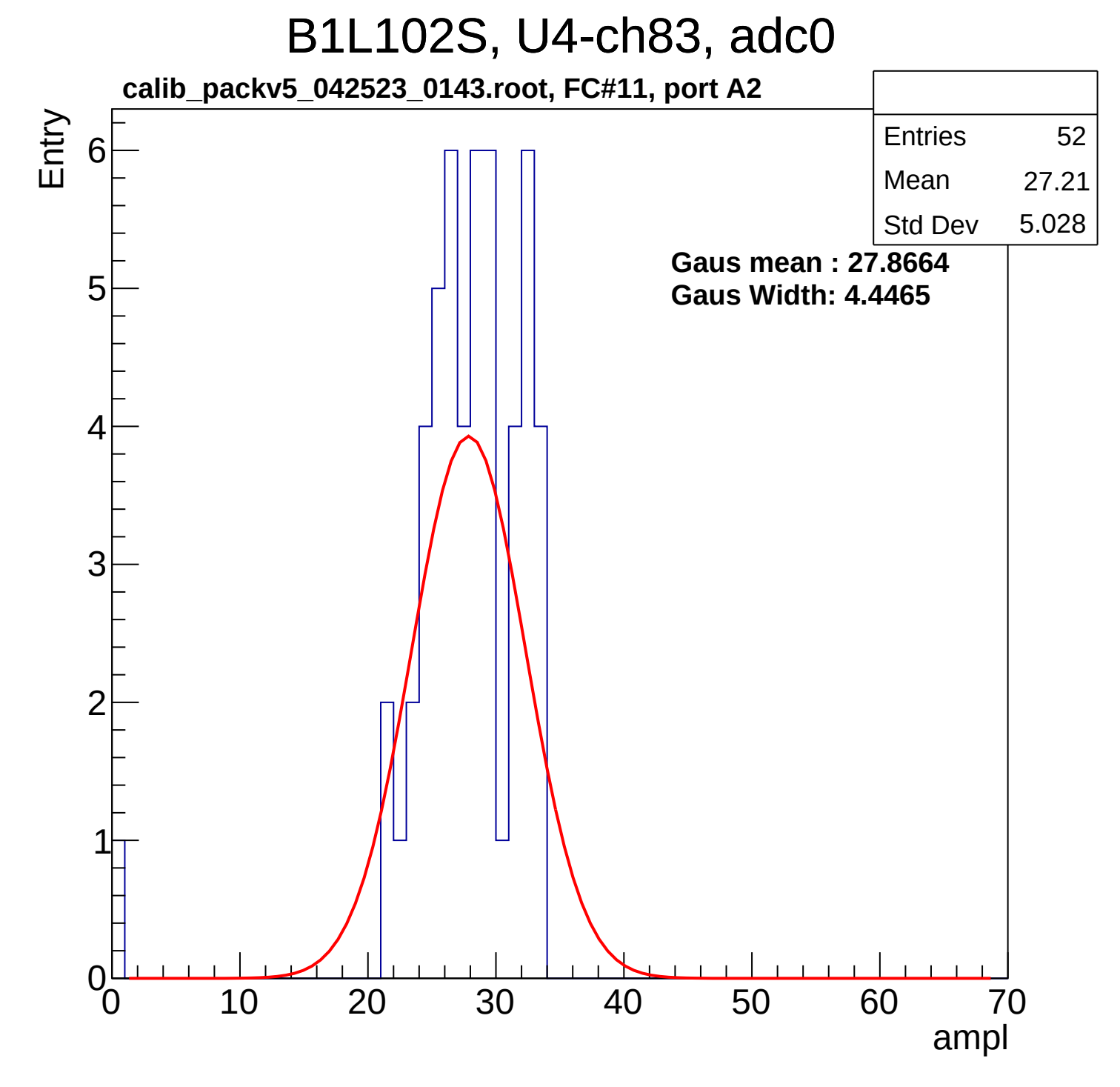
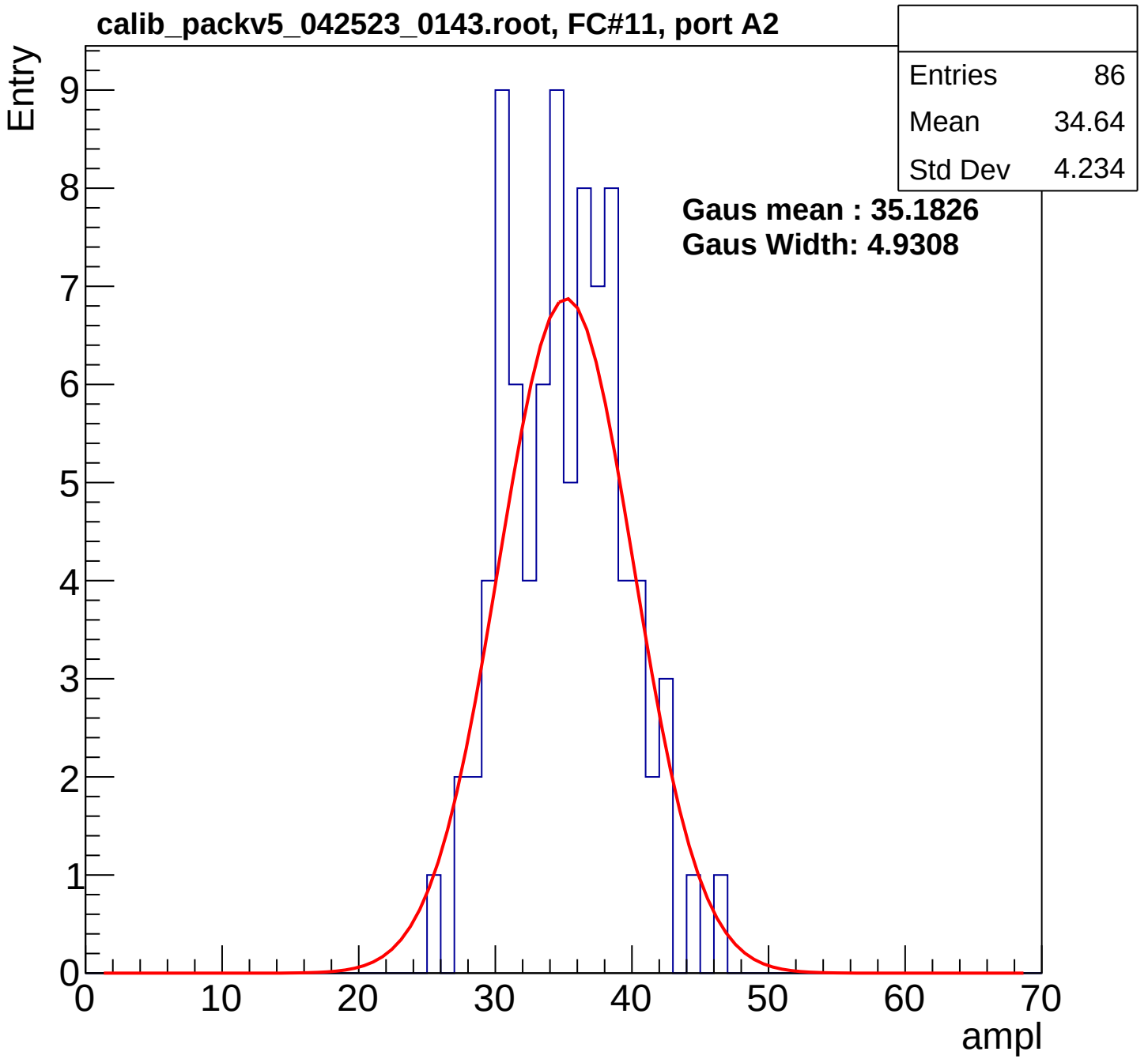
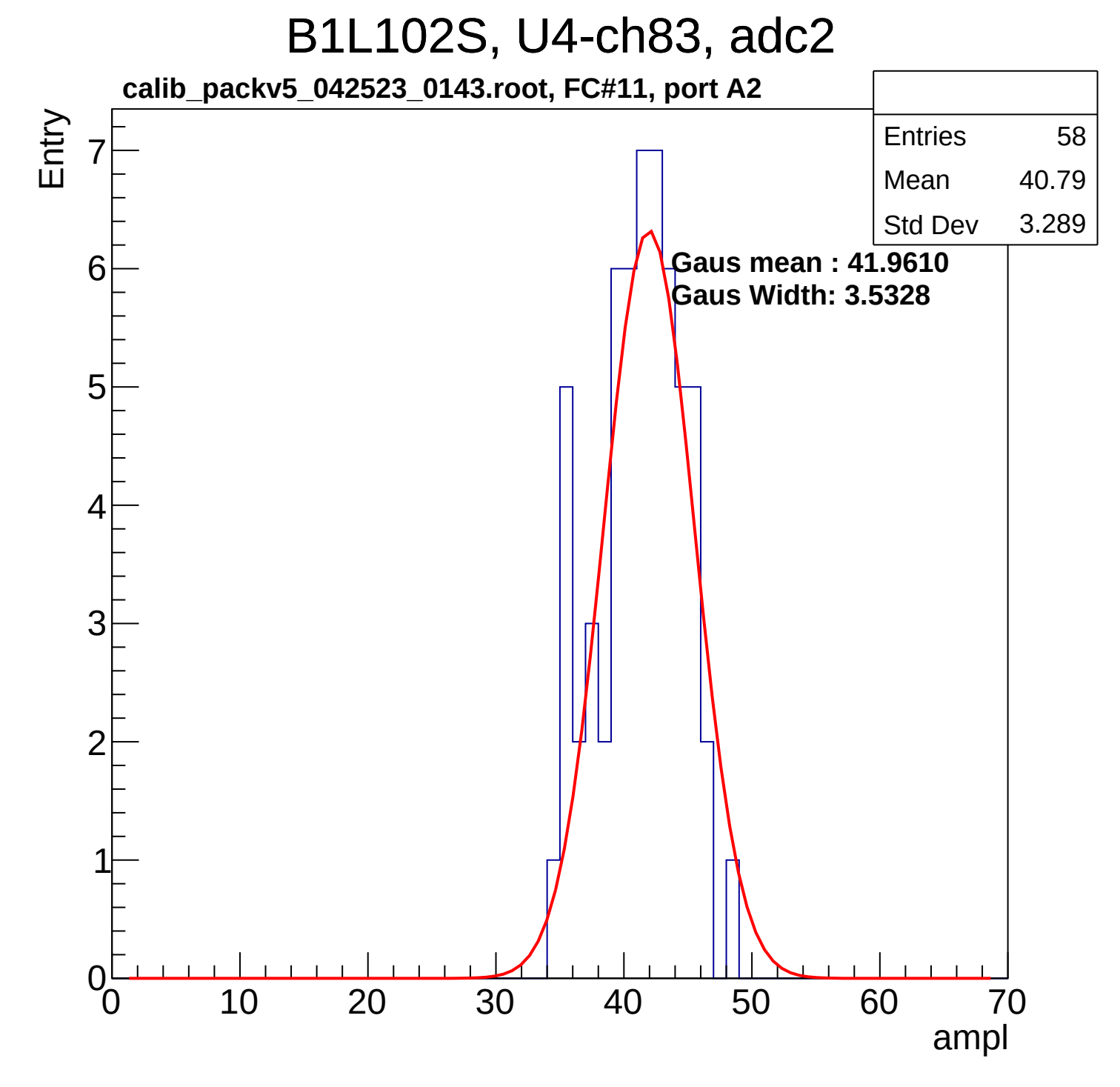
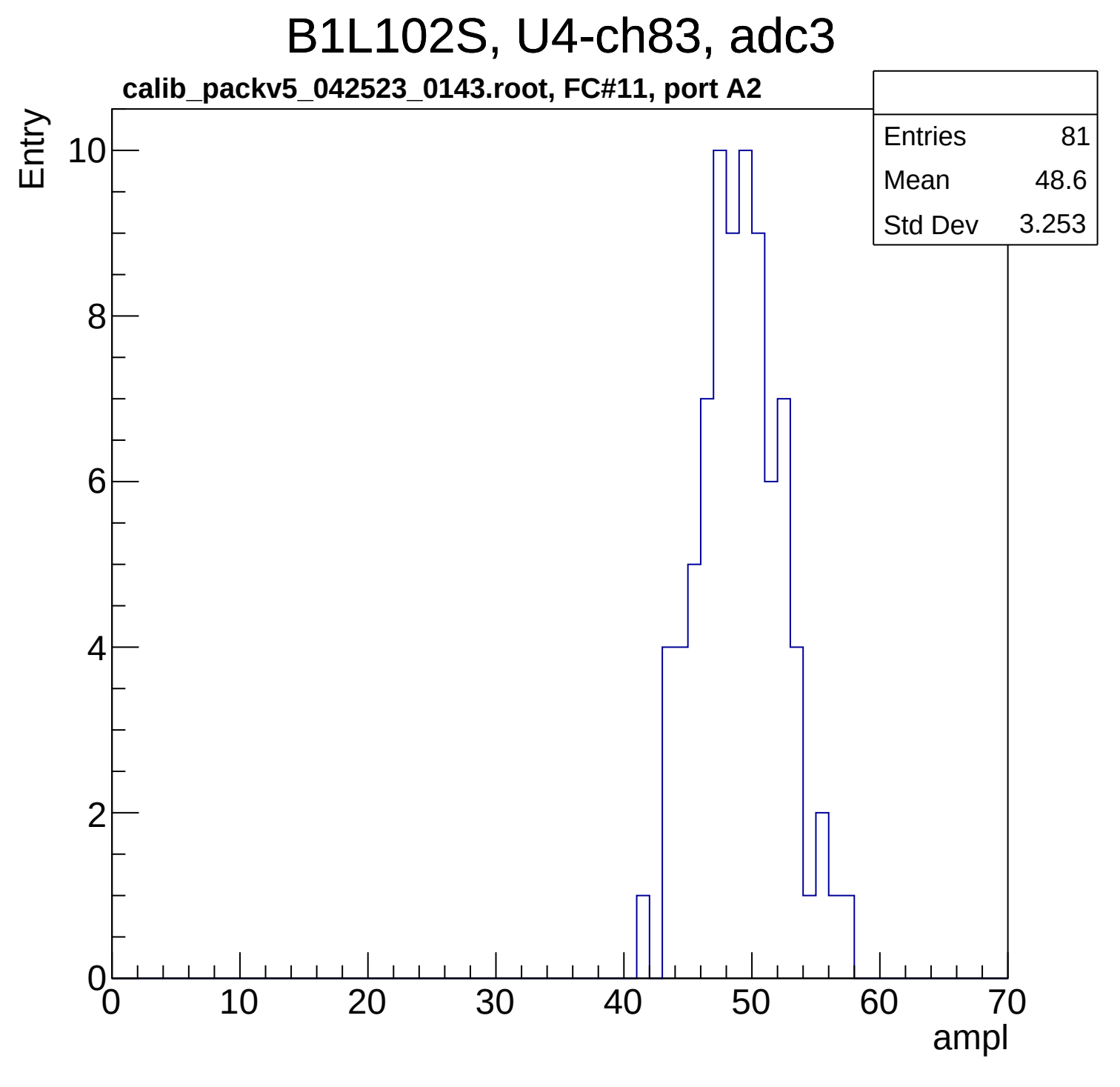

B1L102S, U4-ch82, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 18
Mean 61.11
Std Dev 2.052
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

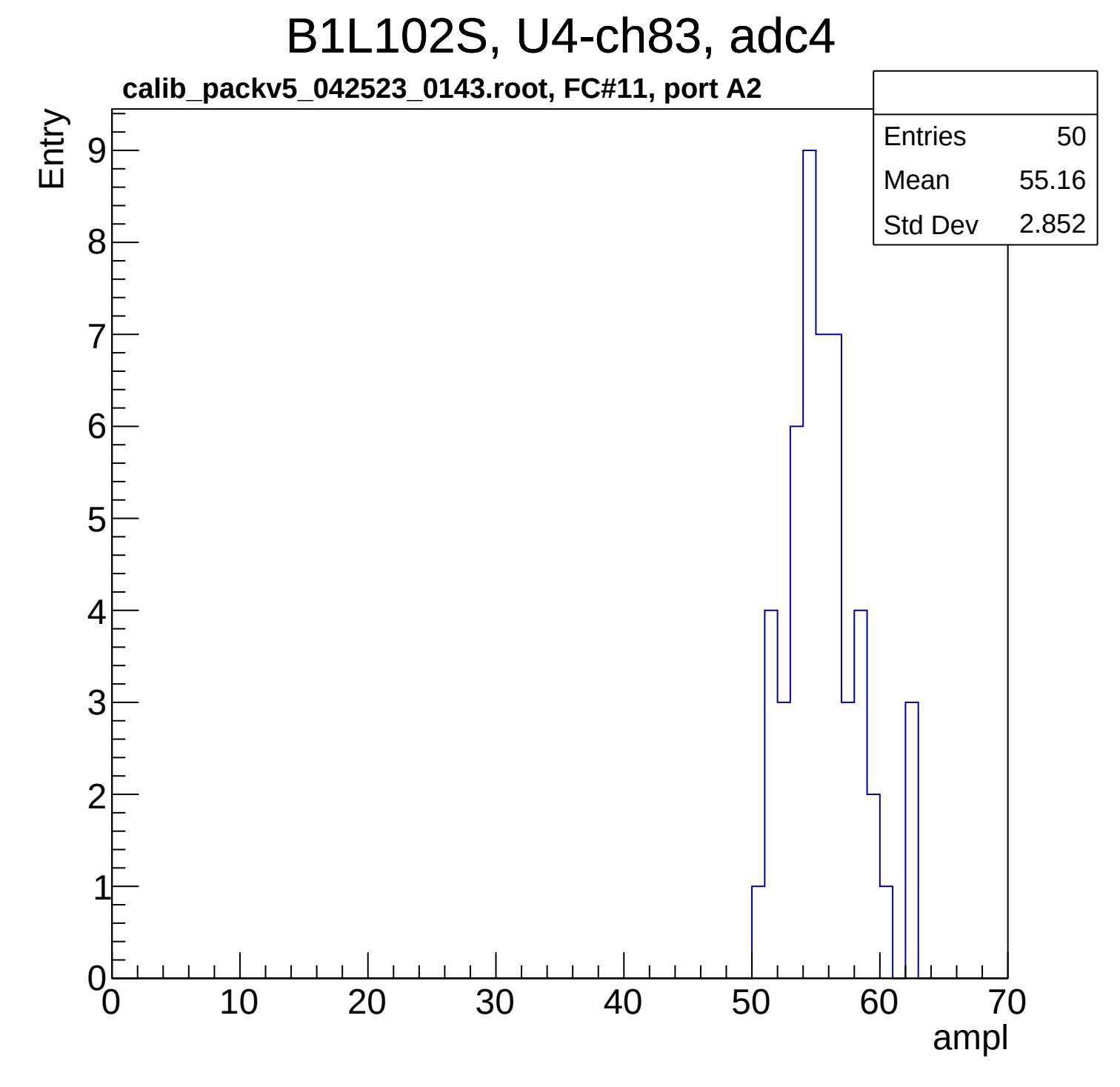

B1L102S, U4-ch82, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch83, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 52
Mean 27.21
Std Dev 5.028
Gaus mean : 27.8664
Gaus Width: 4.4465
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L102S, U4-ch83, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 86
Mean 34.64
Std Dev 4.234
Gaus mean : 35.1826
Gaus Width: 4.9308
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch83, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 40.79
Std Dev 3.289
Gaus mean : 41.9610
Gaus Width: 3.5328
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch83, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 81
Mean 48.6
Std Dev 3.253
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch83, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 50
Mean 55.16
Std Dev 2.852
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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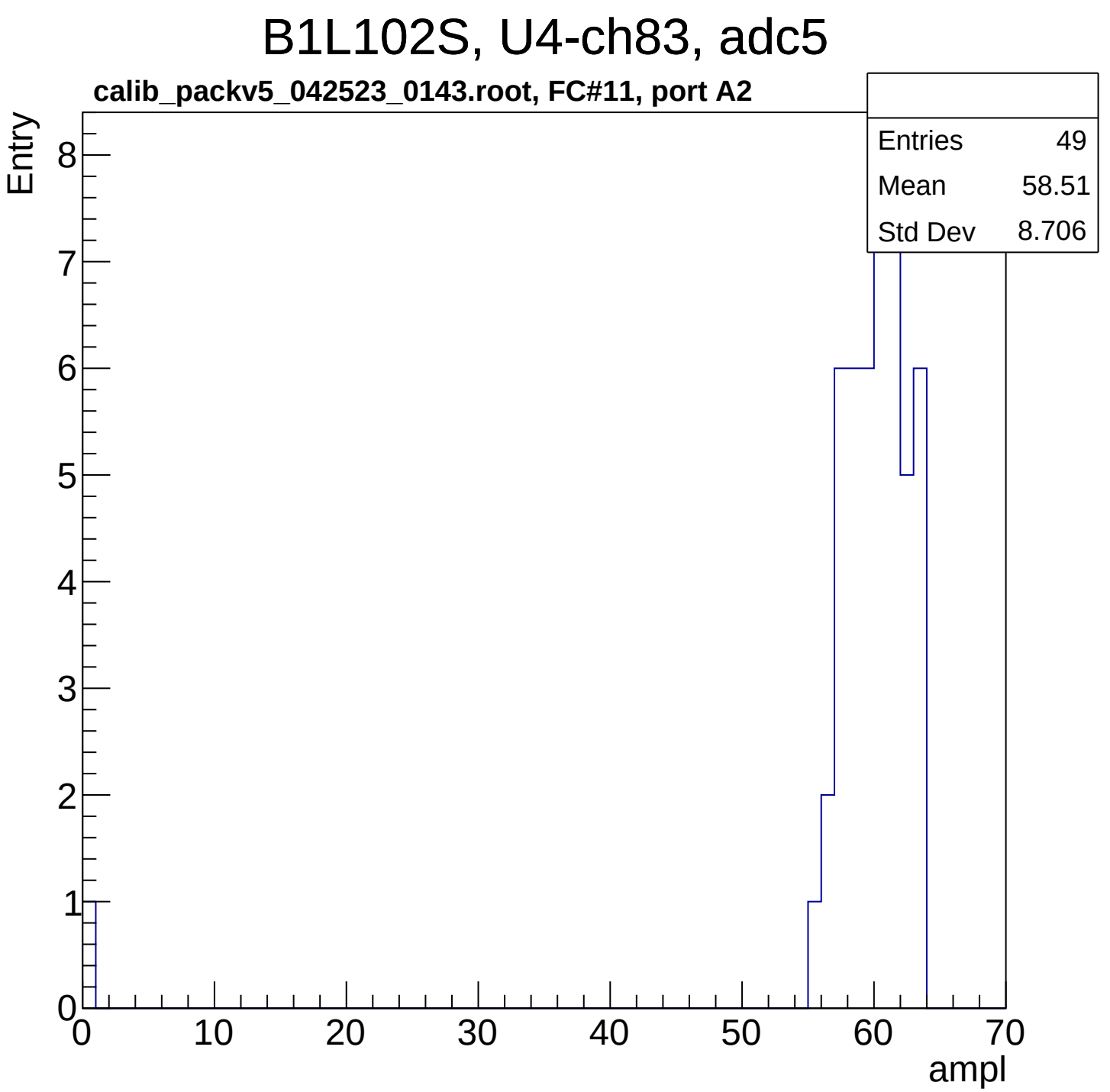
B1L102S, U4-ch83, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 58.51
Std Dev 8.706
Entry
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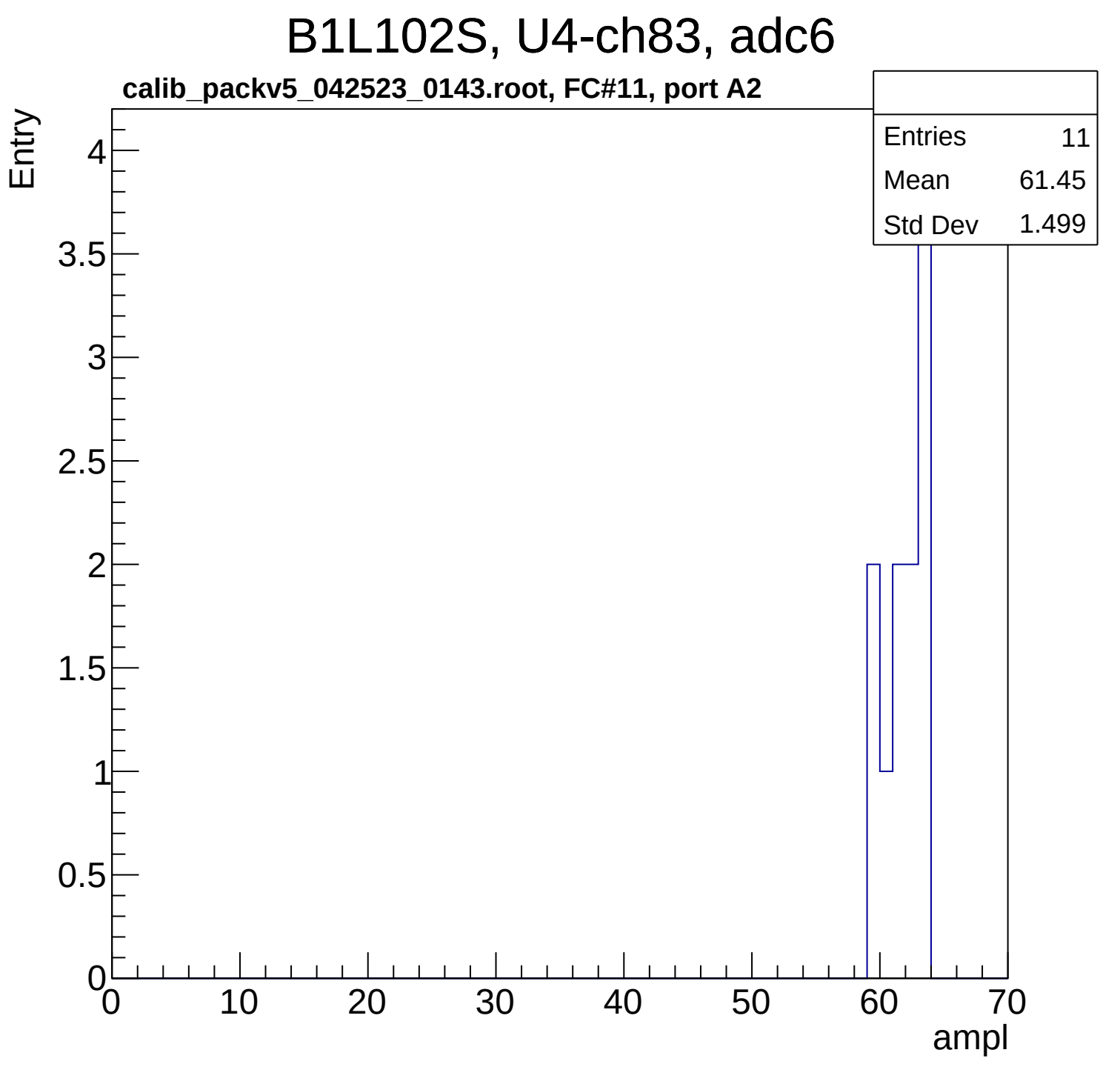
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch83, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 11
Mean 61.45
Std Dev 1.499
Entry
ampl
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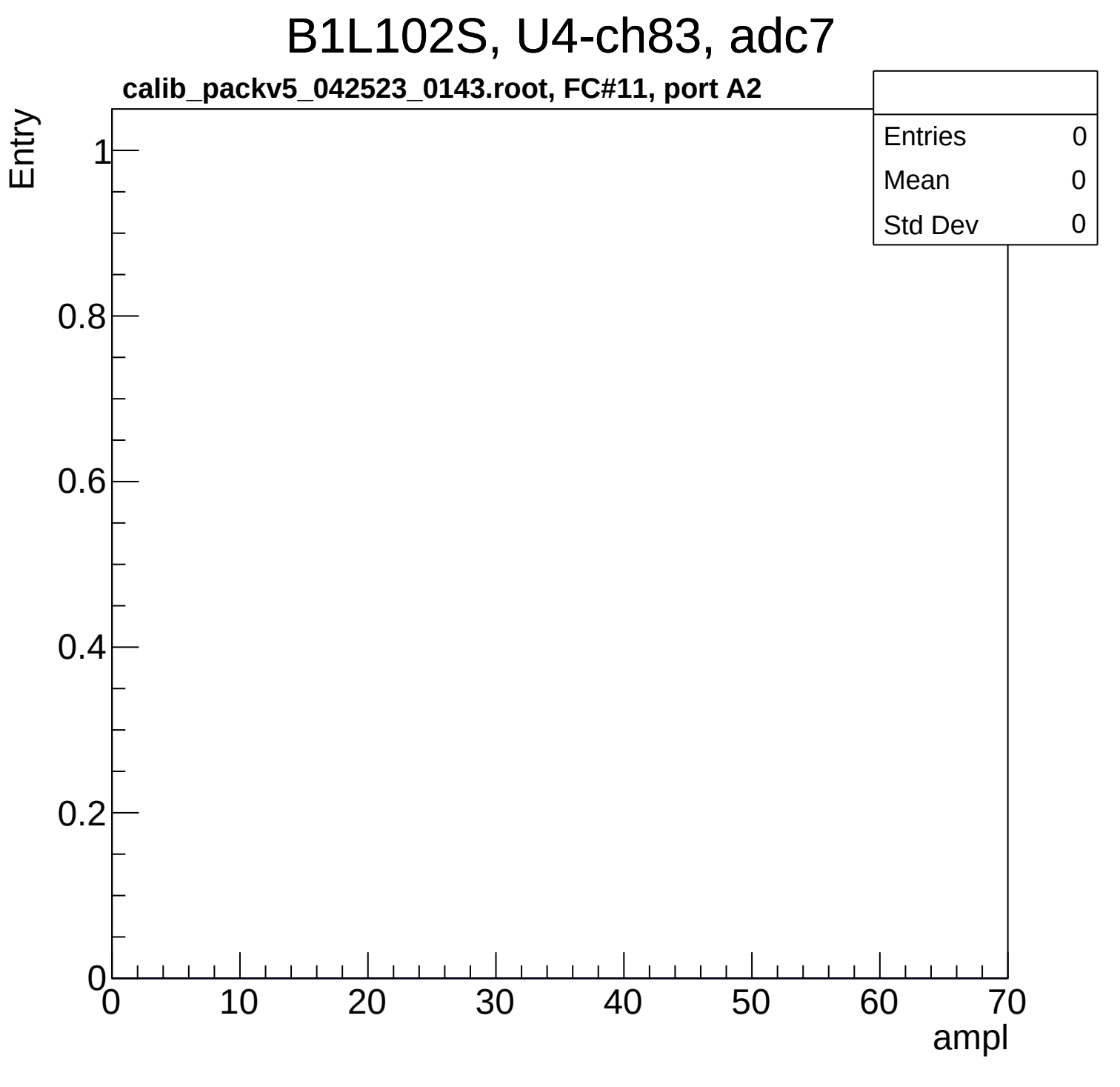
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U4-ch83, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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0.8
0.6
0.4
0.2
0
0
10
20
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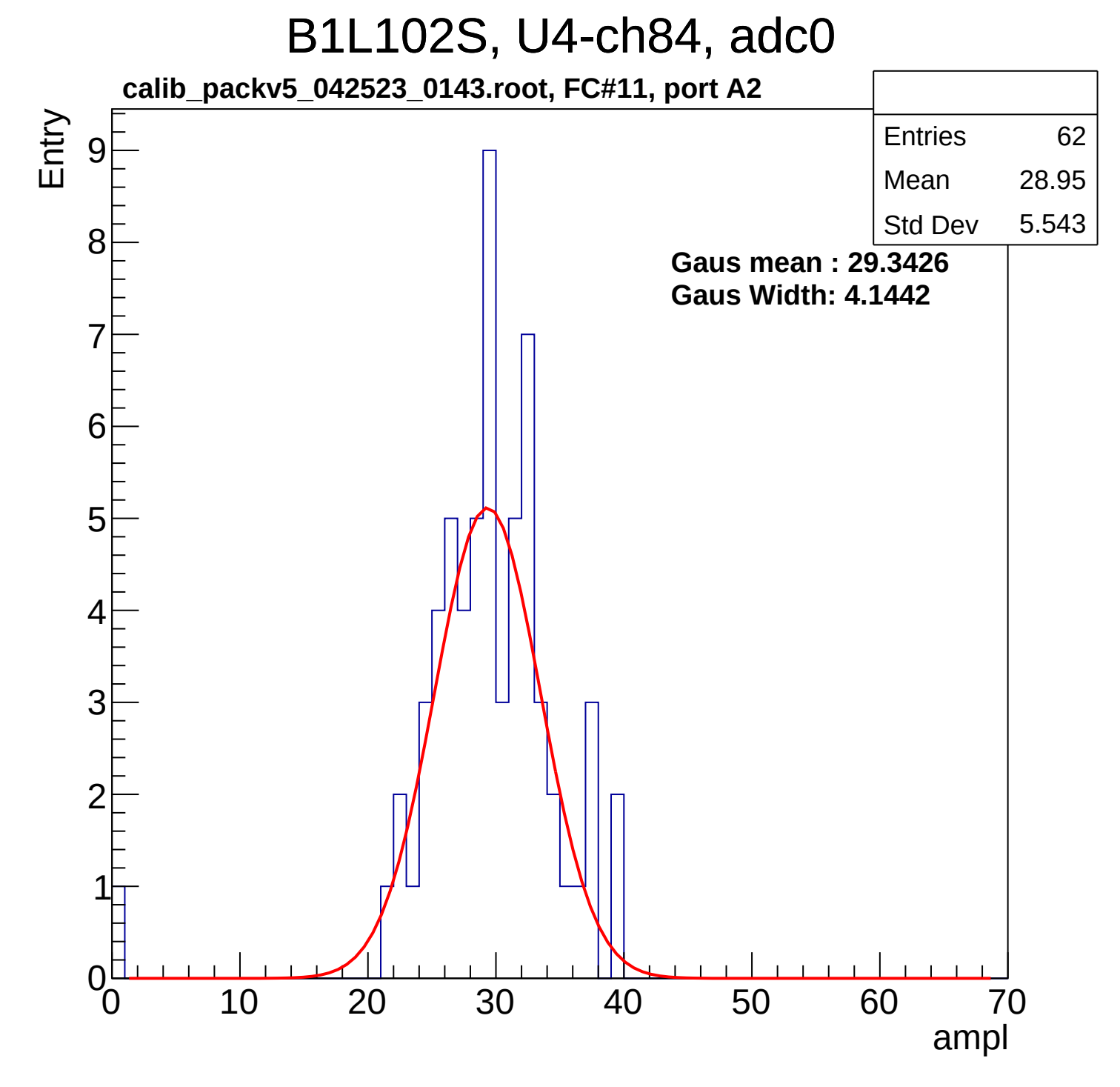
40
50
60
70
ampl


B1L102S, U4-ch84, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 28.95
Std Dev 5.543
Gaus mean : 29.3426
Gaus Width: 4.1442
Entry
ampl
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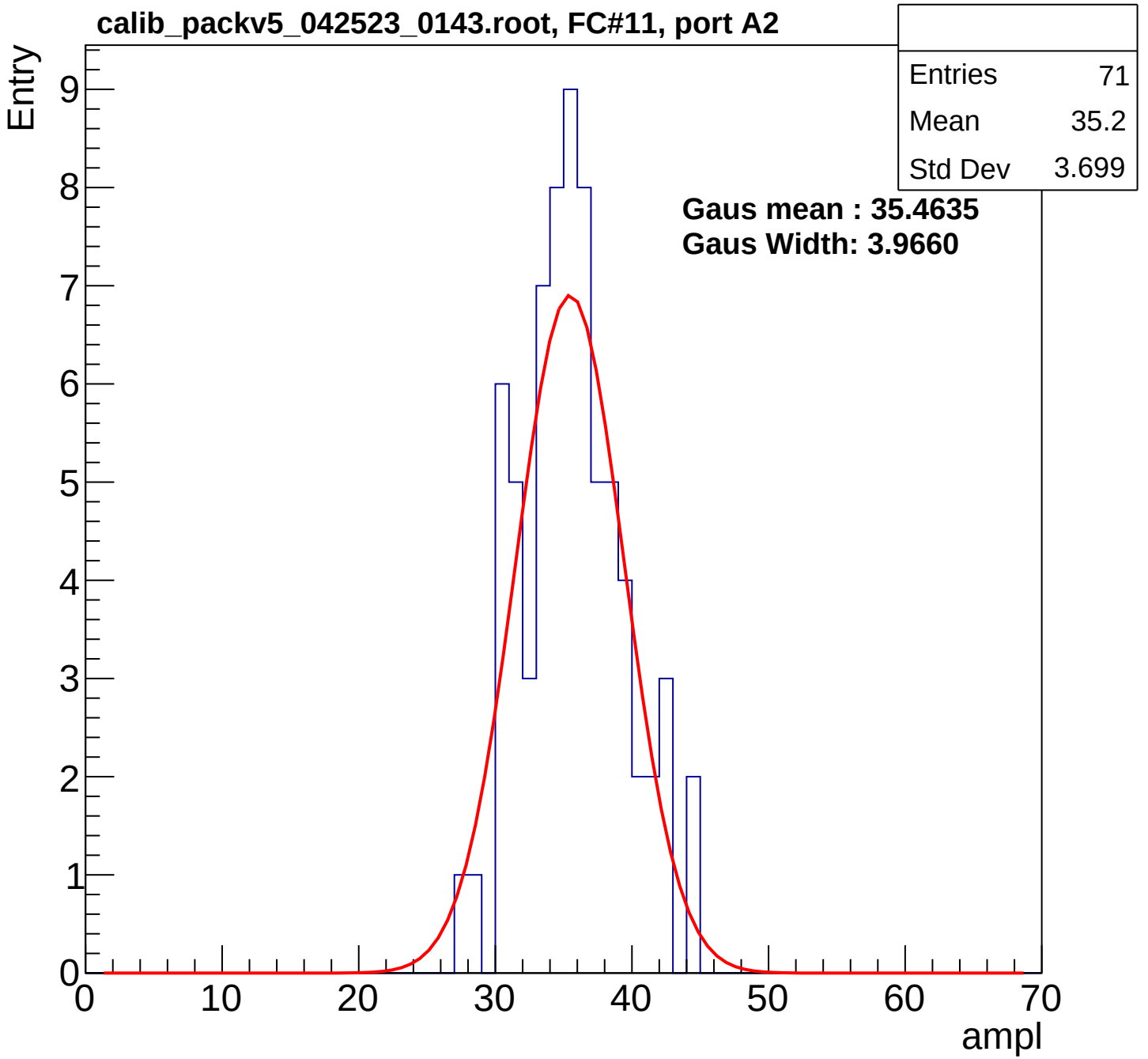
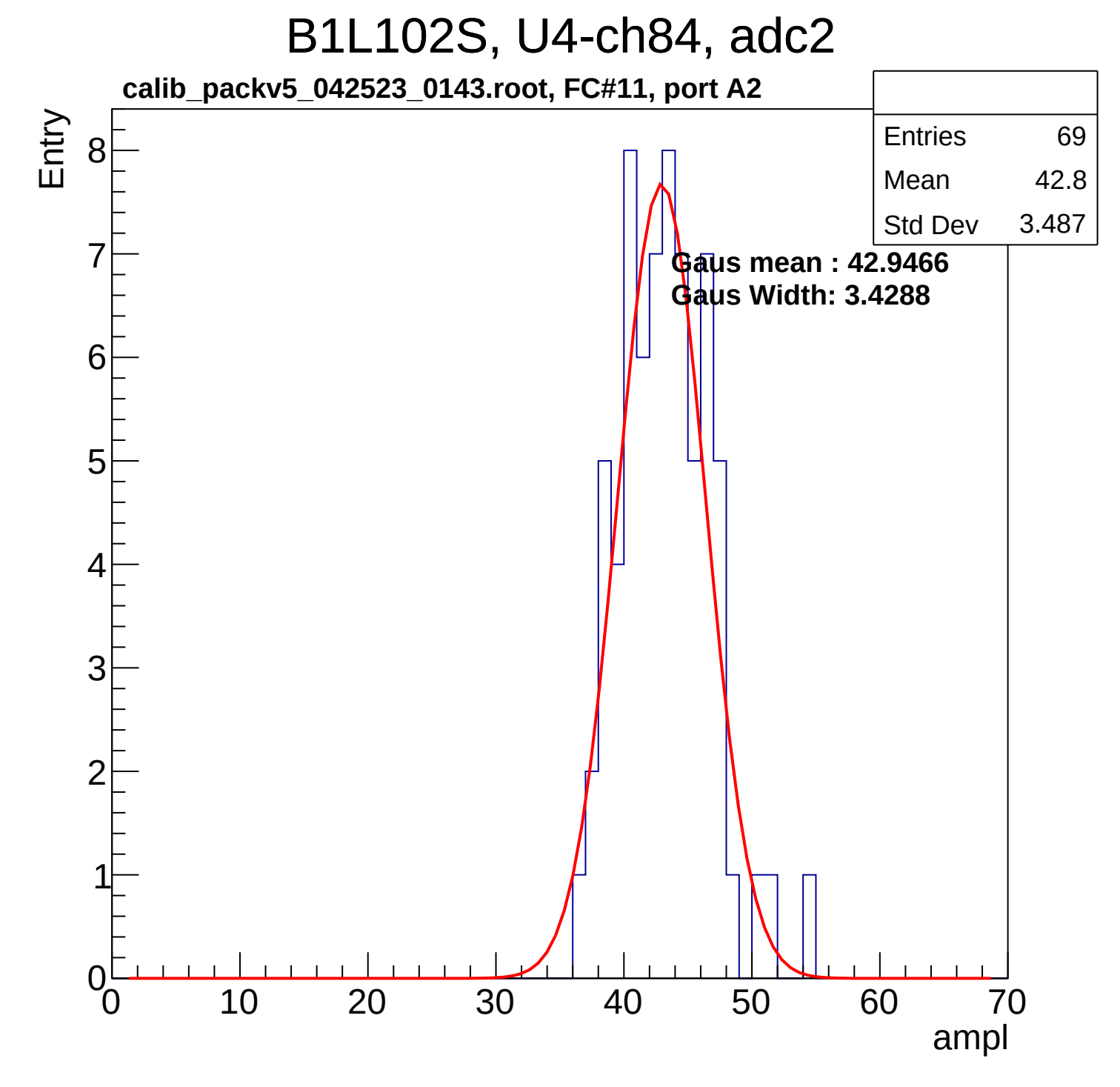
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch84, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 35.2
Std Dev 3.699
Gaus mean : 35.4635
Gaus Width: 3.9660
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch84, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 42.8
Std Dev 3.487
Gaus mean : 42.9466
Gaus Width: 3.4288
Entry
ampl
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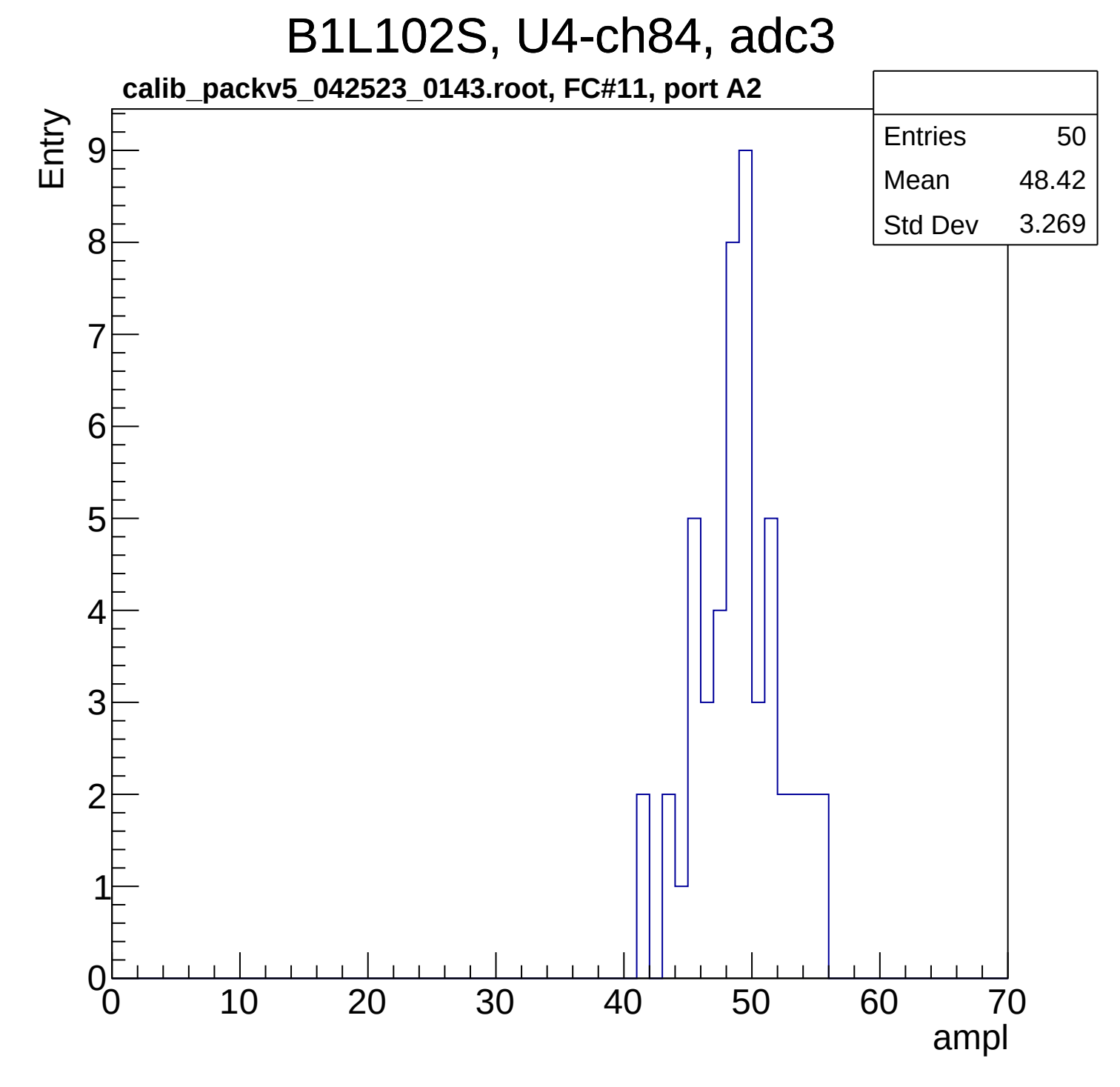
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch84, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 50
Mean 48.42
Std Dev 3.269
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
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60
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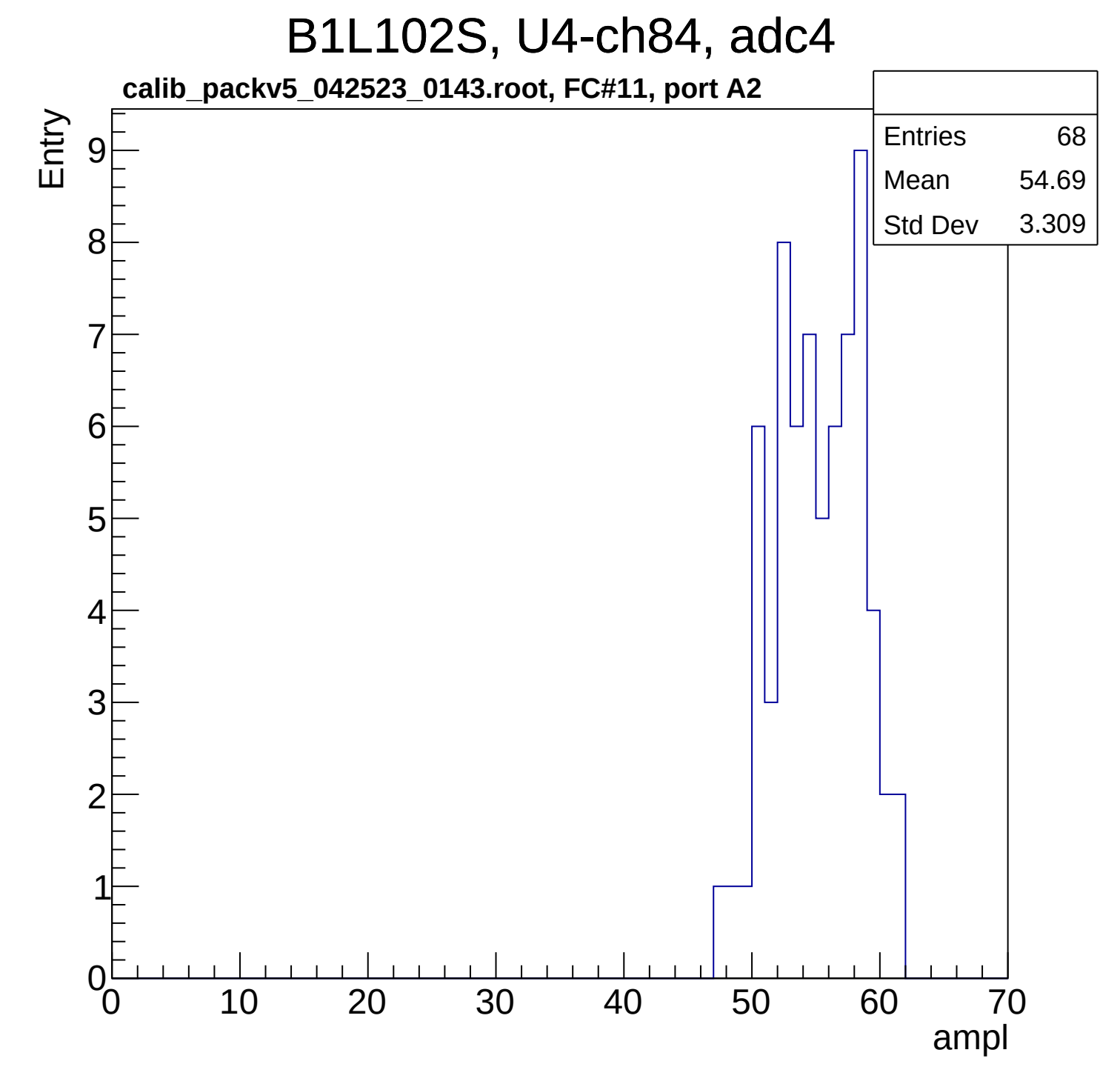
B1L102S, U4-ch84, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 54.69
Std Dev 3.309
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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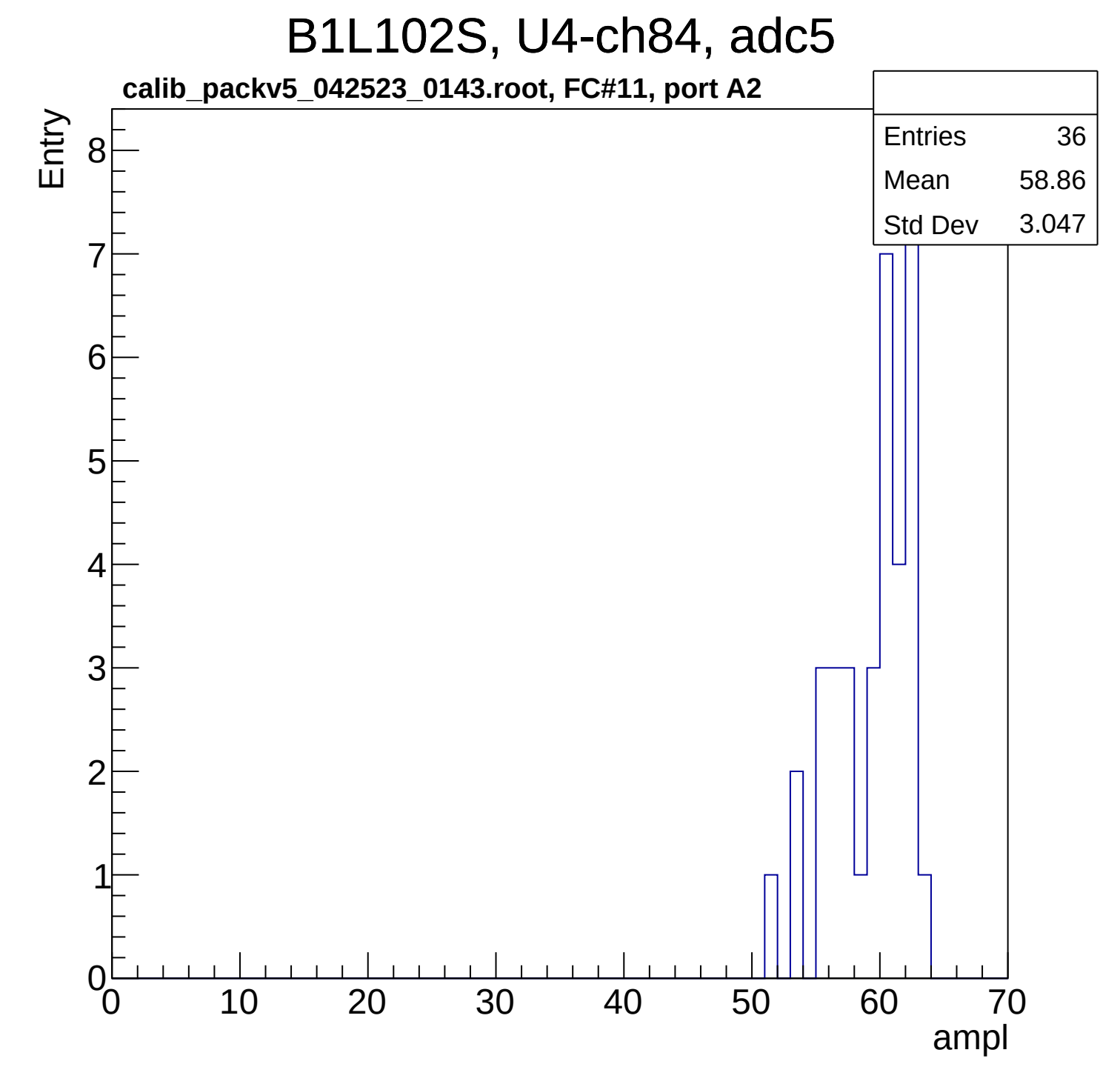
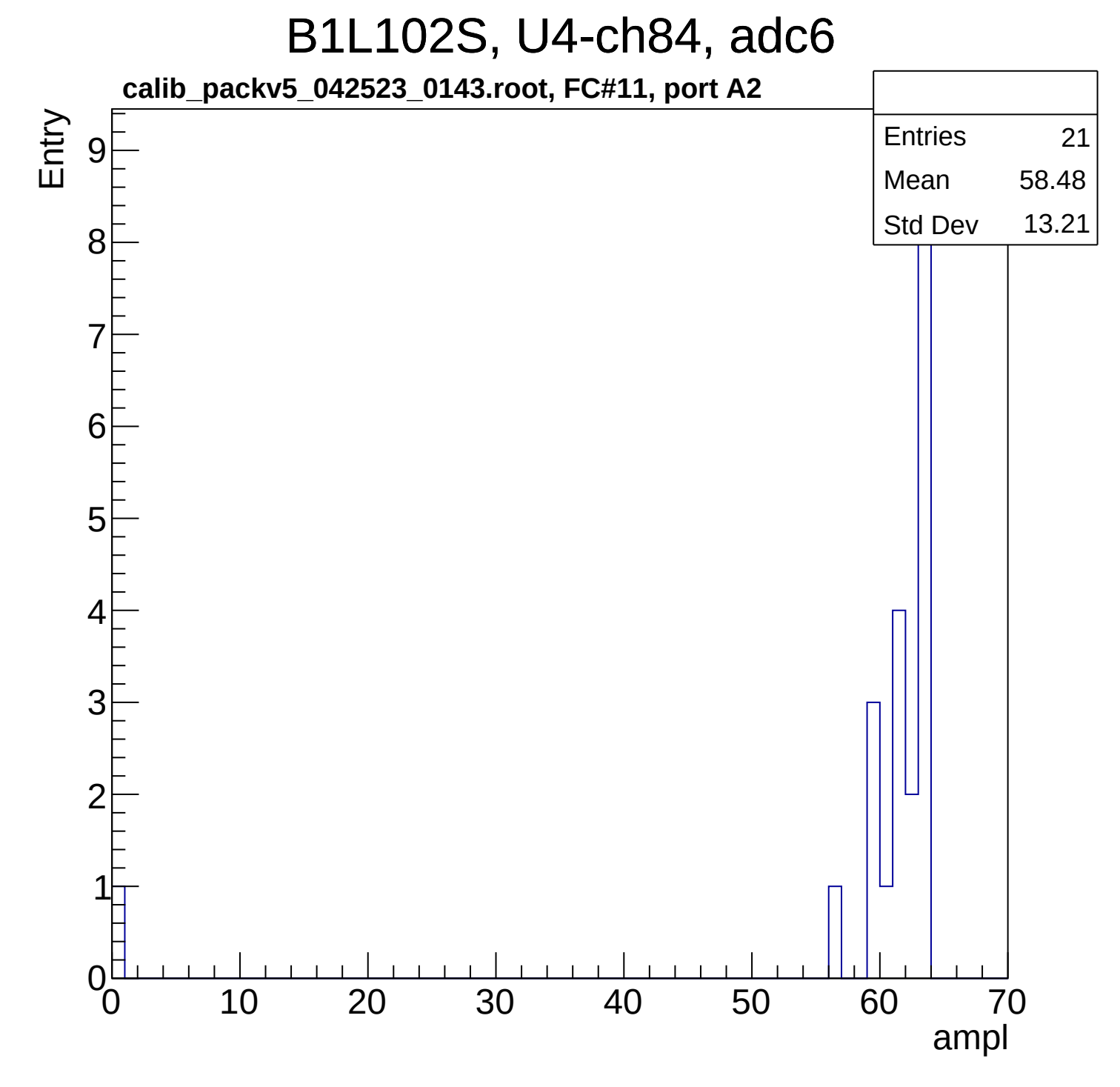

B1L102S, U4-ch84, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 36
Mean 58.86
Std Dev 3.047
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch84, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 21
Mean 58.48
Std Dev 13.21
Entry
ampl
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3
4
5
6
7
8
9
0
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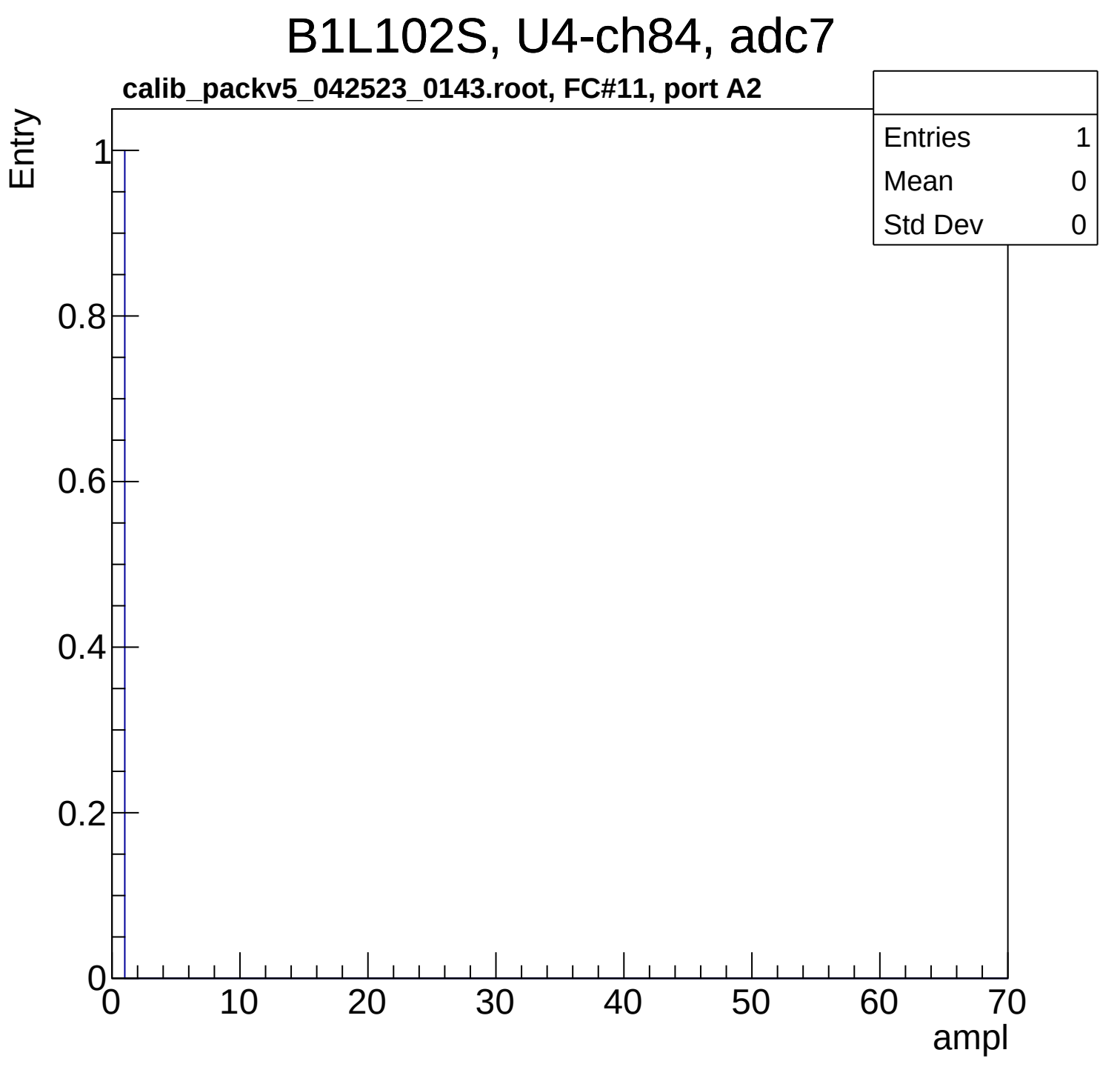
B1L102S, U4-ch84, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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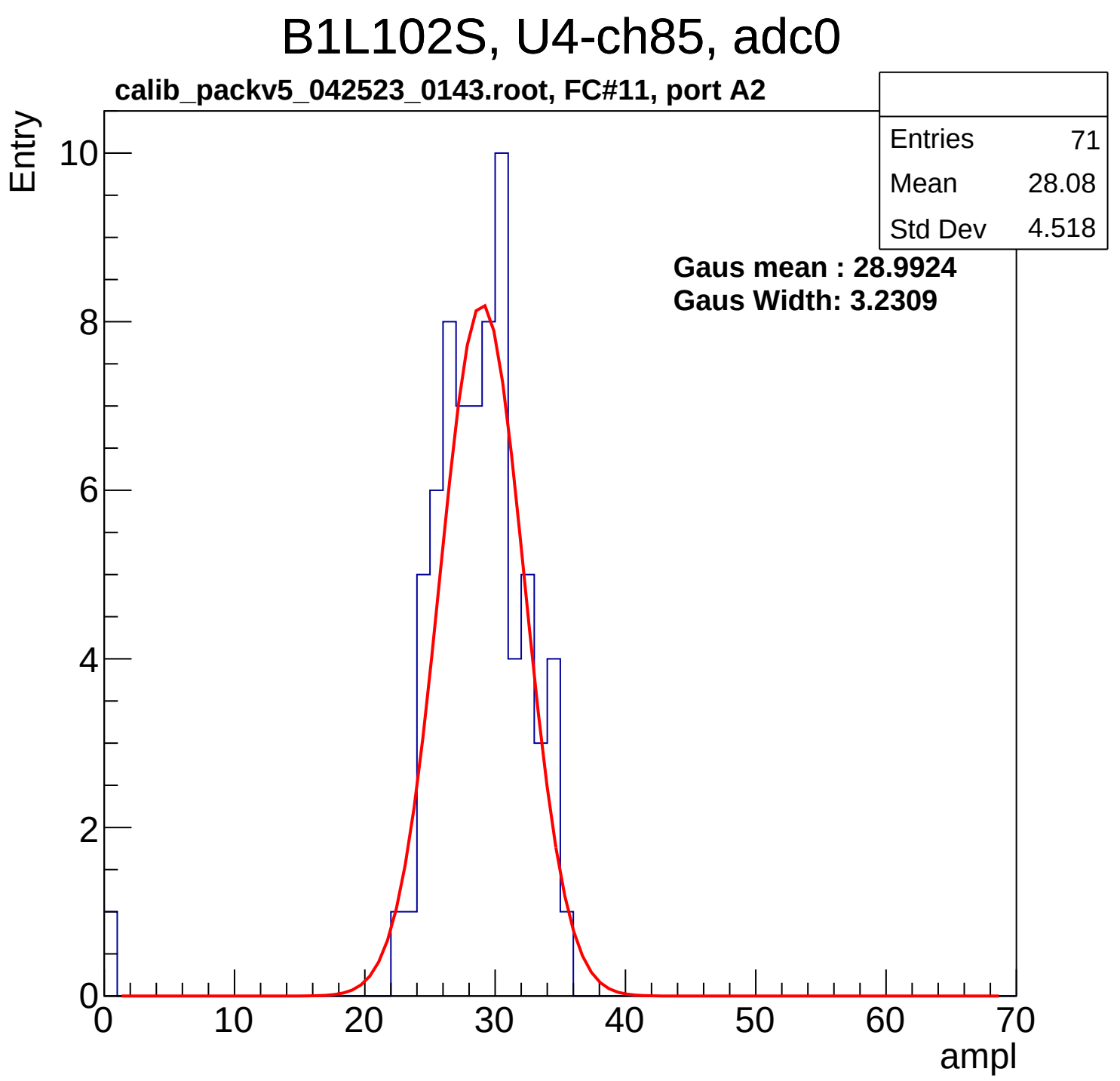
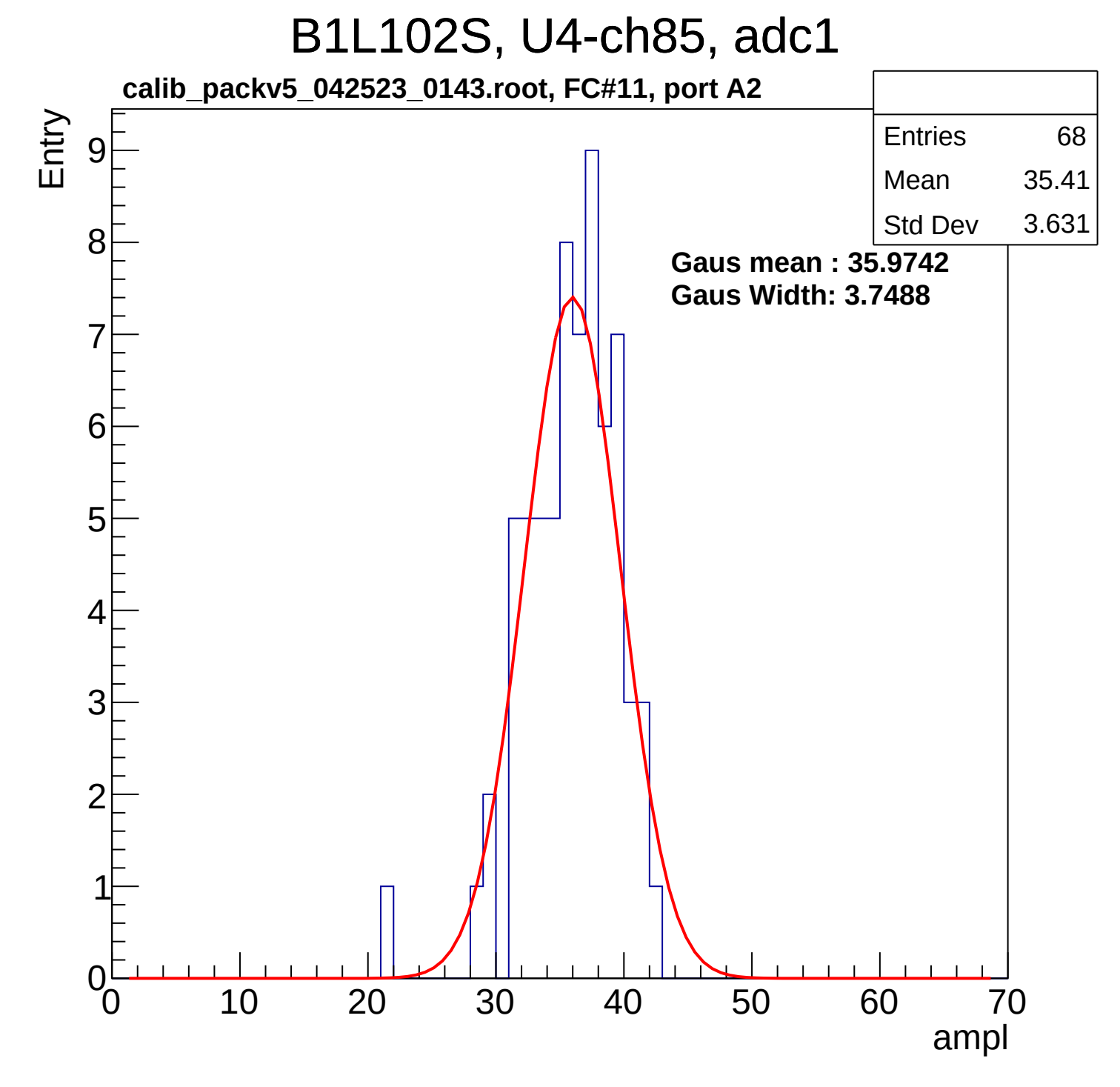
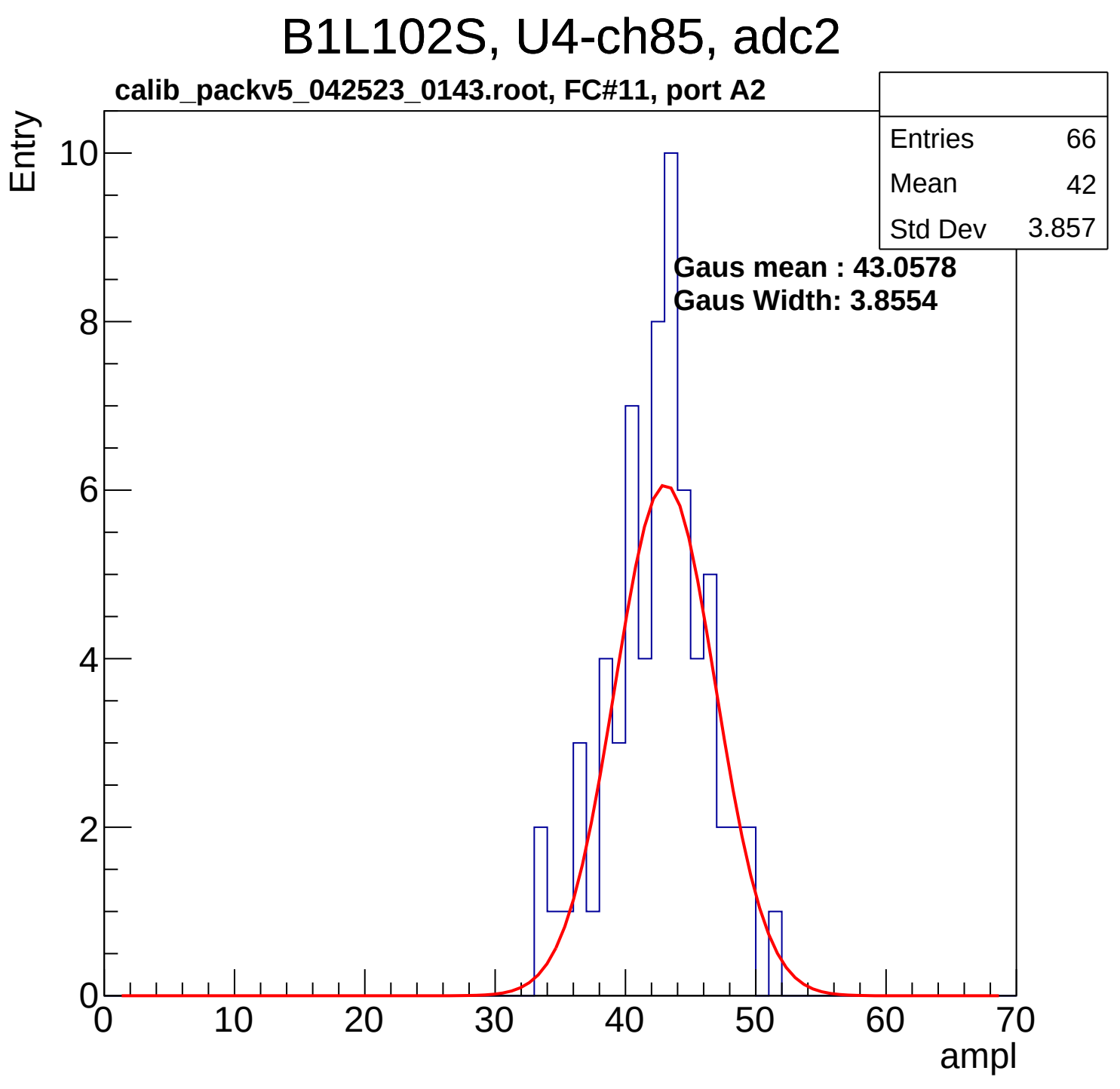
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch85, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 28.08
Std Dev 4.518
Gaus mean : 28.9924
Gaus Width: 3.2309
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch85, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 35.41
Std Dev 3.631
Gaus mean : 35.9742
Gaus Width: 3.7488
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L102S, U4-ch85, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 42
Std Dev 3.857
Gaus mean : 43.0578
Gaus Width: 3.8554
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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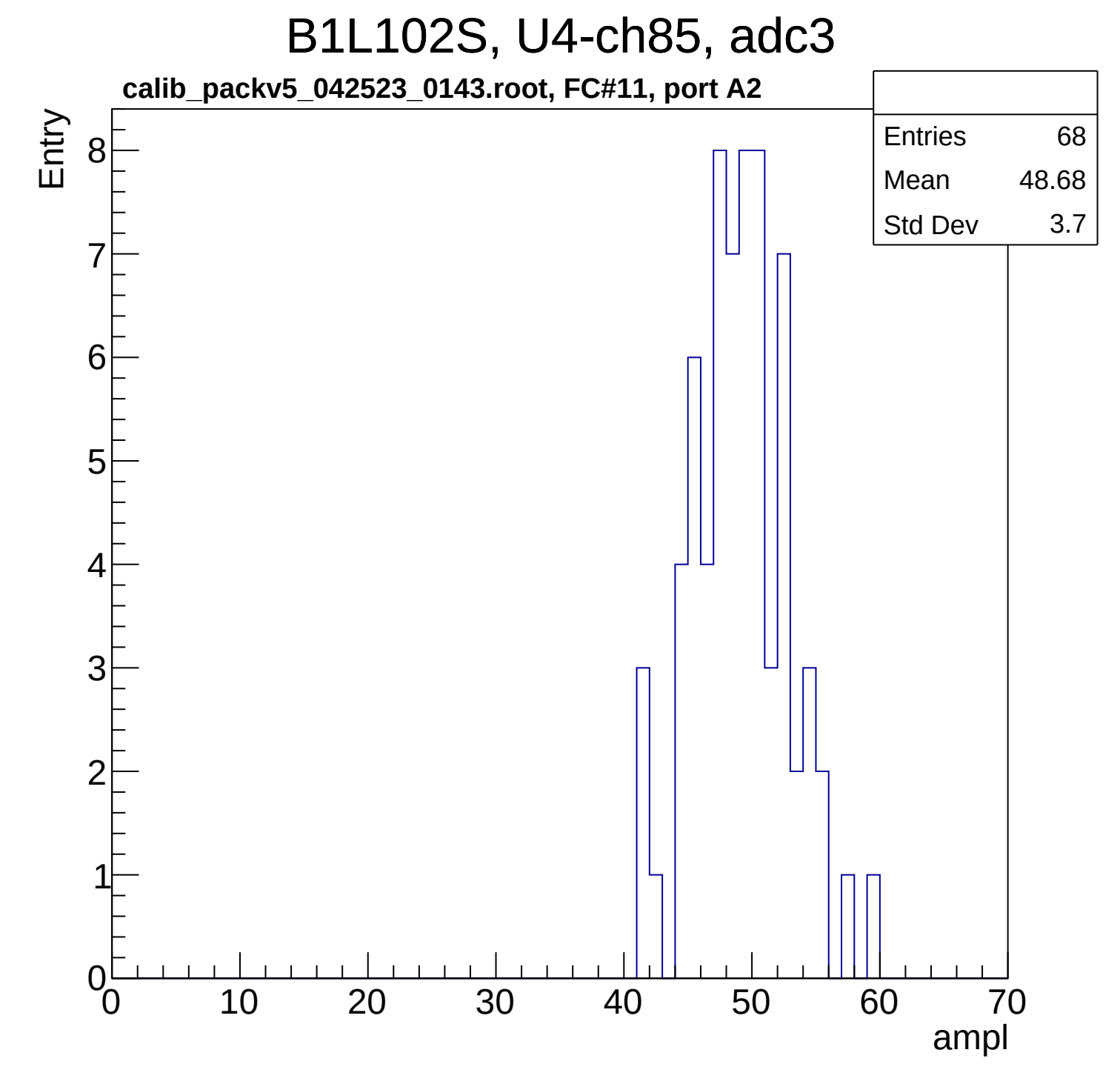
B1L102S, U4-ch85, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 48.68
Std Dev 3.7
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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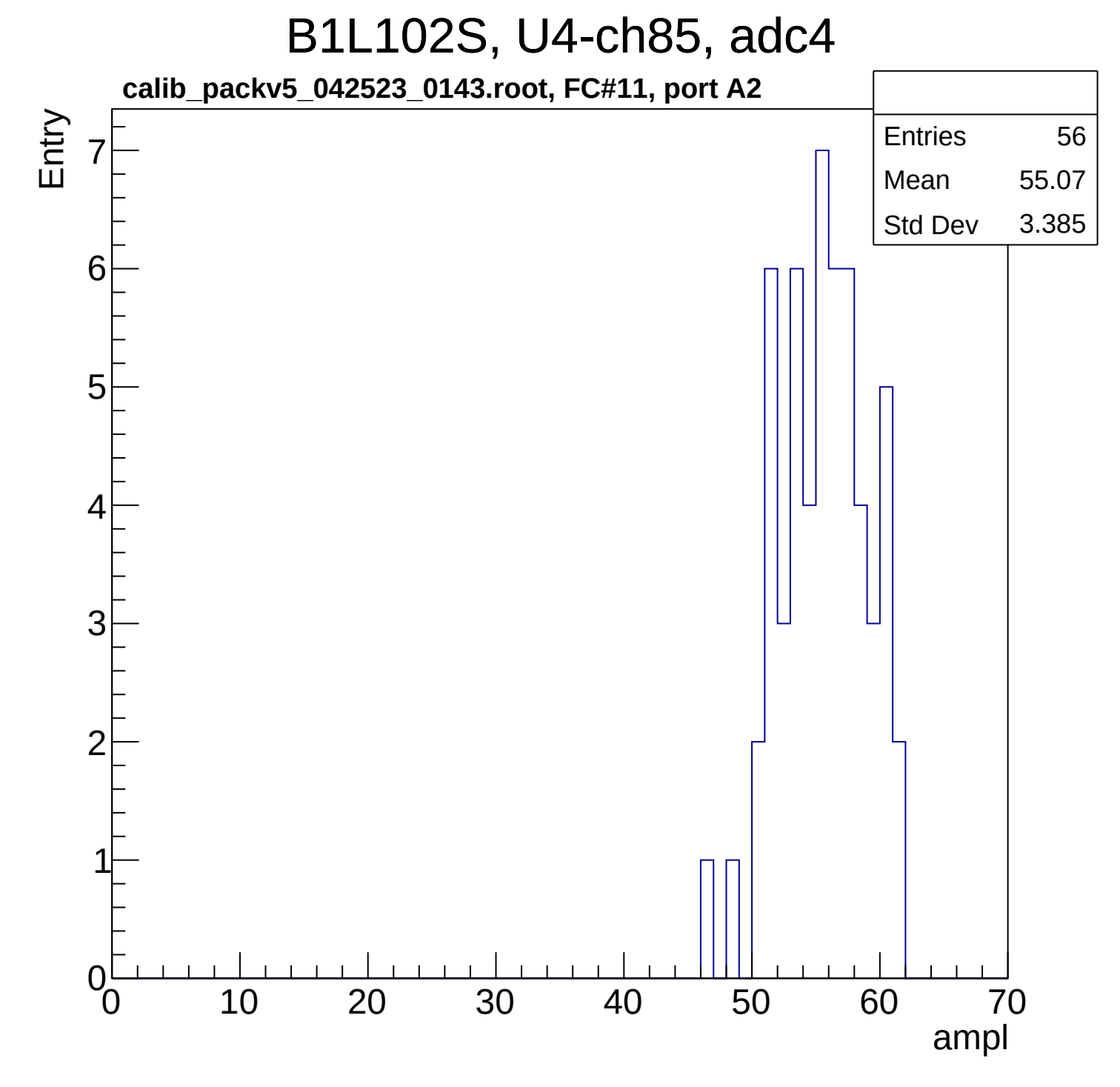
B1L102S, U4-ch85, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 55.07
Std Dev 3.385
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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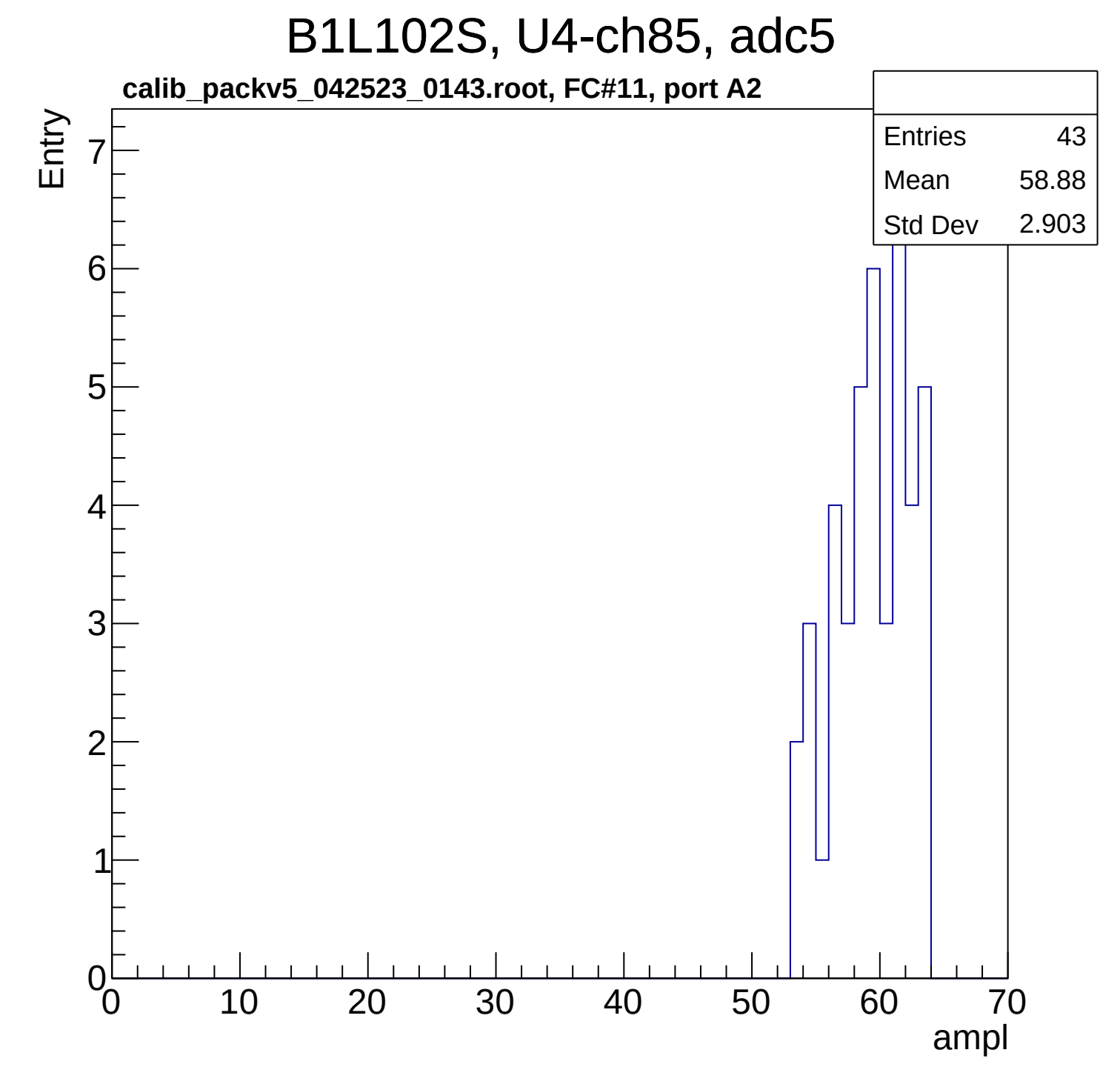
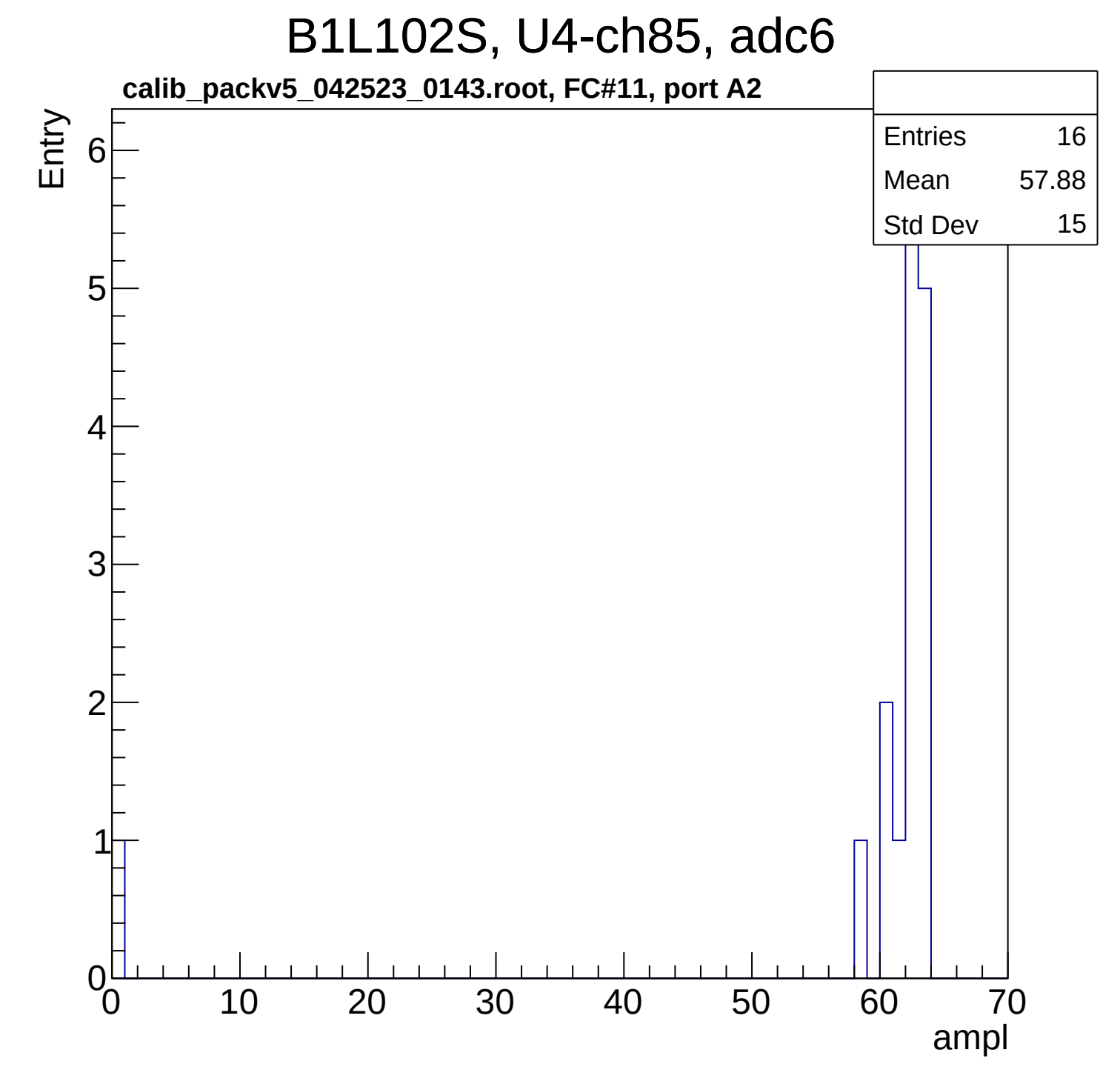
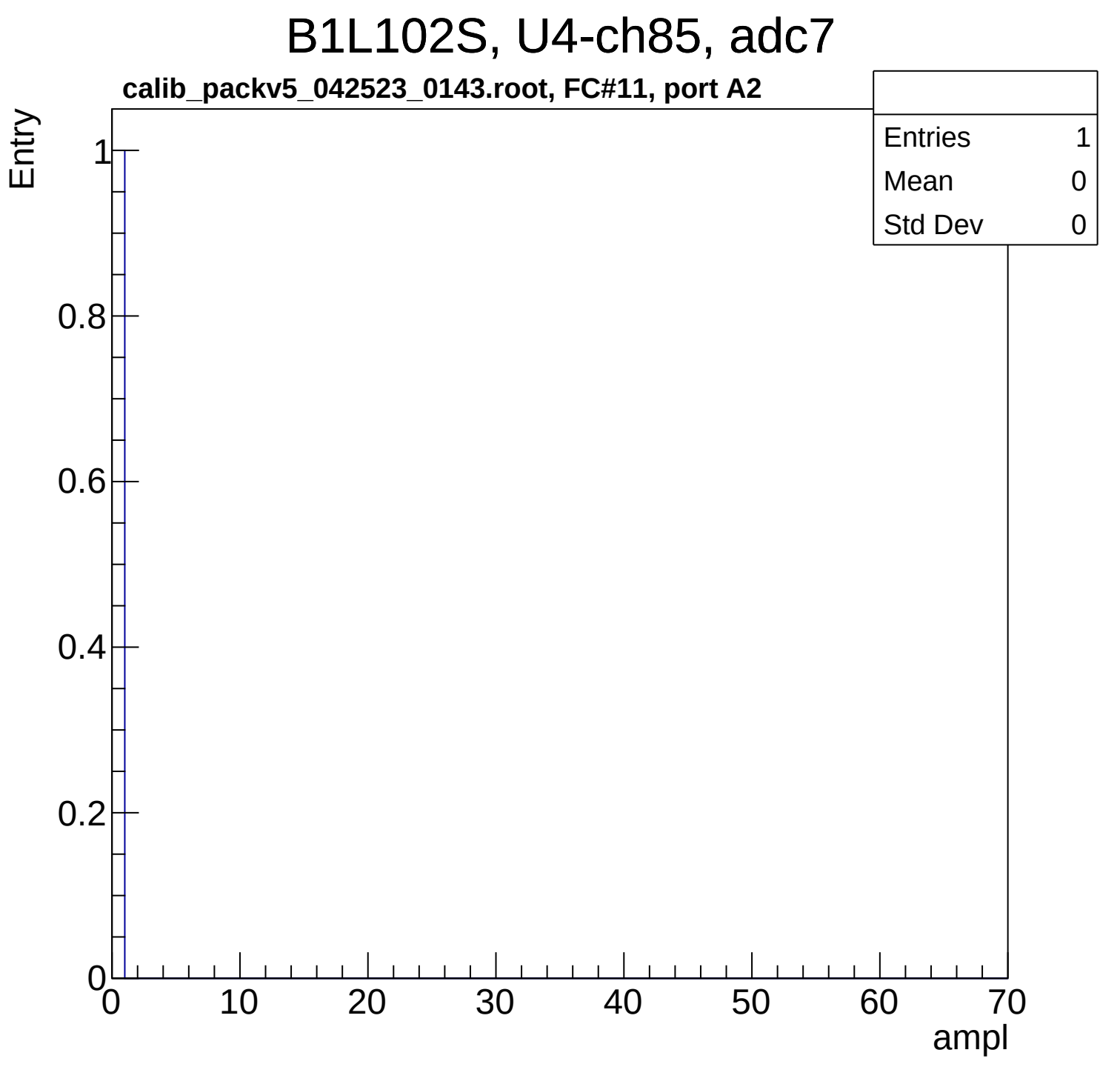
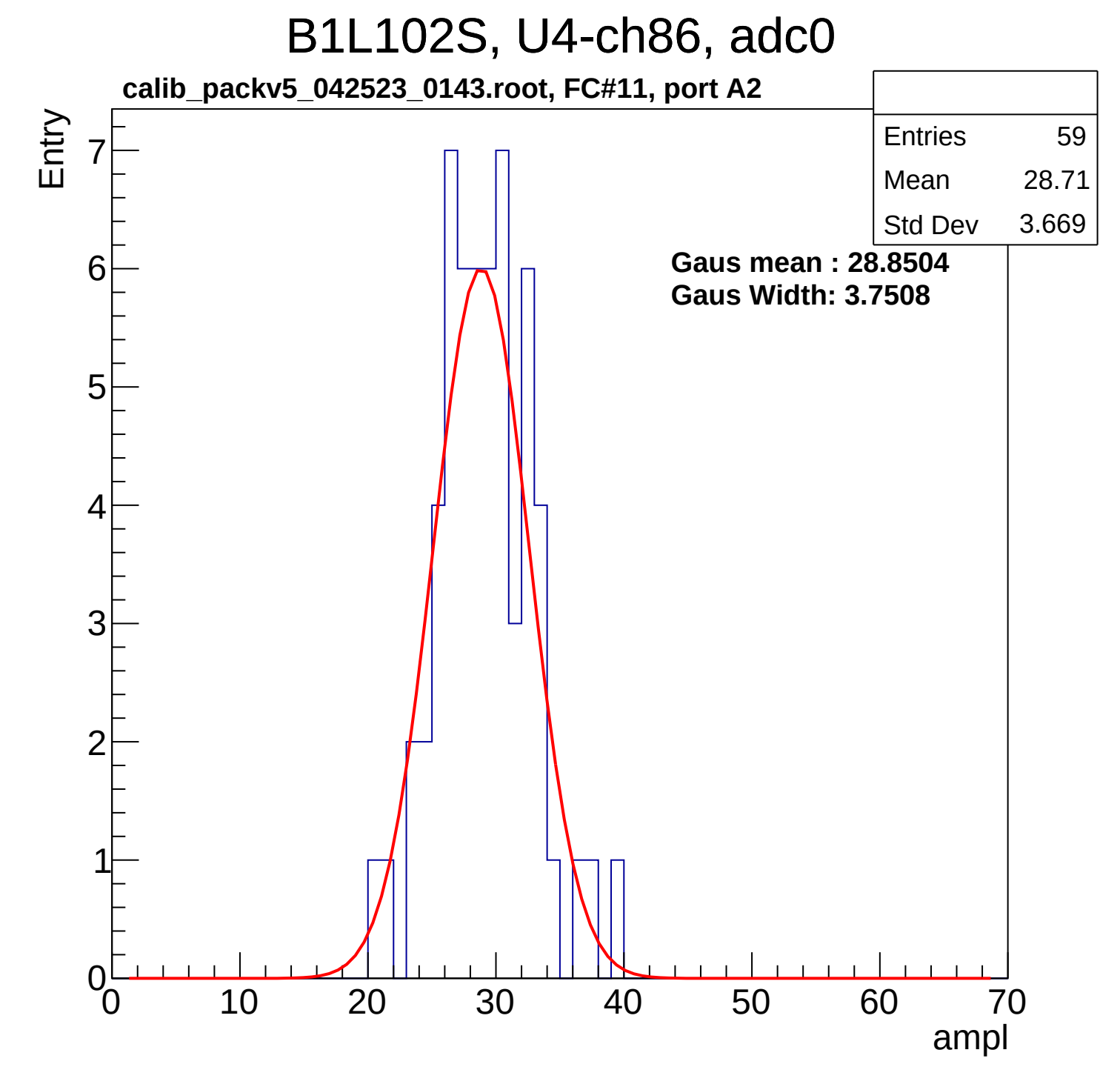
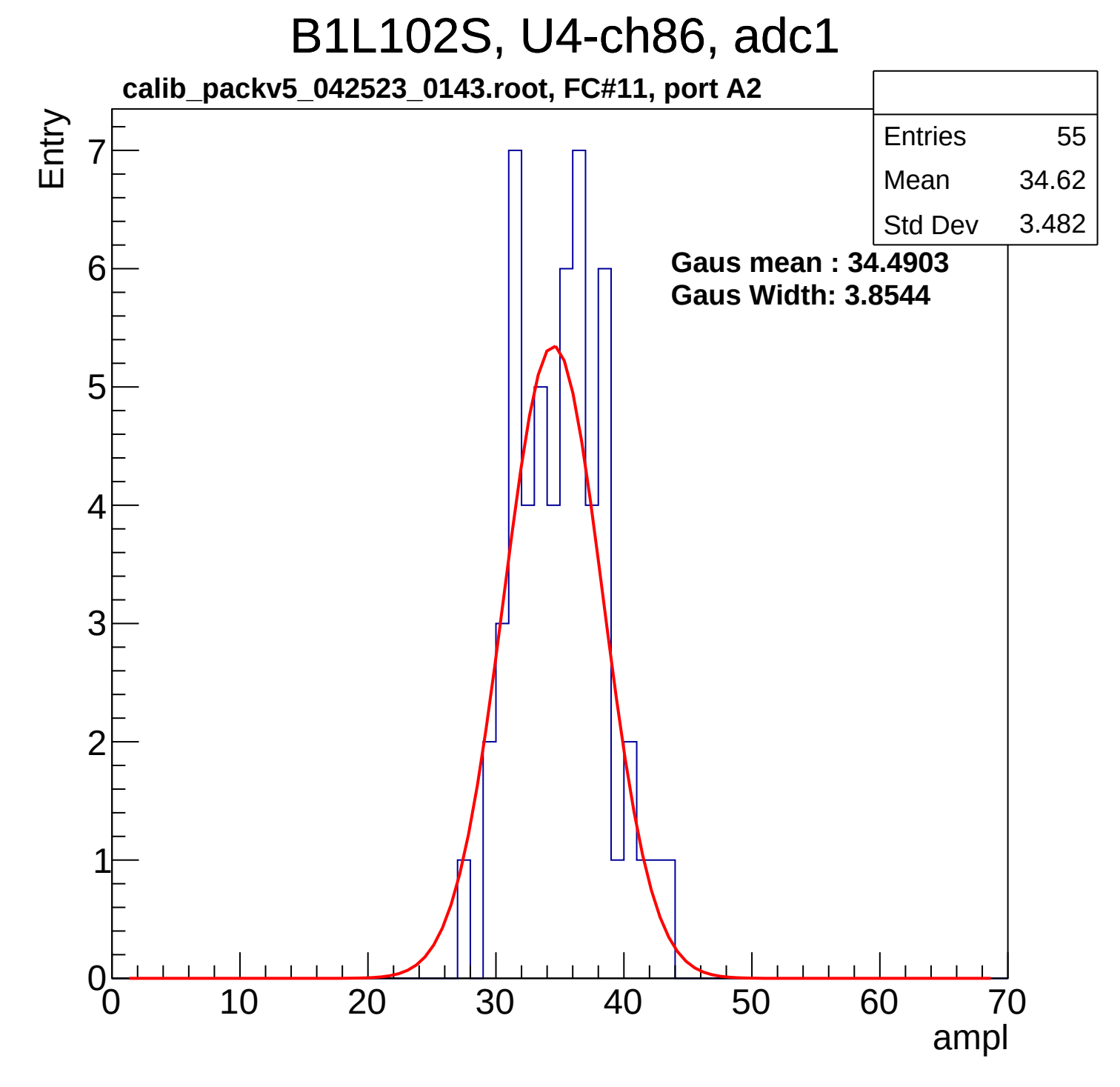
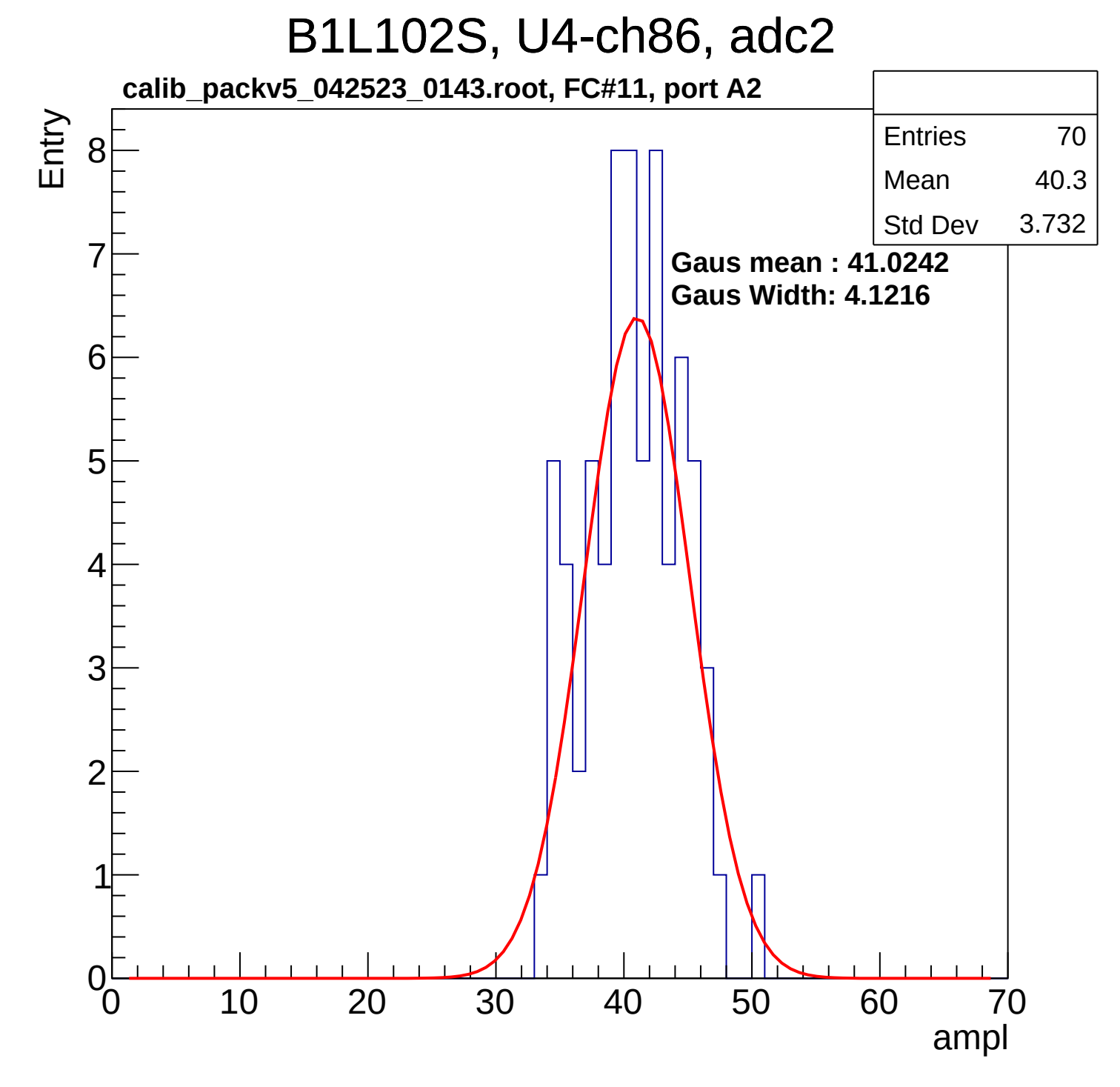

B1L102S, U4-ch85, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 43
Mean 58.88
Std Dev 2.903
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

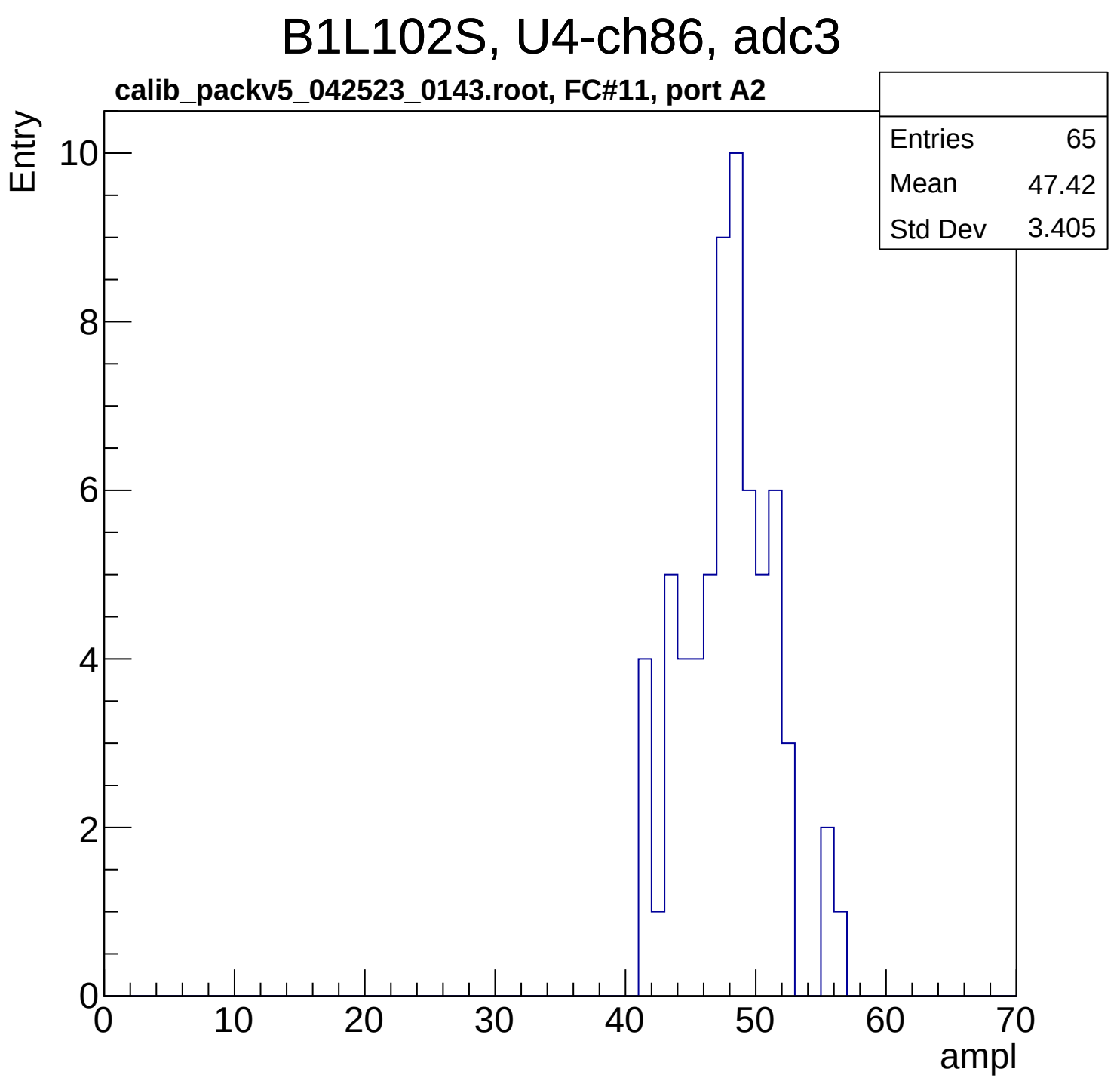

B1L102S, U4-ch85, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 16
Mean 57.88
Std Dev 15
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

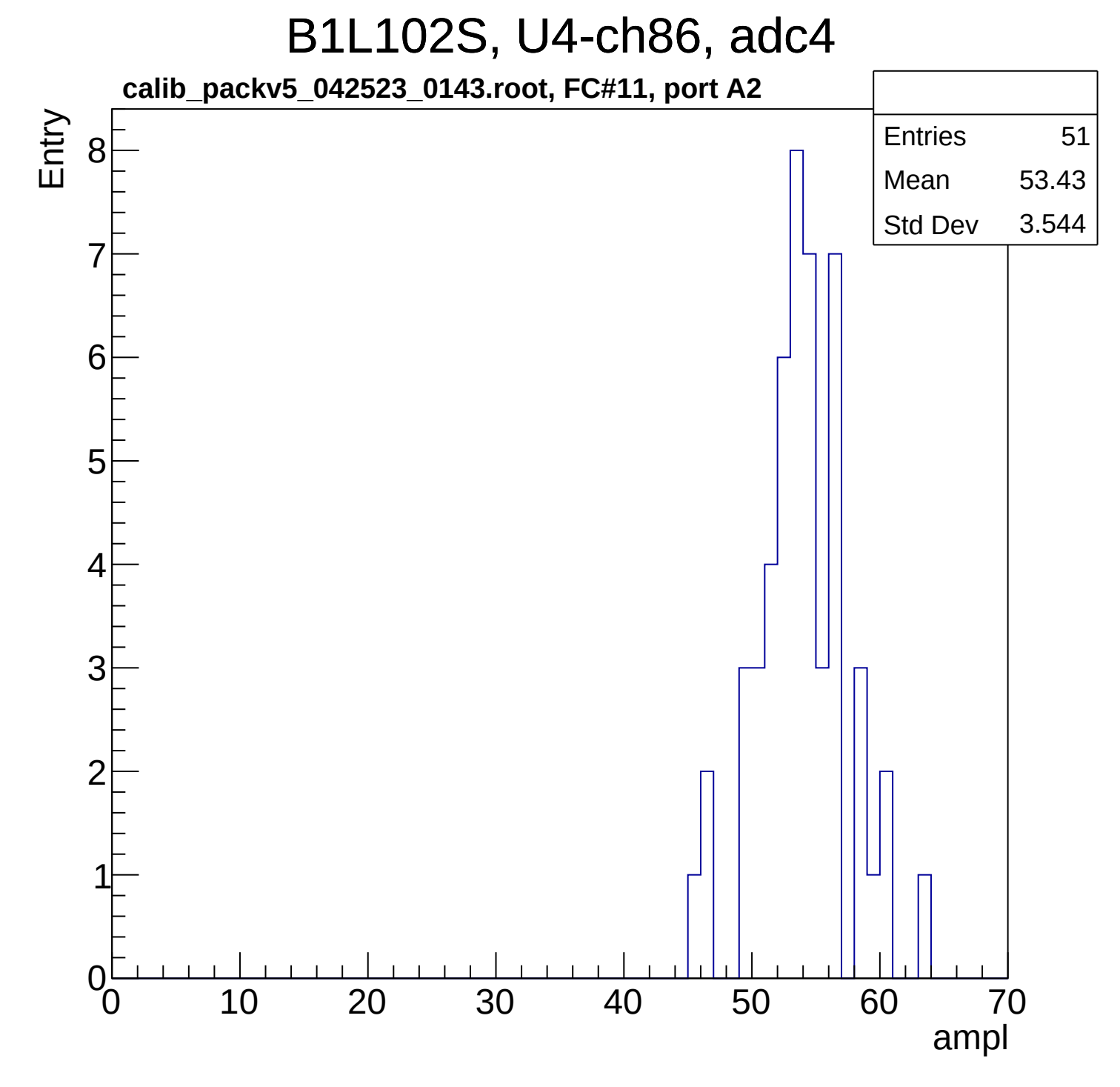

B1L102S, U4-ch85, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch86, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 28.71
Std Dev 3.669
Gaus mean : 28.8504
Gaus Width: 3.7508
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch86, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 34.62
Std Dev 3.482
Gaus mean : 34.4903
Gaus Width: 3.8544
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch86, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 40.3
Std Dev 3.732
Gaus mean : 41.0242
Gaus Width: 4.1216
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch86, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 47.42
Std Dev 3.405
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch86, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 53.43
Std Dev 3.544
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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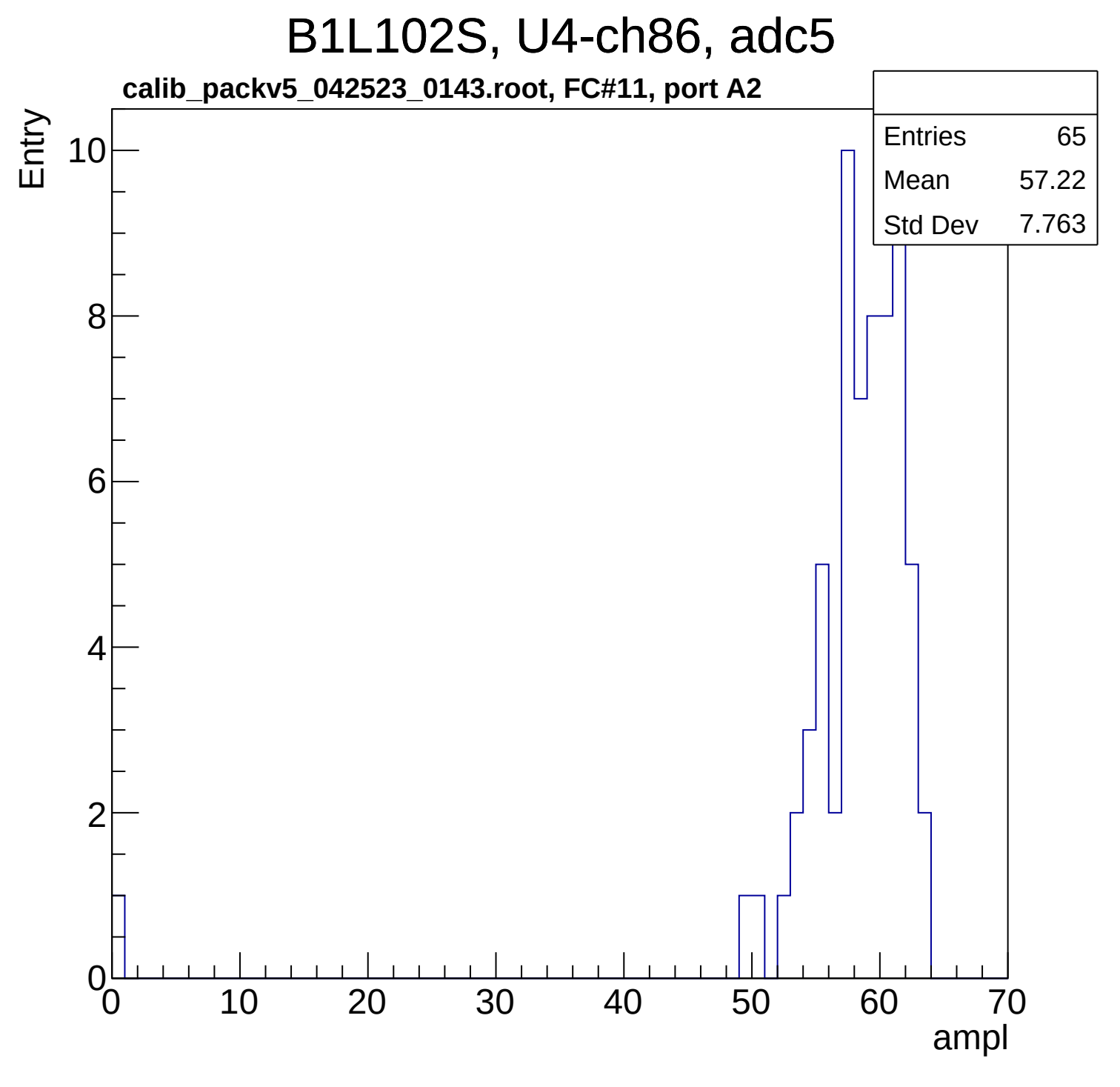
40
50
60
70


B1L102S, U4-ch86, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 57.22
Std Dev 7.763
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
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60
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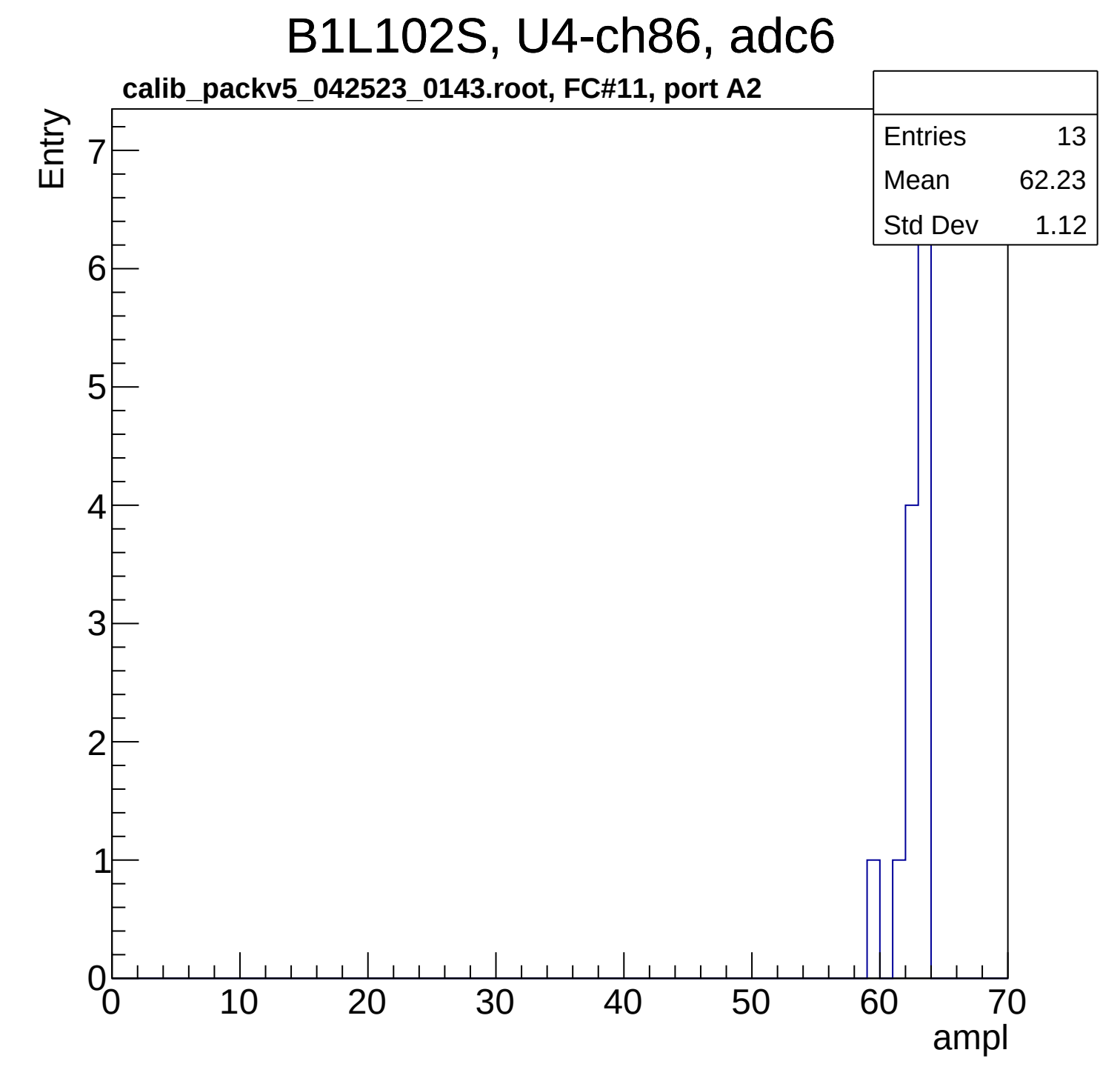
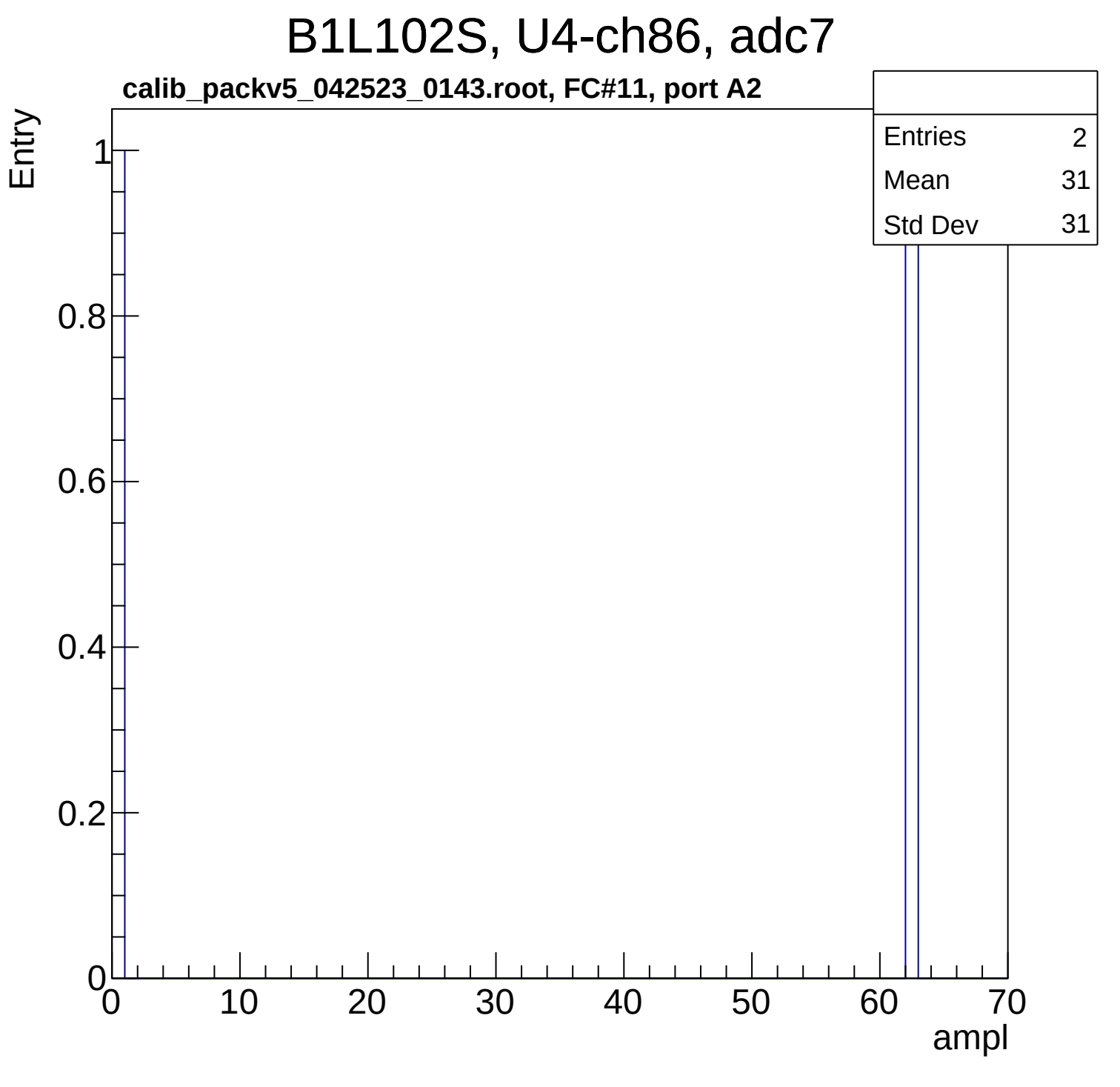
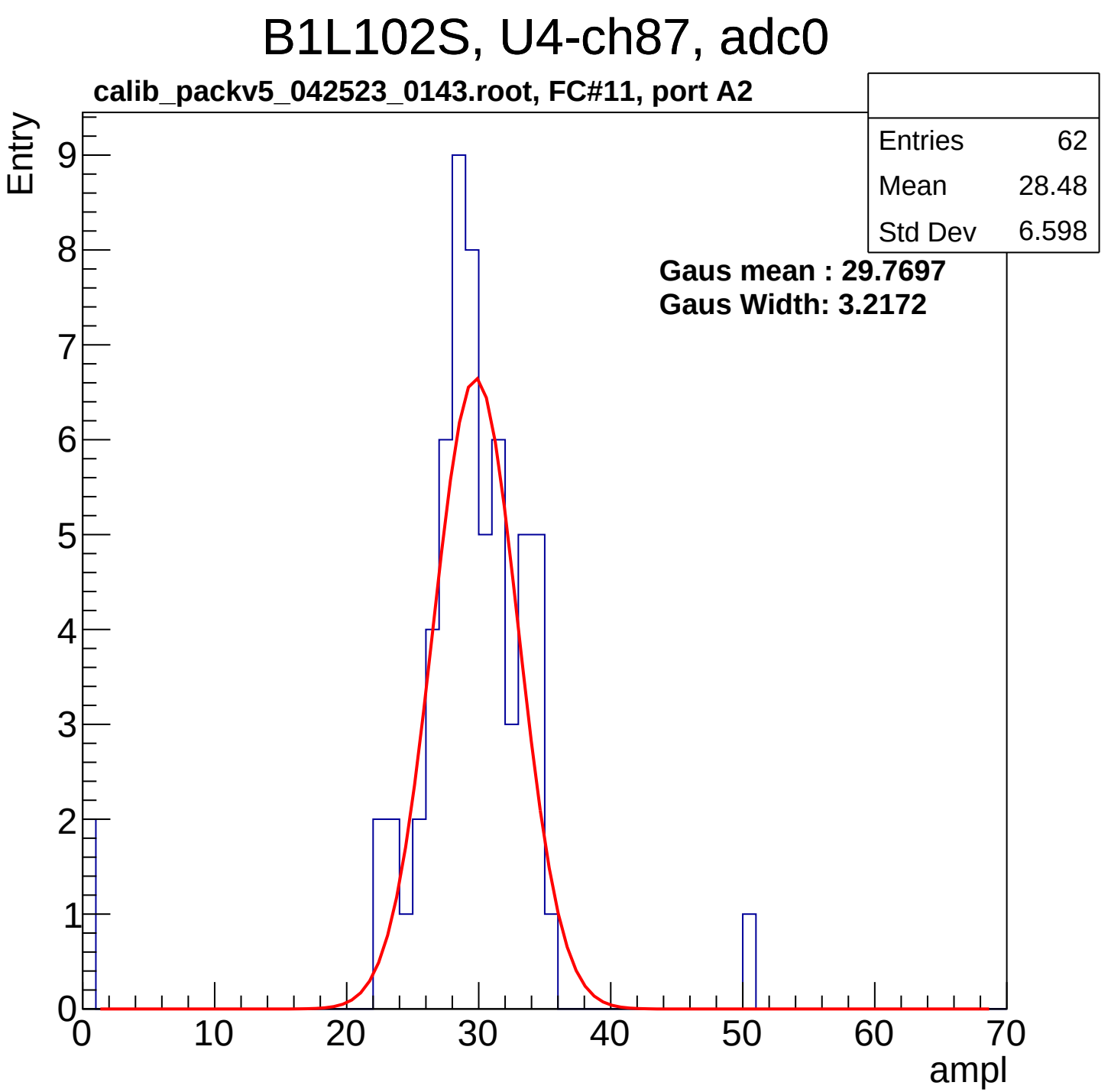
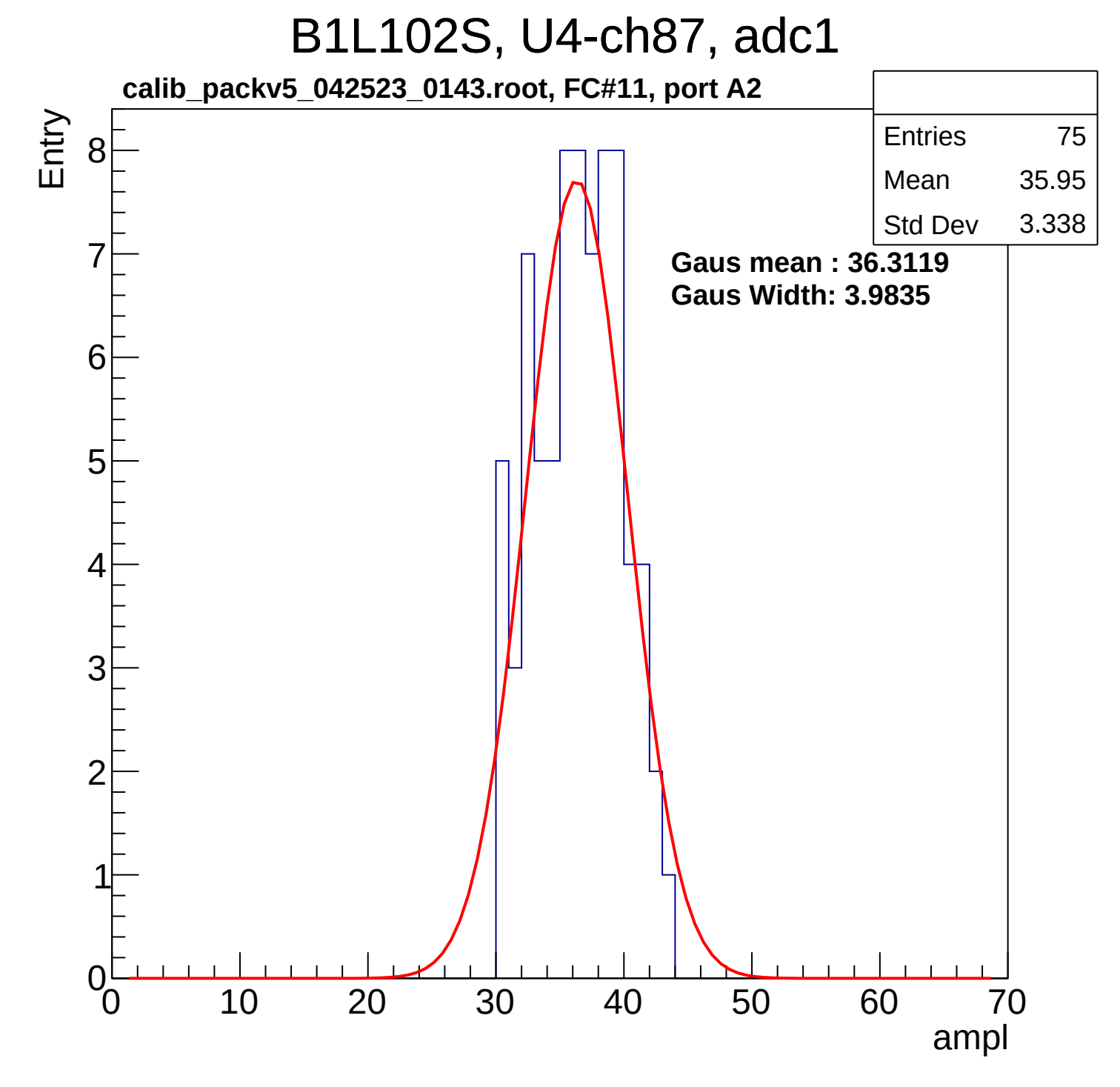
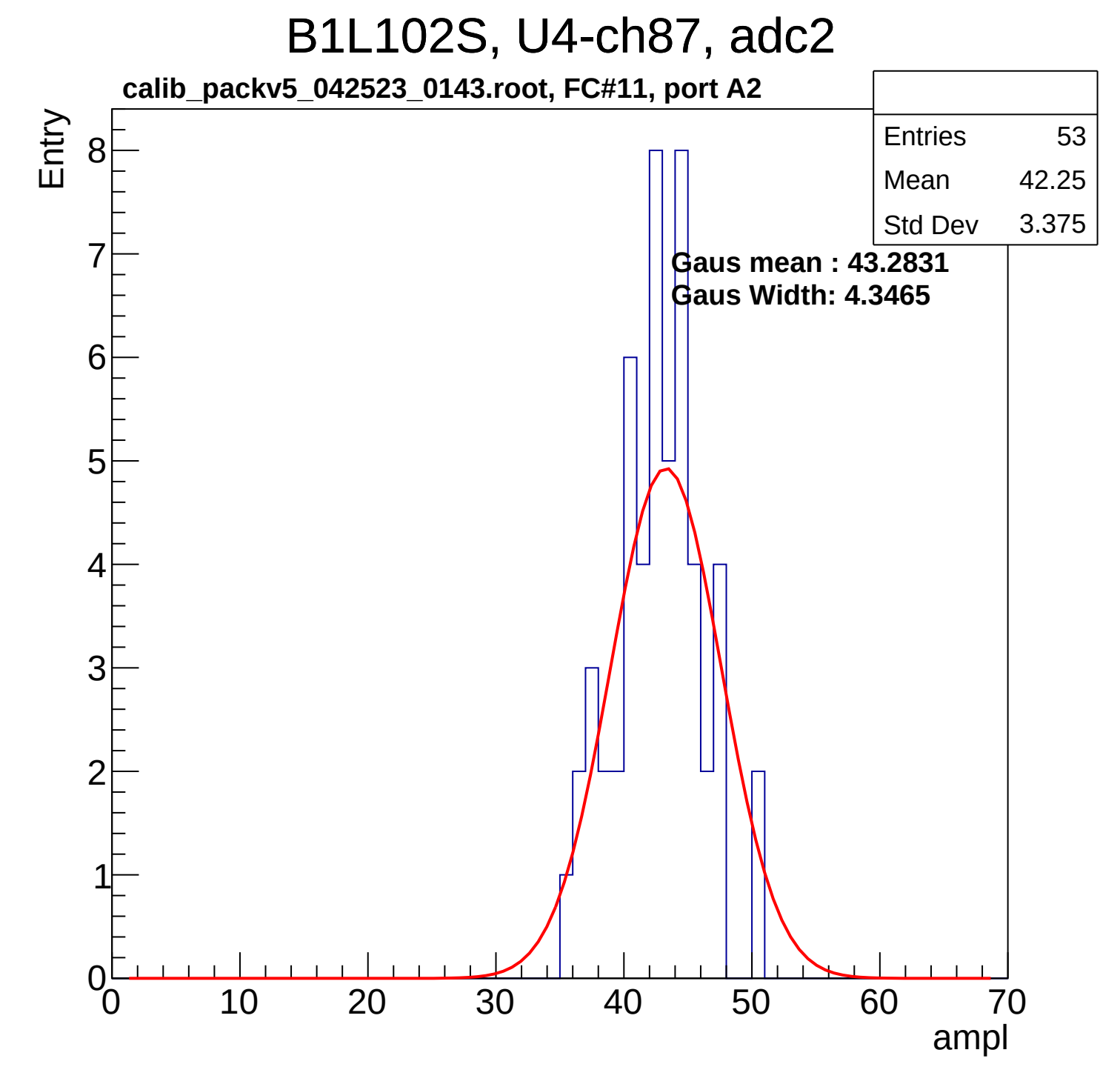
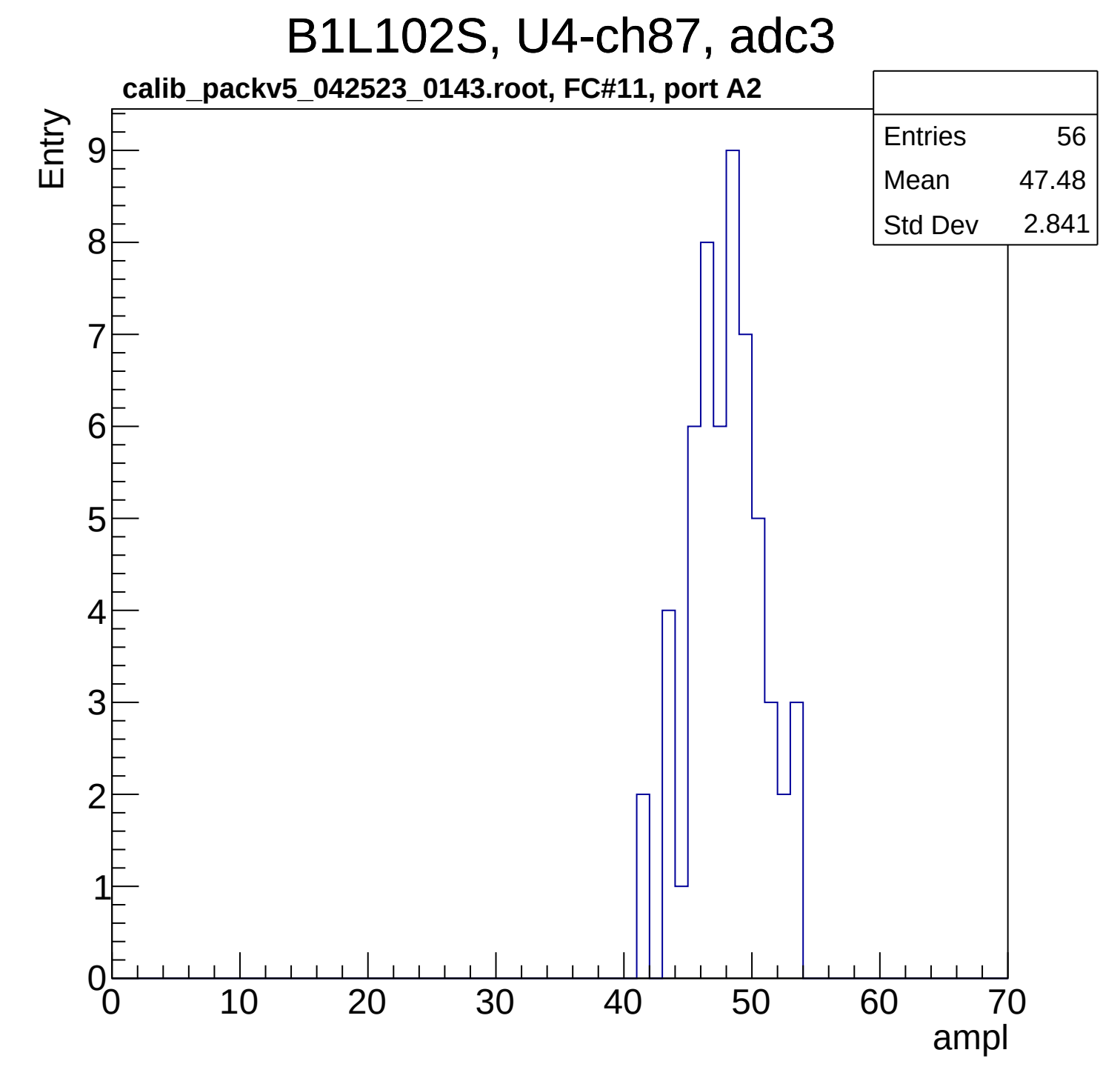

B1L102S, U4-ch86, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 13
Mean 62.23
Std Dev 1.12
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch86, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 31
Std Dev 31
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch87, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 28.48
Std Dev 6.598
Gaus mean : 29.7697
Gaus Width: 3.2172
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch87, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 35.95
Std Dev 3.338
Gaus mean : 36.3119
Gaus Width: 3.9835
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch87, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 42.25
Std Dev 3.375
Gaus mean : 43.2831
Gaus Width: 4.3465
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch87, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 47.48
Std Dev 2.841
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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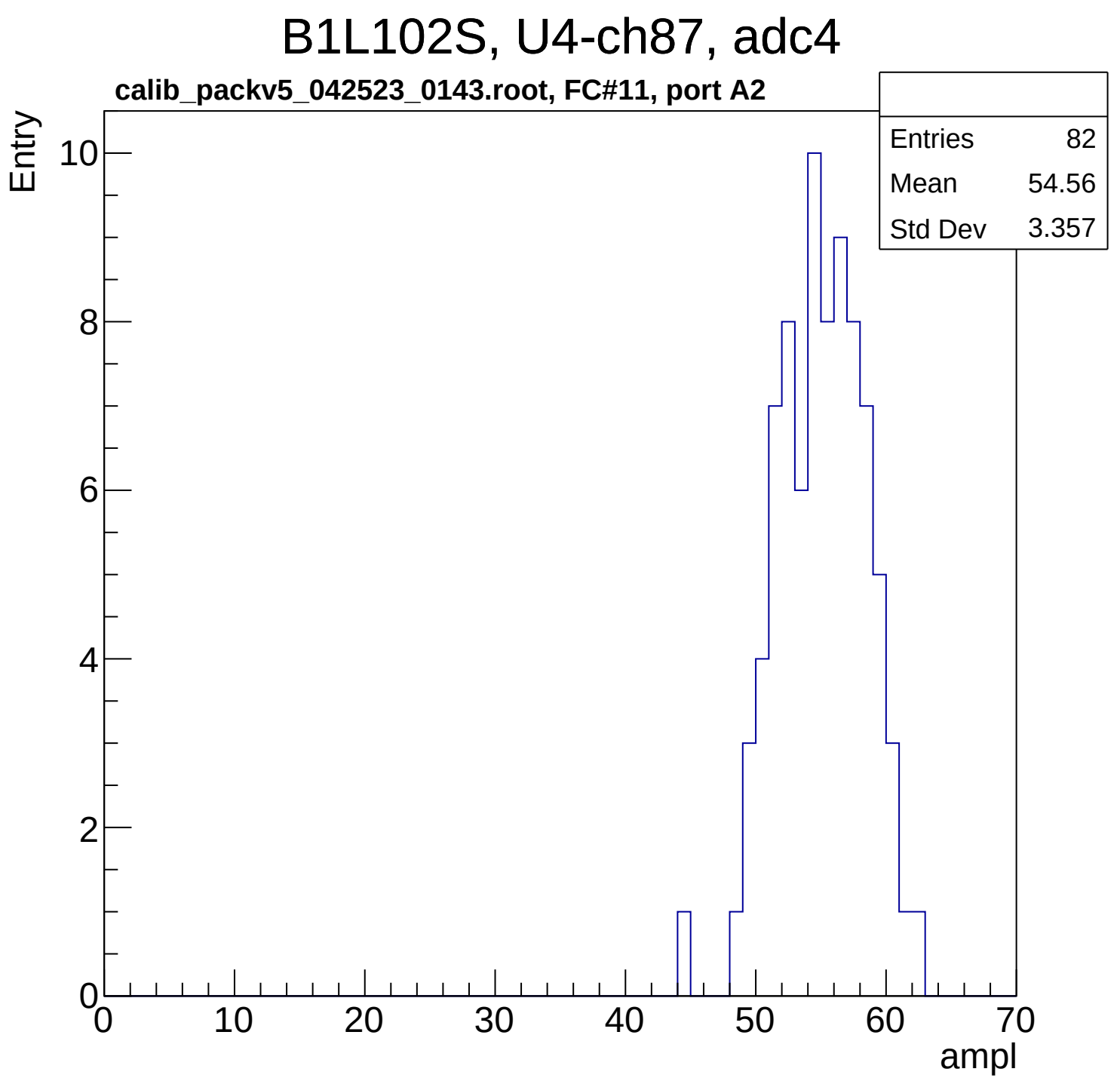
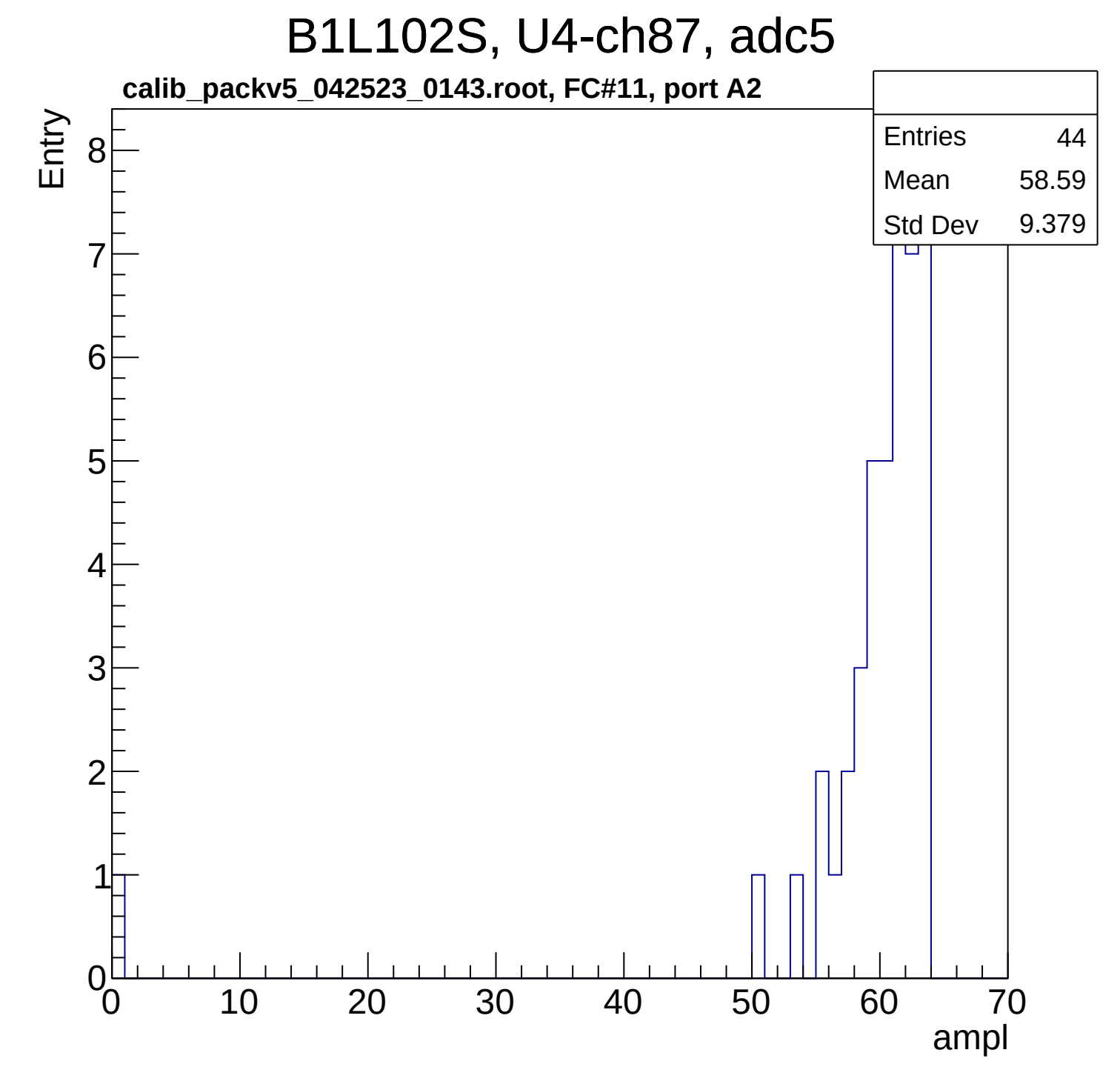

B1L102S, U4-ch87, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 82
Mean 54.56
Std Dev 3.357
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch87, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 44
Mean 58.59
Std Dev 9.379
Entry
ampl
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2
3
4
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7
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0
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20
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40
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60
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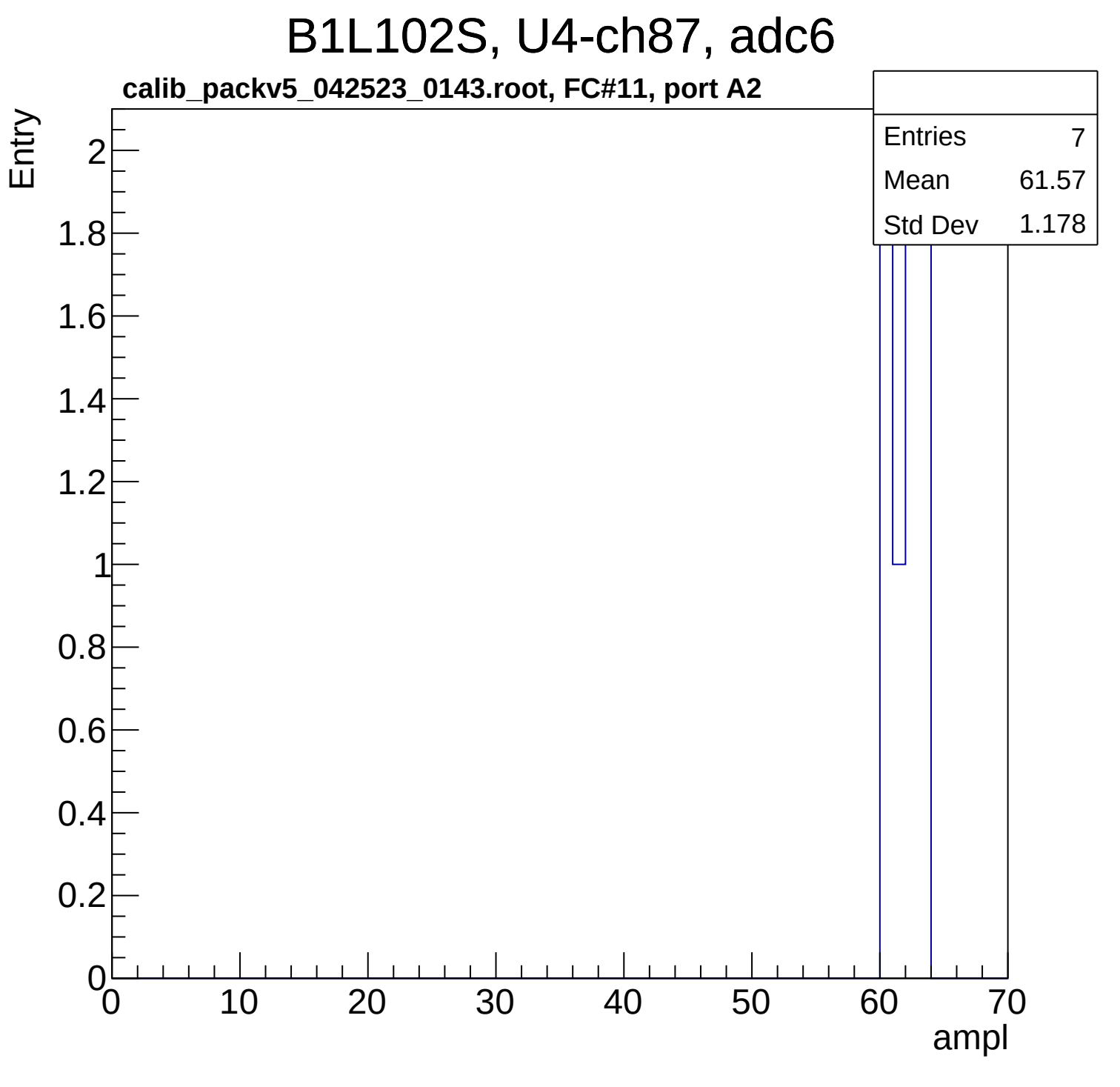
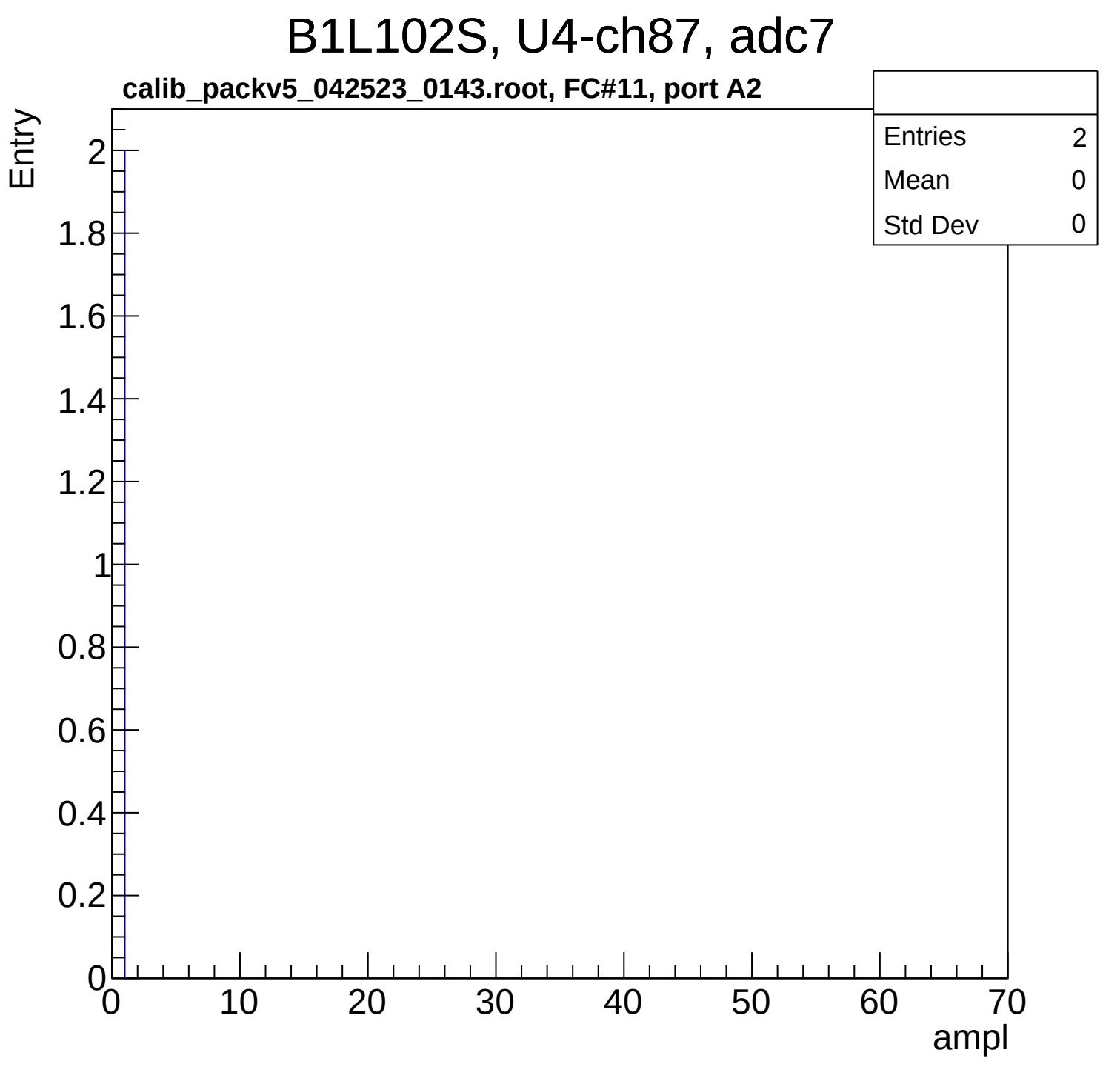

B1L102S, U4-ch87, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 7
Mean 61.57
Std Dev 1.178
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L102S, U4-ch87, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
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60
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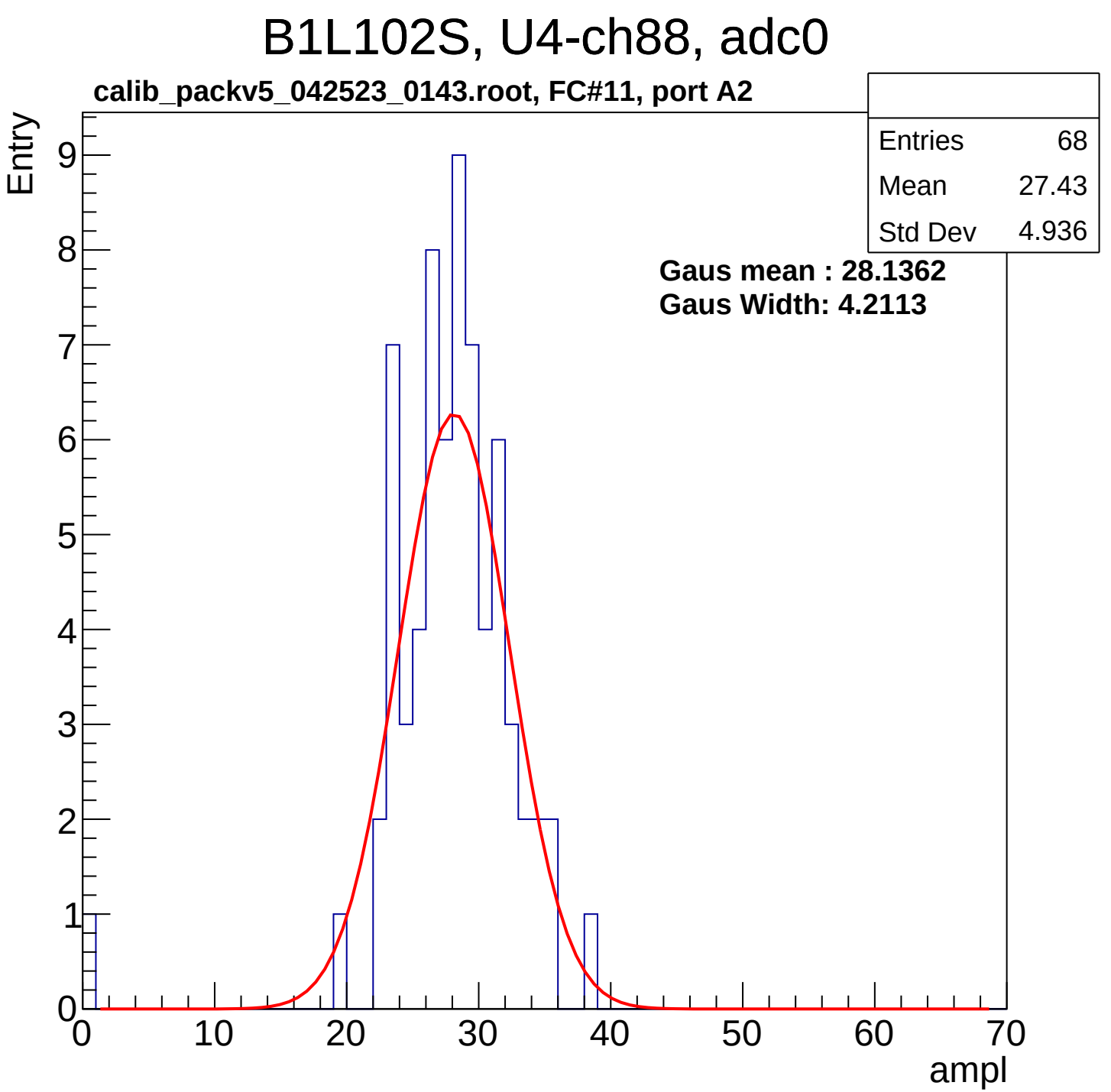
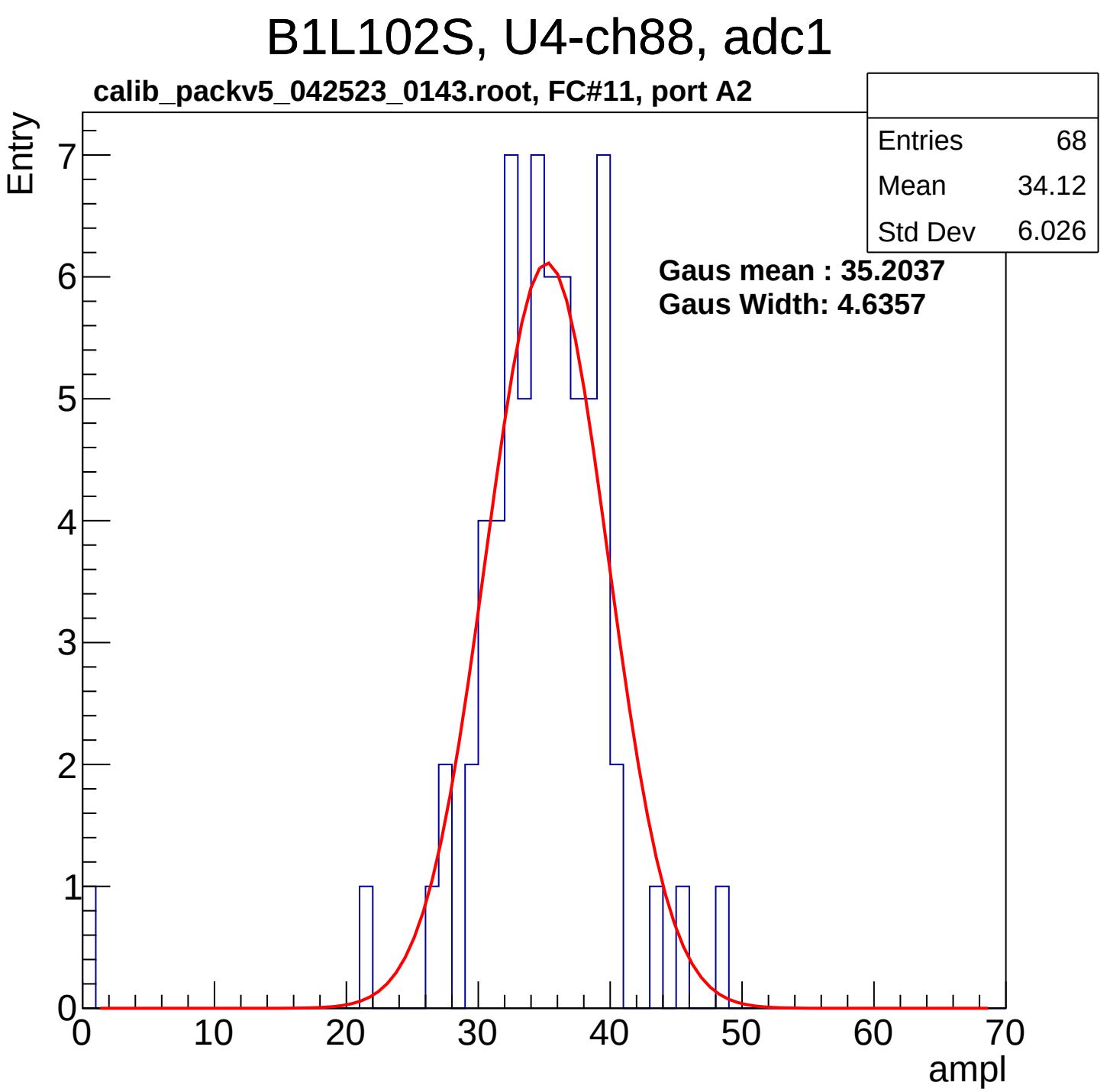

B1L102S, U4-ch88, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 27.43
Std Dev 4.936
Gaus mean : 28.1362
Gaus Width: 4.2113
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch88, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 34.12
Std Dev 6.026
Gaus mean : 35.2037
Gaus Width: 4.6357
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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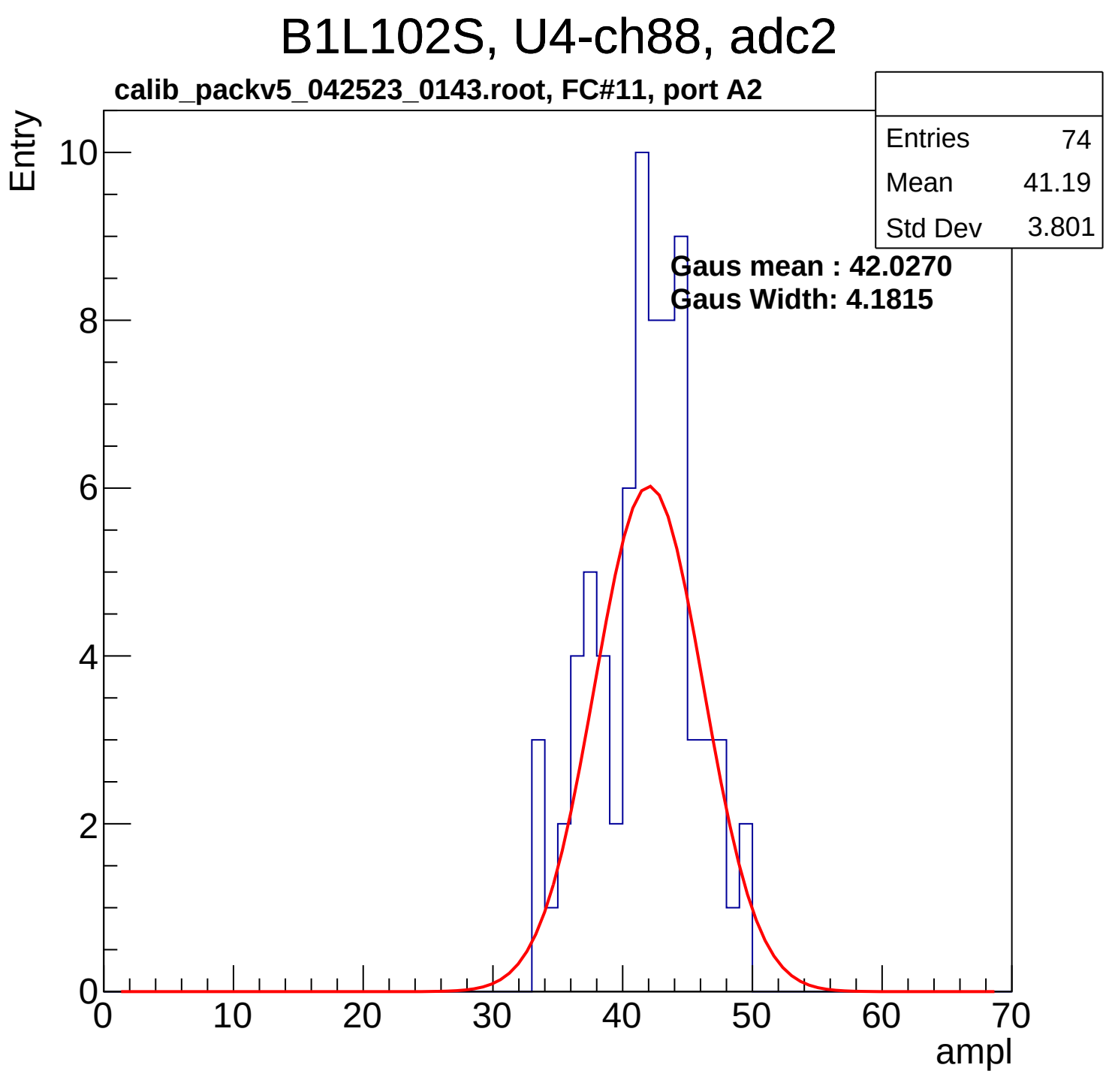
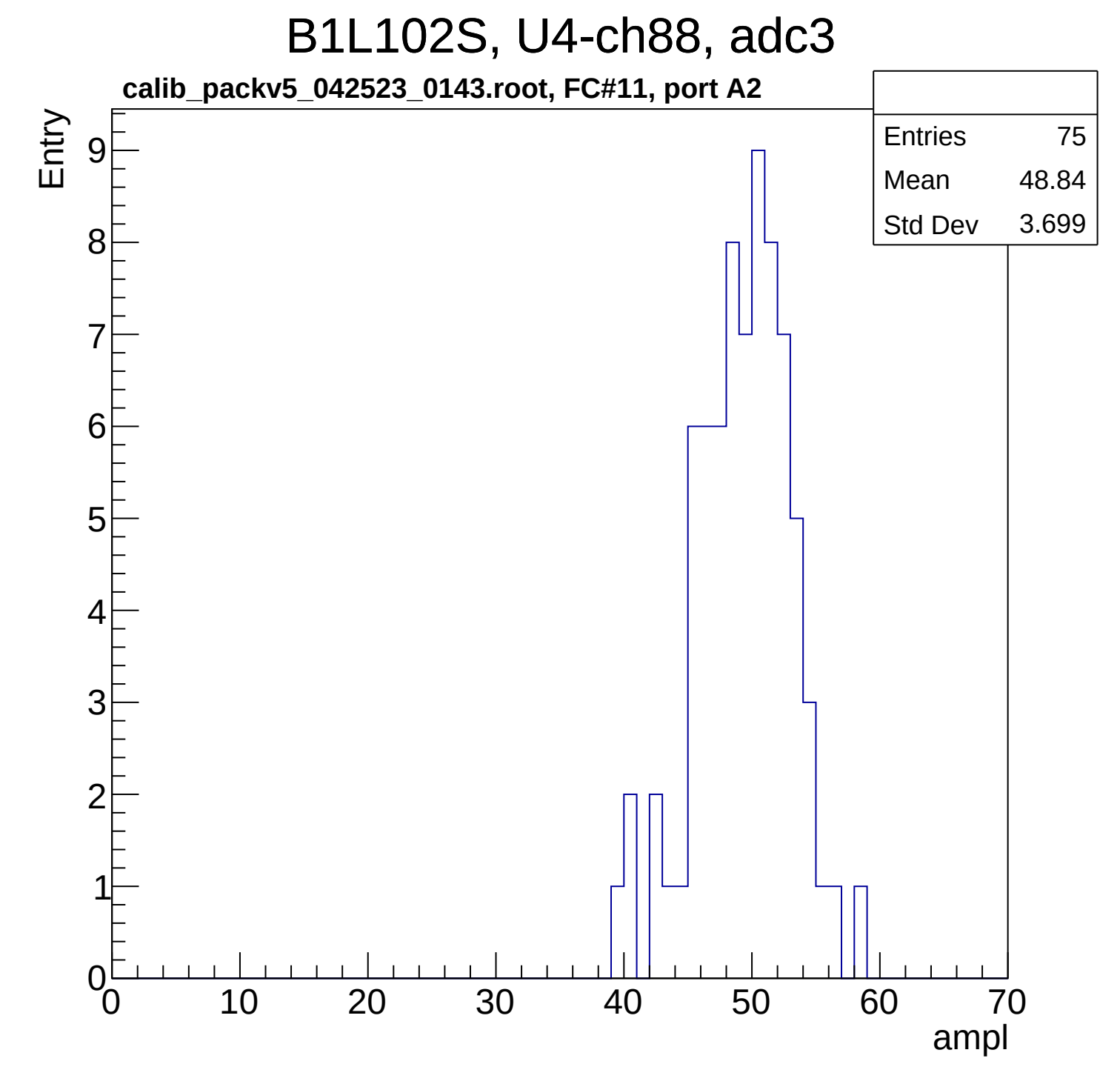

B1L102S, U4-ch88, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 41.19
Std Dev 3.801
Gaus mean : 42.0270
Gaus Width: 4.1815
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch88, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 48.84
Std Dev 3.699
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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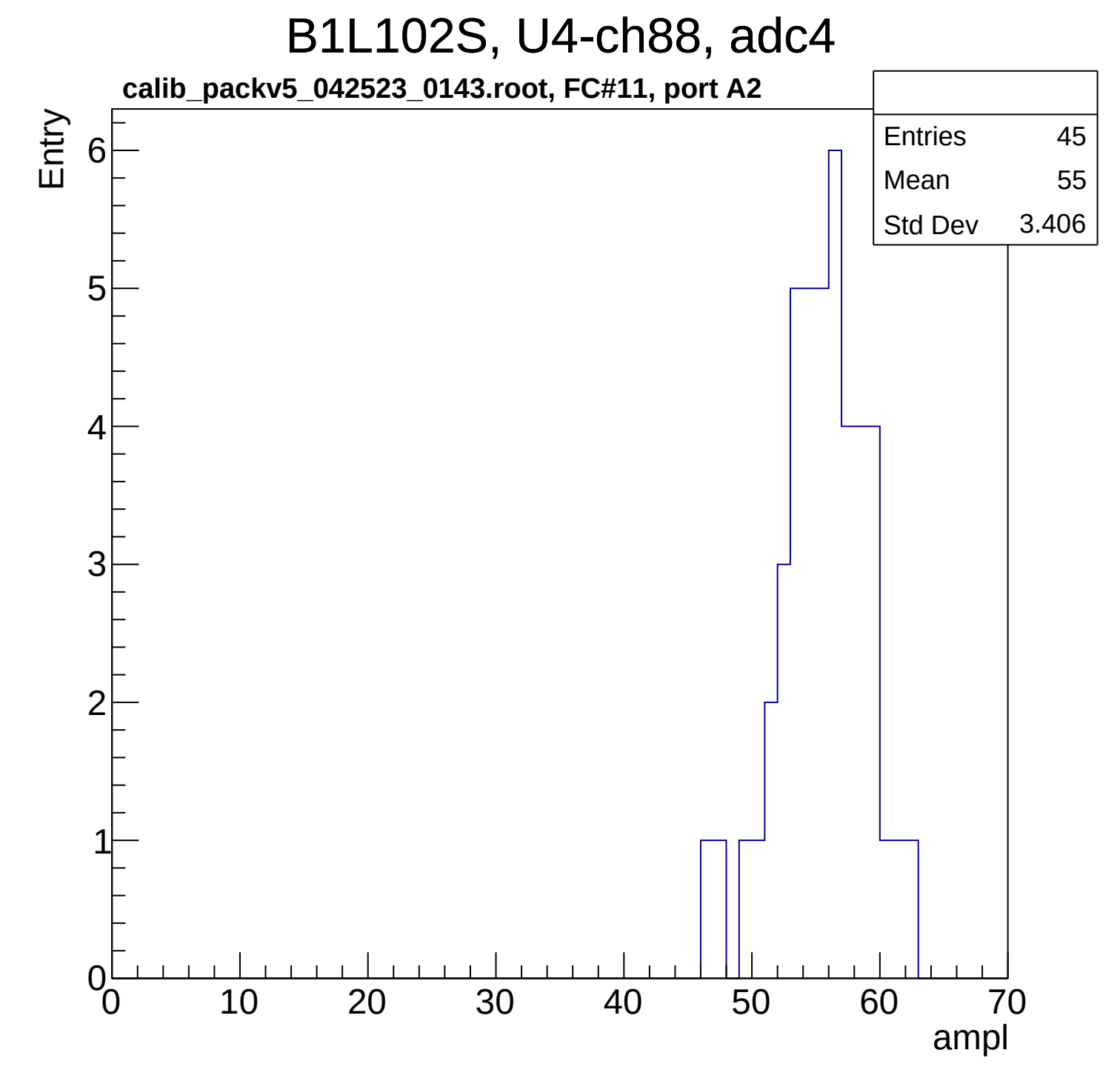
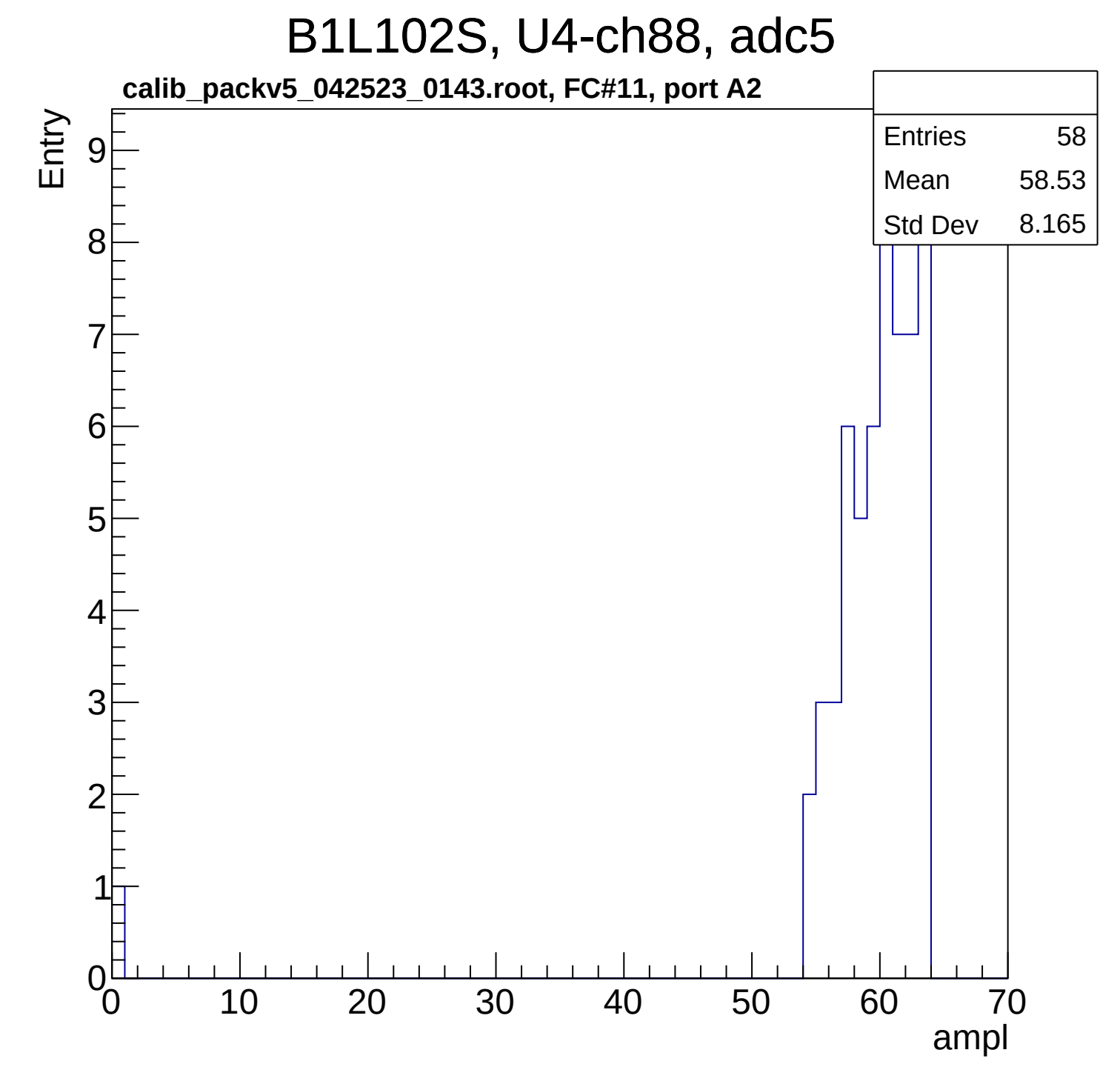

B1L102S, U4-ch88, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 45
Mean 55
Std Dev 3.406
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L102S, U4-ch88, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 58.53
Std Dev 8.165
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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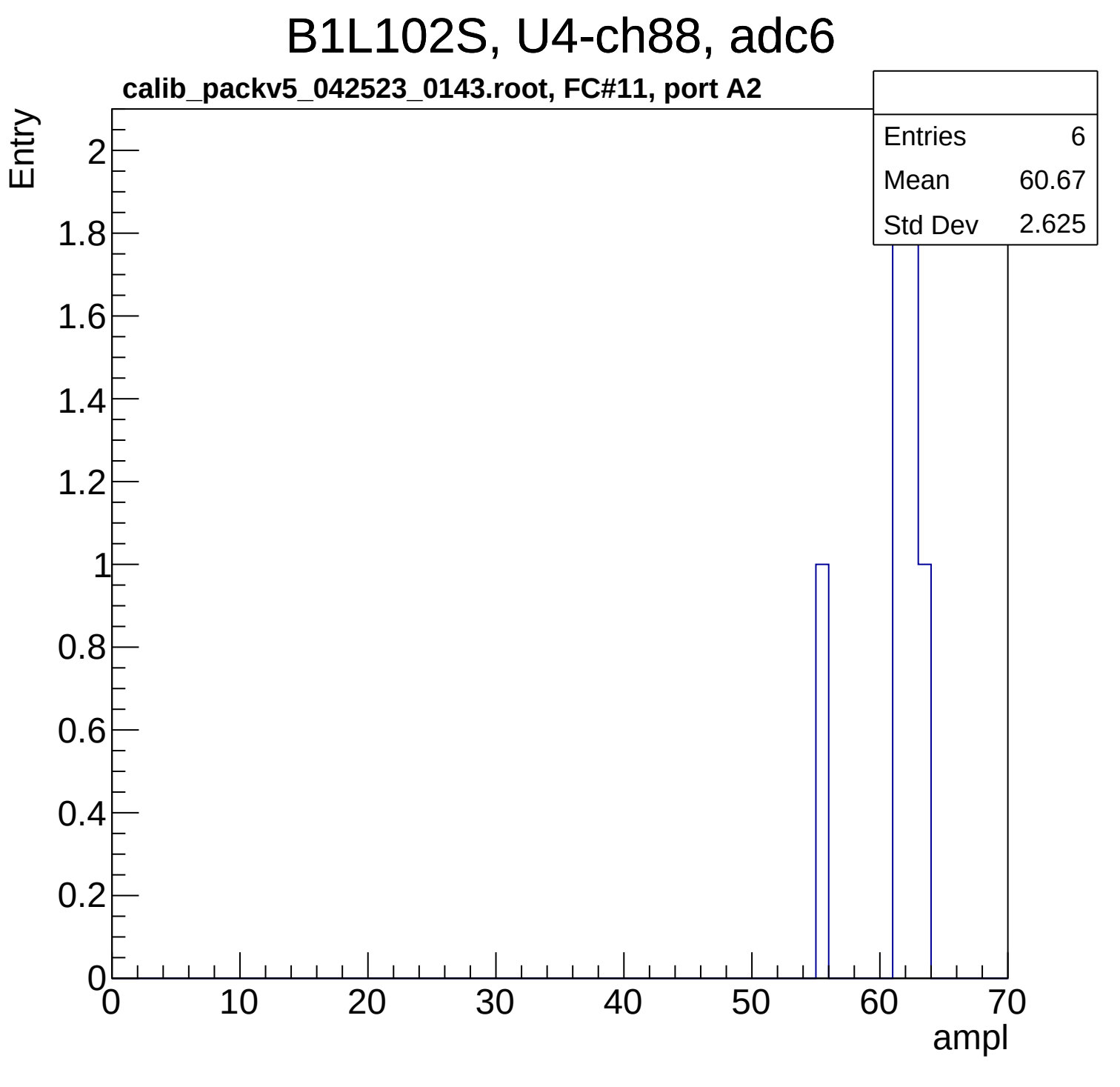
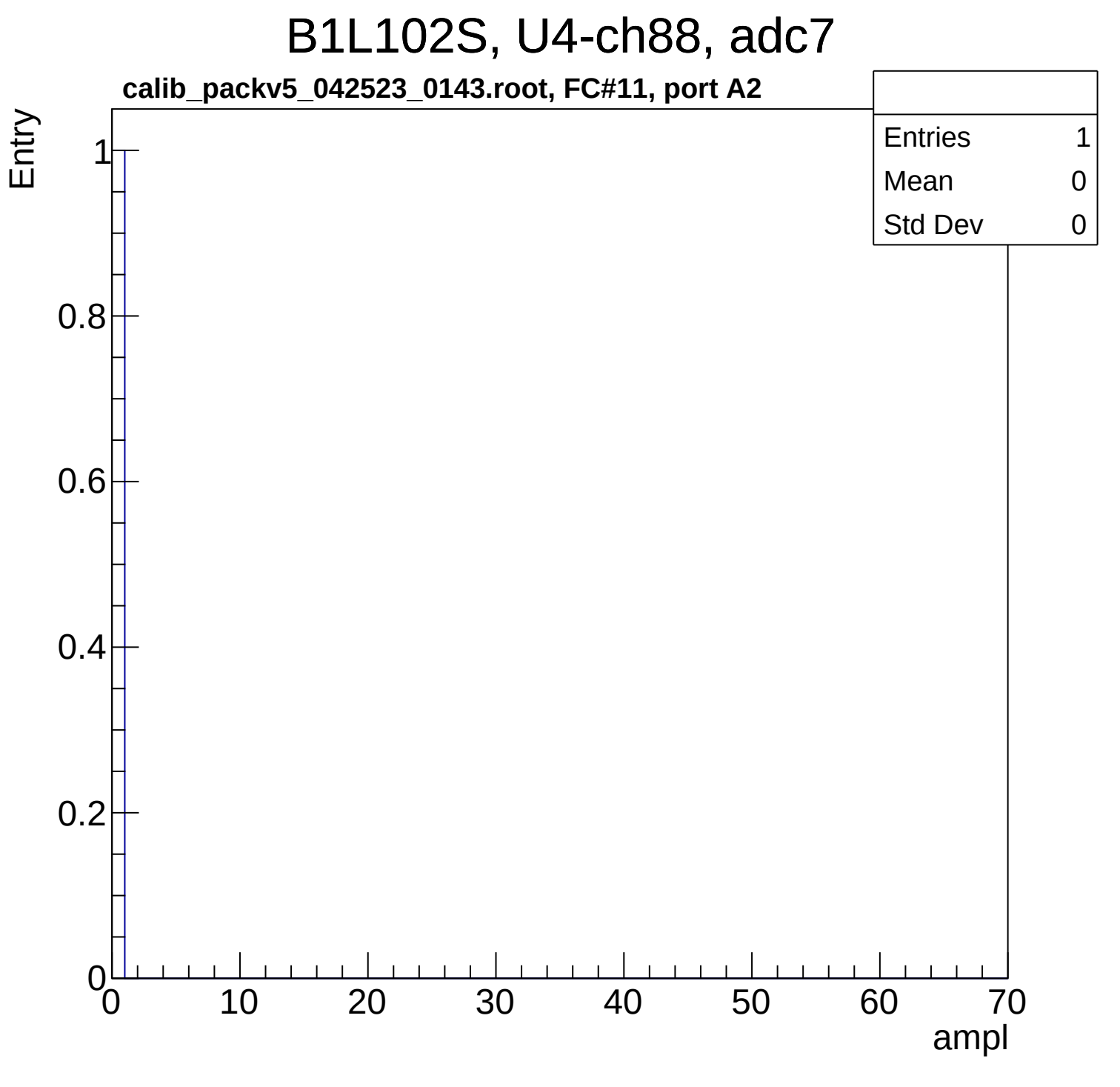
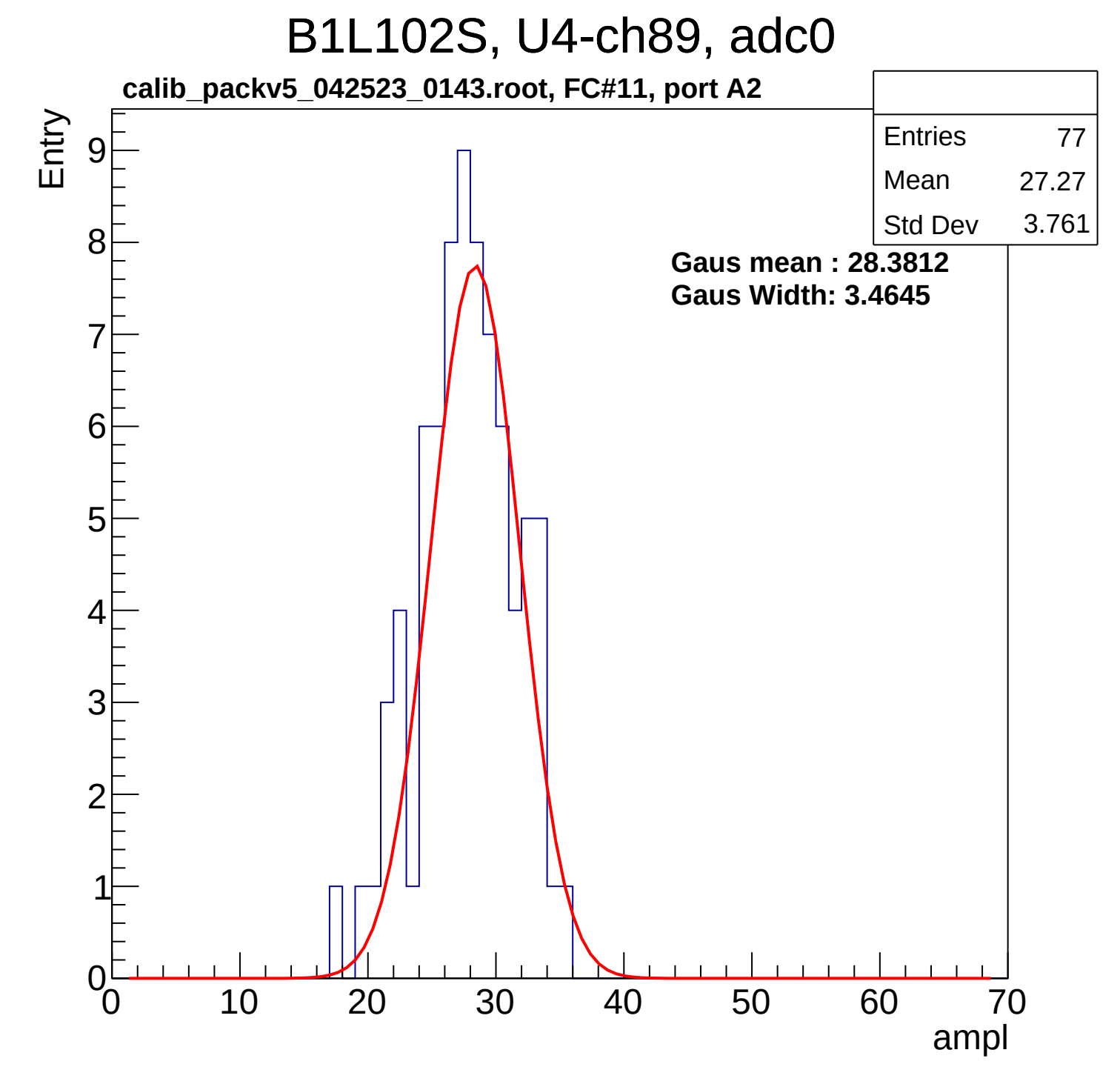
40
50
60
70


B1L102S, U4-ch88, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 6
Mean 60.67
Std Dev 2.625
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L102S, U4-ch88, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch89, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 77
Mean 27.27
Std Dev 3.761
Gaus mean : 28.3812
Gaus Width: 3.4645
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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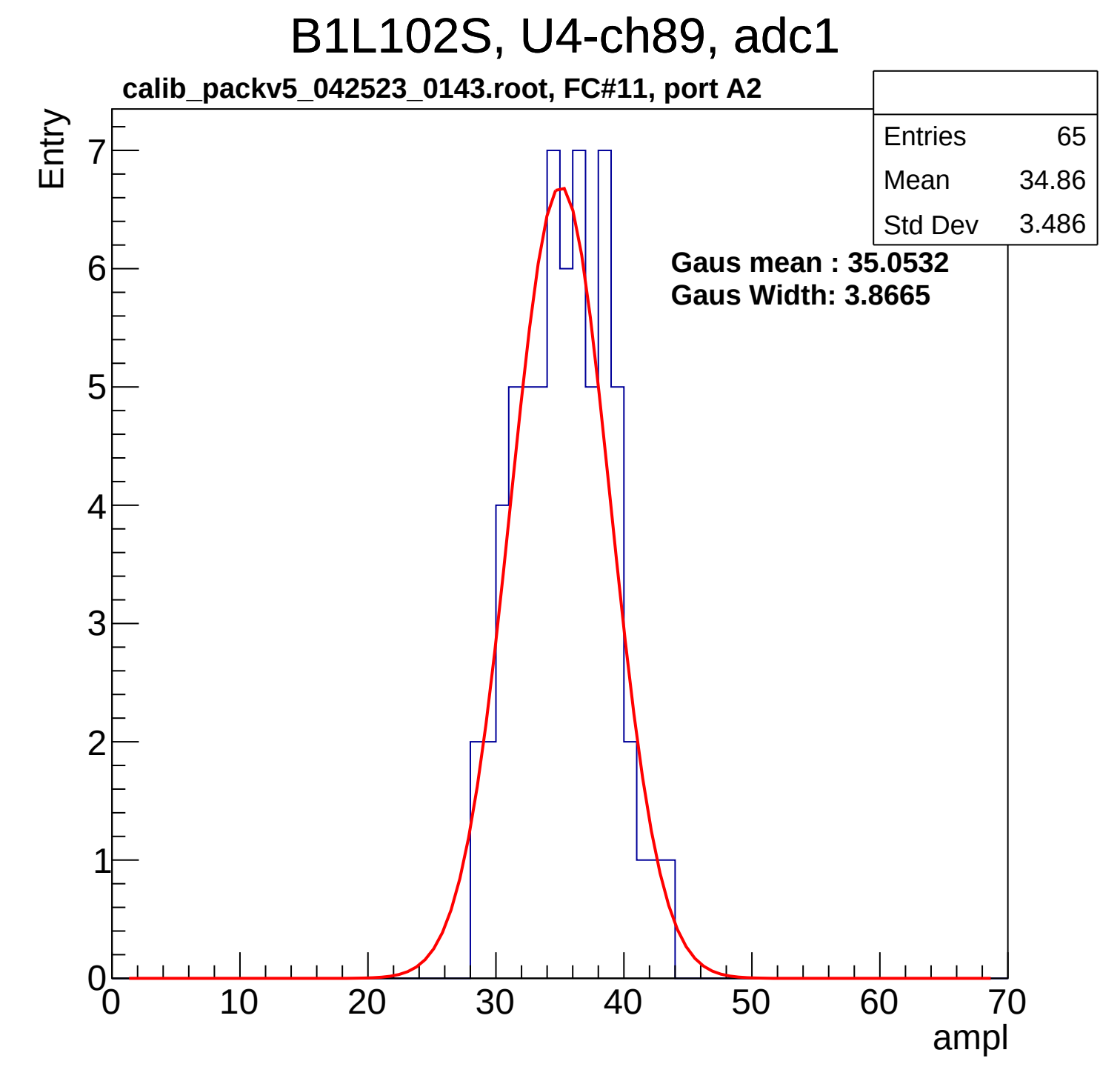
B1L102S, U4-ch89, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 34.86
Std Dev 3.486
Gaus mean : 35.0532
Gaus Width: 3.8665
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
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60
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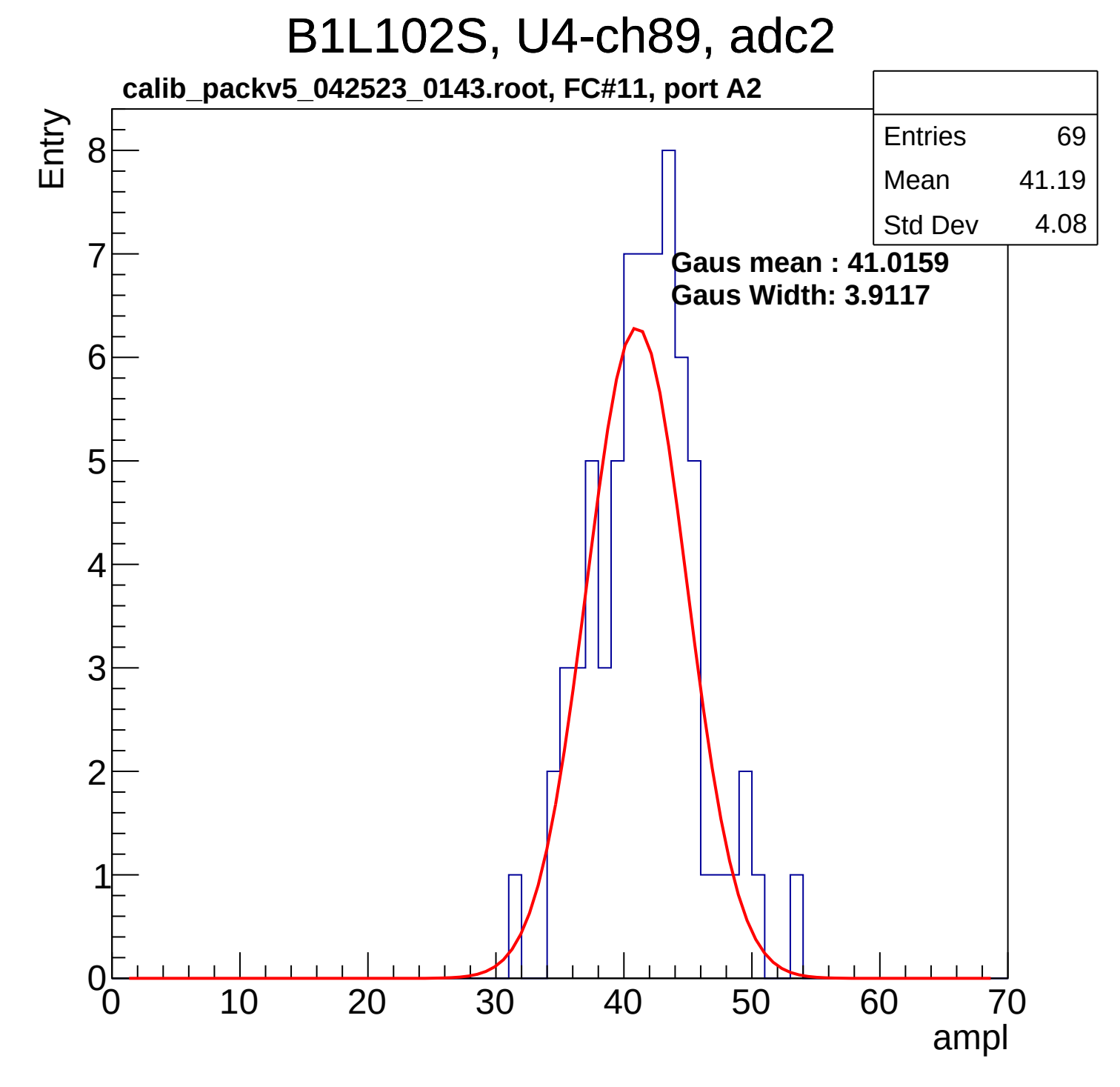
B1L102S, U4-ch89, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 41.19
Std Dev 4.08
Gaus mean : 41.0159
Gaus Width: 3.9117
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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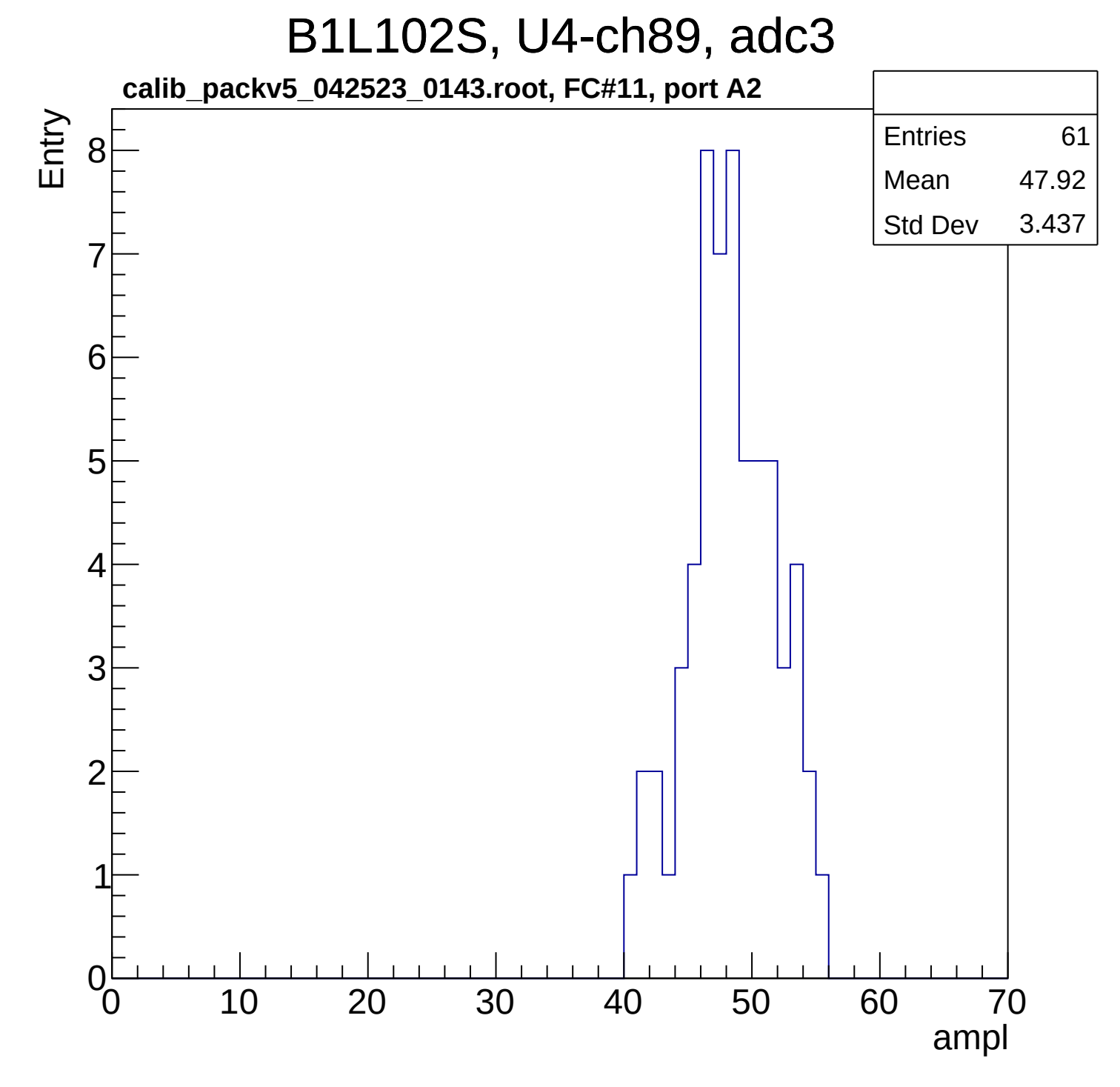
B1L102S, U4-ch89, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 47.92
Std Dev 3.437
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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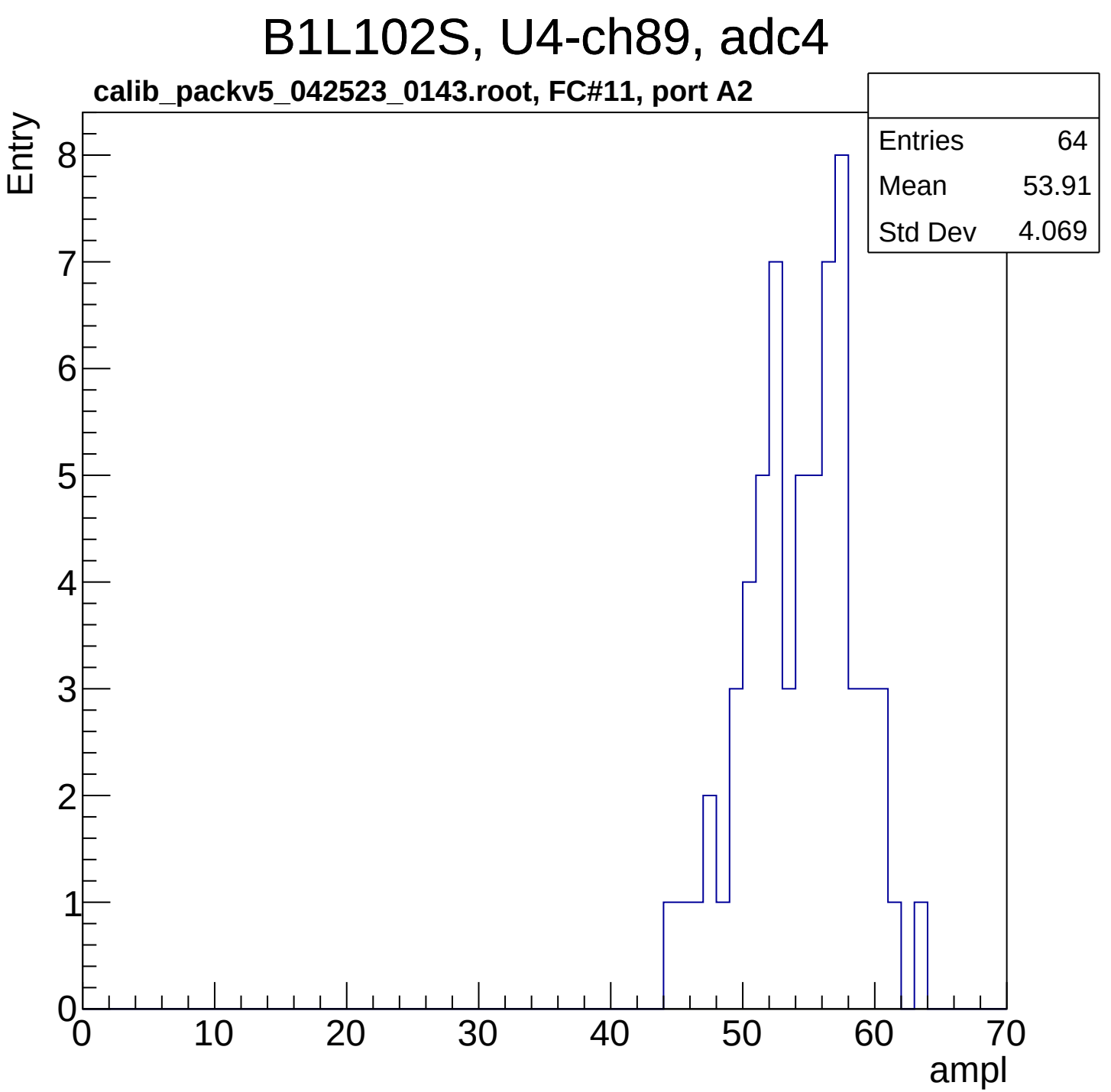
B1L102S, U4-ch89, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 53.91
Std Dev 4.069
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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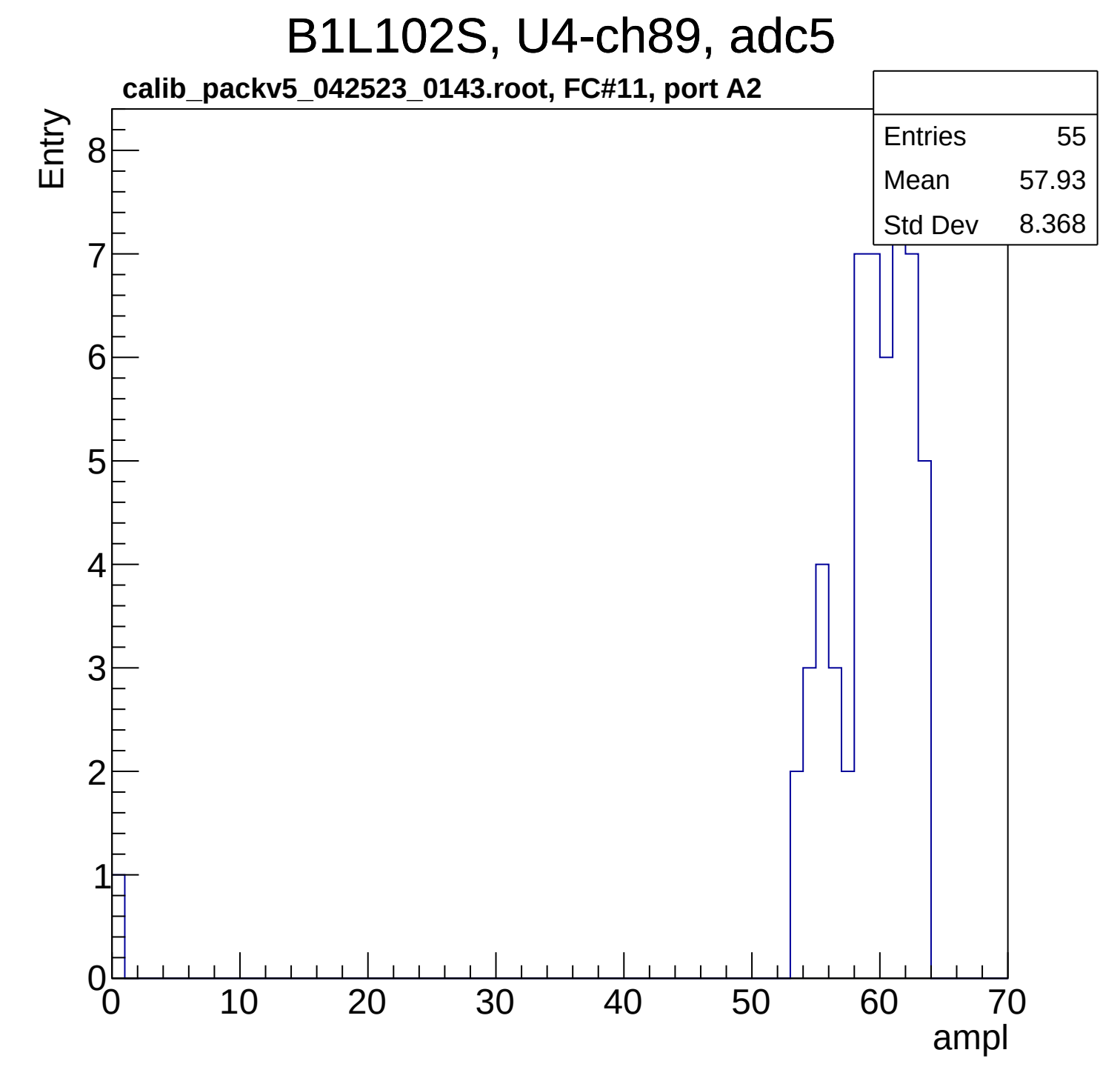
B1L102S, U4-ch89, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 57.93
Std Dev 8.368
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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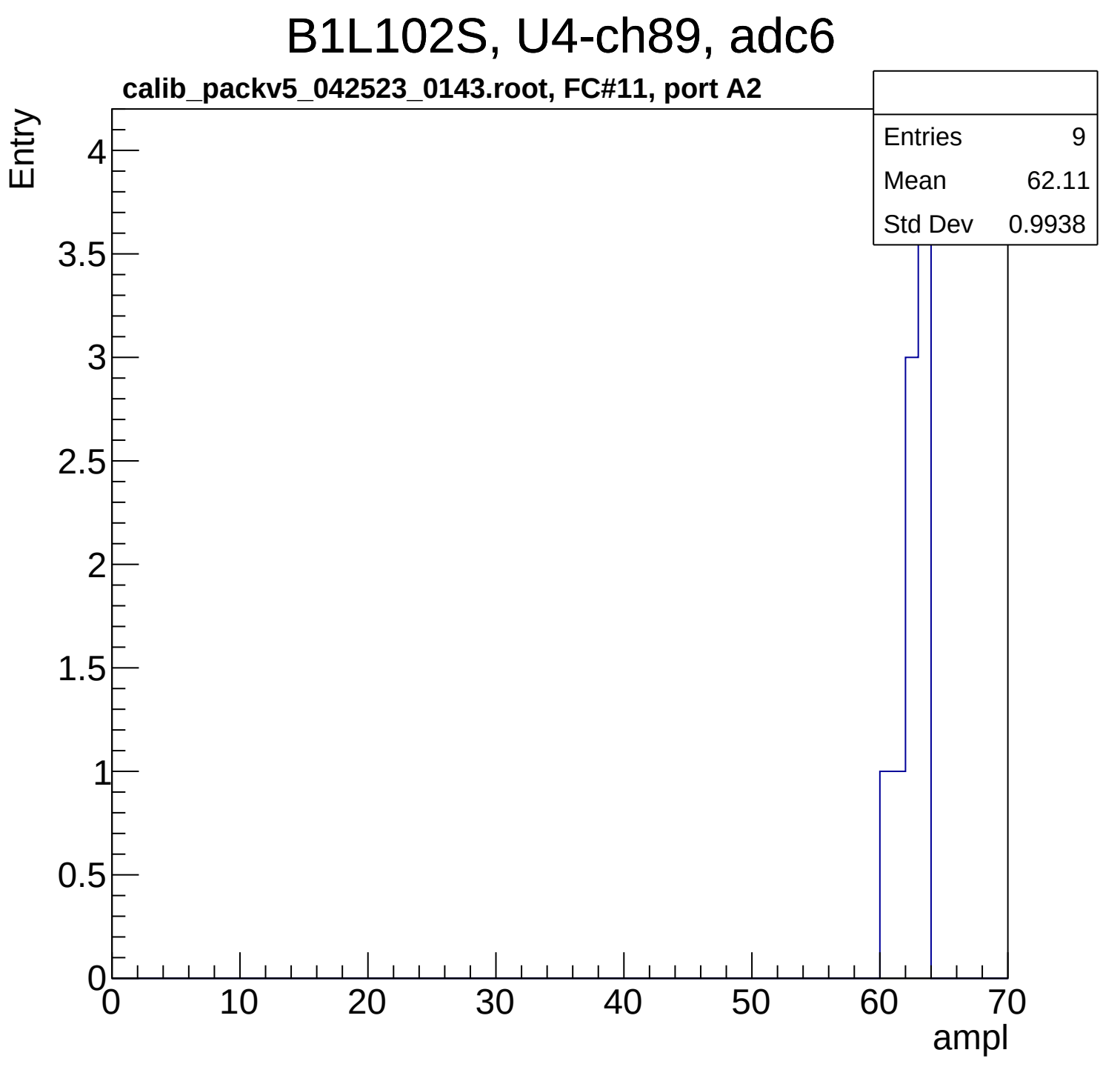
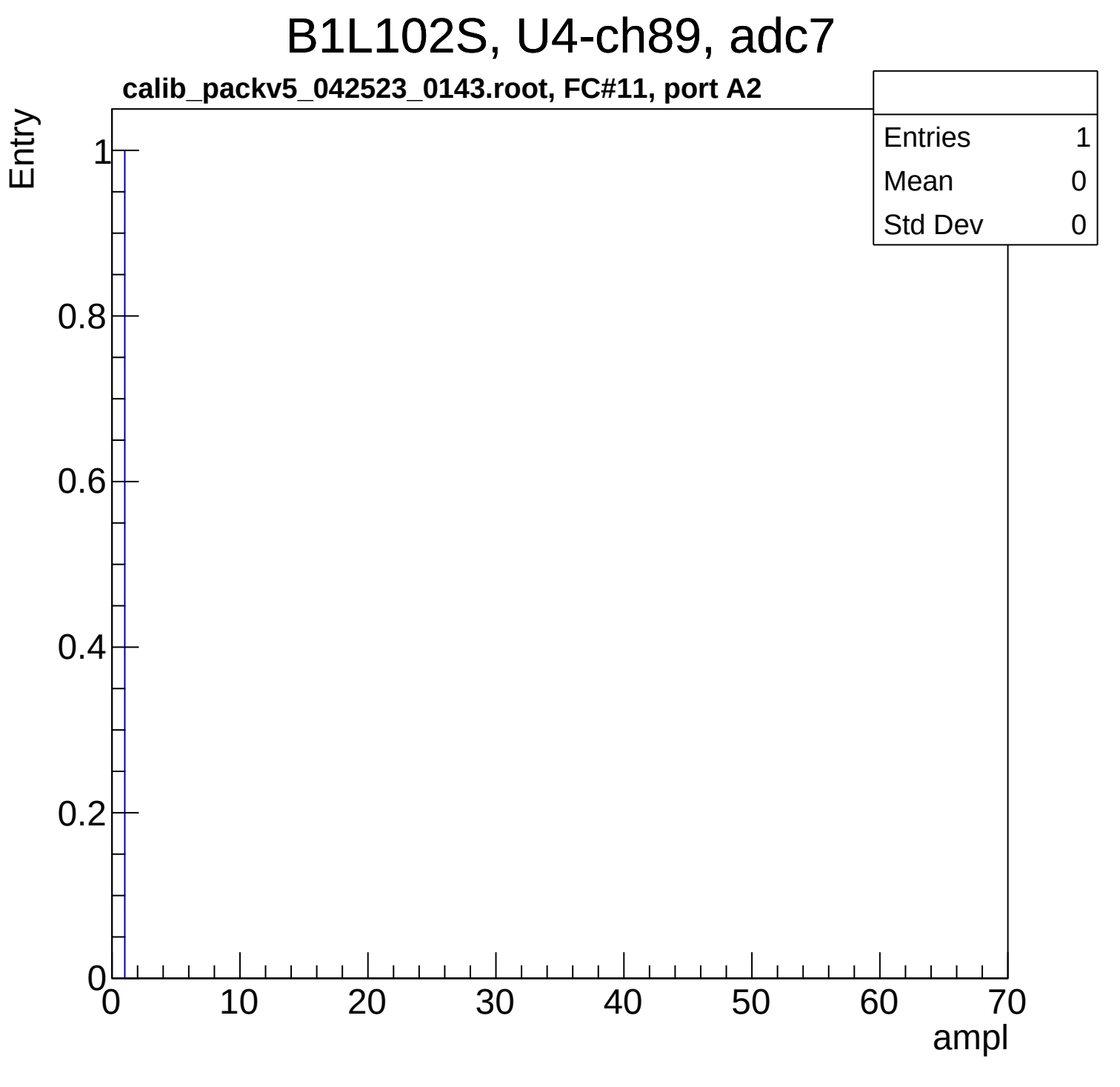

B1L102S, U4-ch89, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 9
Mean 62.11
Std Dev 0.9938
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U4-ch89, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
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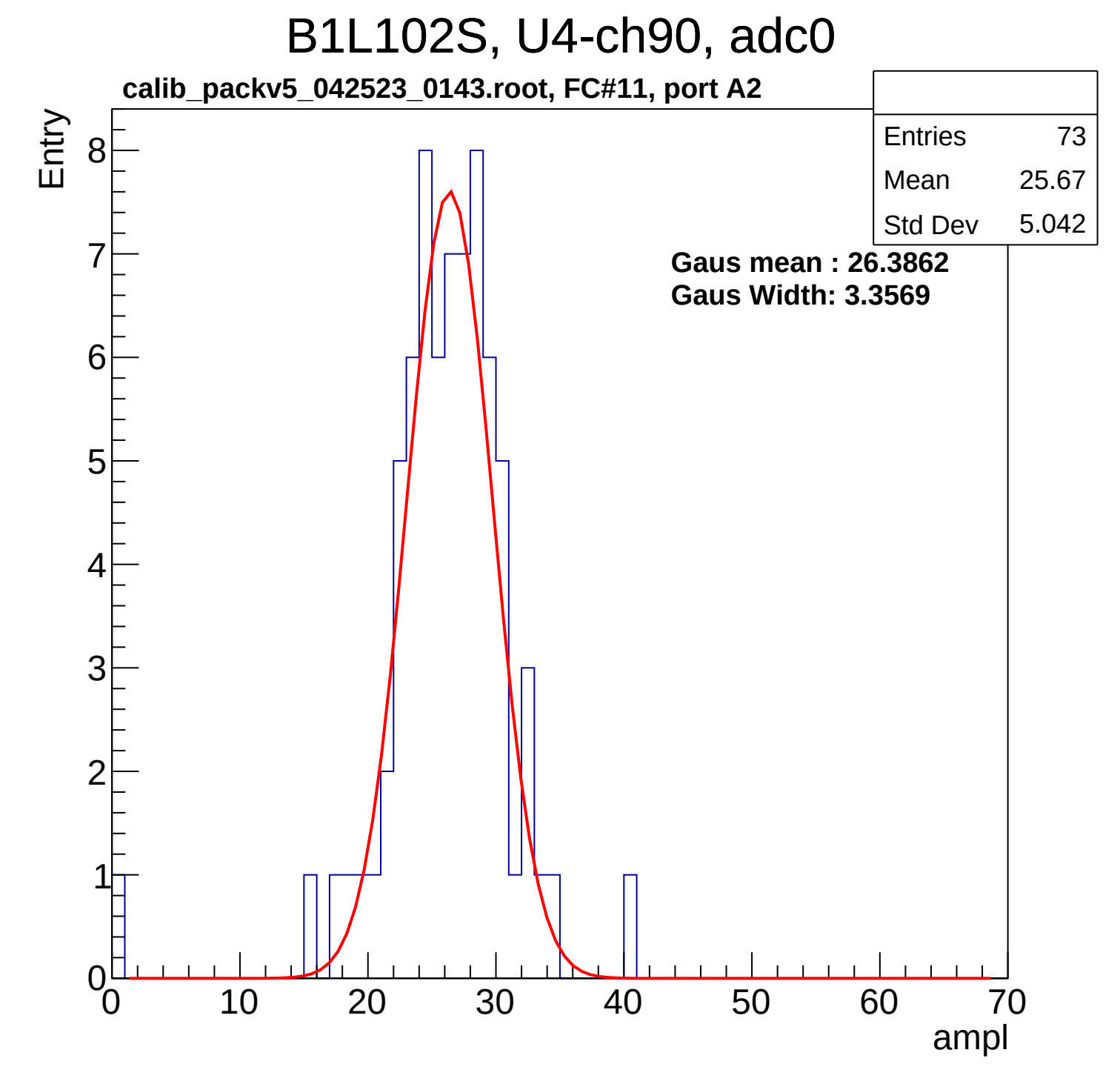
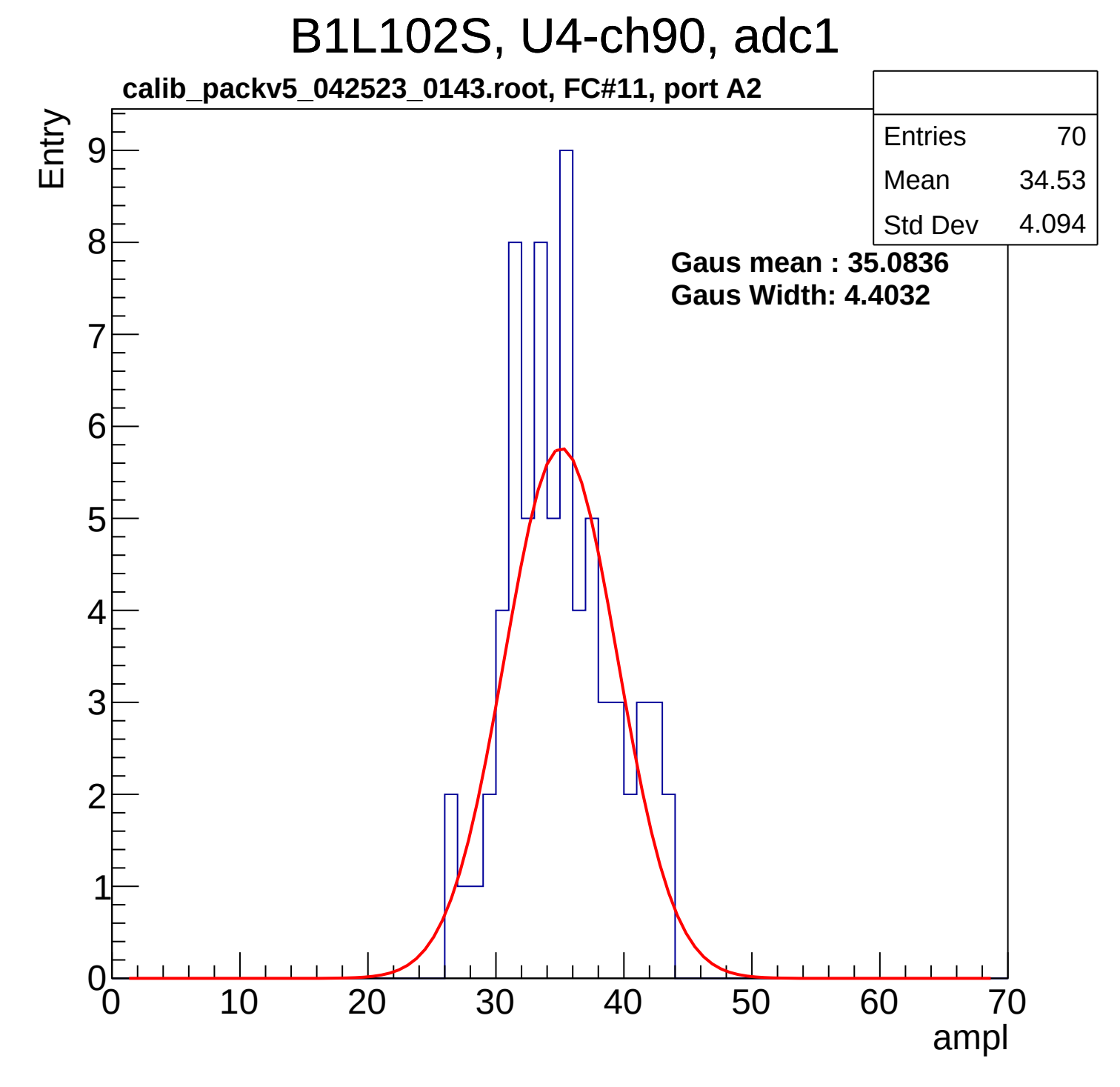
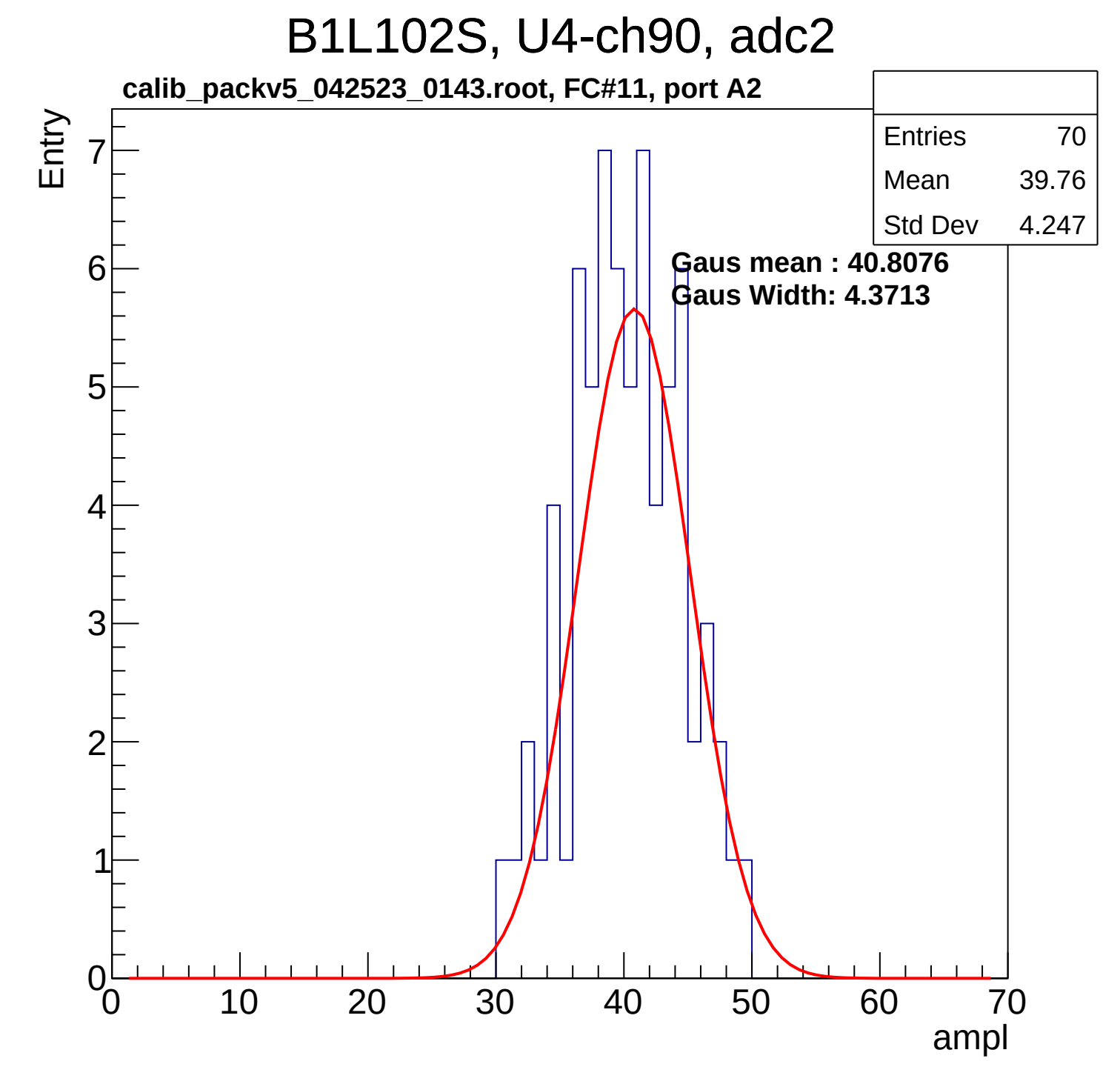
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch90, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 25.67
Std Dev 5.042
Gaus mean : 26.3862
Gaus Width: 3.3569
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch90, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 34.53
Std Dev 4.094
Gaus mean : 35.0836
Gaus Width: 4.4032
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch90, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 39.76
Std Dev 4.247
Gaus mean : 40.8076
Gaus Width: 4.3713
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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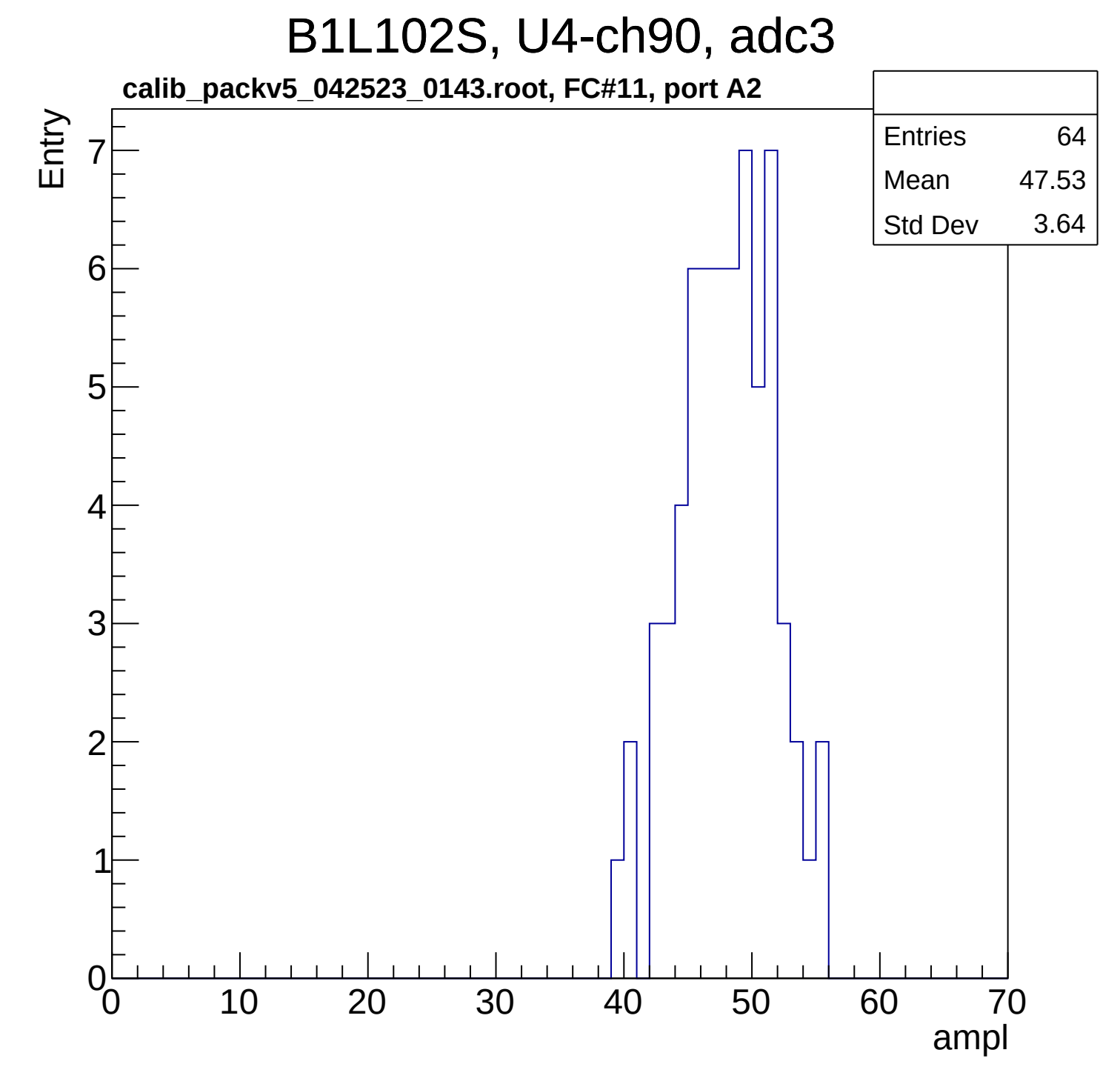
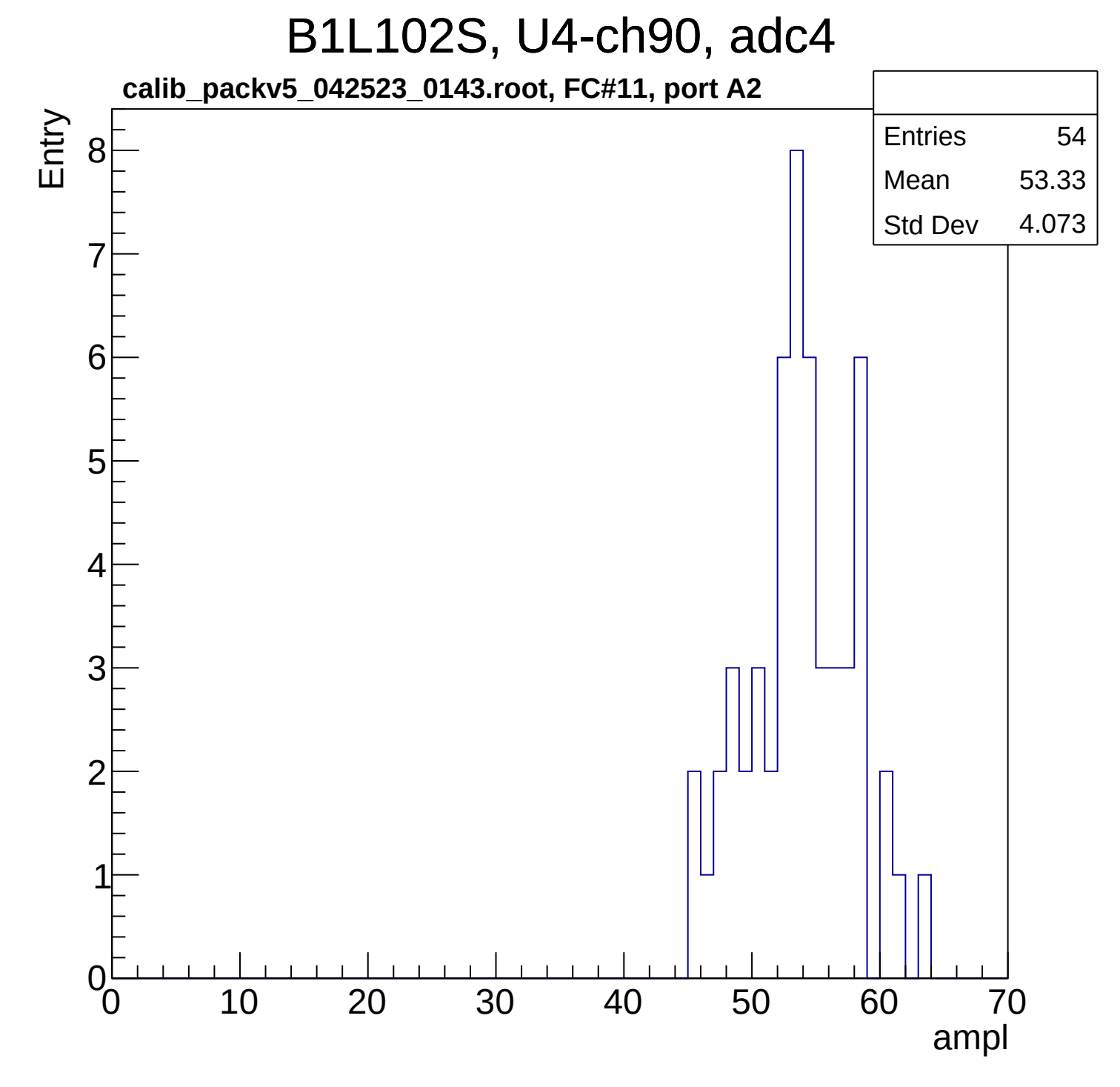

B1L102S, U4-ch90, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 47.53
Std Dev 3.64
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch90, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 53.33
Std Dev 4.073
Entry
ampl
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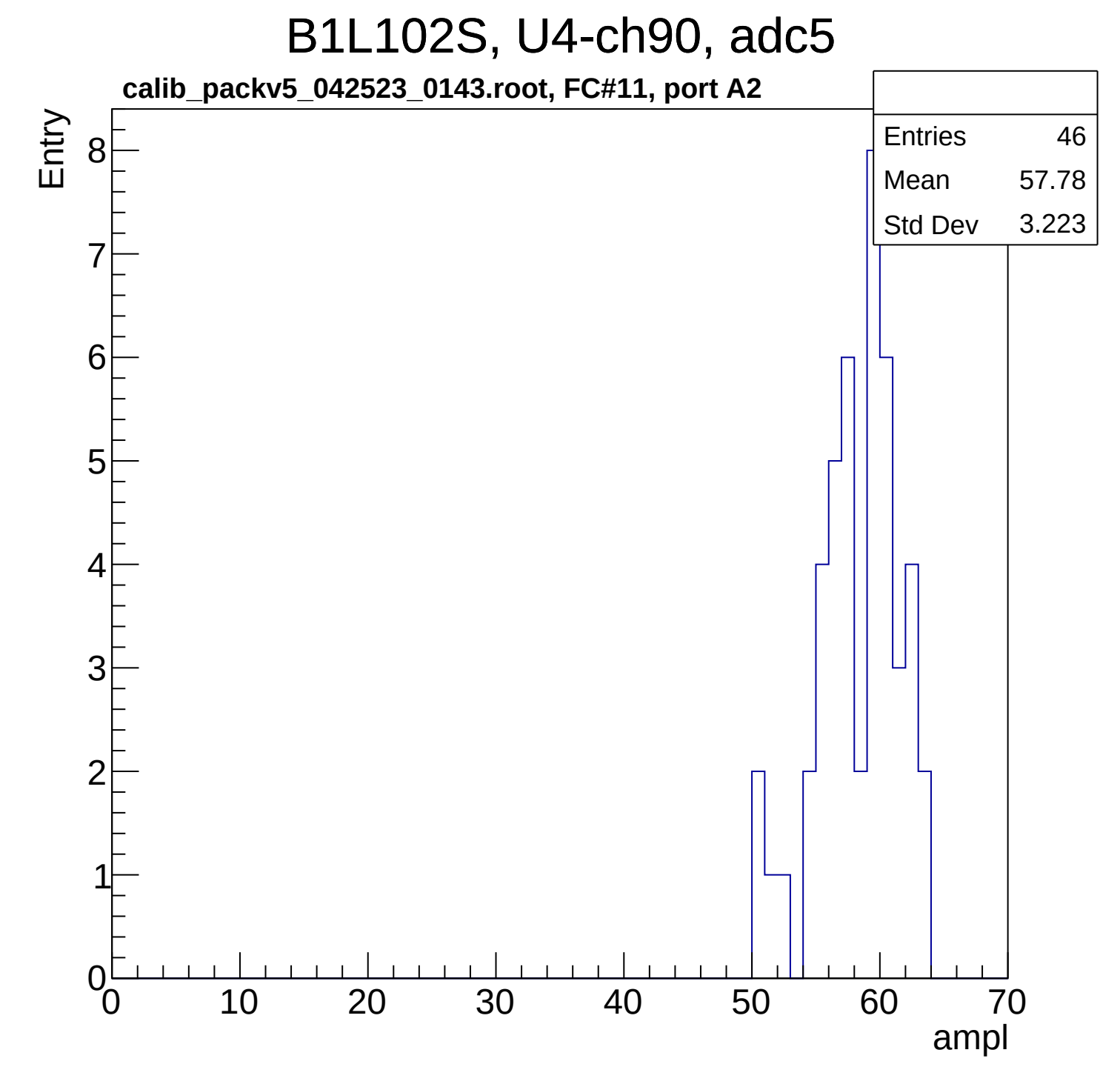
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch90, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 46
Mean 57.78
Std Dev 3.223
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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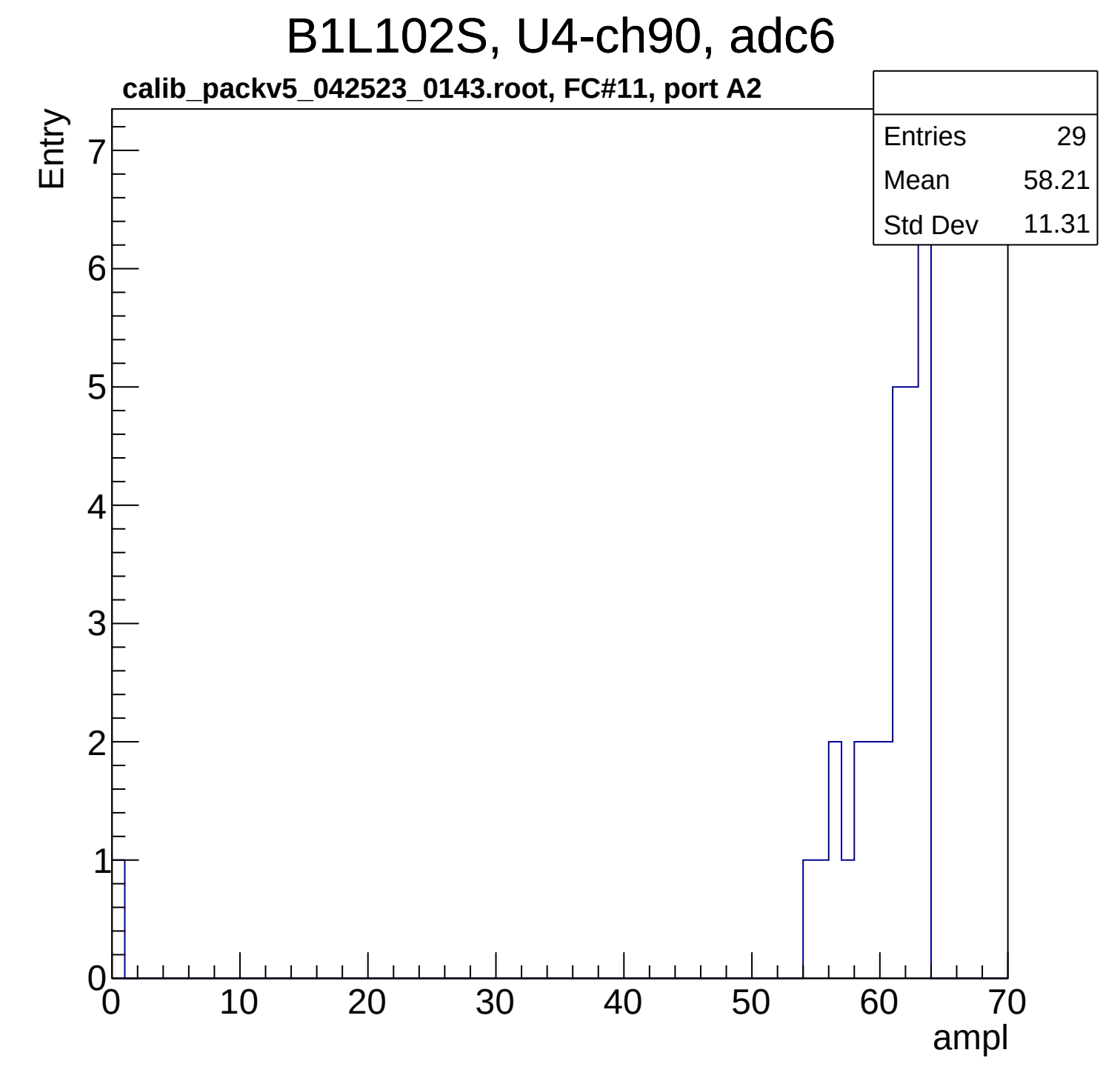
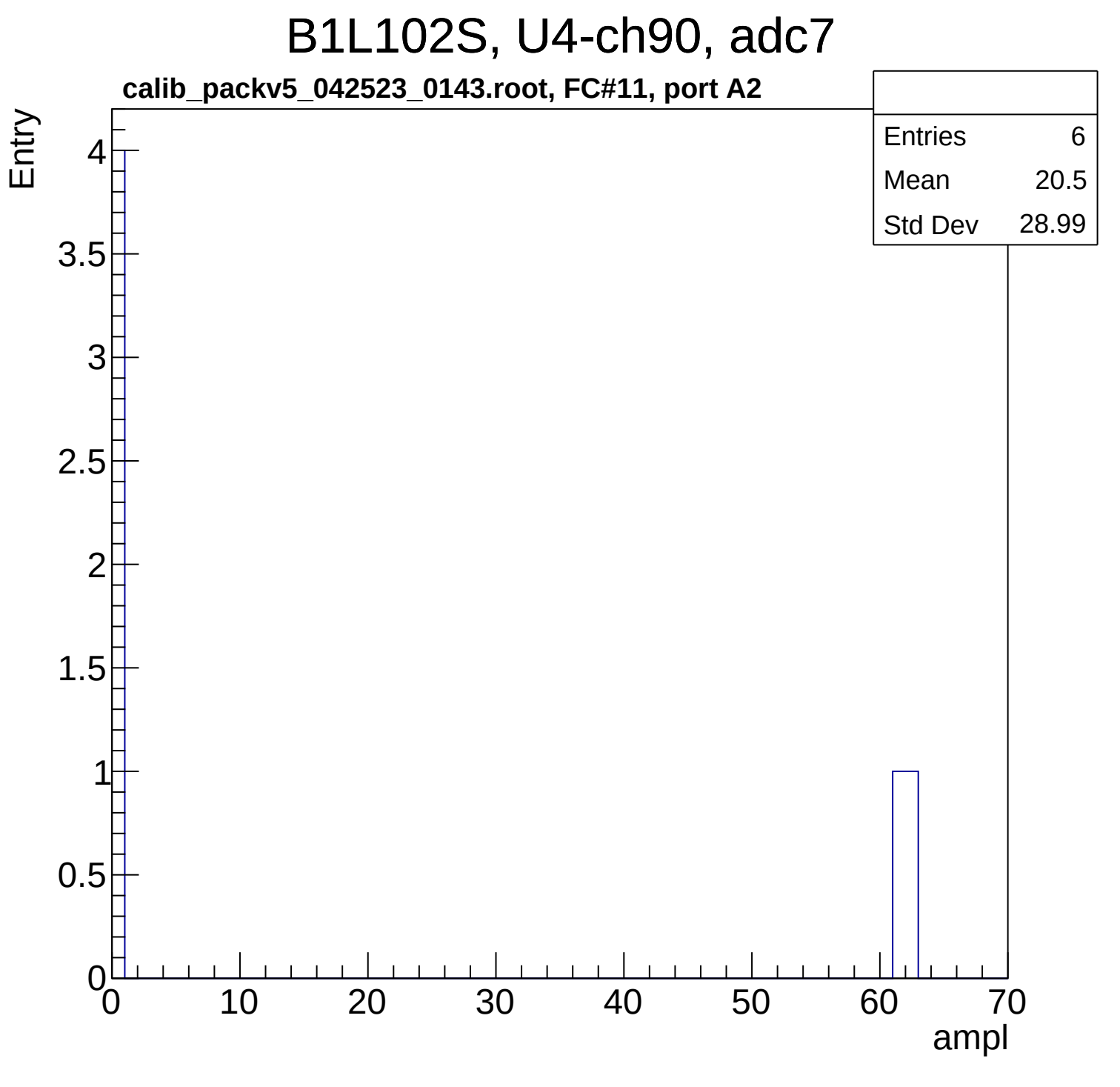

B1L102S, U4-ch90, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 29
Mean 58.21
Std Dev 11.31
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch90, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 6
Mean 20.5
Std Dev 28.99
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
10
20
30
40
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60
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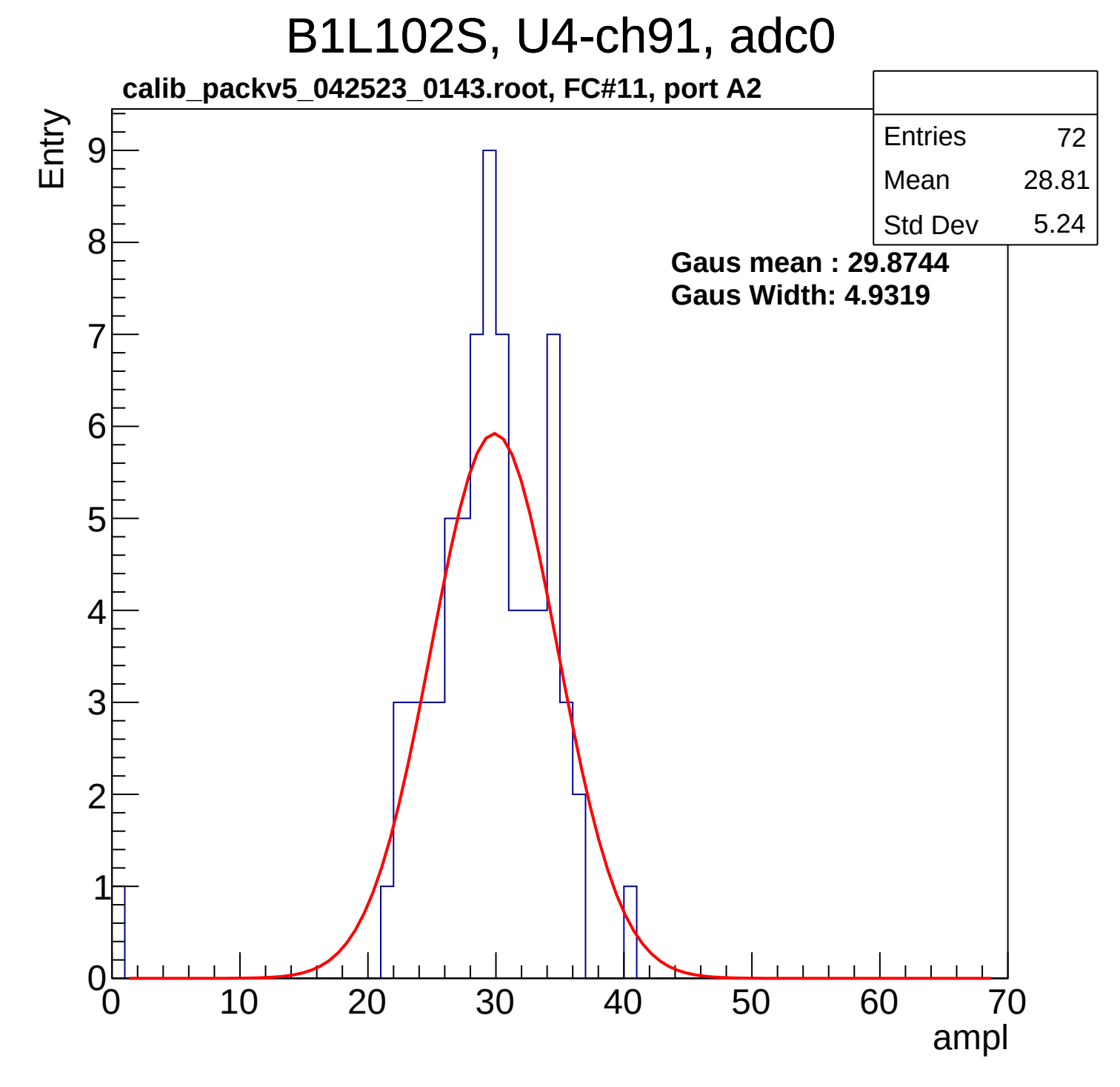
B1L102S, U4-ch91, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 72
Mean 28.81
Std Dev 5.24
Gaus mean : 29.8744
Gaus Width: 4.9319
Entry
ampl
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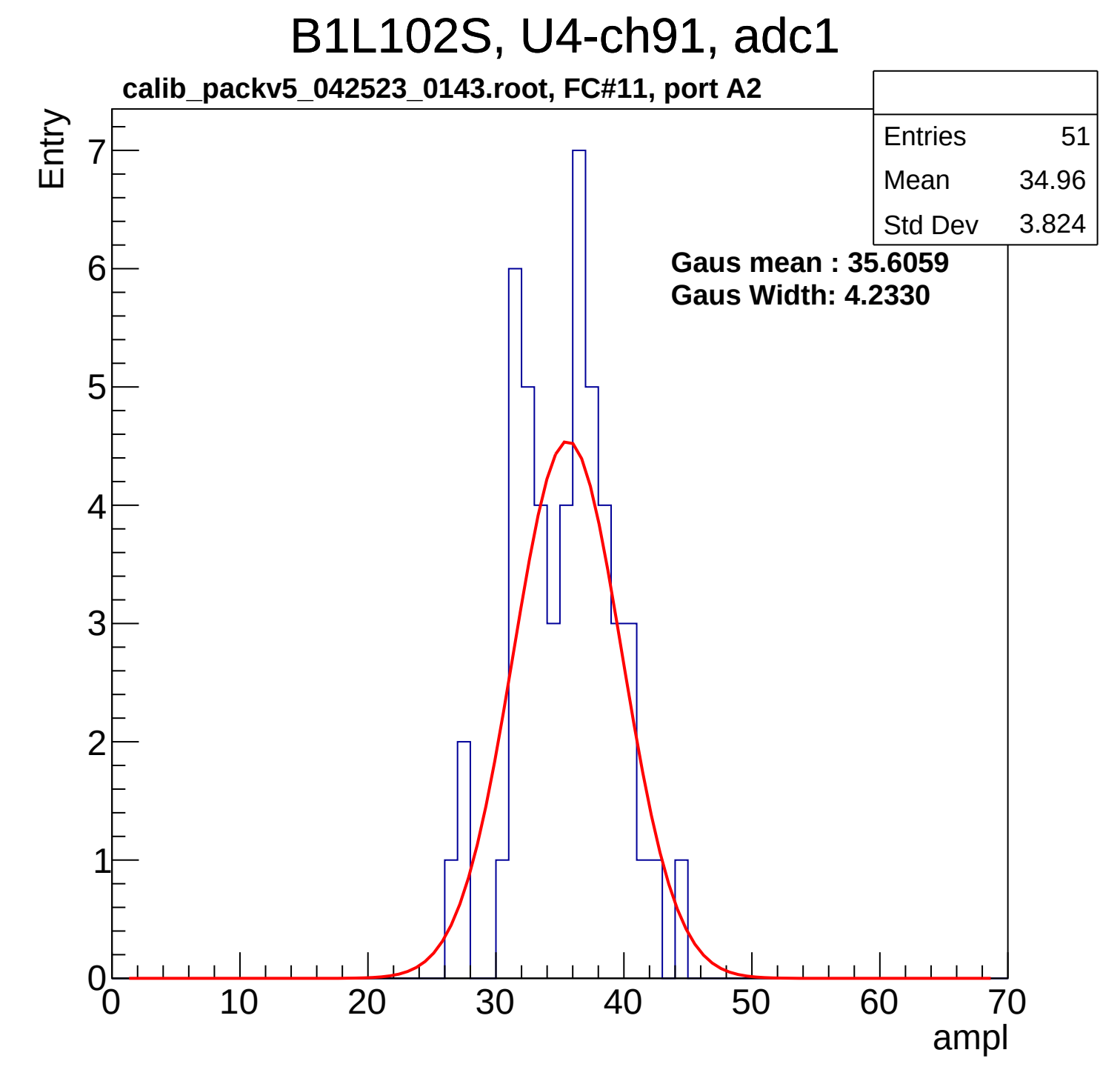
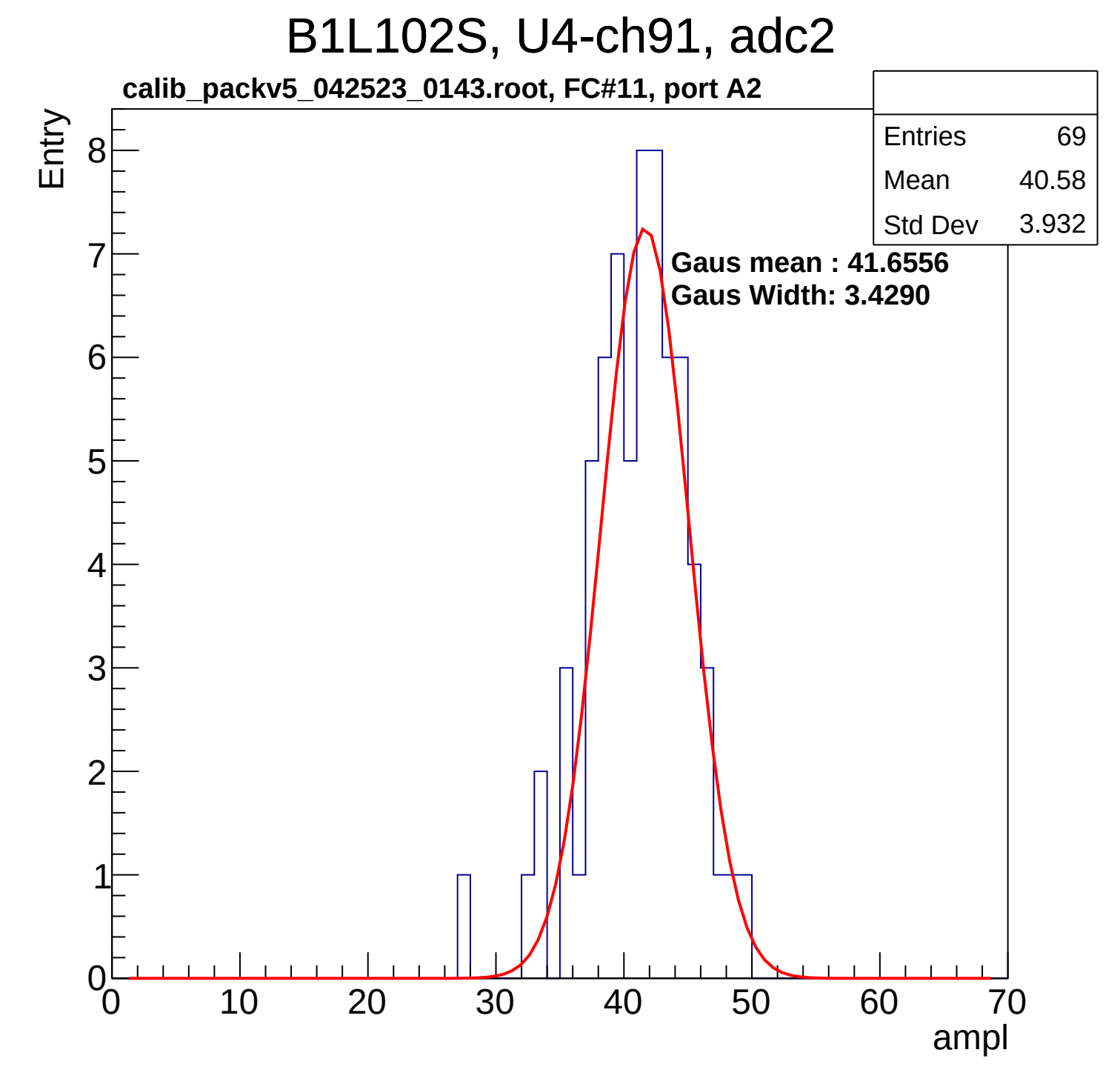
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L102S, U4-ch91, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 34.96
Std Dev 3.824
Gaus mean : 35.6059
Gaus Width: 4.2330
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch91, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 40.58
Std Dev 3.932
Gaus mean : 41.6556
Gaus Width: 3.4290
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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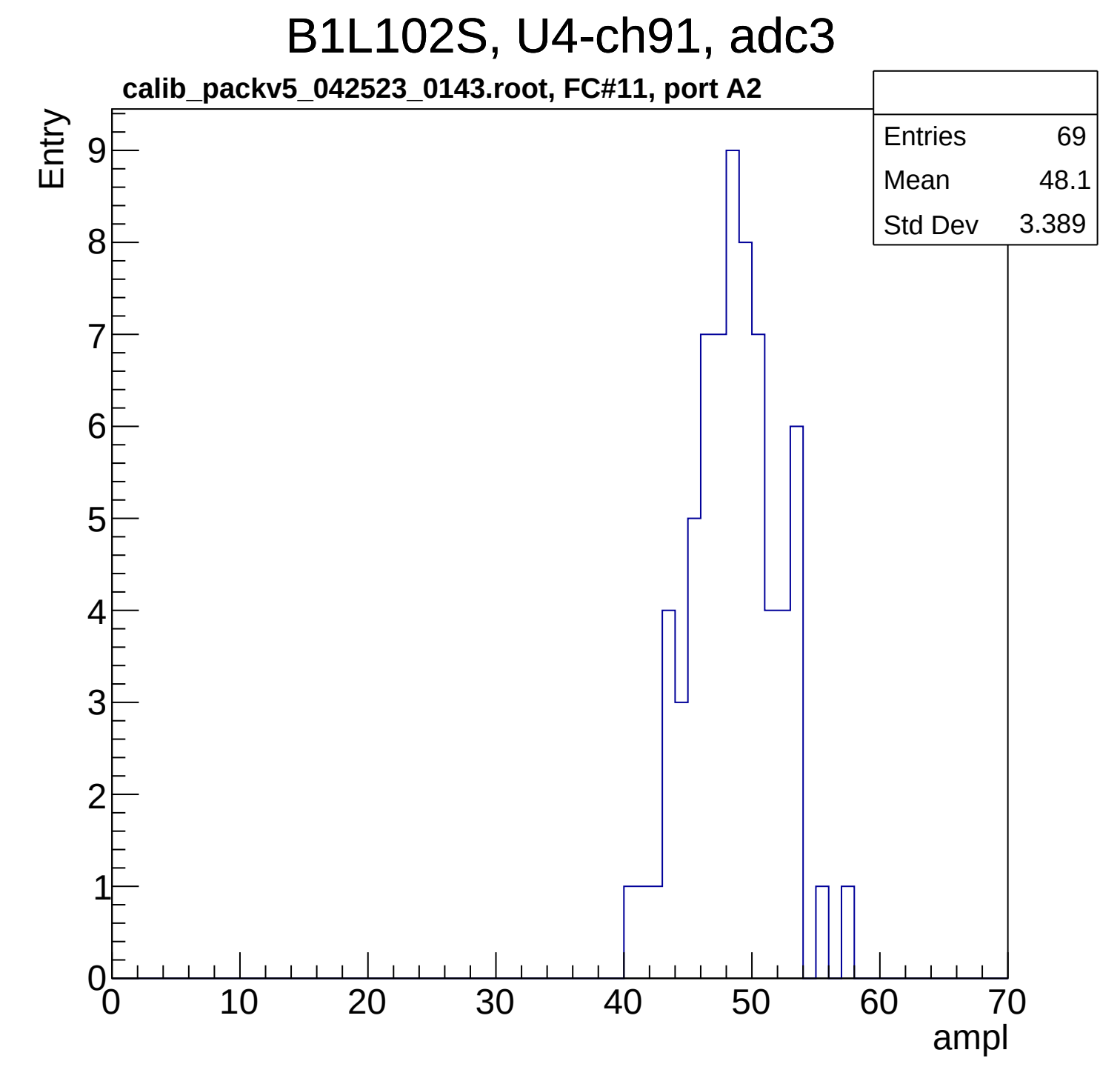
B1L102S, U4-ch91, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 48.1
Std Dev 3.389
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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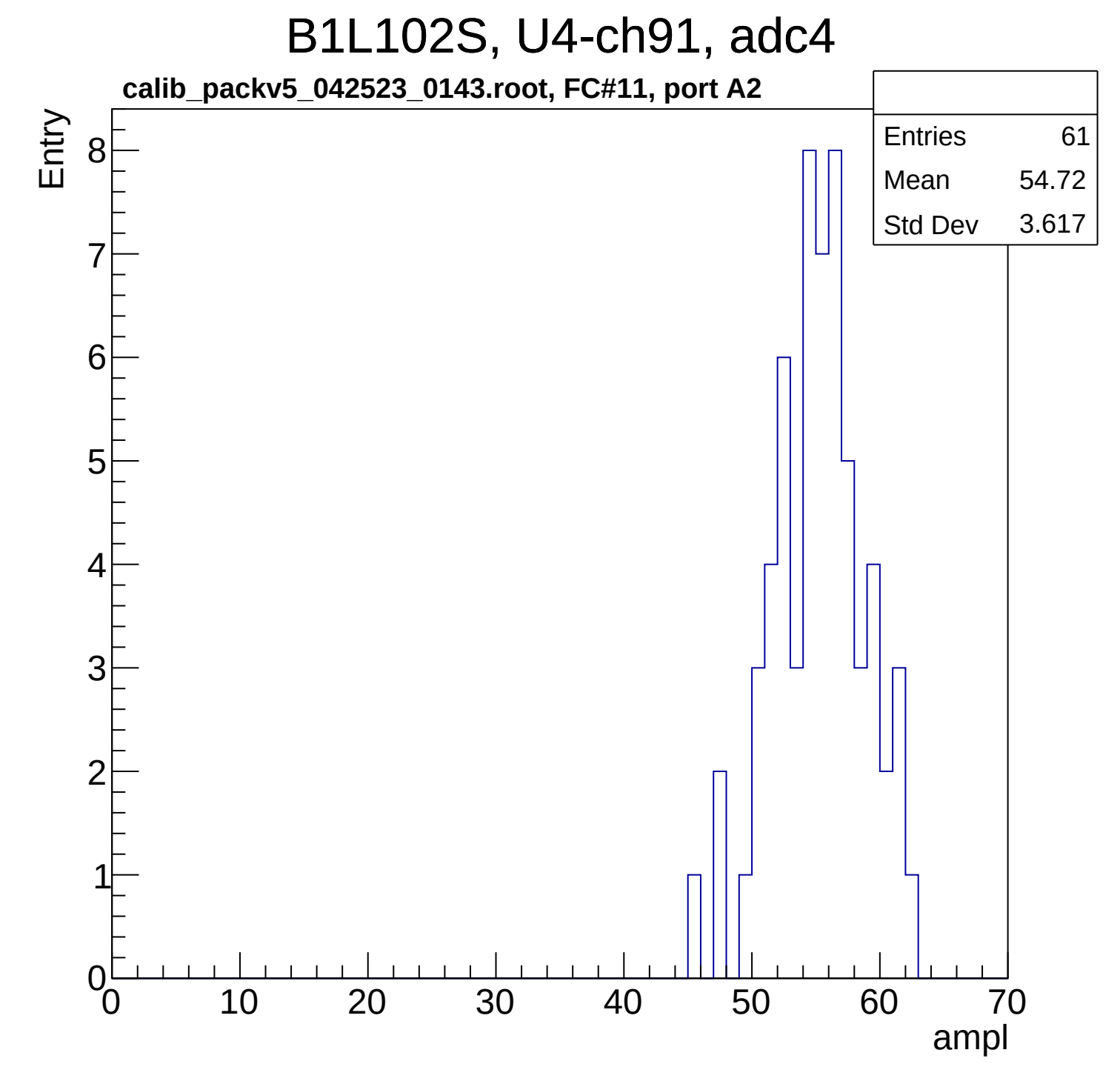
60
70


B1L102S, U4-ch91, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 54.72
Std Dev 3.617
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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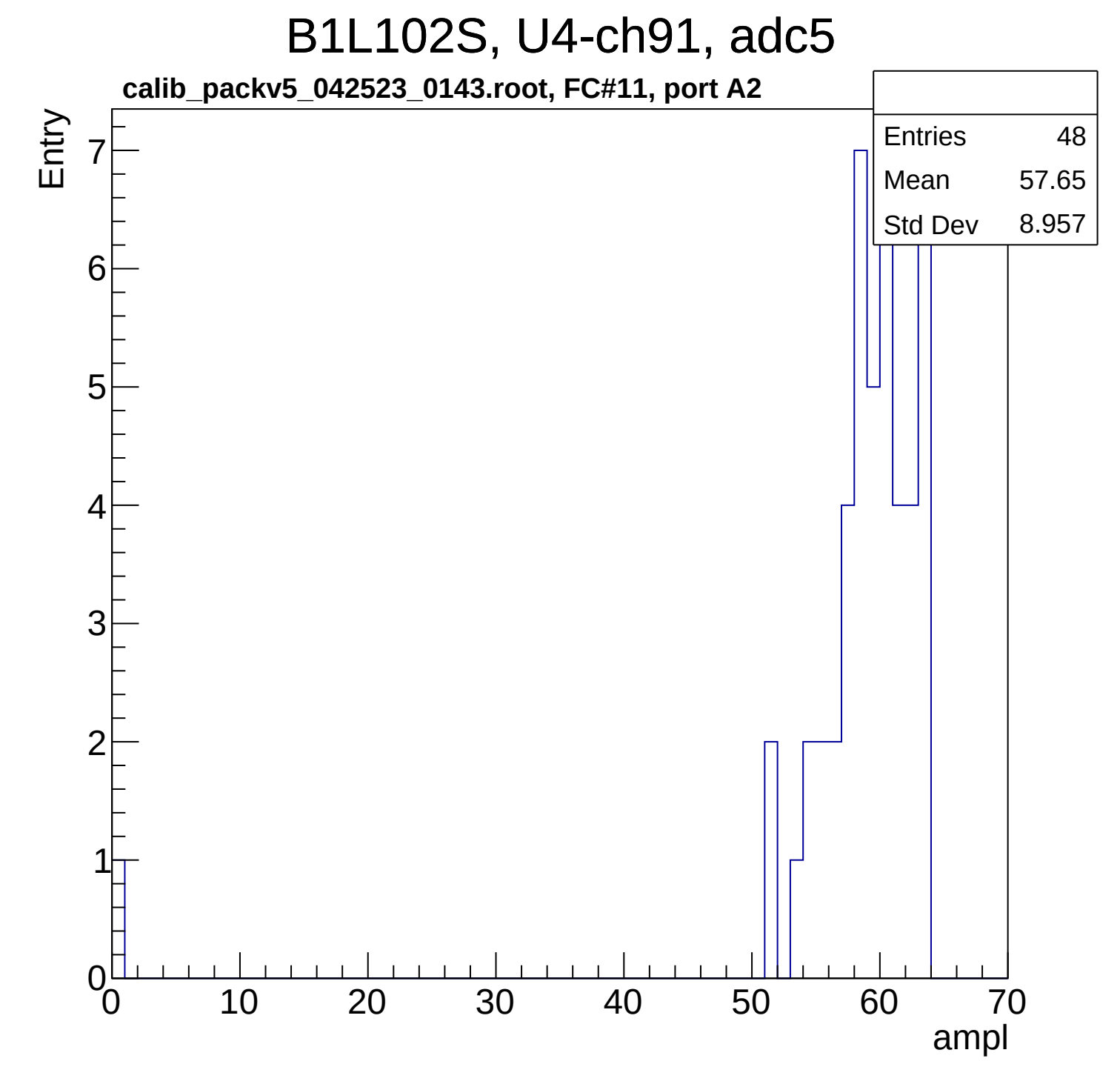
40
50
60
70


B1L102S, U4-ch91, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 48
Mean 57.65
Std Dev 8.957
Entry
ampl
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1
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3
4
5
6
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0
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20
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40
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60
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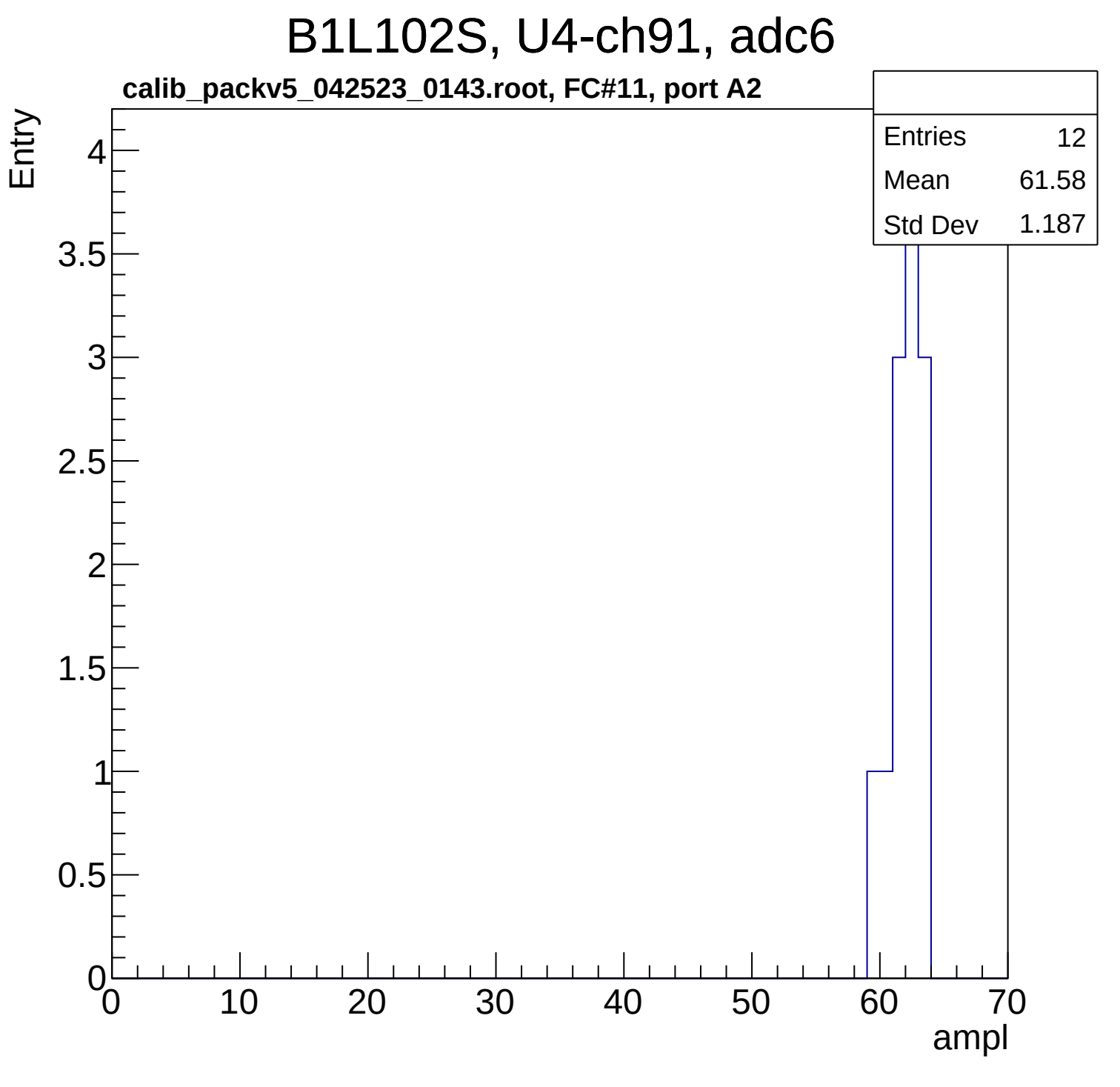
B1L102S, U4-ch91, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 12
Mean 61.58
Std Dev 1.187
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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20
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40
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60
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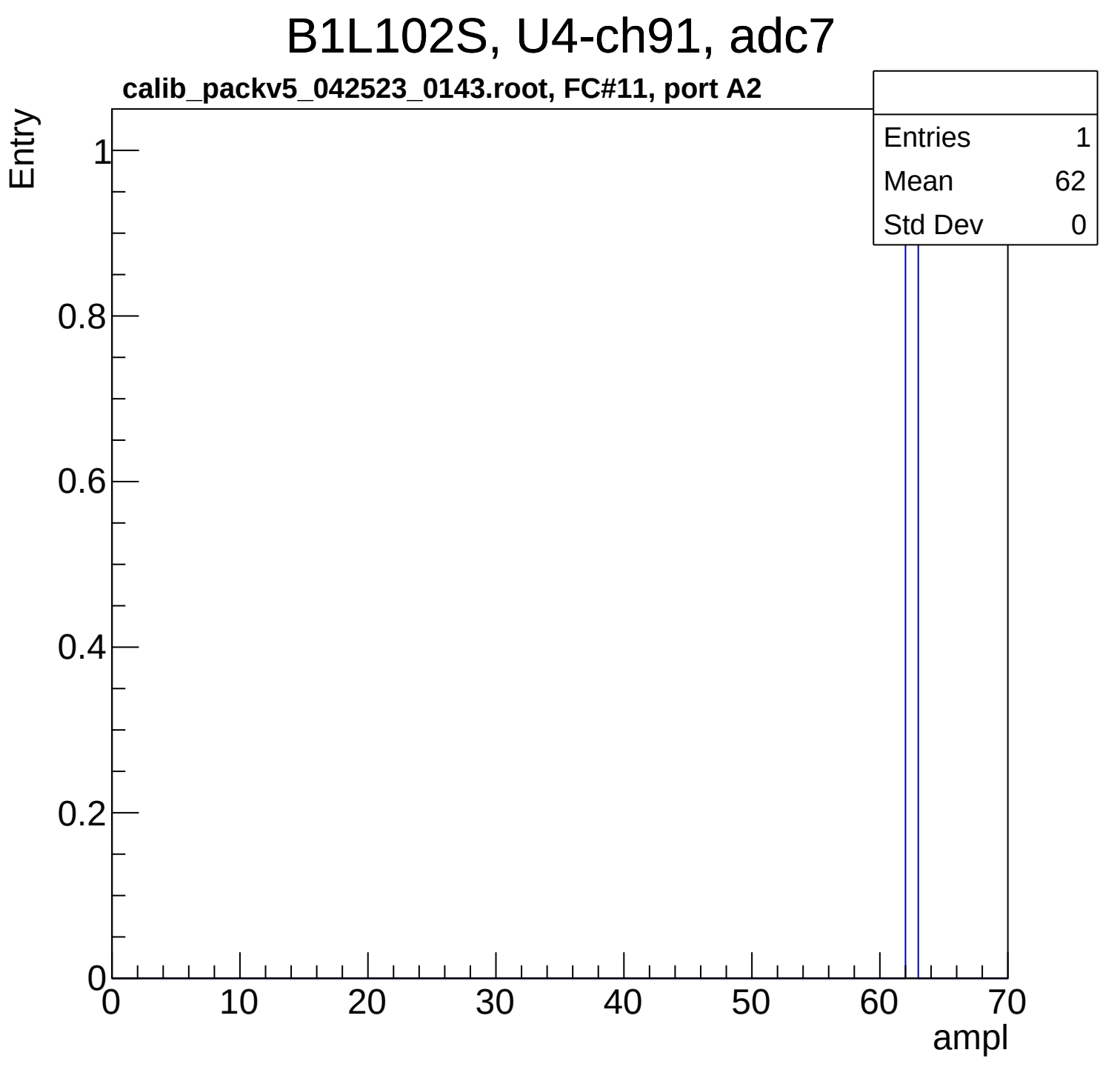
B1L102S, U4-ch91, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 62
Std Dev 0
Entry
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0.6
0.4
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10
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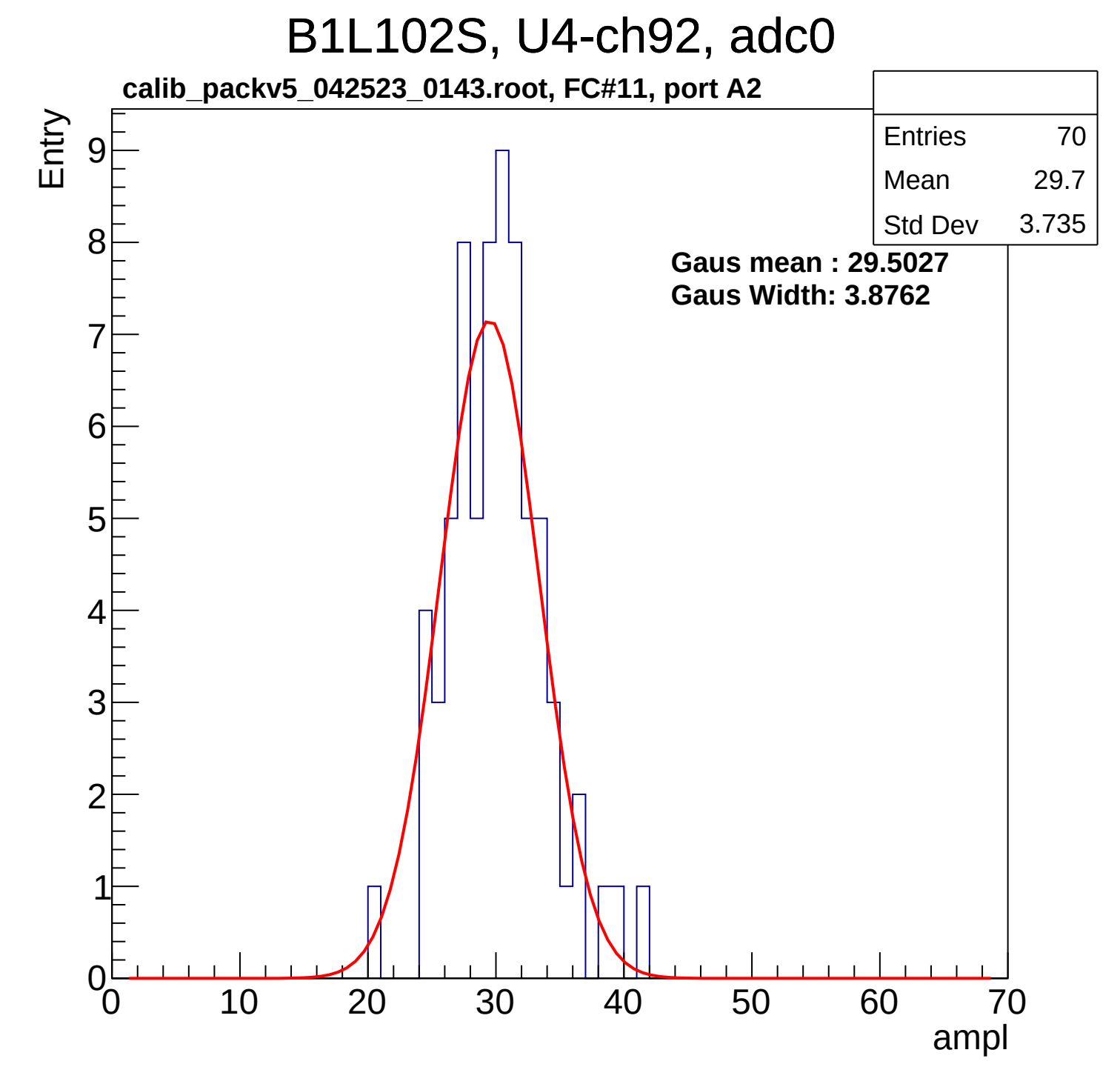
50
60
70
ampl


B1L102S, U4-ch92, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 29.7
Std Dev 3.735
Gaus mean : 29.5027
Gaus Width: 3.8762
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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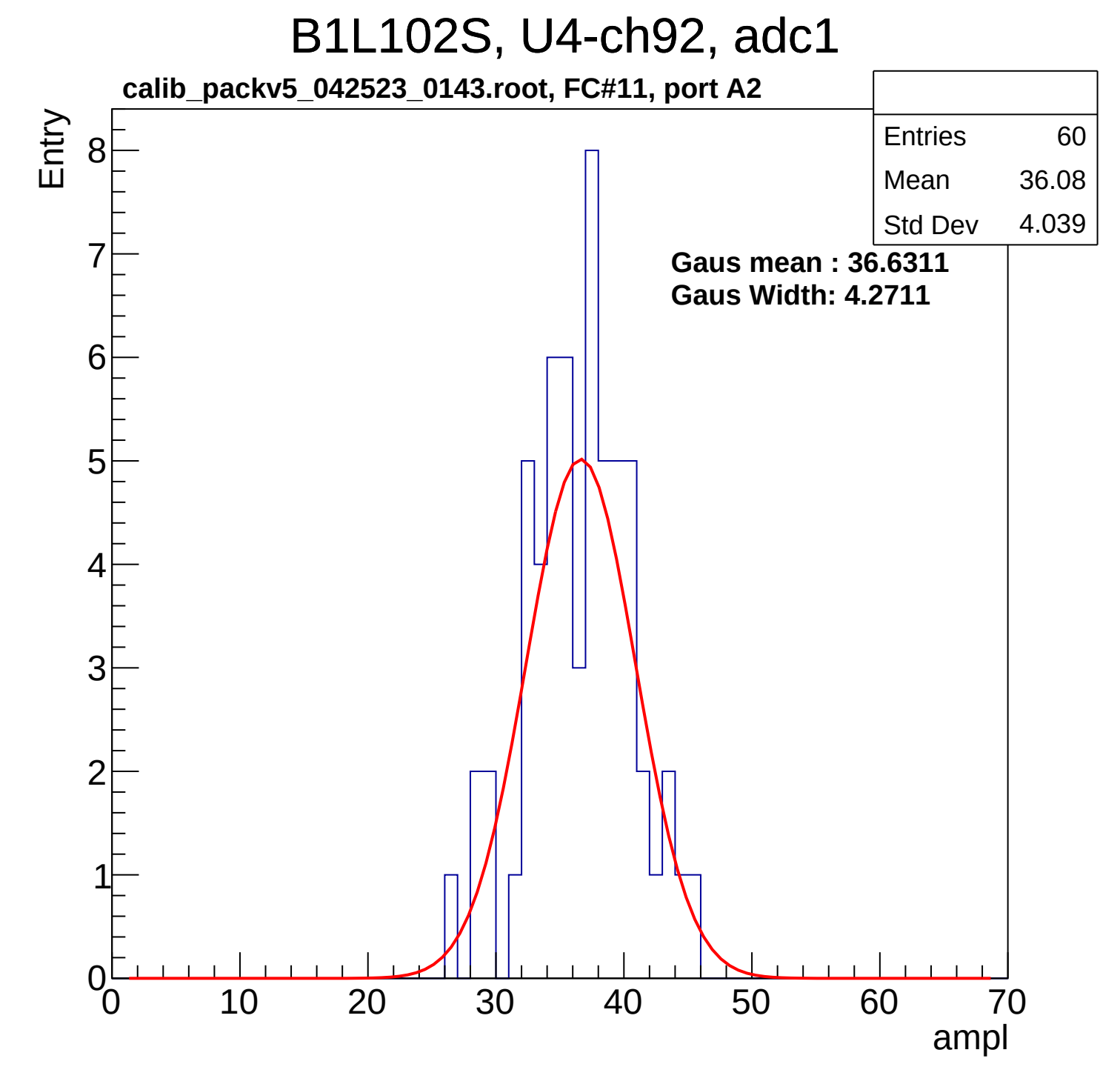
B1L102S, U4-ch92, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 36.08
Std Dev 4.039
Gaus mean : 36.6311
Gaus Width: 4.2711
Entry
ampl
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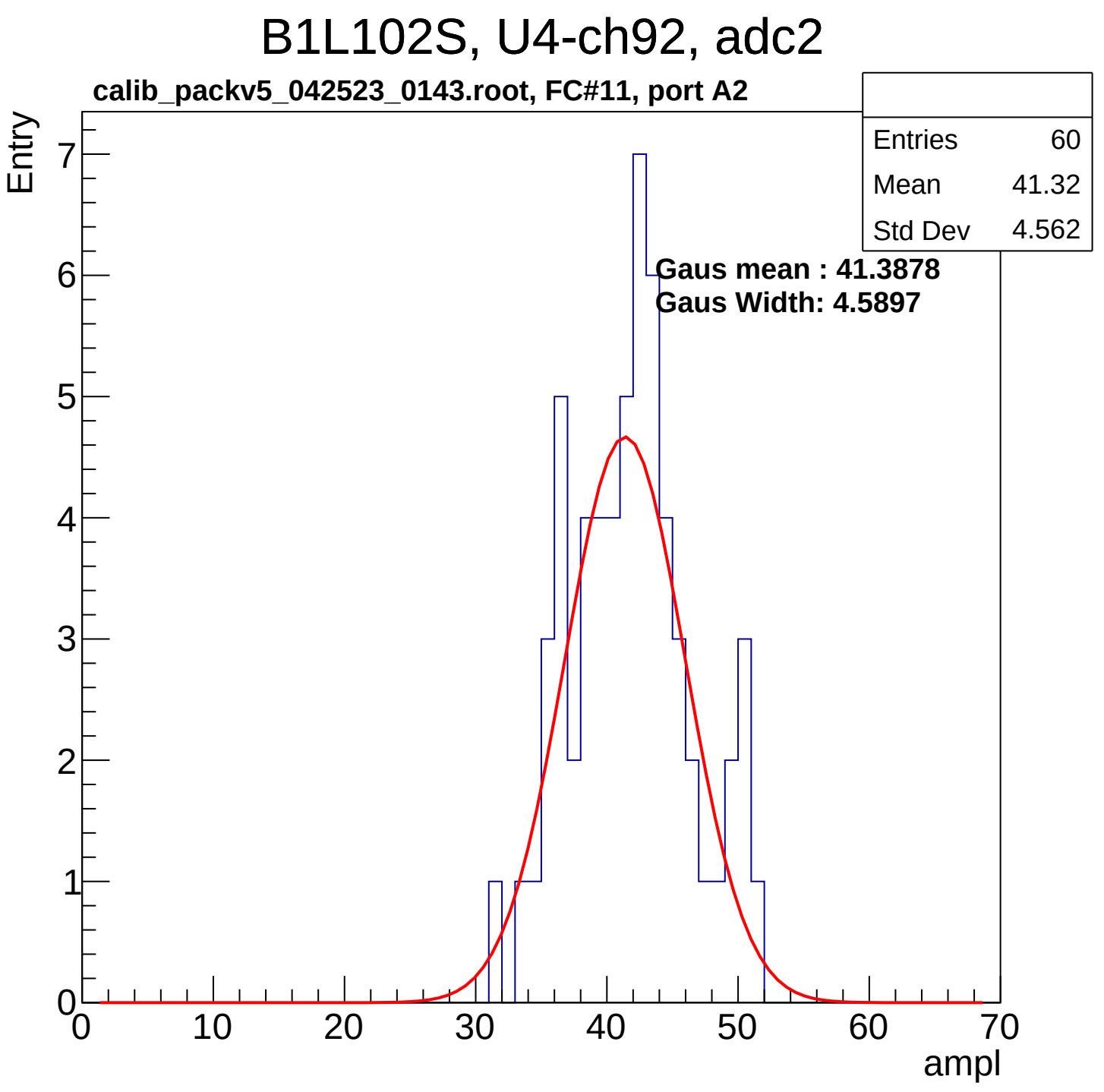
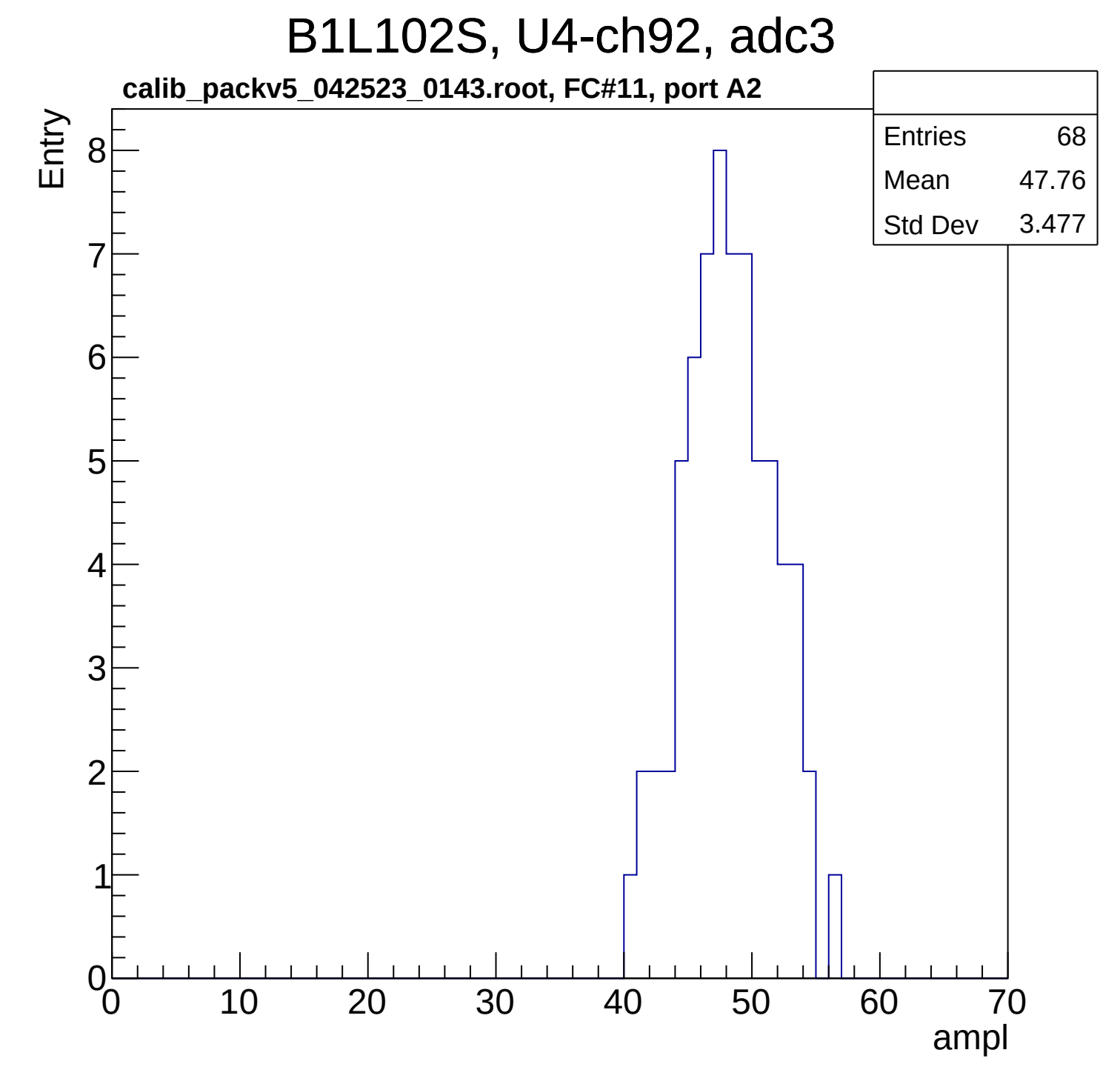
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch92, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 41.32
Std Dev 4.562
Gaus mean : 41.3878
Gaus Width: 4.5897
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch92, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 47.76
Std Dev 3.477
Entry
ampl
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1
2
3
4
5
6
7
8
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20
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60
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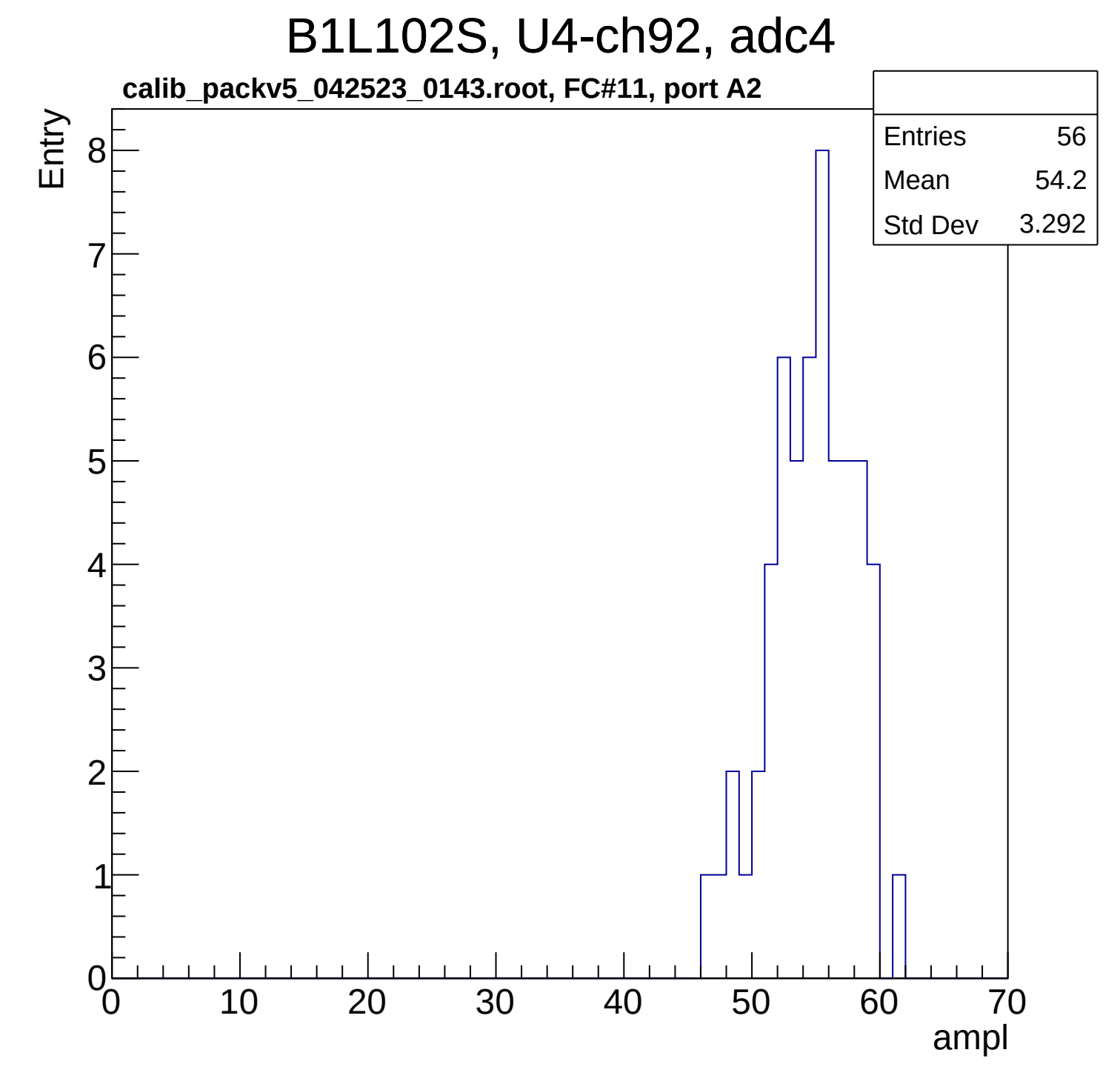
B1L102S, U4-ch92, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 54.2
Std Dev 3.292
Entry
ampl
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4
5
6
7
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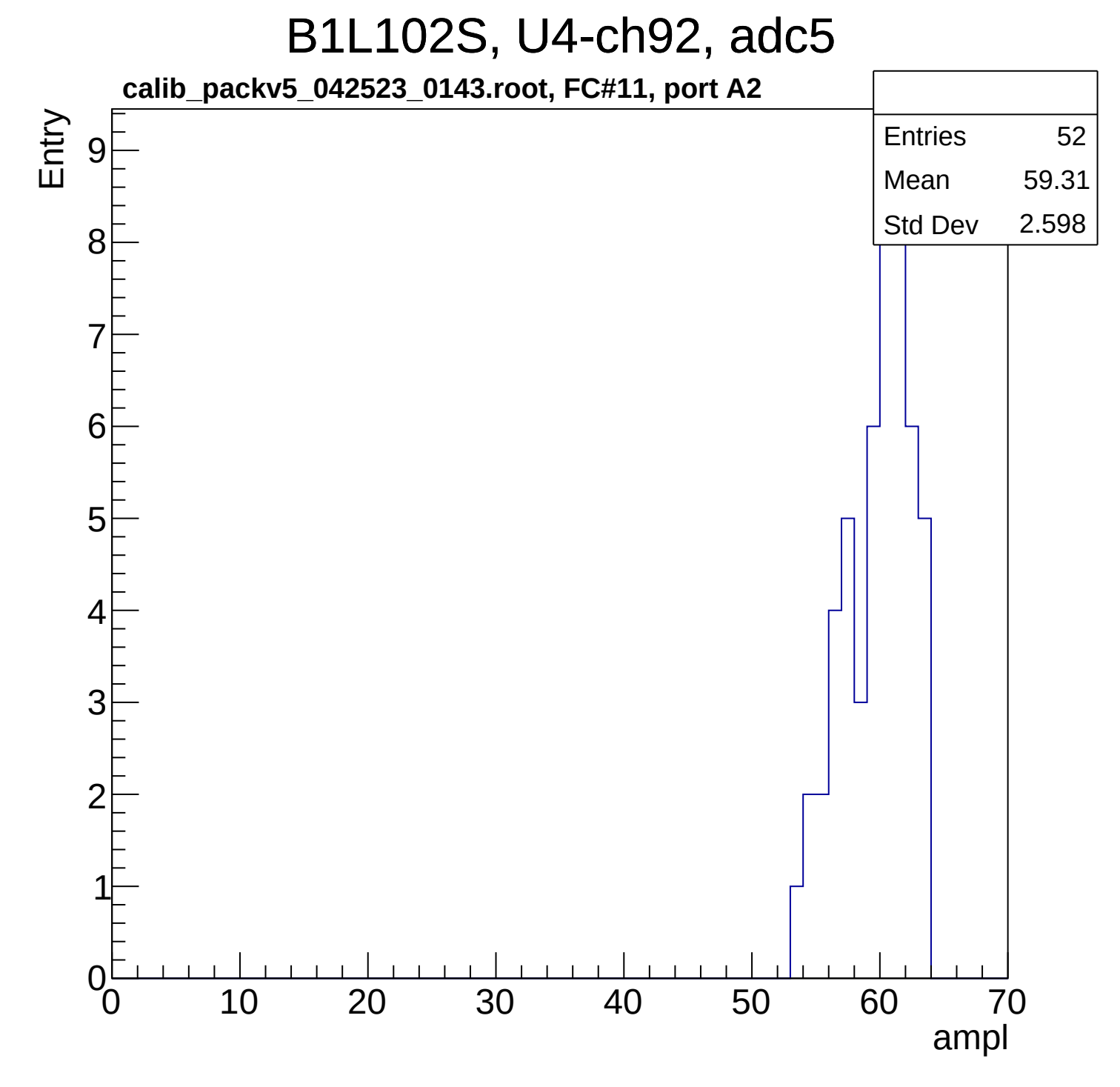
B1L102S, U4-ch92, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 52
Mean 59.31
Std Dev 2.598
Entry
ampl
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3
4
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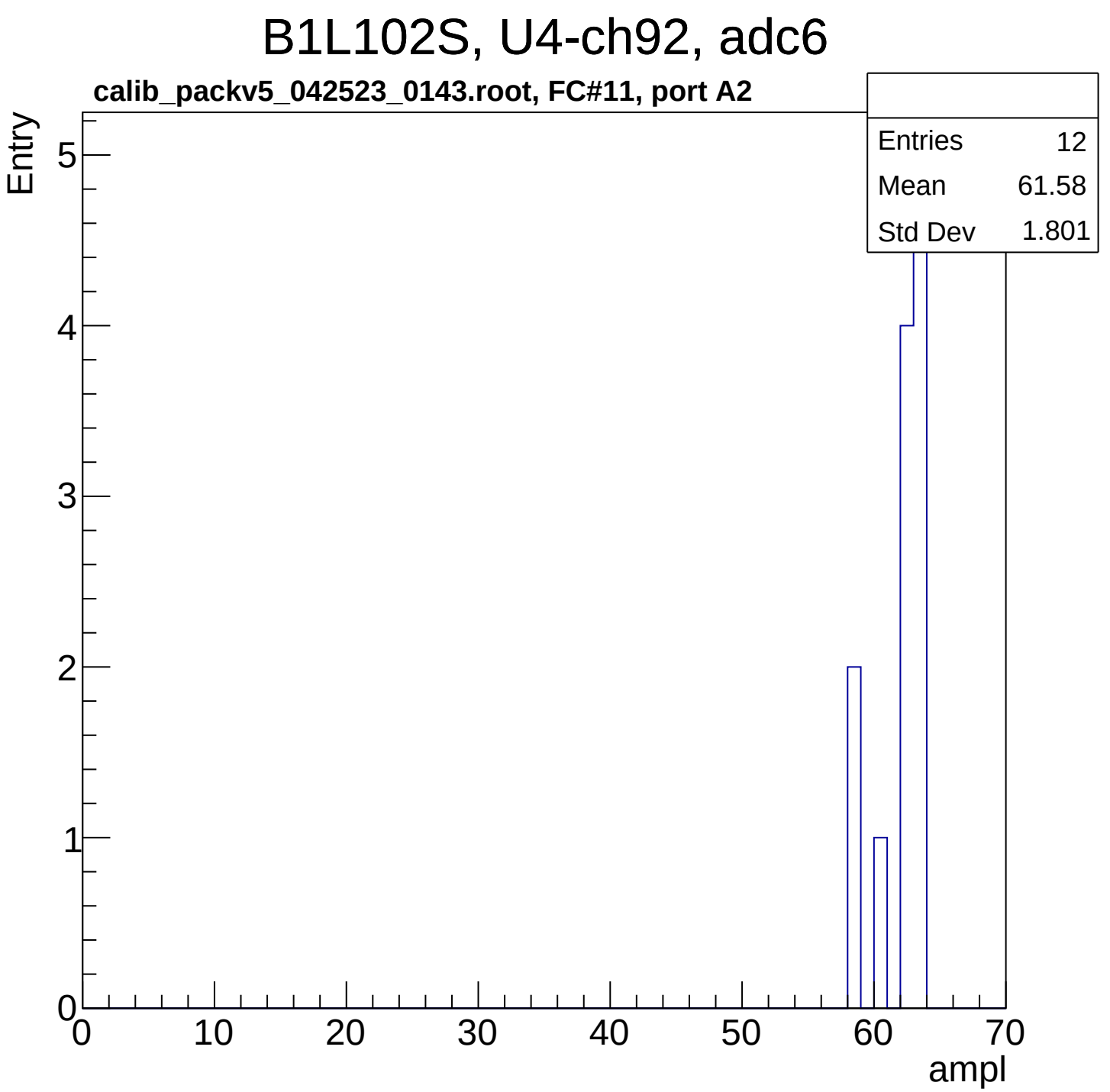
B1L102S, U4-ch92, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 12
Mean 61.58
Std Dev 1.801
Entry
ampl
0
1
2
3
4
5
0
10
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60
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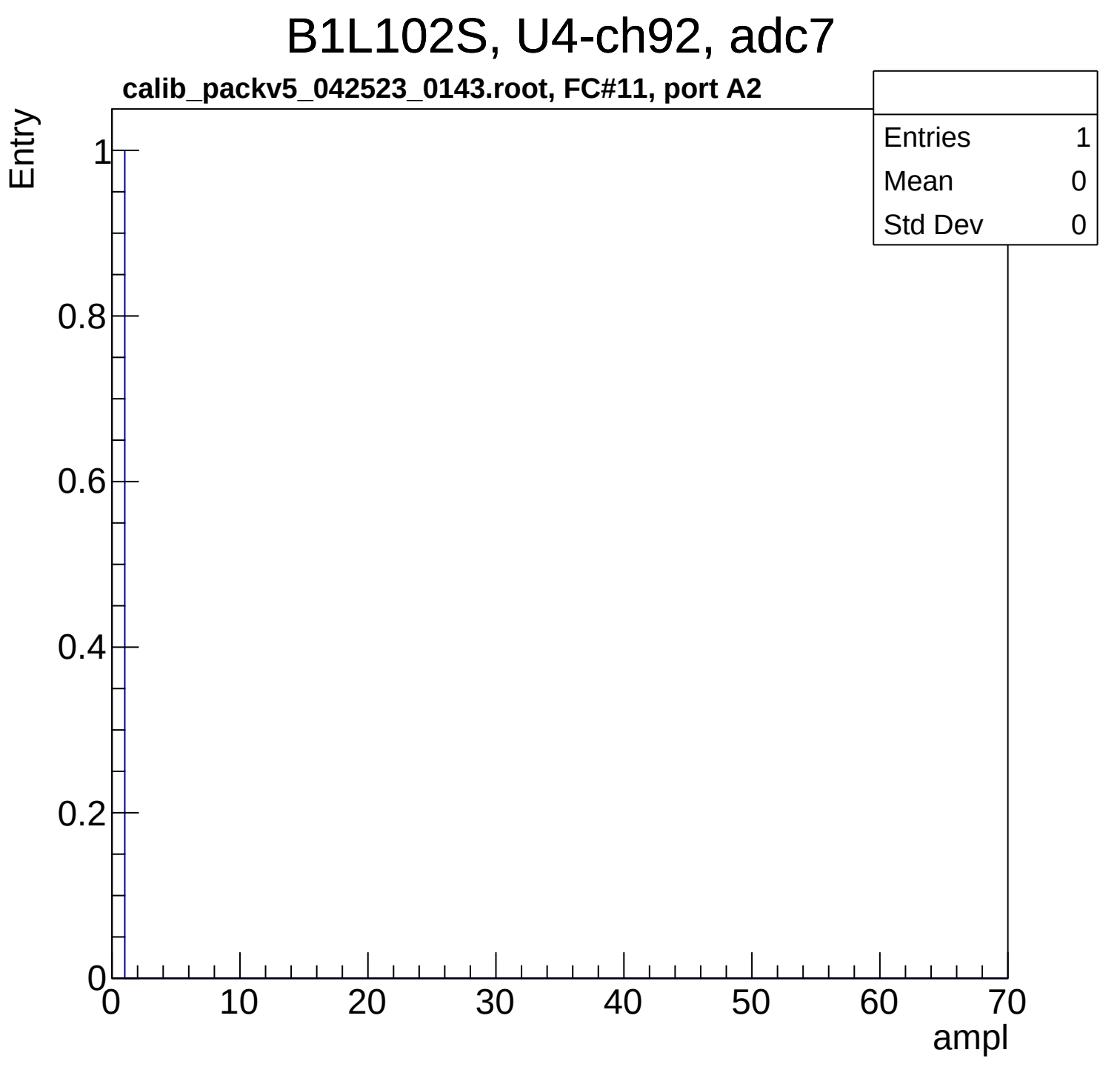
B1L102S, U4-ch92, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
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10
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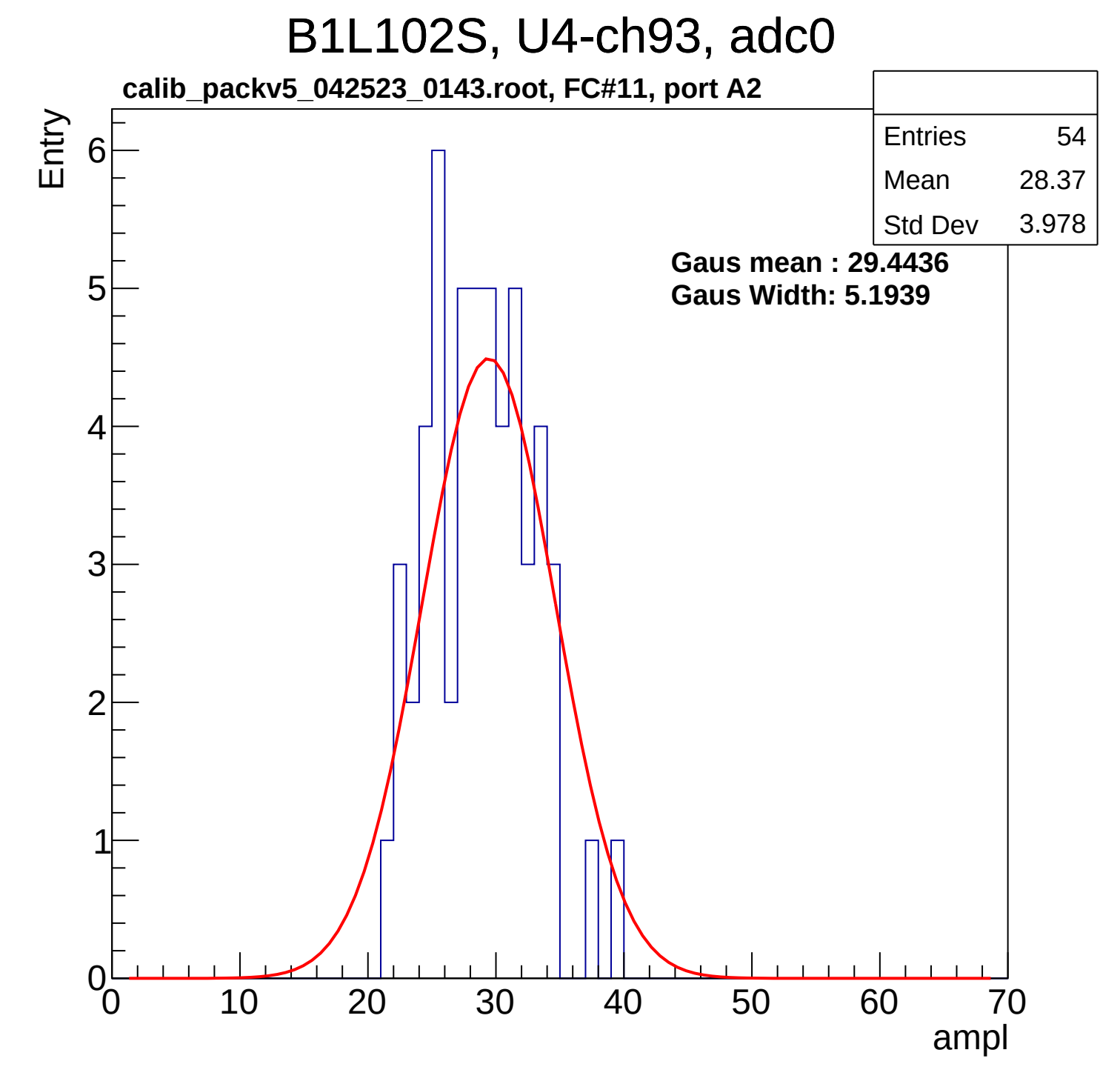
70
ampl


B1L102S, U4-ch93, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 28.37
Std Dev 3.978
Gaus mean : 29.4436
Gaus Width: 5.1939
Entry
ampl
0
1
2
3
4
5
6
0
10
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40
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60
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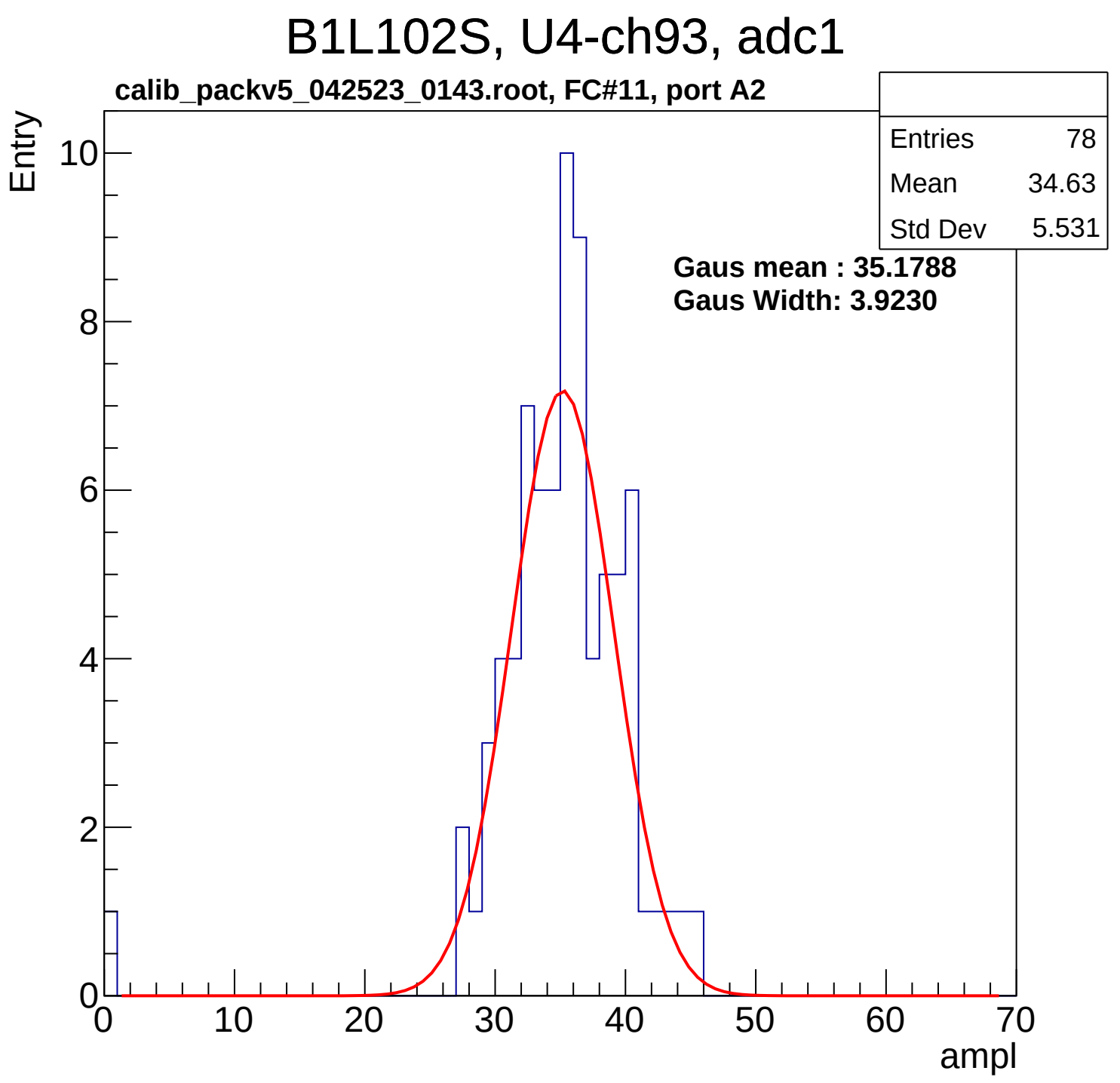
B1L102S, U4-ch93, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 78
Mean 34.63
Std Dev 5.531
Gaus mean : 35.1788
Gaus Width: 3.9230
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
50
60
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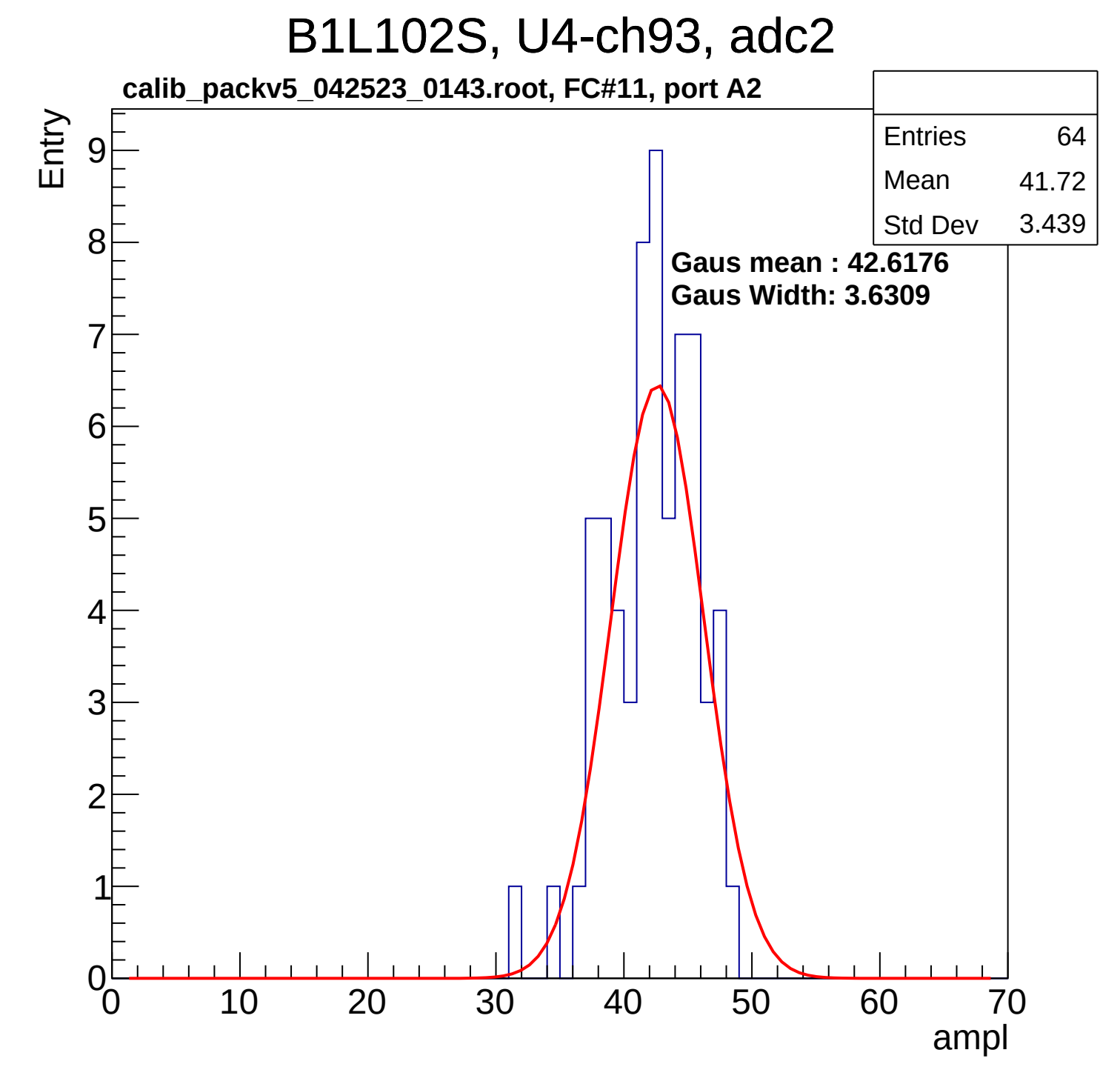
B1L102S, U4-ch93, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 41.72
Std Dev 3.439
Gaus mean : 42.6176
Gaus Width: 3.6309
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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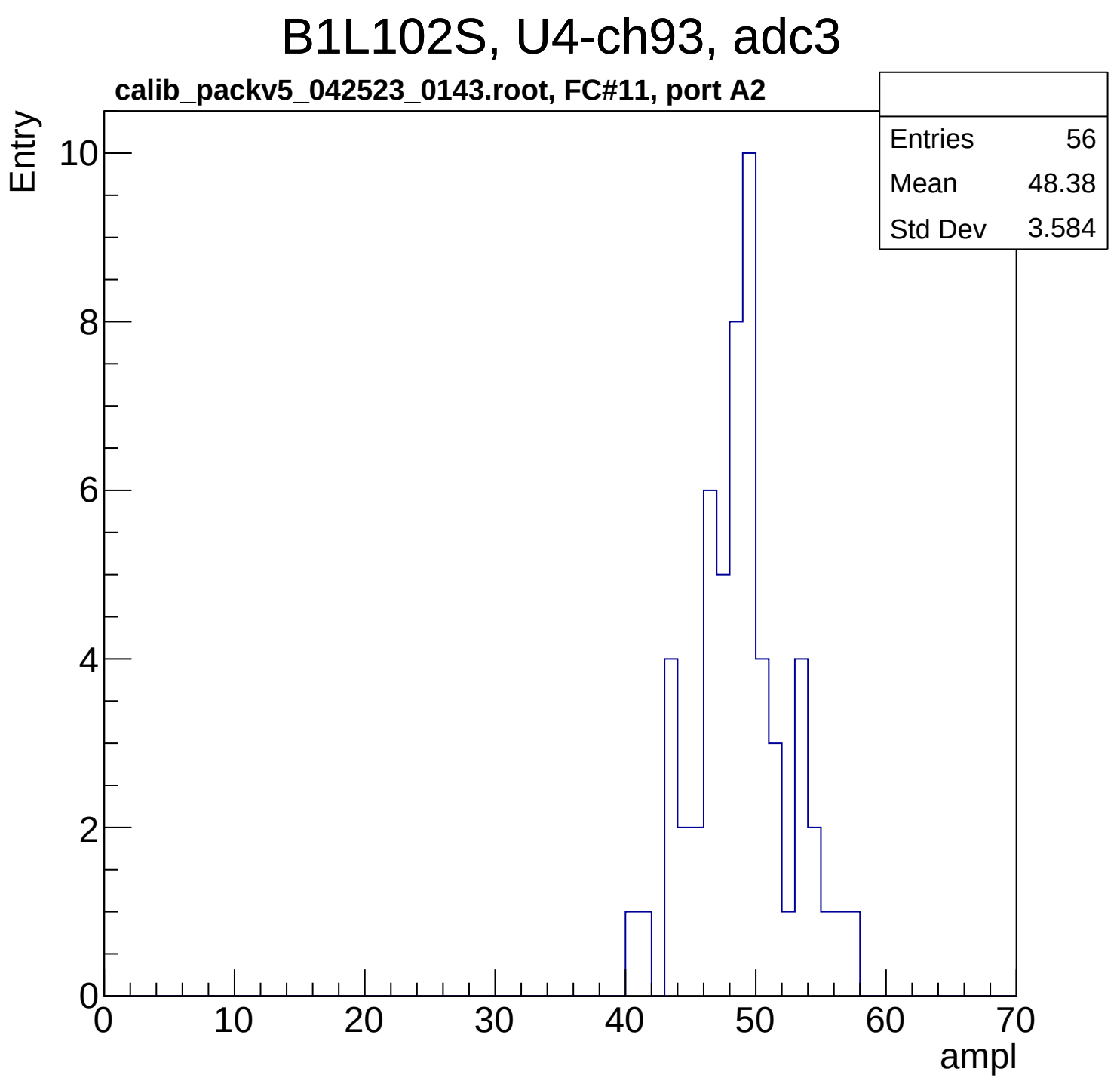
B1L102S, U4-ch93, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 48.38
Std Dev 3.584
Entry
ampl
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2
4
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0
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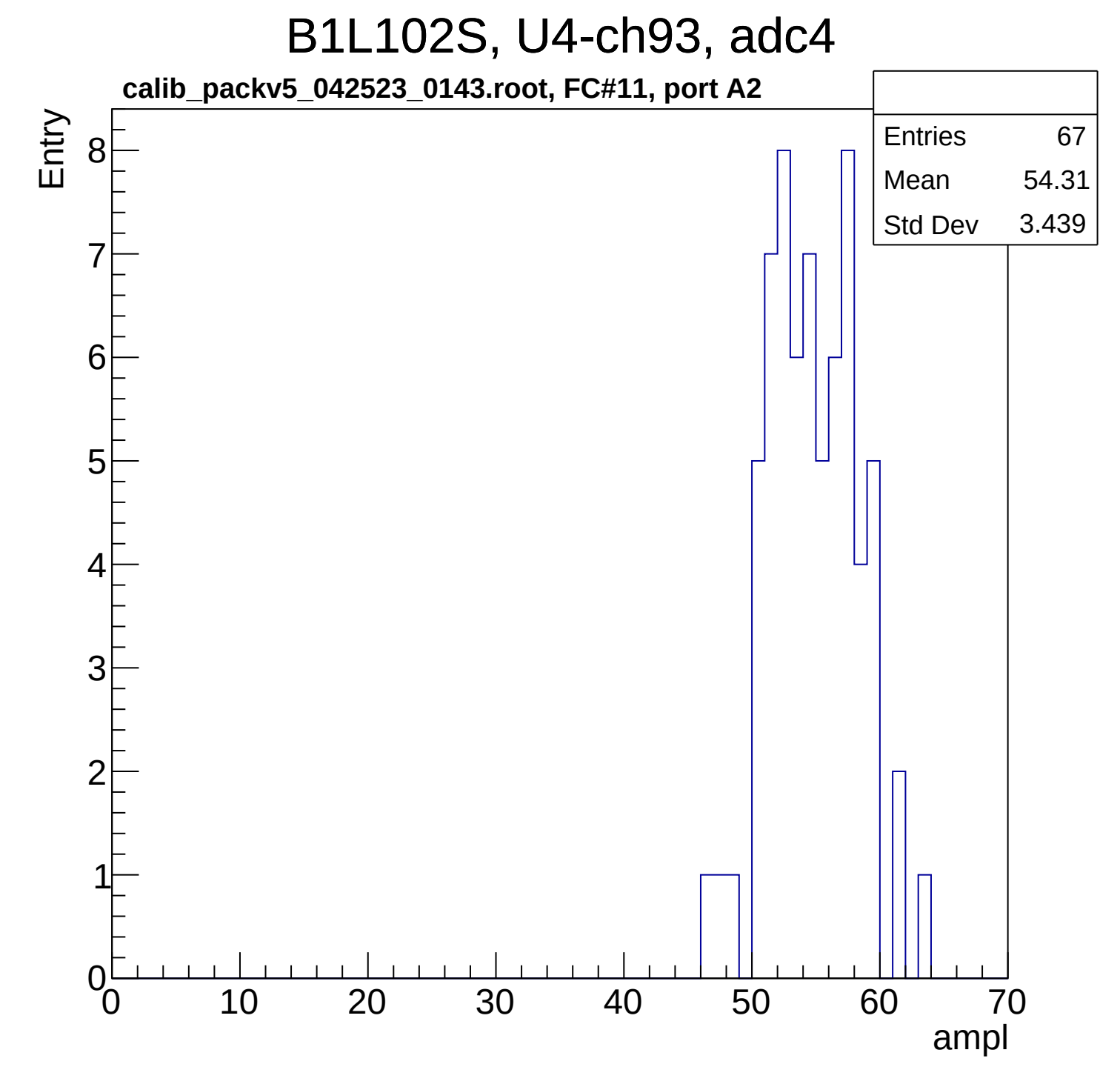
B1L102S, U4-ch93, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 54.31
Std Dev 3.439
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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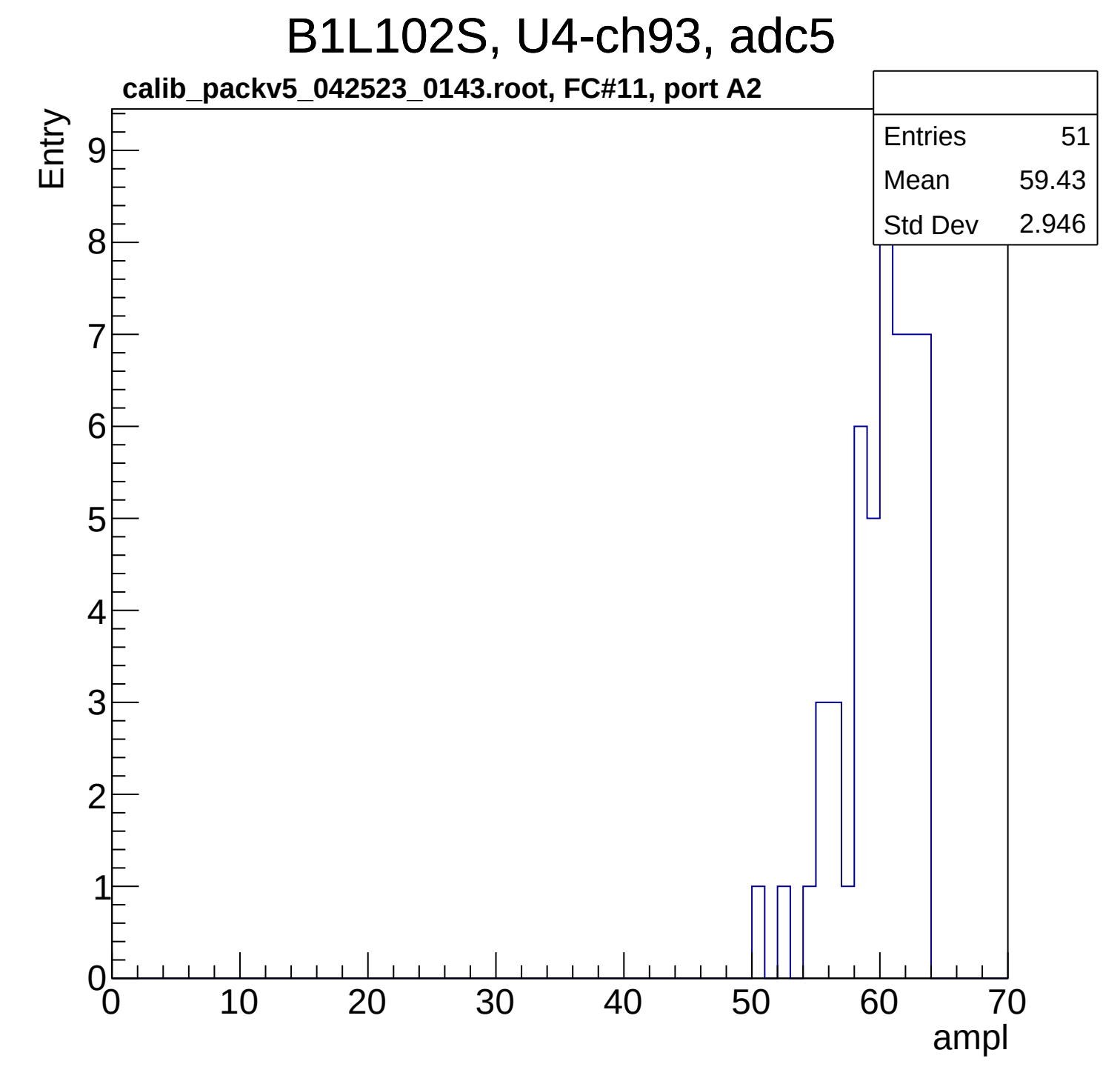
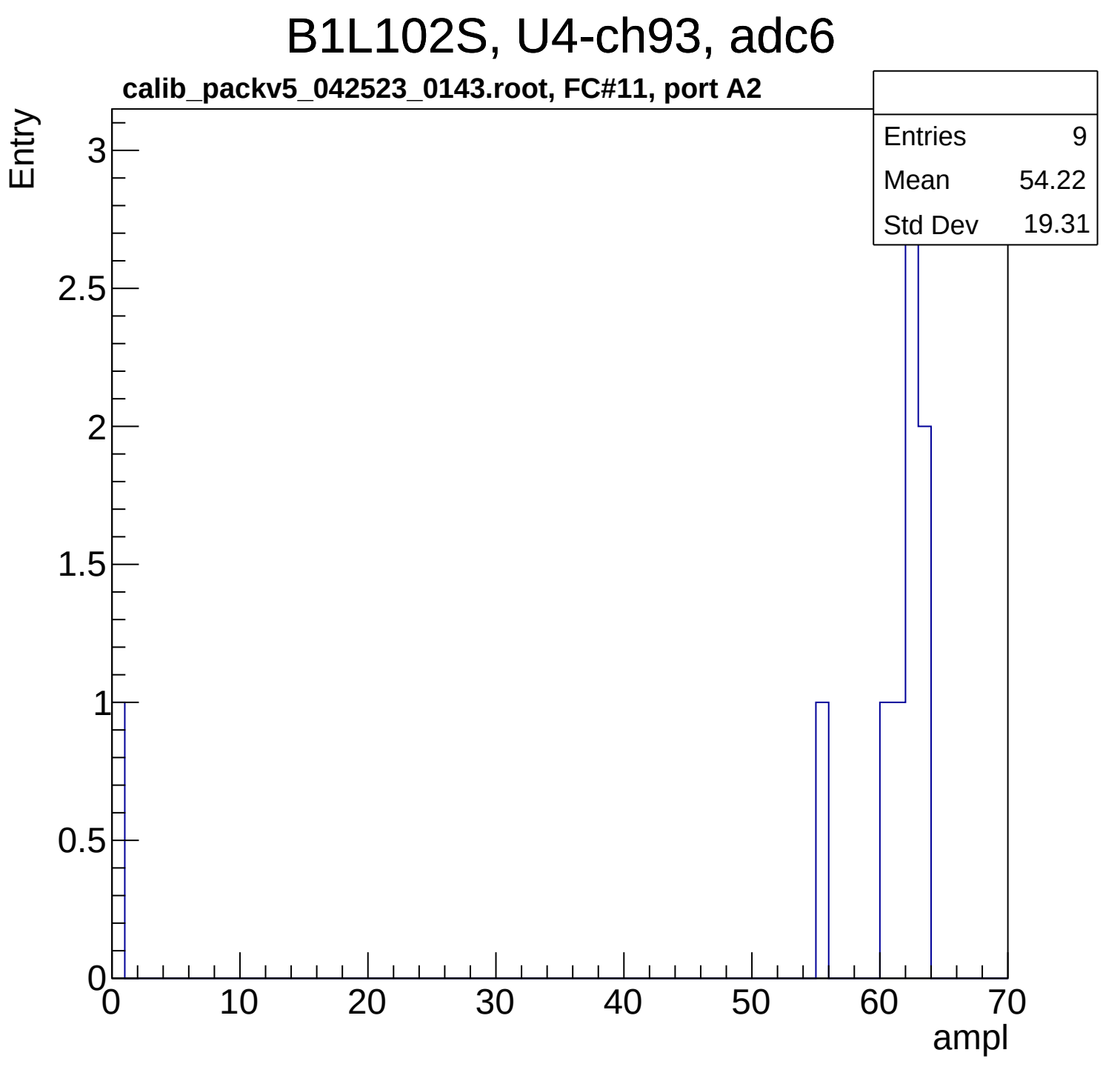

B1L102S, U4-ch93, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 59.43
Std Dev 2.946
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch93, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 9
Mean 54.22
Std Dev 19.31
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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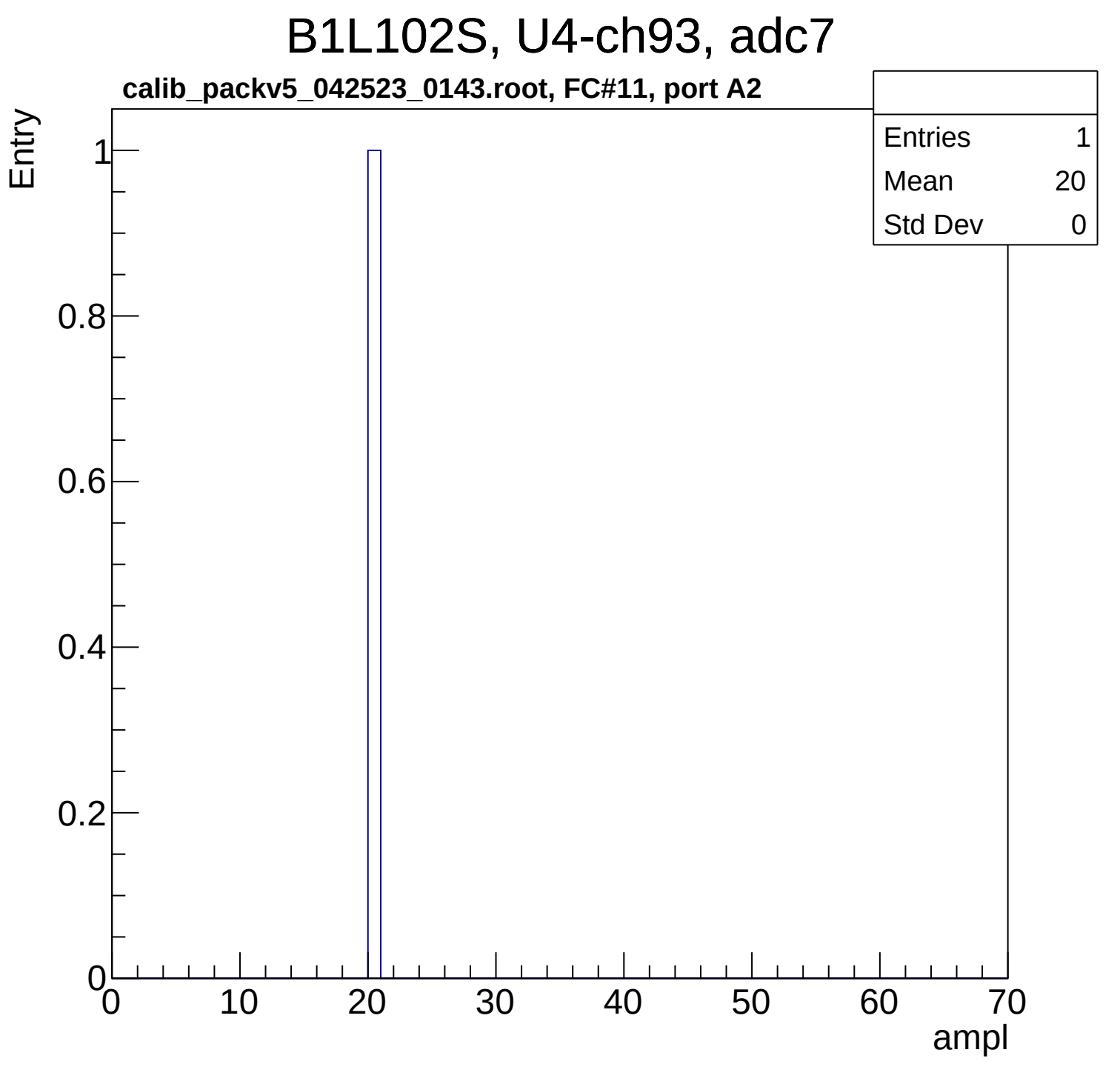
40
50
60
70


B1L102S, U4-ch93, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 20
Std Dev 0
Entry
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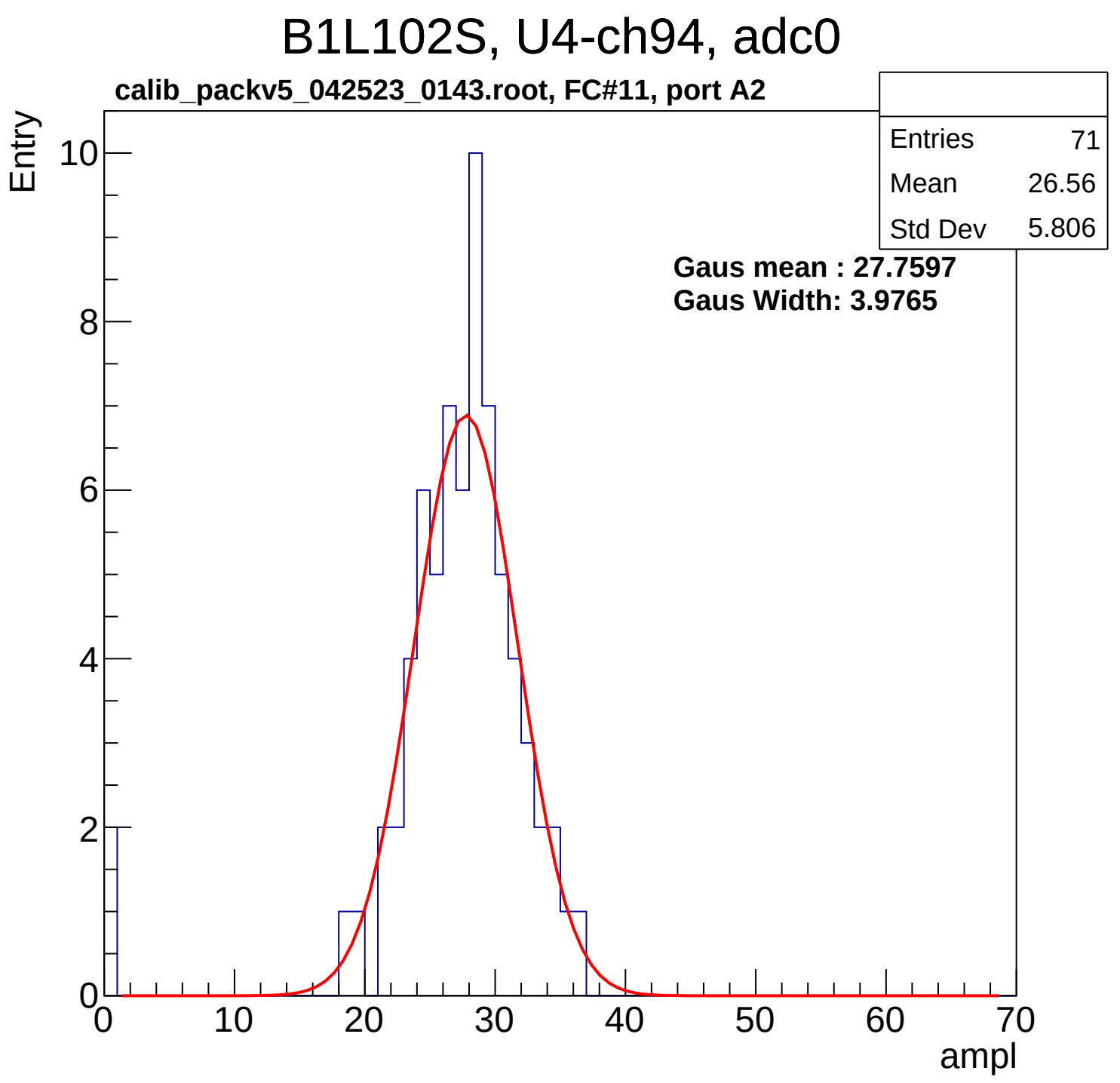
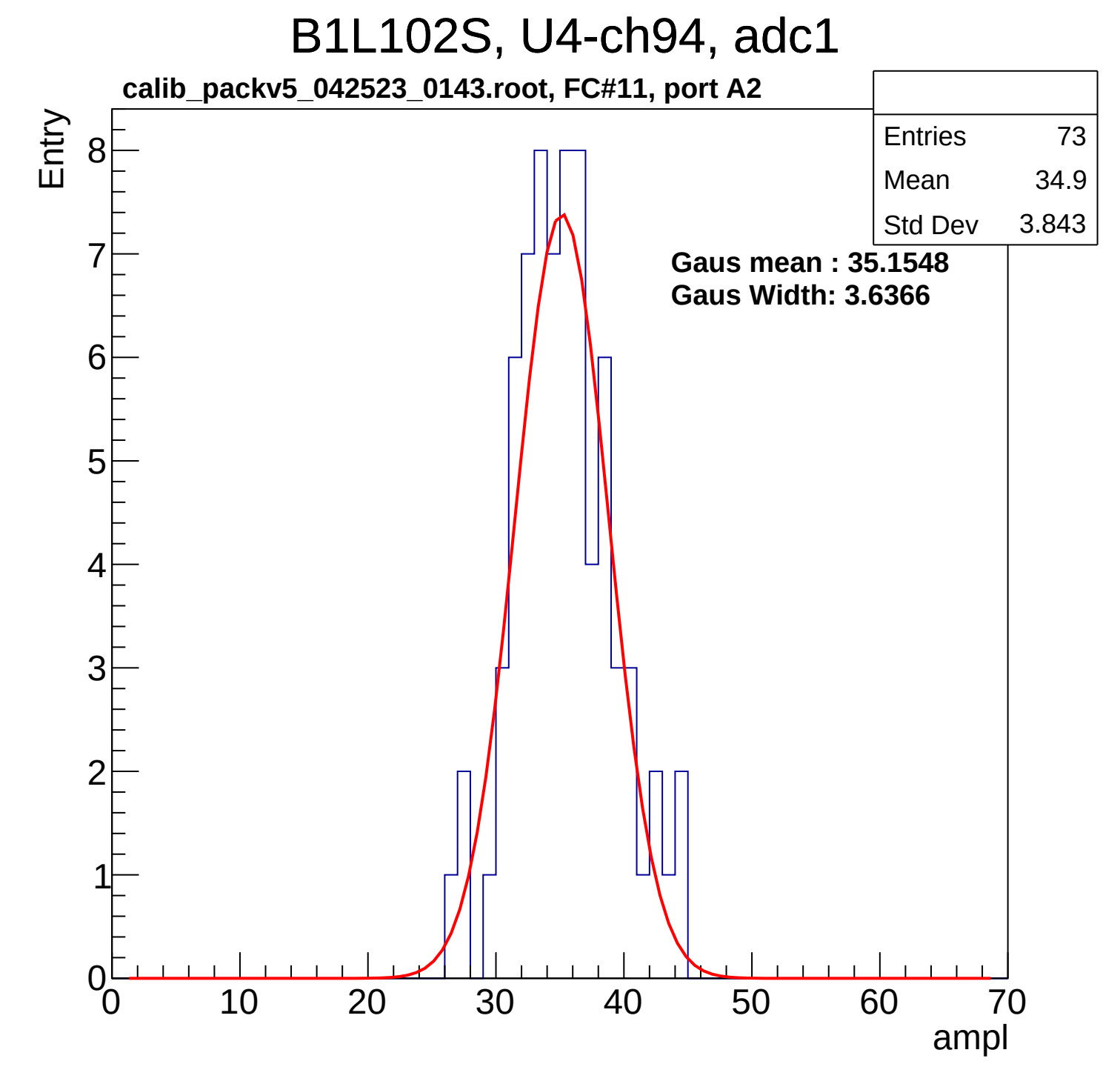
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch94, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 26.56
Std Dev 5.806
Gaus mean : 27.7597
Gaus Width: 3.9765
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch94, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 34.9
Std Dev 3.843
Gaus mean : 35.1548
Gaus Width: 3.6366
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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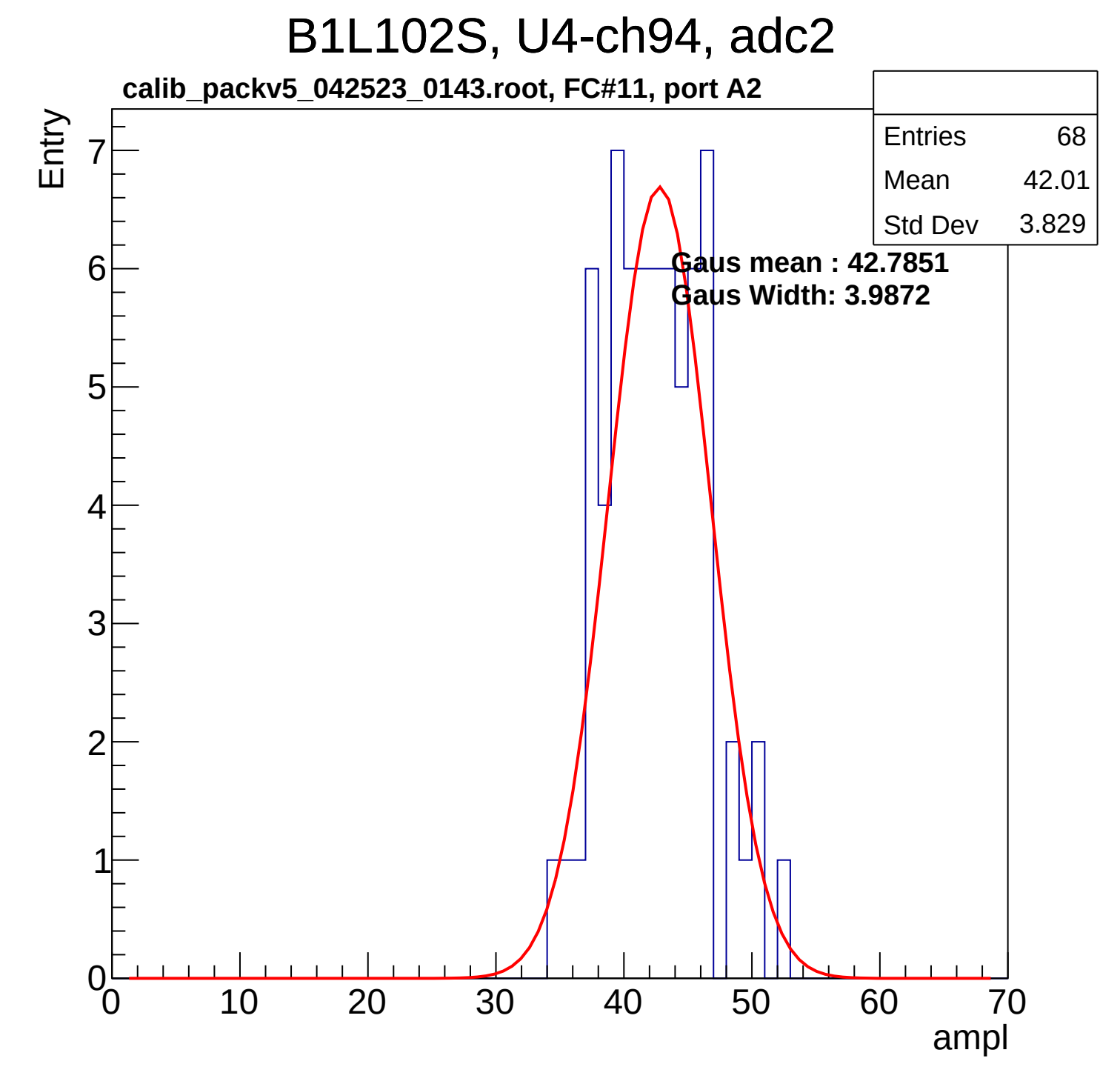
B1L102S, U4-ch94, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 42.01
Std Dev 3.829
Gaus mean : 42.7851
Gaus Width: 3.9872
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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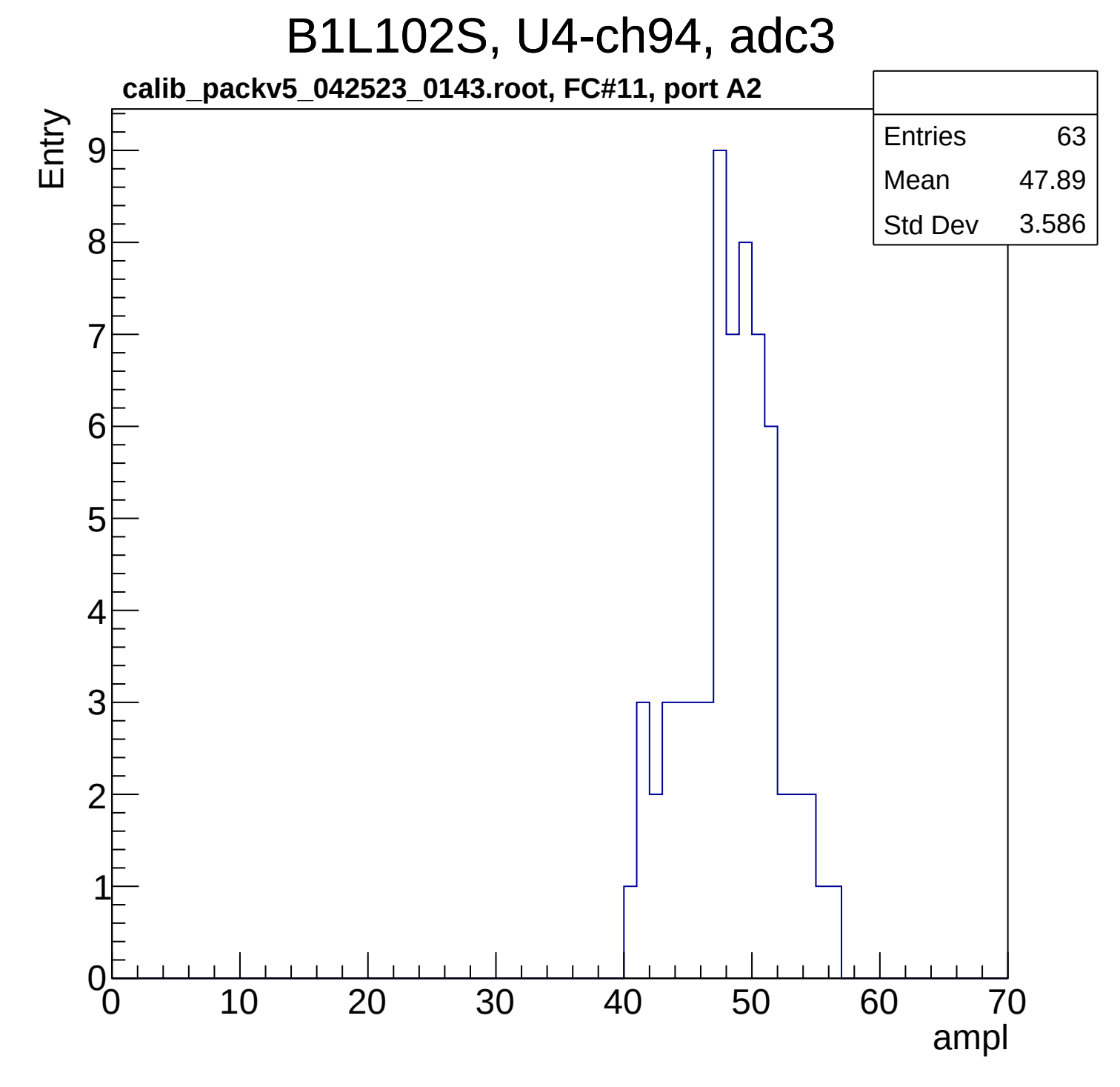
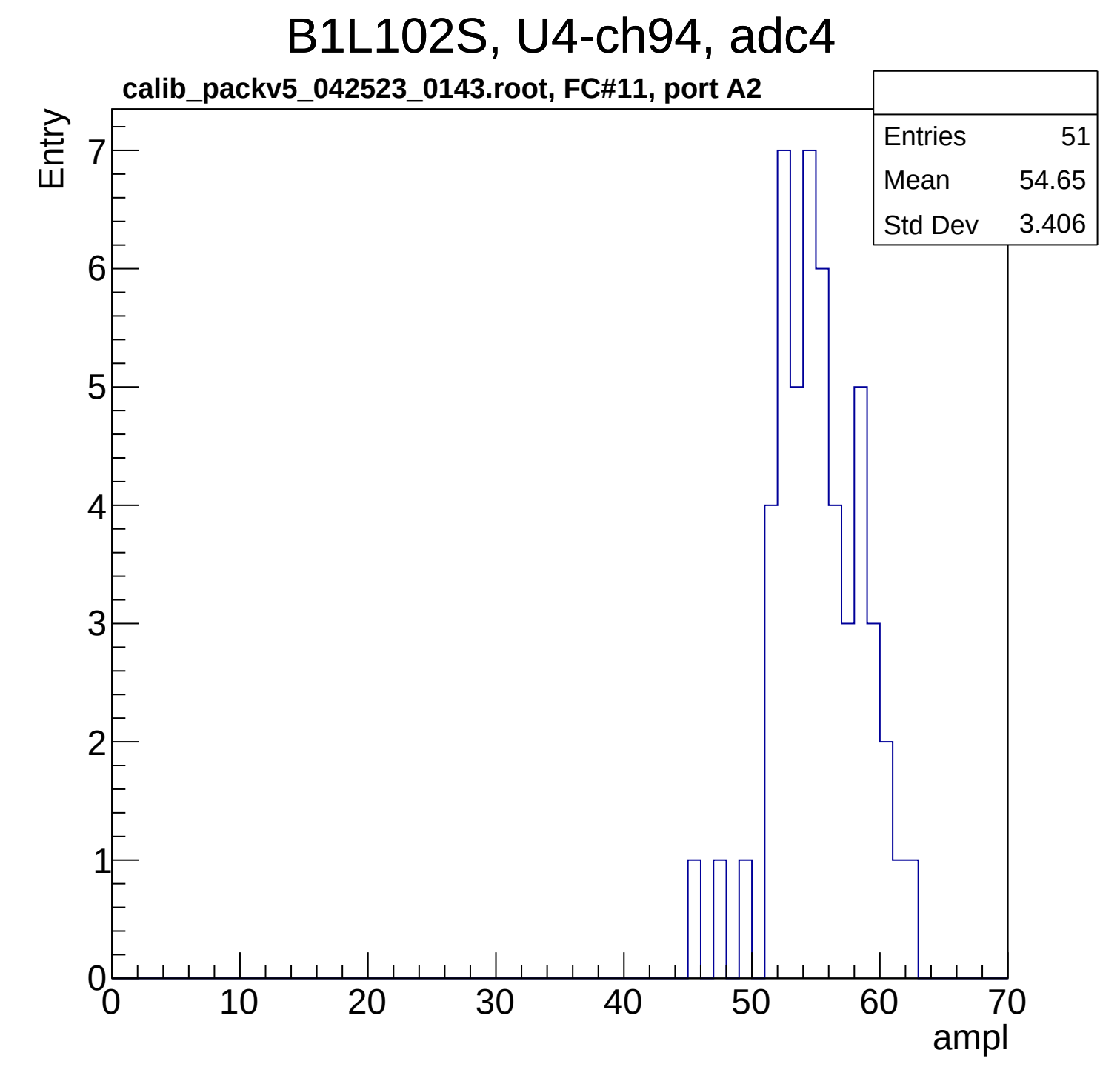
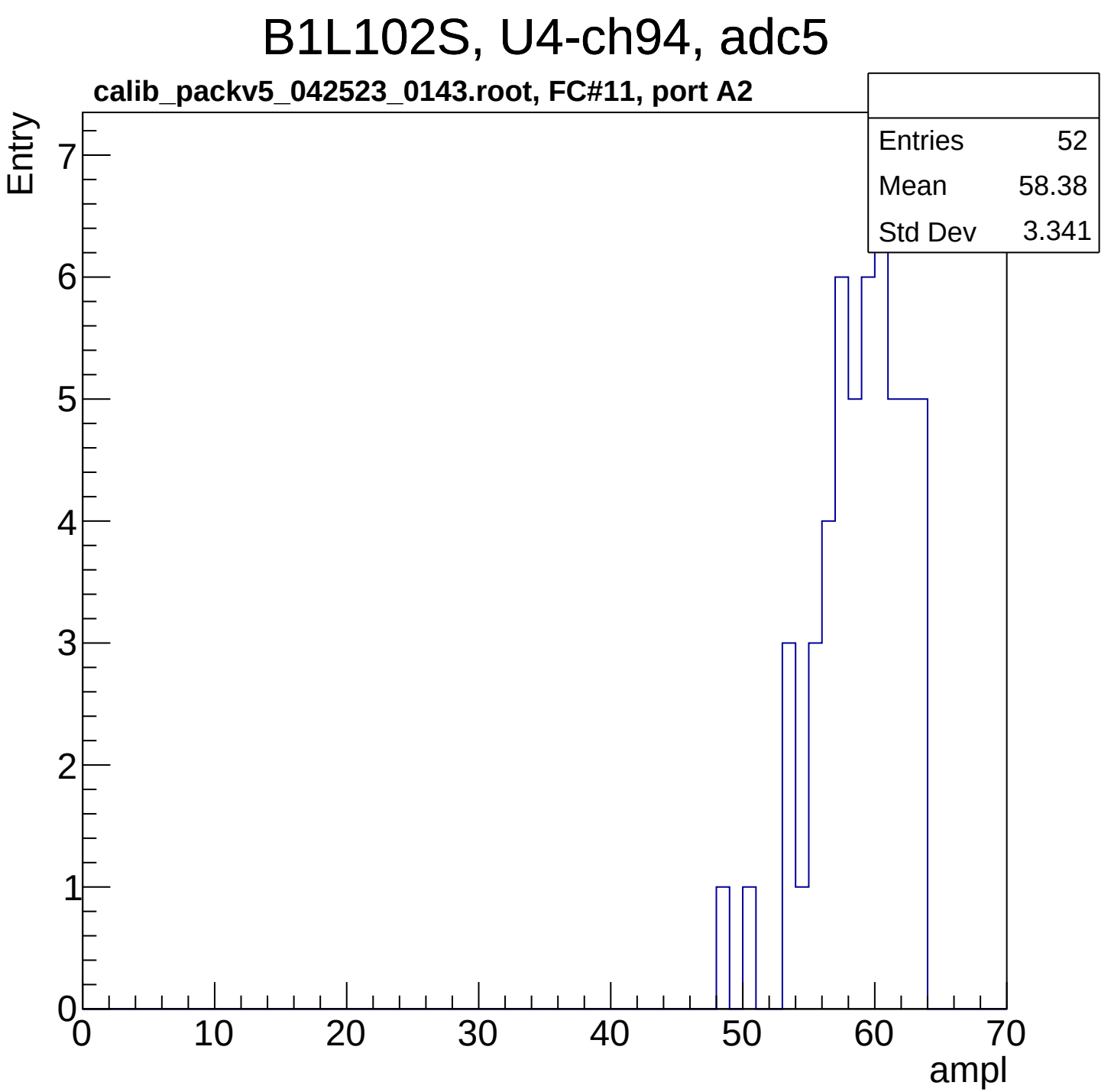

B1L102S, U4-ch94, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 47.89
Std Dev 3.586
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch94, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 54.65
Std Dev 3.406
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch94, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 52
Mean 58.38
Std Dev 3.341
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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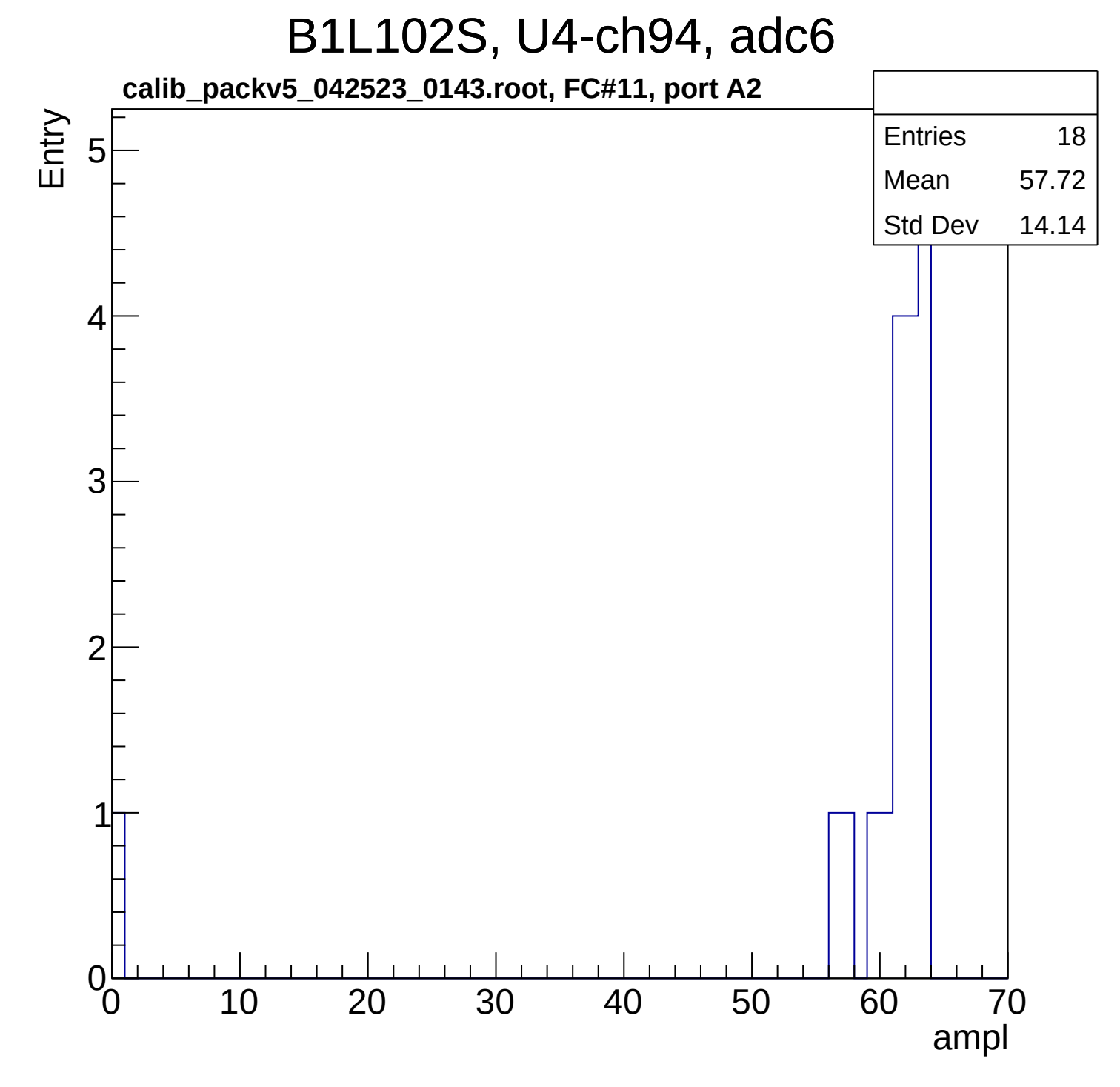
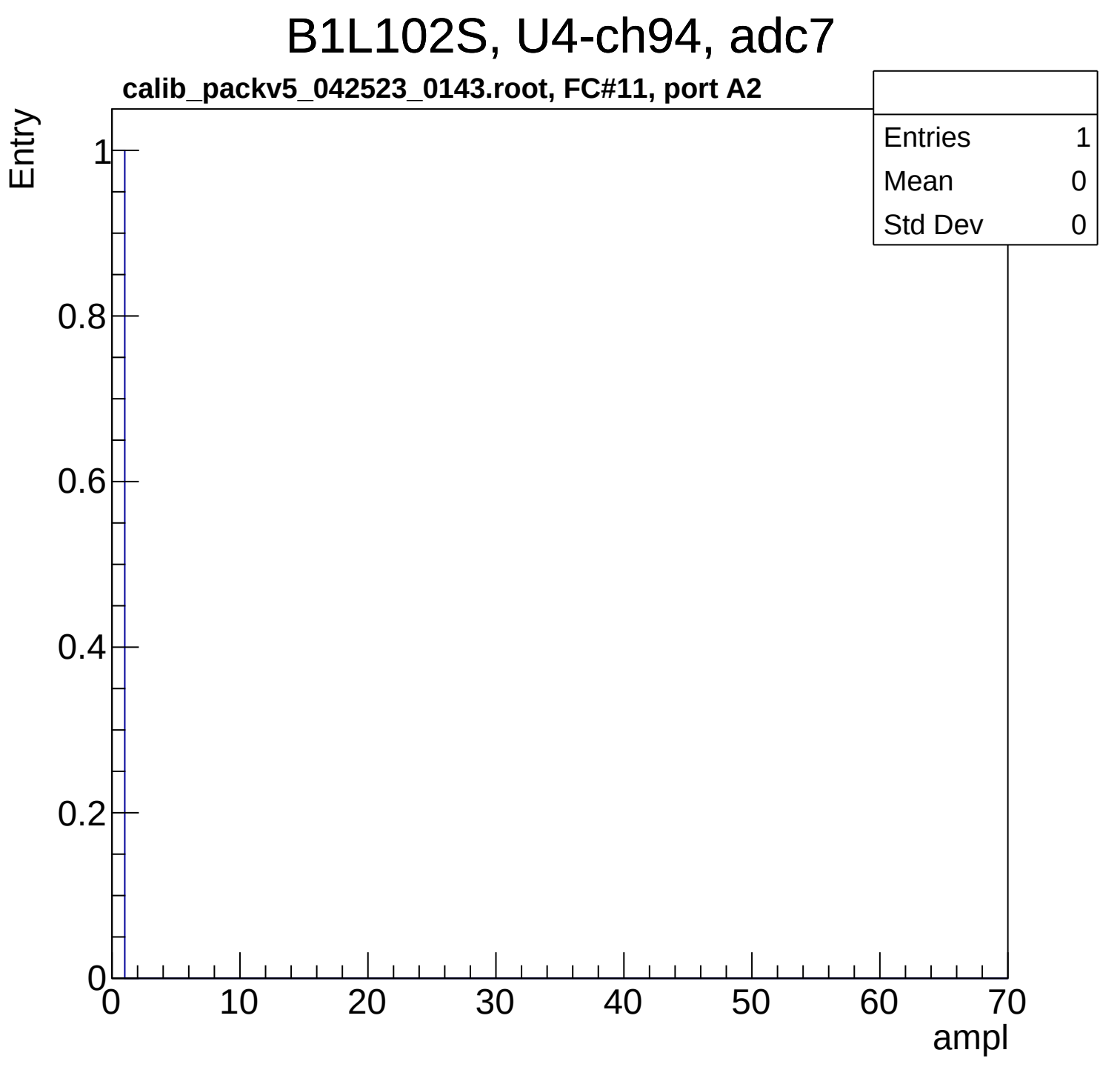
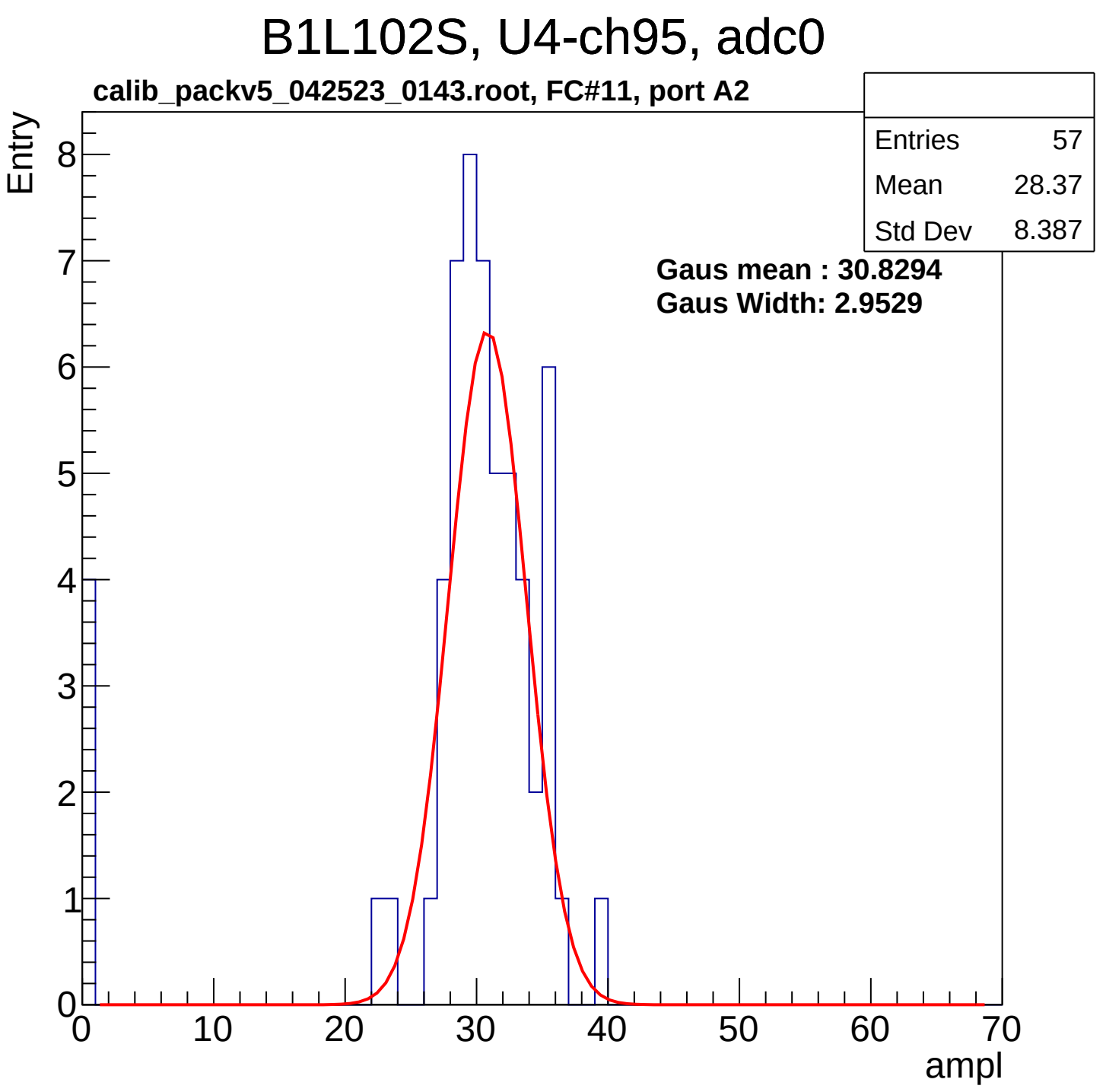
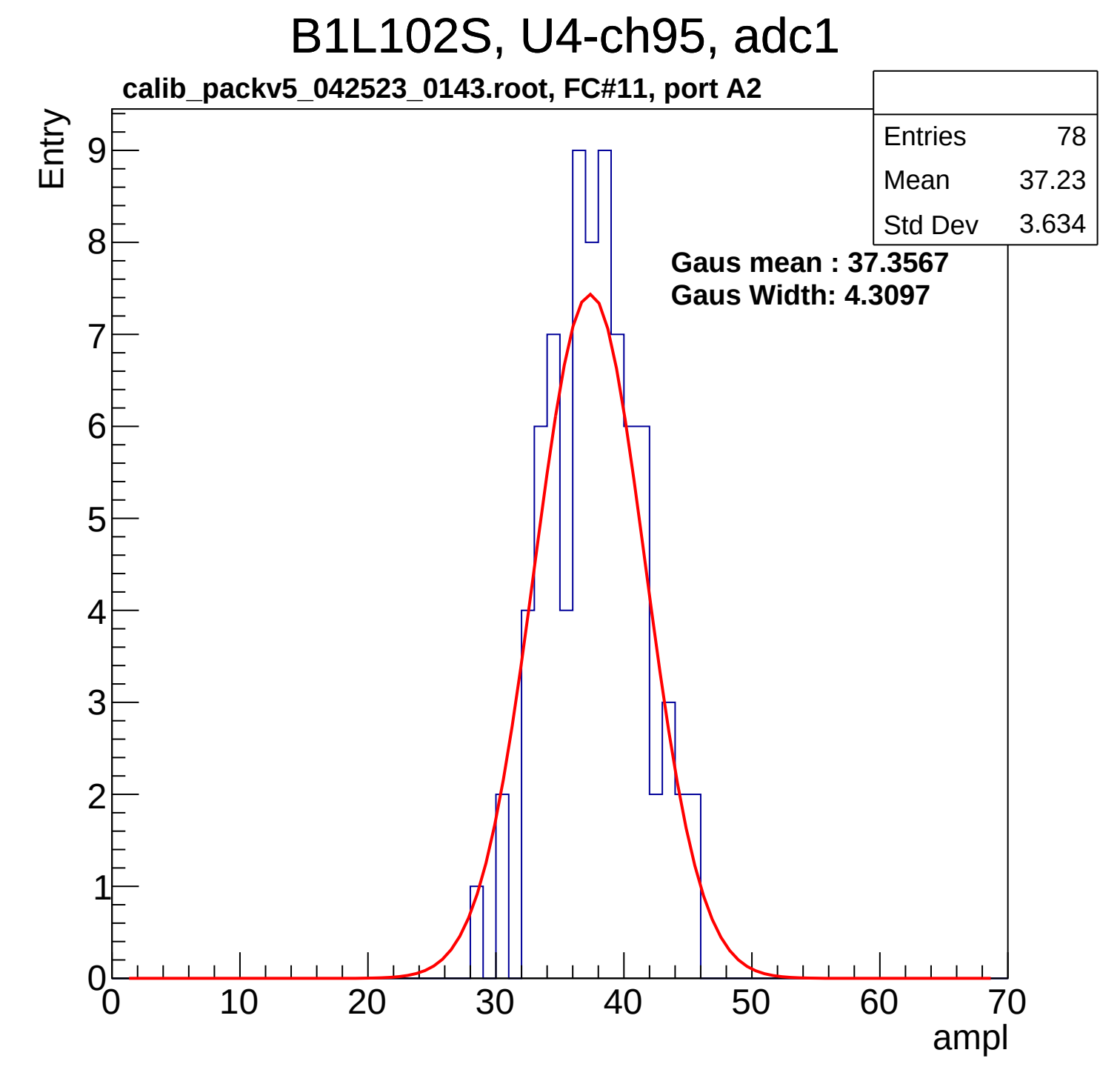
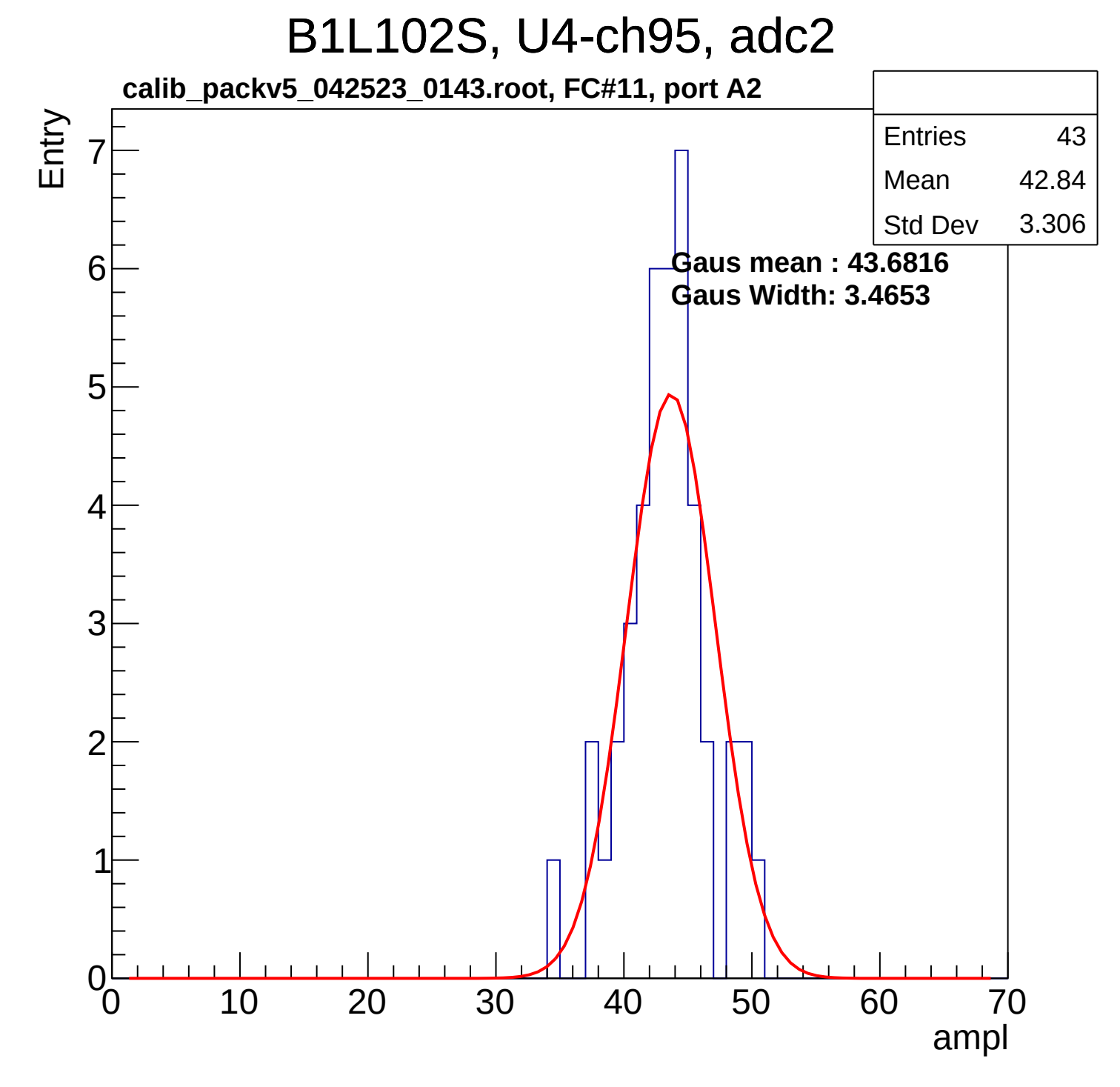
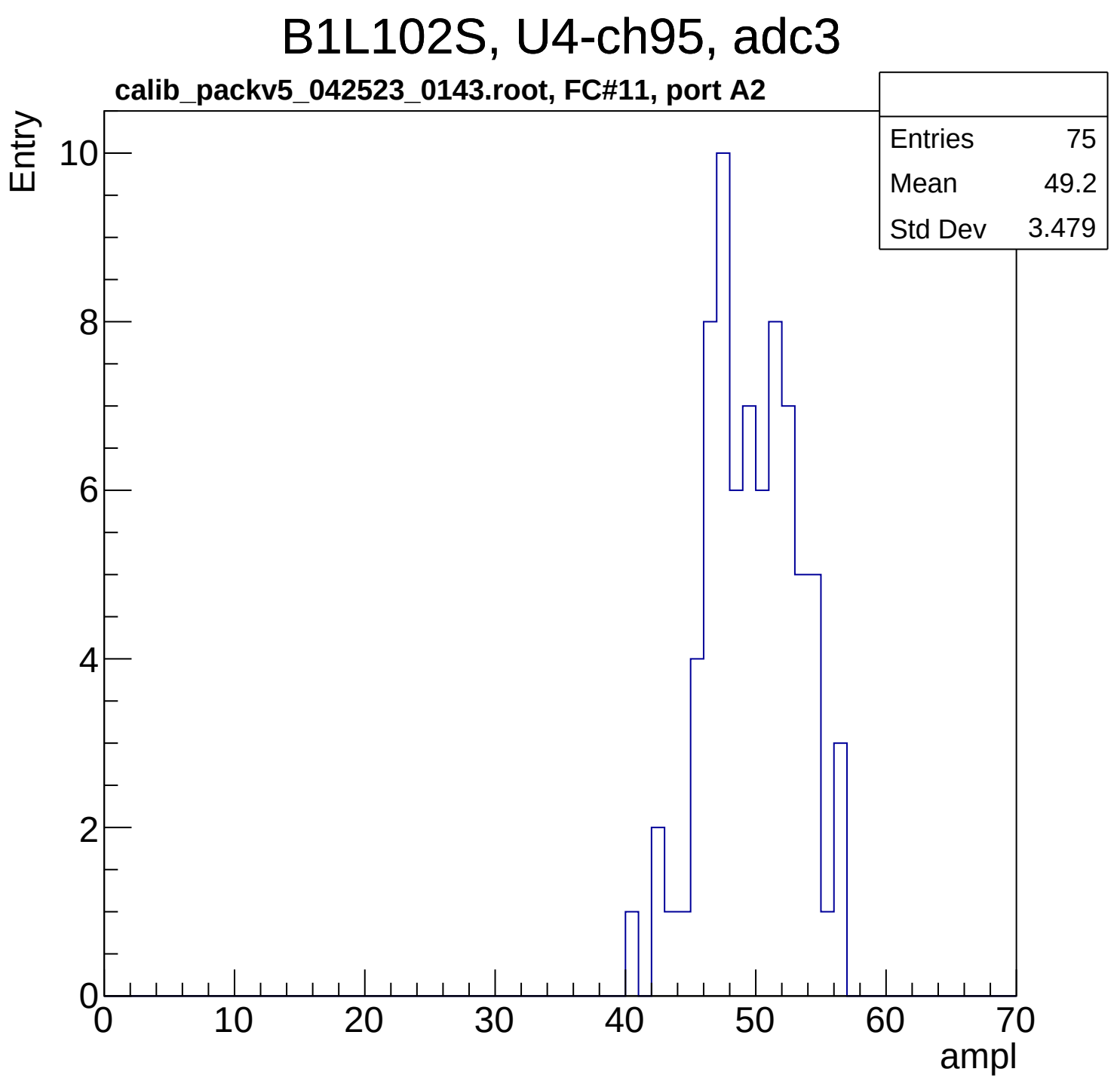

B1L102S, U4-ch94, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 18
Mean 57.72
Std Dev 14.14
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

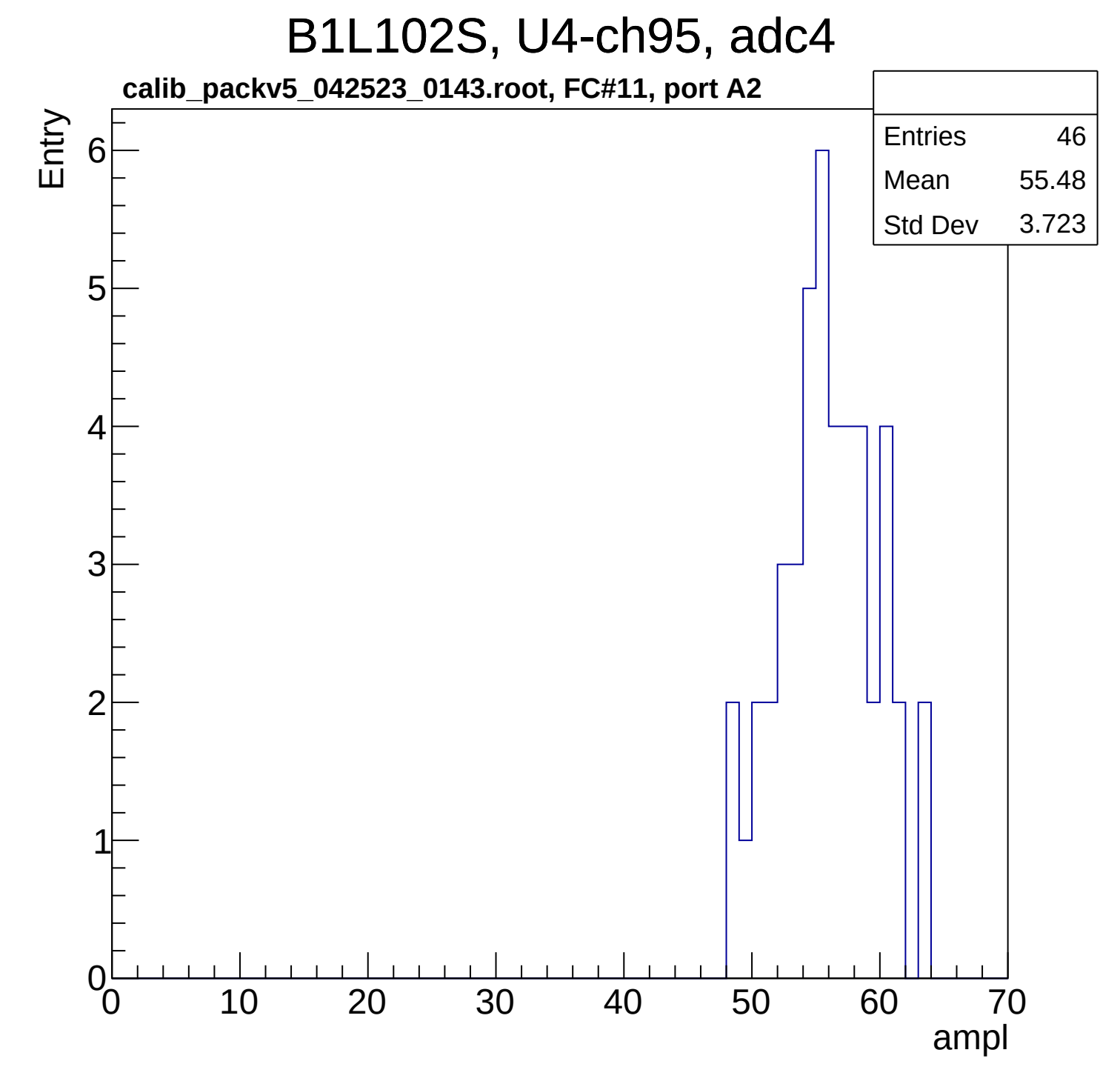

B1L102S, U4-ch94, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch95, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 57
Mean 28.37
Std Dev 8.387
Gaus mean : 30.8294
Gaus Width: 2.9529
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch95, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 78
Mean 37.23
Std Dev 3.634
Gaus mean : 37.3567
Gaus Width: 4.3097
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch95, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 43
Mean 42.84
Std Dev 3.306
Gaus mean : 43.6816
Gaus Width: 3.4653
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch95, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 49.2
Std Dev 3.479
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch95, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 46
Mean 55.48
Std Dev 3.723
Entry
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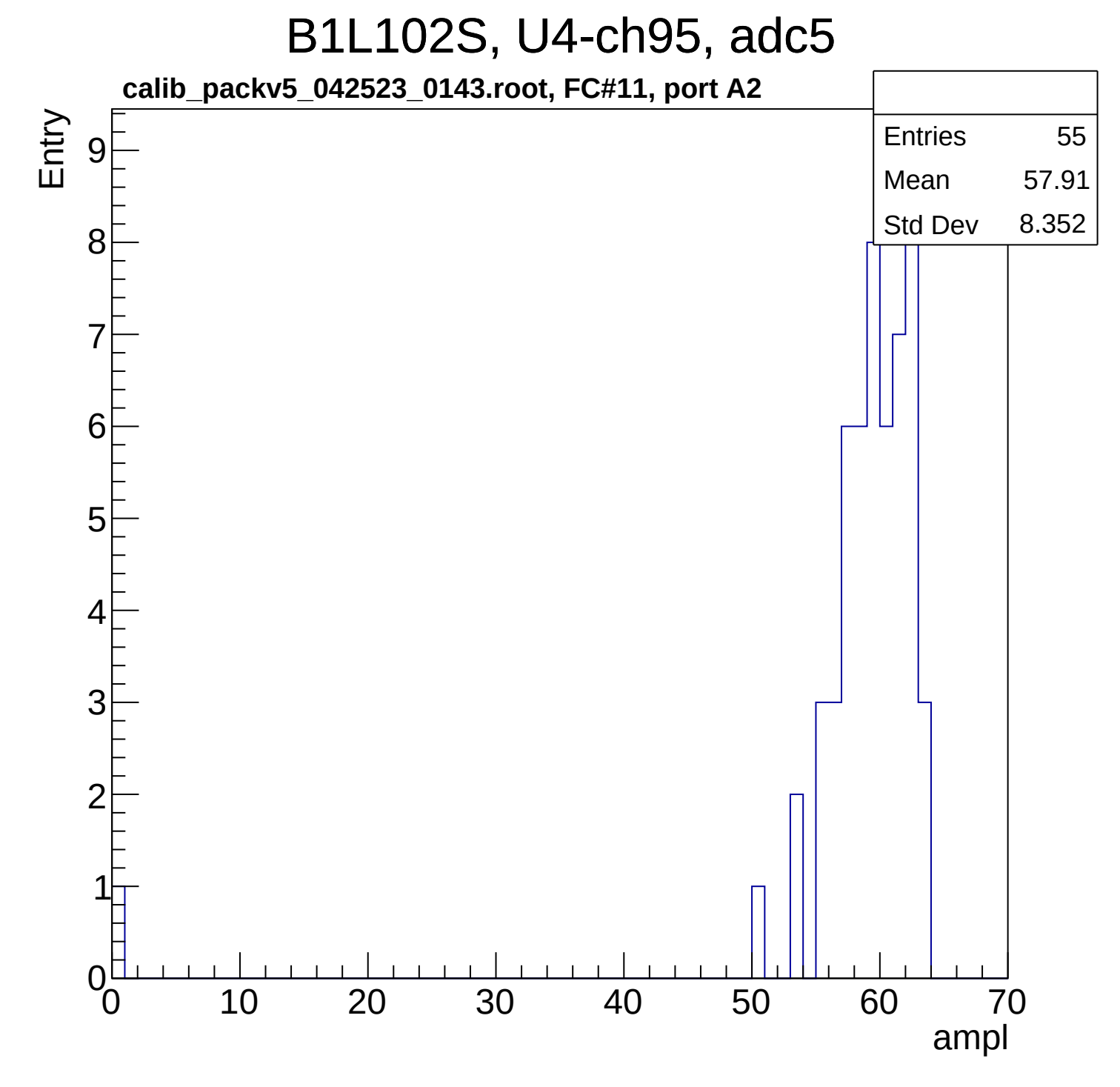
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch95, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 57.91
Std Dev 8.352
Entry
ampl
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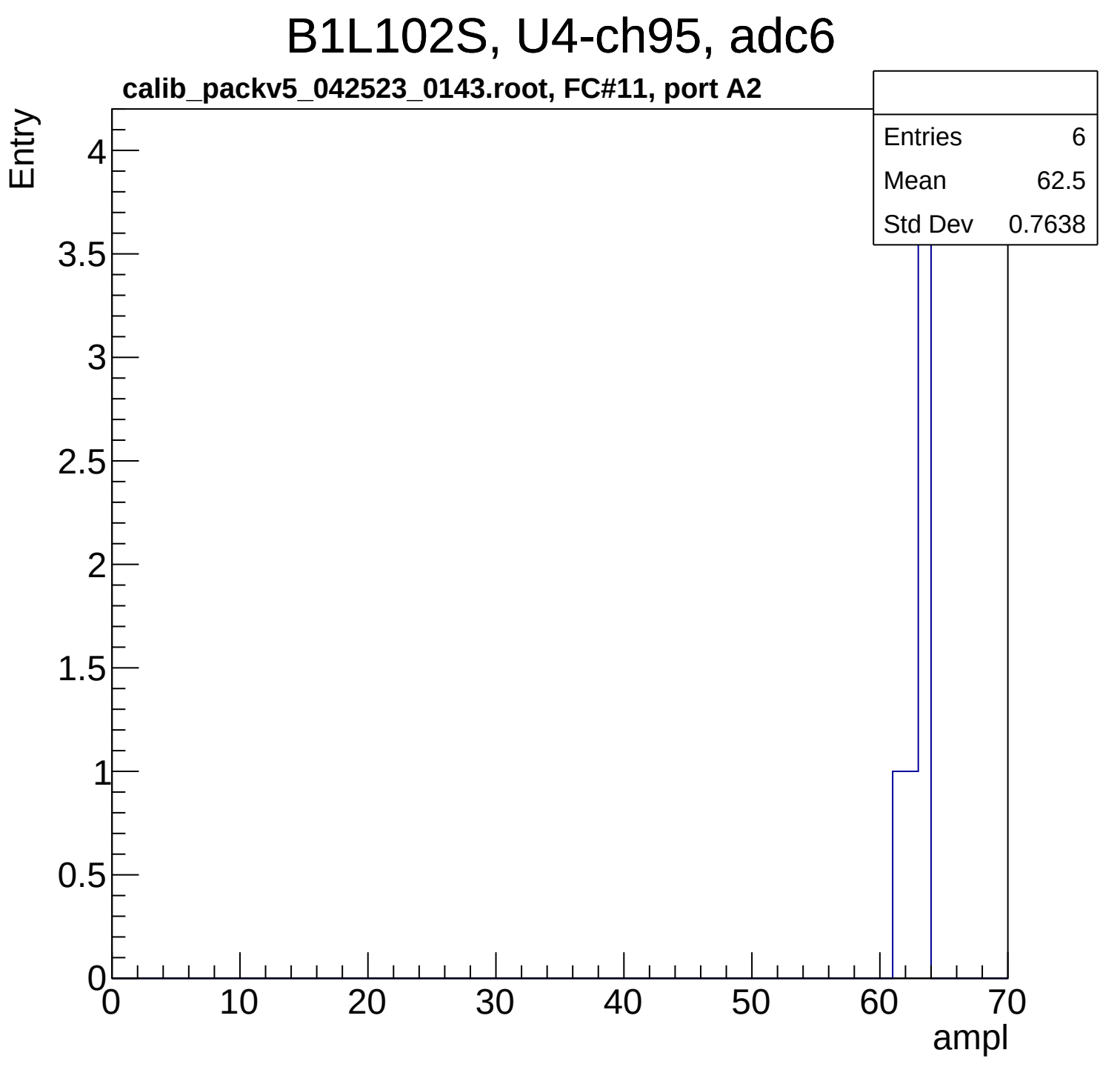
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch95, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 6
Mean 62.5
Std Dev 0.7638
Entry
ampl
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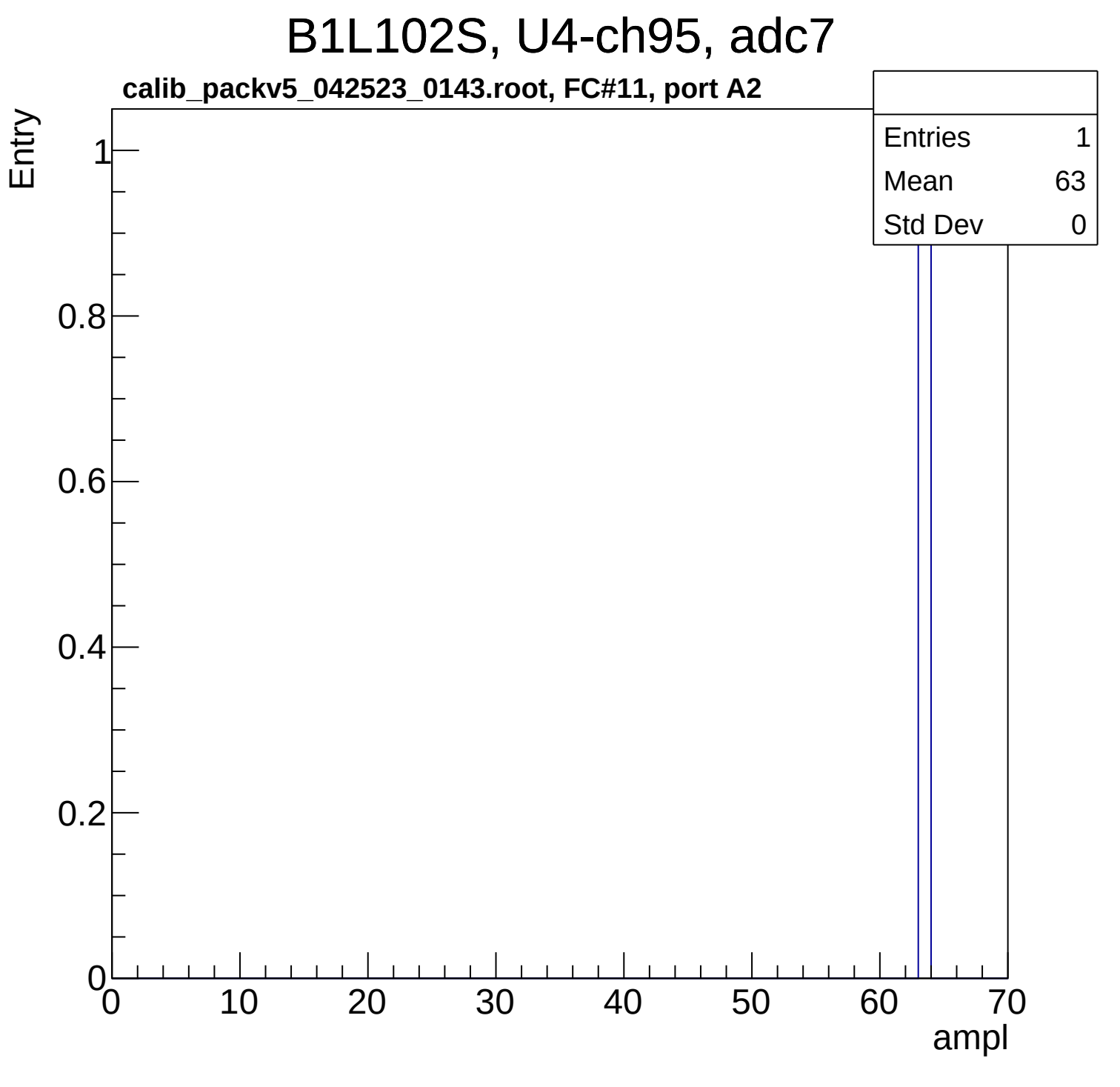
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U4-ch95, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 63
Std Dev 0
Entry
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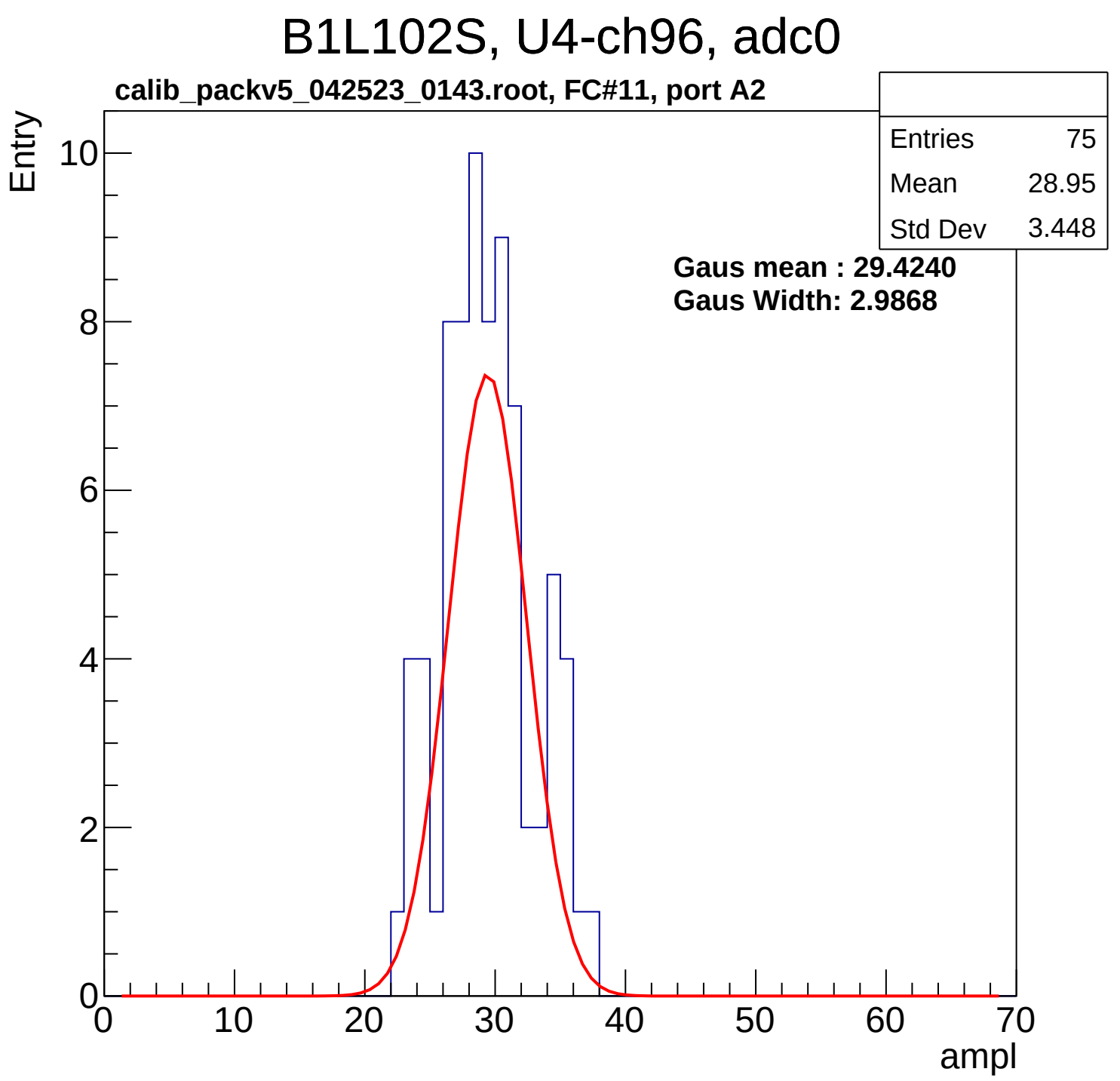
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch96, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 28.95
Std Dev 3.448
Gaus mean : 29.4240
Gaus Width: 2.9868
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
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60
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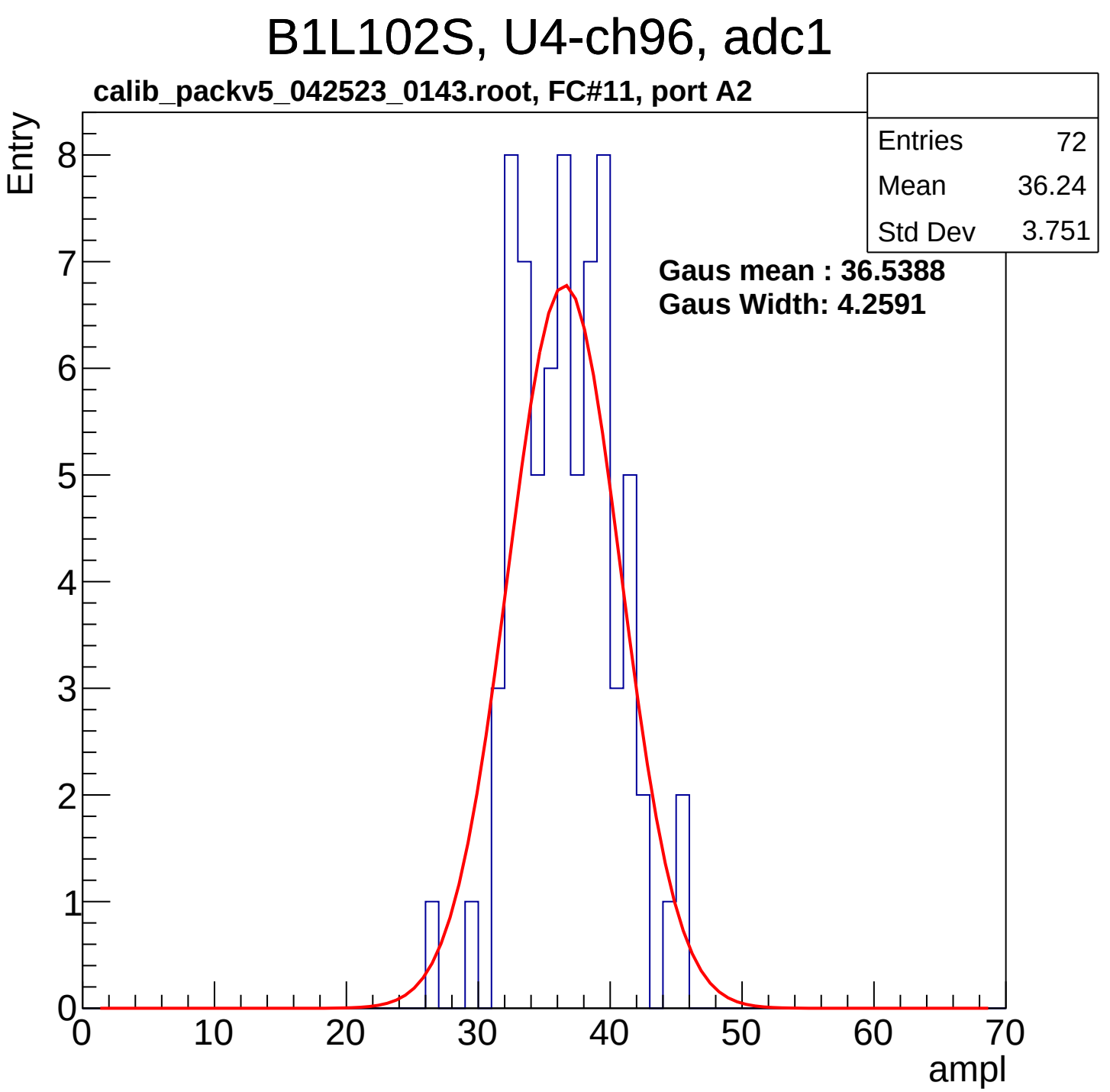
B1L102S, U4-ch96, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 72
Mean 36.24
Std Dev 3.751
Gaus mean : 36.5388
Gaus Width: 4.2591
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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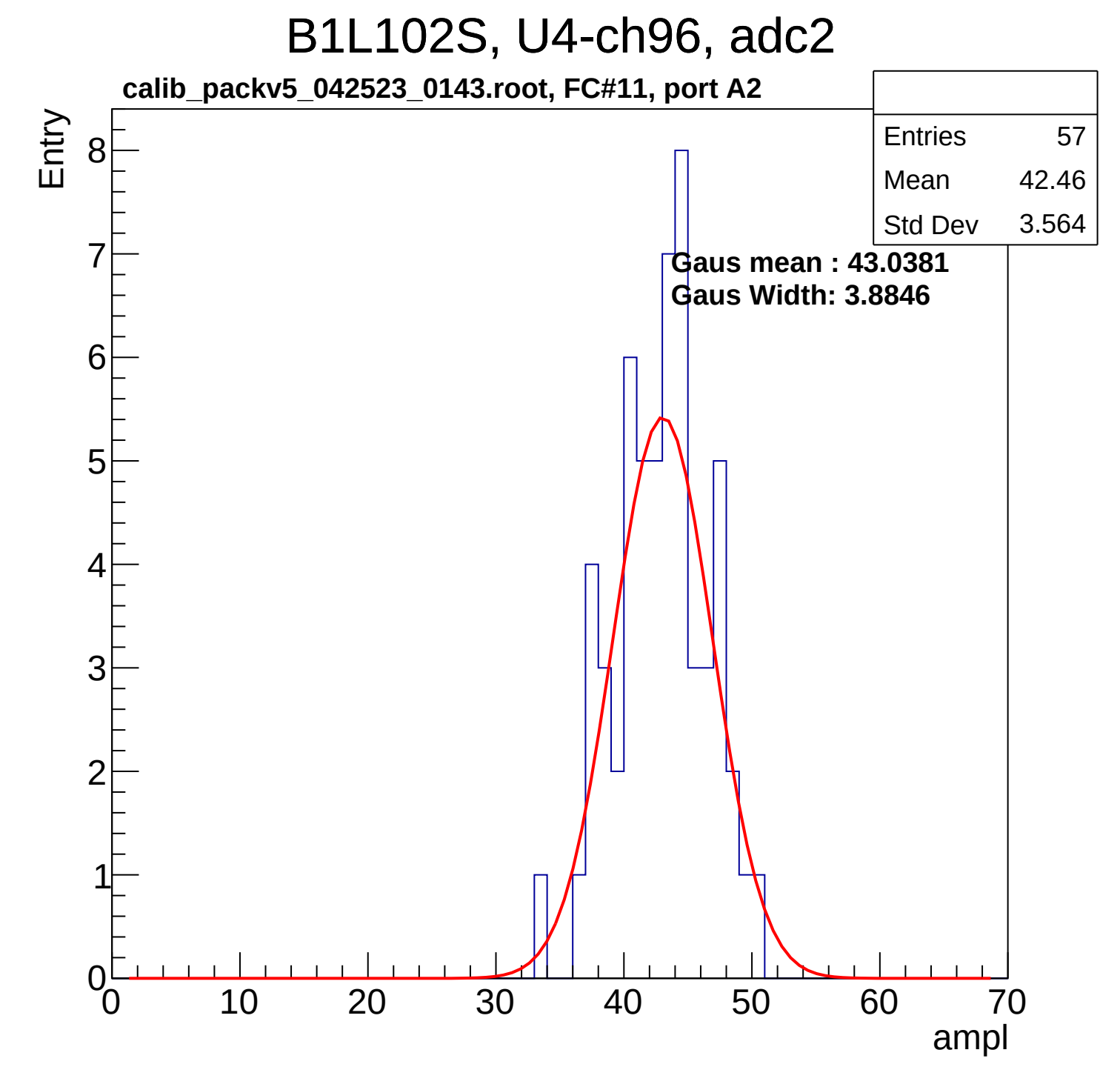
B1L102S, U4-ch96, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 57
Mean 42.46
Std Dev 3.564
Gaus mean : 43.0381
Gaus Width: 3.8846
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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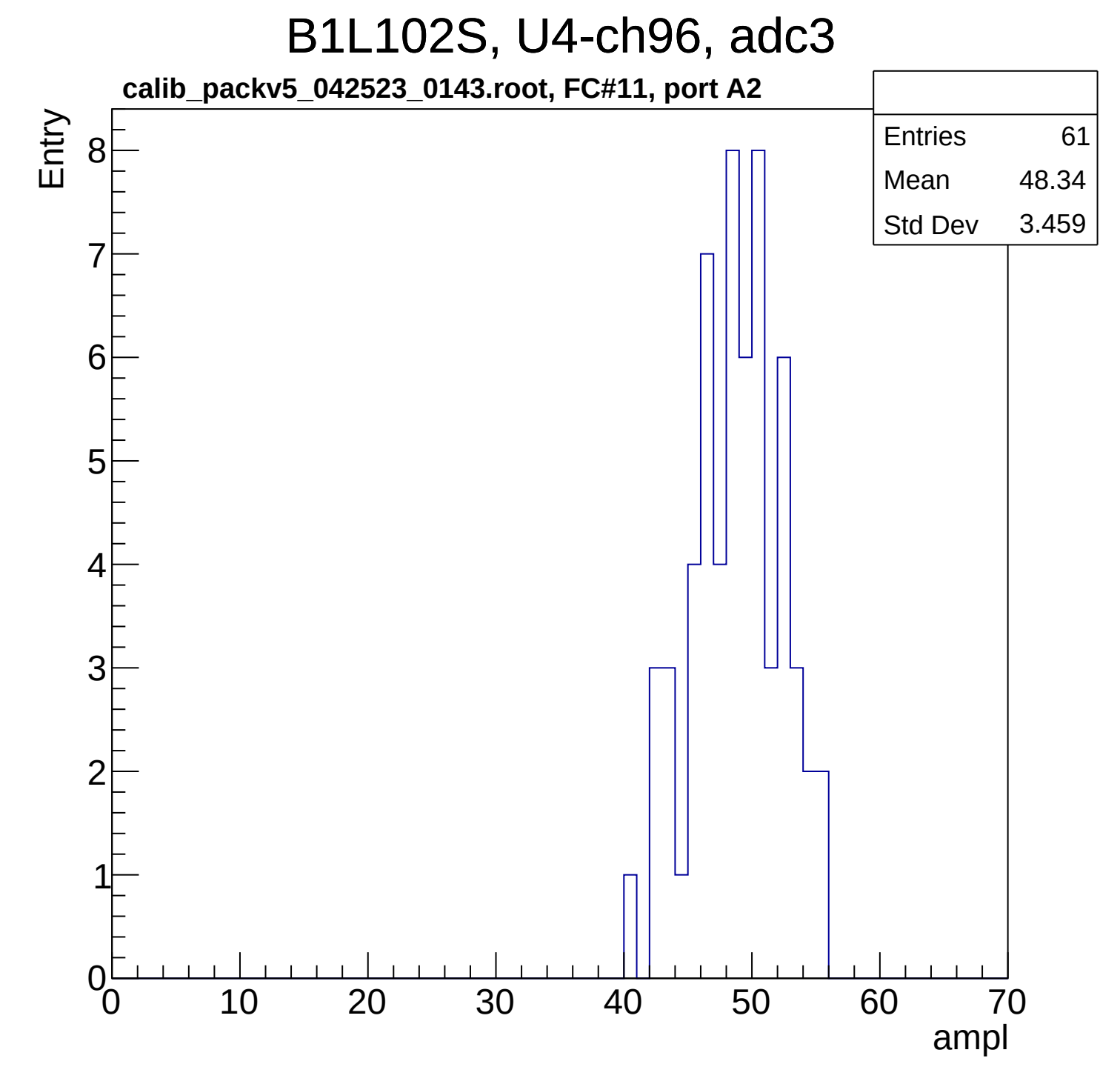
B1L102S, U4-ch96, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 48.34
Std Dev 3.459
Entry
ampl
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3
4
5
6
7
8
0
10
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60
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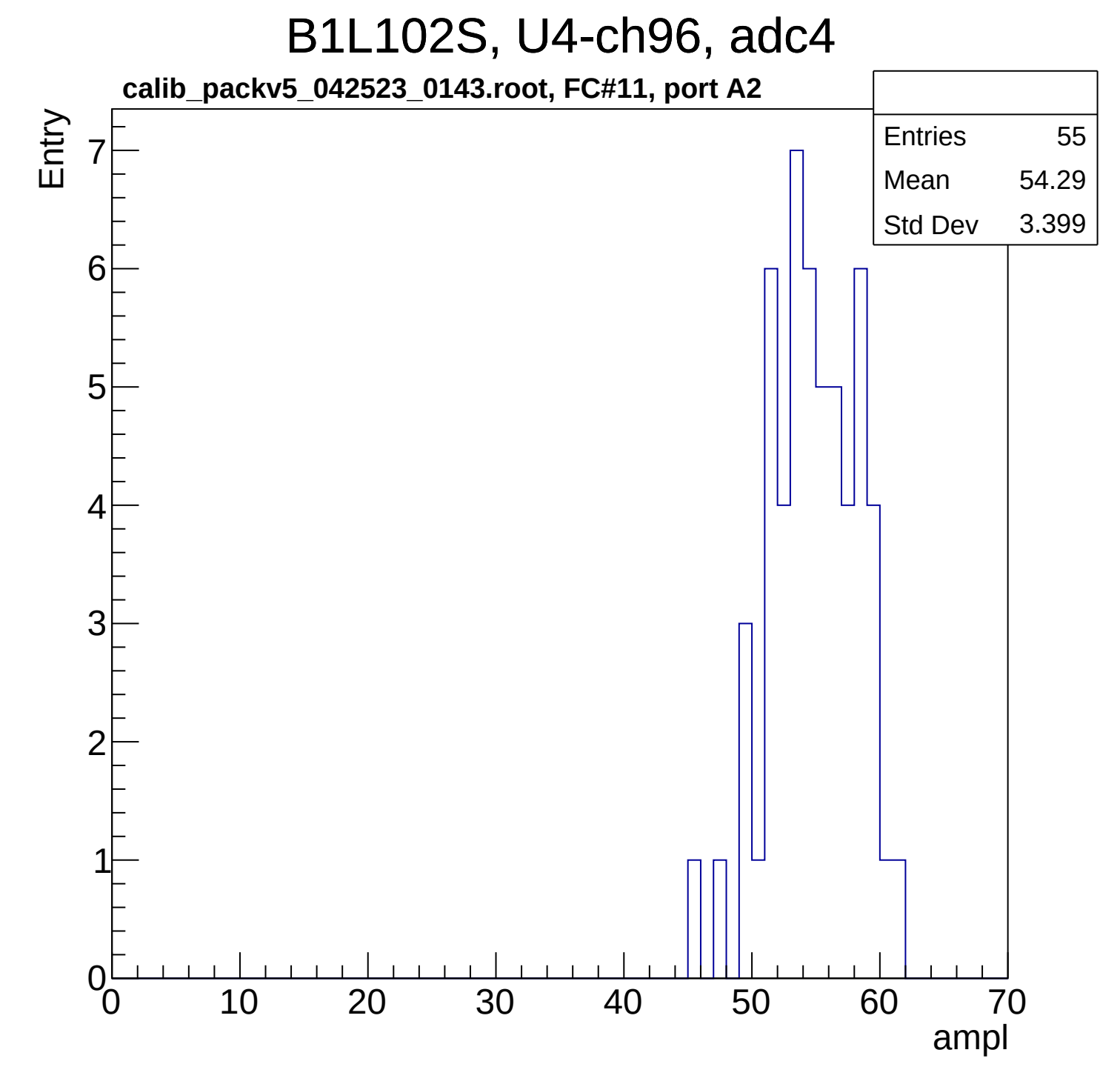
B1L102S, U4-ch96, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 54.29
Std Dev 3.399
Entry
ampl
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2
3
4
5
6
7
0
10
20
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40
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60
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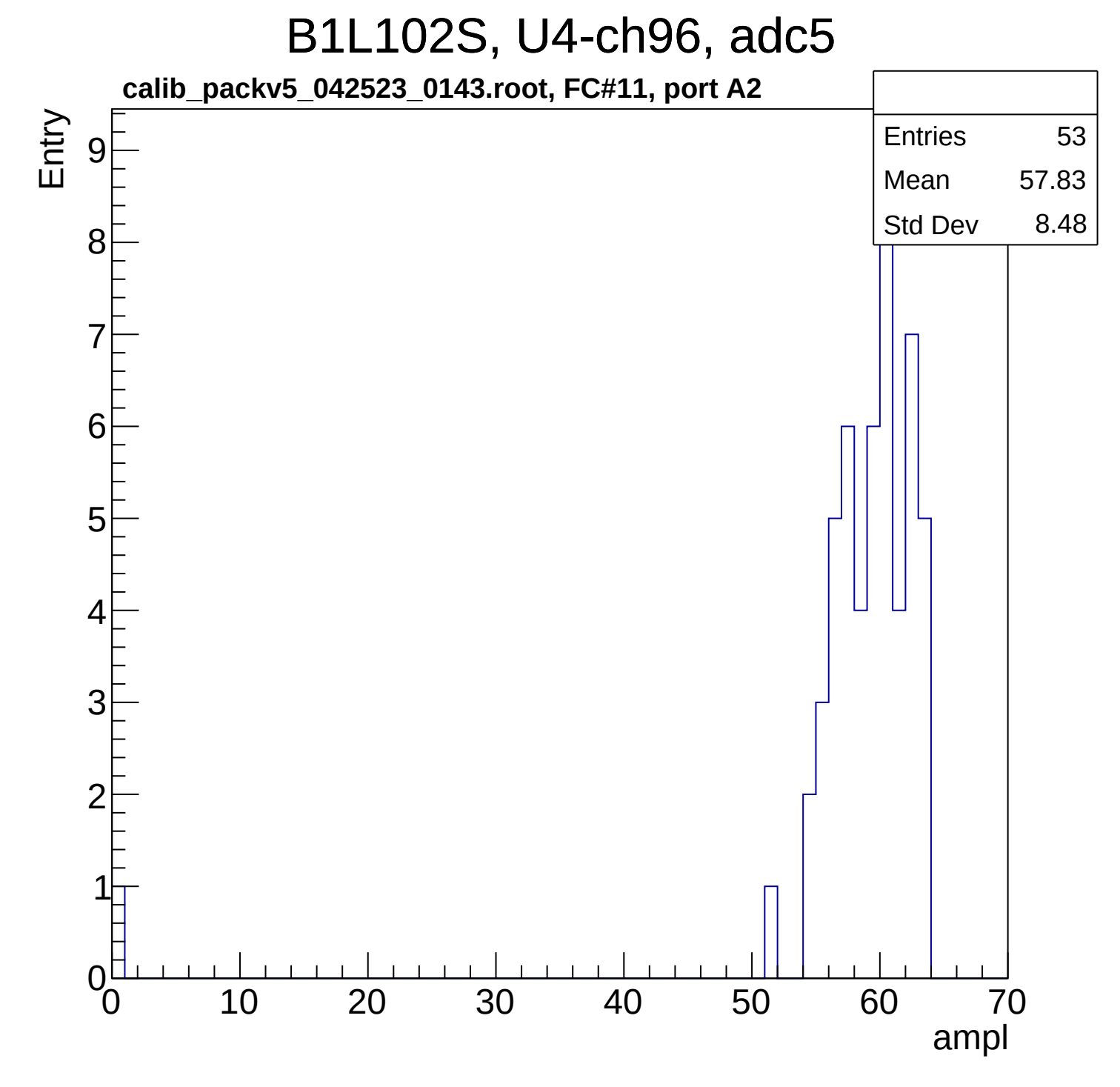
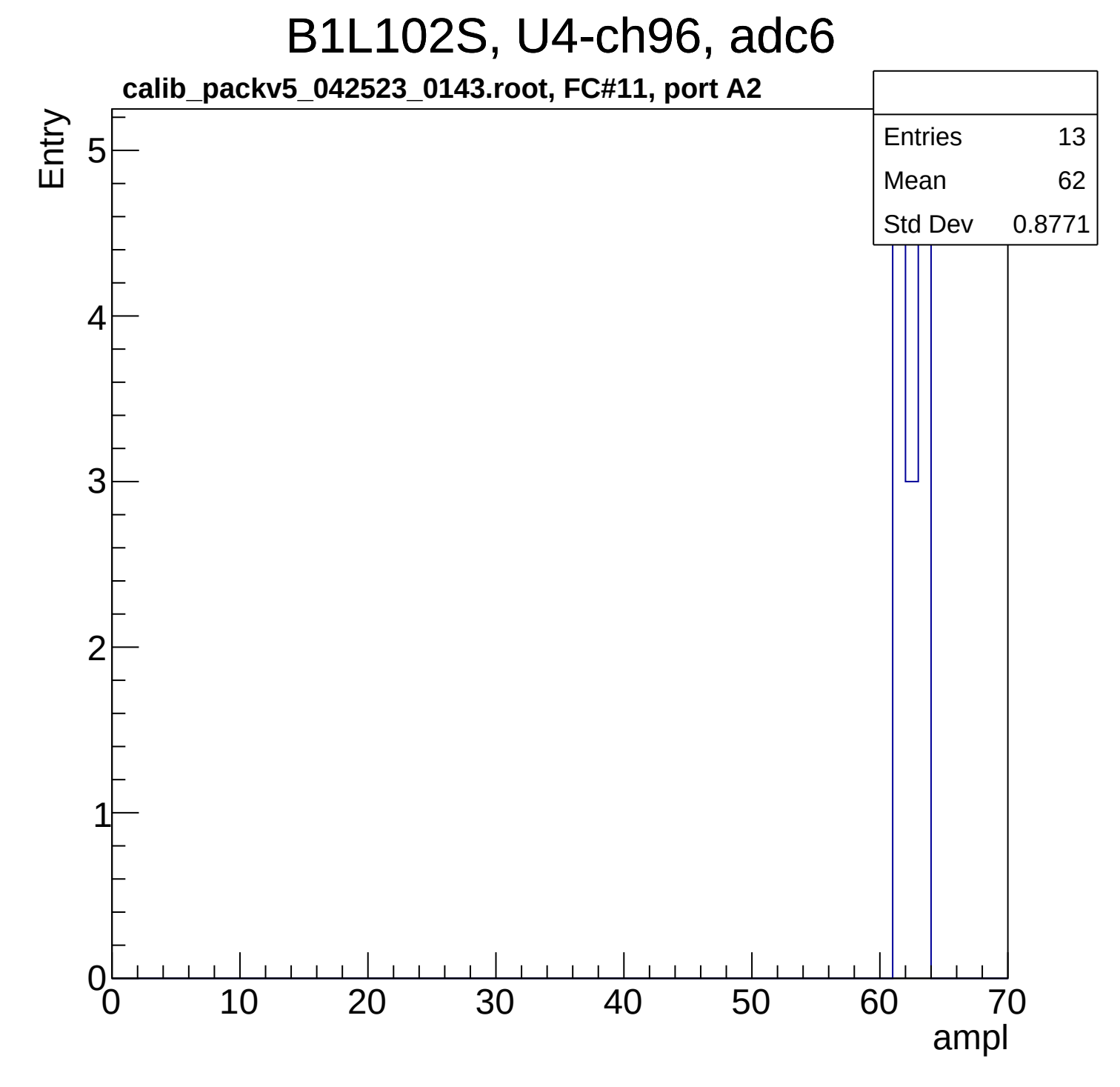

B1L102S, U4-ch96, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 57.83
Std Dev 8.48
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch96, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 13
Mean 62
Std Dev 0.8771
Entry
0
1
2
3
4
5
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10
20
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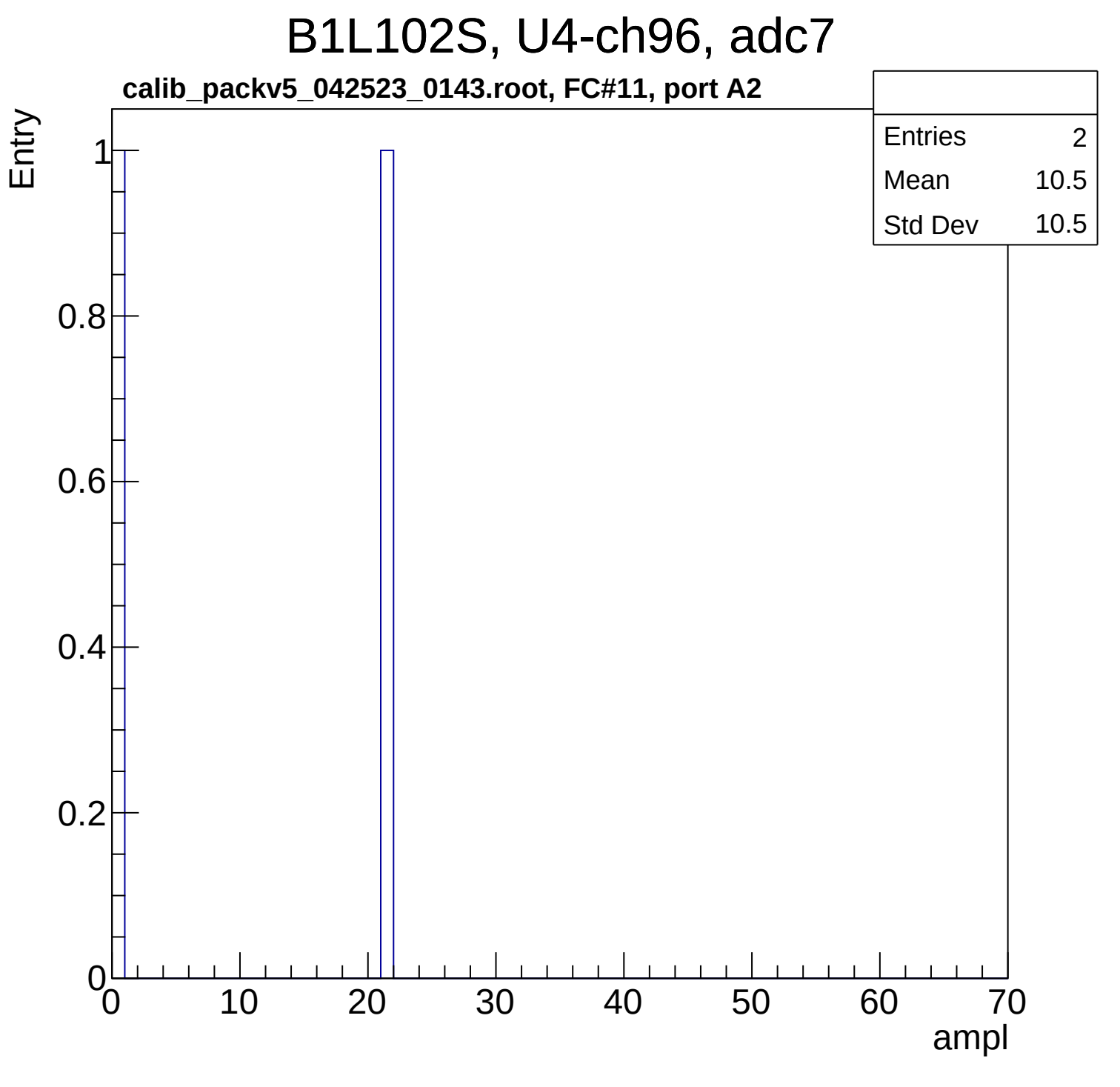
50
60
70
ampl


B1L102S, U4-ch96, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 10.5
Std Dev 10.5
Entry
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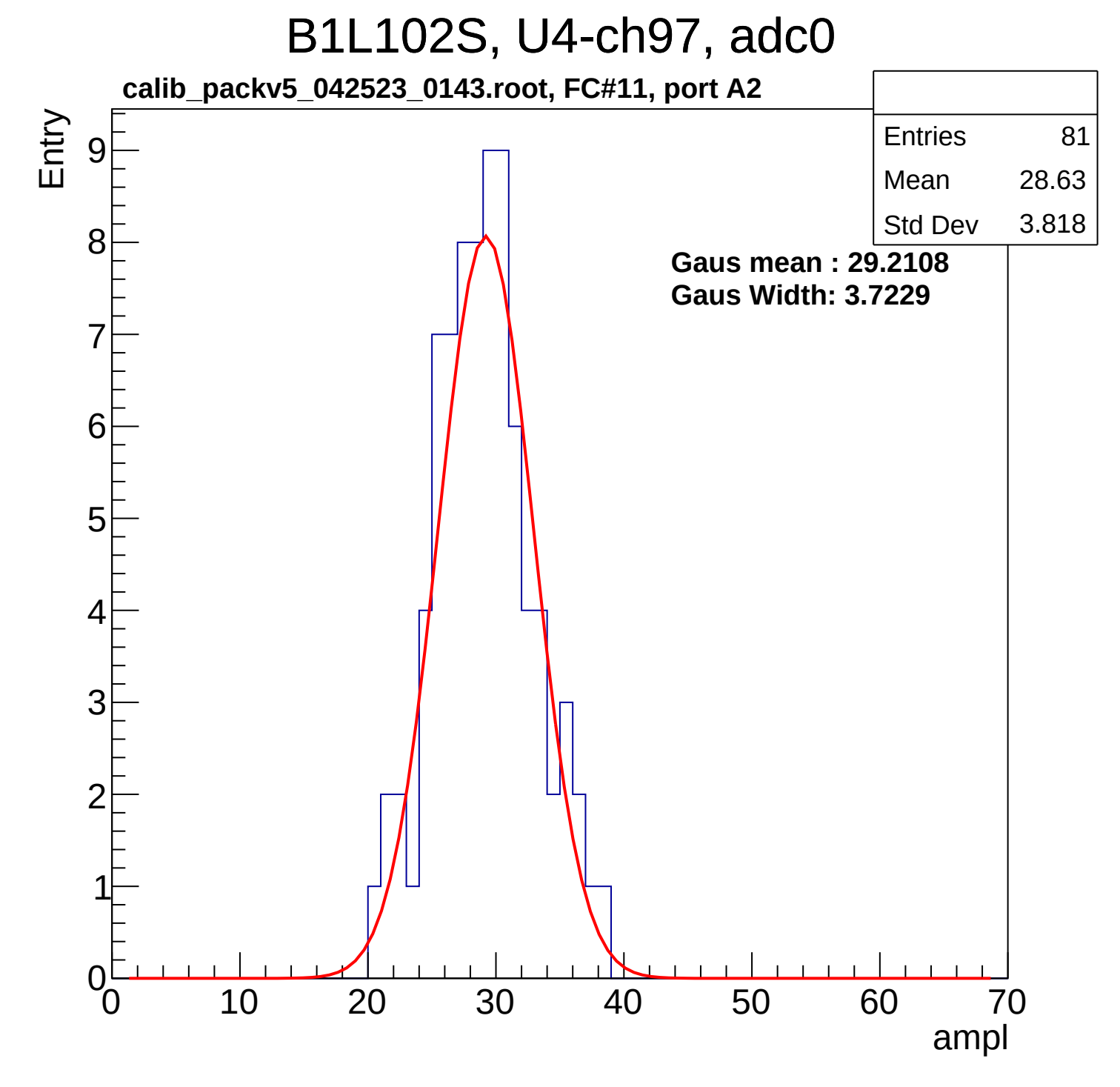
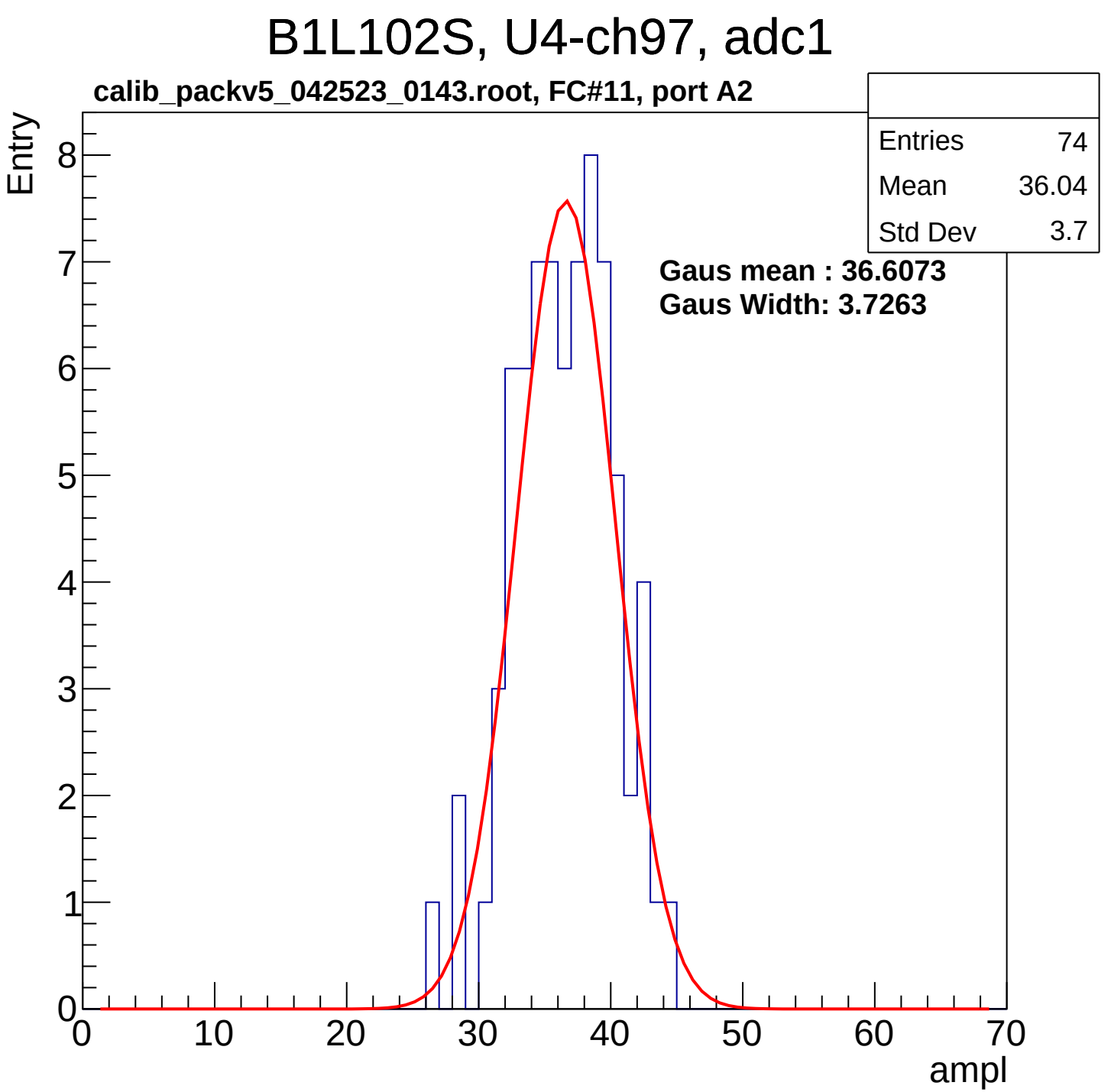
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch97, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 81
Mean 28.63
Std Dev 3.818
Gaus mean : 29.2108
Gaus Width: 3.7229
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L102S, U4-ch97, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 36.04
Std Dev 3.7
Gaus mean : 36.6073
Gaus Width: 3.7263
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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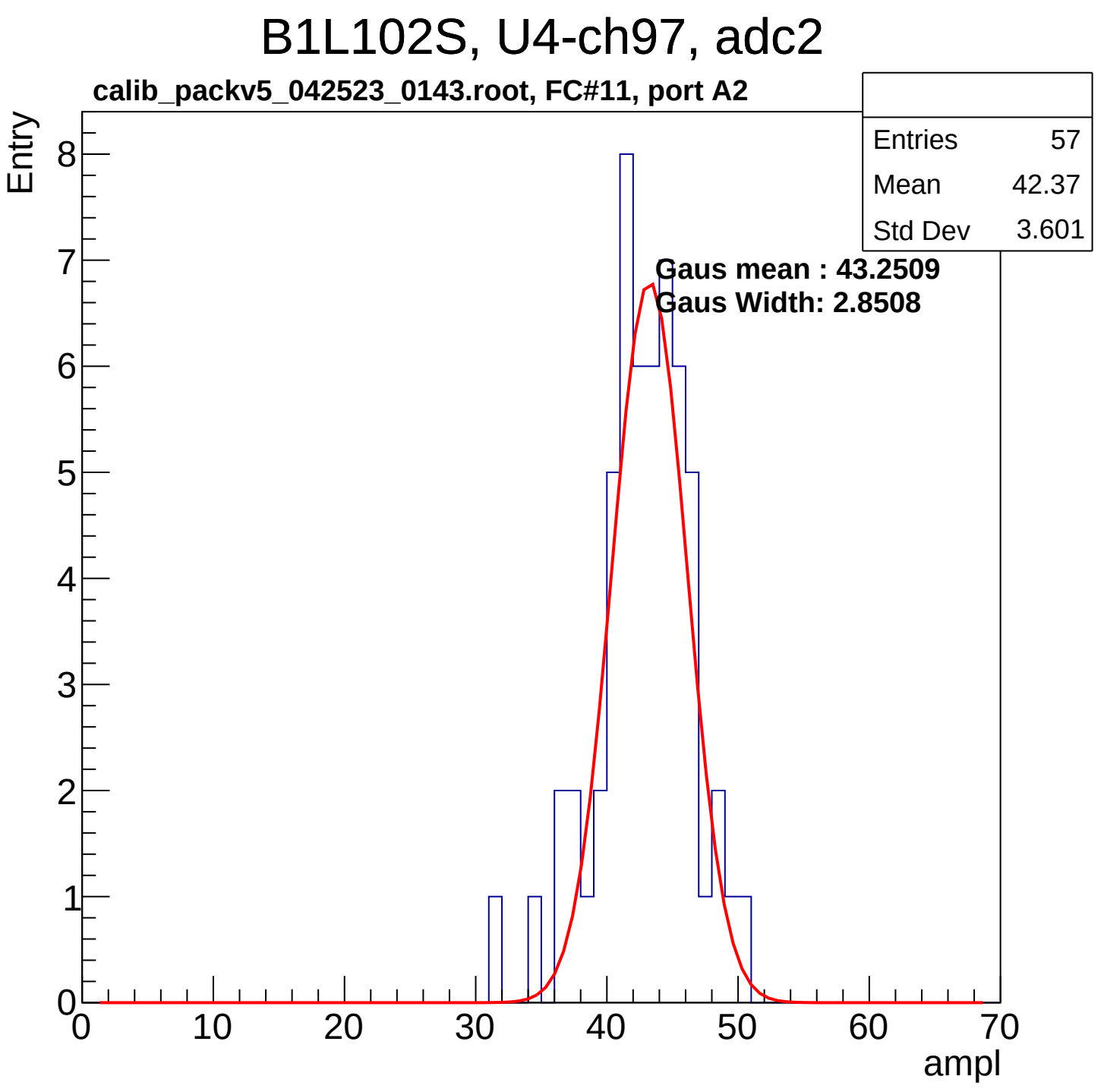
B1L102S, U4-ch97, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 57
Mean 42.37
Std Dev 3.601
Gaus mean : 43.2509
Gaus Width: 2.8508
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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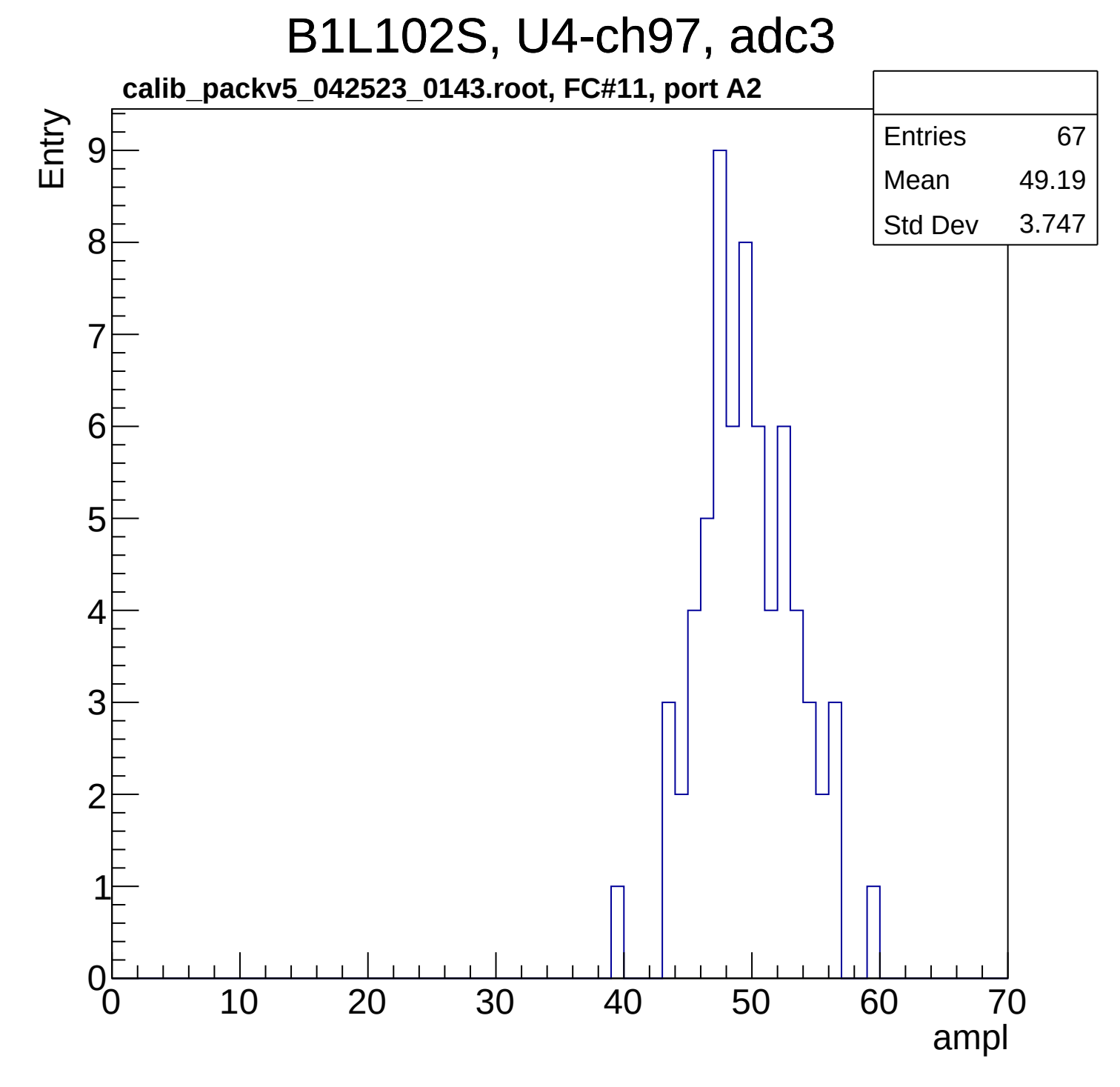
B1L102S, U4-ch97, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 49.19
Std Dev 3.747
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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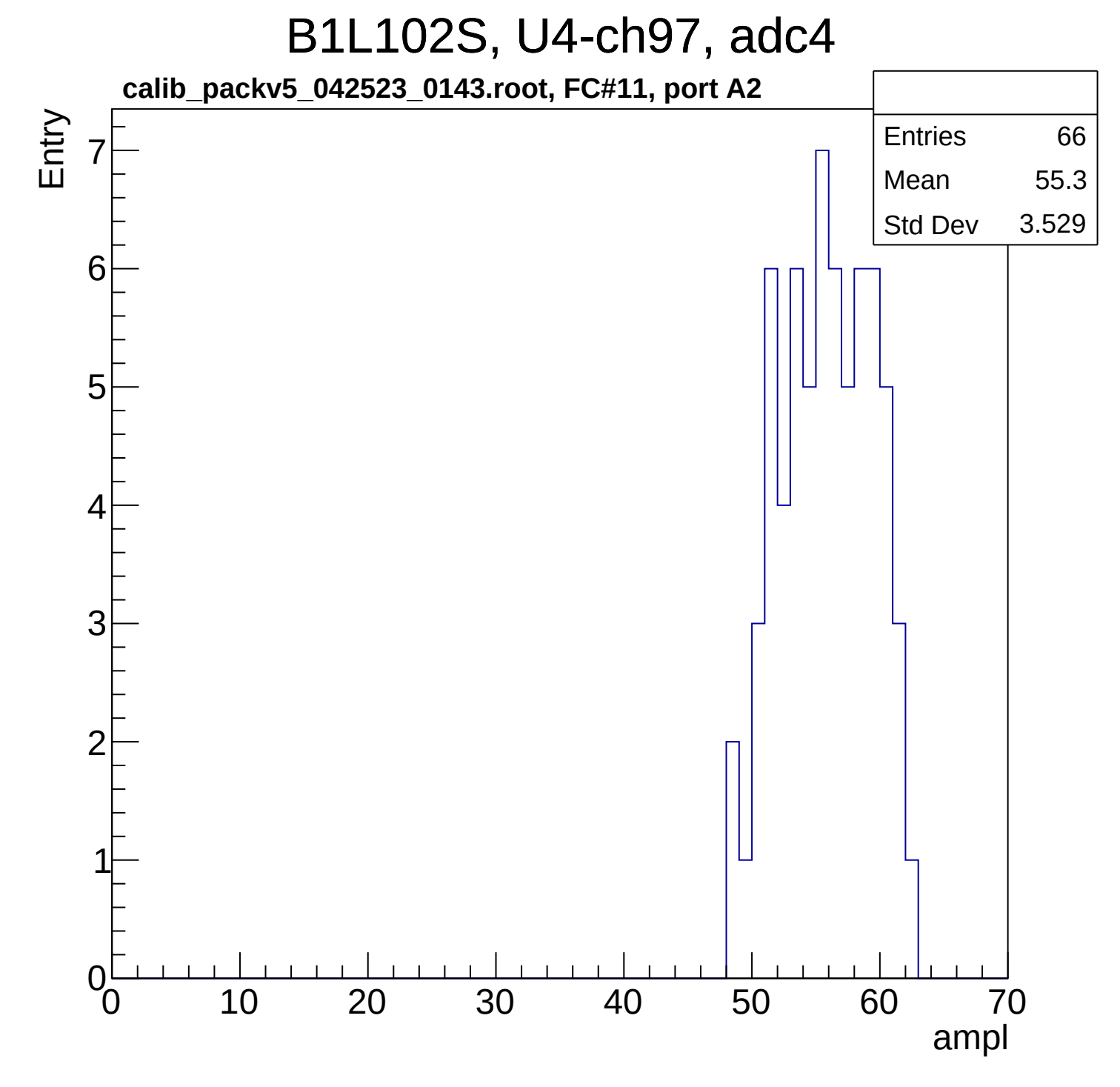
B1L102S, U4-ch97, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 55.3
Std Dev 3.529
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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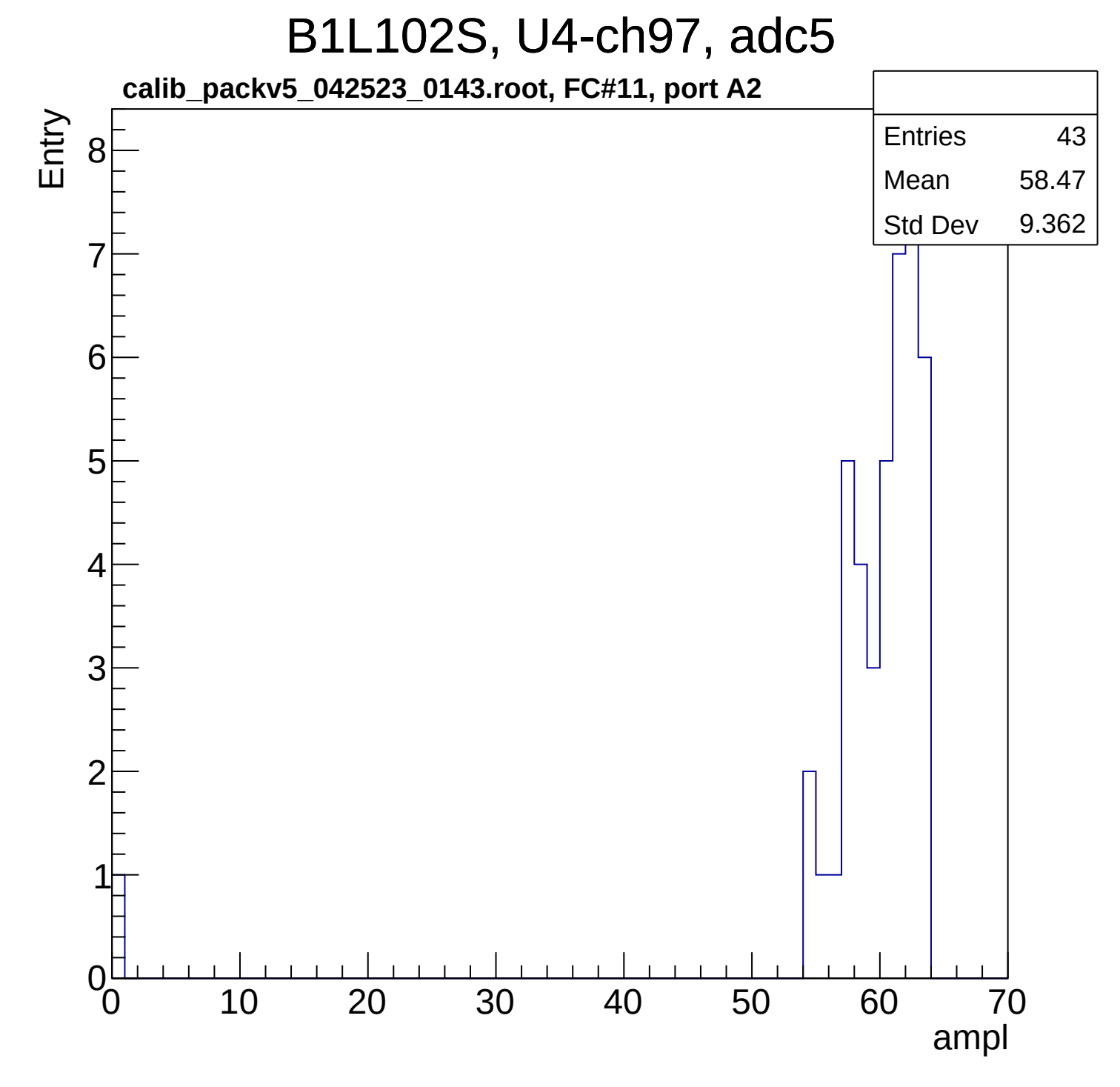
B1L102S, U4-ch97, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 43
Mean 58.47
Std Dev 9.362
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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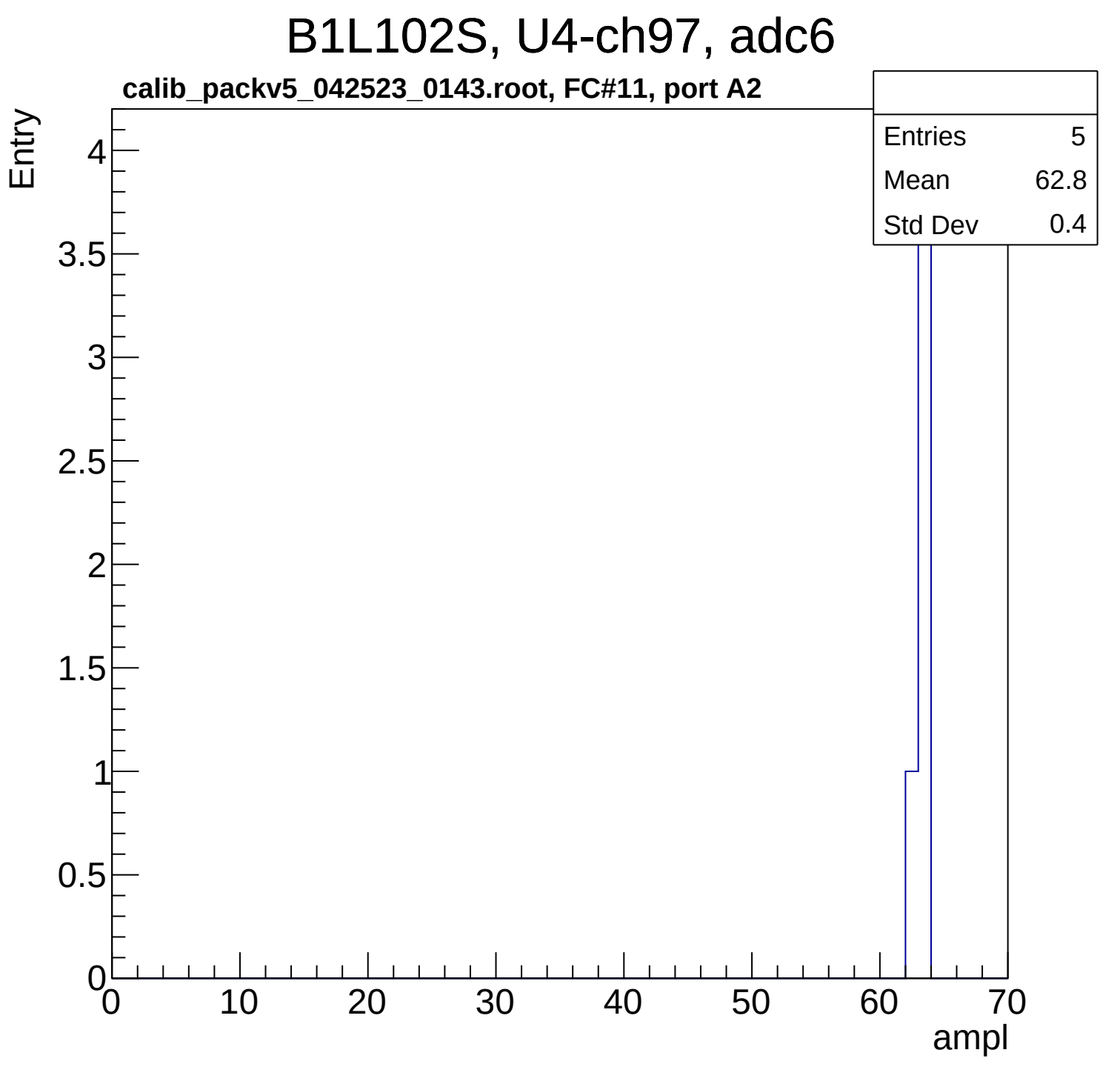
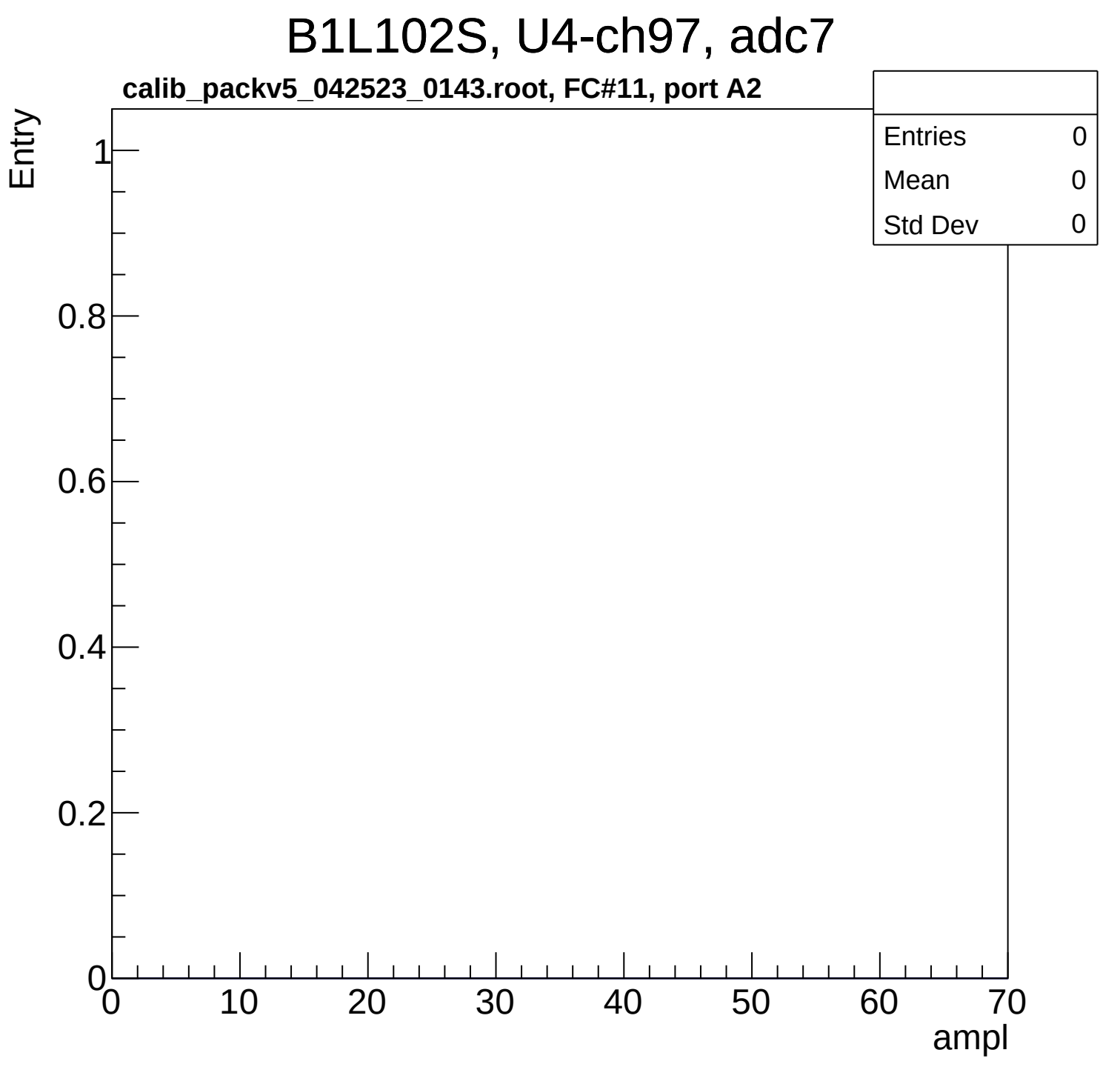
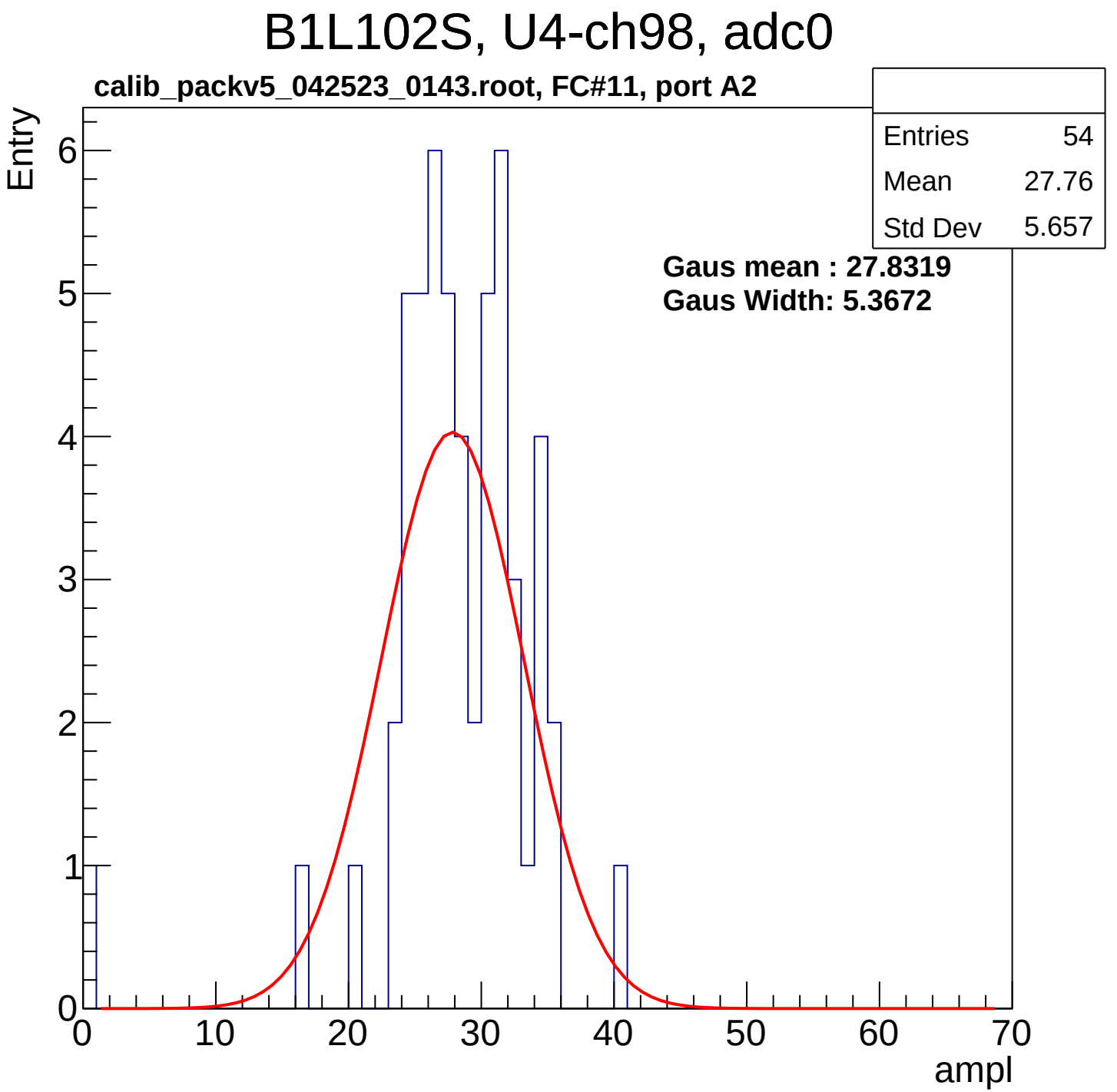
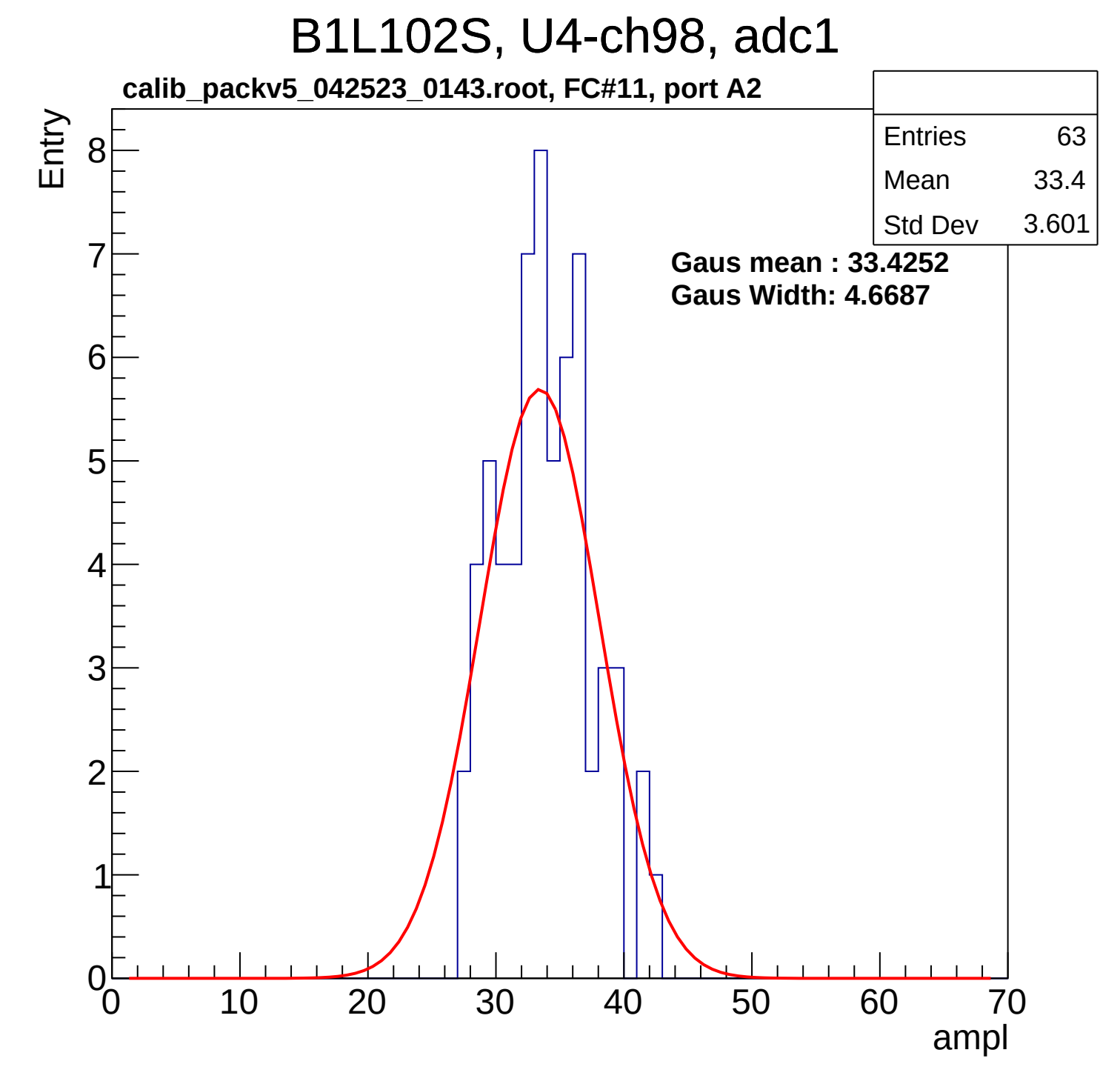

B1L102S, U4-ch97, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 5
Mean 62.8
Std Dev 0.4
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U4-ch97, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch98, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 27.76
Std Dev 5.657
Gaus mean : 27.8319
Gaus Width: 5.3672
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L102S, U4-ch98, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 33.4
Std Dev 3.601
Gaus mean : 33.4252
Gaus Width: 4.6687
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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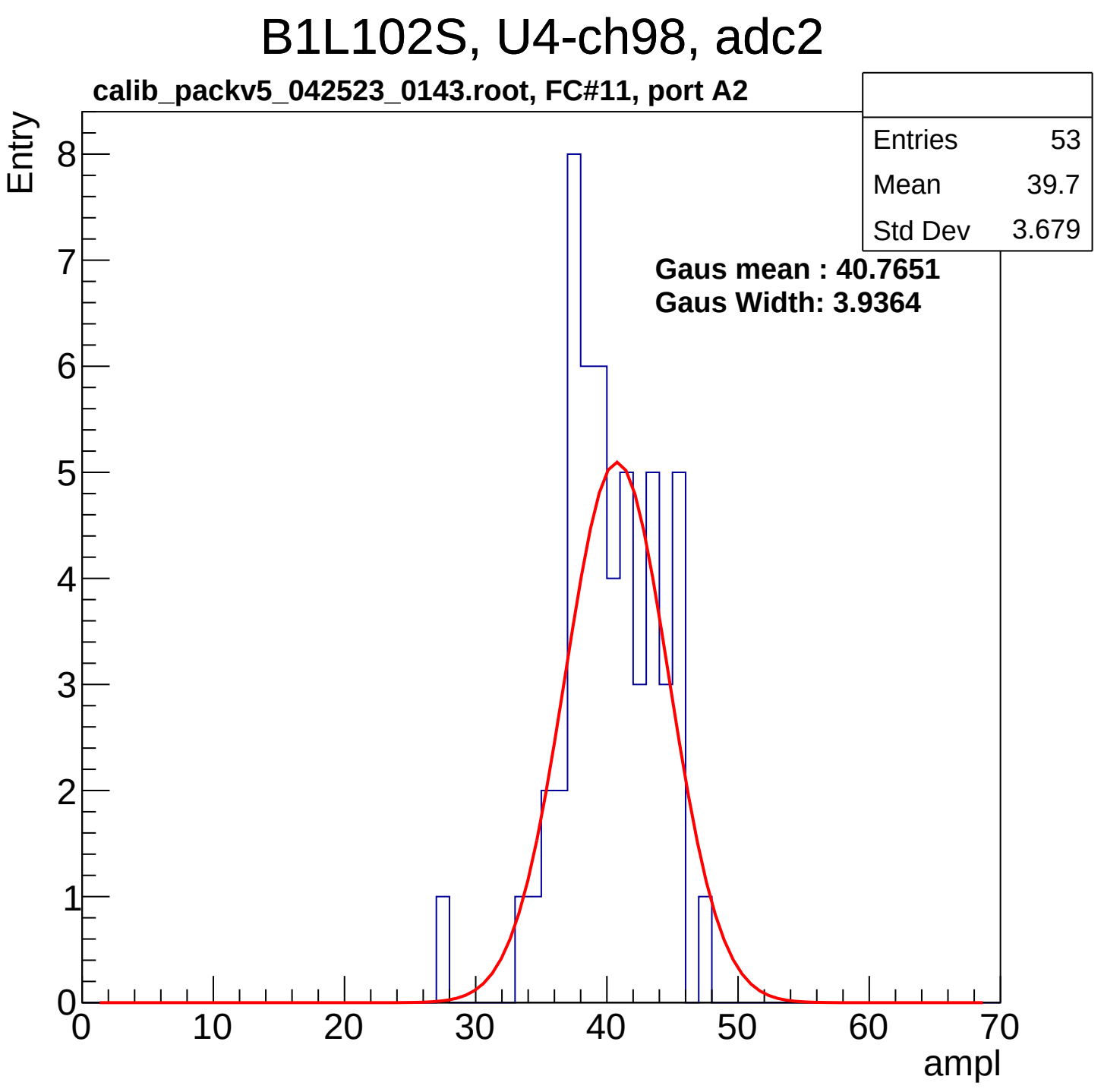
B1L102S, U4-ch98, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 39.7
Std Dev 3.679
Gaus mean : 40.7651
Gaus Width: 3.9364
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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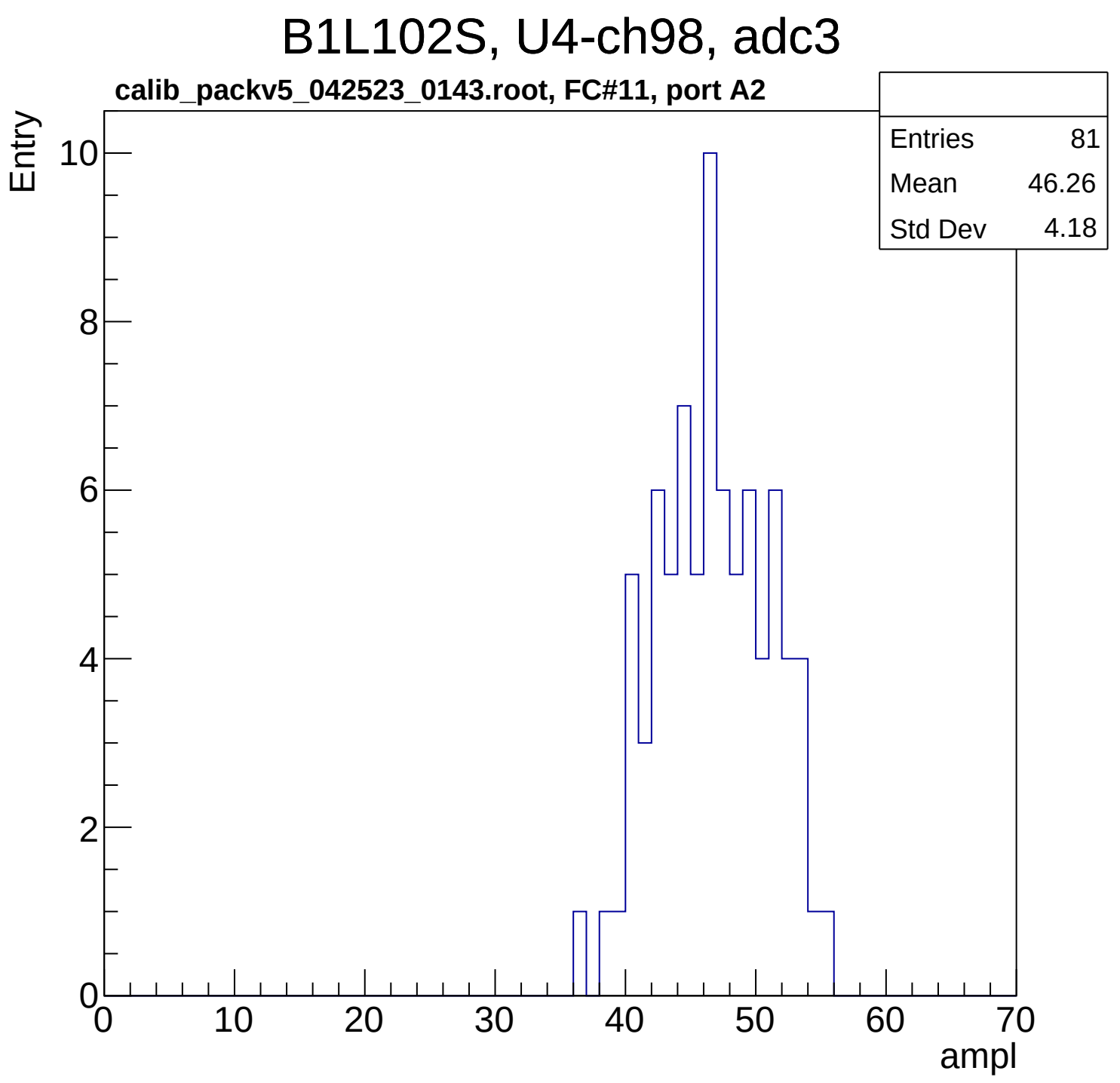
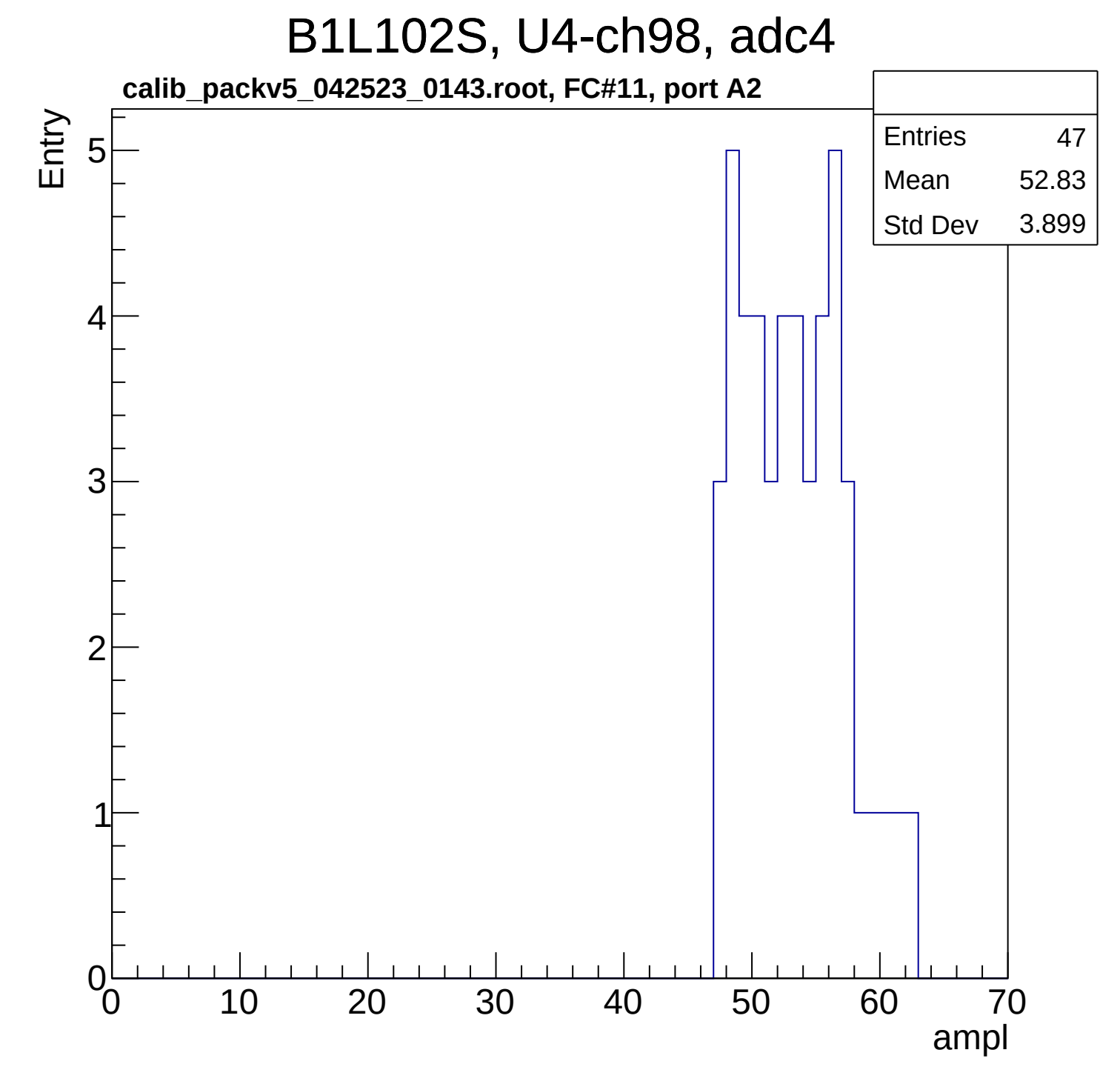
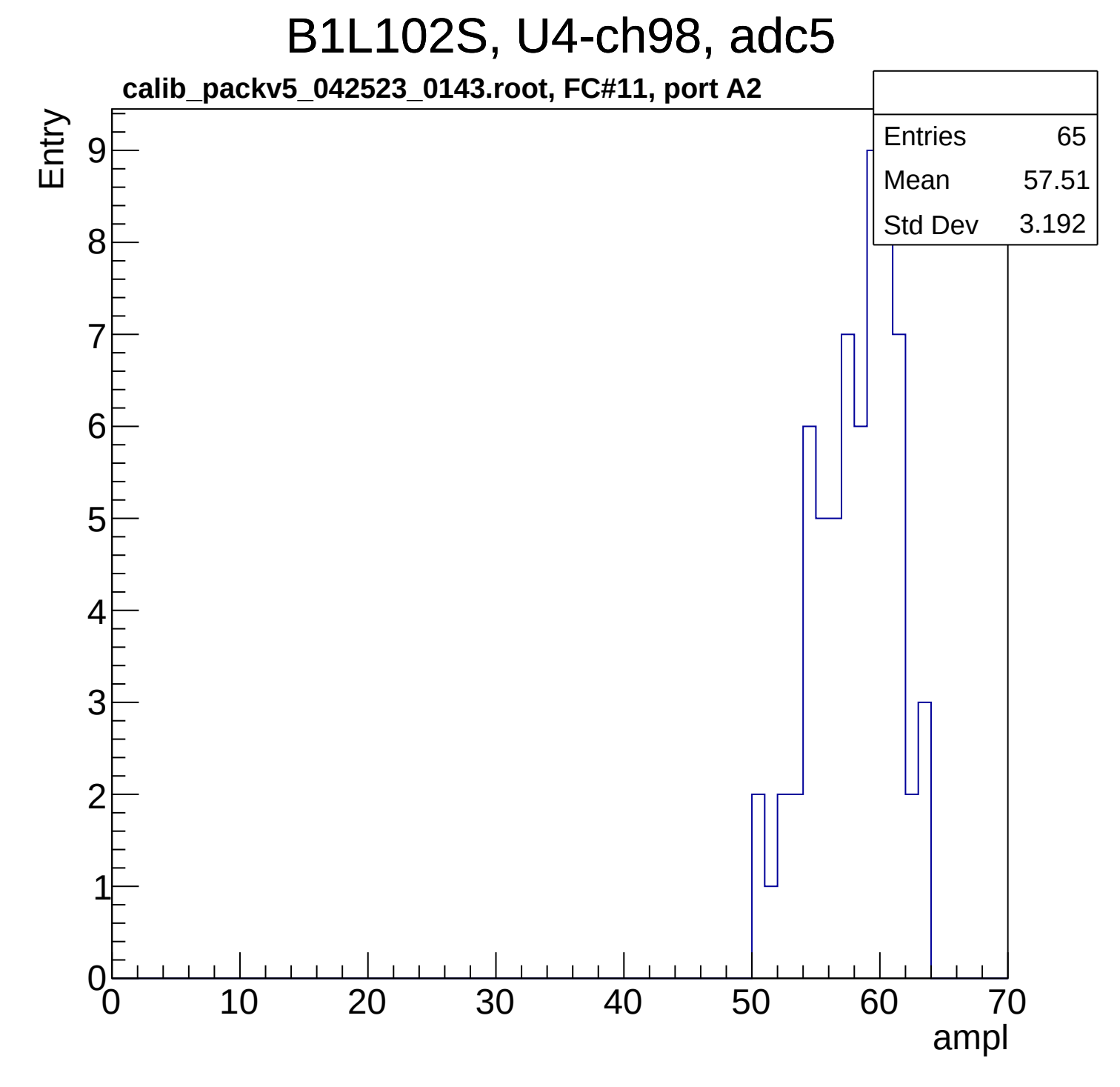

B1L102S, U4-ch98, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 81
Mean 46.26
Std Dev 4.18
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch98, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 47
Mean 52.83
Std Dev 3.899
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L102S, U4-ch98, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 57.51
Std Dev 3.192
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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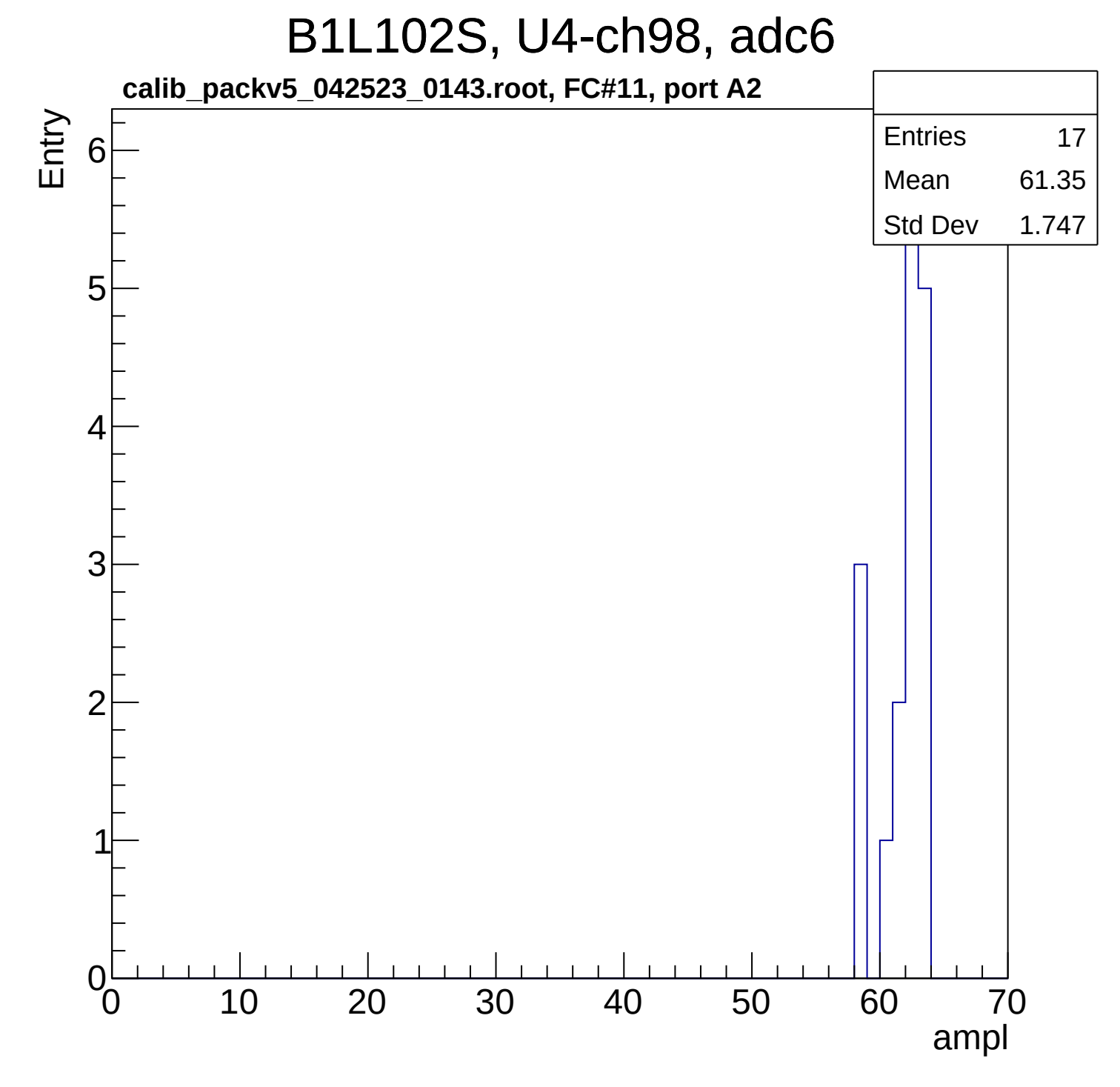
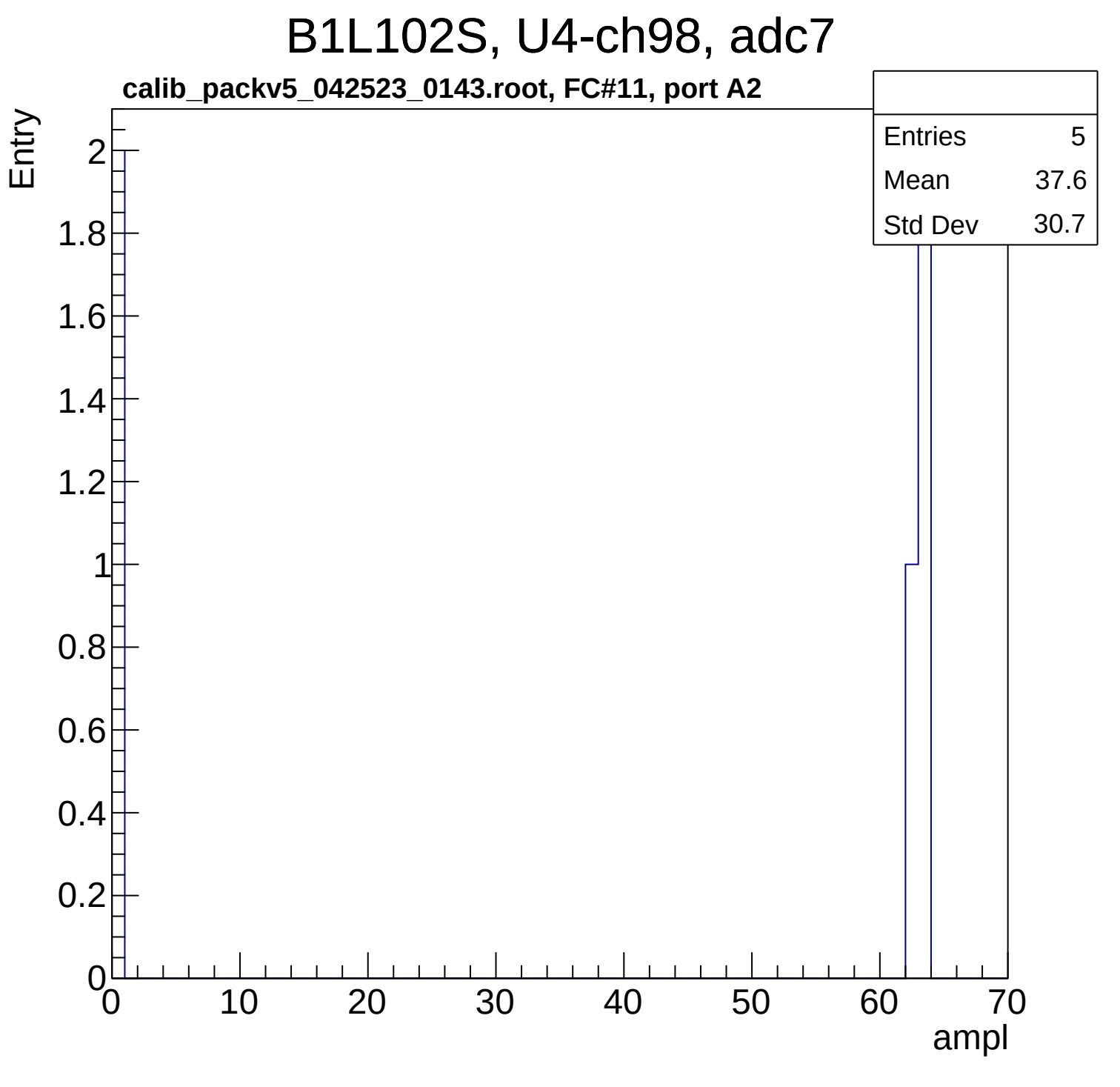
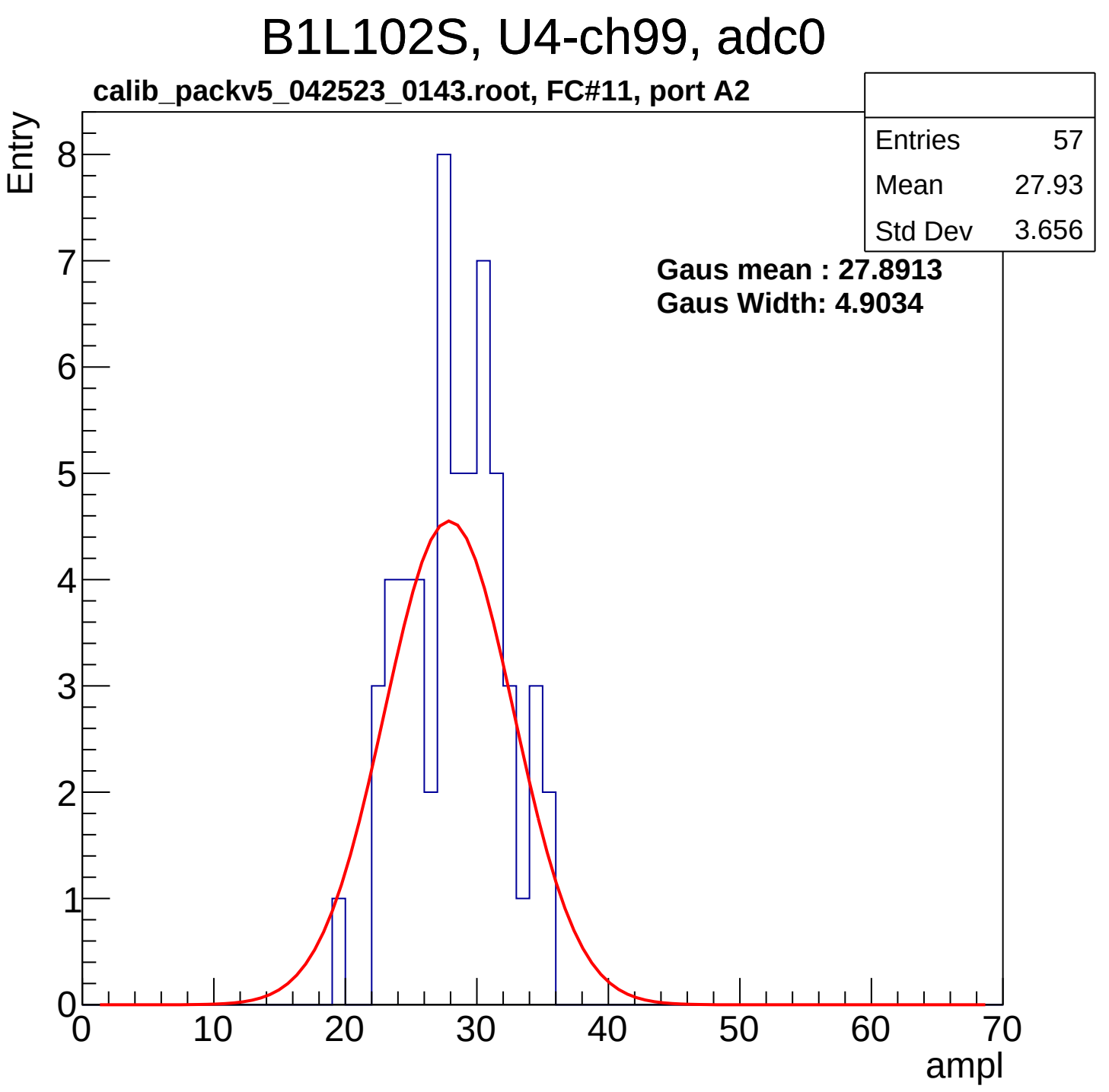
60
70


B1L102S, U4-ch98, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 17
Mean 61.35
Std Dev 1.747
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch98, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 5
Mean 37.6
Std Dev 30.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L102S, U4-ch99, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 57
Mean 27.93
Std Dev 3.656
Gaus mean : 27.8913
Gaus Width: 4.9034
Entry
ampl
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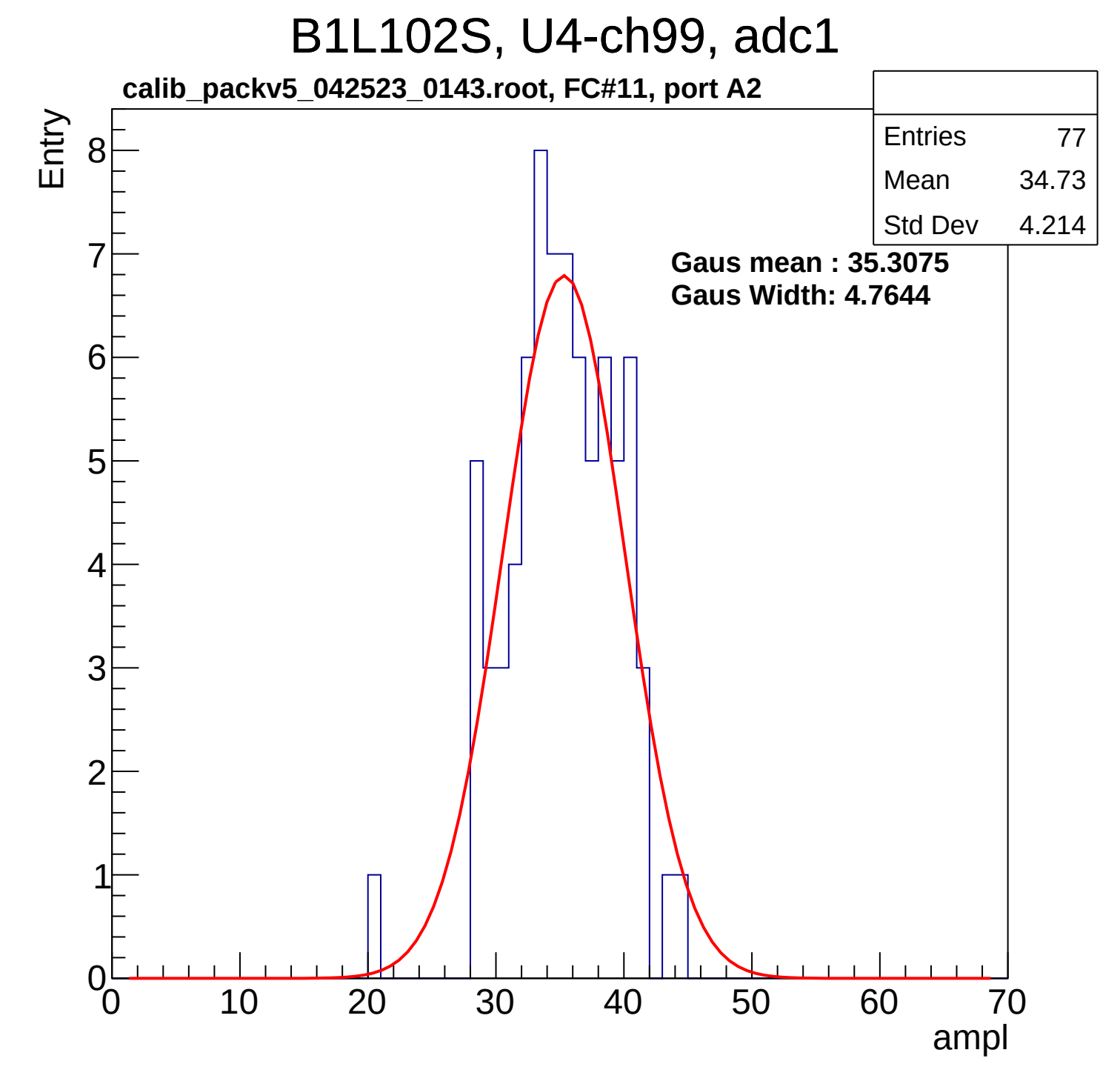
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch99, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 77
Mean 34.73
Std Dev 4.214
Gaus mean : 35.3075
Gaus Width: 4.7644
Entry
ampl
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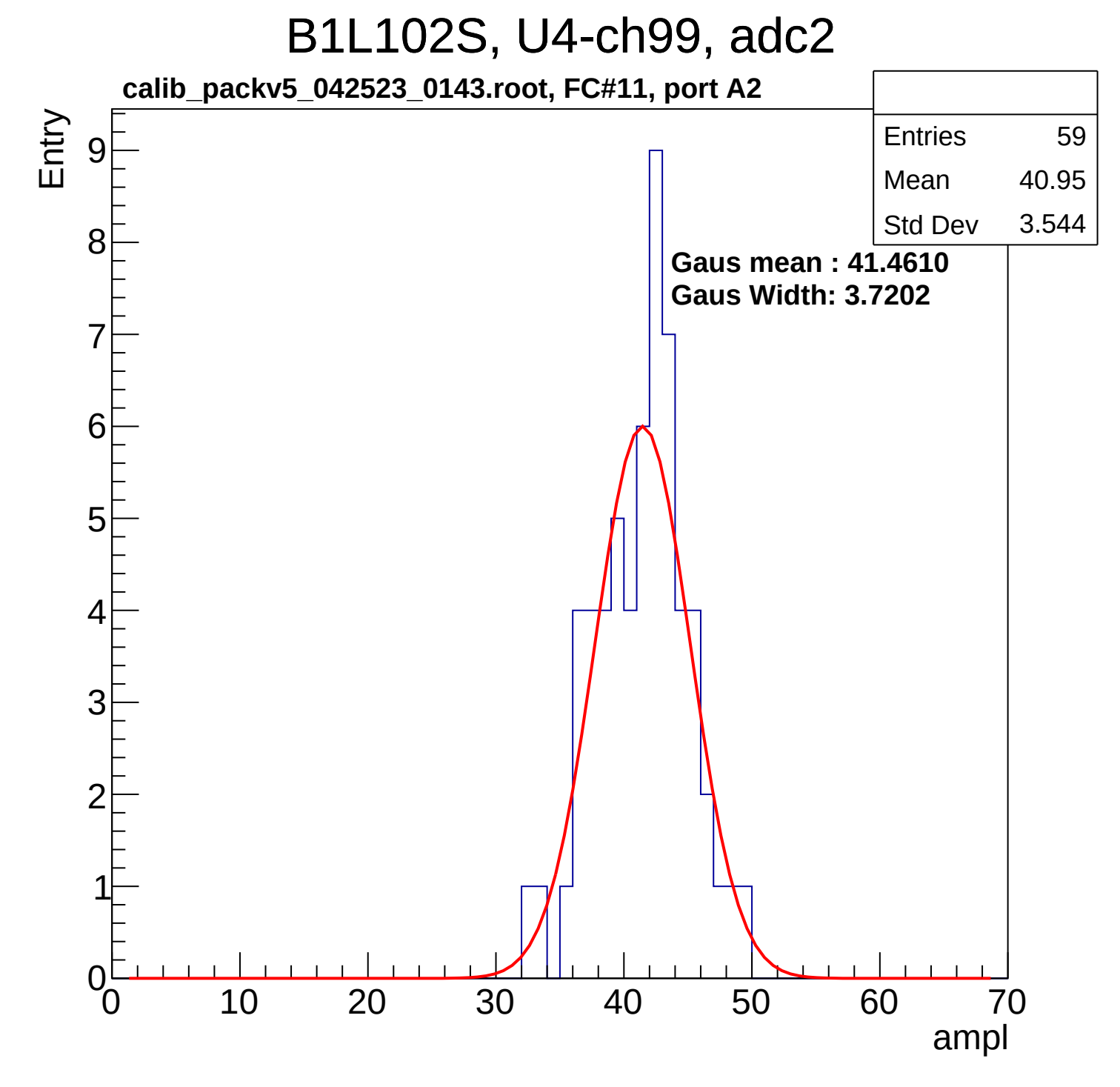
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch99, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 40.95
Std Dev 3.544
Gaus mean : 41.4610
Gaus Width: 3.7202
Entry
ampl
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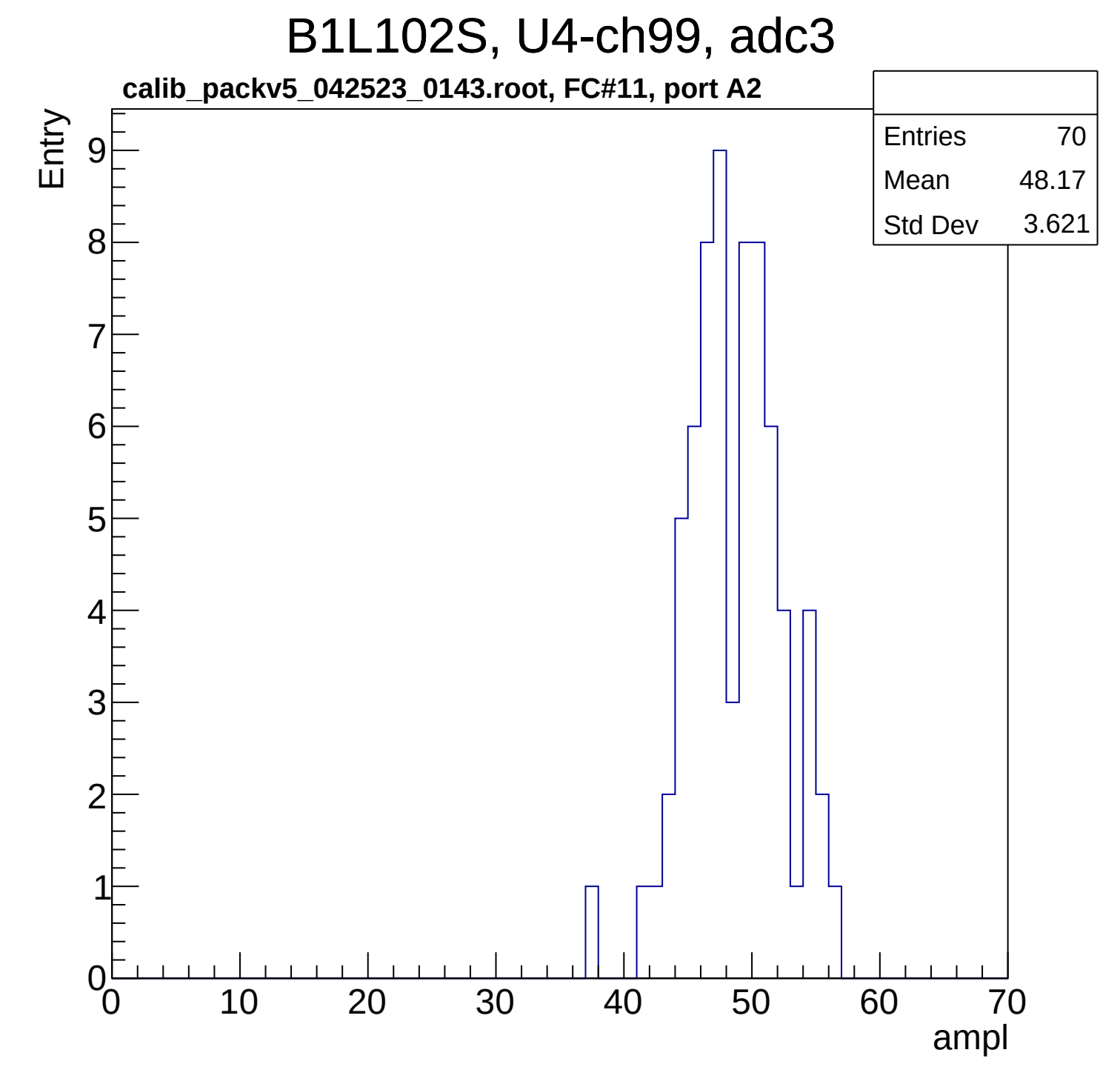
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch99, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 48.17
Std Dev 3.621
Entry
ampl
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3
4
5
6
7
8
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0
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20
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60
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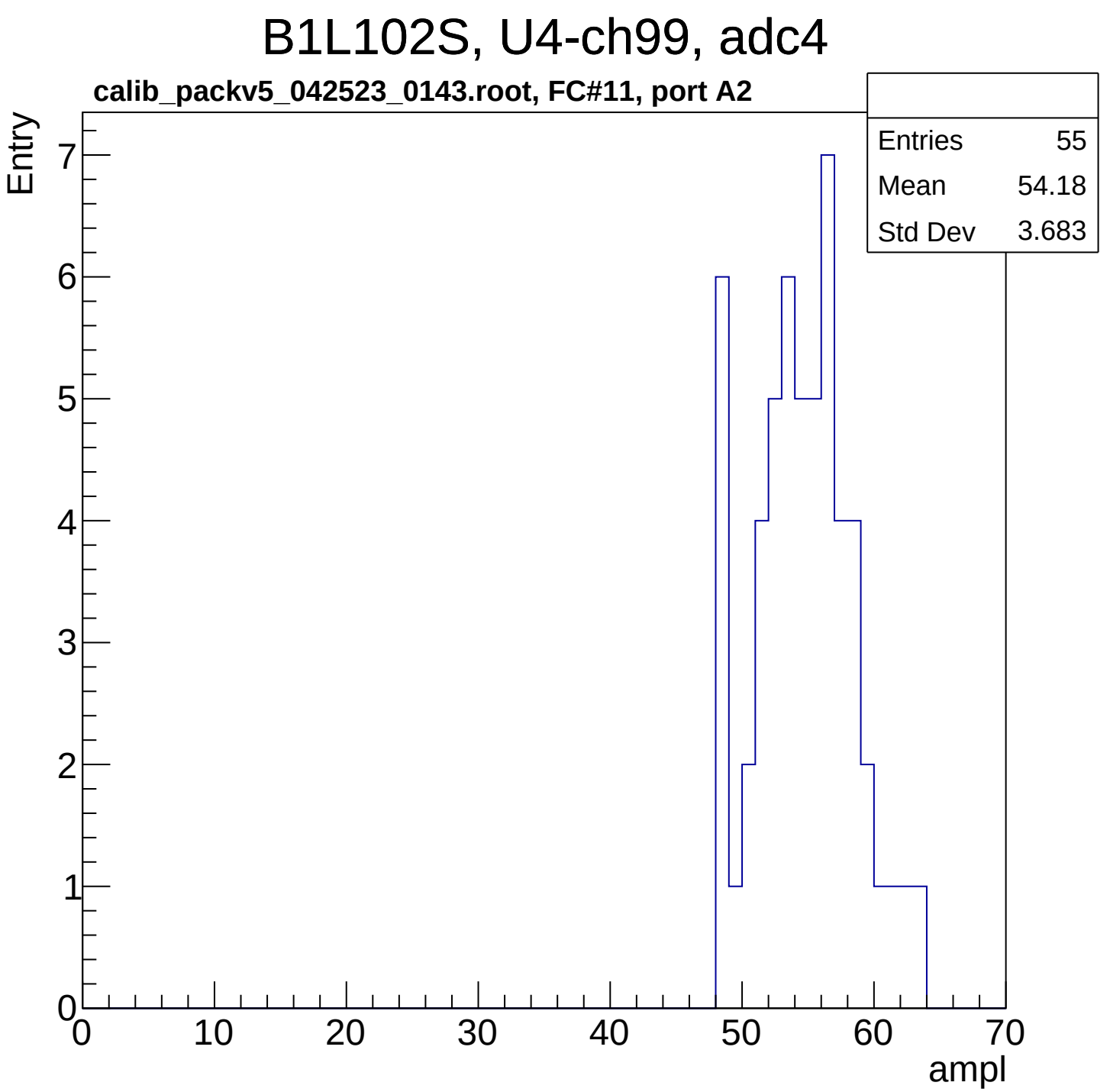
B1L102S, U4-ch99, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 54.18
Std Dev 3.683
Entry
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1
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3
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5
6
7
0
10
20
30
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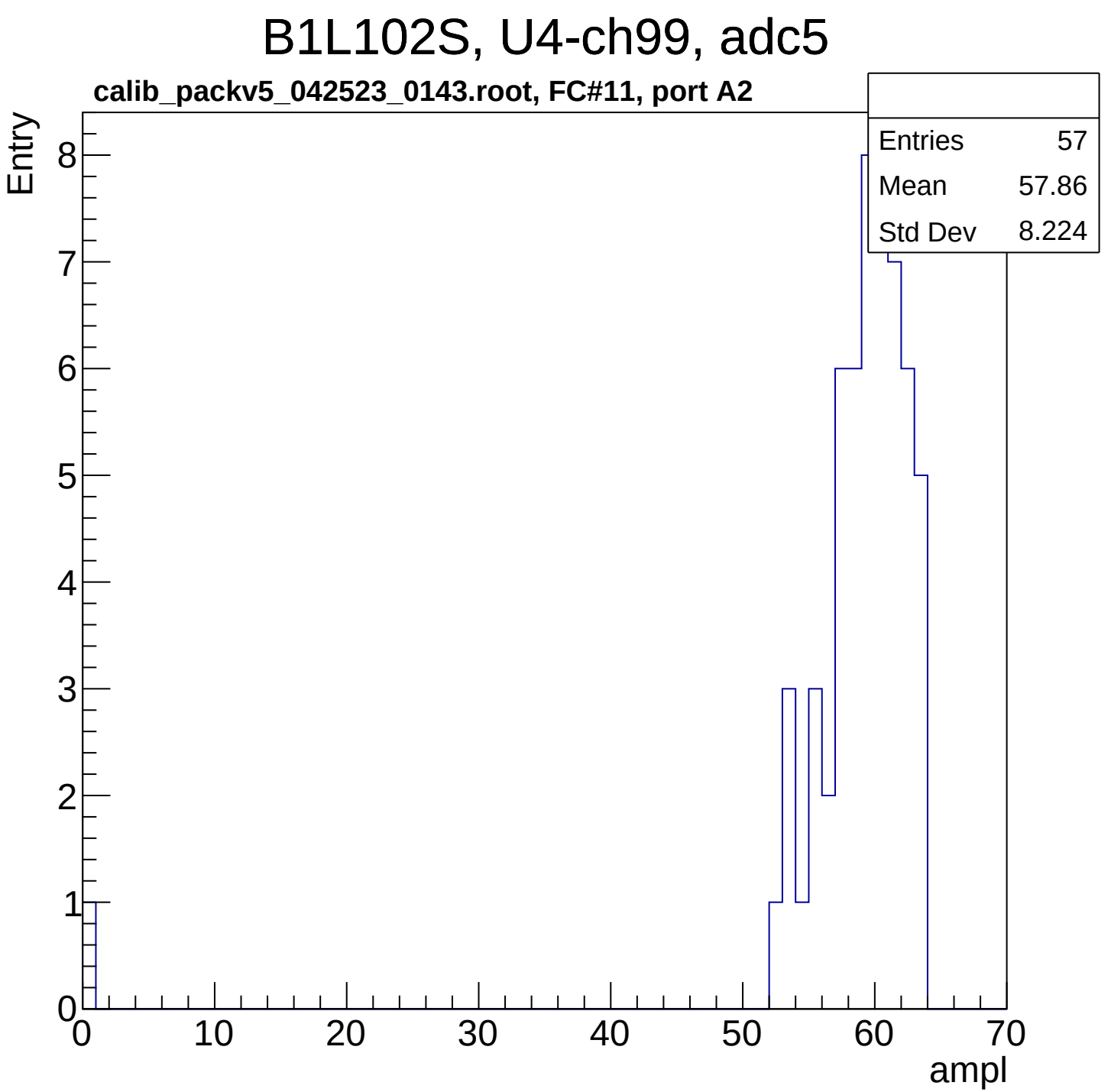
50
60
70
ampl


B1L102S, U4-ch99, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 57
Mean 57.86
Std Dev 8.224
Entry
ampl
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2
3
4
5
6
7
8
0
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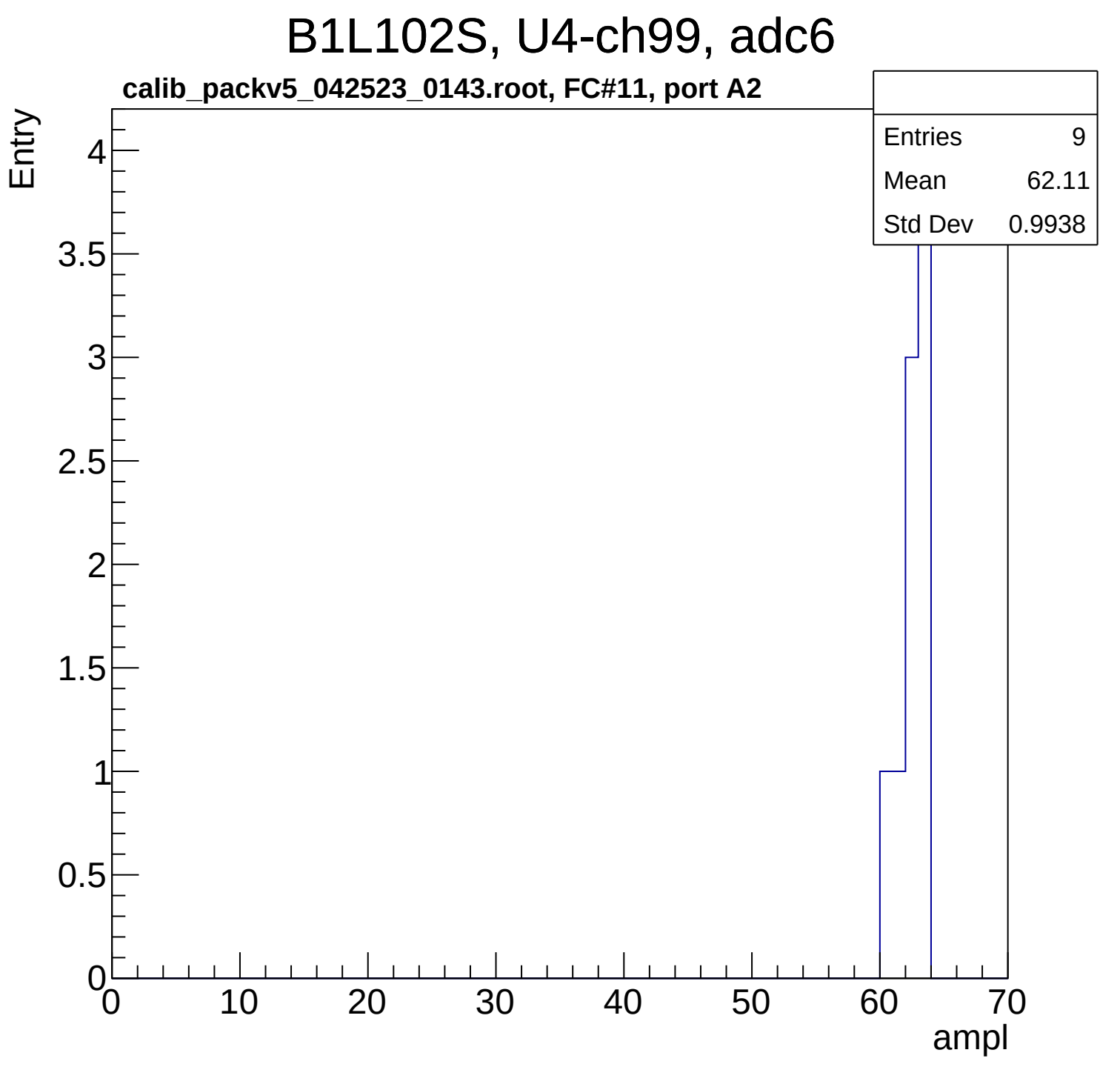
20
30
40
50
60
70


B1L102S, U4-ch99, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 9
Mean 62.11
Std Dev 0.9938
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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20
30
40
50
60
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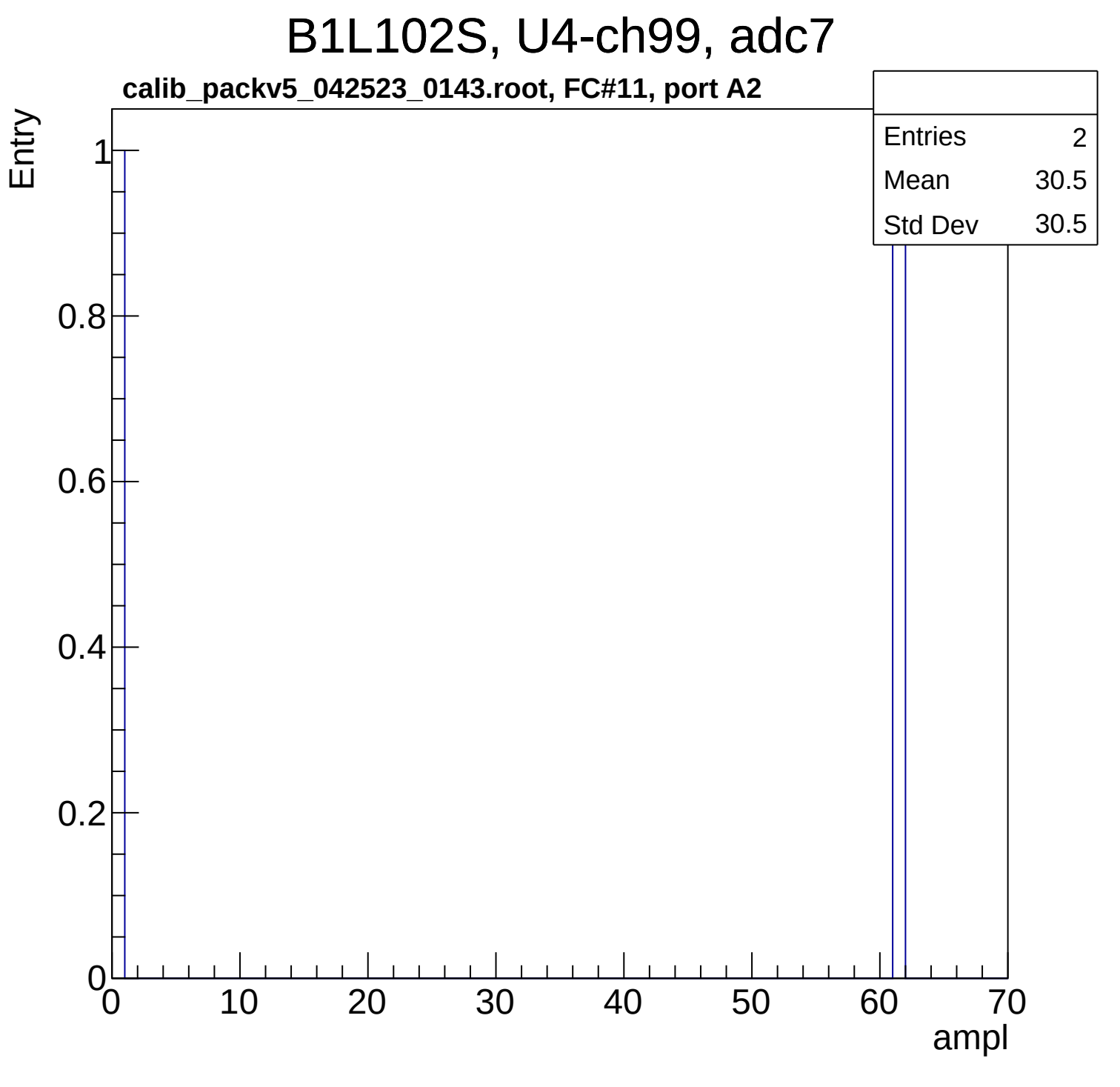
B1L102S, U4-ch99, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 30.5
Std Dev 30.5
Entry
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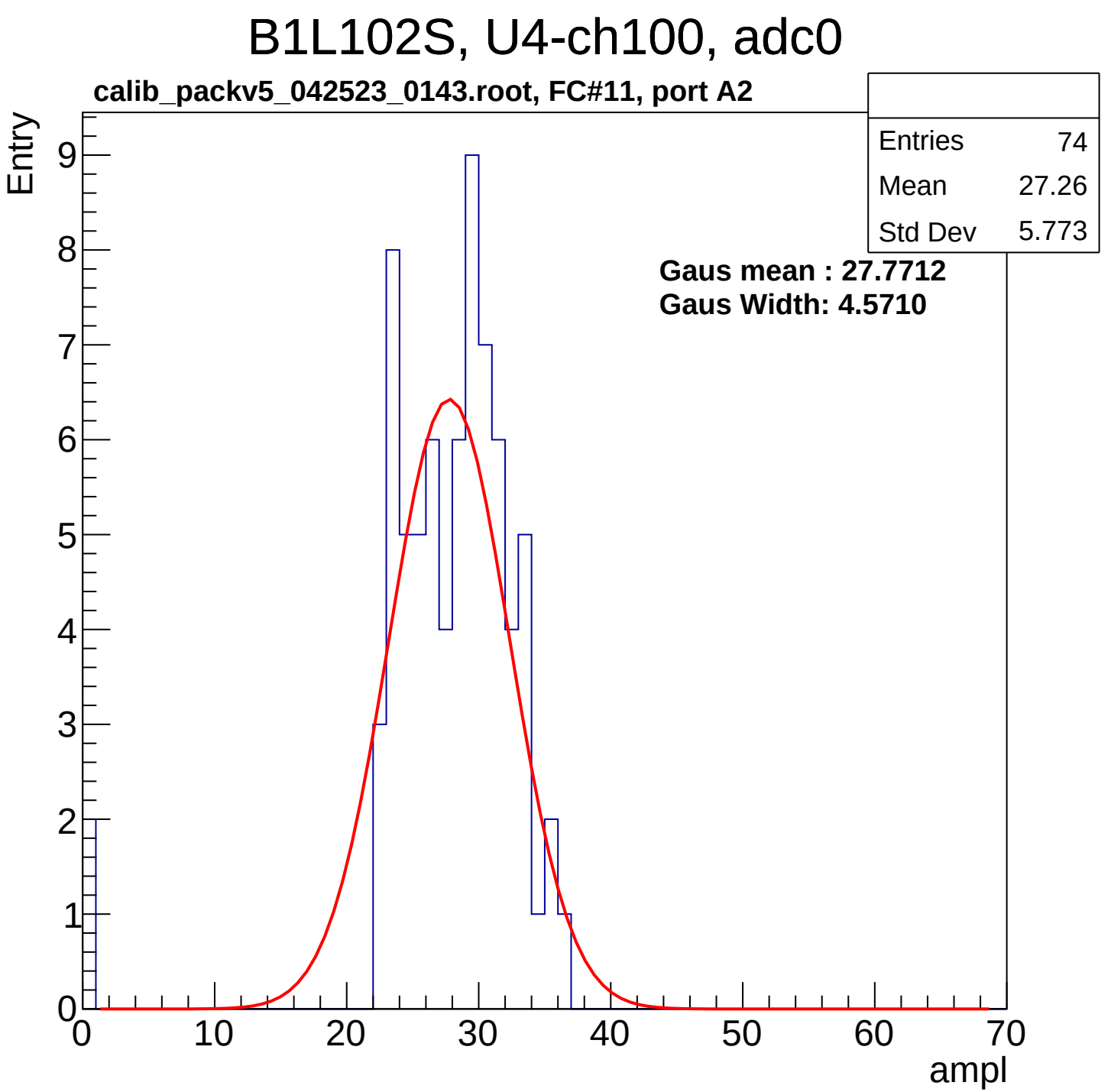
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch100, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 27.26
Std Dev 5.773
Gaus mean : 27.7712
Gaus Width: 4.5710
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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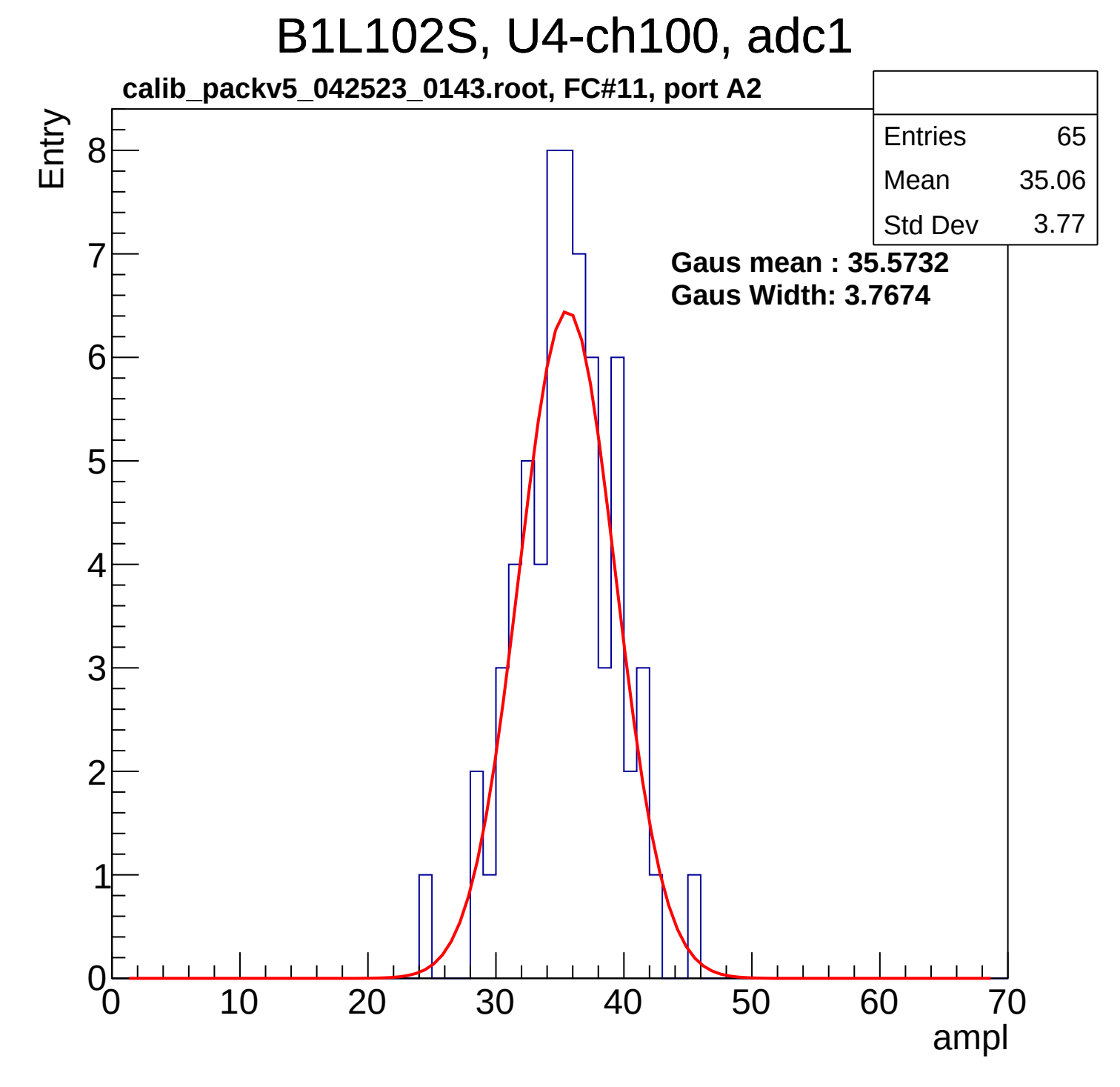
B1L102S, U4-ch100, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 35.06
Std Dev 3.77
Gaus mean : 35.5732
Gaus Width: 3.7674
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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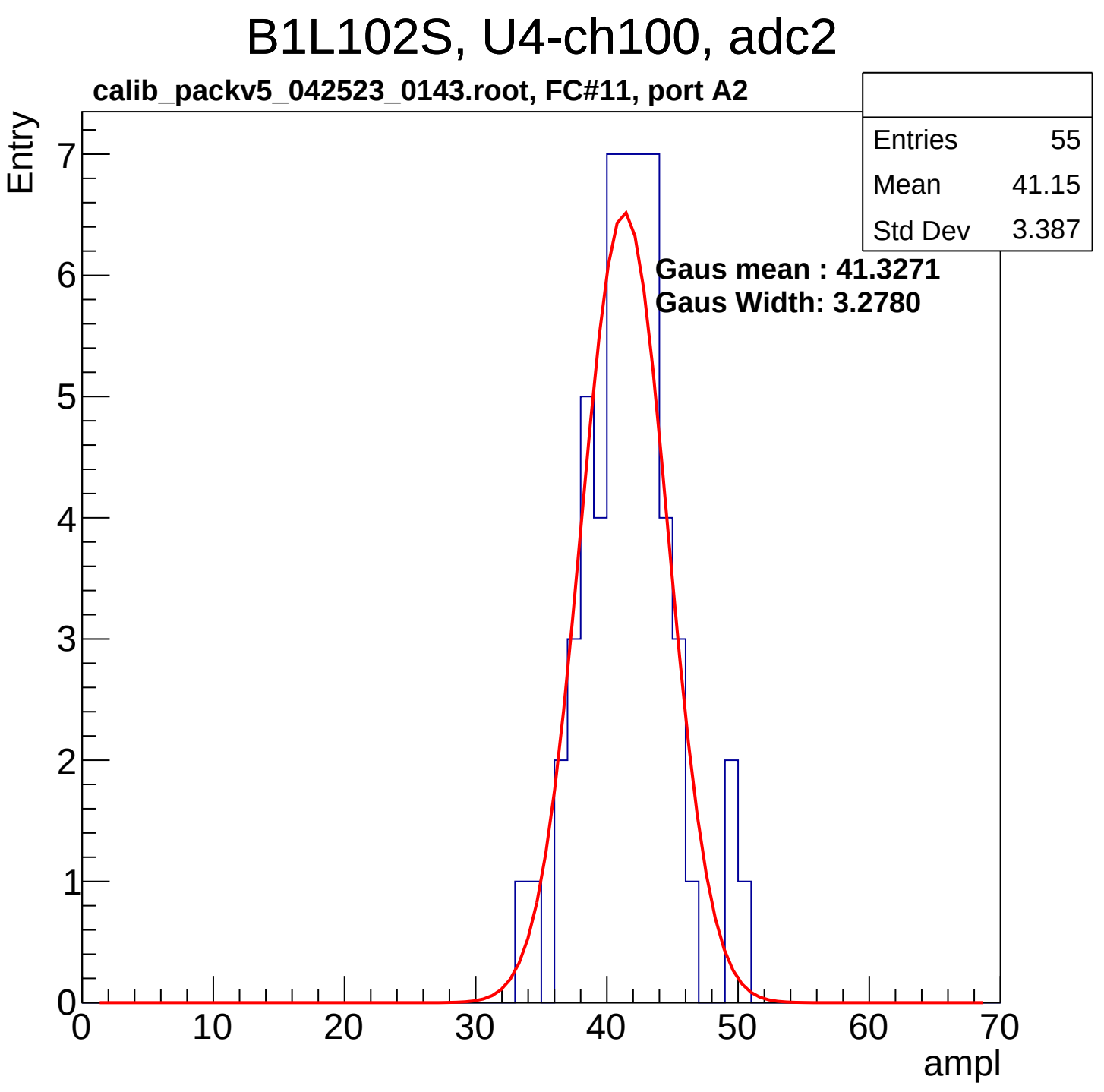
B1L102S, U4-ch100, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 41.15
Std Dev 3.387
Gaus mean : 41.3271
Gaus Width: 3.2780
Entry
ampl
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1
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3
4
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0
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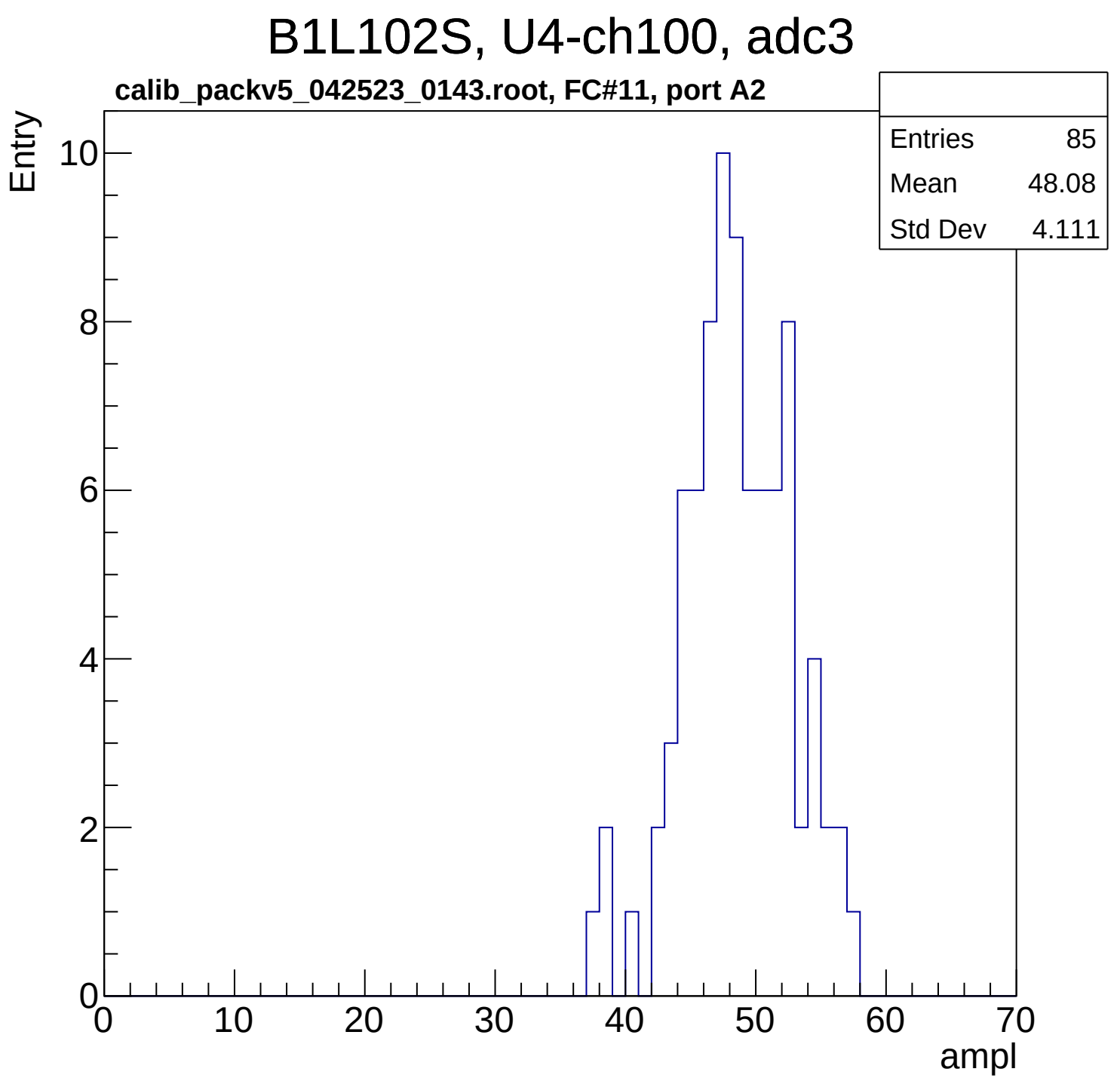
B1L102S, U4-ch100, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 85
Mean 48.08
Std Dev 4.111
Entry
ampl
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60
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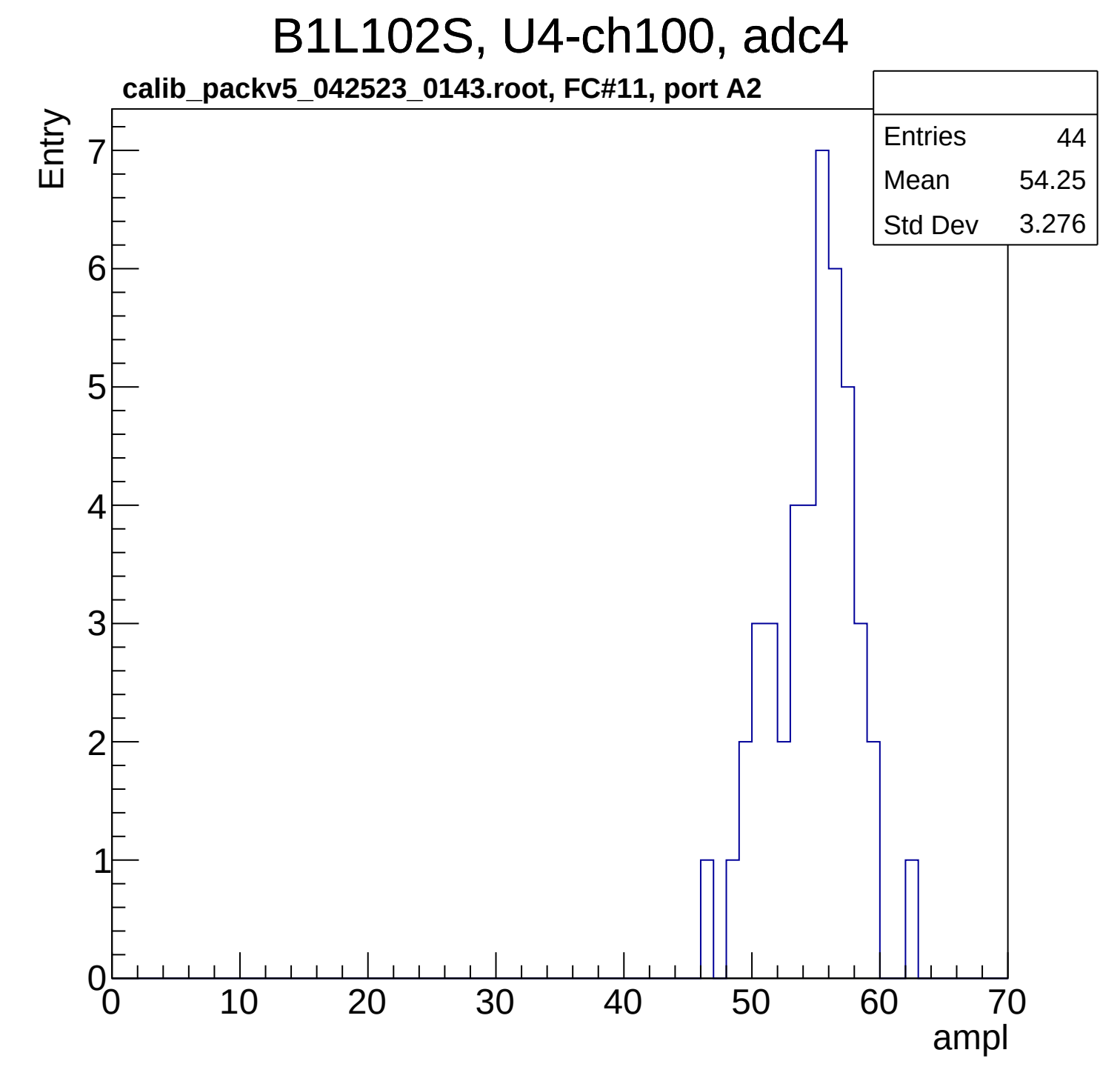
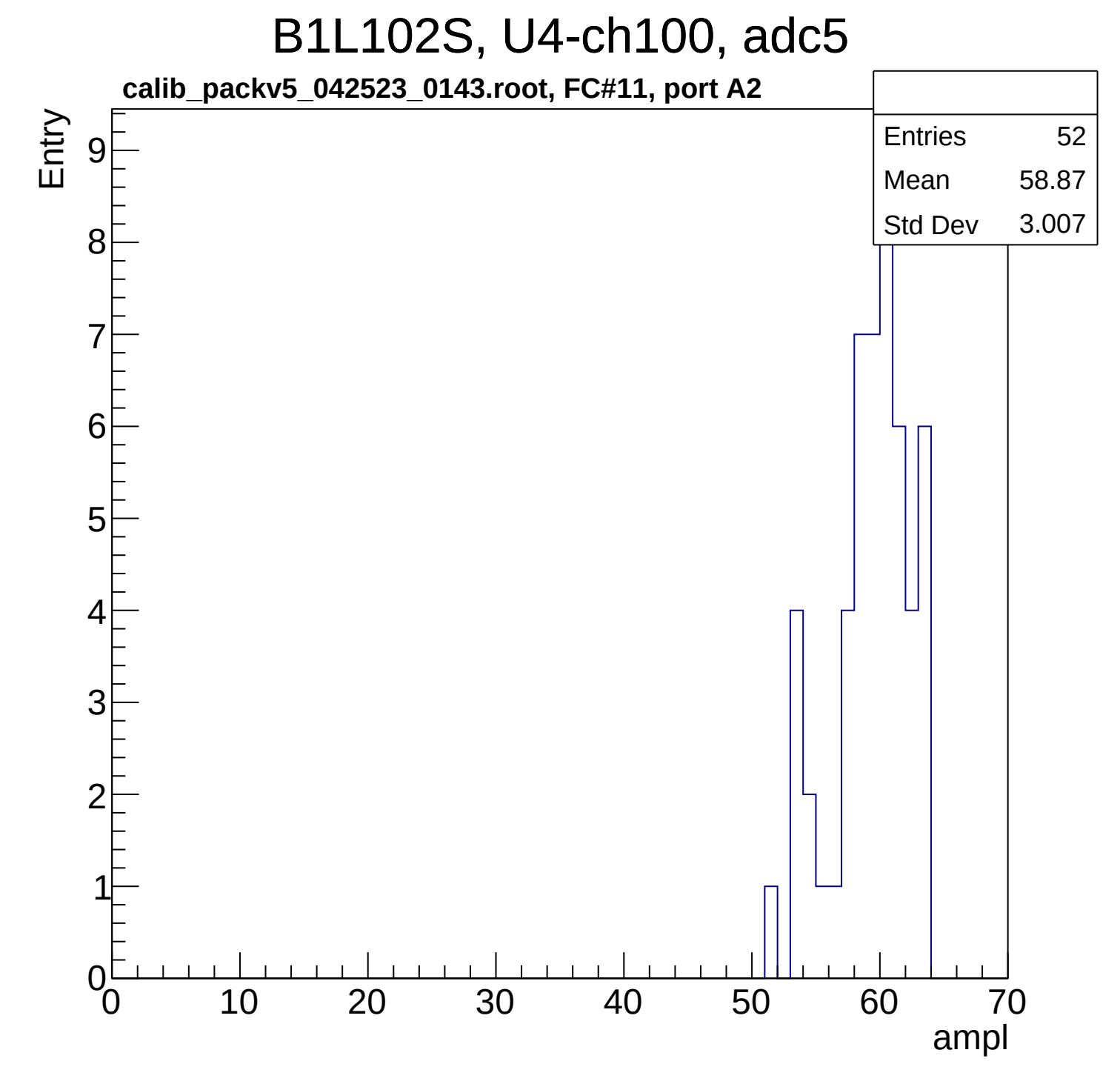

B1L102S, U4-ch100, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 44
Mean 54.25
Std Dev 3.276
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch100, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 52
Mean 58.87
Std Dev 3.007
Entry
ampl
0
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2
3
4
5
6
7
8
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0
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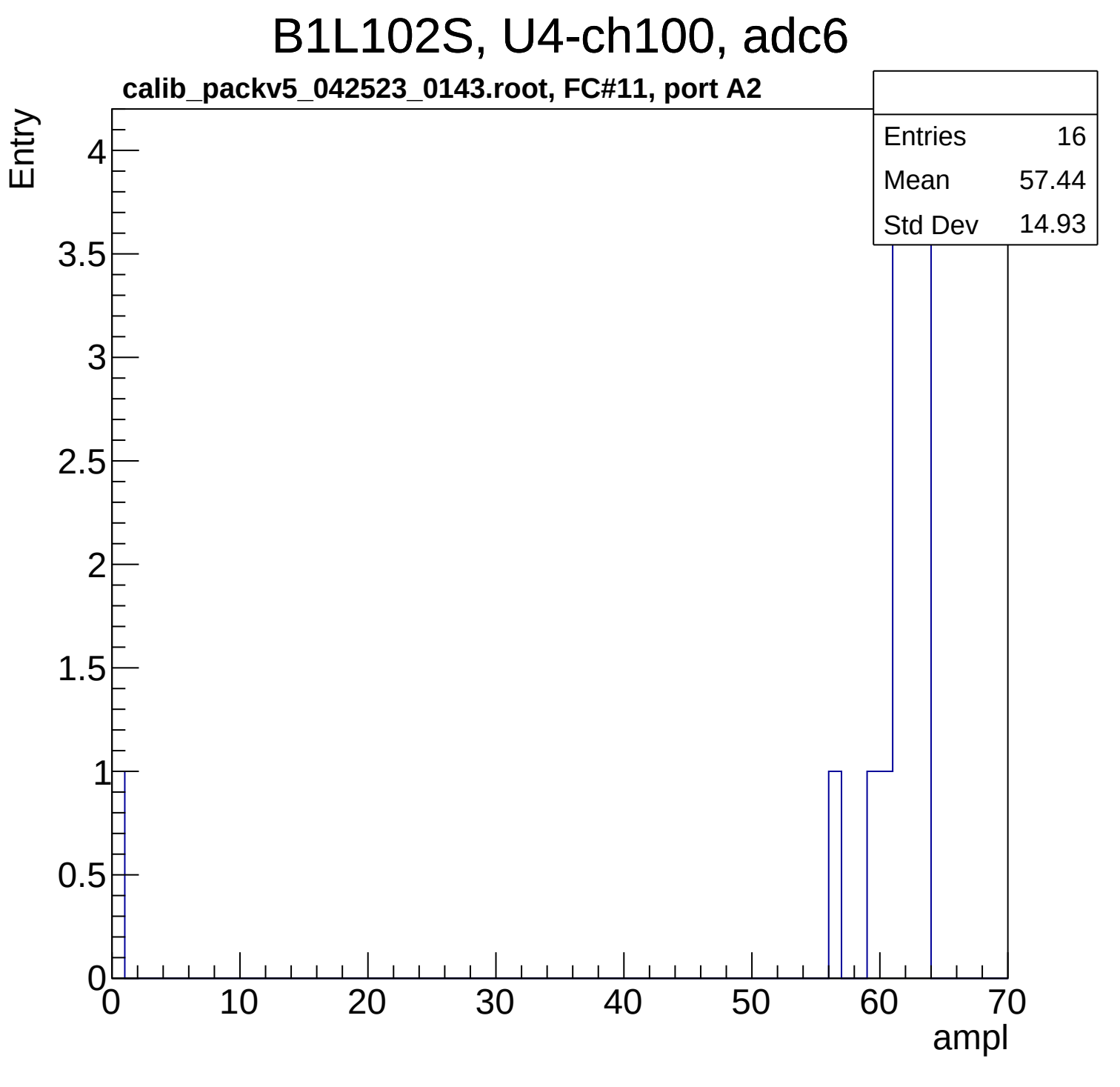
B1L102S, U4-ch100, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 16
Mean 57.44
Std Dev 14.93
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
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60
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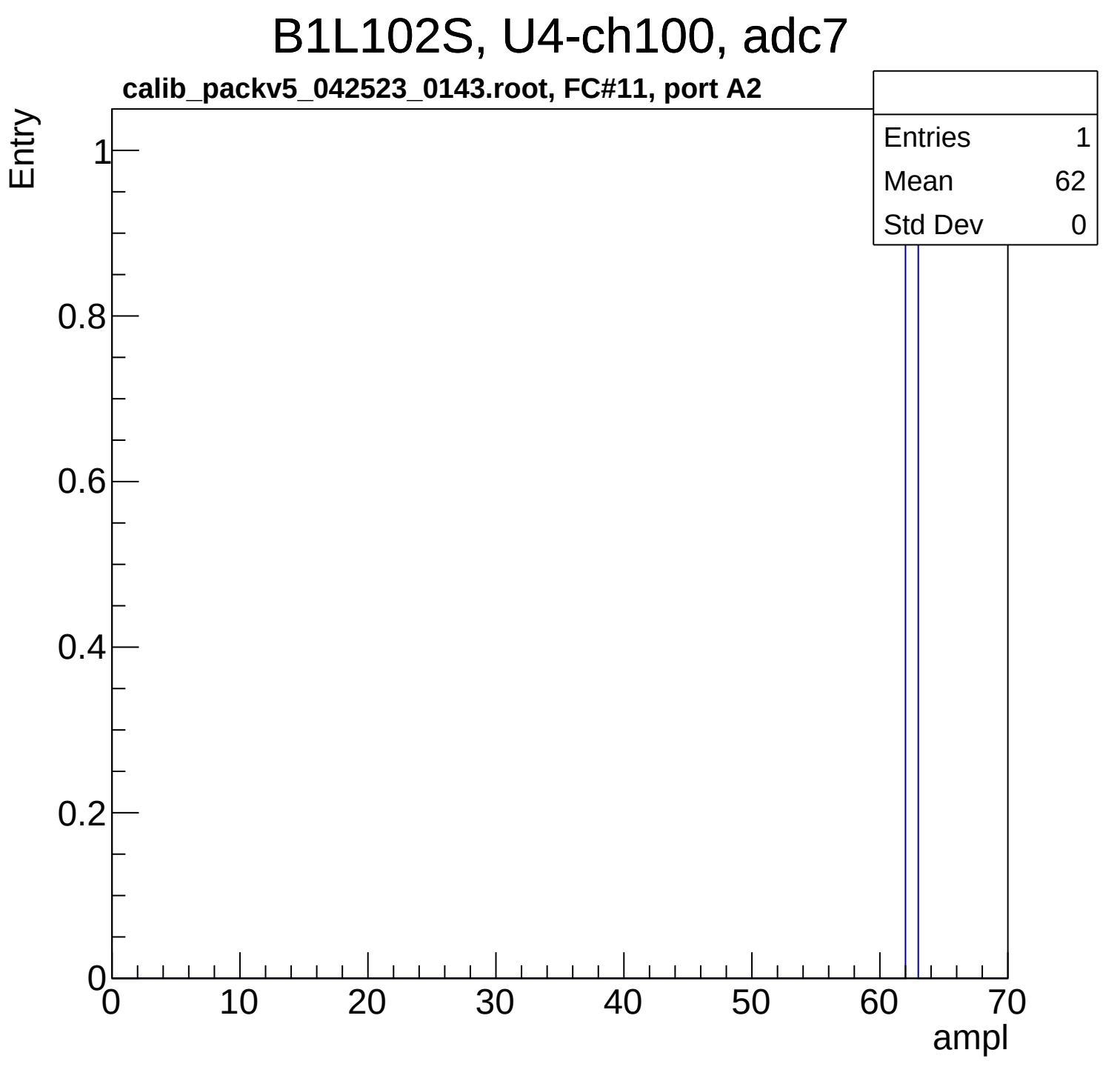
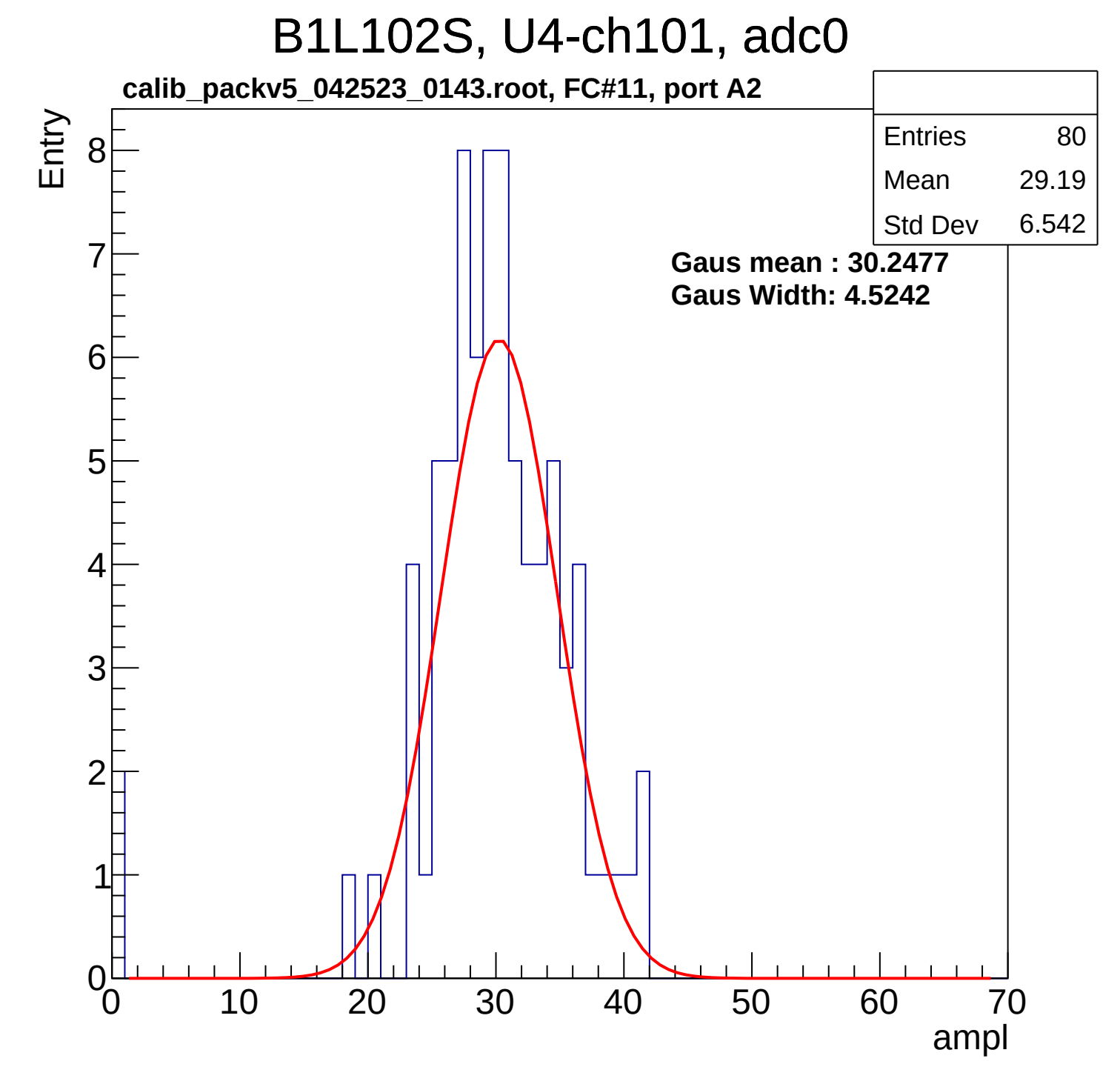
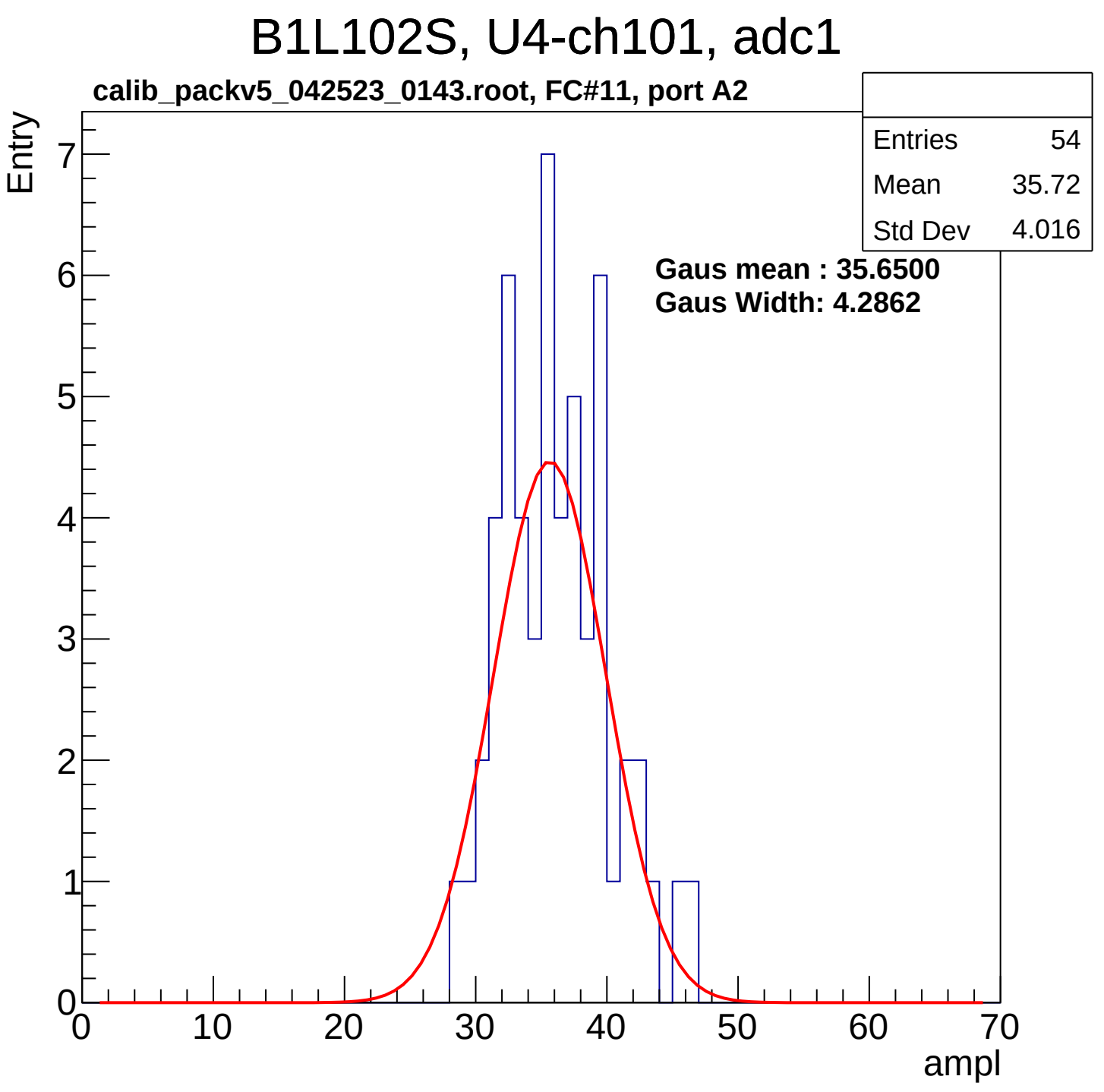

B1L102S, U4-ch100, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch101, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 80
Mean 29.19
Std Dev 6.542
Gaus mean : 30.2477
Gaus Width: 4.5242
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch101, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 35.72
Std Dev 4.016
Gaus mean : 35.6500
Gaus Width: 4.2862
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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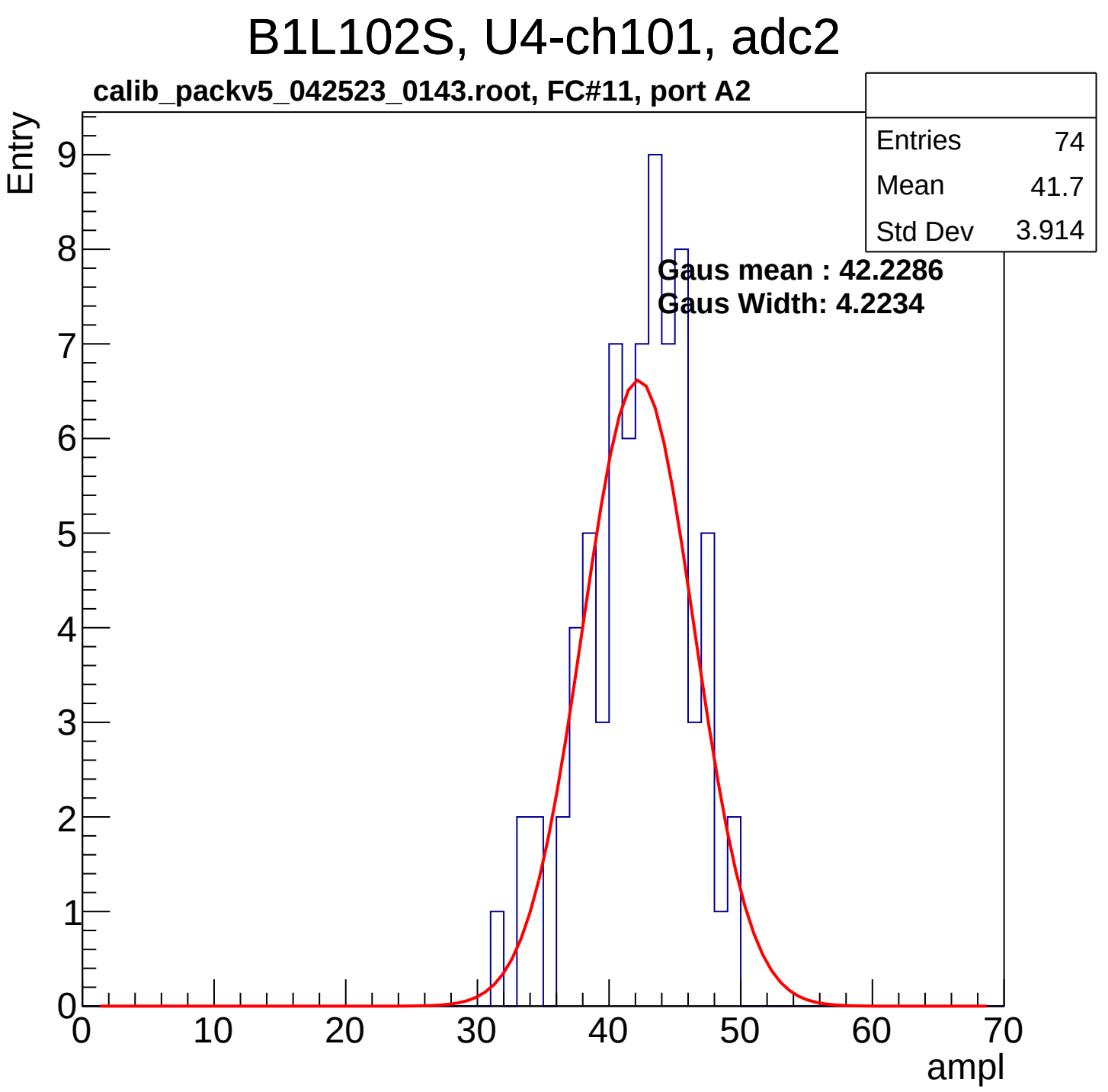
B1L102S, U4-ch101, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 41.7
Std Dev 3.914
Gaus mean : 42.2286
Gaus Width: 4.2234
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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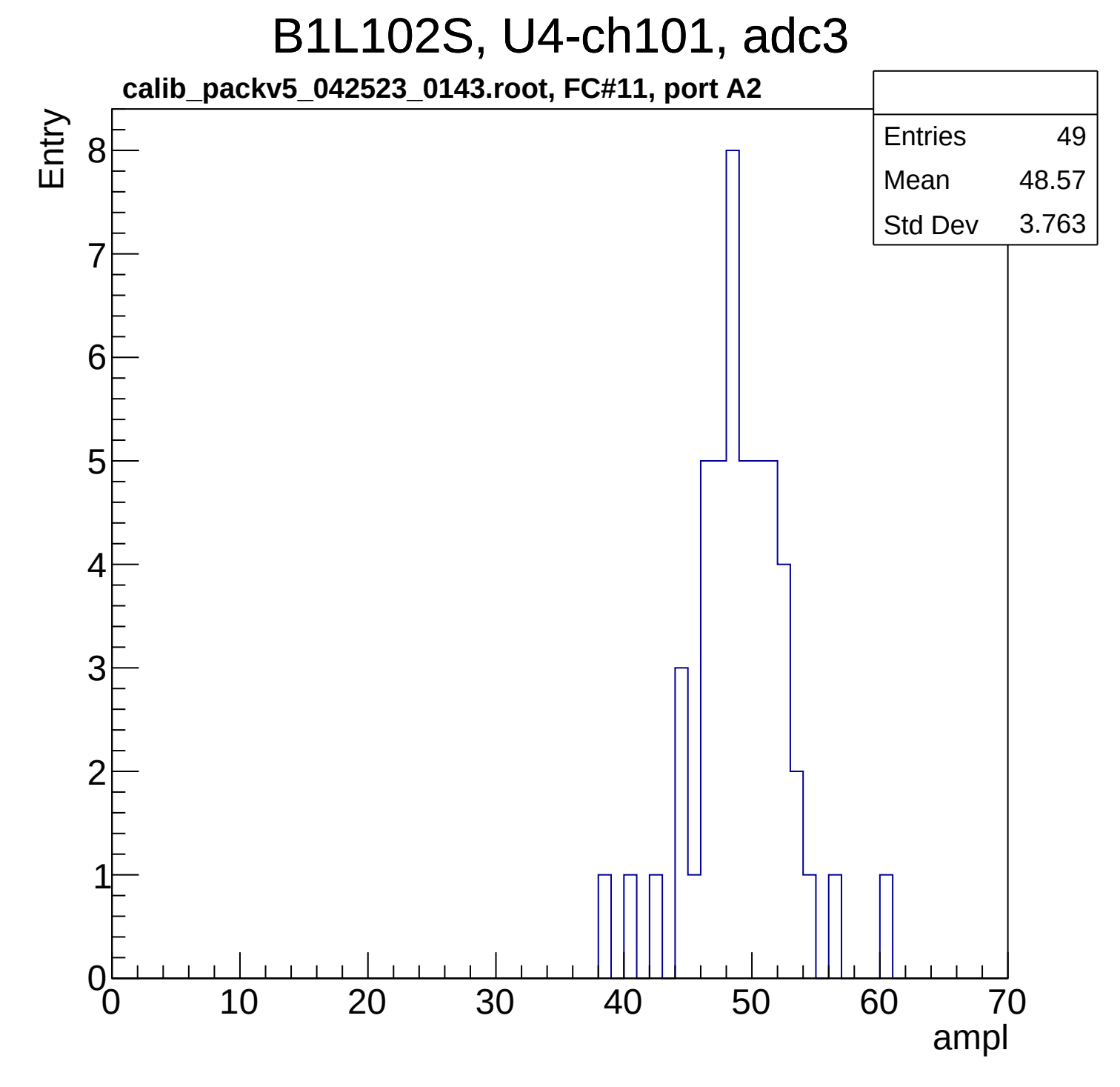
B1L102S, U4-ch101, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 48.57
Std Dev 3.763
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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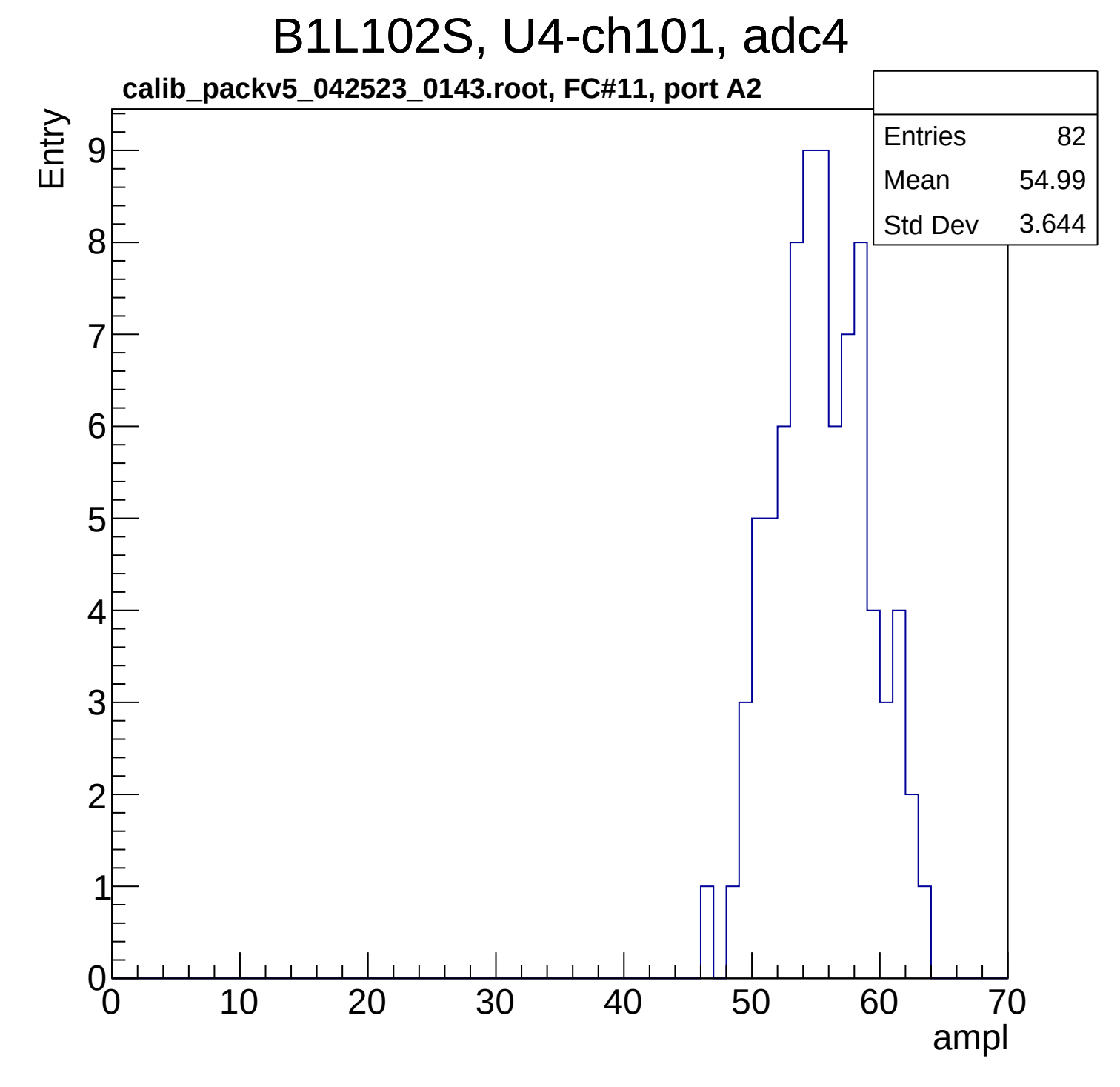
B1L102S, U4-ch101, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 82
Mean 54.99
Std Dev 3.644
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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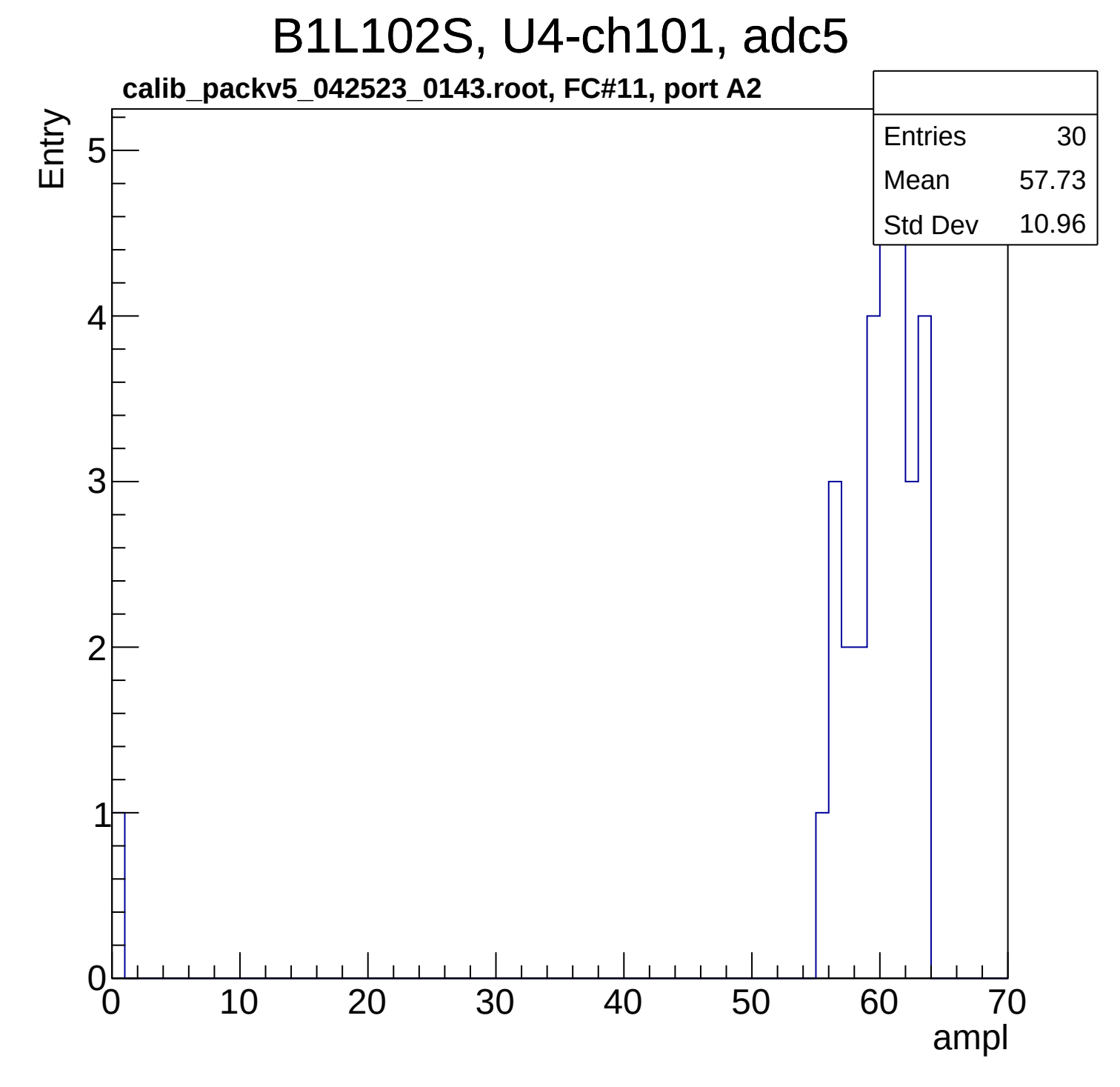
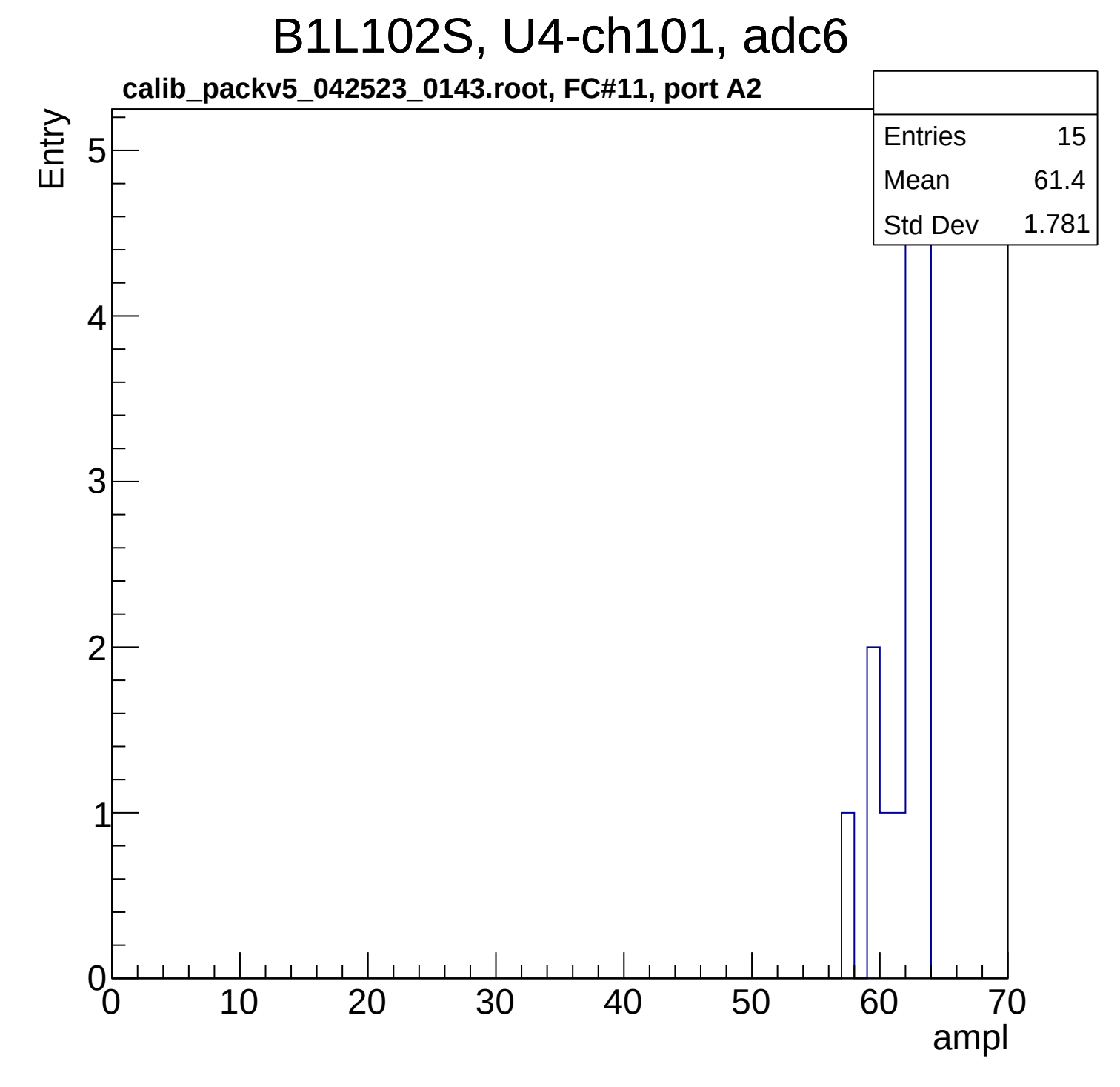
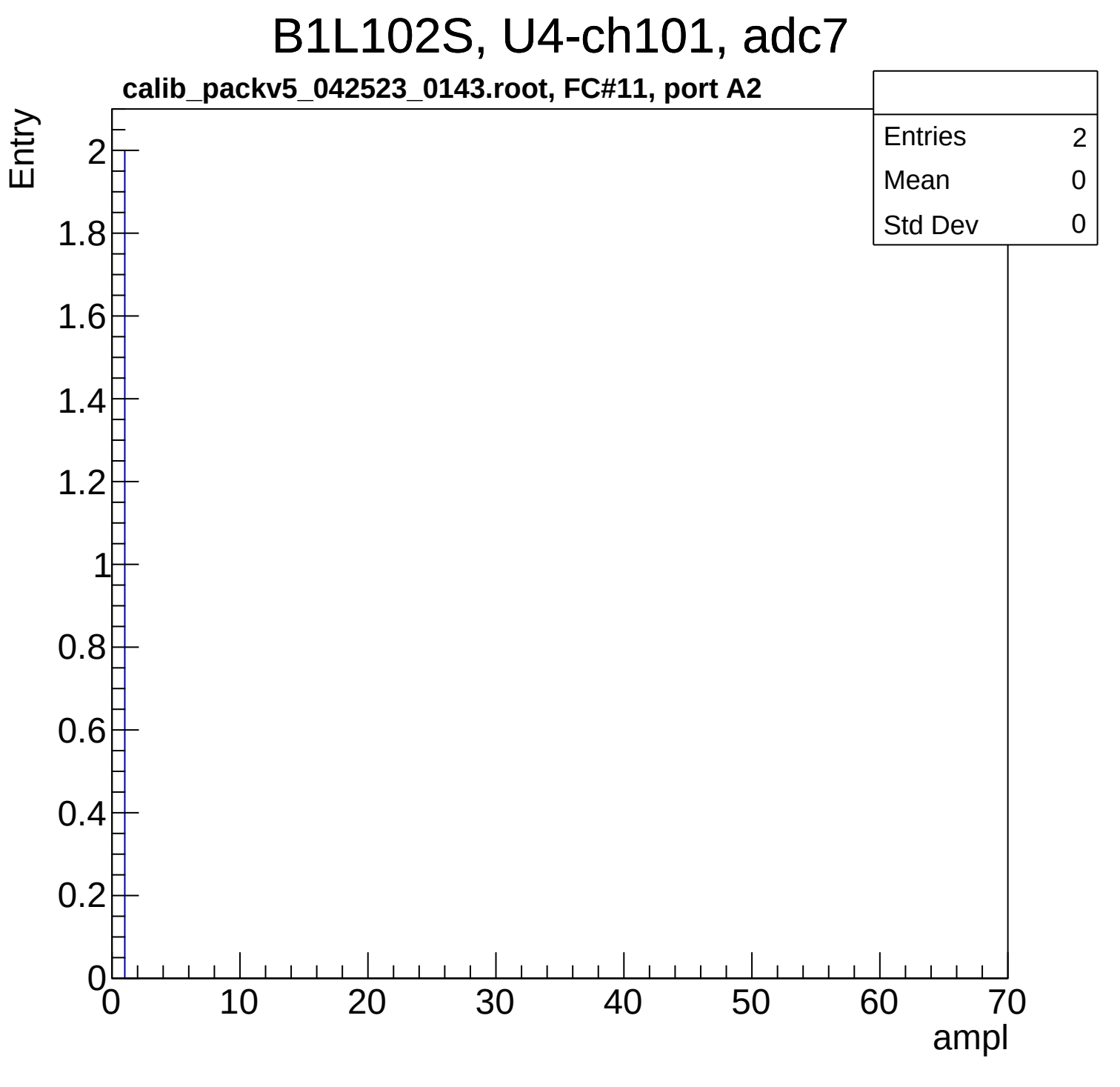
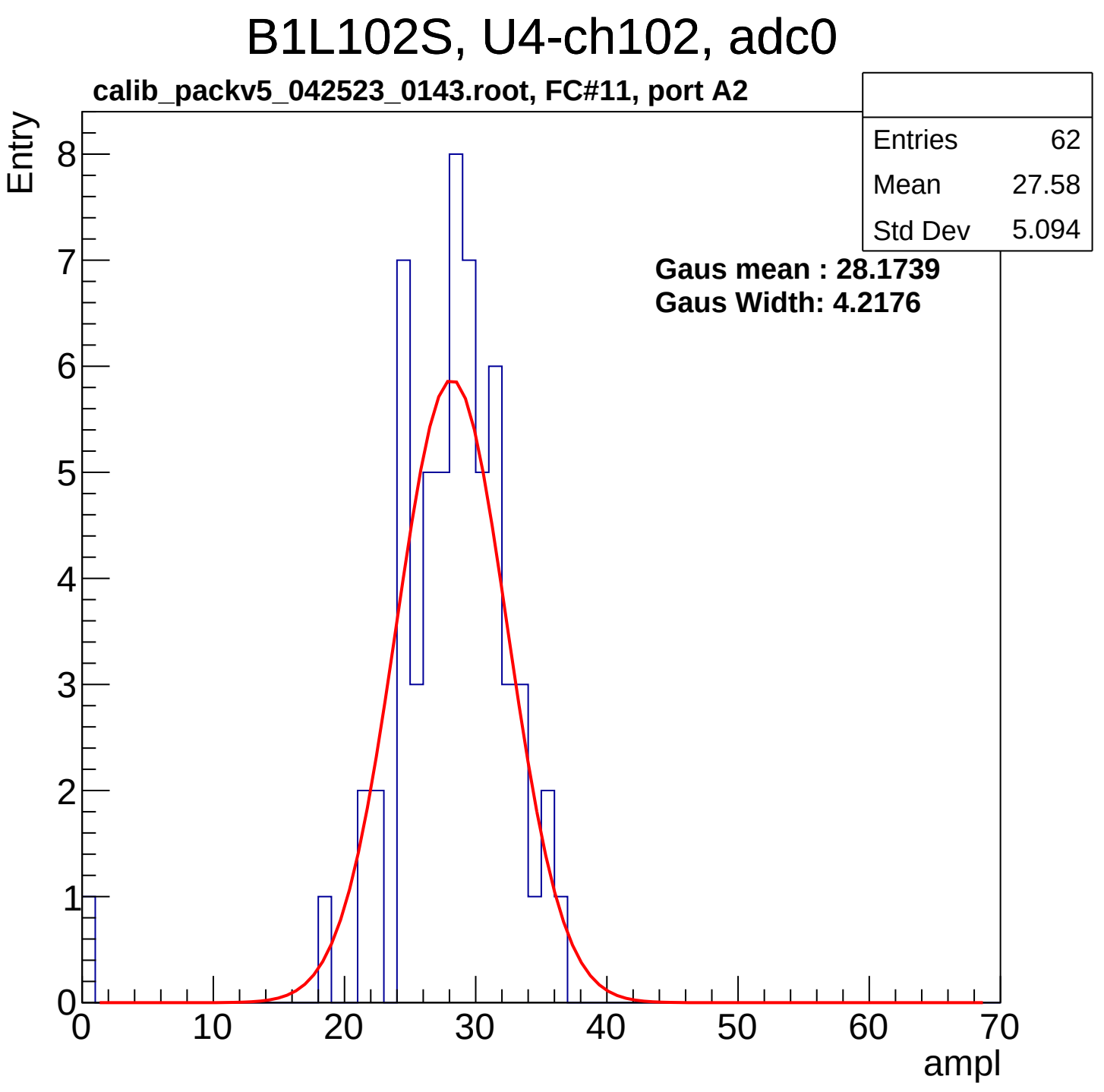
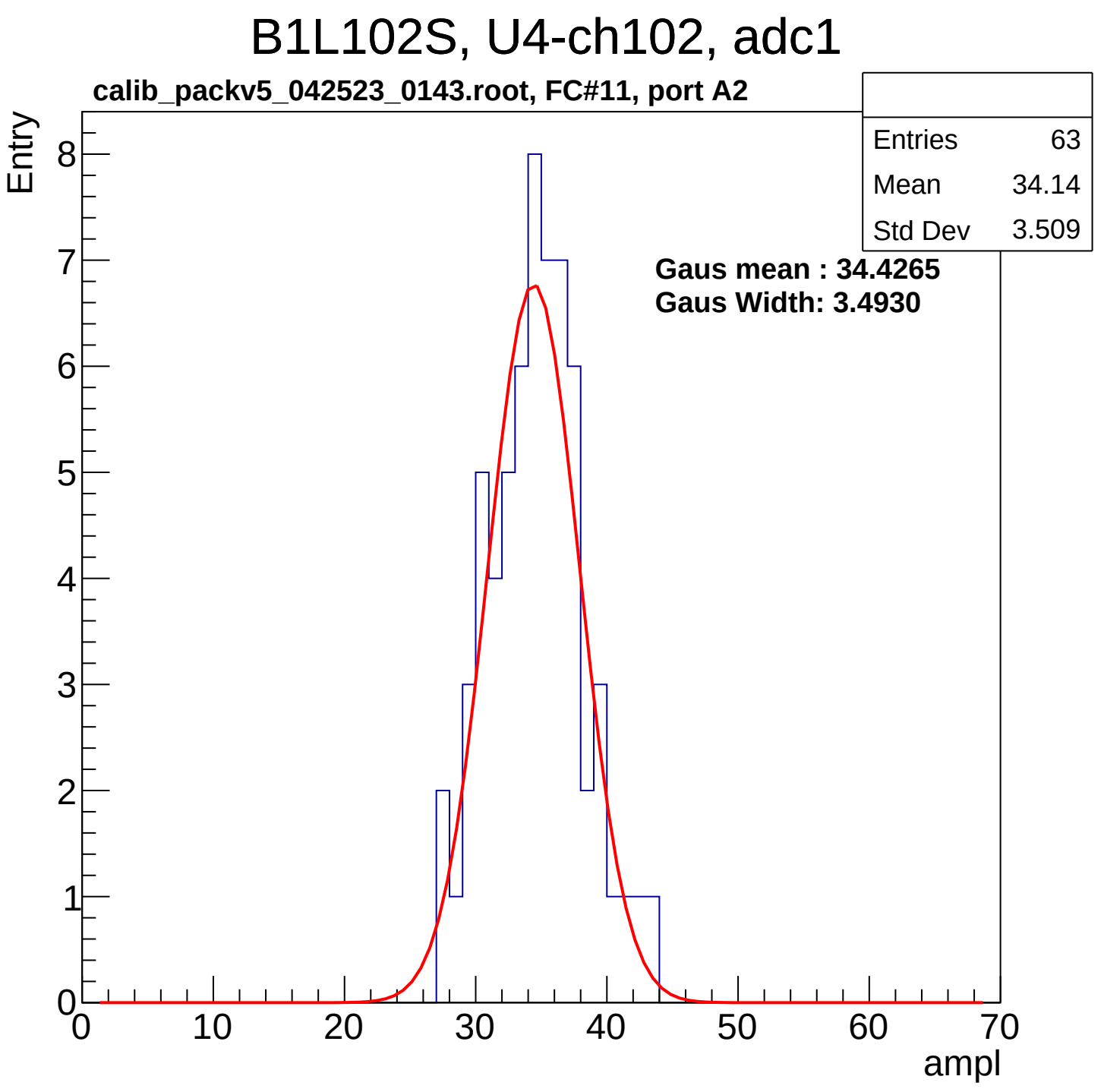
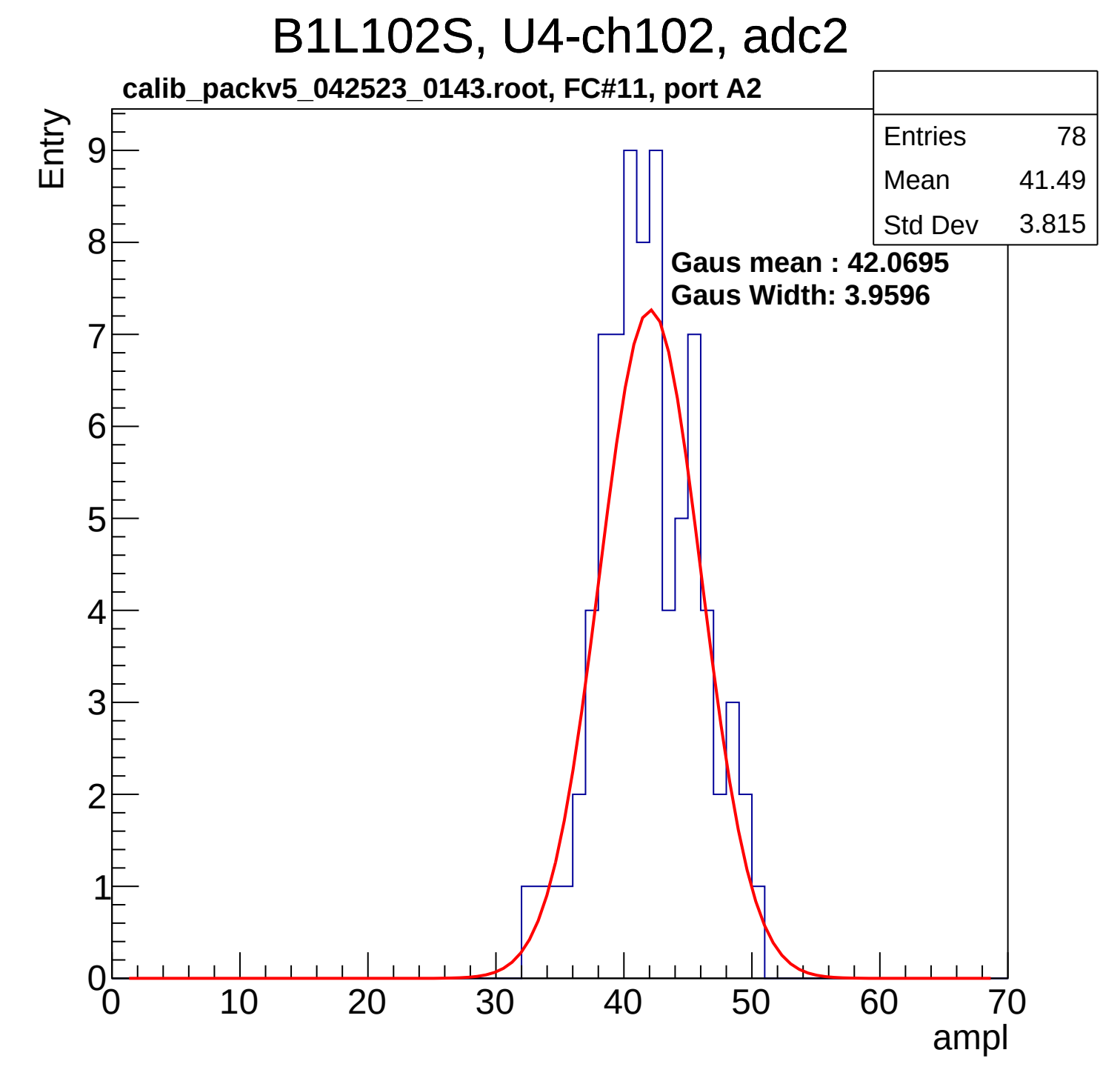

B1L102S, U4-ch101, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 30
Mean 57.73
Std Dev 10.96
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

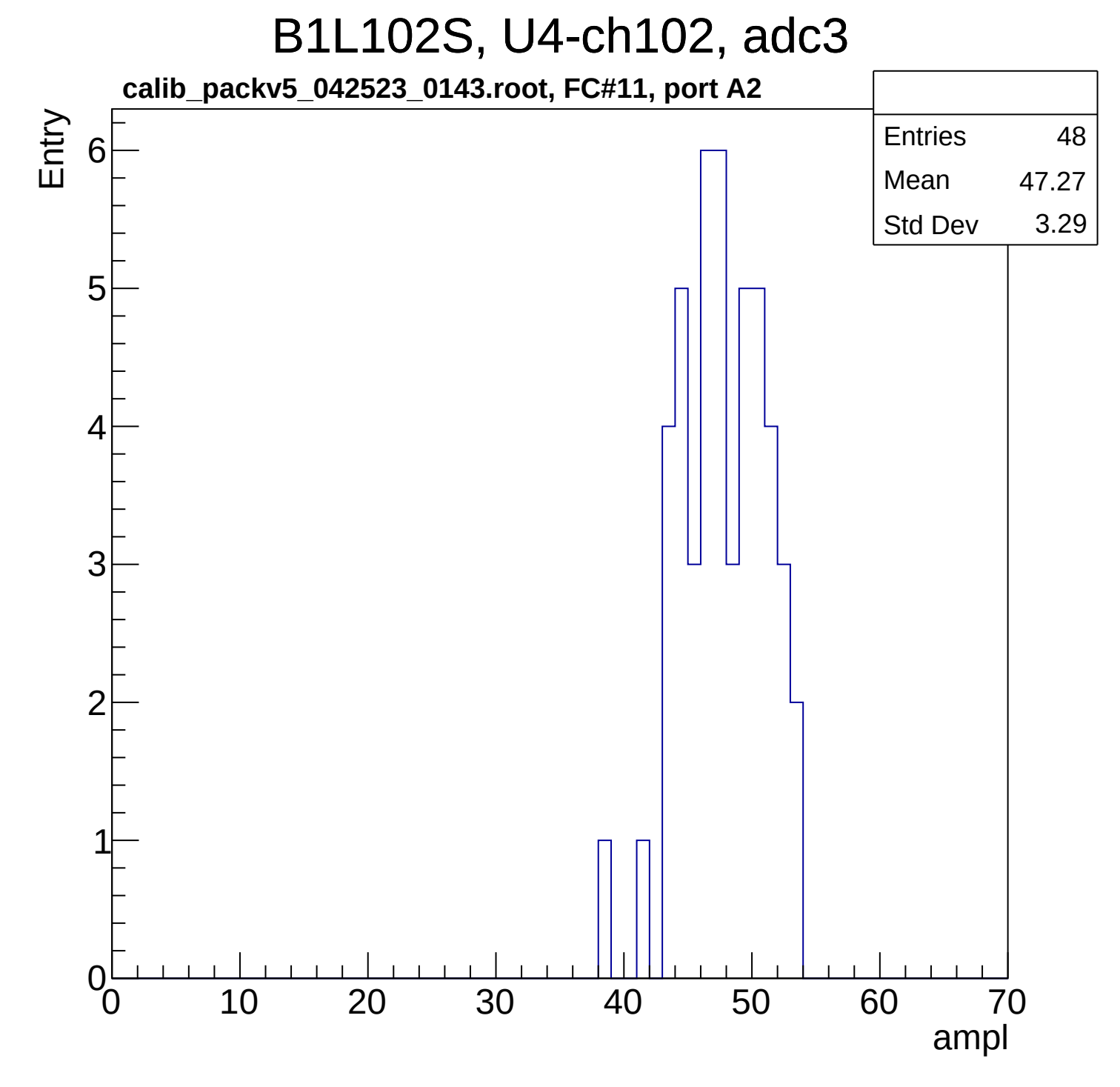

B1L102S, U4-ch101, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 15
Mean 61.4
Std Dev 1.781
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

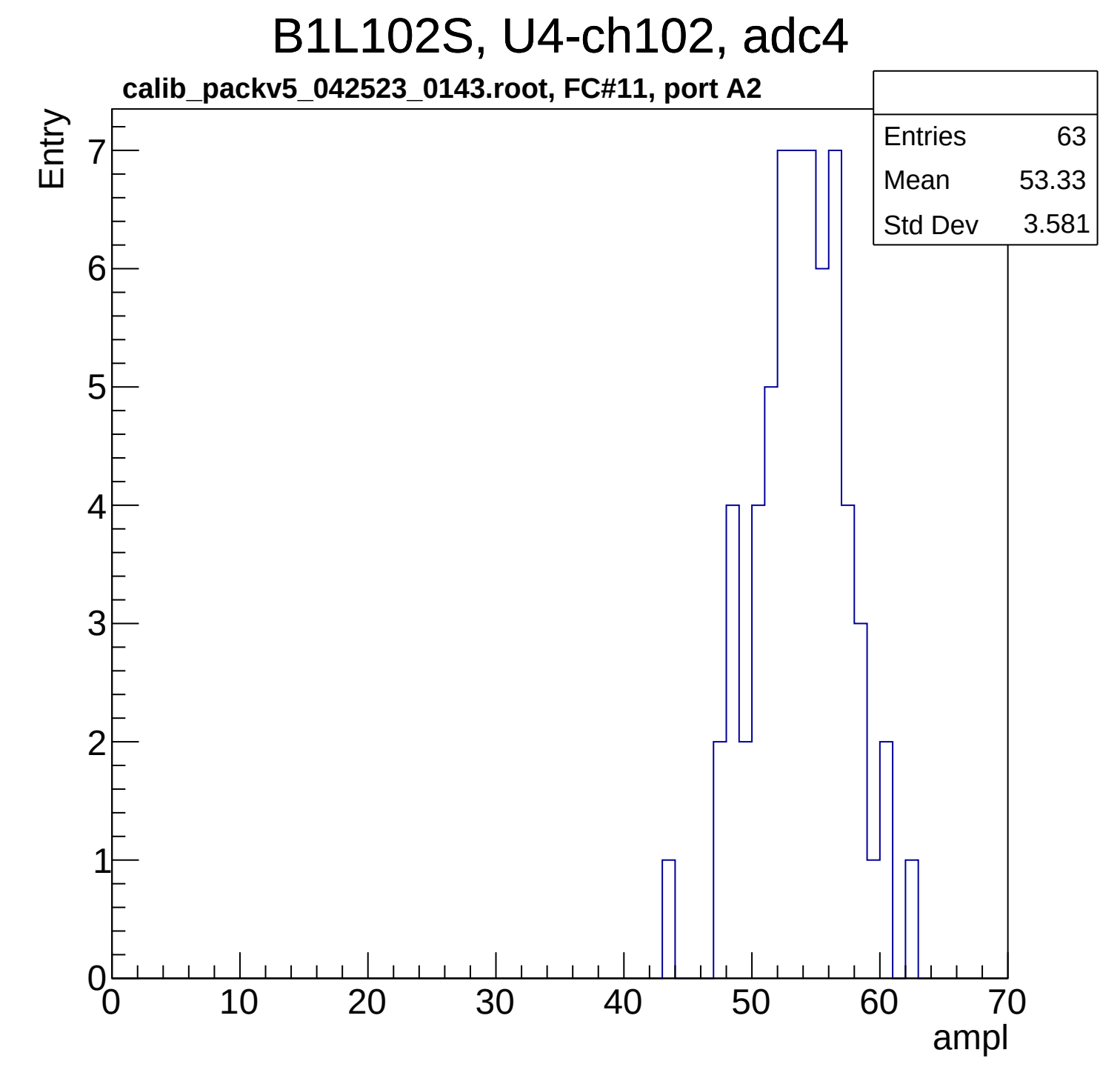

B1L102S, U4-ch101, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

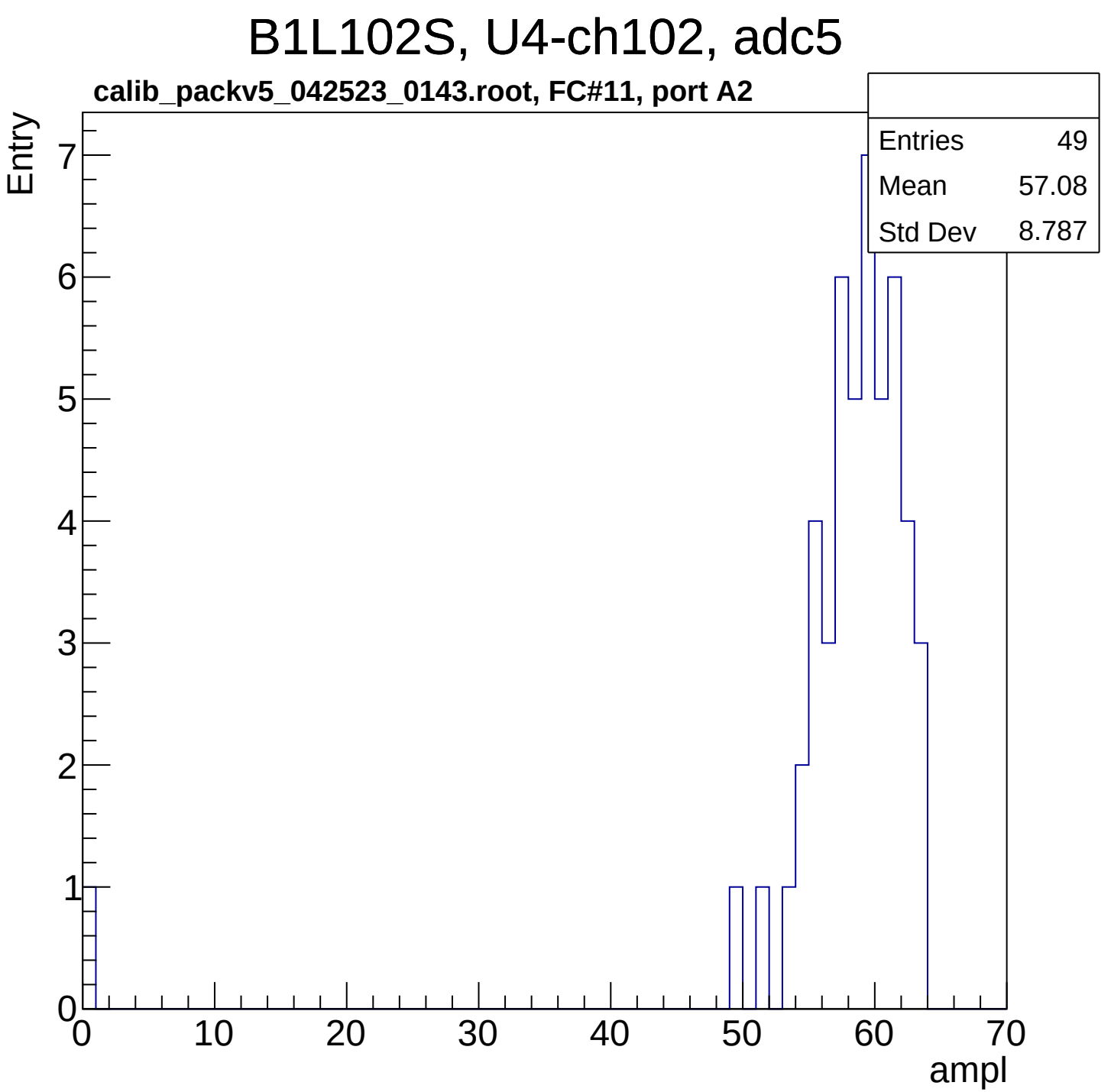

B1L102S, U4-ch102, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 27.58
Std Dev 5.094
Gaus mean : 28.1739
Gaus Width: 4.2176
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

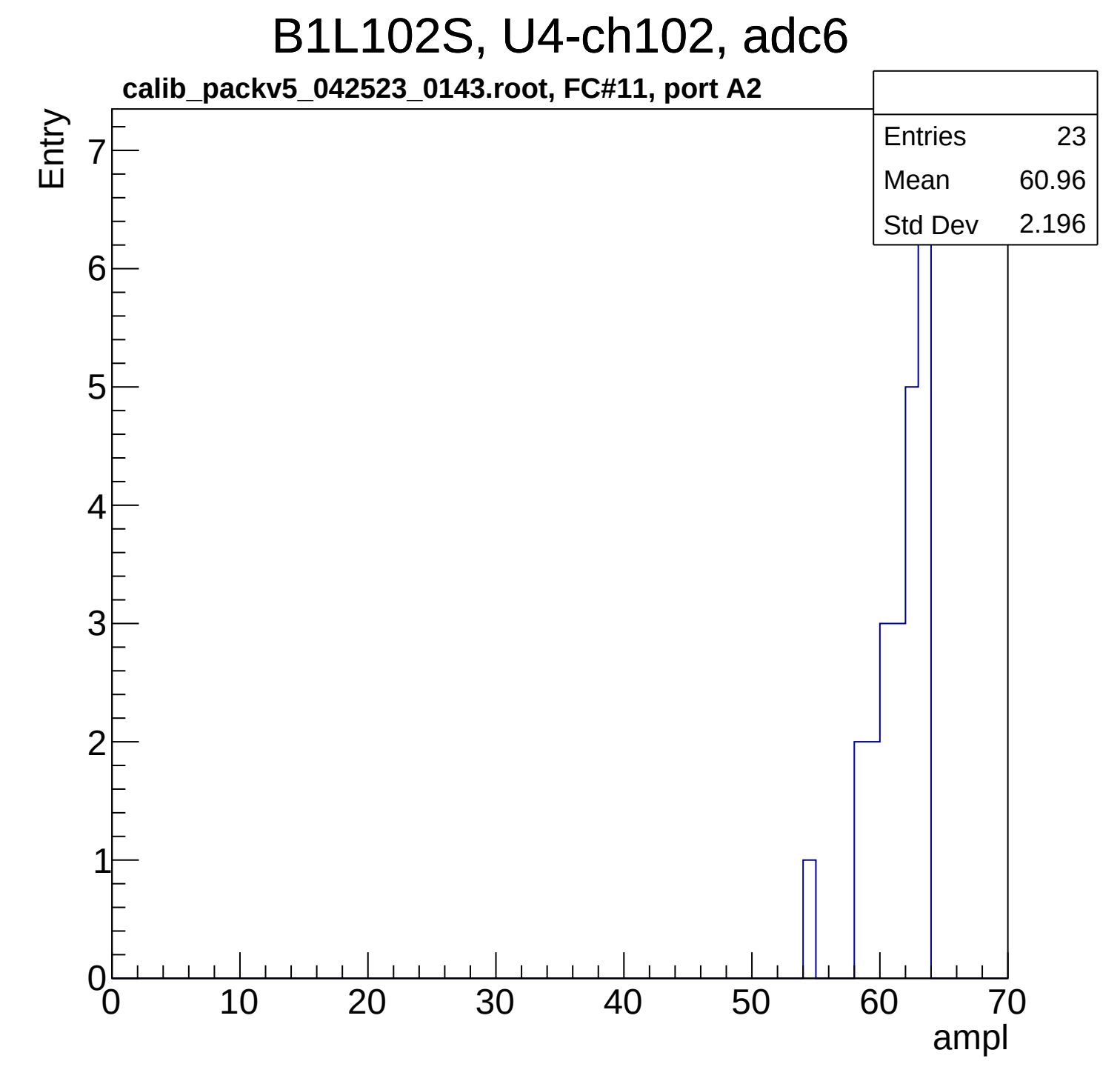

B1L102S, U4-ch102, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 34.14
Std Dev 3.509
Gaus mean : 34.4265
Gaus Width: 3.4930
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

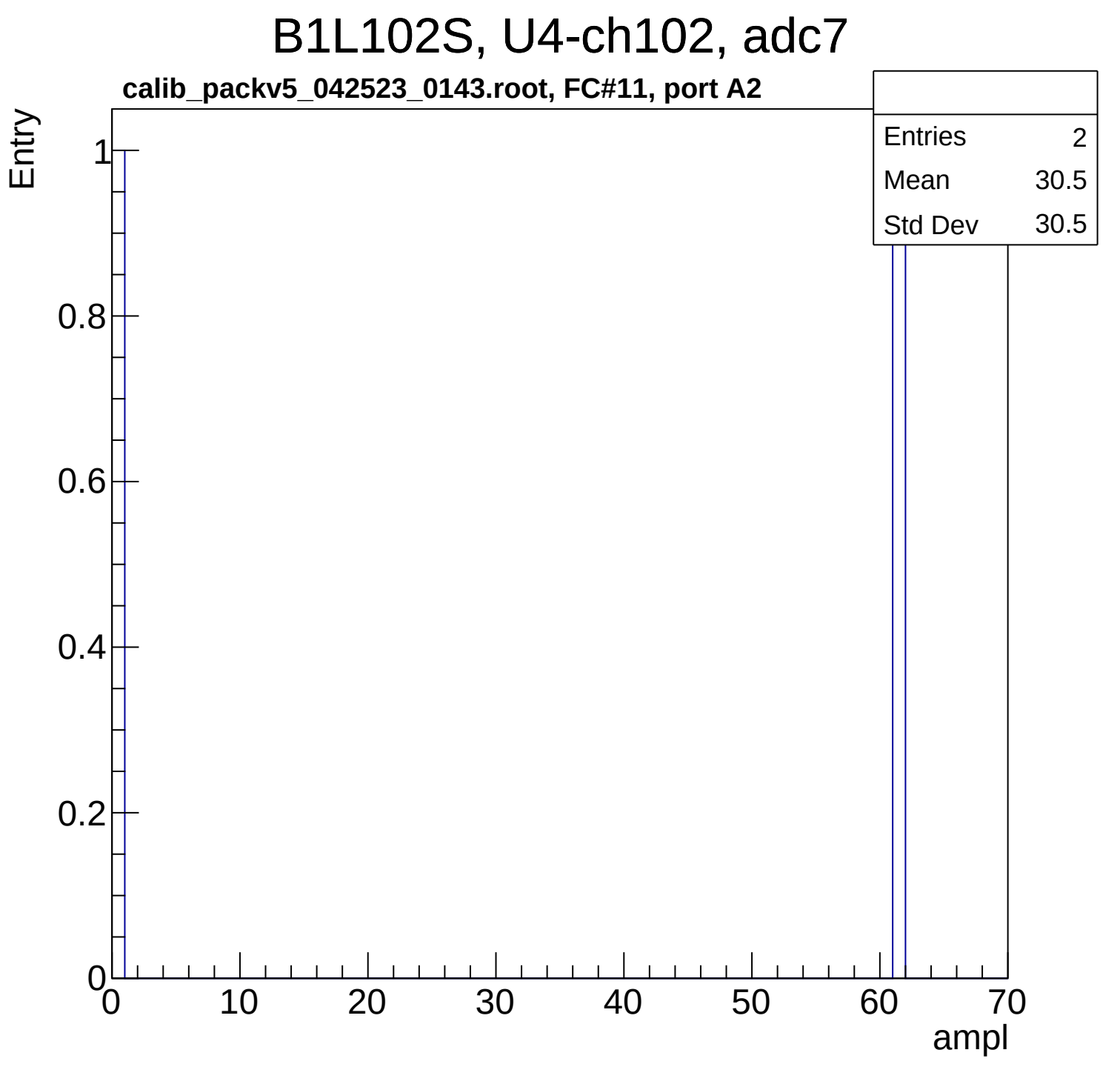

B1L102S, U4-ch102, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 78
Mean 41.49
Std Dev 3.815
Gaus mean : 42.0695
Gaus Width: 3.9596
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch102, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 48
Mean 47.27
Std Dev 3.29
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch102, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 53.33
Std Dev 3.581
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch102, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 57.08
Std Dev 8.787
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch102, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 23
Mean 60.96
Std Dev 2.196
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch102, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 30.5
Std Dev 30.5
Entry
1
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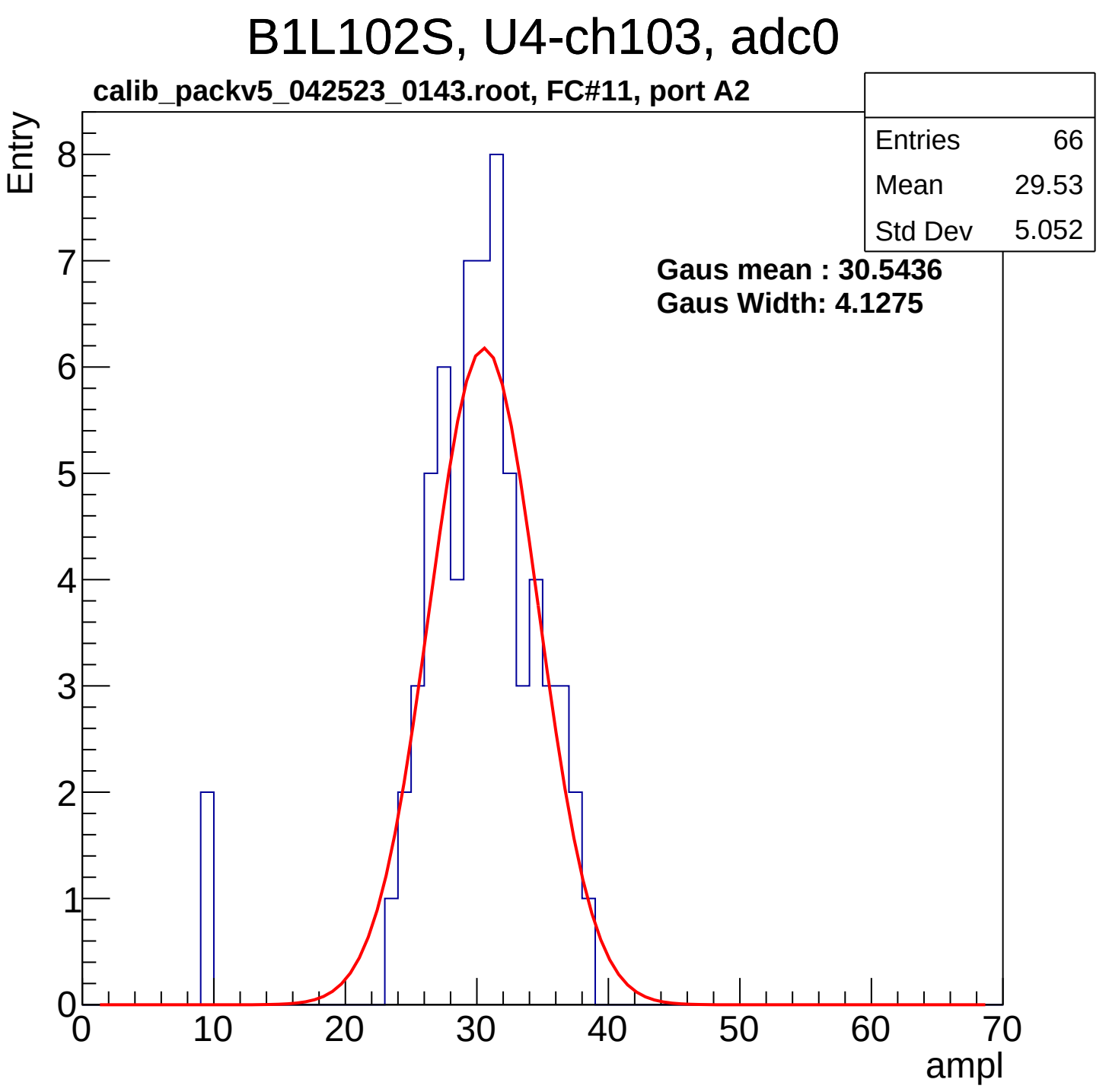
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch103, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 29.53
Std Dev 5.052
Gaus mean : 30.5436
Gaus Width: 4.1275
Entry
ampl
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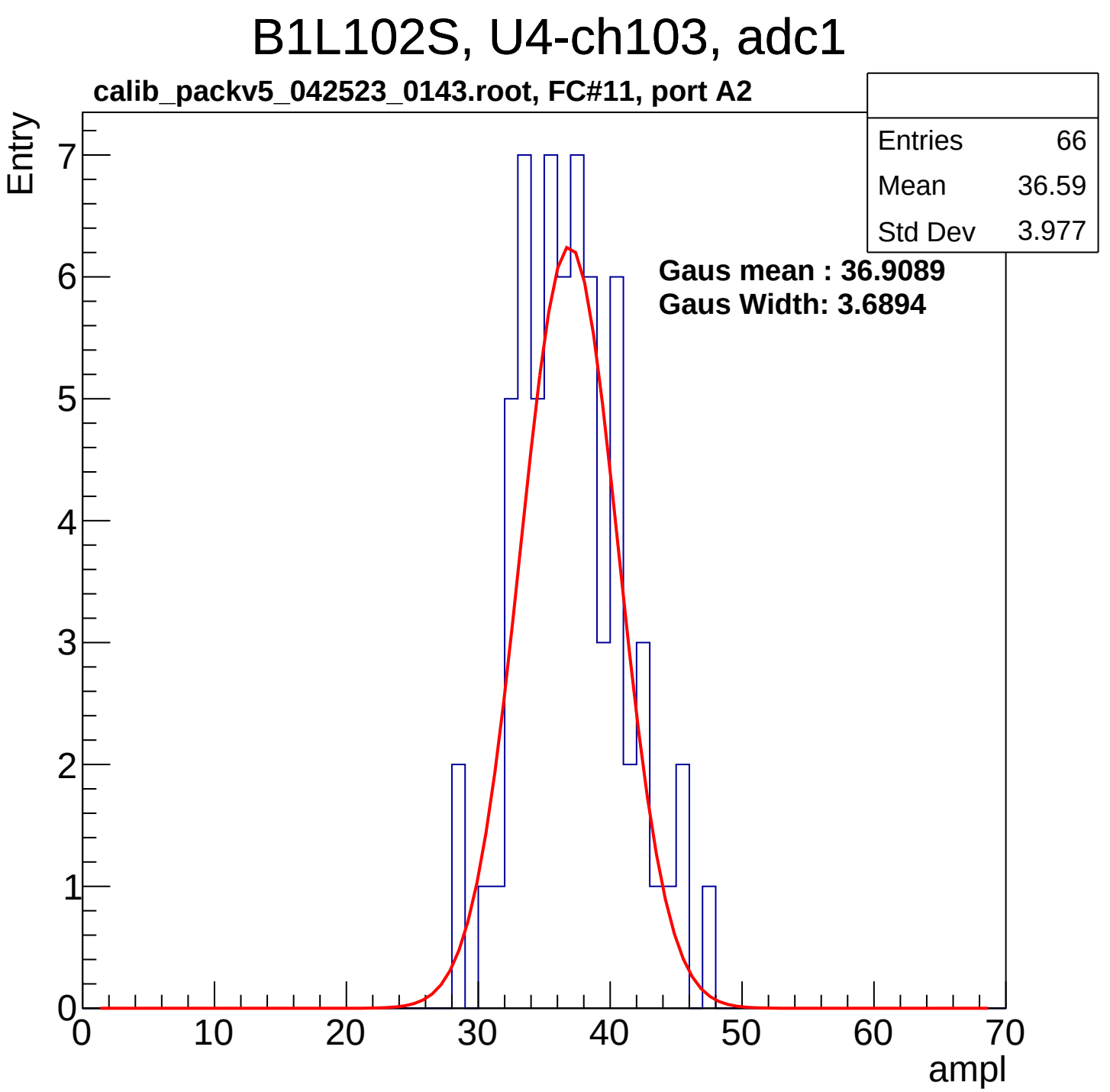
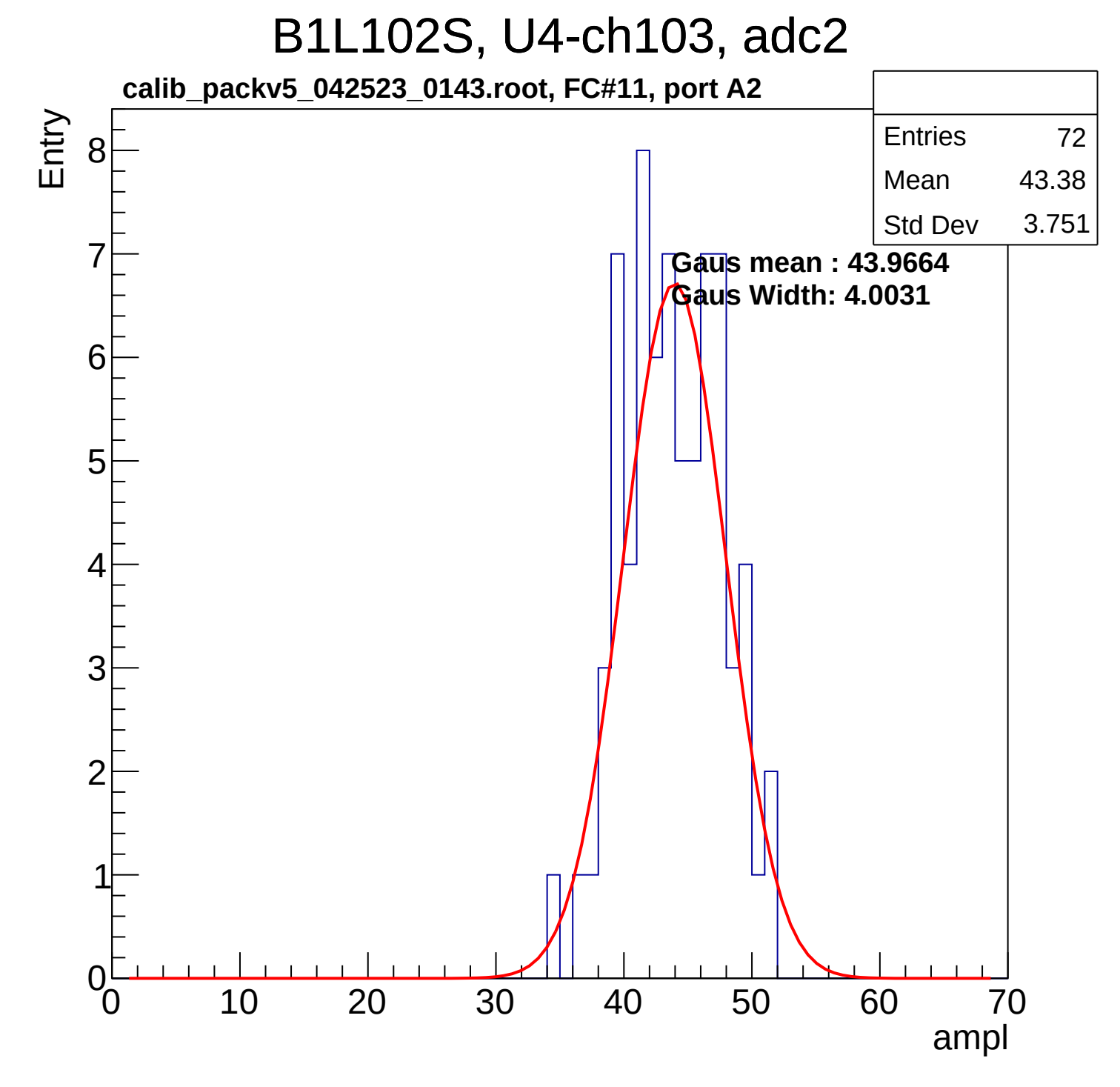
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch103, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 36.59
Std Dev 3.977
Gaus mean : 36.9089
Gaus Width: 3.6894
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch103, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 72
Mean 43.38
Std Dev 3.751
Gaus mean : 43.9664
Gaus Width: 4.0031
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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20
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40
50
60
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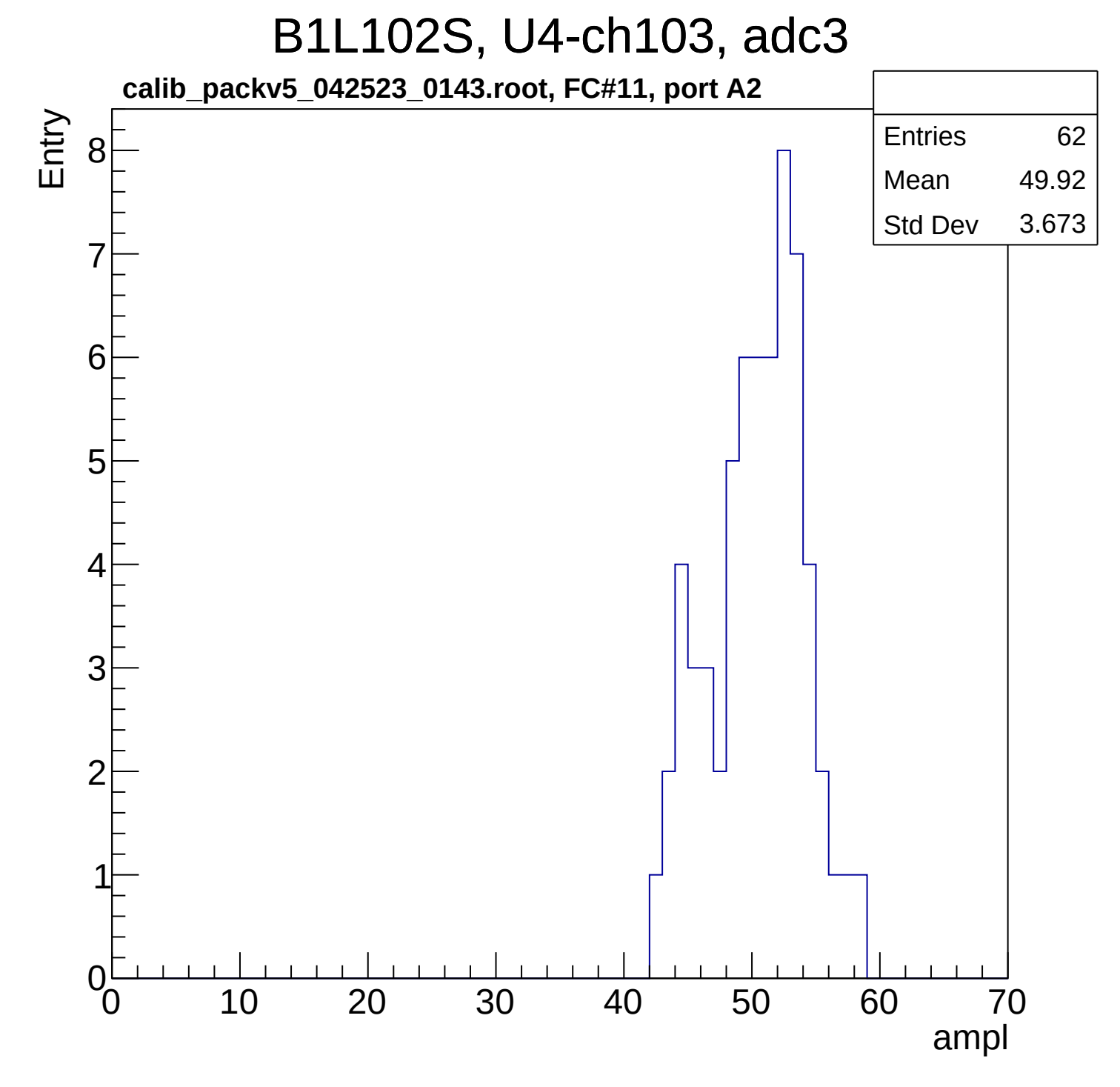
B1L102S, U4-ch103, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 49.92
Std Dev 3.673
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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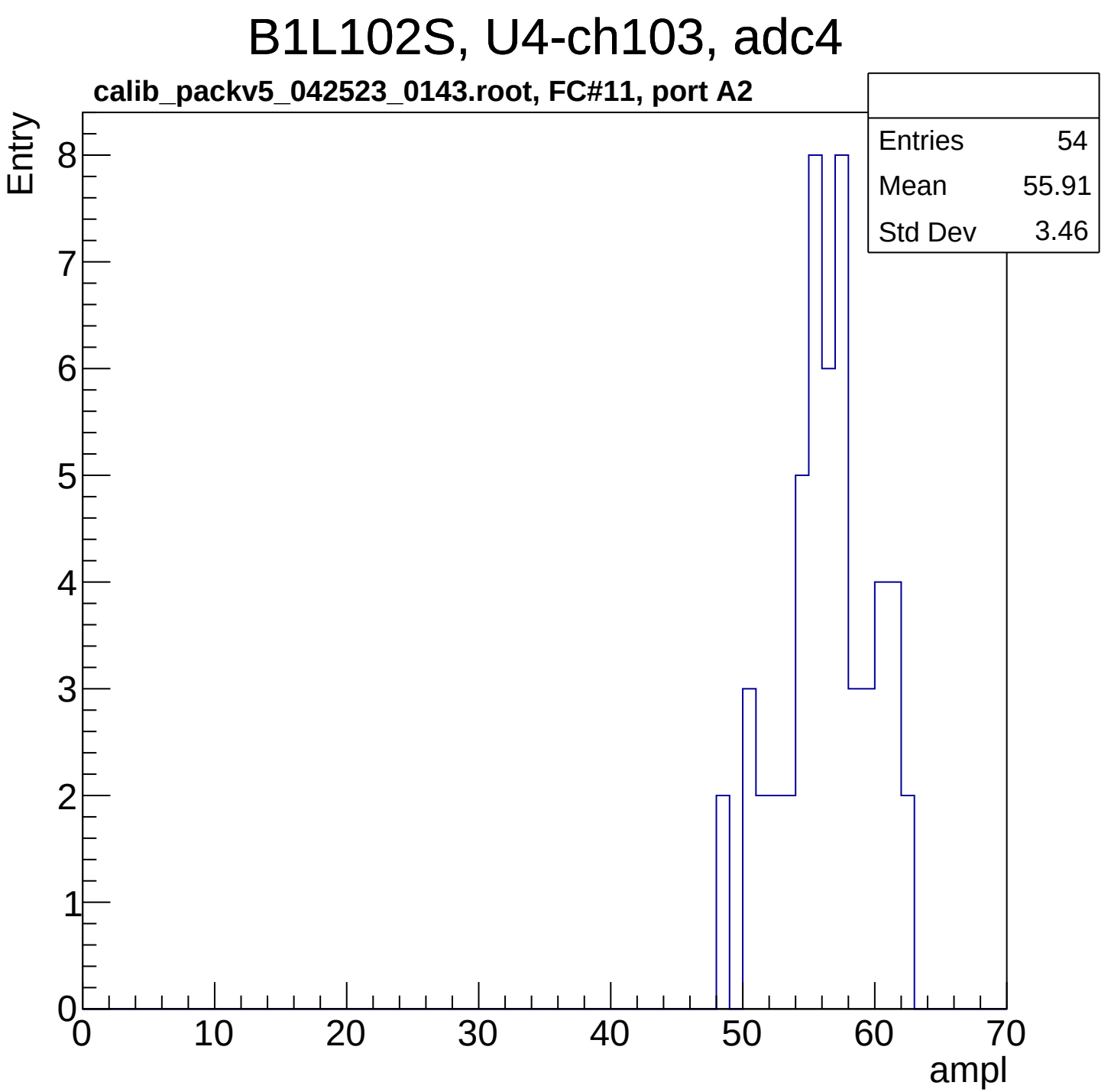
B1L102S, U4-ch103, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 55.91
Std Dev 3.46
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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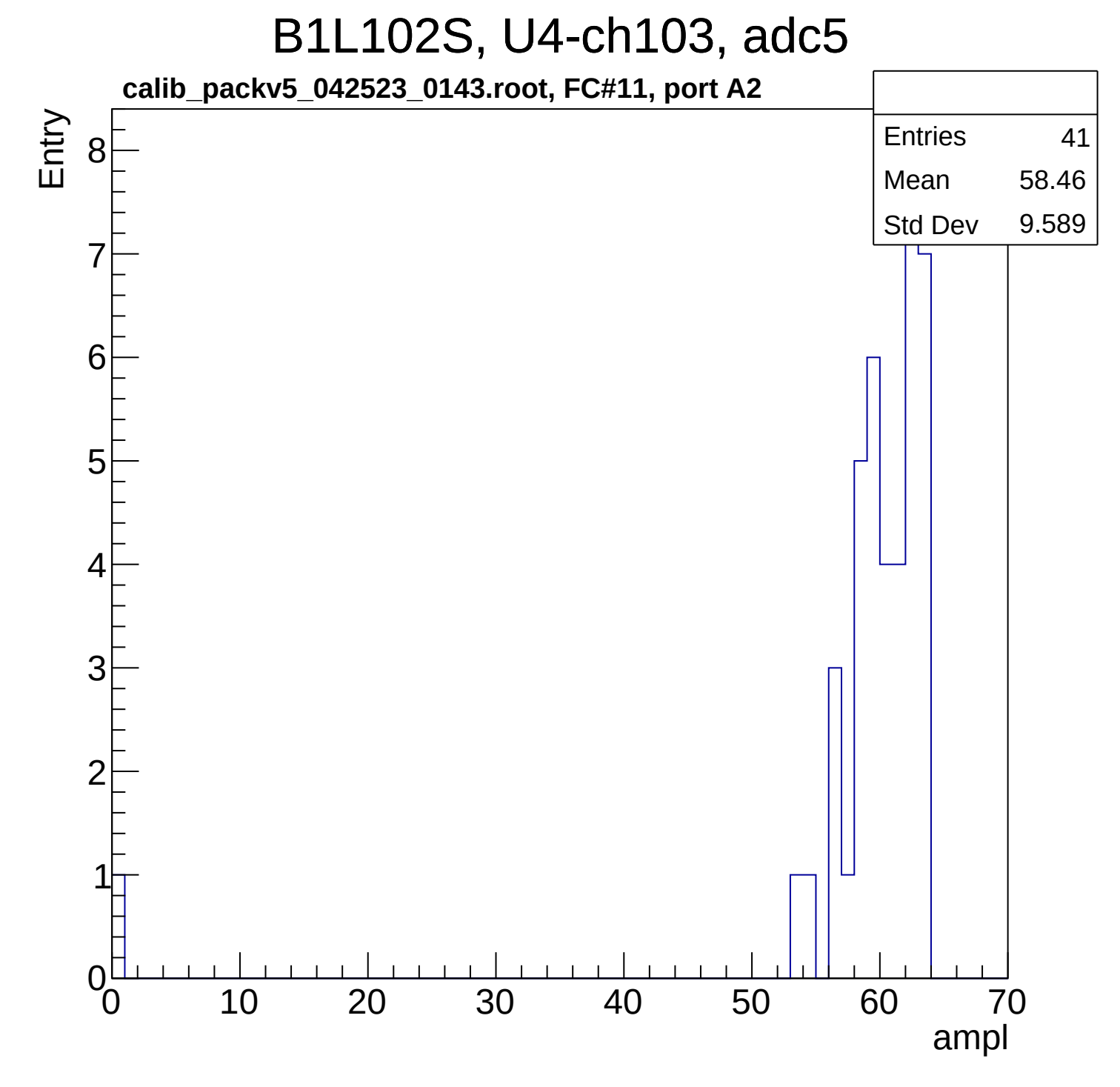
B1L102S, U4-ch103, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 41
Mean 58.46
Std Dev 9.589
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
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60
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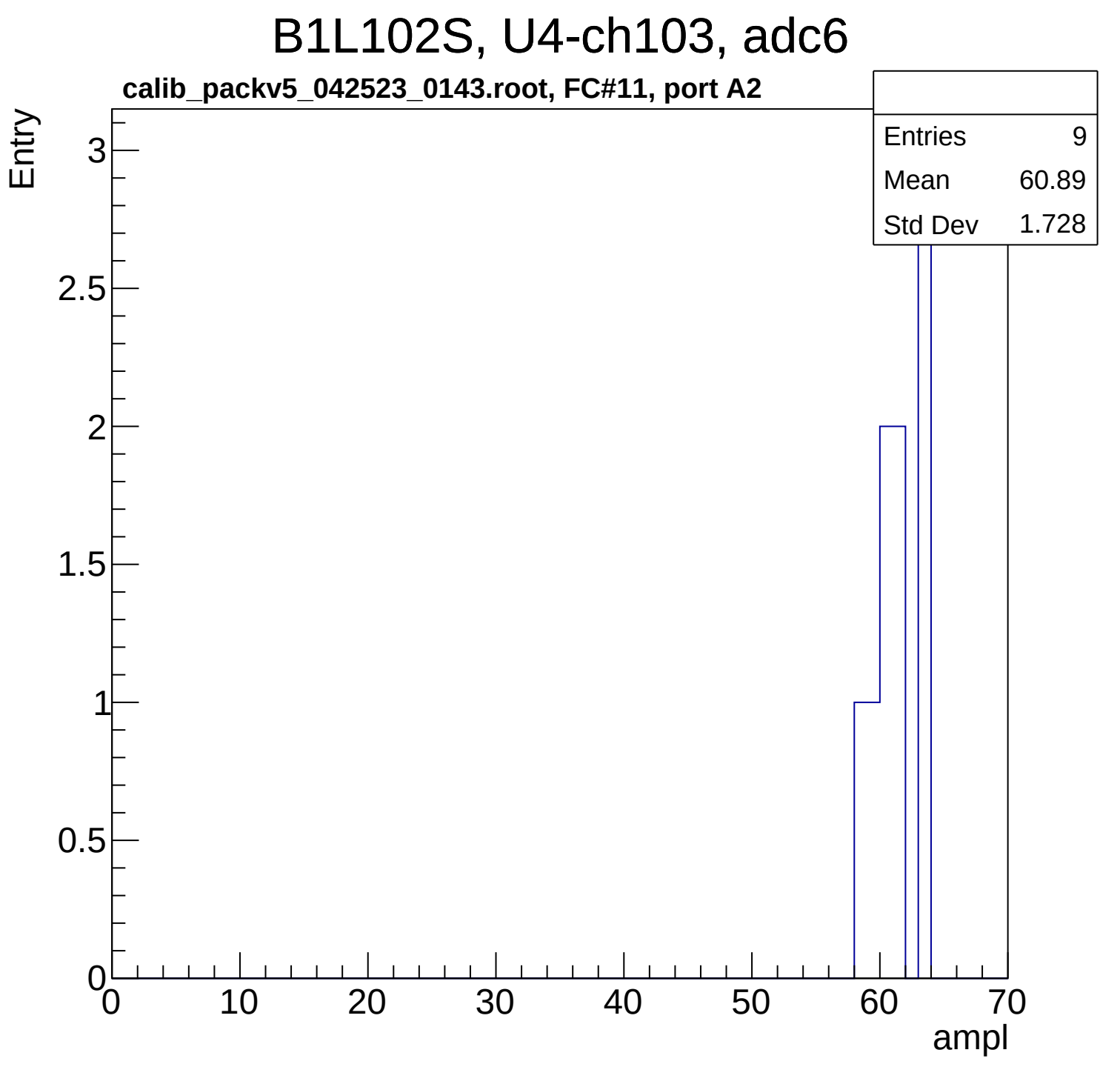
B1L102S, U4-ch103, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 9
Mean 60.89
Std Dev 1.728
Entry
ampl
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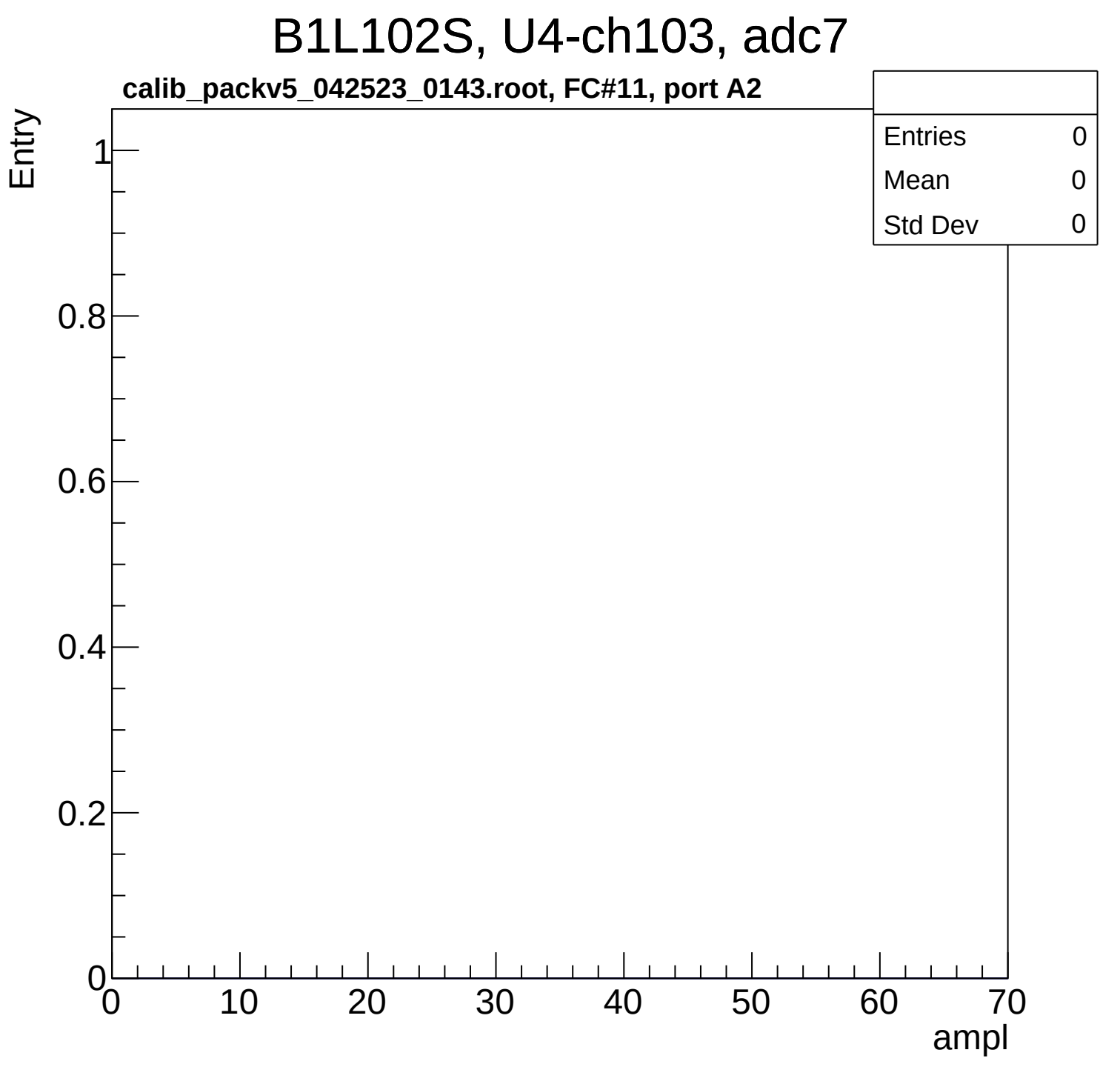
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U4-ch103, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 0
Mean 0
Std Dev 0
Entry
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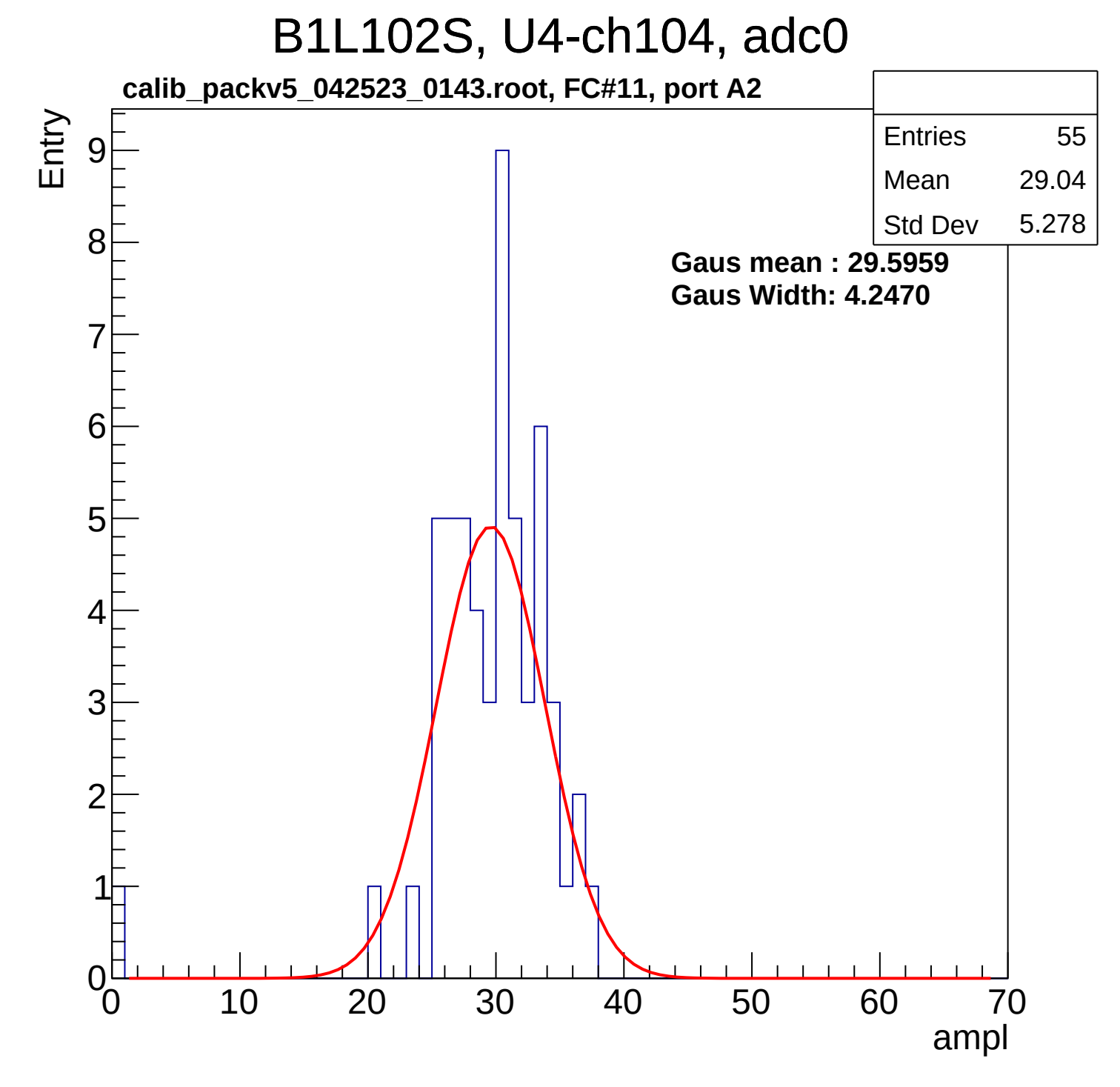
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch104, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 29.04
Std Dev 5.278
Gaus mean : 29.5959
Gaus Width: 4.2470
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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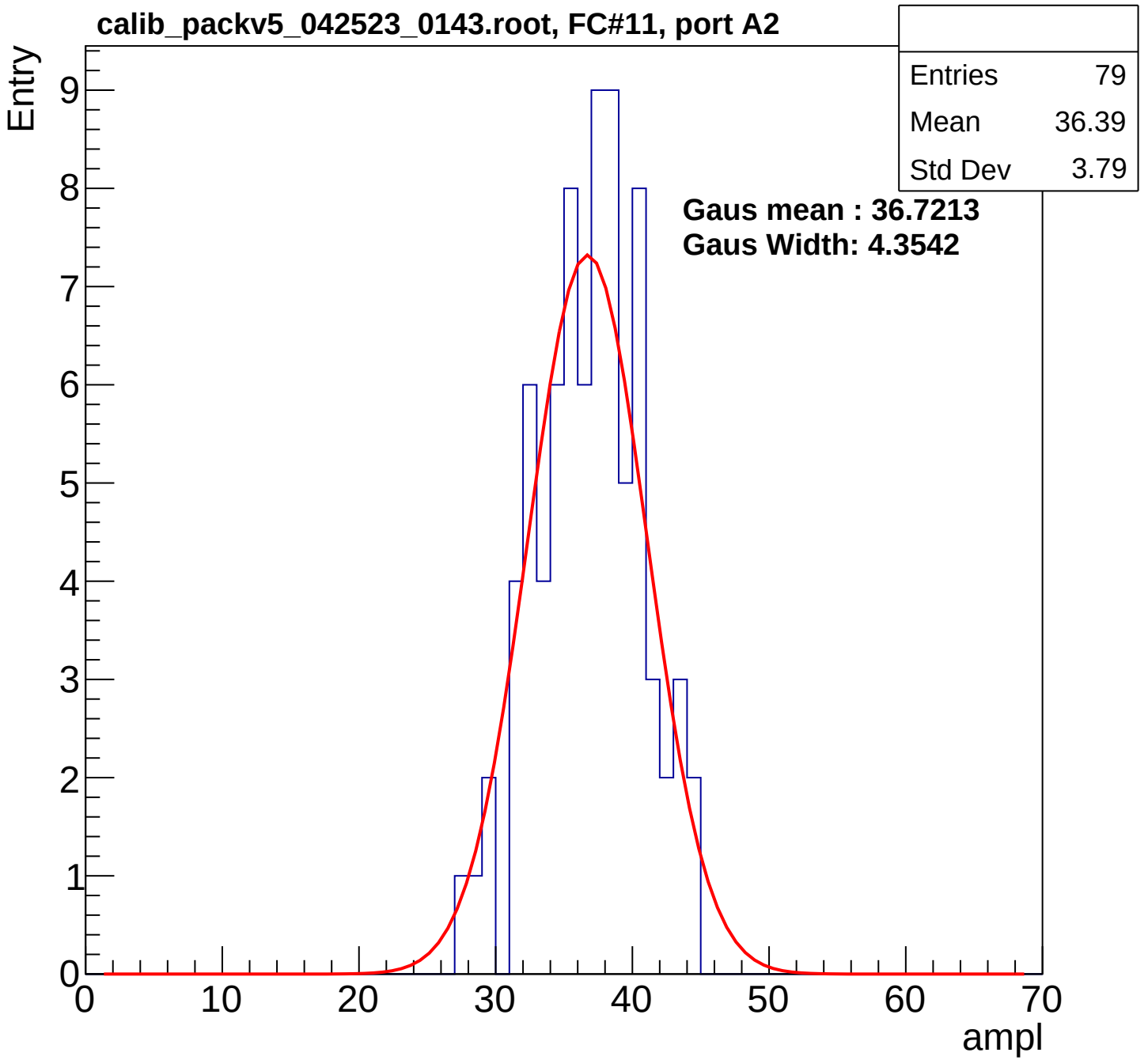
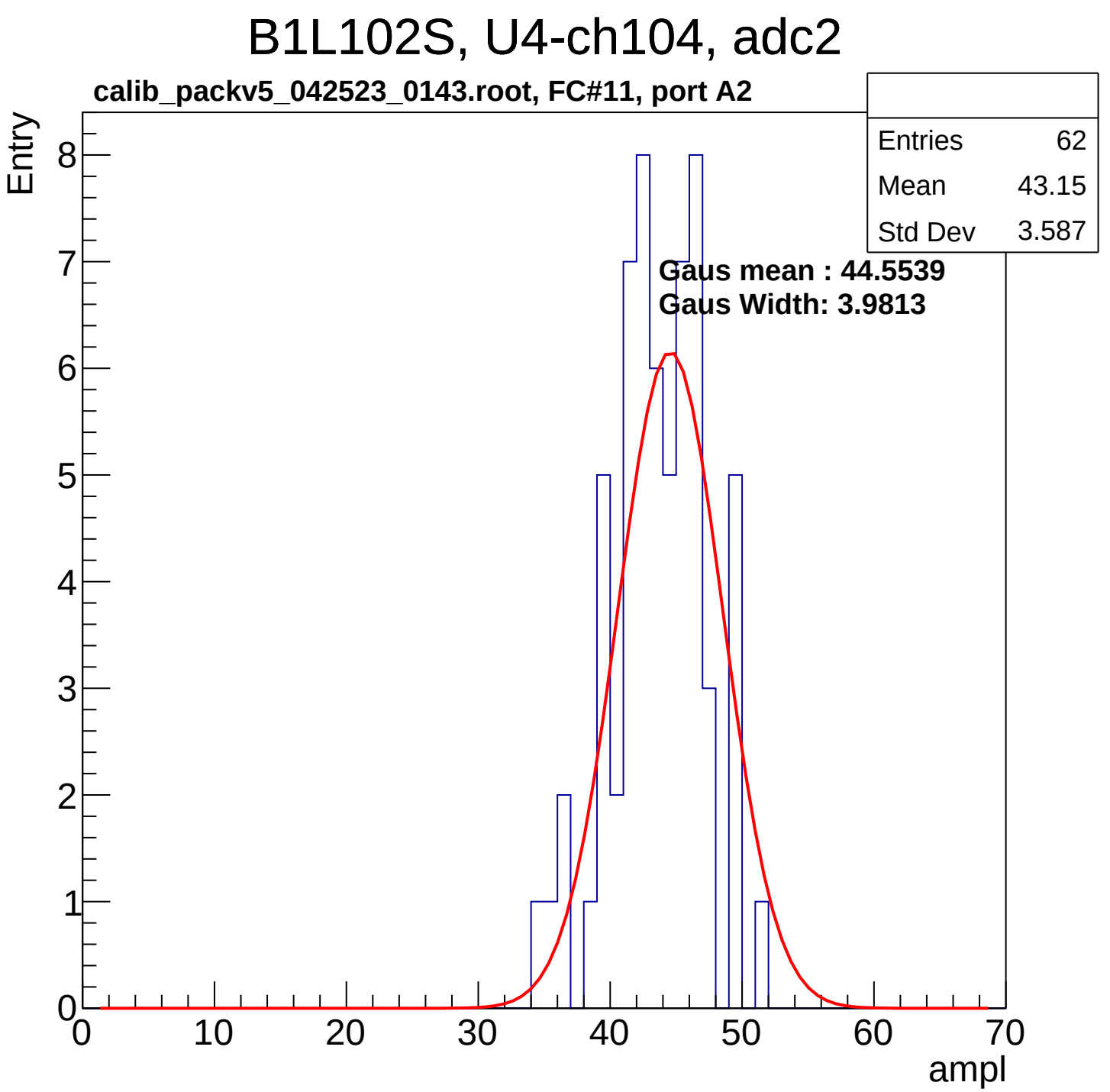
40
50
60
70


B1L102S, U4-ch104, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 79
Mean 36.39
Std Dev 3.79
Gaus mean : 36.7213
Gaus Width: 4.3542
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch104, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 43.15
Std Dev 3.587
Gaus mean : 44.5539
Gaus Width: 3.9813
Entry
ampl
0
1
2
3
4
5
6
7
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0
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20
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40
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60
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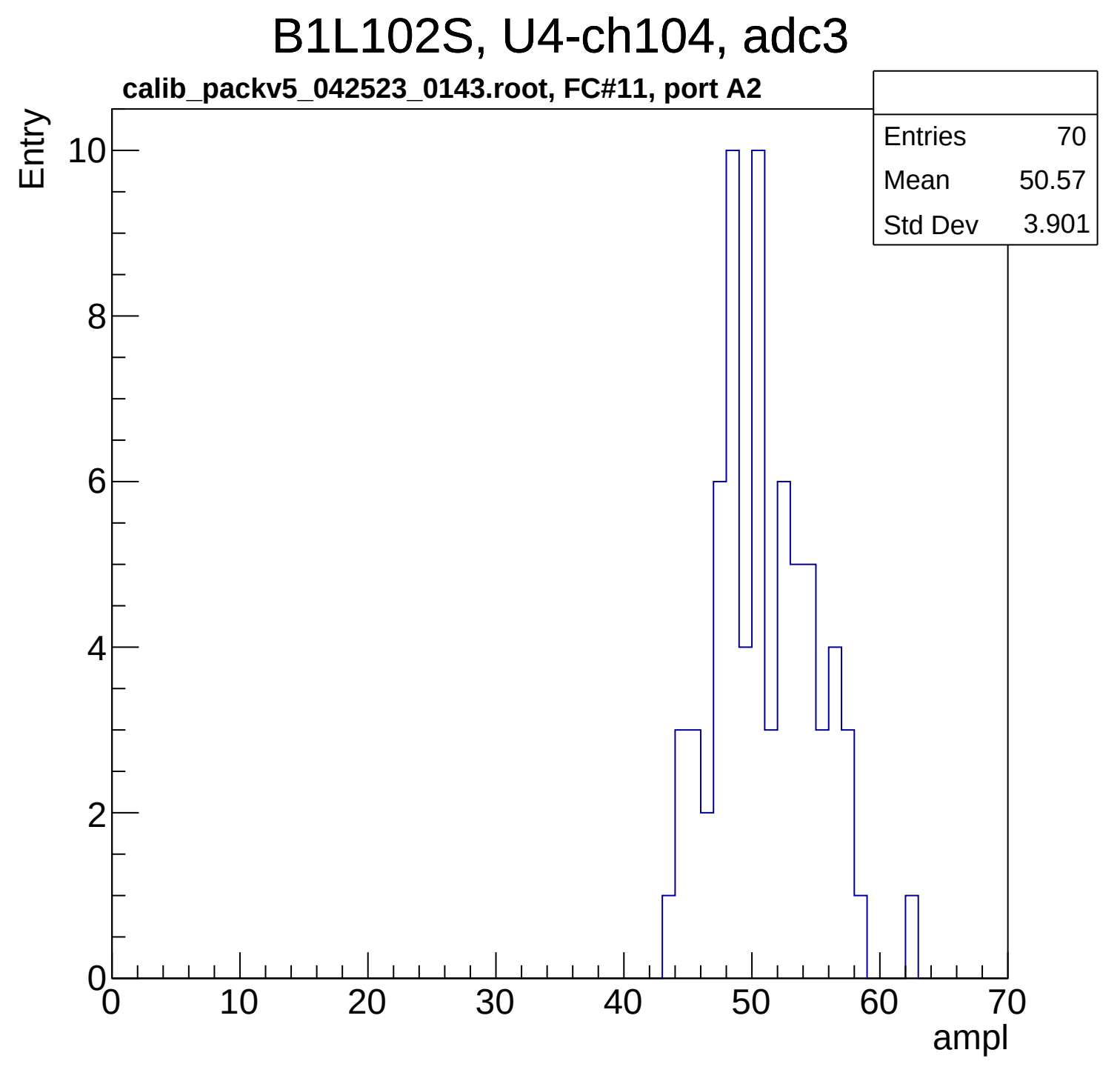
B1L102S, U4-ch104, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 50.57
Std Dev 3.901
Entry
0
2
4
6
8
10
0
10
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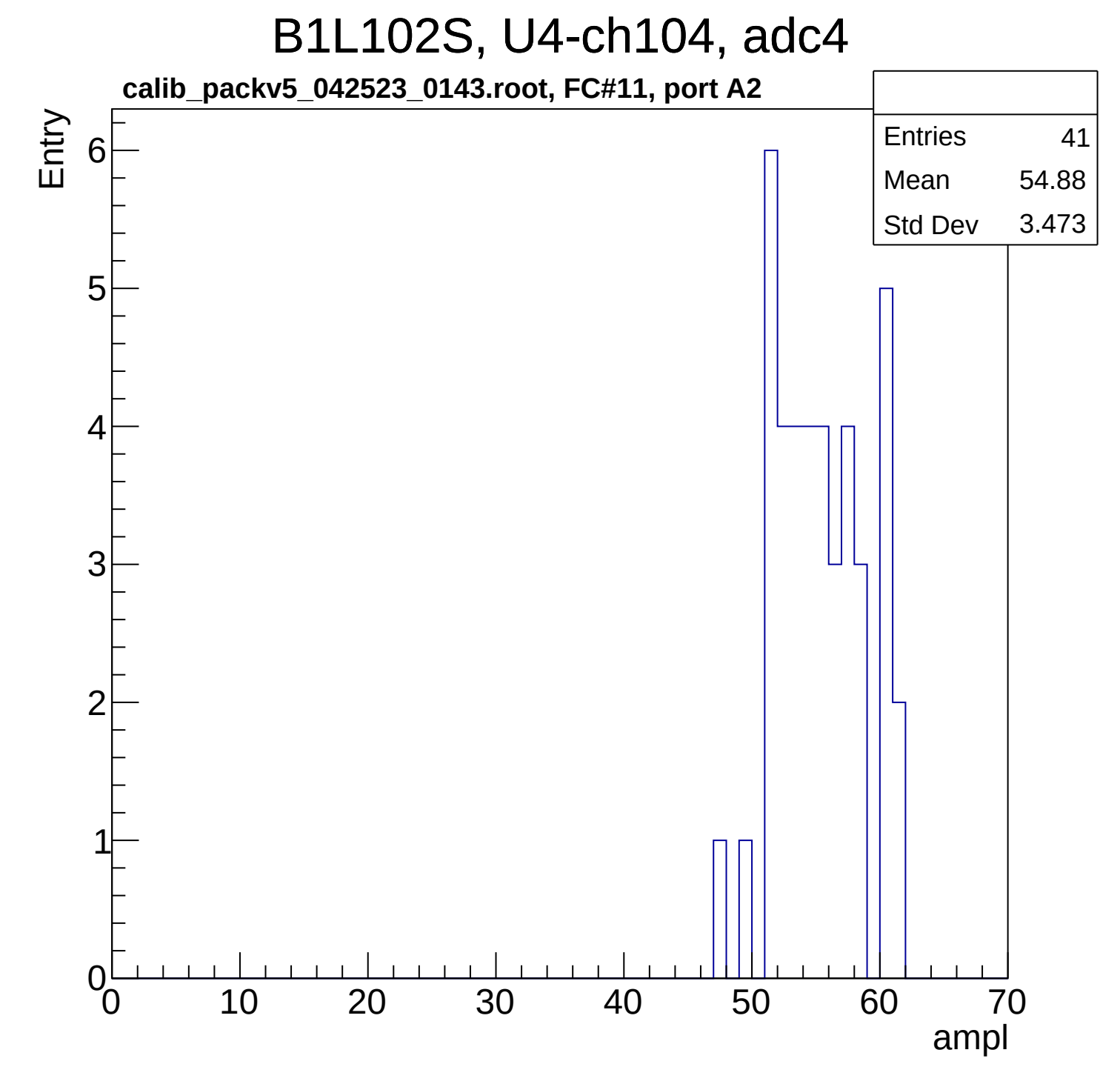
50
60
70
ampl


B1L102S, U4-ch104, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 41
Mean 54.88
Std Dev 3.473
Entry
ampl
0
1
2
3
4
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60
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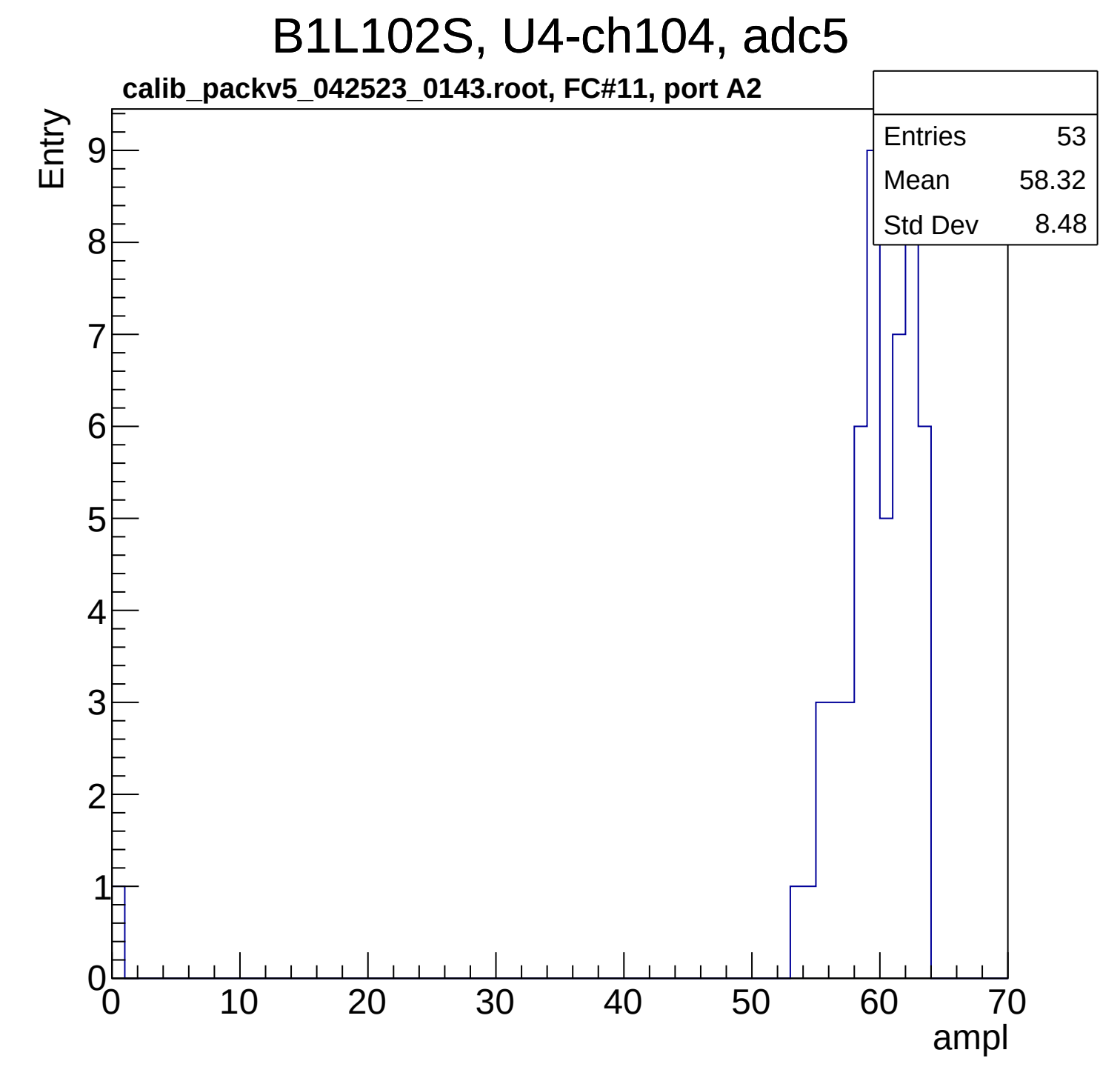
B1L102S, U4-ch104, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 58.32
Std Dev 8.48
Entry
ampl
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1
2
3
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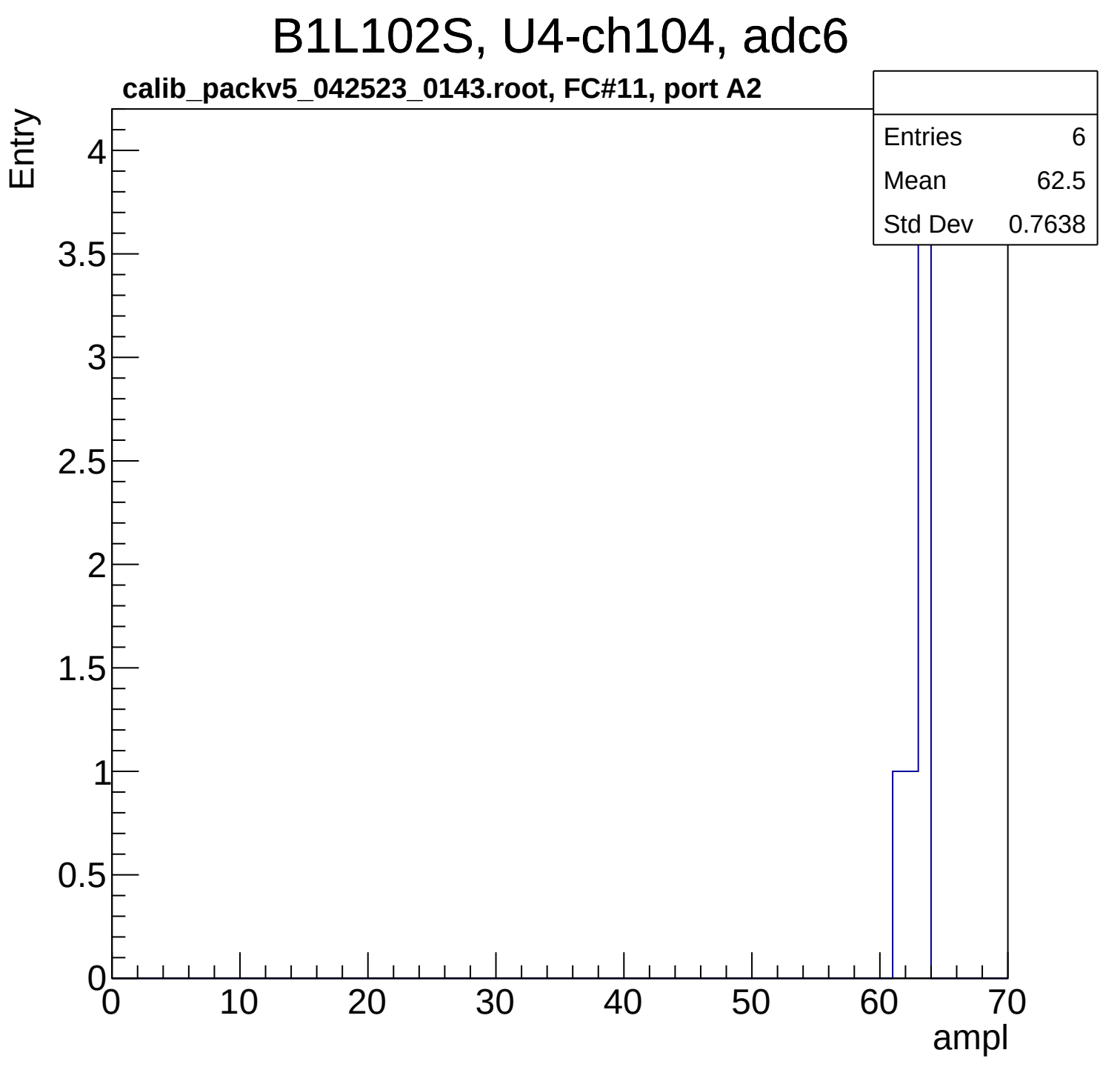
B1L102S, U4-ch104, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 6
Mean 62.5
Std Dev 0.7638
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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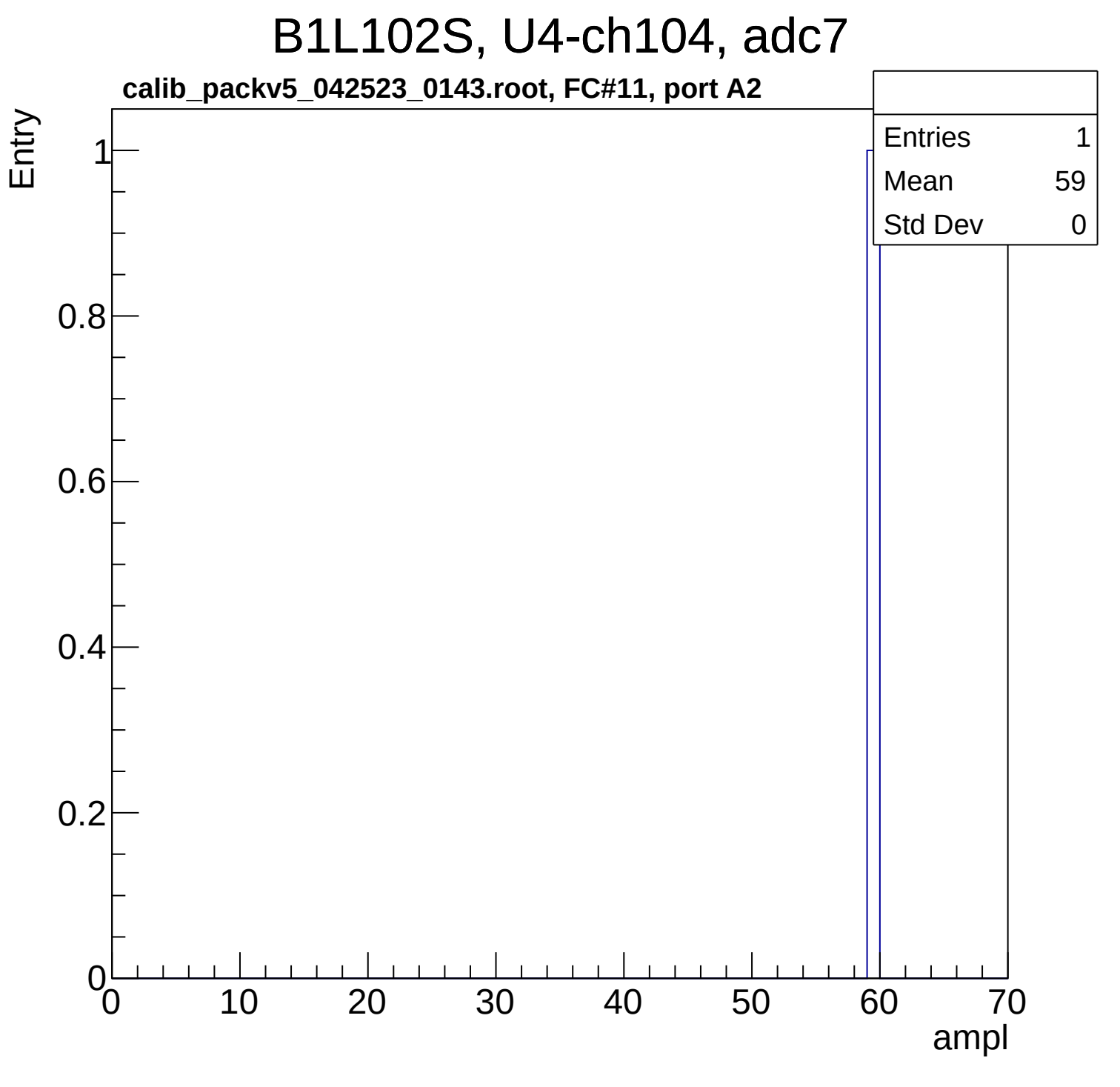
B1L102S, U4-ch104, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 59
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
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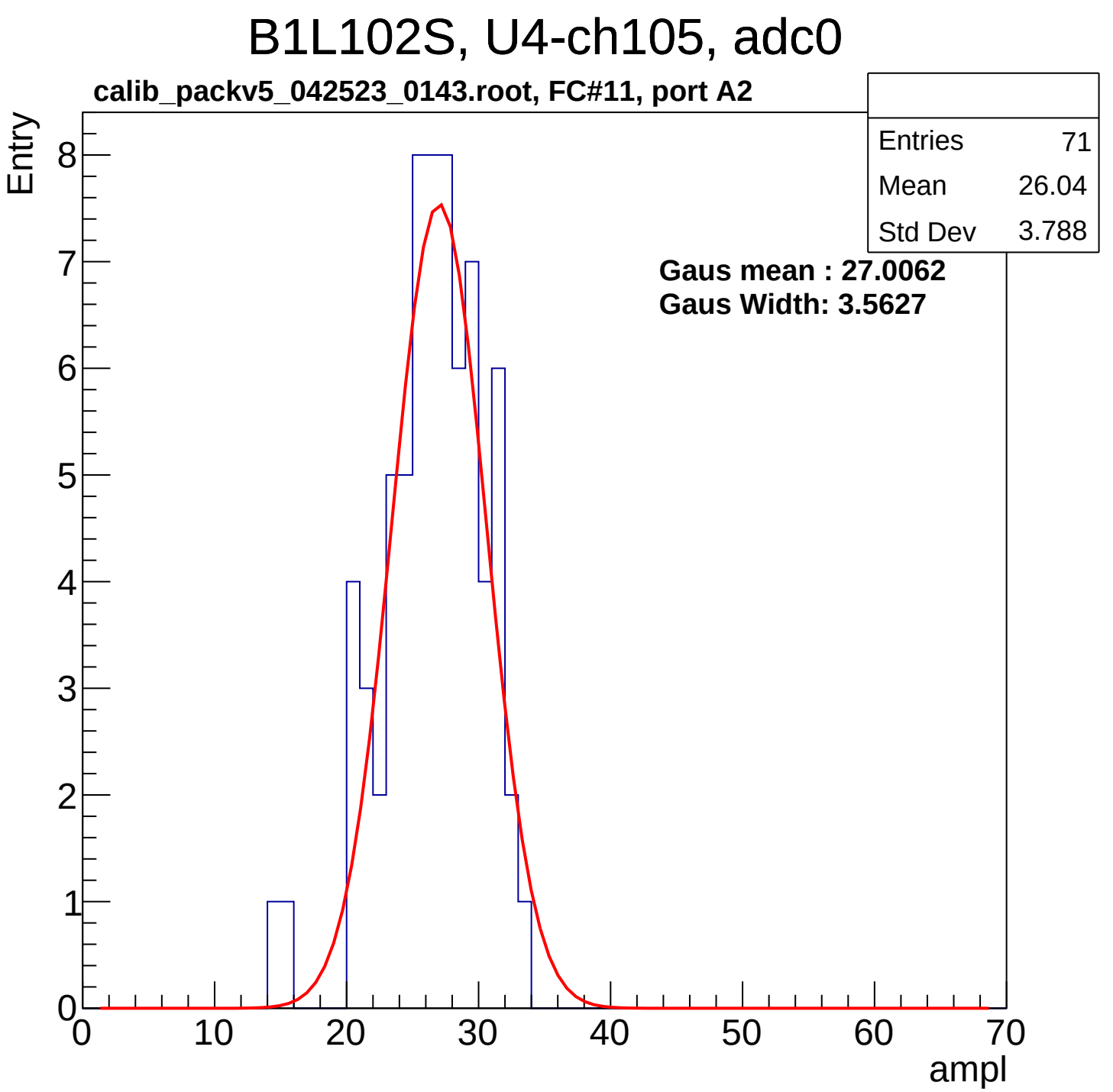
40
50
60
70
ampl


B1L102S, U4-ch105, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 26.04
Std Dev 3.788
Gaus mean : 27.0062
Gaus Width: 3.5627
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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20
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40
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60
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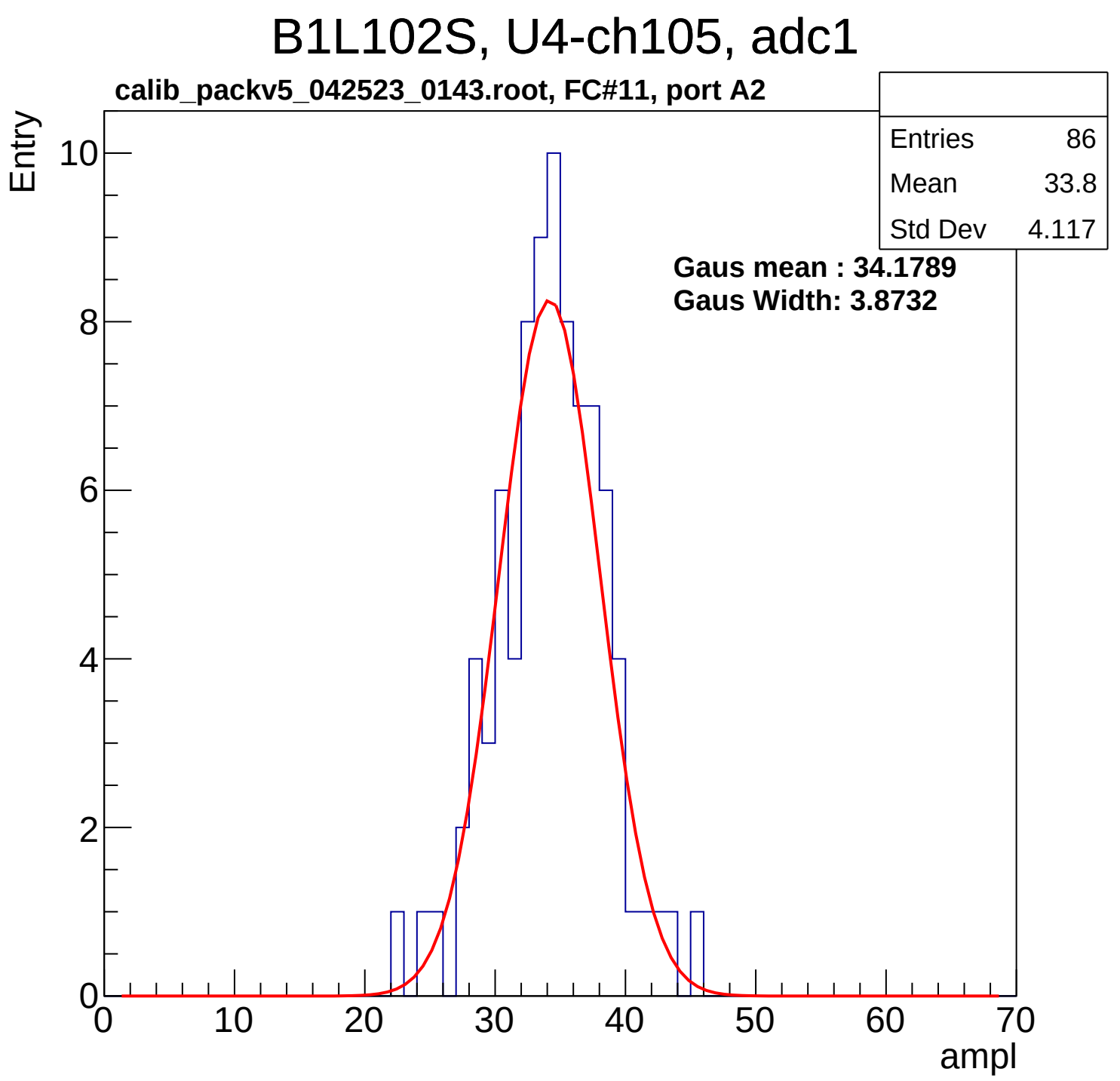
B1L102S, U4-ch105, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 86
Mean 33.8
Std Dev 4.117
Gaus mean : 34.1789
Gaus Width: 3.8732
Entry
ampl
0
2
4
6
8
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0
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40
50
60
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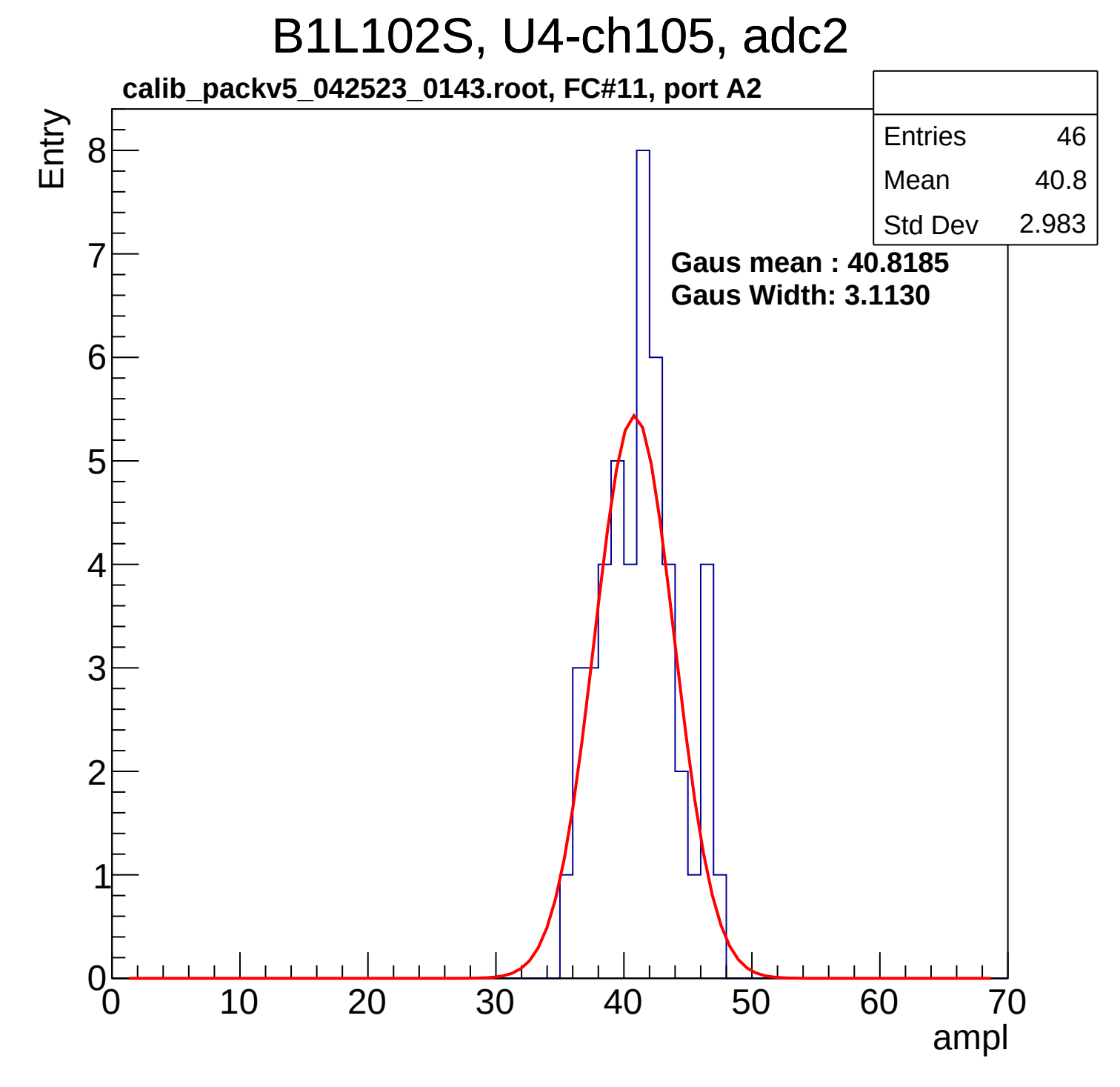
B1L102S, U4-ch105, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 46
Mean 40.8
Std Dev 2.983
Gaus mean : 40.8185
Gaus Width: 3.1130
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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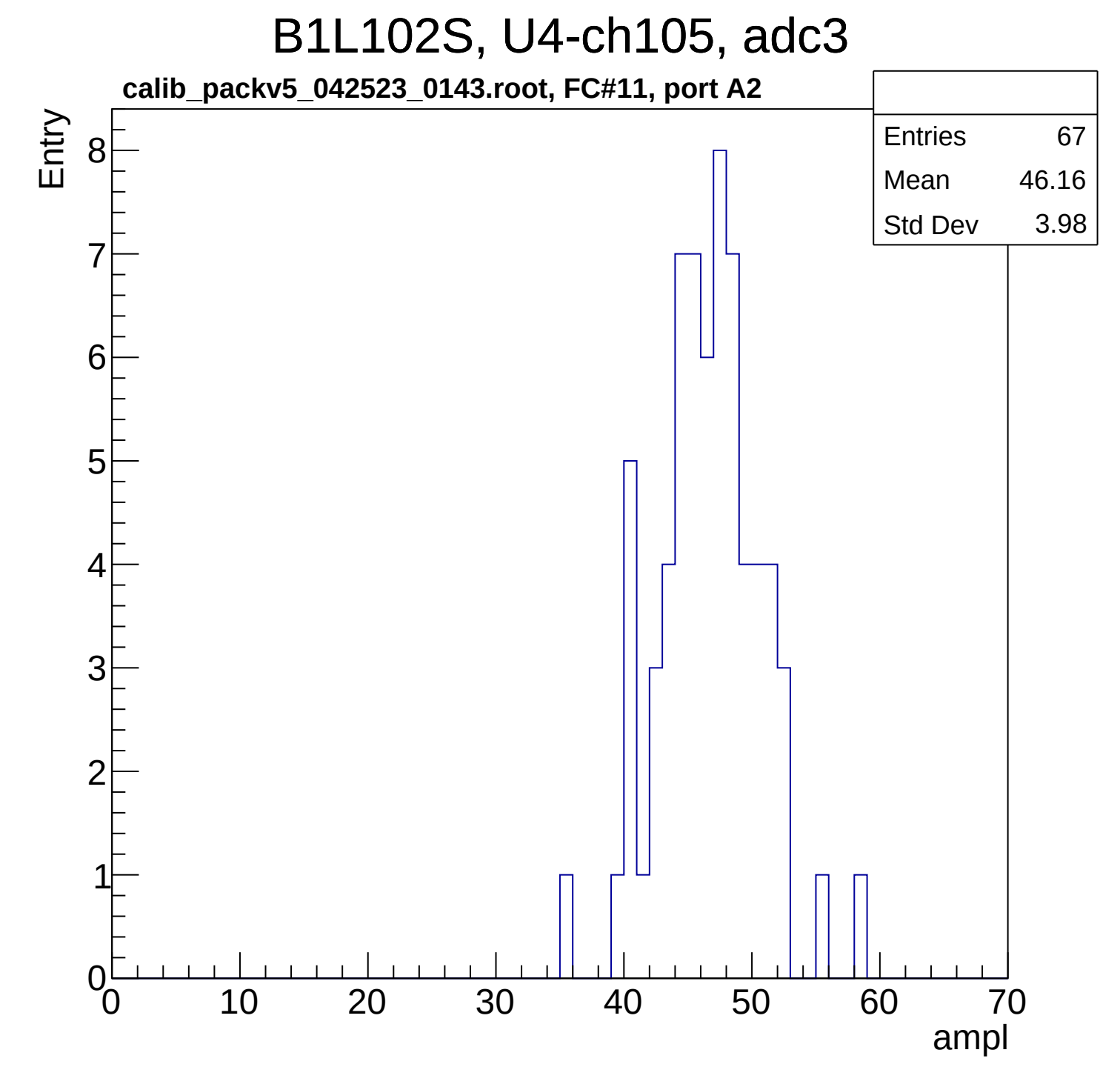
B1L102S, U4-ch105, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 46.16
Std Dev 3.98
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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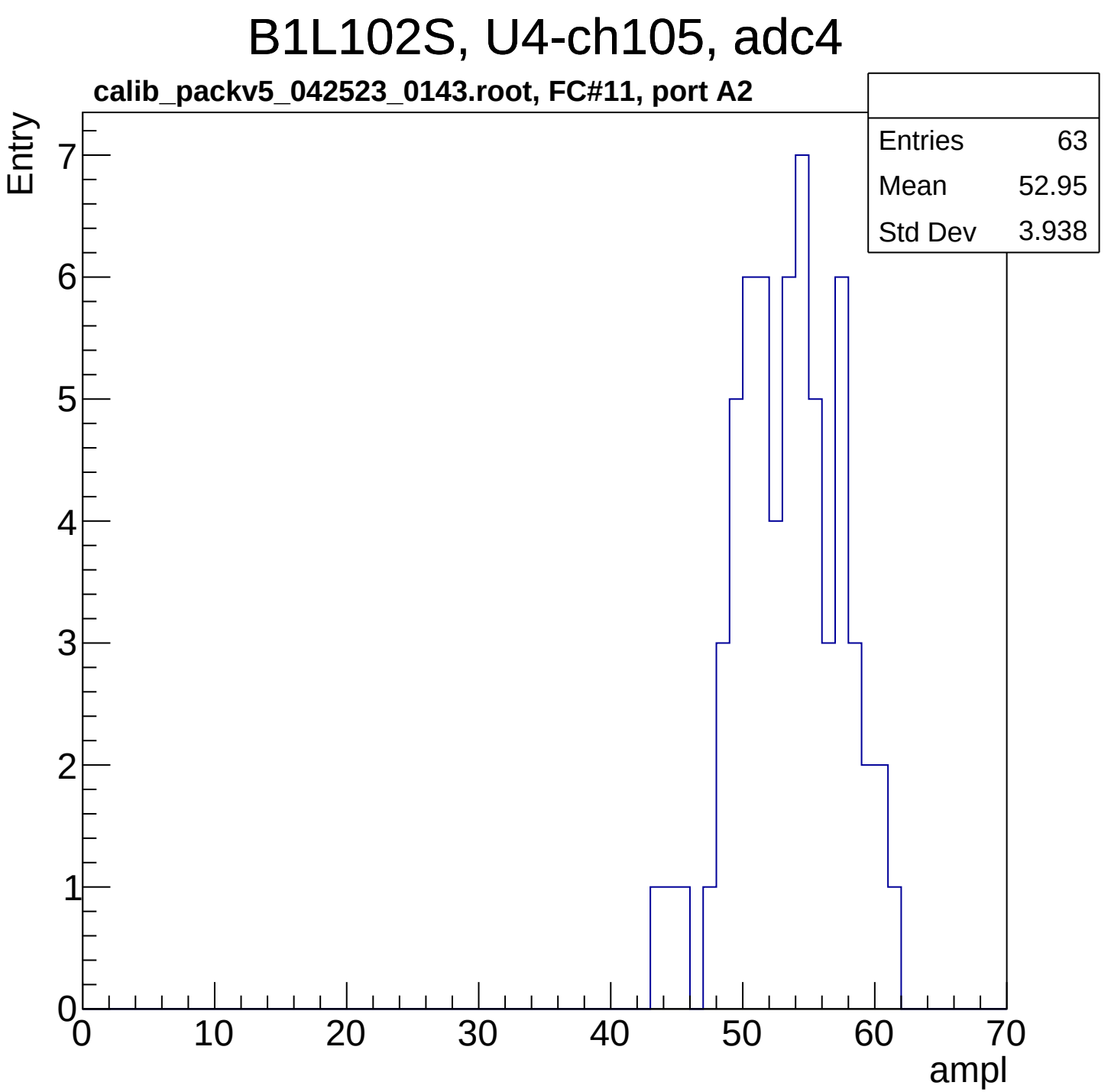
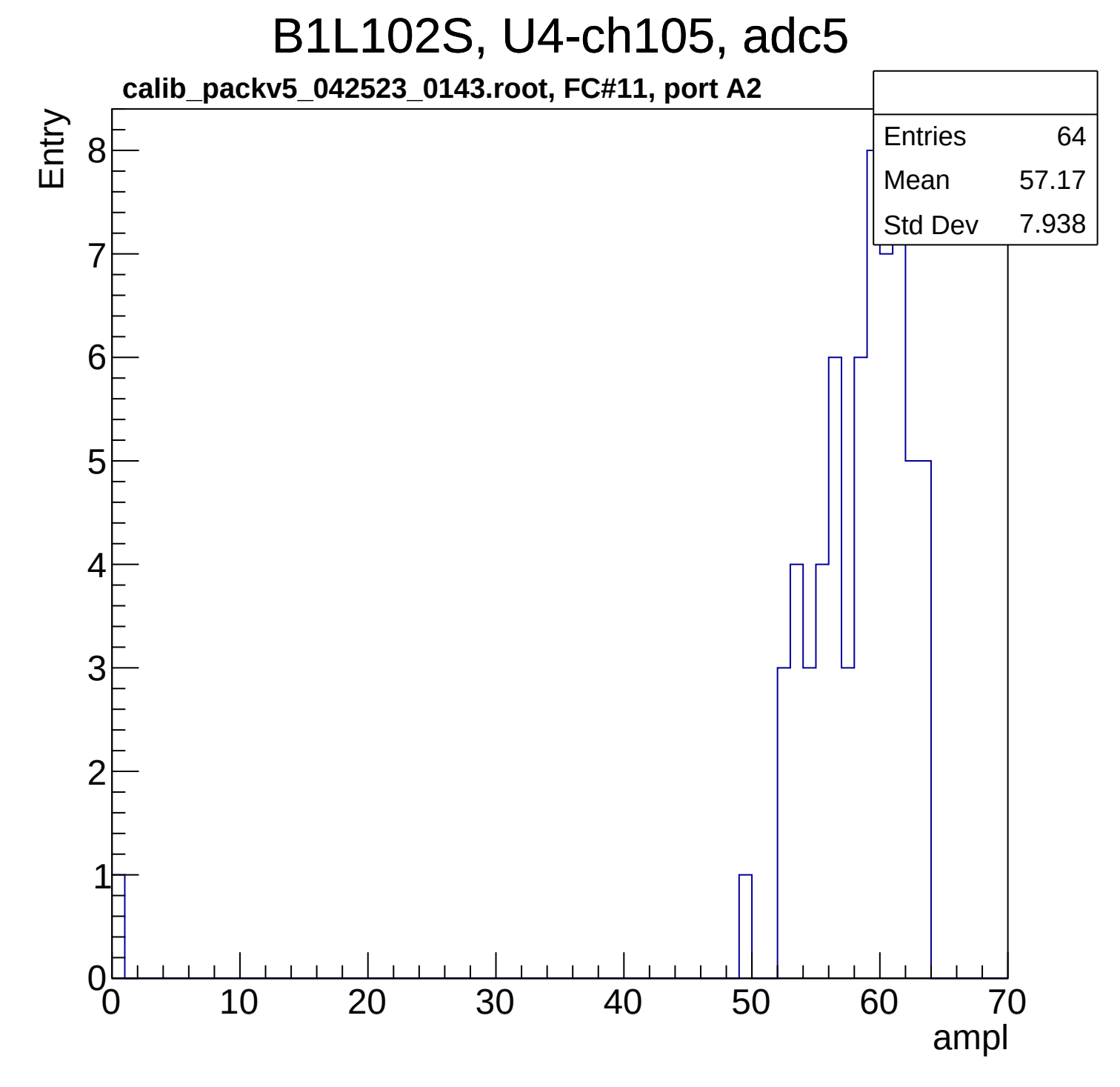
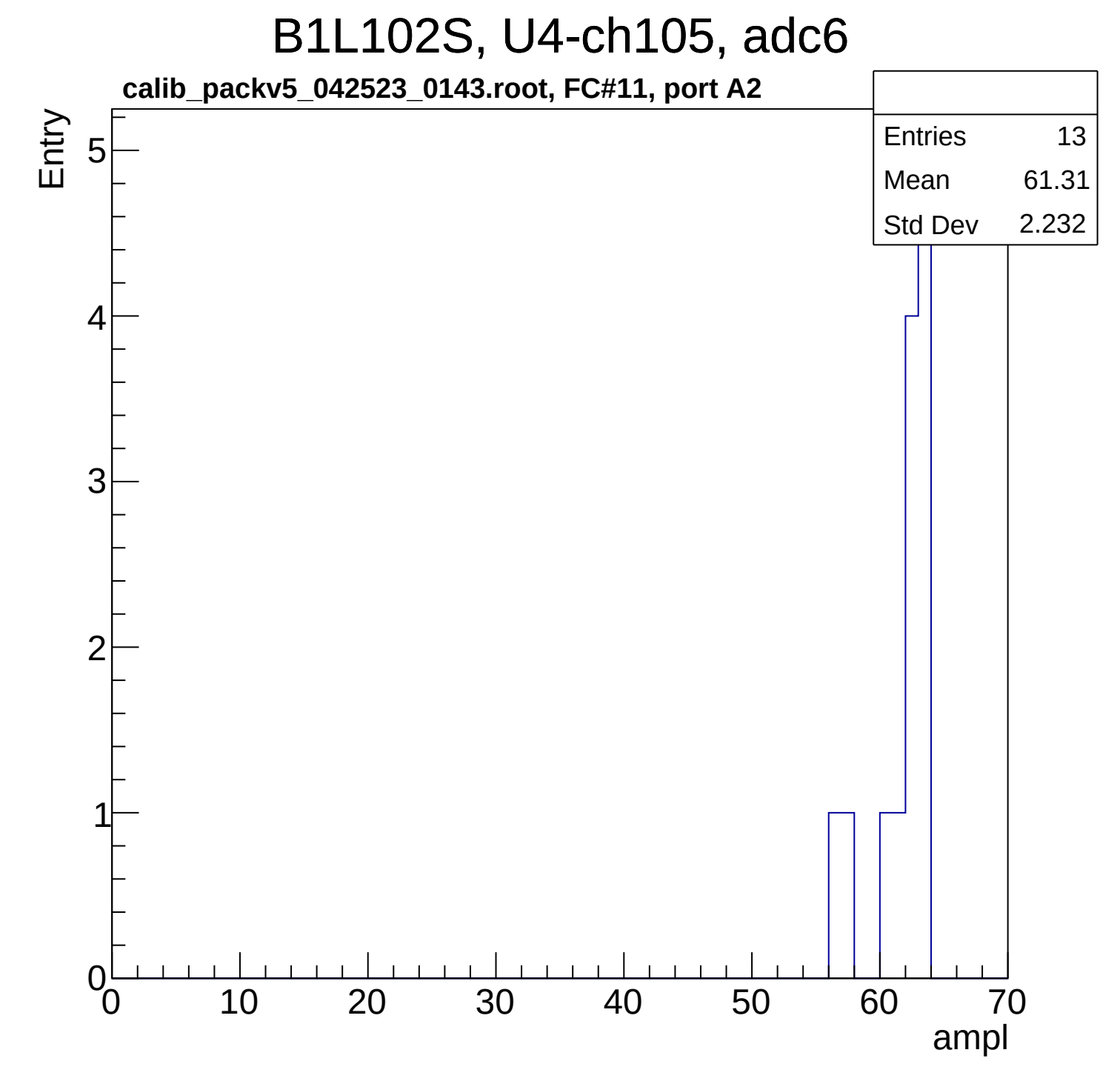

B1L102S, U4-ch105, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 52.95
Std Dev 3.938
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch105, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 57.17
Std Dev 7.938
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch105, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 13
Mean 61.31
Std Dev 2.232
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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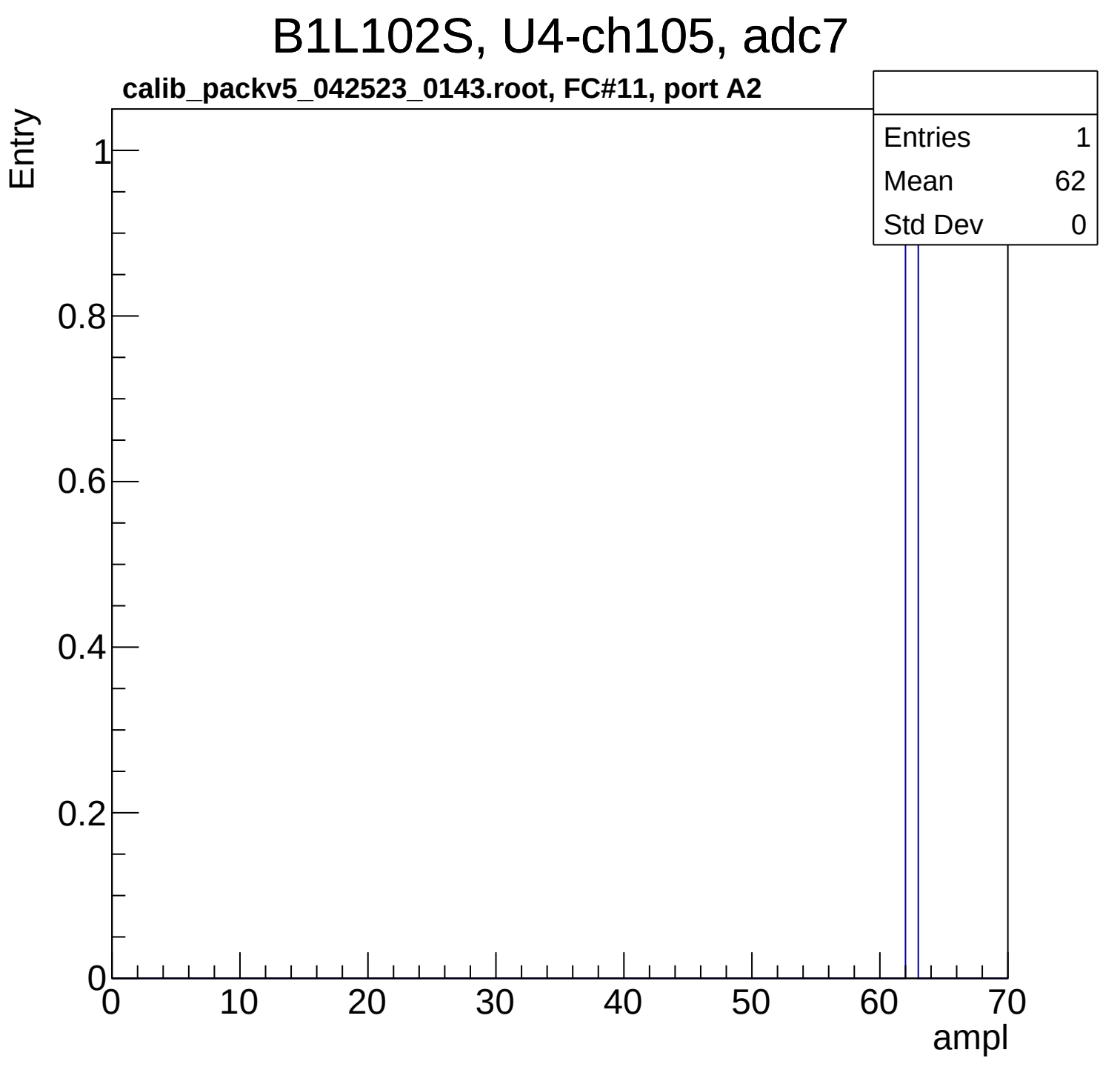
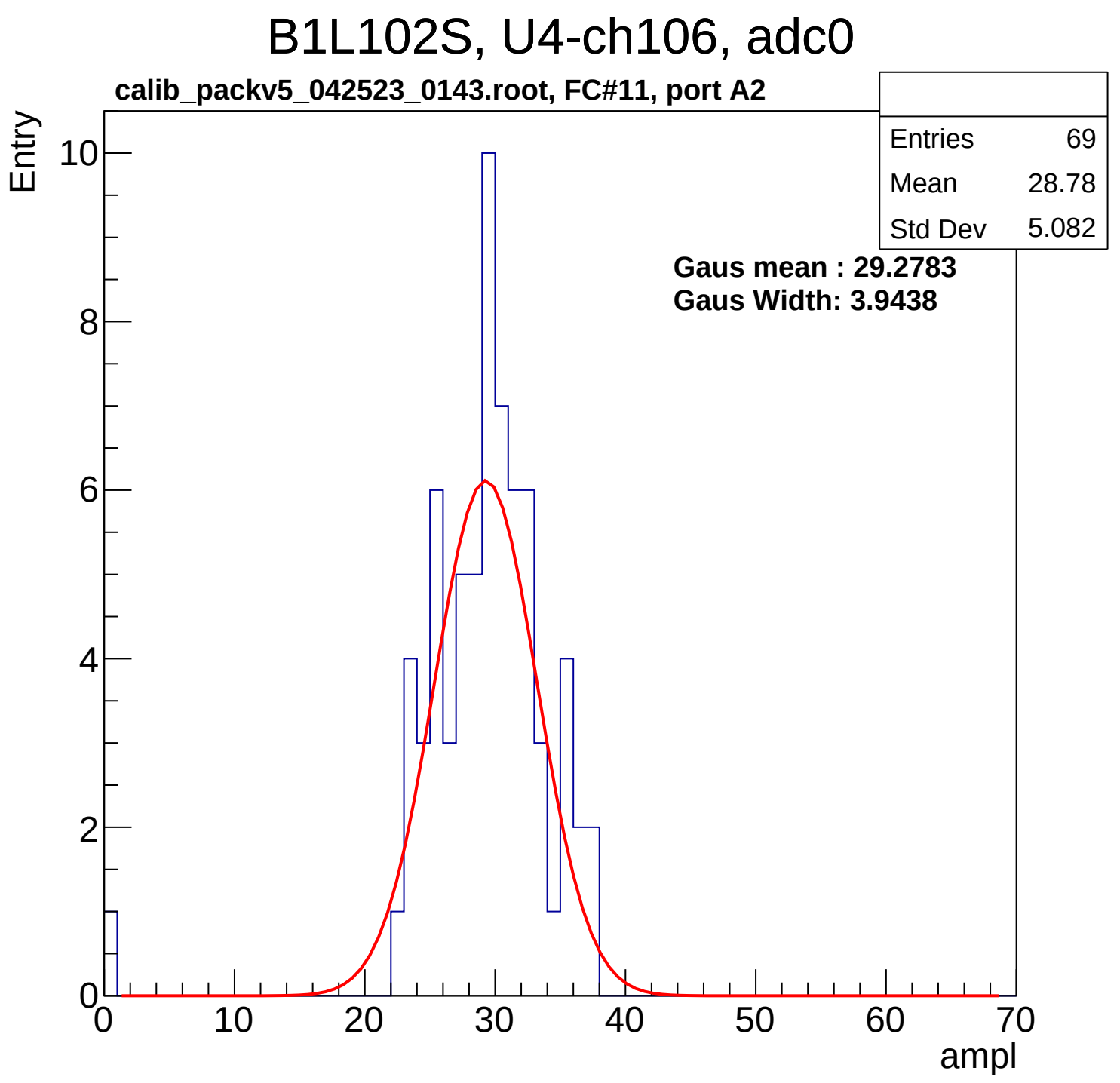
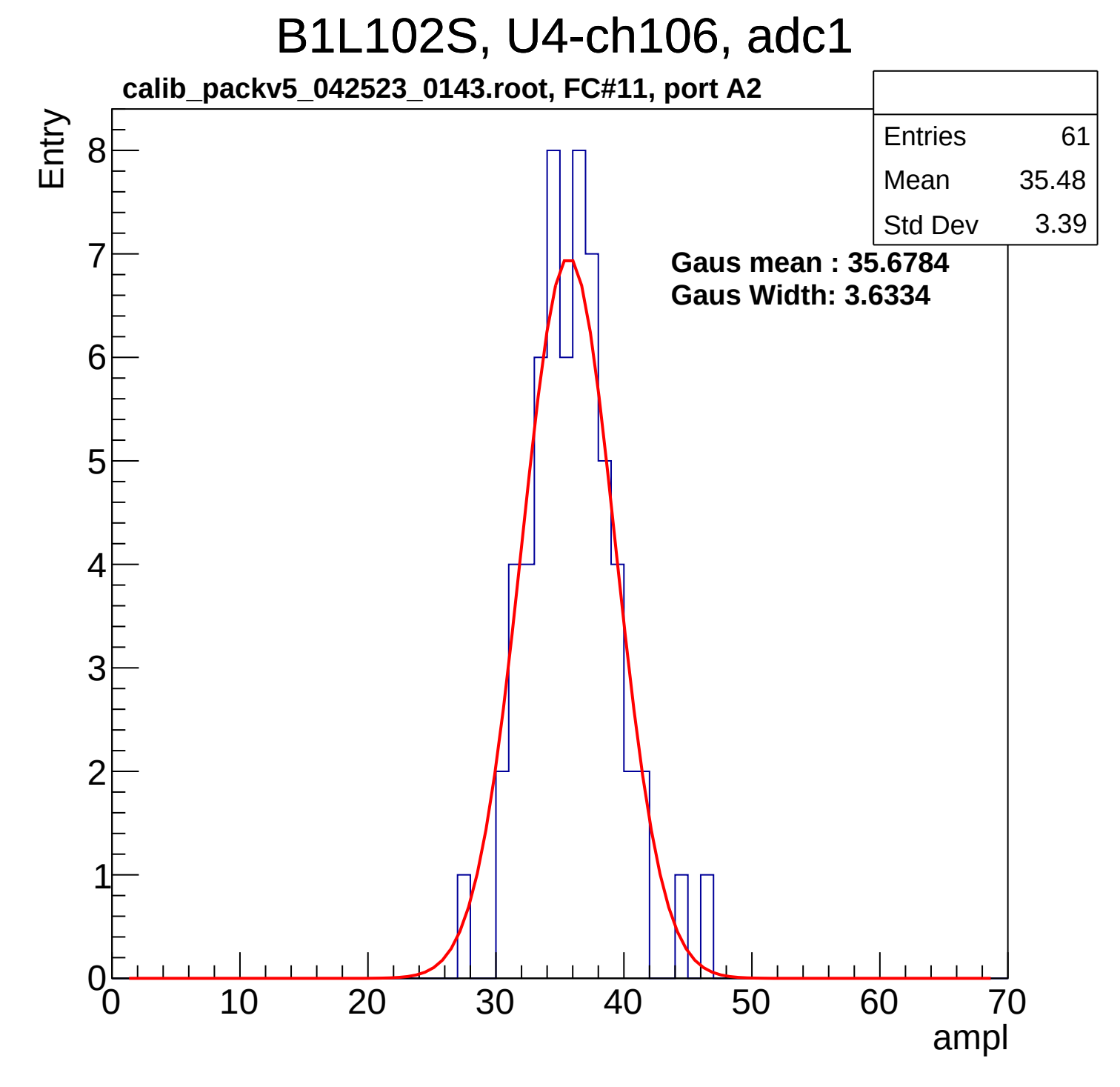
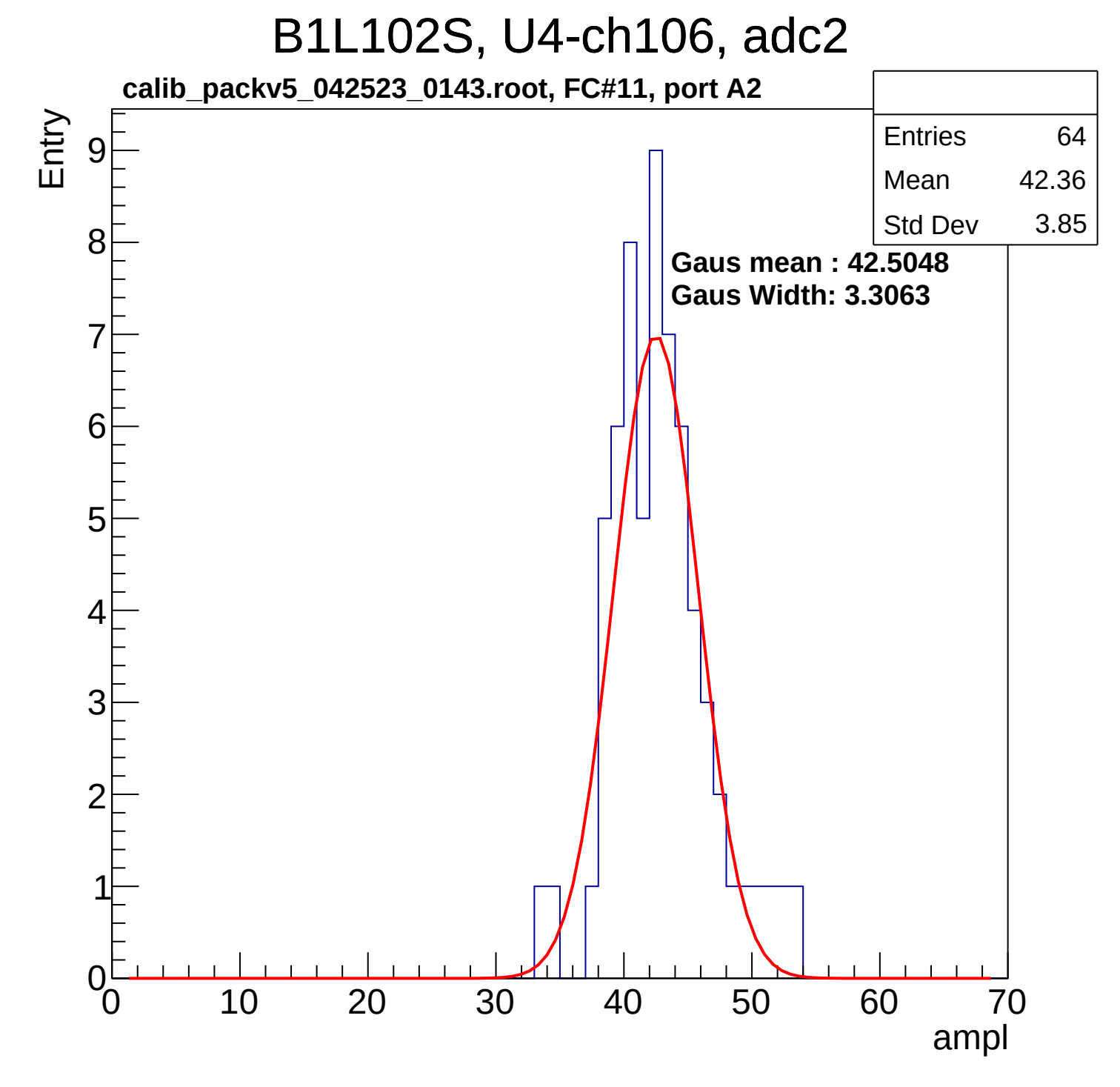

B1L102S, U4-ch105, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch106, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 28.78
Std Dev 5.082
Gaus mean : 29.2783
Gaus Width: 3.9438
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch106, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 35.48
Std Dev 3.39
Gaus mean : 35.6784
Gaus Width: 3.6334
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch106, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 42.36
Std Dev 3.85
Gaus mean : 42.5048
Gaus Width: 3.3063
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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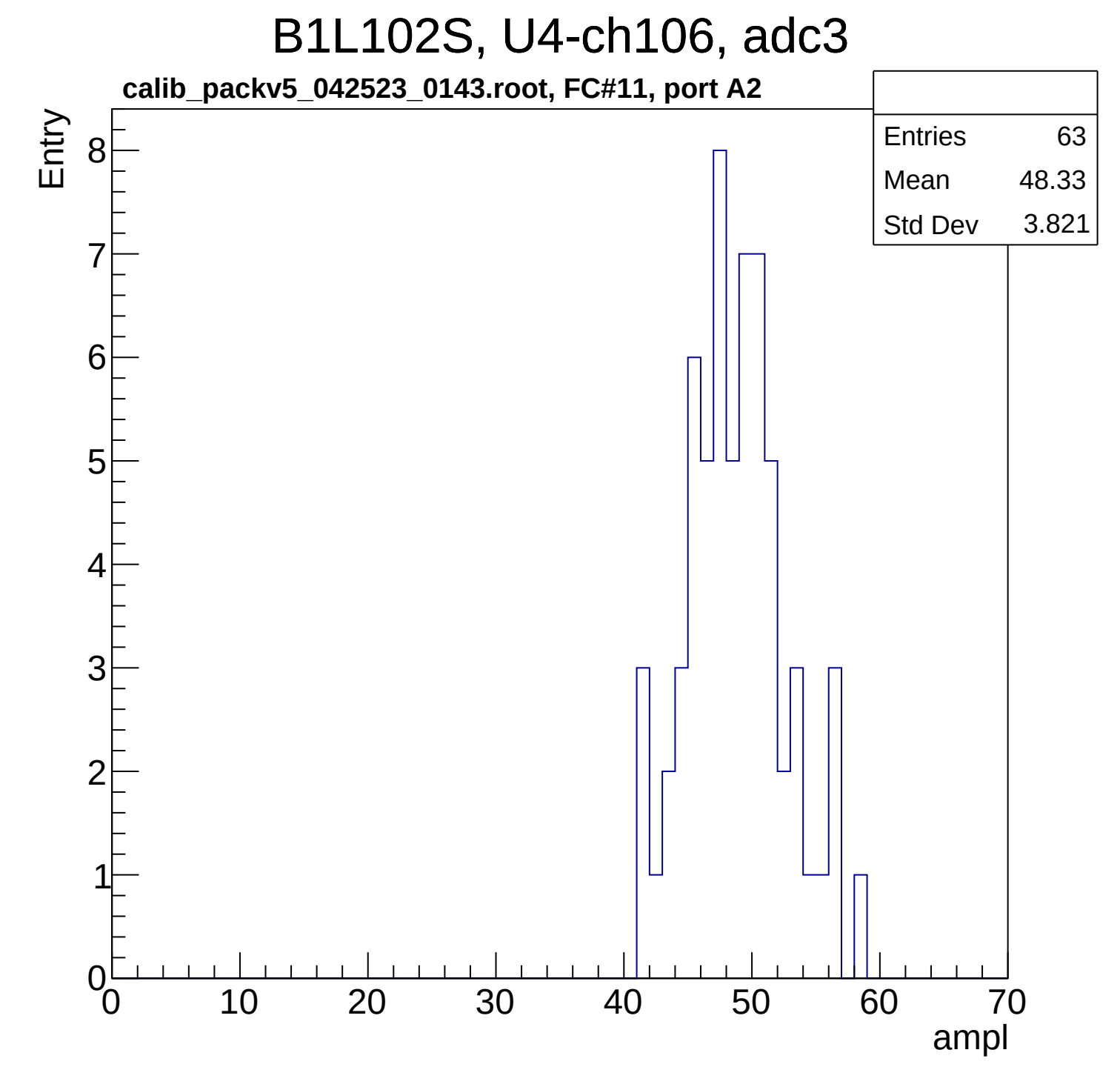
B1L102S, U4-ch106, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 48.33
Std Dev 3.821
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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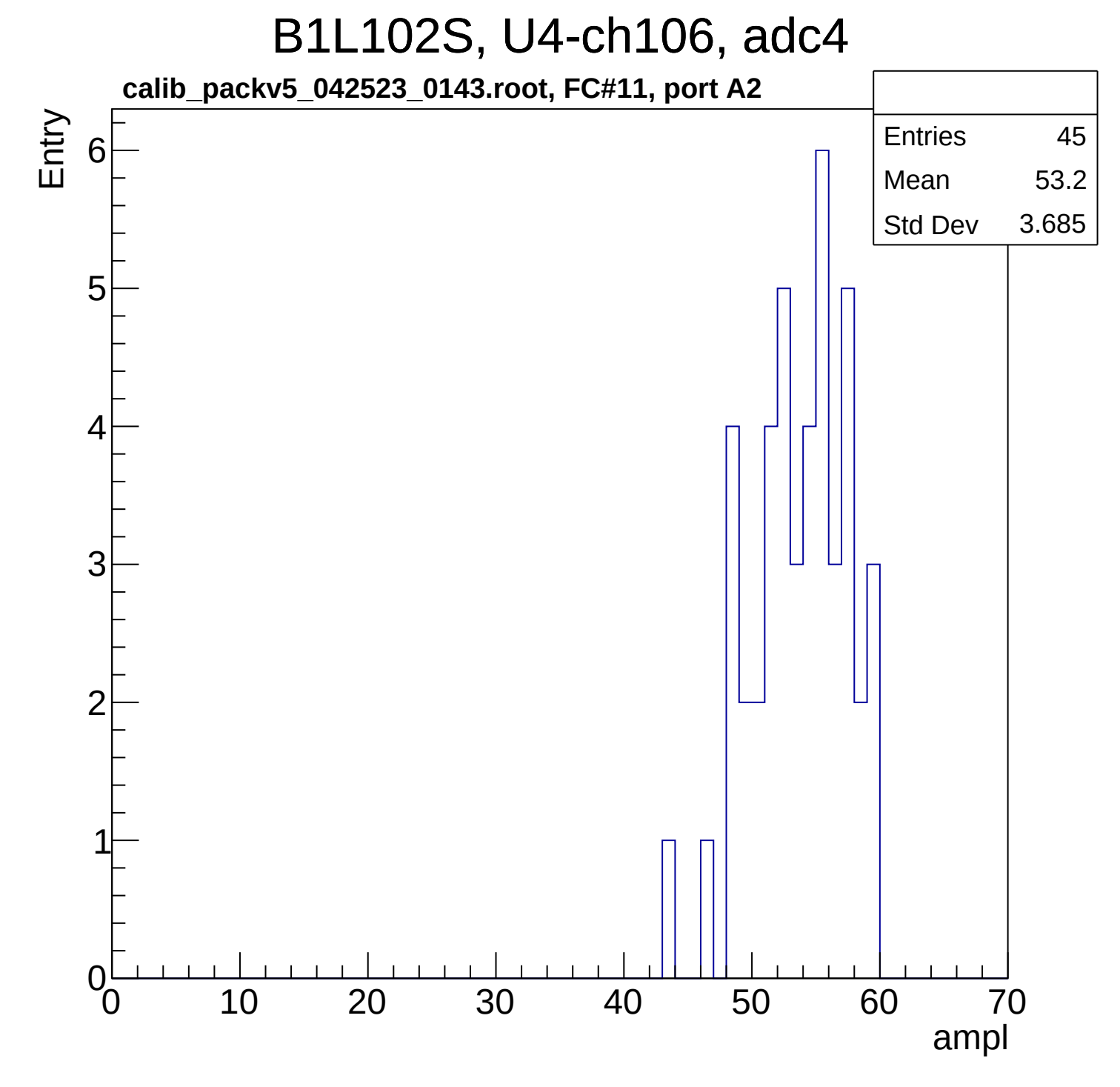
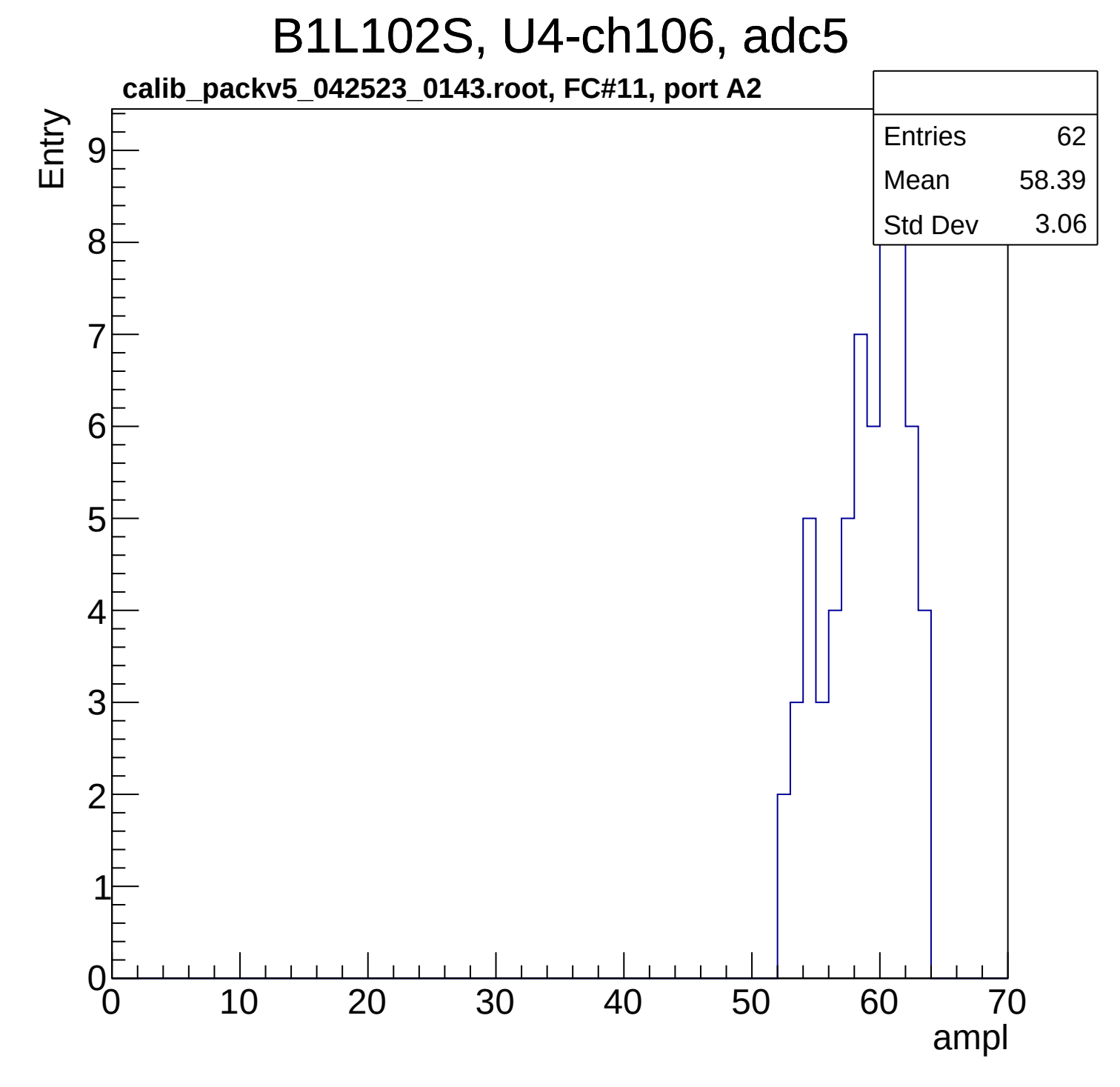

B1L102S, U4-ch106, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 45
Mean 53.2
Std Dev 3.685
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L102S, U4-ch106, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 58.39
Std Dev 3.06
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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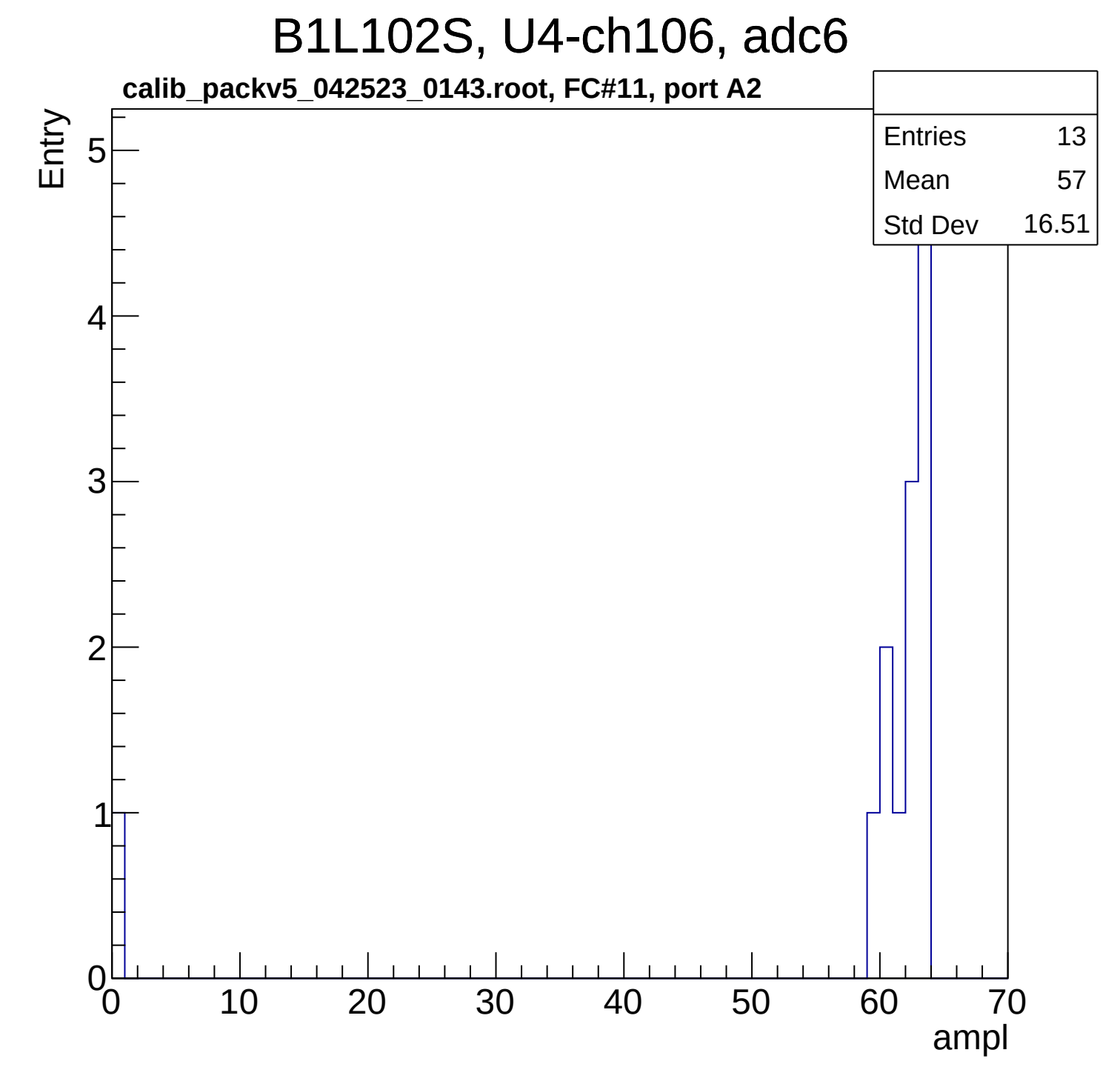
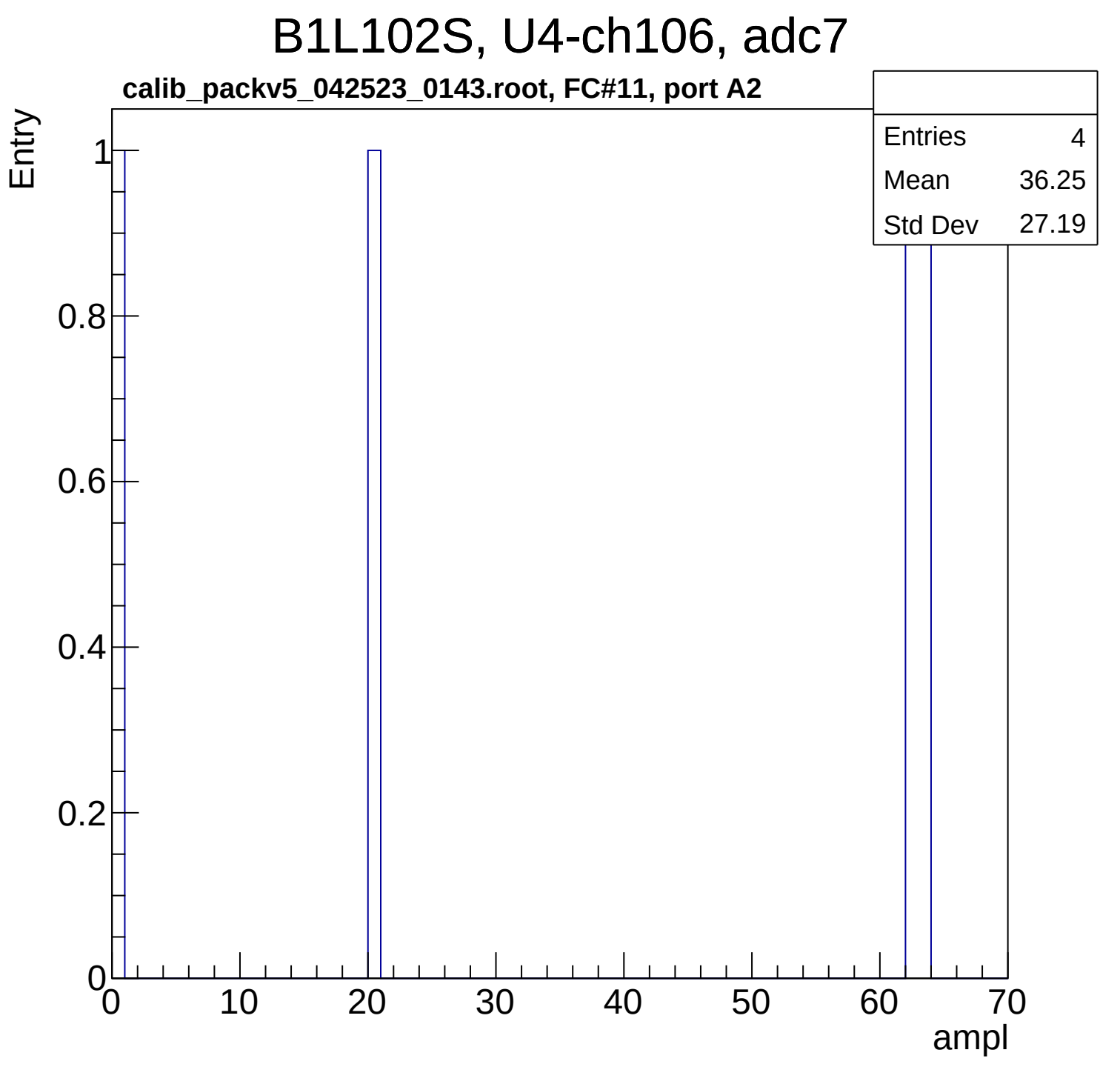

B1L102S, U4-ch106, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 13
Mean 57
Std Dev 16.51
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch106, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 4
Mean 36.25
Std Dev 27.19
Entry
ampl
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0.2
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0.6
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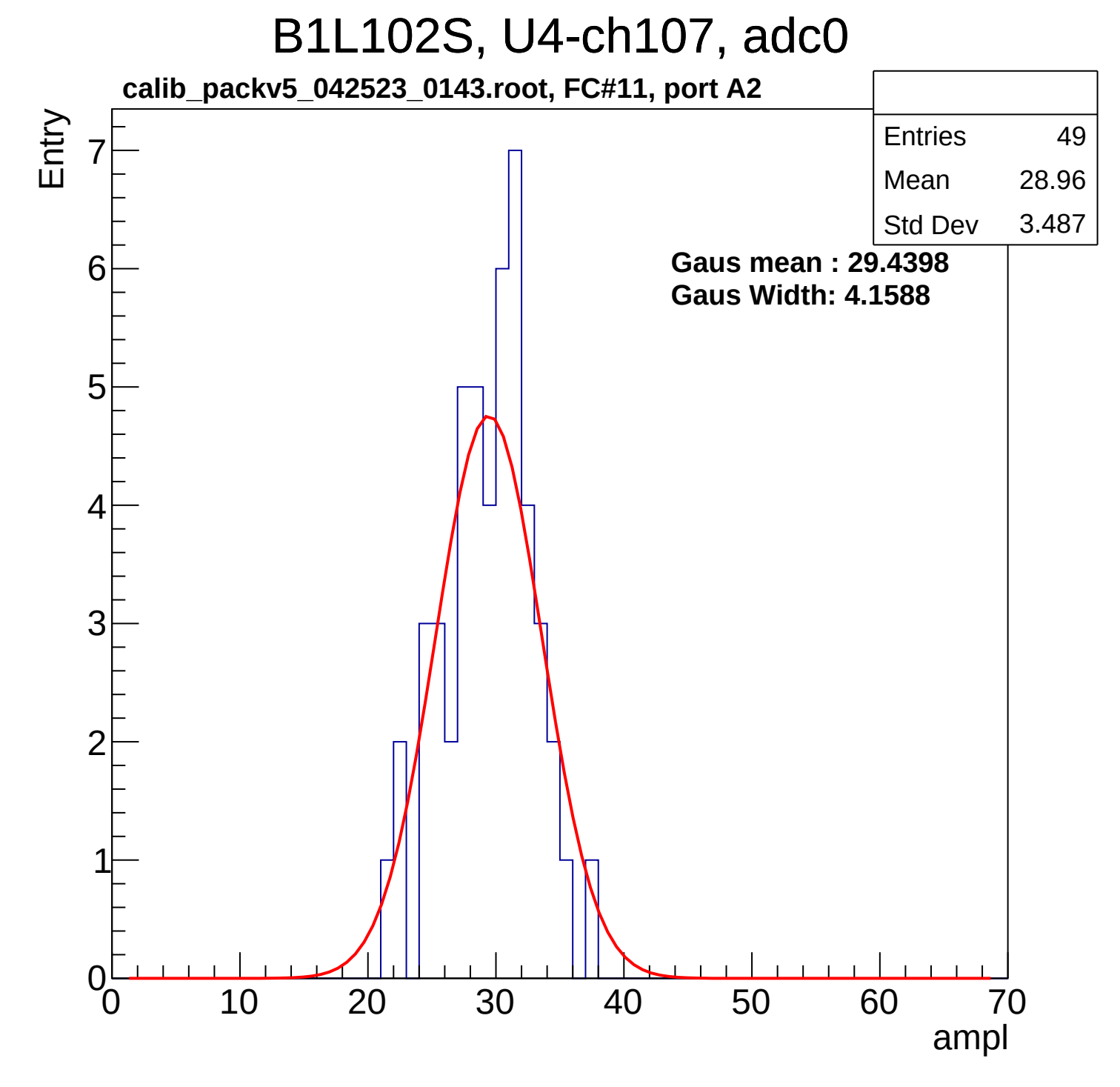
B1L102S, U4-ch107, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 28.96
Std Dev 3.487
Gaus mean : 29.4398
Gaus Width: 4.1588
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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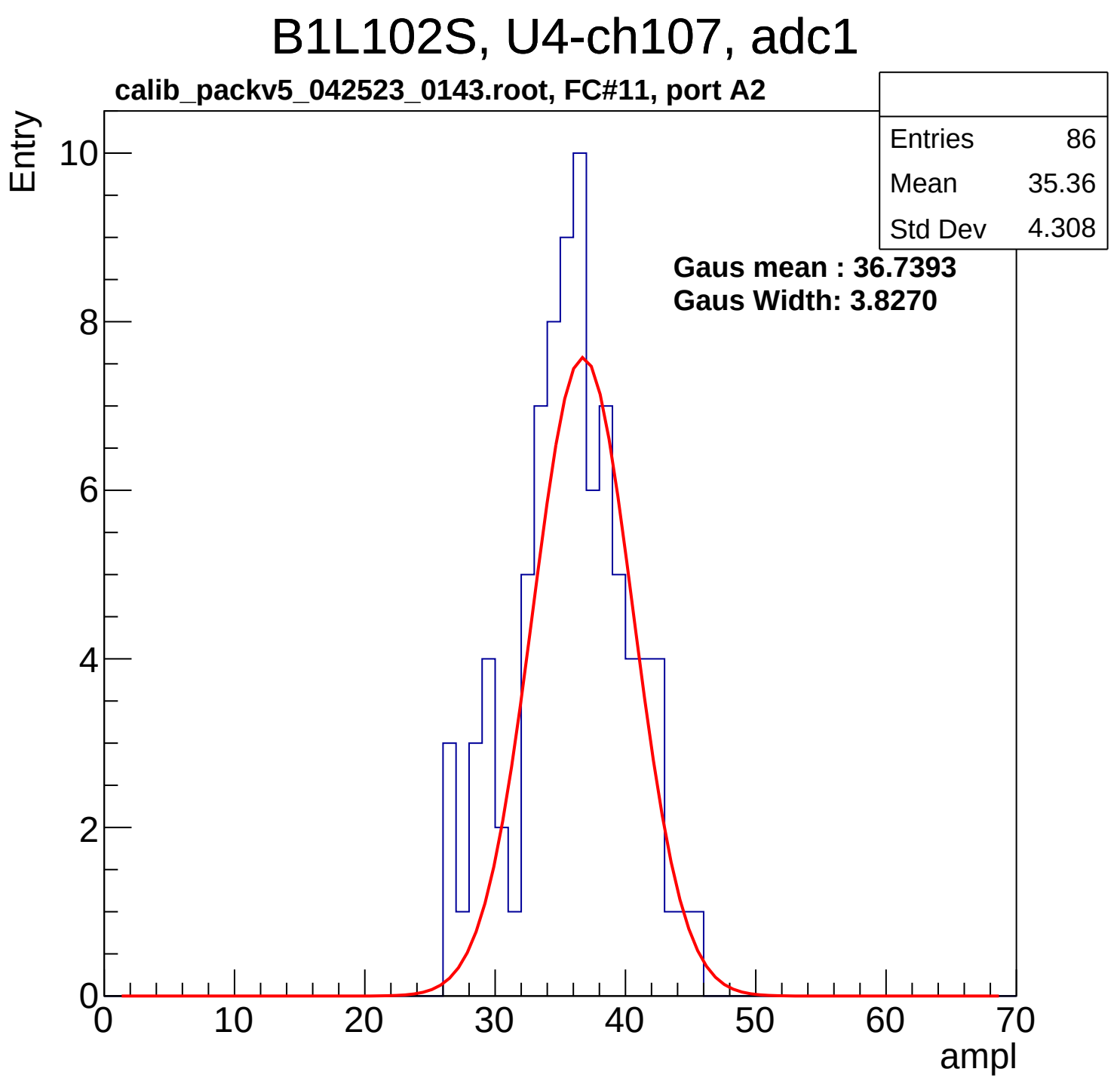
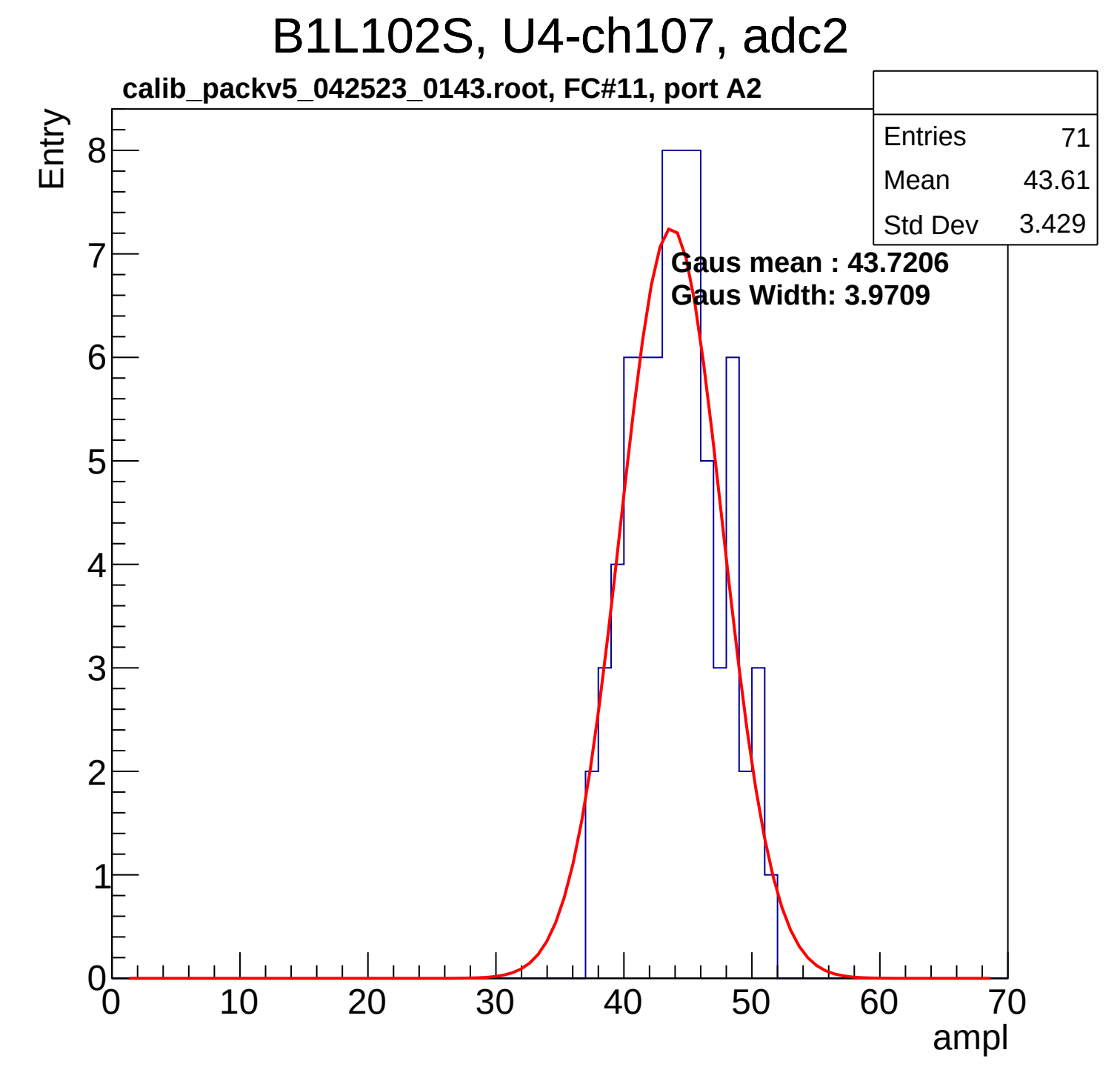

B1L102S, U4-ch107, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 86
Mean 35.36
Std Dev 4.308
Gaus mean : 36.7393
Gaus Width: 3.8270
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch107, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 43.61
Std Dev 3.429
Gaus mean : 43.7206
Gaus Width: 3.9709
Entry
ampl
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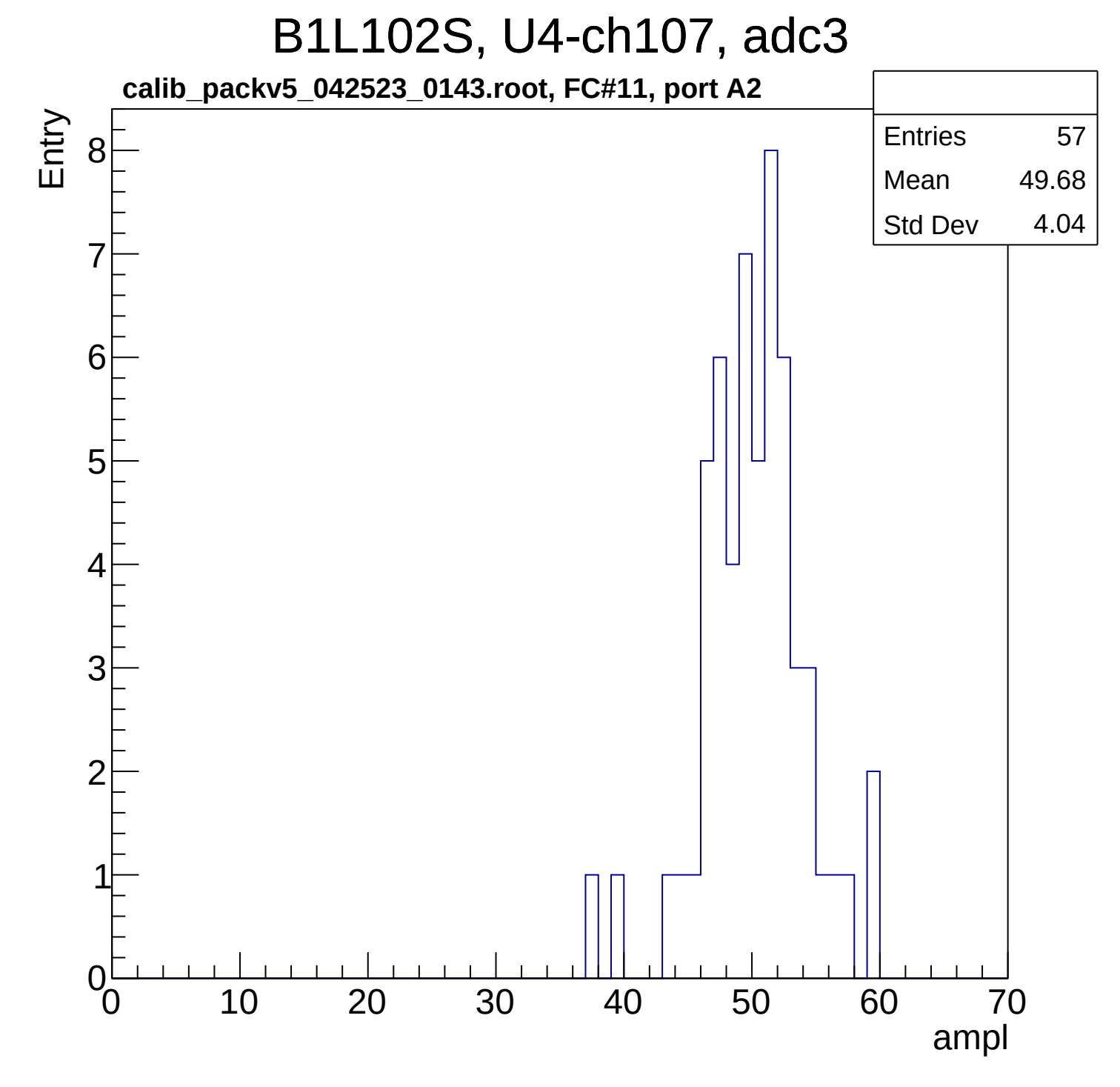
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch107, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 57
Mean 49.68
Std Dev 4.04
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
50
60
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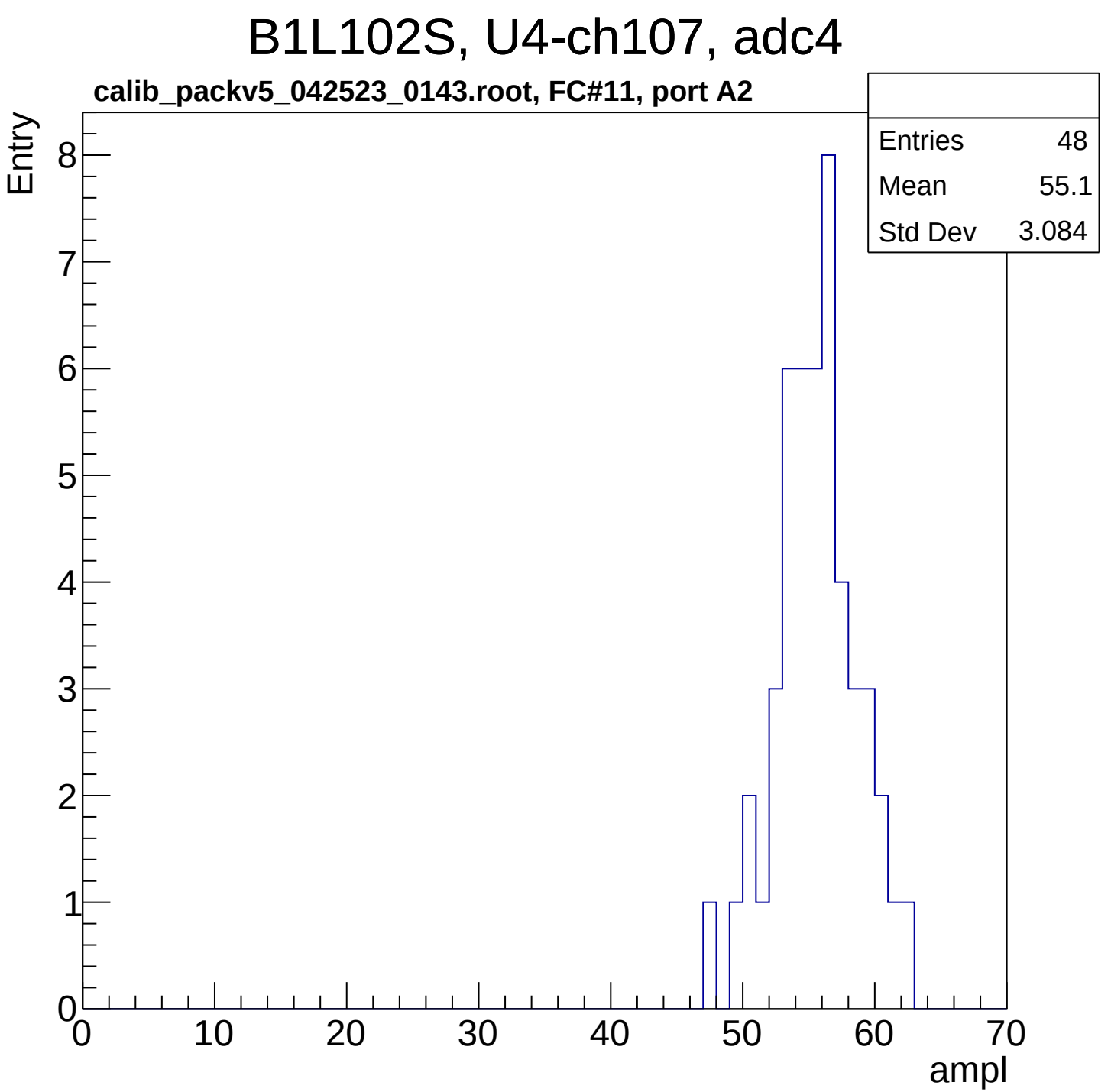
B1L102S, U4-ch107, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 48
Mean 55.1
Std Dev 3.084
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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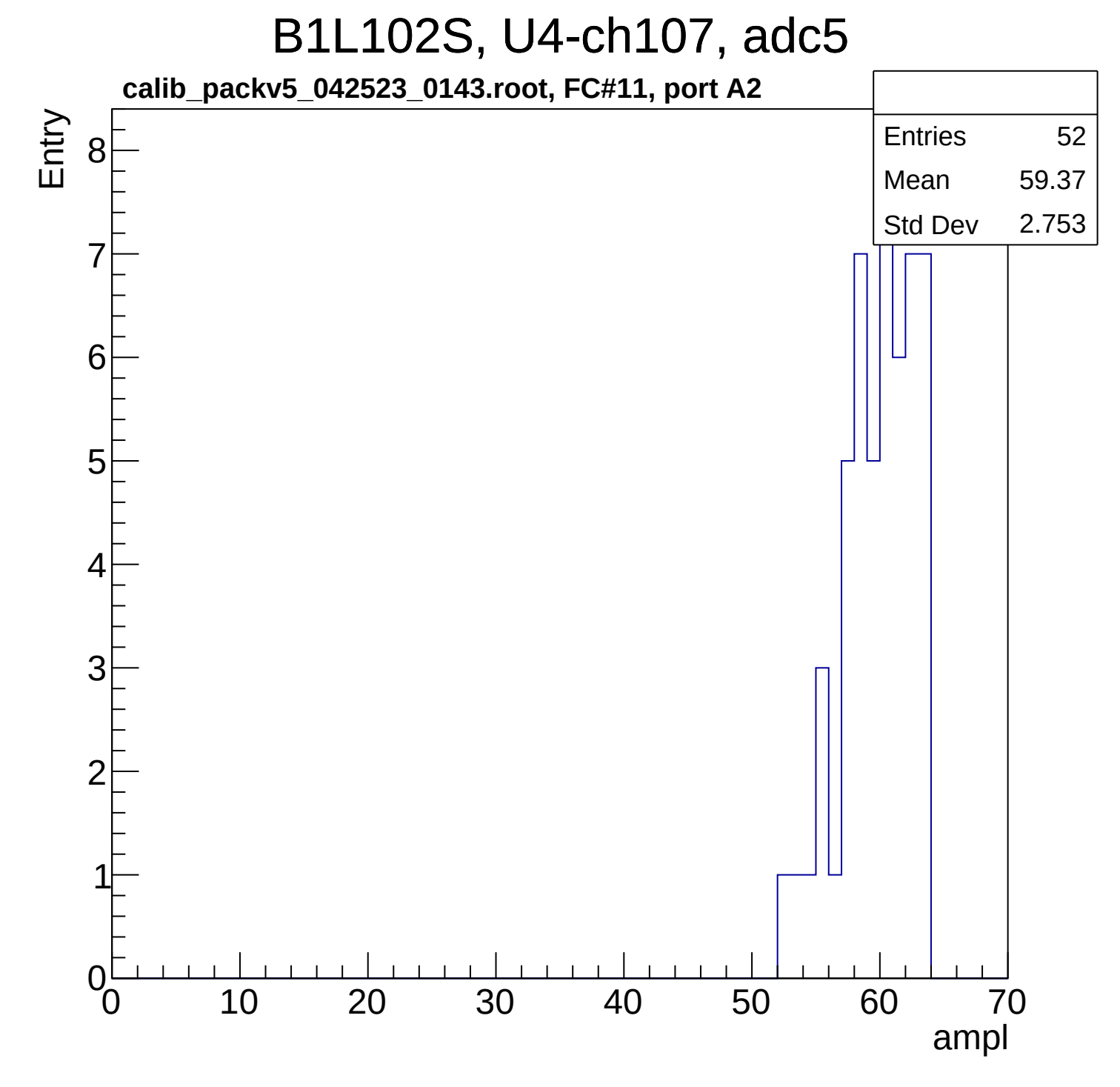
B1L102S, U4-ch107, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 52
Mean 59.37
Std Dev 2.753
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
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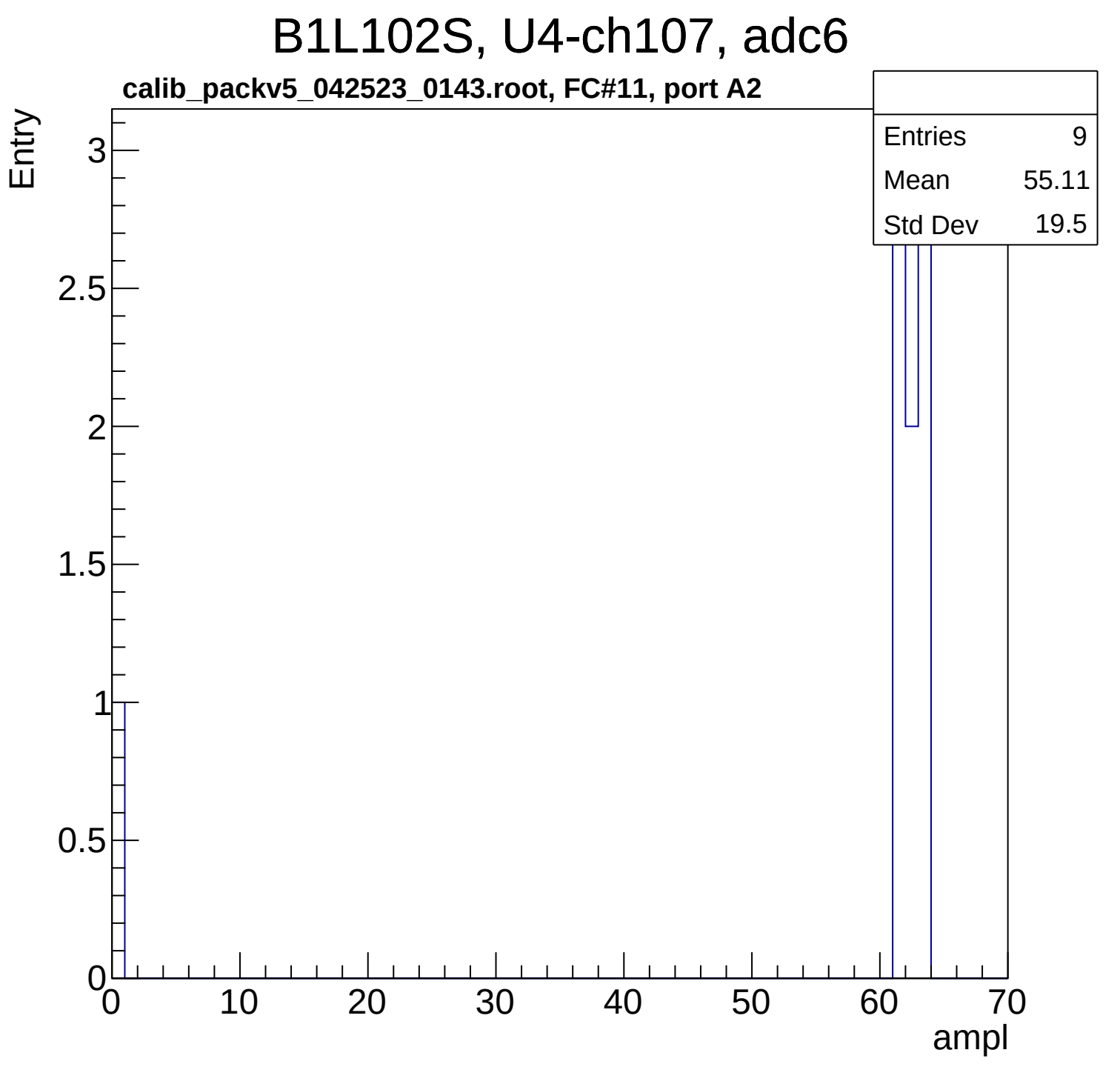
60
70


B1L102S, U4-ch107, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 9
Mean 55.11
Std Dev 19.5
Entry
ampl
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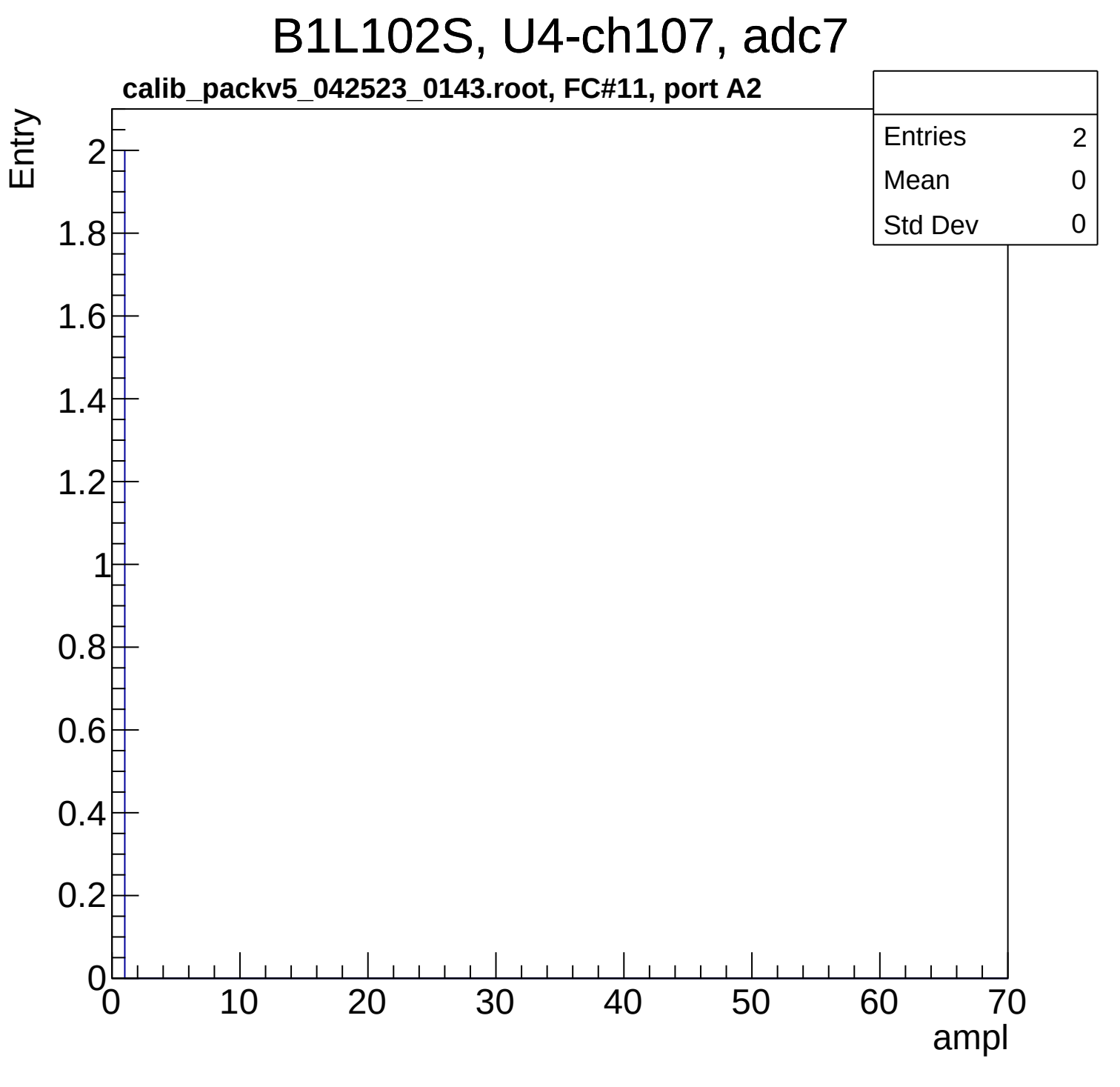
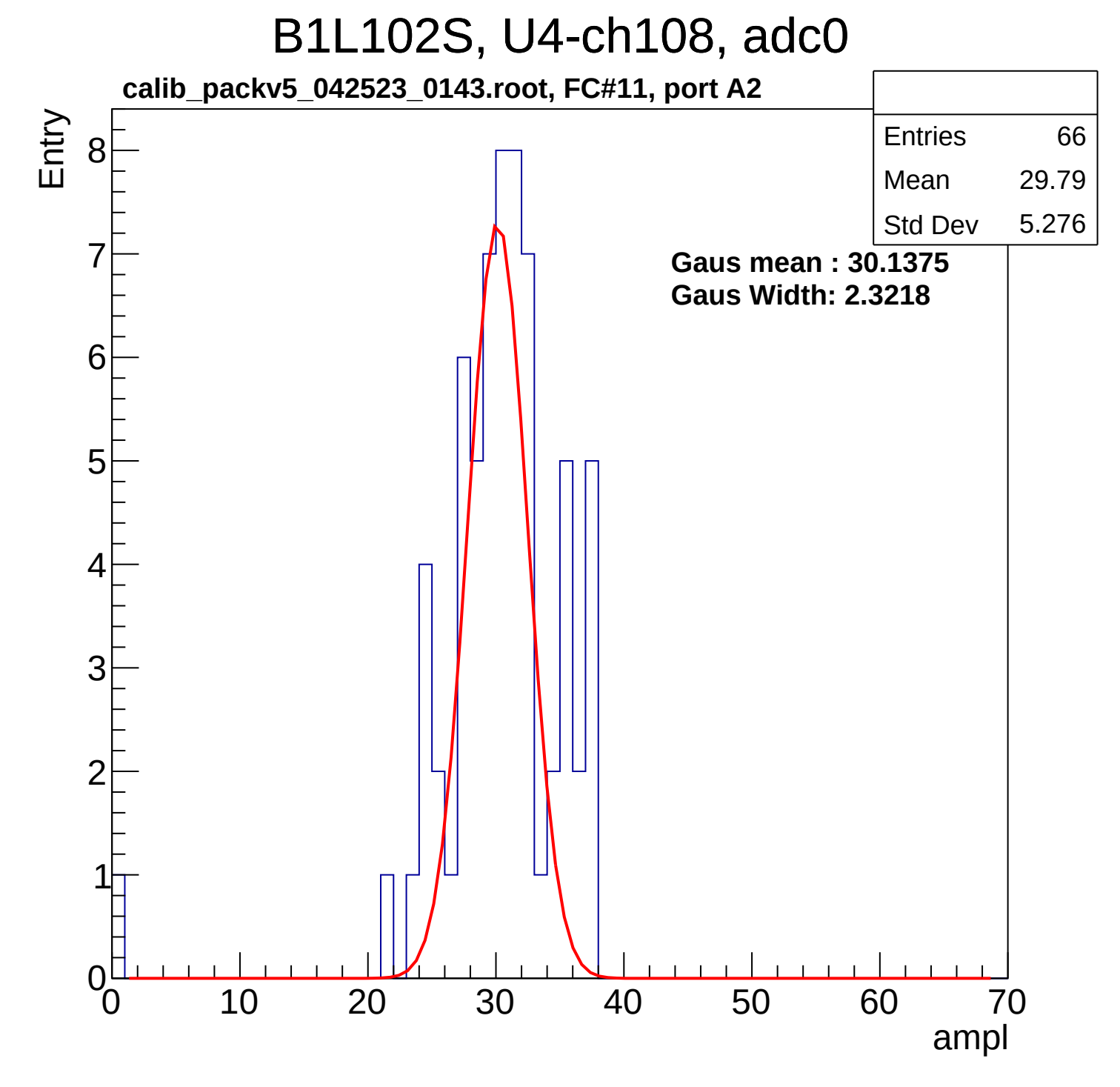
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U4-ch107, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L102S, U4-ch108, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 29.79
Std Dev 5.276
Gaus mean : 30.1375
Gaus Width: 2.3218
Entry
ampl
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1
2
3
4
5
6
7
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0
10
20
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40
50
60
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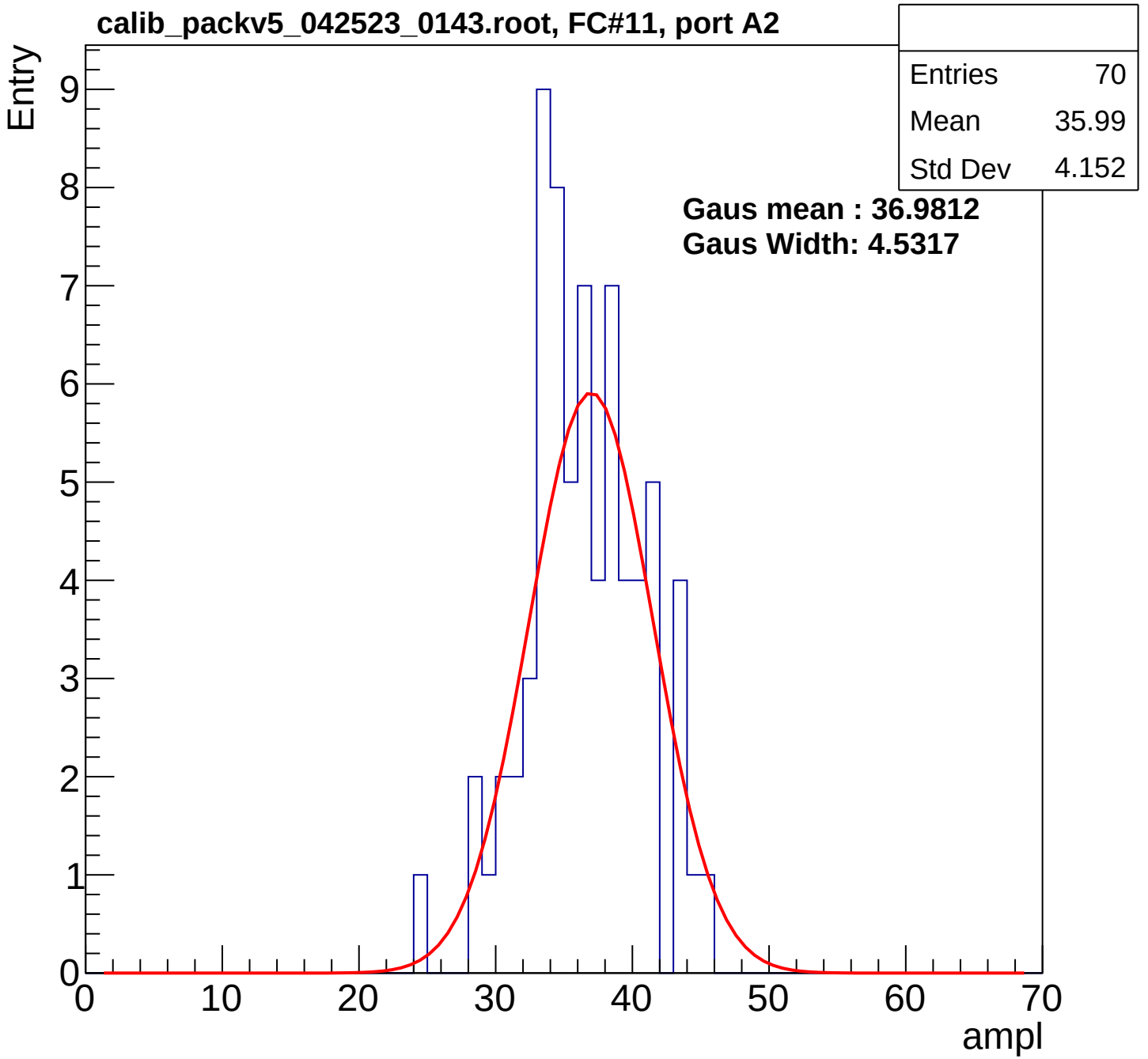
B1L102S, U4-ch108, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 35.99
Std Dev 4.152
Gaus mean : 36.9812
Gaus Width: 4.5317
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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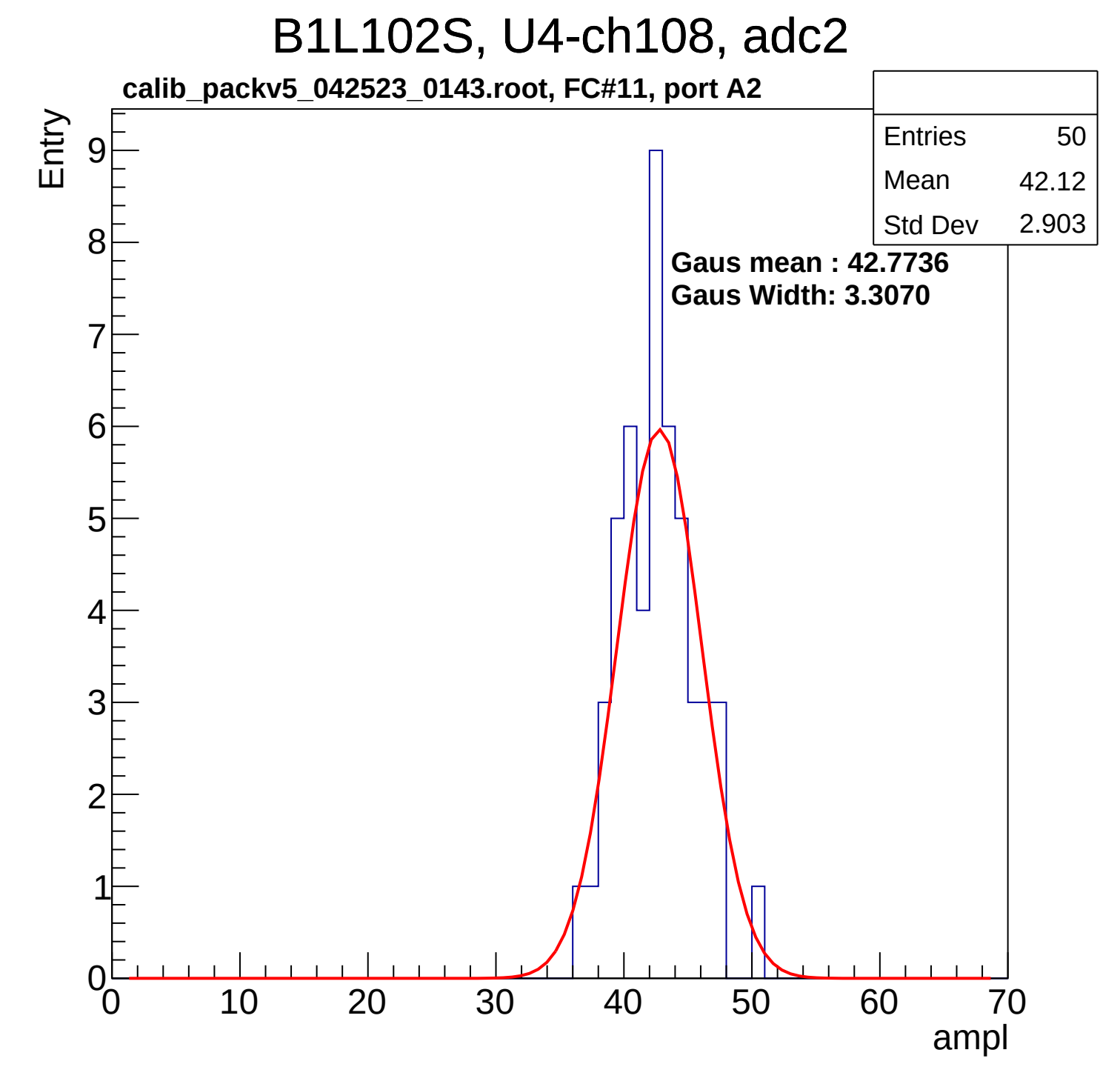
B1L102S, U4-ch108, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 50
Mean 42.12
Std Dev 2.903
Gaus mean : 42.7736
Gaus Width: 3.3070
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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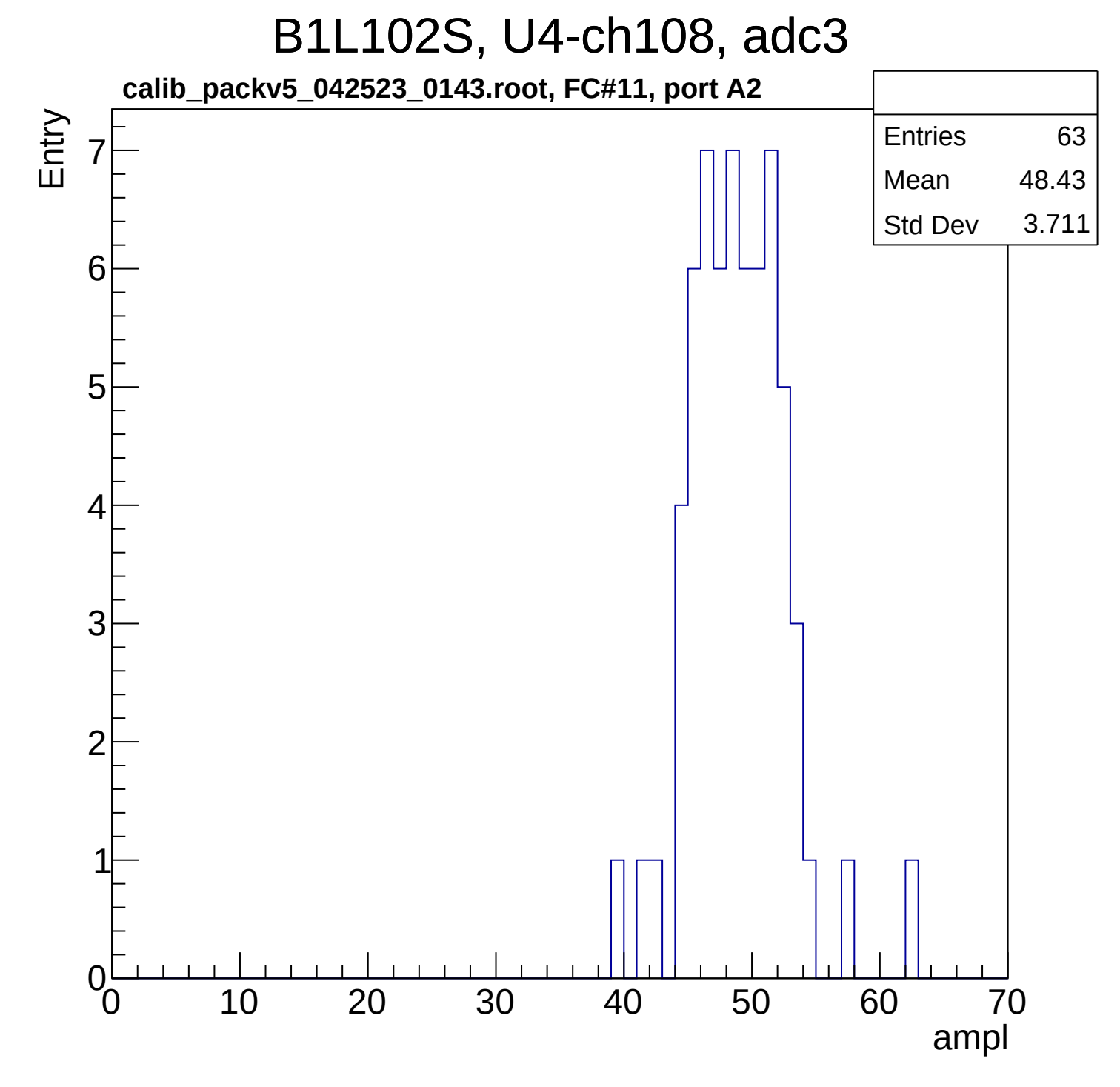
B1L102S, U4-ch108, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 48.43
Std Dev 3.711
Entry
ampl
0
1
2
3
4
5
6
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0
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20
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40
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60
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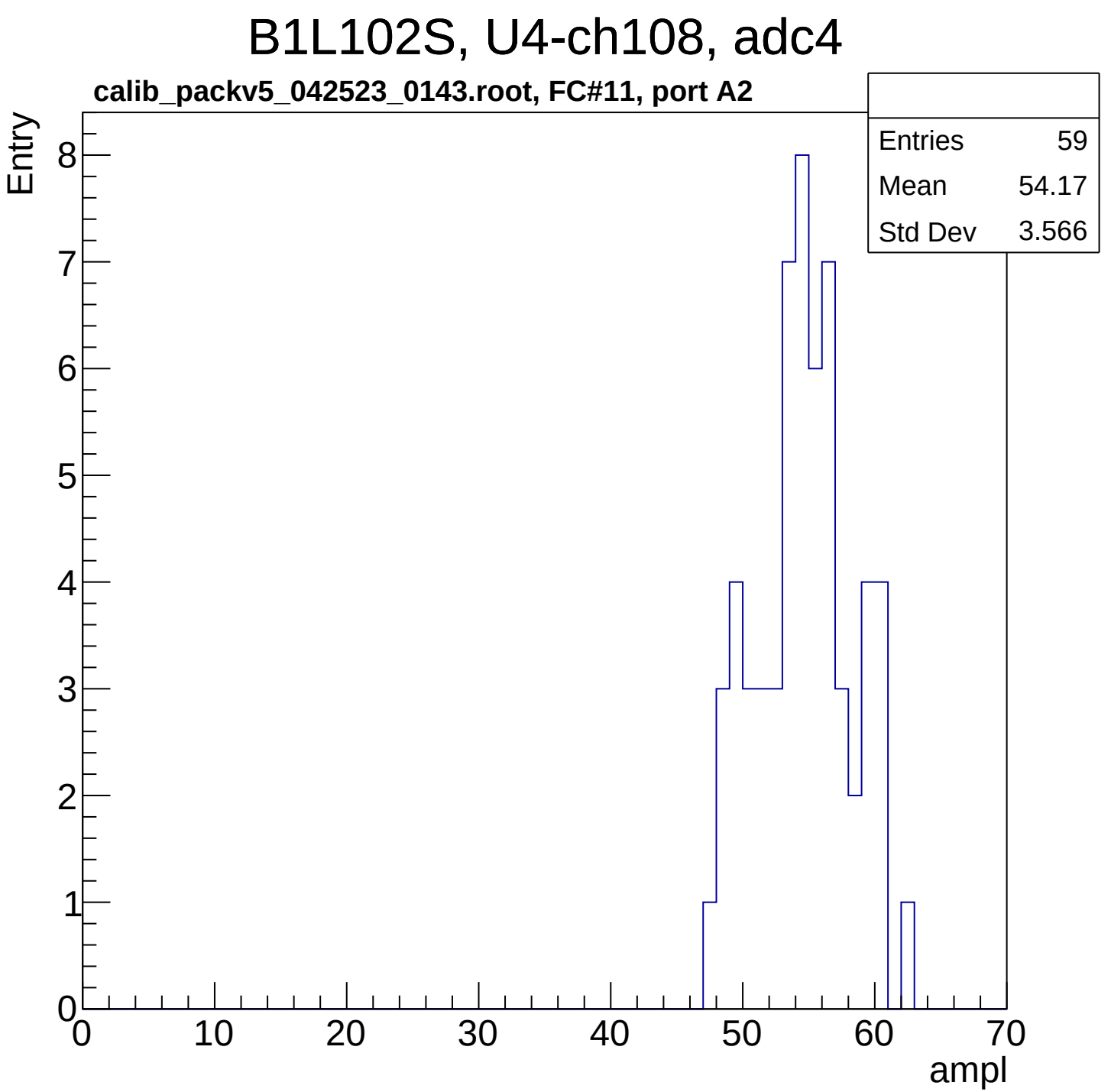
B1L102S, U4-ch108, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 54.17
Std Dev 3.566
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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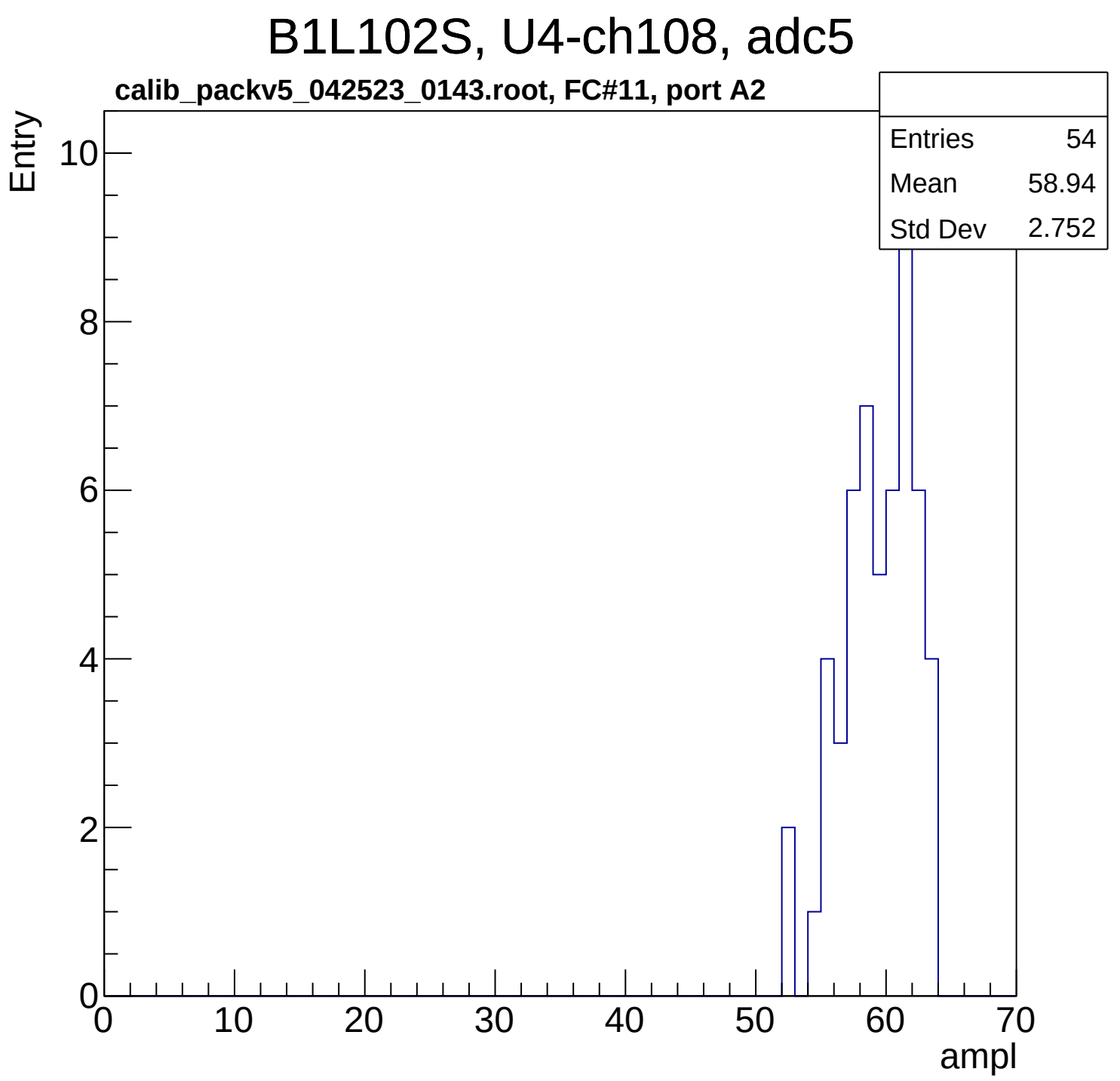
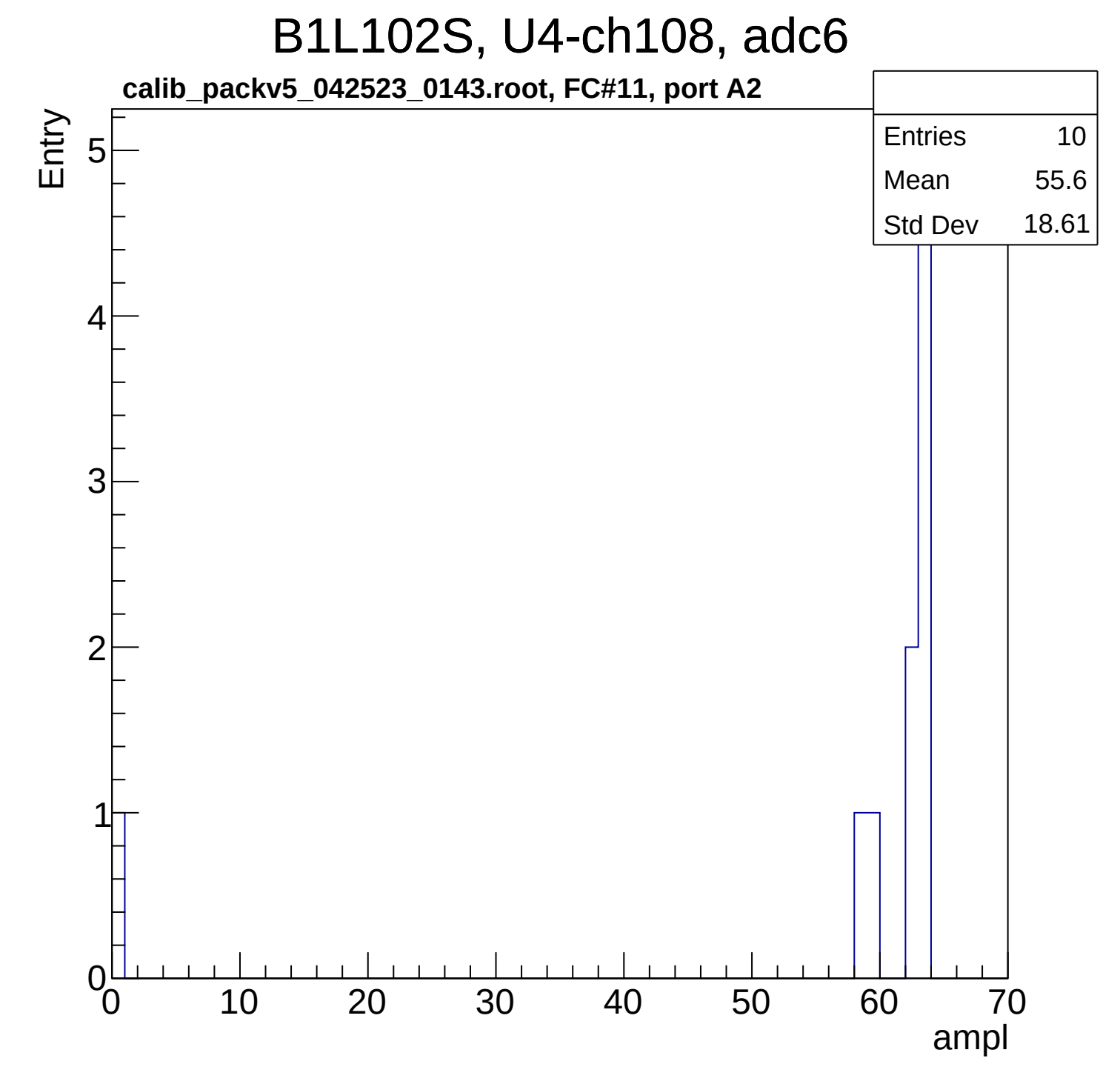
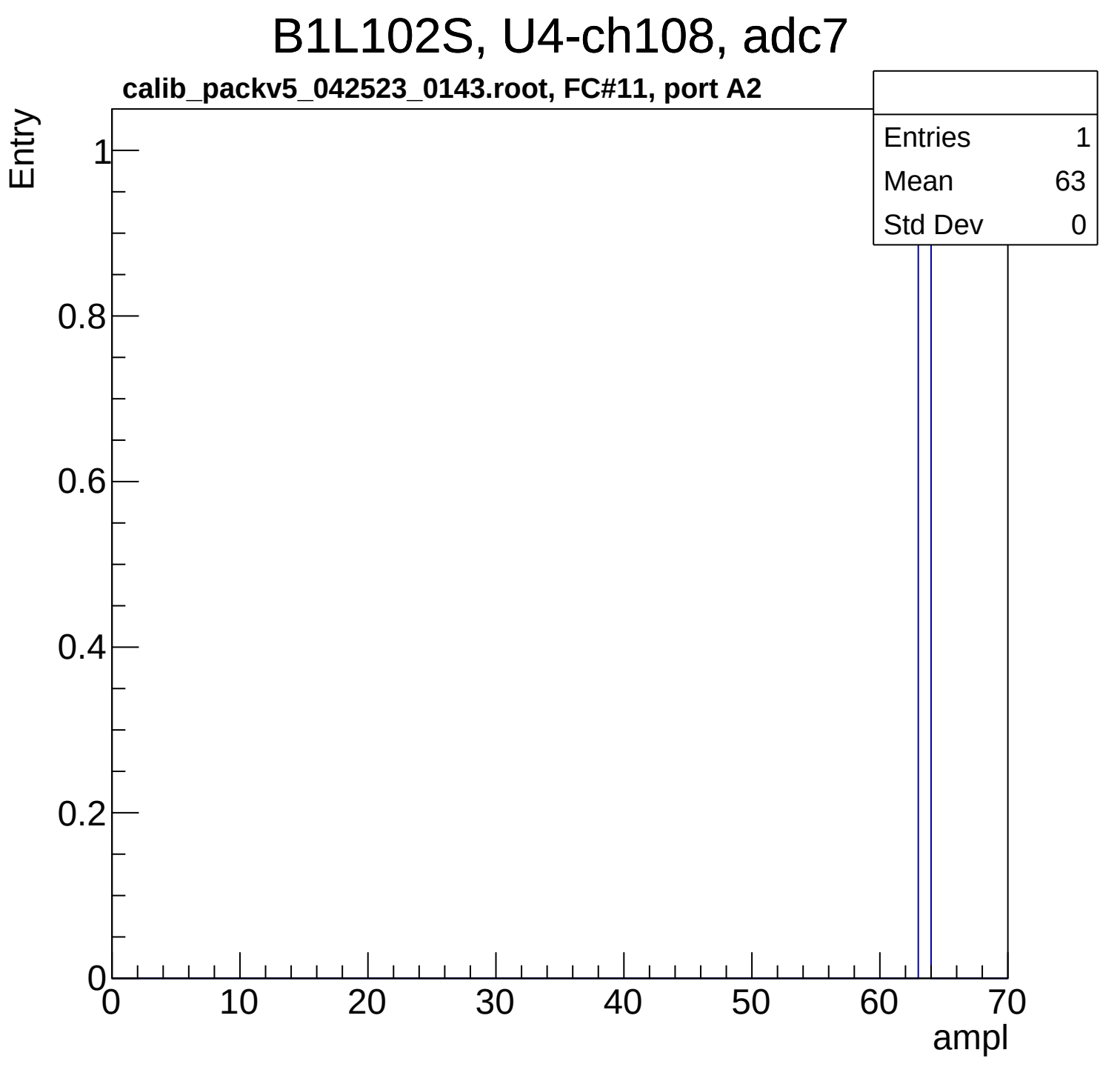
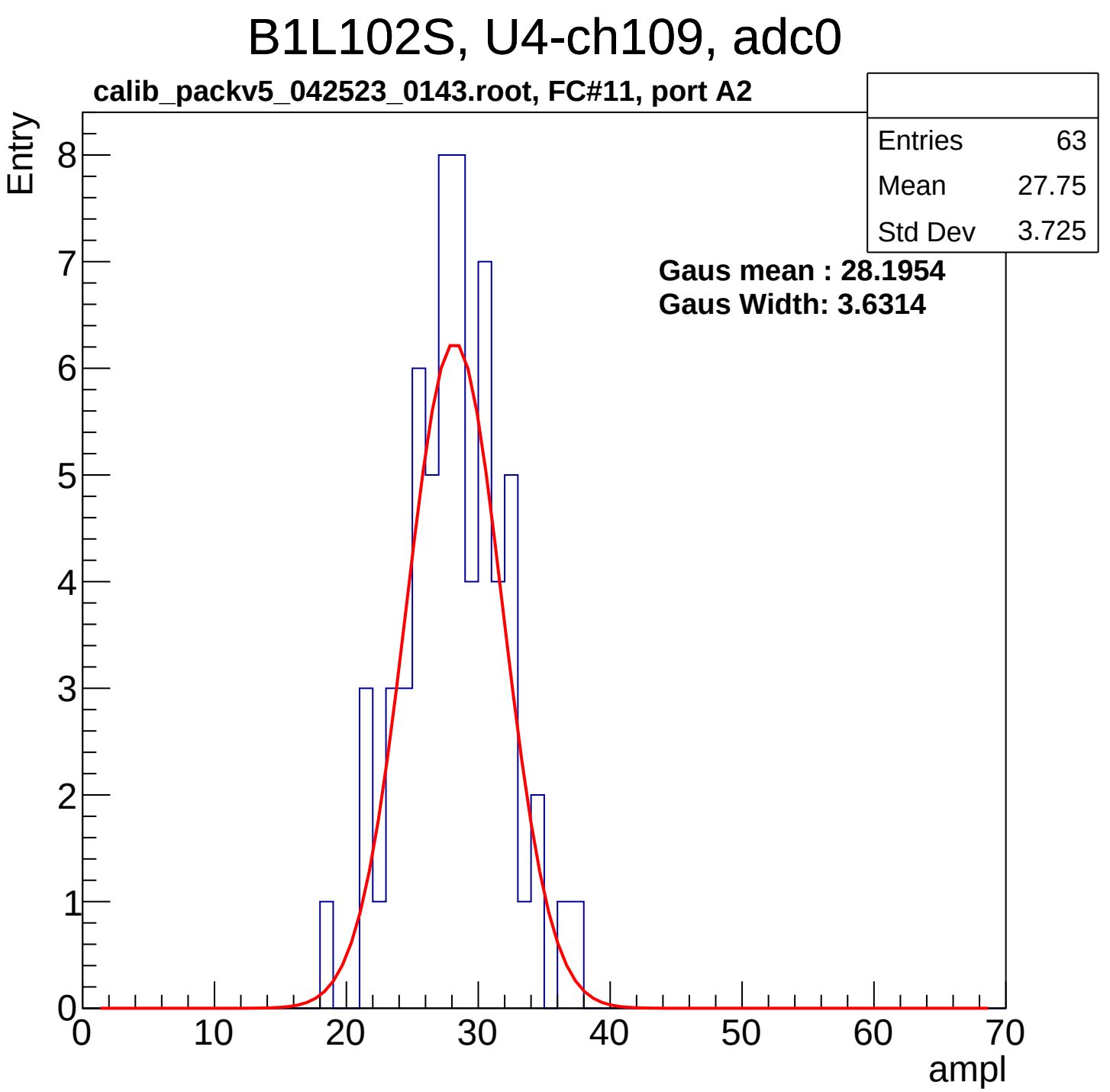

B1L102S, U4-ch108, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 58.94
Std Dev 2.752
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch108, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 10
Mean 55.6
Std Dev 18.61
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch108, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch109, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 27.75
Std Dev 3.725
Gaus mean : 28.1954
Gaus Width: 3.6314
Entry
ampl
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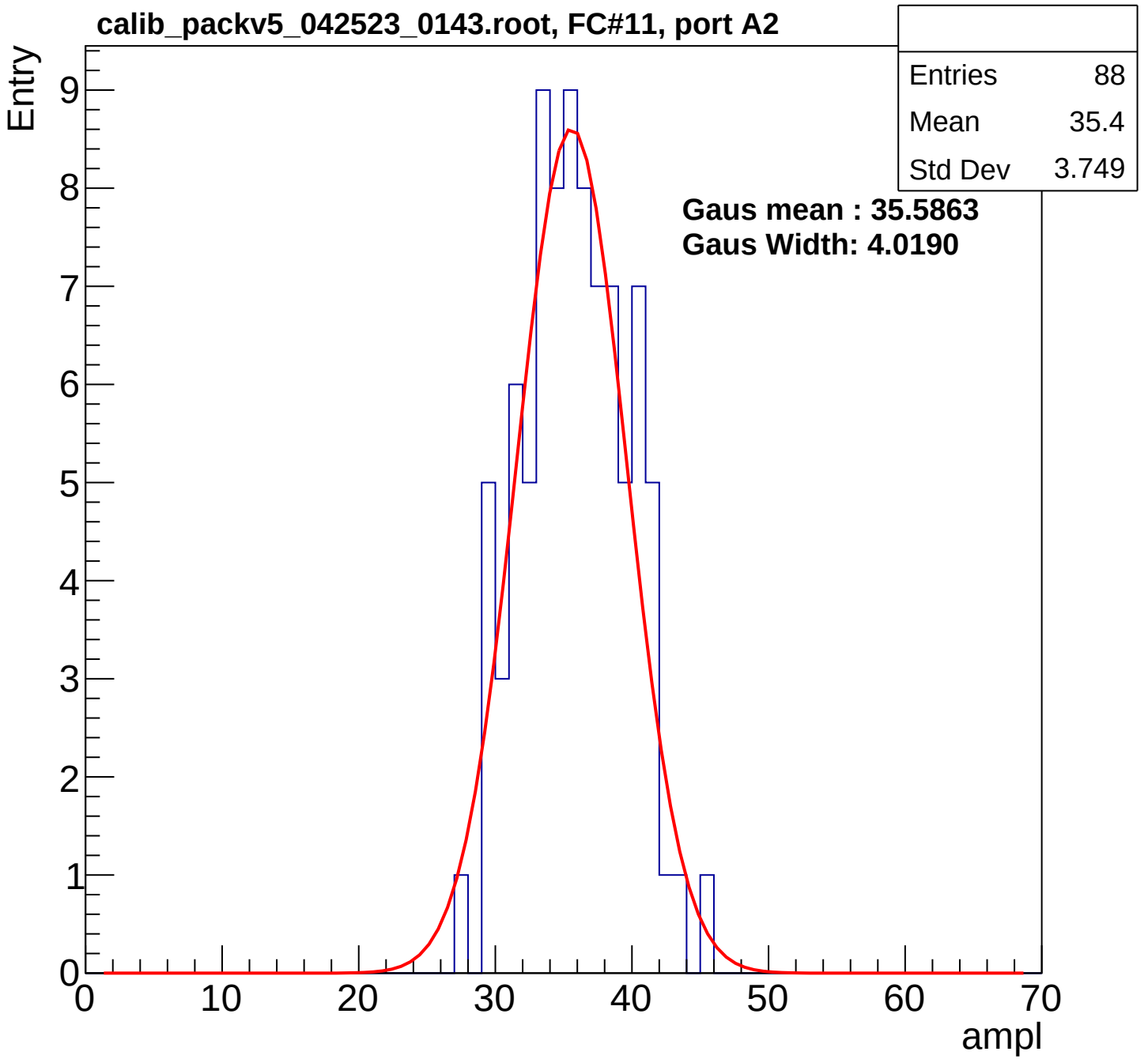
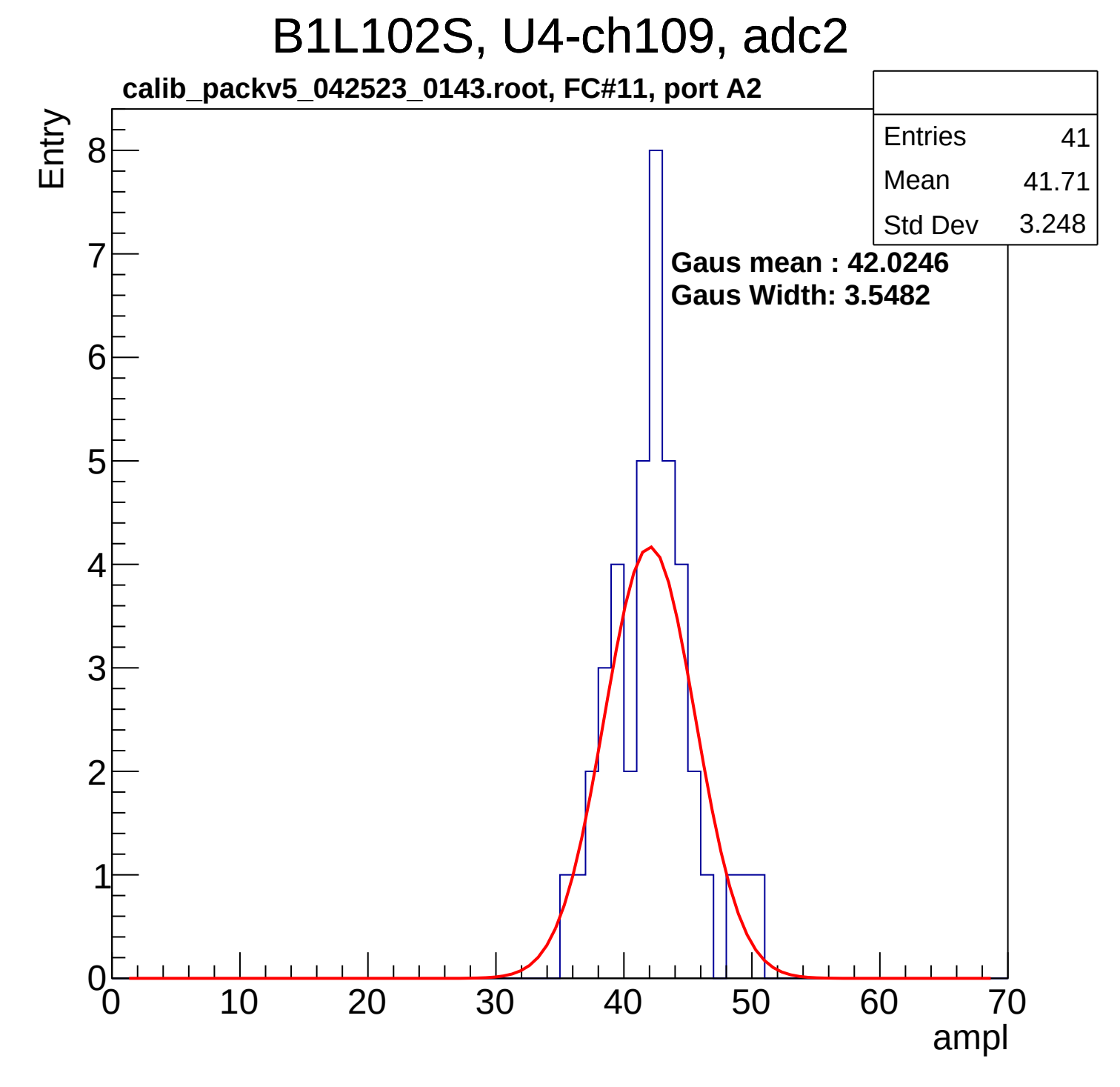
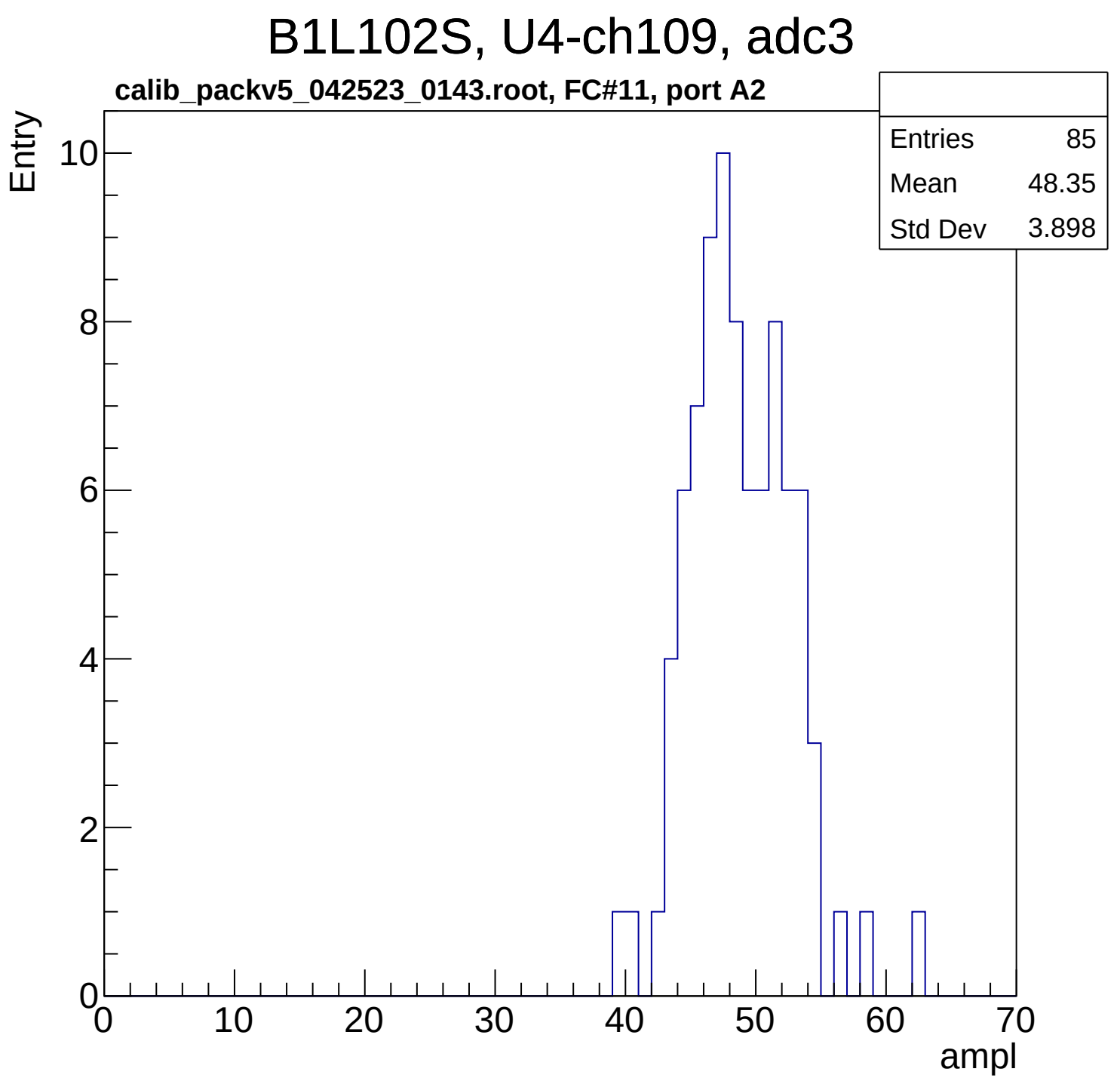
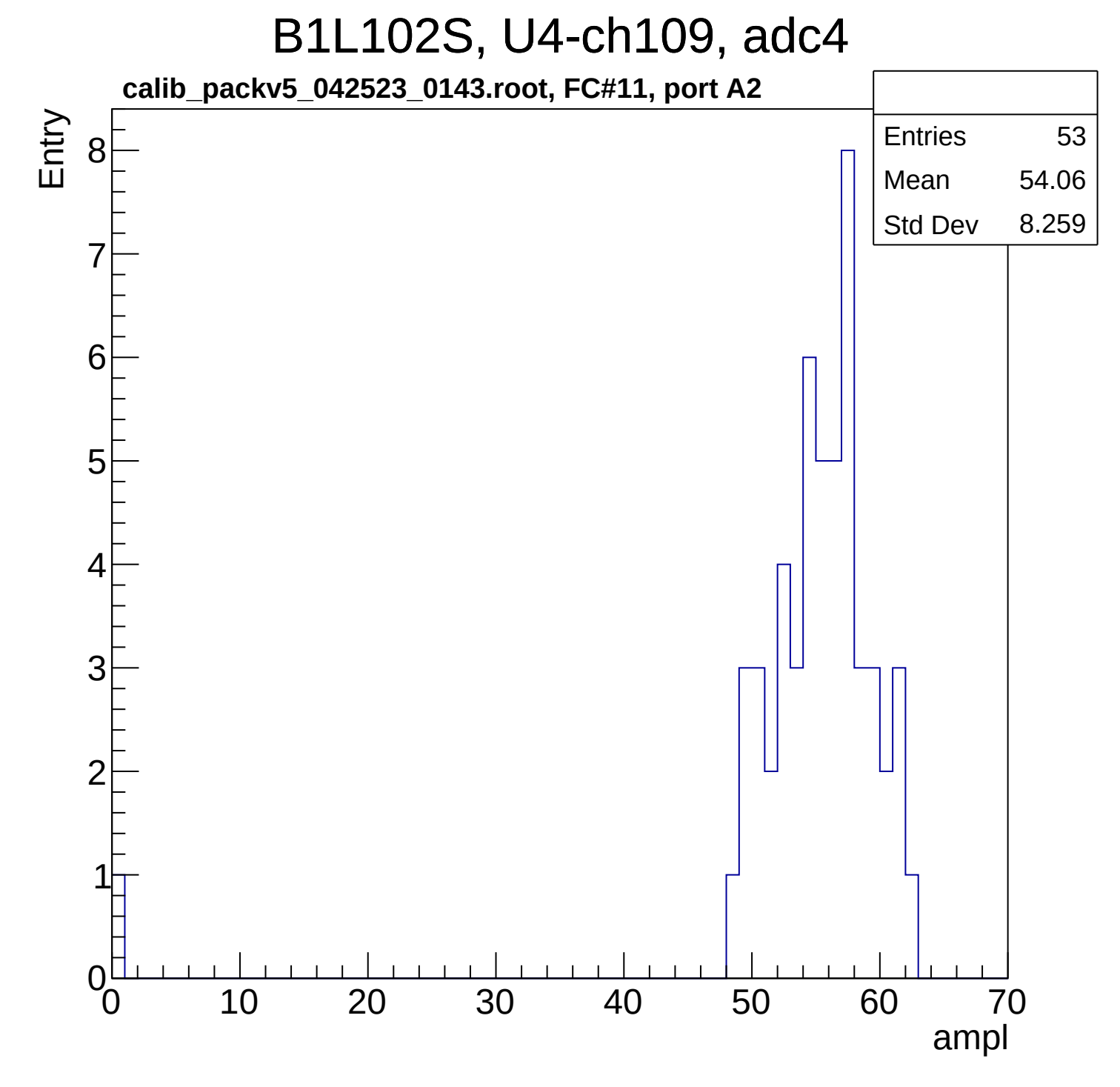
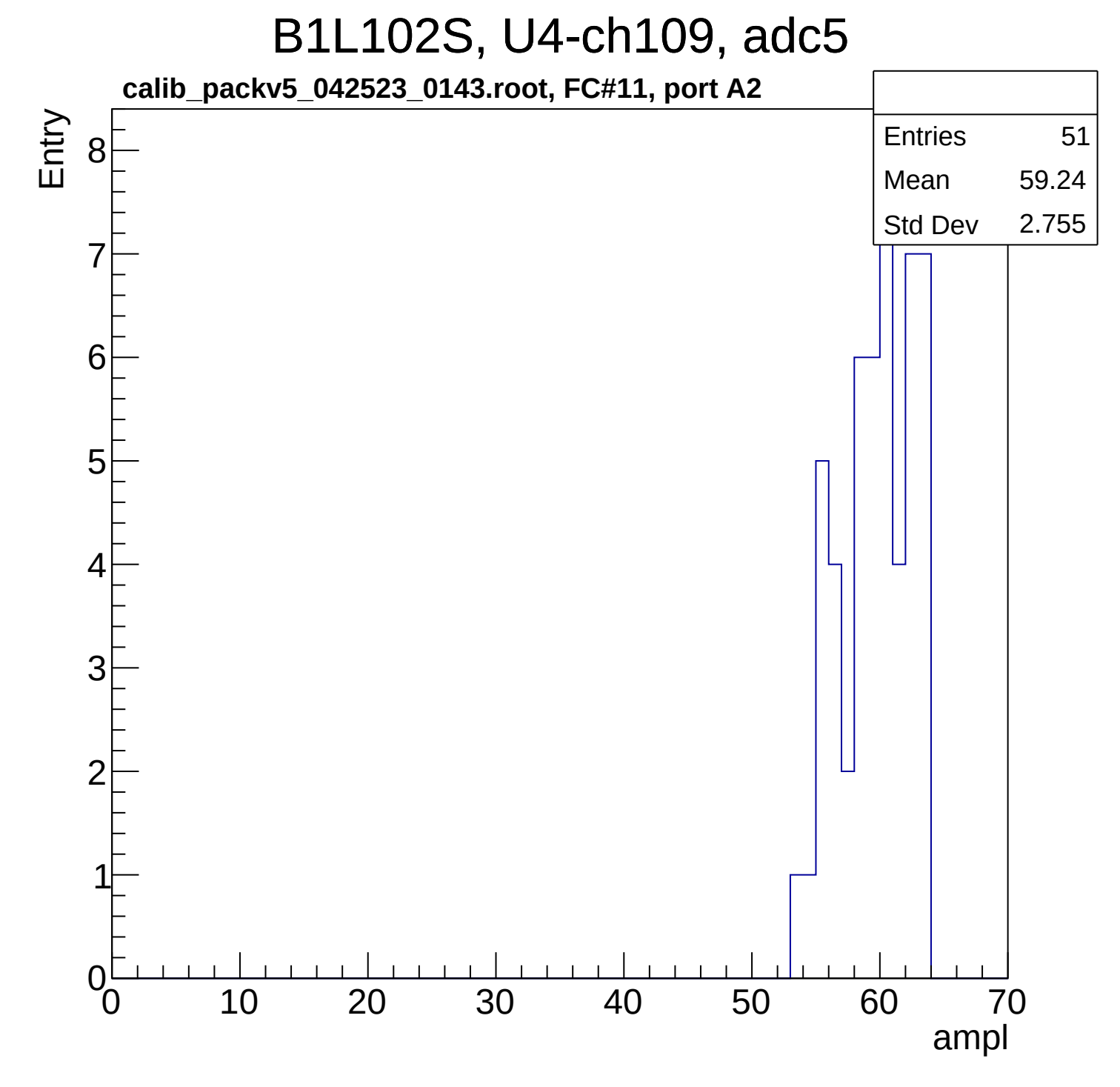
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch109, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 88
Mean 35.4
Std Dev 3.749
Gaus mean : 35.5863
Gaus Width: 4.0190
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch109, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 41
Mean 41.71
Std Dev 3.248
Gaus mean : 42.0246
Gaus Width: 3.5482
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch109, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 85
Mean 48.35
Std Dev 3.898
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch109, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 54.06
Std Dev 8.259
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch109, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 59.24
Std Dev 2.755
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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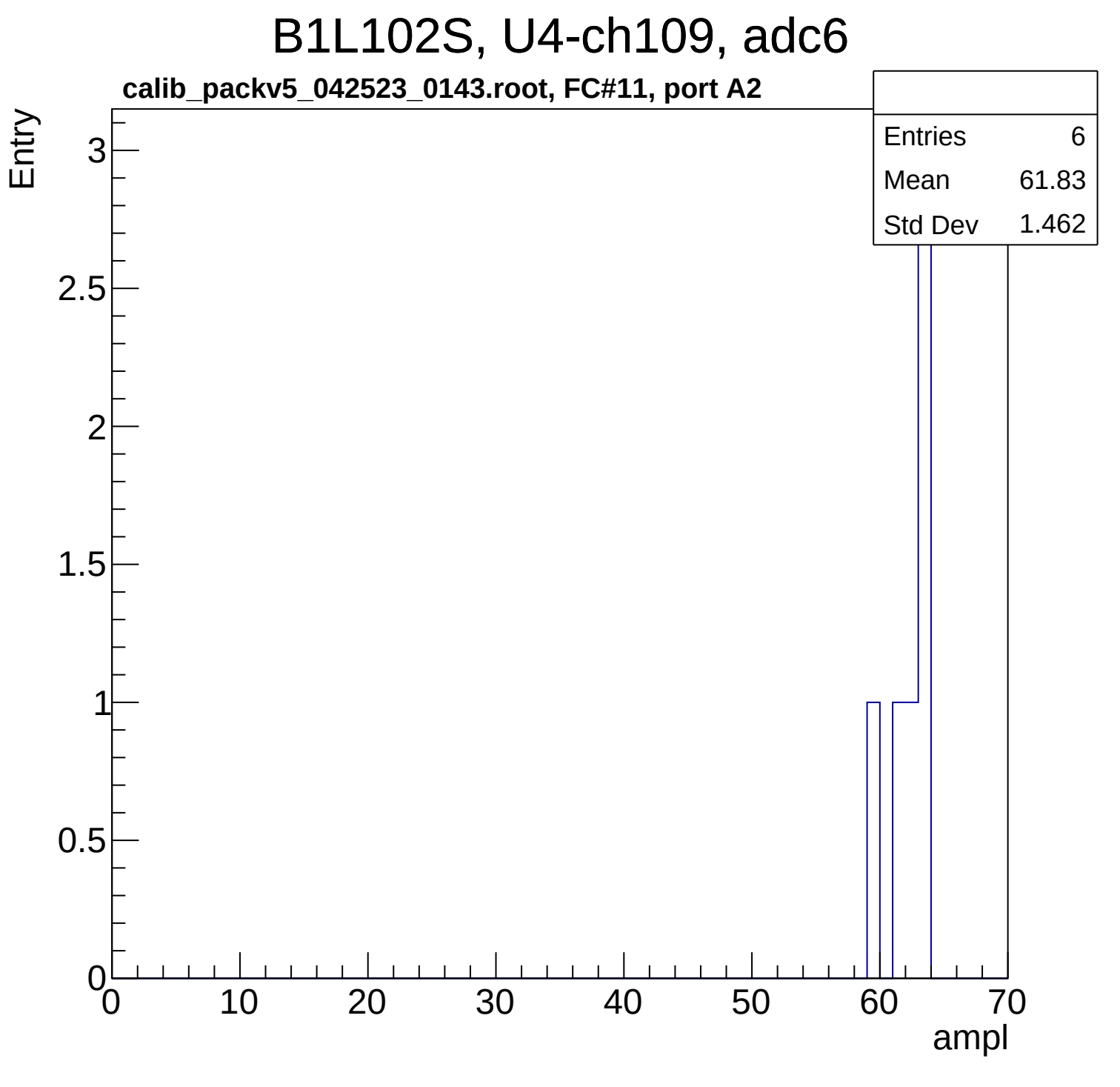
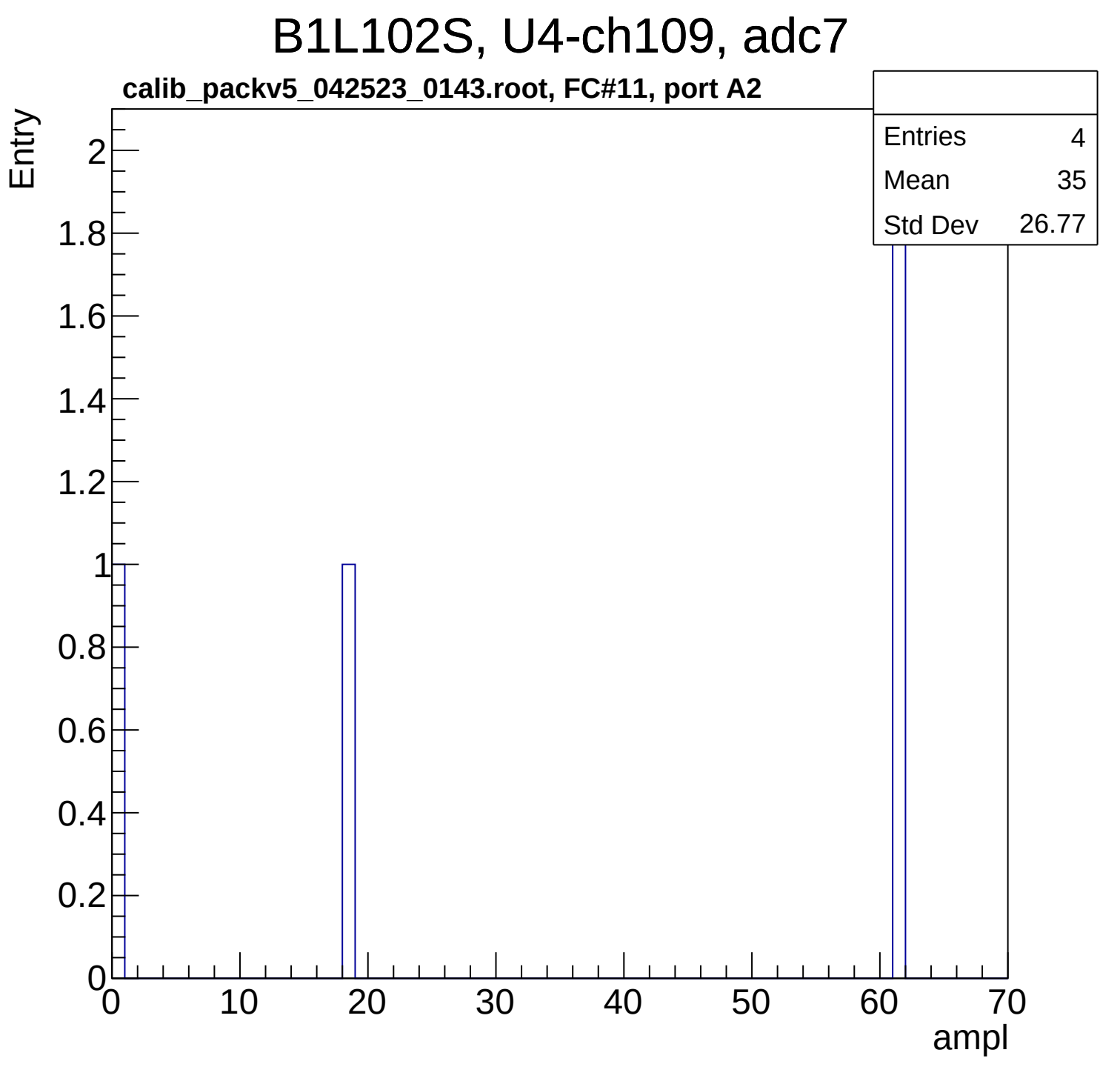
40
50
60
70


B1L102S, U4-ch109, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 6
Mean 61.83
Std Dev 1.462
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U4-ch109, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 4
Mean 35
Std Dev 26.77
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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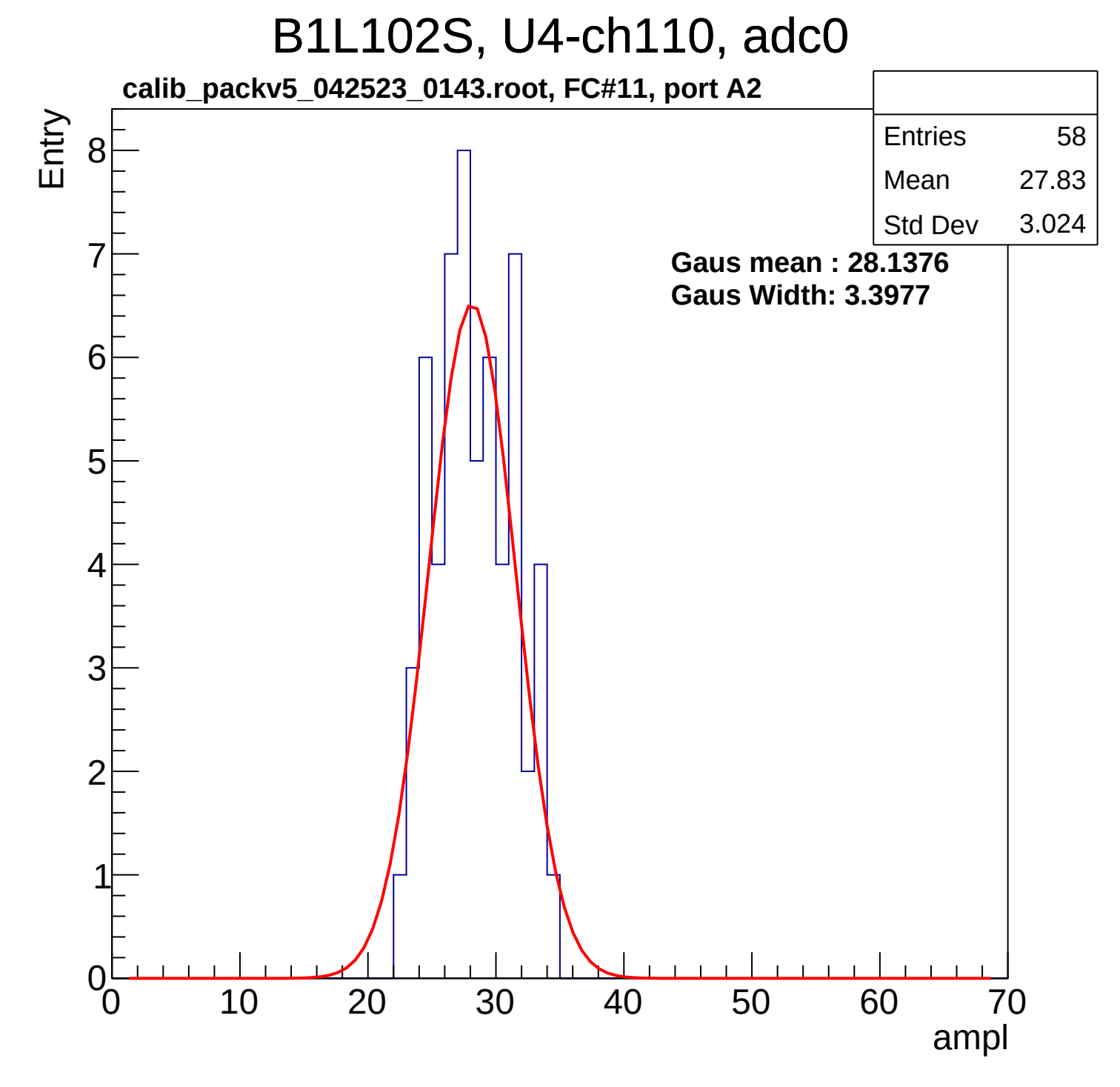
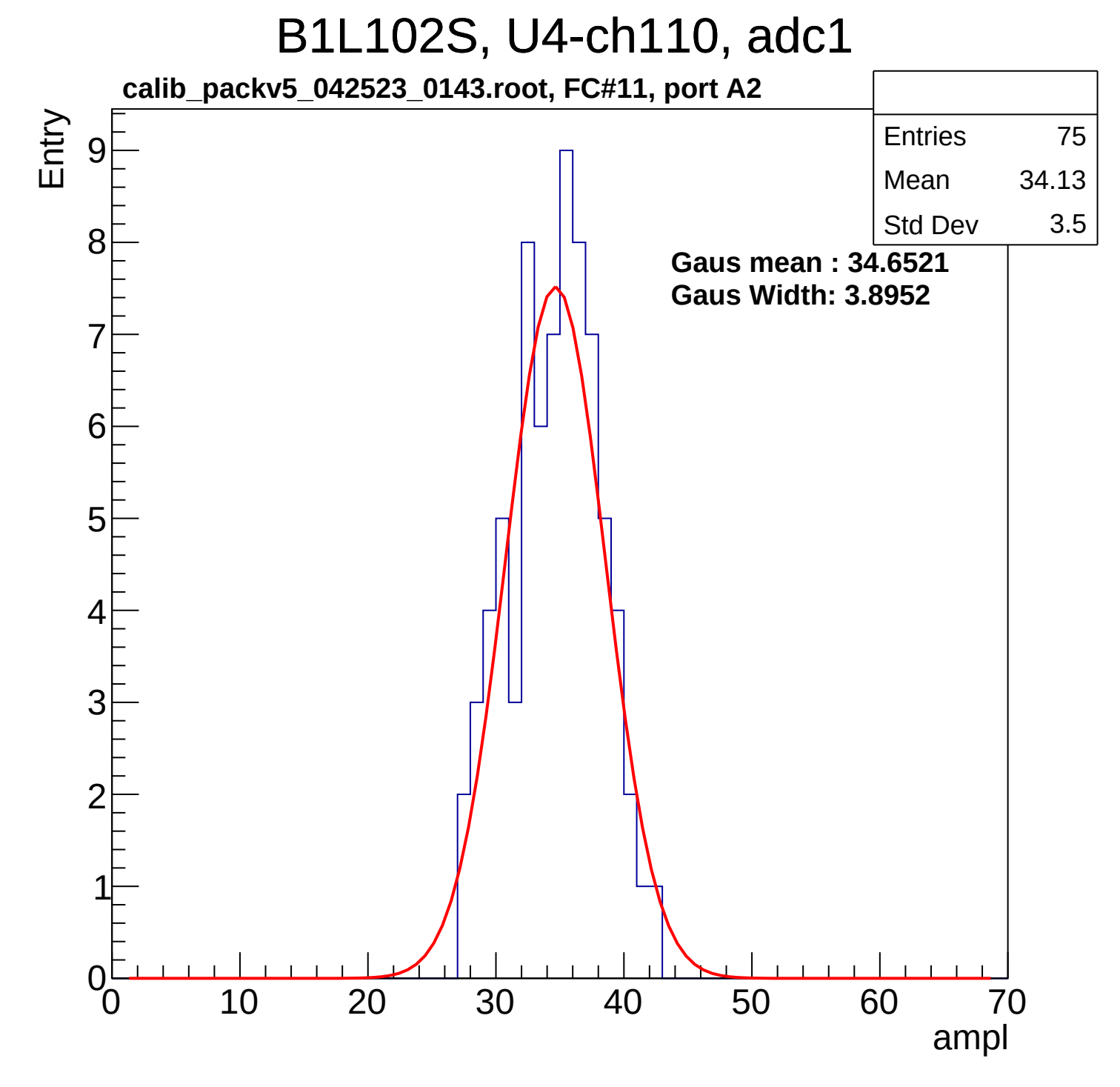
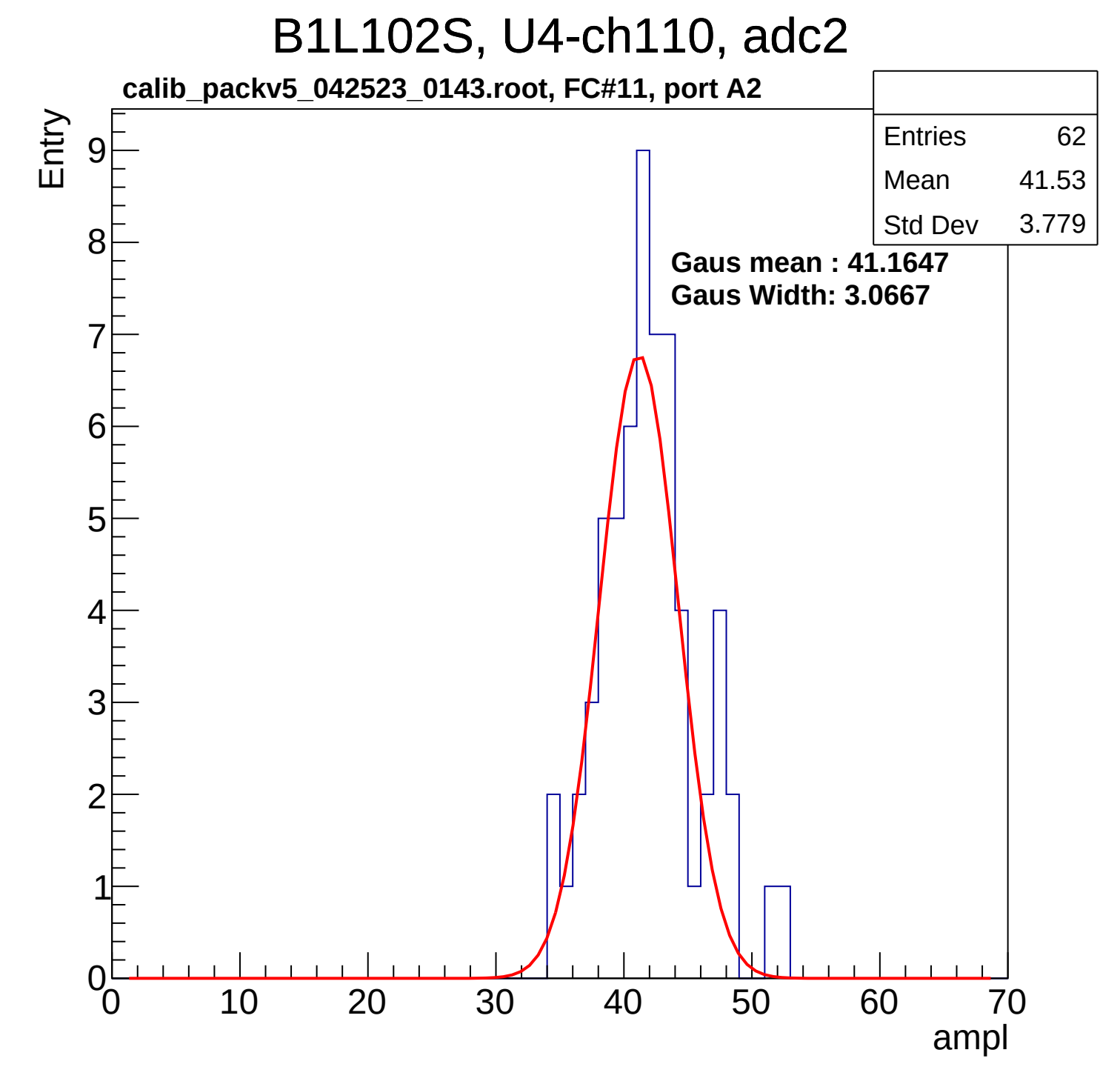

B1L102S, U4-ch110, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 27.83
Std Dev 3.024
Gaus mean : 28.1376
Gaus Width: 3.3977
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch110, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 34.13
Std Dev 3.5
Gaus mean : 34.6521
Gaus Width: 3.8952
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L102S, U4-ch110, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 41.53
Std Dev 3.779
Gaus mean : 41.1647
Gaus Width: 3.0667
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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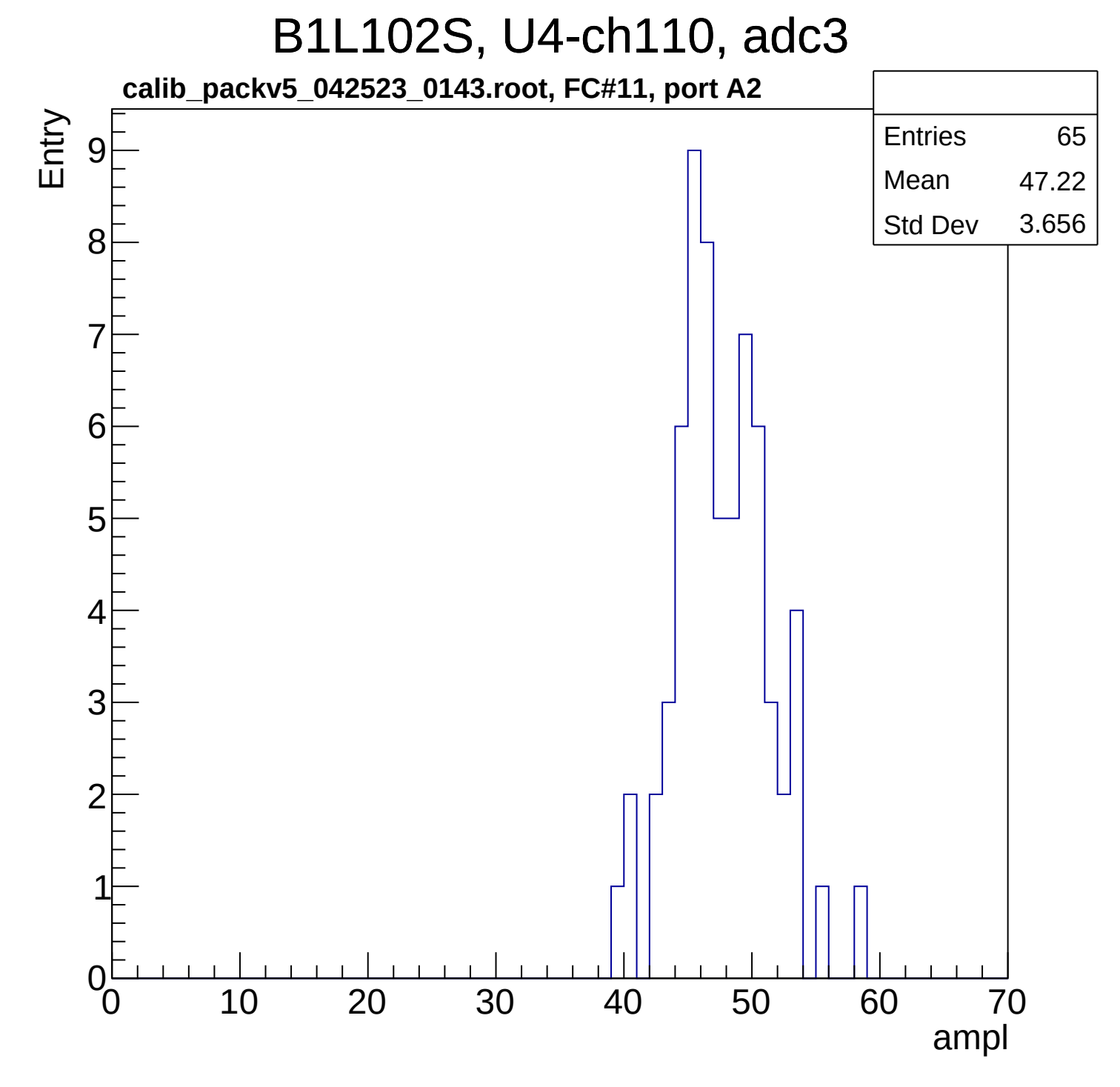
B1L102S, U4-ch110, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 47.22
Std Dev 3.656
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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60
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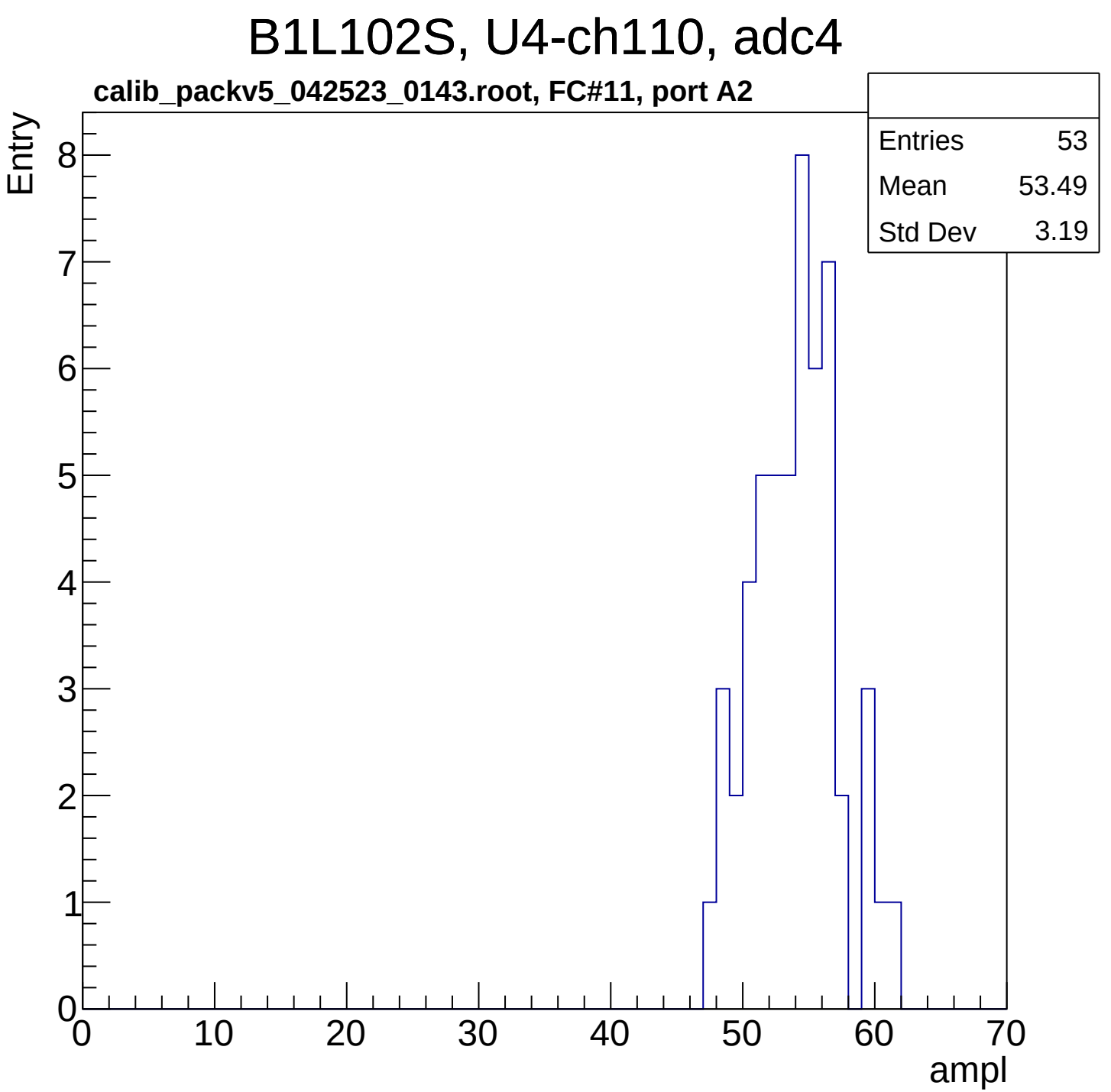
B1L102S, U4-ch110, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 53.49
Std Dev 3.19
Entry
ampl
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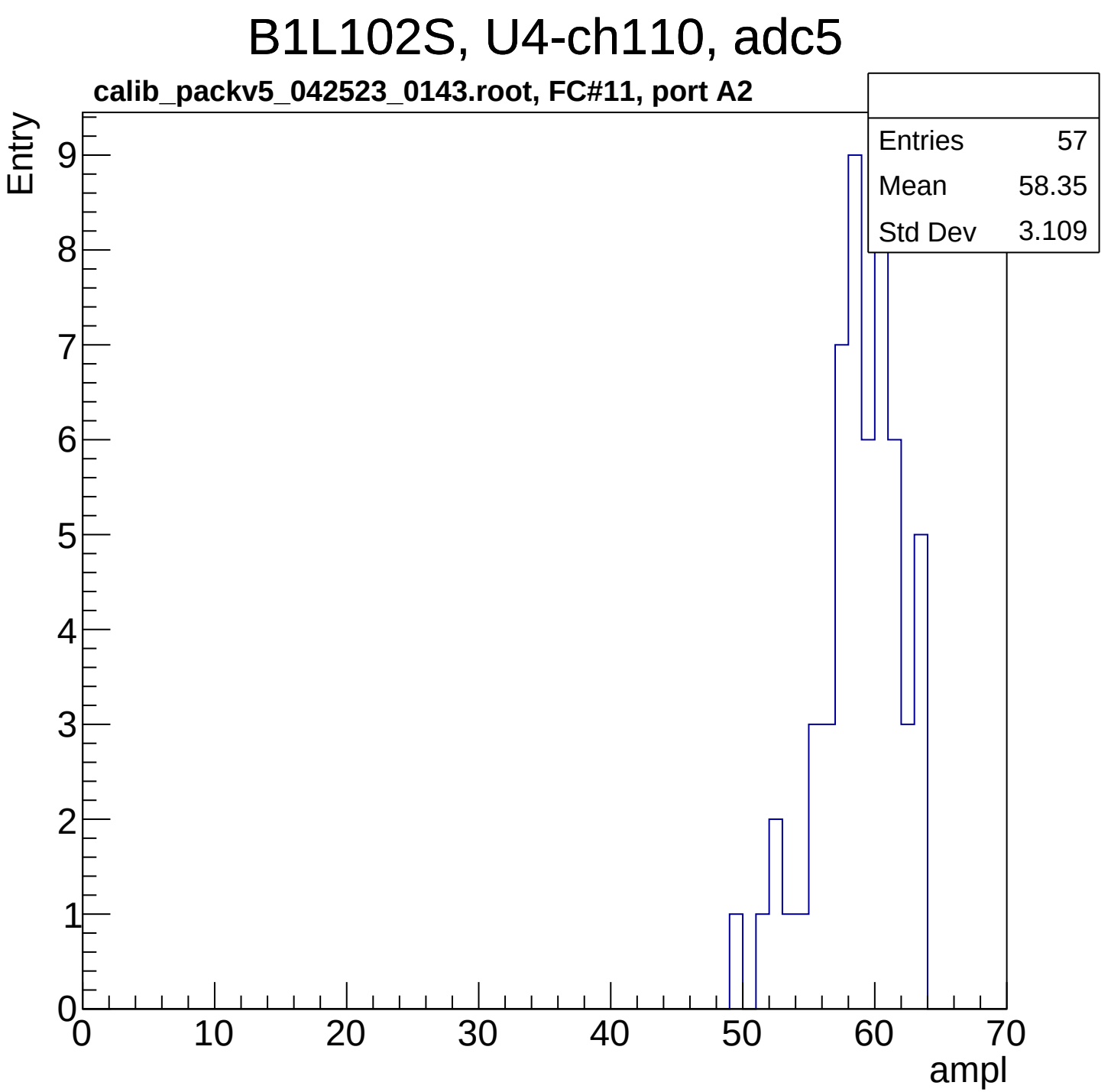
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch110, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 57
Mean 58.35
Std Dev 3.109
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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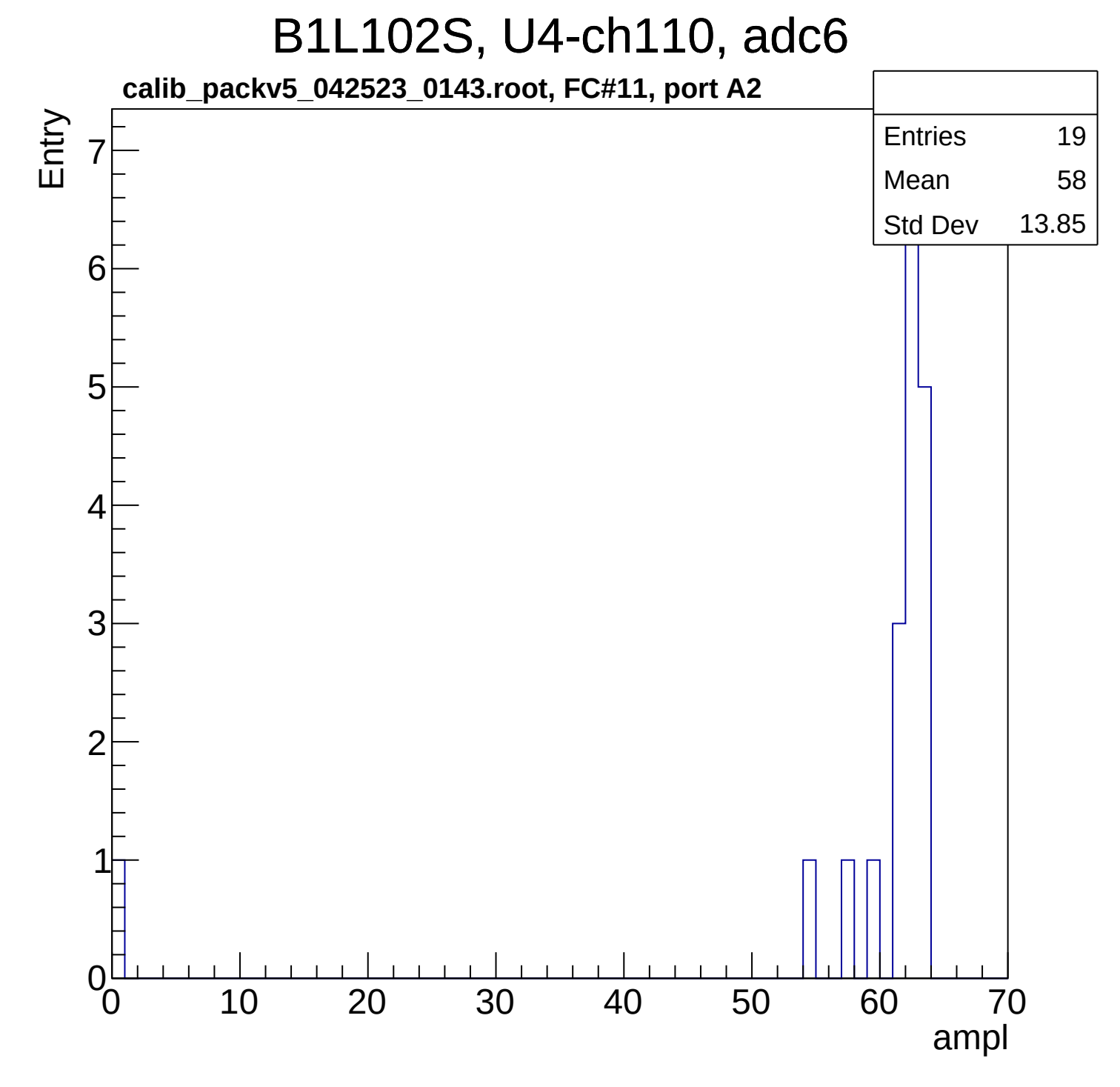
B1L102S, U4-ch110, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 19
Mean 58
Std Dev 13.85
Entry
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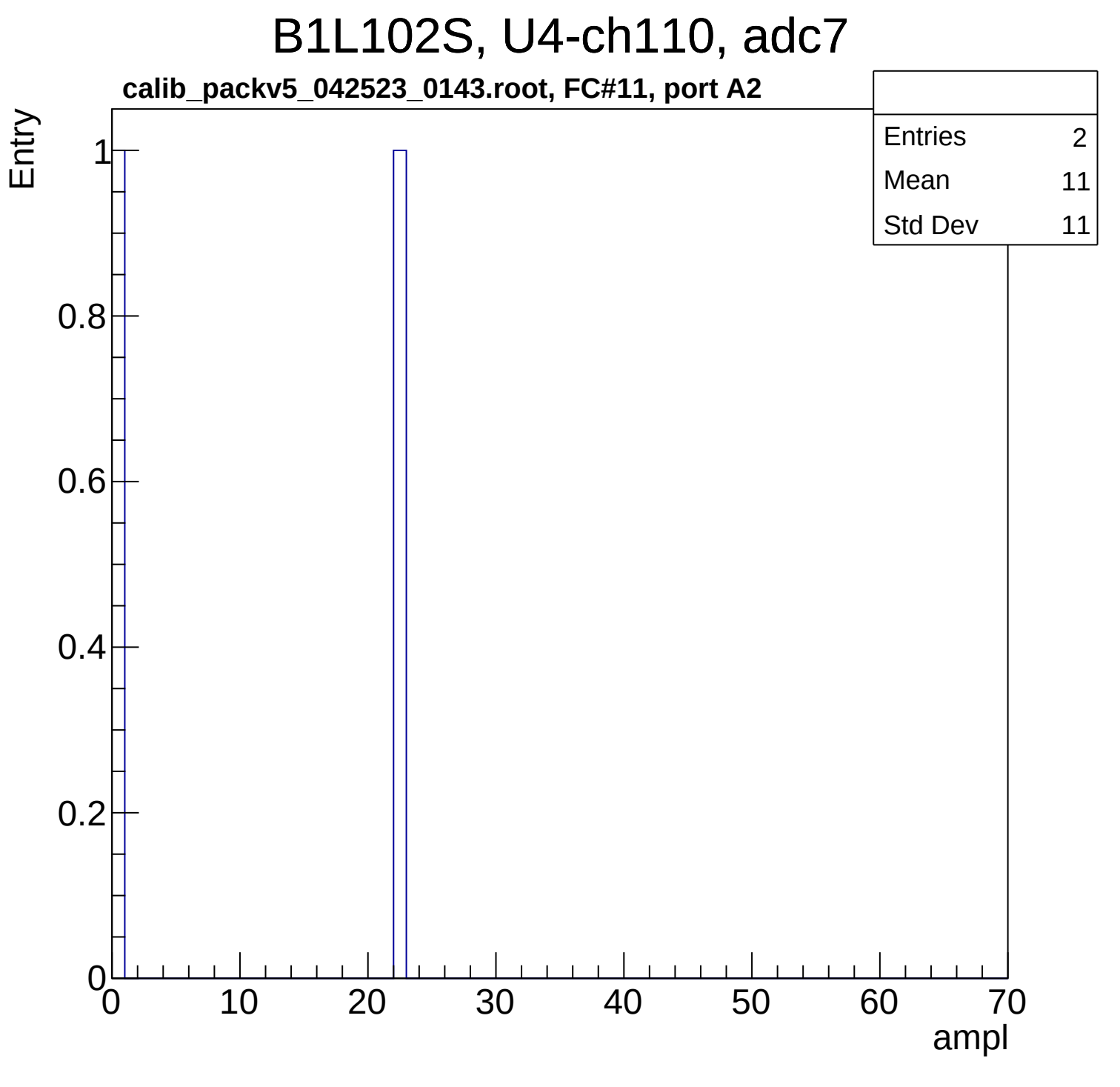
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch110, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 11
Std Dev 11
Entry
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0.6
0.4
0.2
0
0
10
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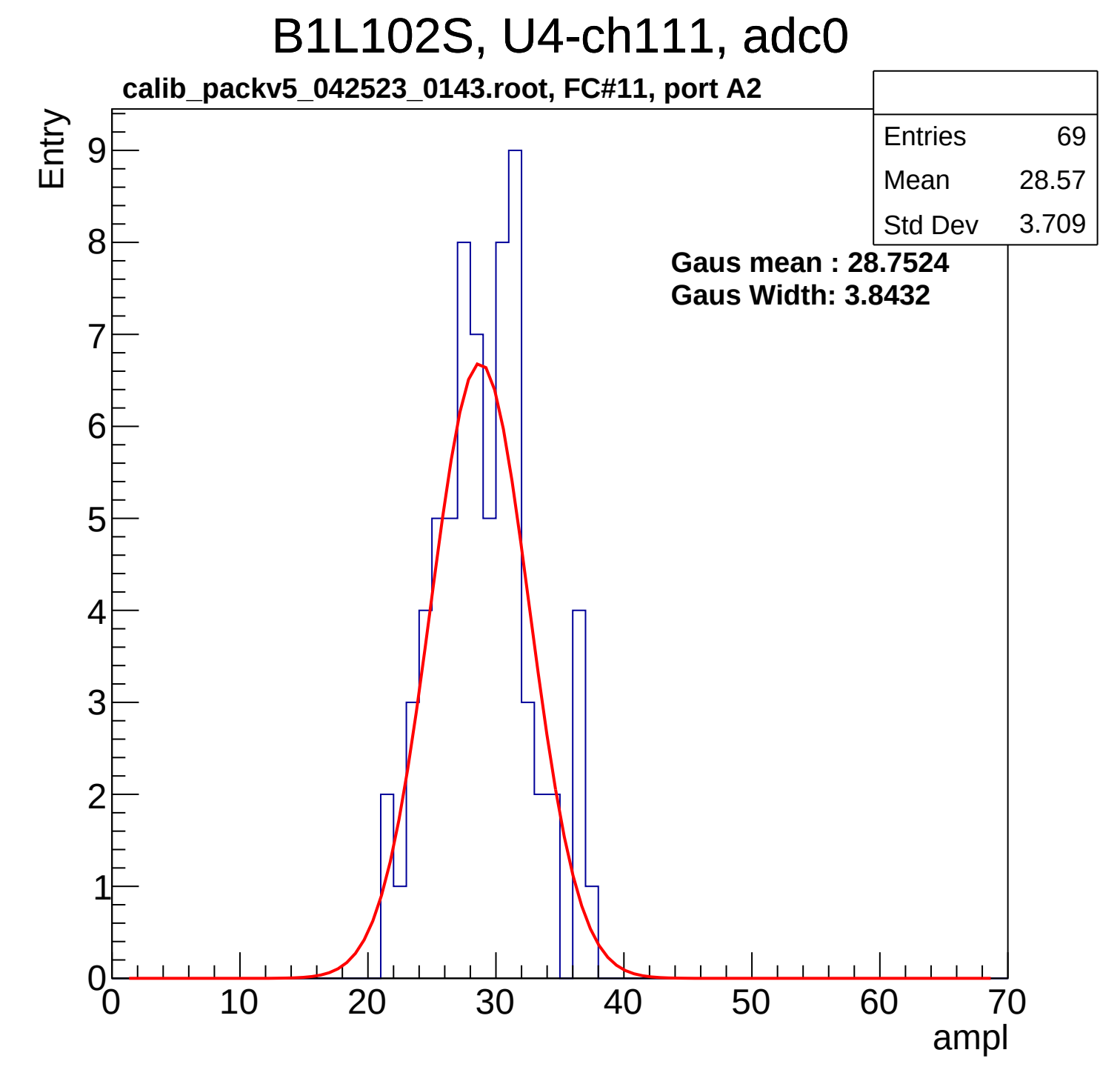
30
40
50
60
70
ampl


B1L102S, U4-ch111, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 28.57
Std Dev 3.709
Gaus mean : 28.7524
Gaus Width: 3.8432
Entry
ampl
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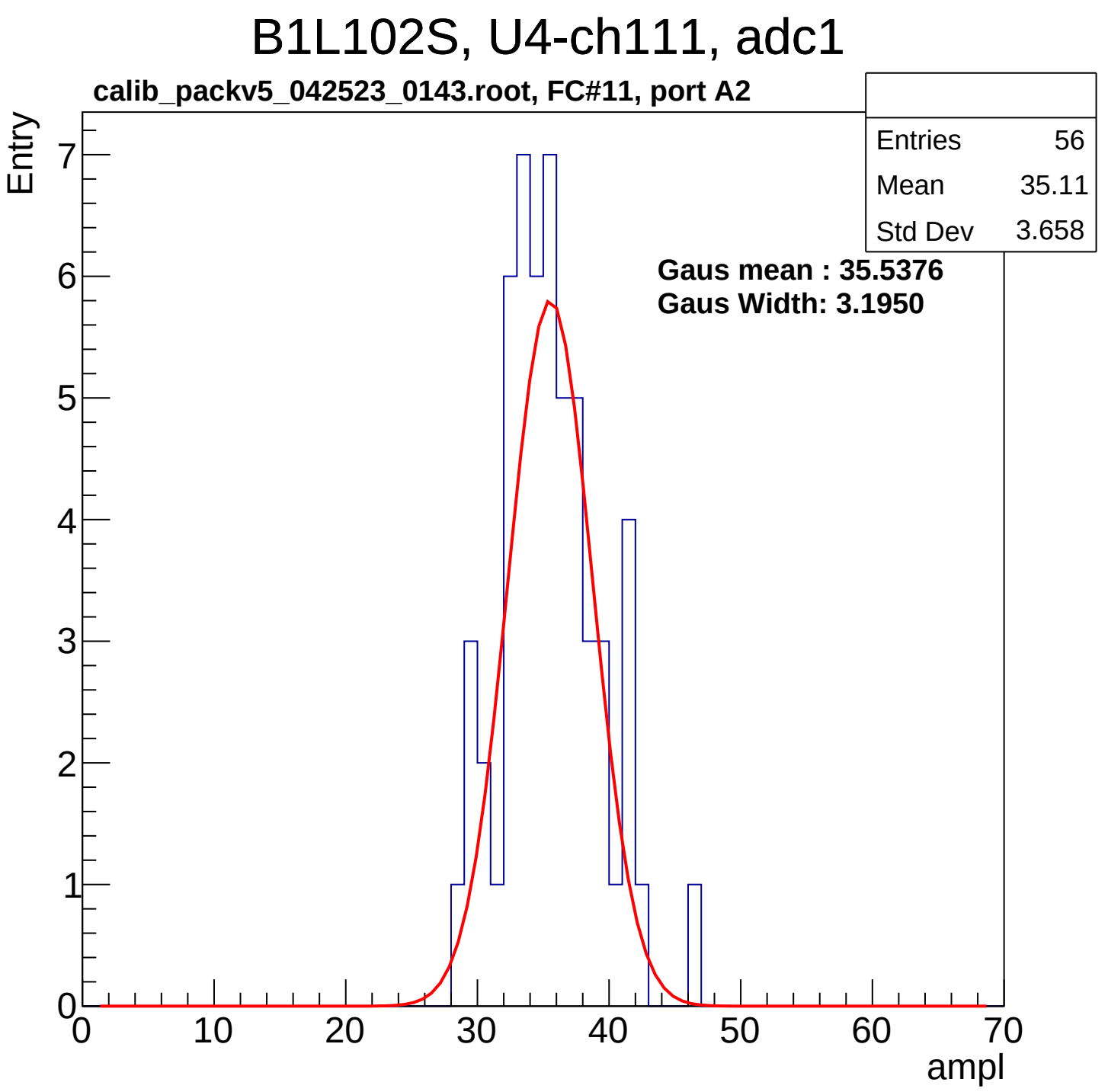
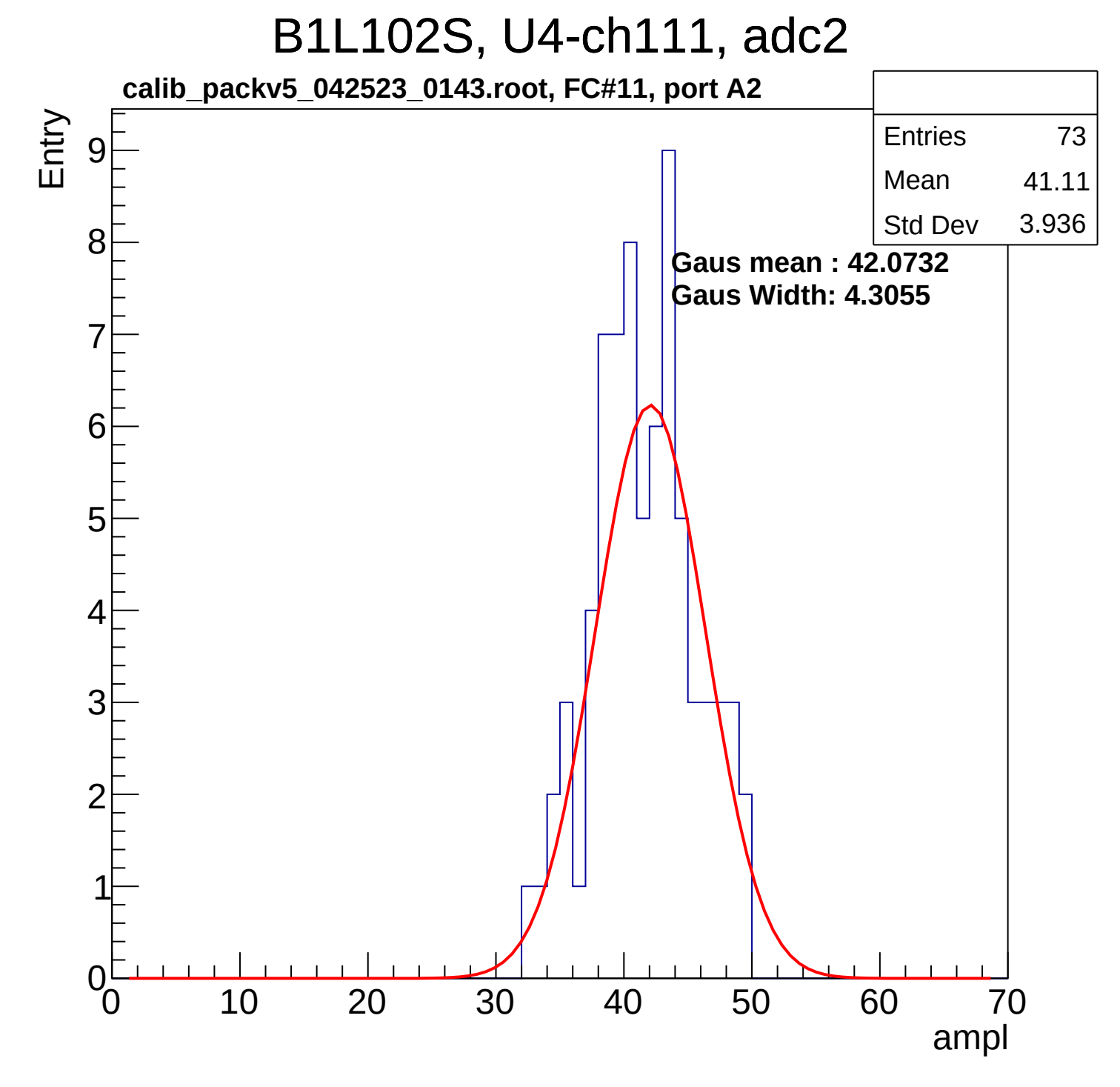
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch111, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 35.11
Std Dev 3.658
Gaus mean : 35.5376
Gaus Width: 3.1950
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch111, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 73
Mean 41.11
Std Dev 3.936
Gaus mean : 42.0732
Gaus Width: 4.3055
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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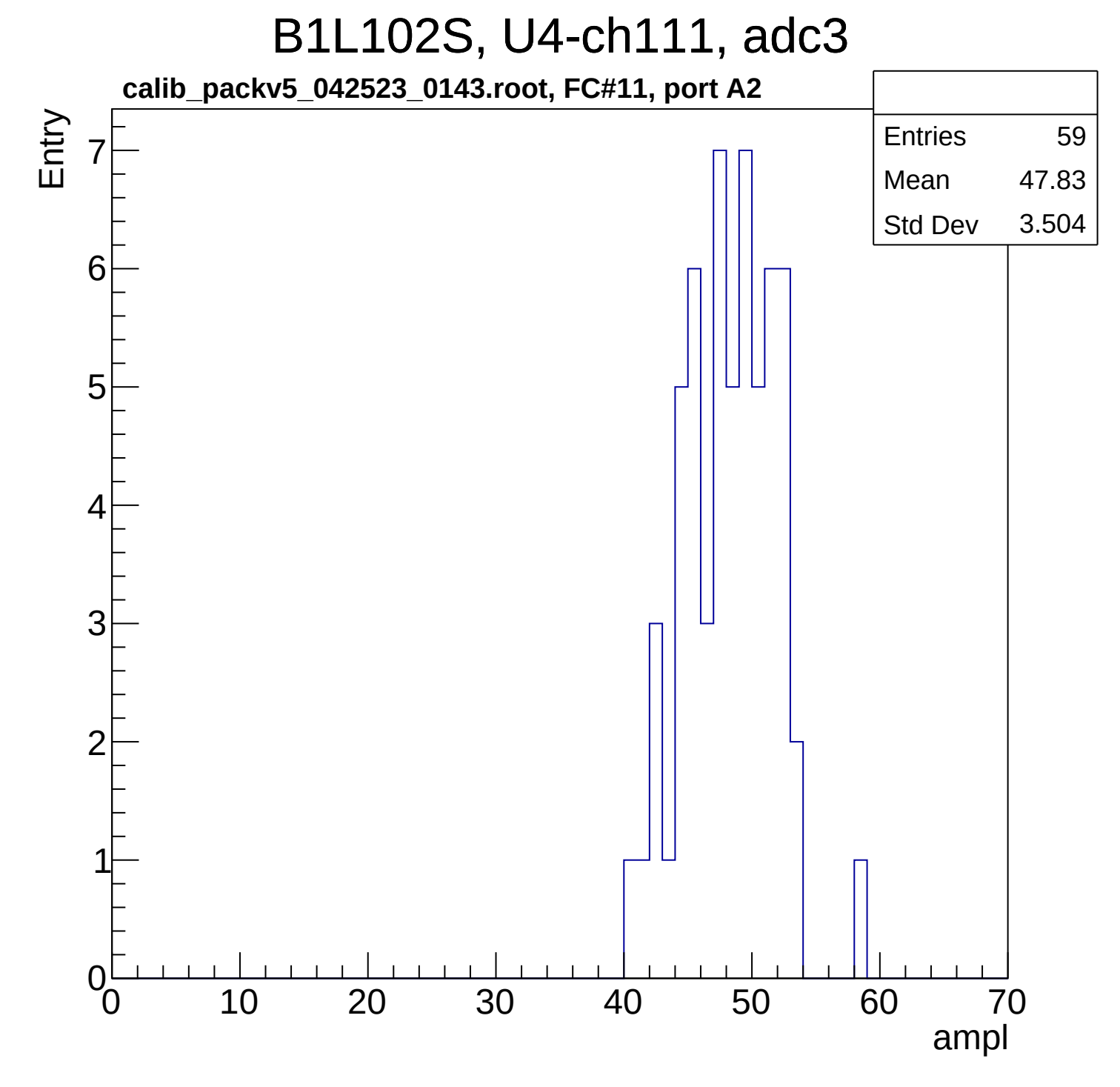
B1L102S, U4-ch111, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 47.83
Std Dev 3.504
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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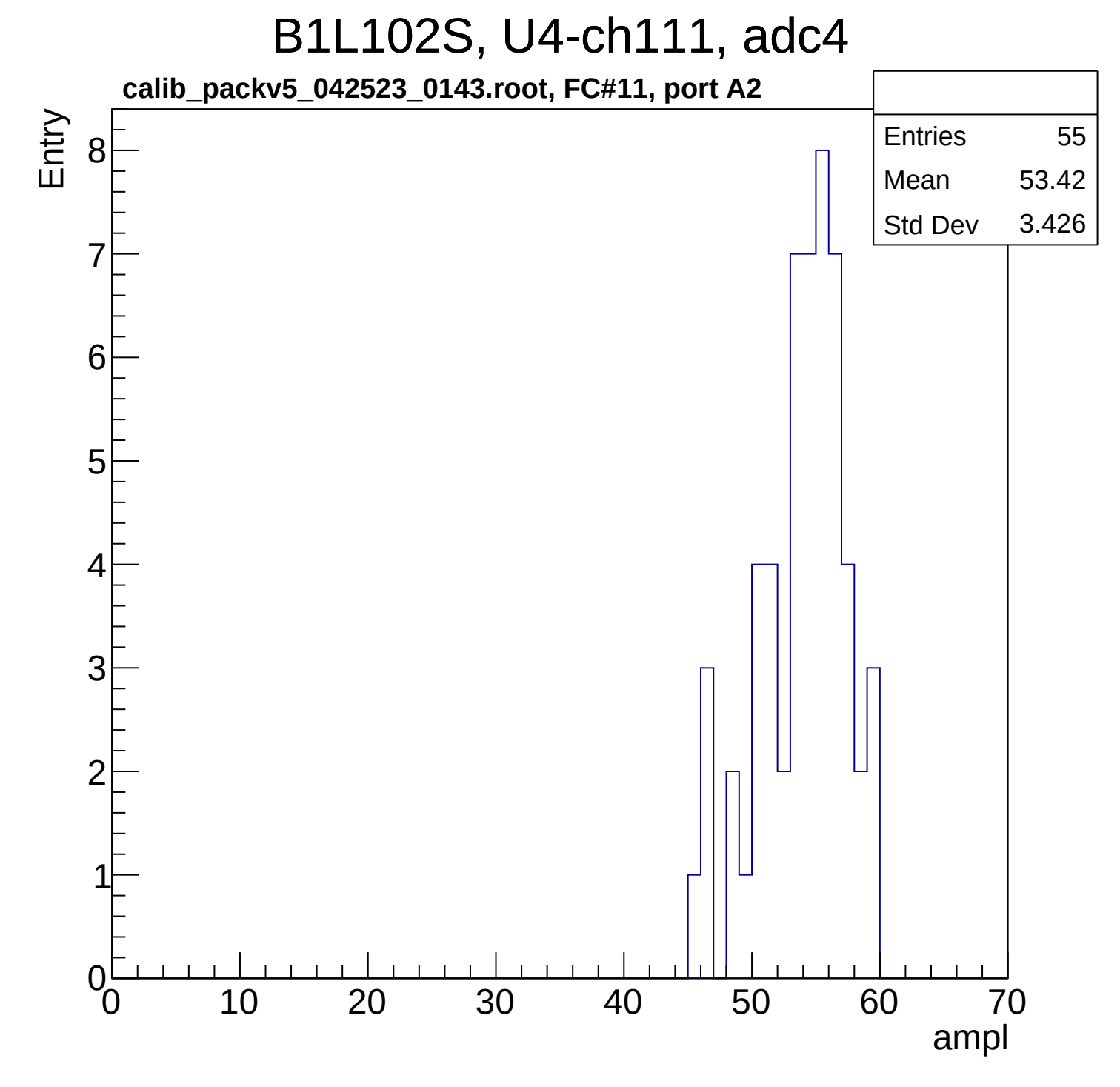
B1L102S, U4-ch111, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 53.42
Std Dev 3.426
Entry
ampl
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1
2
3
4
5
6
7
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0
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40
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60
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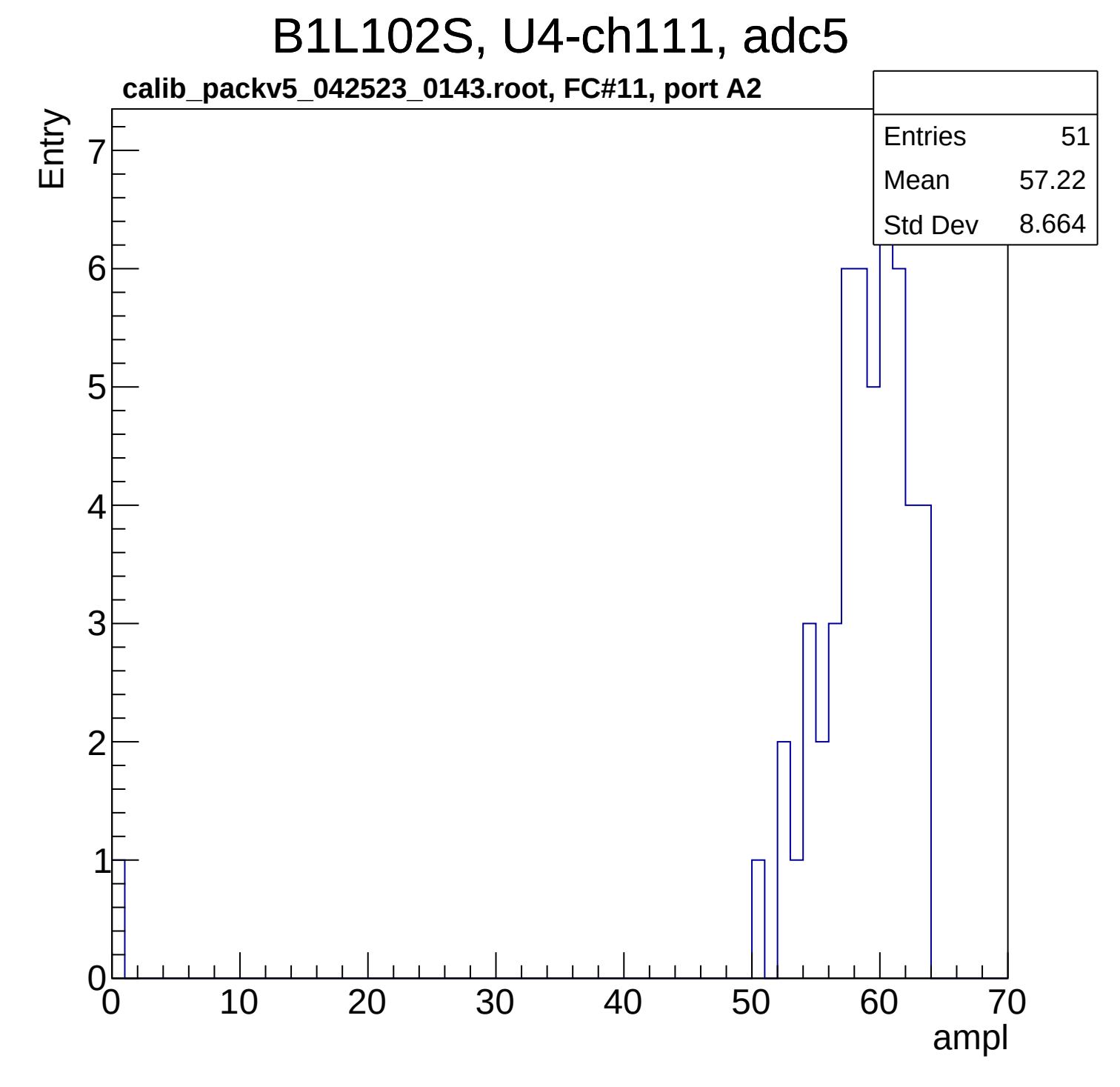
B1L102S, U4-ch111, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 57.22
Std Dev 8.664
Entry
ampl
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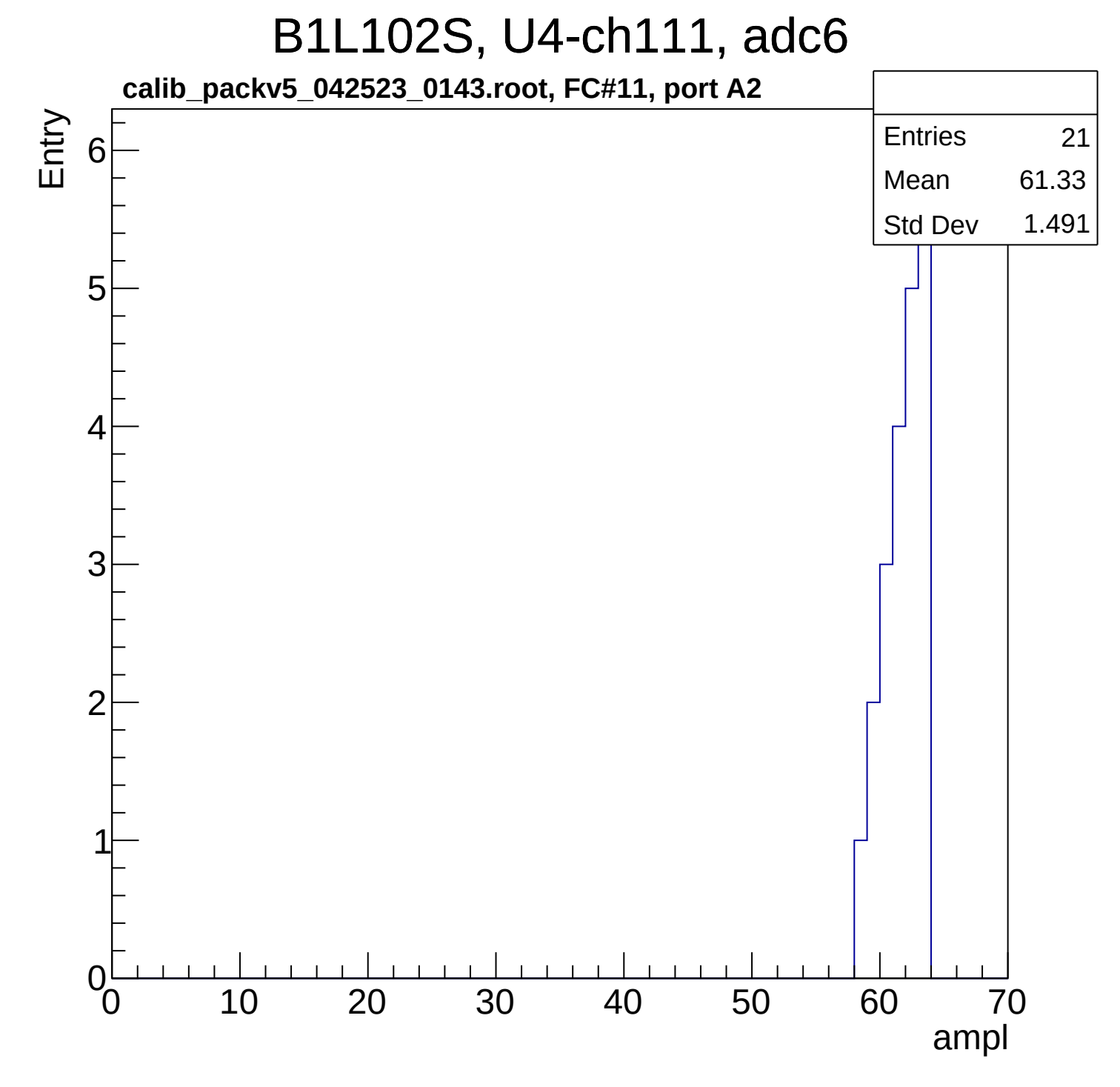
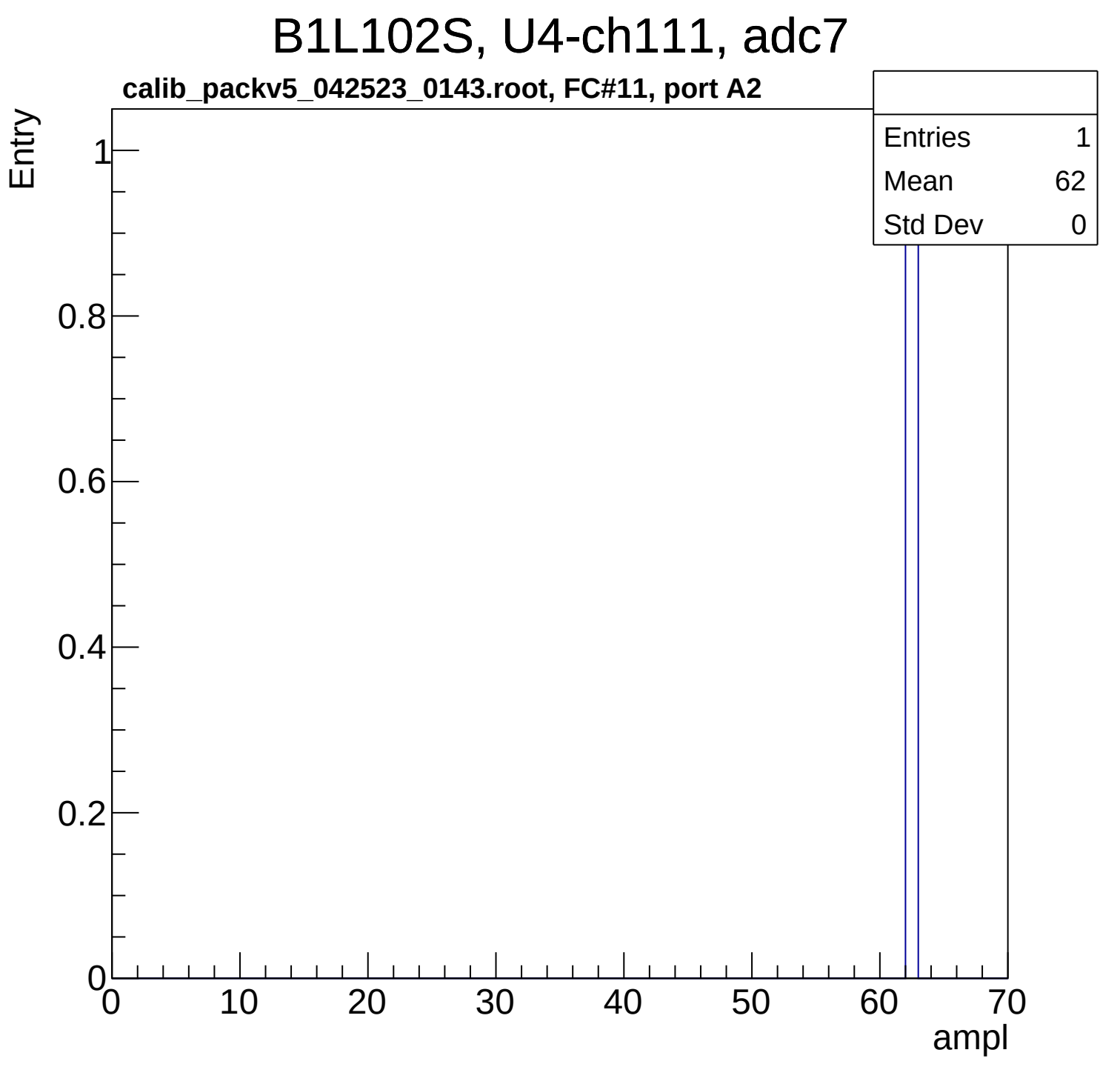
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch111, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 21
Mean 61.33
Std Dev 1.491
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch111, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 62
Std Dev 0
Entry
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0.6
0.4
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0
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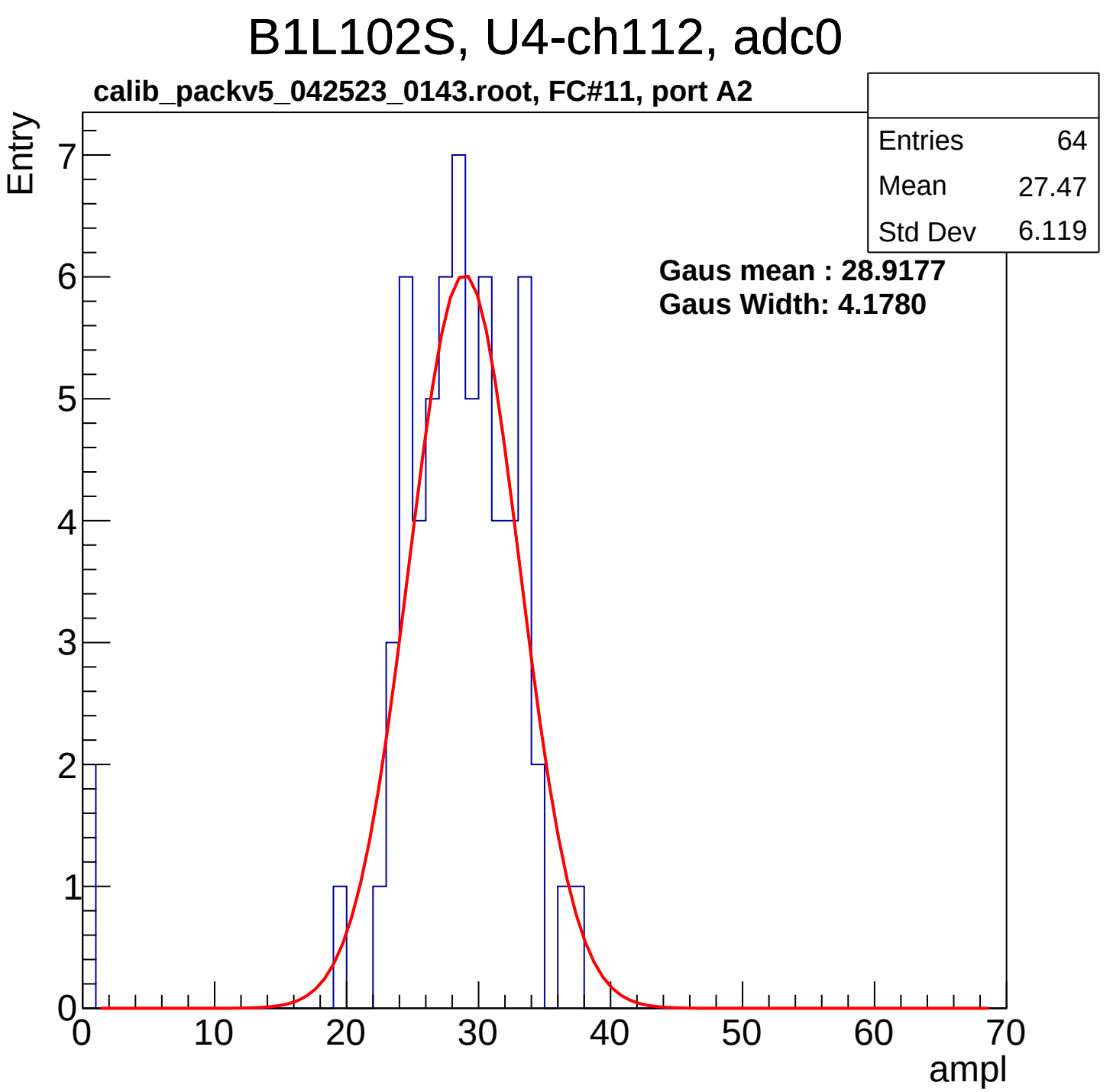
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch112, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 27.47
Std Dev 6.119
Gaus mean : 28.9177
Gaus Width: 4.1780
Entry
ampl
0
1
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3
4
5
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7
0
10
20
30
40
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60
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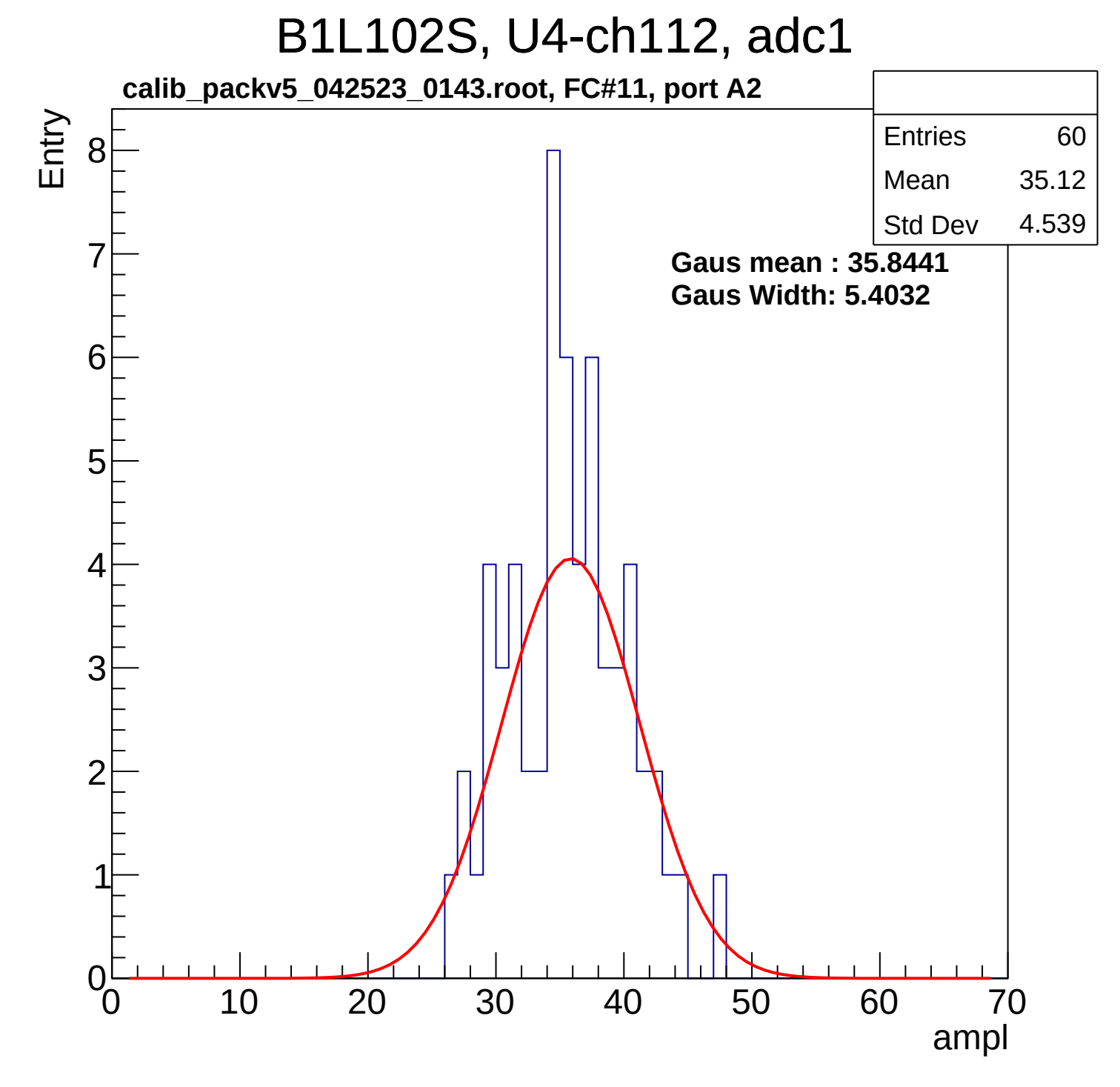
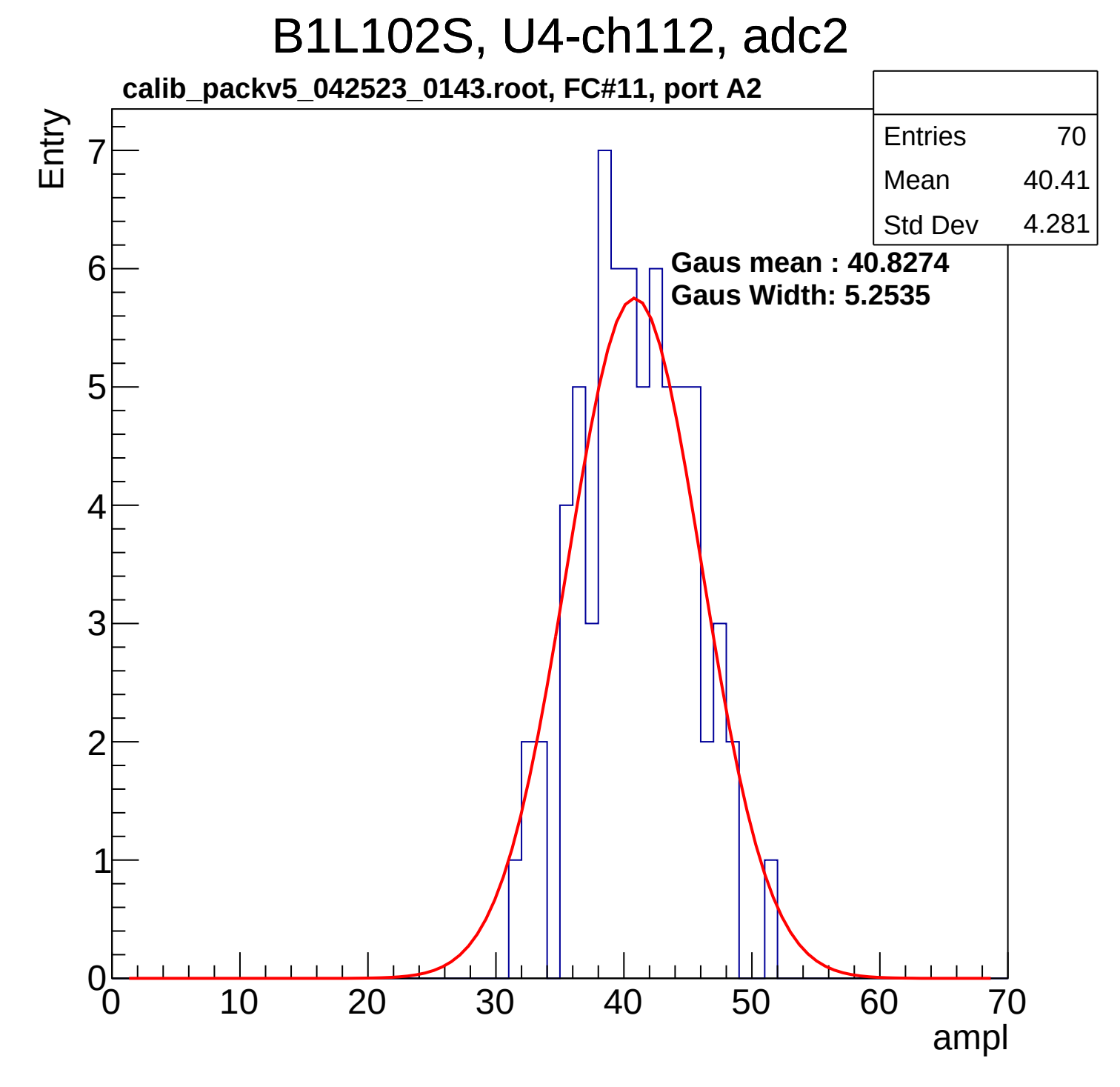

B1L102S, U4-ch112, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 35.12
Std Dev 4.539
Gaus mean : 35.8441
Gaus Width: 5.4032
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch112, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 40.41
Std Dev 4.281
Gaus mean : 40.8274
Gaus Width: 5.2535
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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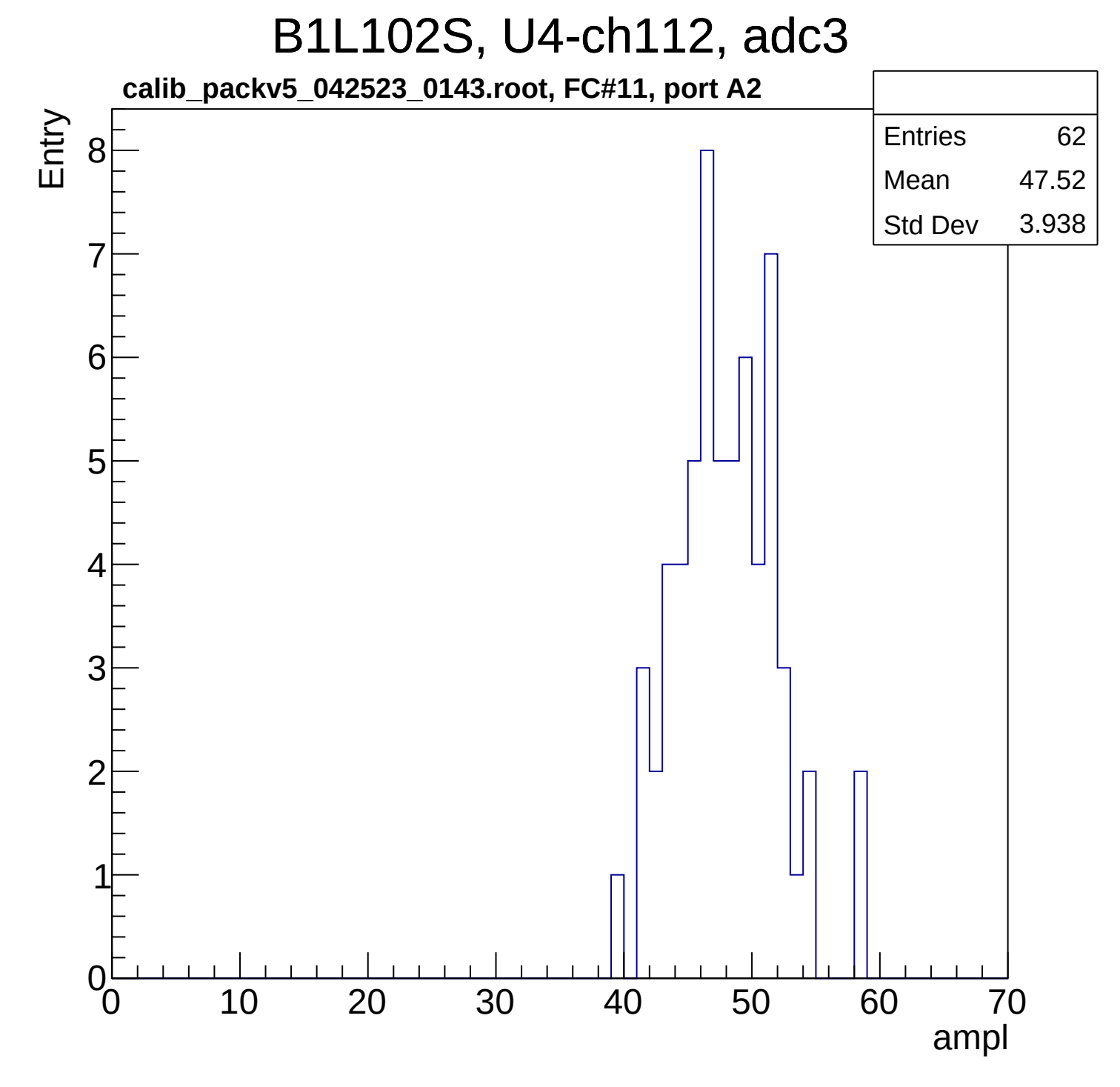
B1L102S, U4-ch112, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 47.52
Std Dev 3.938
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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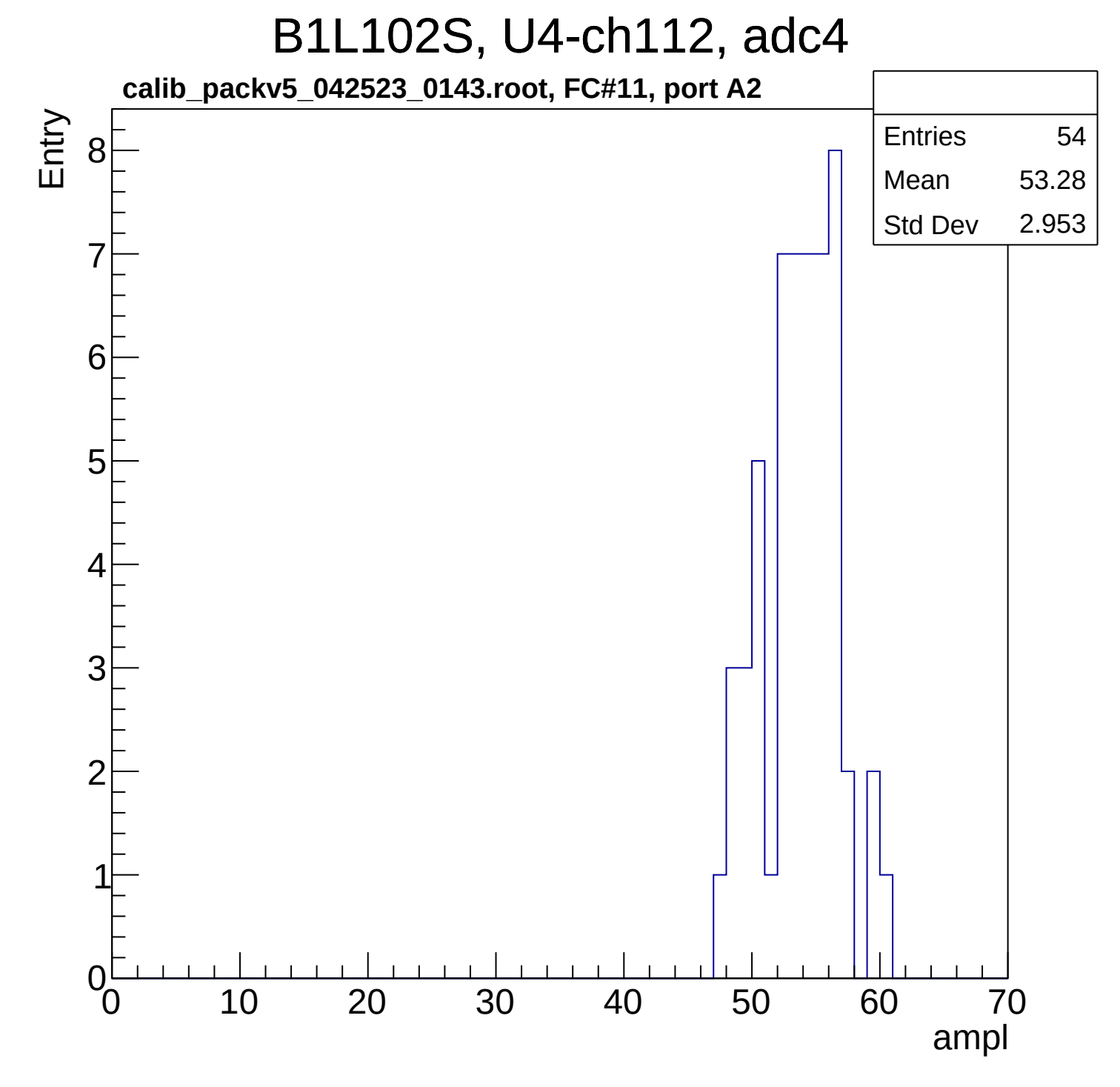
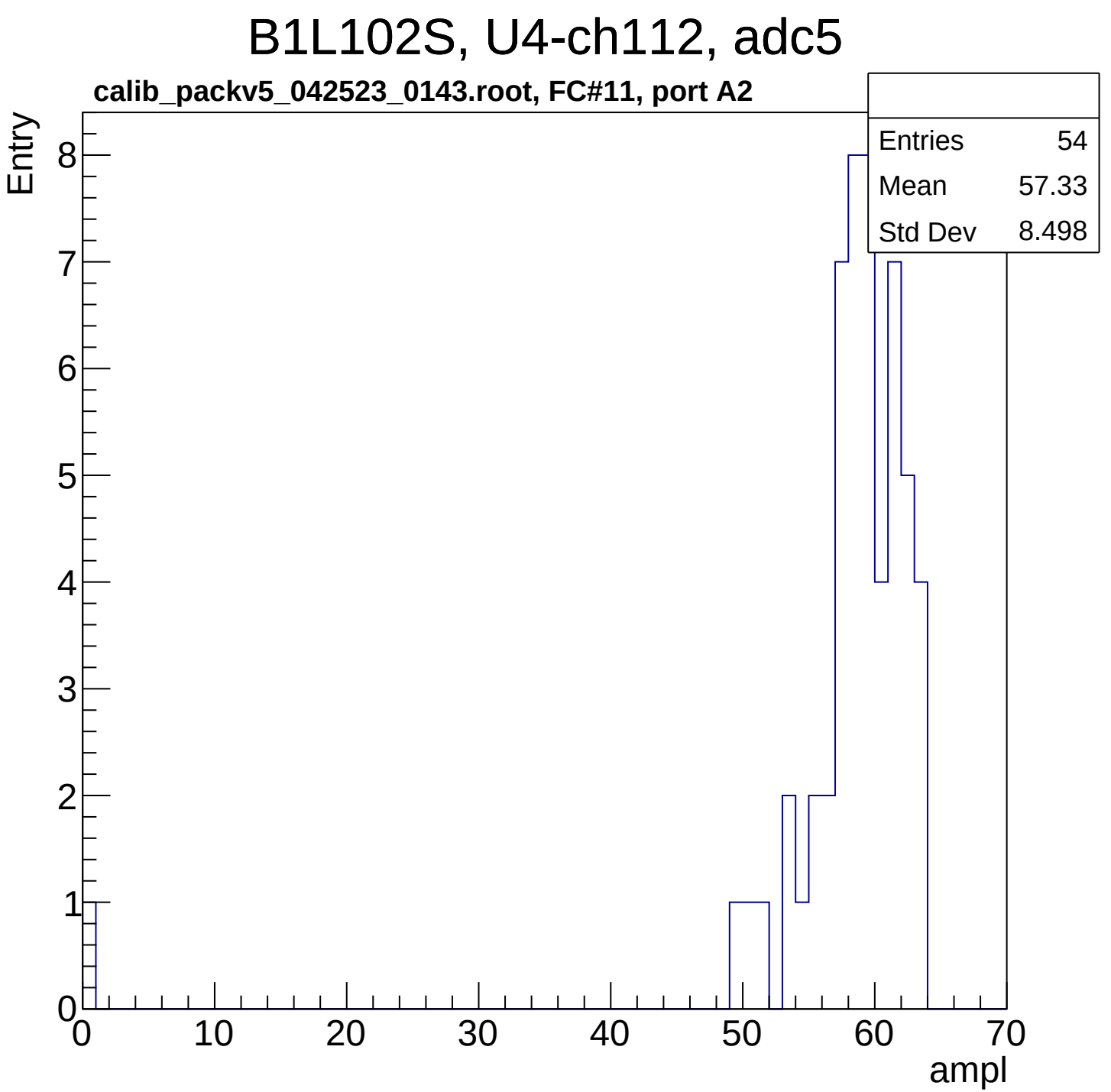

B1L102S, U4-ch112, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 53.28
Std Dev 2.953
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch112, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 57.33
Std Dev 8.498
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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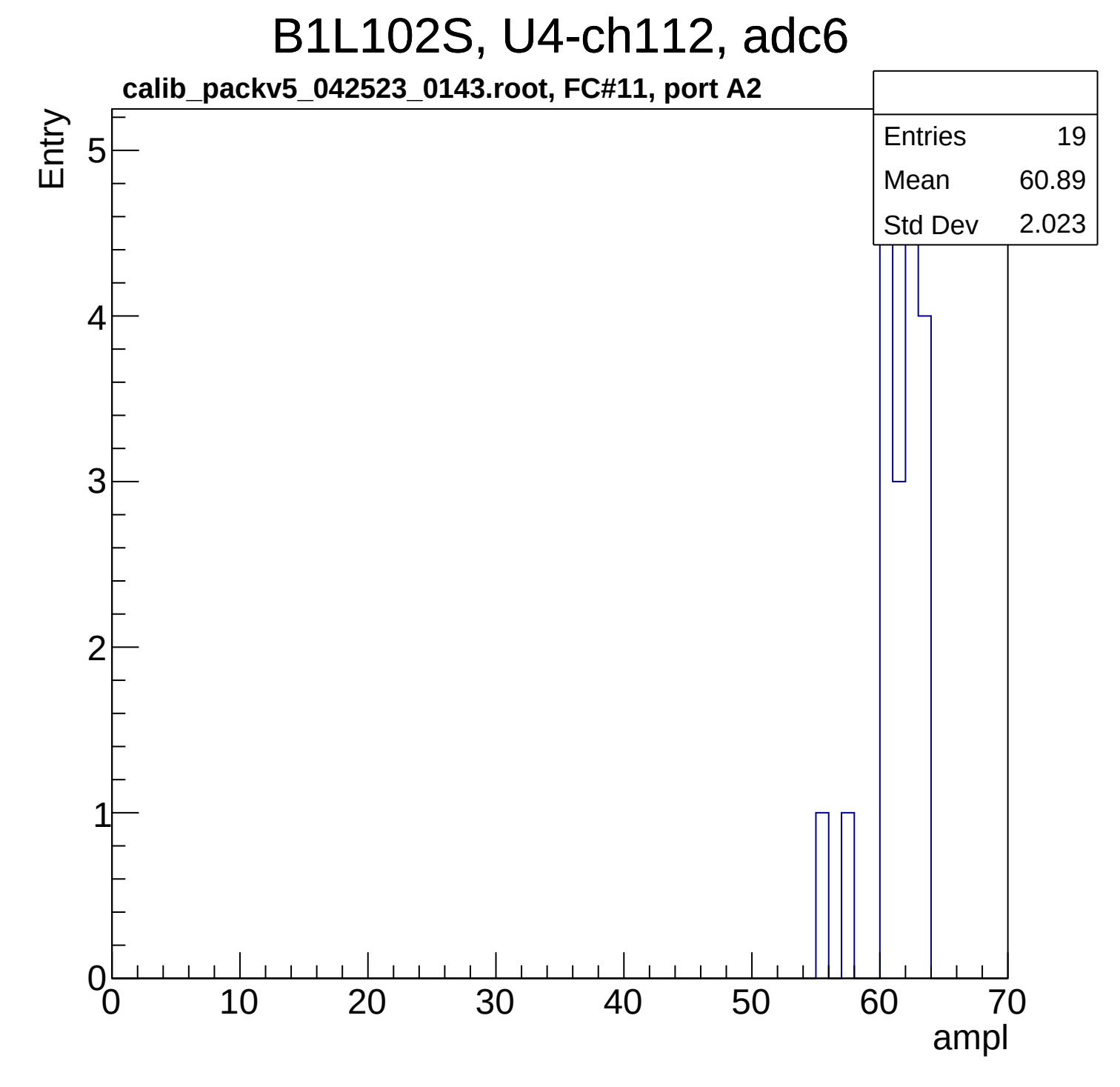
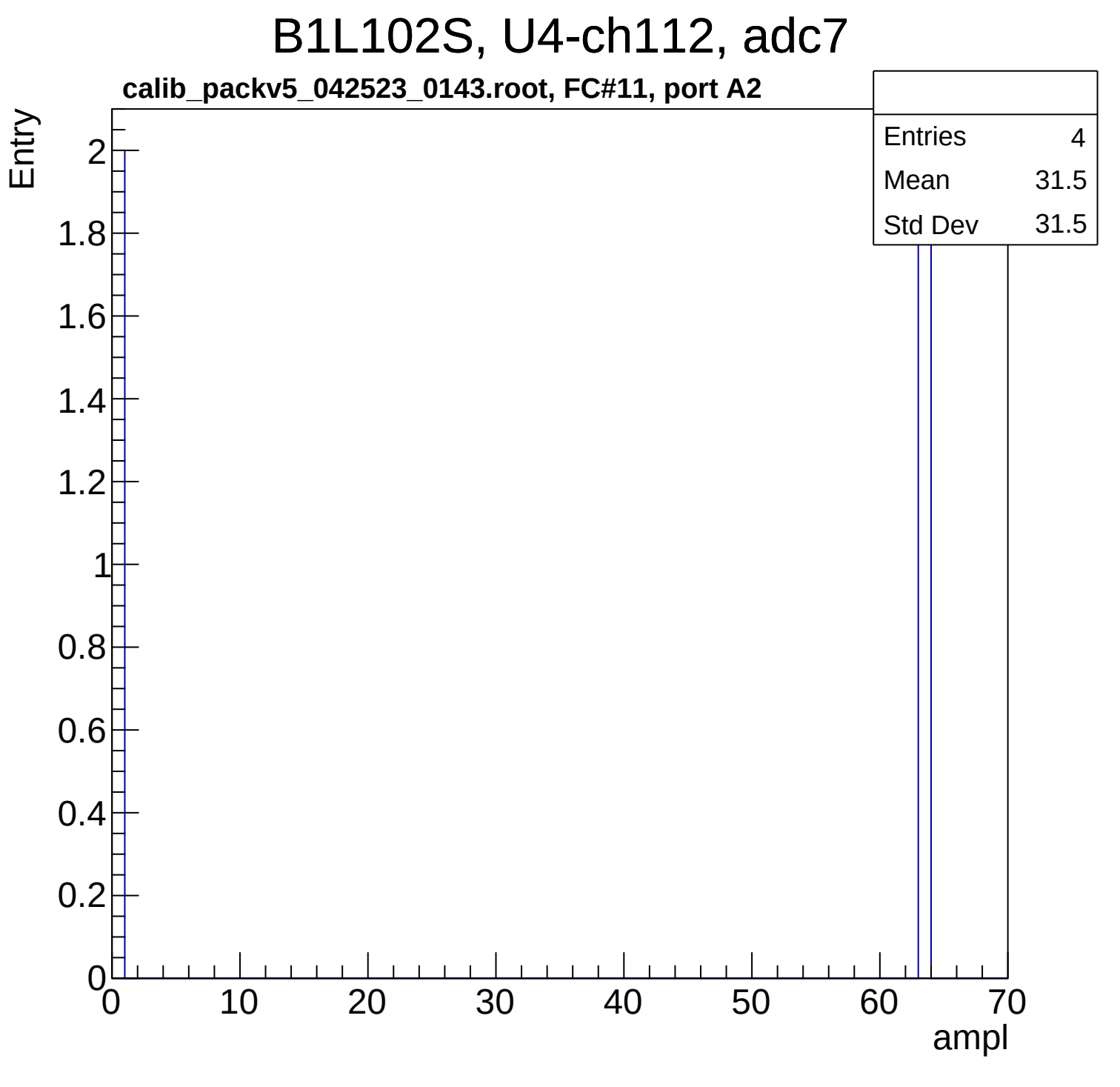
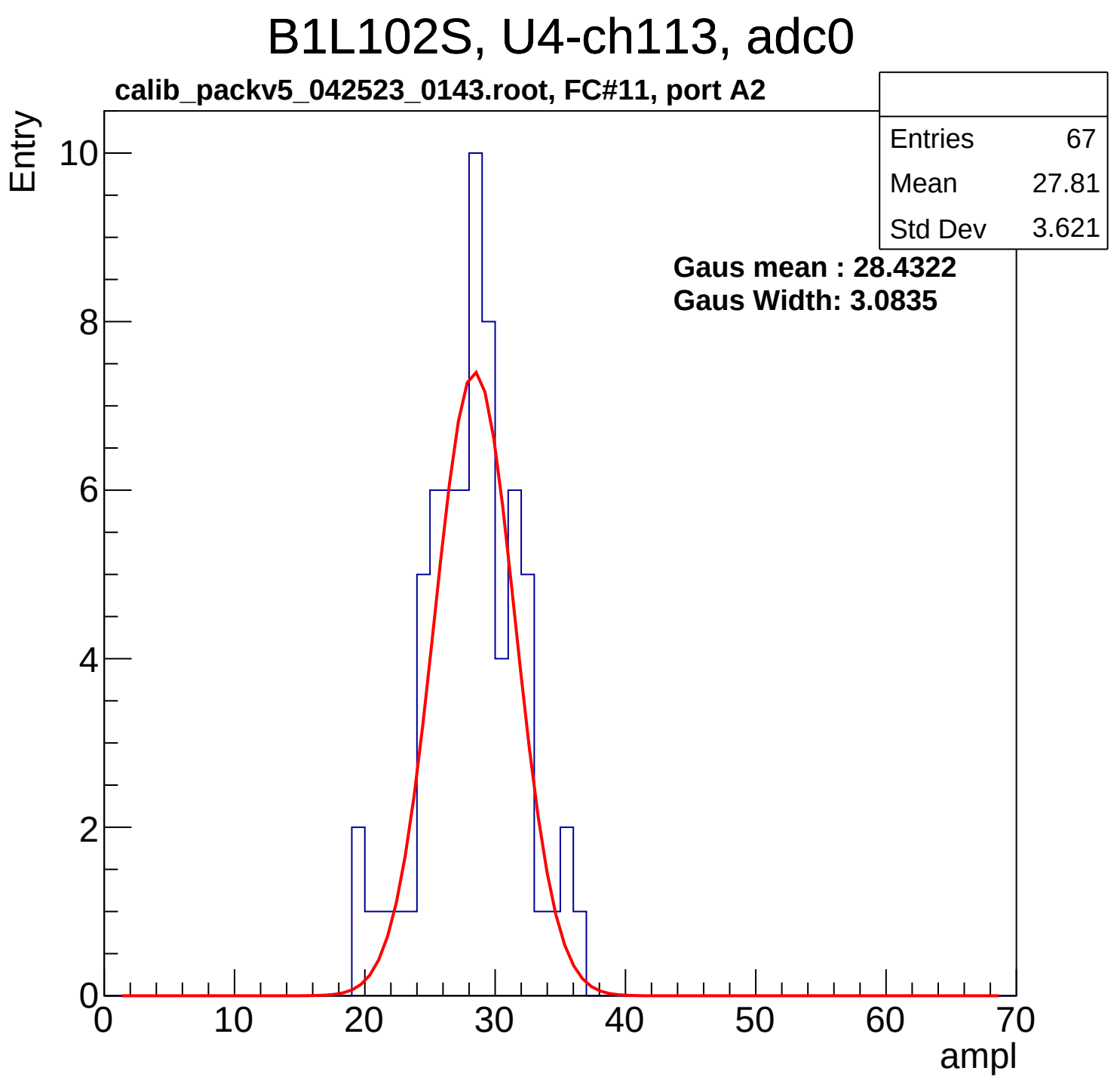
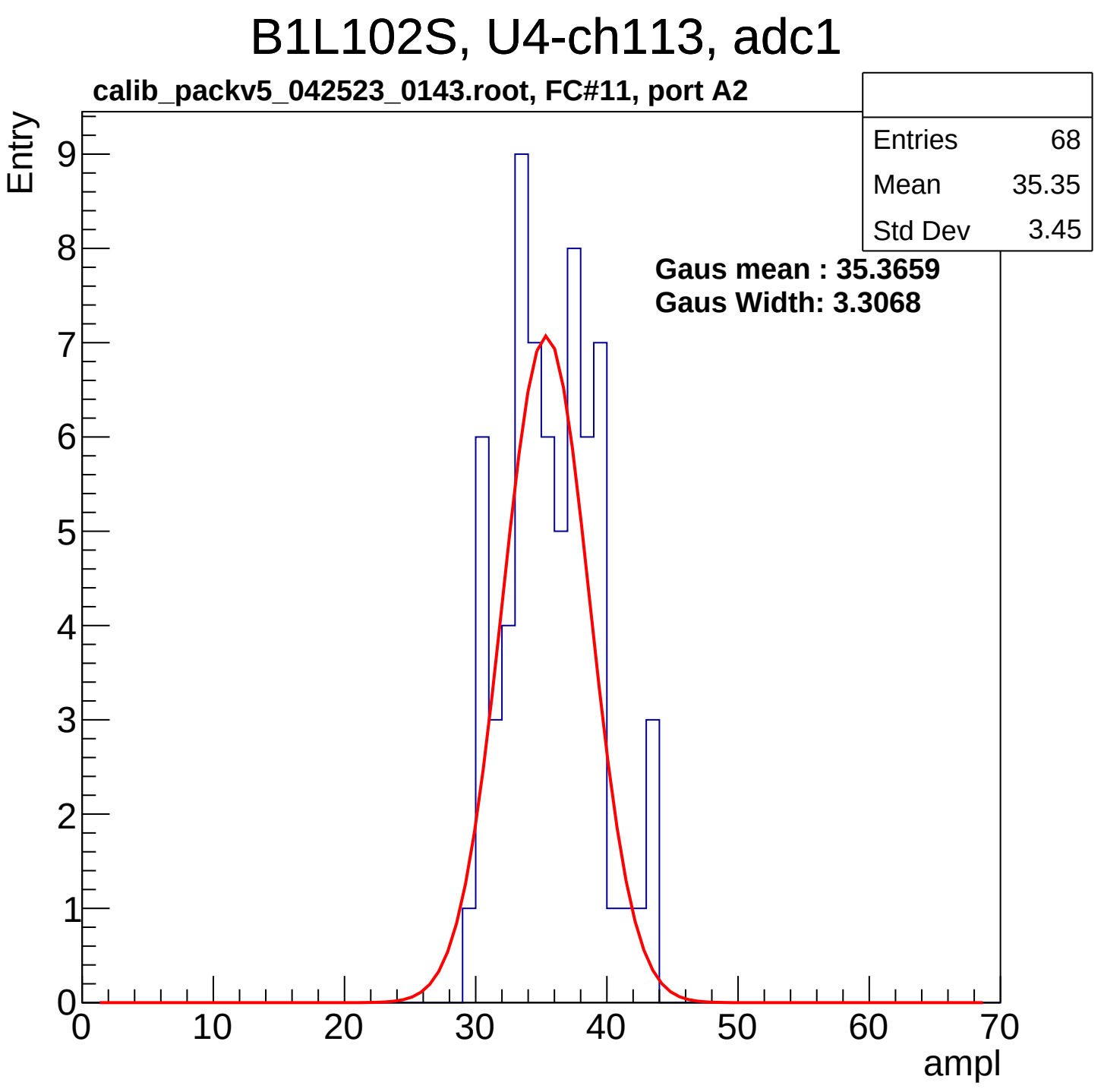
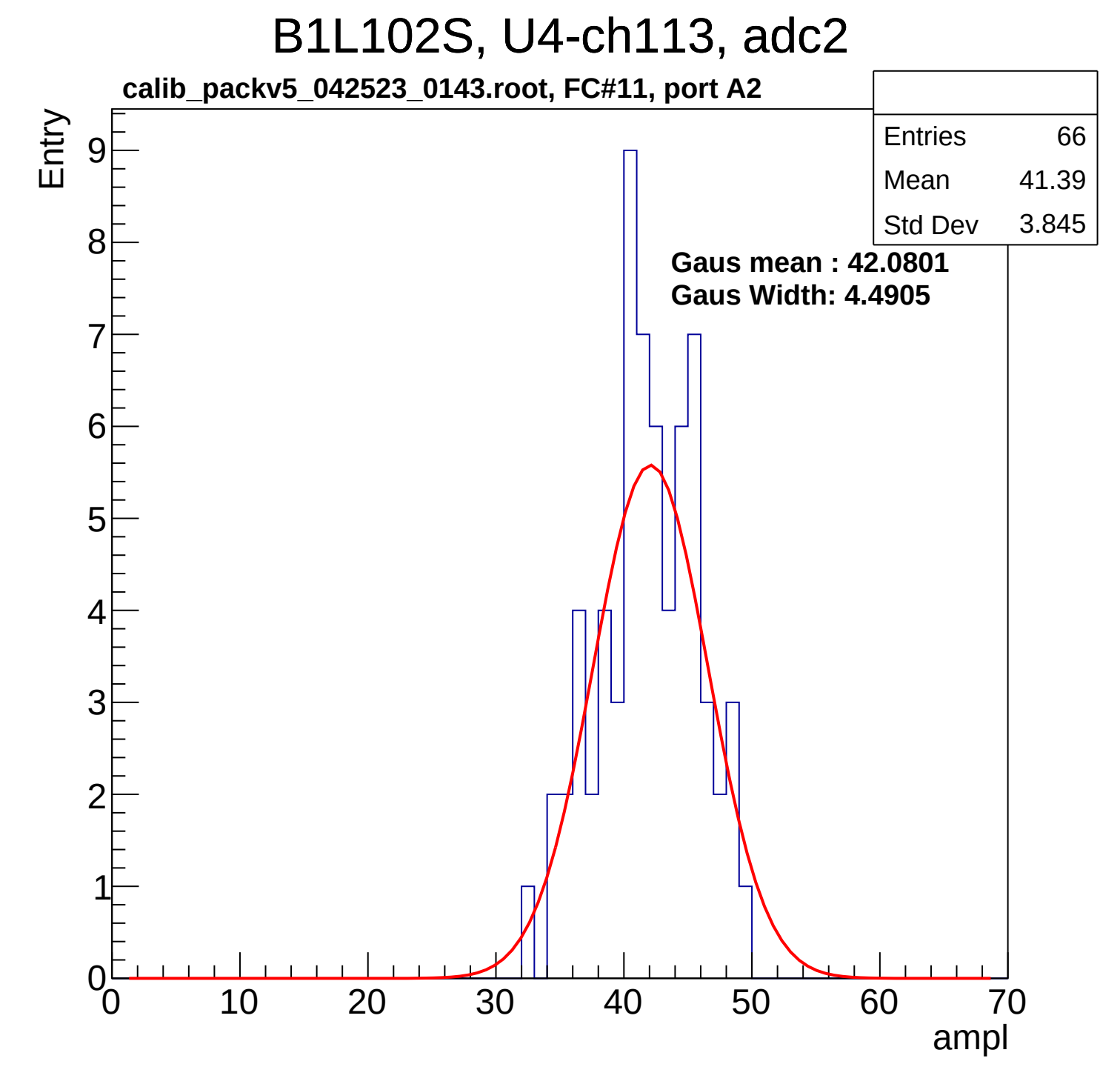
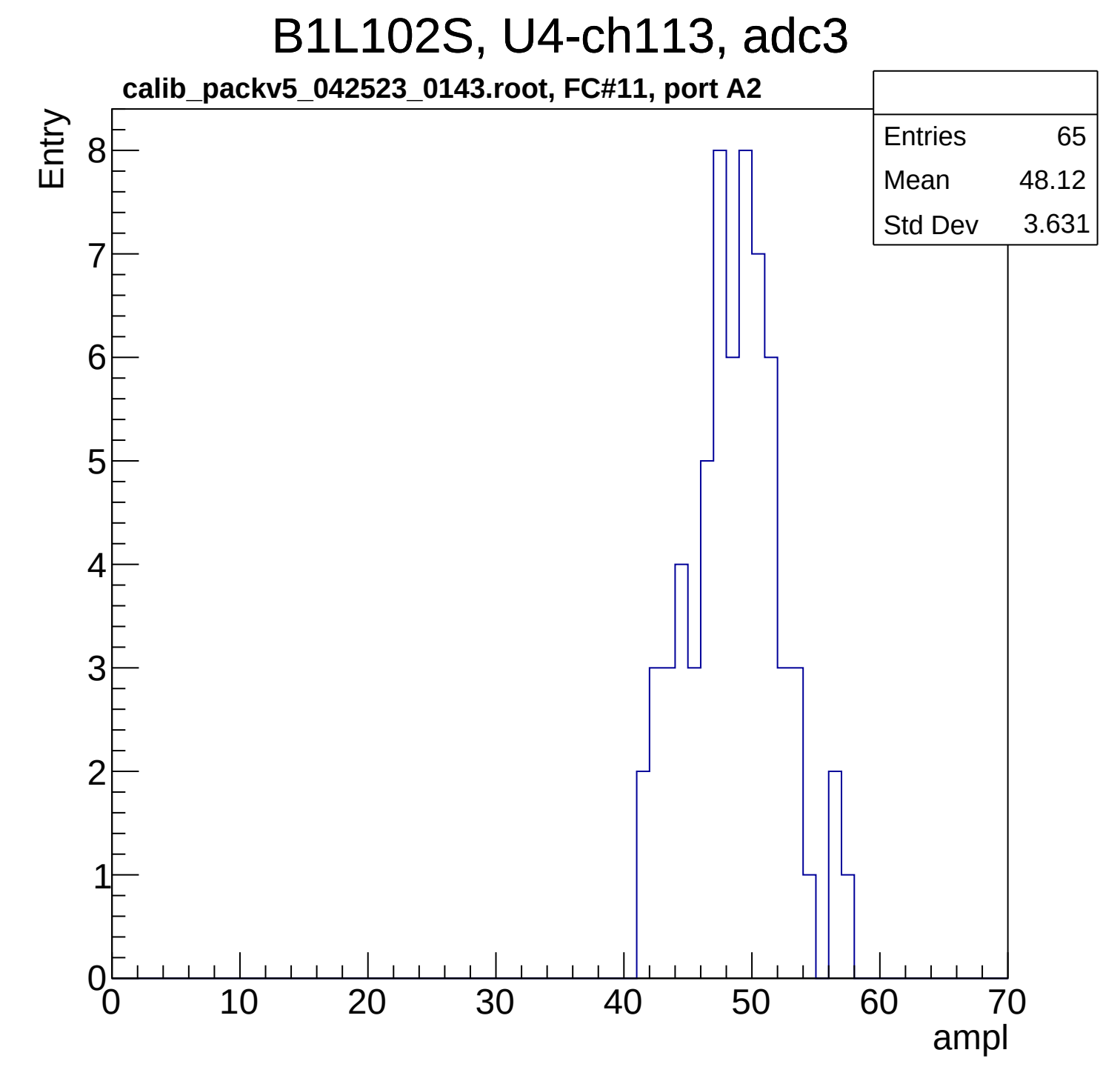

B1L102S, U4-ch112, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 19
Mean 60.89
Std Dev 2.023
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L102S, U4-ch112, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 4
Mean 31.5
Std Dev 31.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L102S, U4-ch113, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 27.81
Std Dev 3.621
Gaus mean : 28.4322
Gaus Width: 3.0835
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch113, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 35.35
Std Dev 3.45
Gaus mean : 35.3659
Gaus Width: 3.3068
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch113, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 41.39
Std Dev 3.845
Gaus mean : 42.0801
Gaus Width: 4.4905
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch113, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 48.12
Std Dev 3.631
Entry
ampl
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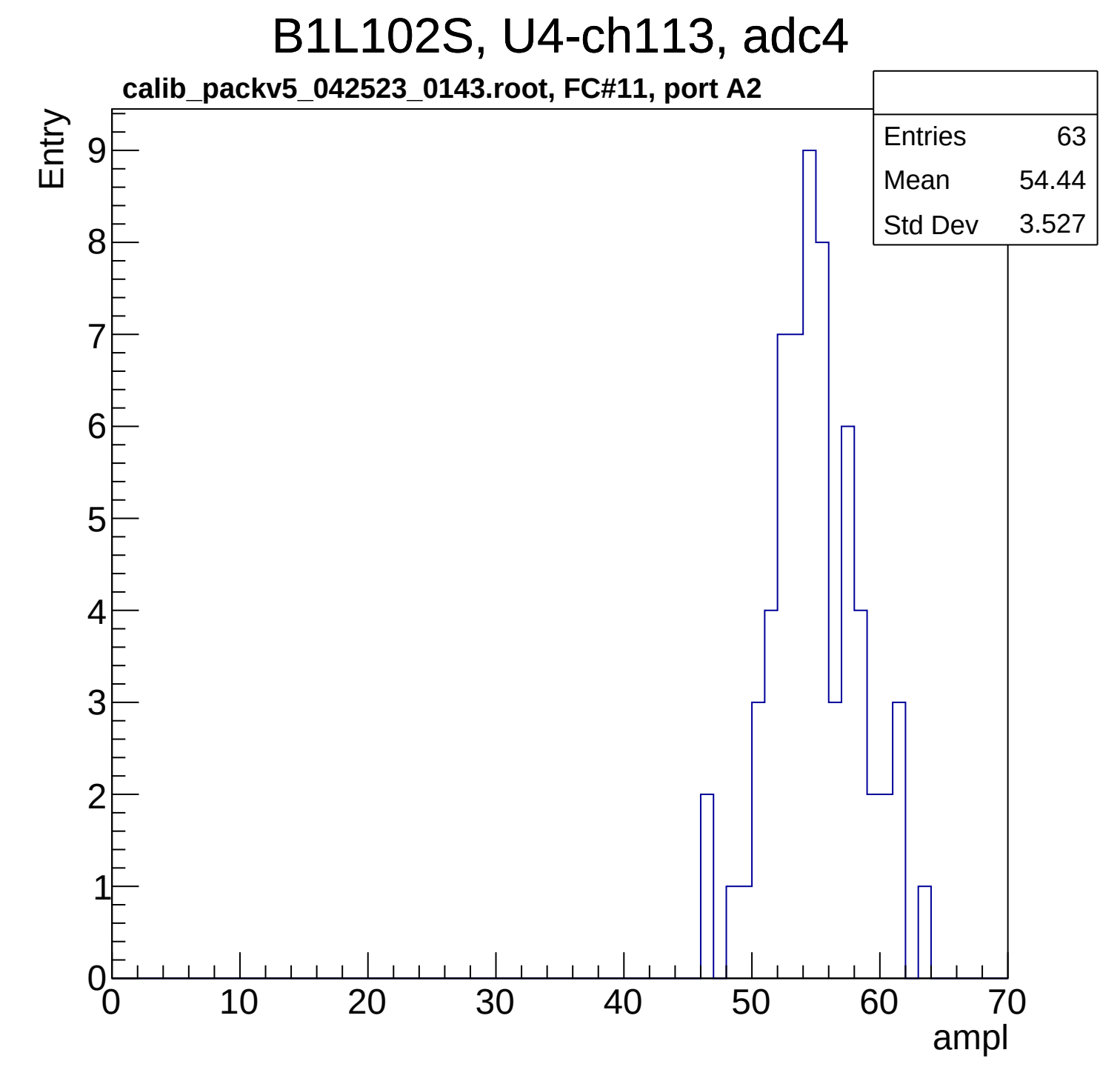
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch113, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 63
Mean 54.44
Std Dev 3.527
Entry
ampl
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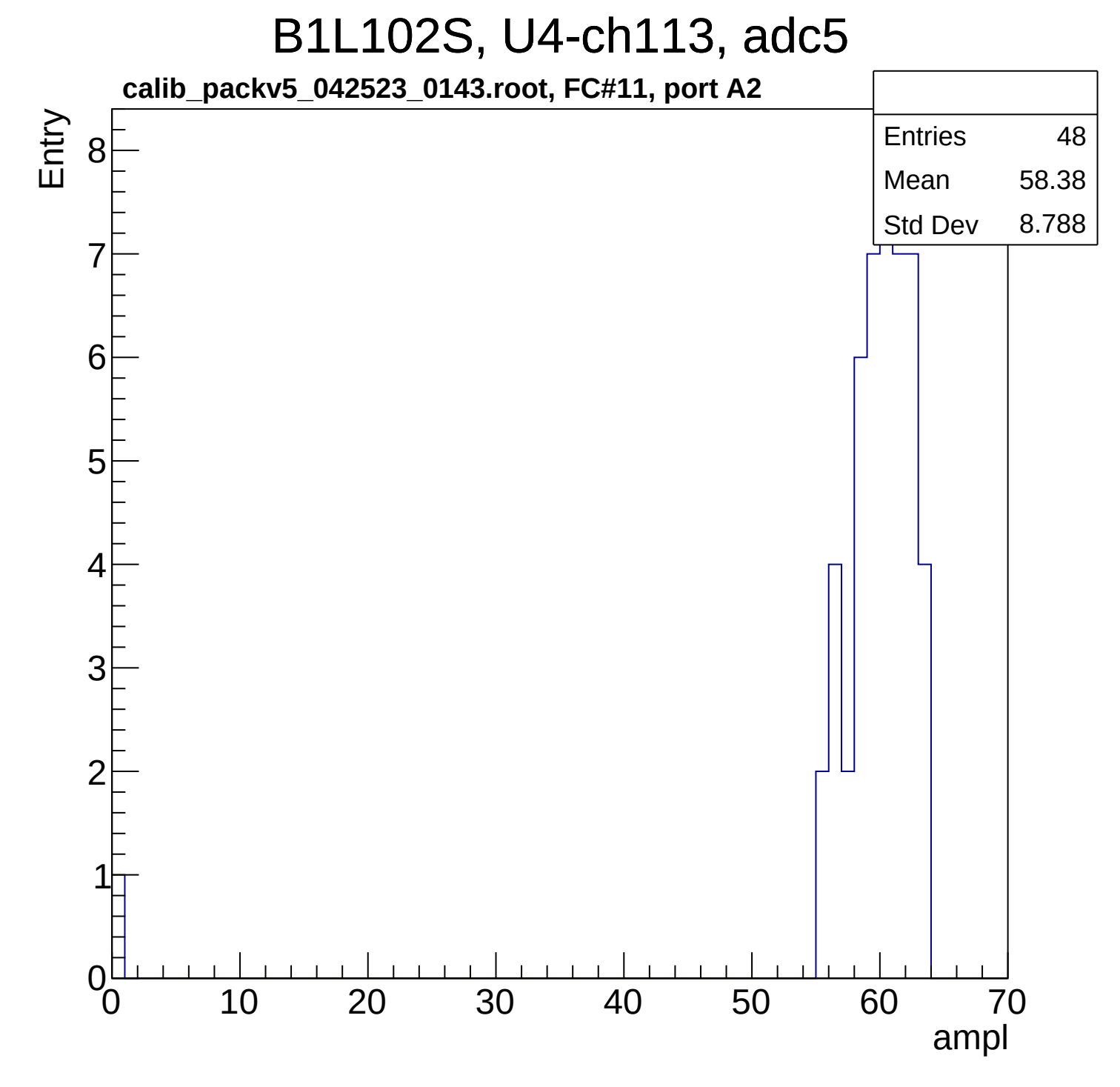
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch113, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 48
Mean 58.38
Std Dev 8.788
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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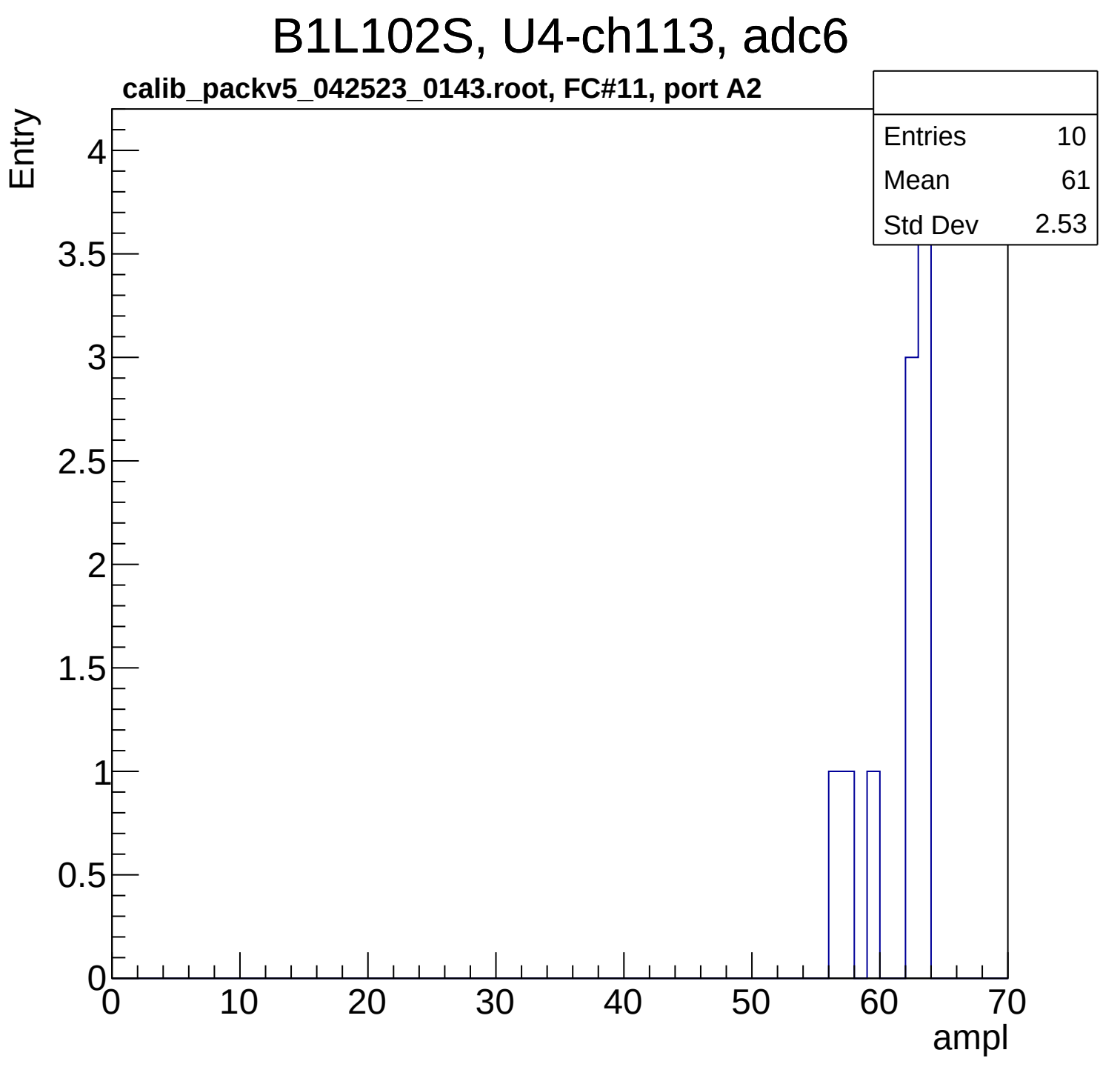
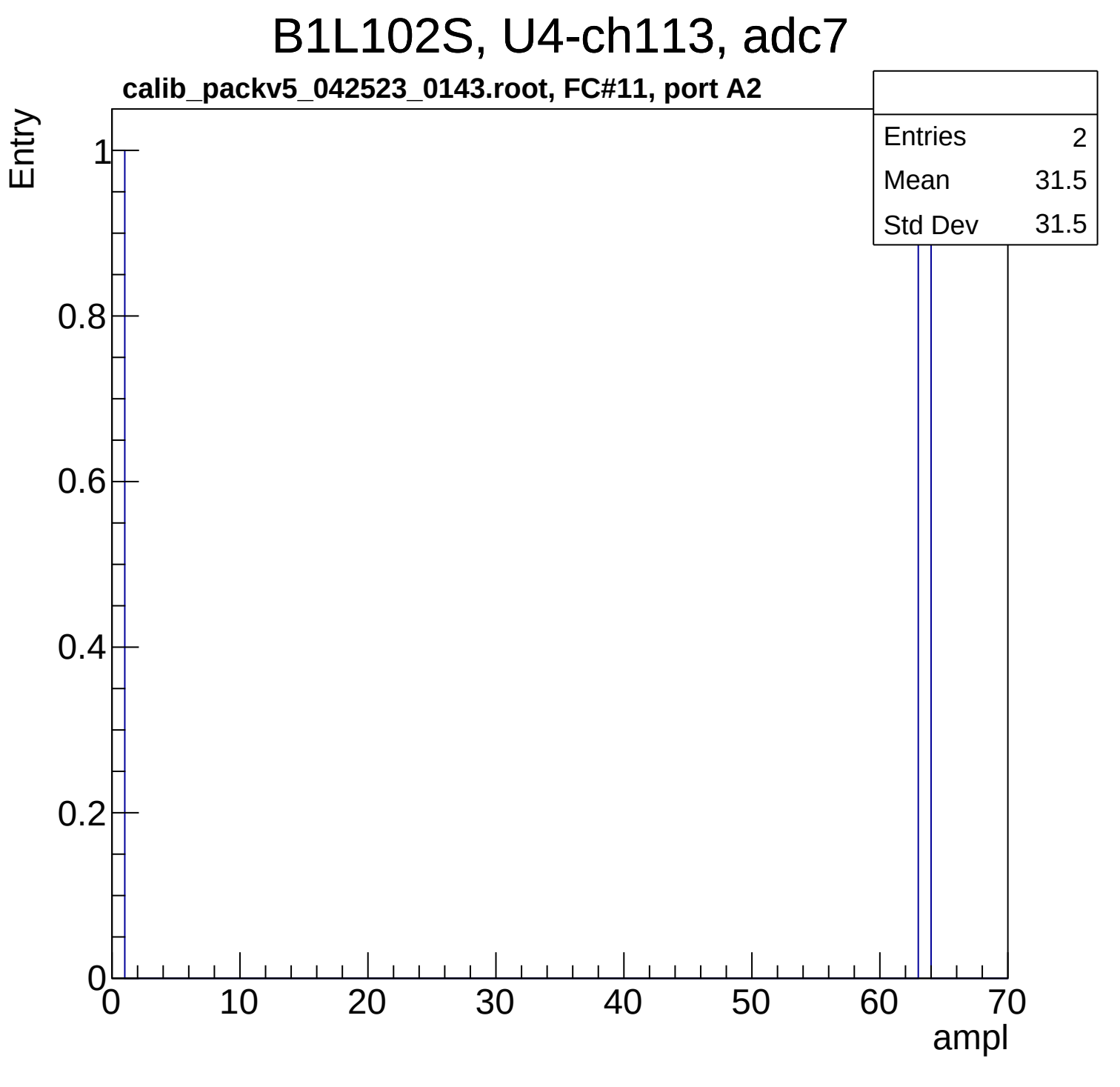
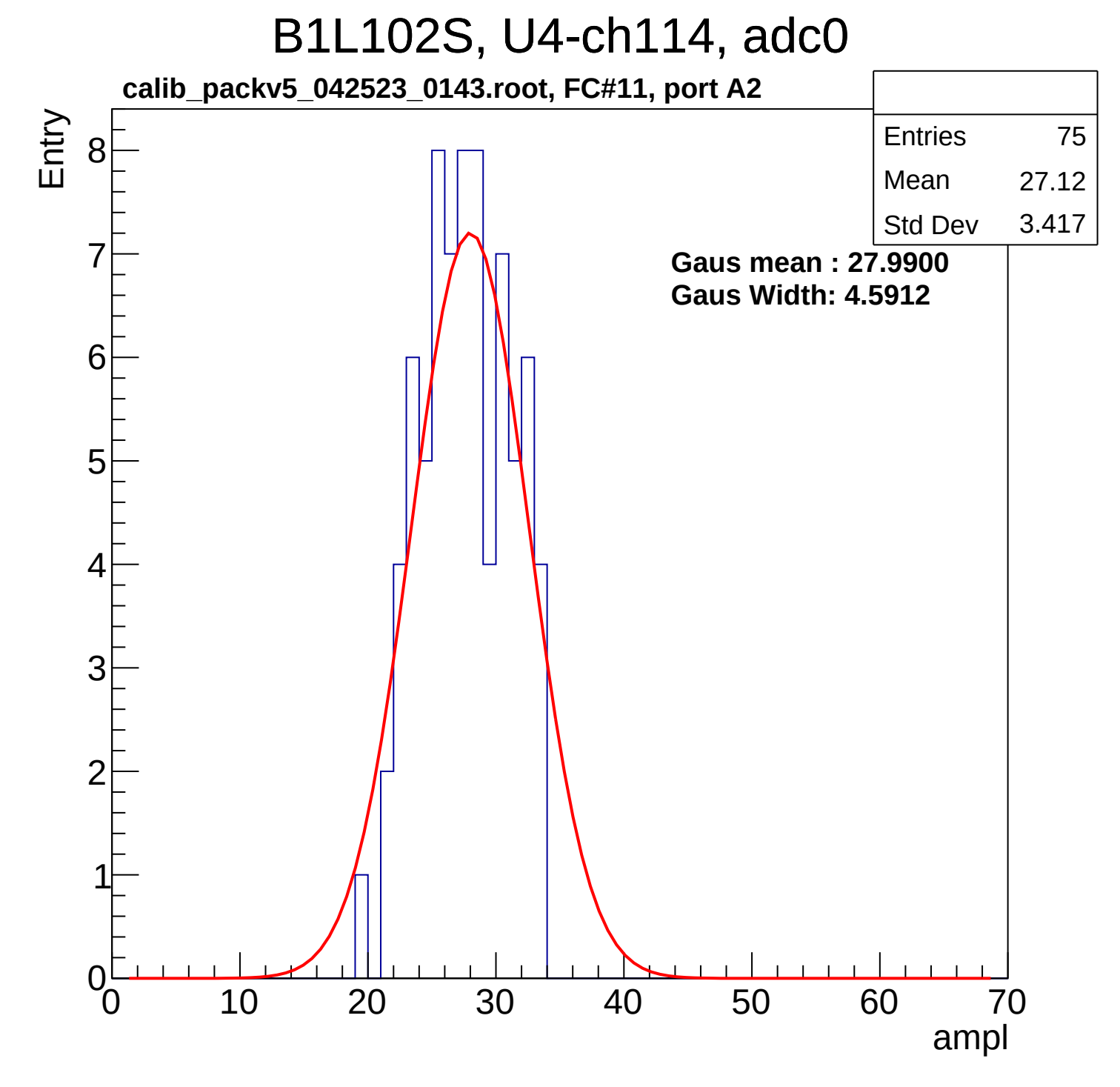

B1L102S, U4-ch113, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 10
Mean 61
Std Dev 2.53
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U4-ch113, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch114, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 27.12
Std Dev 3.417
Gaus mean : 27.9900
Gaus Width: 4.5912
Entry
ampl
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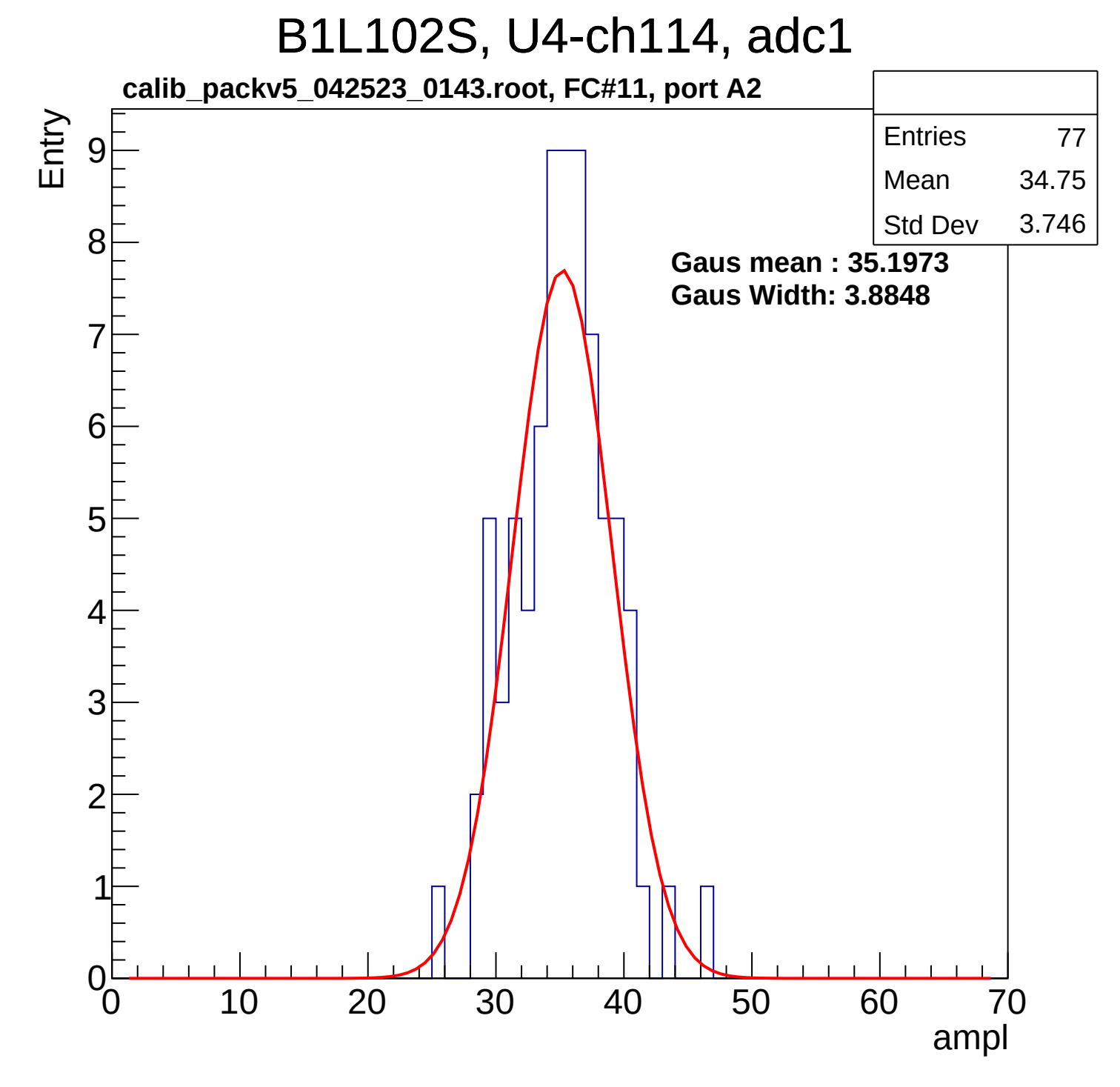
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch114, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 77
Mean 34.75
Std Dev 3.746
Gaus mean : 35.1973
Gaus Width: 3.8848
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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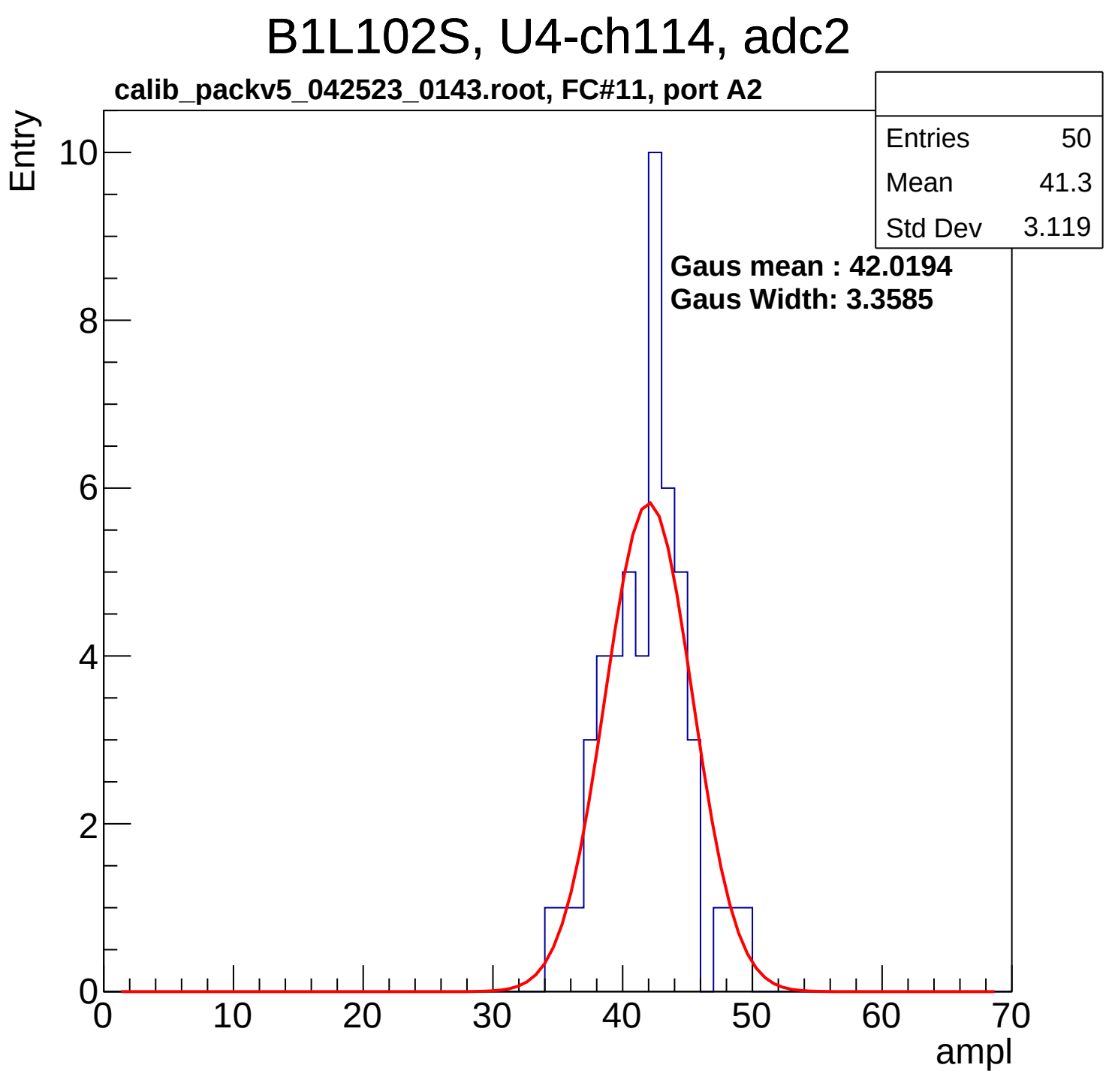
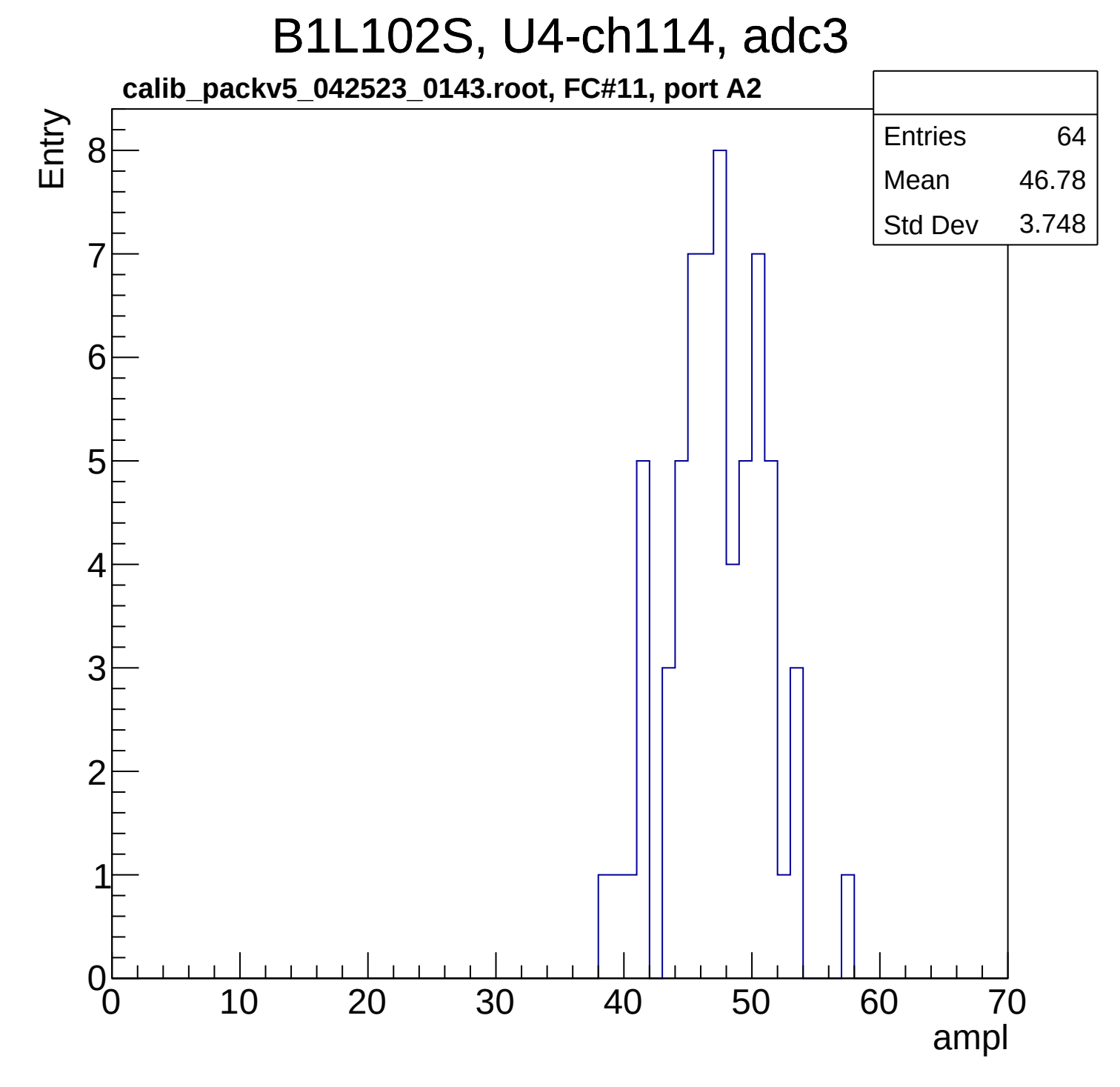

B1L102S, U4-ch114, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 50
Mean 41.3
Std Dev 3.119
Gaus mean : 42.0194
Gaus Width: 3.3585
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch114, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 46.78
Std Dev 3.748
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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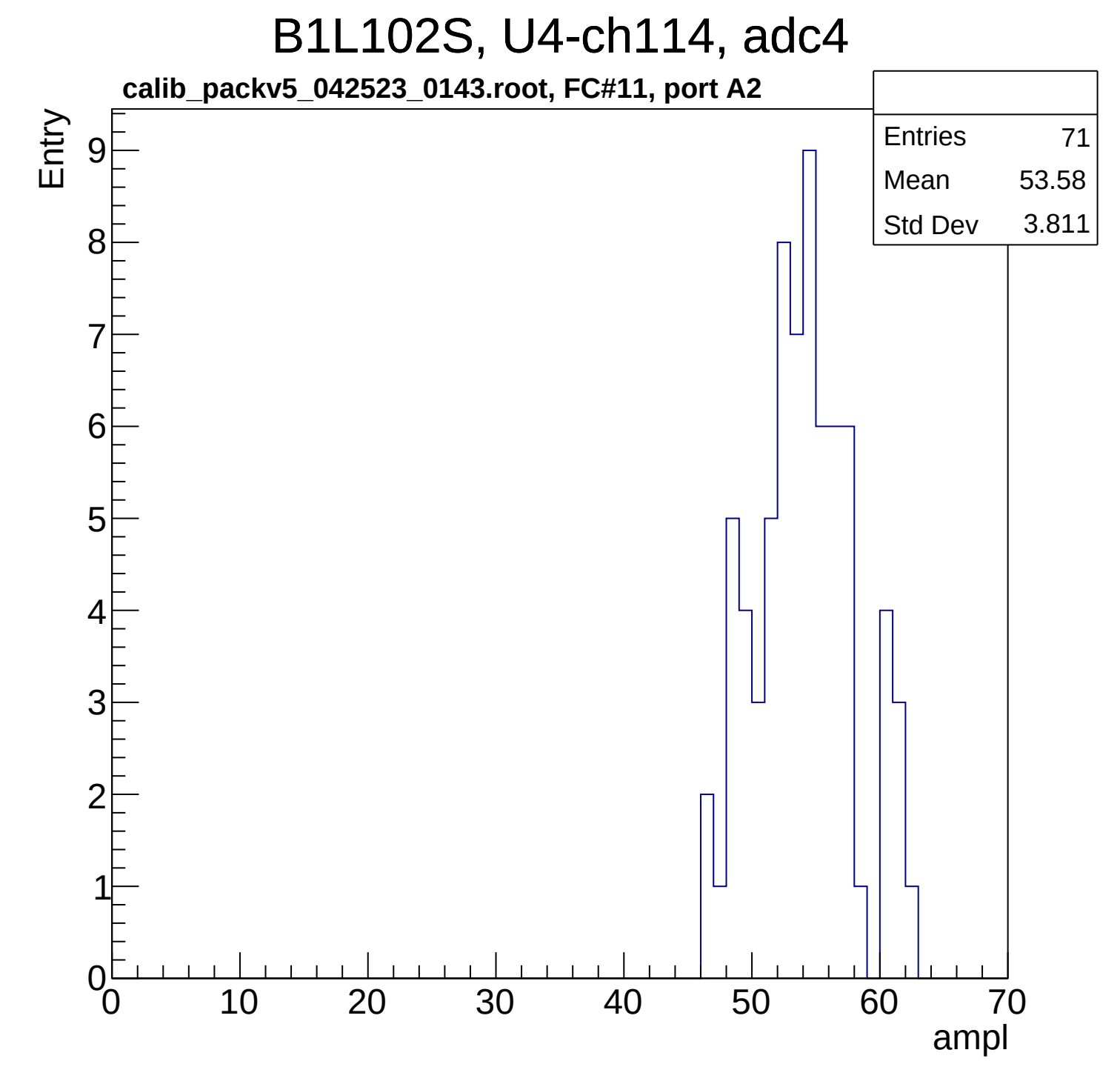
B1L102S, U4-ch114, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 53.58
Std Dev 3.811
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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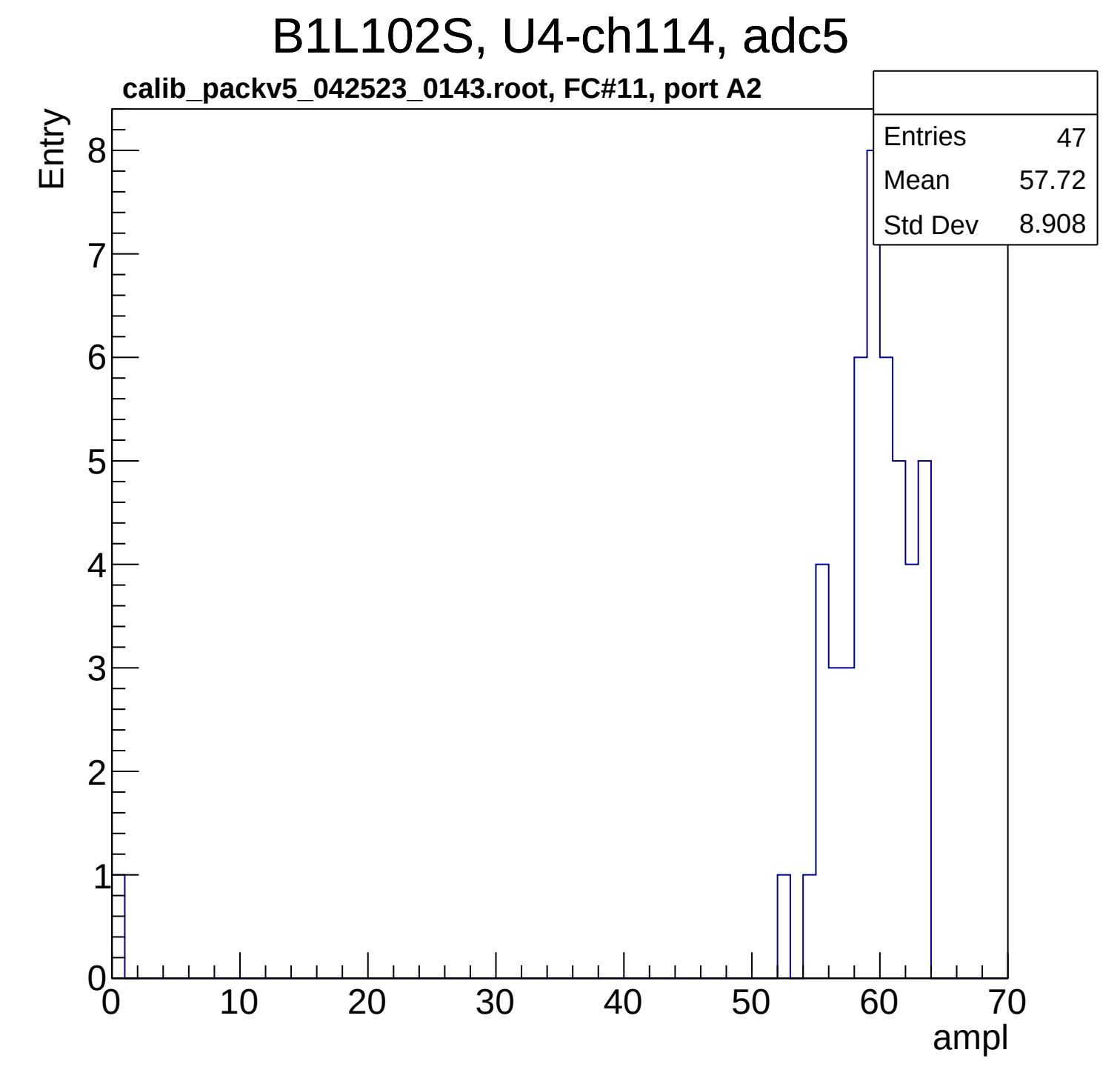
B1L102S, U4-ch114, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 47
Mean 57.72
Std Dev 8.908
Entry
ampl
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1
2
3
4
5
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7
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0
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60
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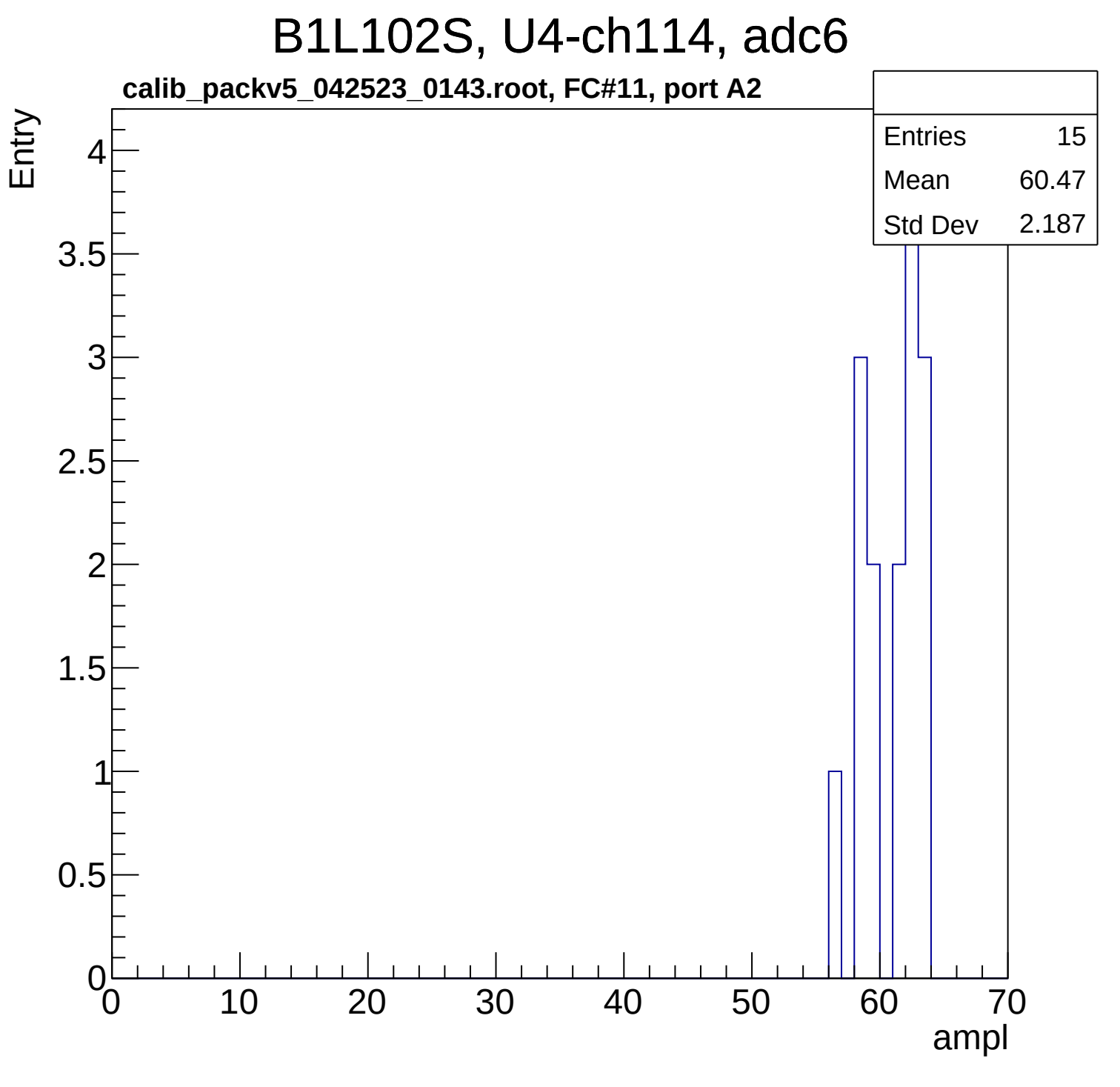
B1L102S, U4-ch114, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 15
Mean 60.47
Std Dev 2.187
Entry
ampl
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0.5
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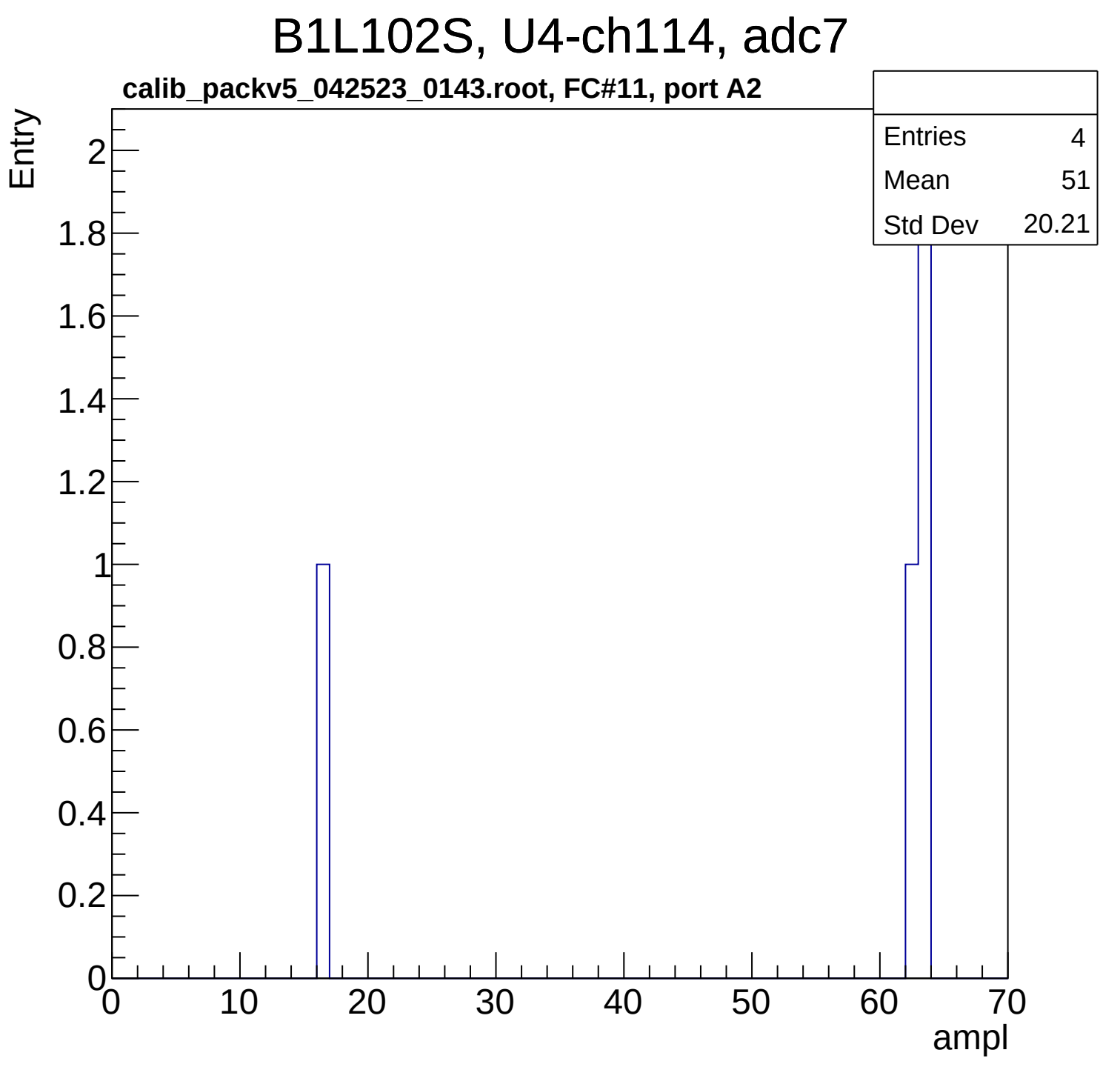
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U4-ch114, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 4
Mean 51
Std Dev 20.21
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
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60
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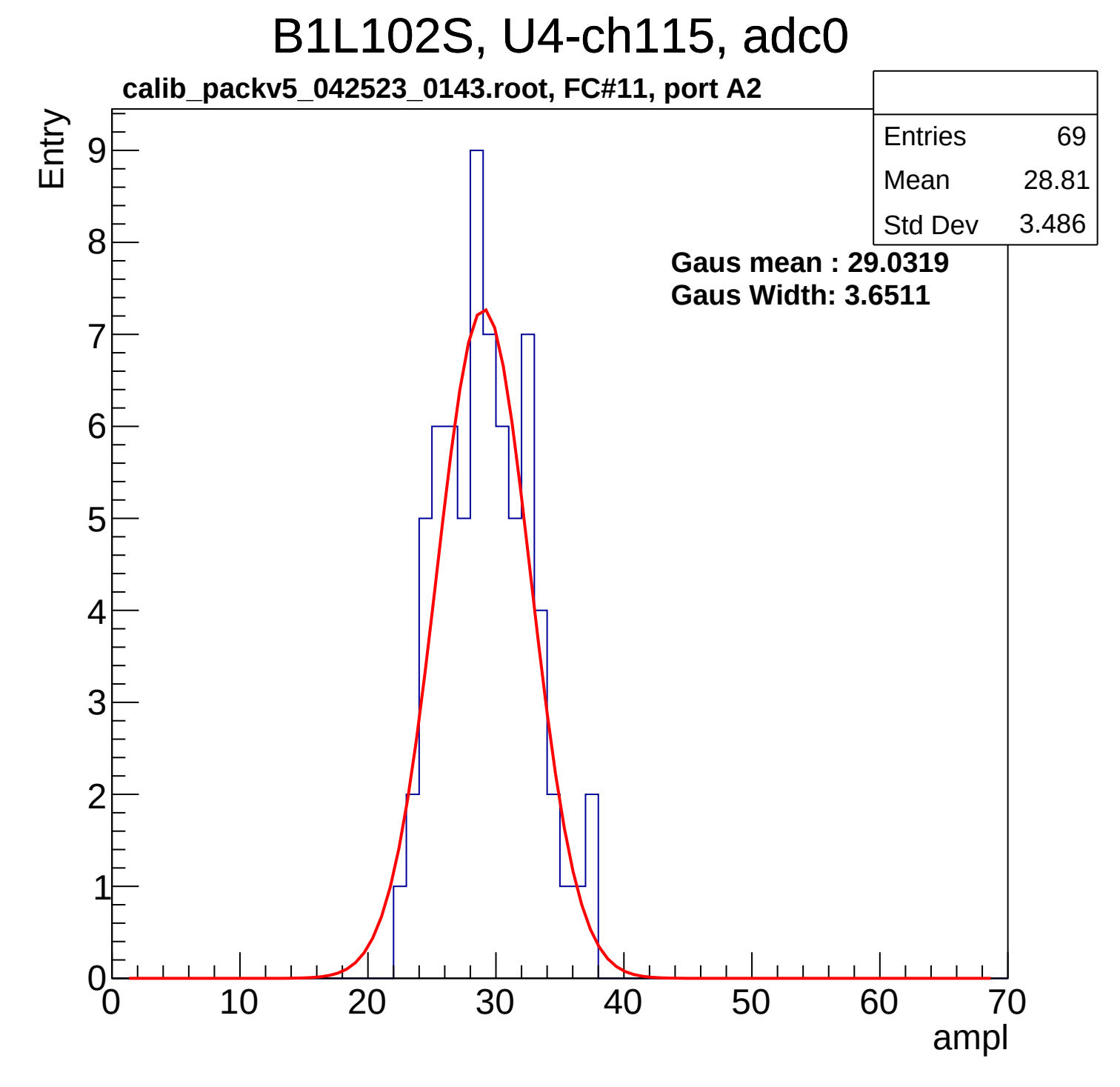
B1L102S, U4-ch115, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 28.81
Std Dev 3.486
Gaus mean : 29.0319
Gaus Width: 3.6511
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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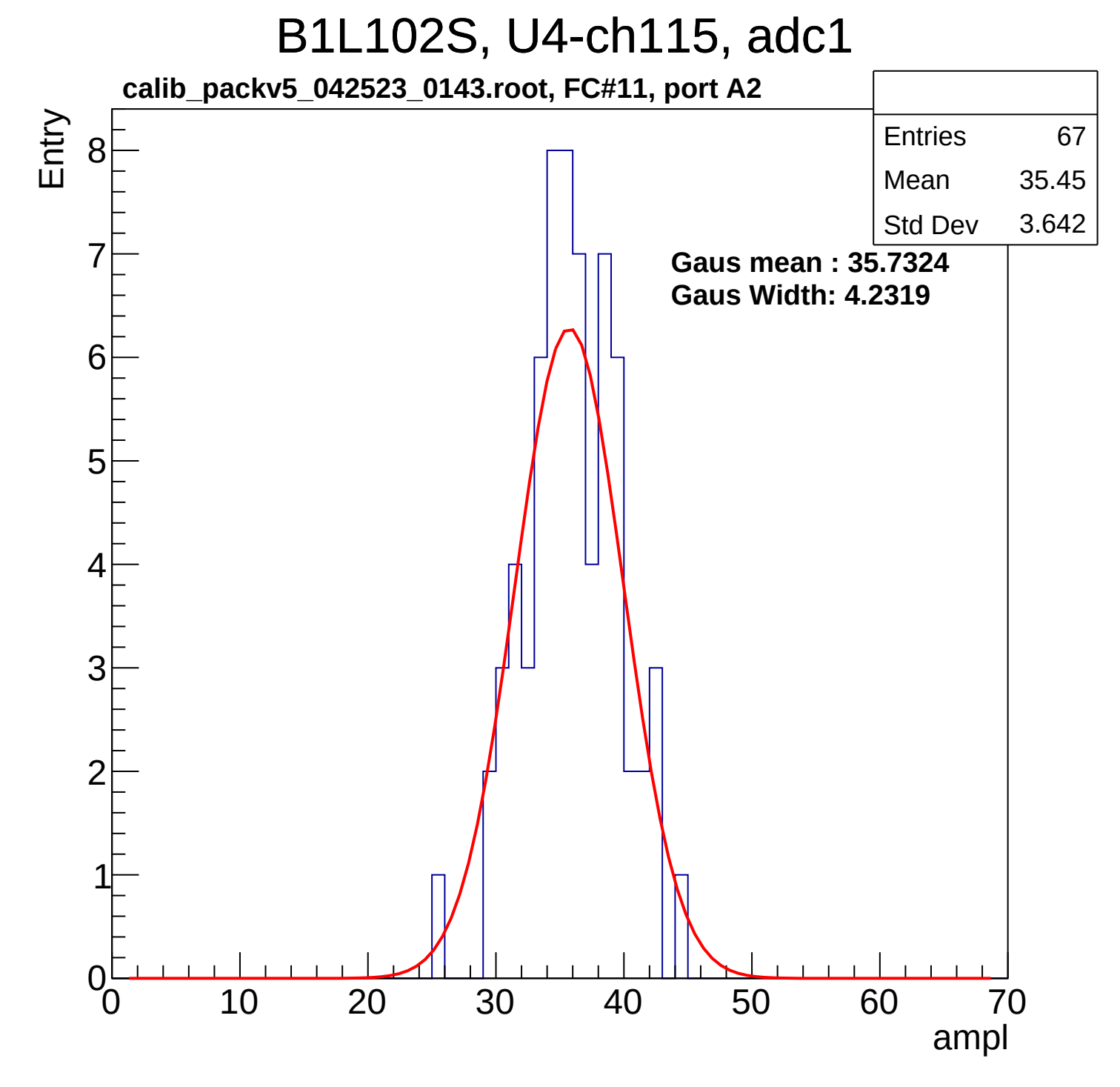
60
70


B1L102S, U4-ch115, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 35.45
Std Dev 3.642
Gaus mean : 35.7324
Gaus Width: 4.2319
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
50
60
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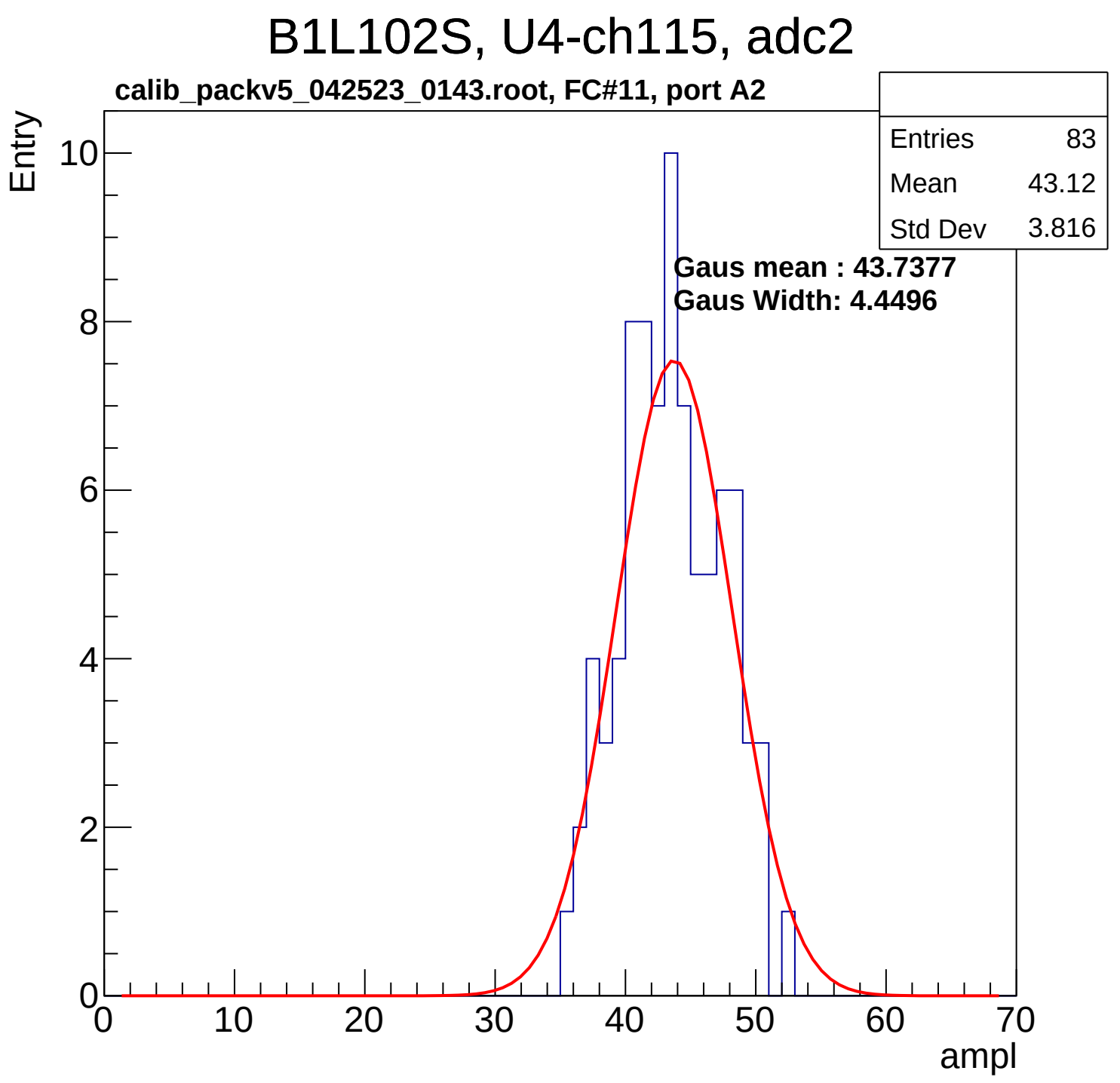
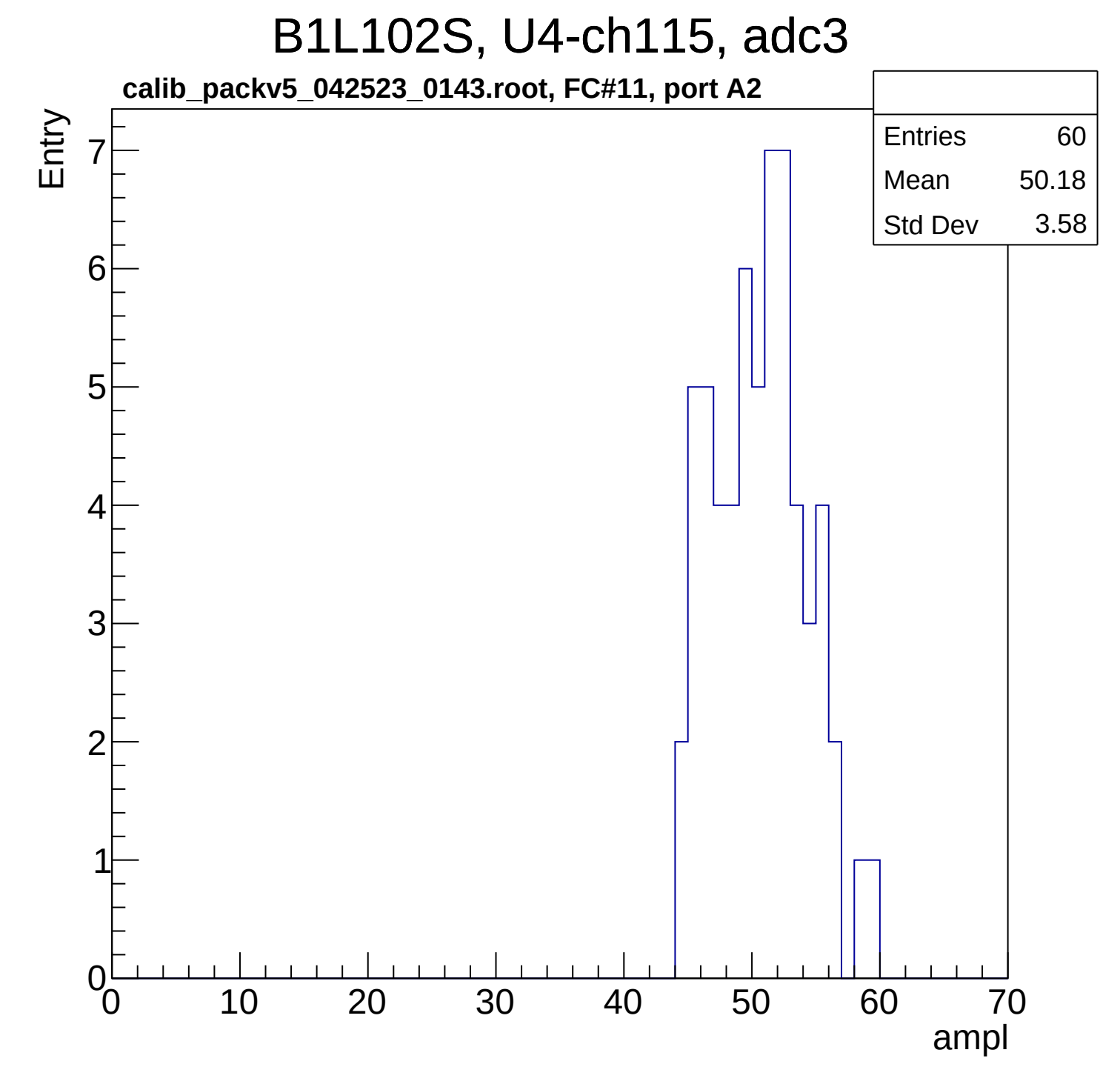

B1L102S, U4-ch115, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 83
Mean 43.12
Std Dev 3.816
Gaus mean : 43.7377
Gaus Width: 4.4496
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch115, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 60
Mean 50.18
Std Dev 3.58
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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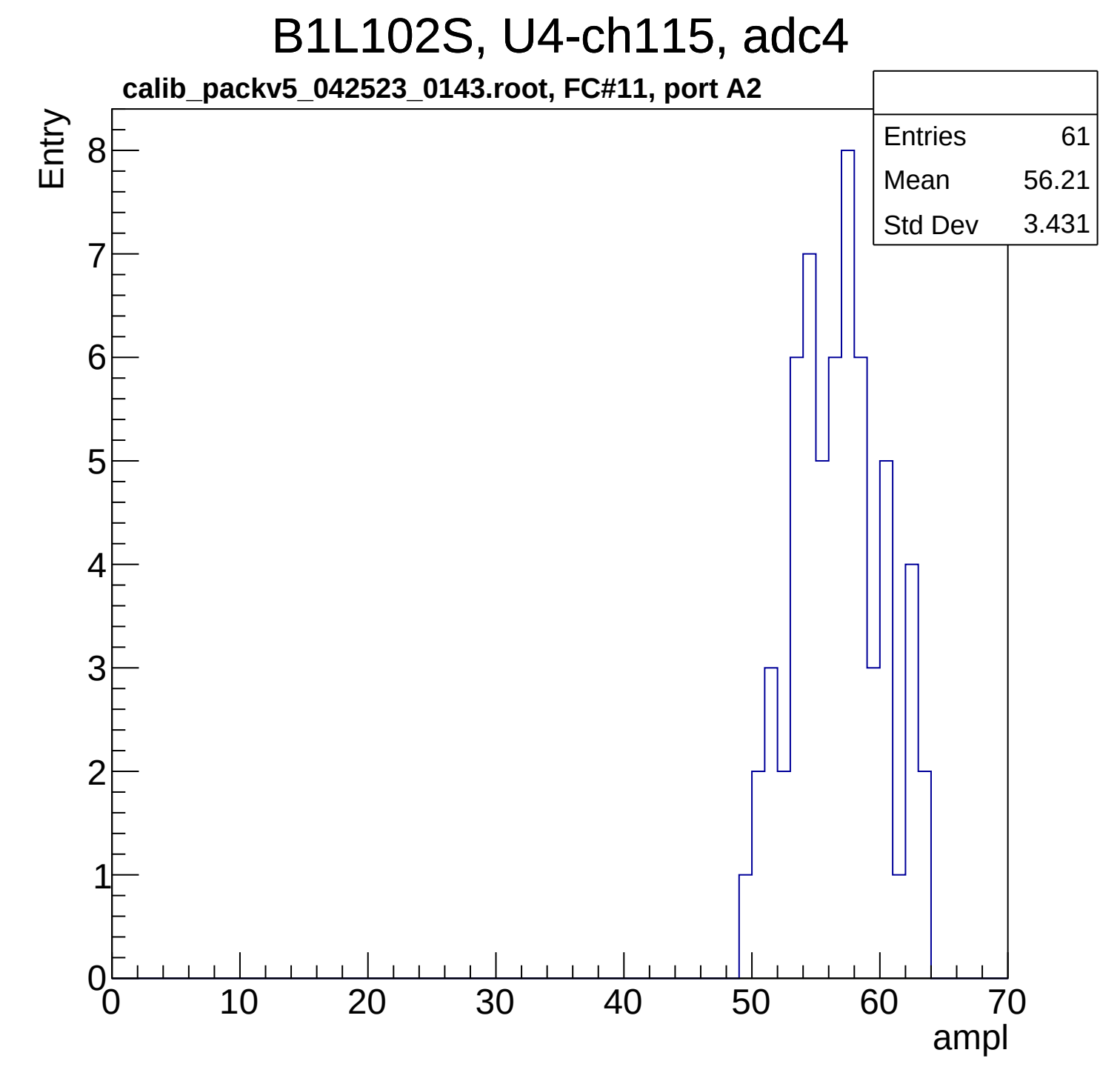
B1L102S, U4-ch115, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 56.21
Std Dev 3.431
Entry
ampl
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2
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4
5
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0
10
20
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40
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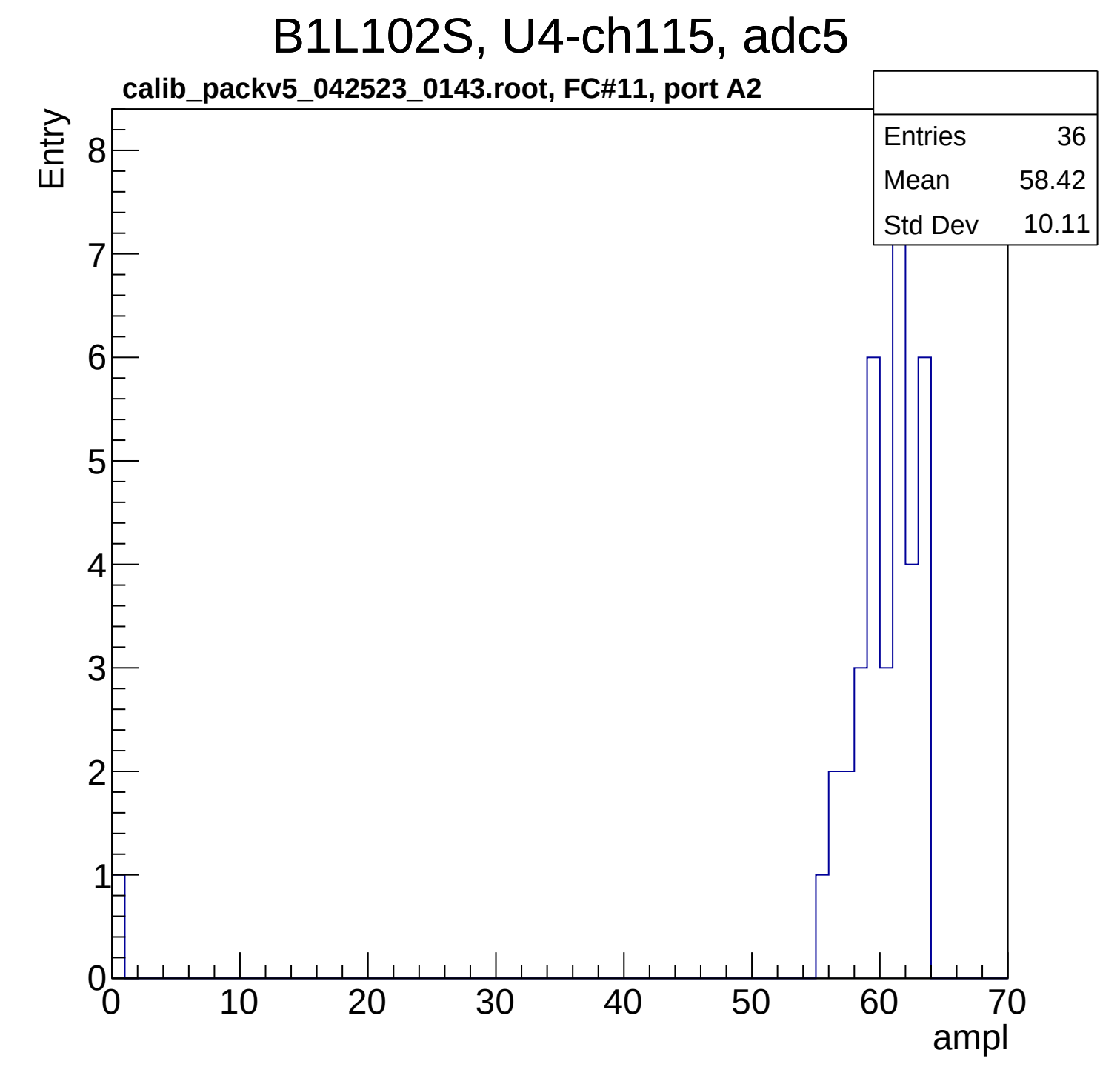
60
70


B1L102S, U4-ch115, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 36
Mean 58.42
Std Dev 10.11
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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30
40
50
60
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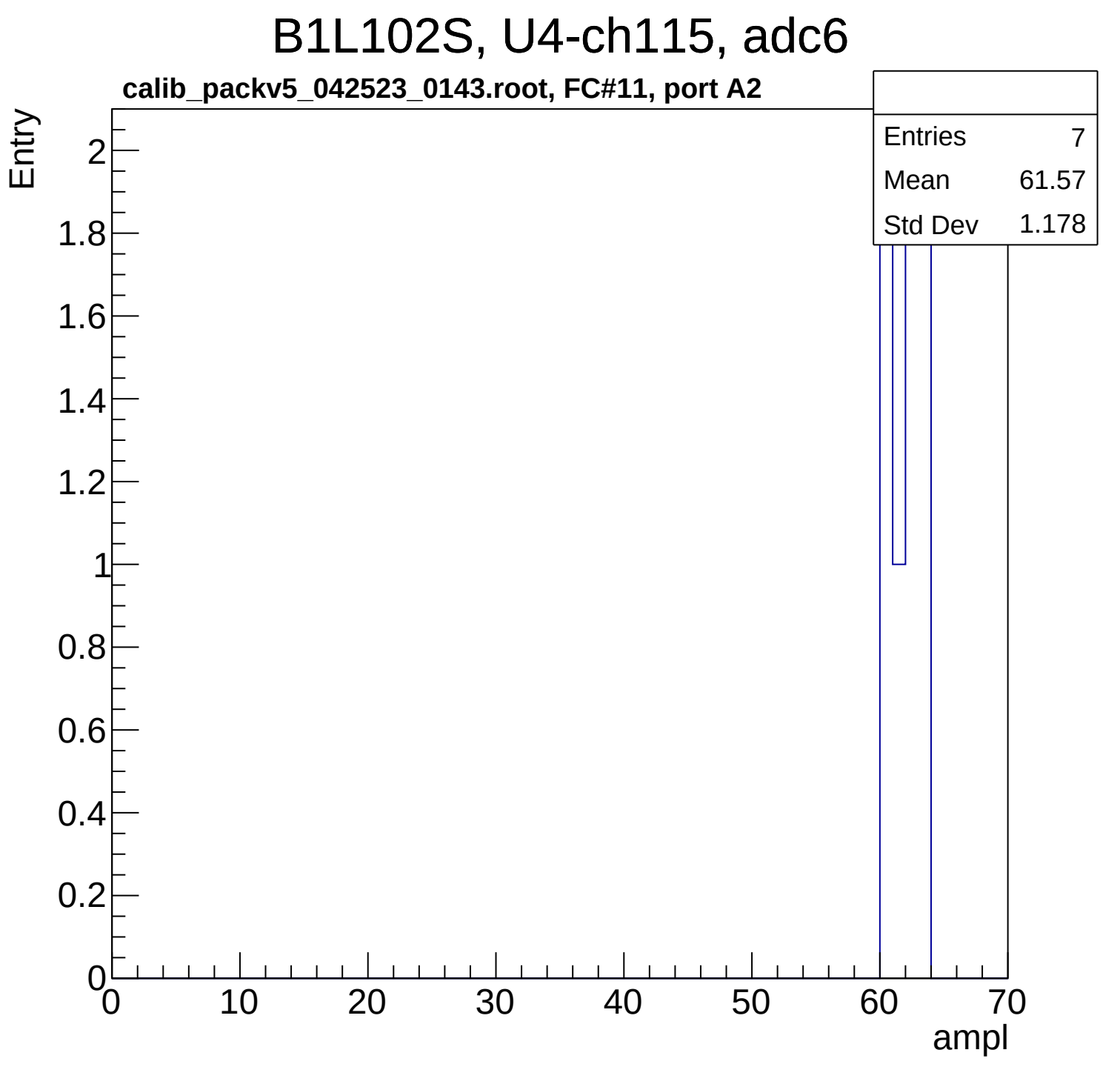
B1L102S, U4-ch115, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 7
Mean 61.57
Std Dev 1.178
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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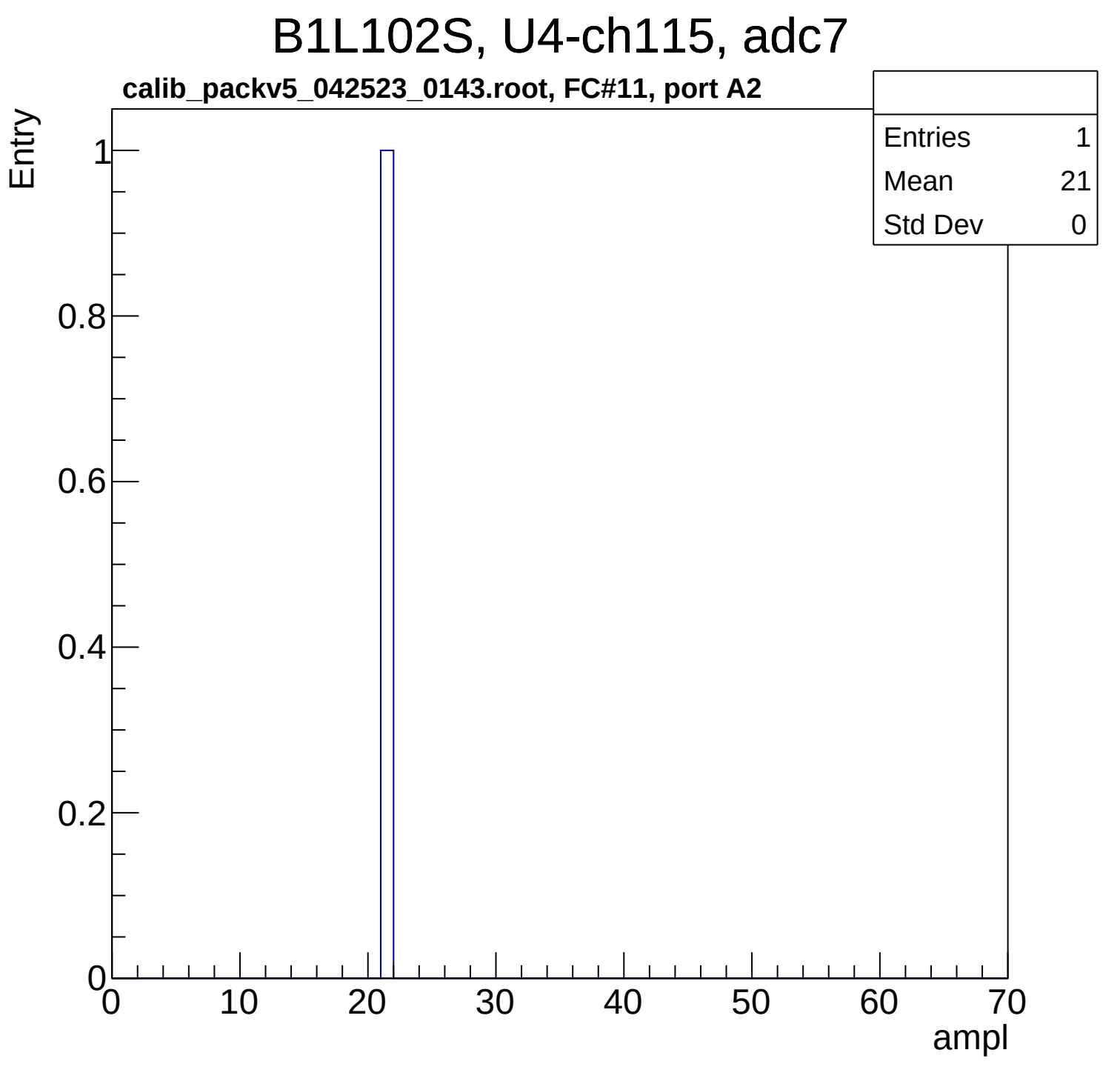
40
50
60
70


B1L102S, U4-ch115, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 21
Std Dev 0
Entry
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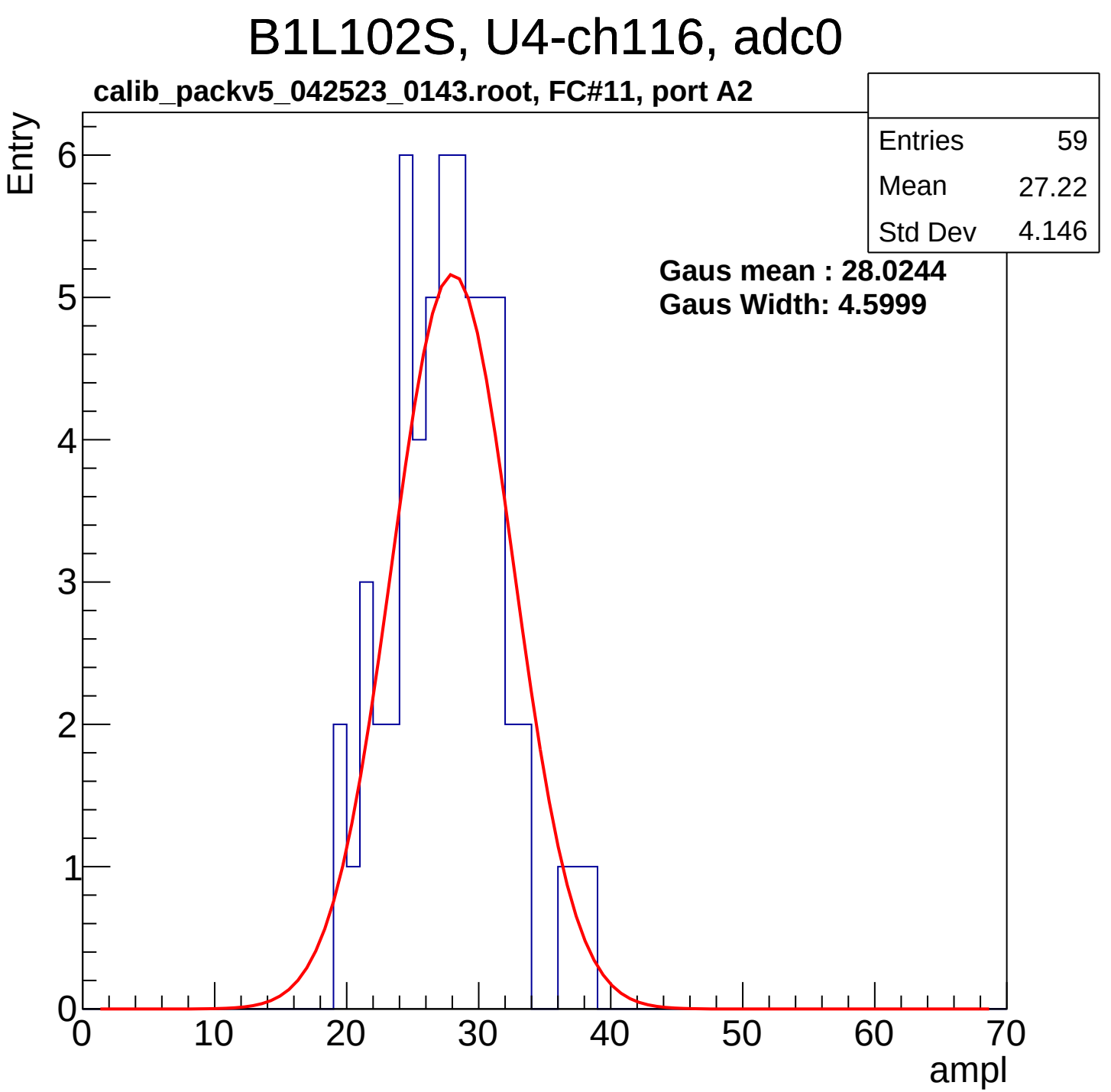
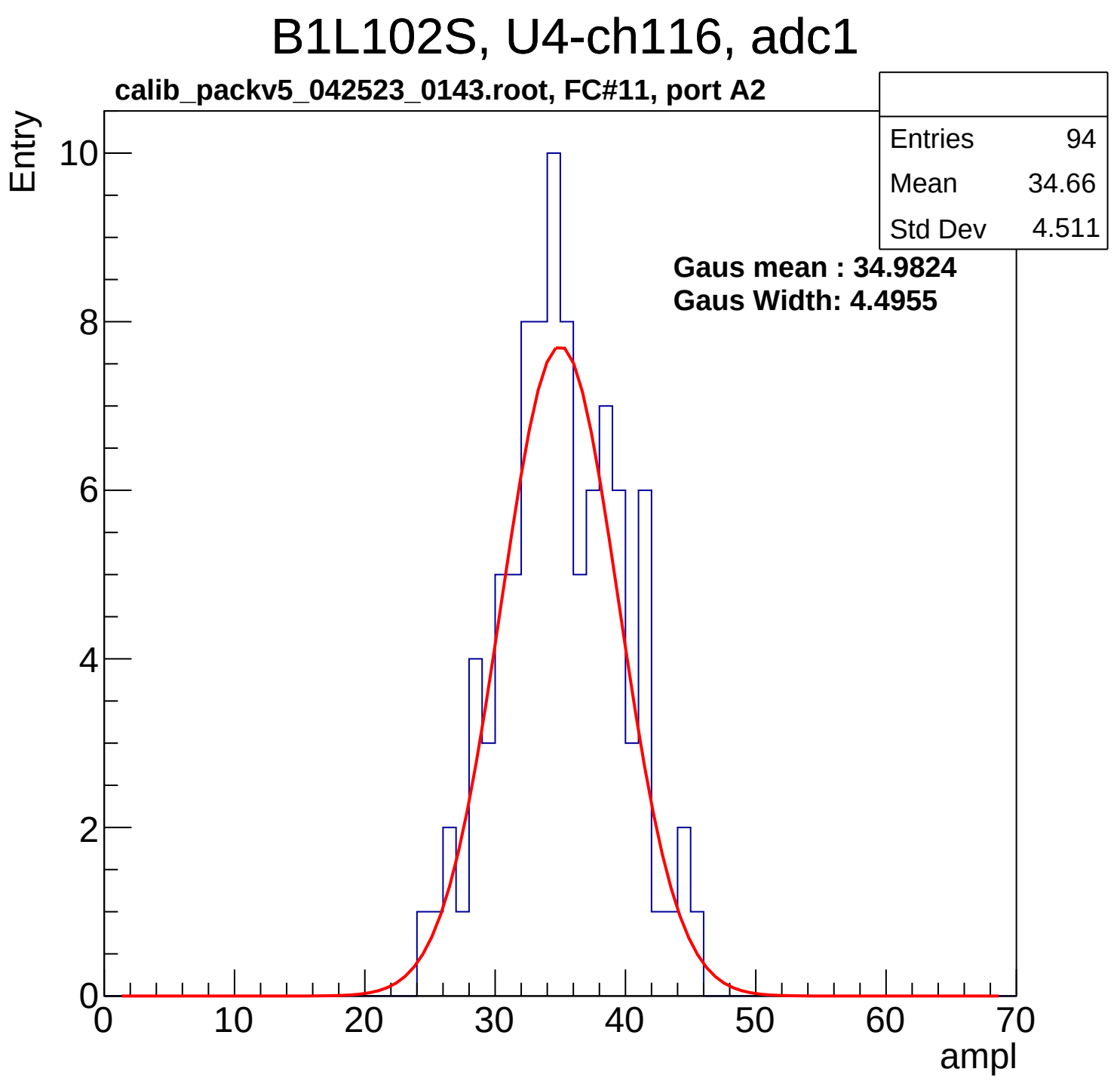
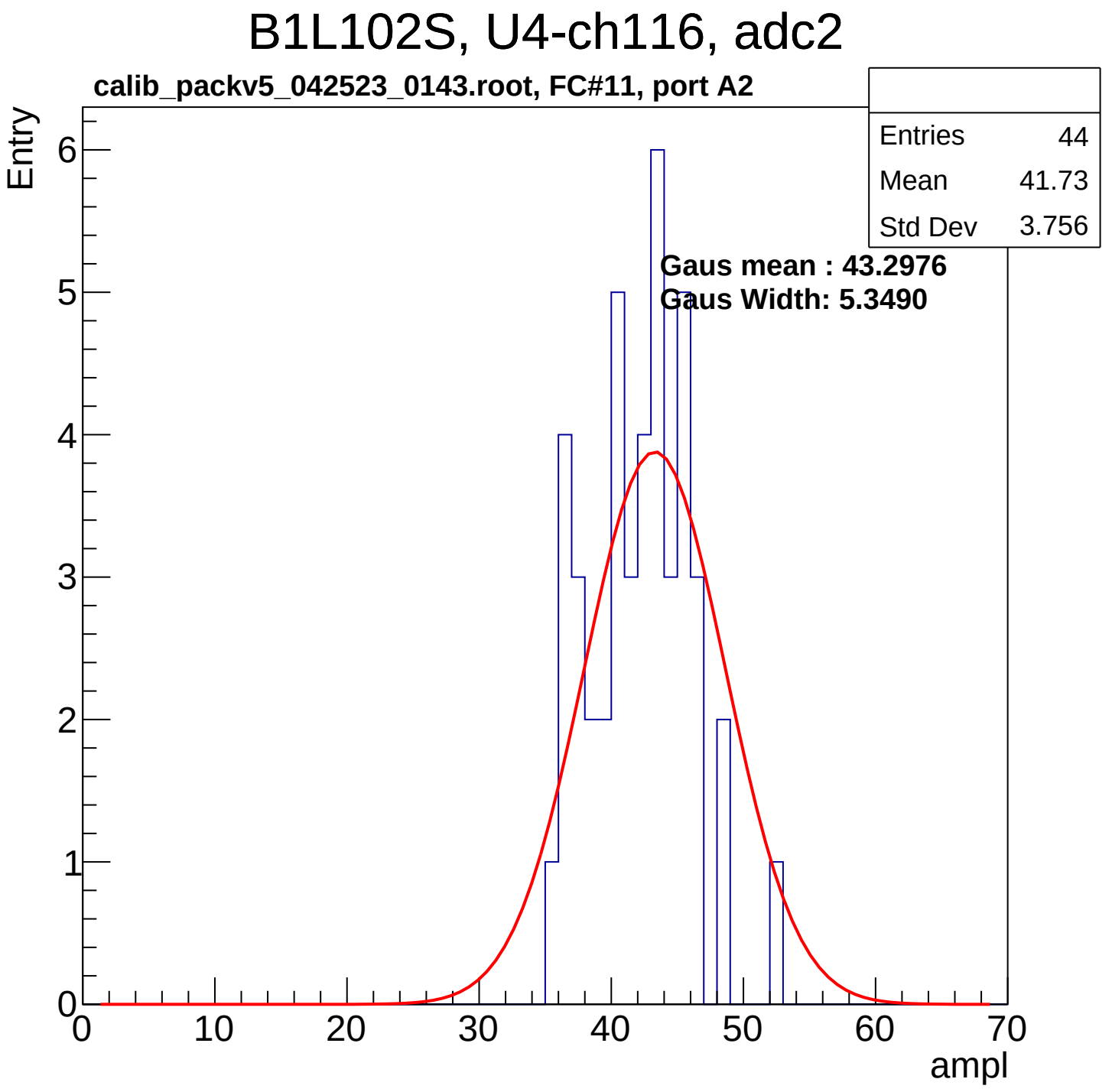
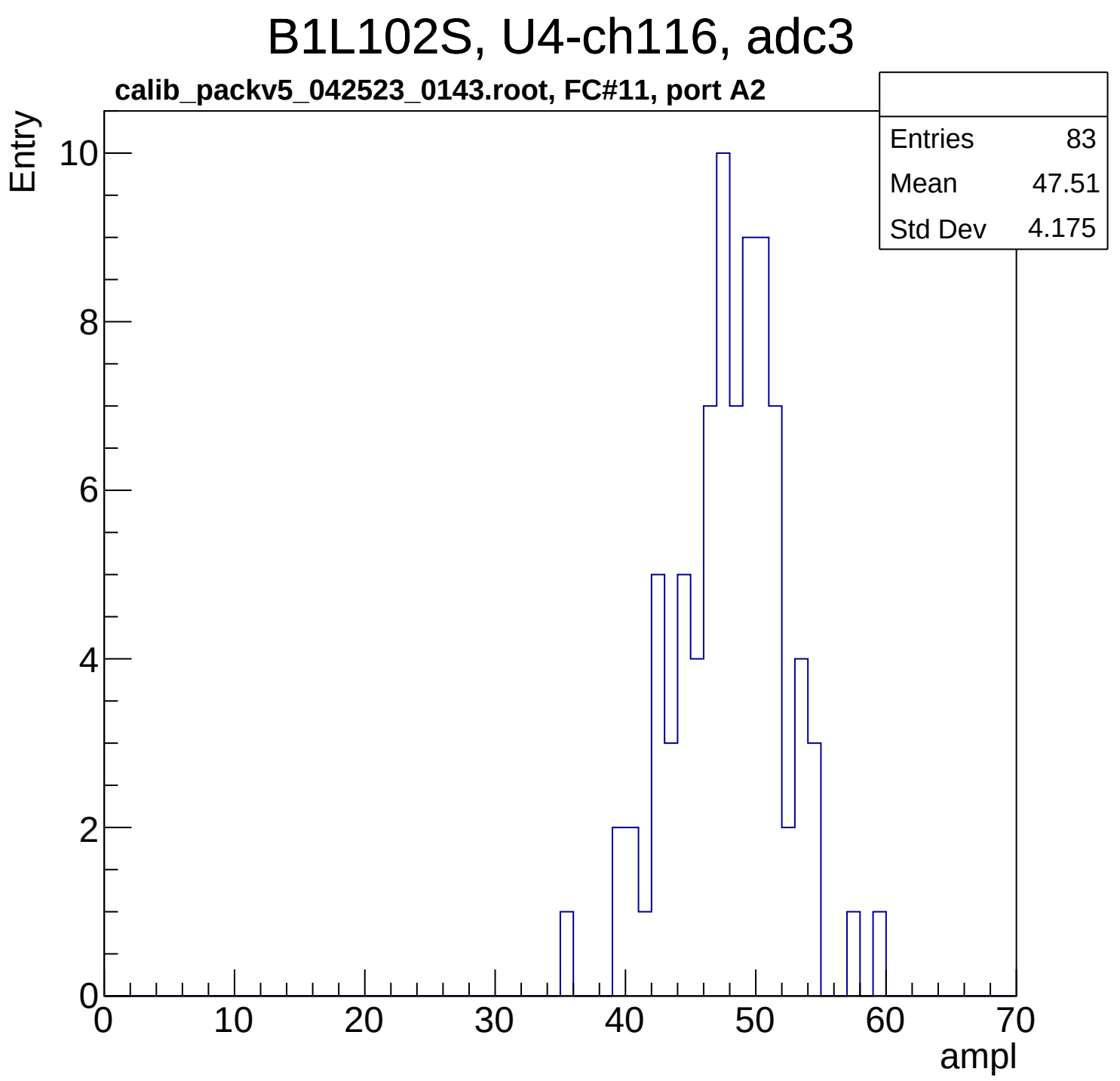
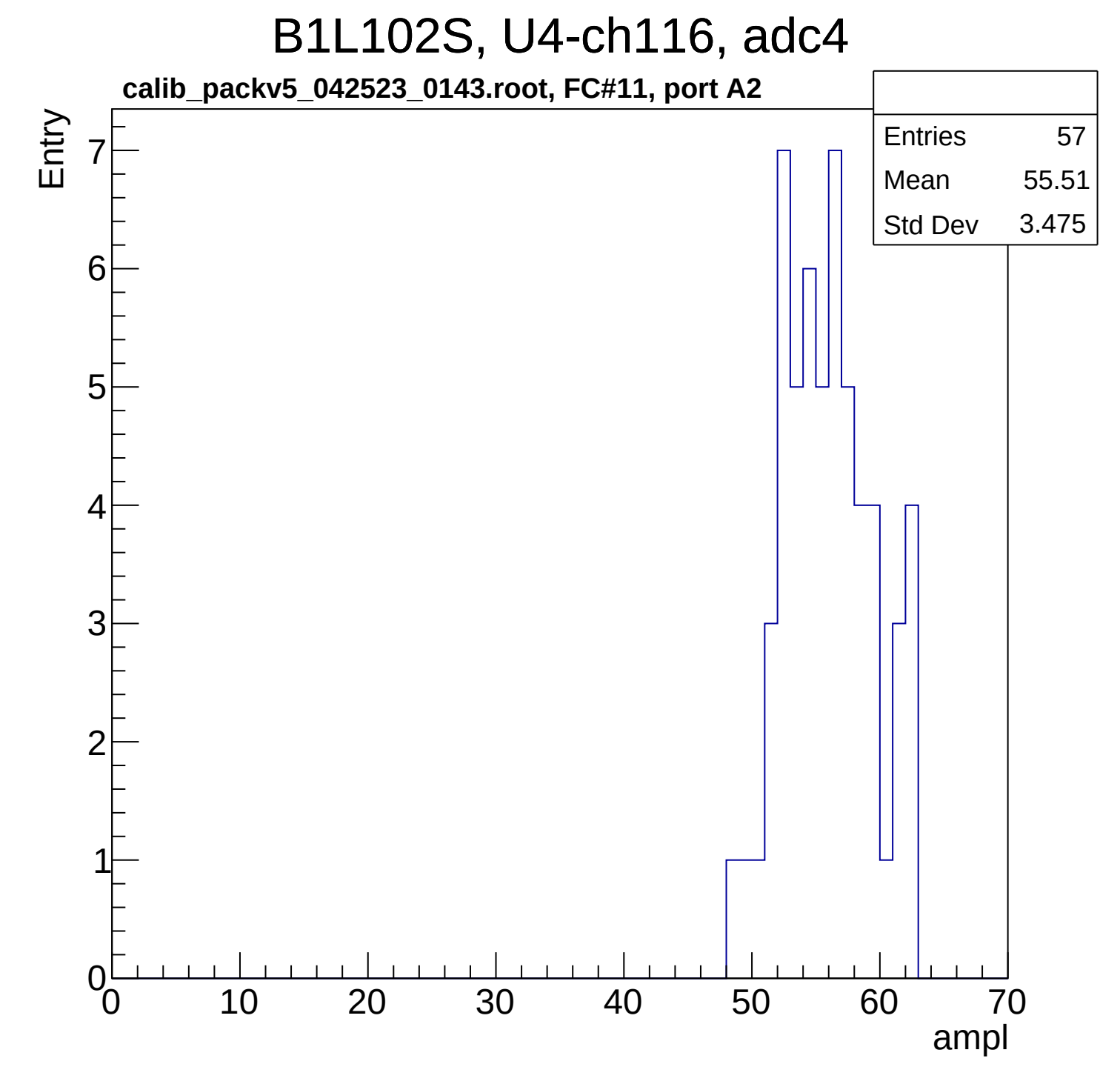
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

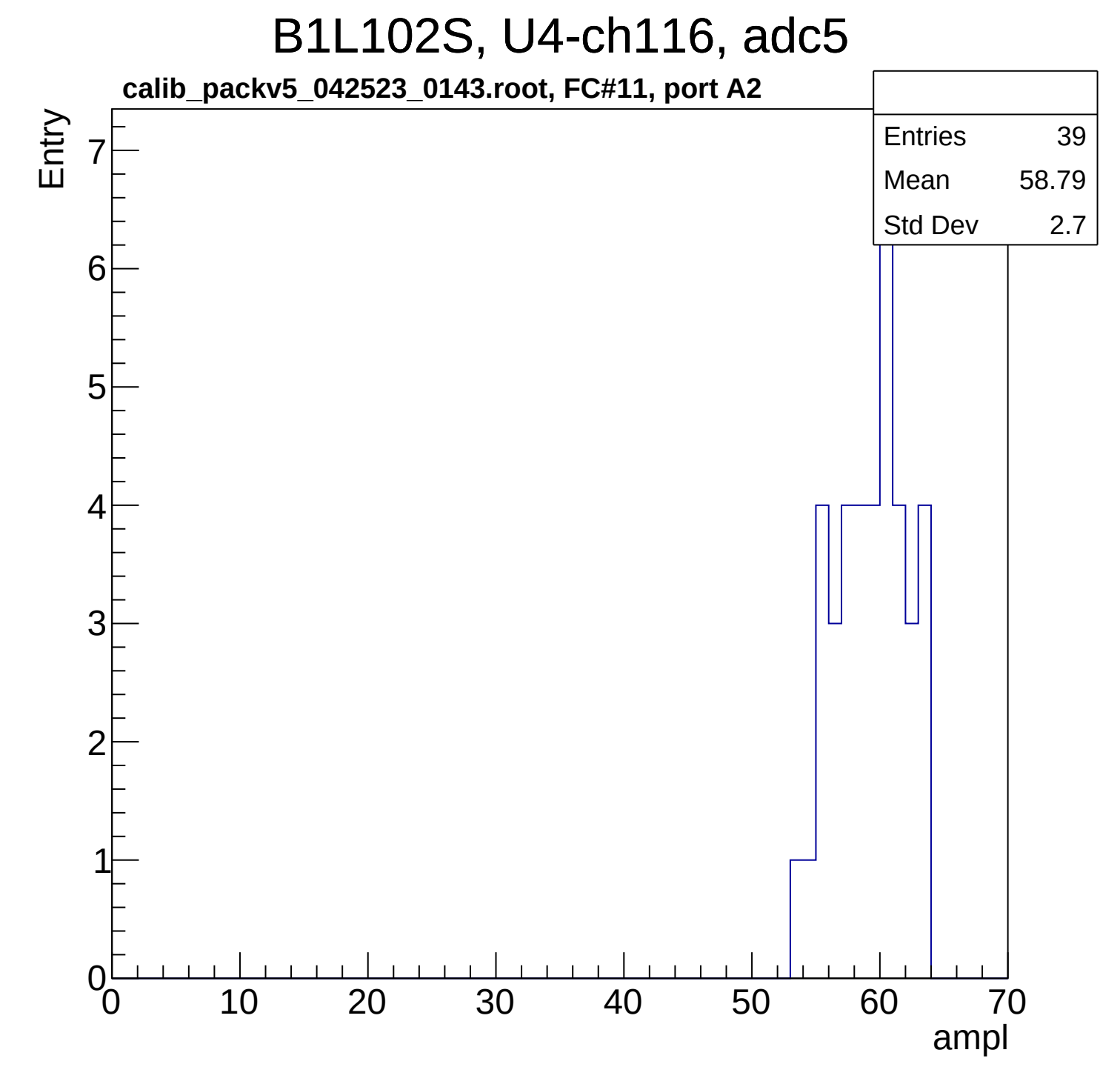

B1L102S, U4-ch116, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 59
Mean 27.22
Std Dev 4.146
Gaus mean : 28.0244
Gaus Width: 4.5999
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

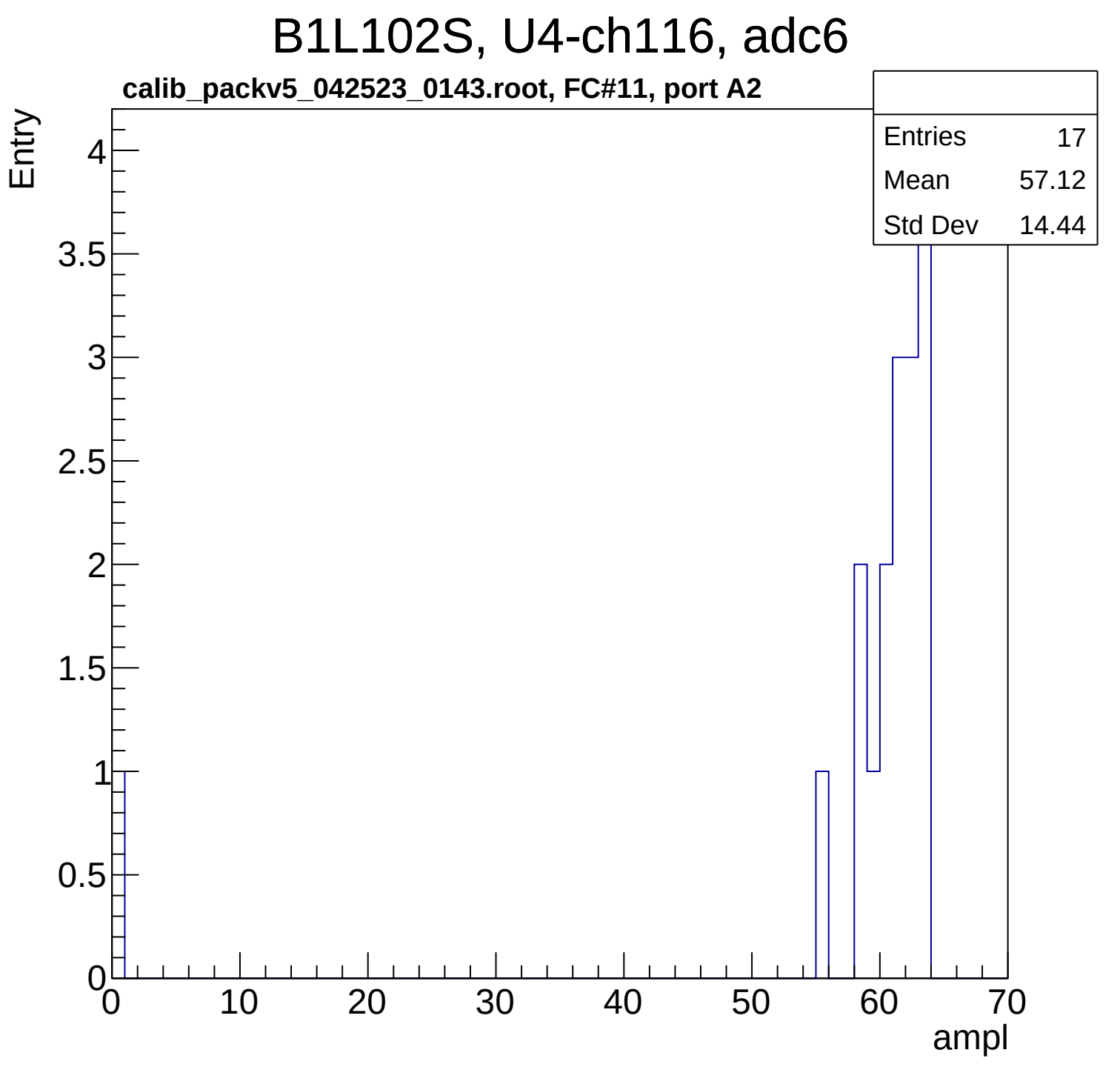

B1L102S, U4-ch116, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 94
Mean 34.66
Std Dev 4.511
Gaus mean : 34.9824
Gaus Width: 4.4955
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

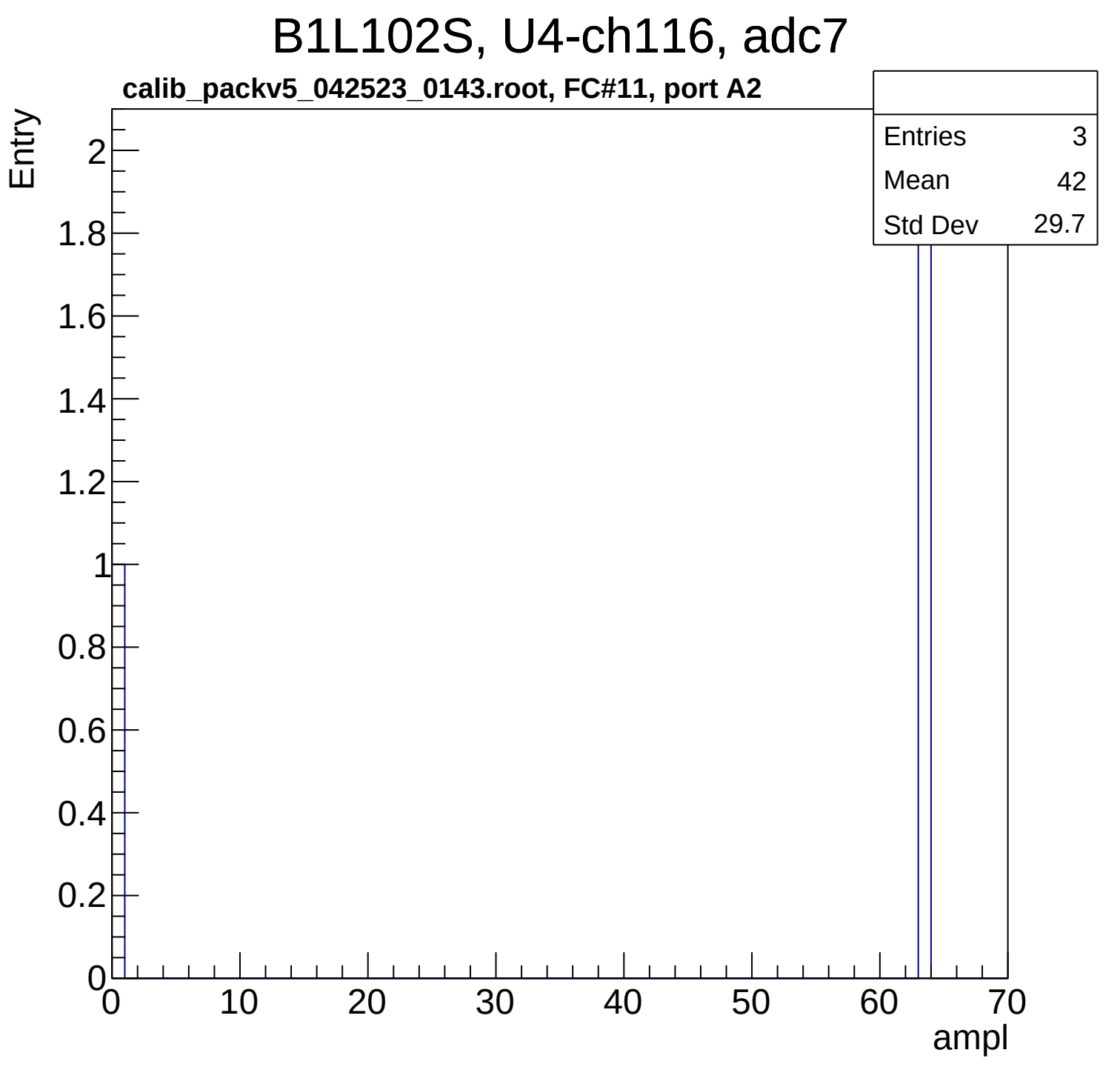

B1L102S, U4-ch116, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 44
Mean 41.73
Std Dev 3.756
Gaus mean : 43.2976
Gaus Width: 5.3490
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

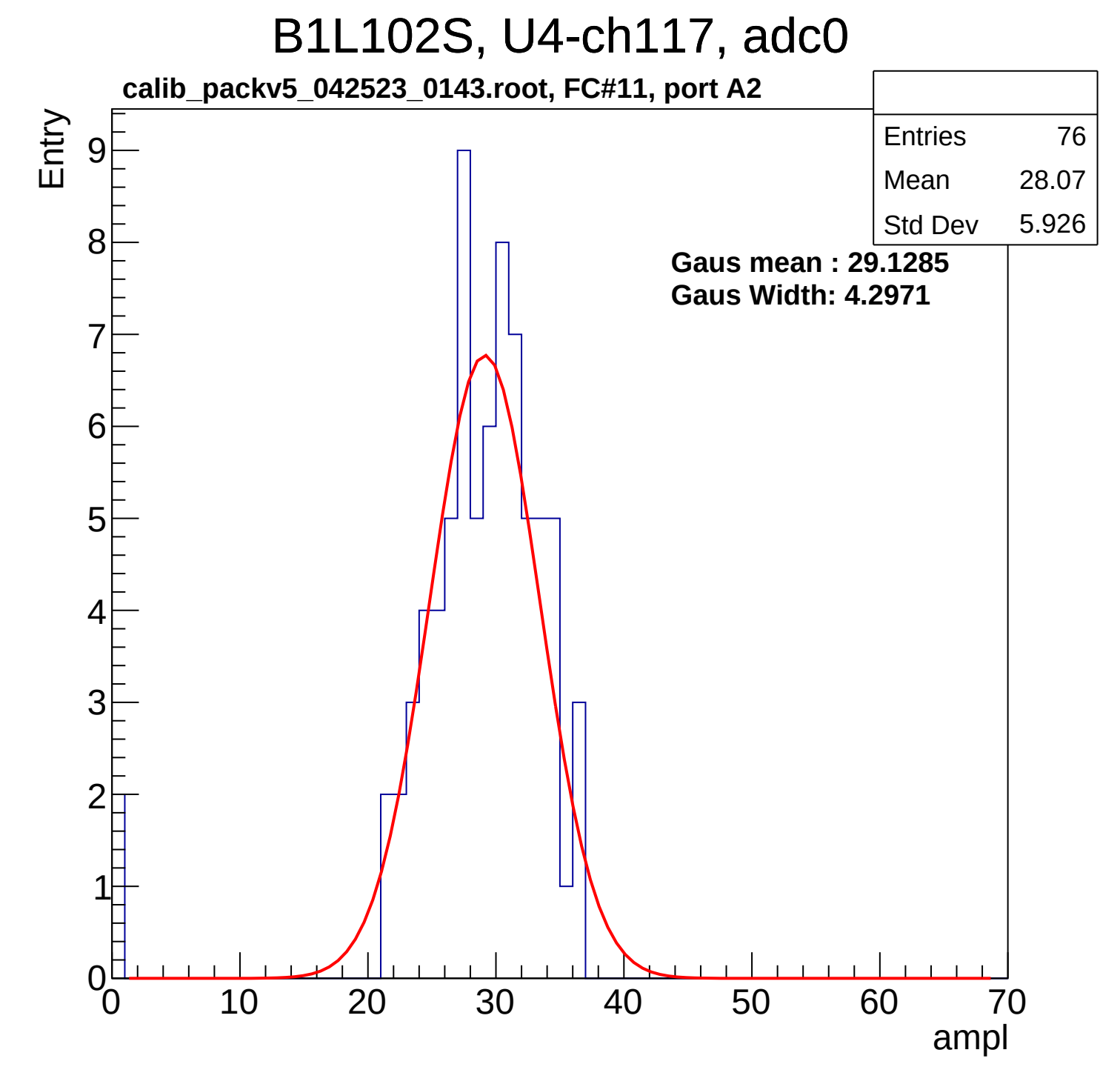

B1L102S, U4-ch116, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 83
Mean 47.51
Std Dev 4.175
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

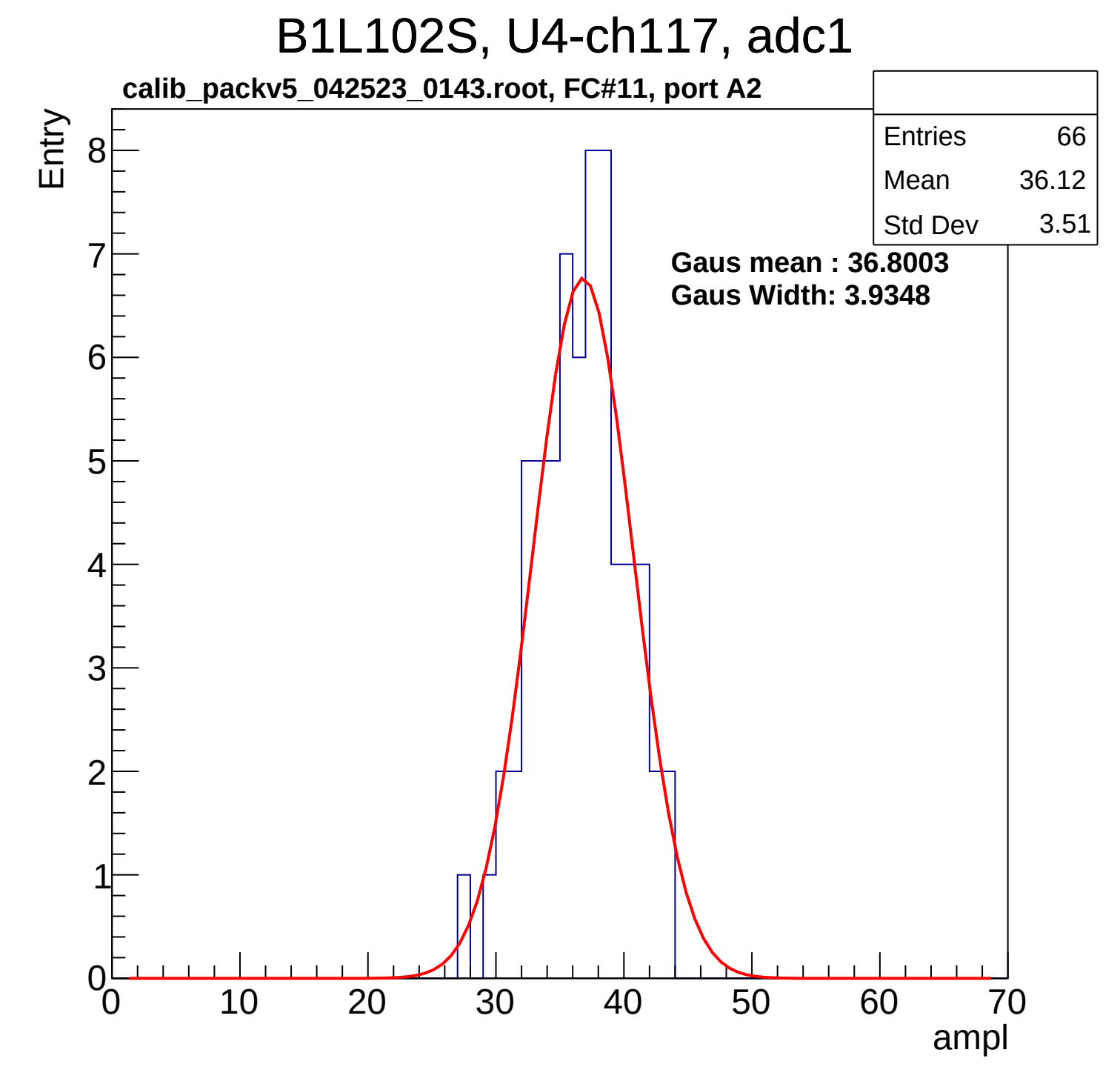

B1L102S, U4-ch116, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 57
Mean 55.51
Std Dev 3.475
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

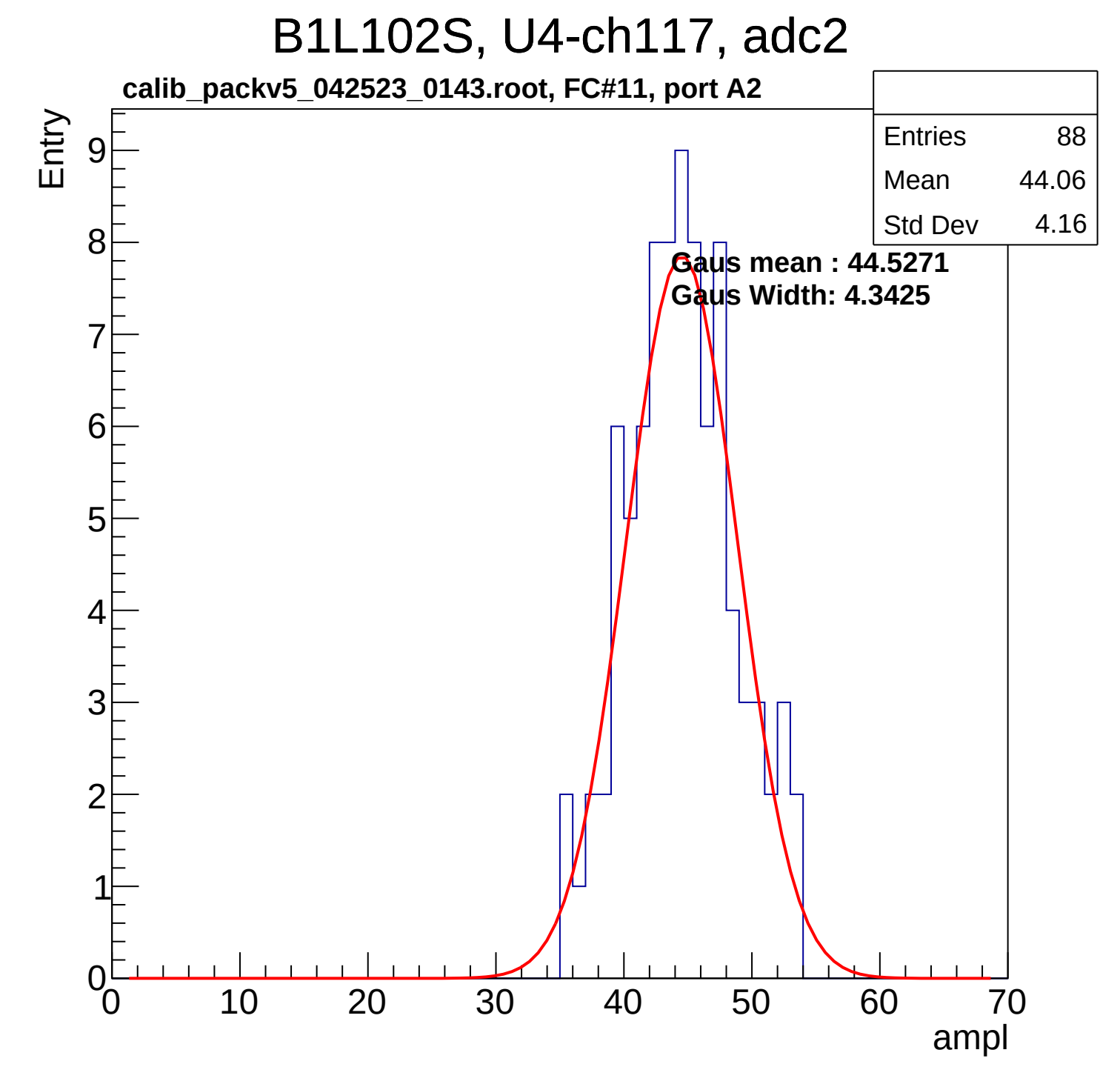

B1L102S, U4-ch116, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 39
Mean 58.79
Std Dev 2.7
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

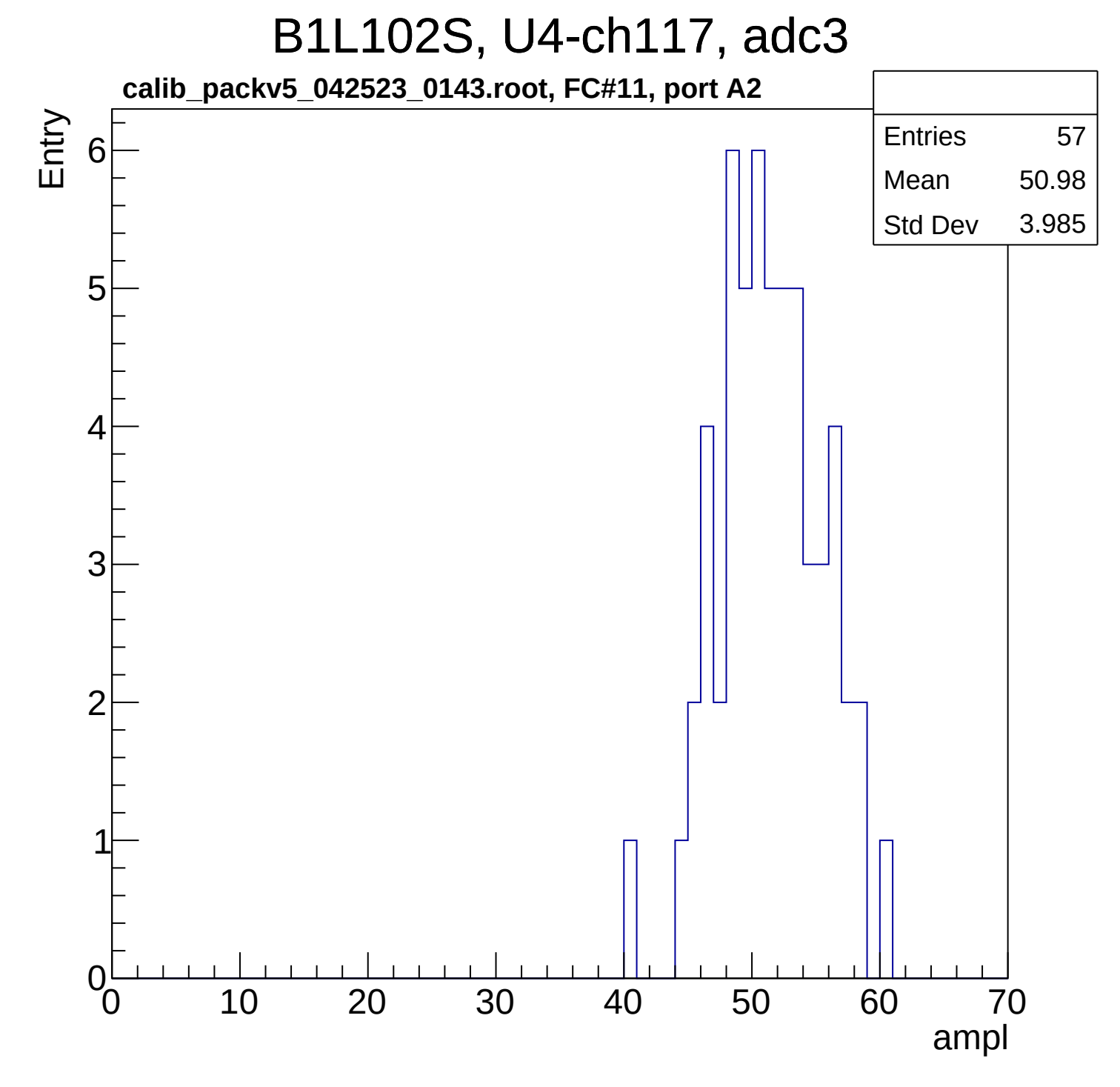

B1L102S, U4-ch116, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 17
Mean 57.12
Std Dev 14.44
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

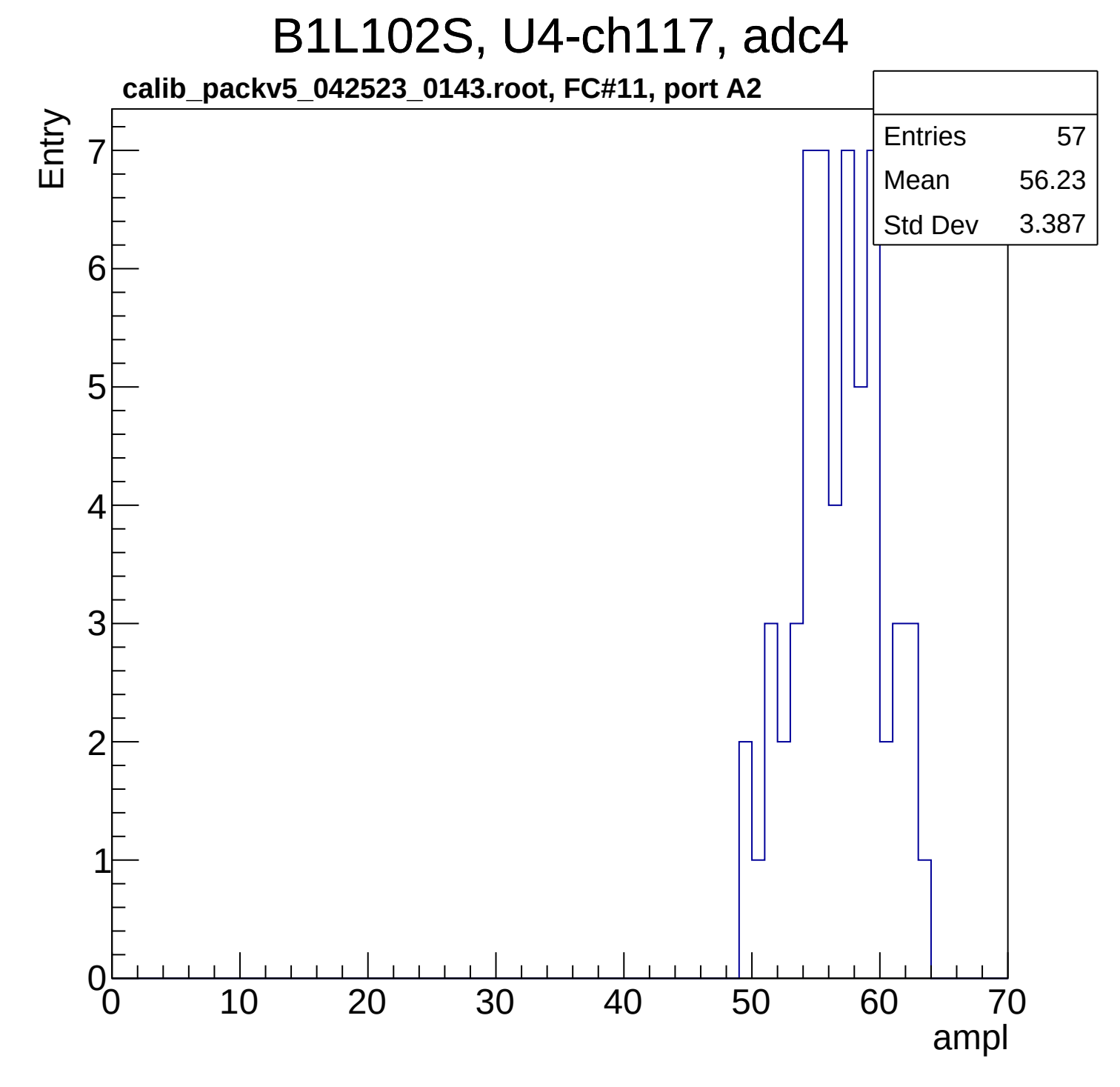

B1L102S, U4-ch116, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 42
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

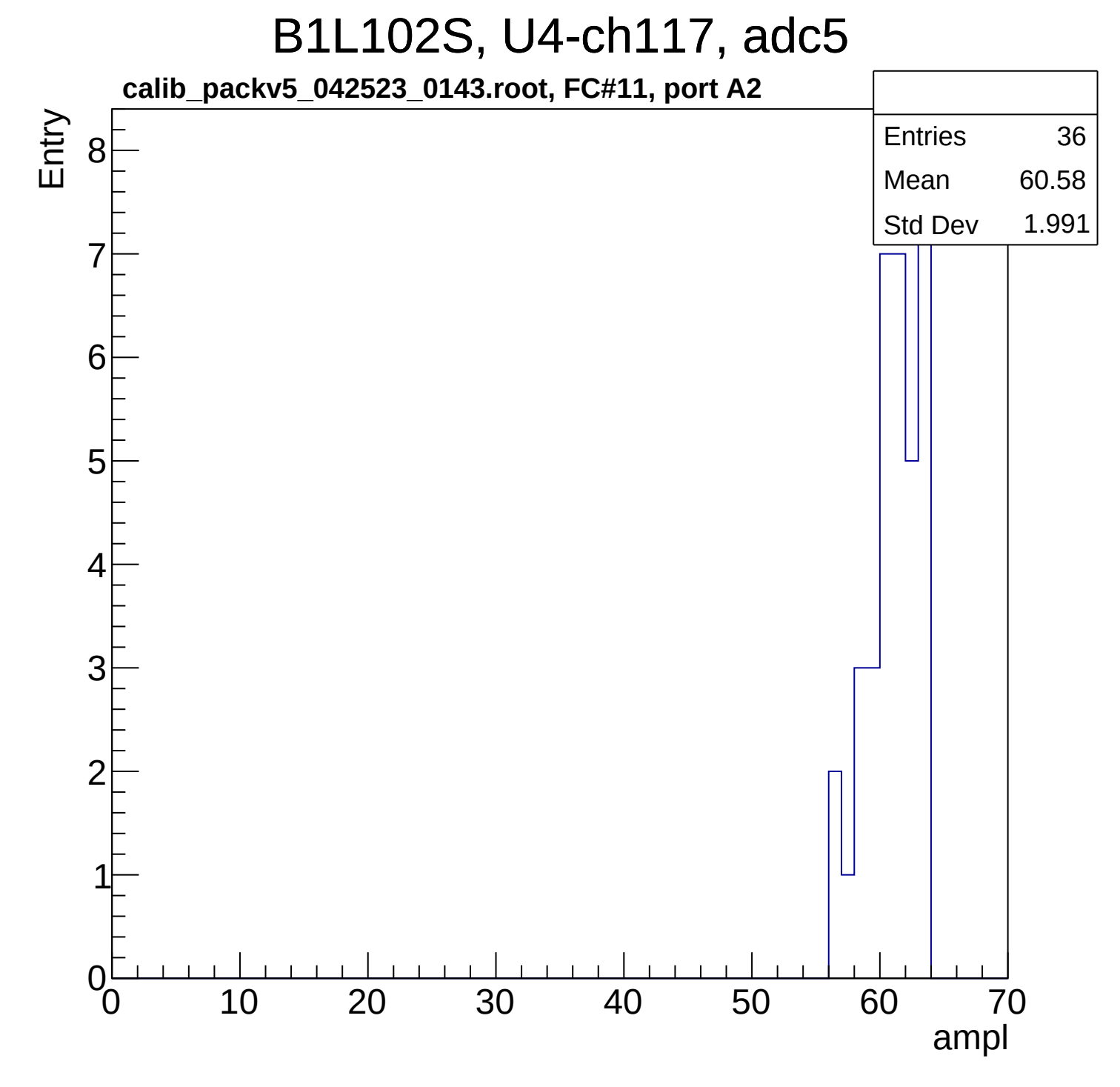

B1L102S, U4-ch117, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 28.07
Std Dev 5.926
Gaus mean : 29.1285
Gaus Width: 4.2971
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

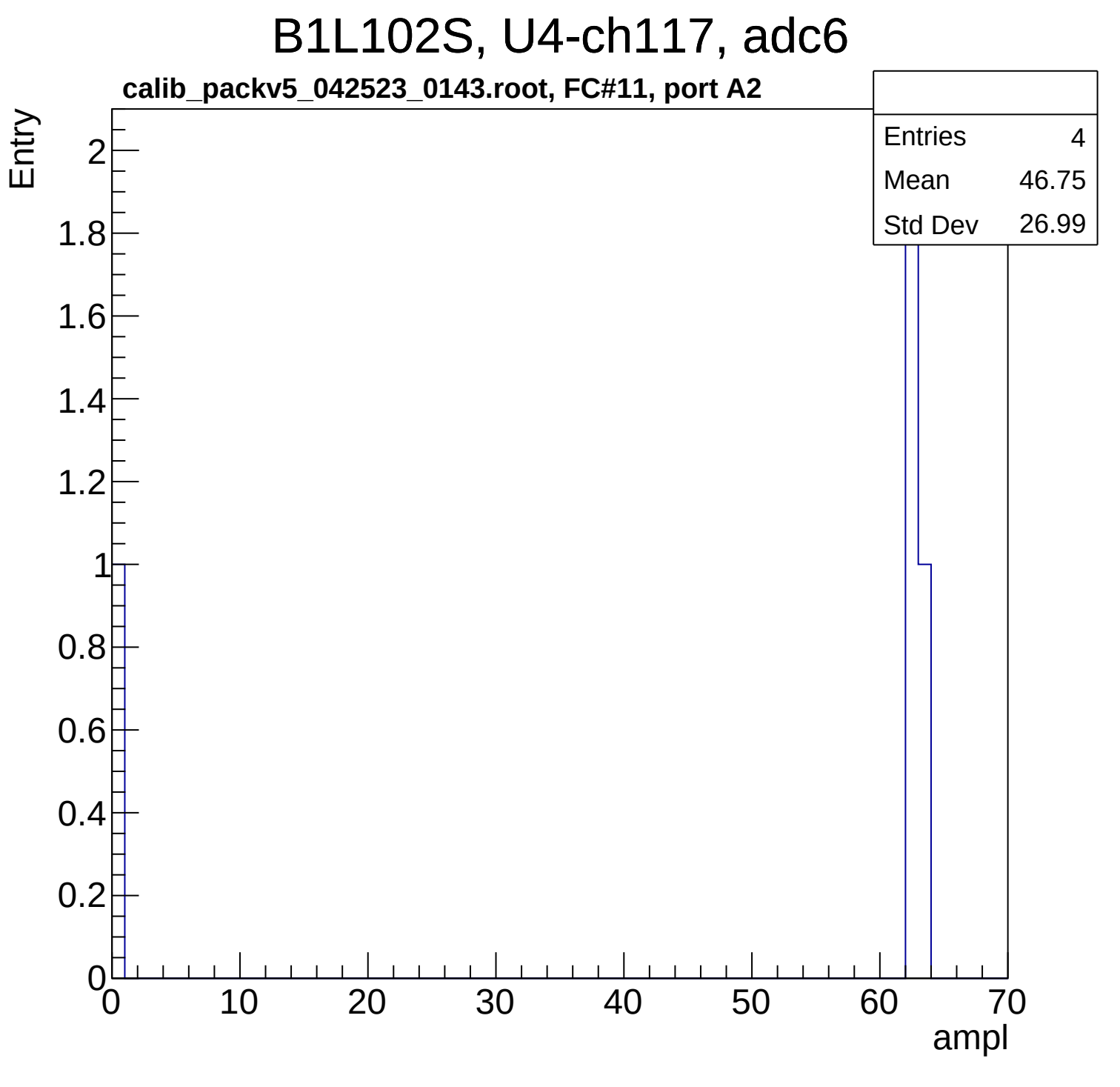

B1L102S, U4-ch117, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 36.12
Std Dev 3.51
Gaus mean : 36.8003
Gaus Width: 3.9348
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

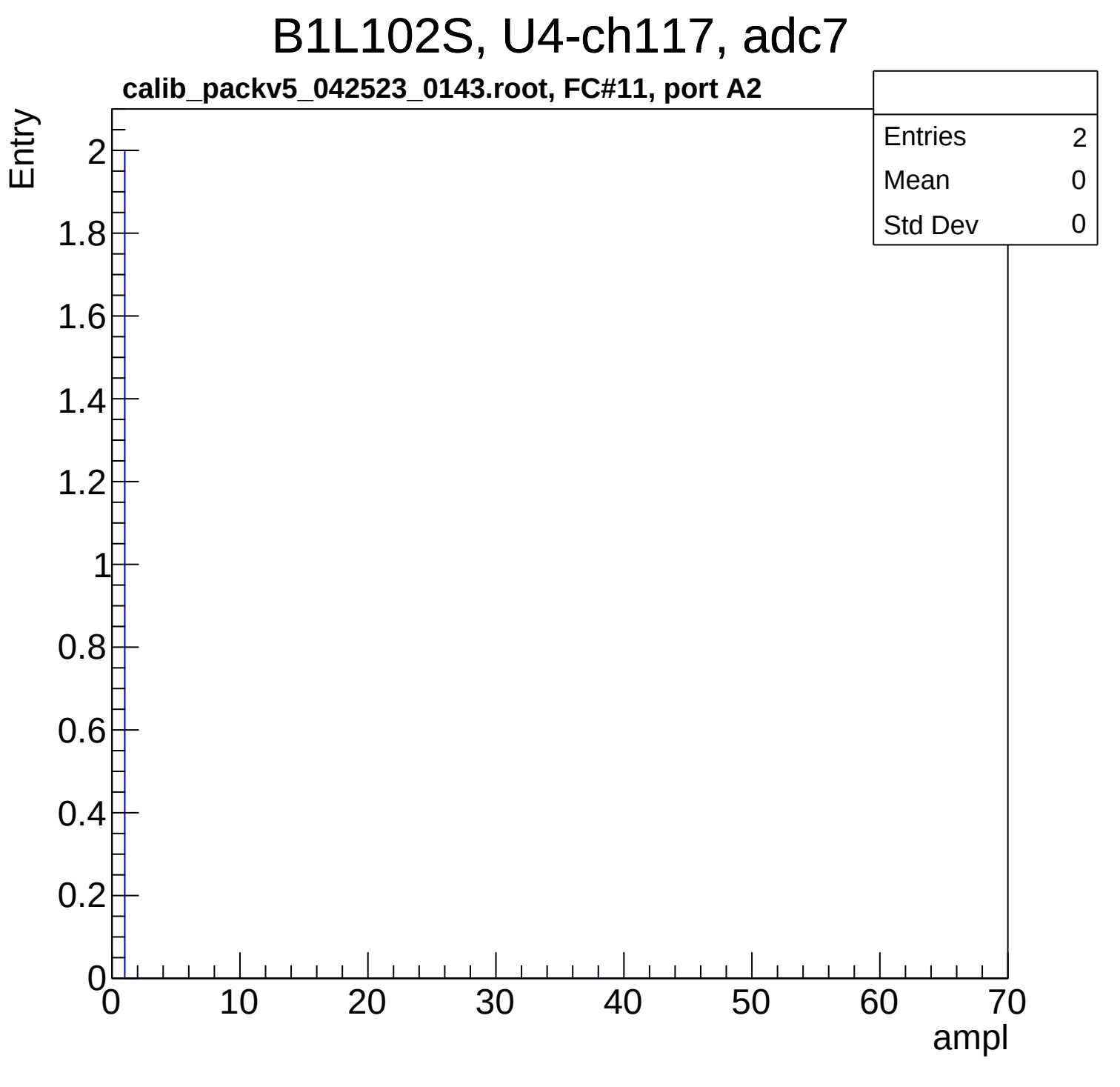

B1L102S, U4-ch117, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 88
Mean 44.06
Std Dev 4.16
Gaus mean : 44.5271
Gaus Width: 4.3425
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

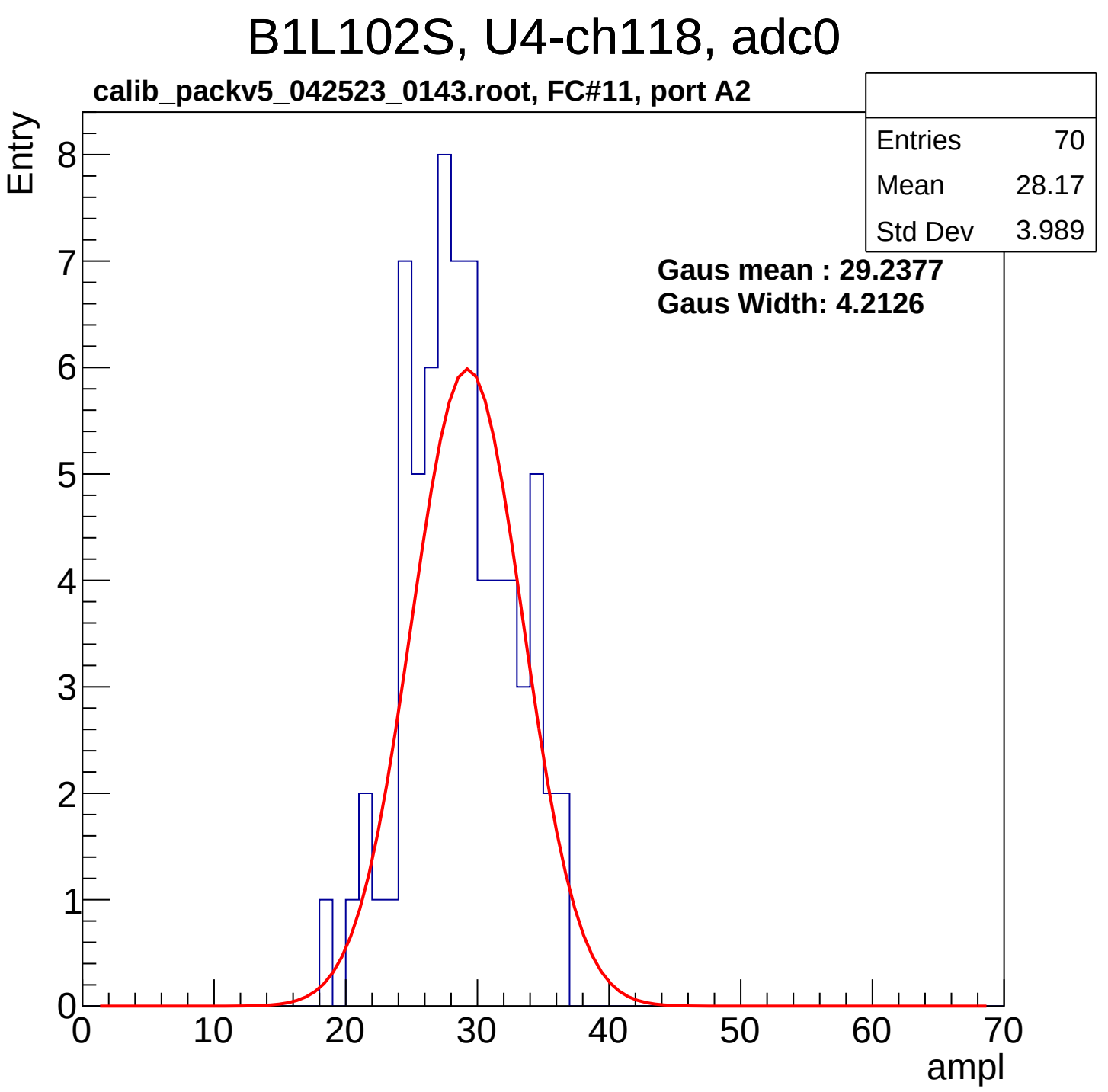

B1L102S, U4-ch117, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 57
Mean 50.98
Std Dev 3.985
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

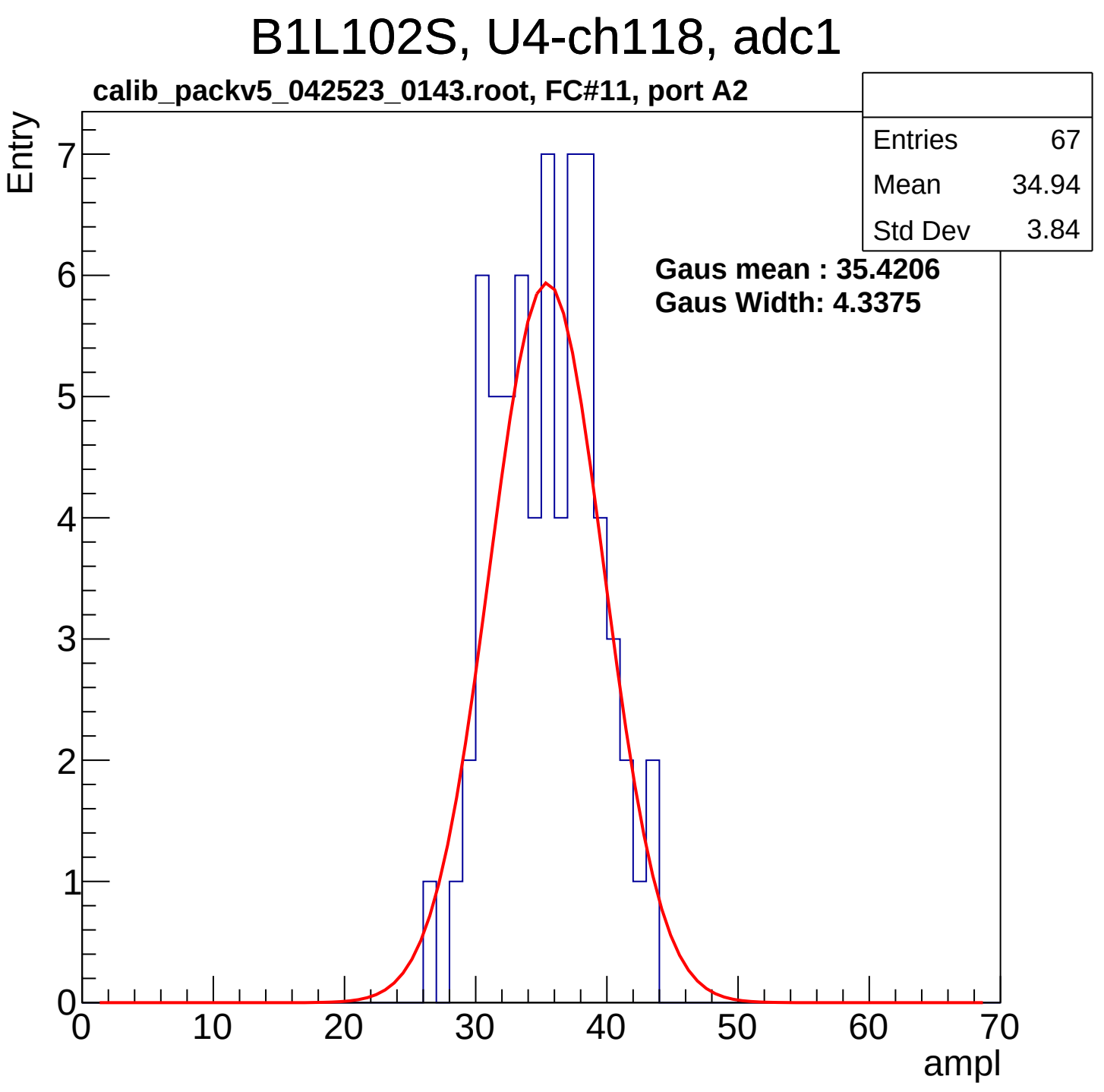

B1L102S, U4-ch117, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 57
Mean 56.23
Std Dev 3.387
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

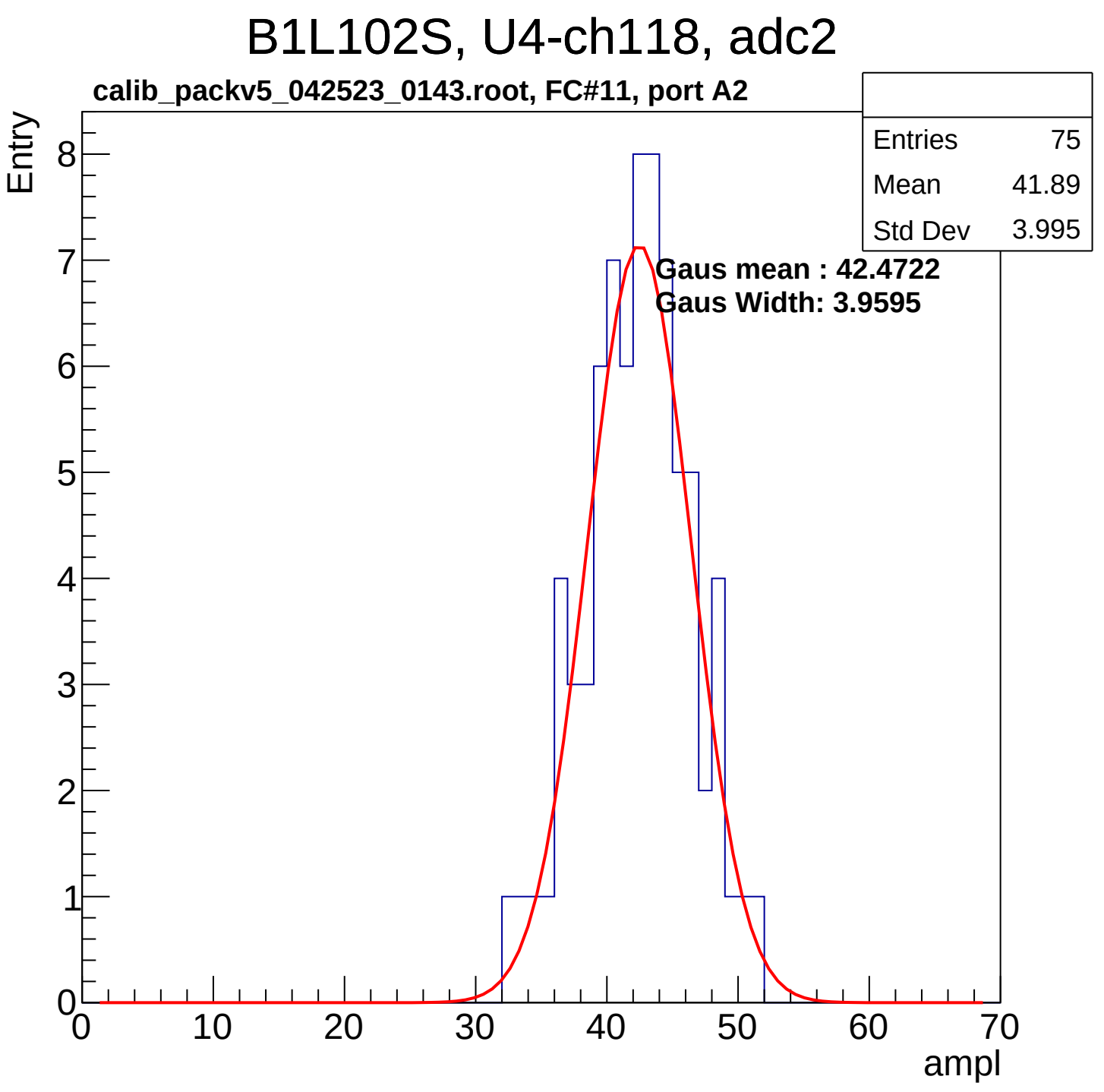

B1L102S, U4-ch117, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 36
Mean 60.58
Std Dev 1.991
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

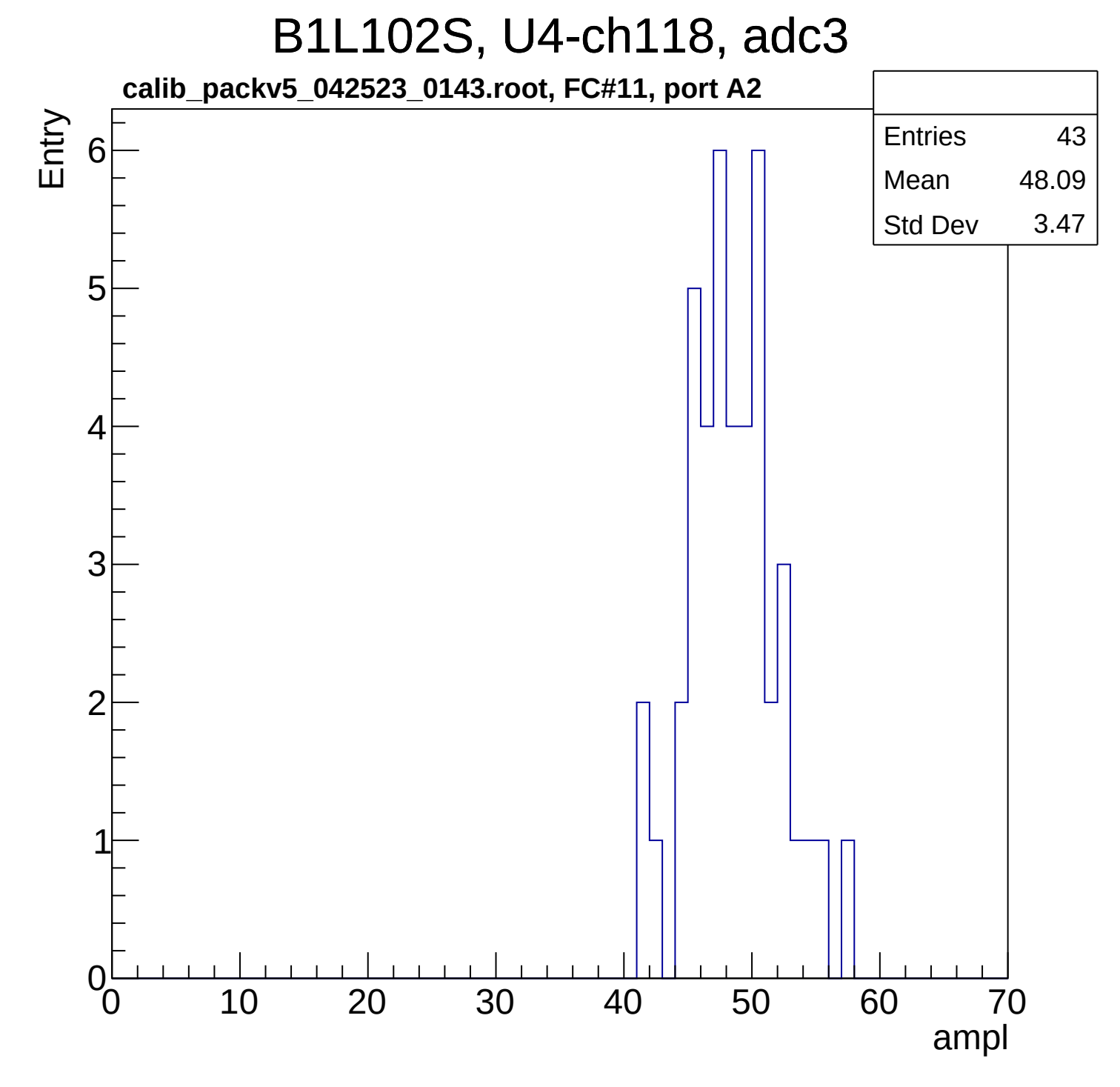

B1L102S, U4-ch117, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 4
Mean 46.75
Std Dev 26.99
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

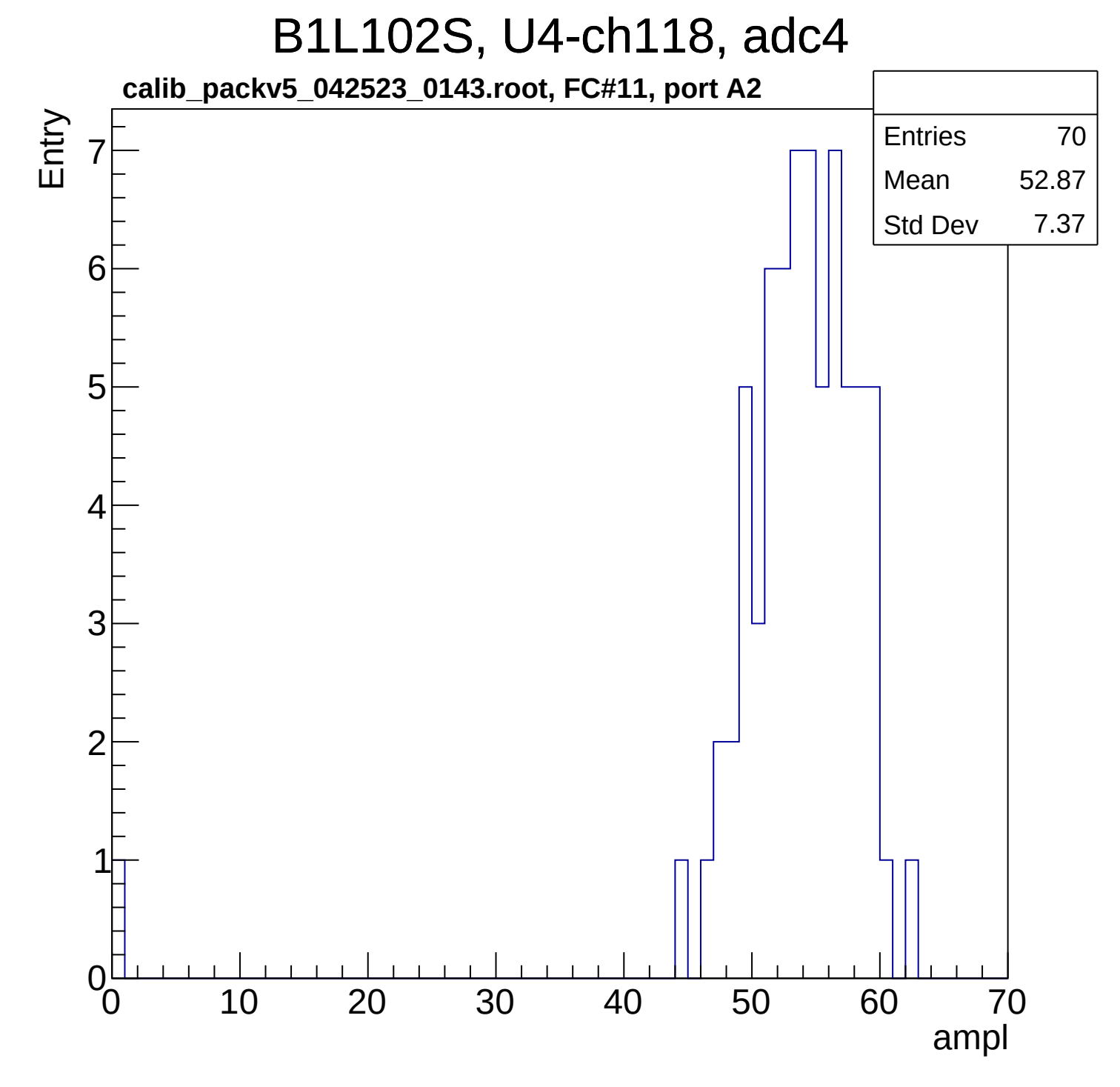

B1L102S, U4-ch117, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L102S, U4-ch118, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 28.17
Std Dev 3.989
Gaus mean : 29.2377
Gaus Width: 4.2126
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch118, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 34.94
Std Dev 3.84
Gaus mean : 35.4206
Gaus Width: 4.3375
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch118, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 41.89
Std Dev 3.995
Gaus mean : 42.4722
Gaus Width: 3.9595
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch118, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 43
Mean 48.09
Std Dev 3.47
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L102S, U4-ch118, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 70
Mean 52.87
Std Dev 7.37
Entry
ampl
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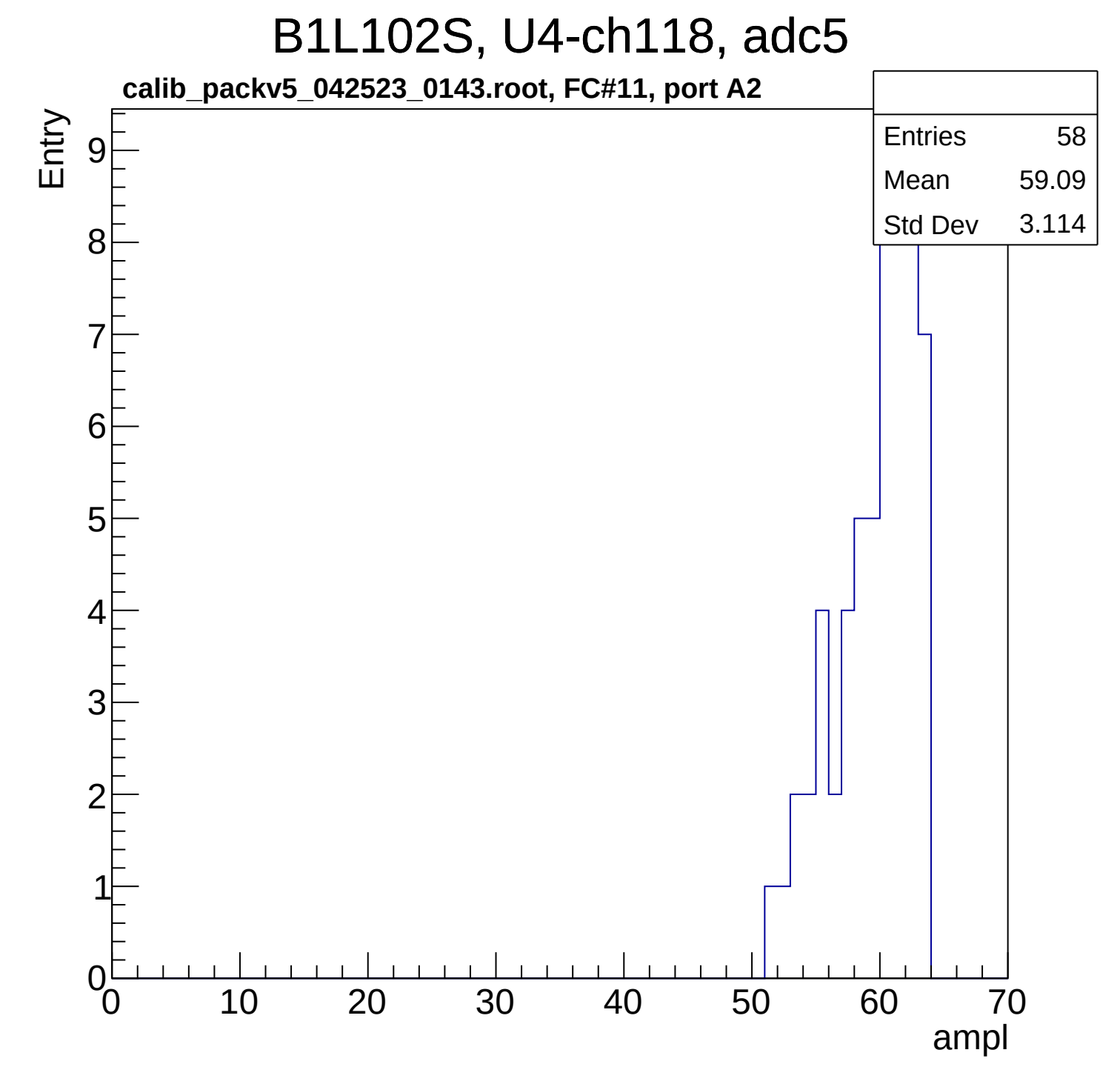
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch118, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 58
Mean 59.09
Std Dev 3.114
Entry
ampl
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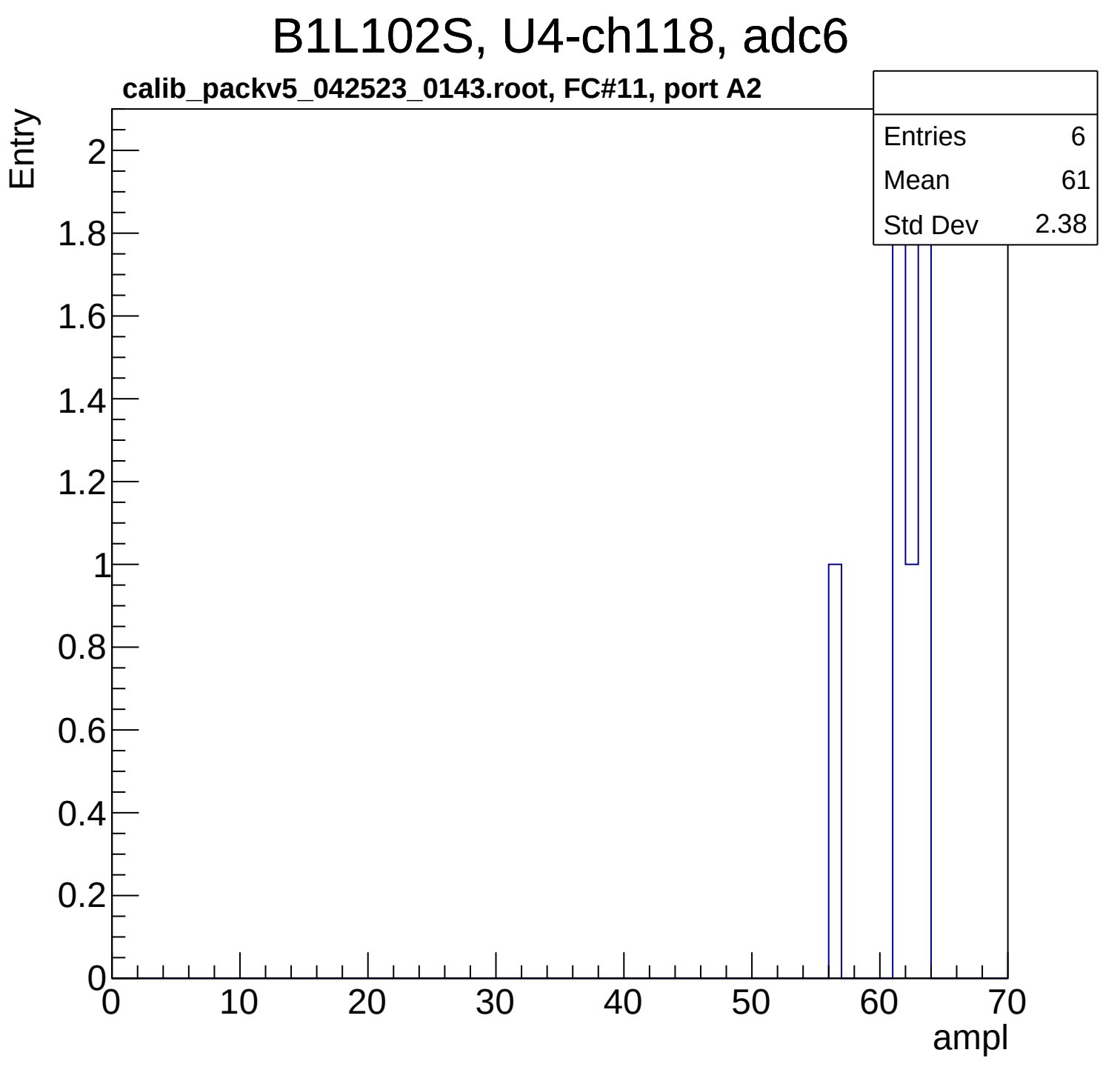
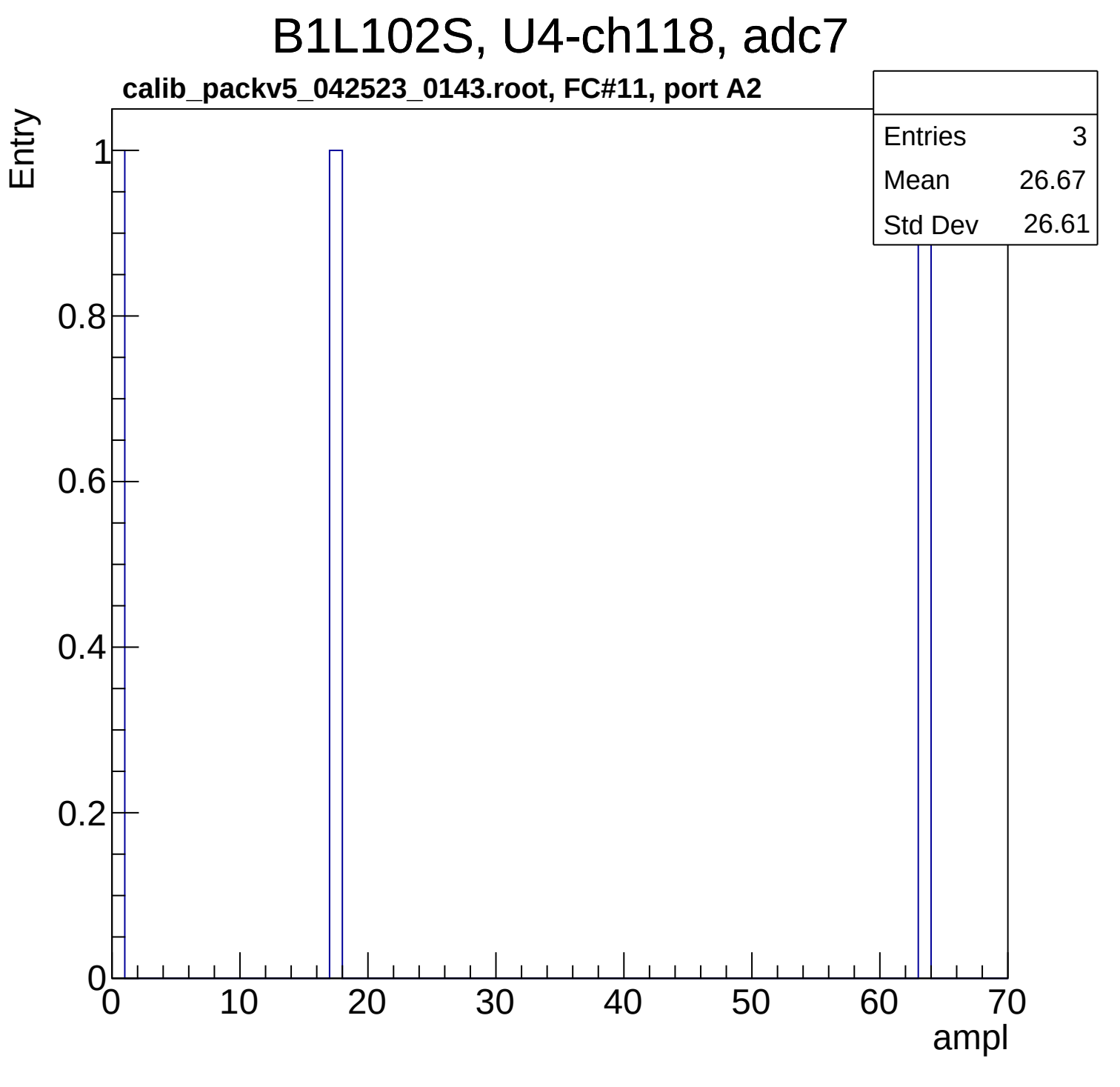
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch118, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 6
Mean 61
Std Dev 2.38
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L102S, U4-ch118, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 3
Mean 26.67
Std Dev 26.61
Entry
ampl
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0.4
0.6
0.8
1
0
10
20
30
40
50
60
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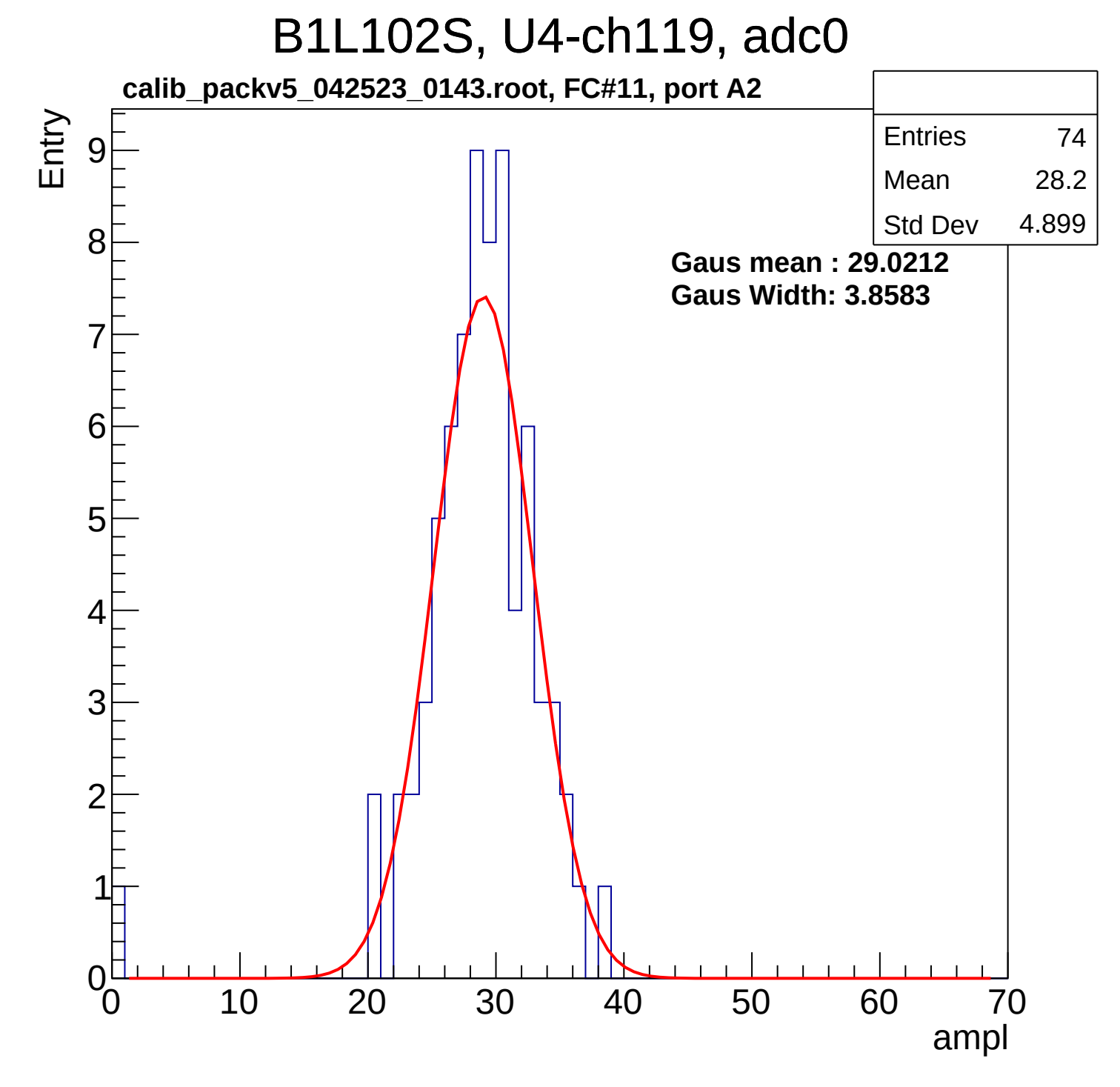
B1L102S, U4-ch119, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 74
Mean 28.2
Std Dev 4.899
Gaus mean : 29.0212
Gaus Width: 3.8583
Entry
ampl
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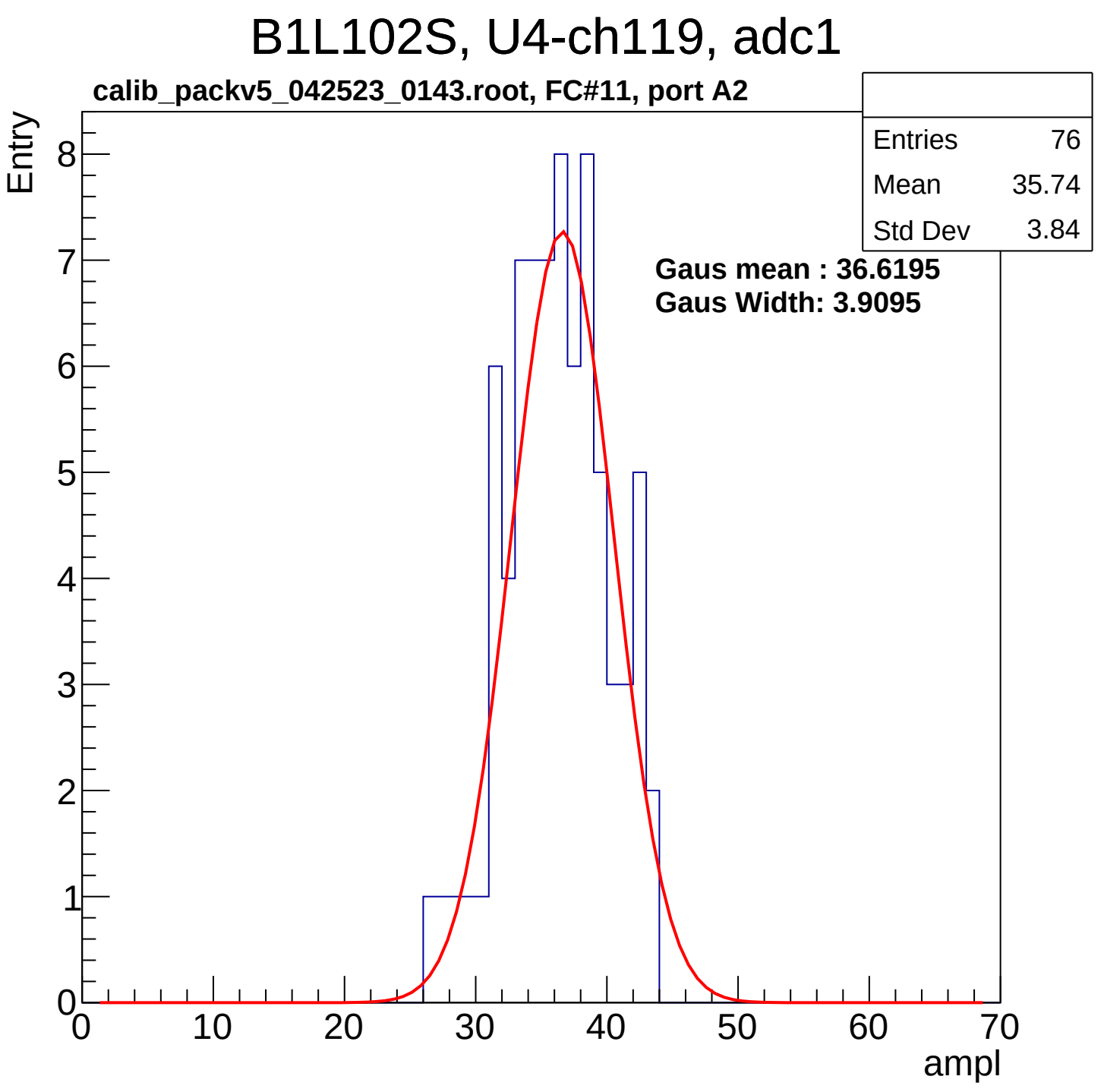
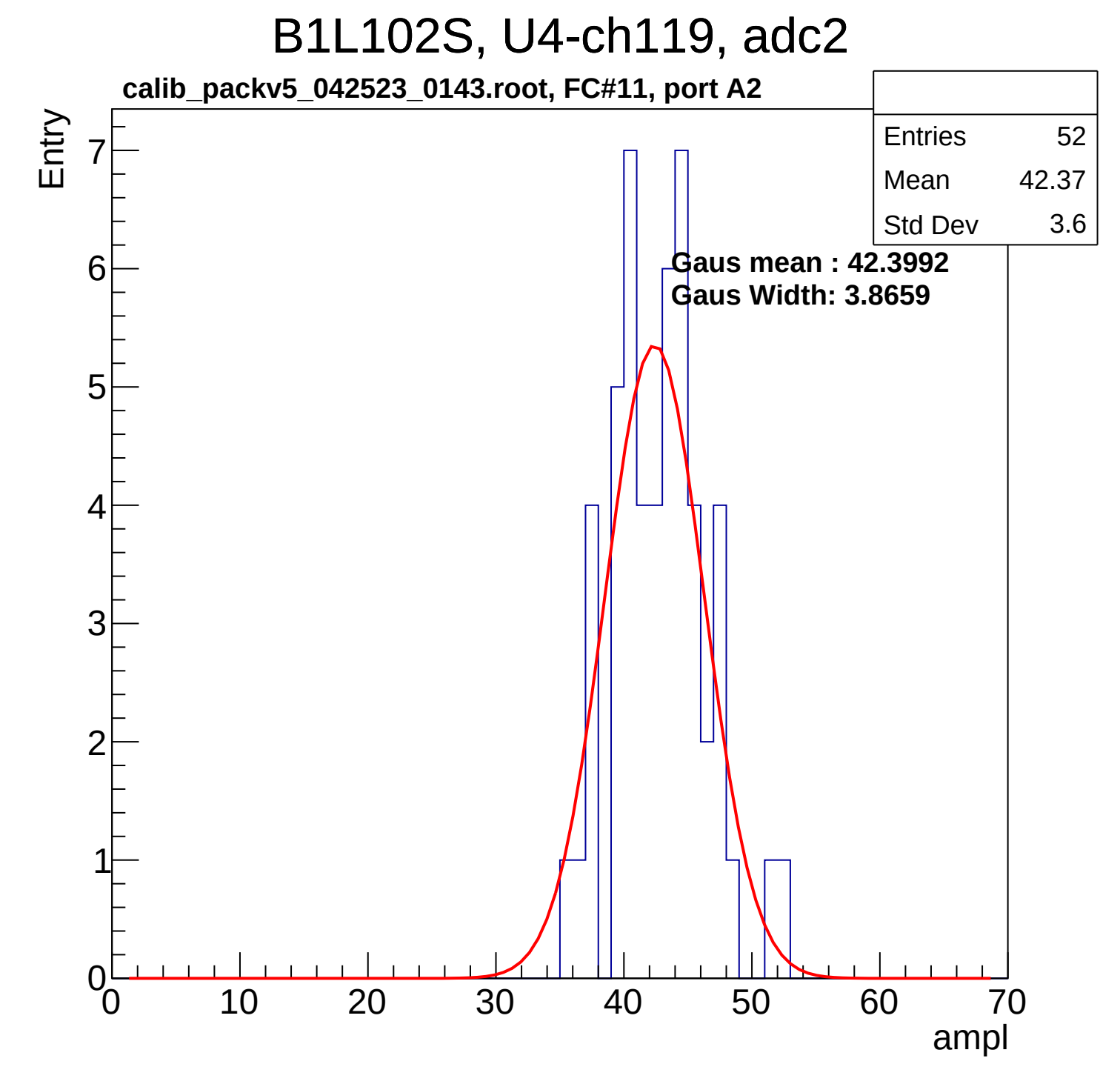
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L102S, U4-ch119, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 35.74
Std Dev 3.84
Gaus mean : 36.6195
Gaus Width: 3.9095
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch119, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 52
Mean 42.37
Std Dev 3.6
Gaus mean : 42.3992
Gaus Width: 3.8659
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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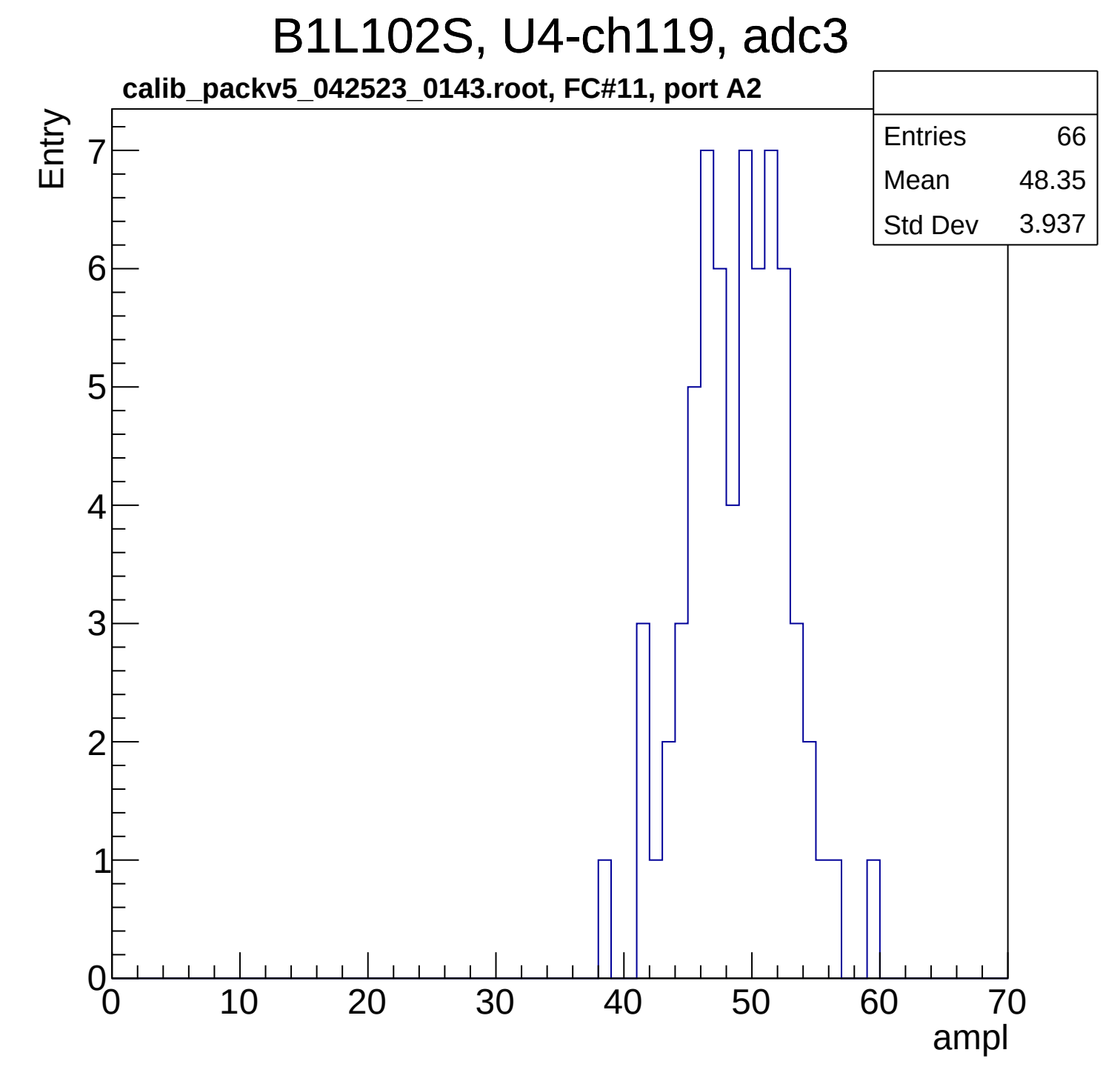
B1L102S, U4-ch119, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 48.35
Std Dev 3.937
Entry
ampl
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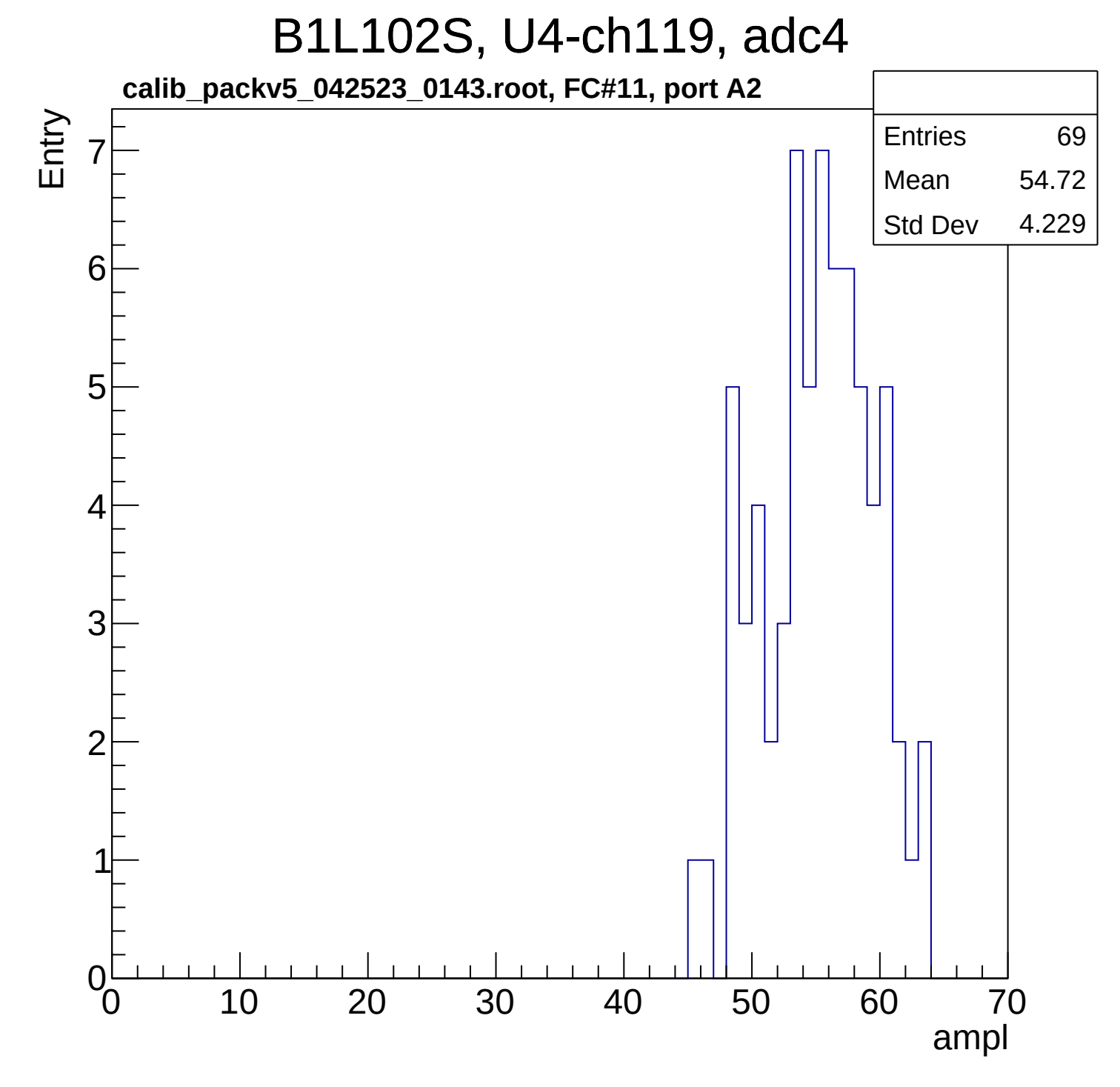
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch119, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 54.72
Std Dev 4.229
Entry
ampl
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1
2
3
4
5
6
7
0
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20
30
40
50
60
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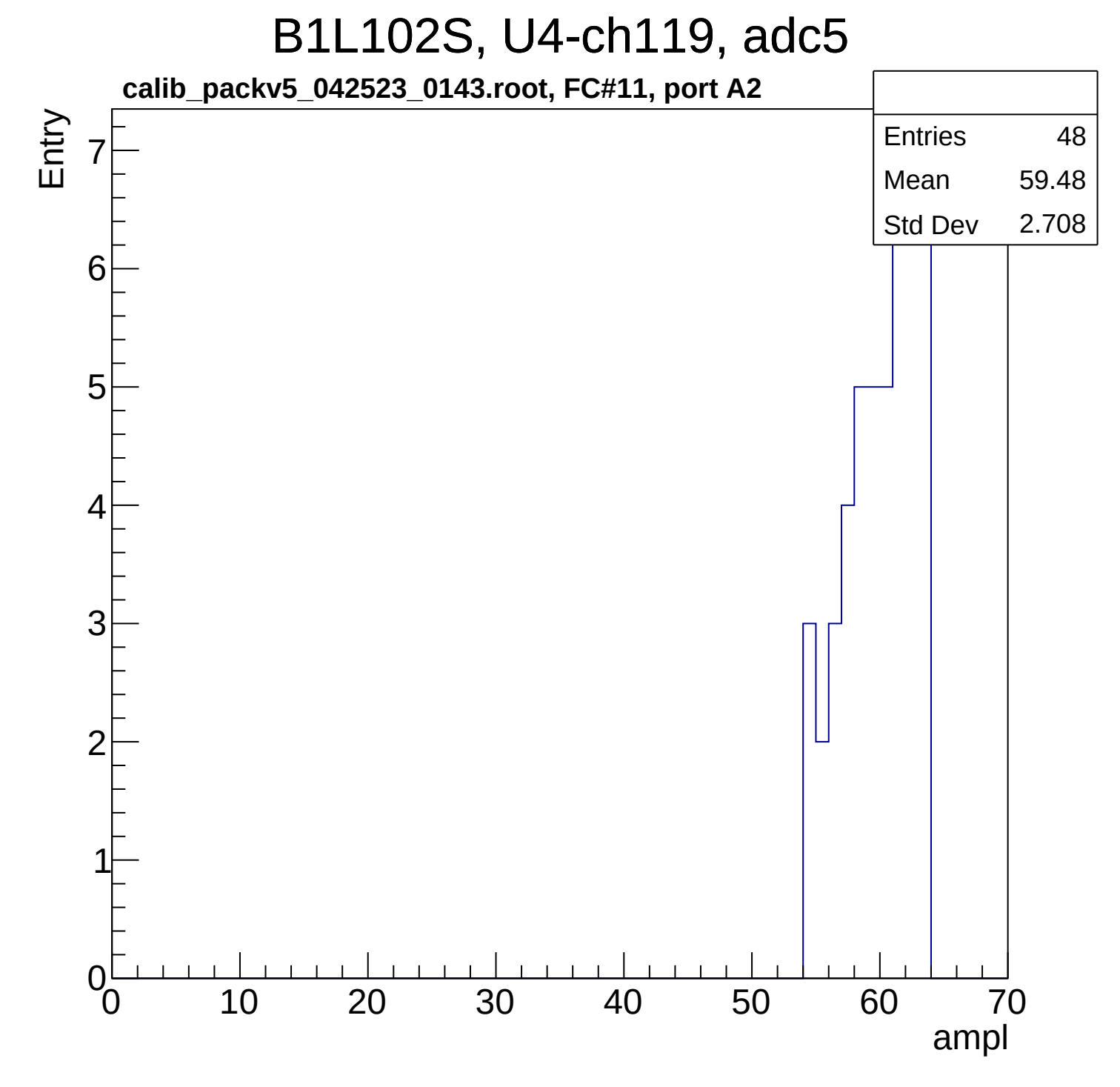
B1L102S, U4-ch119, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 48
Mean 59.48
Std Dev 2.708
Entry
ampl
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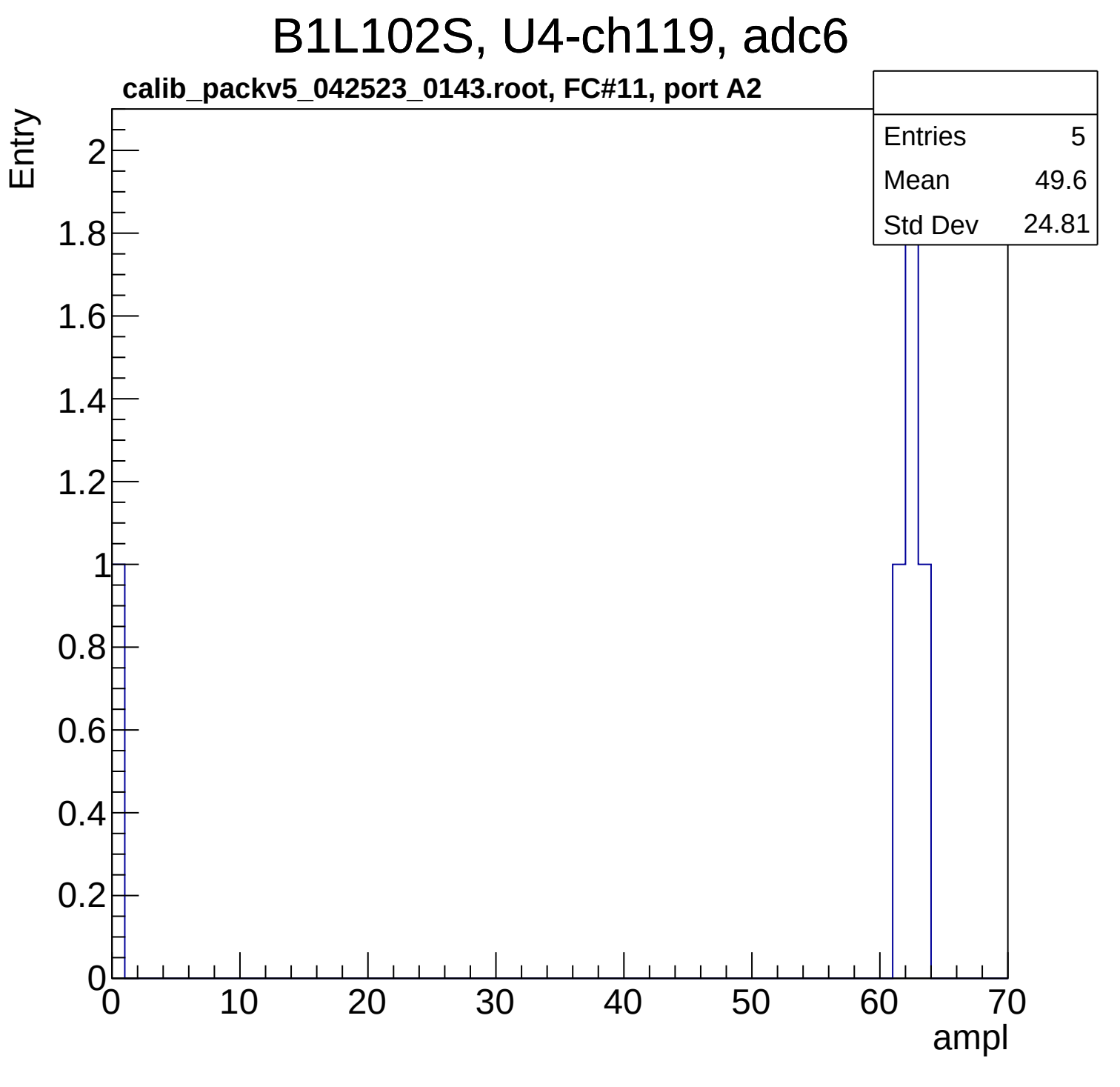
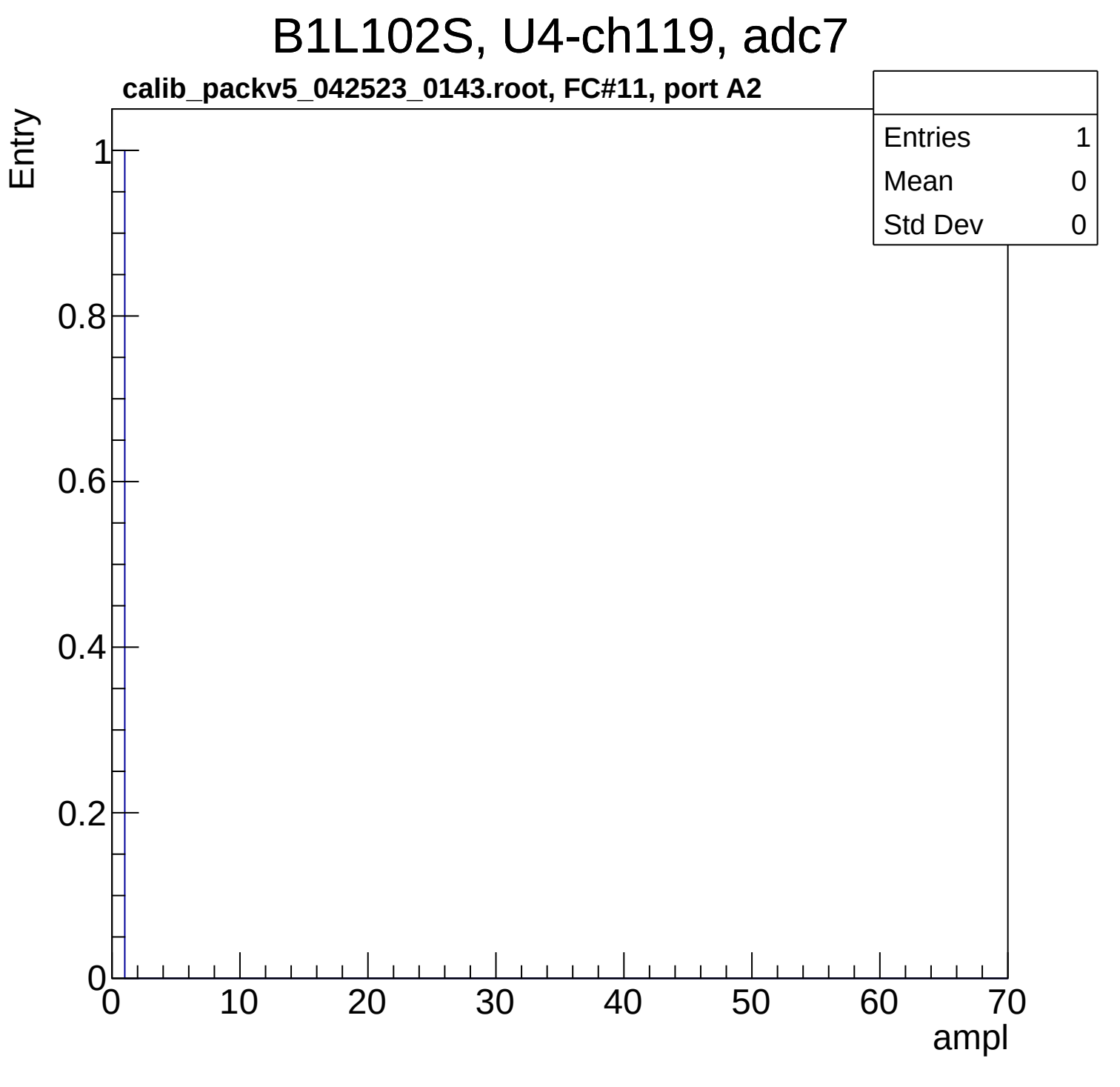
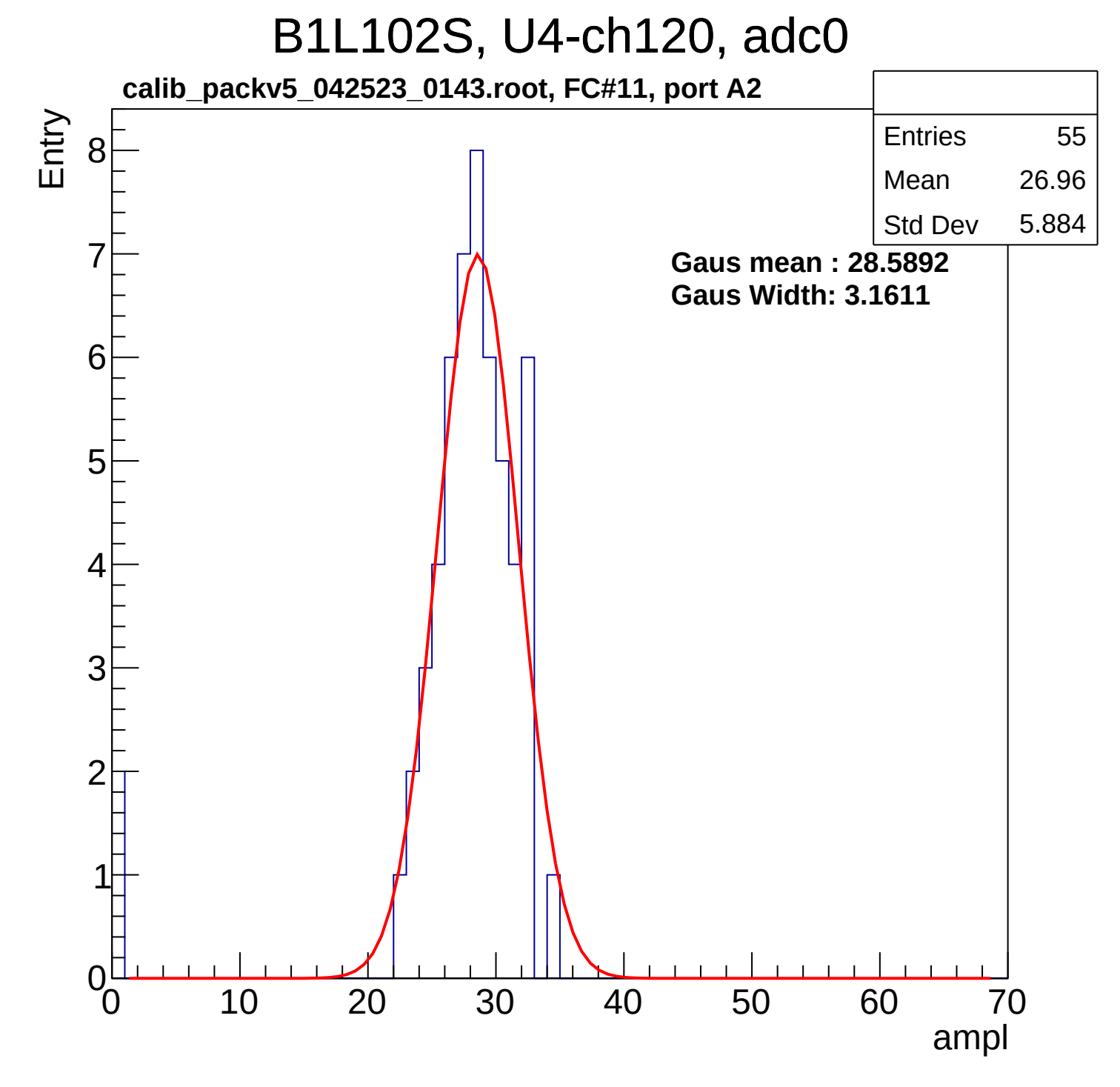
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch119, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 5
Mean 49.6
Std Dev 24.81
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L102S, U4-ch119, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch120, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 26.96
Std Dev 5.884
Gaus mean : 28.5892
Gaus Width: 3.1611
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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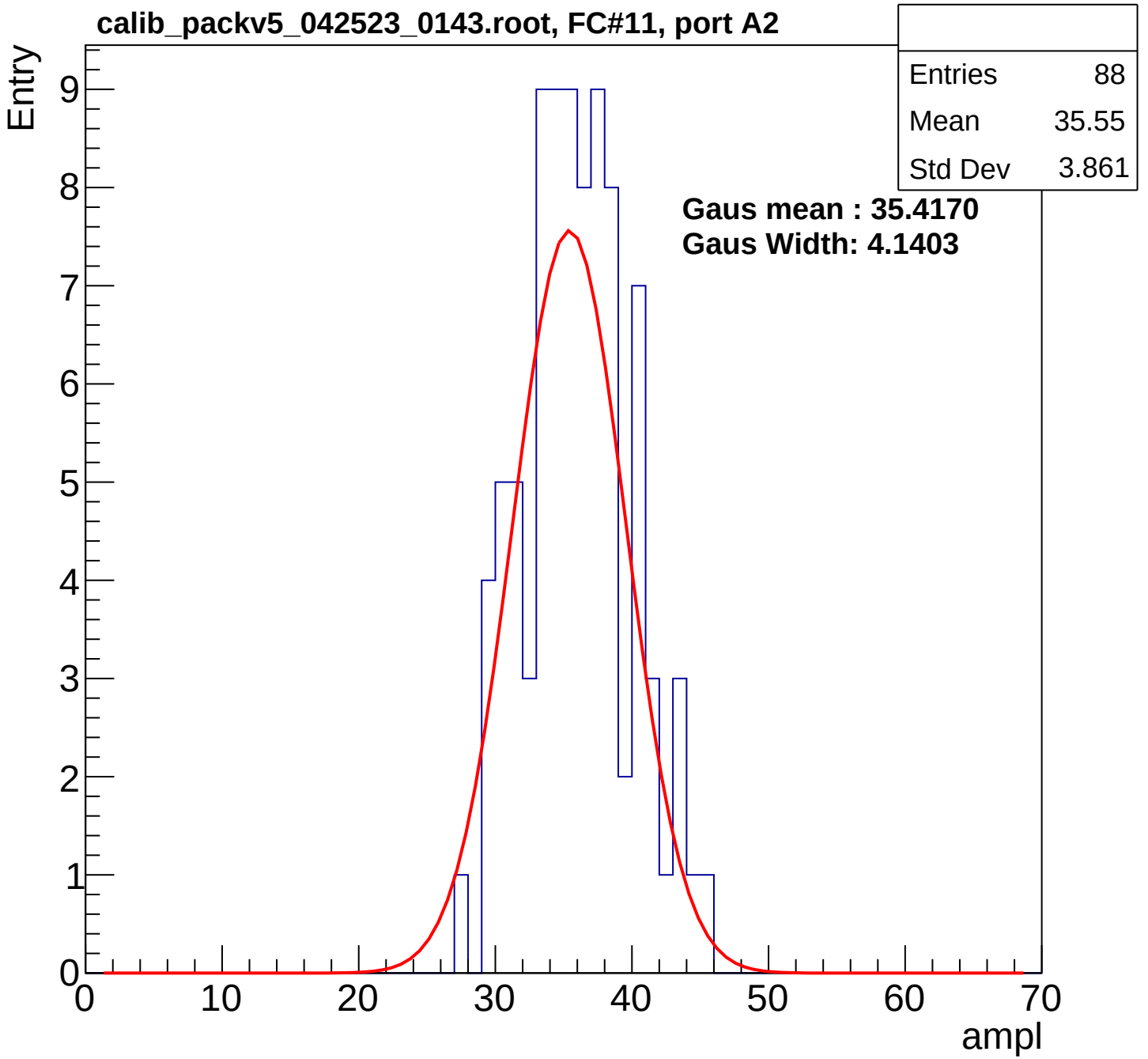
B1L102S, U4-ch120, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 88
Mean 35.55
Std Dev 3.861
Gaus mean : 35.4170
Gaus Width: 4.1403
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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60
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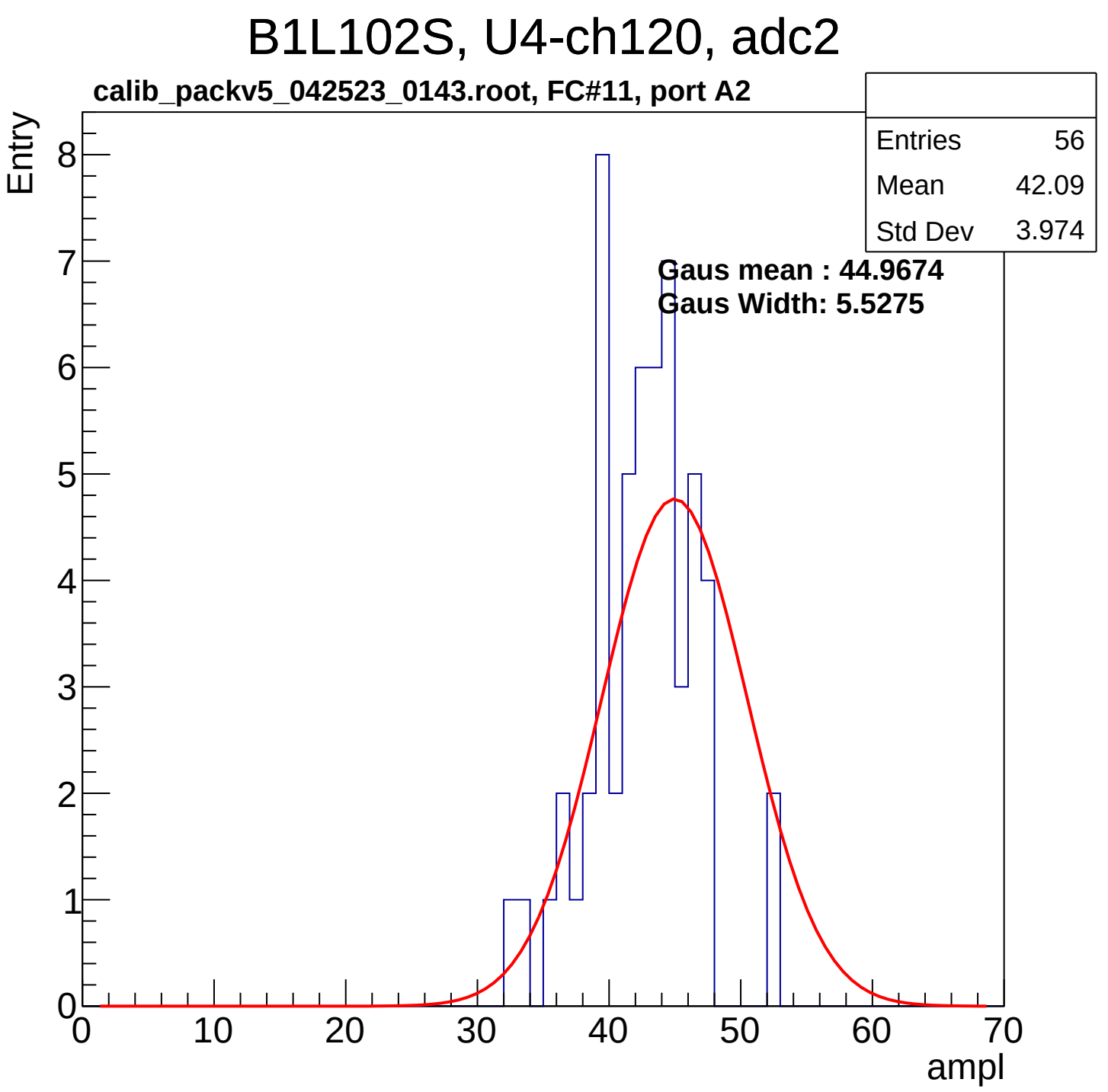
B1L102S, U4-ch120, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 42.09
Std Dev 3.974
Gaus mean : 44.9674
Gaus Width: 5.5275
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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40
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60
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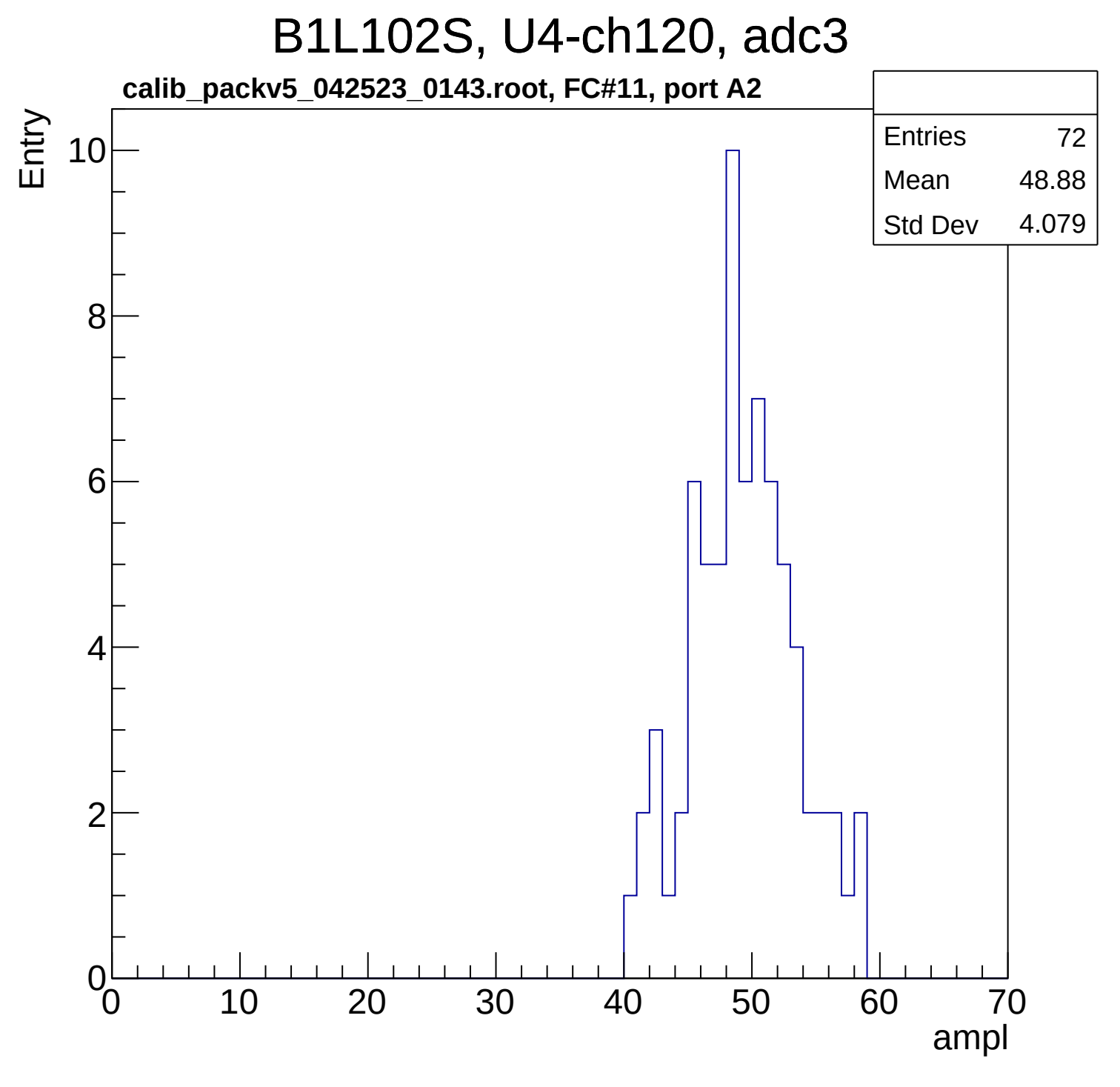
B1L102S, U4-ch120, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 72
Mean 48.88
Std Dev 4.079
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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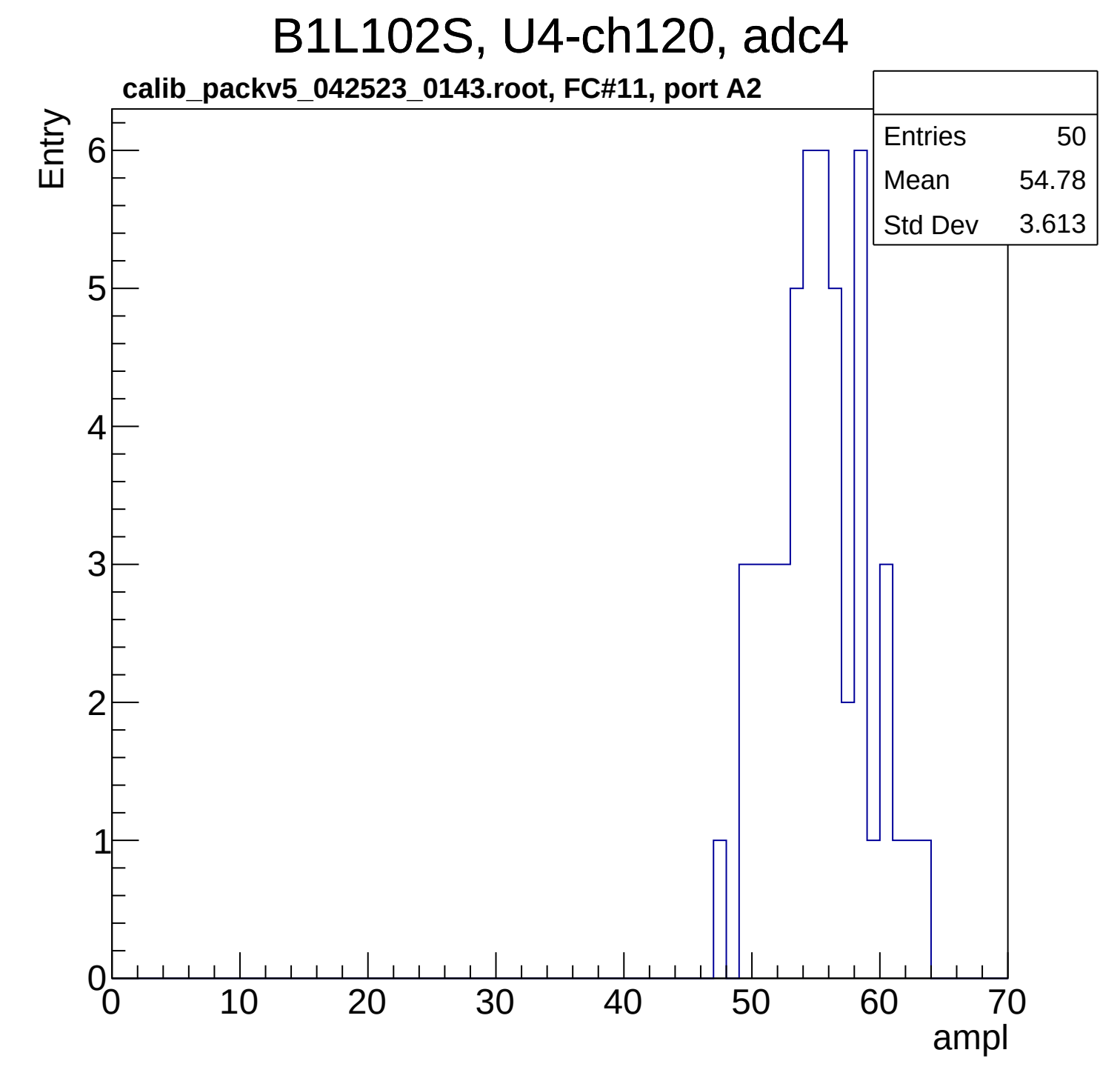
B1L102S, U4-ch120, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 50
Mean 54.78
Std Dev 3.613
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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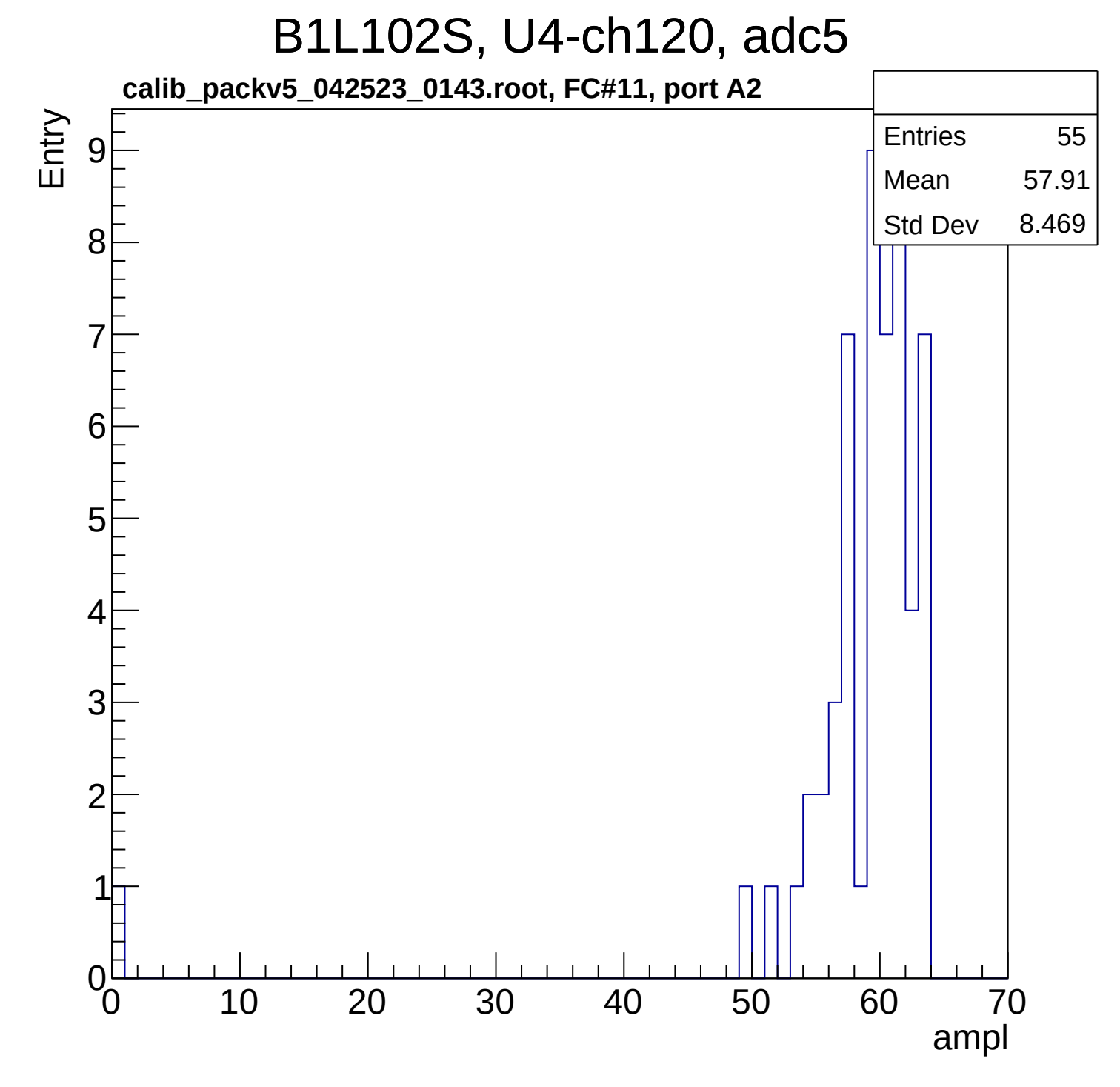
B1L102S, U4-ch120, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 55
Mean 57.91
Std Dev 8.469
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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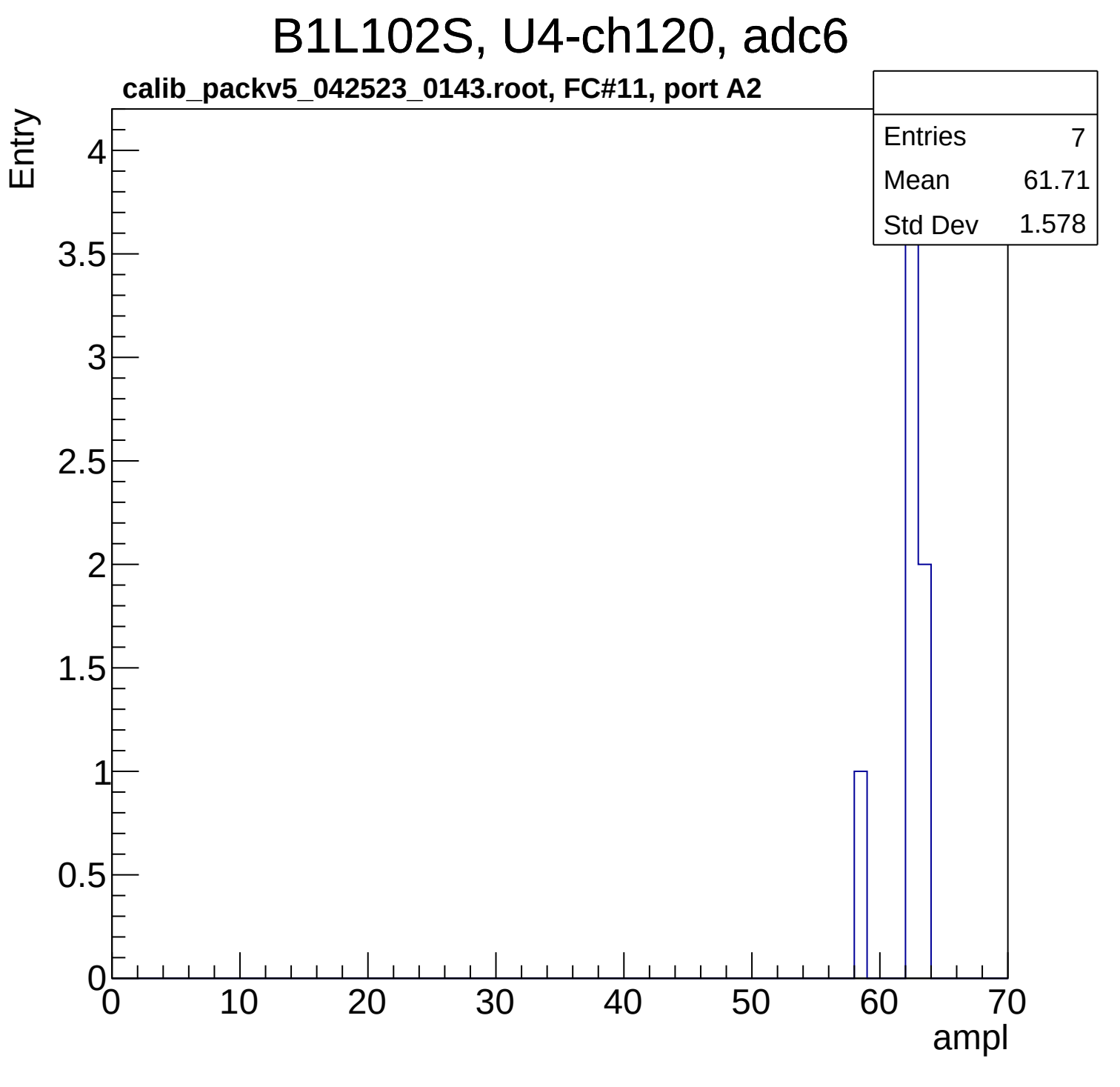
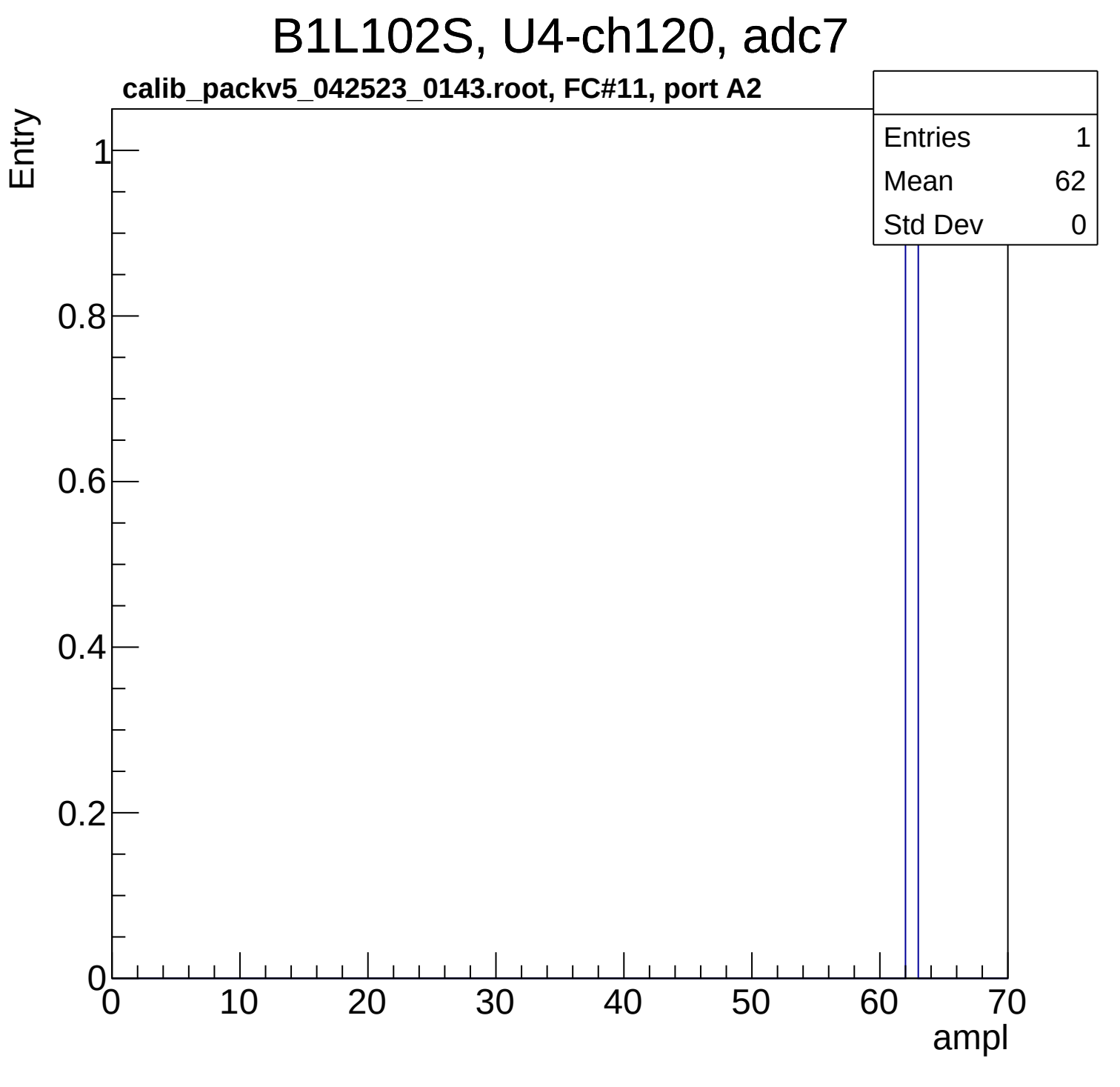

B1L102S, U4-ch120, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 7
Mean 61.71
Std Dev 1.578
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U4-ch120, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 62
Std Dev 0
Entry
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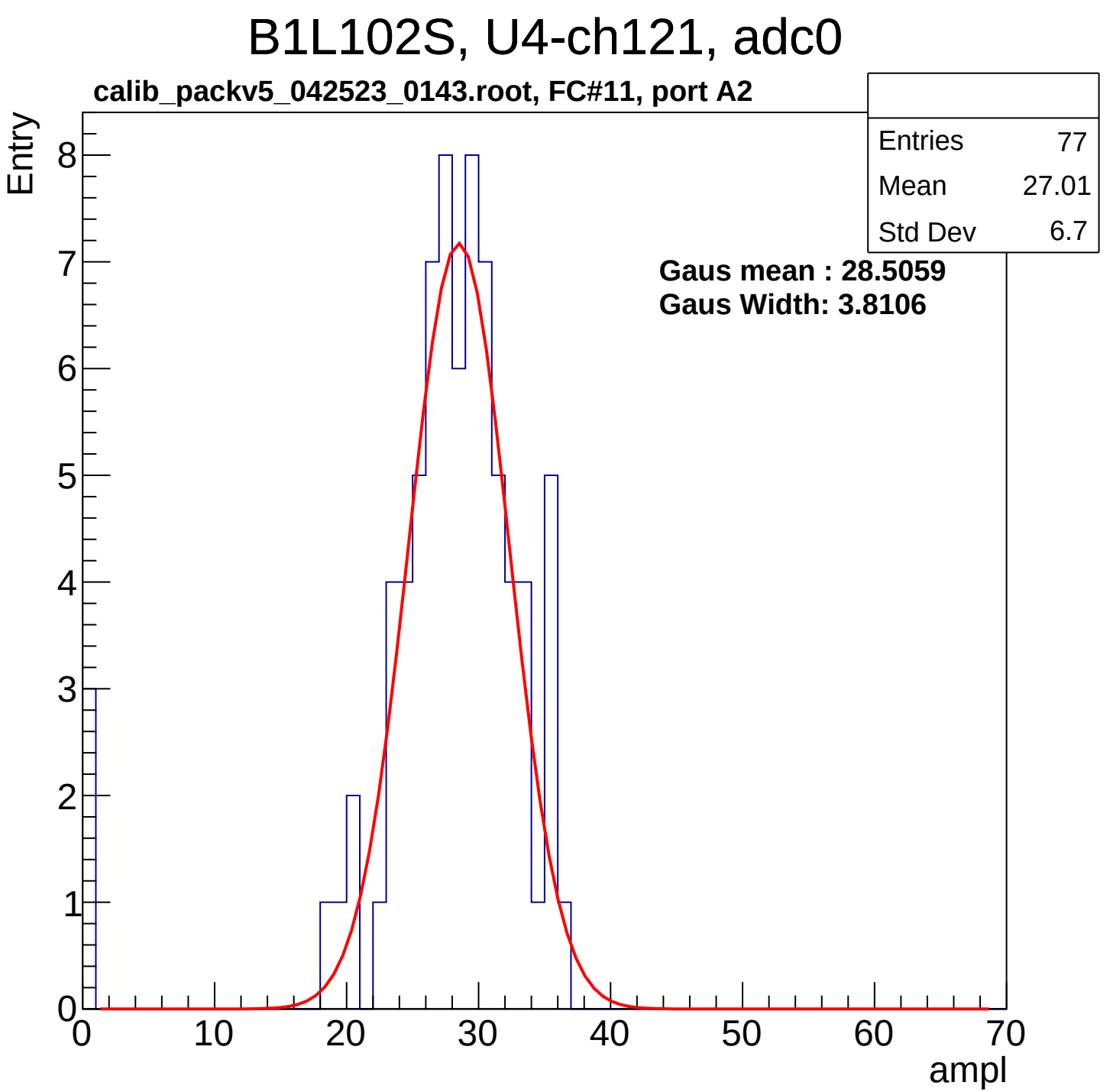
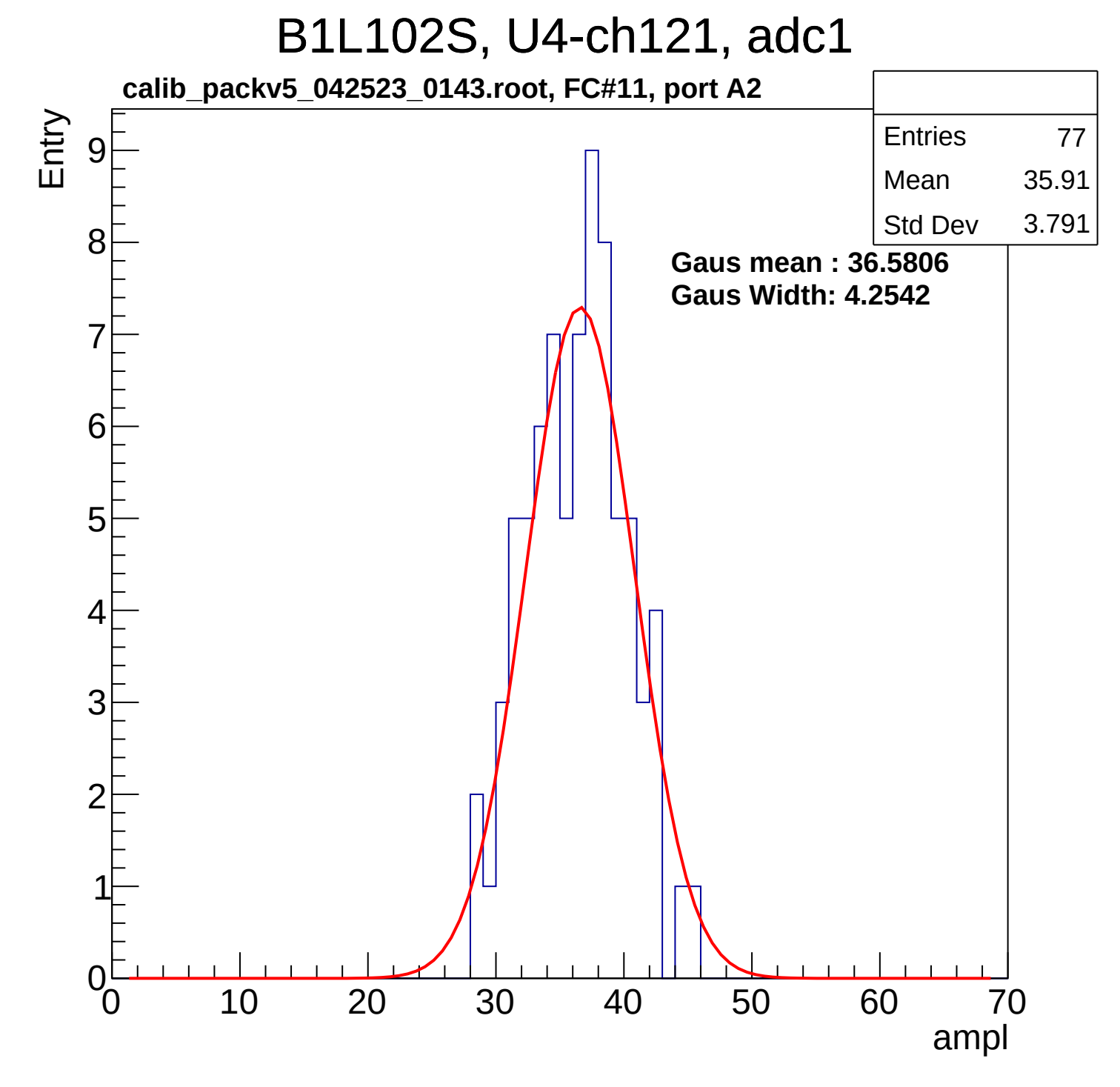
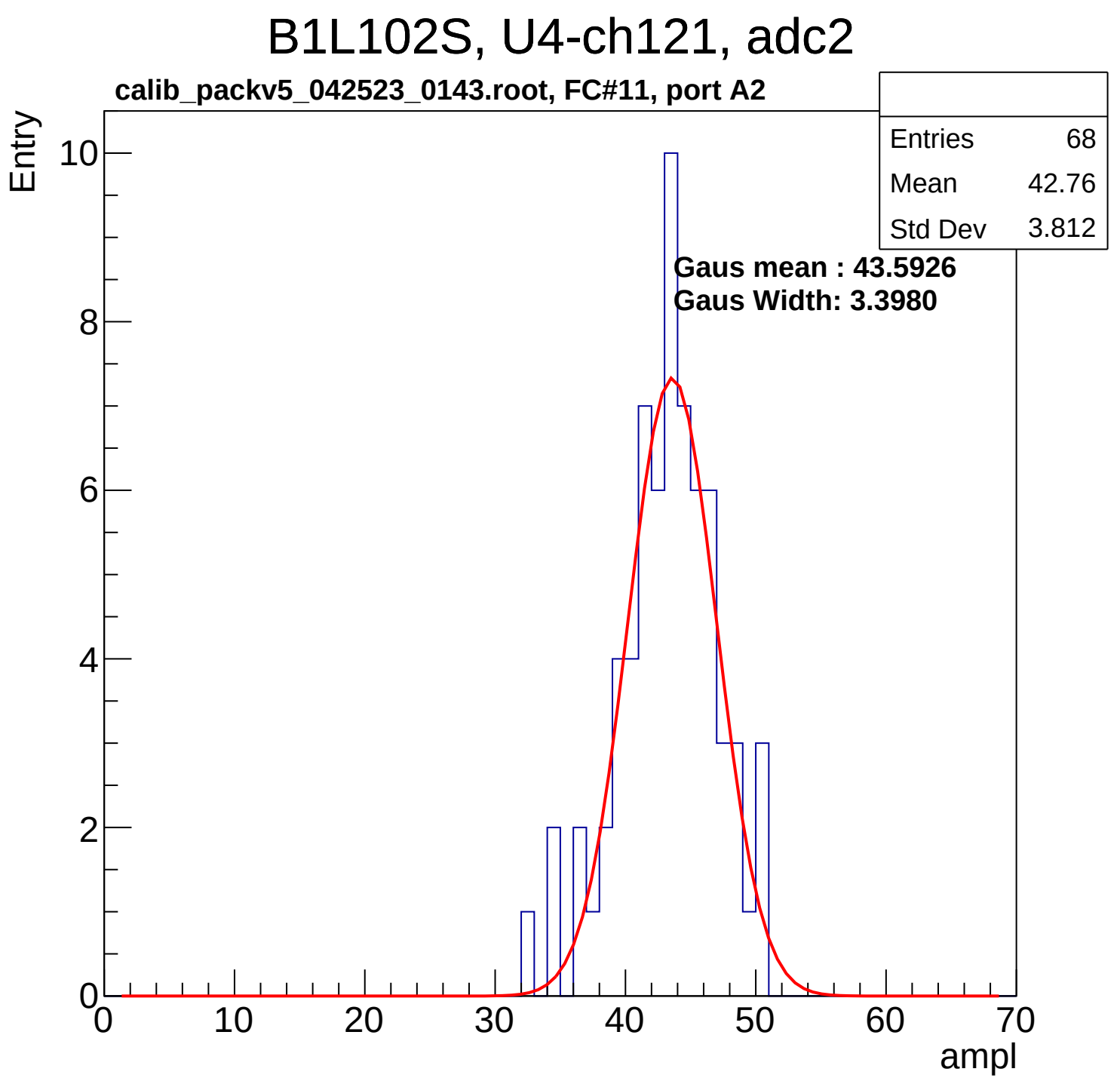
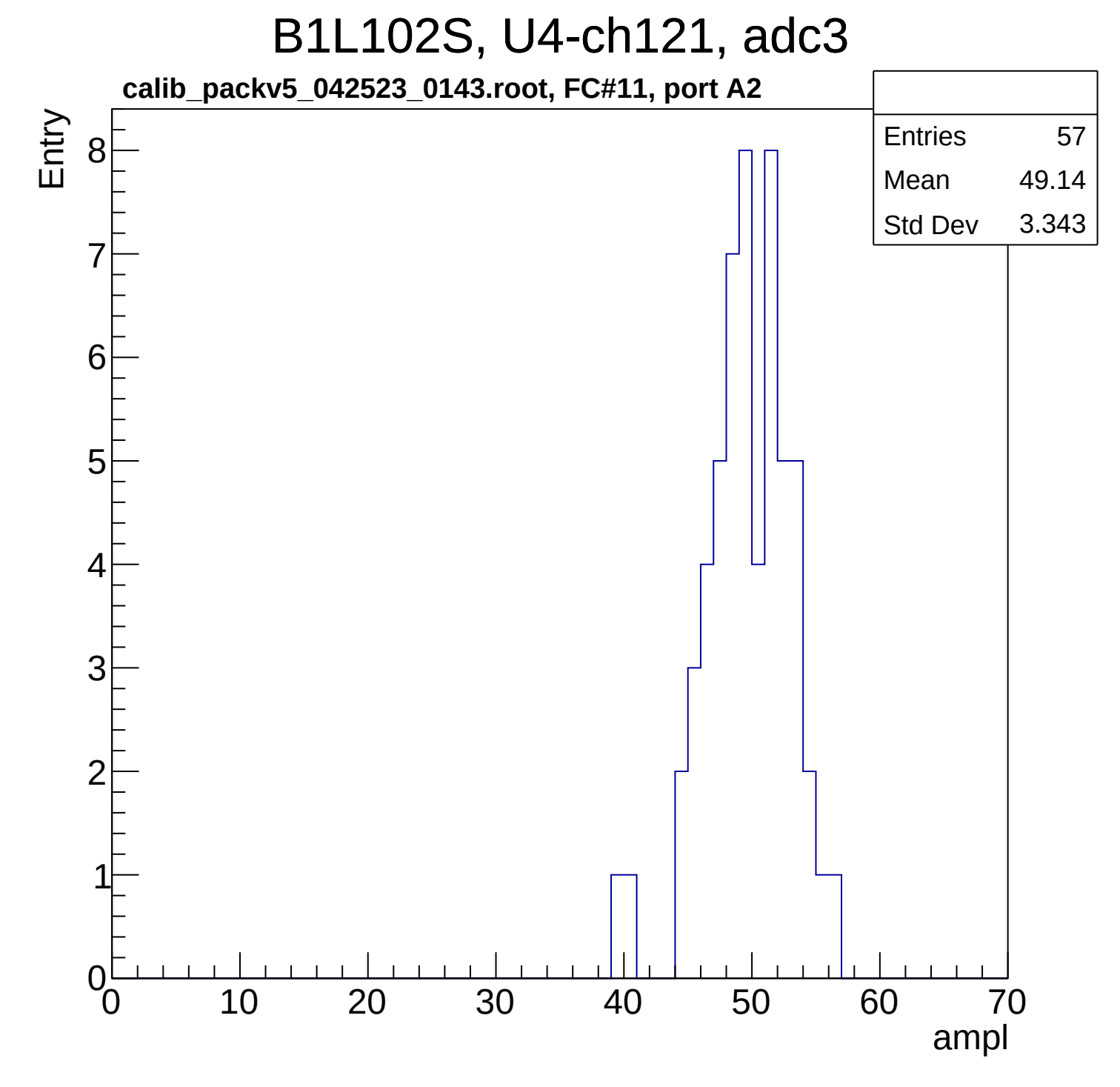
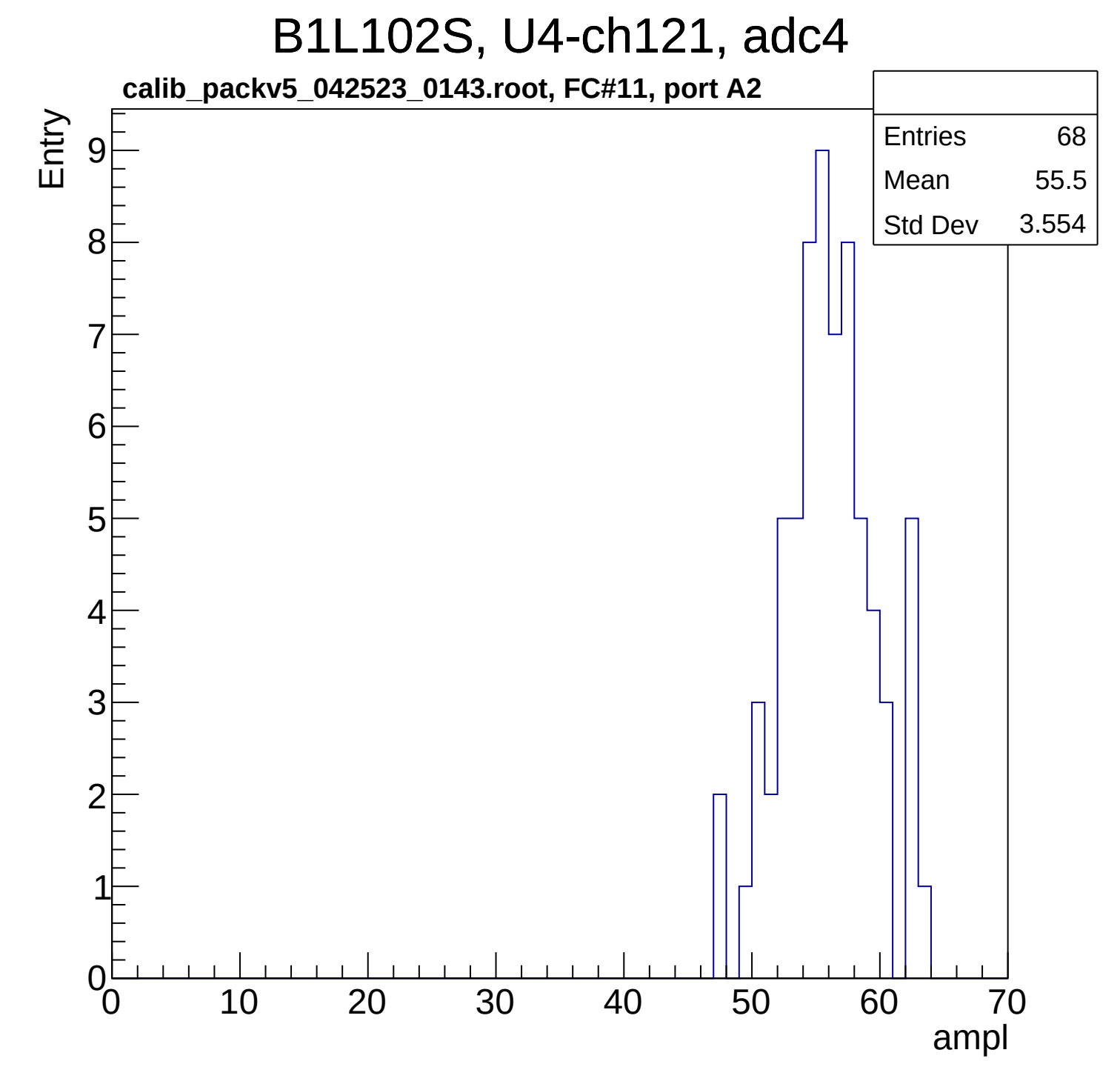
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

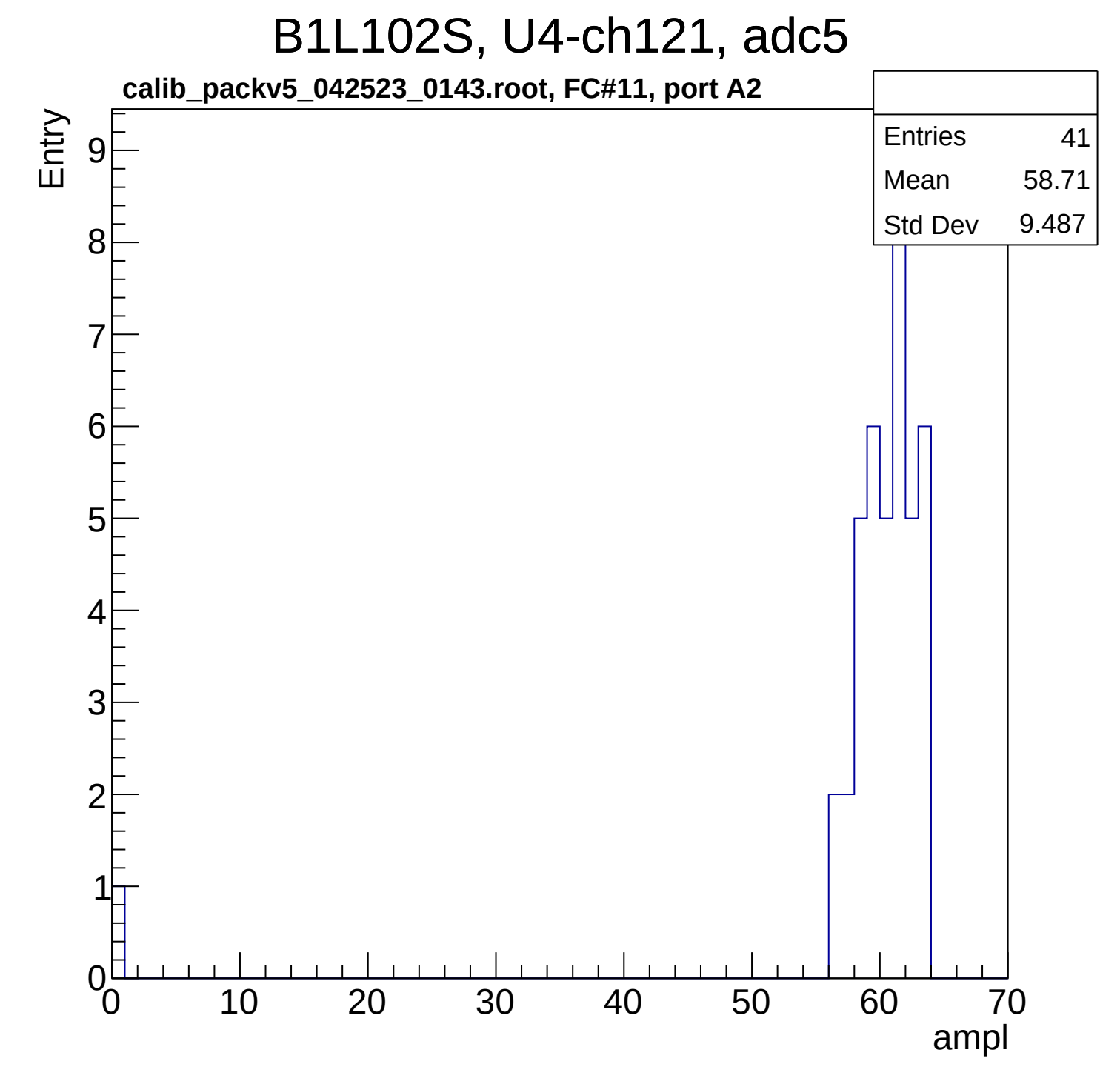

B1L102S, U4-ch121, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 77
Mean 27.01
Std Dev 6.7
Gaus mean : 28.5059
Gaus Width: 3.8106
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch121, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 77
Mean 35.91
Std Dev 3.791
Gaus mean : 36.5806
Gaus Width: 4.2542
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch121, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 42.76
Std Dev 3.812
Gaus mean : 43.5926
Gaus Width: 3.3980
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch121, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 57
Mean 49.14
Std Dev 3.343
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch121, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 55.5
Std Dev 3.554
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch121, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 41
Mean 58.71
Std Dev 9.487
Entry
ampl
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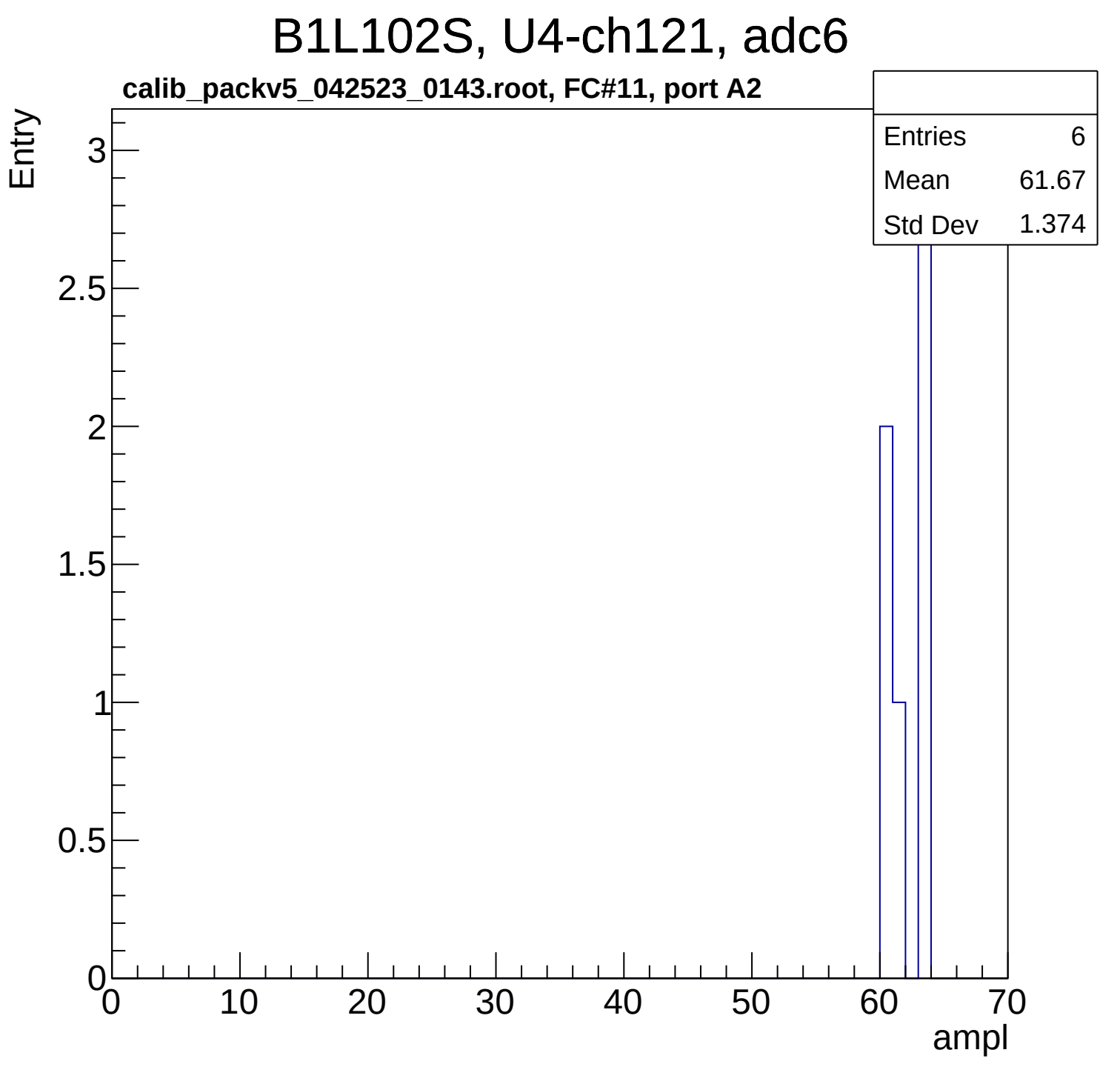
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch121, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 6
Mean 61.67
Std Dev 1.374
Entry
ampl
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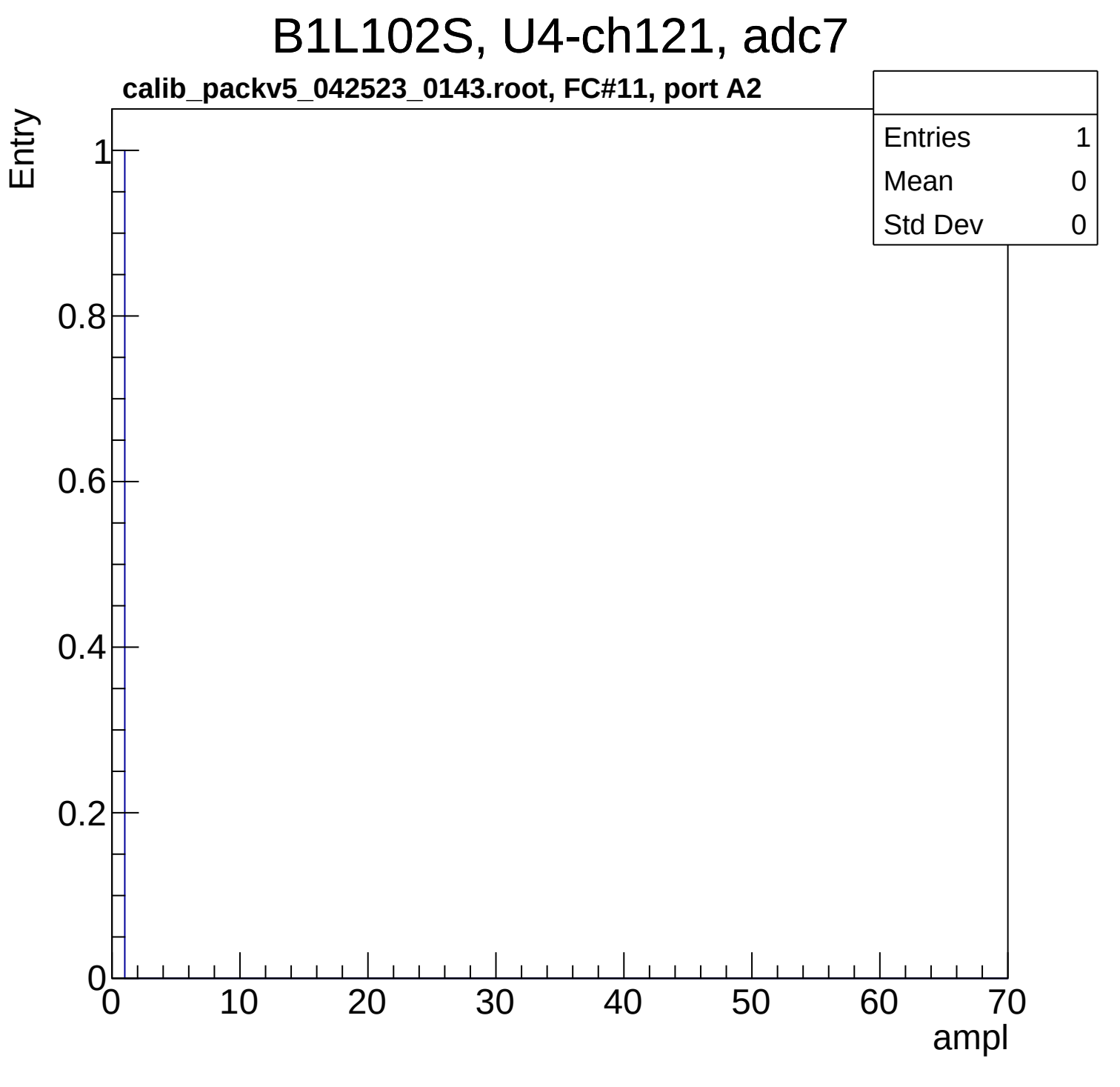
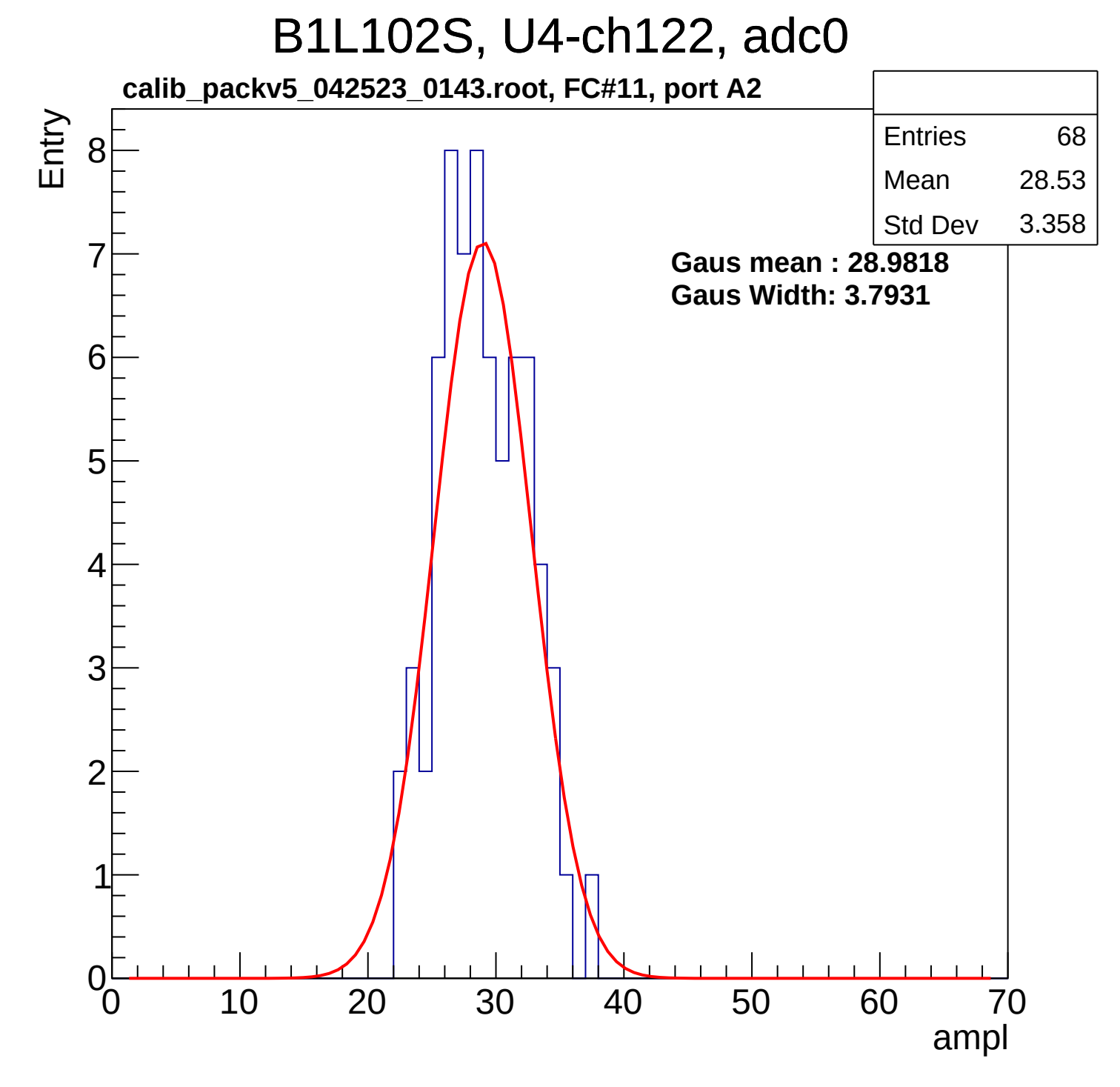
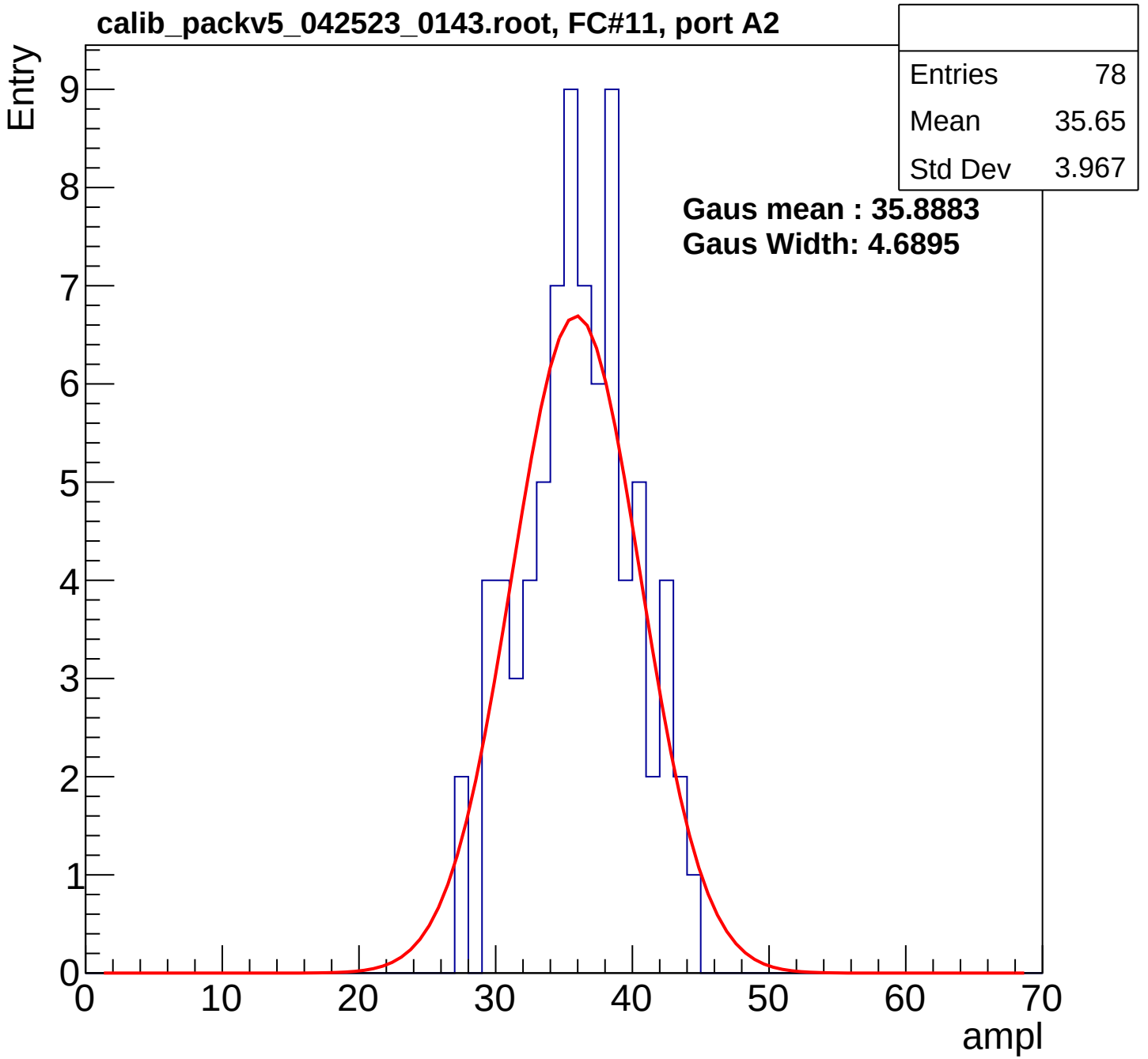
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U4-ch121, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch122, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 68
Mean 28.53
Std Dev 3.358
Gaus mean : 28.9818
Gaus Width: 3.7931
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch122, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 78
Mean 35.65
Std Dev 3.967
Gaus mean : 35.8883
Gaus Width: 4.6895
Entry
ampl
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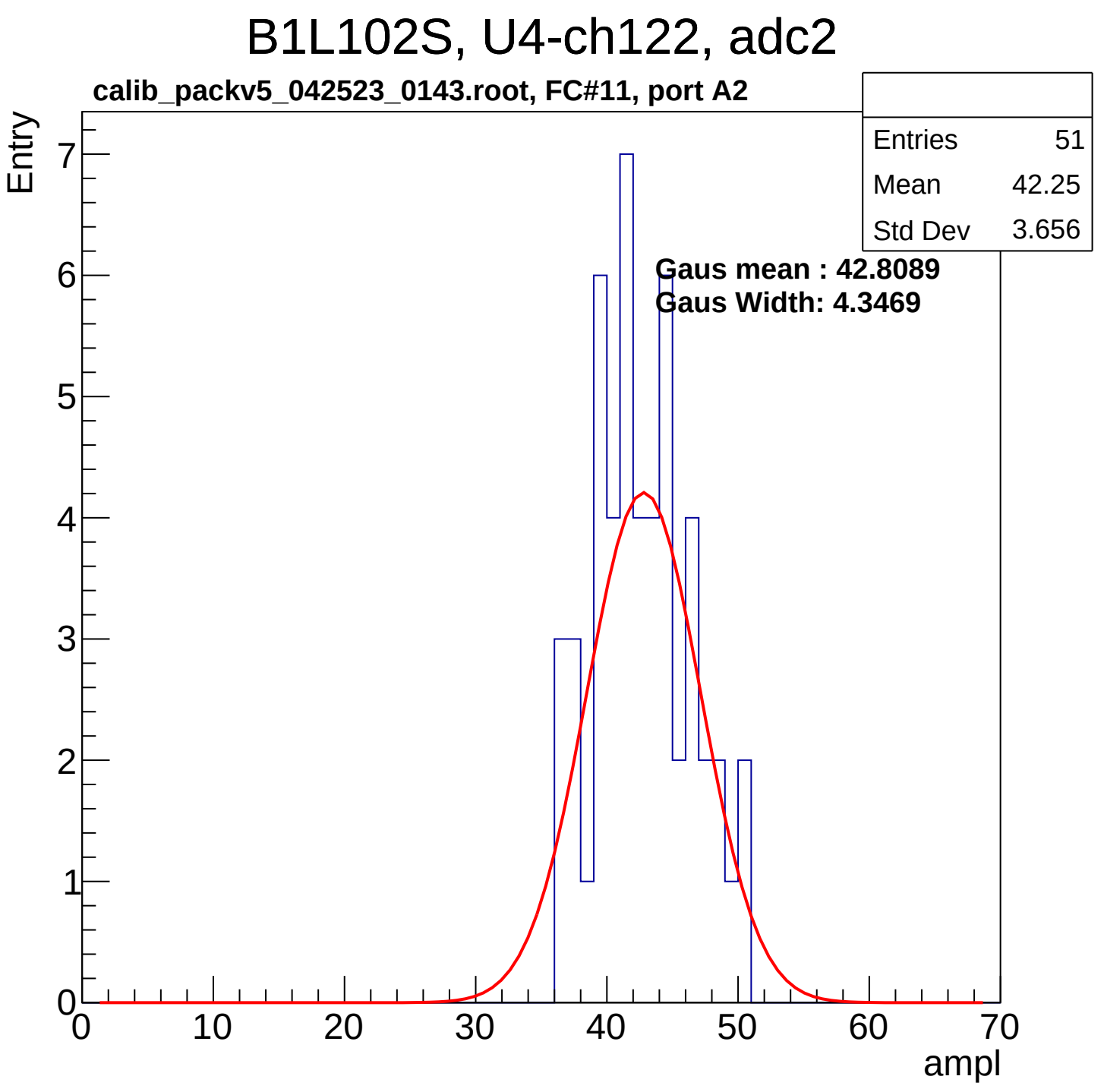
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch122, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 51
Mean 42.25
Std Dev 3.656
Gaus mean : 42.8089
Gaus Width: 4.3469
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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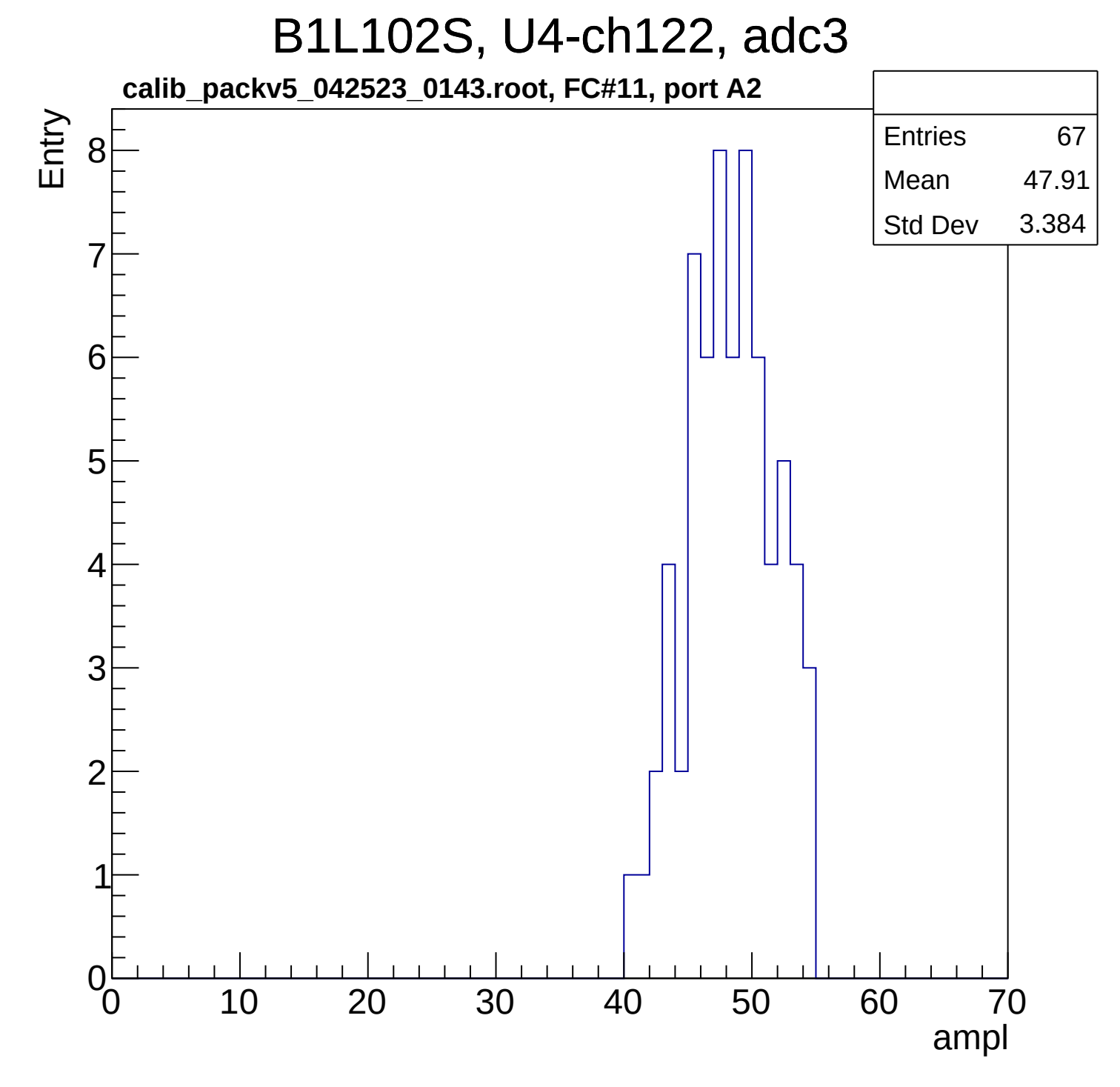
40
50
60
70


B1L102S, U4-ch122, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 67
Mean 47.91
Std Dev 3.384
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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60
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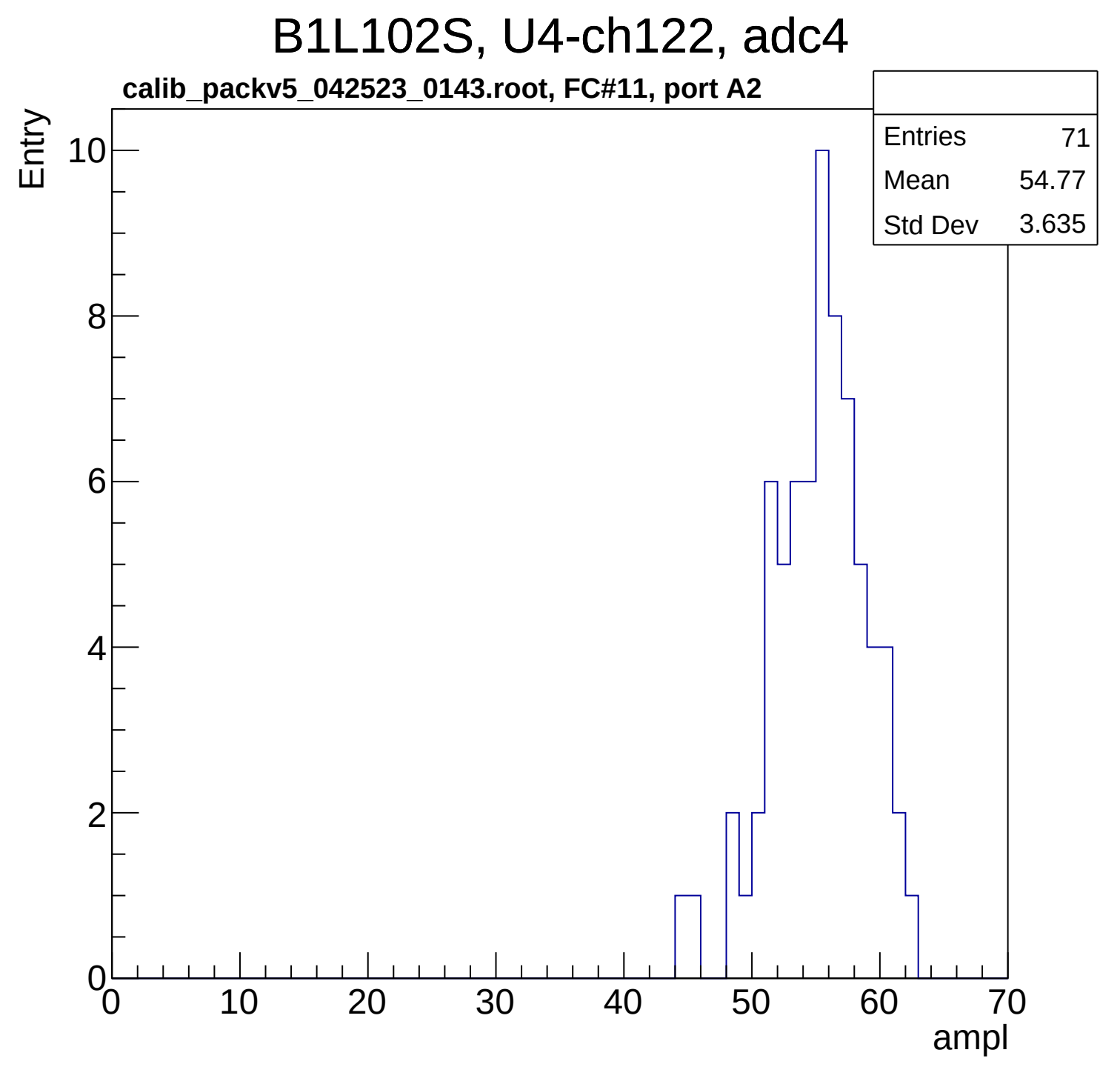
B1L102S, U4-ch122, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 54.77
Std Dev 3.635
Entry
ampl
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8
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0
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60
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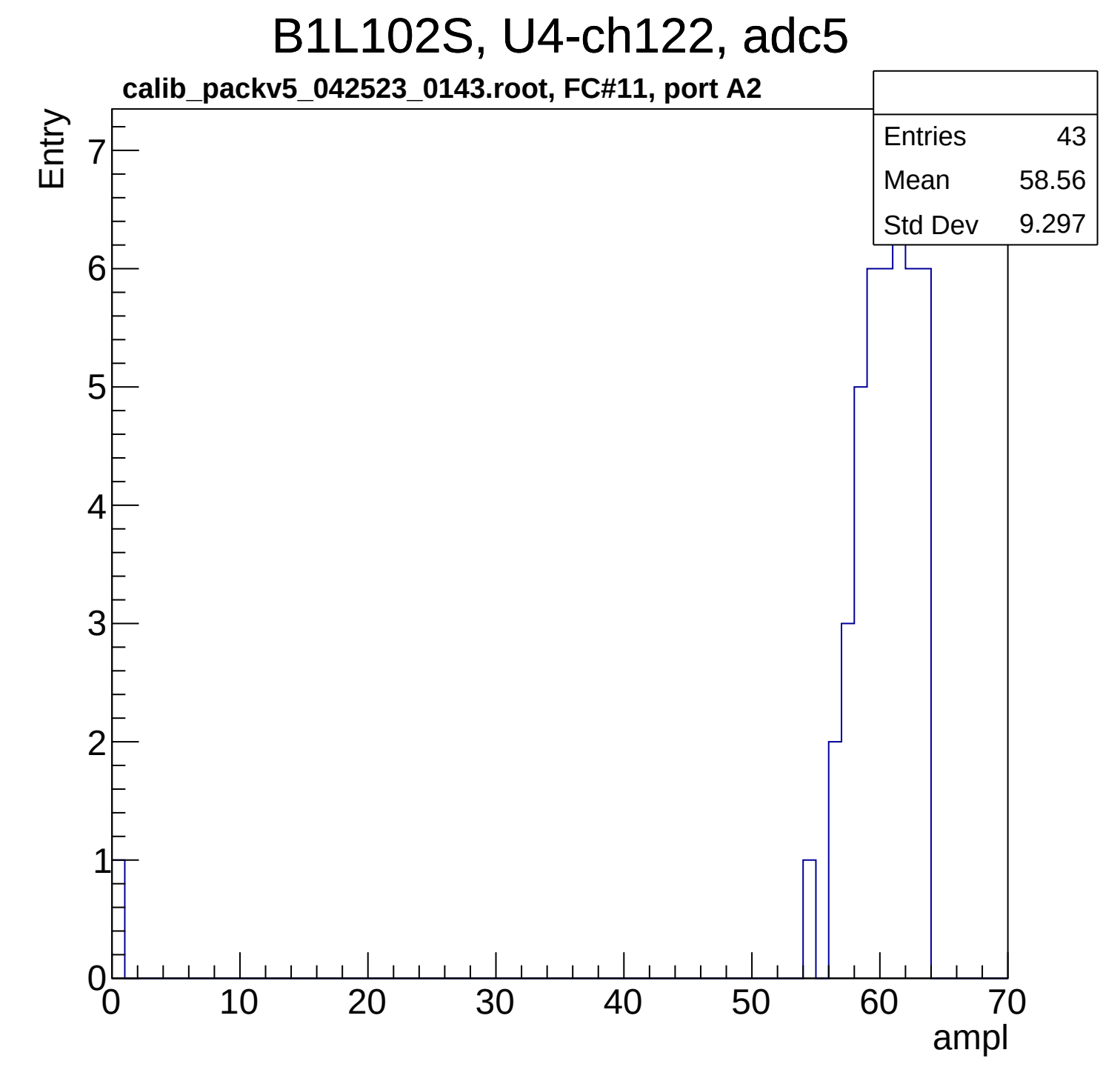
B1L102S, U4-ch122, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 43
Mean 58.56
Std Dev 9.297
Entry
ampl
0
1
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3
4
5
6
7
0
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20
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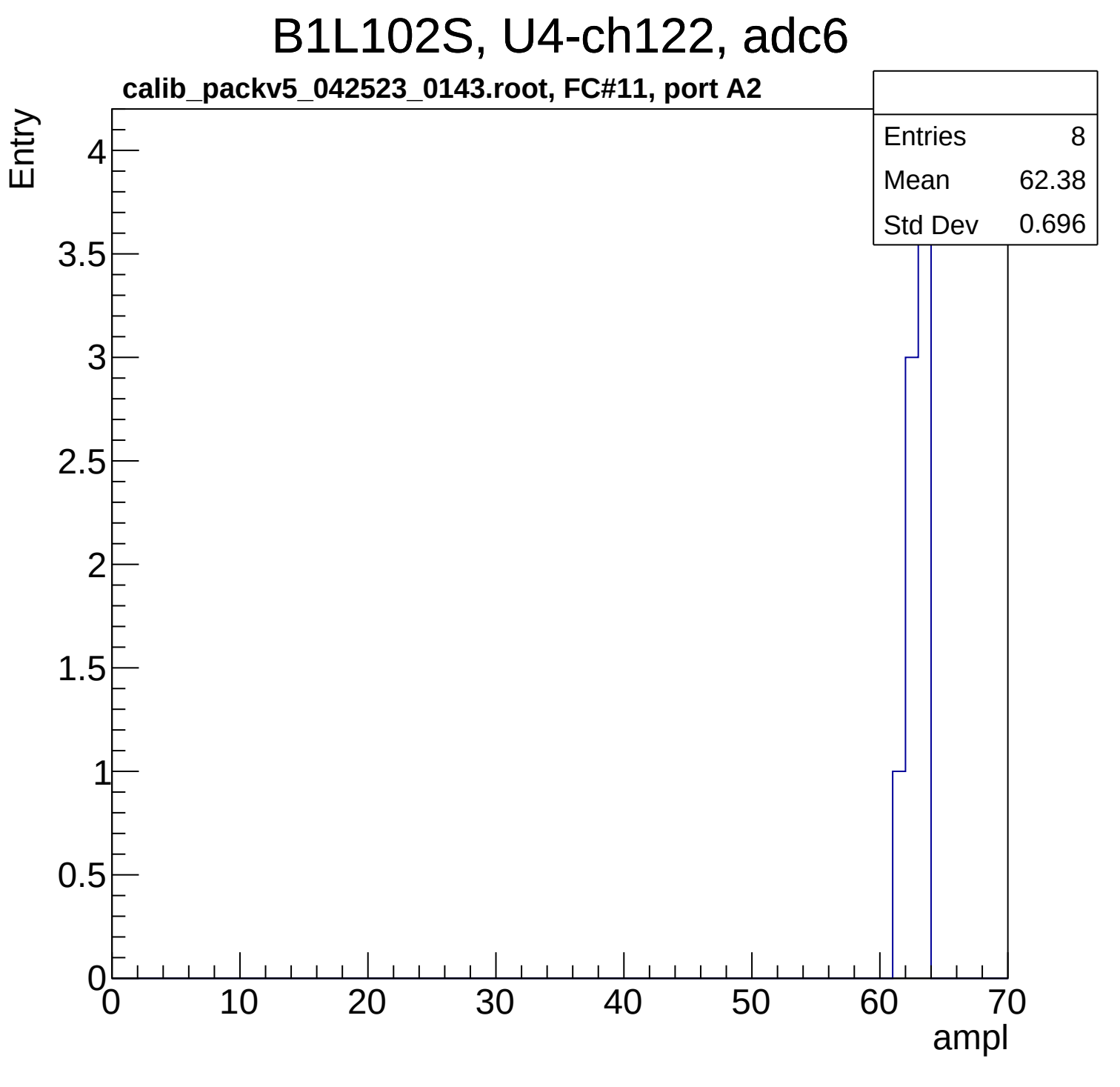
40
50
60
70


B1L102S, U4-ch122, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 8
Mean 62.38
Std Dev 0.696
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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20
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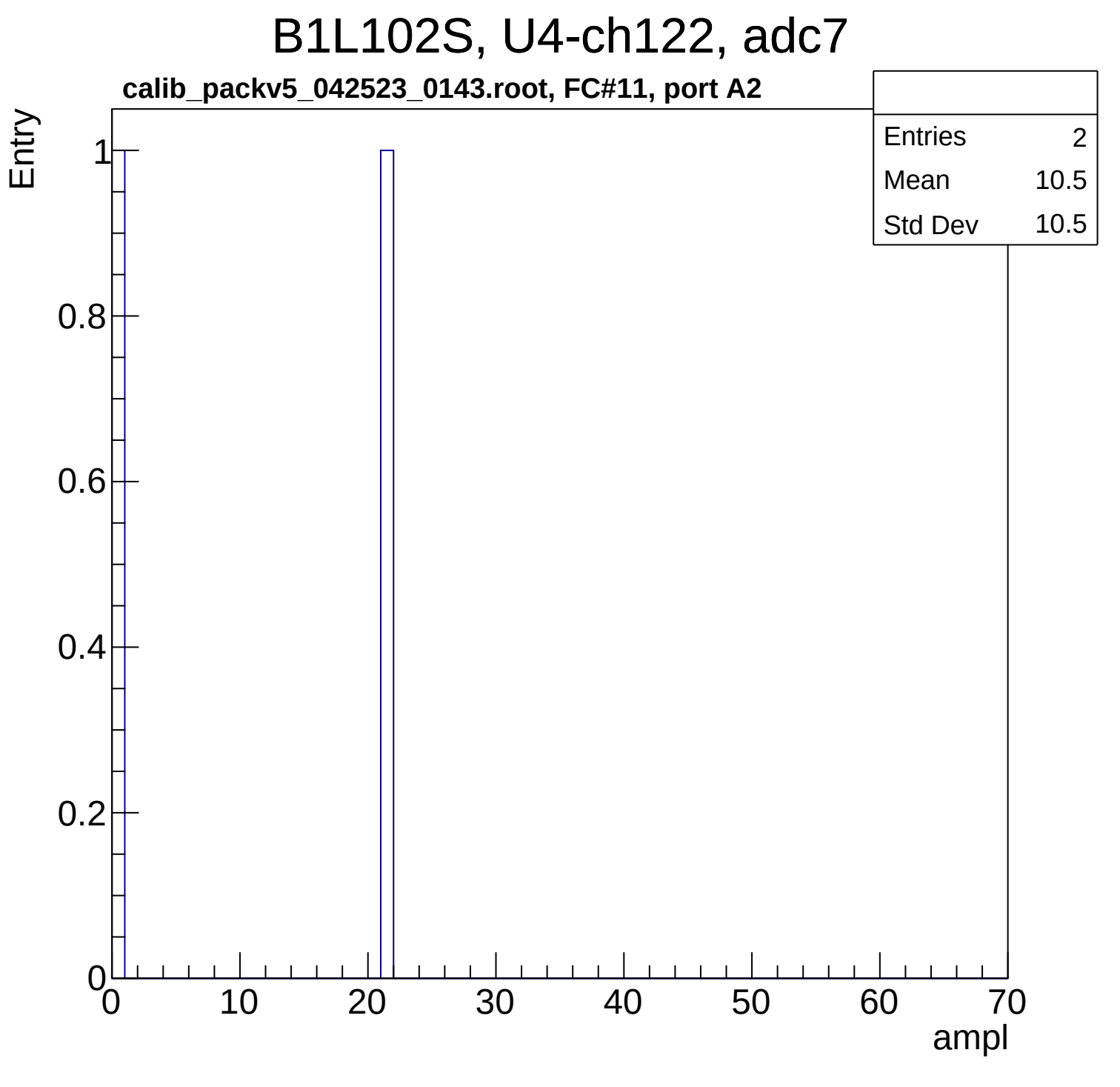
40
50
60
70


B1L102S, U4-ch122, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 10.5
Std Dev 10.5
Entry
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0.6
0.4
0.2
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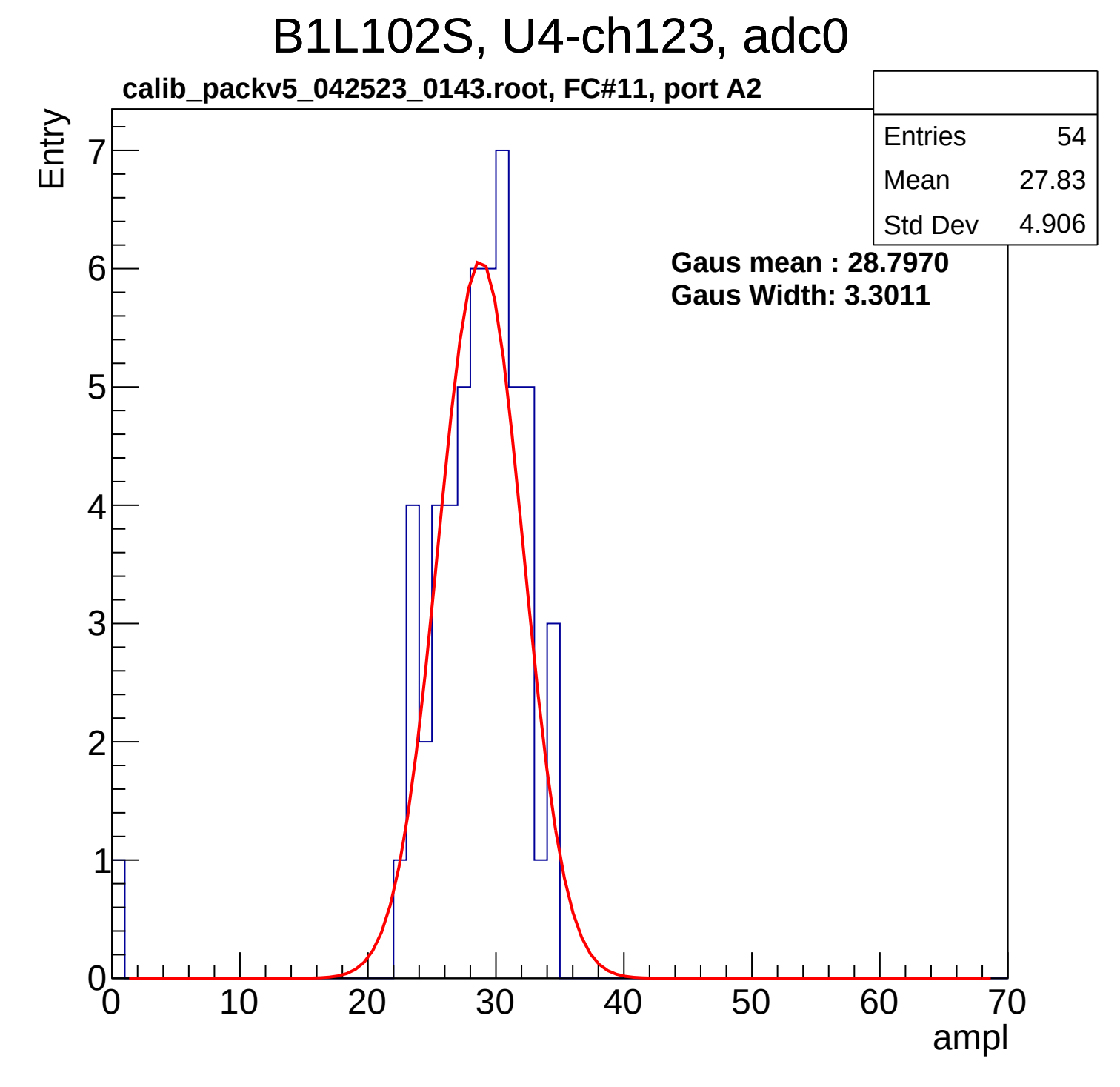
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch123, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 54
Mean 27.83
Std Dev 4.906
Gaus mean : 28.7970
Gaus Width: 3.3011
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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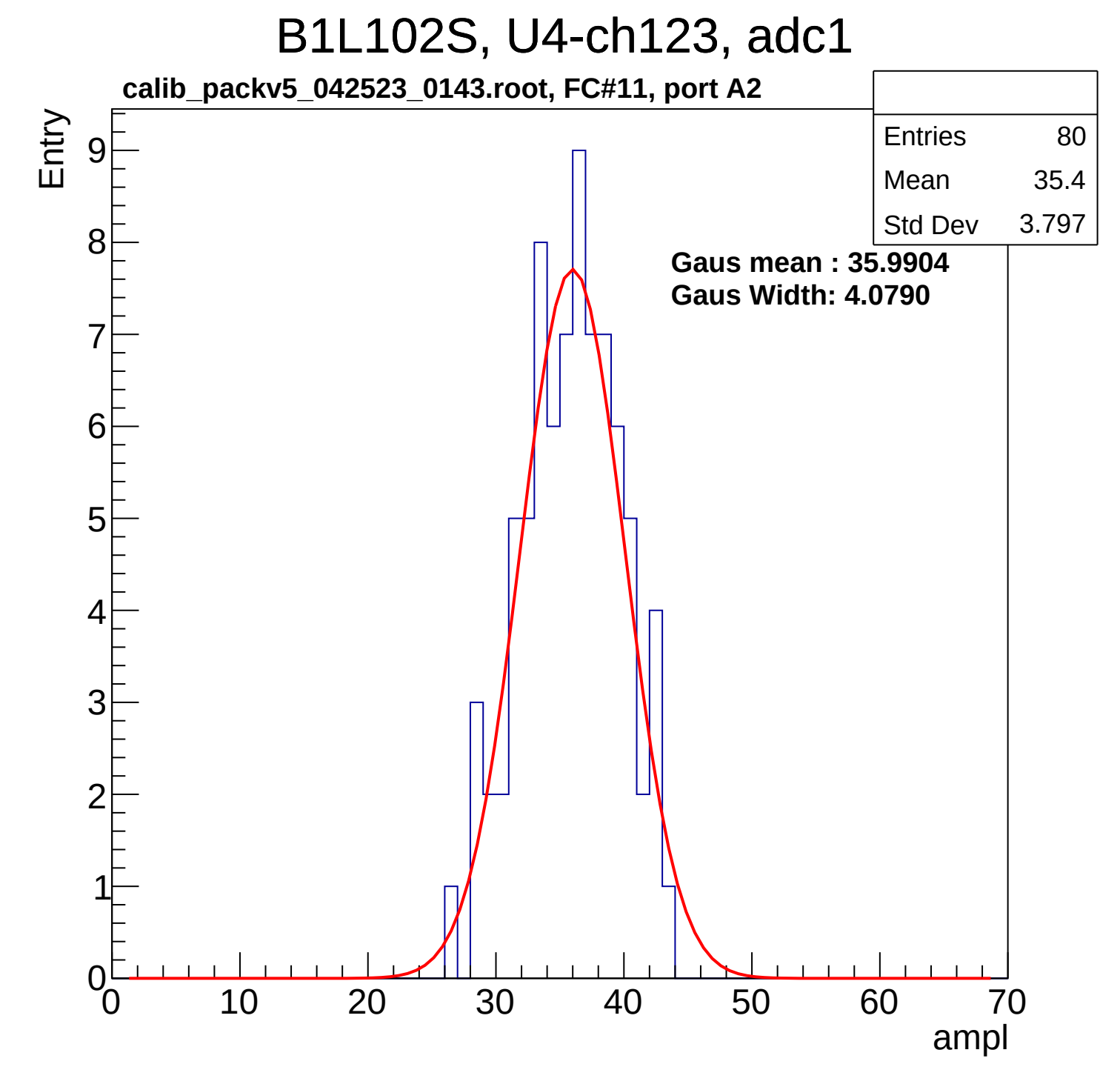
B1L102S, U4-ch123, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 80
Mean 35.4
Std Dev 3.797
Gaus mean : 35.9904
Gaus Width: 4.0790
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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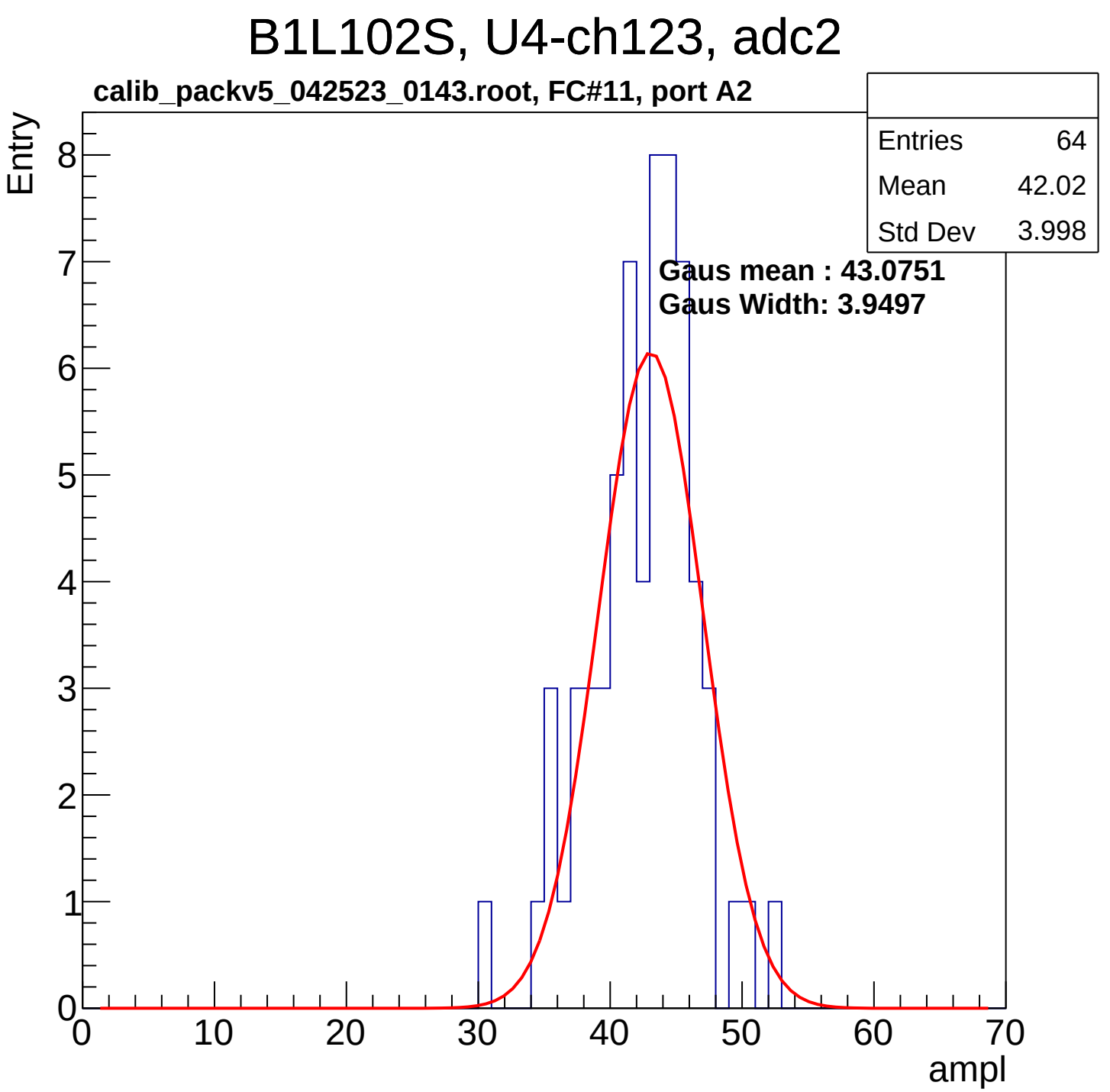
B1L102S, U4-ch123, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 42.02
Std Dev 3.998
Gaus mean : 43.0751
Gaus Width: 3.9497
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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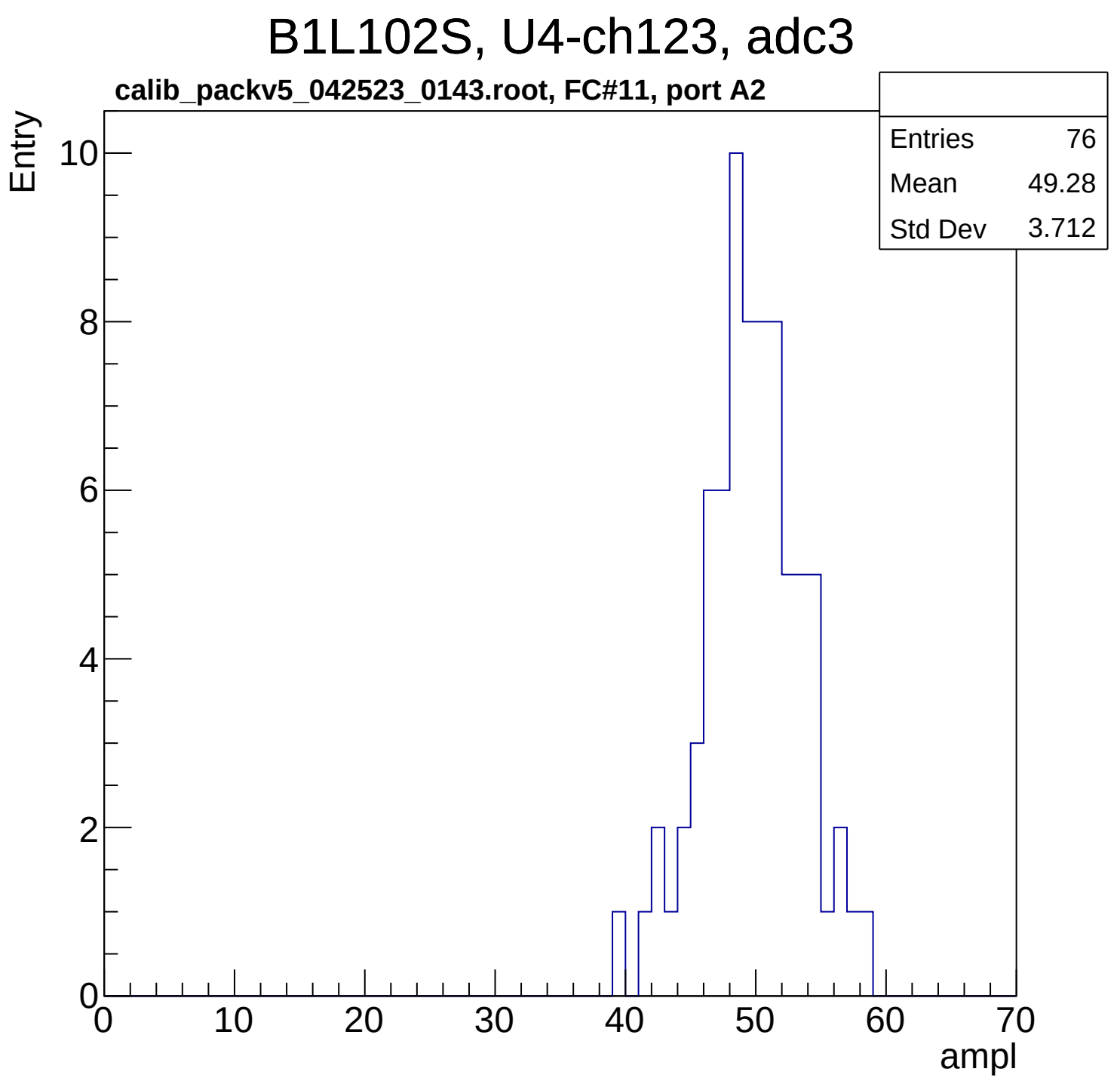
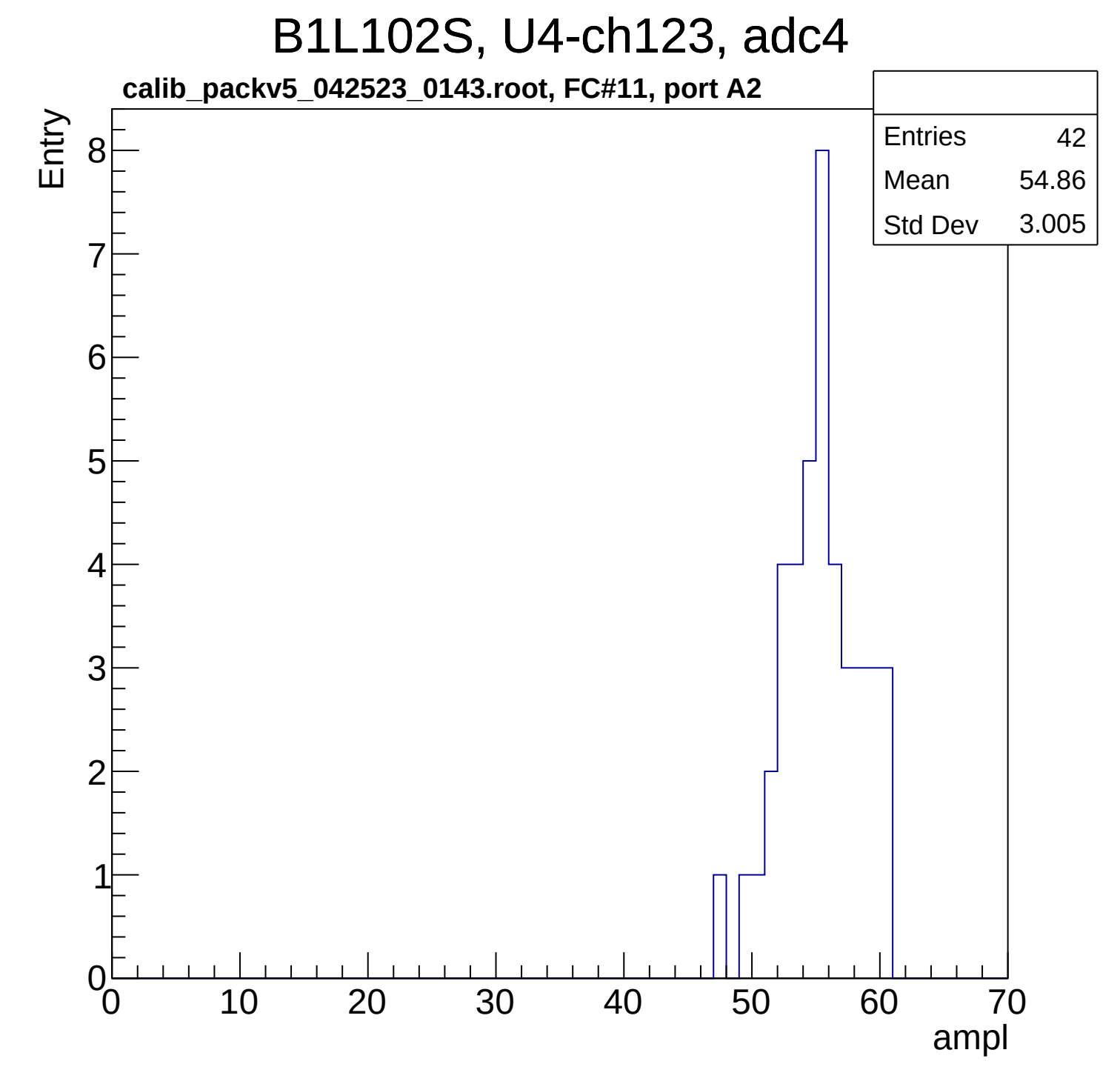

B1L102S, U4-ch123, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 76
Mean 49.28
Std Dev 3.712
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch123, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 42
Mean 54.86
Std Dev 3.005
Entry
ampl
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2
3
4
5
6
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0
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40
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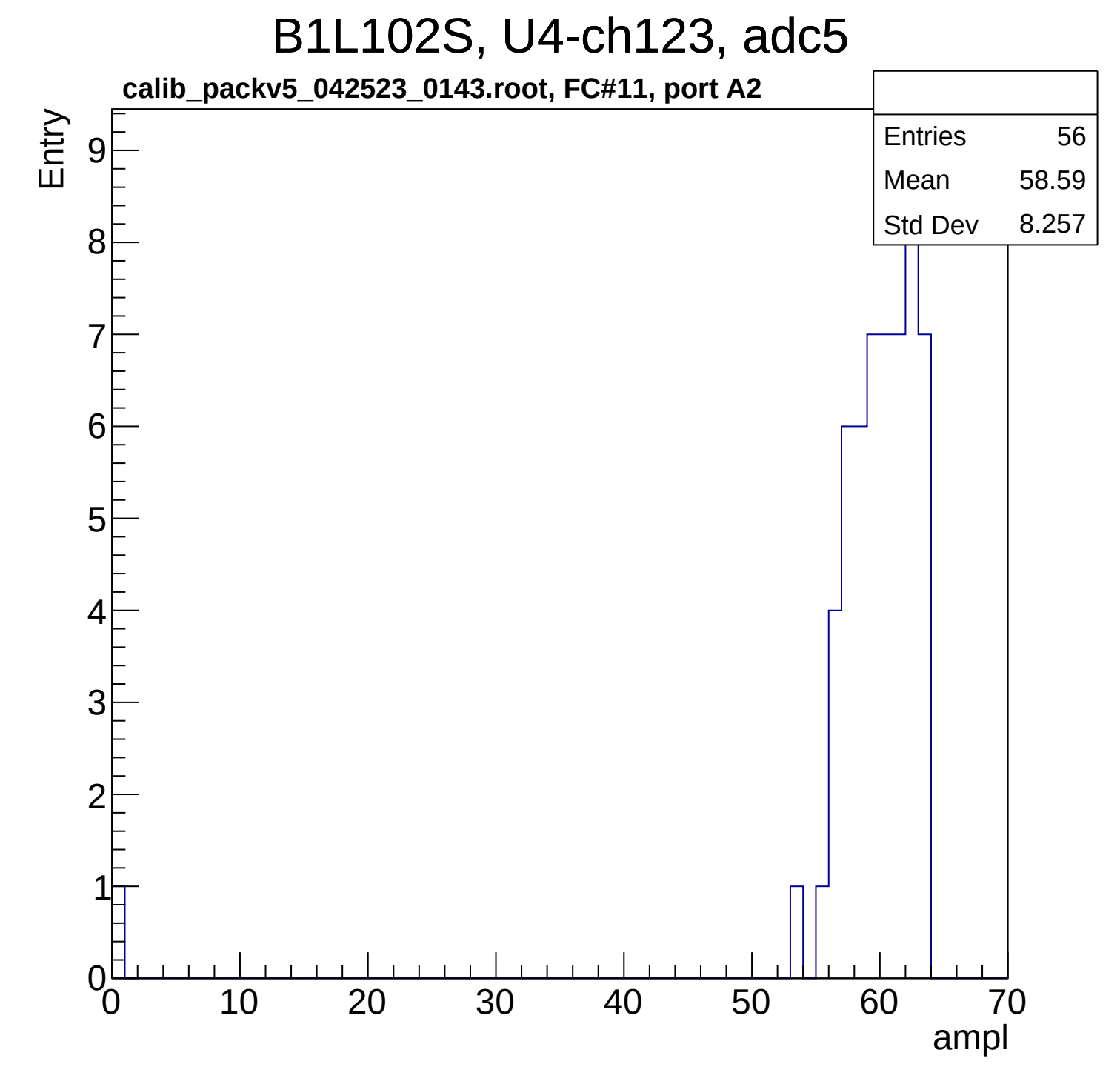
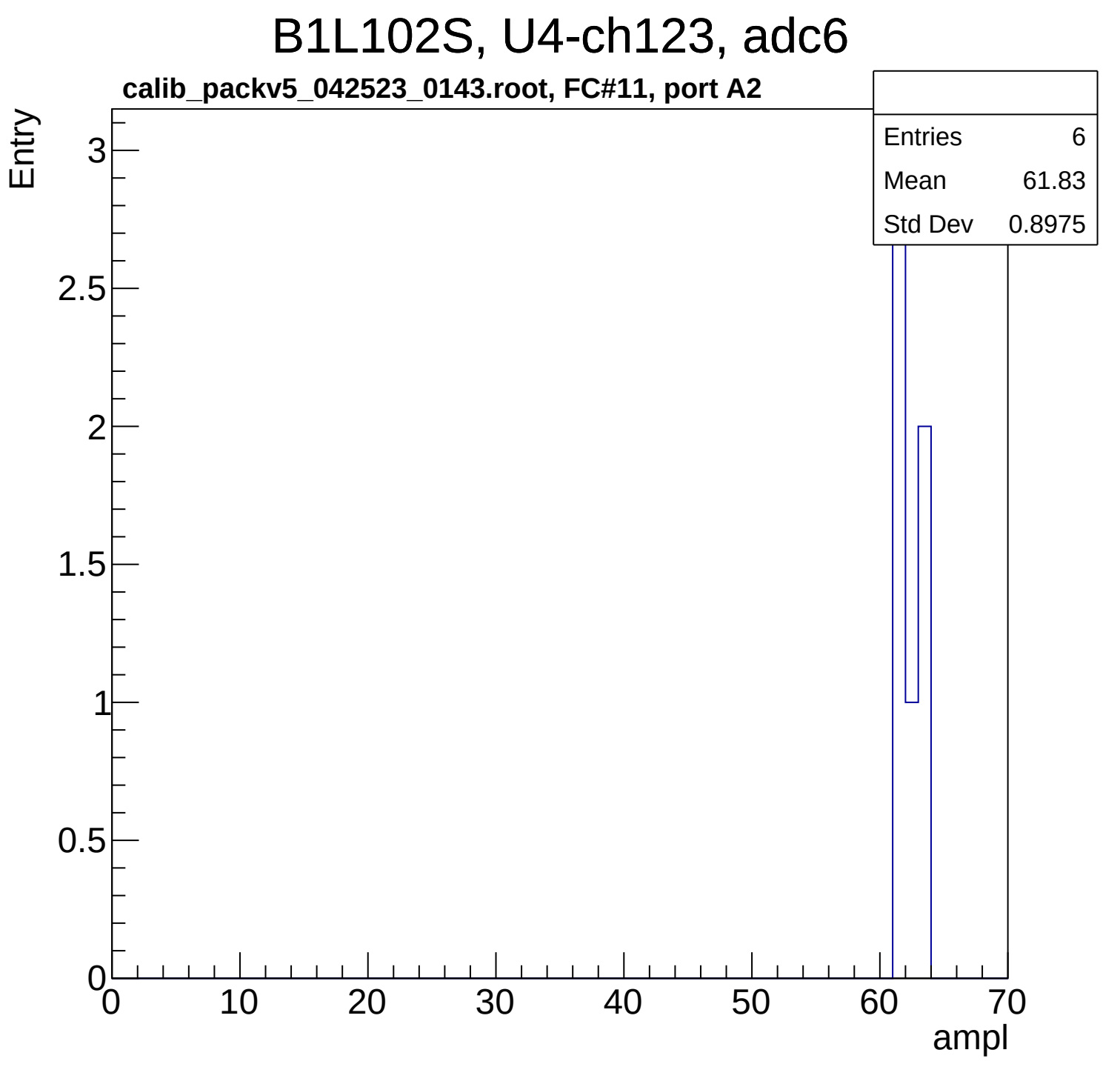

B1L102S, U4-ch123, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 56
Mean 58.59
Std Dev 8.257
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L102S, U4-ch123, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 6
Mean 61.83
Std Dev 0.8975
Entry
ampl
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0.5
1
1.5
2
2.5
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0
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60
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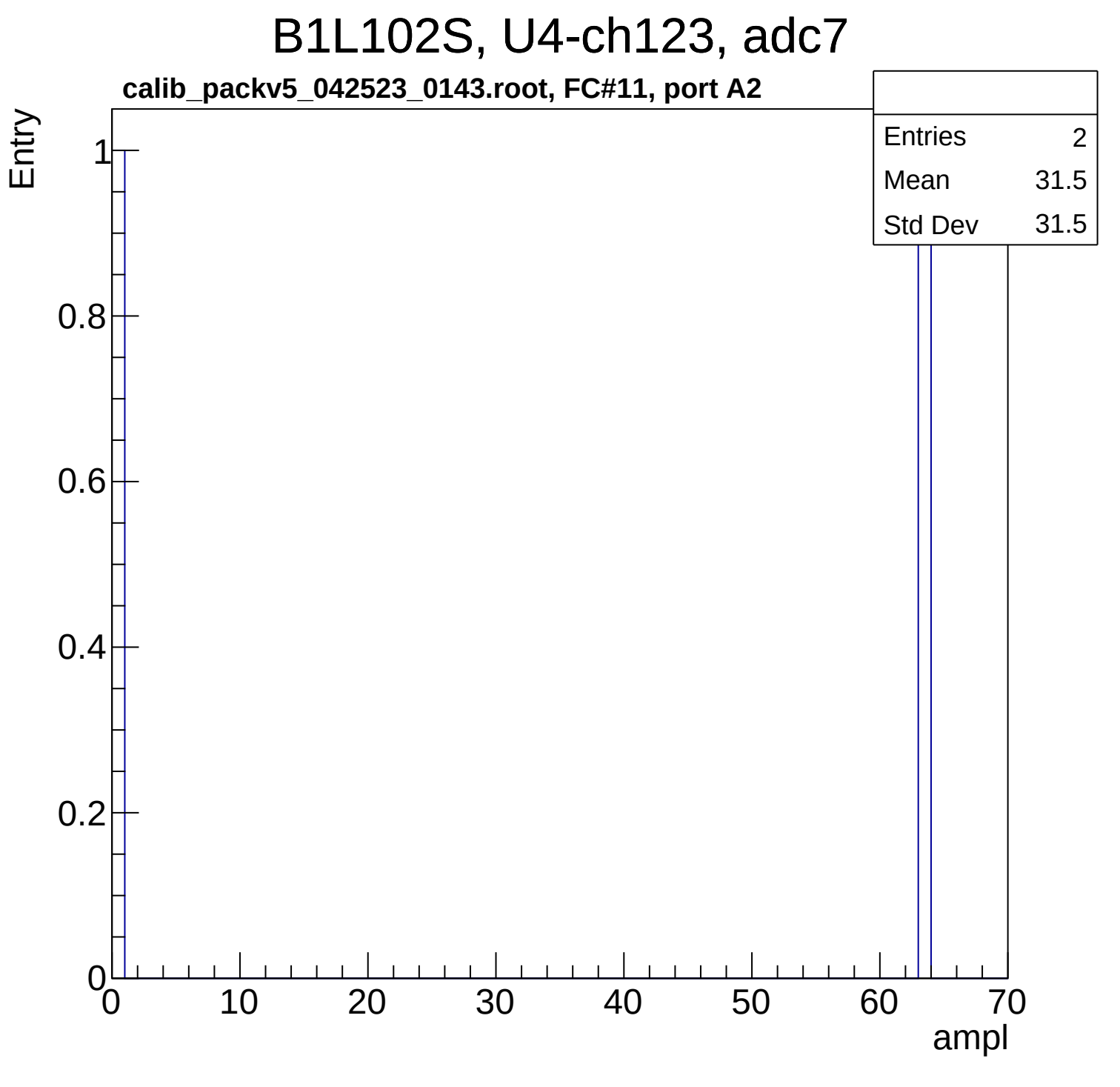
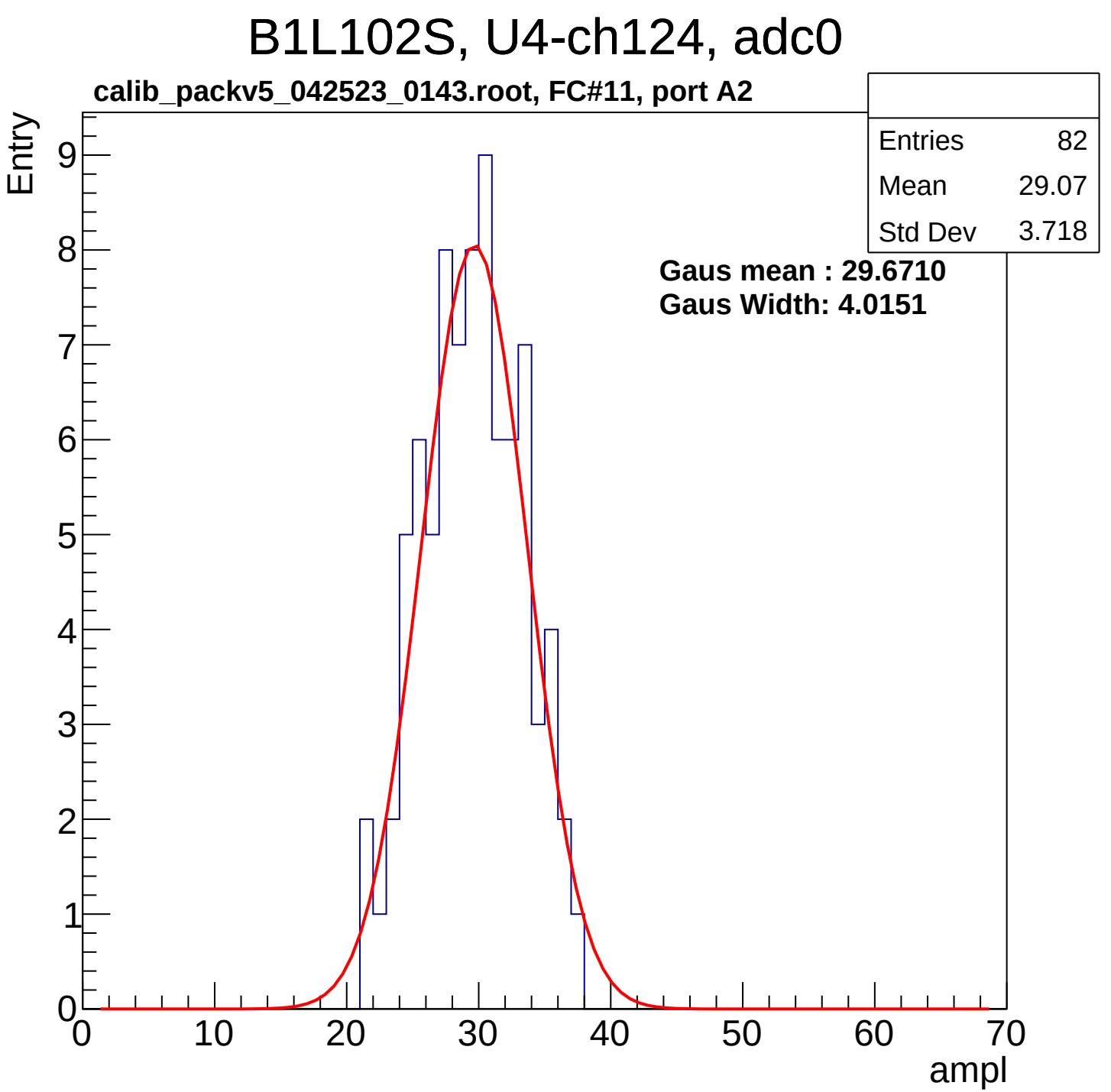

B1L102S, U4-ch123, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch124, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 82
Mean 29.07
Std Dev 3.718
Gaus mean : 29.6710
Gaus Width: 4.0151
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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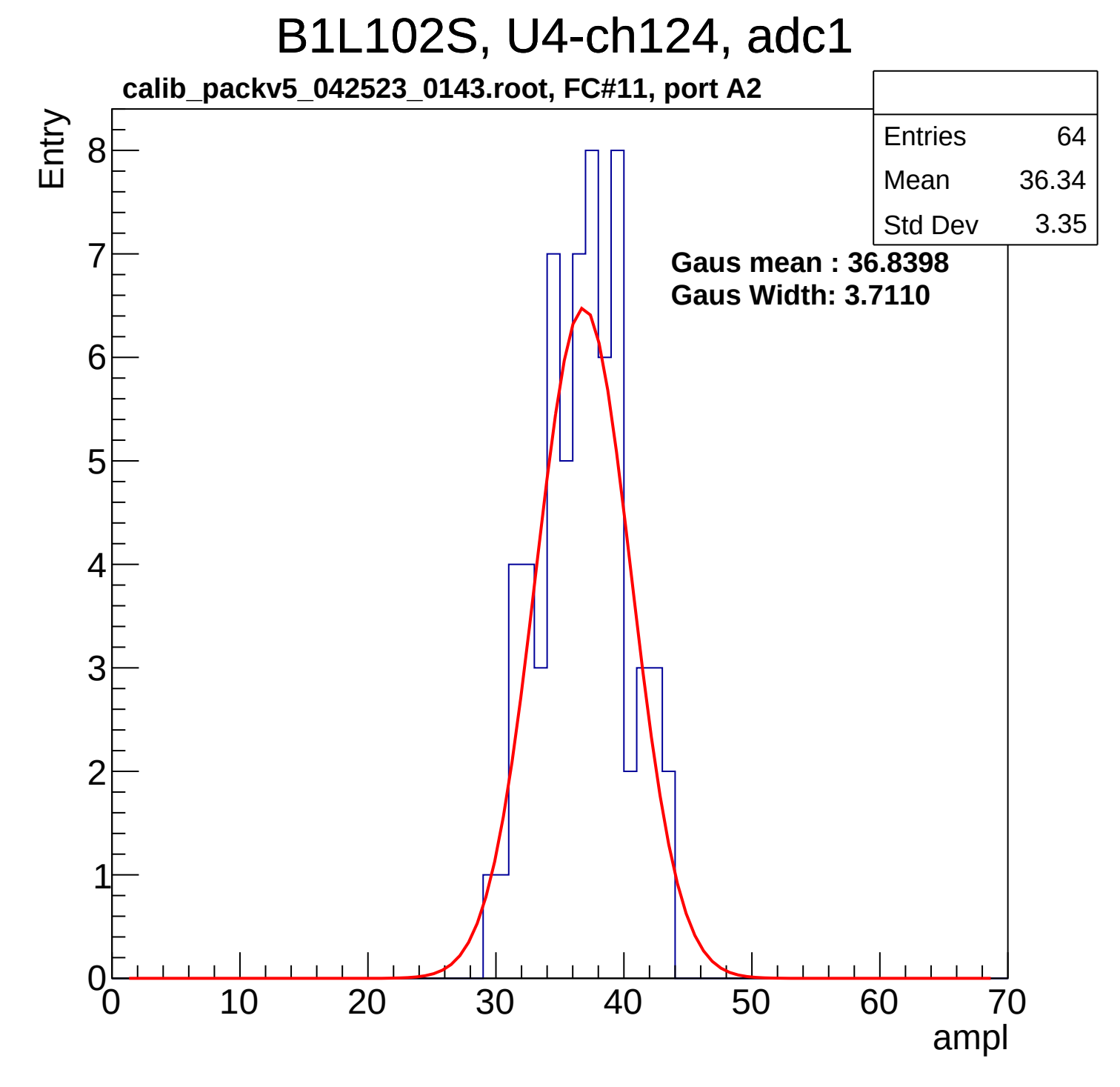
B1L102S, U4-ch124, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 36.34
Std Dev 3.35
Gaus mean : 36.8398
Gaus Width: 3.7110
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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40
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60
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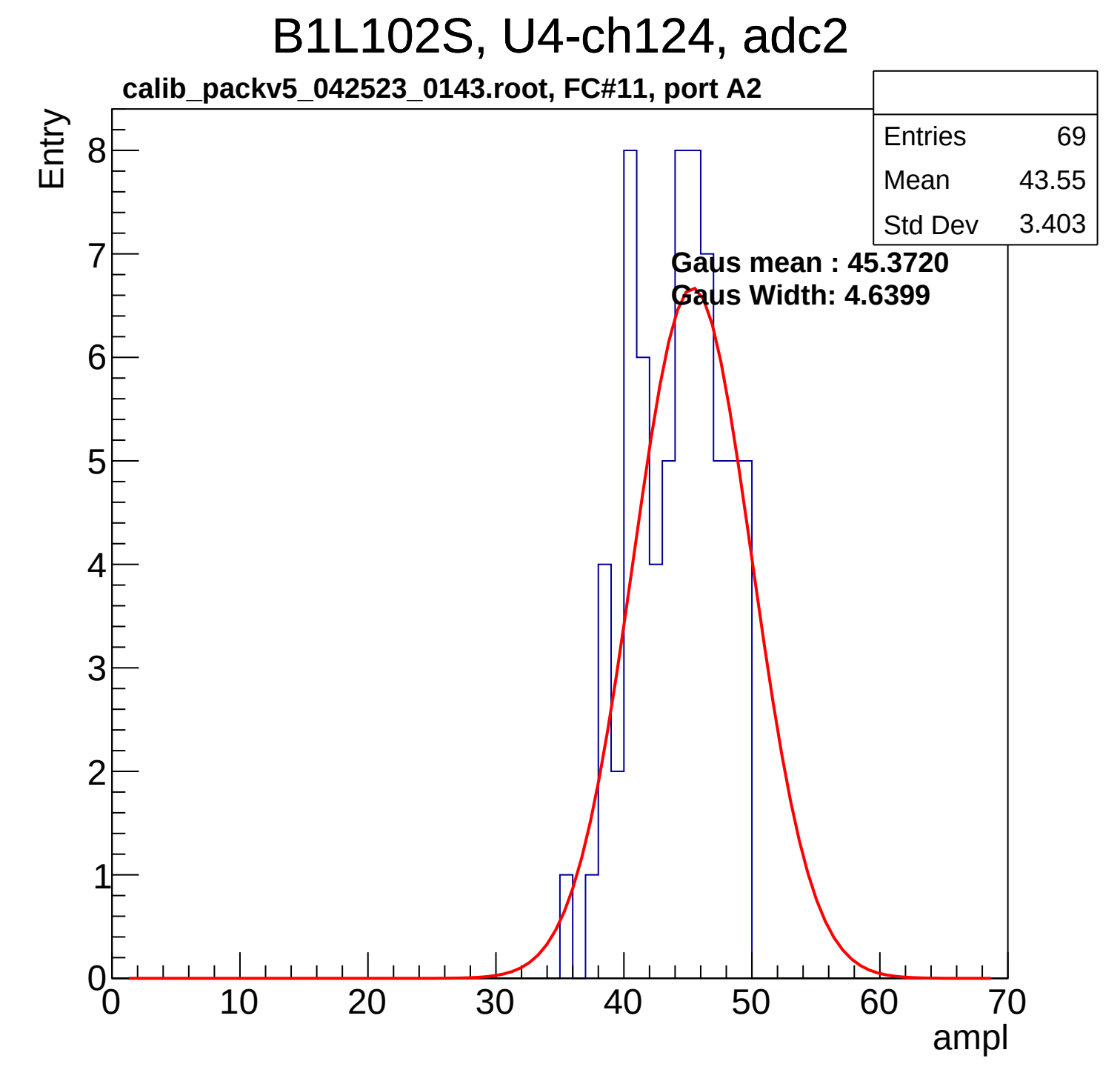
B1L102S, U4-ch124, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 69
Mean 43.55
Std Dev 3.403
Gaus mean : 45.3720
Gaus Width: 4.6399
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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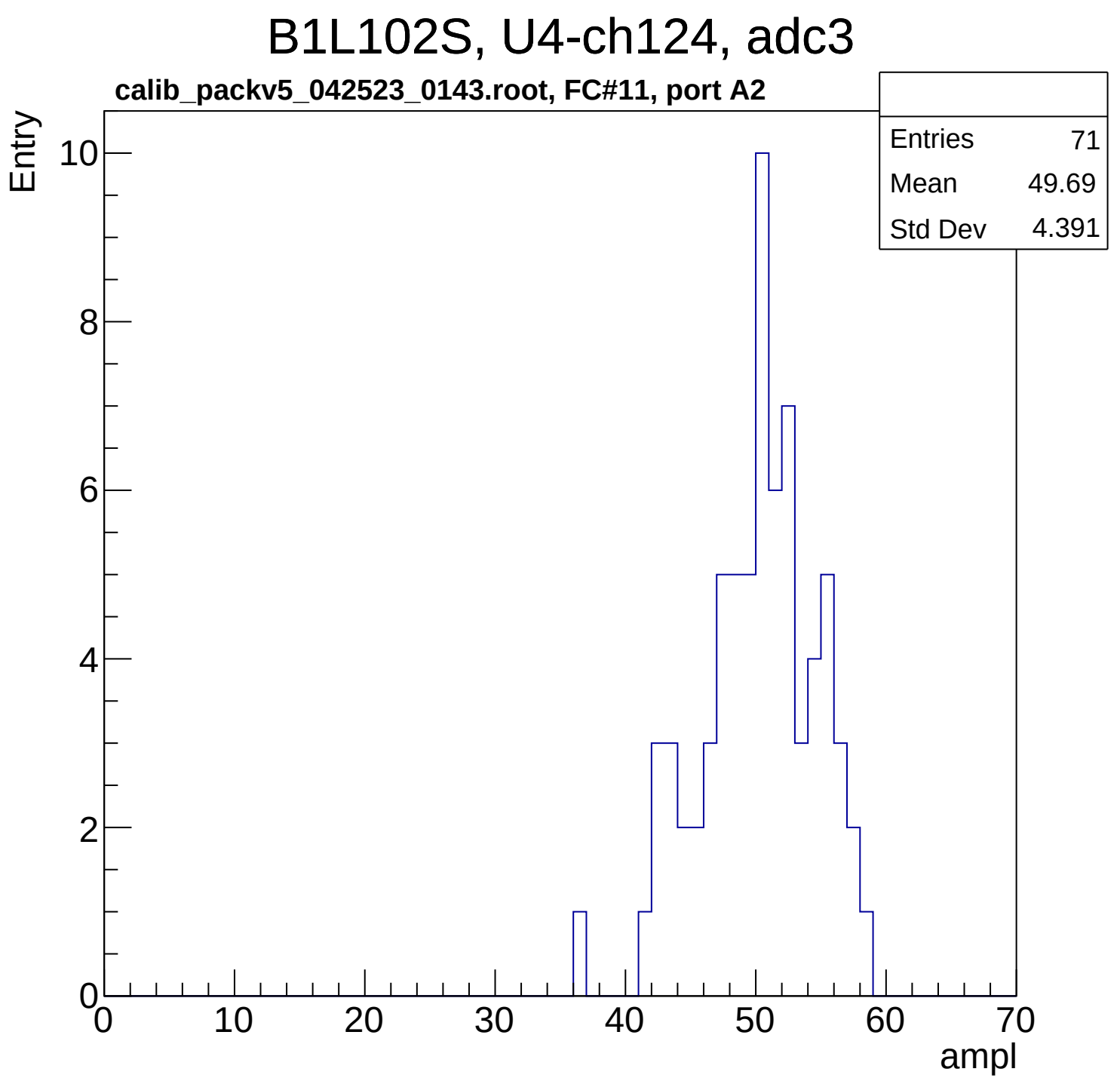
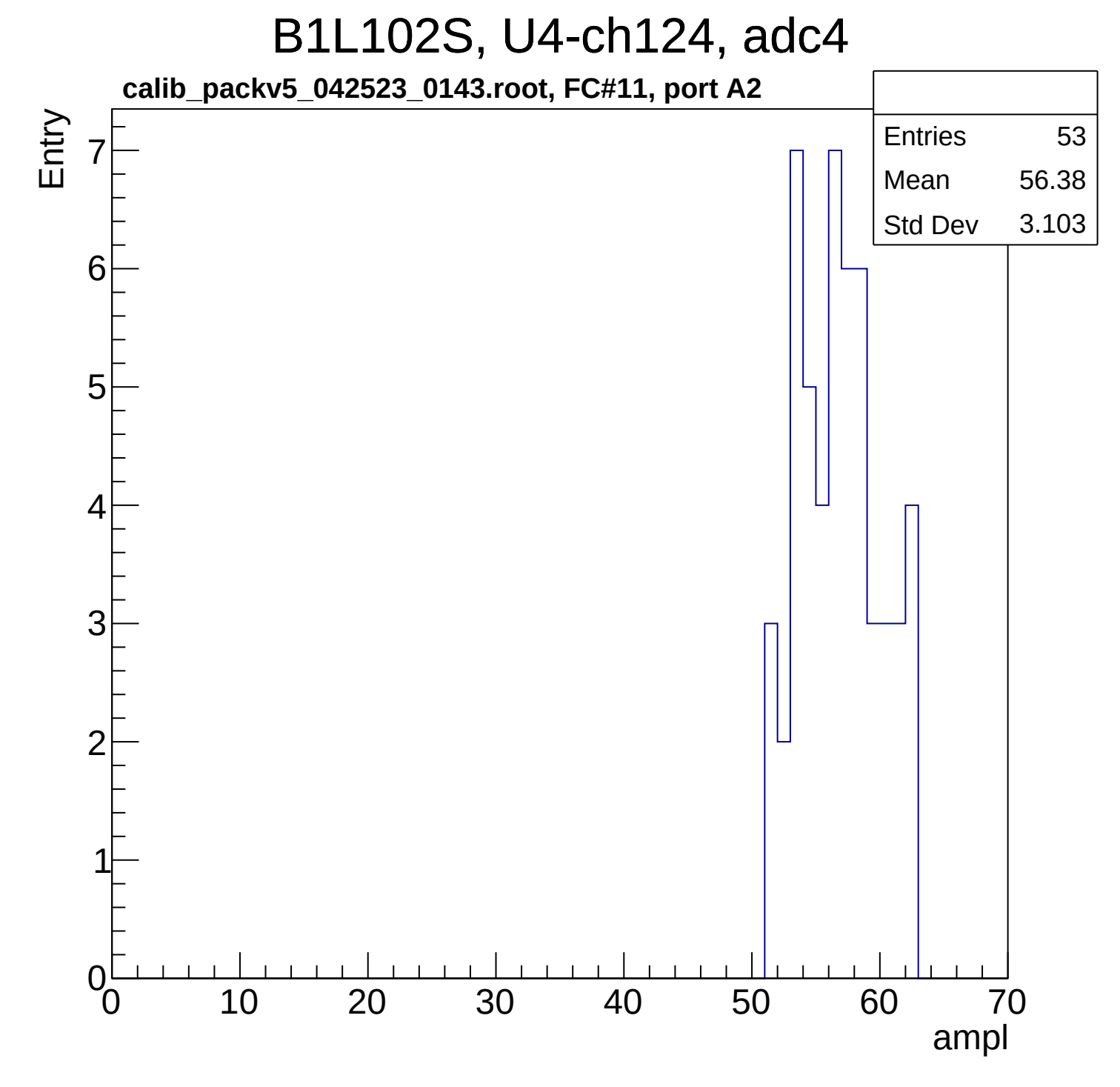

B1L102S, U4-ch124, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 49.69
Std Dev 4.391
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch124, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 53
Mean 56.38
Std Dev 3.103
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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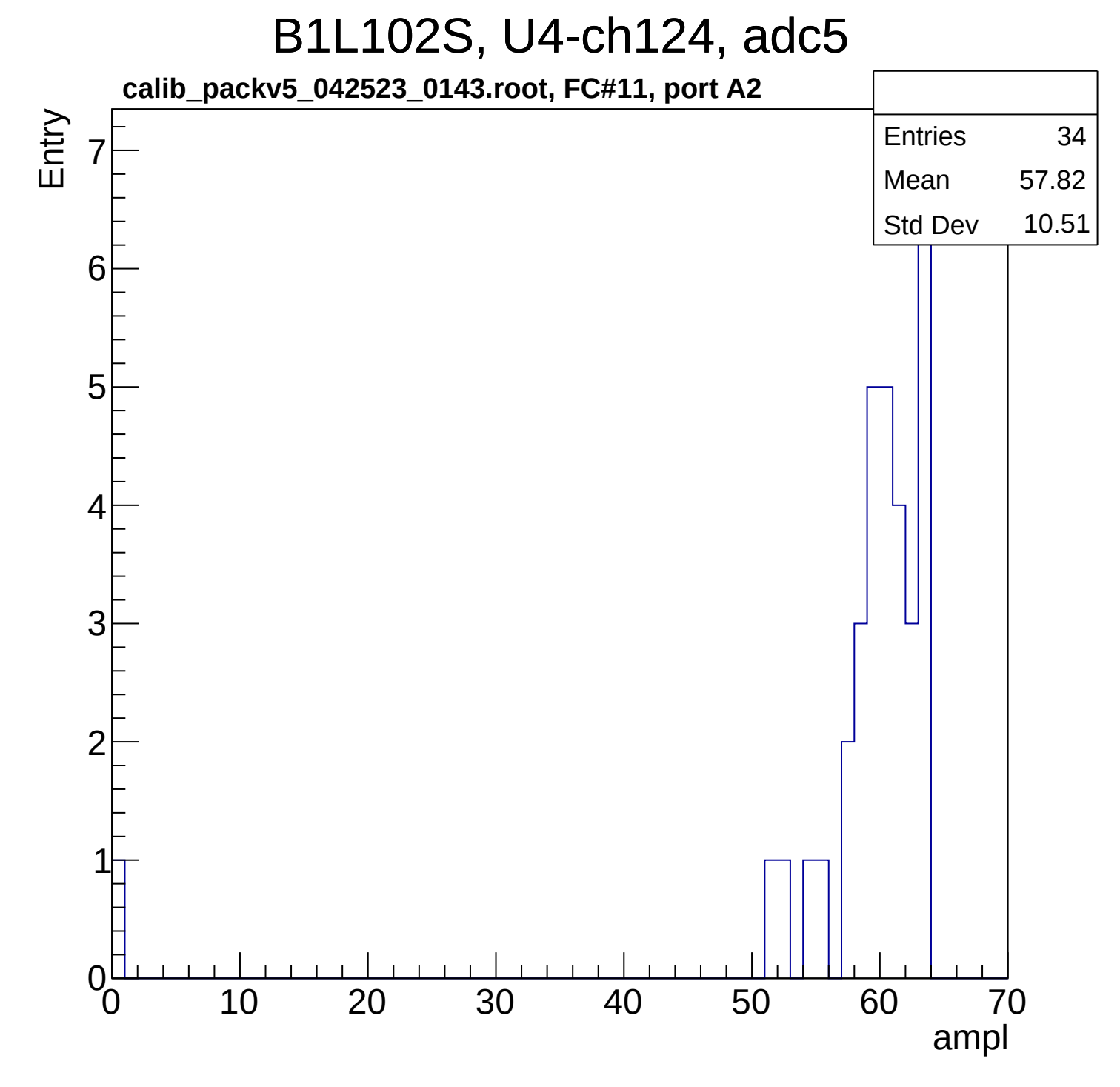
B1L102S, U4-ch124, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 34
Mean 57.82
Std Dev 10.51
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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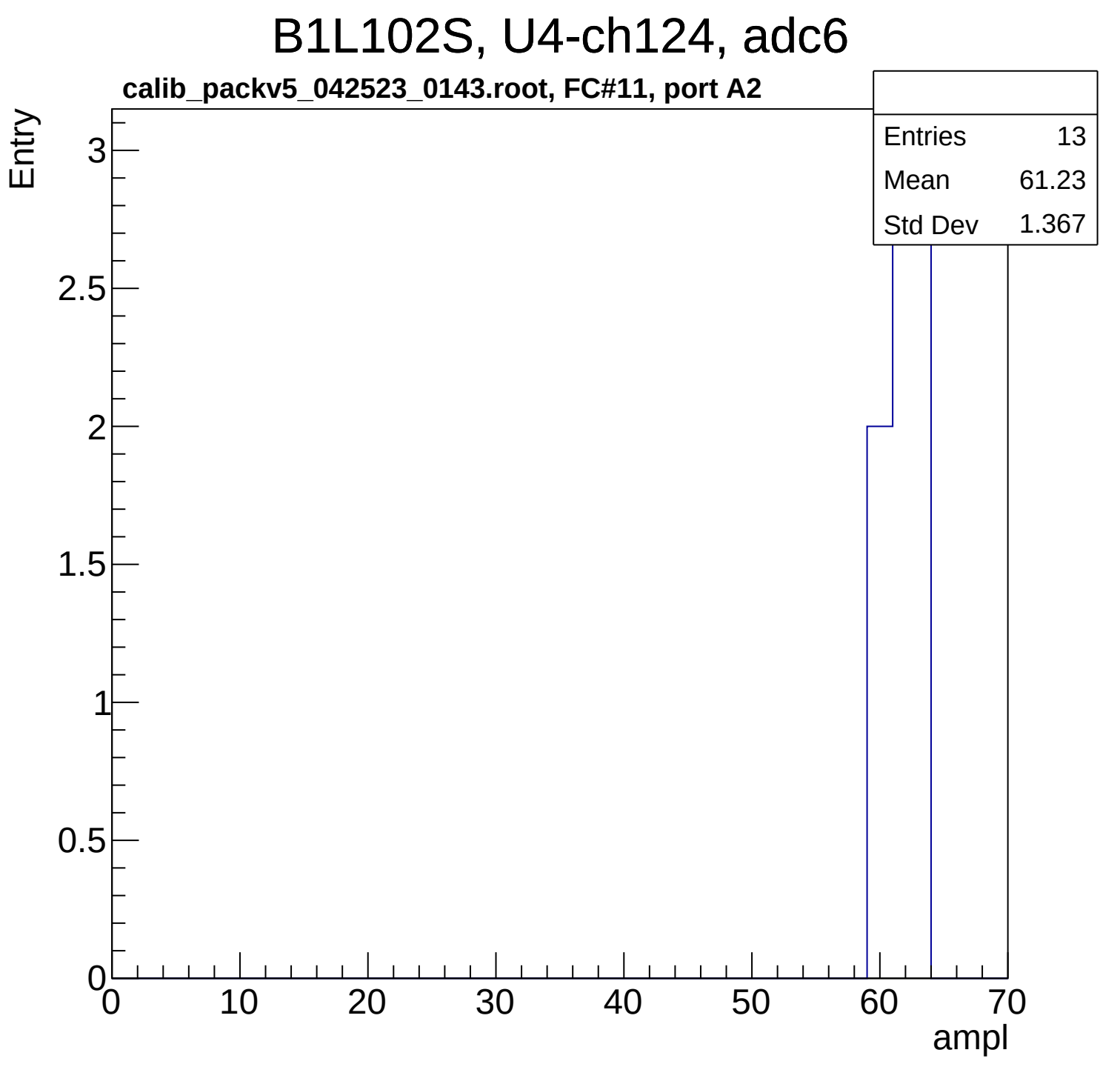
B1L102S, U4-ch124, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 13
Mean 61.23
Std Dev 1.367
Entry
ampl
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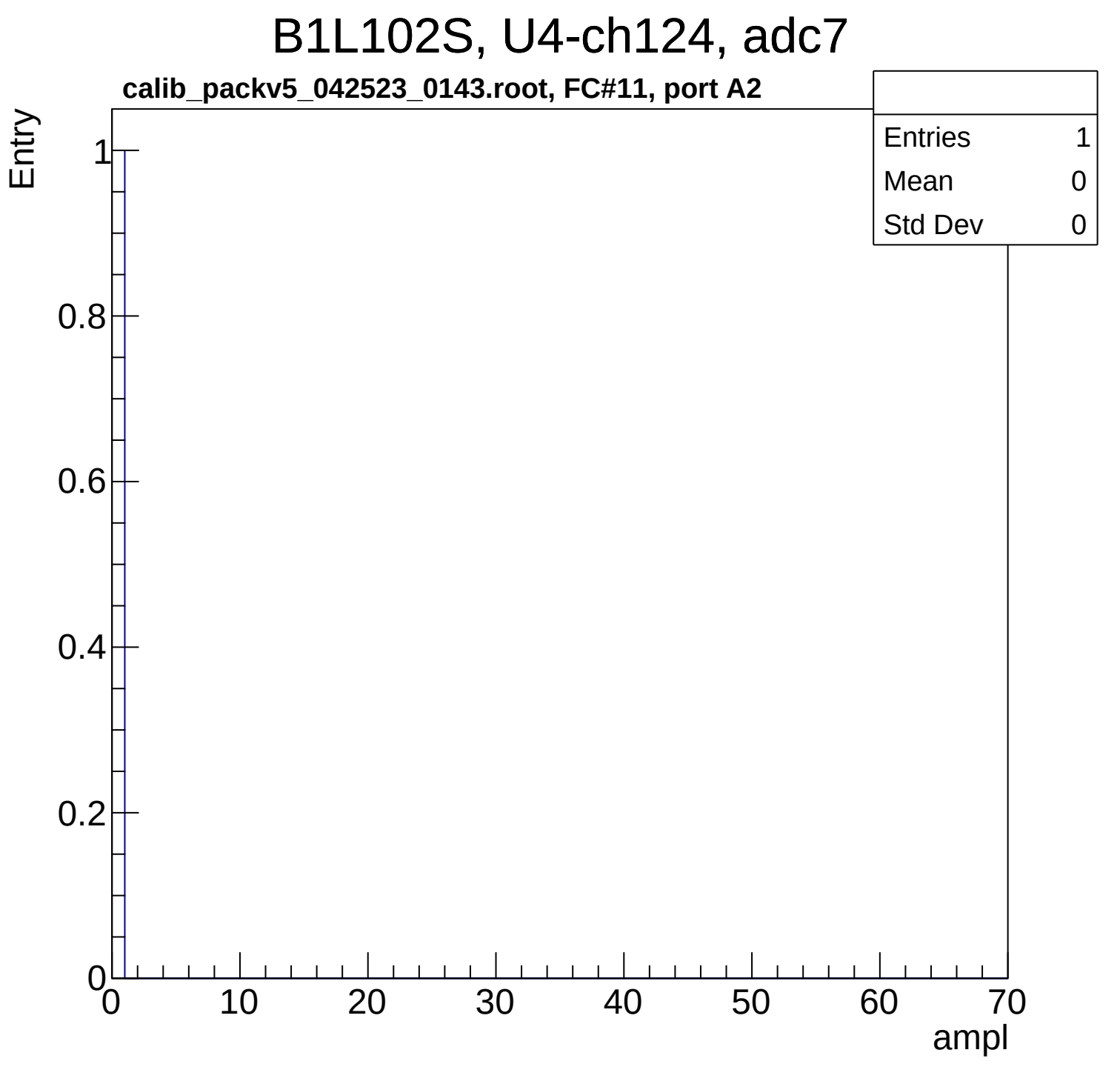
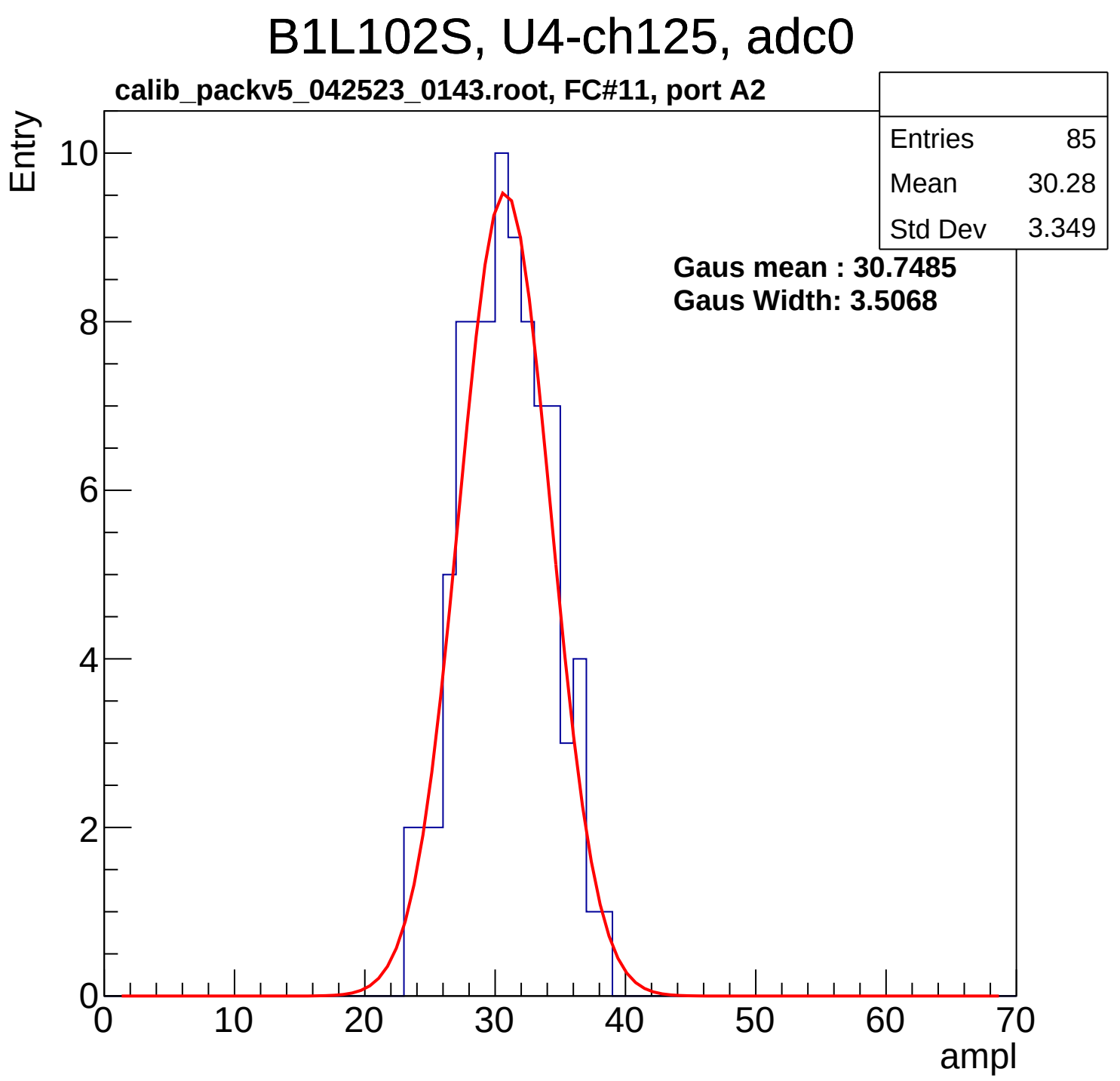
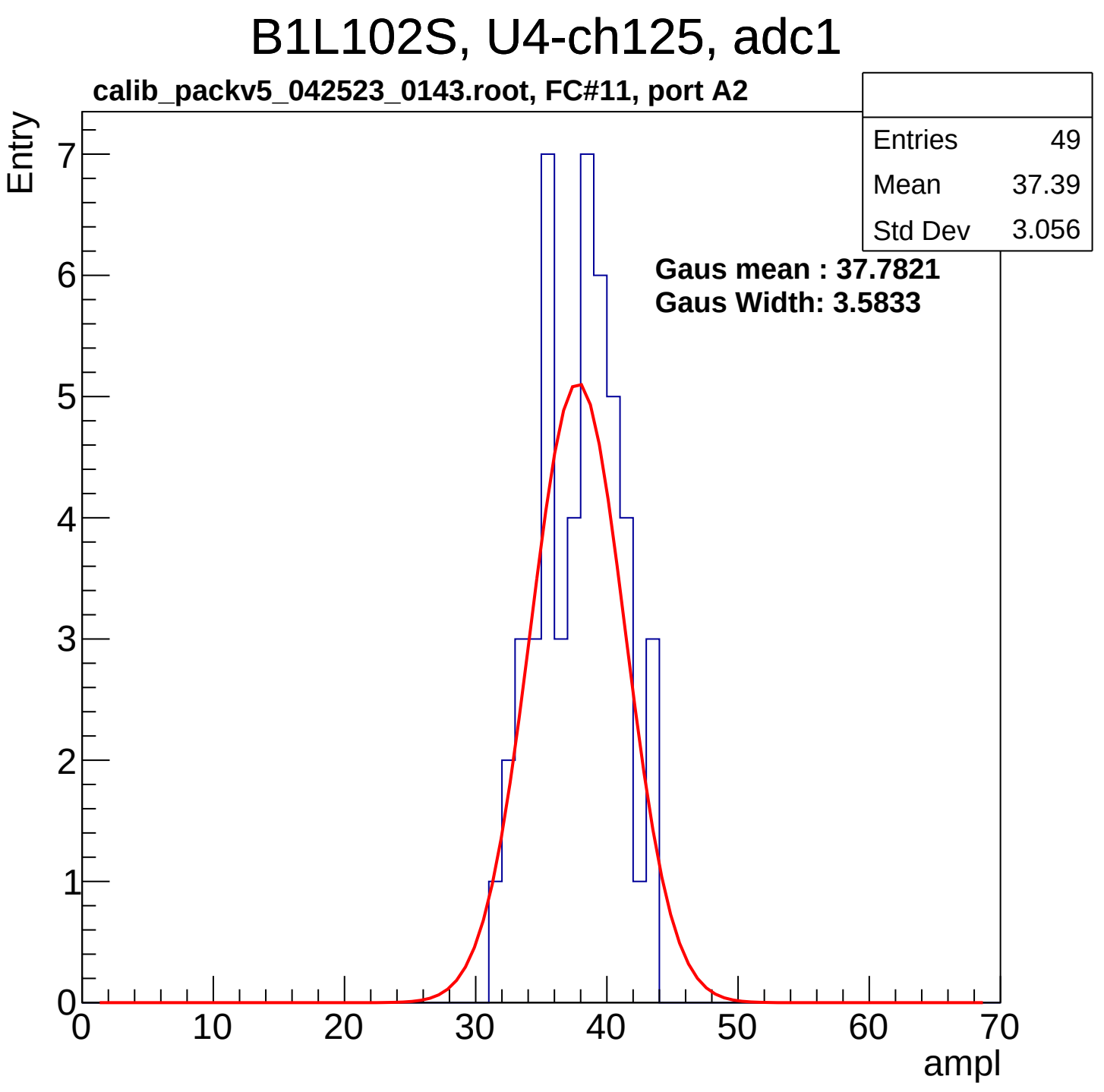
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L102S, U4-ch124, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch125, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 85
Mean 30.28
Std Dev 3.349
Gaus mean : 30.7485
Gaus Width: 3.5068
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L102S, U4-ch125, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 49
Mean 37.39
Std Dev 3.056
Gaus mean : 37.7821
Gaus Width: 3.5833
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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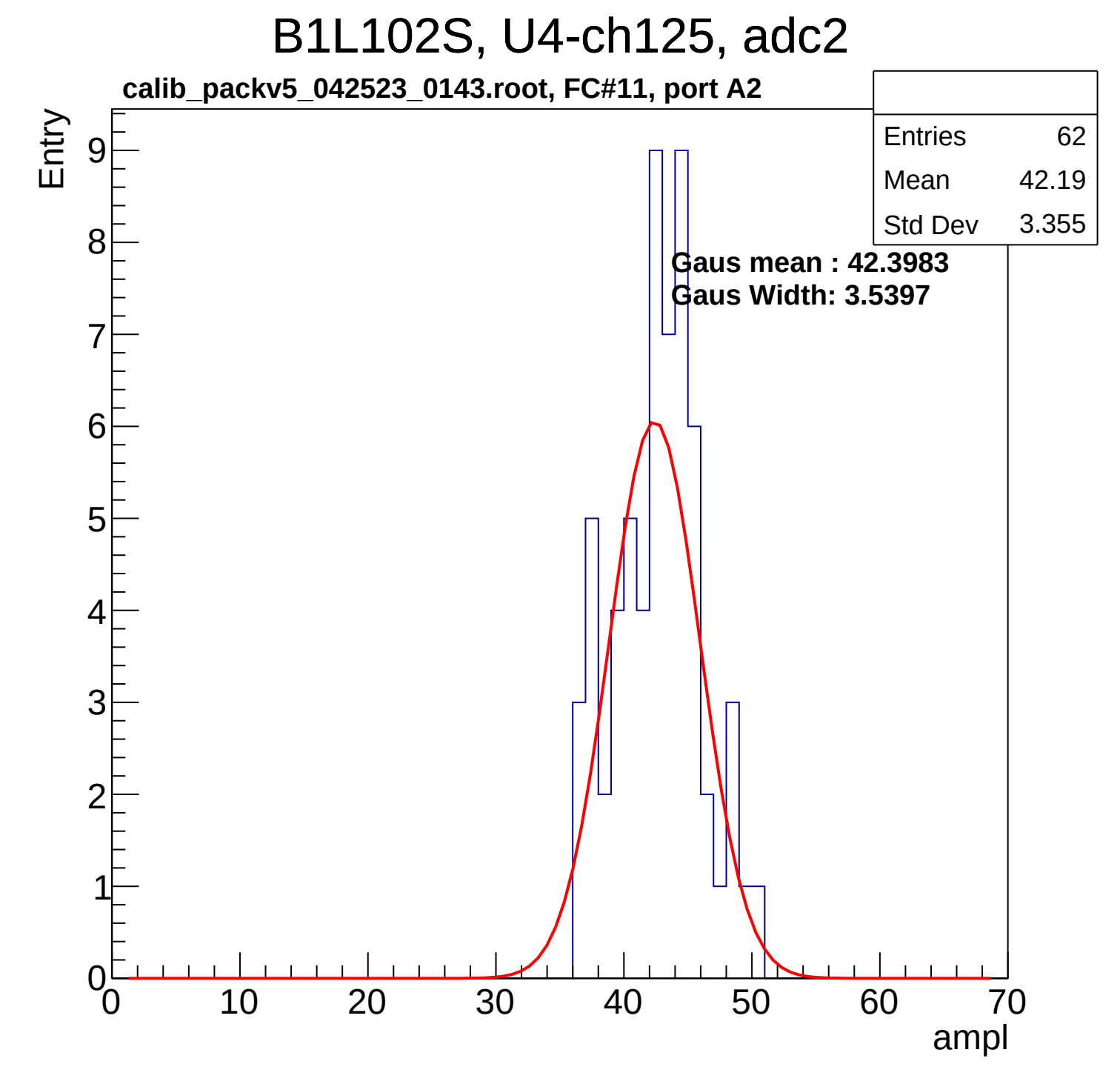
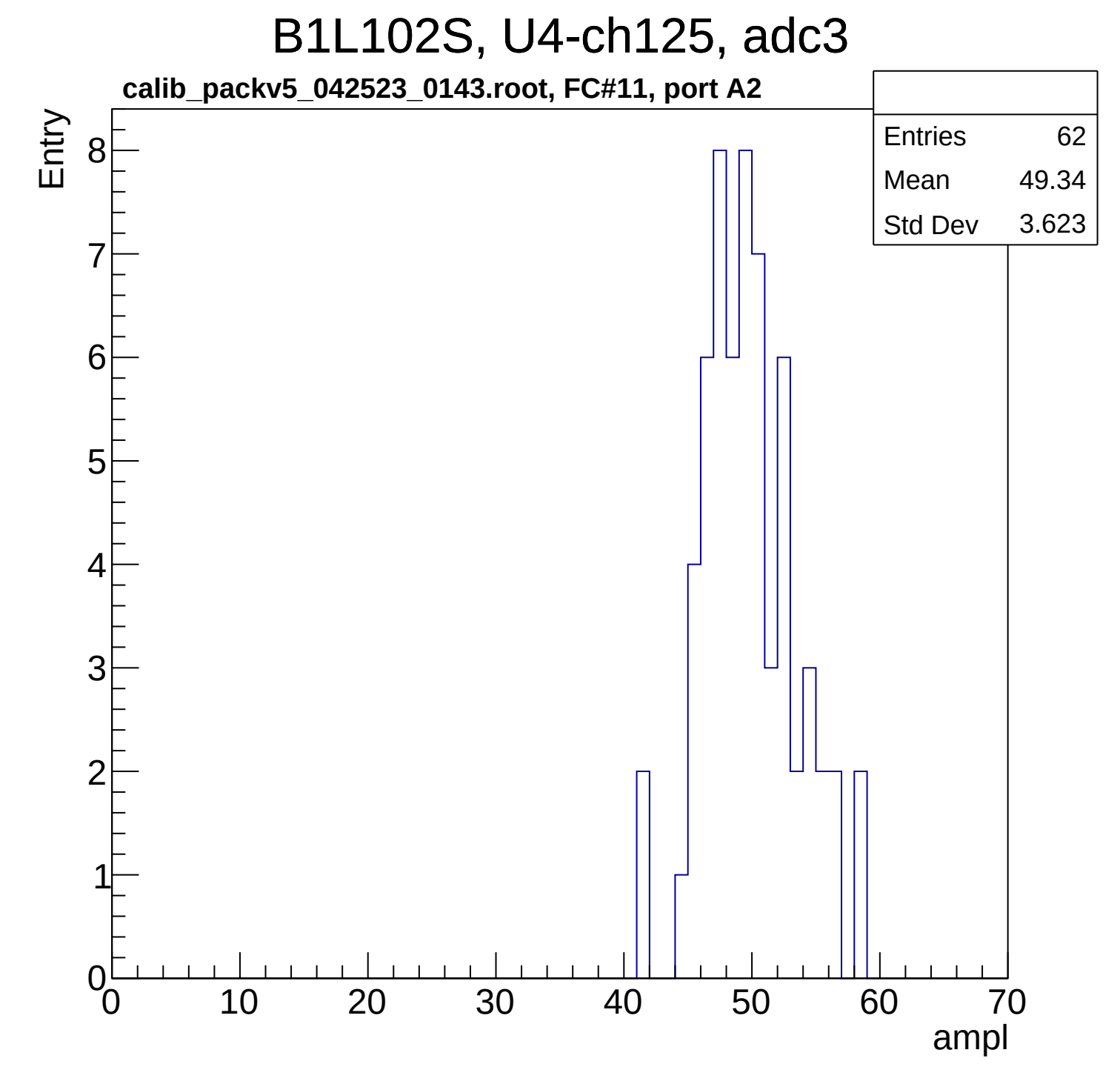
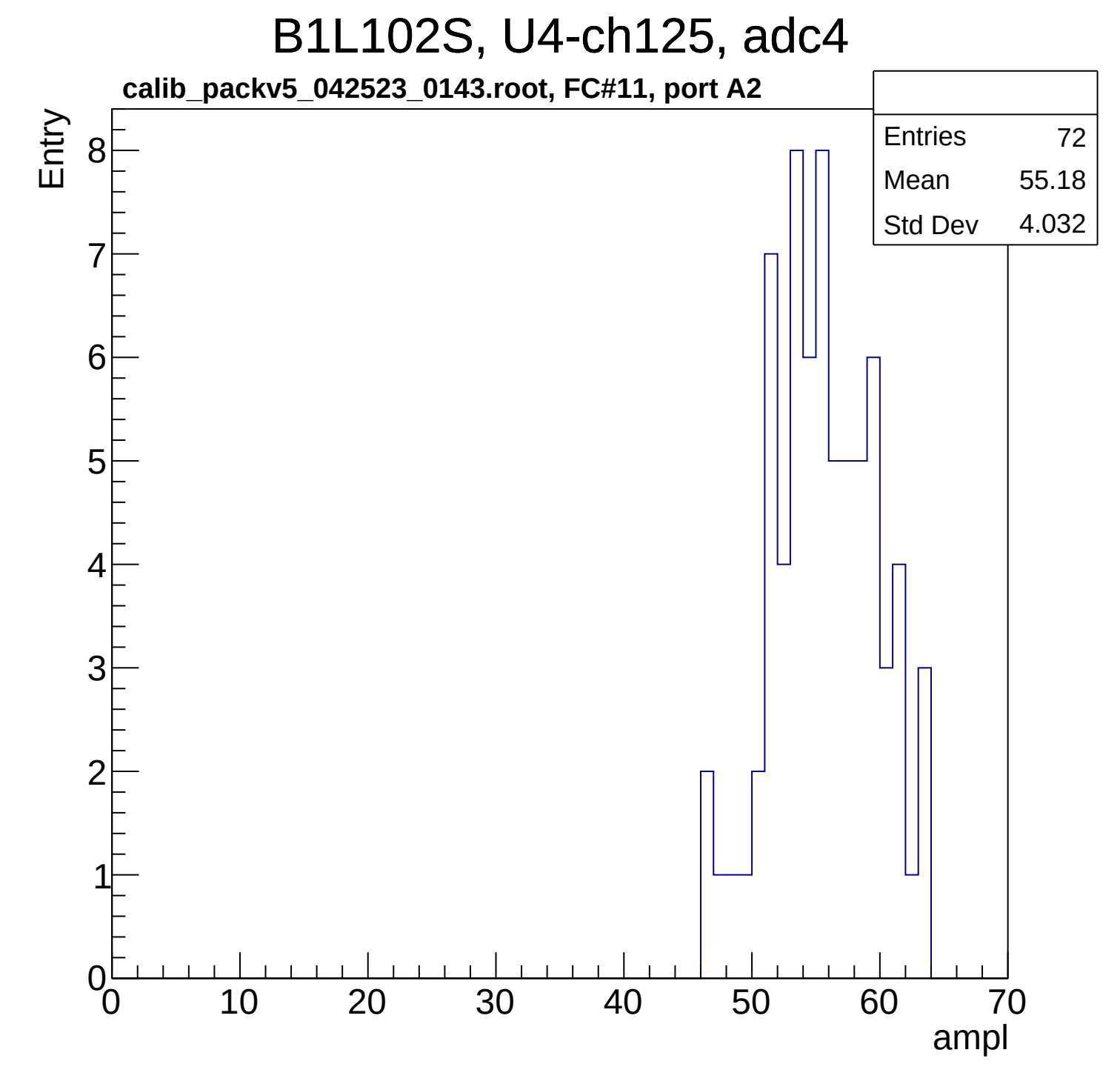

B1L102S, U4-ch125, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 42.19
Std Dev 3.355
Gaus mean : 42.3983
Gaus Width: 3.5397
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L102S, U4-ch125, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 49.34
Std Dev 3.623
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch125, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 72
Mean 55.18
Std Dev 4.032
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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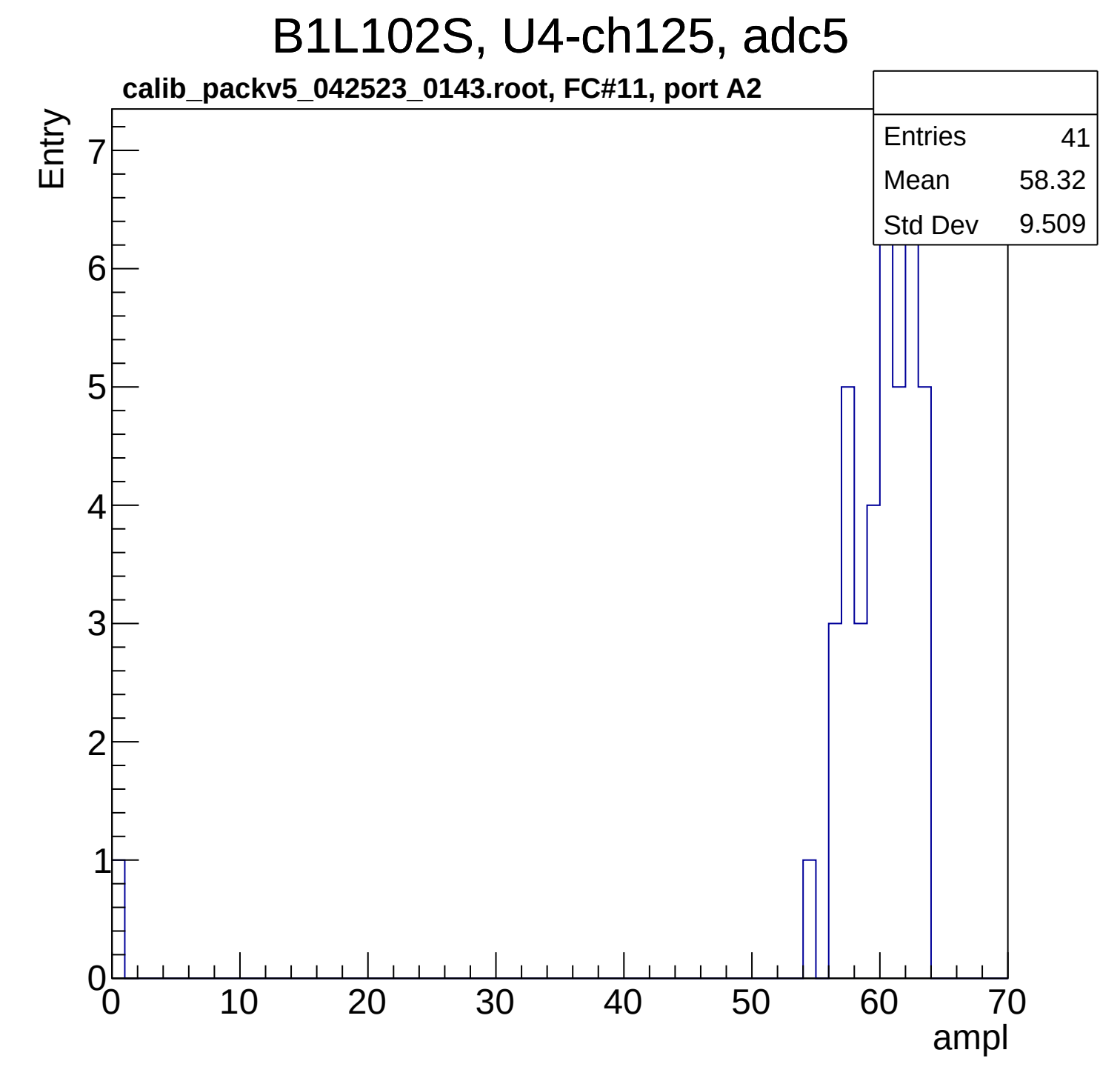
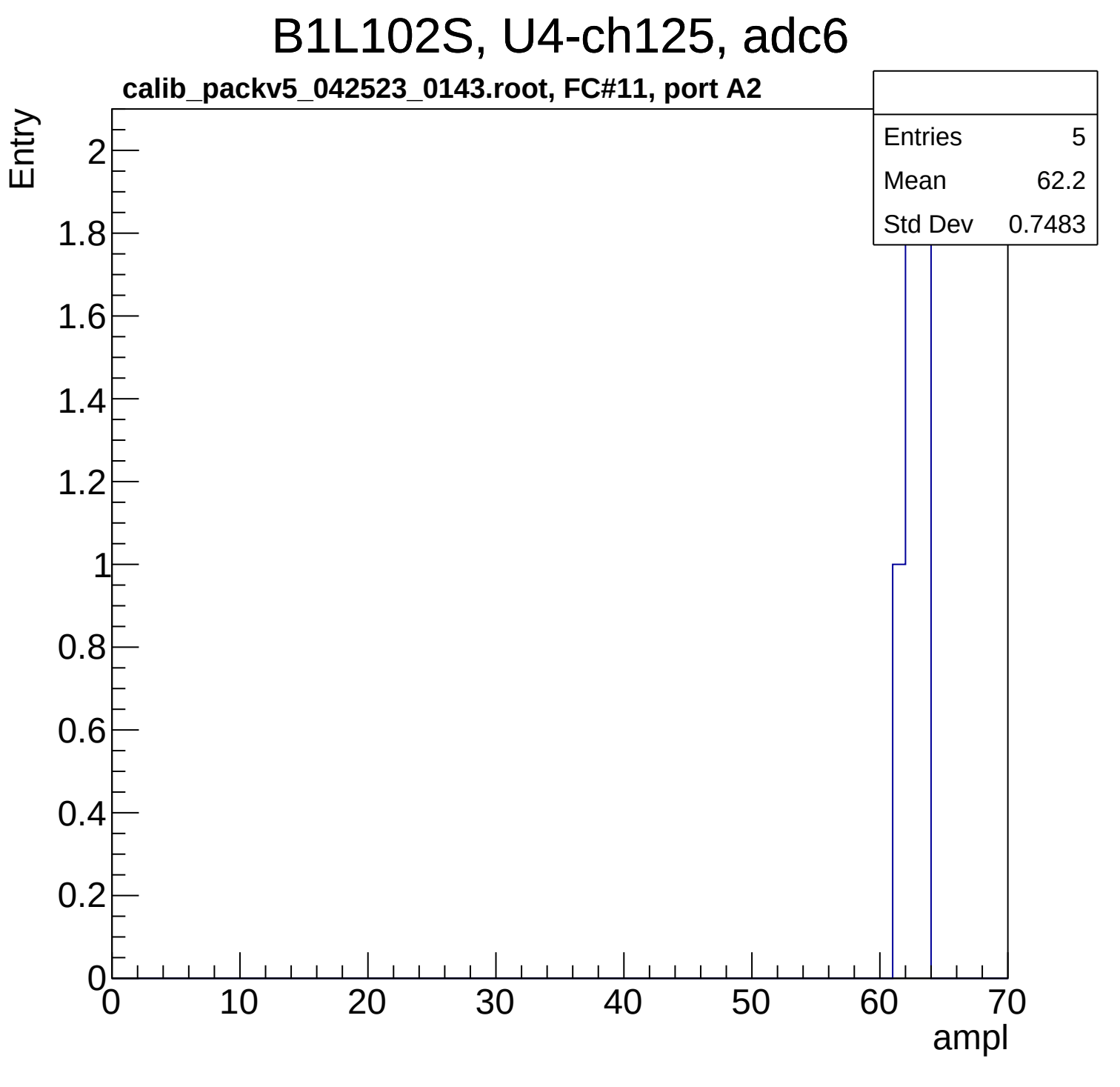
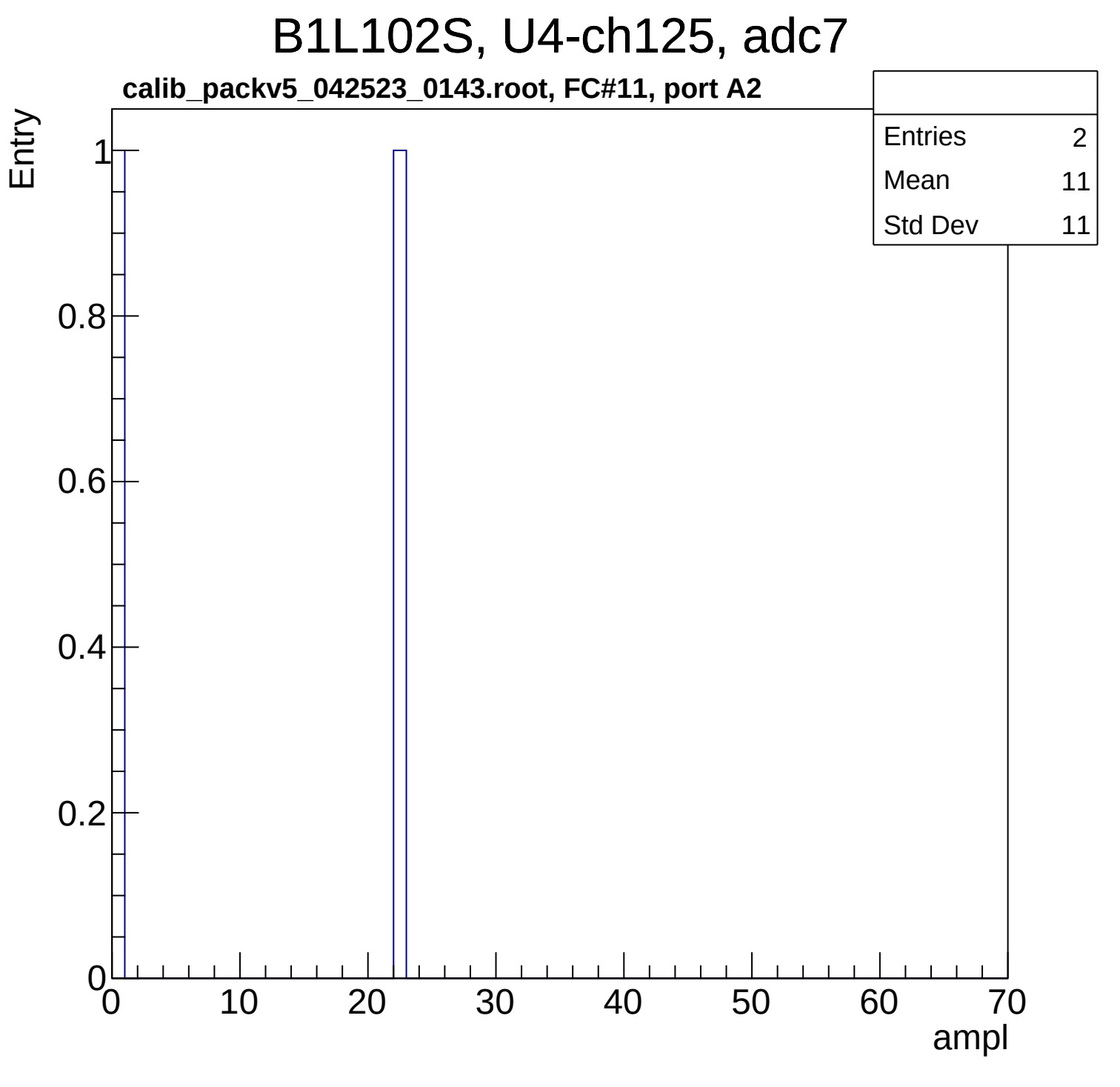
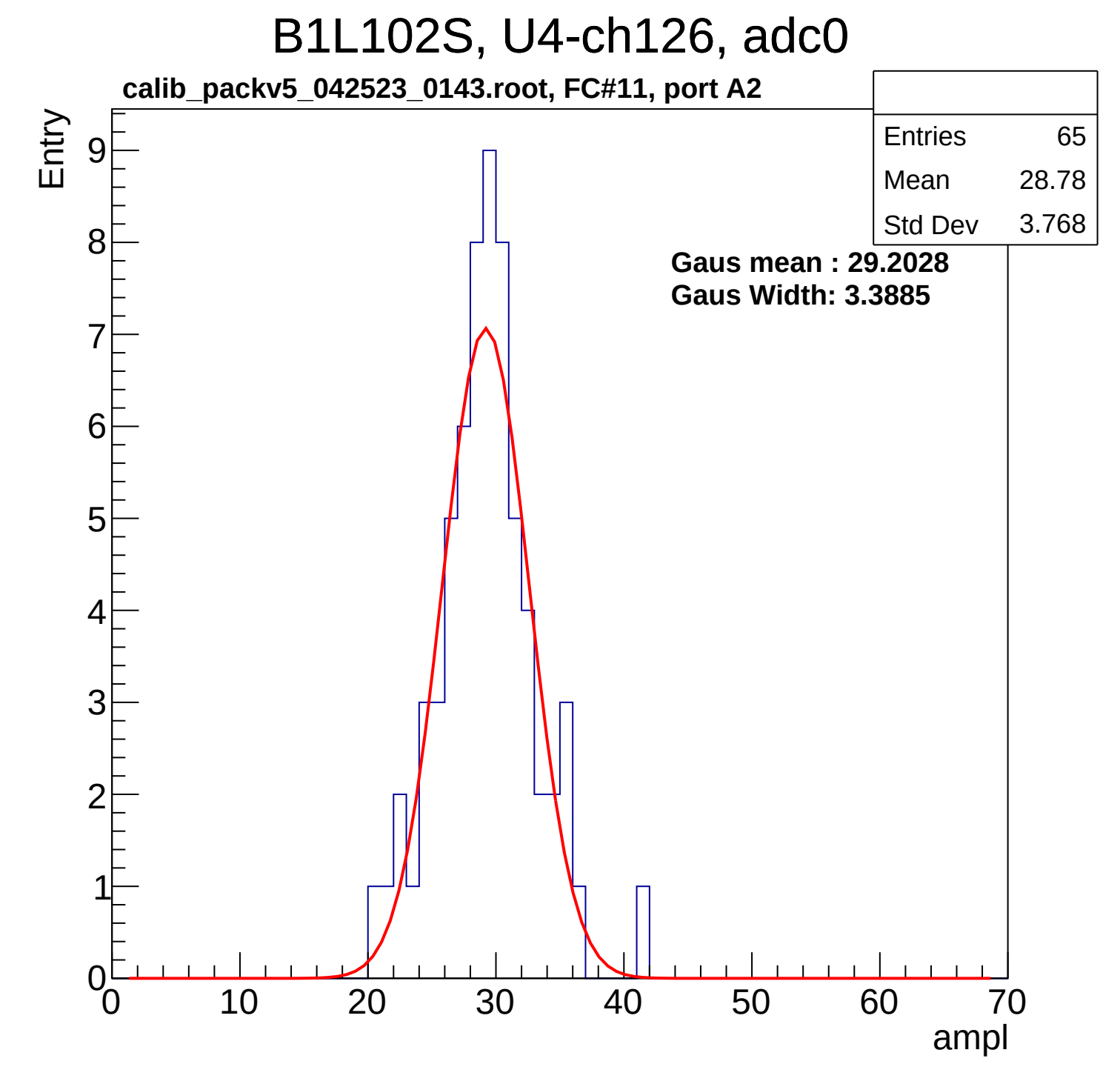

B1L102S, U4-ch125, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 41
Mean 58.32
Std Dev 9.509
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch125, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 5
Mean 62.2
Std Dev 0.7483
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L102S, U4-ch125, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 11
Std Dev 11
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch126, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 65
Mean 28.78
Std Dev 3.768
Gaus mean : 29.2028
Gaus Width: 3.3885
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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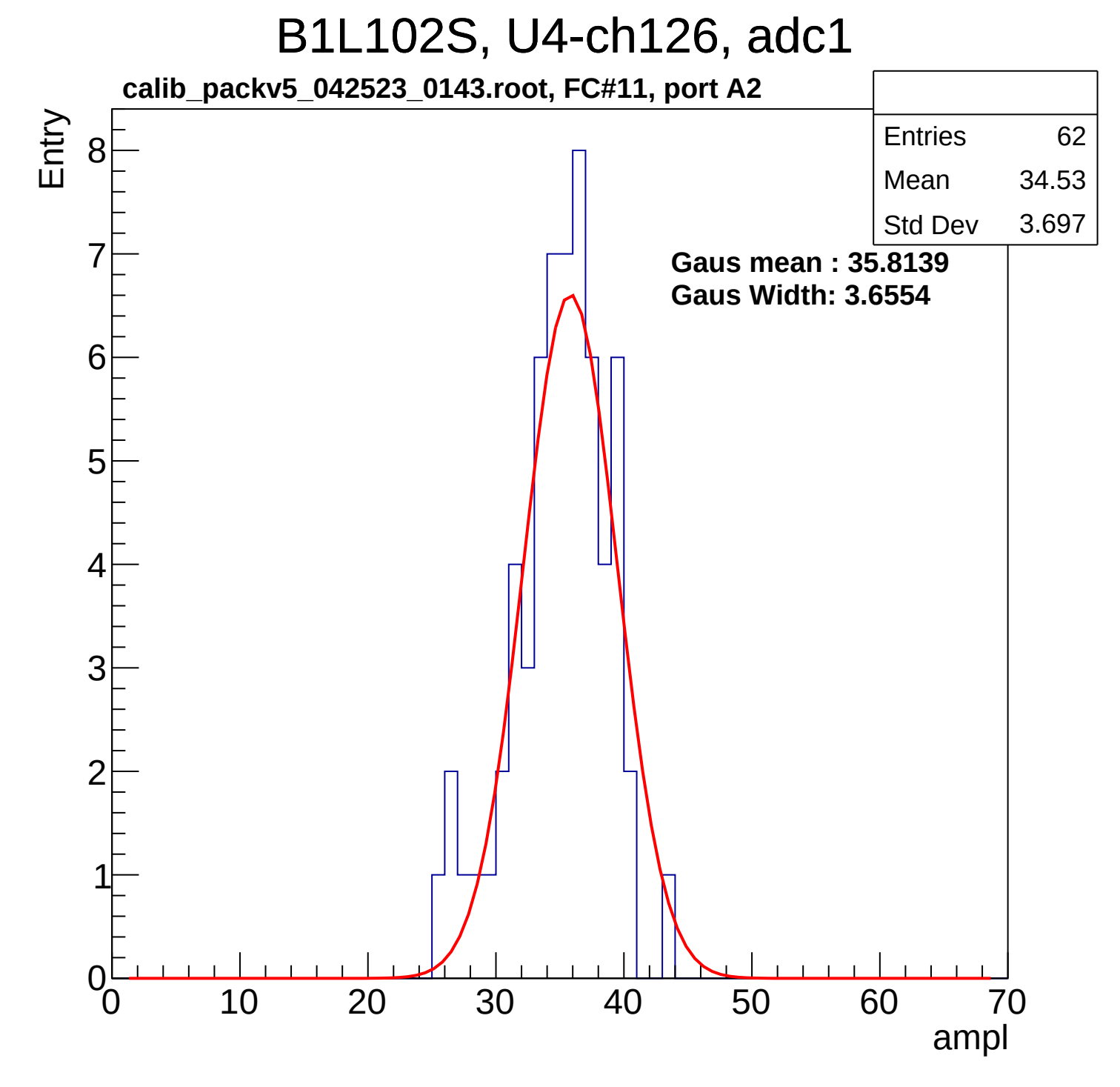
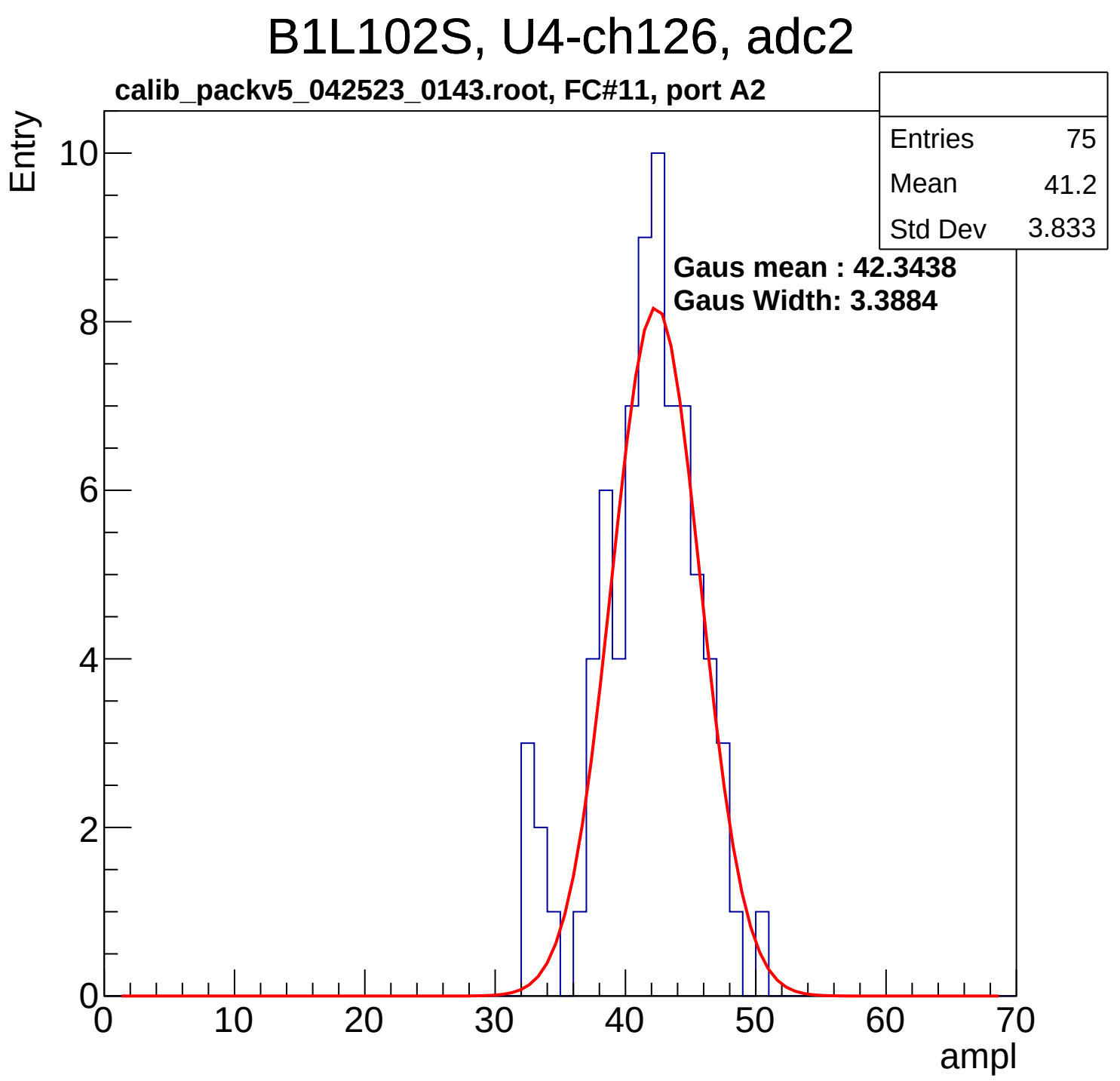

B1L102S, U4-ch126, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 62
Mean 34.53
Std Dev 3.697
Gaus mean : 35.8139
Gaus Width: 3.6554
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch126, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 75
Mean 41.2
Std Dev 3.833
Gaus mean : 42.3438
Gaus Width: 3.3884
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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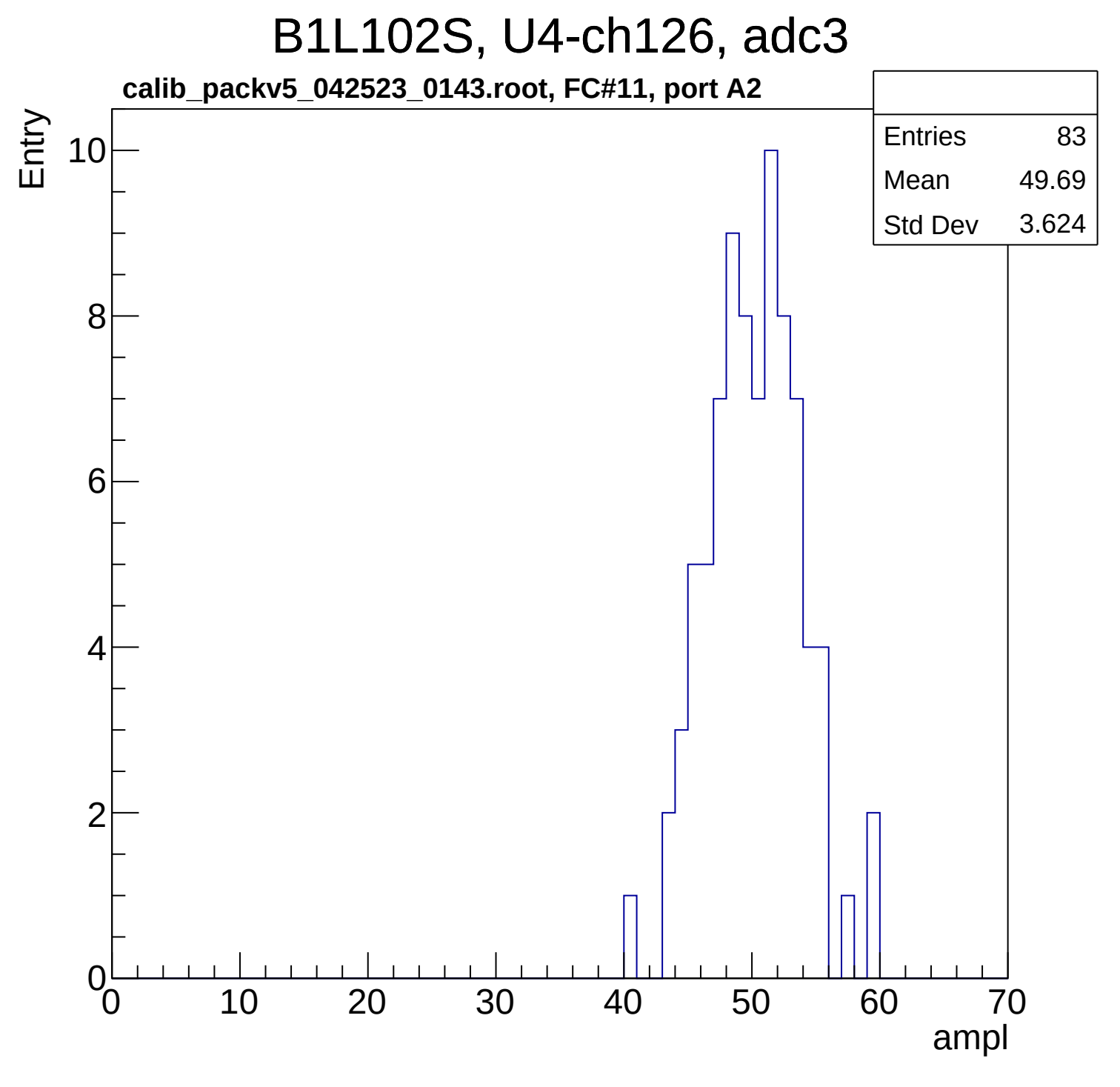
B1L102S, U4-ch126, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 83
Mean 49.69
Std Dev 3.624
Entry
ampl
0
2
4
6
8
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0
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40
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60
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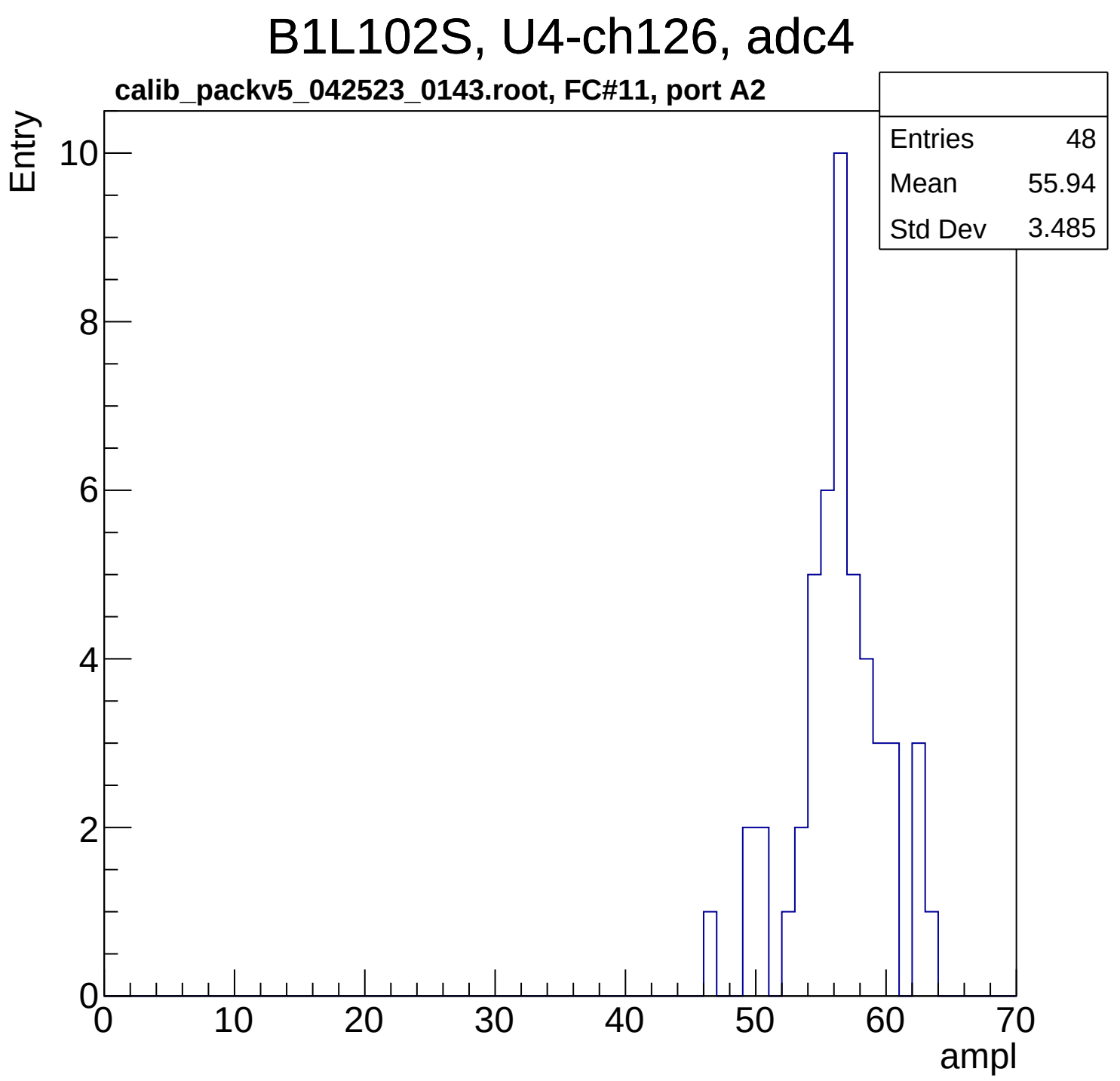
B1L102S, U4-ch126, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 48
Mean 55.94
Std Dev 3.485
Entry
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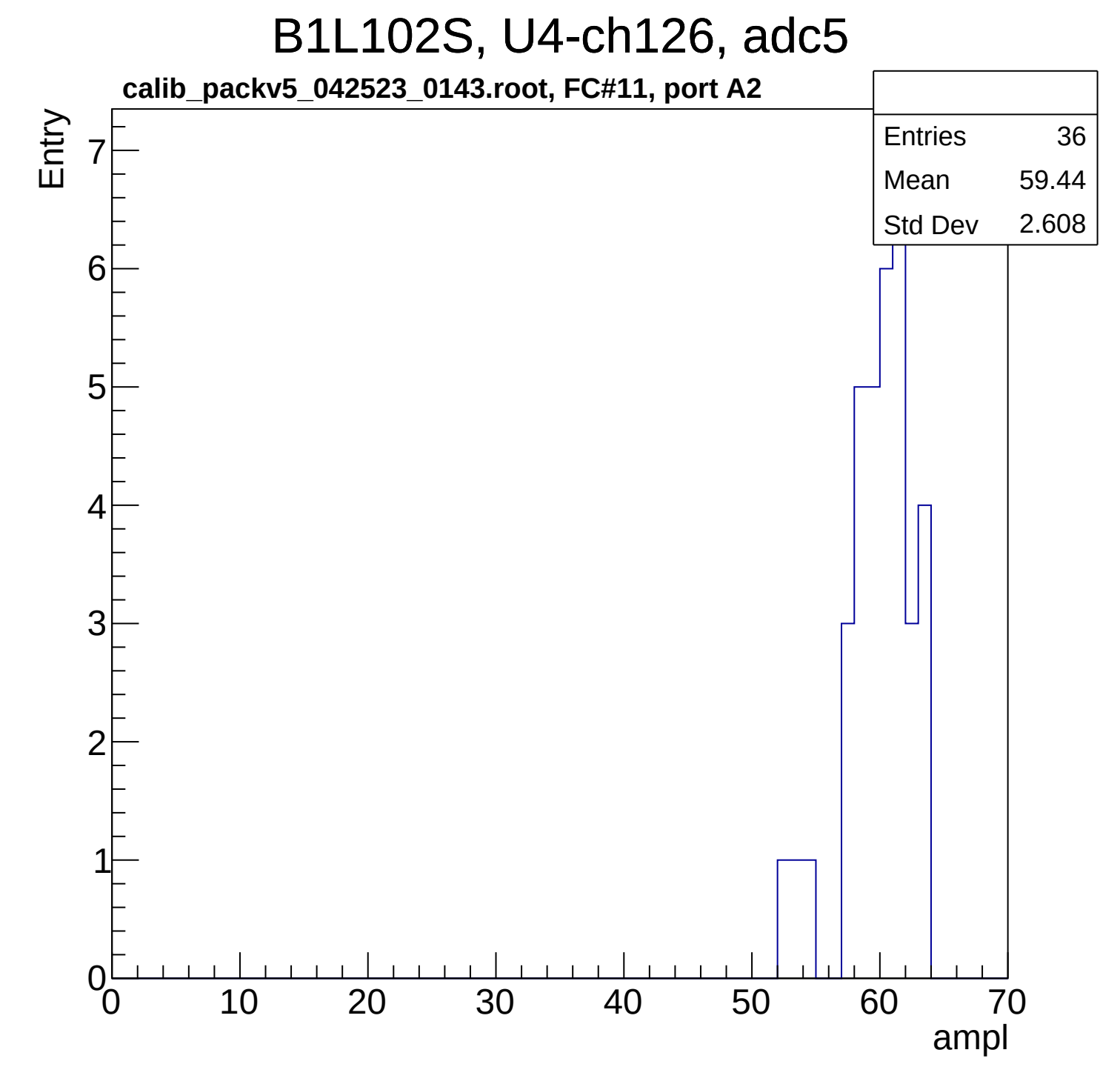
10
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch126, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 36
Mean 59.44
Std Dev 2.608
Entry
ampl
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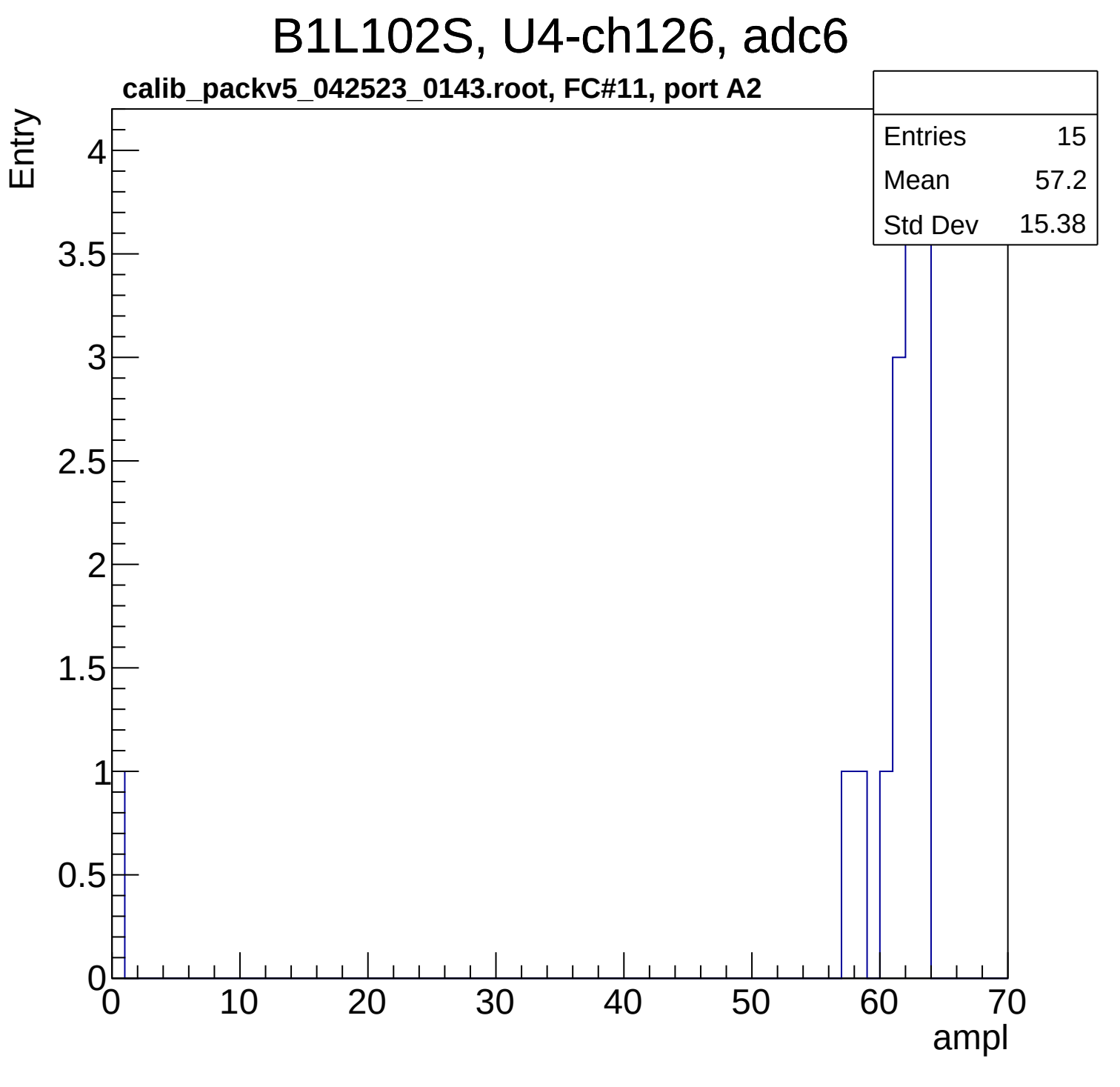
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L102S, U4-ch126, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 15
Mean 57.2
Std Dev 15.38
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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20
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40
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60
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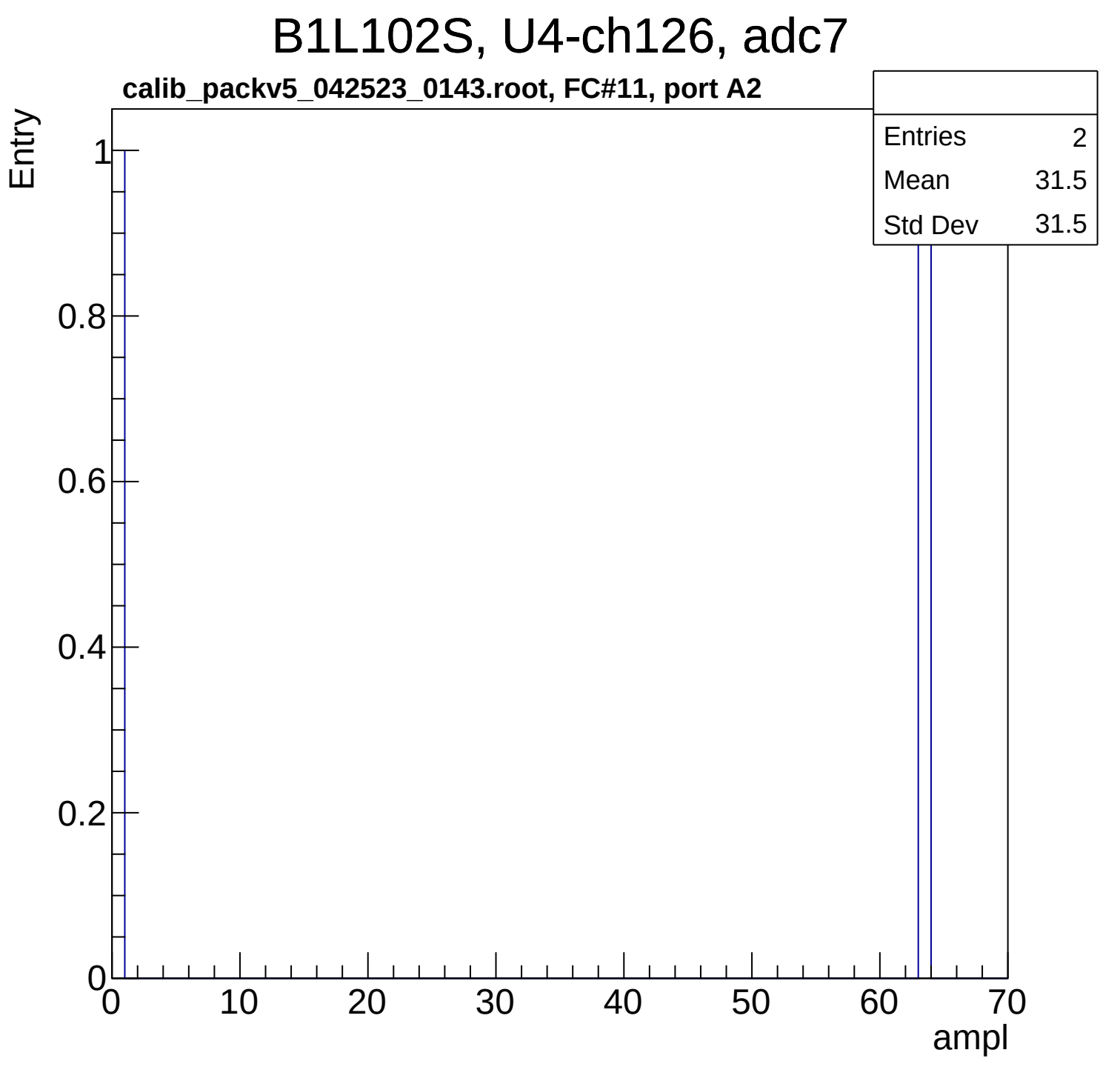
B1L102S, U4-ch126, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
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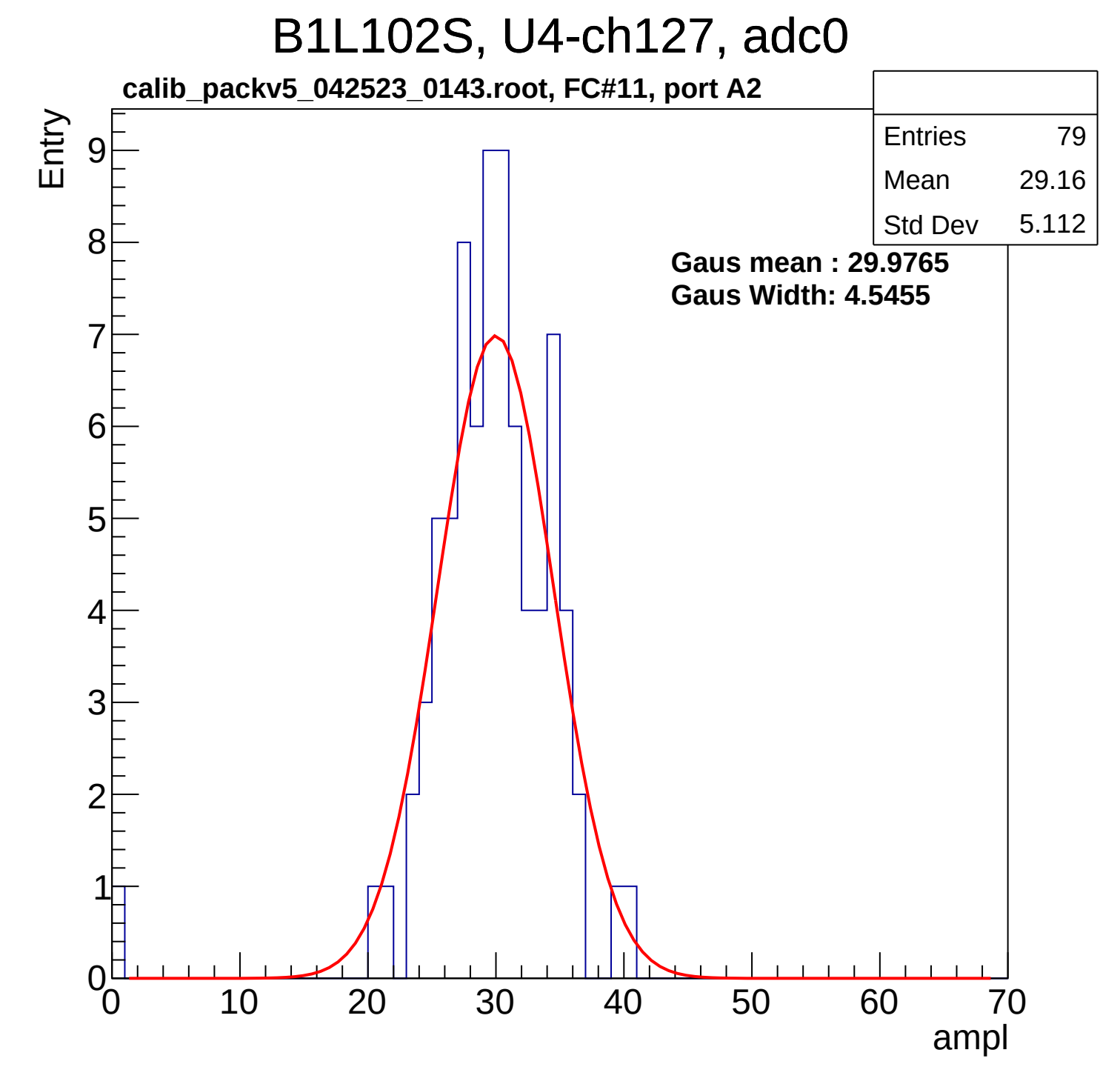
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch127, adc0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 79
Mean 29.16
Std Dev 5.112
Gaus mean : 29.9765
Gaus Width: 4.5455
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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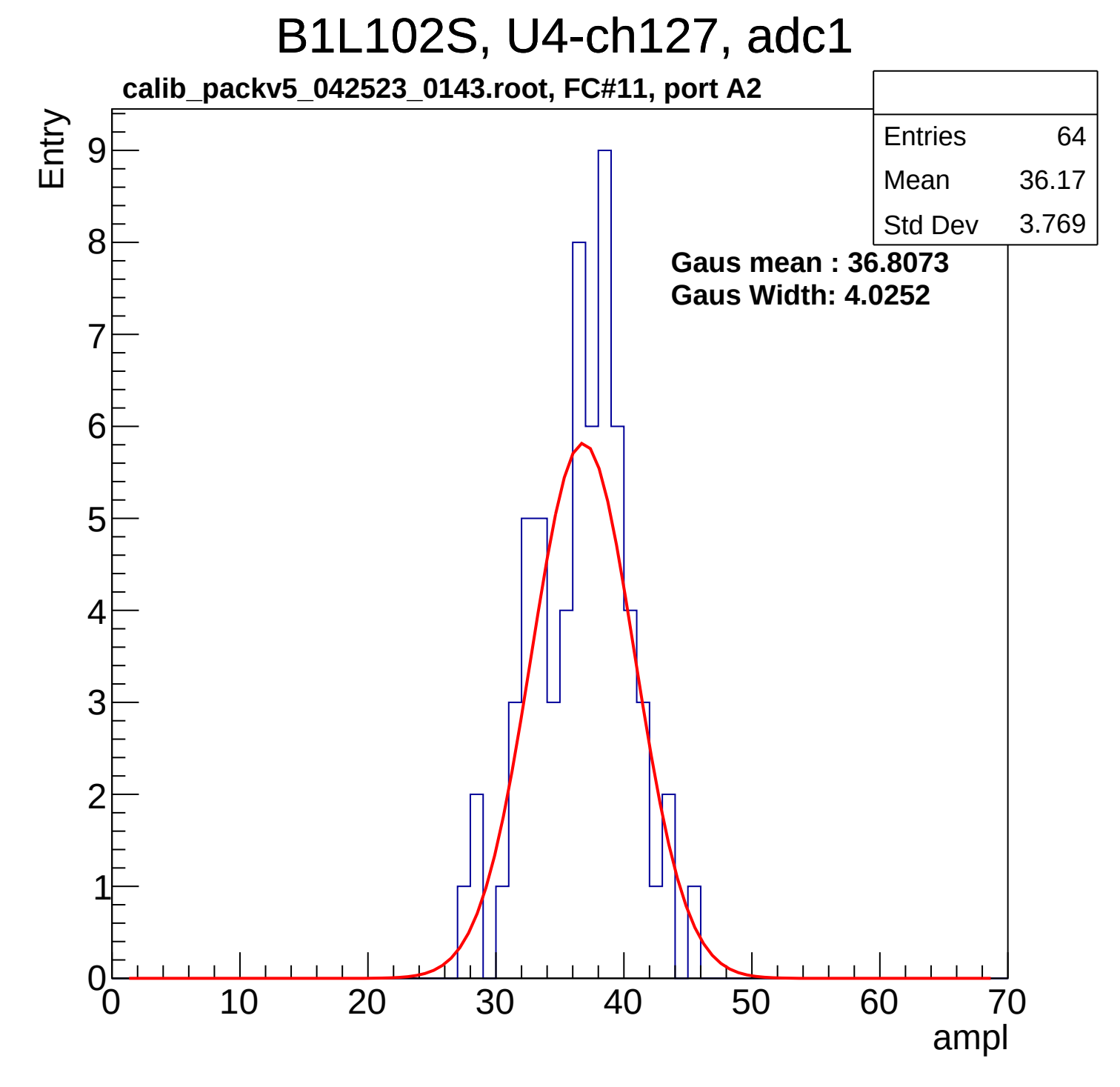
B1L102S, U4-ch127, adc1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 64
Mean 36.17
Std Dev 3.769
Gaus mean : 36.8073
Gaus Width: 4.0252
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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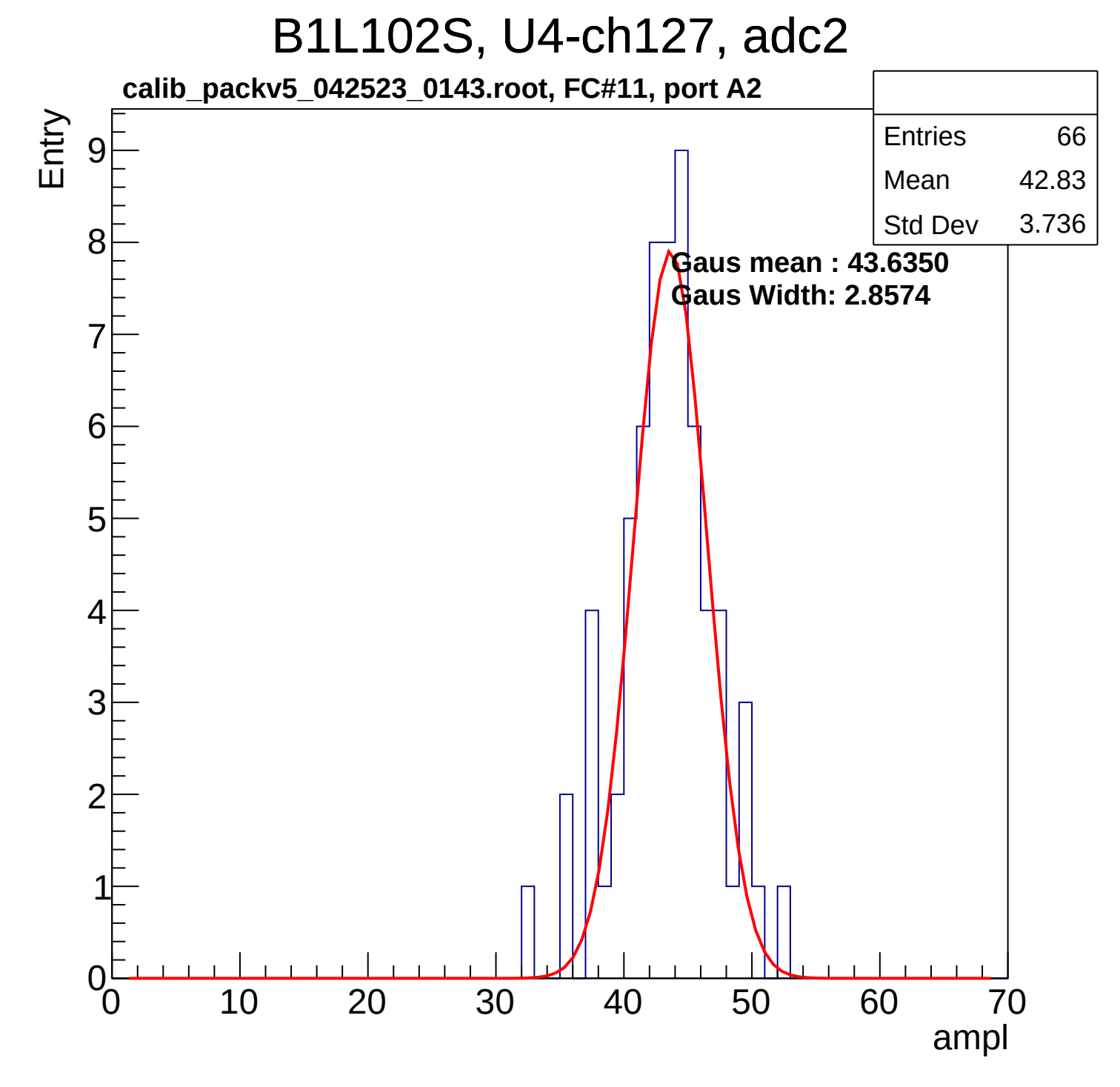
B1L102S, U4-ch127, adc2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 66
Mean 42.83
Std Dev 3.736
Gaus mean : 43.6350
Gaus Width: 2.8574
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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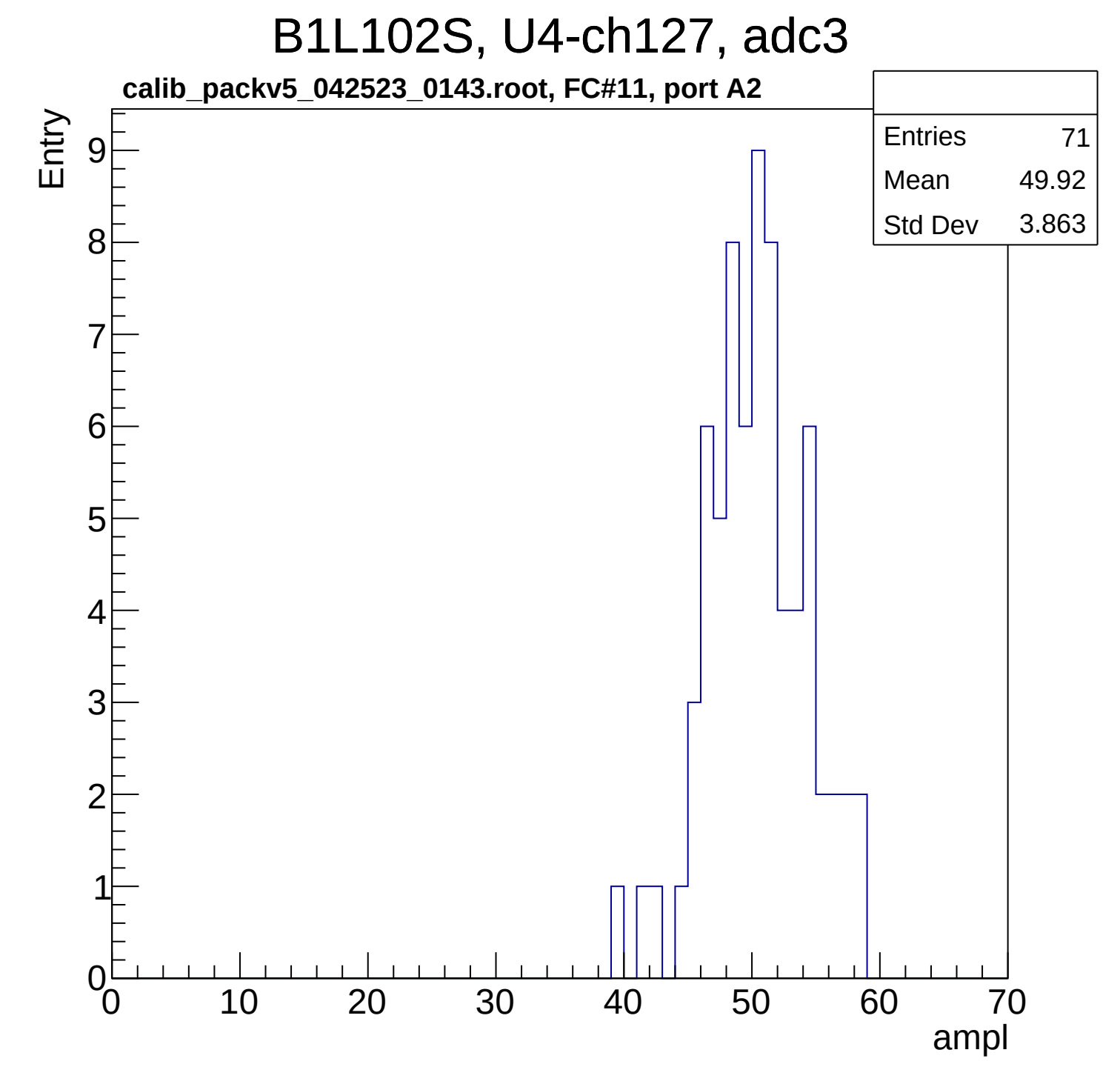
B1L102S, U4-ch127, adc3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 71
Mean 49.92
Std Dev 3.863
Entry
ampl
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3
4
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7
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60
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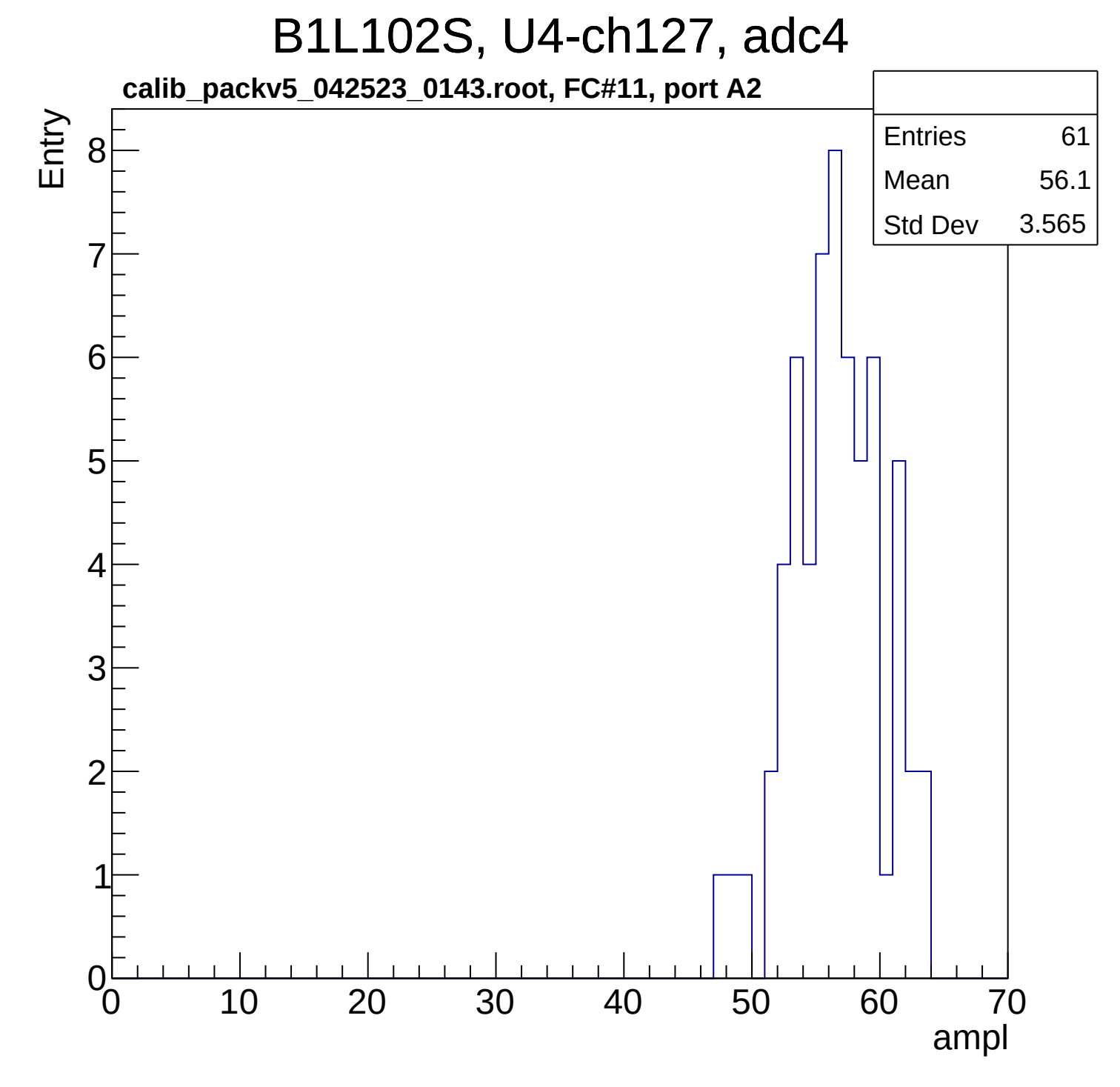
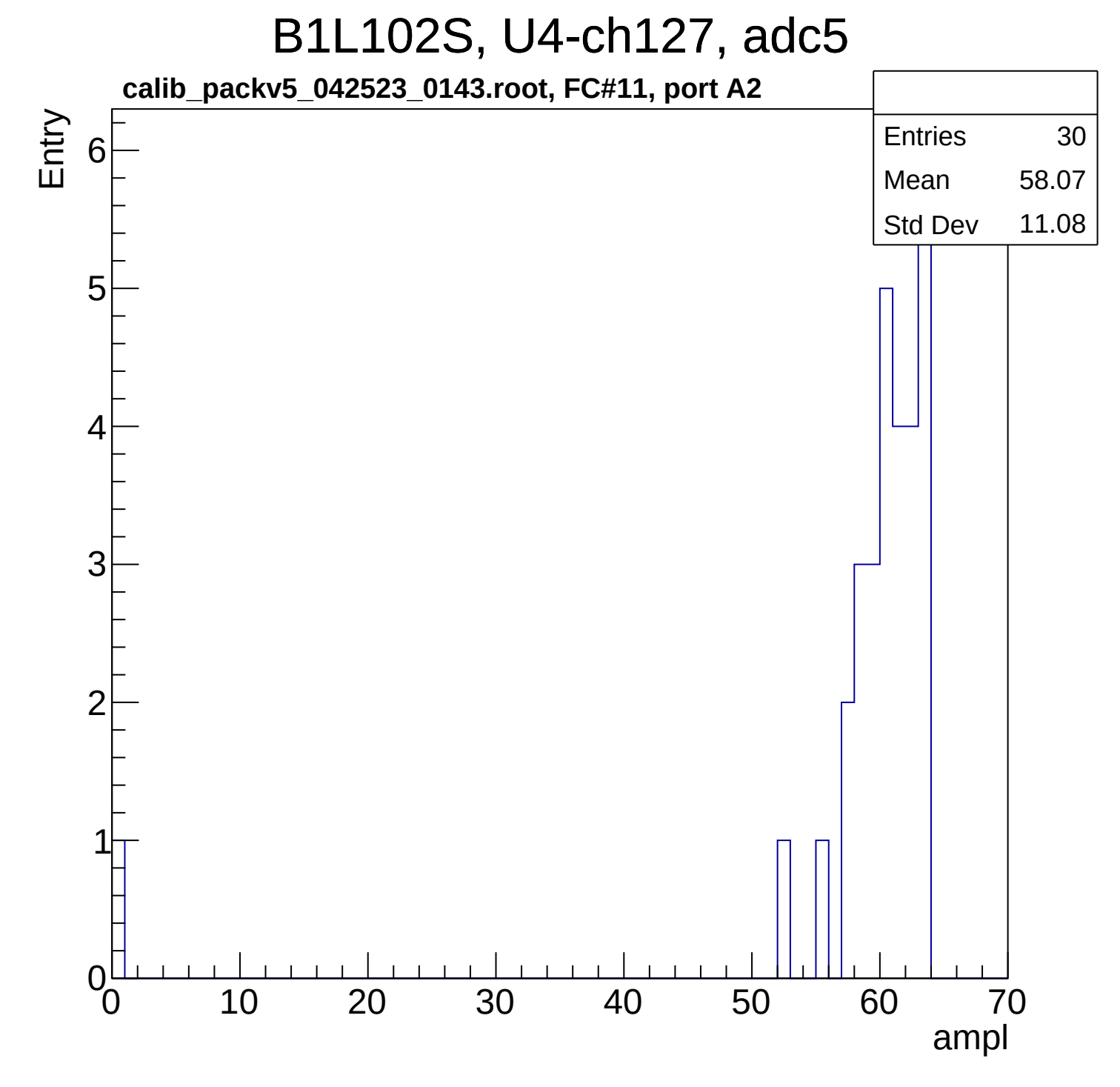
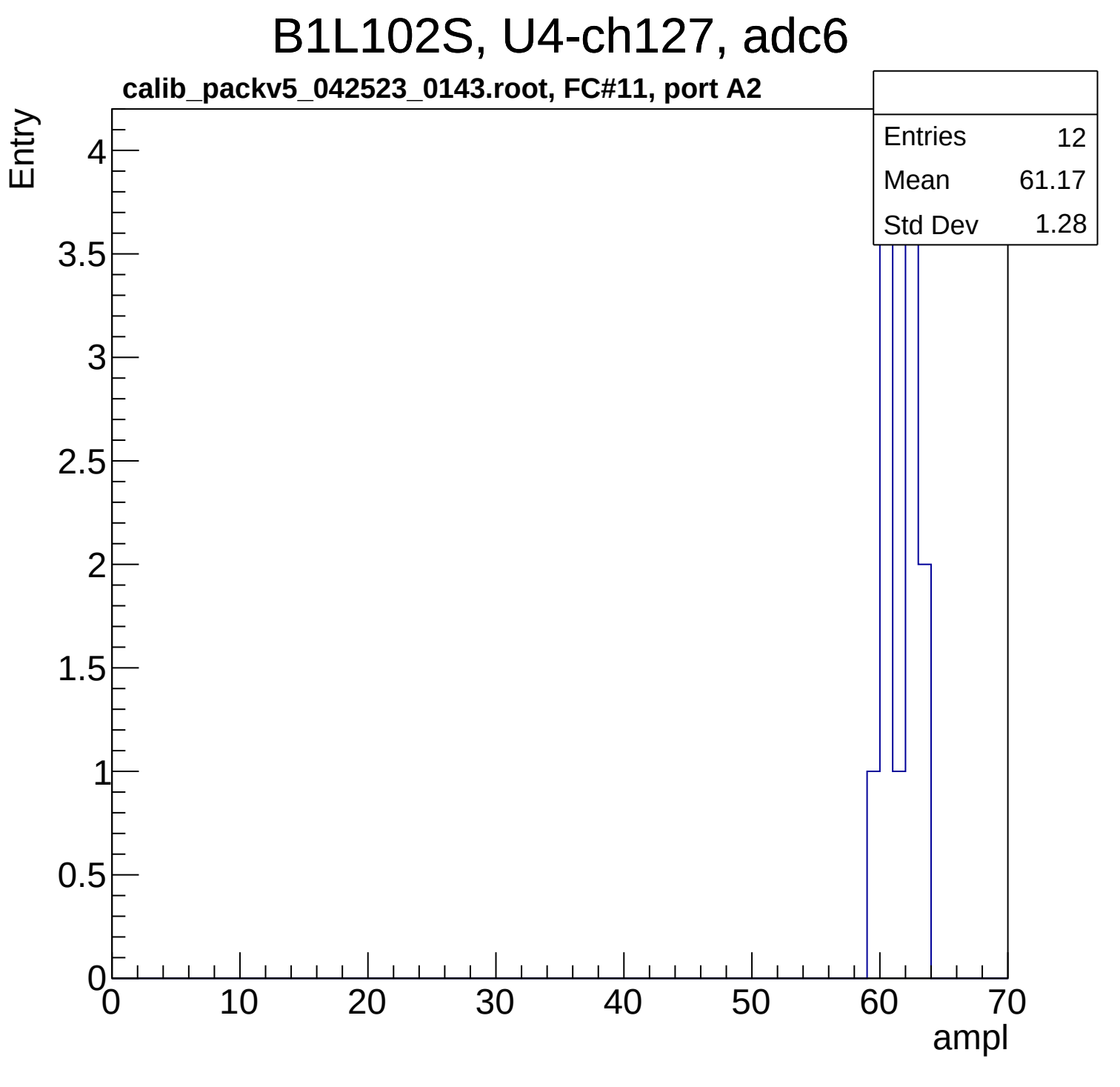
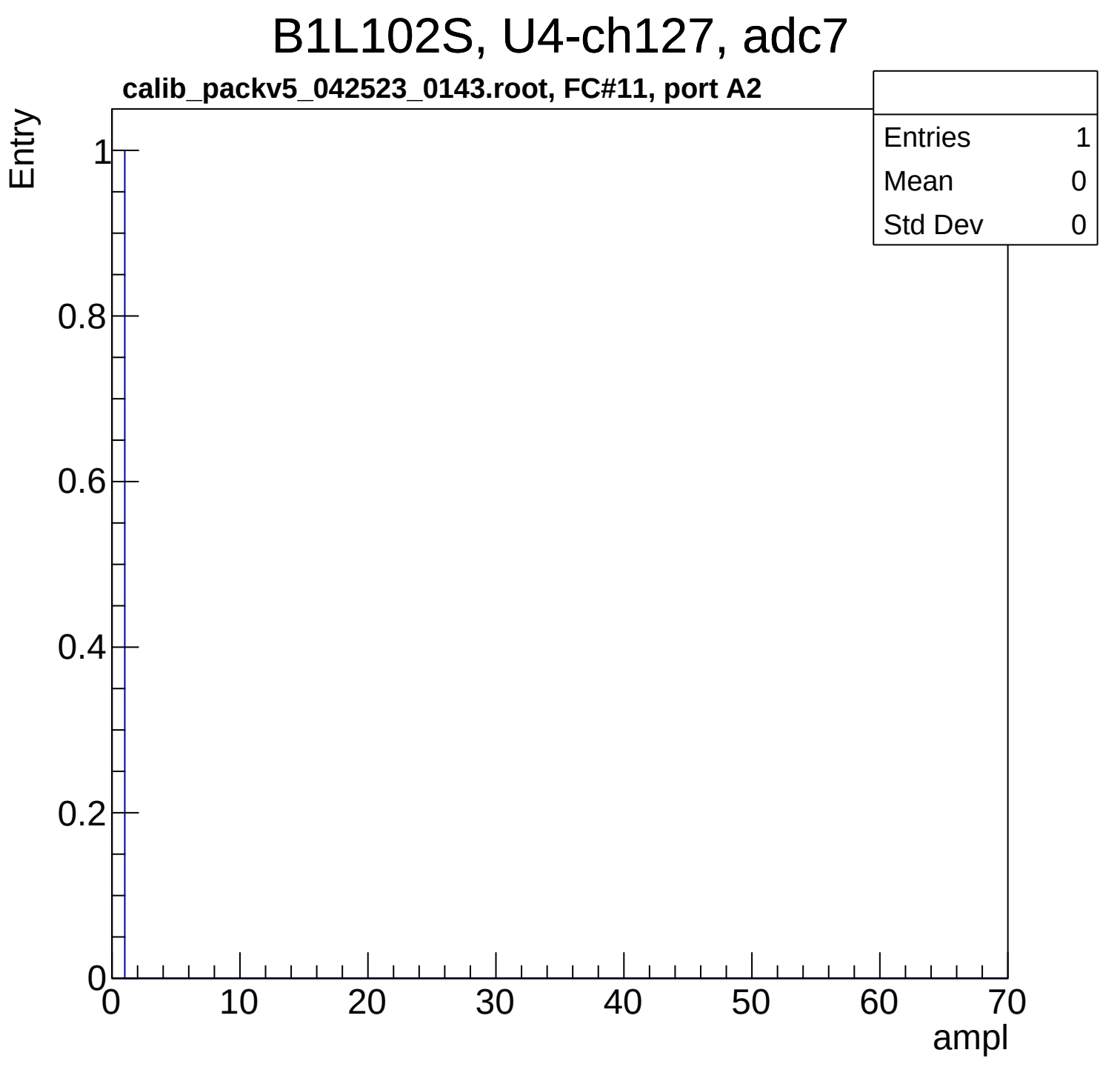
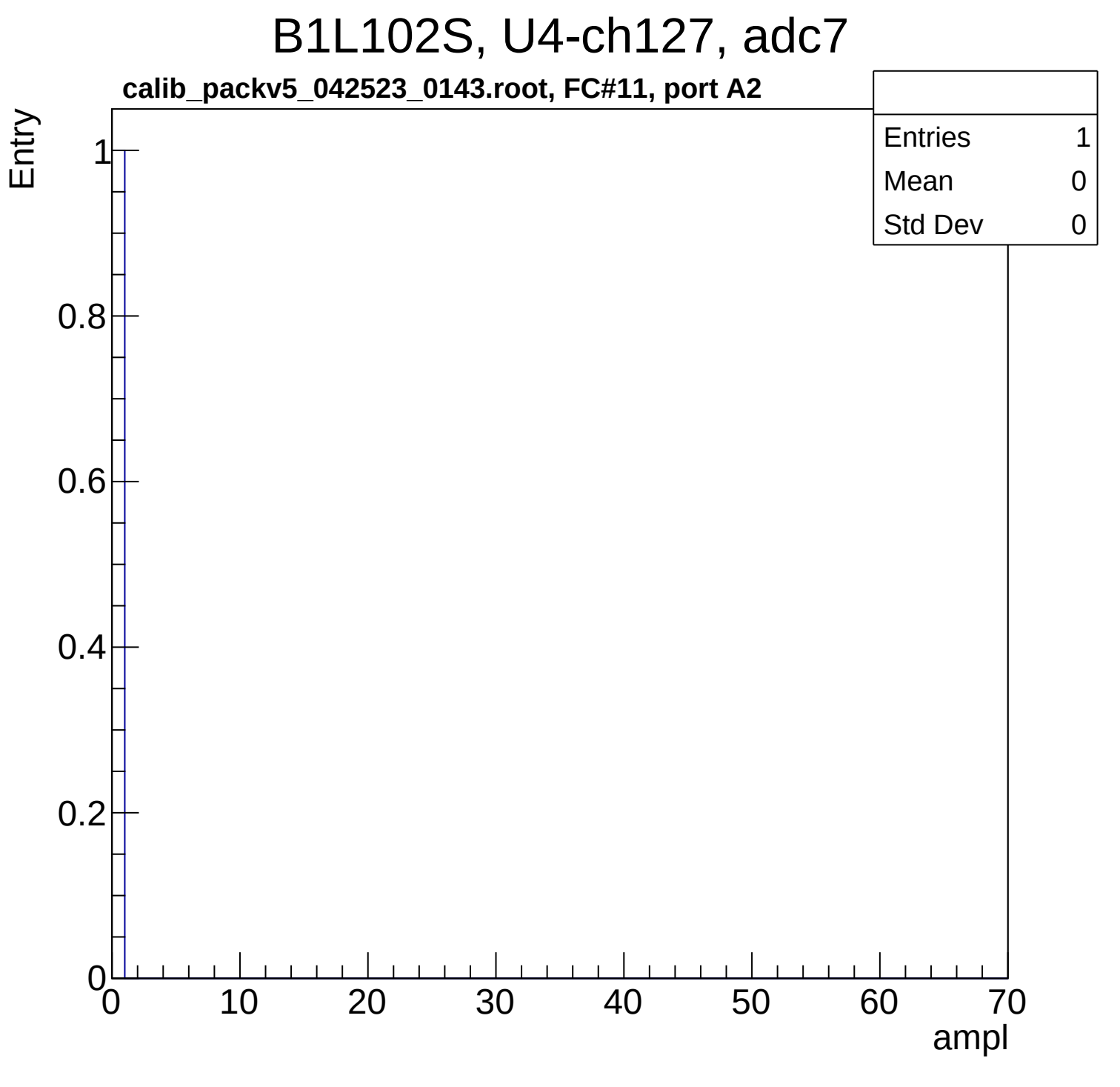

B1L102S, U4-ch127, adc4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 61
Mean 56.1
Std Dev 3.565
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L102S, U4-ch127, adc5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 30
Mean 58.07
Std Dev 11.08
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch127, adc6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 12
Mean 61.17
Std Dev 1.28
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L102S, U4-ch127, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L102S, U4-ch127, adc7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl