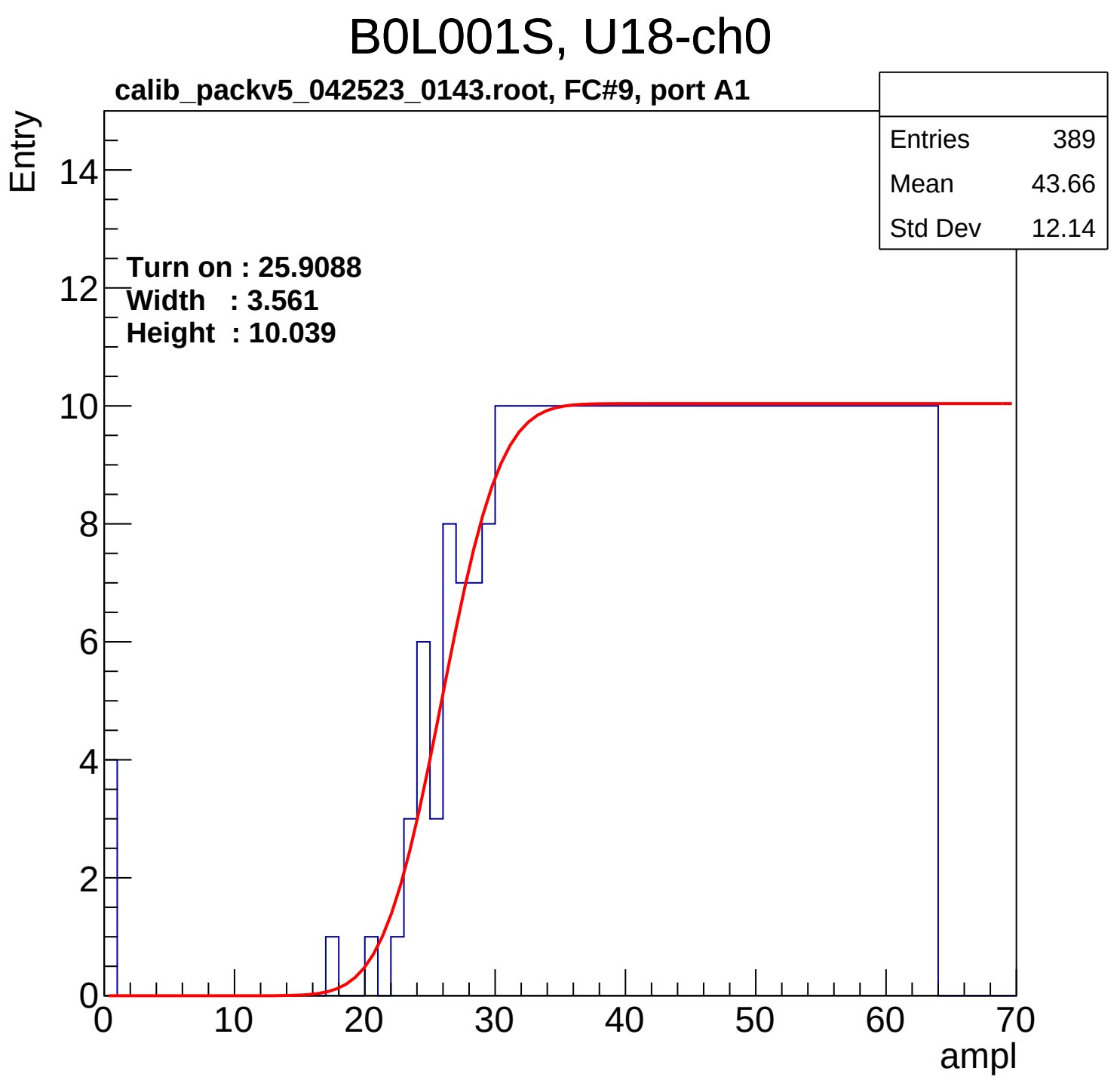
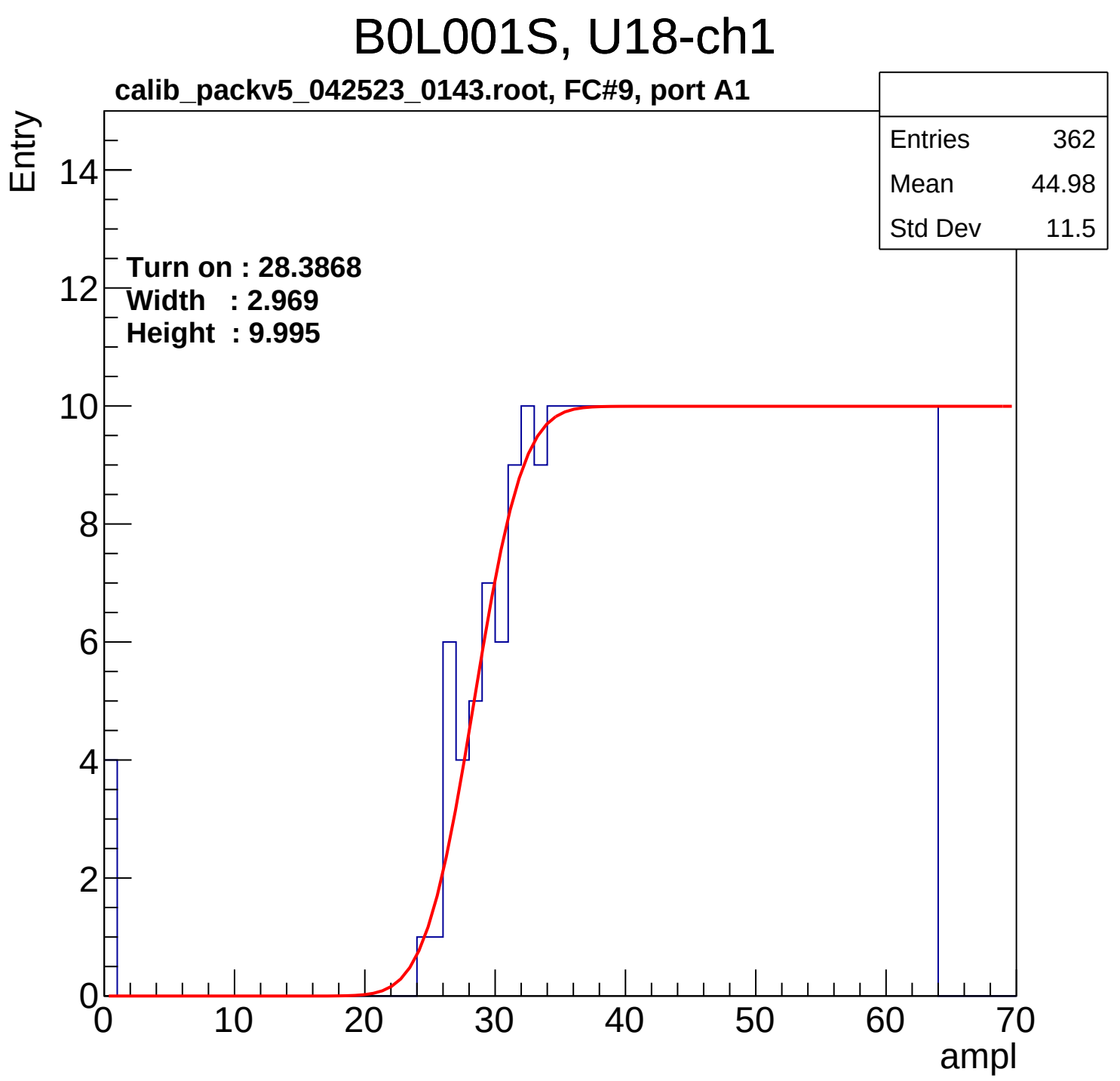
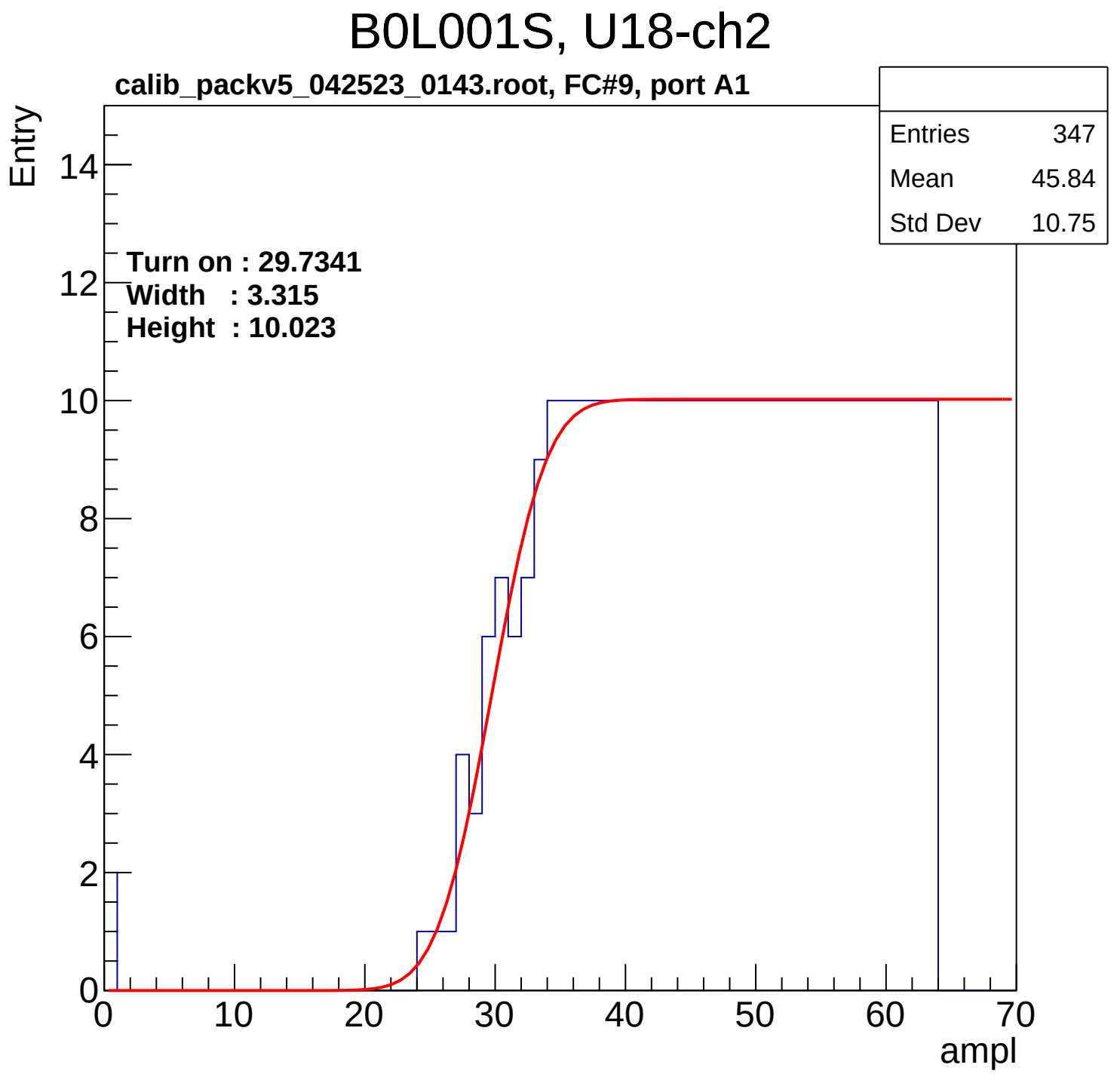
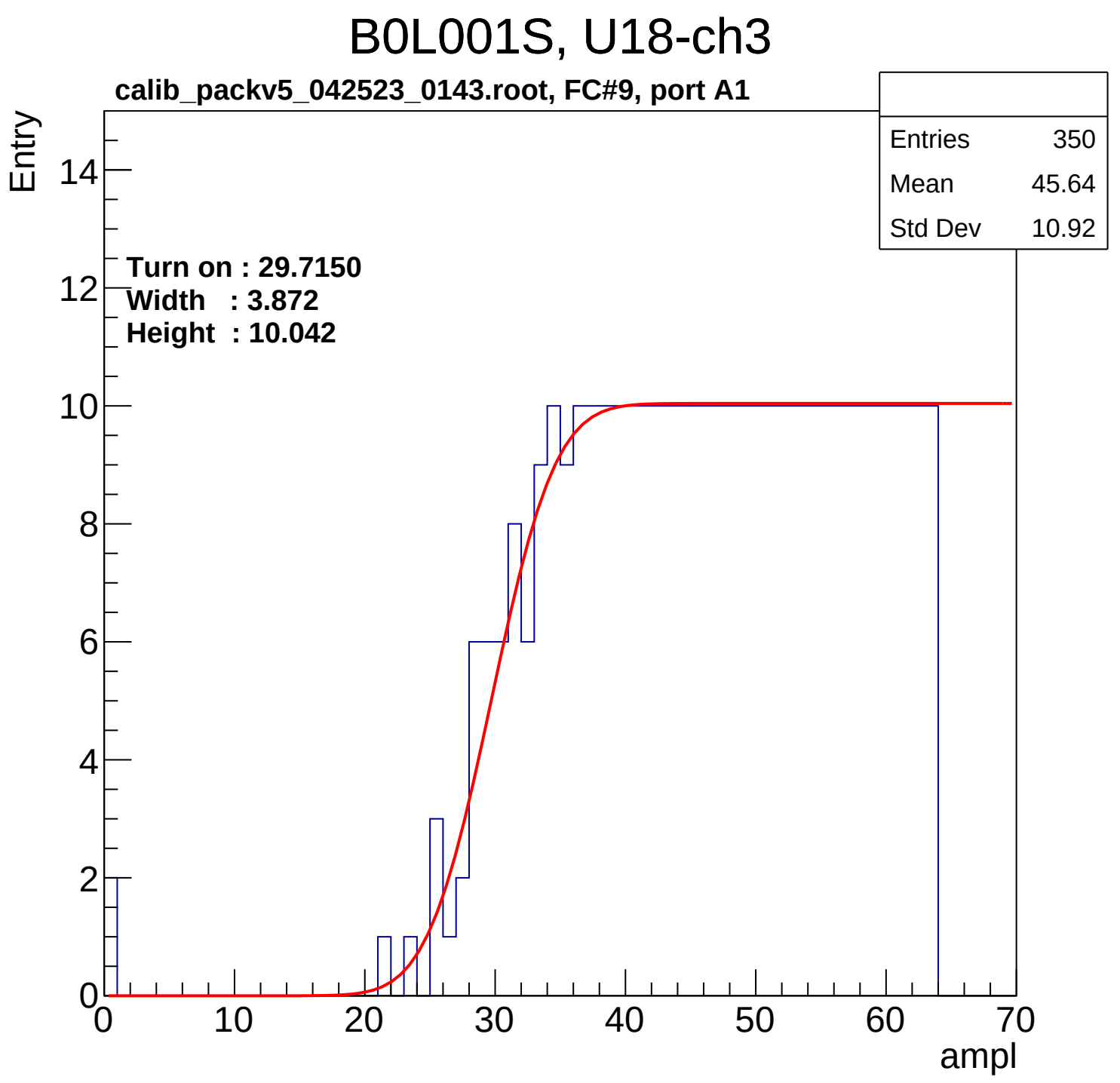
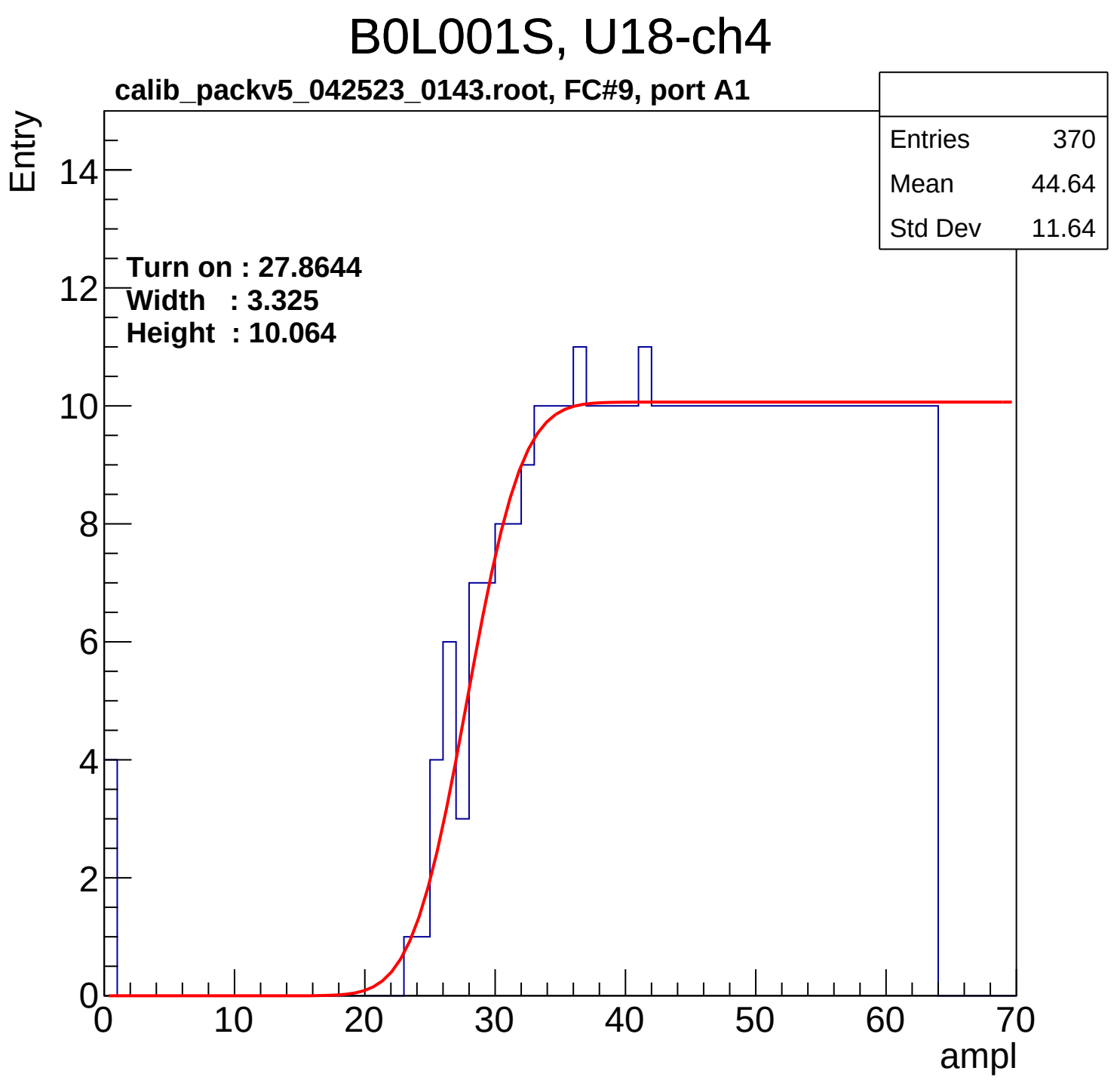
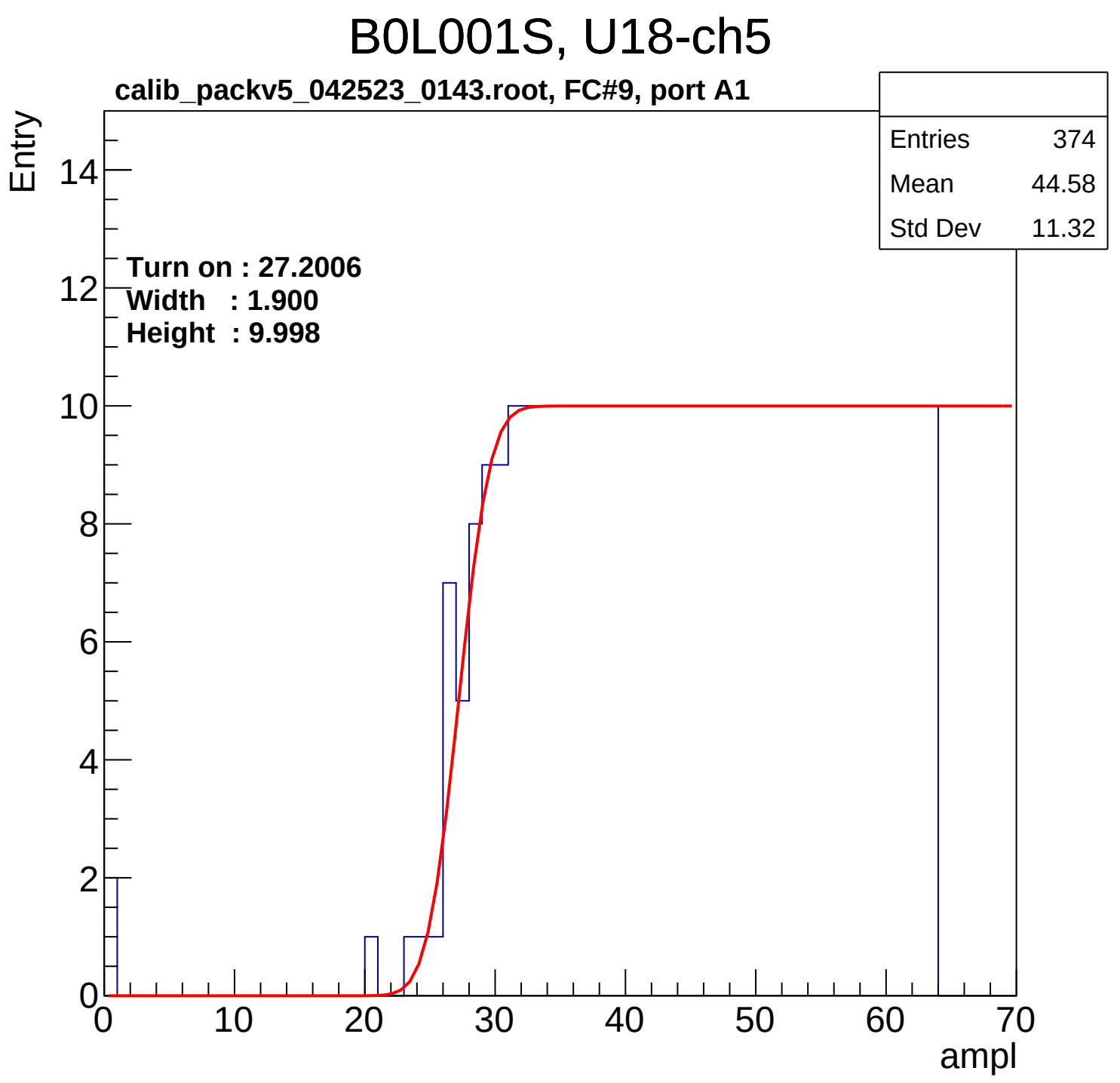

B0L001S, U18-ch0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 389
Mean 43.66
Std Dev 12.14
Turn on : 25.9088
Width : 3.561
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

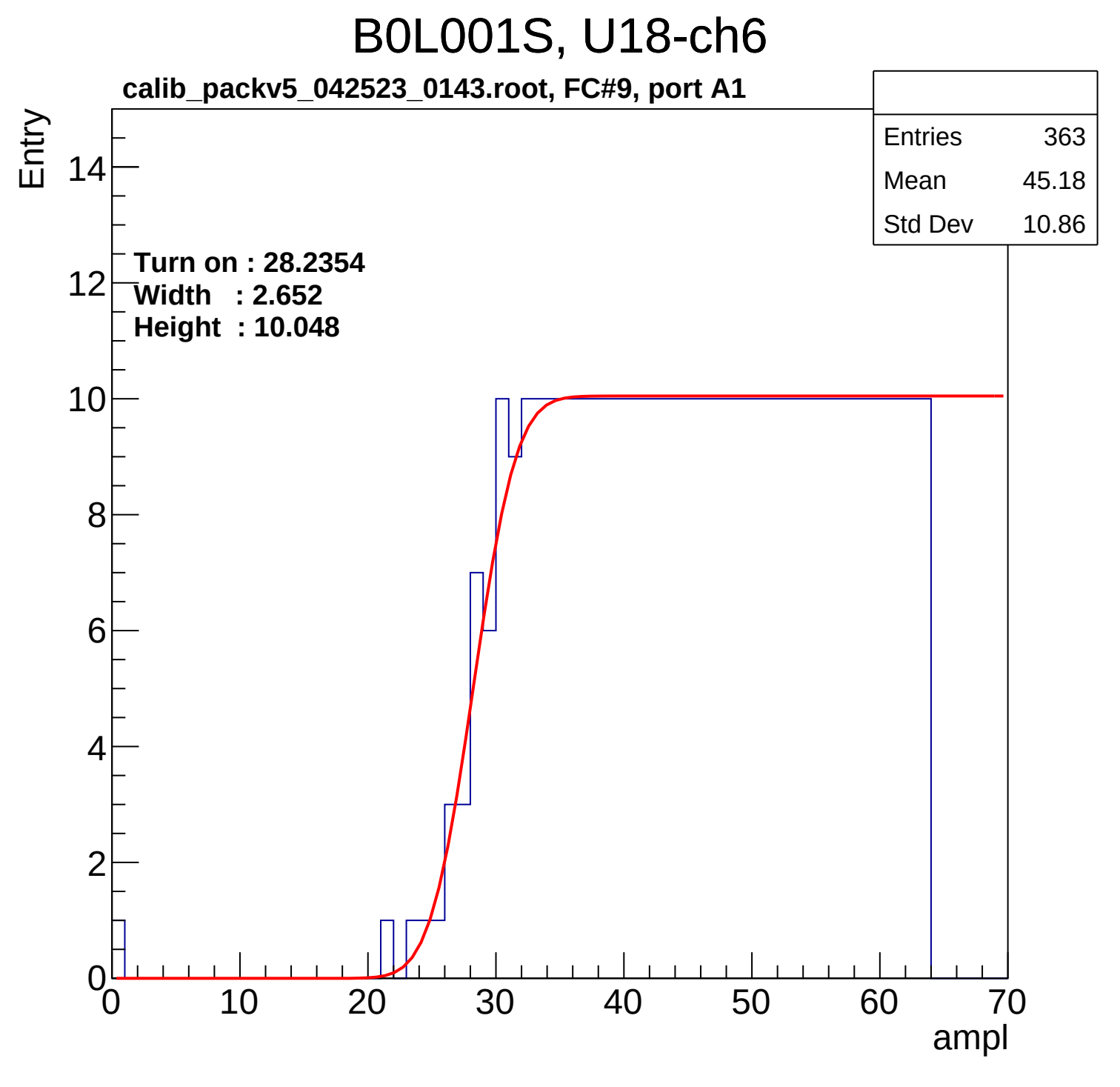

B0L001S, U18-ch1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 44.98
Std Dev 11.5
Turn on : 28.3868
Width : 2.969
Height : 9.995
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

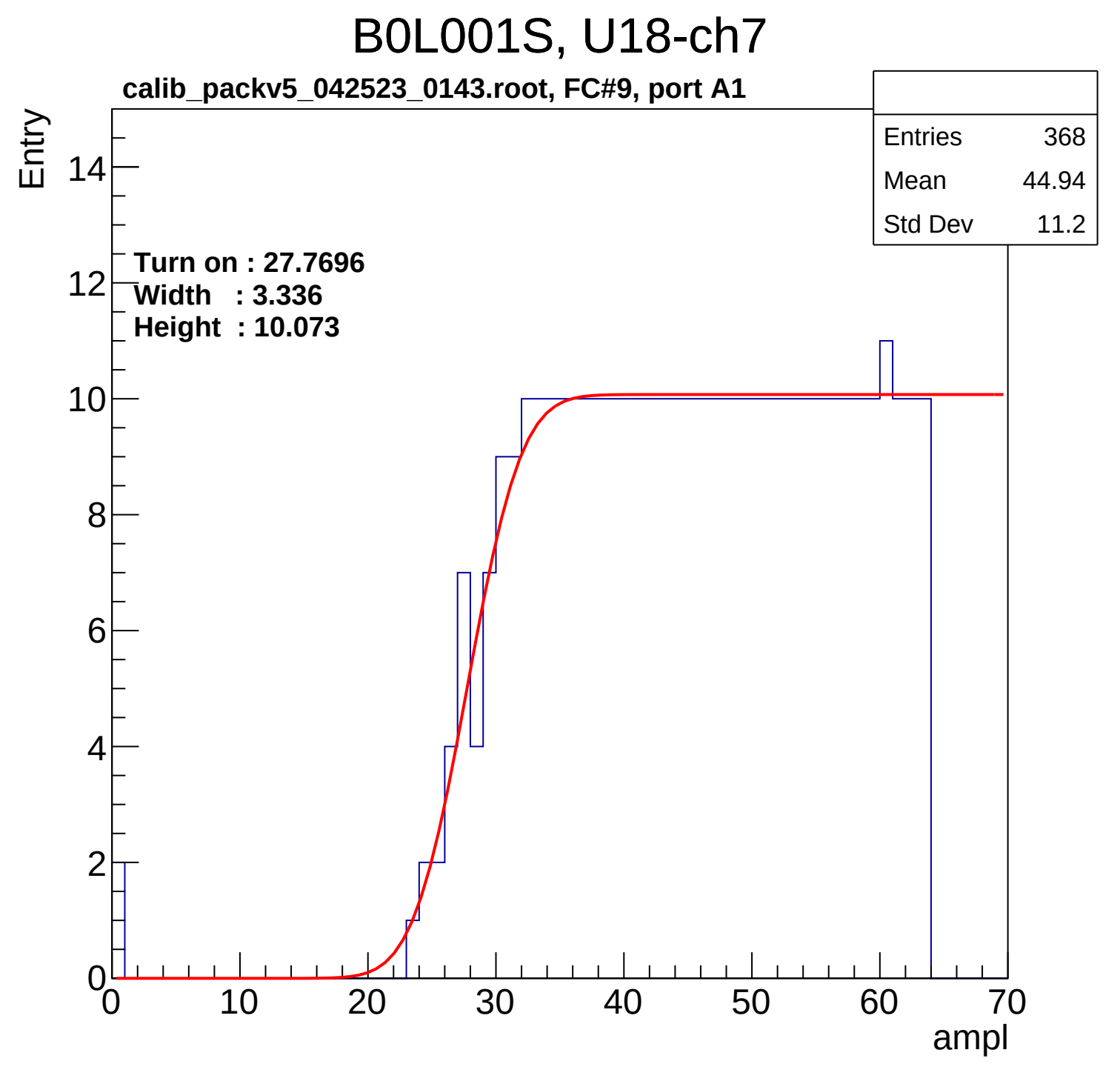

B0L001S, U18-ch2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 347
Mean 45.84
Std Dev 10.75
Turn on : 29.7341
Width : 3.315
Height : 10.023
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

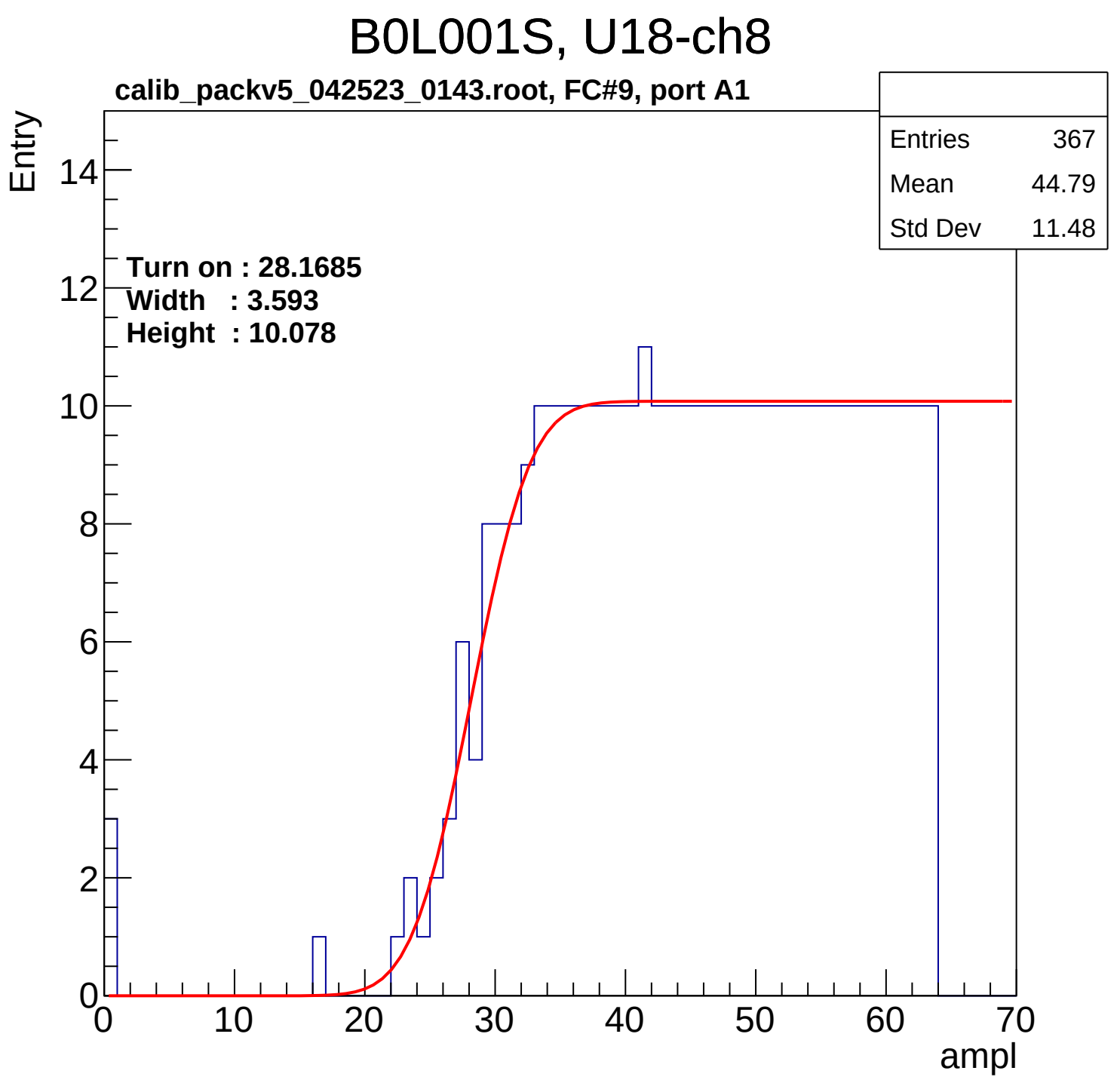

B0L001S, U18-ch3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.64
Std Dev 10.92
Turn on : 29.7150
Width : 3.872
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

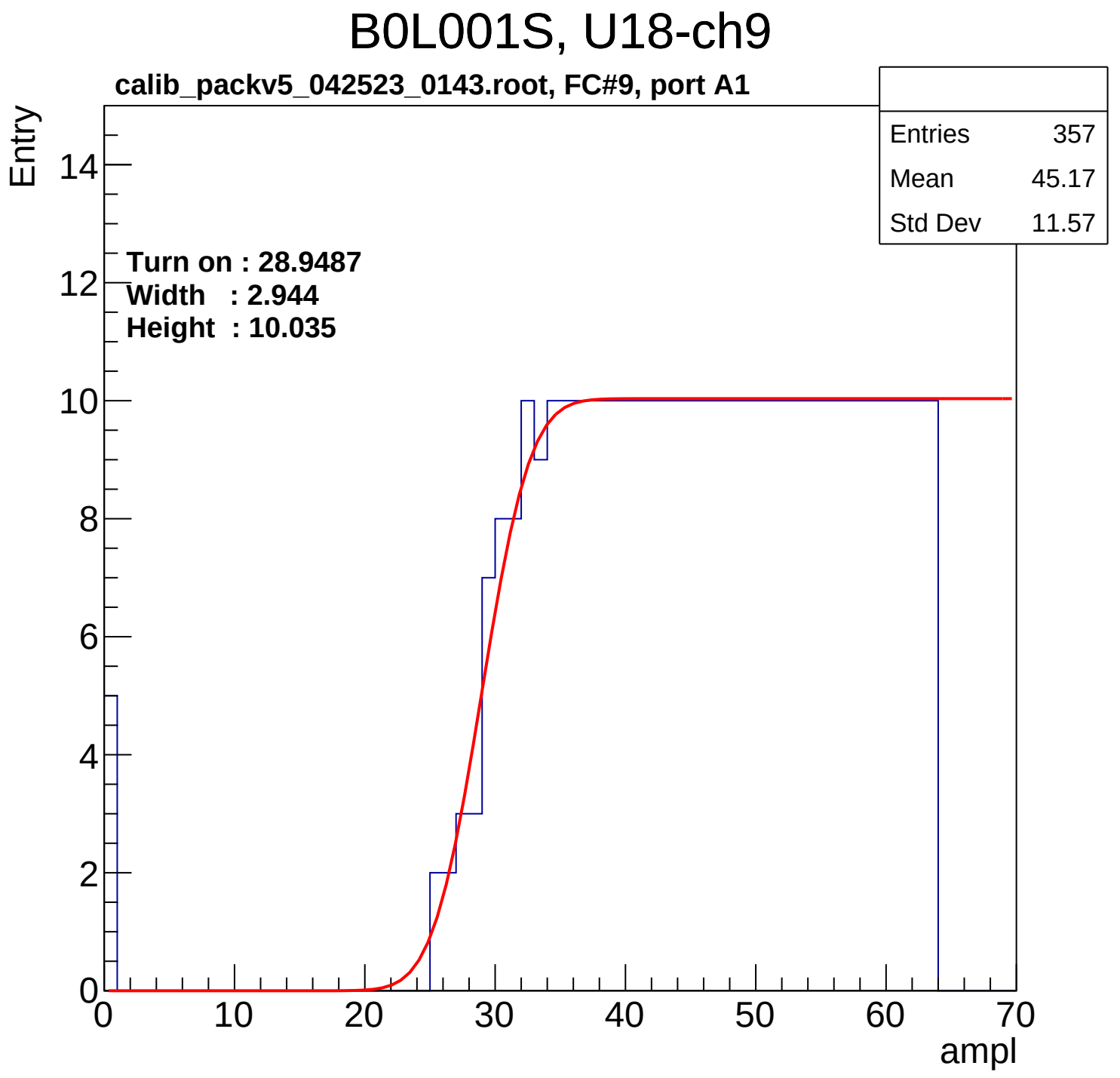

B0L001S, U18-ch4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.64
Std Dev 11.64
Turn on : 27.8644
Width : 3.325
Height : 10.064
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

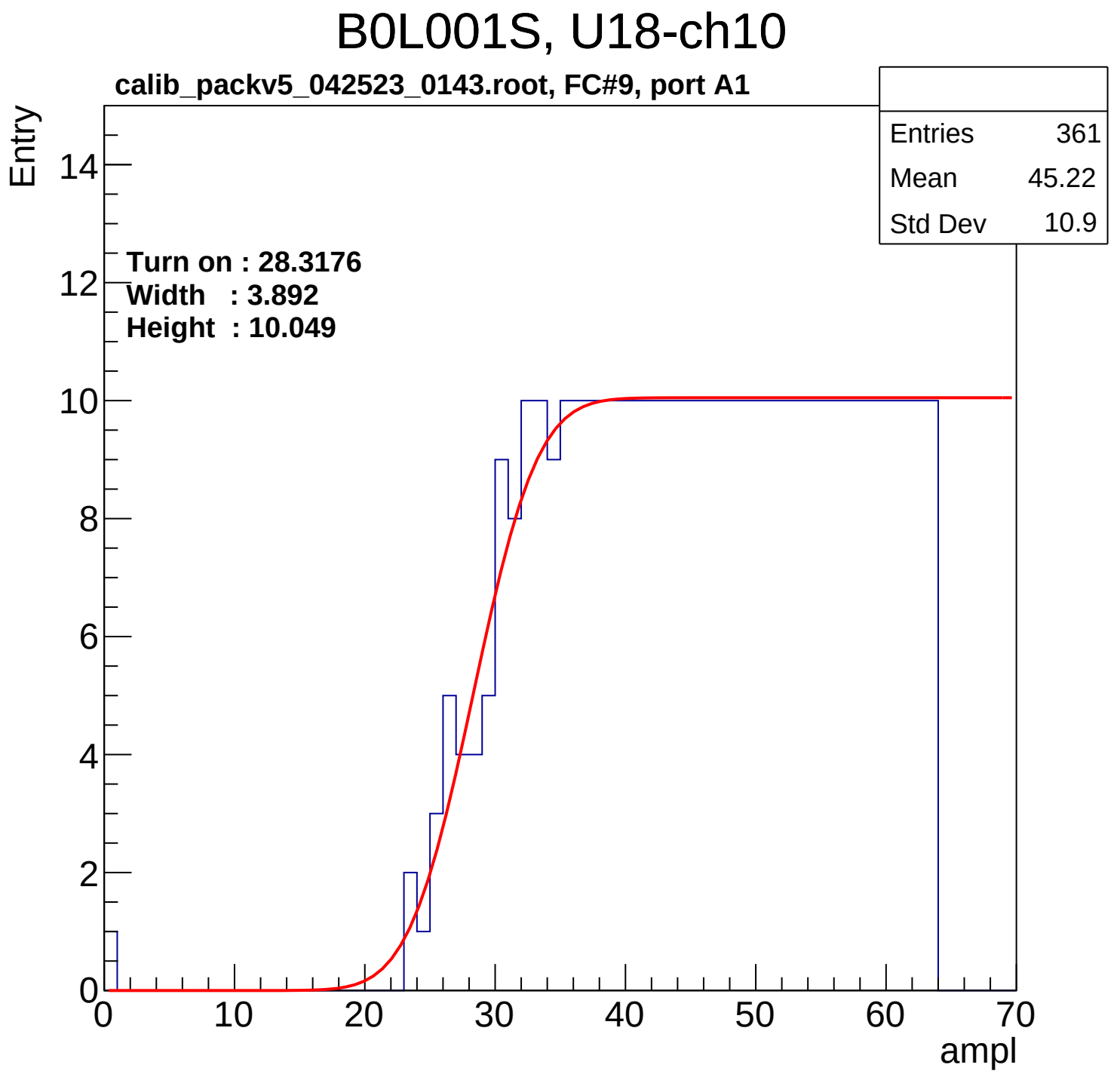

B0L001S, U18-ch5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.58
Std Dev 11.32
Turn on : 27.2006
Width : 1.900
Height : 9.998
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

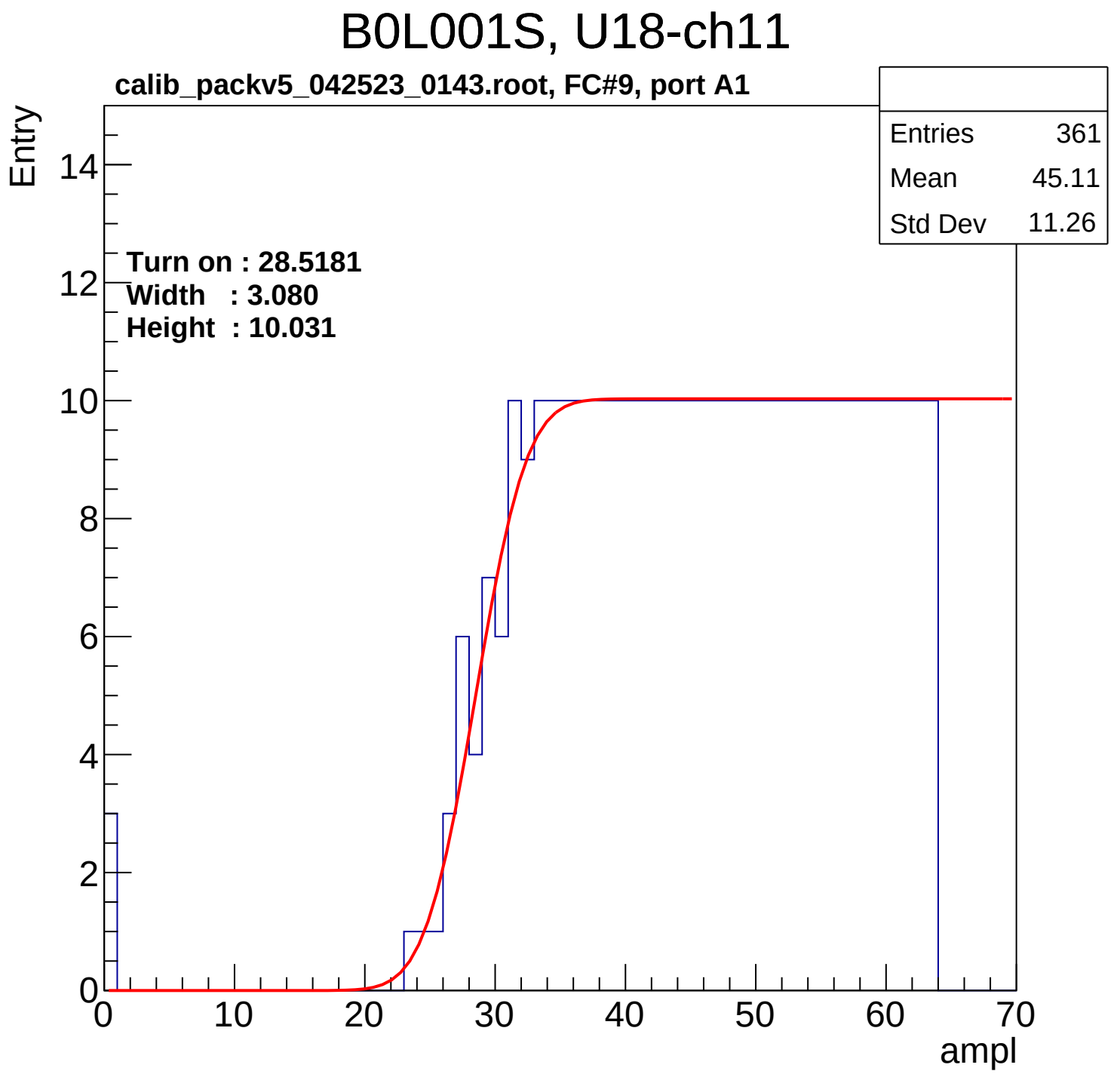

B0L001S, U18-ch6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.18
Std Dev 10.86
Turn on : 28.2354
Width : 2.652
Height : 10.048
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

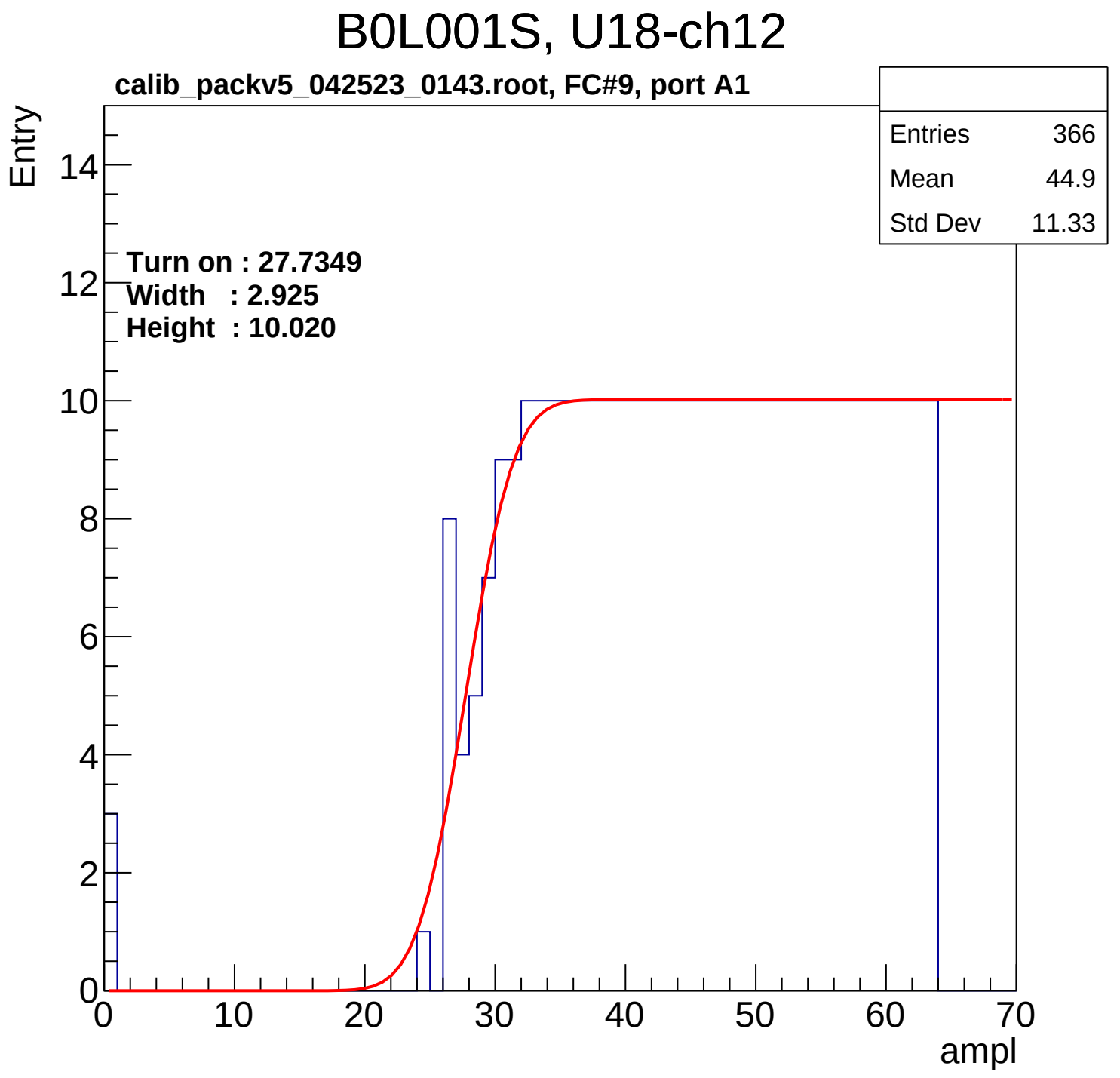

B0L001S, U18-ch7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.94
Std Dev 11.2
Turn on : 27.7696
Width : 3.336
Height : 10.073
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

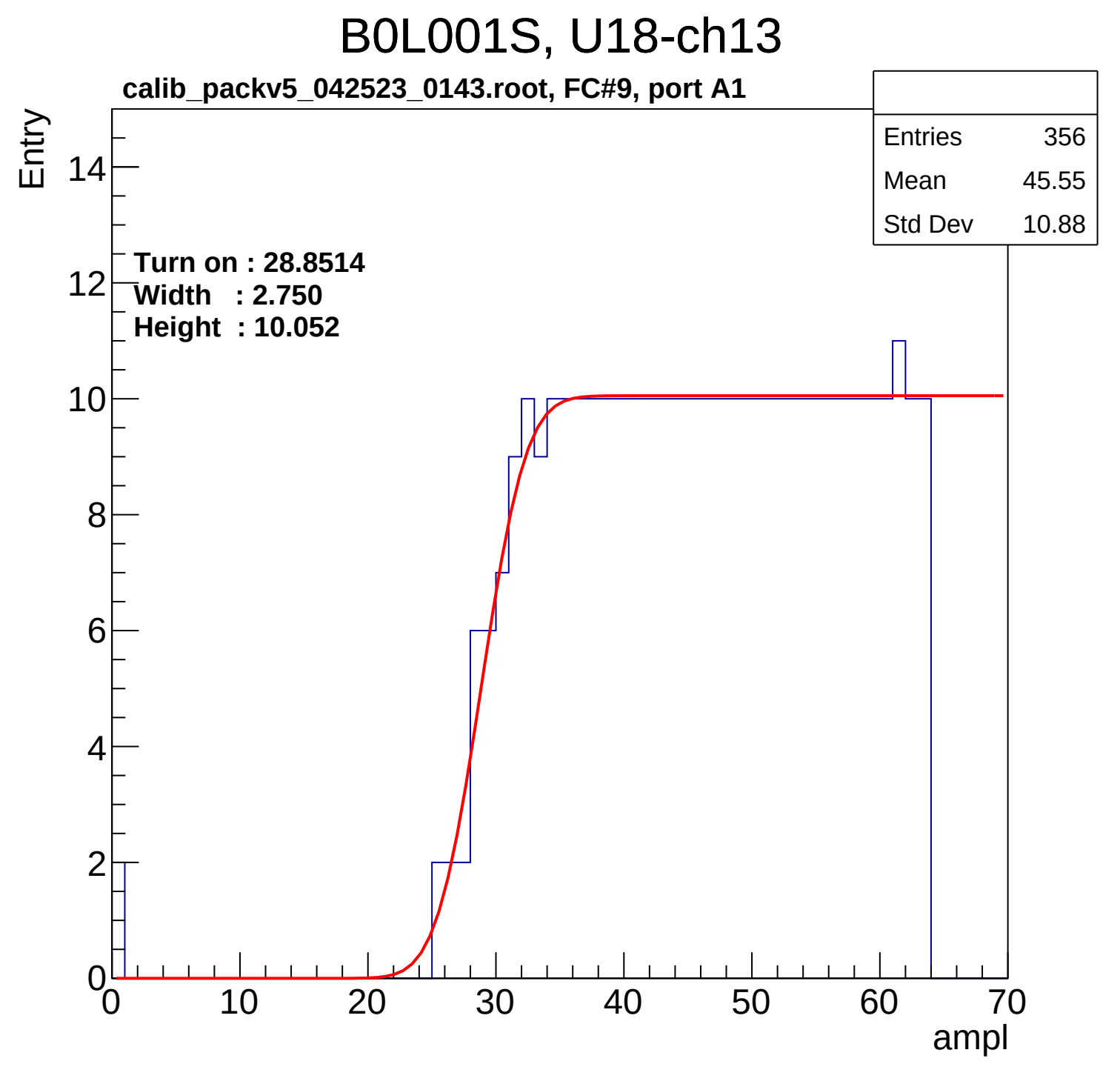

B0L001S, U18-ch8
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.79
Std Dev 11.48
Turn on : 28.1685
Width : 3.593
Height : 10.078
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

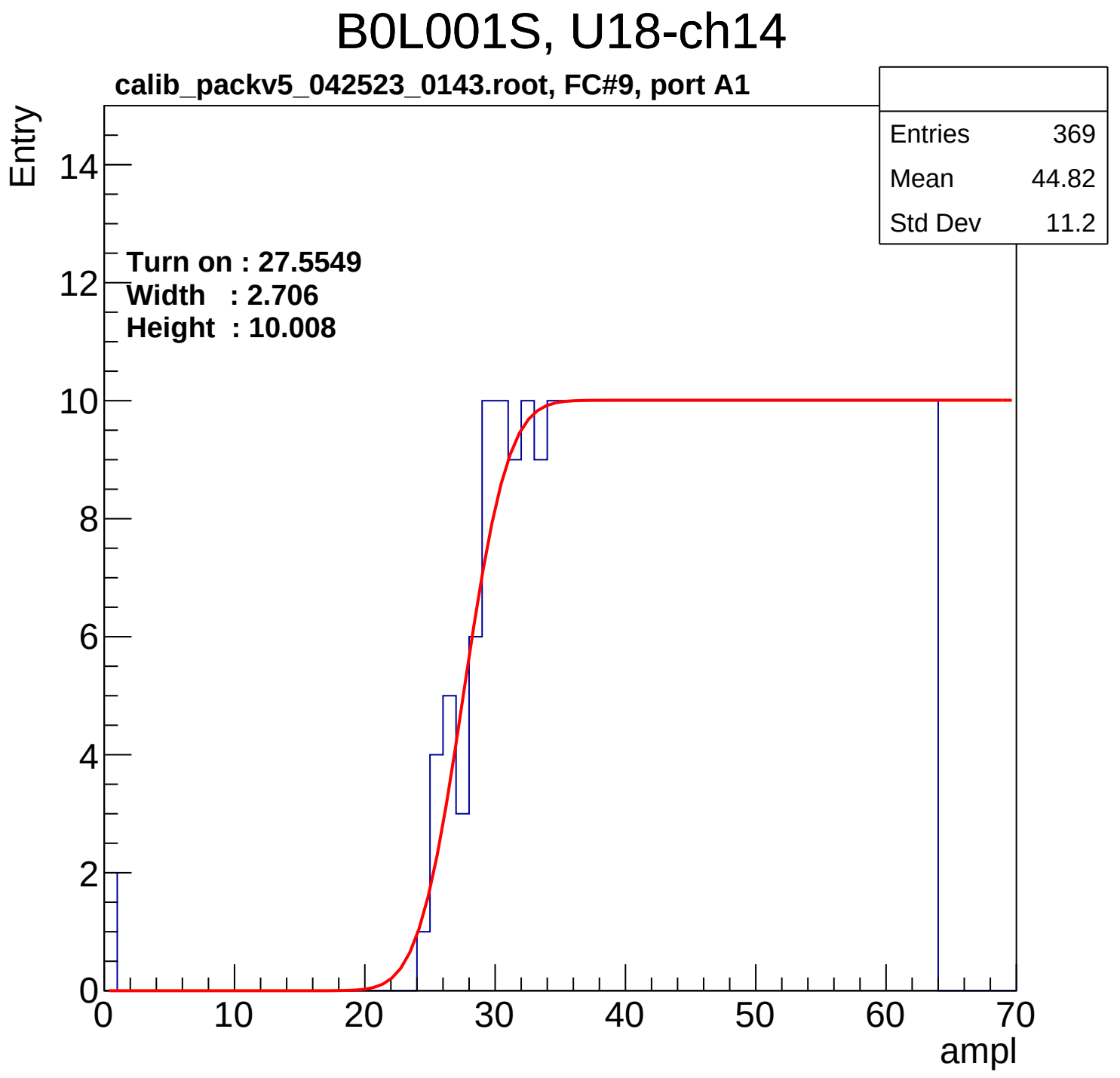

B0L001S, U18-ch9
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.17
Std Dev 11.57
Turn on : 28.9487
Width : 2.944
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

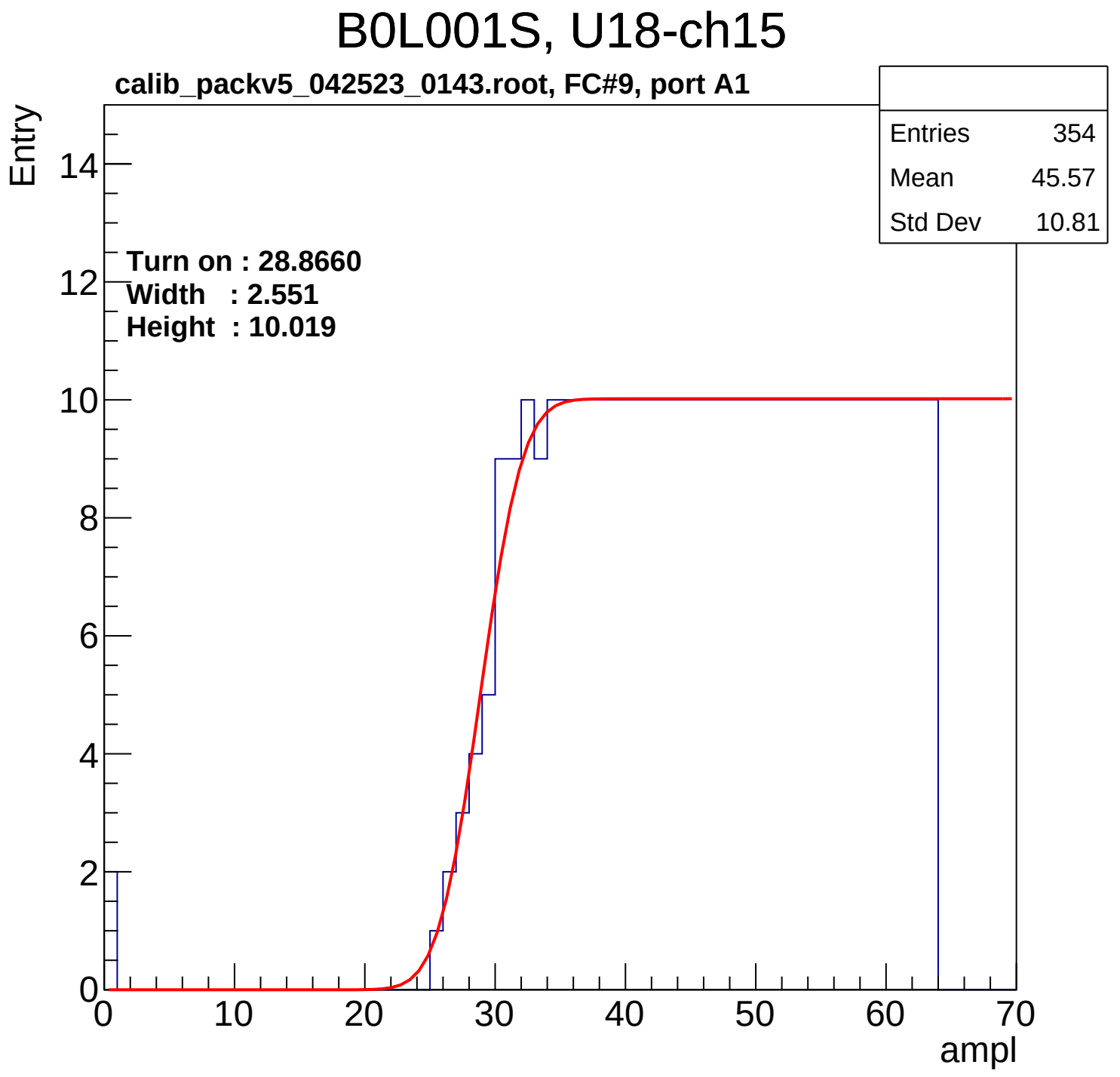

B0L001S, U18-ch10
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.22
Std Dev 10.9
Turn on : 28.3176
Width : 3.892
Height : 10.049
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

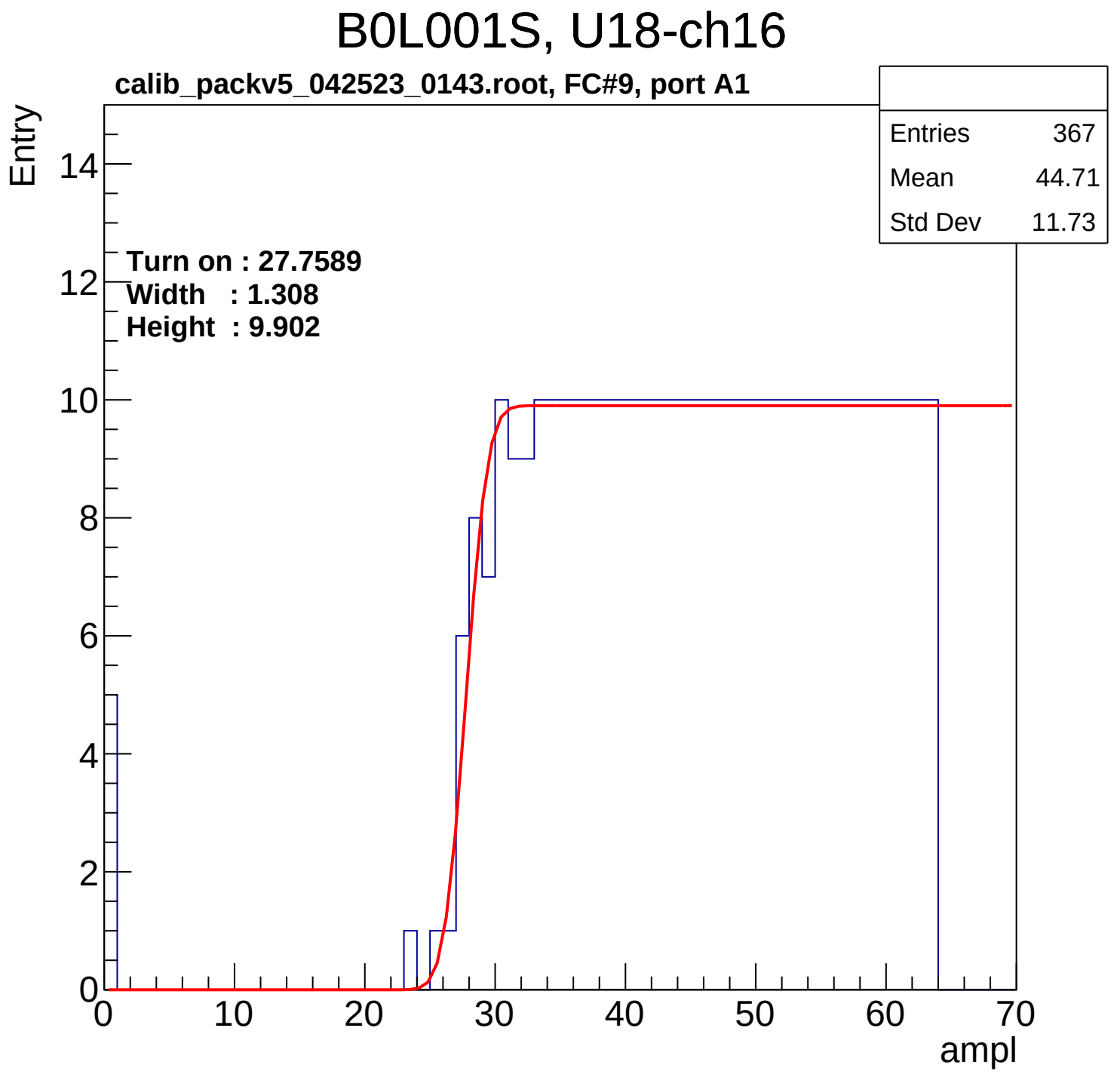

B0L001S, U18-ch11
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.11
Std Dev 11.26
Turn on : 28.5181
Width : 3.080
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

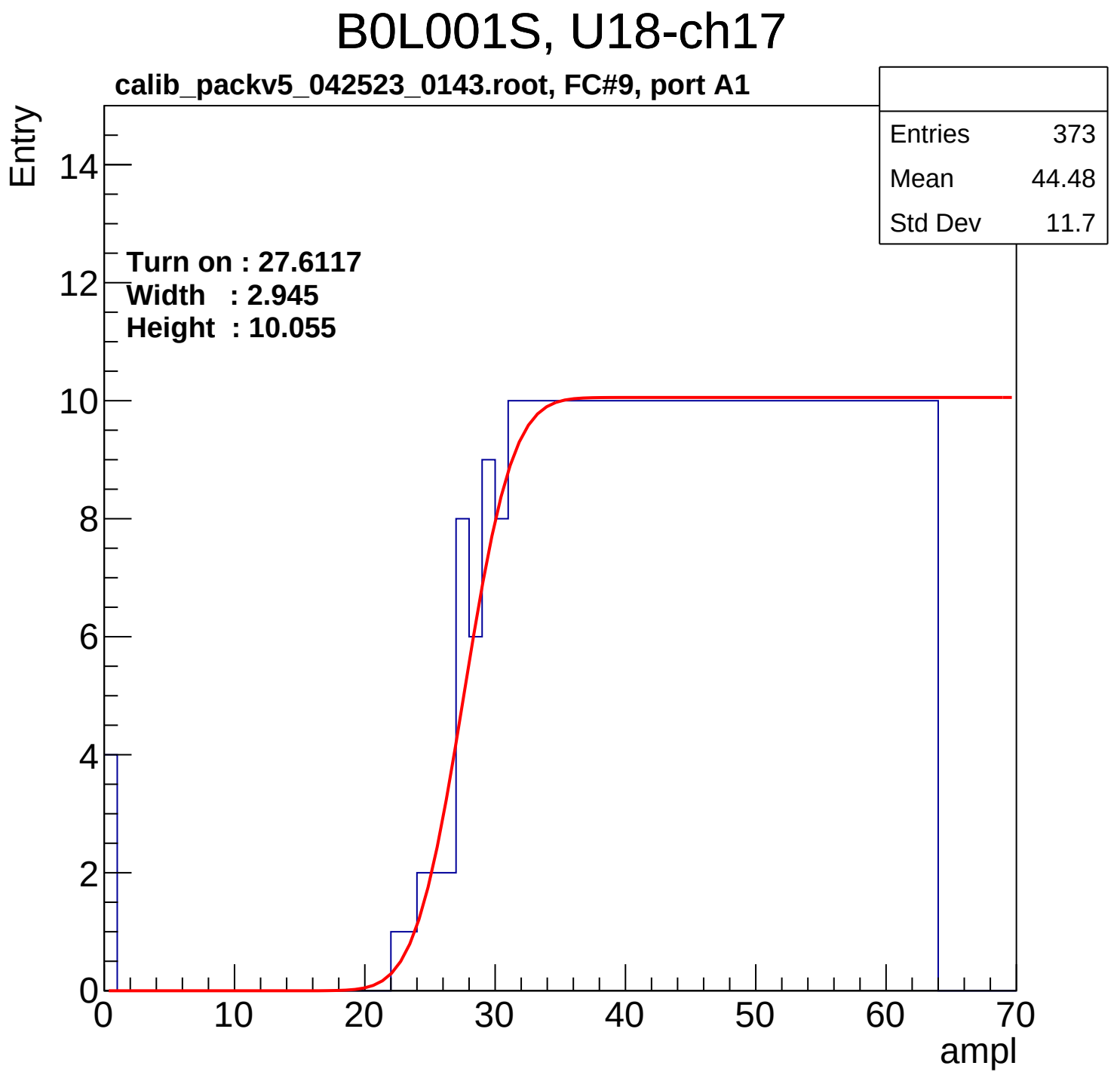

B0L001S, U18-ch12
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.9
Std Dev 11.33
Turn on : 27.7349
Width : 2.925
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

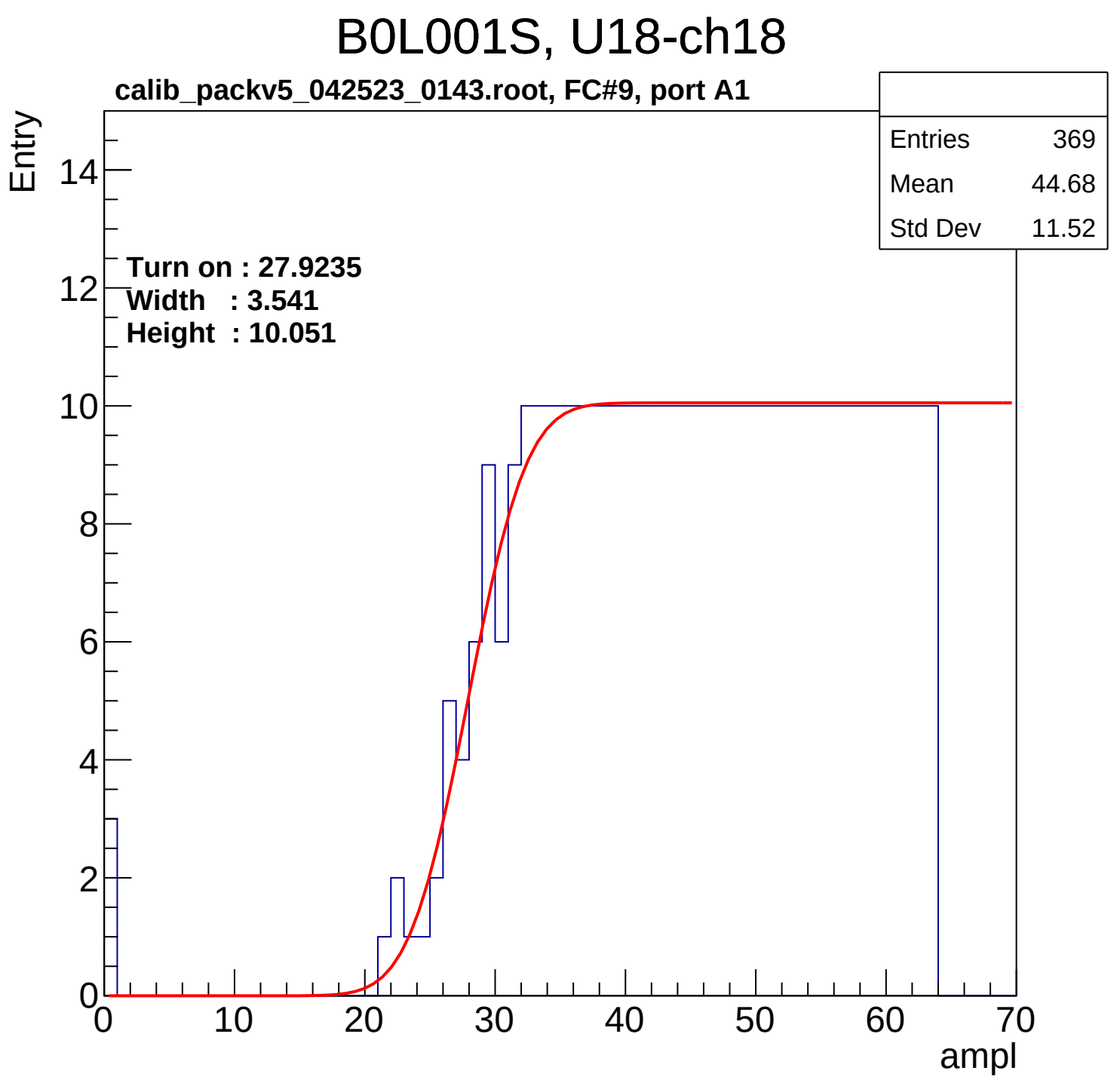

B0L001S, U18-ch13
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.55
Std Dev 10.88
Turn on : 28.8514
Width : 2.750
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

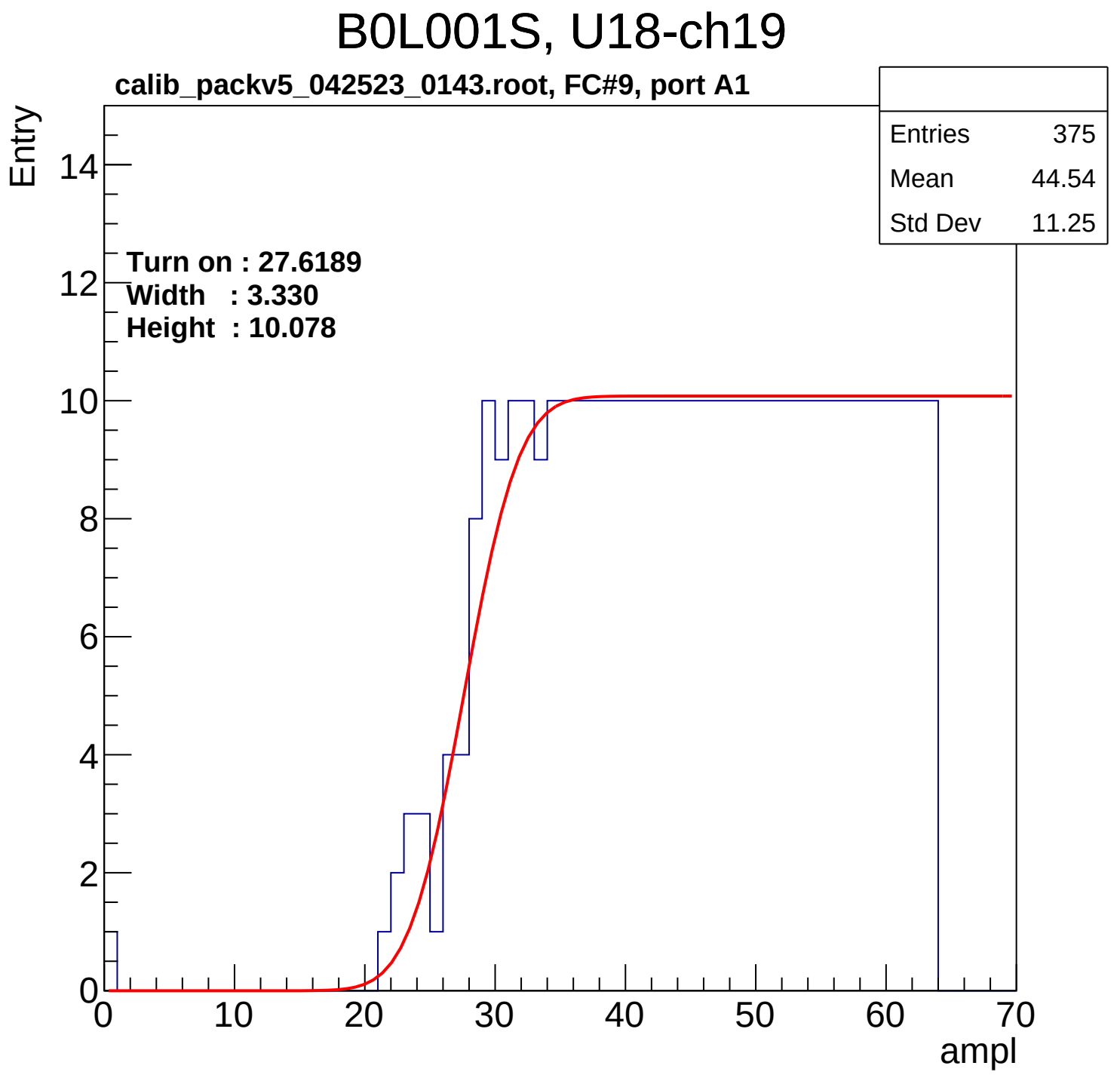

B0L001S, U18-ch14
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.82
Std Dev 11.2
Turn on : 27.5549
Width : 2.706
Height : 10.008
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

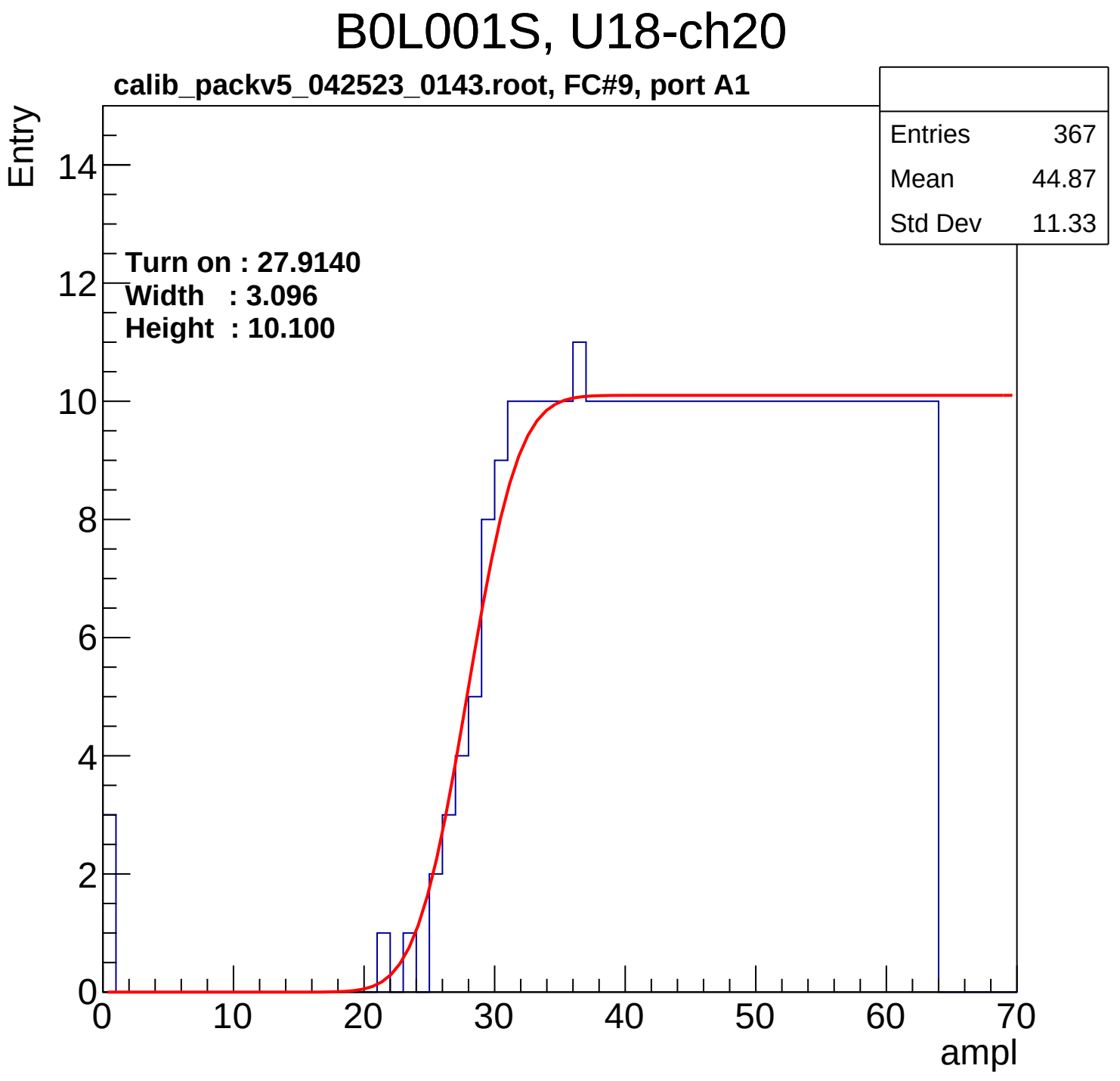

B0L001S, U18-ch15
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.57
Std Dev 10.81
Turn on : 28.8660
Width : 2.551
Height : 10.019
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

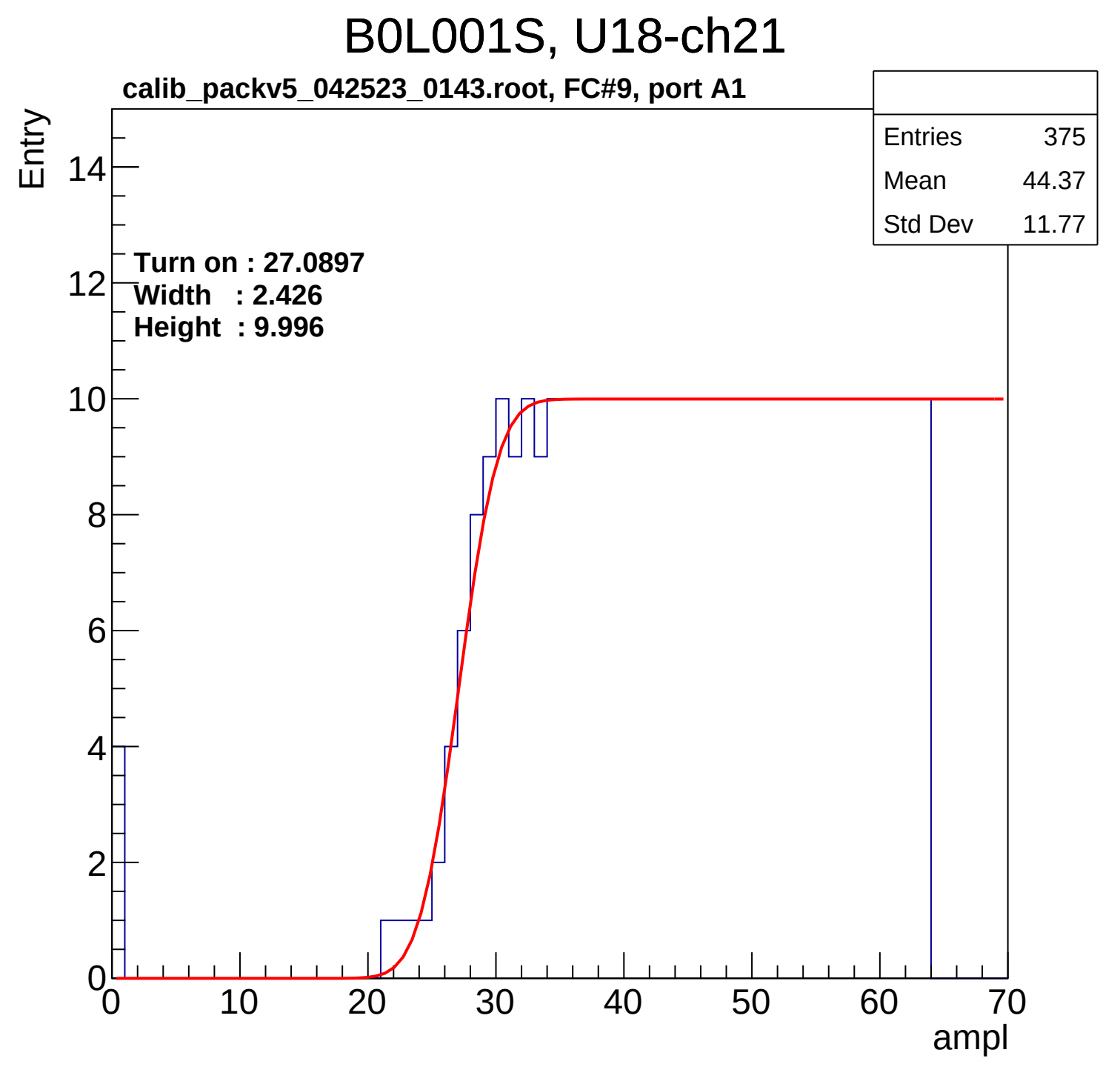

B0L001S, U18-ch16
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.71
Std Dev 11.73
Turn on : 27.7589
Width : 1.308
Height : 9.902
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

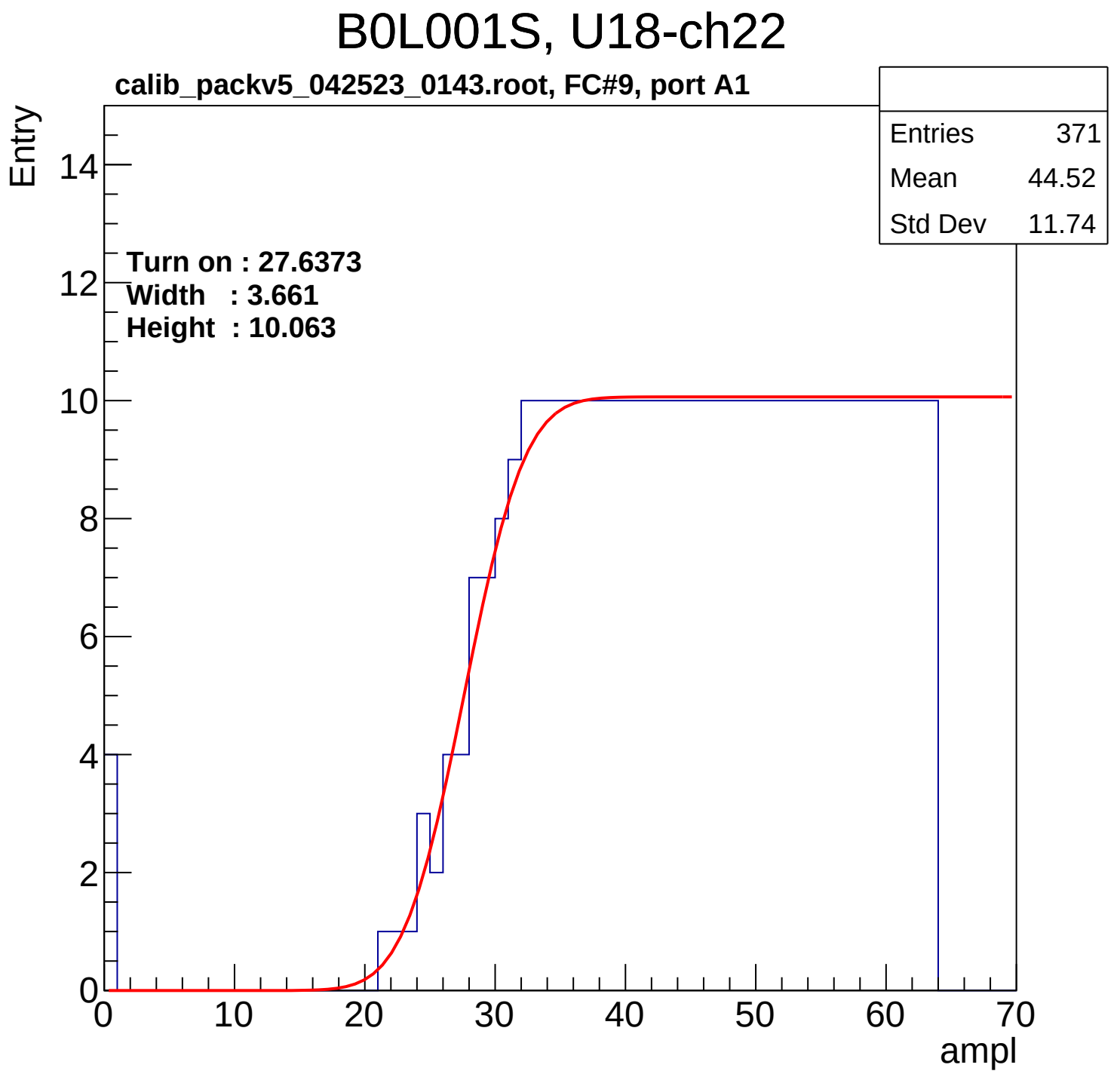

B0L001S, U18-ch17
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.48
Std Dev 11.7
Turn on : 27.6117
Width : 2.945
Height : 10.055
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

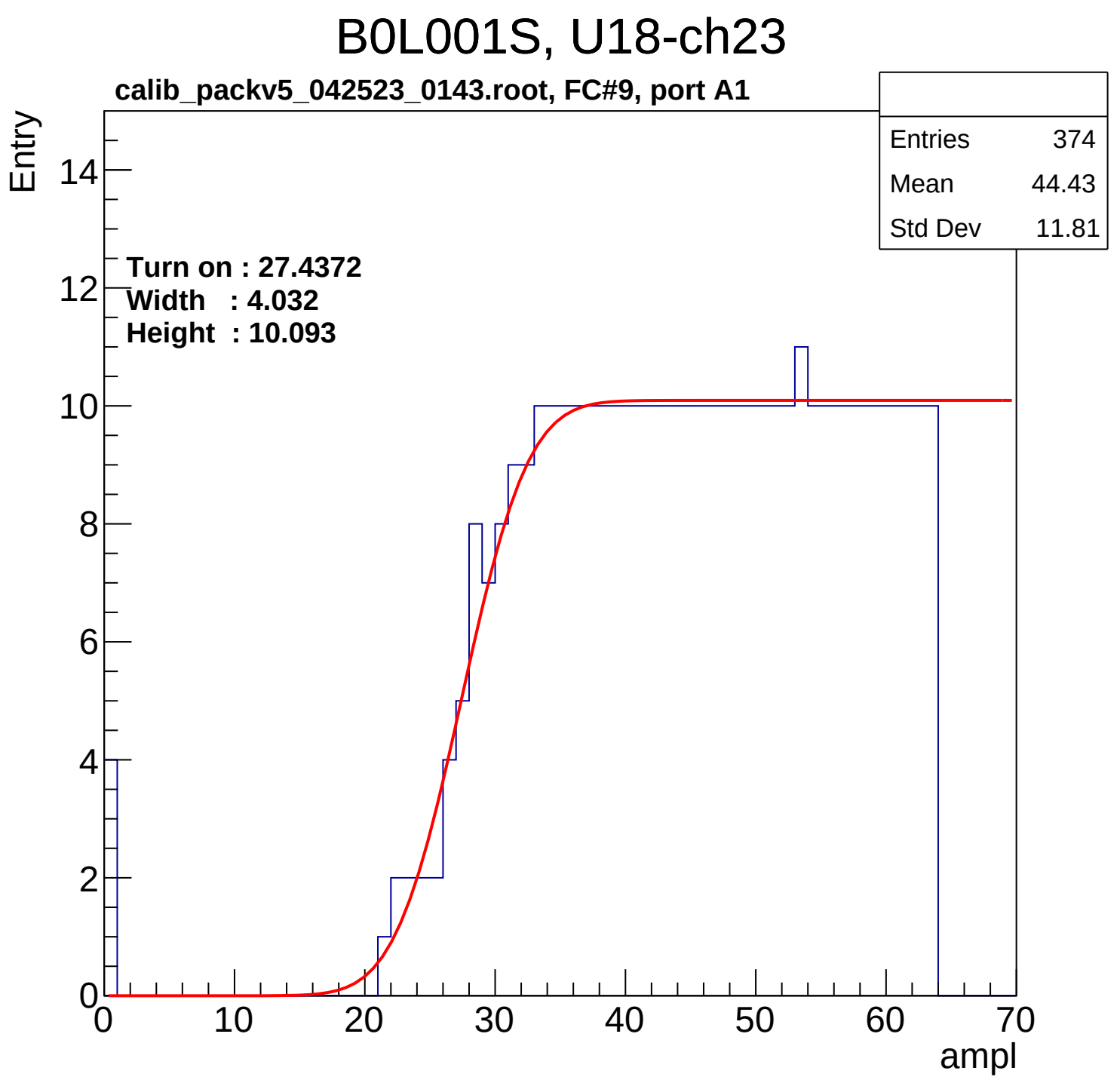

B0L001S, U18-ch18
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.68
Std Dev 11.52
Turn on : 27.9235
Width : 3.541
Height : 10.051
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

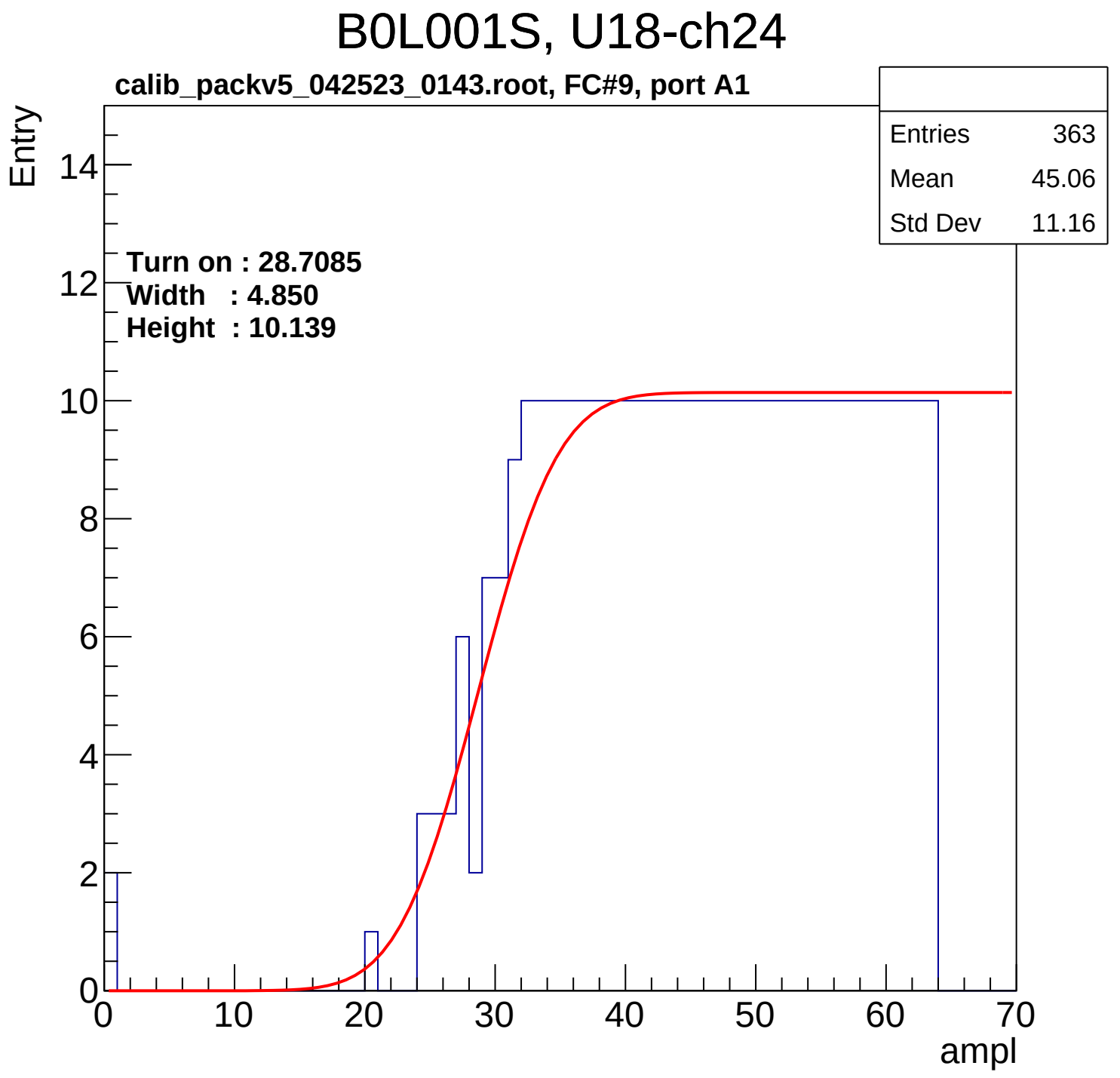

B0L001S, U18-ch19
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.54
Std Dev 11.25
Turn on : 27.6189
Width : 3.330
Height : 10.078
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

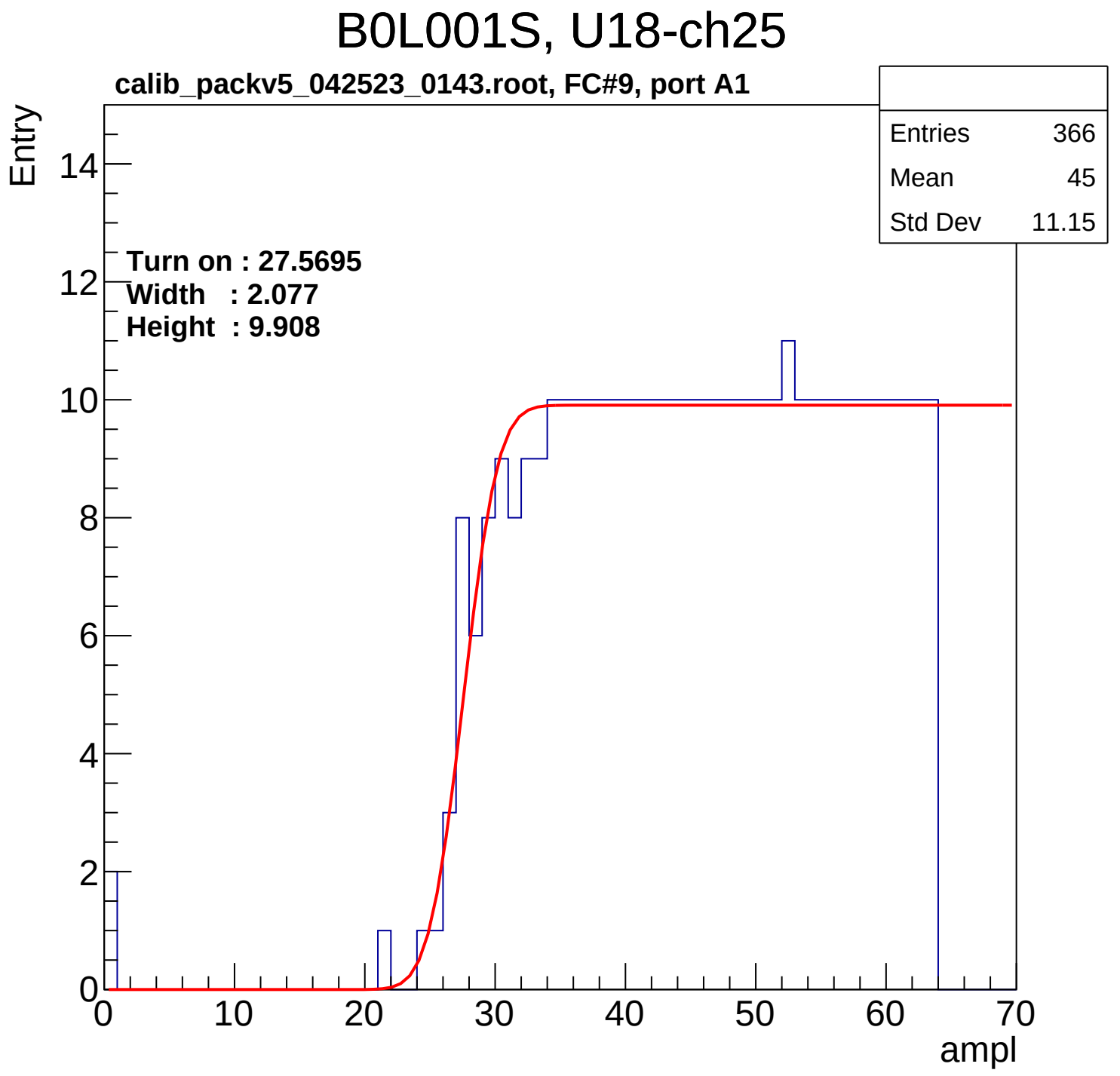

B0L001S, U18-ch20
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.87
Std Dev 11.33
Turn on : 27.9140
Width : 3.096
Height : 10.100
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

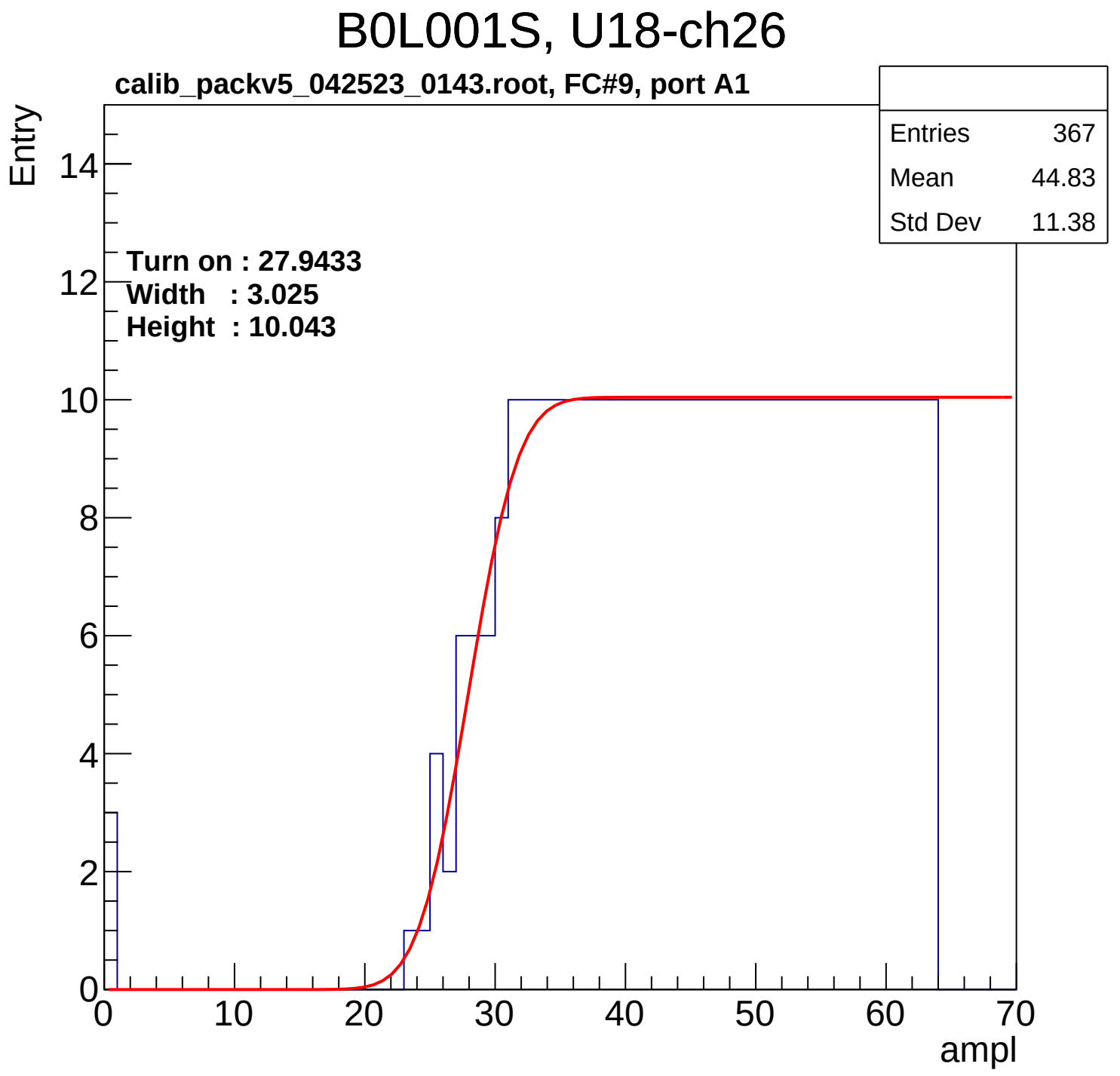

B0L001S, U18-ch21
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.37
Std Dev 11.77
Turn on : 27.0897
Width : 2.426
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

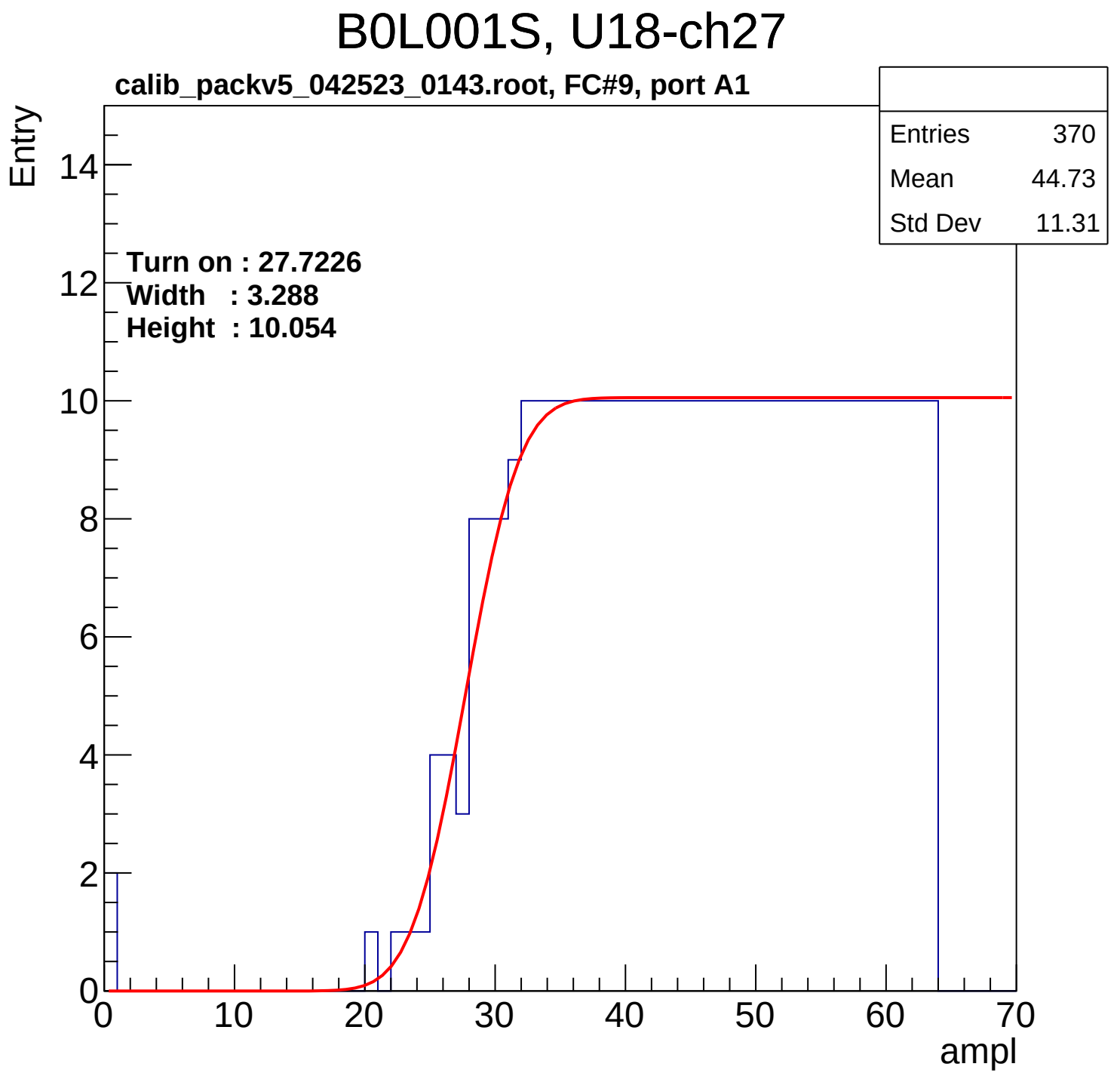

B0L001S, U18-ch22
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.52
Std Dev 11.74
Turn on : 27.6373
Width : 3.661
Height : 10.063
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

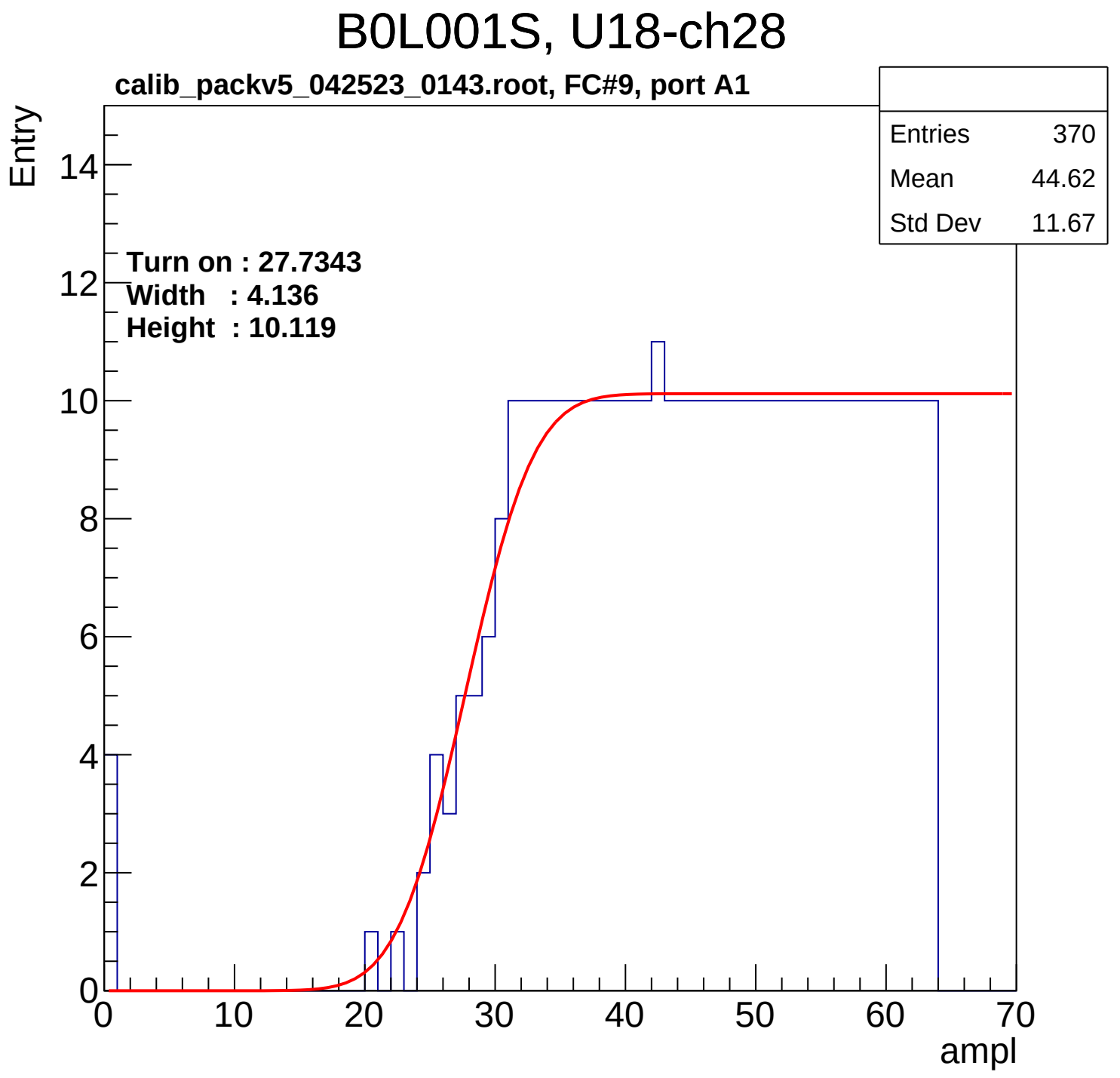

B0L001S, U18-ch23
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.43
Std Dev 11.81
Turn on : 27.4372
Width : 4.032
Height : 10.093
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

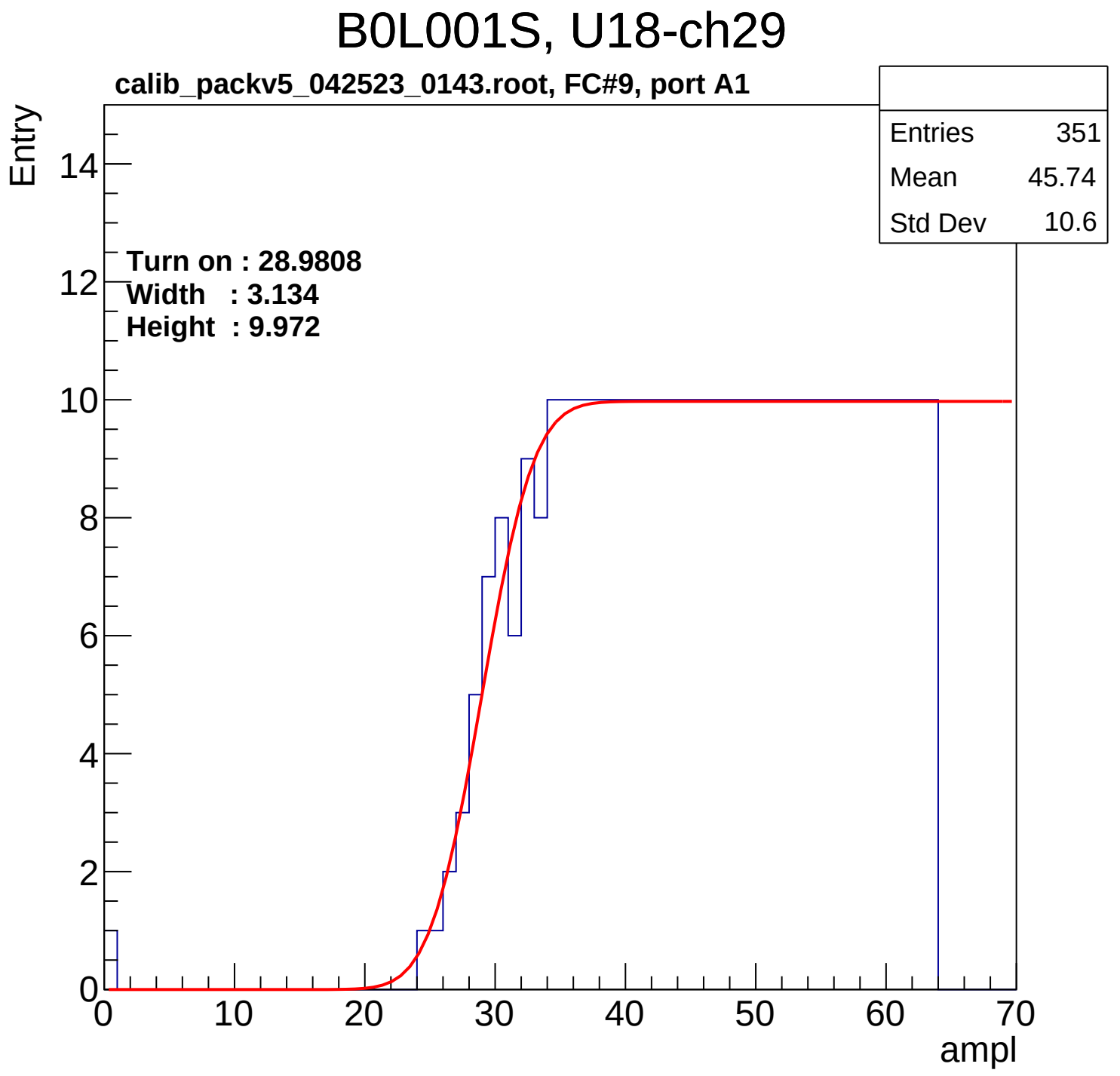

B0L001S, U18-ch24
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.06
Std Dev 11.16
Turn on : 28.7085
Width : 4.850
Height : 10.139
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

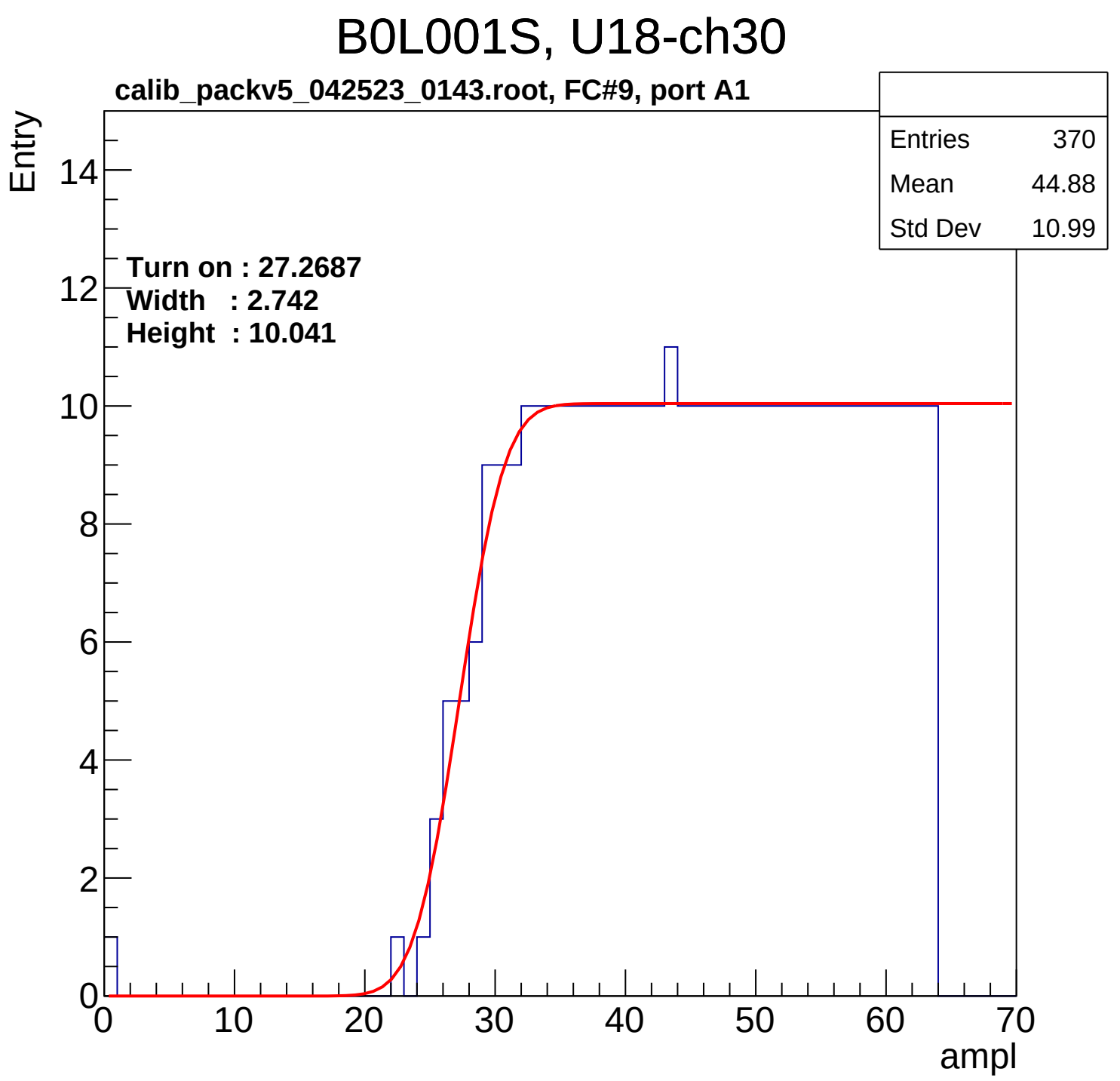

B0L001S, U18-ch25
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 45
Std Dev 11.15
Turn on : 27.5695
Width : 2.077
Height : 9.908
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

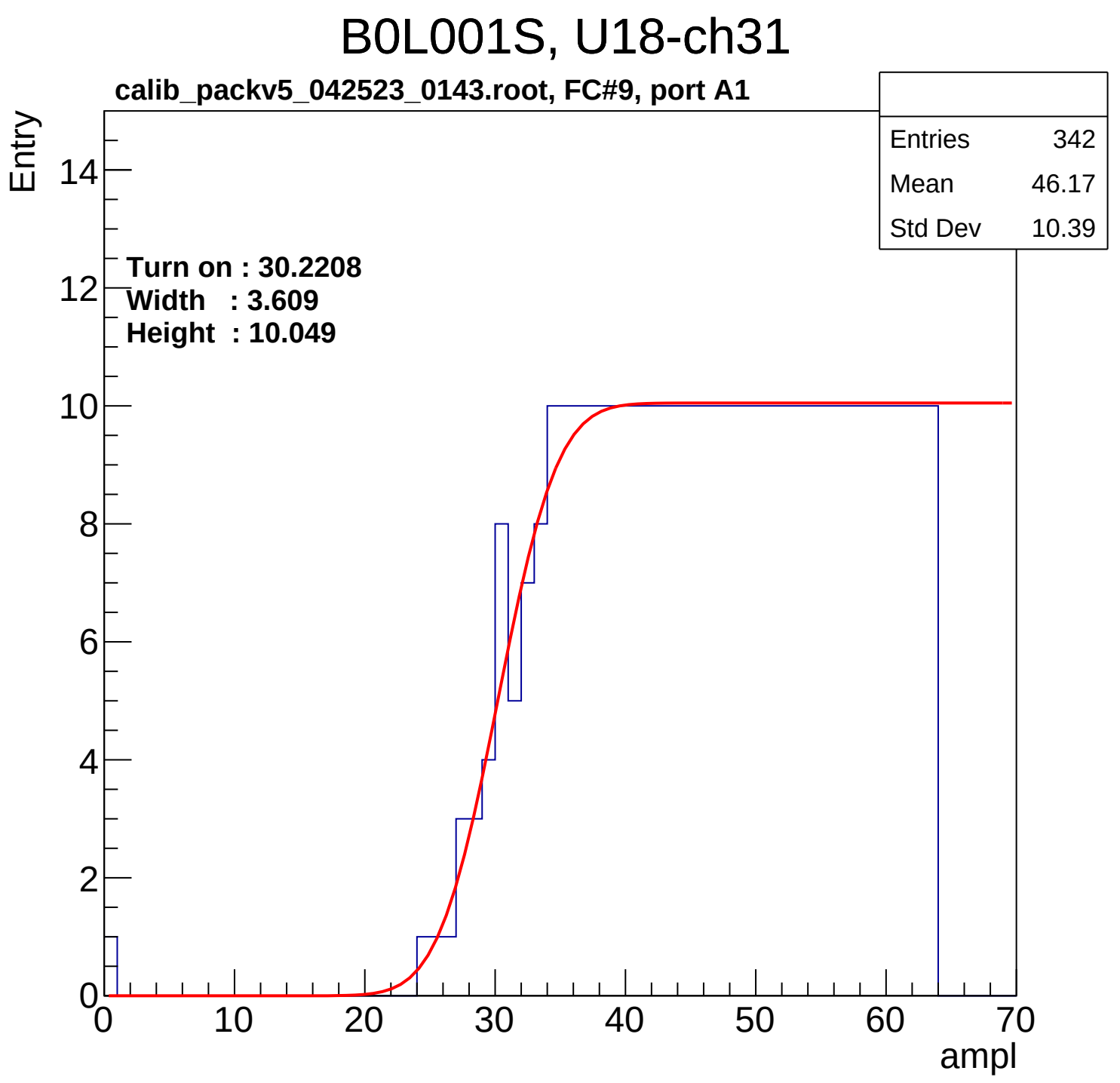

B0L001S, U18-ch26
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.83
Std Dev 11.38
Turn on : 27.9433
Width : 3.025
Height : 10.043
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

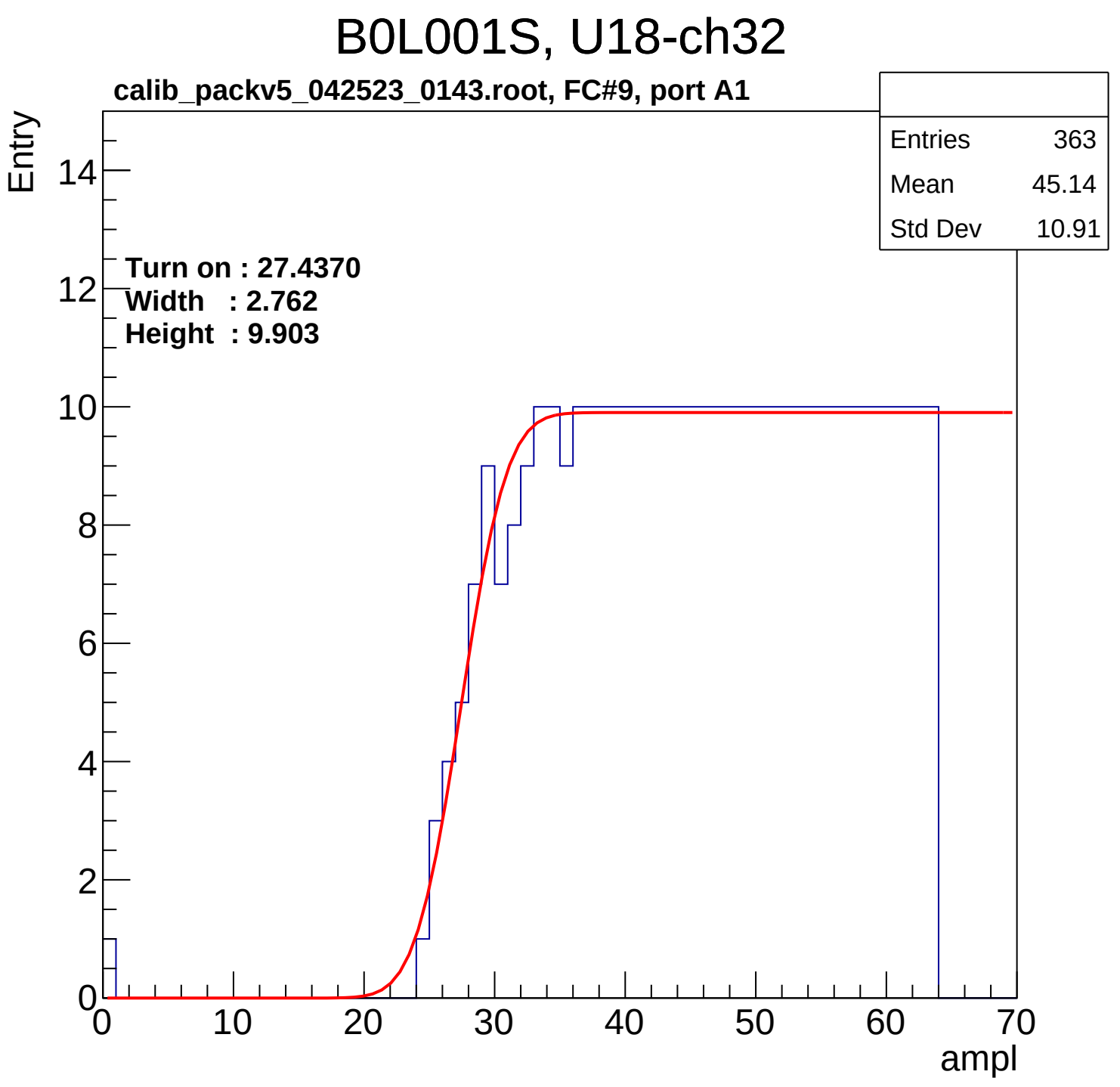

B0L001S, U18-ch27
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.73
Std Dev 11.31
Turn on : 27.7226
Width : 3.288
Height : 10.054
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

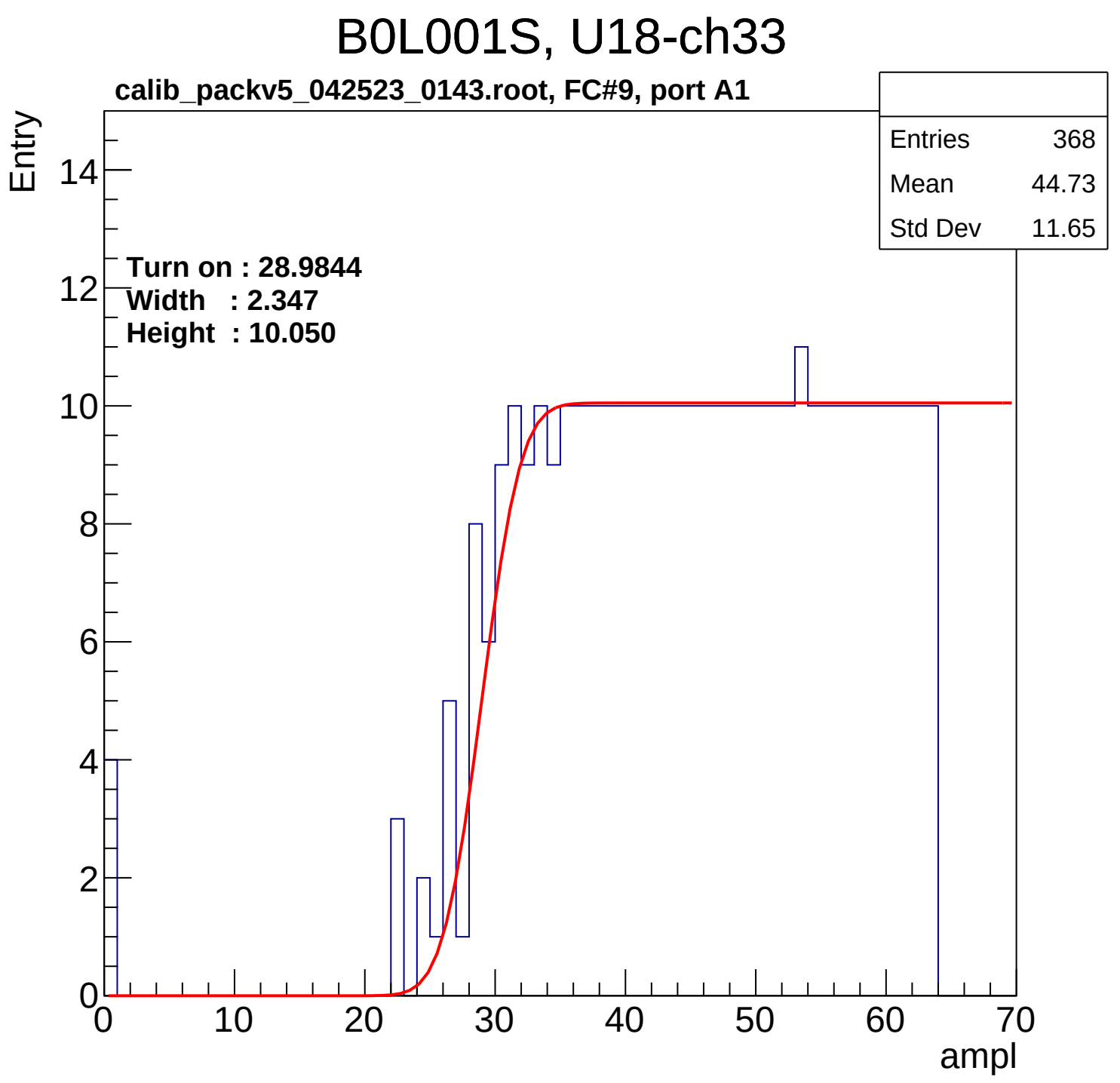

B0L001S, U18-ch28
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.62
Std Dev 11.67
Turn on : 27.7343
Width : 4.136
Height : 10.119
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

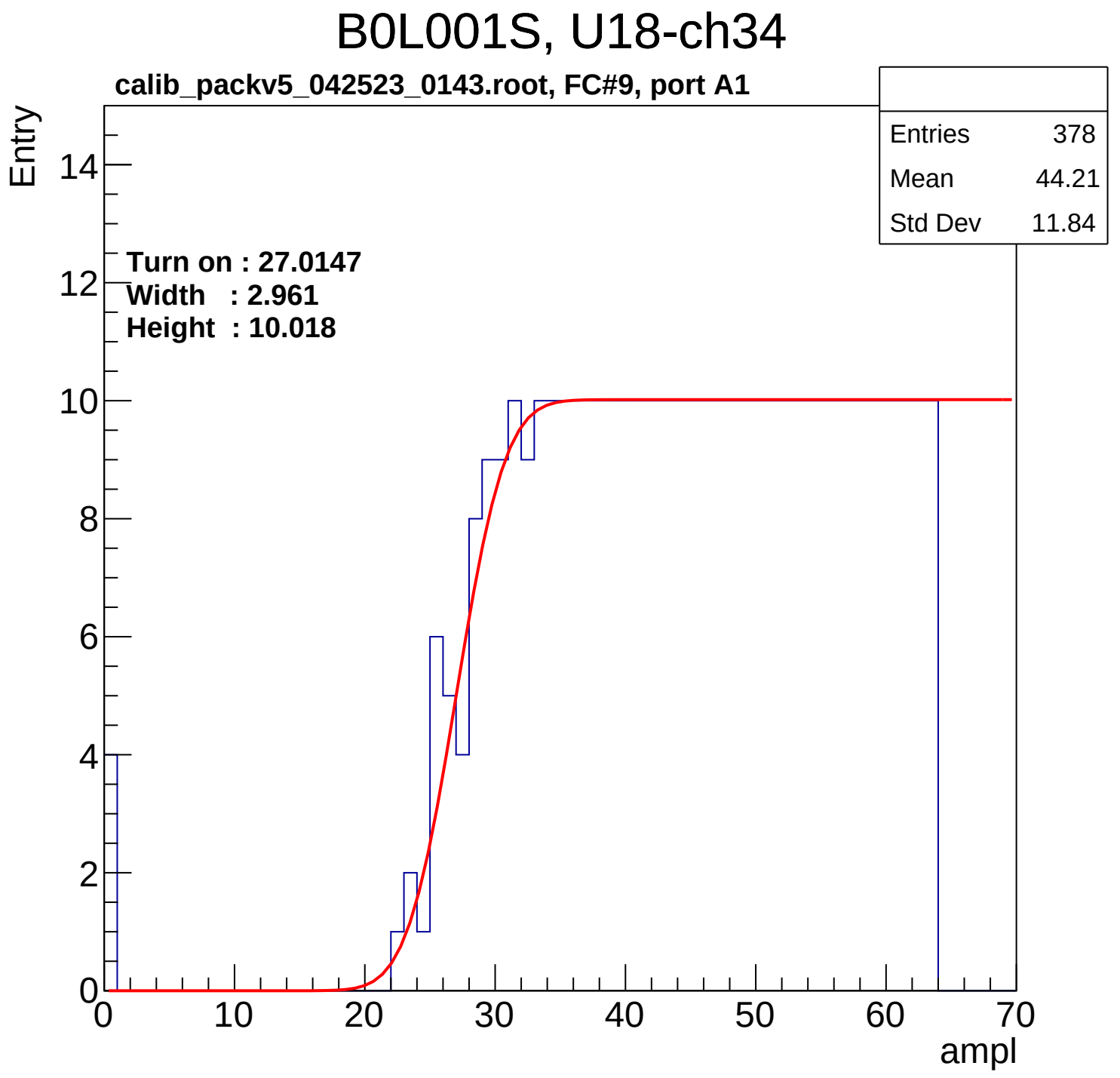

B0L001S, U18-ch29
calib_packv5_042523_0143.root, FC#9, port A1
Entries 351
Mean 45.74
Std Dev 10.6
Turn on : 28.9808
Width : 3.134
Height : 9.972
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

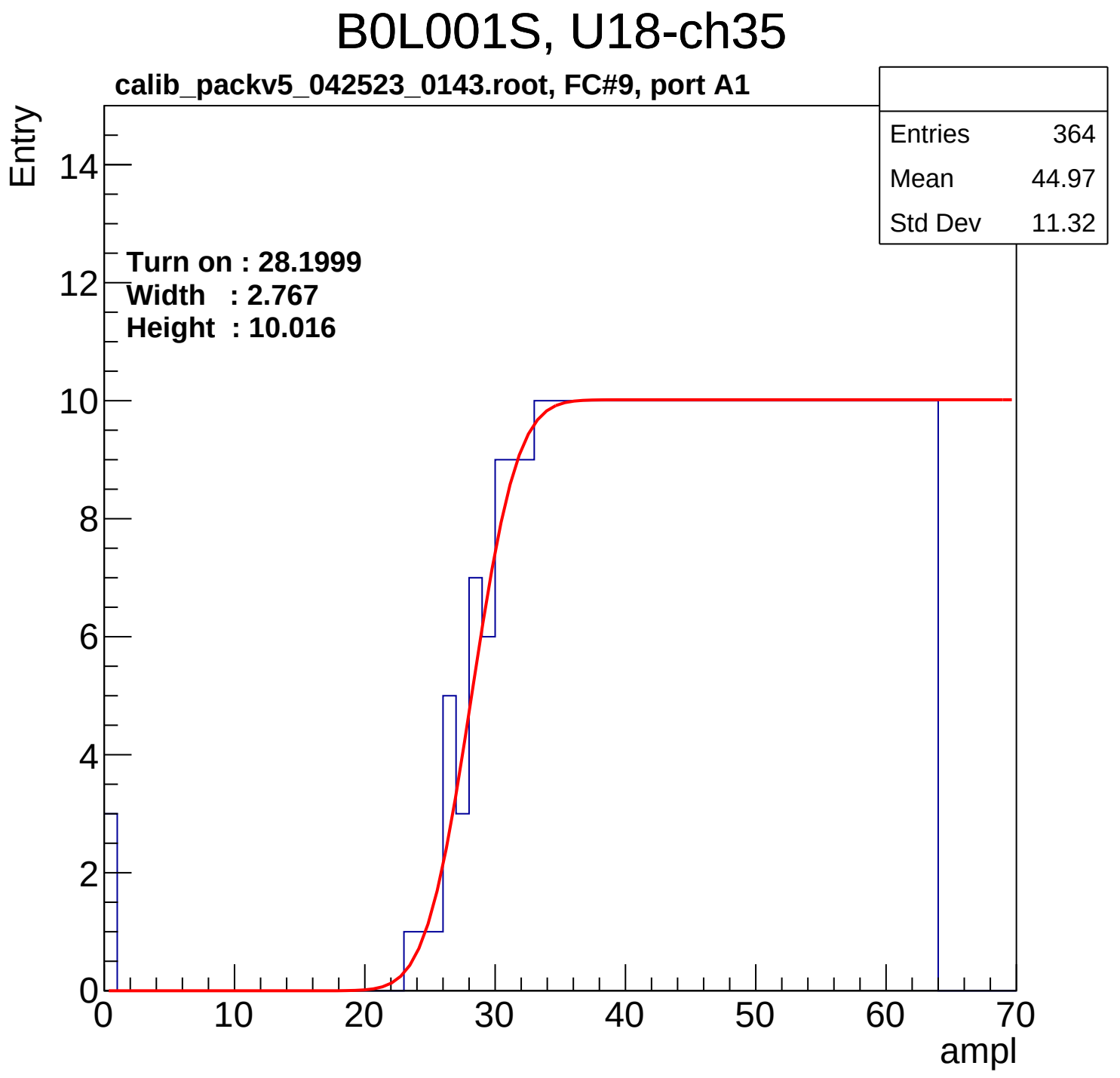

B0L001S, U18-ch30
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.88
Std Dev 10.99
Turn on : 27.2687
Width : 2.742
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

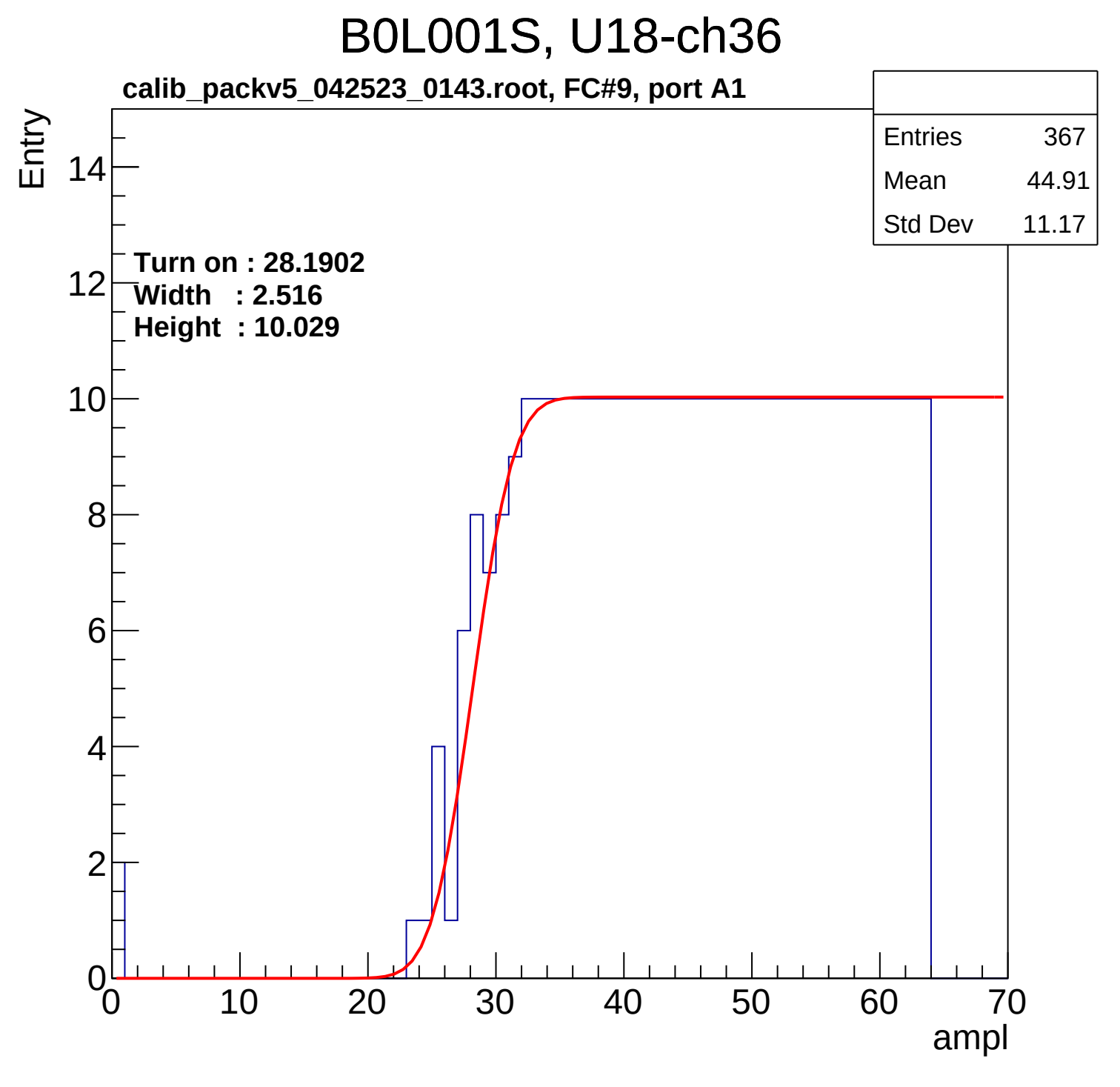

B0L001S, U18-ch31
calib_packv5_042523_0143.root, FC#9, port A1
Entries 342
Mean 46.17
Std Dev 10.39
Turn on : 30.2208
Width : 3.609
Height : 10.049
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

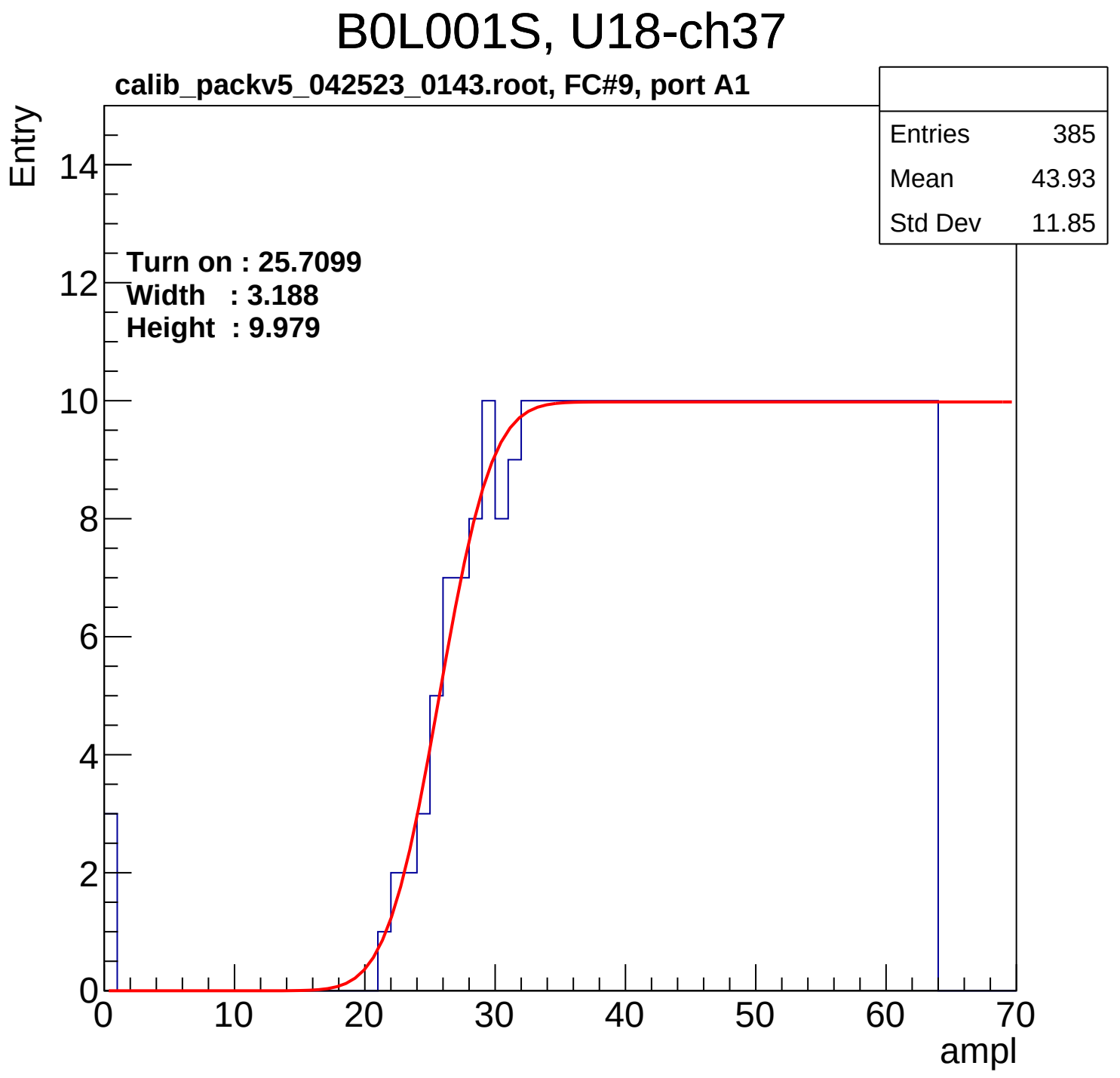

B0L001S, U18-ch32
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.14
Std Dev 10.91
Turn on : 27.4370
Width : 2.762
Height : 9.903
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

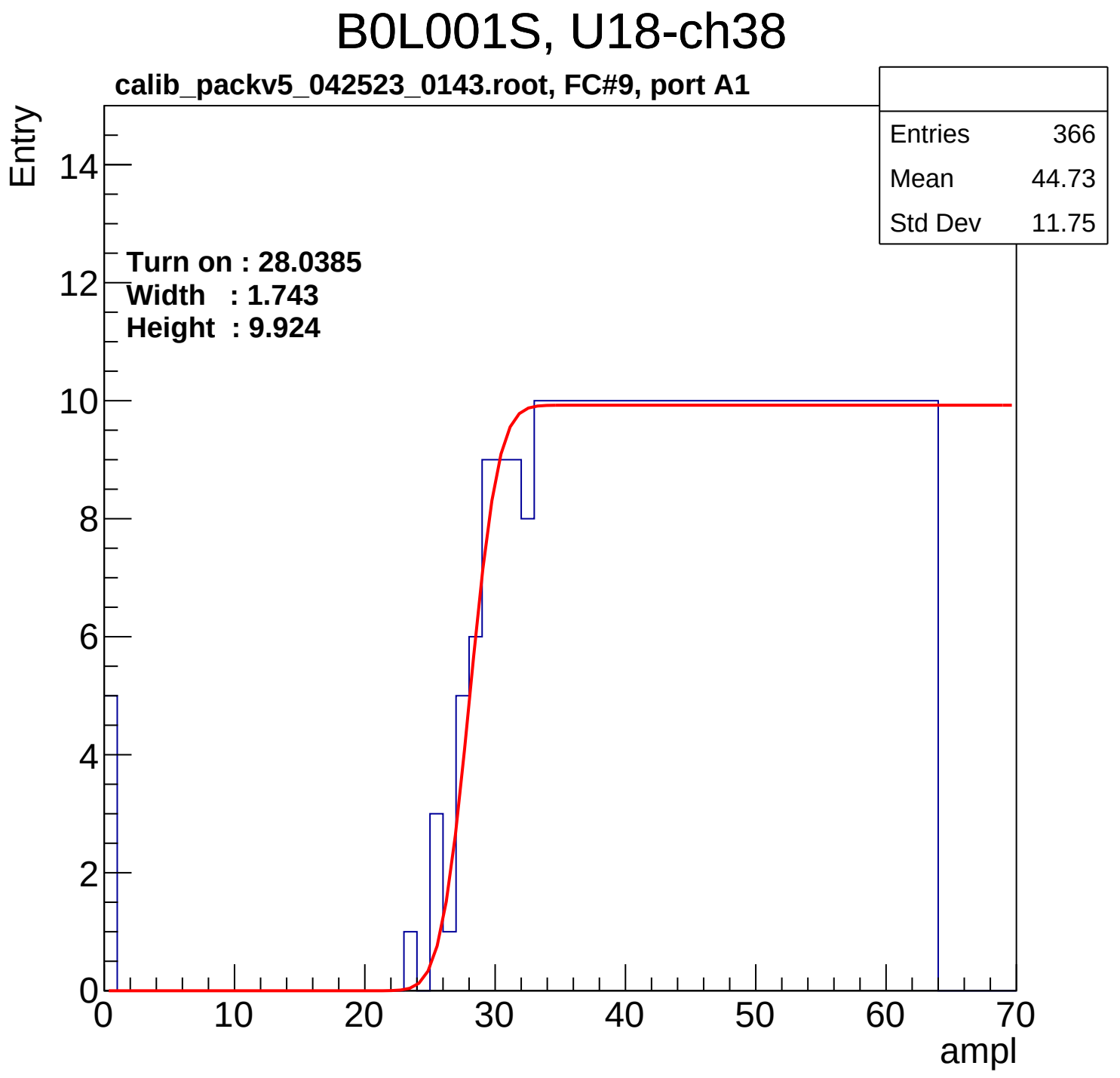

B0L001S, U18-ch33
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.73
Std Dev 11.65
Turn on : 28.9844
Width : 2.347
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

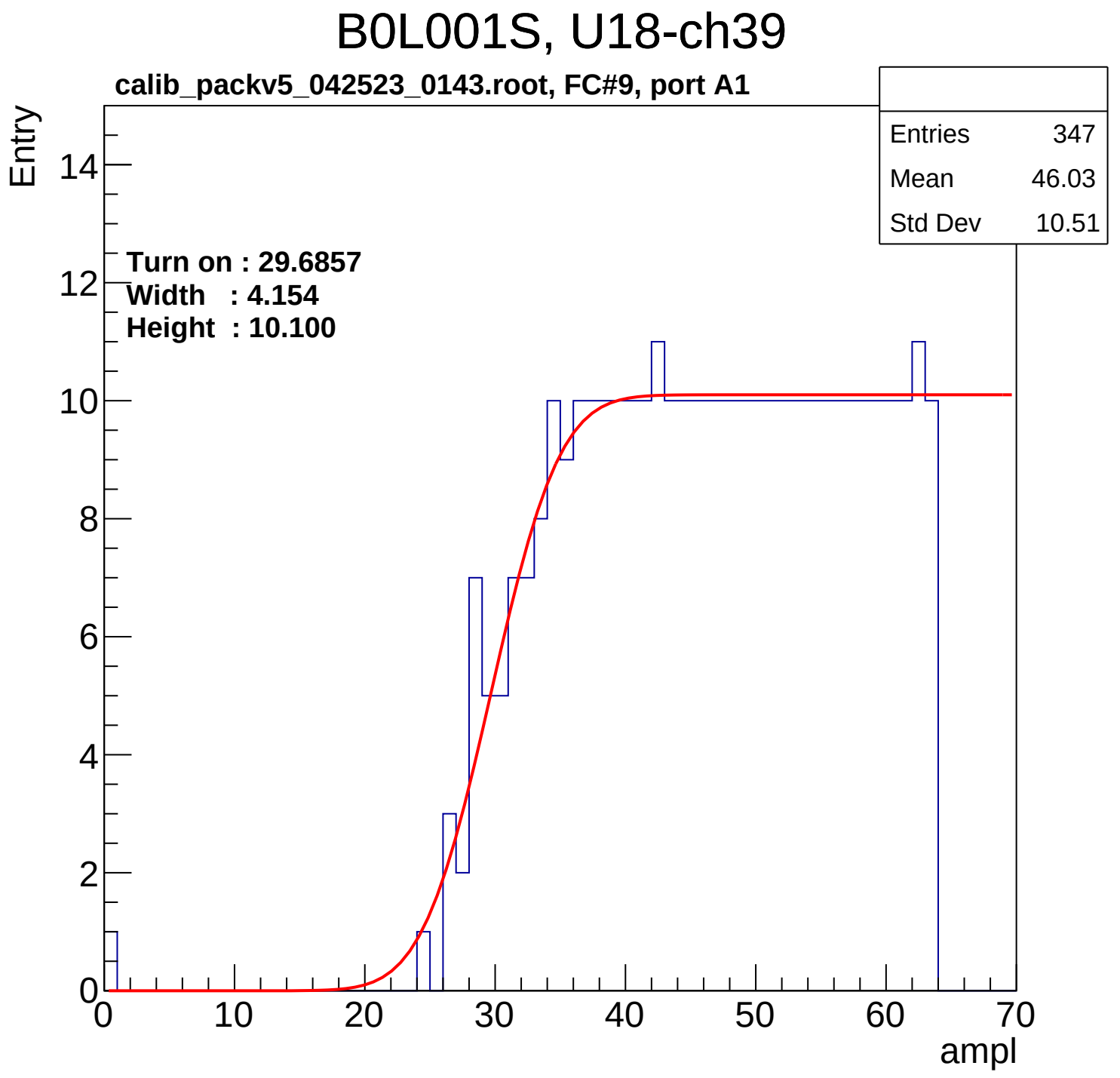

B0L001S, U18-ch34
calib_packv5_042523_0143.root, FC#9, port A1
Entries 378
Mean 44.21
Std Dev 11.84
Turn on : 27.0147
Width : 2.961
Height : 10.018
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

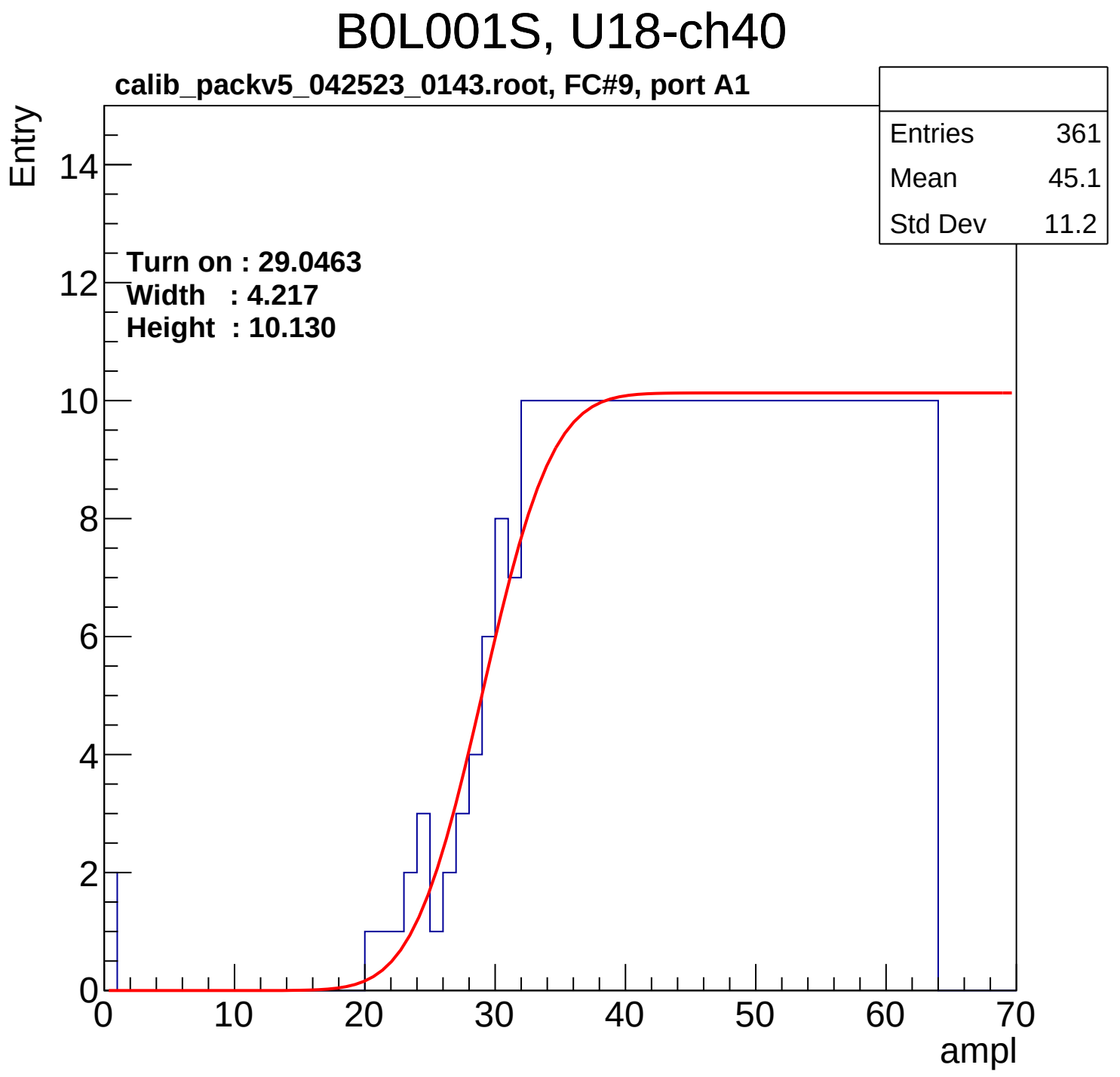

B0L001S, U18-ch35
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.97
Std Dev 11.32
Turn on : 28.1999
Width : 2.767
Height : 10.016
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

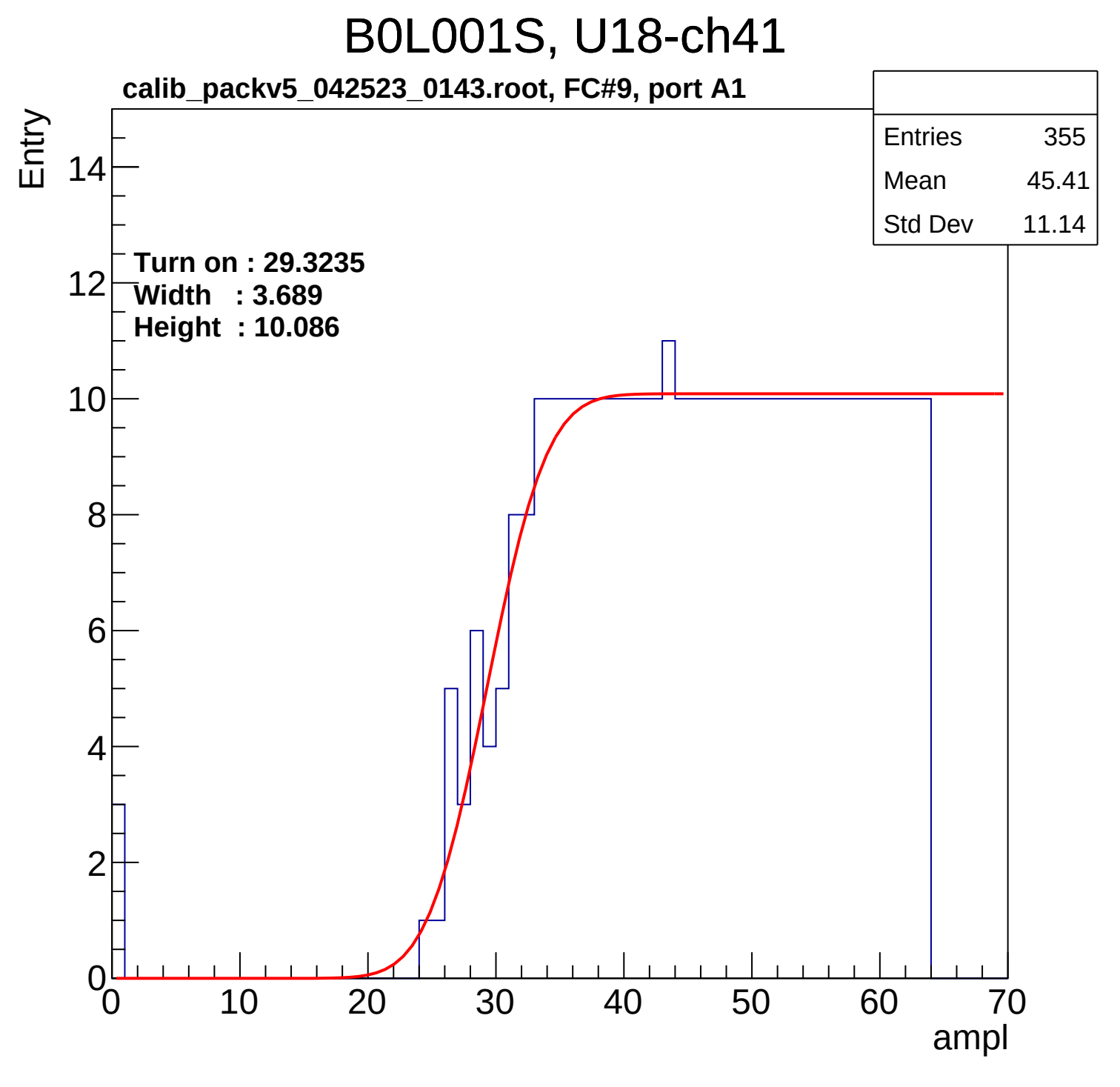

B0L001S, U18-ch36
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.91
Std Dev 11.17
Turn on : 28.1902
Width : 2.516
Height : 10.029
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

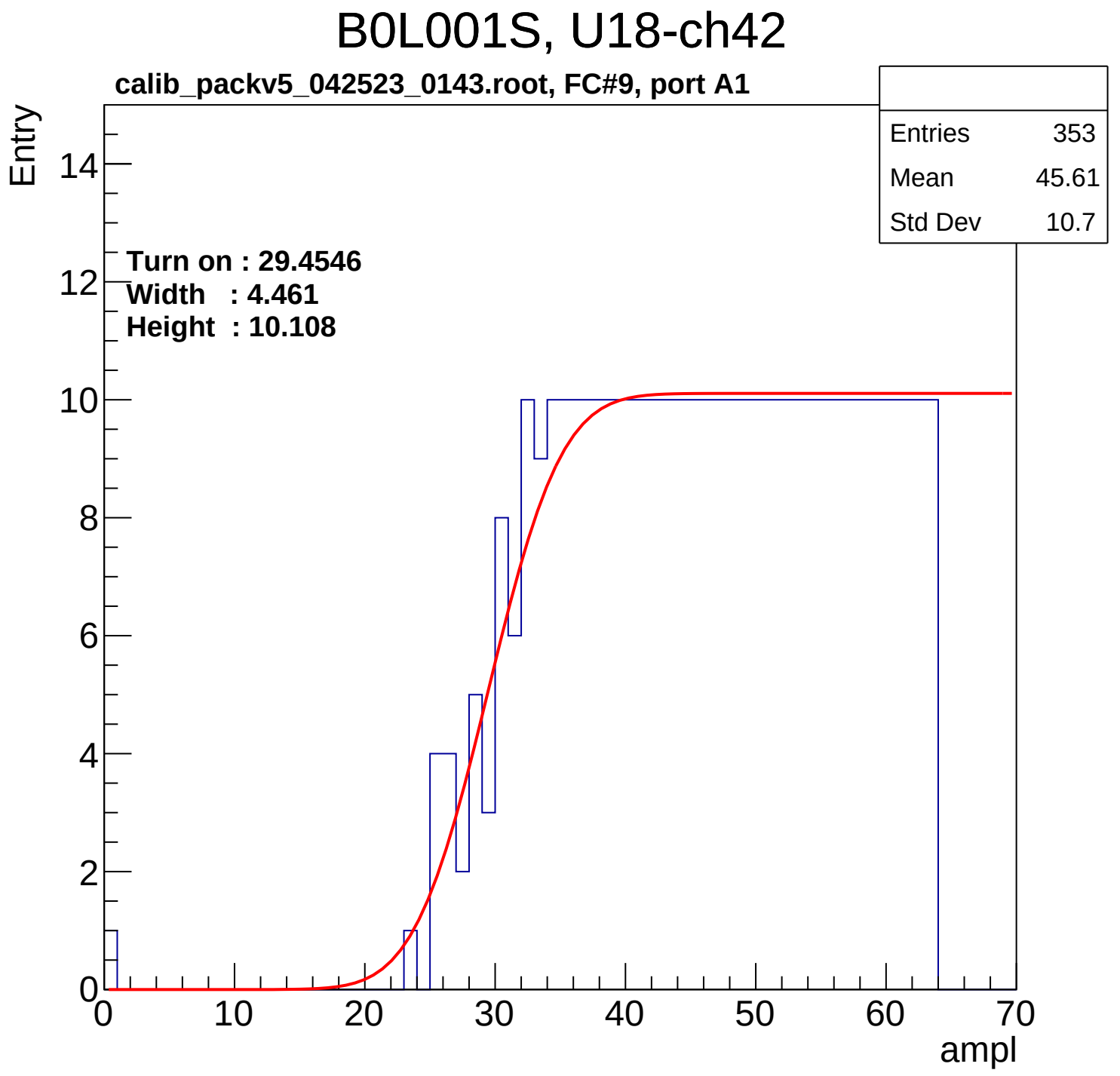

B0L001S, U18-ch37
calib_packv5_042523_0143.root, FC#9, port A1
Entries 385
Mean 43.93
Std Dev 11.85
Turn on : 25.7099
Width : 3.188
Height : 9.979
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

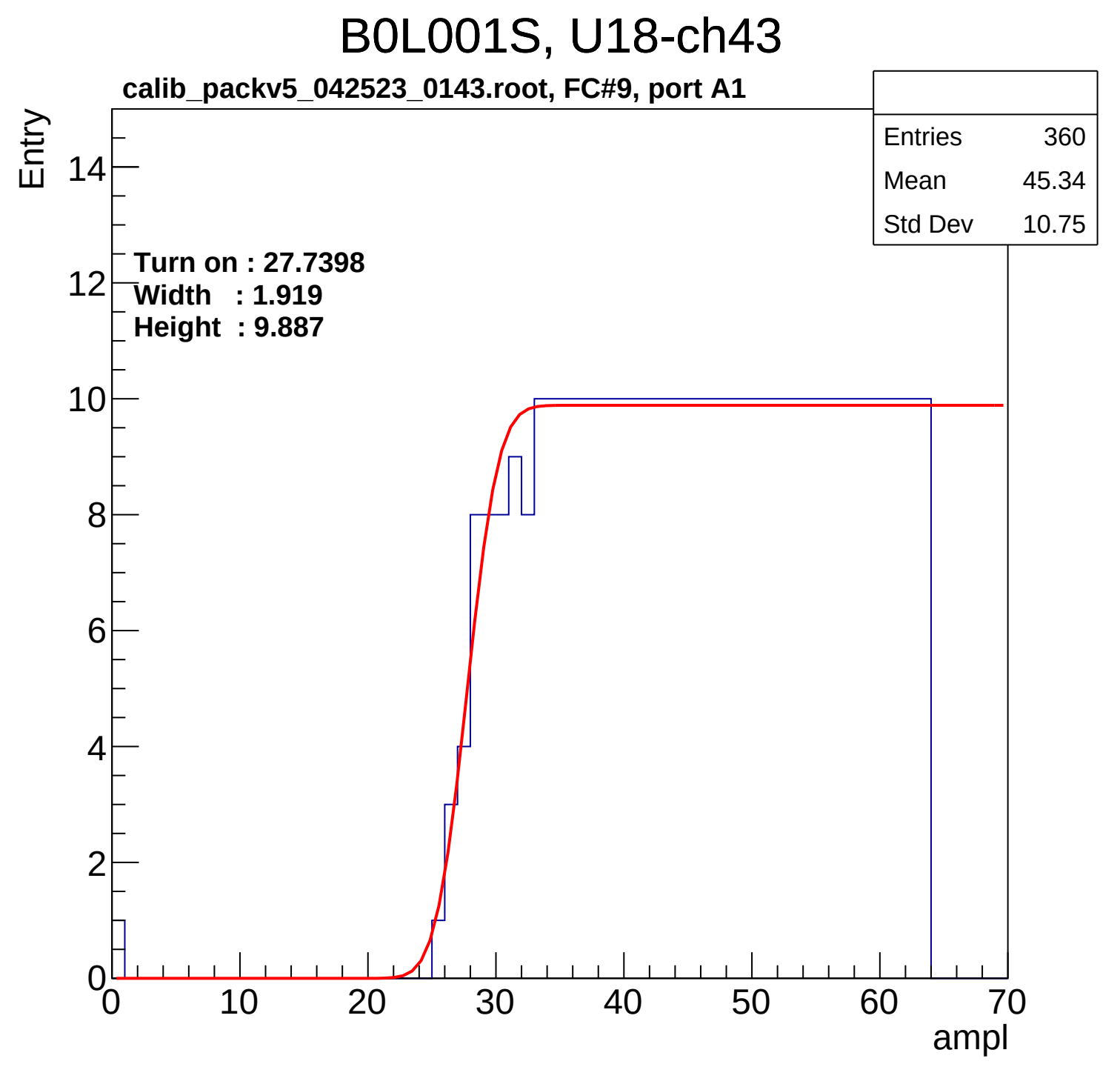

B0L001S, U18-ch38
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.73
Std Dev 11.75
Turn on : 28.0385
Width : 1.743
Height : 9.924
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

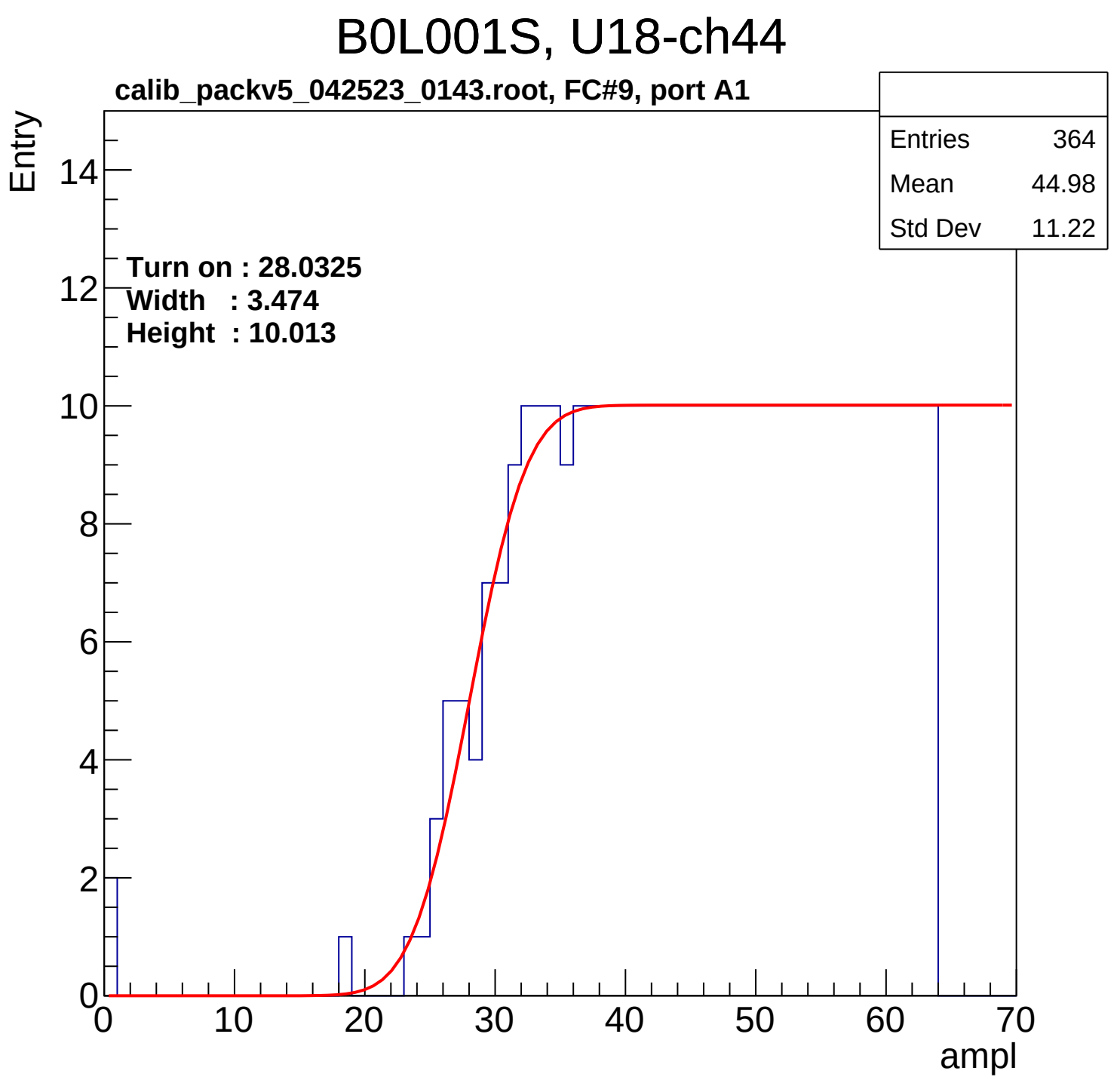

B0L001S, U18-ch39
calib_packv5_042523_0143.root, FC#9, port A1
Entries 347
Mean 46.03
Std Dev 10.51
Turn on : 29.6857
Width : 4.154
Height : 10.100
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

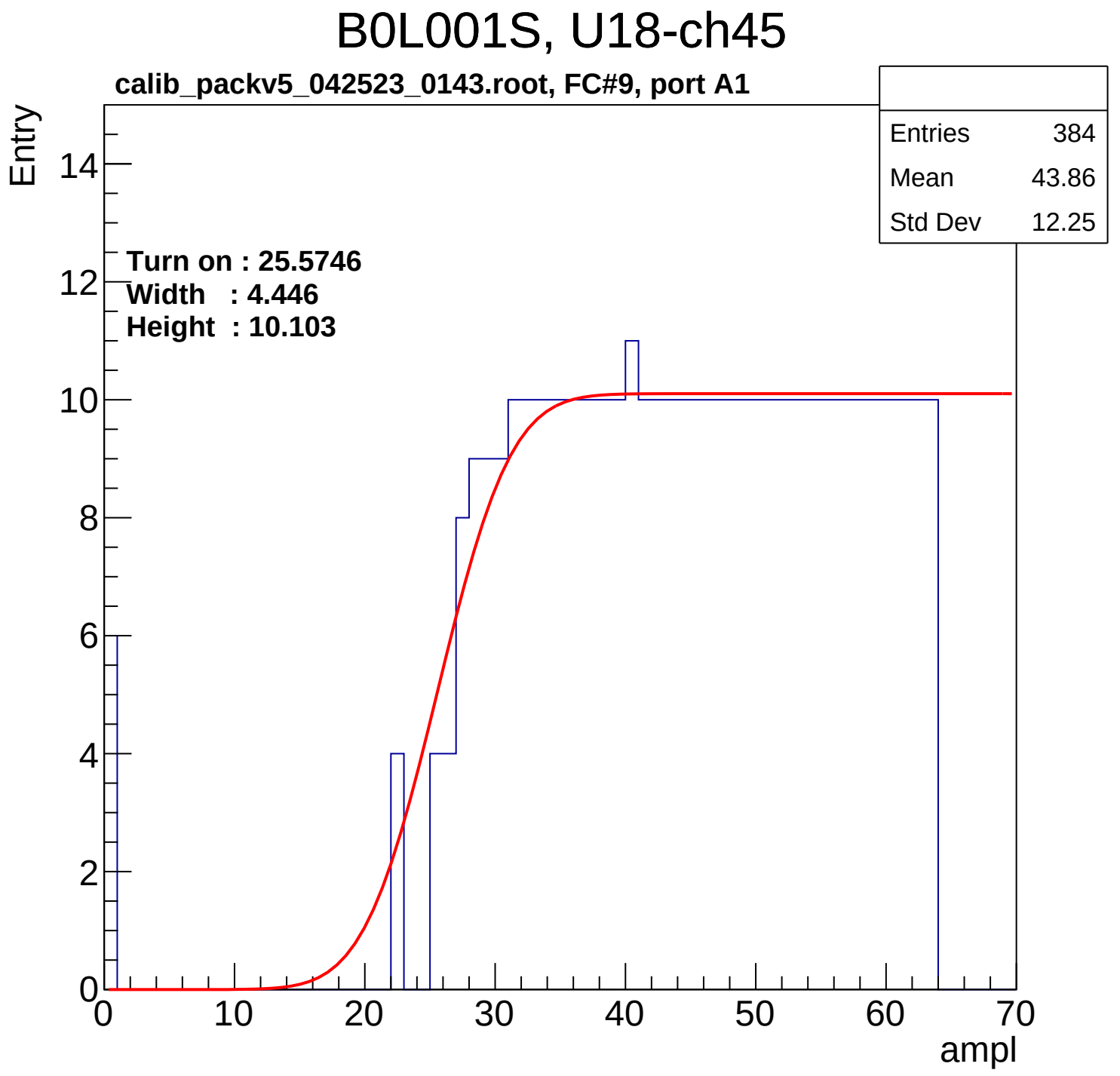

B0L001S, U18-ch40
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.1
Std Dev 11.2
Turn on : 29.0463
Width : 4.217
Height : 10.130
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

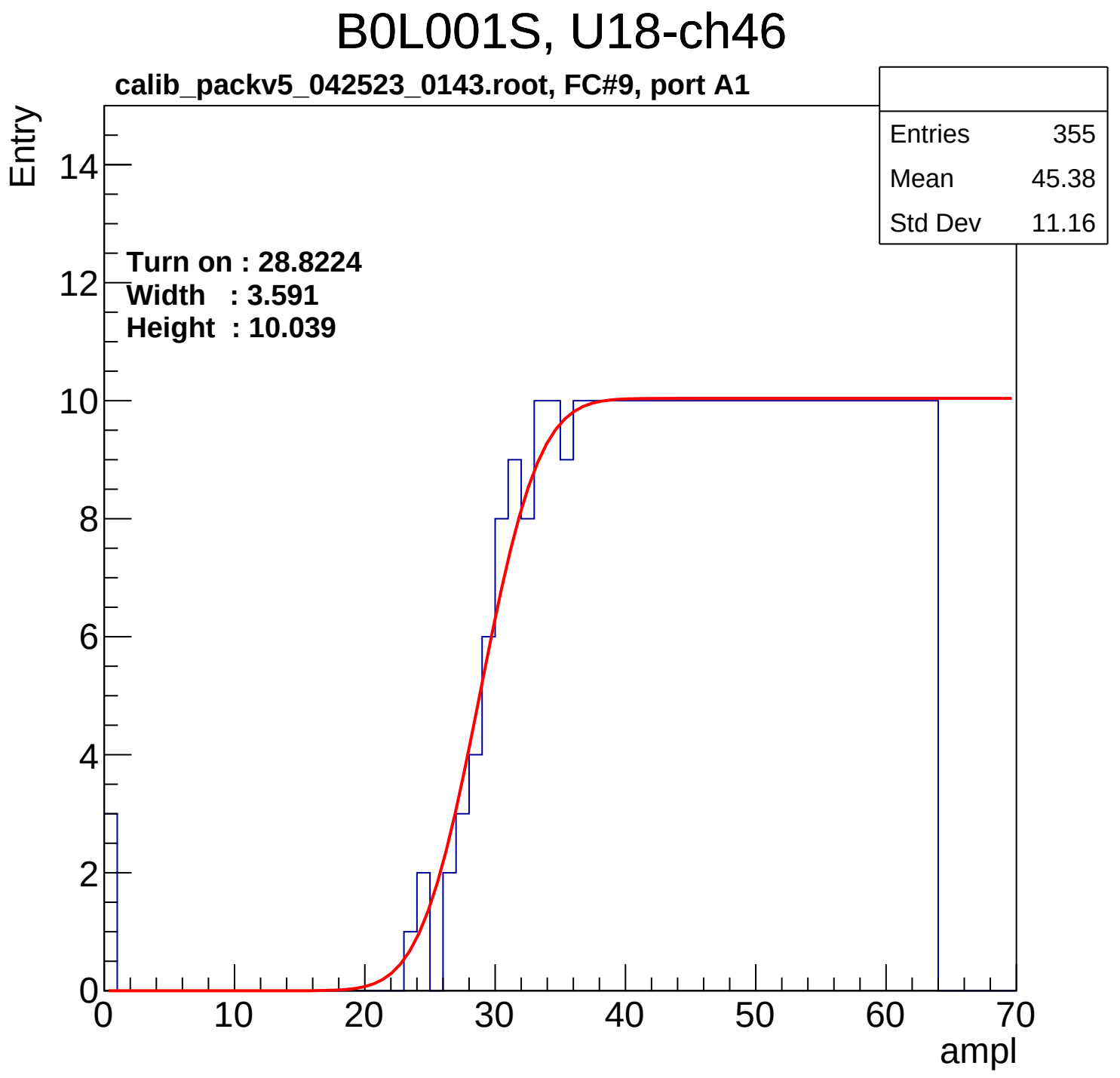

B0L001S, U18-ch41
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.41
Std Dev 11.14
Turn on : 29.3235
Width : 3.689
Height : 10.086
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

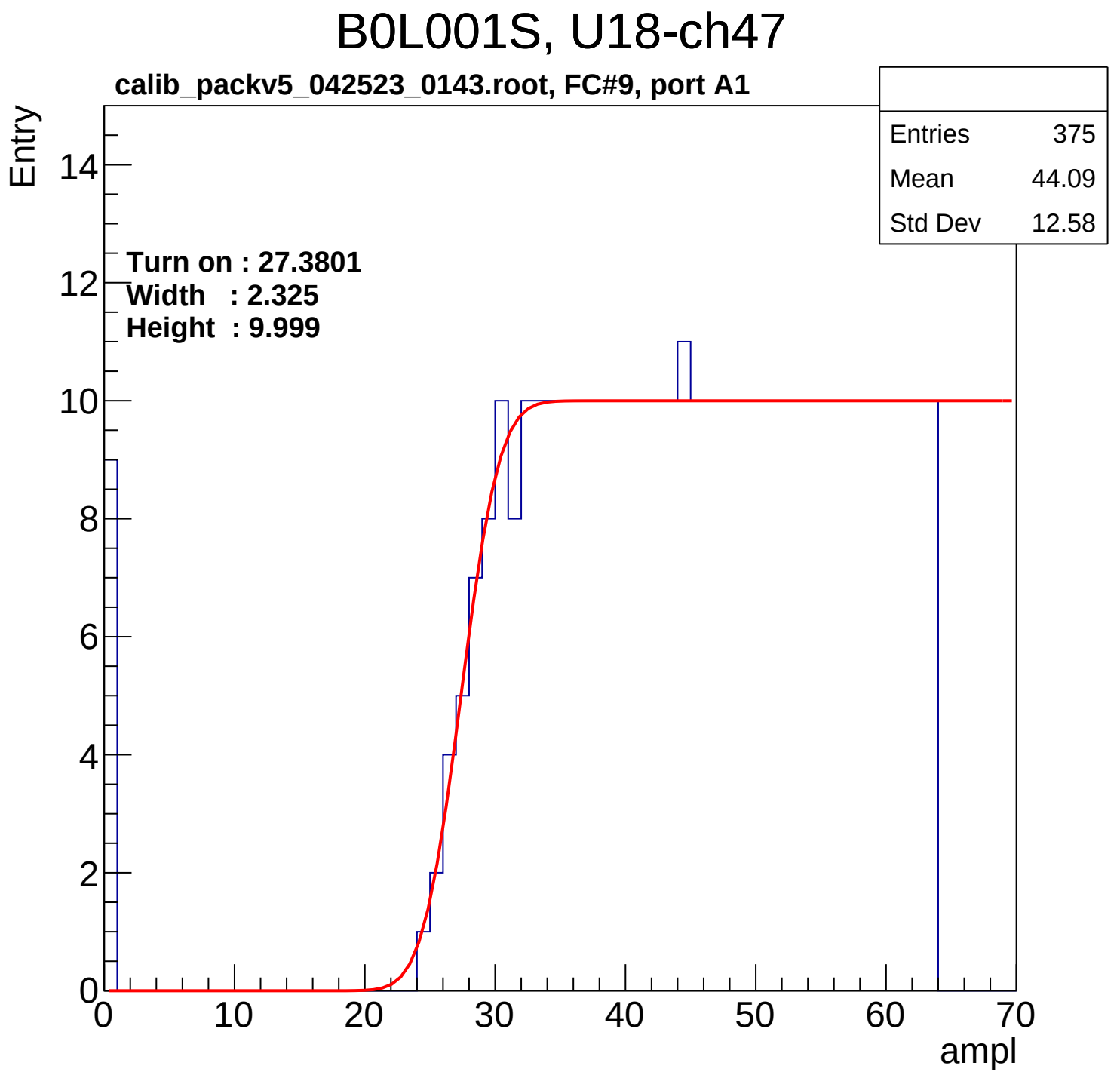

B0L001S, U18-ch42
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.61
Std Dev 10.7
Turn on : 29.4546
Width : 4.461
Height : 10.108
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

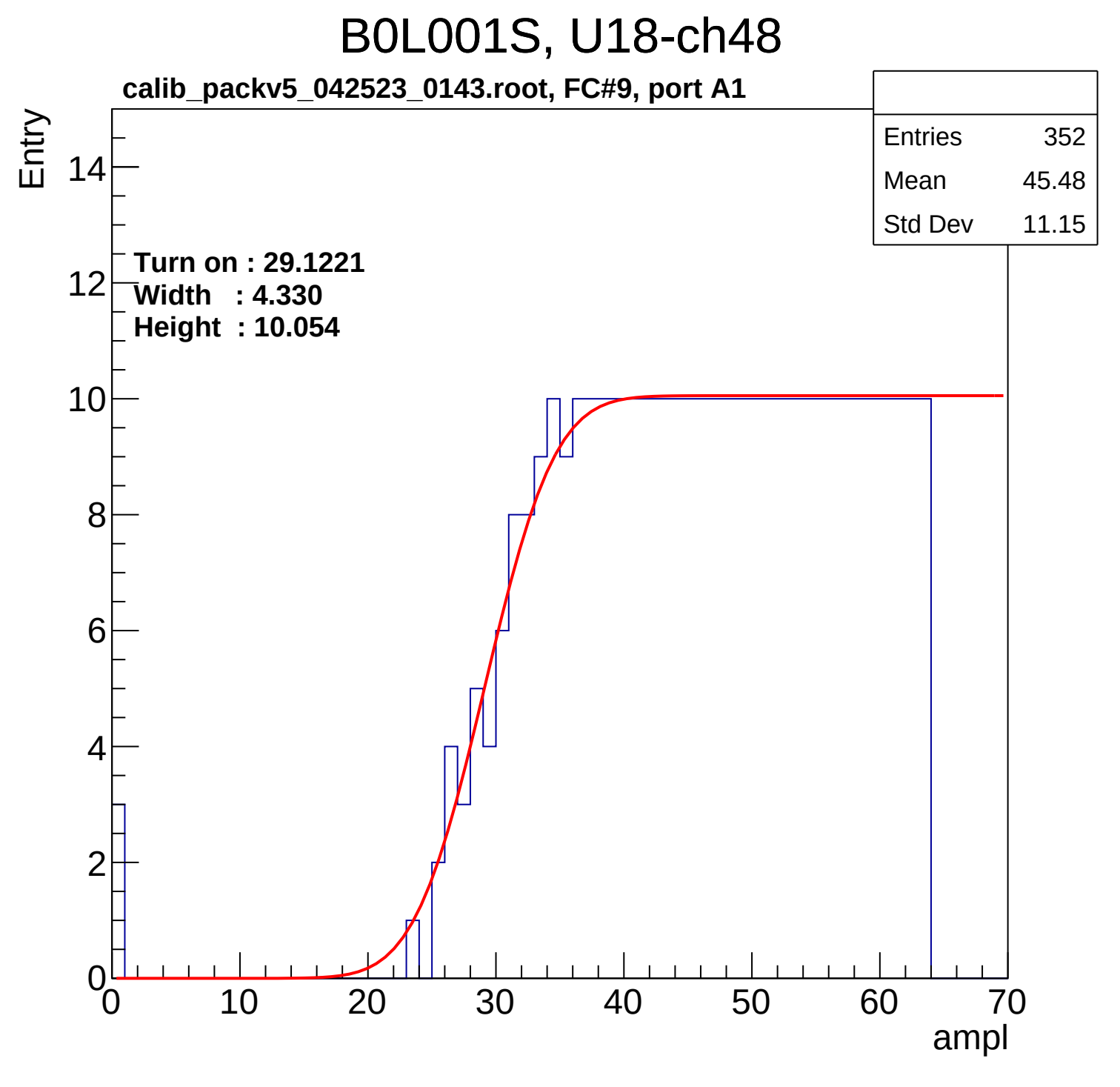

B0L001S, U18-ch43
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.34
Std Dev 10.75
Turn on : 27.7398
Width : 1.919
Height : 9.887
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

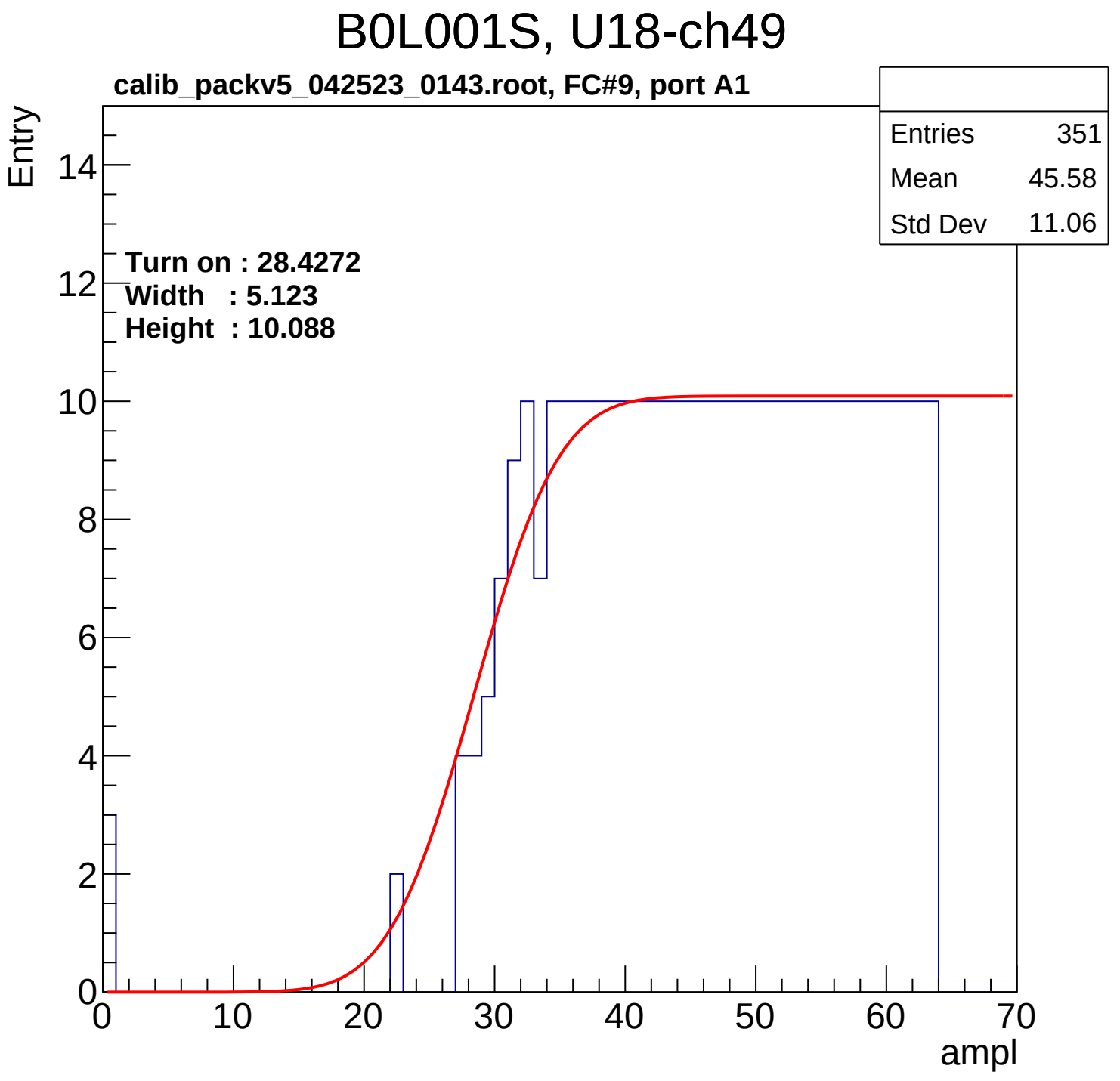

B0L001S, U18-ch44
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.98
Std Dev 11.22
Turn on : 28.0325
Width : 3.474
Height : 10.013
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

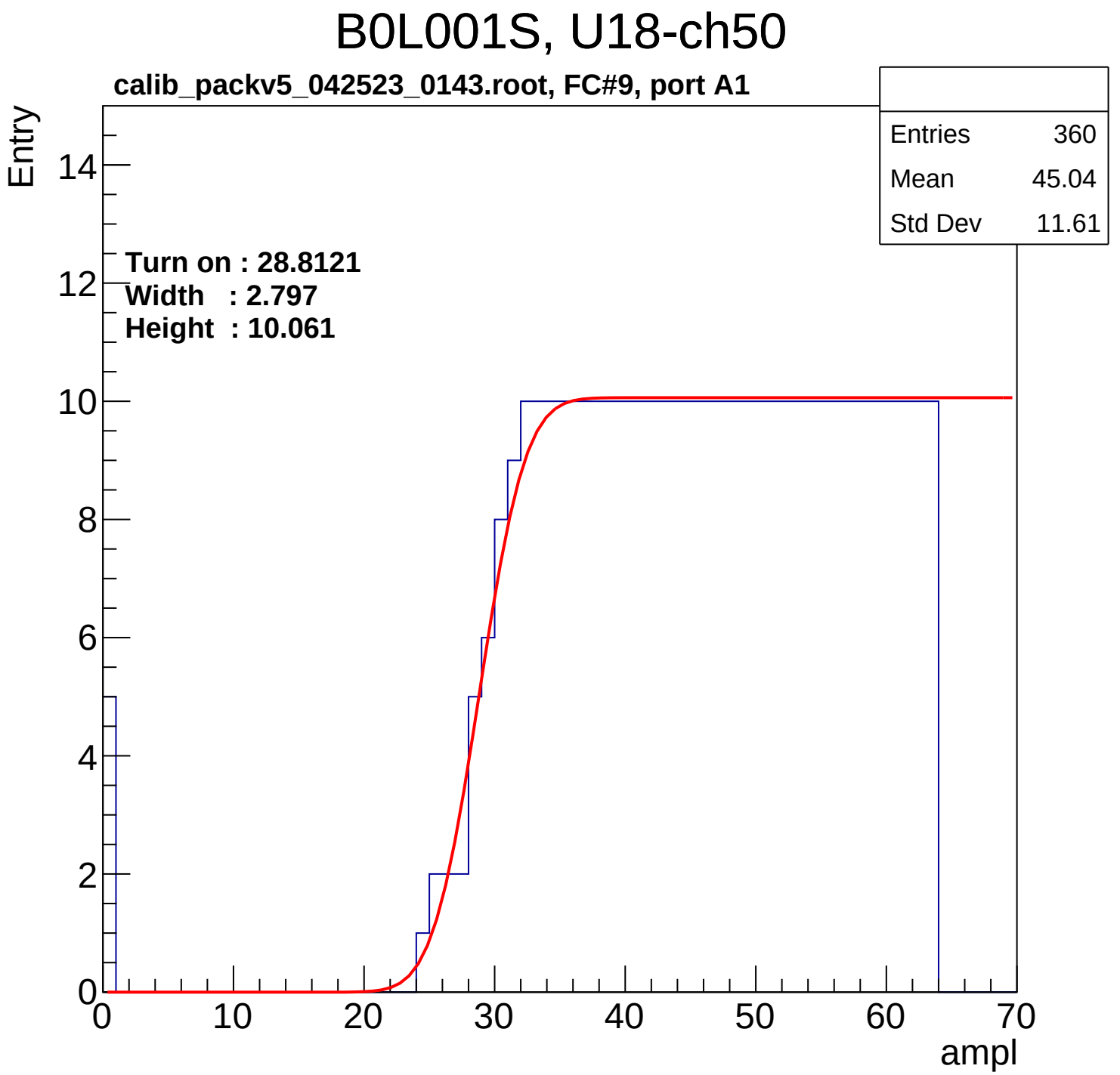

B0L001S, U18-ch45
calib_packv5_042523_0143.root, FC#9, port A1
Entries 384
Mean 43.86
Std Dev 12.25
Turn on : 25.5746
Width : 4.446
Height : 10.103
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

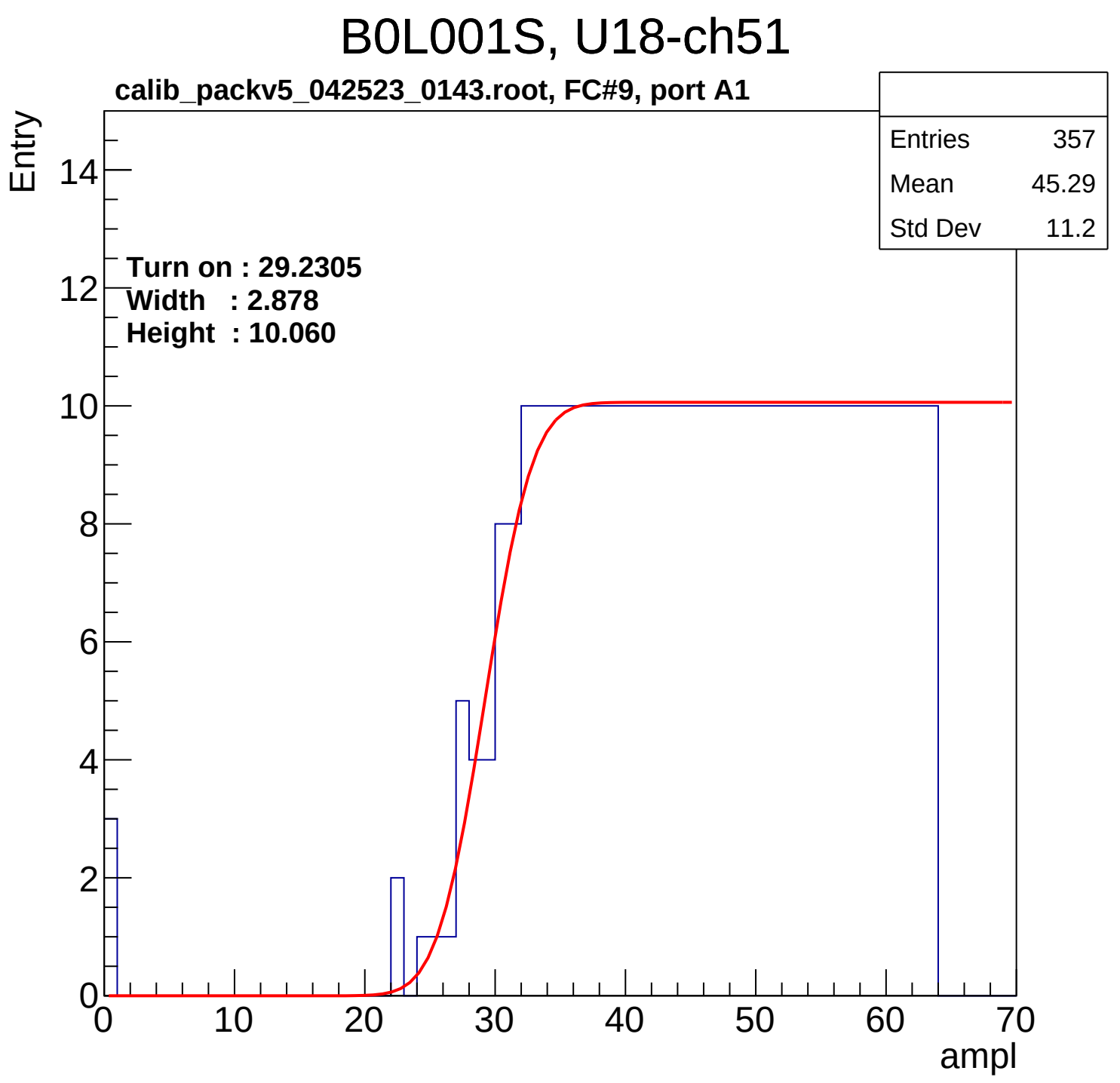

B0L001S, U18-ch46
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.38
Std Dev 11.16
Turn on : 28.8224
Width : 3.591
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

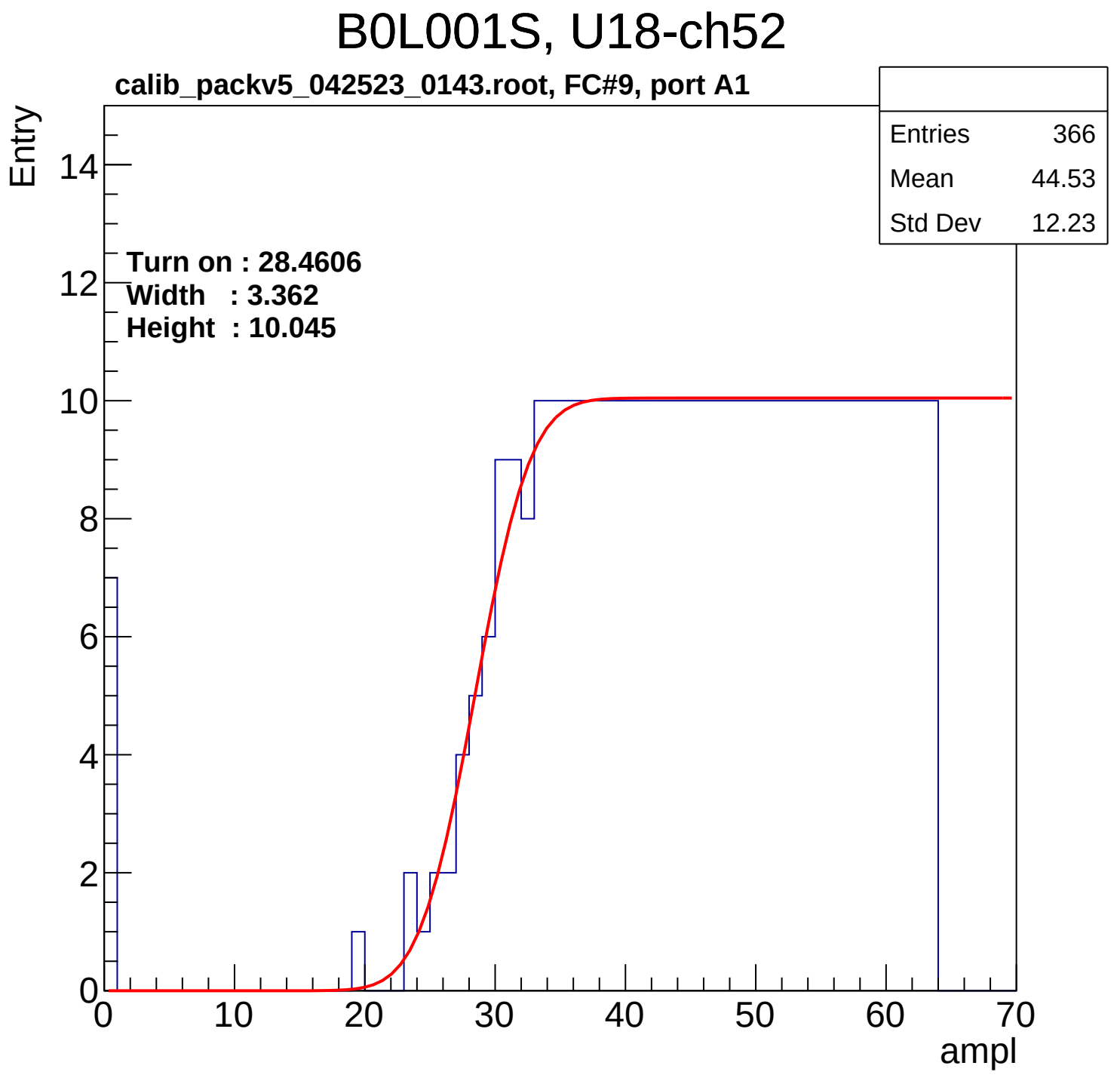

B0L001S, U18-ch47
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.09
Std Dev 12.58
Turn on : 27.3801
Width : 2.325
Height : 9.999
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

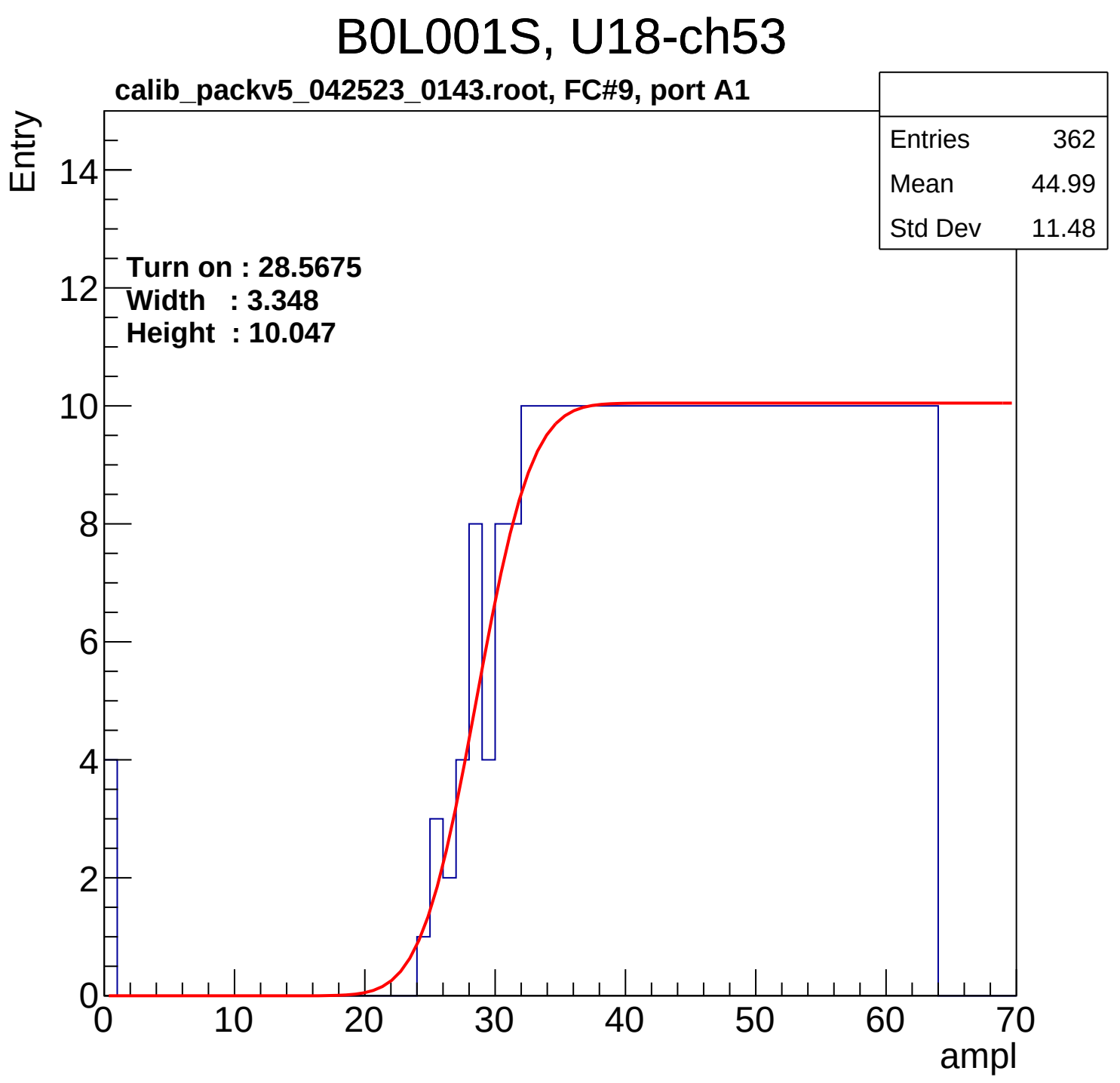

B0L001S, U18-ch48
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.48
Std Dev 11.15
Turn on : 29.1221
Width : 4.330
Height : 10.054
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

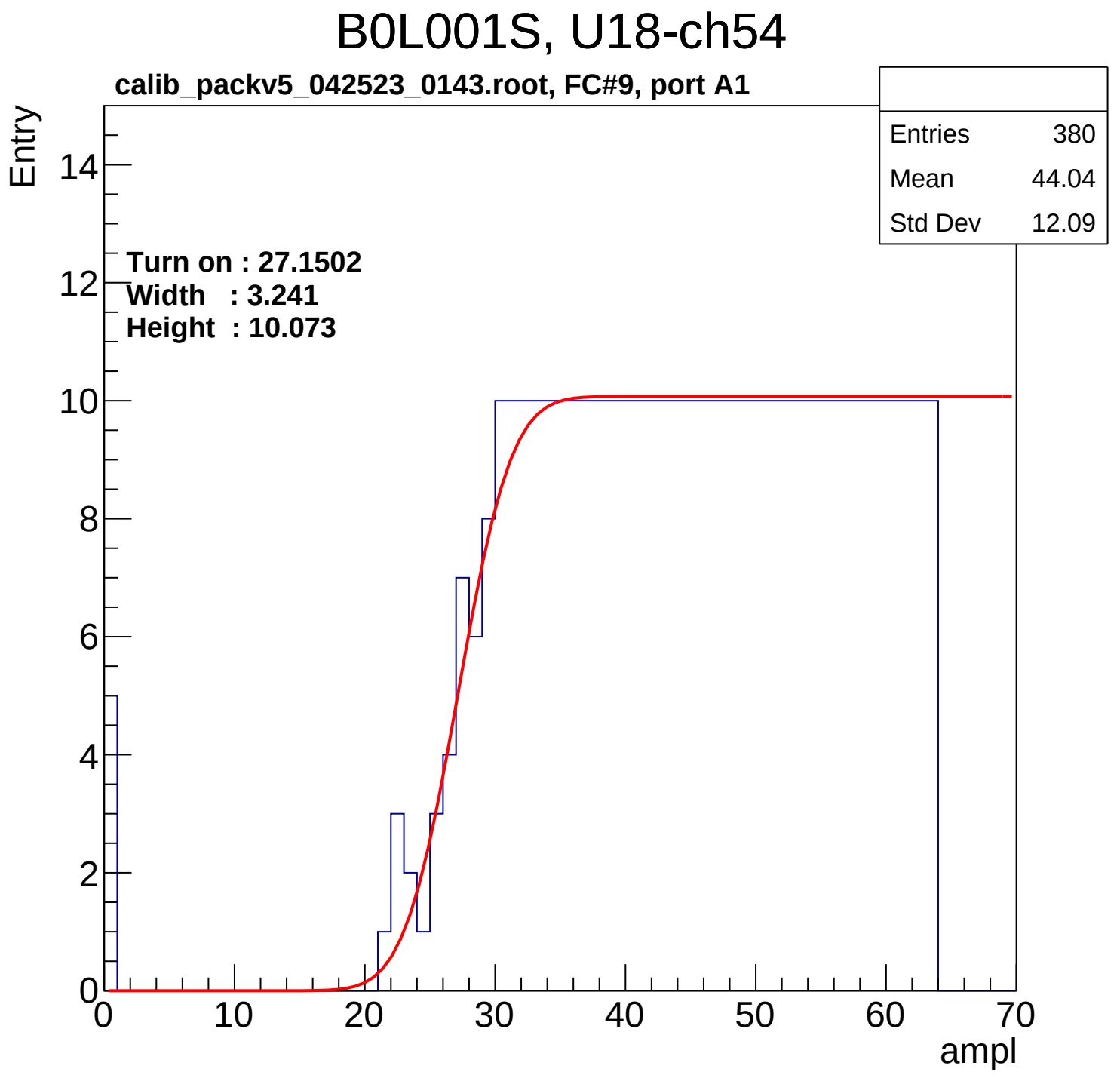

B0L001S, U18-ch49
calib_packv5_042523_0143.root, FC#9, port A1
Entries 351
Mean 45.58
Std Dev 11.06
Turn on : 28.4272
Width : 5.123
Height : 10.088
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

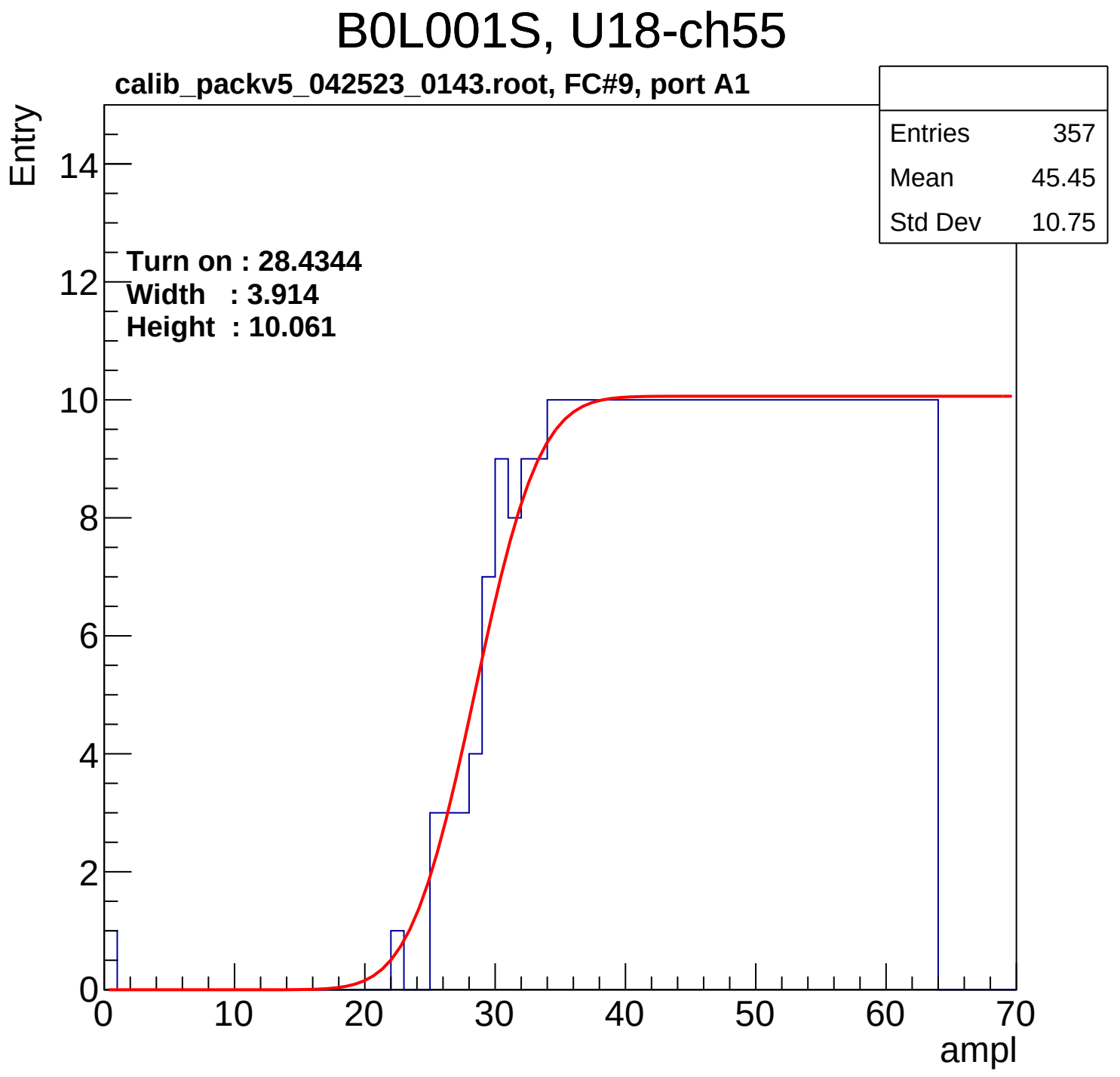

B0L001S, U18-ch50
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.04
Std Dev 11.61
Turn on : 28.8121
Width : 2.797
Height : 10.061
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

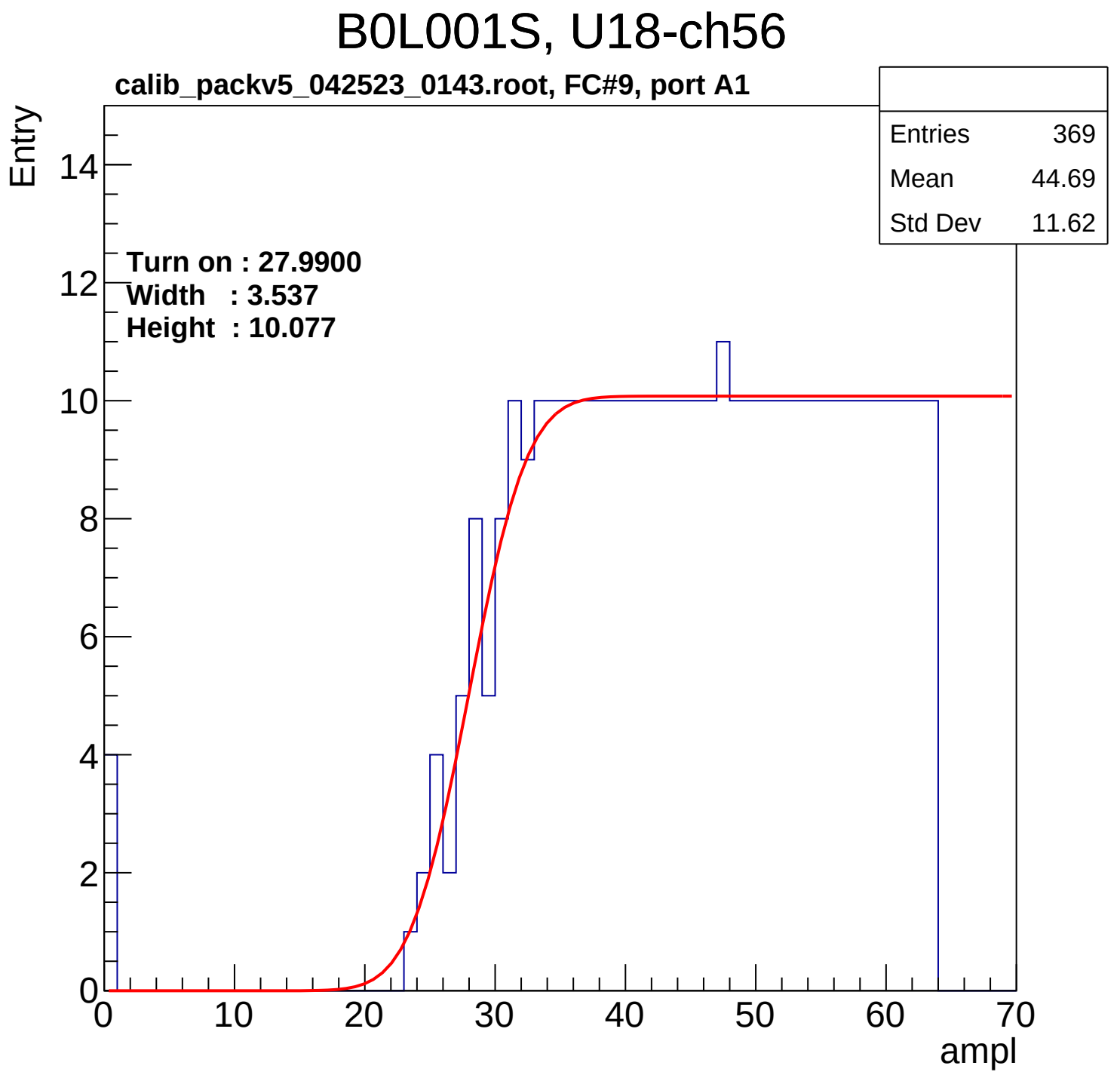

B0L001S, U18-ch51
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.29
Std Dev 11.2
Turn on : 29.2305
Width : 2.878
Height : 10.060
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

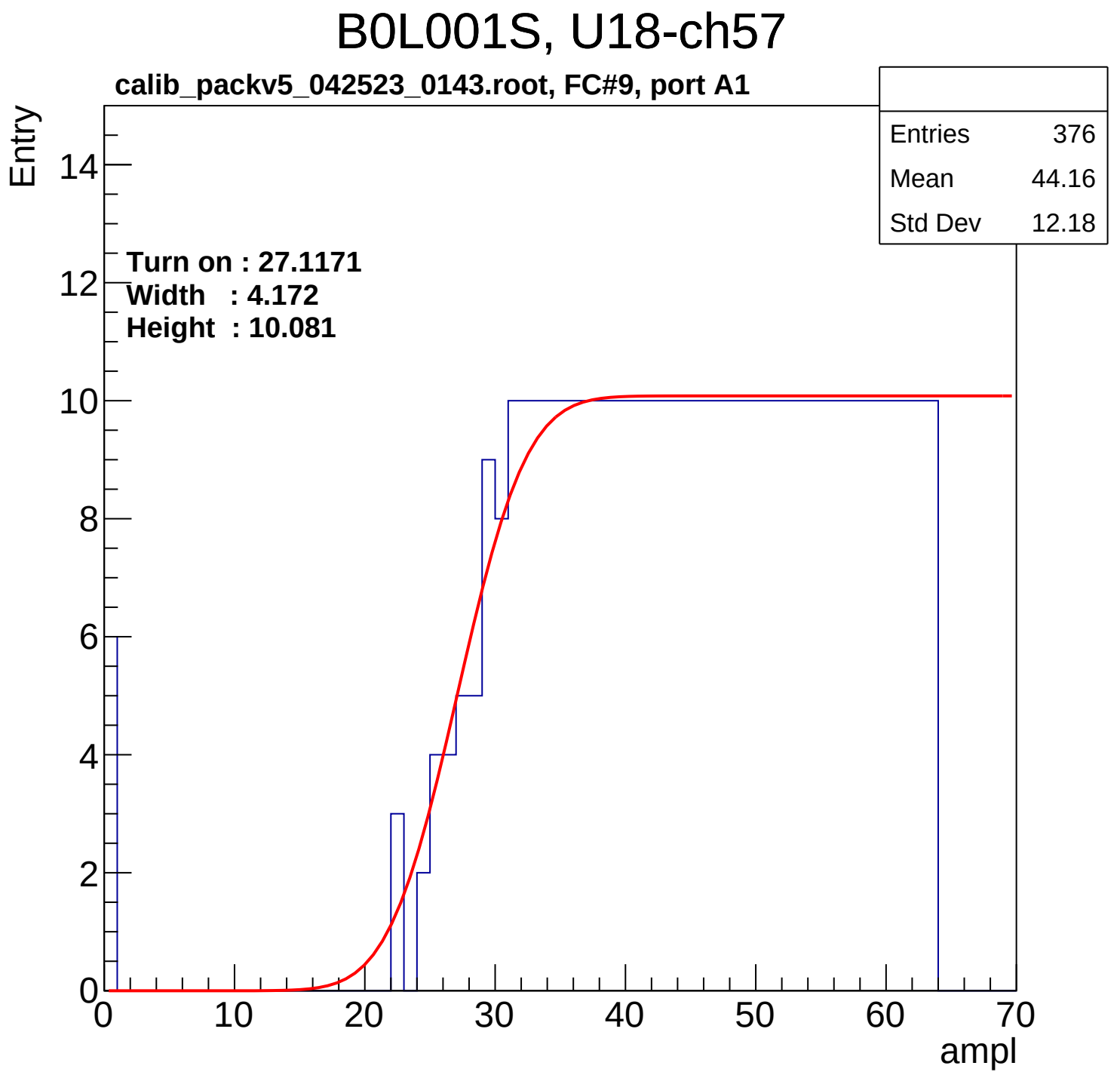

B0L001S, U18-ch52
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.53
Std Dev 12.23
Turn on : 28.4606
Width : 3.362
Height : 10.045
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

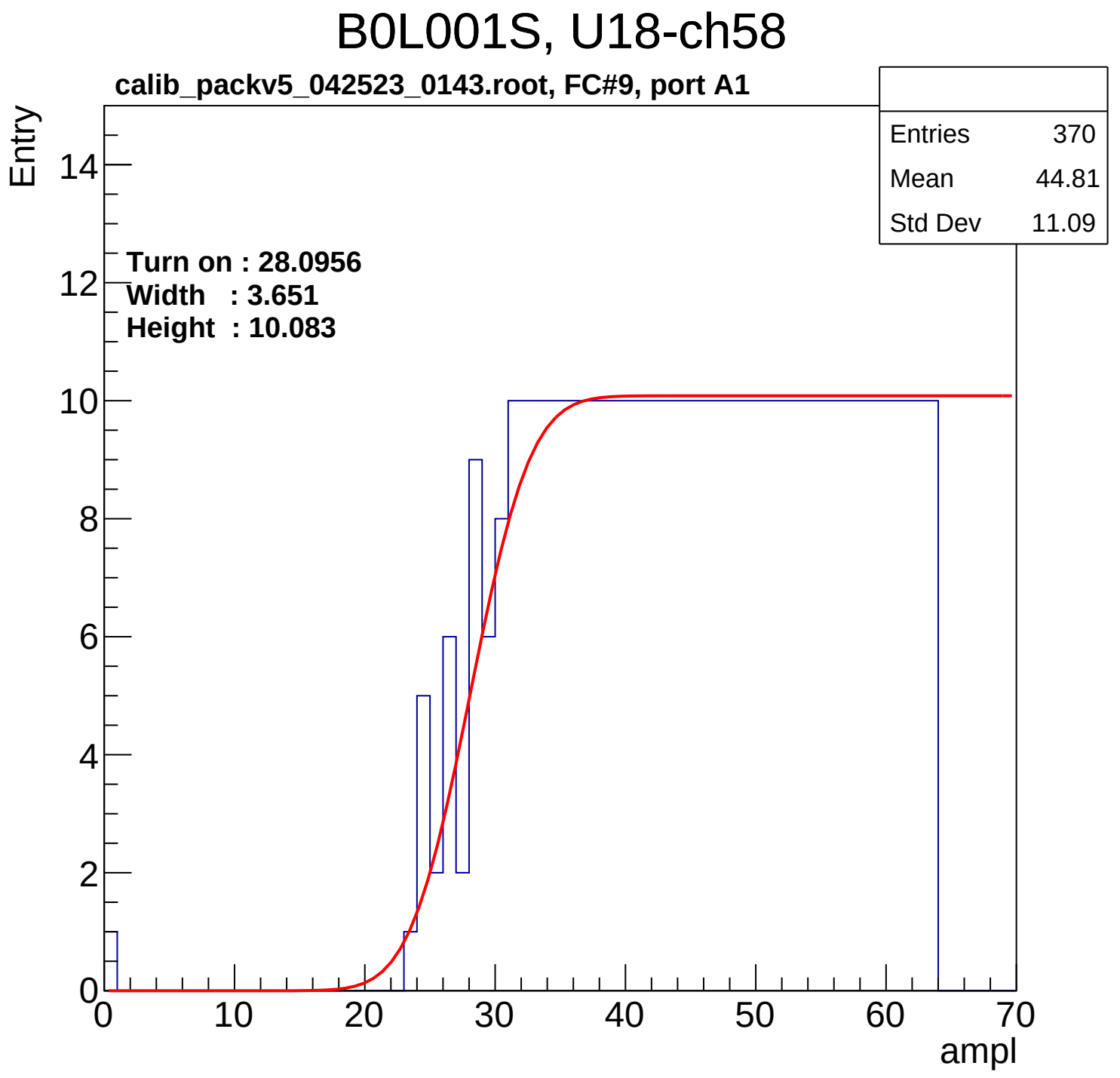

B0L001S, U18-ch53
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 44.99
Std Dev 11.48
Turn on : 28.5675
Width : 3.348
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

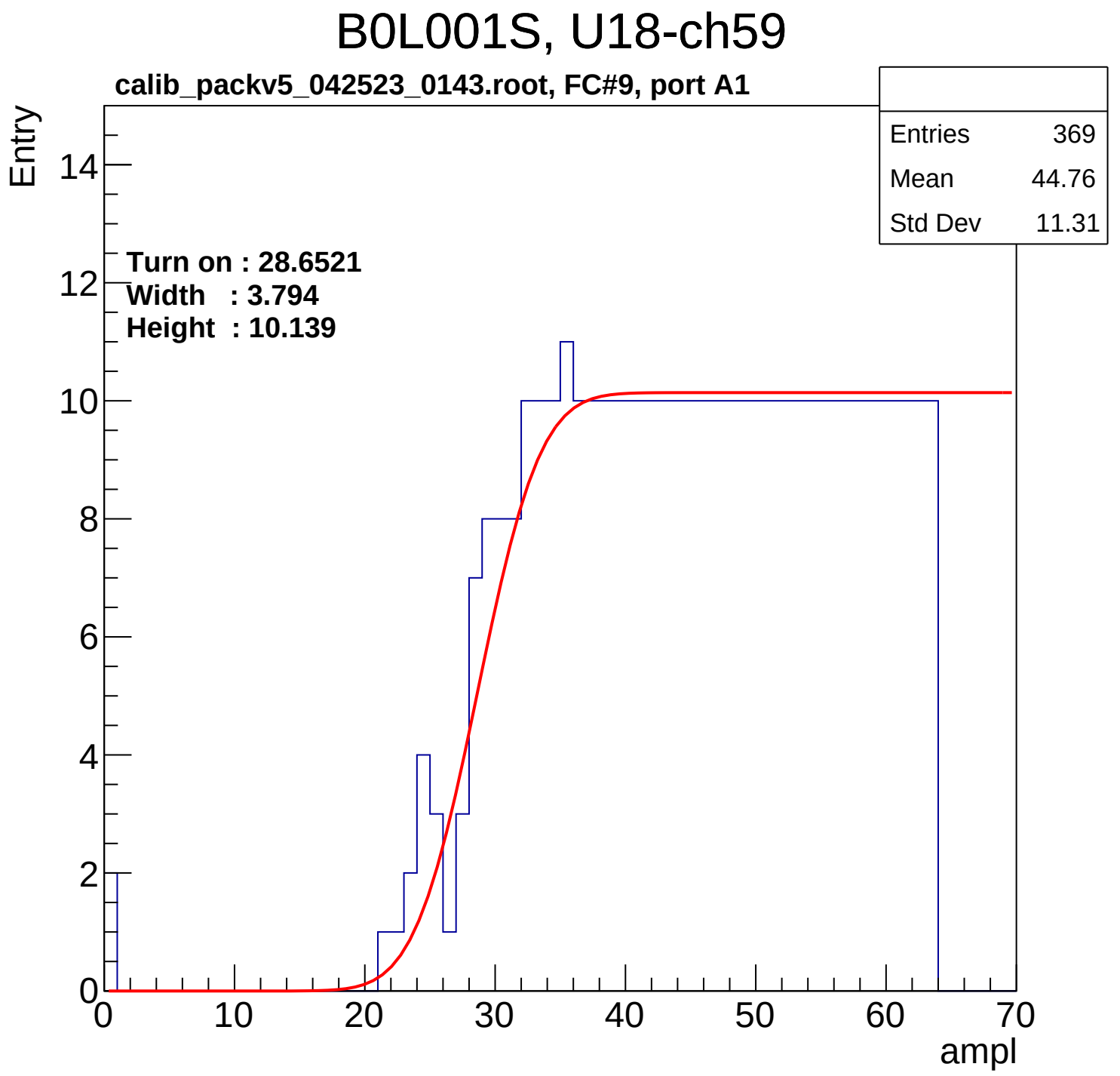

B0L001S, U18-ch54
calib_packv5_042523_0143.root, FC#9, port A1
Entries 380
Mean 44.04
Std Dev 12.09
Turn on : 27.1502
Width : 3.241
Height : 10.073
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

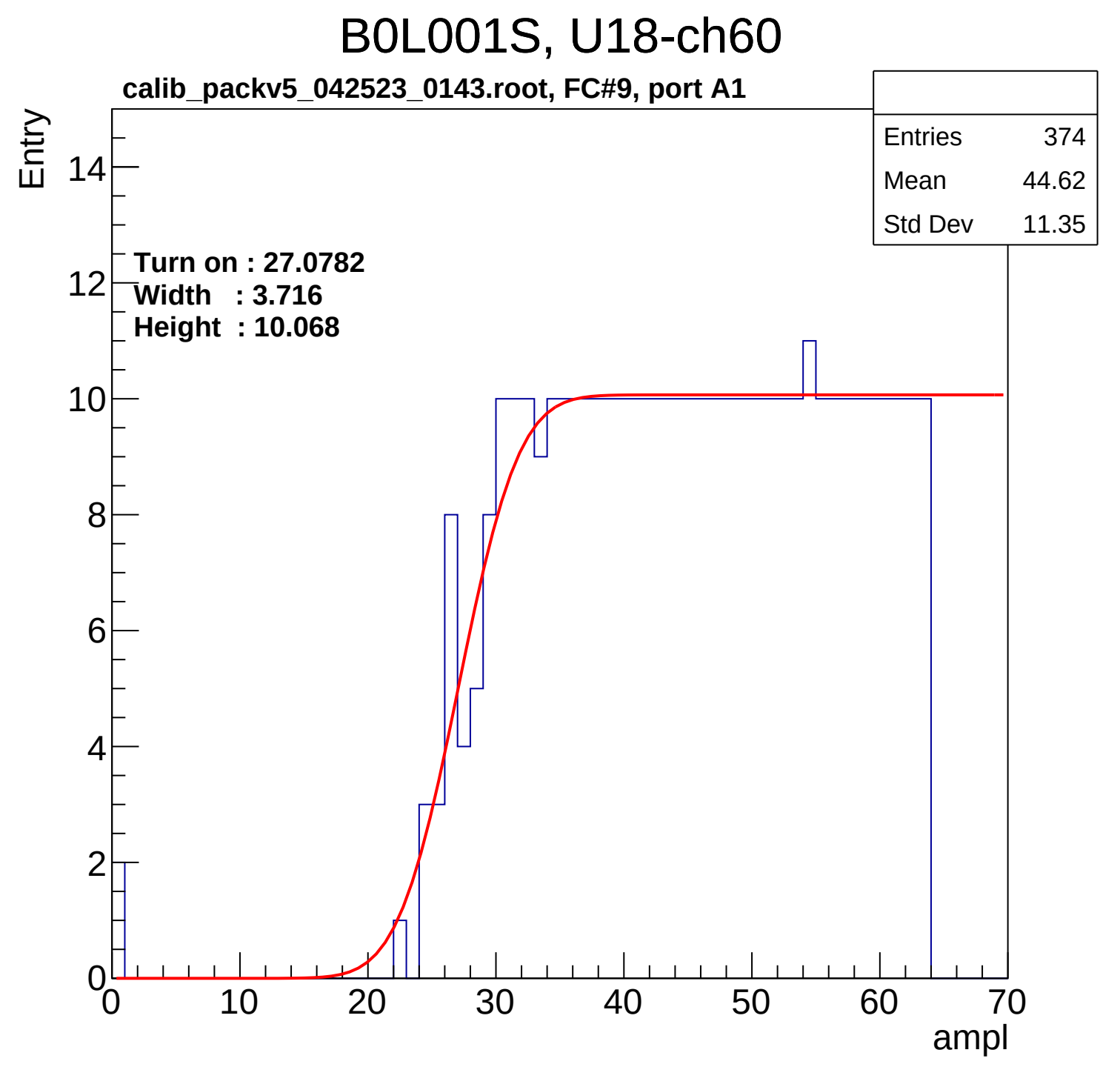

B0L001S, U18-ch55
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.45
Std Dev 10.75
Turn on : 28.4344
Width : 3.914
Height : 10.061
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

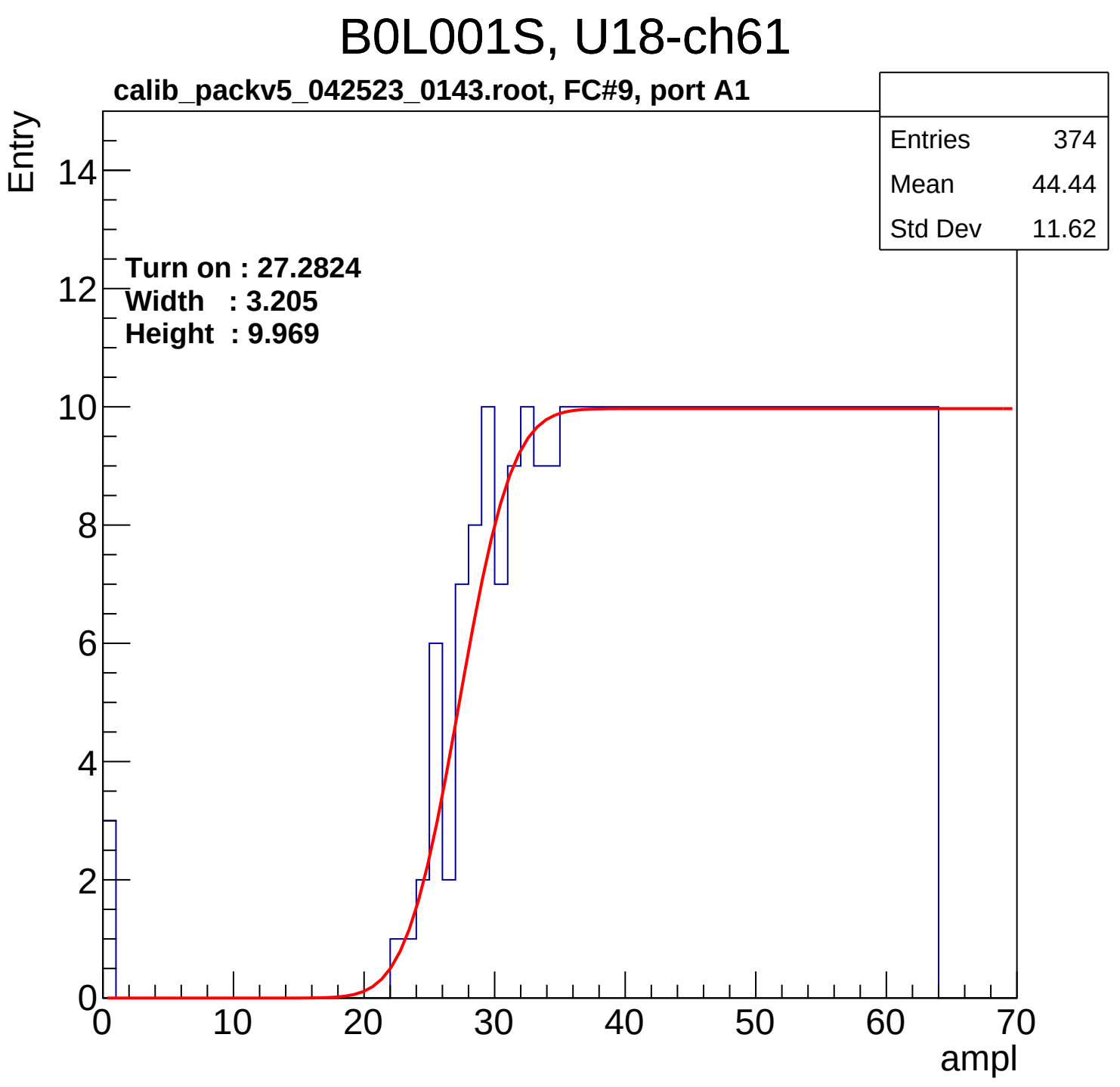

B0L001S, U18-ch56
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.69
Std Dev 11.62
Turn on : 27.9900
Width : 3.537
Height : 10.077
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

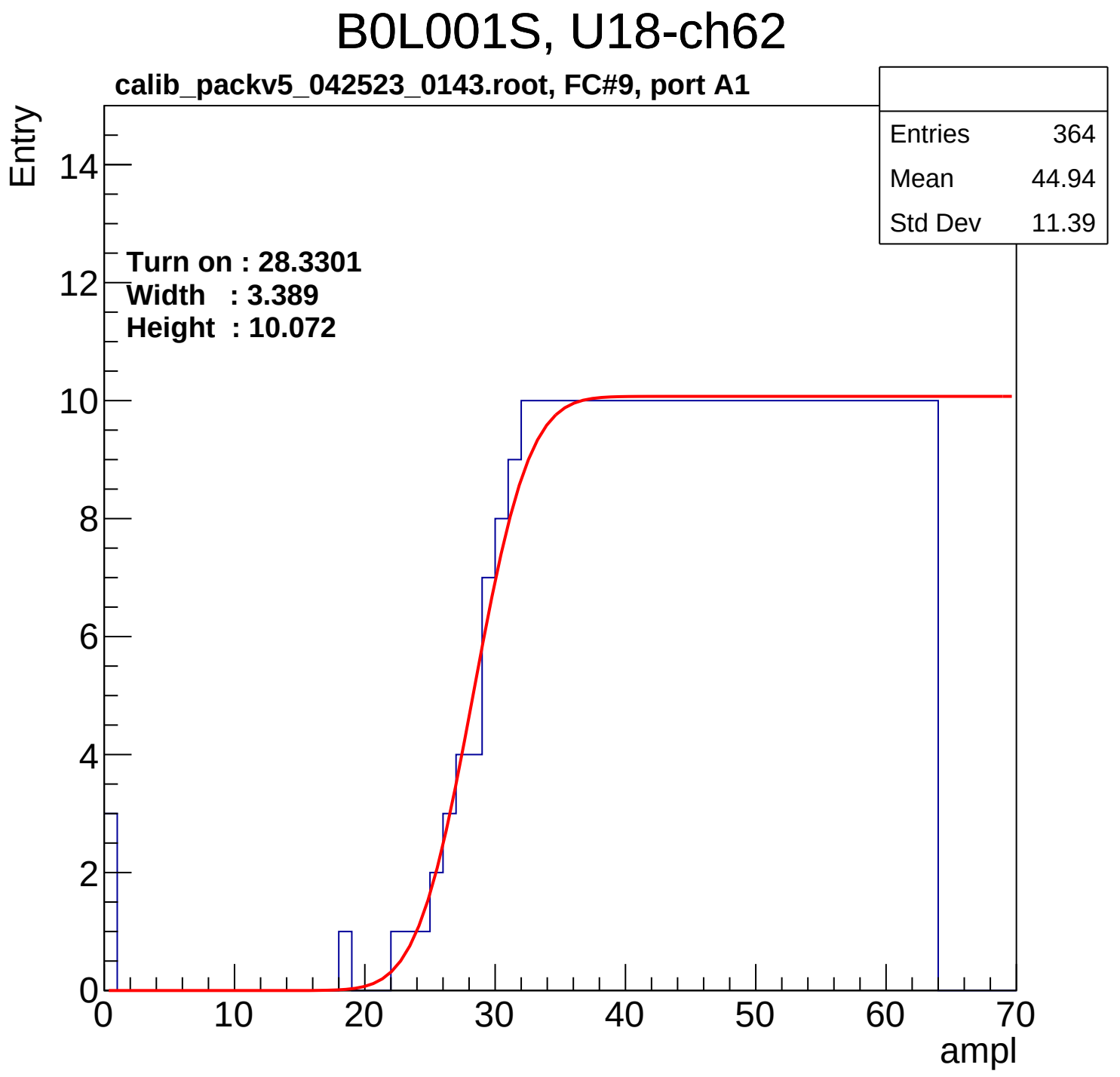

B0L001S, U18-ch57
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.16
Std Dev 12.18
Turn on : 27.1171
Width : 4.172
Height : 10.081
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

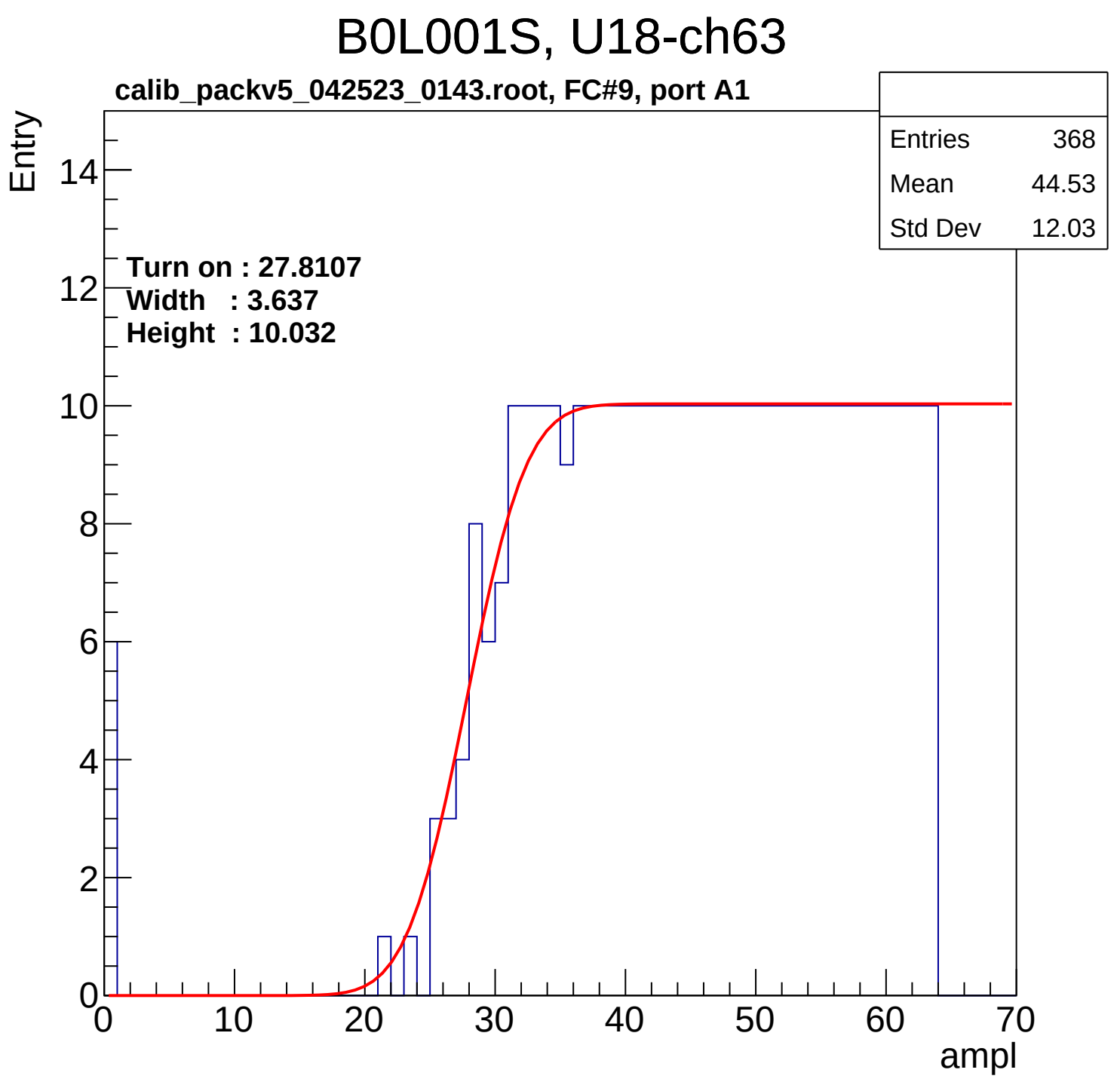

B0L001S, U18-ch58
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.81
Std Dev 11.09
Turn on : 28.0956
Width : 3.651
Height : 10.083
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

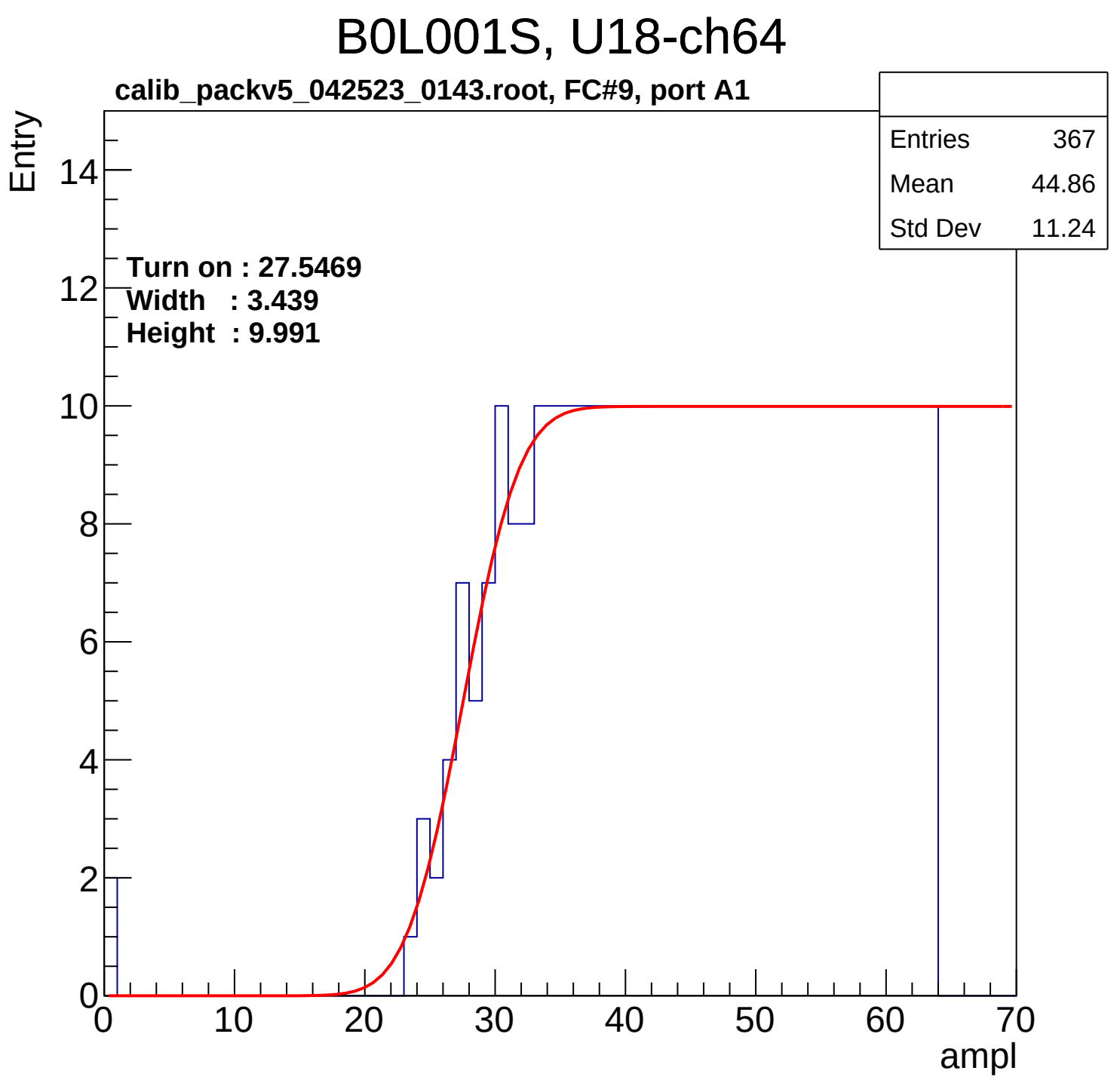

B0L001S, U18-ch59
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.76
Std Dev 11.31
Turn on : 28.6521
Width : 3.794
Height : 10.139
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

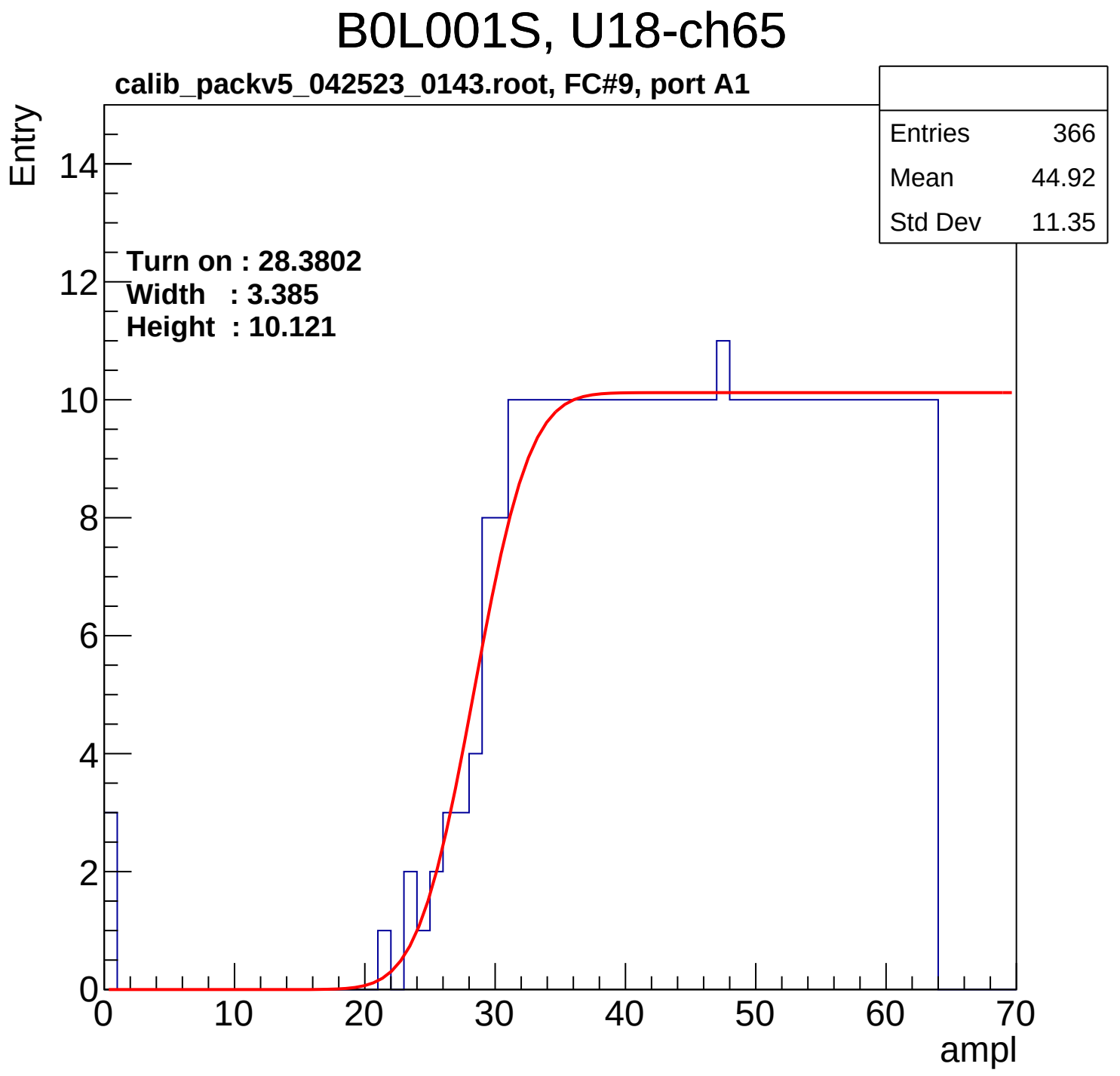

B0L001S, U18-ch60
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.62
Std Dev 11.35
Turn on : 27.0782
Width : 3.716
Height : 10.068
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

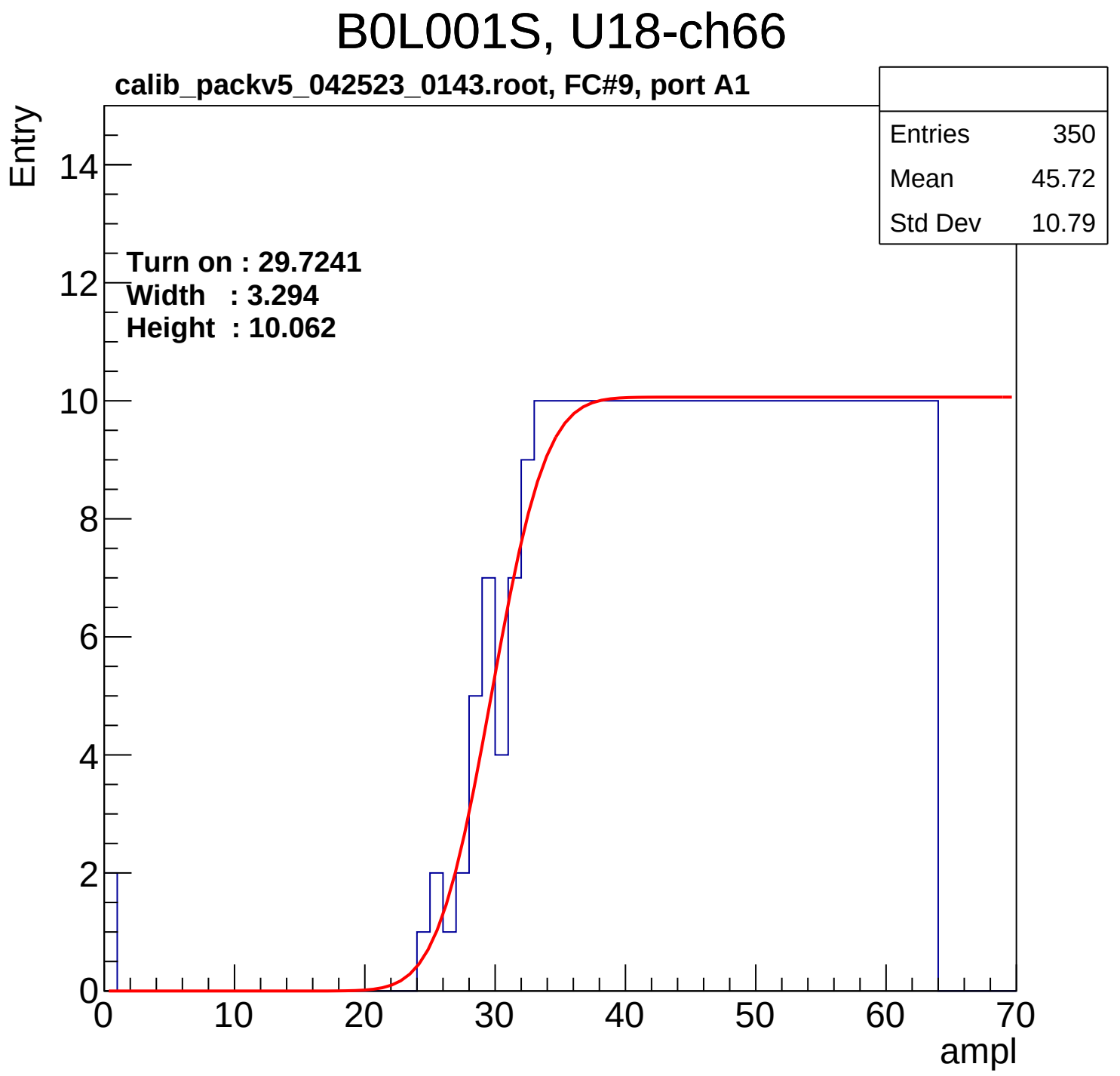

B0L001S, U18-ch61
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.44
Std Dev 11.62
Turn on : 27.2824
Width : 3.205
Height : 9.969
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

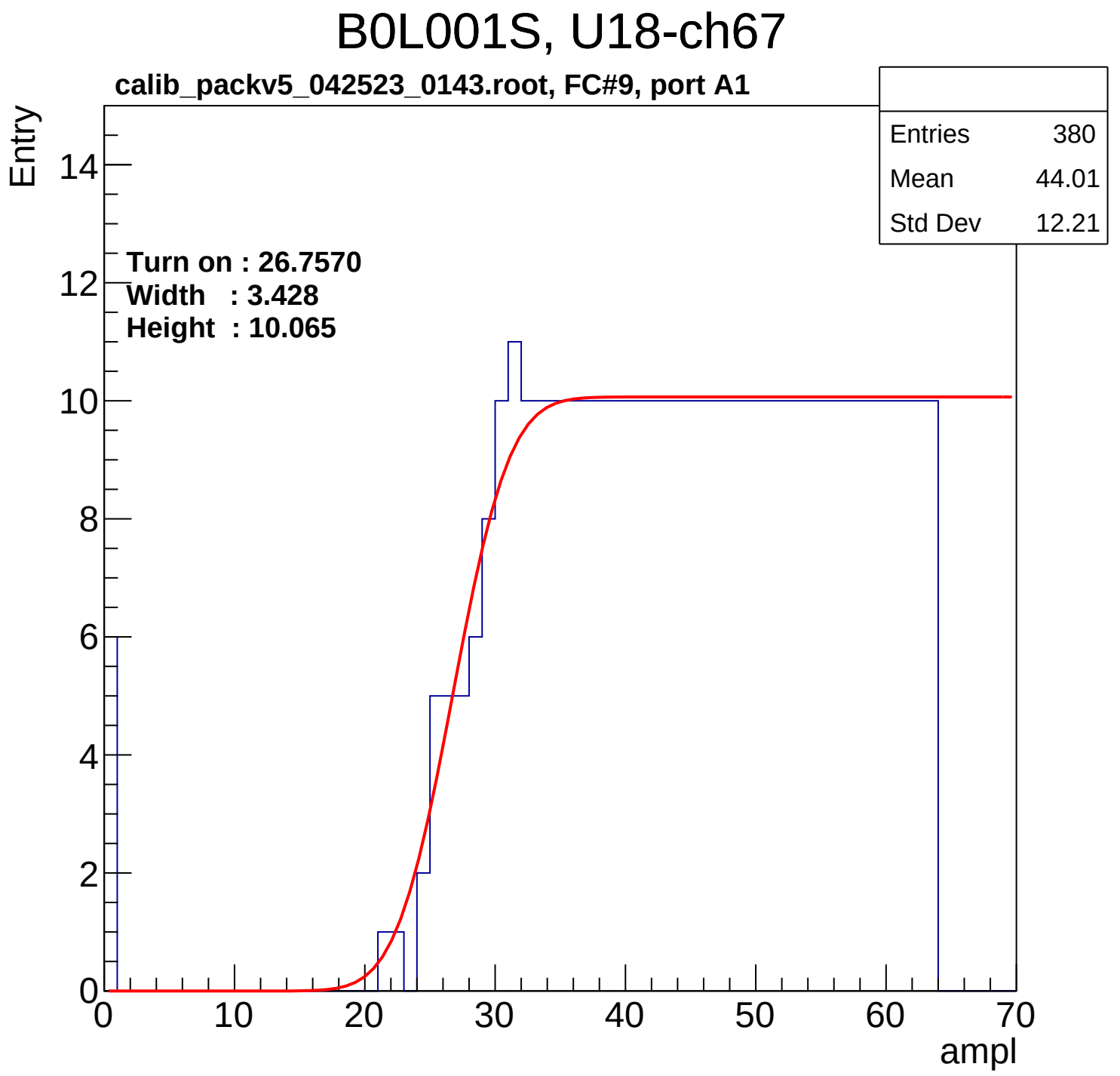

B0L001S, U18-ch62
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.94
Std Dev 11.39
Turn on : 28.3301
Width : 3.389
Height : 10.072
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

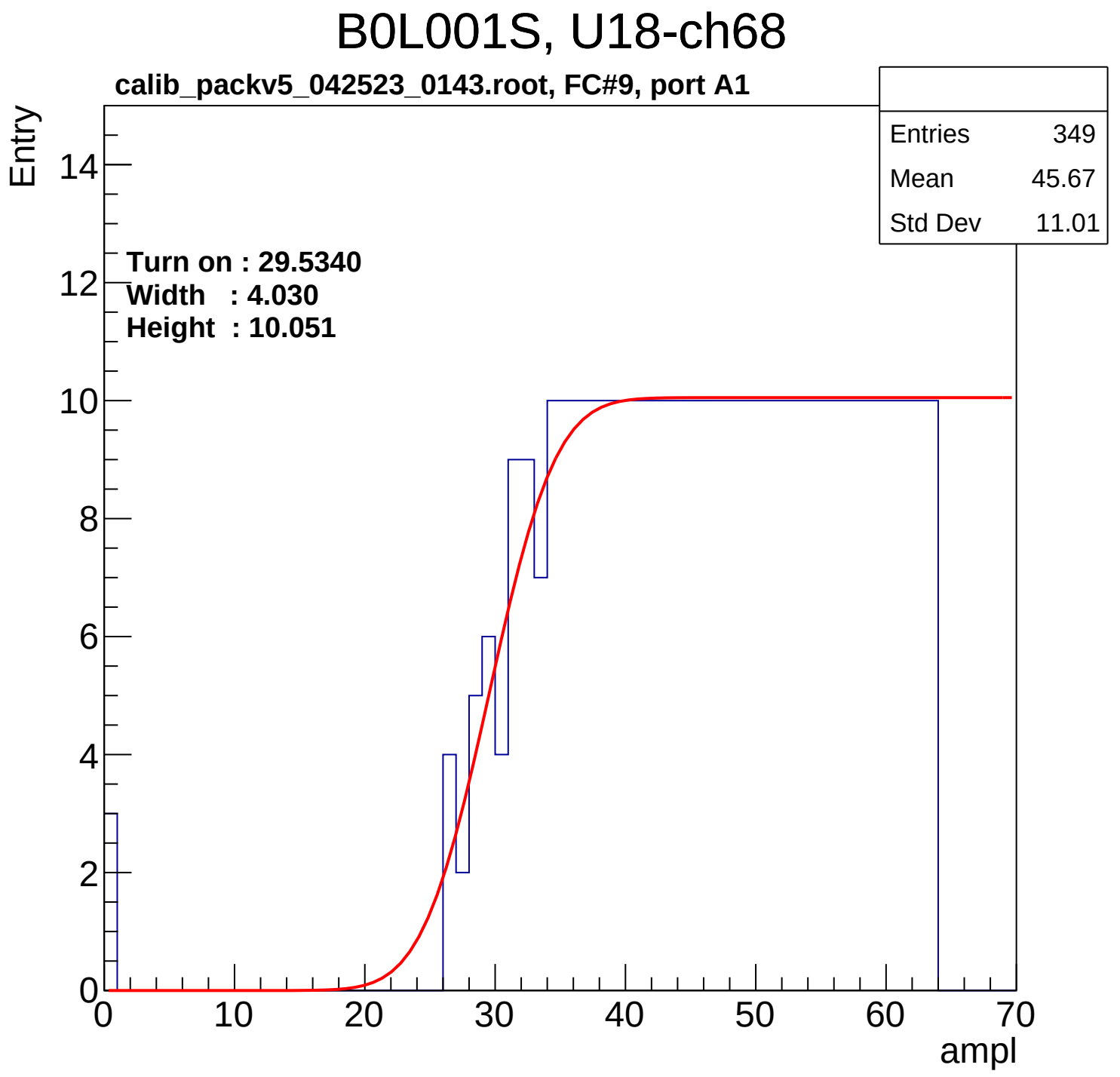

B0L001S, U18-ch63
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.53
Std Dev 12.03
Turn on : 27.8107
Width : 3.637
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

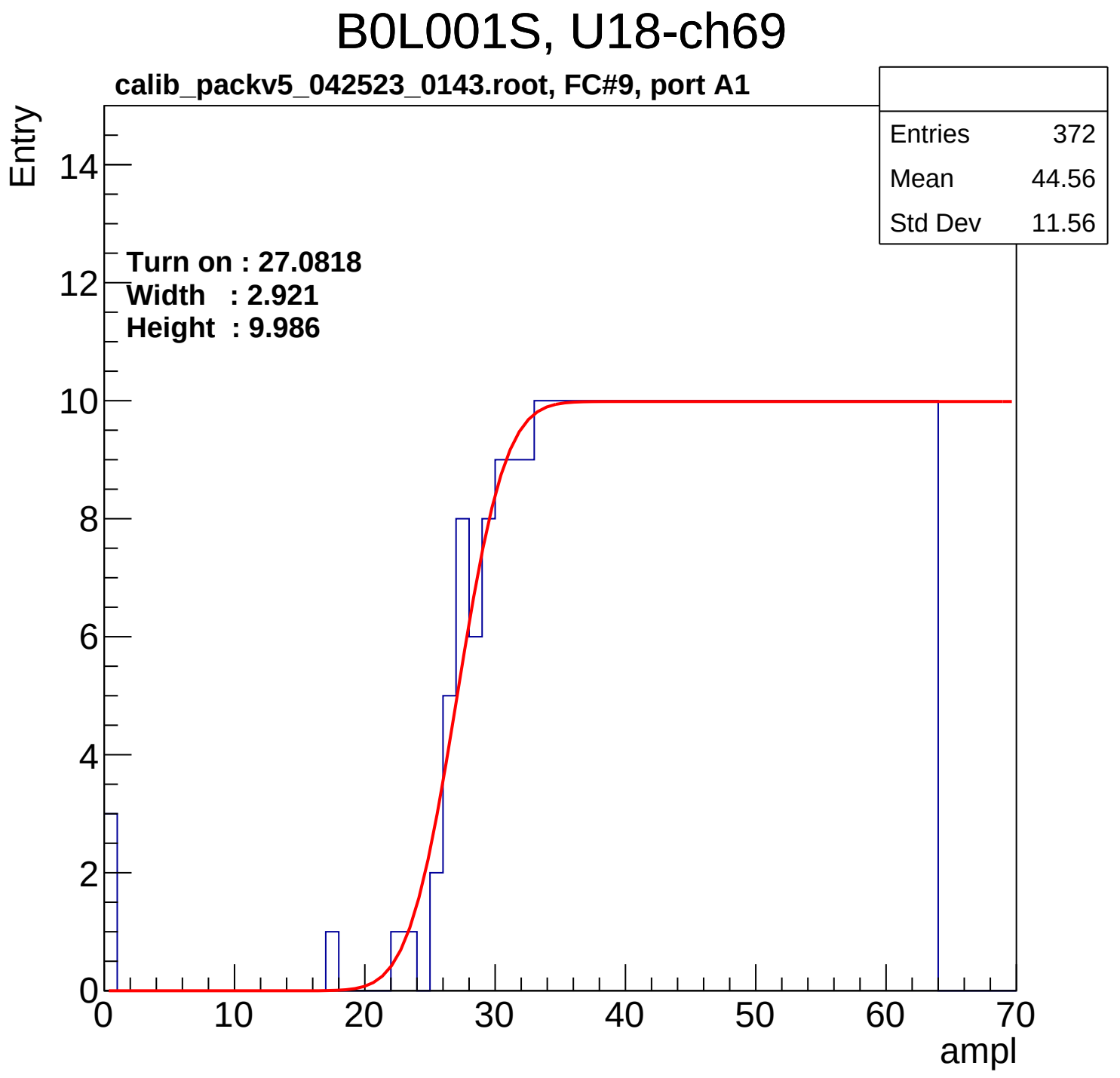

B0L001S, U18-ch64
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.86
Std Dev 11.24
Turn on : 27.5469
Width : 3.439
Height : 9.991
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

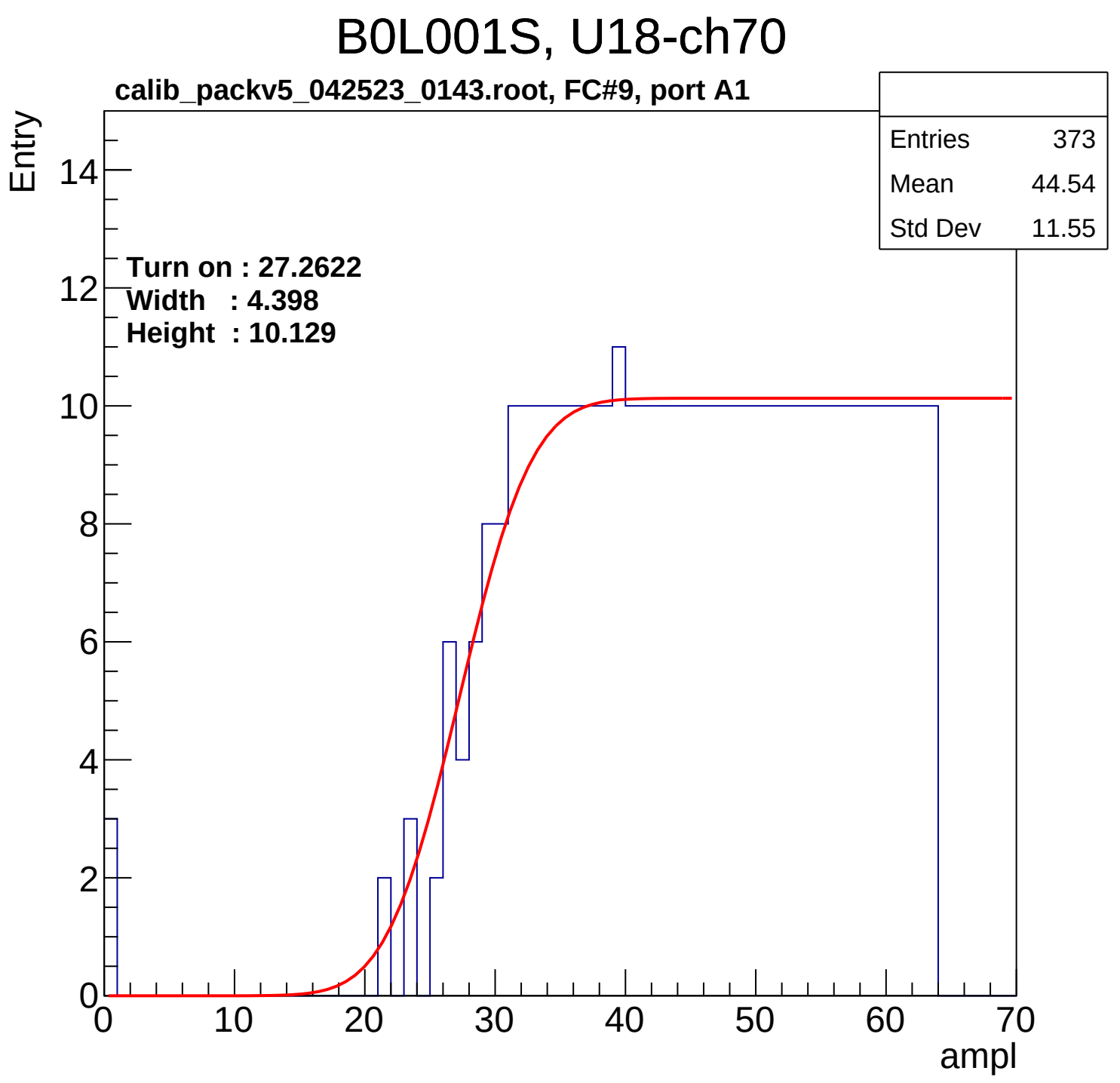

B0L001S, U18-ch65
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.92
Std Dev 11.35
Turn on : 28.3802
Width : 3.385
Height : 10.121
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

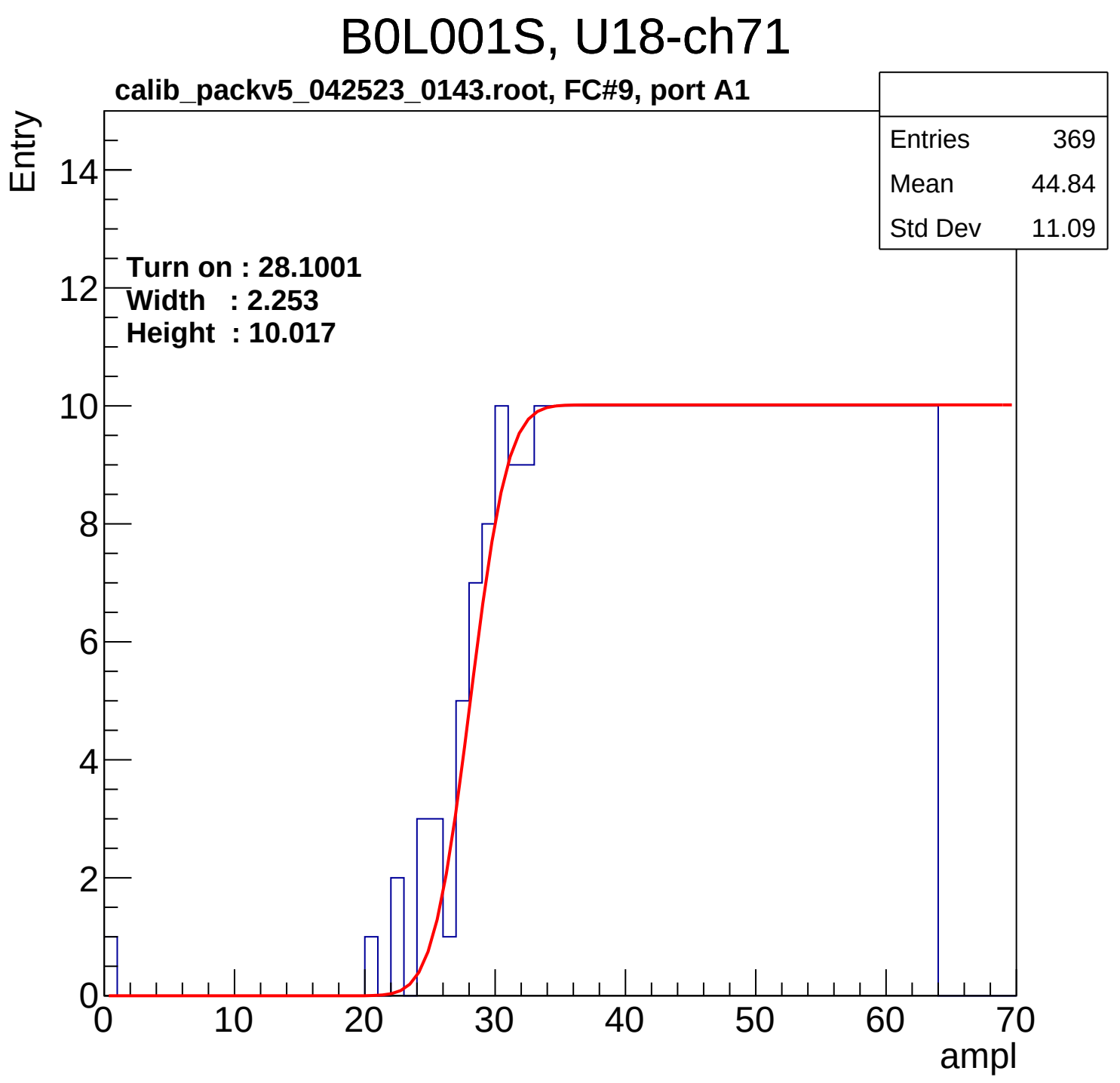

B0L001S, U18-ch66
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.72
Std Dev 10.79
Turn on : 29.7241
Width : 3.294
Height : 10.062
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

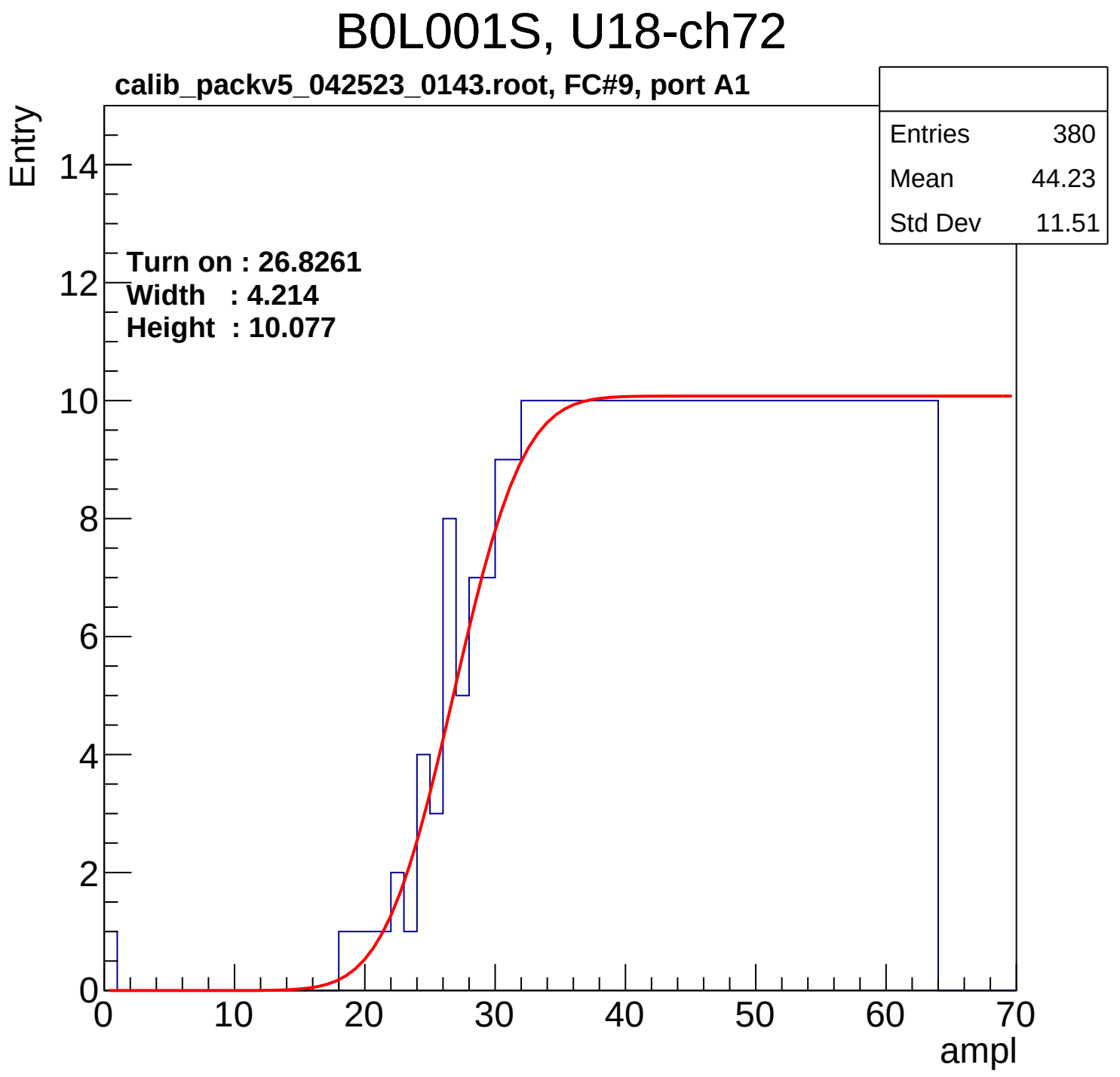

B0L001S, U18-ch67
calib_packv5_042523_0143.root, FC#9, port A1
Entries 380
Mean 44.01
Std Dev 12.21
Turn on : 26.7570
Width : 3.428
Height : 10.065
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

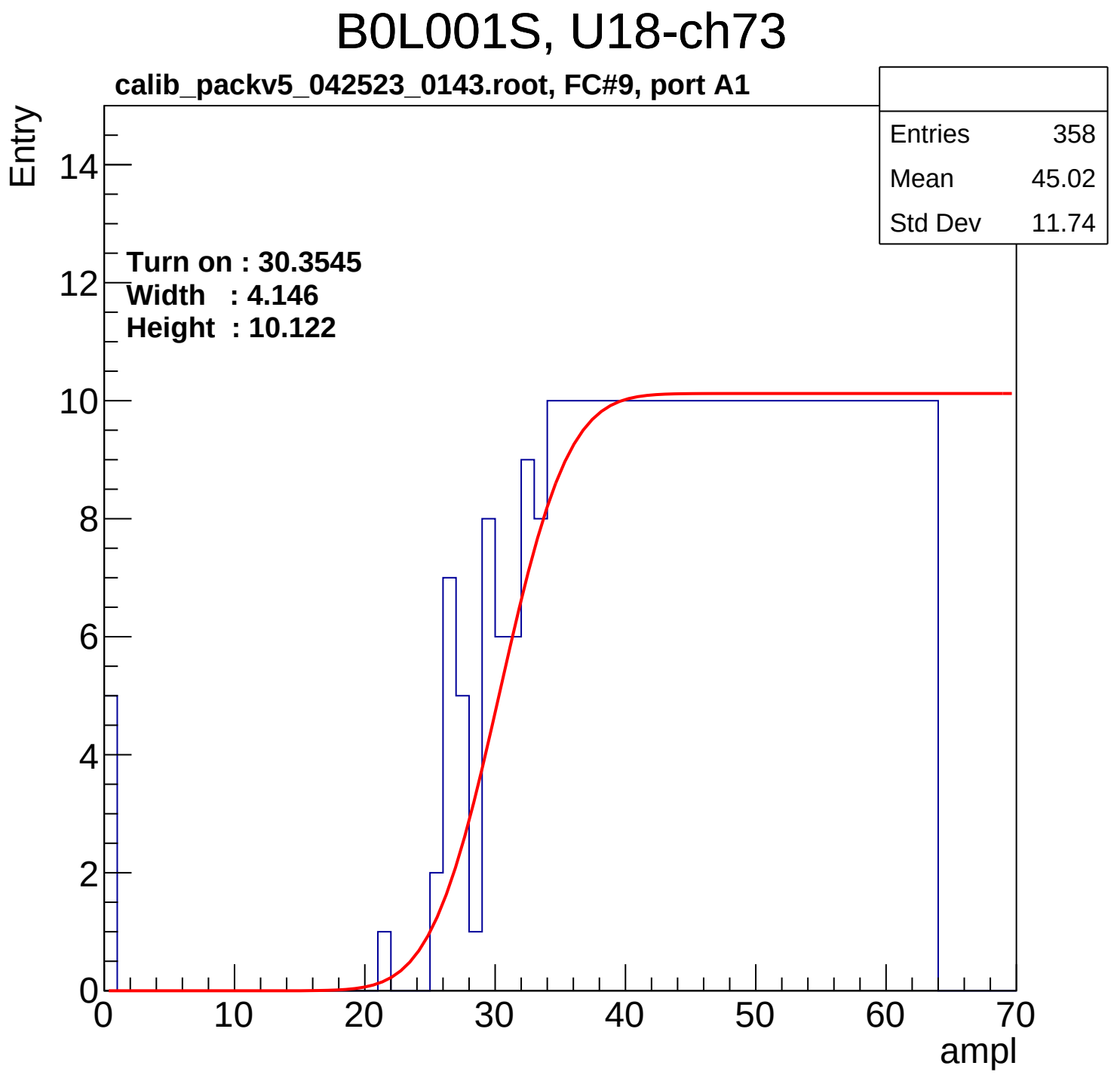

B0L001S, U18-ch68
calib_packv5_042523_0143.root, FC#9, port A1
Entries 349
Mean 45.67
Std Dev 11.01
Turn on : 29.5340
Width : 4.030
Height : 10.051
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

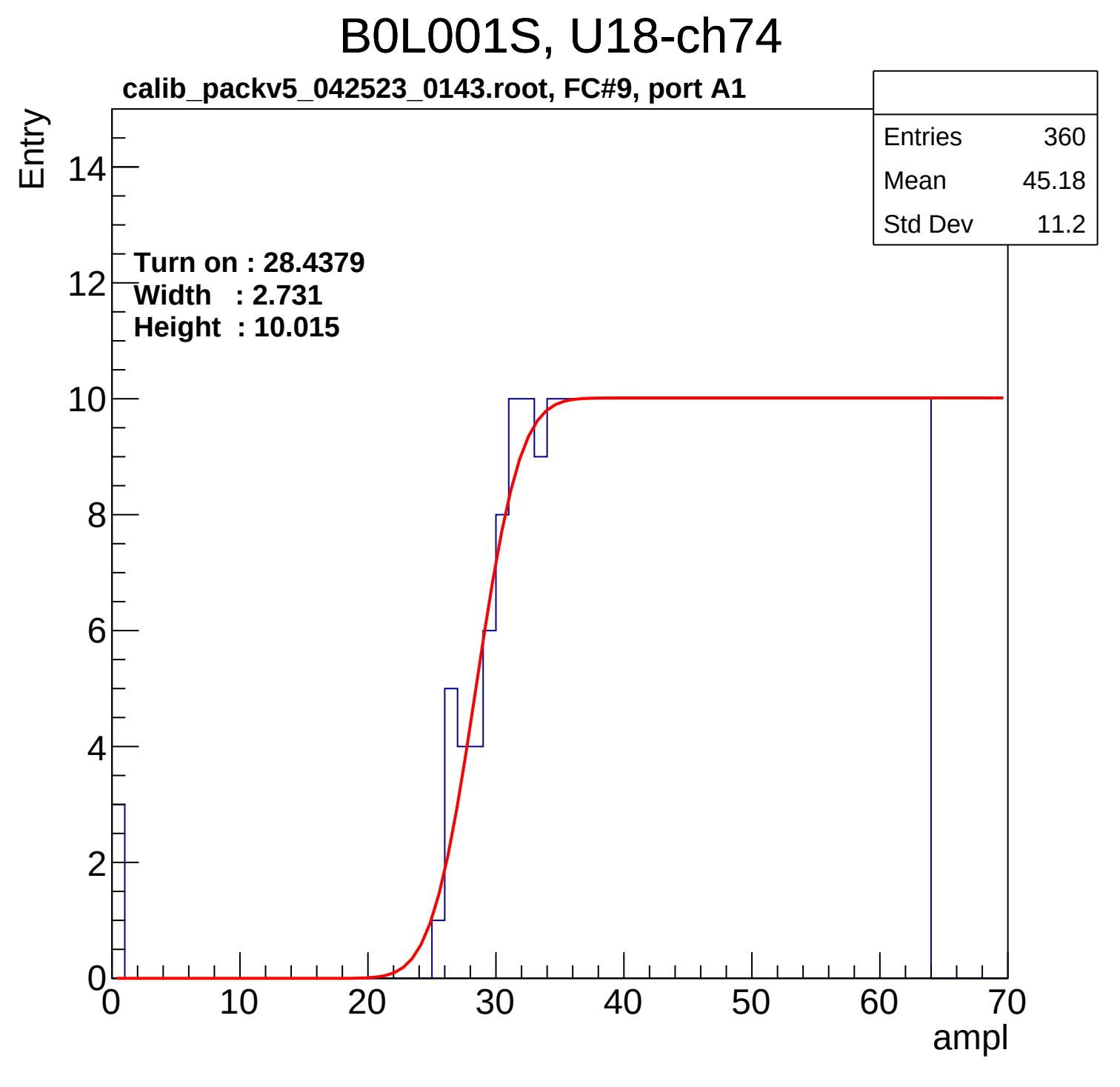

B0L001S, U18-ch69
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.56
Std Dev 11.56
Turn on : 27.0818
Width : 2.921
Height : 9.986
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

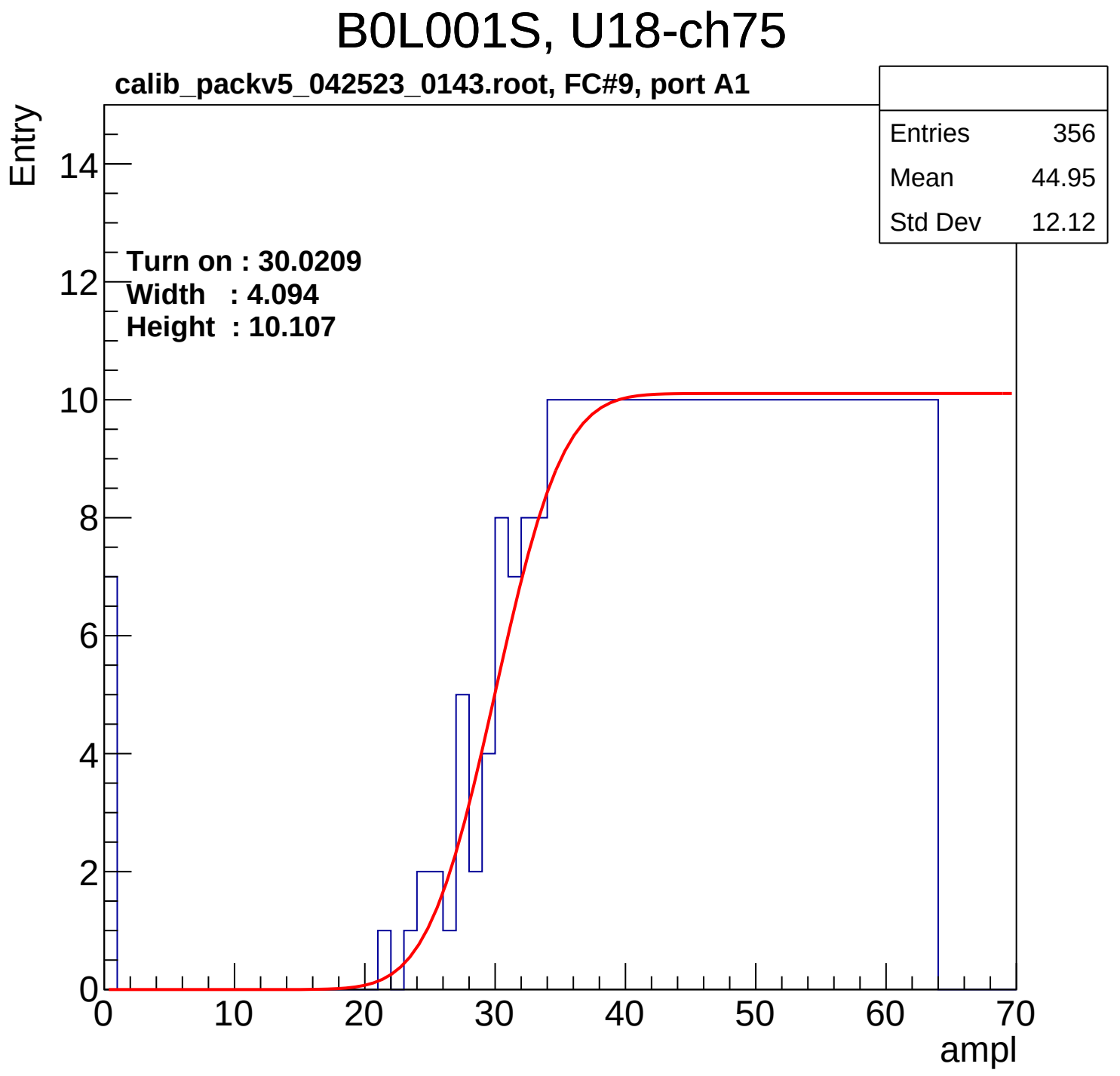

B0L001S, U18-ch70
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.54
Std Dev 11.55
Turn on : 27.2622
Width : 4.398
Height : 10.129
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

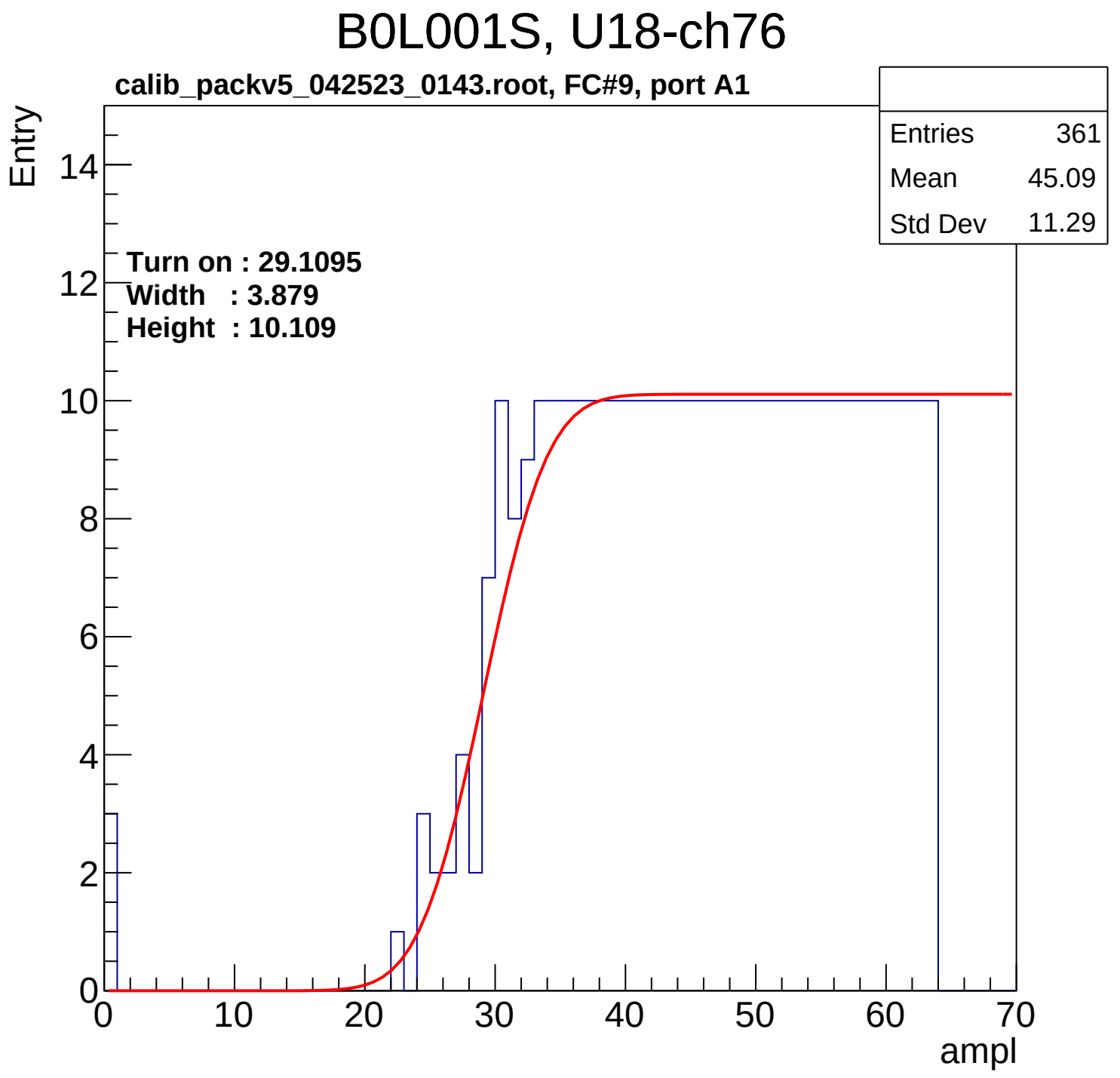

B0L001S, U18-ch71
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.84
Std Dev 11.09
Turn on : 28.1001
Width : 2.253
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

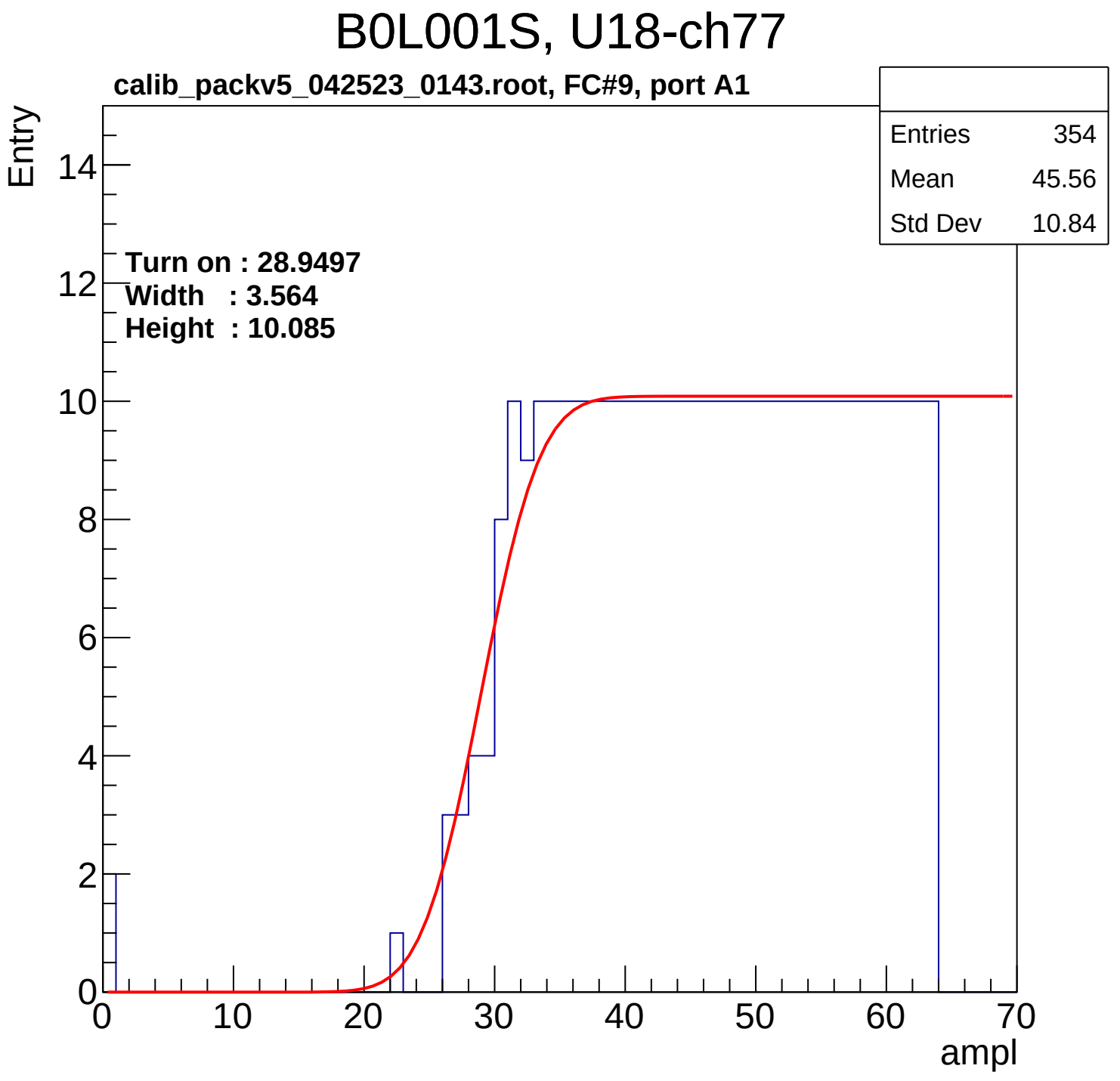

B0L001S, U18-ch72
calib_packv5_042523_0143.root, FC#9, port A1
Entries 380
Mean 44.23
Std Dev 11.51
Turn on : 26.8261
Width : 4.214
Height : 10.077
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

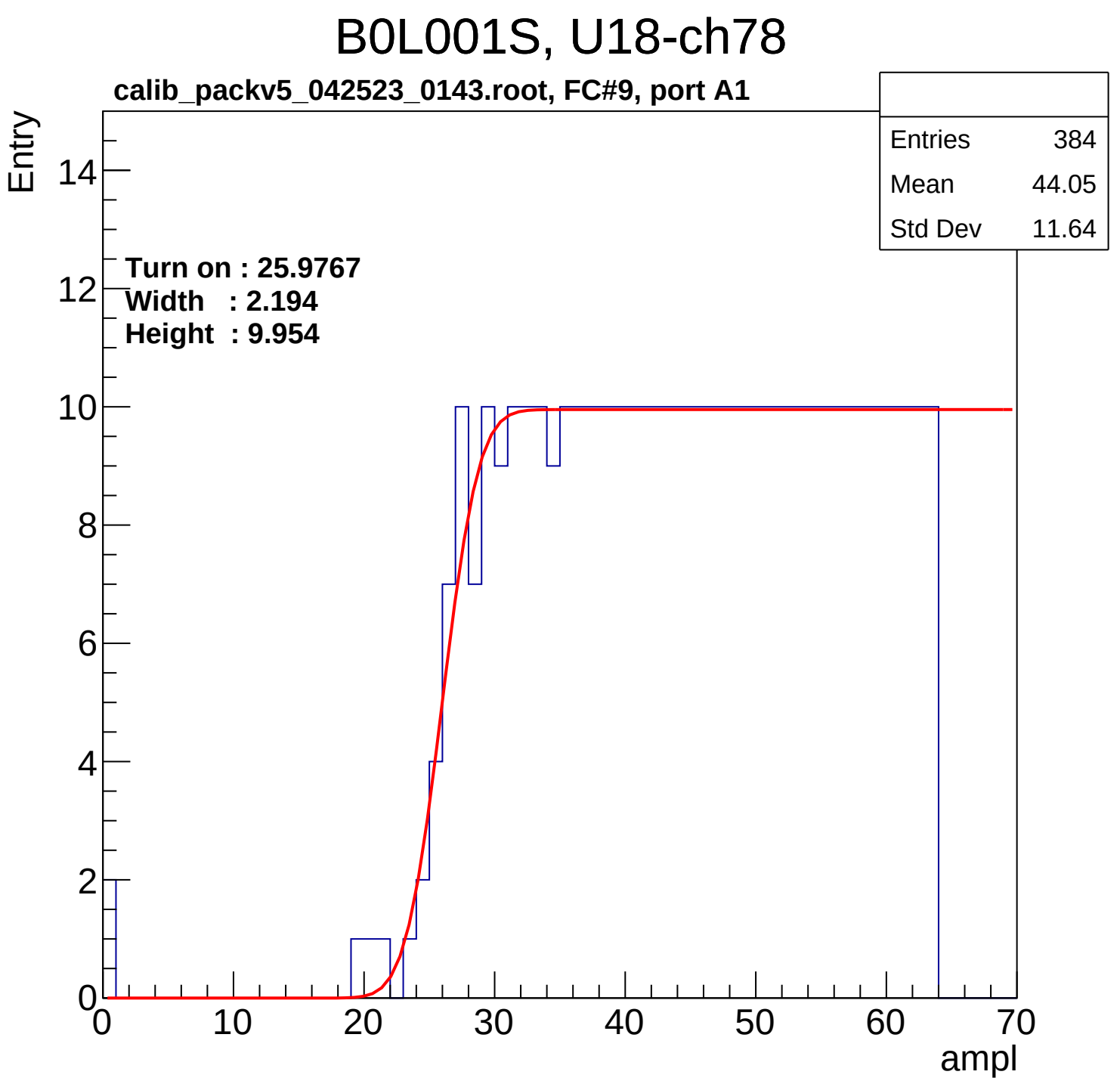

B0L001S, U18-ch73
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.02
Std Dev 11.74
Turn on : 30.3545
Width : 4.146
Height : 10.122
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

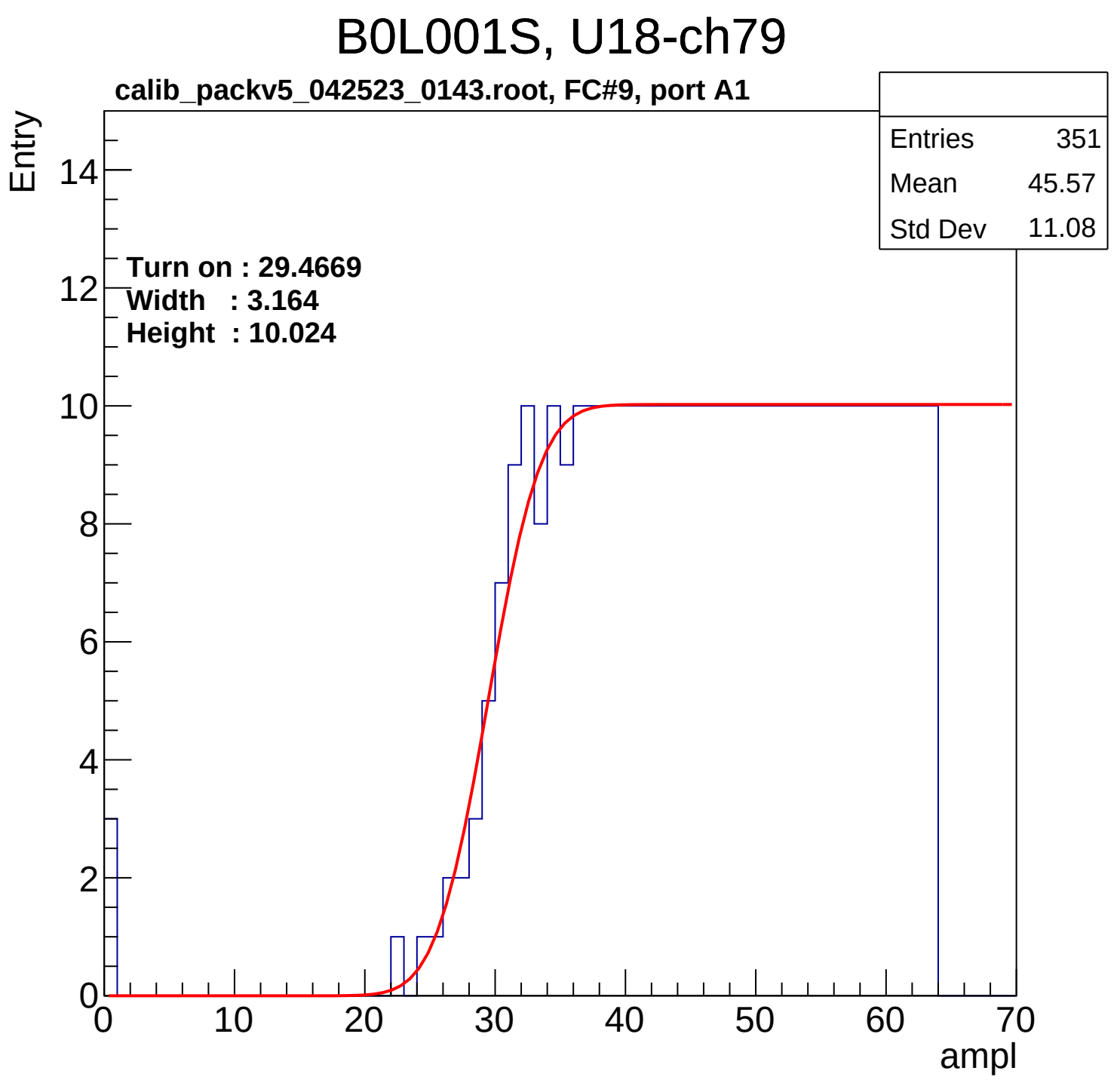

B0L001S, U18-ch74
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.18
Std Dev 11.2
Turn on : 28.4379
Width : 2.731
Height : 10.015
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

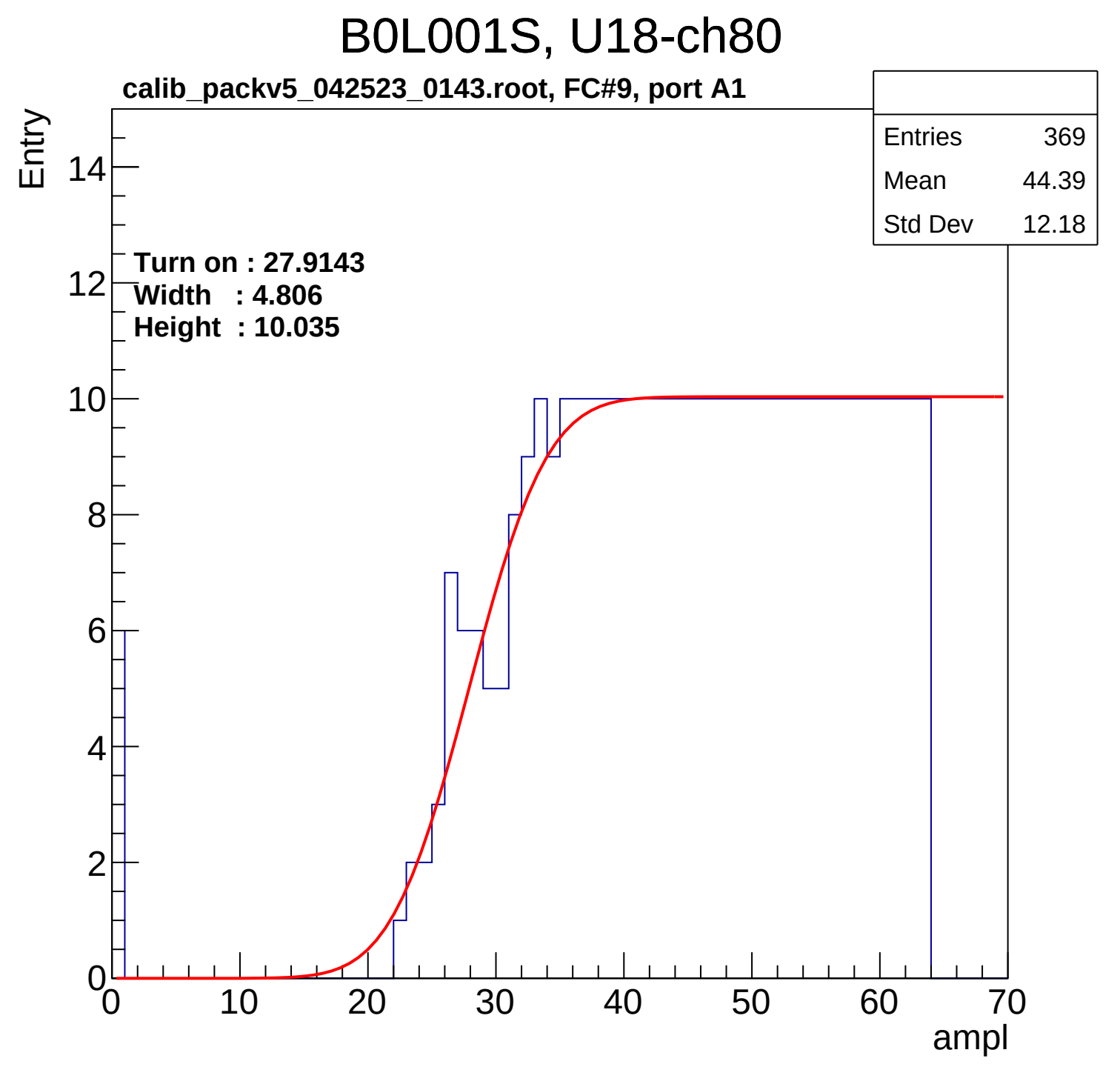

B0L001S, U18-ch75
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 44.95
Std Dev 12.12
Turn on : 30.0209
Width : 4.094
Height : 10.107
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

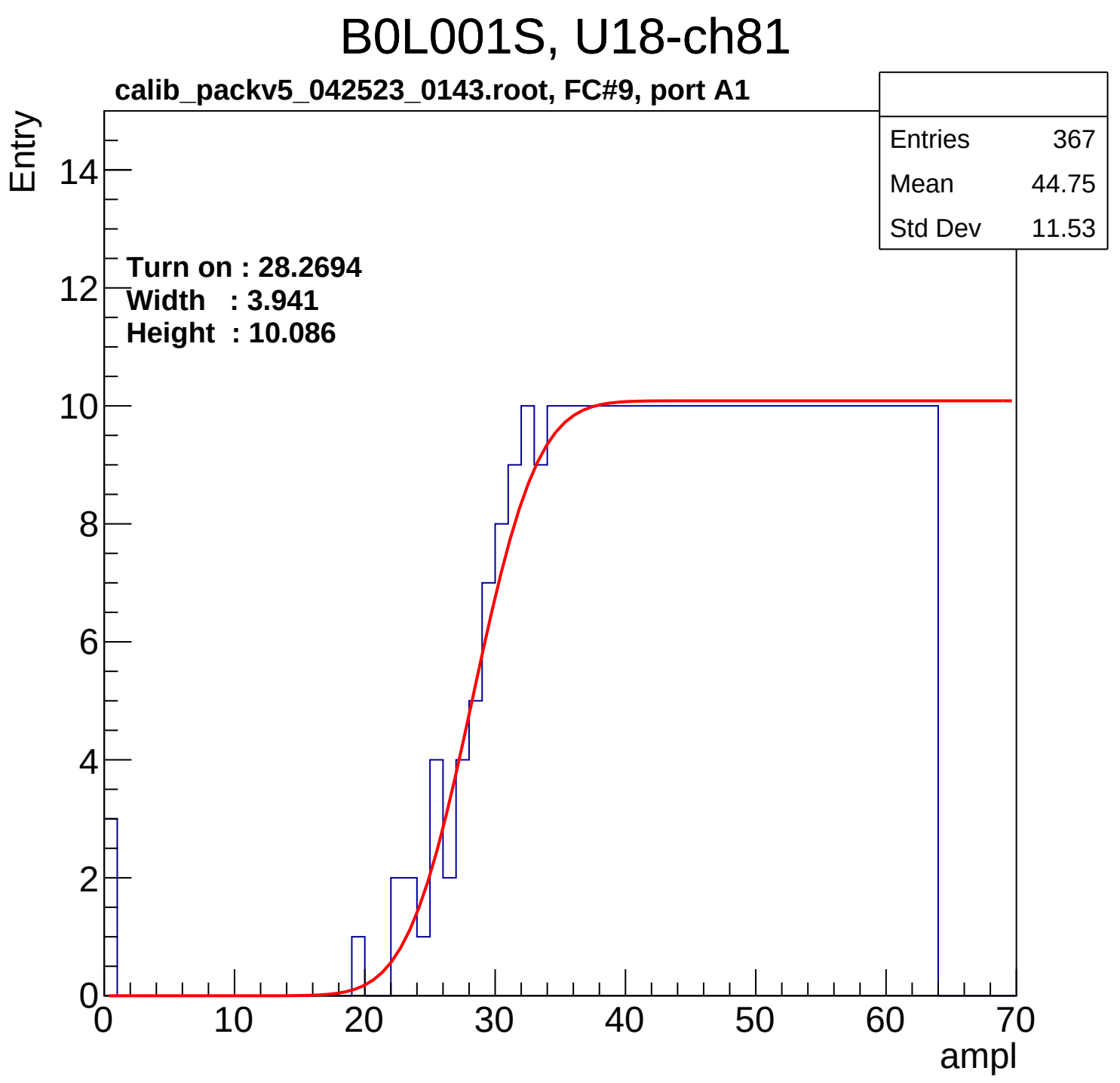

B0L001S, U18-ch76
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.09
Std Dev 11.29
Turn on : 29.1095
Width : 3.879
Height : 10.109
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

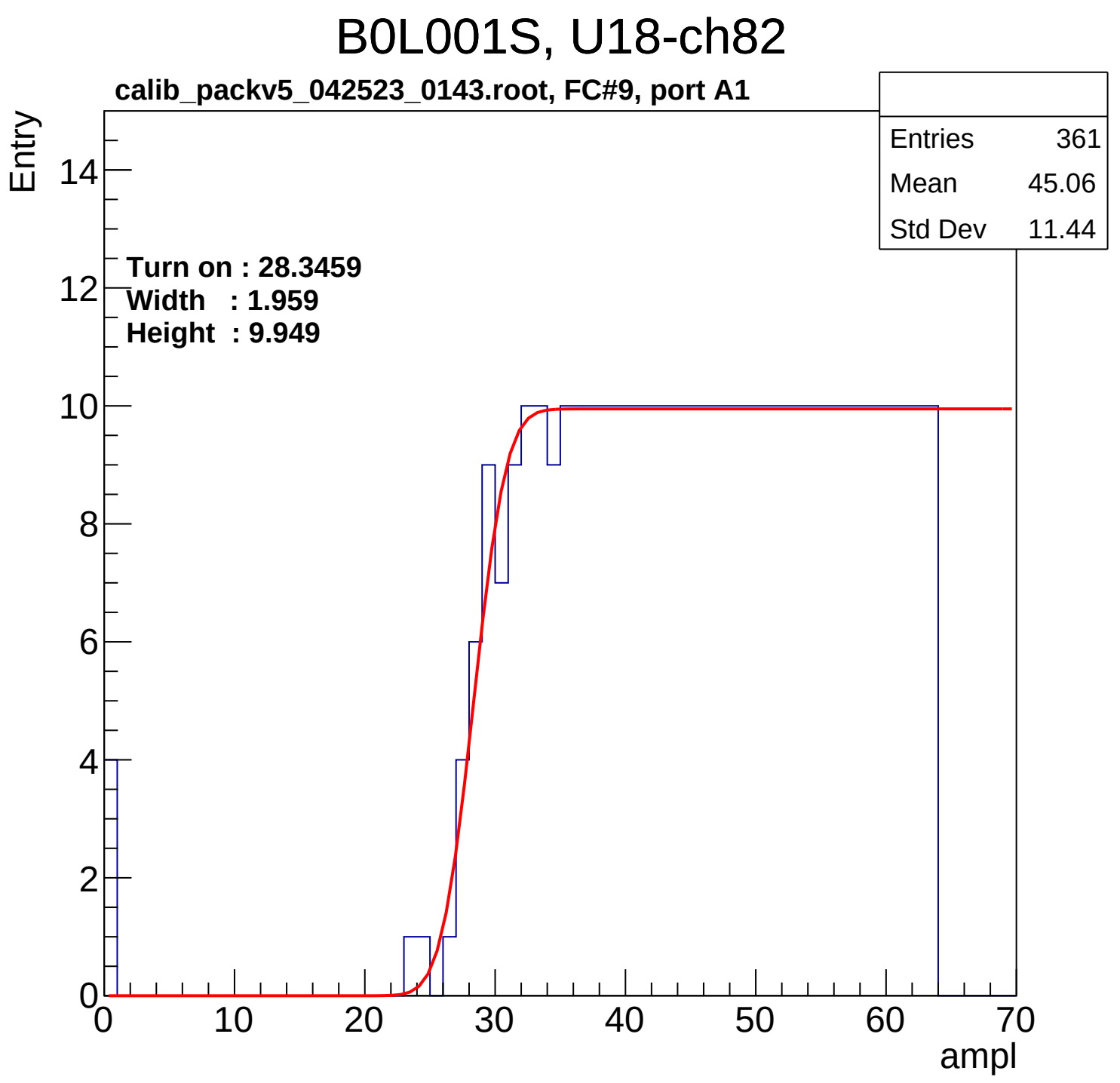

B0L001S, U18-ch77
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.56
Std Dev 10.84
Turn on : 28.9497
Width : 3.564
Height : 10.085
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

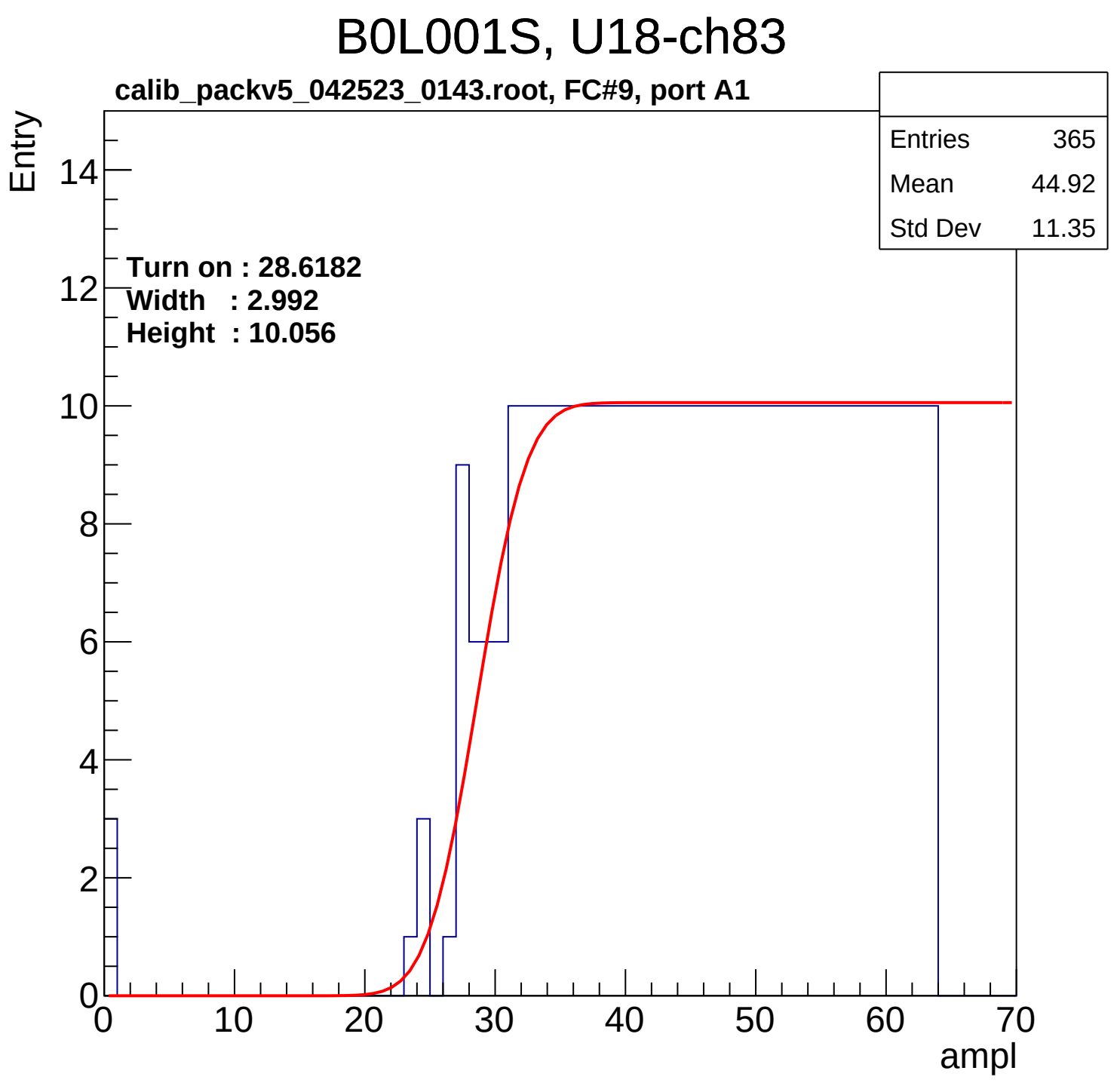

B0L001S, U18-ch78
calib_packv5_042523_0143.root, FC#9, port A1
Entries 384
Mean 44.05
Std Dev 11.64
Turn on : 25.9767
Width : 2.194
Height : 9.954
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

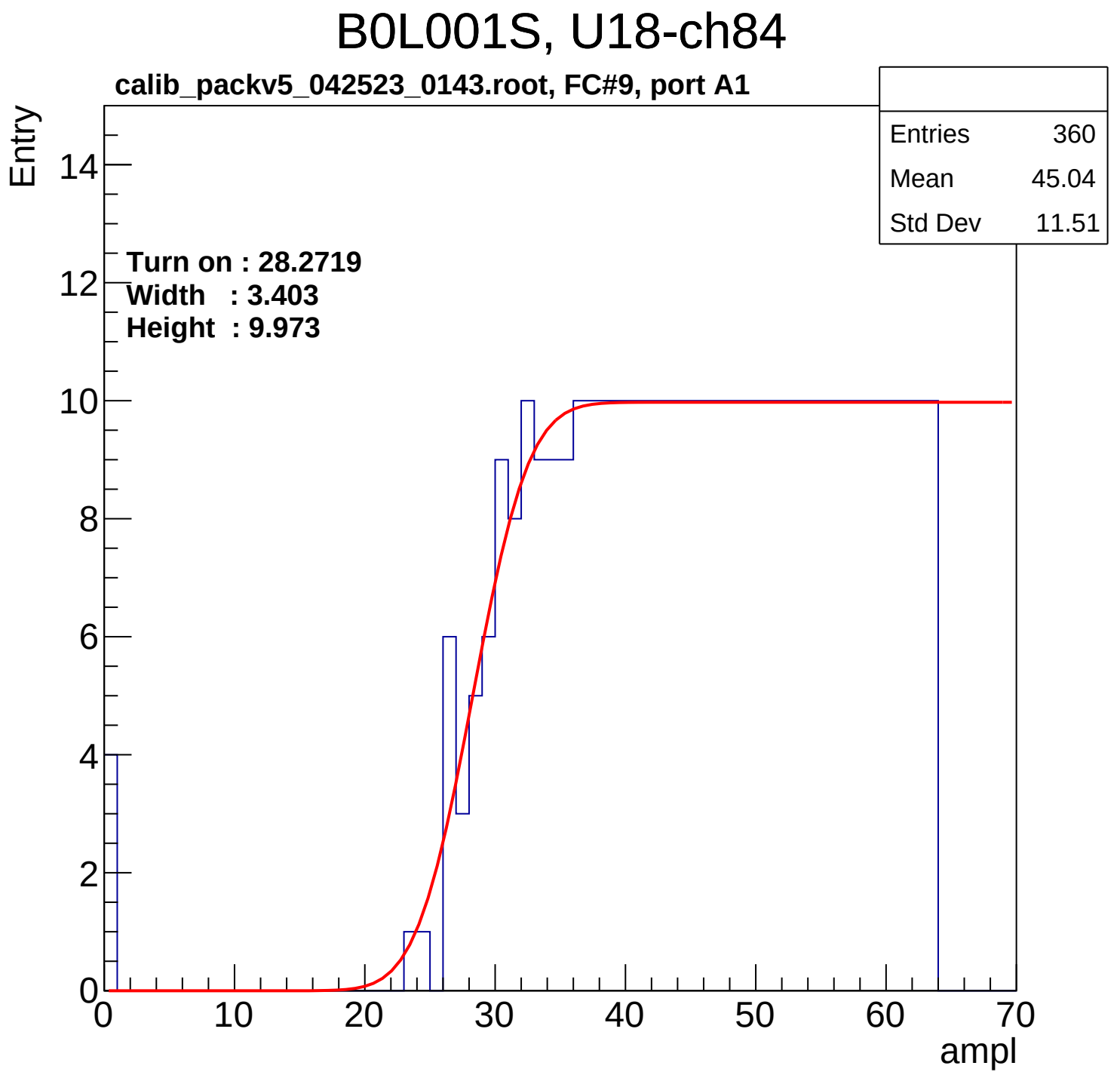

B0L001S, U18-ch79
calib_packv5_042523_0143.root, FC#9, port A1
Entries 351
Mean 45.57
Std Dev 11.08
Turn on : 29.4669
Width : 3.164
Height : 10.024
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

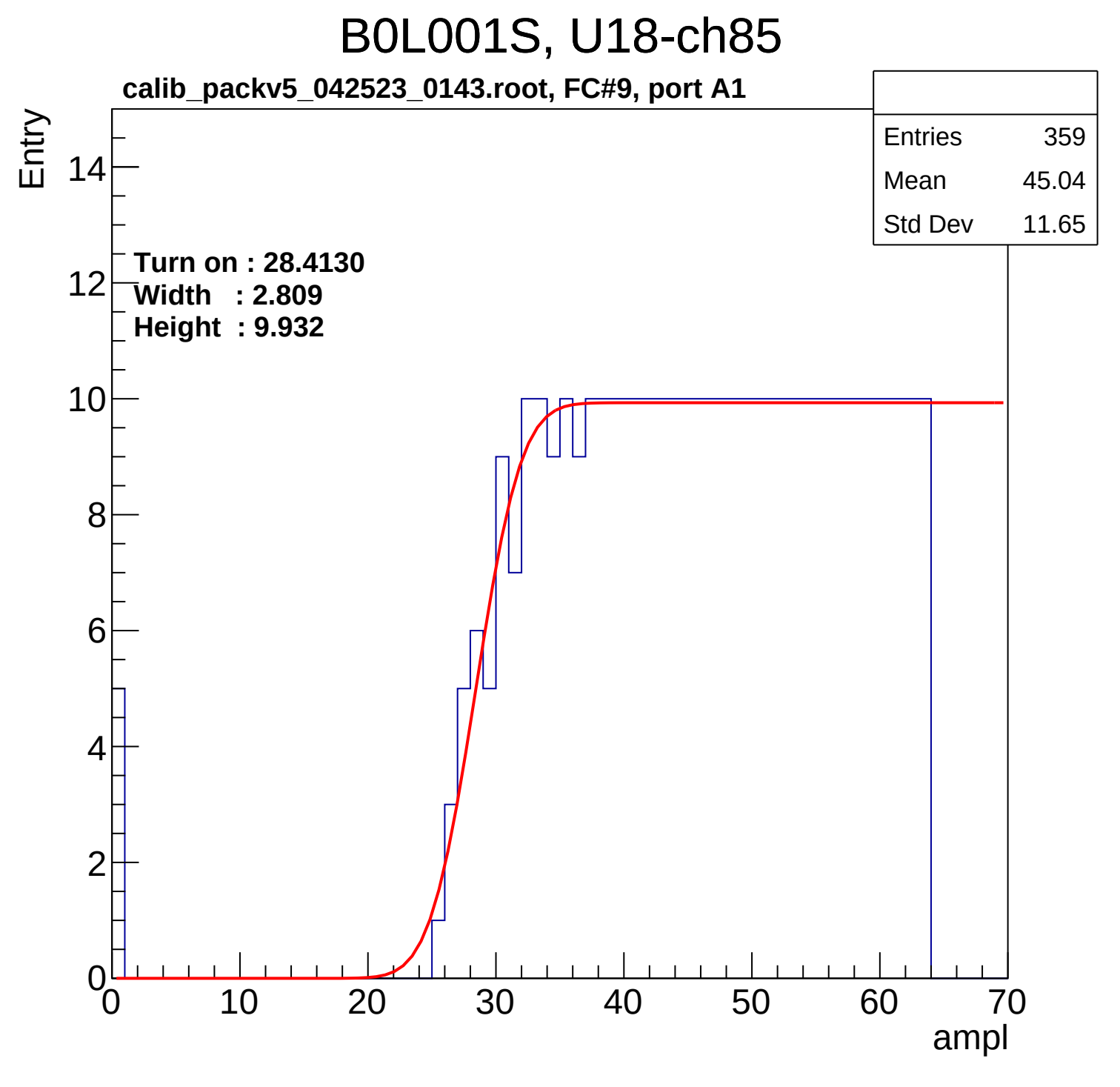

B0L001S, U18-ch80
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.39
Std Dev 12.18
Turn on : 27.9143
Width : 4.806
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

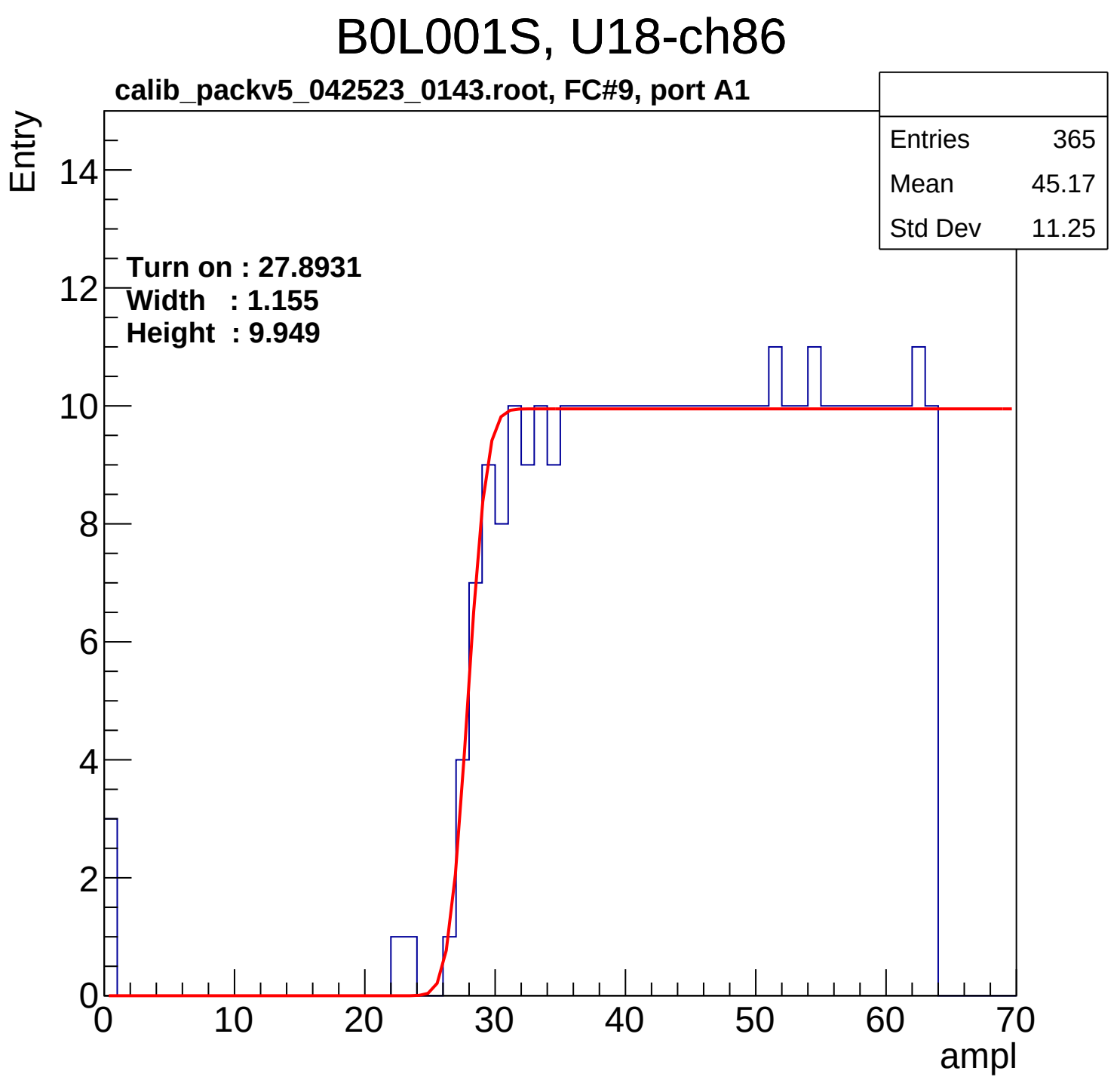

B0L001S, U18-ch81
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.75
Std Dev 11.53
Turn on : 28.2694
Width : 3.941
Height : 10.086
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

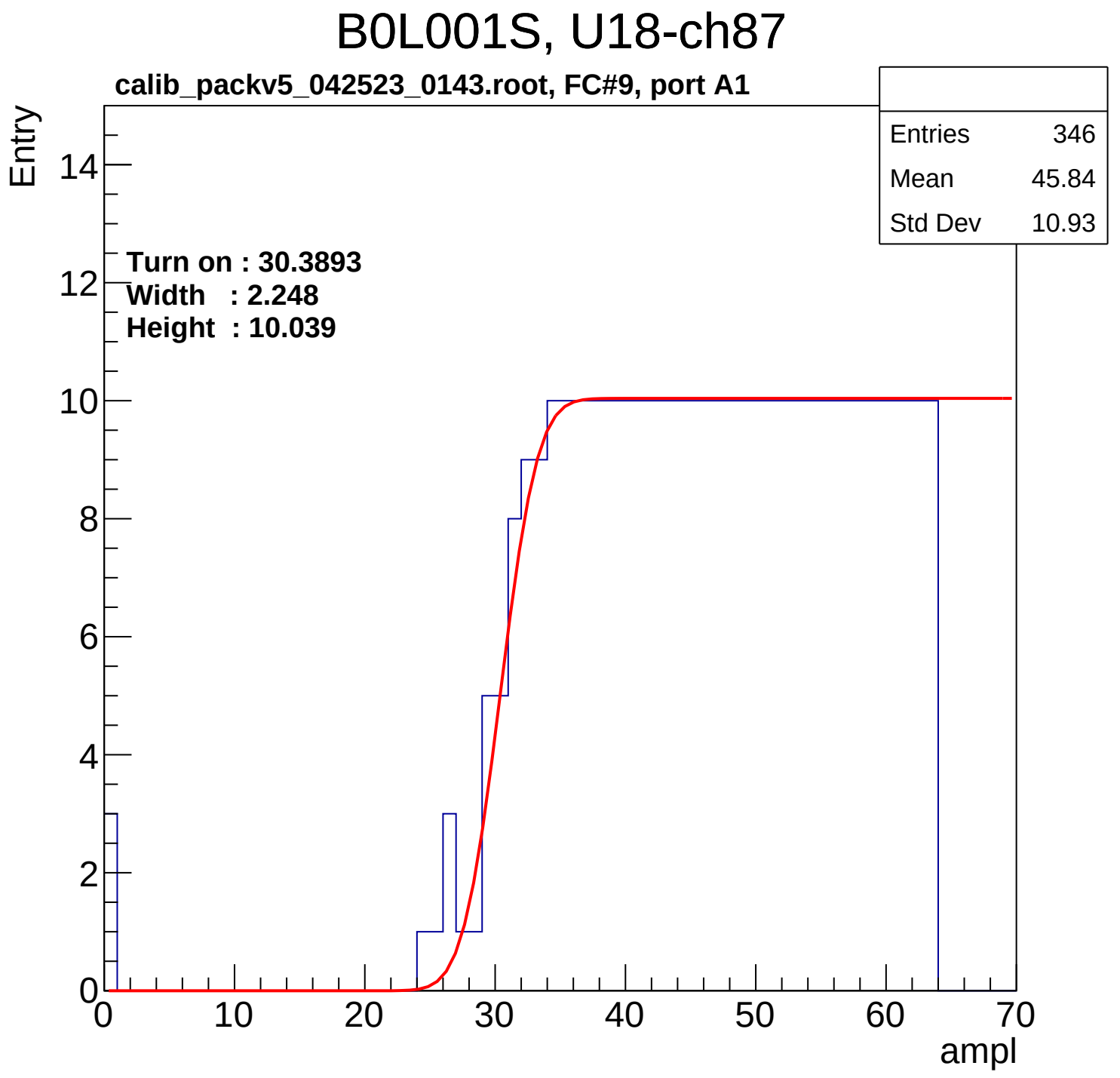

B0L001S, U18-ch82
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.06
Std Dev 11.44
Turn on : 28.3459
Width : 1.959
Height : 9.949
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

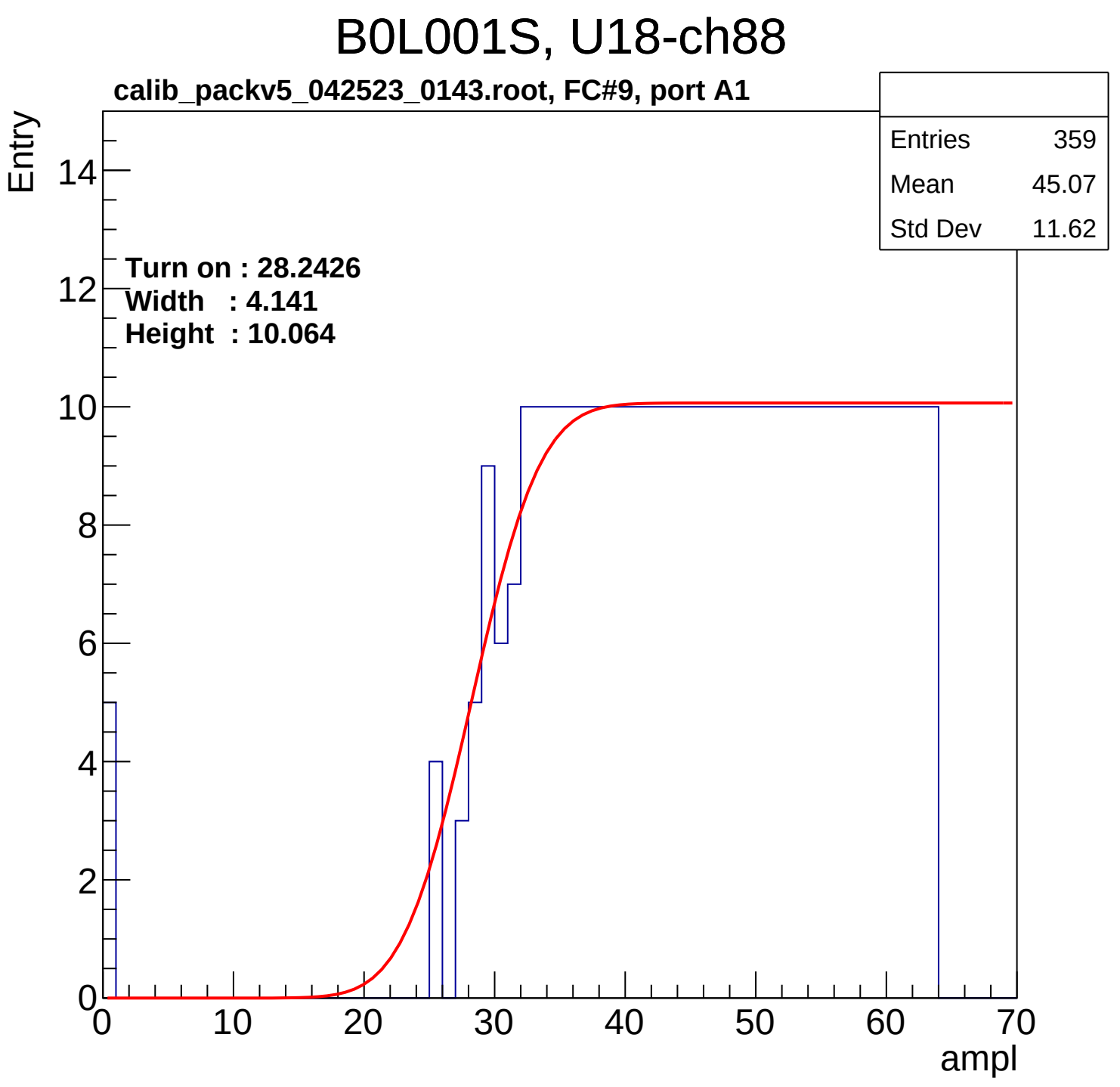

B0L001S, U18-ch83
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.92
Std Dev 11.35
Turn on : 28.6182
Width : 2.992
Height : 10.056
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

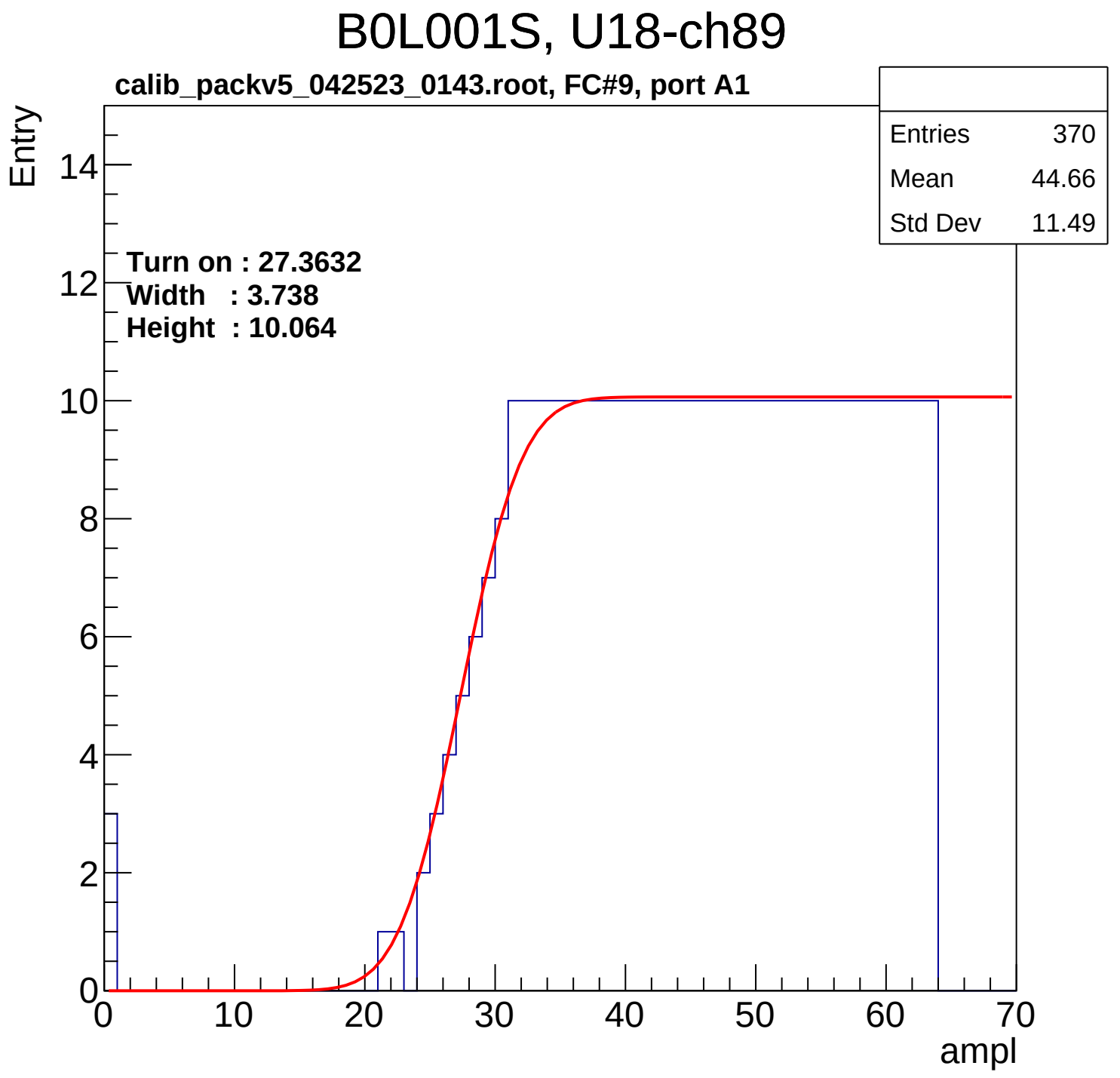

B0L001S, U18-ch84
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.04
Std Dev 11.51
Turn on : 28.2719
Width : 3.403
Height : 9.973
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

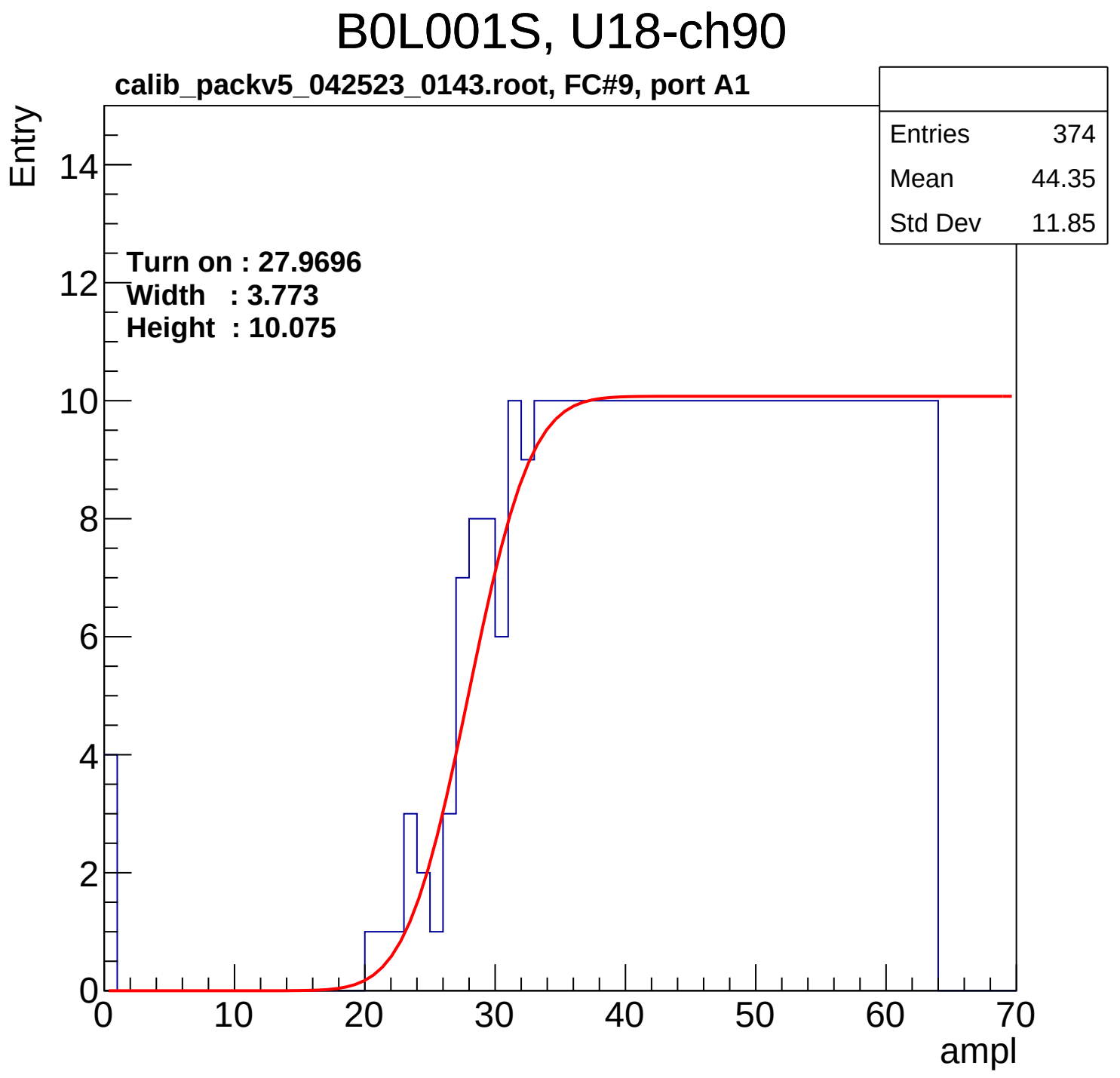

B0L001S, U18-ch85
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.04
Std Dev 11.65
Turn on : 28.4130
Width : 2.809
Height : 9.932
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

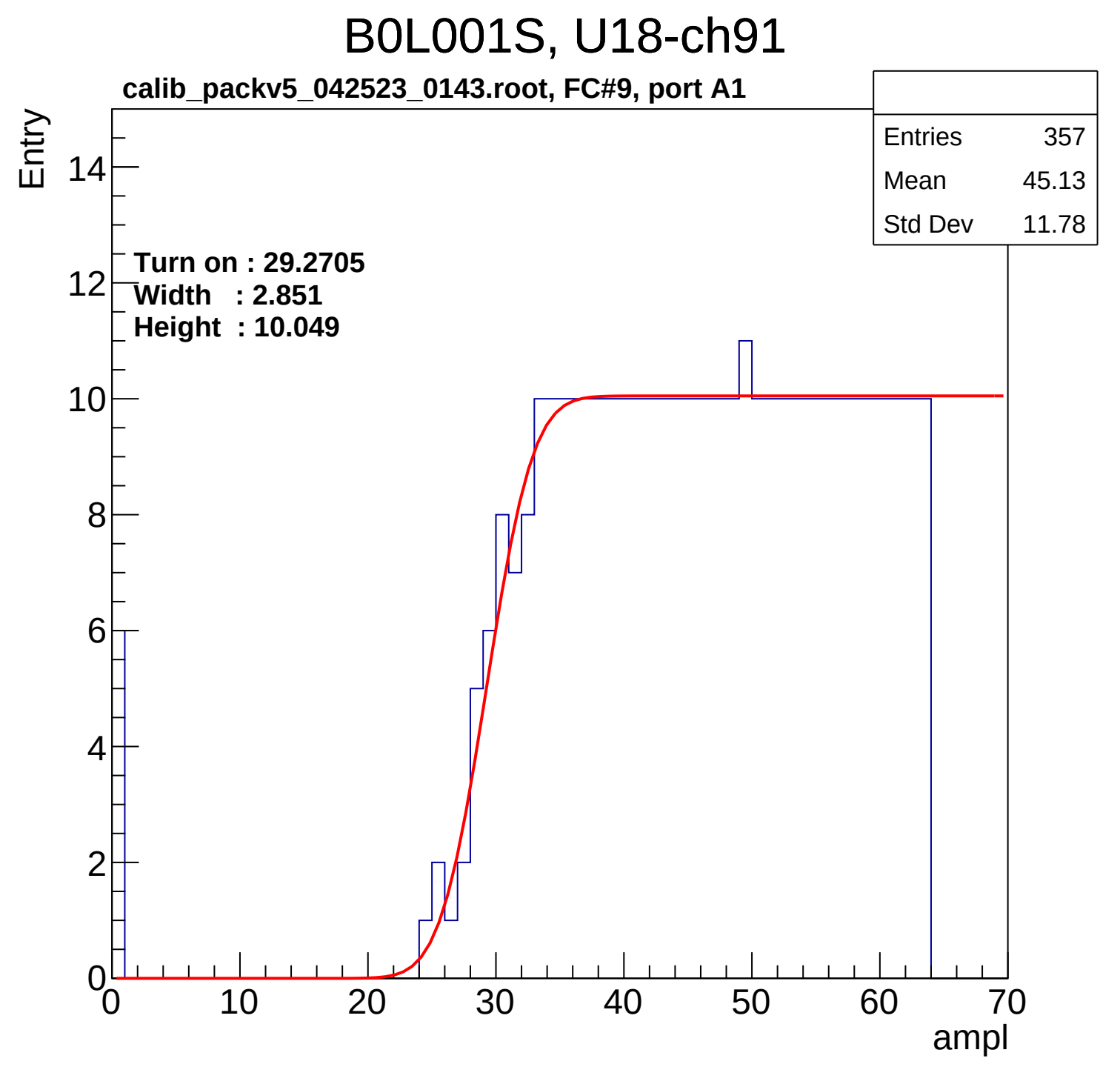

B0L001S, U18-ch86
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 45.17
Std Dev 11.25
Turn on : 27.8931
Width : 1.155
Height : 9.949
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

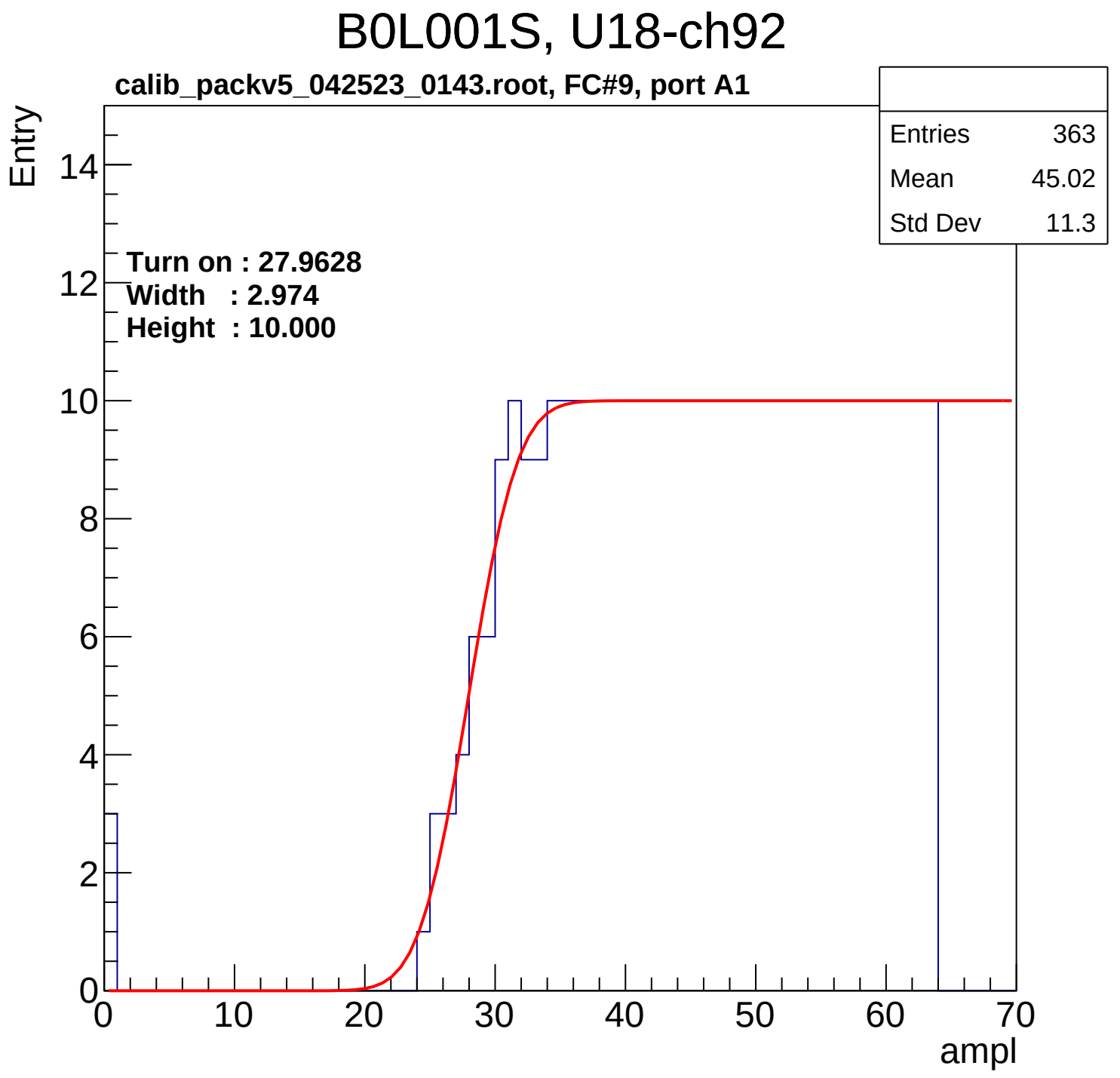

B0L001S, U18-ch87
calib_packv5_042523_0143.root, FC#9, port A1
Entries 346
Mean 45.84
Std Dev 10.93
Turn on : 30.3893
Width : 2.248
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

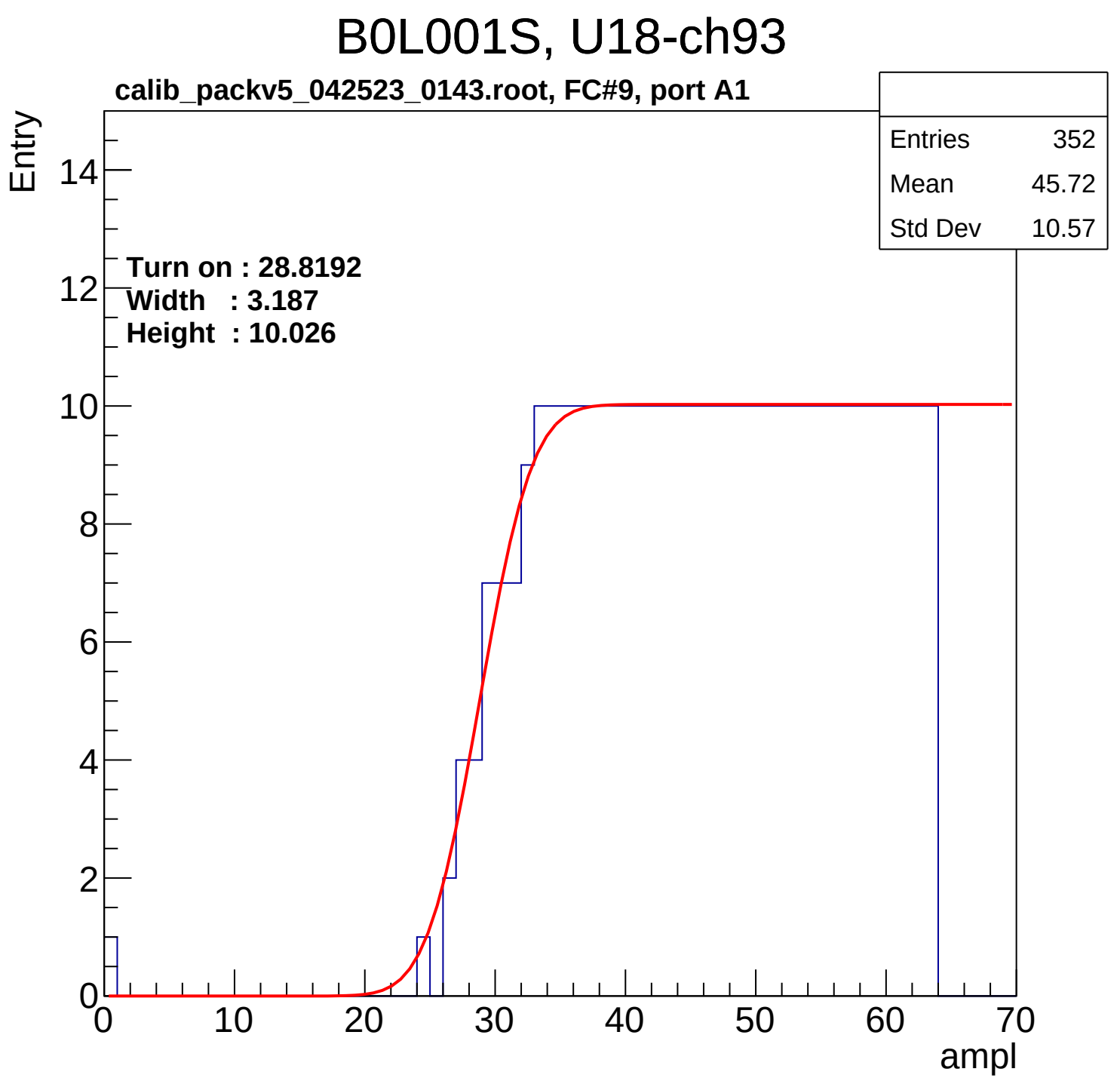

B0L001S, U18-ch88
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.07
Std Dev 11.62
Turn on : 28.2426
Width : 4.141
Height : 10.064
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

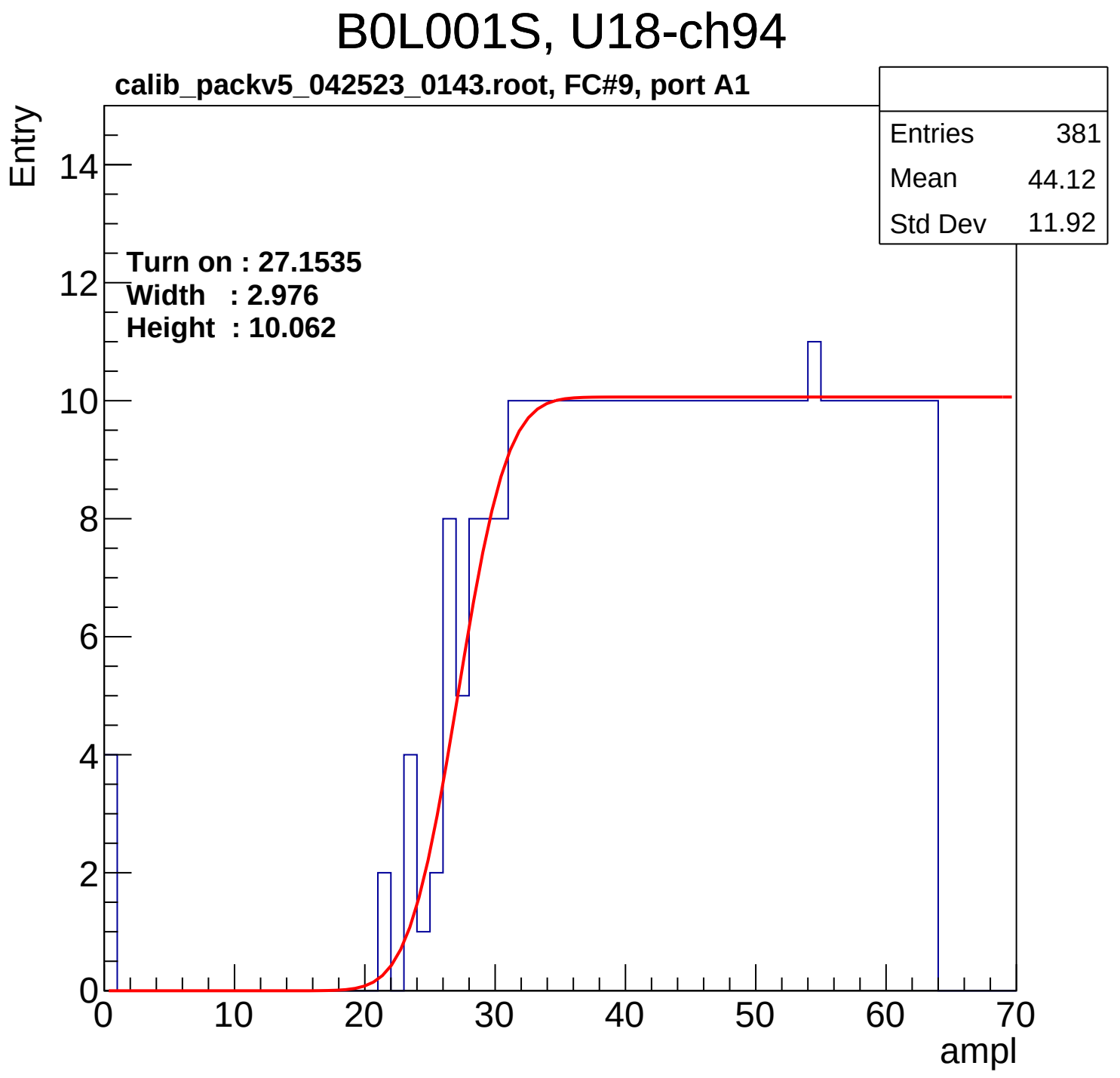

B0L001S, U18-ch89
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.66
Std Dev 11.49
Turn on : 27.3632
Width : 3.738
Height : 10.064
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

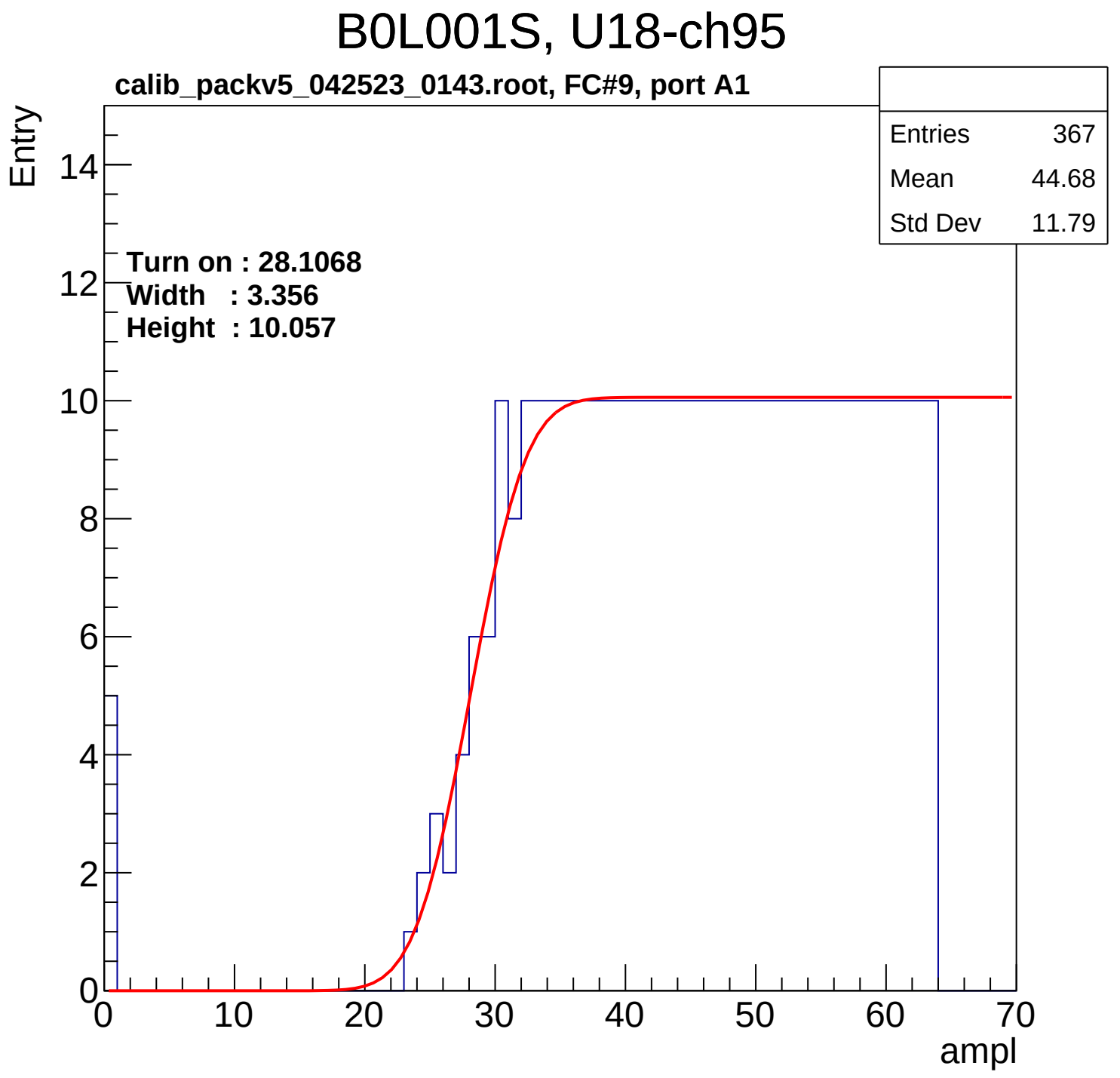

B0L001S, U18-ch90
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.35
Std Dev 11.85
Turn on : 27.9696
Width : 3.773
Height : 10.075
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

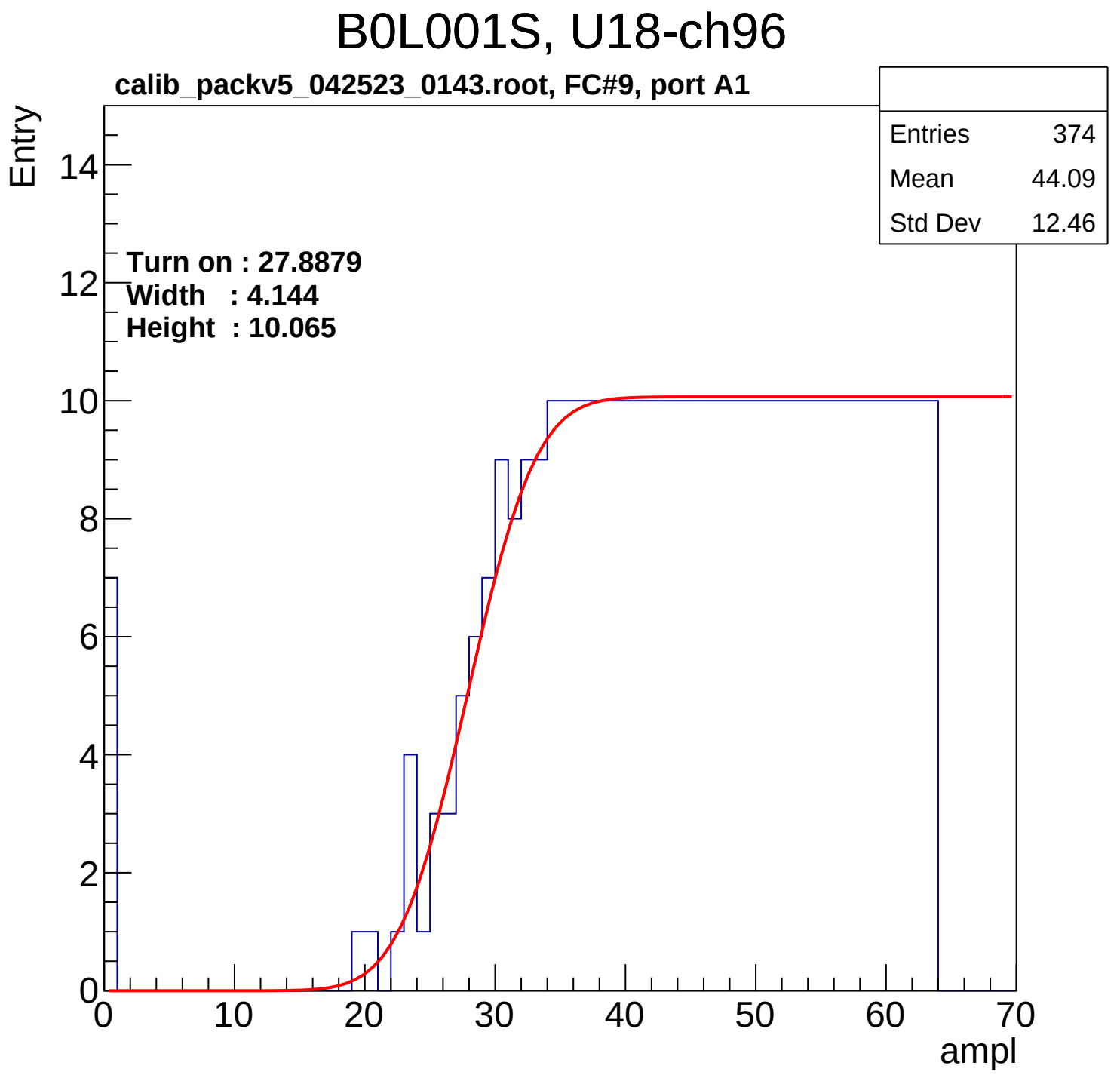

B0L001S, U18-ch91
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.13
Std Dev 11.78
Turn on : 29.2705
Width : 2.851
Height : 10.049
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

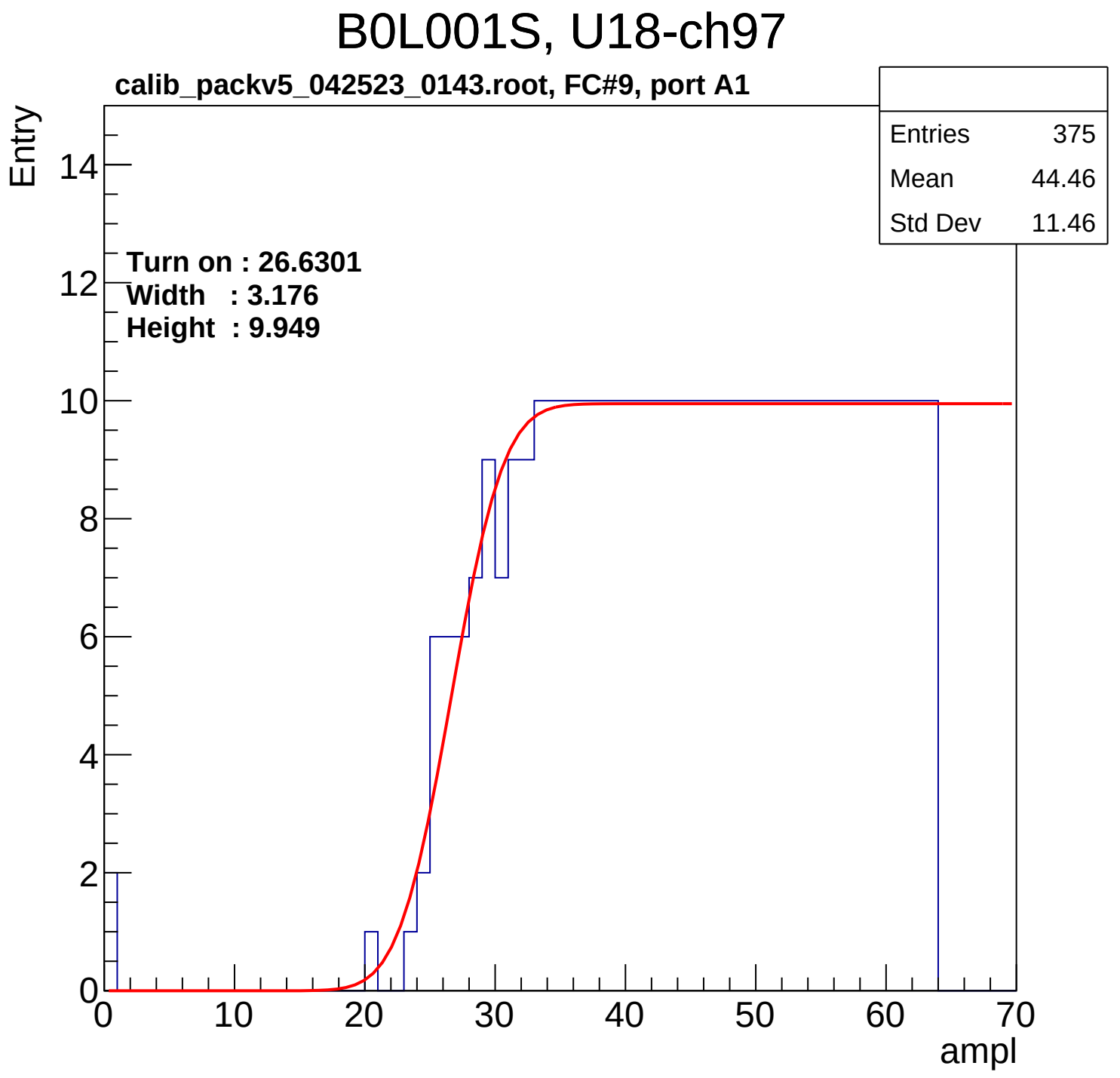

B0L001S, U18-ch92
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.02
Std Dev 11.3
Turn on : 27.9628
Width : 2.974
Height : 10.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

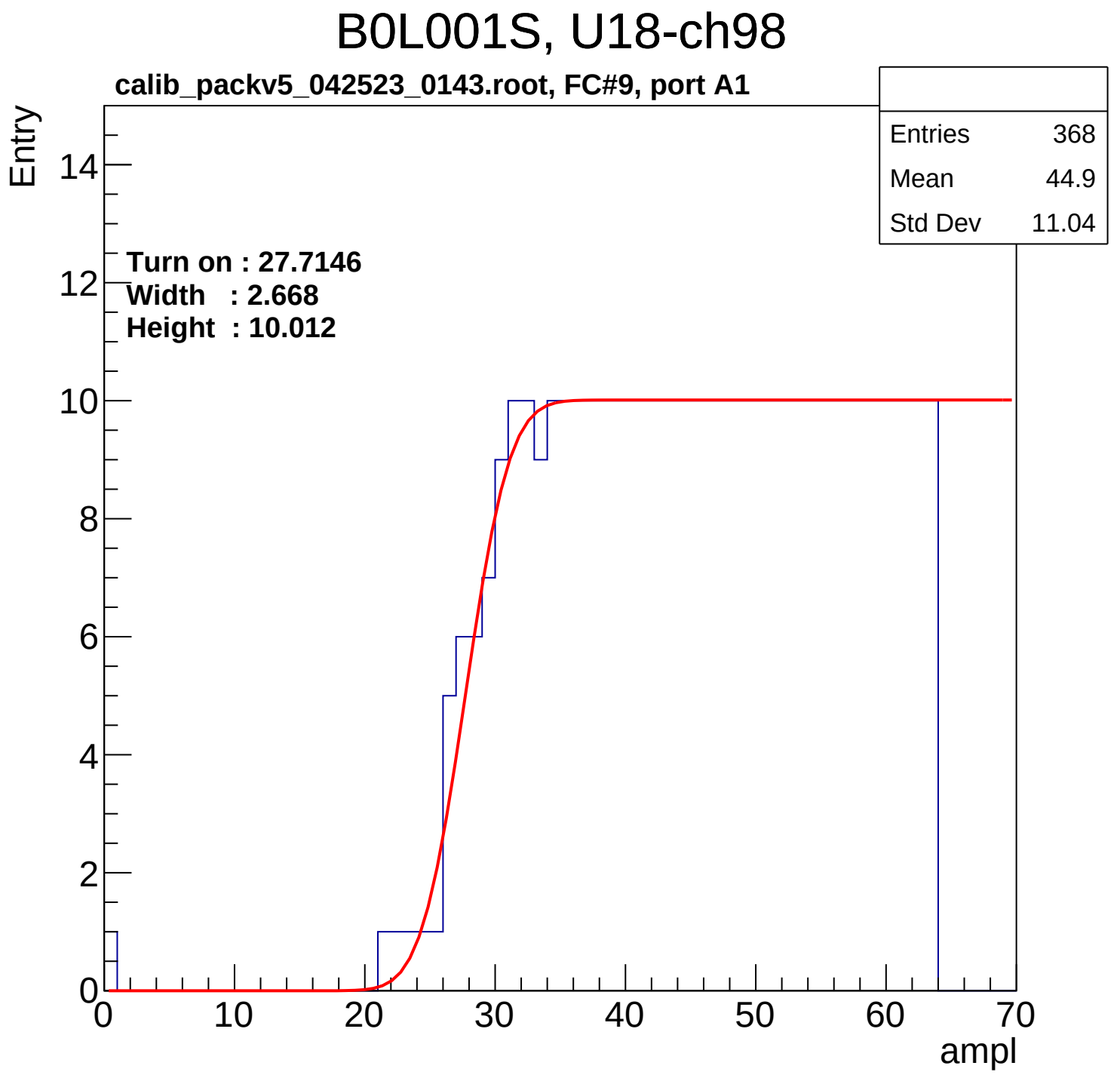

B0L001S, U18-ch93
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.72
Std Dev 10.57
Turn on : 28.8192
Width : 3.187
Height : 10.026
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

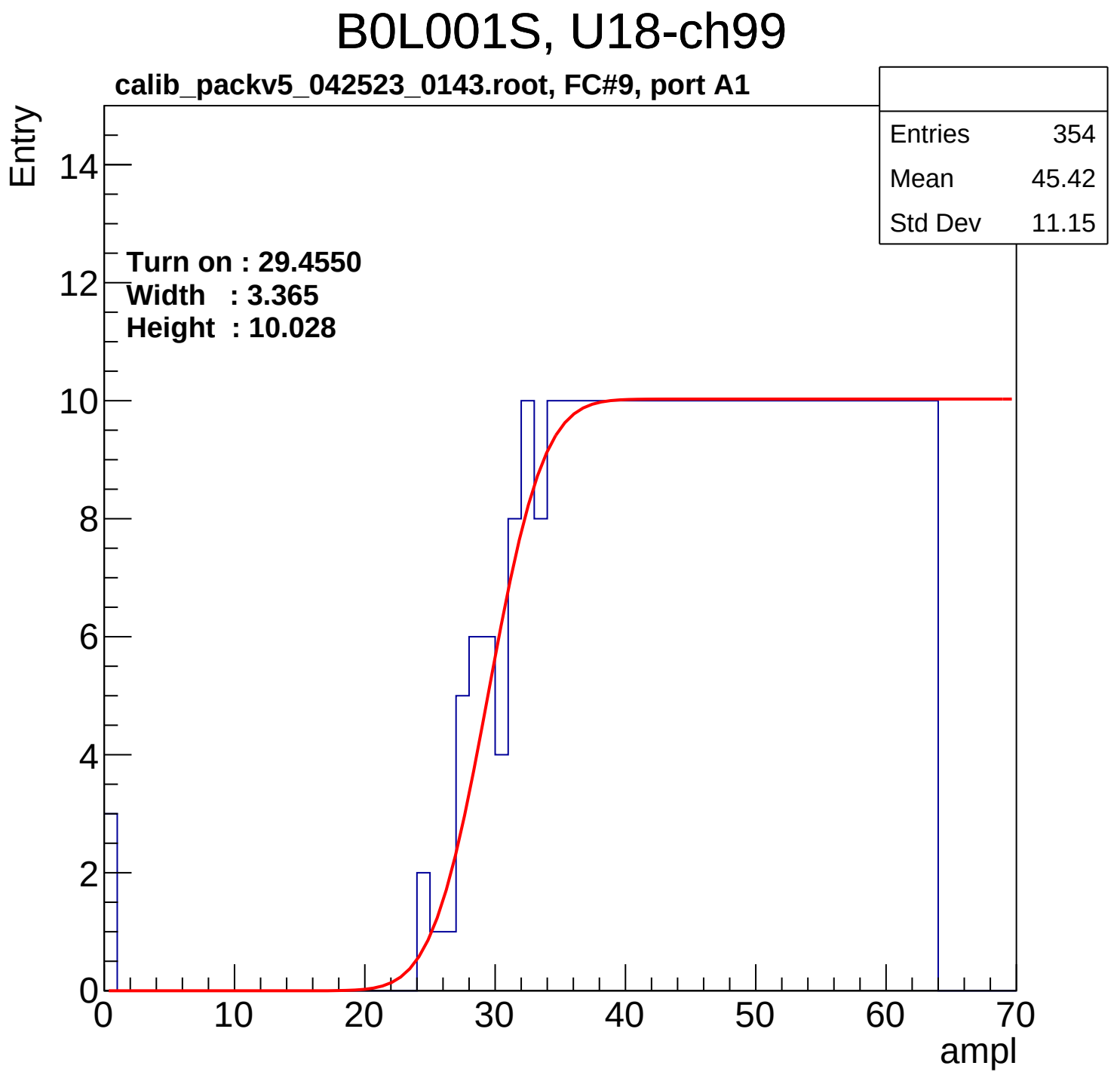

B0L001S, U18-ch94
calib_packv5_042523_0143.root, FC#9, port A1
Entries 381
Mean 44.12
Std Dev 11.92
Turn on : 27.1535
Width : 2.976
Height : 10.062
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

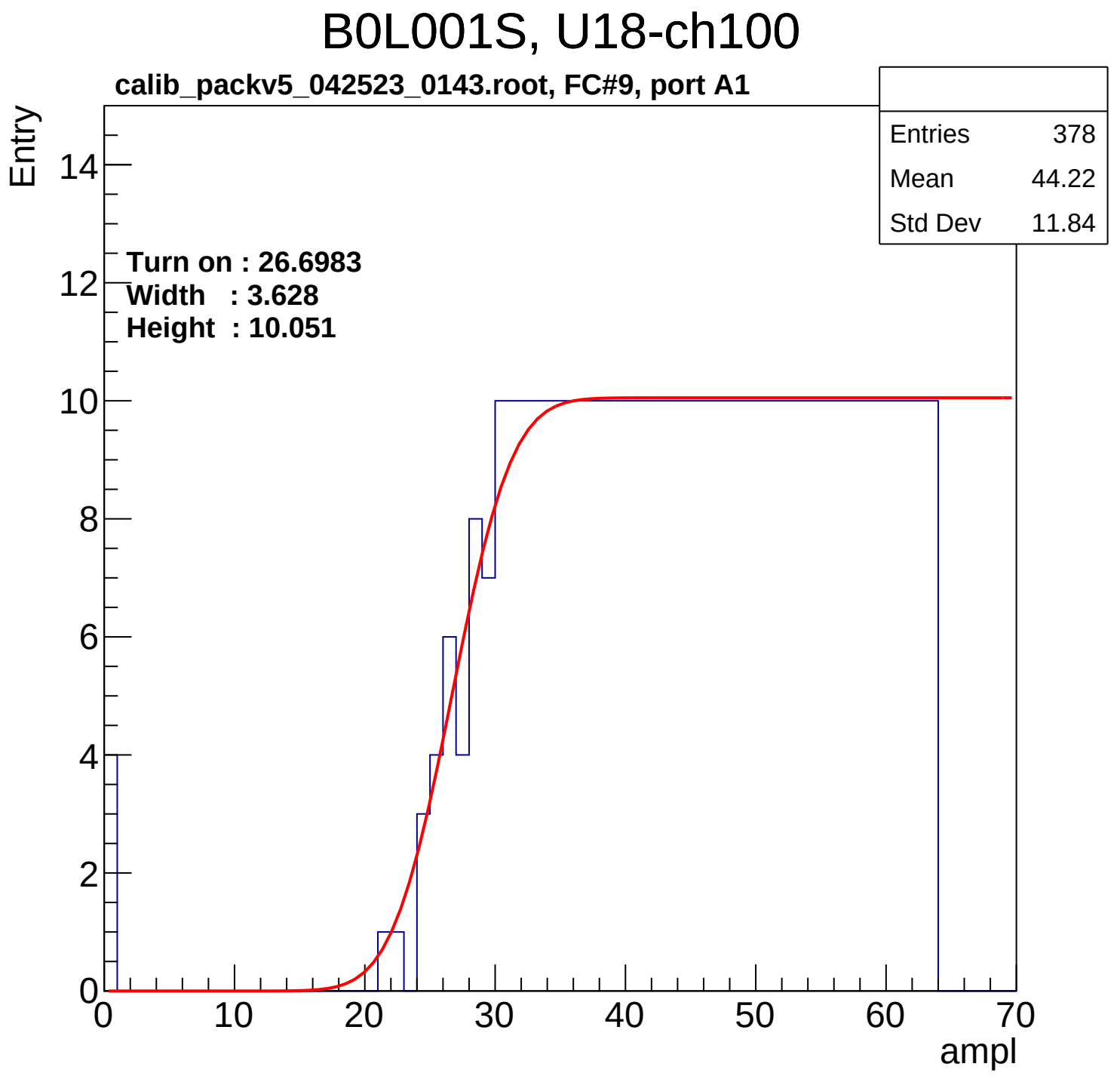

B0L001S, U18-ch95
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.68
Std Dev 11.79
Turn on : 28.1068
Width : 3.356
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

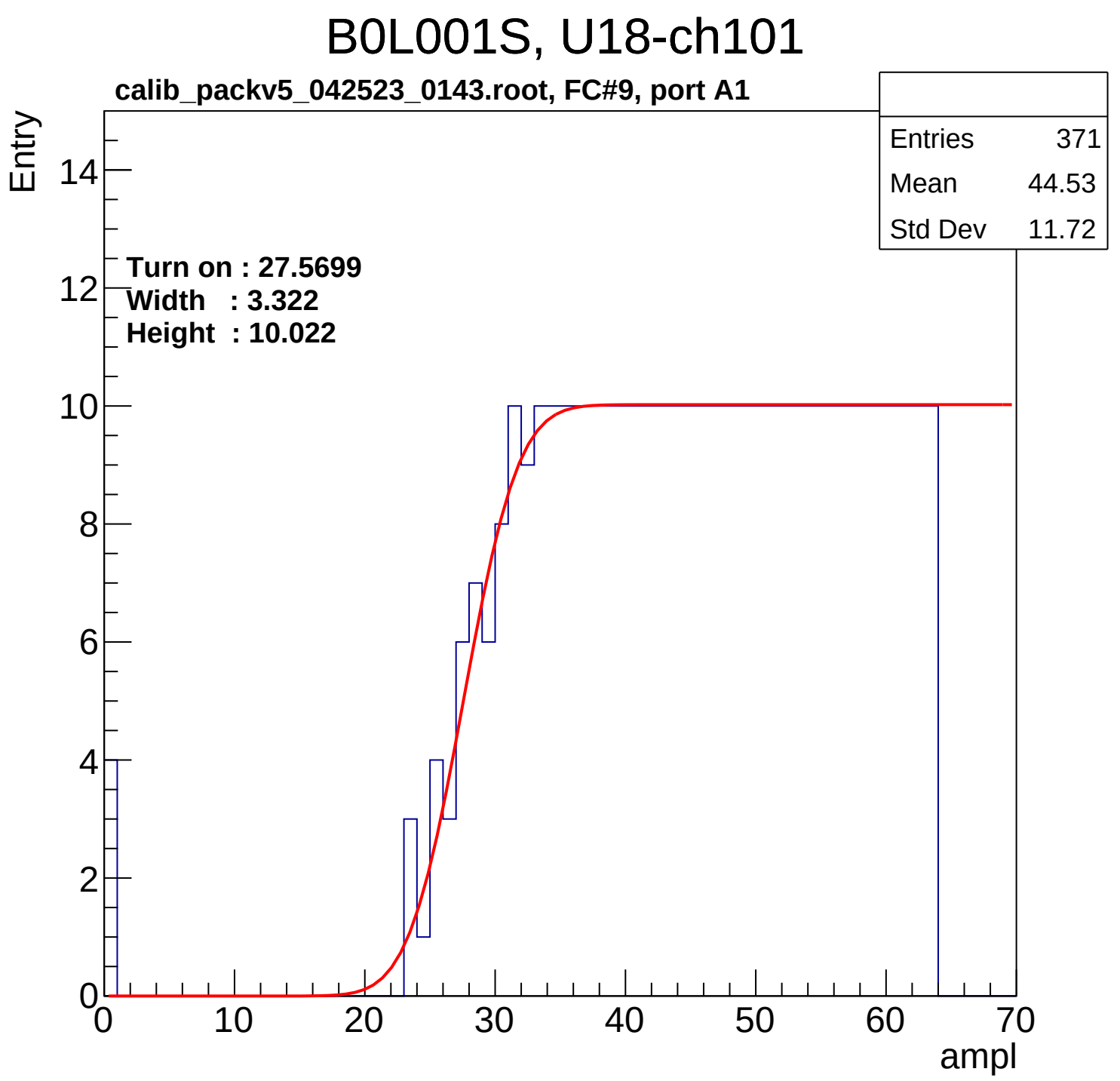

B0L001S, U18-ch96
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.09
Std Dev 12.46
Turn on : 27.8879
Width : 4.144
Height : 10.065
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

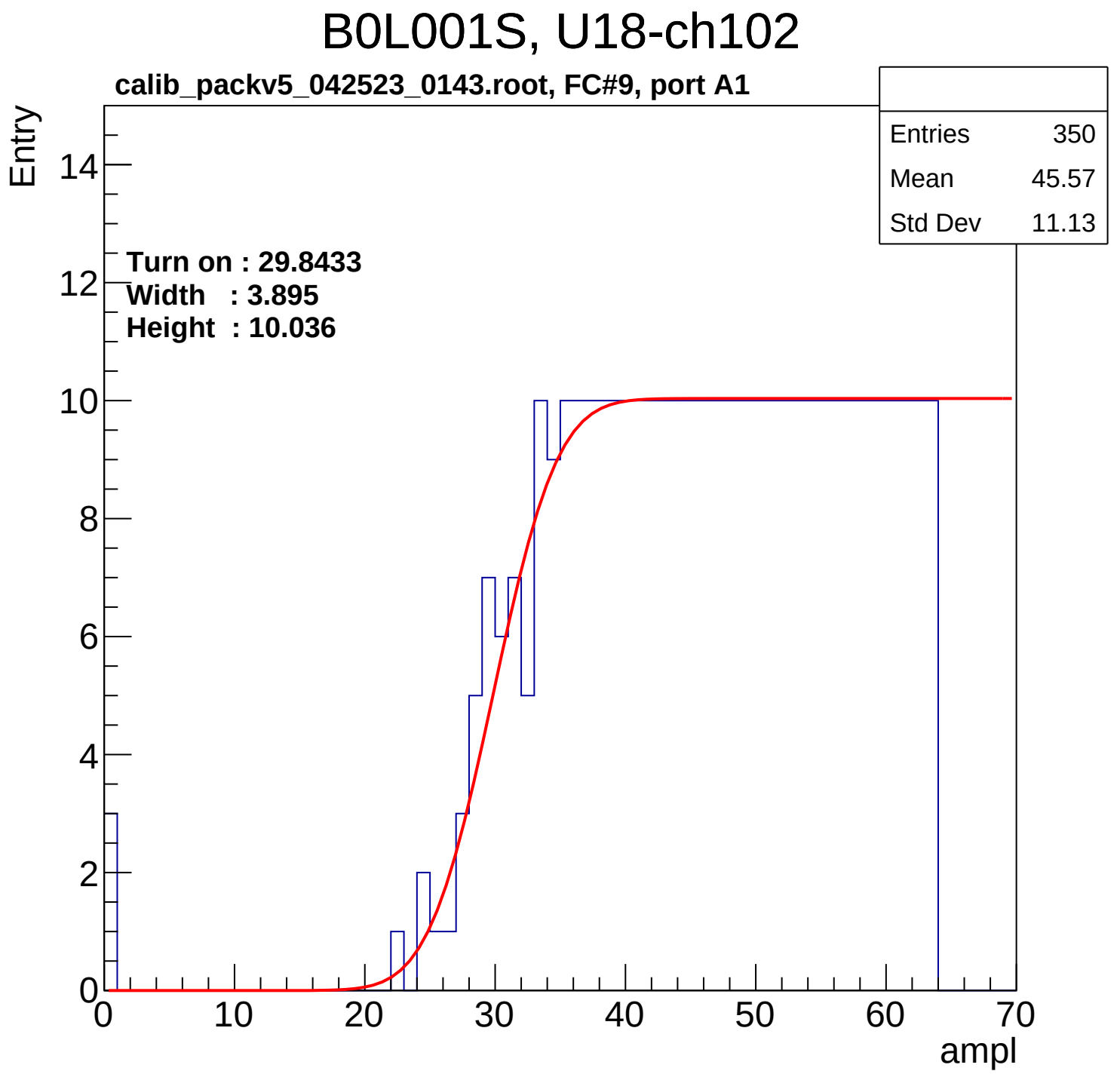

B0L001S, U18-ch97
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.46
Std Dev 11.46
Turn on : 26.6301
Width : 3.176
Height : 9.949
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

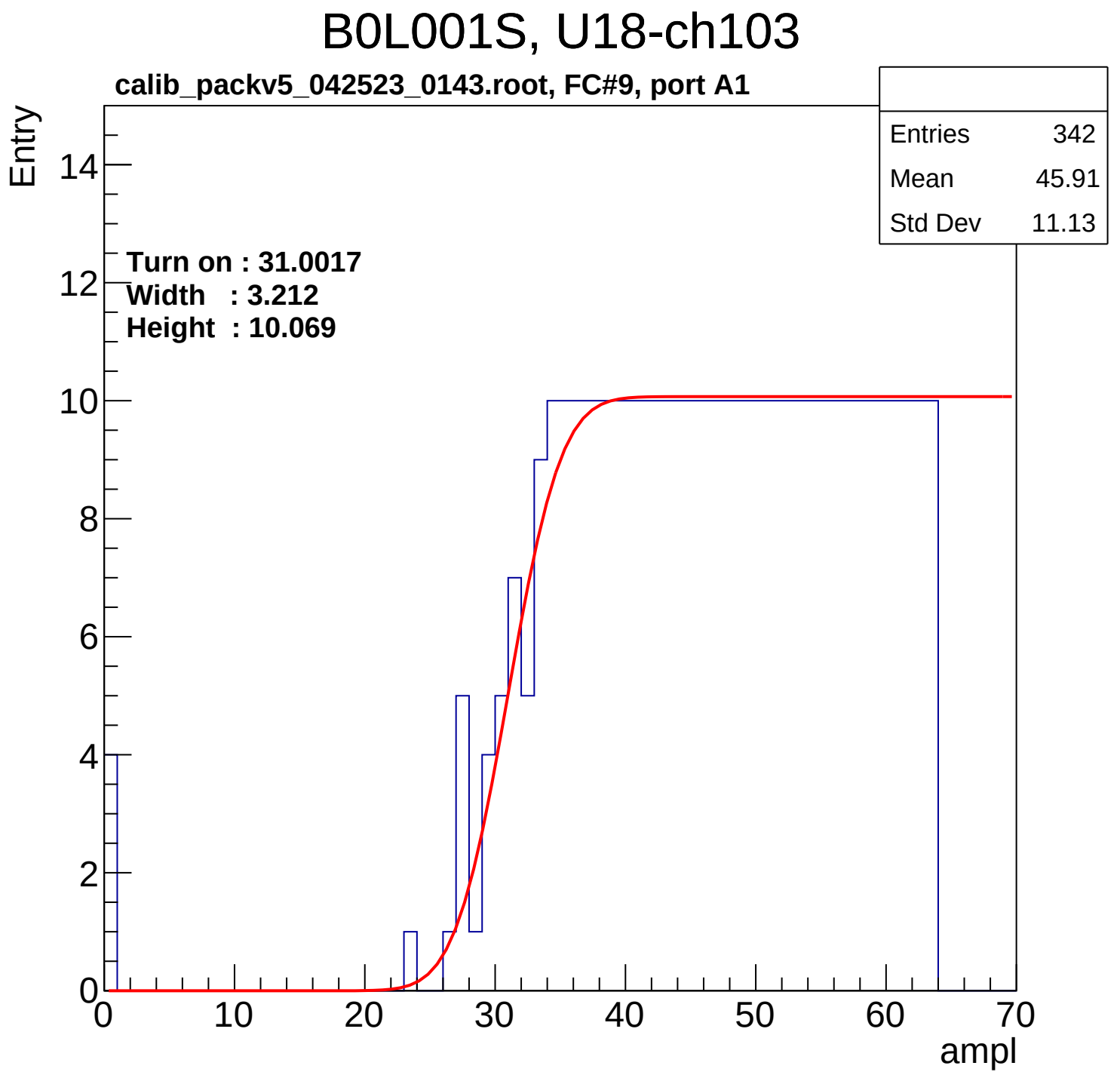

B0L001S, U18-ch98
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.9
Std Dev 11.04
Turn on : 27.7146
Width : 2.668
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

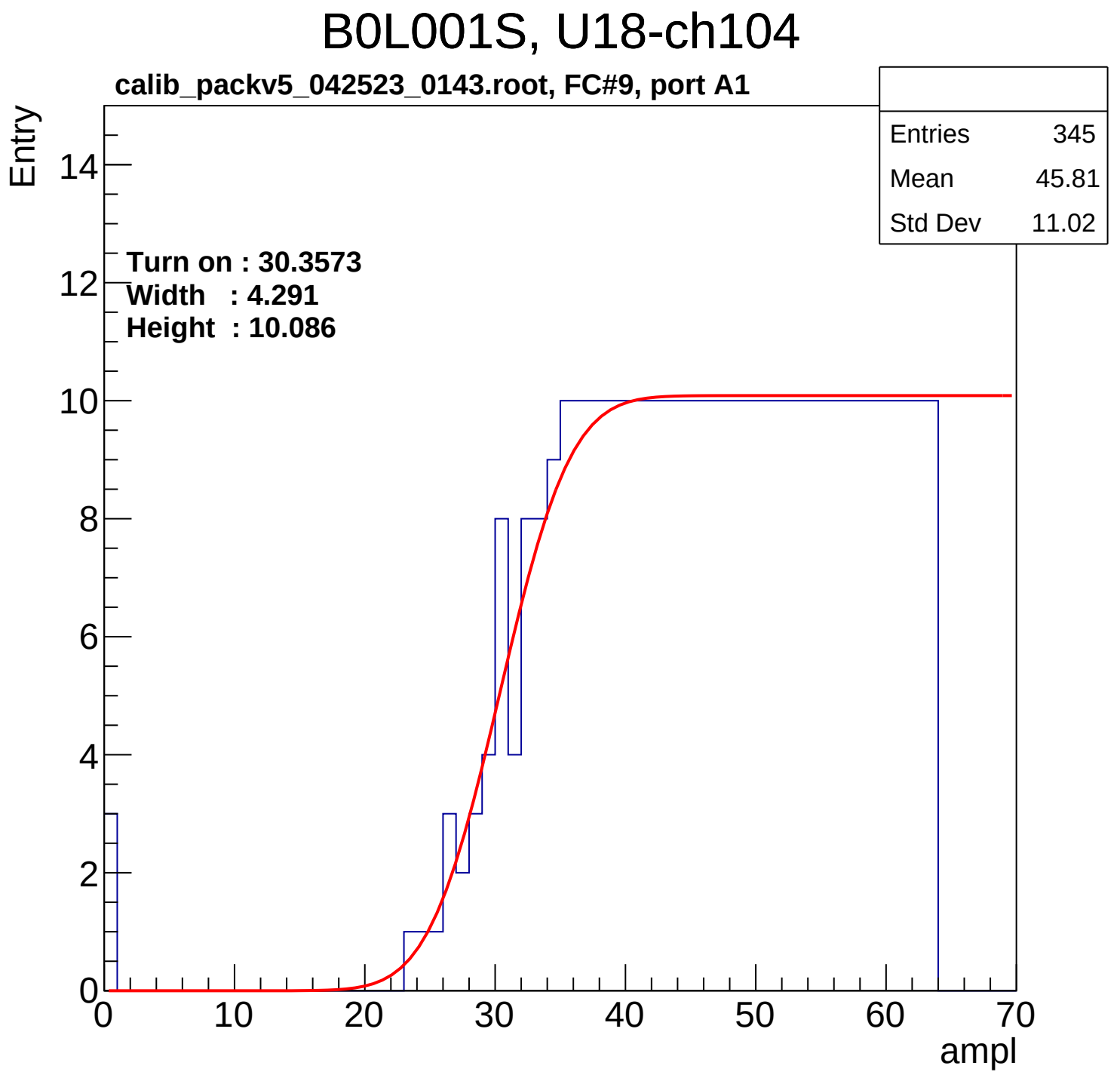

B0L001S, U18-ch99
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.42
Std Dev 11.15
Turn on : 29.4550
Width : 3.365
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

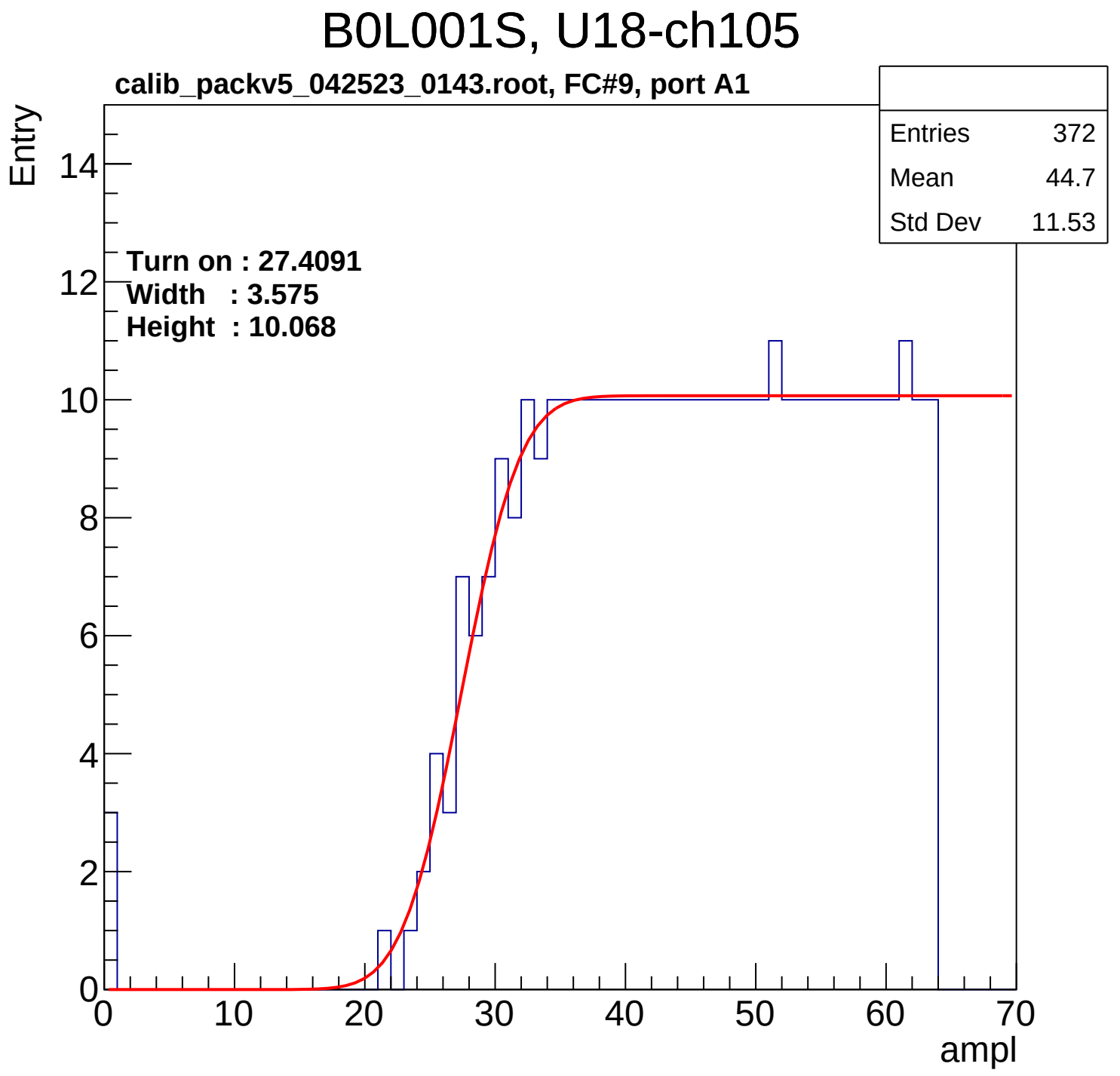

B0L001S, U18-ch100
calib_packv5_042523_0143.root, FC#9, port A1
Entries 378
Mean 44.22
Std Dev 11.84
Turn on : 26.6983
Width : 3.628
Height : 10.051
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

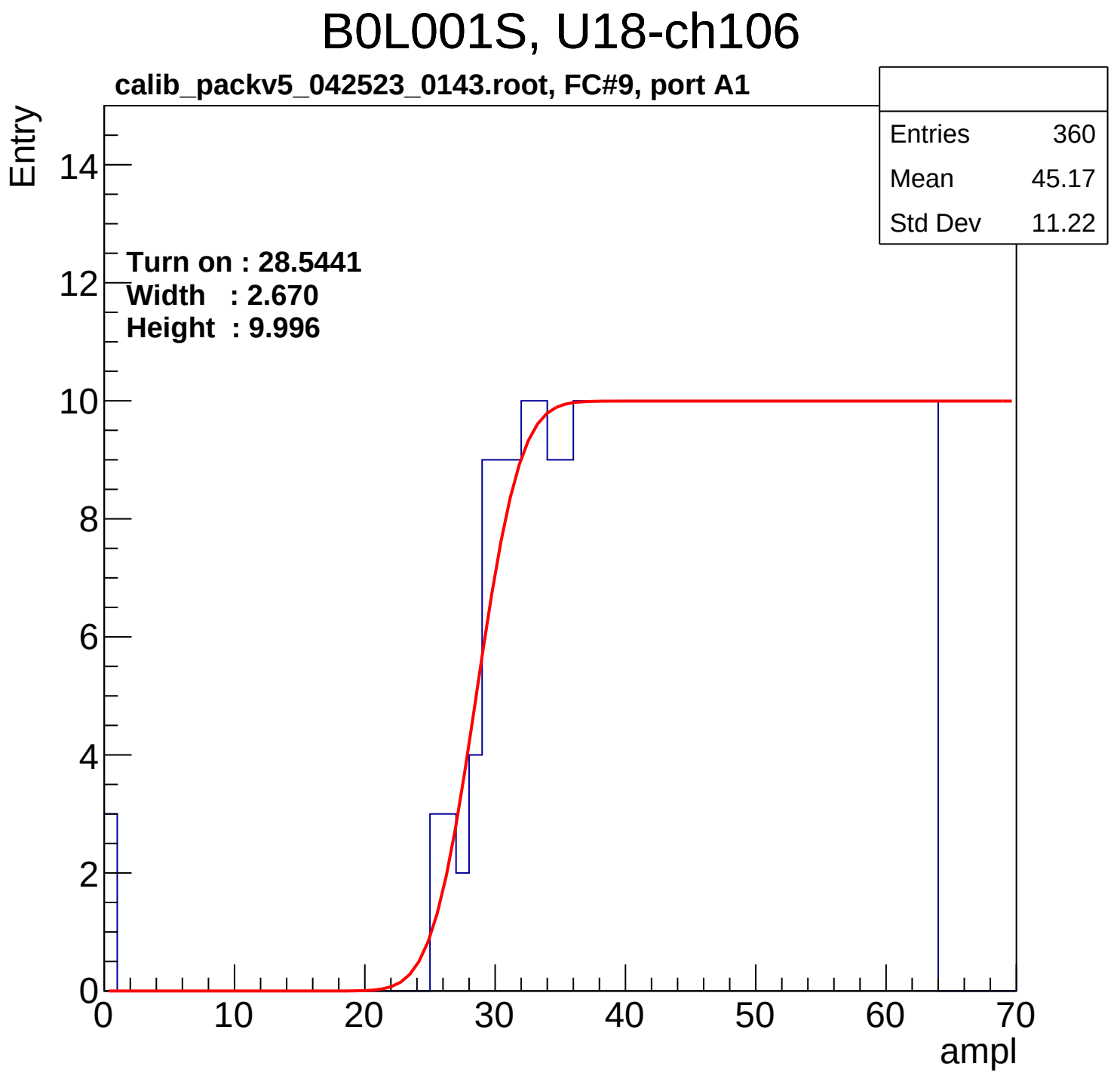

B0L001S, U18-ch101
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.53
Std Dev 11.72
Turn on : 27.5699
Width : 3.322
Height : 10.022
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

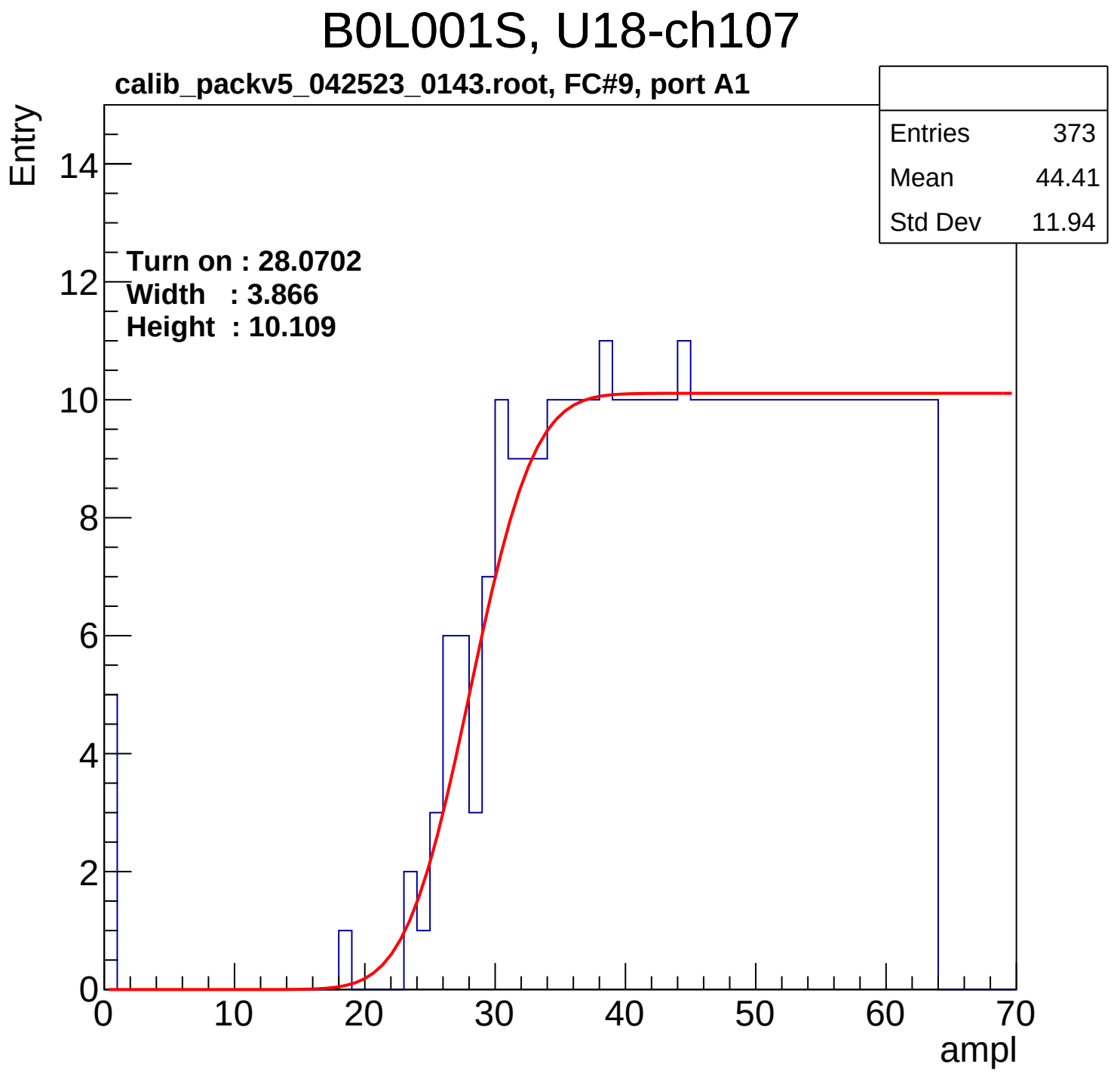

B0L001S, U18-ch102
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.57
Std Dev 11.13
Turn on : 29.8433
Width : 3.895
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

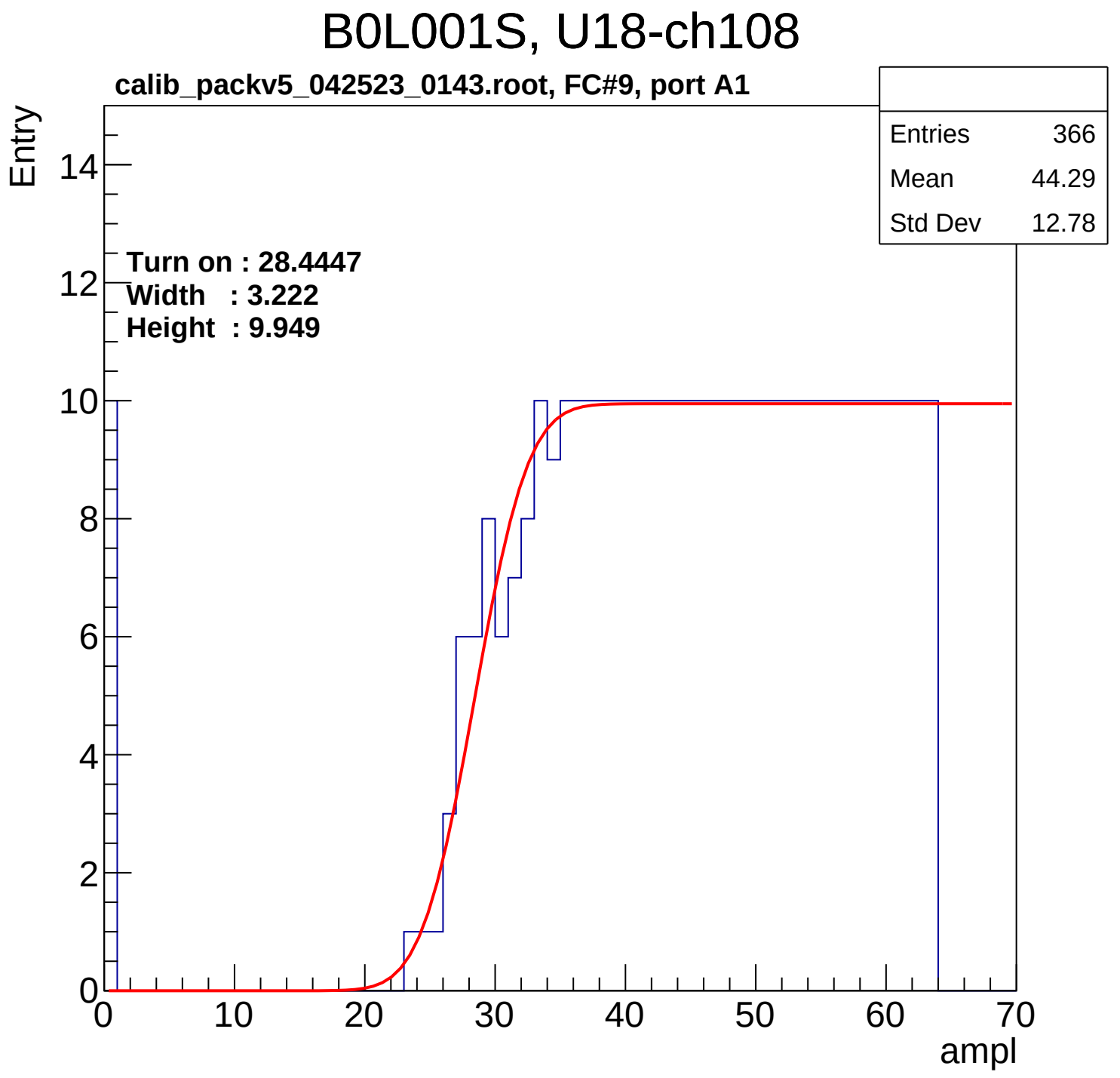

B0L001S, U18-ch103
calib_packv5_042523_0143.root, FC#9, port A1
Entries 342
Mean 45.91
Std Dev 11.13
Turn on : 31.0017
Width : 3.212
Height : 10.069
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

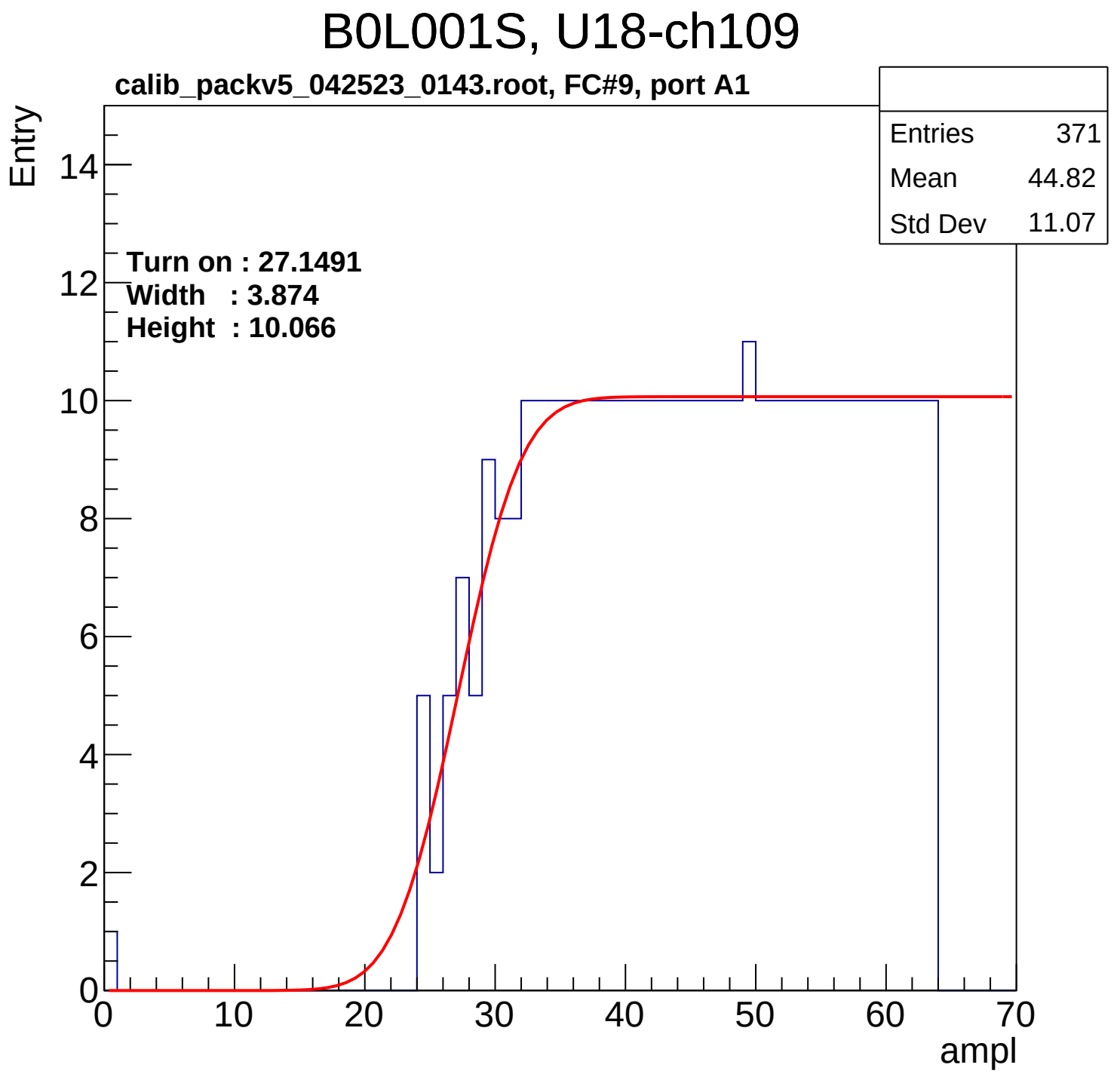

B0L001S, U18-ch104
calib_packv5_042523_0143.root, FC#9, port A1
Entries 345
Mean 45.81
Std Dev 11.02
Turn on : 30.3573
Width : 4.291
Height : 10.086
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

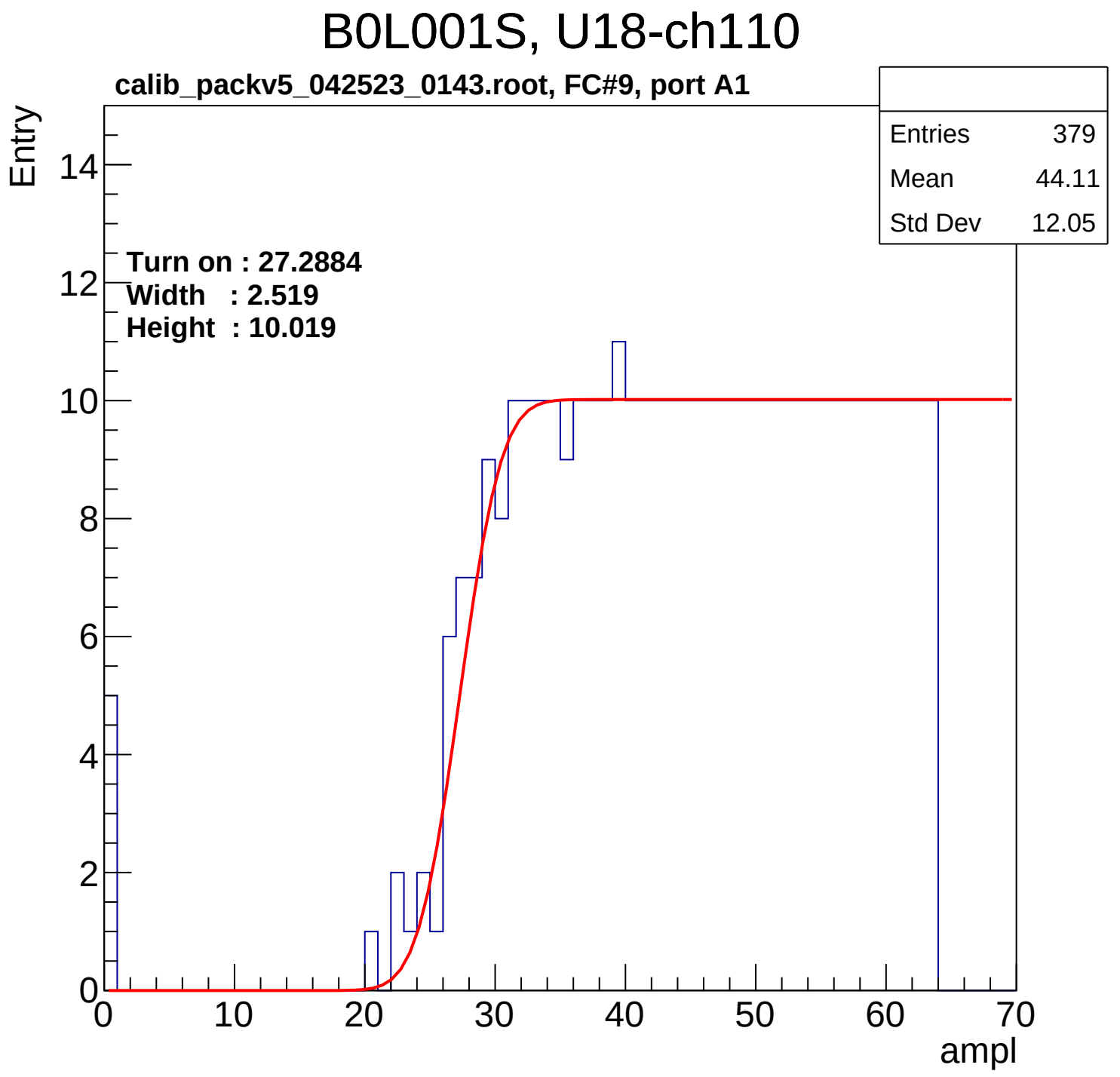

B0L001S, U18-ch105
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.7
Std Dev 11.53
Turn on : 27.4091
Width : 3.575
Height : 10.068
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

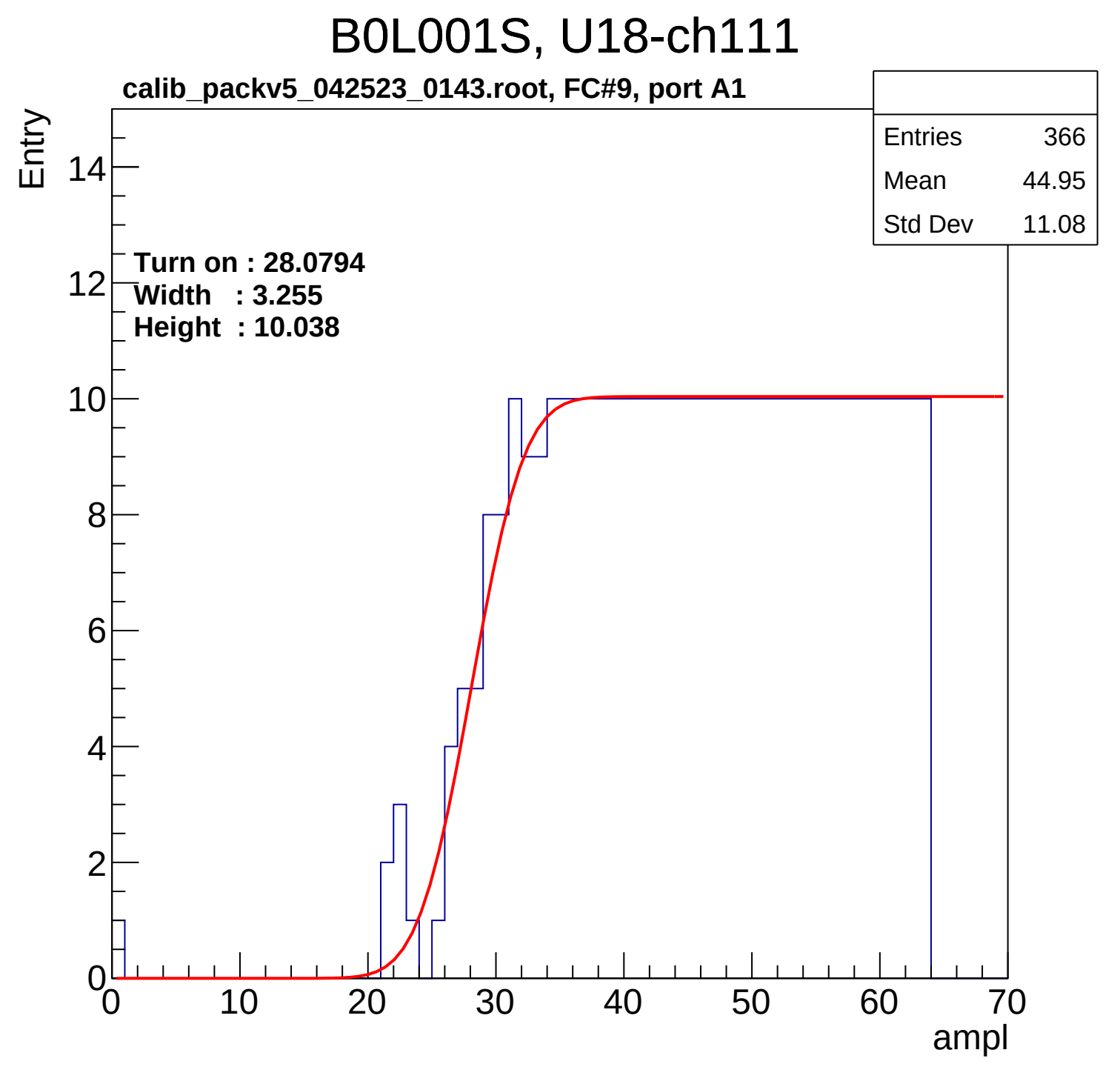

B0L001S, U18-ch106
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.17
Std Dev 11.22
Turn on : 28.5441
Width : 2.670
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

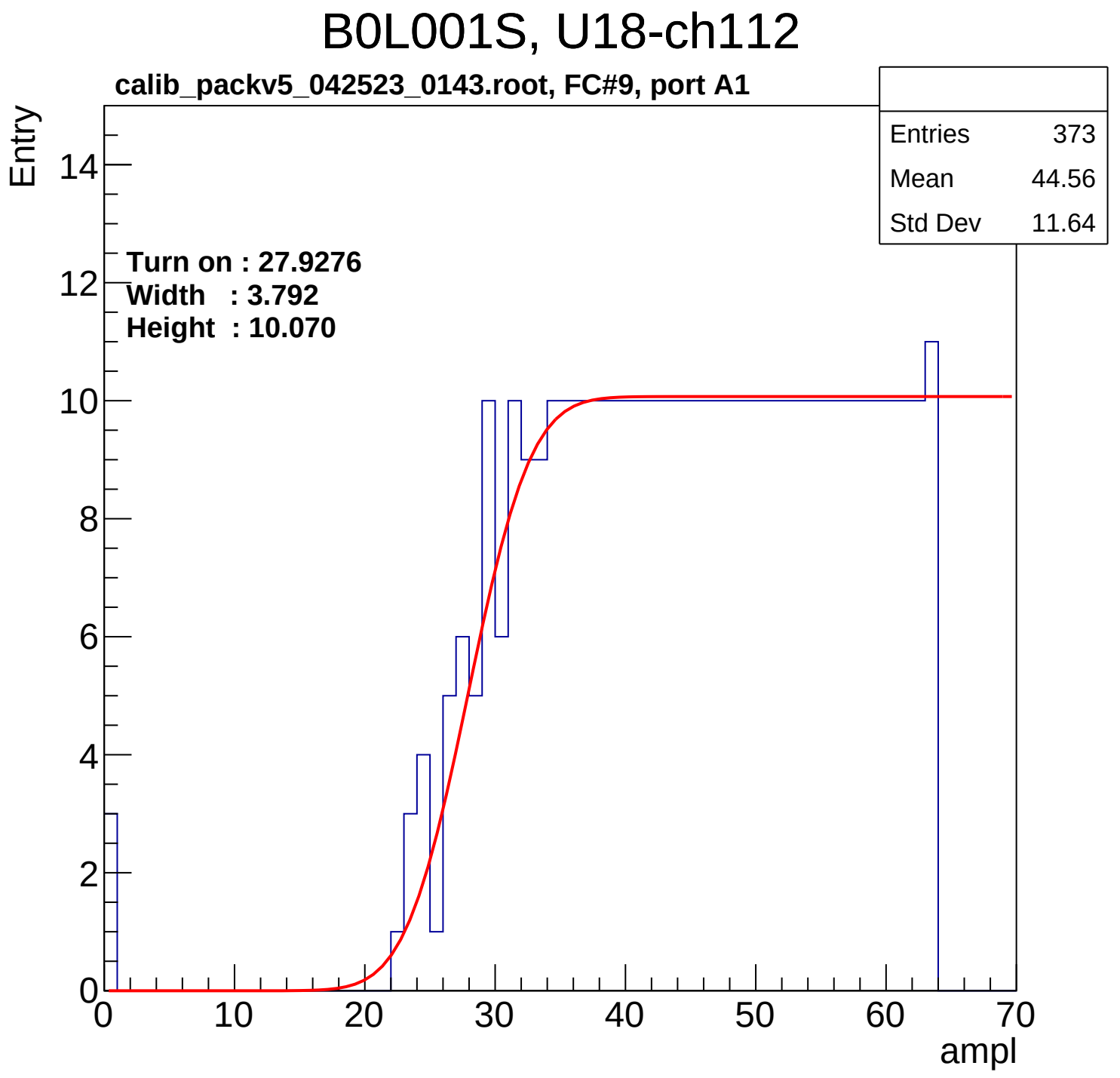

B0L001S, U18-ch107
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.41
Std Dev 11.94
Turn on : 28.0702
Width : 3.866
Height : 10.109
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

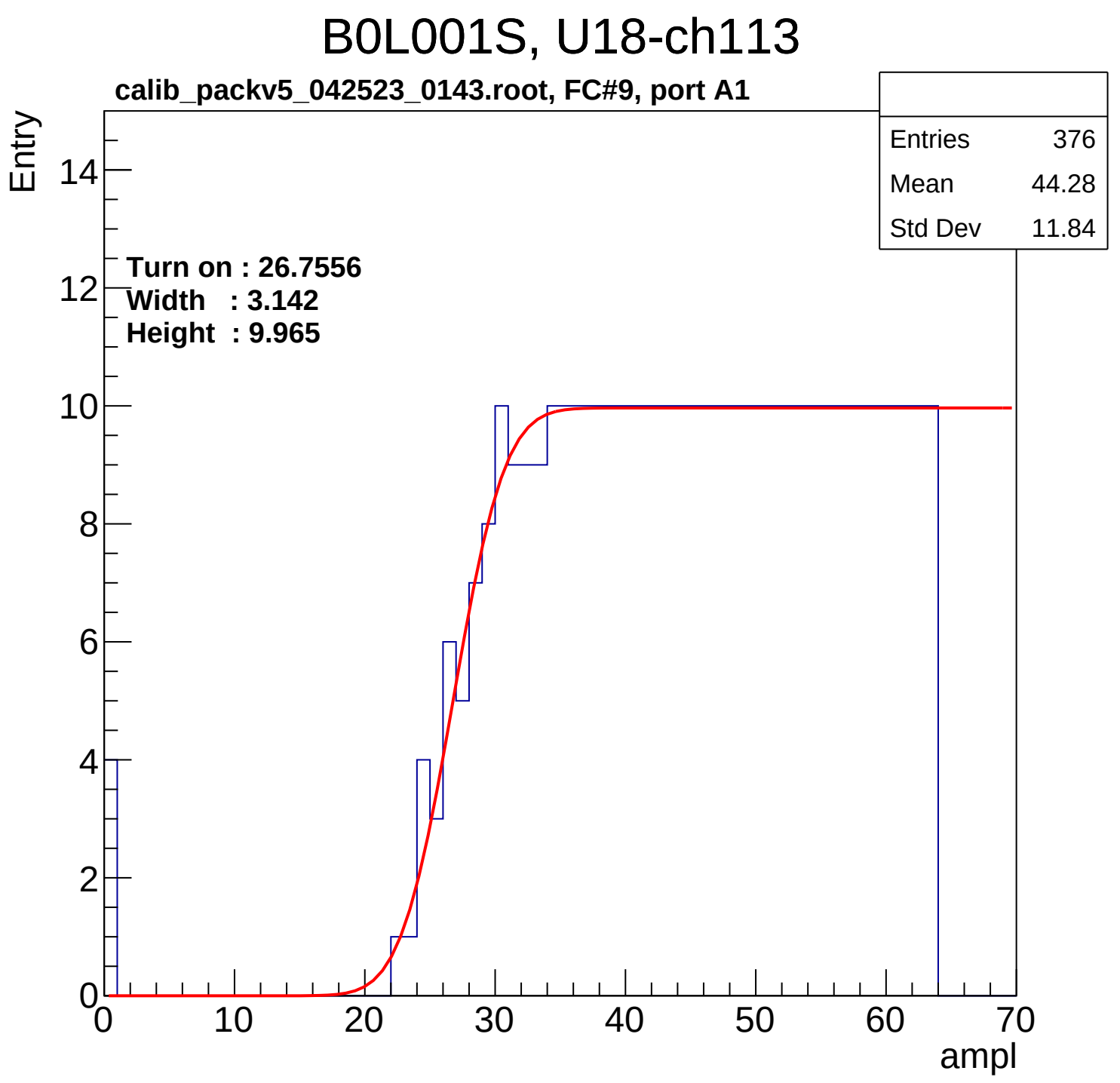

B0L001S, U18-ch108
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.29
Std Dev 12.78
Turn on : 28.4447
Width : 3.222
Height : 9.949
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

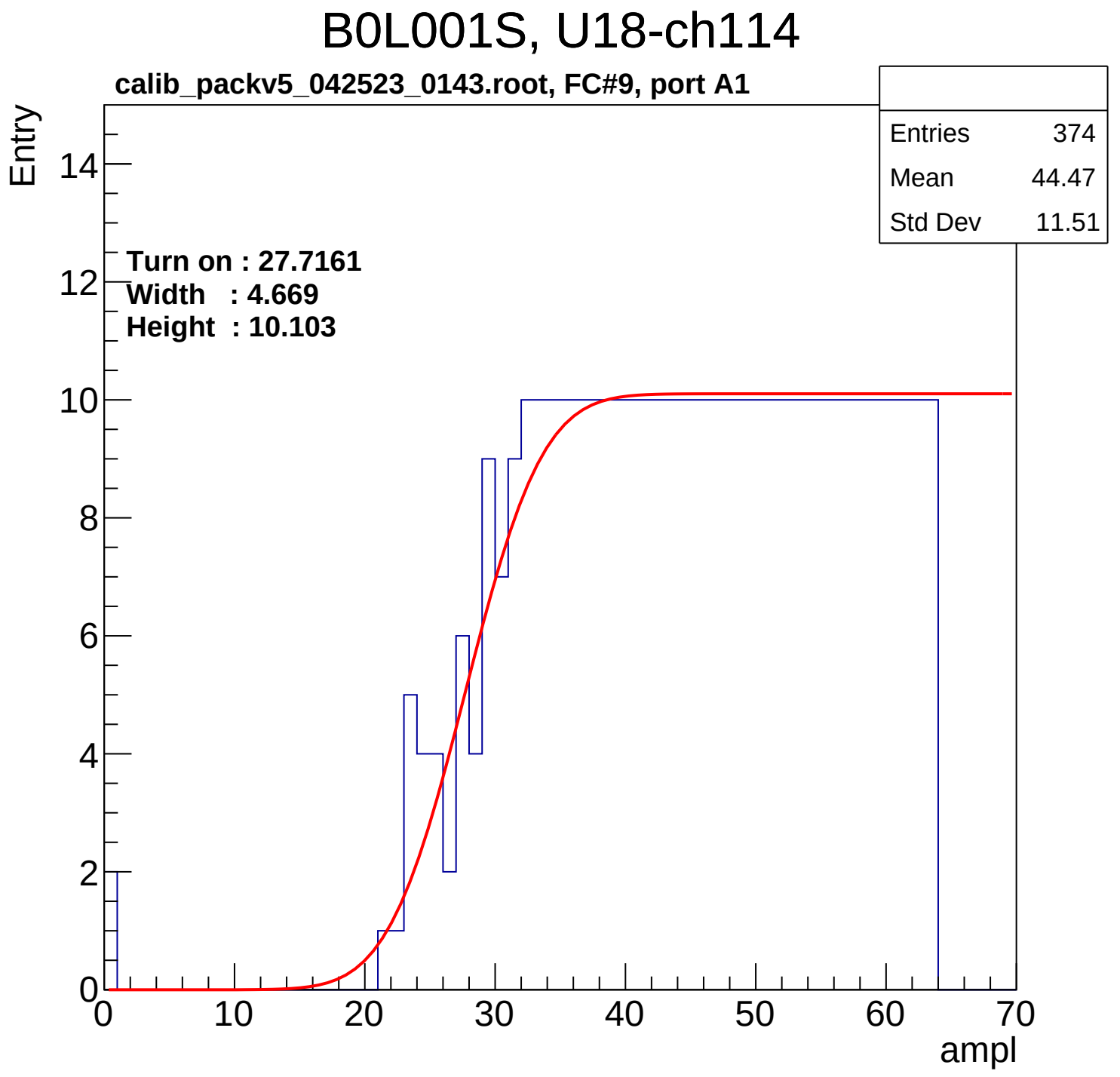

B0L001S, U18-ch109
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.82
Std Dev 11.07
Turn on : 27.1491
Width : 3.874
Height : 10.066
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

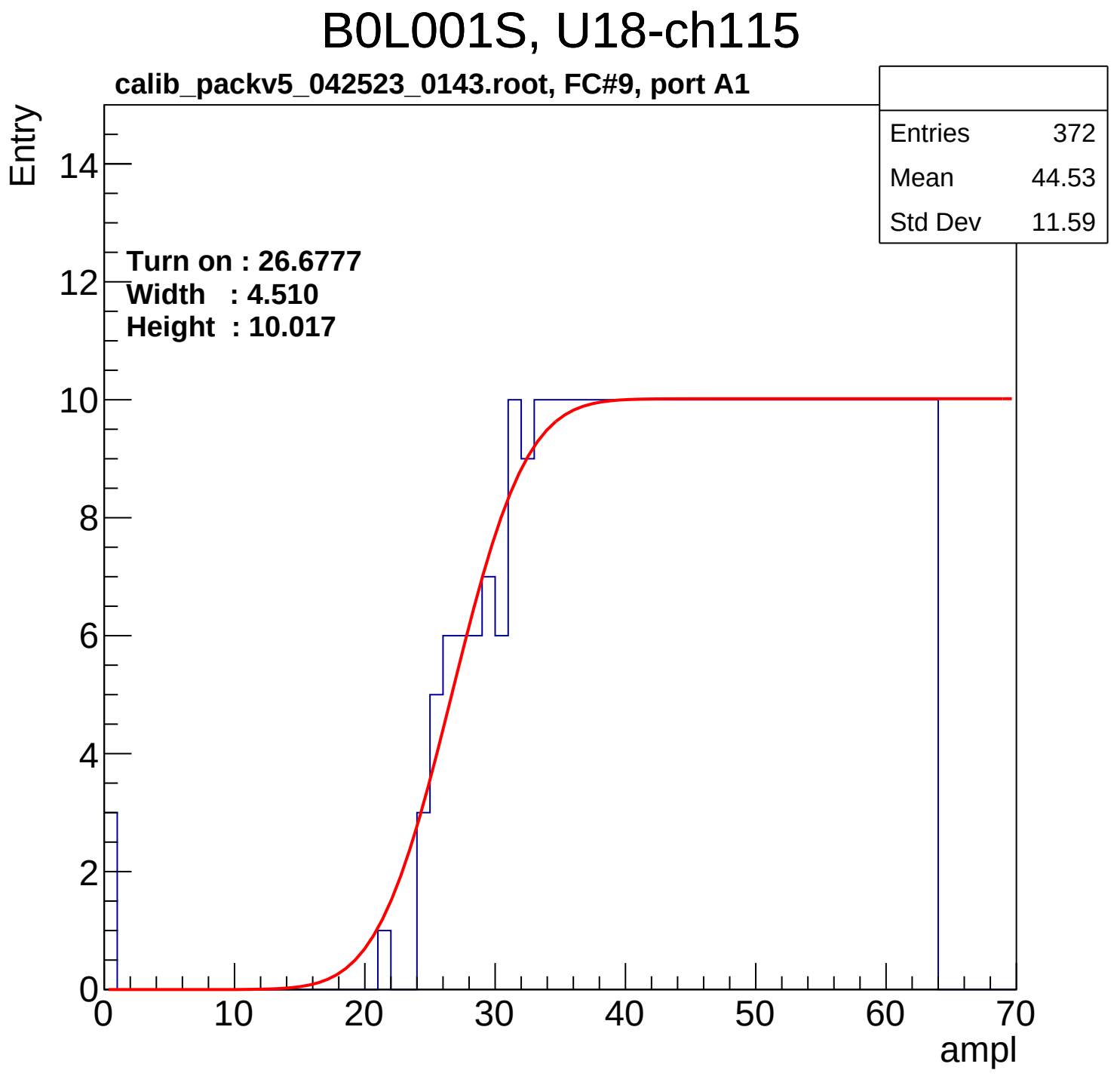

B0L001S, U18-ch110
calib_packv5_042523_0143.root, FC#9, port A1
Entries 379
Mean 44.11
Std Dev 12.05
Turn on : 27.2884
Width : 2.519
Height : 10.019
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

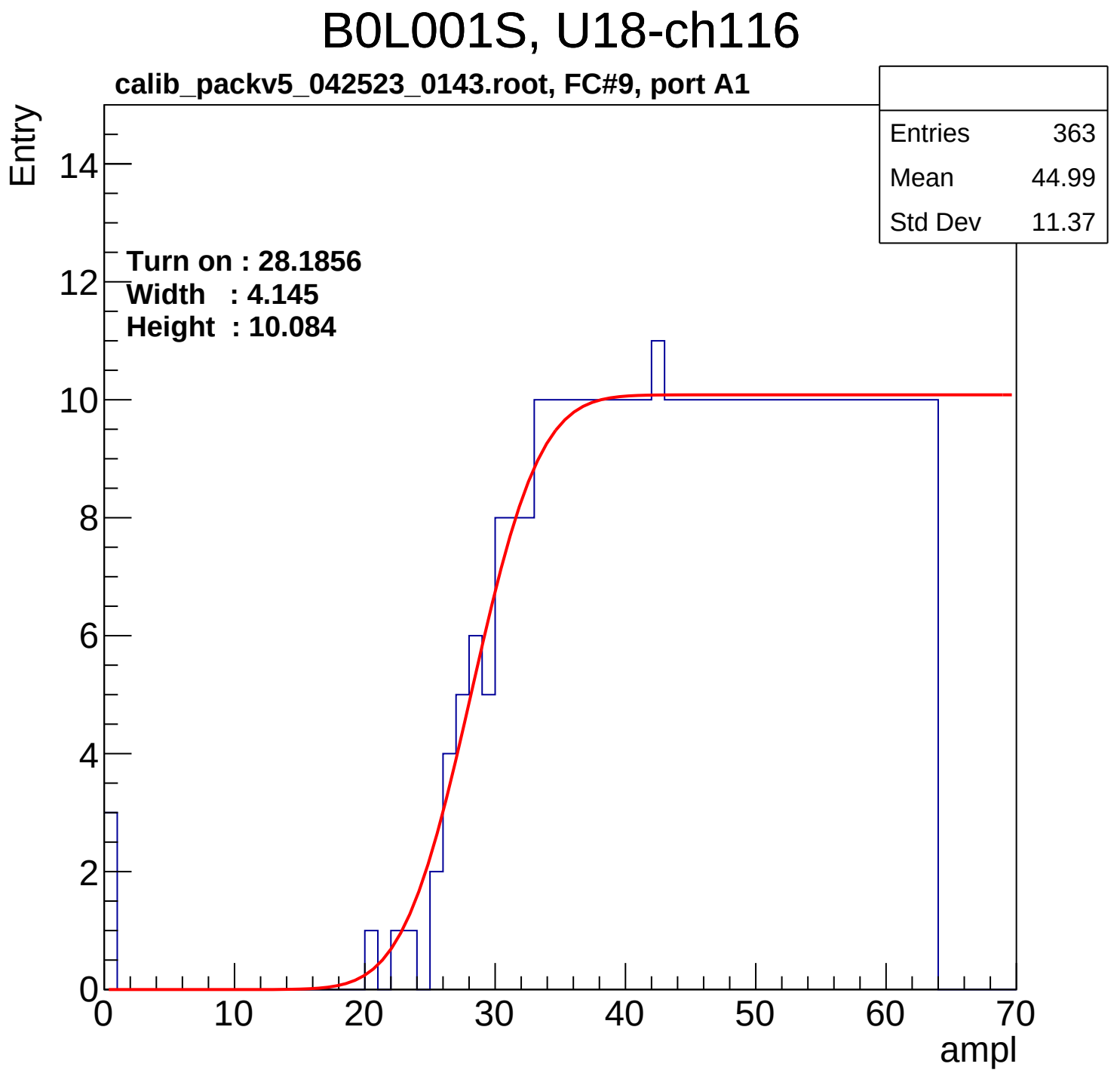

B0L001S, U18-ch111
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.95
Std Dev 11.08
Turn on : 28.0794
Width : 3.255
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

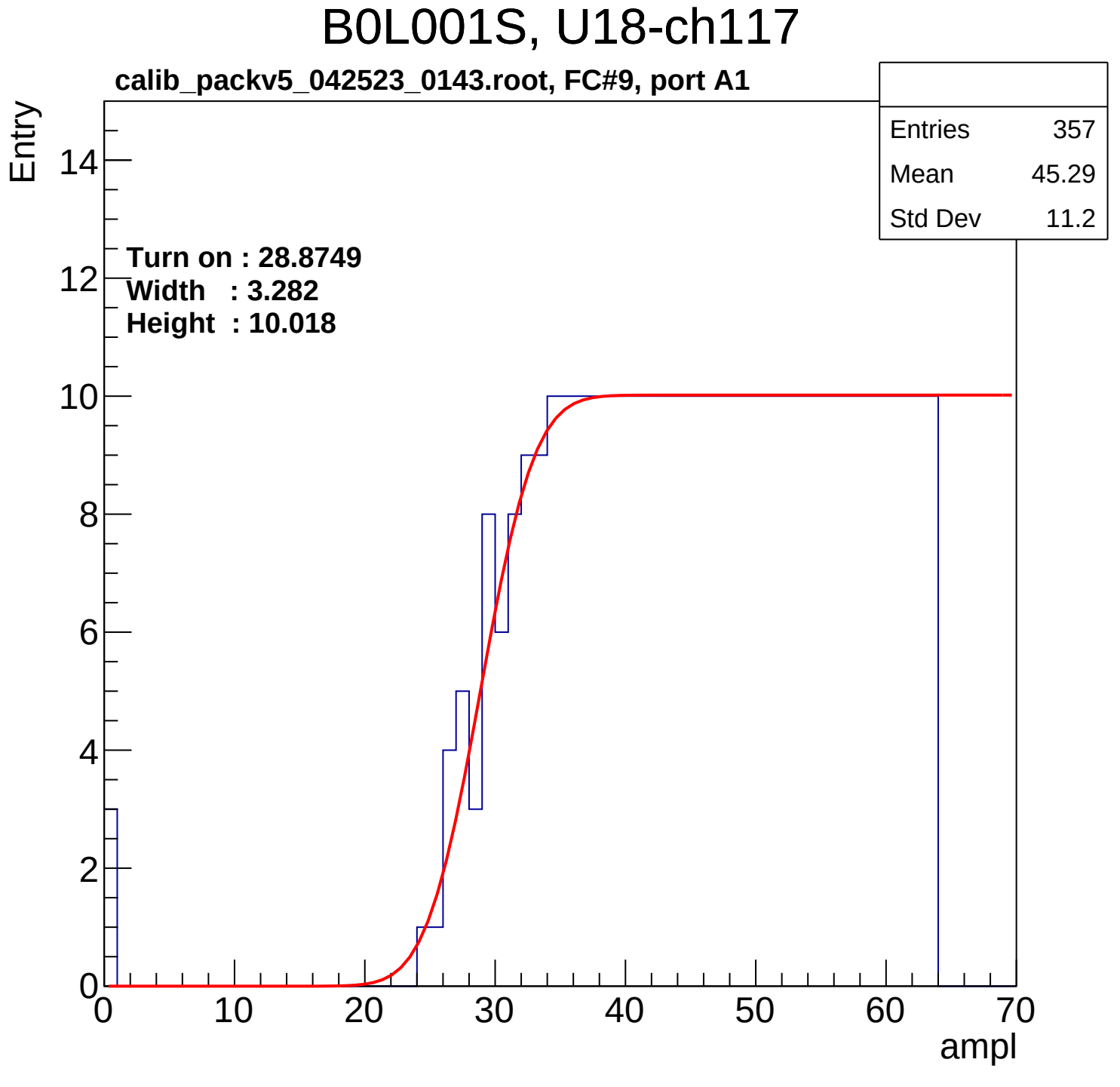

B0L001S, U18-ch112
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.56
Std Dev 11.64
Turn on : 27.9276
Width : 3.792
Height : 10.070
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

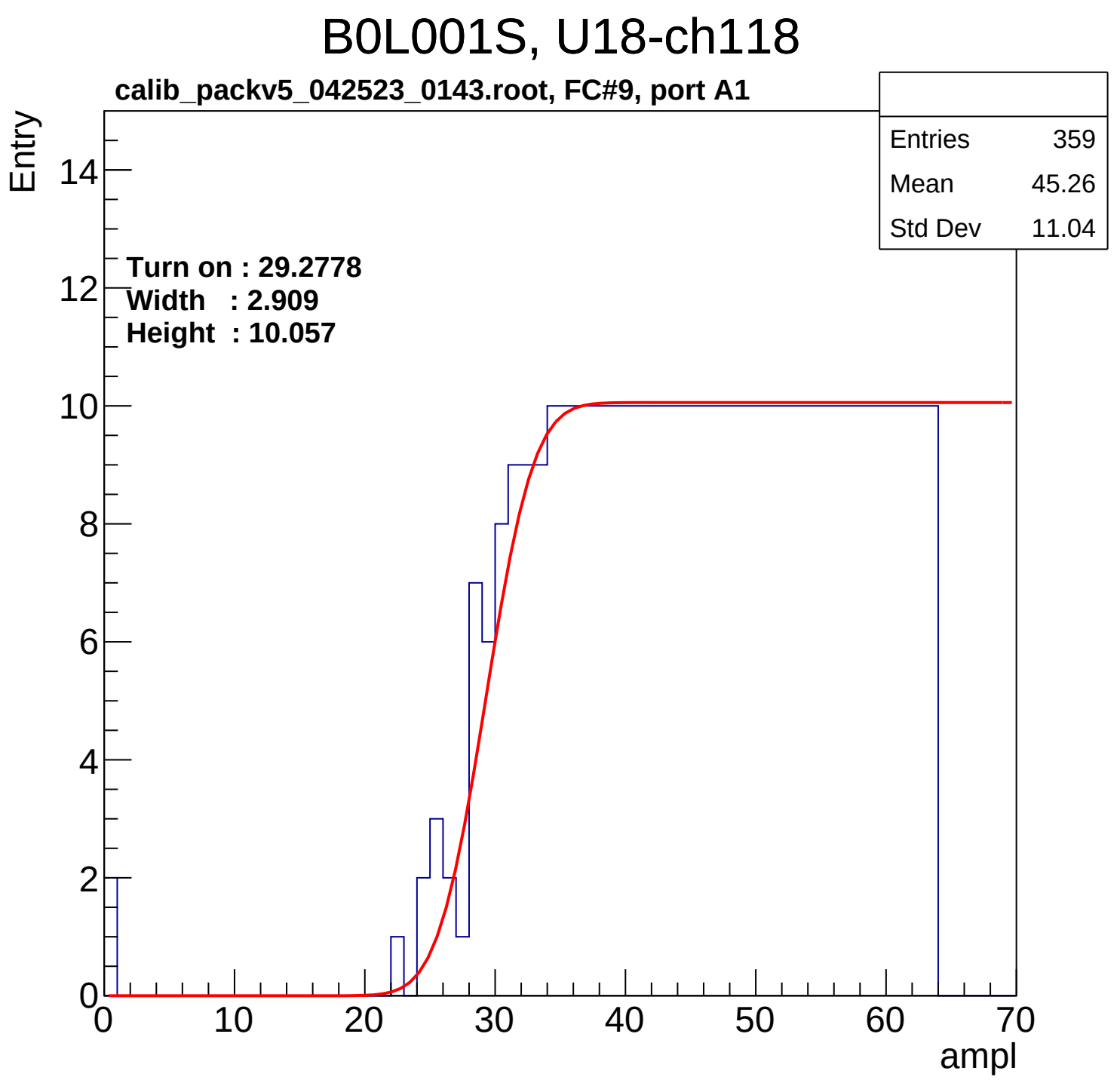

B0L001S, U18-ch113
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.28
Std Dev 11.84
Turn on : 26.7556
Width : 3.142
Height : 9.965
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

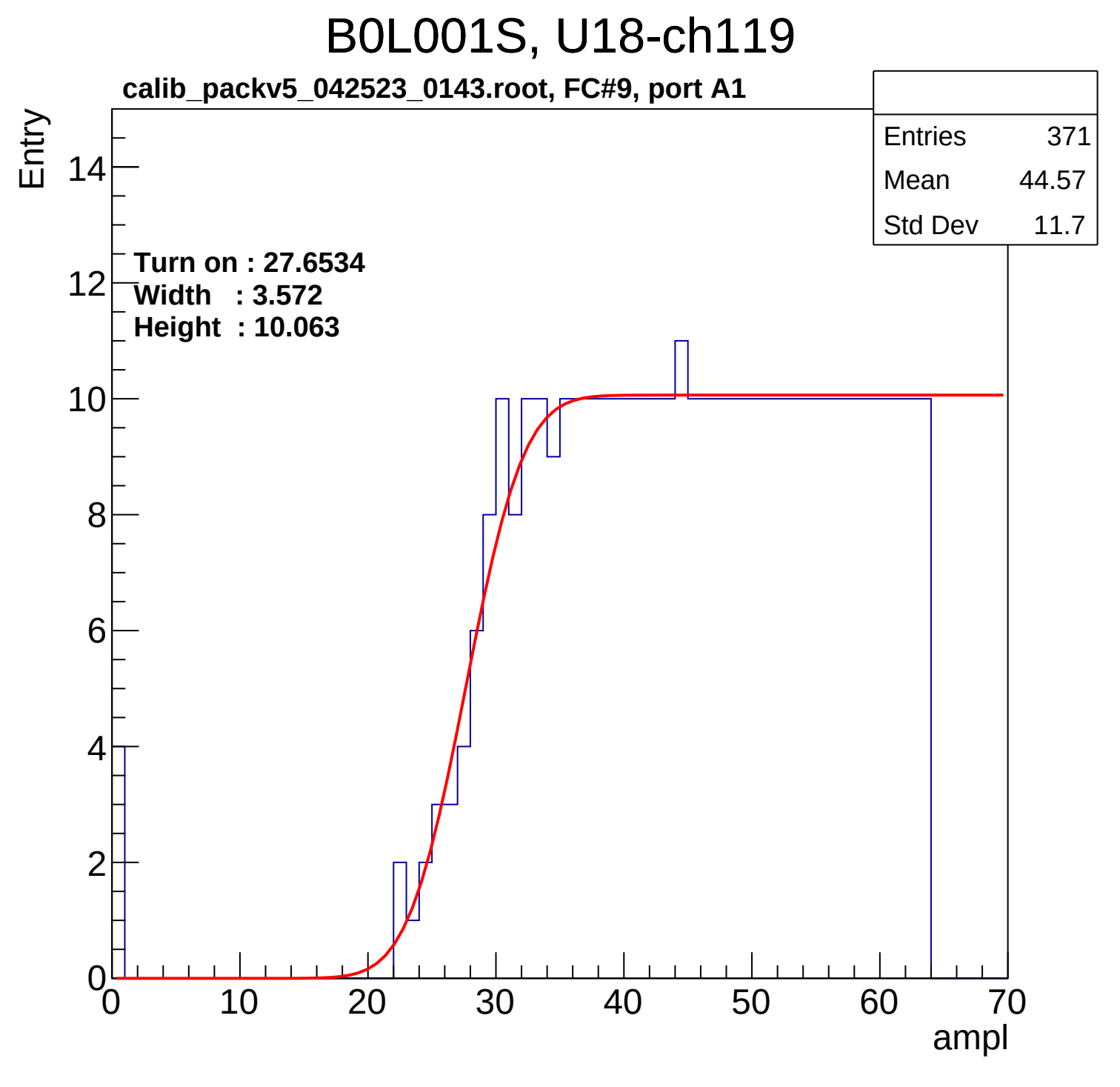

B0L001S, U18-ch114
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.47
Std Dev 11.51
Turn on : 27.7161
Width : 4.669
Height : 10.103
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

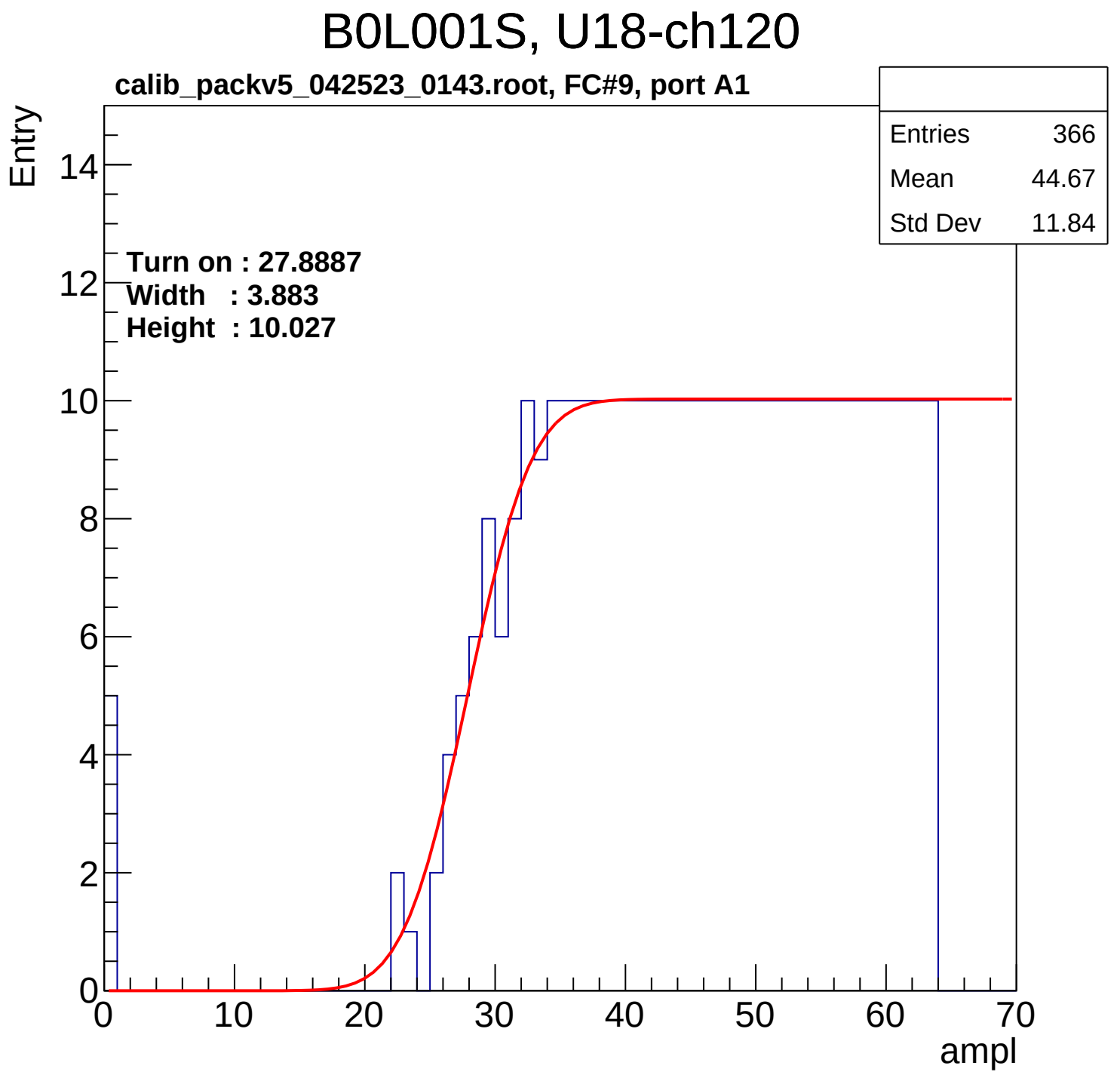

B0L001S, U18-ch115
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.53
Std Dev 11.59
Turn on : 26.6777
Width : 4.510
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

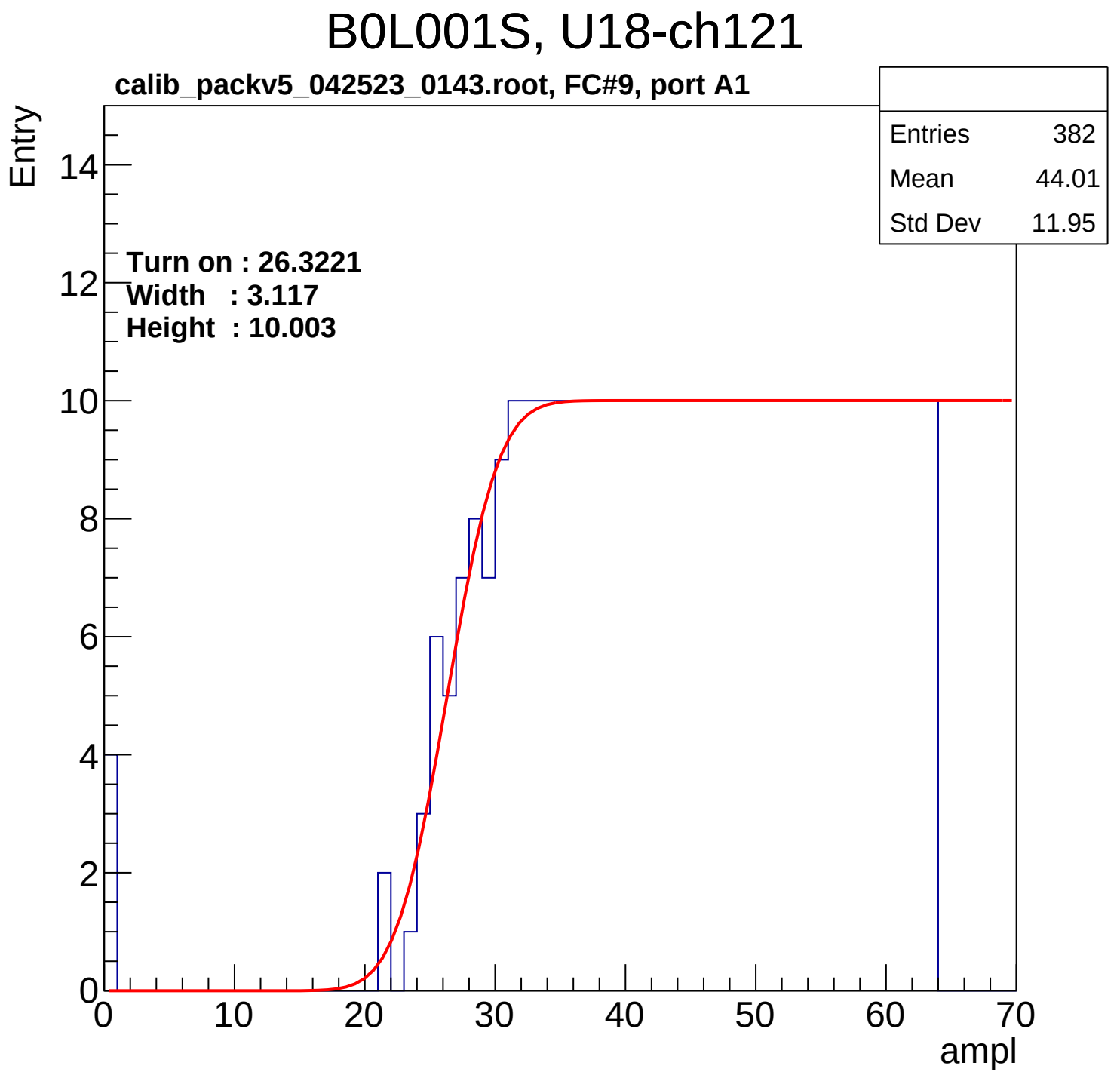

B0L001S, U18-ch116
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 44.99
Std Dev 11.37
Turn on : 28.1856
Width : 4.145
Height : 10.084
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

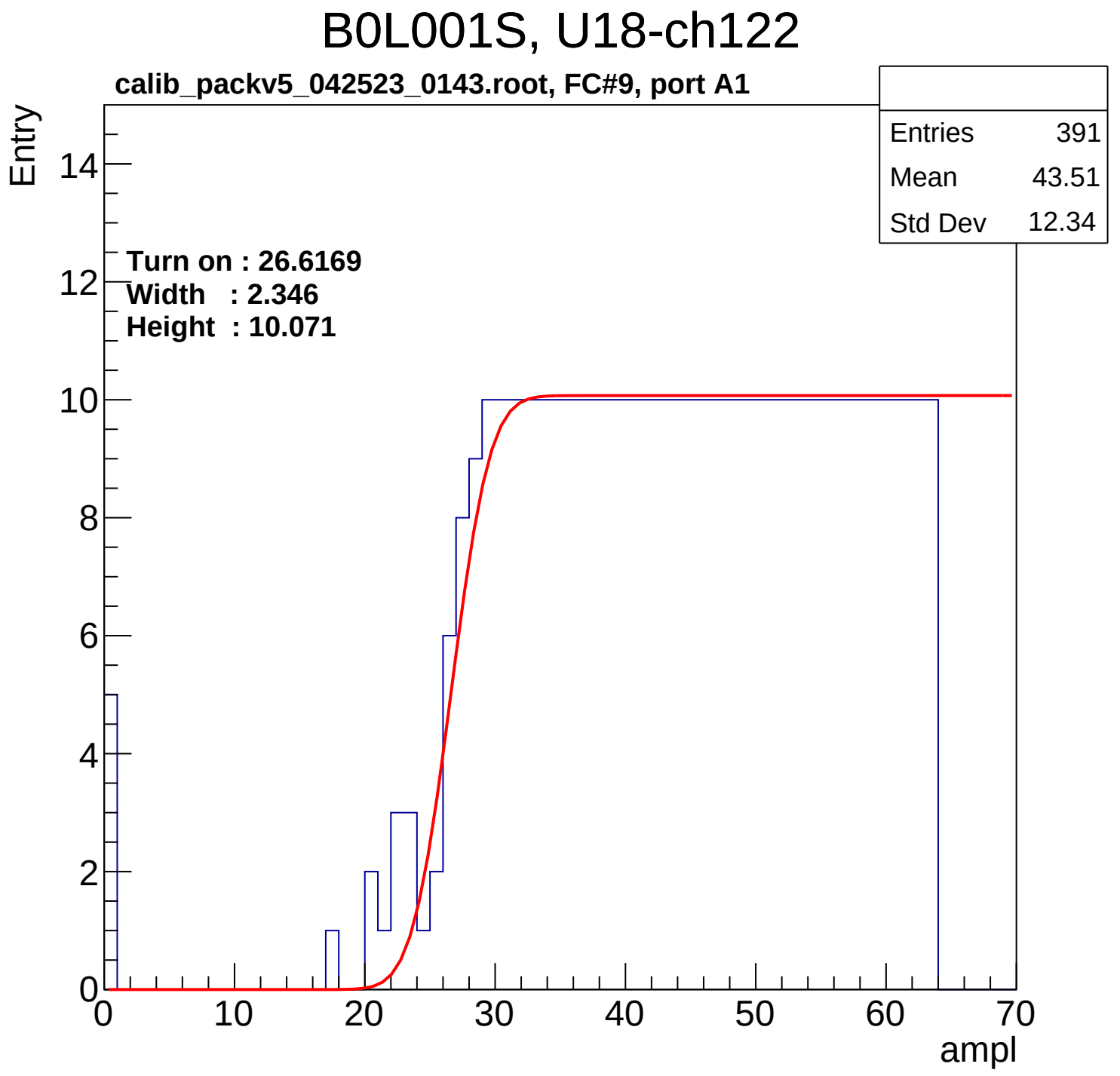

B0L001S, U18-ch117
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.29
Std Dev 11.2
Turn on : 28.8749
Width : 3.282
Height : 10.018
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

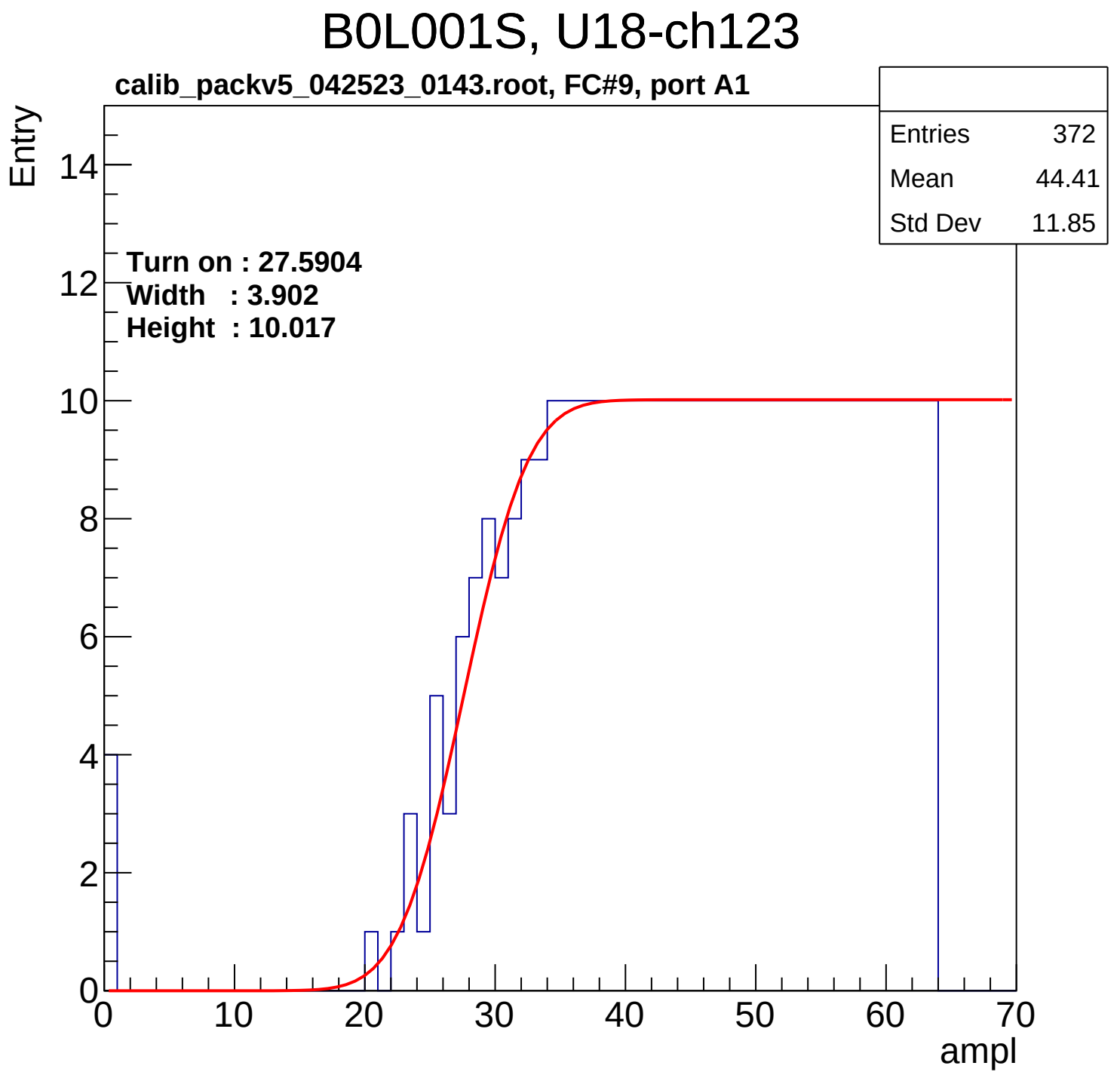

B0L001S, U18-ch118
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.26
Std Dev 11.04
Turn on : 29.2778
Width : 2.909
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

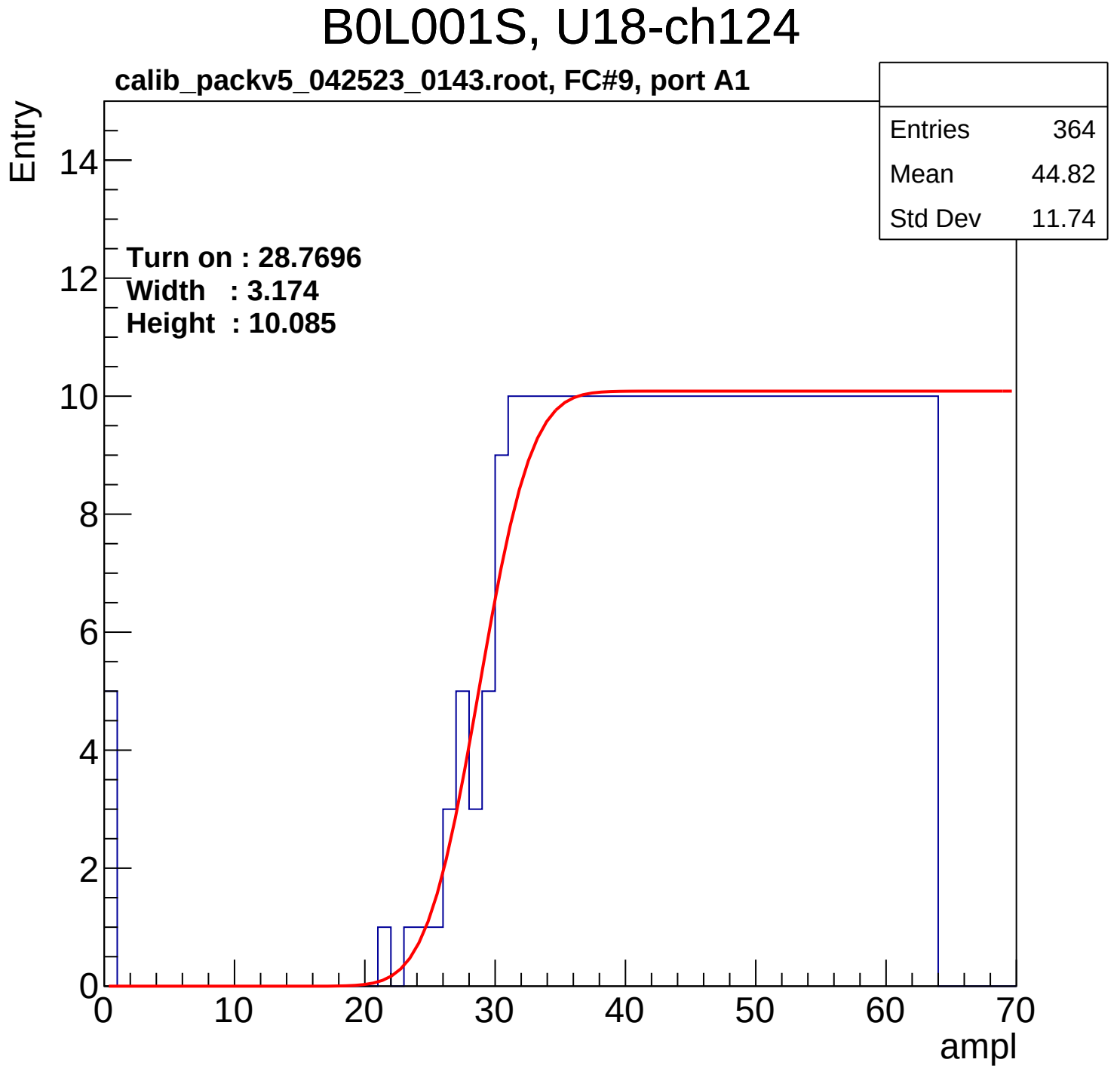

B0L001S, U18-ch119
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.57
Std Dev 11.7
Turn on : 27.6534
Width : 3.572
Height : 10.063
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

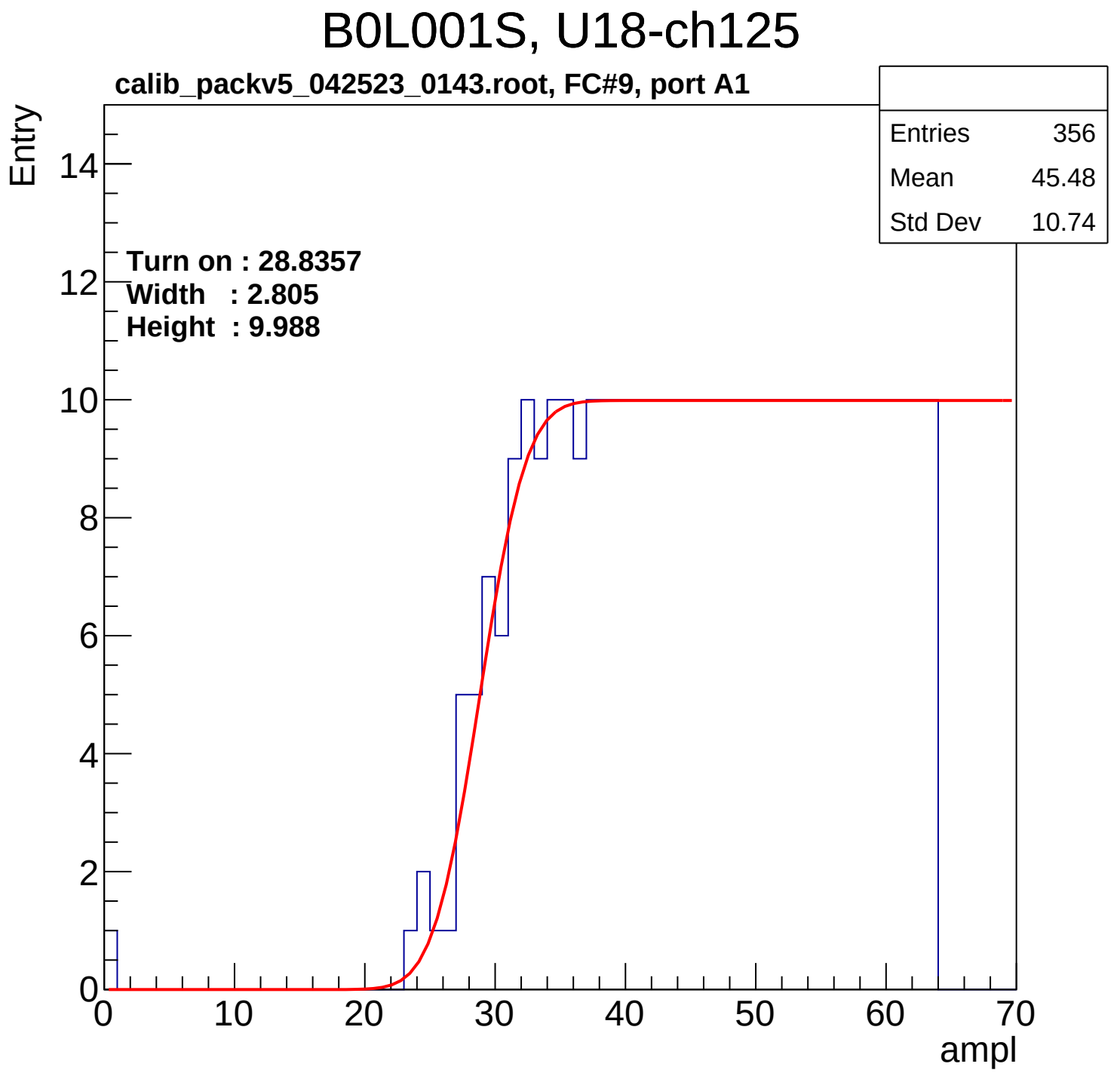

B0L001S, U18-ch120
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.67
Std Dev 11.84
Turn on : 27.8887
Width : 3.883
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

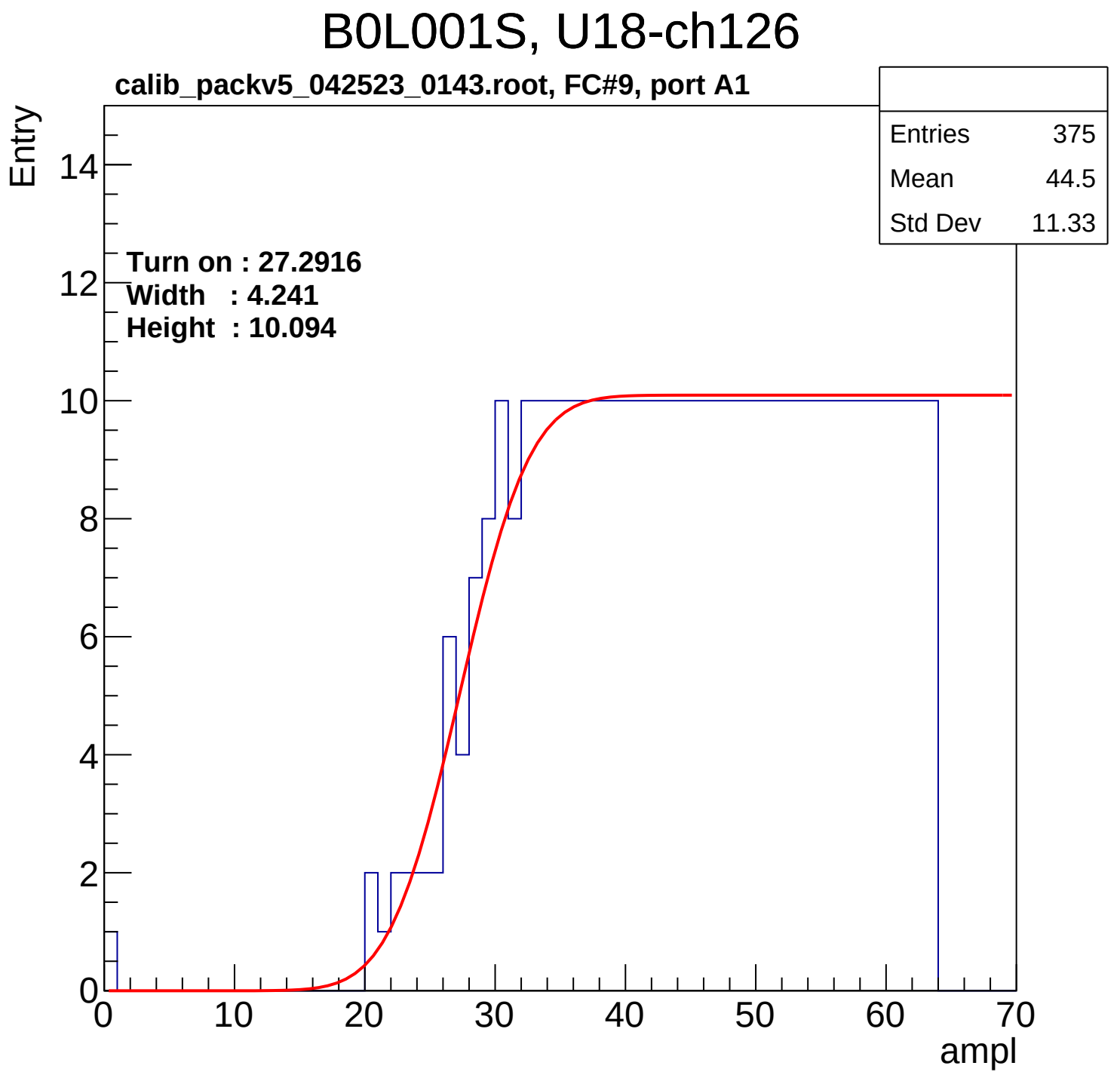

B0L001S, U18-ch121
calib_packv5_042523_0143.root, FC#9, port A1
Entries 382
Mean 44.01
Std Dev 11.95
Turn on : 26.3221
Width : 3.117
Height : 10.003
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

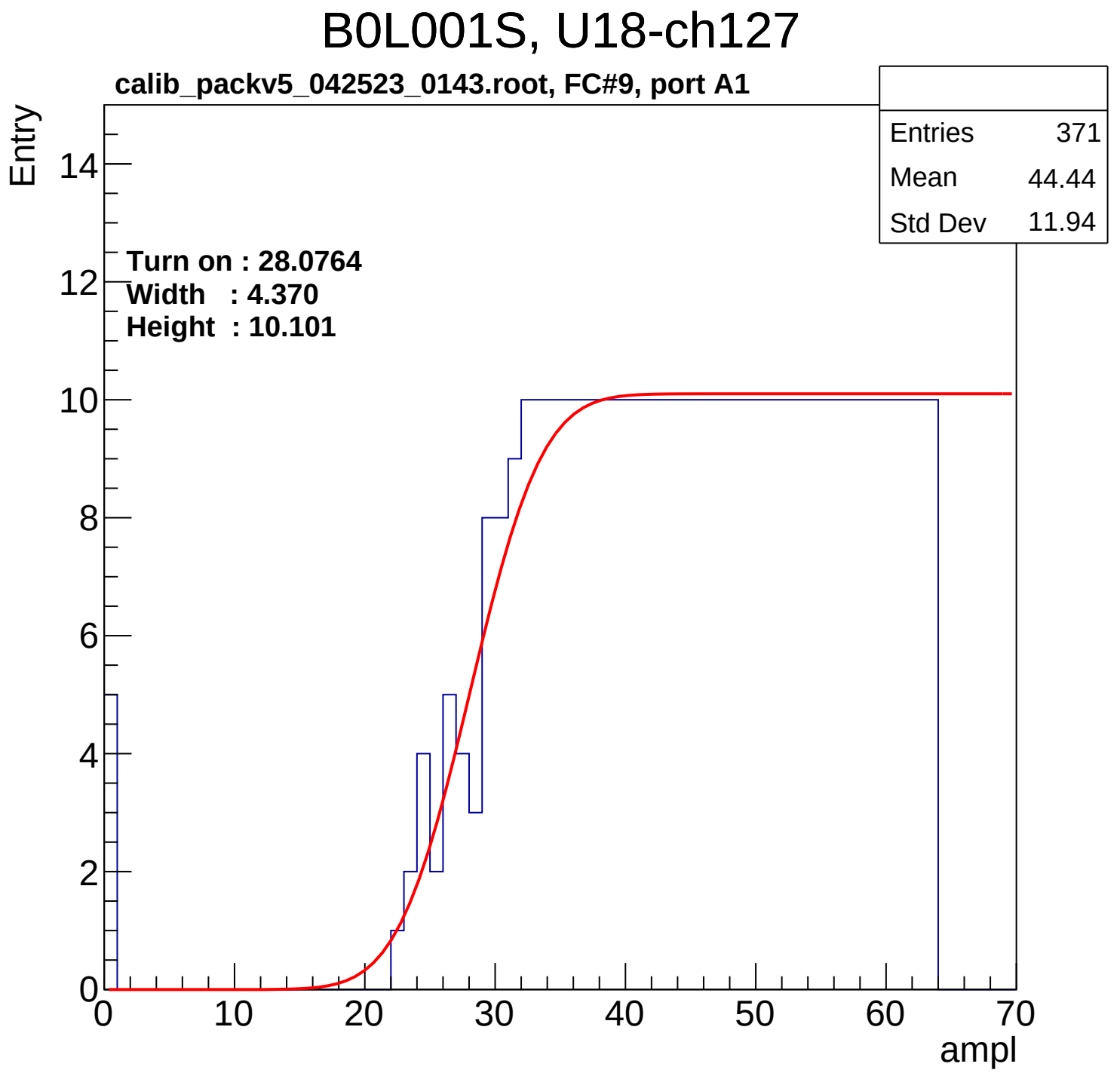

B0L001S, U18-ch122
calib_packv5_042523_0143.root, FC#9, port A1
Entries 391
Mean 43.51
Std Dev 12.34
Turn on : 26.6169
Width : 2.346
Height : 10.071
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

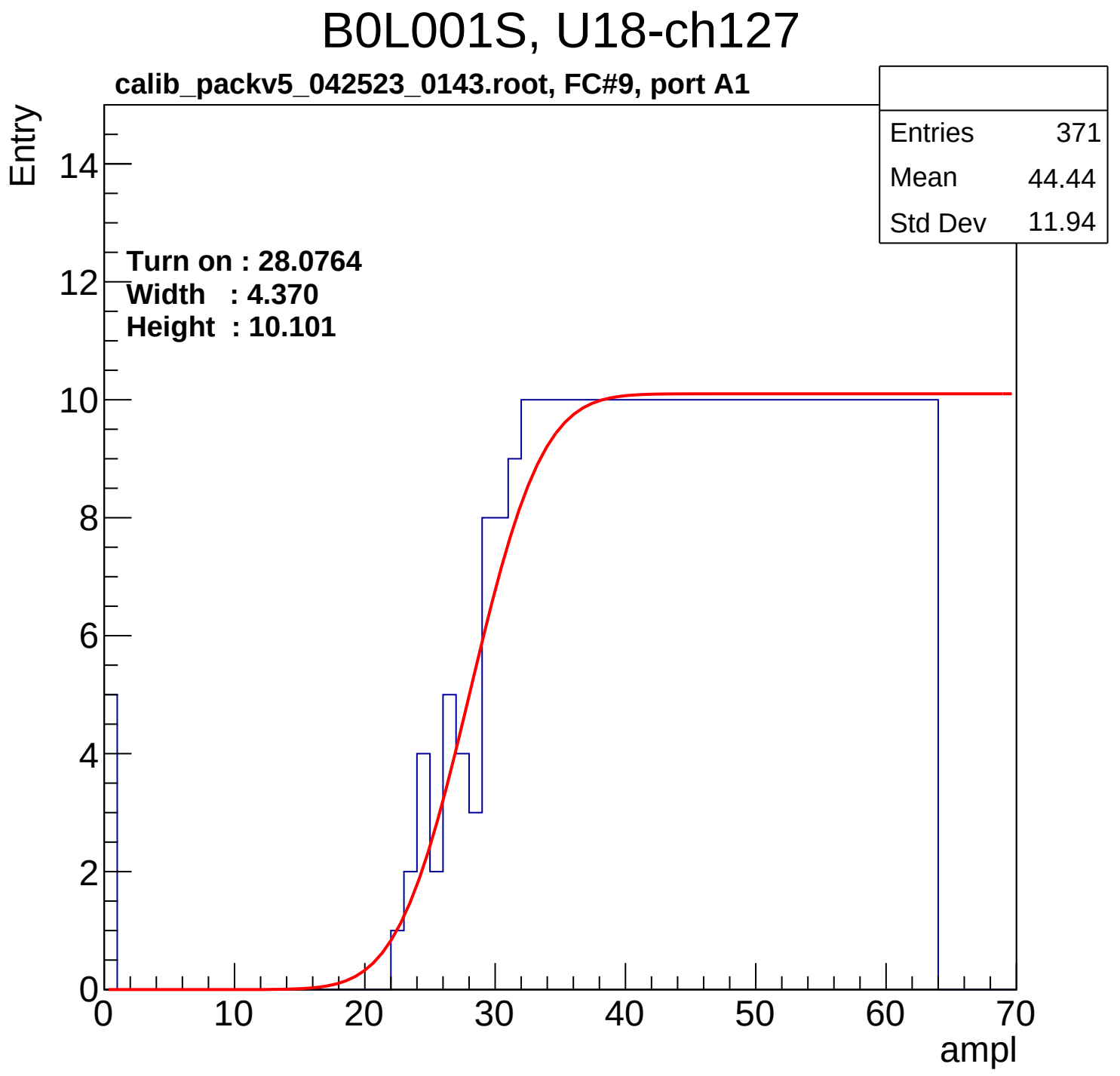

B0L001S, U18-ch123
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.41
Std Dev 11.85
Turn on : 27.5904
Width : 3.902
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U18-ch124
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.82
Std Dev 11.74
Turn on : 28.7696
Width : 3.174
Height : 10.085
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U18-ch125
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.48
Std Dev 10.74
Turn on : 28.8357
Width : 2.805
Height : 9.988
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U18-ch126
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.5
Std Dev 11.33
Turn on : 27.2916
Width : 4.241
Height : 10.094
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U18-ch127
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.44
Std Dev 11.94
Turn on : 28.0764
Width : 4.370
Height : 10.101
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U18-ch127
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.44
Std Dev 11.94
Turn on : 28.0764
Width : 4.370
Height : 10.101
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70