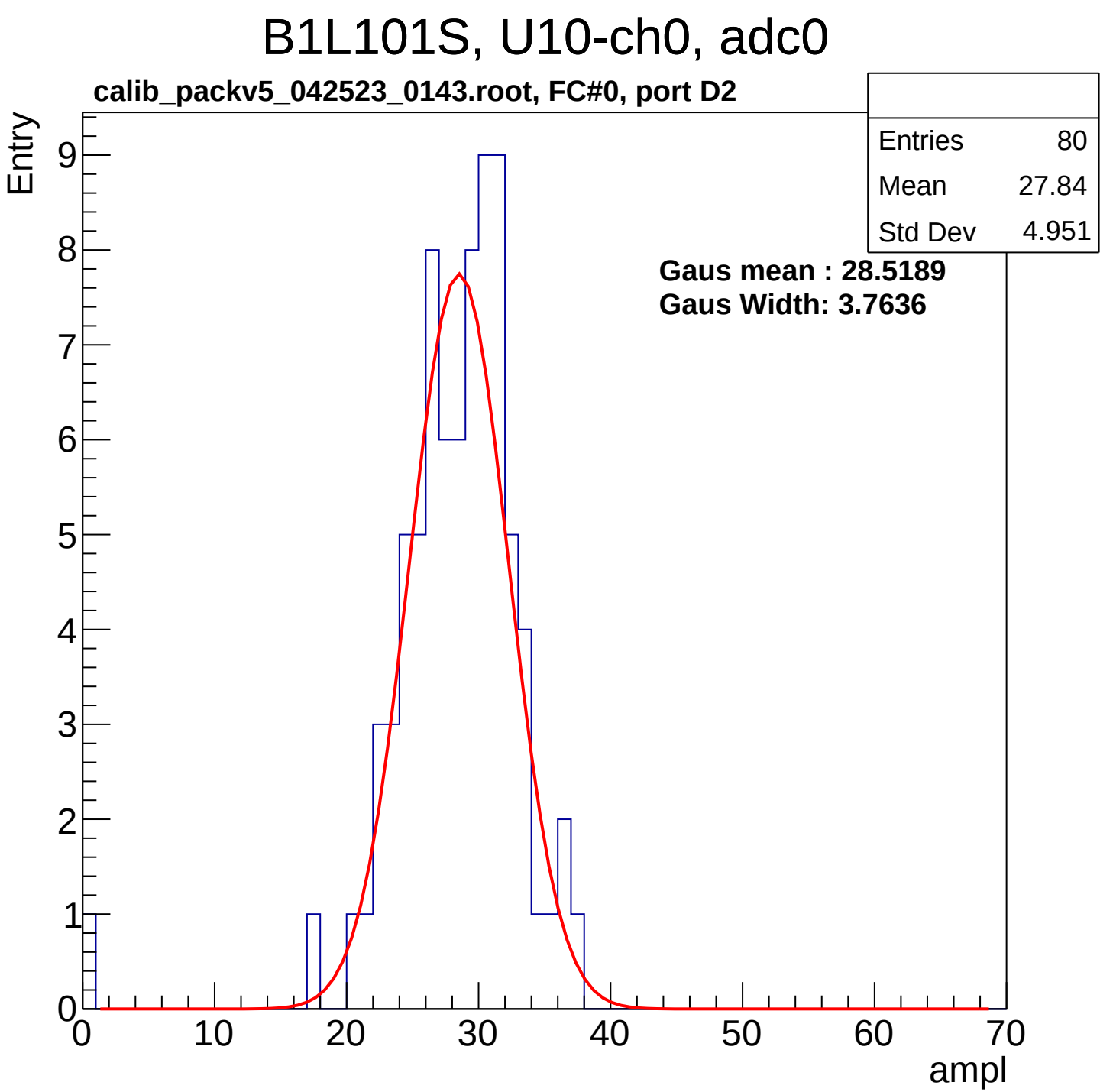
B1L101S, U10-ch0, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 80
Mean 27.84
Std Dev 4.951
Gaus mean : 28.5189
Gaus Width: 3.7636
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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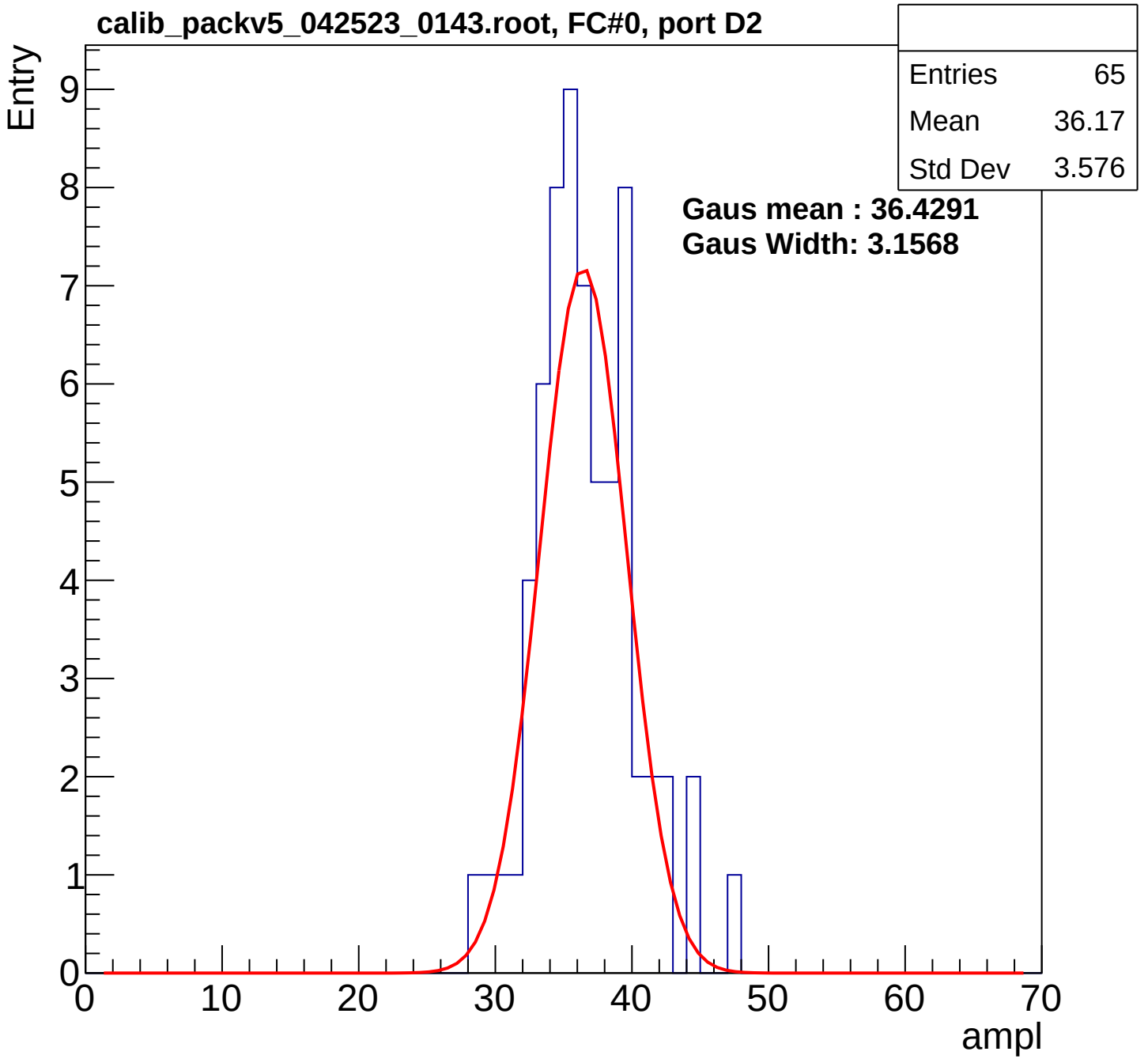
B1L101S, U10-ch0, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 36.17
Std Dev 3.576
Gaus mean : 36.4291
Gaus Width: 3.1568
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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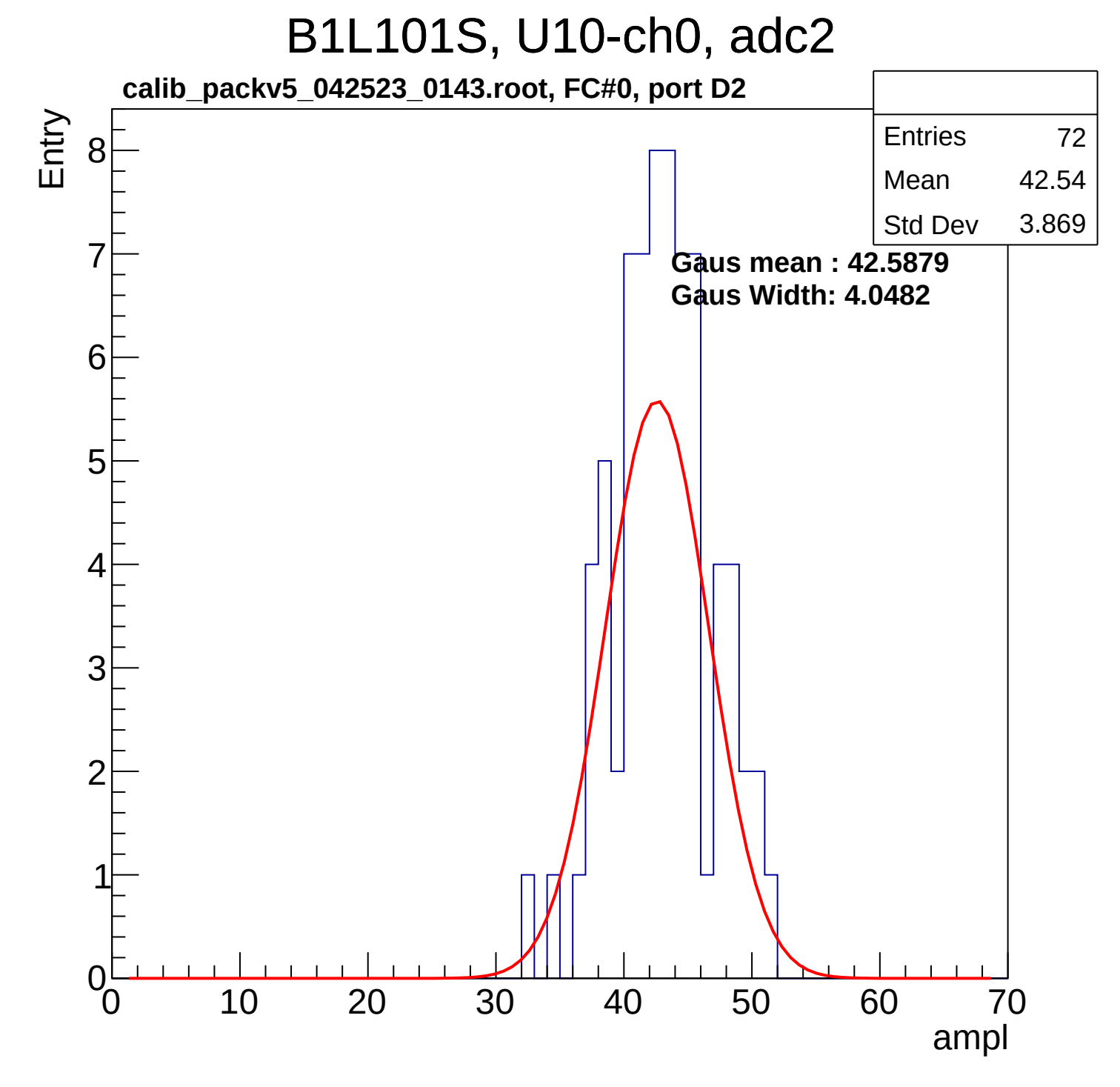
B1L101S, U10-ch0, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 42.54
Std Dev 3.869
Gaus mean : 42.5879
Gaus Width: 4.0482
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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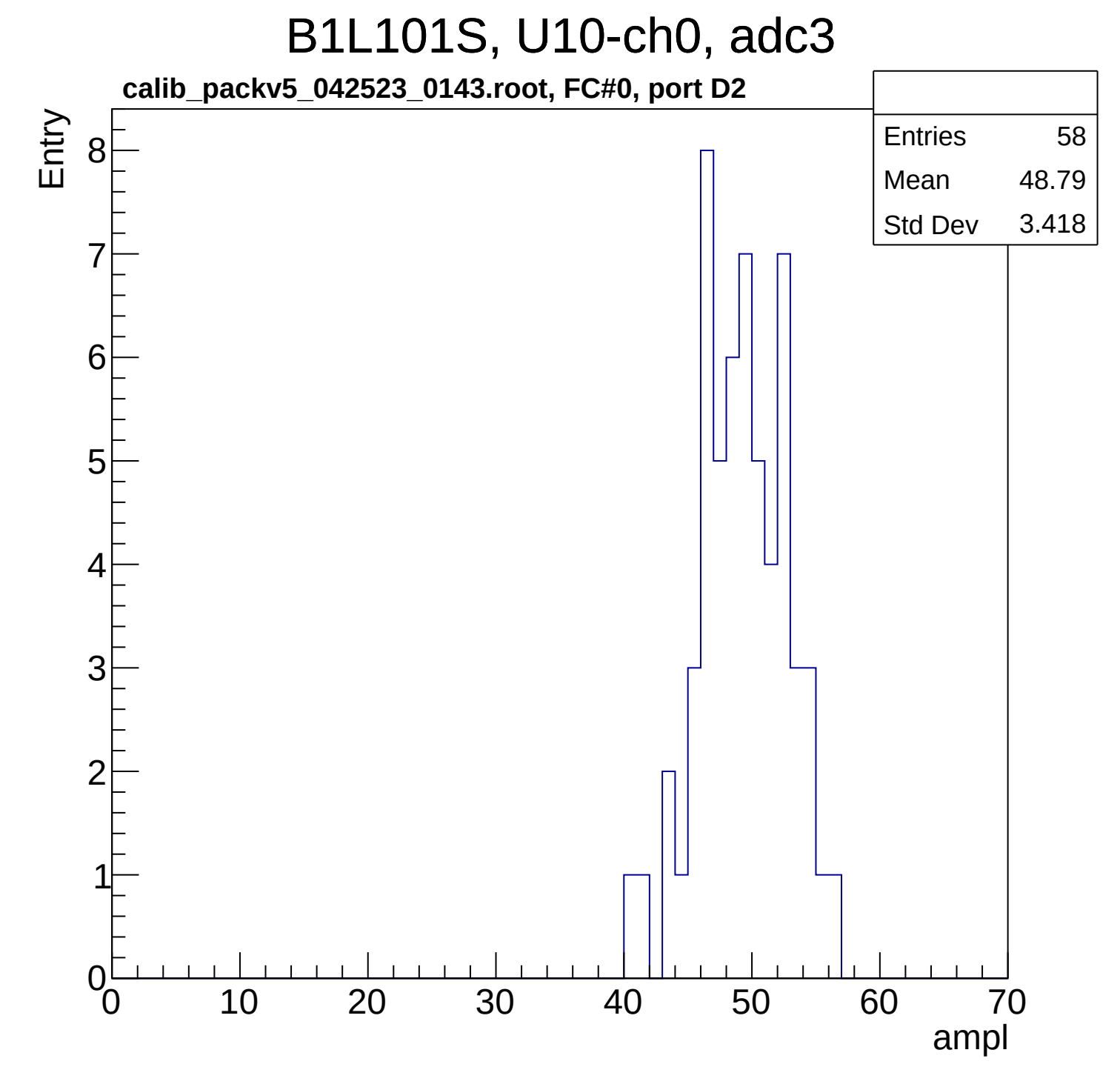
B1L101S, U10-ch0, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 48.79
Std Dev 3.418
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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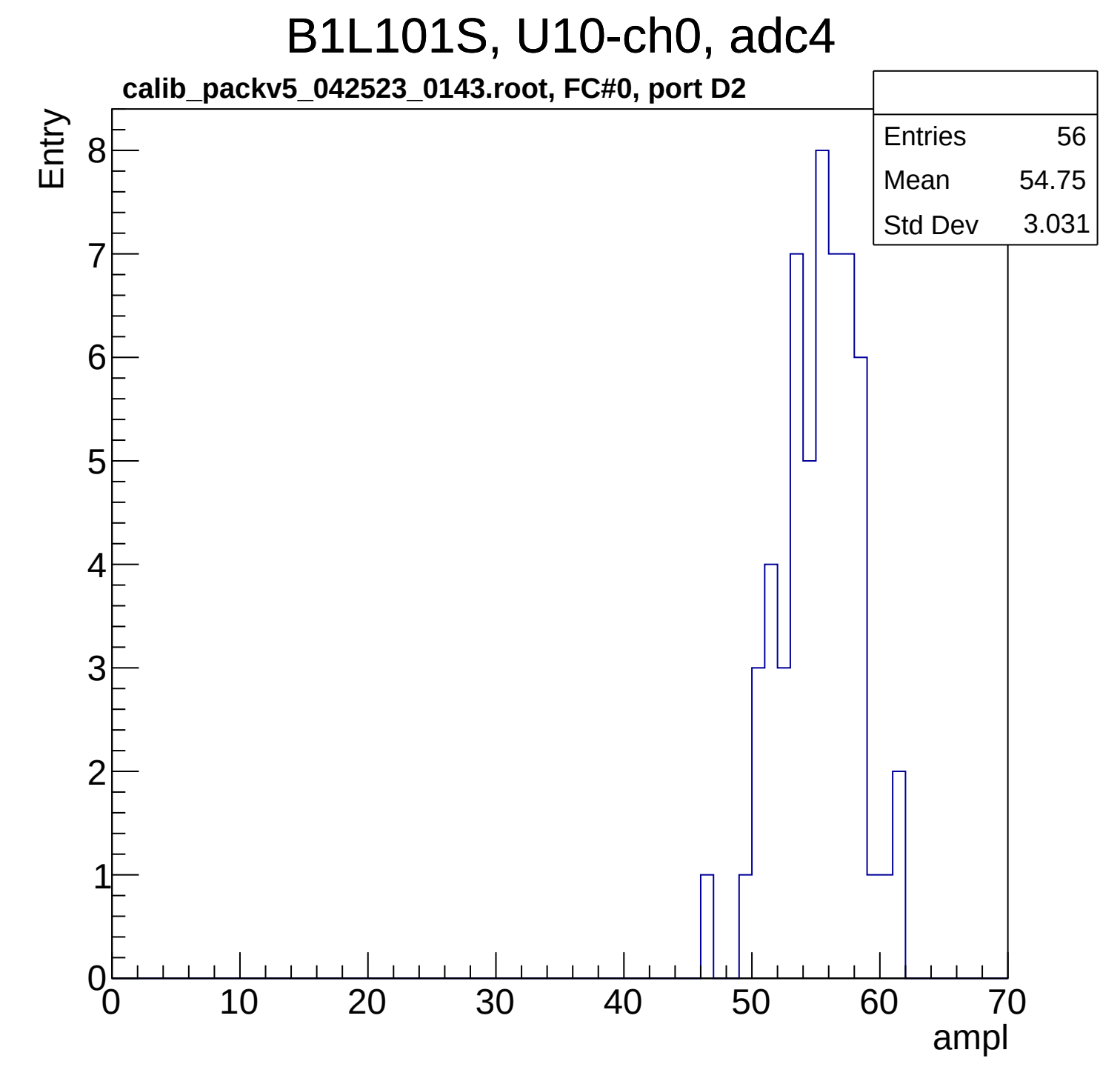
B1L101S, U10-ch0, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 54.75
Std Dev 3.031
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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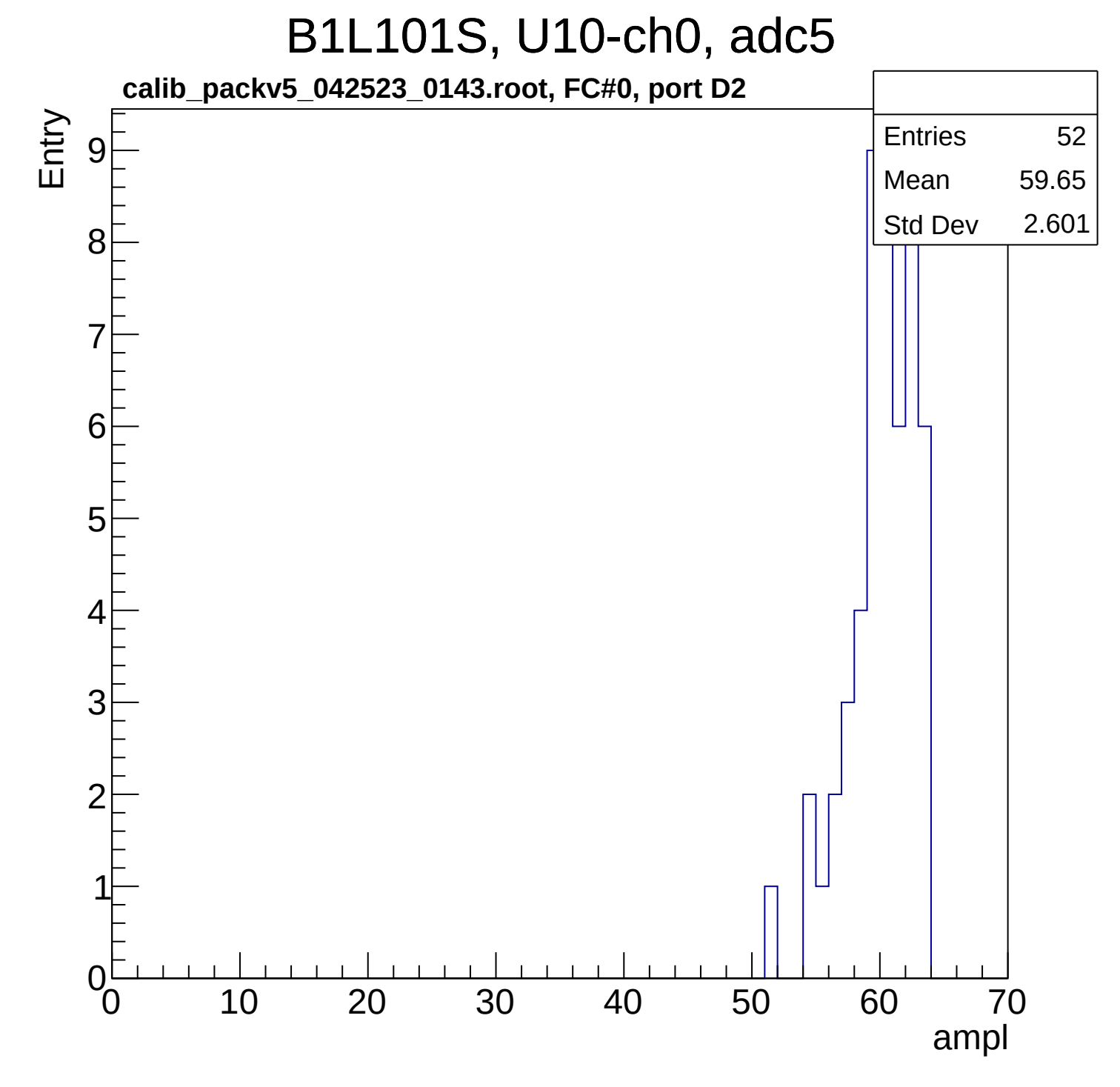
B1L101S, U10-ch0, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 59.65
Std Dev 2.601
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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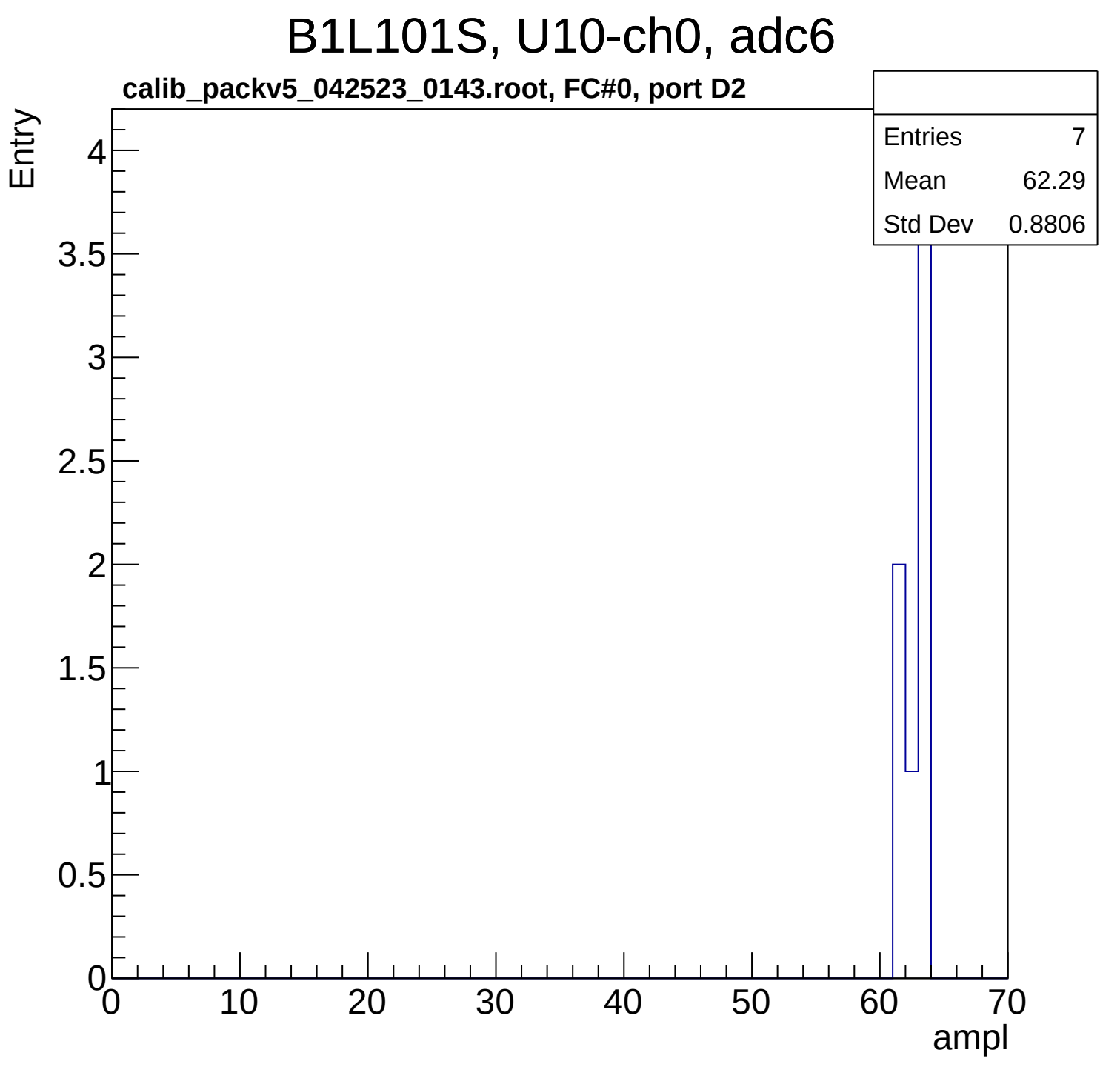
B1L101S, U10-ch0, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 62.29
Std Dev 0.8806
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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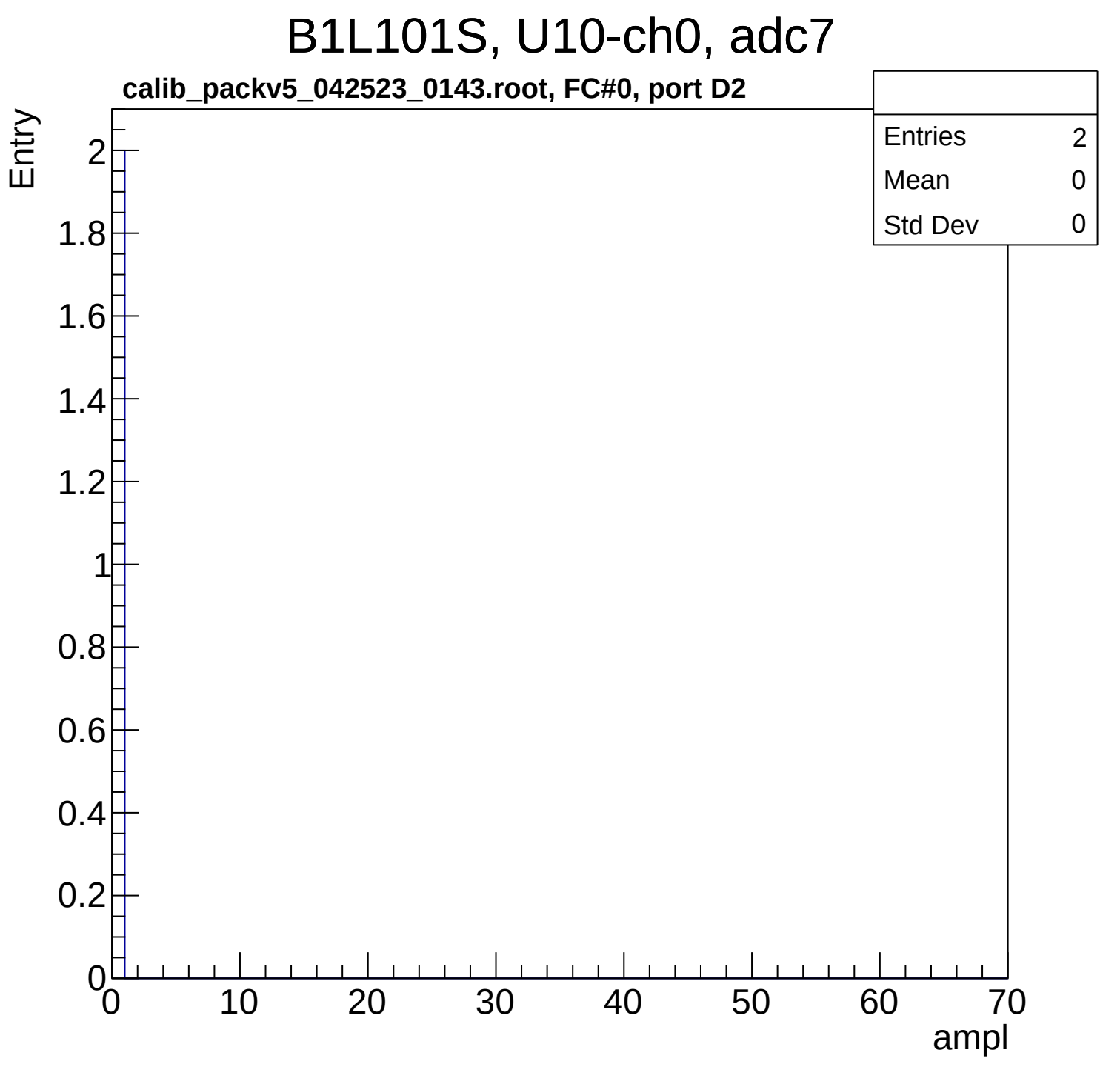
B1L101S, U10-ch0, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
50
60
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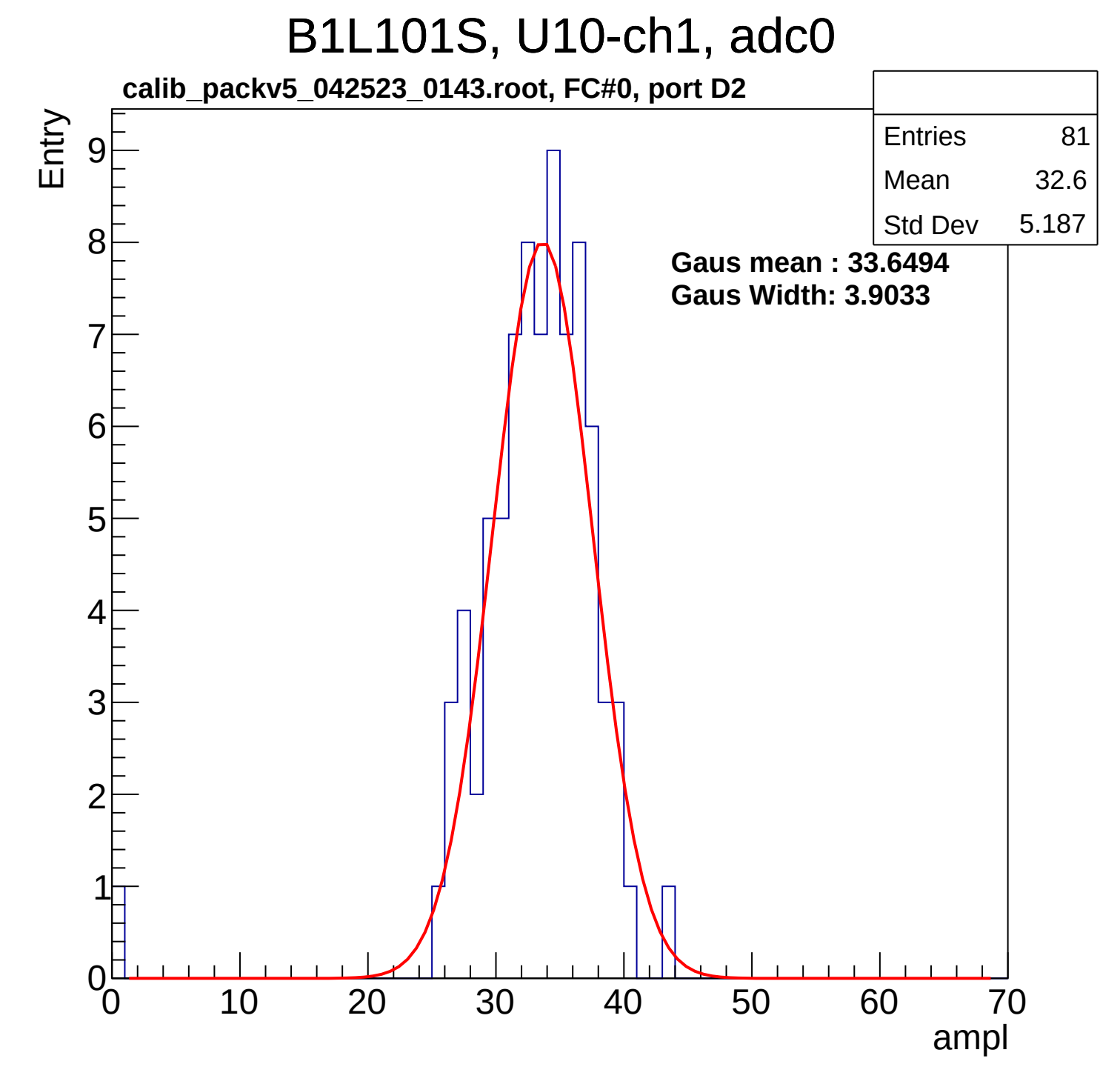
B1L101S, U10-ch1, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 81
Mean 32.6
Std Dev 5.187
Gaus mean : 33.6494
Gaus Width: 3.9033
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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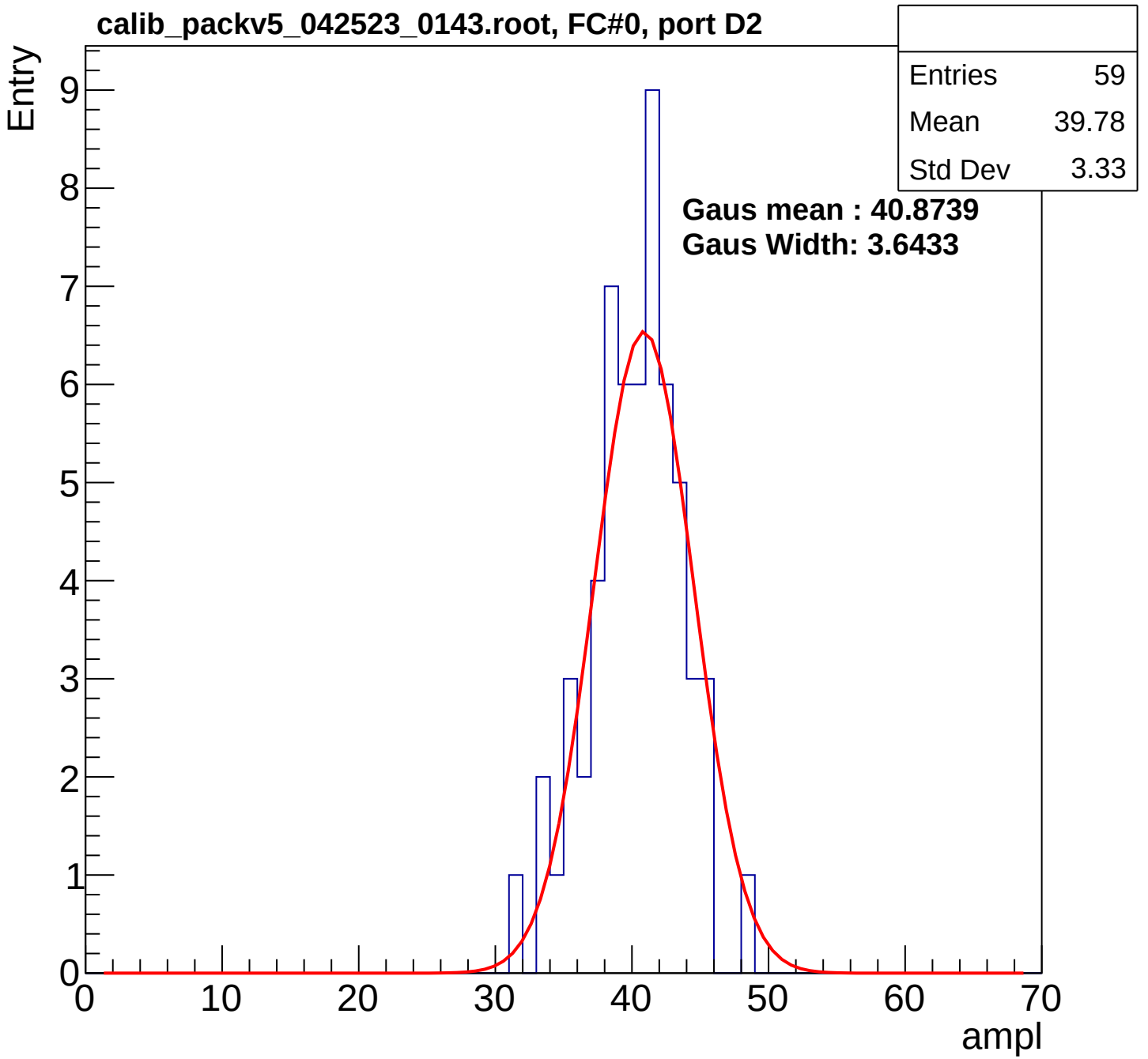
B1L101S, U10-ch1, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 39.78
Std Dev 3.33
Gaus mean : 40.8739
Gaus Width: 3.6433
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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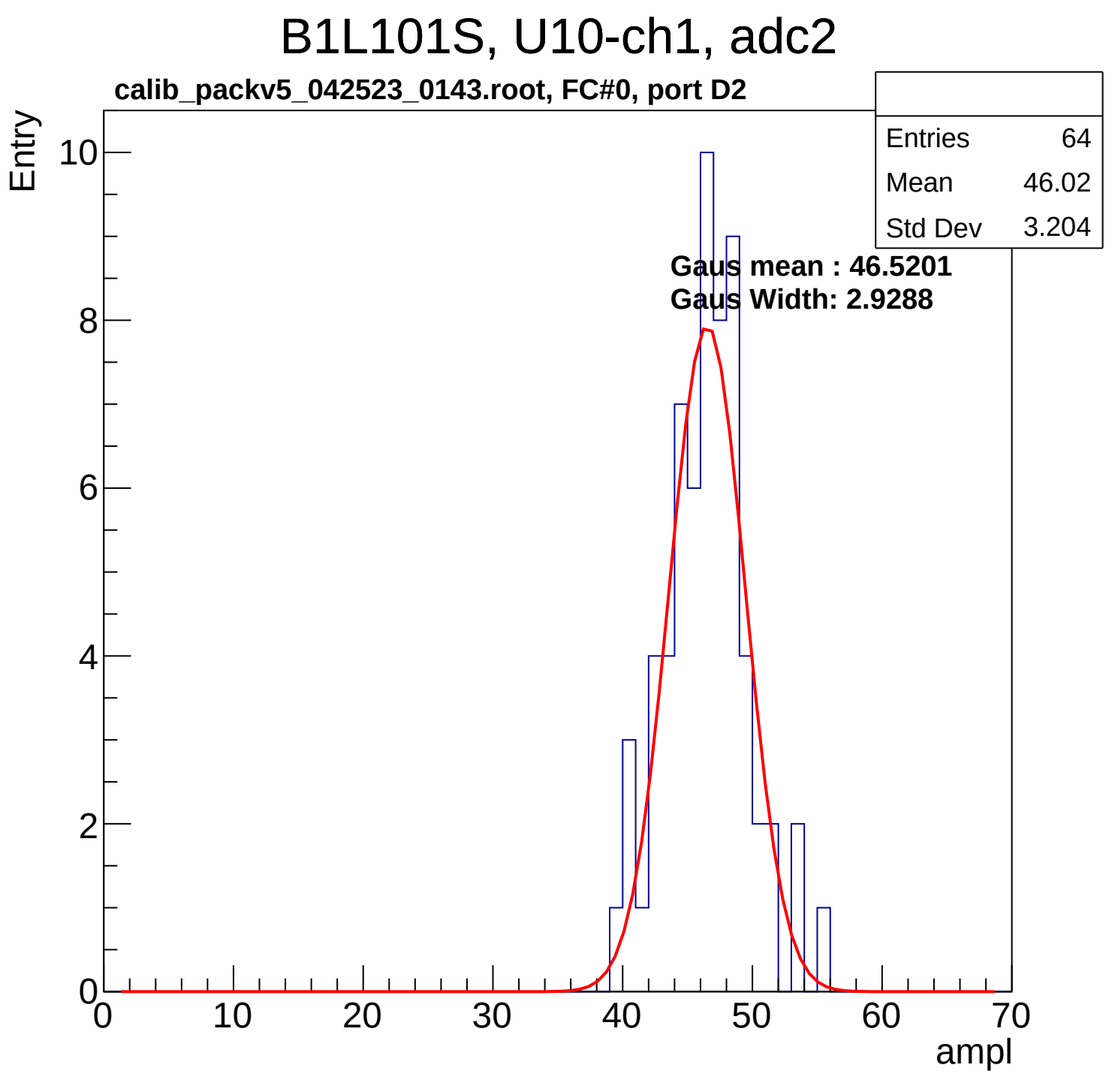
B1L101S, U10-ch1, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 46.02
Std Dev 3.204
Gaus mean : 46.5201
Gaus Width: 2.9288
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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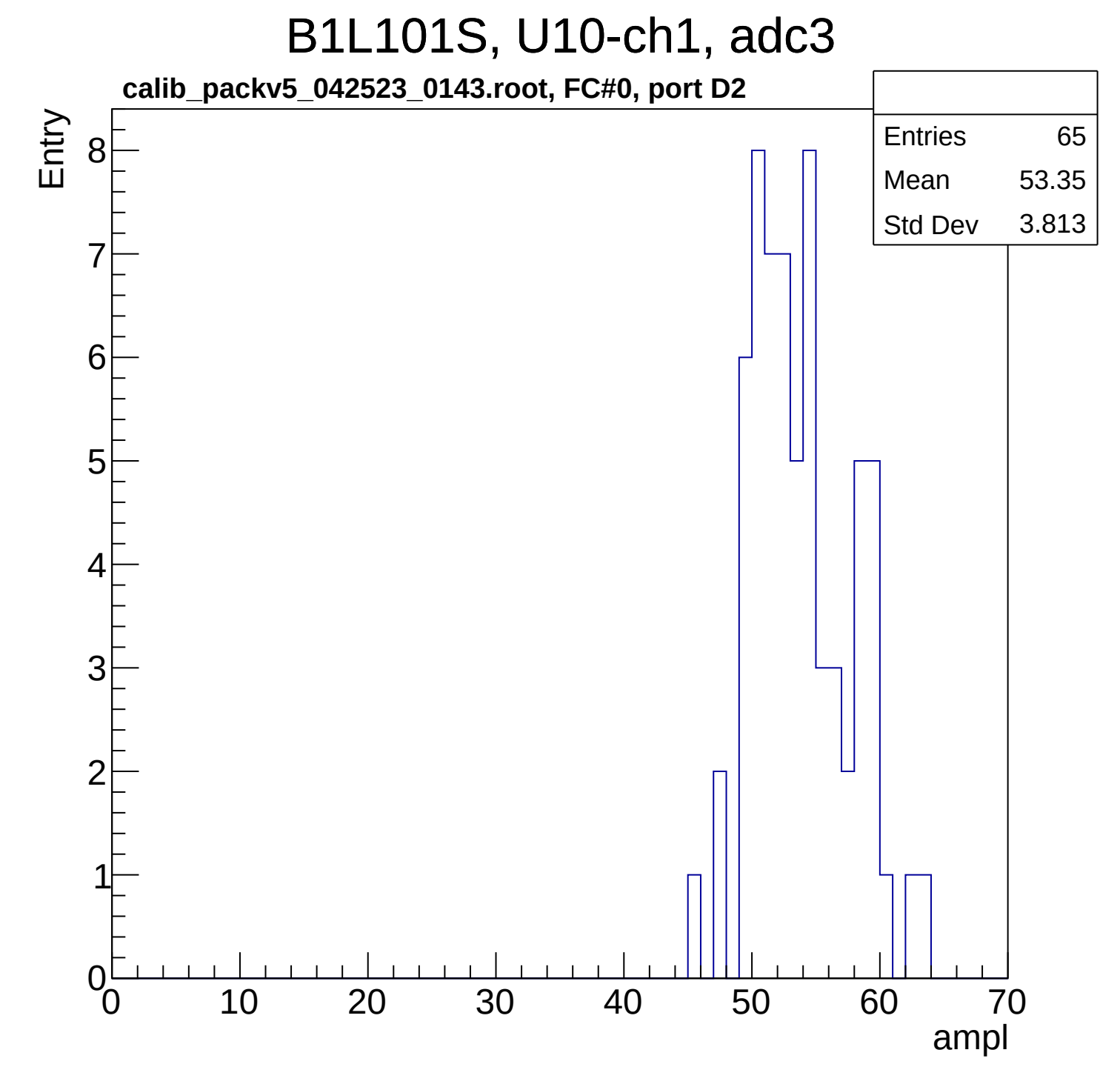
B1L101S, U10-ch1, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 53.35
Std Dev 3.813
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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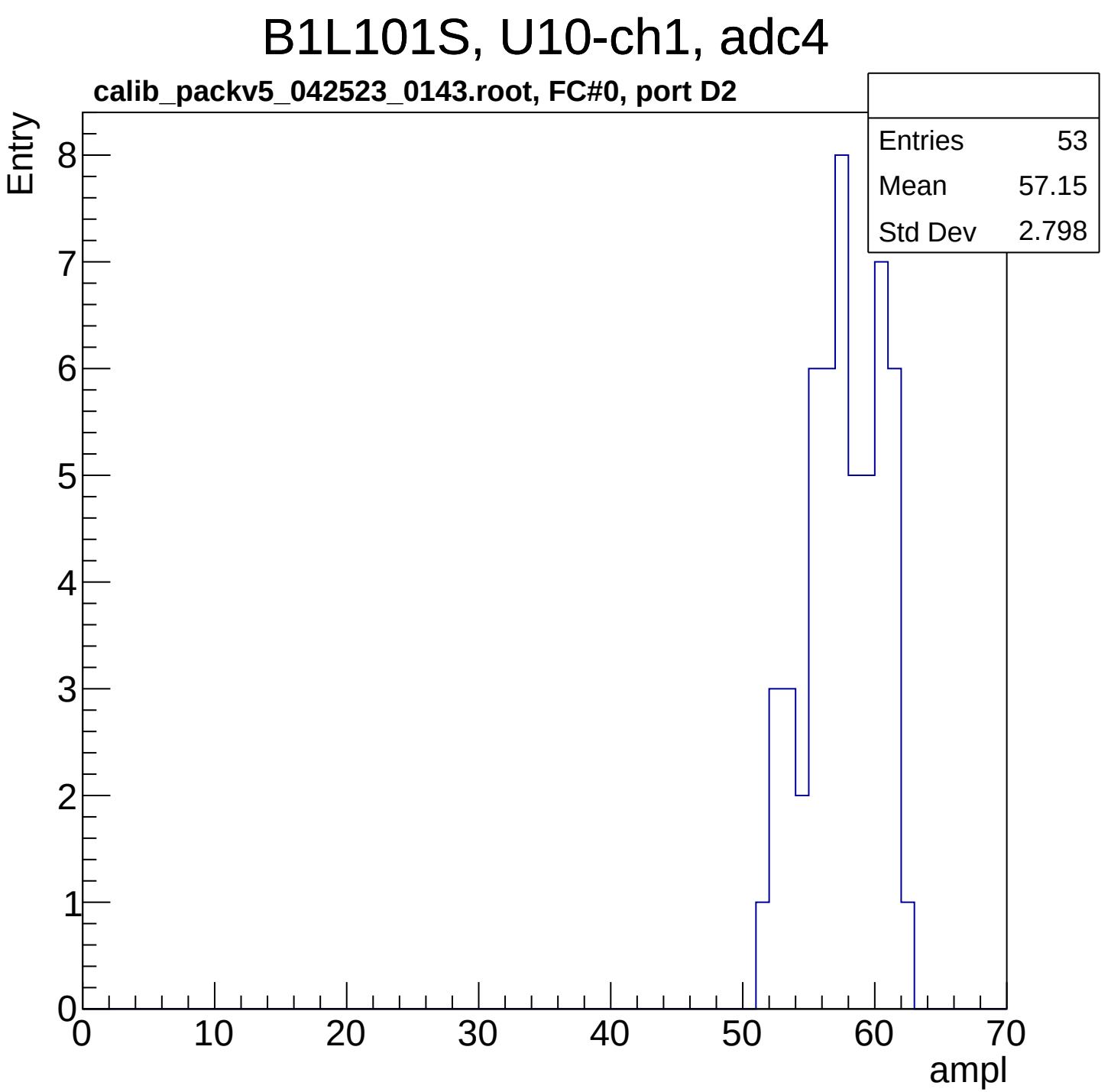
40
50
60
70


B1L101S, U10-ch1, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 57.15
Std Dev 2.798
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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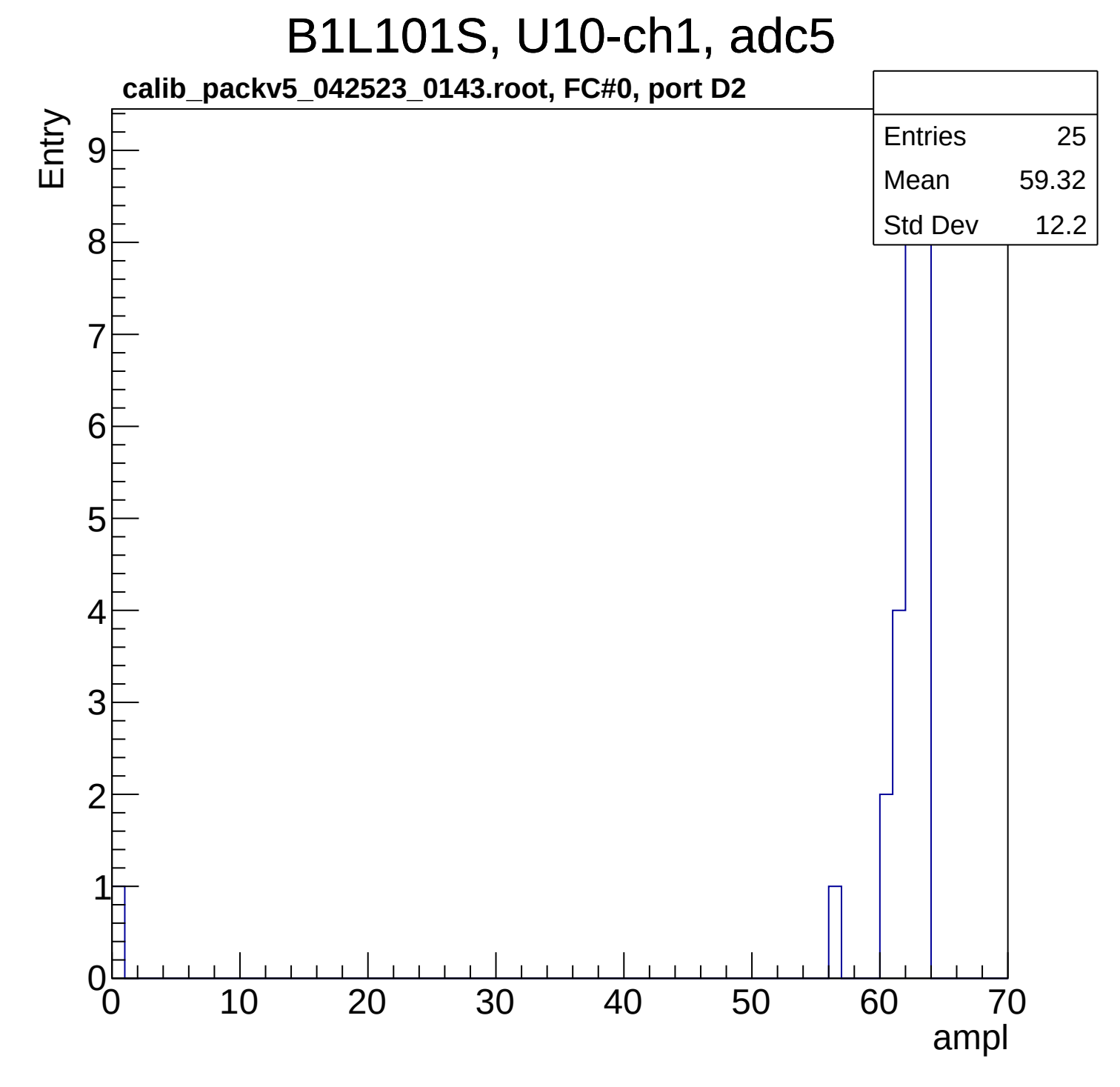
B1L101S, U10-ch1, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 25
Mean 59.32
Std Dev 12.2
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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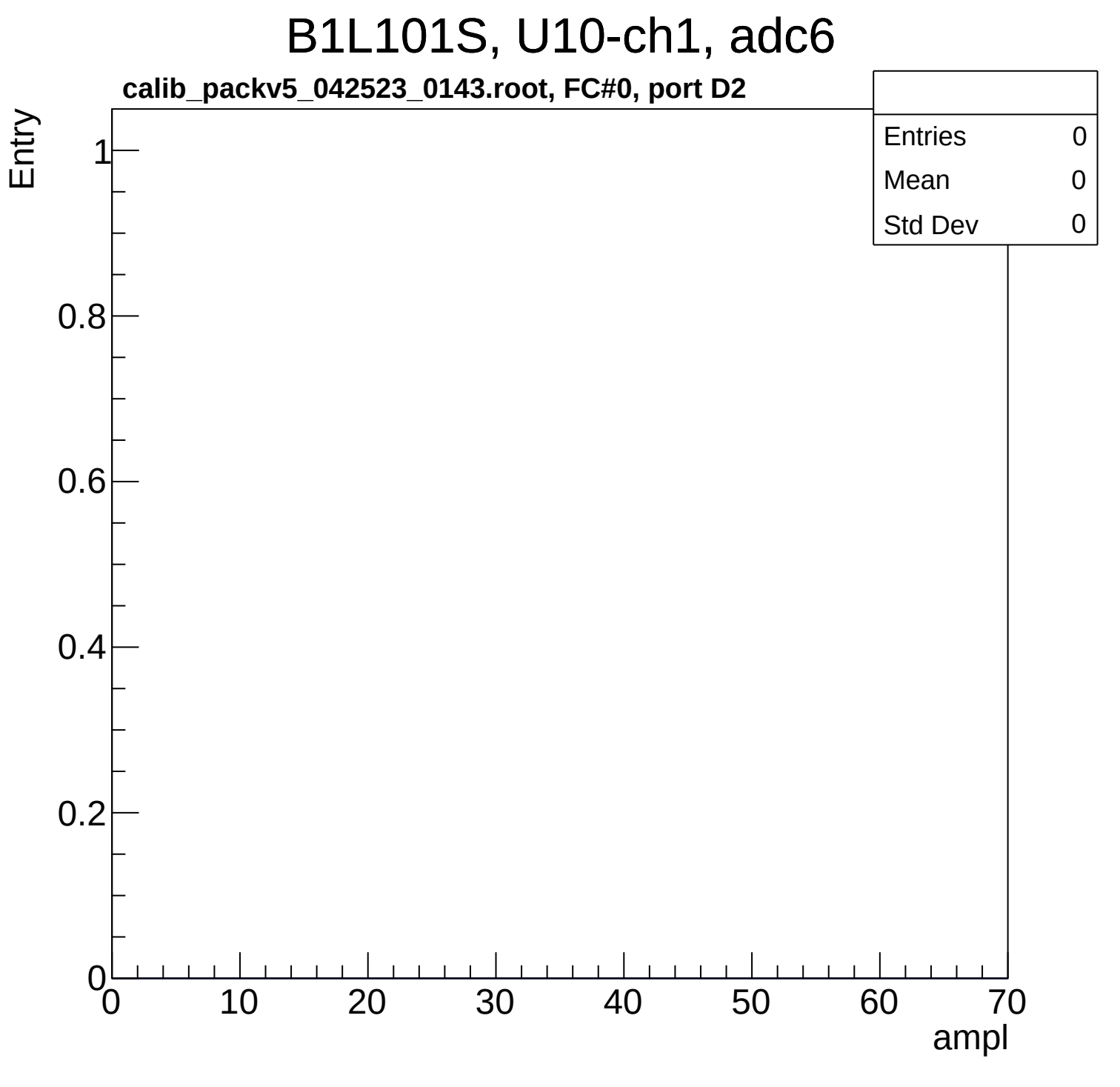
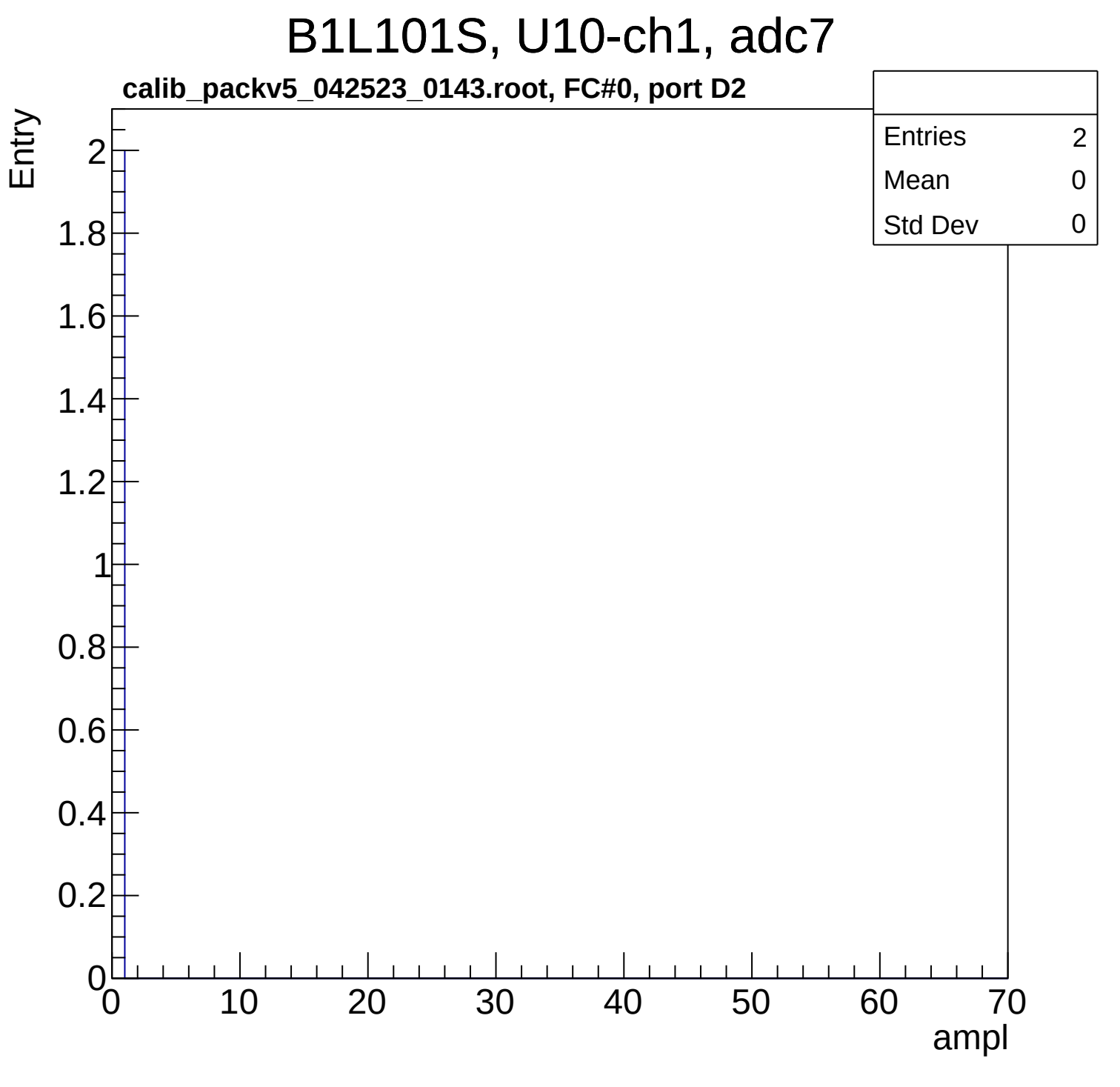

B1L101S, U10-ch1, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch1, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
50
60
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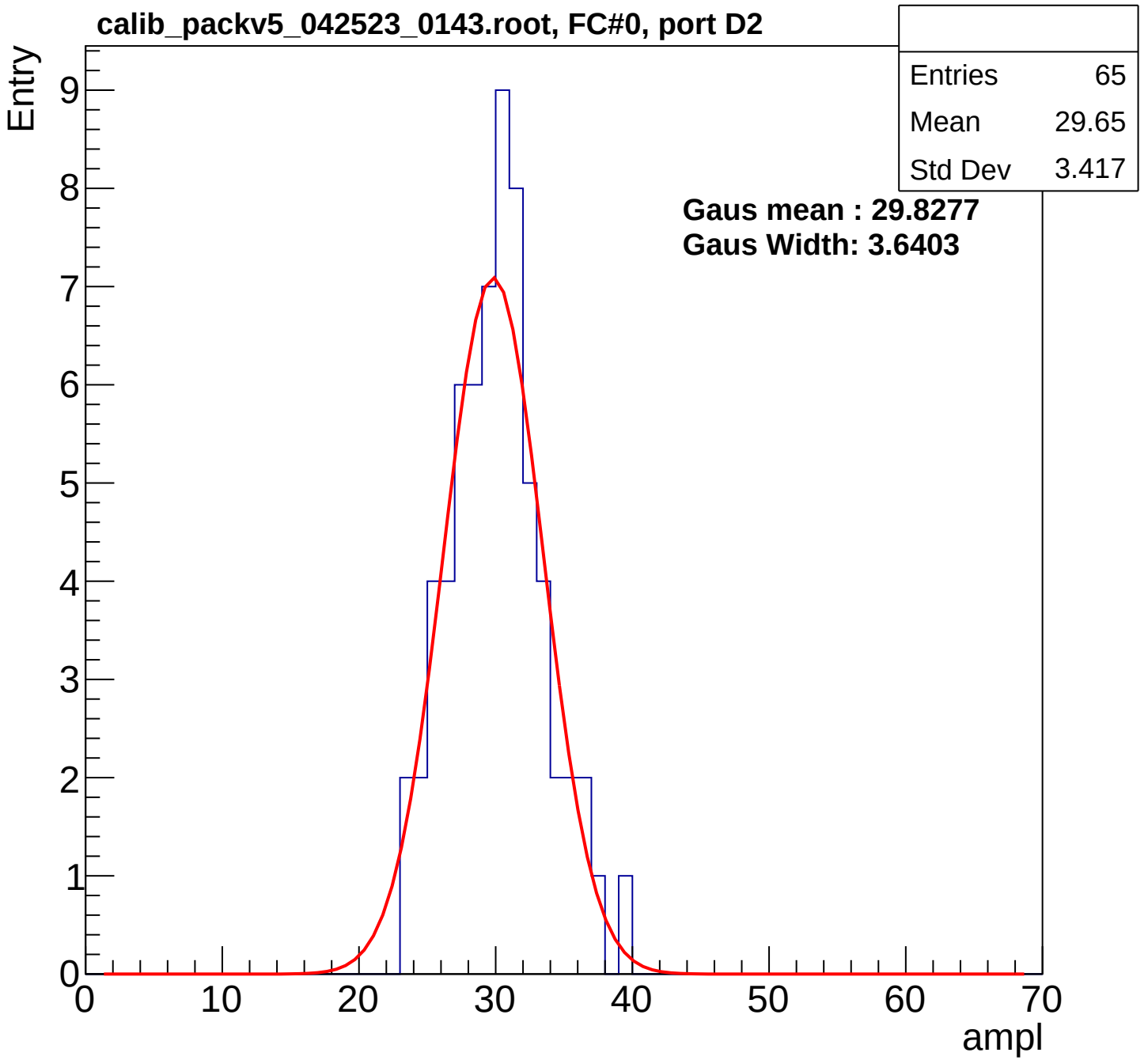
B1L101S, U10-ch2, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 29.65
Std Dev 3.417
Gaus mean : 29.8277
Gaus Width: 3.6403
Entry
ampl
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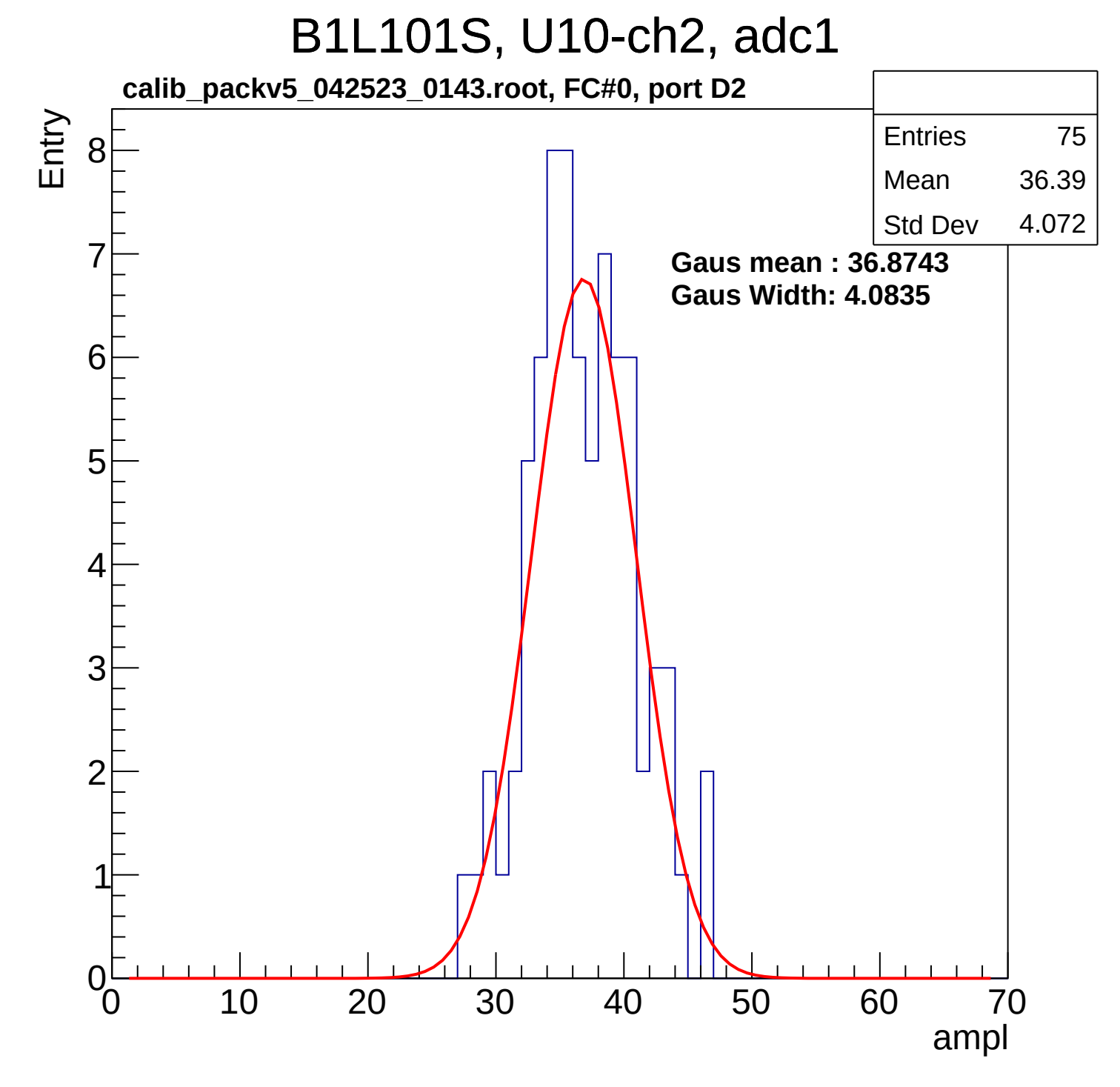
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch2, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 36.39
Std Dev 4.072
Gaus mean : 36.8743
Gaus Width: 4.0835
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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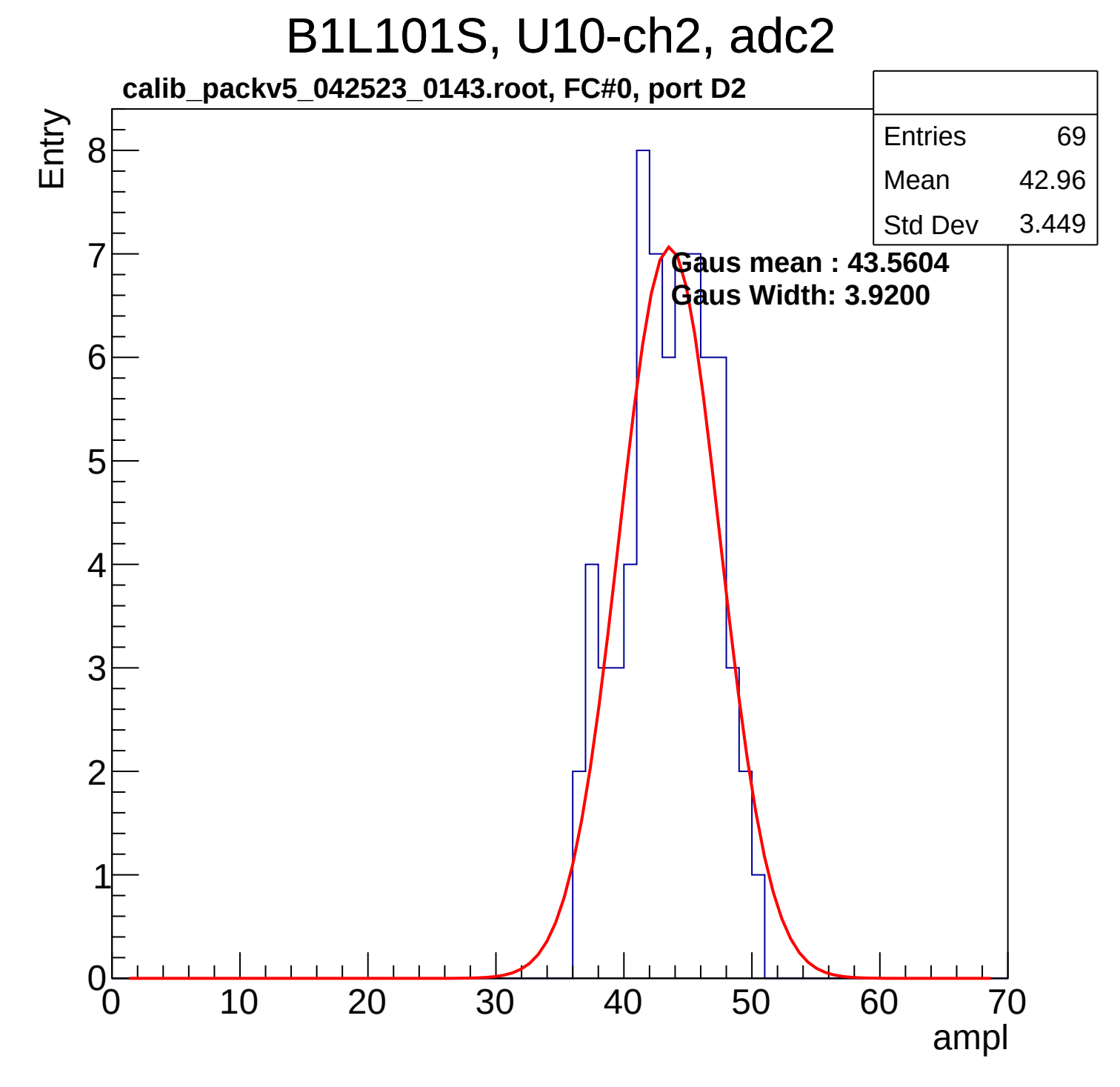
B1L101S, U10-ch2, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 42.96
Std Dev 3.449
Gaus mean : 43.5604
Gaus Width: 3.9200
Entry
ampl
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2
3
4
5
6
7
8
0
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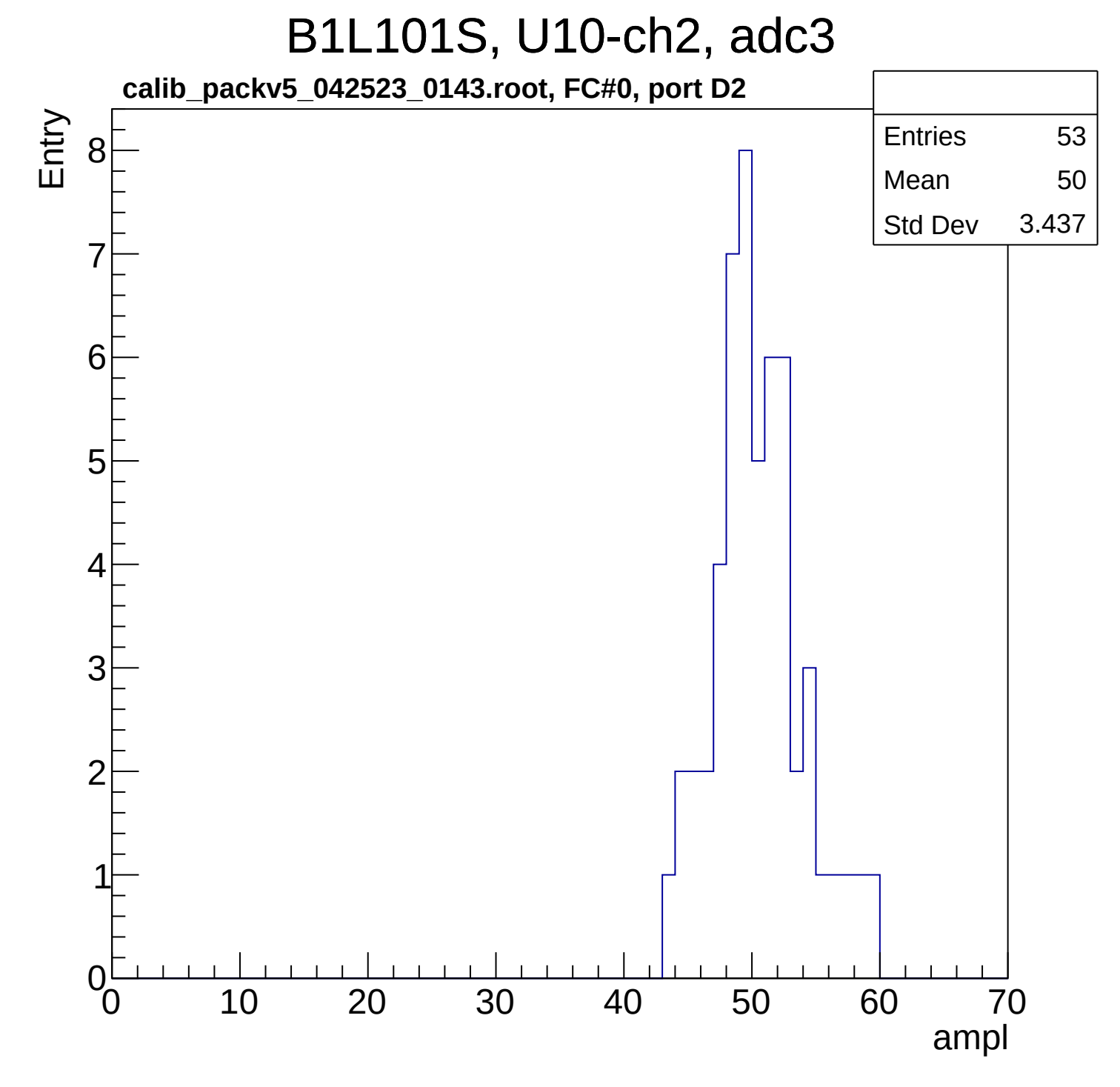
B1L101S, U10-ch2, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 50
Std Dev 3.437
Entry
ampl
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5
6
7
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0
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60
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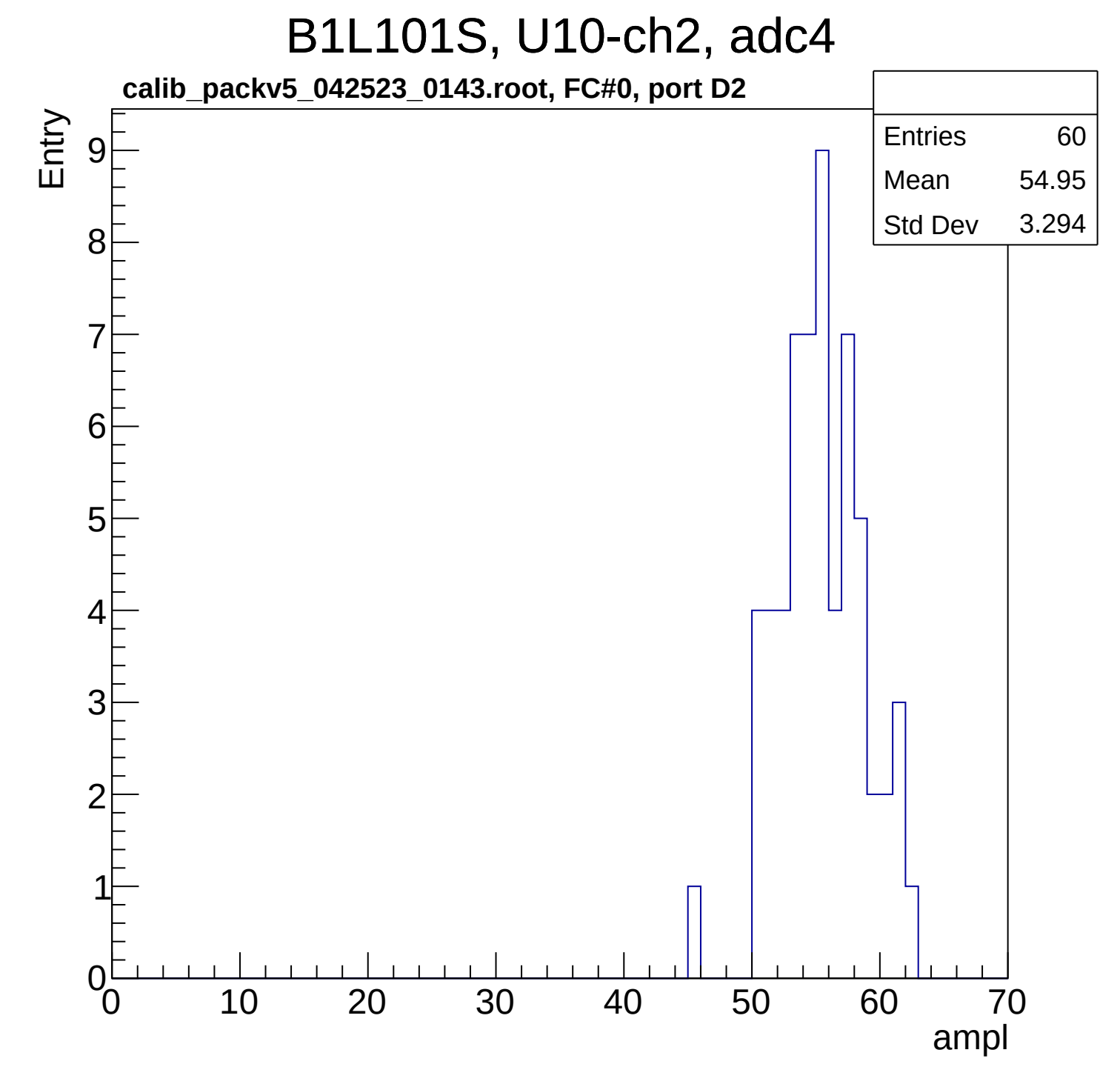
B1L101S, U10-ch2, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 54.95
Std Dev 3.294
Entry
ampl
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3
4
5
6
7
8
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0
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60
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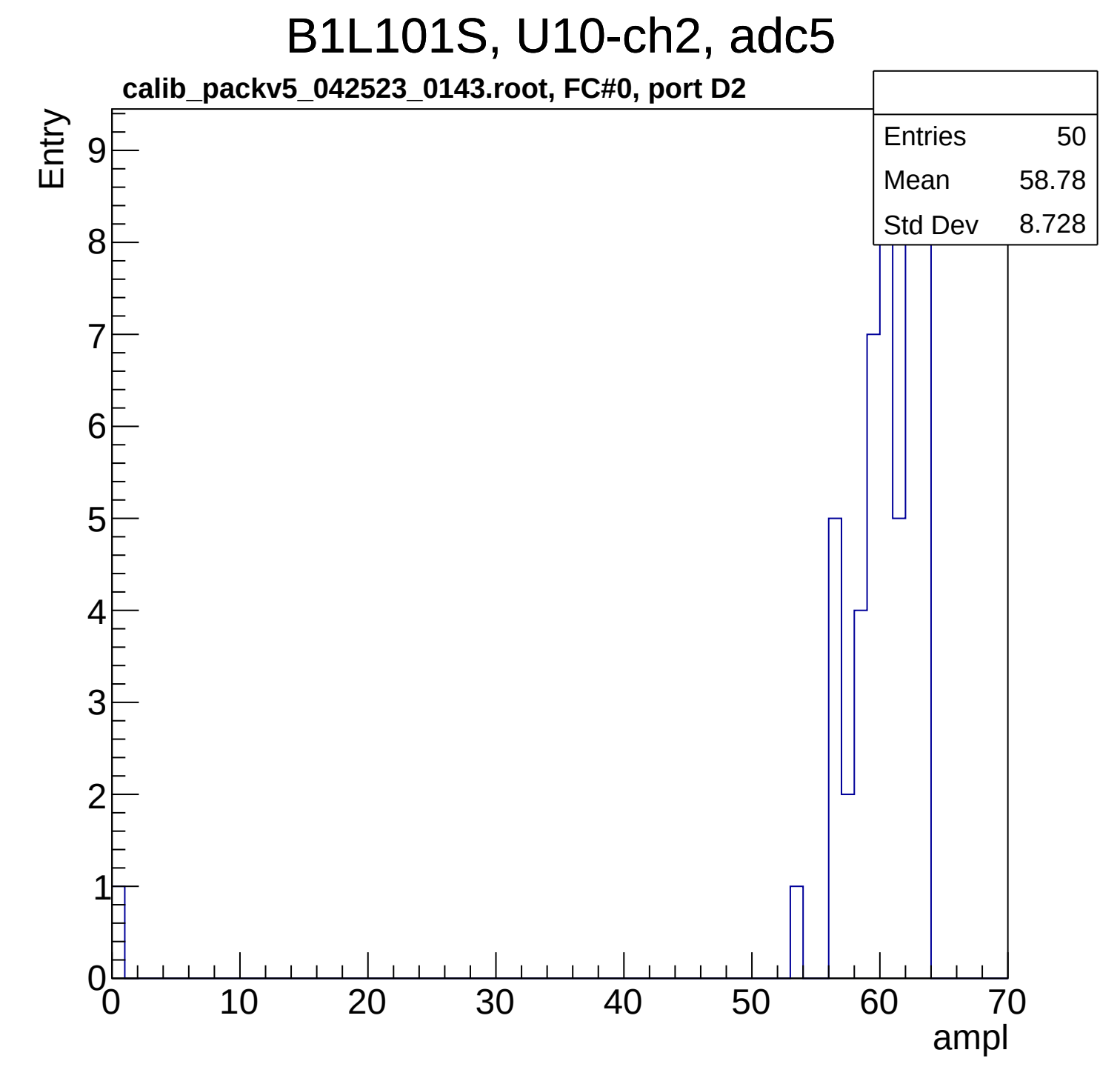
B1L101S, U10-ch2, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 58.78
Std Dev 8.728
Entry
ampl
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4
5
6
7
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0
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60
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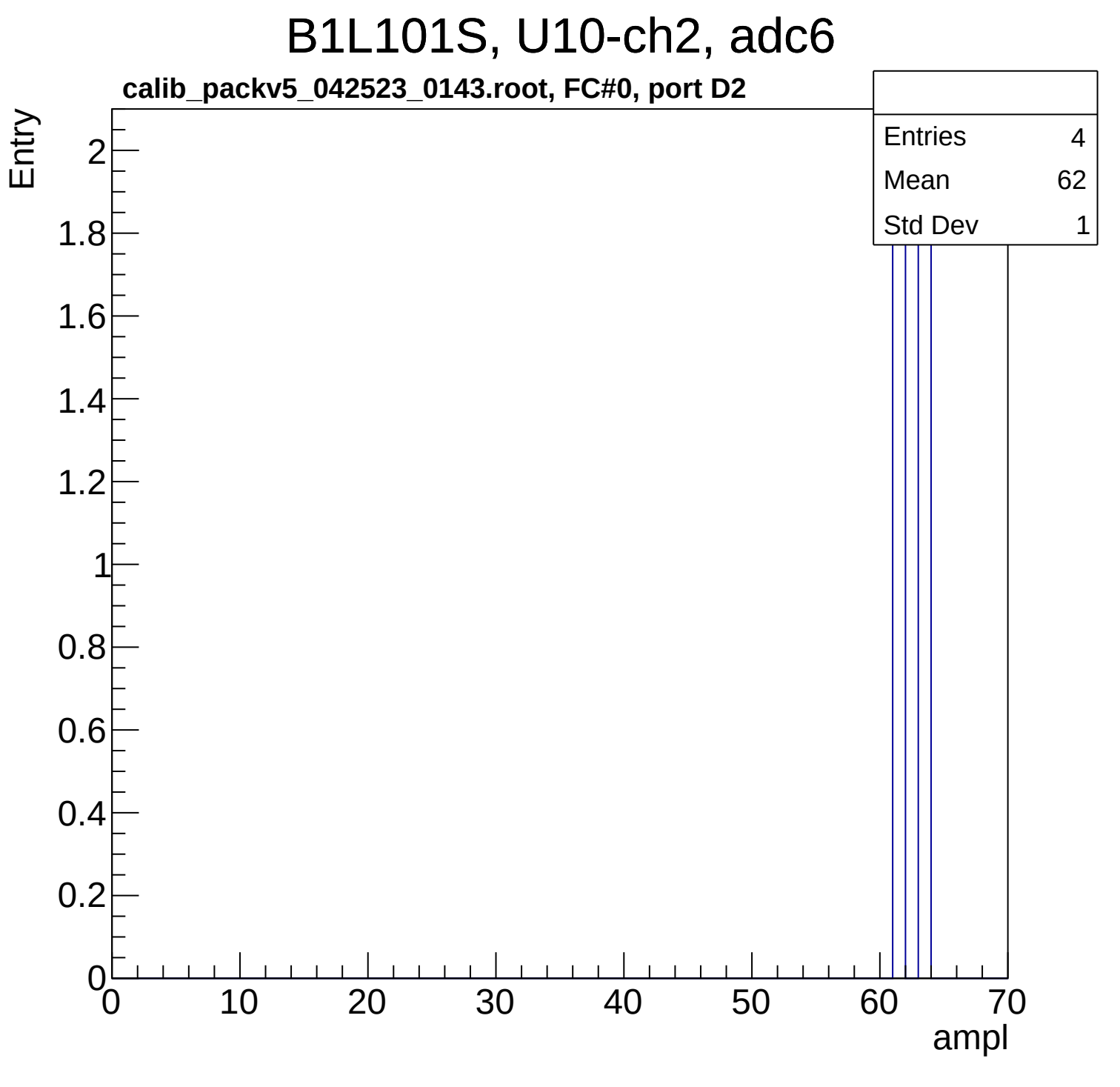
B1L101S, U10-ch2, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 62
Std Dev 1
Entry
ampl
0
0.2
0.4
0.6
0.8
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1.2
1.4
1.6
1.8
2
0
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40
50
60
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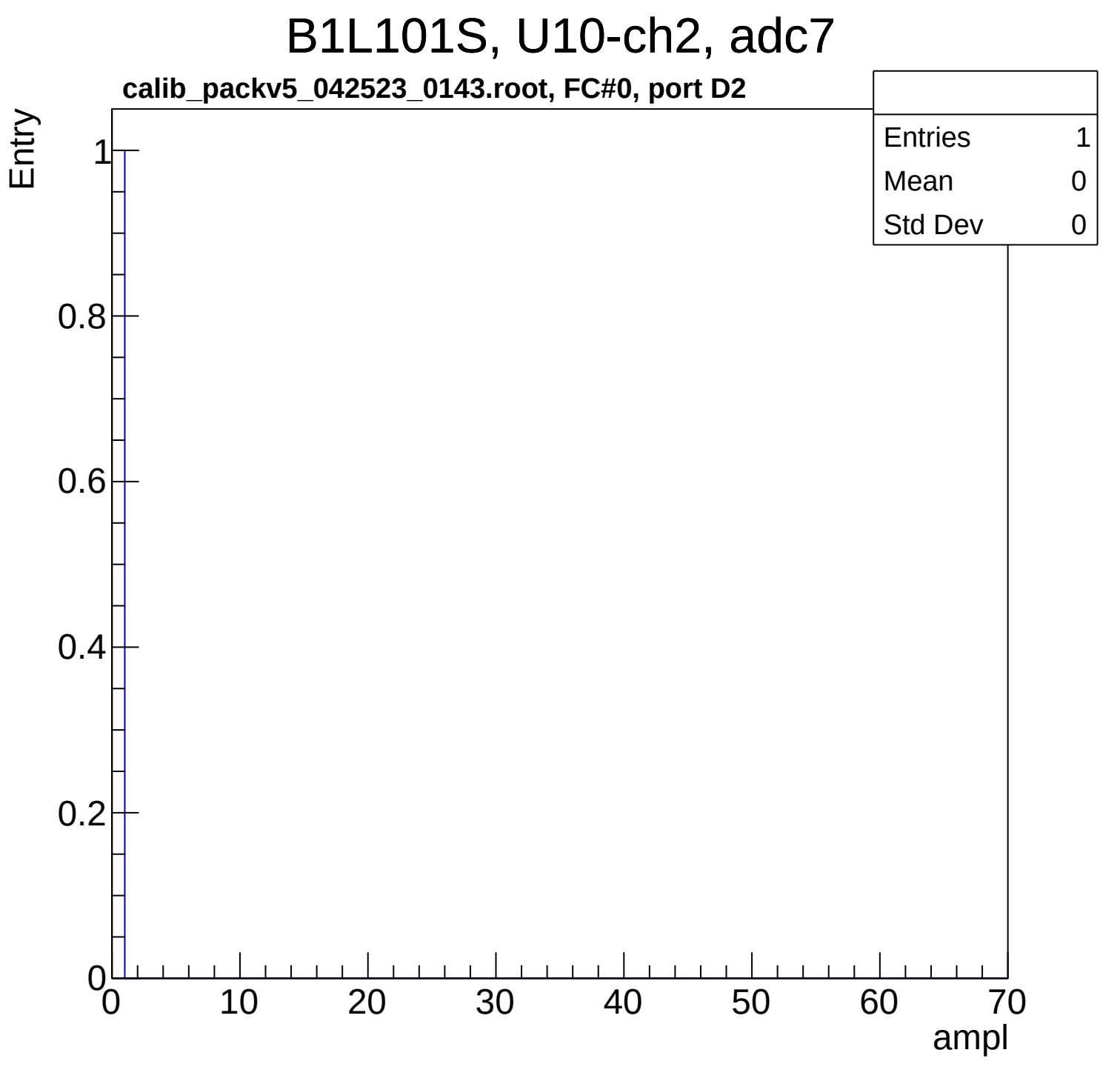
B1L101S, U10-ch2, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
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0.6
0.4
0.2
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10
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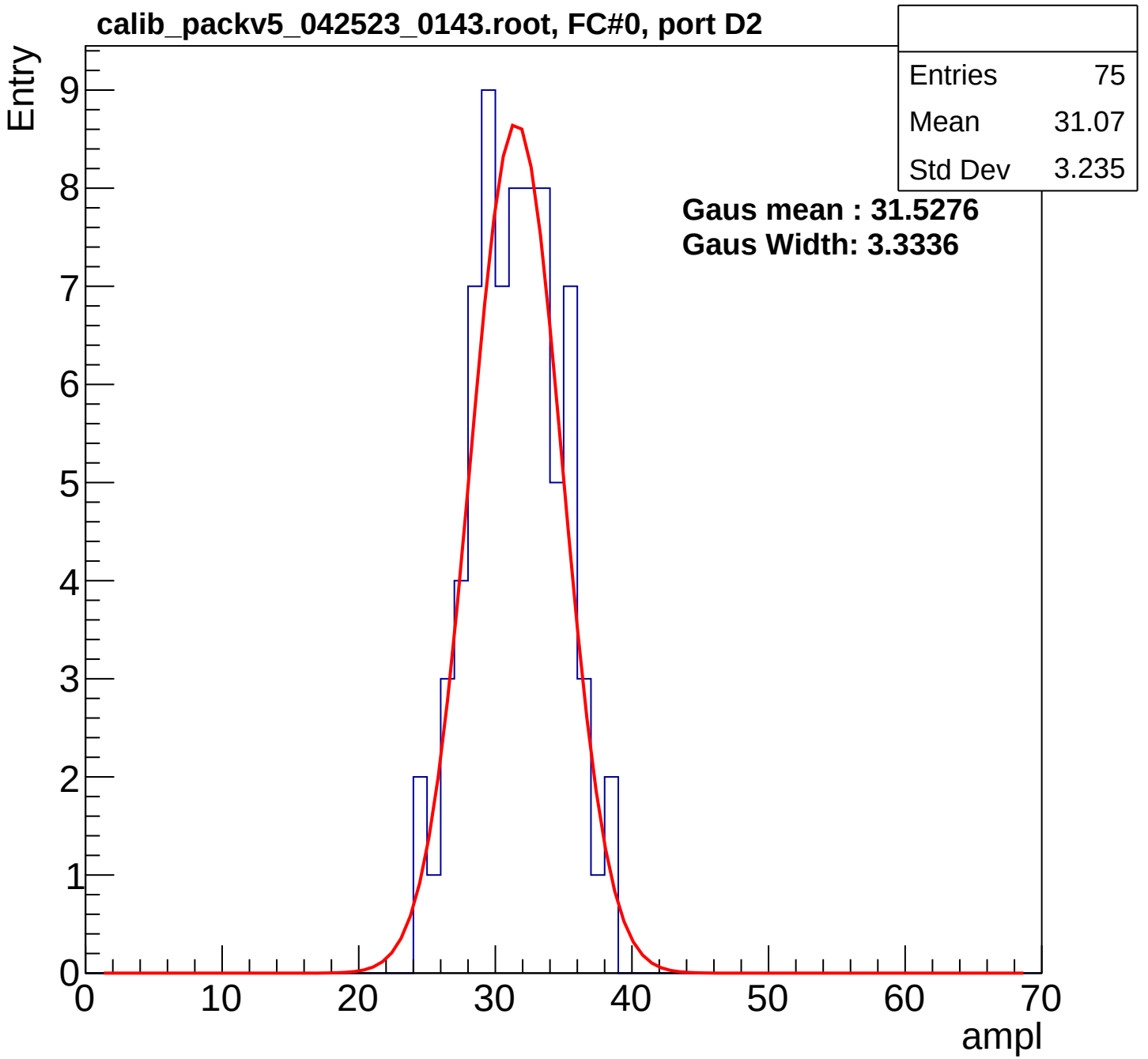
40
50
60
70
ampl


B1L101S, U10-ch3, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 31.07
Std Dev 3.235
Gaus mean : 31.5276
Gaus Width: 3.3336
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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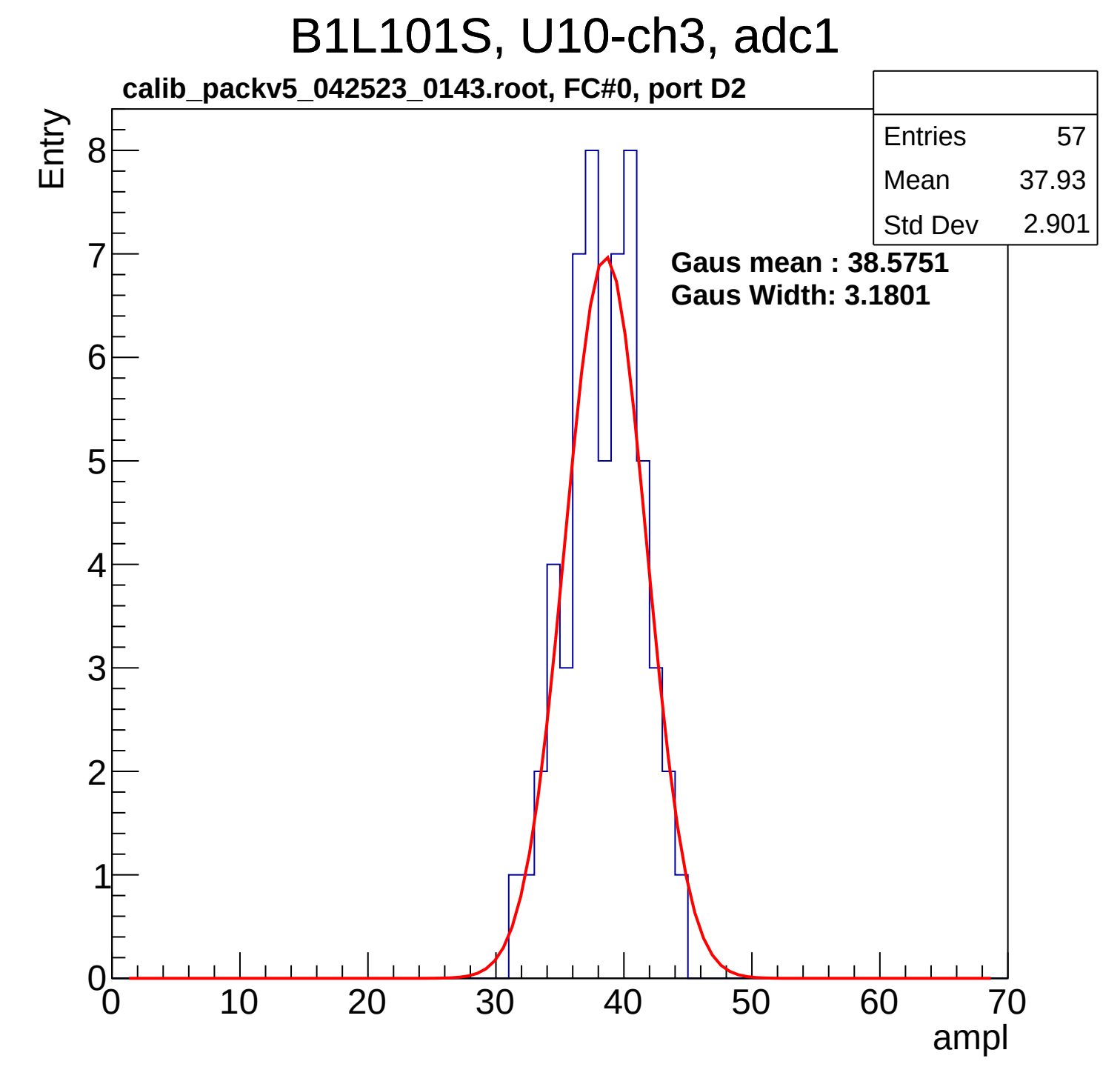
B1L101S, U10-ch3, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 37.93
Std Dev 2.901
Gaus mean : 38.5751
Gaus Width: 3.1801
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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20
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40
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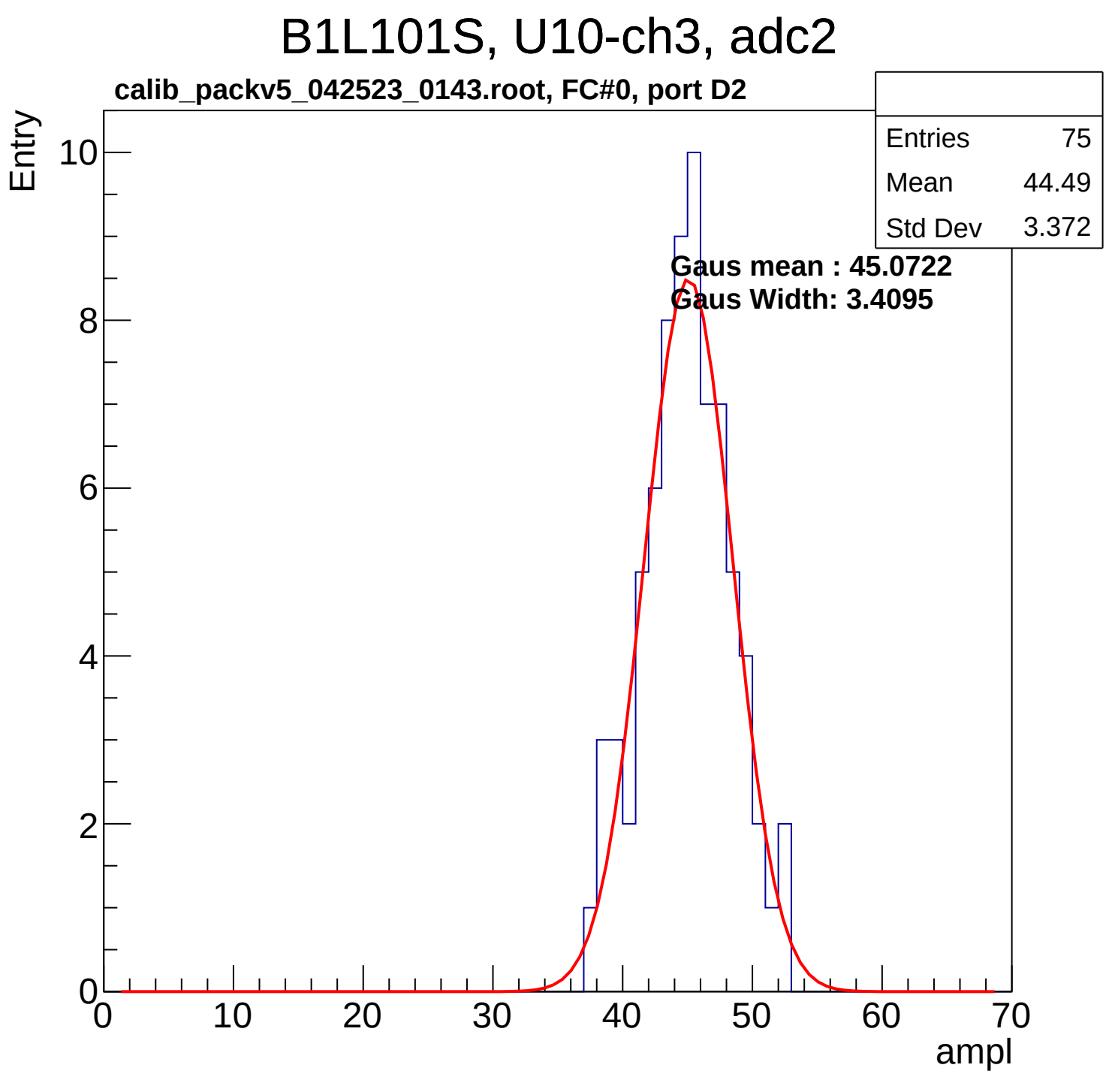
B1L101S, U10-ch3, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 44.49
Std Dev 3.372
Gaus mean : 45.0722
Gaus Width: 3.4095
Entry
ampl
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2
4
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8
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0
10
20
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50
60
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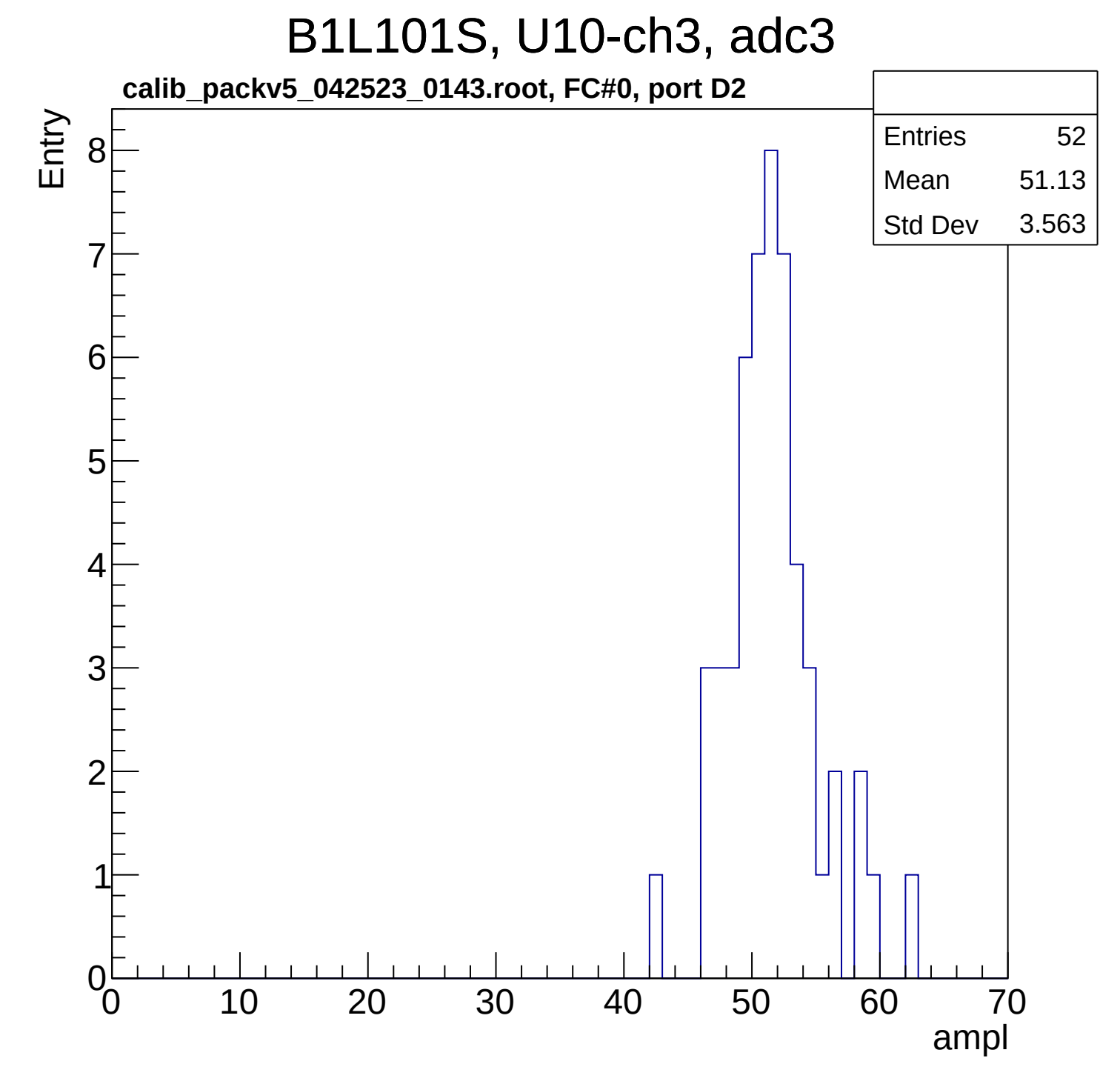
B1L101S, U10-ch3, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 51.13
Std Dev 3.563
Entry
ampl
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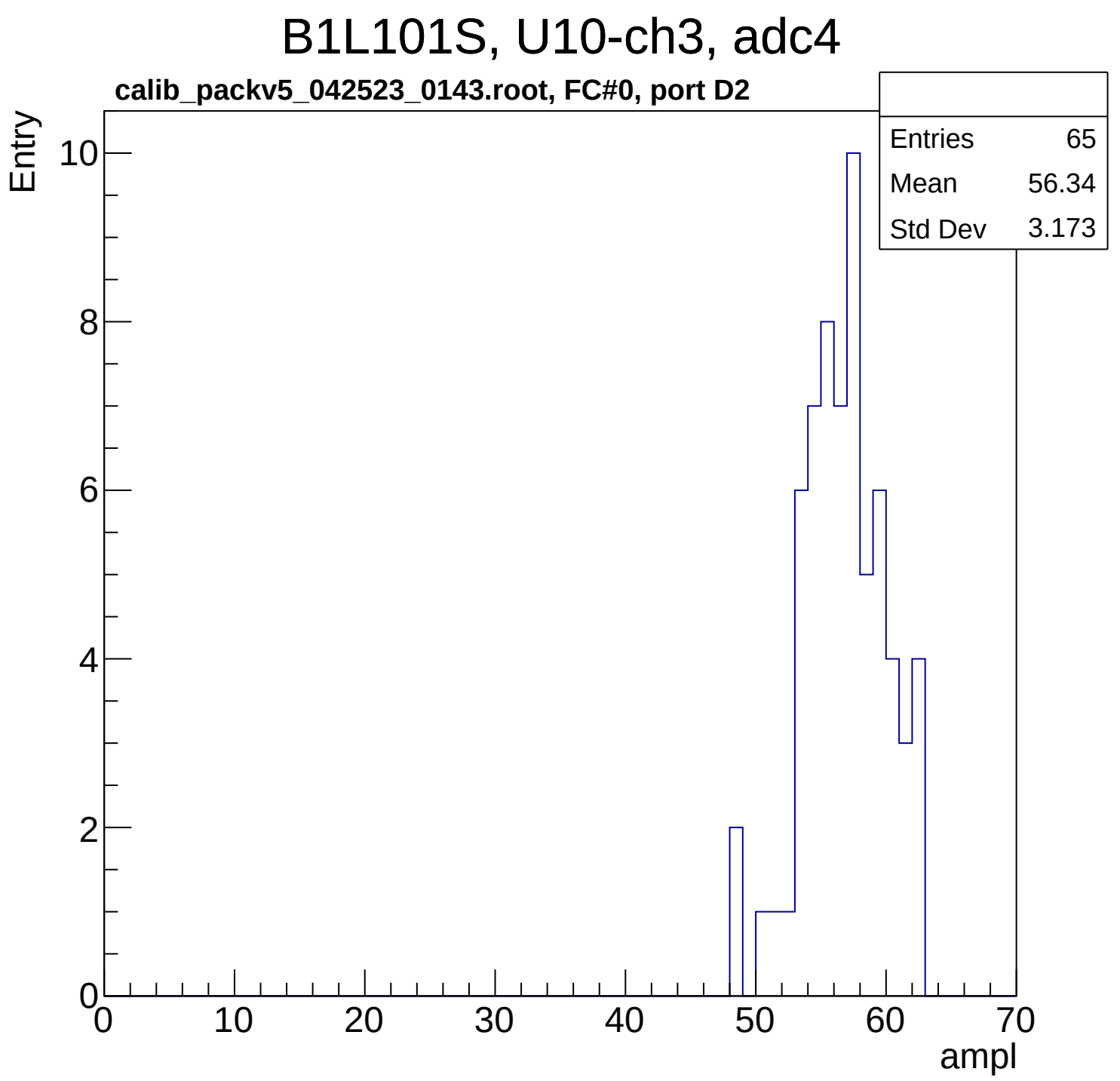
B1L101S, U10-ch3, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 56.34
Std Dev 3.173
Entry
ampl
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4
6
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0
10
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60
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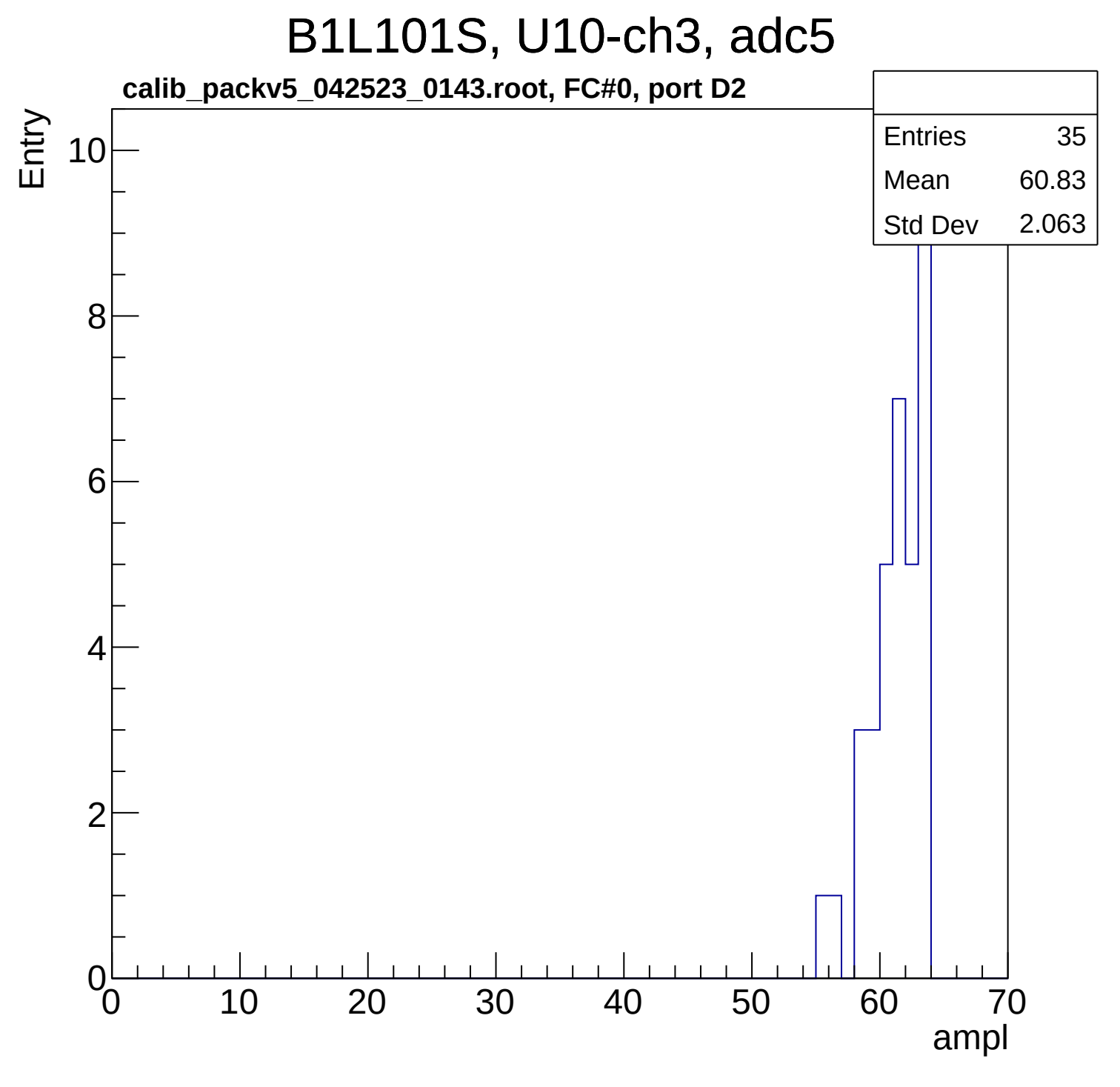
B1L101S, U10-ch3, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 35
Mean 60.83
Std Dev 2.063
Entry
ampl
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2
4
6
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10
0
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40
50
60
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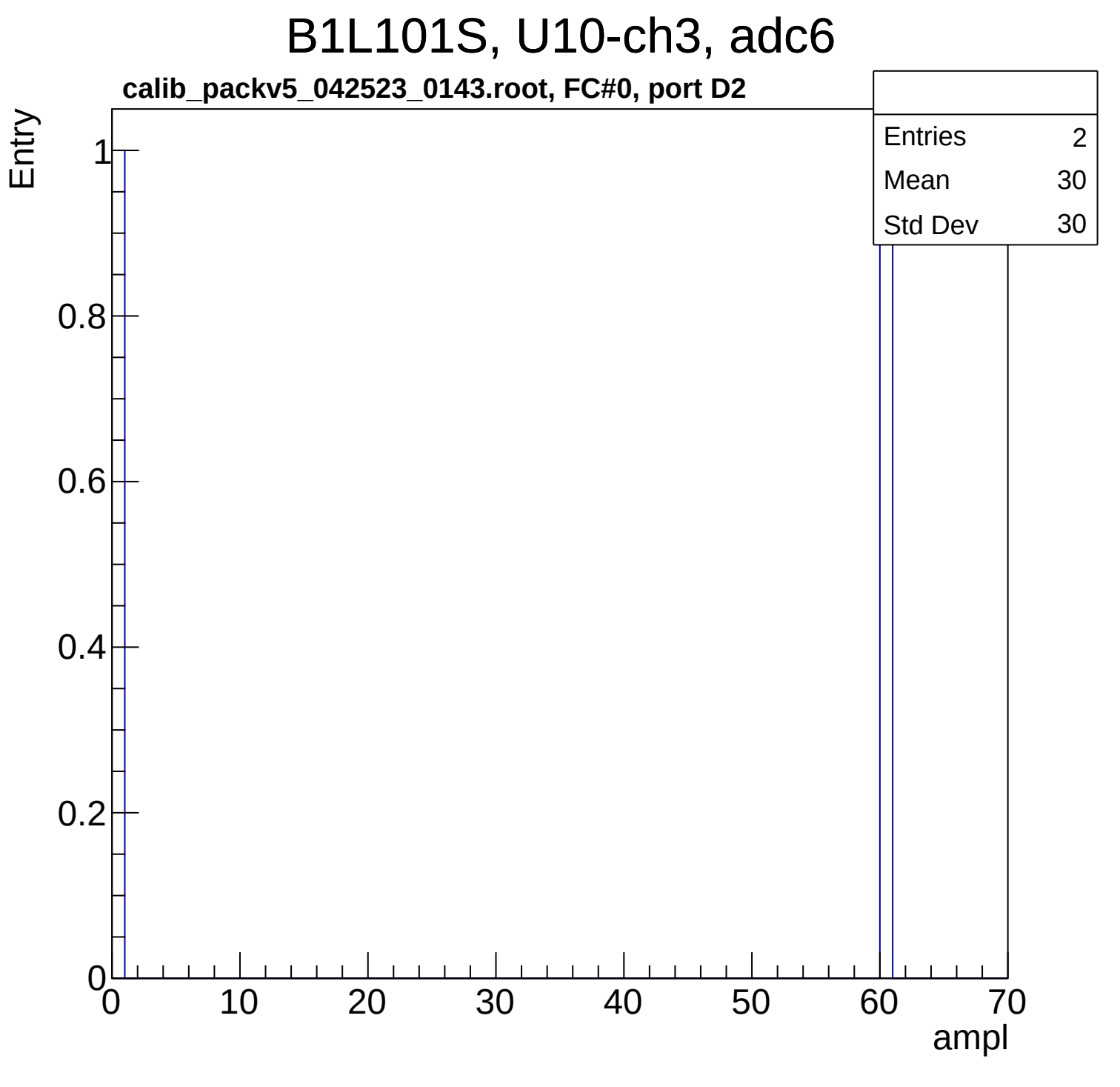
B1L101S, U10-ch3, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 30
Std Dev 30
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
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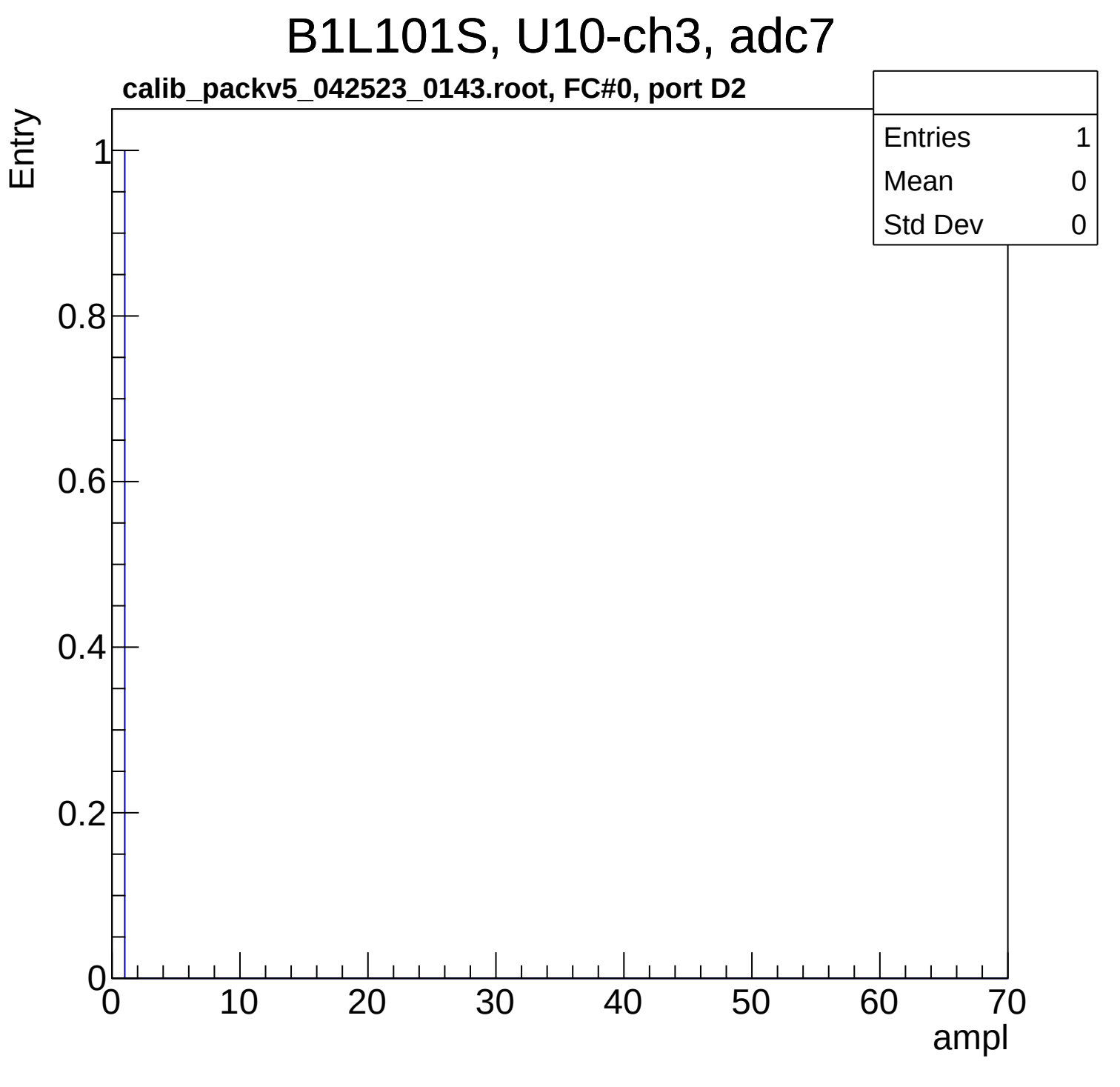
50
60
70
ampl


B1L101S, U10-ch3, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
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0.6
0.4
0.2
0
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10
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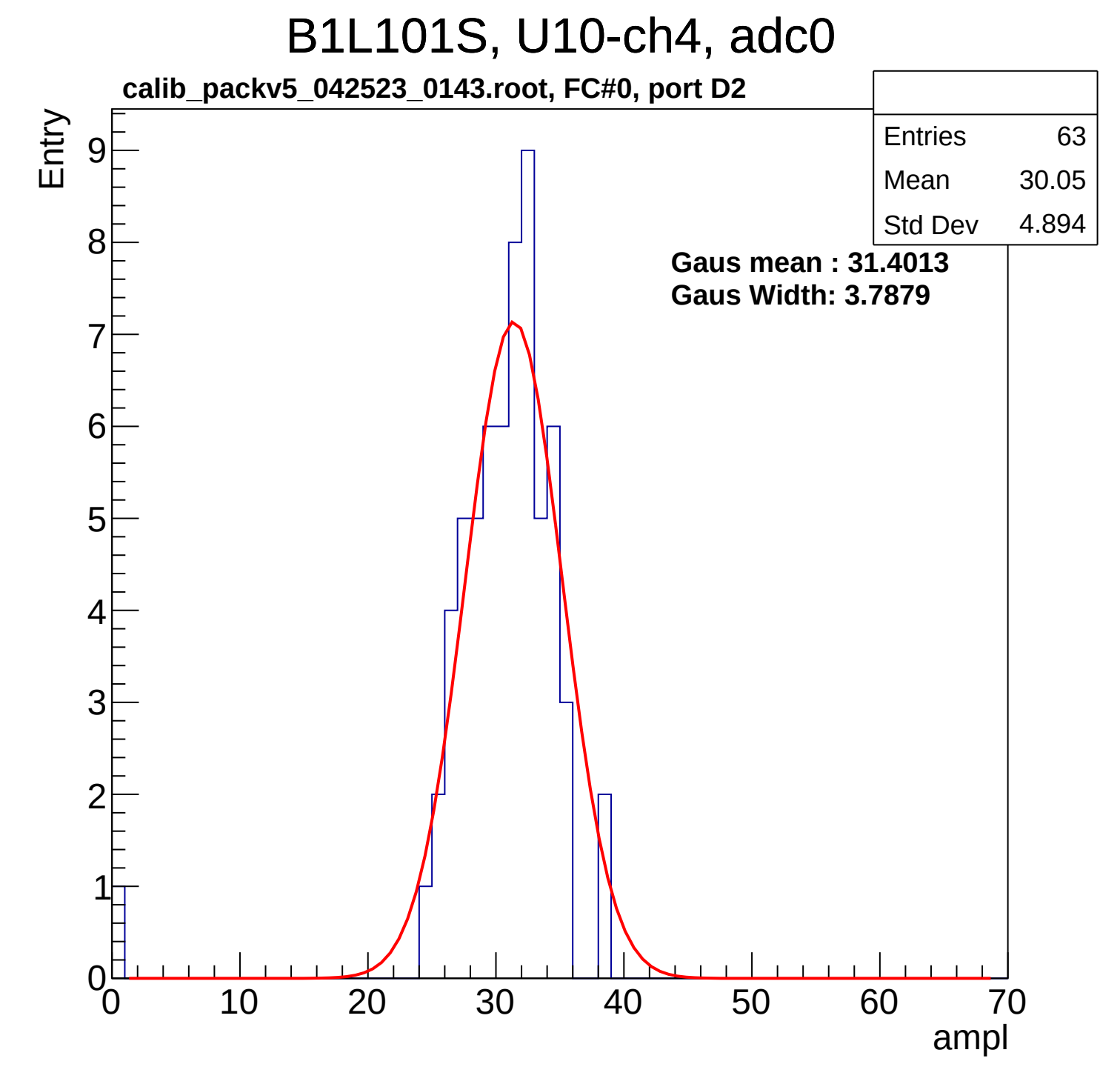
ampl


B1L101S, U10-ch4, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 30.05
Std Dev 4.894
Gaus mean : 31.4013
Gaus Width: 3.7879
Entry
ampl
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1
2
3
4
5
6
7
8
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0
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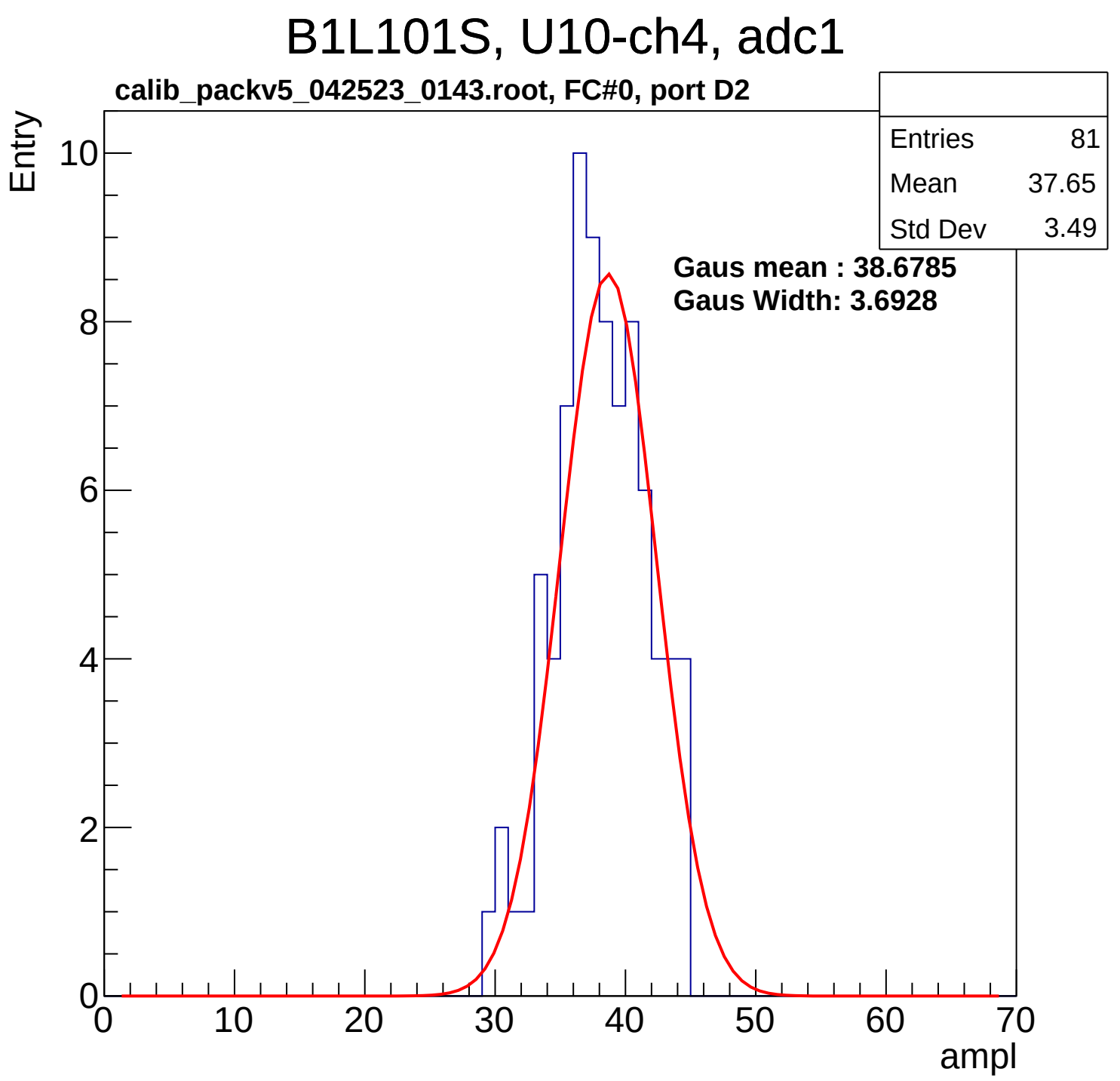
B1L101S, U10-ch4, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 81
Mean 37.65
Std Dev 3.49
Gaus mean : 38.6785
Gaus Width: 3.6928
Entry
ampl
0
2
4
6
8
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0
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60
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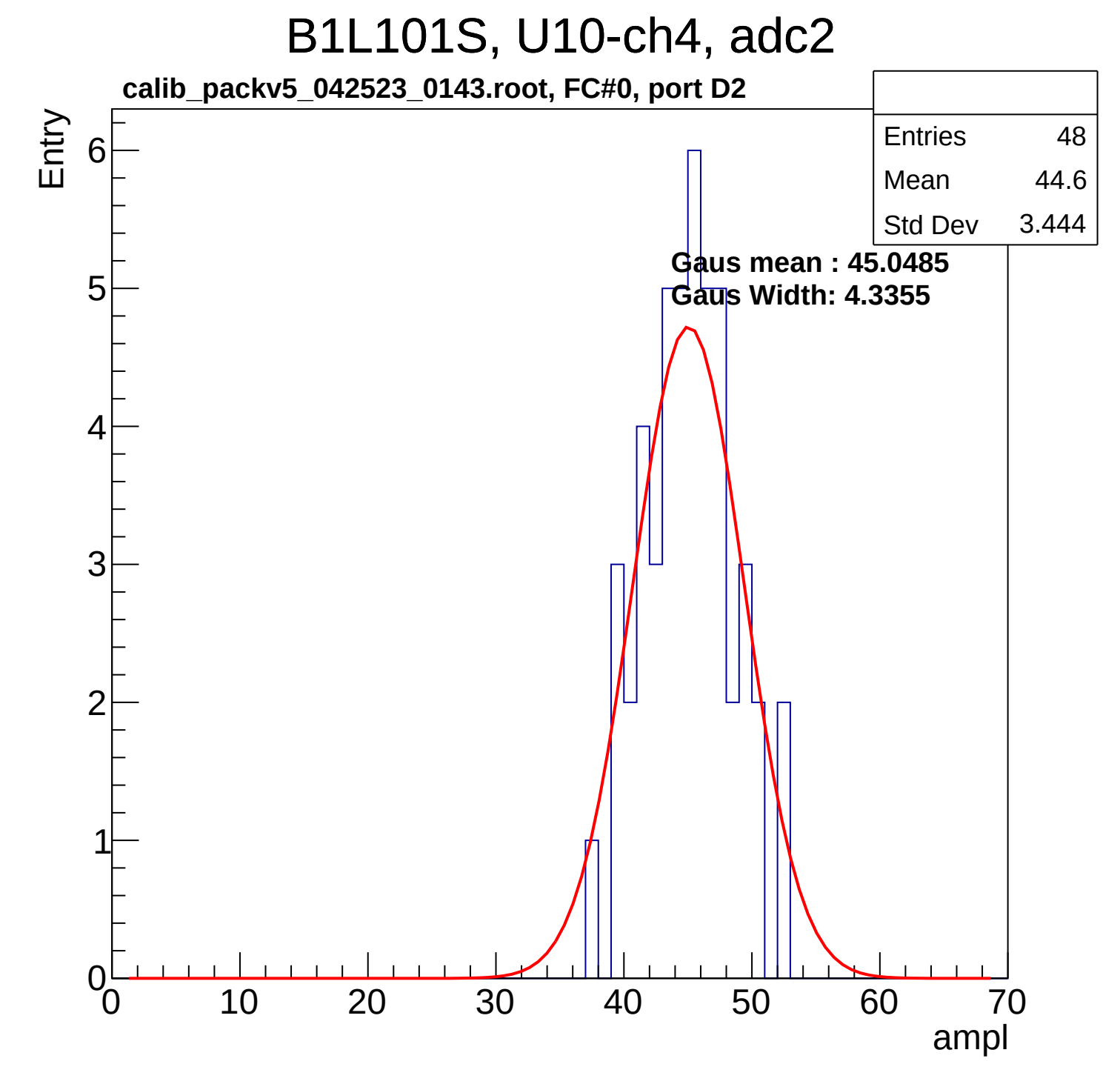
B1L101S, U10-ch4, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 44.6
Std Dev 3.444
Gaus mean : 45.0485
Gaus Width: 4.3355
Entry
ampl
0
1
2
3
4
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0
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60
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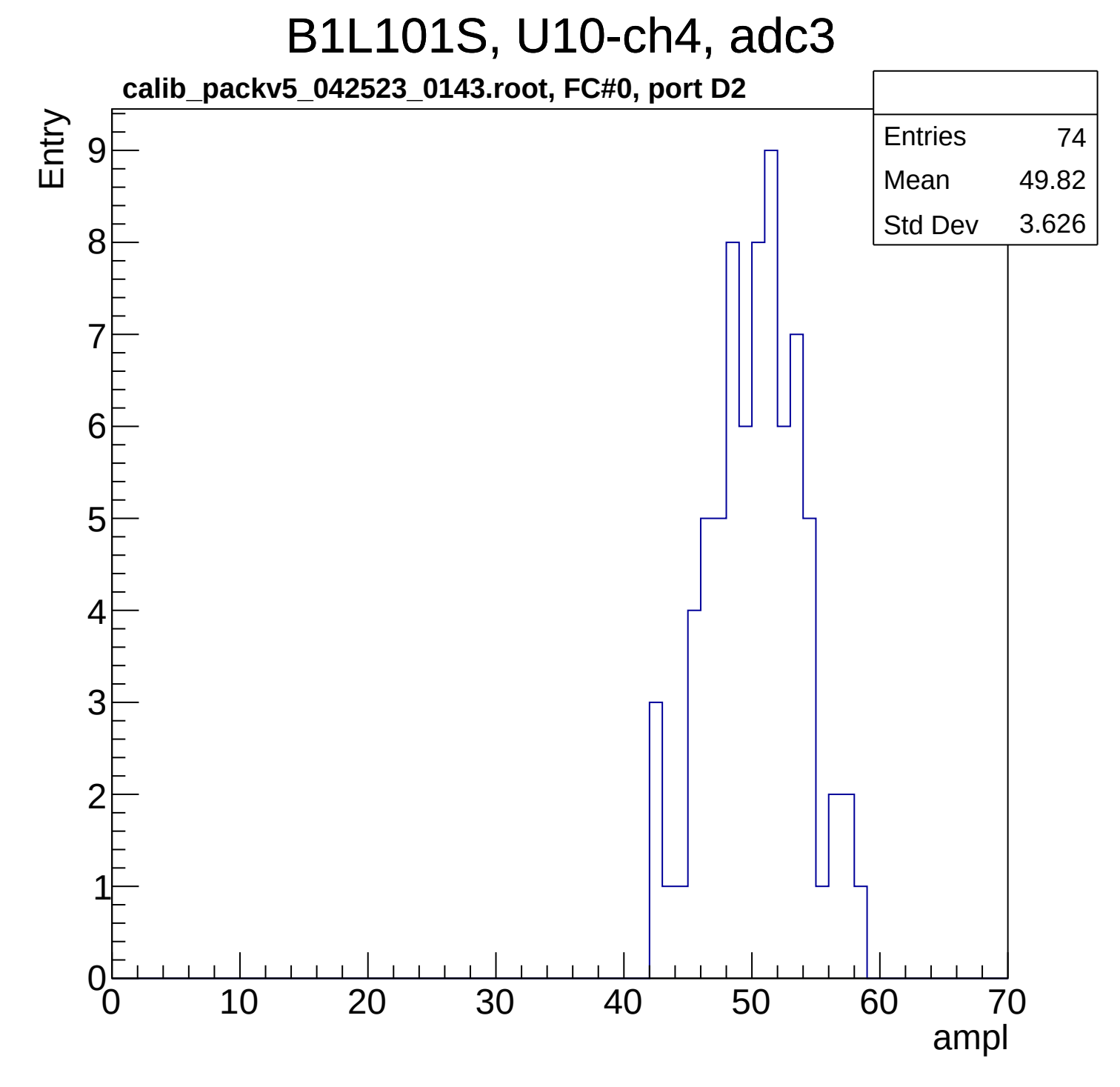
B1L101S, U10-ch4, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 49.82
Std Dev 3.626
Entry
ampl
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2
3
4
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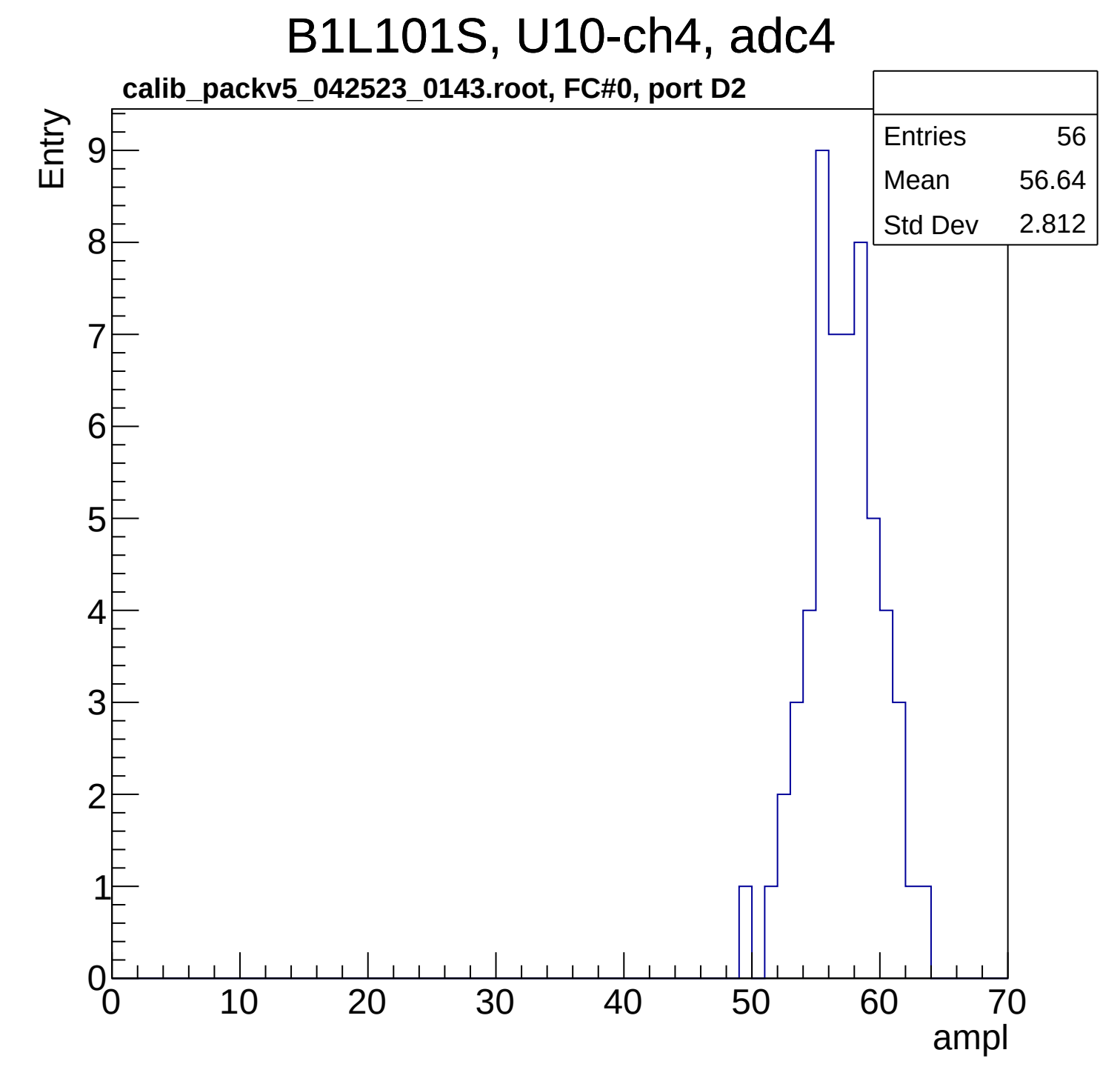
B1L101S, U10-ch4, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 56.64
Std Dev 2.812
Entry
ampl
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1
2
3
4
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6
7
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0
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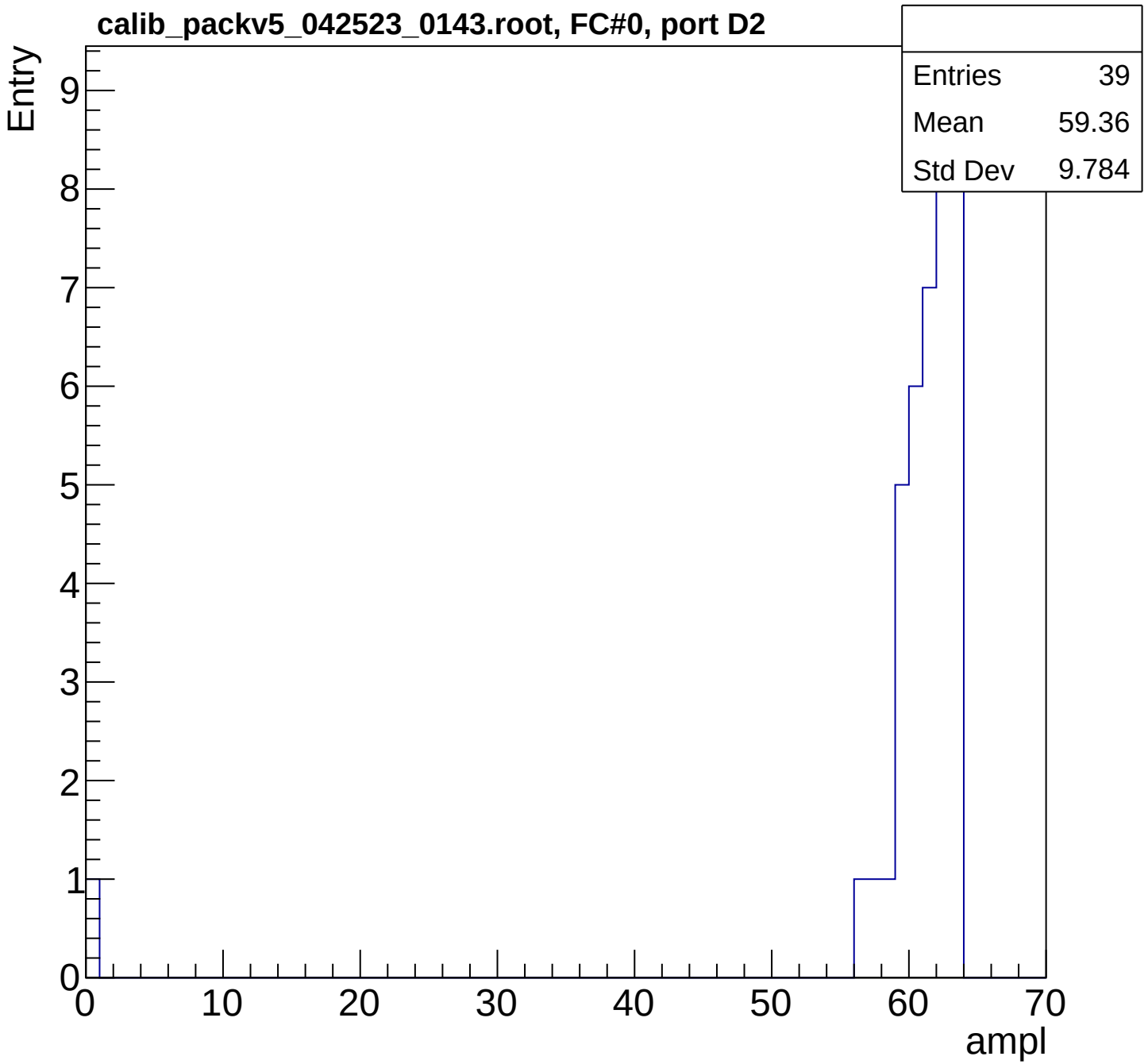
B1L101S, U10-ch4, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 39
Mean 59.36
Std Dev 9.784
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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60
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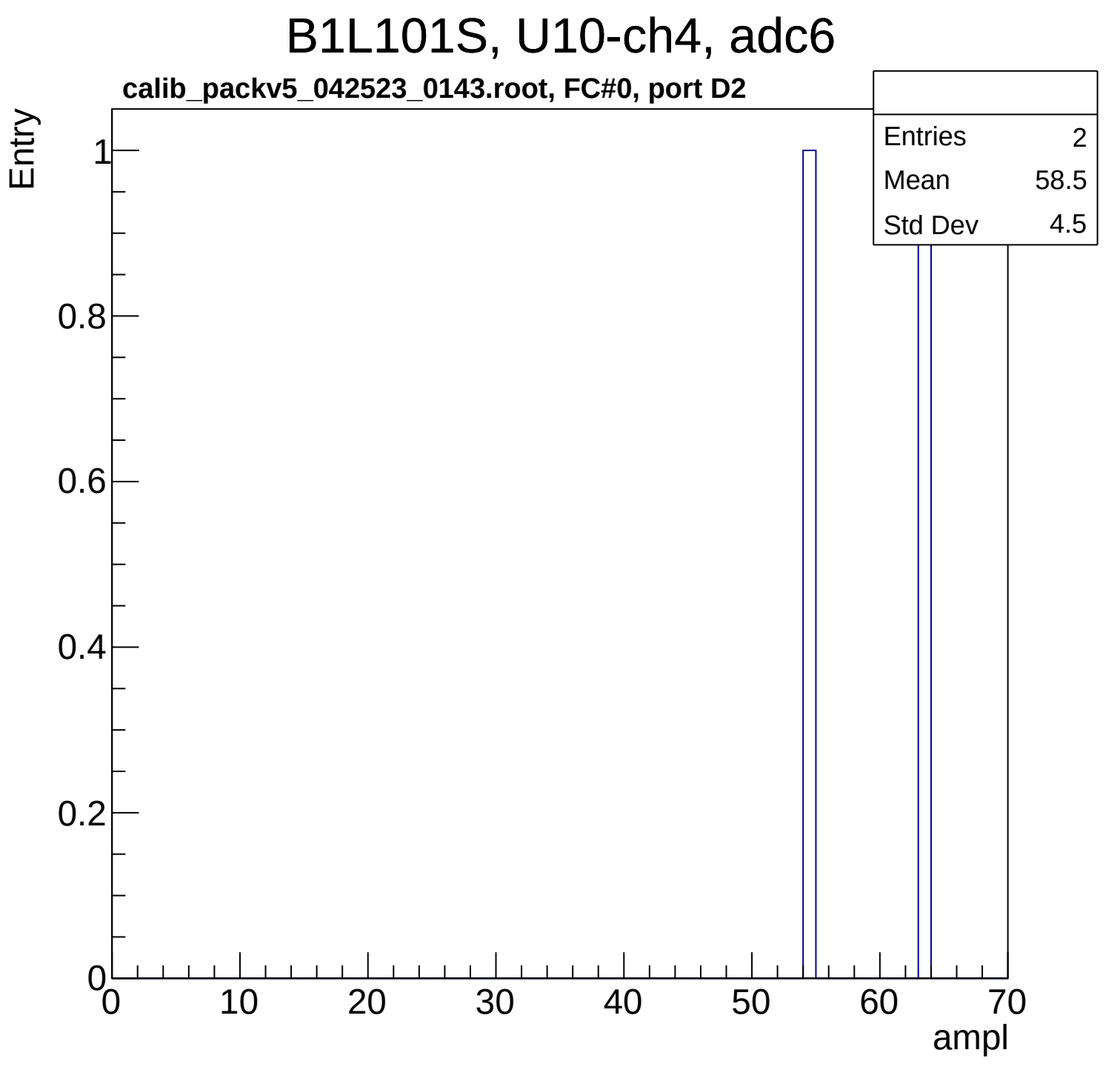
B1L101S, U10-ch4, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 58.5
Std Dev 4.5
Entry
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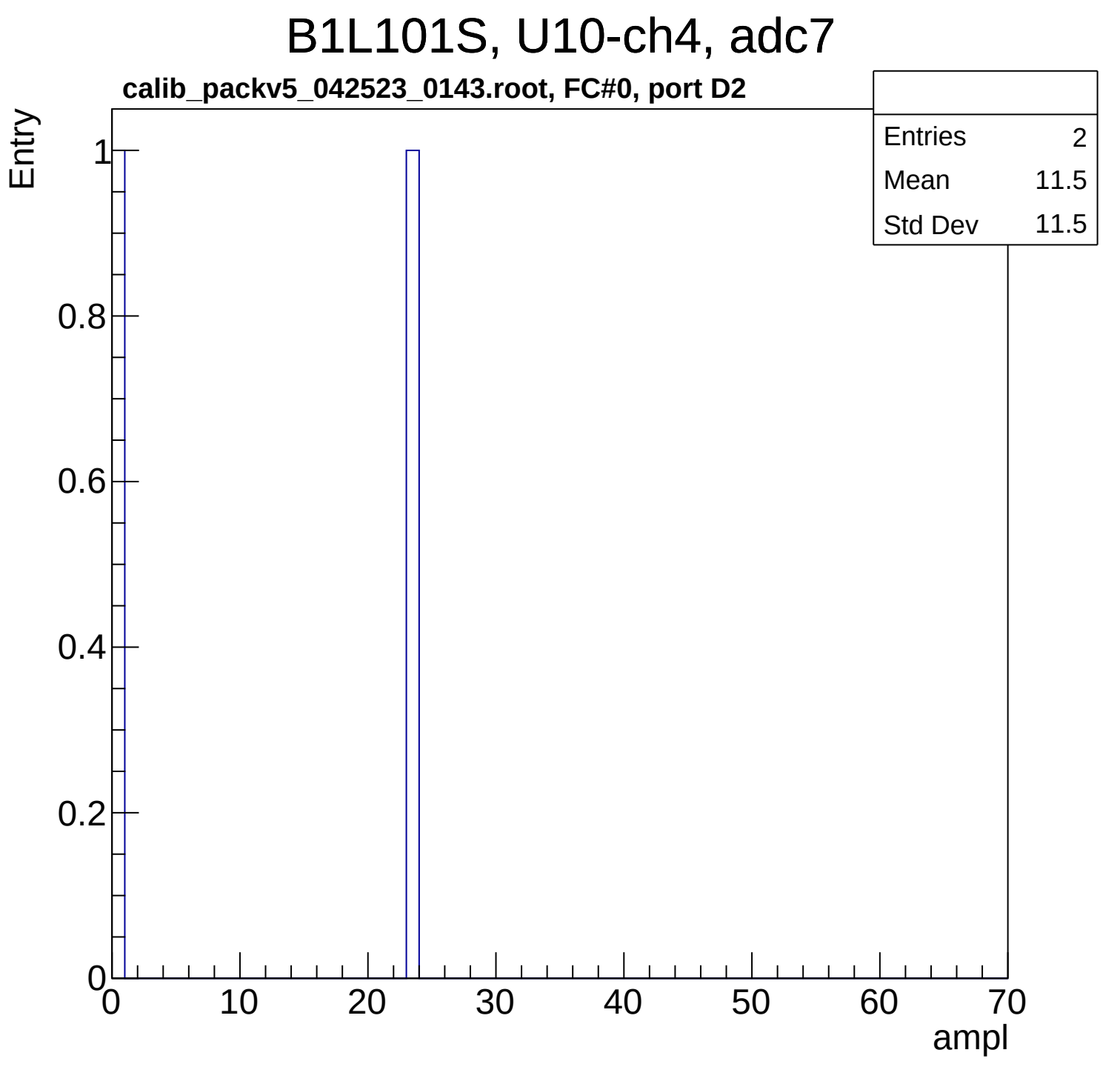
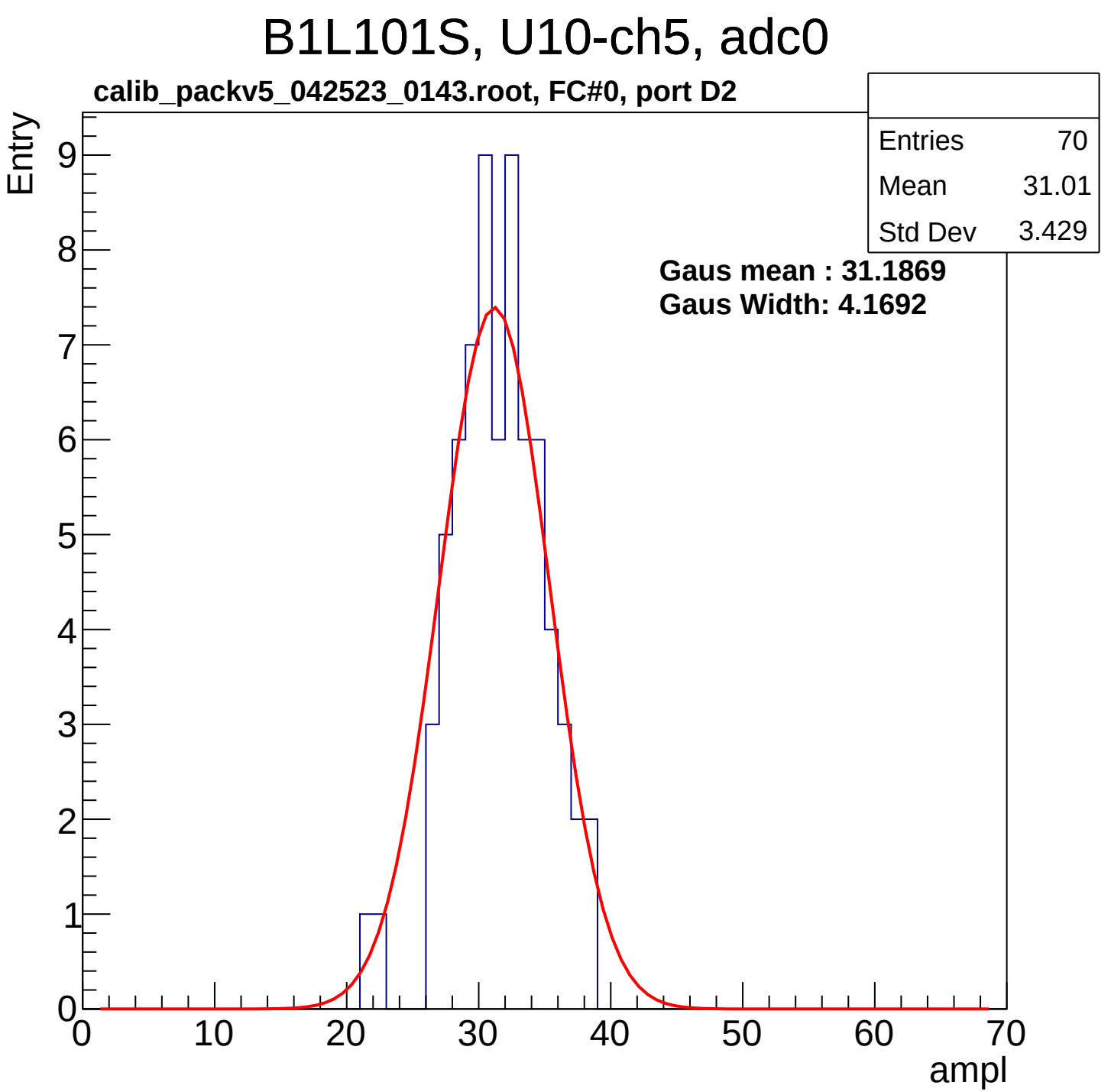
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch4, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 11.5
Std Dev 11.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L101S, U10-ch5, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 31.01
Std Dev 3.429
Gaus mean : 31.1869
Gaus Width: 4.1692
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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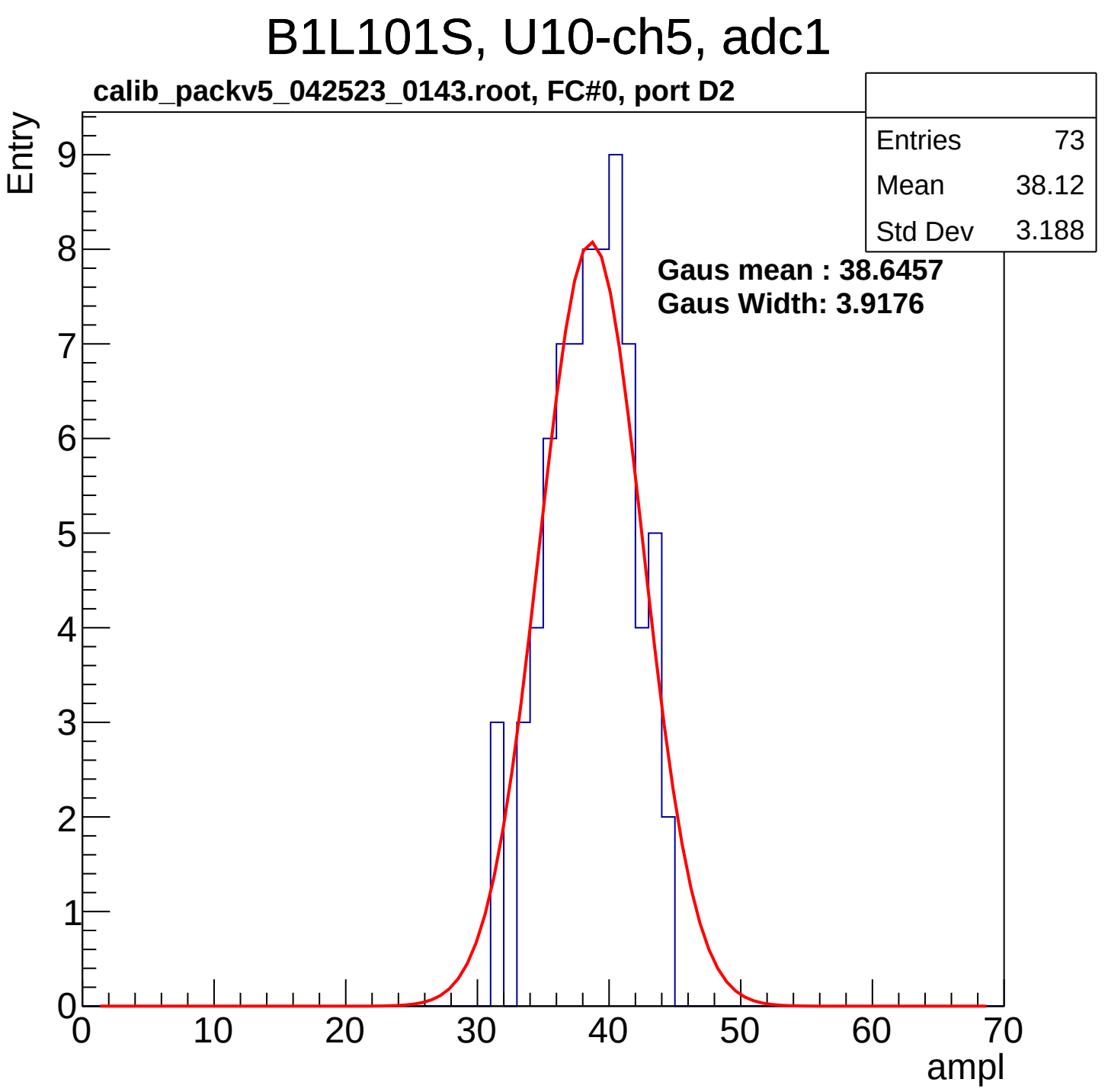
B1L101S, U10-ch5, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 38.12
Std Dev 3.188
Gaus mean : 38.6457
Gaus Width: 3.9176
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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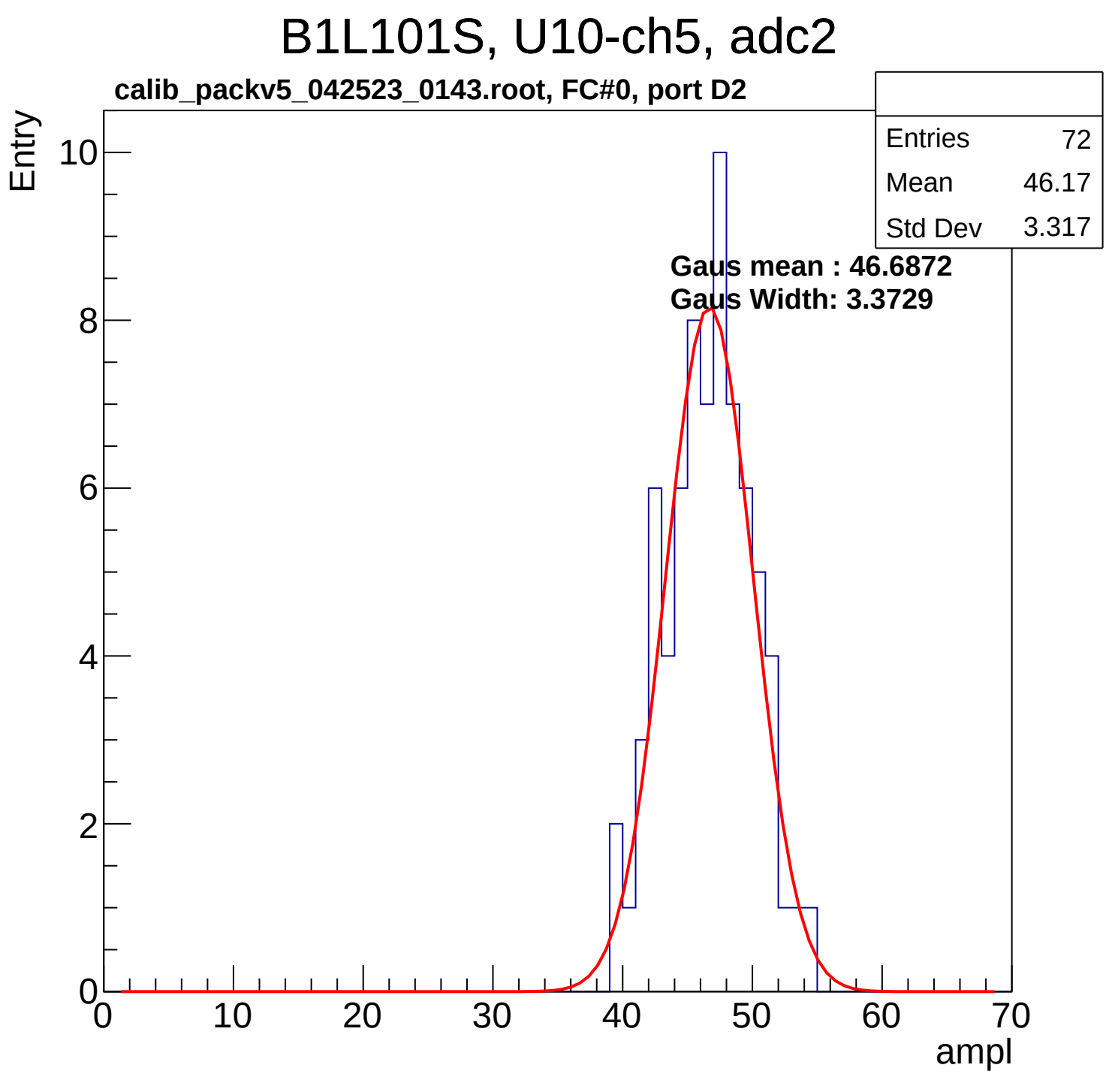
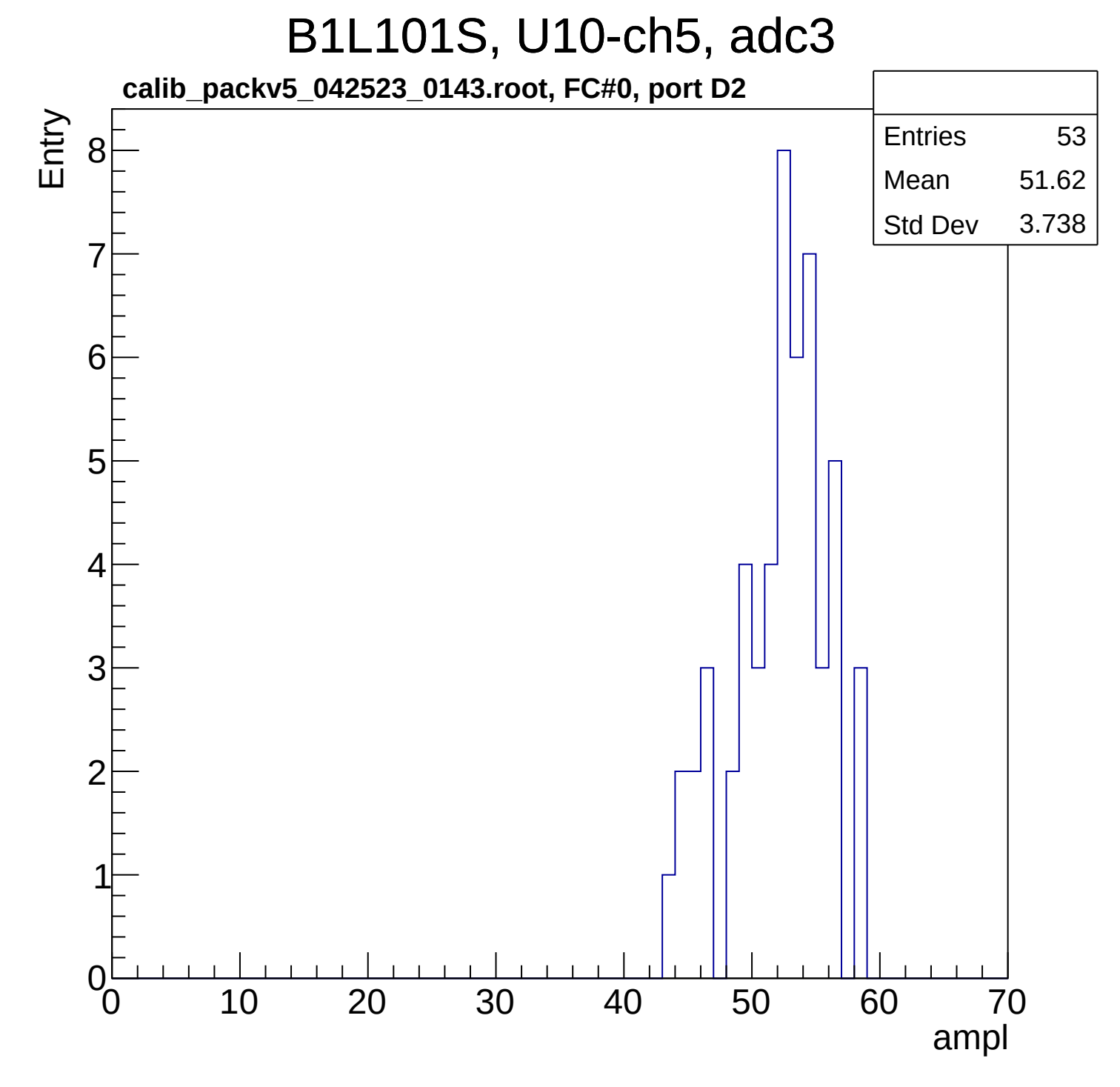

B1L101S, U10-ch5, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 46.17
Std Dev 3.317
Gaus mean : 46.6872
Gaus Width: 3.3729
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch5, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 51.62
Std Dev 3.738
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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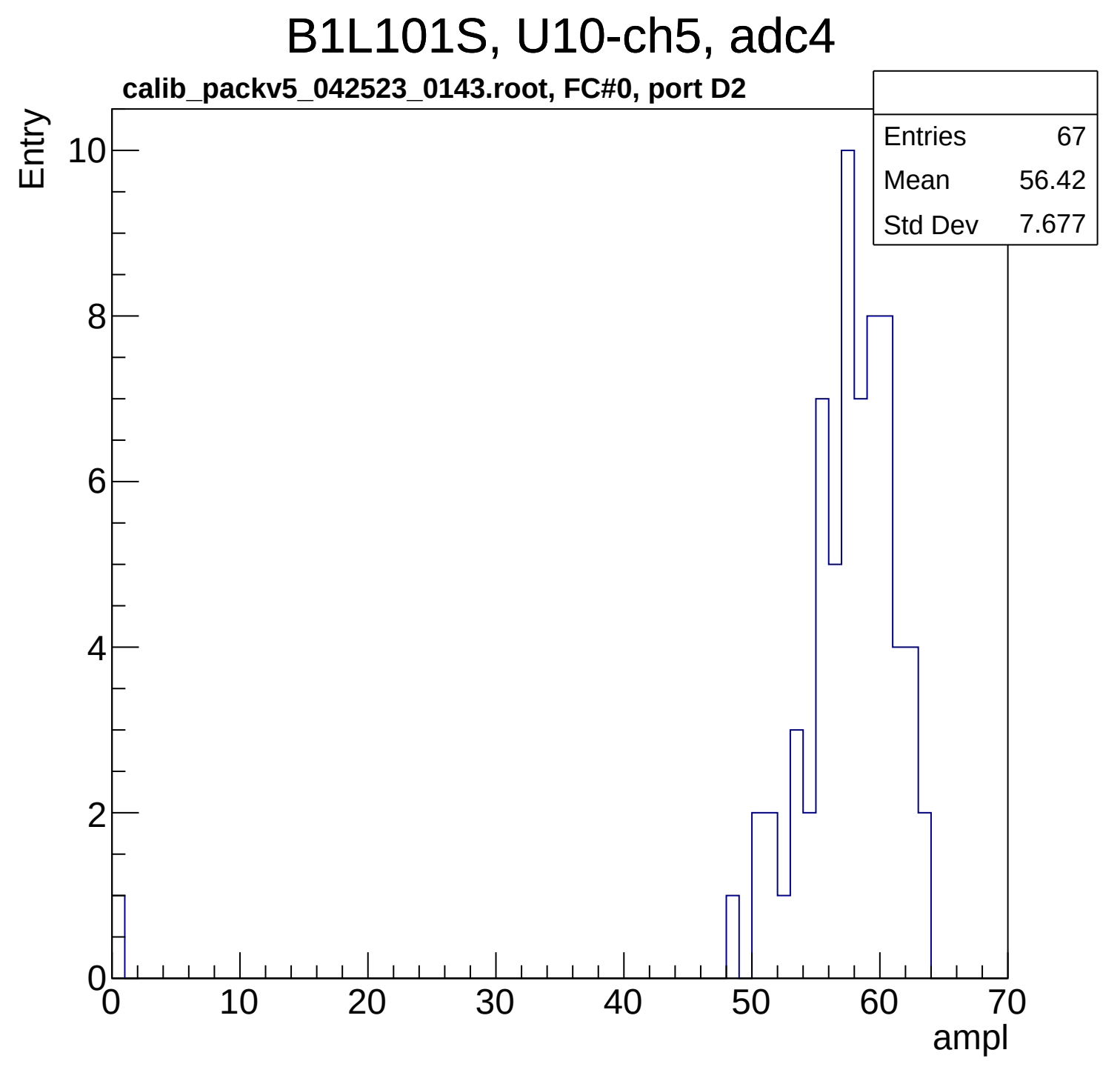
B1L101S, U10-ch5, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 56.42
Std Dev 7.677
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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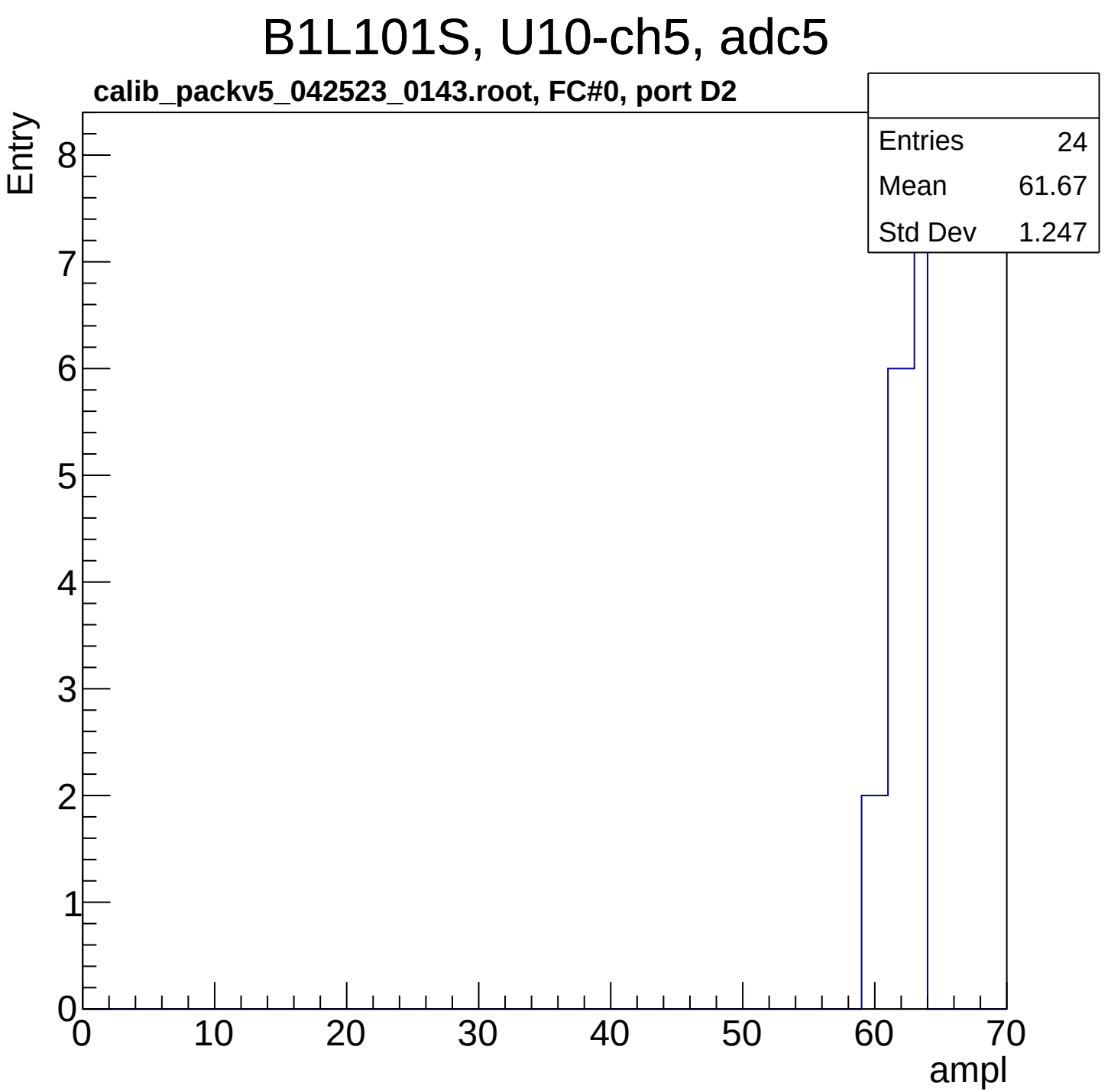
B1L101S, U10-ch5, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 24
Mean 61.67
Std Dev 1.247
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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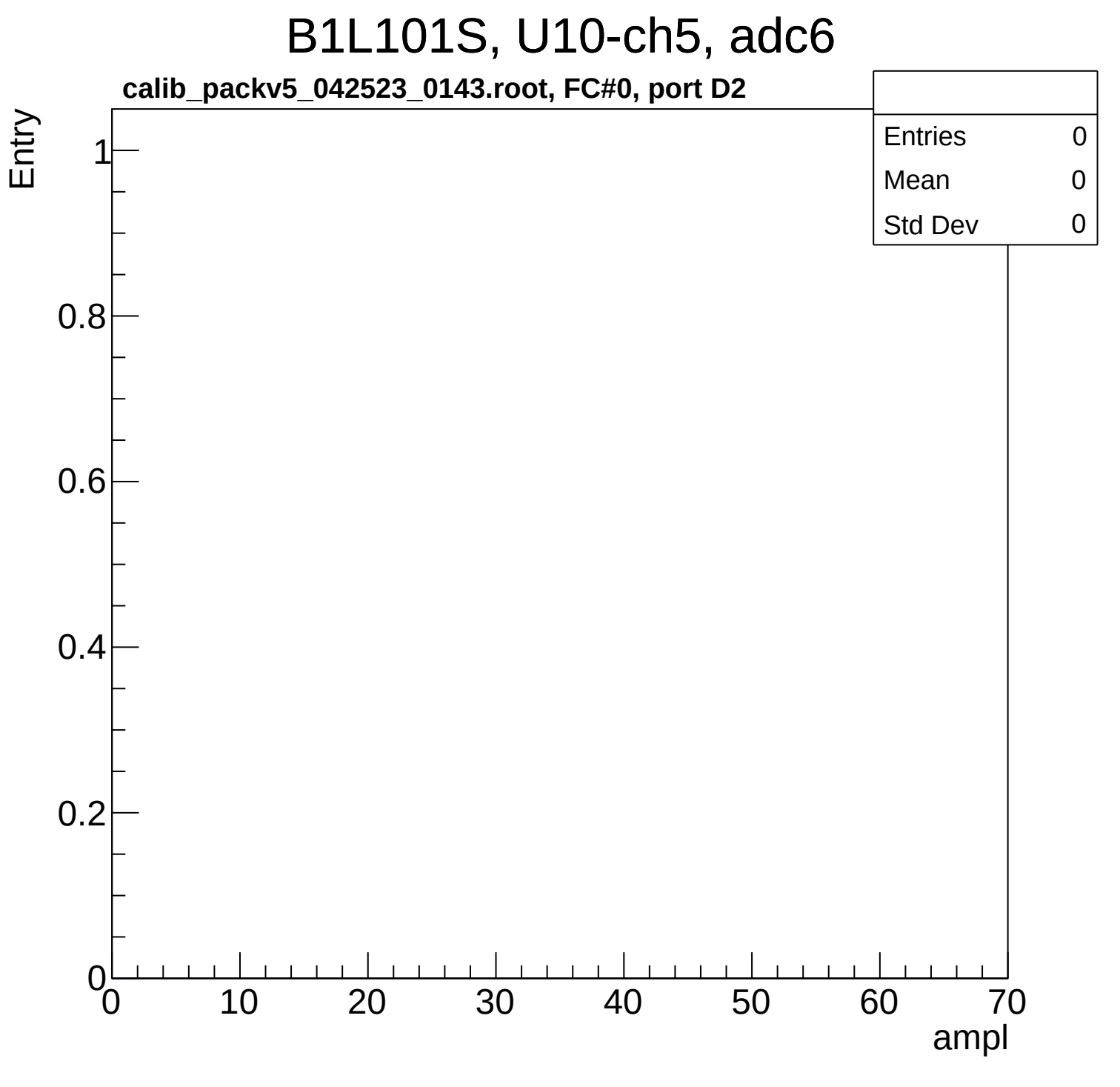
B1L101S, U10-ch5, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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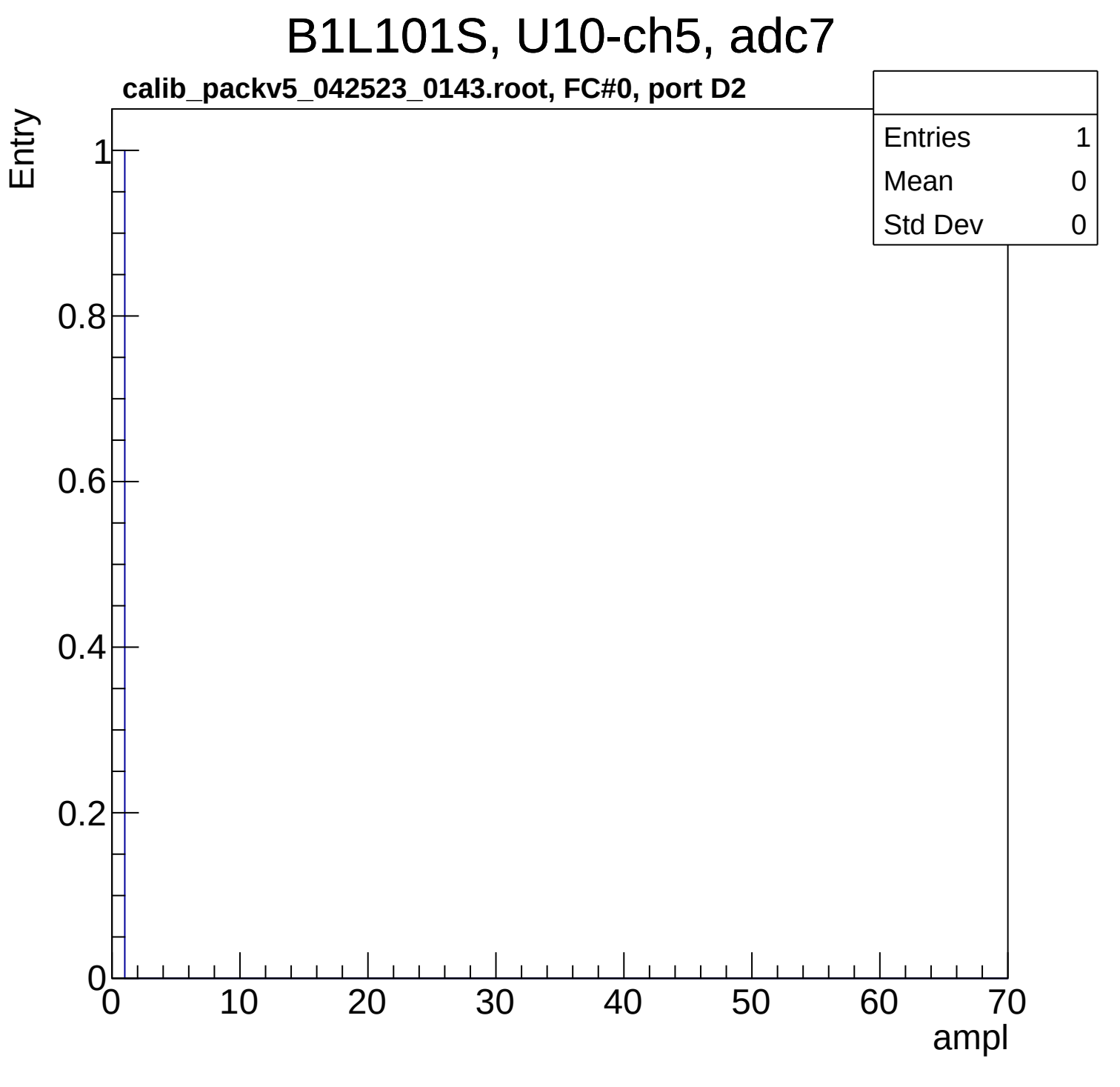
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch5, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
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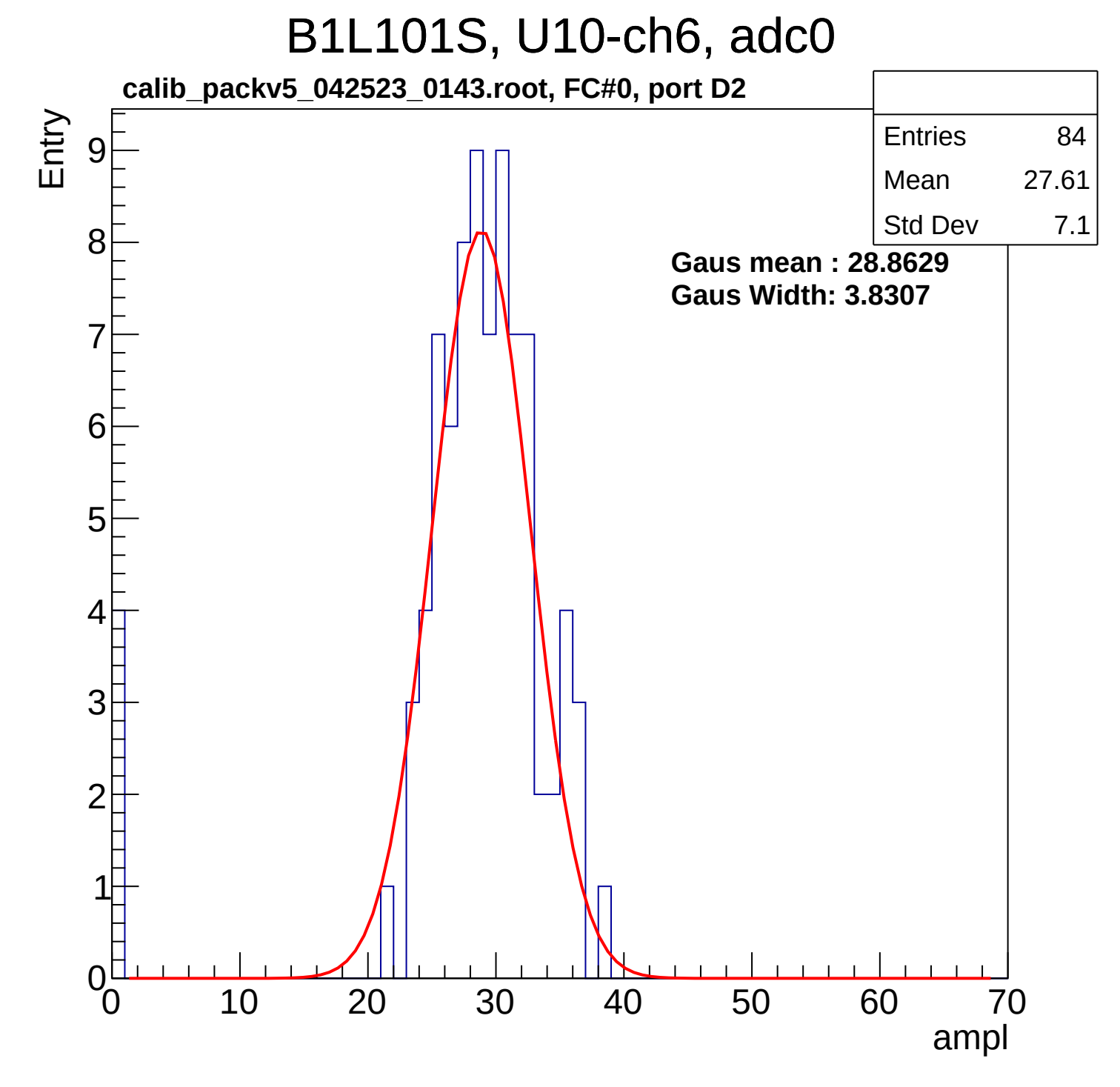
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch6, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 84
Mean 27.61
Std Dev 7.1
Gaus mean : 28.8629
Gaus Width: 3.8307
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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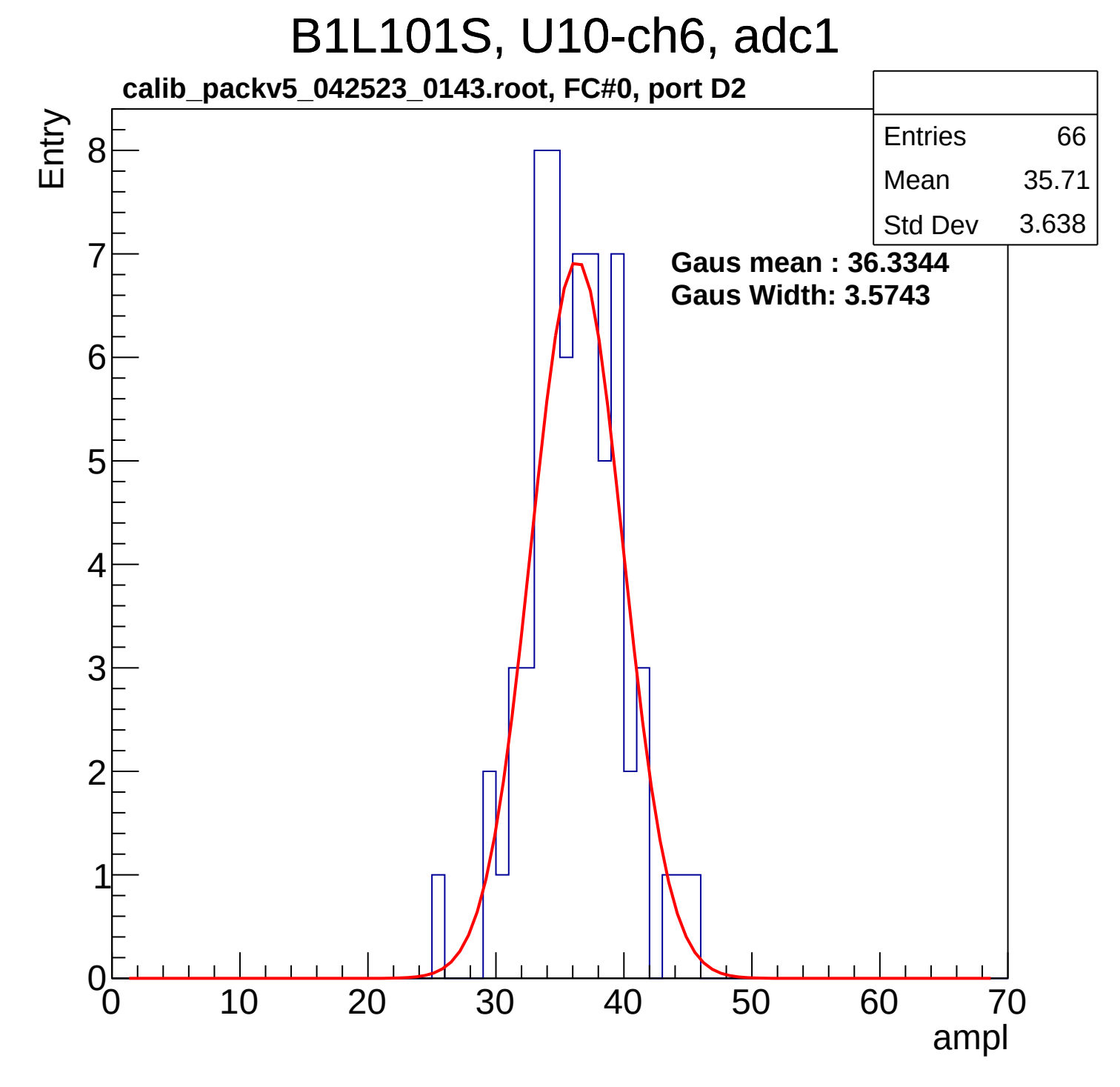
B1L101S, U10-ch6, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 35.71
Std Dev 3.638
Gaus mean : 36.3344
Gaus Width: 3.5743
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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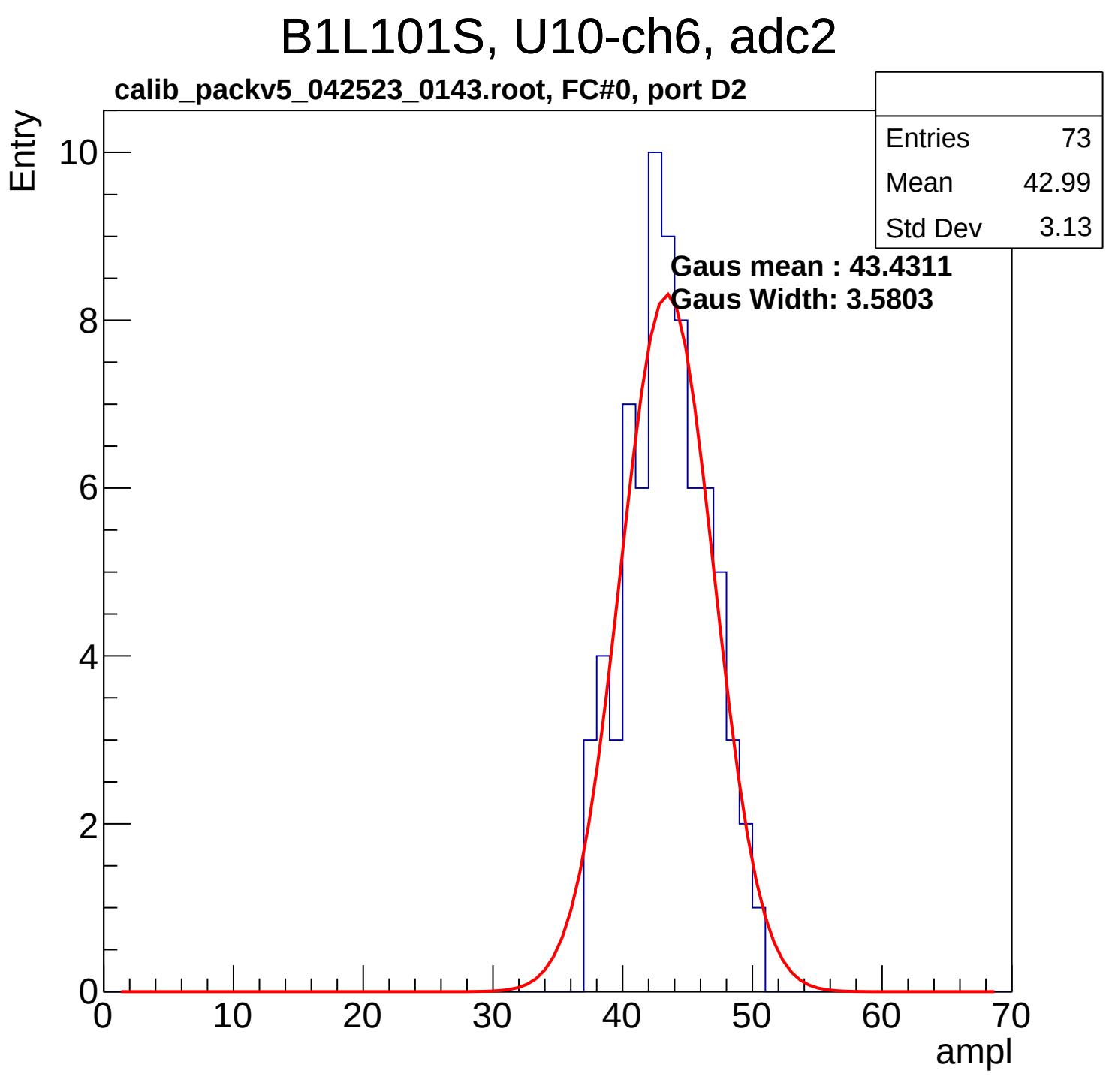
B1L101S, U10-ch6, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 42.99
Std Dev 3.13
Gaus mean : 43.4311
Gaus Width: 3.5803
Entry
ampl
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2
4
6
8
10
0
10
20
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50
60
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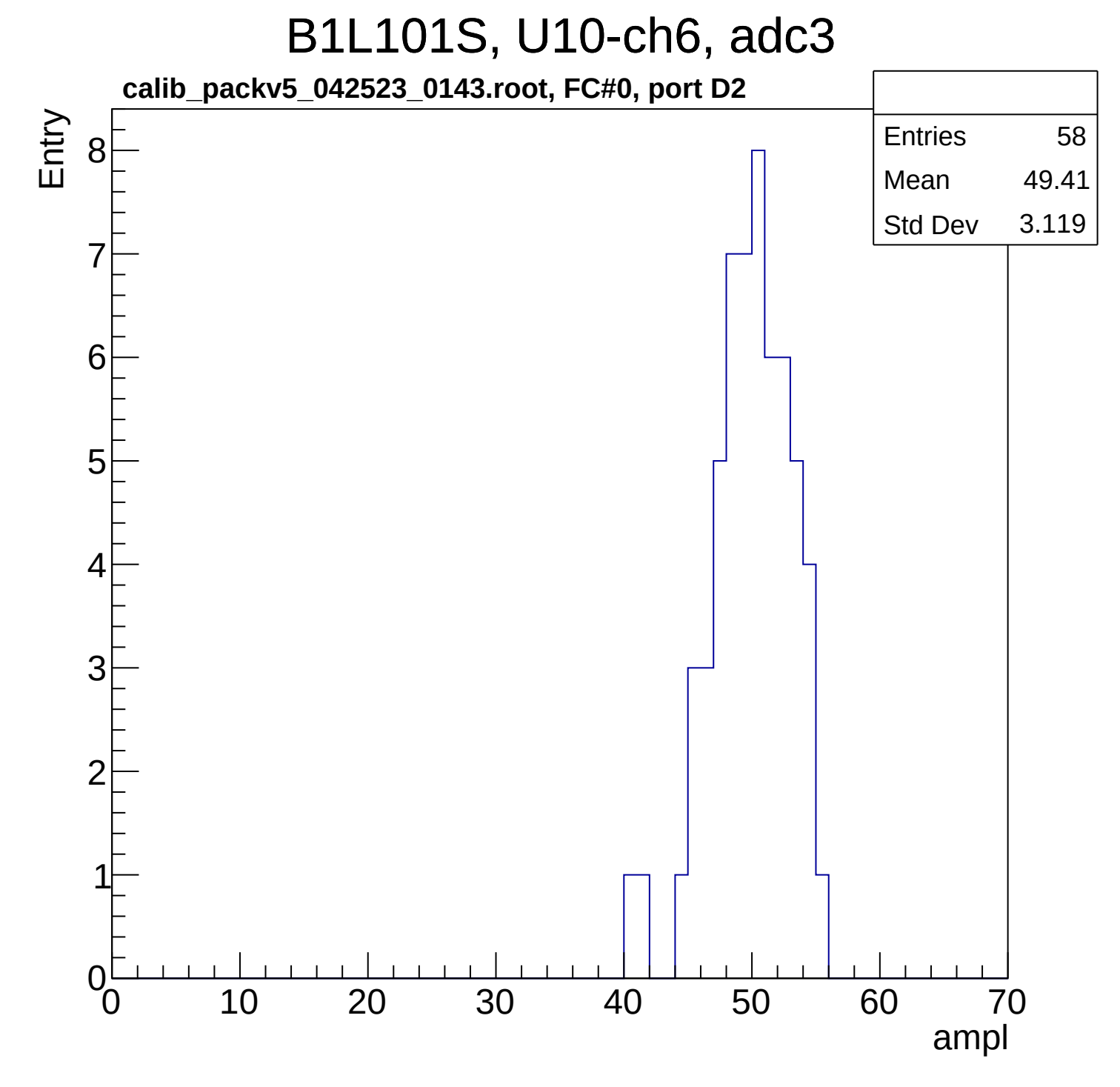
B1L101S, U10-ch6, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 49.41
Std Dev 3.119
Entry
ampl
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4
5
6
7
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0
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60
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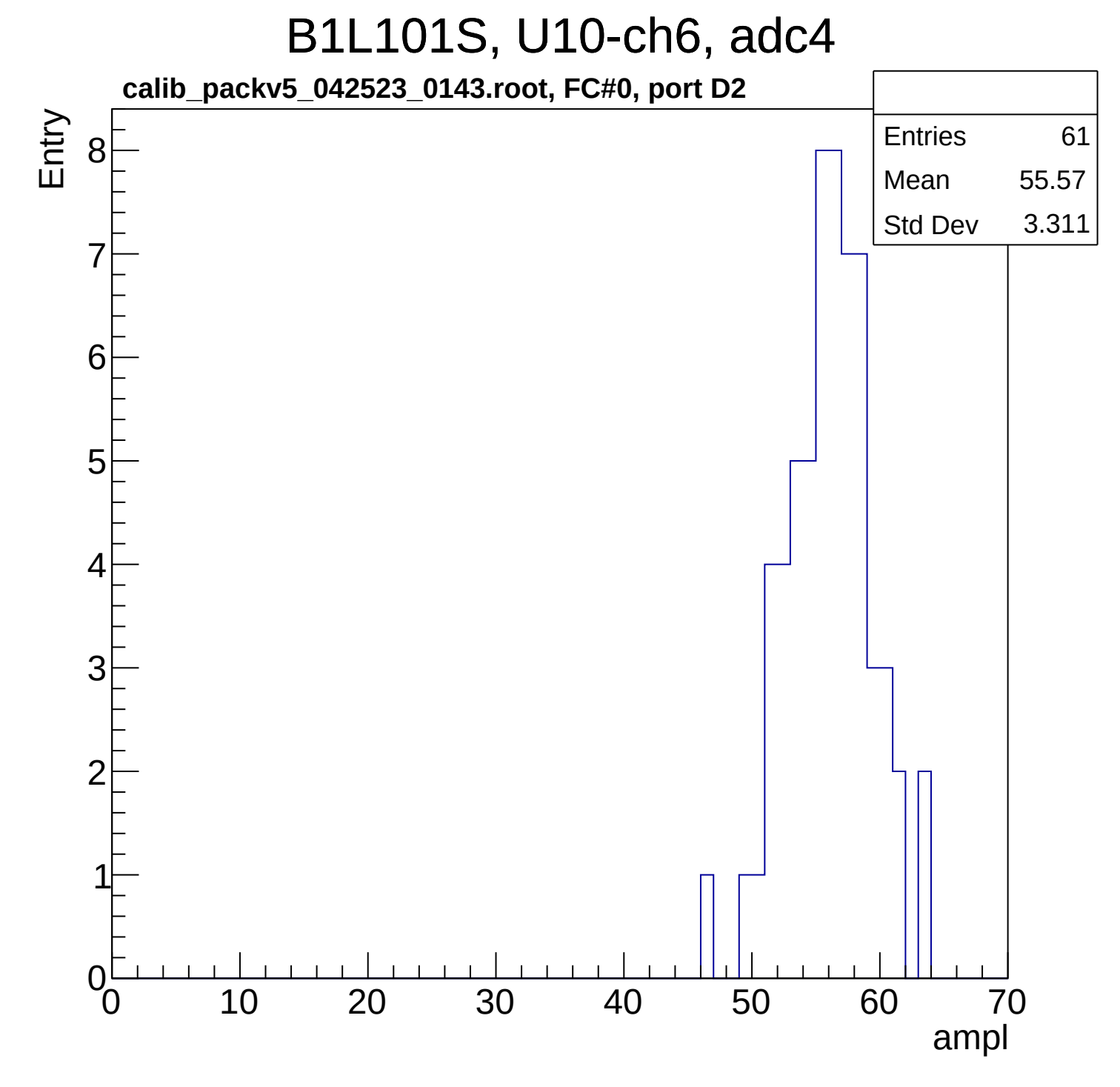
B1L101S, U10-ch6, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 55.57
Std Dev 3.311
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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40
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60
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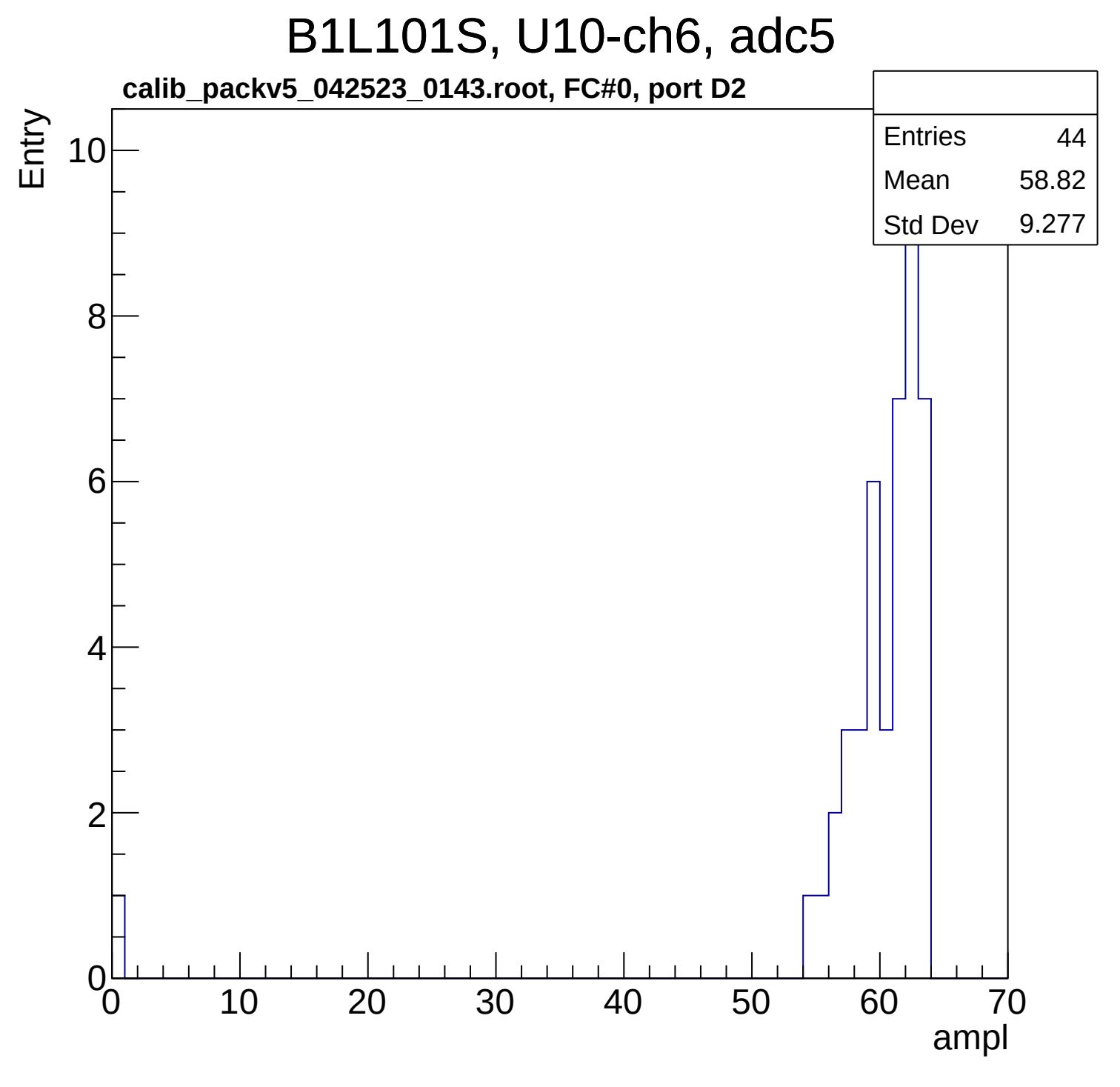
B1L101S, U10-ch6, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 44
Mean 58.82
Std Dev 9.277
Entry
ampl
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4
6
8
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0
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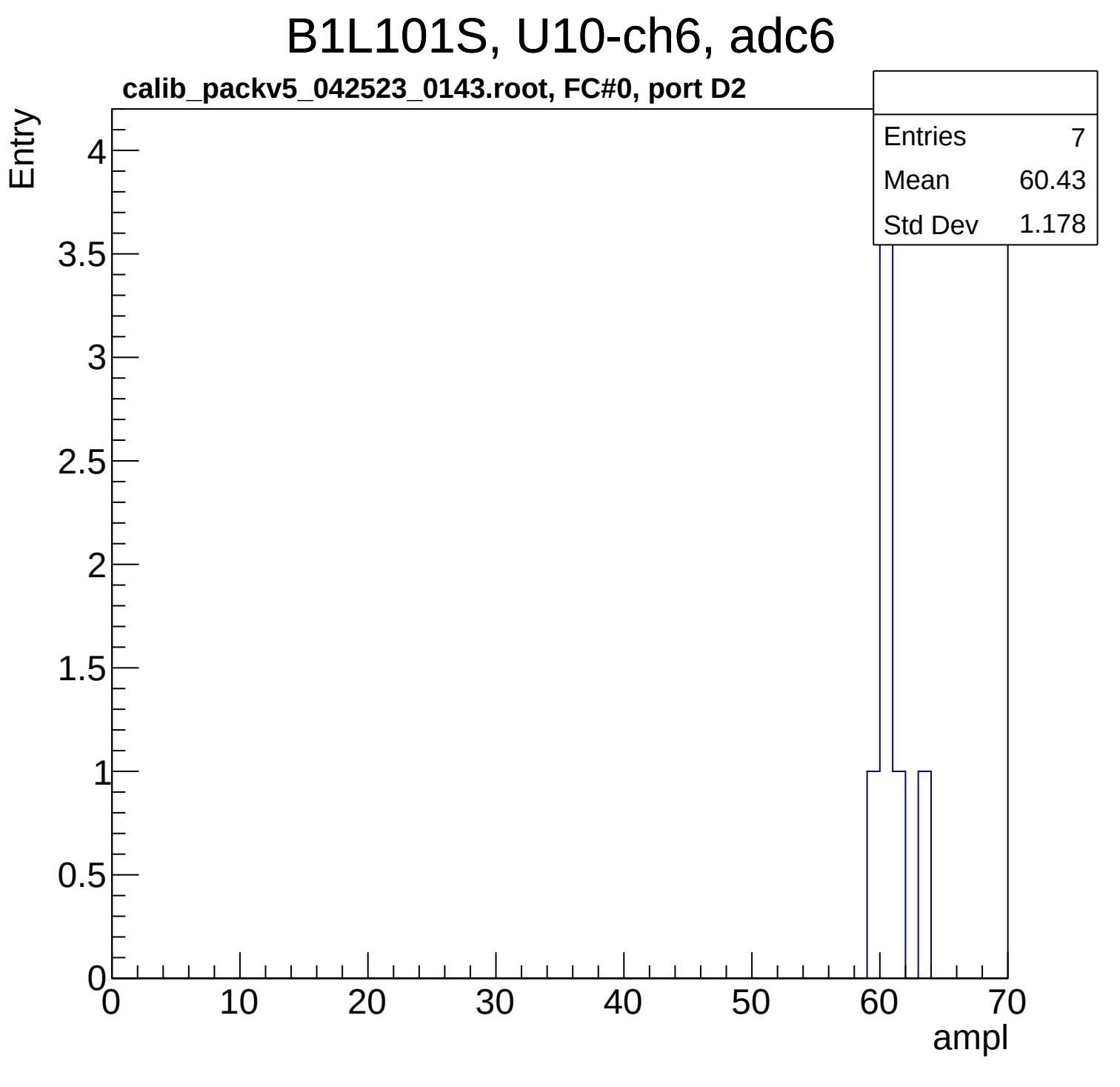
B1L101S, U10-ch6, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 60.43
Std Dev 1.178
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
10
20
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40
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60
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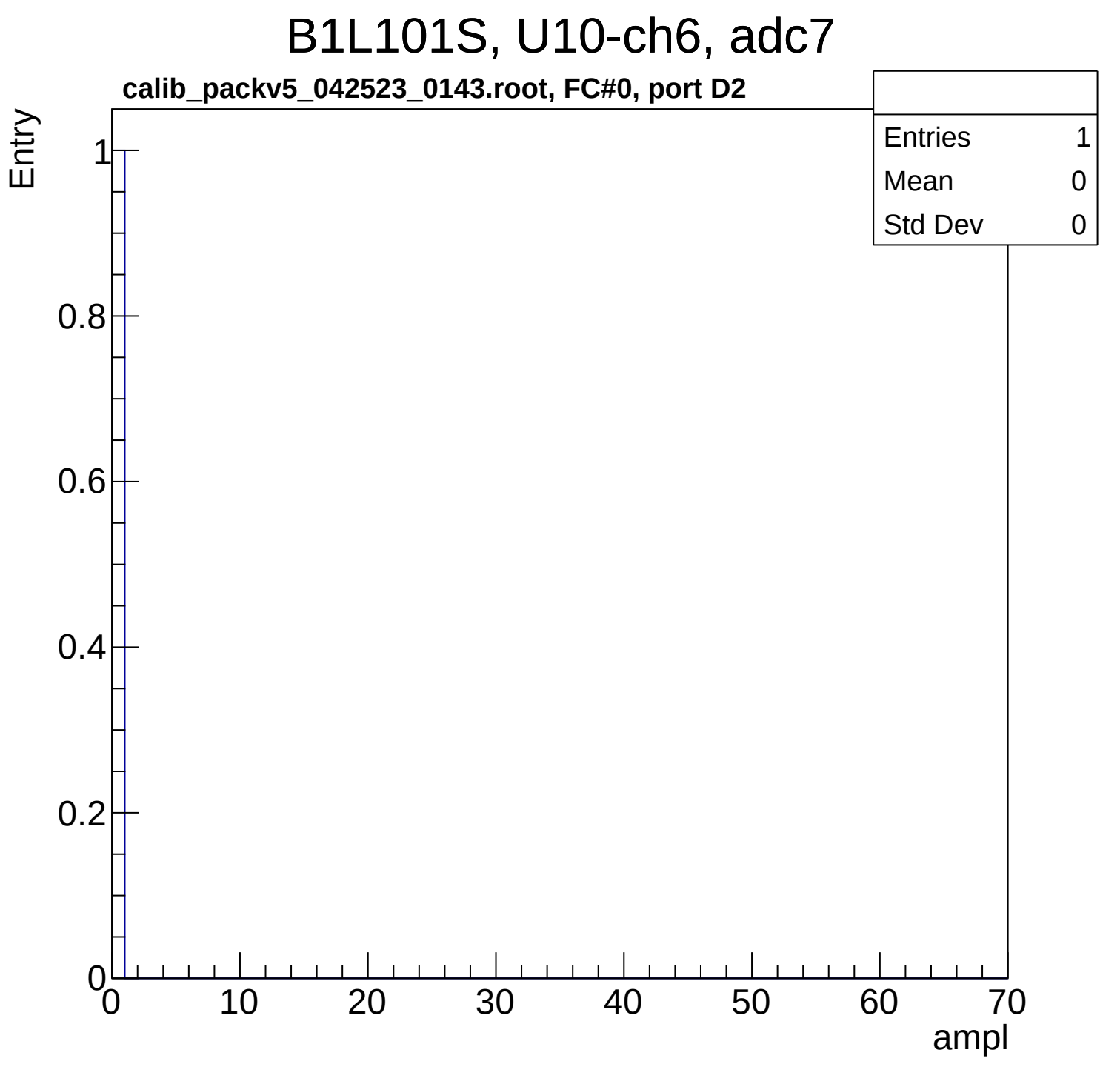
B1L101S, U10-ch6, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
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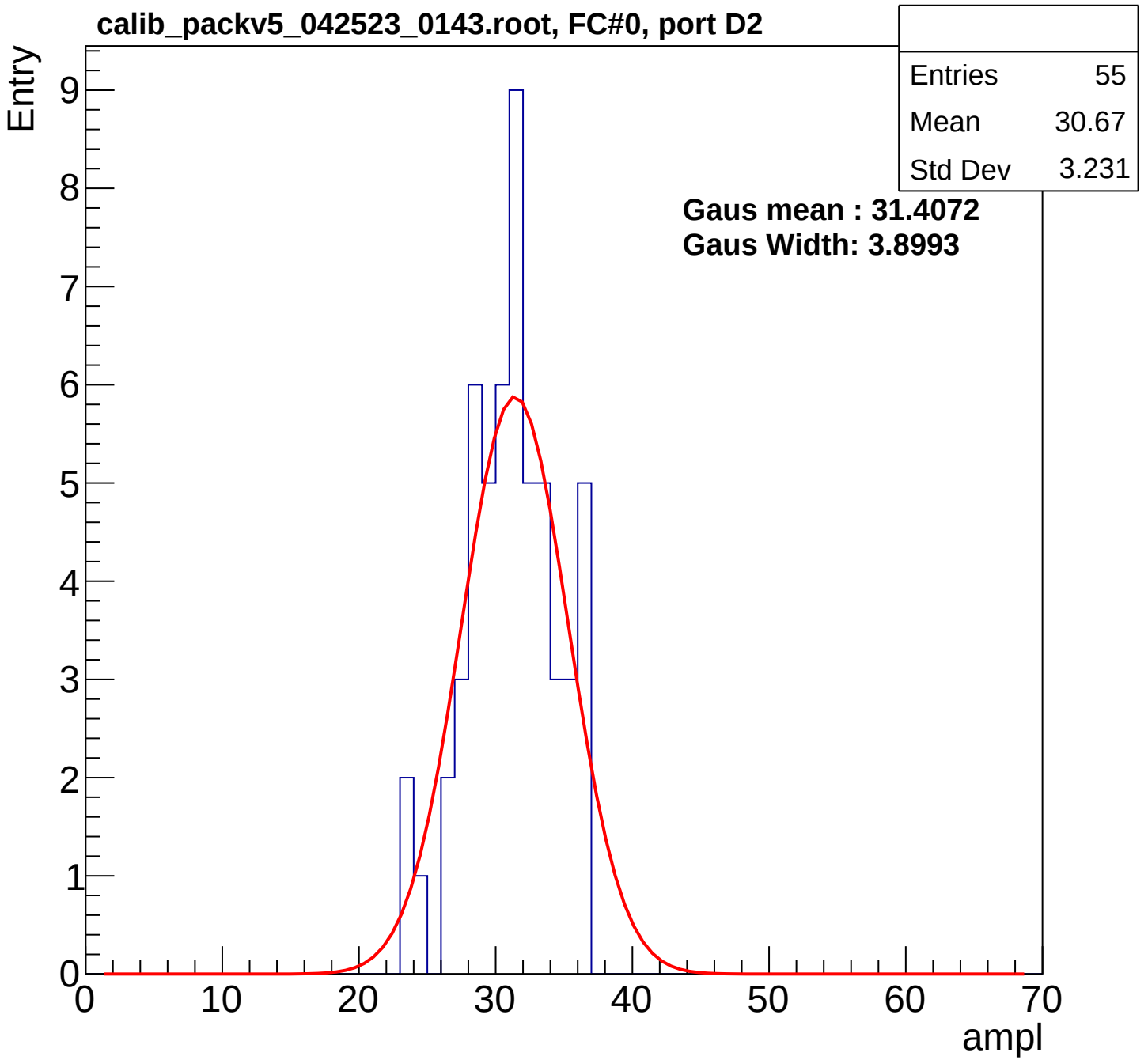
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch7, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 30.67
Std Dev 3.231
Gaus mean : 31.4072
Gaus Width: 3.8993
Entry
ampl
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2
3
4
5
6
7
8
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0
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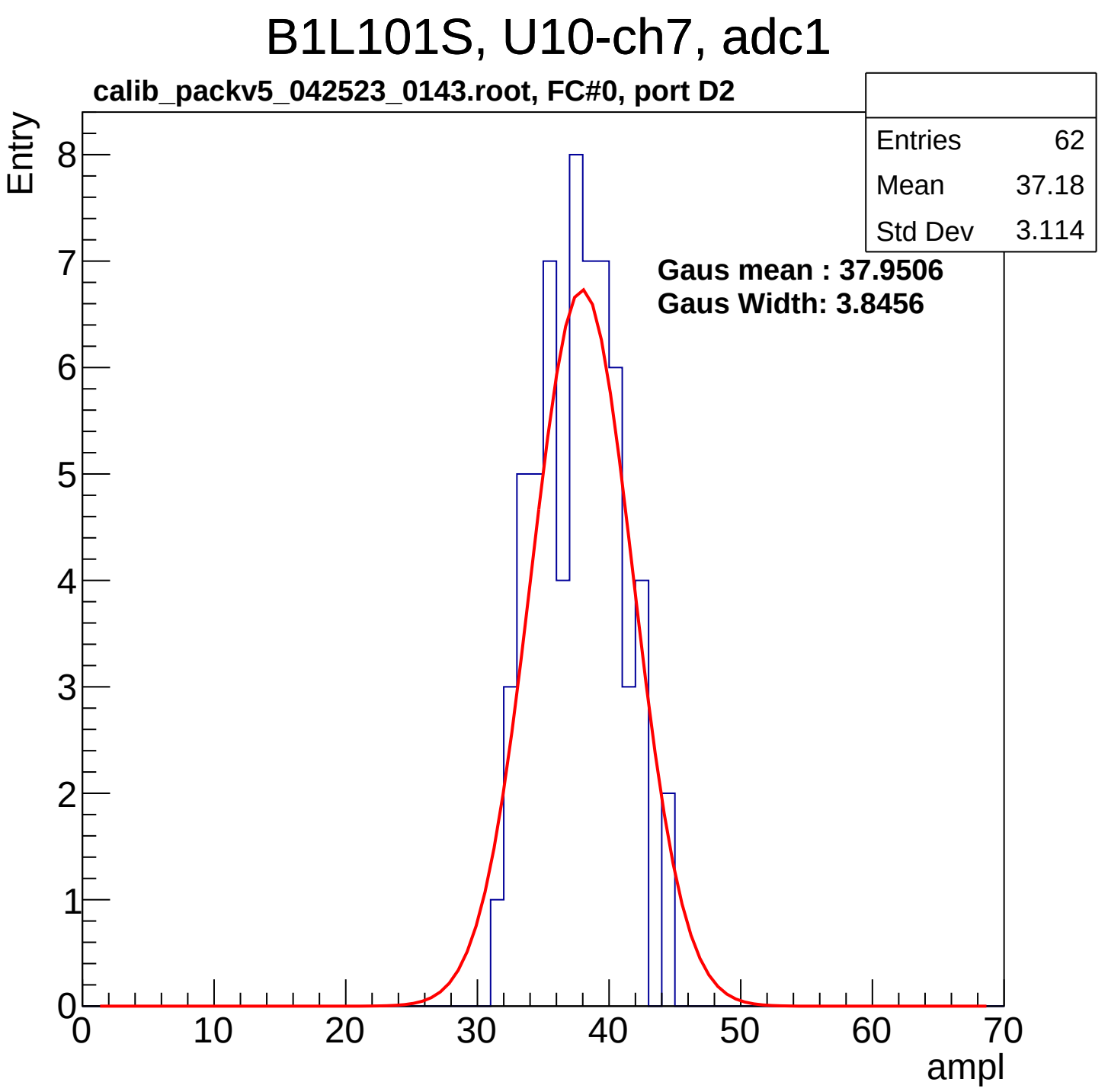
B1L101S, U10-ch7, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 37.18
Std Dev 3.114
Gaus mean : 37.9506
Gaus Width: 3.8456
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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60
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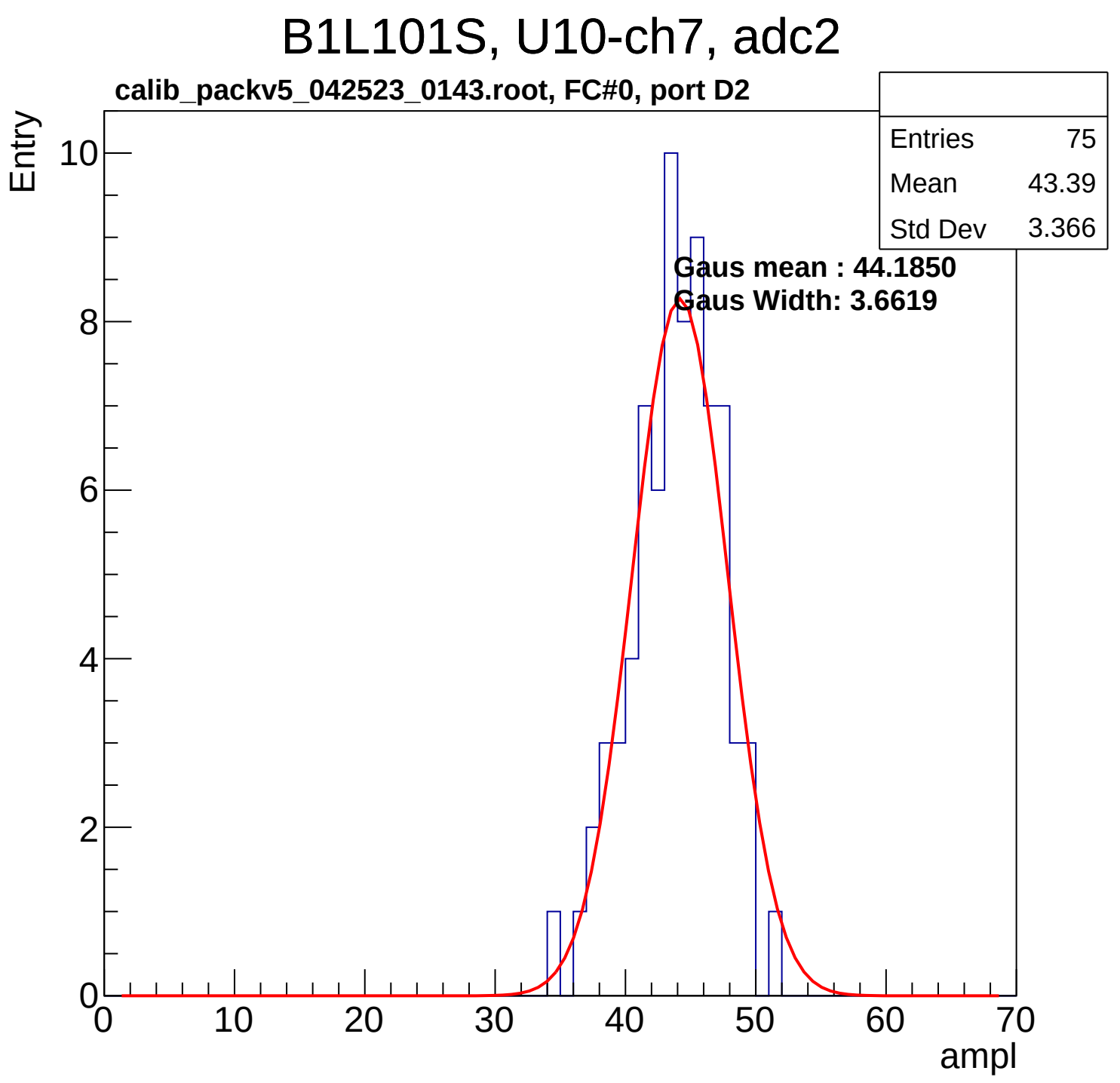
B1L101S, U10-ch7, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 43.39
Std Dev 3.366
Gaus mean : 44.1850
Gaus Width: 3.6619
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
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60
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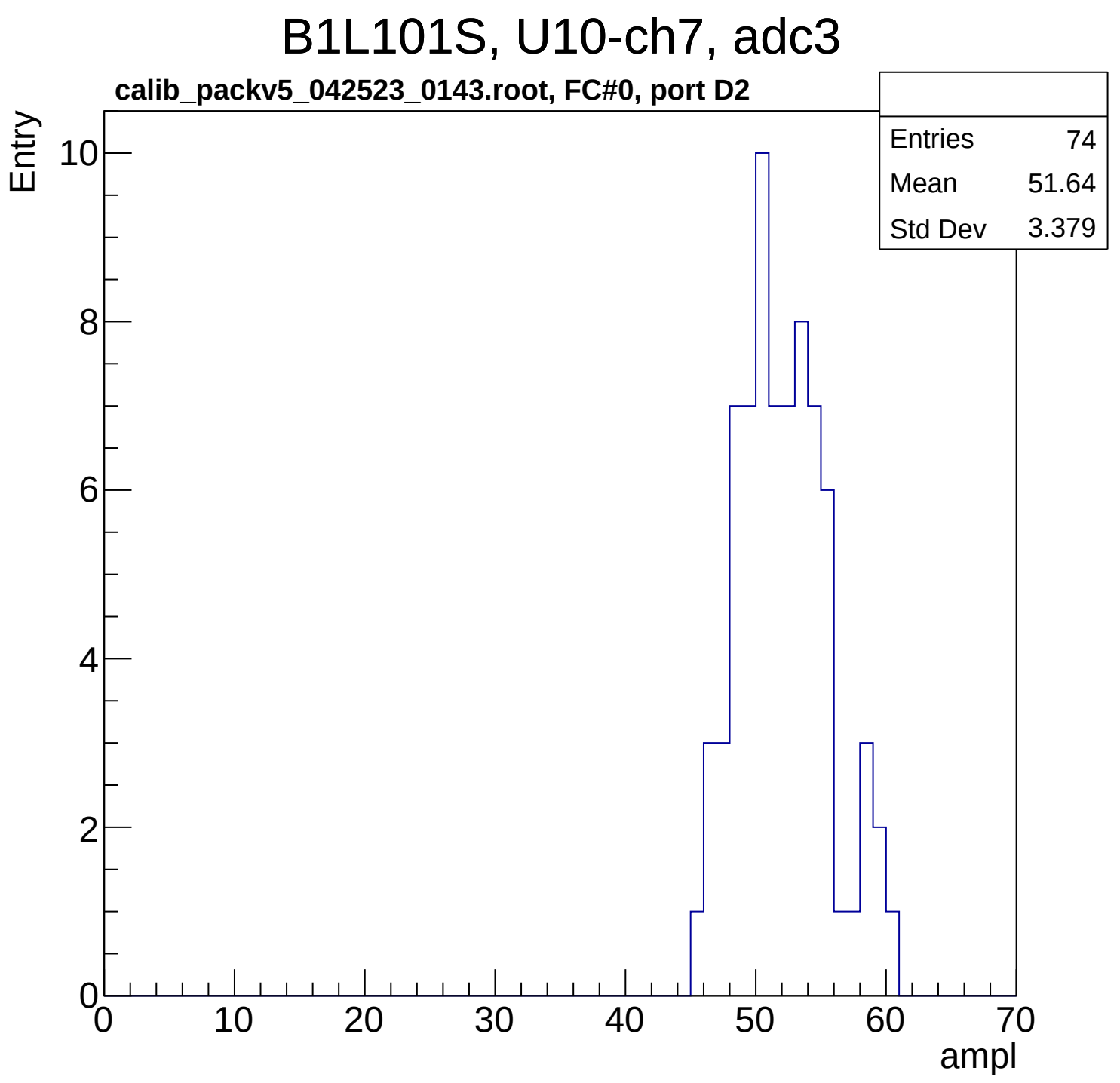
B1L101S, U10-ch7, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 51.64
Std Dev 3.379
Entry
ampl
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4
6
8
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0
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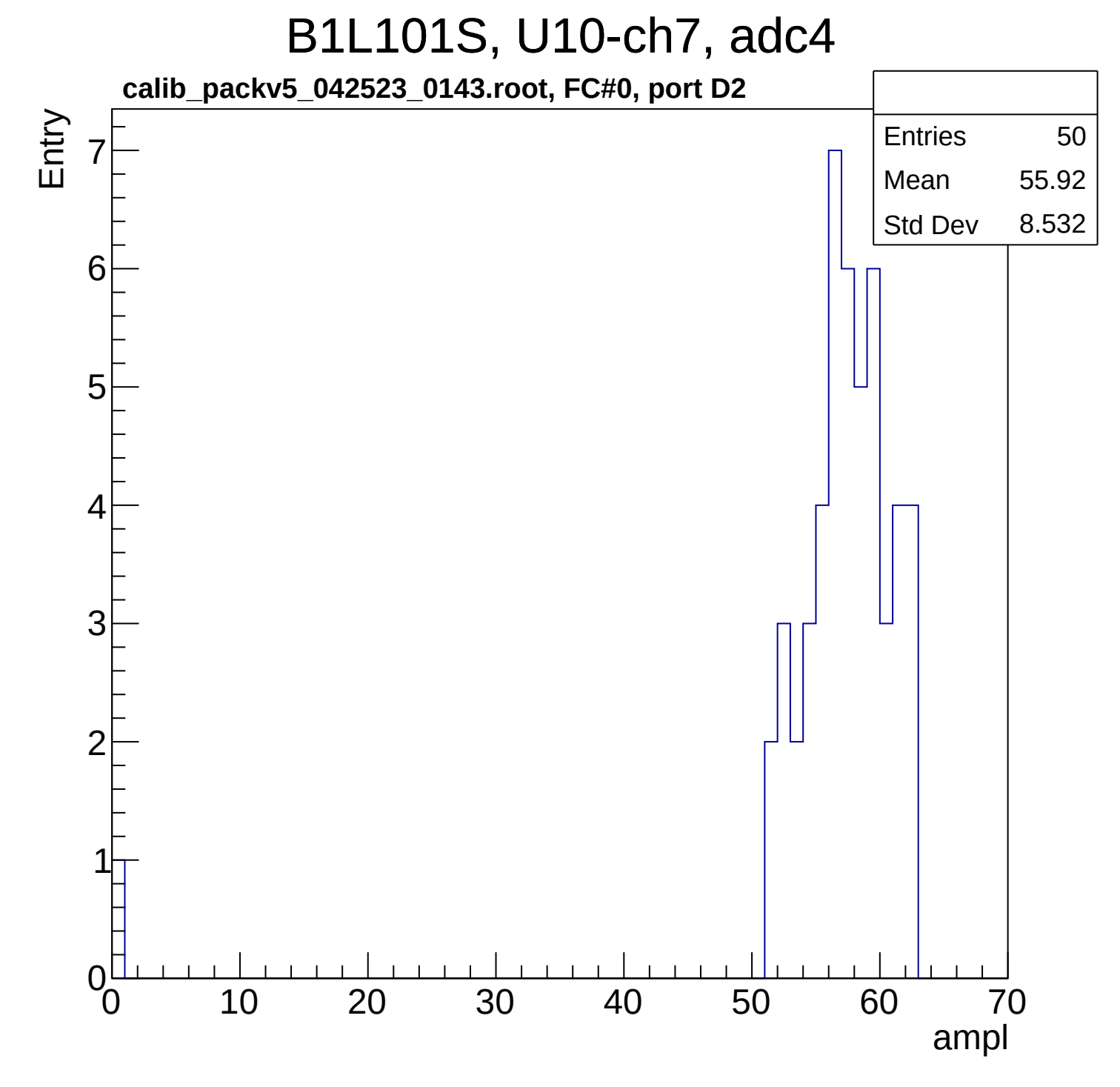
B1L101S, U10-ch7, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 55.92
Std Dev 8.532
Entry
ampl
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3
4
5
6
7
0
10
20
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40
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60
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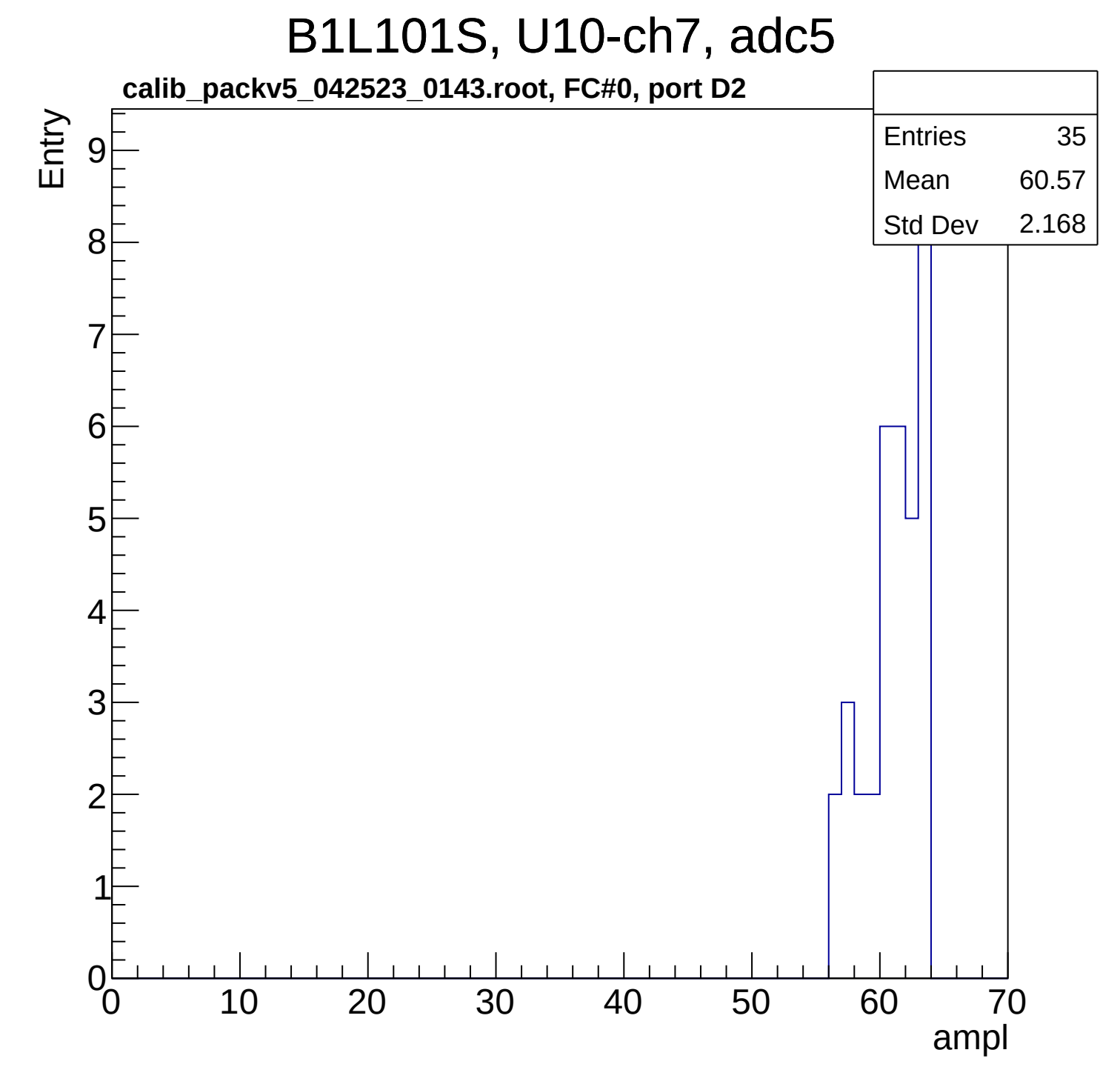
B1L101S, U10-ch7, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 35
Mean 60.57
Std Dev 2.168
Entry
ampl
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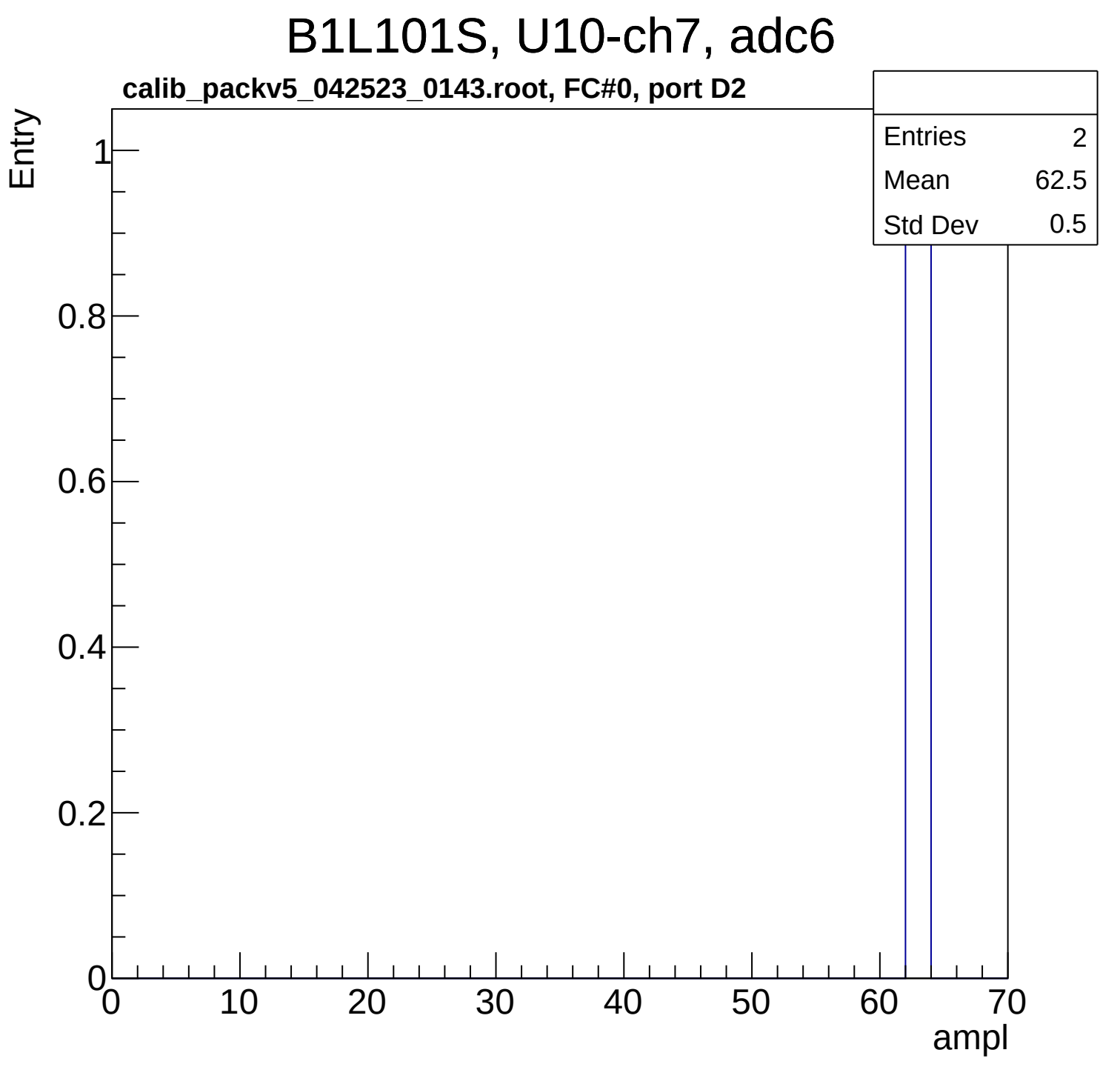
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch7, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
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0.6
0.4
0.2
0
0
10
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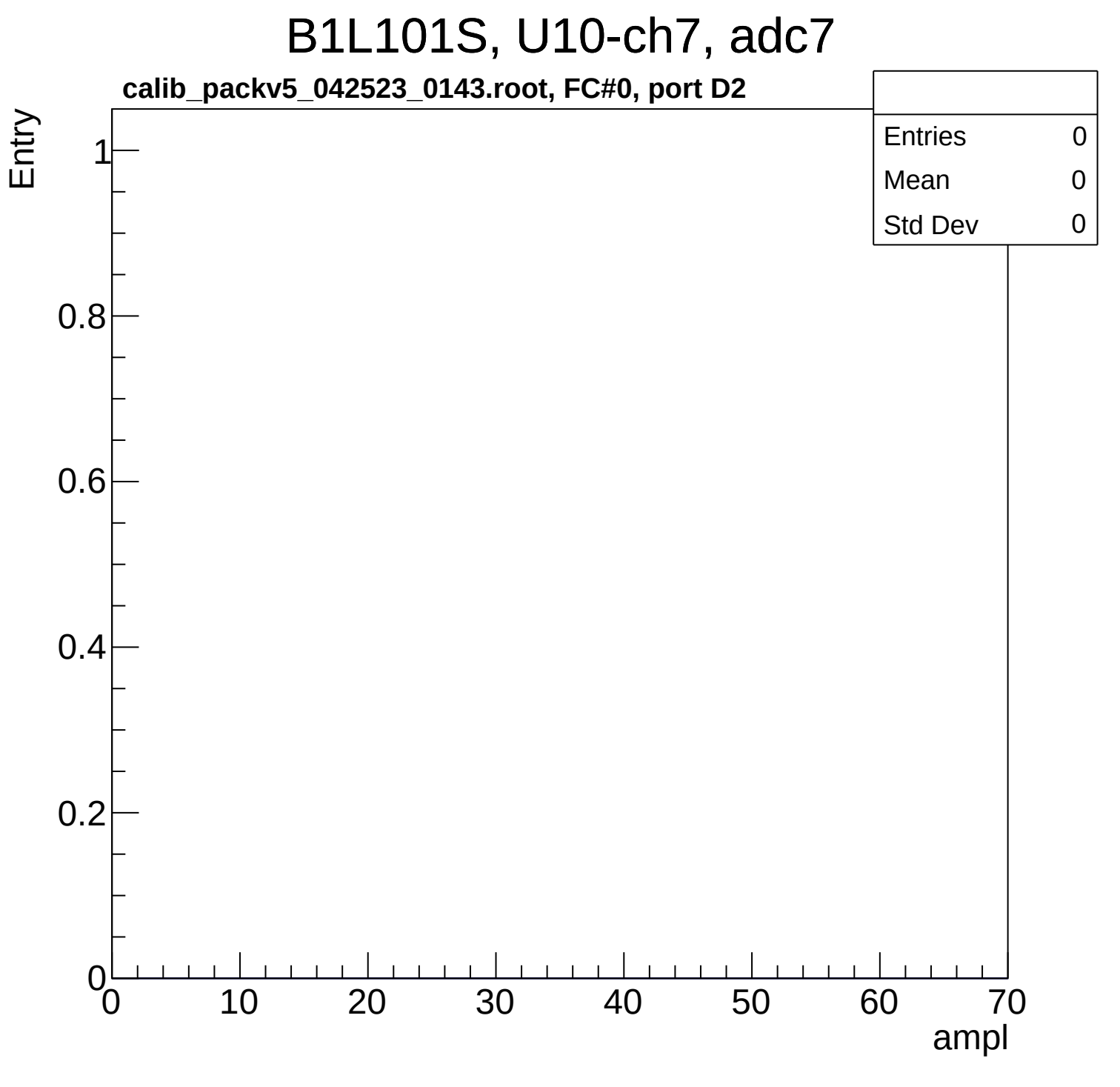
70
ampl


B1L101S, U10-ch7, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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0.6
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10
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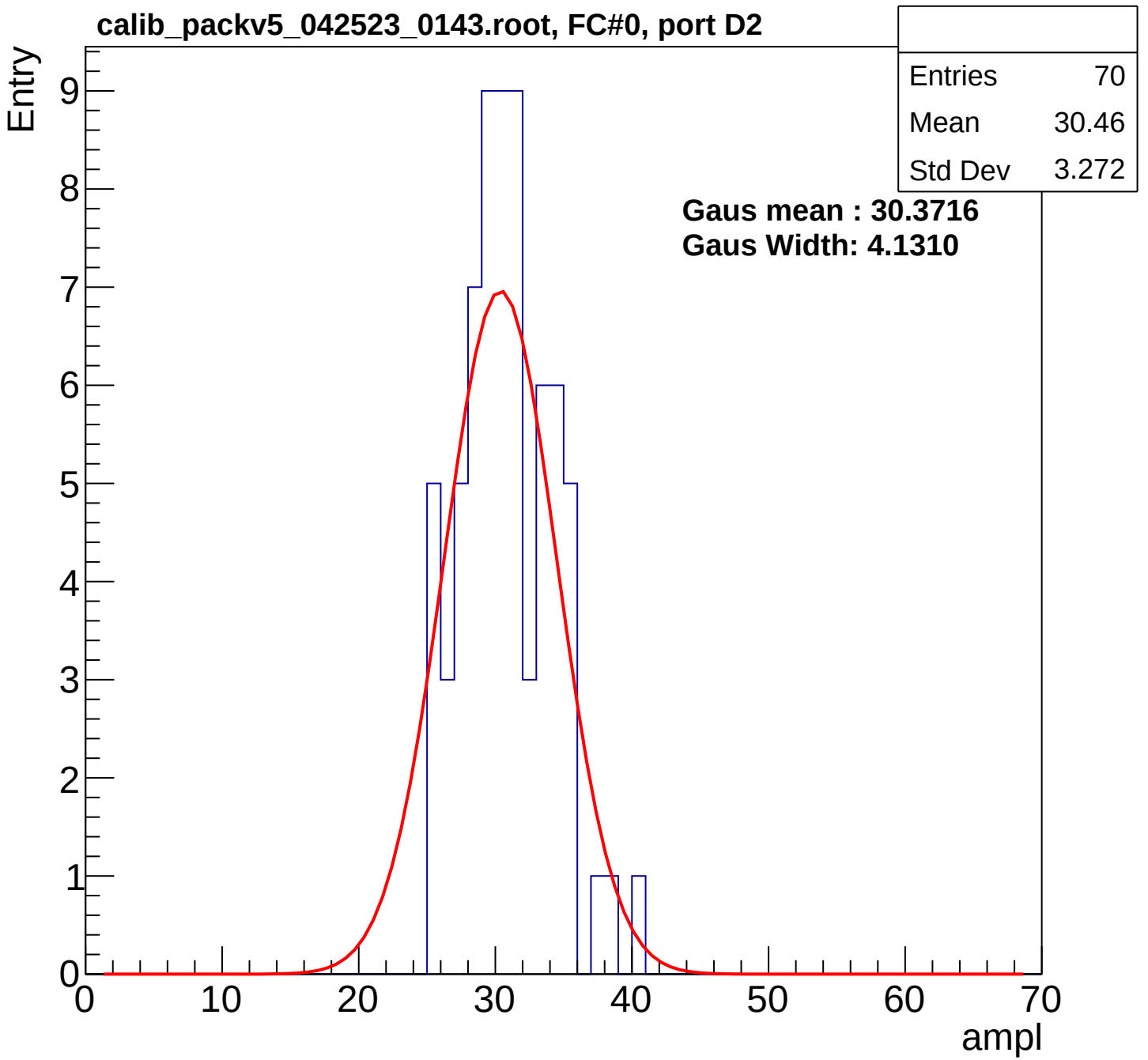
70
ampl


B1L101S, U10-ch8, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 30.46
Std Dev 3.272
Gaus mean : 30.3716
Gaus Width: 4.1310
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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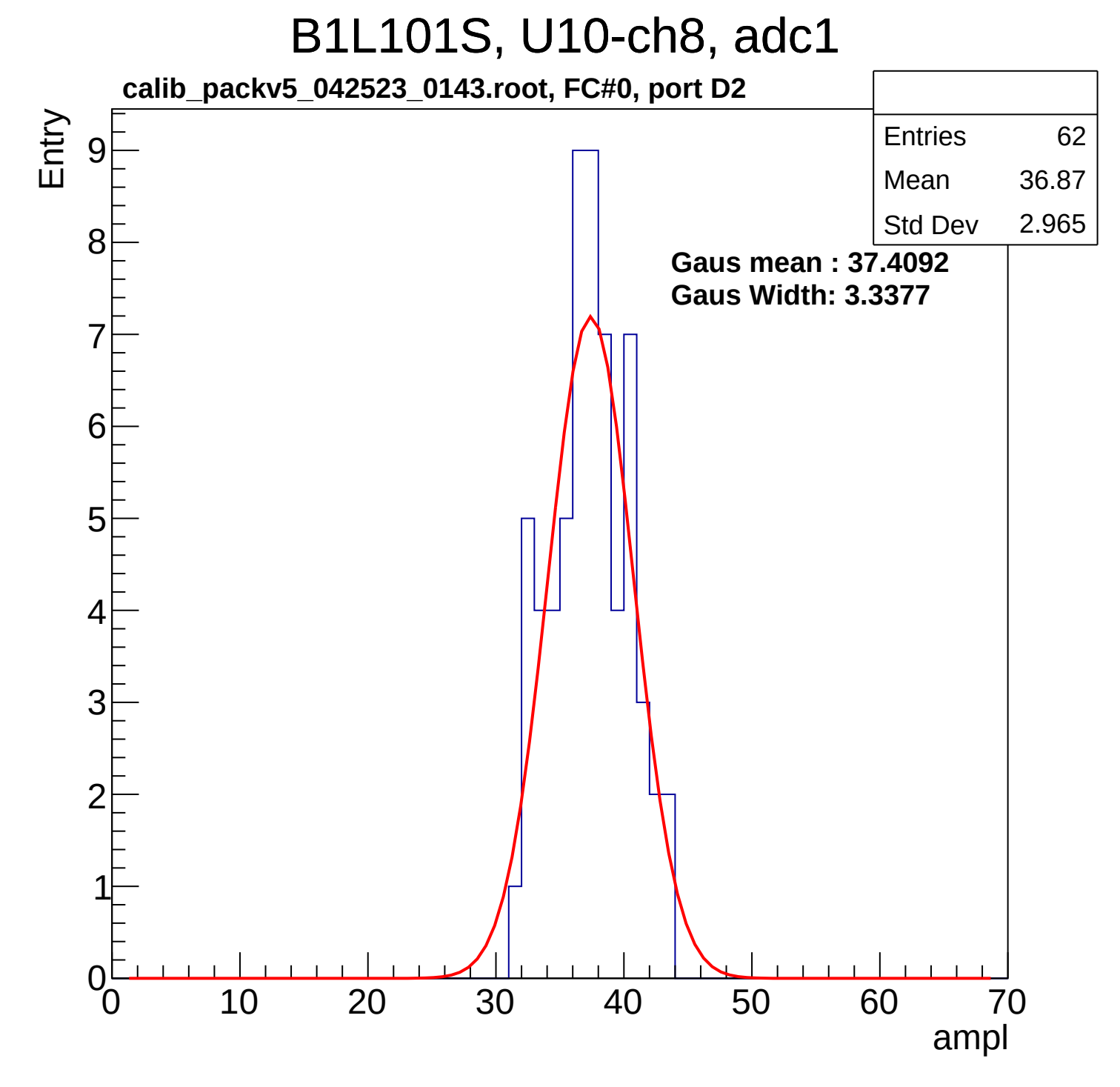
B1L101S, U10-ch8, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 36.87
Std Dev 2.965
Gaus mean : 37.4092
Gaus Width: 3.3377
Entry
ampl
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10
20
30
40
50
60
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1
2
3
4
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6
7
8
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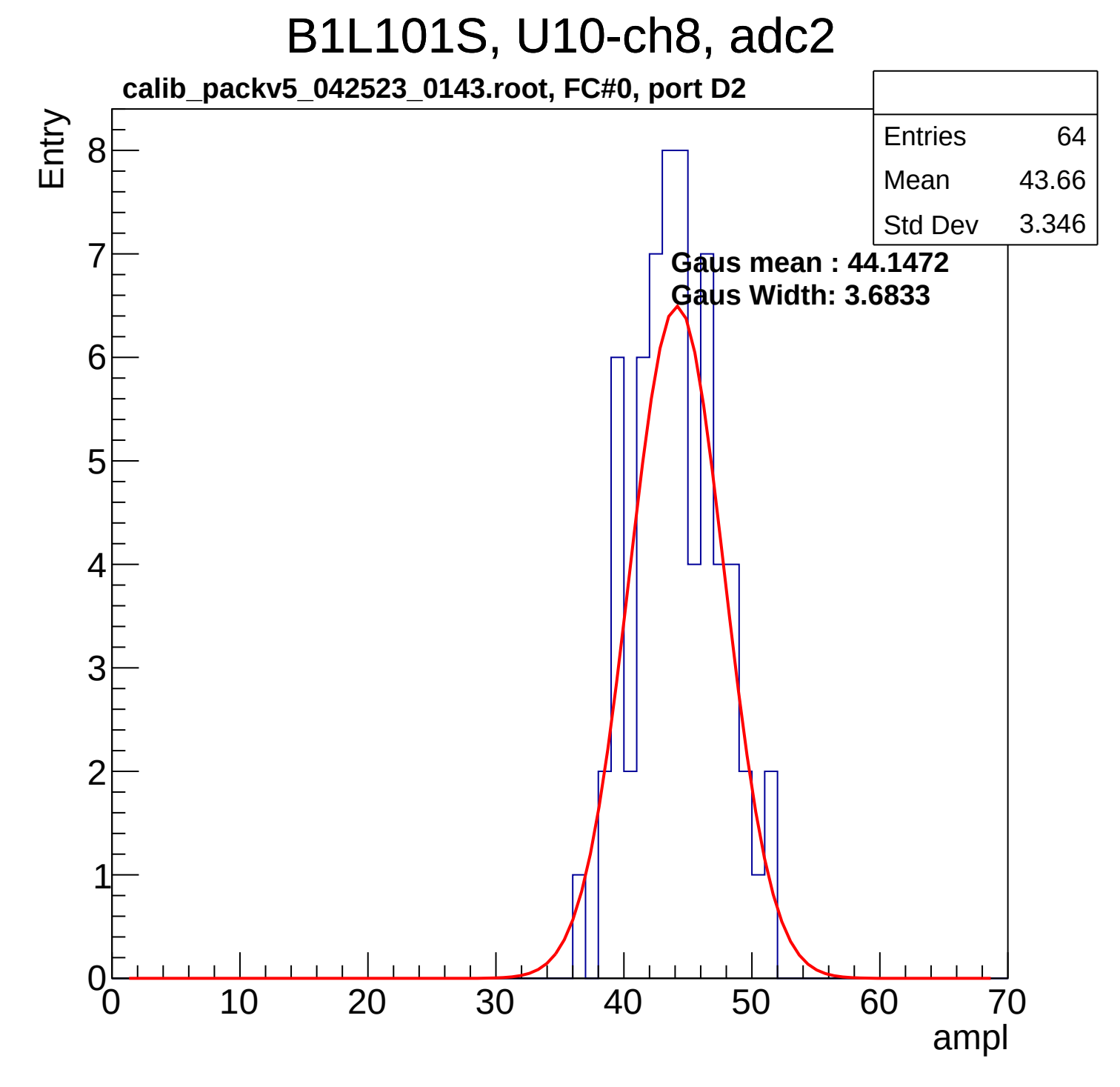
B1L101S, U10-ch8, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 43.66
Std Dev 3.346
Gaus mean : 44.1472
Gaus Width: 3.6833
Entry
ampl
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1
2
3
4
5
6
7
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0
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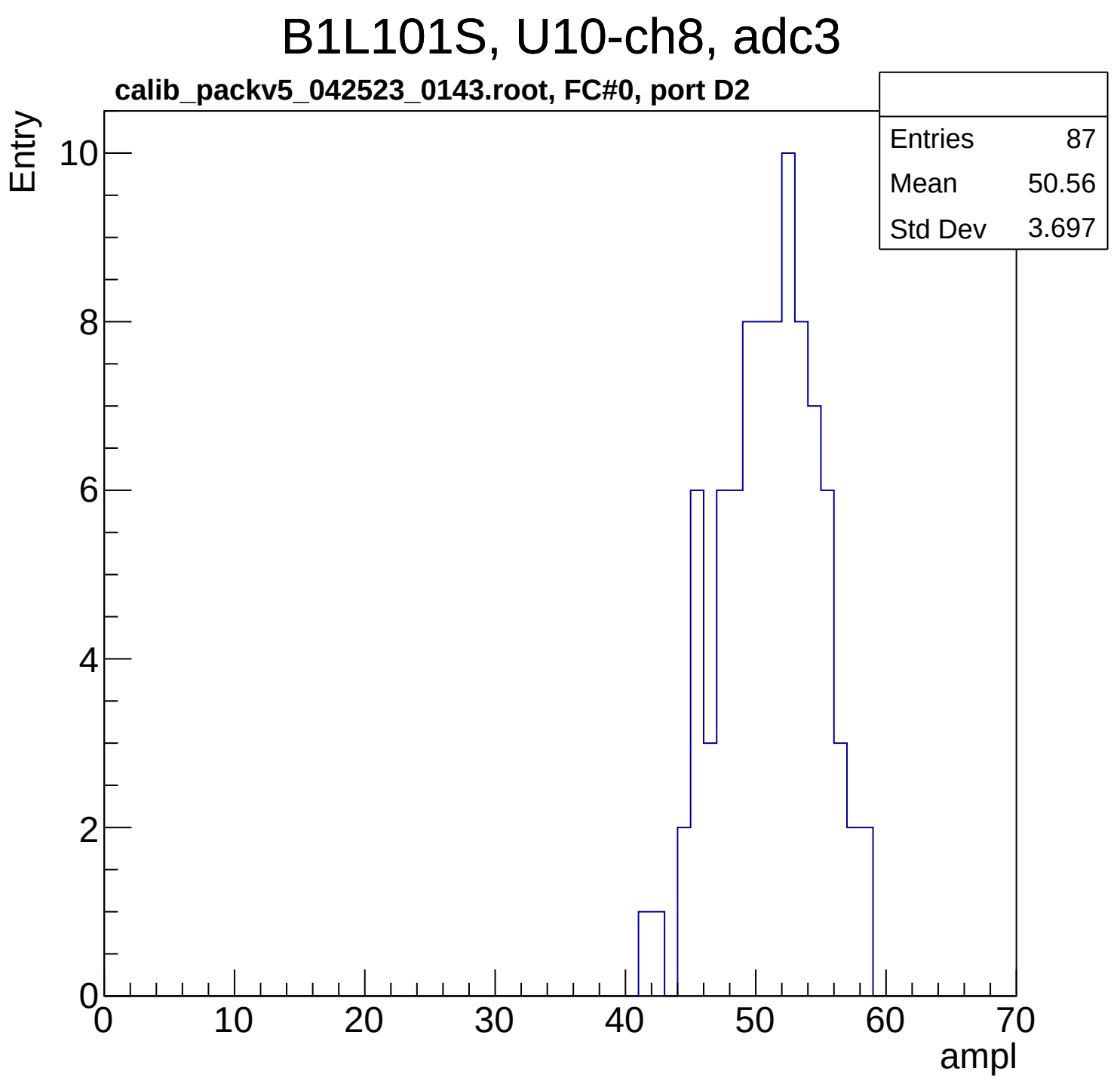
B1L101S, U10-ch8, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 87
Mean 50.56
Std Dev 3.697
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
50
60
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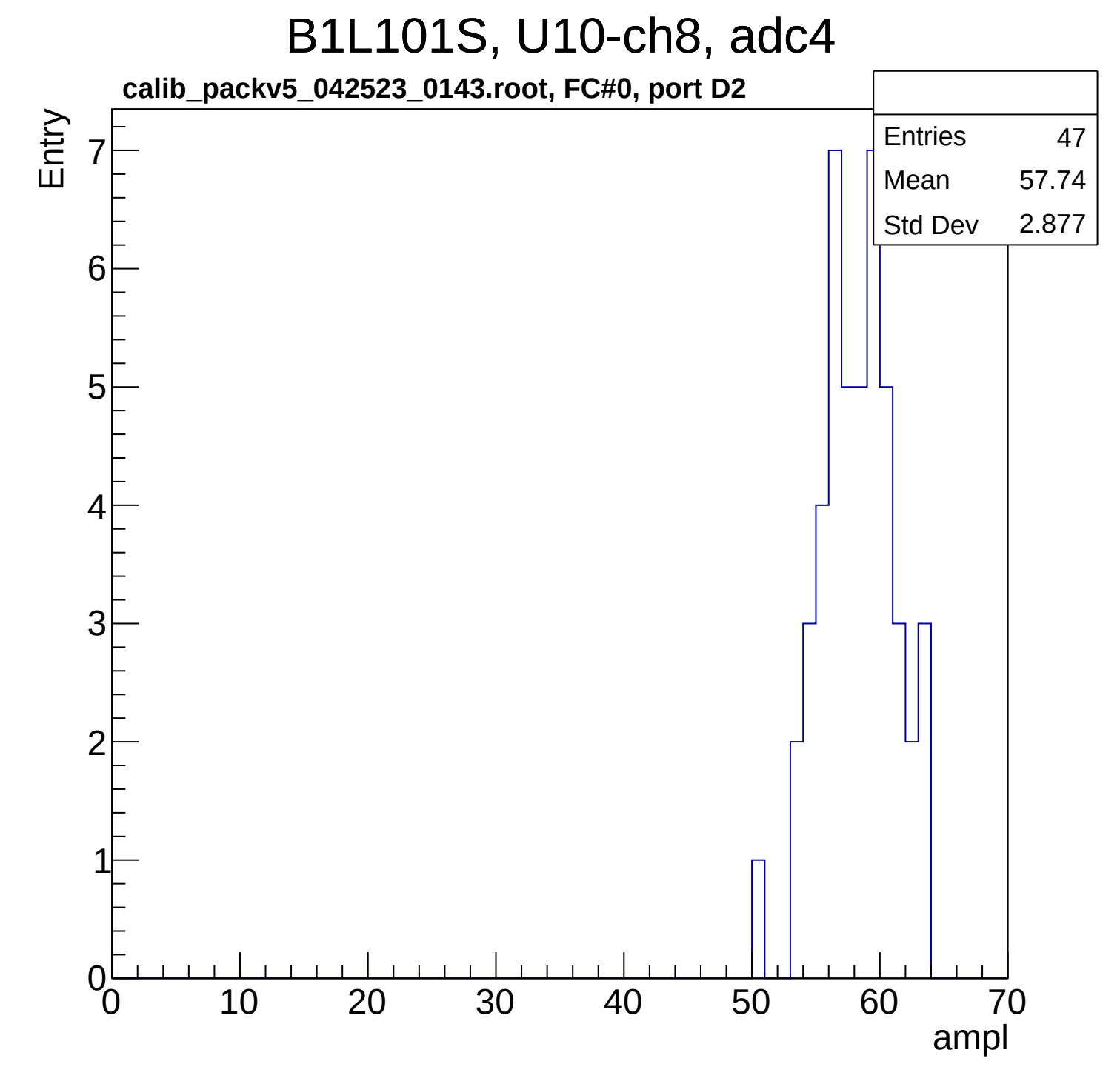
B1L101S, U10-ch8, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 57.74
Std Dev 2.877
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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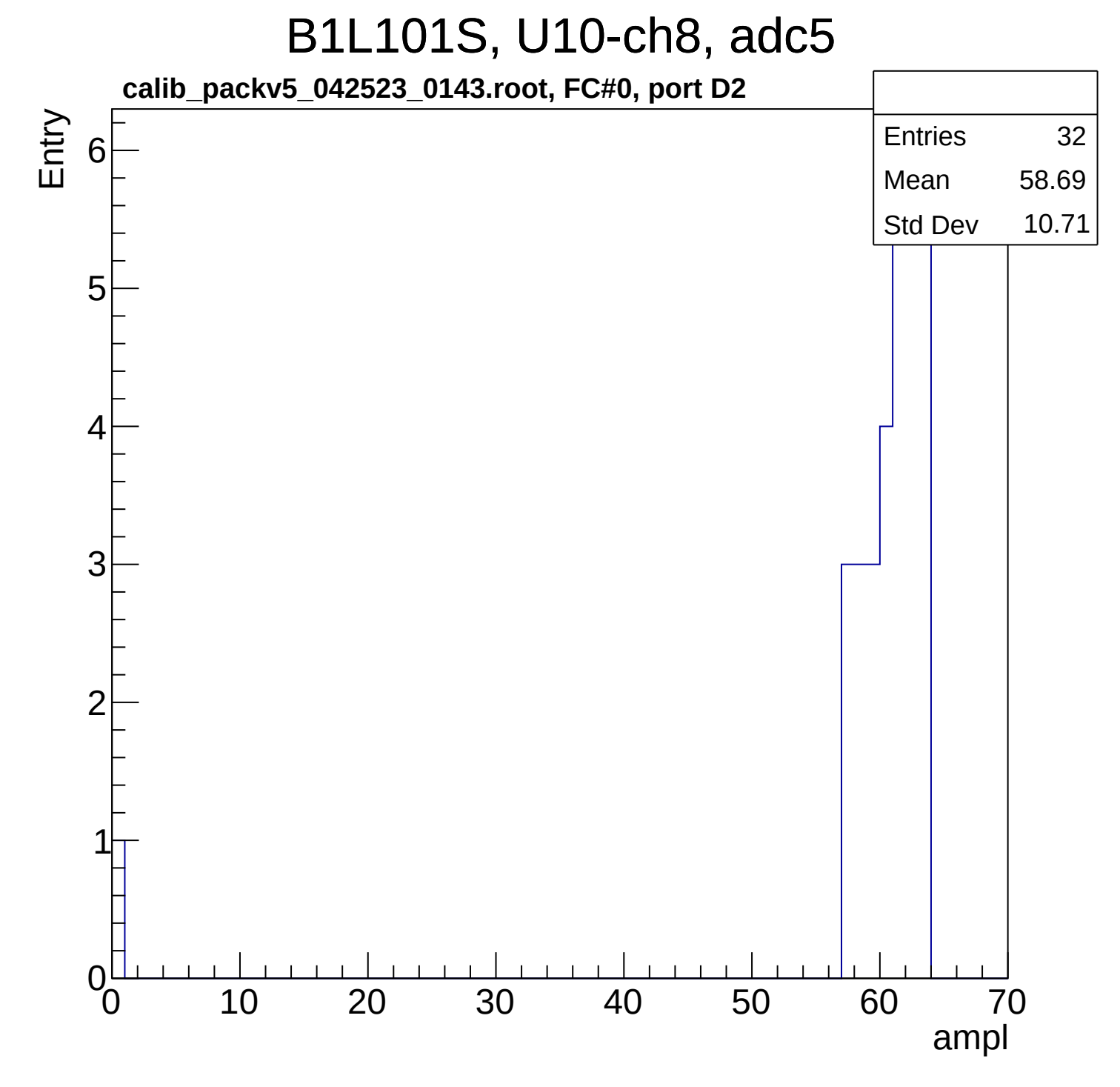
B1L101S, U10-ch8, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 32
Mean 58.69
Std Dev 10.71
Entry
ampl
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1
2
3
4
5
6
0
10
20
30
40
50
60
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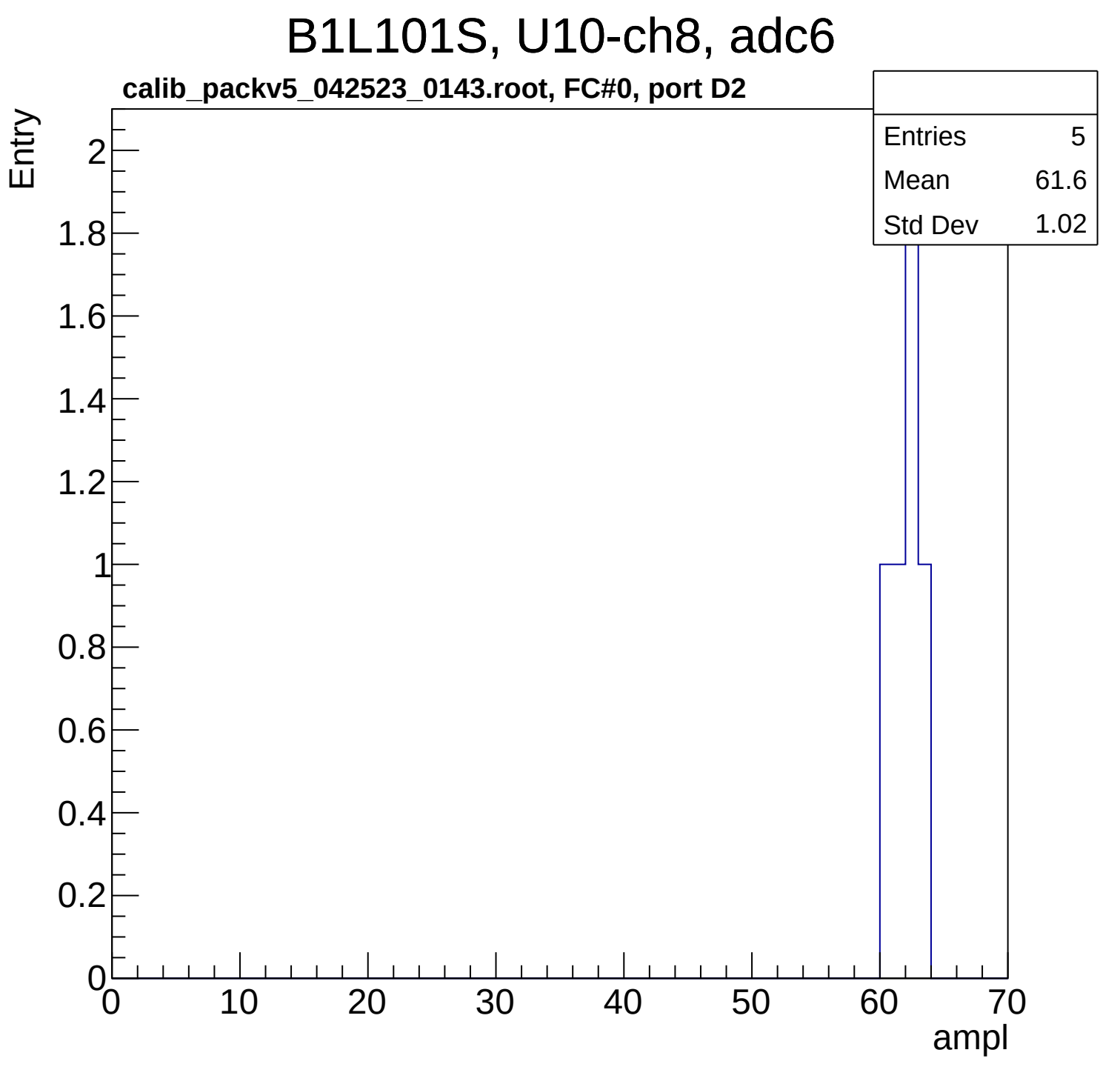
B1L101S, U10-ch8, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 61.6
Std Dev 1.02
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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20
30
40
50
60
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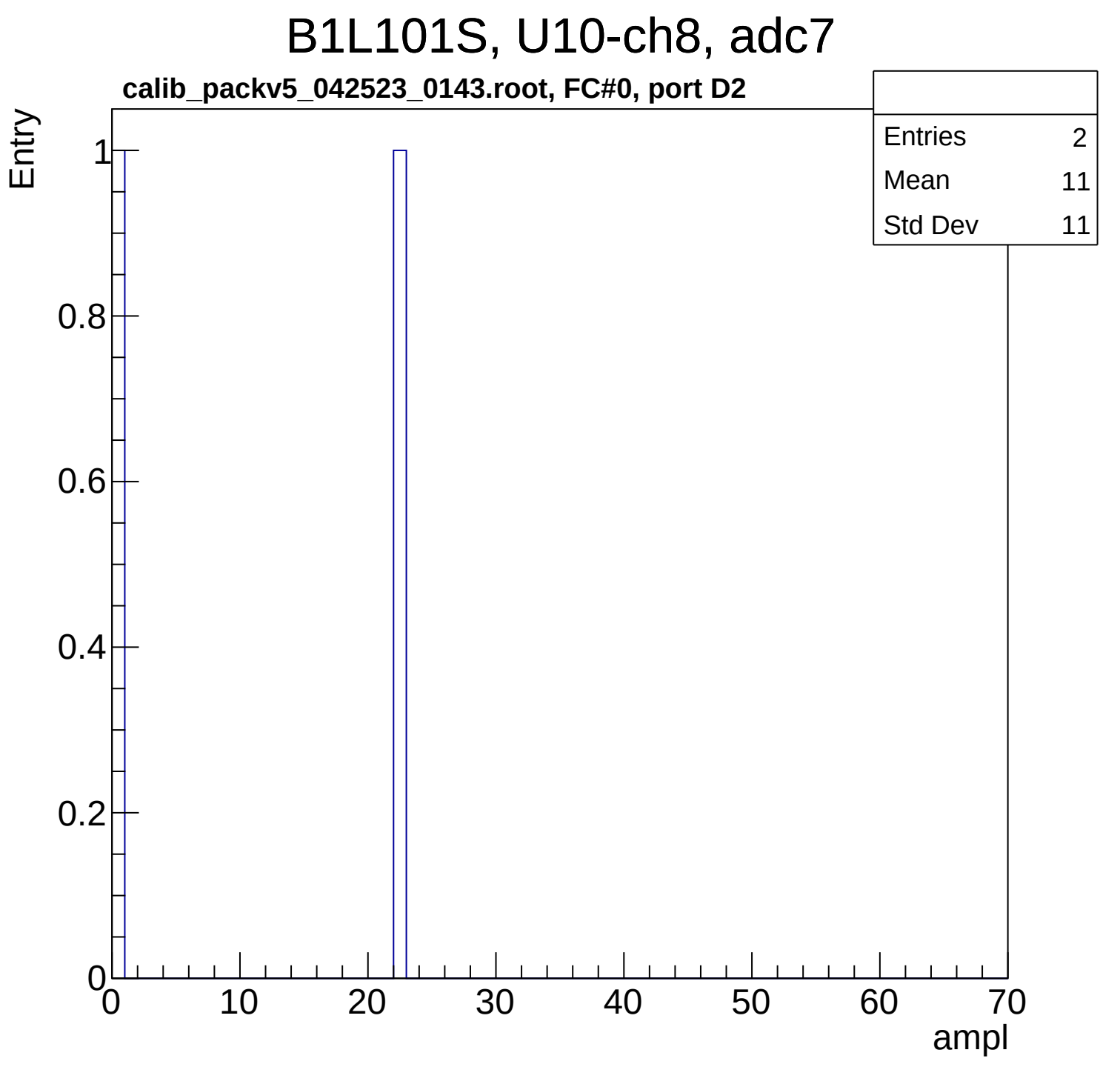
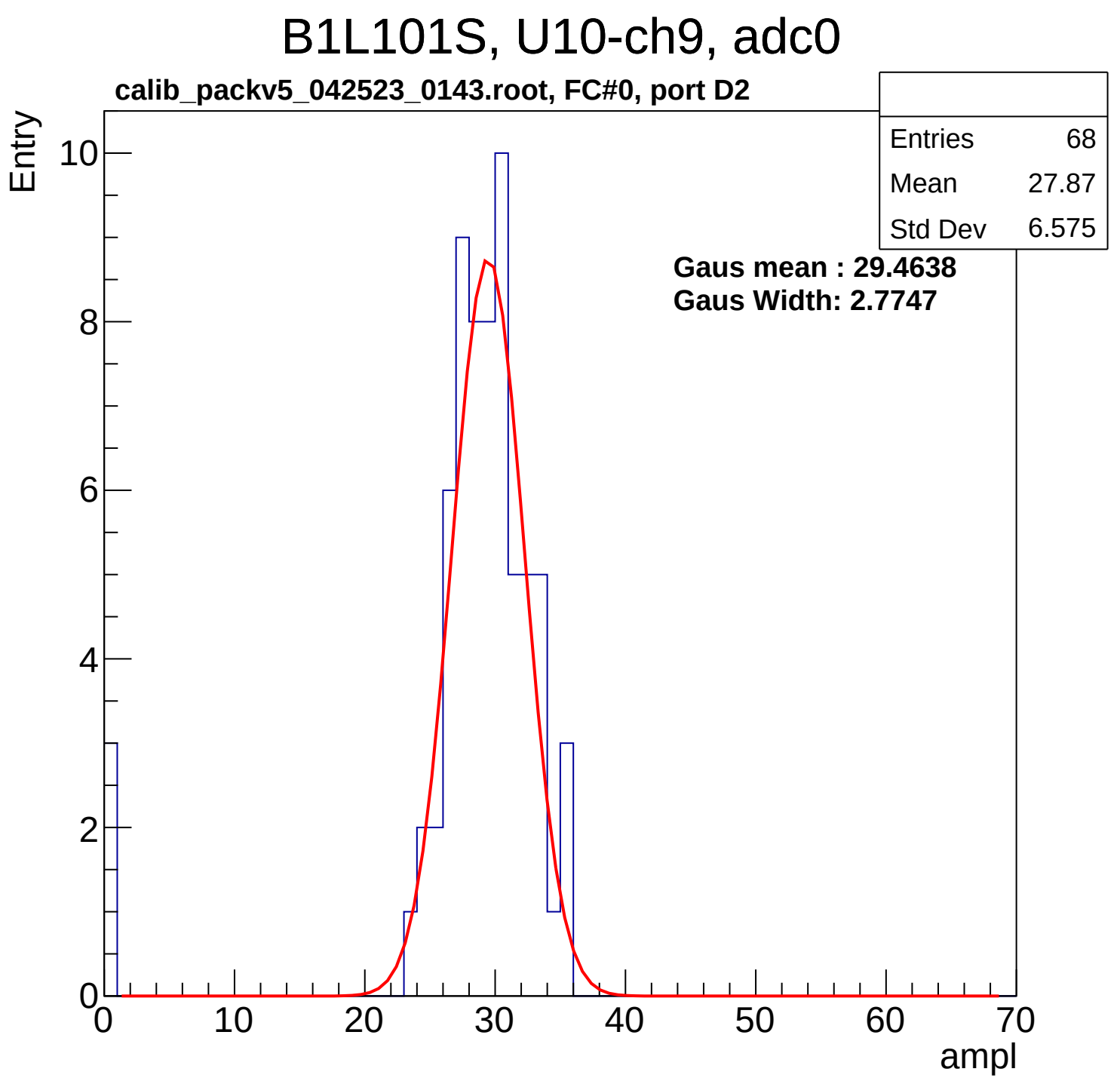
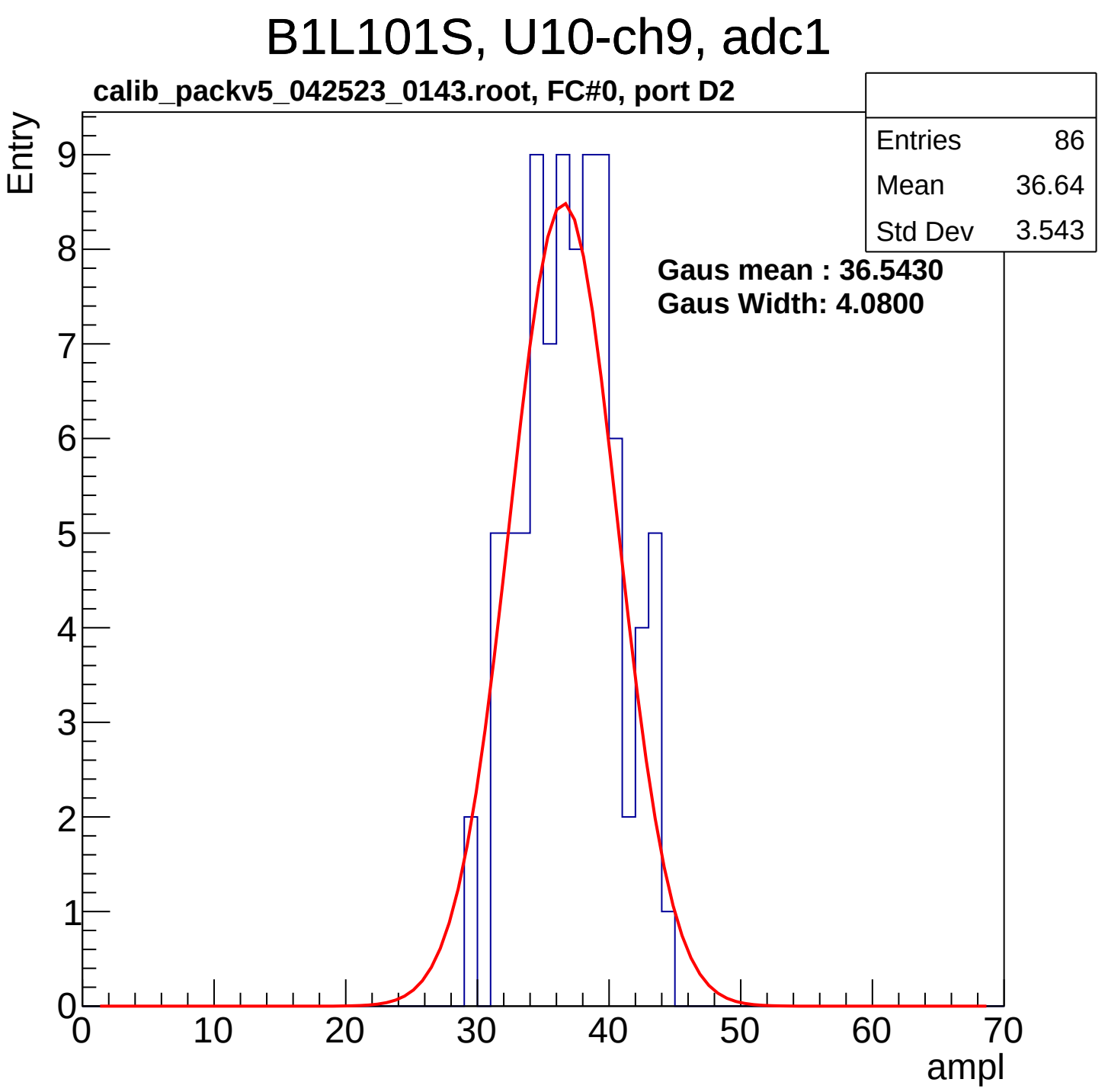
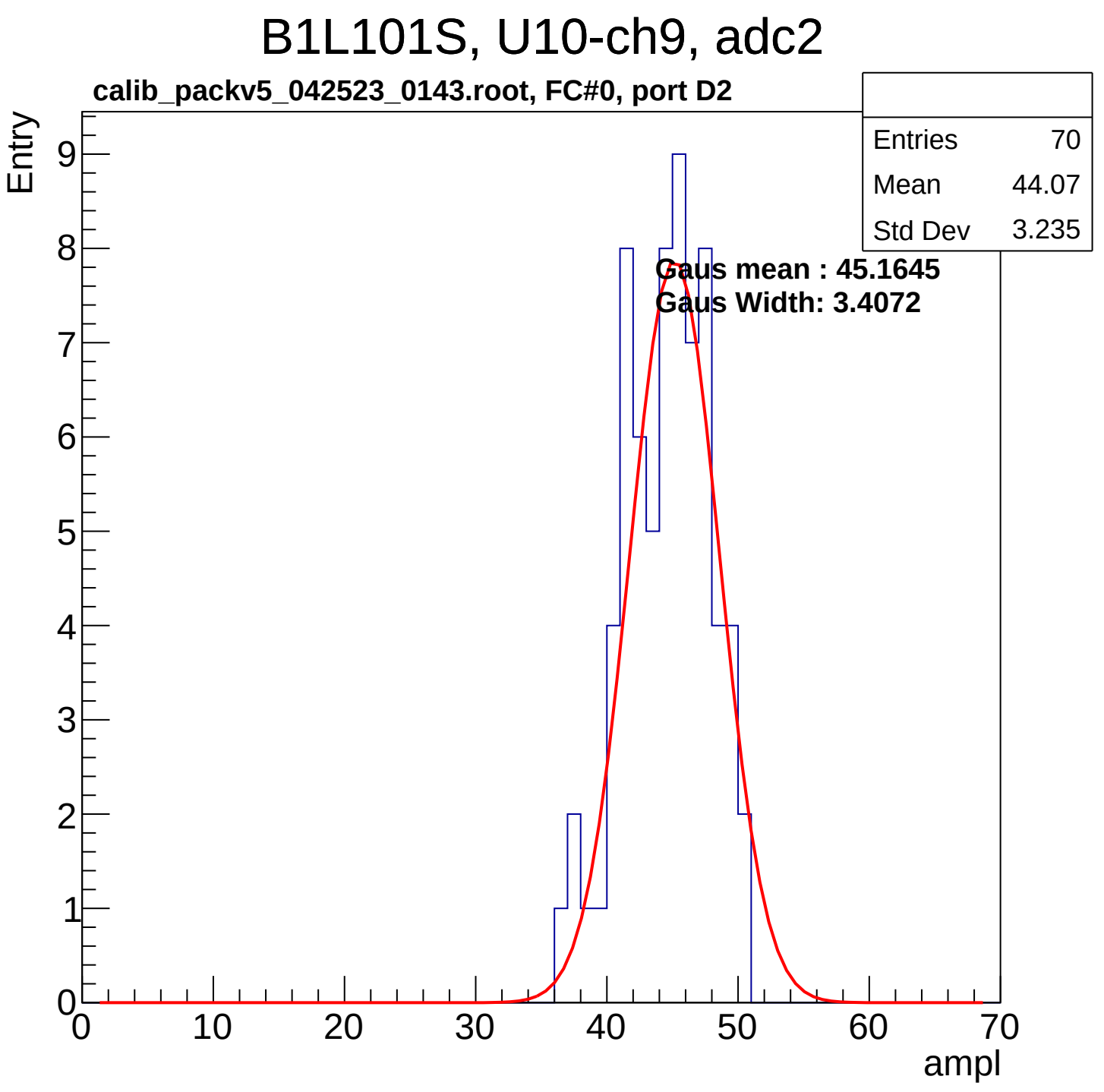

B1L101S, U10-ch8, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 11
Std Dev 11
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch9, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 27.87
Std Dev 6.575
Gaus mean : 29.4638
Gaus Width: 2.7747
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch9, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 86
Mean 36.64
Std Dev 3.543
Gaus mean : 36.5430
Gaus Width: 4.0800
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L101S, U10-ch9, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 44.07
Std Dev 3.235
Gaus mean : 45.1645
Gaus Width: 3.4072
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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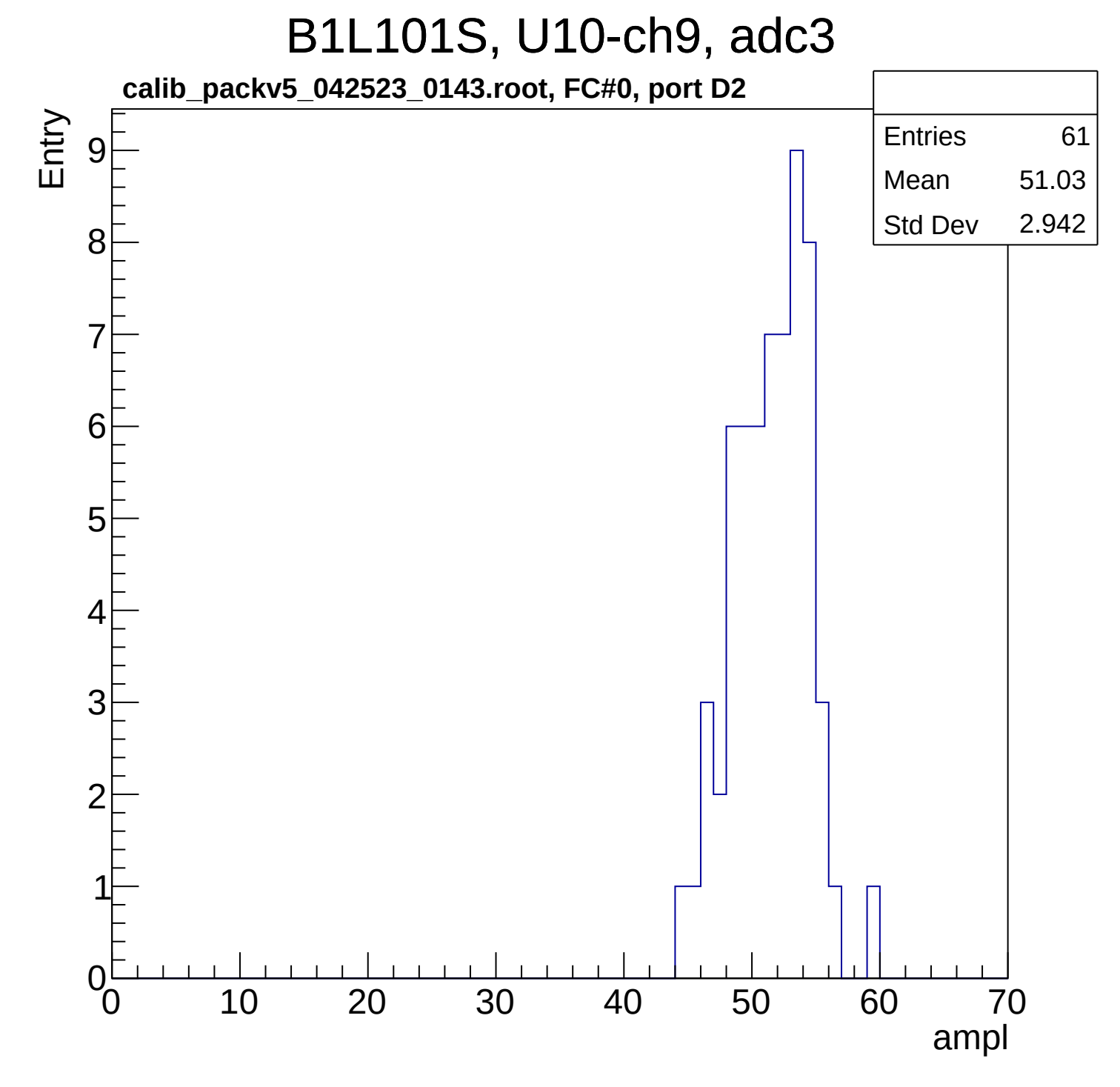
B1L101S, U10-ch9, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 51.03
Std Dev 2.942
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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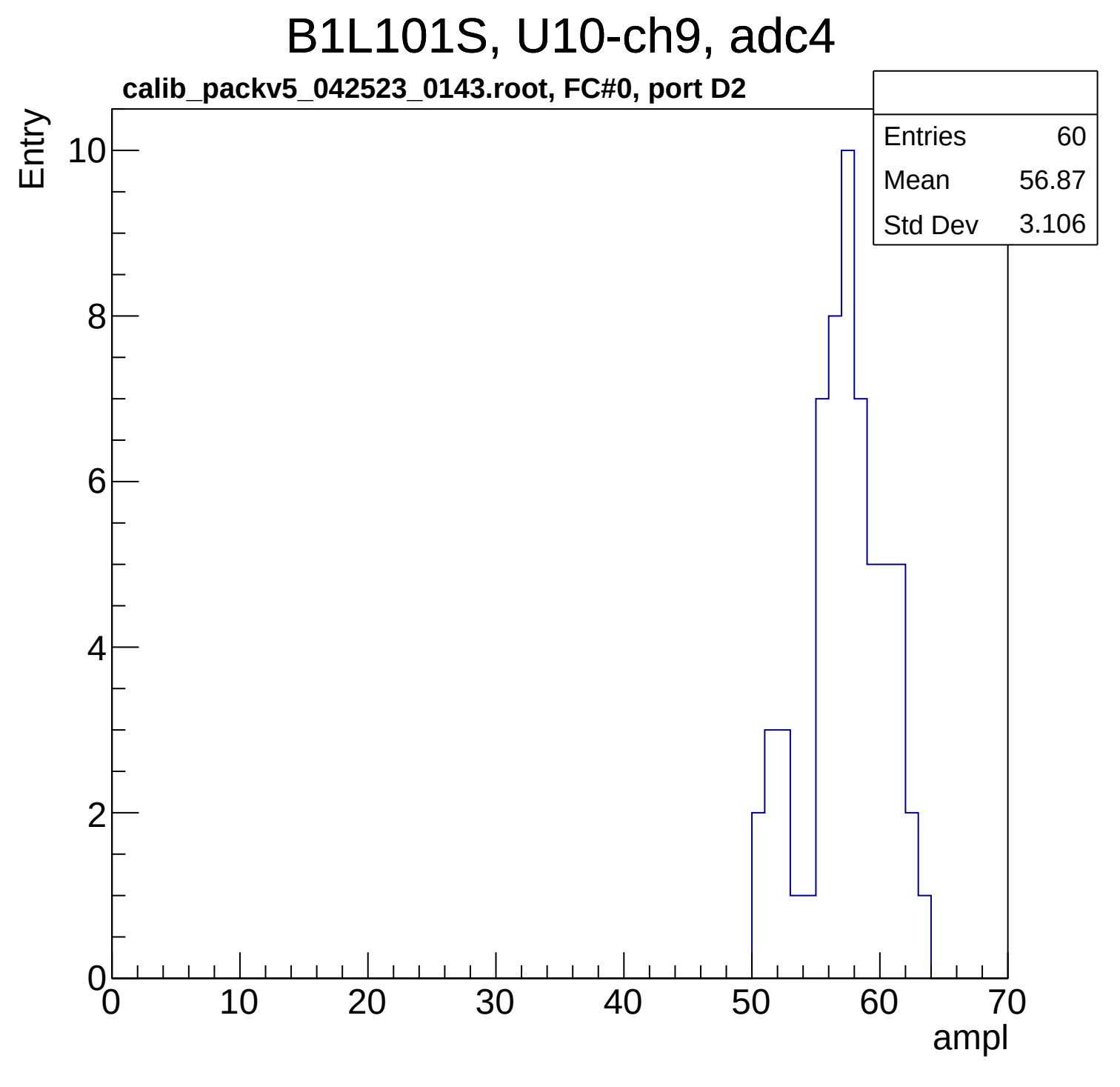
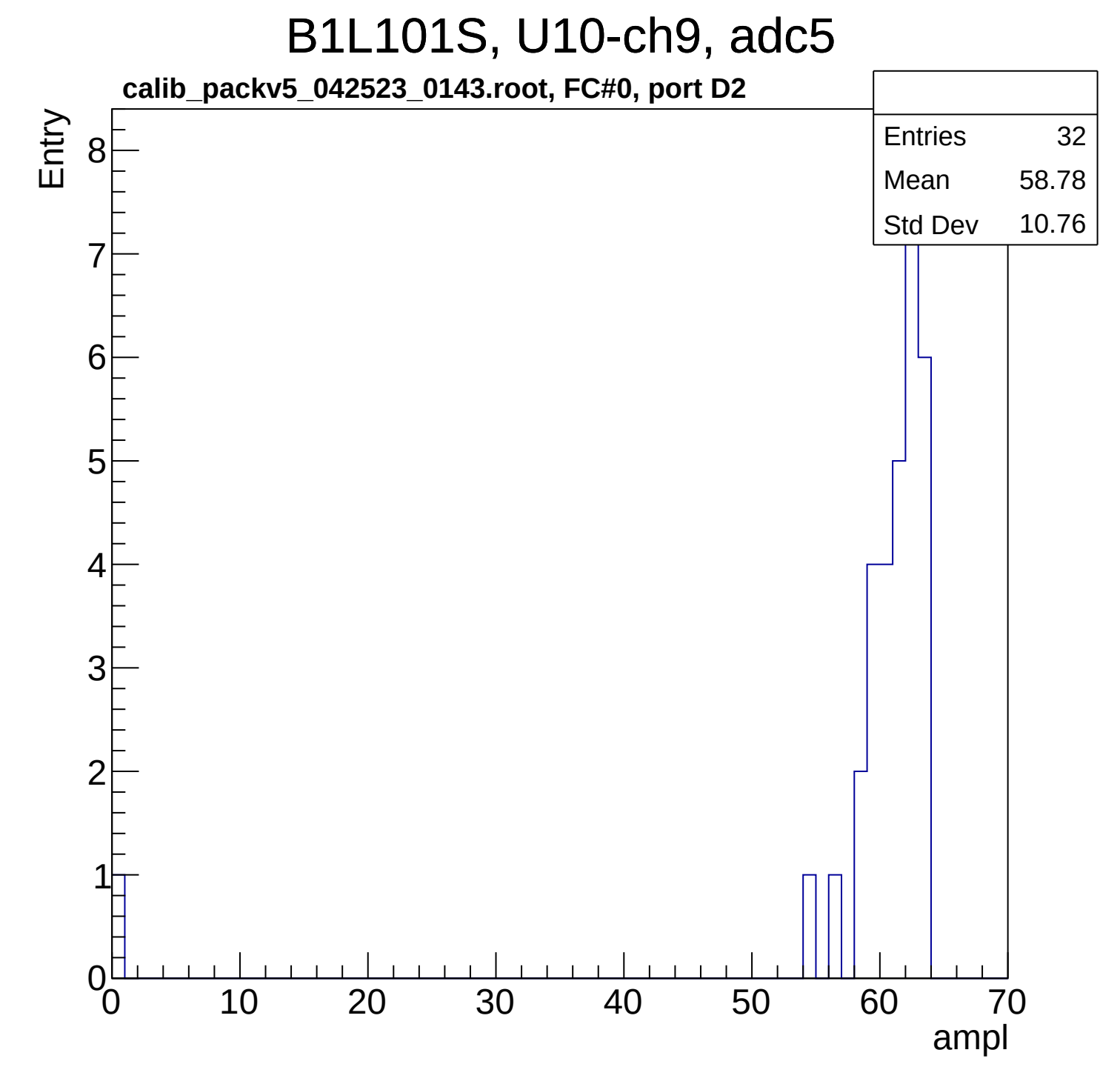
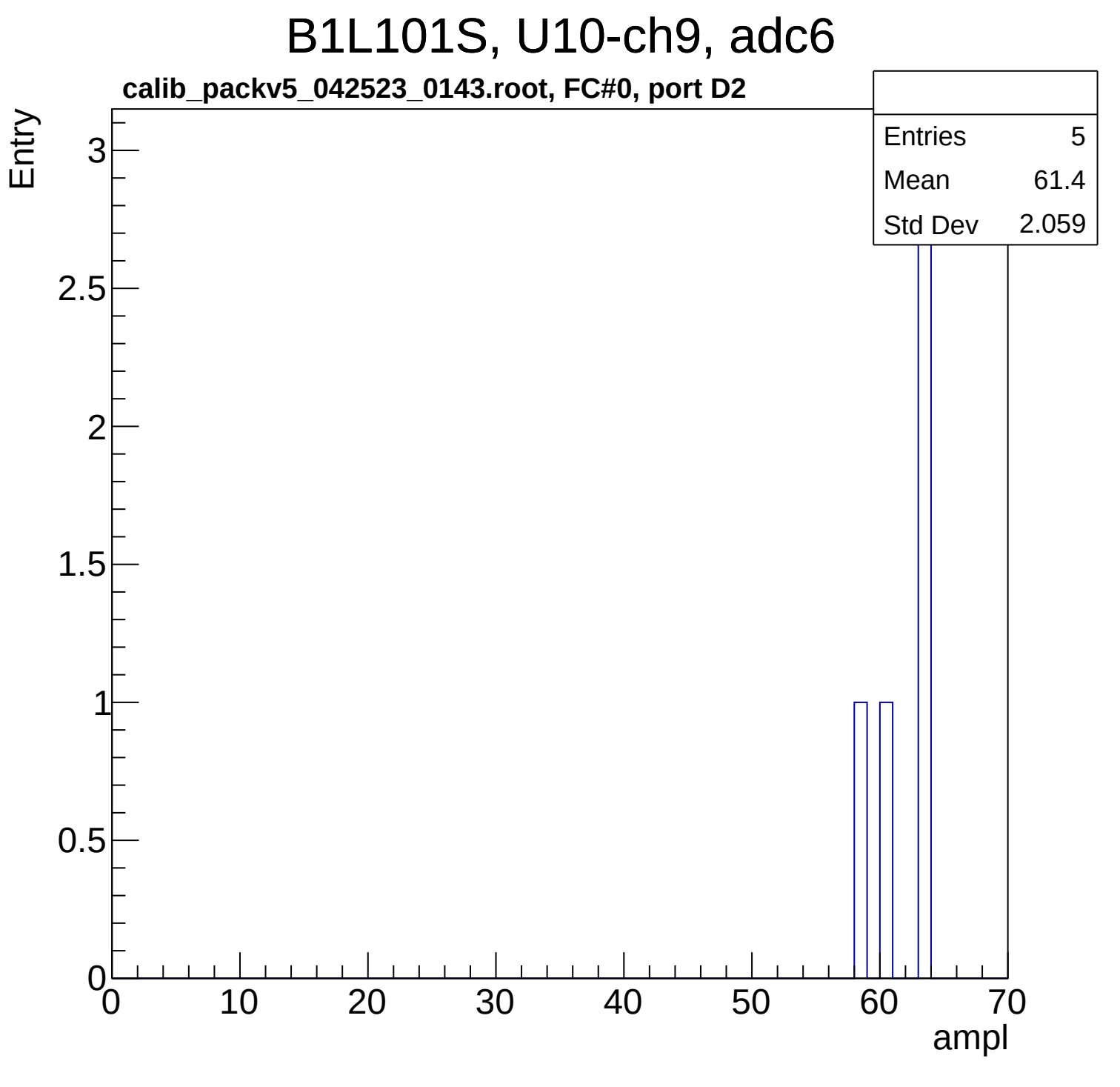

B1L101S, U10-ch9, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 56.87
Std Dev 3.106
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch9, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 32
Mean 58.78
Std Dev 10.76
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch9, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 61.4
Std Dev 2.059
Entry
ampl
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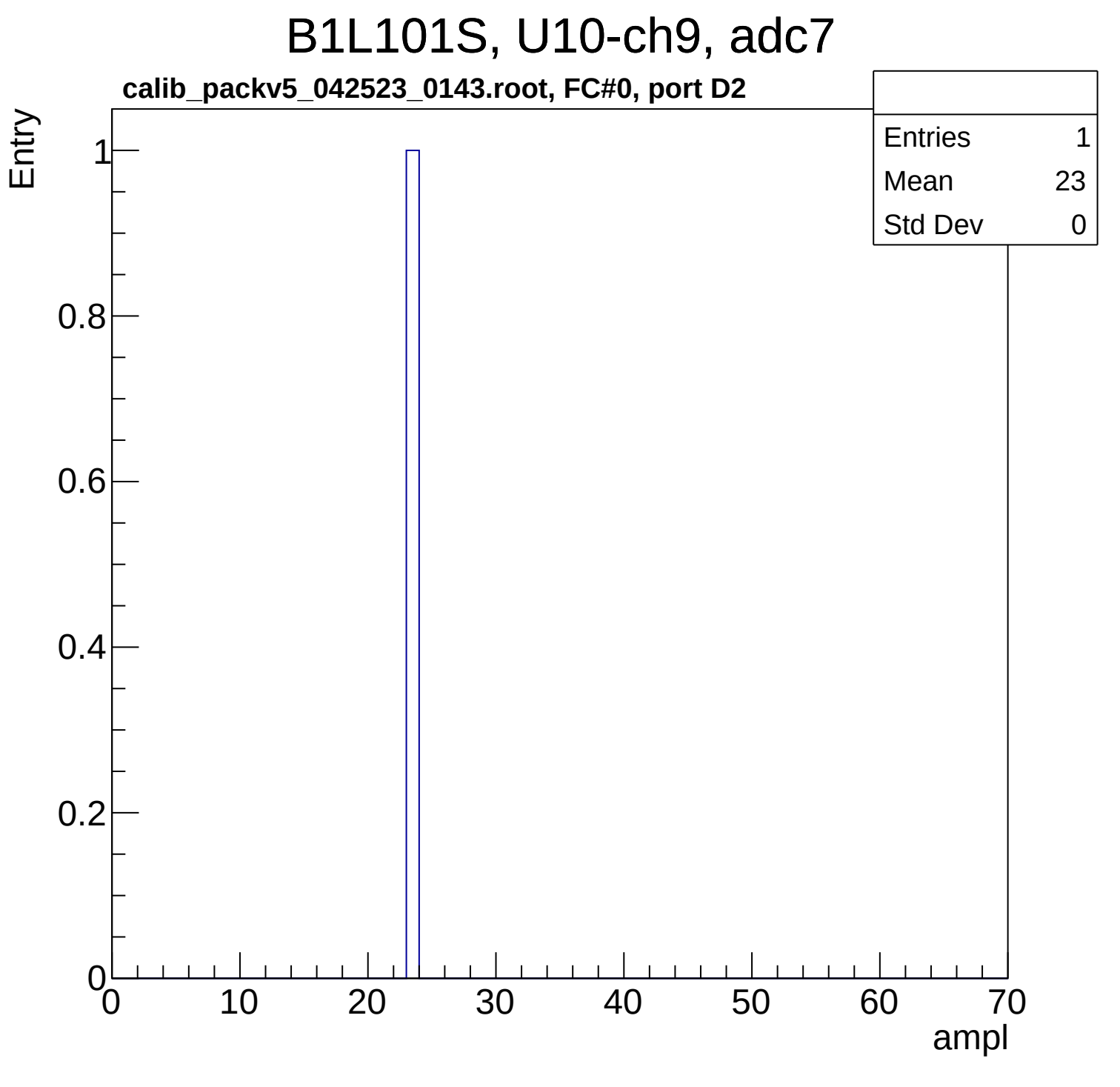
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U10-ch9, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 23
Std Dev 0
Entry
1
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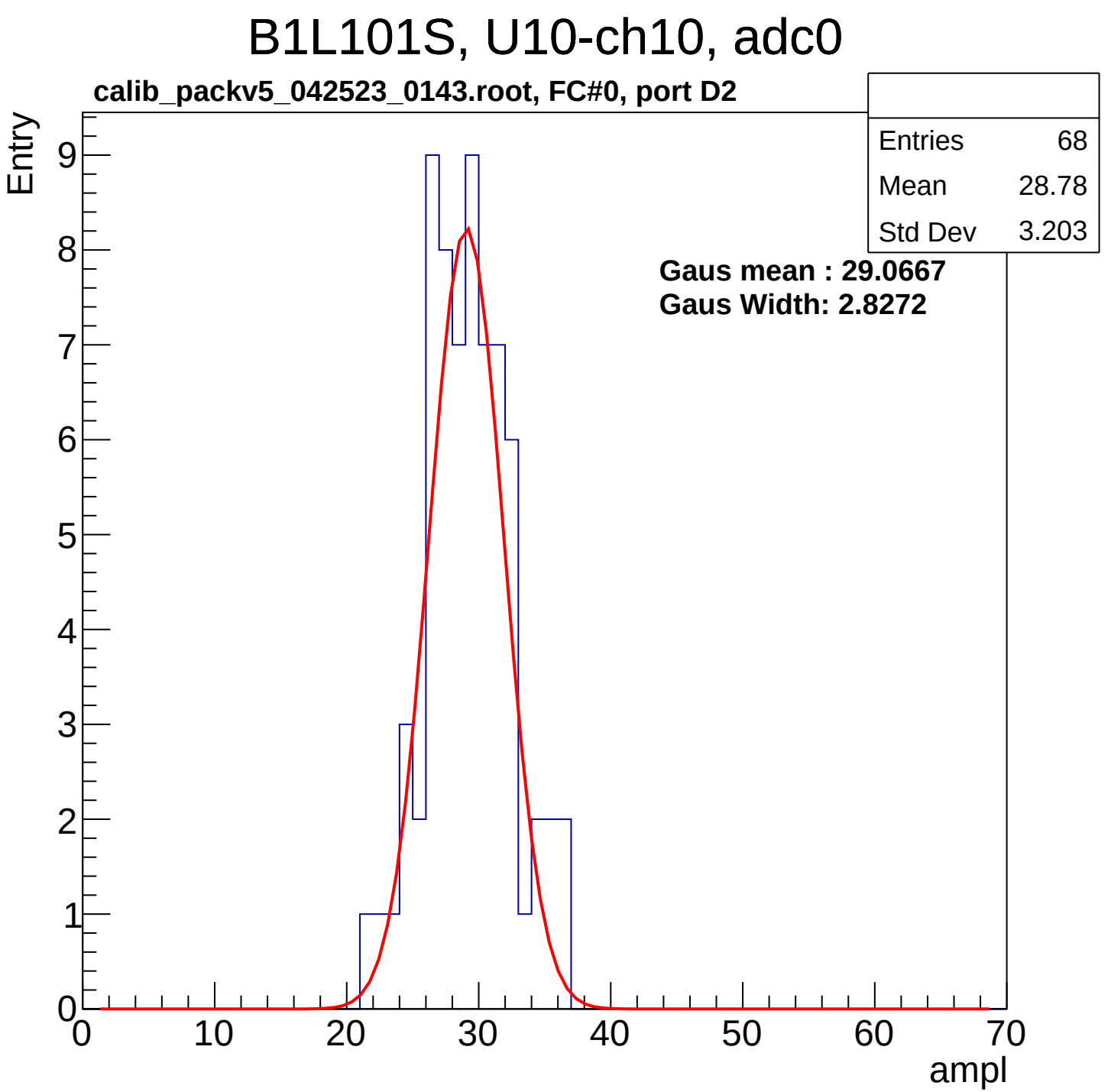
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch10, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 28.78
Std Dev 3.203
Gaus mean : 29.0667
Gaus Width: 2.8272
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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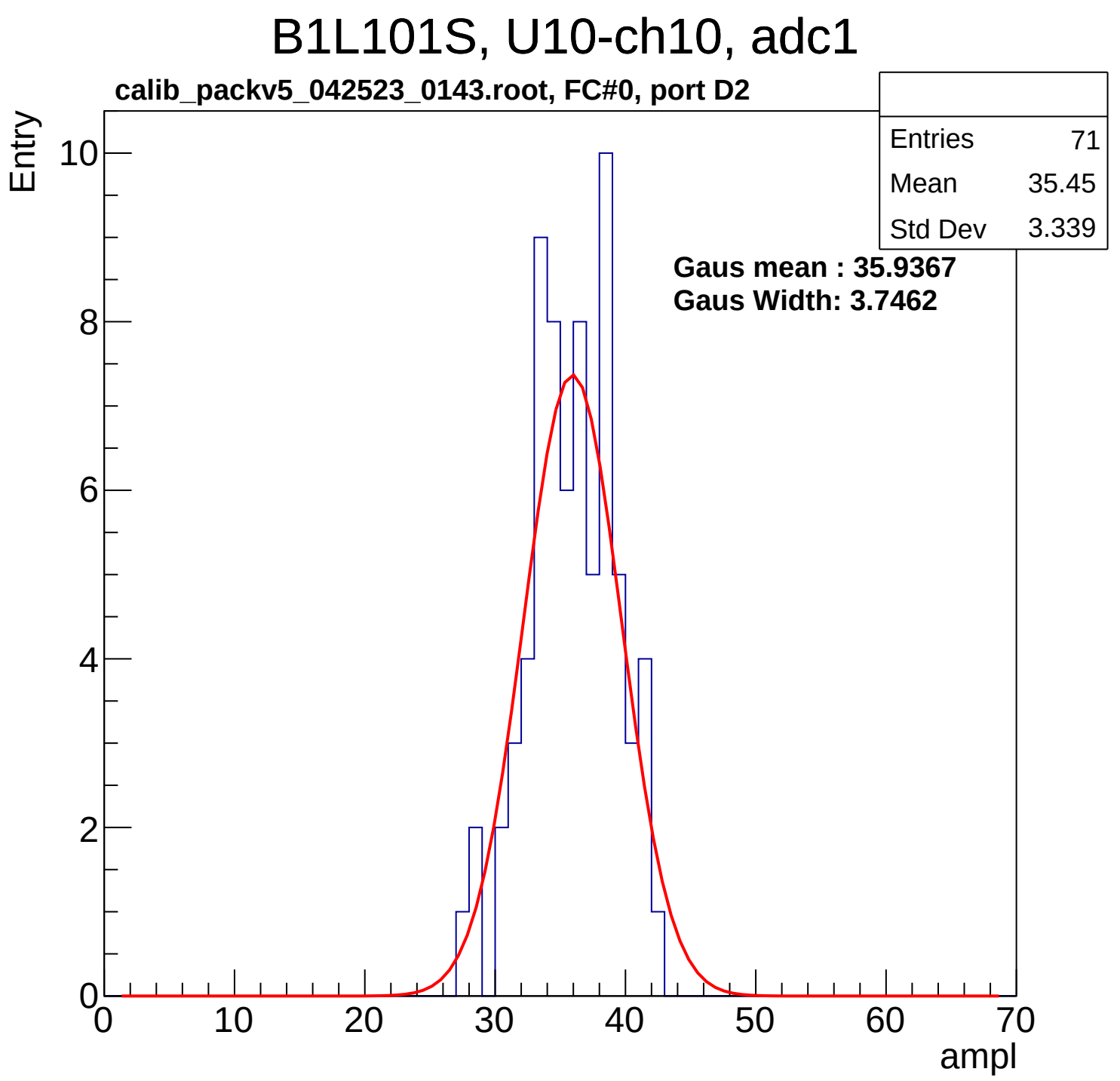
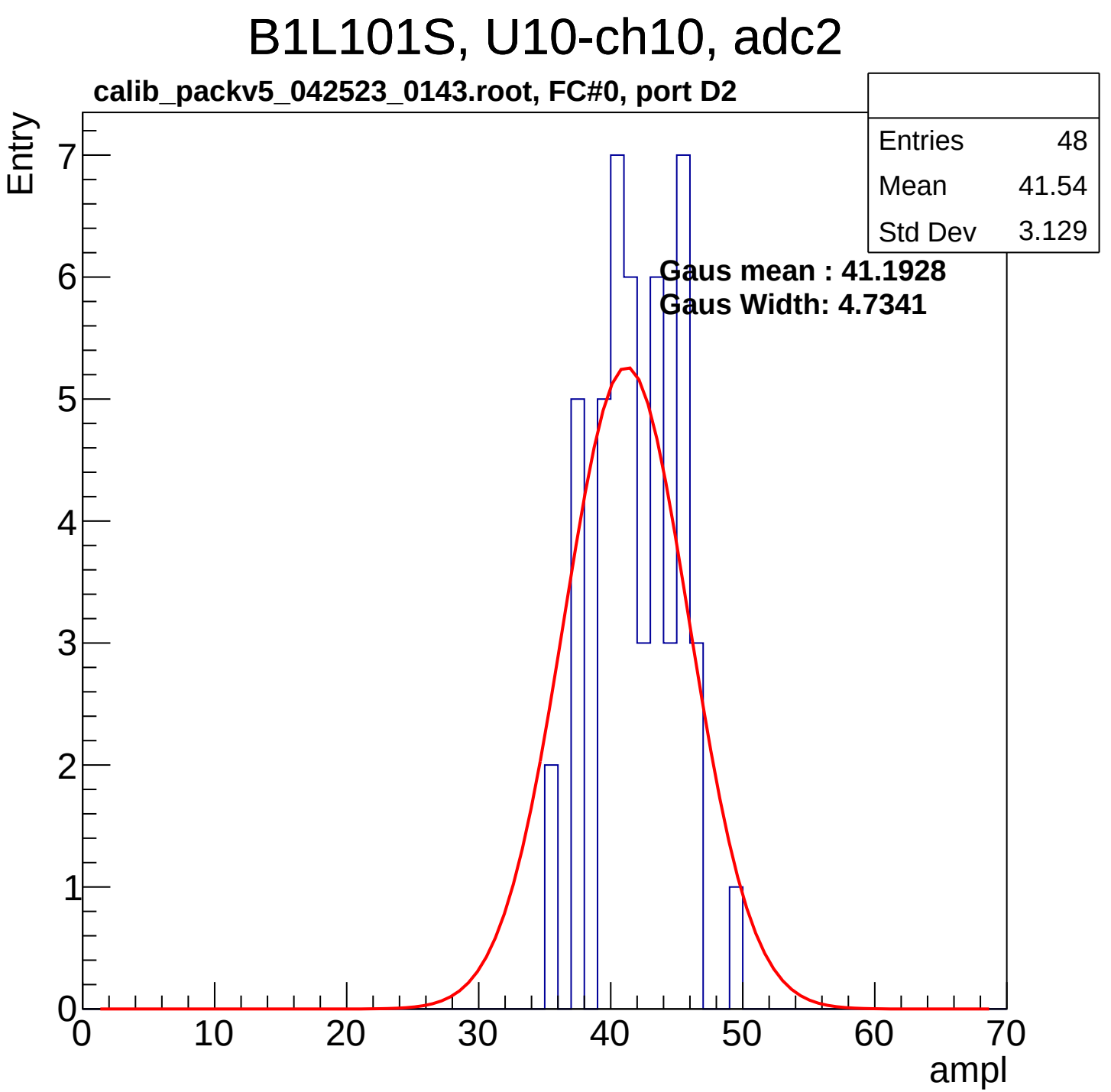

B1L101S, U10-ch10, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 35.45
Std Dev 3.339
Gaus mean : 35.9367
Gaus Width: 3.7462
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch10, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 41.54
Std Dev 3.129
Gaus mean : 41.1928
Gaus Width: 4.7341
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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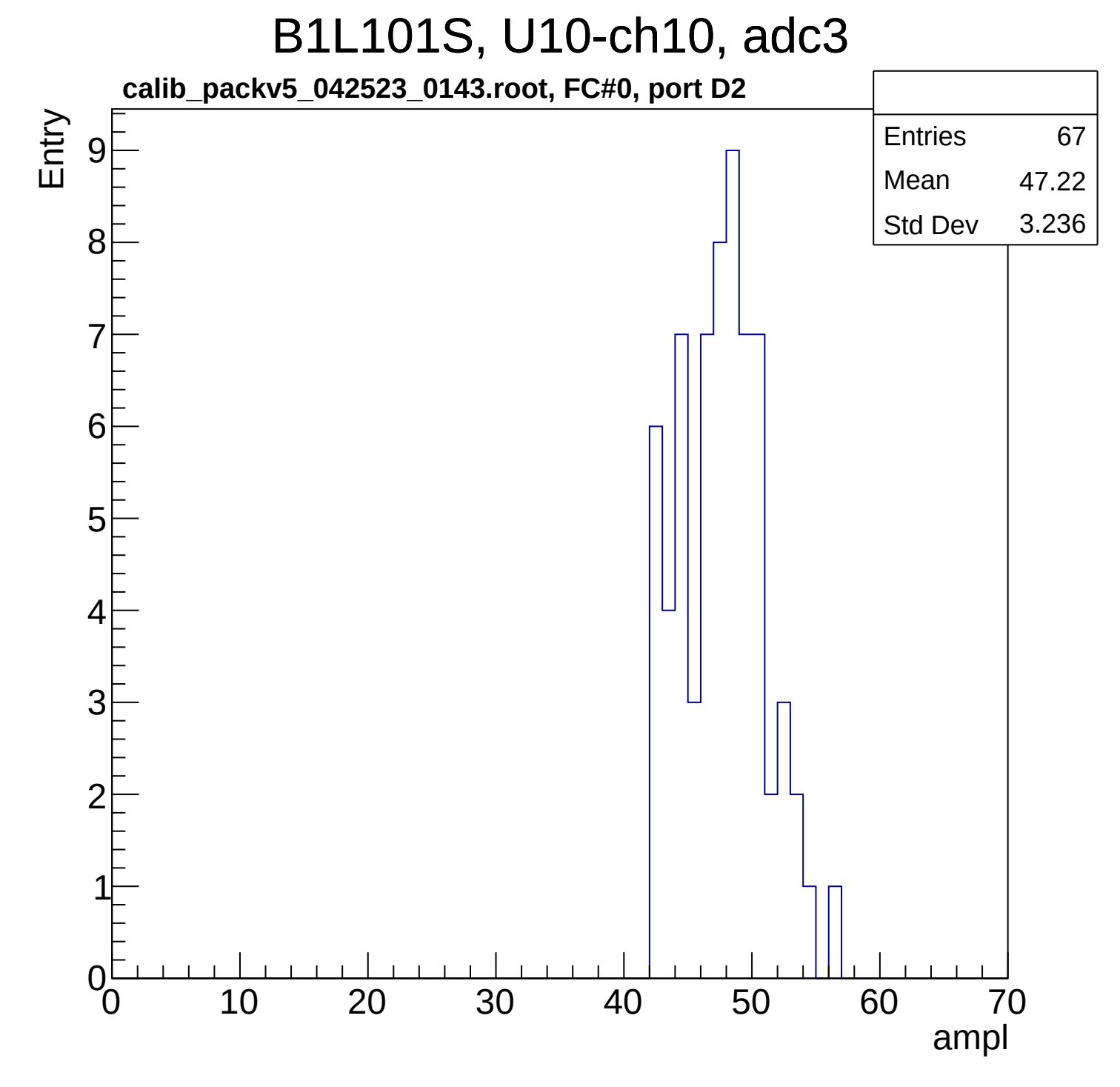
B1L101S, U10-ch10, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 47.22
Std Dev 3.236
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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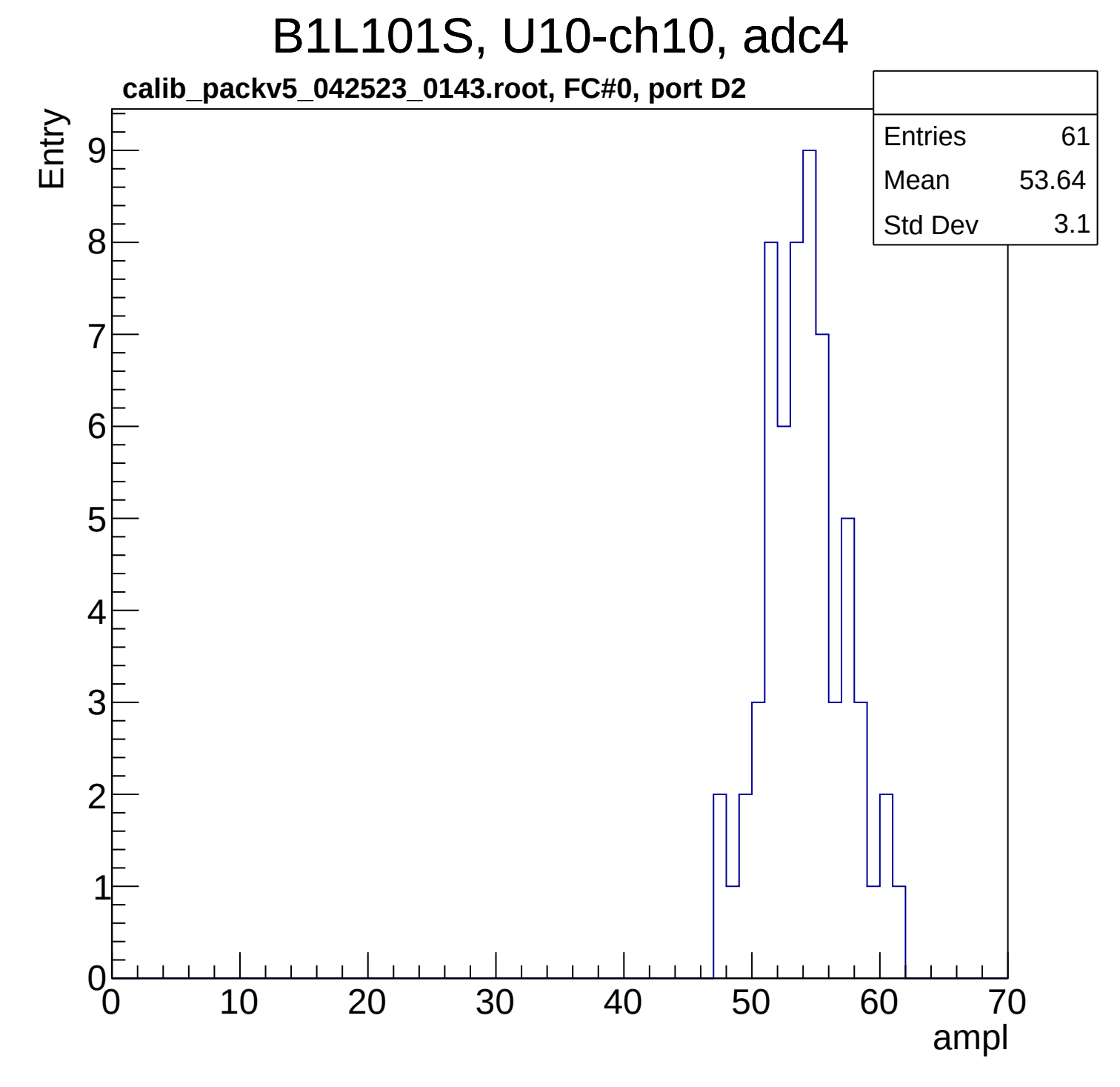
B1L101S, U10-ch10, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 53.64
Std Dev 3.1
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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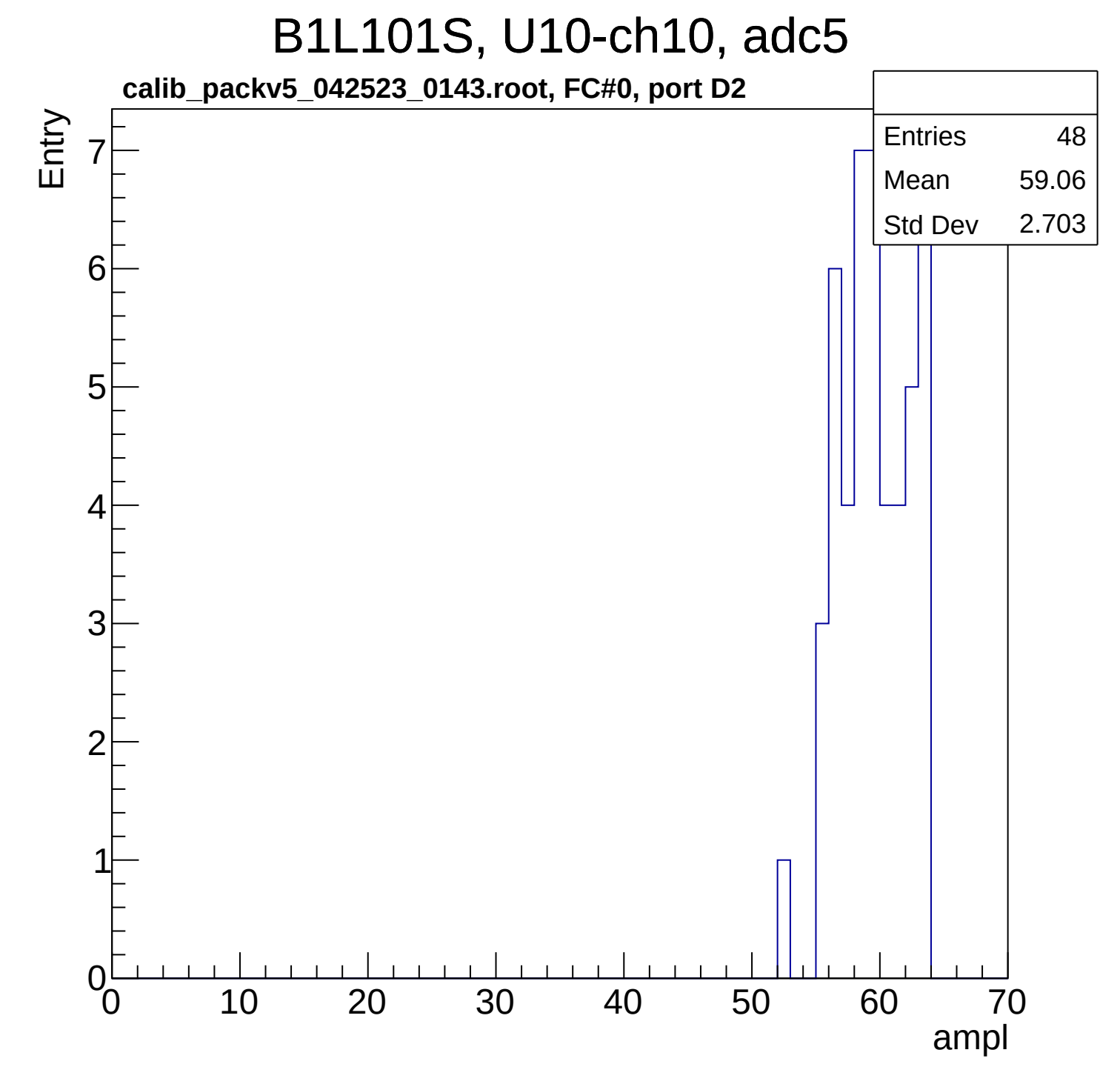
B1L101S, U10-ch10, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 59.06
Std Dev 2.703
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
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60
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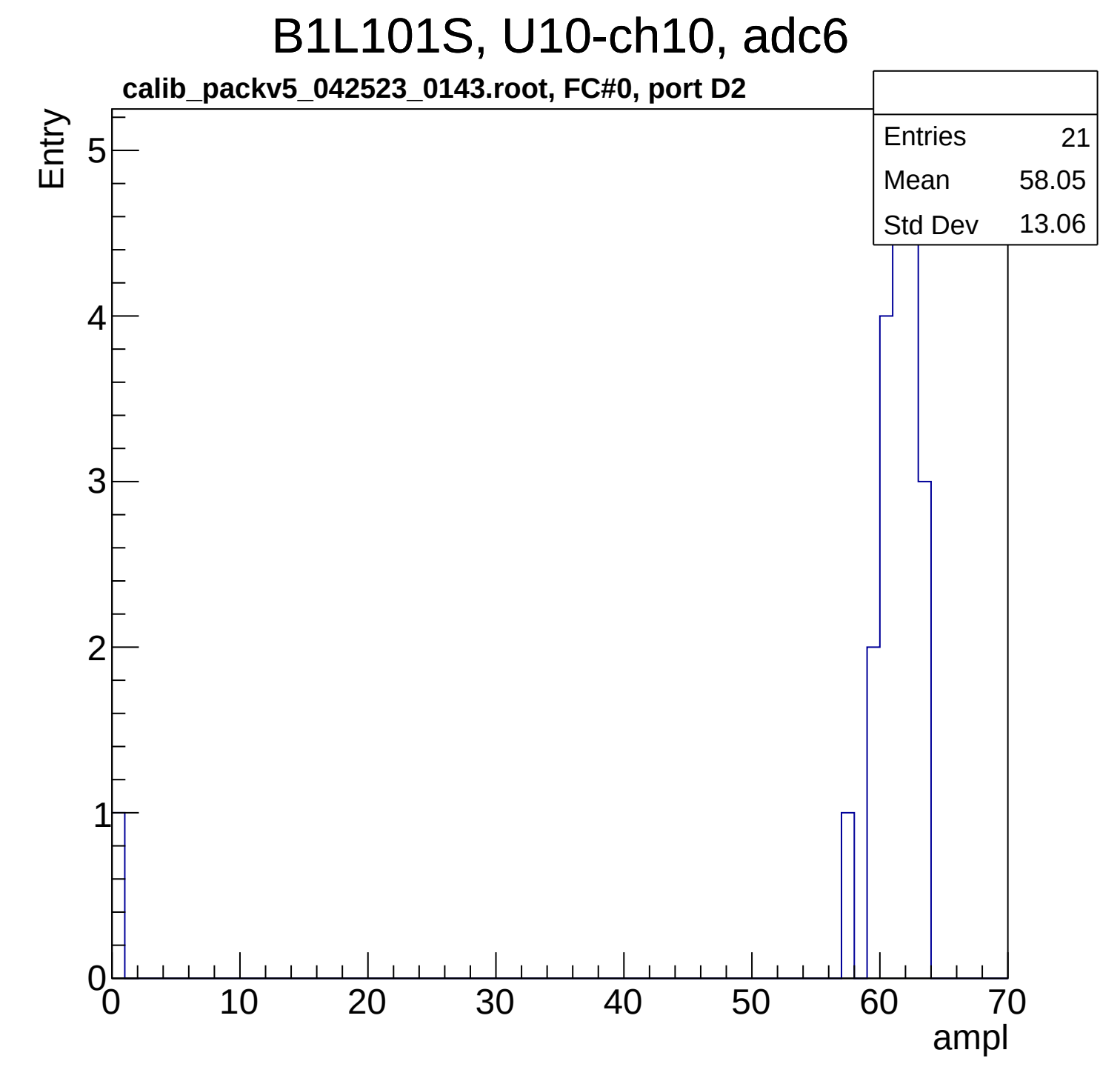
B1L101S, U10-ch10, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 21
Mean 58.05
Std Dev 13.06
Entry
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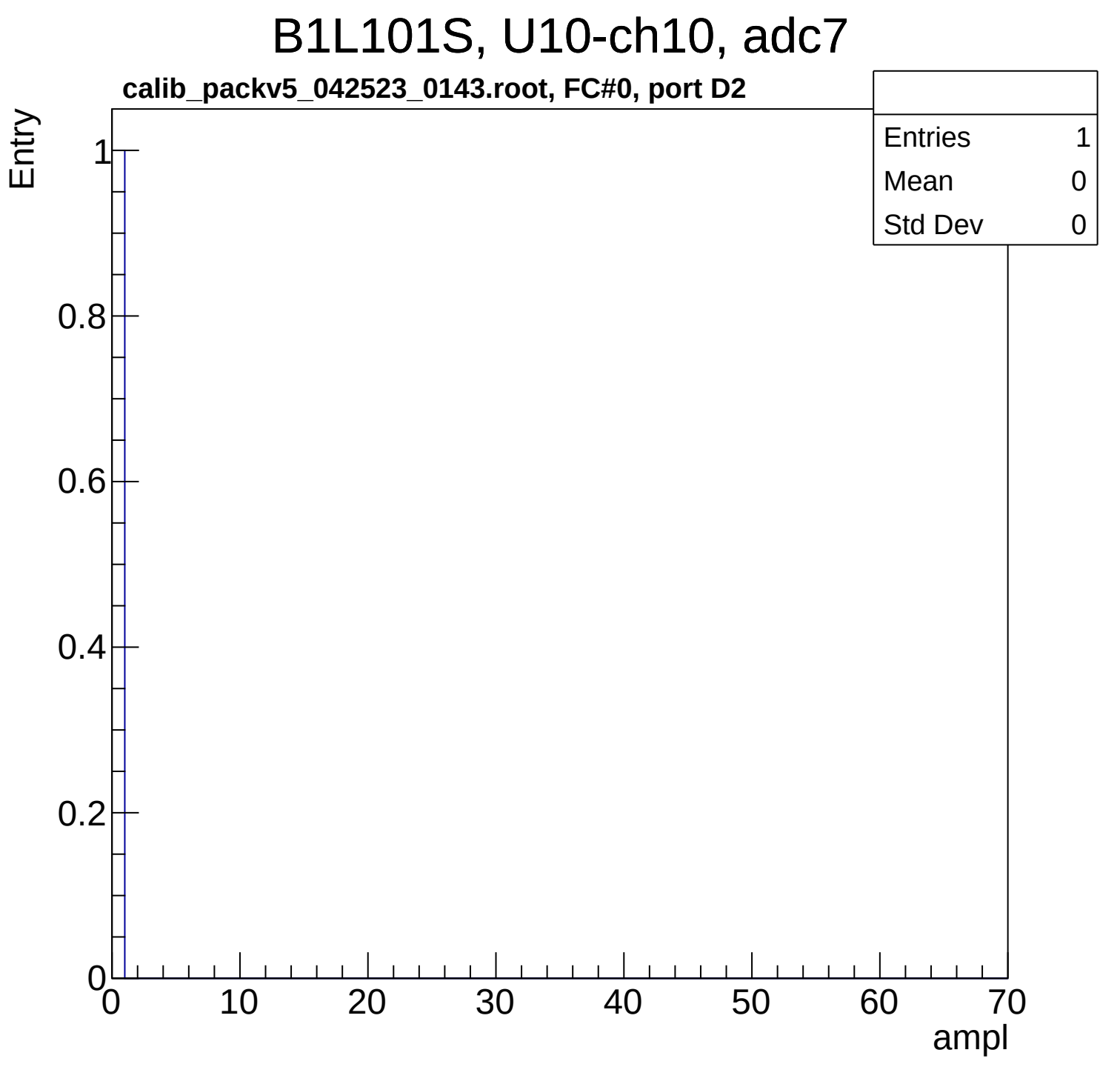
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch10, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
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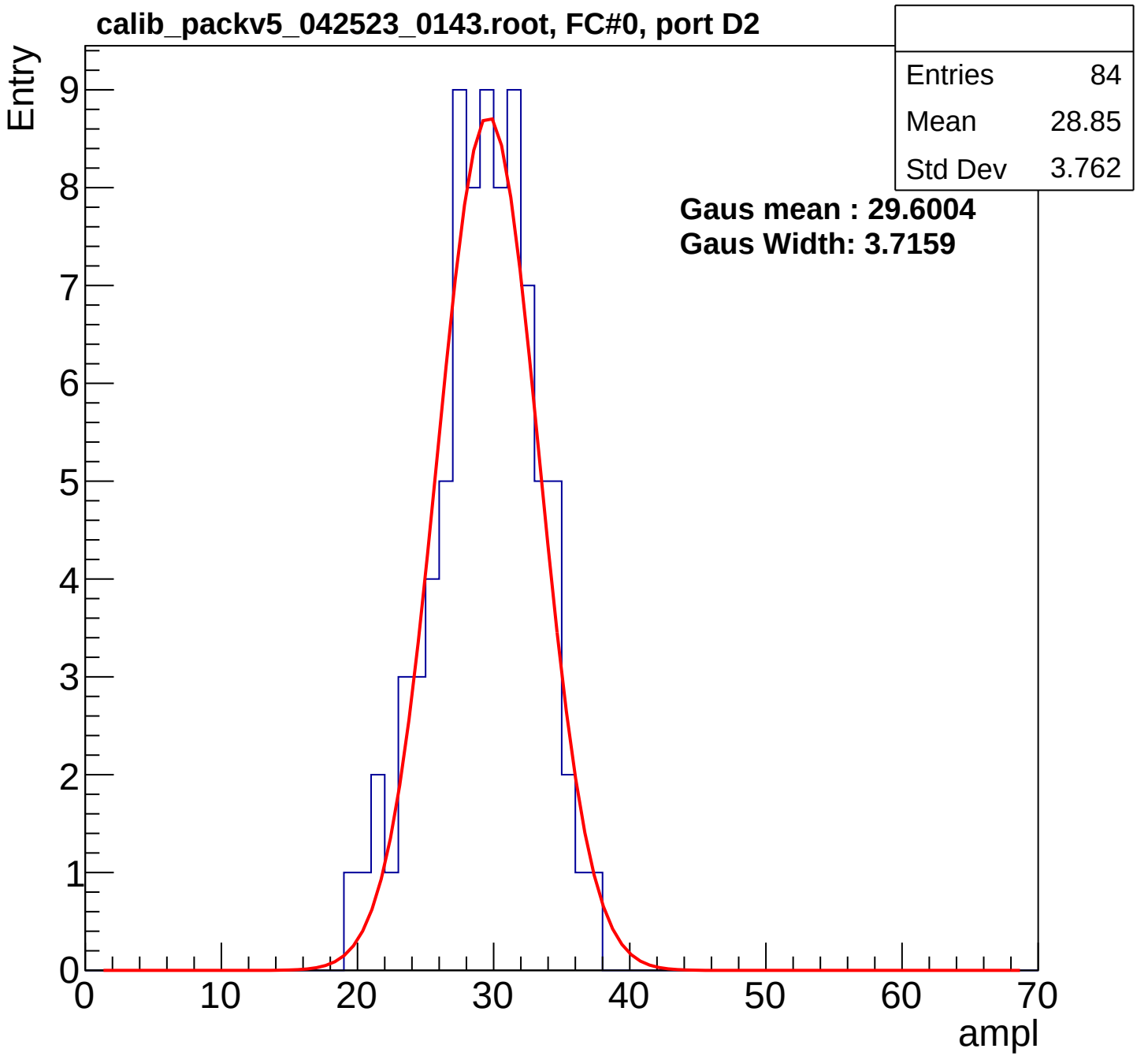
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch11, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 84
Mean 28.85
Std Dev 3.762
Gaus mean : 29.6004
Gaus Width: 3.7159
Entry
ampl
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2
3
4
5
6
7
8
9
0
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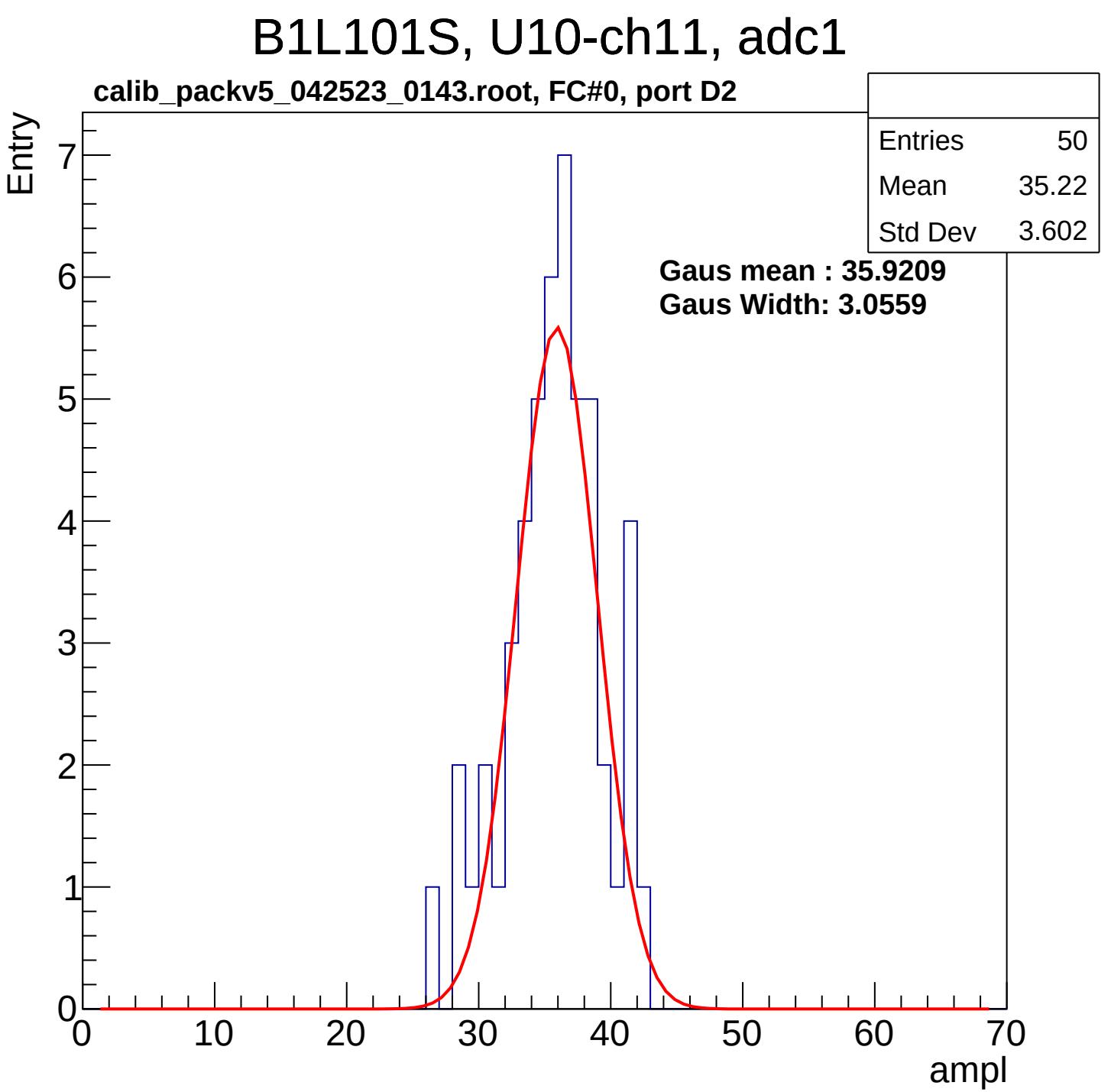
B1L101S, U10-ch11, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 35.22
Std Dev 3.602
Gaus mean : 35.9209
Gaus Width: 3.0559
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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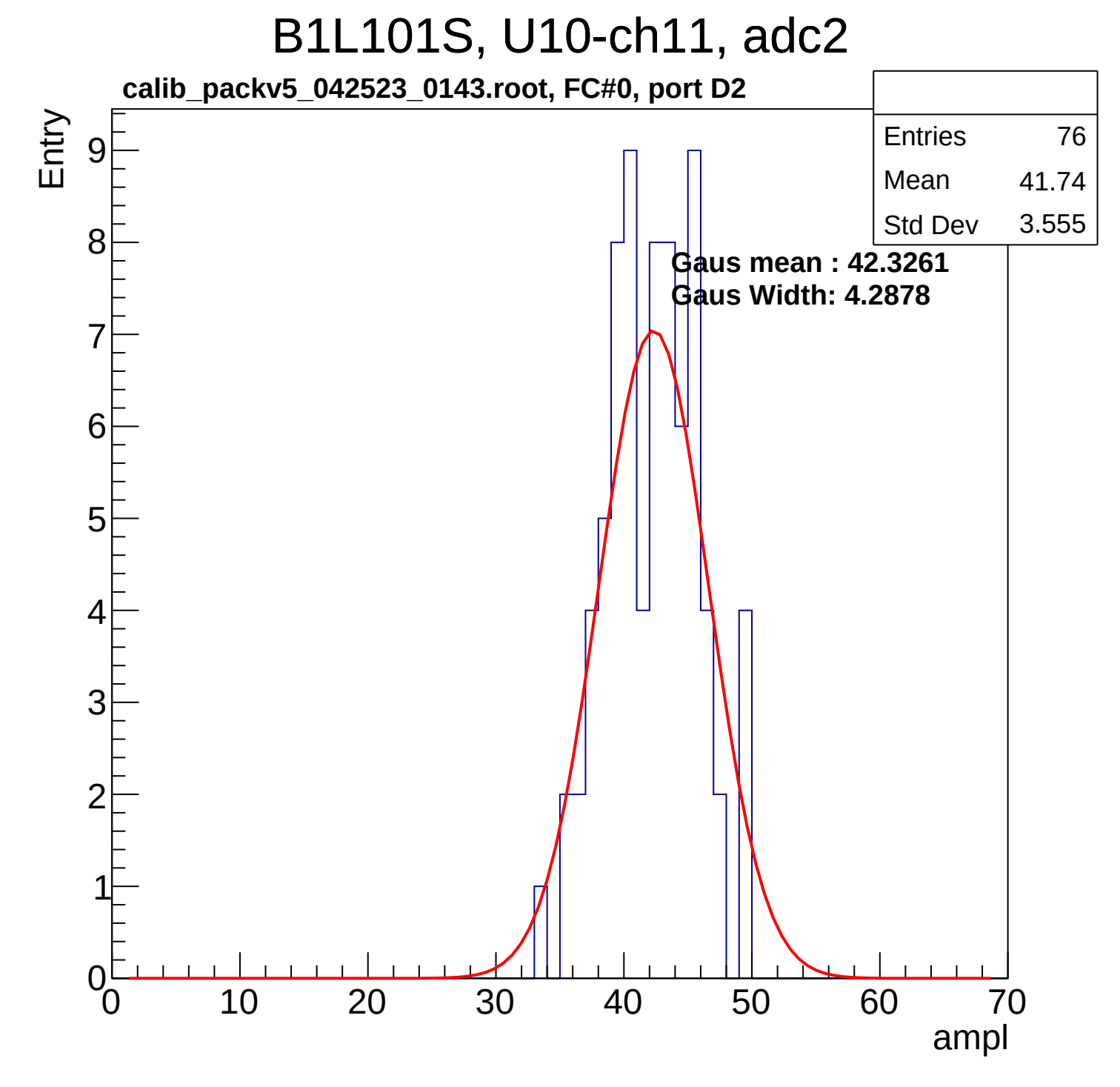
B1L101S, U10-ch11, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 41.74
Std Dev 3.555
Gaus mean : 42.3261
Gaus Width: 4.2878
Entry
ampl
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2
3
4
5
6
7
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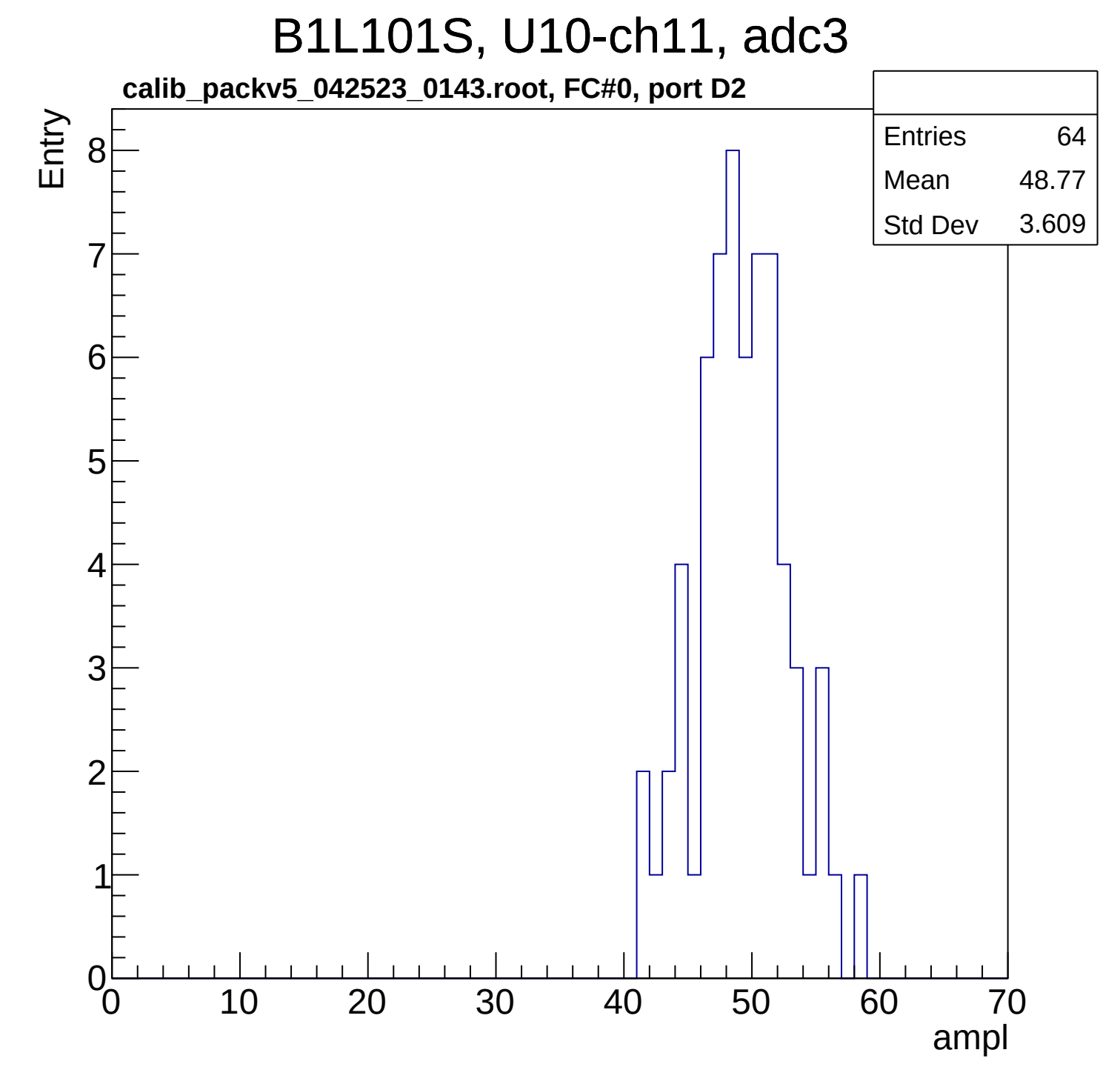
B1L101S, U10-ch11, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 48.77
Std Dev 3.609
Entry
ampl
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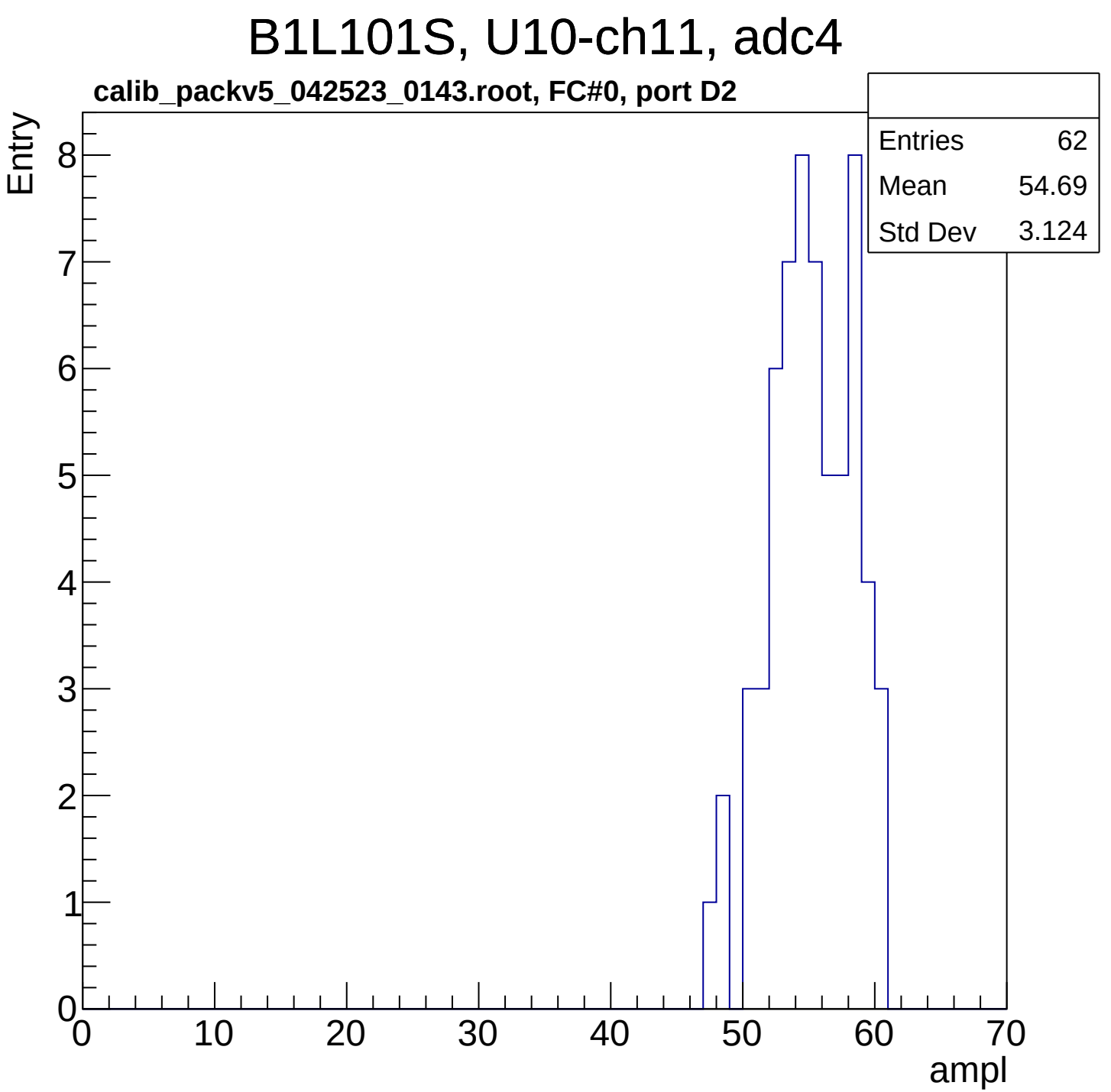
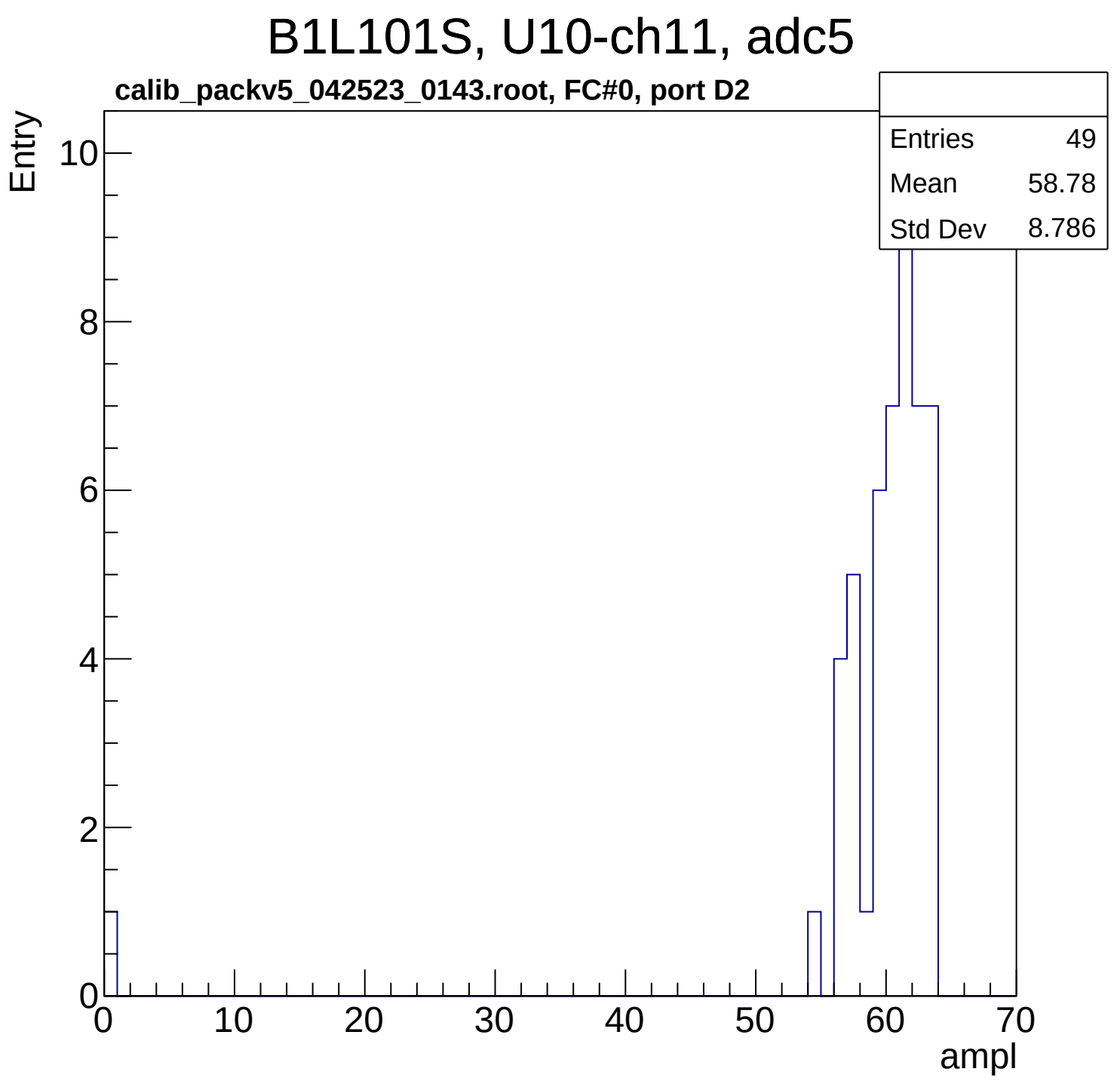

B1L101S, U10-ch11, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 54.69
Std Dev 3.124
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch11, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 58.78
Std Dev 8.786
Entry
0
2
4
6
8
10
0
10
20
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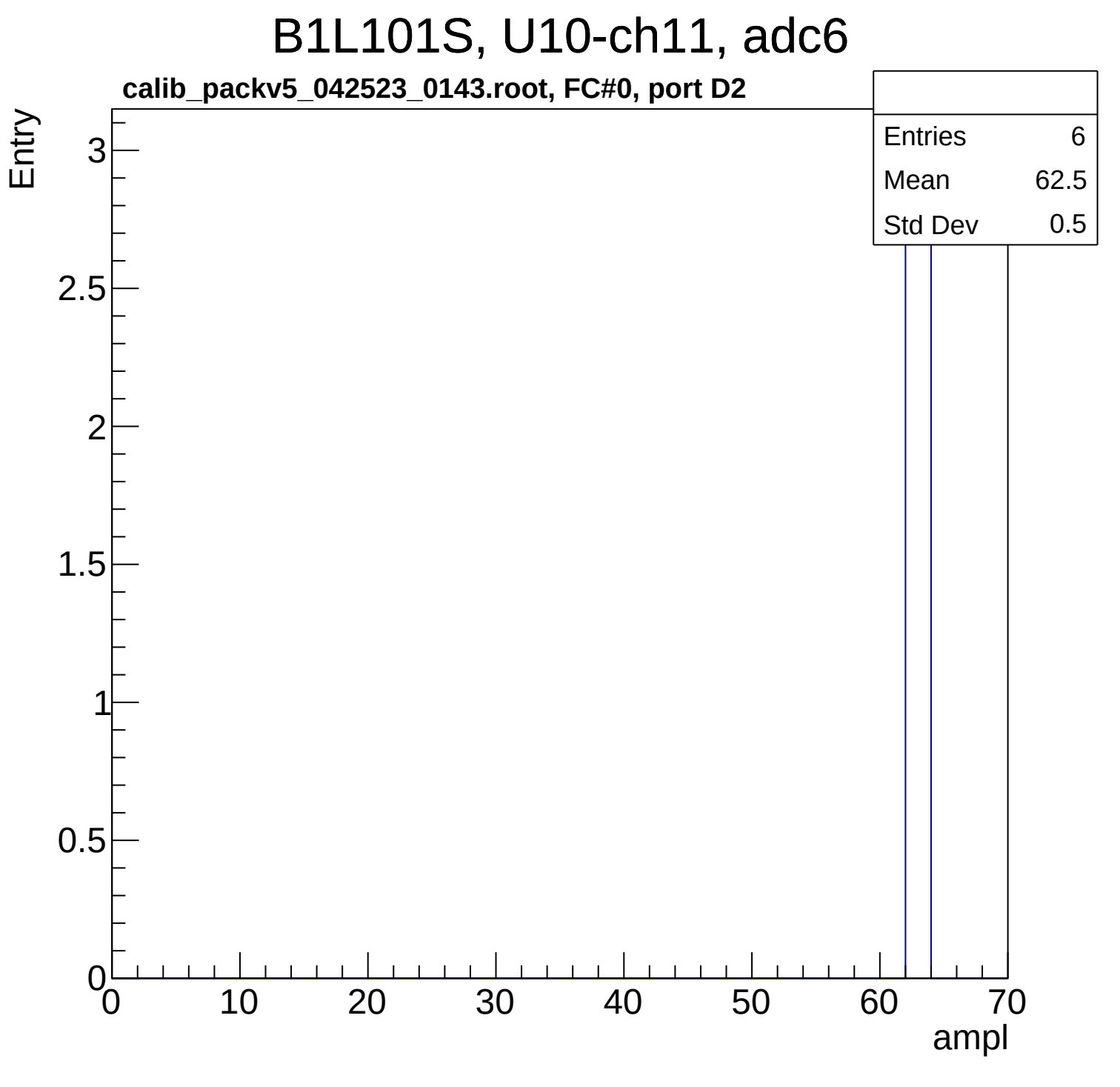
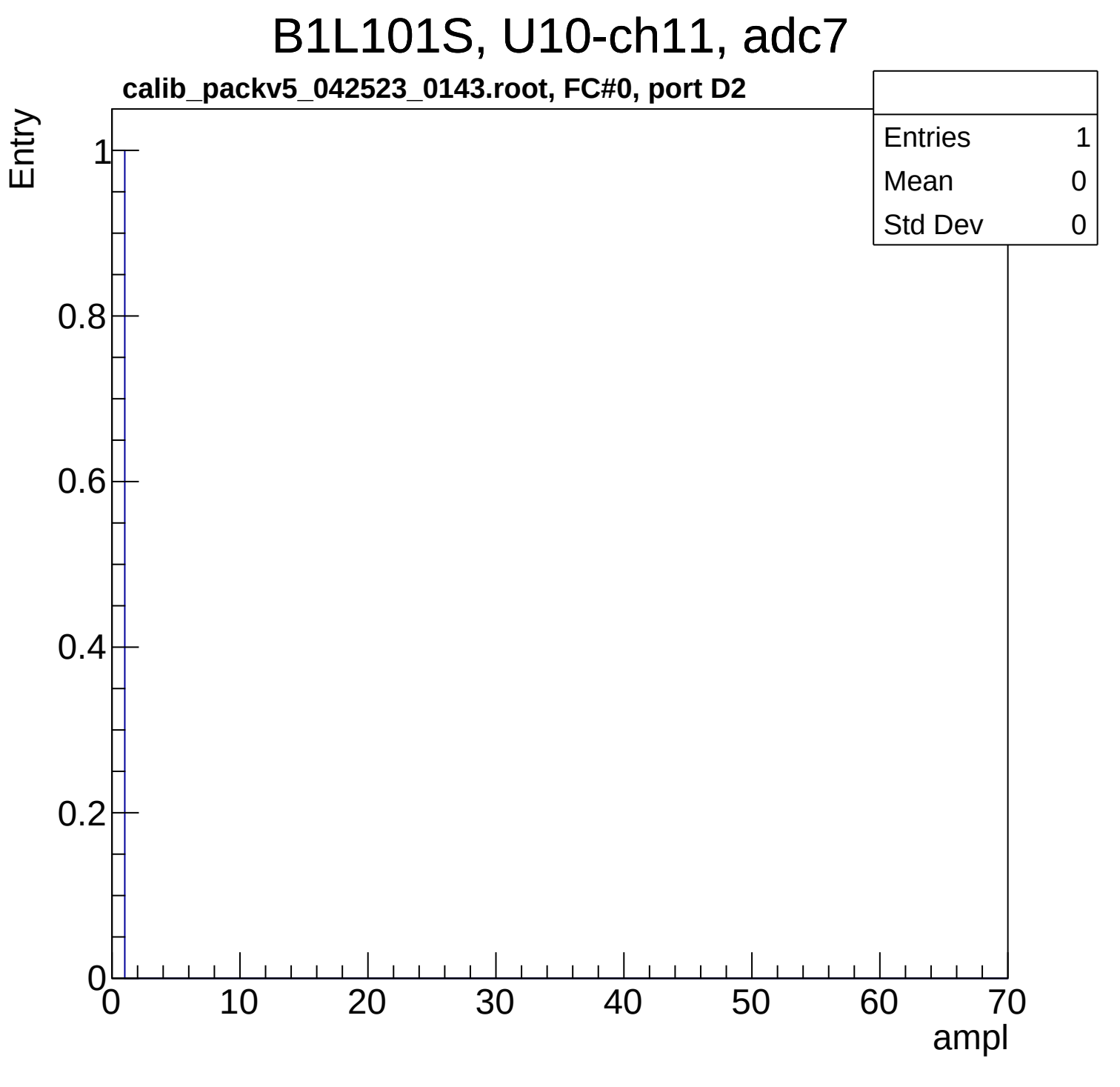
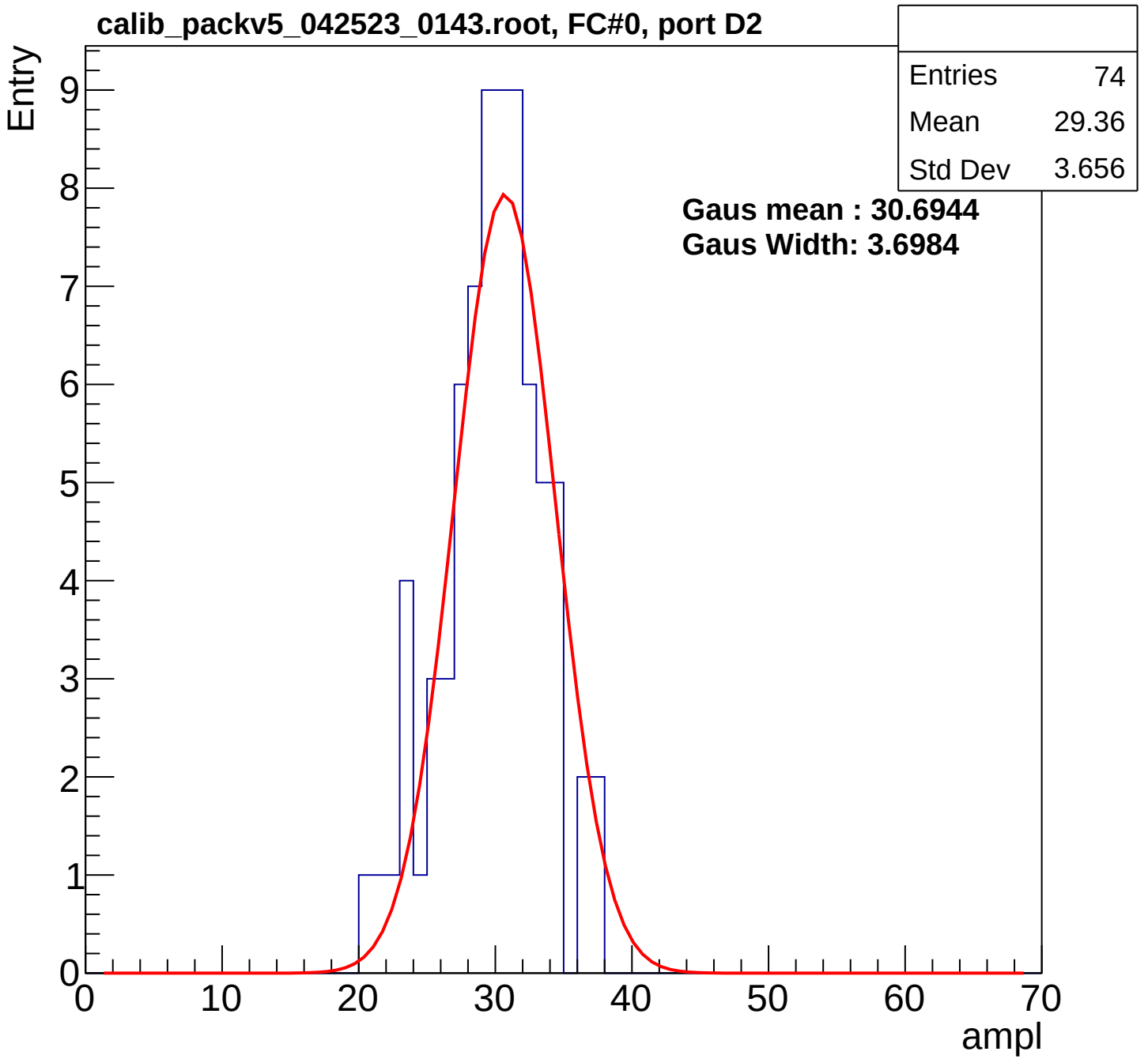
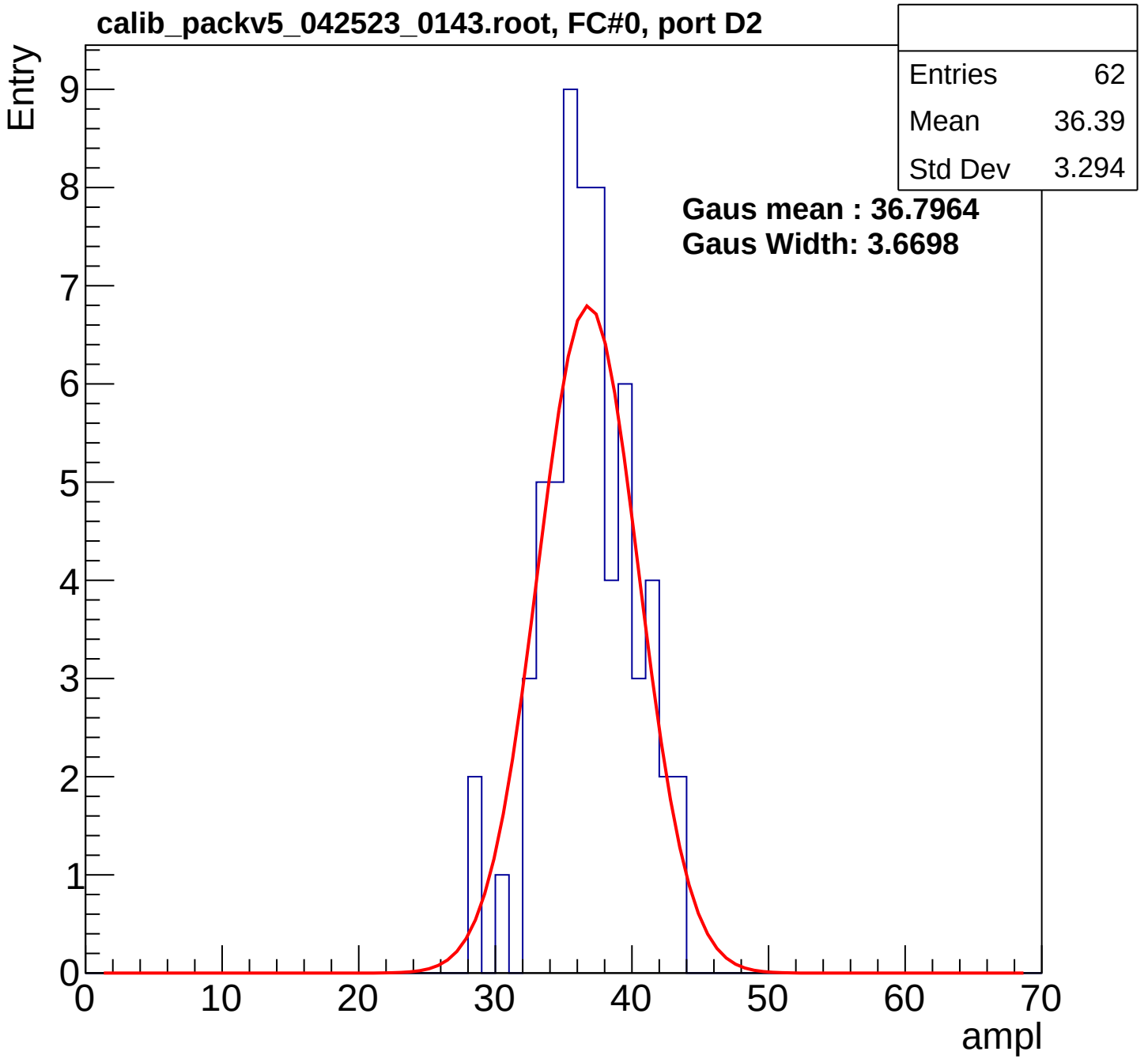
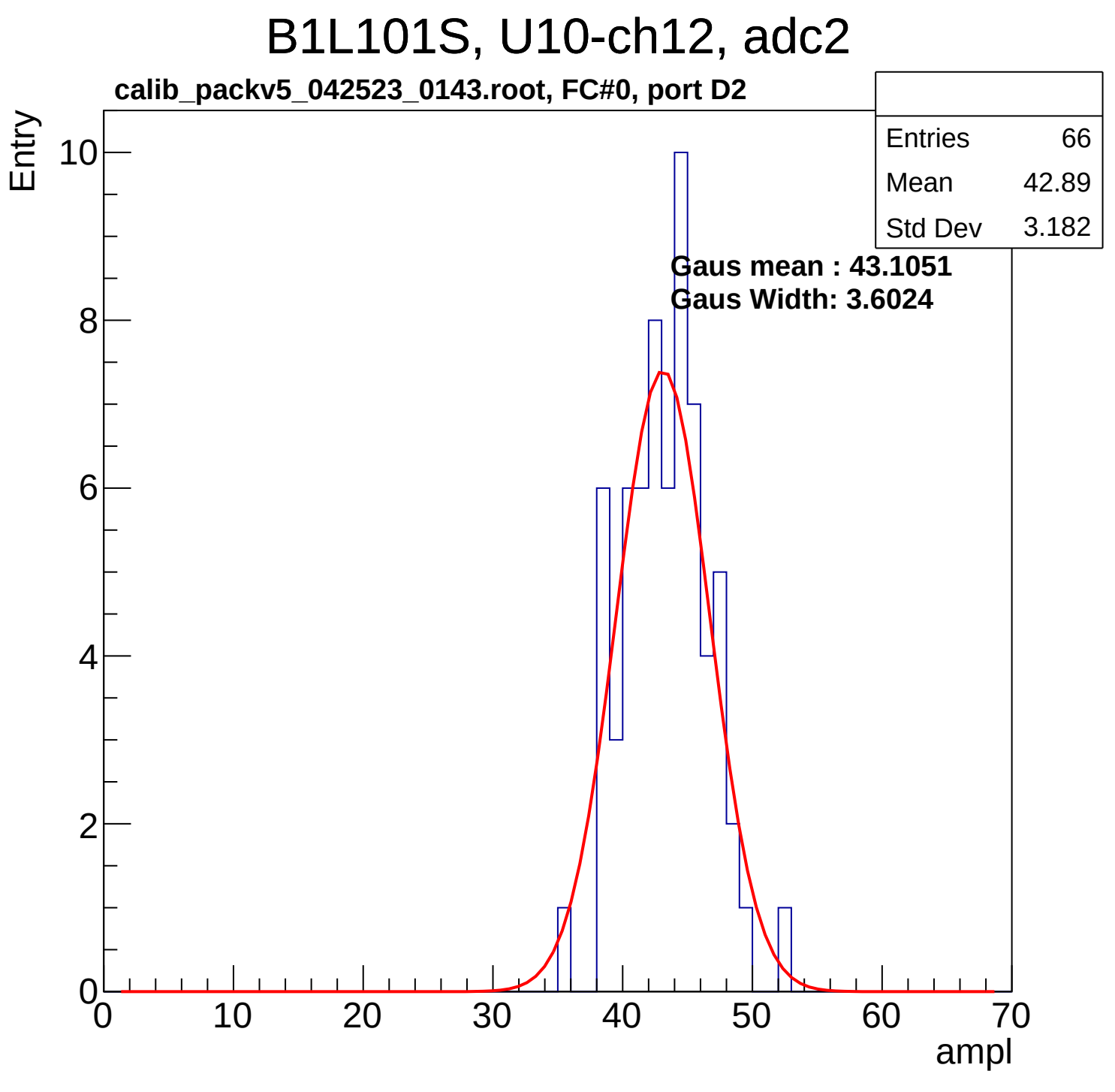
50
60
70
ampl

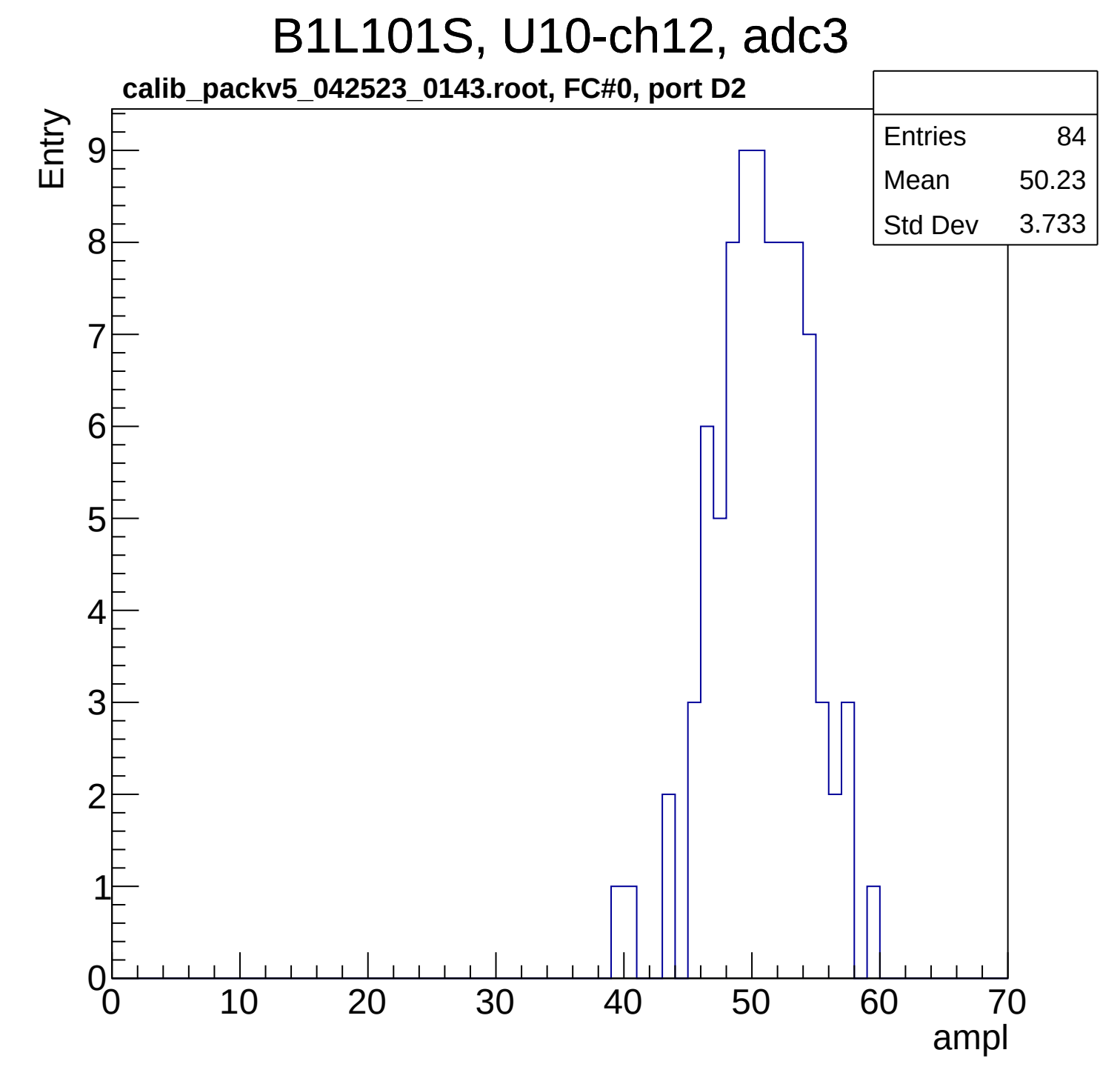

B1L101S, U10-ch11, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 62.5
Std Dev 0.5
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl

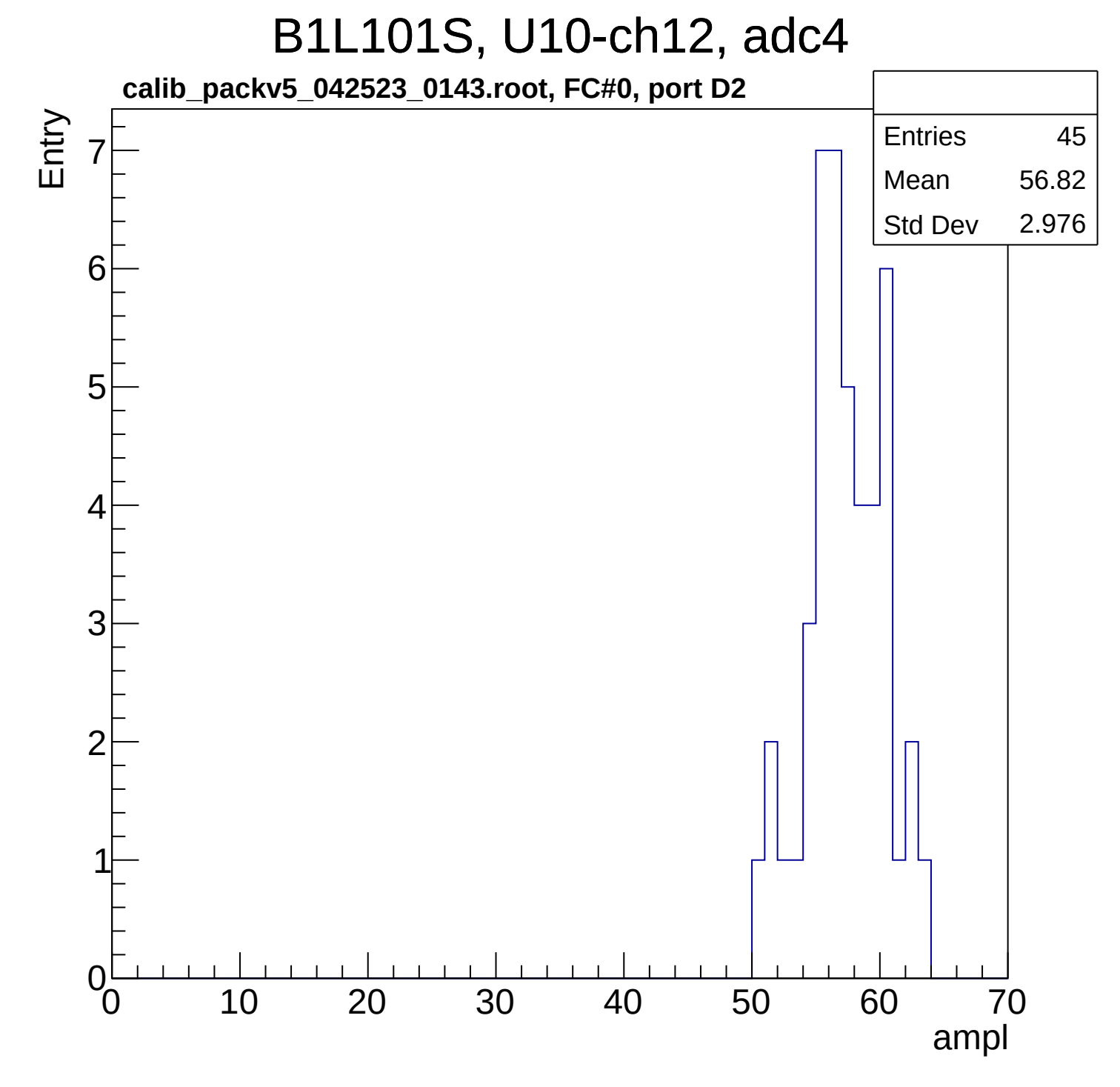

B1L101S, U10-ch11, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch12, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 29.36
Std Dev 3.656
Gaus mean : 30.6944
Gaus Width: 3.6984
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch12, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 36.39
Std Dev 3.294
Gaus mean : 36.7964
Gaus Width: 3.6698
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch12, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 42.89
Std Dev 3.182
Gaus mean : 43.1051
Gaus Width: 3.6024
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch12, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 84
Mean 50.23
Std Dev 3.733
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch12, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 56.82
Std Dev 2.976
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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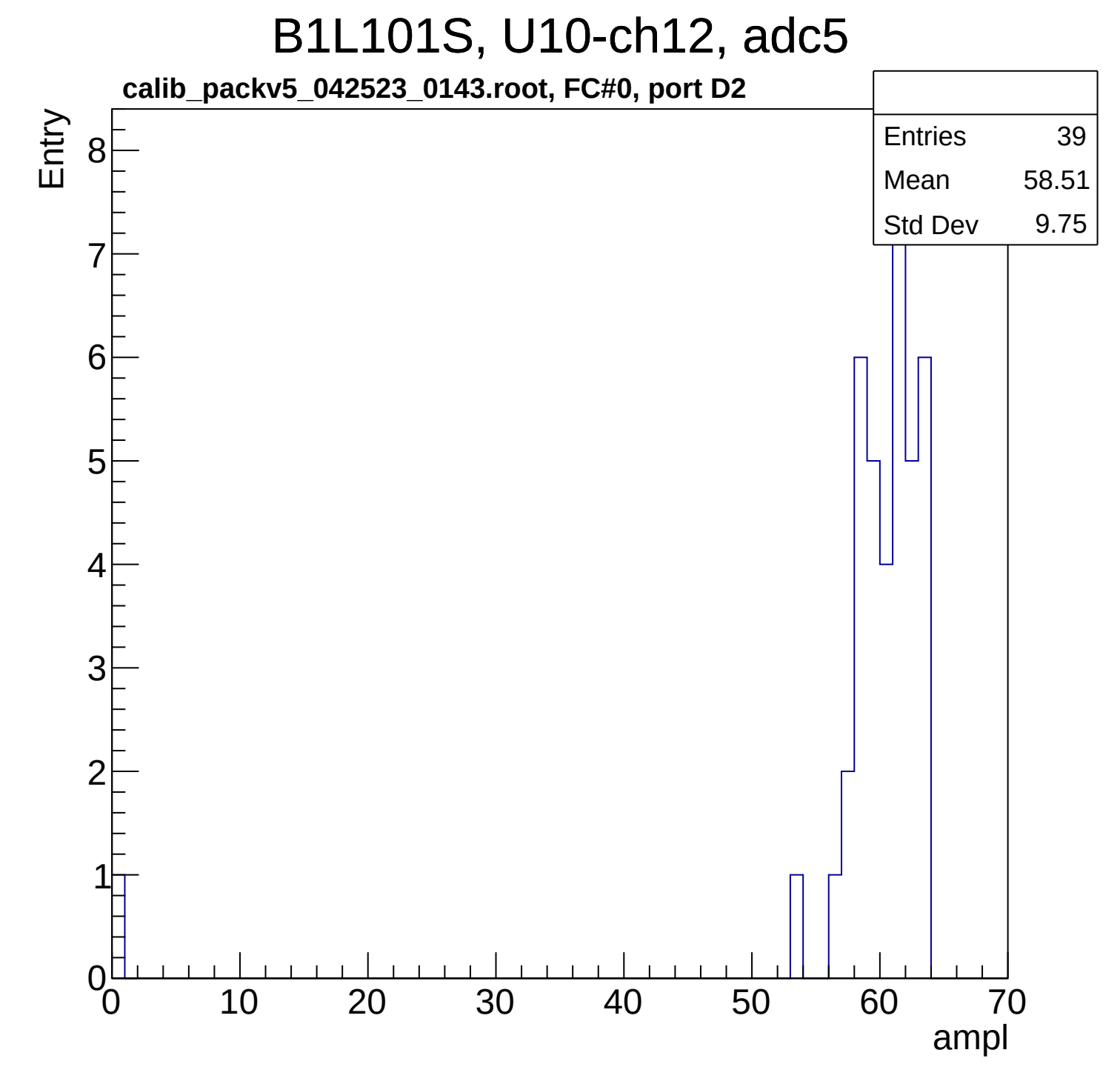
B1L101S, U10-ch12, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 39
Mean 58.51
Std Dev 9.75
Entry
ampl
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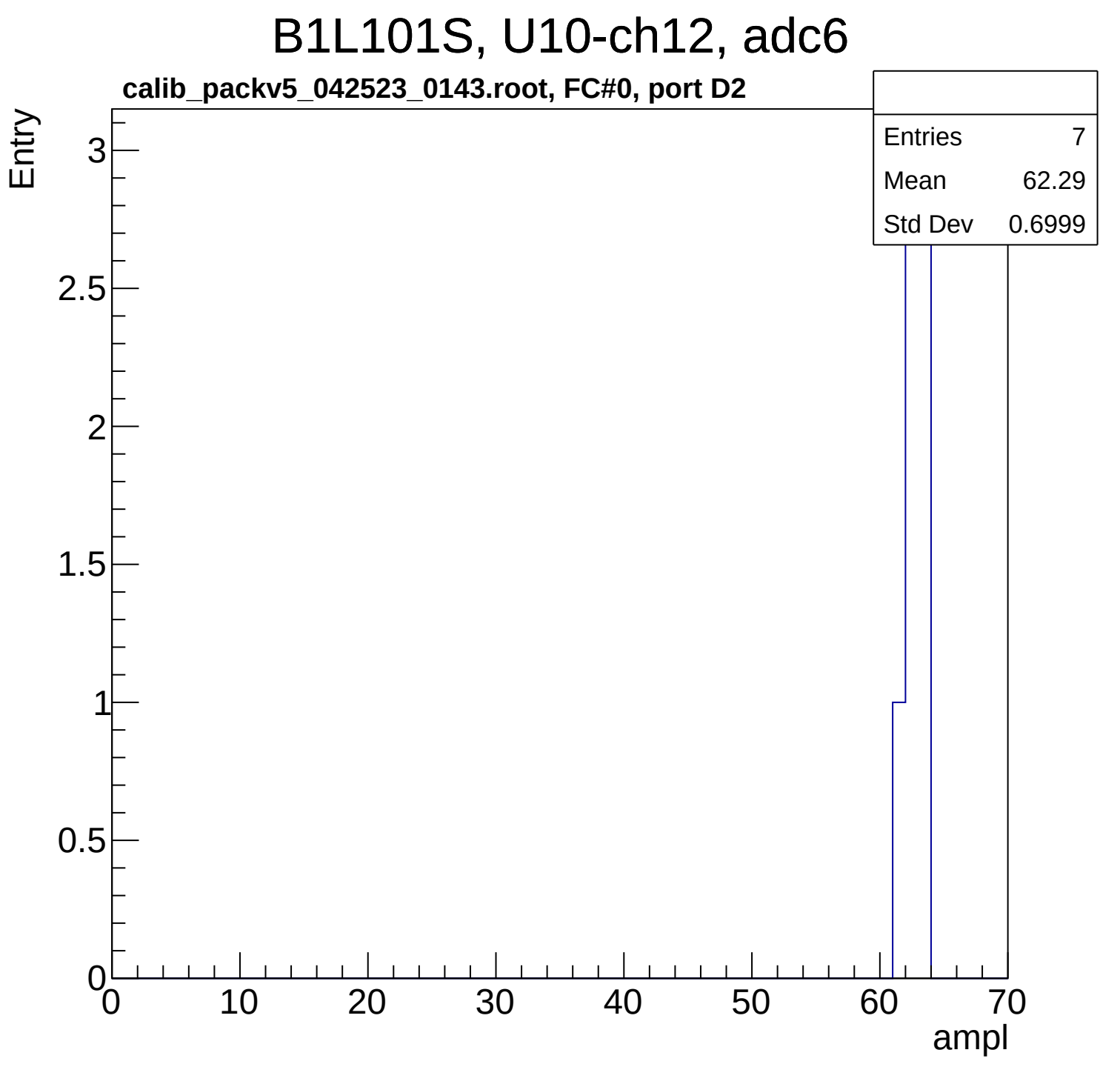
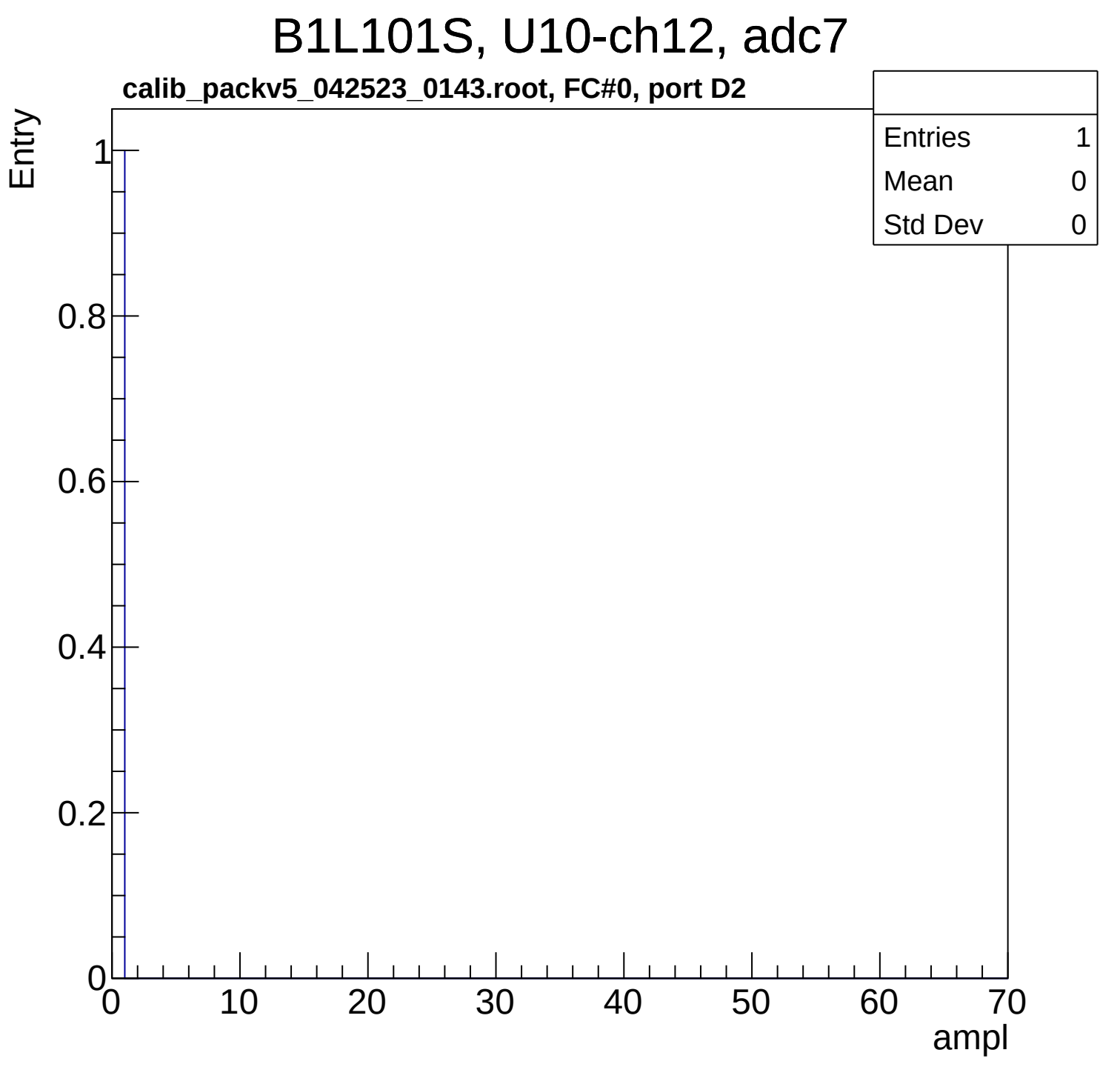
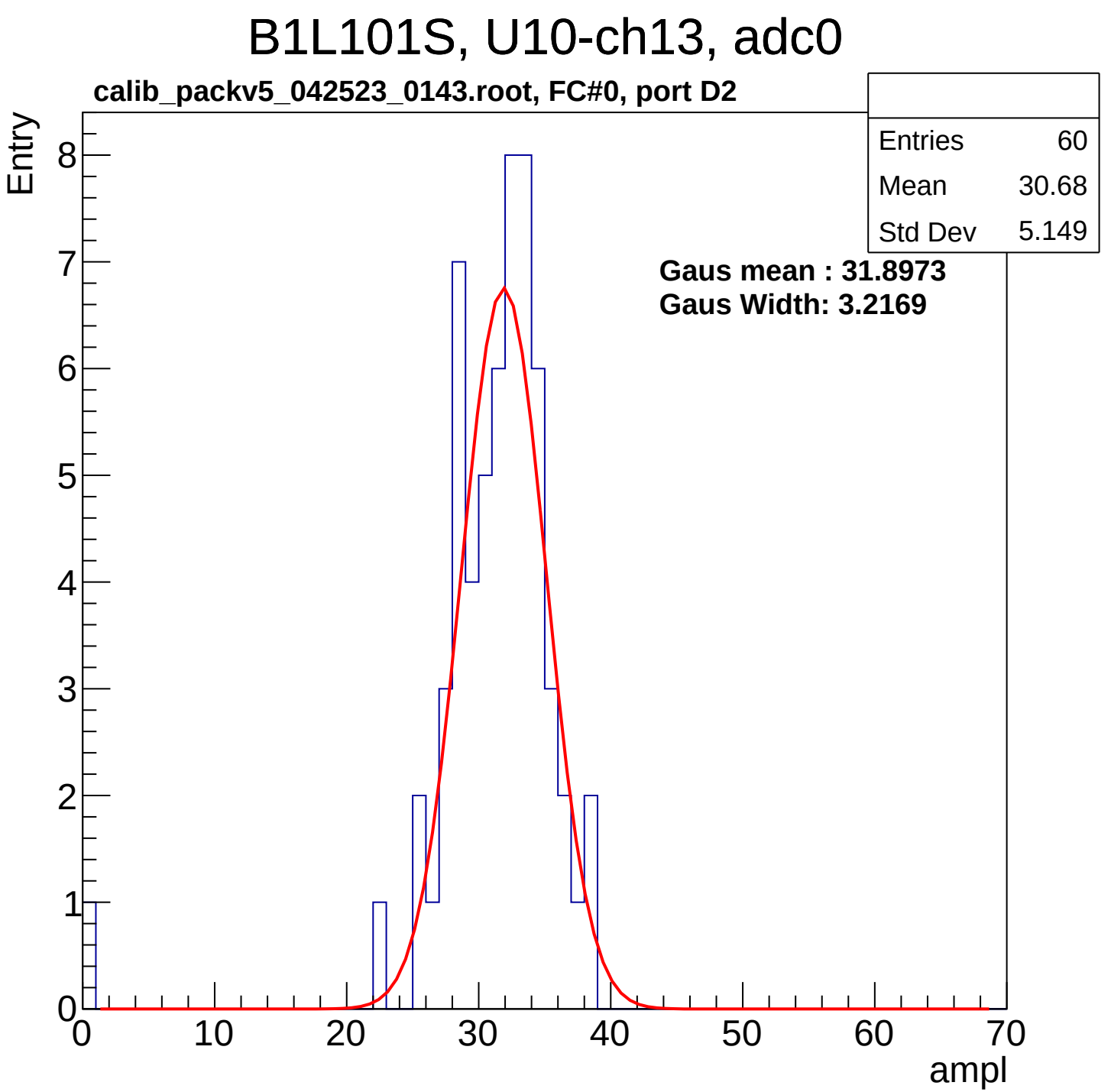
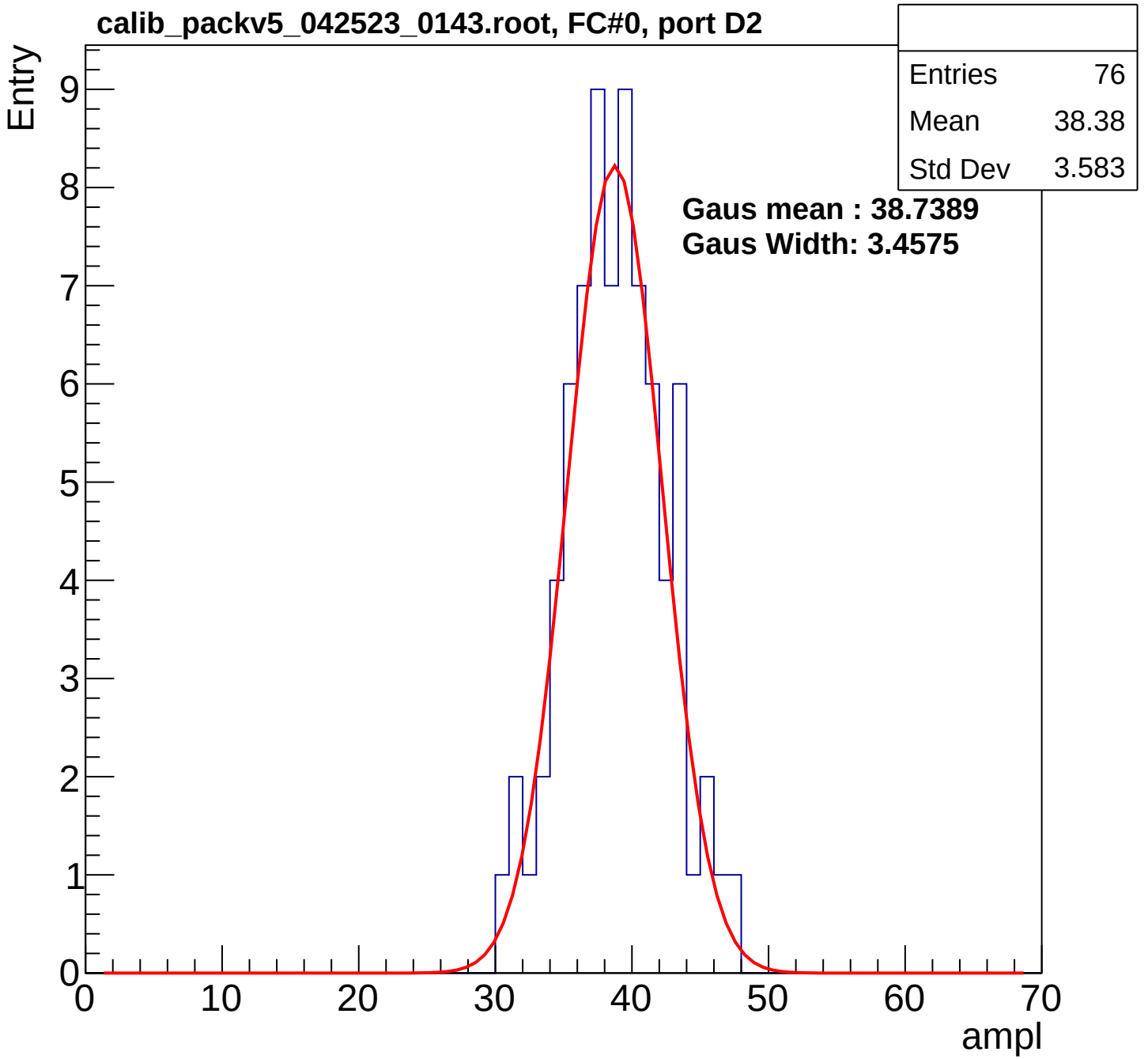
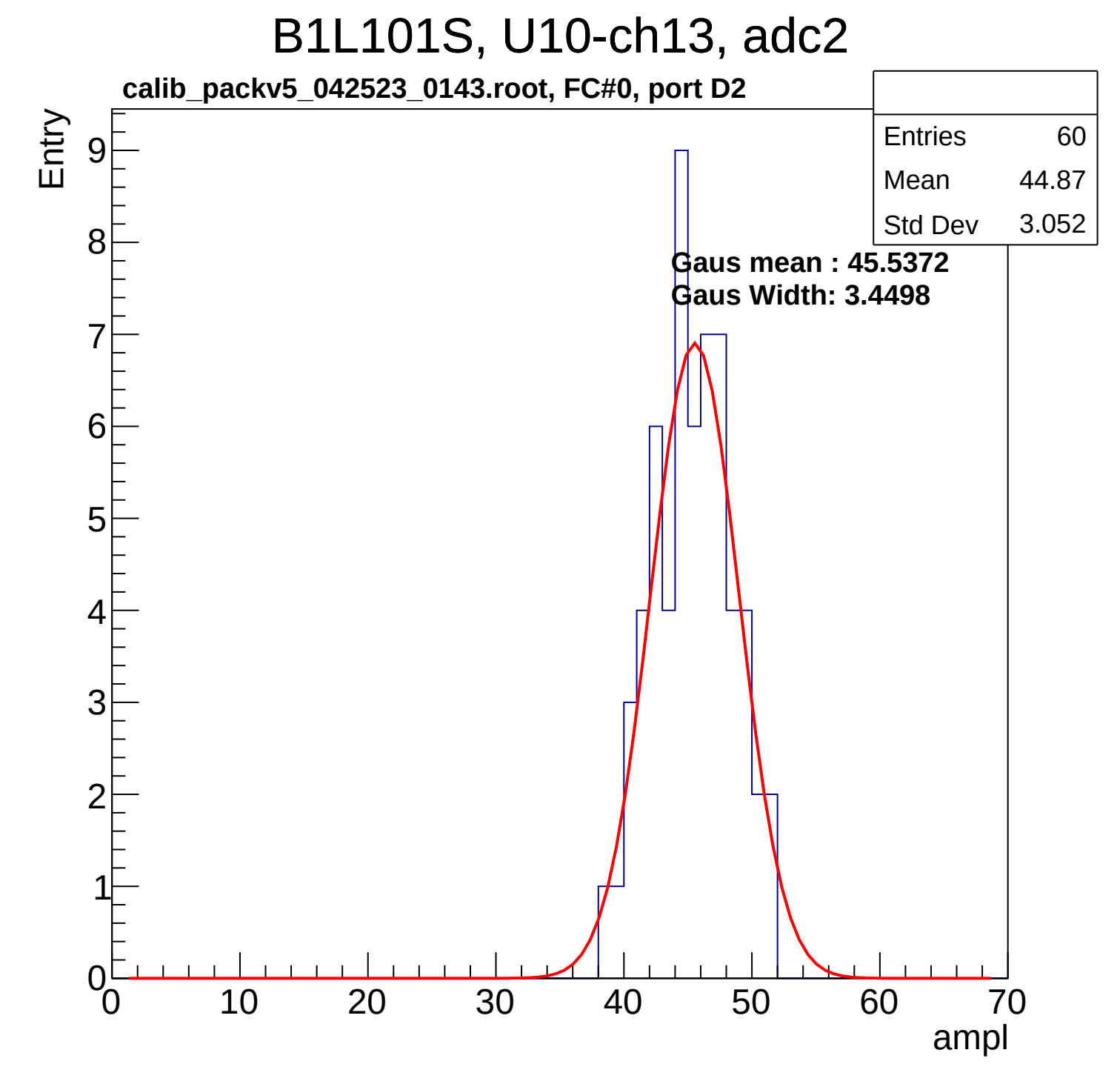
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

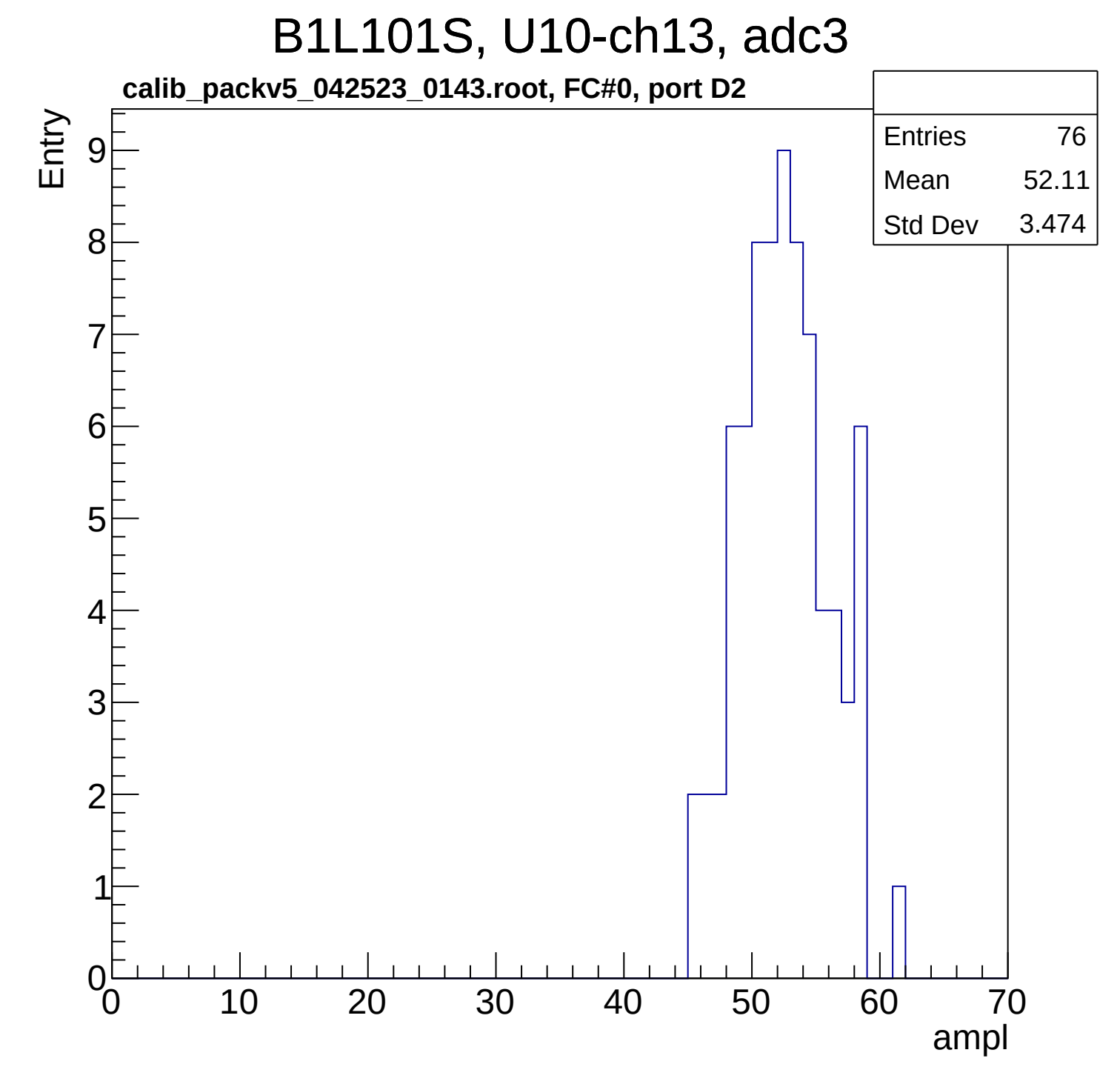

B1L101S, U10-ch12, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 62.29
Std Dev 0.6999
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

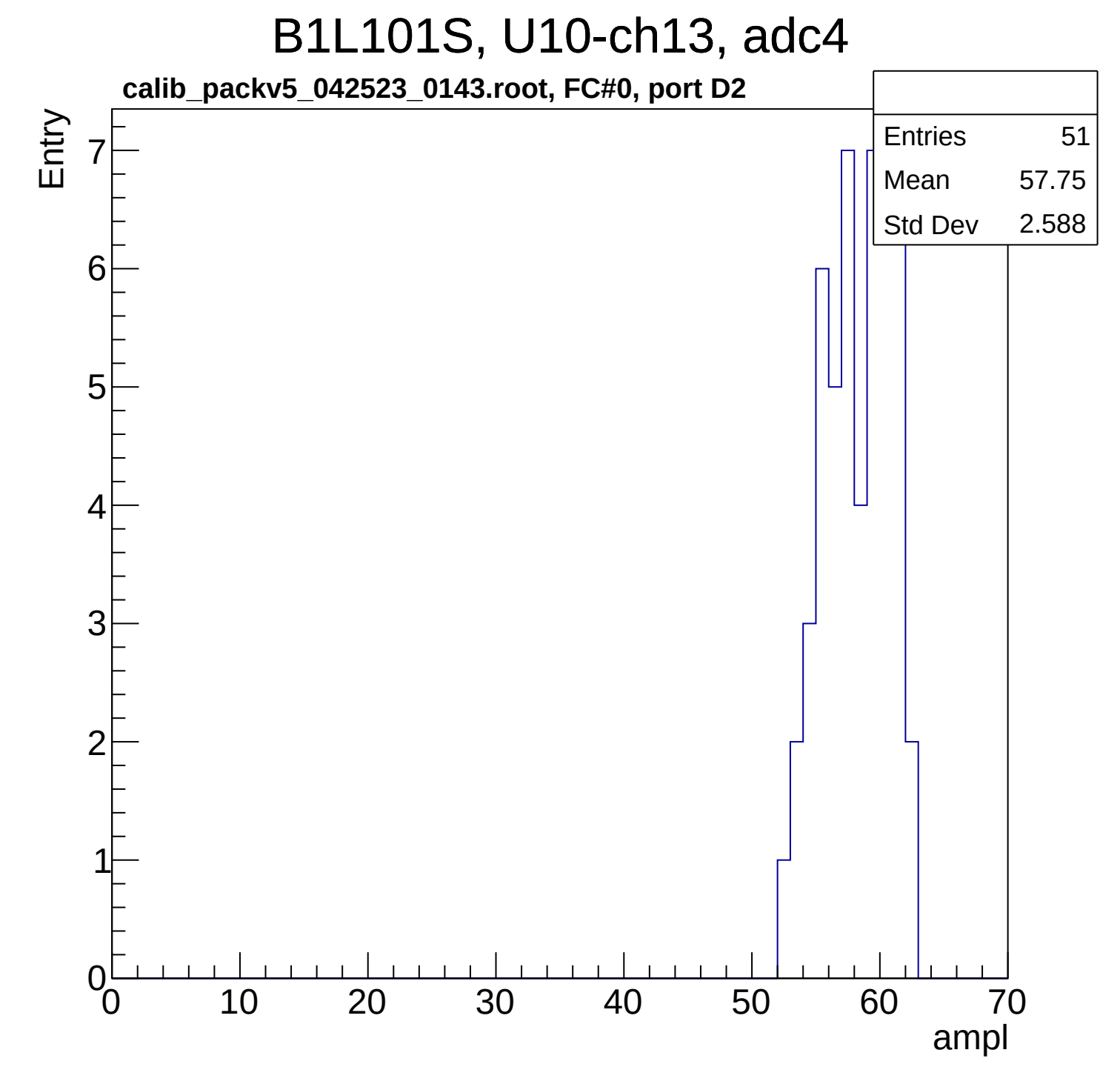

B1L101S, U10-ch12, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

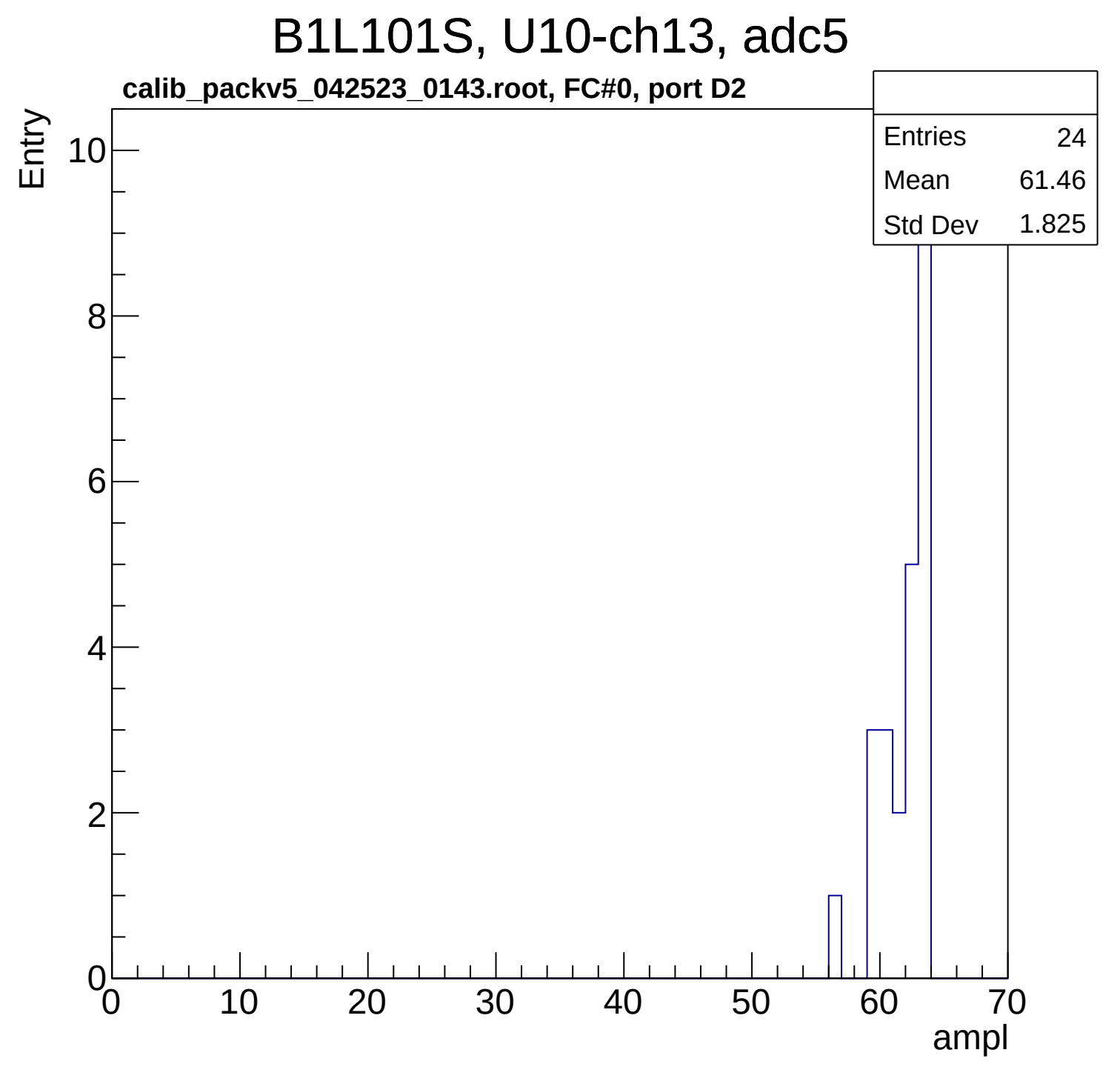

B1L101S, U10-ch13, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 30.68
Std Dev 5.149
Gaus mean : 31.8973
Gaus Width: 3.2169
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

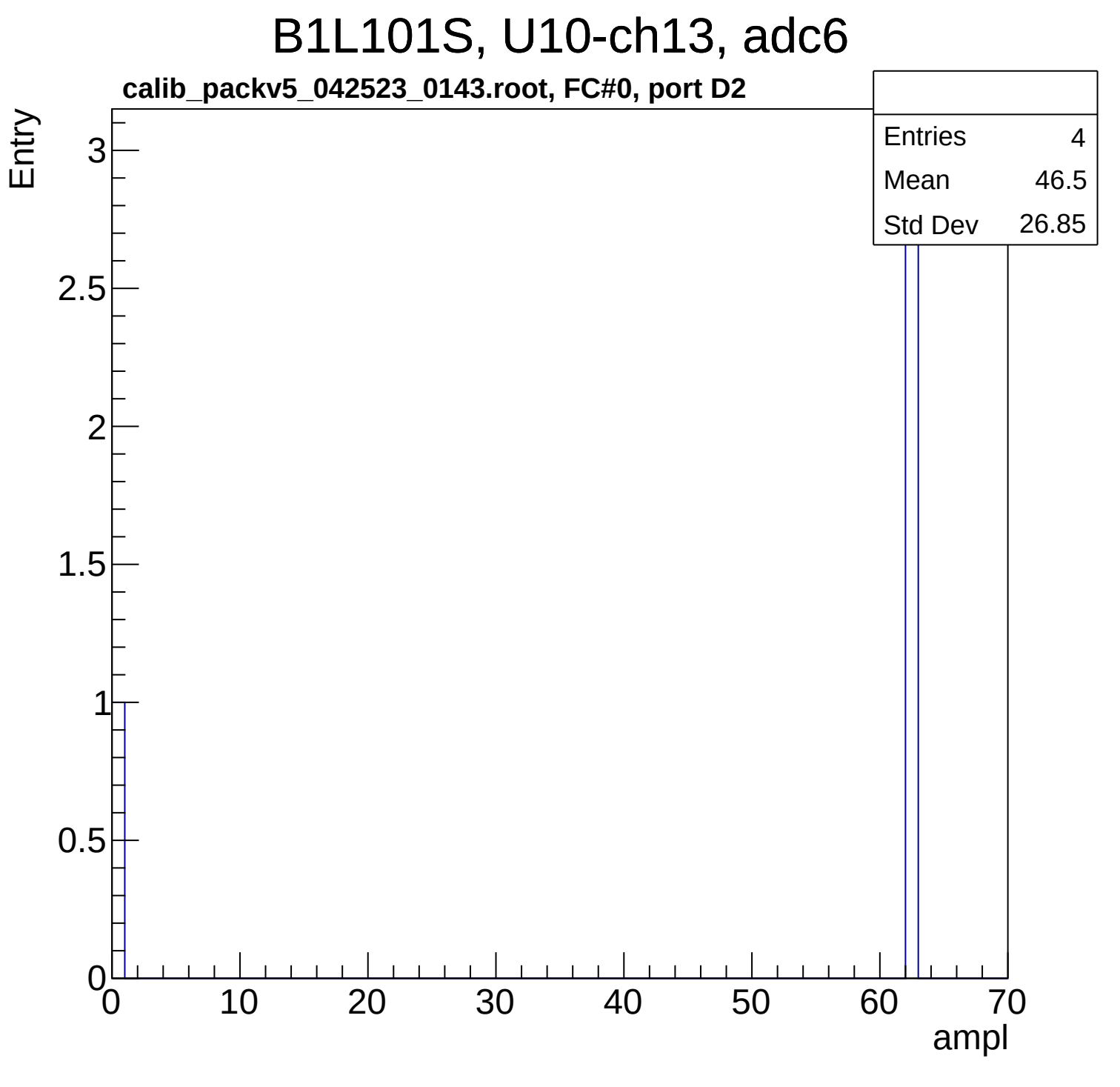

B1L101S, U10-ch13, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 38.38
Std Dev 3.583
Gaus mean : 38.7389
Gaus Width: 3.4575
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch13, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 44.87
Std Dev 3.052
Gaus mean : 45.5372
Gaus Width: 3.4498
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L101S, U10-ch13, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 52.11
Std Dev 3.474
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch13, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 57.75
Std Dev 2.588
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U10-ch13, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 24
Mean 61.46
Std Dev 1.825
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch13, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 46.5
Std Dev 26.85
Entry
ampl
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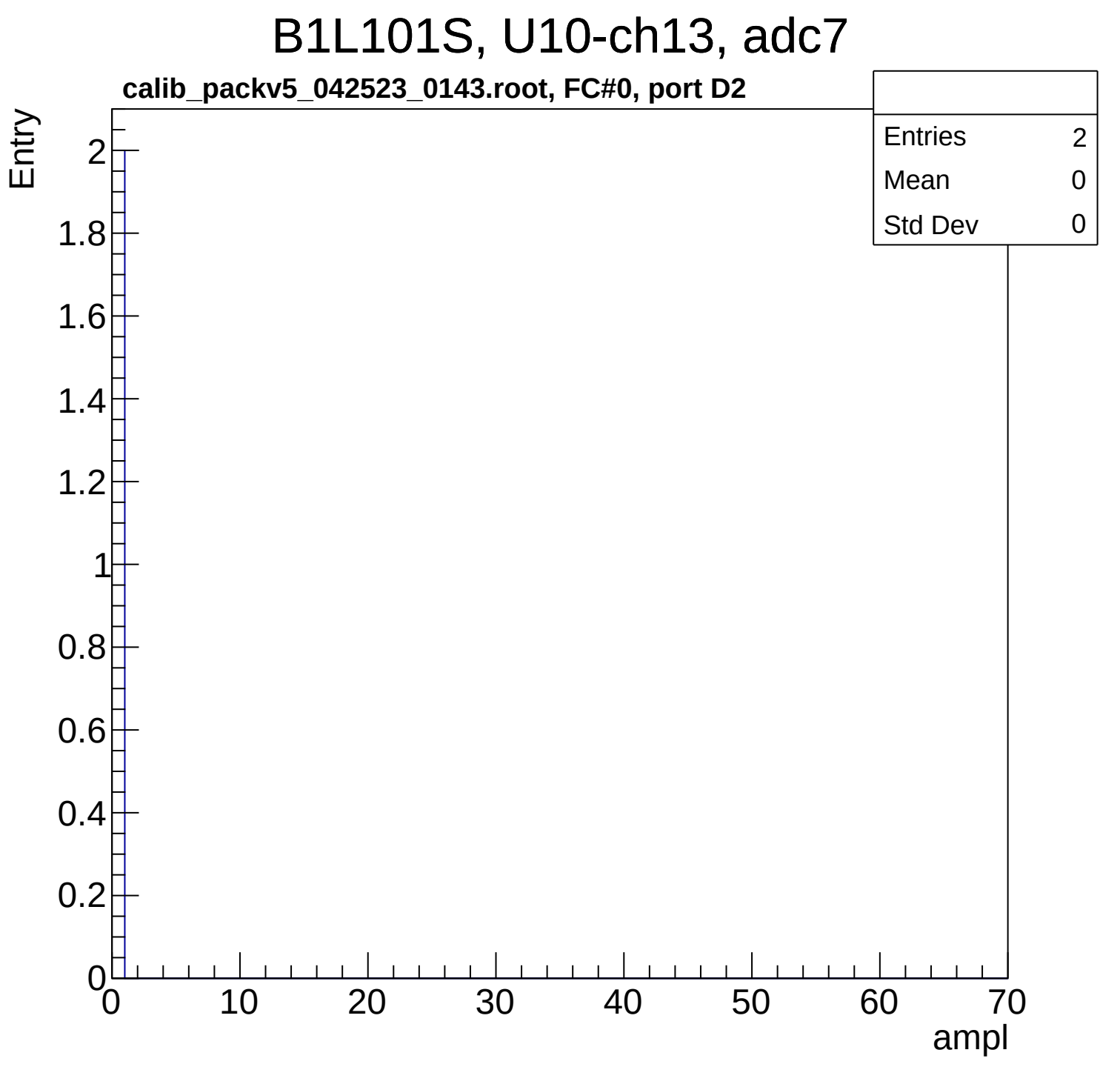
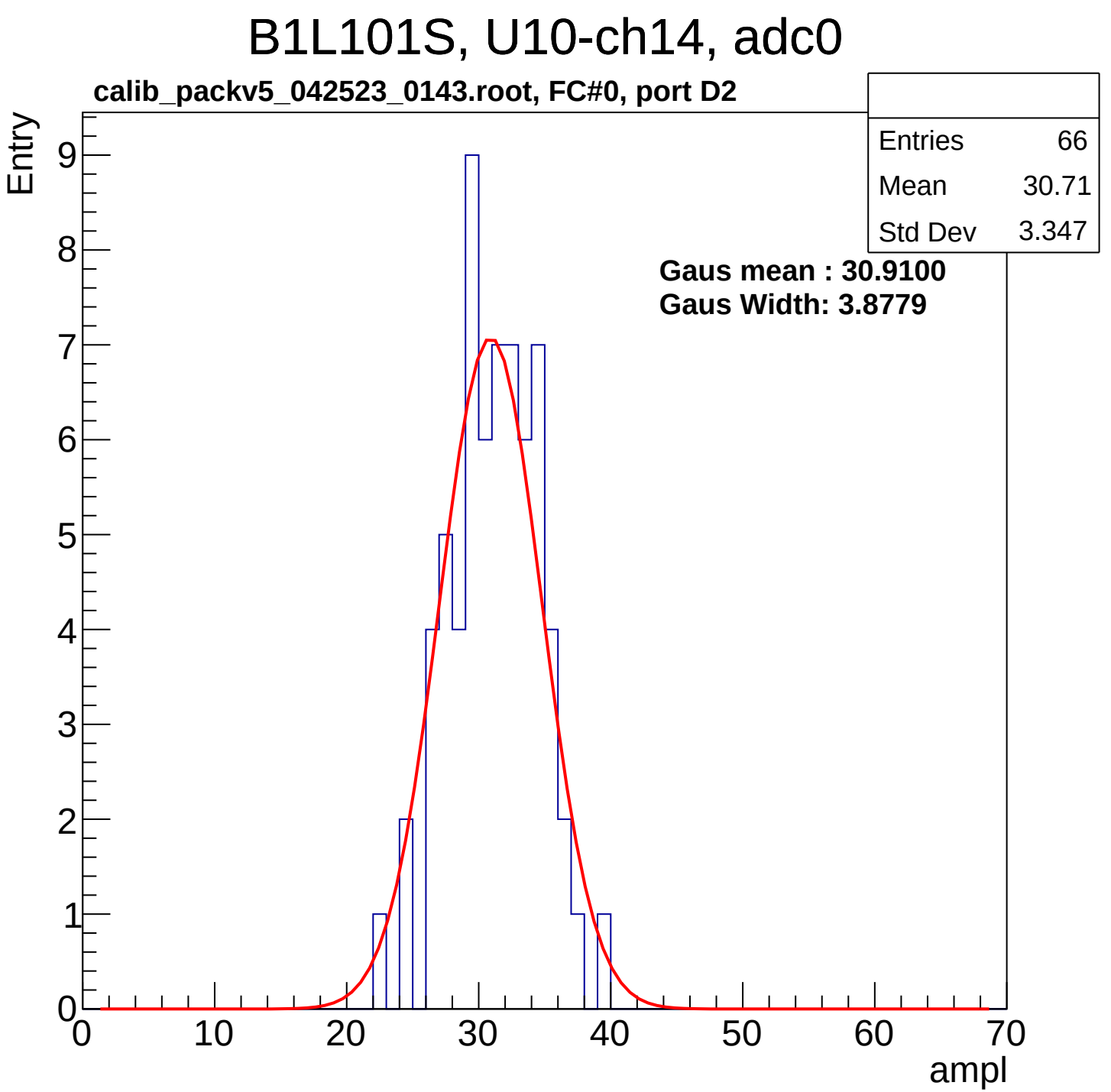
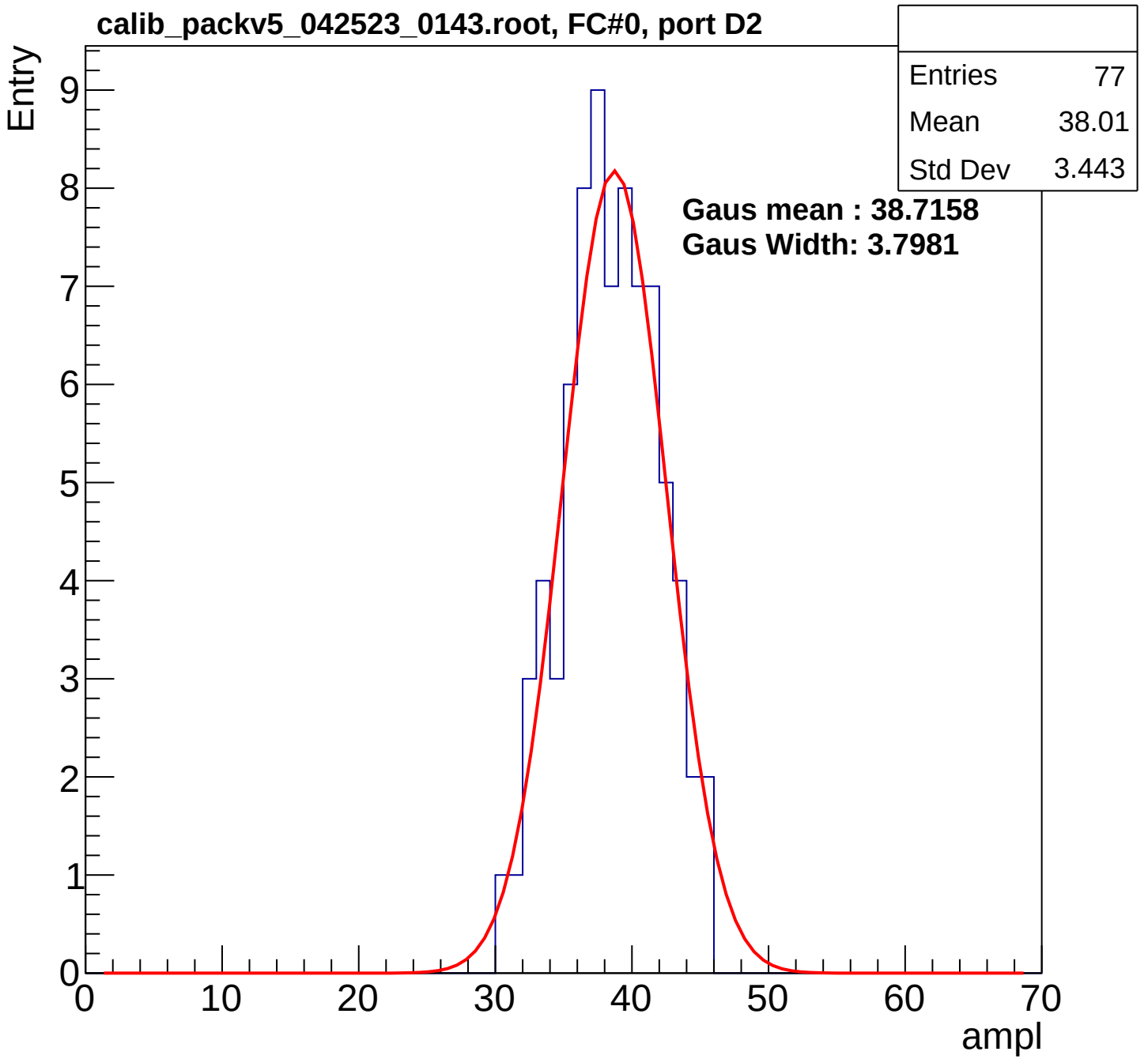
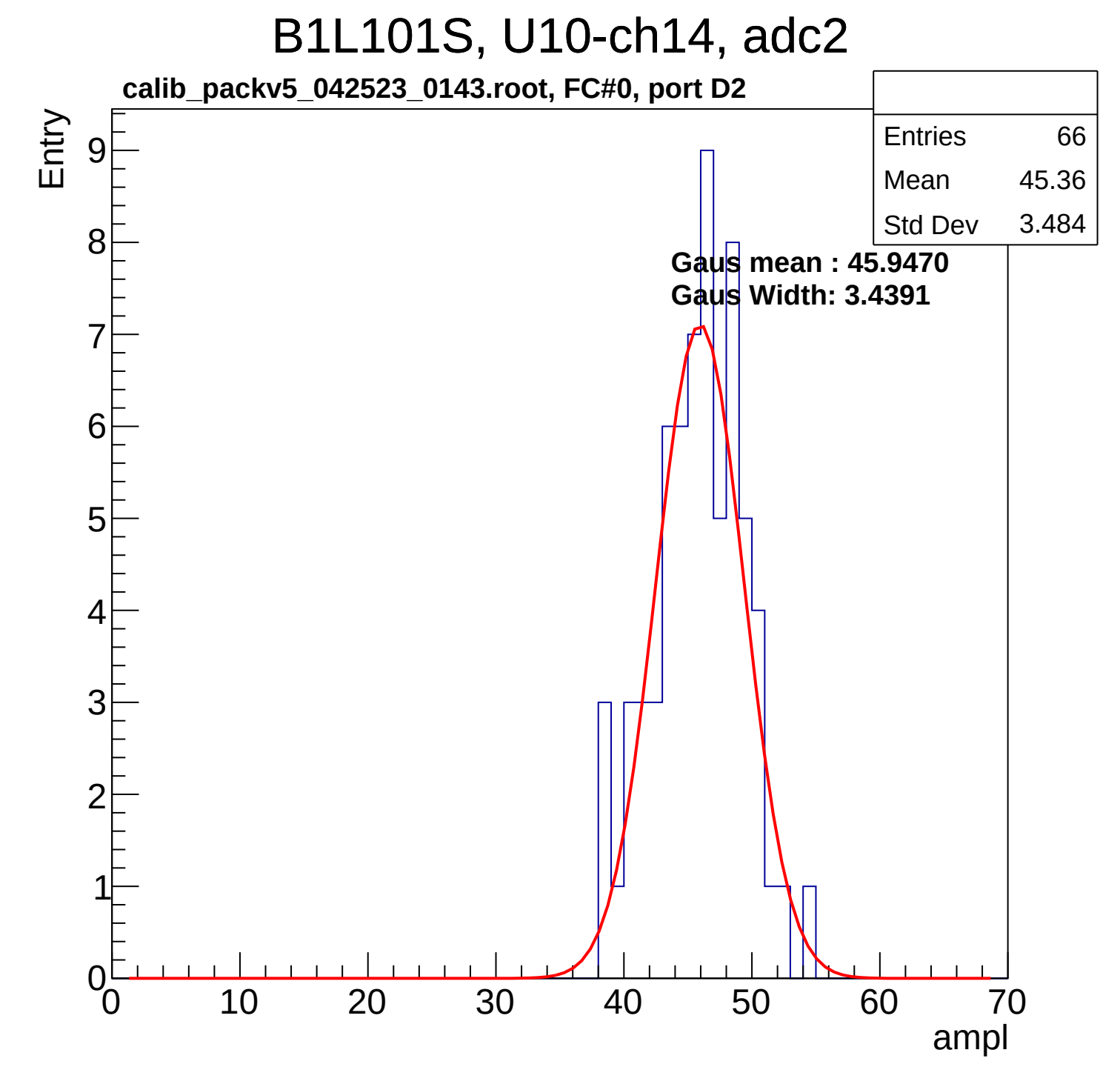
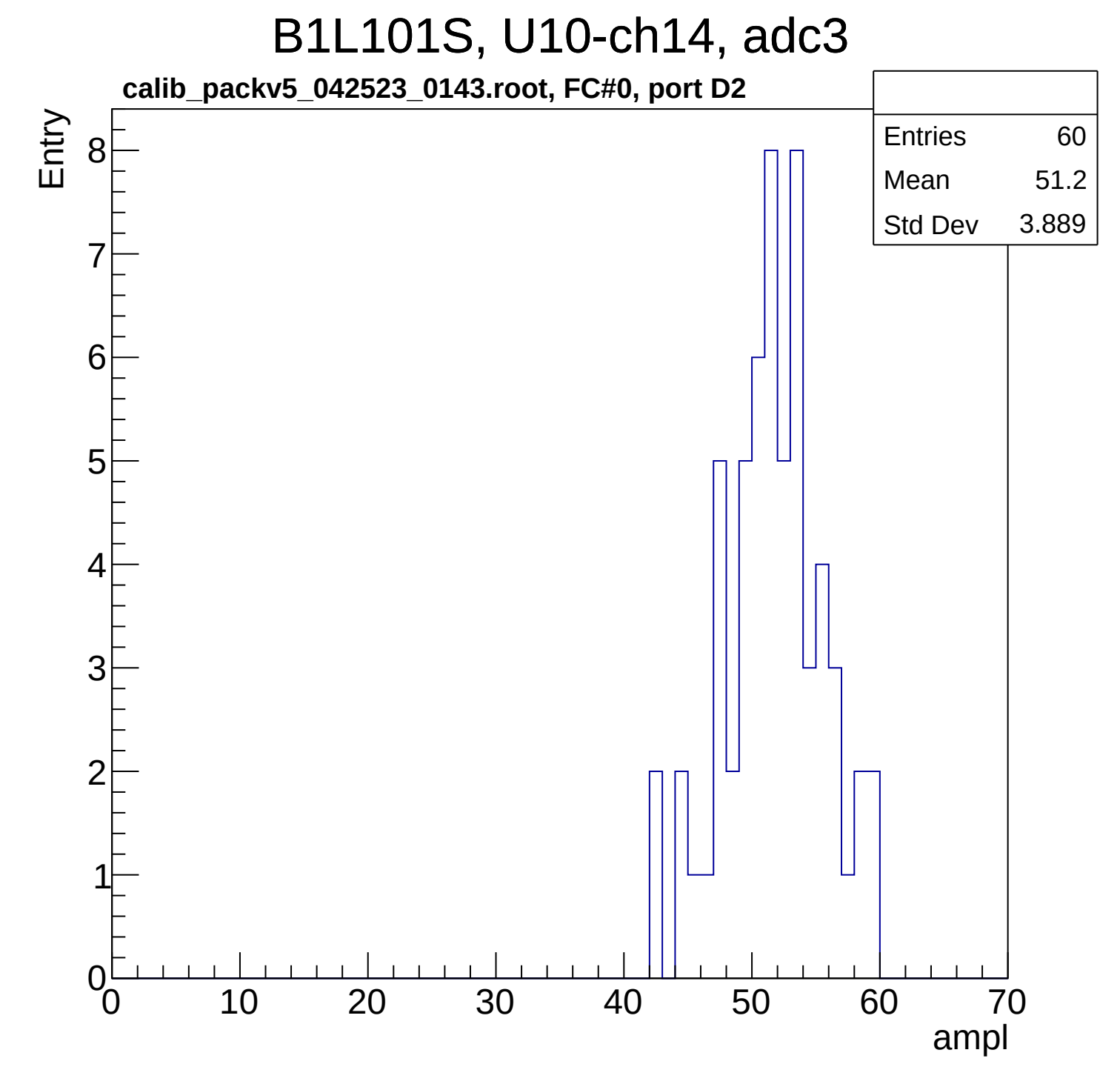
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U10-ch13, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch14, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 30.71
Std Dev 3.347
Gaus mean : 30.9100
Gaus Width: 3.8779
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch14, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 38.01
Std Dev 3.443
Gaus mean : 38.7158
Gaus Width: 3.7981
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch14, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 45.36
Std Dev 3.484
Gaus mean : 45.9470
Gaus Width: 3.4391
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch14, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 51.2
Std Dev 3.889
Entry
ampl
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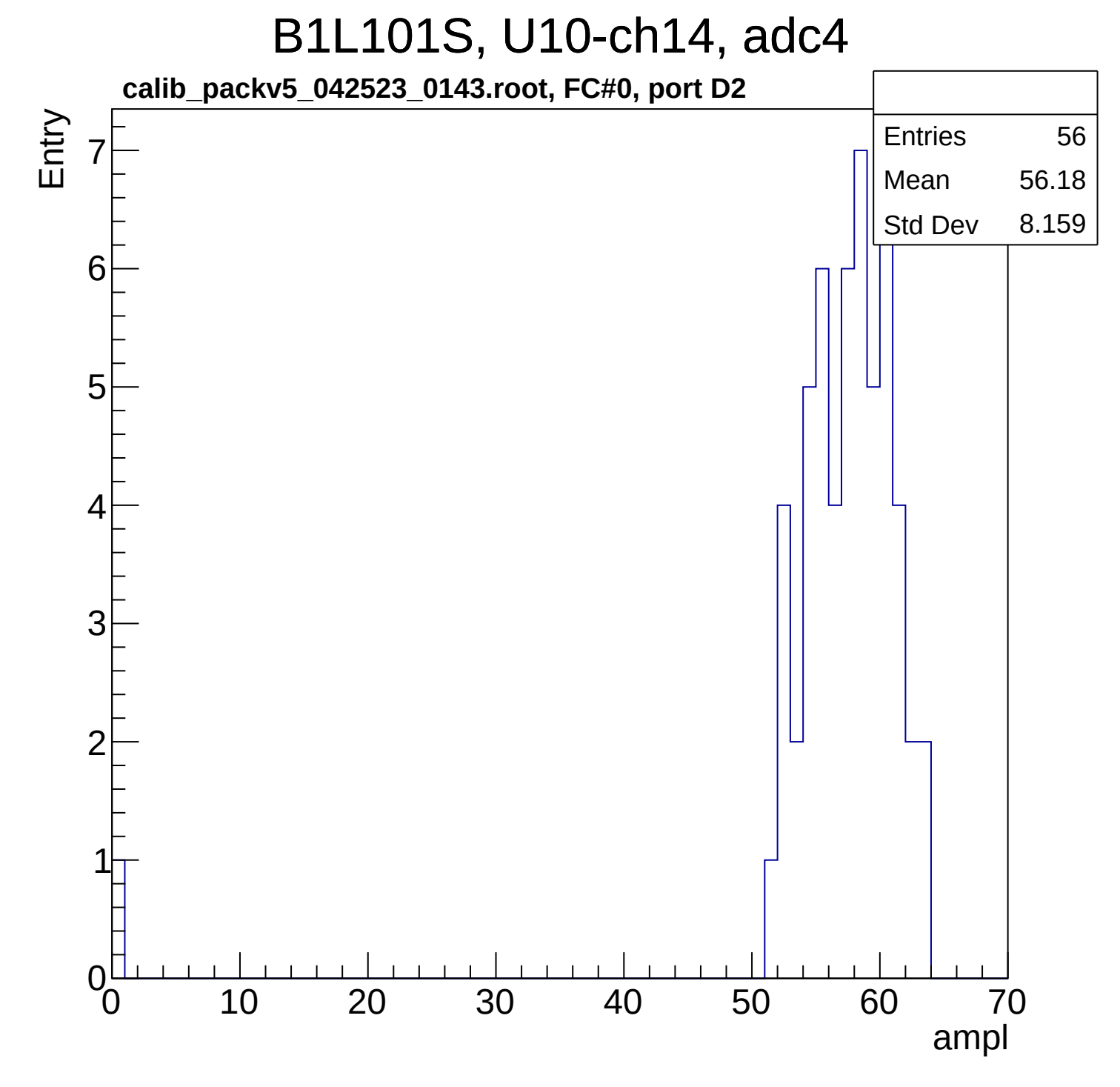
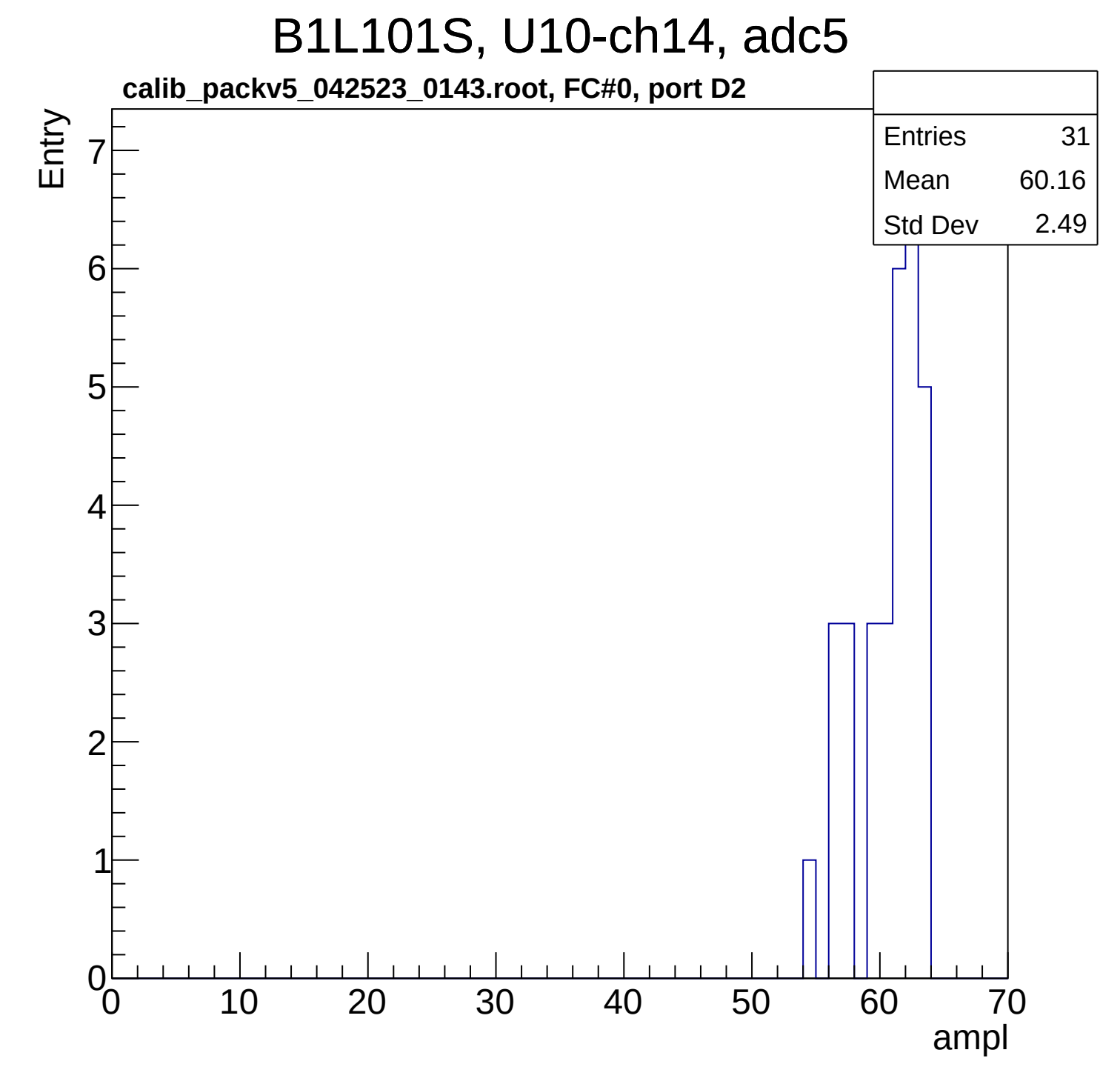
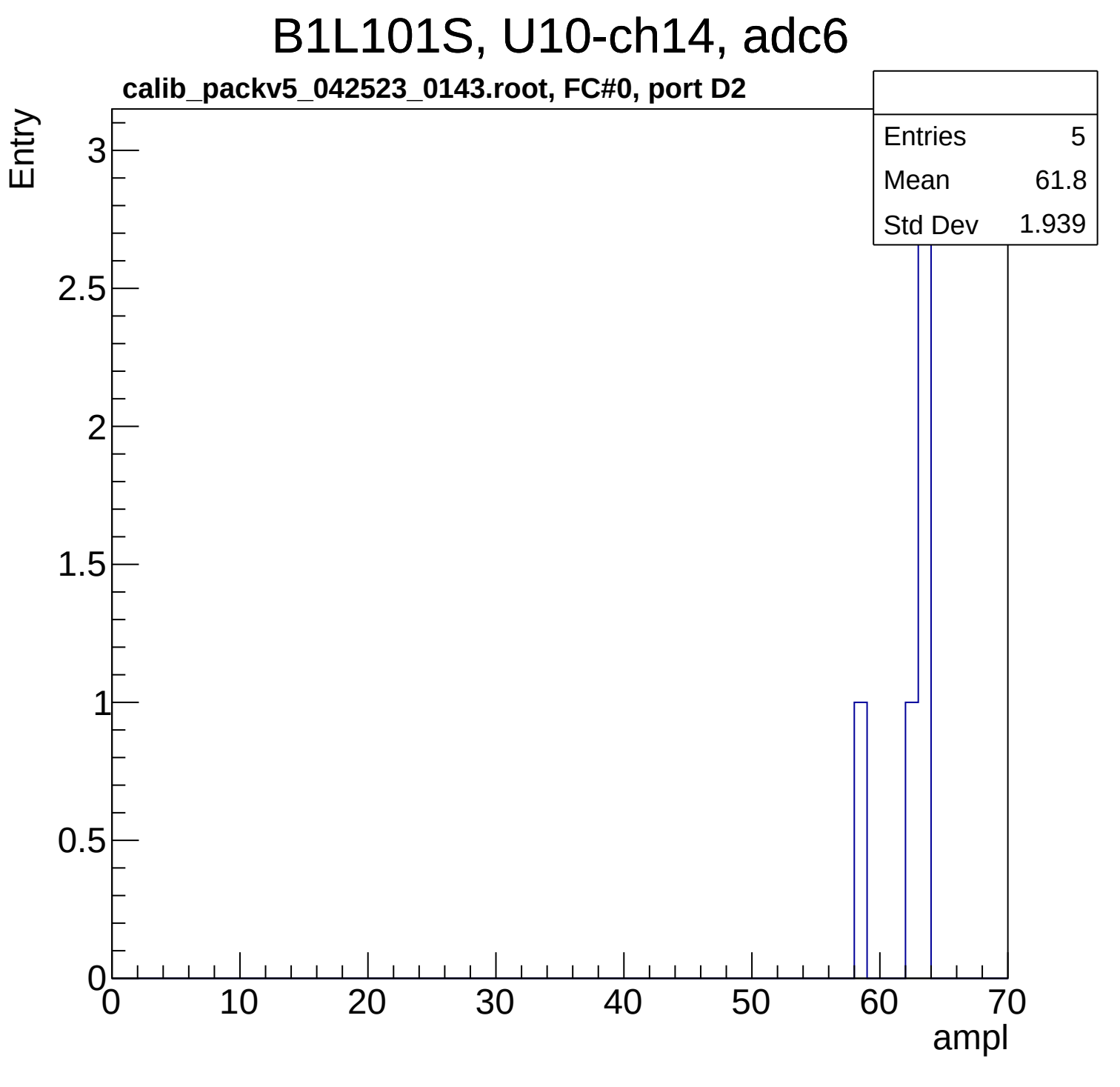
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch14, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 56.18
Std Dev 8.159
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U10-ch14, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 31
Mean 60.16
Std Dev 2.49
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U10-ch14, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 61.8
Std Dev 1.939
Entry
ampl
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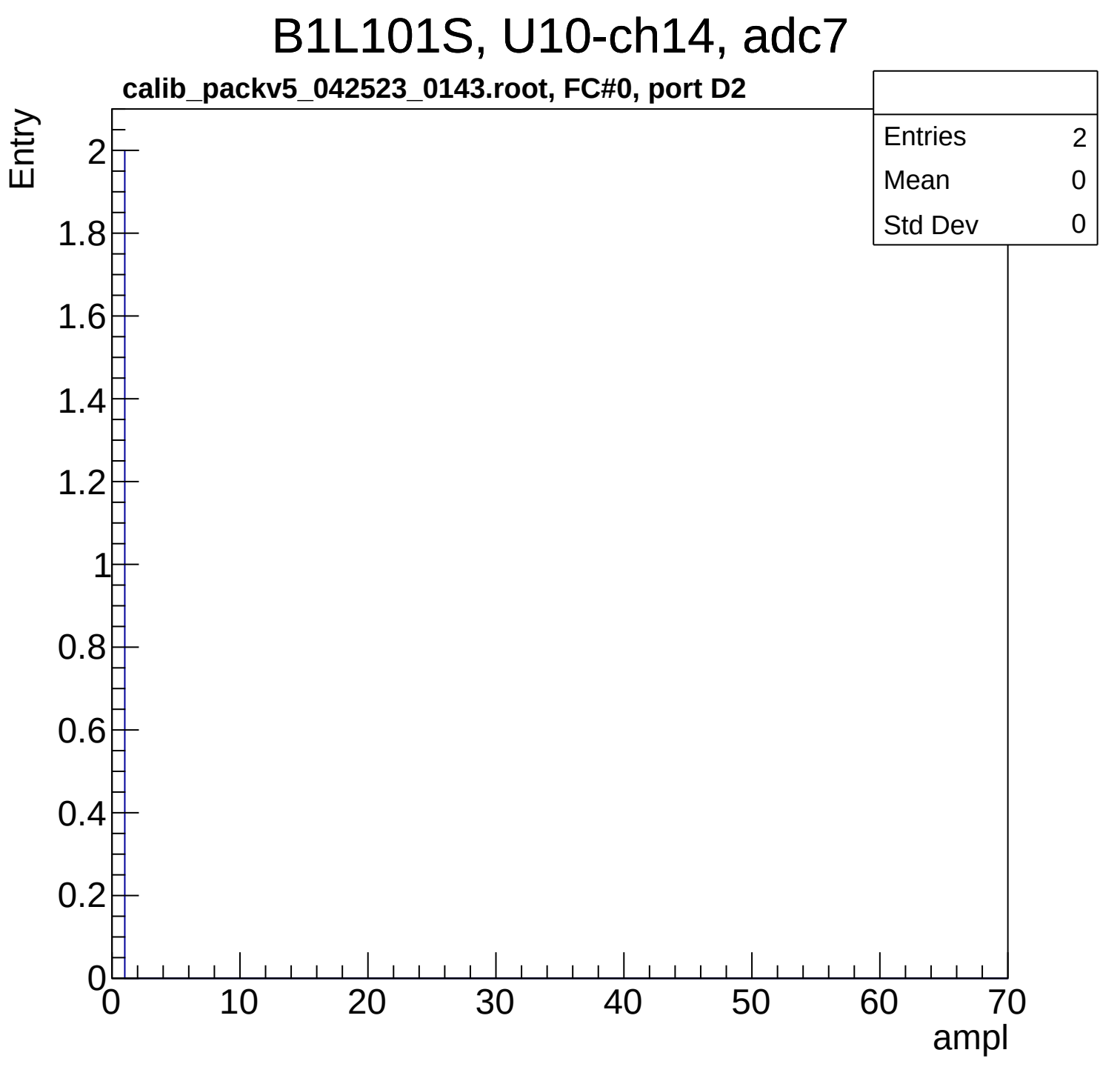
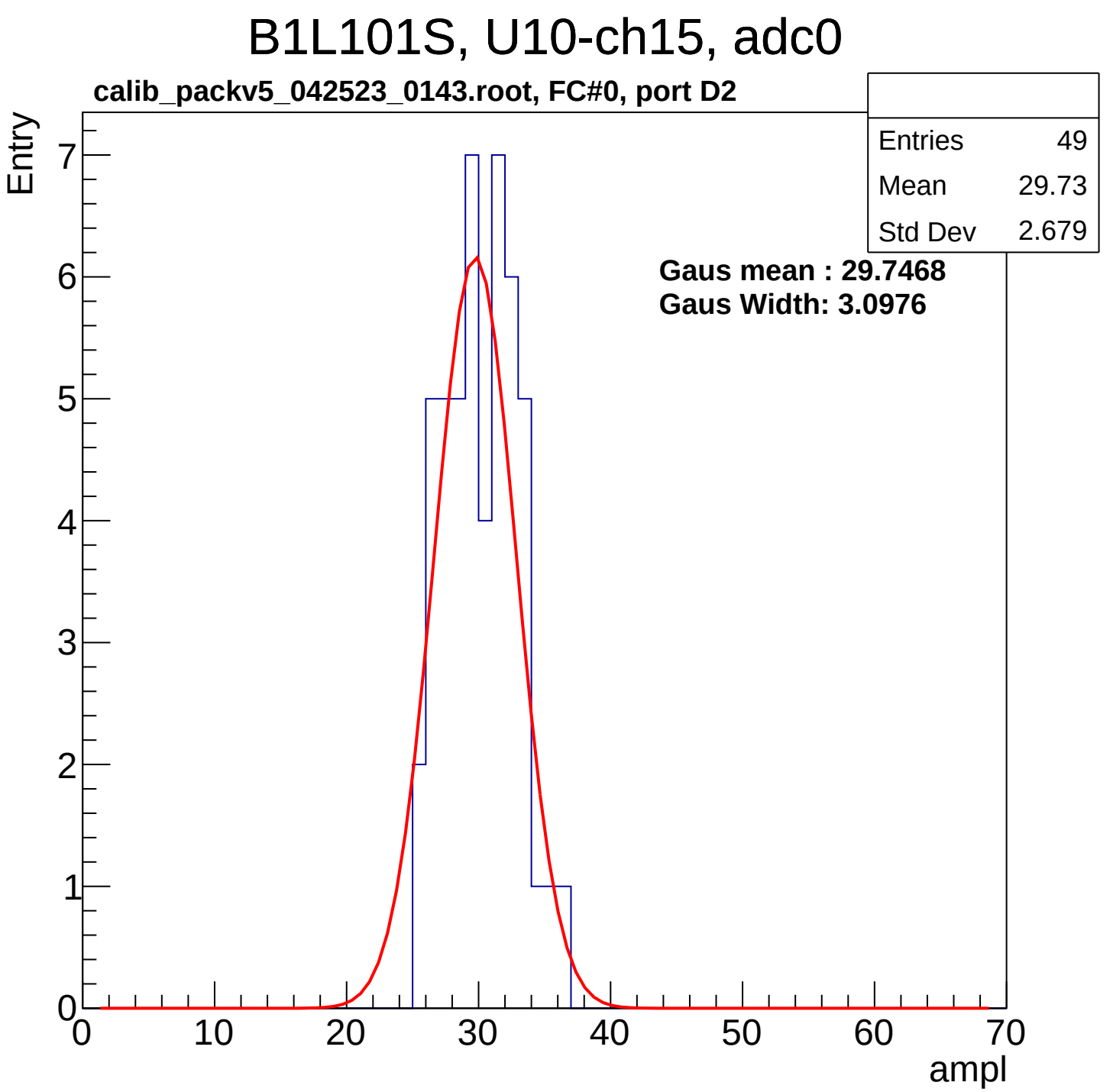
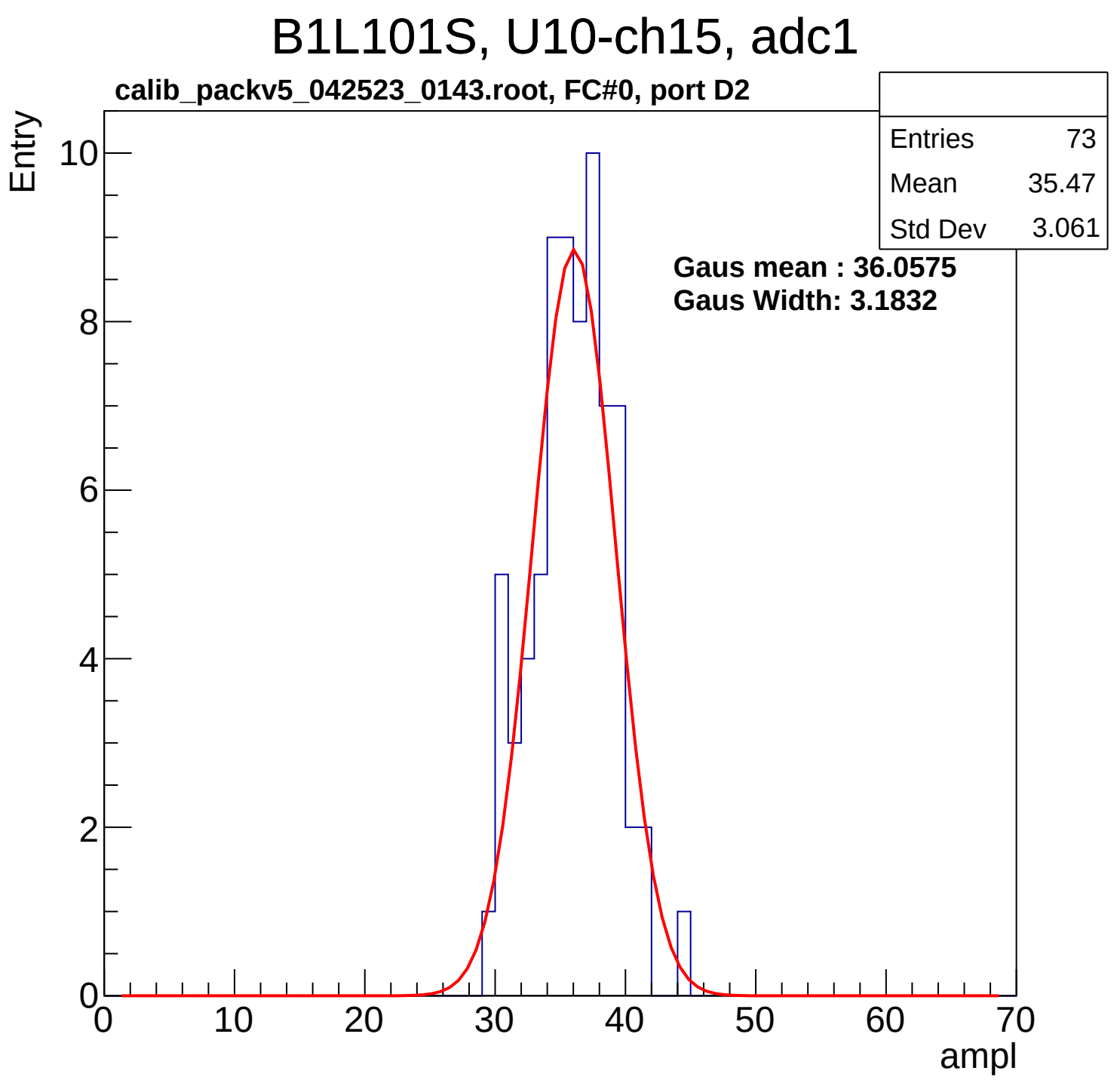
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U10-ch14, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U10-ch15, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 29.73
Std Dev 2.679
Gaus mean : 29.7468
Gaus Width: 3.0976
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U10-ch15, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 35.47
Std Dev 3.061
Gaus mean : 36.0575
Gaus Width: 3.1832
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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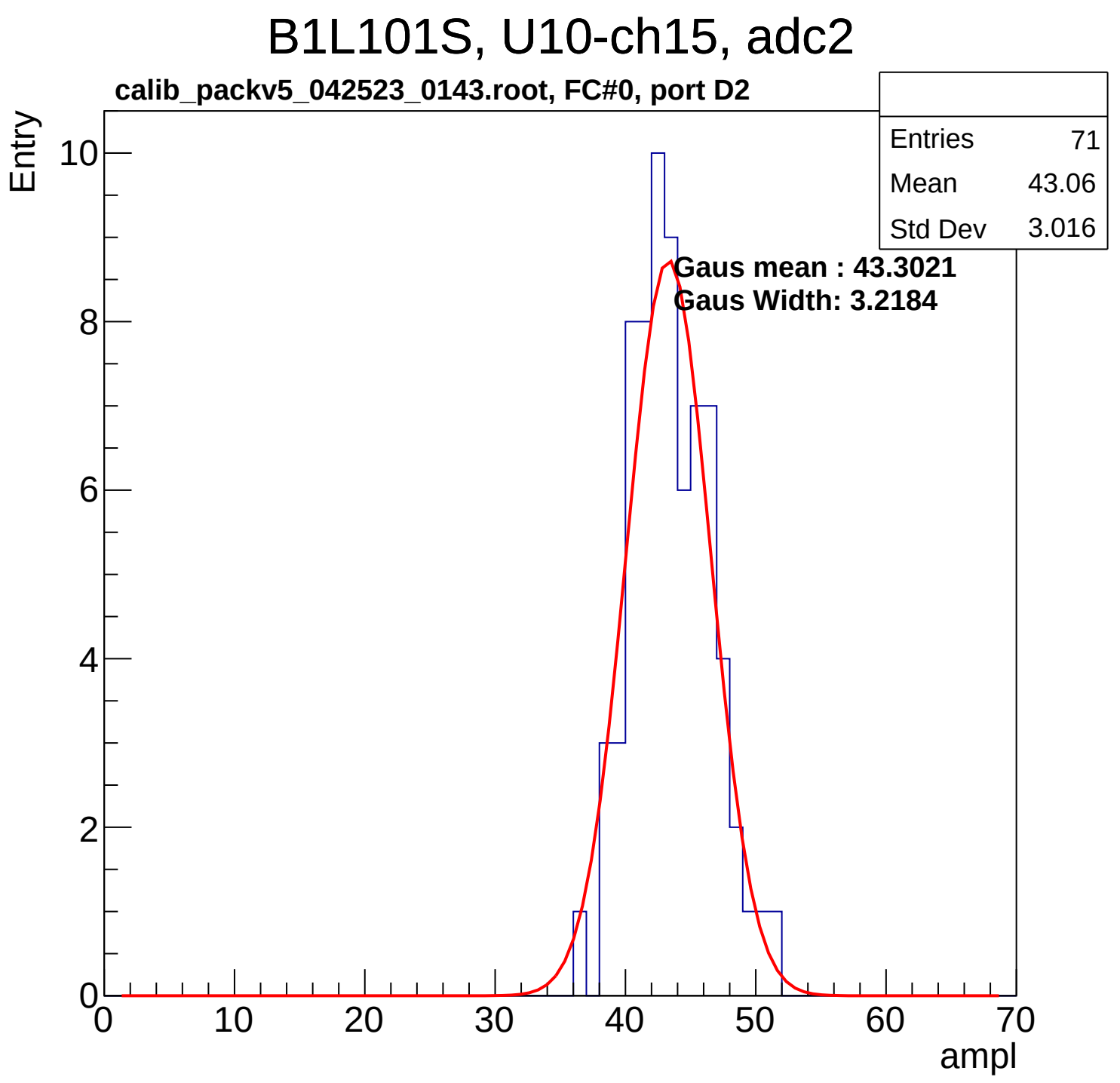
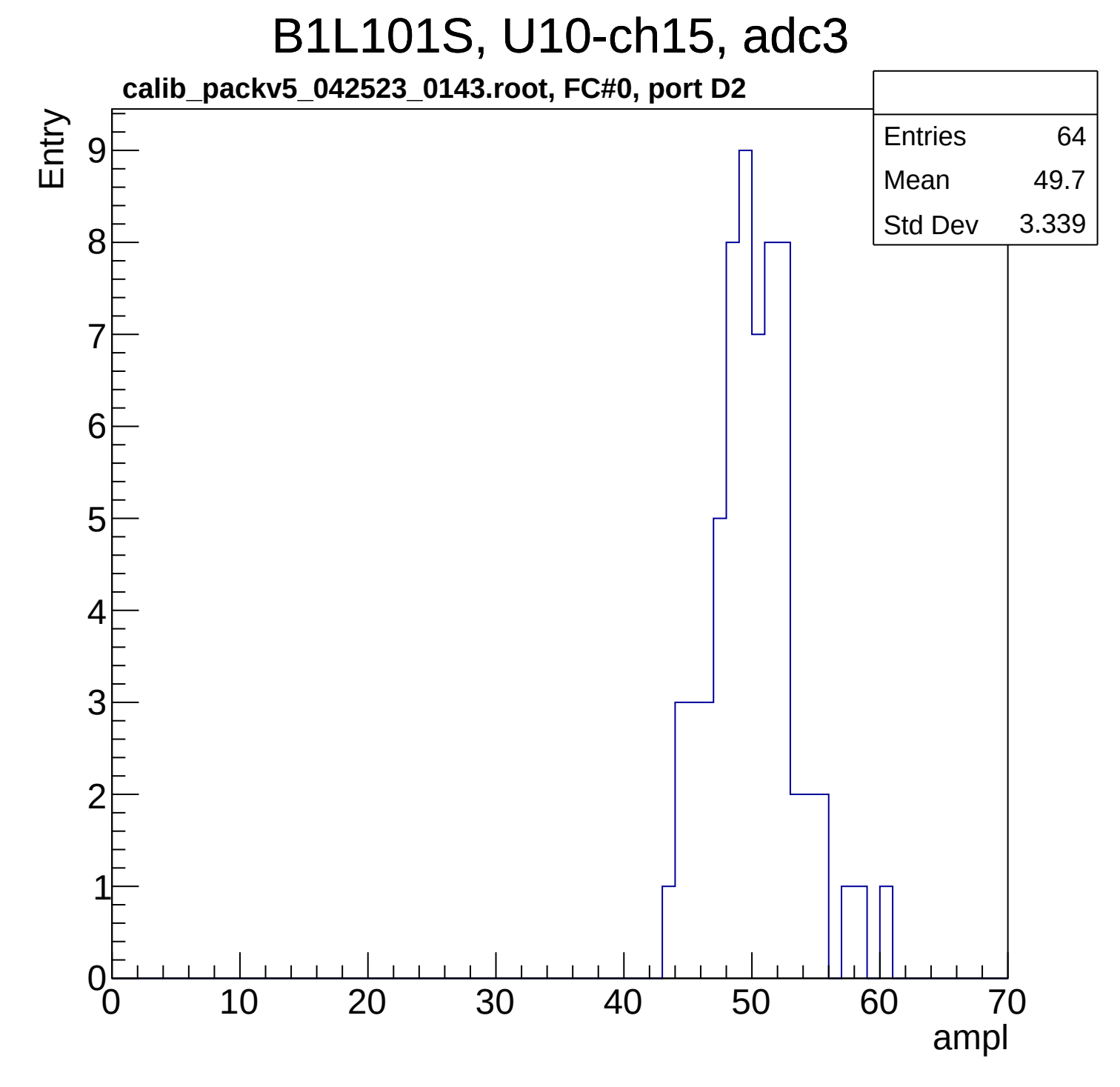

B1L101S, U10-ch15, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 43.06
Std Dev 3.016
Gaus mean : 43.3021
Gaus Width: 3.2184
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch15, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 49.7
Std Dev 3.339
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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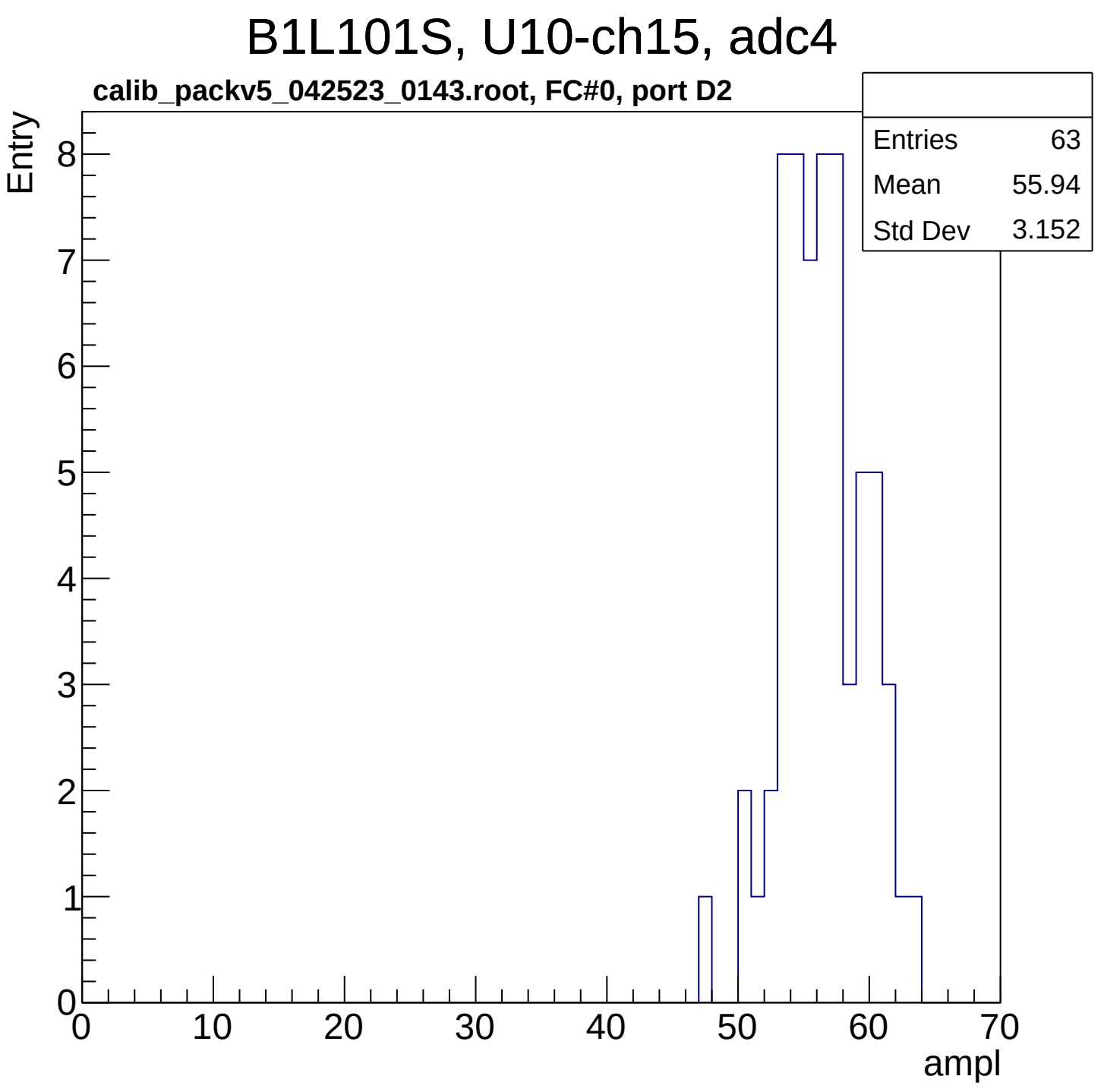
B1L101S, U10-ch15, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 55.94
Std Dev 3.152
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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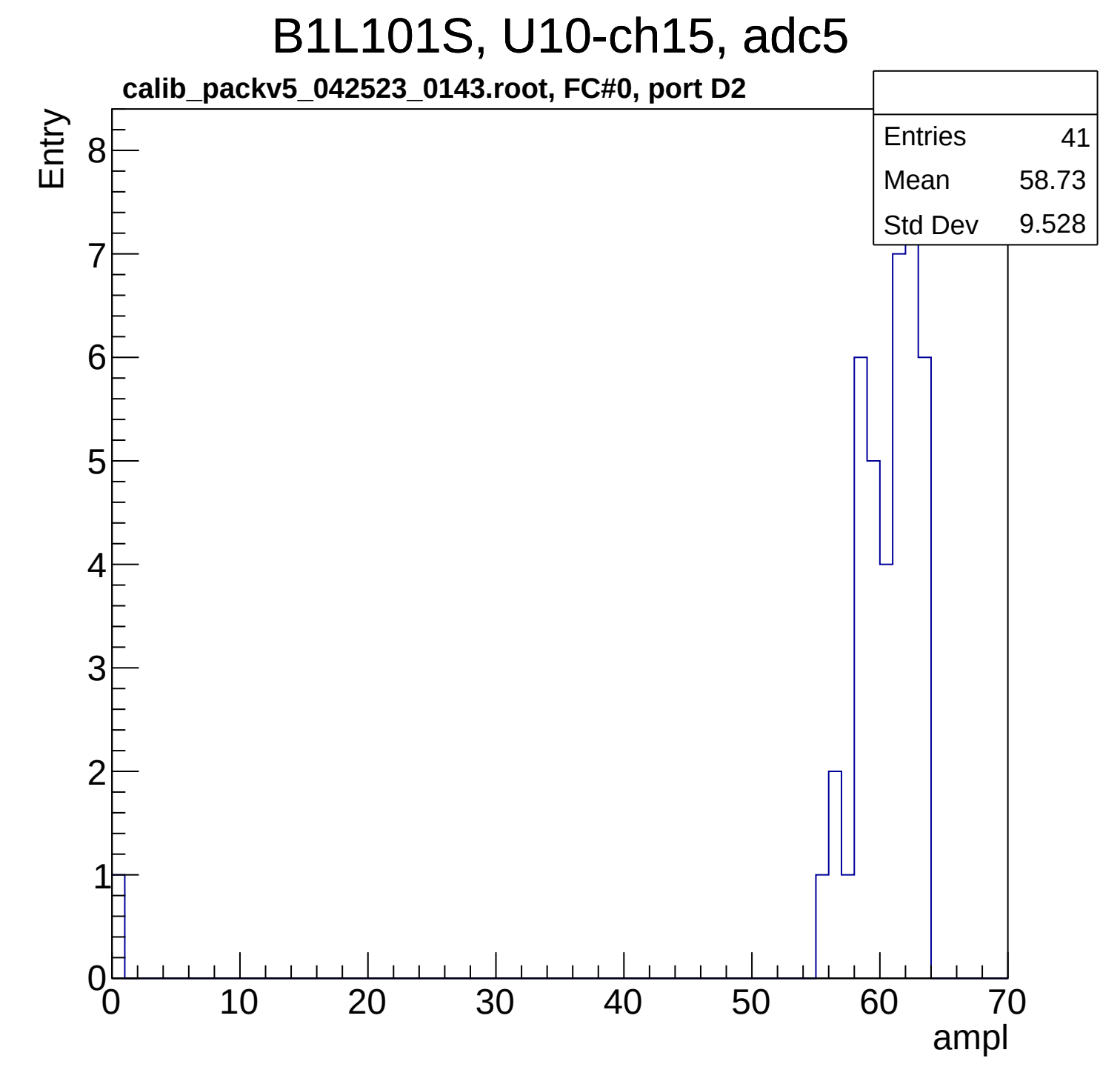
B1L101S, U10-ch15, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 41
Mean 58.73
Std Dev 9.528
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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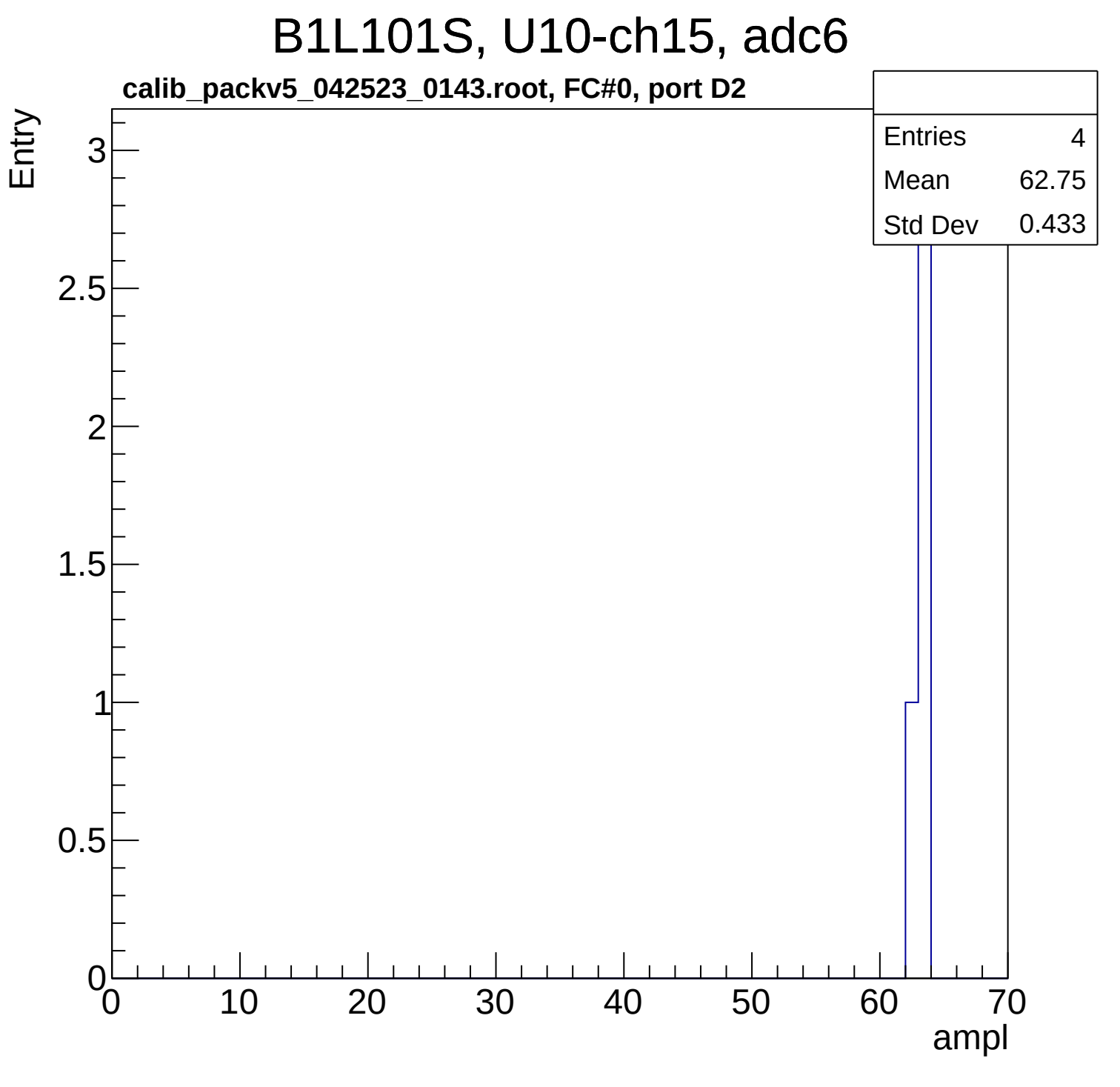
B1L101S, U10-ch15, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 62.75
Std Dev 0.433
Entry
ampl
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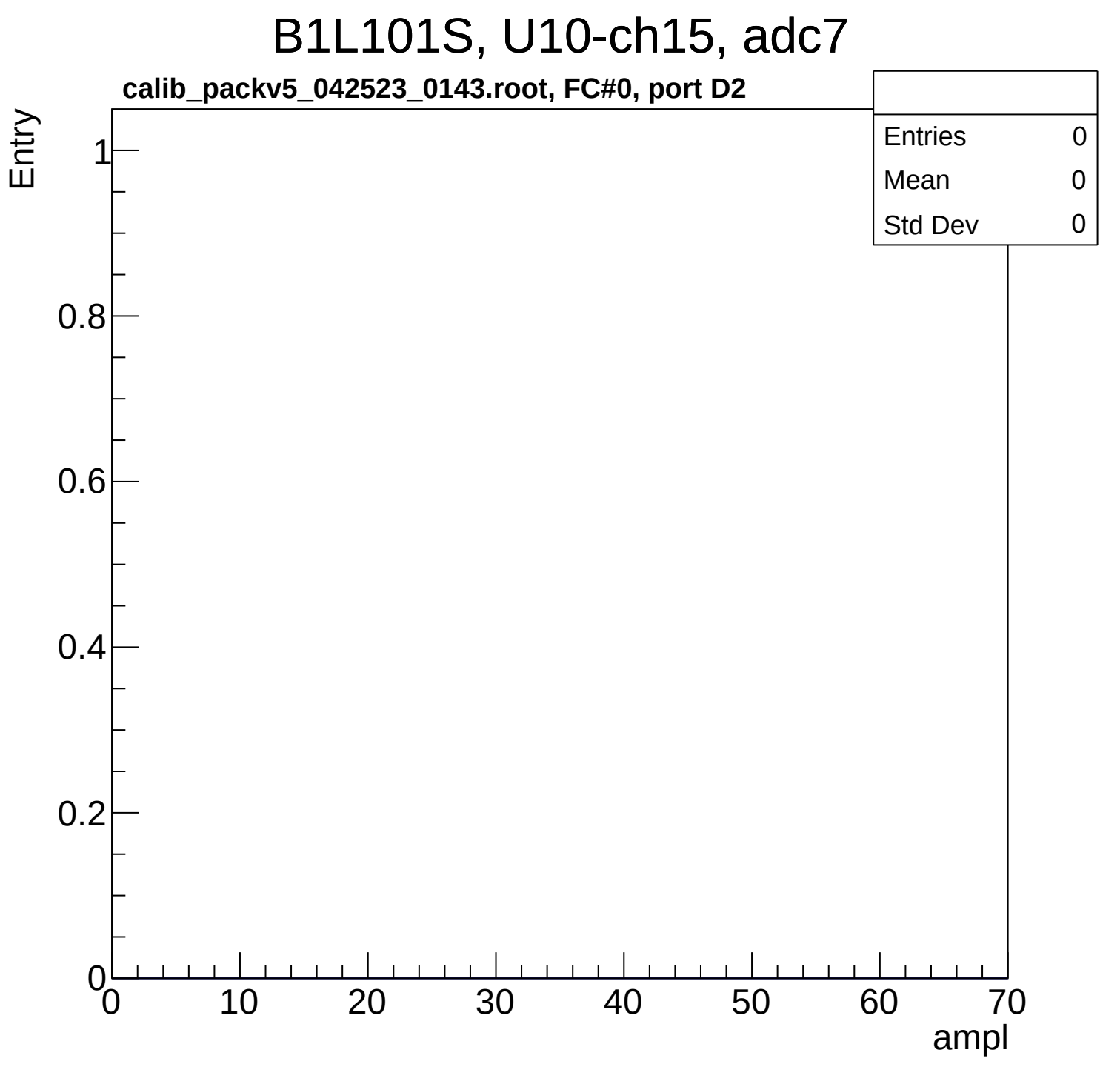
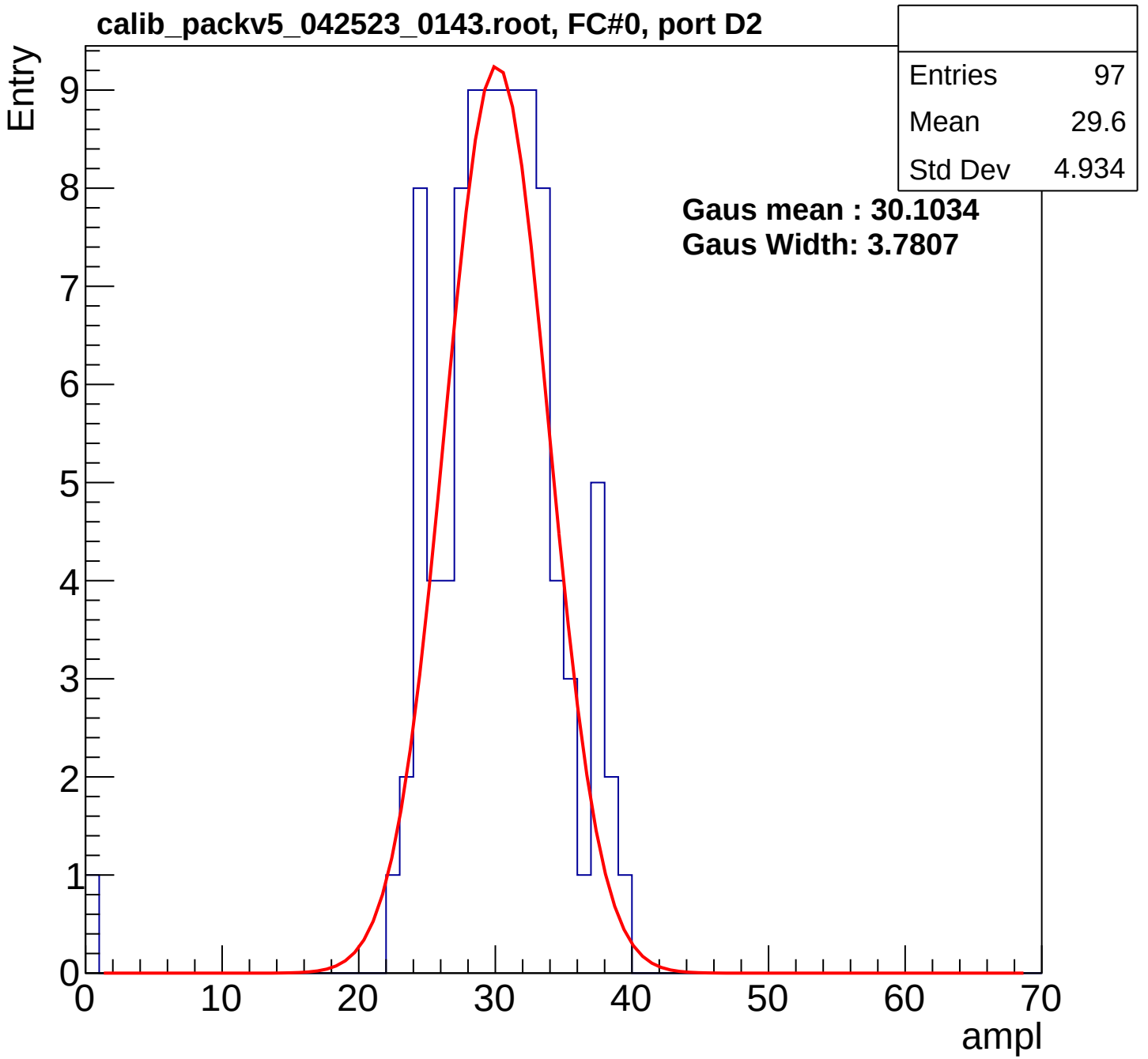
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U10-ch15, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch16, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 97
Mean 29.6
Std Dev 4.934
Gaus mean : 30.1034
Gaus Width: 3.7807
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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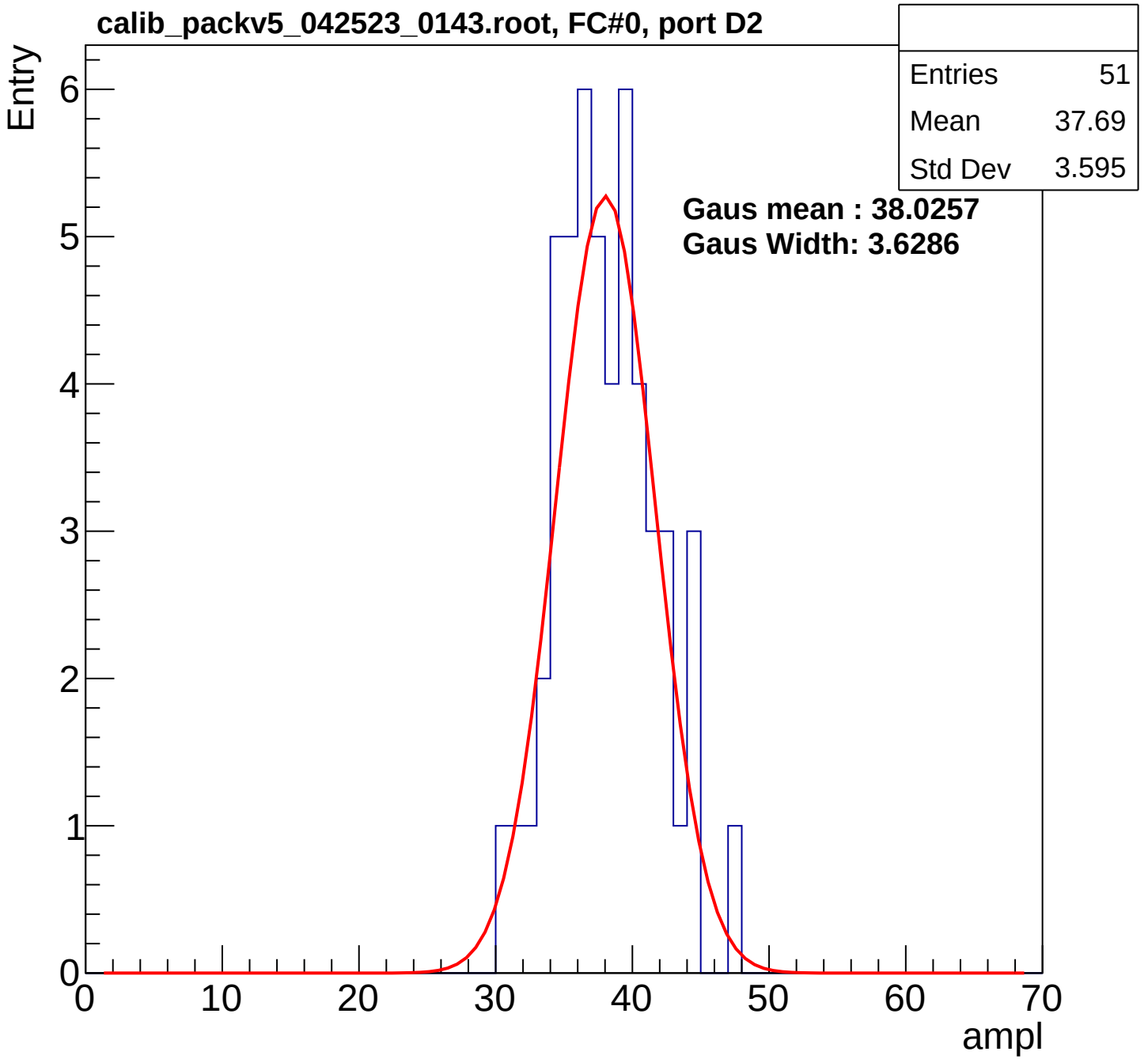
B1L101S, U10-ch16, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 37.69
Std Dev 3.595
Gaus mean : 38.0257
Gaus Width: 3.6286
Entry
ampl
0
1
2
3
4
5
6
0
10
20
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40
50
60
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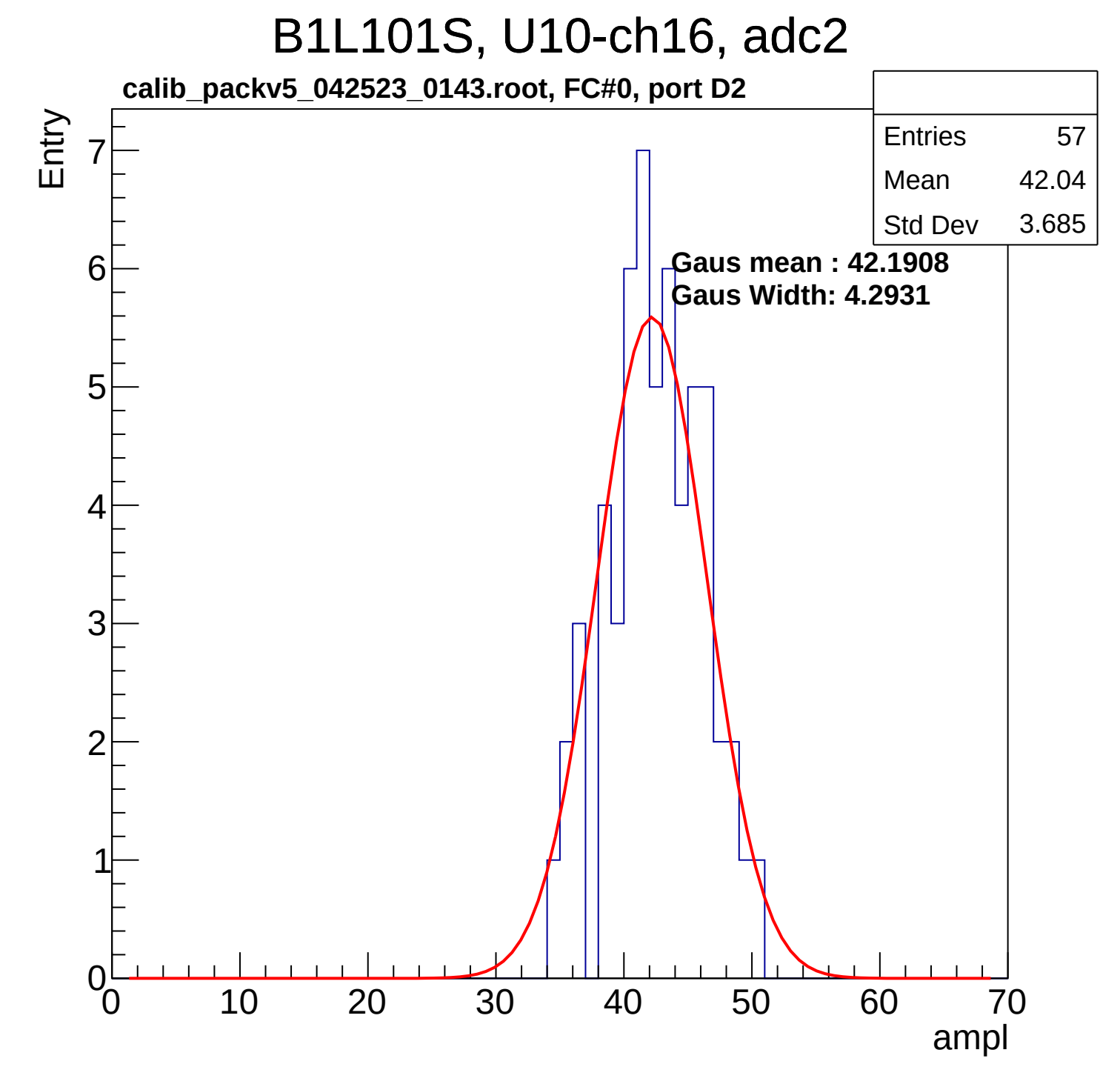
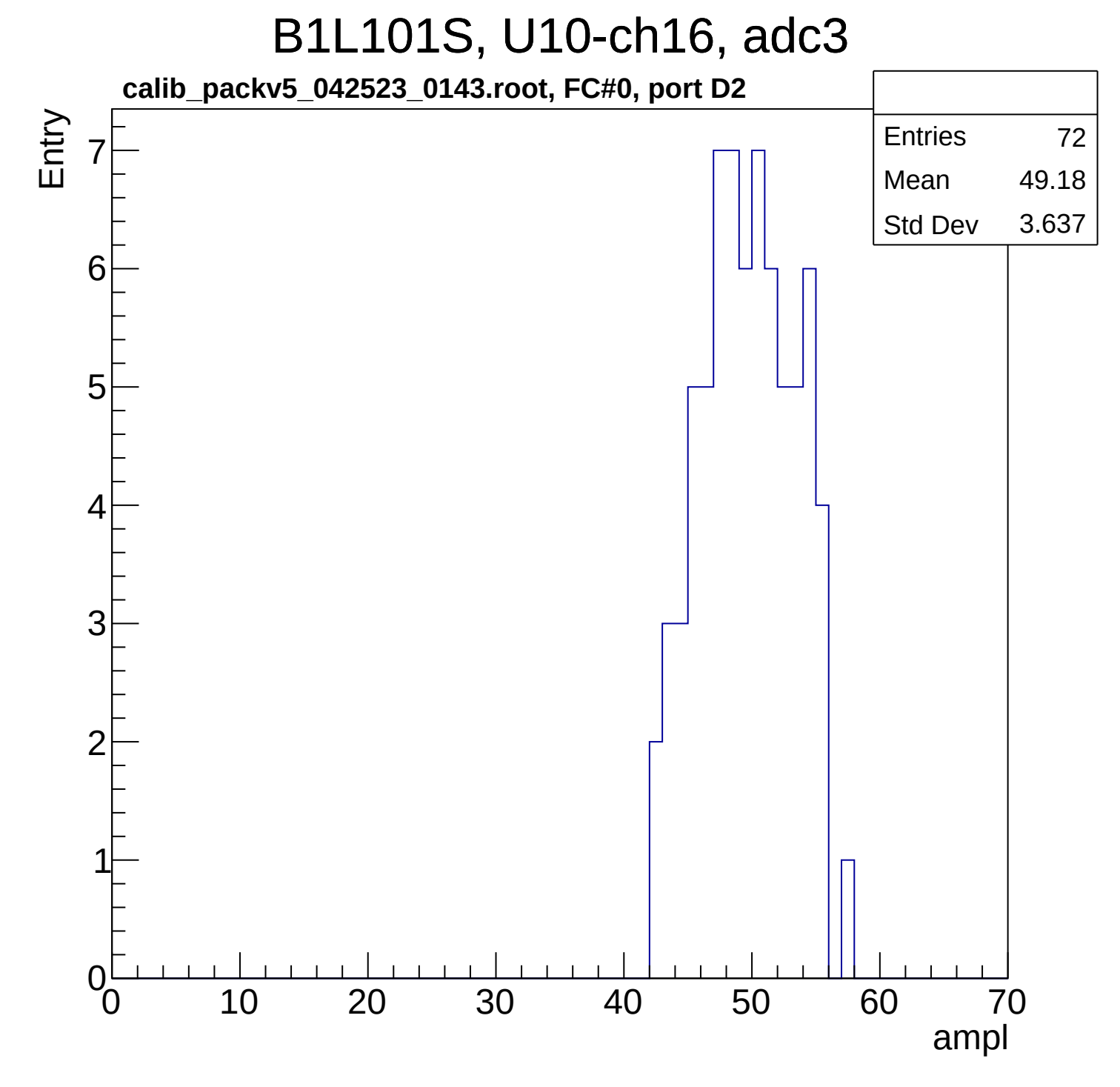
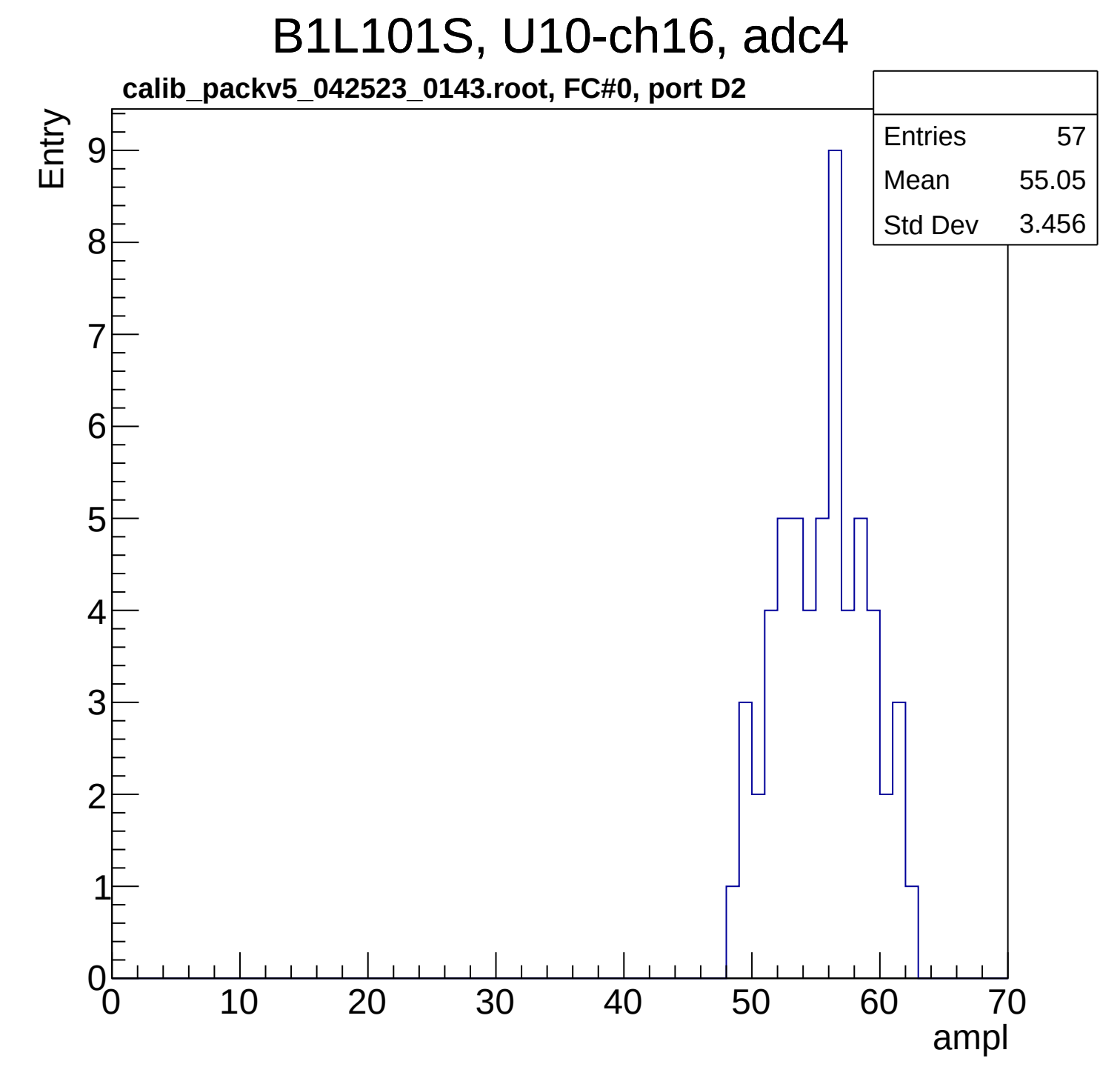

B1L101S, U10-ch16, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 42.04
Std Dev 3.685
Gaus mean : 42.1908
Gaus Width: 4.2931
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U10-ch16, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 49.18
Std Dev 3.637
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U10-ch16, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 55.05
Std Dev 3.456
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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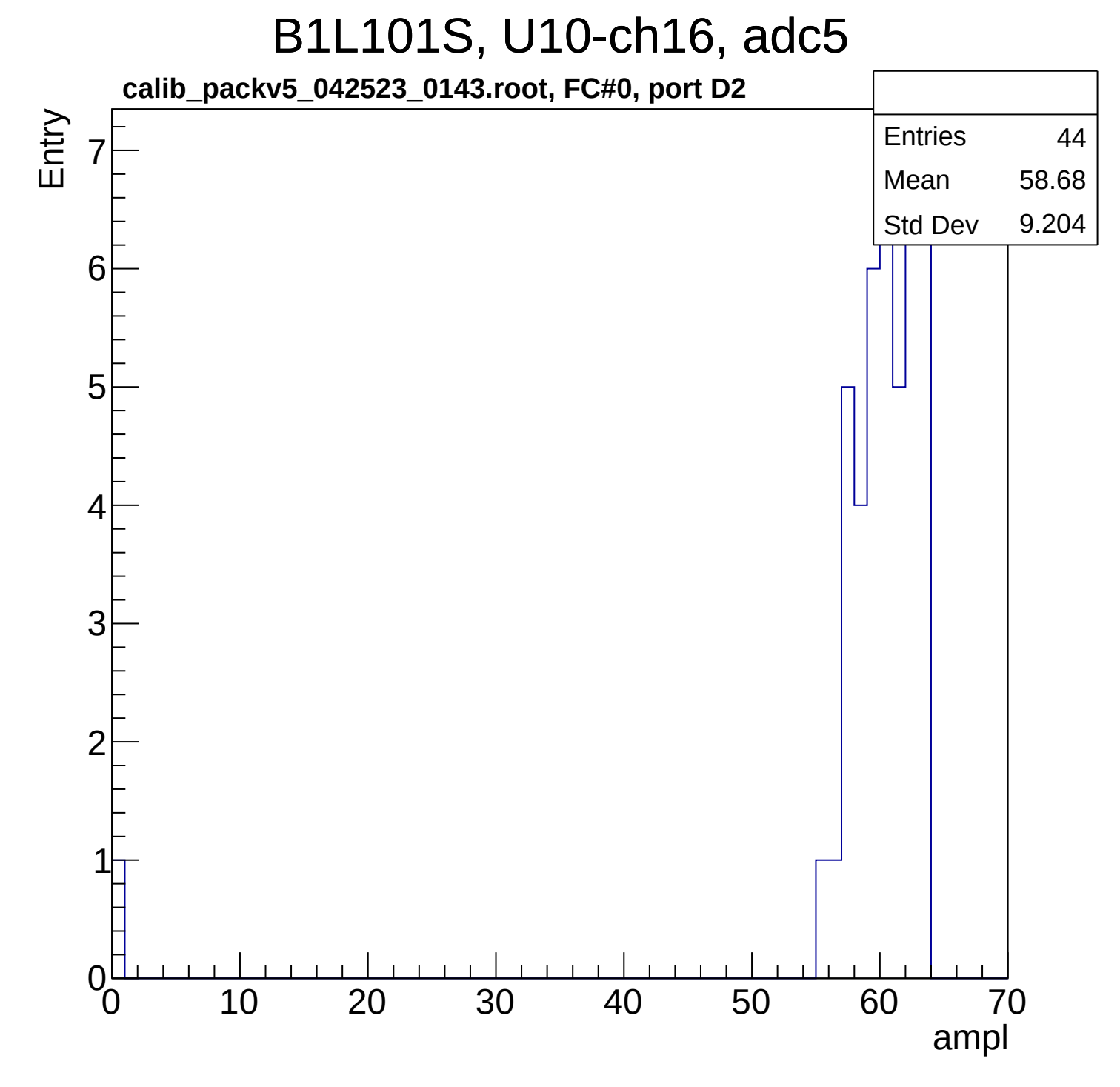
B1L101S, U10-ch16, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 44
Mean 58.68
Std Dev 9.204
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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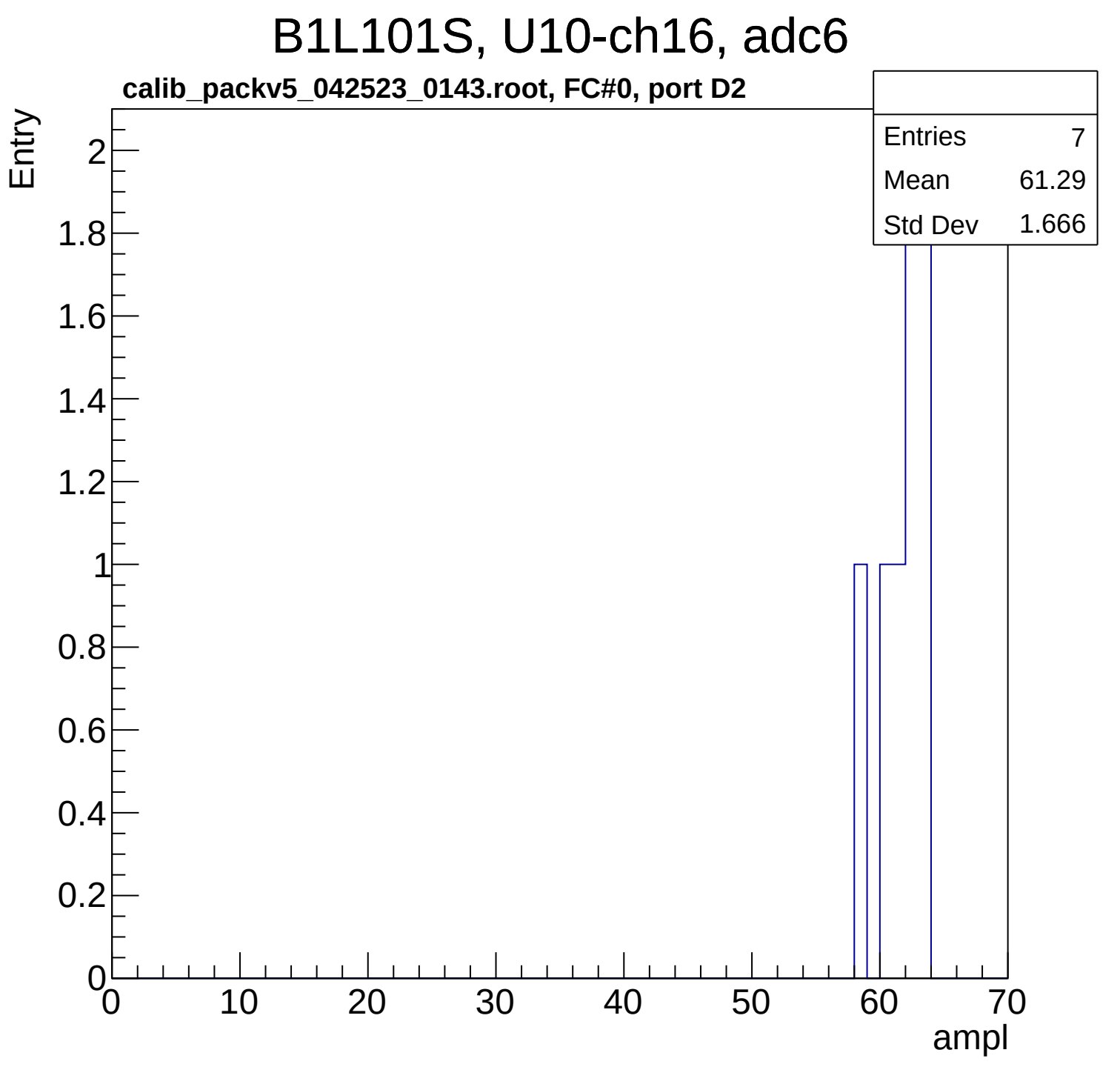
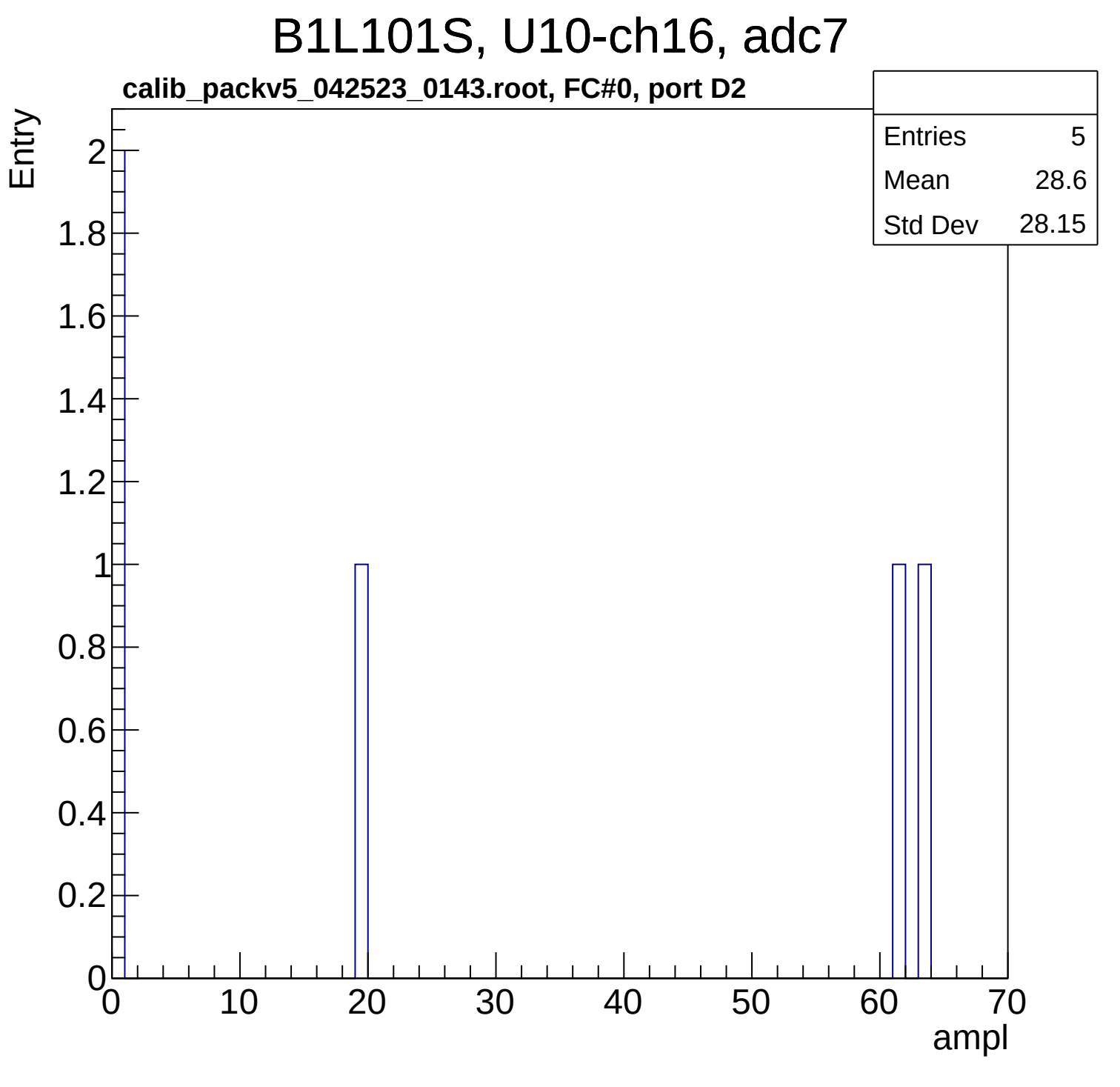

B1L101S, U10-ch16, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 61.29
Std Dev 1.666
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U10-ch16, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 28.6
Std Dev 28.15
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
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60
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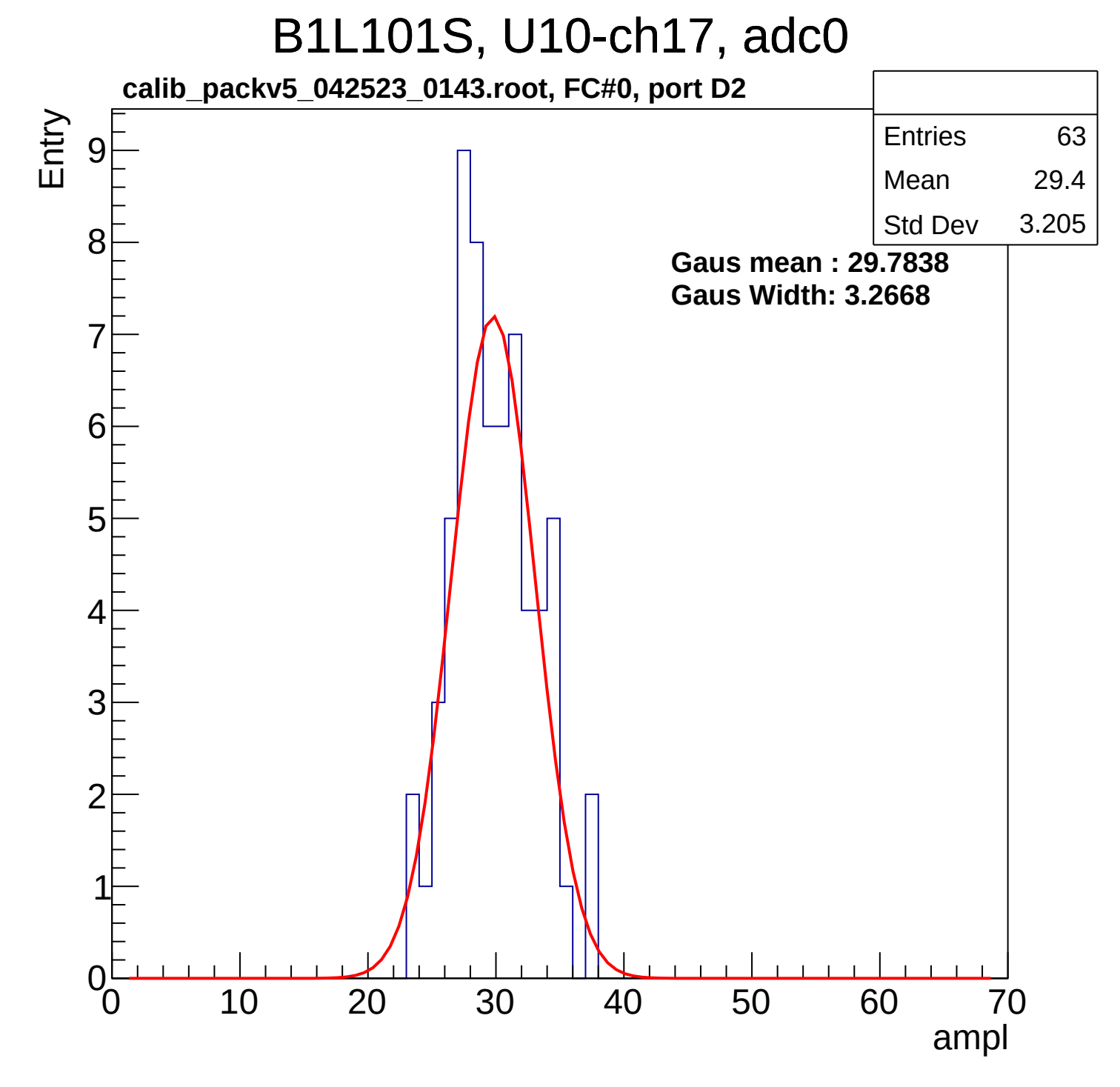
B1L101S, U10-ch17, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 29.4
Std Dev 3.205
Gaus mean : 29.7838
Gaus Width: 3.2668
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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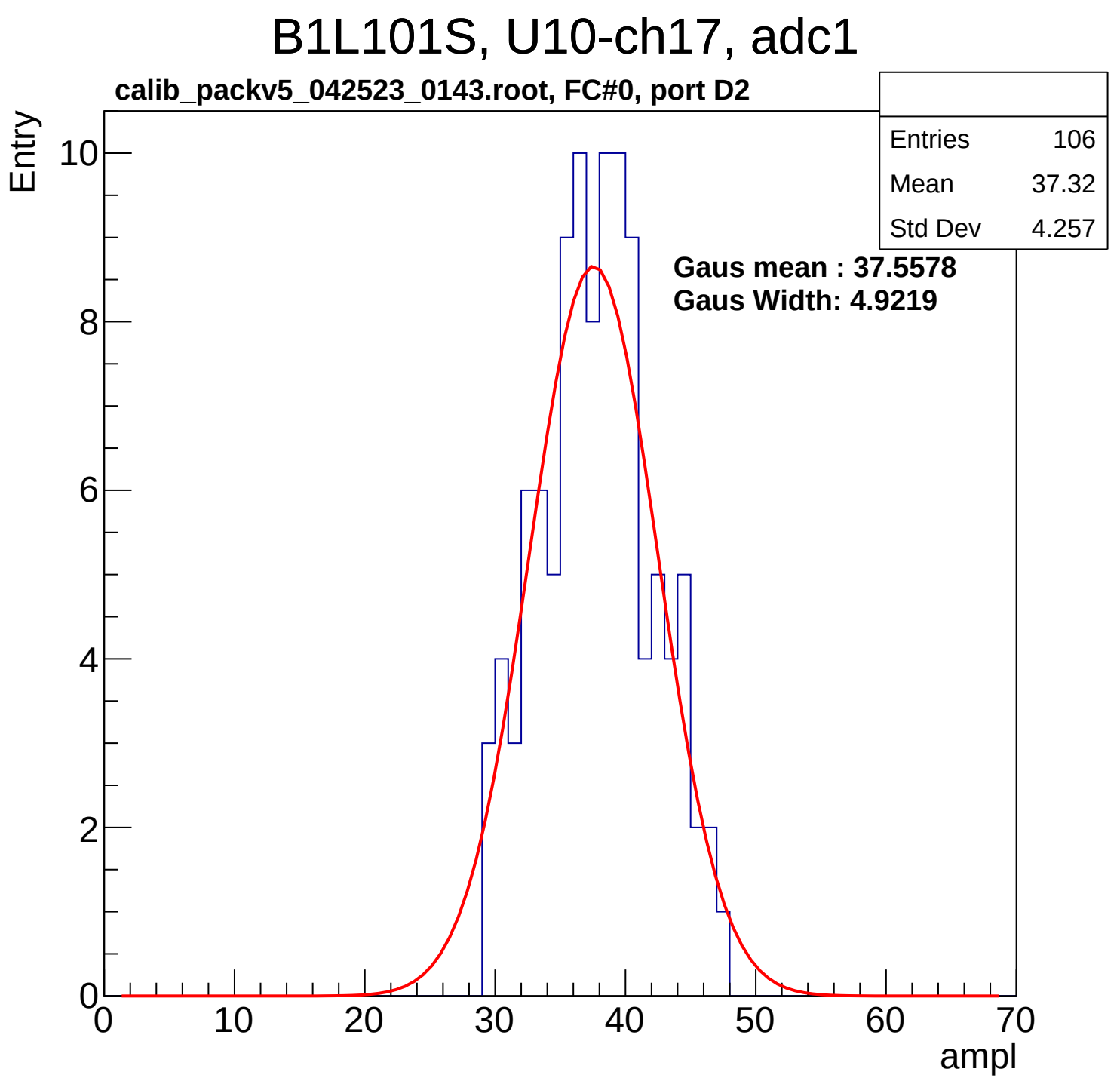
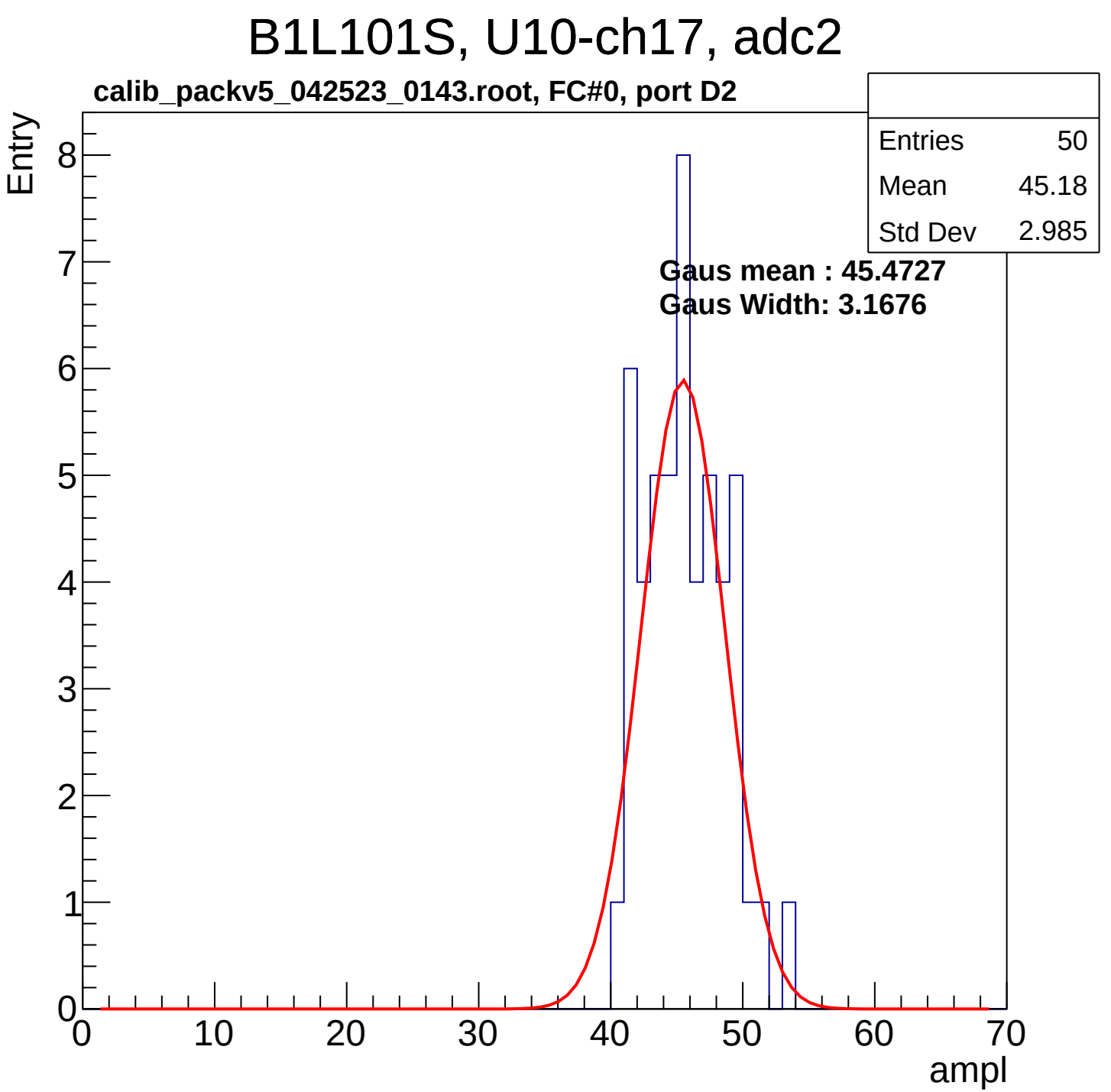

B1L101S, U10-ch17, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 106
Mean 37.32
Std Dev 4.257
Gaus mean : 37.5578
Gaus Width: 4.9219
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch17, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 45.18
Std Dev 2.985
Gaus mean : 45.4727
Gaus Width: 3.1676
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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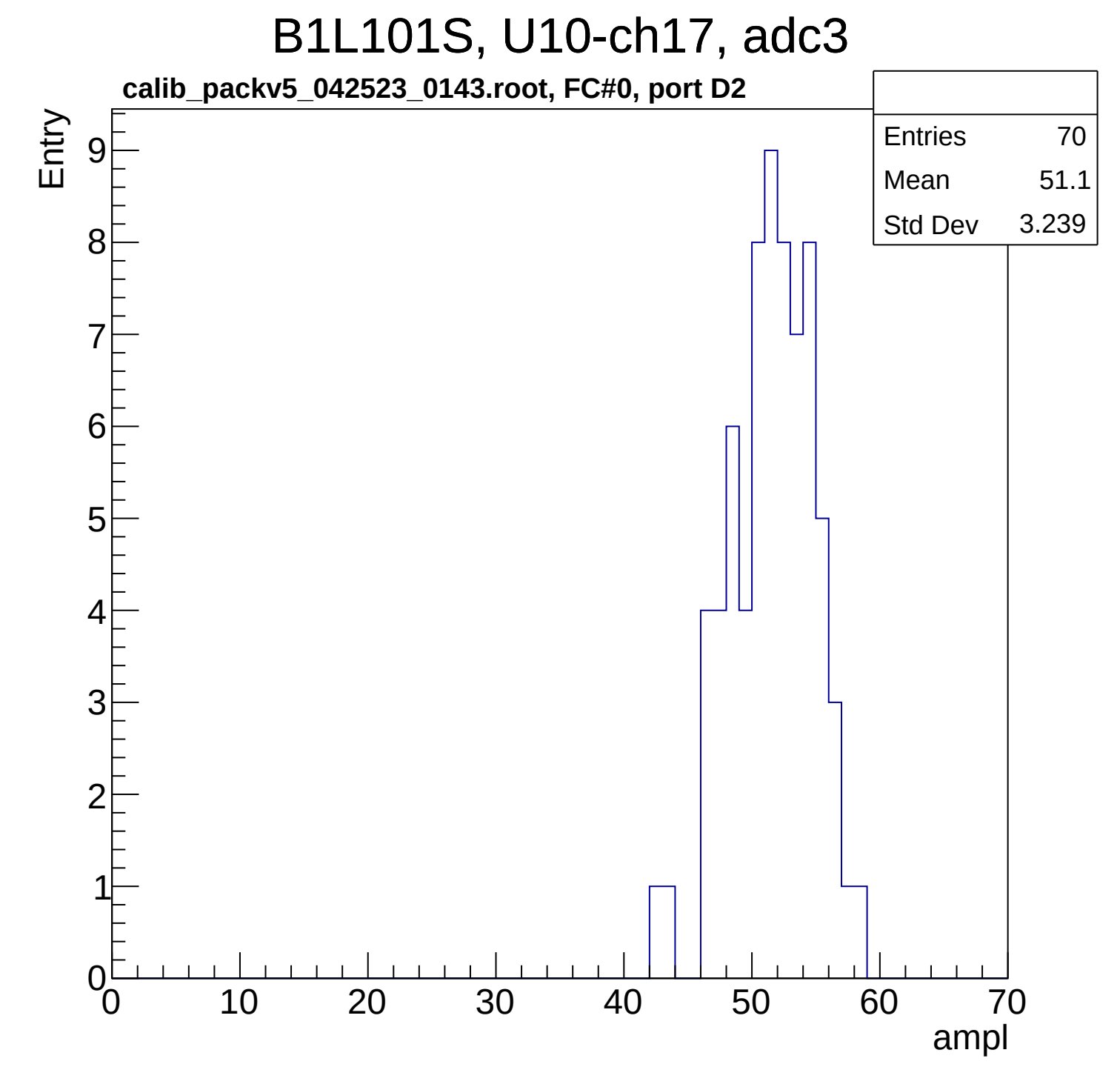
B1L101S, U10-ch17, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 51.1
Std Dev 3.239
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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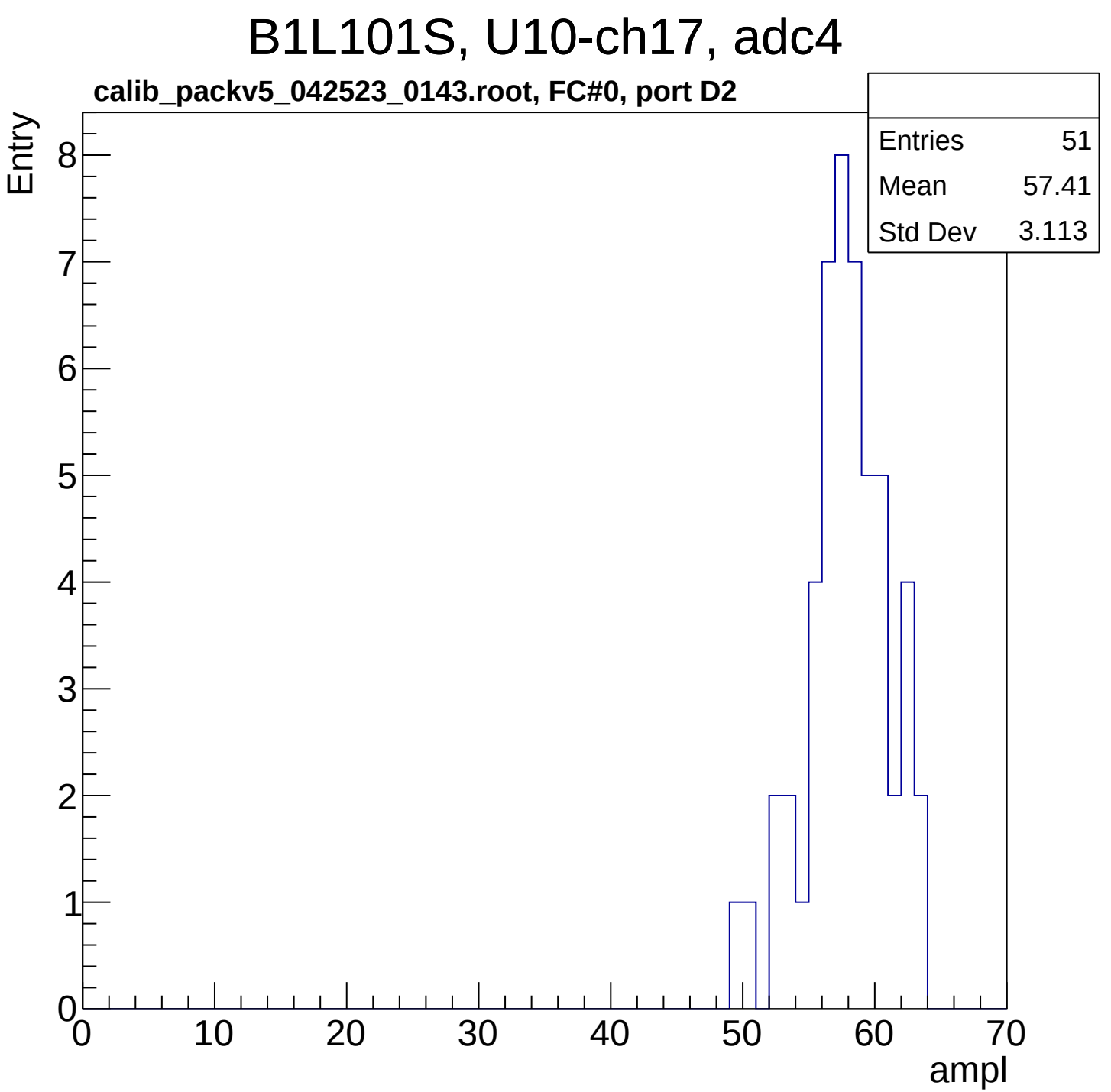
B1L101S, U10-ch17, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 57.41
Std Dev 3.113
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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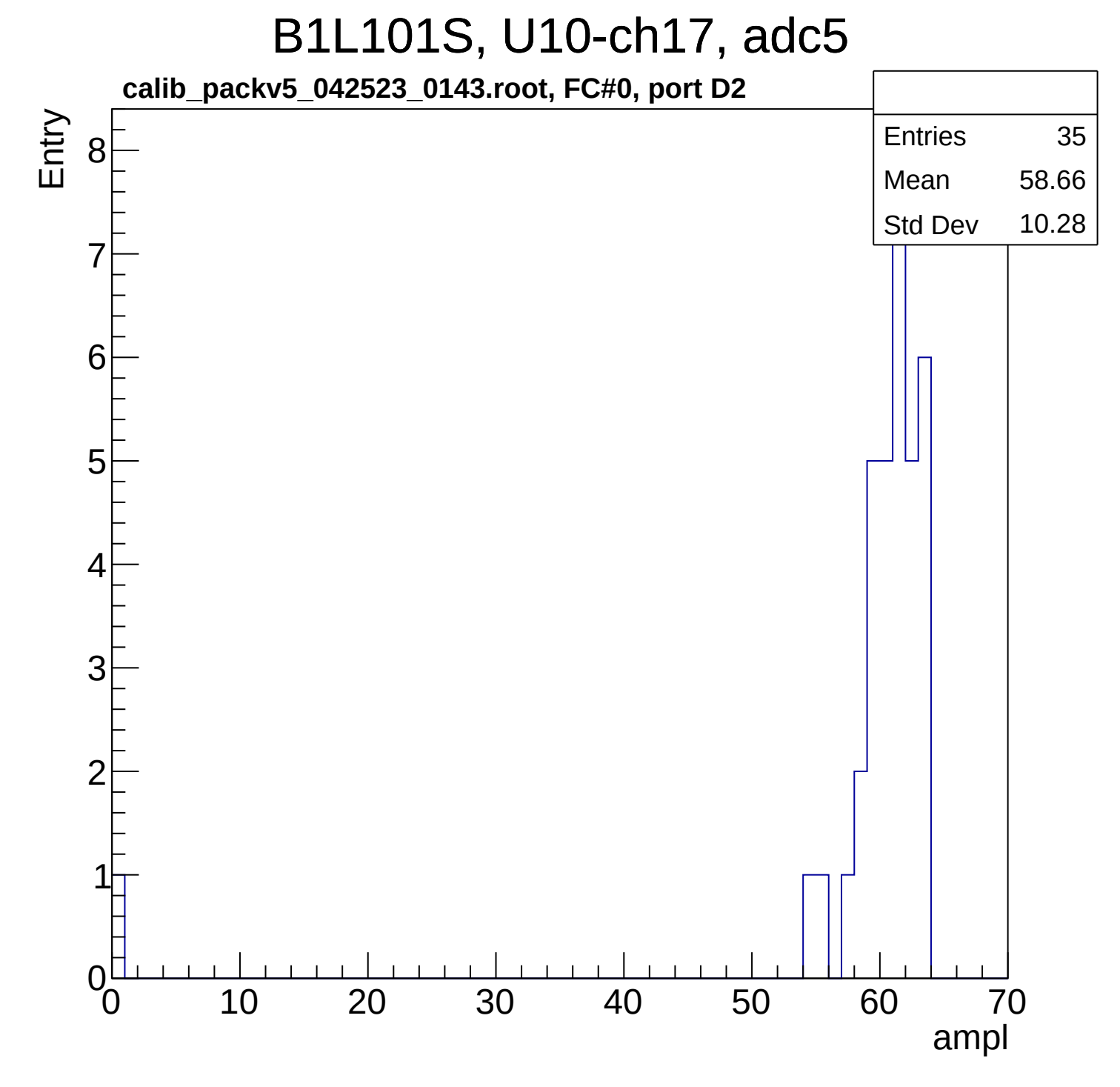
B1L101S, U10-ch17, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 35
Mean 58.66
Std Dev 10.28
Entry
ampl
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2
3
4
5
6
7
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0
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20
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40
50
60
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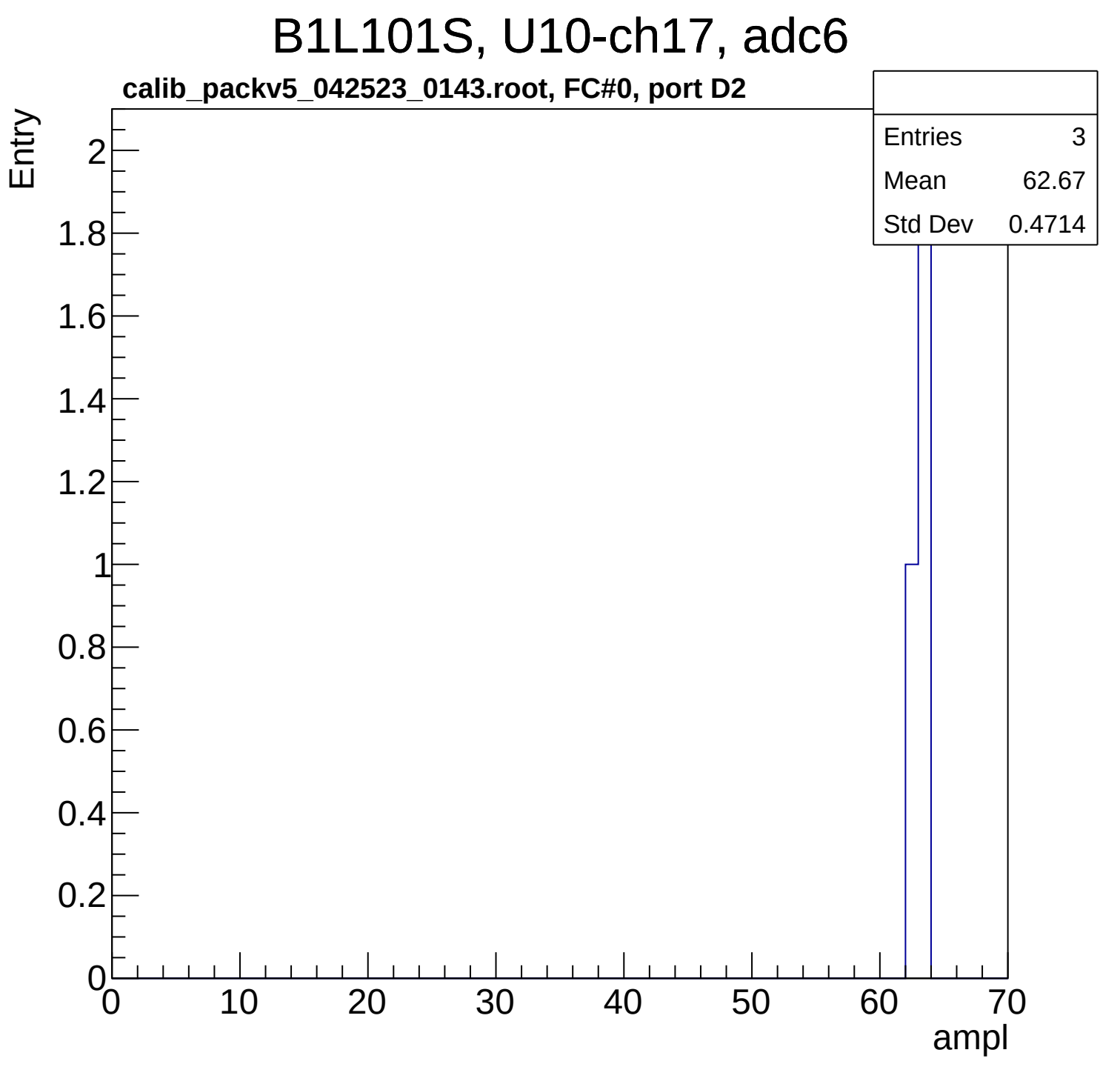
B1L101S, U10-ch17, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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60
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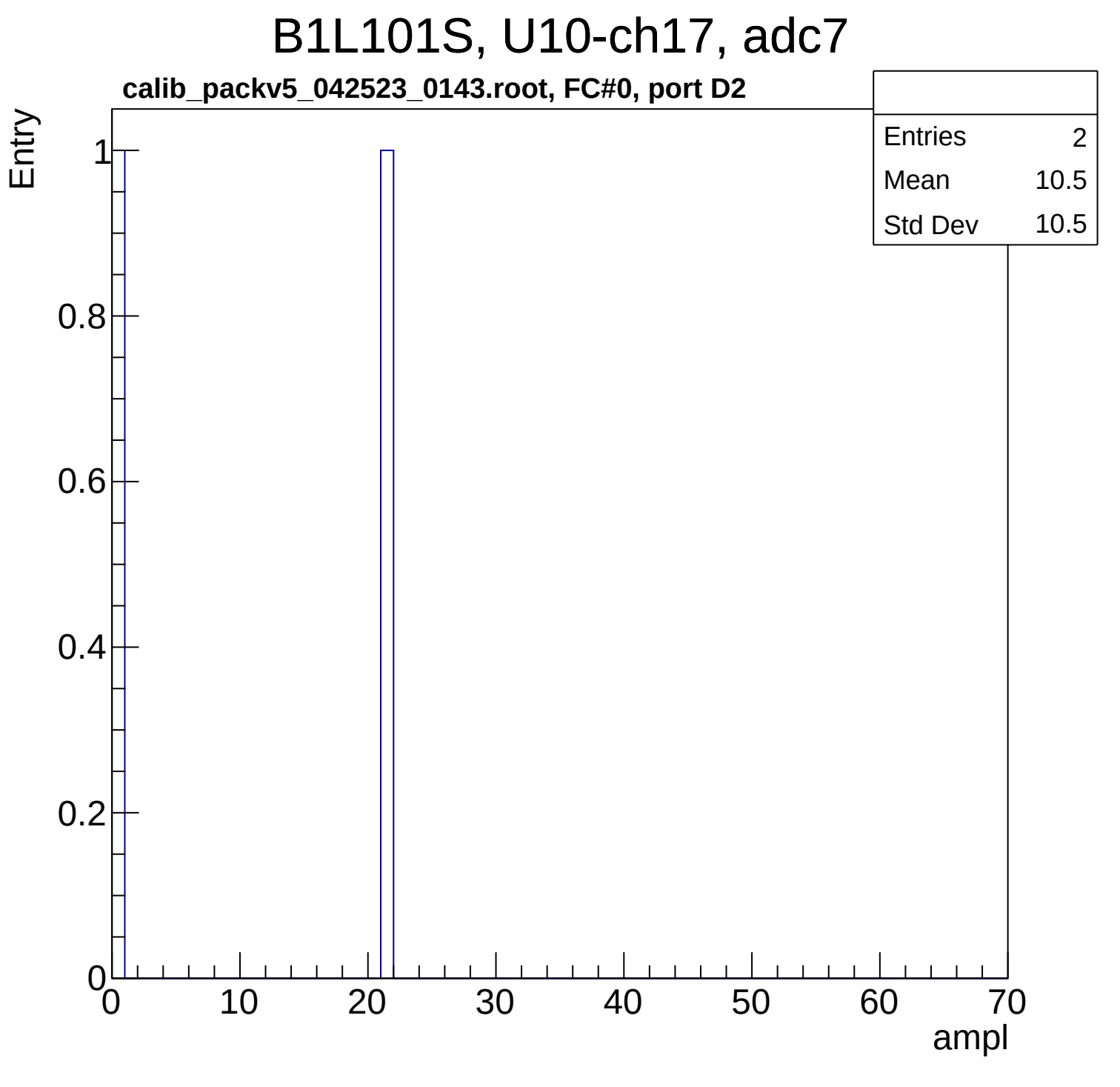
B1L101S, U10-ch17, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 10.5
Std Dev 10.5
Entry
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0.6
0.4
0.2
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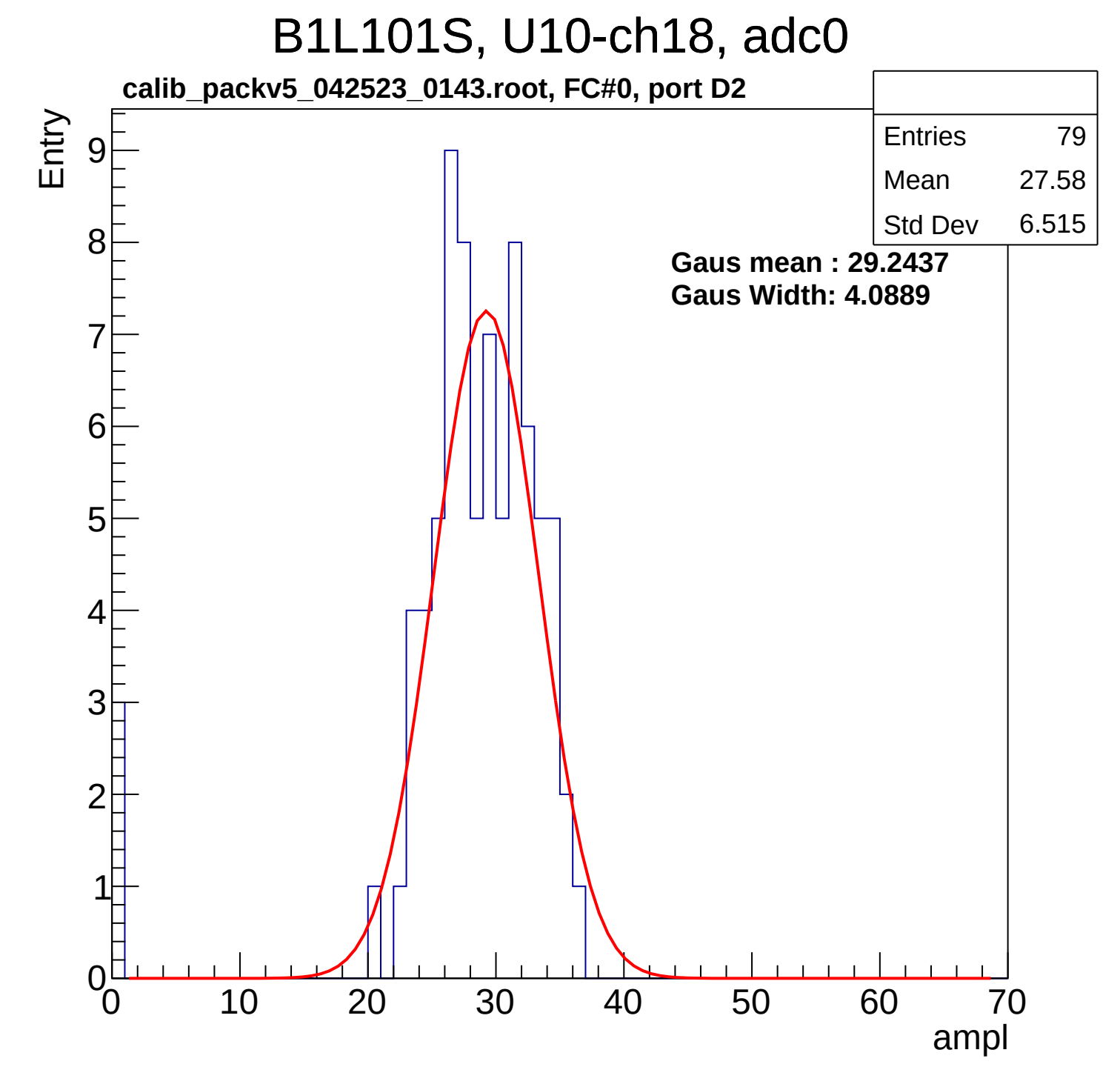
70
ampl


B1L101S, U10-ch18, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 27.58
Std Dev 6.515
Gaus mean : 29.2437
Gaus Width: 4.0889
Entry
ampl
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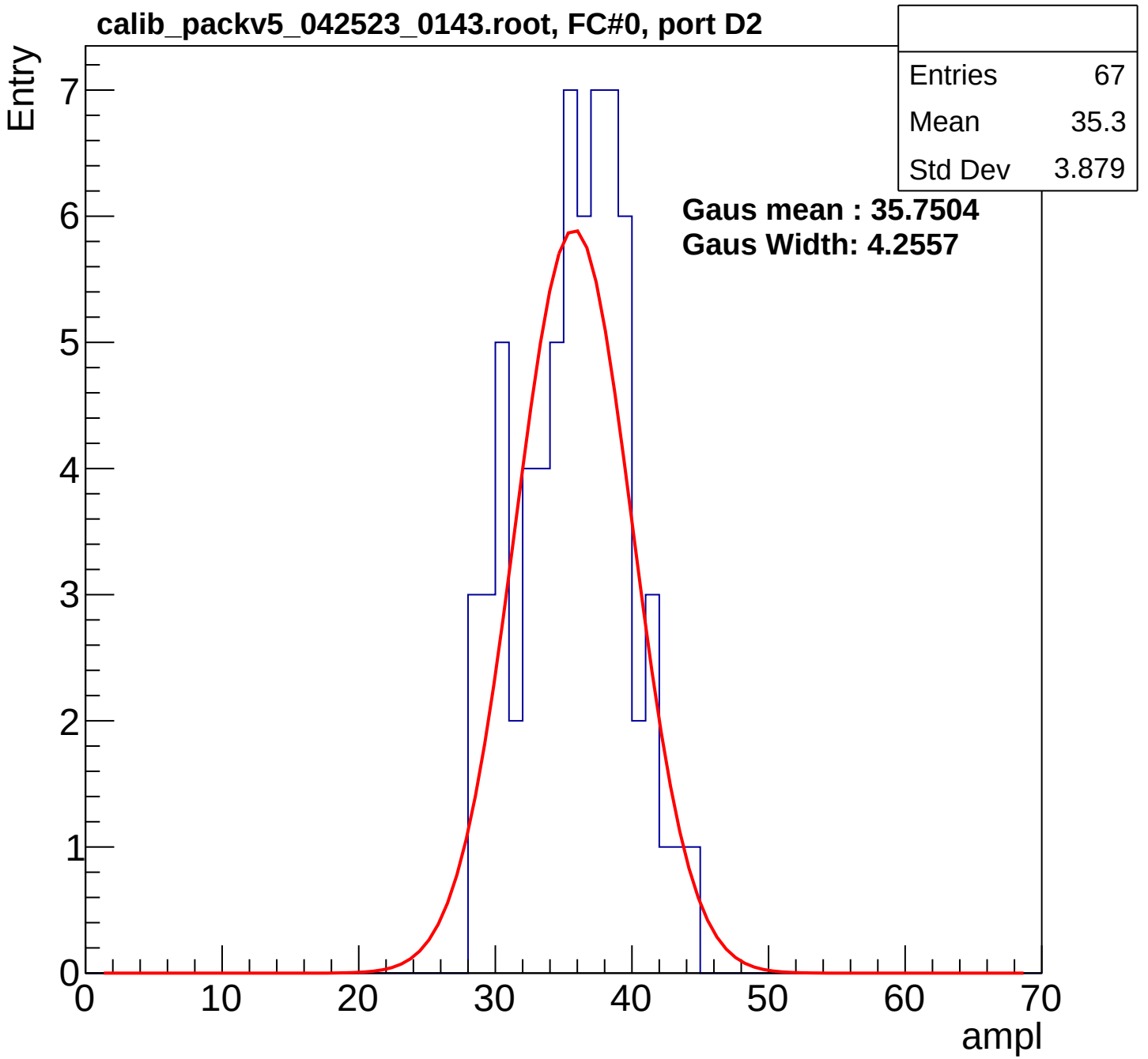
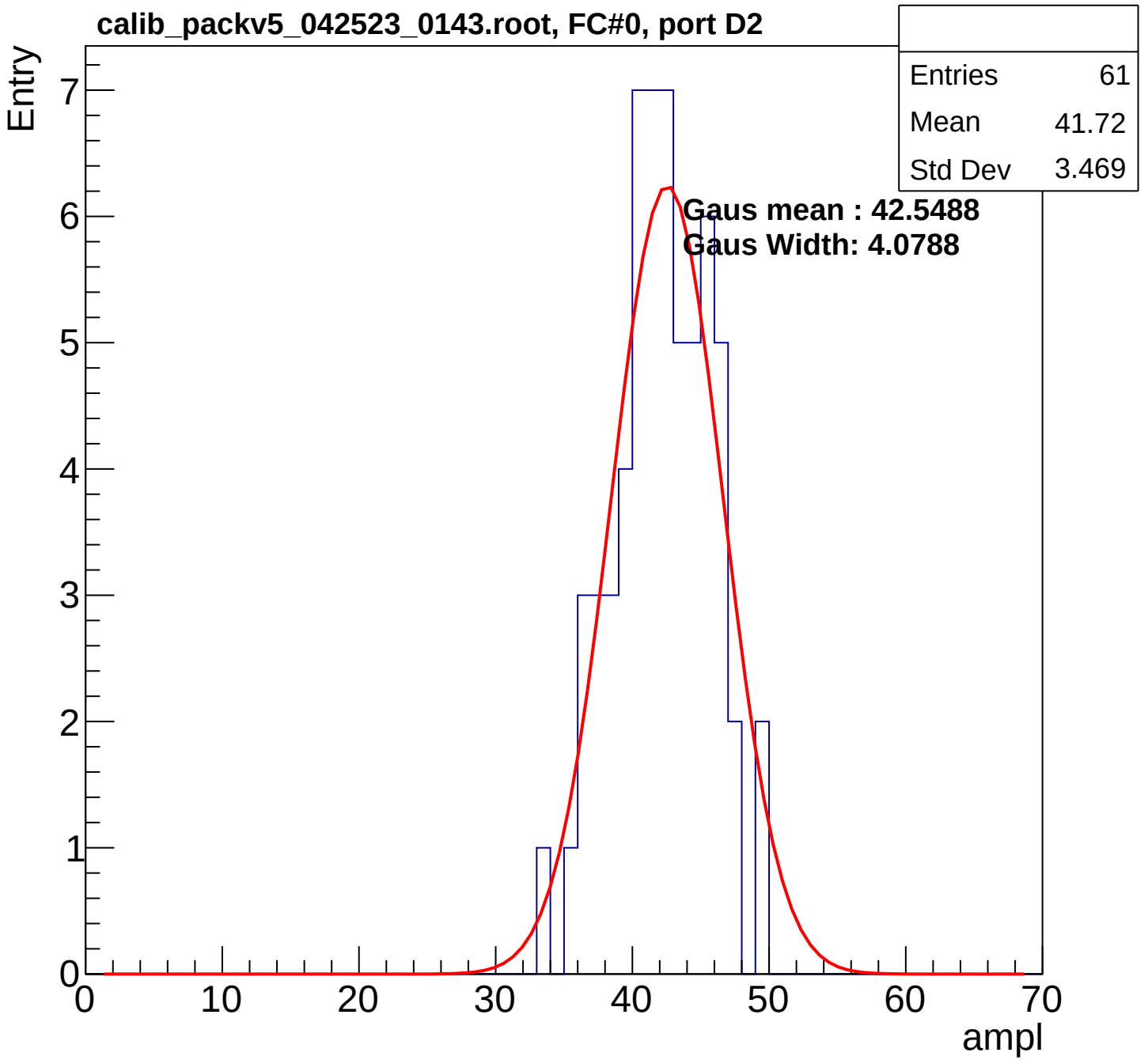
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch18, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 35.3
Std Dev 3.879
Gaus mean : 35.7504
Gaus Width: 4.2557
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U10-ch18, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 41.72
Std Dev 3.469
Gaus mean : 42.5488
Gaus Width: 4.0788
Entry
ampl
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1
2
3
4
5
6
7
0
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40
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60
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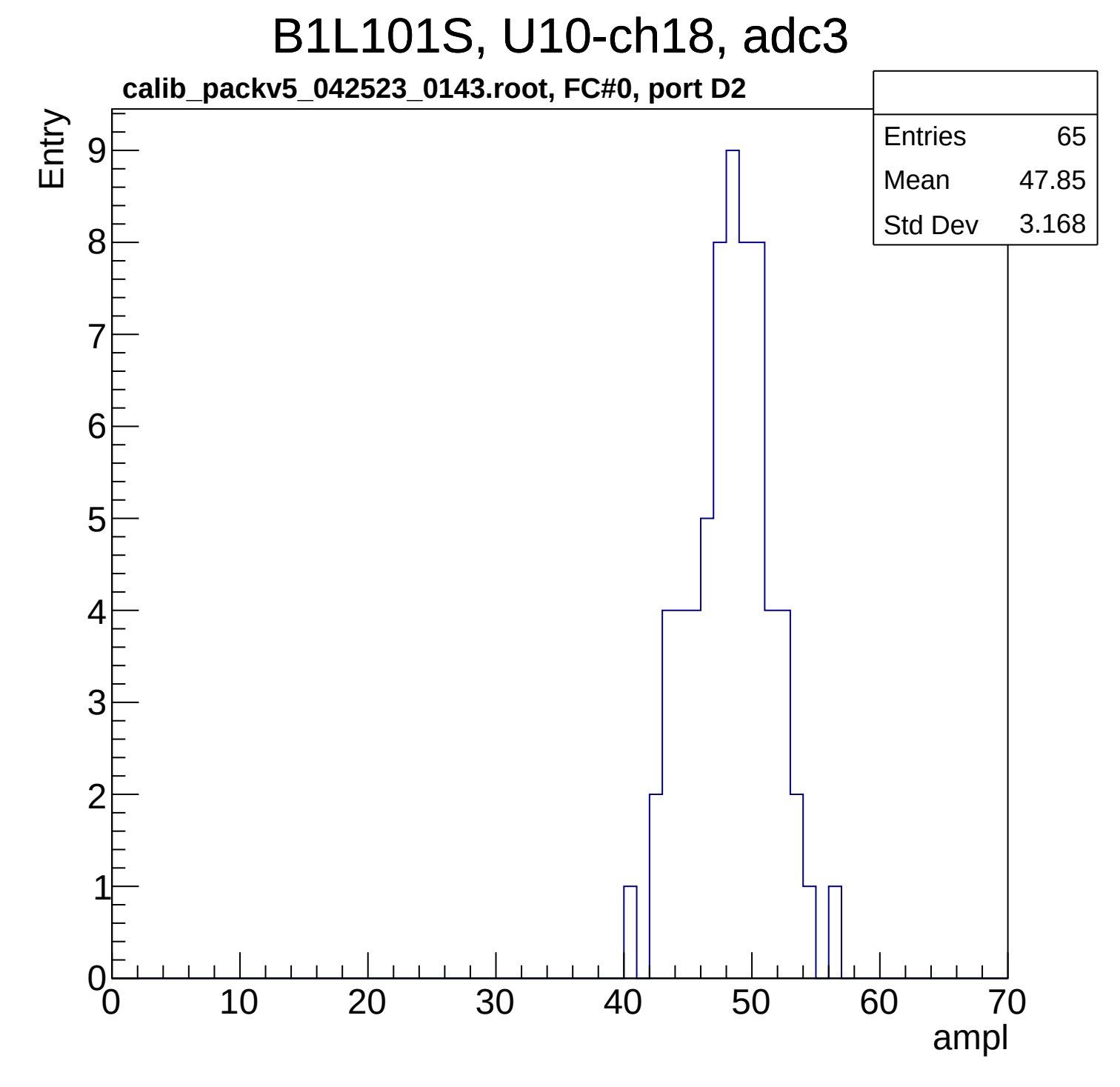
B1L101S, U10-ch18, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 47.85
Std Dev 3.168
Entry
ampl
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2
3
4
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6
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0
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60
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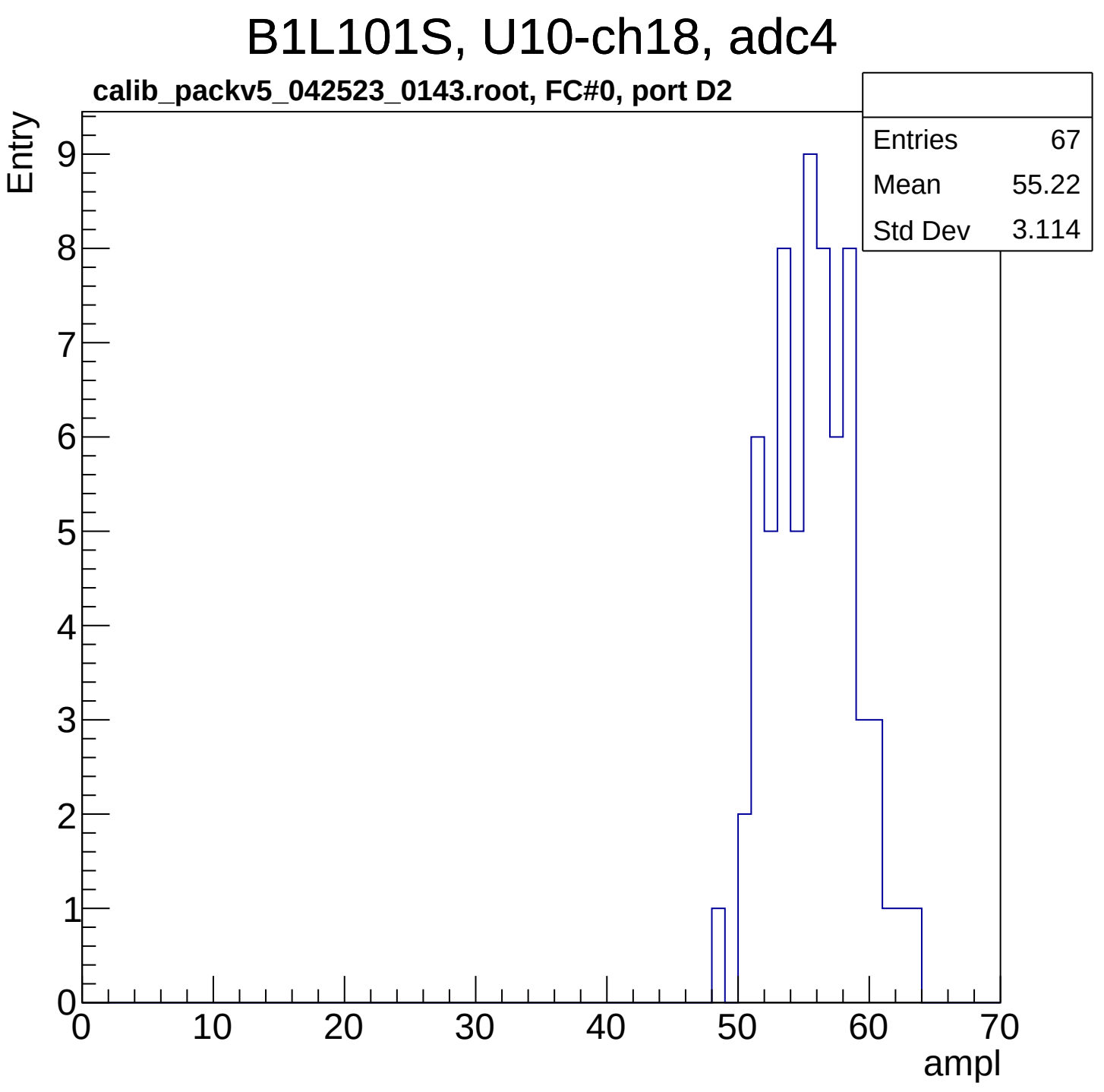
B1L101S, U10-ch18, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 55.22
Std Dev 3.114
Entry
ampl
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4
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8
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0
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60
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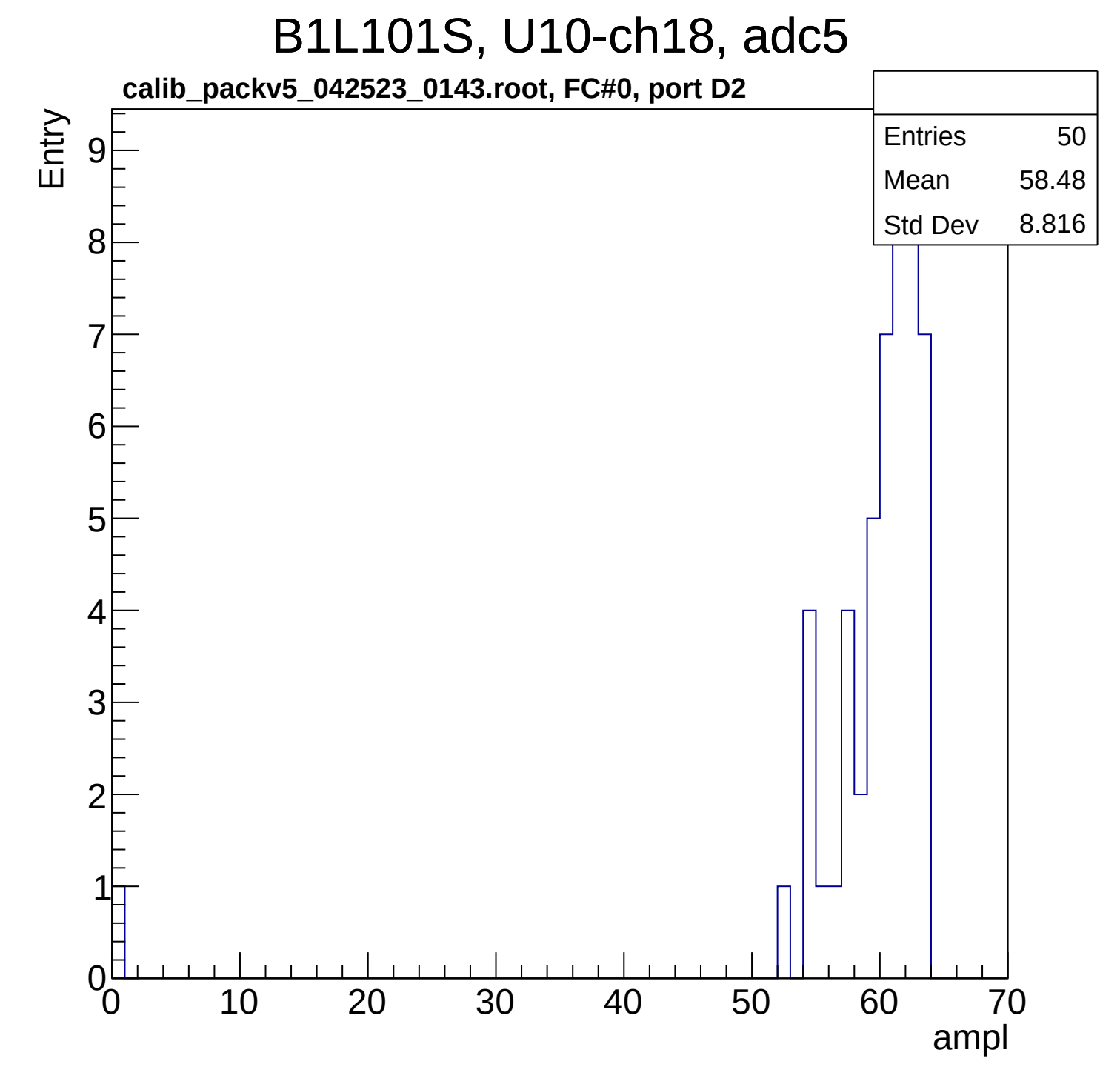
B1L101S, U10-ch18, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 58.48
Std Dev 8.816
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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60
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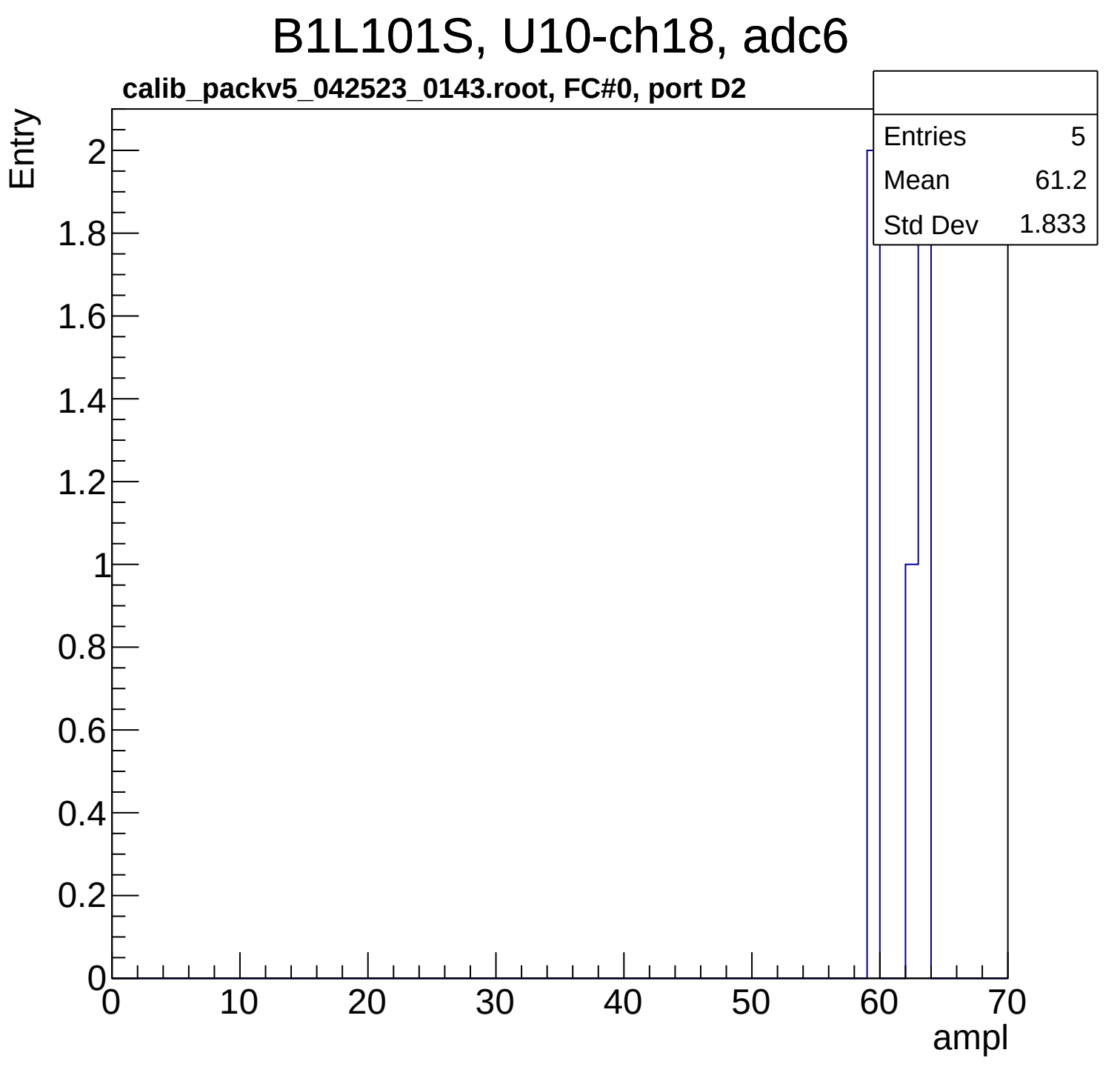
B1L101S, U10-ch18, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 61.2
Std Dev 1.833
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
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60
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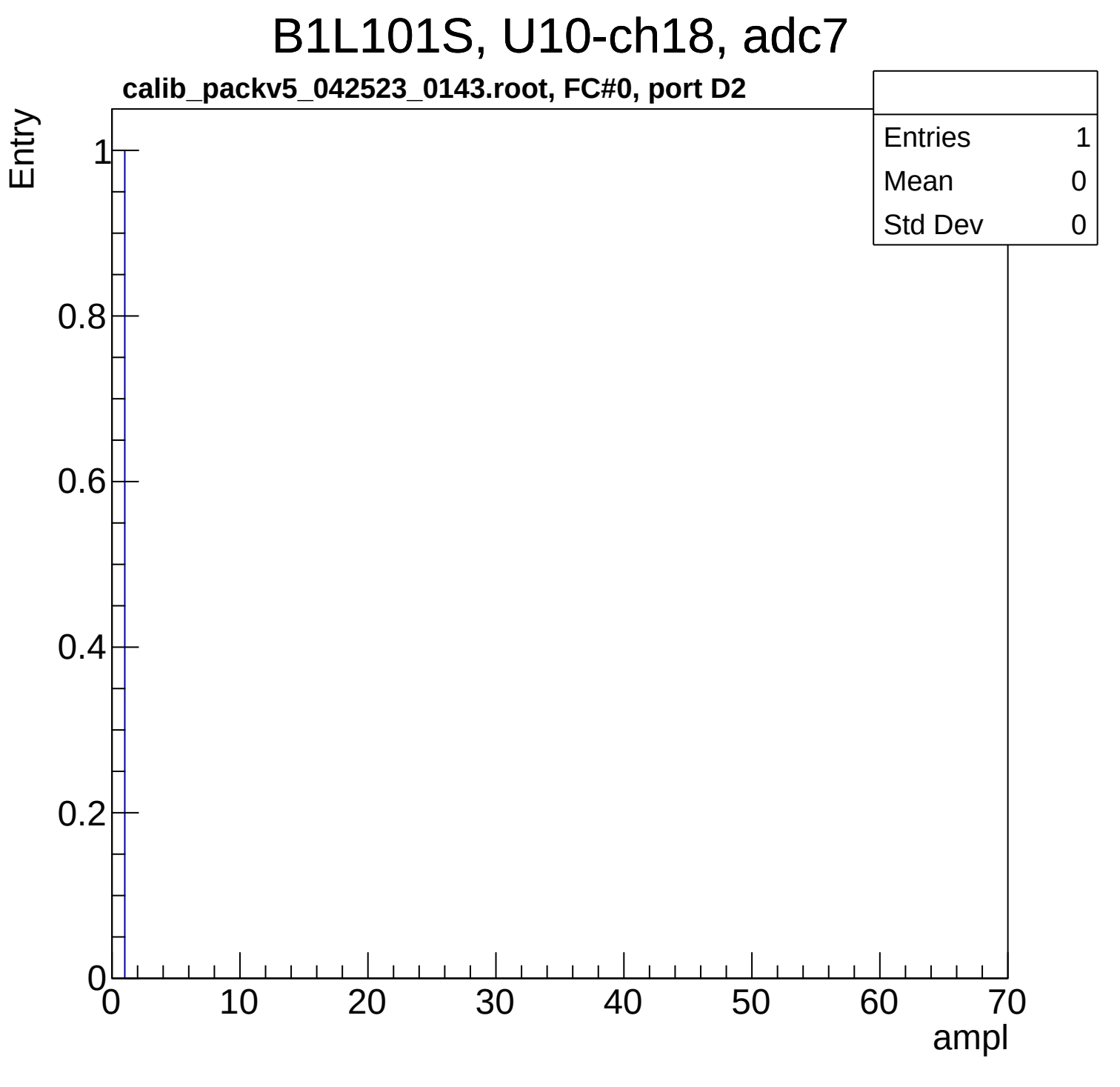
B1L101S, U10-ch18, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
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0.6
0.4
0.2
0
0
10
20
30
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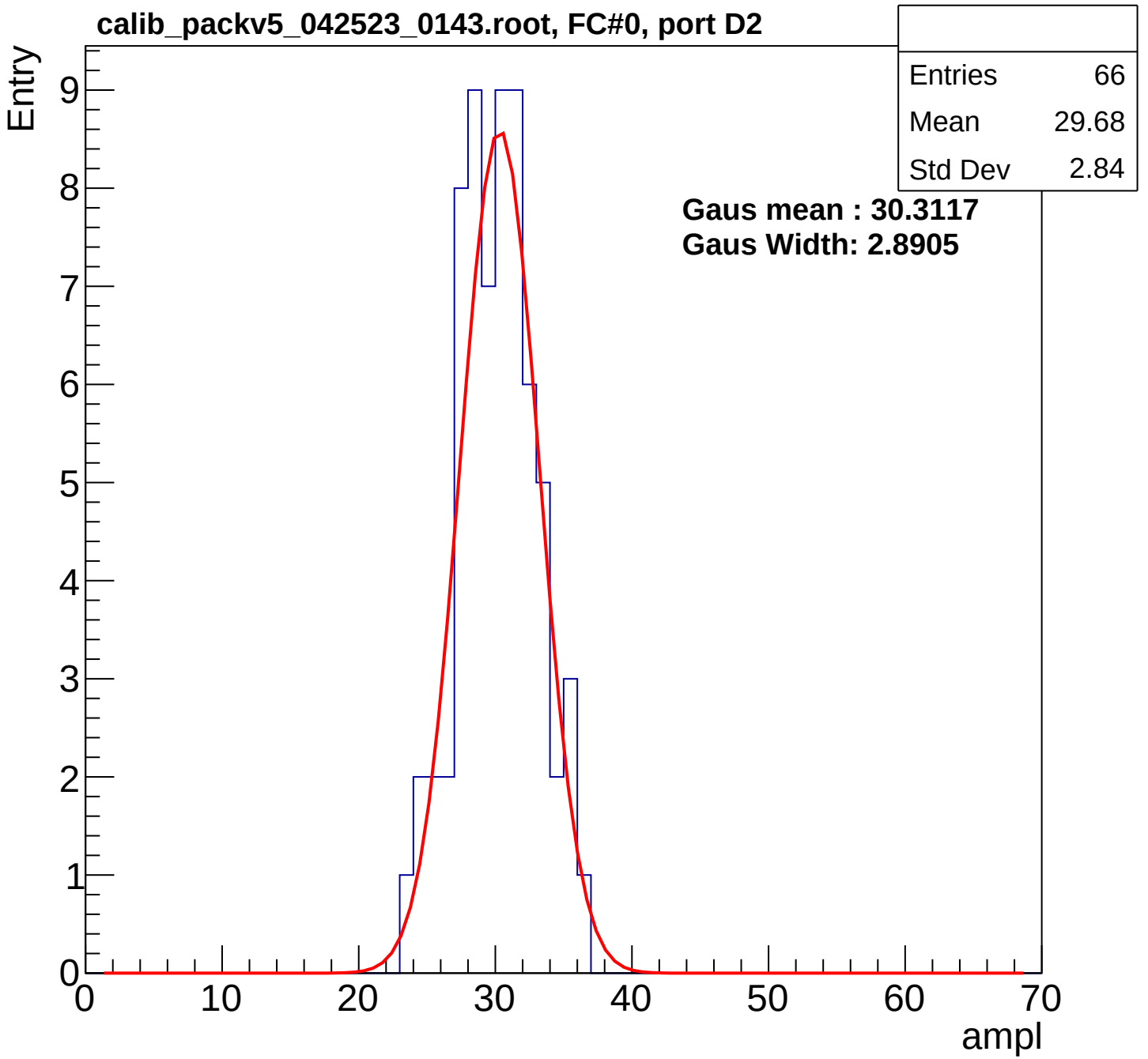
50
60
70
ampl


B1L101S, U10-ch19, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 29.68
Std Dev 2.84
Gaus mean : 30.3117
Gaus Width: 2.8905
Entry
ampl
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2
3
4
5
6
7
8
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0
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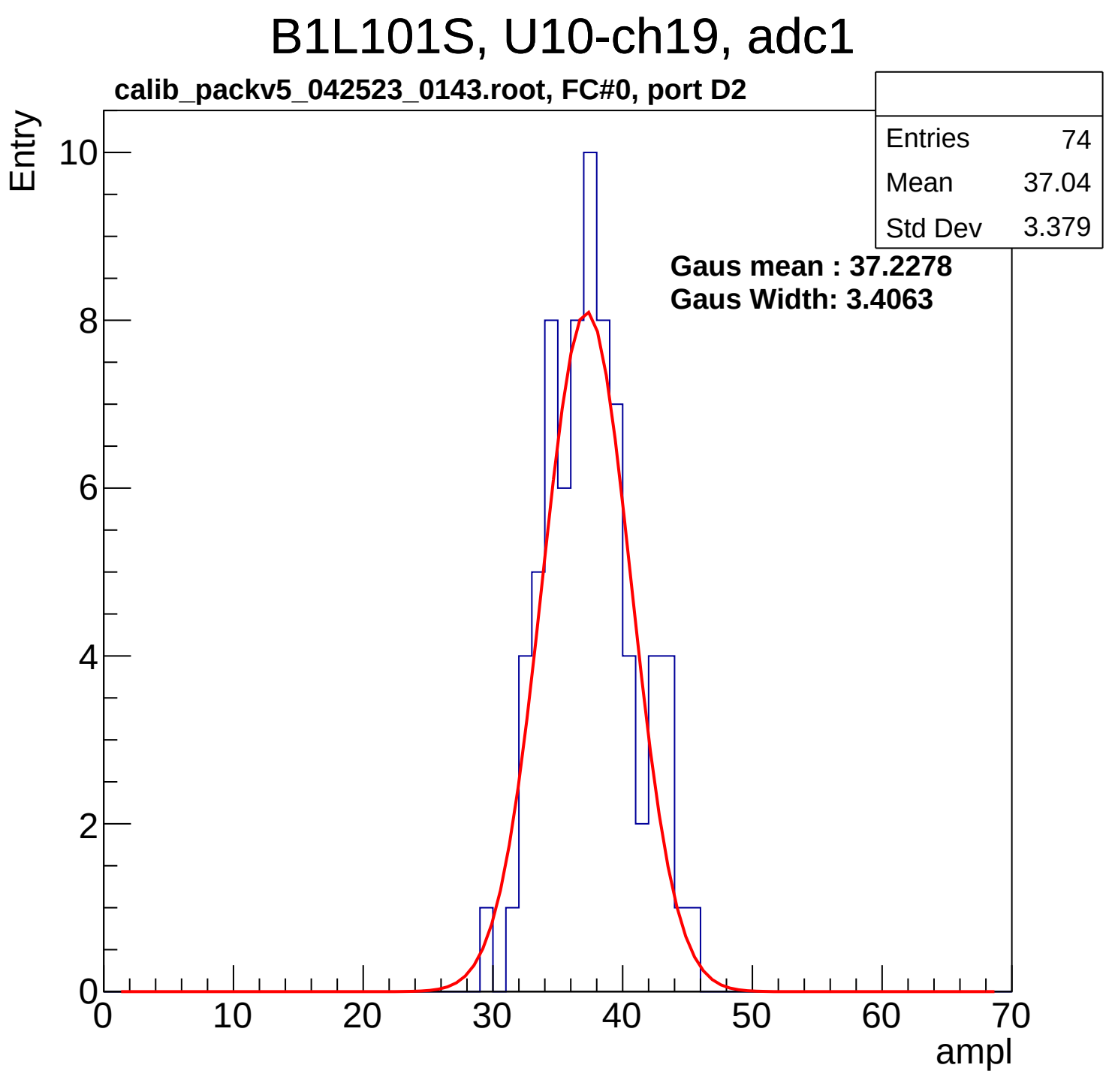
B1L101S, U10-ch19, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 37.04
Std Dev 3.379
Gaus mean : 37.2278
Gaus Width: 3.4063
Entry
ampl
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4
6
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10
0
10
20
30
40
50
60
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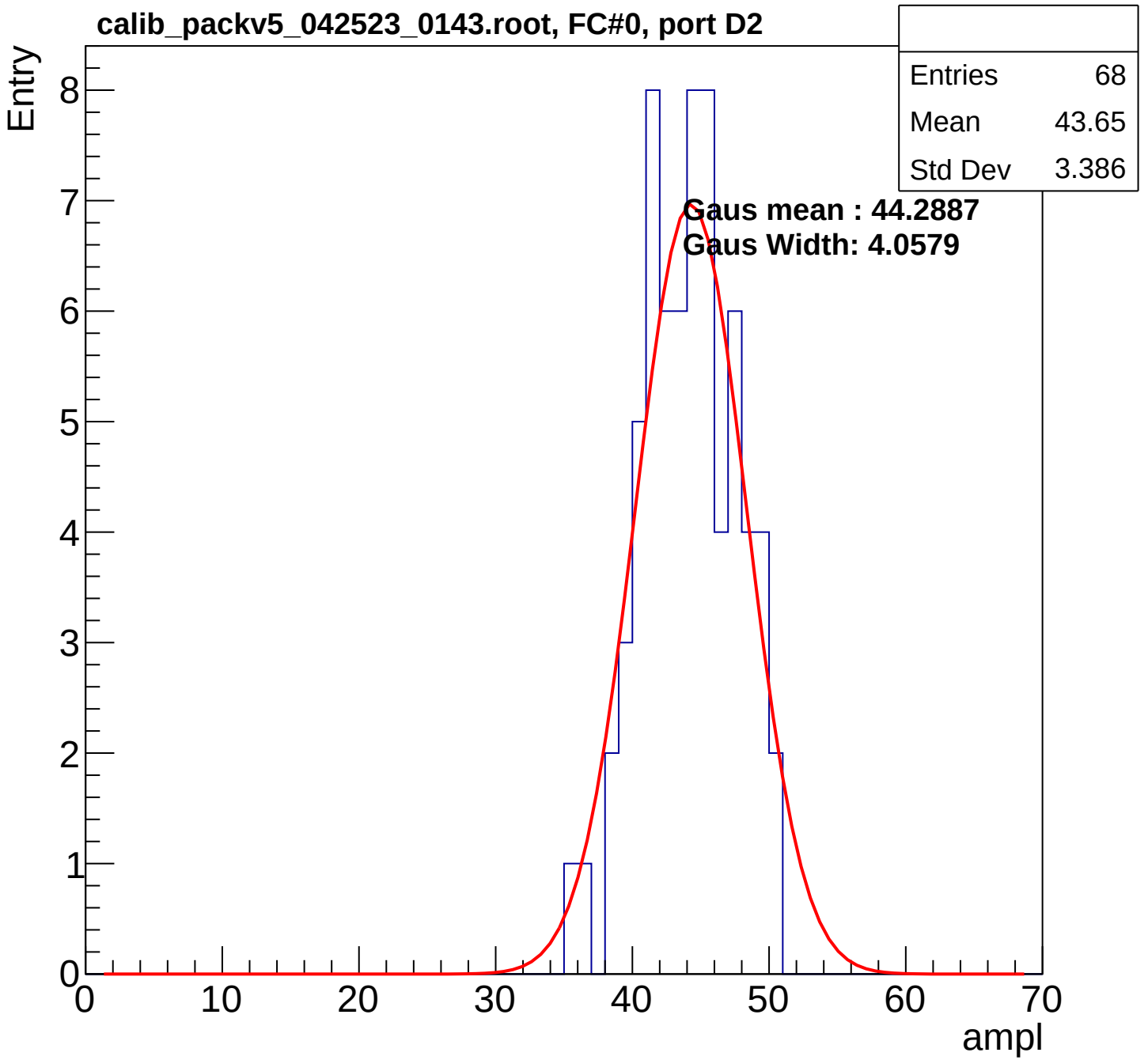
B1L101S, U10-ch19, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 43.65
Std Dev 3.386
Gaus mean : 44.2887
Gaus Width: 4.0579
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
50
60
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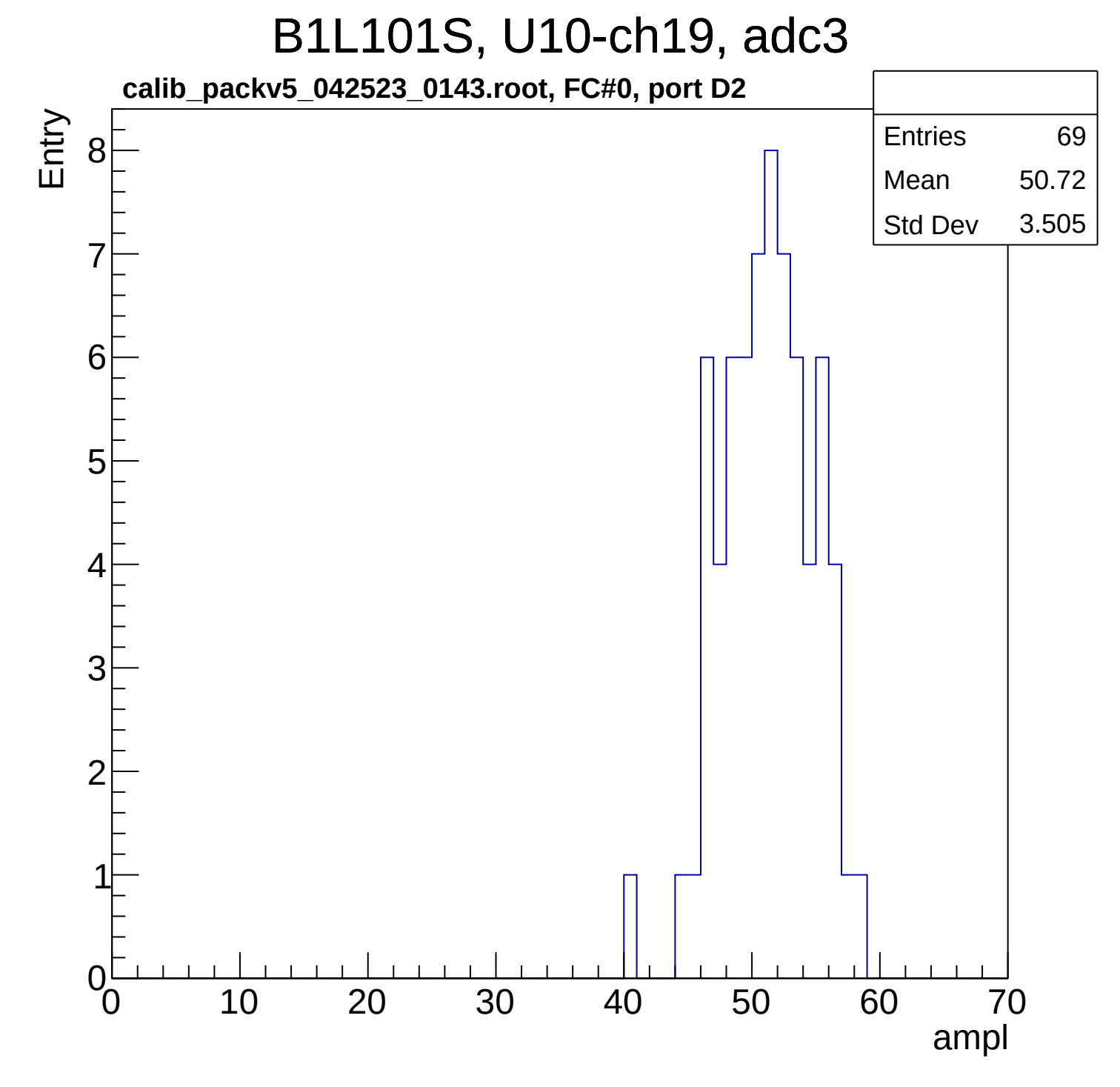
B1L101S, U10-ch19, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 50.72
Std Dev 3.505
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
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60
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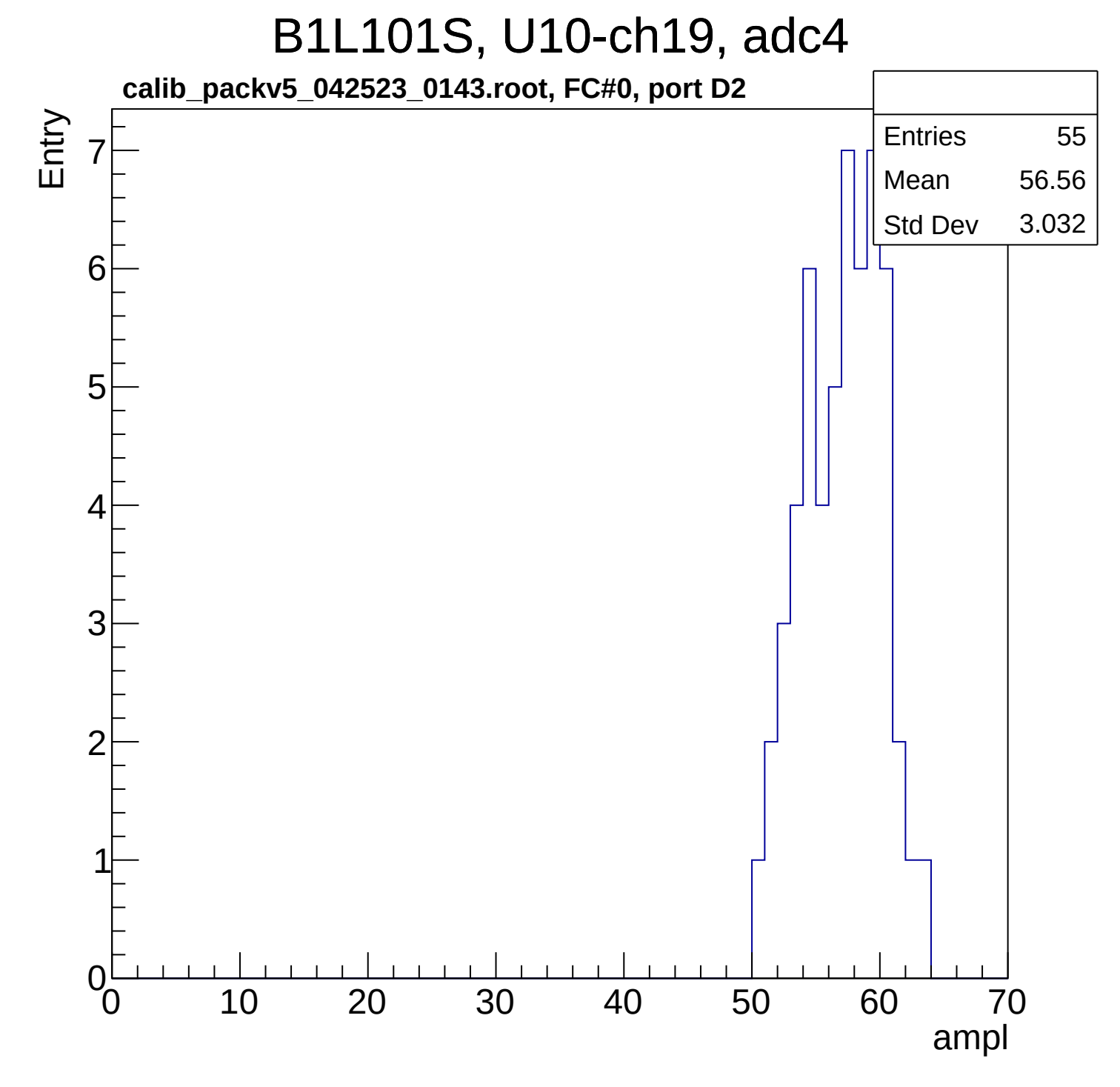
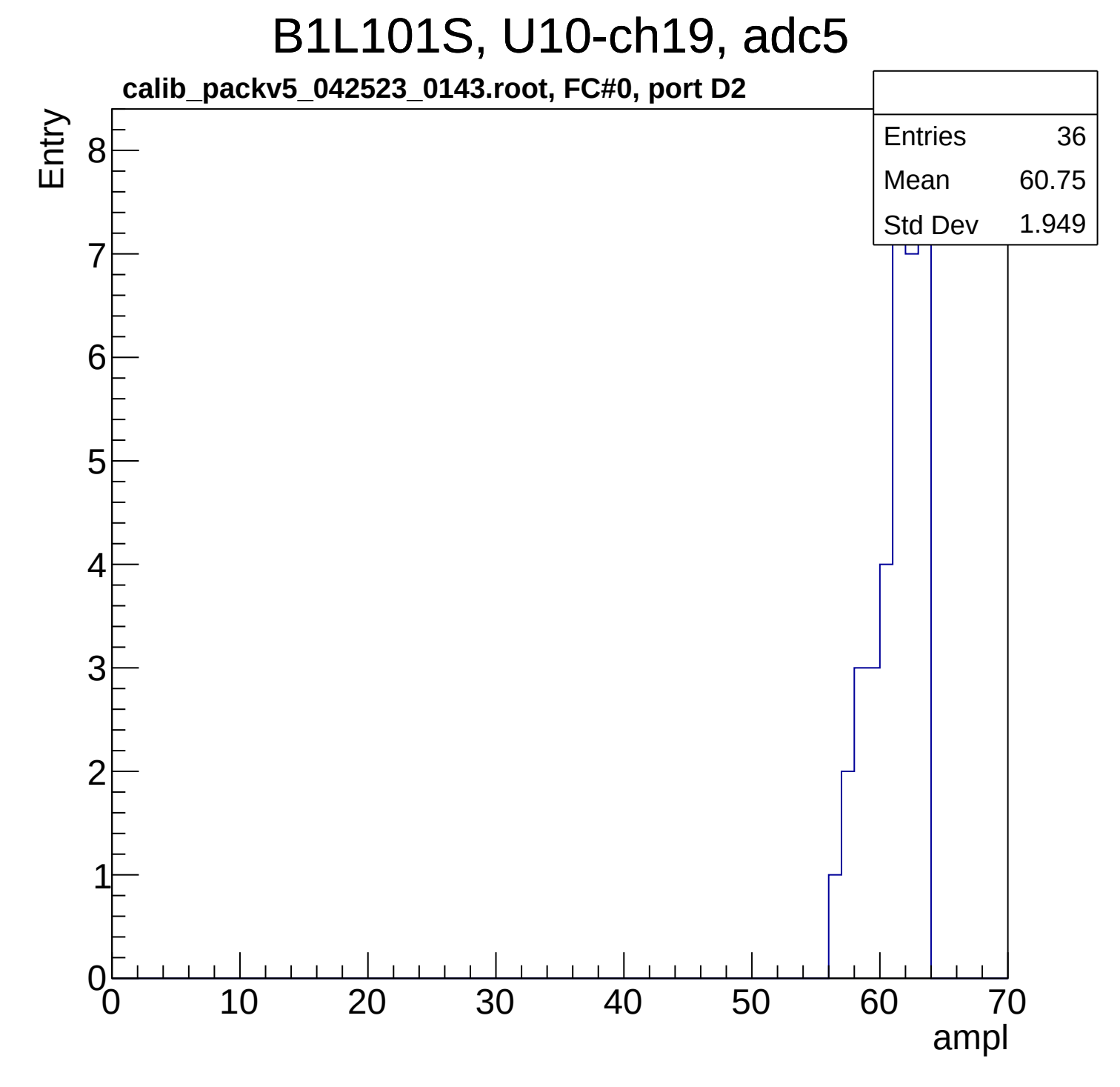

B1L101S, U10-ch19, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 56.56
Std Dev 3.032
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U10-ch19, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 36
Mean 60.75
Std Dev 1.949
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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40
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60
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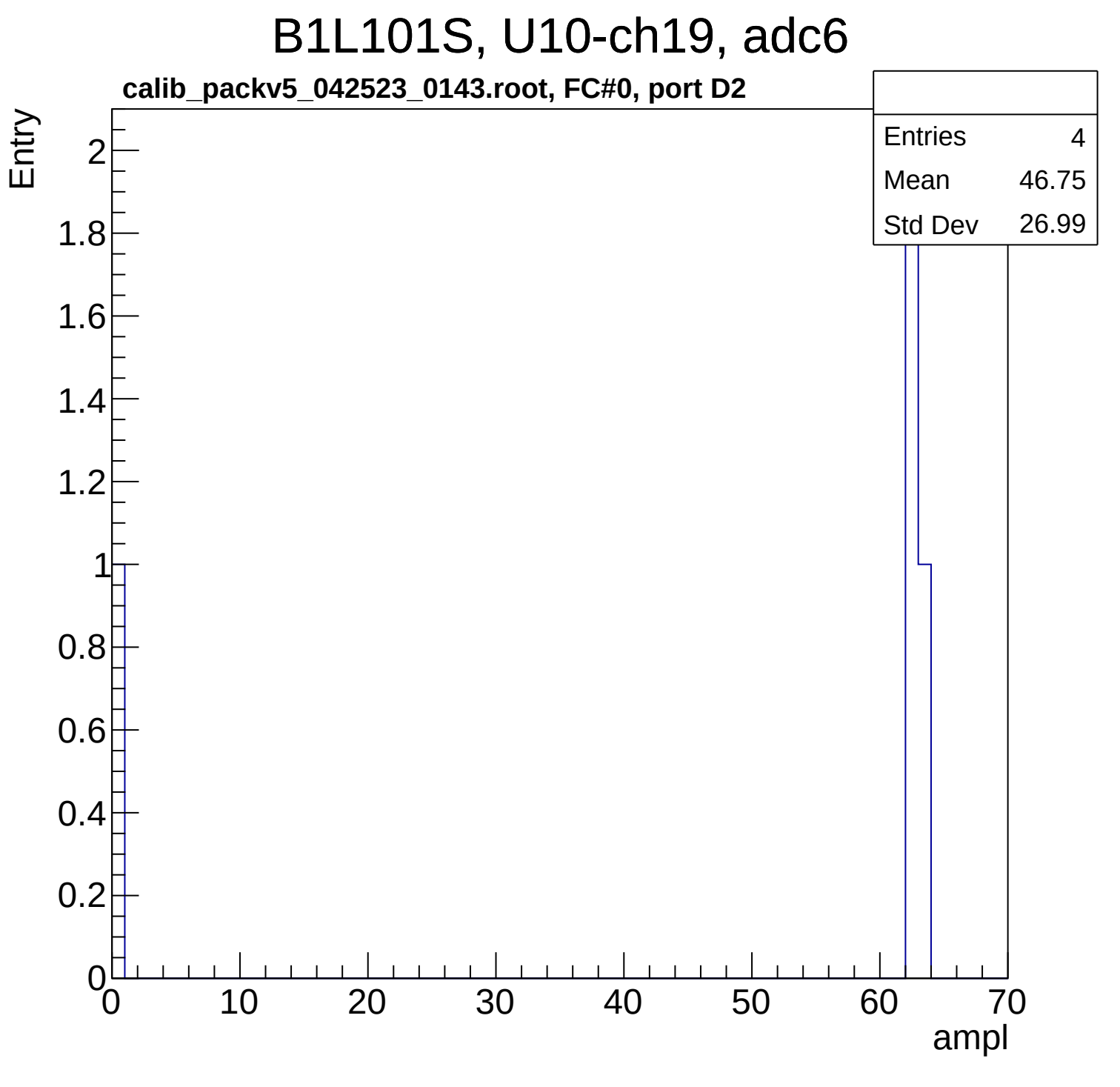
B1L101S, U10-ch19, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 46.75
Std Dev 26.99
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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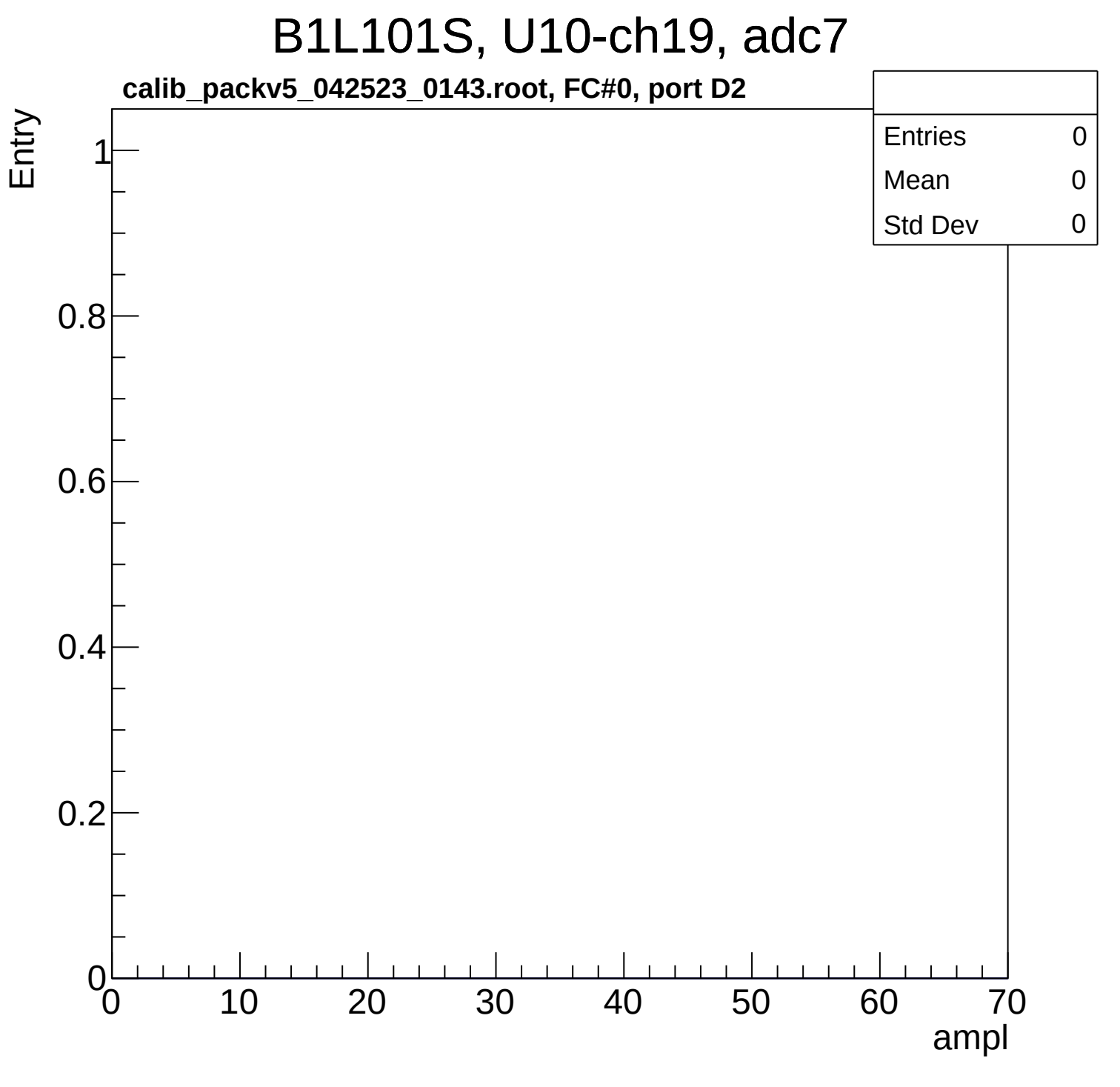
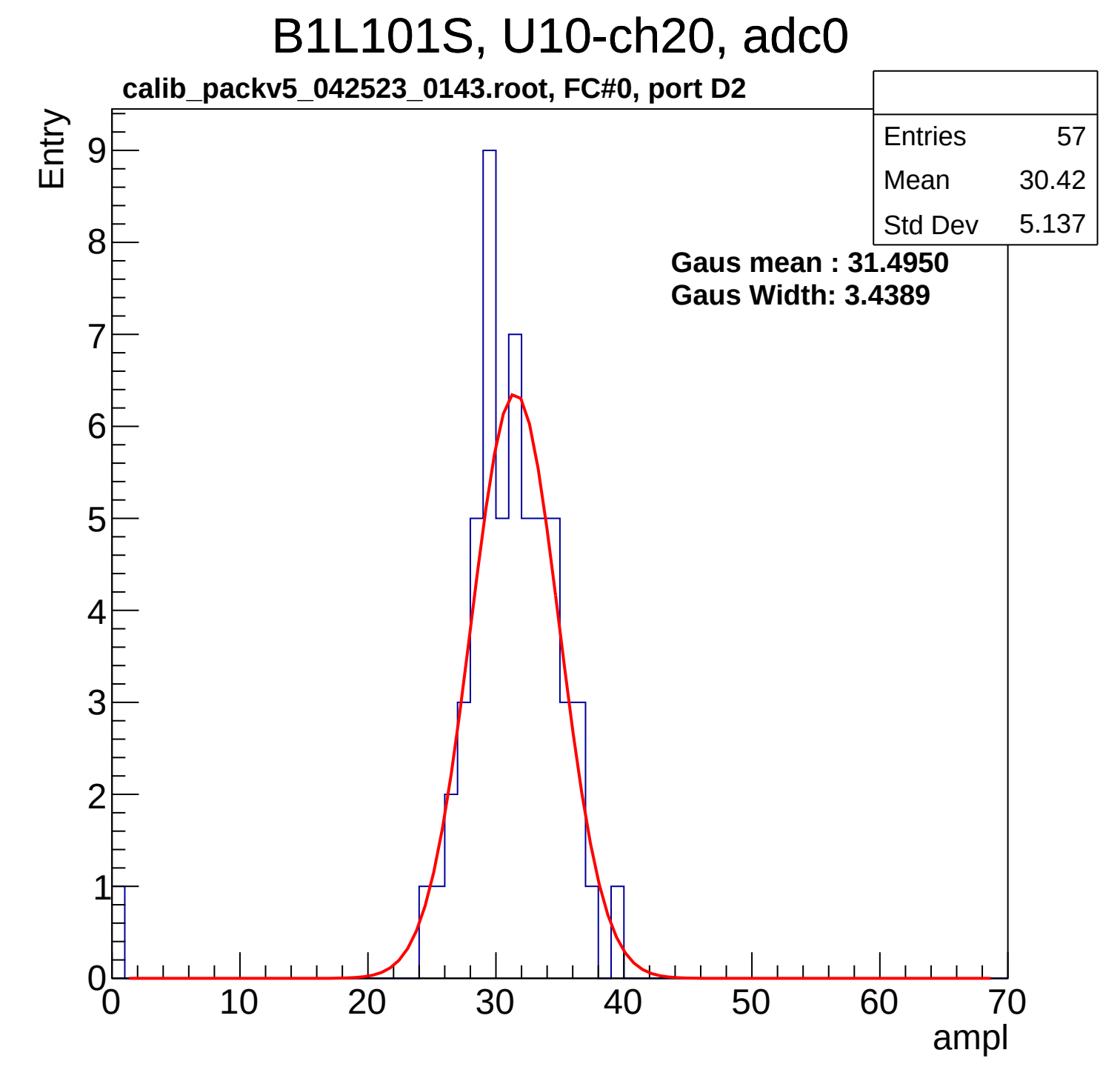

B1L101S, U10-ch19, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch20, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 30.42
Std Dev 5.137
Gaus mean : 31.4950
Gaus Width: 3.4389
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
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40
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60
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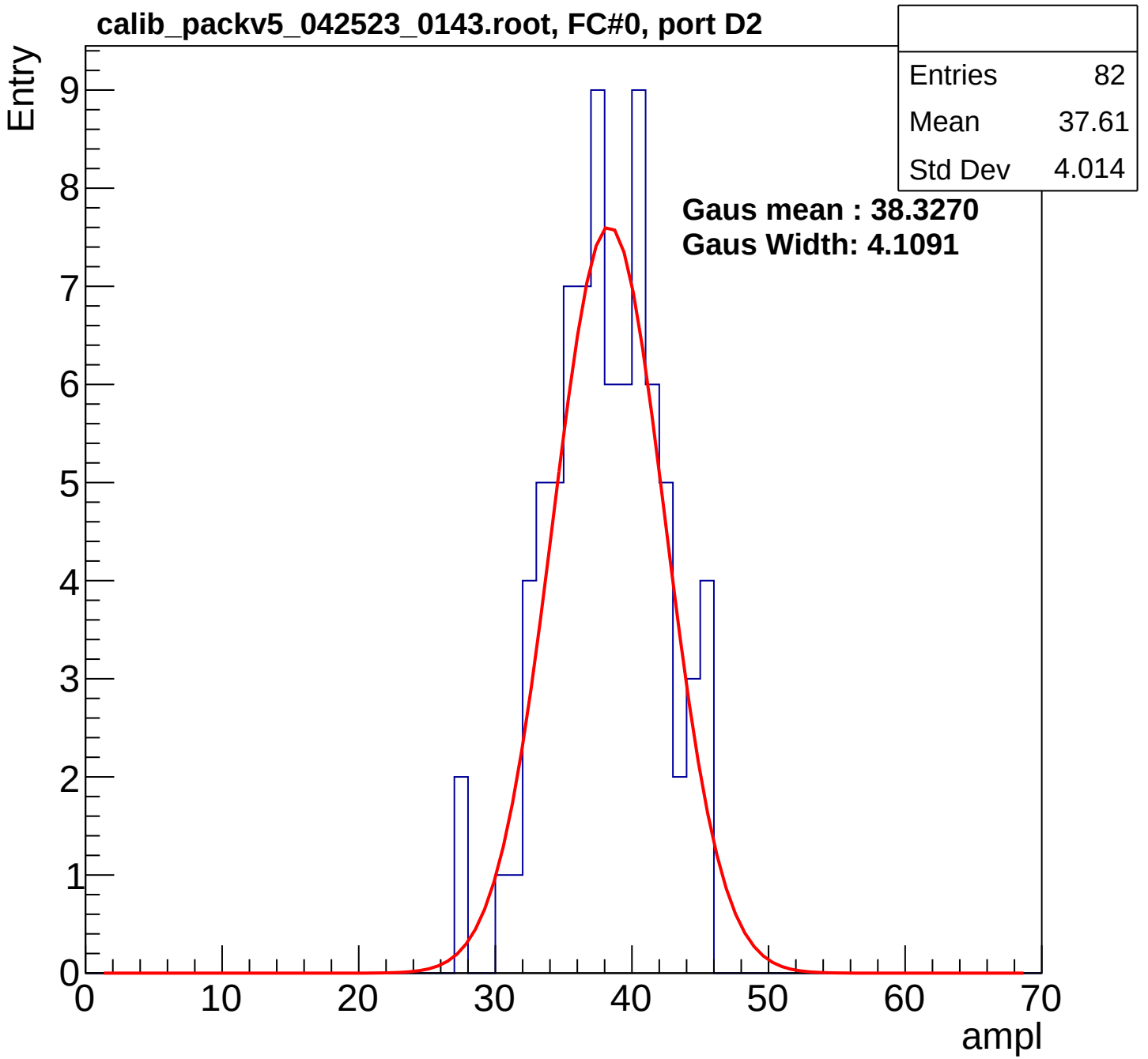
B1L101S, U10-ch20, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 82
Mean 37.61
Std Dev 4.014
Gaus mean : 38.3270
Gaus Width: 4.1091
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
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40
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60
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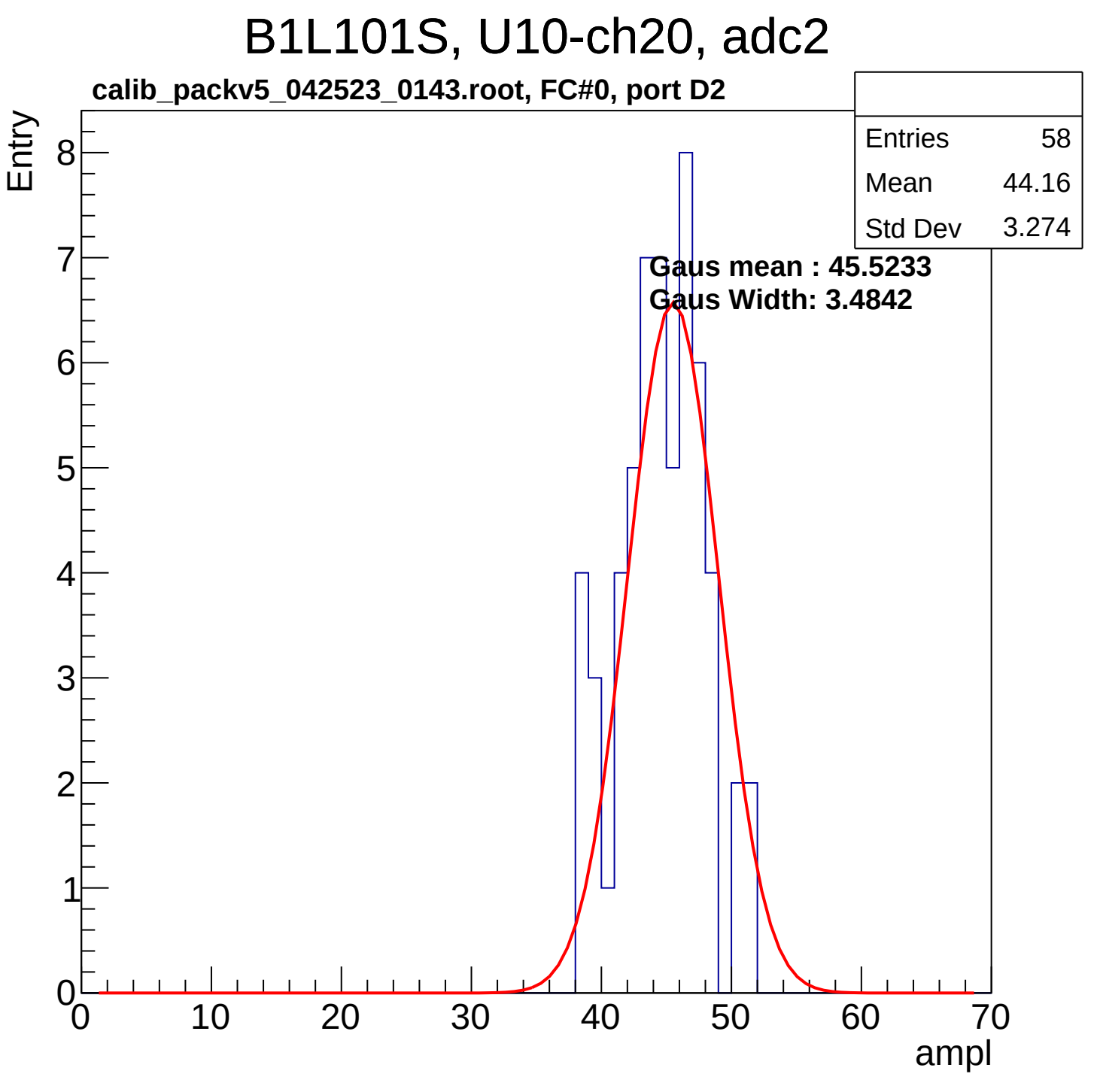
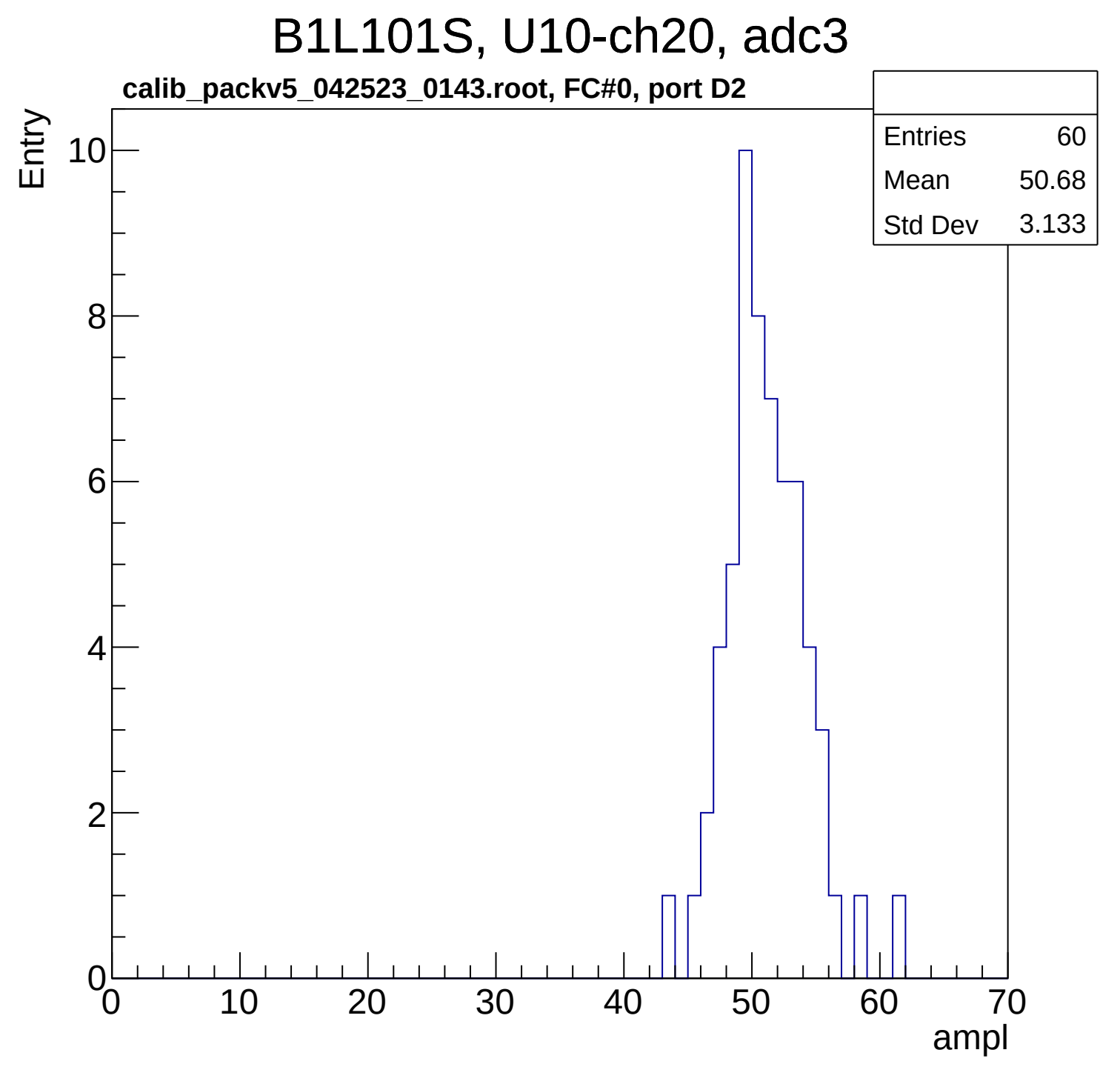
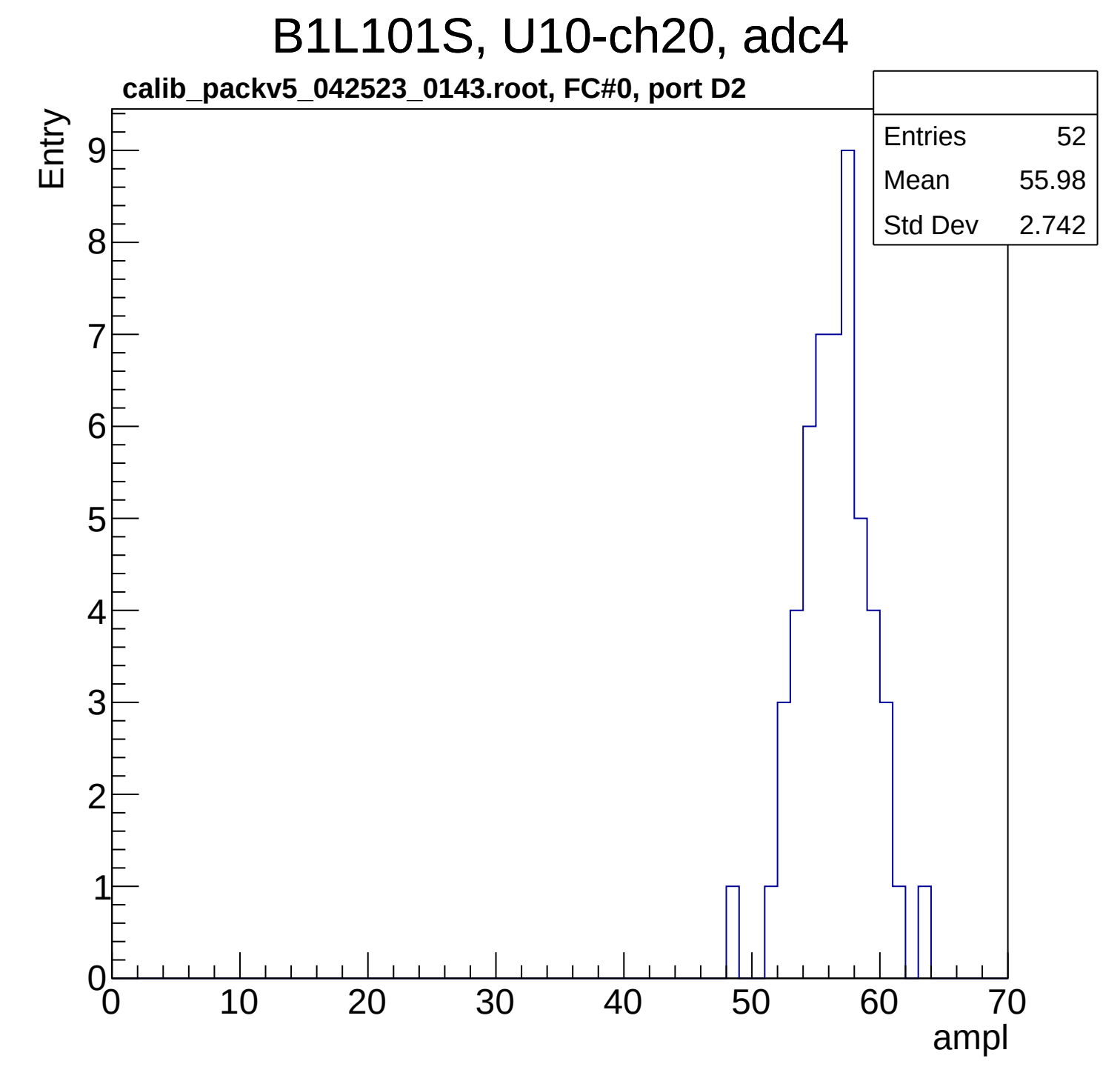

B1L101S, U10-ch20, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 44.16
Std Dev 3.274
Gaus mean : 45.5233
Gaus Width: 3.4842
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch20, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 50.68
Std Dev 3.133
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch20, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 55.98
Std Dev 2.742
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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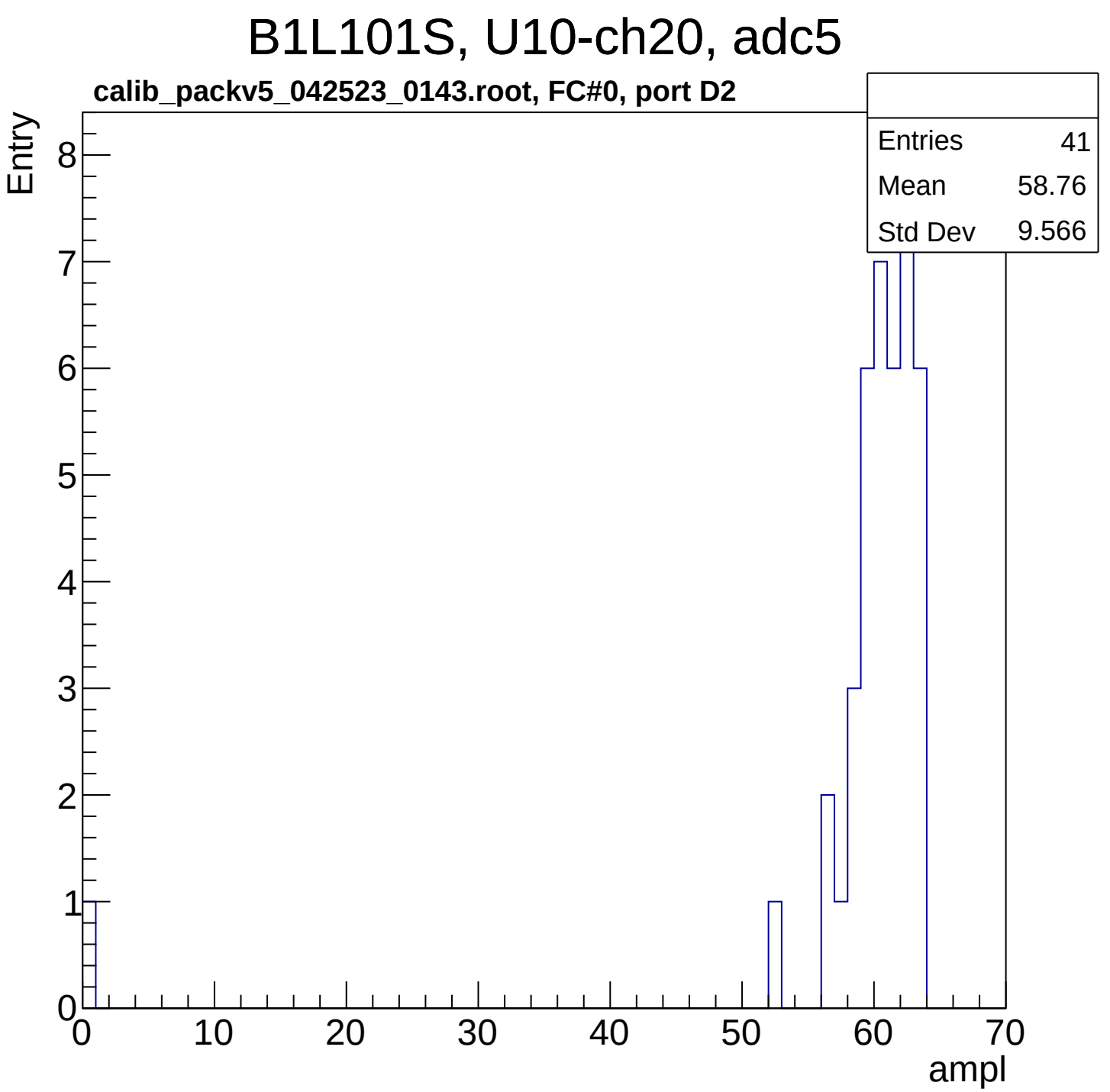
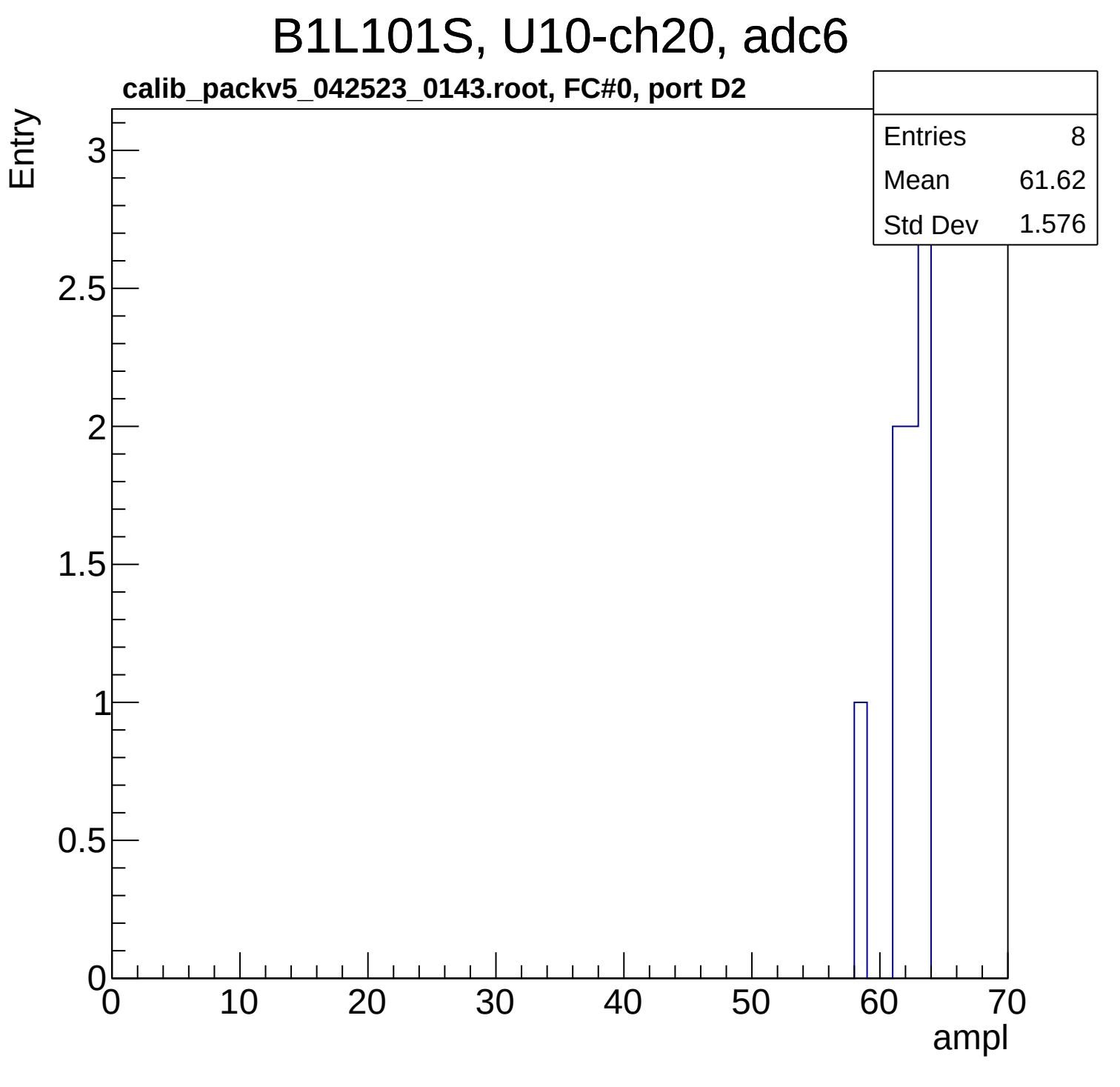
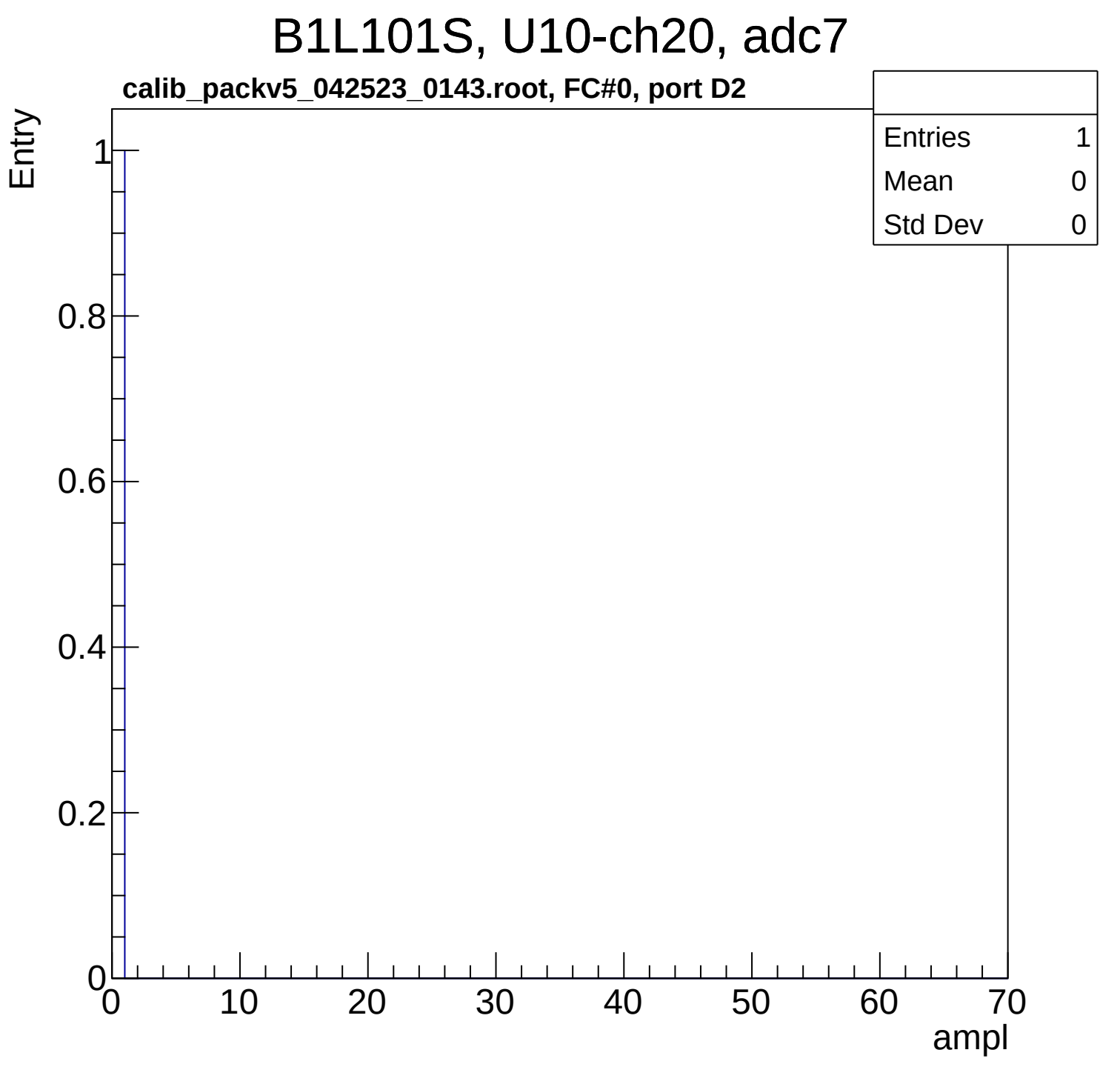
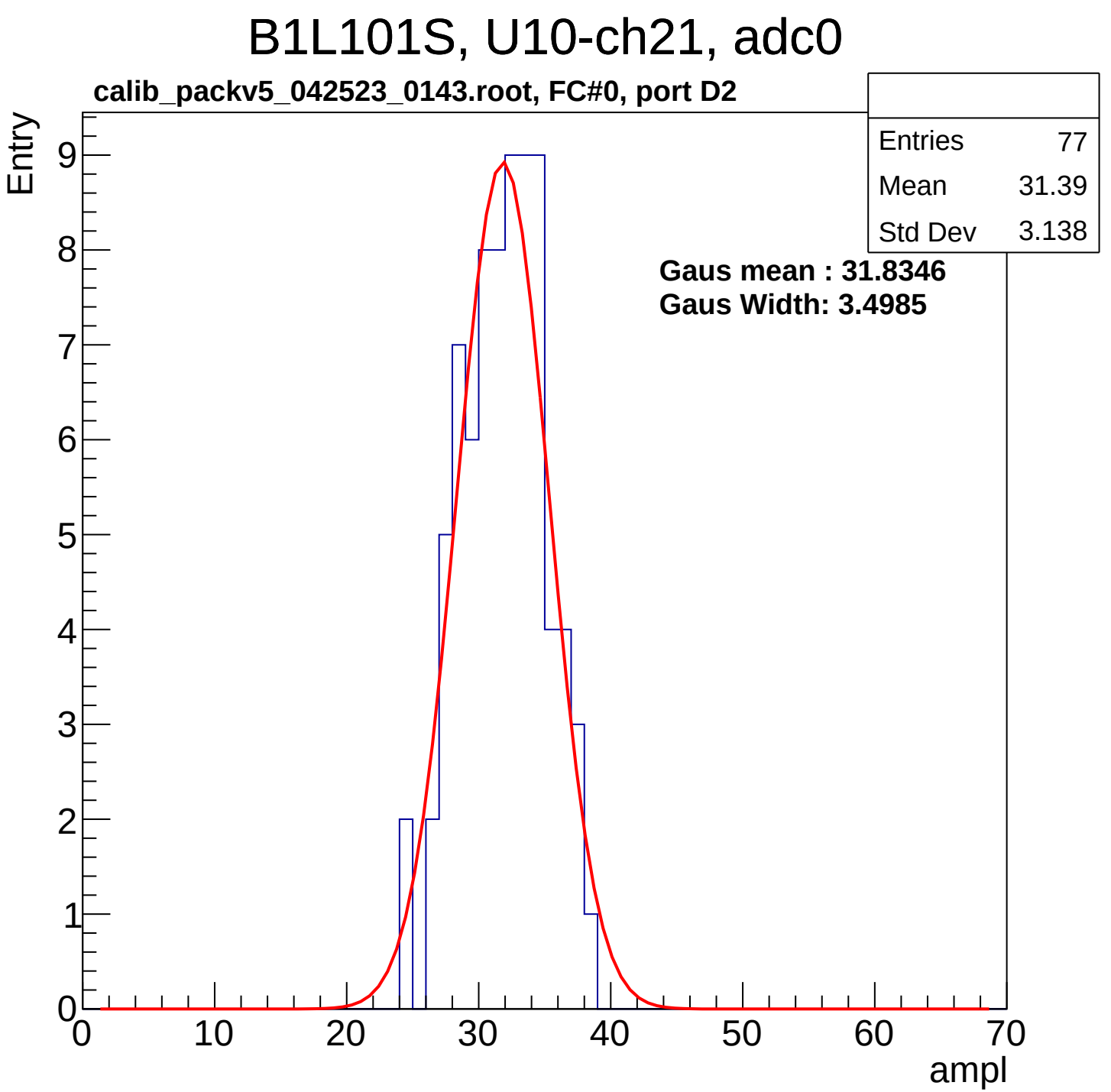
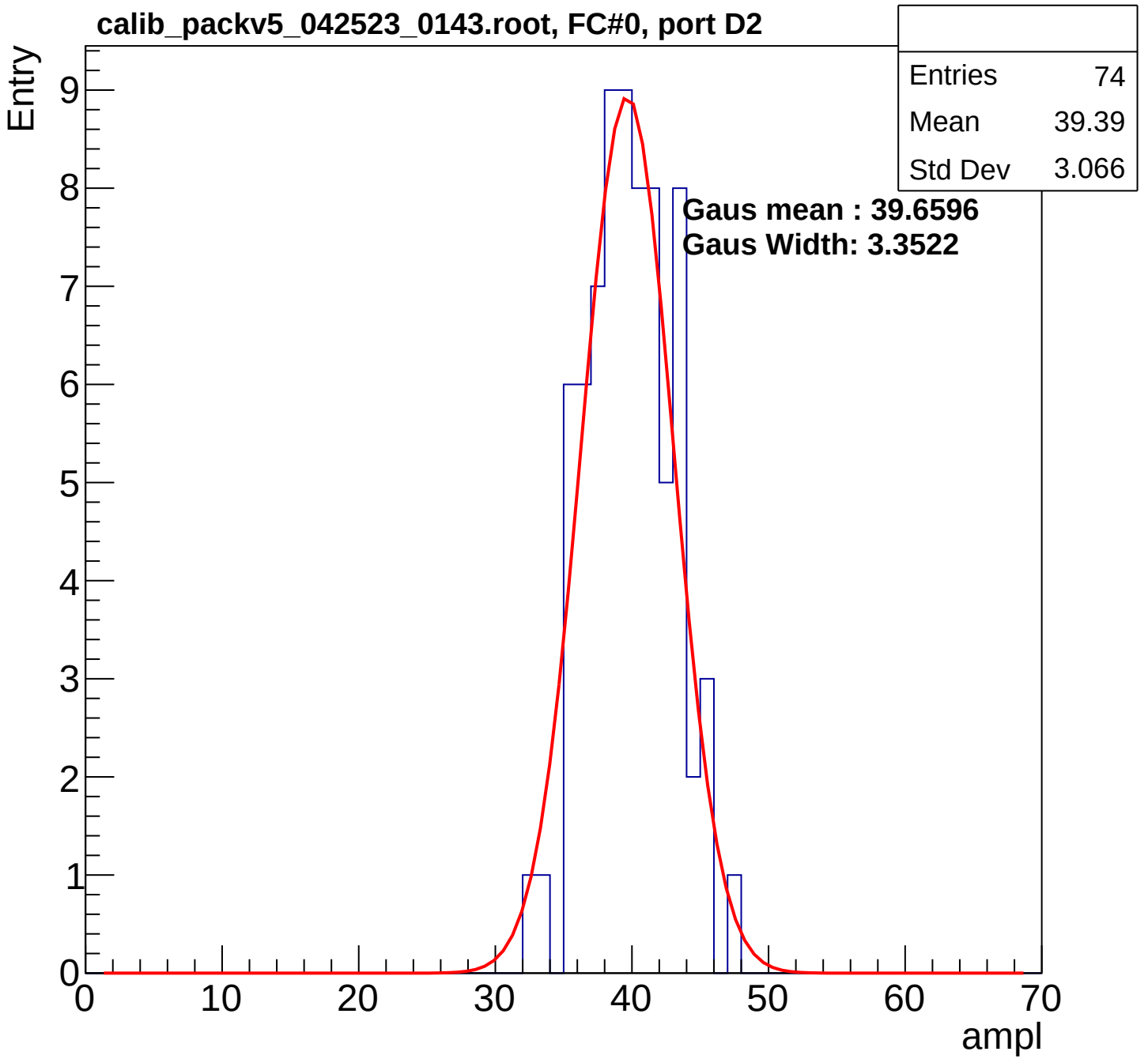

B1L101S, U10-ch20, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 41
Mean 58.76
Std Dev 9.566
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch20, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 61.62
Std Dev 1.576
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U10-ch20, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch21, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 31.39
Std Dev 3.138
Gaus mean : 31.8346
Gaus Width: 3.4985
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch21, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 39.39
Std Dev 3.066
Gaus mean : 39.6596
Gaus Width: 3.3522
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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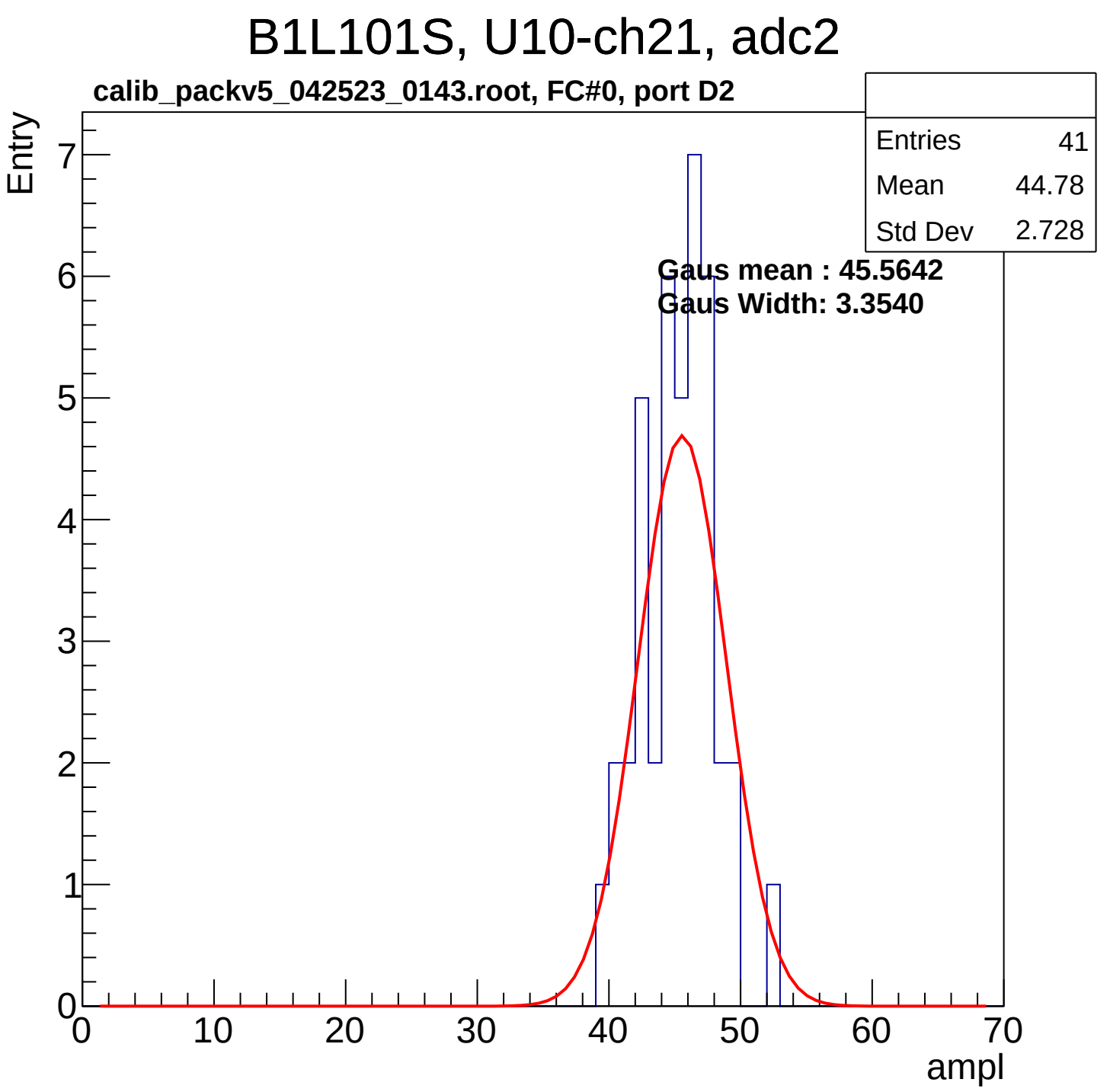
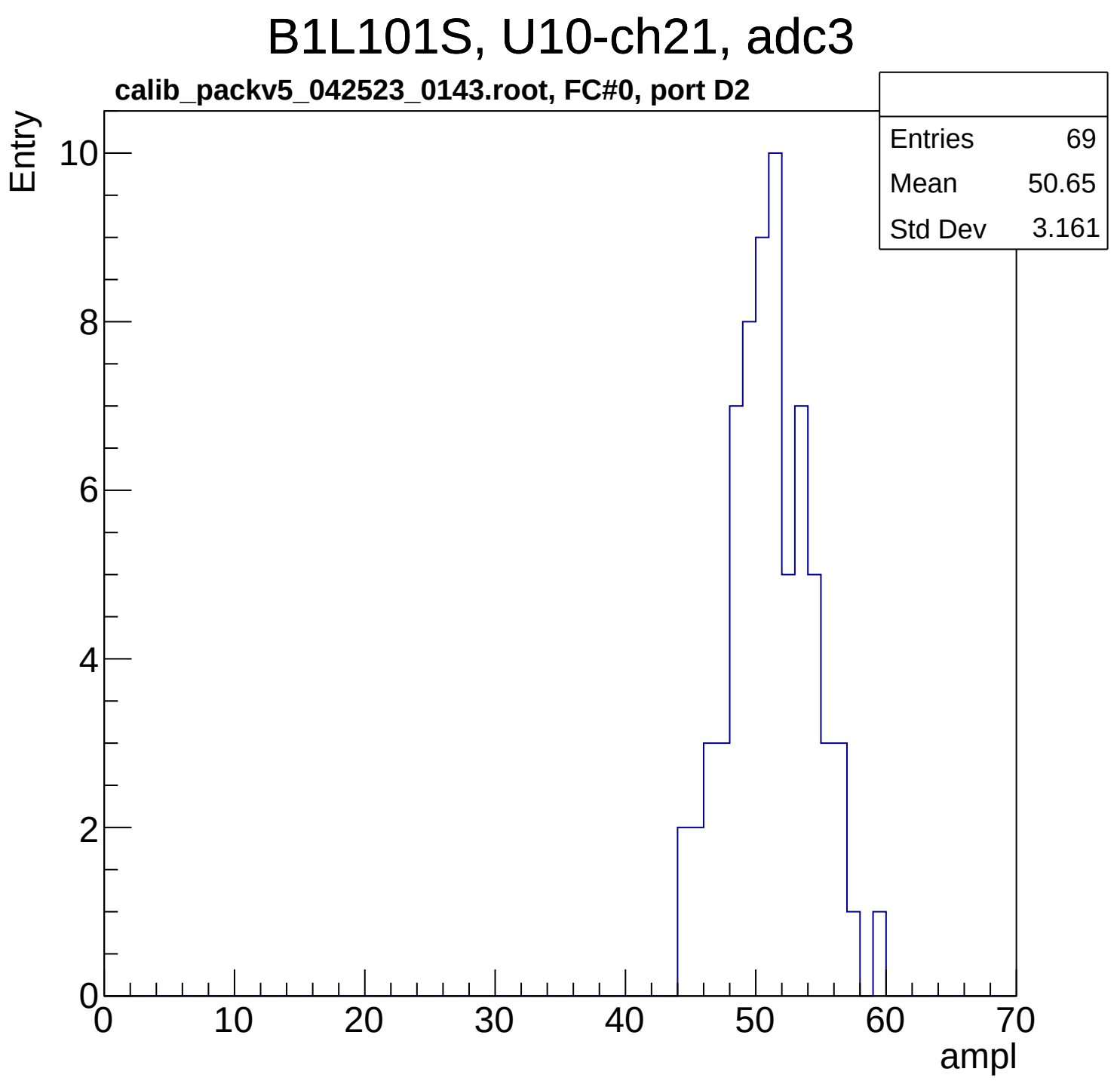
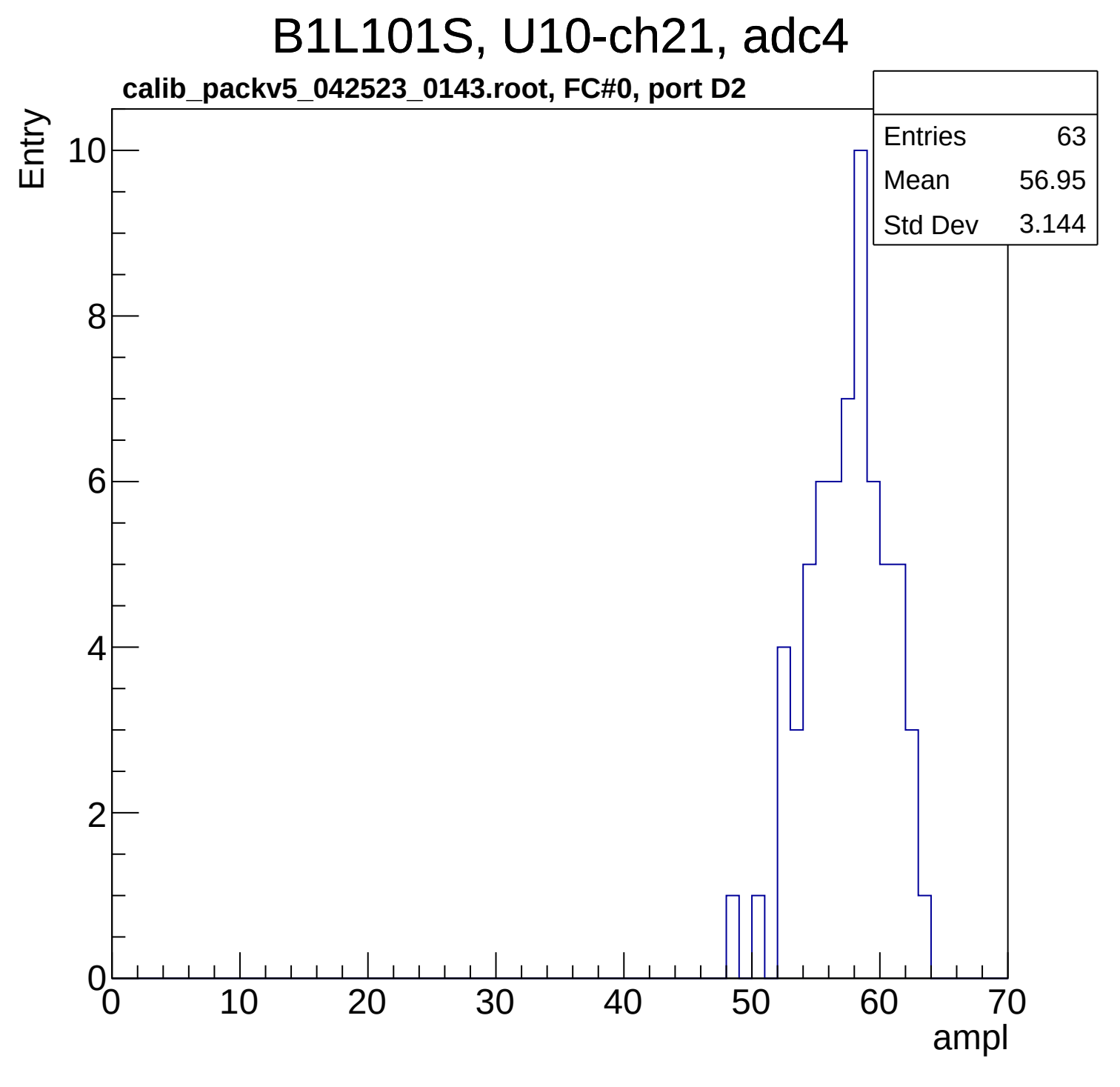

B1L101S, U10-ch21, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 41
Mean 44.78
Std Dev 2.728
Gaus mean : 45.5642
Gaus Width: 3.3540
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U10-ch21, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 50.65
Std Dev 3.161
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch21, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 56.95
Std Dev 3.144
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
50
60
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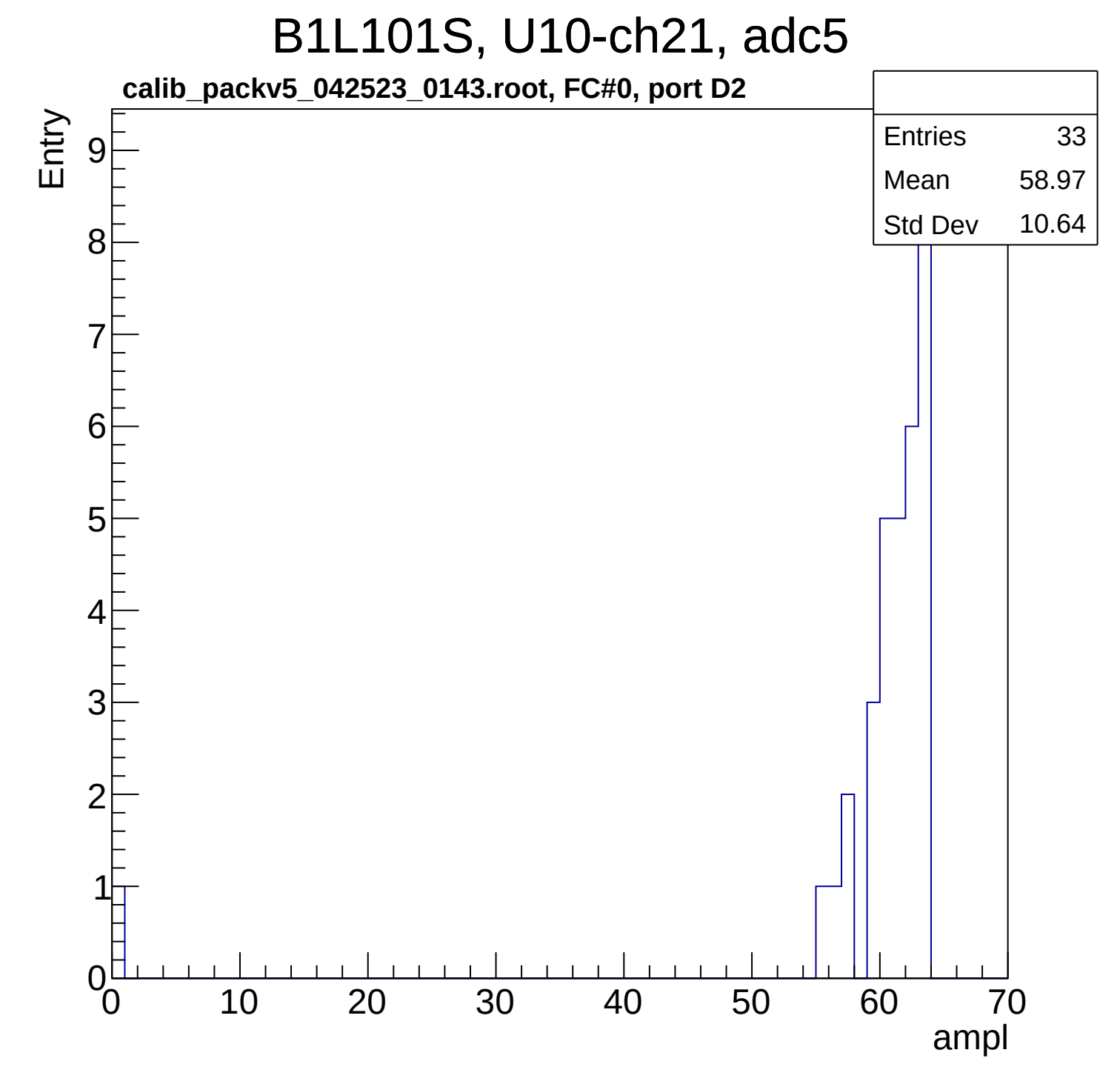
B1L101S, U10-ch21, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 33
Mean 58.97
Std Dev 10.64
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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60
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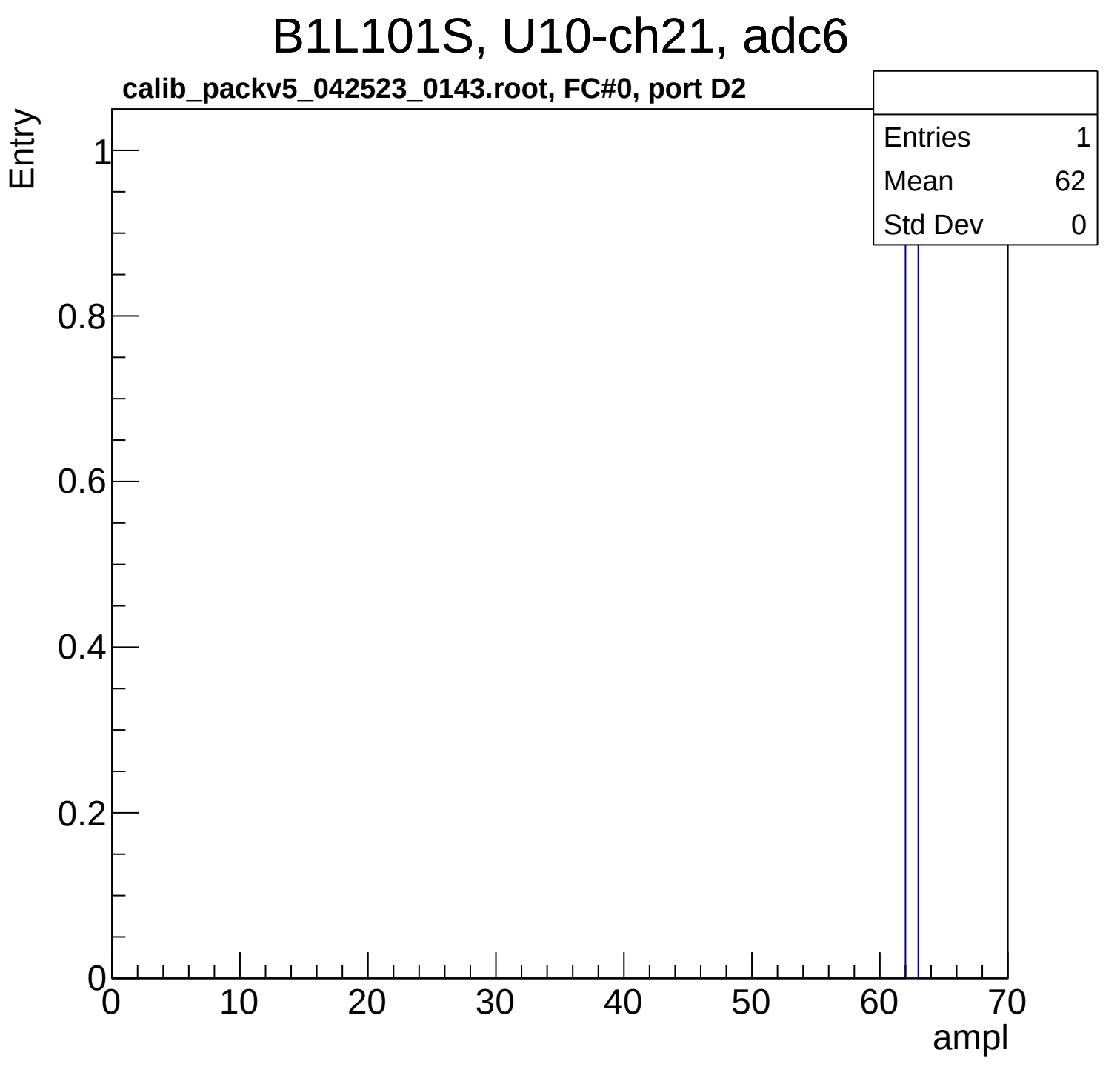
B1L101S, U10-ch21, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 62
Std Dev 0
Entry
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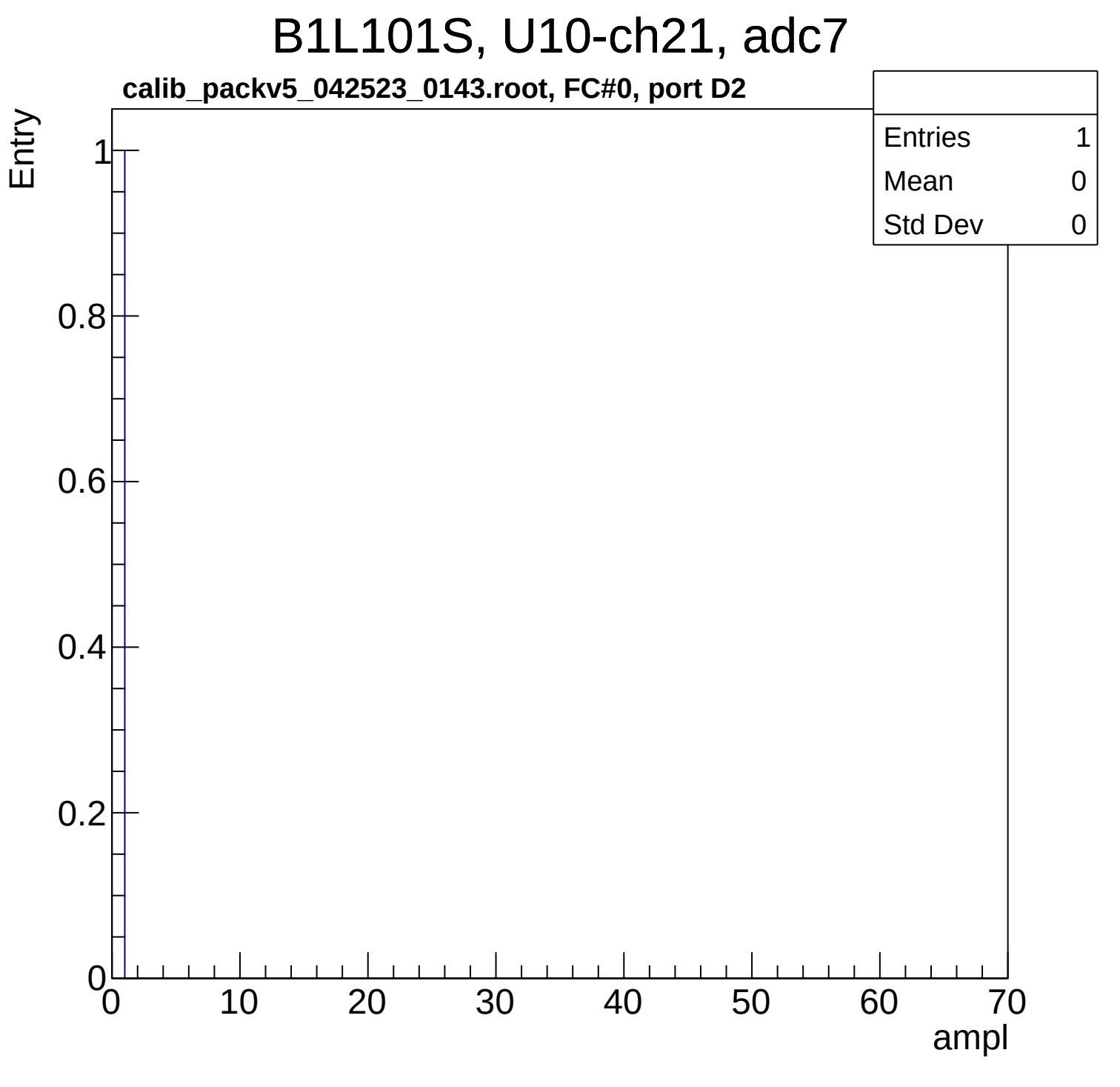
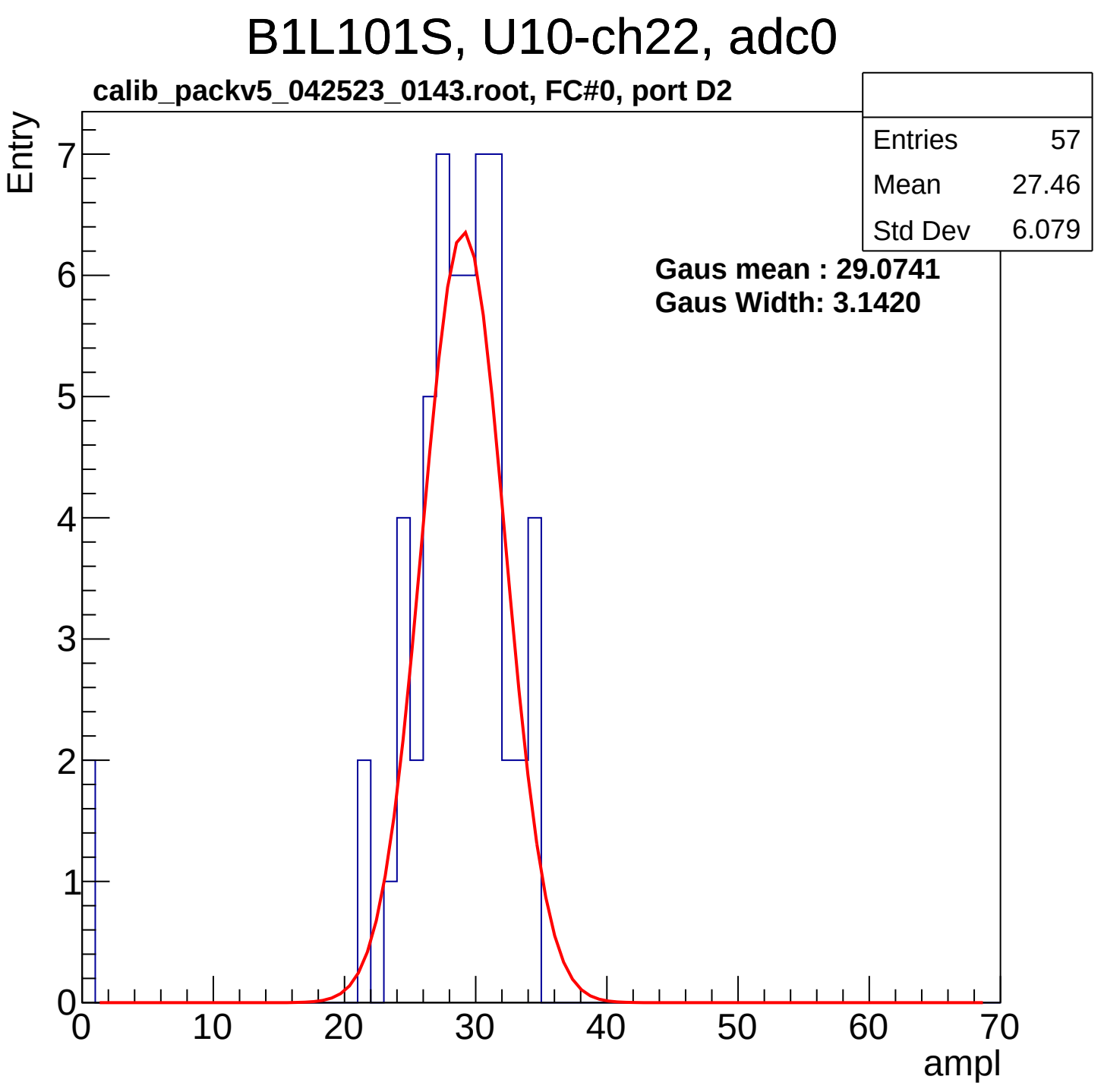
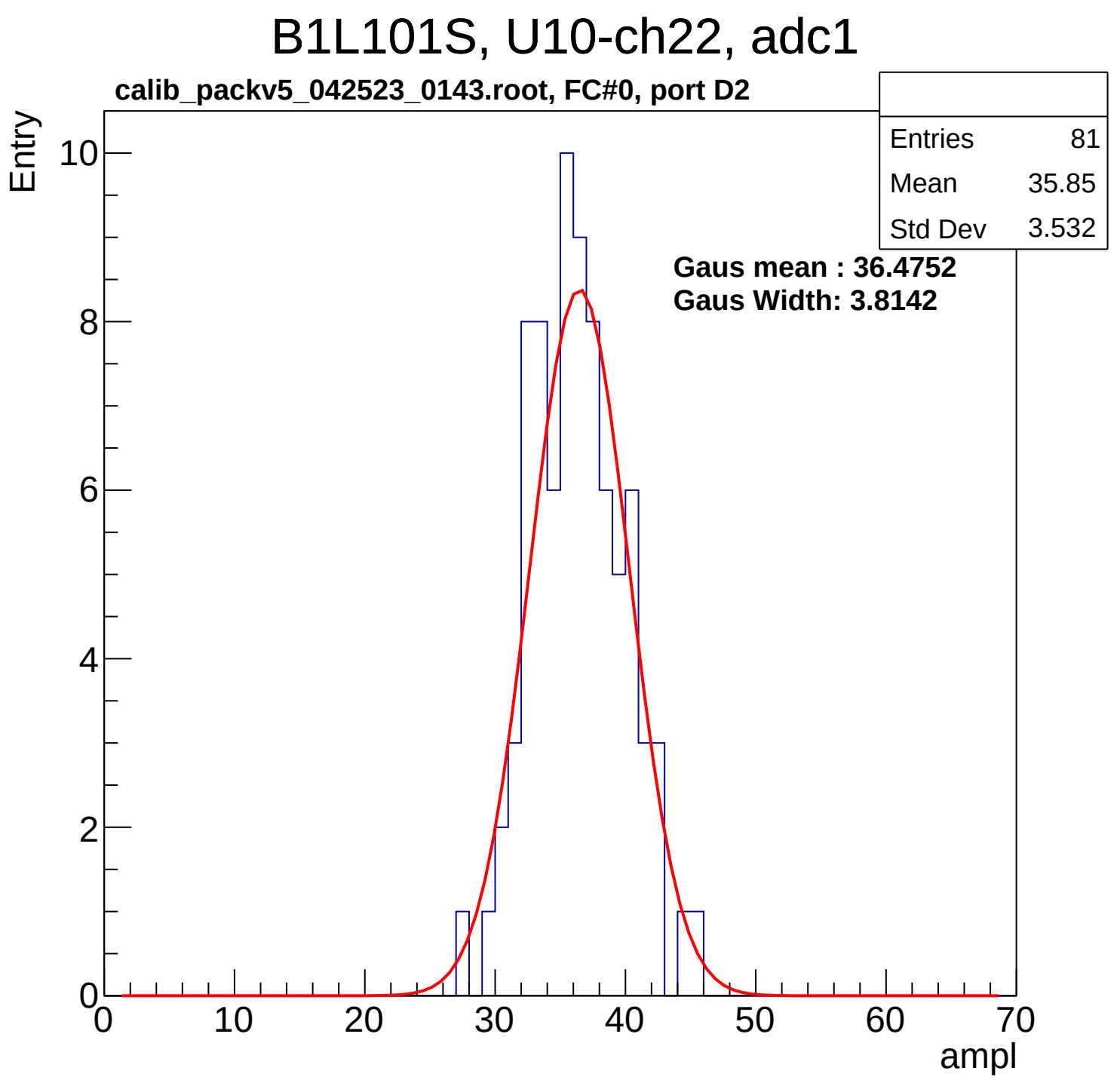
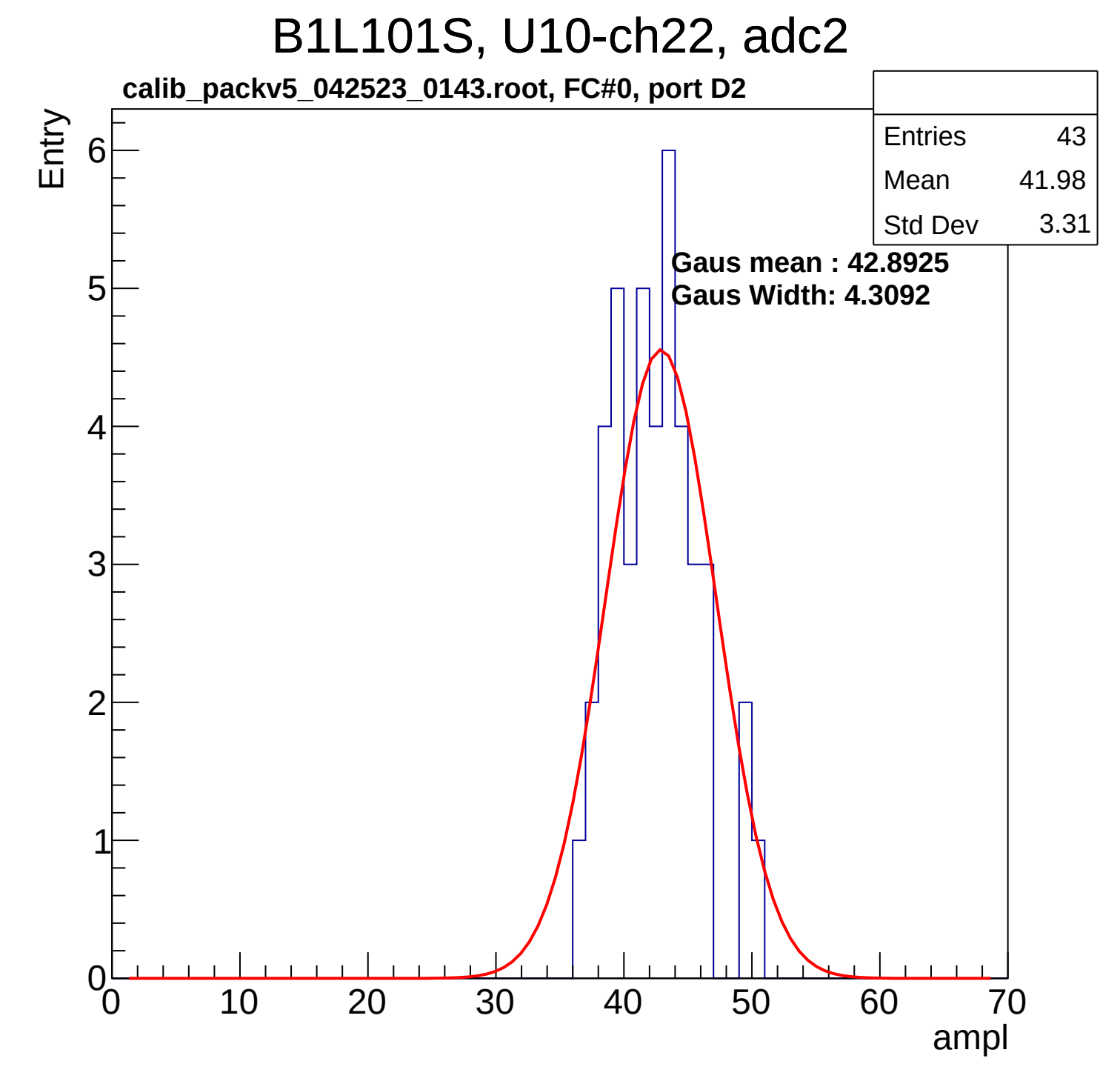
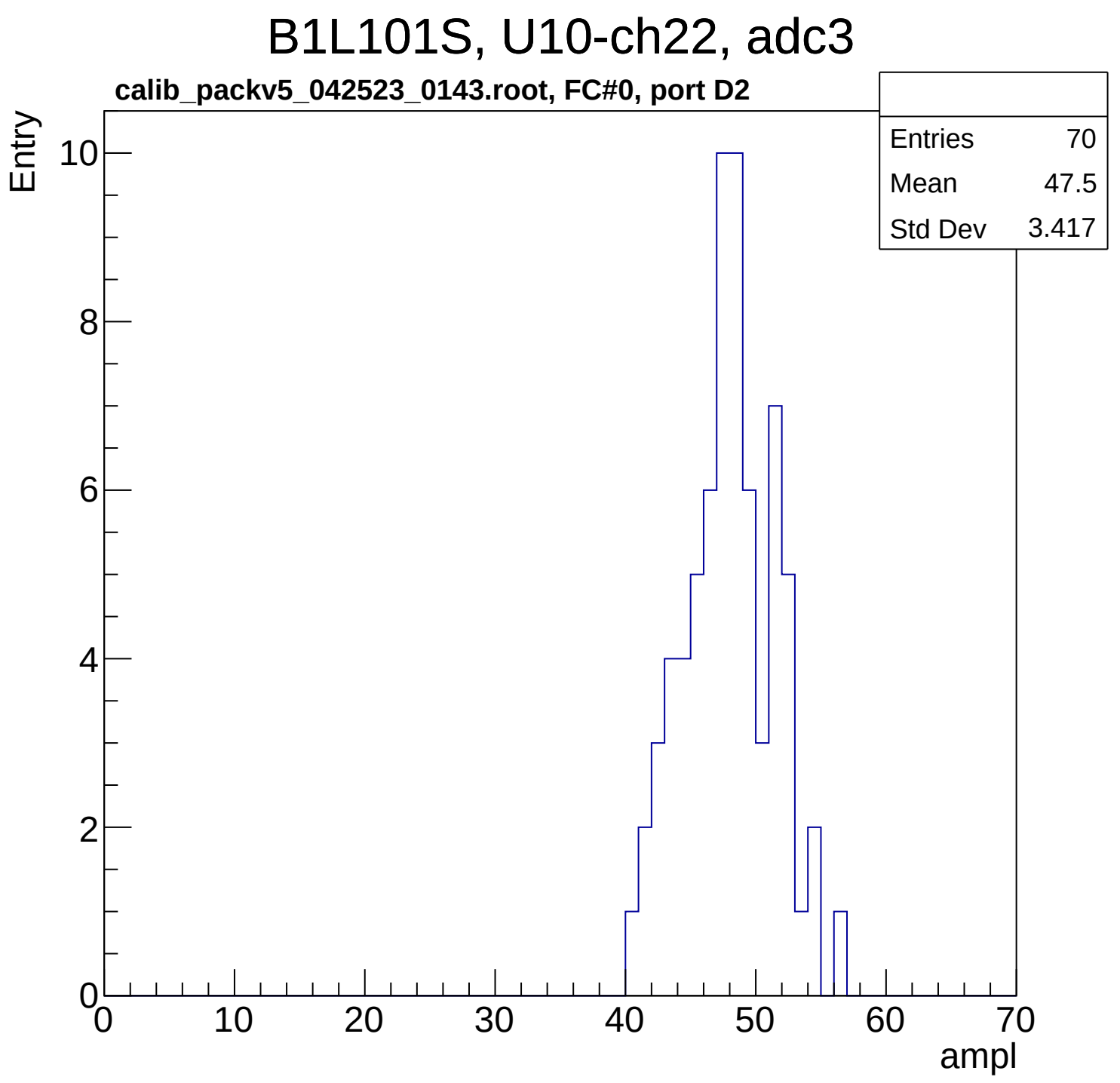
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

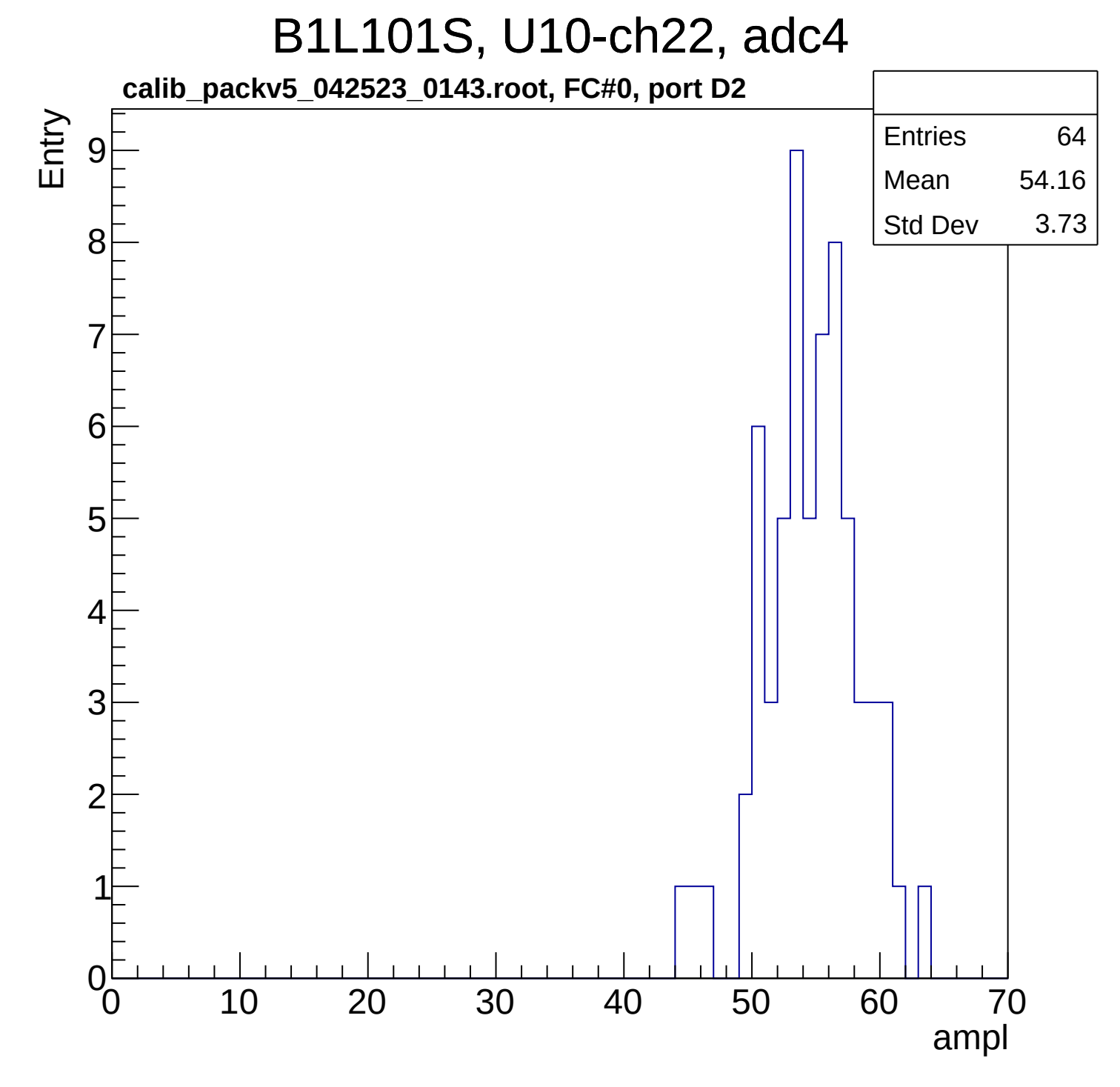

B1L101S, U10-ch21, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch22, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 27.46
Std Dev 6.079
Gaus mean : 29.0741
Gaus Width: 3.1420
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U10-ch22, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 81
Mean 35.85
Std Dev 3.532
Gaus mean : 36.4752
Gaus Width: 3.8142
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch22, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 43
Mean 41.98
Std Dev 3.31
Gaus mean : 42.8925
Gaus Width: 4.3092
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L101S, U10-ch22, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 47.5
Std Dev 3.417
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch22, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 54.16
Std Dev 3.73
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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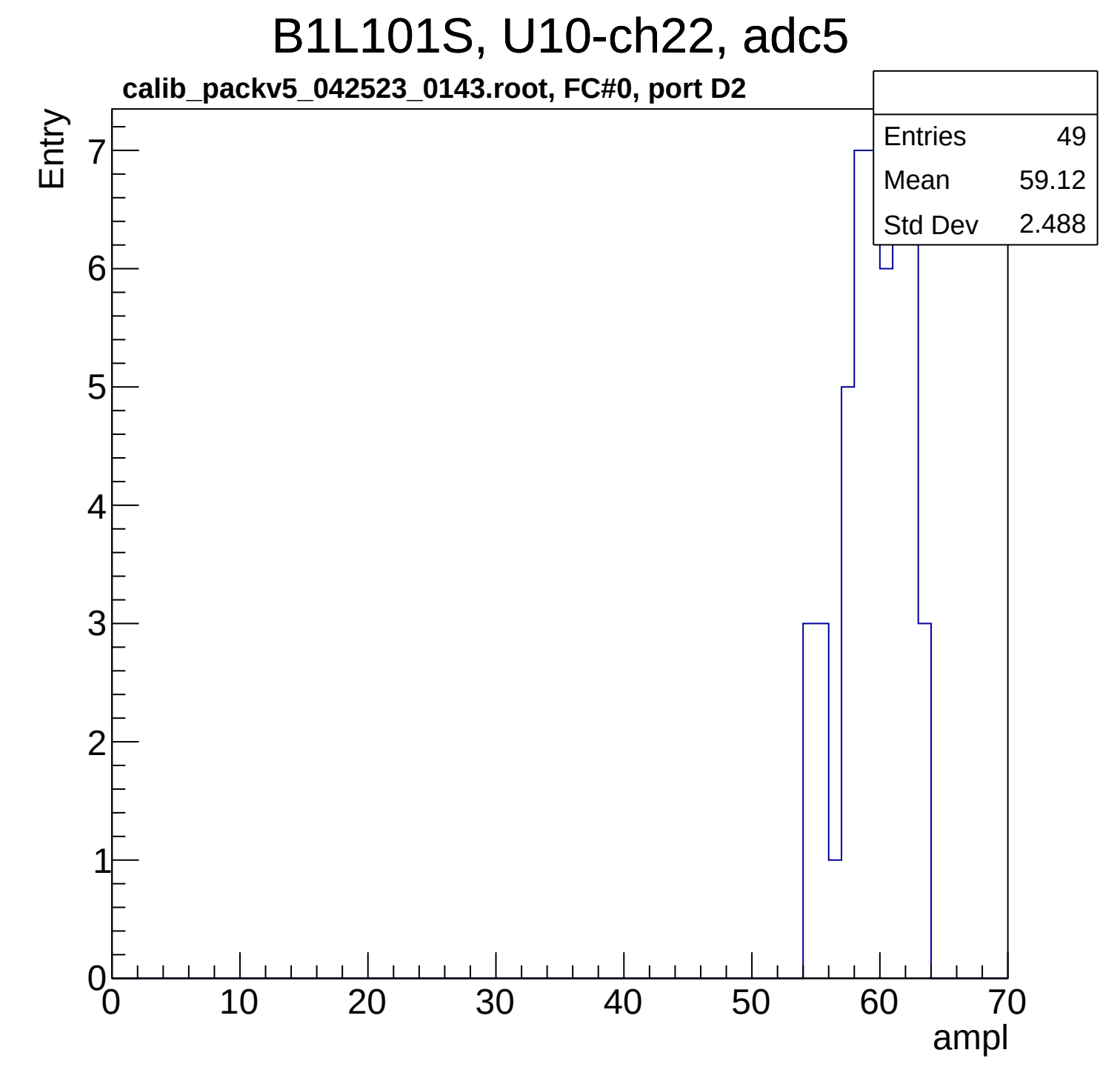
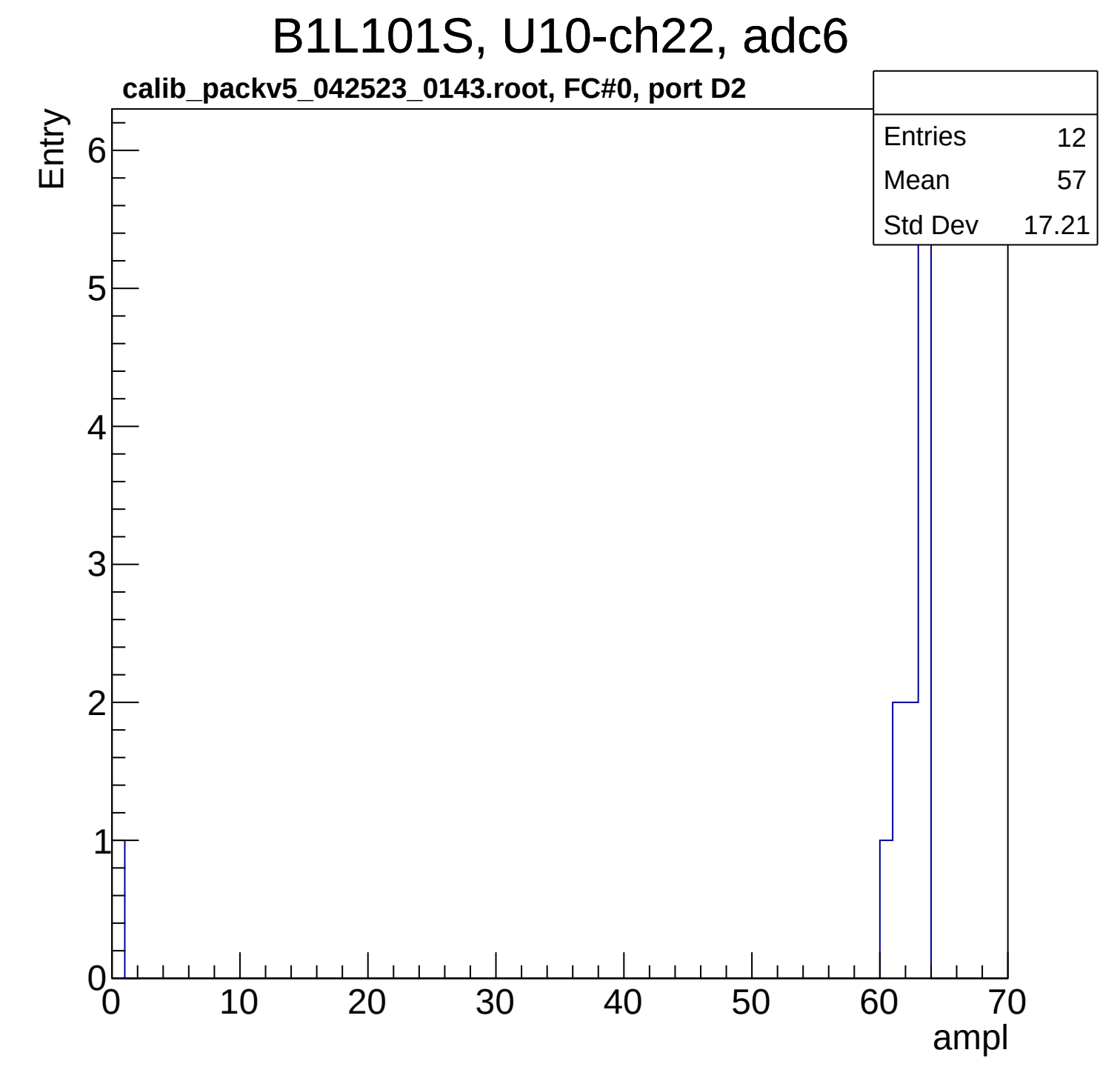

B1L101S, U10-ch22, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 59.12
Std Dev 2.488
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U10-ch22, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 12
Mean 57
Std Dev 17.21
Entry
0
1
2
3
4
5
6
0
10
20
30
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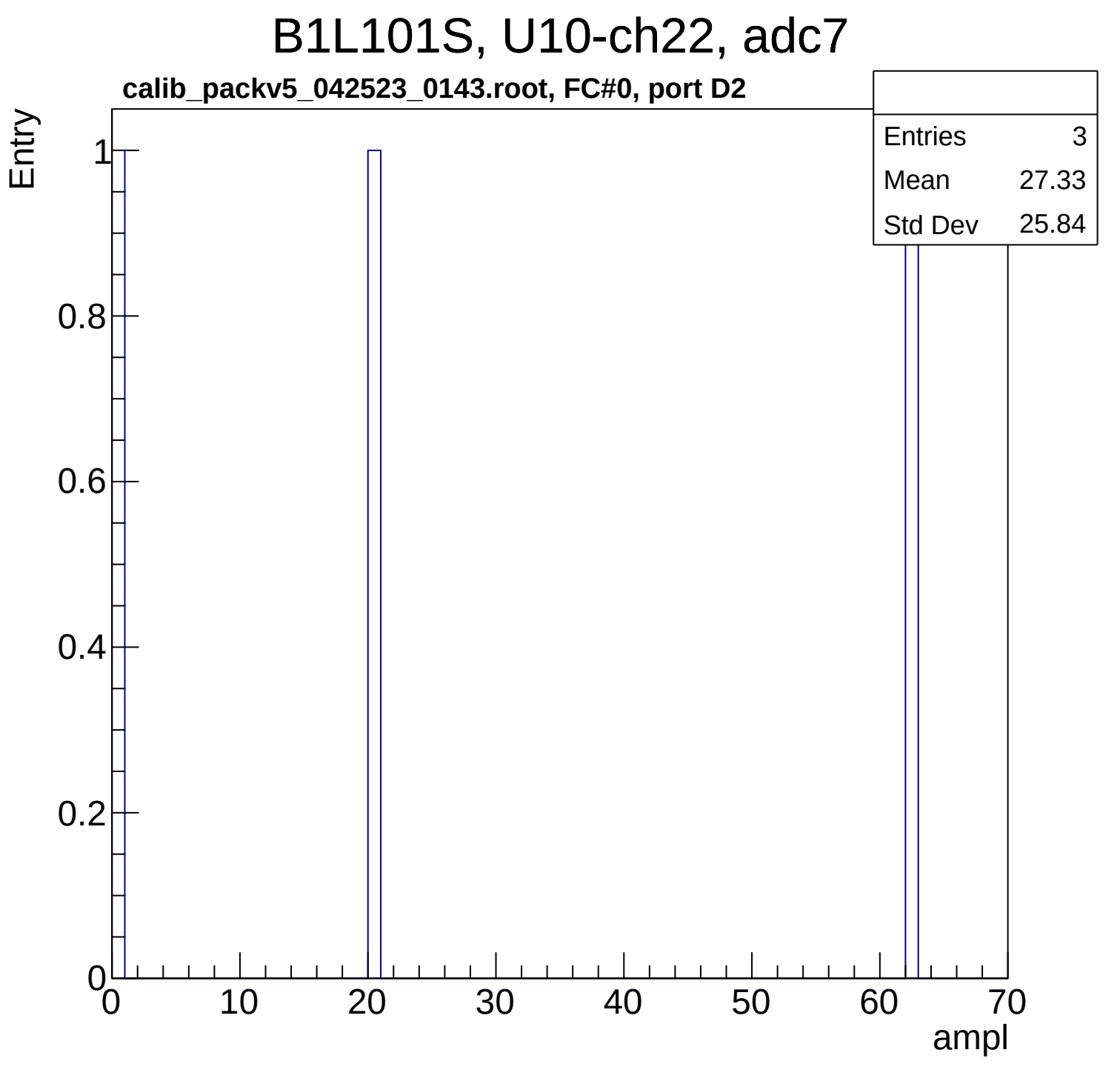
50
60
70
ampl


B1L101S, U10-ch22, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 27.33
Std Dev 25.84
Entry
ampl
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0.2
0.4
0.6
0.8
1
0
10
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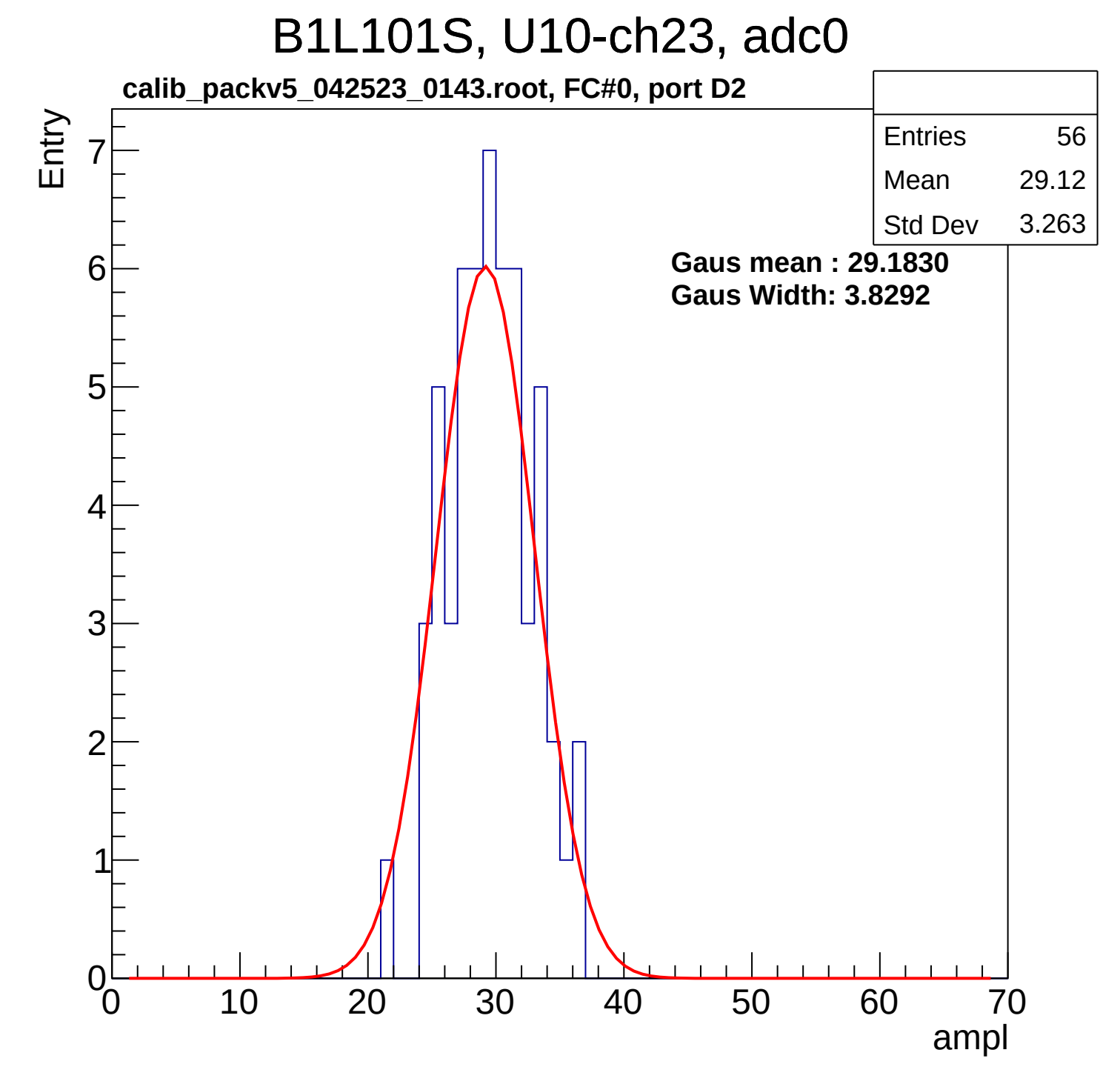
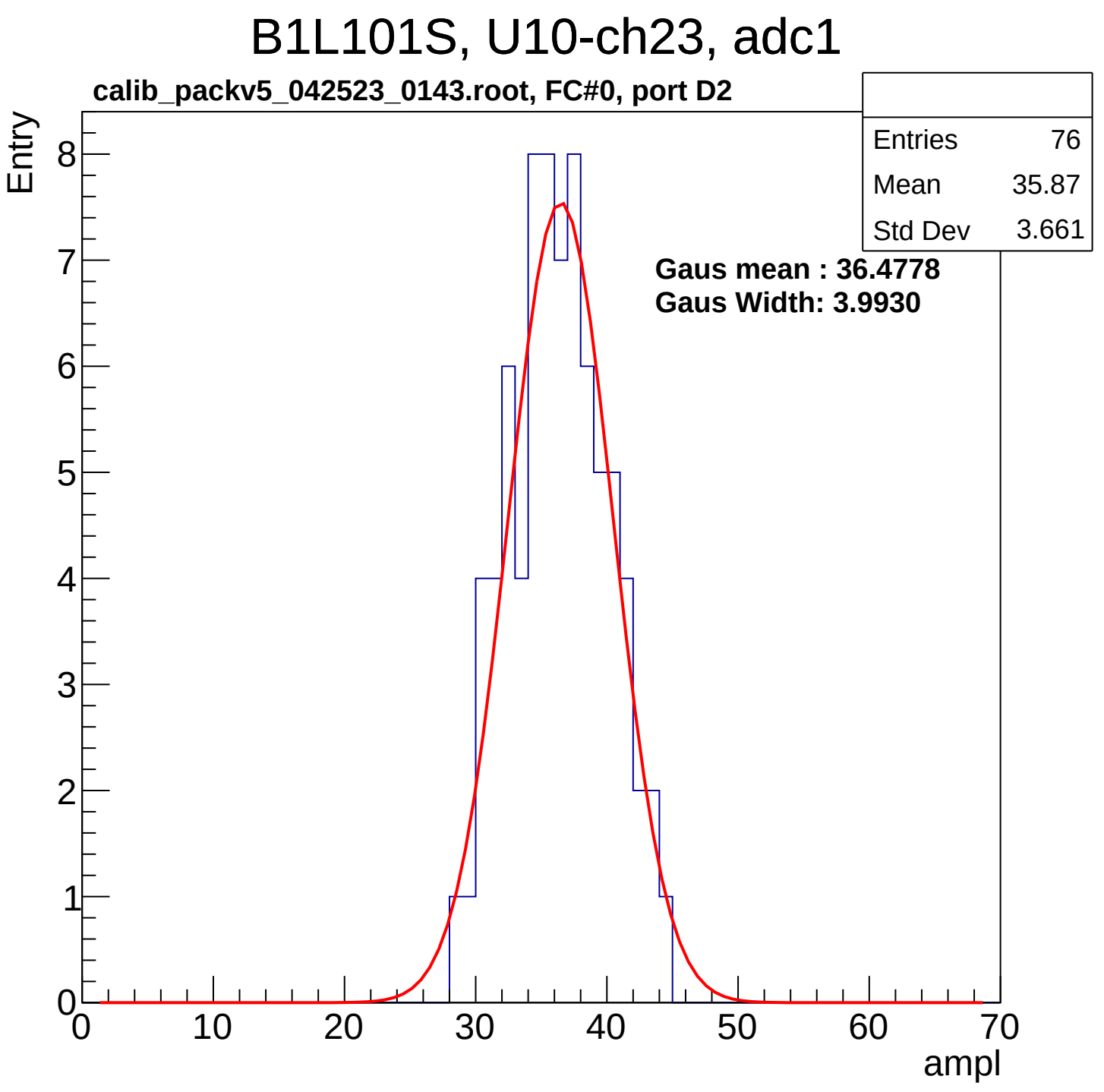
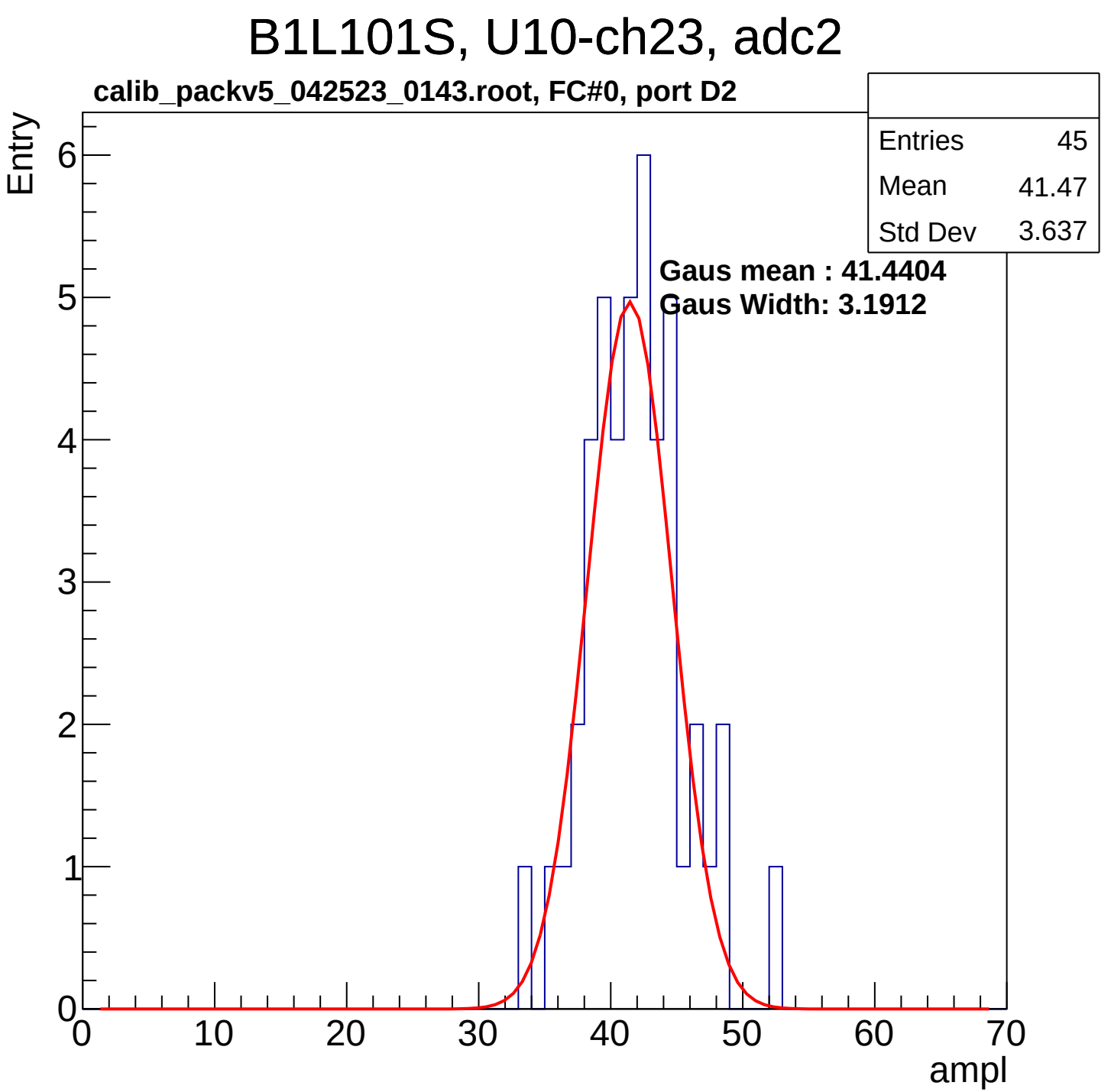
40
50
60
70


B1L101S, U10-ch23, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 29.12
Std Dev 3.263
Gaus mean : 29.1830
Gaus Width: 3.8292
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U10-ch23, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 35.87
Std Dev 3.661
Gaus mean : 36.4778
Gaus Width: 3.9930
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch23, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 41.47
Std Dev 3.637
Gaus mean : 41.4404
Gaus Width: 3.1912
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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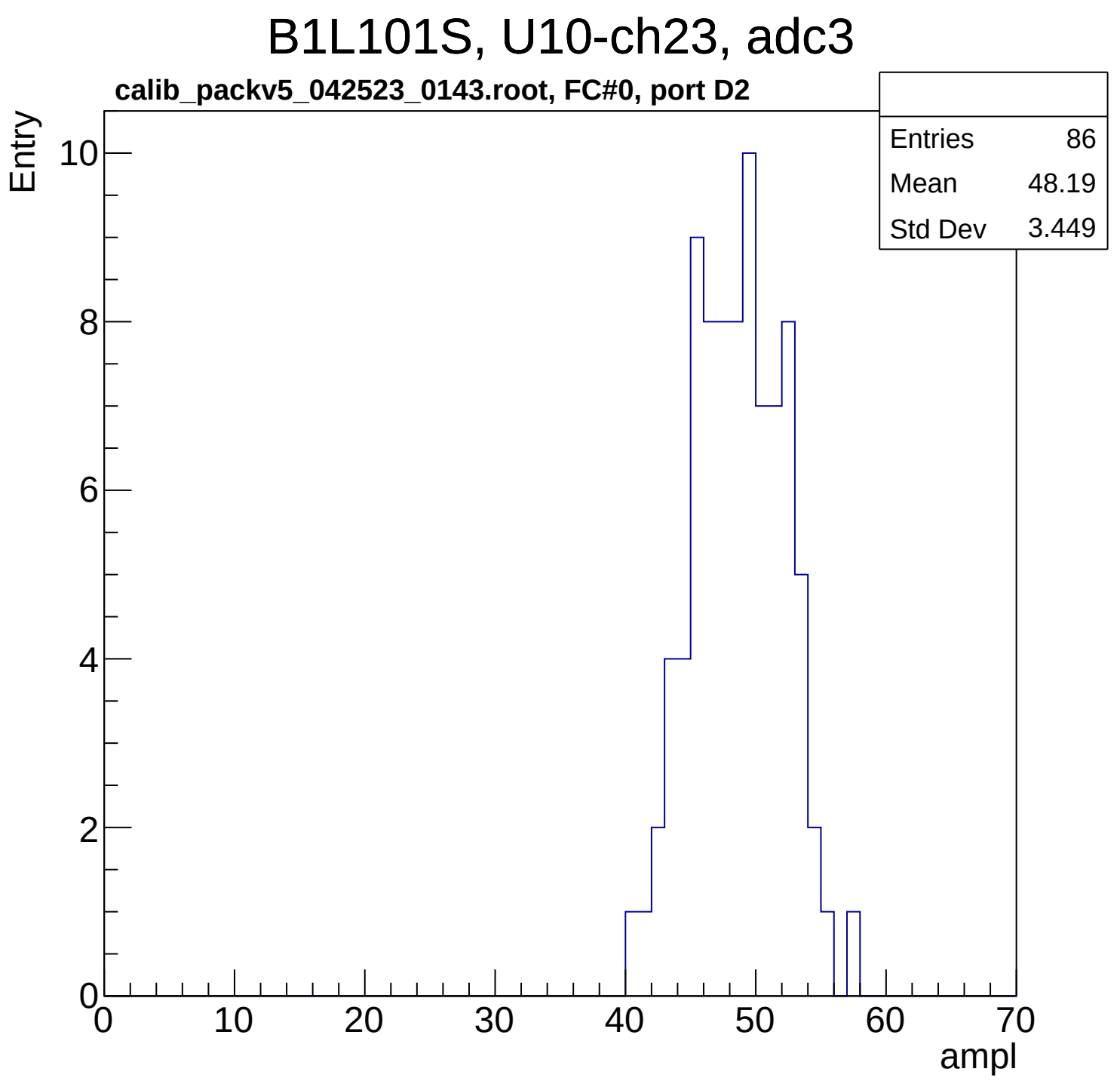
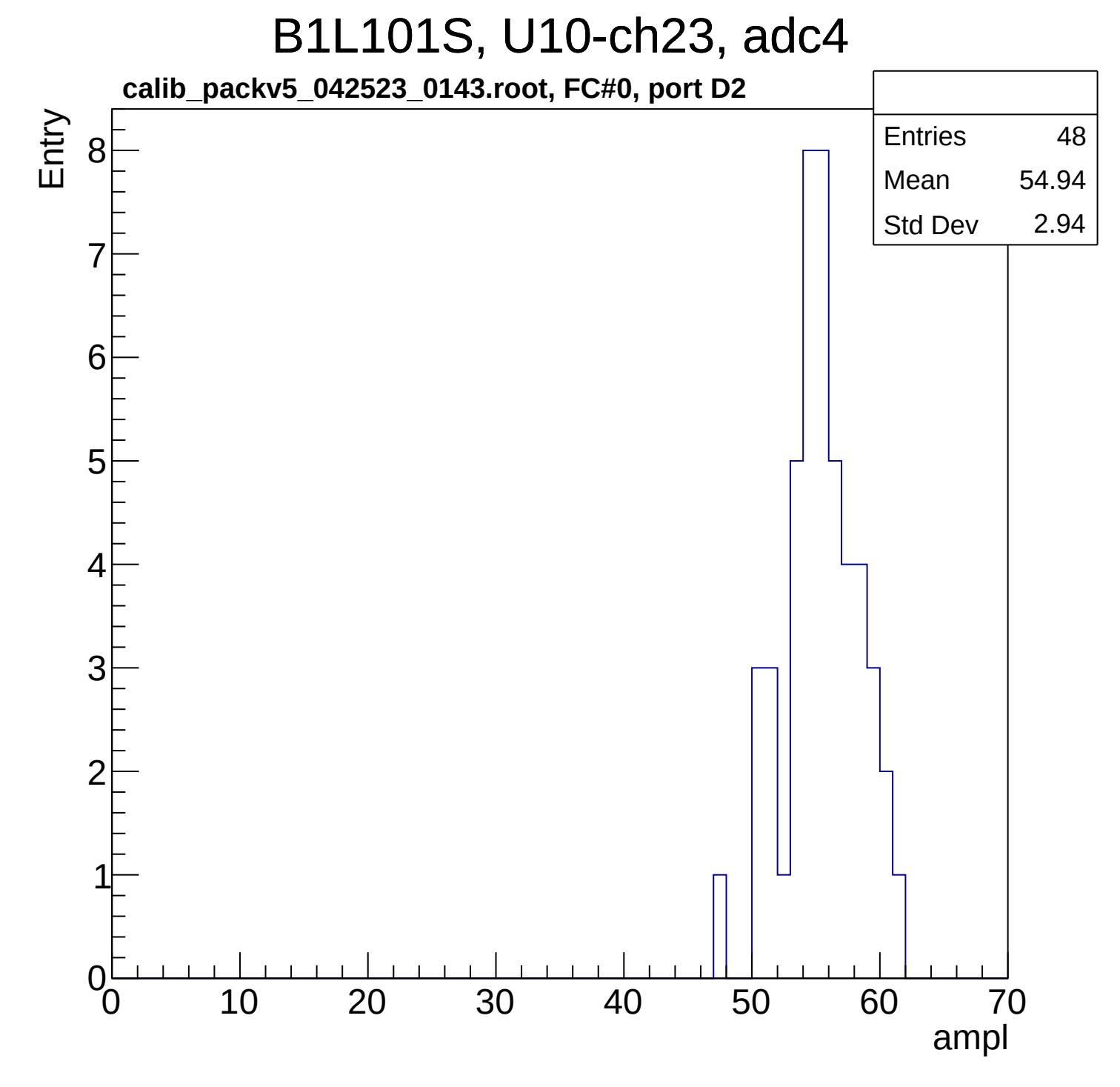
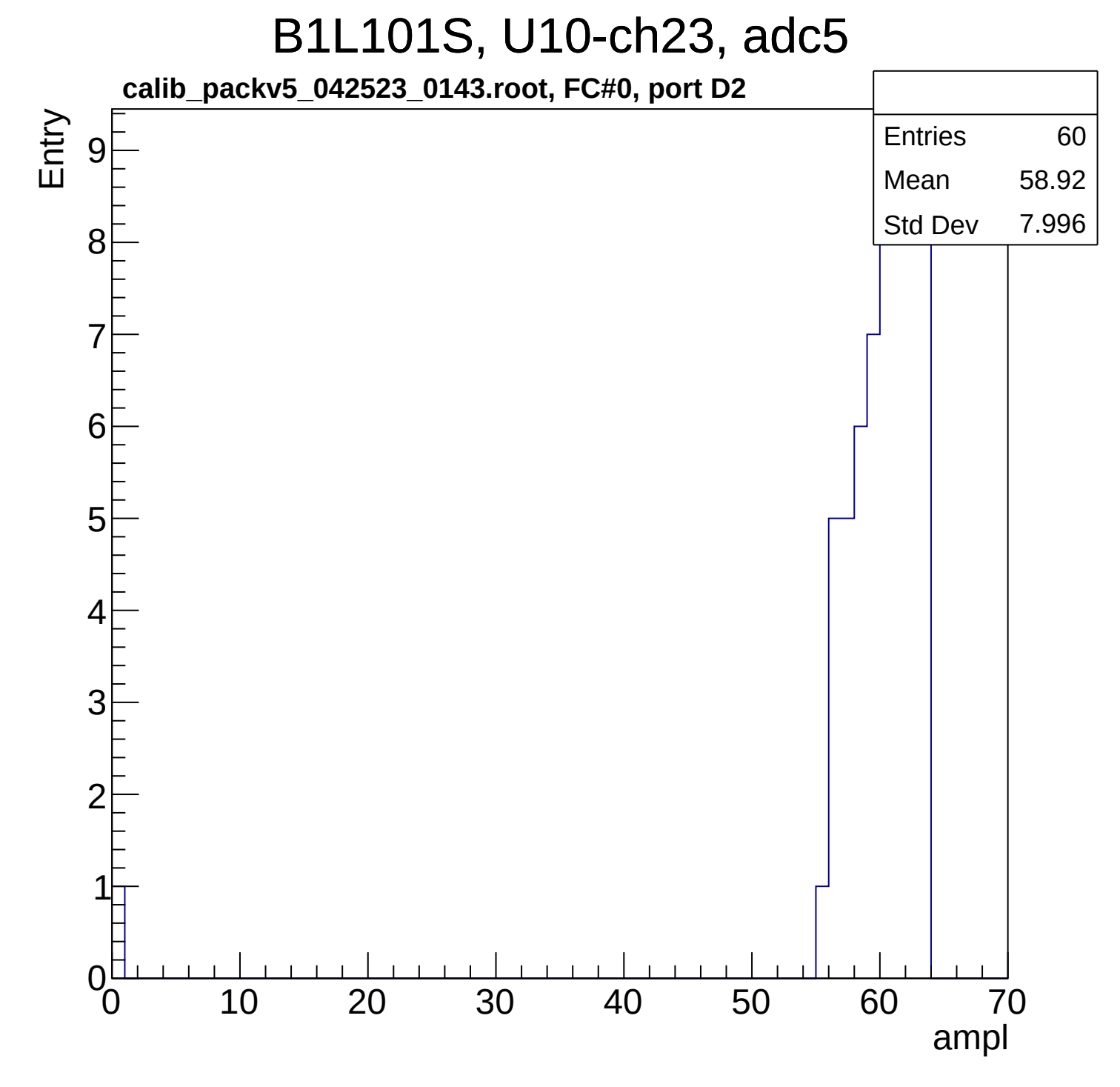
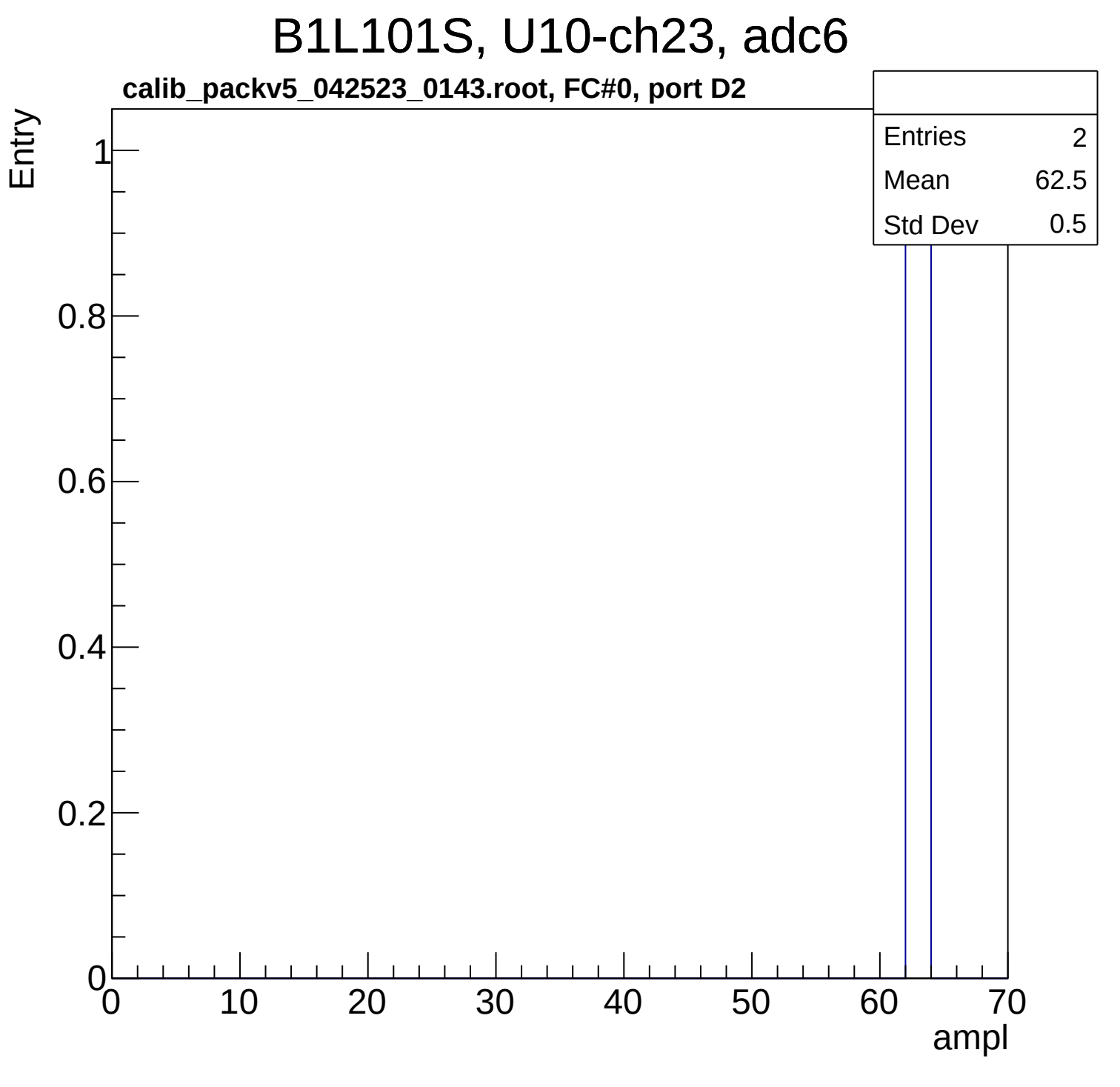
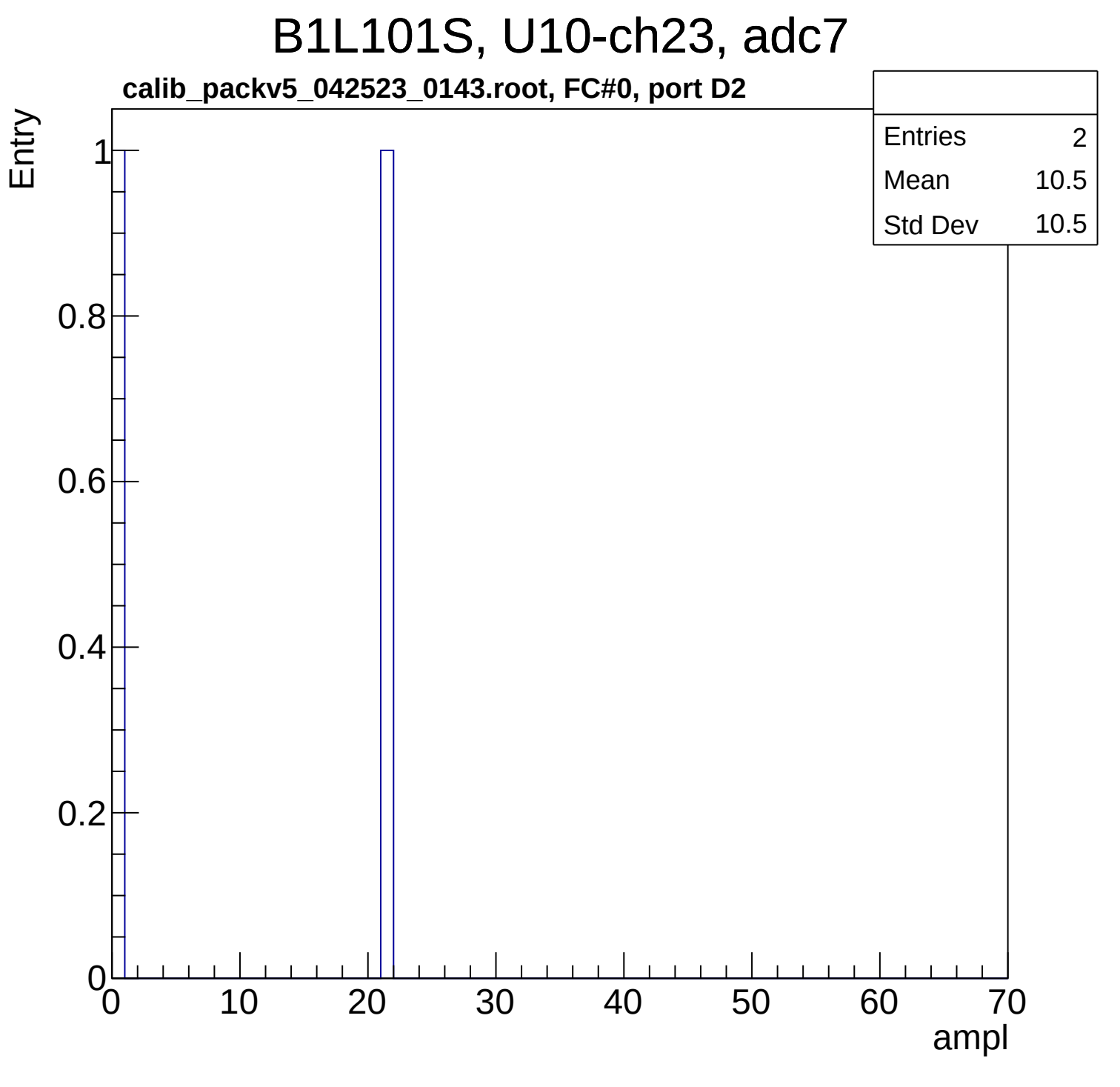
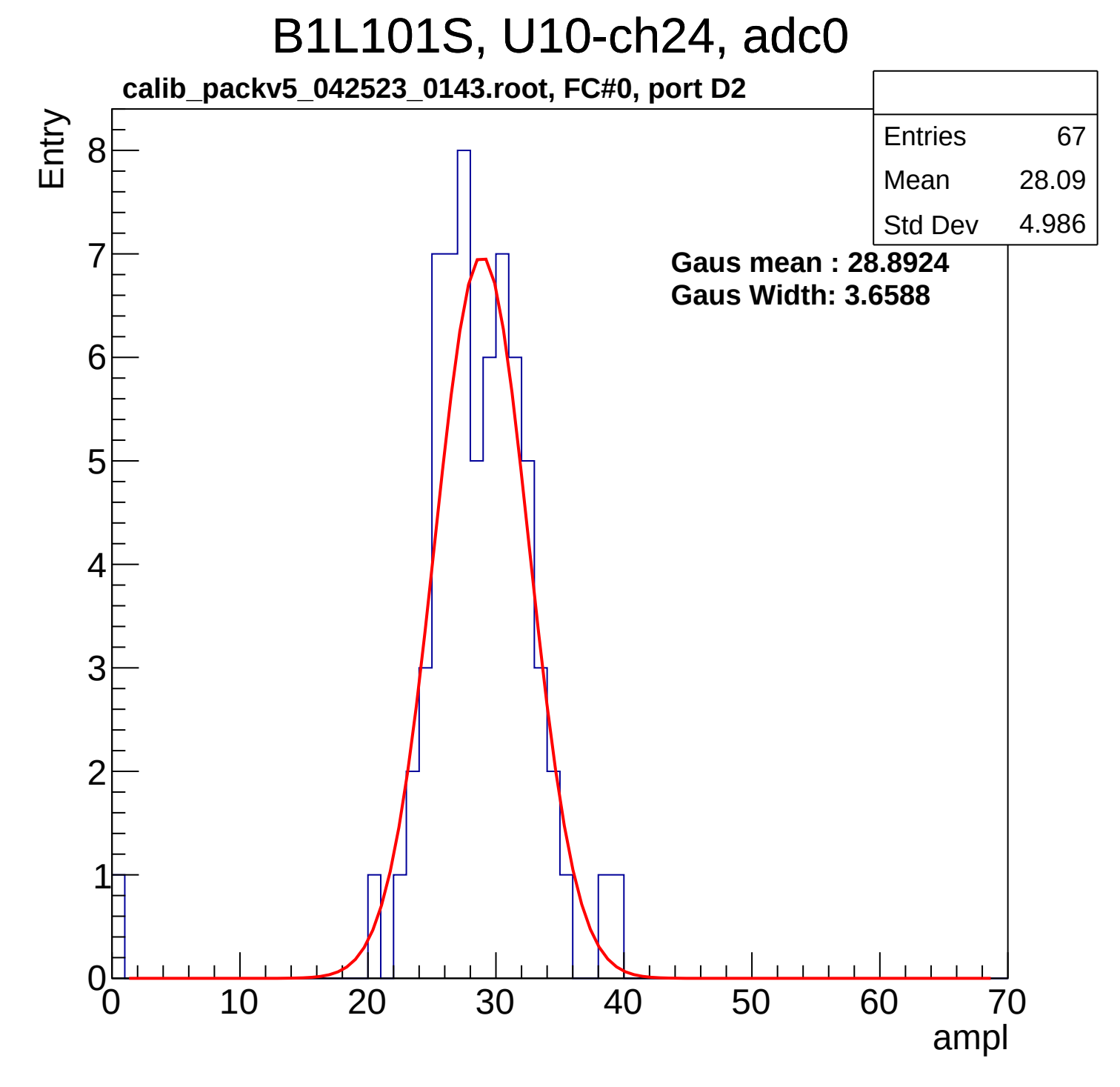

B1L101S, U10-ch23, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 86
Mean 48.19
Std Dev 3.449
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

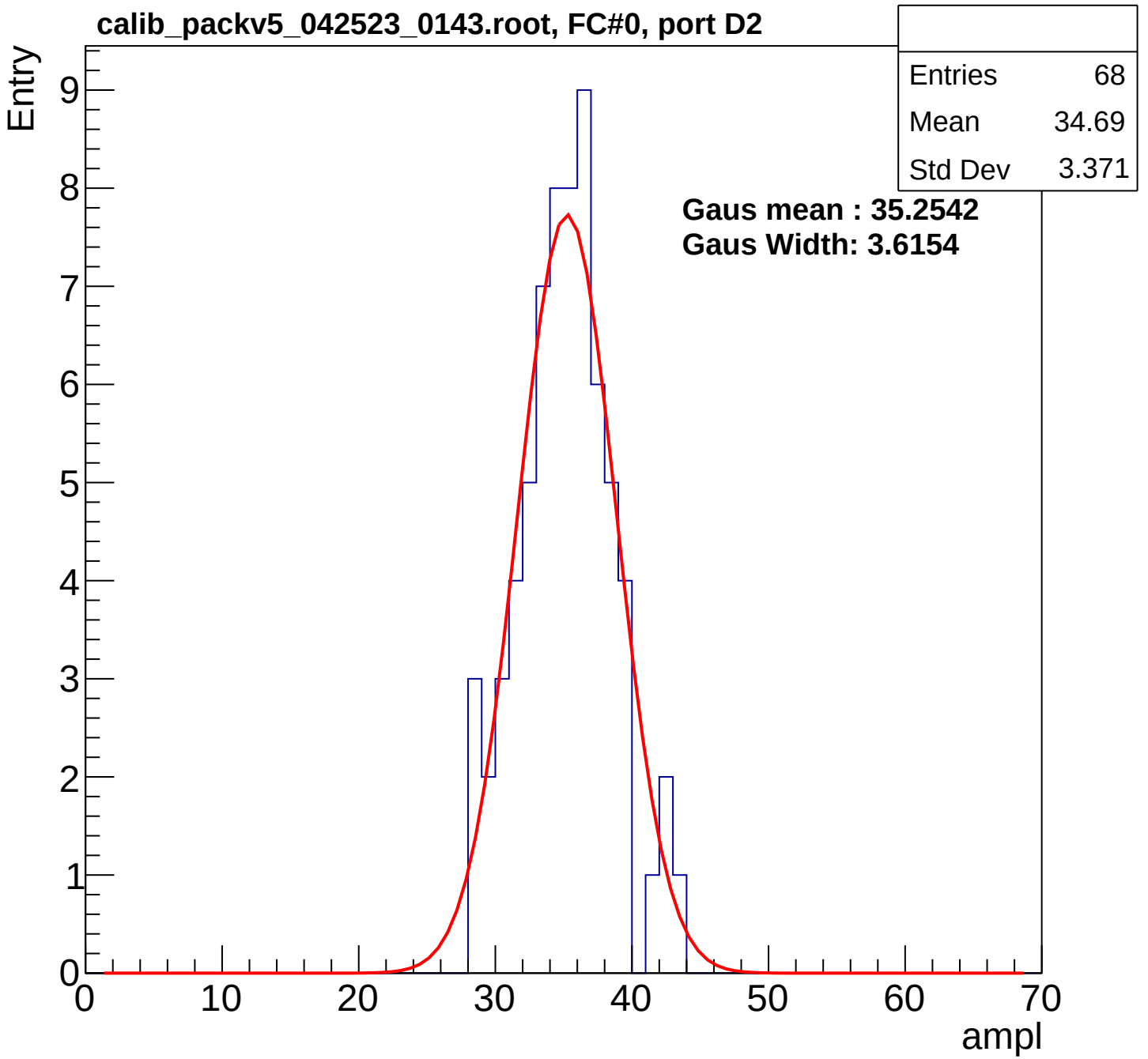

B1L101S, U10-ch23, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 54.94
Std Dev 2.94
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

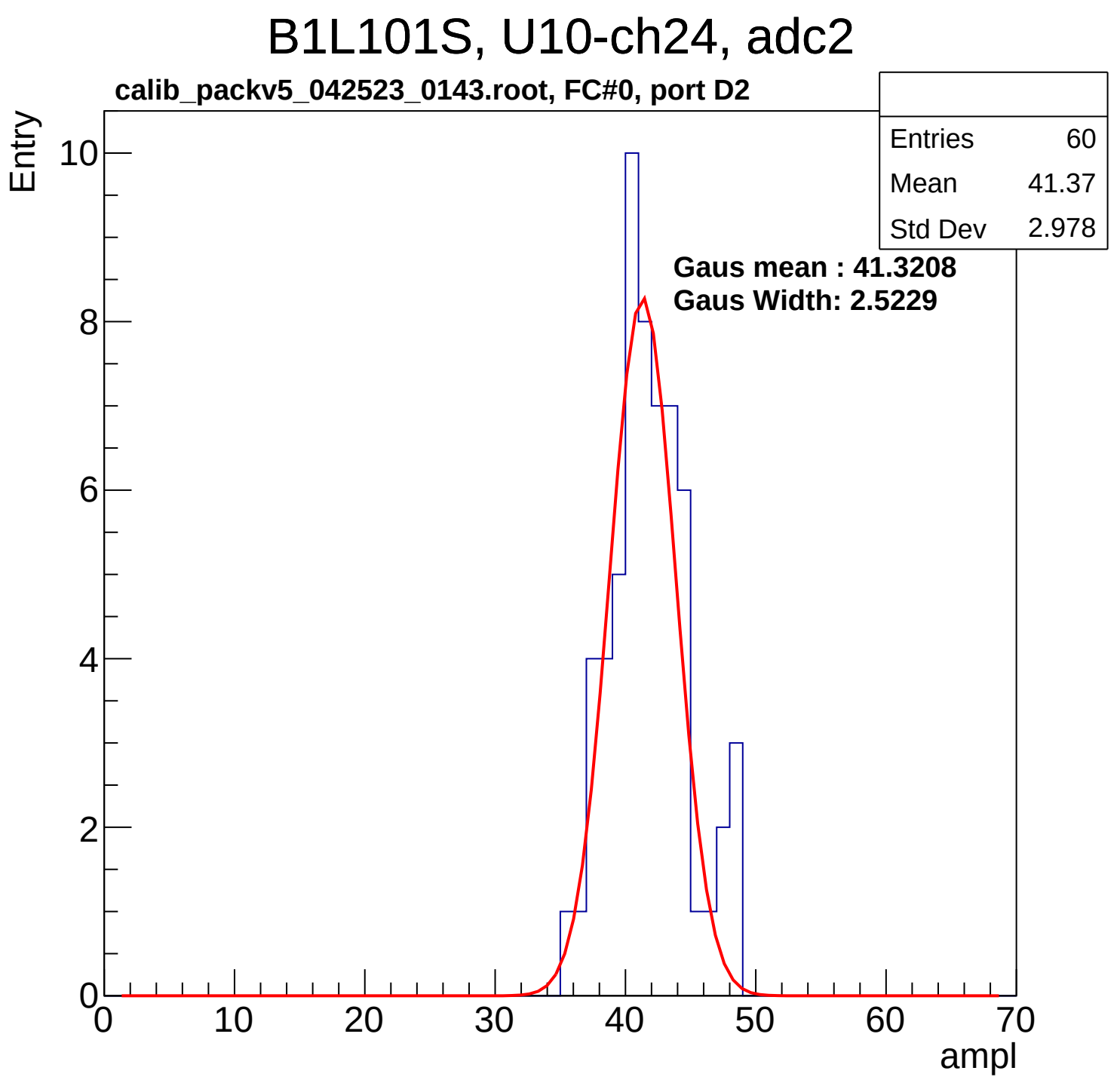

B1L101S, U10-ch23, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 58.92
Std Dev 7.996
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

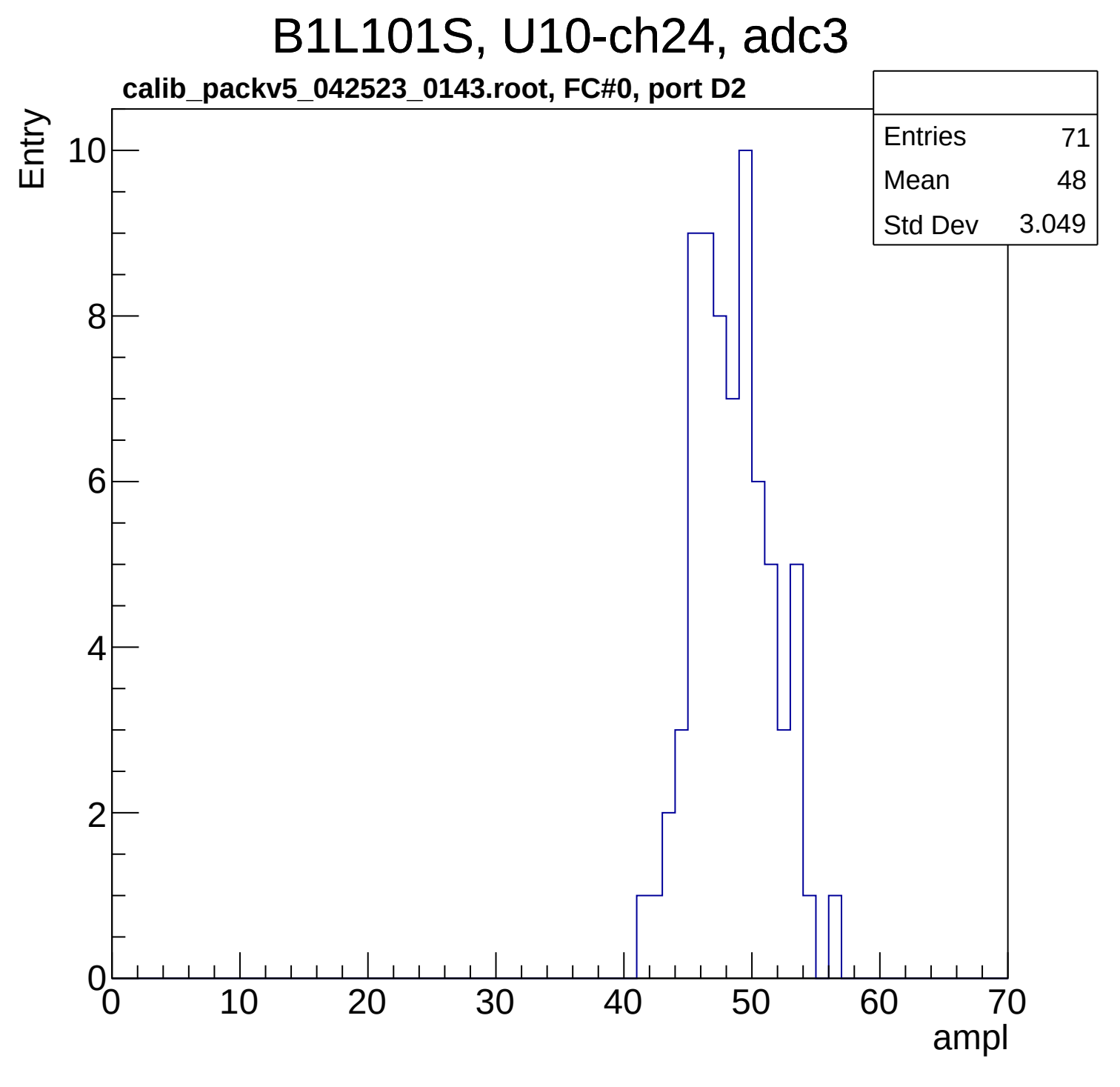

B1L101S, U10-ch23, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

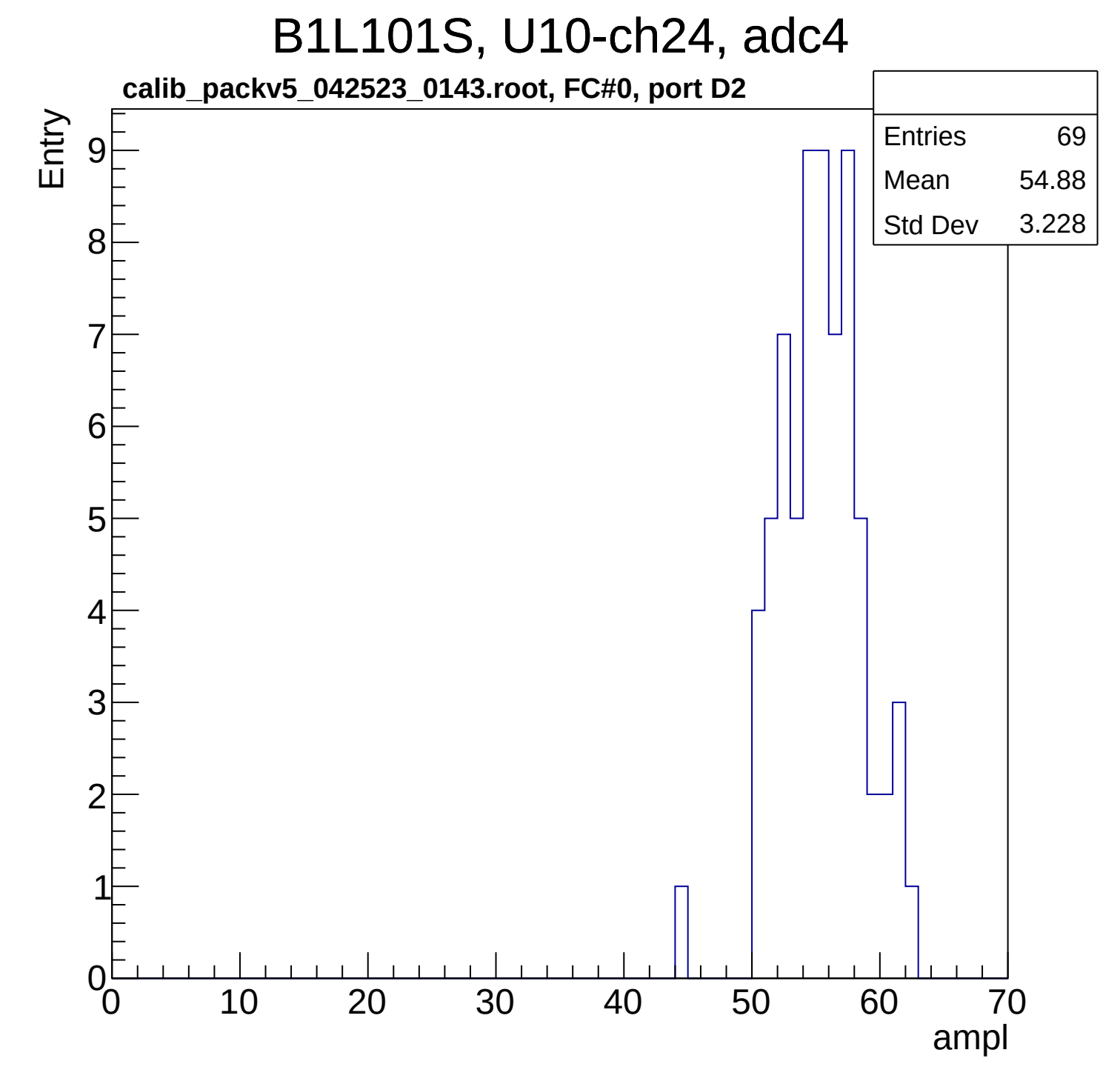

B1L101S, U10-ch23, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 10.5
Std Dev 10.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch24, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 28.09
Std Dev 4.986
Gaus mean : 28.8924
Gaus Width: 3.6588
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch24, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 34.69
Std Dev 3.371
Gaus mean : 35.2542
Gaus Width: 3.6154
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch24, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 41.37
Std Dev 2.978
Gaus mean : 41.3208
Gaus Width: 2.5229
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch24, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 48
Std Dev 3.049
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch24, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 54.88
Std Dev 3.228
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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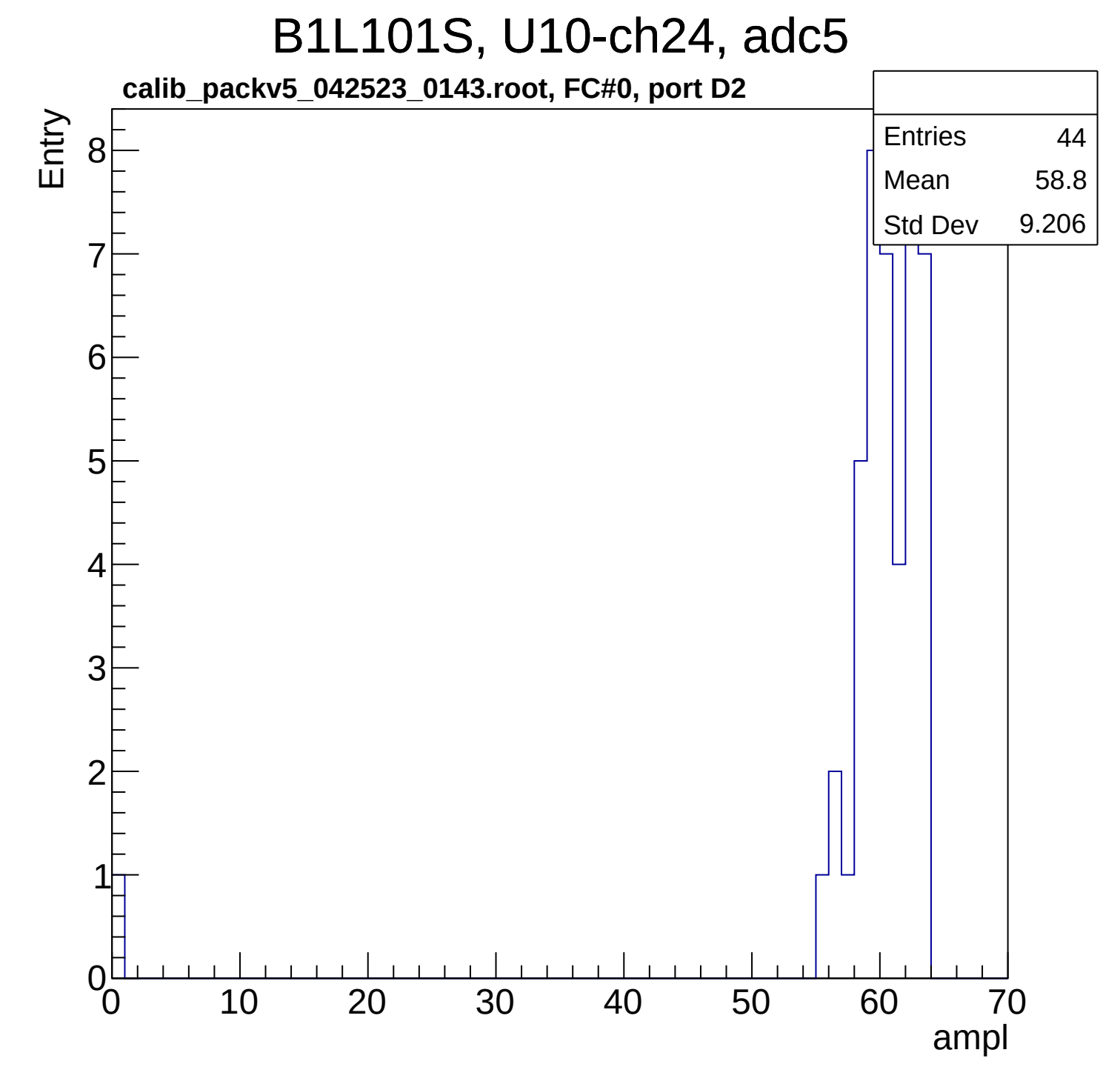
B1L101S, U10-ch24, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 44
Mean 58.8
Std Dev 9.206
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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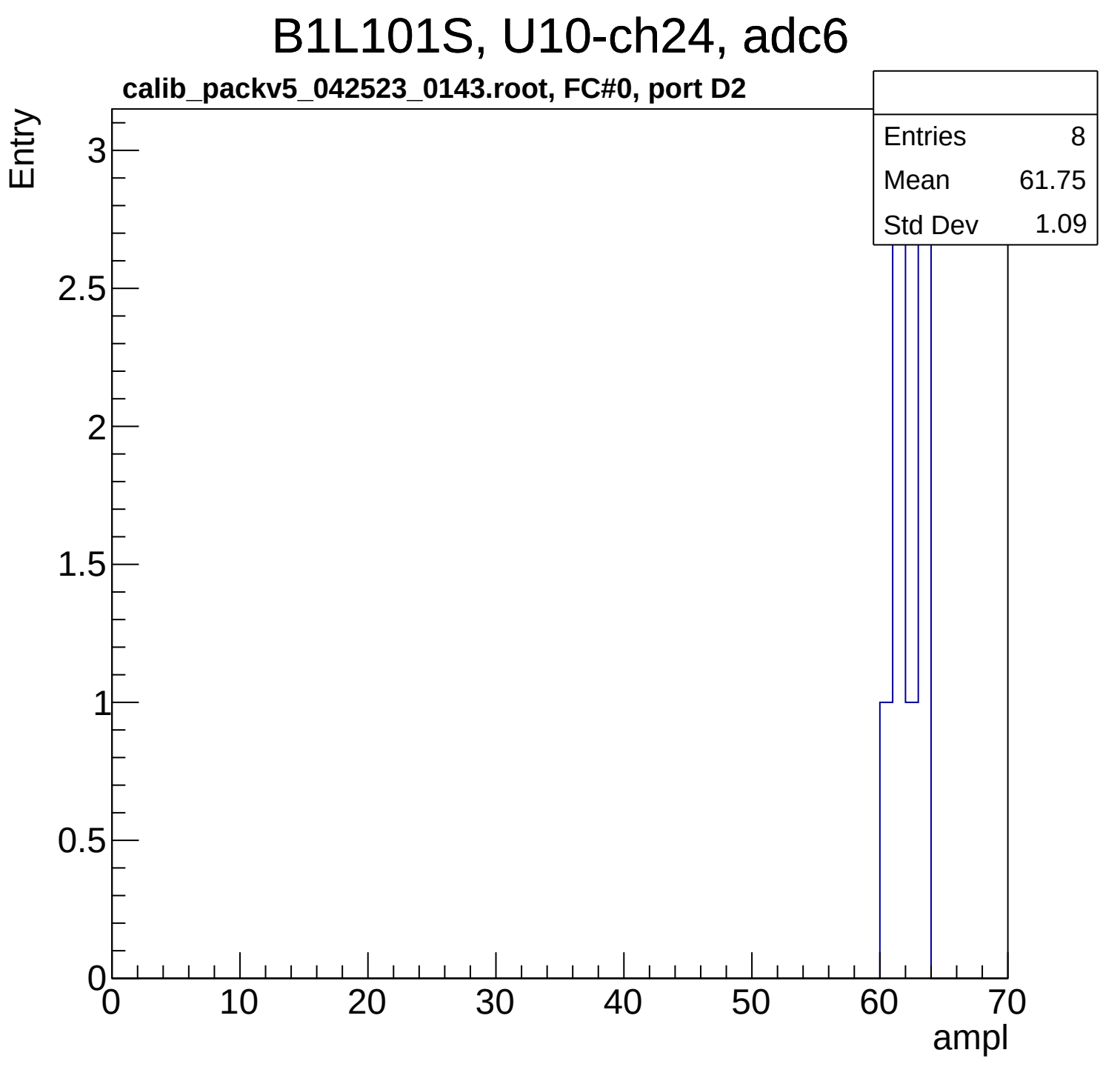
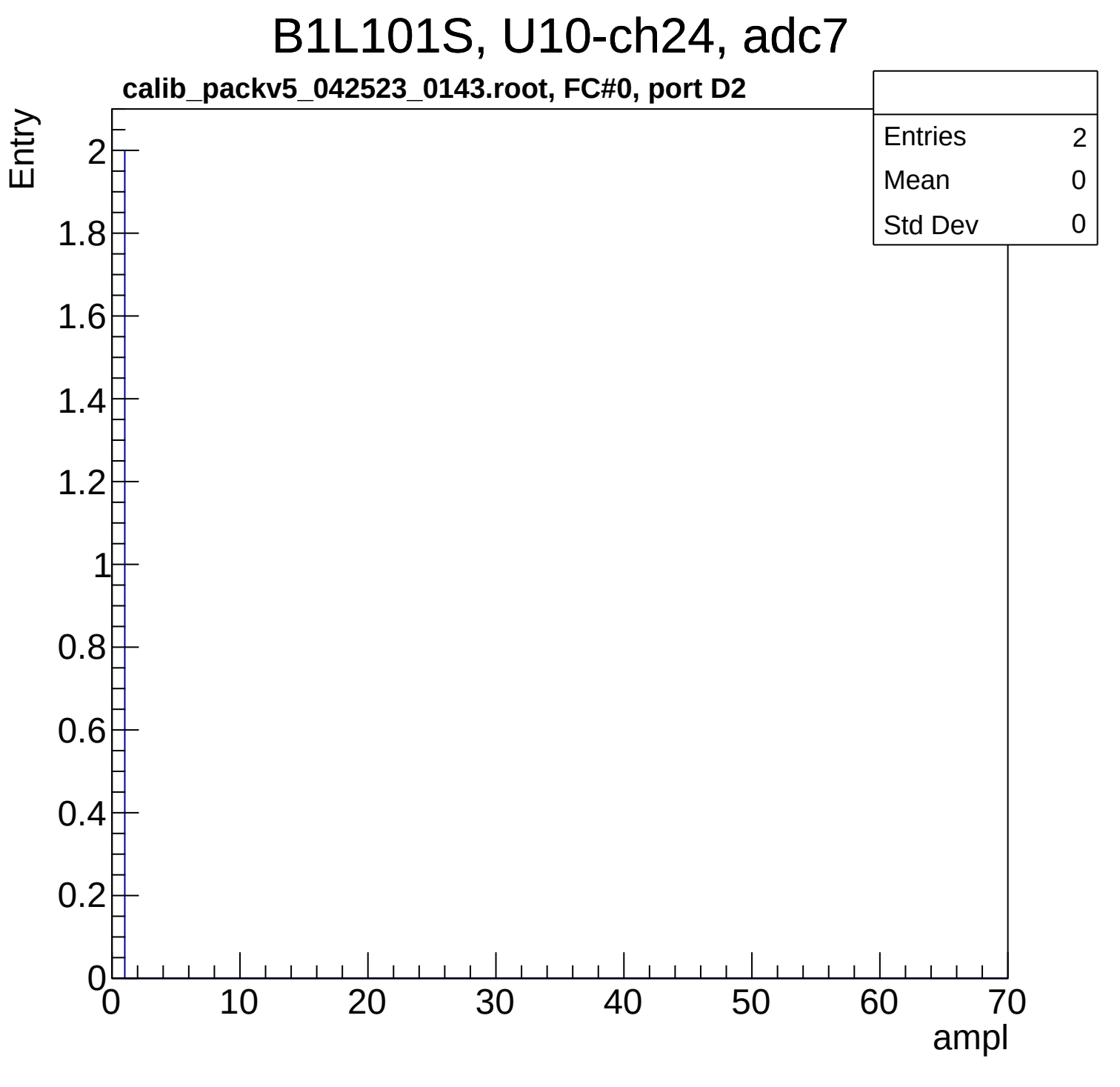
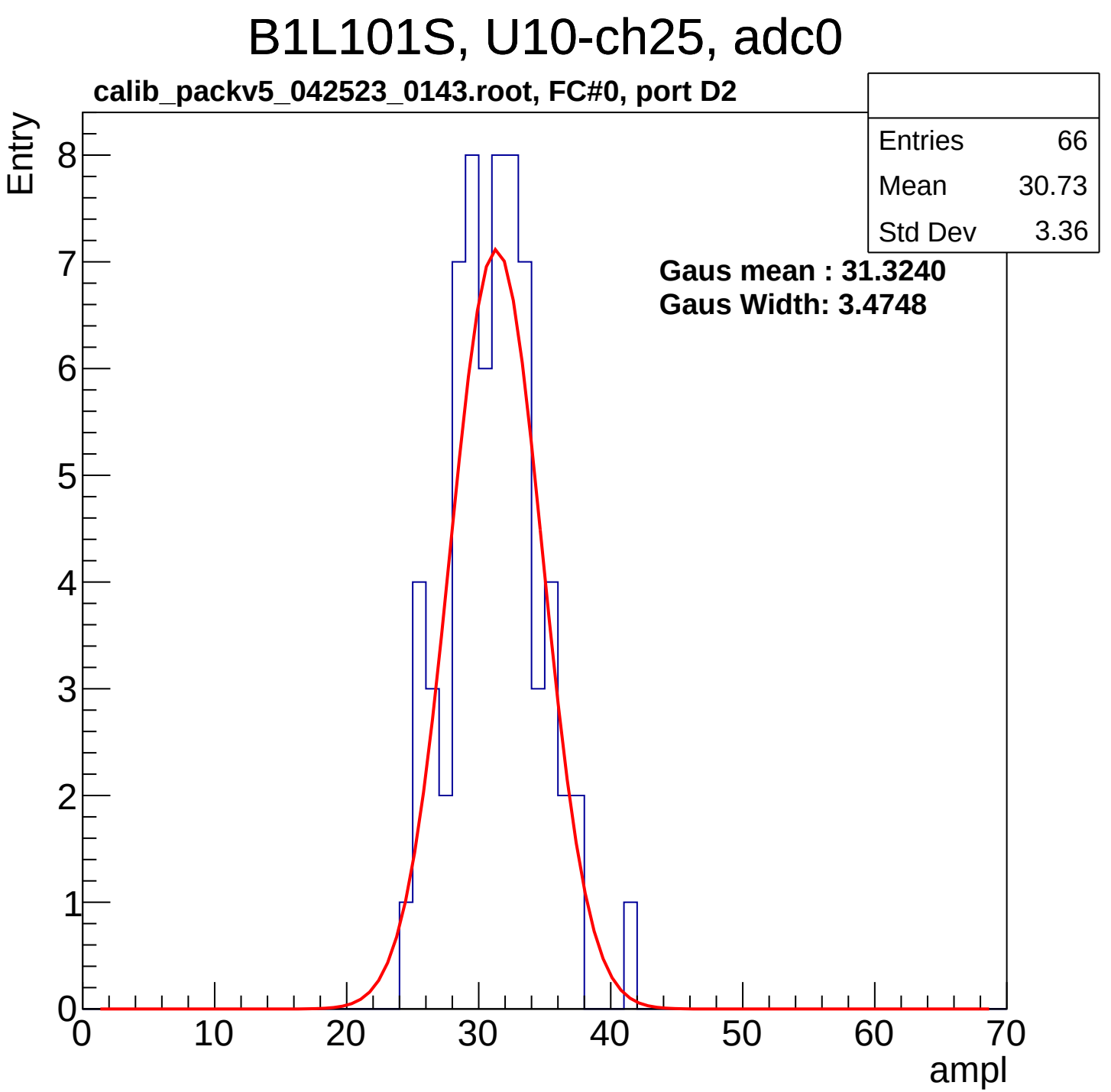
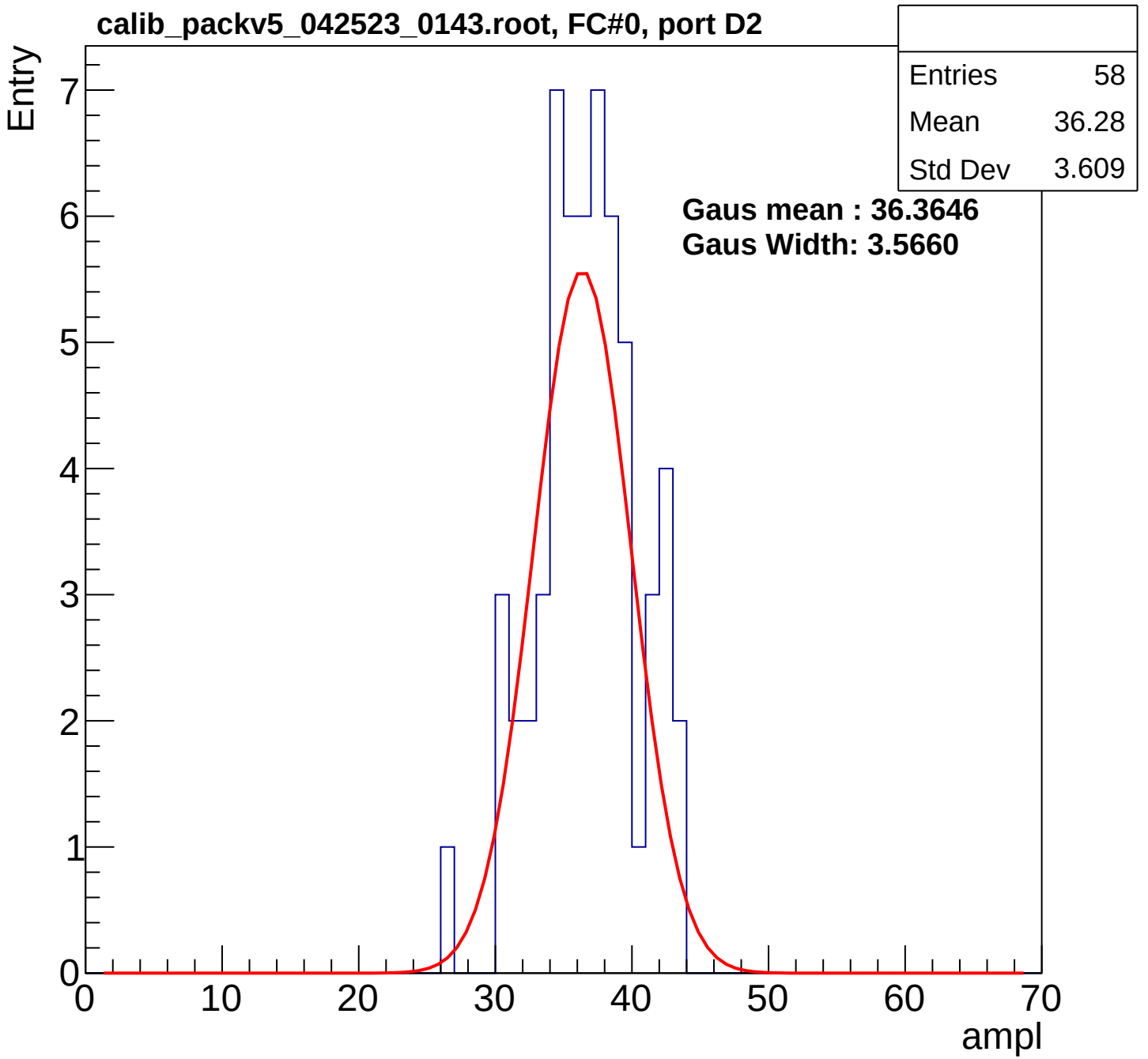
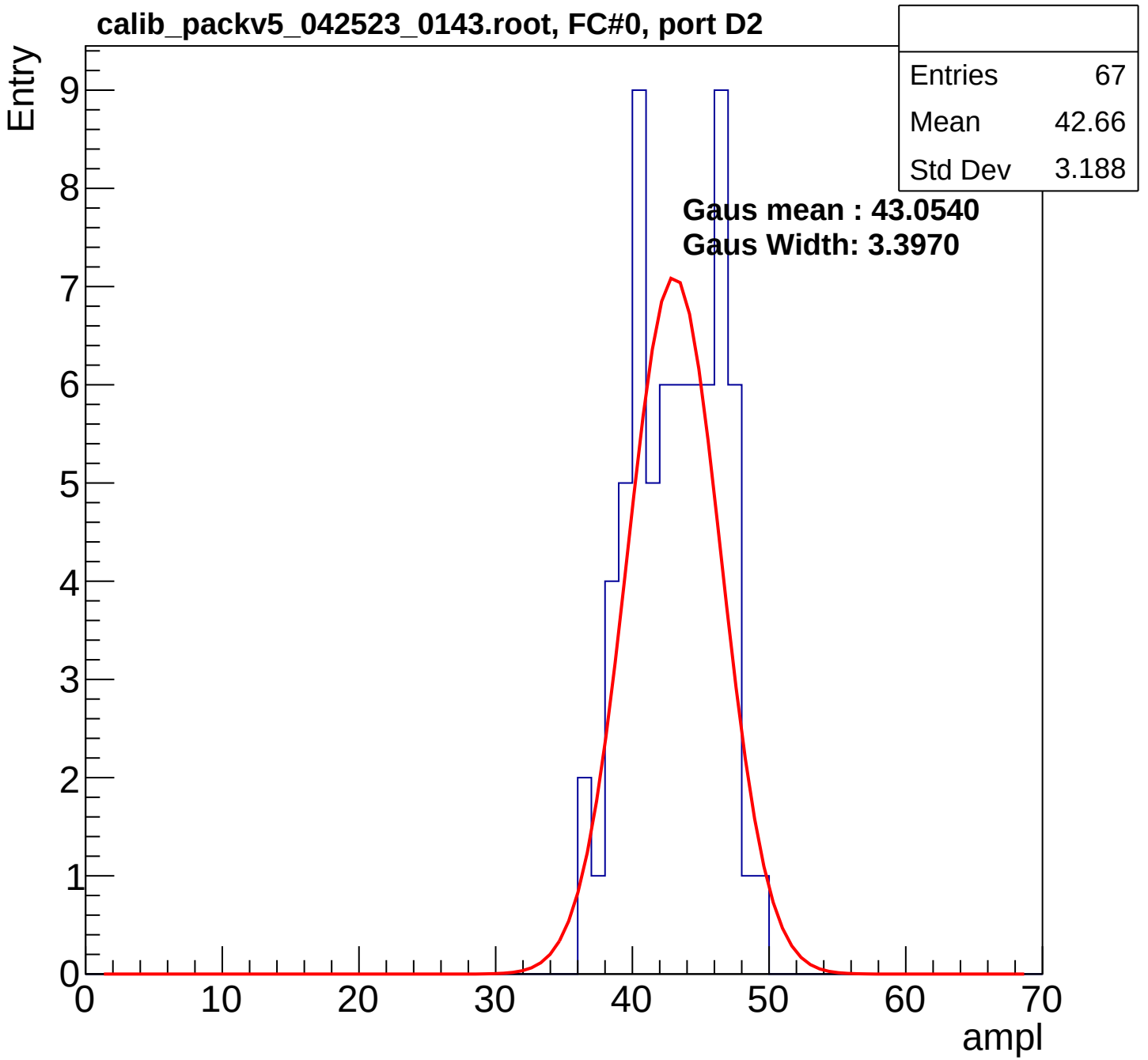
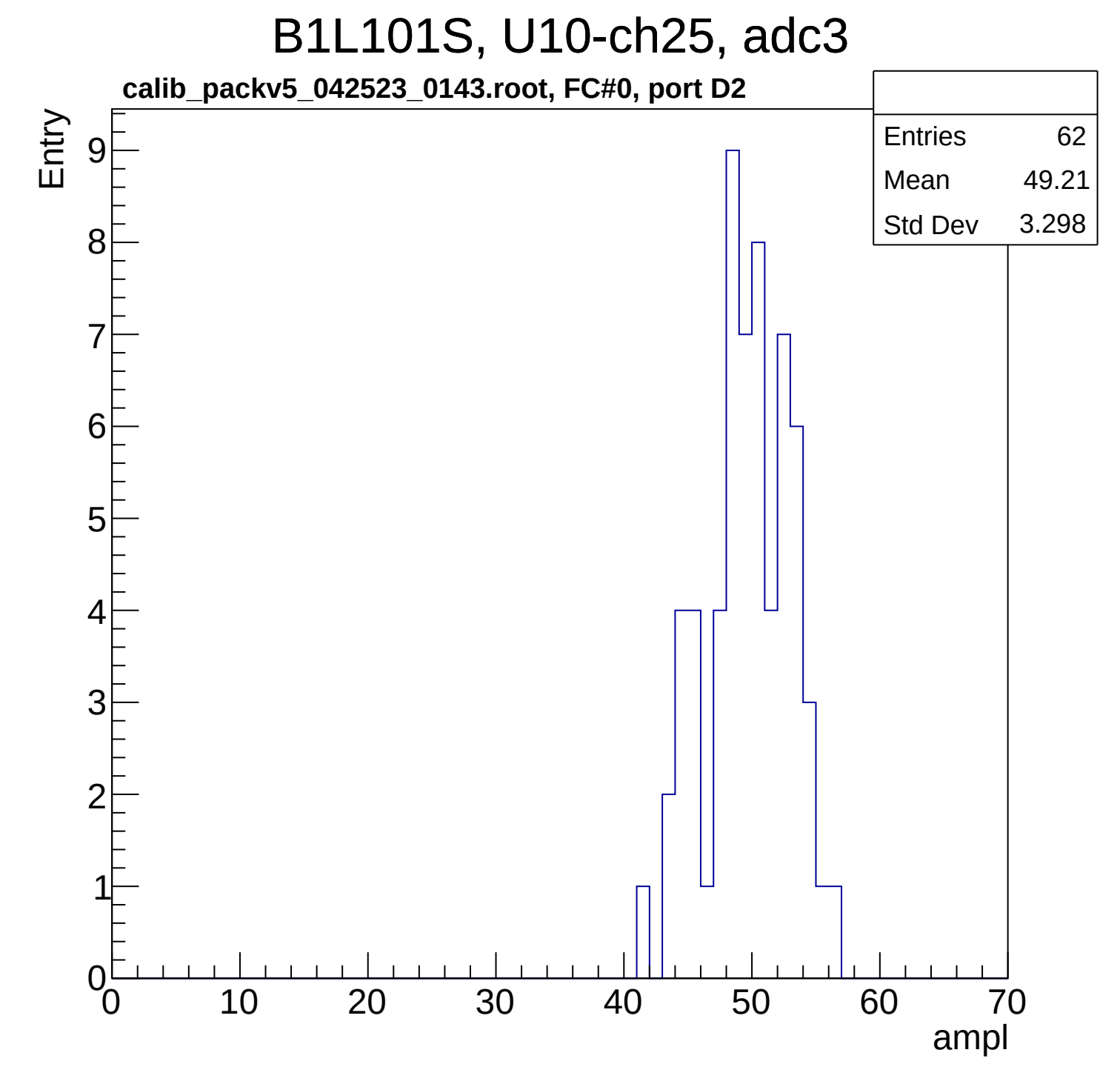

B1L101S, U10-ch24, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 61.75
Std Dev 1.09
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U10-ch24, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch25, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 30.73
Std Dev 3.36
Gaus mean : 31.3240
Gaus Width: 3.4748
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch25, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 36.28
Std Dev 3.609
Gaus mean : 36.3646
Gaus Width: 3.5660
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U10-ch25, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 42.66
Std Dev 3.188
Gaus mean : 43.0540
Gaus Width: 3.3970
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch25, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 49.21
Std Dev 3.298
Entry
ampl
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2
3
4
5
6
7
8
9
0
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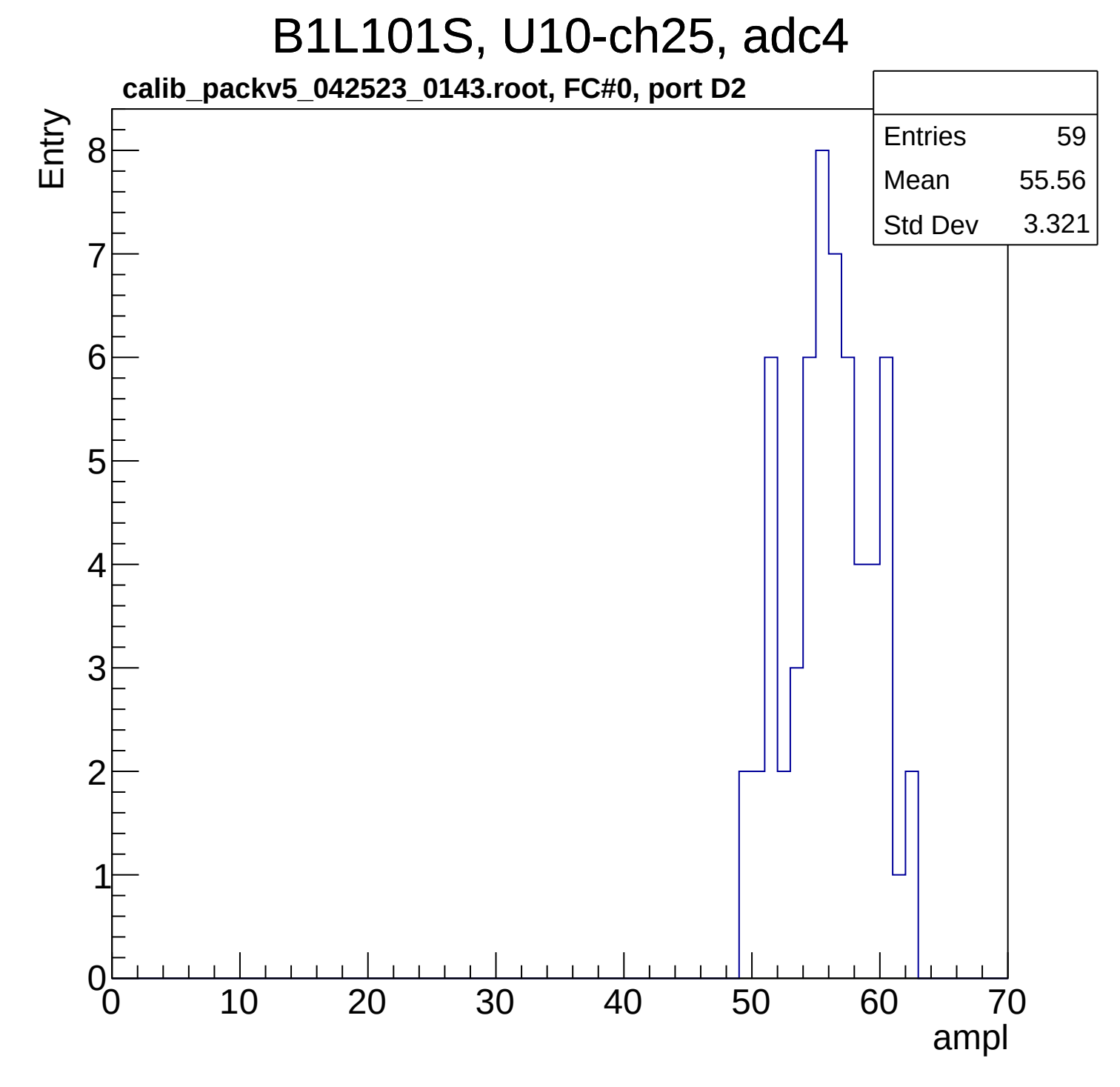
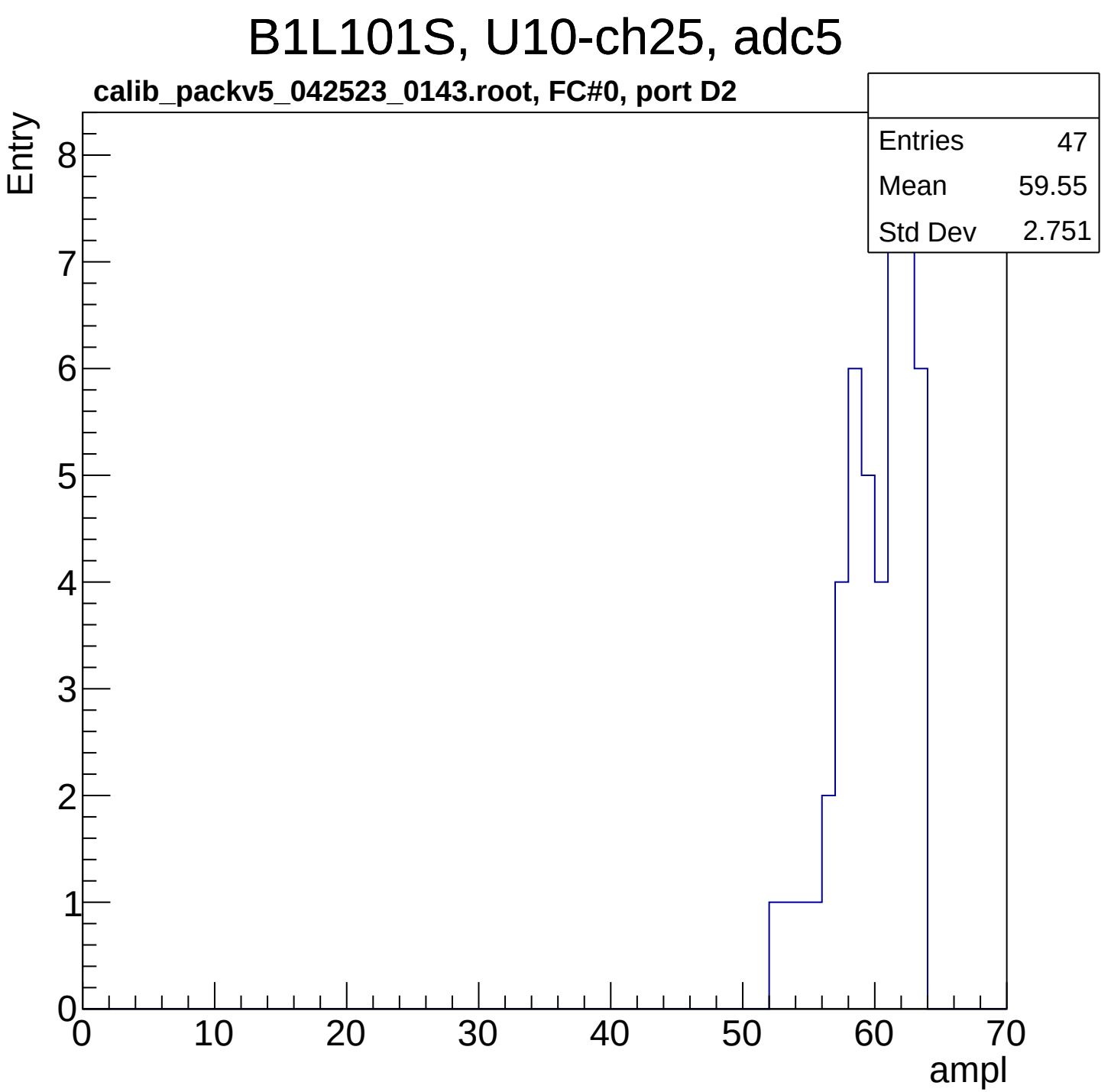
20
30
40
50
60
70


B1L101S, U10-ch25, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 55.56
Std Dev 3.321
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch25, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 59.55
Std Dev 2.751
Entry
ampl
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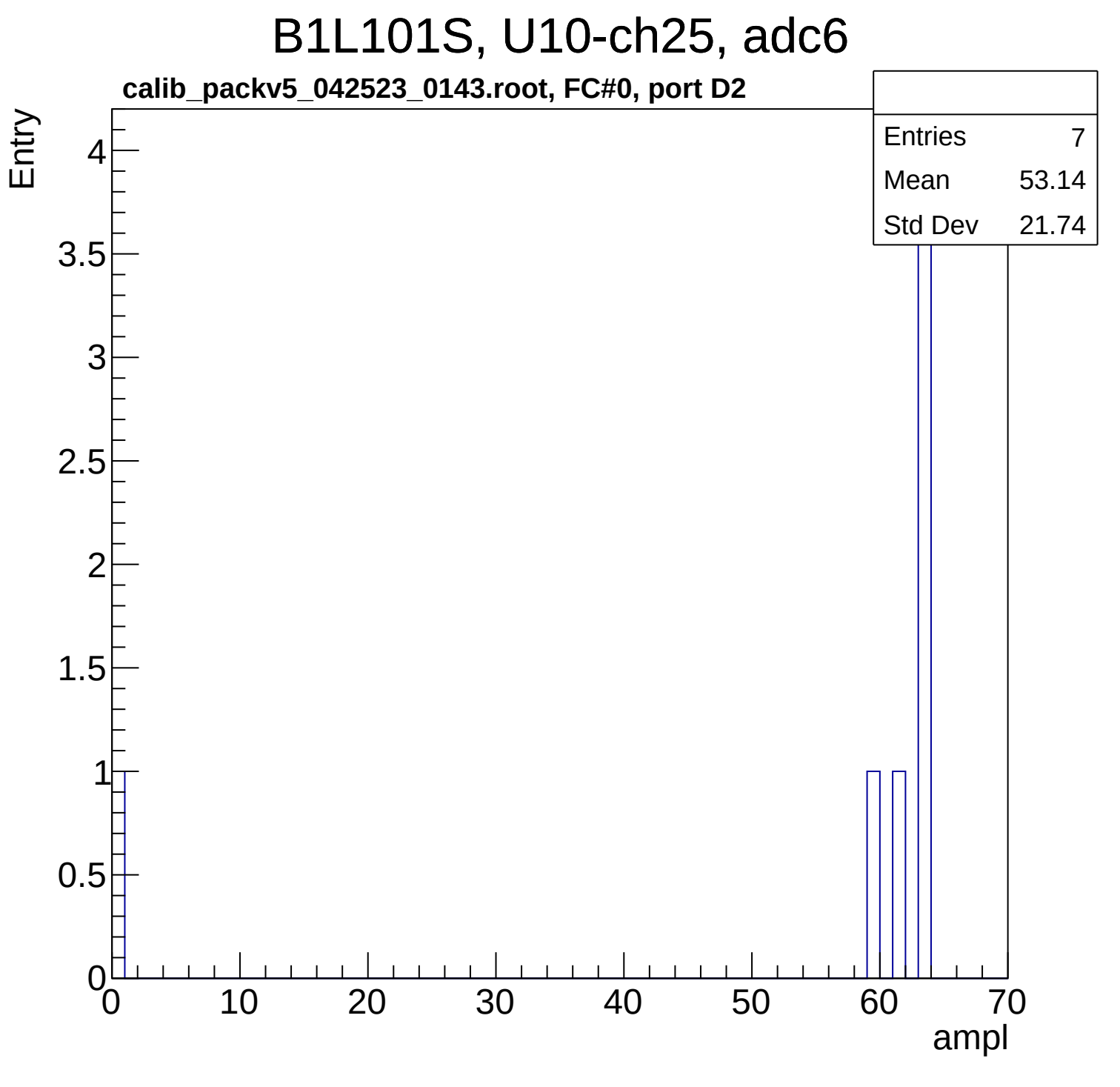
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch25, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 53.14
Std Dev 21.74
Entry
ampl
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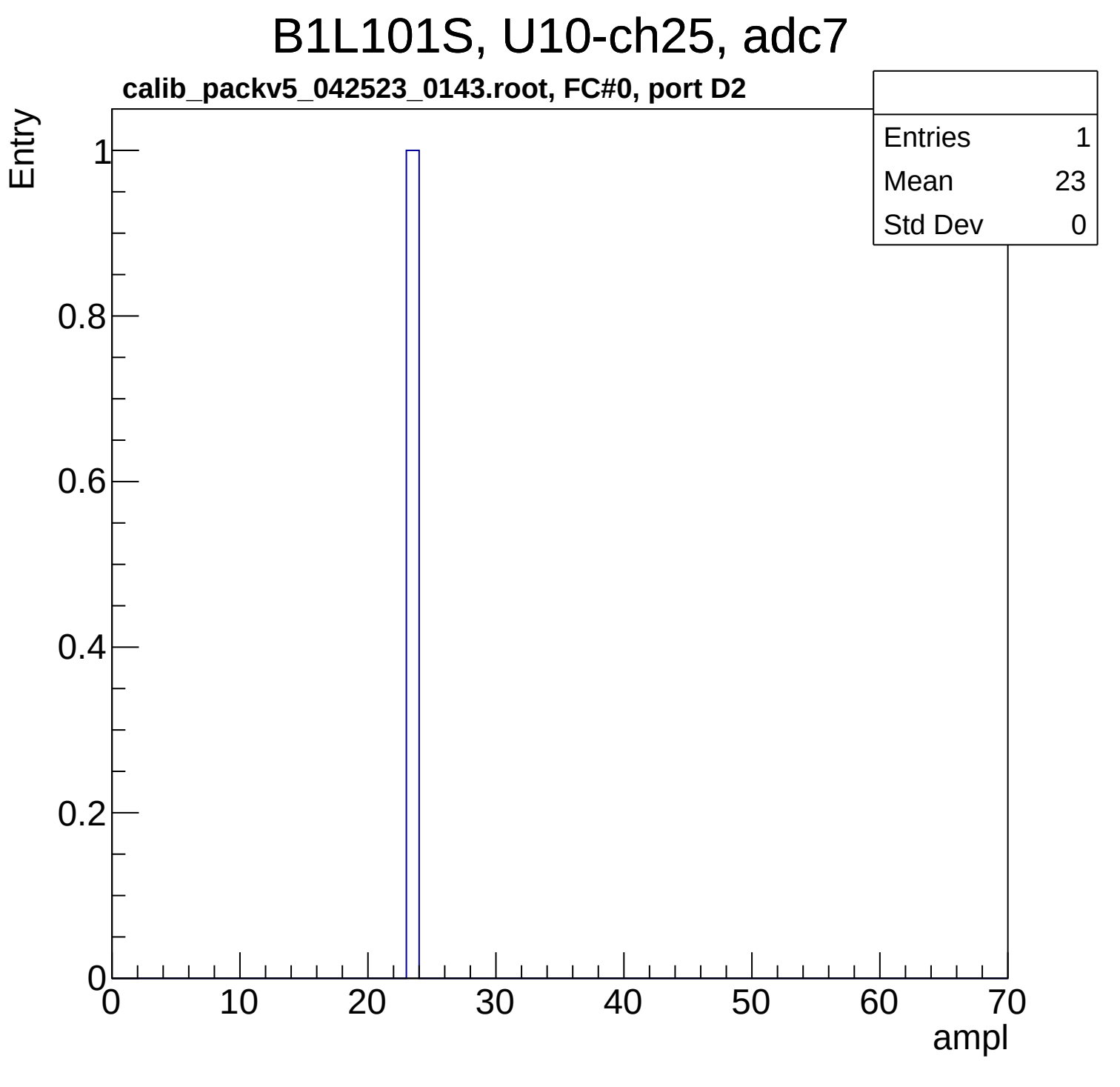
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L101S, U10-ch25, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 23
Std Dev 0
Entry
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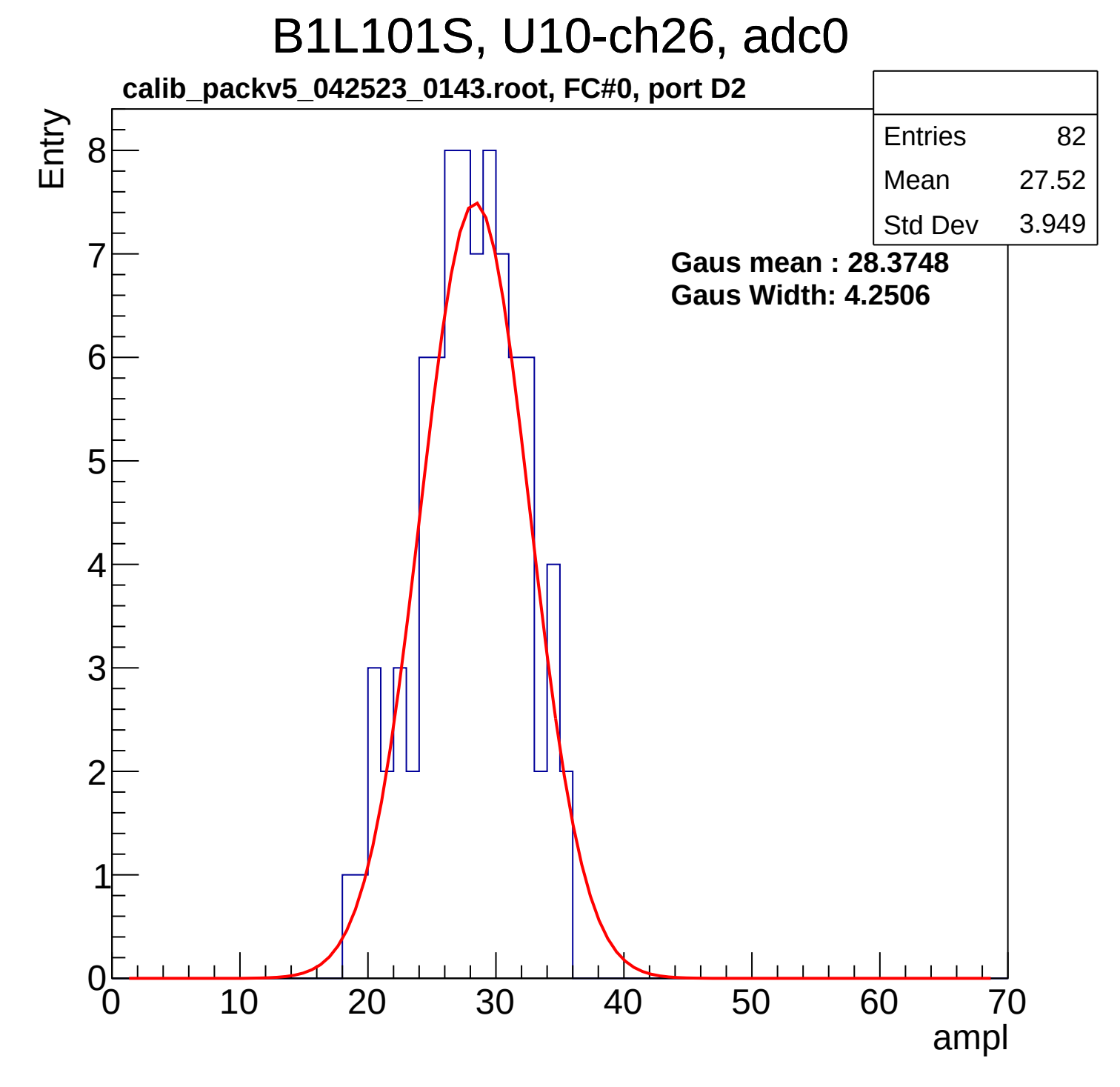
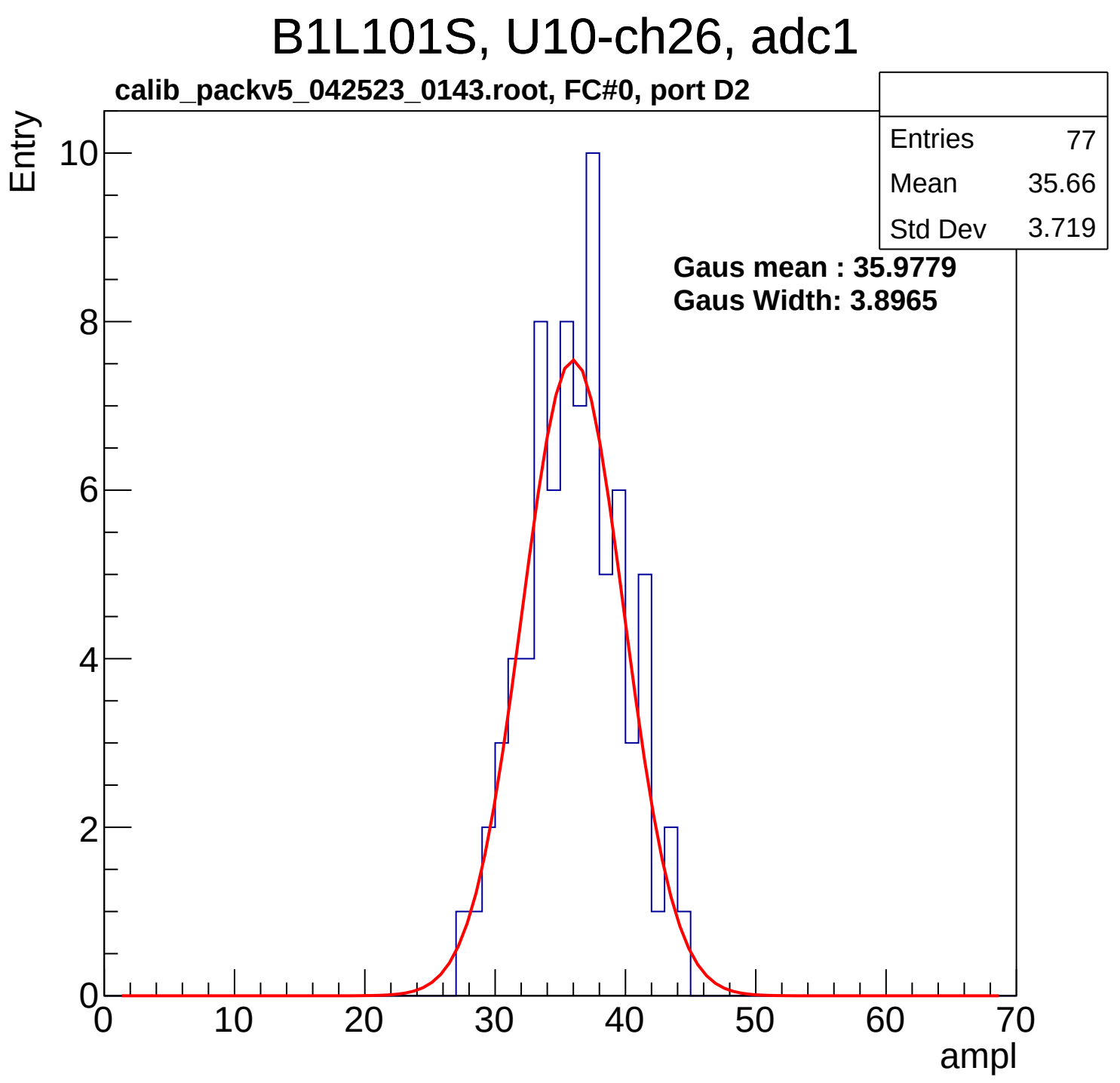
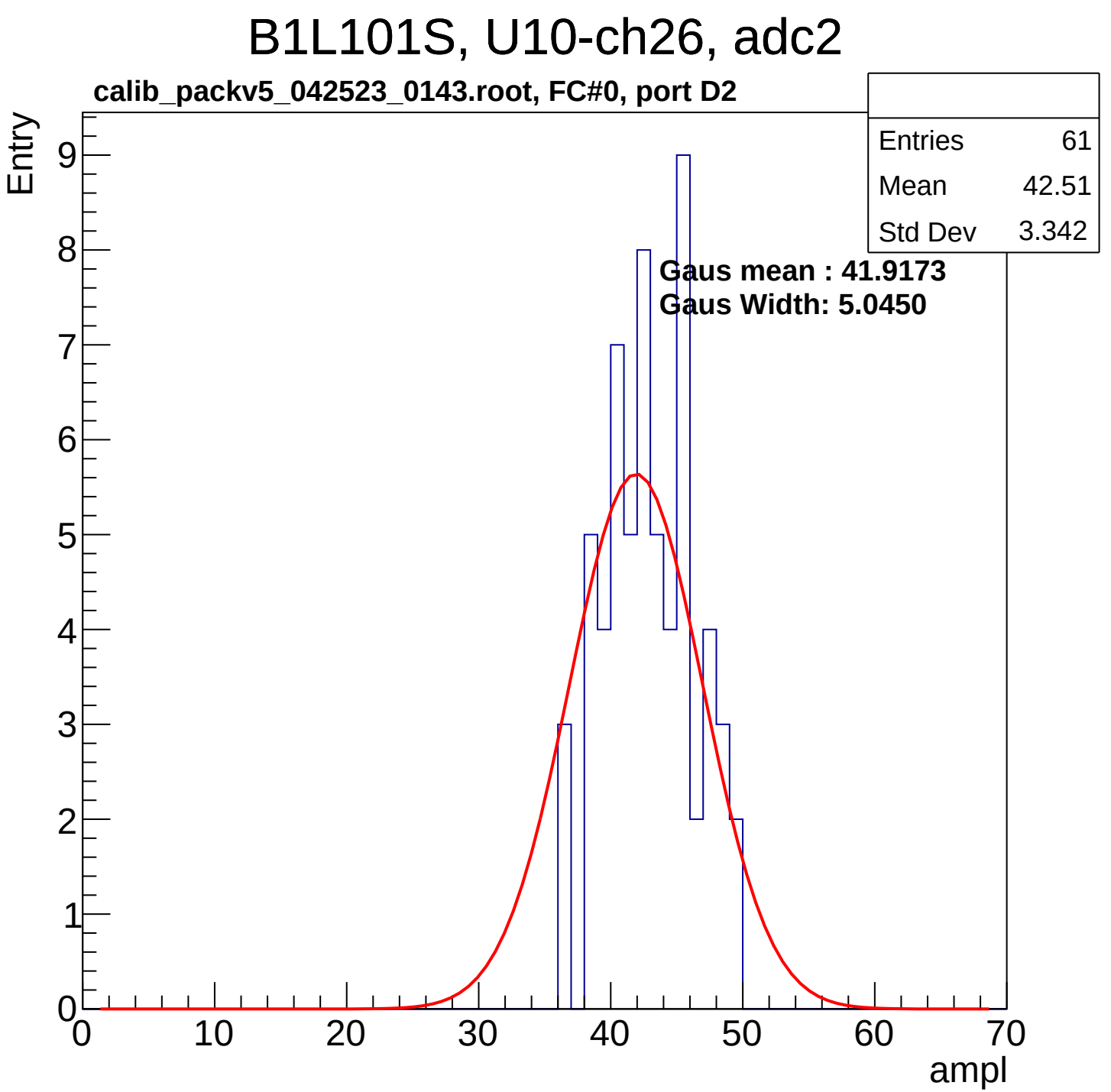
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch26, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 82
Mean 27.52
Std Dev 3.949
Gaus mean : 28.3748
Gaus Width: 4.2506
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch26, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 35.66
Std Dev 3.719
Gaus mean : 35.9779
Gaus Width: 3.8965
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch26, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 42.51
Std Dev 3.342
Gaus mean : 41.9173
Gaus Width: 5.0450
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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40
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60
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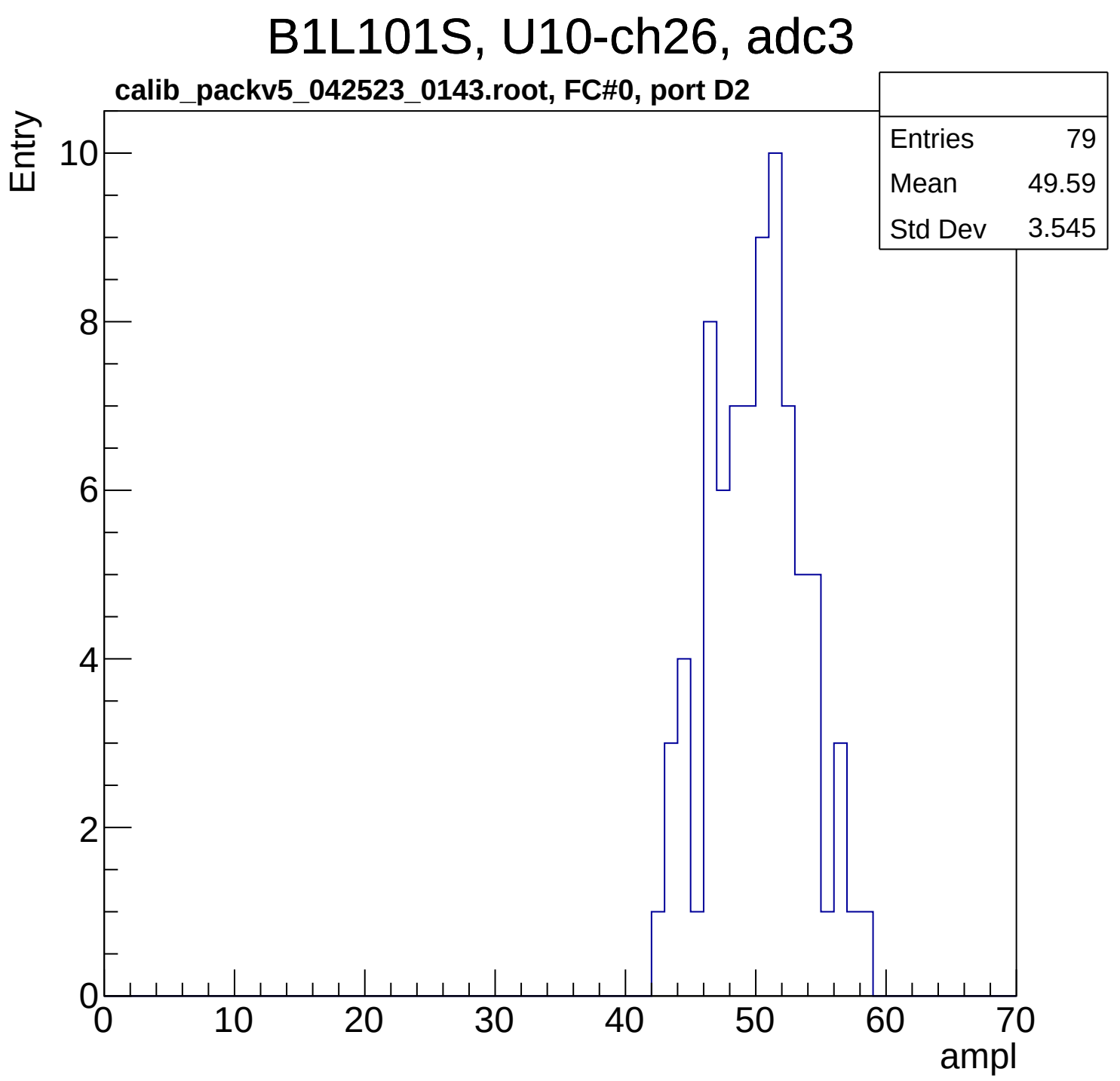
B1L101S, U10-ch26, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 49.59
Std Dev 3.545
Entry
ampl
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2
4
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0
10
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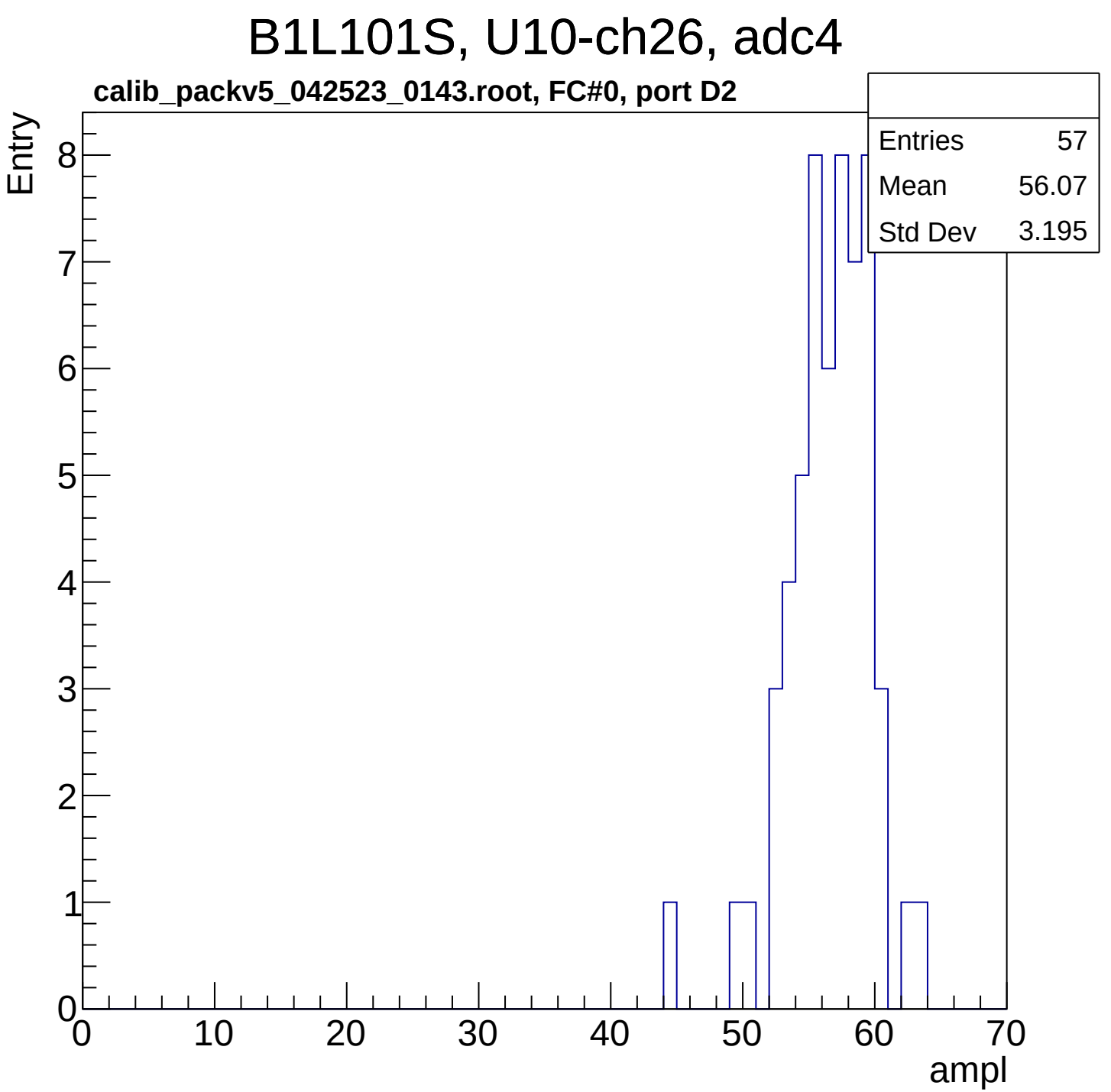
40
50
60
70


B1L101S, U10-ch26, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 56.07
Std Dev 3.195
Entry
ampl
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1
2
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4
5
6
7
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50
60
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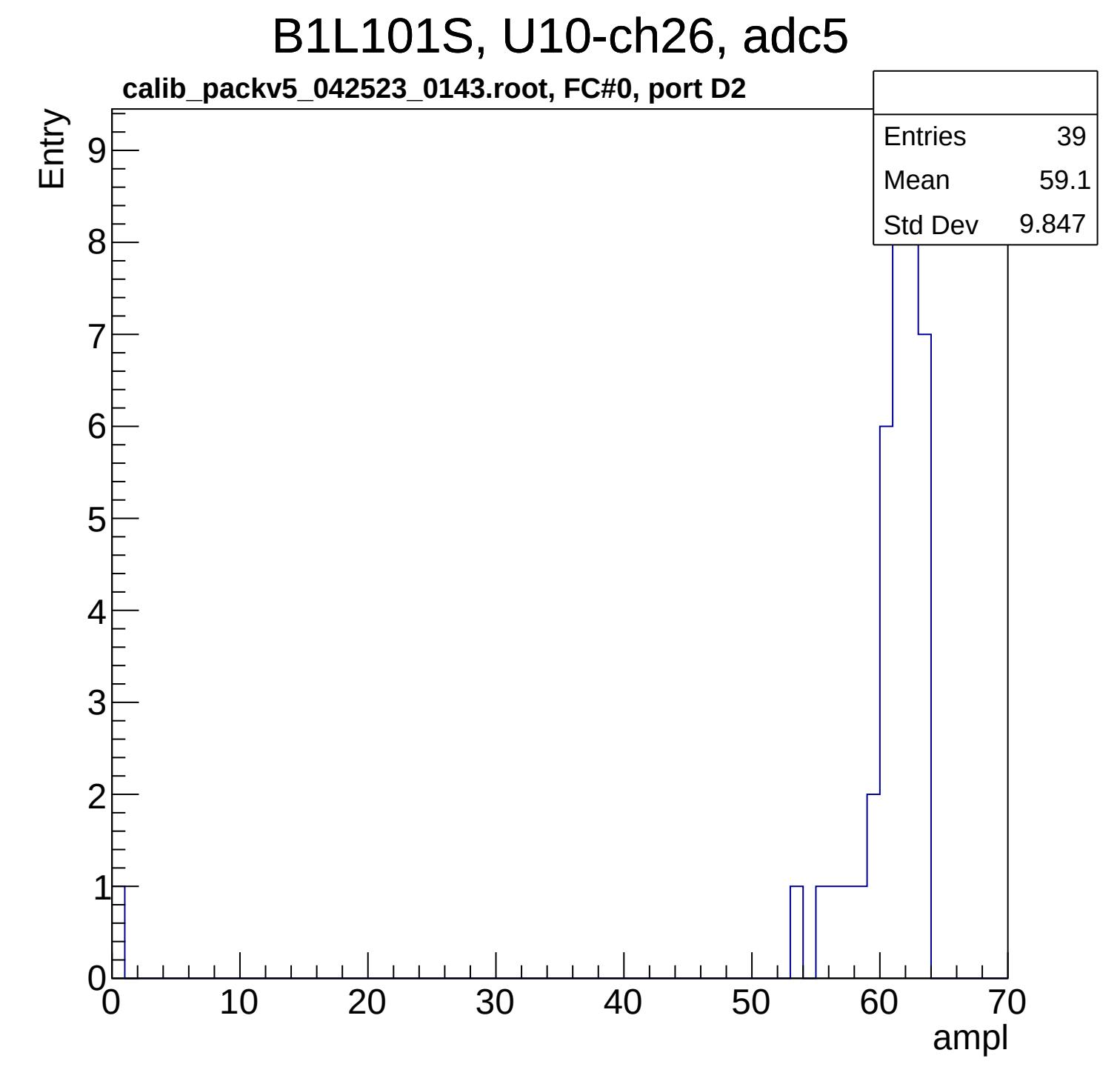
B1L101S, U10-ch26, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 39
Mean 59.1
Std Dev 9.847
Entry
ampl
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3
4
5
6
7
8
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0
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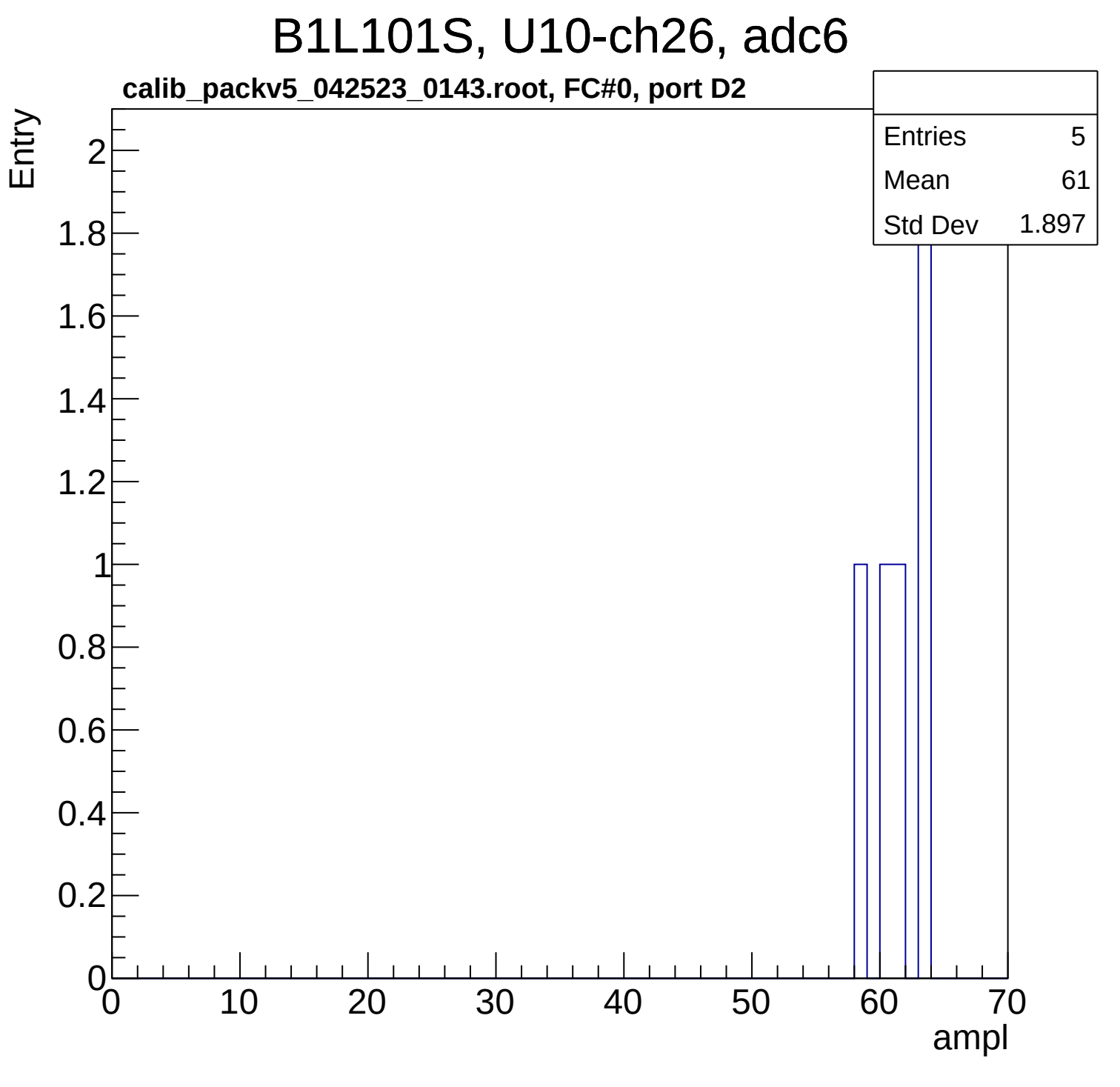
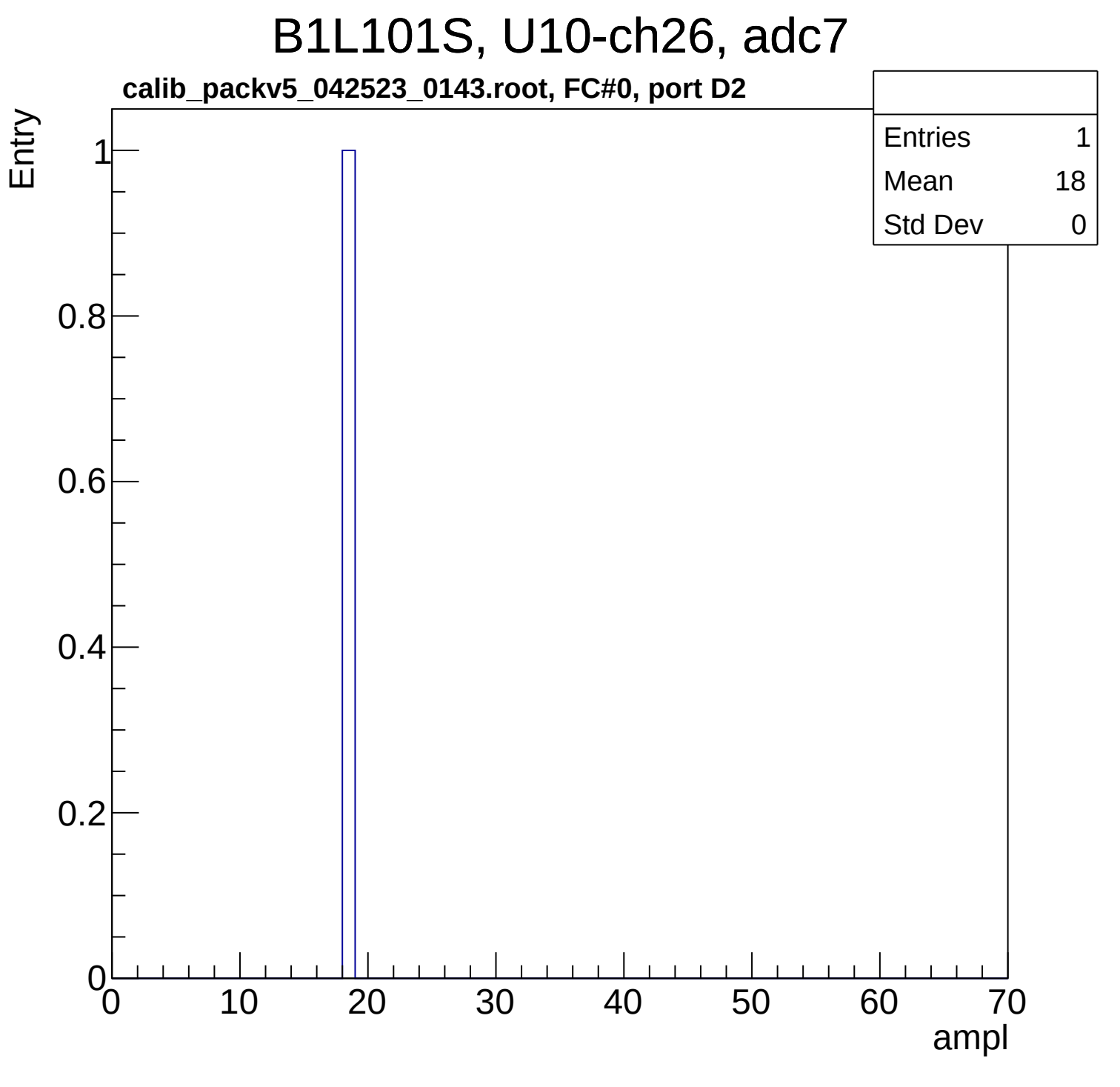
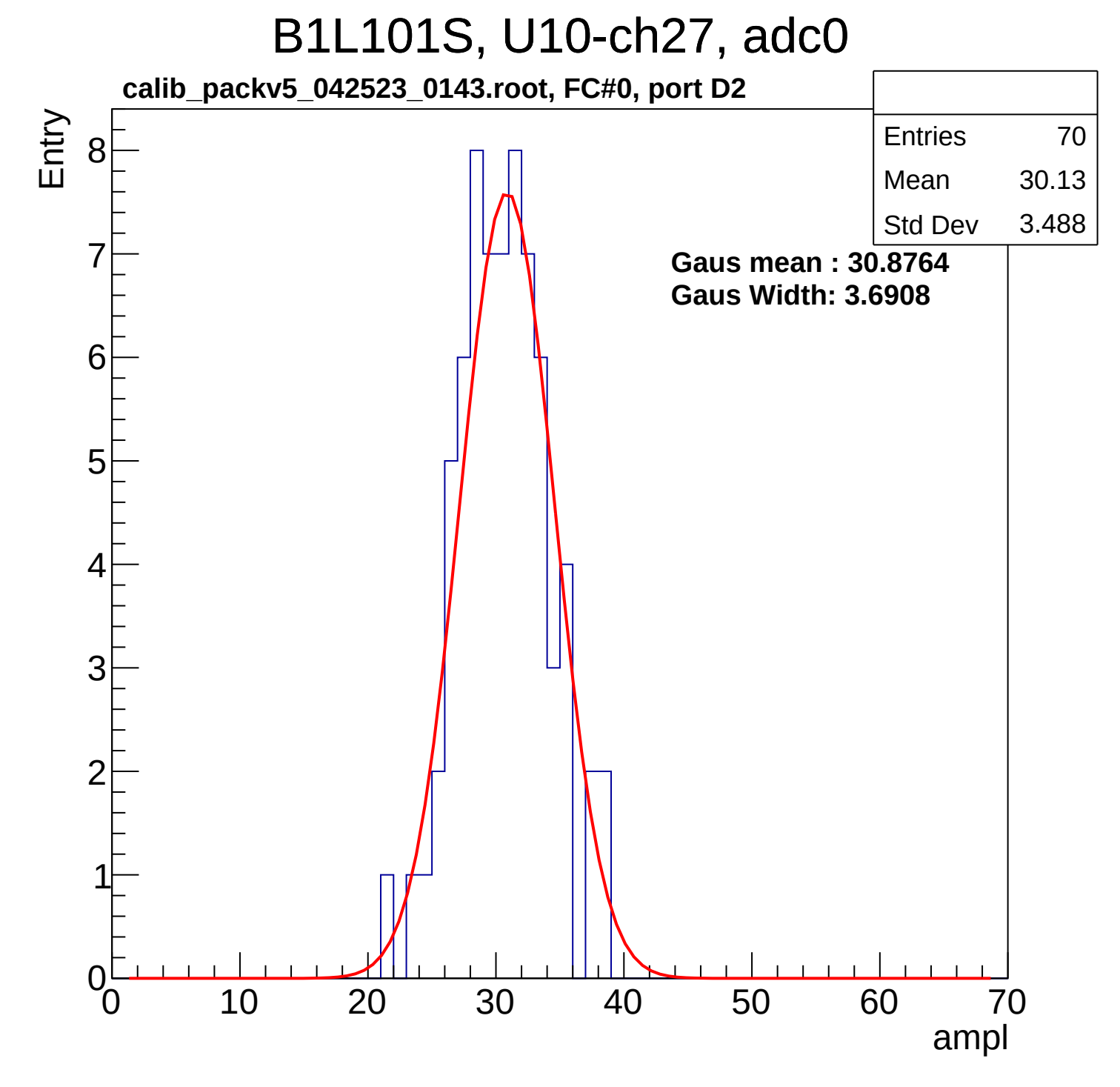

B1L101S, U10-ch26, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 61
Std Dev 1.897
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U10-ch26, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 18
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch27, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 30.13
Std Dev 3.488
Gaus mean : 30.8764
Gaus Width: 3.6908
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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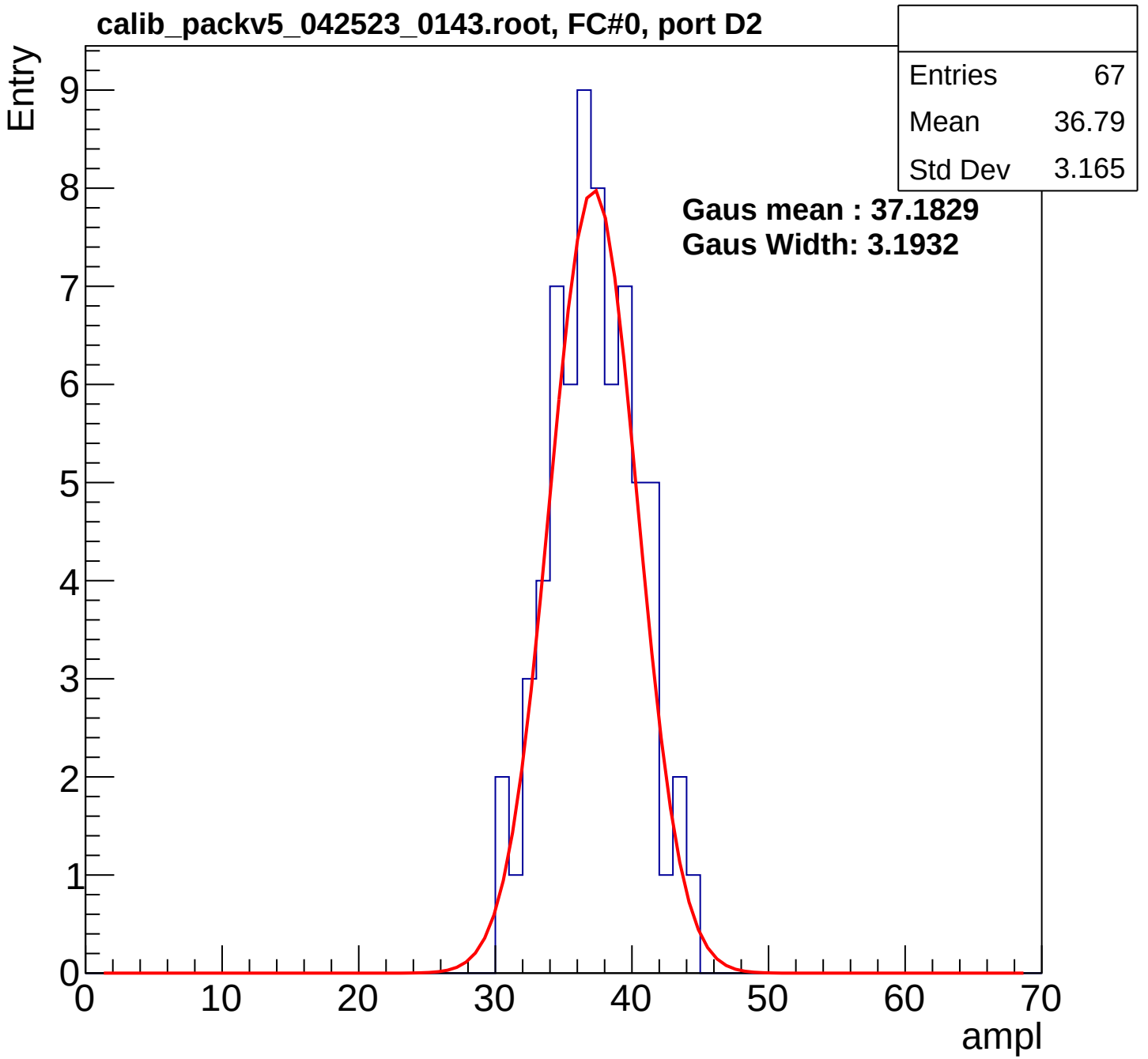
B1L101S, U10-ch27, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 36.79
Std Dev 3.165
Gaus mean : 37.1829
Gaus Width: 3.1932
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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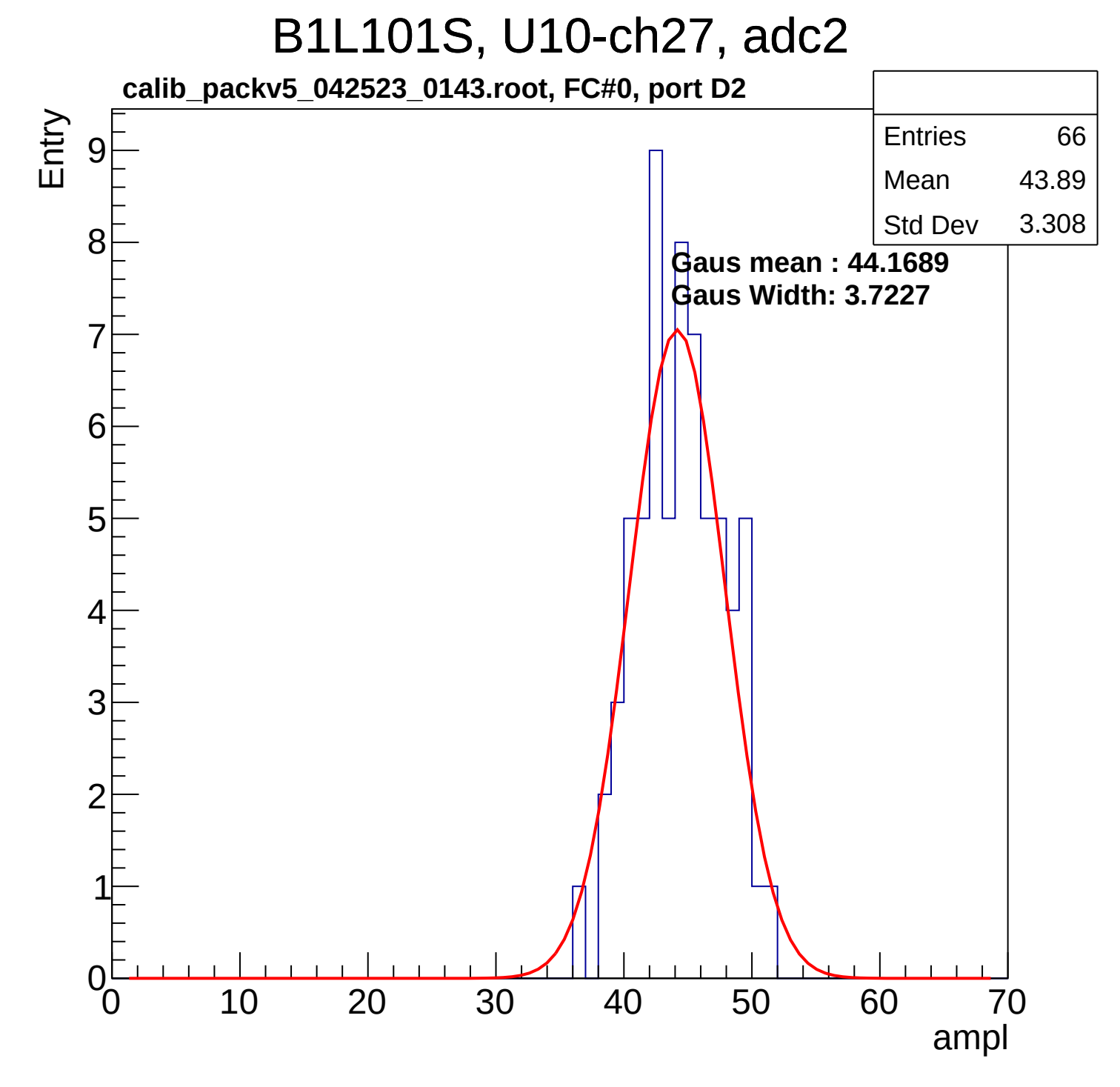
B1L101S, U10-ch27, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 43.89
Std Dev 3.308
Gaus mean : 44.1689
Gaus Width: 3.7227
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
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60
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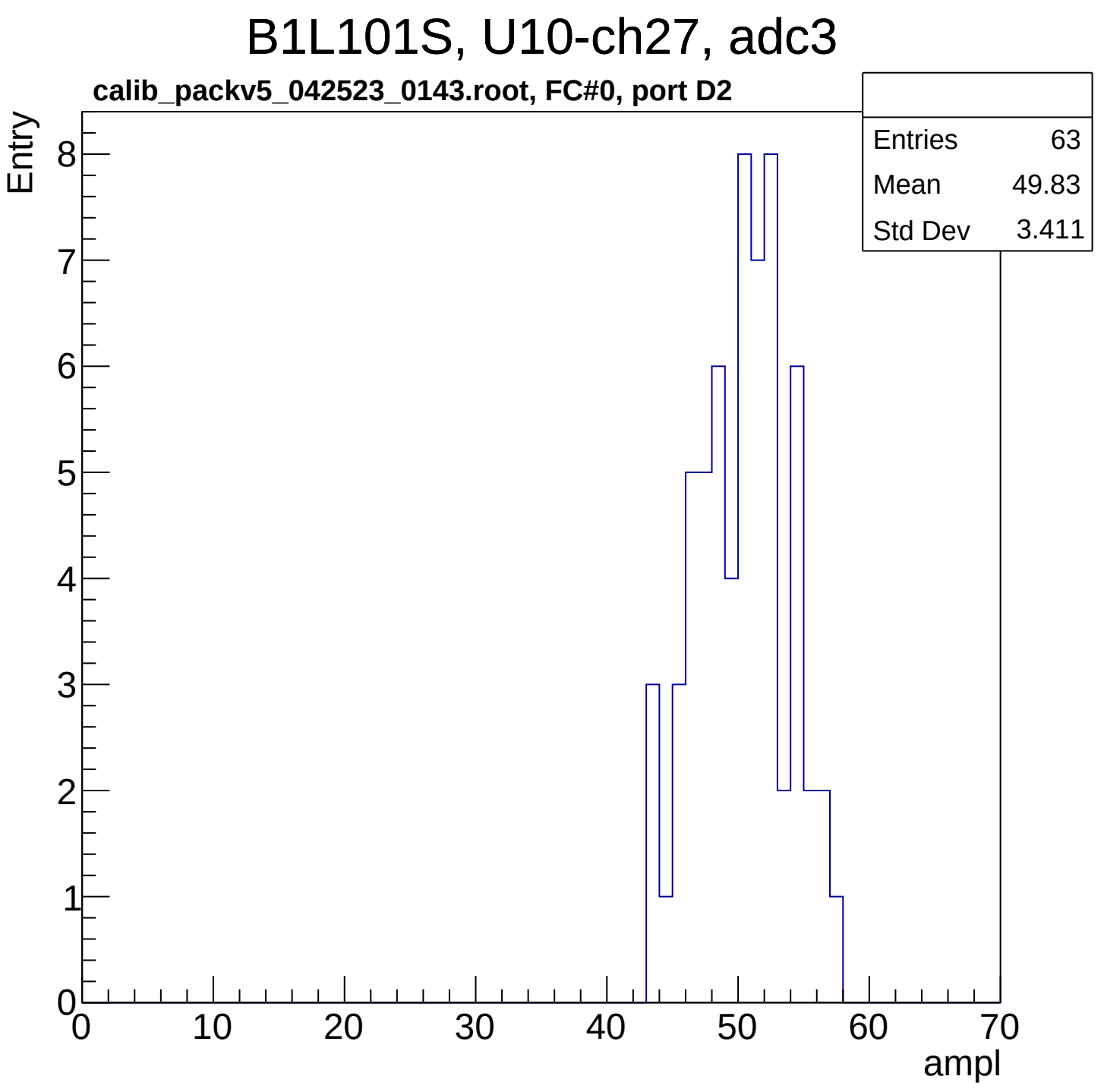
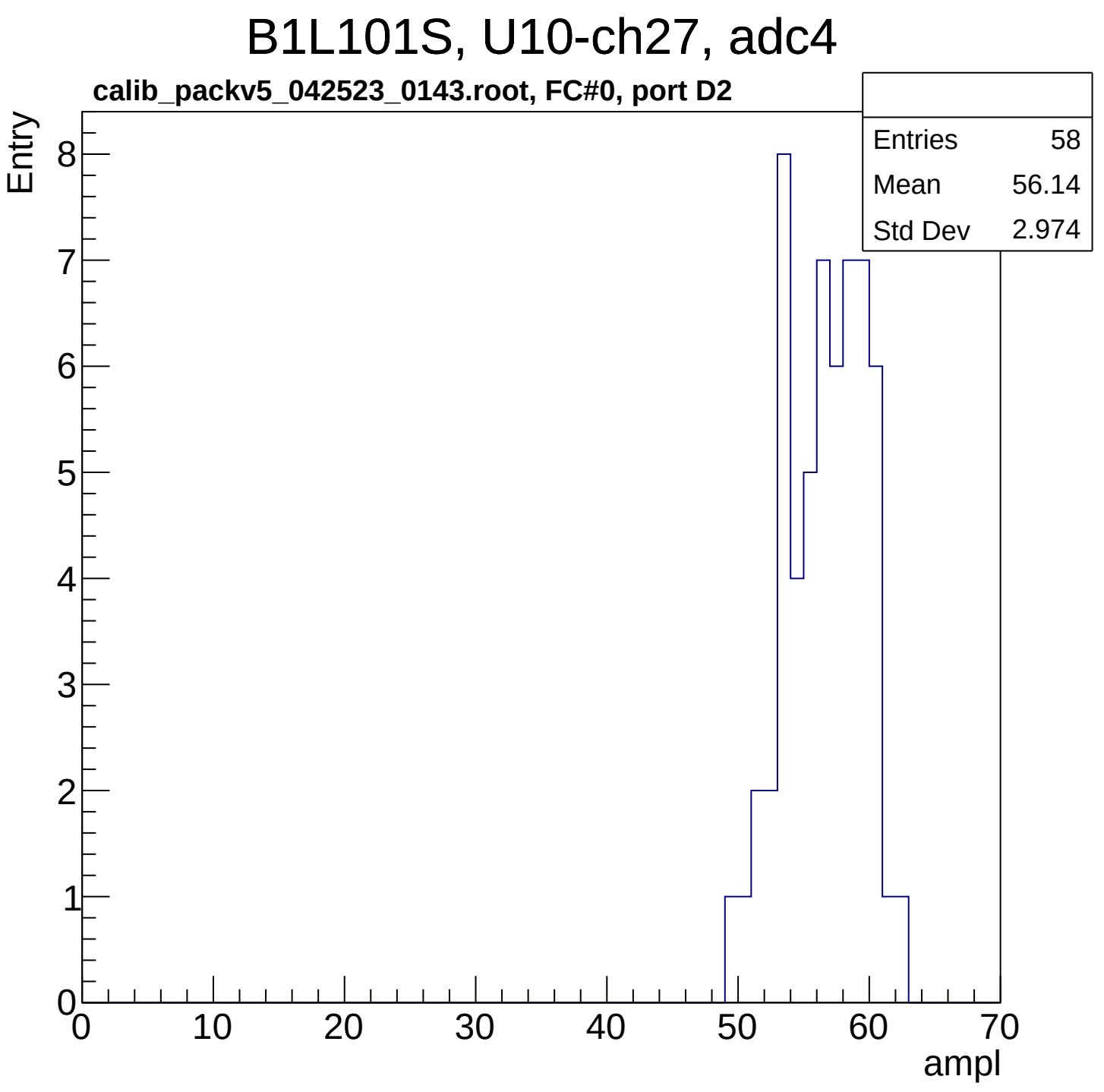
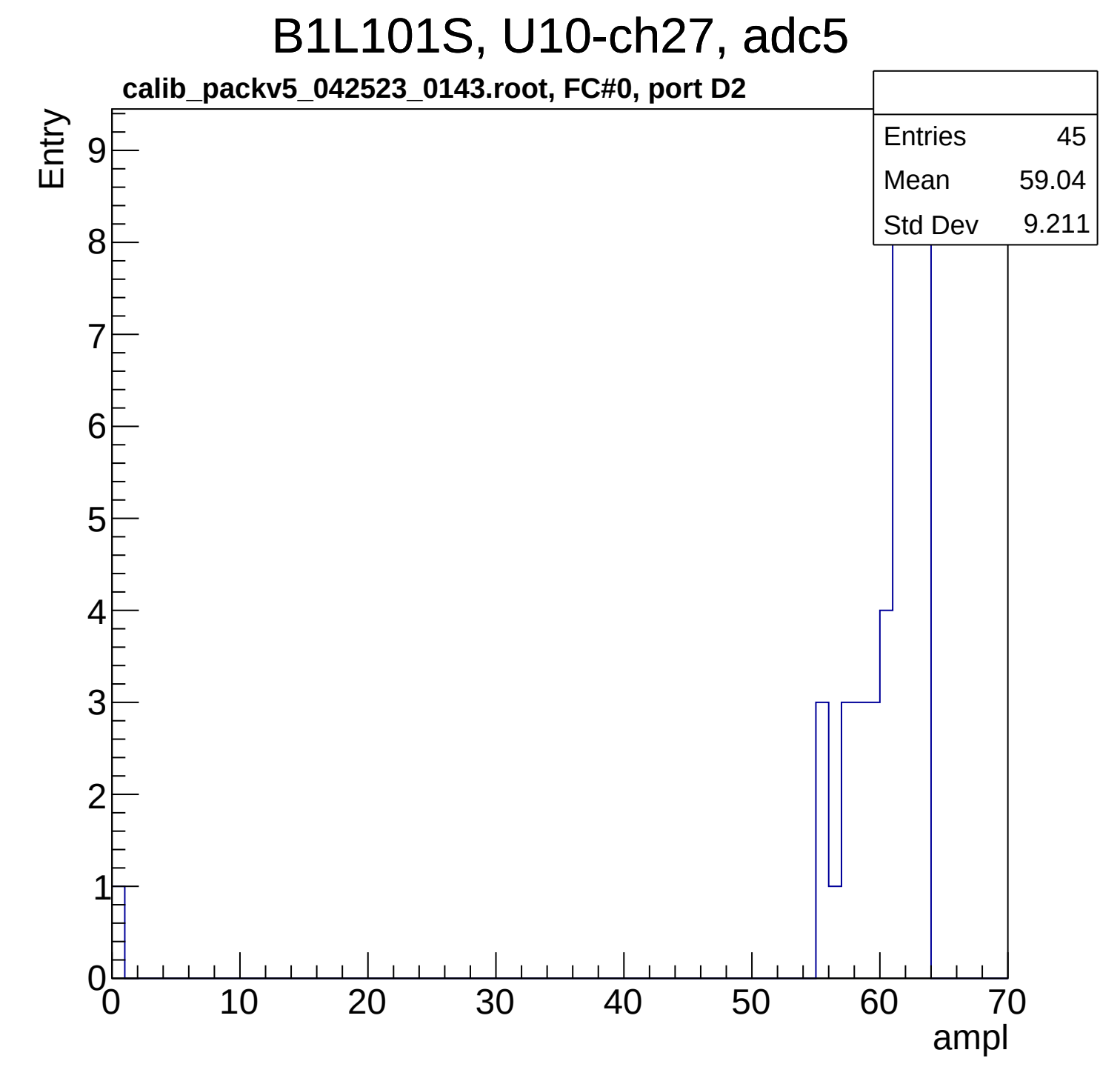

B1L101S, U10-ch27, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 49.83
Std Dev 3.411
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch27, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 56.14
Std Dev 2.974
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch27, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 59.04
Std Dev 9.211
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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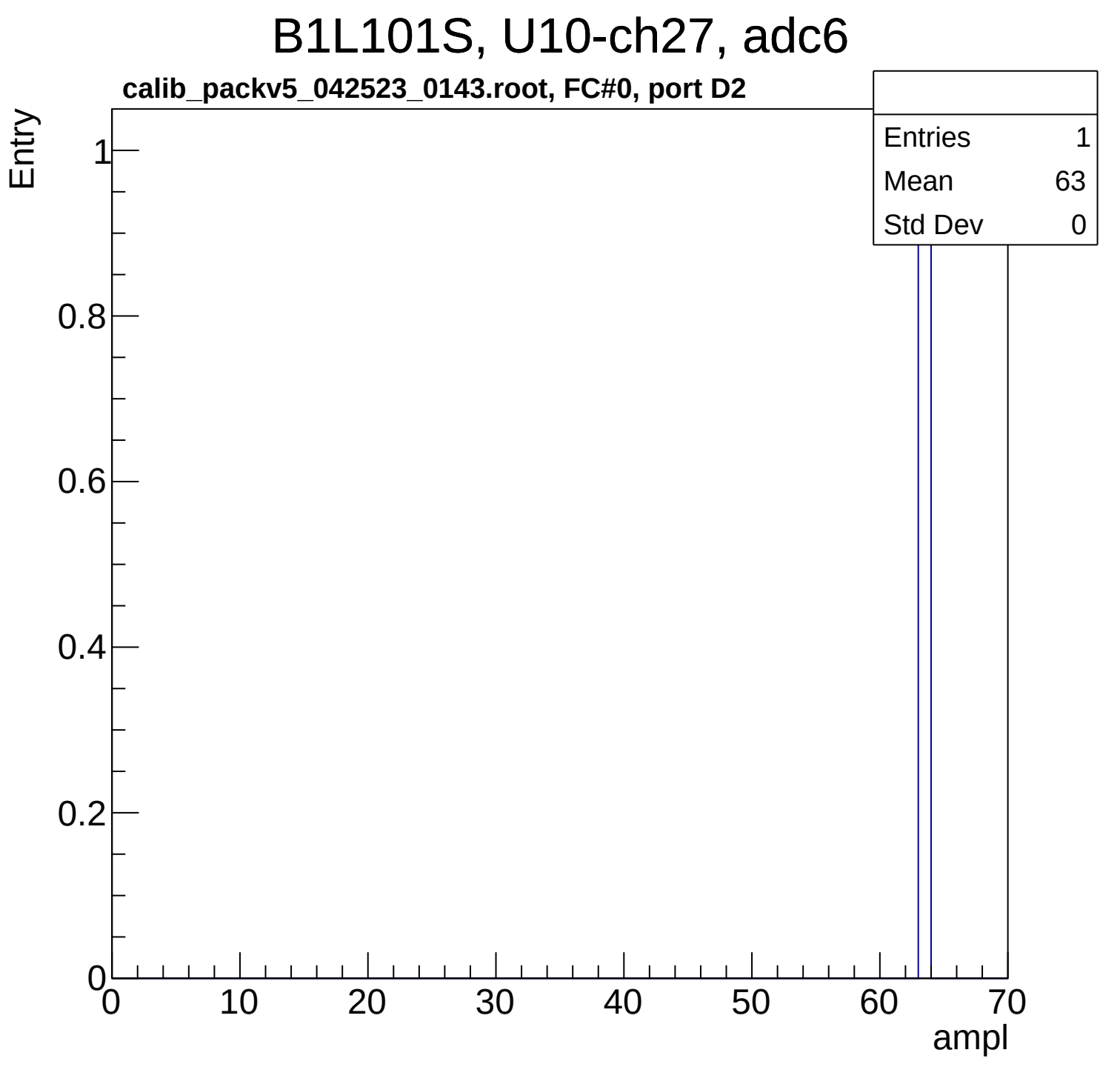
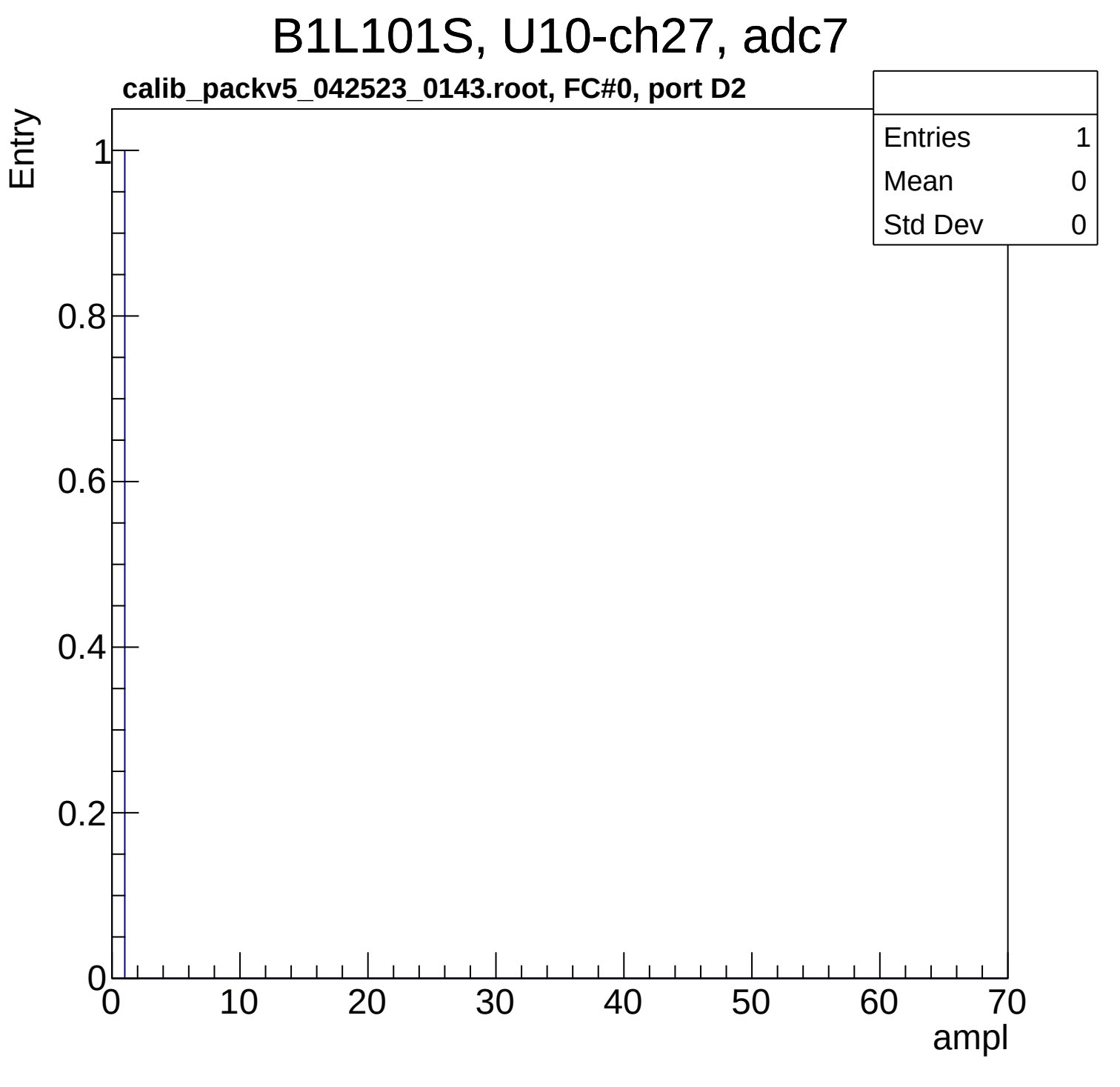
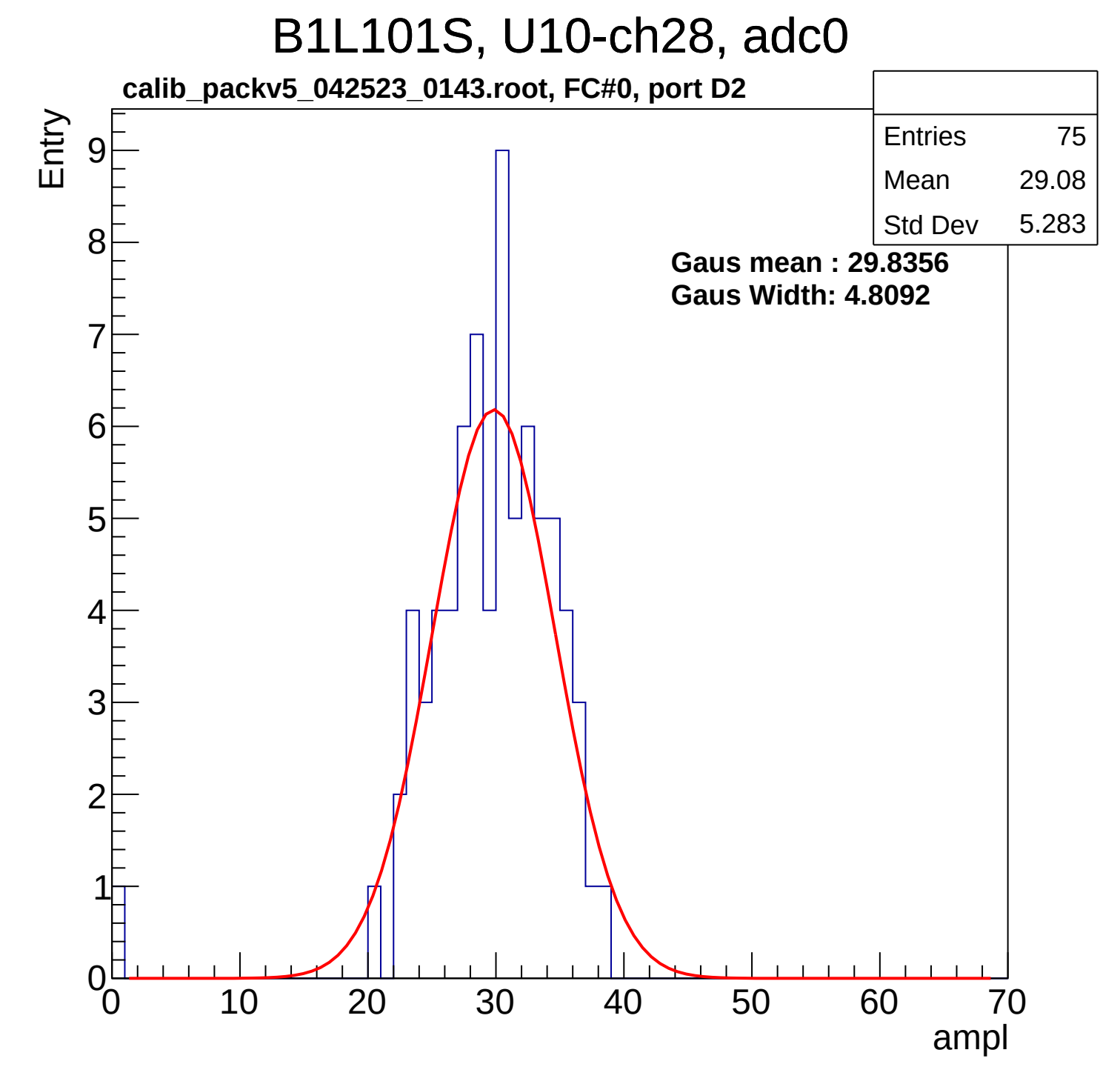
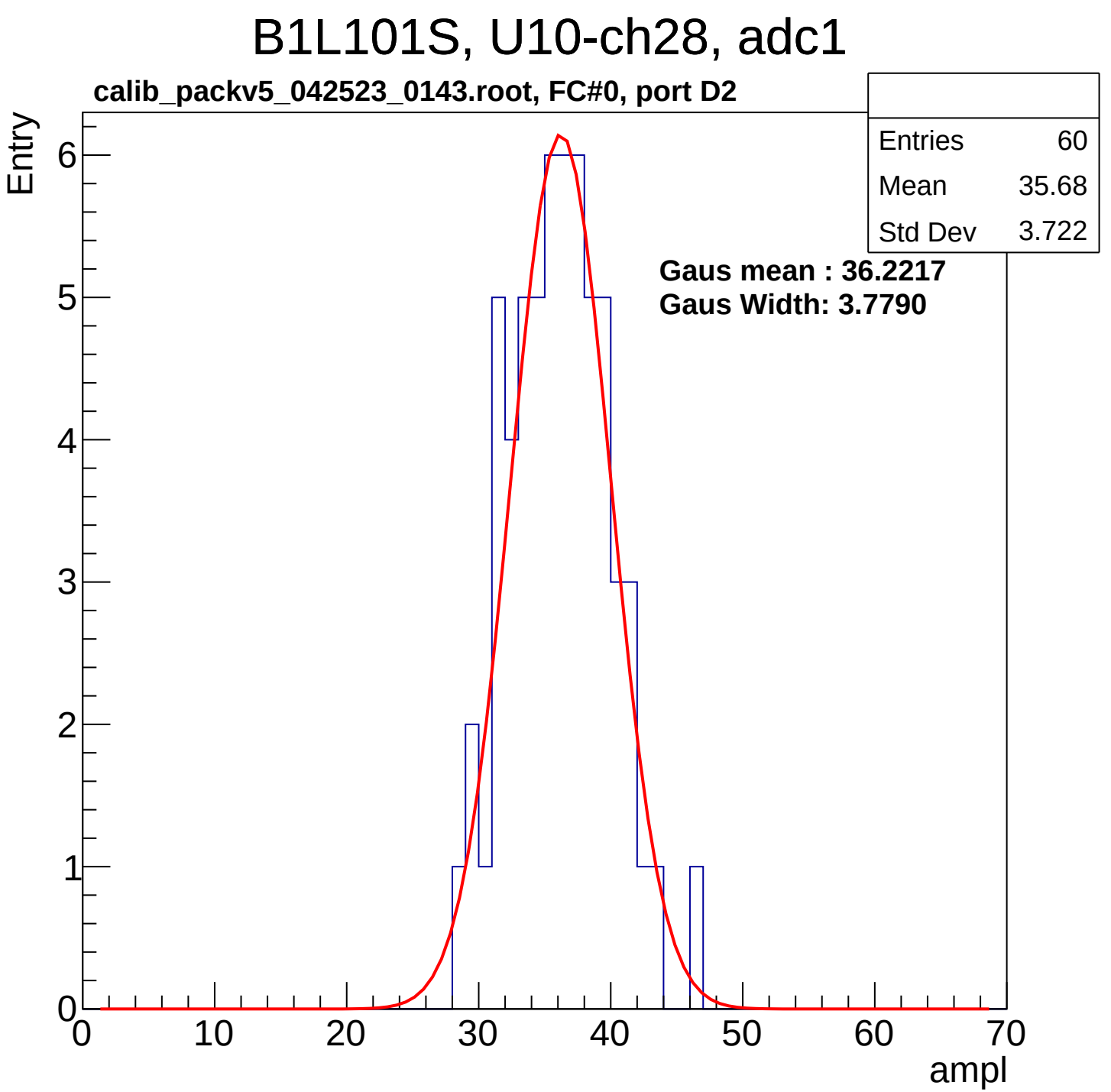
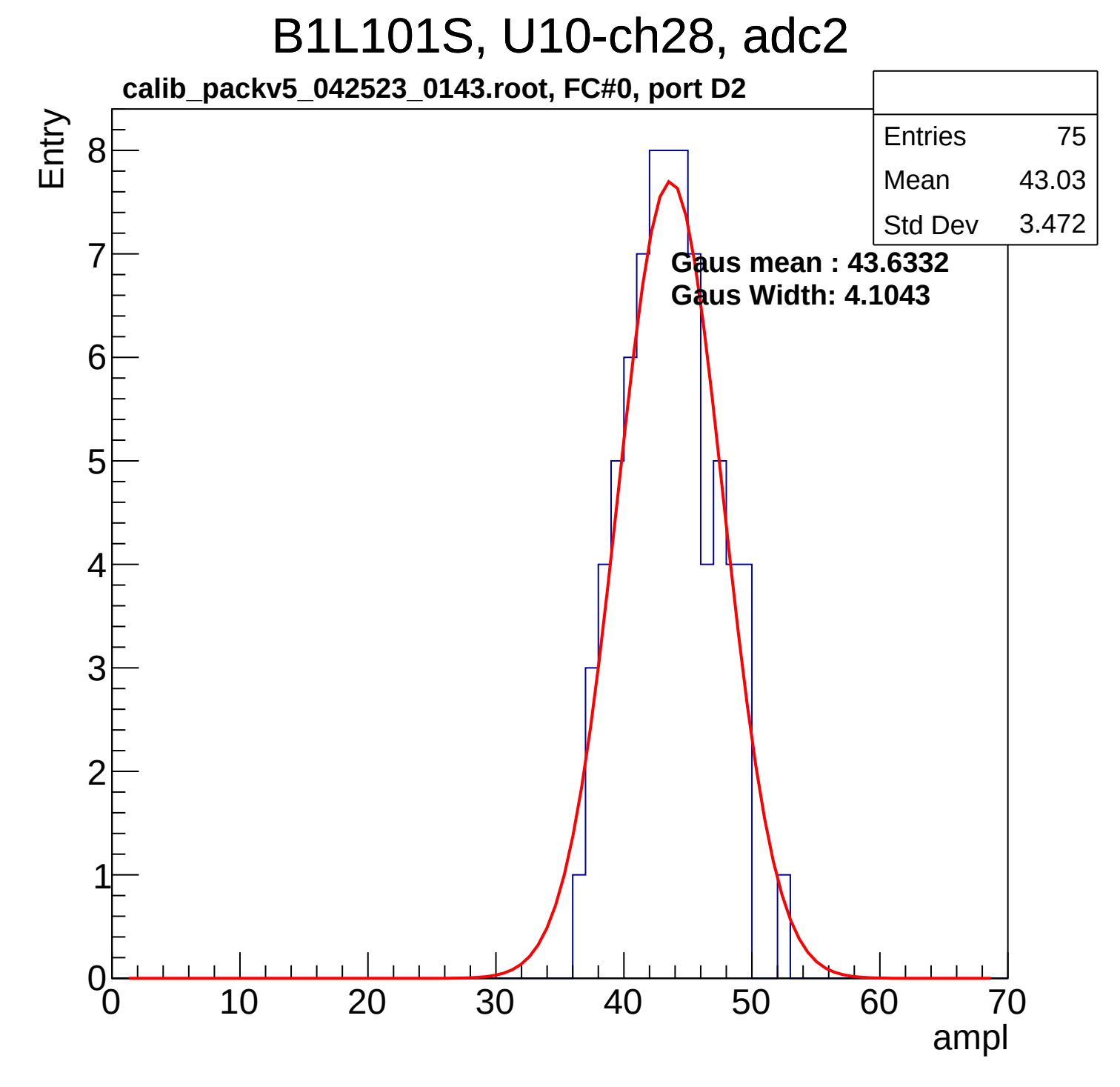

B1L101S, U10-ch27, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch27, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch28, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 29.08
Std Dev 5.283
Gaus mean : 29.8356
Gaus Width: 4.8092
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch28, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 35.68
Std Dev 3.722
Gaus mean : 36.2217
Gaus Width: 3.7790
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L101S, U10-ch28, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 43.03
Std Dev 3.472
Gaus mean : 43.6332
Gaus Width: 4.1043
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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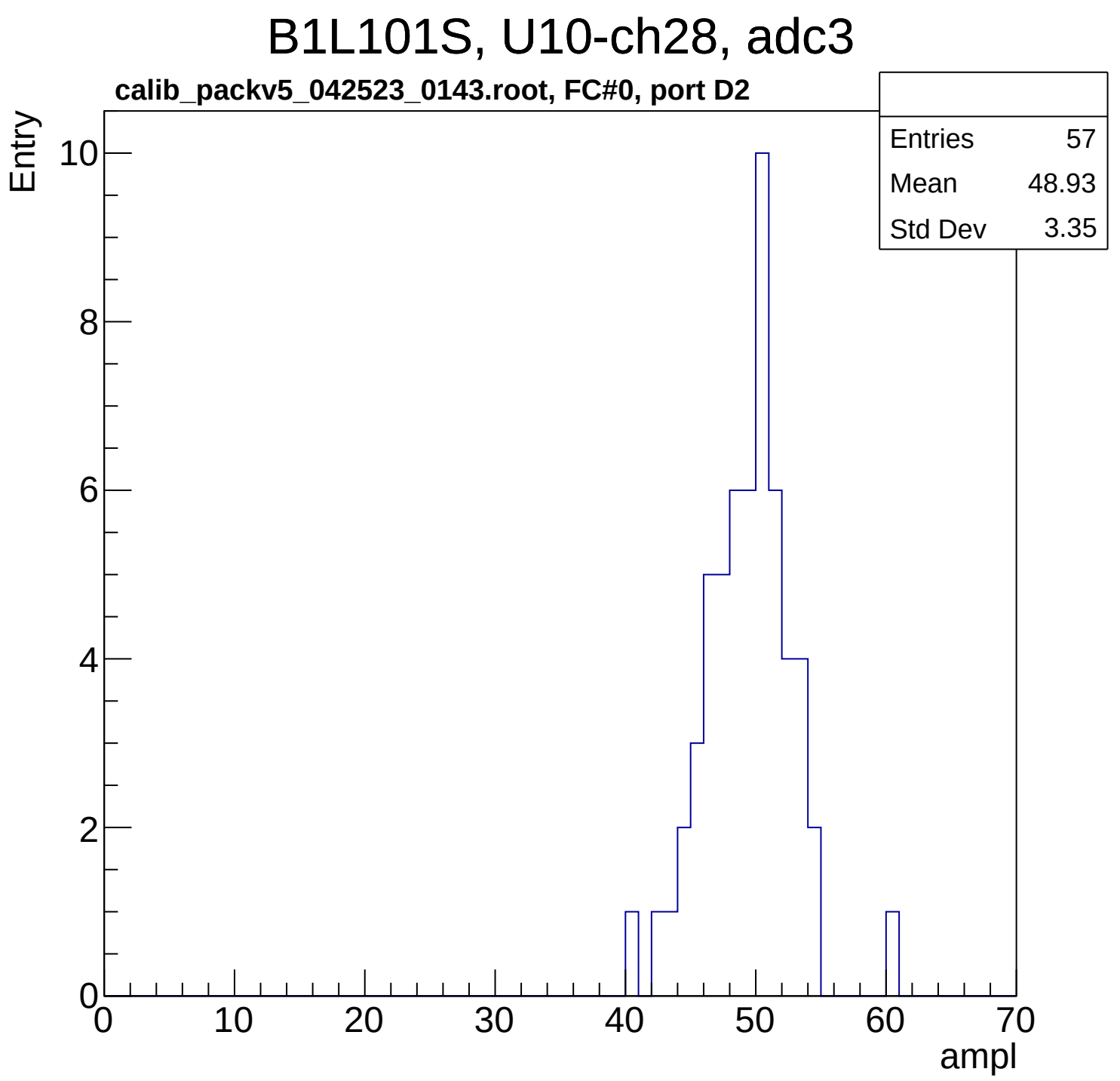
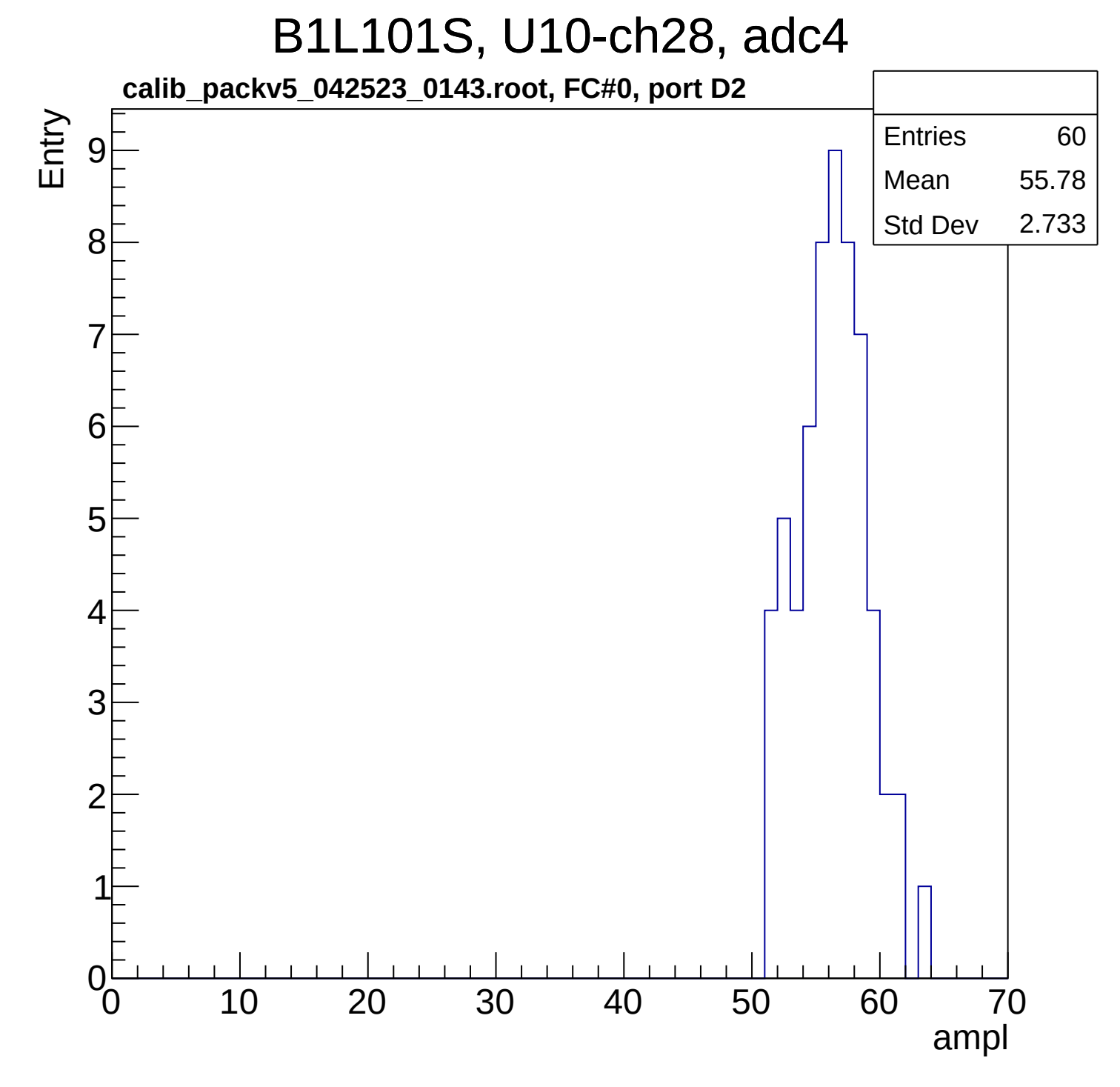
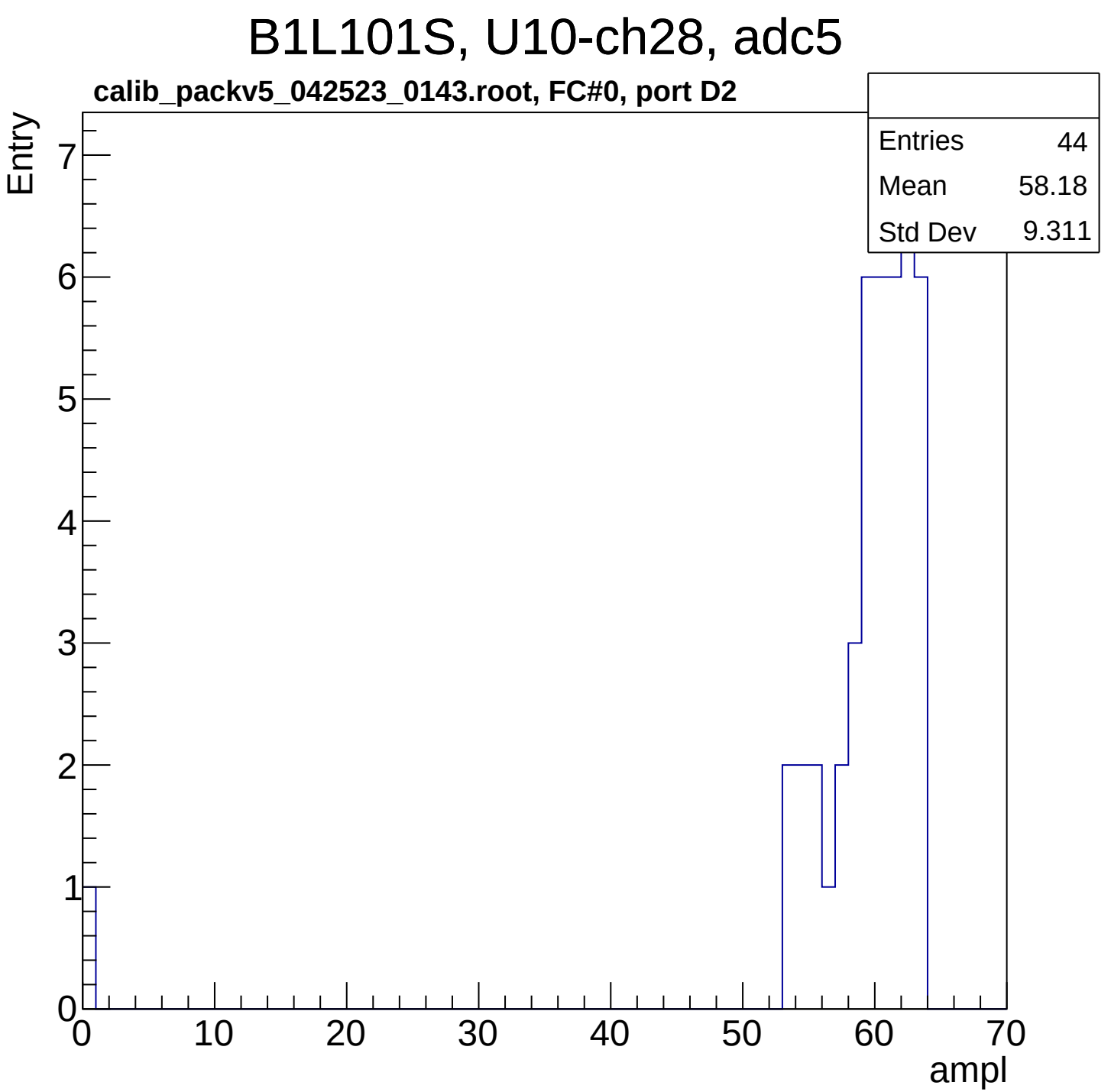
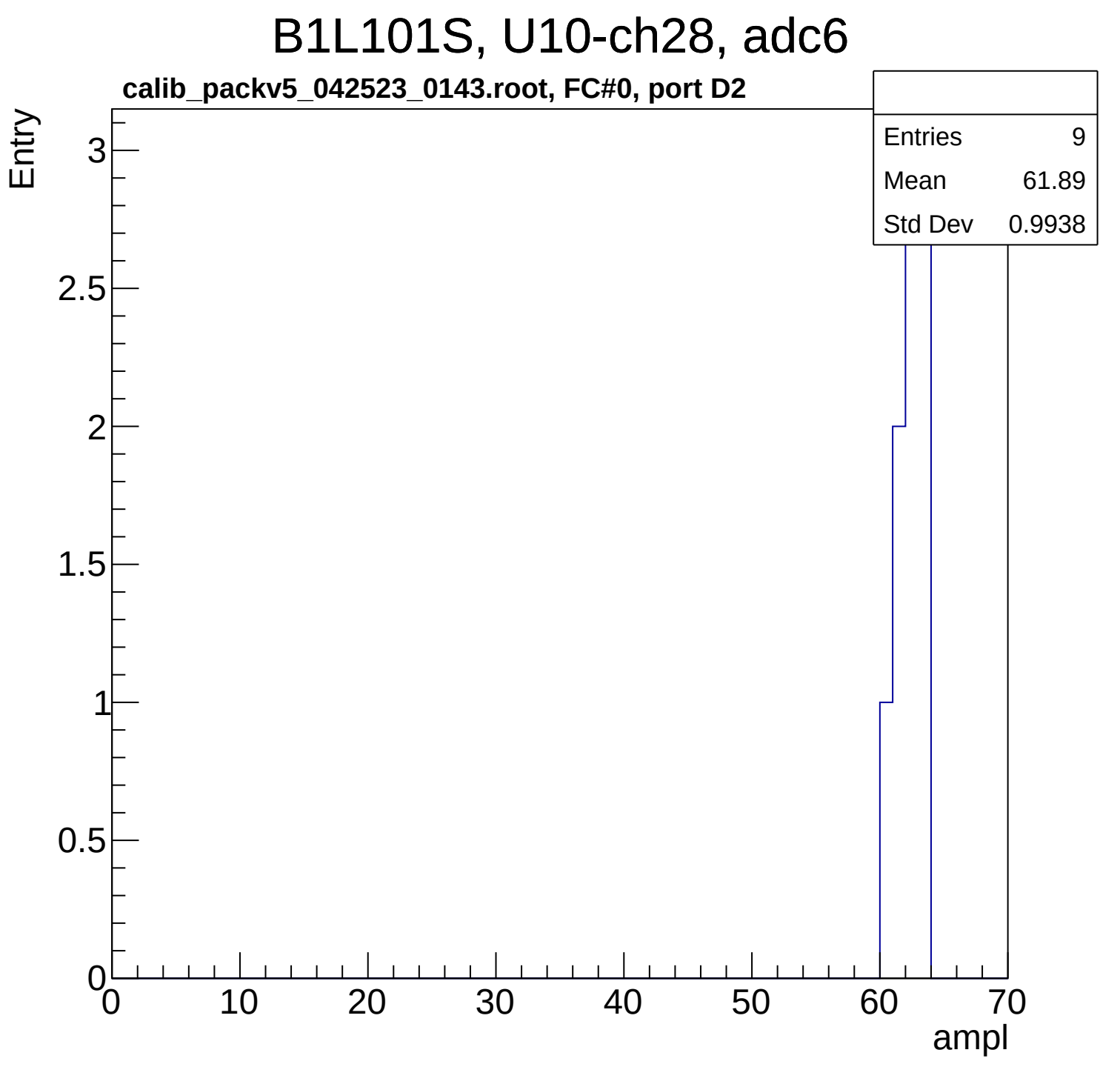
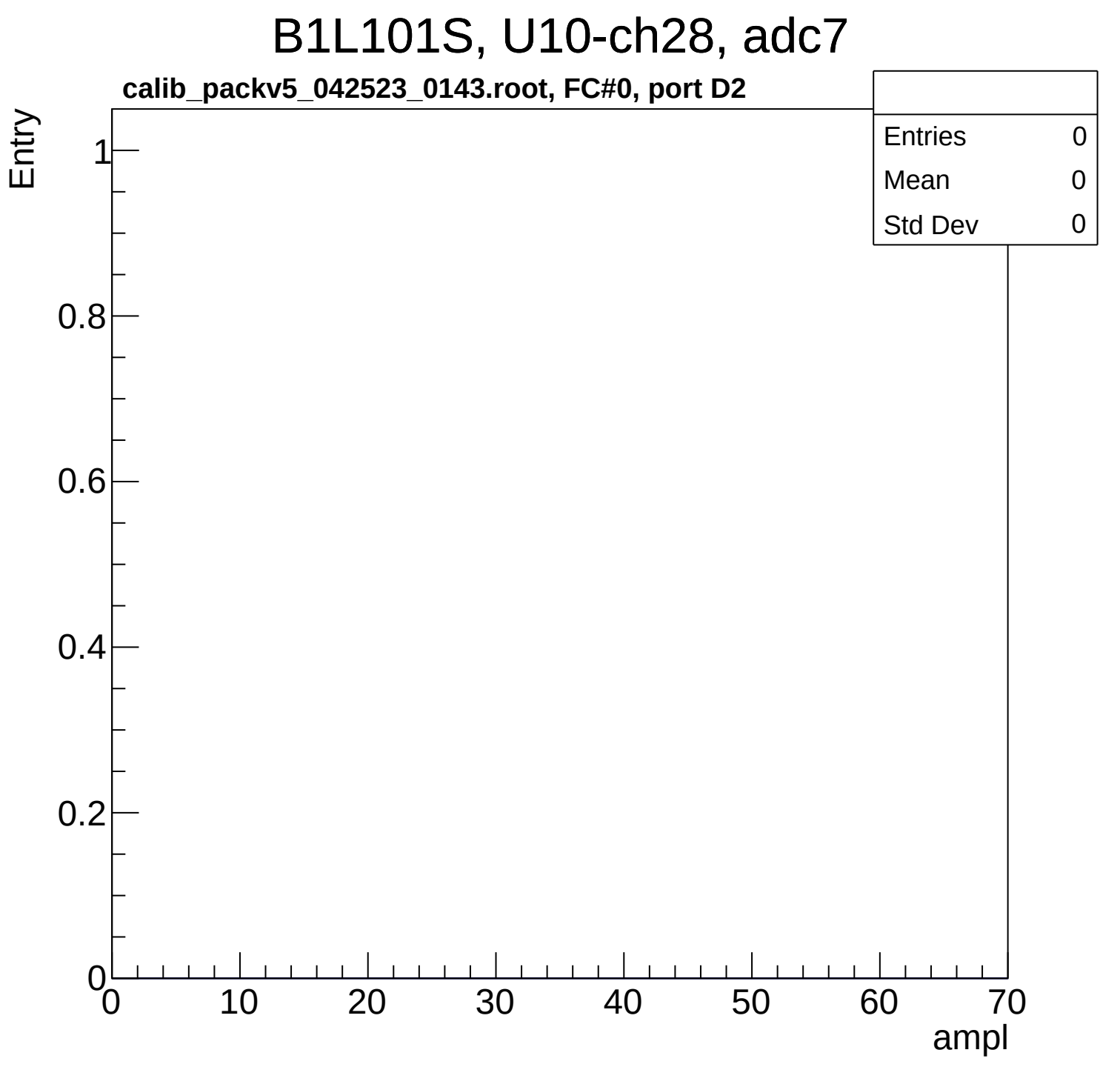
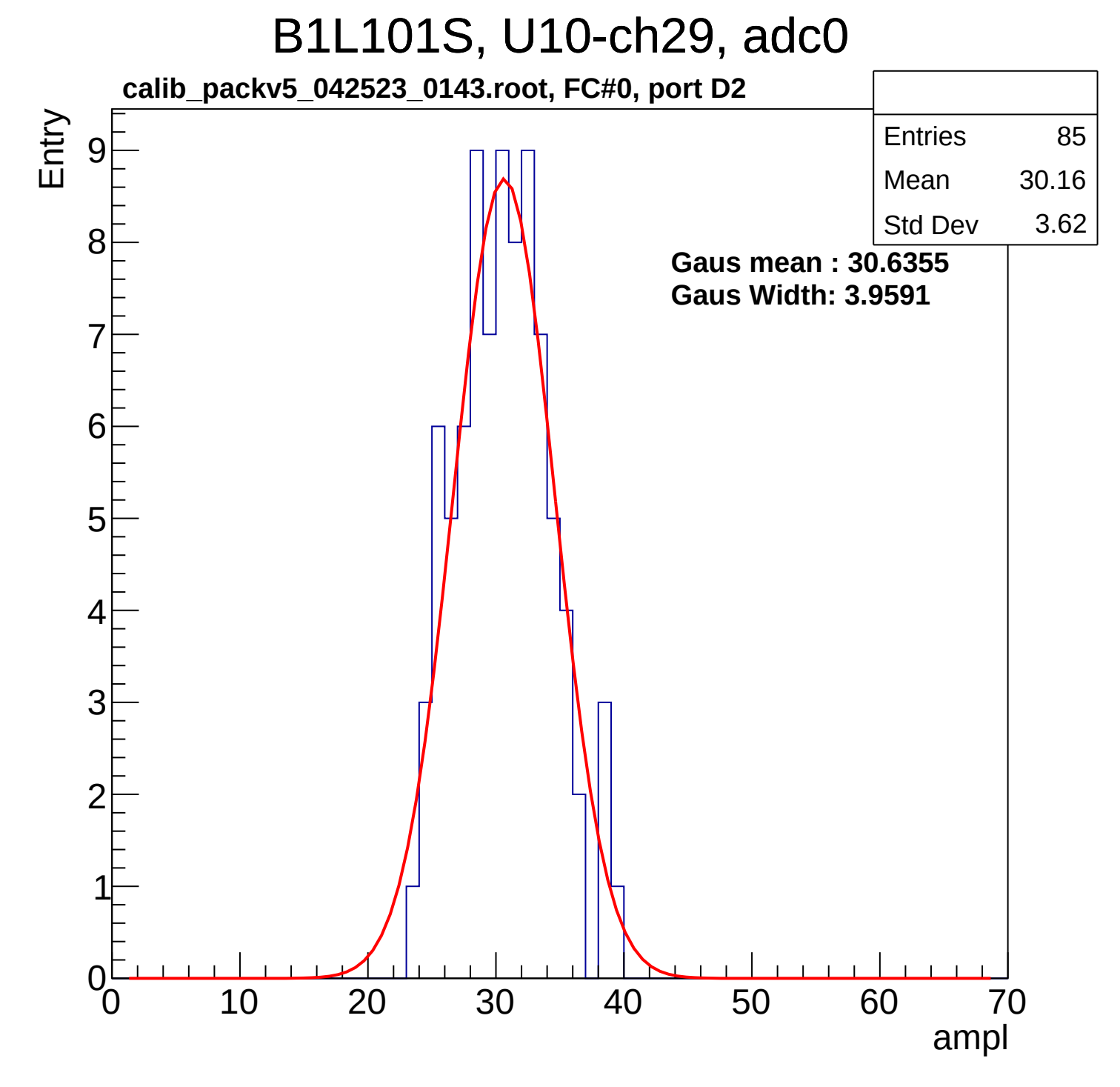

B1L101S, U10-ch28, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 48.93
Std Dev 3.35
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

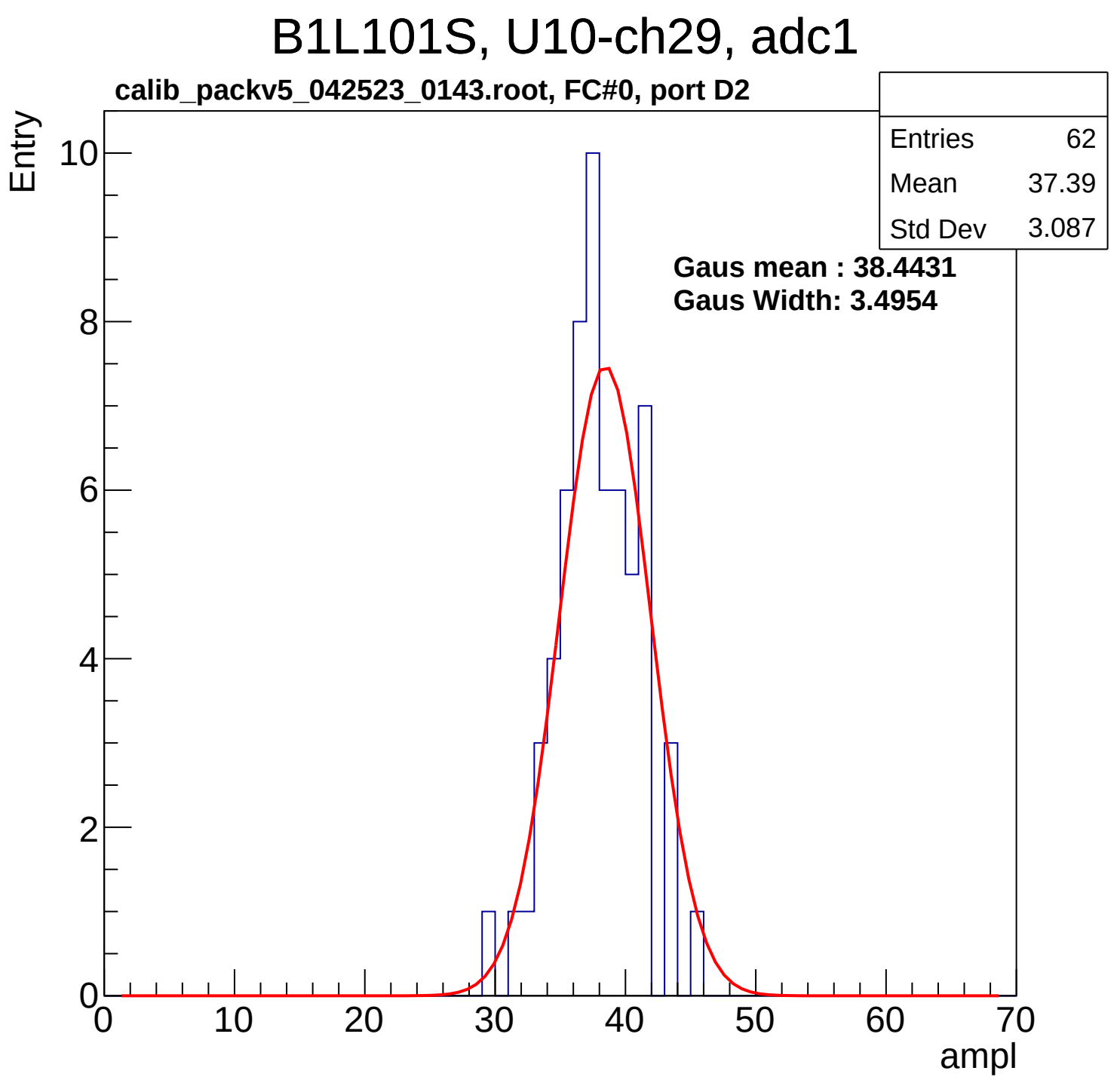

B1L101S, U10-ch28, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 55.78
Std Dev 2.733
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

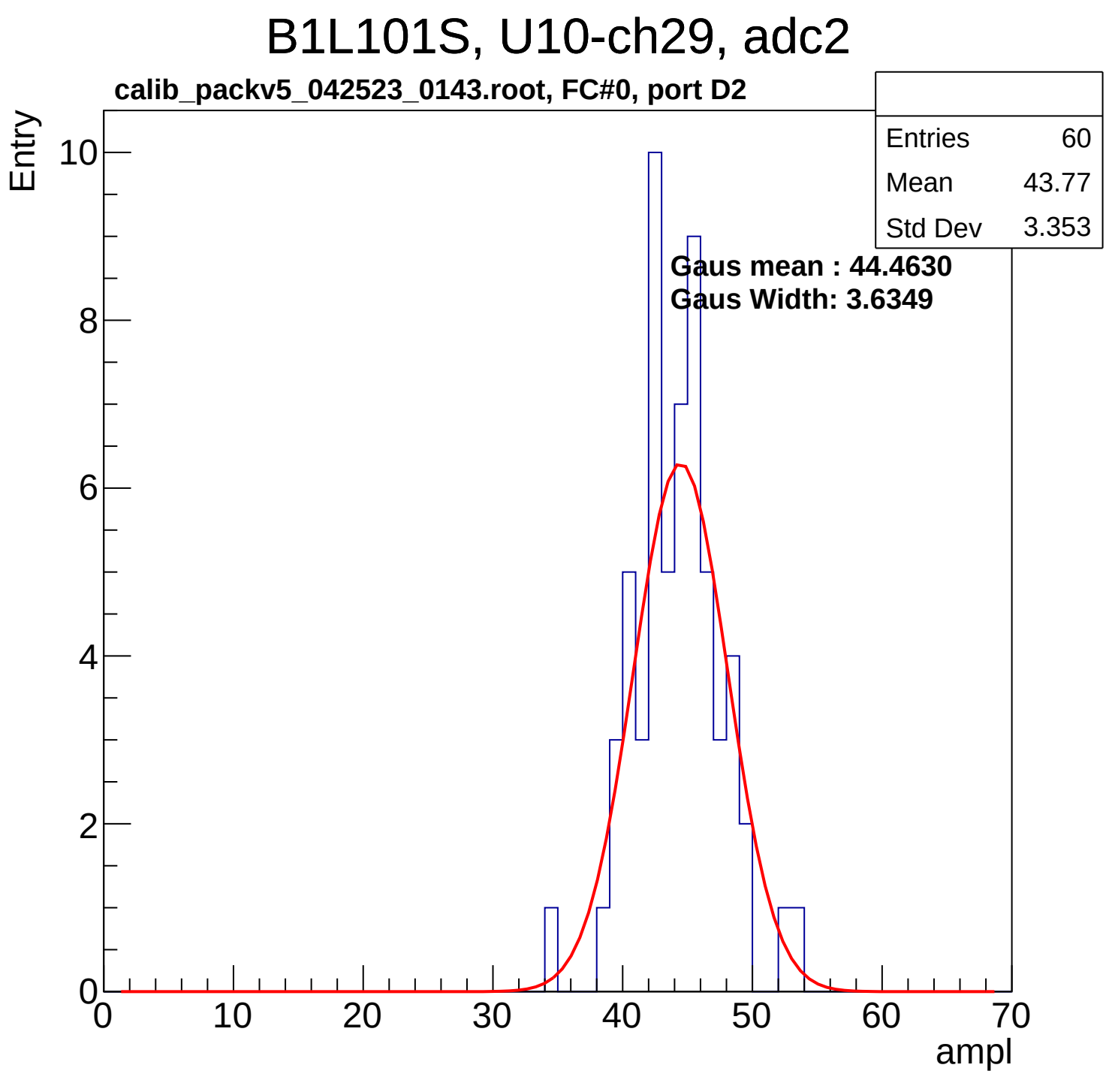

B1L101S, U10-ch28, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 44
Mean 58.18
Std Dev 9.311
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U10-ch28, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 61.89
Std Dev 0.9938
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U10-ch28, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch29, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 85
Mean 30.16
Std Dev 3.62
Gaus mean : 30.6355
Gaus Width: 3.9591
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch29, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 37.39
Std Dev 3.087
Gaus mean : 38.4431
Gaus Width: 3.4954
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch29, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 43.77
Std Dev 3.353
Gaus mean : 44.4630
Gaus Width: 3.6349
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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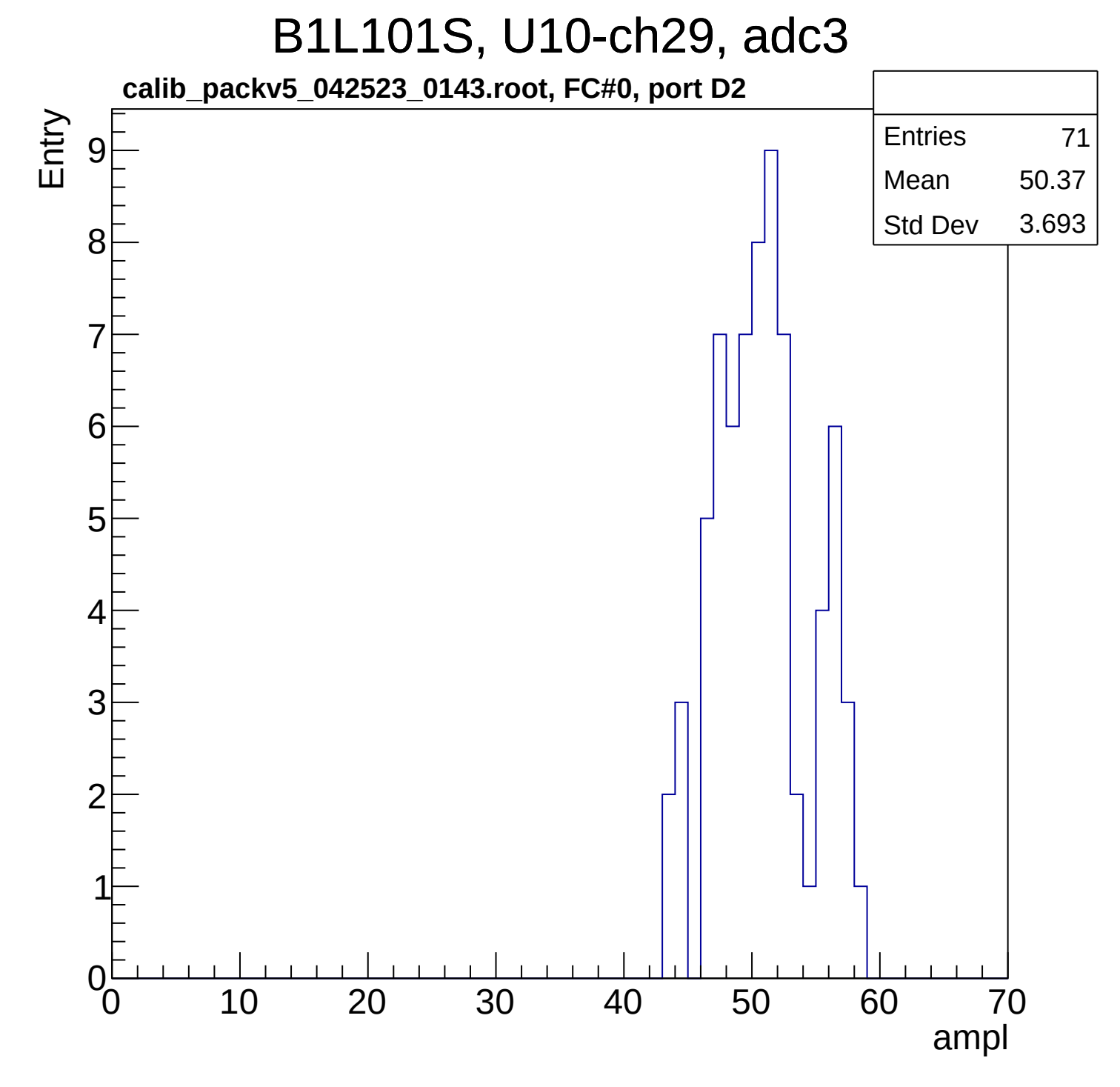
B1L101S, U10-ch29, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 50.37
Std Dev 3.693
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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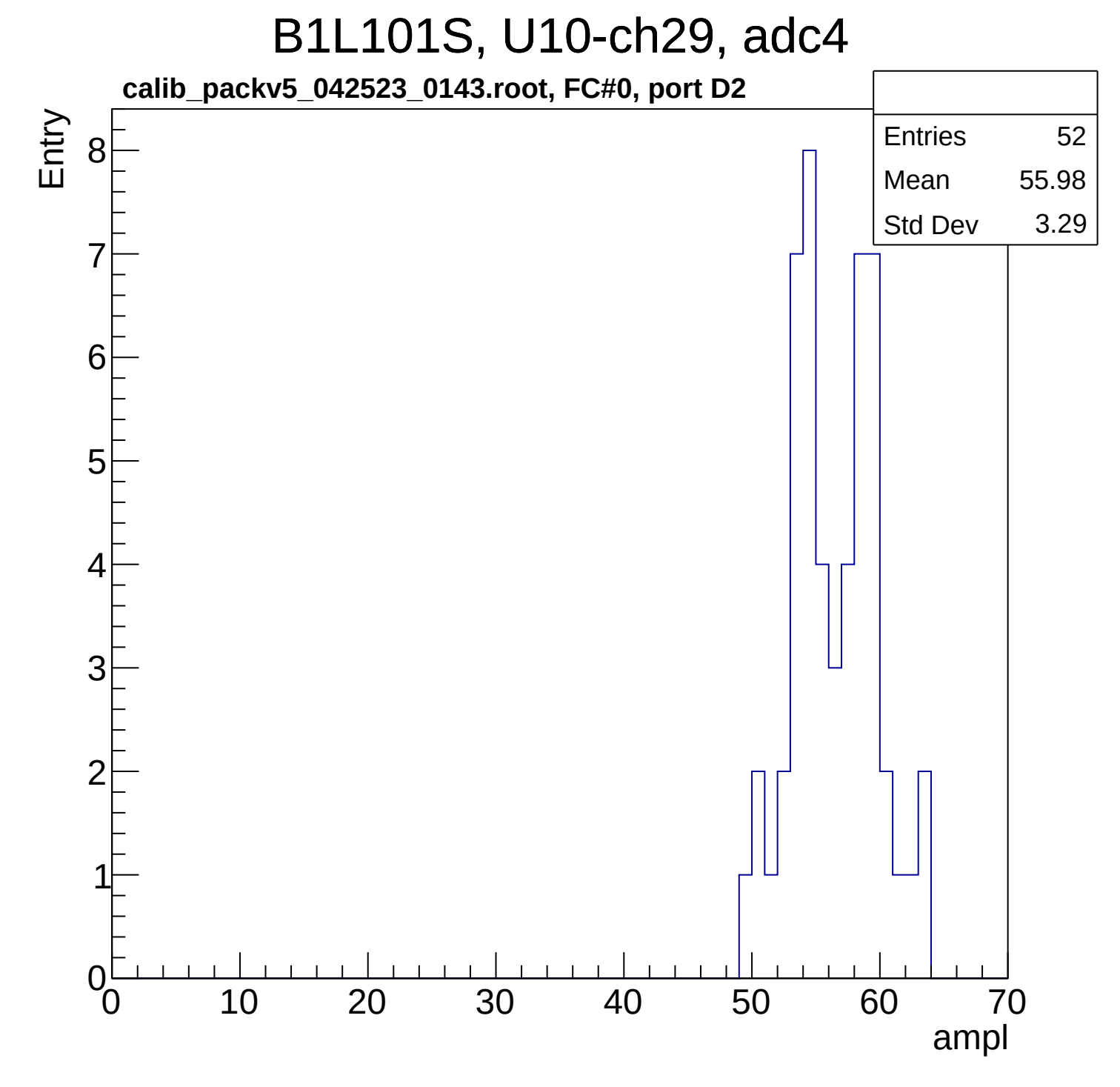
B1L101S, U10-ch29, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 55.98
Std Dev 3.29
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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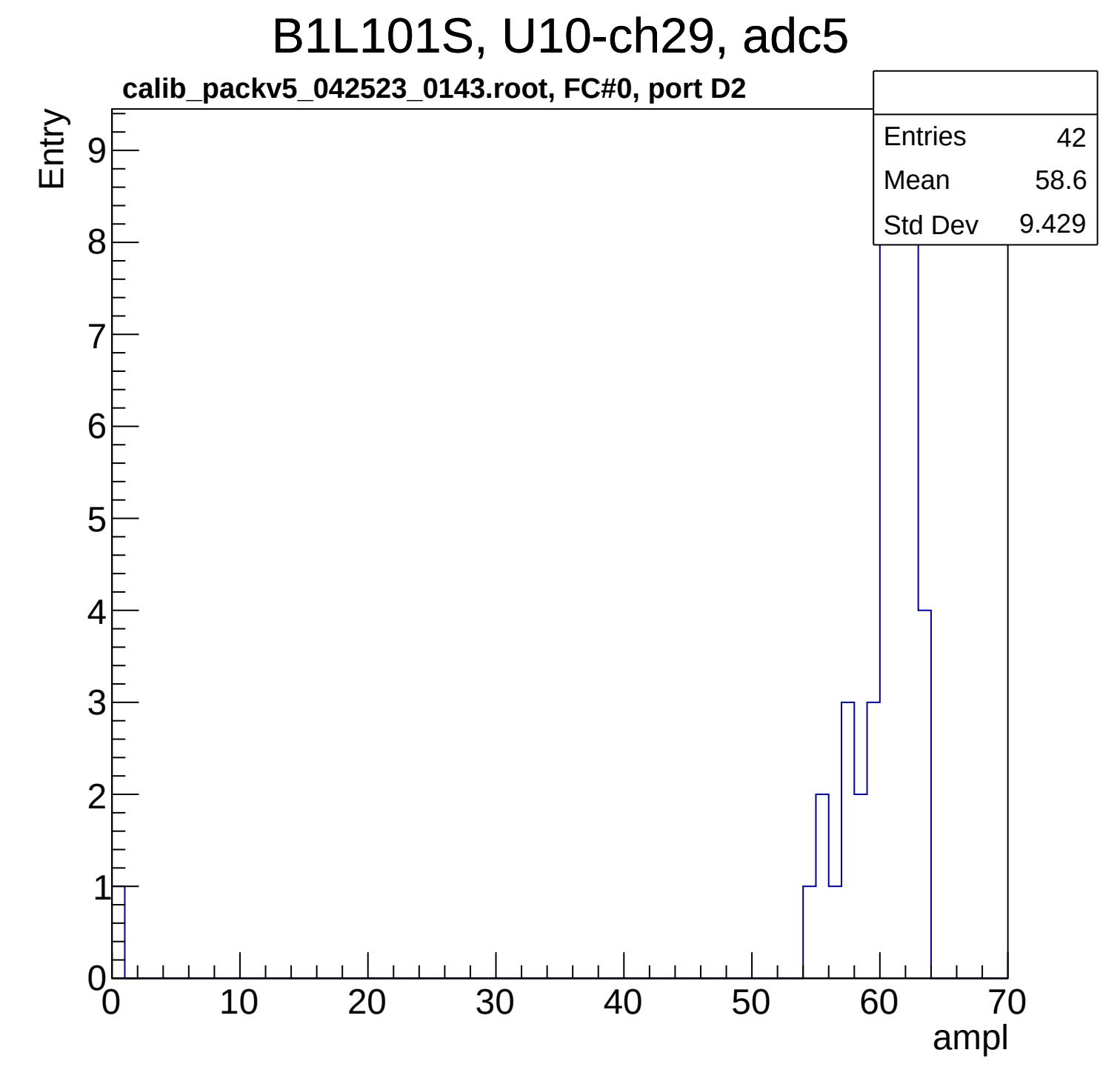
B1L101S, U10-ch29, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 58.6
Std Dev 9.429
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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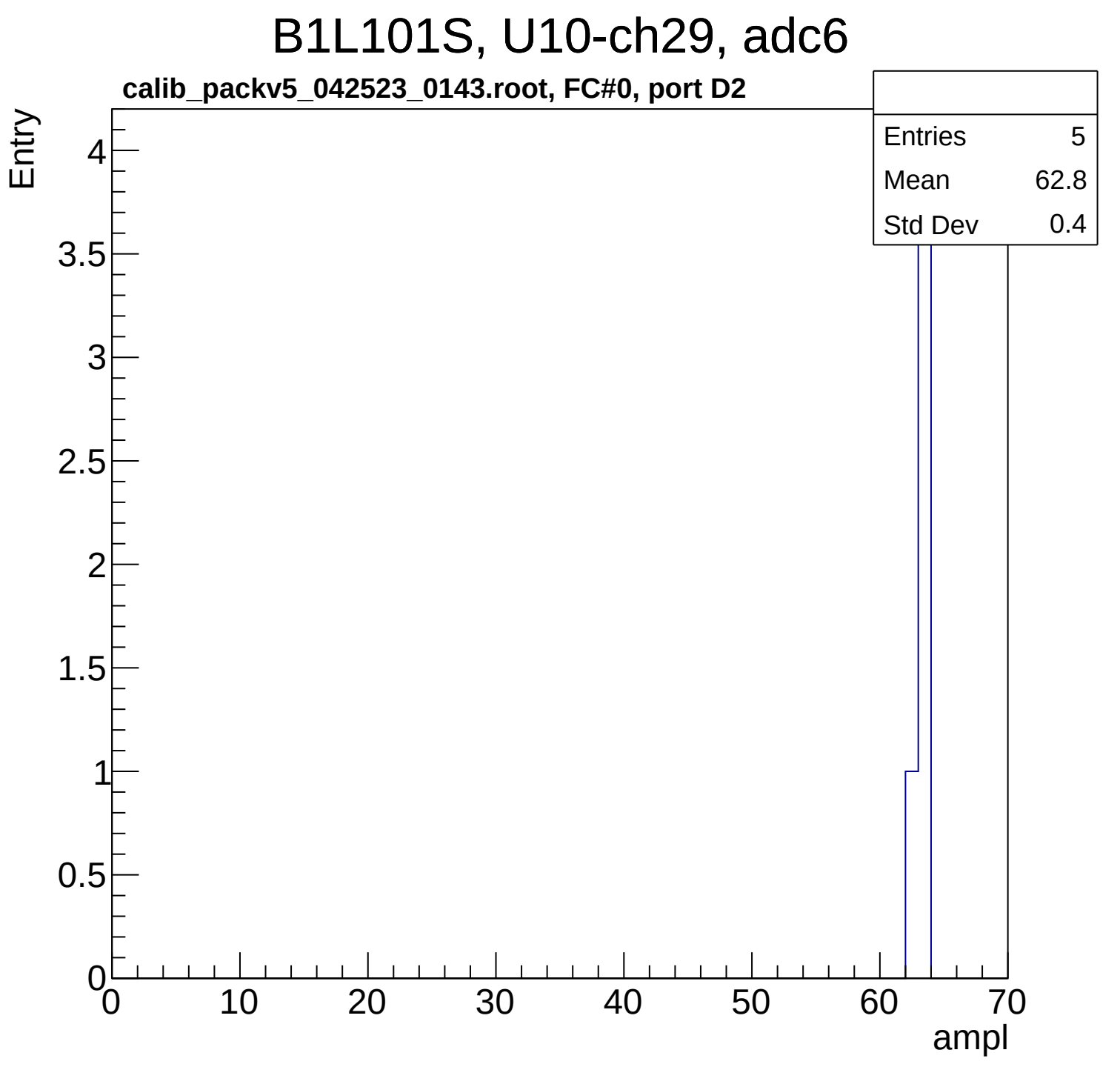
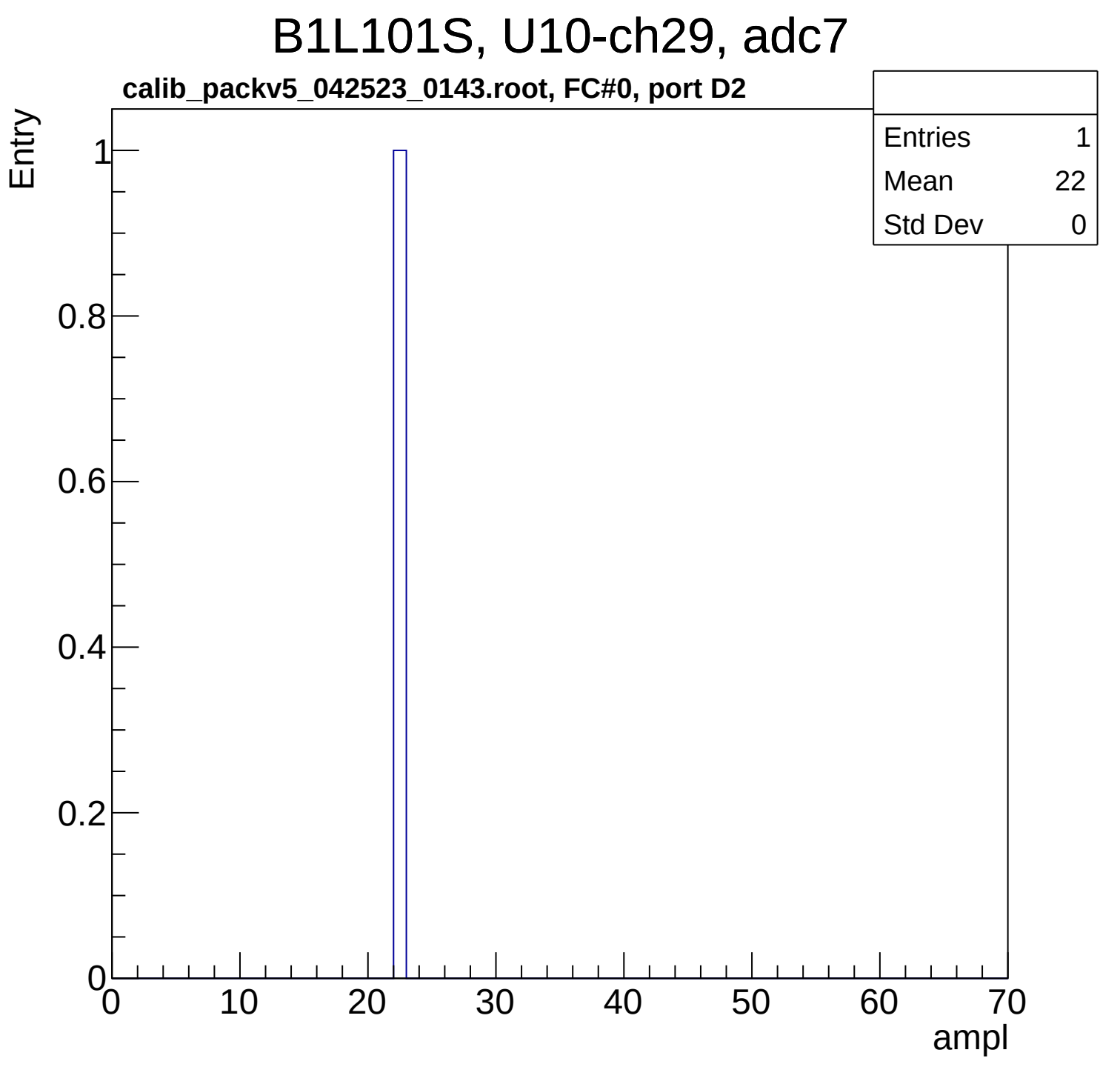

B1L101S, U10-ch29, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 62.8
Std Dev 0.4
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L101S, U10-ch29, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 22
Std Dev 0
Entry
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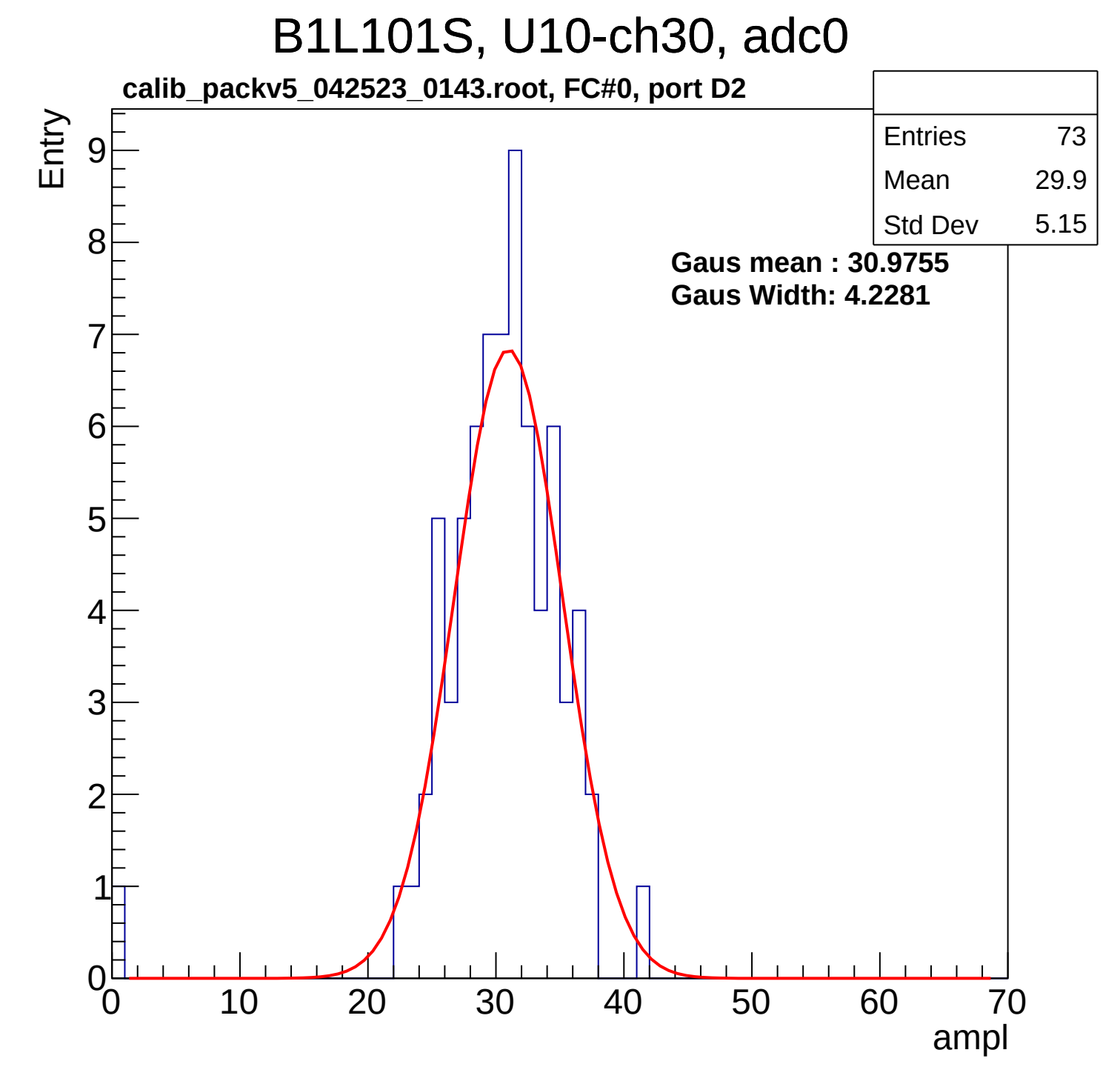
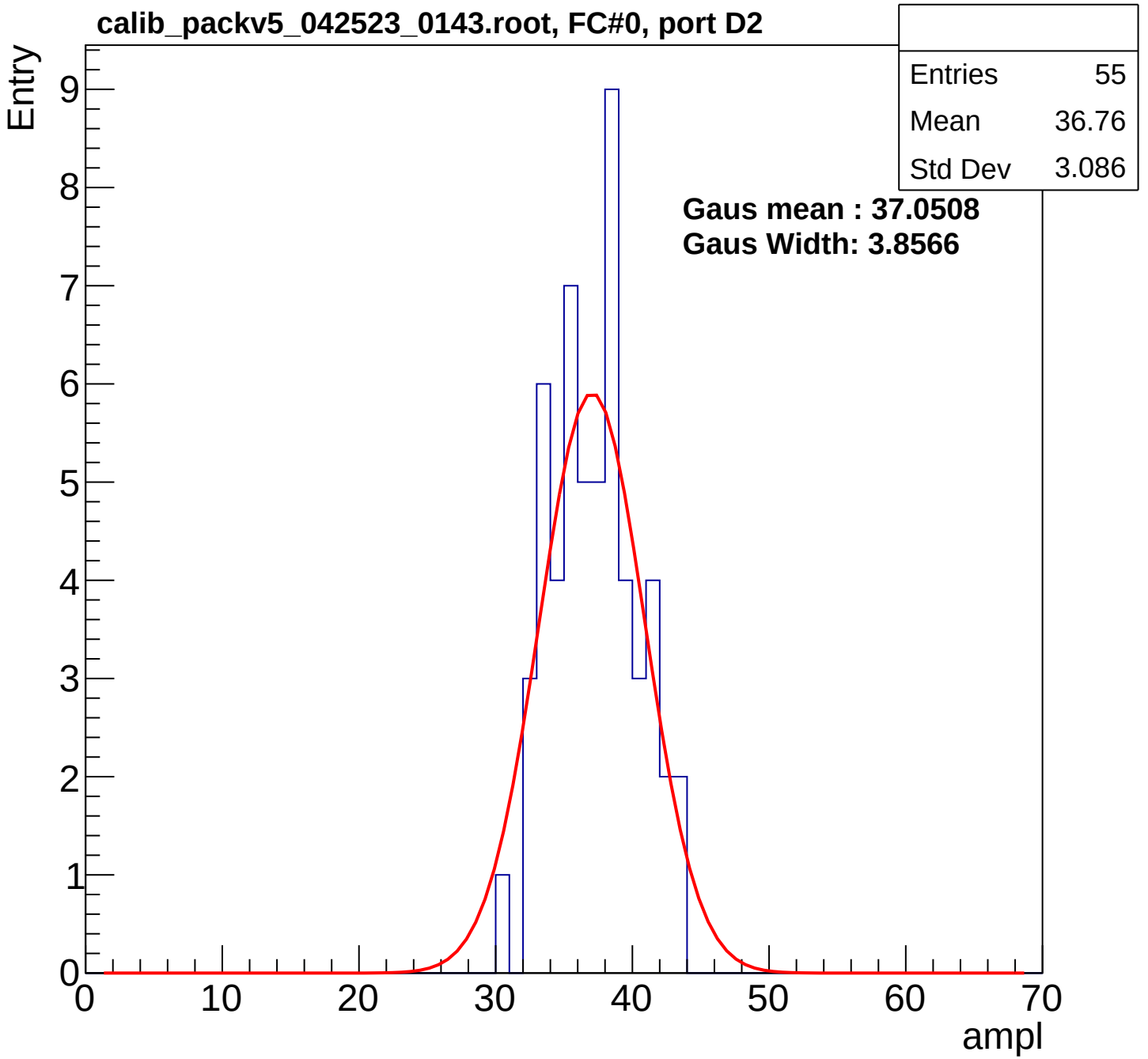
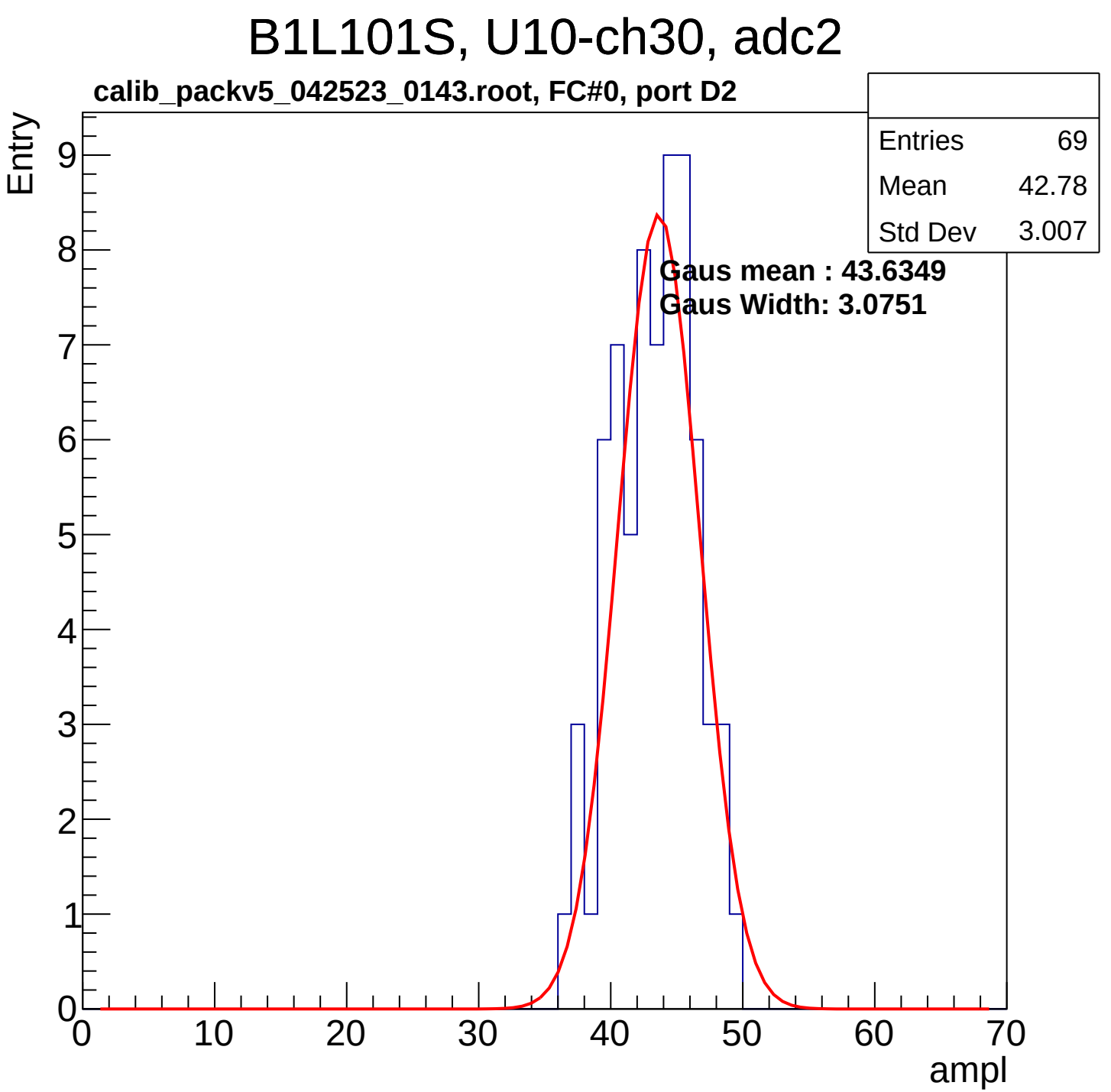
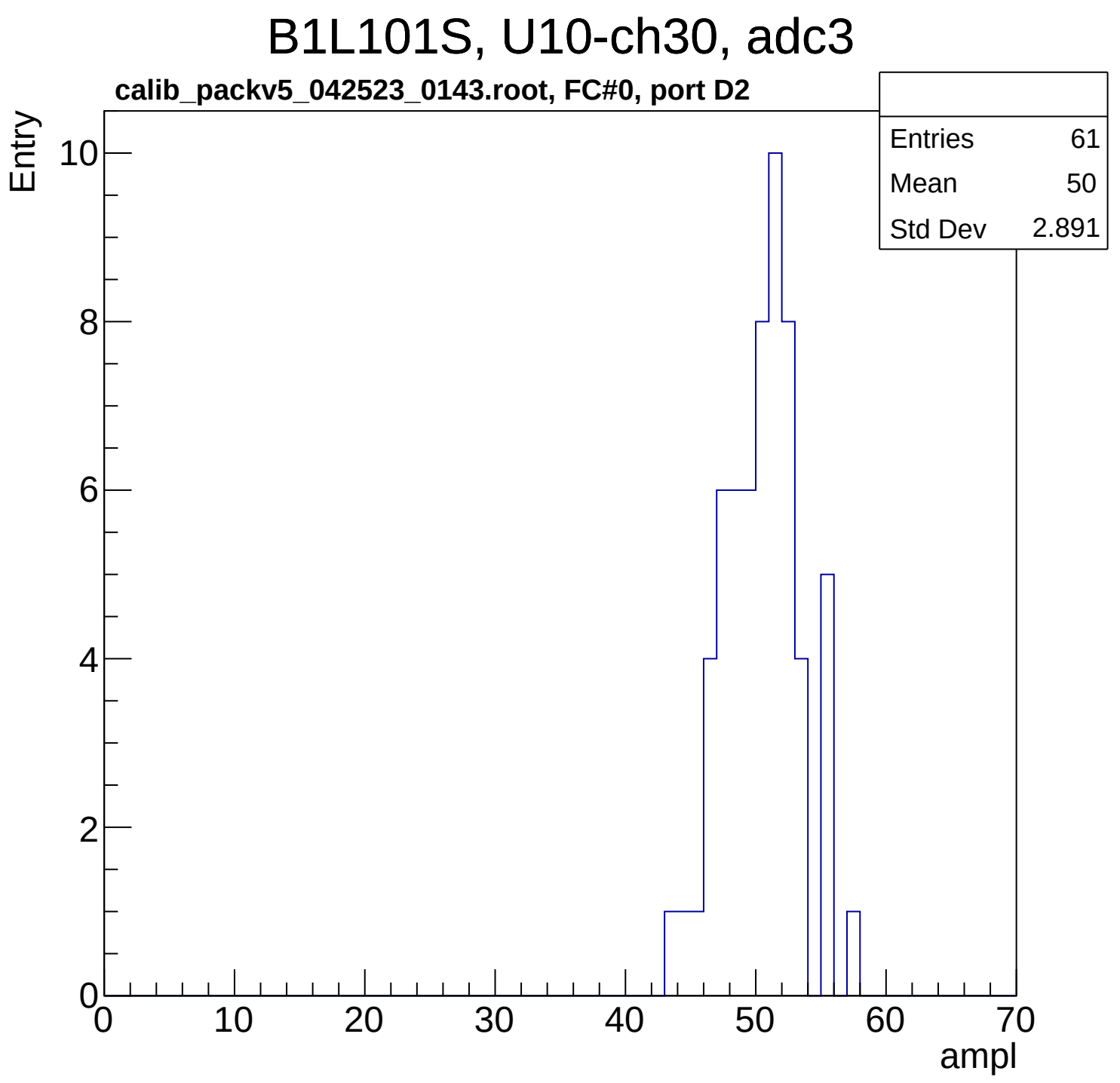
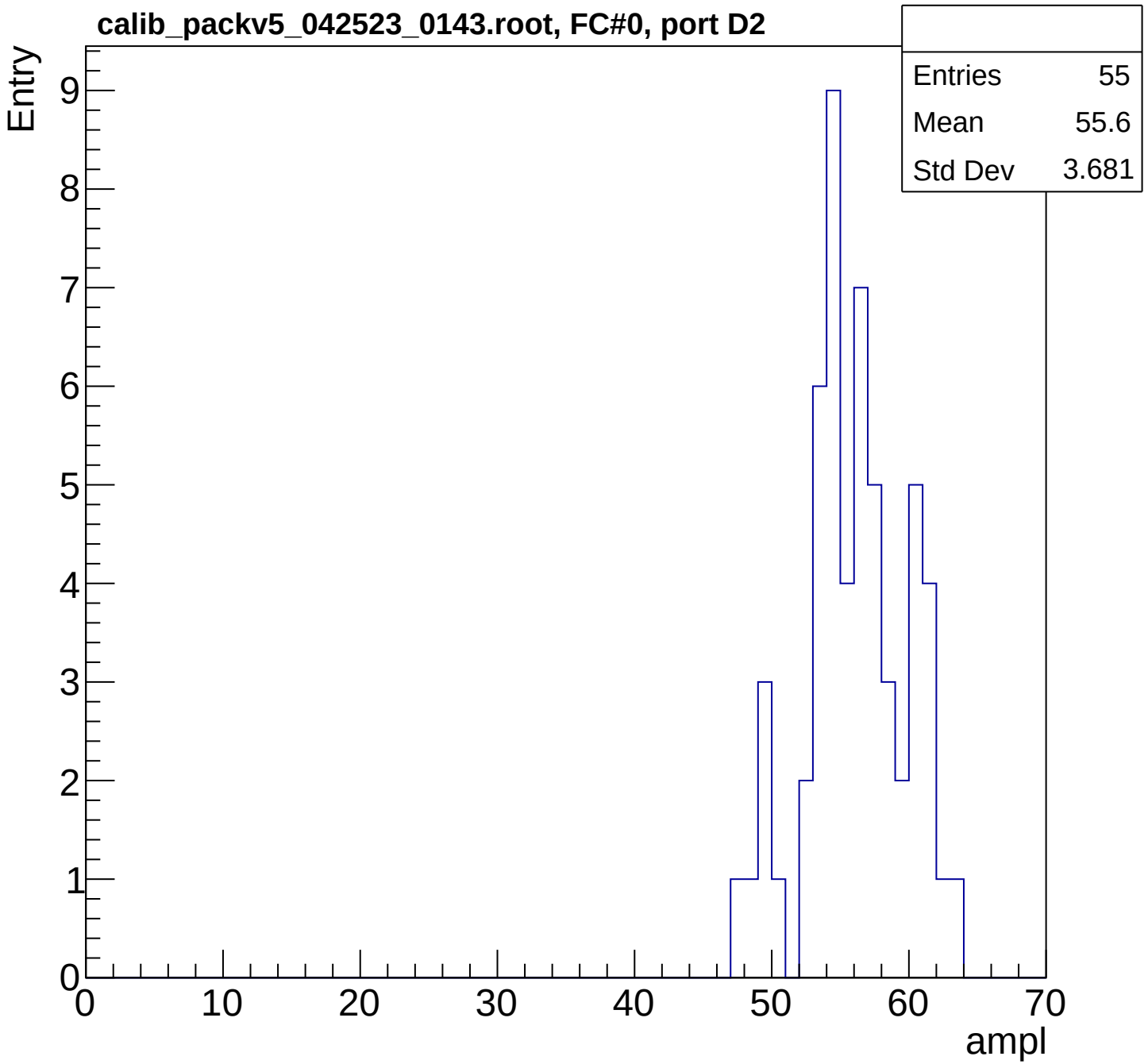
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch30, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 29.9
Std Dev 5.15
Gaus mean : 30.9755
Gaus Width: 4.2281
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch30, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 36.76
Std Dev 3.086
Gaus mean : 37.0508
Gaus Width: 3.8566
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch30, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 42.78
Std Dev 3.007
Gaus mean : 43.6349
Gaus Width: 3.0751
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch30, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 50
Std Dev 2.891
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch30, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 55.6
Std Dev 3.681
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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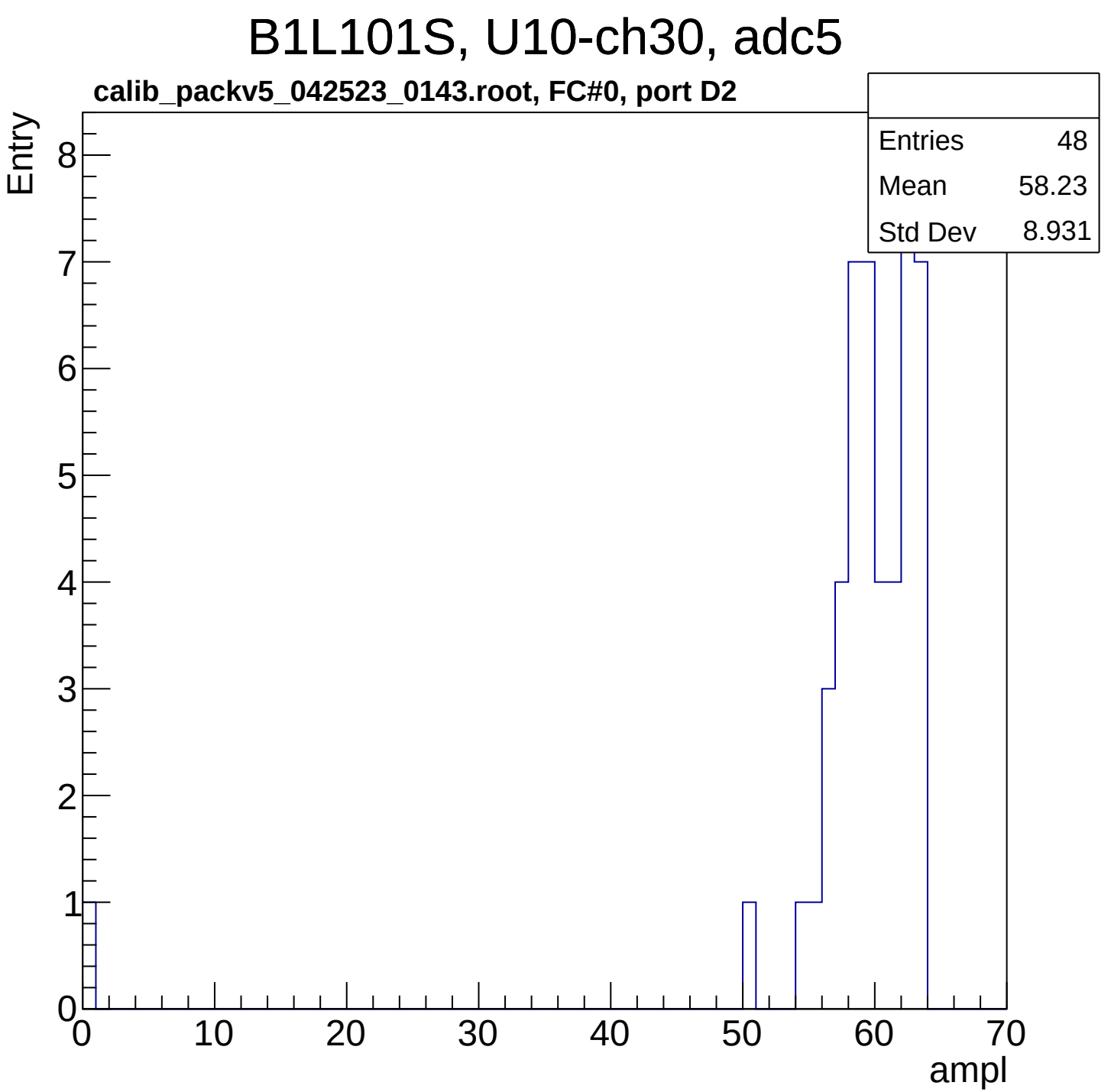
40
50
60
70


B1L101S, U10-ch30, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 58.23
Std Dev 8.931
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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40
50
60
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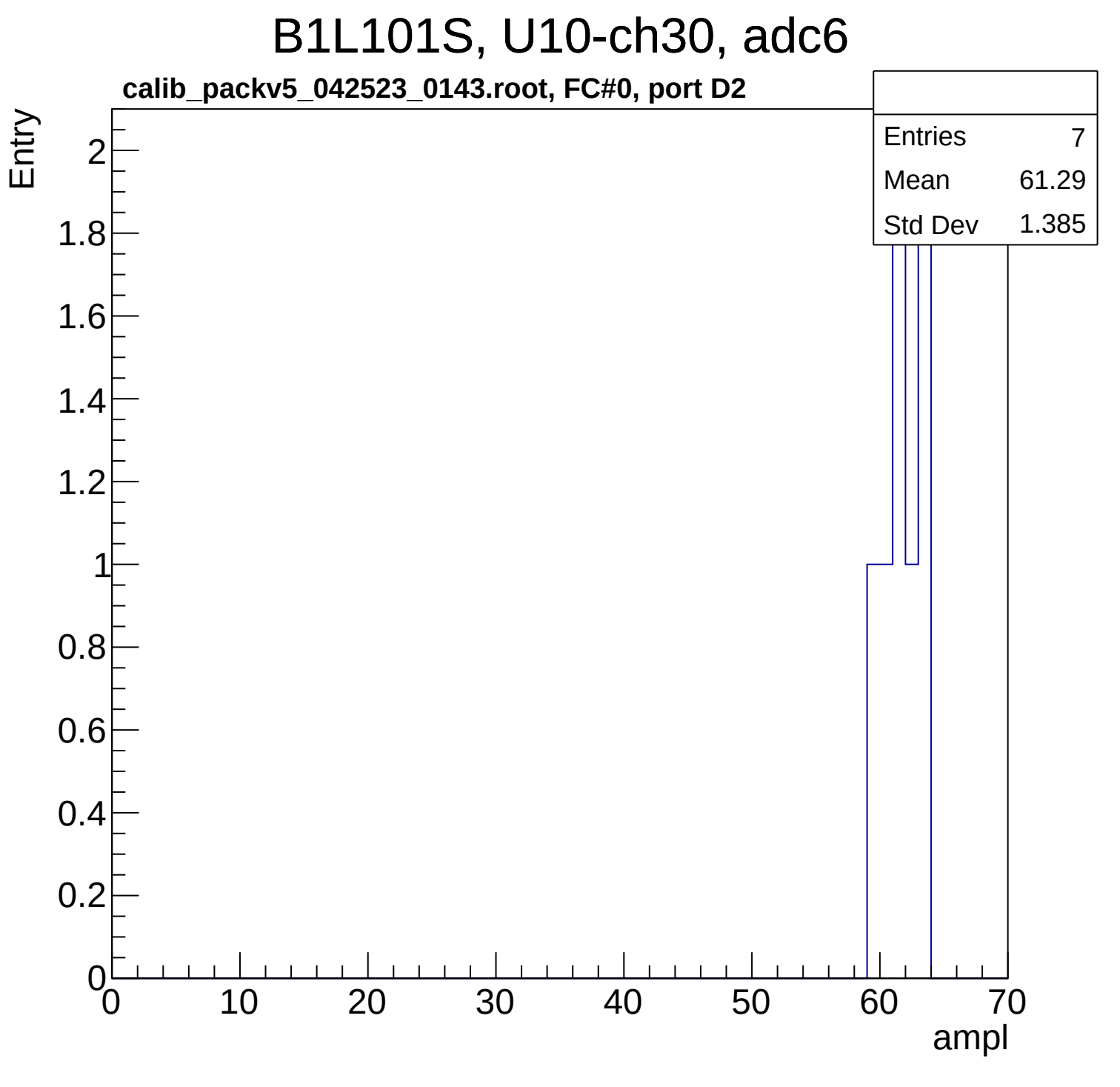
B1L101S, U10-ch30, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 61.29
Std Dev 1.385
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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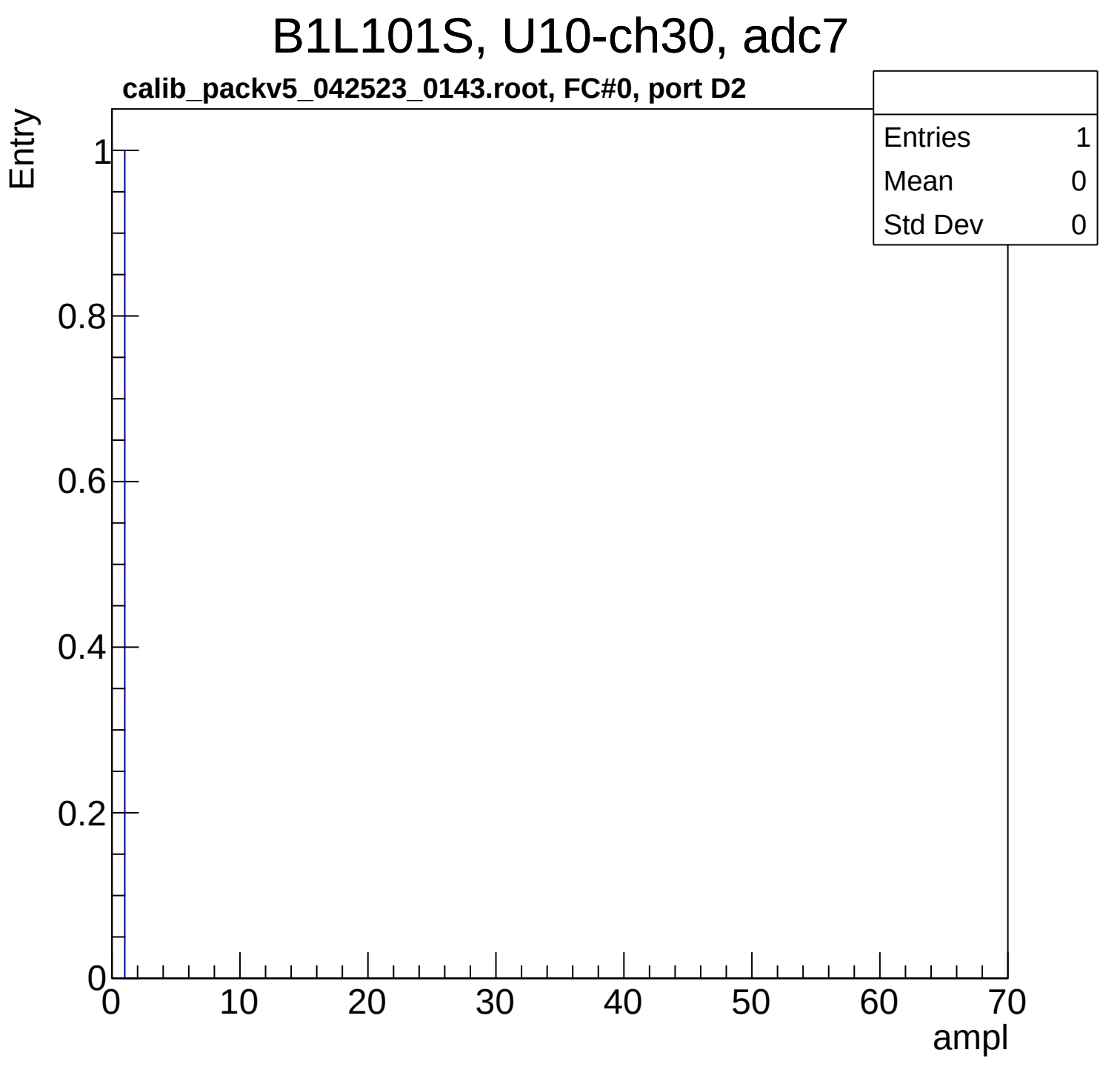
40
50
60
70


B1L101S, U10-ch30, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
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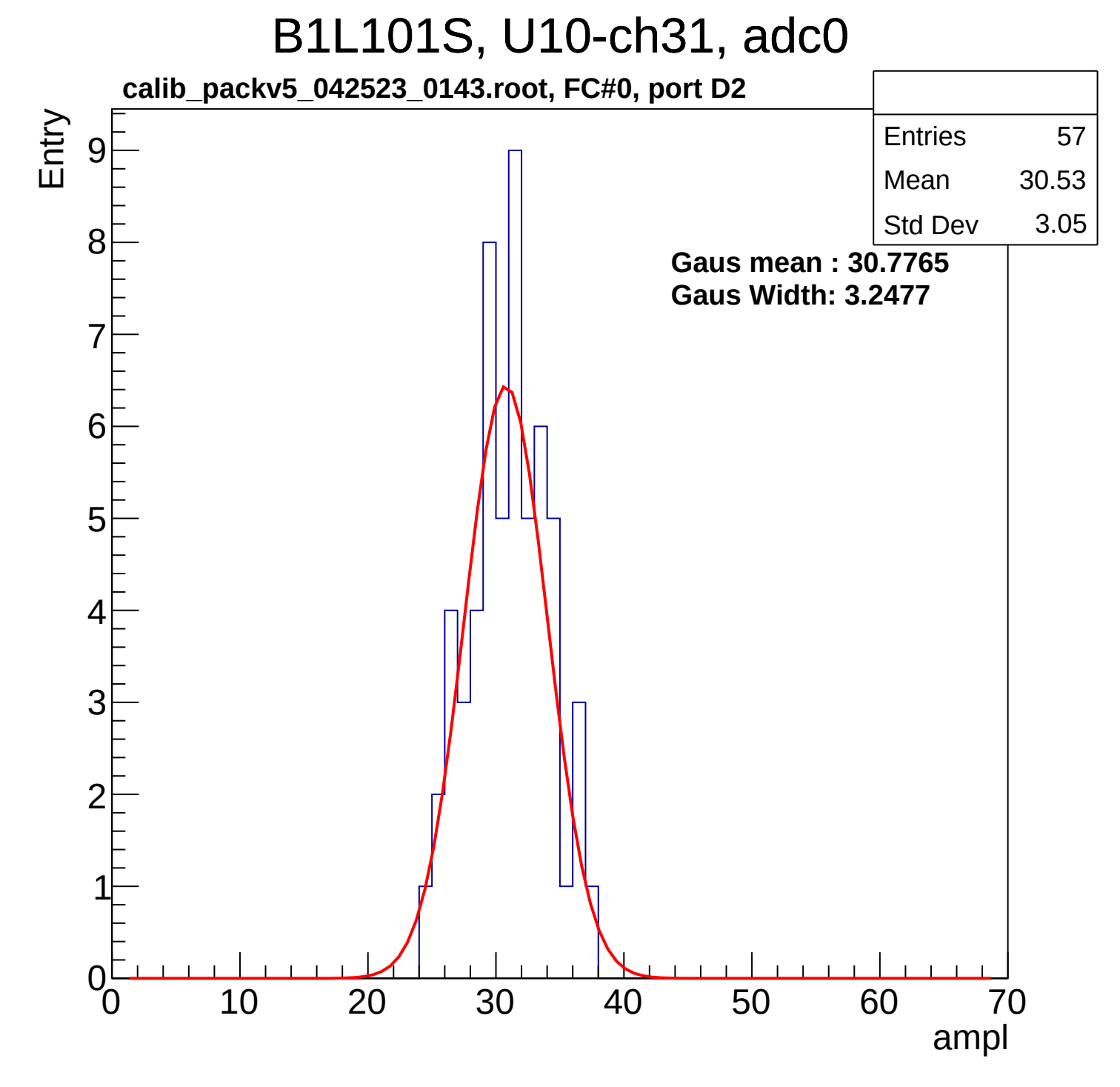
50
60
70
ampl


B1L101S, U10-ch31, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 30.53
Std Dev 3.05
Gaus mean : 30.7765
Gaus Width: 3.2477
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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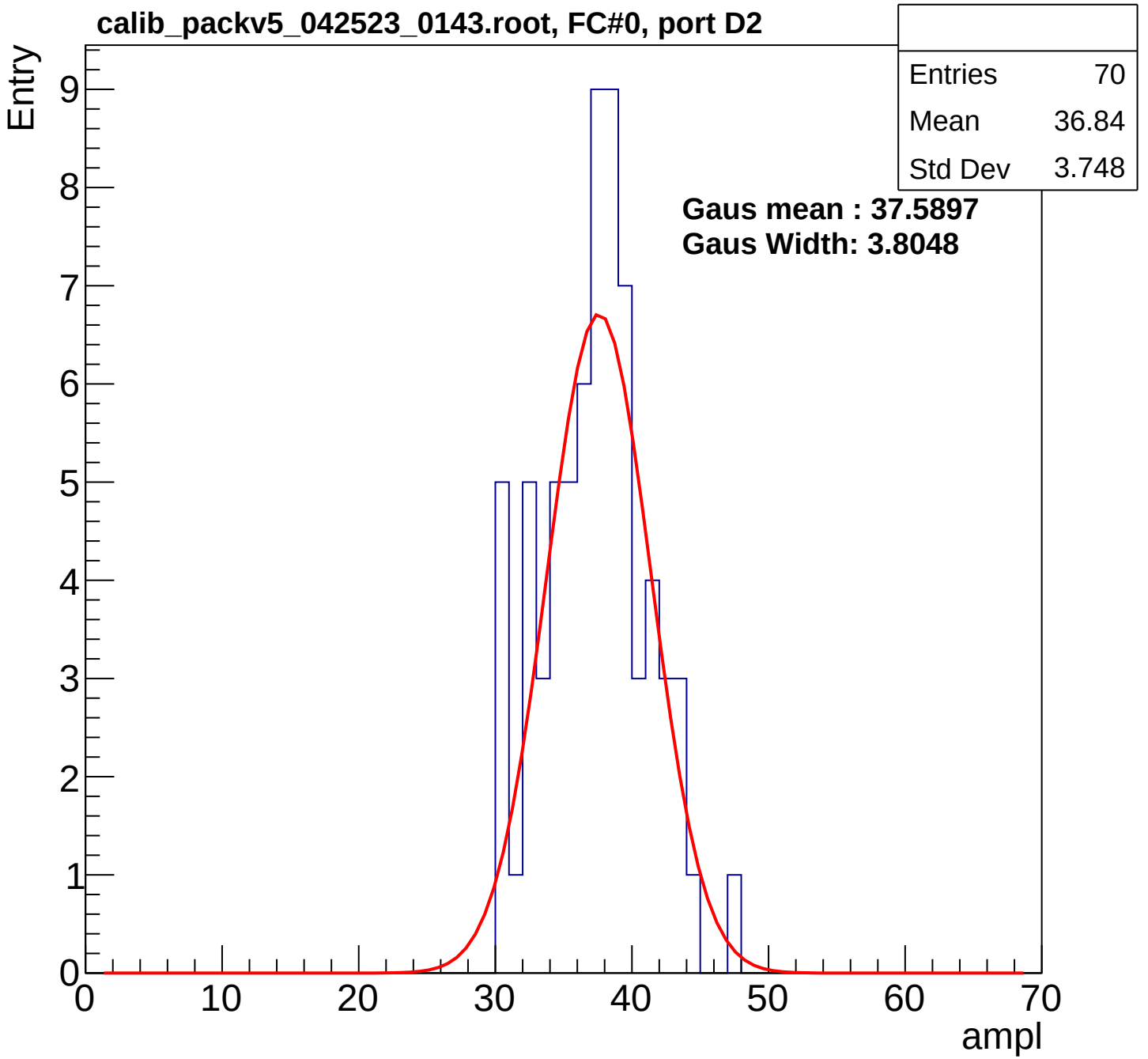
B1L101S, U10-ch31, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 36.84
Std Dev 3.748
Gaus mean : 37.5897
Gaus Width: 3.8048
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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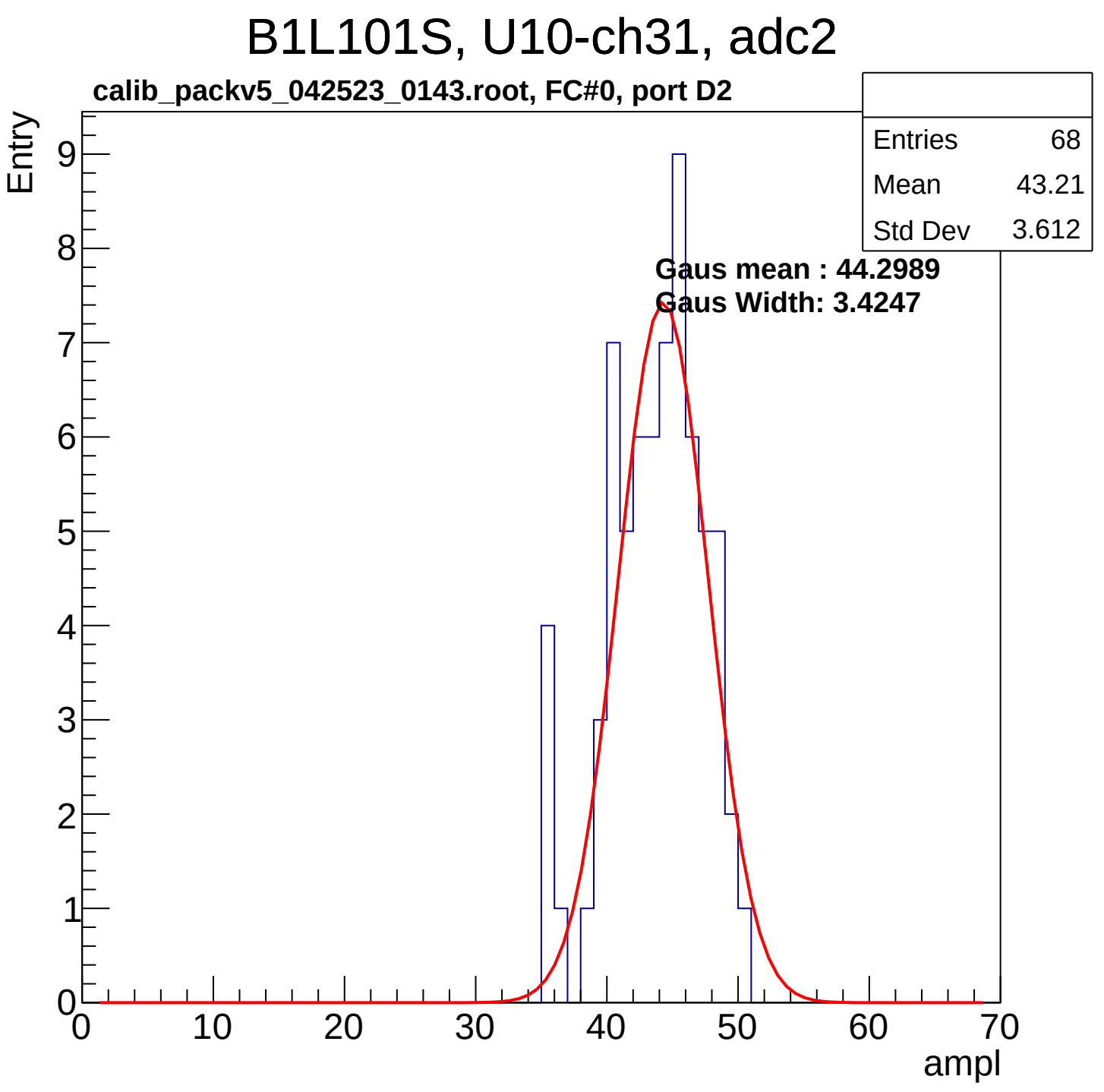
B1L101S, U10-ch31, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 43.21
Std Dev 3.612
Gaus mean : 44.2989
Gaus Width: 3.4247
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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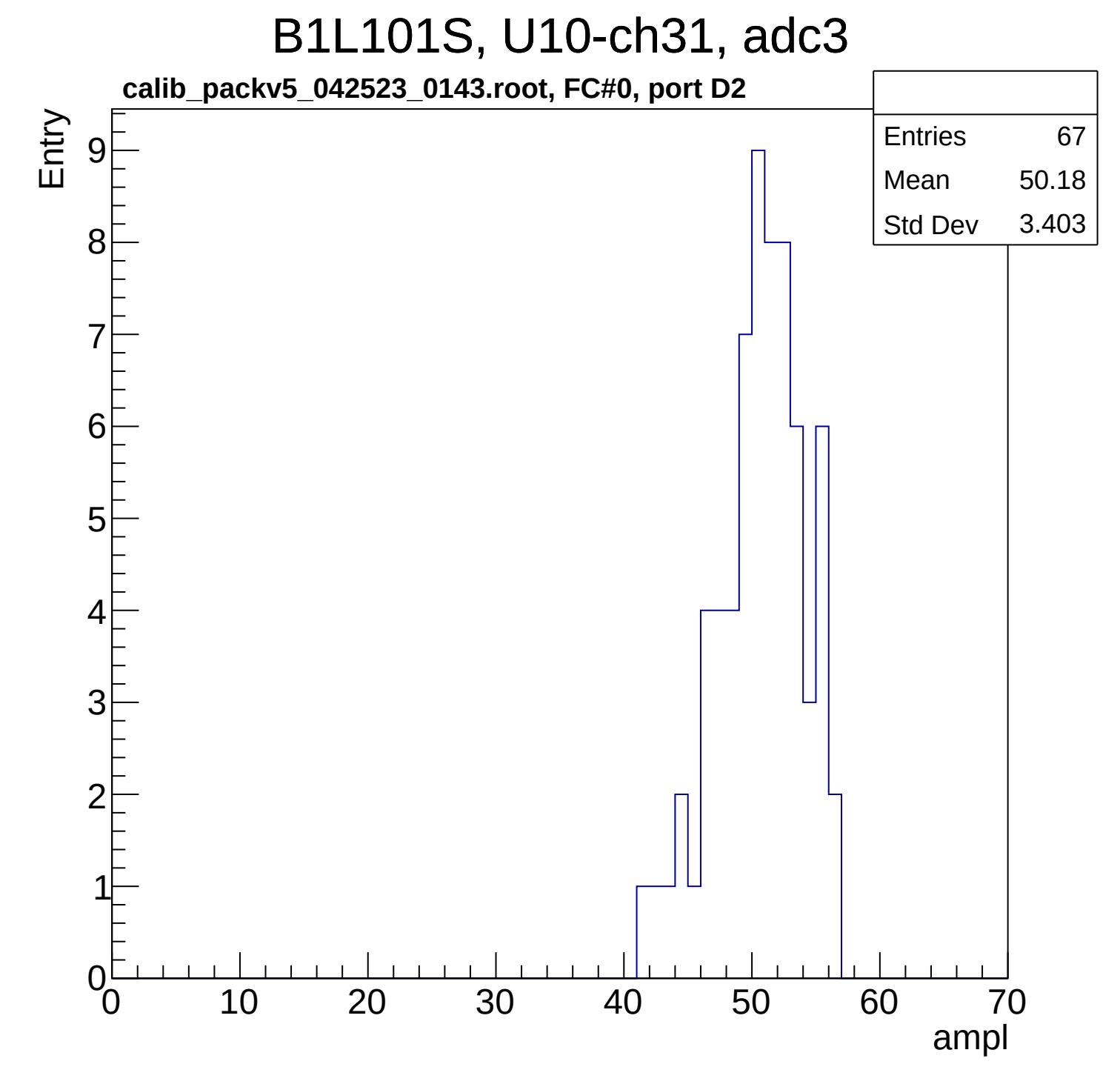
B1L101S, U10-ch31, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 50.18
Std Dev 3.403
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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30
40
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60
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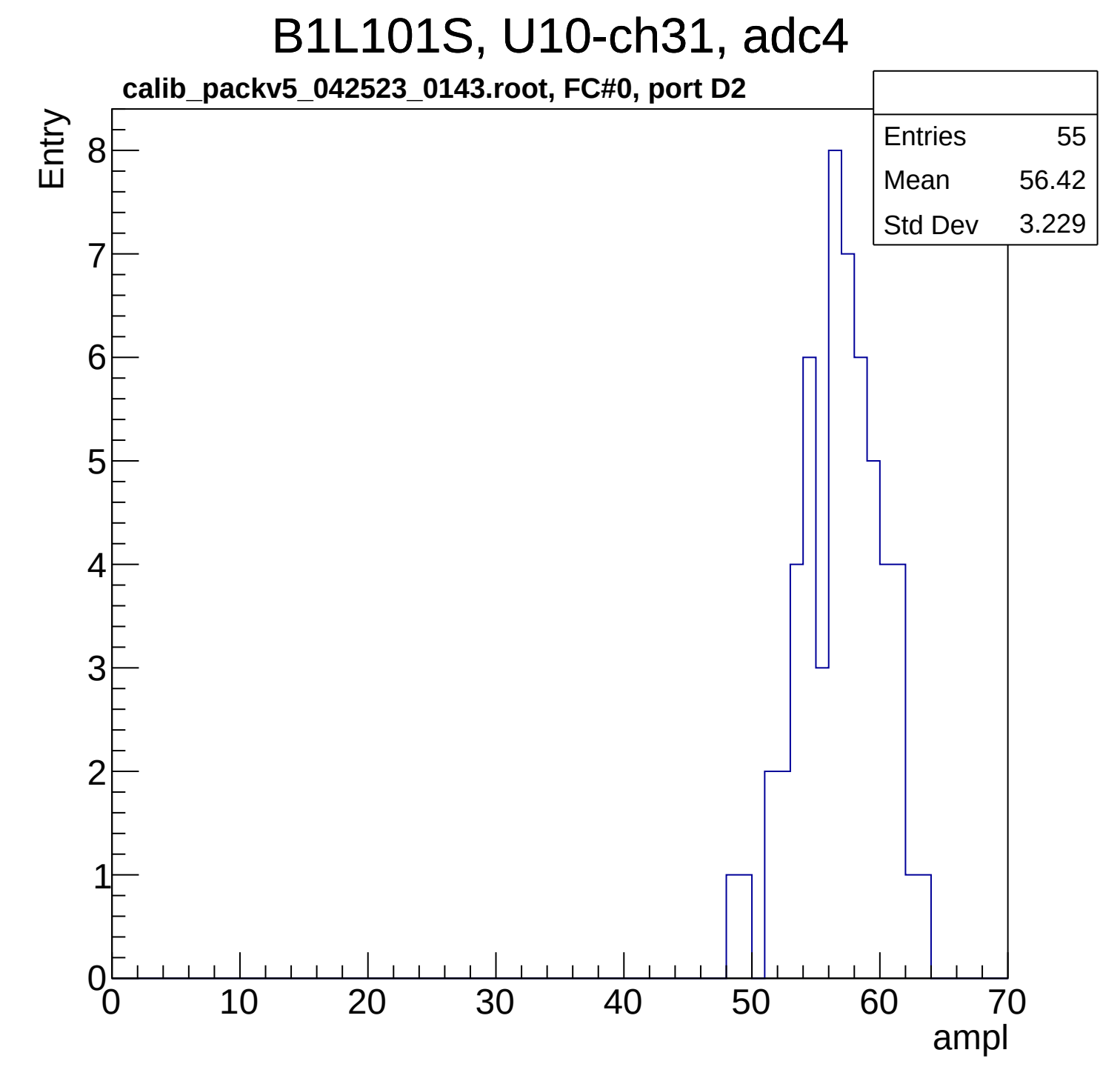
B1L101S, U10-ch31, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 56.42
Std Dev 3.229
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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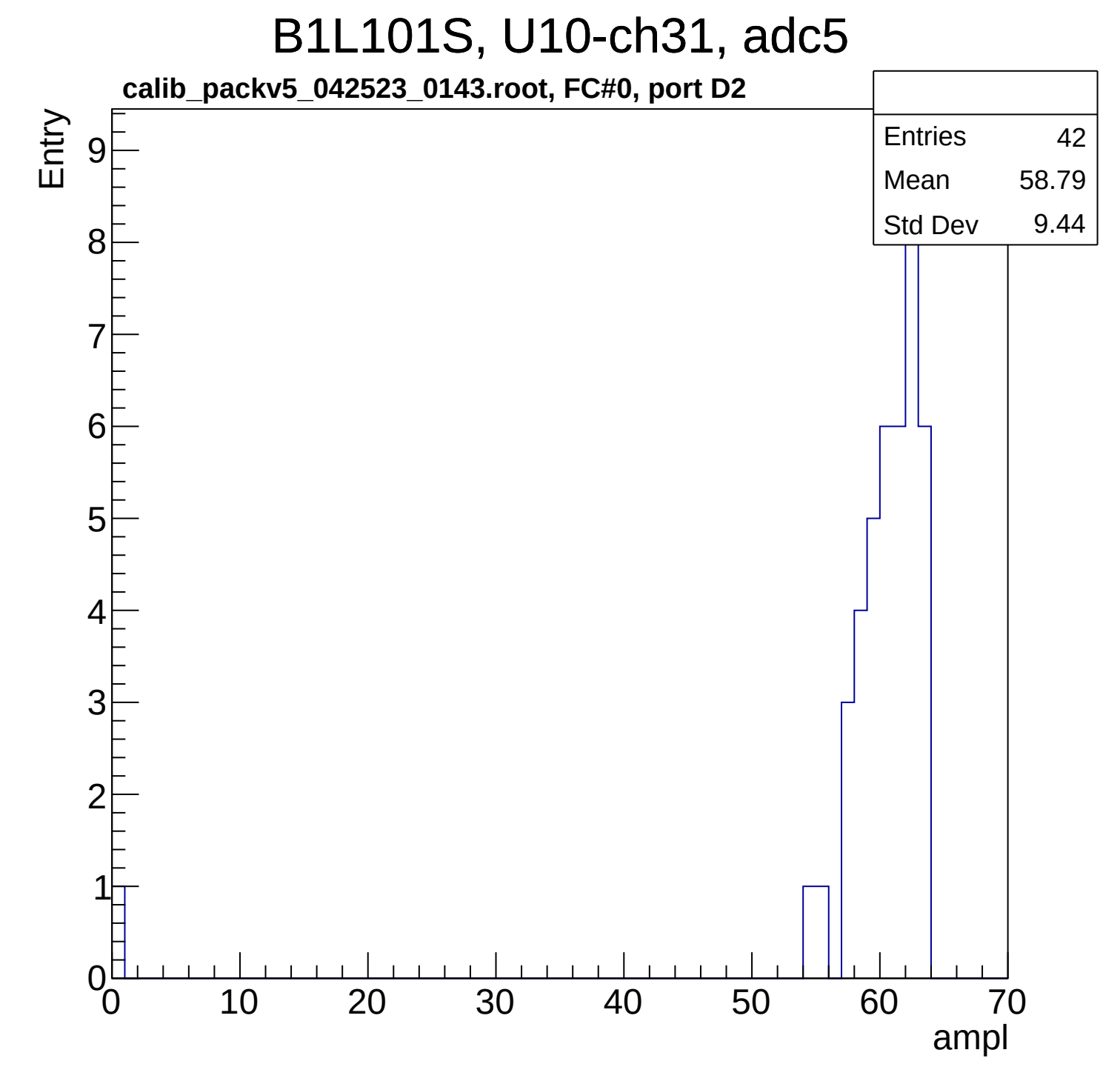
B1L101S, U10-ch31, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 58.79
Std Dev 9.44
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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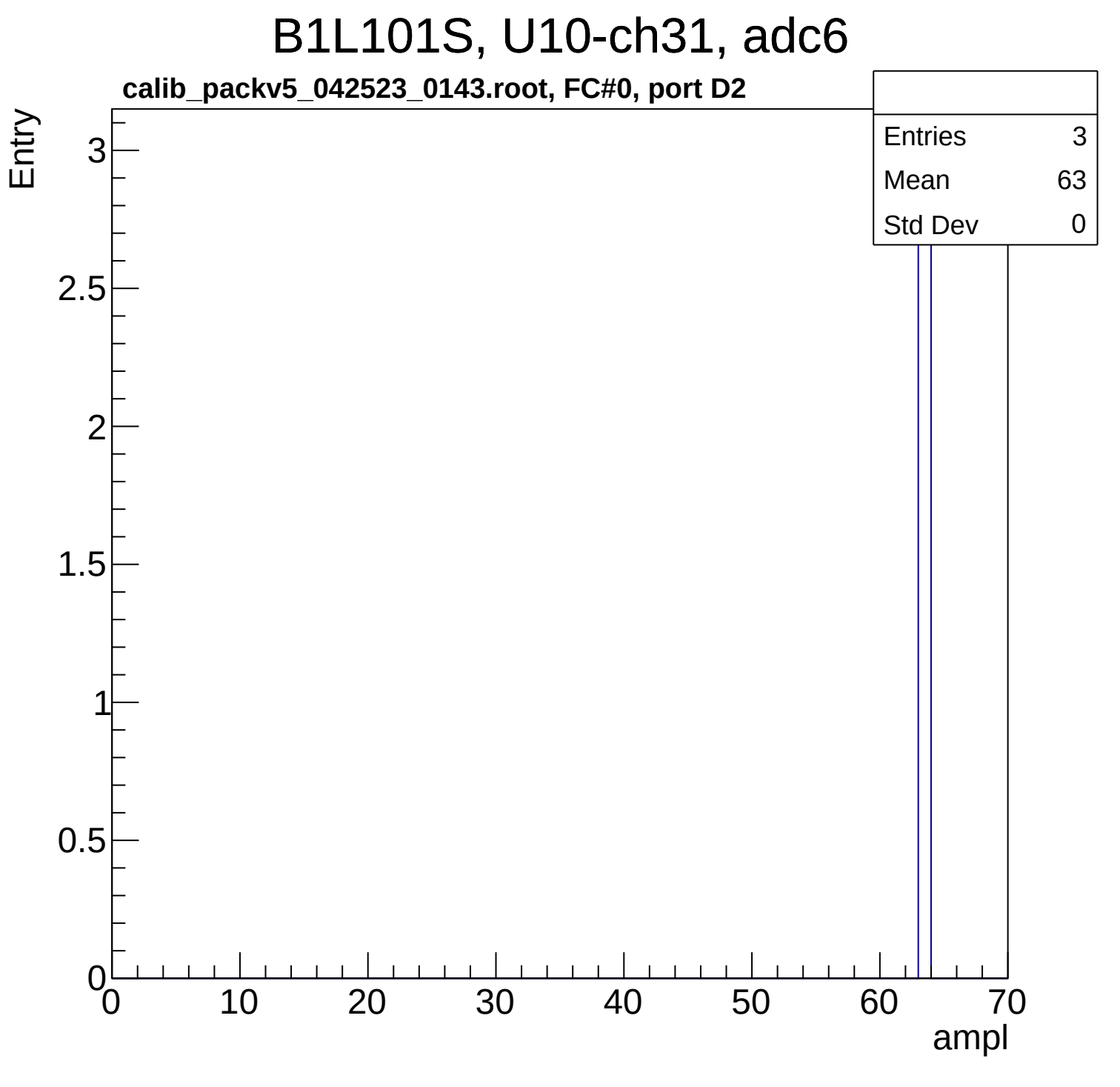
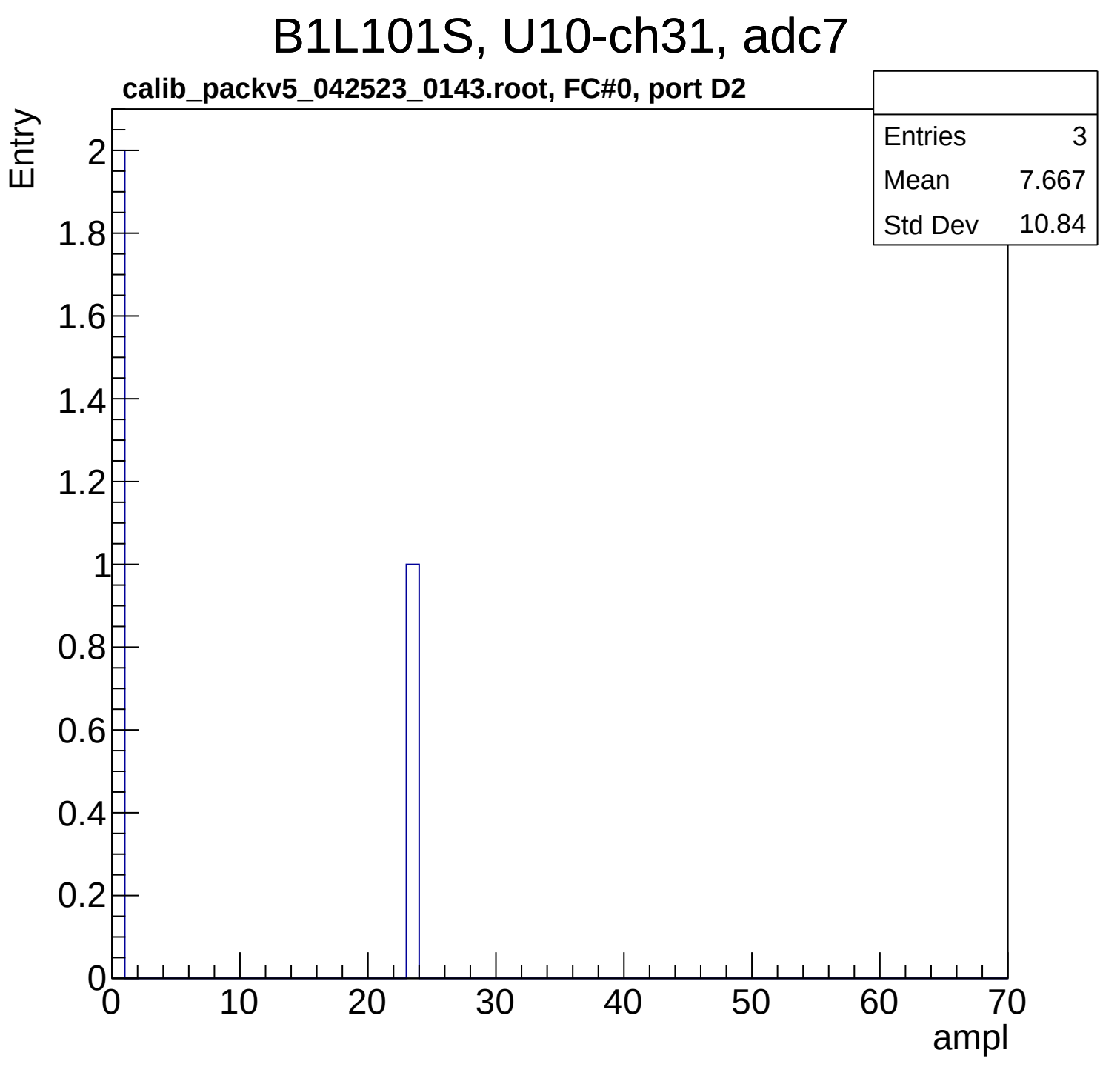

B1L101S, U10-ch31, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 63
Std Dev 0
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U10-ch31, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 7.667
Std Dev 10.84
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
50
60
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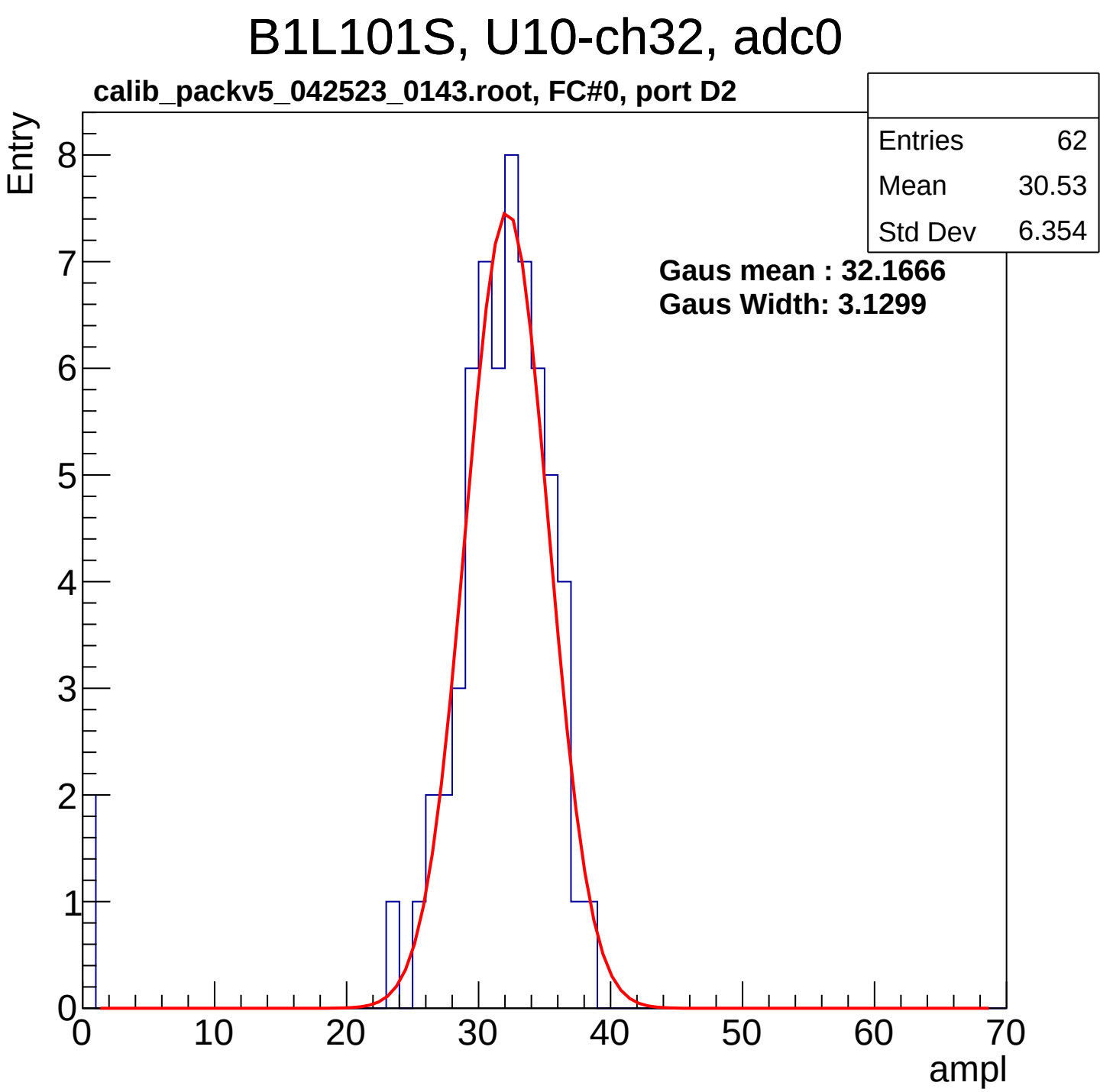
B1L101S, U10-ch32, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 30.53
Std Dev 6.354
Gaus mean : 32.1666
Gaus Width: 3.1299
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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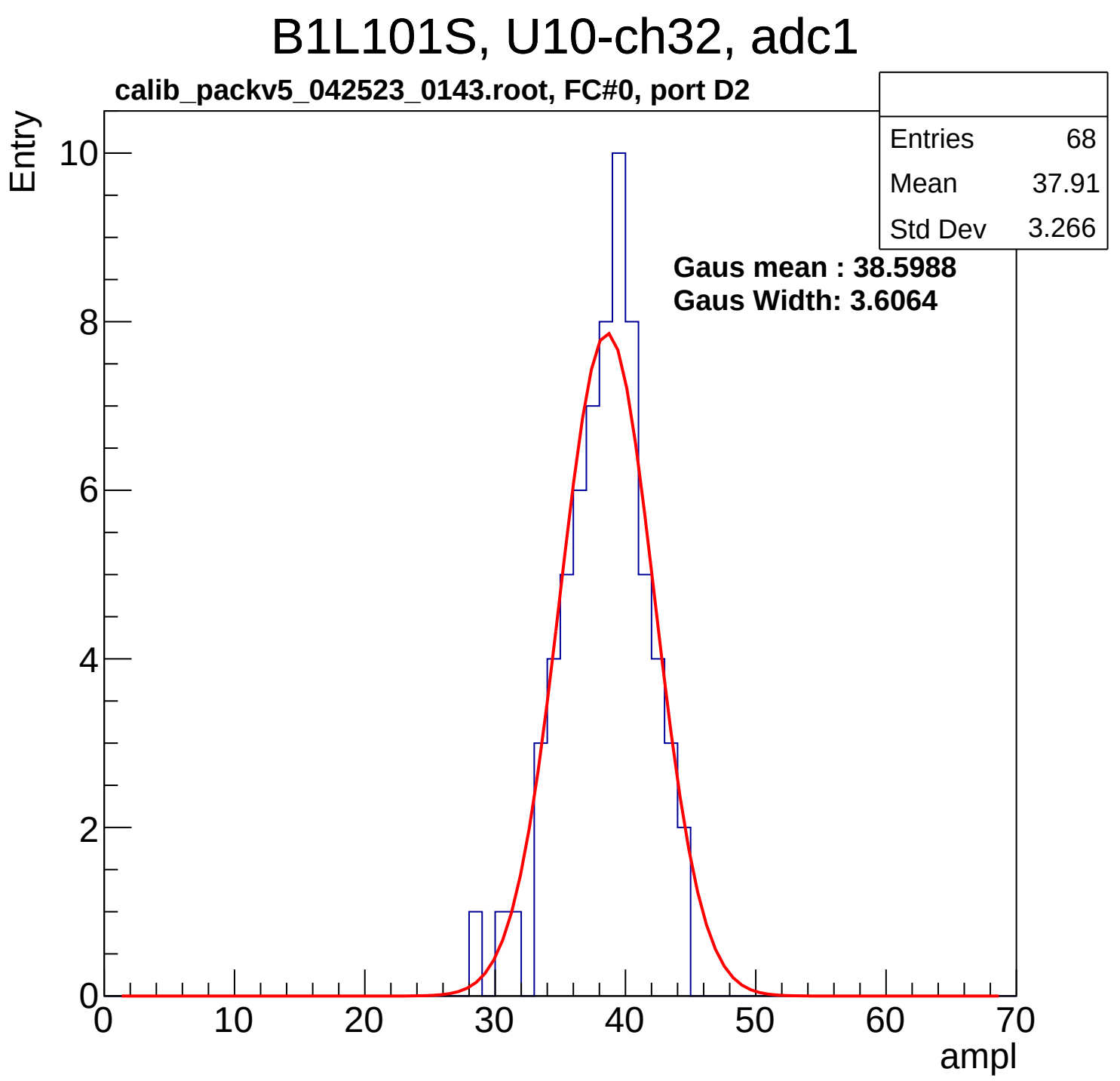
B1L101S, U10-ch32, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 37.91
Std Dev 3.266
Gaus mean : 38.5988
Gaus Width: 3.6064
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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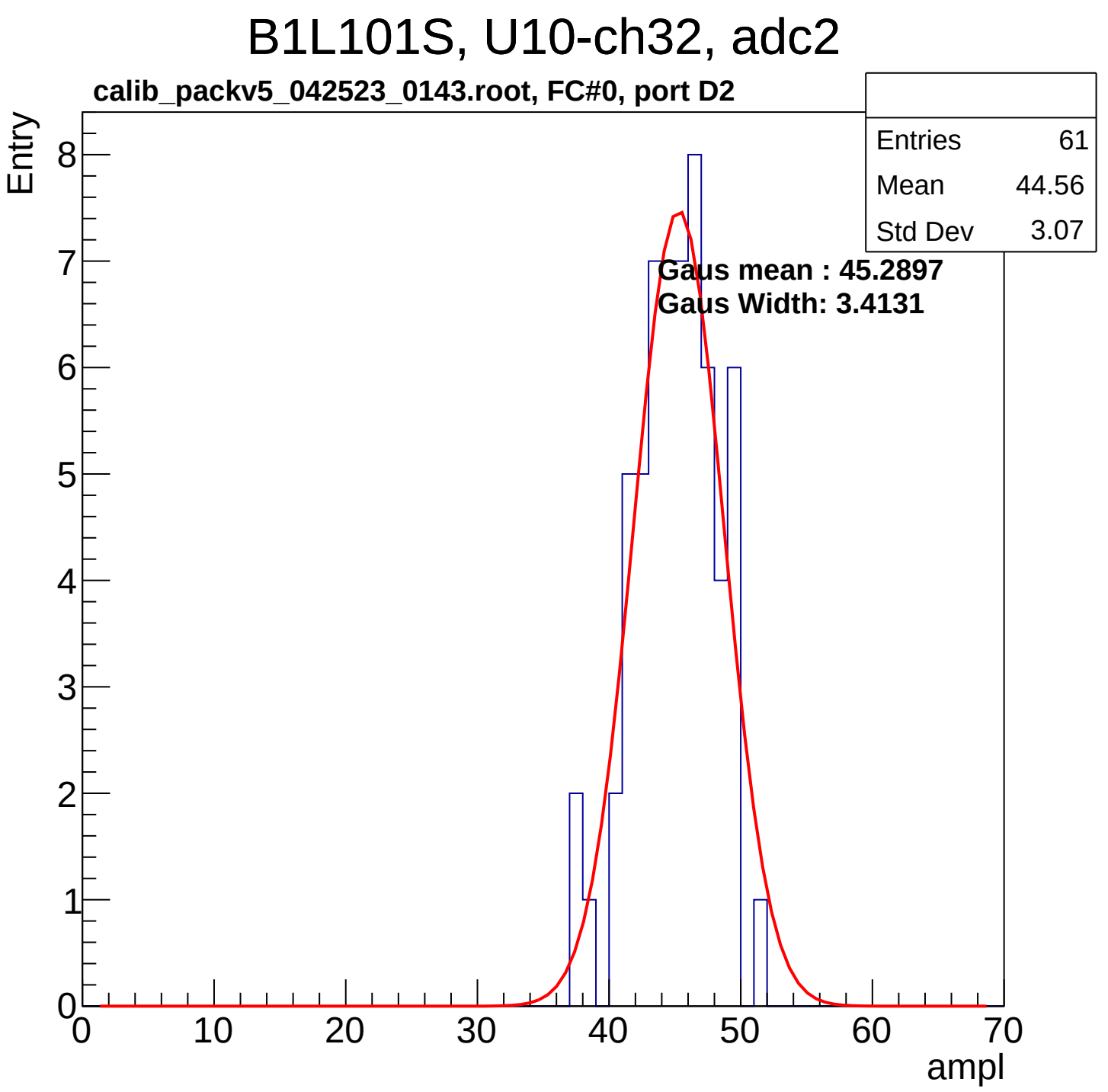
B1L101S, U10-ch32, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 44.56
Std Dev 3.07
Gaus mean : 45.2897
Gaus Width: 3.4131
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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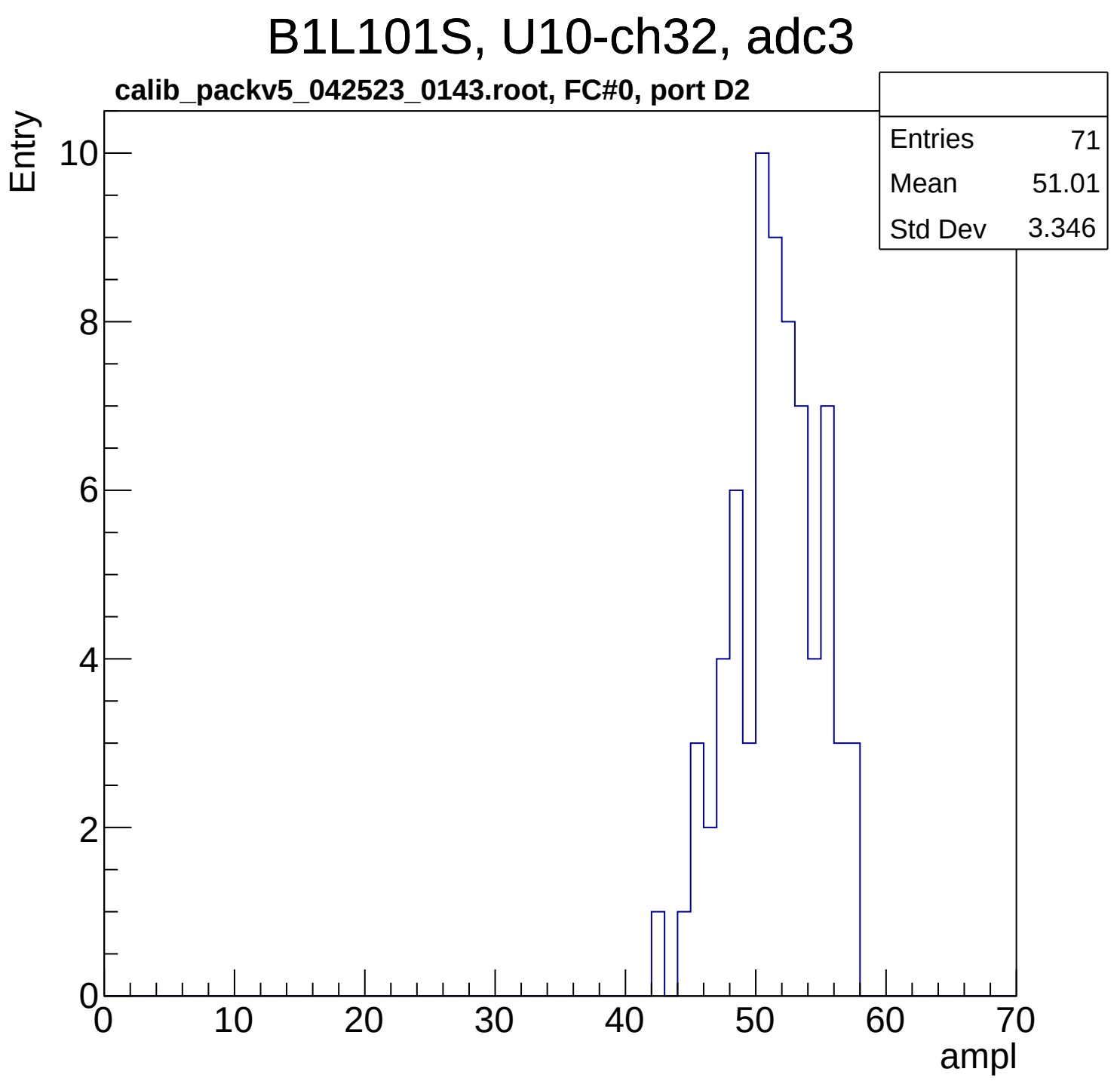
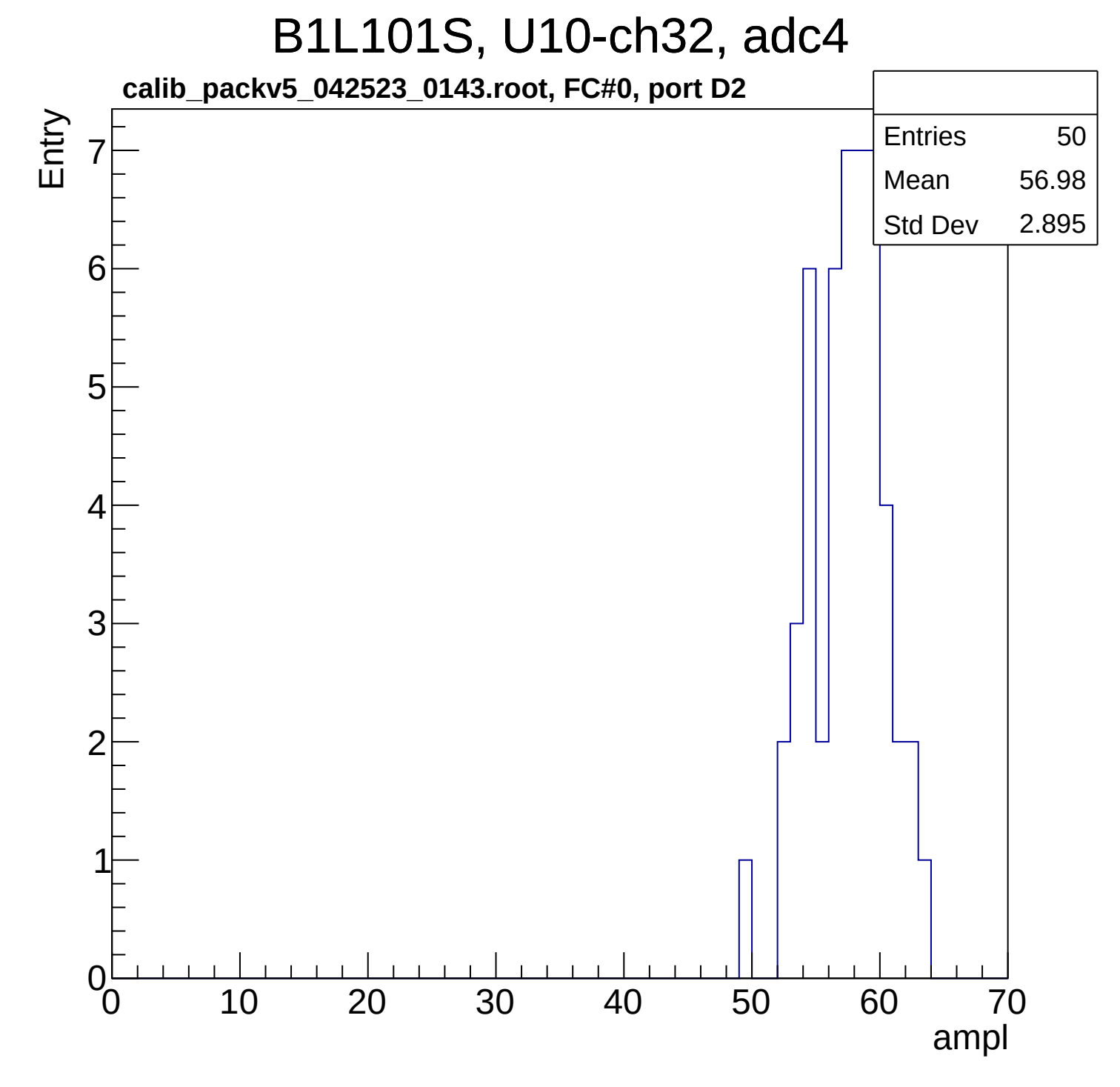

B1L101S, U10-ch32, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 51.01
Std Dev 3.346
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch32, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 56.98
Std Dev 2.895
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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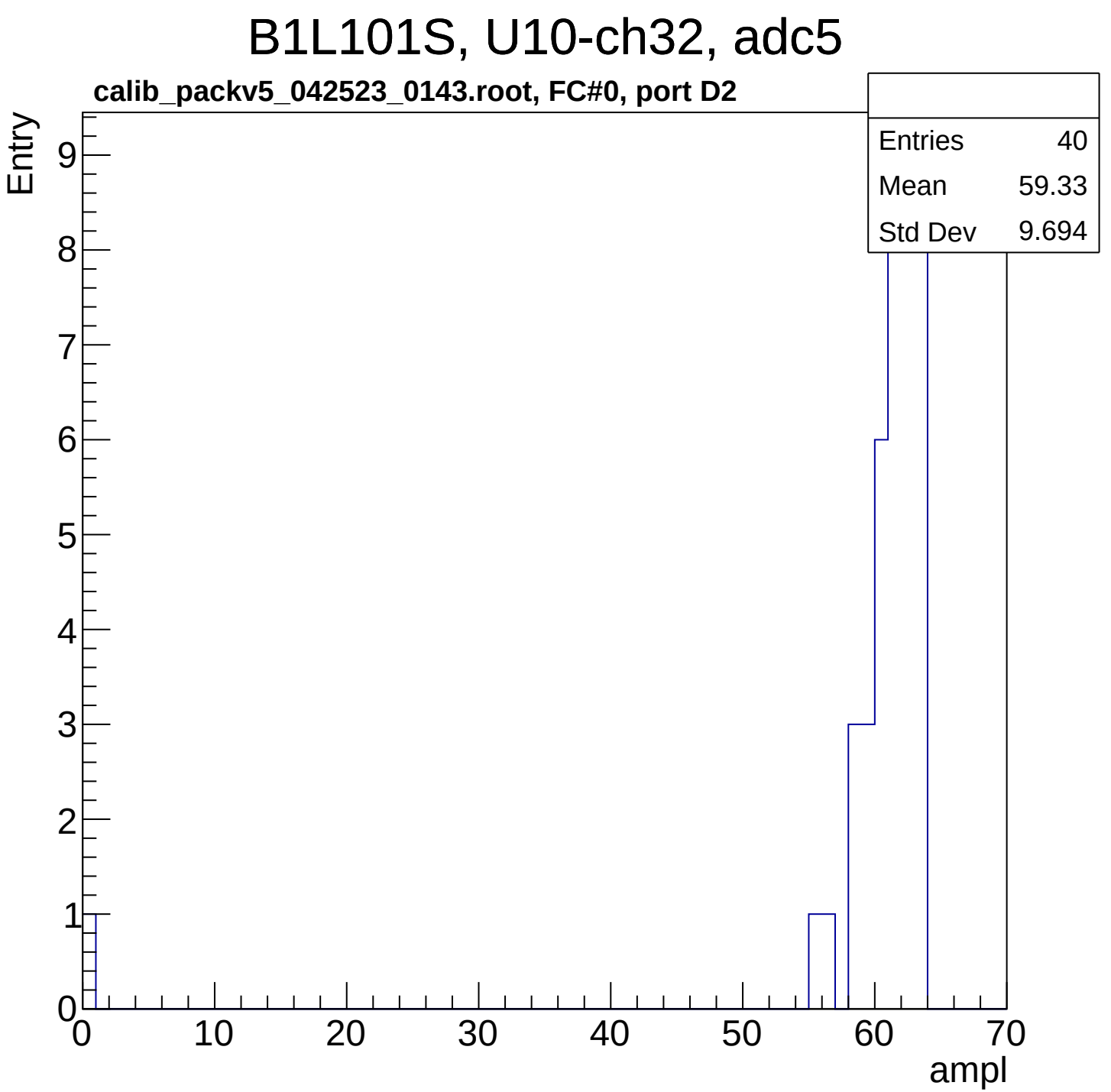
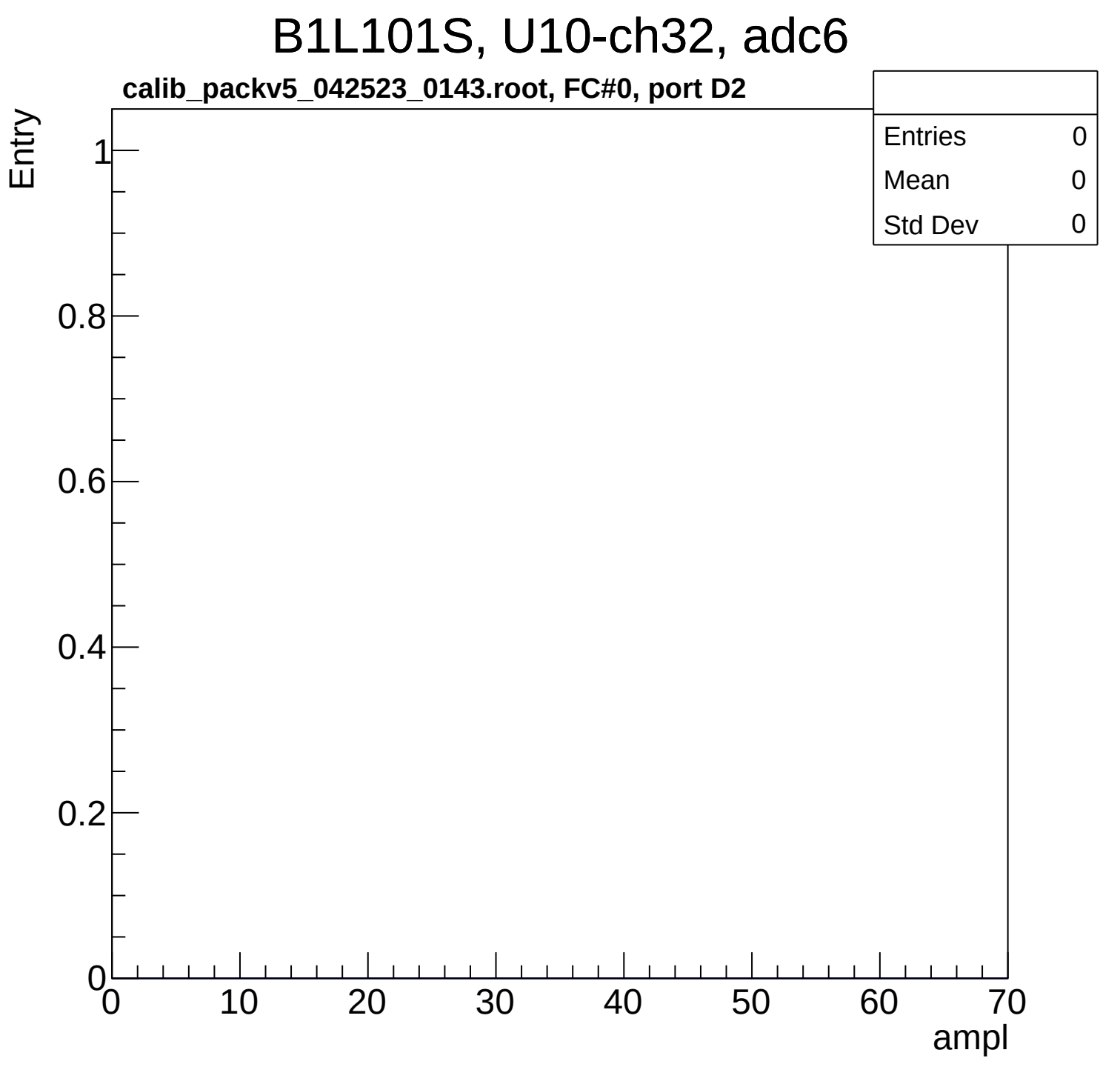
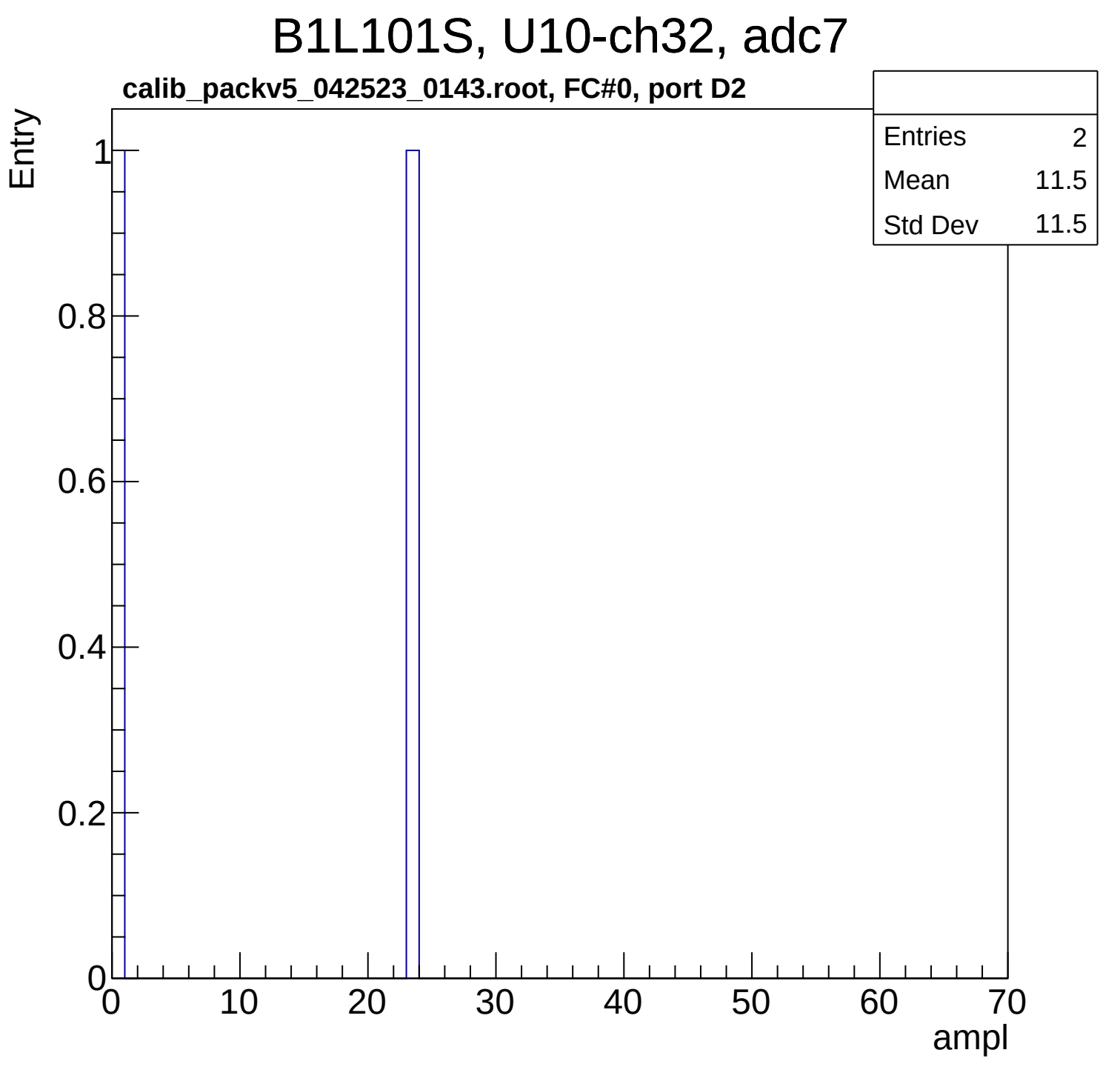

B1L101S, U10-ch32, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 40
Mean 59.33
Std Dev 9.694
Entry
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch32, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch32, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 11.5
Std Dev 11.5
Entry
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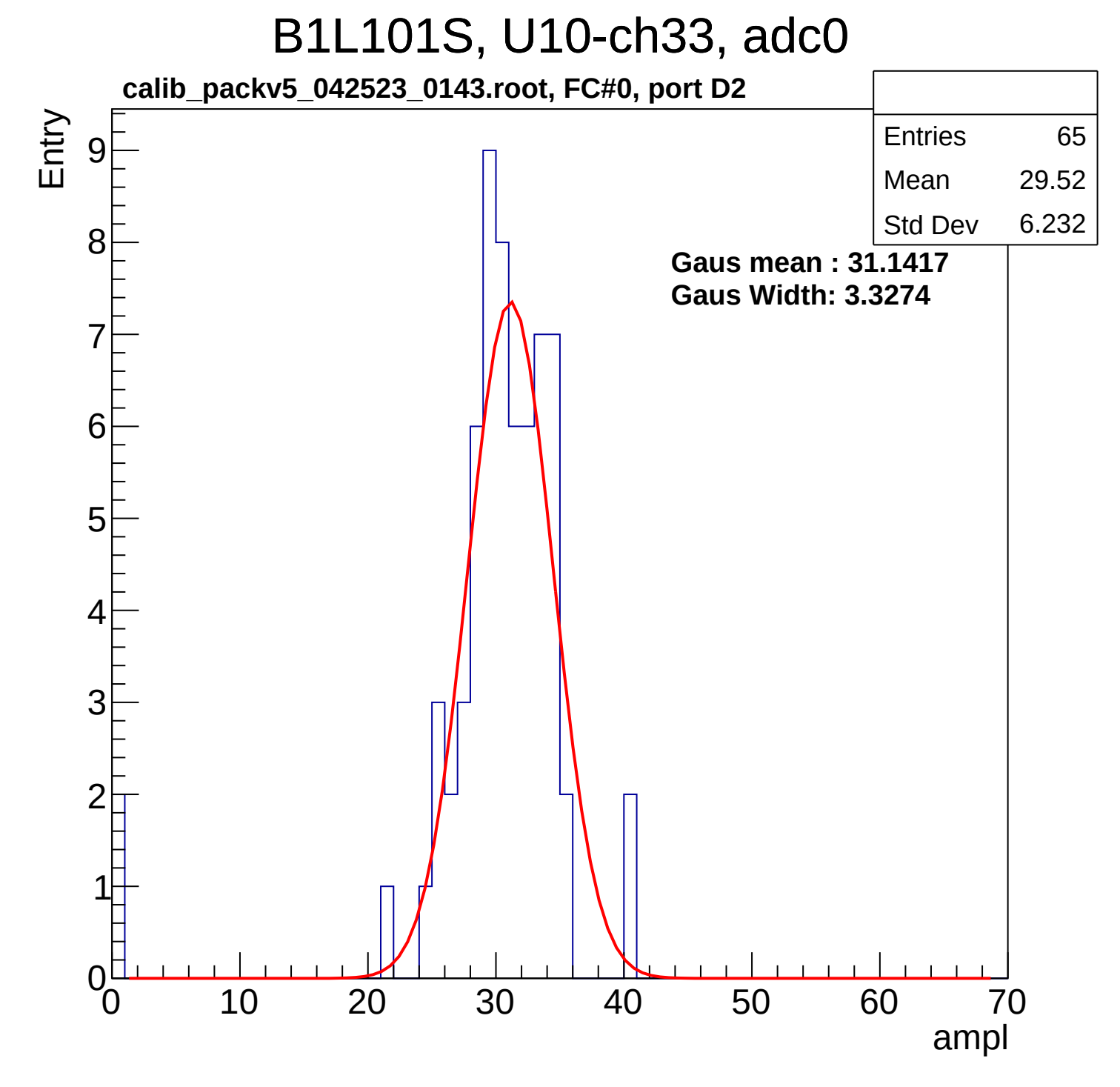
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch33, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 29.52
Std Dev 6.232
Gaus mean : 31.1417
Gaus Width: 3.3274
Entry
ampl
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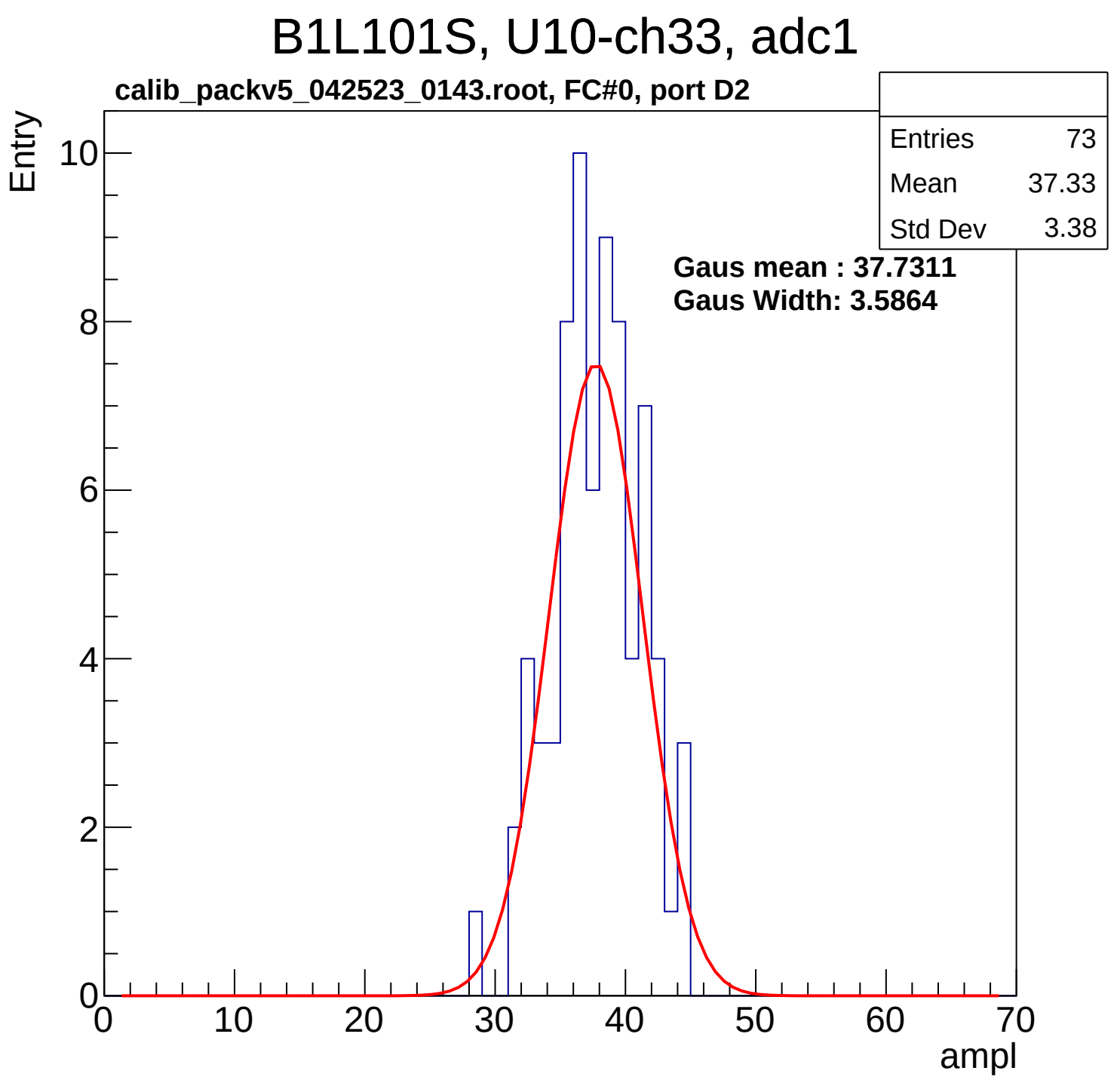
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch33, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 37.33
Std Dev 3.38
Gaus mean : 37.7311
Gaus Width: 3.5864
Entry
ampl
0
2
4
6
8
10
0
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20
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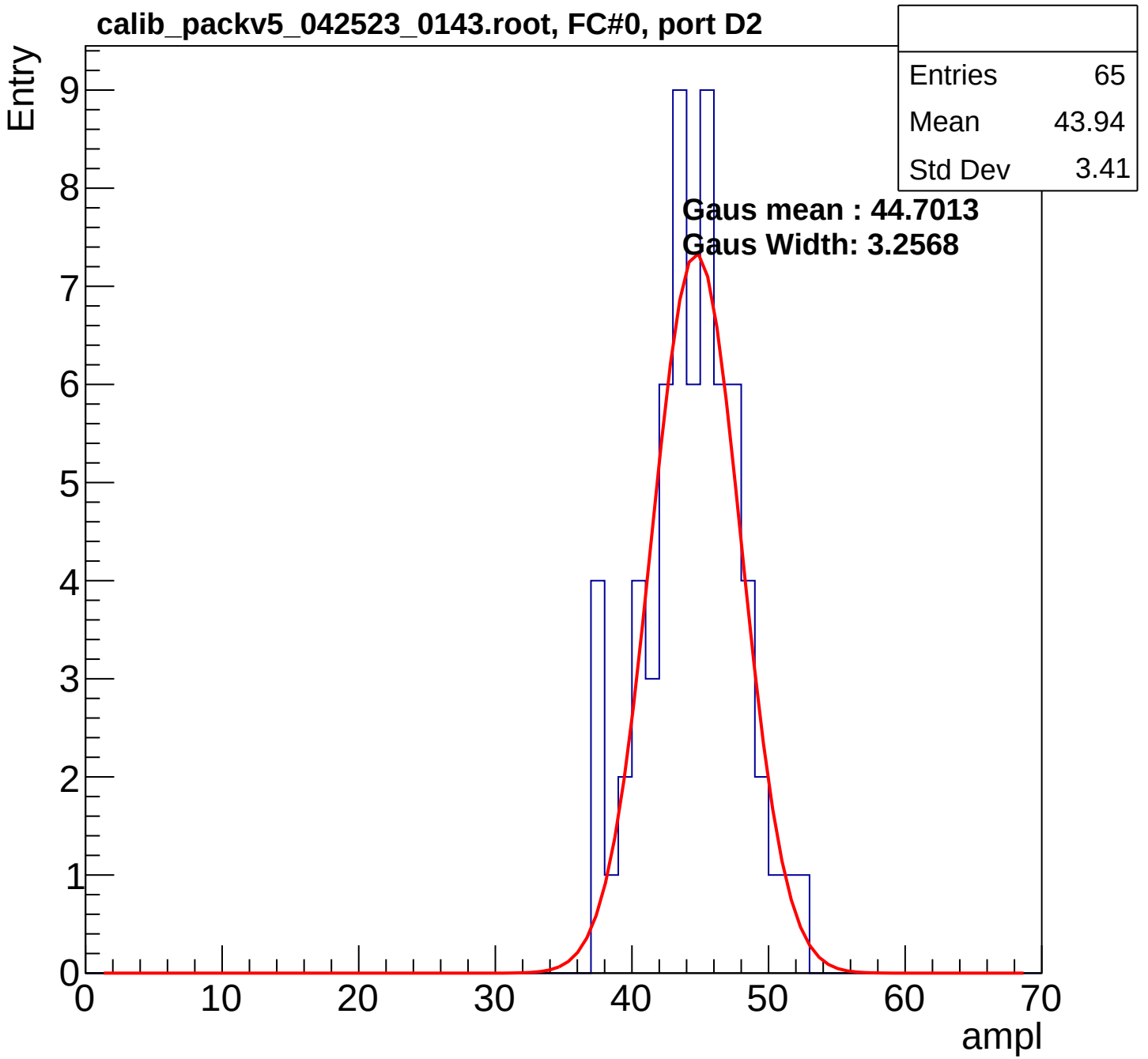
40
50
60
70


B1L101S, U10-ch33, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 43.94
Std Dev 3.41
Gaus mean : 44.7013
Gaus Width: 3.2568
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
50
60
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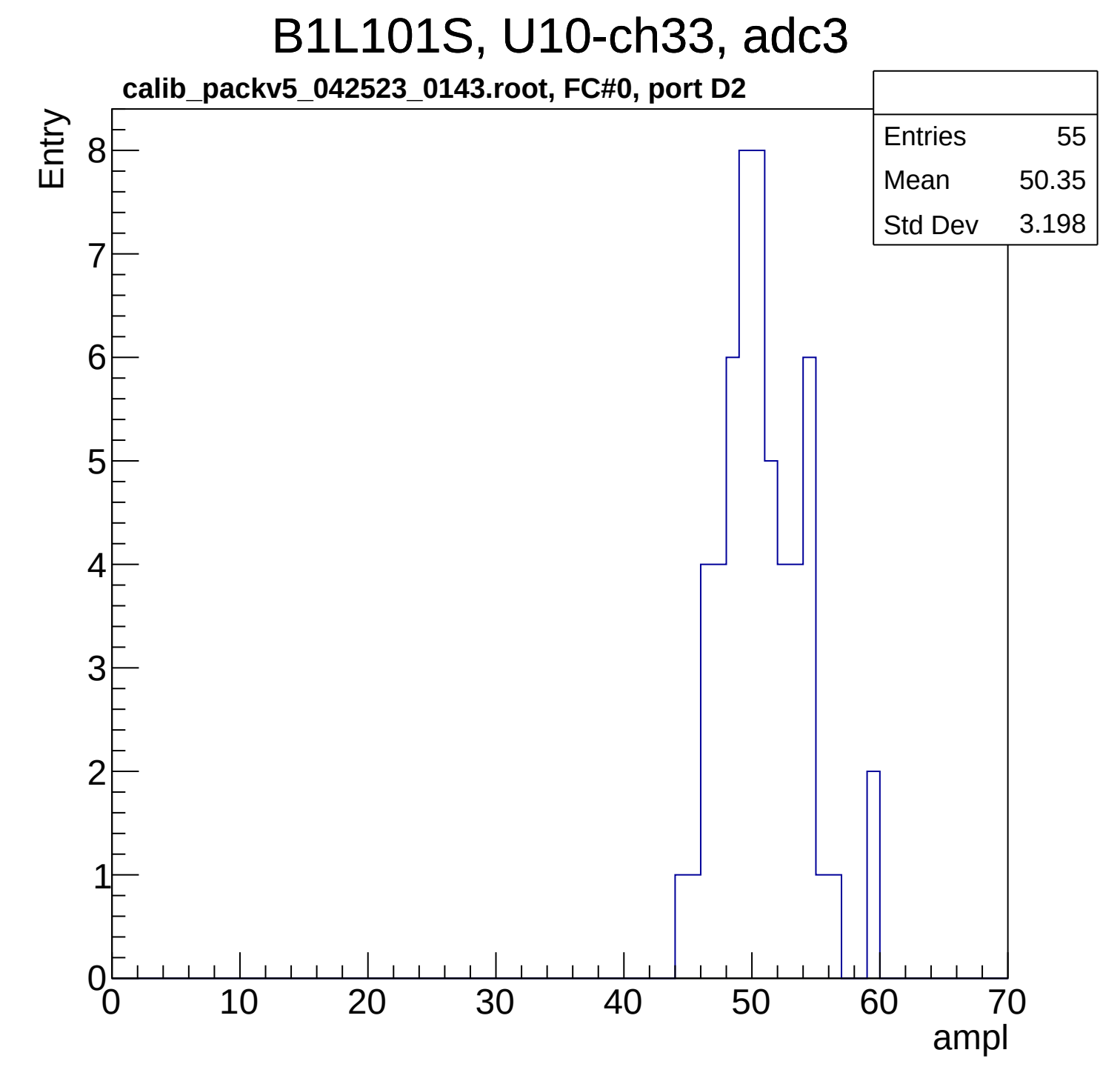
B1L101S, U10-ch33, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 50.35
Std Dev 3.198
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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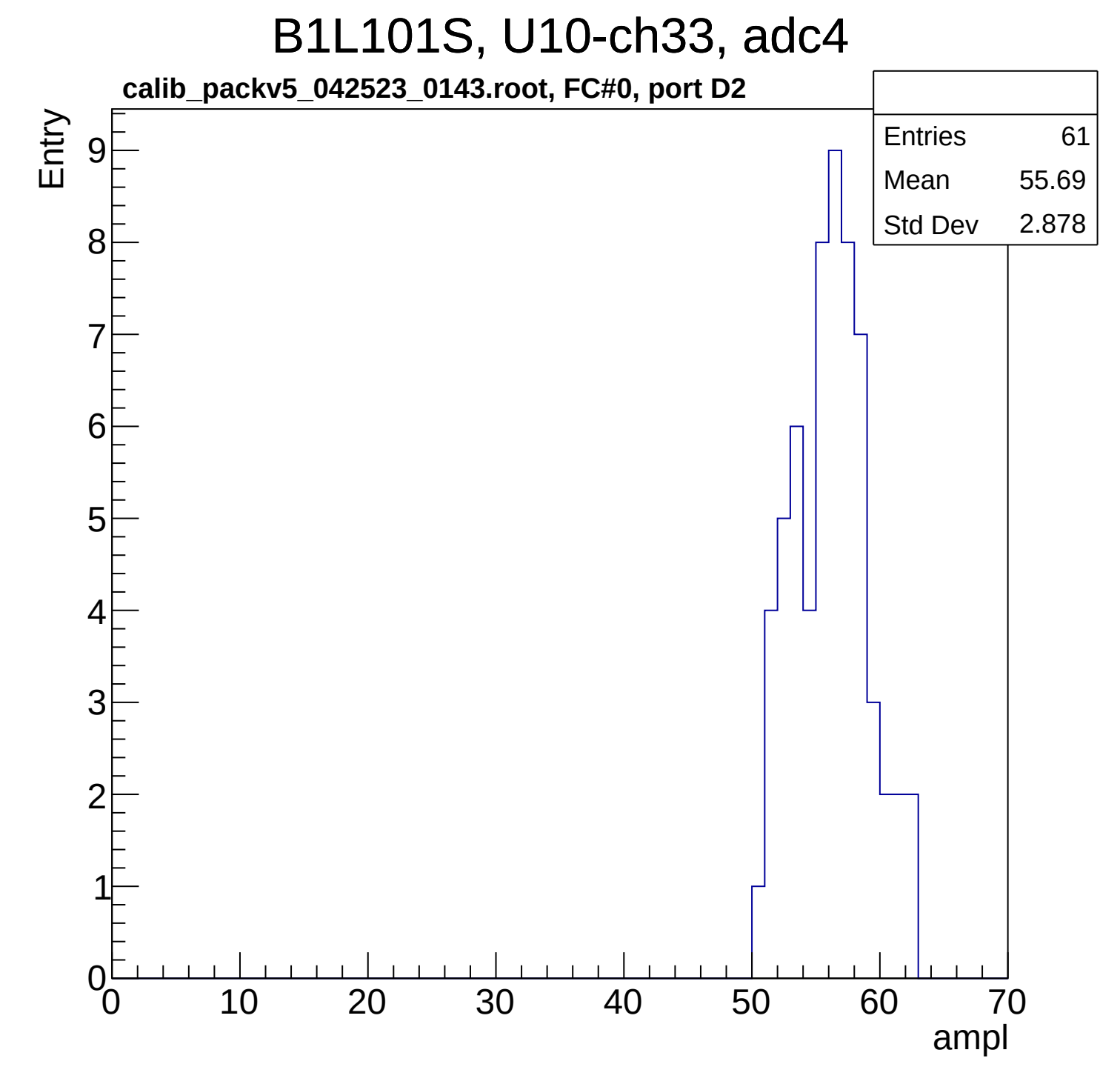
40
50
60
70


B1L101S, U10-ch33, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 55.69
Std Dev 2.878
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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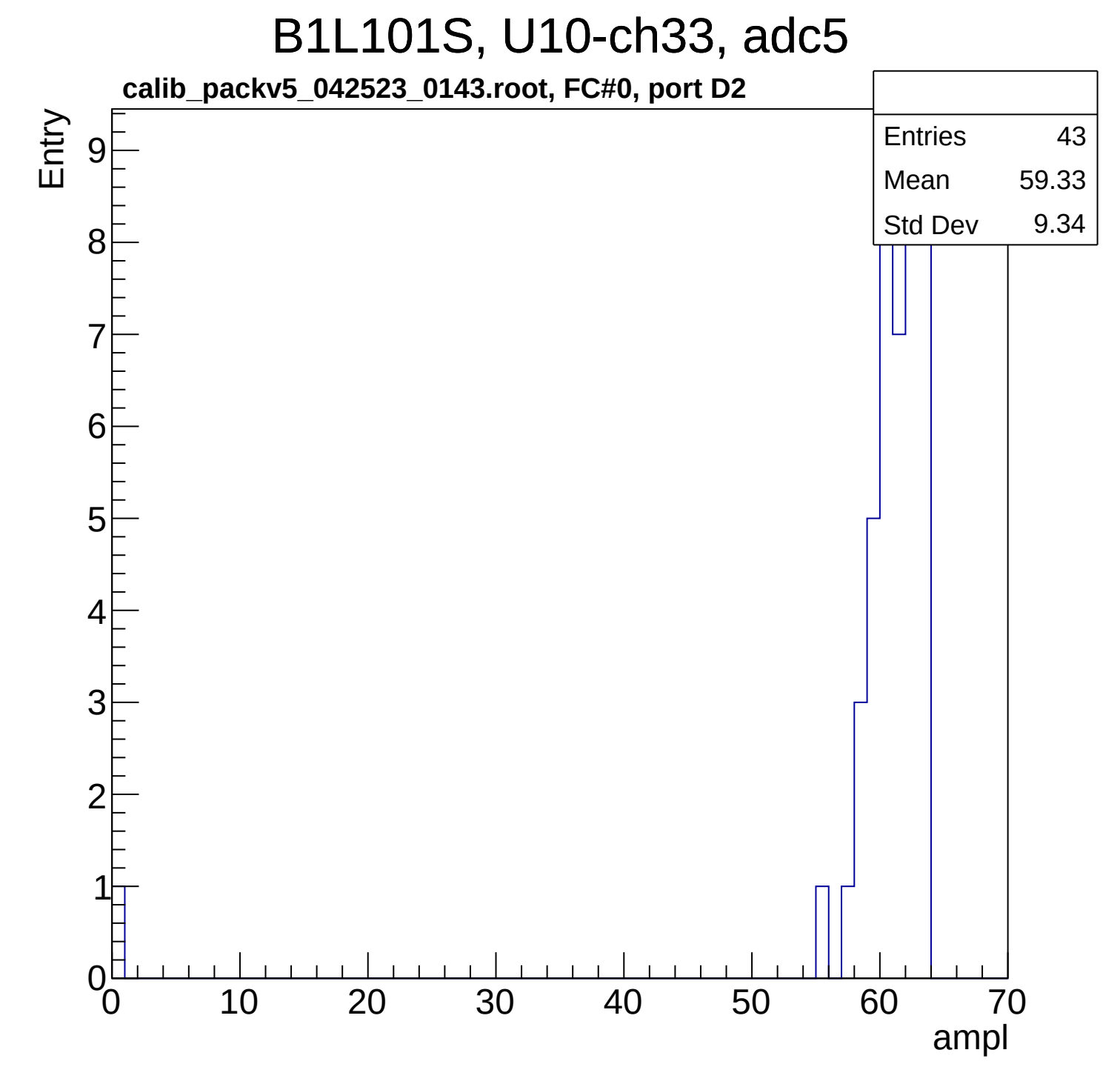
B1L101S, U10-ch33, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 43
Mean 59.33
Std Dev 9.34
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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60
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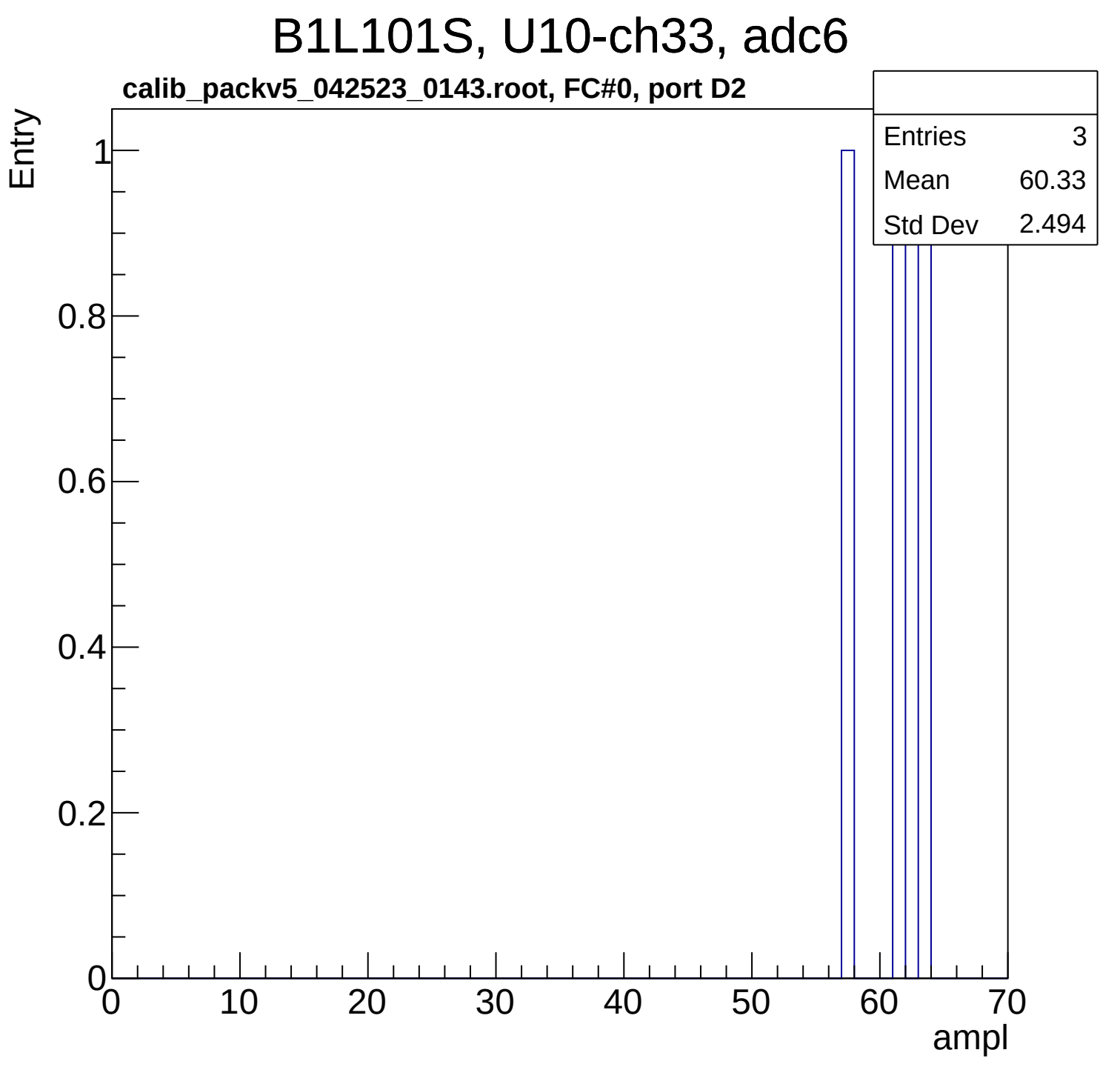
B1L101S, U10-ch33, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 60.33
Std Dev 2.494
Entry
ampl
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0.4
0.6
0.8
1
0
10
20
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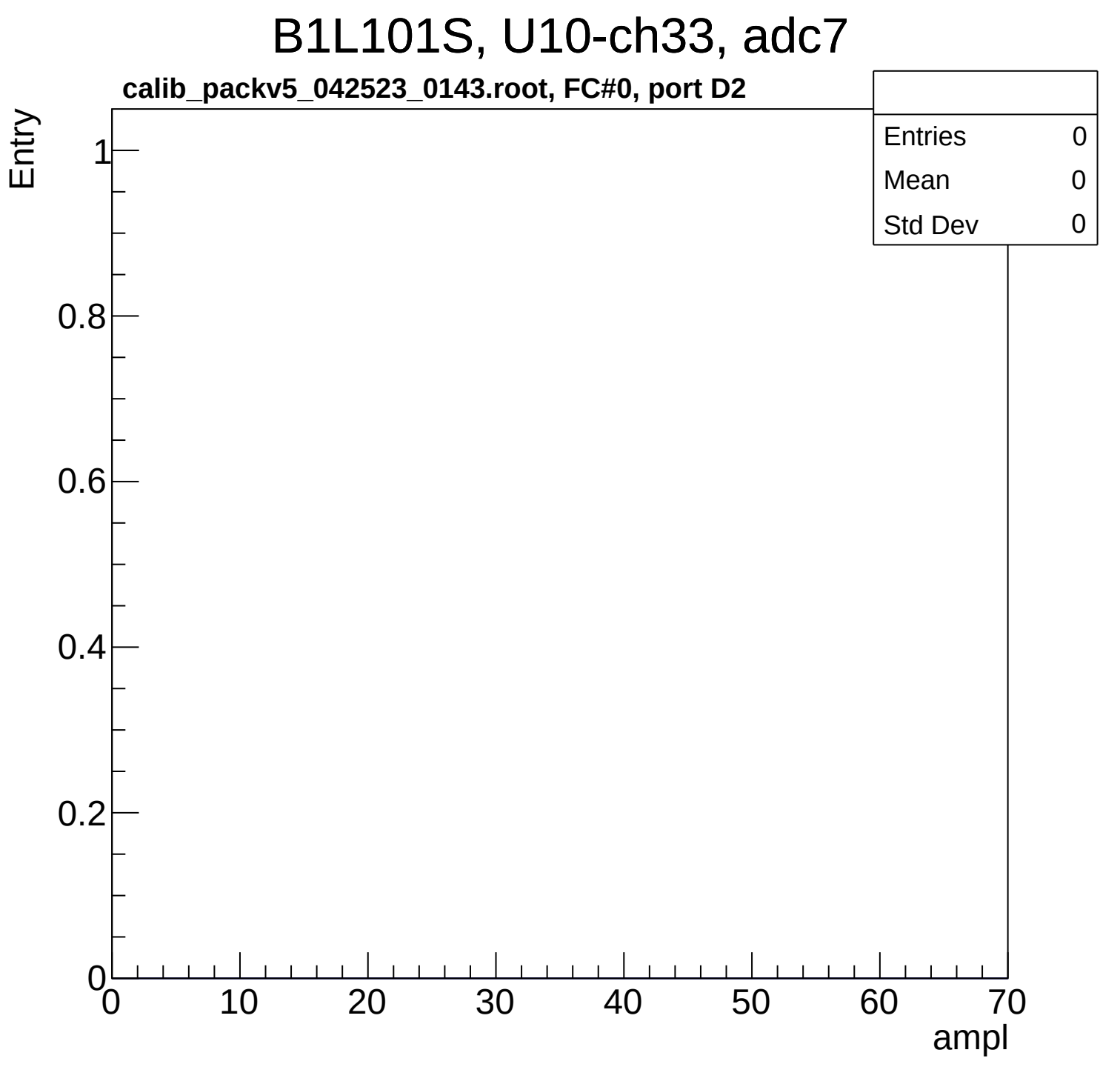
40
50
60
70


B1L101S, U10-ch33, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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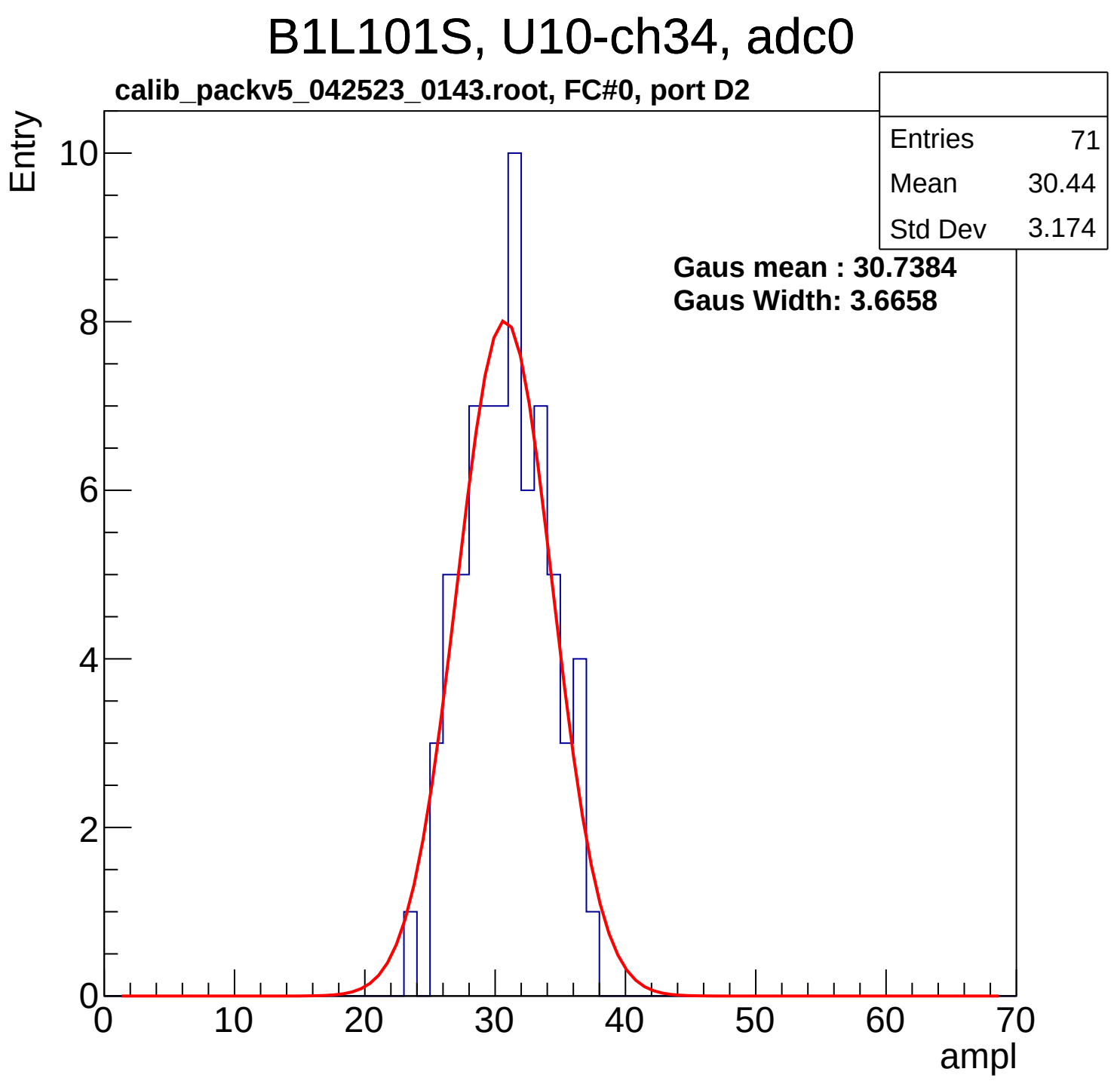
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch34, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 30.44
Std Dev 3.174
Gaus mean : 30.7384
Gaus Width: 3.6658
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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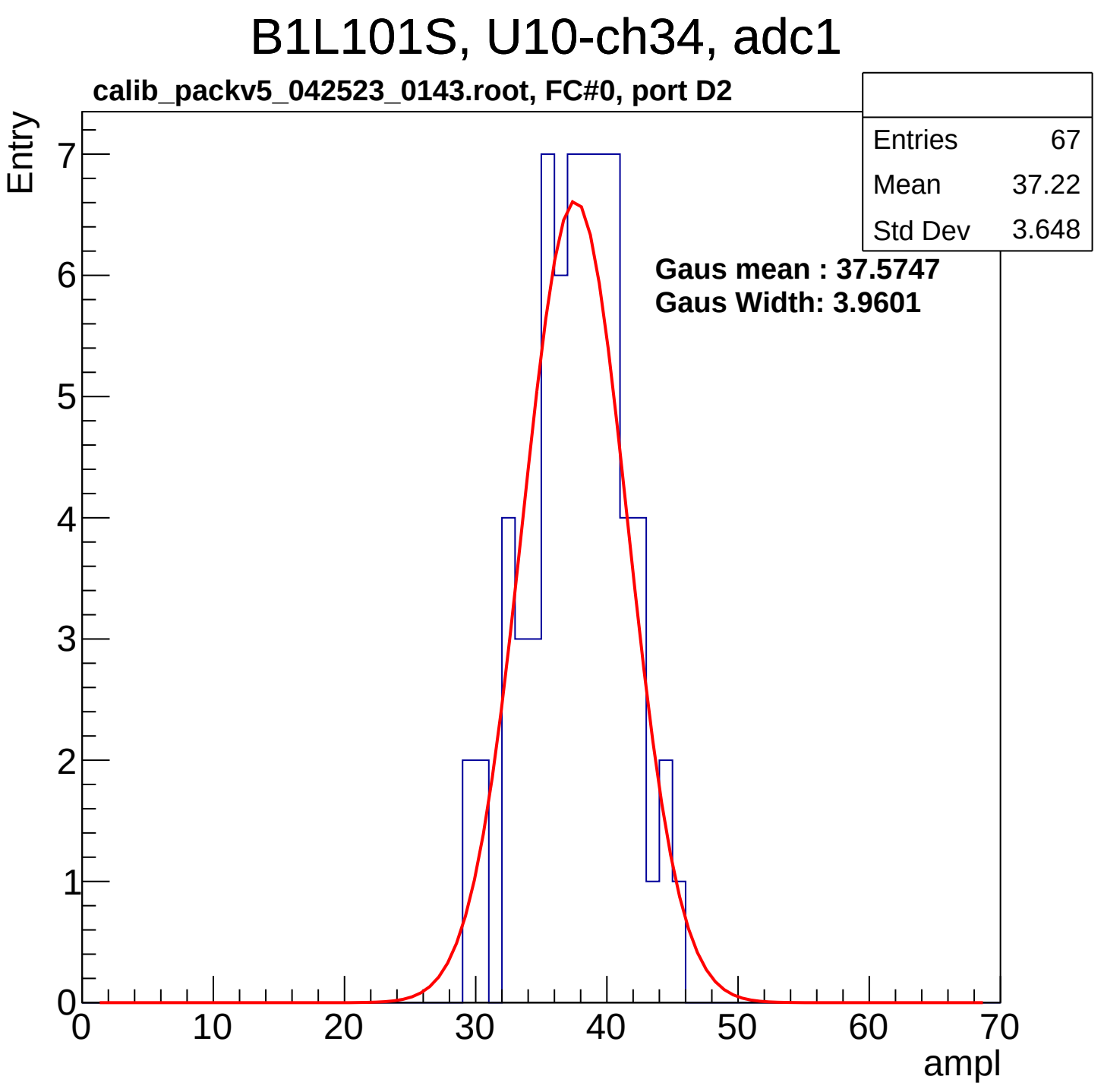
B1L101S, U10-ch34, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 37.22
Std Dev 3.648
Gaus mean : 37.5747
Gaus Width: 3.9601
Entry
ampl
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2
3
4
5
6
7
0
10
20
30
40
50
60
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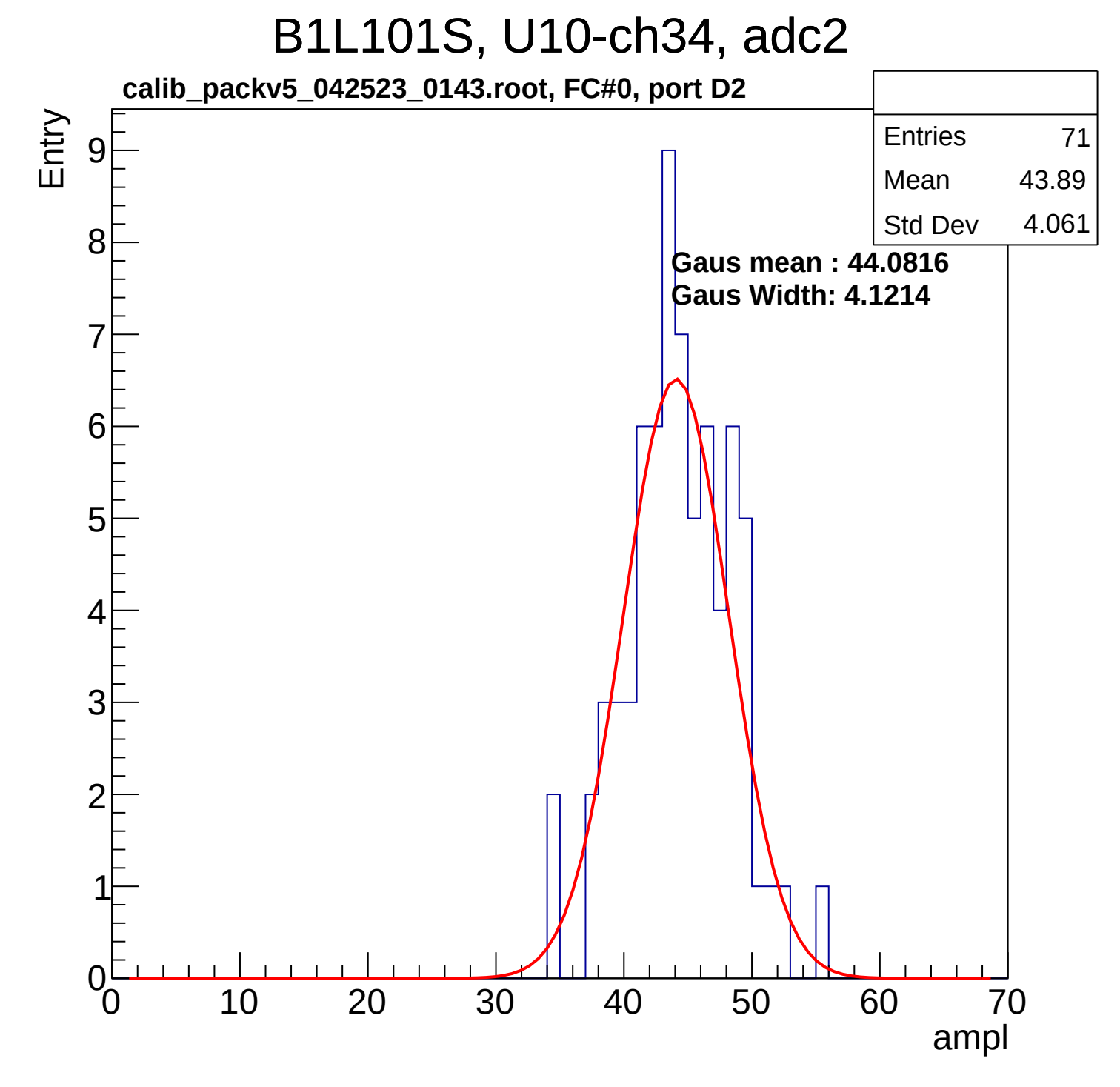
B1L101S, U10-ch34, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 43.89
Std Dev 4.061
Gaus mean : 44.0816
Gaus Width: 4.1214
Entry
ampl
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3
4
5
6
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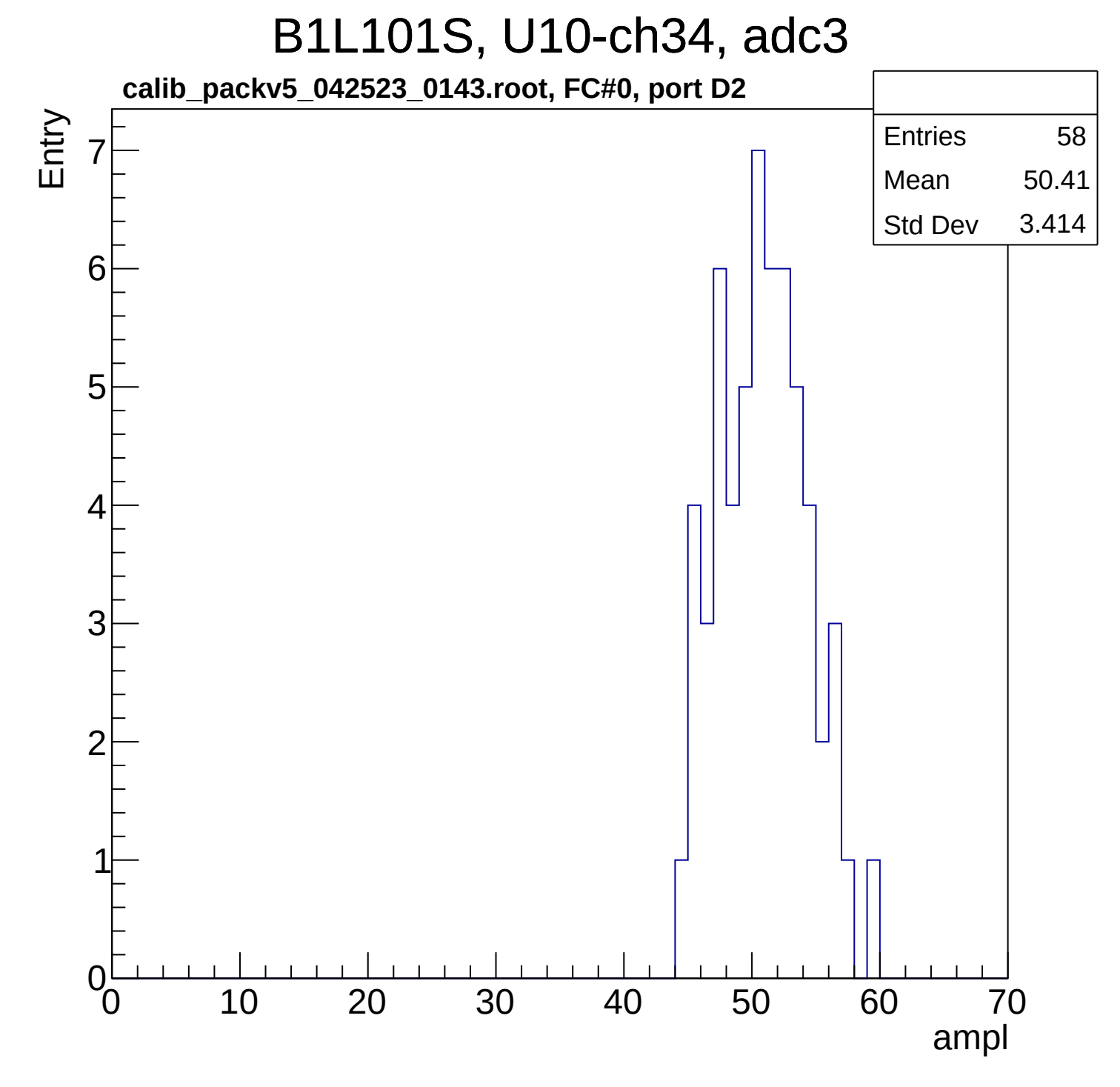
B1L101S, U10-ch34, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 50.41
Std Dev 3.414
Entry
ampl
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3
4
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6
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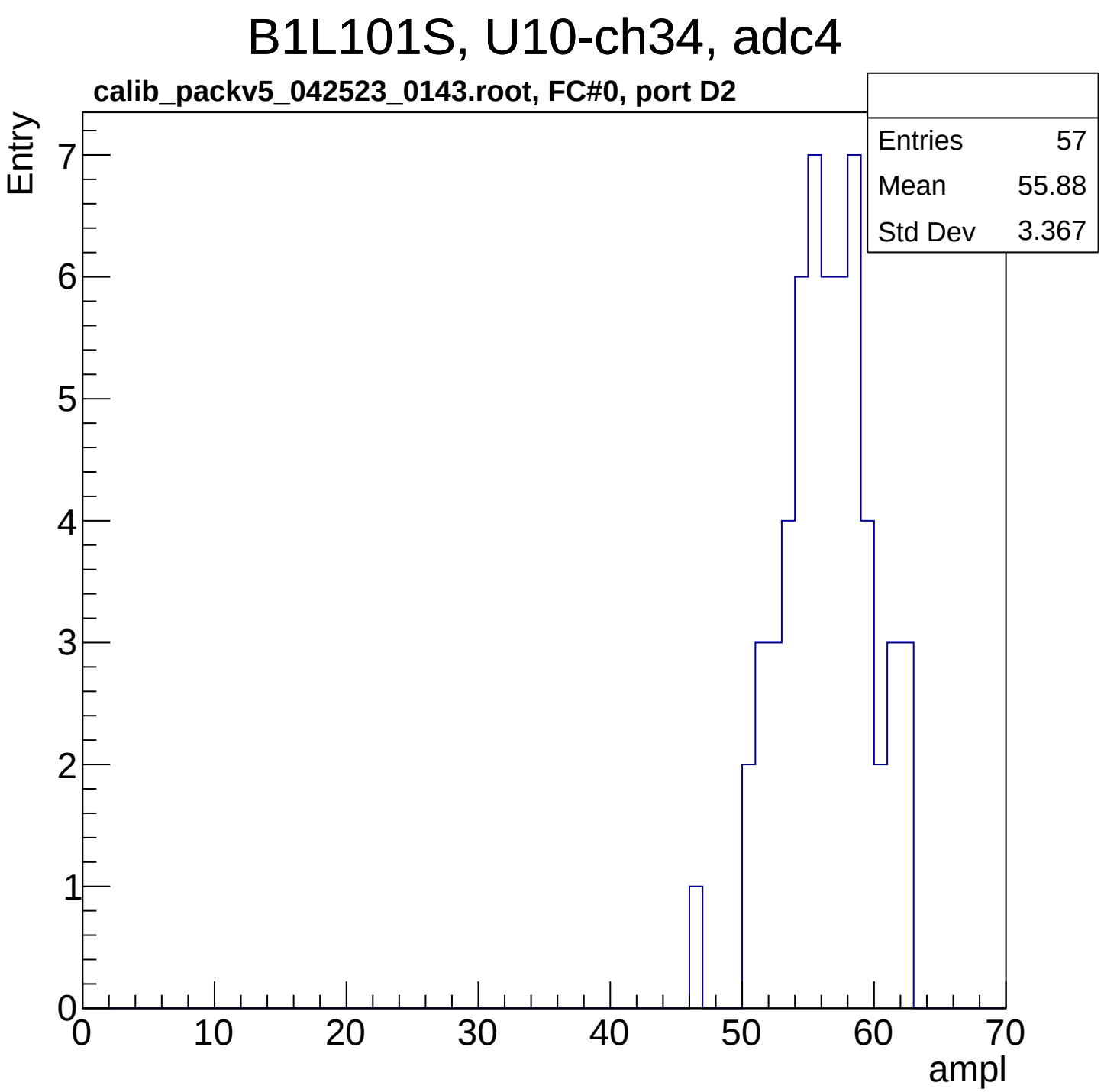
B1L101S, U10-ch34, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 55.88
Std Dev 3.367
Entry
ampl
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40
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60
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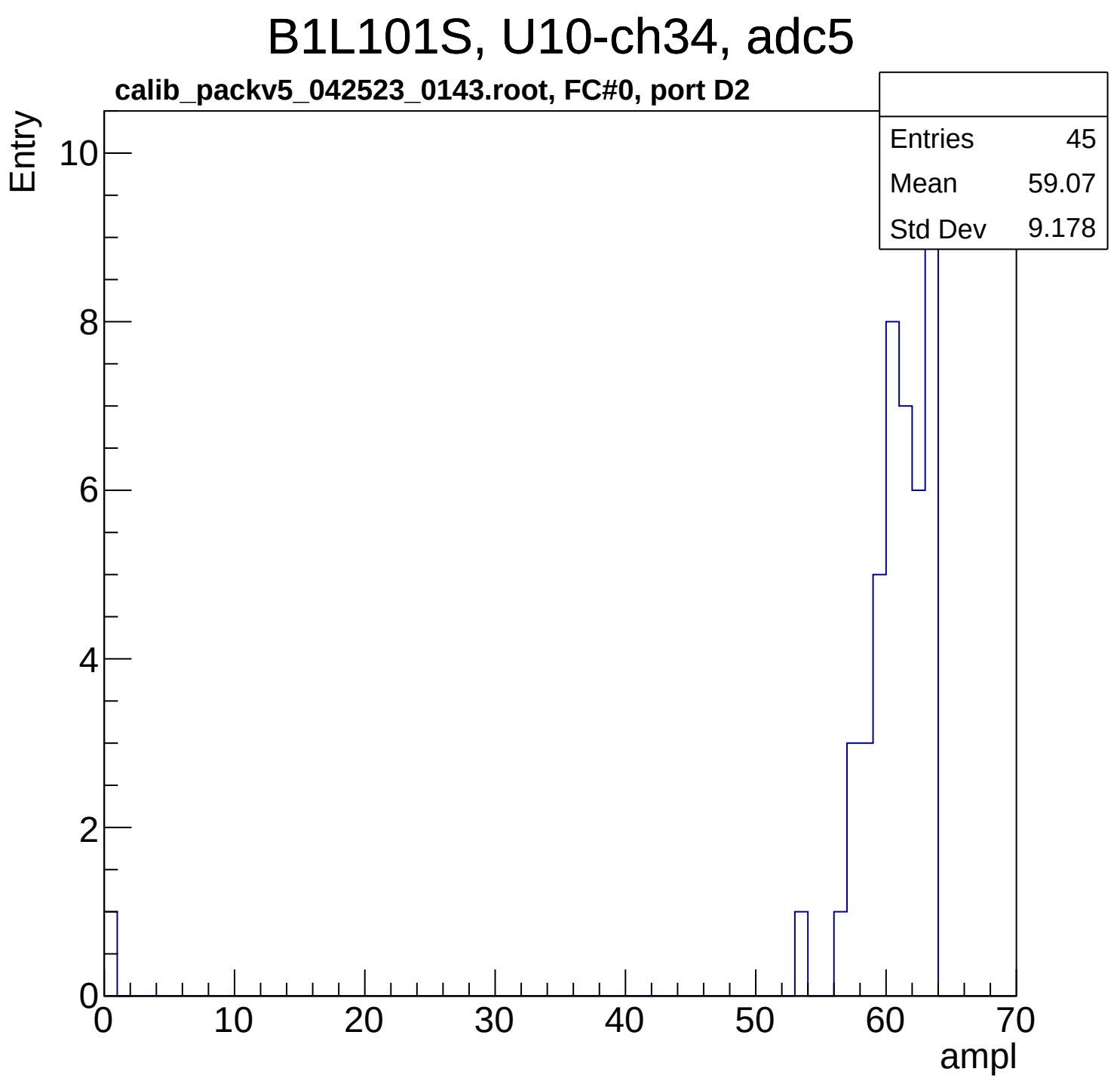
B1L101S, U10-ch34, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 59.07
Std Dev 9.178
Entry
0
2
4
6
8
10
0
10
20
30
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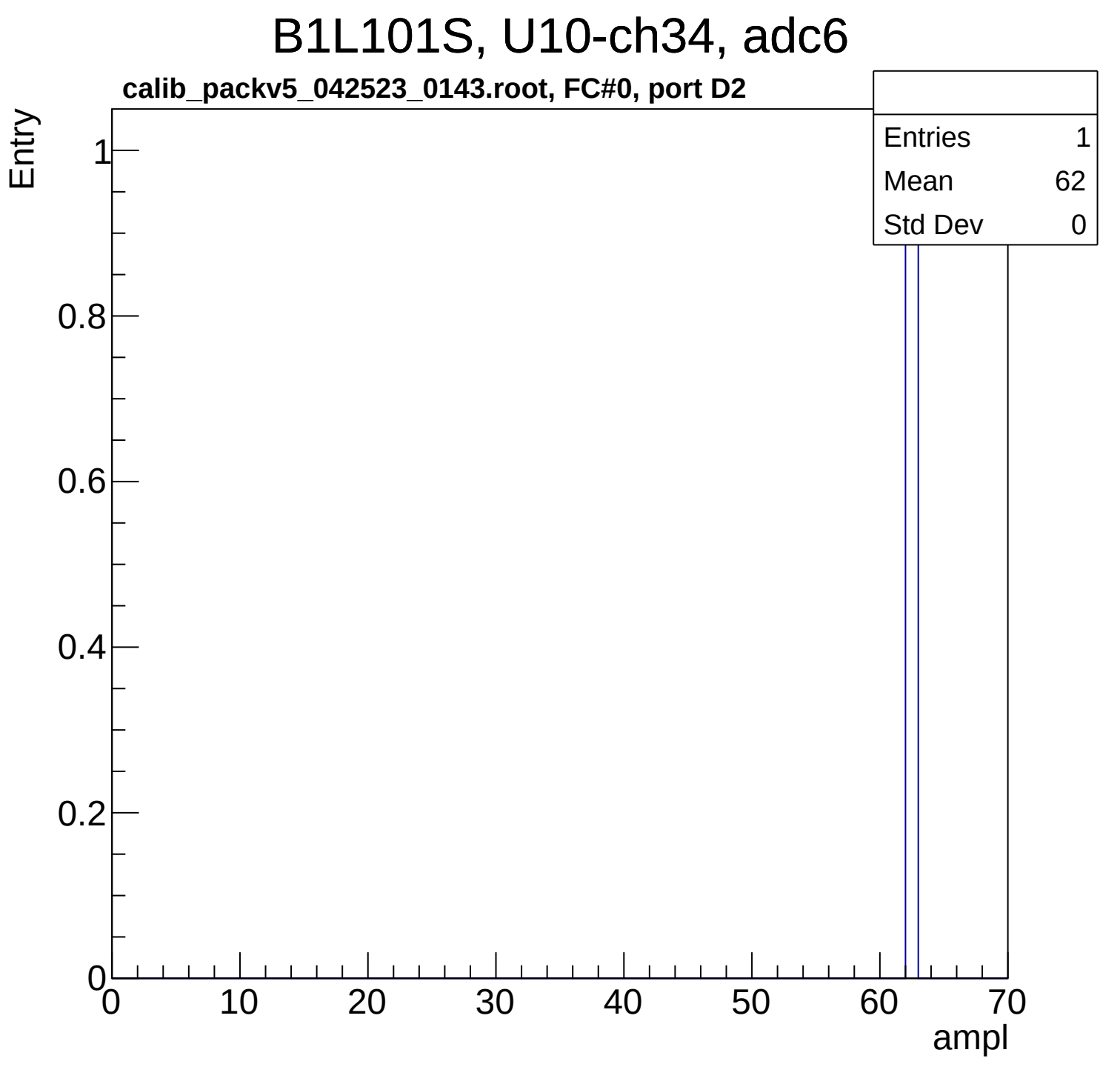
50
60
70
ampl


B1L101S, U10-ch34, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 62
Std Dev 0
Entry
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0.6
0.4
0.2
0
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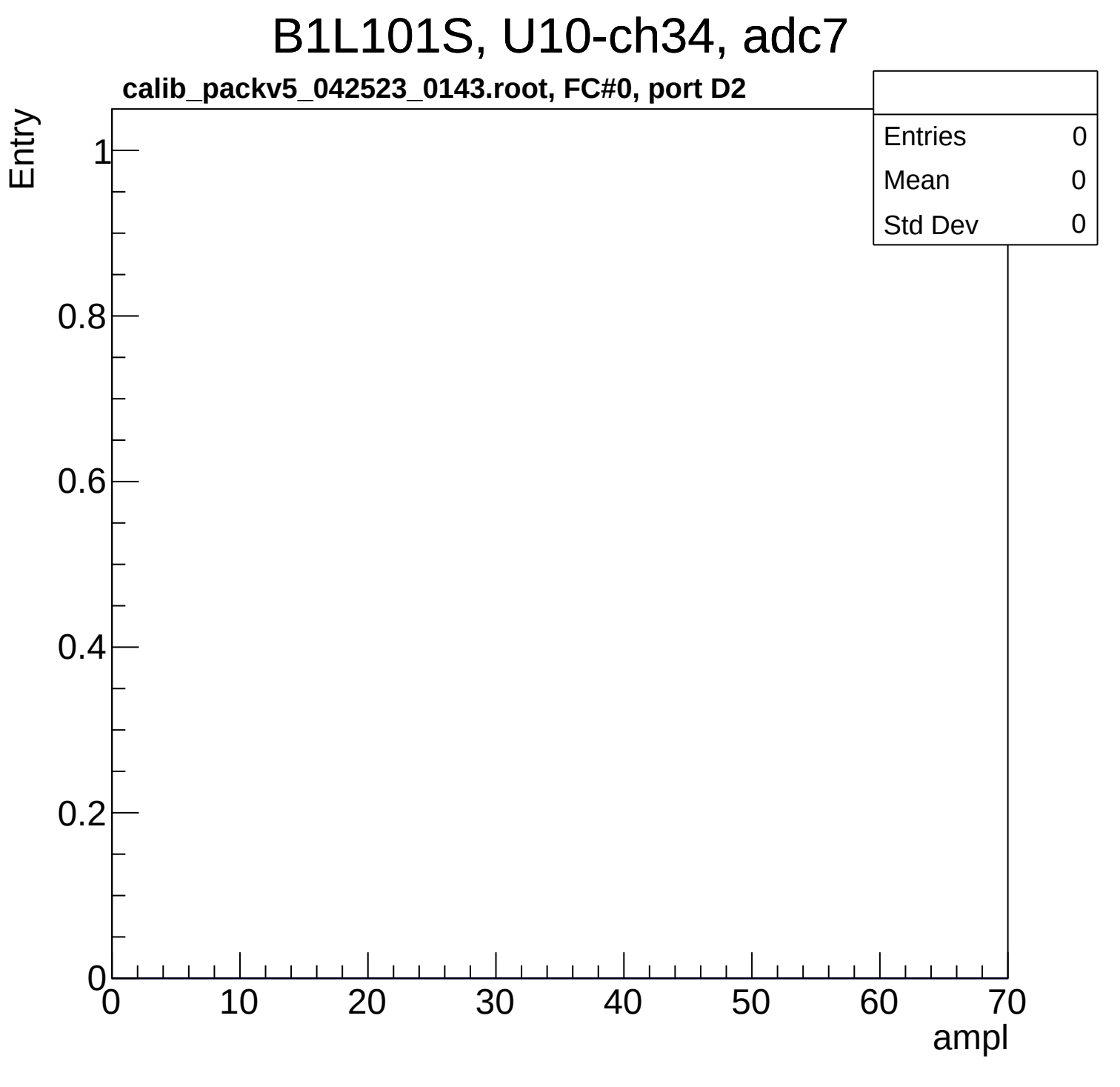
70
ampl


B1L101S, U10-ch34, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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0.6
0.4
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10
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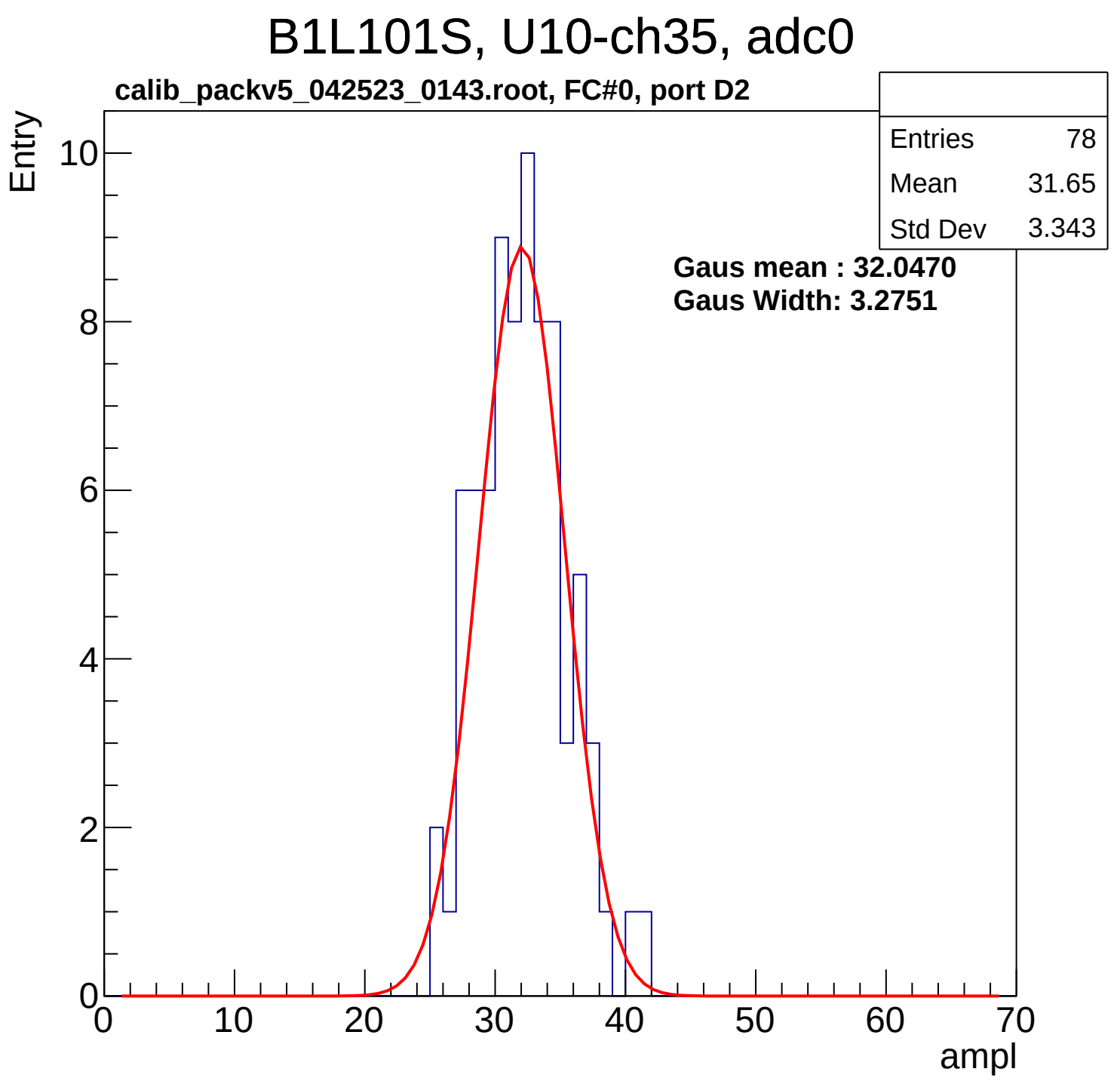
60
70
ampl


B1L101S, U10-ch35, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 31.65
Std Dev 3.343
Gaus mean : 32.0470
Gaus Width: 3.2751
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
50
60
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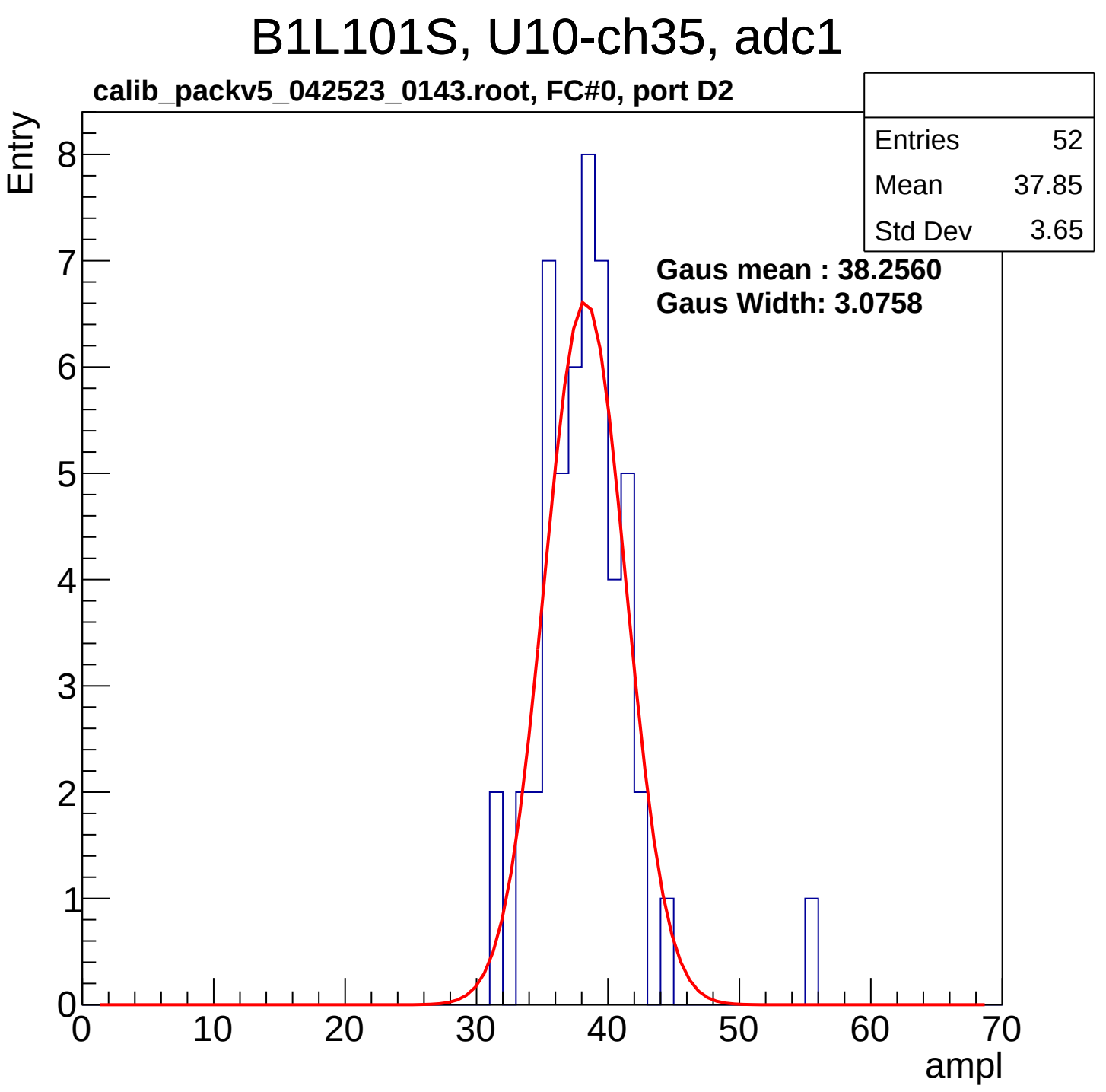
B1L101S, U10-ch35, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 37.85
Std Dev 3.65
Gaus mean : 38.2560
Gaus Width: 3.0758
Entry
ampl
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1
2
3
4
5
6
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0
10
20
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40
50
60
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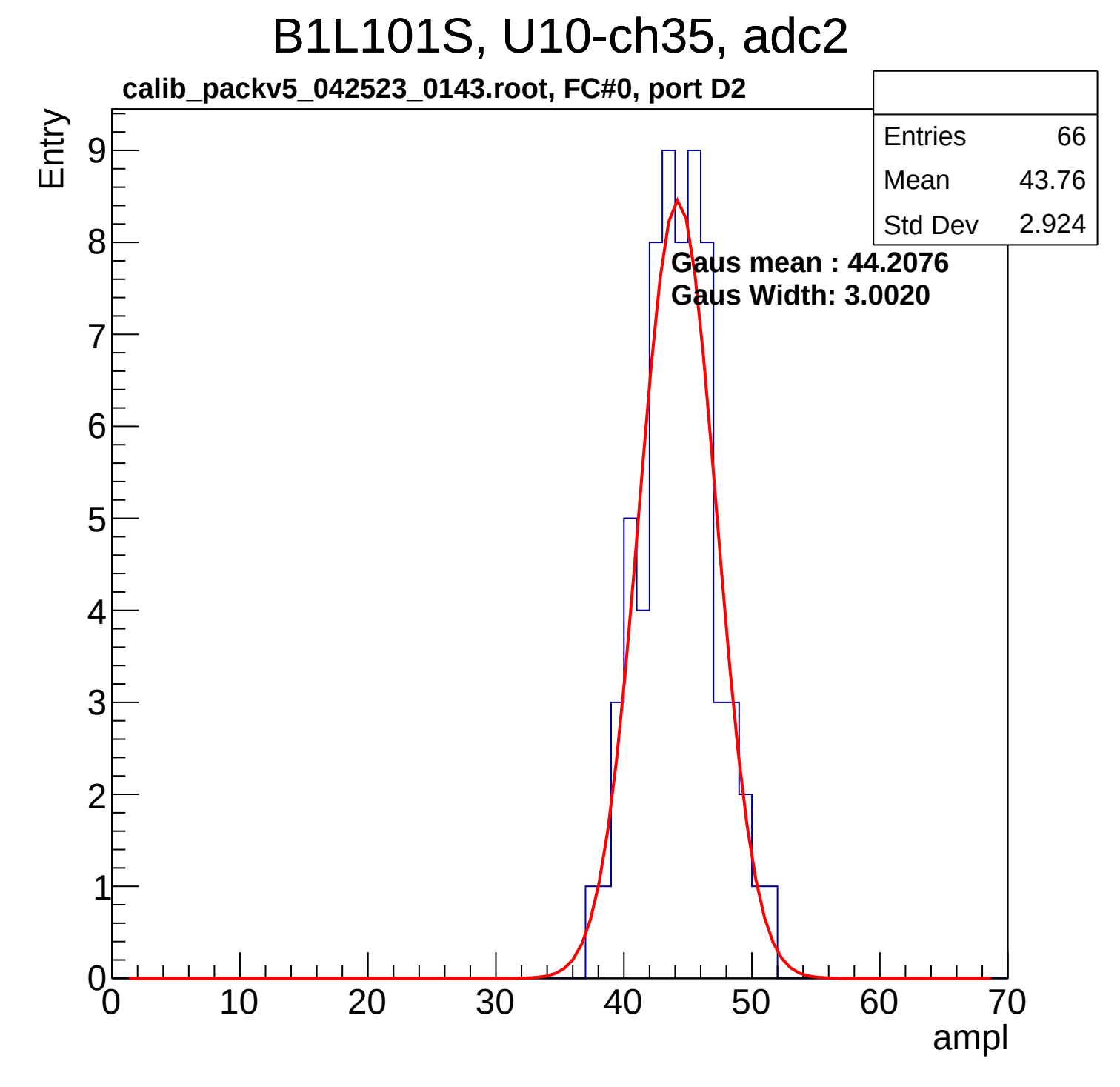
B1L101S, U10-ch35, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 43.76
Std Dev 2.924
Gaus mean : 44.2076
Gaus Width: 3.0020
Entry
ampl
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2
3
4
5
6
7
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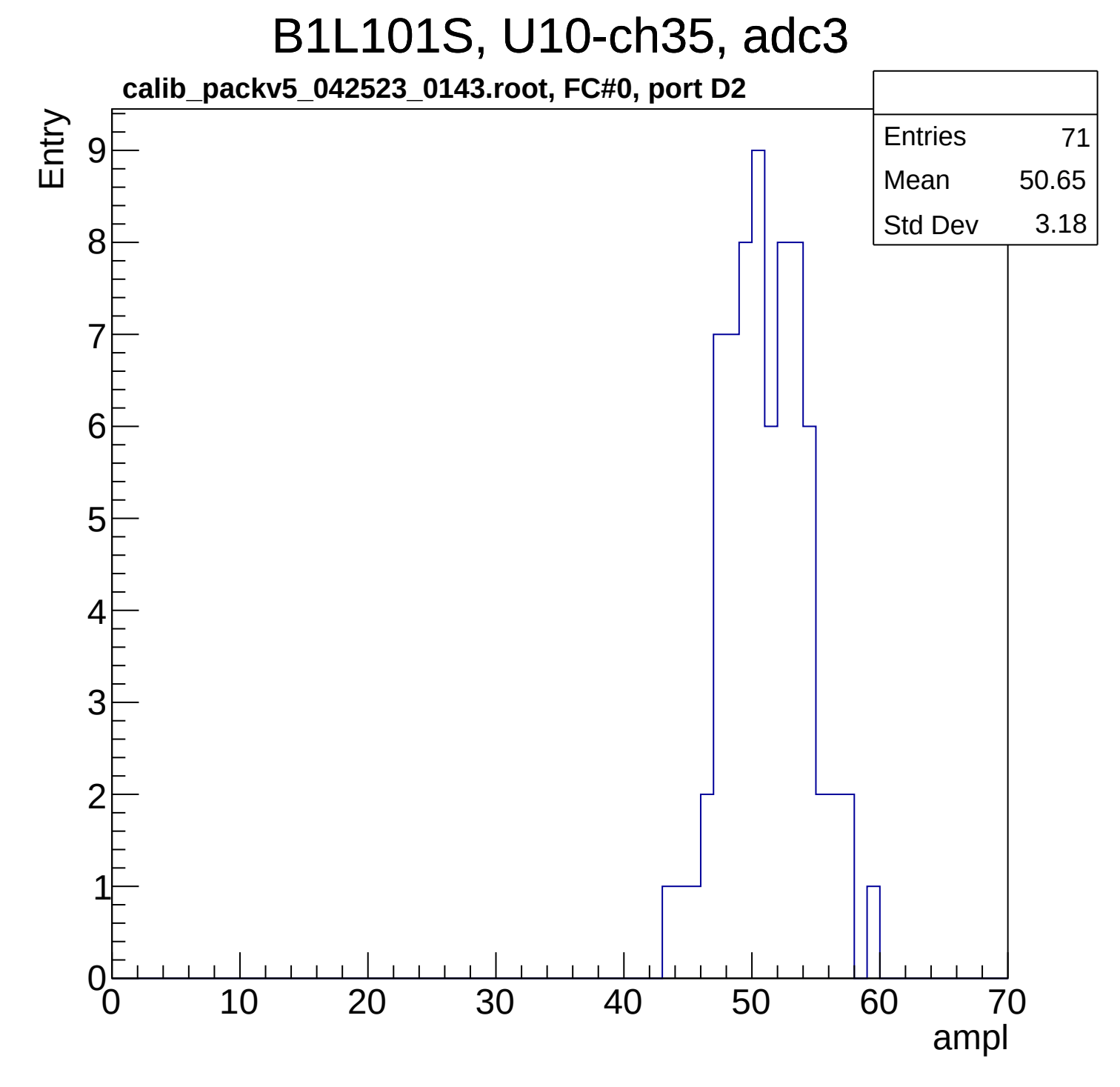
B1L101S, U10-ch35, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 50.65
Std Dev 3.18
Entry
ampl
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2
3
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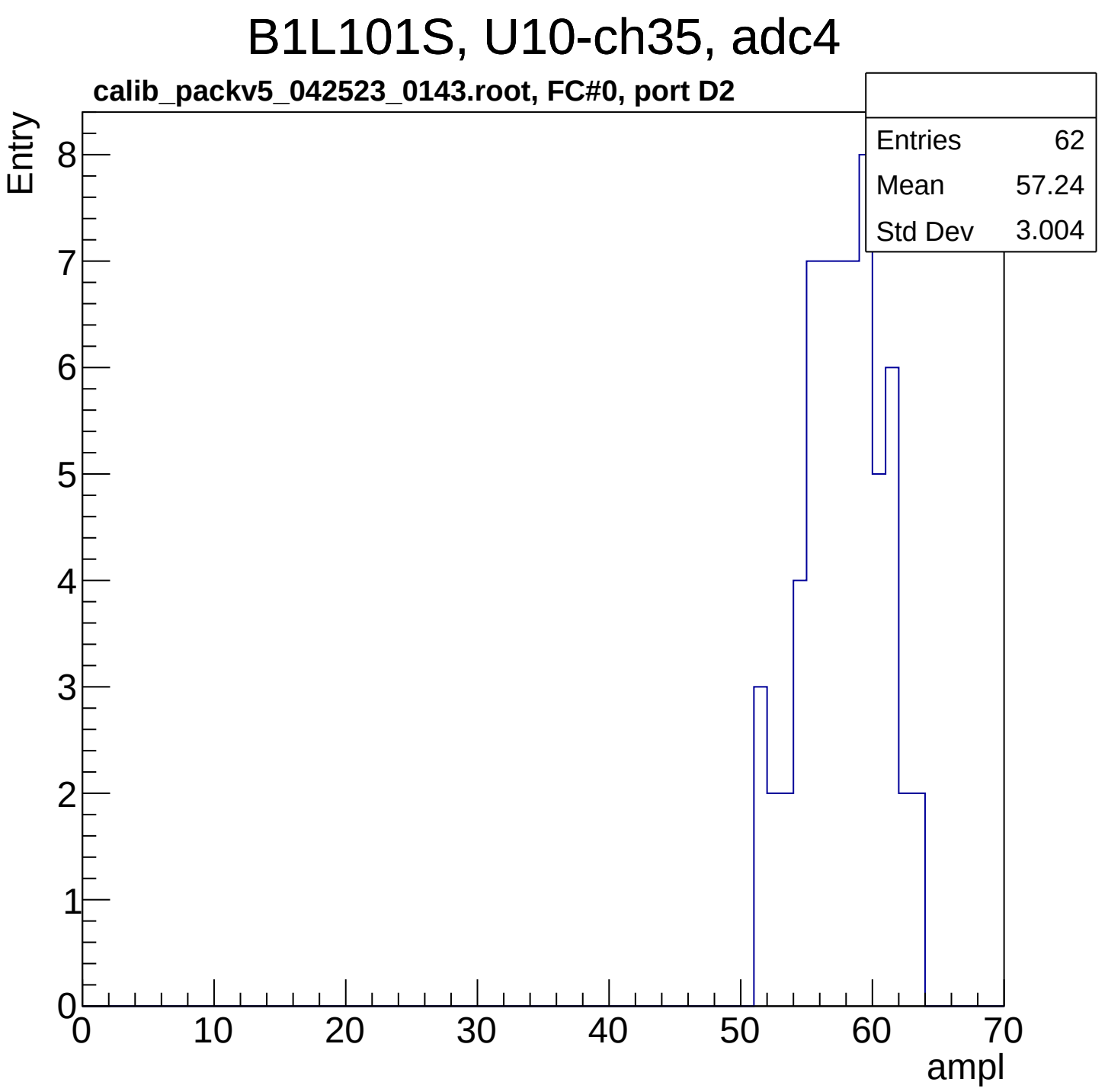
B1L101S, U10-ch35, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 57.24
Std Dev 3.004
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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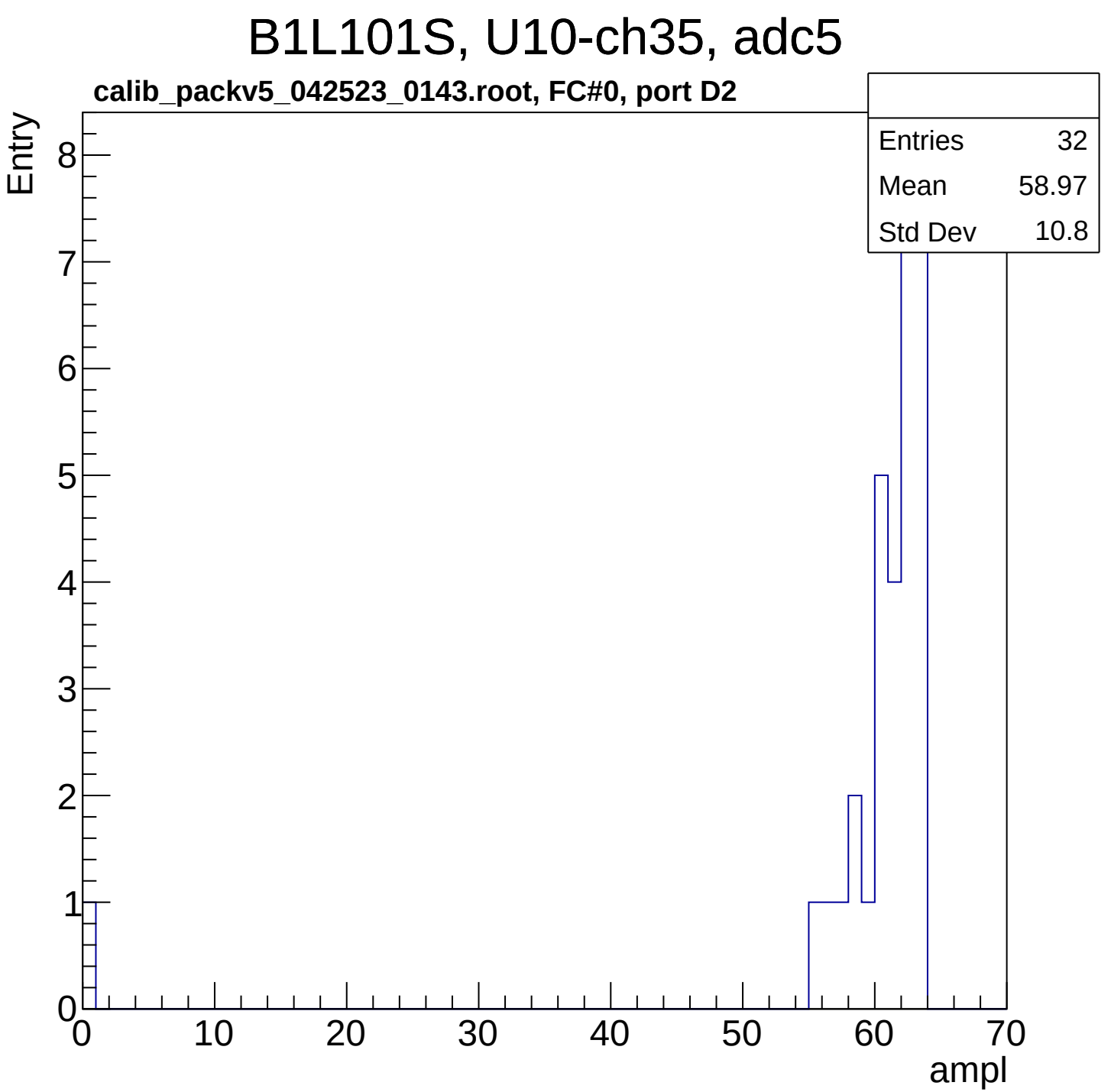
40
50
60
70


B1L101S, U10-ch35, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 32
Mean 58.97
Std Dev 10.8
Entry
ampl
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1
2
3
4
5
6
7
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0
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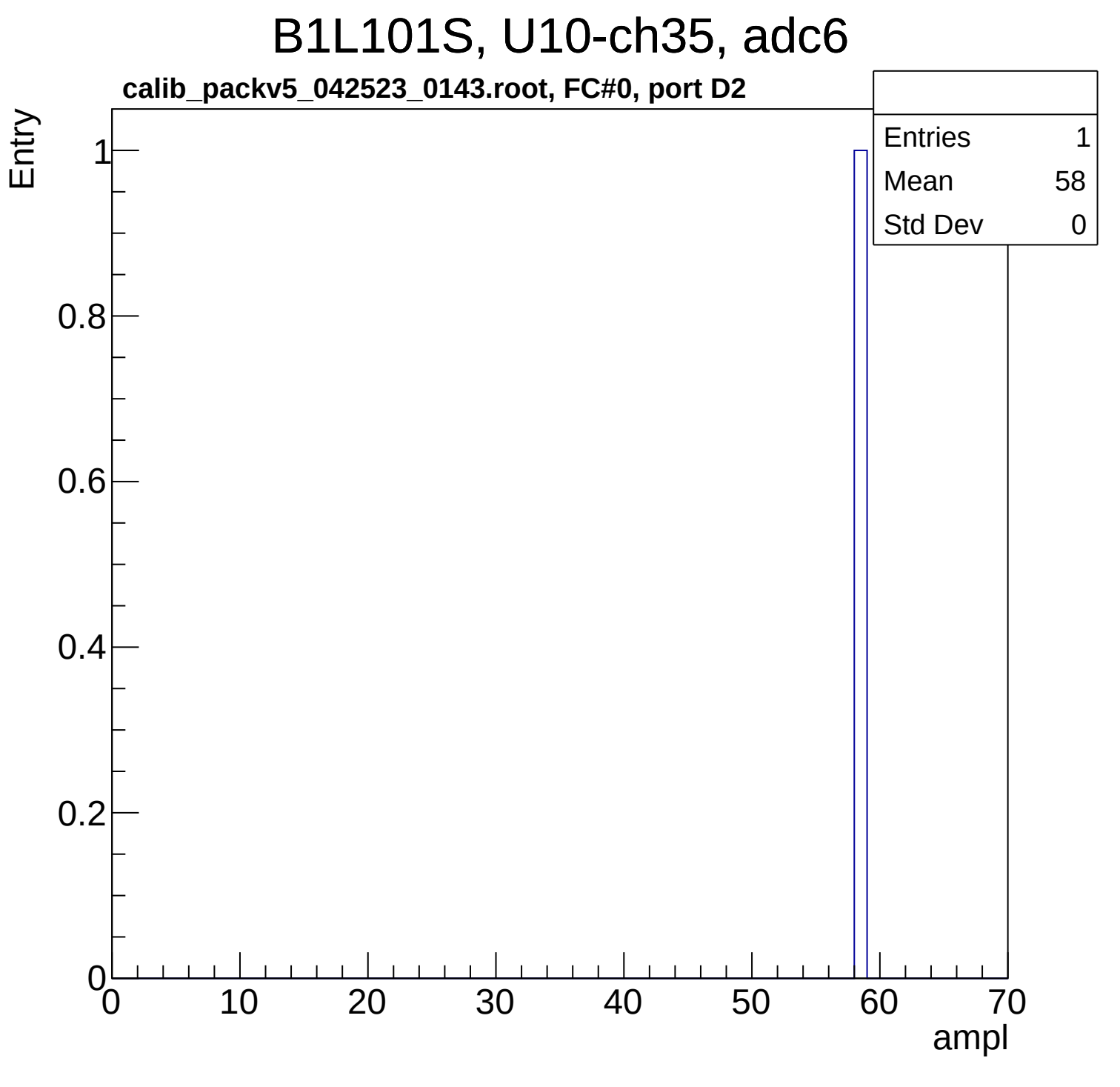
B1L101S, U10-ch35, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 58
Std Dev 0
Entry
ampl
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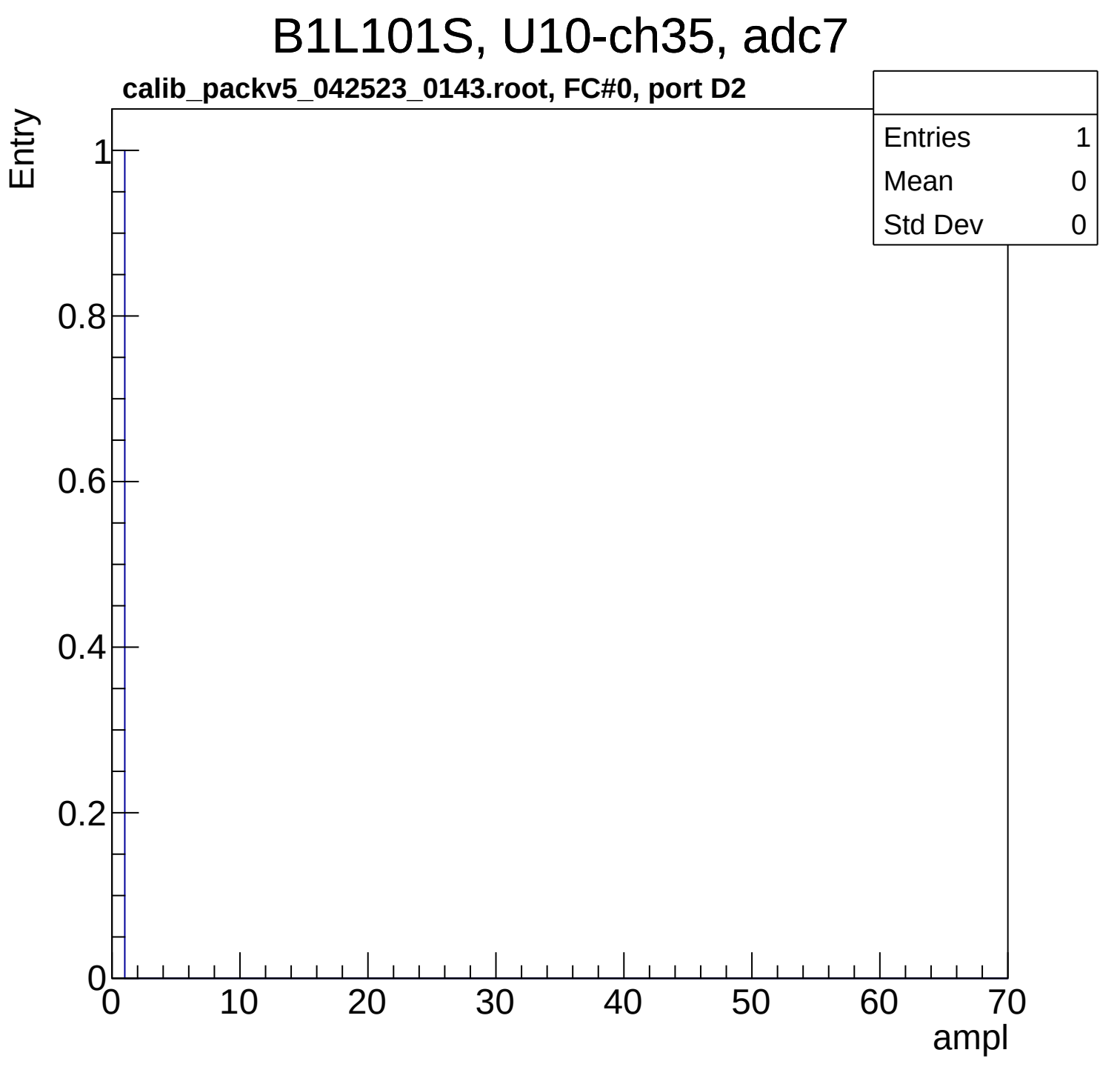
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L101S, U10-ch35, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
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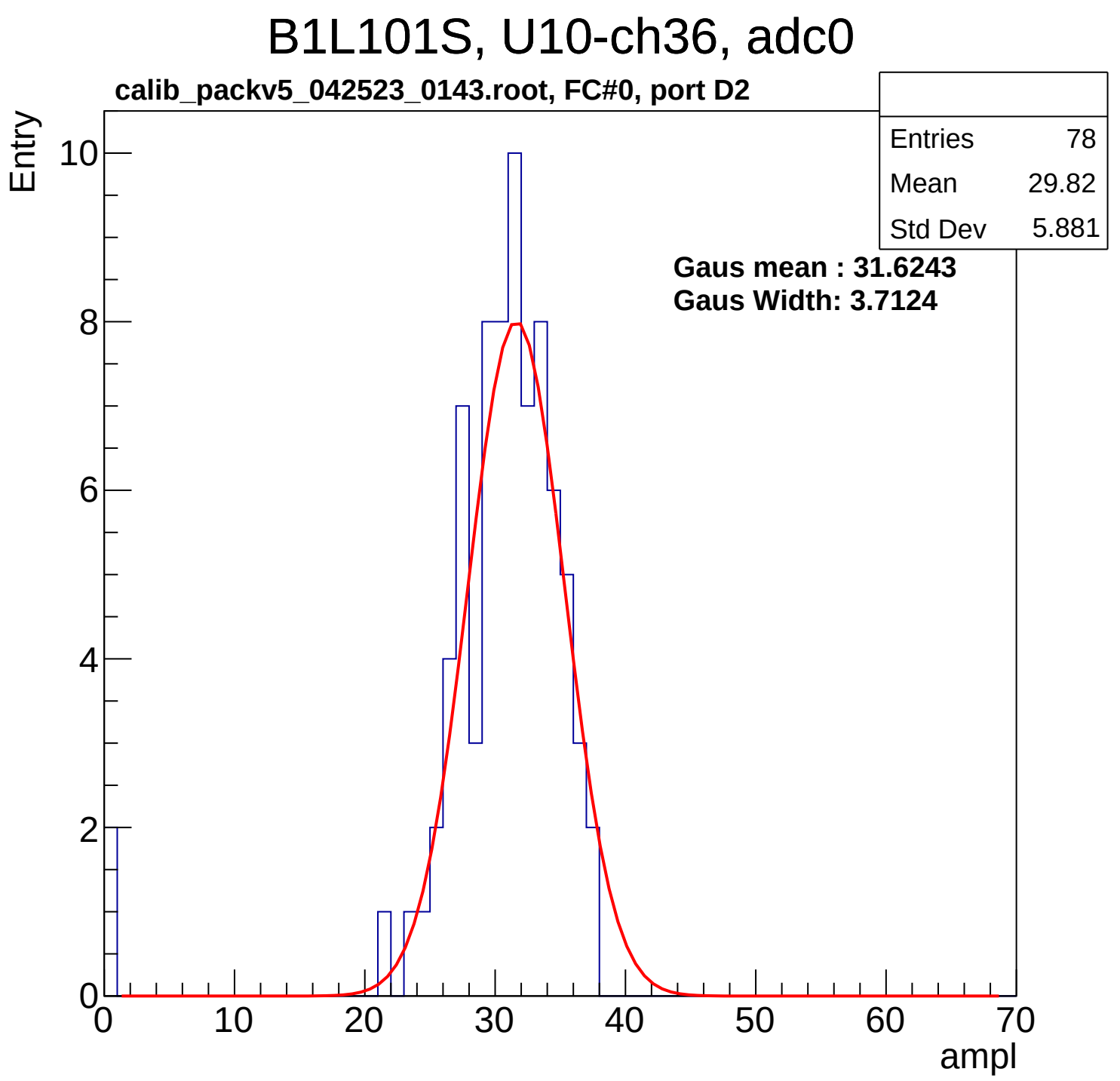
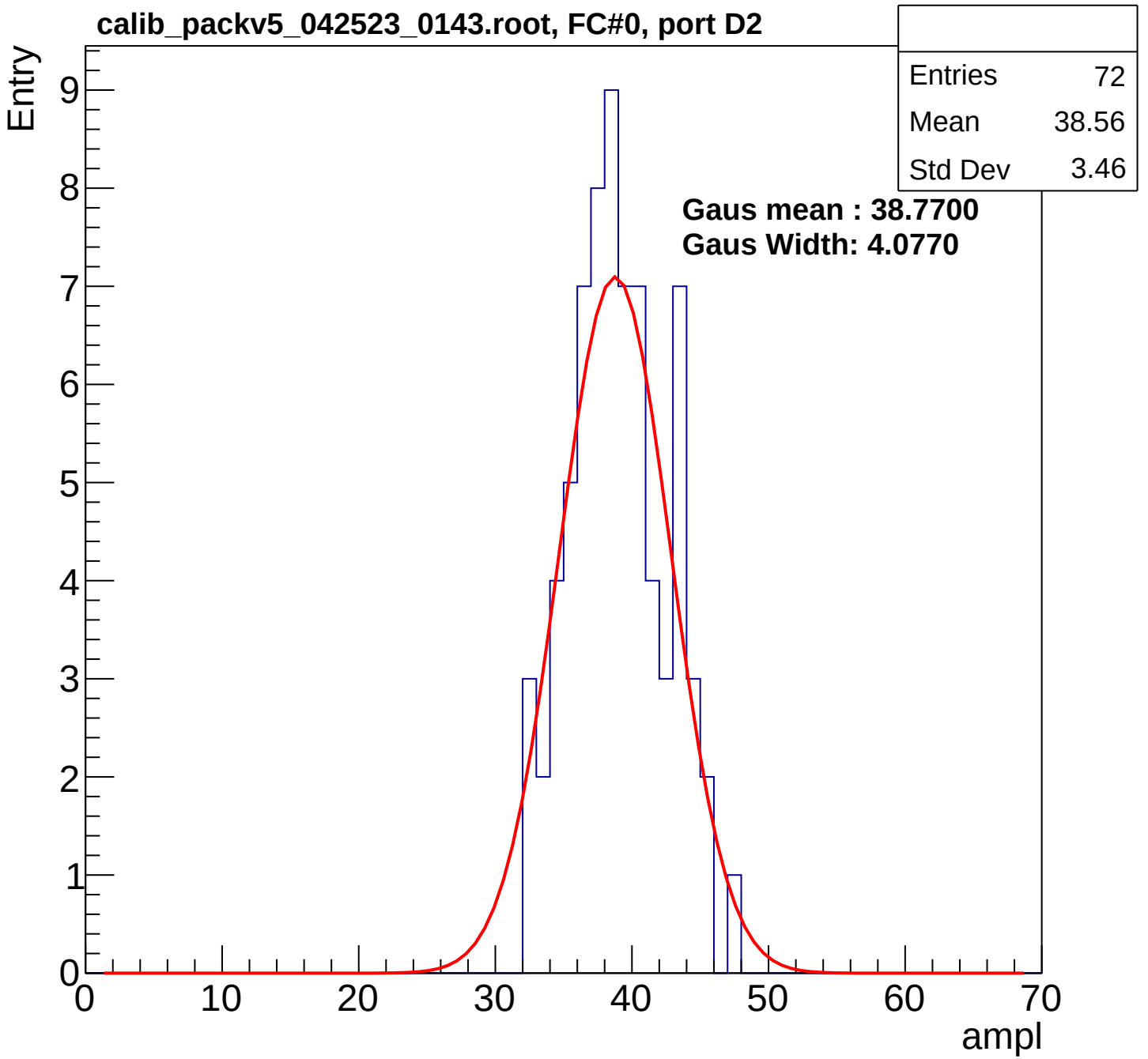
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch36, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 29.82
Std Dev 5.881
Gaus mean : 31.6243
Gaus Width: 3.7124
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch36, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 38.56
Std Dev 3.46
Gaus mean : 38.7700
Gaus Width: 4.0770
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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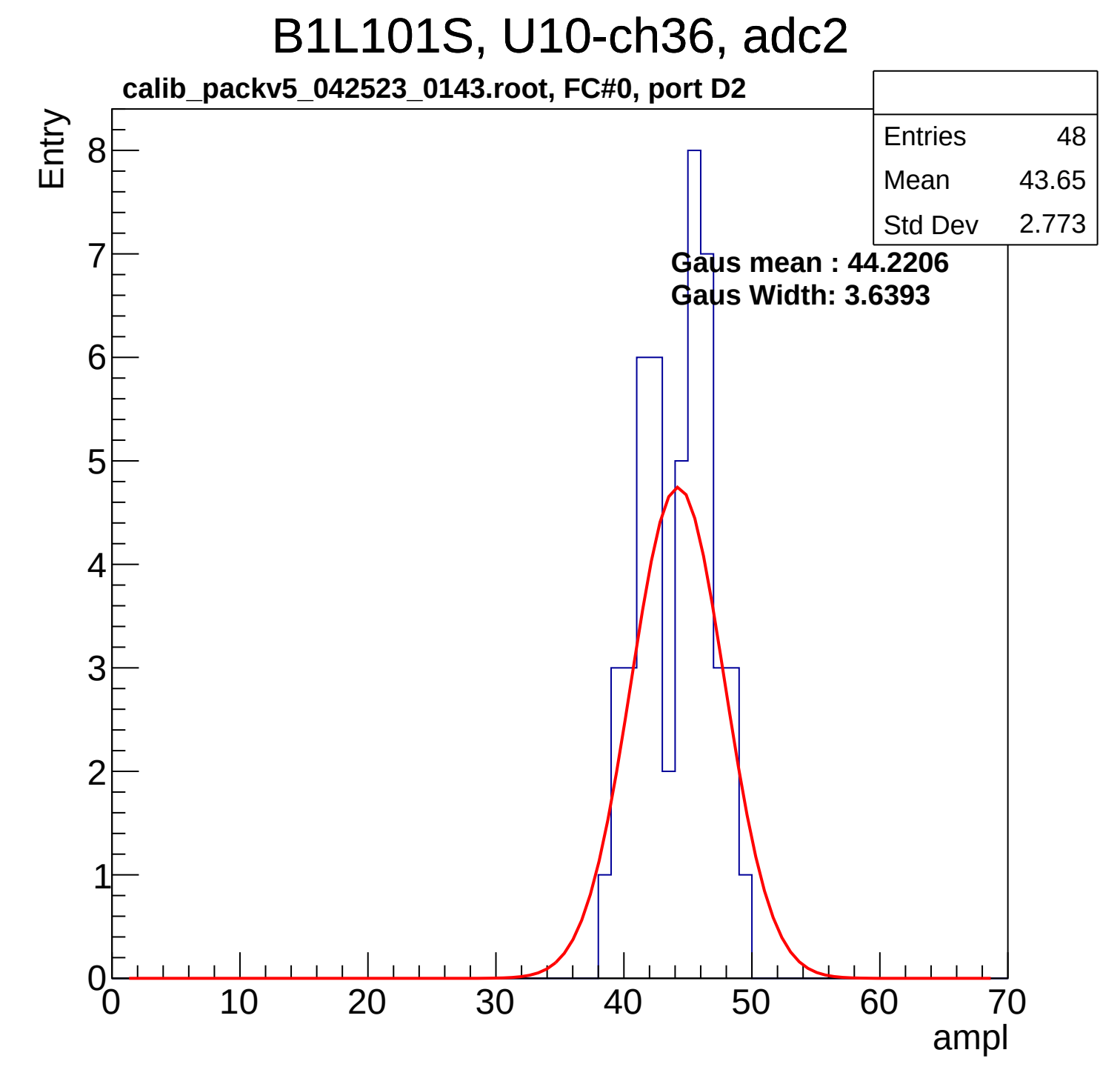
B1L101S, U10-ch36, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 43.65
Std Dev 2.773
Gaus mean : 44.2206
Gaus Width: 3.6393
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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20
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40
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60
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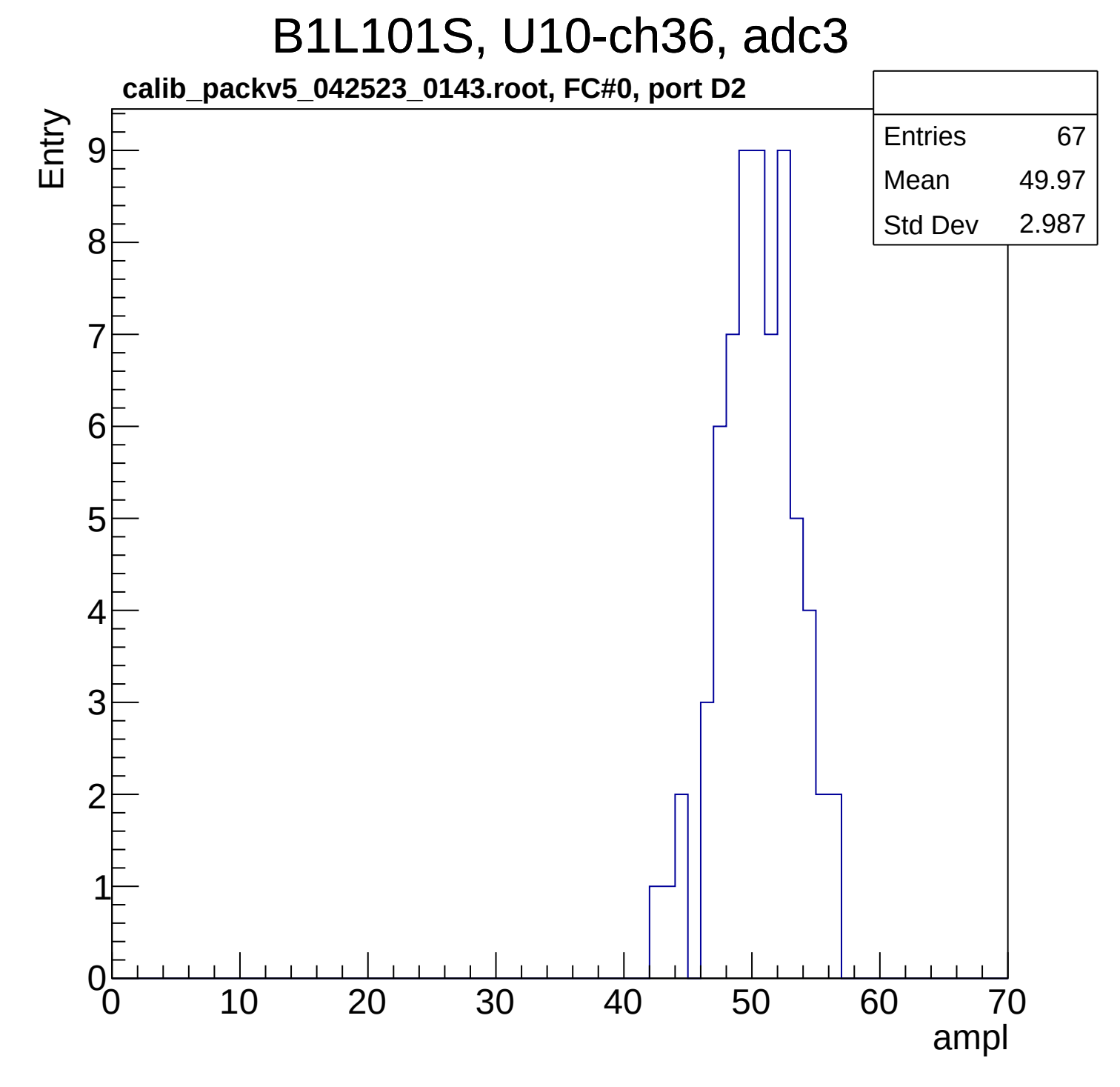
B1L101S, U10-ch36, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 49.97
Std Dev 2.987
Entry
ampl
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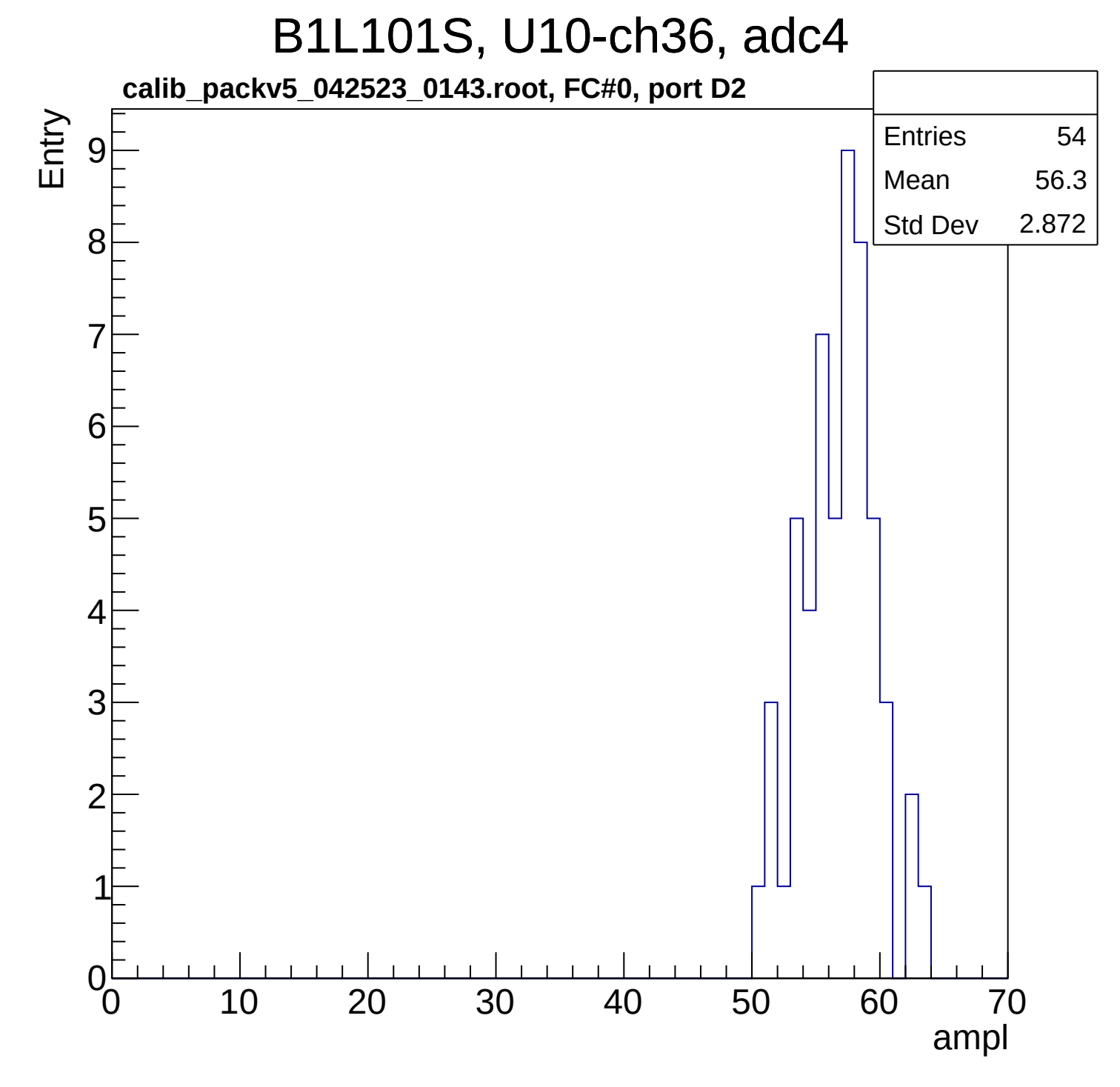
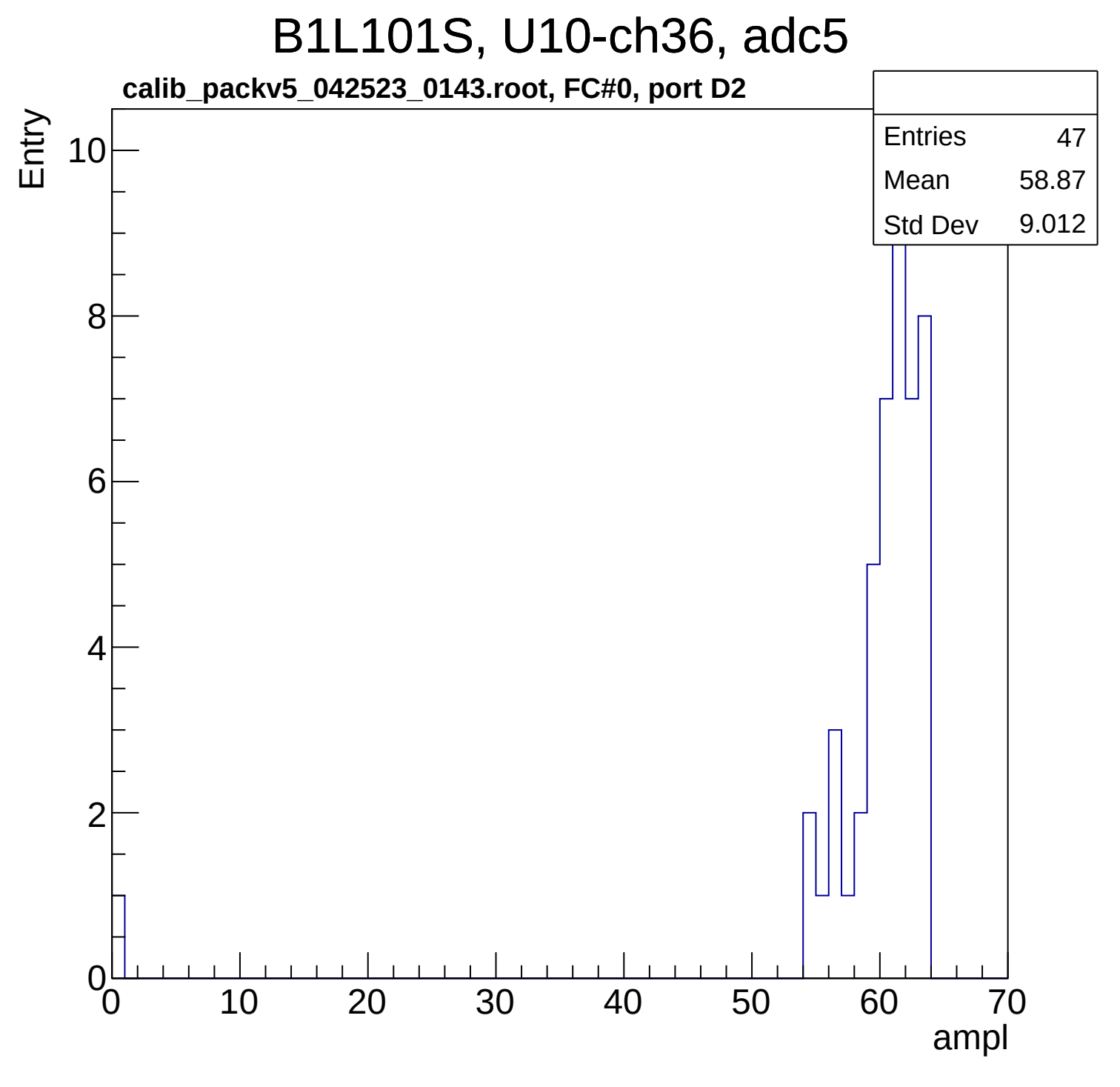
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch36, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 56.3
Std Dev 2.872
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch36, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 58.87
Std Dev 9.012
Entry
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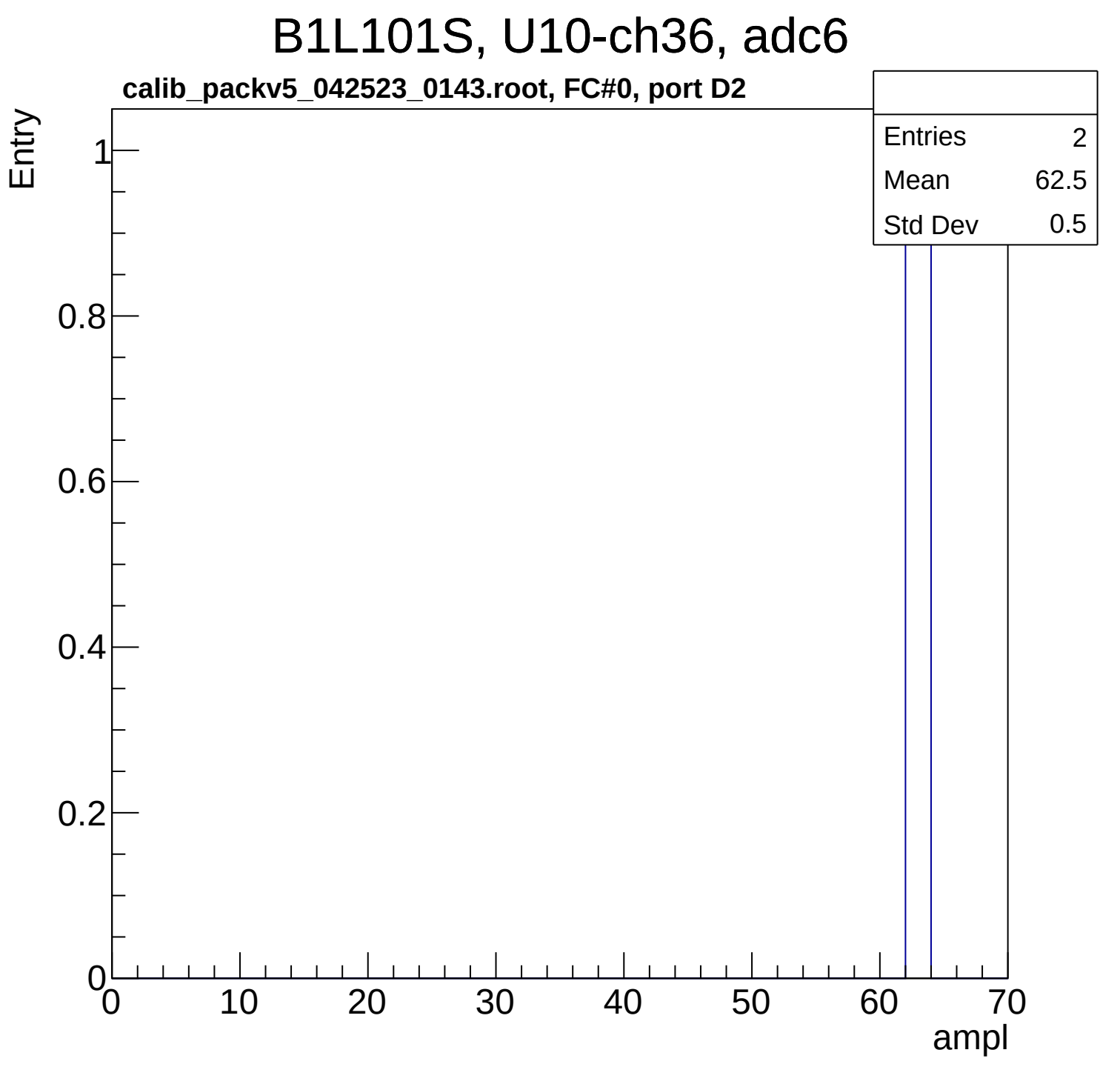
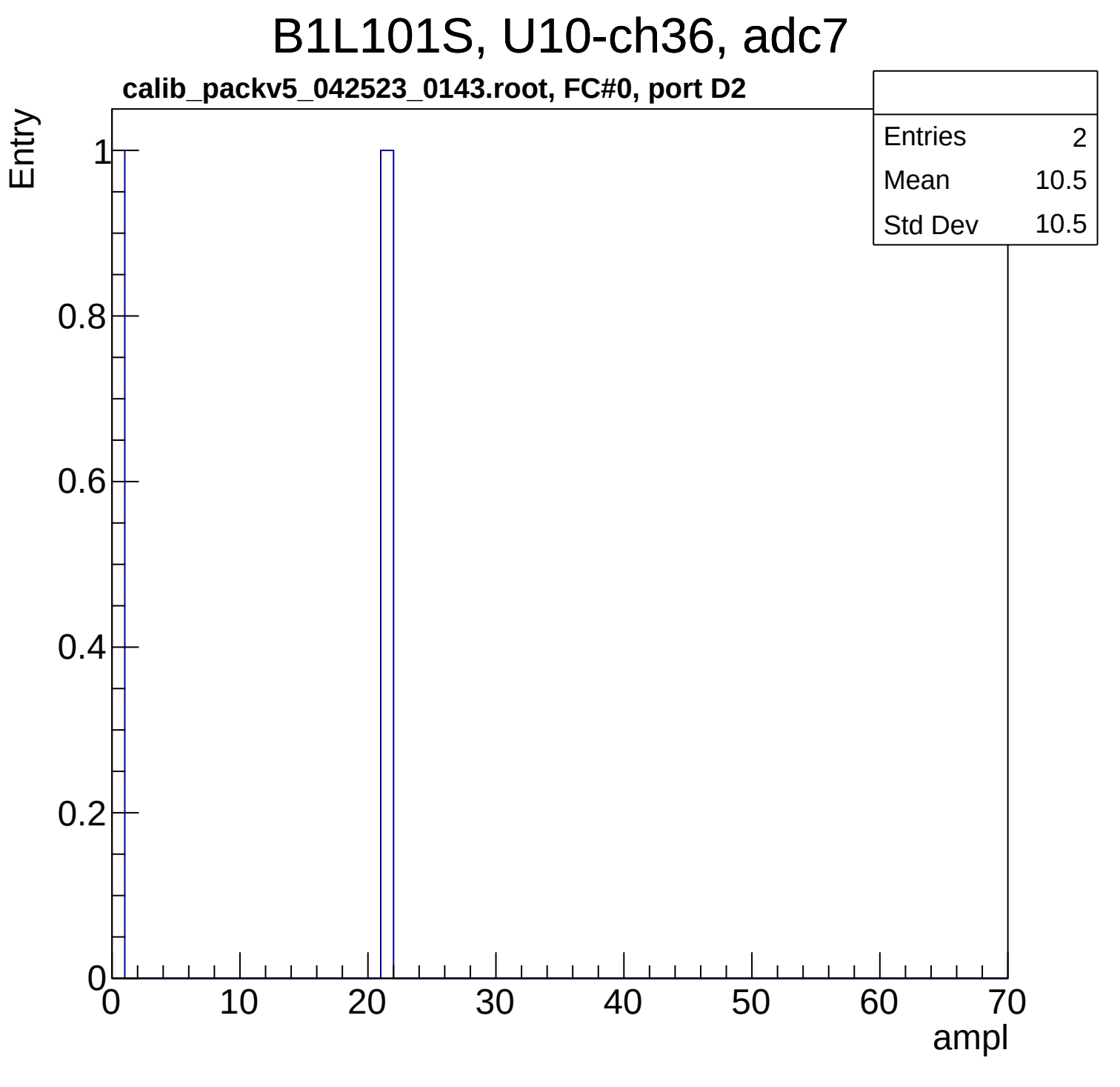
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch36, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch36, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 10.5
Std Dev 10.5
Entry
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0.6
0.4
0.2
0
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10
20
30
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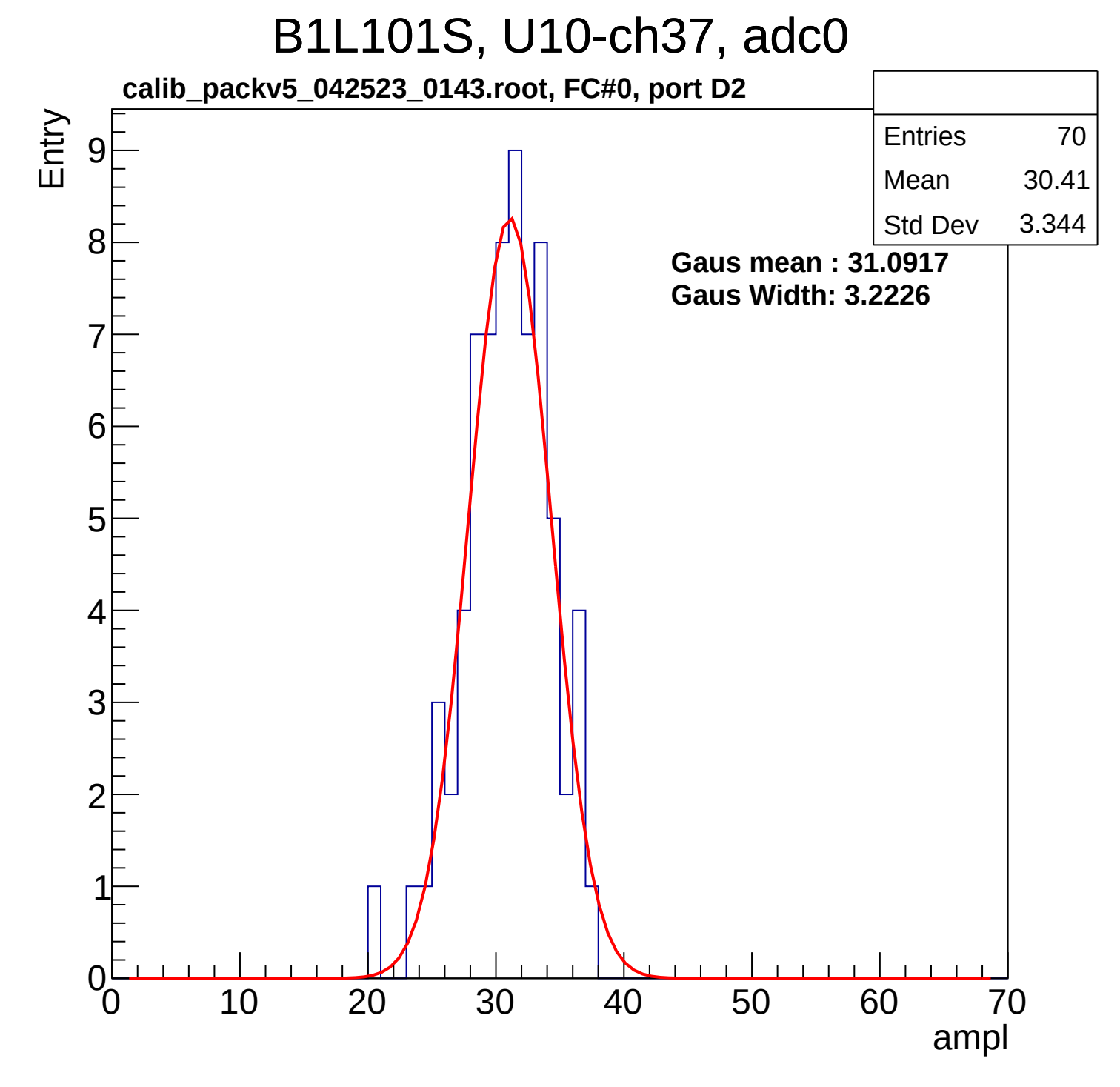
50
60
70
ampl


B1L101S, U10-ch37, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 30.41
Std Dev 3.344
Gaus mean : 31.0917
Gaus Width: 3.2226
Entry
ampl
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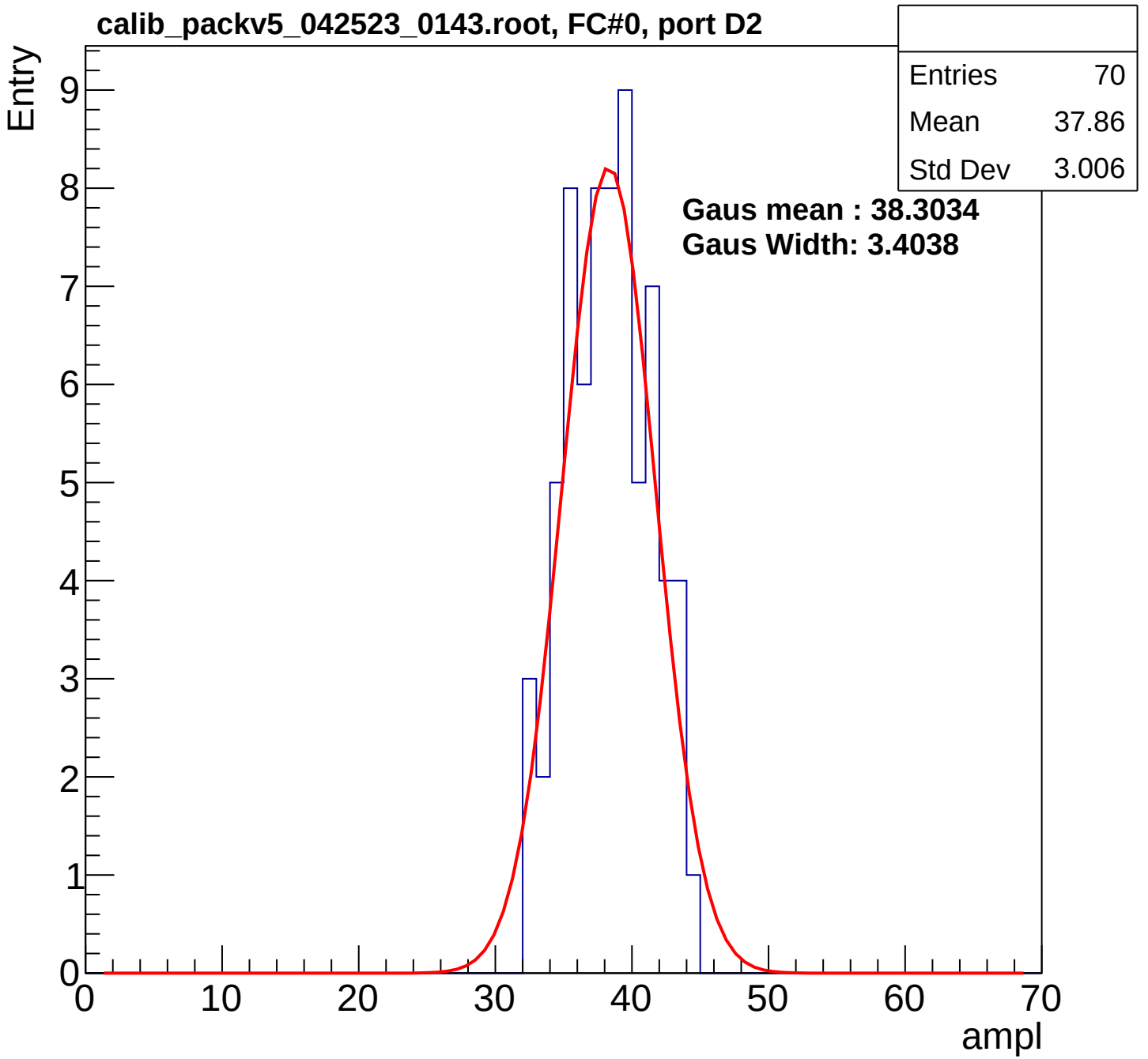
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch37, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 37.86
Std Dev 3.006
Gaus mean : 38.3034
Gaus Width: 3.4038
Entry
ampl
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3
4
5
6
7
8
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0
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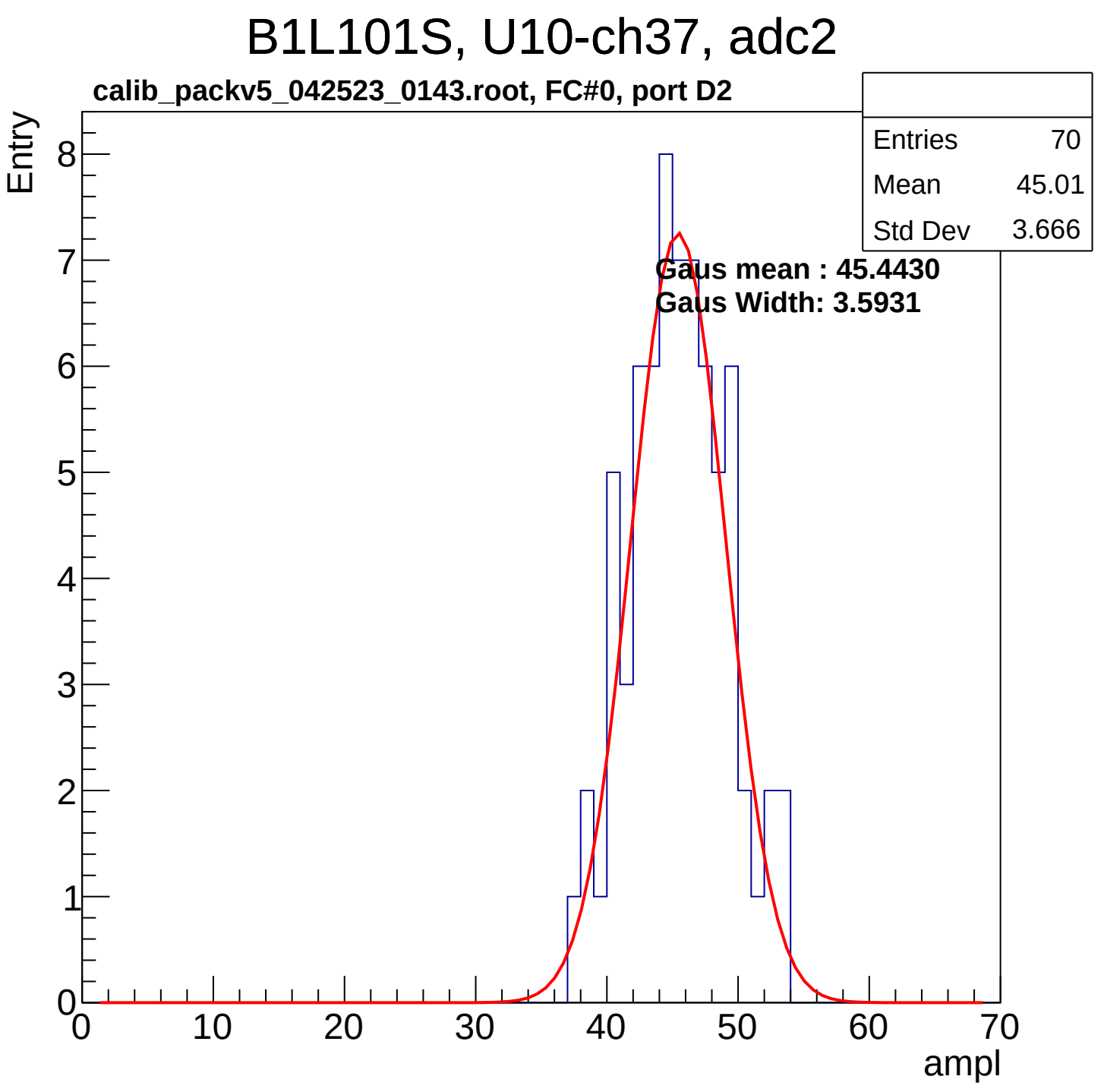
30
40
50
60
70


B1L101S, U10-ch37, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 45.01
Std Dev 3.666
Gaus mean : 45.4430
Gaus Width: 3.5931
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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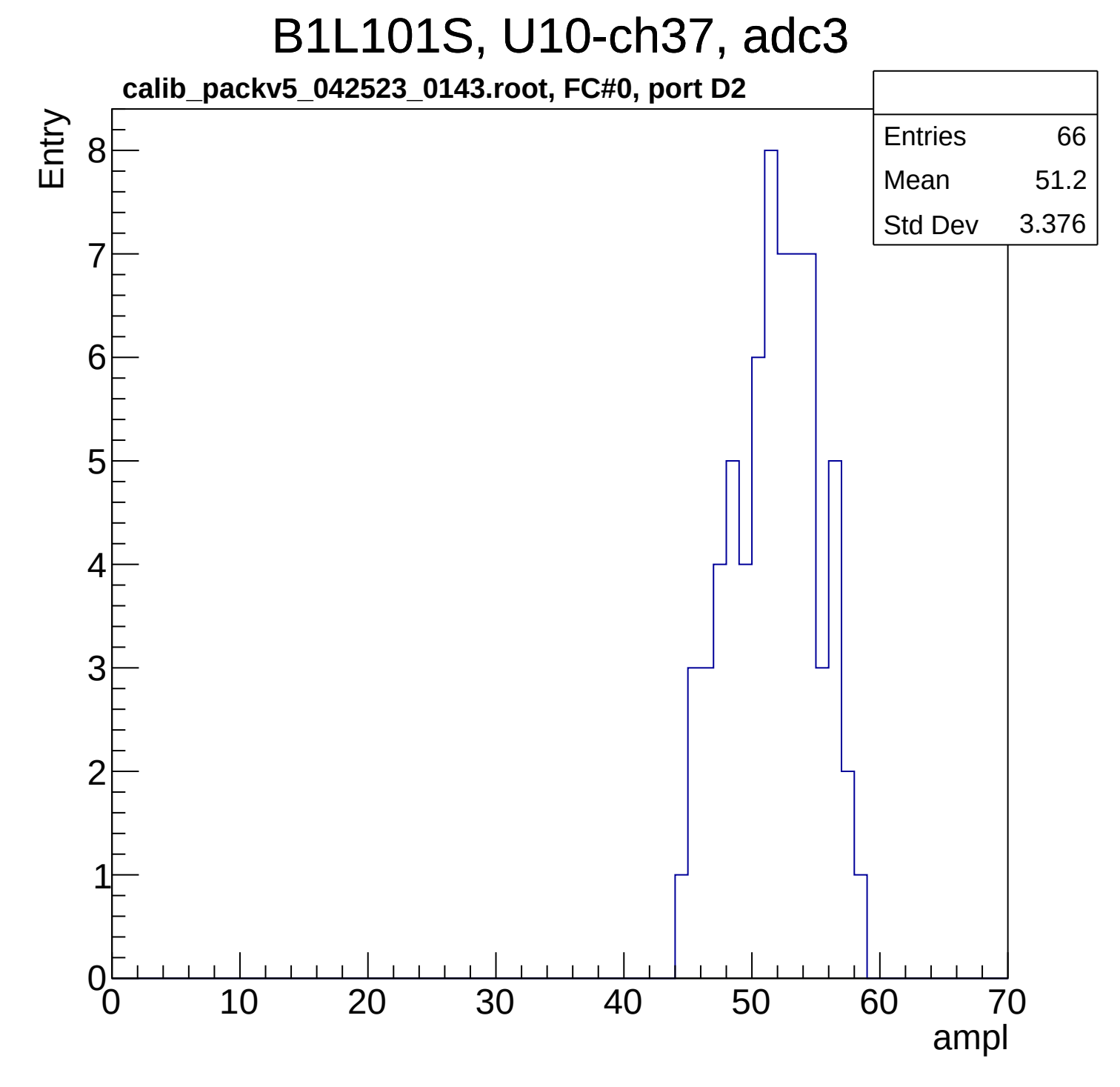
B1L101S, U10-ch37, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 51.2
Std Dev 3.376
Entry
ampl
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3
4
5
6
7
8
0
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20
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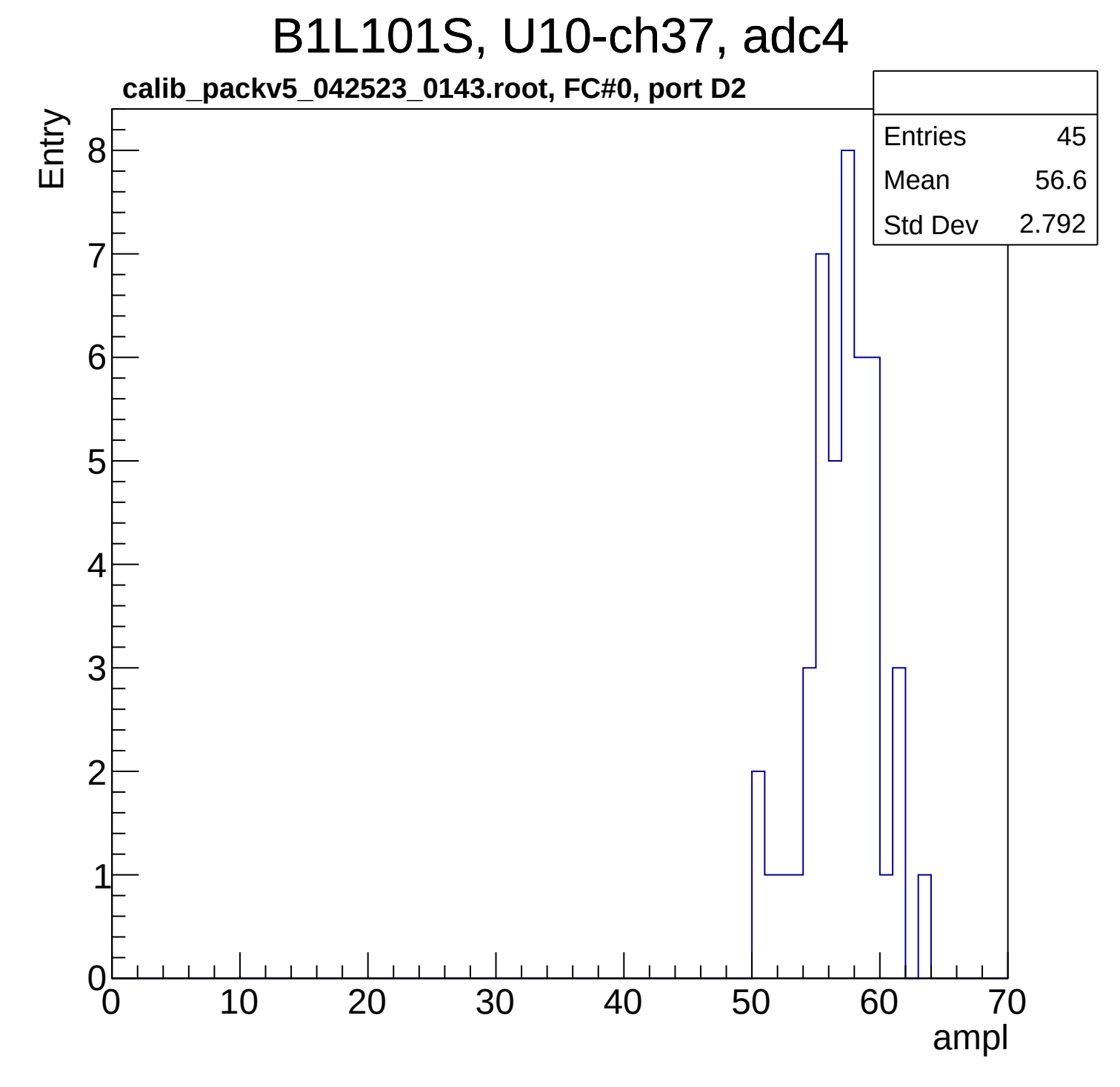
40
50
60
70


B1L101S, U10-ch37, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 56.6
Std Dev 2.792
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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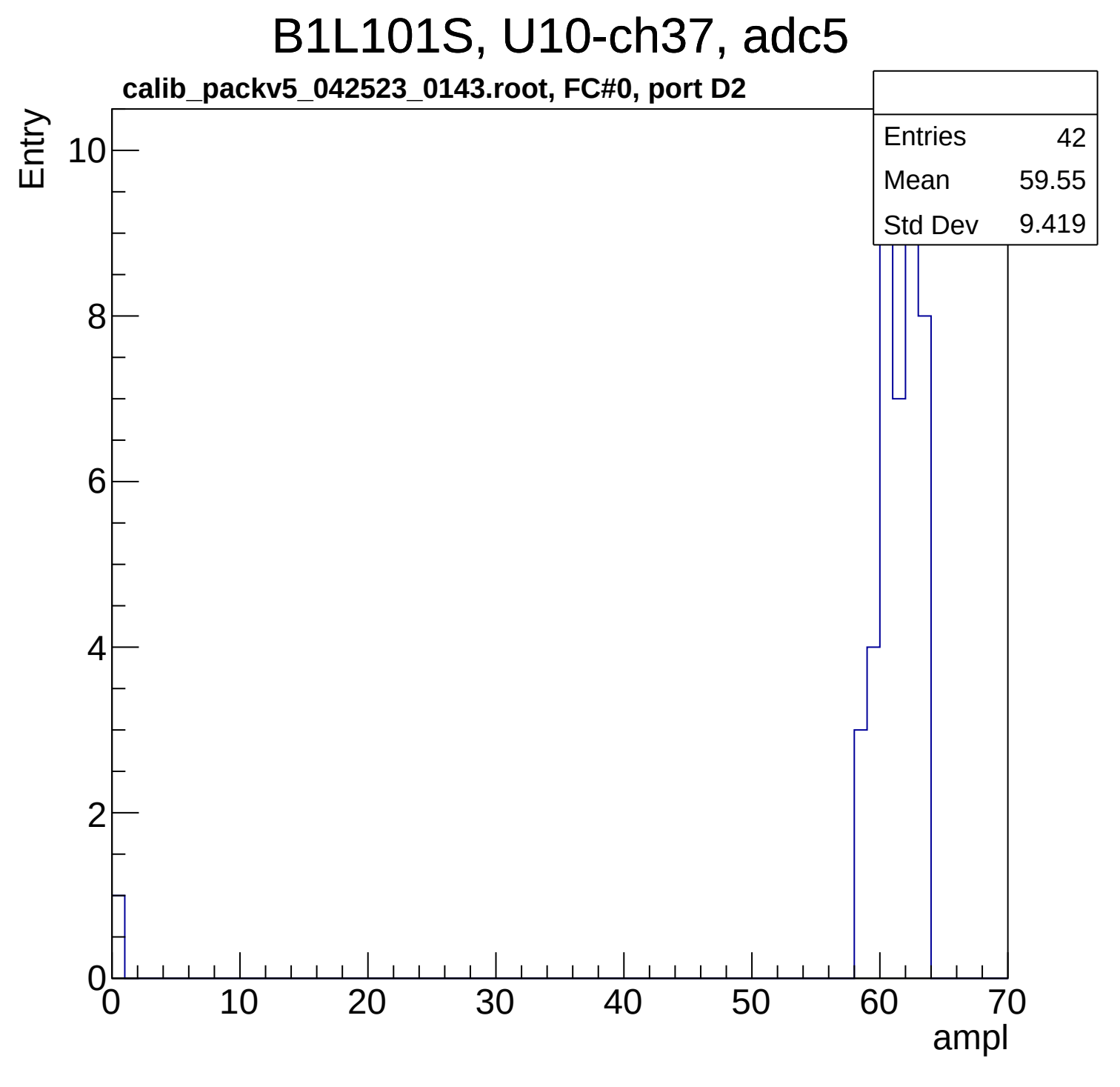
B1L101S, U10-ch37, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 59.55
Std Dev 9.419
Entry
0
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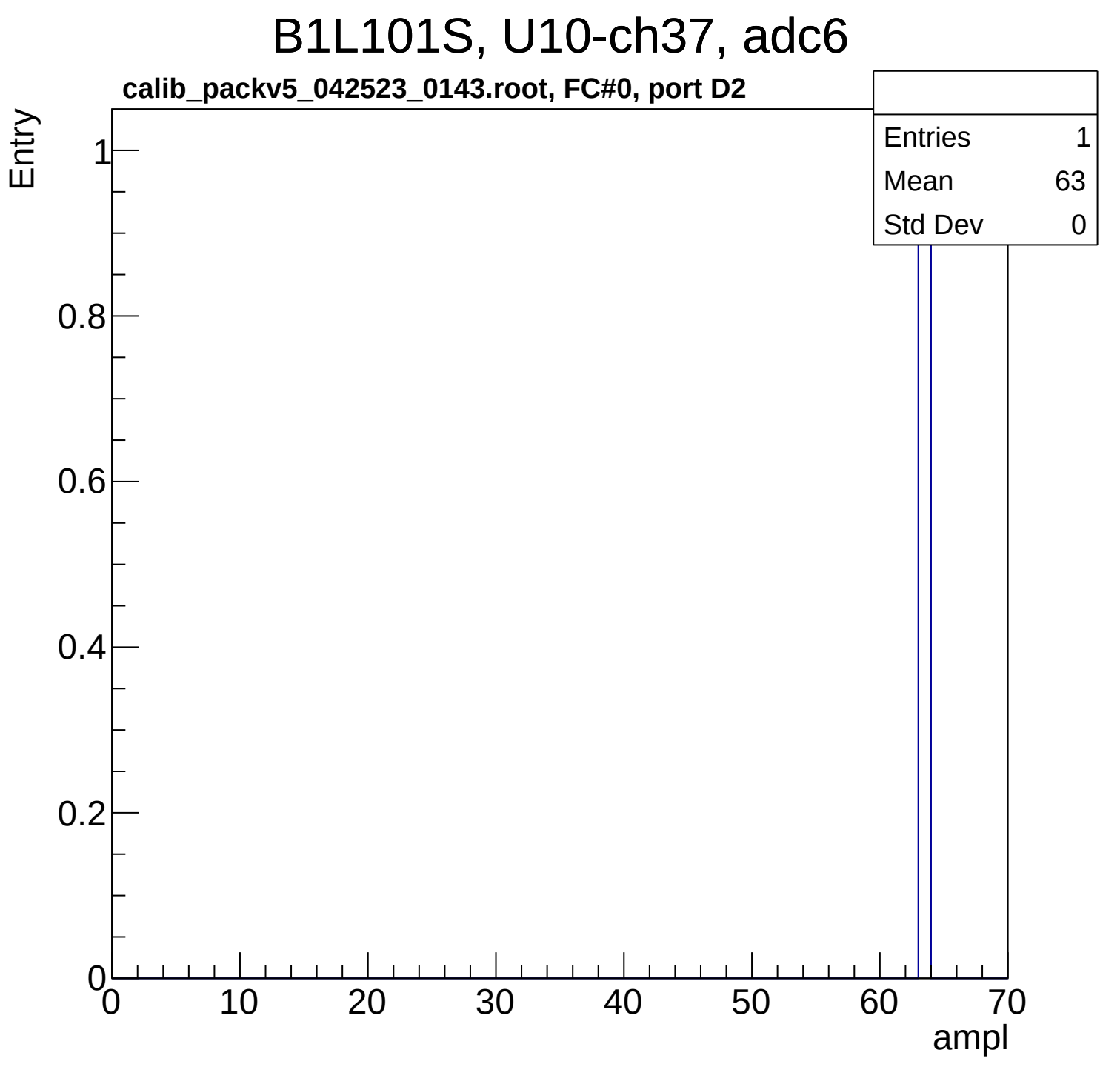
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch37, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 63
Std Dev 0
Entry
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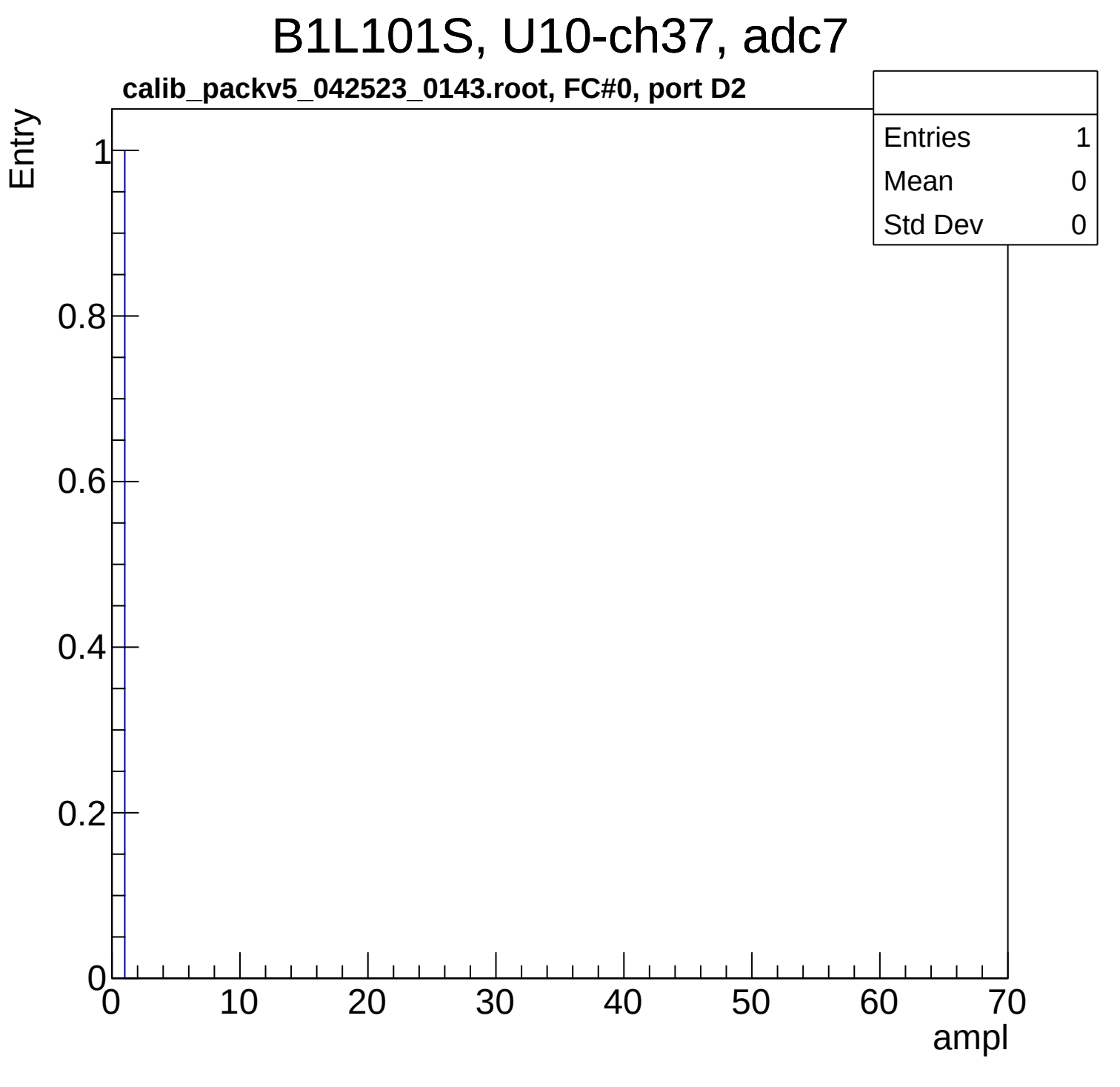
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch37, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
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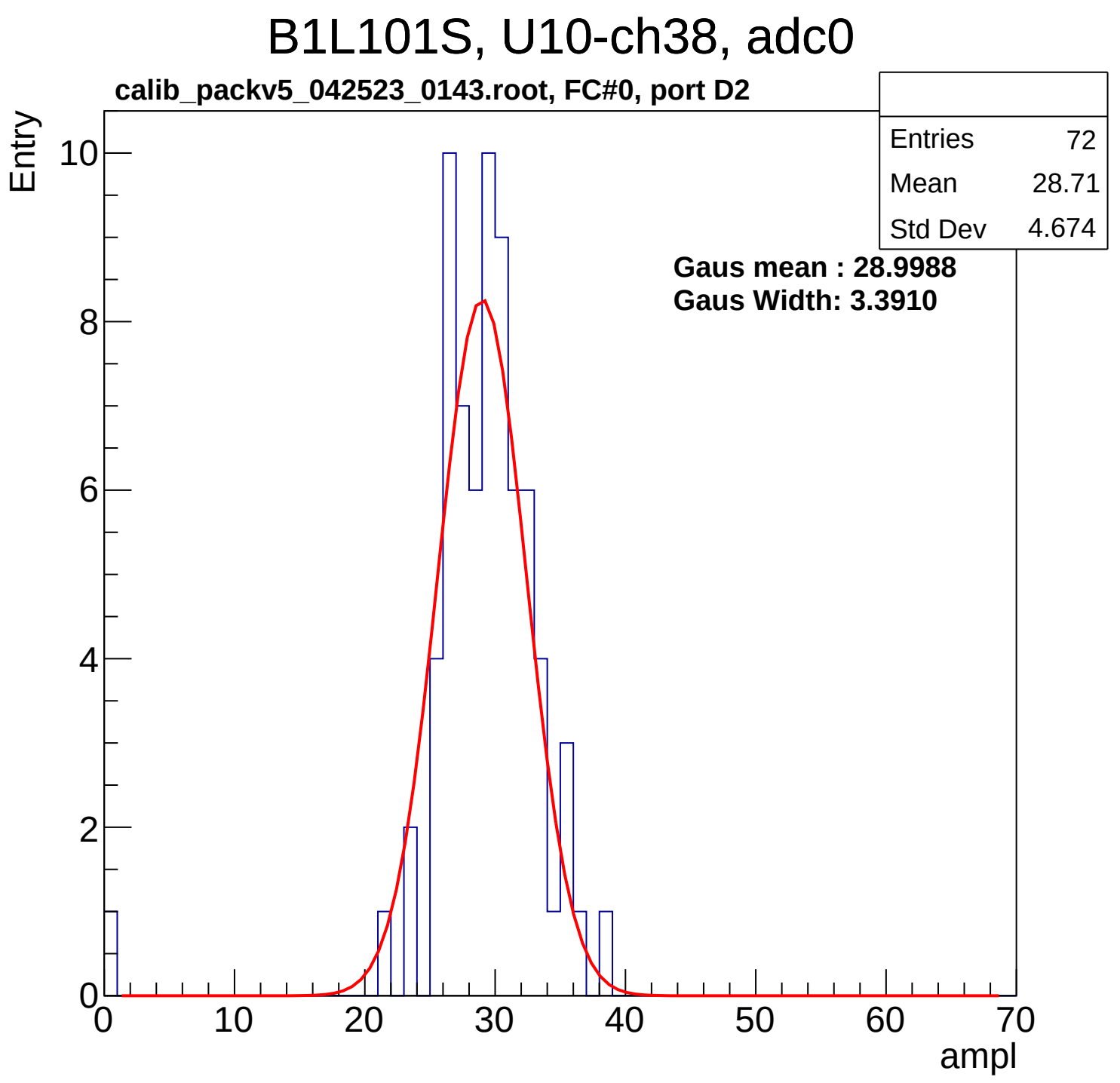
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch38, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 28.71
Std Dev 4.674
Gaus mean : 28.9988
Gaus Width: 3.3910
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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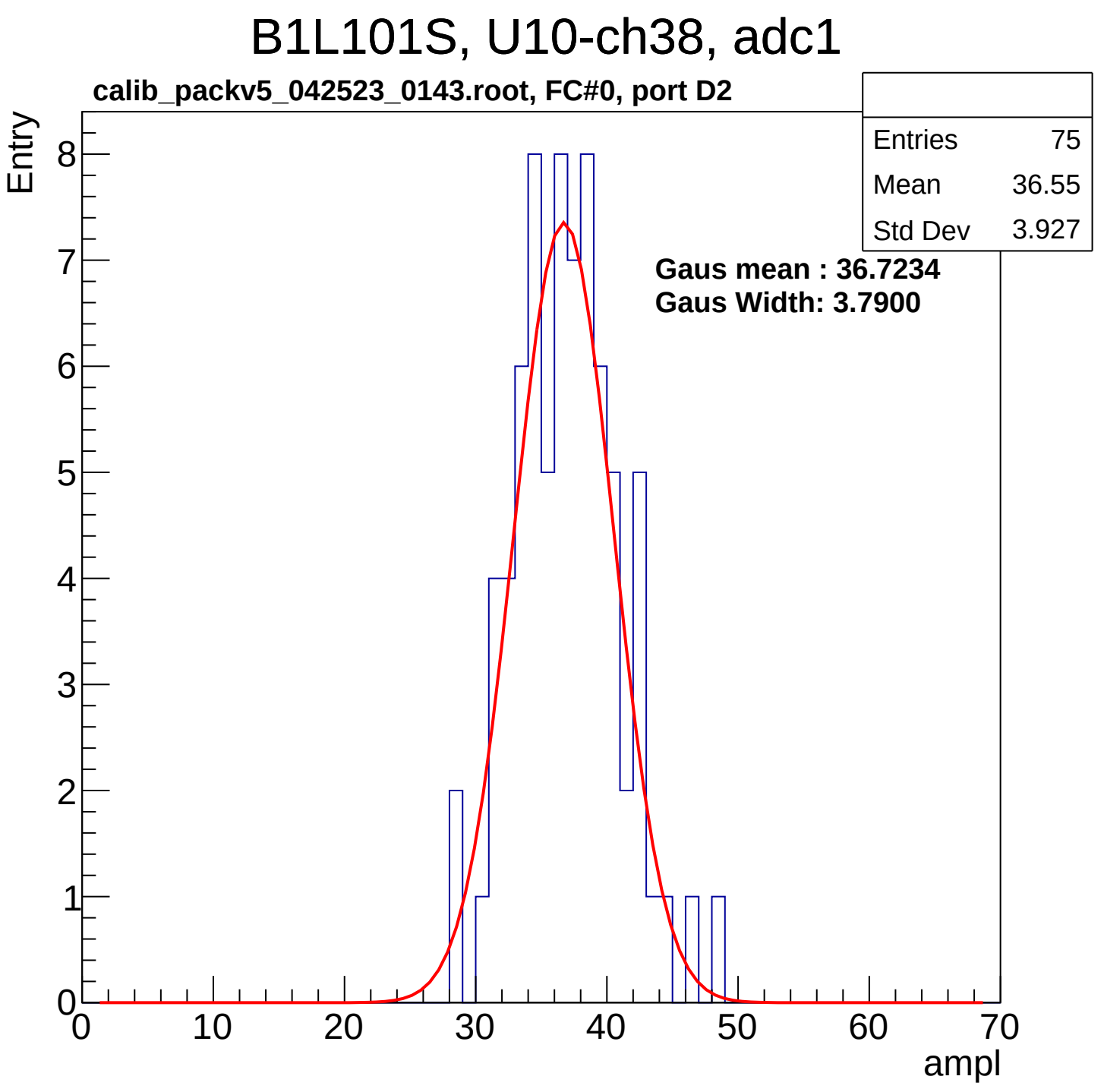
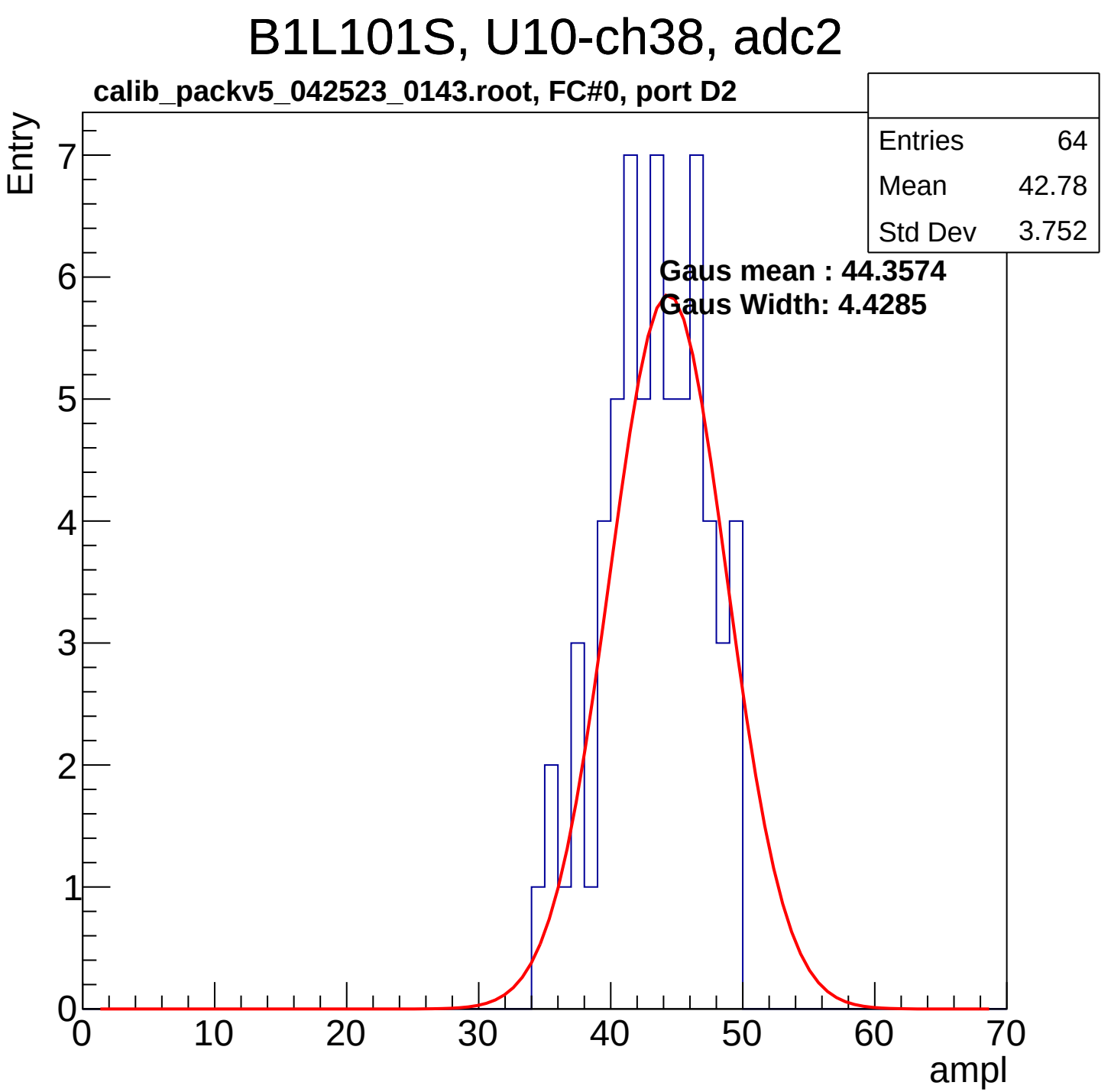

B1L101S, U10-ch38, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 36.55
Std Dev 3.927
Gaus mean : 36.7234
Gaus Width: 3.7900
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch38, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 42.78
Std Dev 3.752
Gaus mean : 44.3574
Gaus Width: 4.4285
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
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60
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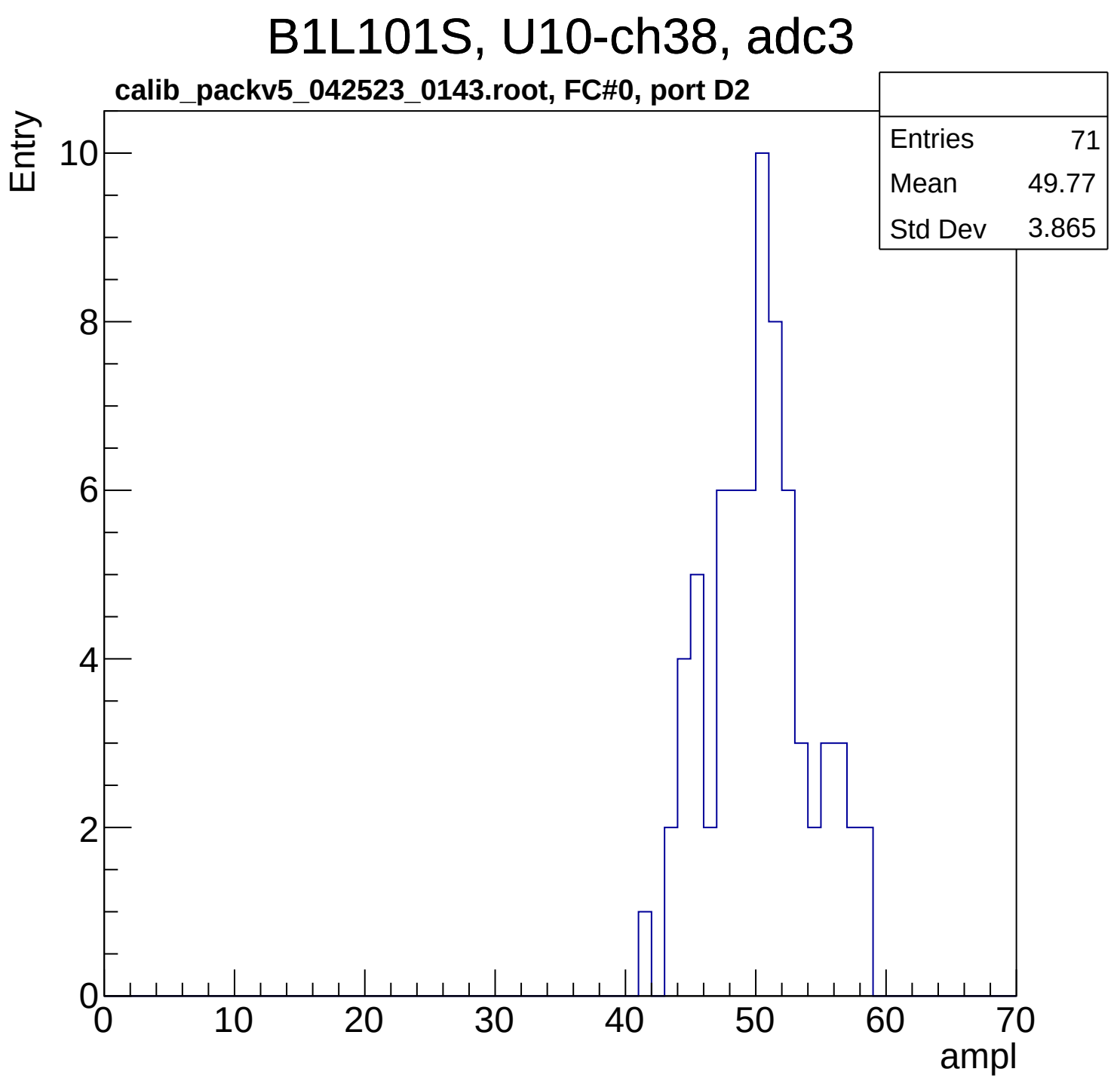
B1L101S, U10-ch38, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 49.77
Std Dev 3.865
Entry
ampl
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10
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40
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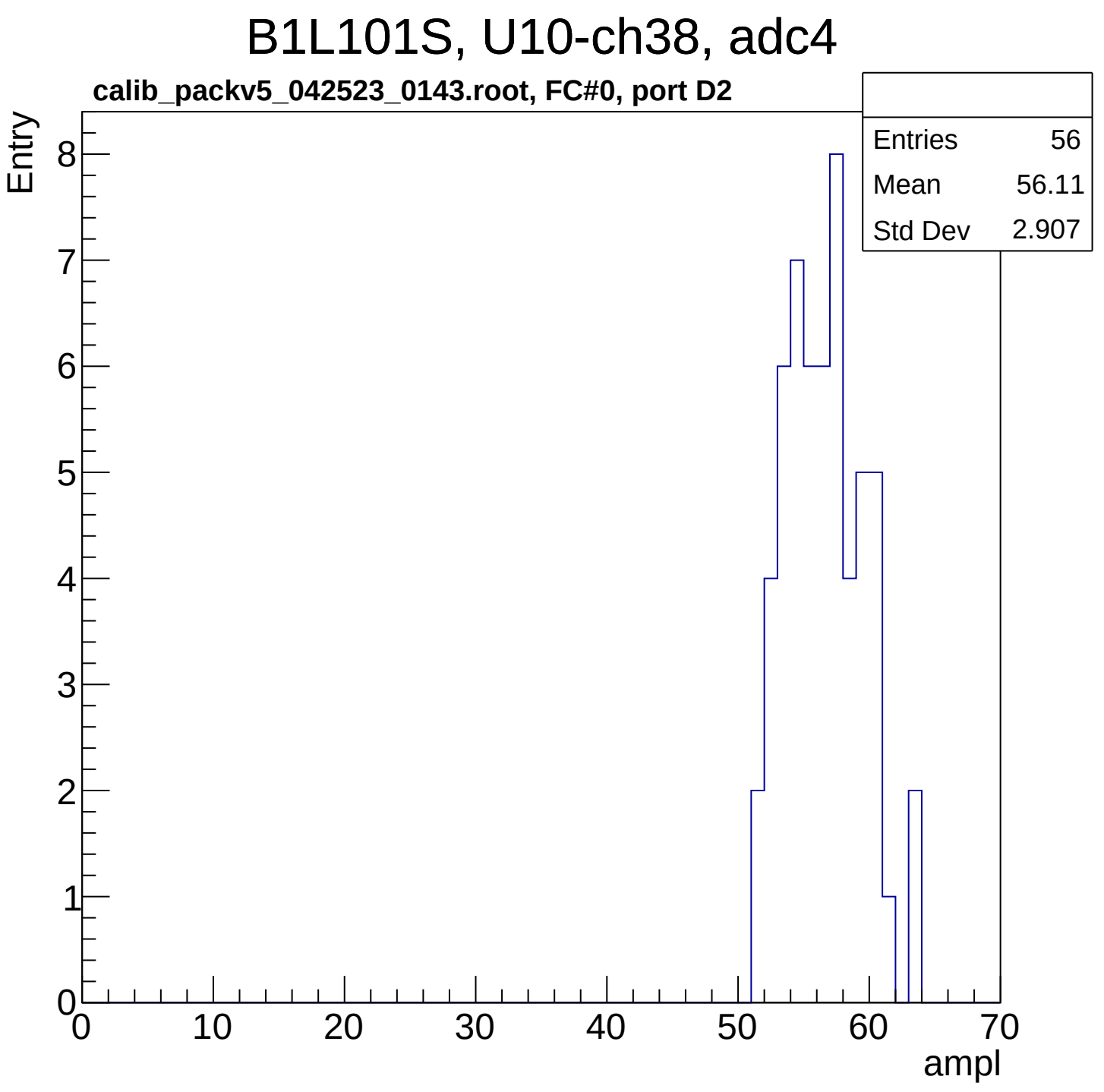
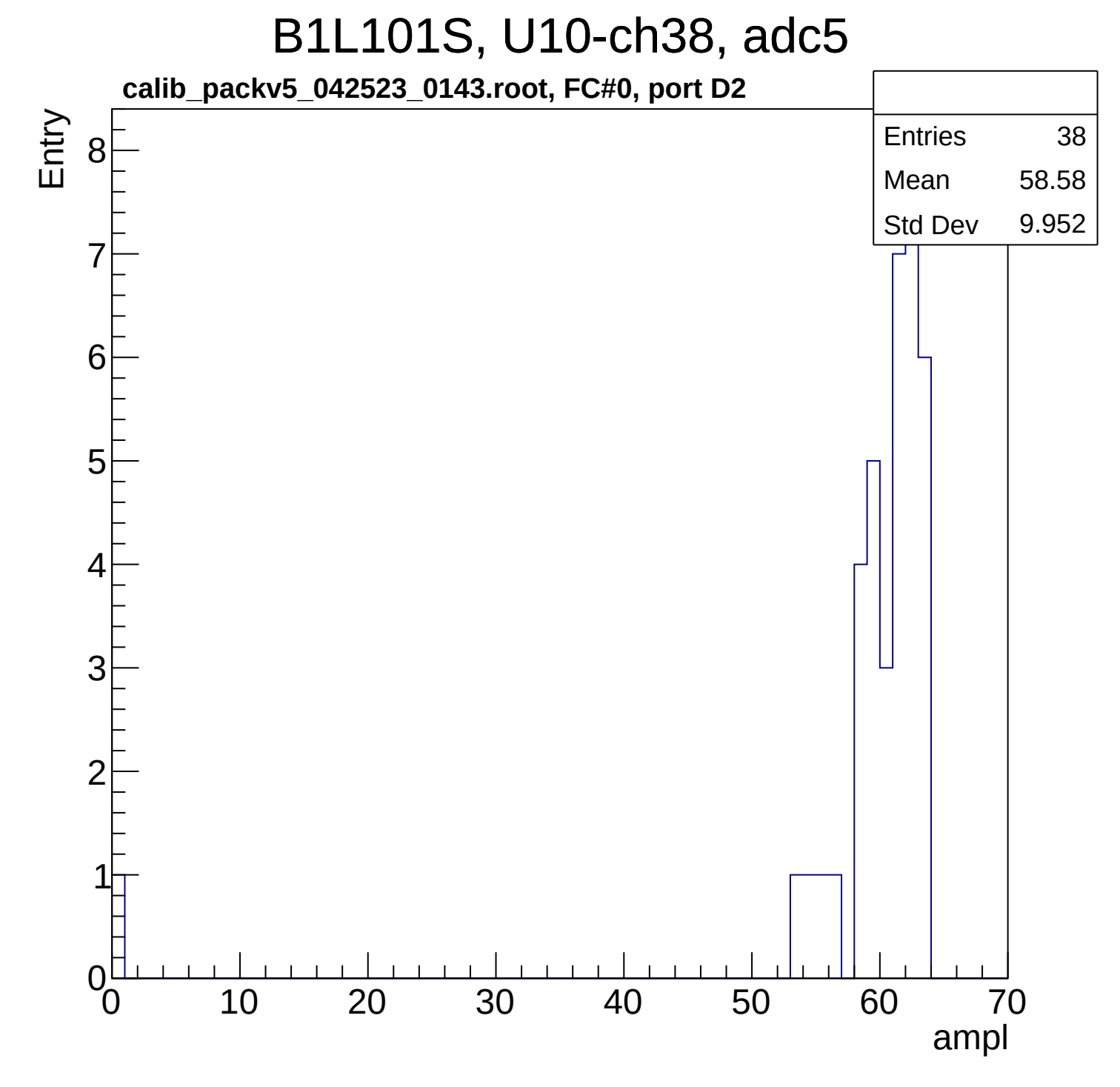

B1L101S, U10-ch38, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 56.11
Std Dev 2.907
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch38, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 38
Mean 58.58
Std Dev 9.952
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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20
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40
50
60
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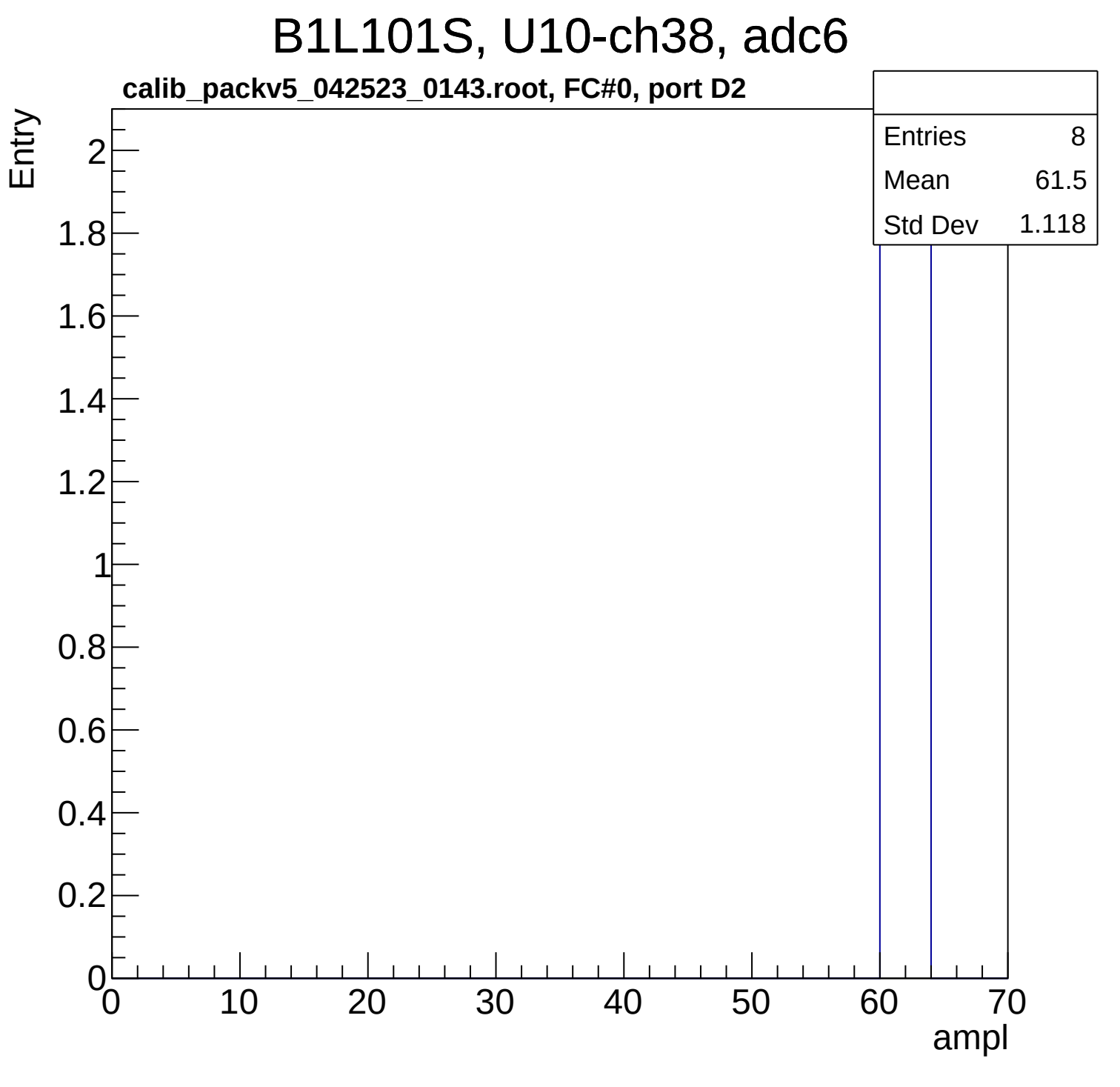
B1L101S, U10-ch38, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 61.5
Std Dev 1.118
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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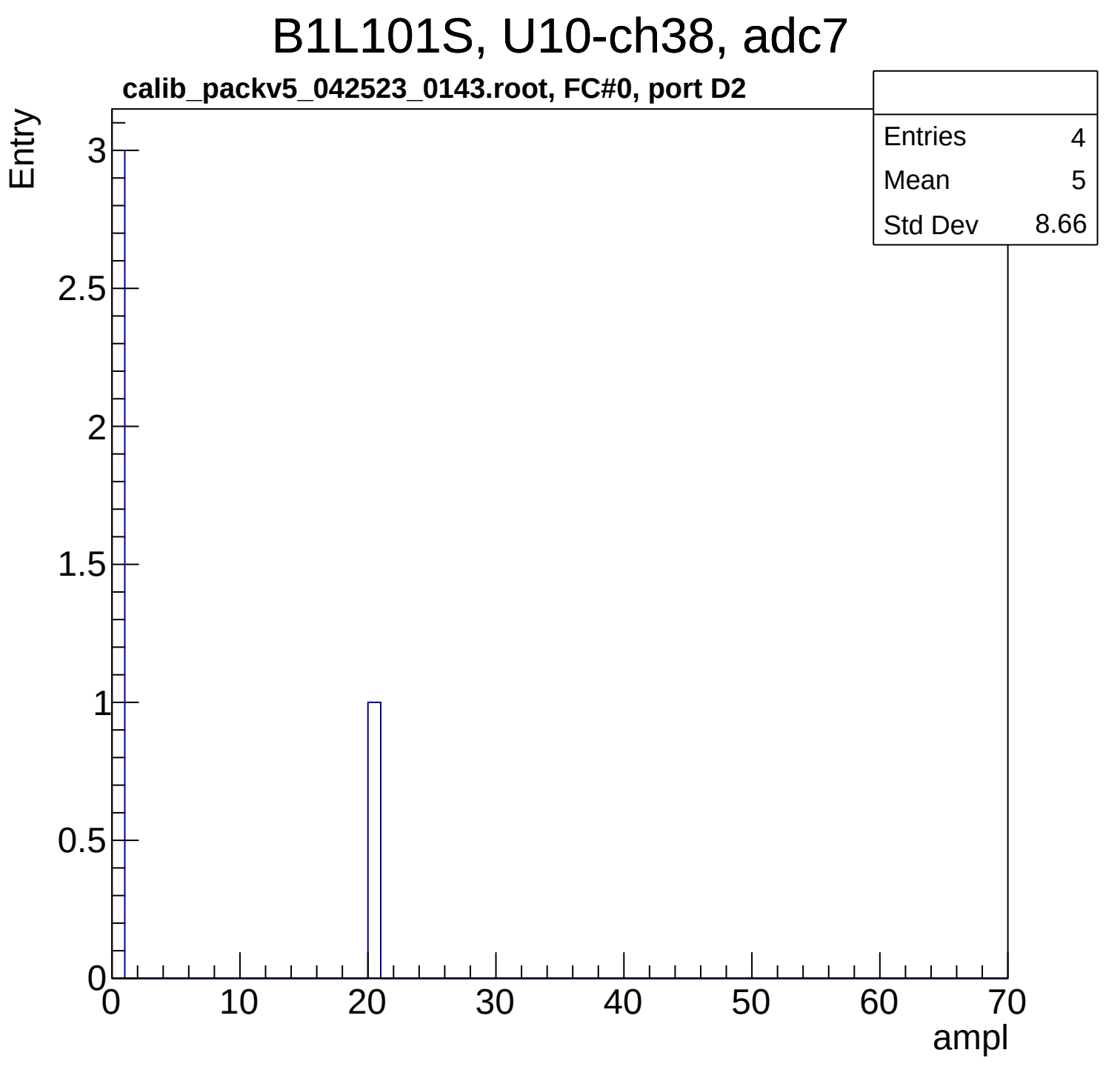
B1L101S, U10-ch38, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 5
Std Dev 8.66
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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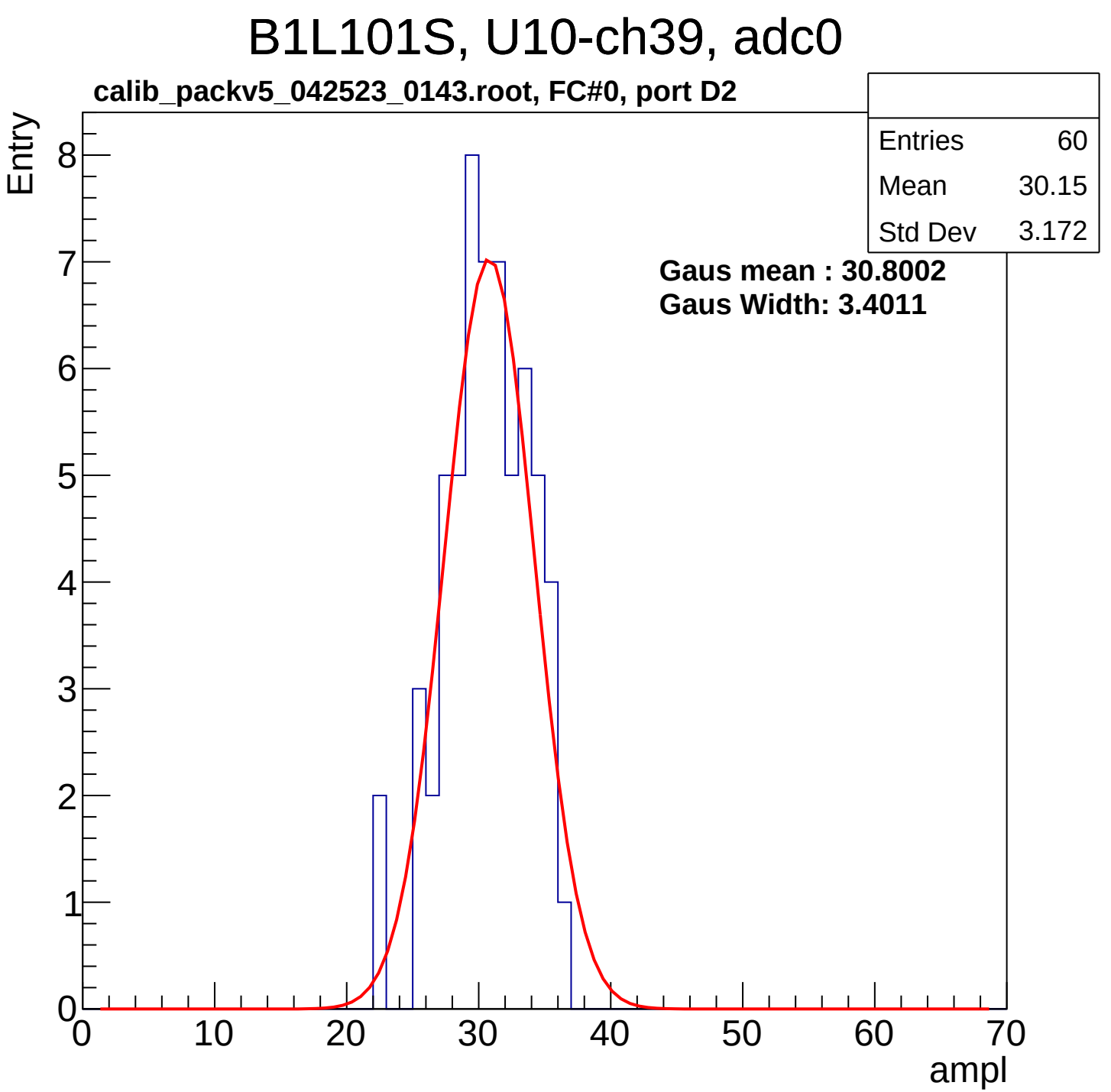
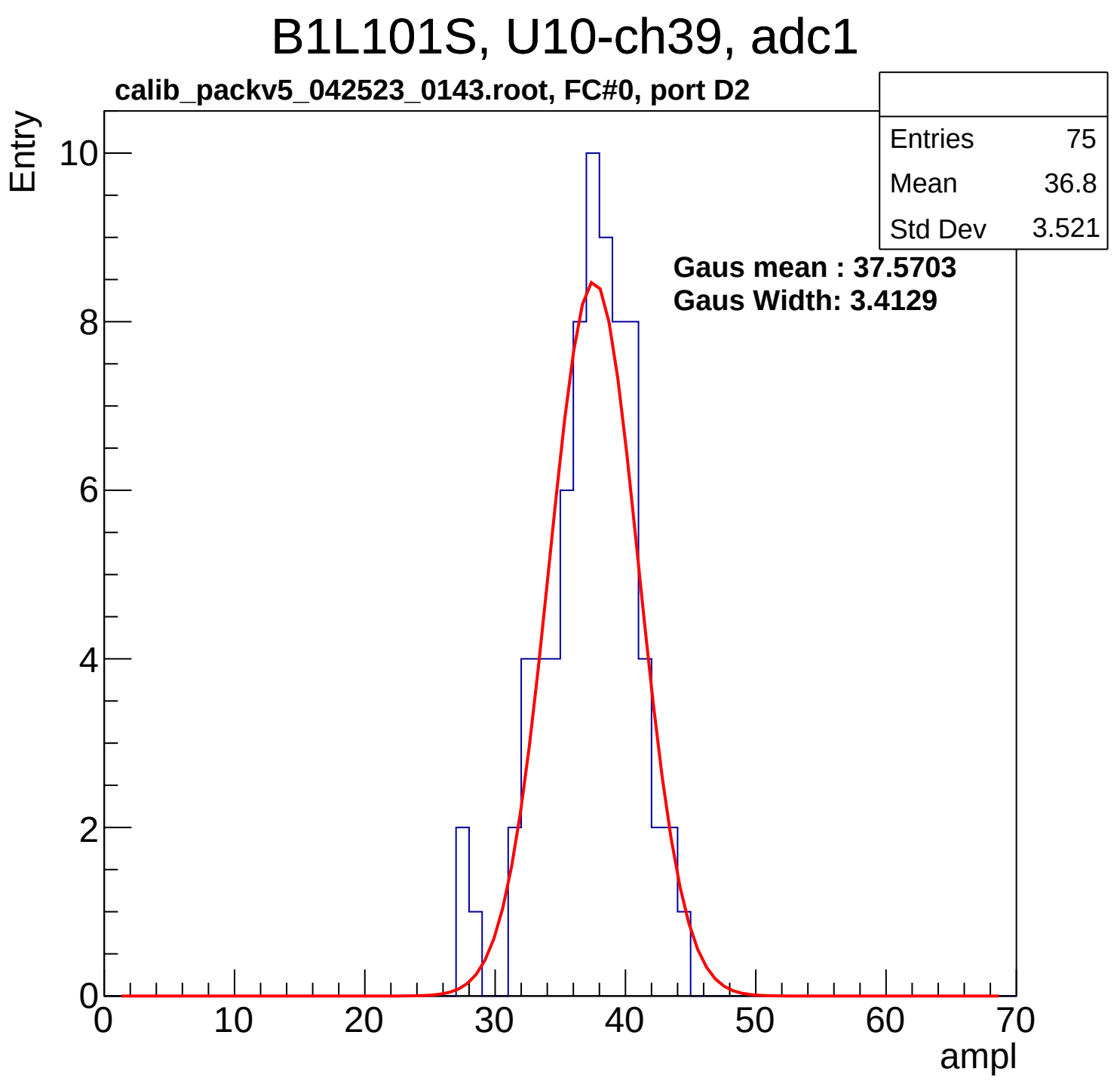

B1L101S, U10-ch39, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 30.15
Std Dev 3.172
Gaus mean : 30.8002
Gaus Width: 3.4011
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch39, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 36.8
Std Dev 3.521
Gaus mean : 37.5703
Gaus Width: 3.4129
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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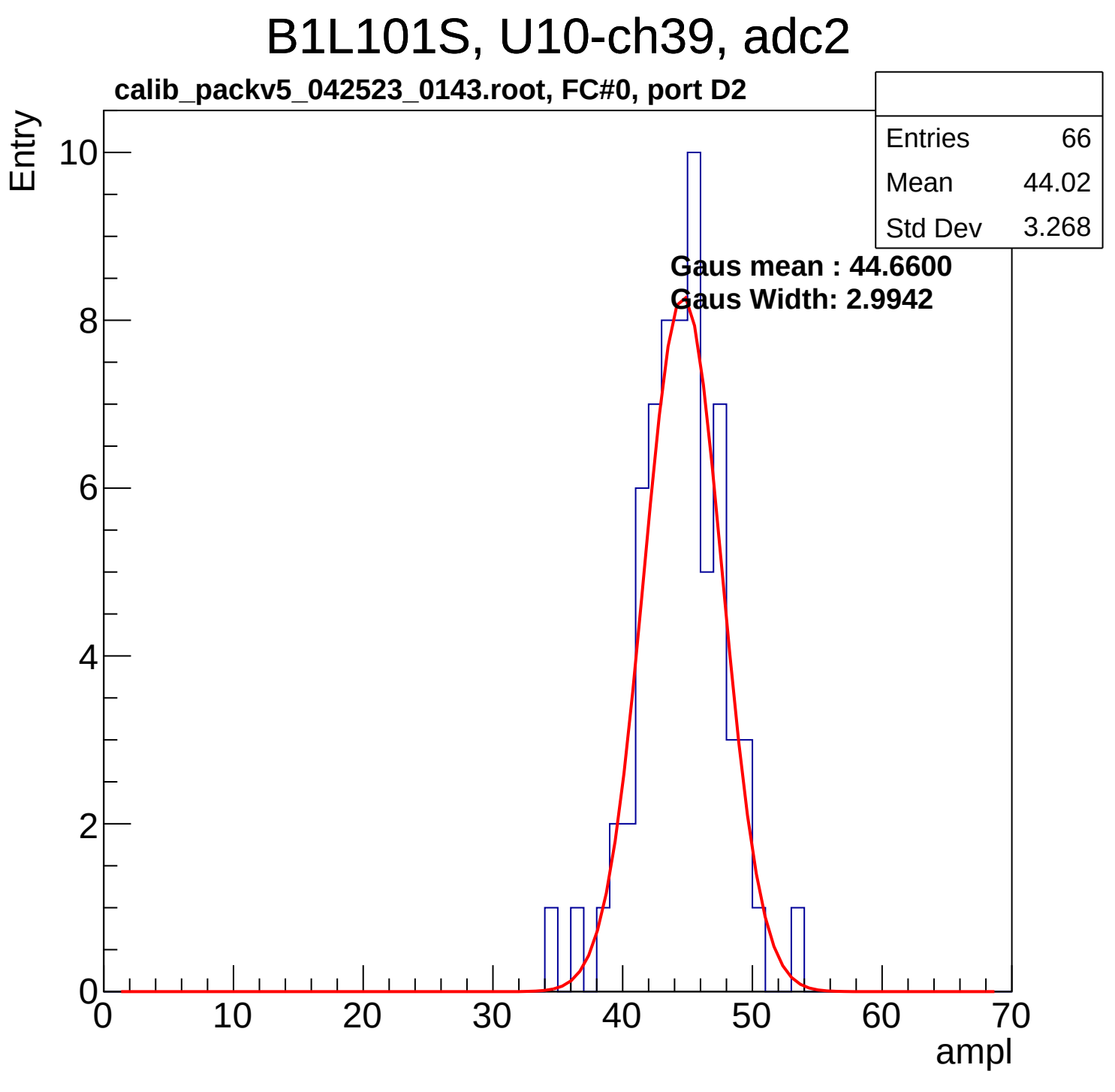
B1L101S, U10-ch39, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 44.02
Std Dev 3.268
Gaus mean : 44.6600
Gaus Width: 2.9942
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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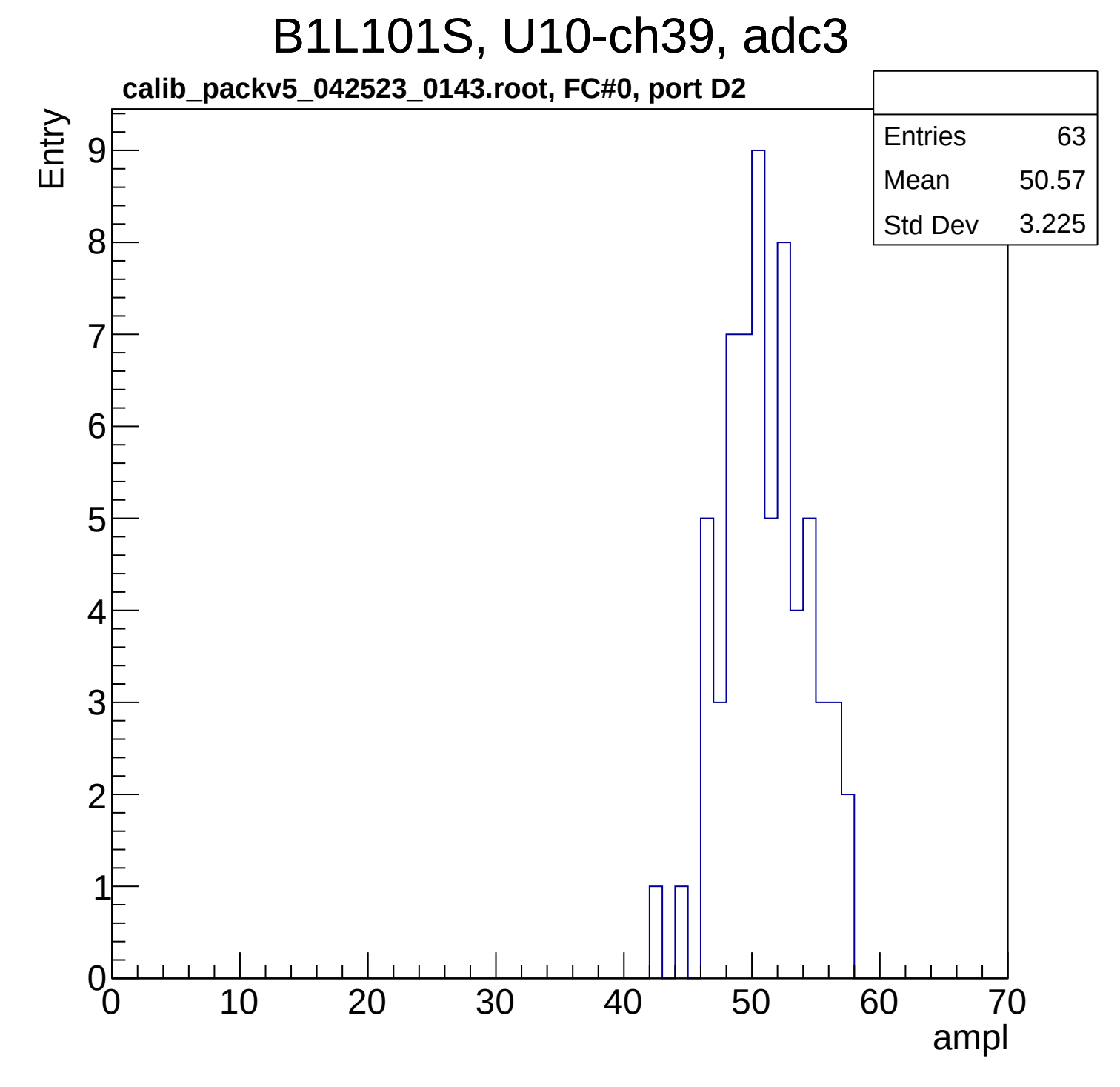
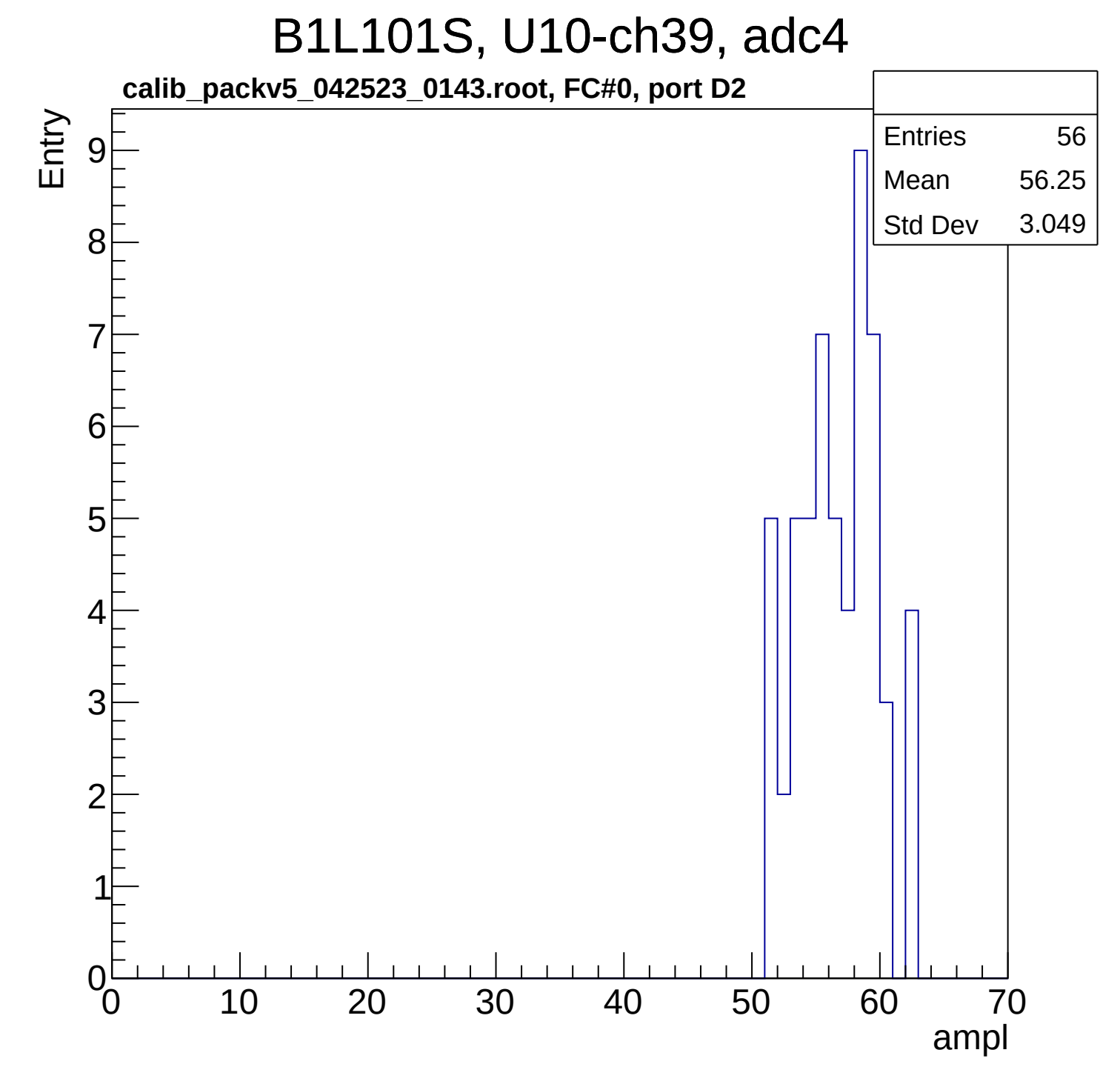
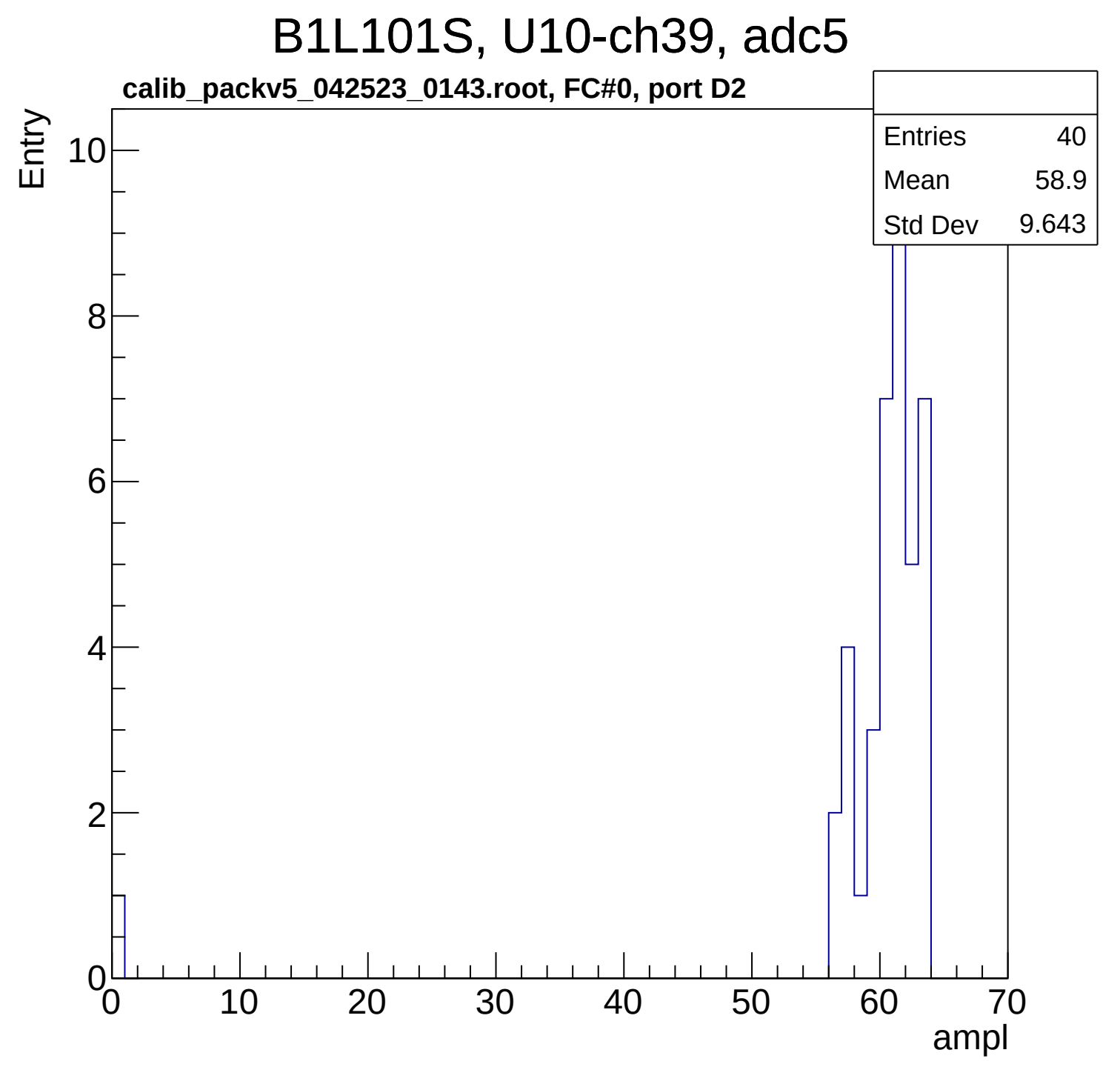
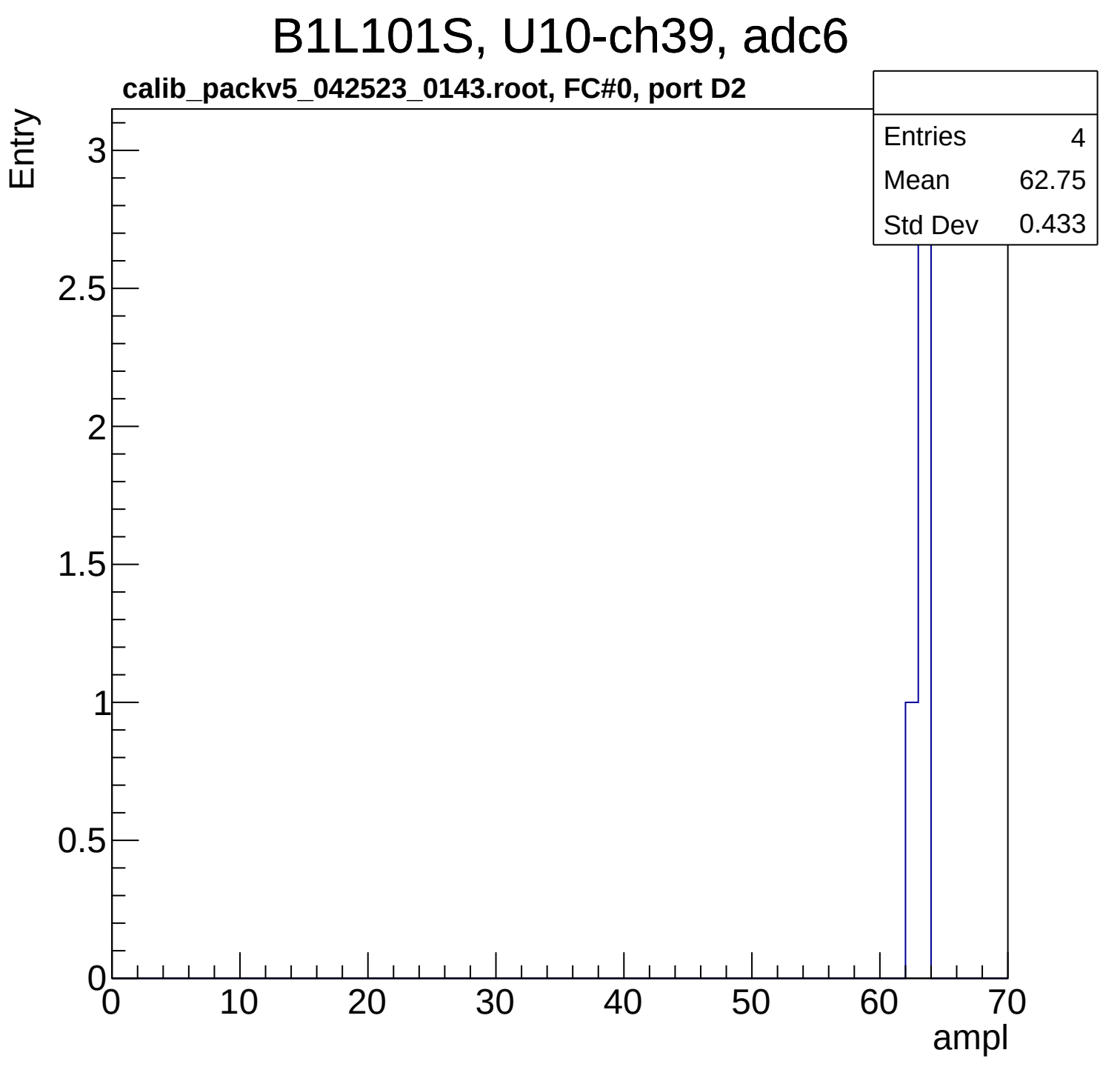

B1L101S, U10-ch39, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 50.57
Std Dev 3.225
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch39, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 56.25
Std Dev 3.049
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch39, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 40
Mean 58.9
Std Dev 9.643
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch39, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 62.75
Std Dev 0.433
Entry
ampl
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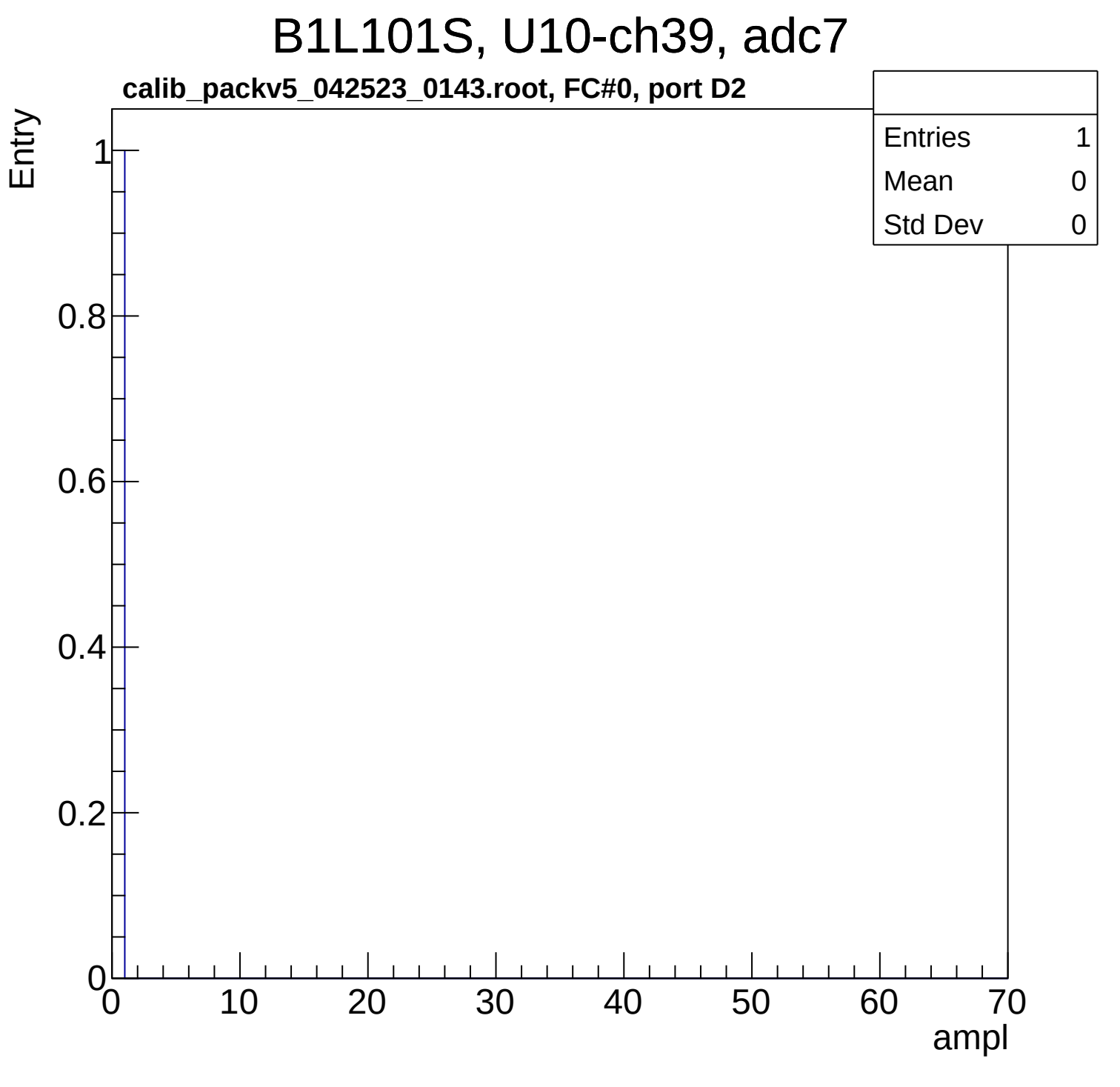
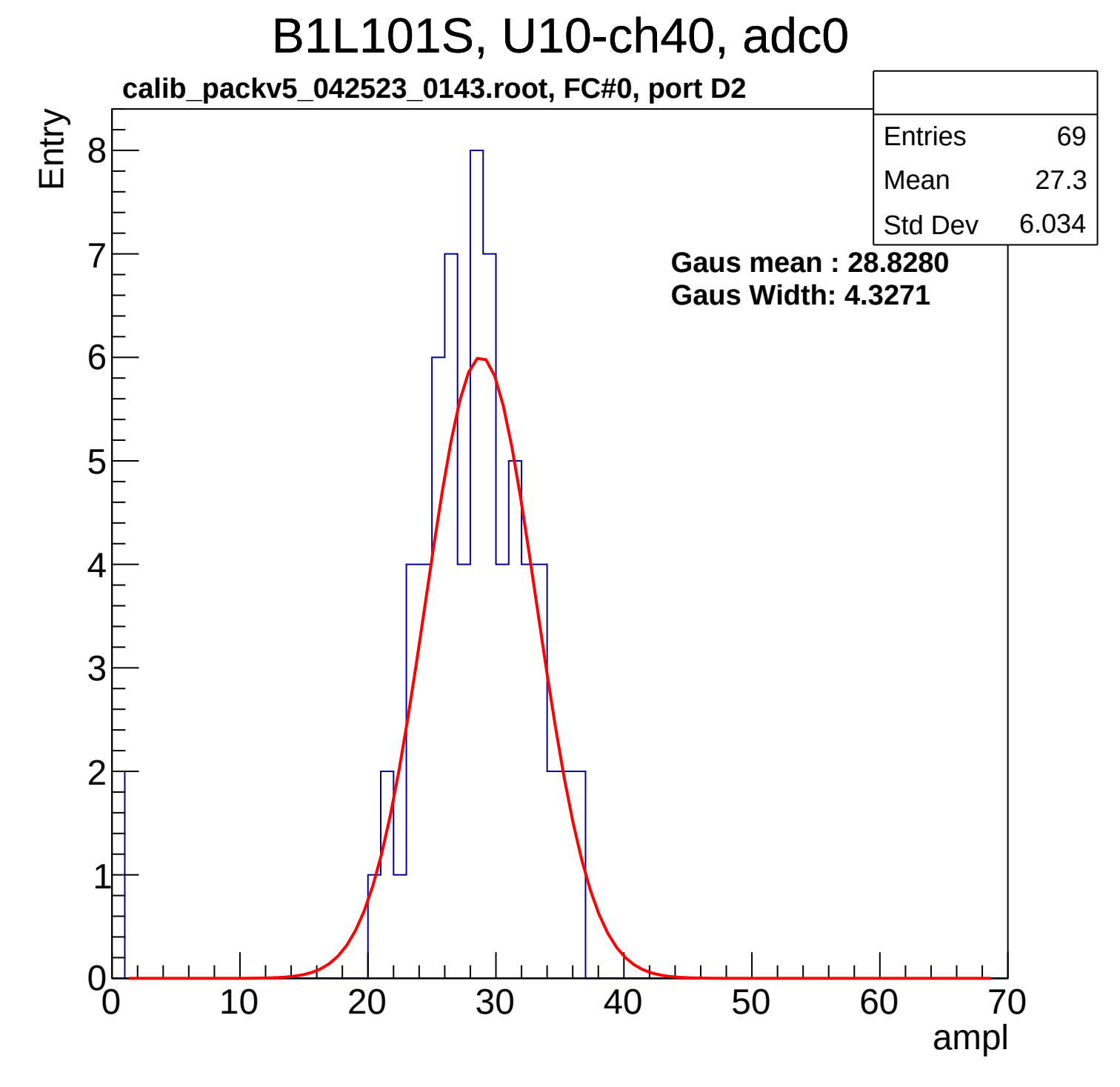
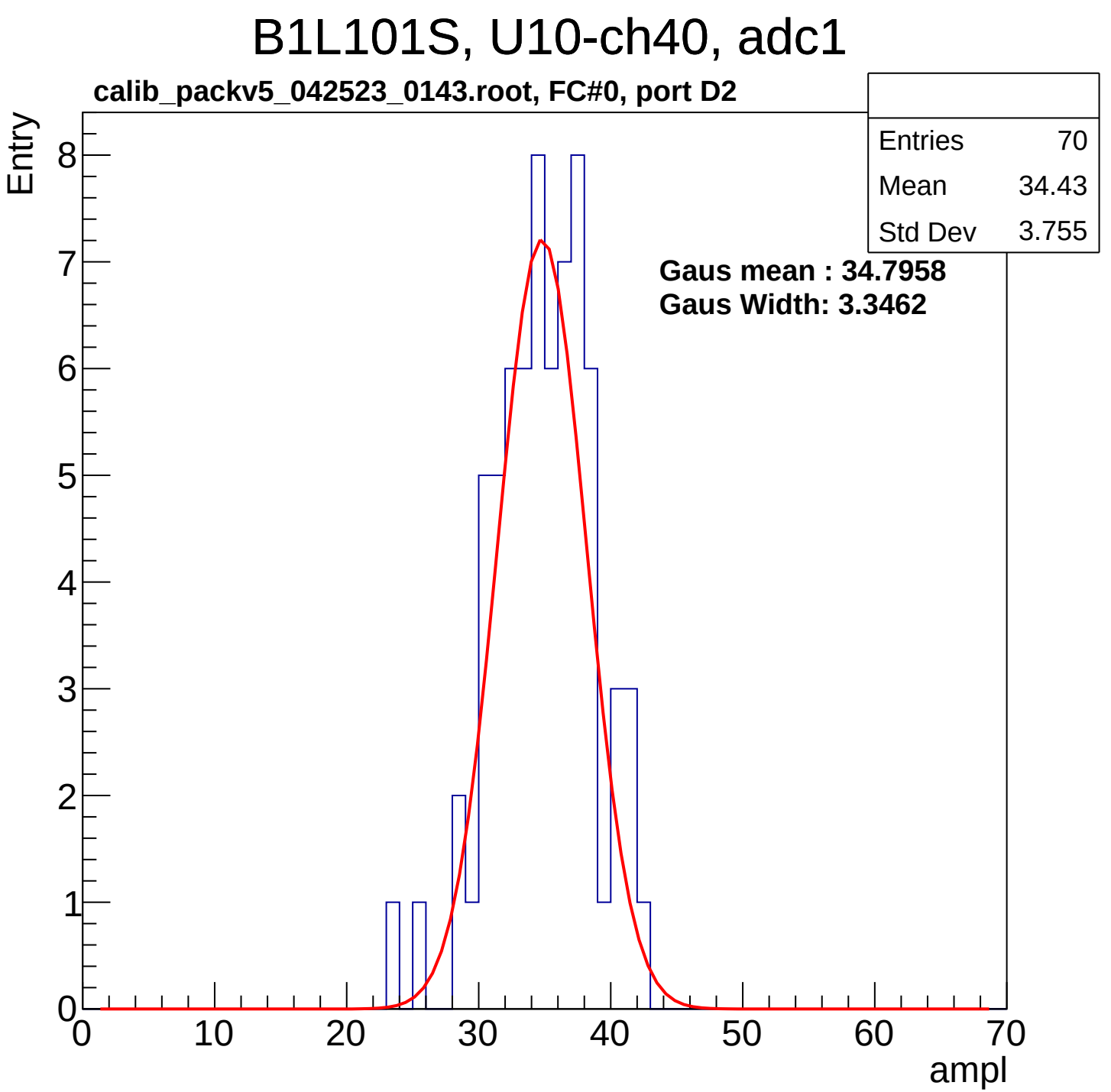
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U10-ch39, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch40, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 27.3
Std Dev 6.034
Gaus mean : 28.8280
Gaus Width: 4.3271
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch40, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 34.43
Std Dev 3.755
Gaus mean : 34.7958
Gaus Width: 3.3462
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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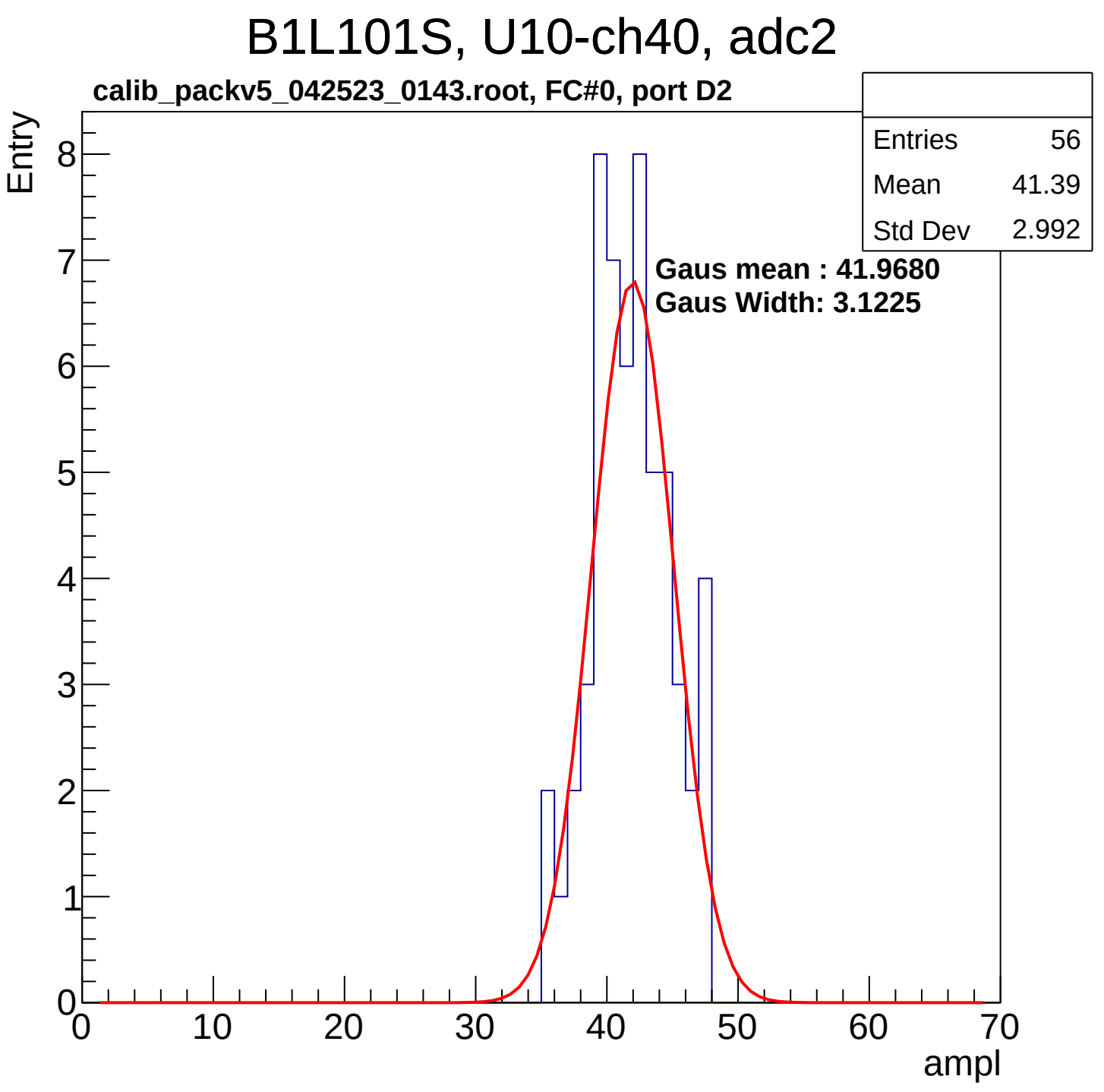
B1L101S, U10-ch40, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 41.39
Std Dev 2.992
Gaus mean : 41.9680
Gaus Width: 3.1225
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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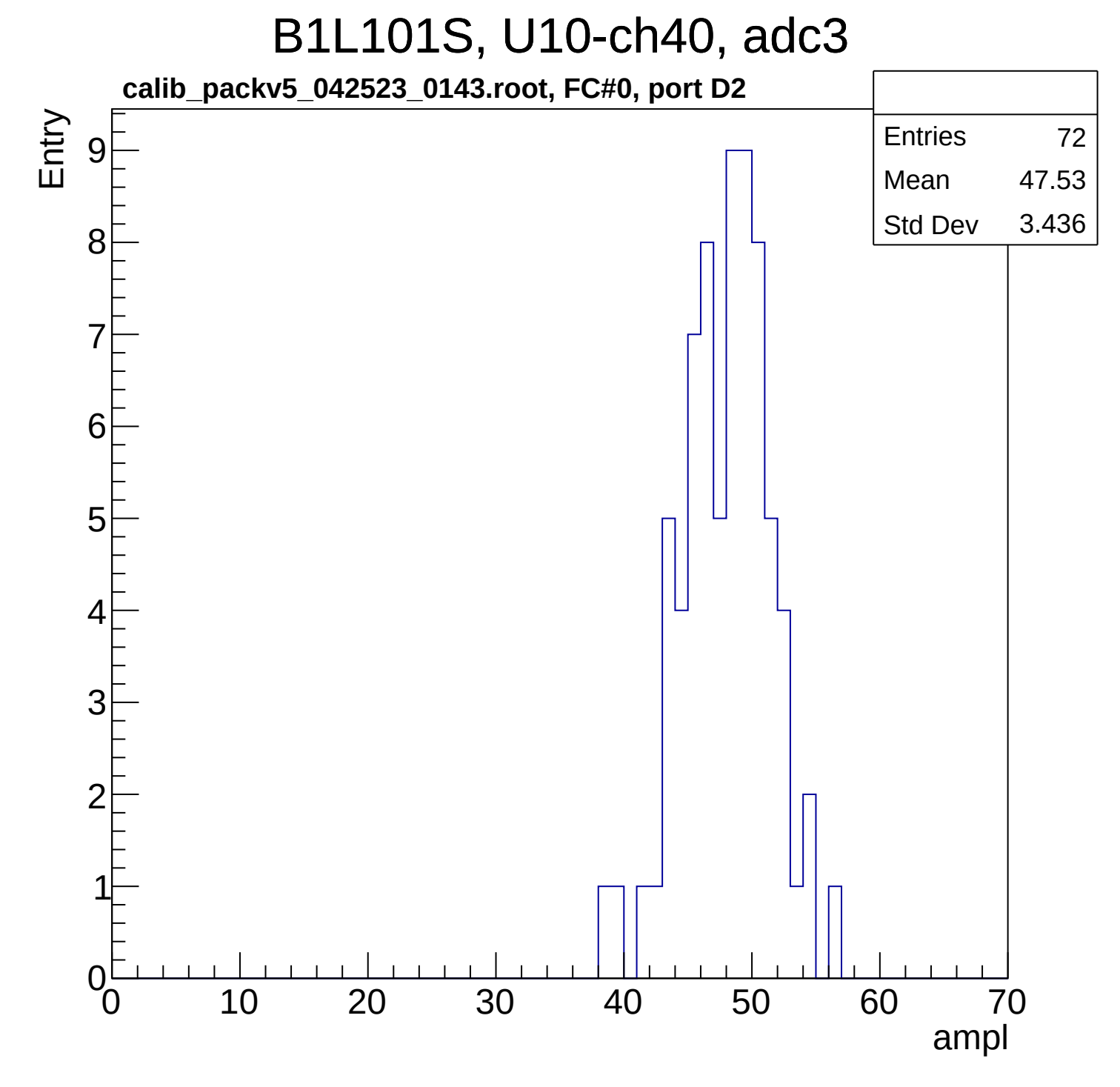
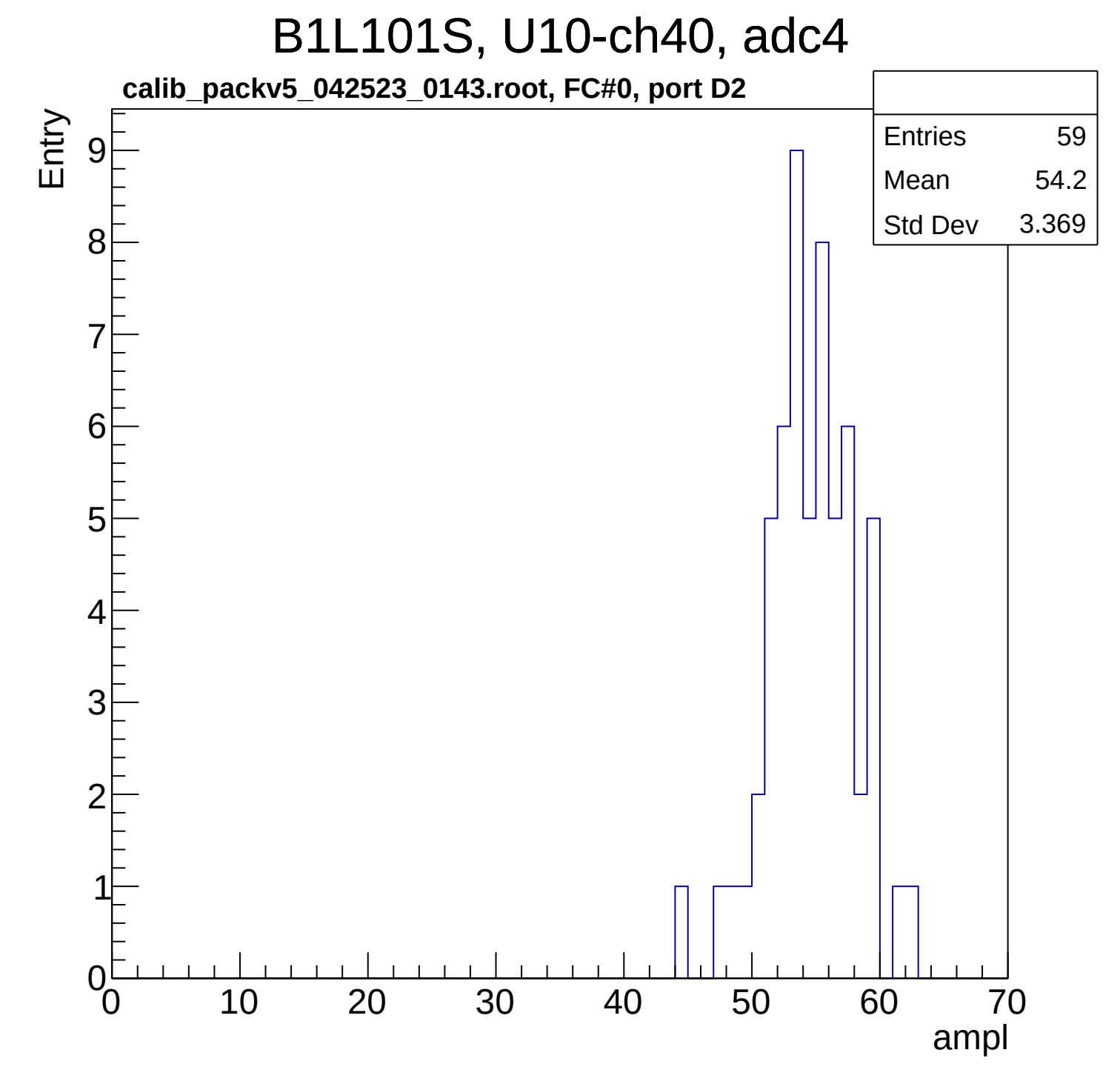
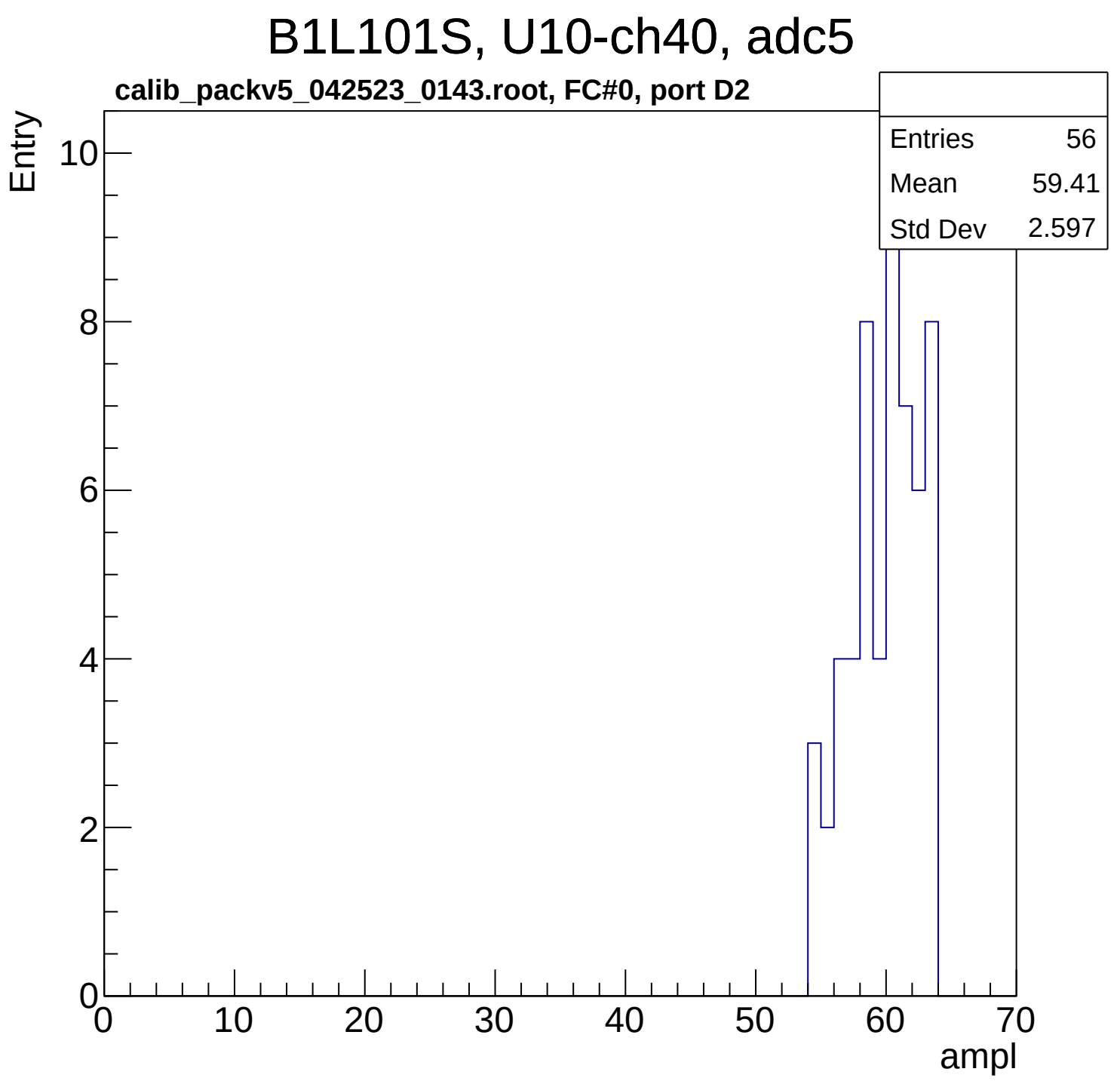
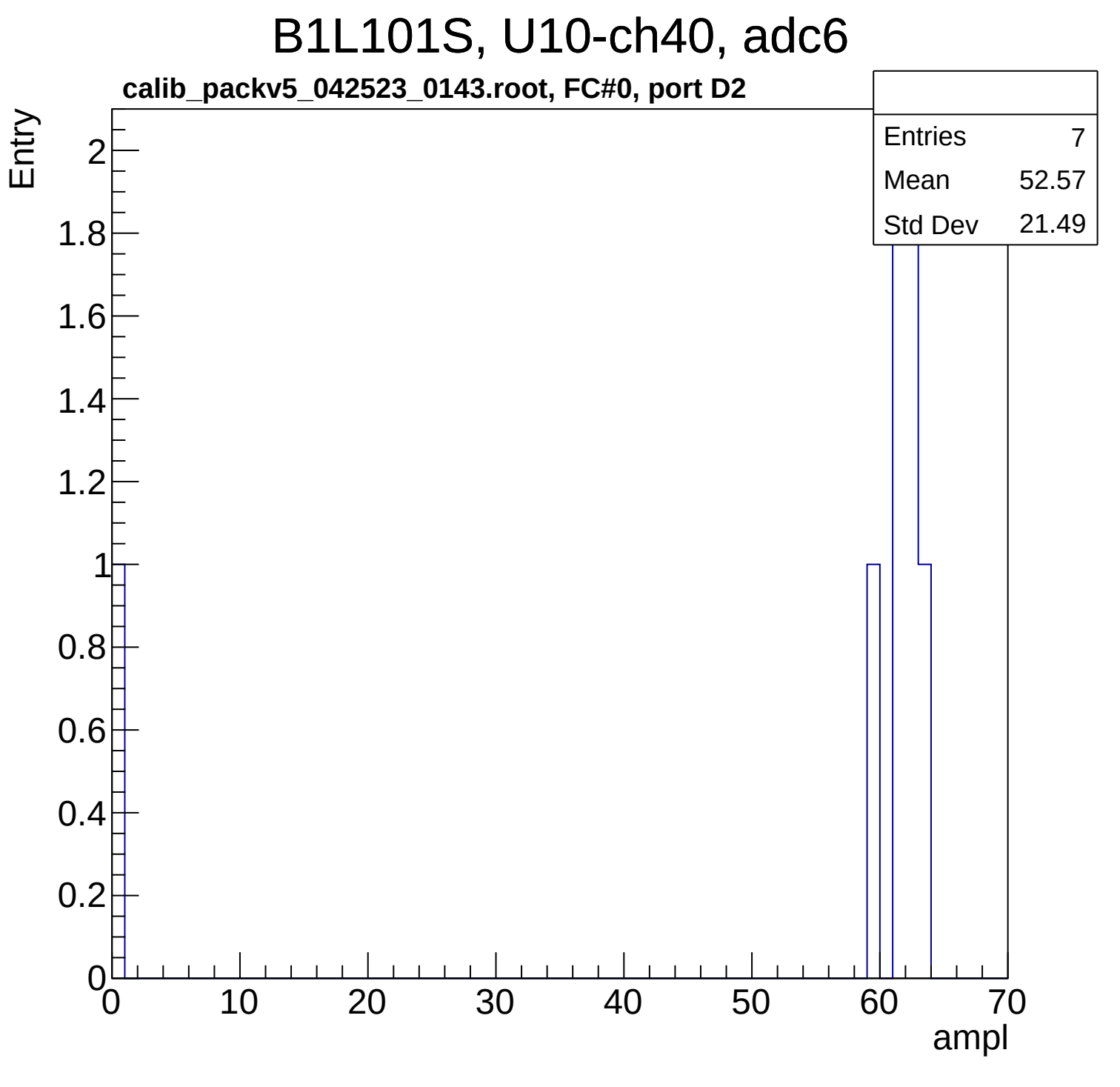
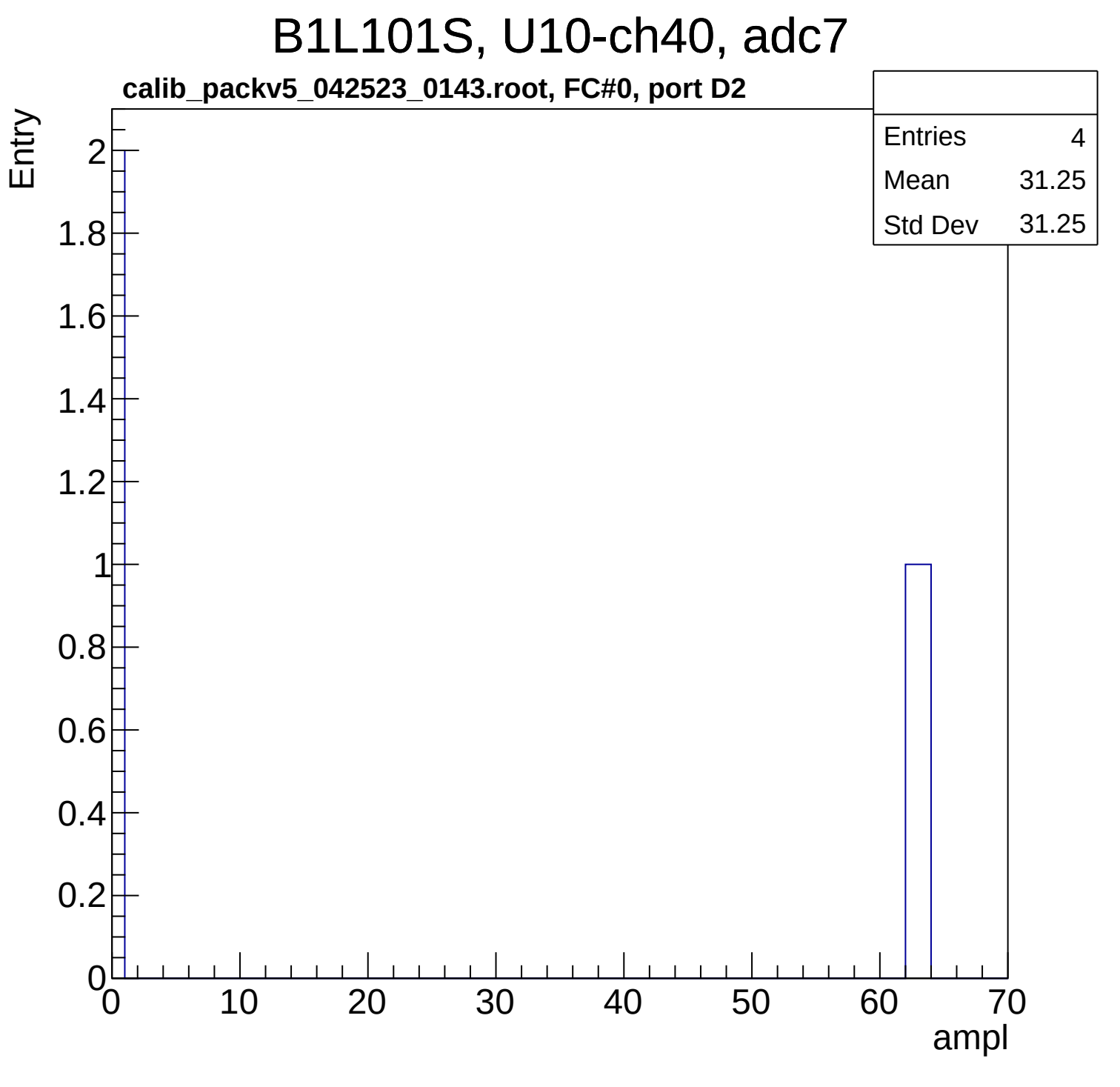

B1L101S, U10-ch40, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 47.53
Std Dev 3.436
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch40, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 54.2
Std Dev 3.369
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch40, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 59.41
Std Dev 2.597
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch40, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 52.57
Std Dev 21.49
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U10-ch40, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 31.25
Std Dev 31.25
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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20
30
40
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60
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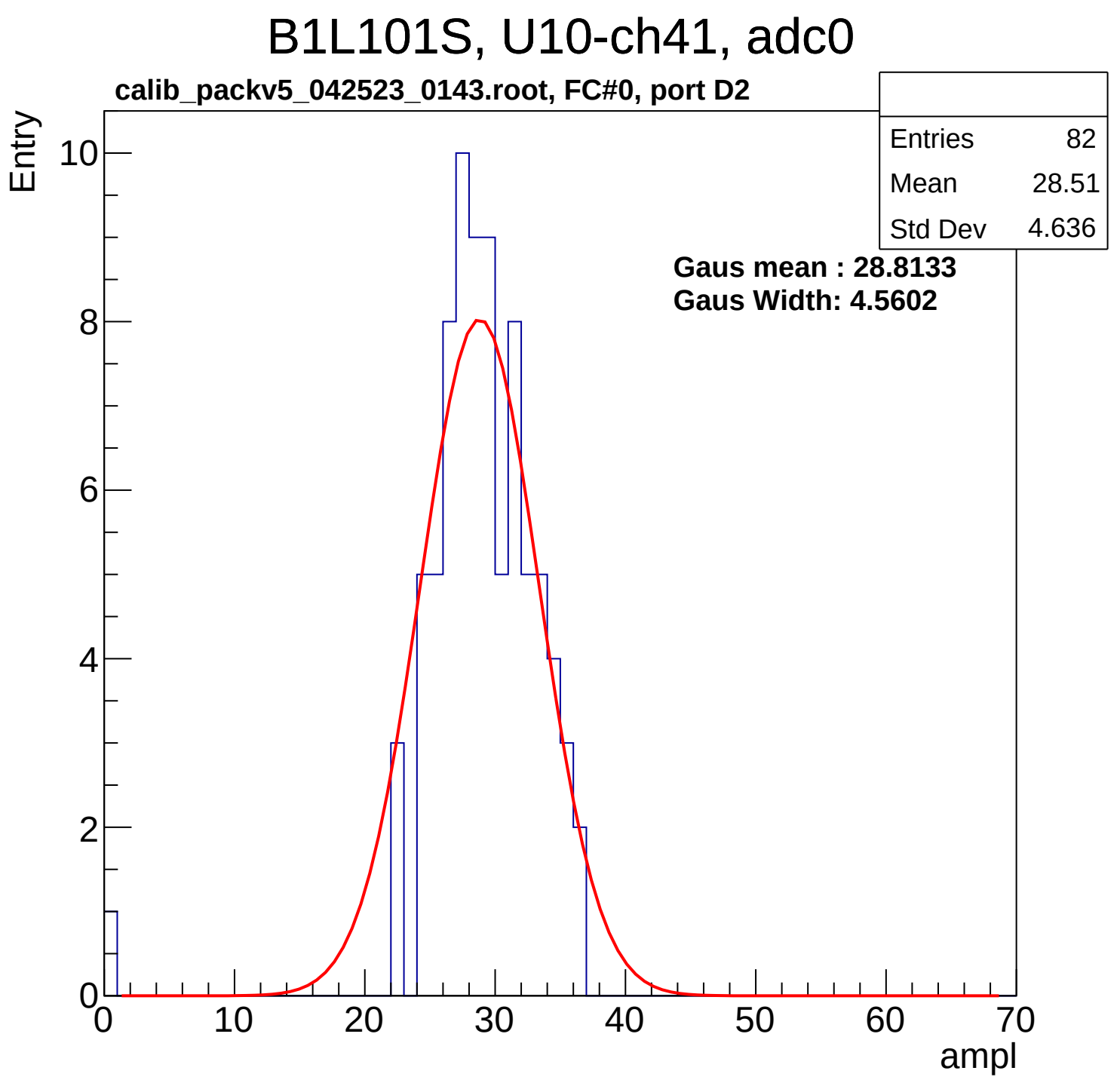
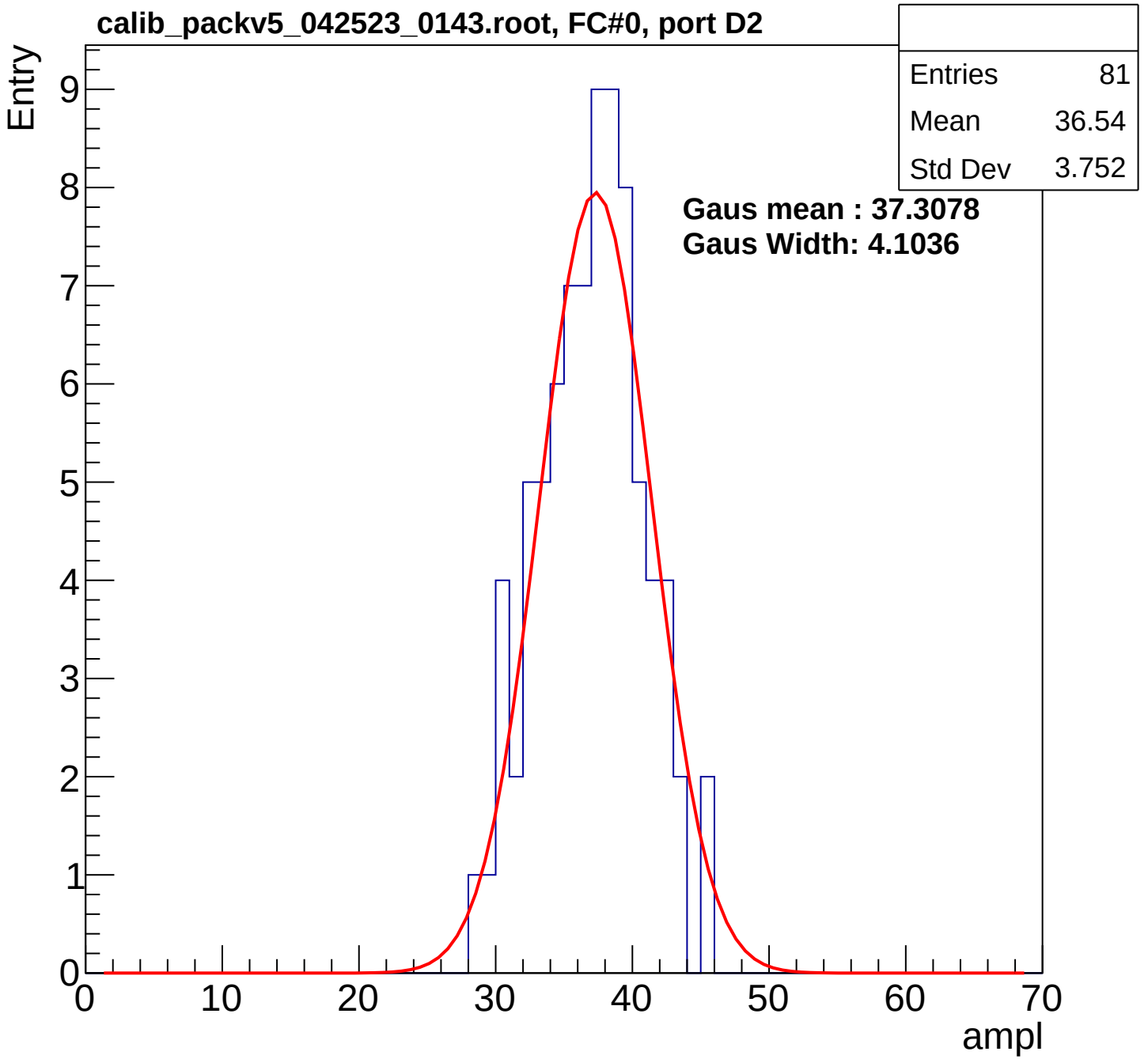
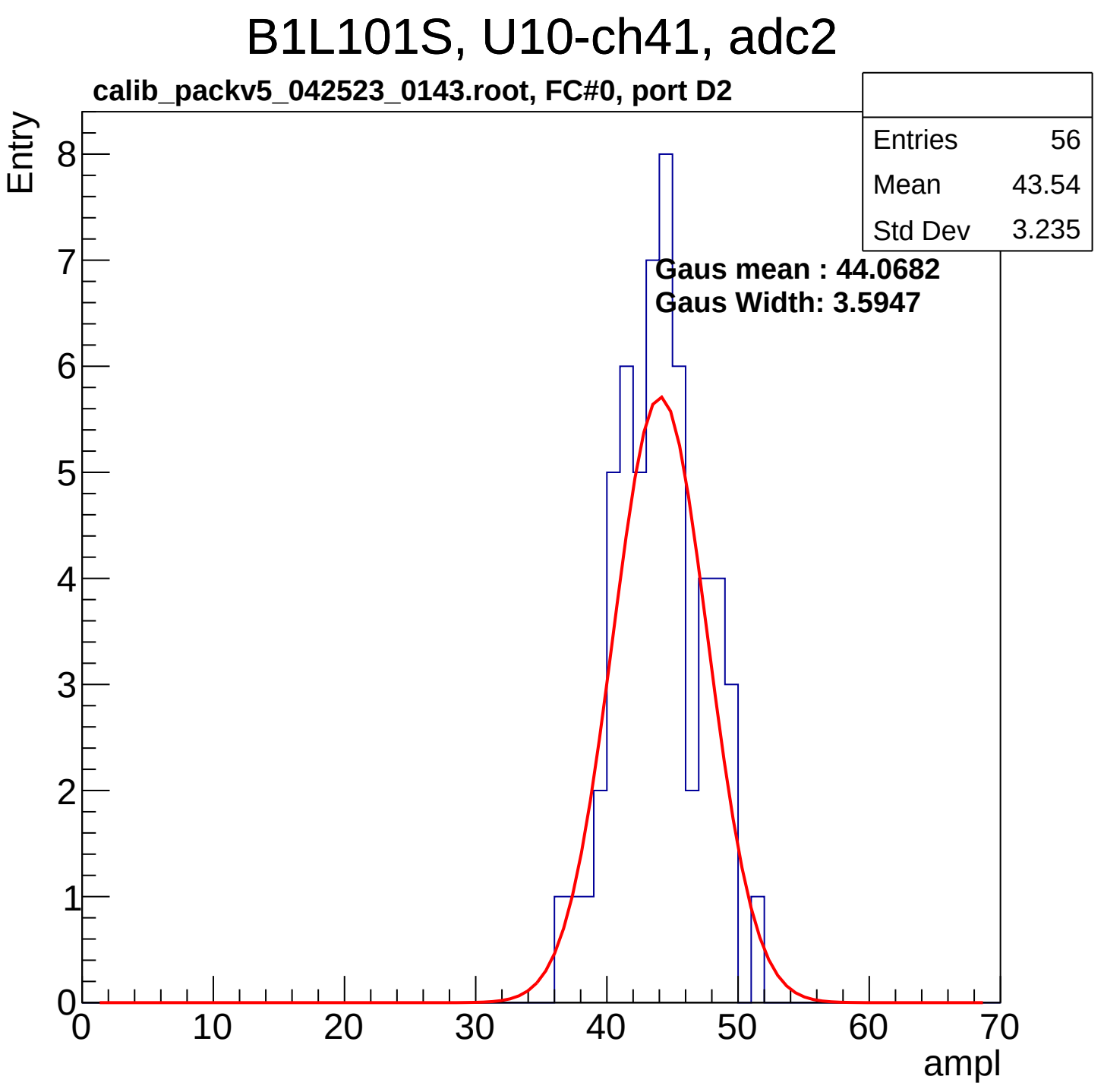

B1L101S, U10-ch41, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 82
Mean 28.51
Std Dev 4.636
Gaus mean : 28.8133
Gaus Width: 4.5602
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch41, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 81
Mean 36.54
Std Dev 3.752
Gaus mean : 37.3078
Gaus Width: 4.1036
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch41, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 43.54
Std Dev 3.235
Gaus mean : 44.0682
Gaus Width: 3.5947
Entry
ampl
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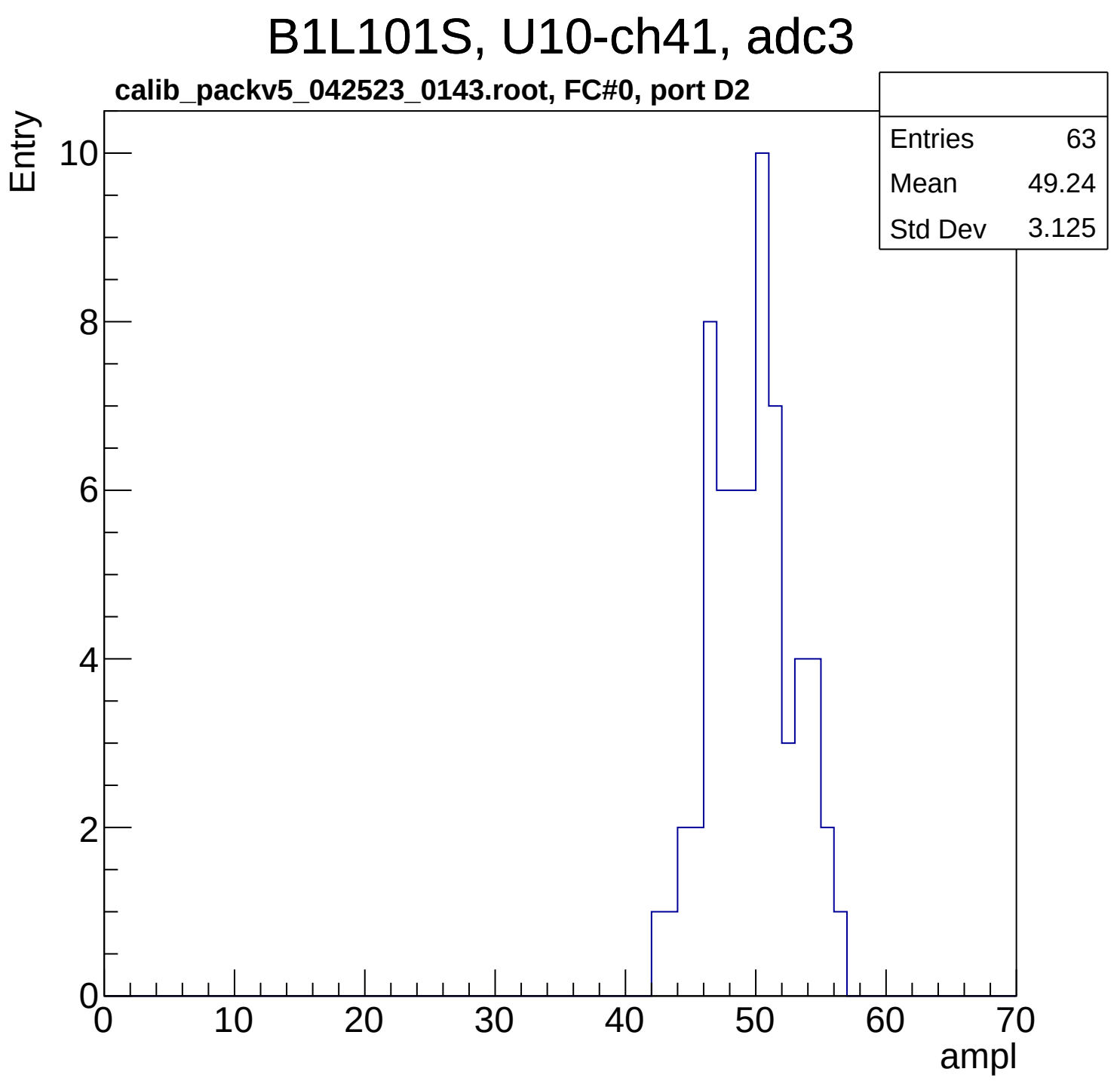
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch41, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 49.24
Std Dev 3.125
Entry
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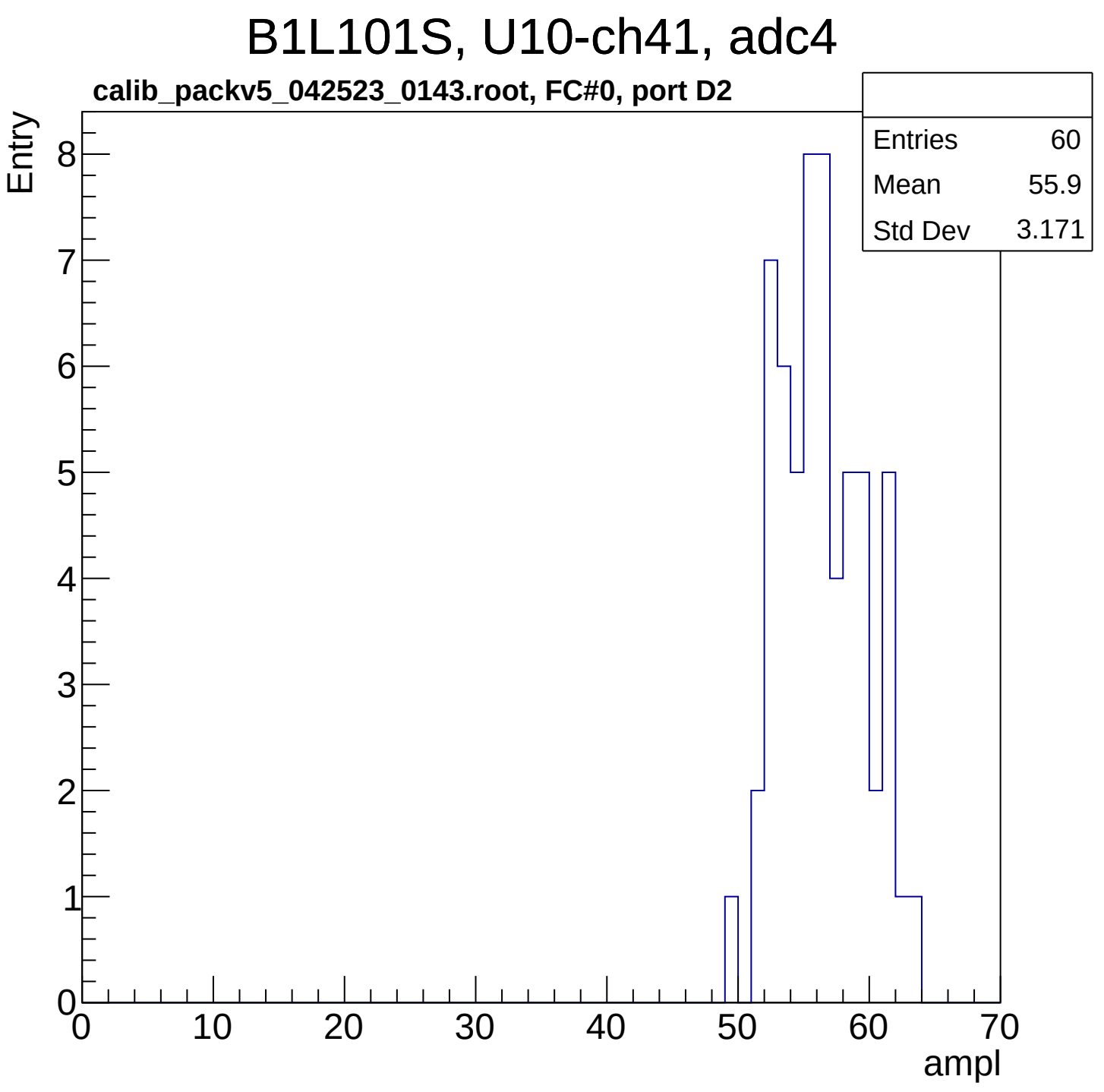
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch41, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 55.9
Std Dev 3.171
Entry
ampl
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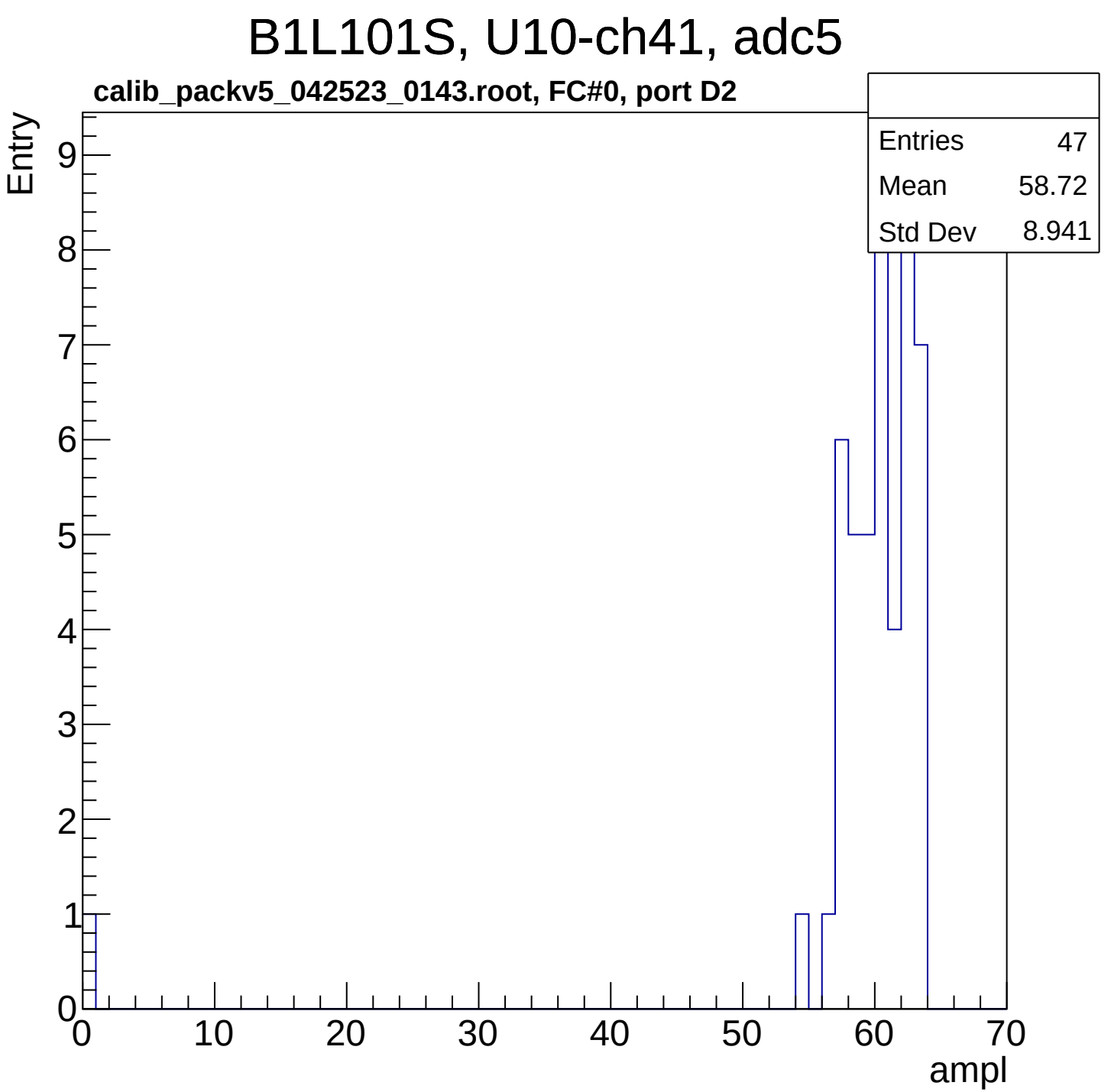
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch41, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 58.72
Std Dev 8.941
Entry
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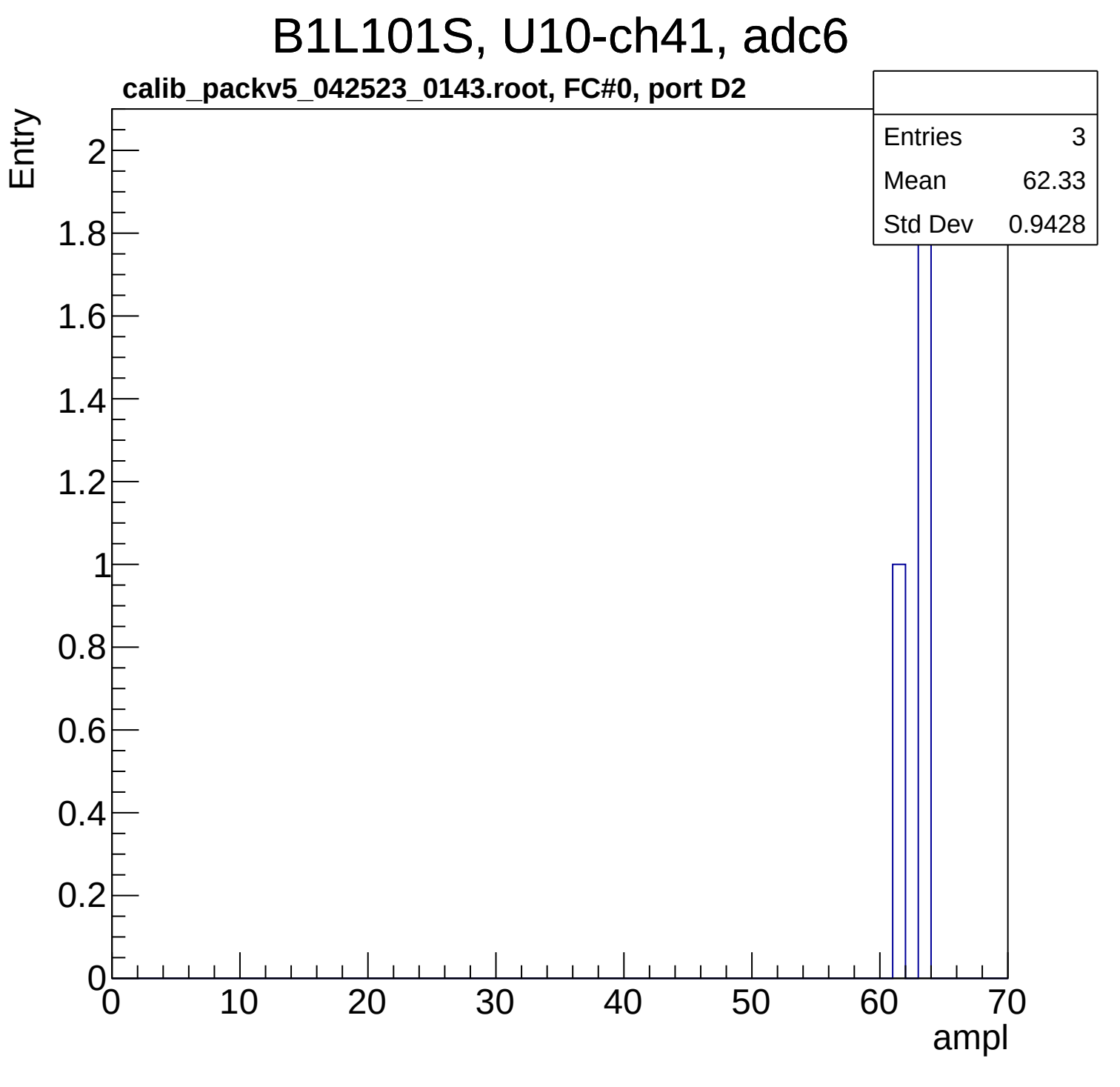
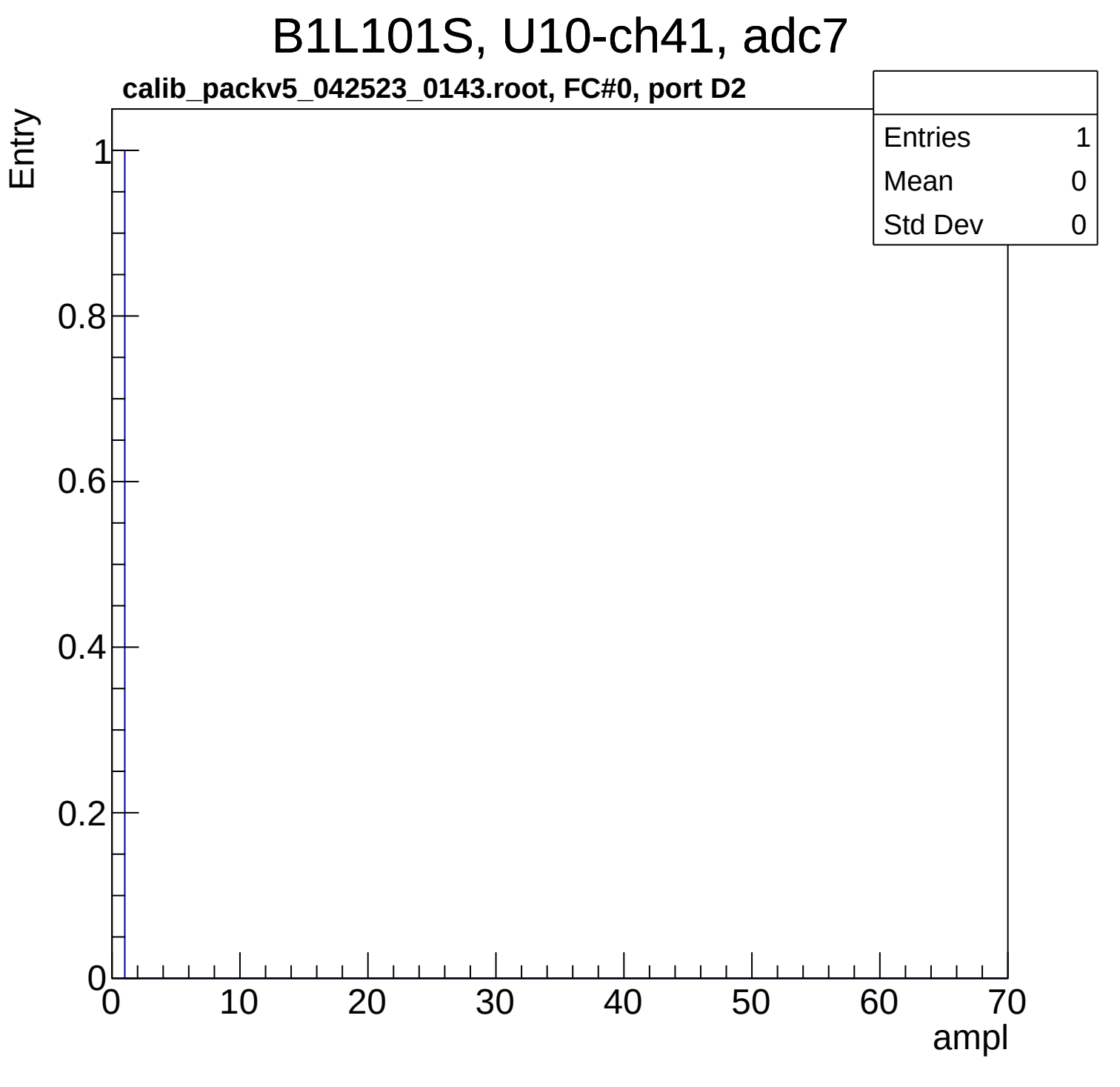
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch41, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 62.33
Std Dev 0.9428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U10-ch41, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
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0.6
0.4
0.2
0
0
10
20
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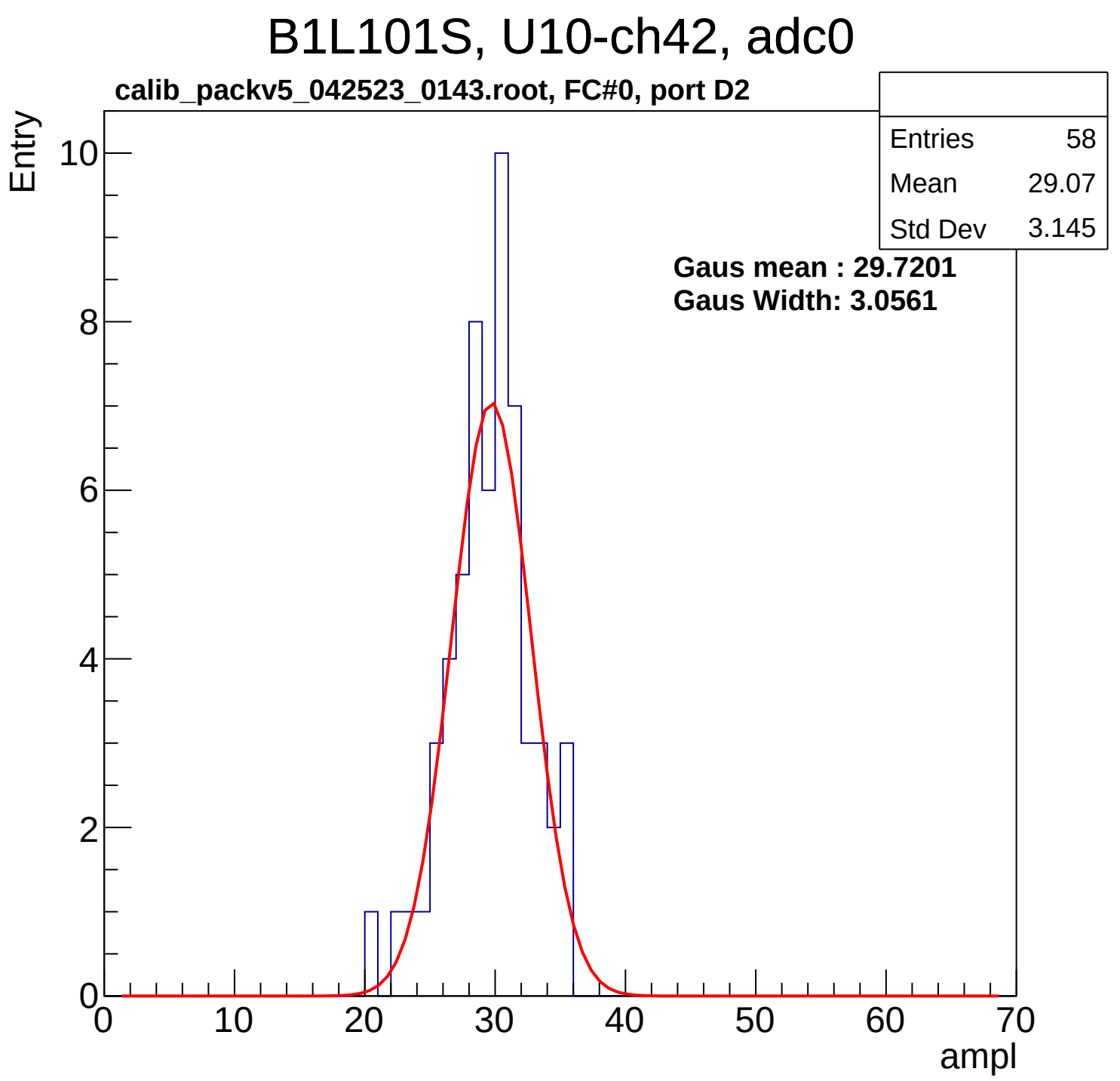
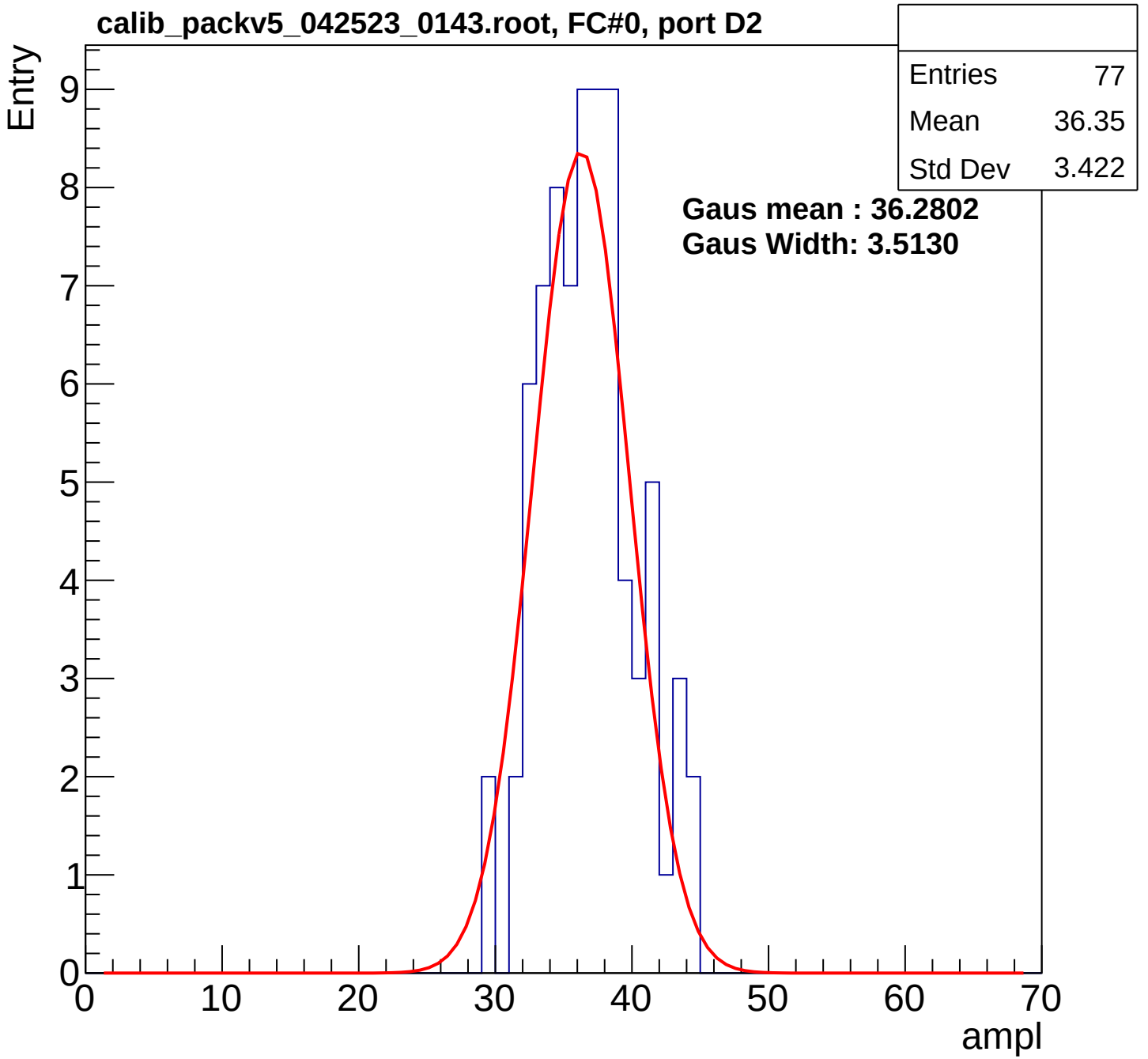
40
50
60
70
ampl


B1L101S, U10-ch42, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 29.07
Std Dev 3.145
Gaus mean : 29.7201
Gaus Width: 3.0561
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch42, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 36.35
Std Dev 3.422
Gaus mean : 36.2802
Gaus Width: 3.5130
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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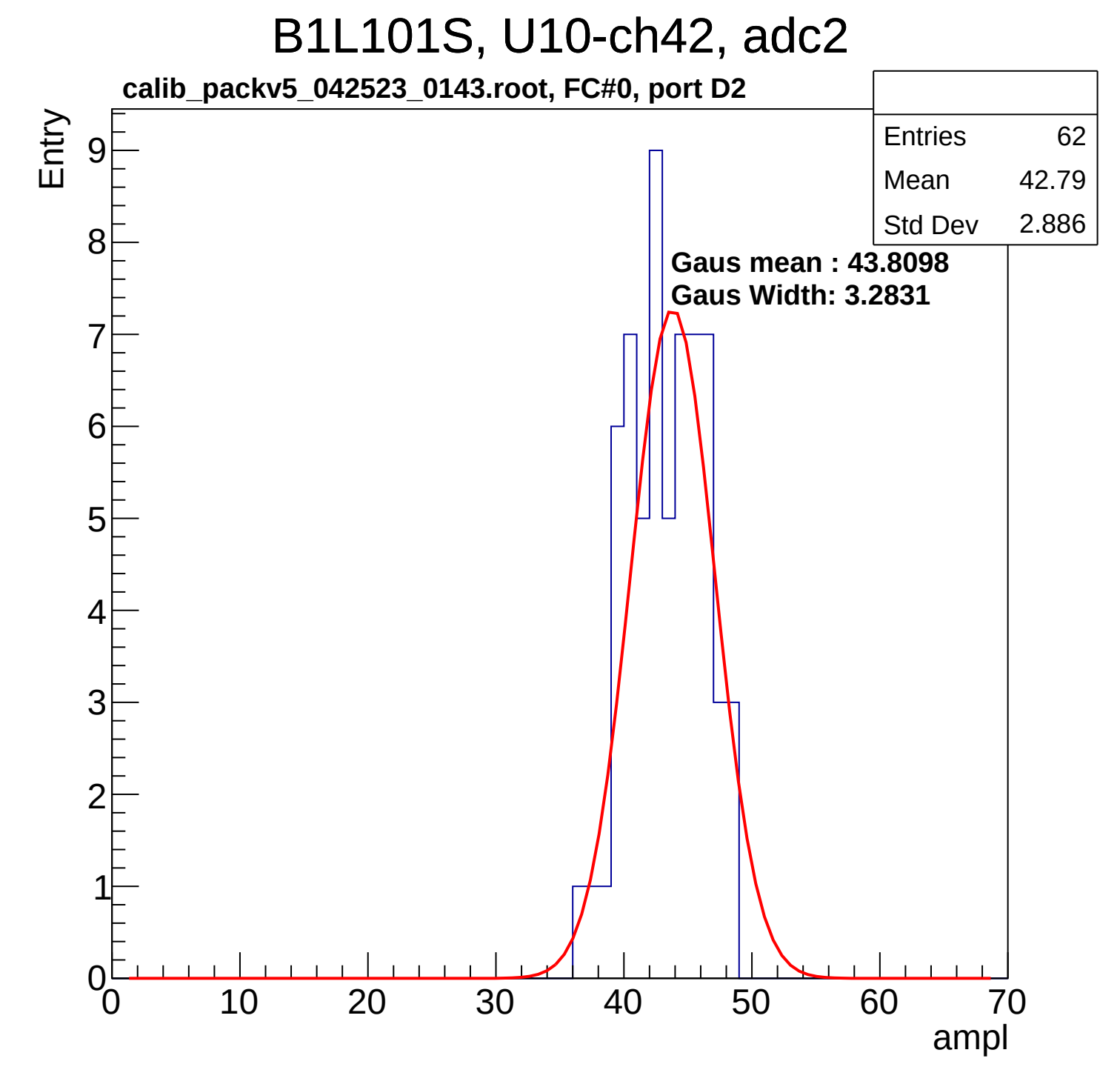
B1L101S, U10-ch42, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 42.79
Std Dev 2.886
Gaus mean : 43.8098
Gaus Width: 3.2831
Entry
ampl
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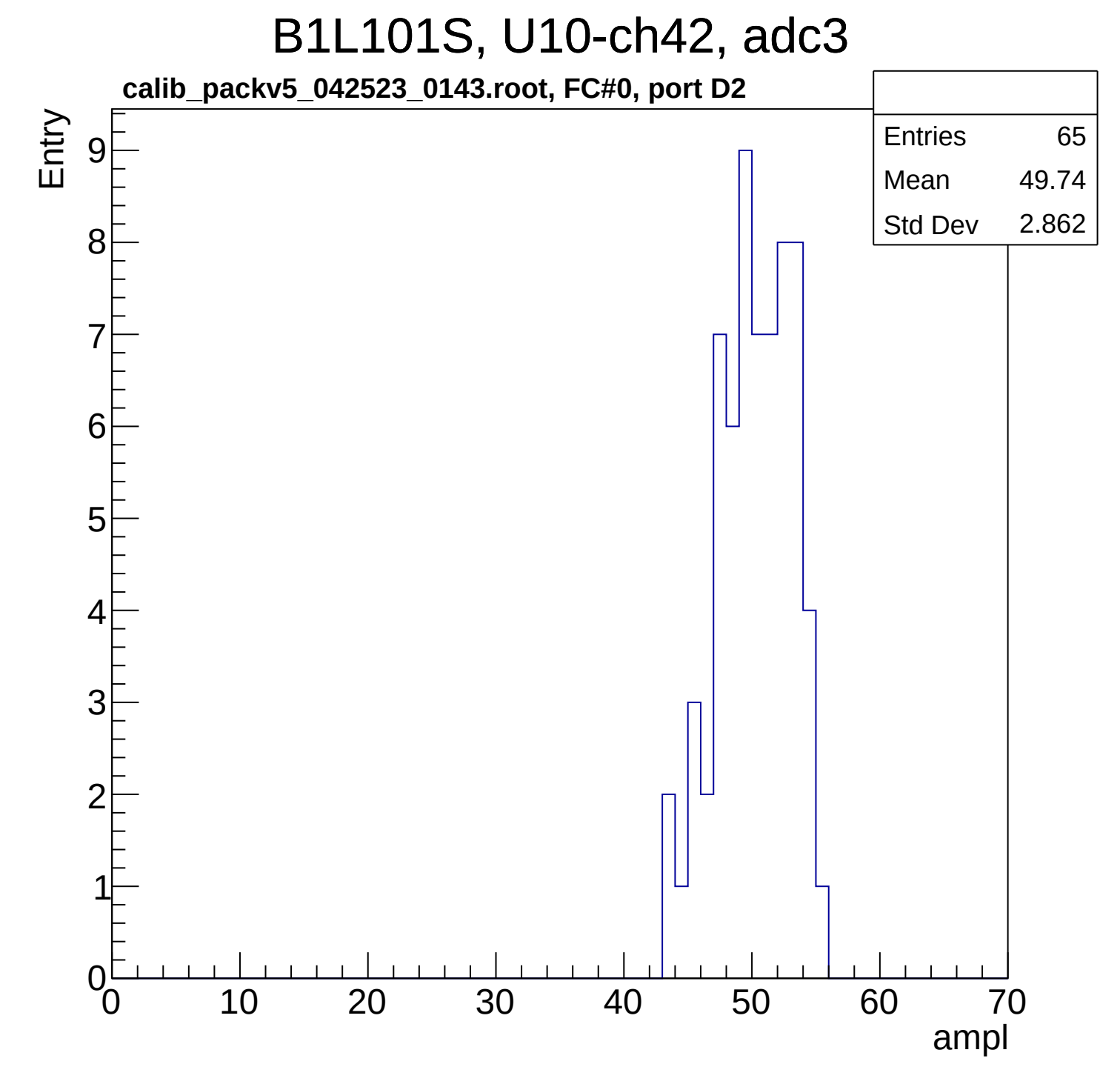
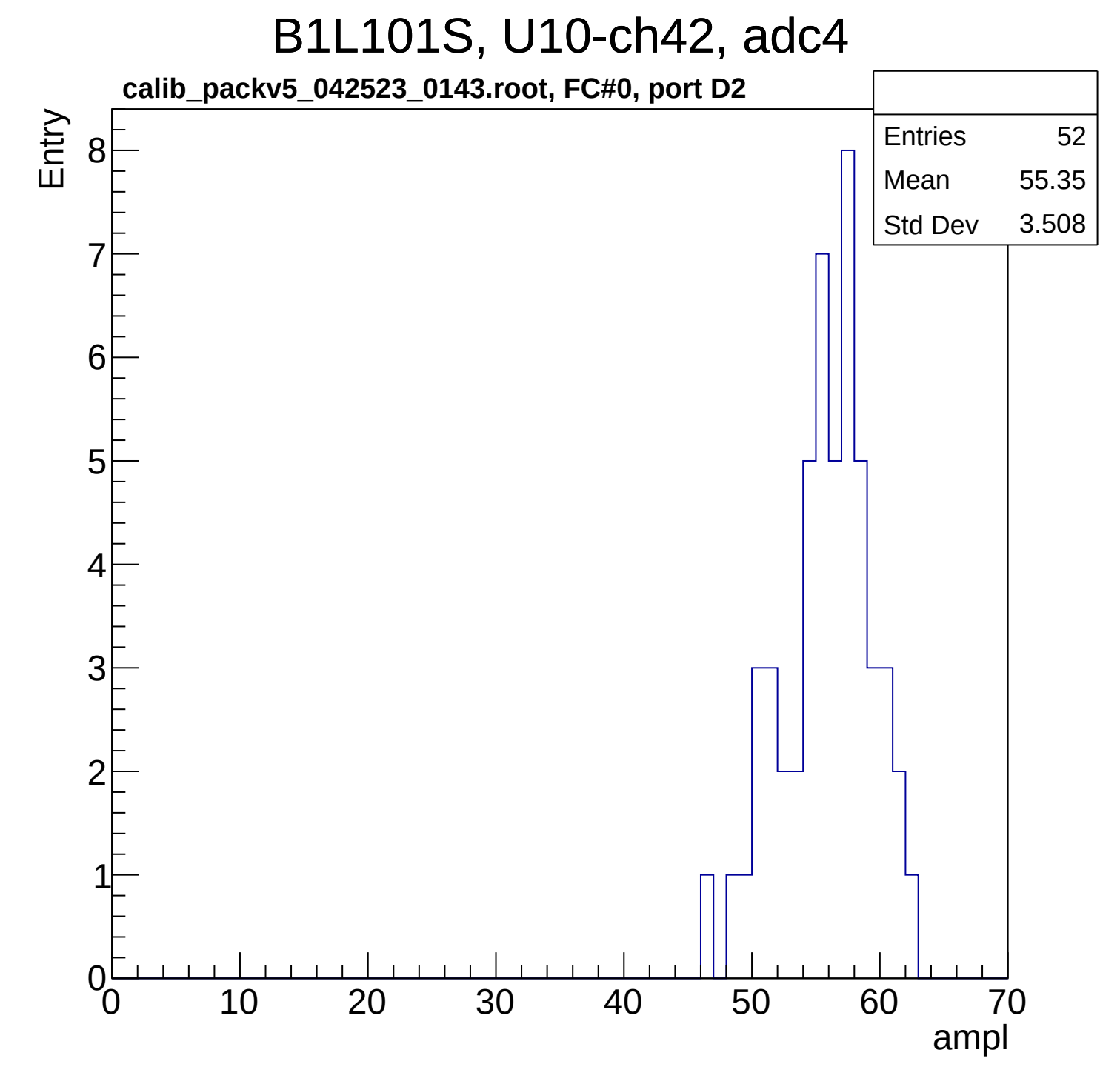
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch42, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 49.74
Std Dev 2.862
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch42, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 55.35
Std Dev 3.508
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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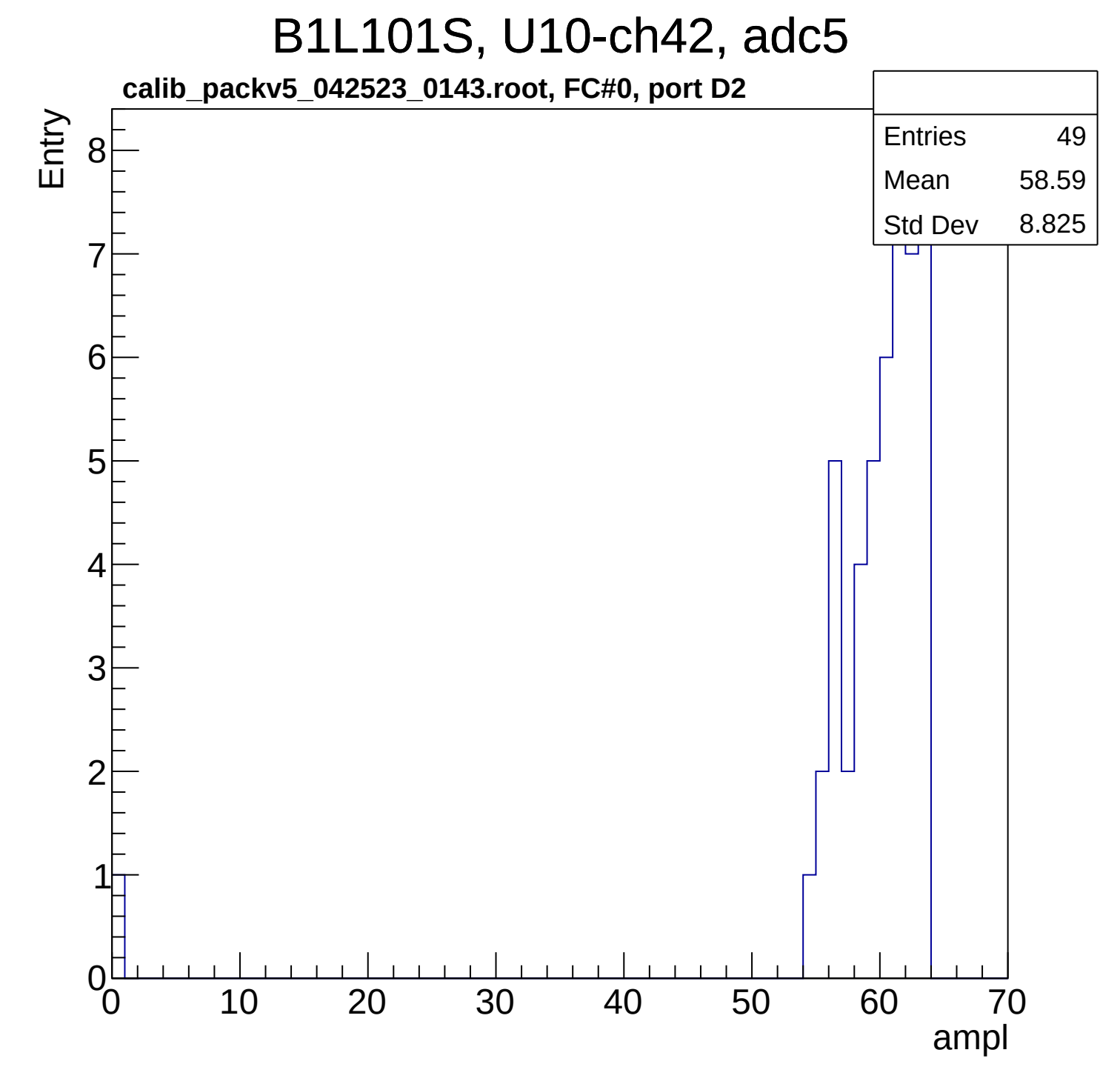
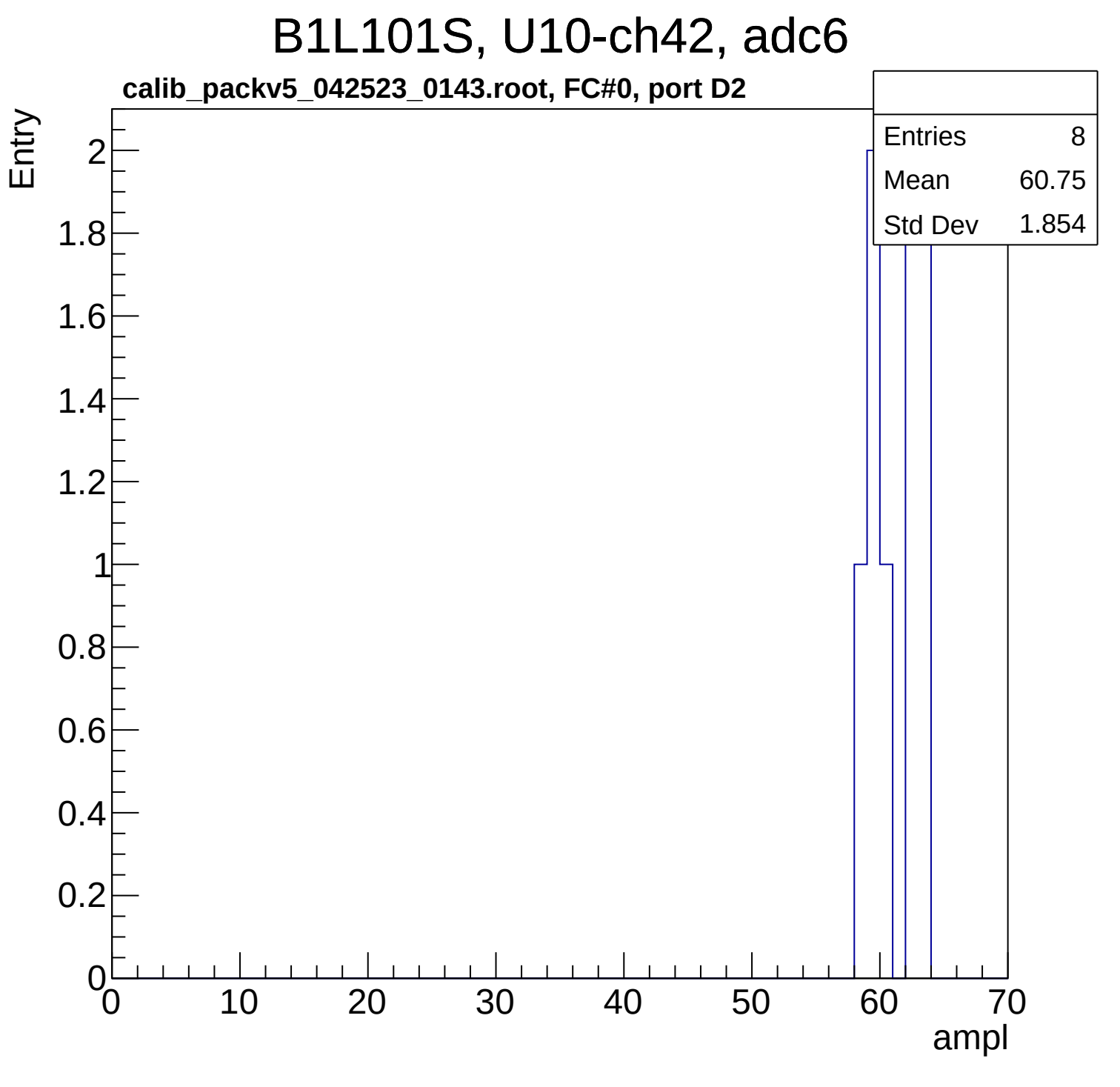
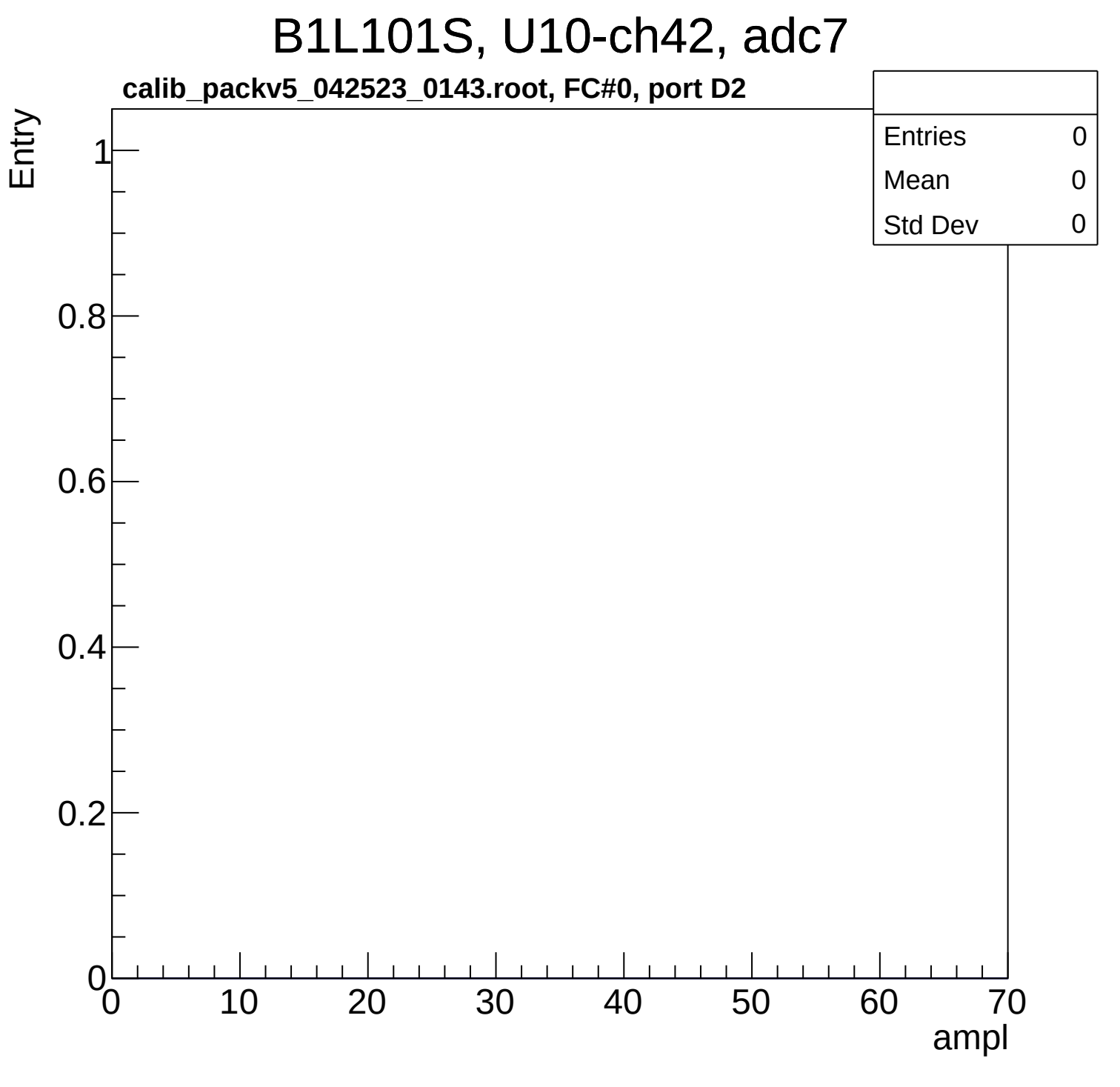
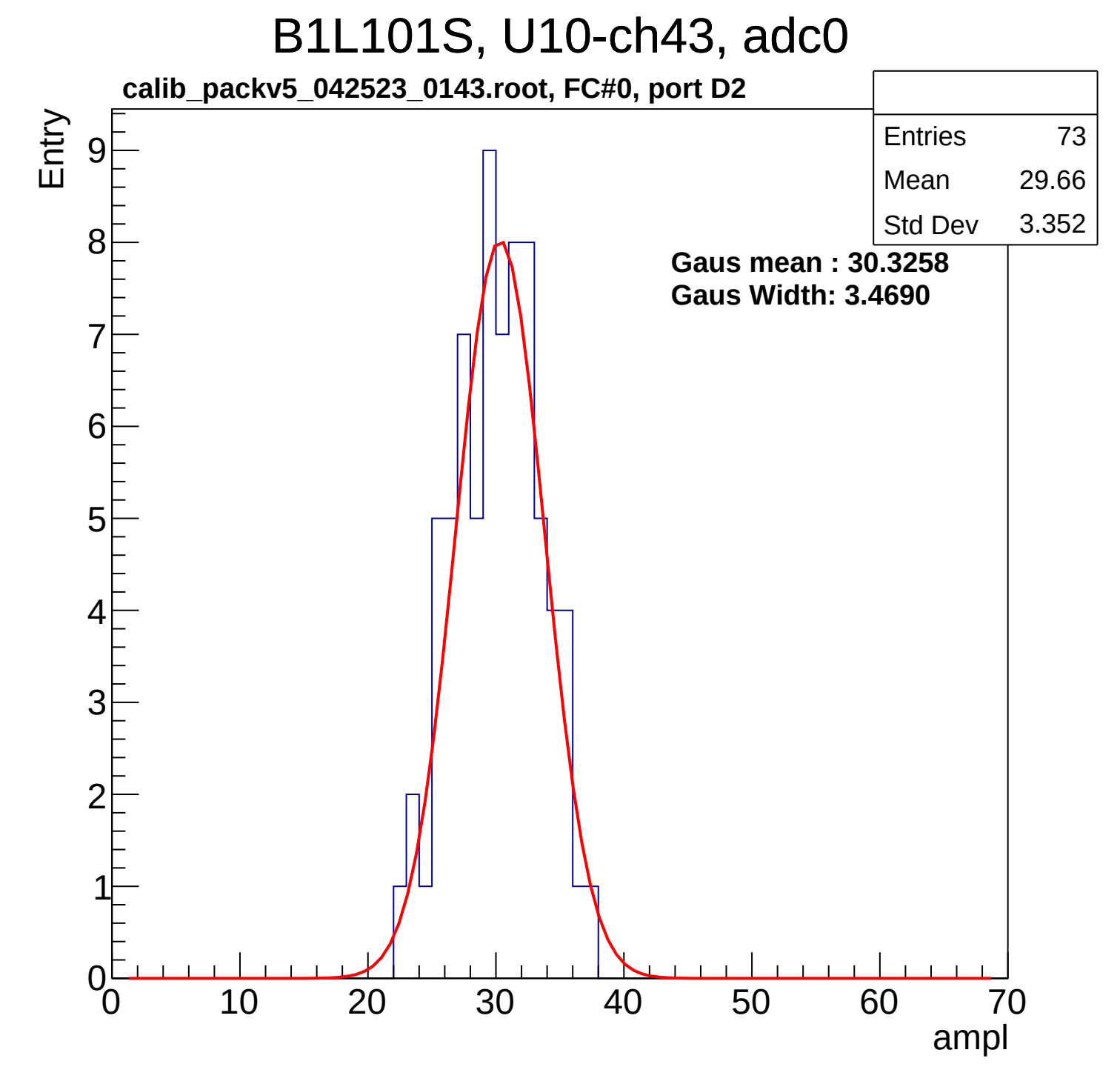

B1L101S, U10-ch42, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 58.59
Std Dev 8.825
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch42, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 60.75
Std Dev 1.854
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U10-ch42, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch43, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 29.66
Std Dev 3.352
Gaus mean : 30.3258
Gaus Width: 3.4690
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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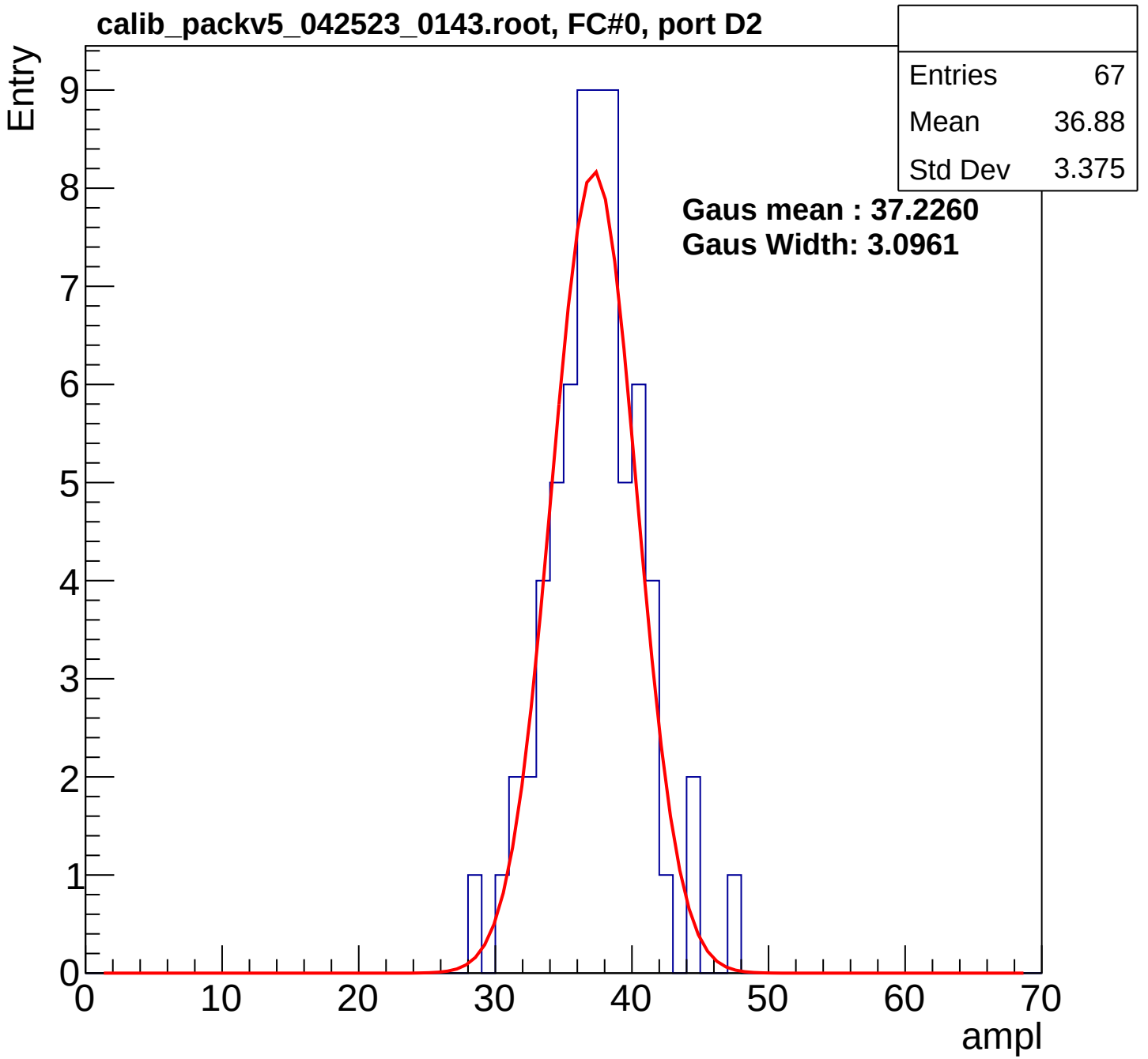
B1L101S, U10-ch43, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 36.88
Std Dev 3.375
Gaus mean : 37.2260
Gaus Width: 3.0961
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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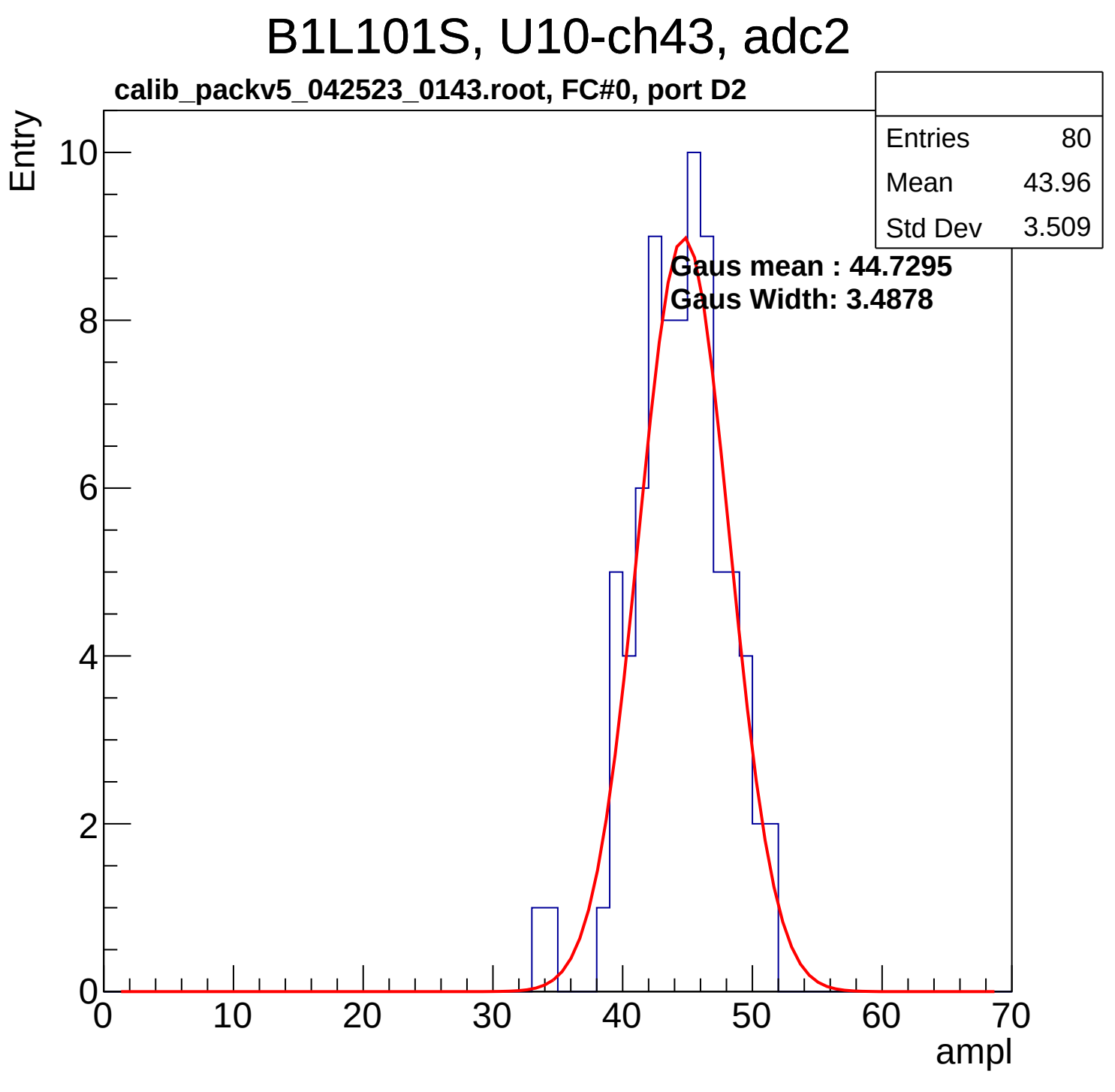
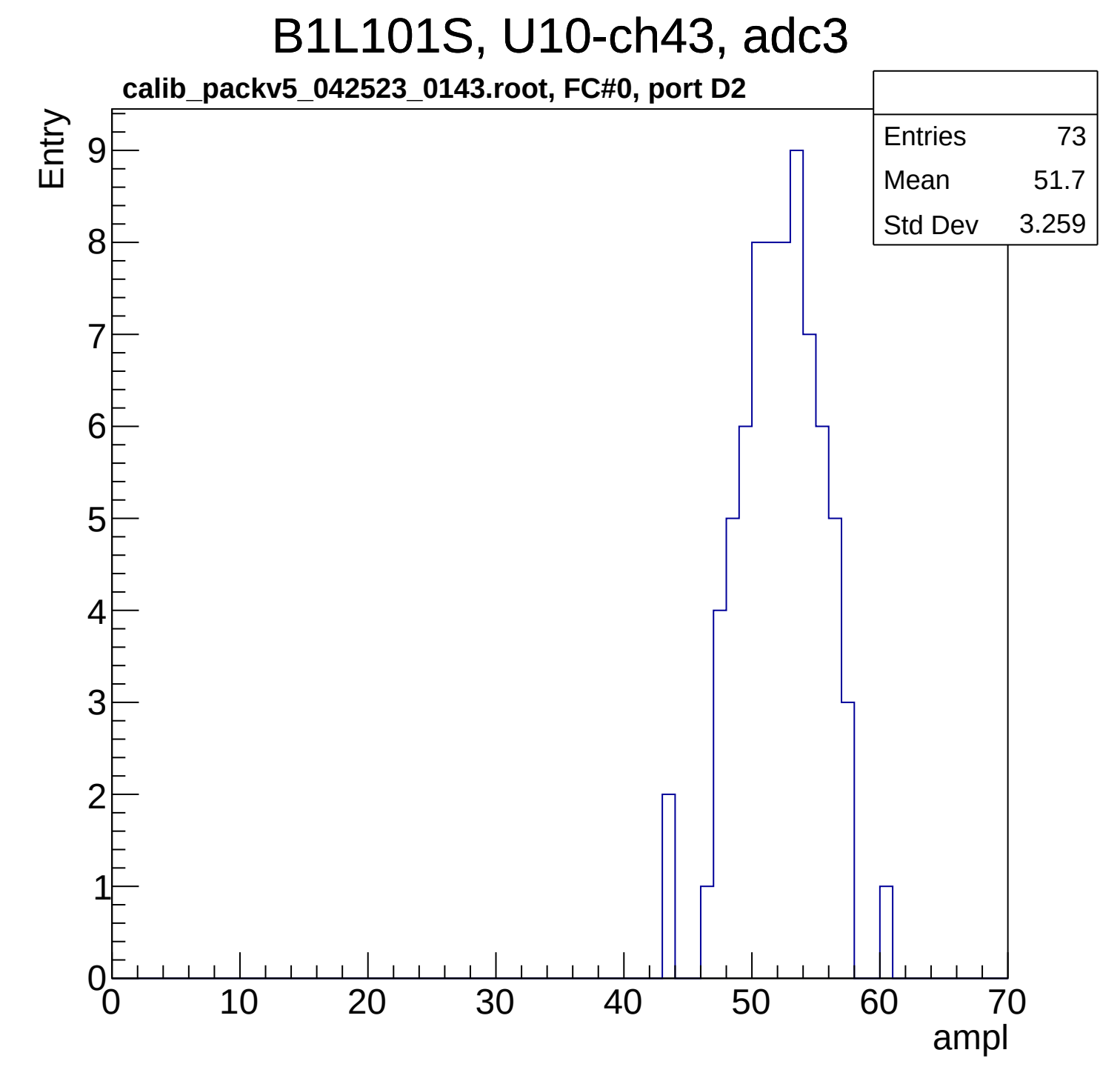
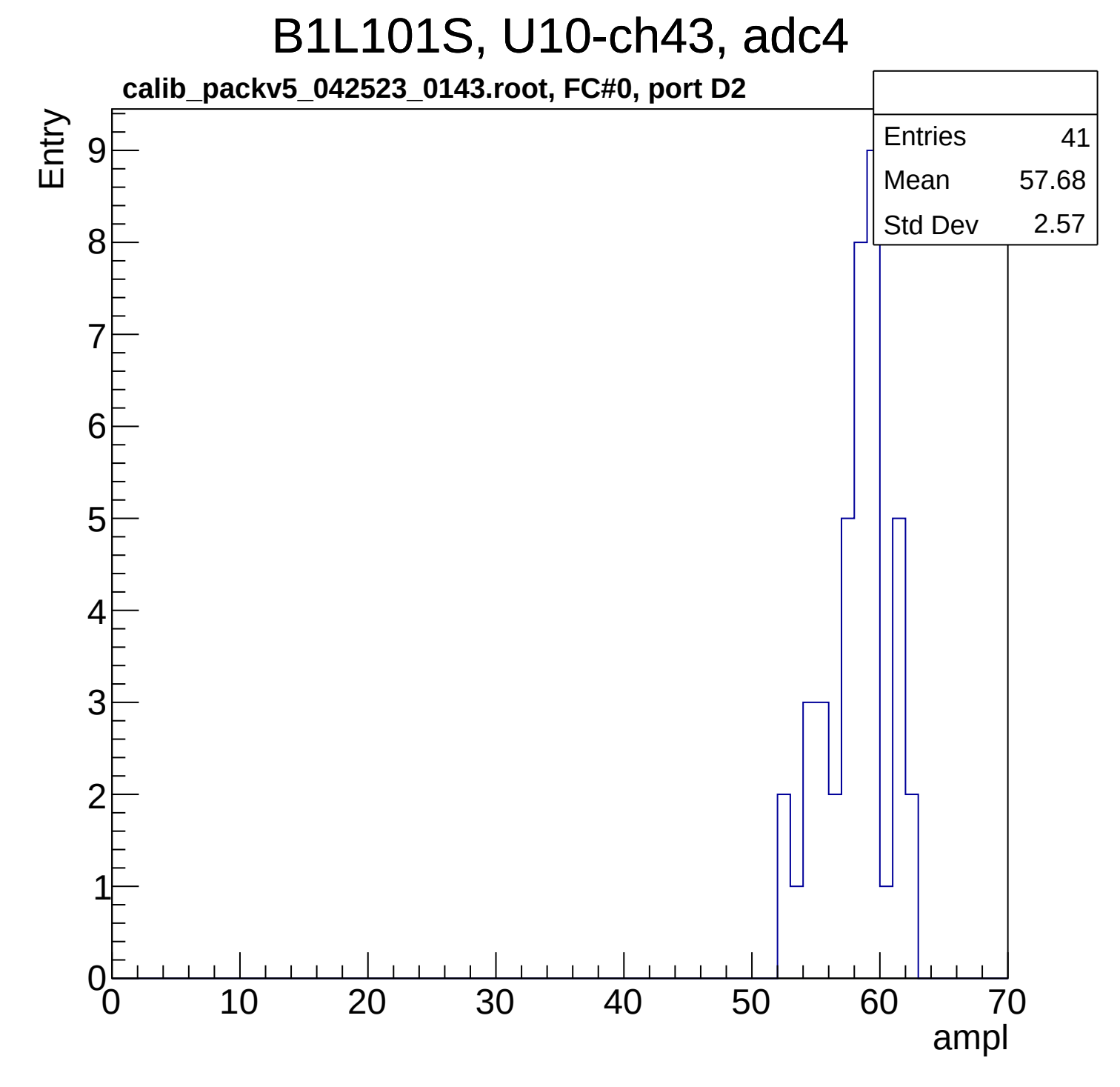

B1L101S, U10-ch43, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 80
Mean 43.96
Std Dev 3.509
Gaus mean : 44.7295
Gaus Width: 3.4878
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch43, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 51.7
Std Dev 3.259
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch43, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 41
Mean 57.68
Std Dev 2.57
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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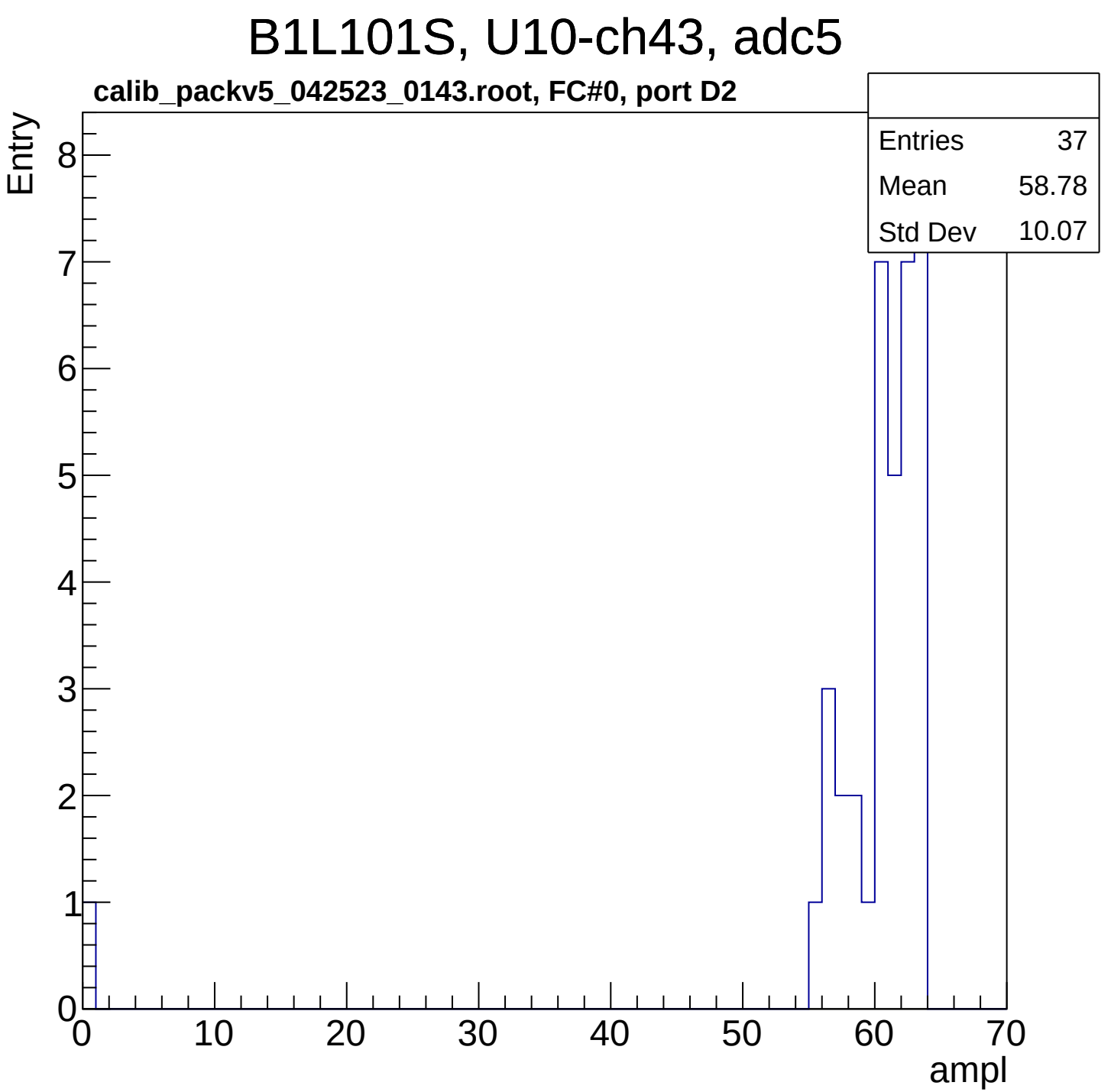
B1L101S, U10-ch43, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 37
Mean 58.78
Std Dev 10.07
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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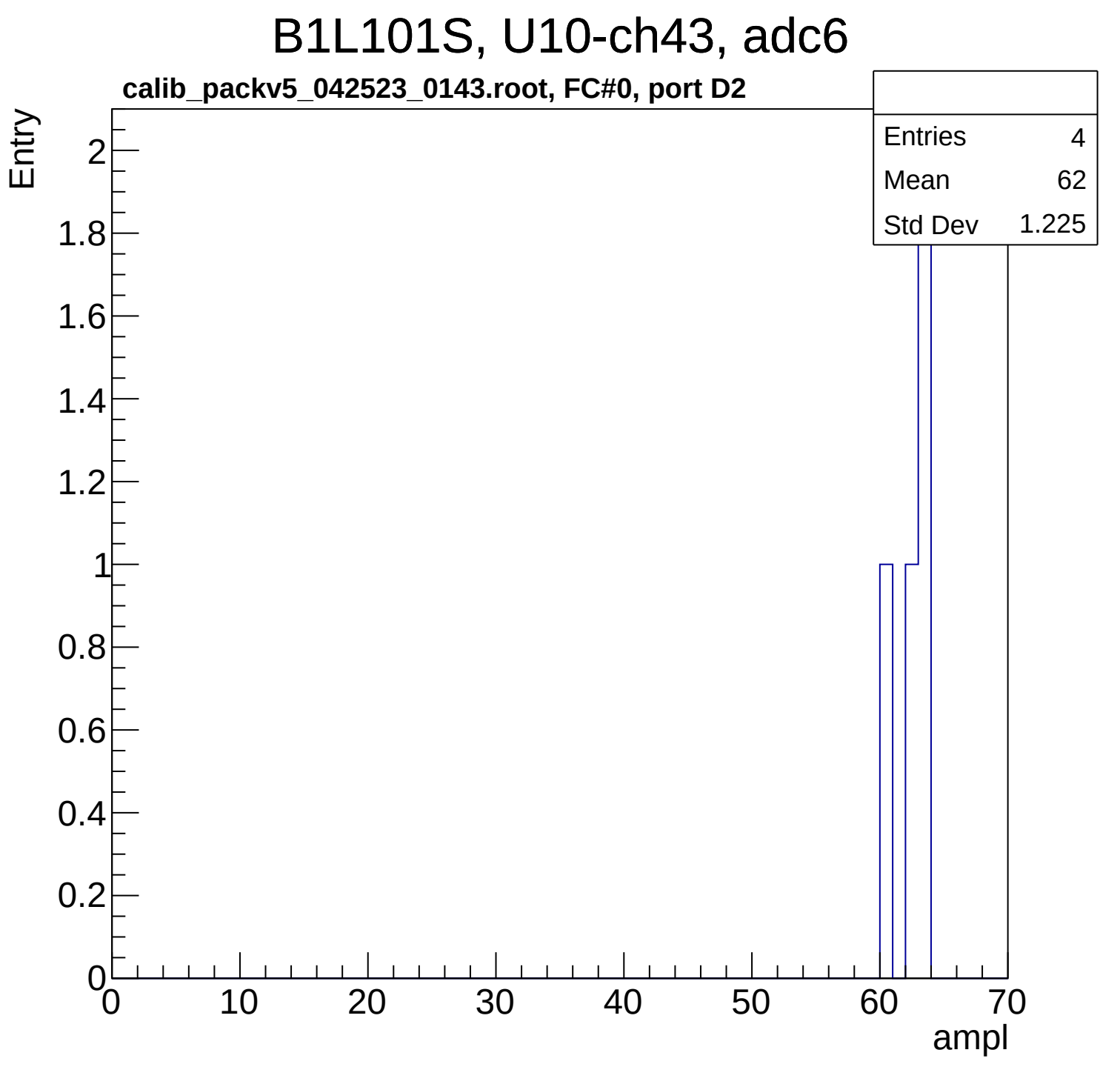
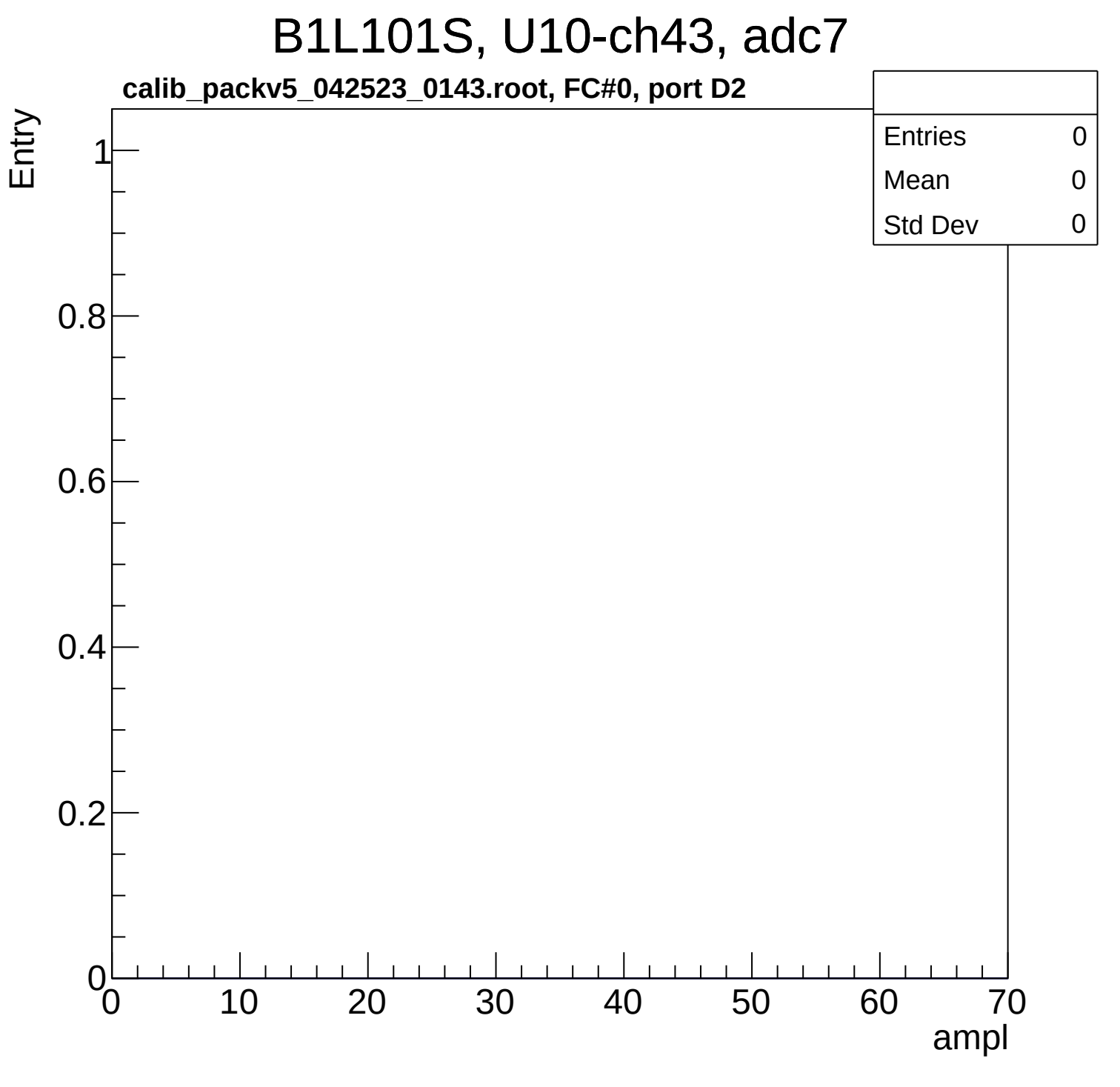
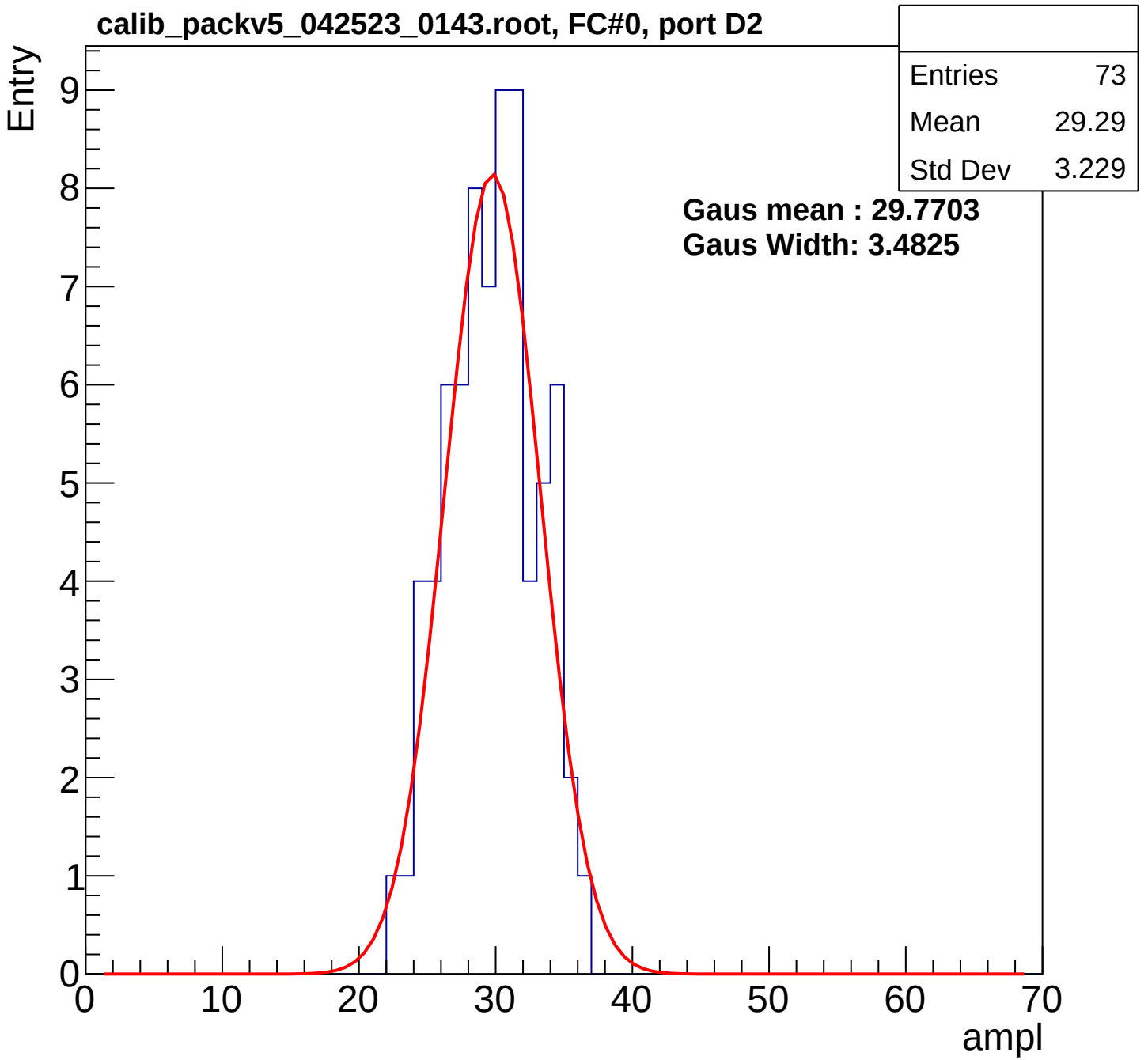
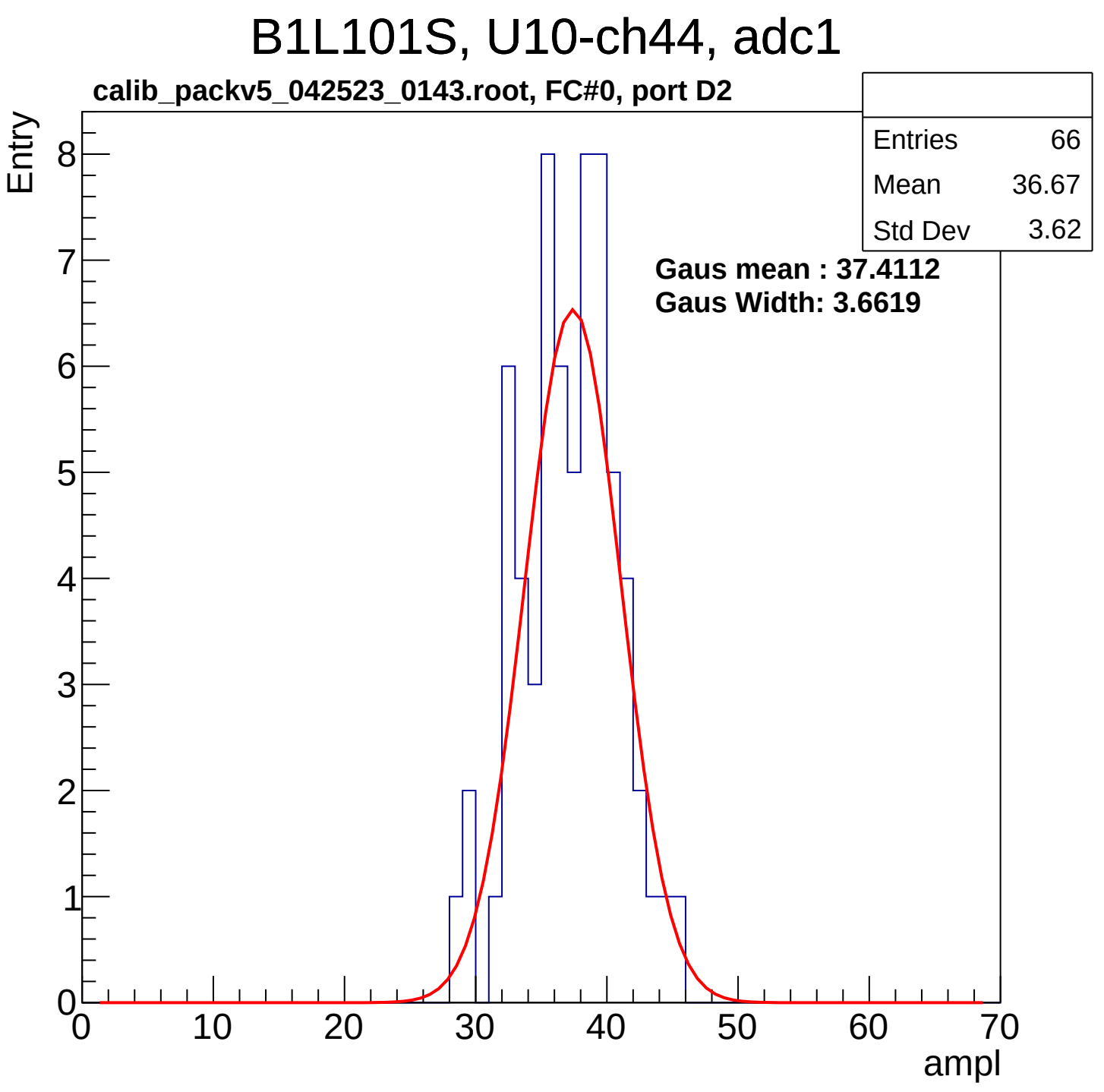

B1L101S, U10-ch43, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 62
Std Dev 1.225
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U10-ch43, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch44, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 29.29
Std Dev 3.229
Gaus mean : 29.7703
Gaus Width: 3.4825
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch44, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 36.67
Std Dev 3.62
Gaus mean : 37.4112
Gaus Width: 3.6619
Entry
ampl
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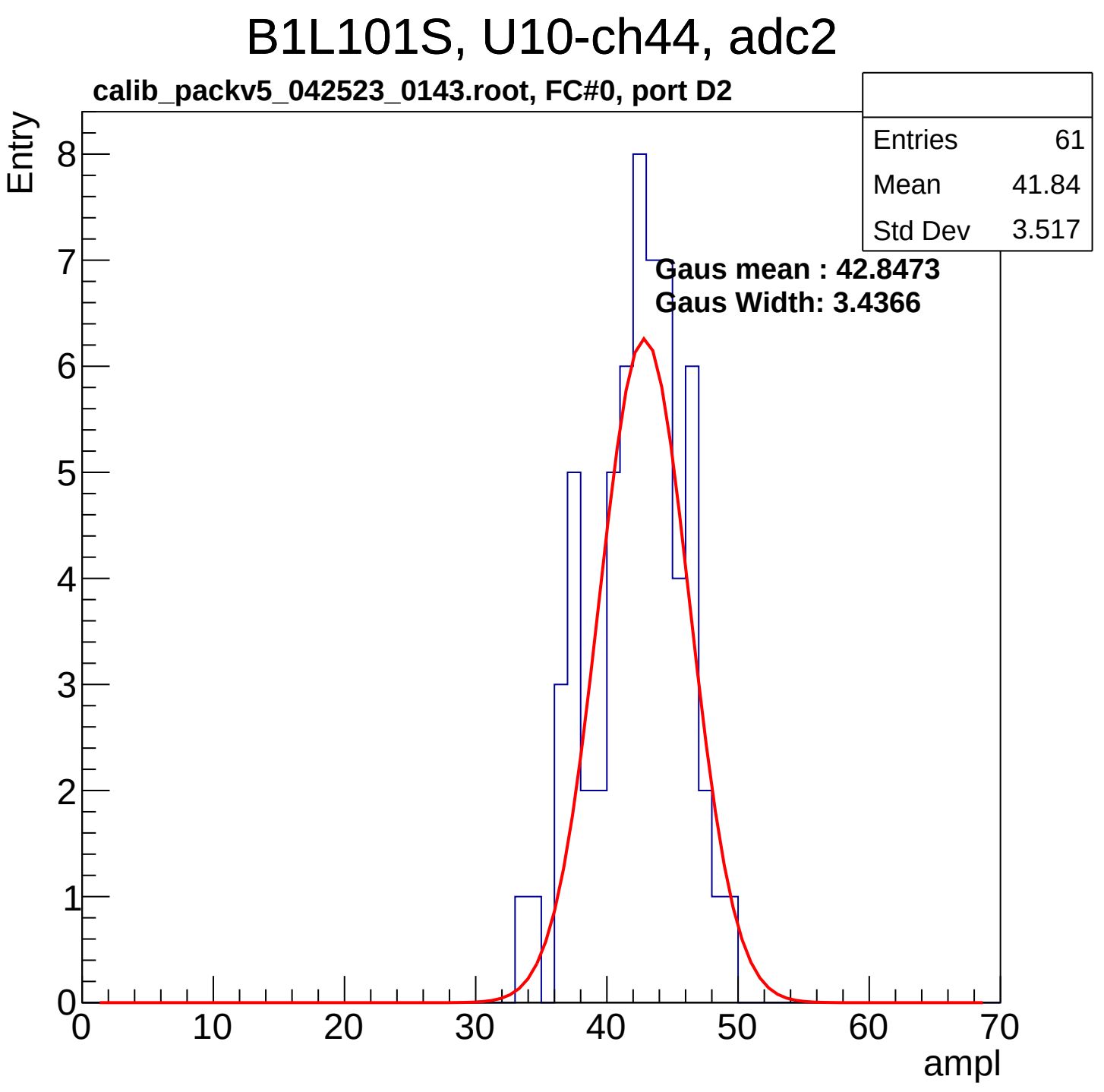
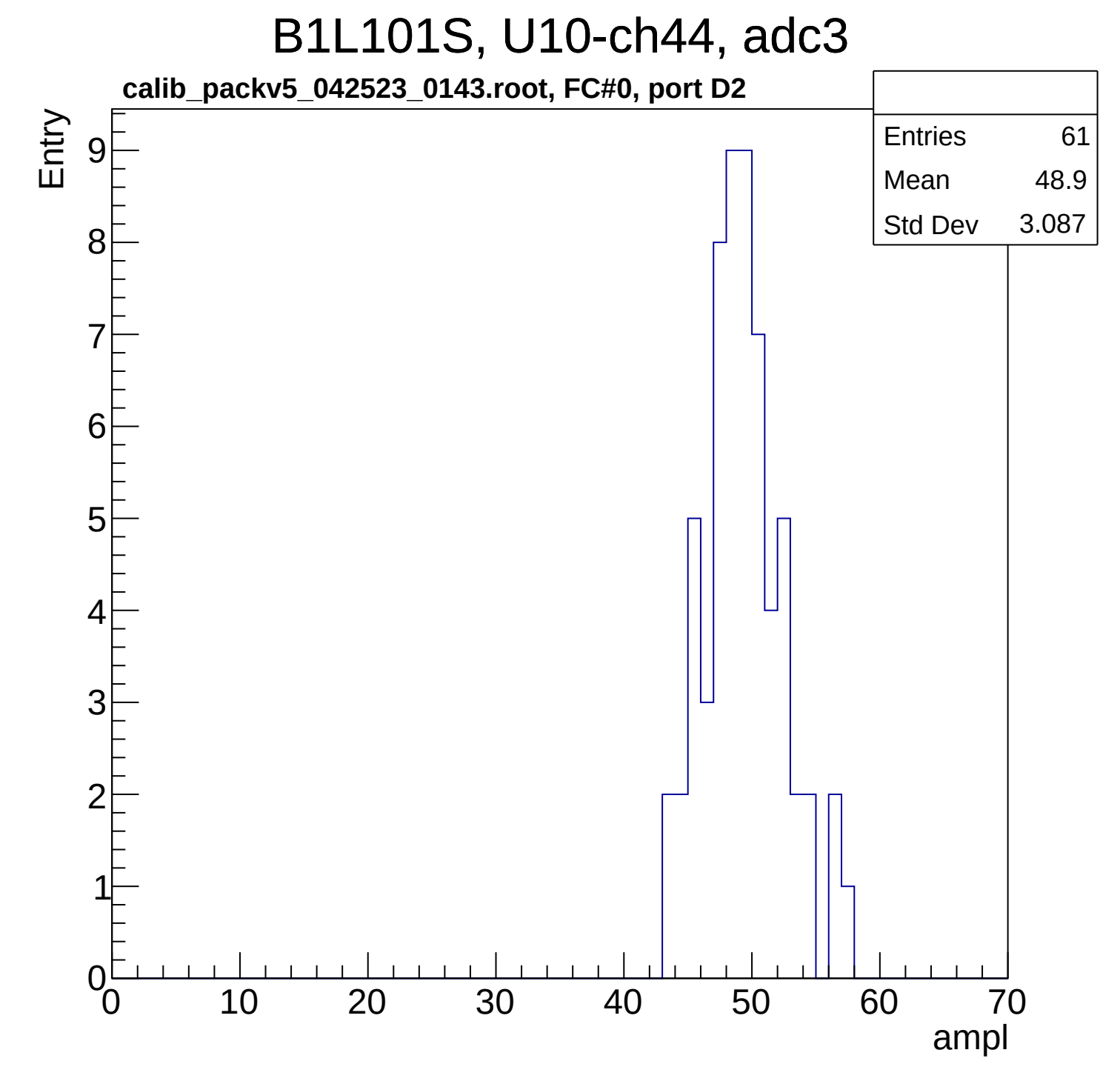
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch44, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 41.84
Std Dev 3.517
Gaus mean : 42.8473
Gaus Width: 3.4366
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch44, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 48.9
Std Dev 3.087
Entry
ampl
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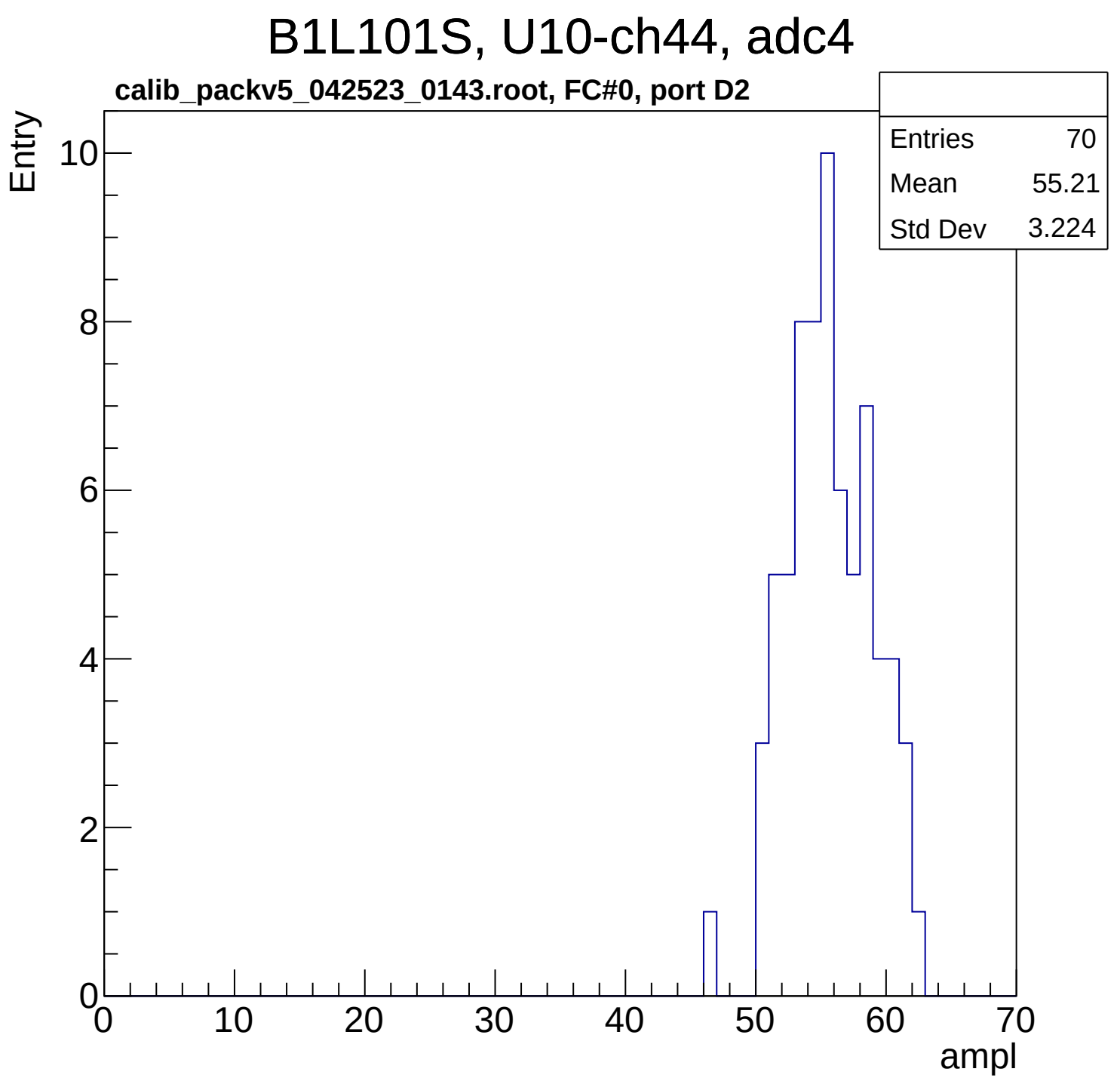
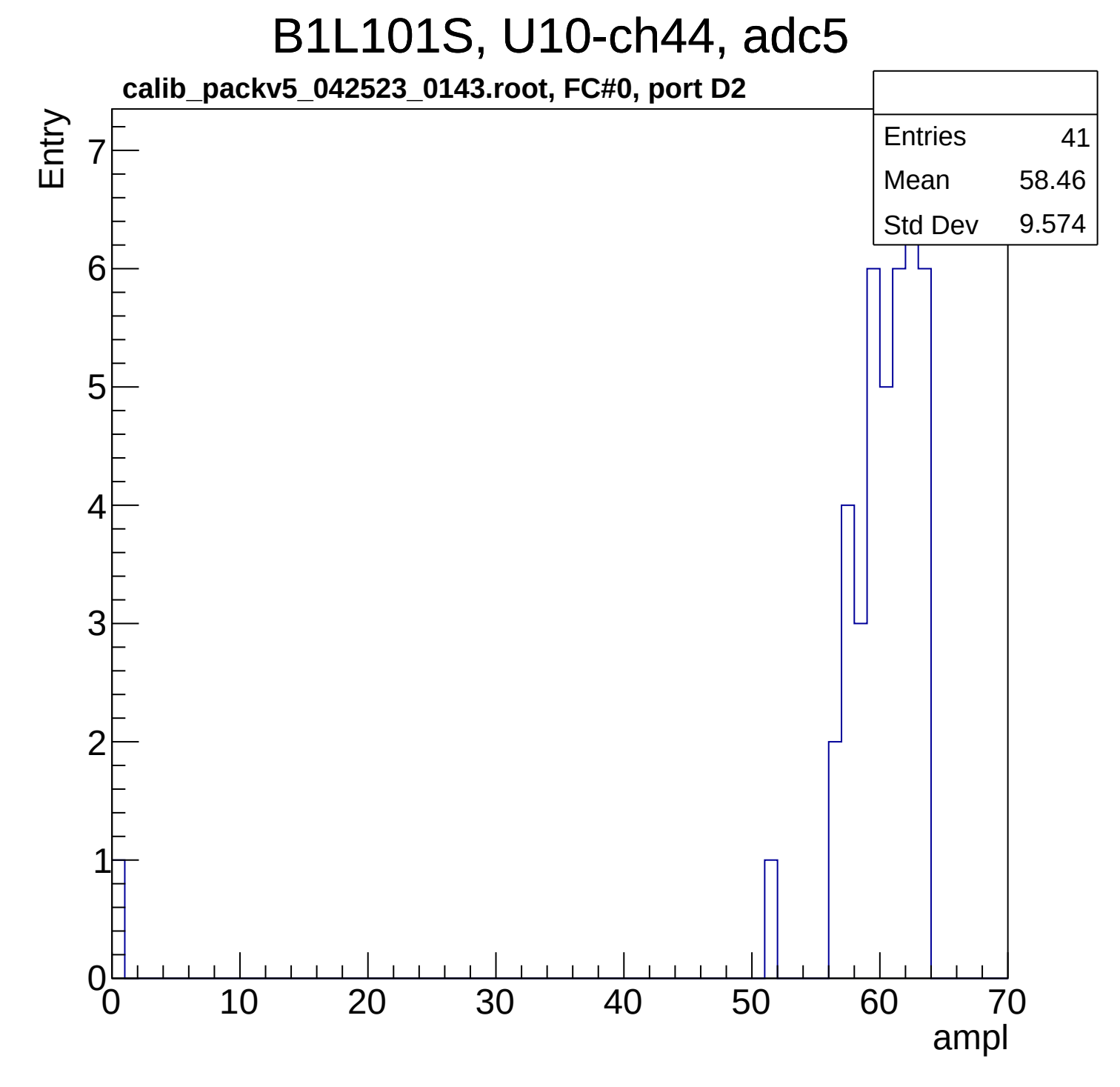
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch44, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 55.21
Std Dev 3.224
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch44, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 41
Mean 58.46
Std Dev 9.574
Entry
ampl
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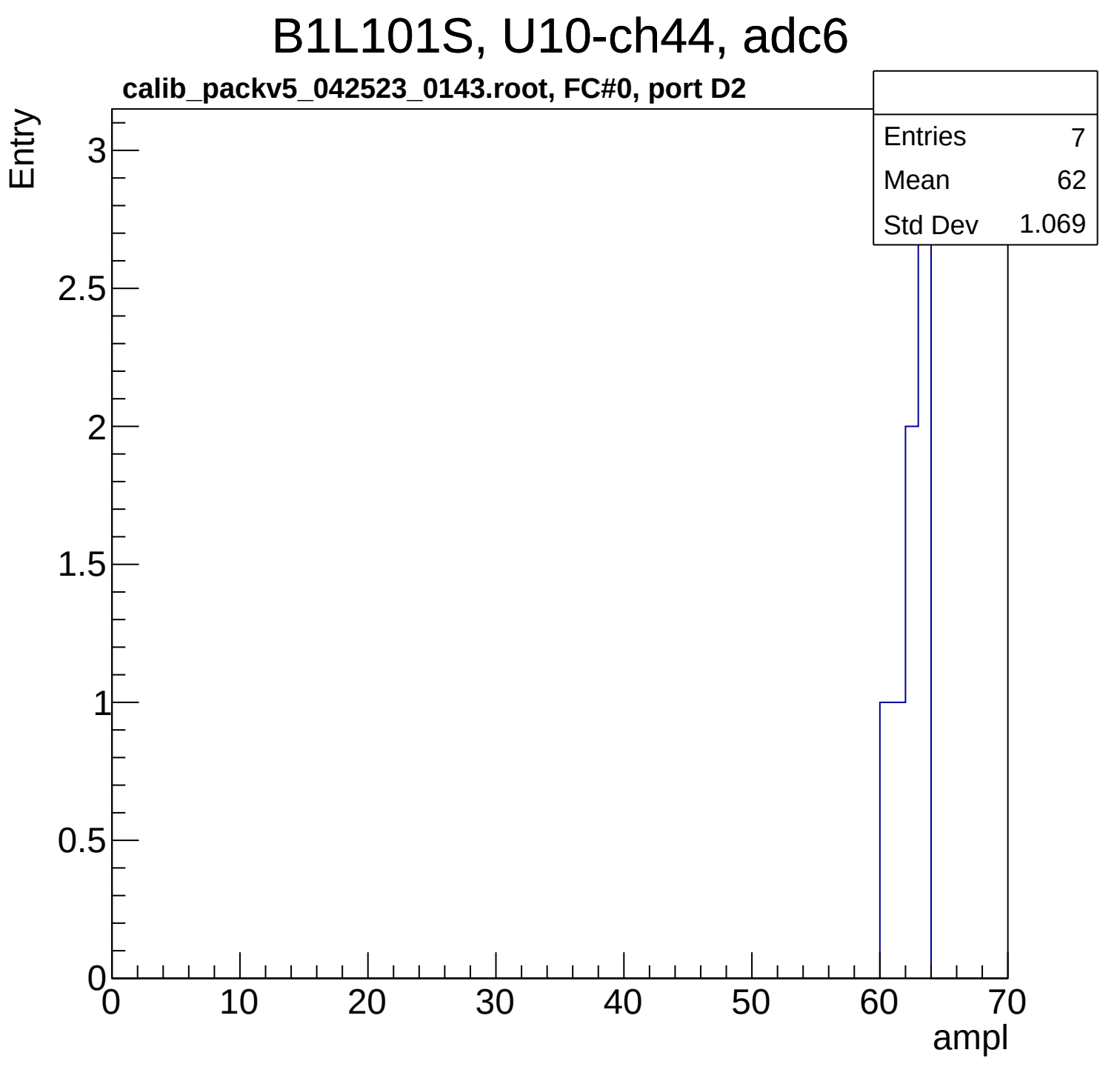
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U10-ch44, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 62
Std Dev 1.069
Entry
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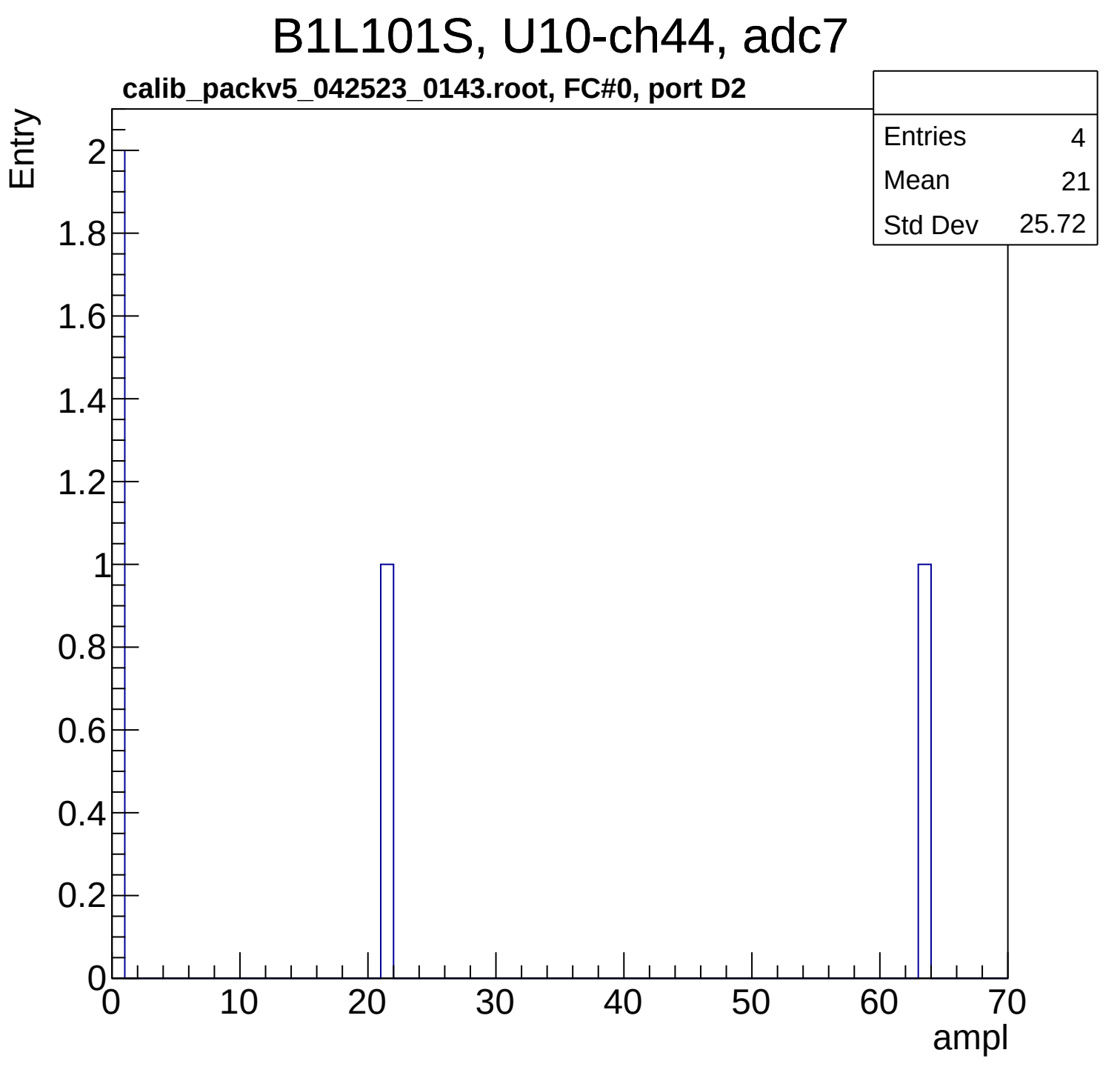
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch44, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 21
Std Dev 25.72
Entry
ampl
0
0.2
0.4
0.6
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1
1.2
1.4
1.6
1.8
2
0
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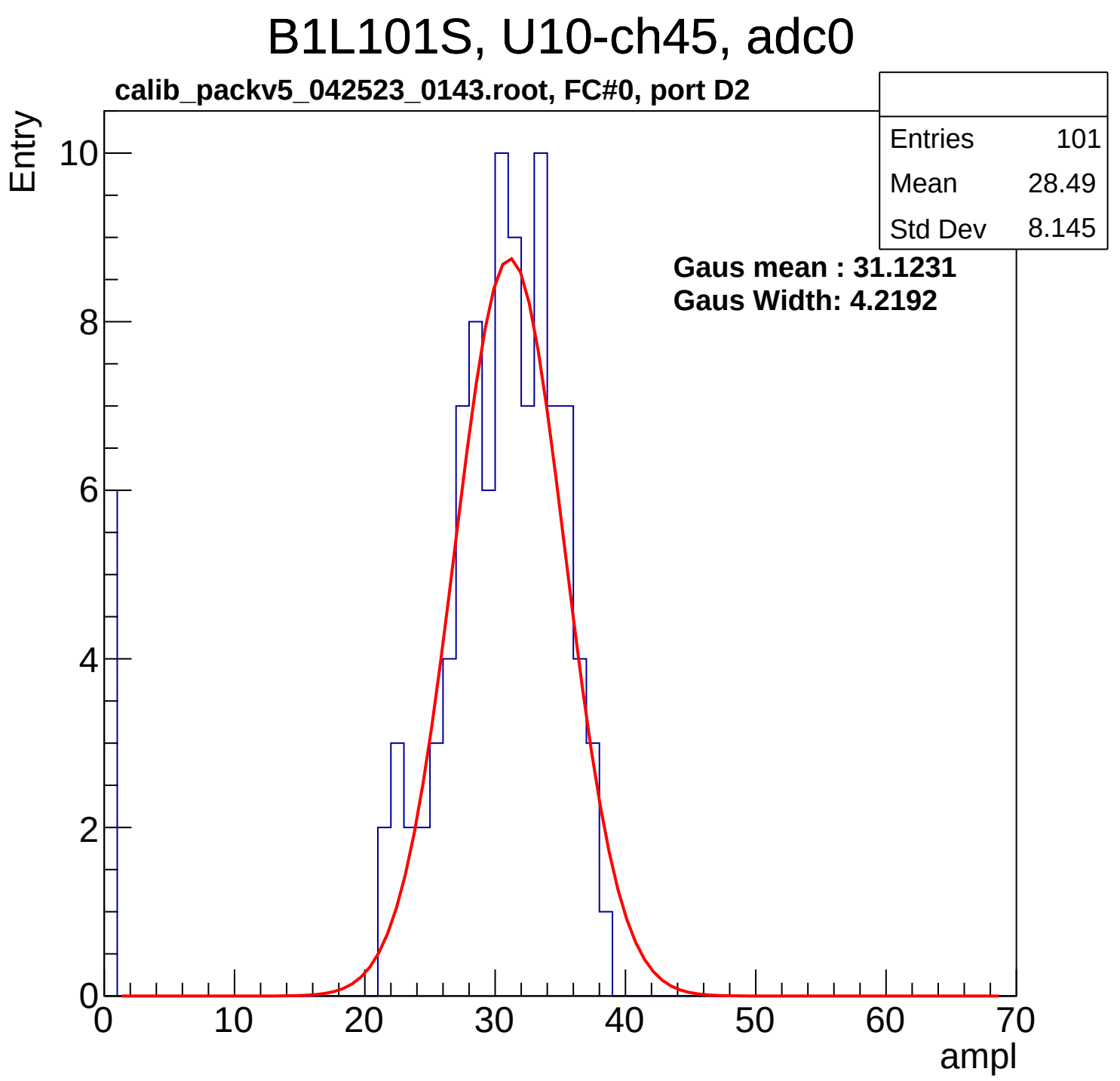
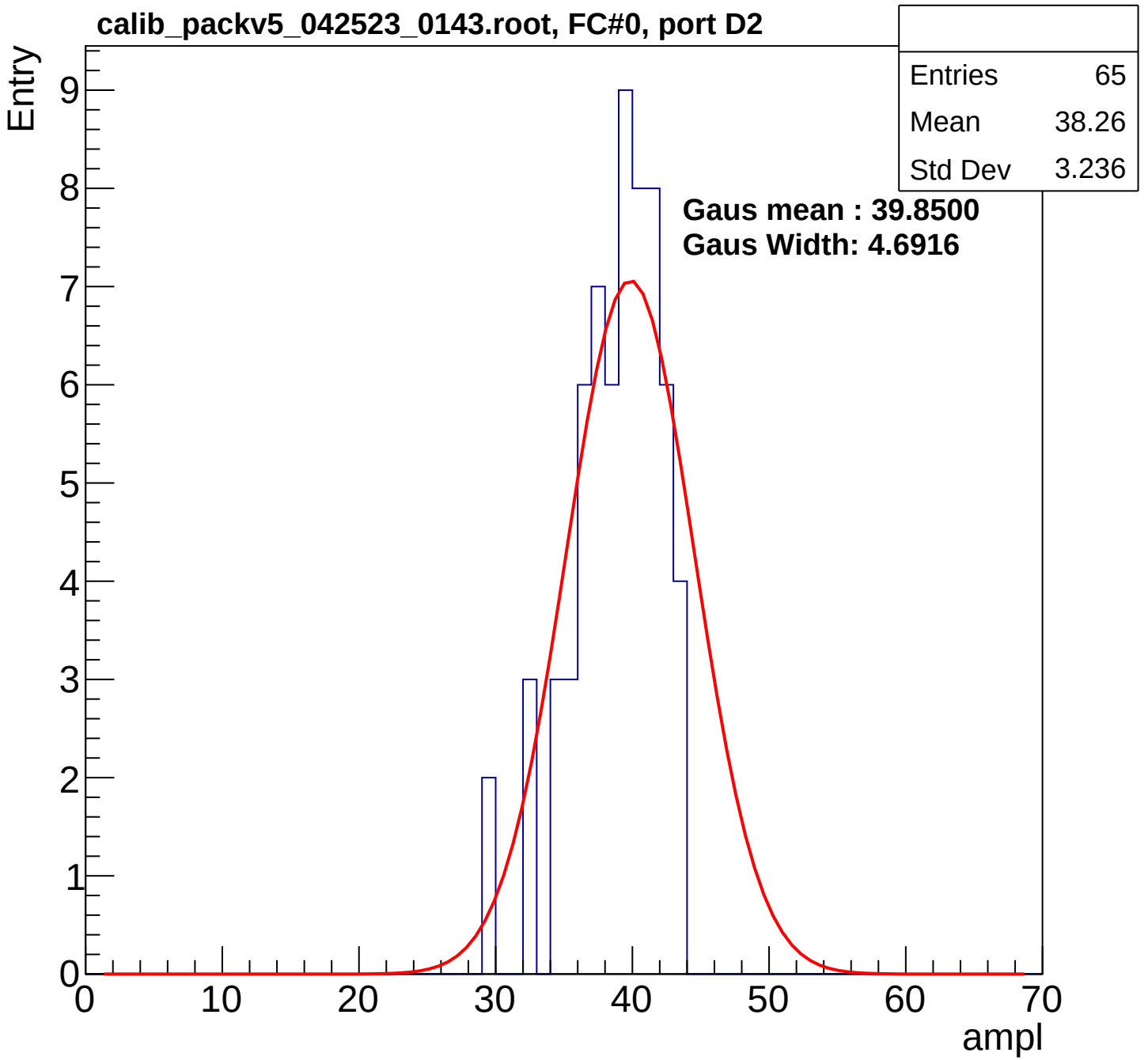
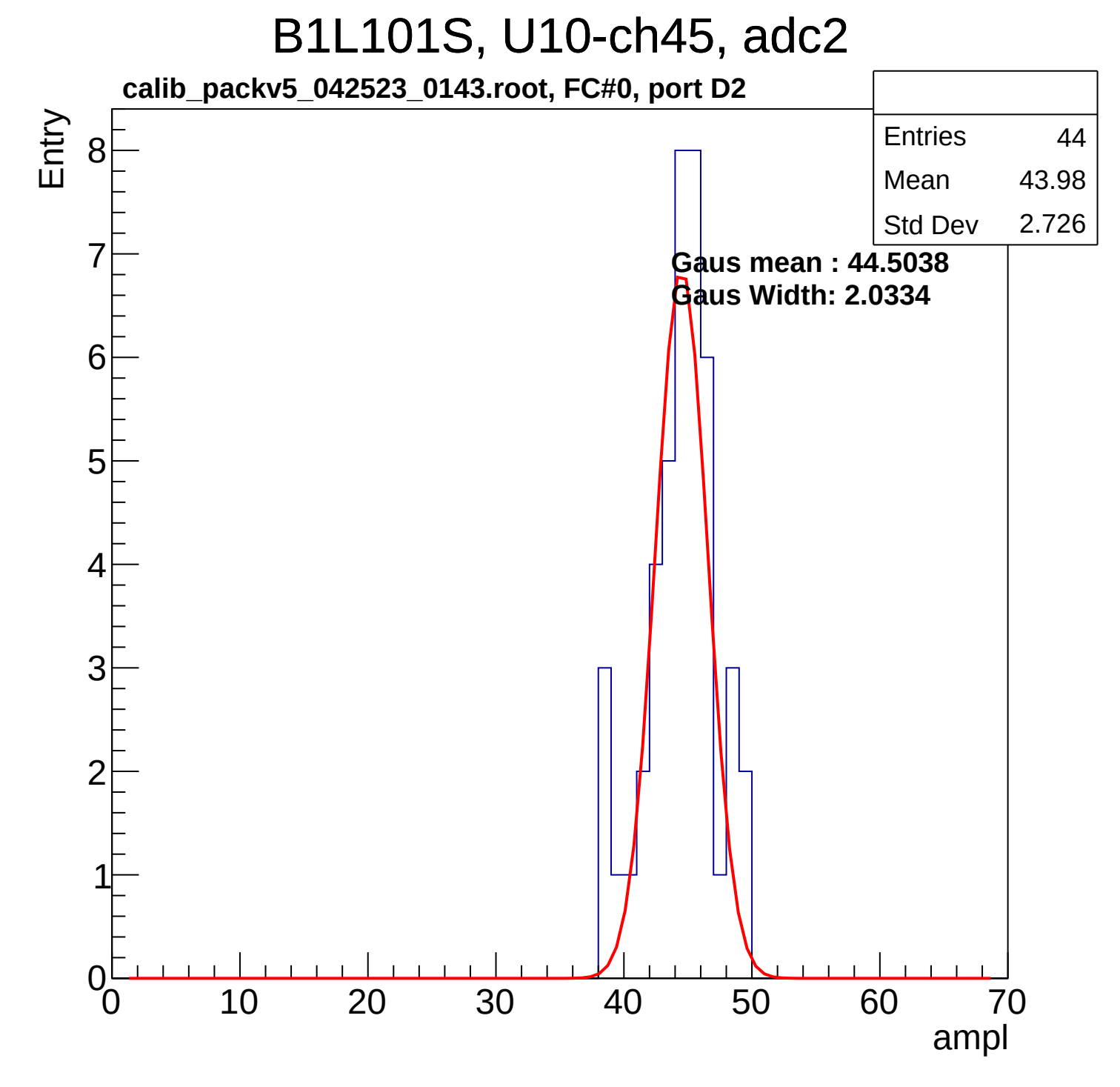
20
30
40
50
60
70


B1L101S, U10-ch45, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 101
Mean 28.49
Std Dev 8.145
Gaus mean : 31.1231
Gaus Width: 4.2192
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch45, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 38.26
Std Dev 3.236
Gaus mean : 39.8500
Gaus Width: 4.6916
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch45, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 44
Mean 43.98
Std Dev 2.726
Gaus mean : 44.5038
Gaus Width: 2.0334
Entry
ampl
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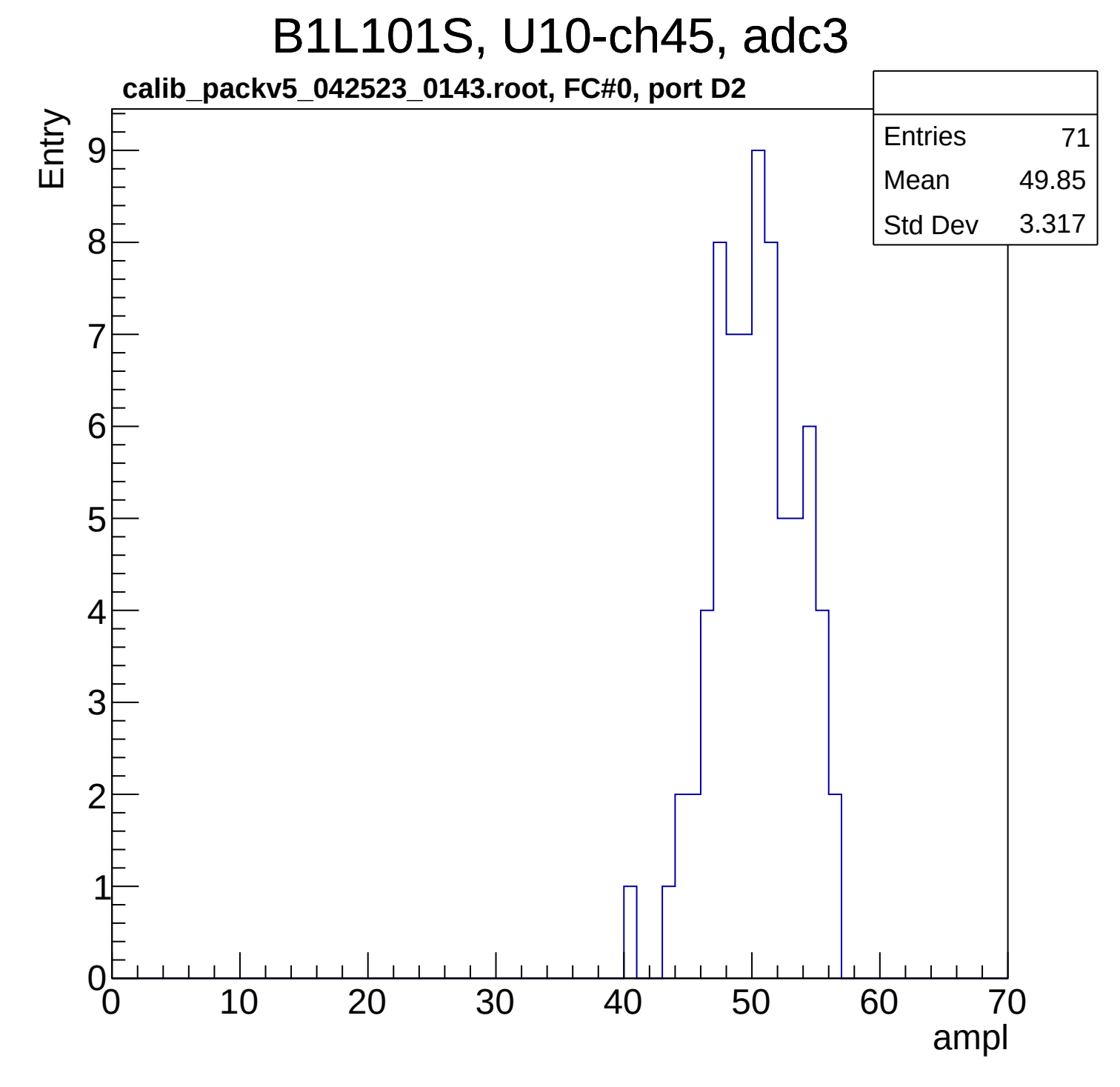
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch45, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 49.85
Std Dev 3.317
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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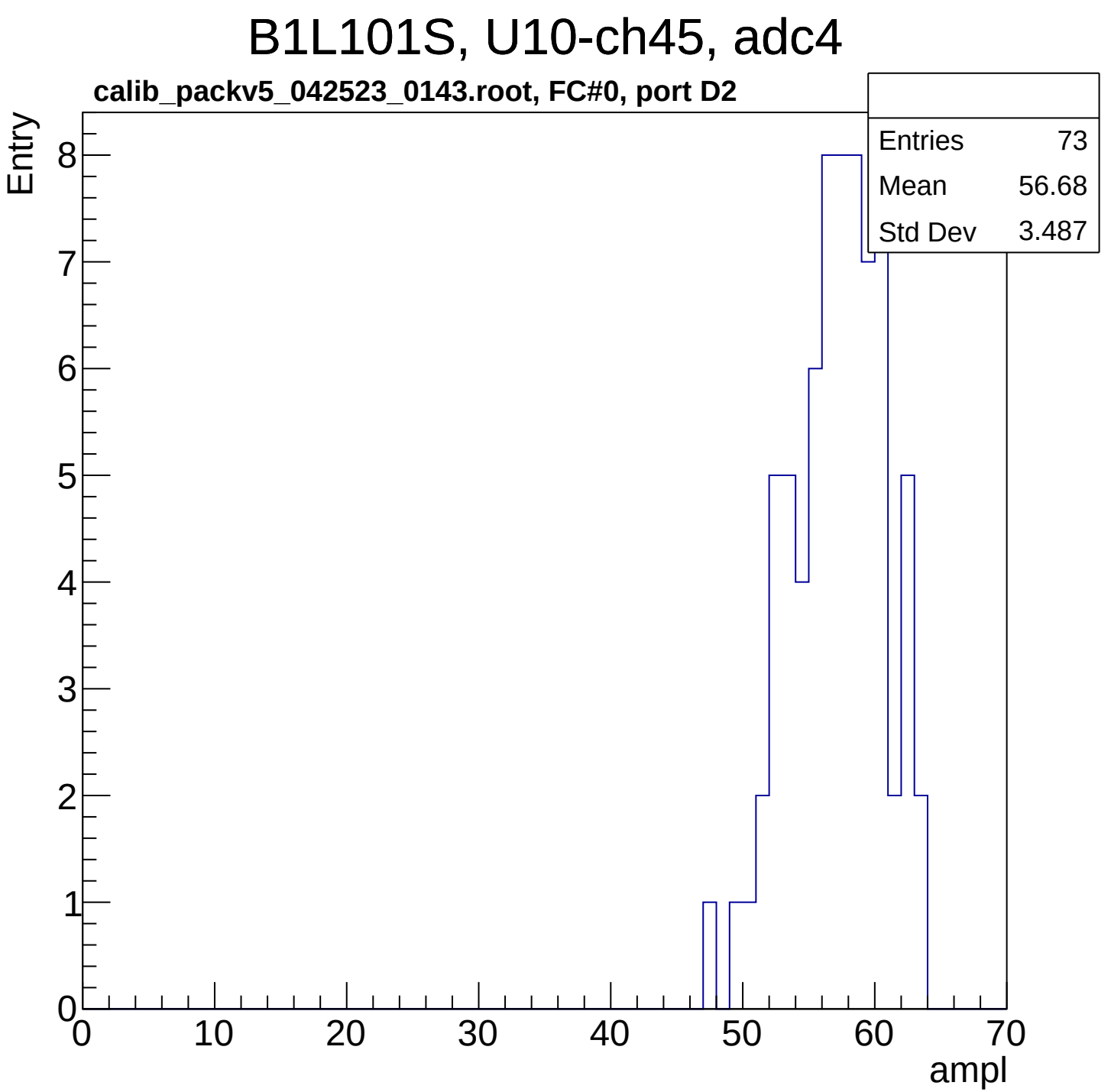
40
50
60
70


B1L101S, U10-ch45, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 56.68
Std Dev 3.487
Entry
ampl
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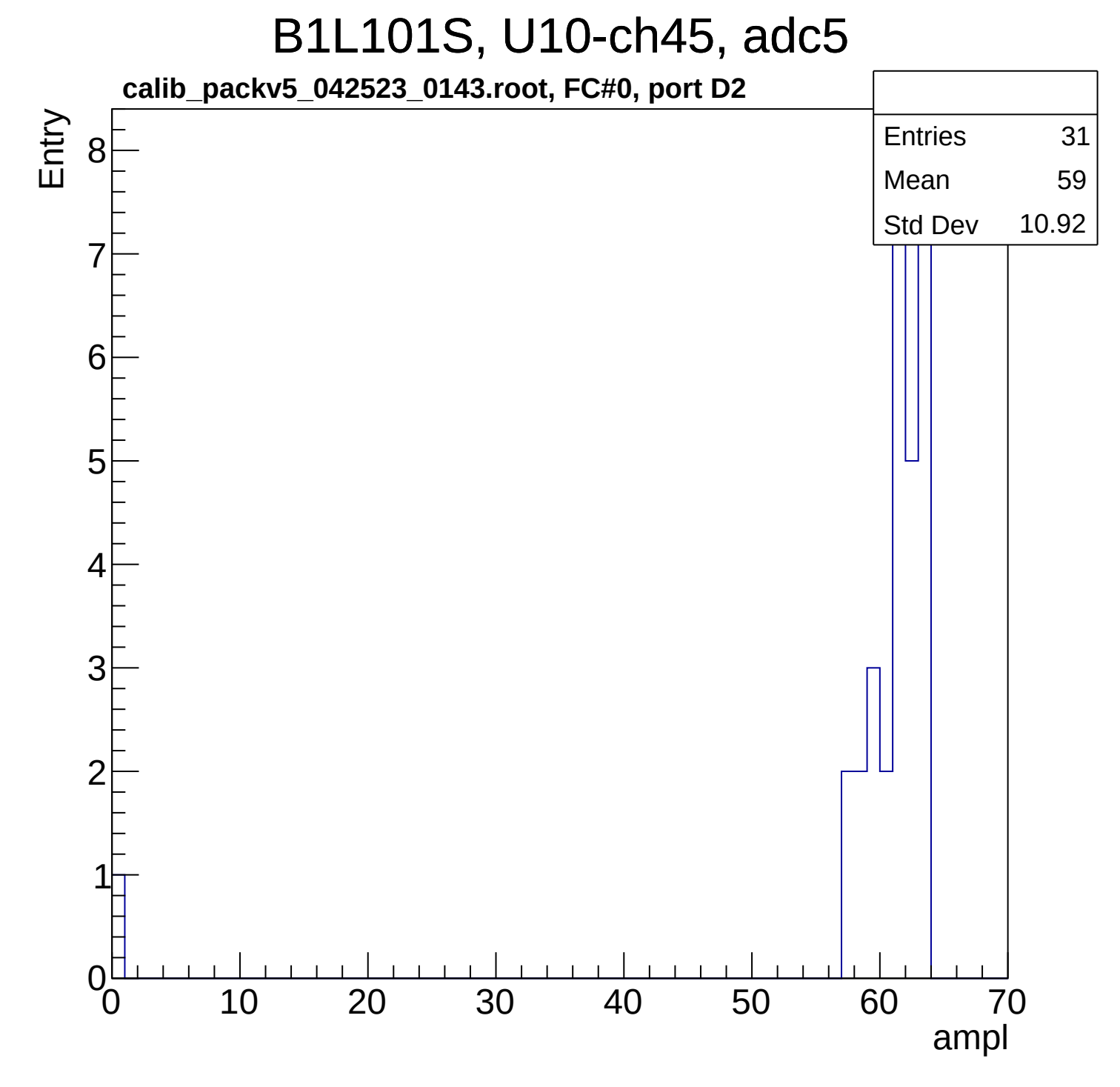
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch45, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 31
Mean 59
Std Dev 10.92
Entry
ampl
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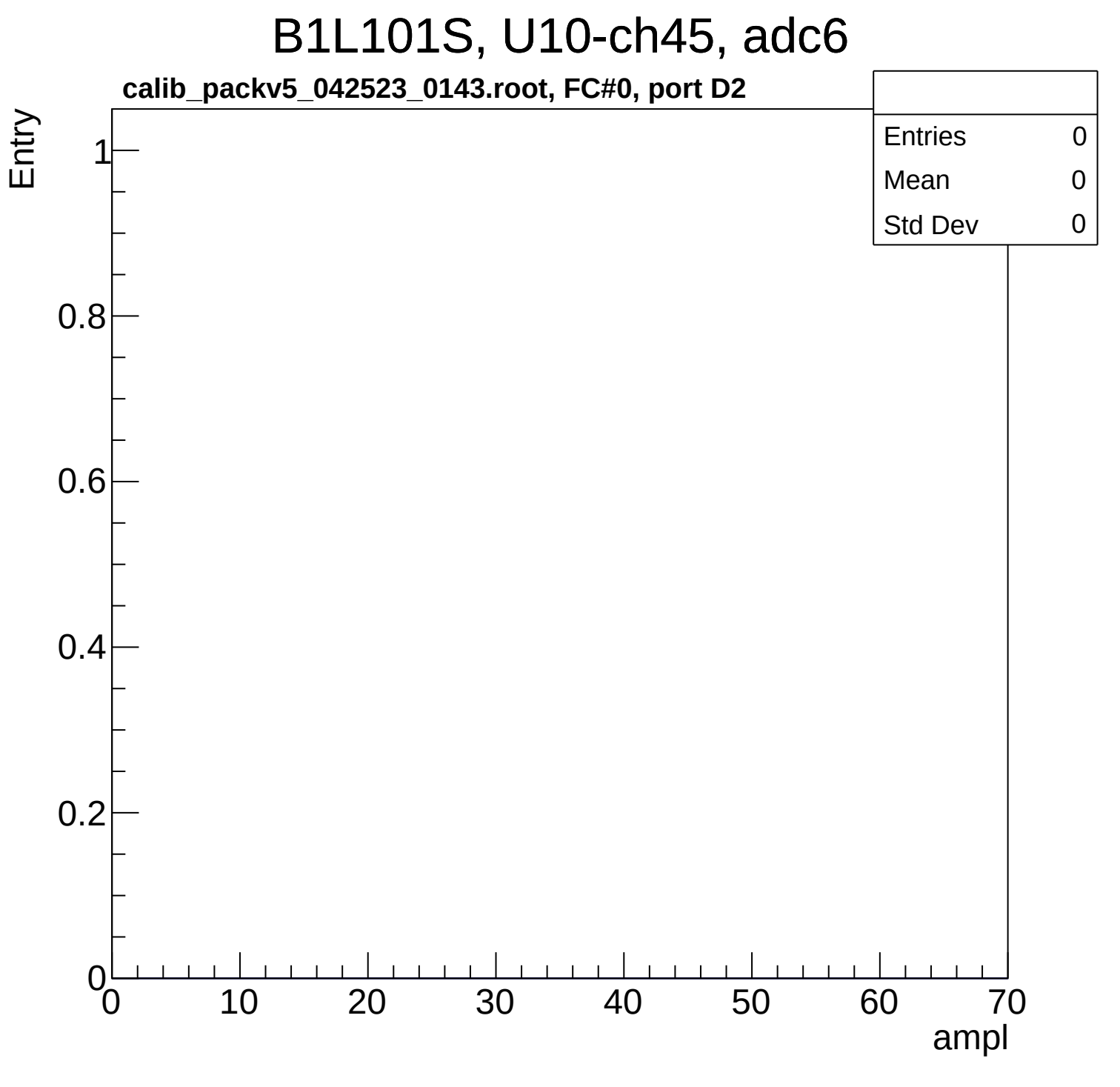
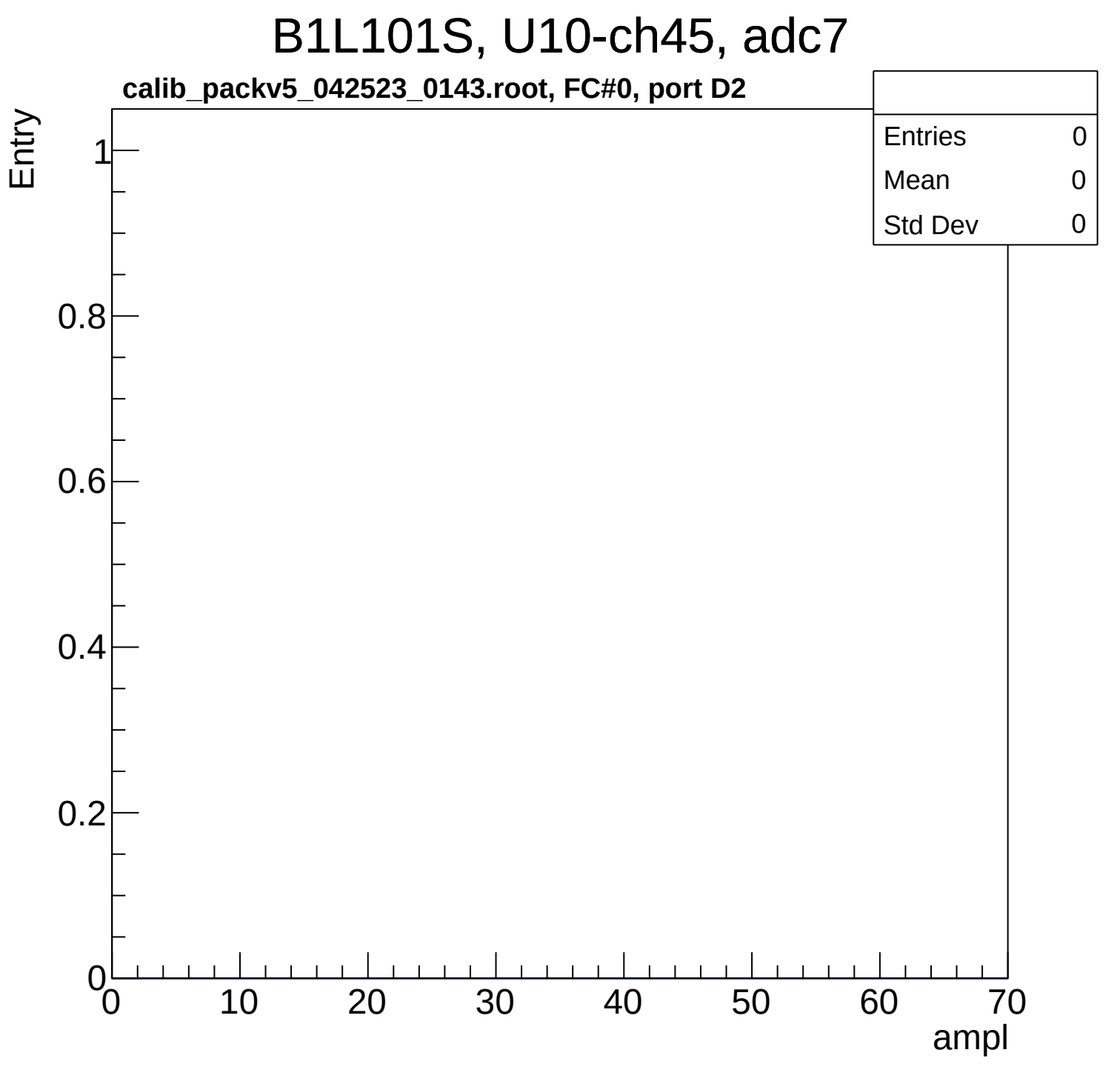
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch45, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch45, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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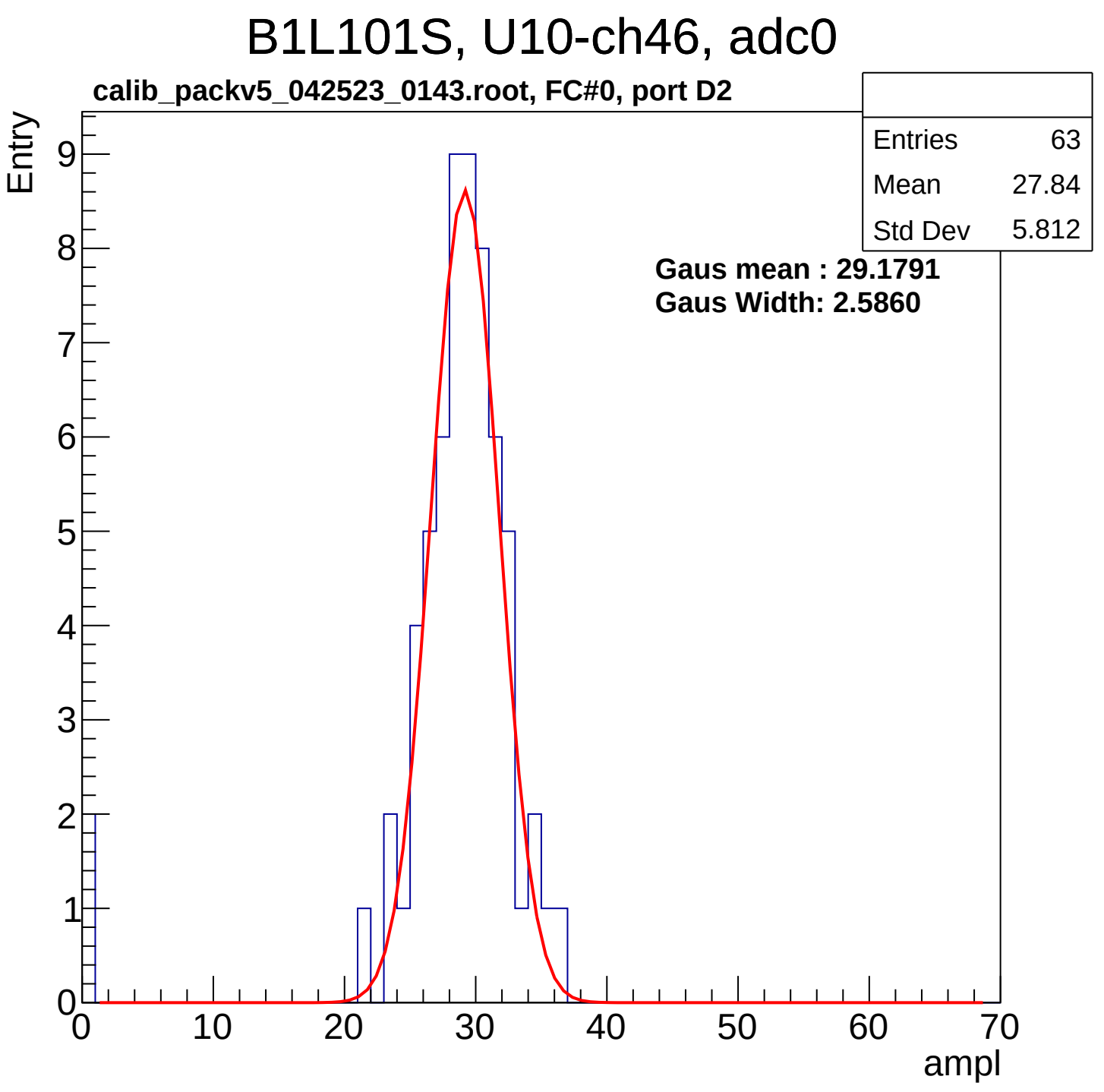
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch46, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 27.84
Std Dev 5.812
Gaus mean : 29.1791
Gaus Width: 2.5860
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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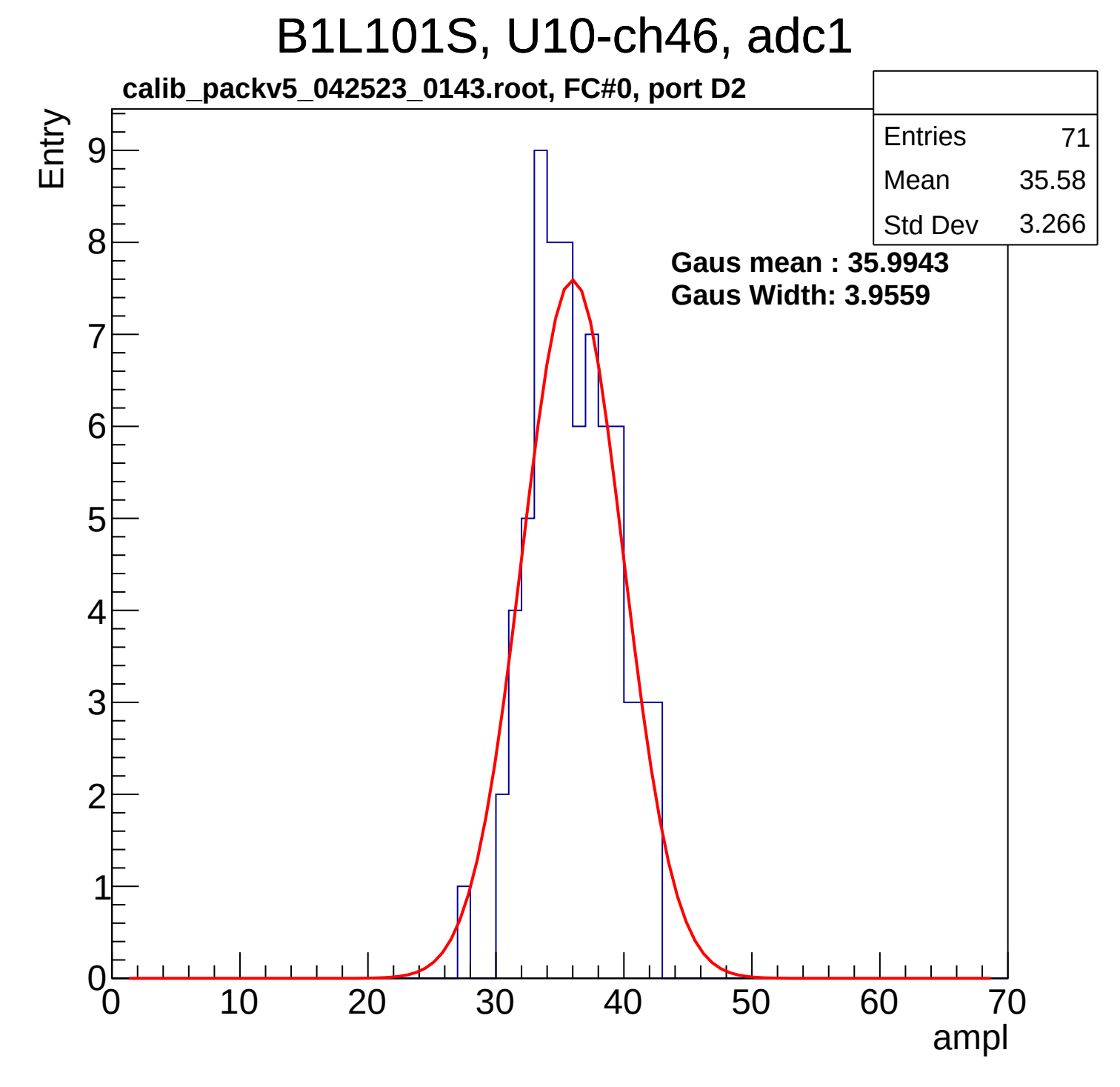
B1L101S, U10-ch46, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 35.58
Std Dev 3.266
Gaus mean : 35.9943
Gaus Width: 3.9559
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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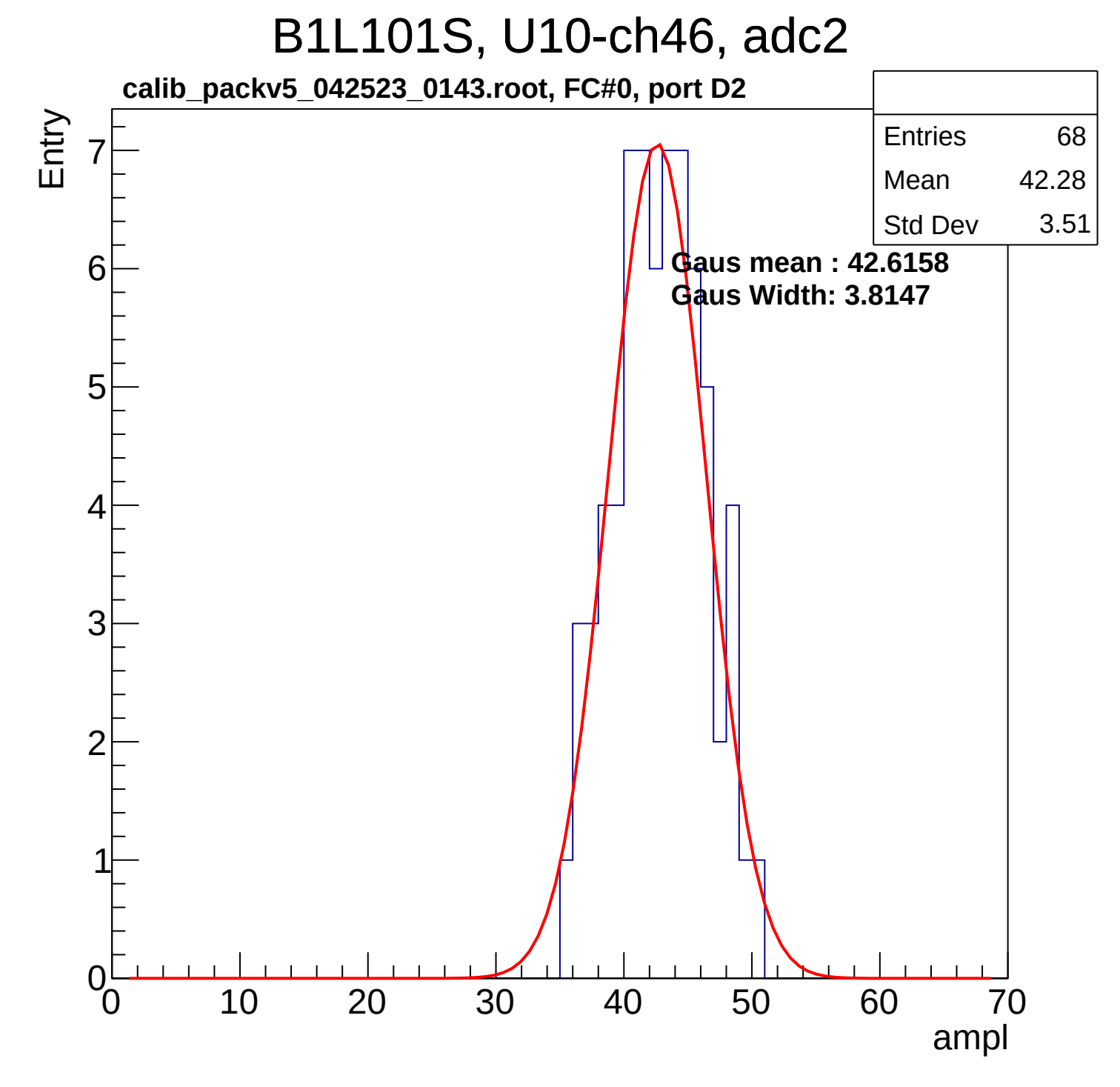
B1L101S, U10-ch46, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 42.28
Std Dev 3.51
Gaus mean : 42.6158
Gaus Width: 3.8147
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
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60
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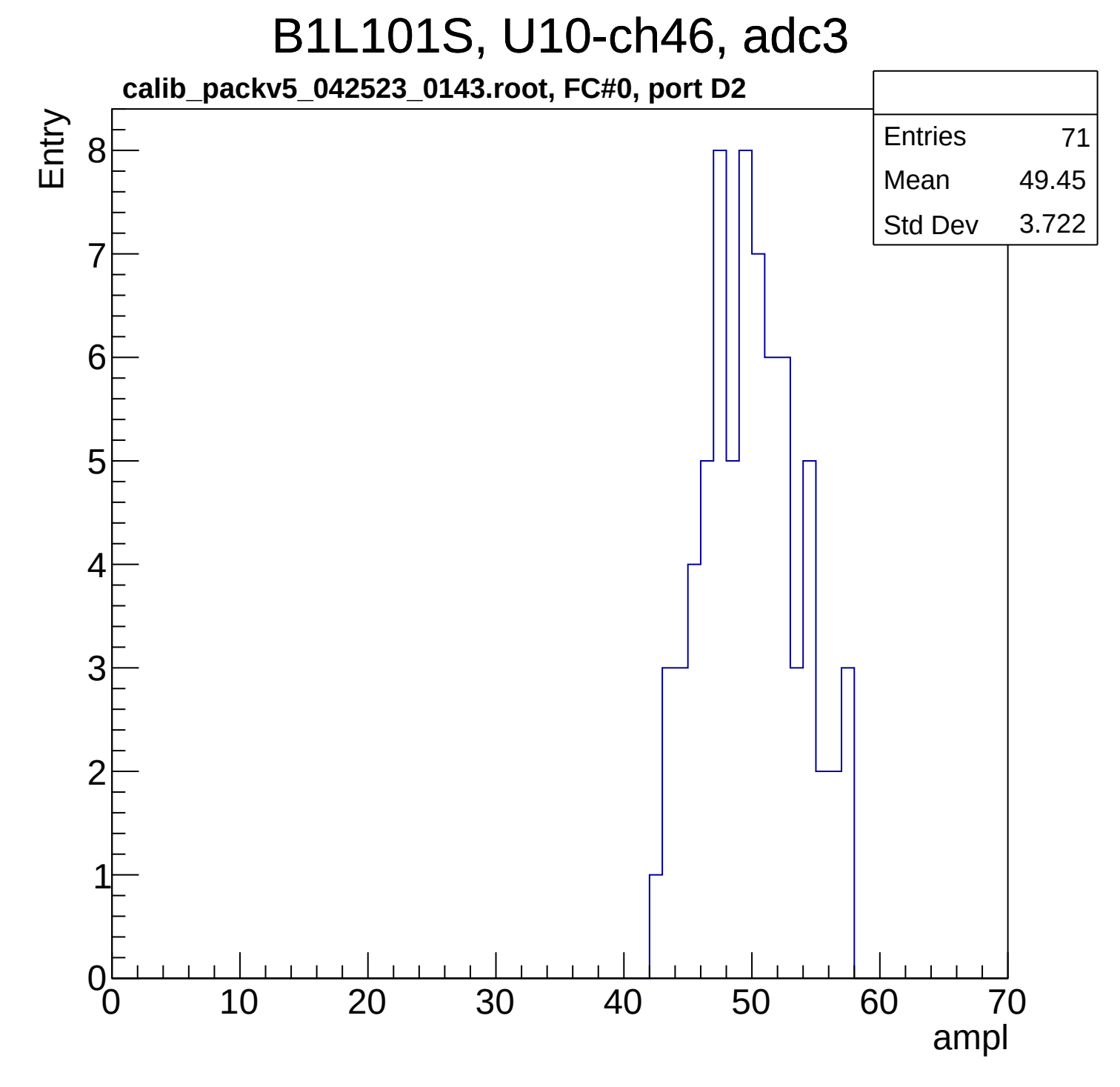
B1L101S, U10-ch46, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 49.45
Std Dev 3.722
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
50
60
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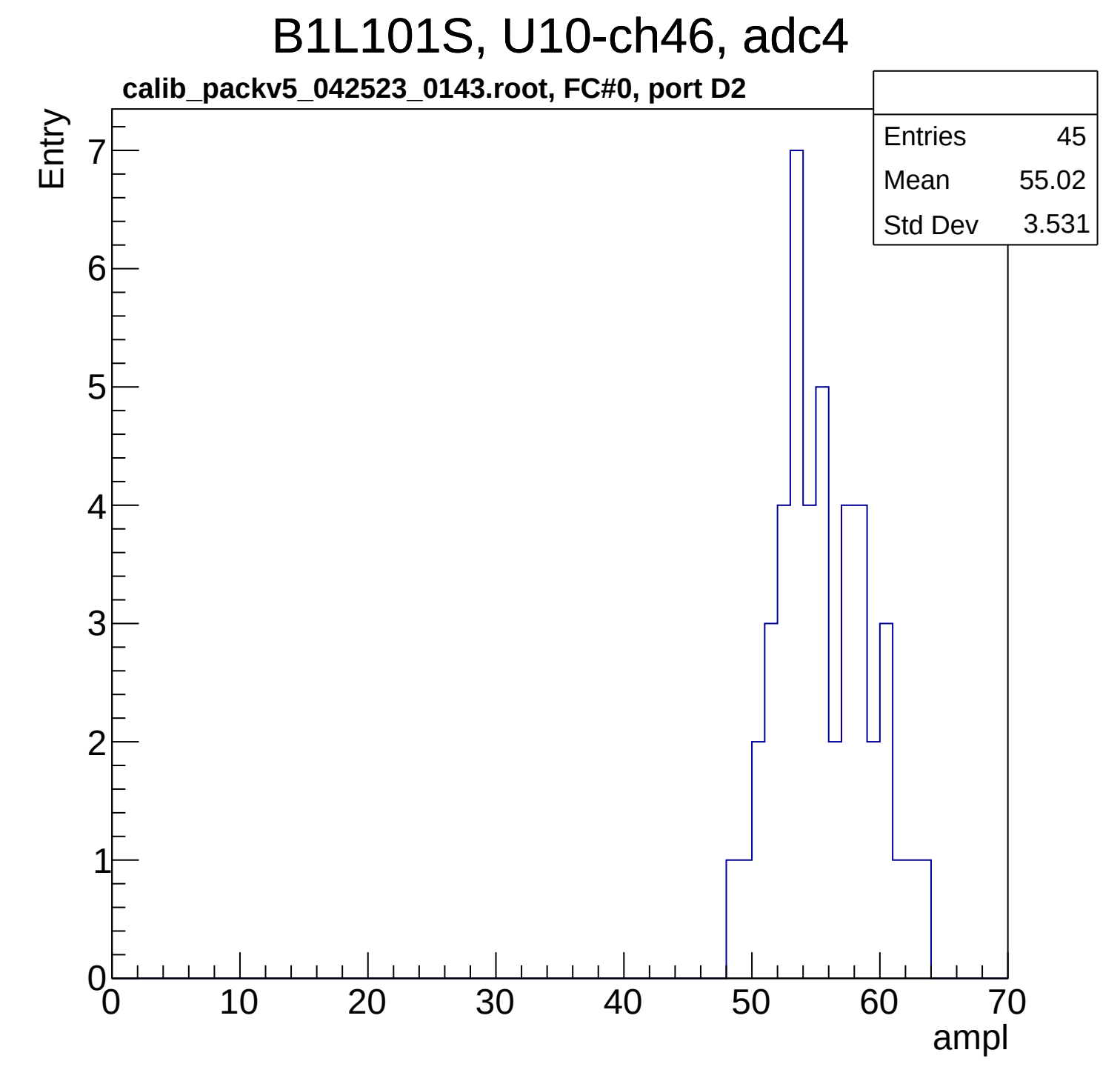
B1L101S, U10-ch46, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 55.02
Std Dev 3.531
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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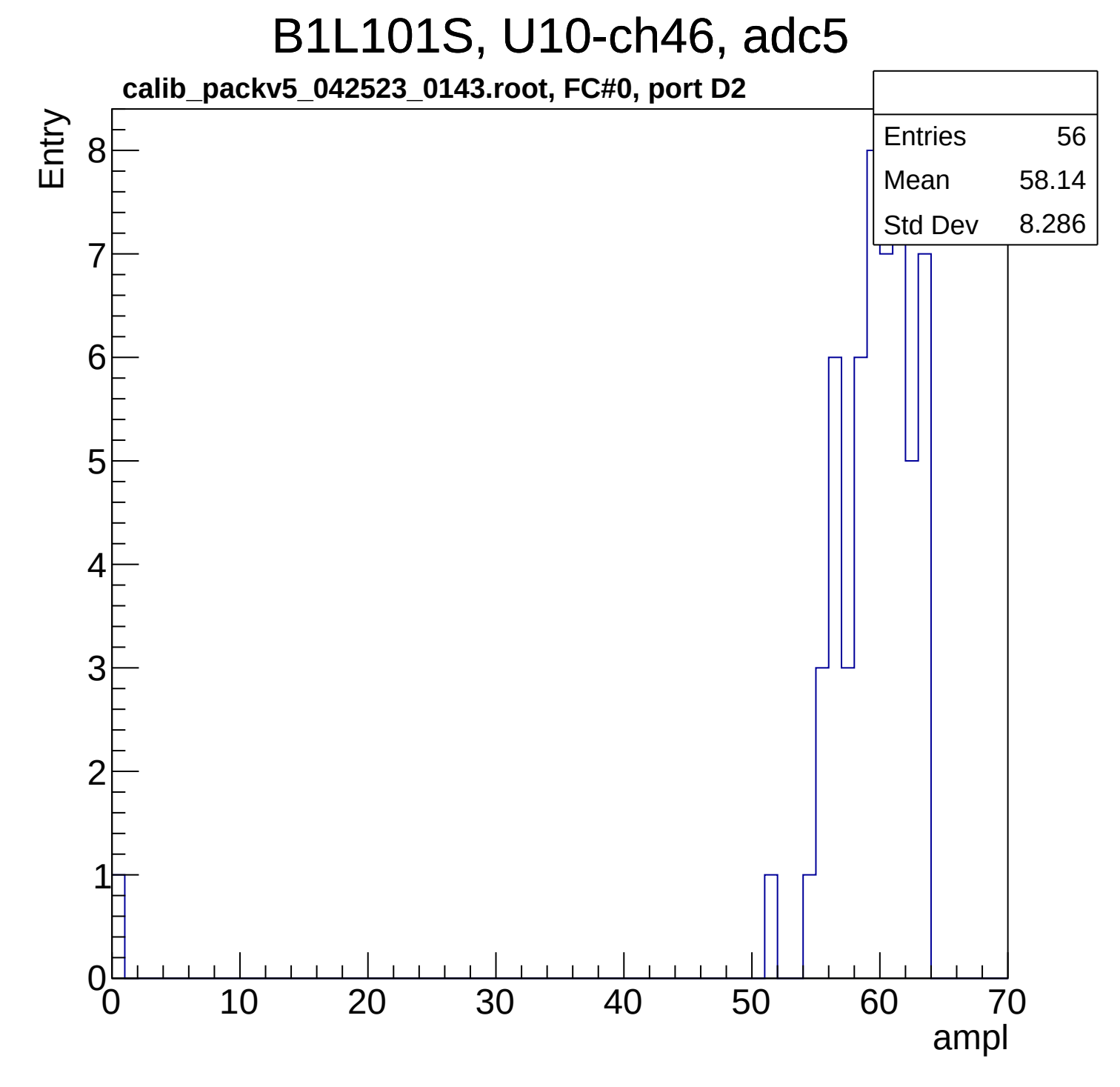
B1L101S, U10-ch46, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 58.14
Std Dev 8.286
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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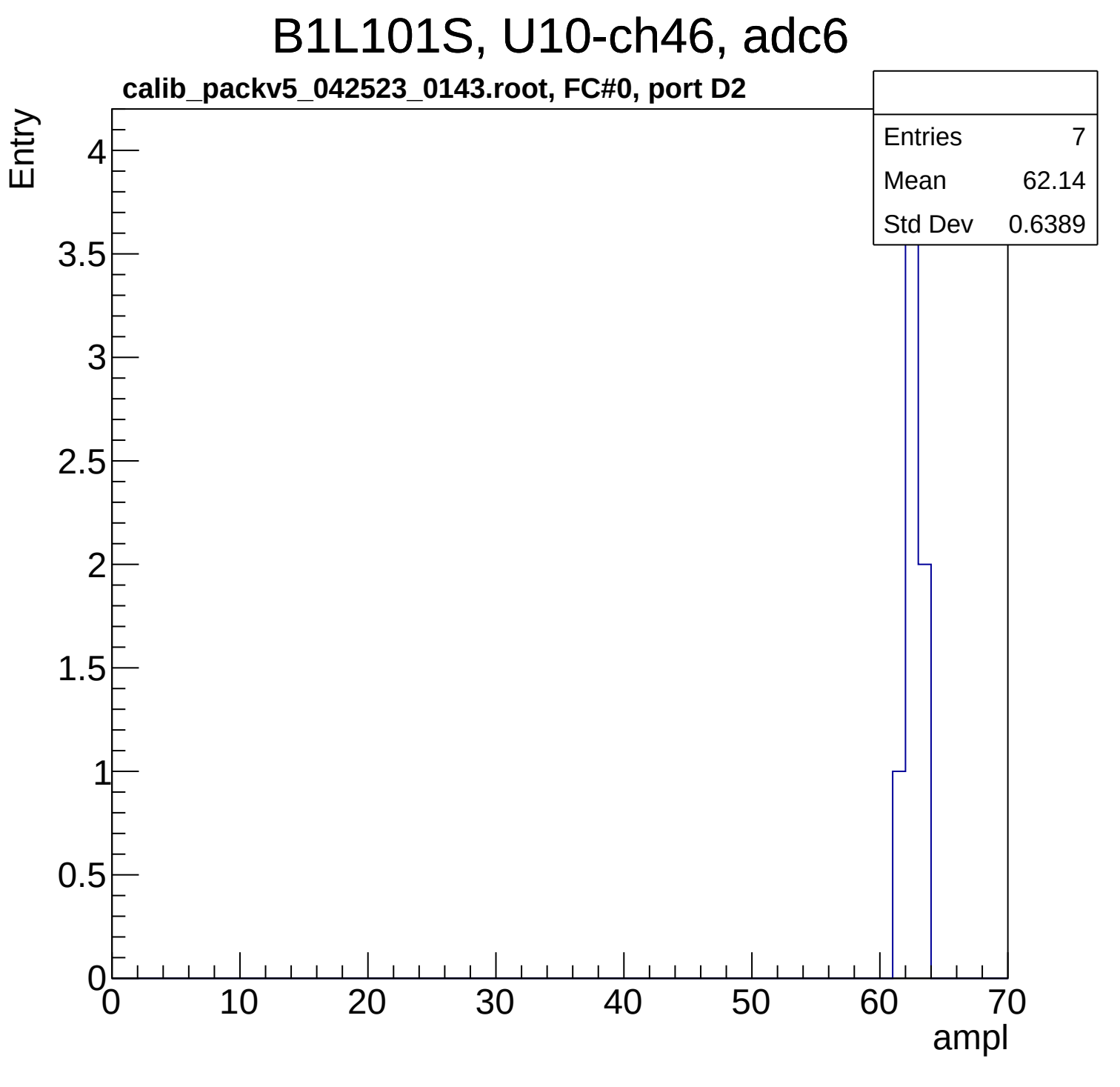
B1L101S, U10-ch46, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 62.14
Std Dev 0.6389
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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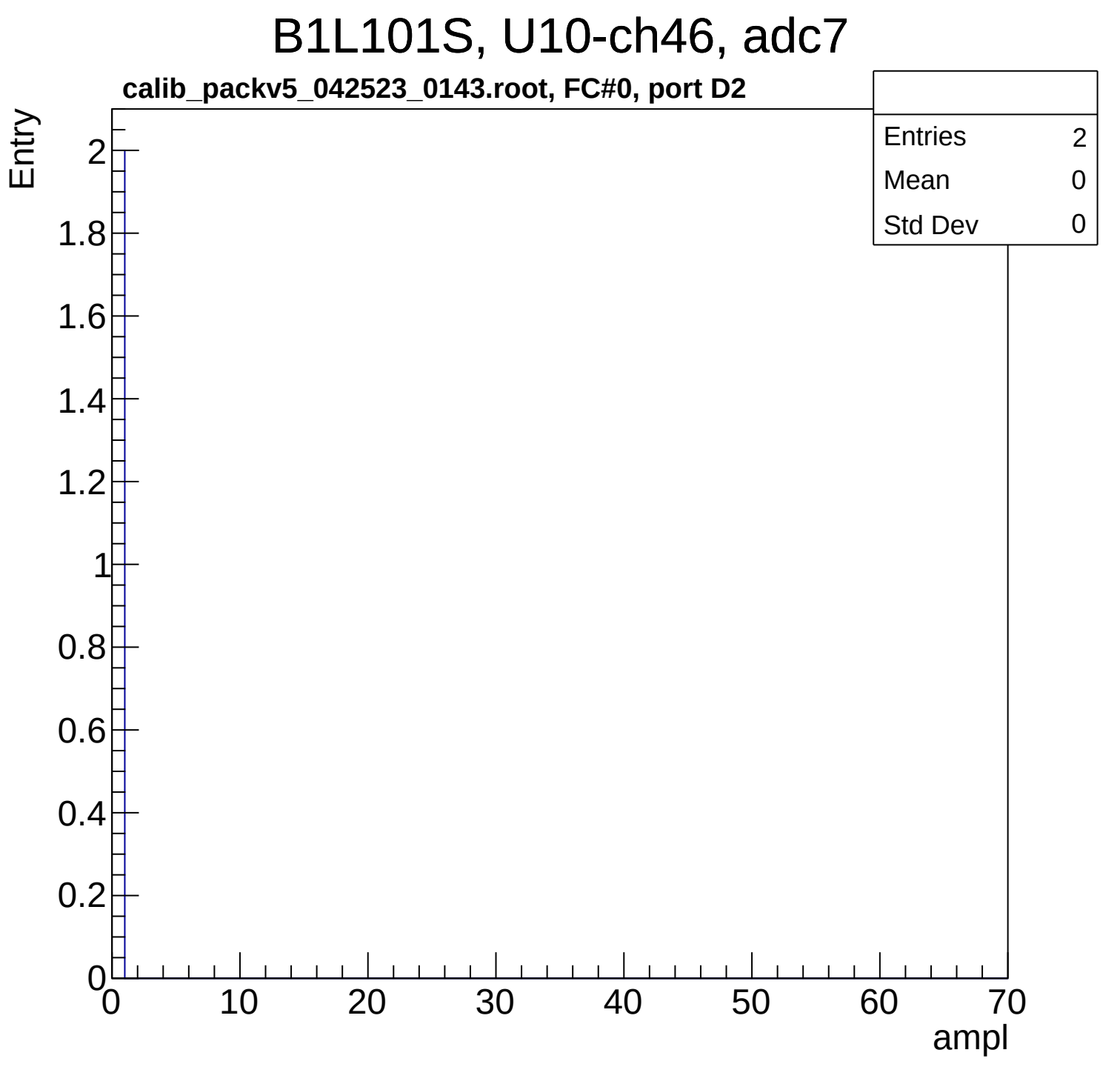
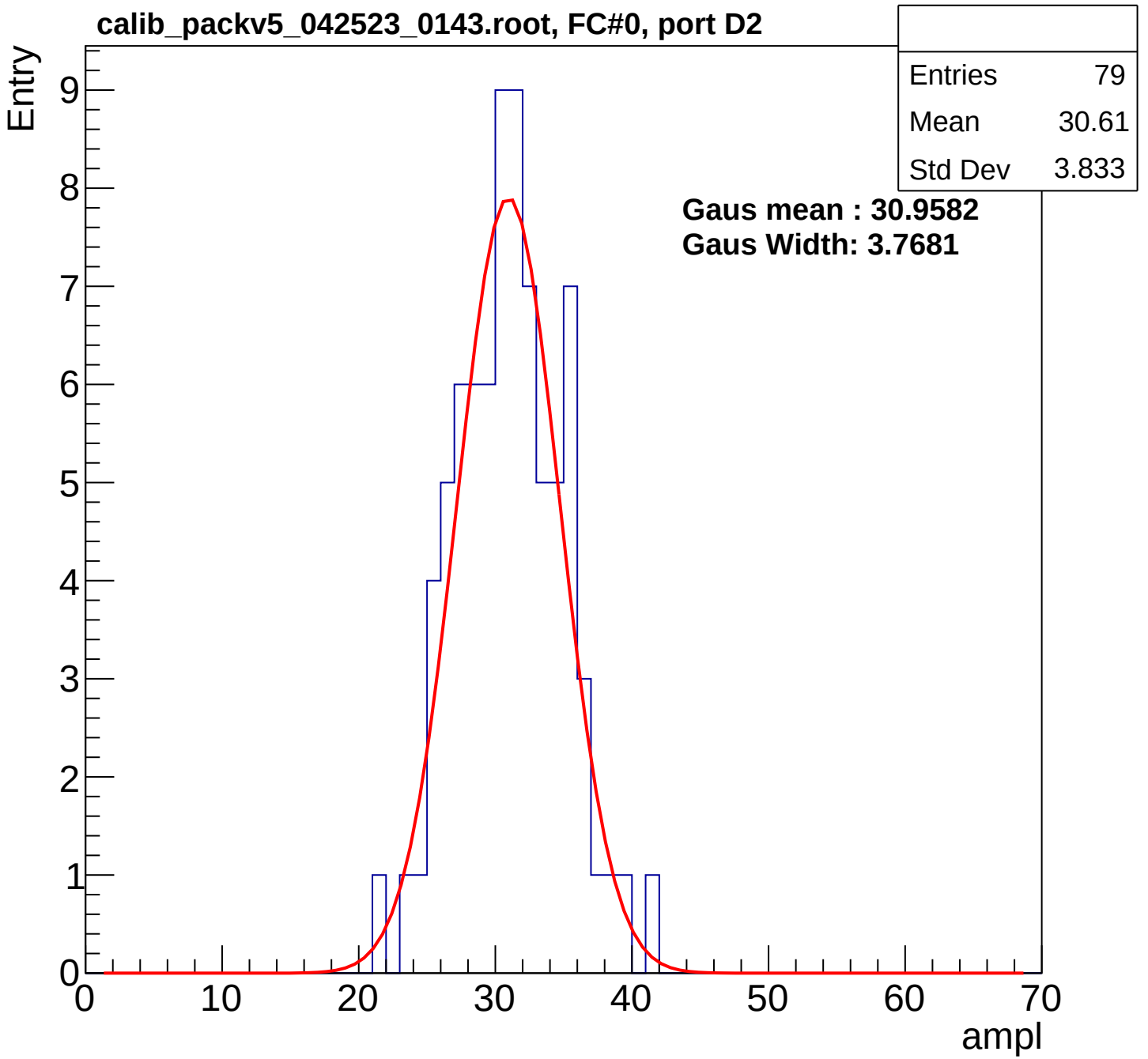

B1L101S, U10-ch46, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch47, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 30.61
Std Dev 3.833
Gaus mean : 30.9582
Gaus Width: 3.7681
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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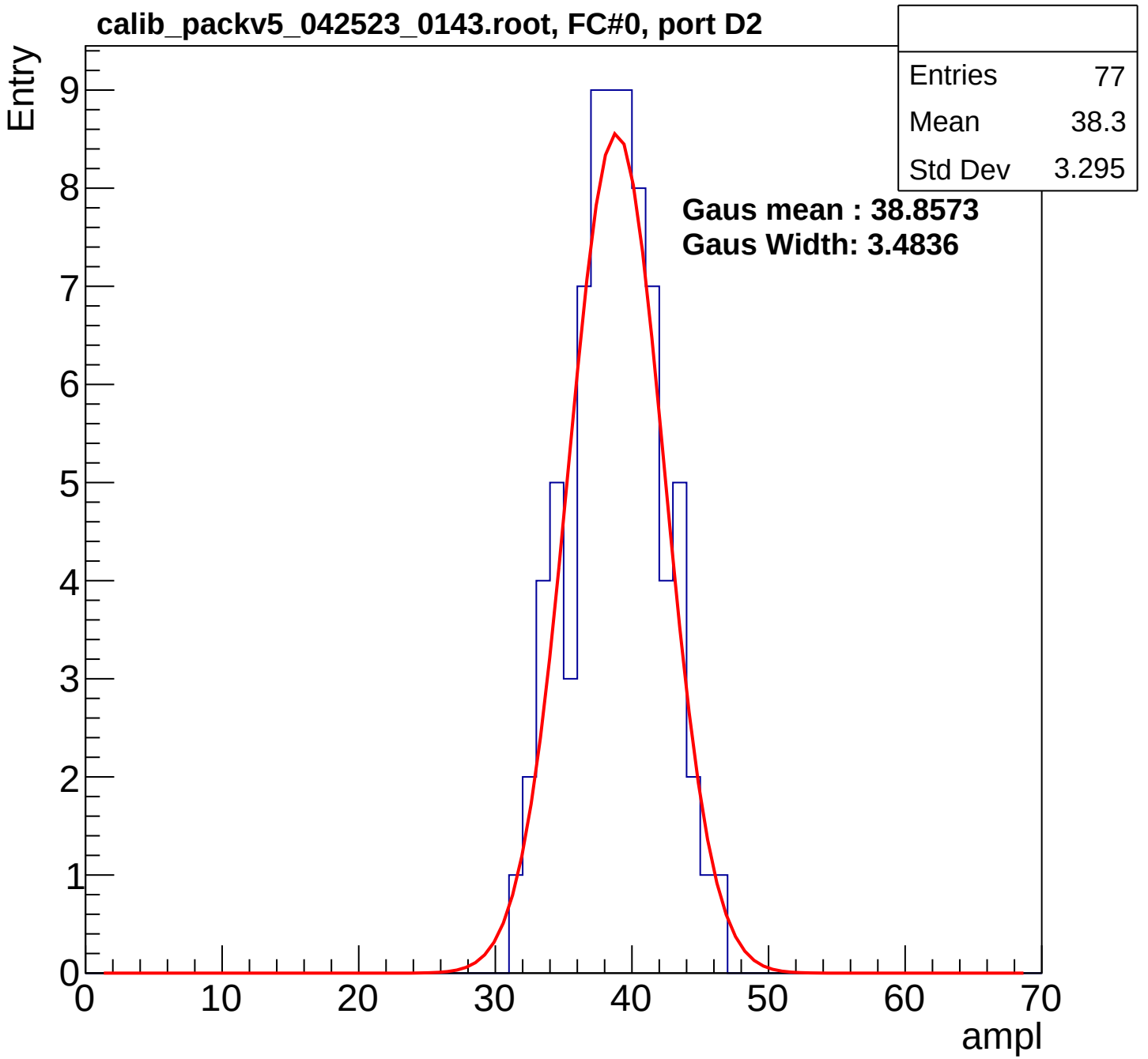
B1L101S, U10-ch47, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 38.3
Std Dev 3.295
Gaus mean : 38.8573
Gaus Width: 3.4836
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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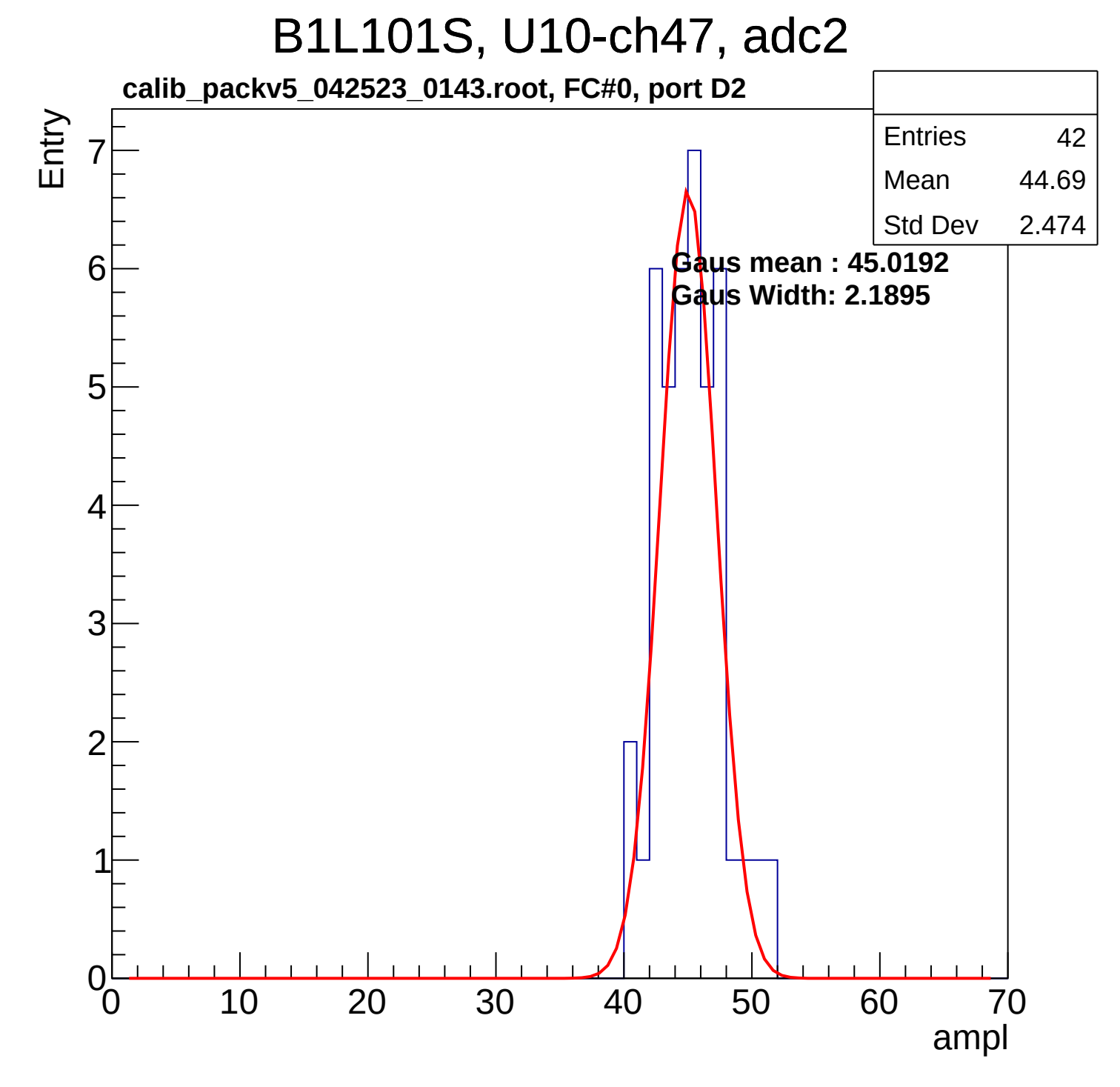
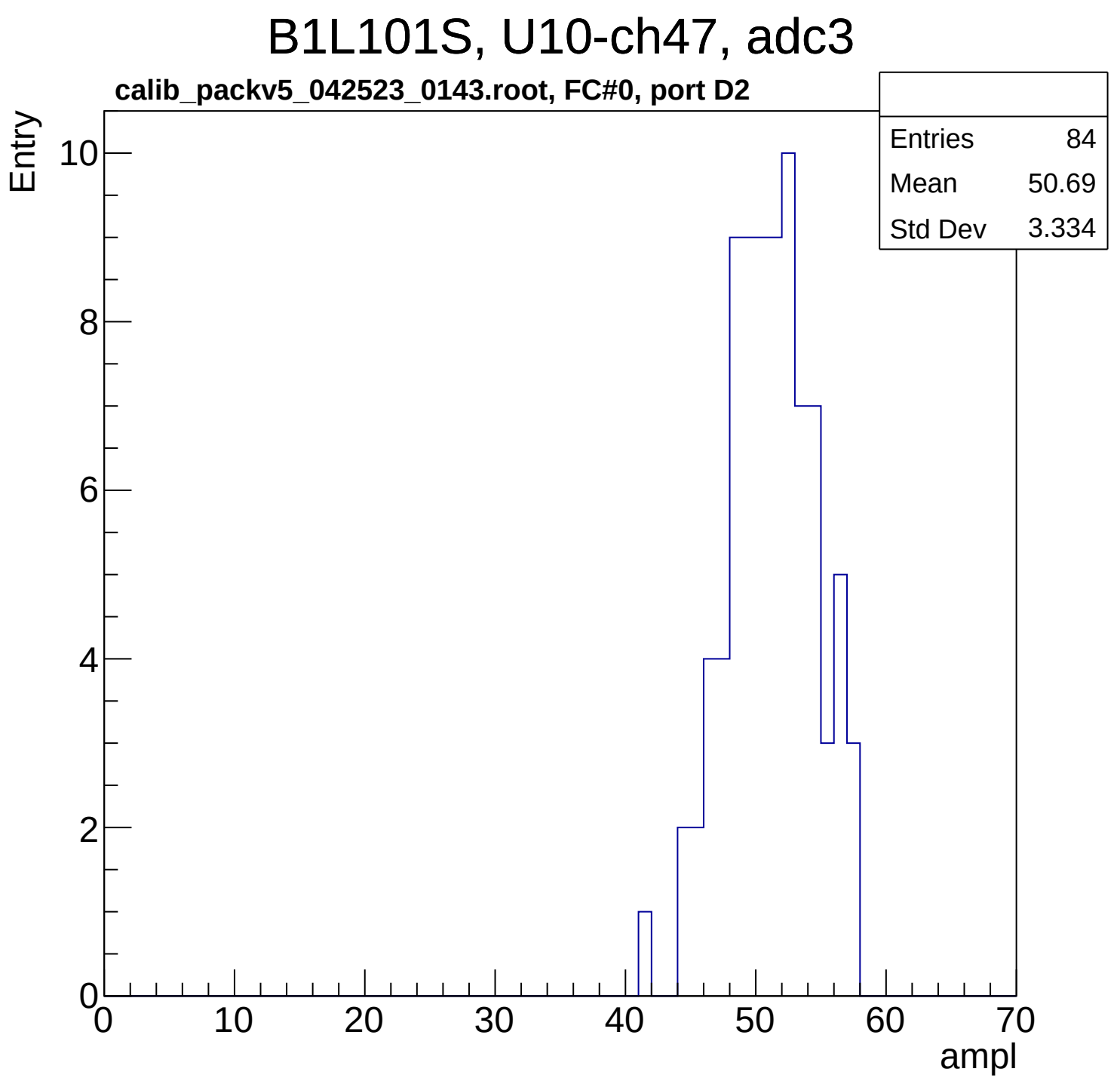
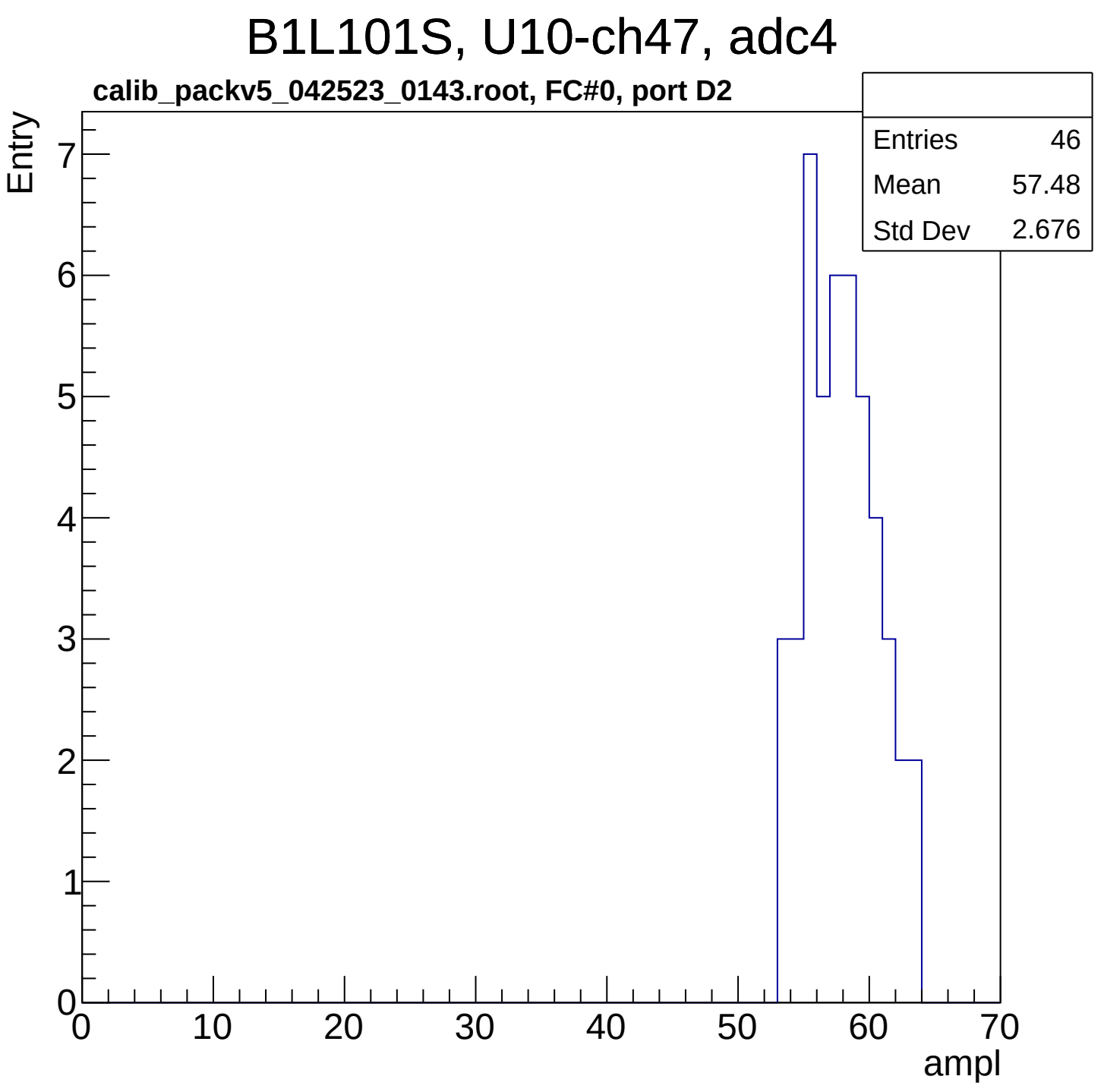
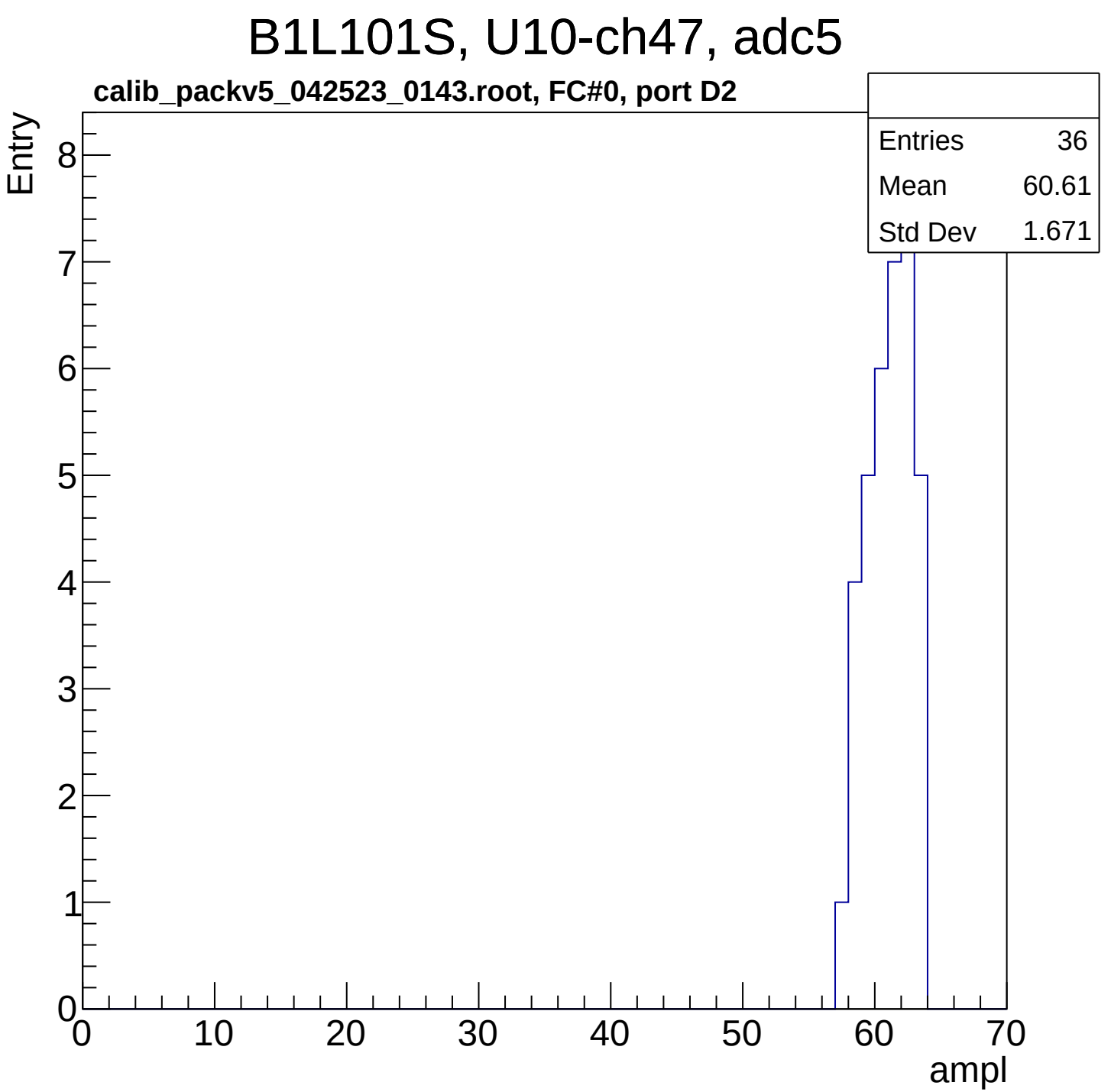

B1L101S, U10-ch47, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 44.69
Std Dev 2.474
Gaus mean : 45.0192
Gaus Width: 2.1895
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U10-ch47, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 84
Mean 50.69
Std Dev 3.334
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch47, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 57.48
Std Dev 2.676
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch47, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 36
Mean 60.61
Std Dev 1.671
Entry
ampl
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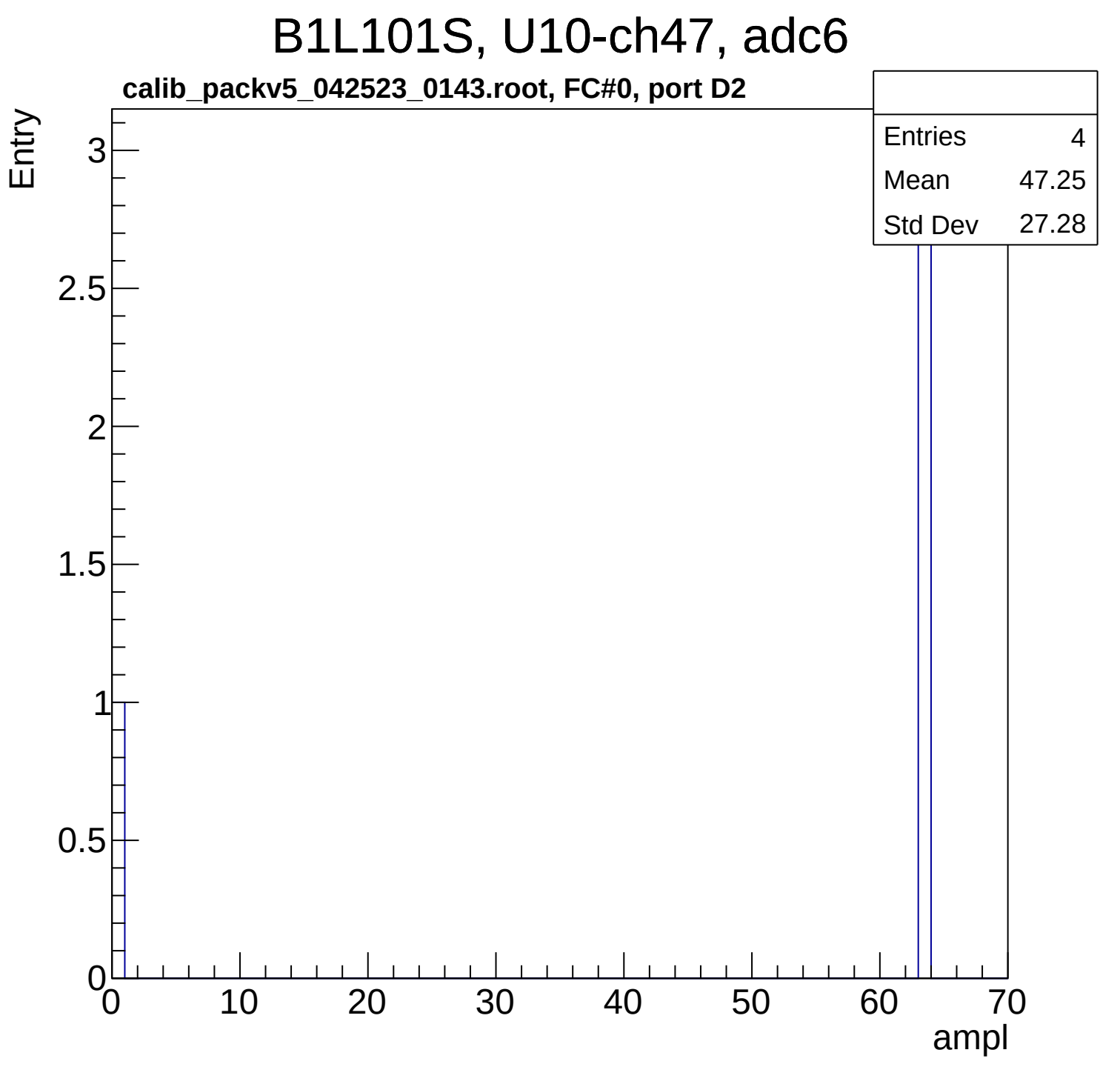
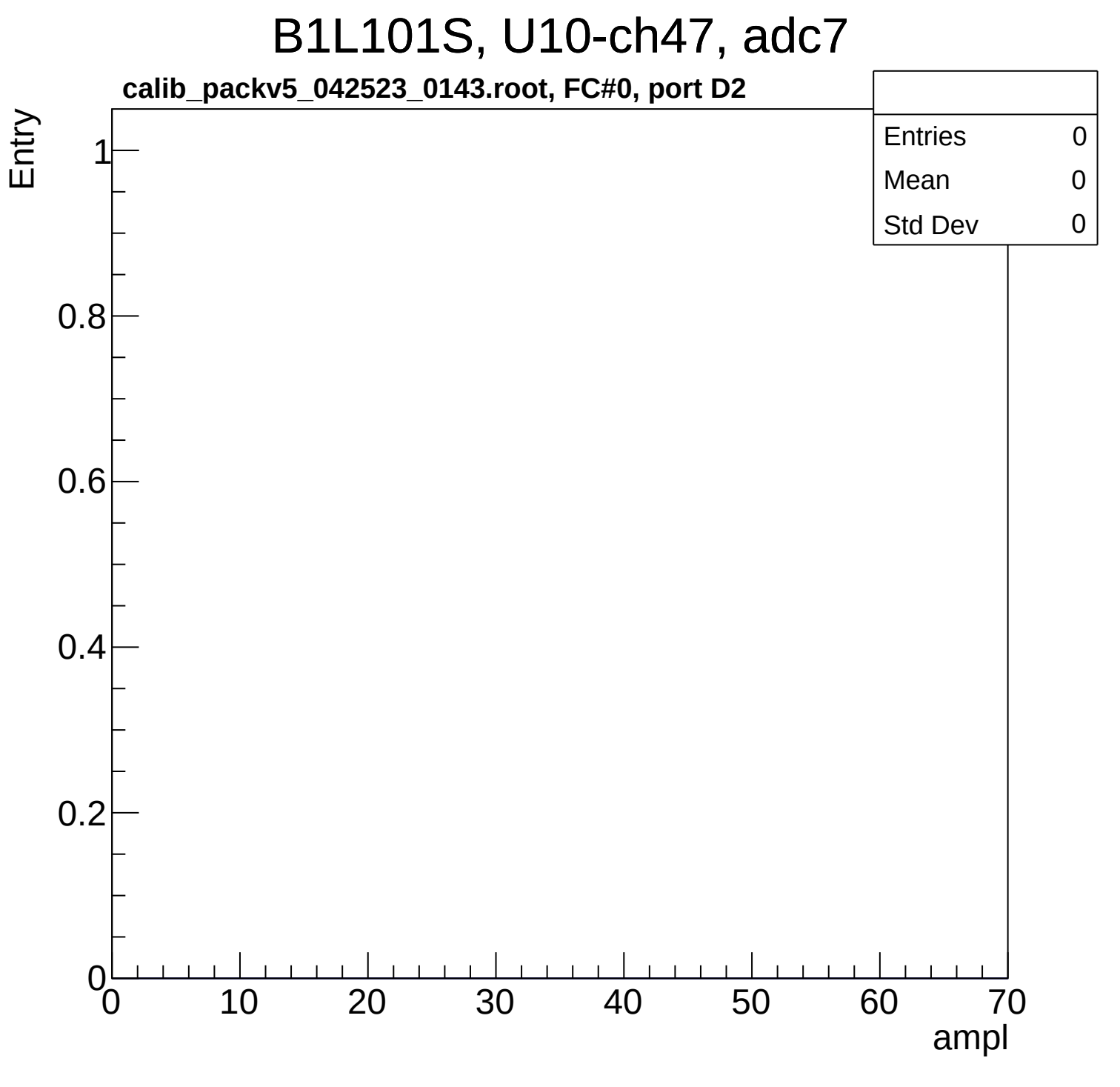
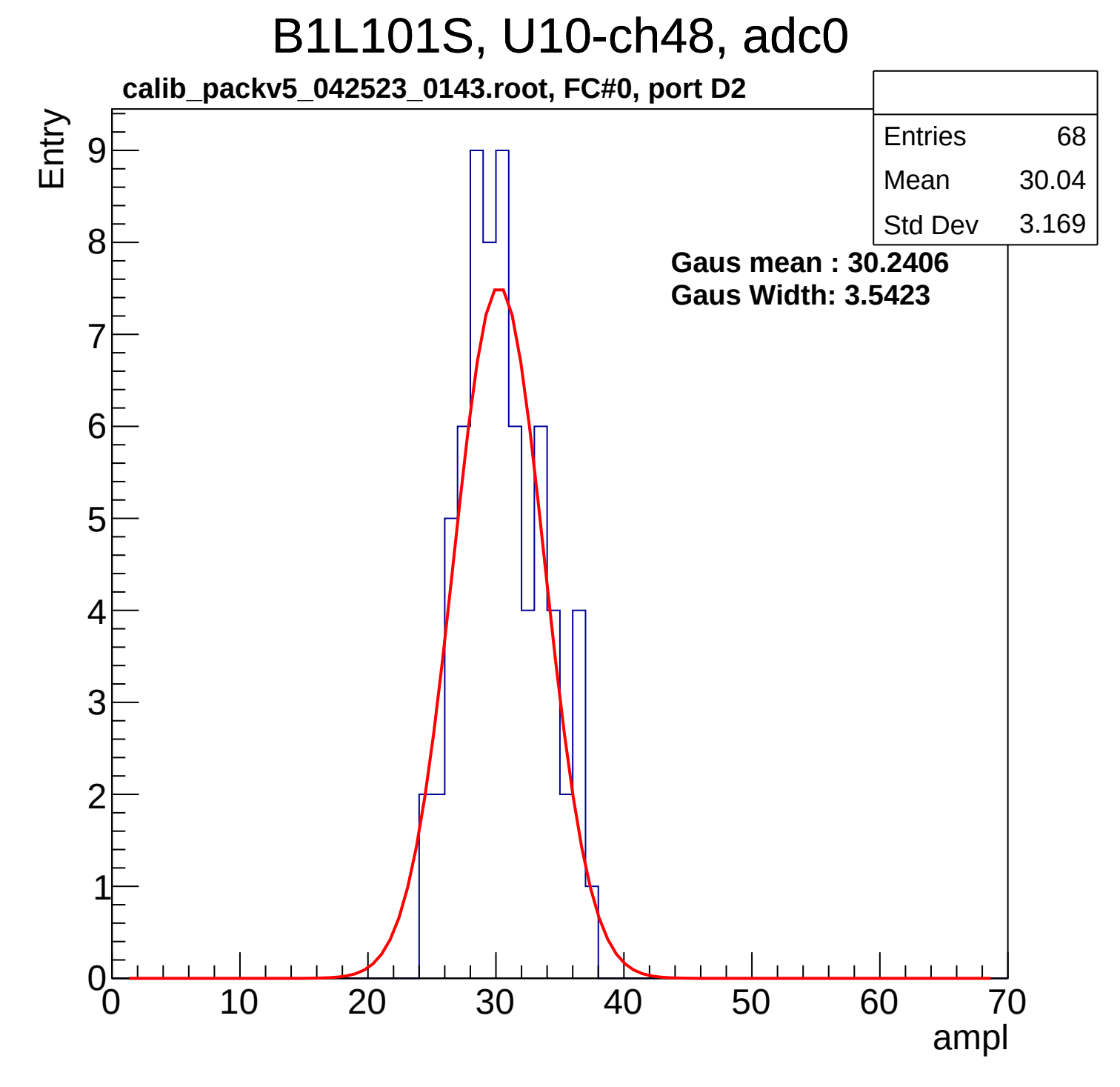
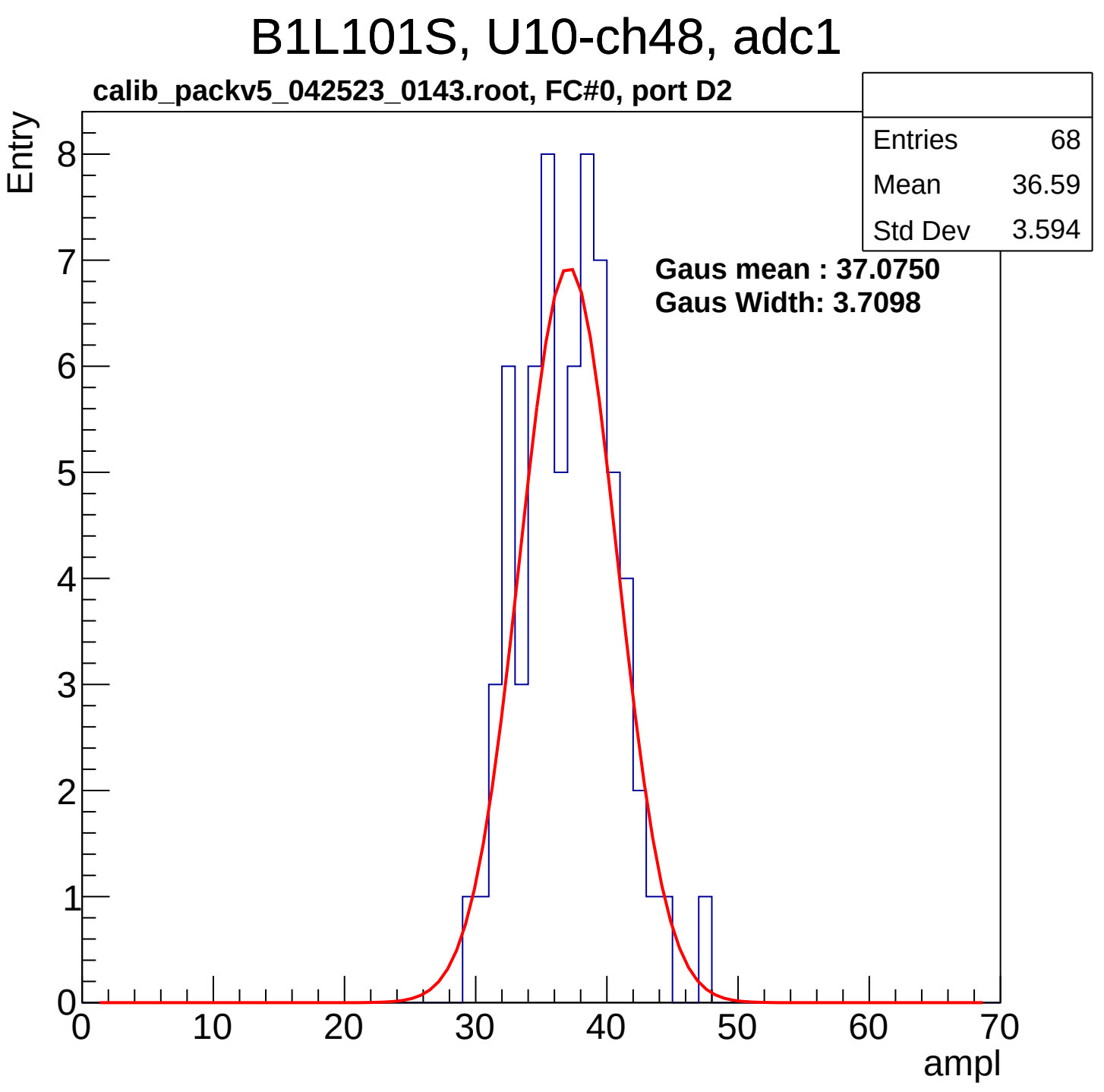
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch47, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 47.25
Std Dev 27.28
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch47, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch48, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 30.04
Std Dev 3.169
Gaus mean : 30.2406
Gaus Width: 3.5423
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch48, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 36.59
Std Dev 3.594
Gaus mean : 37.0750
Gaus Width: 3.7098
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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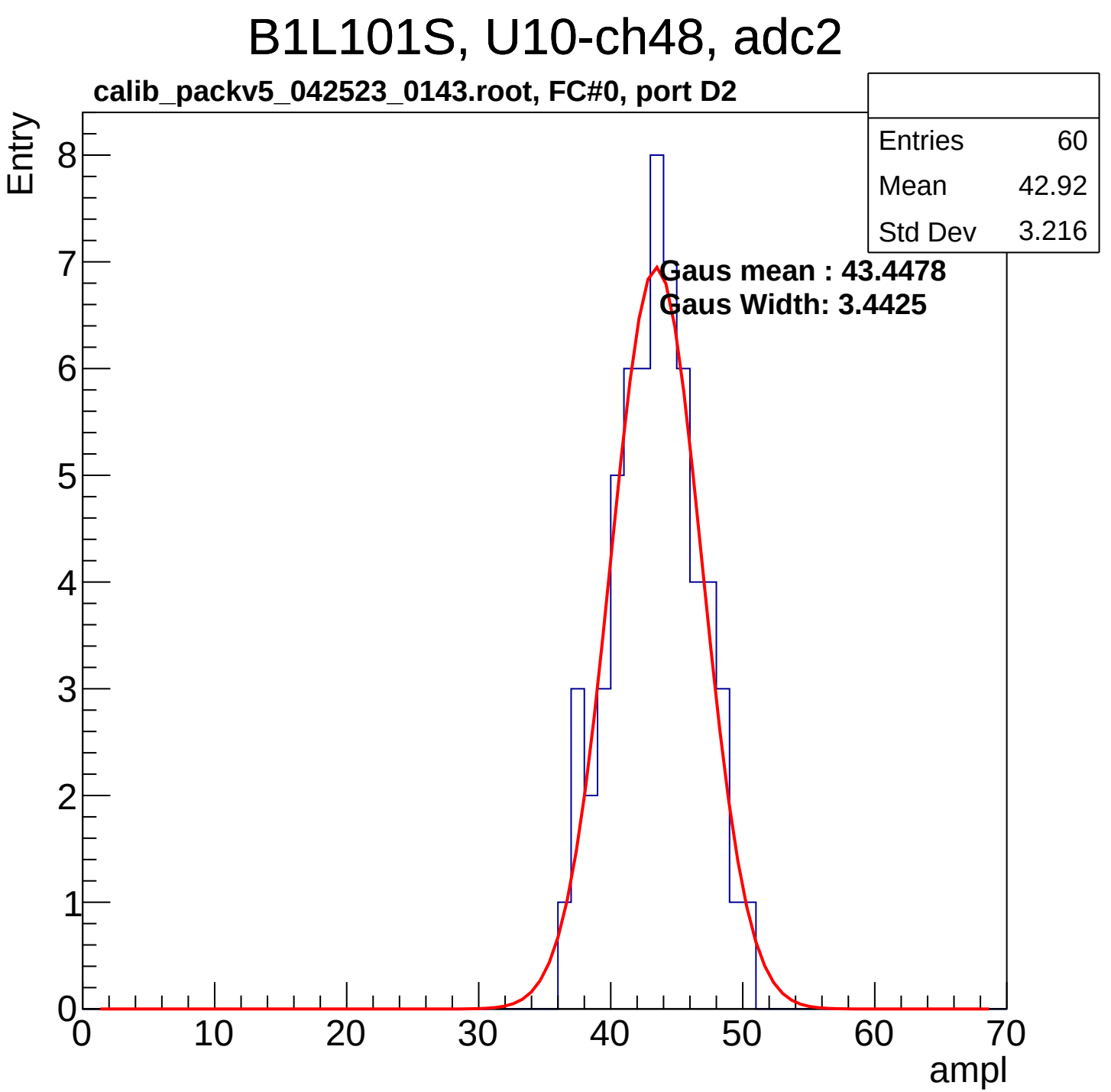
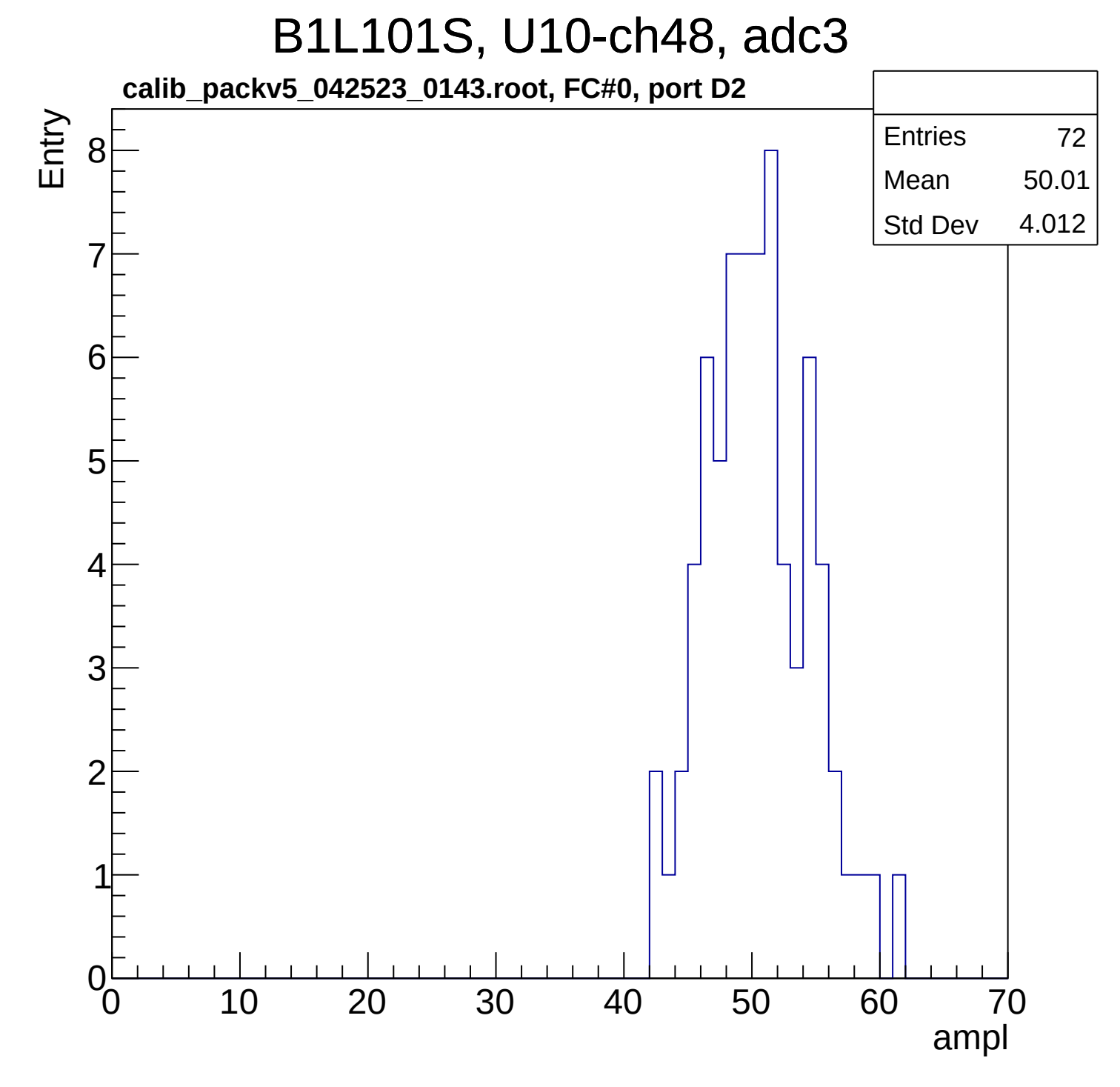

B1L101S, U10-ch48, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 42.92
Std Dev 3.216
Gaus mean : 43.4478
Gaus Width: 3.4425
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch48, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 50.01
Std Dev 4.012
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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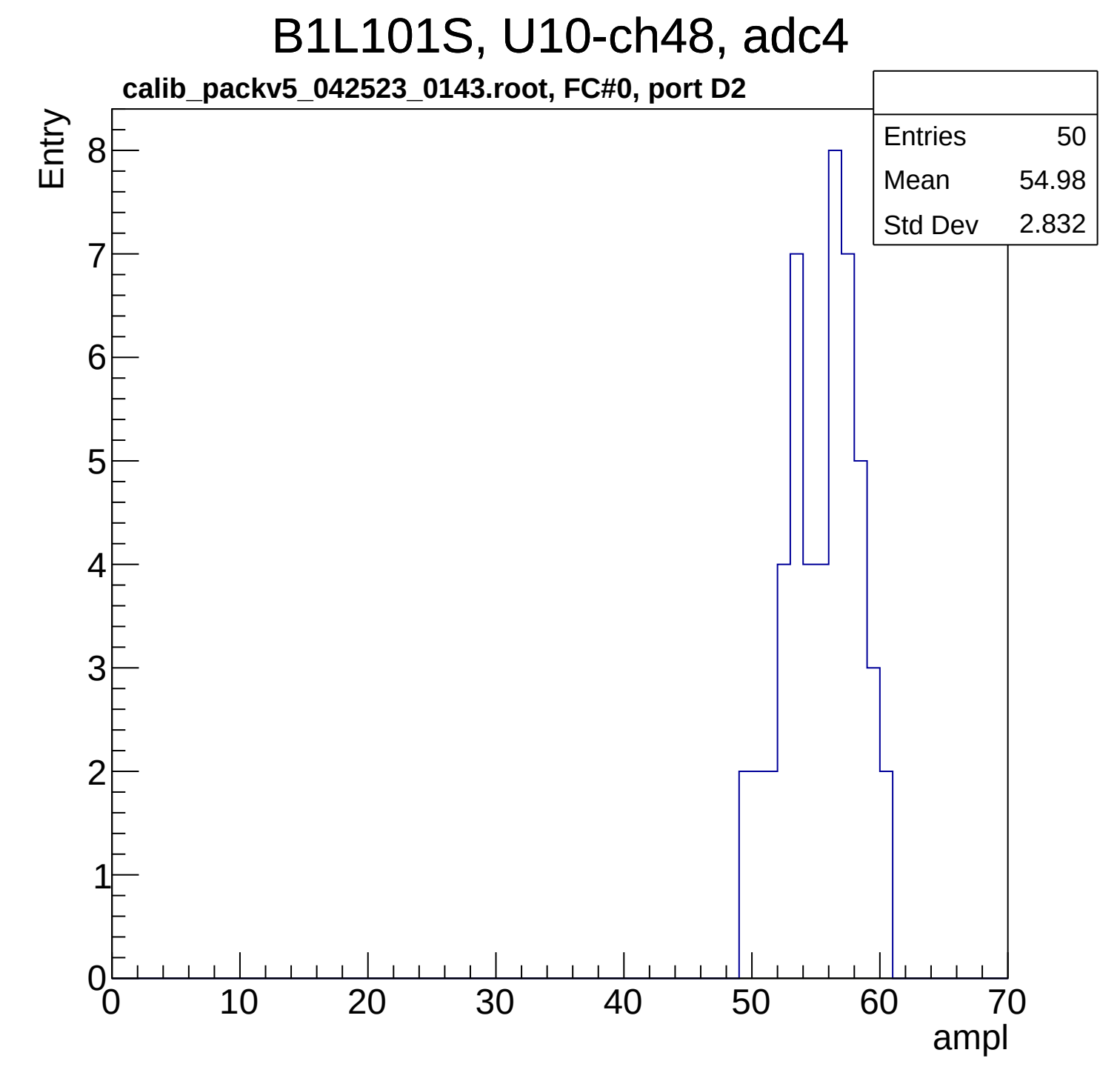
B1L101S, U10-ch48, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 54.98
Std Dev 2.832
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
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60
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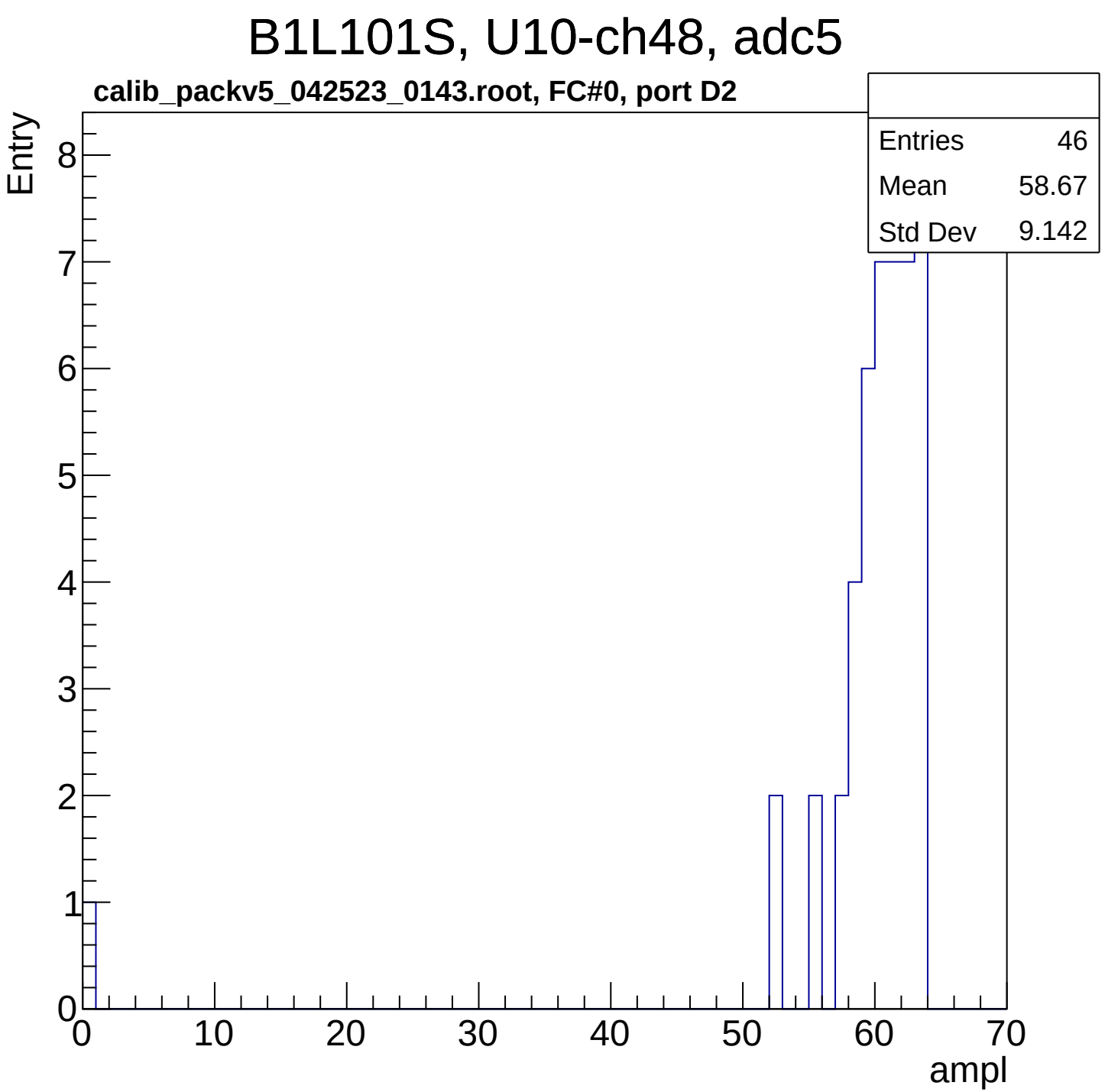
B1L101S, U10-ch48, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 58.67
Std Dev 9.142
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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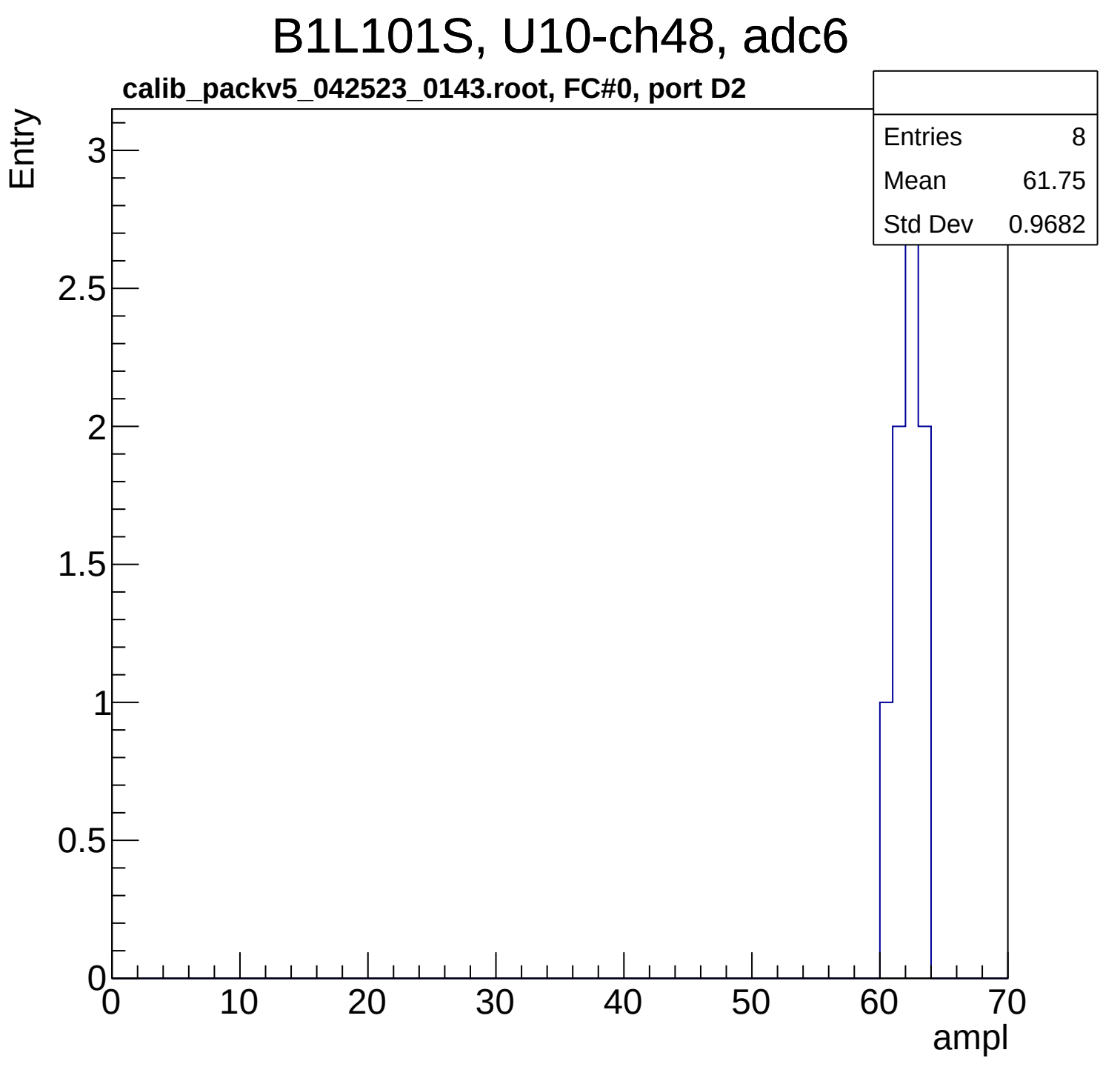
B1L101S, U10-ch48, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 61.75
Std Dev 0.9682
Entry
ampl
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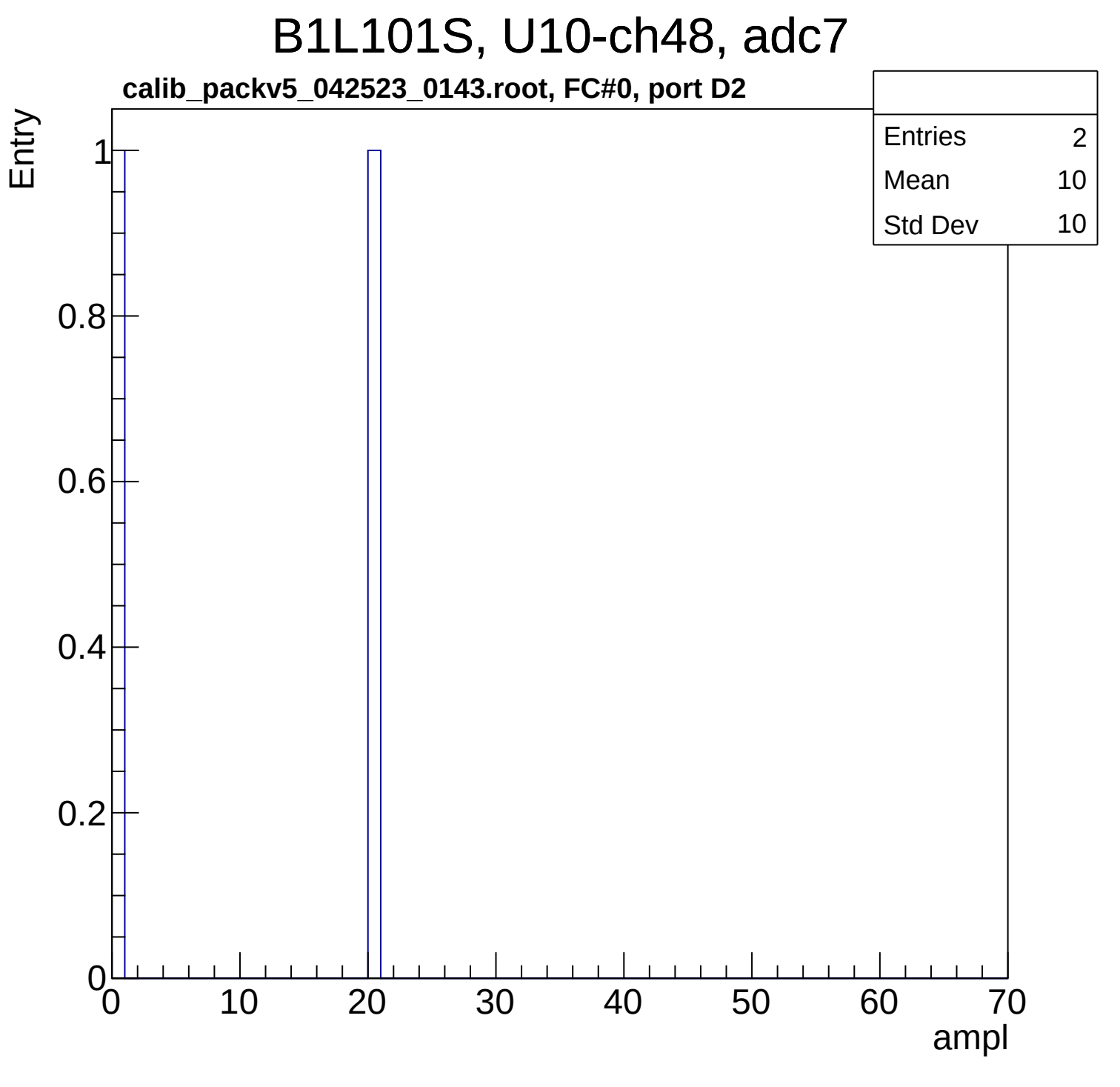
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U10-ch48, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 10
Std Dev 10
Entry
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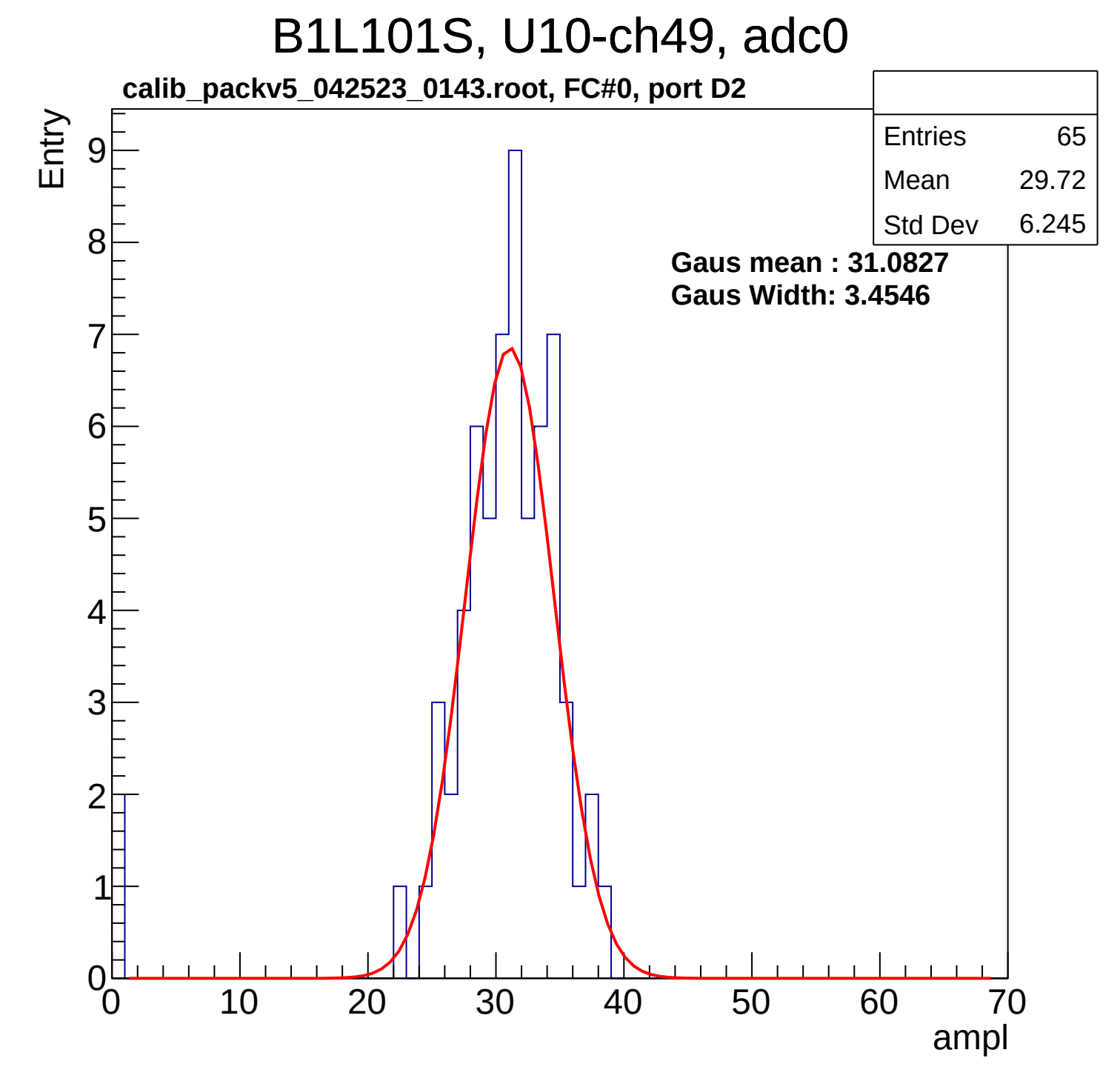
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch49, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 29.72
Std Dev 6.245
Gaus mean : 31.0827
Gaus Width: 3.4546
Entry
ampl
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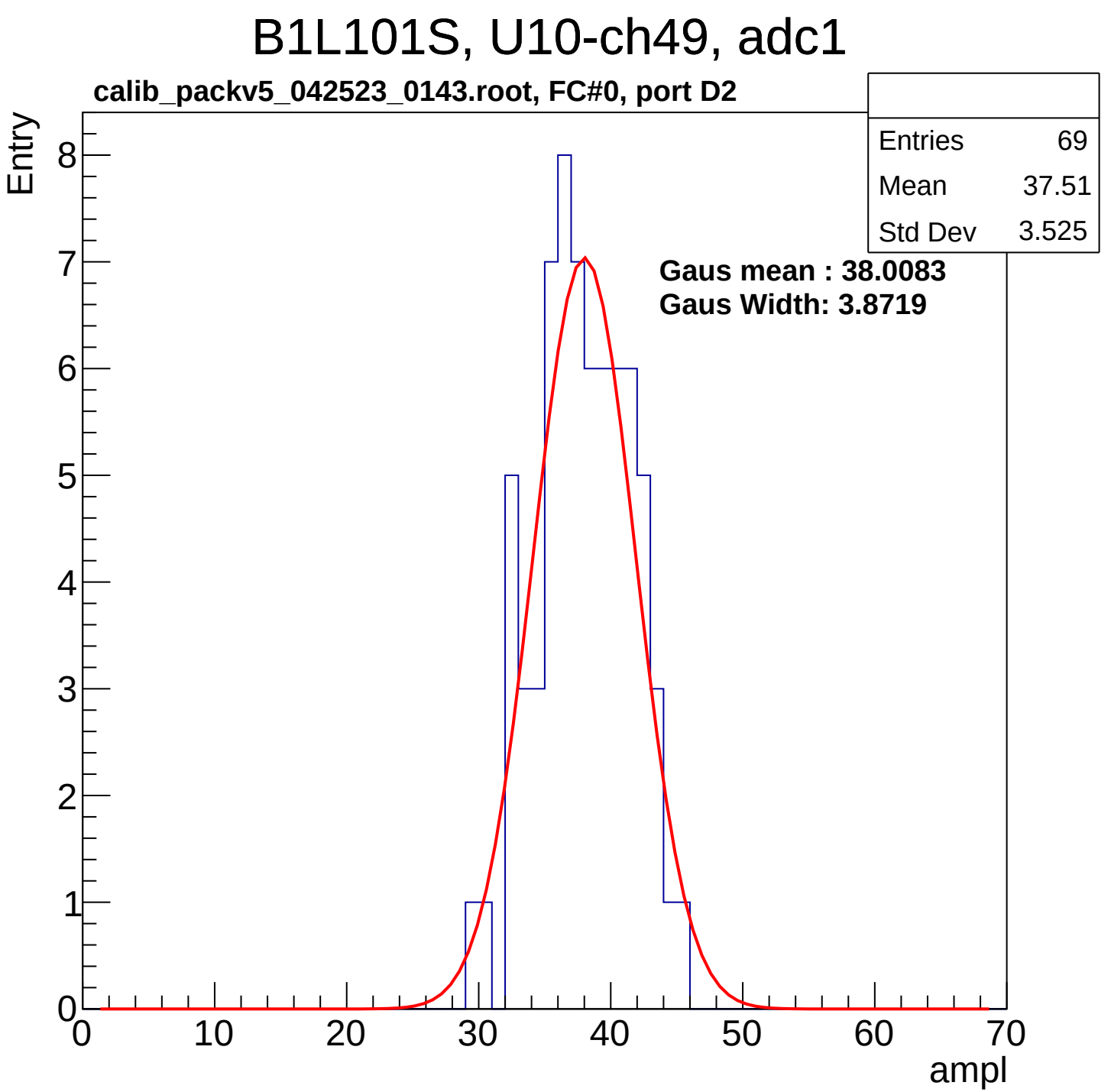
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch49, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 37.51
Std Dev 3.525
Gaus mean : 38.0083
Gaus Width: 3.8719
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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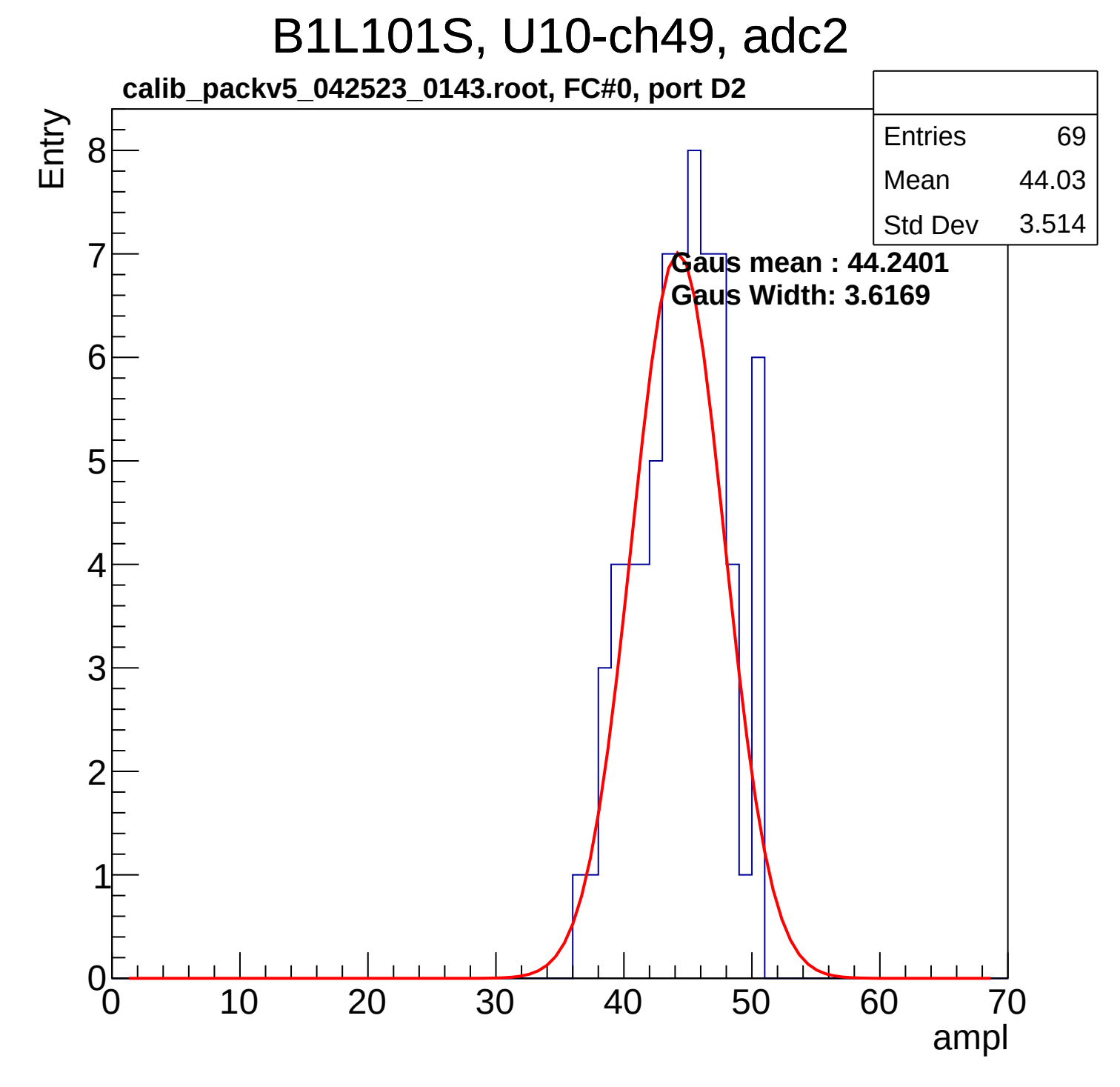
B1L101S, U10-ch49, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 44.03
Std Dev 3.514
Gaus mean : 44.2401
Gaus Width: 3.6169
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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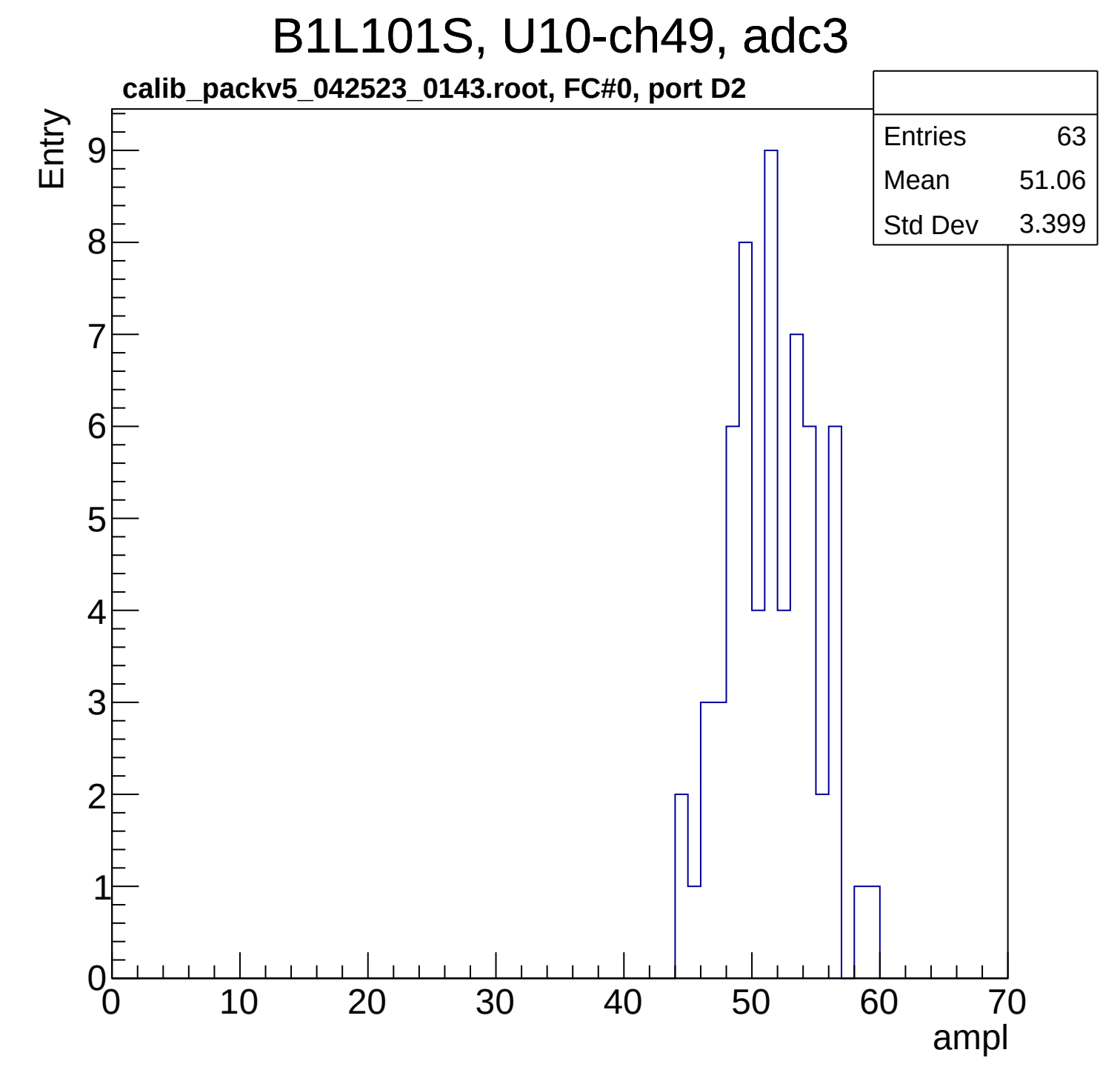
B1L101S, U10-ch49, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 51.06
Std Dev 3.399
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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60
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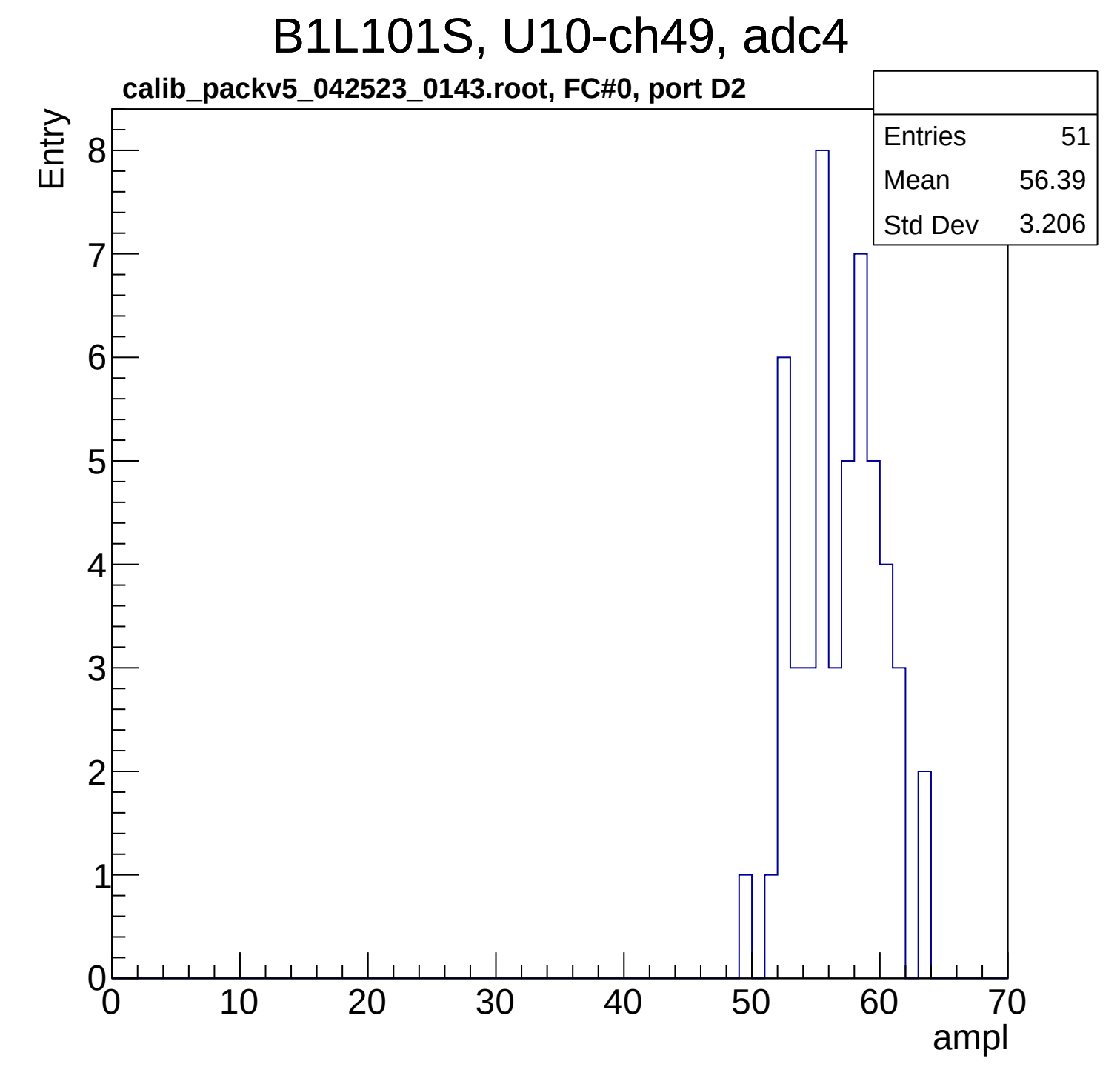
B1L101S, U10-ch49, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 56.39
Std Dev 3.206
Entry
ampl
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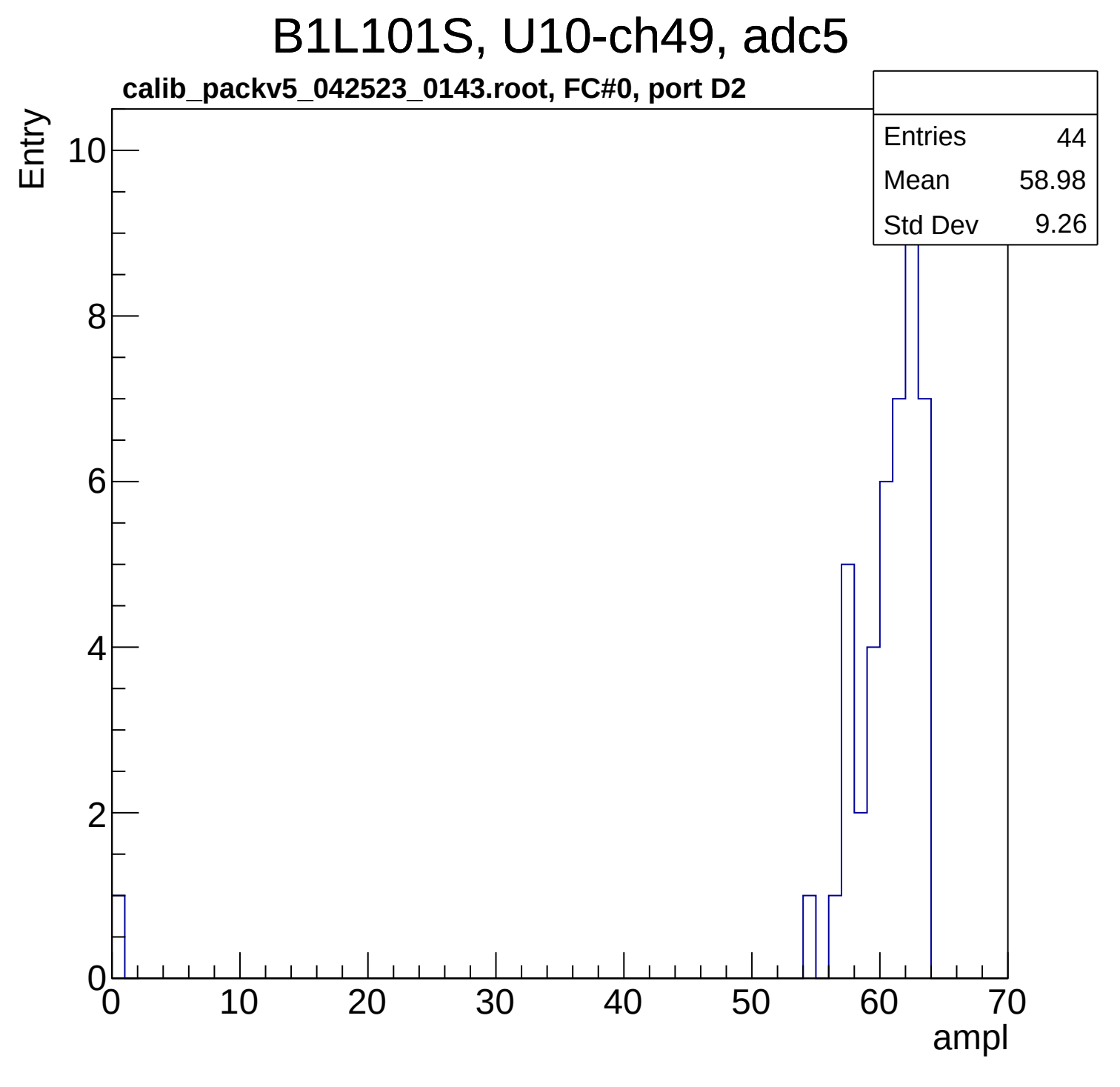
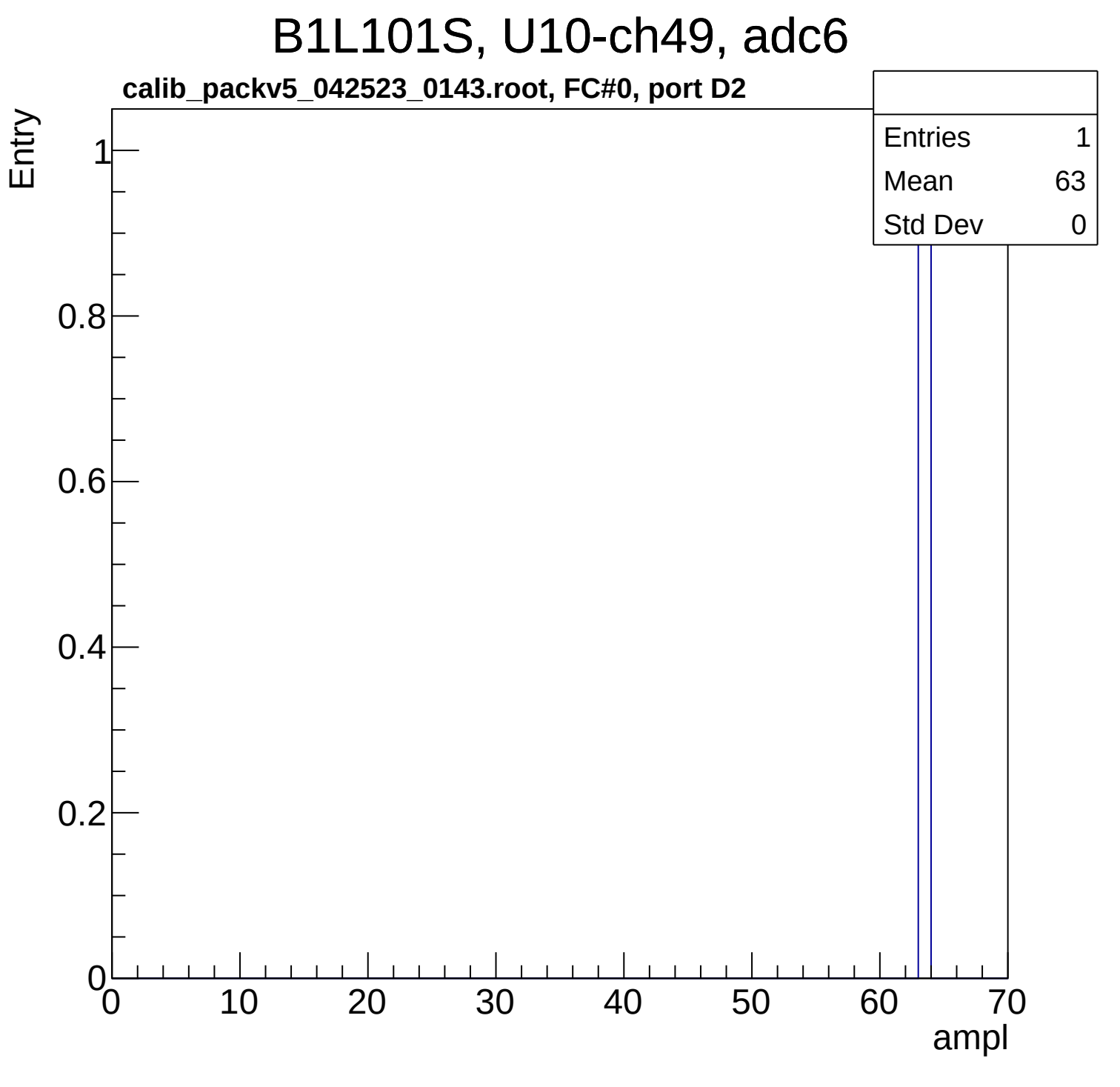
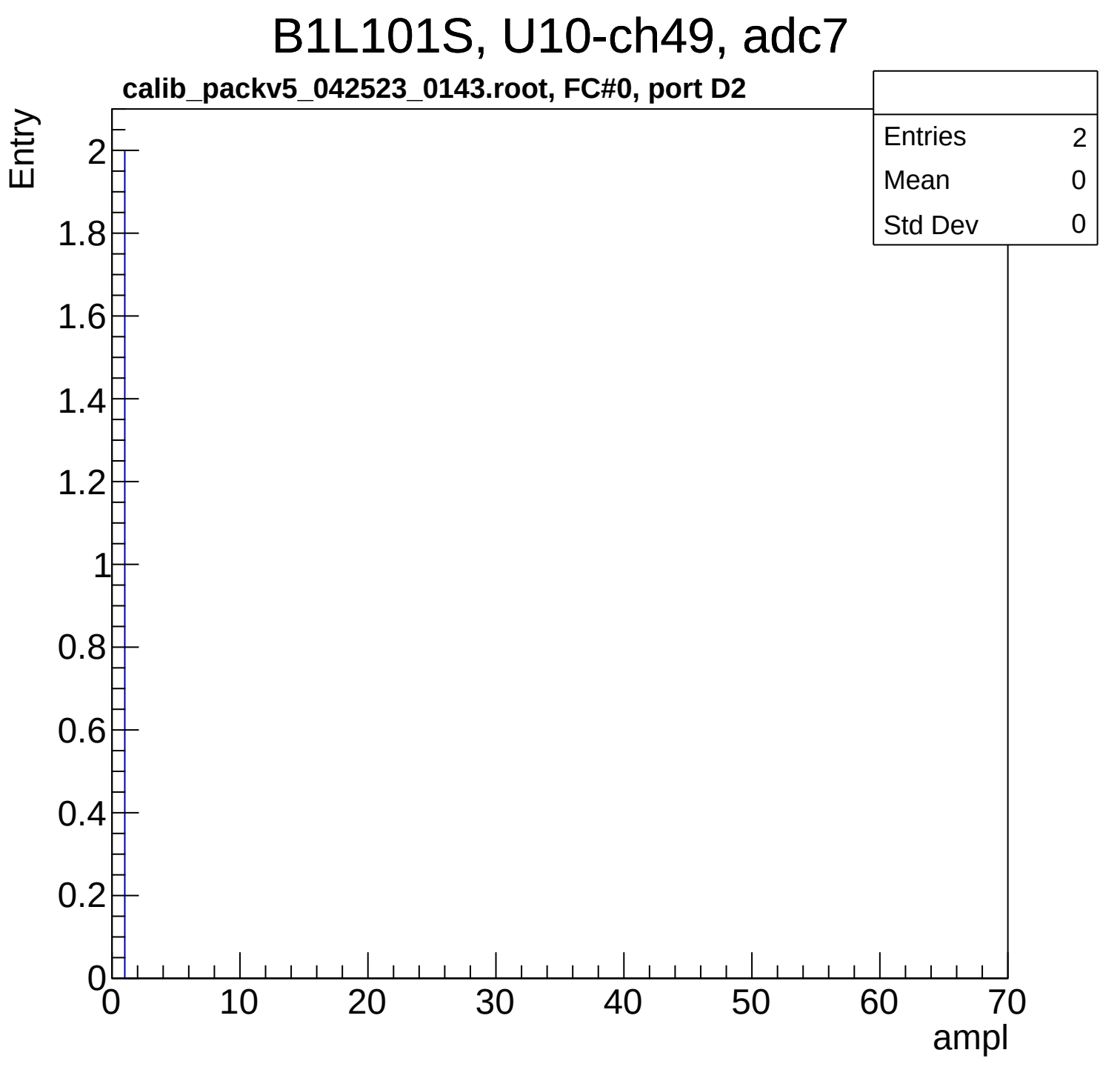
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch49, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 44
Mean 58.98
Std Dev 9.26
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch49, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch49, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
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60
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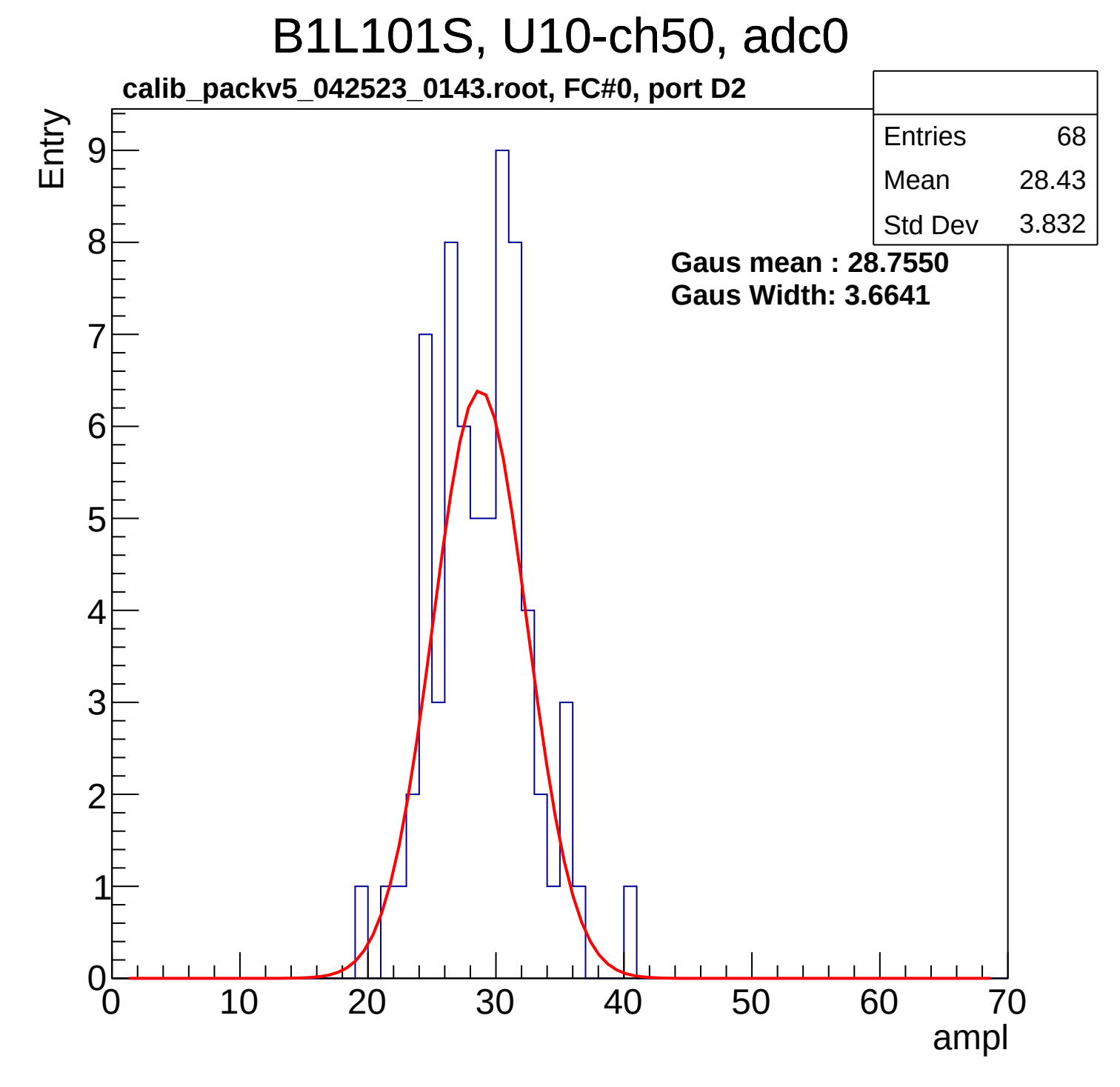
B1L101S, U10-ch50, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 28.43
Std Dev 3.832
Gaus mean : 28.7550
Gaus Width: 3.6641
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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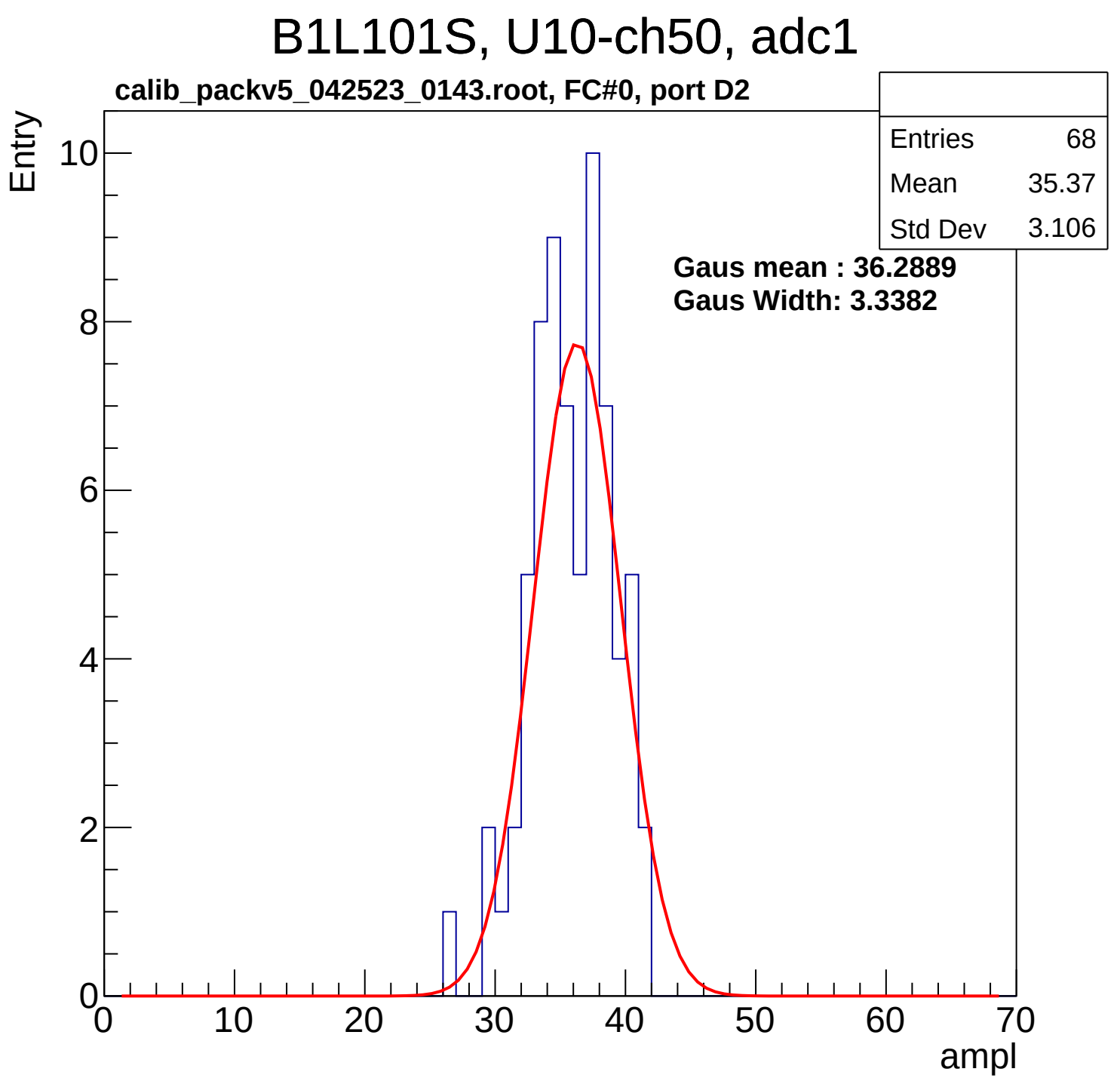
B1L101S, U10-ch50, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 35.37
Std Dev 3.106
Gaus mean : 36.2889
Gaus Width: 3.3382
Entry
ampl
0
2
4
6
8
10
0
10
20
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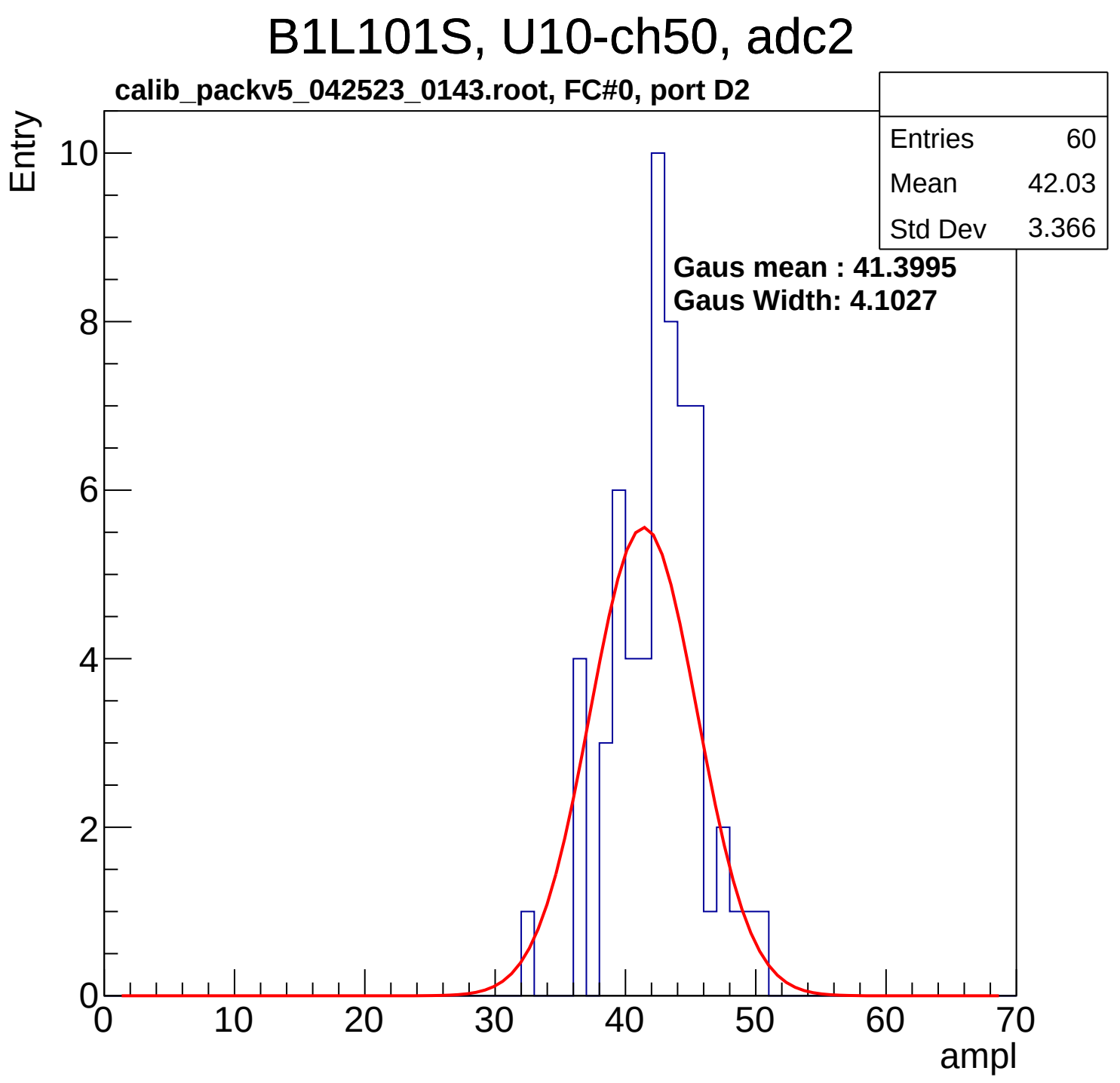
40
50
60
70


B1L101S, U10-ch50, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 42.03
Std Dev 3.366
Gaus mean : 41.3995
Gaus Width: 4.1027
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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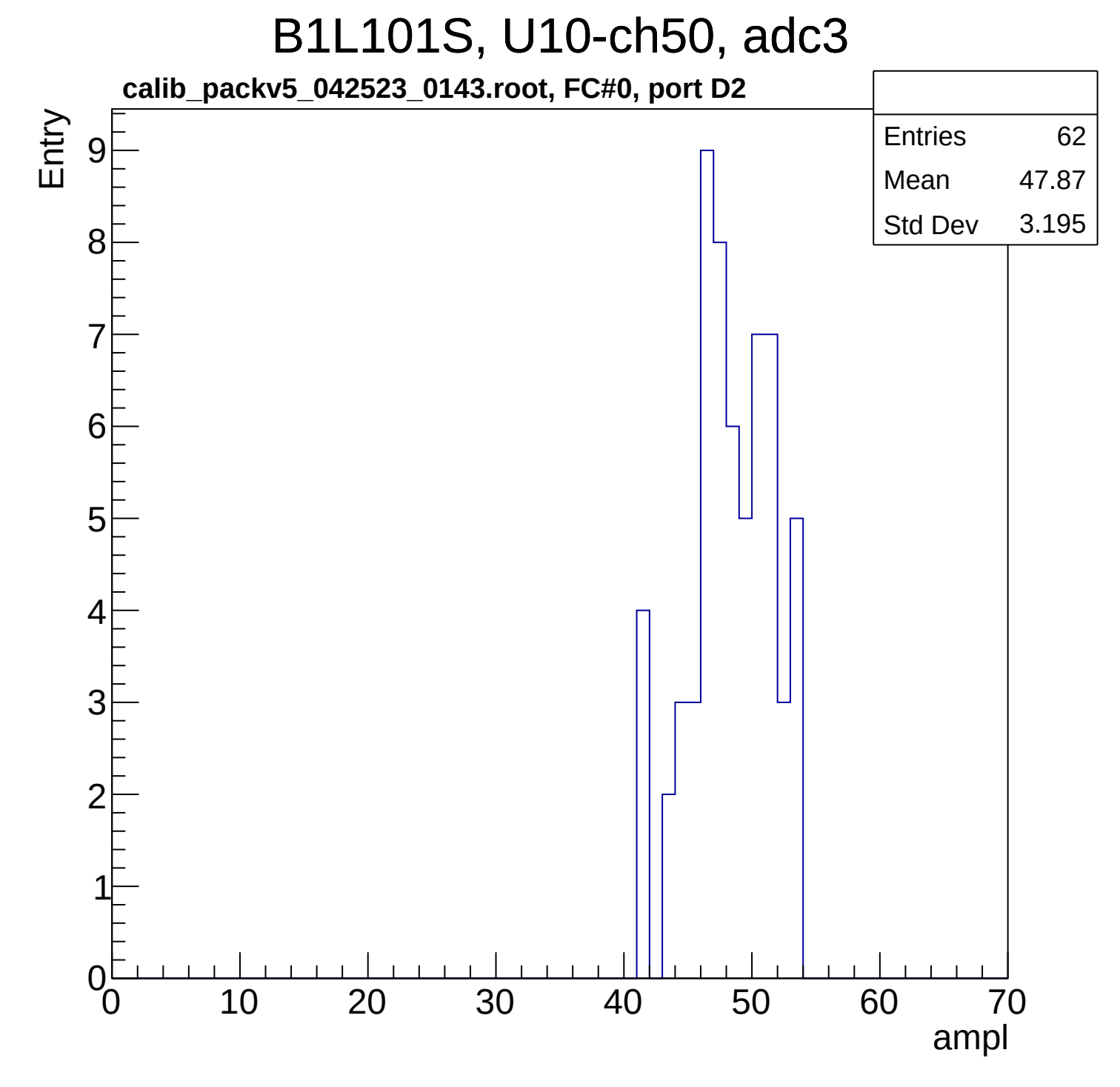
B1L101S, U10-ch50, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 47.87
Std Dev 3.195
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
30
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60
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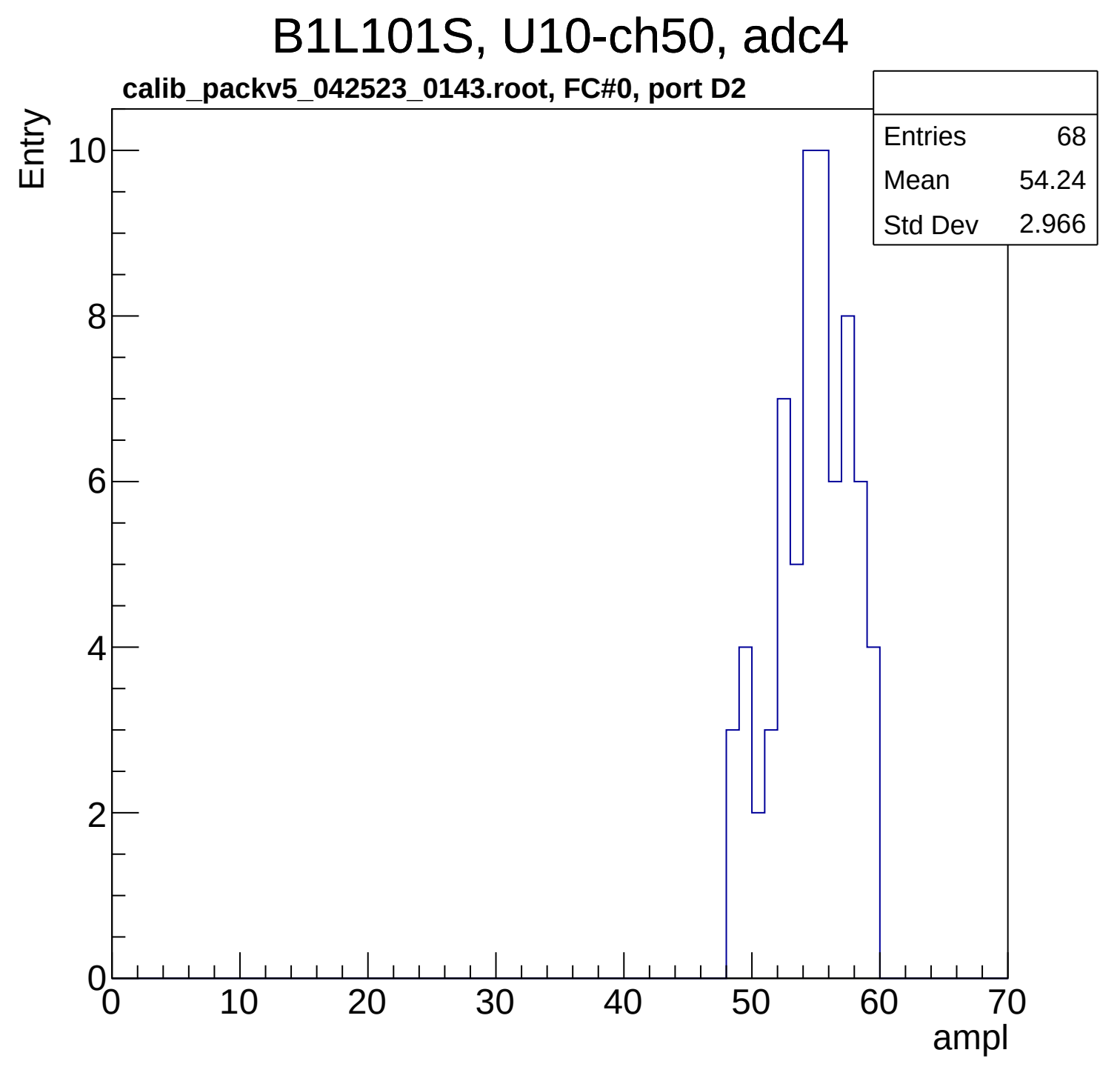
B1L101S, U10-ch50, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 54.24
Std Dev 2.966
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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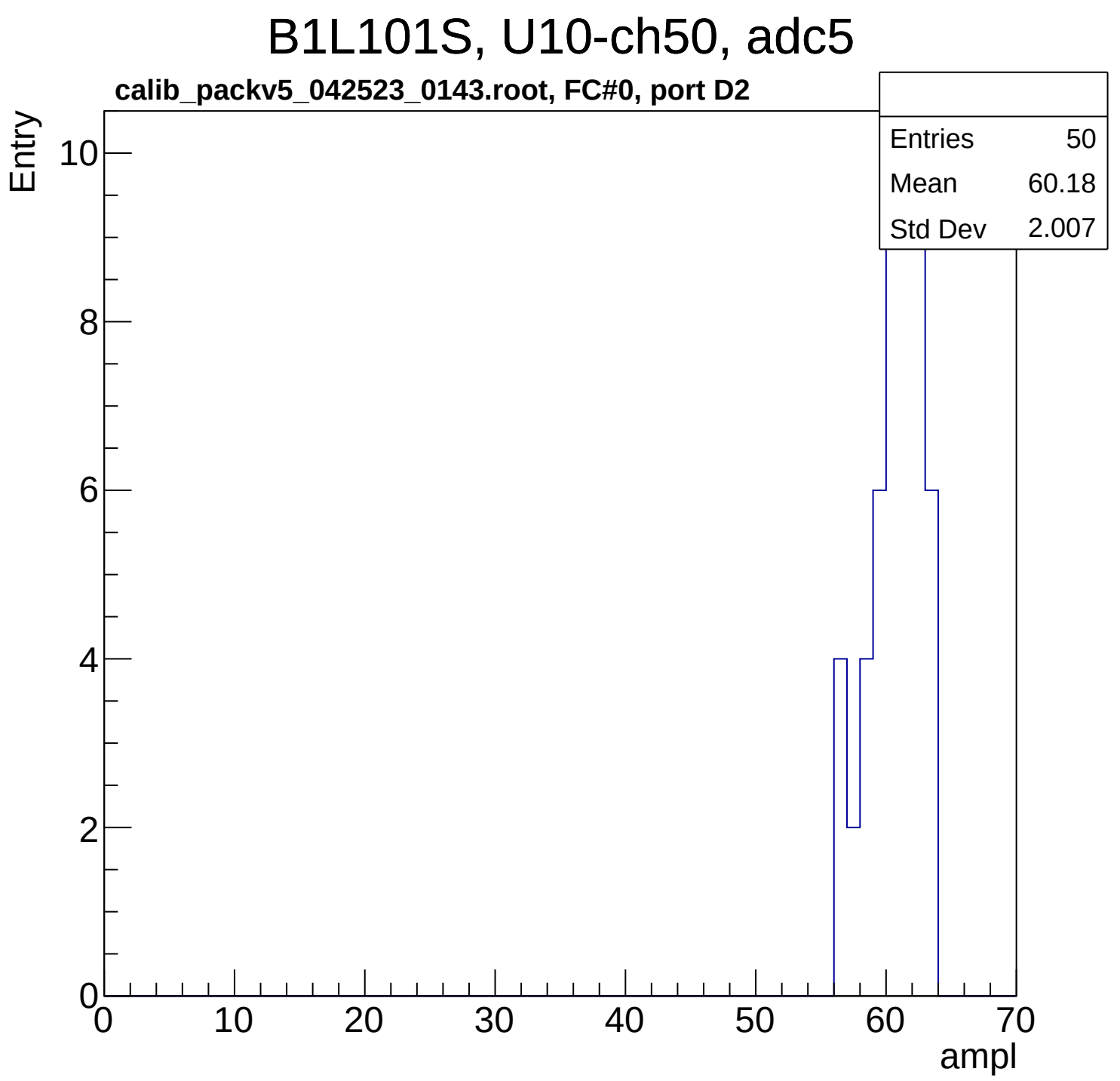
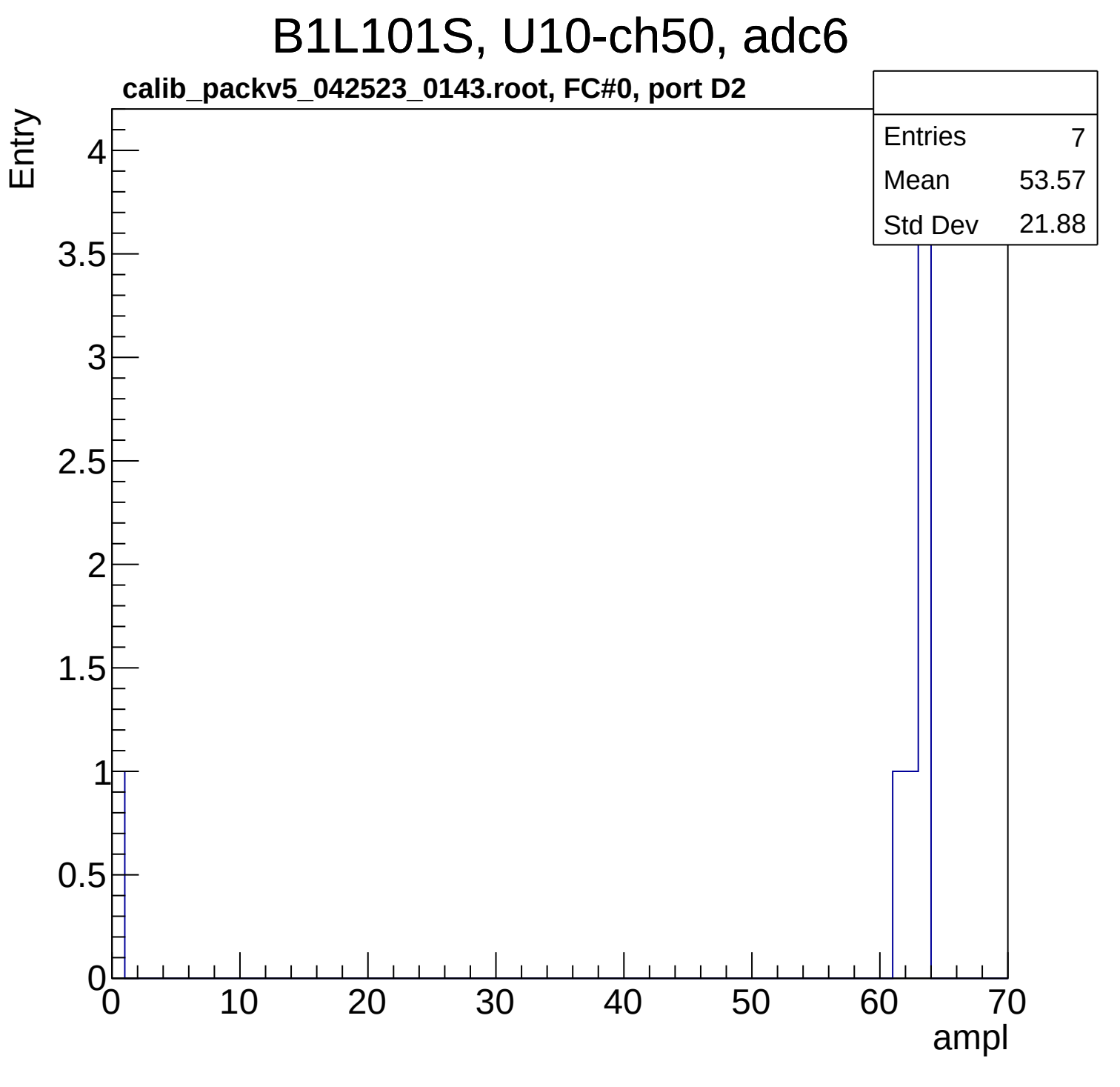

B1L101S, U10-ch50, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 60.18
Std Dev 2.007
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch50, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 53.57
Std Dev 21.88
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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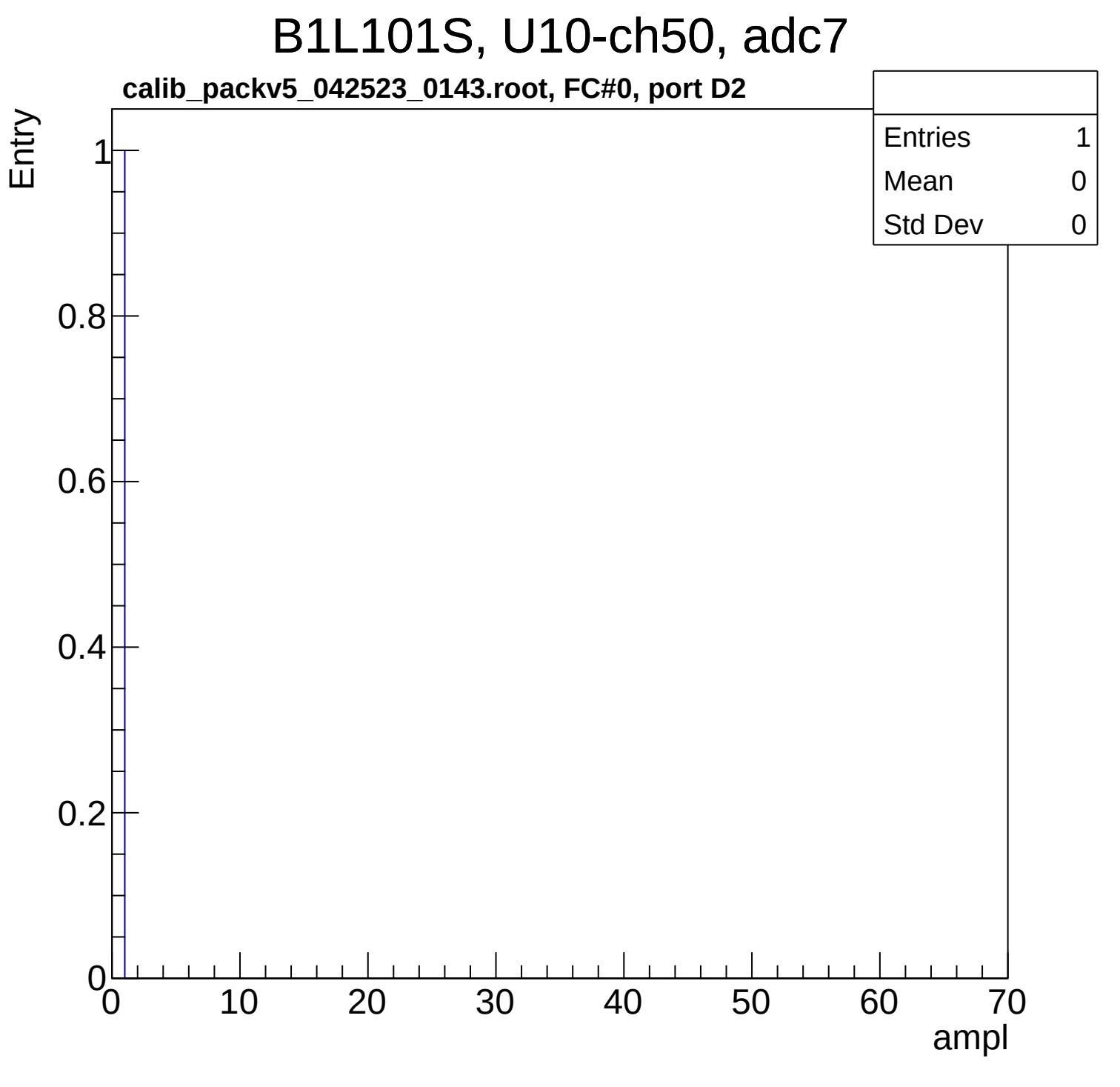
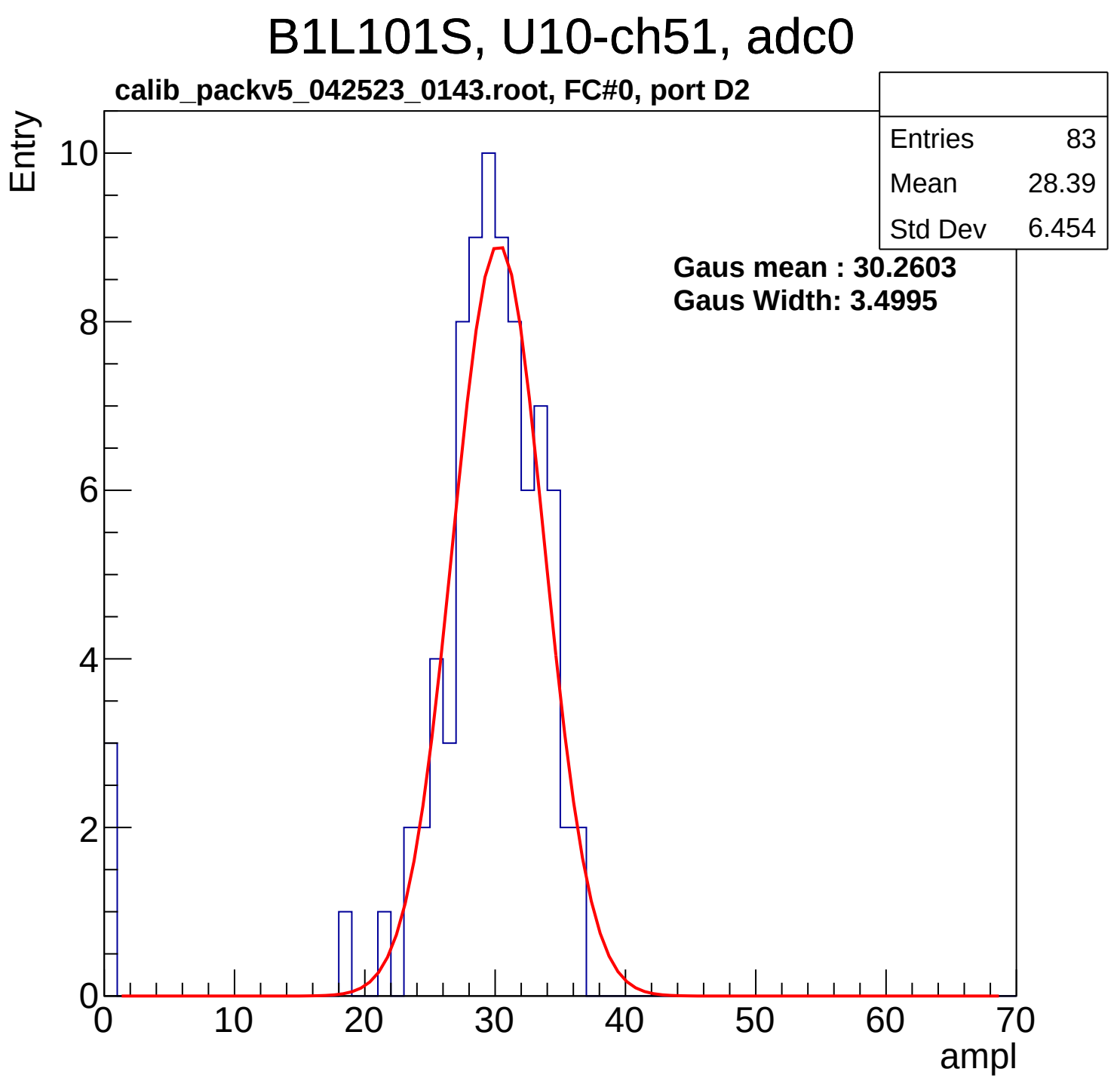
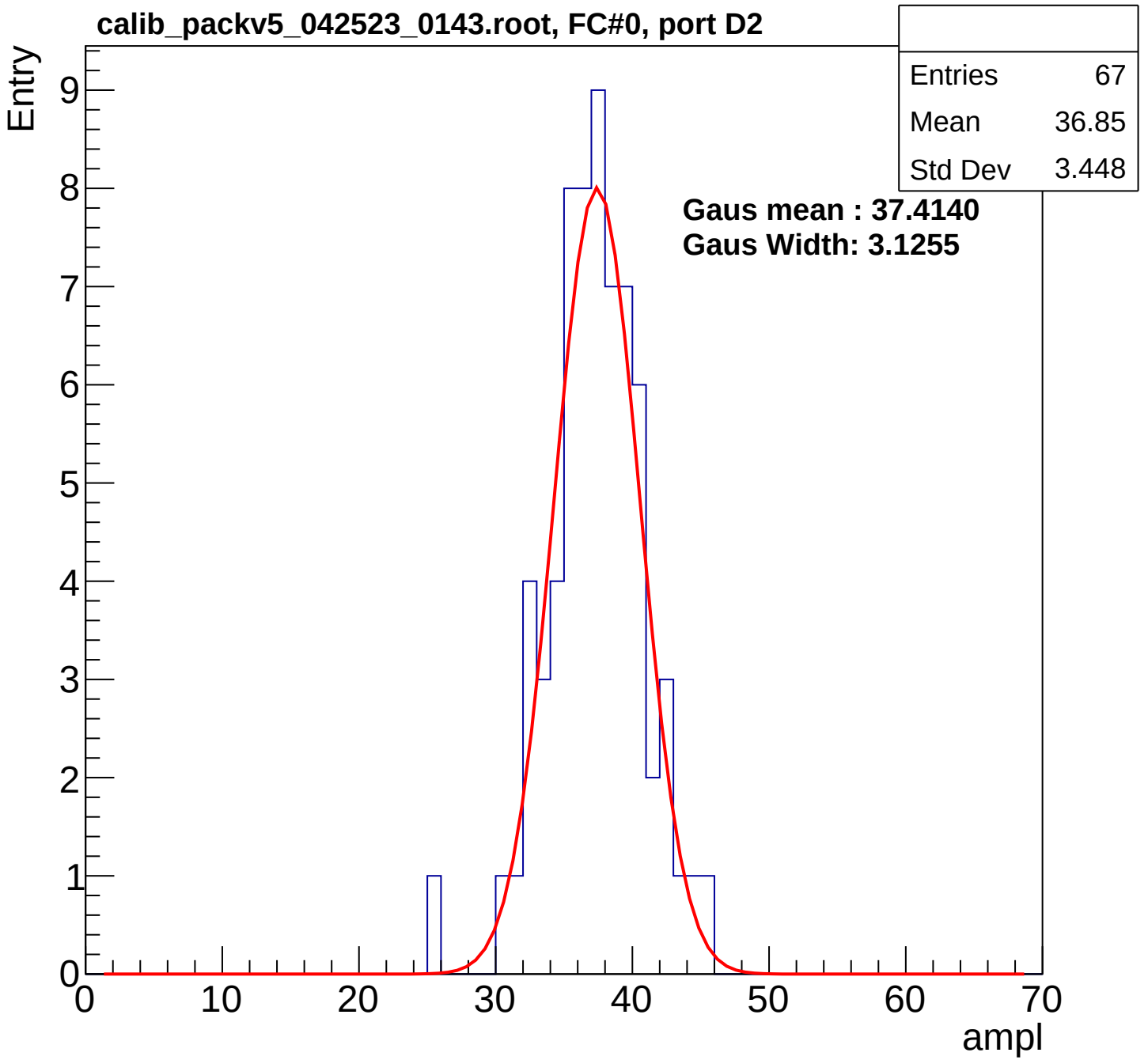
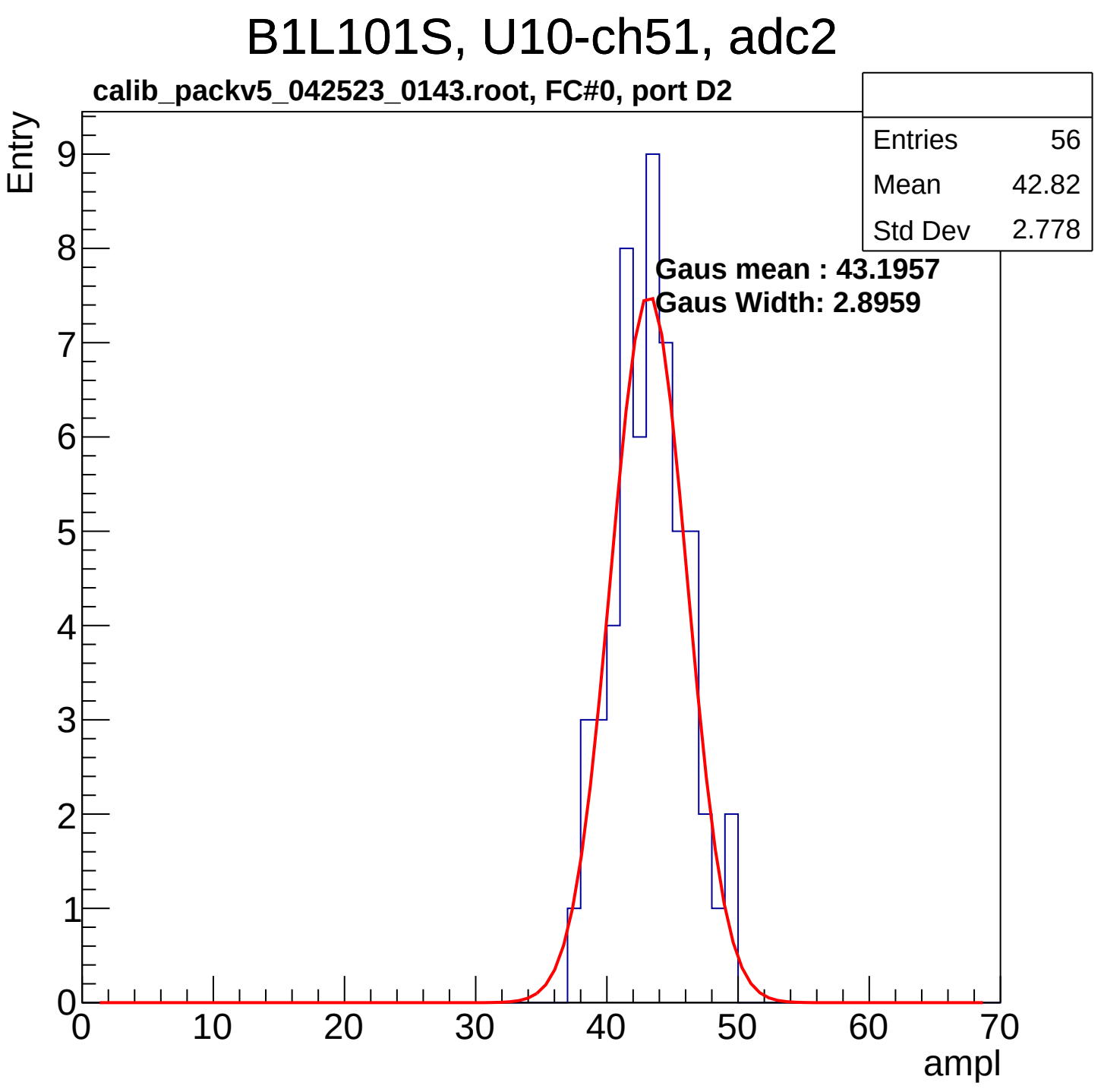

B1L101S, U10-ch50, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch51, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 83
Mean 28.39
Std Dev 6.454
Gaus mean : 30.2603
Gaus Width: 3.4995
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch51, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 36.85
Std Dev 3.448
Gaus mean : 37.4140
Gaus Width: 3.1255
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch51, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 42.82
Std Dev 2.778
Gaus mean : 43.1957
Gaus Width: 2.8959
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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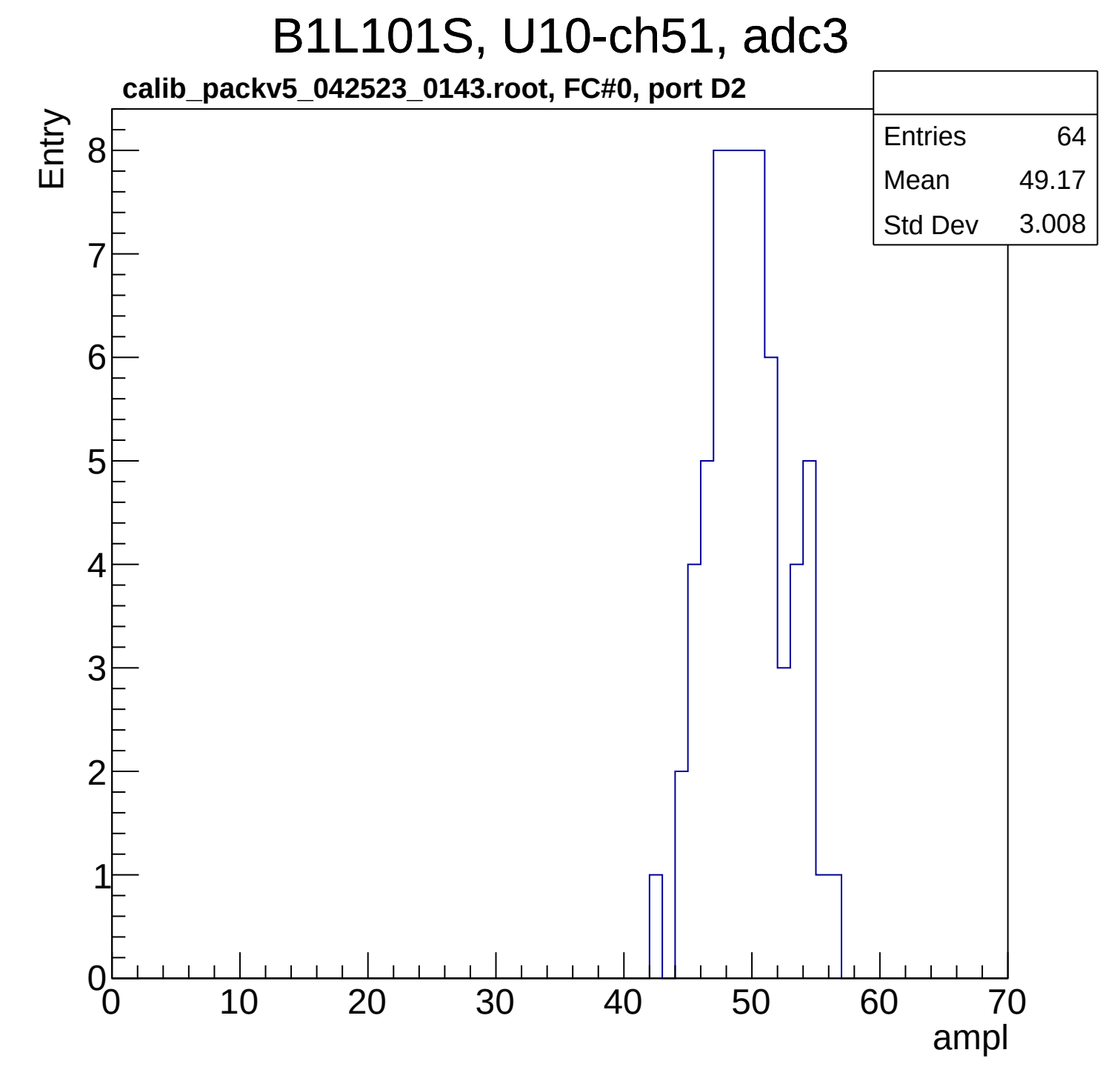
B1L101S, U10-ch51, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 49.17
Std Dev 3.008
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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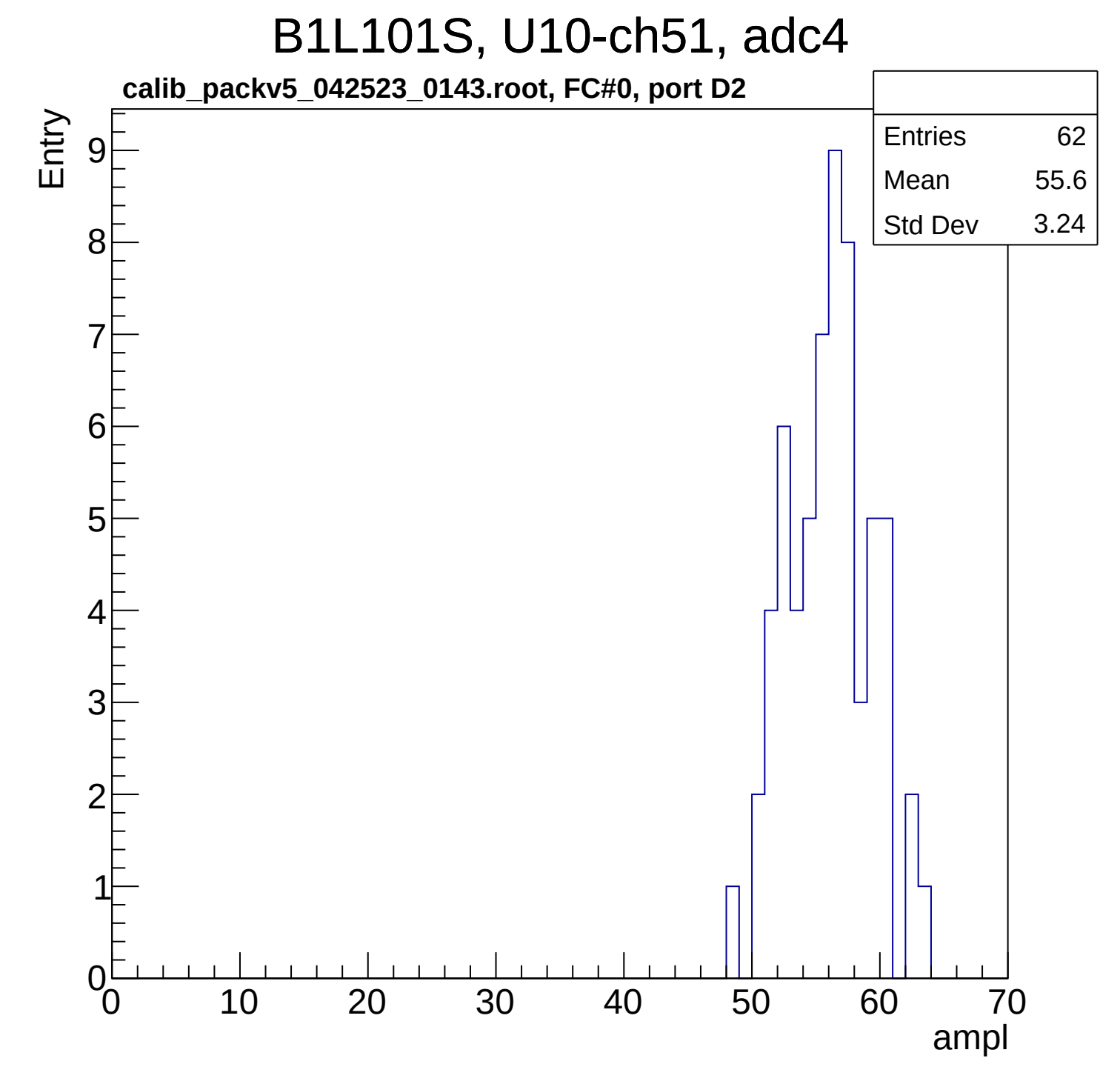
B1L101S, U10-ch51, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 55.6
Std Dev 3.24
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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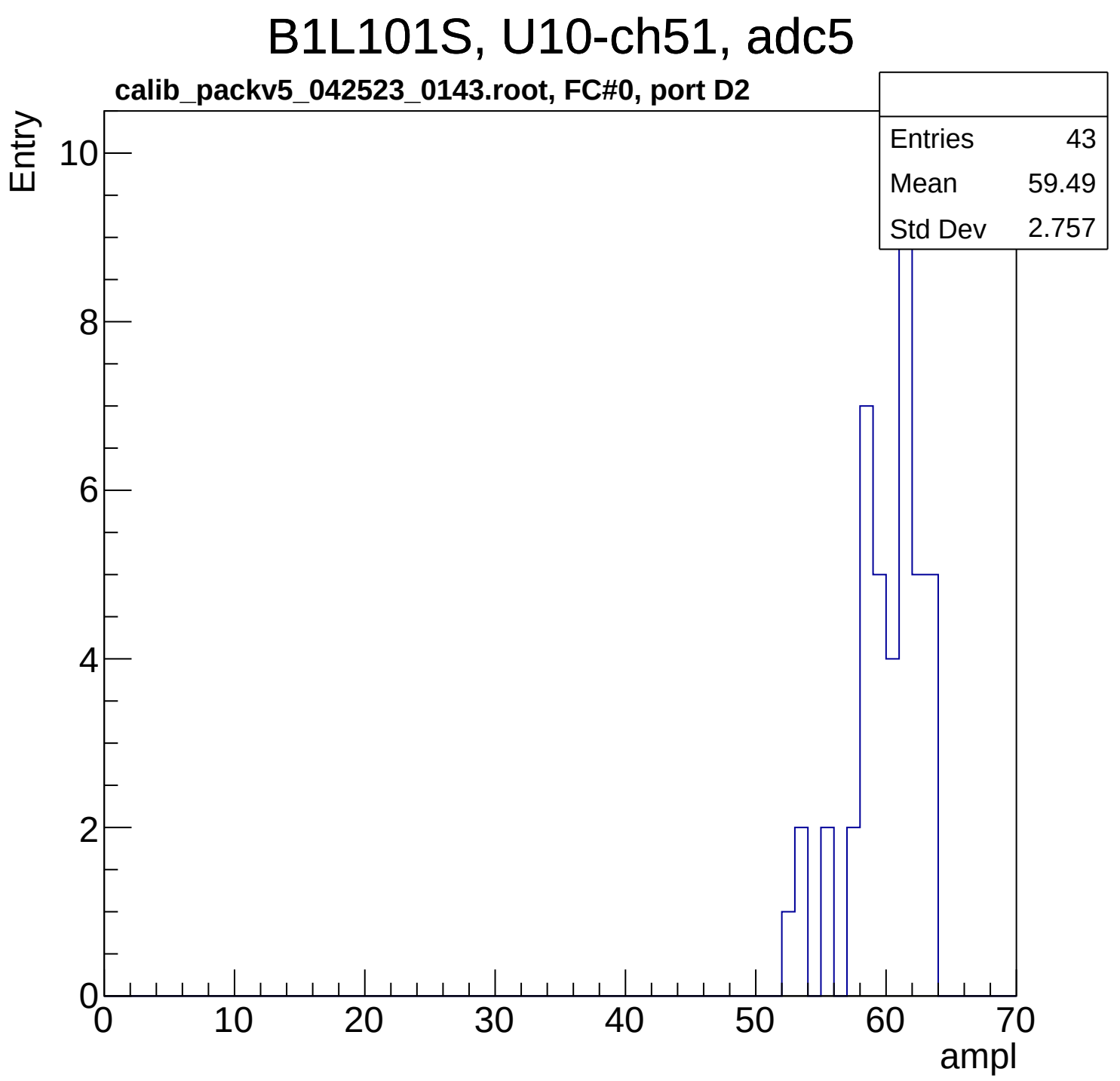
B1L101S, U10-ch51, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 43
Mean 59.49
Std Dev 2.757
Entry
ampl
0
2
4
6
8
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0
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20
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40
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60
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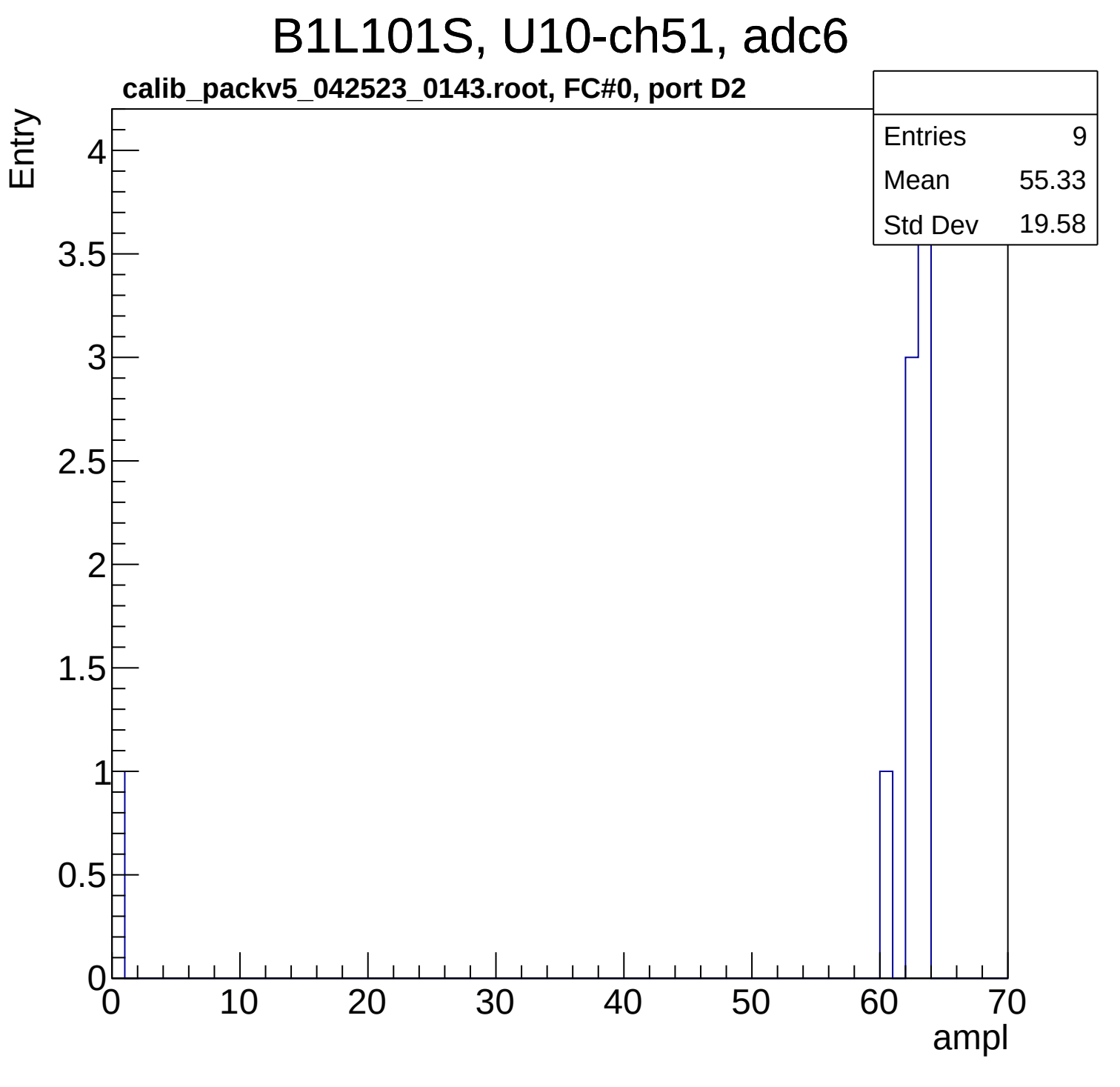
B1L101S, U10-ch51, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 55.33
Std Dev 19.58
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
50
60
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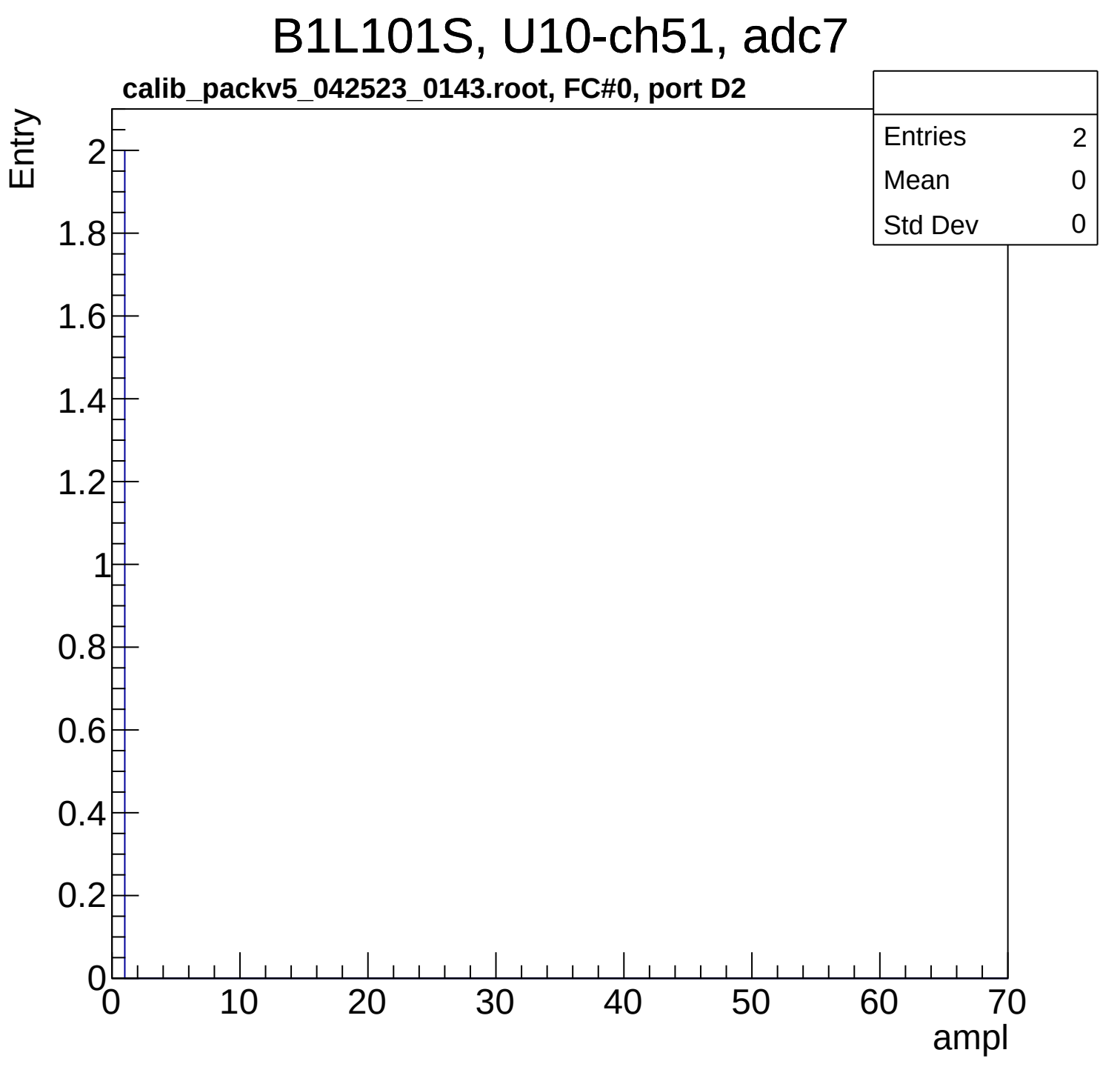
B1L101S, U10-ch51, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
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0.6
0.4
0.2
0
0
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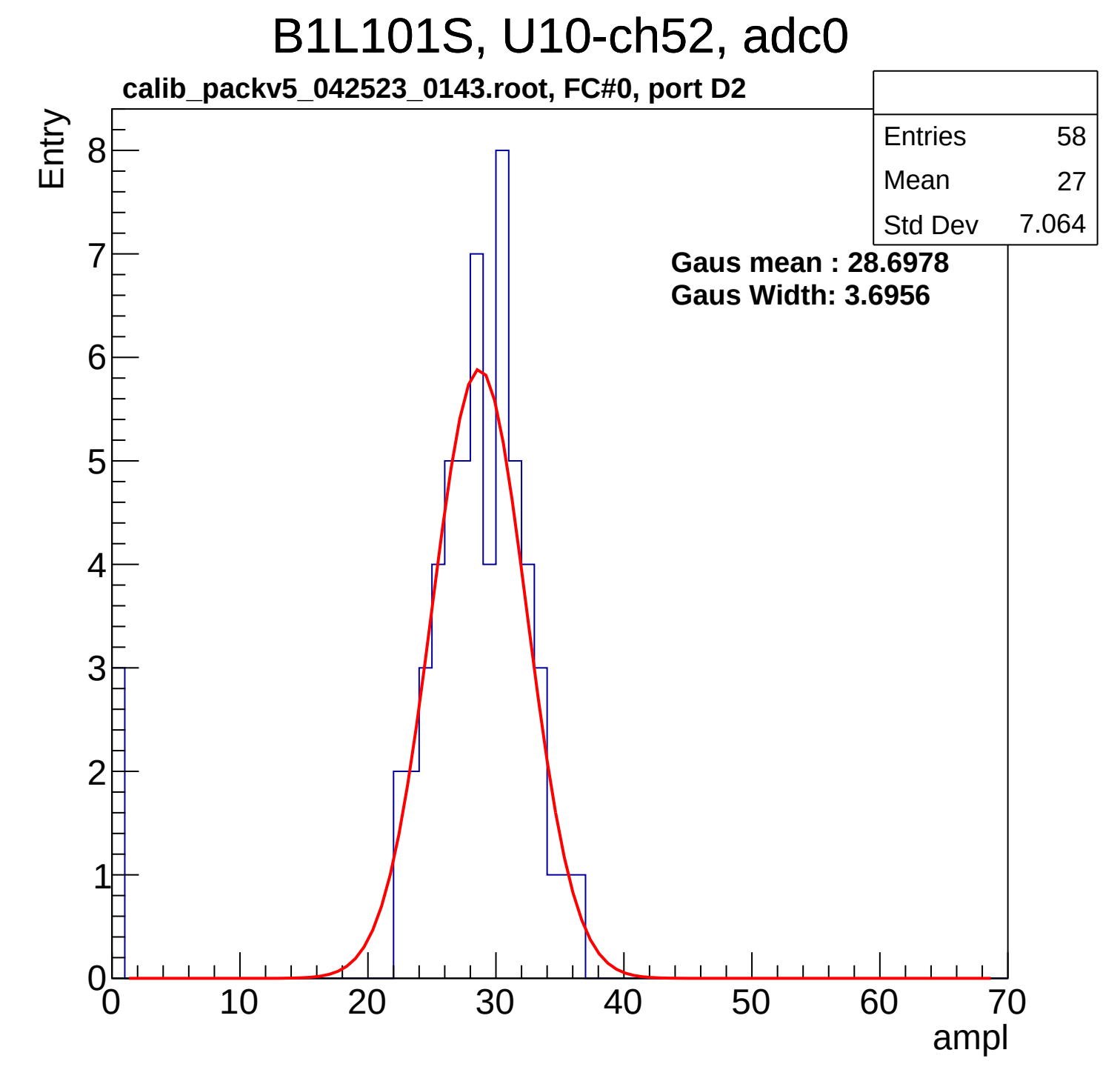
50
60
70
ampl


B1L101S, U10-ch52, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 27
Std Dev 7.064
Gaus mean : 28.6978
Gaus Width: 3.6956
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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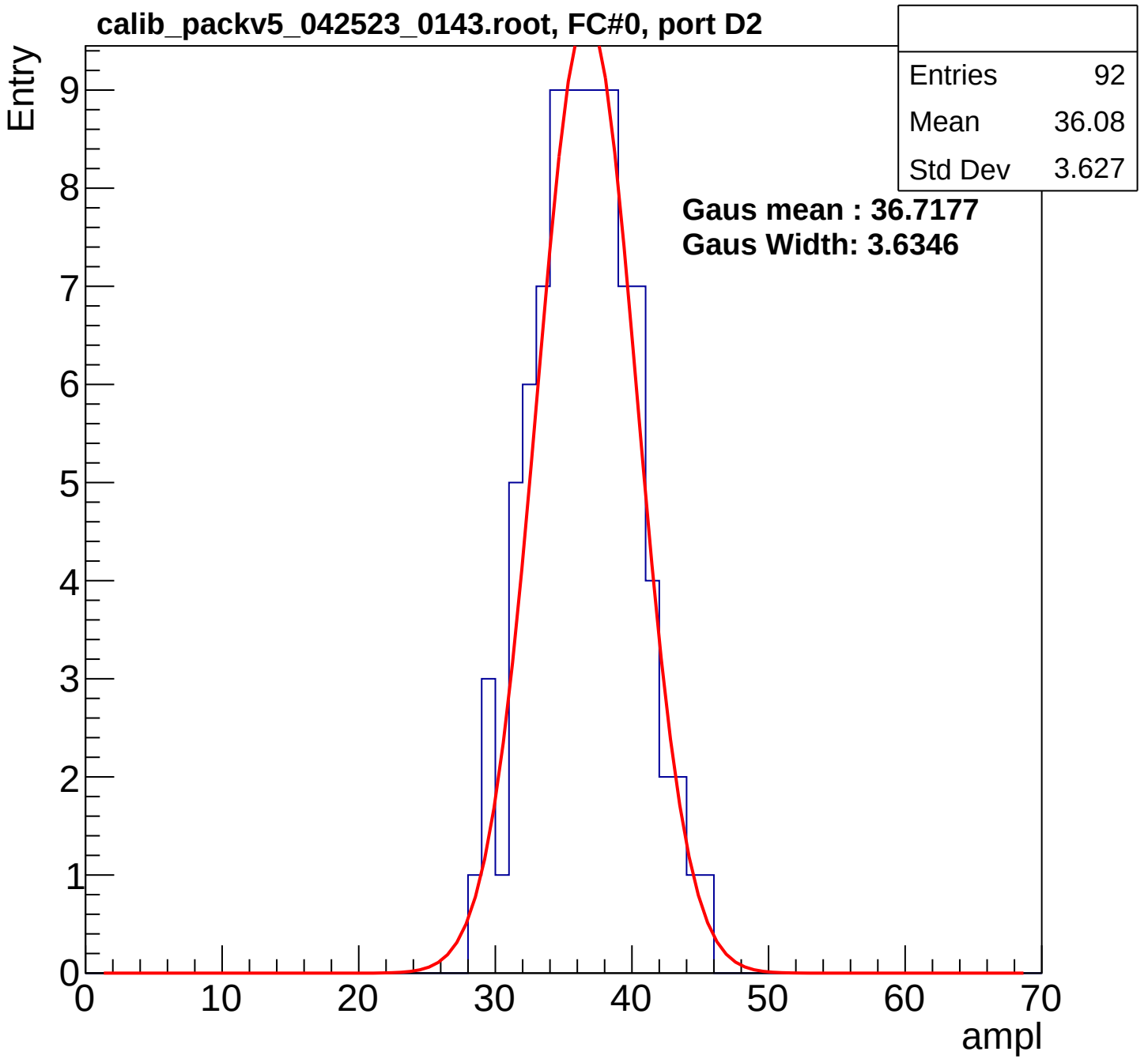
B1L101S, U10-ch52, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 92
Mean 36.08
Std Dev 3.627
Gaus mean : 36.7177
Gaus Width: 3.6346
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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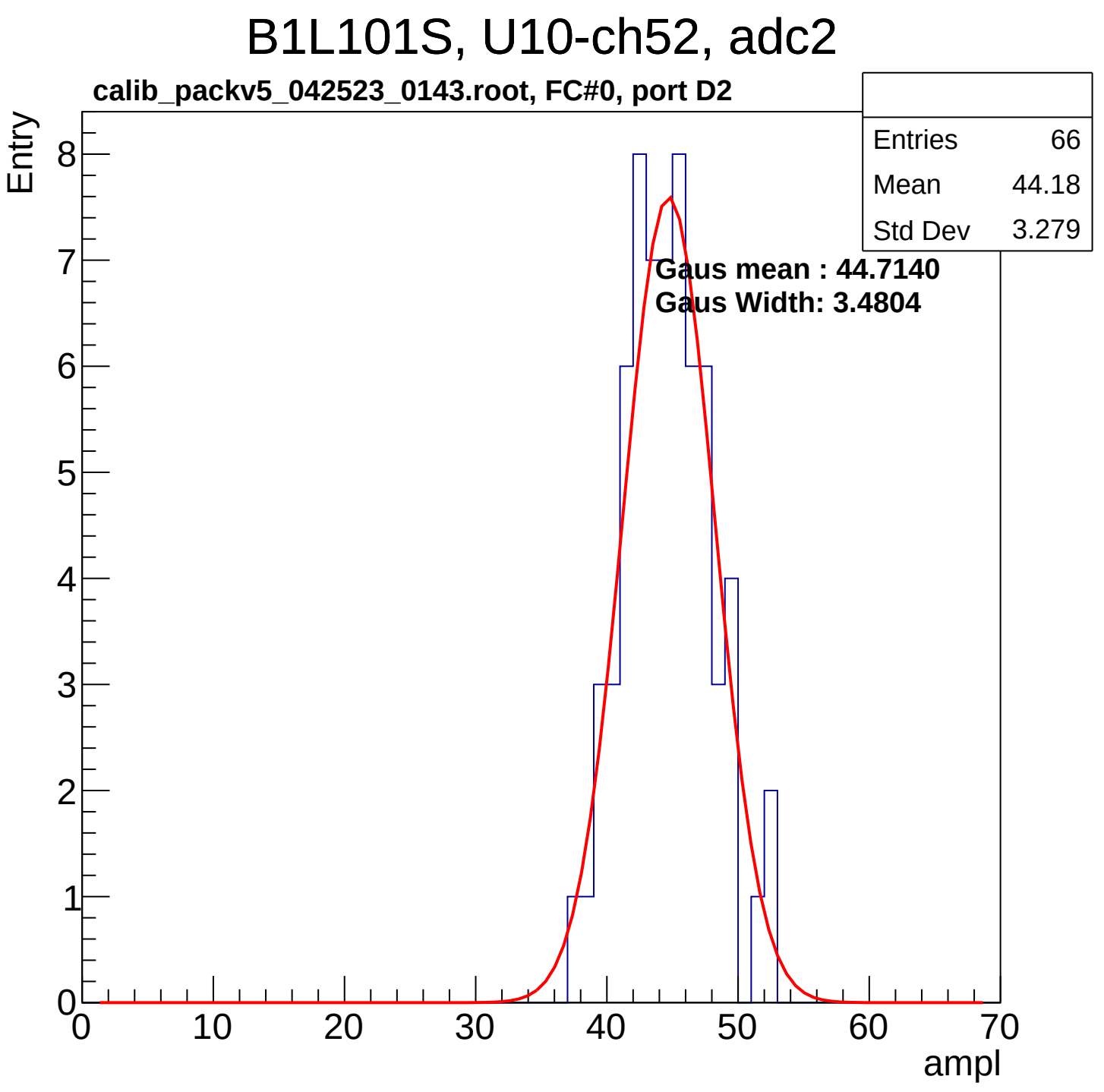
B1L101S, U10-ch52, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 44.18
Std Dev 3.279
Gaus mean : 44.7140
Gaus Width: 3.4804
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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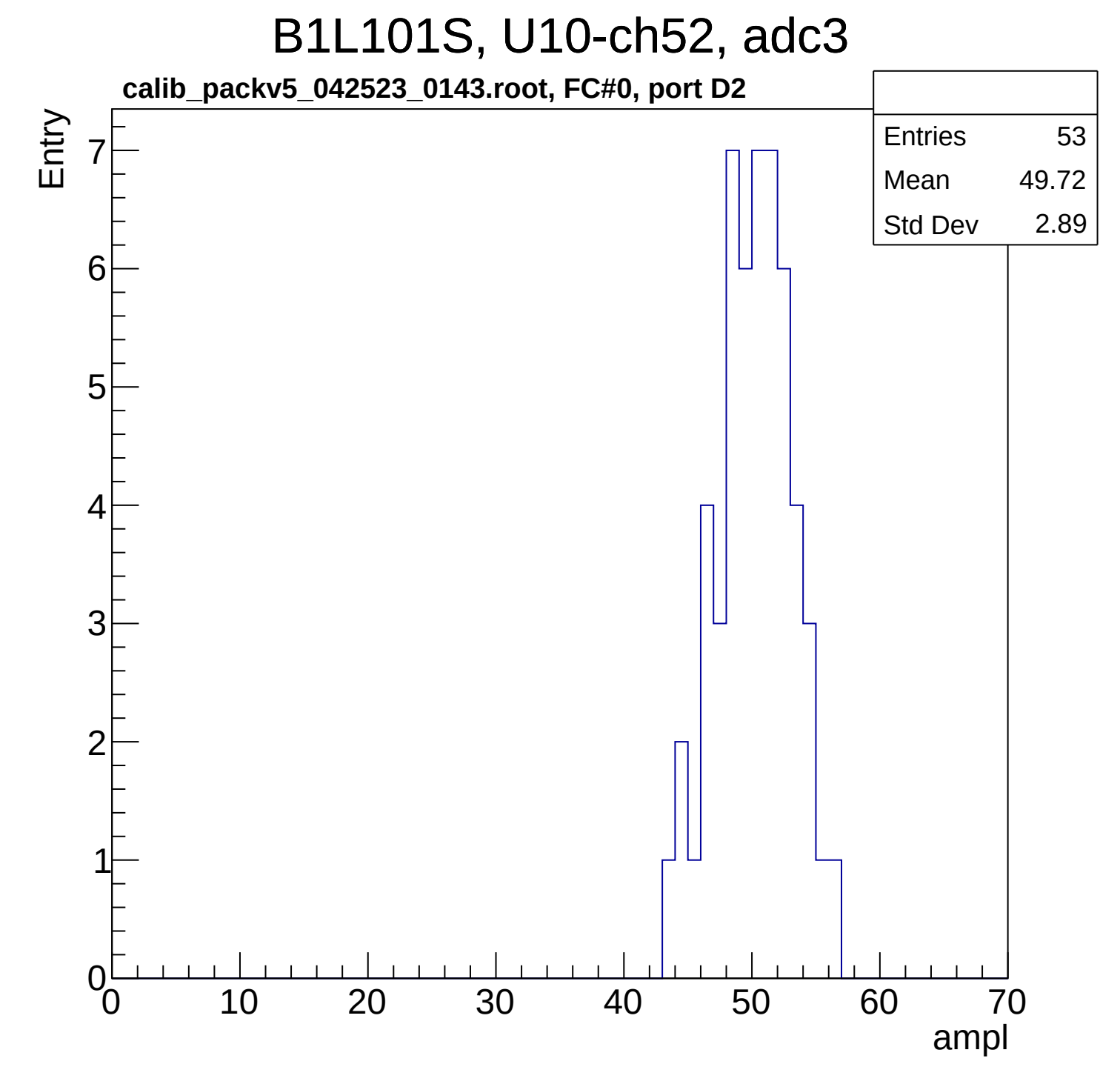
B1L101S, U10-ch52, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 49.72
Std Dev 2.89
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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40
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60
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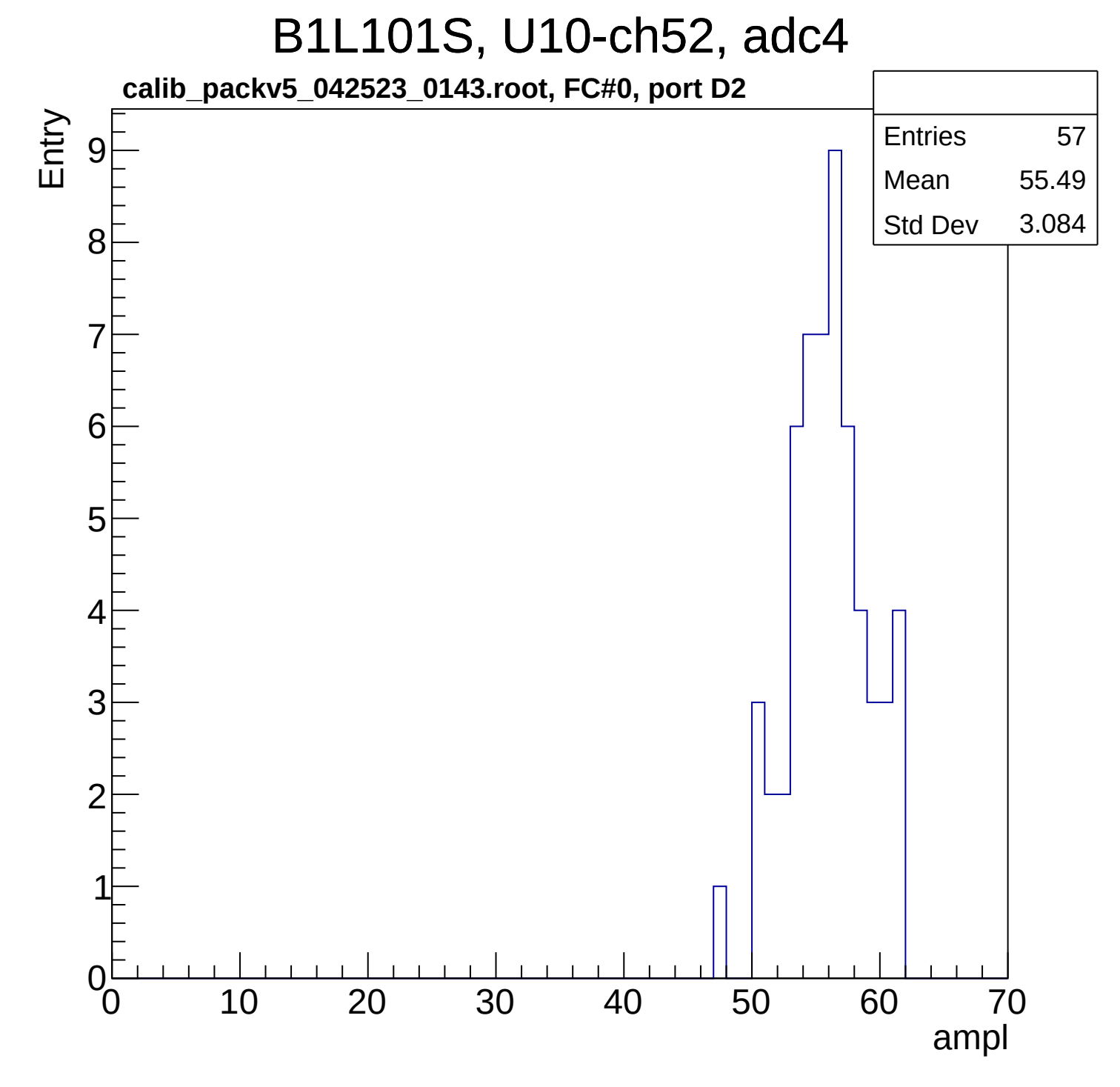
B1L101S, U10-ch52, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 55.49
Std Dev 3.084
Entry
ampl
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3
4
5
6
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0
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60
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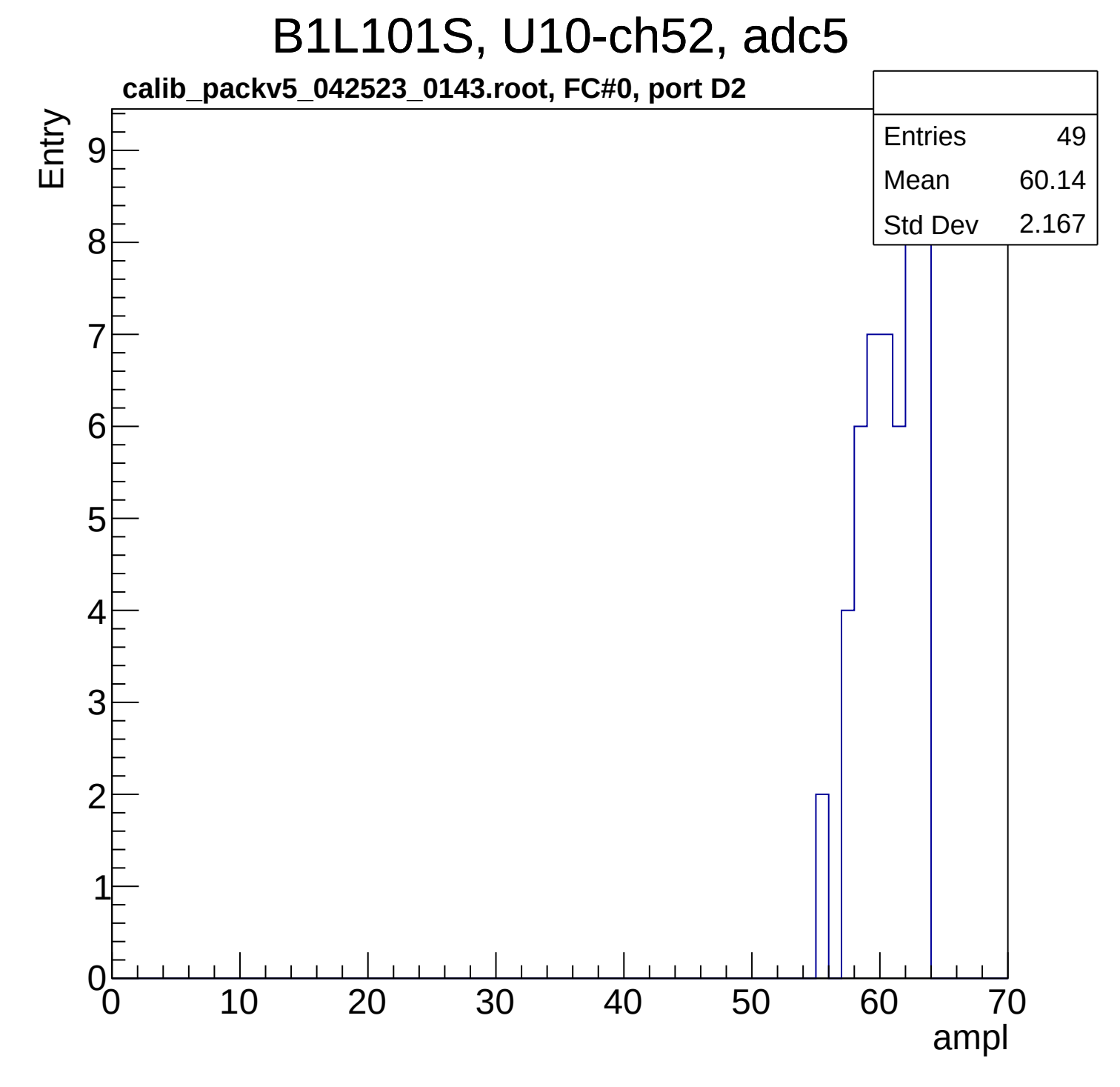
B1L101S, U10-ch52, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 60.14
Std Dev 2.167
Entry
ampl
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2
3
4
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6
7
8
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0
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60
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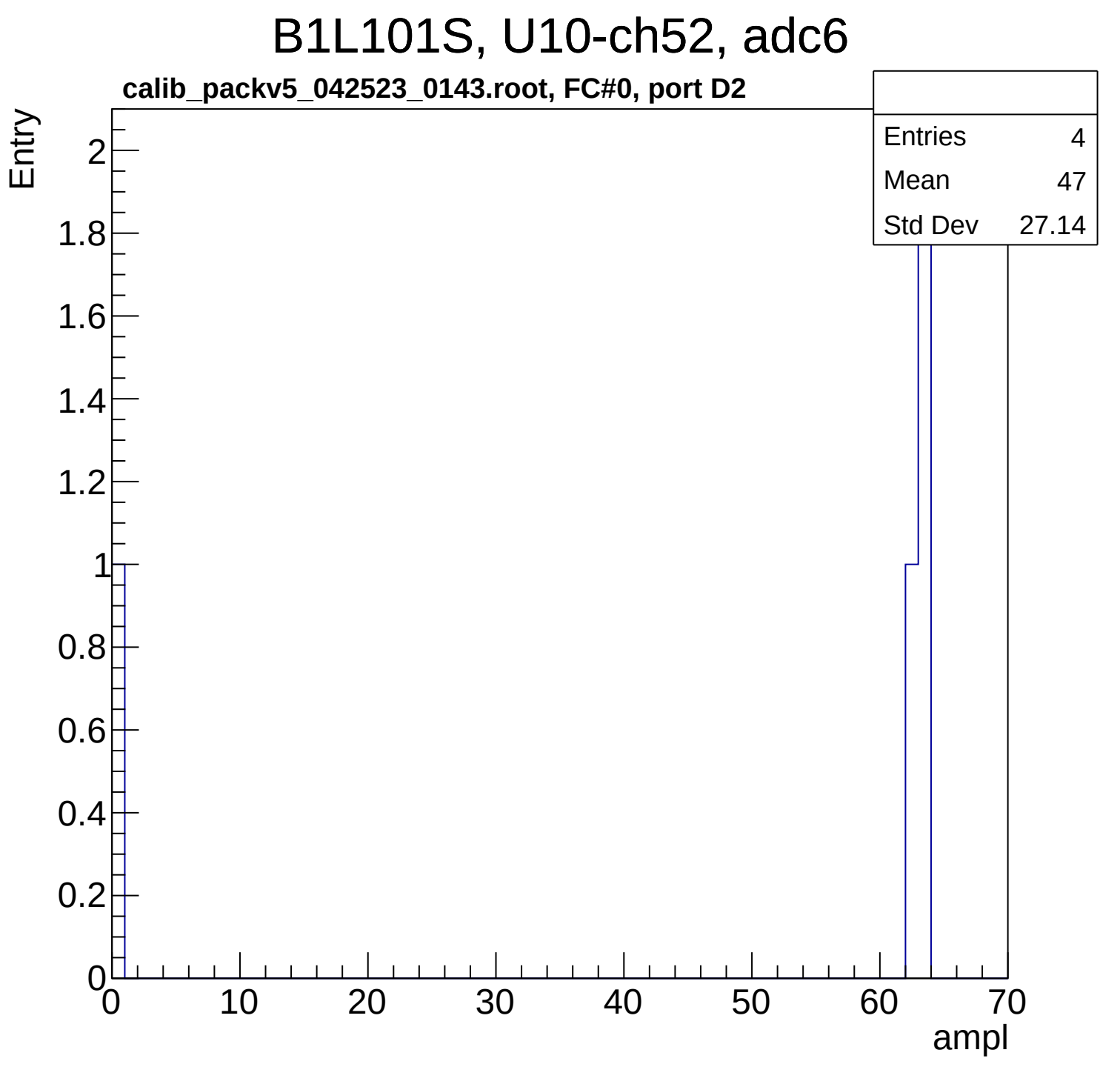
B1L101S, U10-ch52, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 47
Std Dev 27.14
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
50
60
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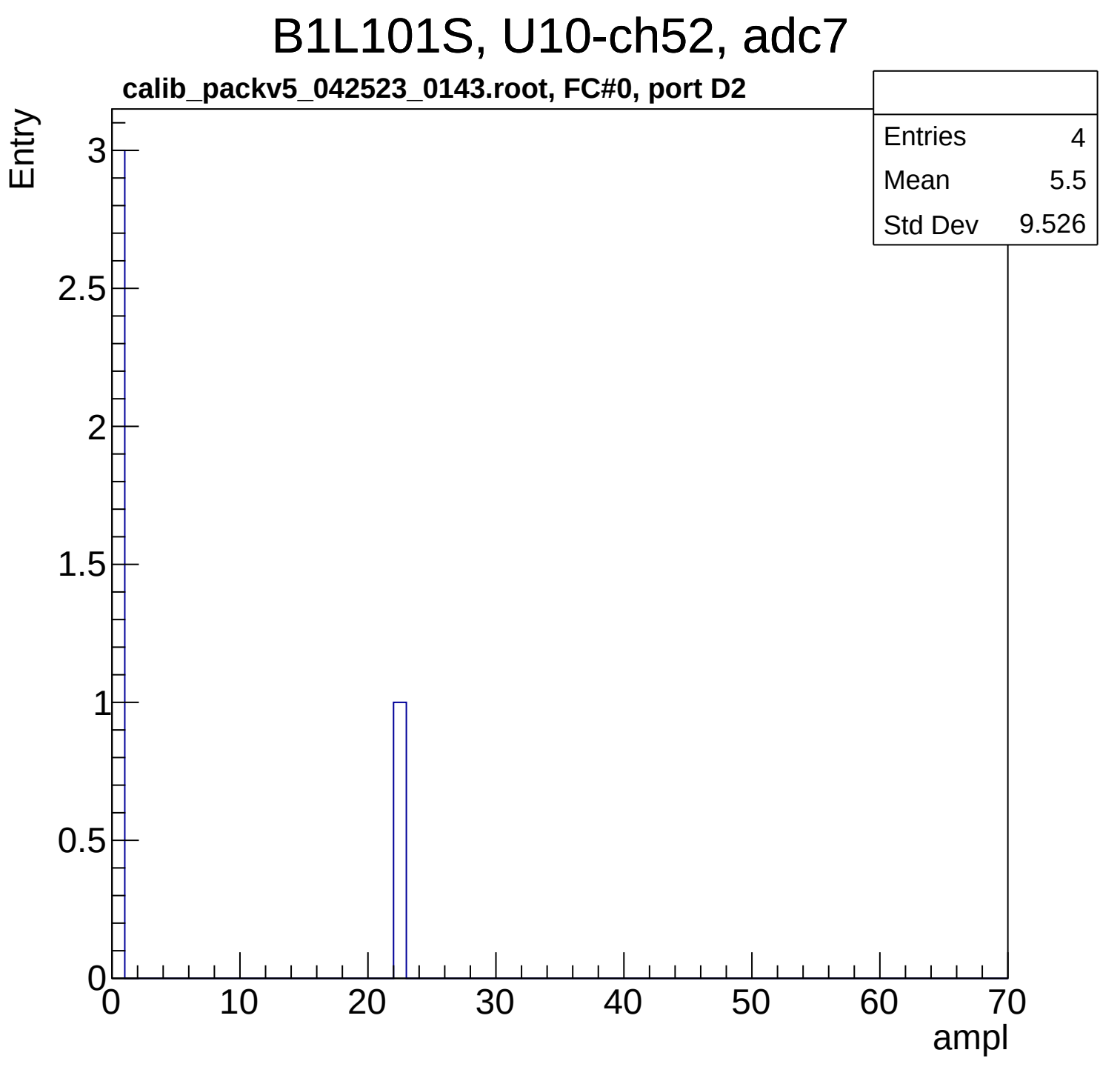
B1L101S, U10-ch52, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 5.5
Std Dev 9.526
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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60
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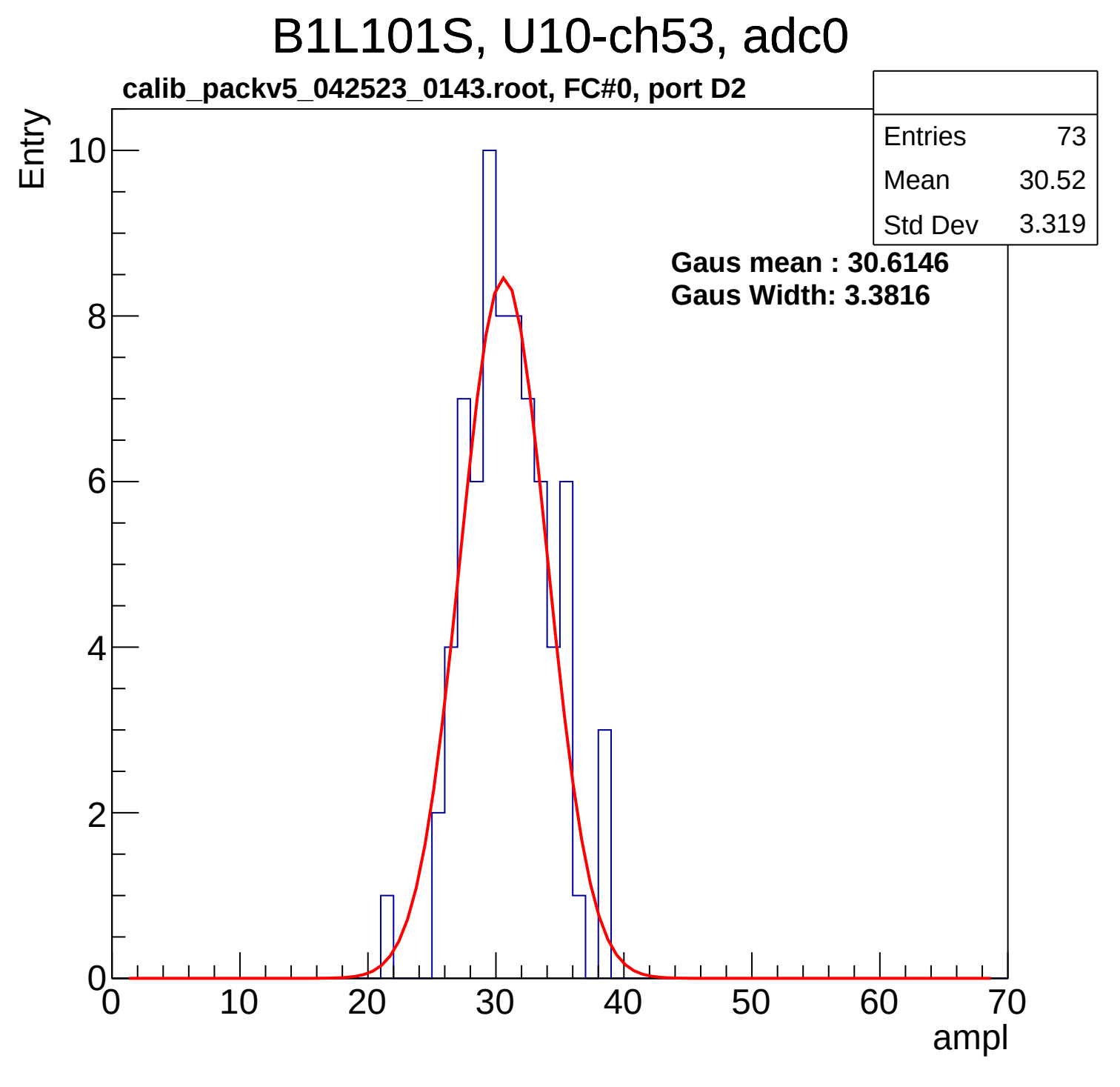
B1L101S, U10-ch53, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 30.52
Std Dev 3.319
Gaus mean : 30.6146
Gaus Width: 3.3816
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
50
60
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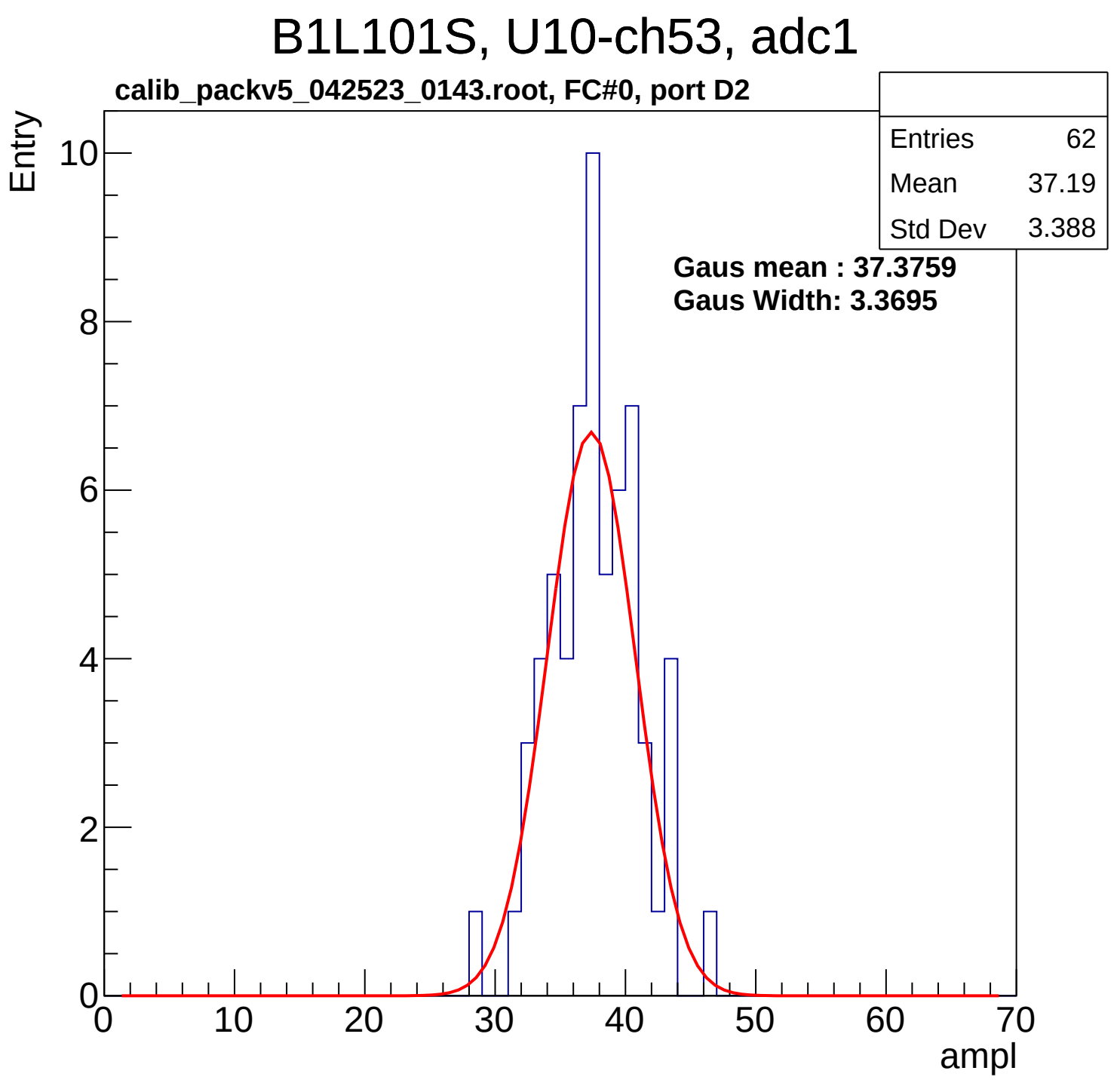
B1L101S, U10-ch53, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 37.19
Std Dev 3.388
Gaus mean : 37.3759
Gaus Width: 3.3695
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
50
60
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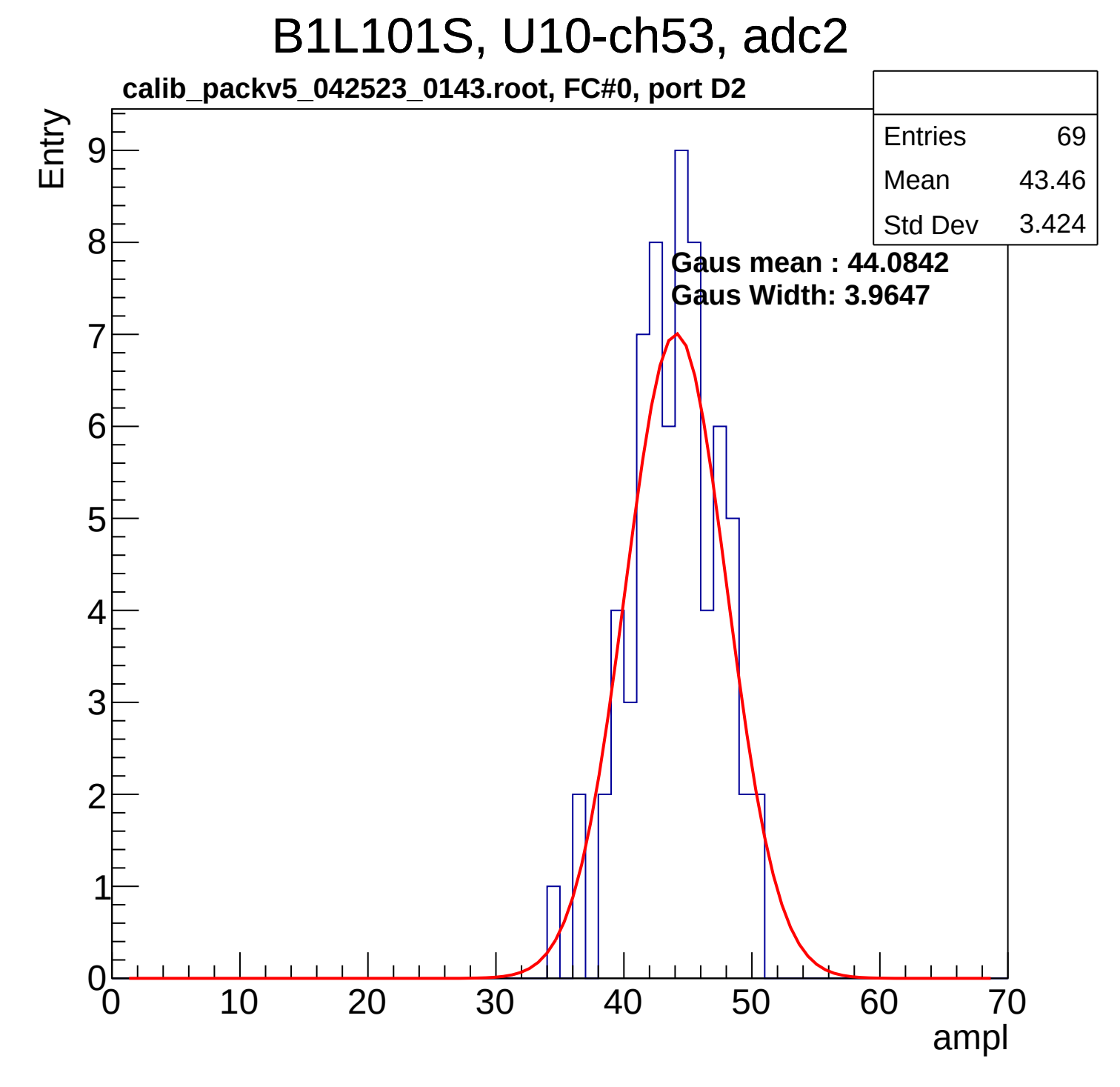
B1L101S, U10-ch53, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 43.46
Std Dev 3.424
Gaus mean : 44.0842
Gaus Width: 3.9647
Entry
ampl
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2
3
4
5
6
7
8
9
0
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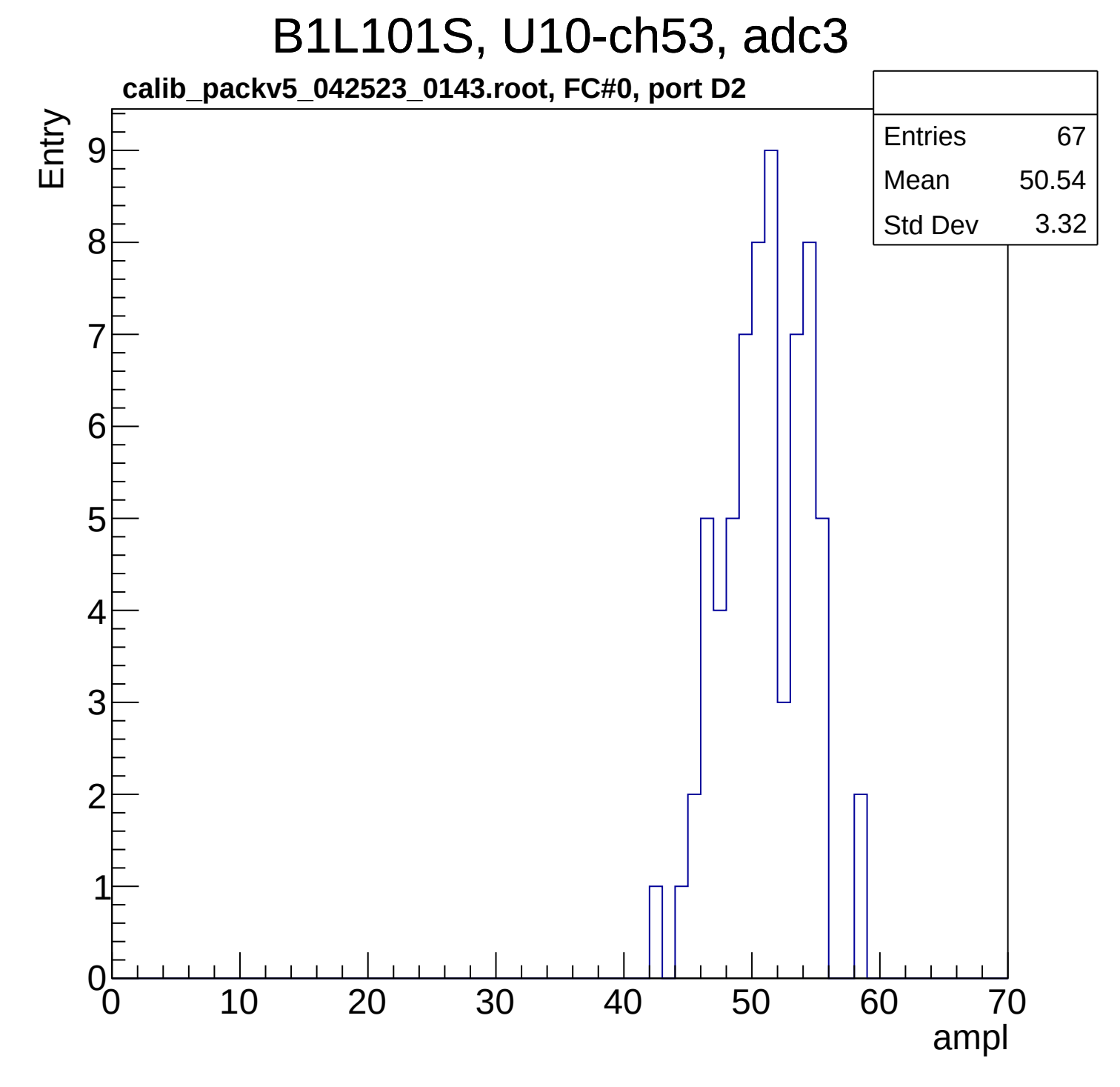
B1L101S, U10-ch53, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 50.54
Std Dev 3.32
Entry
ampl
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2
3
4
5
6
7
8
9
0
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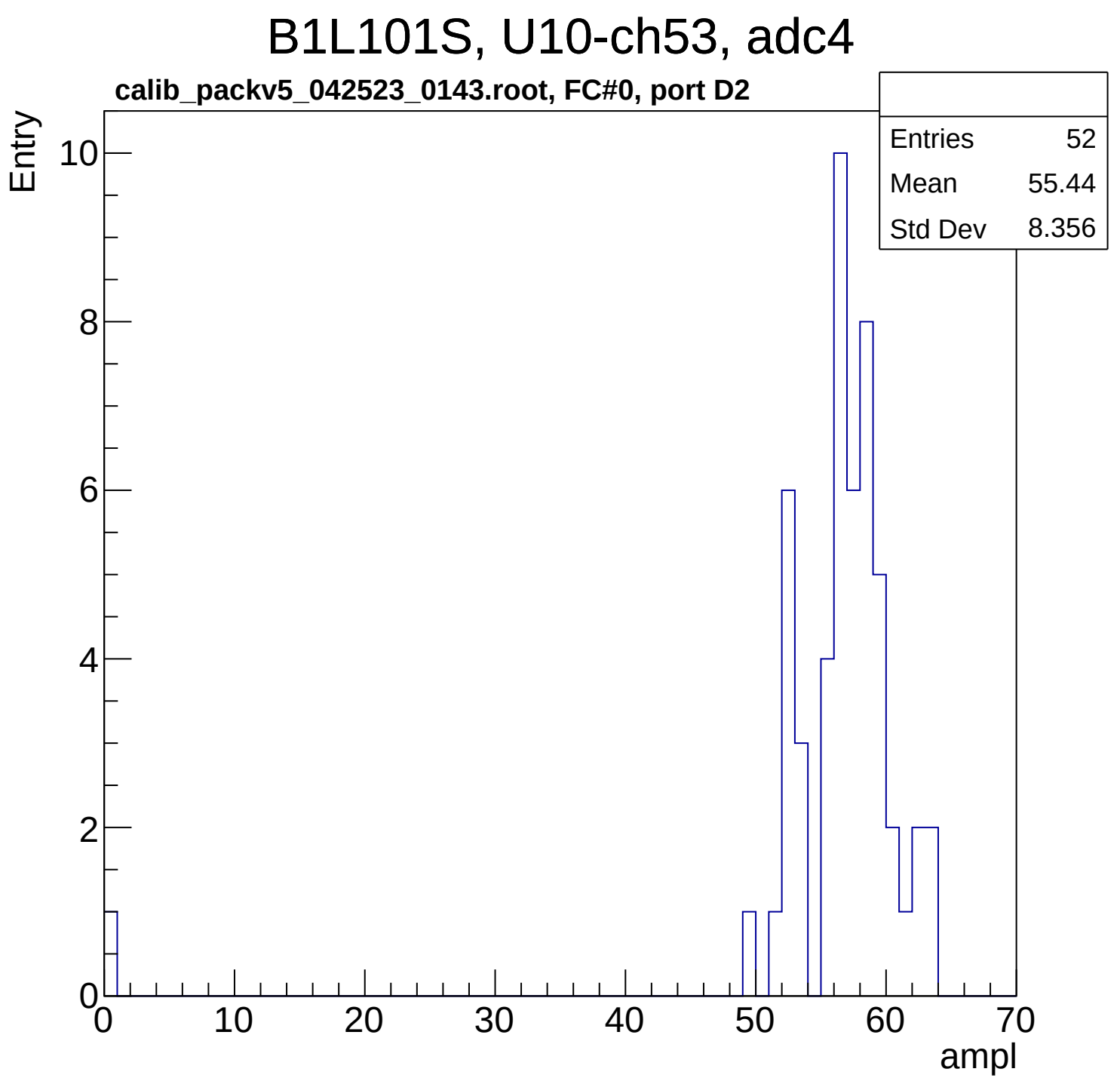
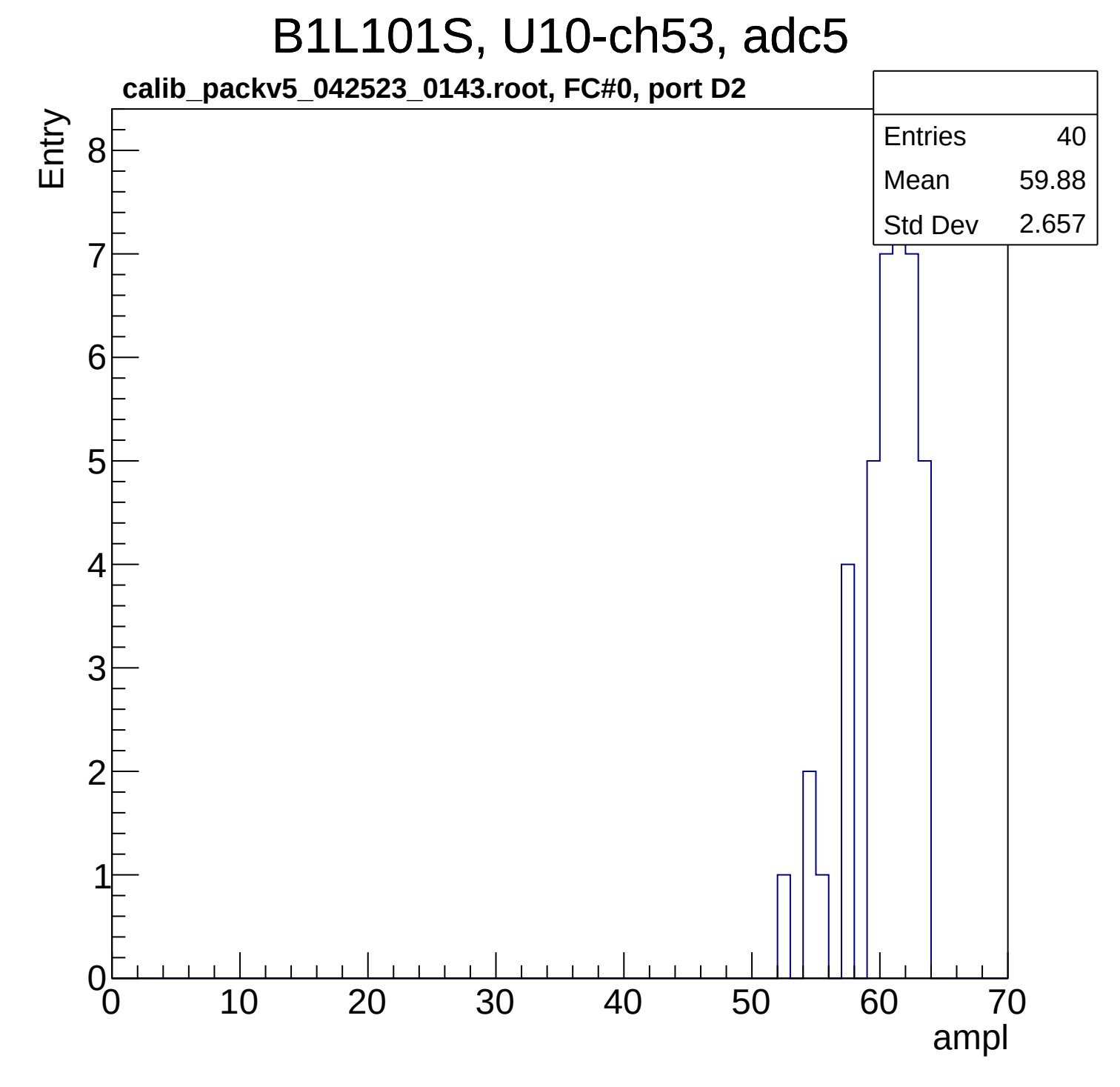

B1L101S, U10-ch53, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 55.44
Std Dev 8.356
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch53, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 40
Mean 59.88
Std Dev 2.657
Entry
ampl
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1
2
3
4
5
6
7
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0
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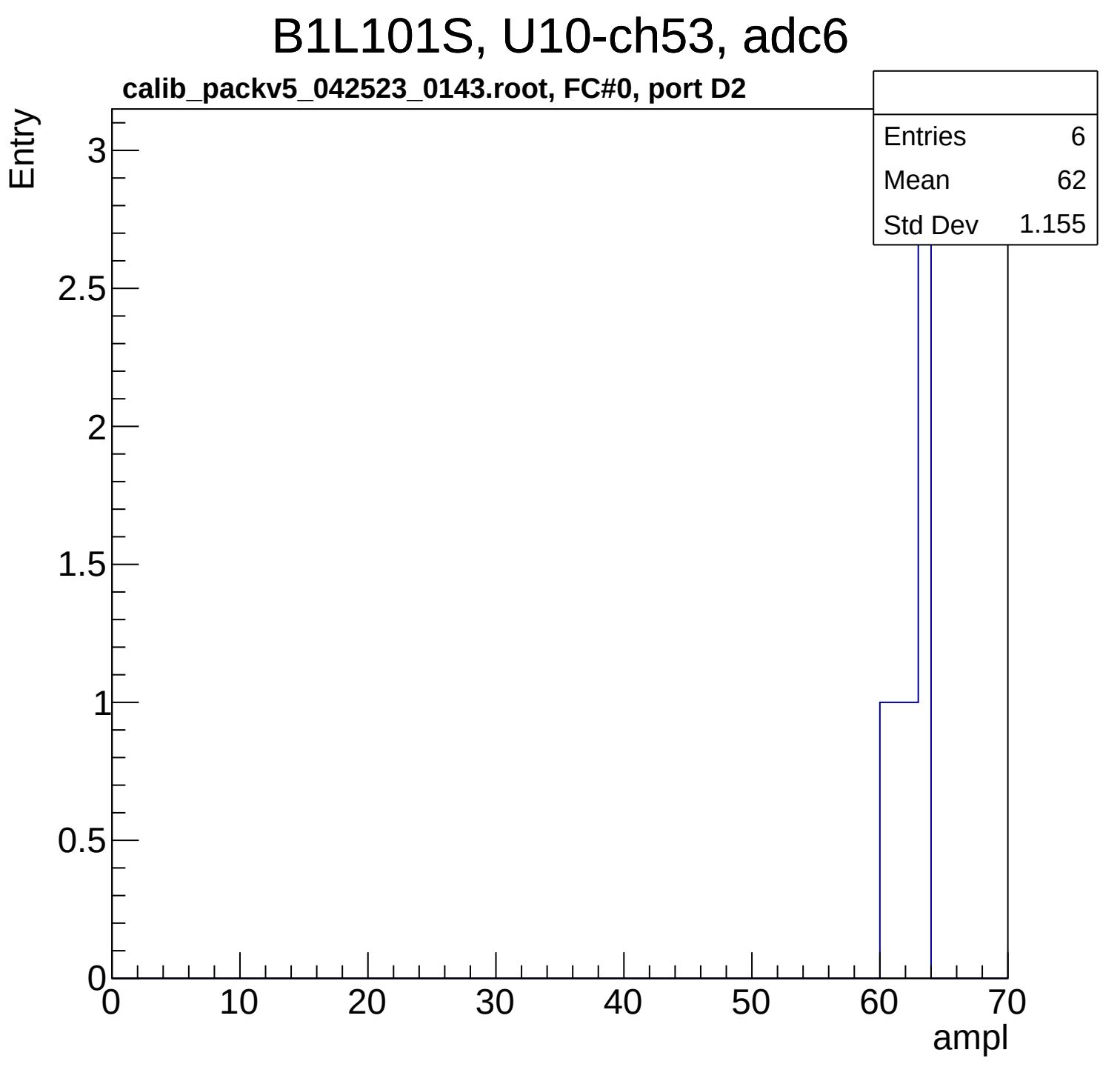
B1L101S, U10-ch53, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 62
Std Dev 1.155
Entry
ampl
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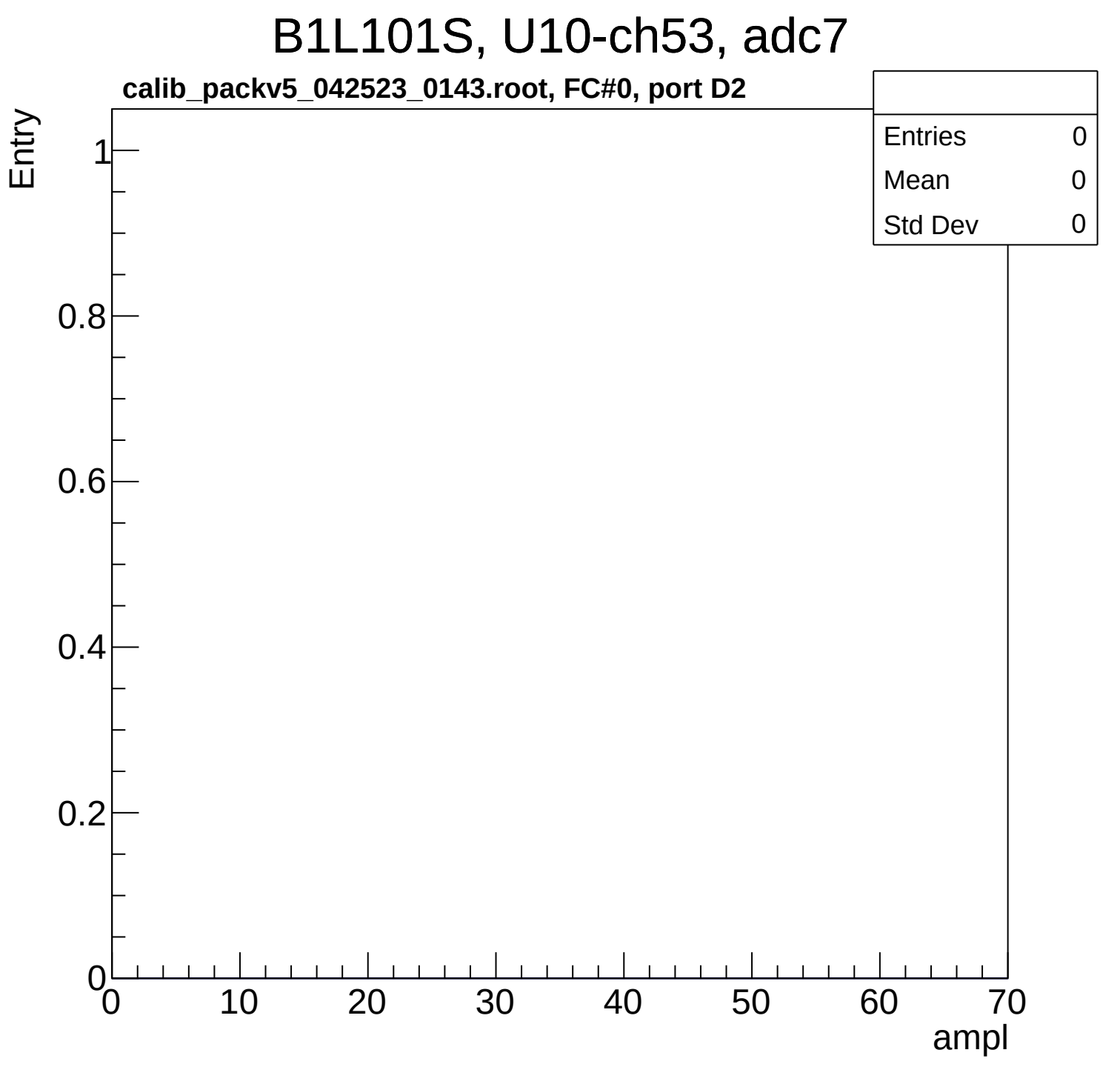
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U10-ch53, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
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50
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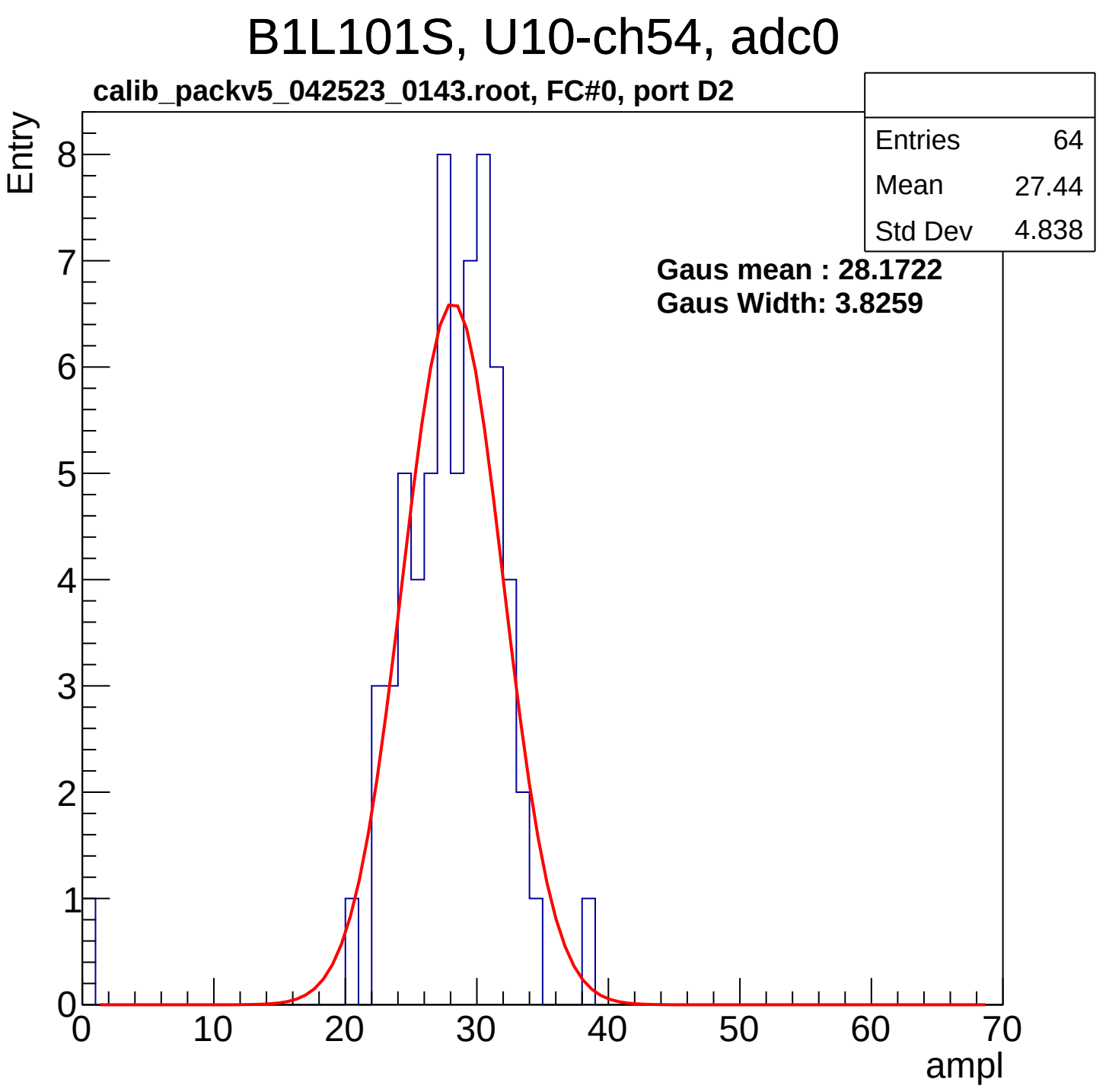
70
ampl


B1L101S, U10-ch54, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 27.44
Std Dev 4.838
Gaus mean : 28.1722
Gaus Width: 3.8259
Entry
ampl
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1
2
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4
5
6
7
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0
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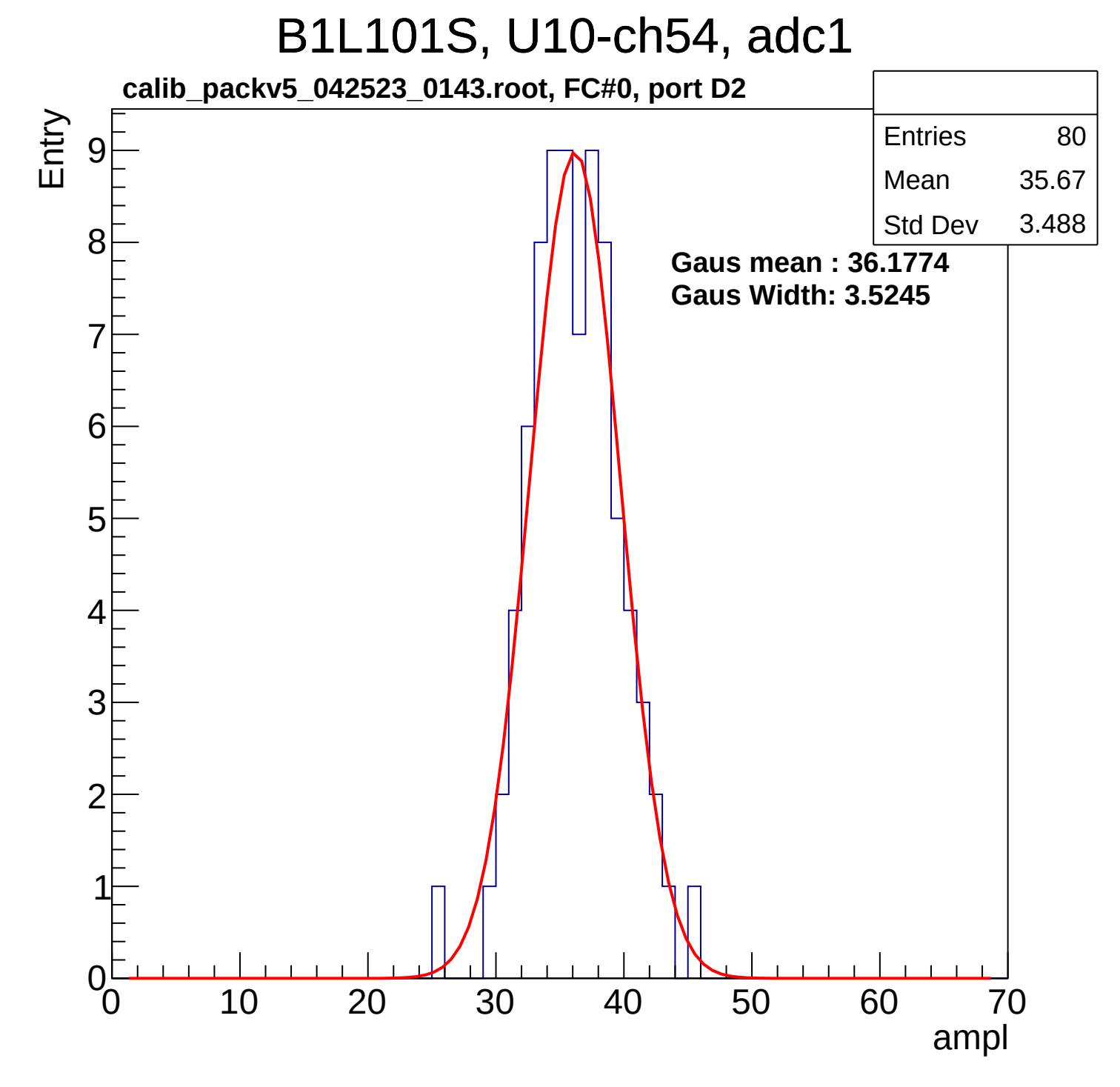
B1L101S, U10-ch54, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 80
Mean 35.67
Std Dev 3.488
Gaus mean : 36.1774
Gaus Width: 3.5245
Entry
ampl
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3
4
5
6
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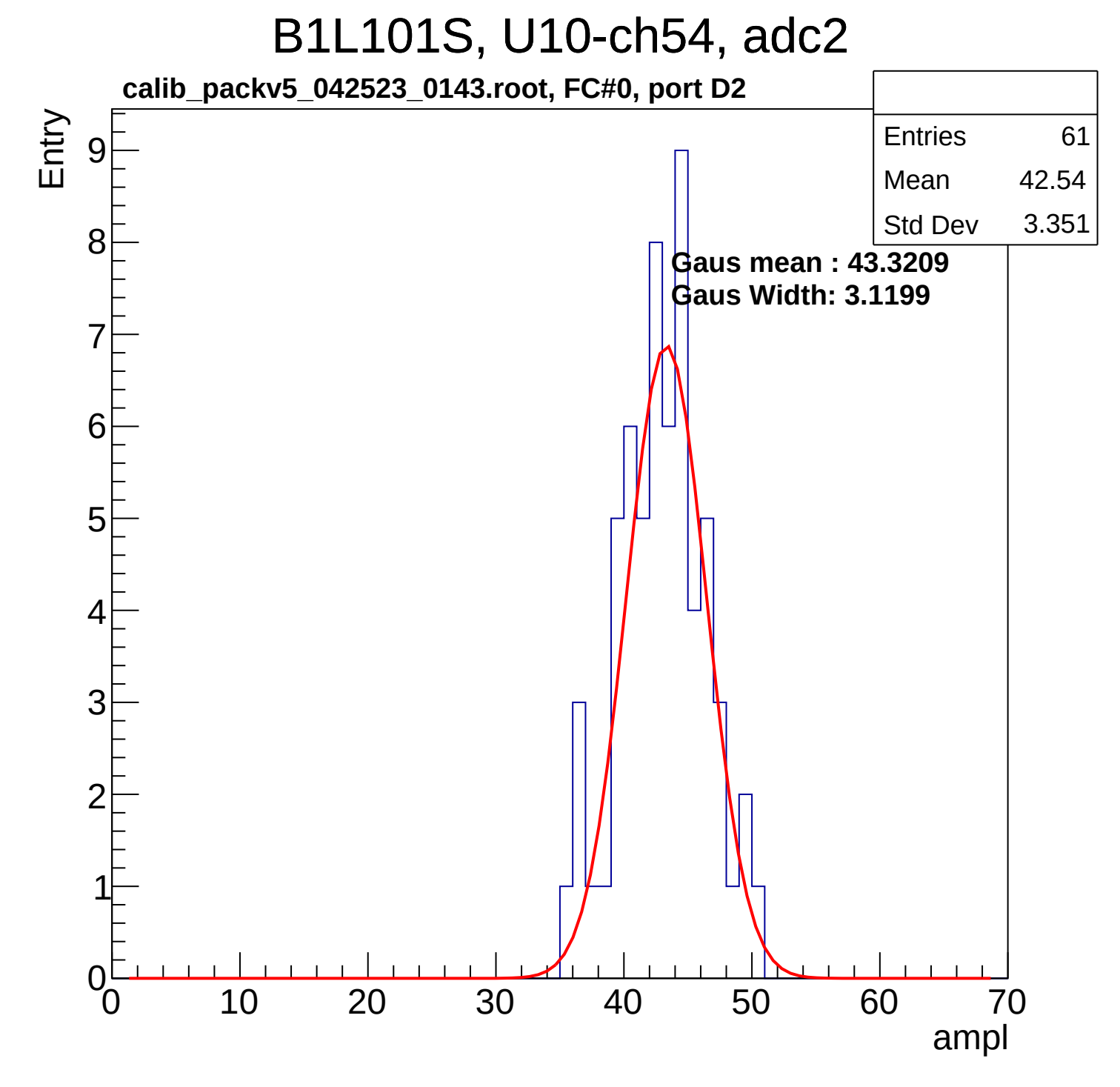
B1L101S, U10-ch54, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 42.54
Std Dev 3.351
Gaus mean : 43.3209
Gaus Width: 3.1199
Entry
ampl
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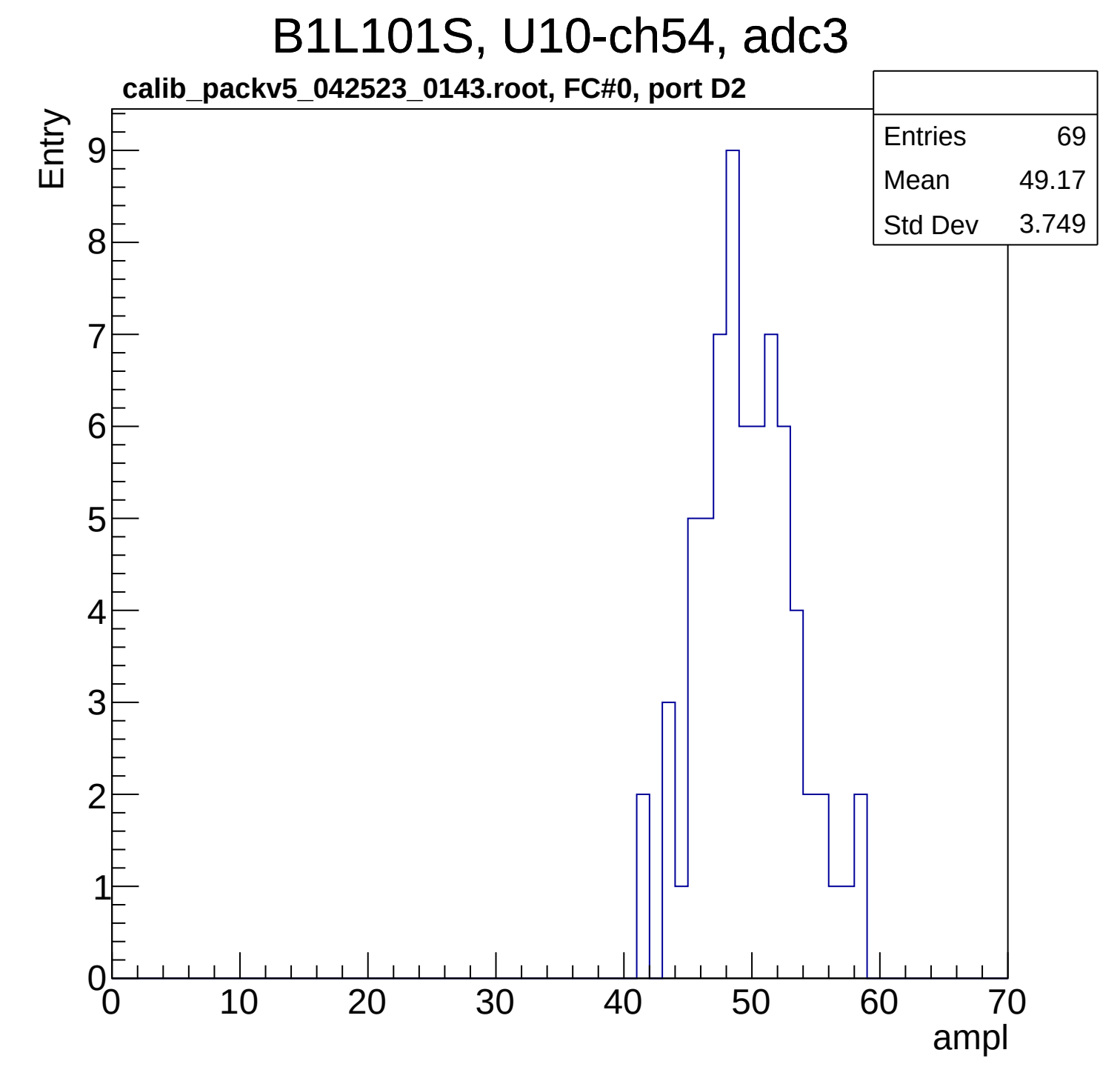
B1L101S, U10-ch54, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 49.17
Std Dev 3.749
Entry
ampl
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3
4
5
6
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0
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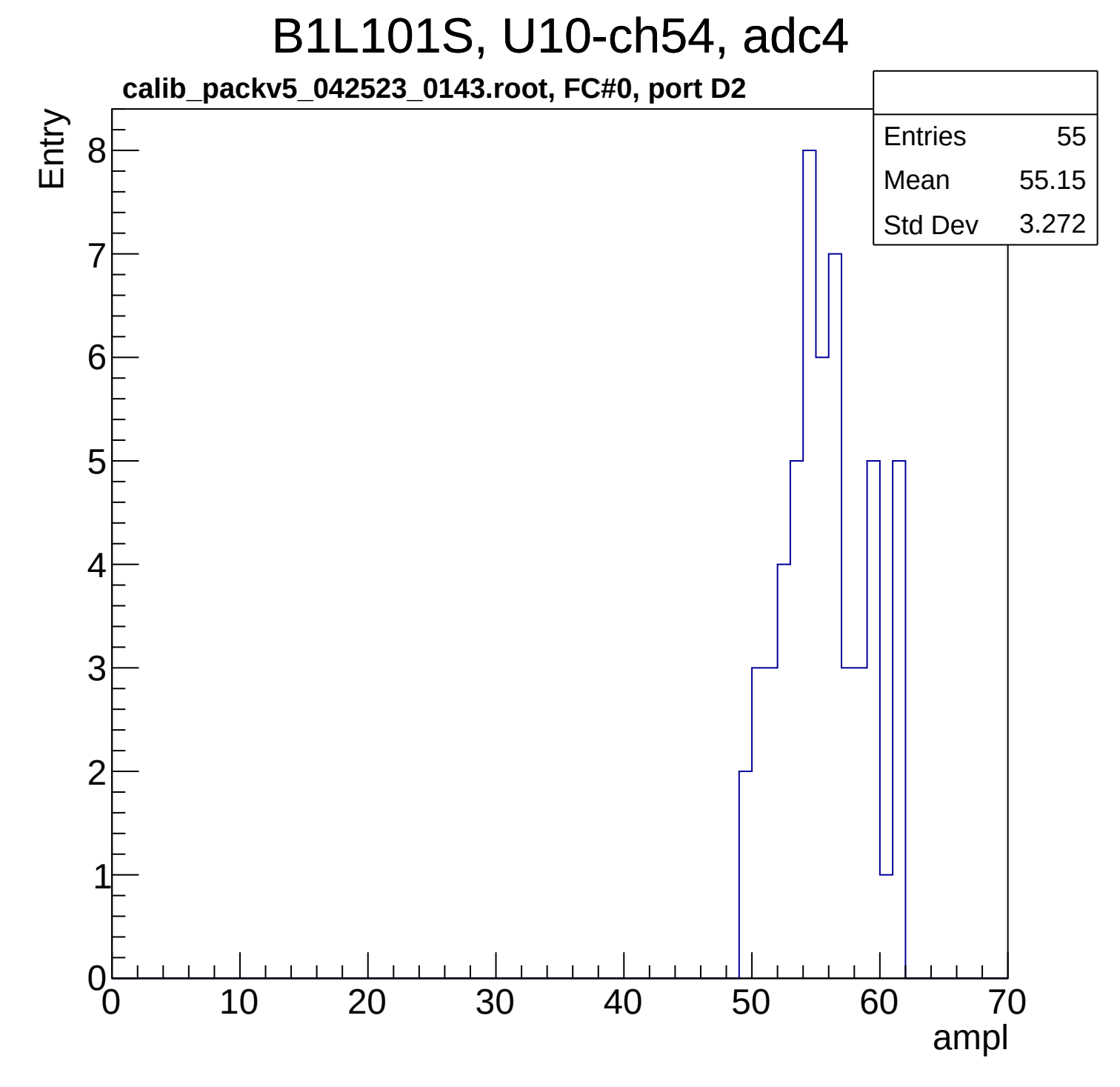
B1L101S, U10-ch54, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 55.15
Std Dev 3.272
Entry
ampl
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1
2
3
4
5
6
7
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0
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40
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60
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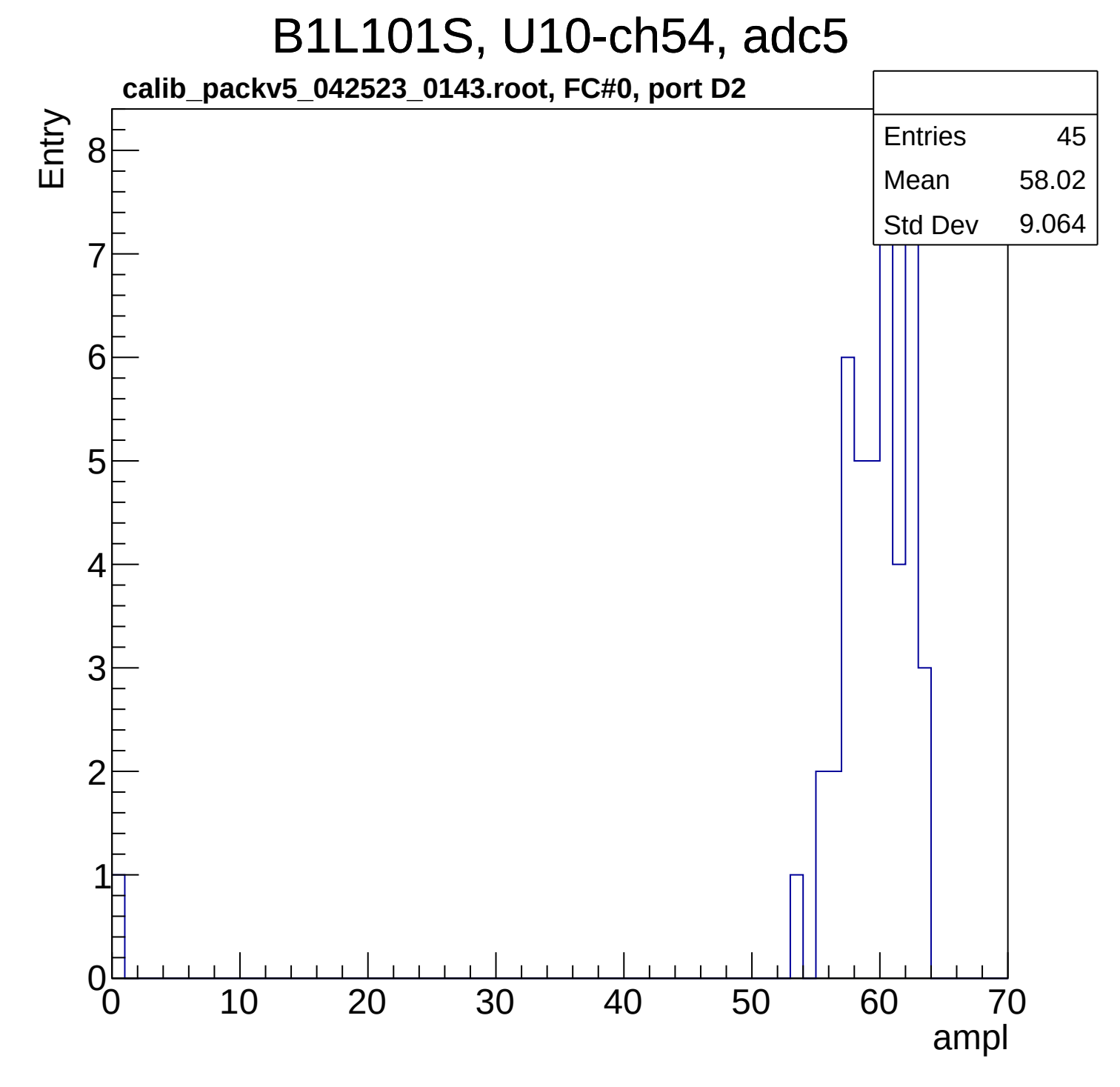
B1L101S, U10-ch54, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 58.02
Std Dev 9.064
Entry
ampl
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1
2
3
4
5
6
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8
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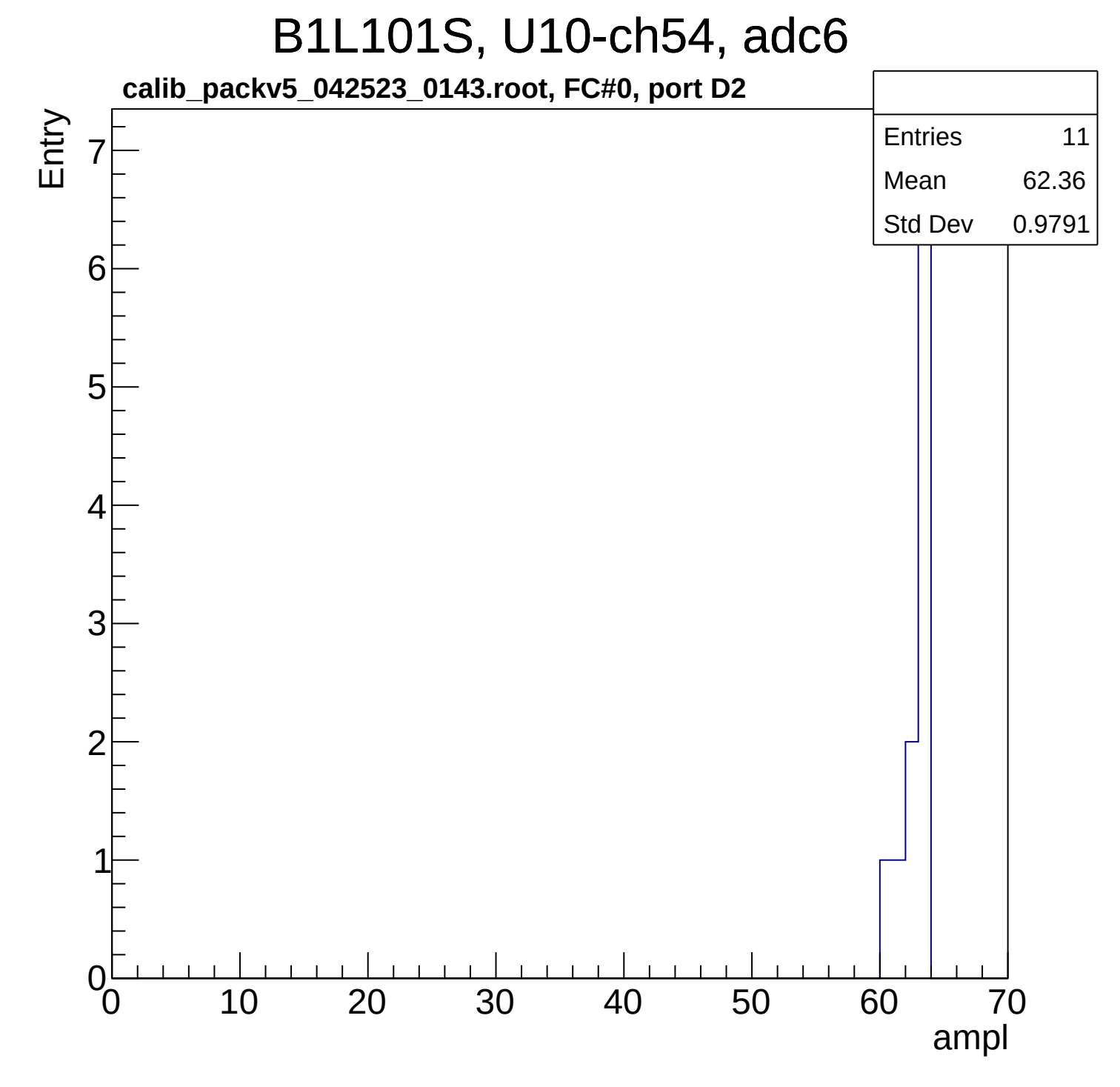
B1L101S, U10-ch54, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 11
Mean 62.36
Std Dev 0.9791
Entry
ampl
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1
2
3
4
5
6
7
0
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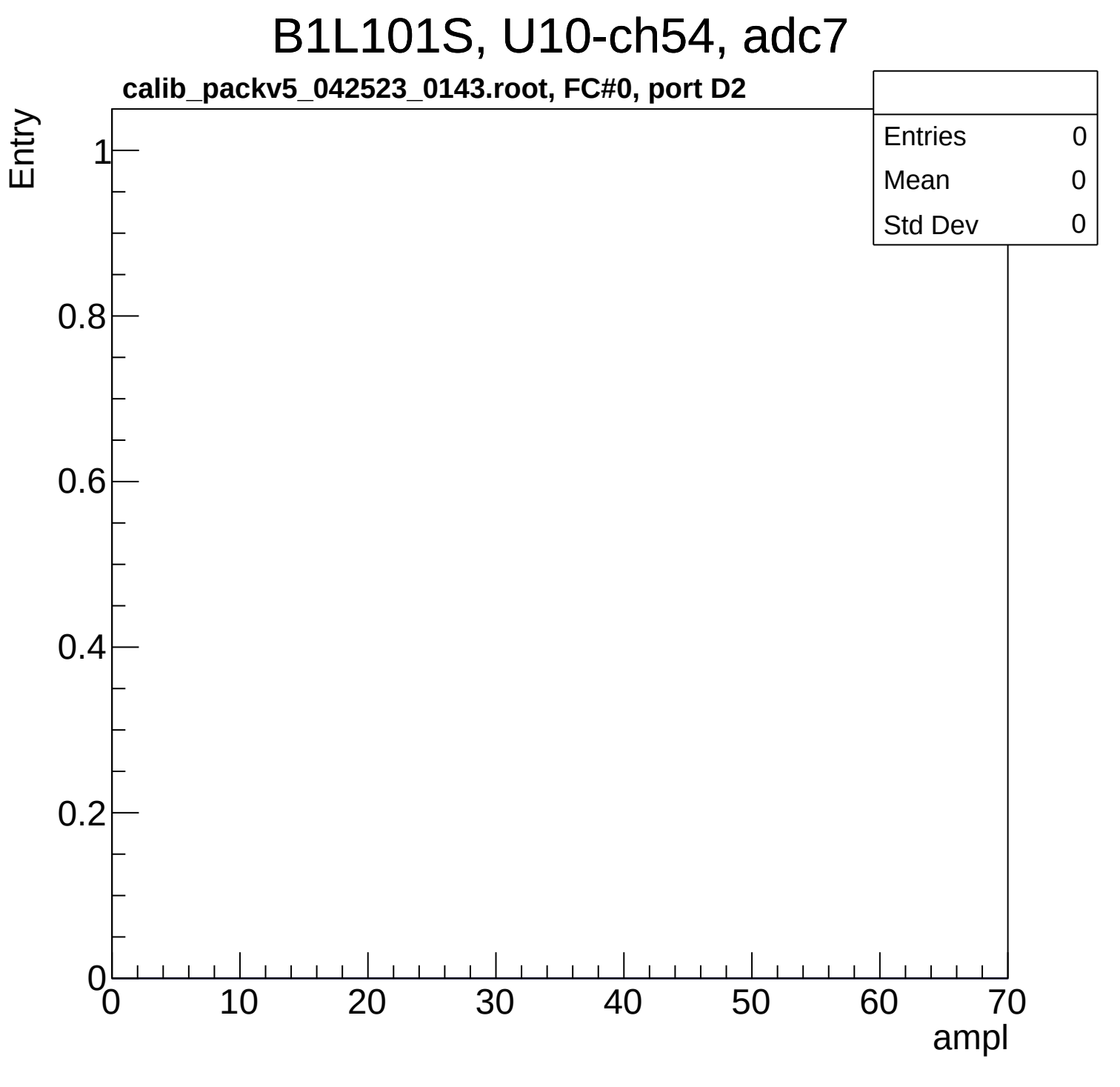
B1L101S, U10-ch54, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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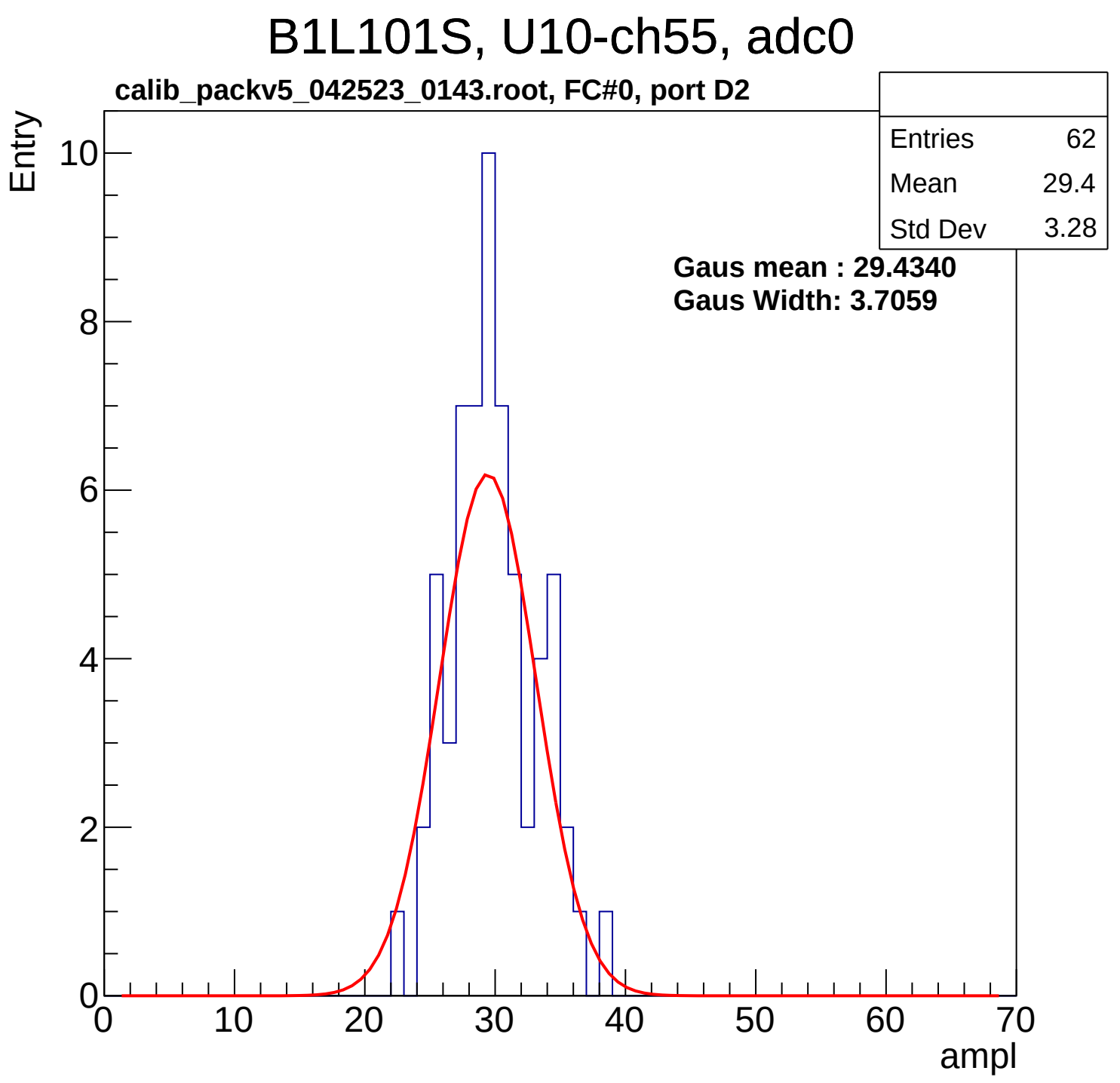
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch55, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 29.4
Std Dev 3.28
Gaus mean : 29.4340
Gaus Width: 3.7059
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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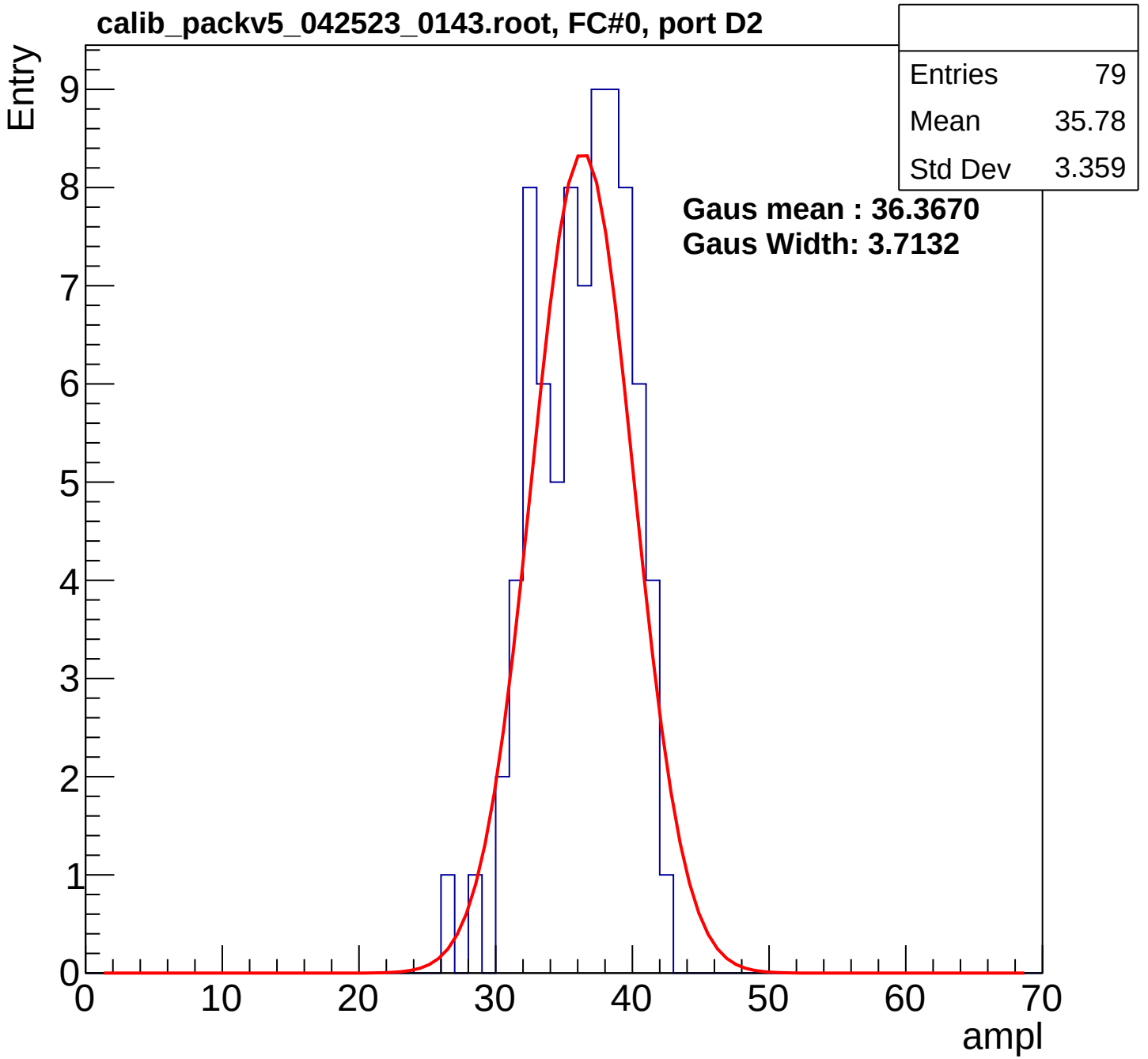
B1L101S, U10-ch55, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 35.78
Std Dev 3.359
Gaus mean : 36.3670
Gaus Width: 3.7132
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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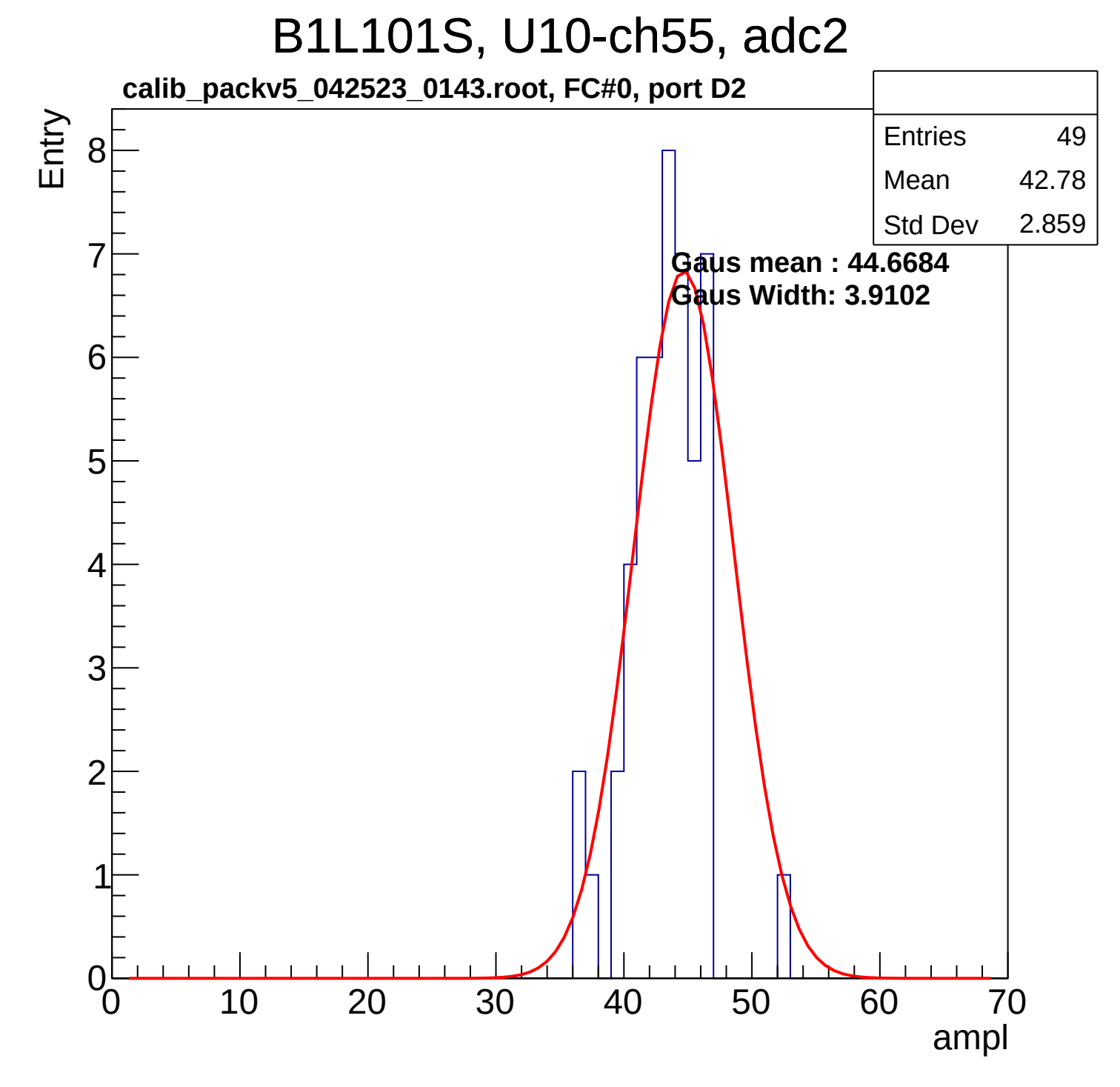
B1L101S, U10-ch55, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 42.78
Std Dev 2.859
Gaus mean : 44.6684
Gaus Width: 3.9102
Entry
ampl
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1
2
3
4
5
6
7
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0
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40
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60
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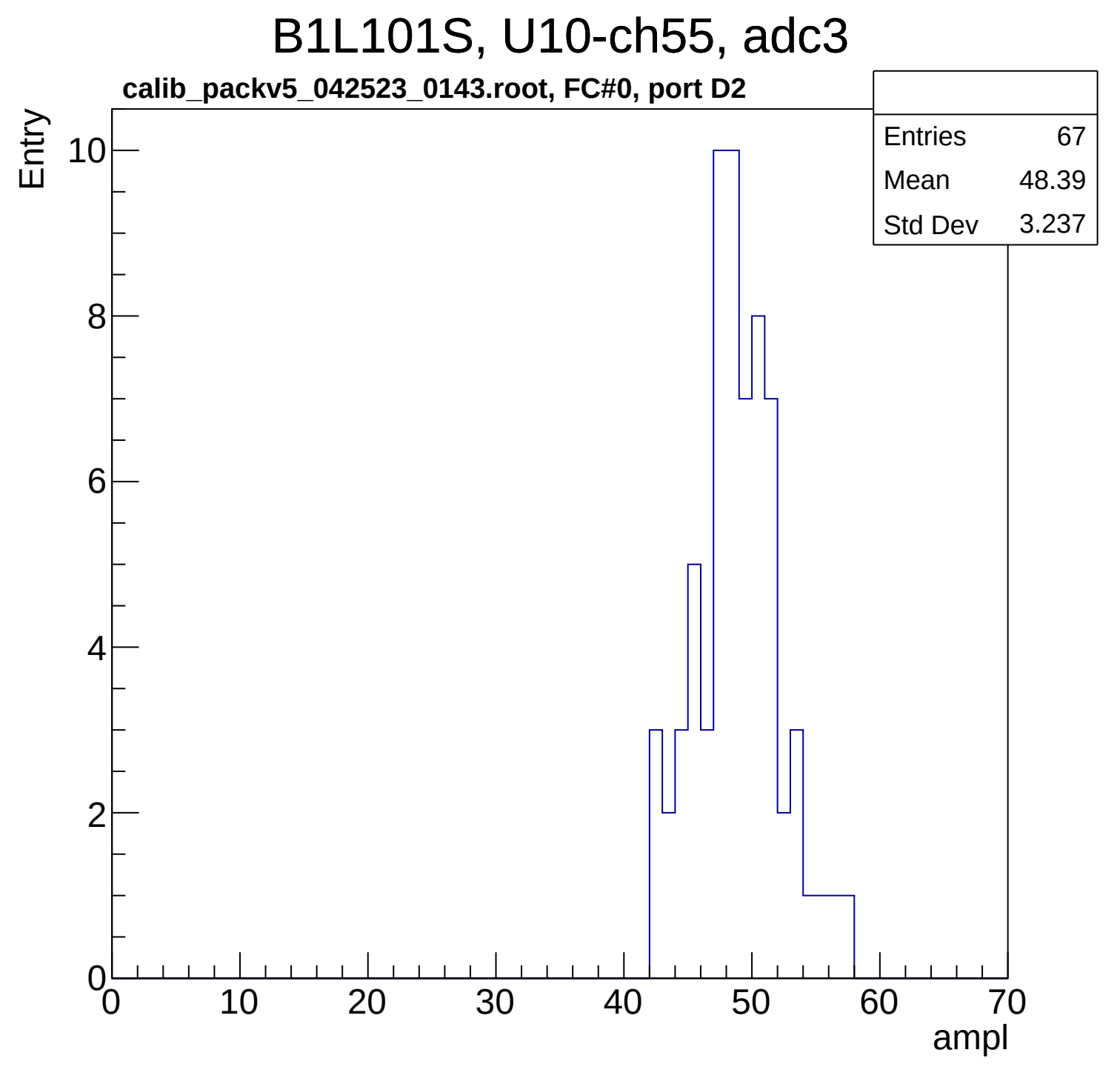
B1L101S, U10-ch55, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 48.39
Std Dev 3.237
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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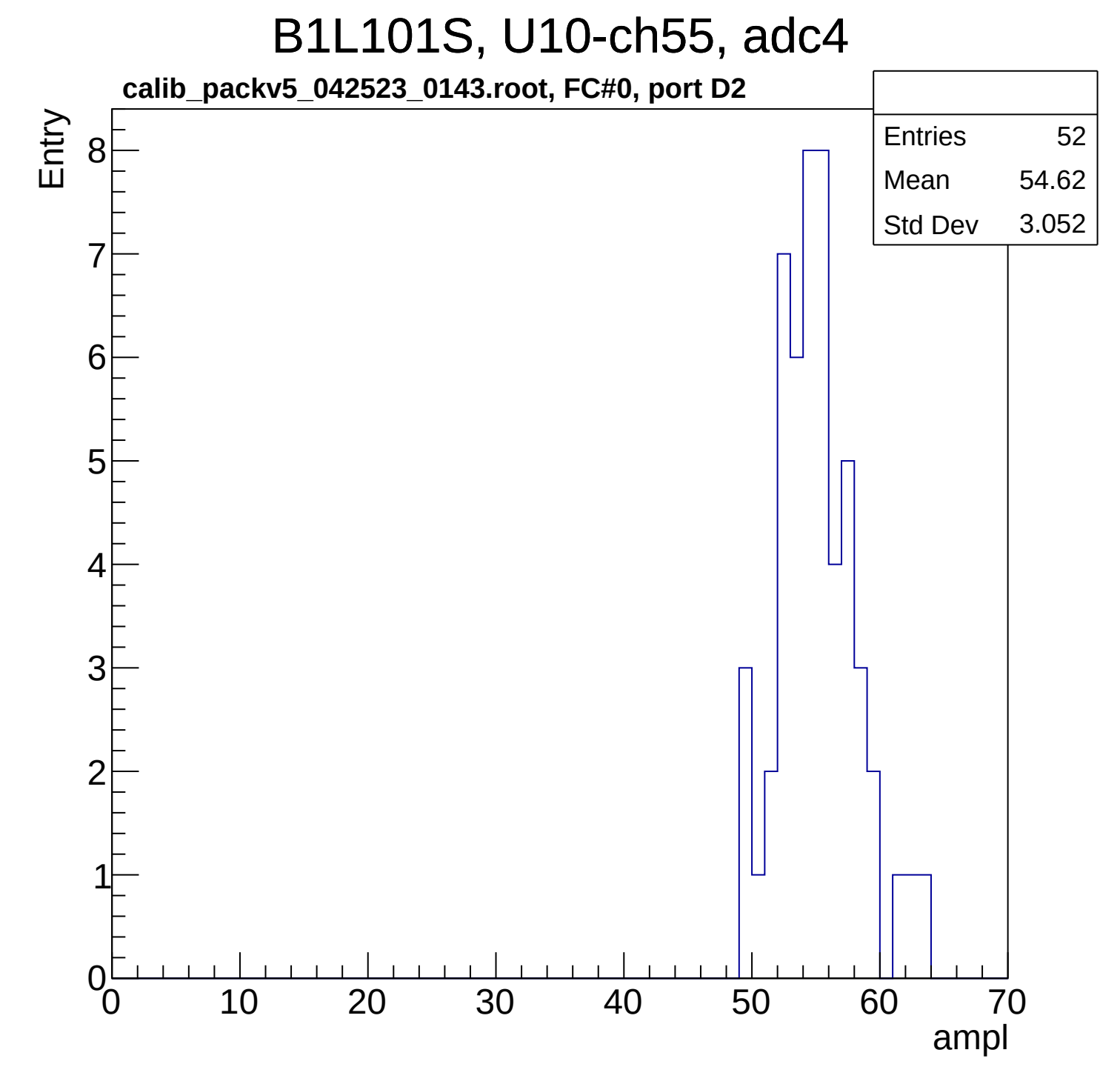
B1L101S, U10-ch55, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 54.62
Std Dev 3.052
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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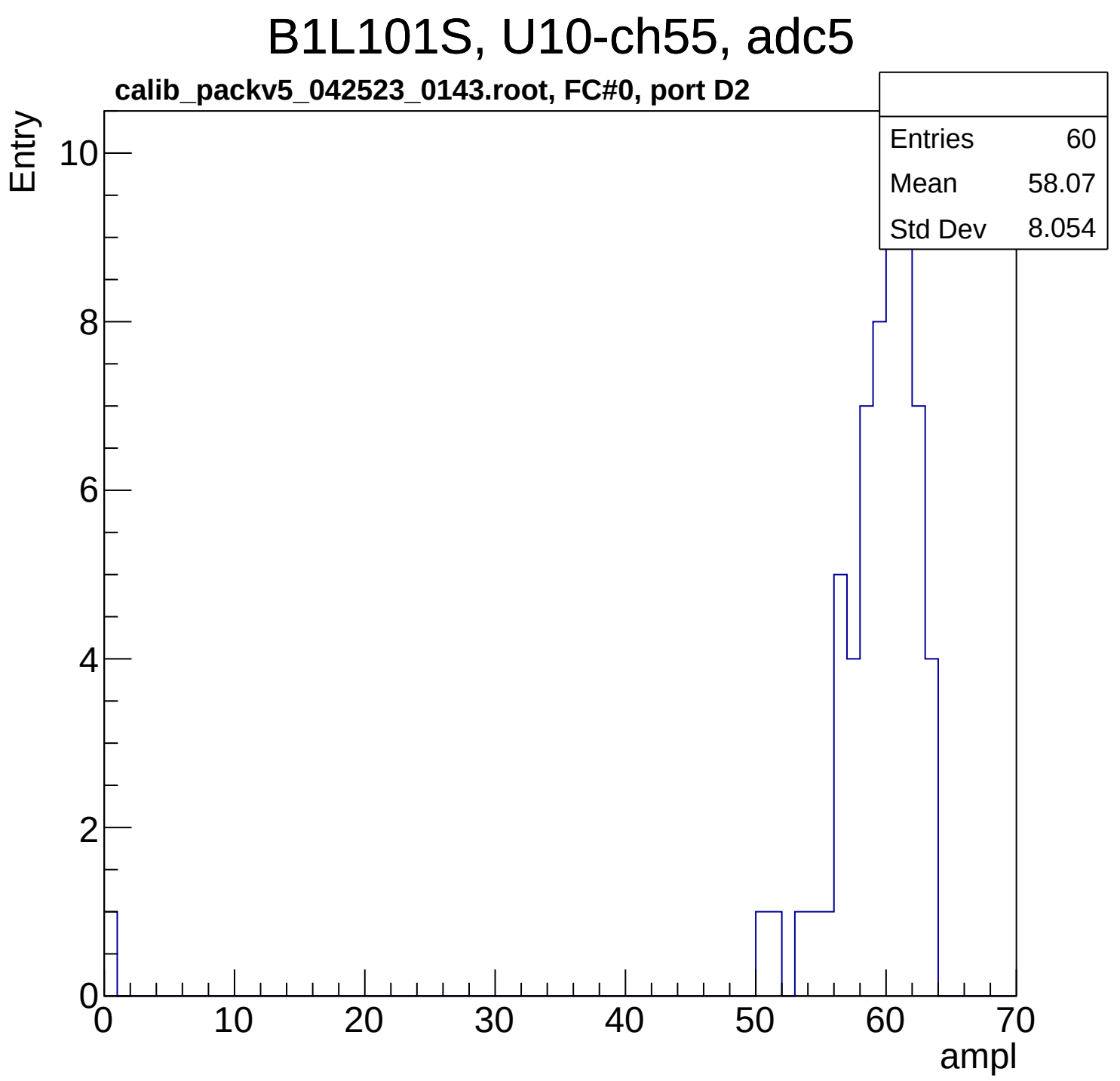
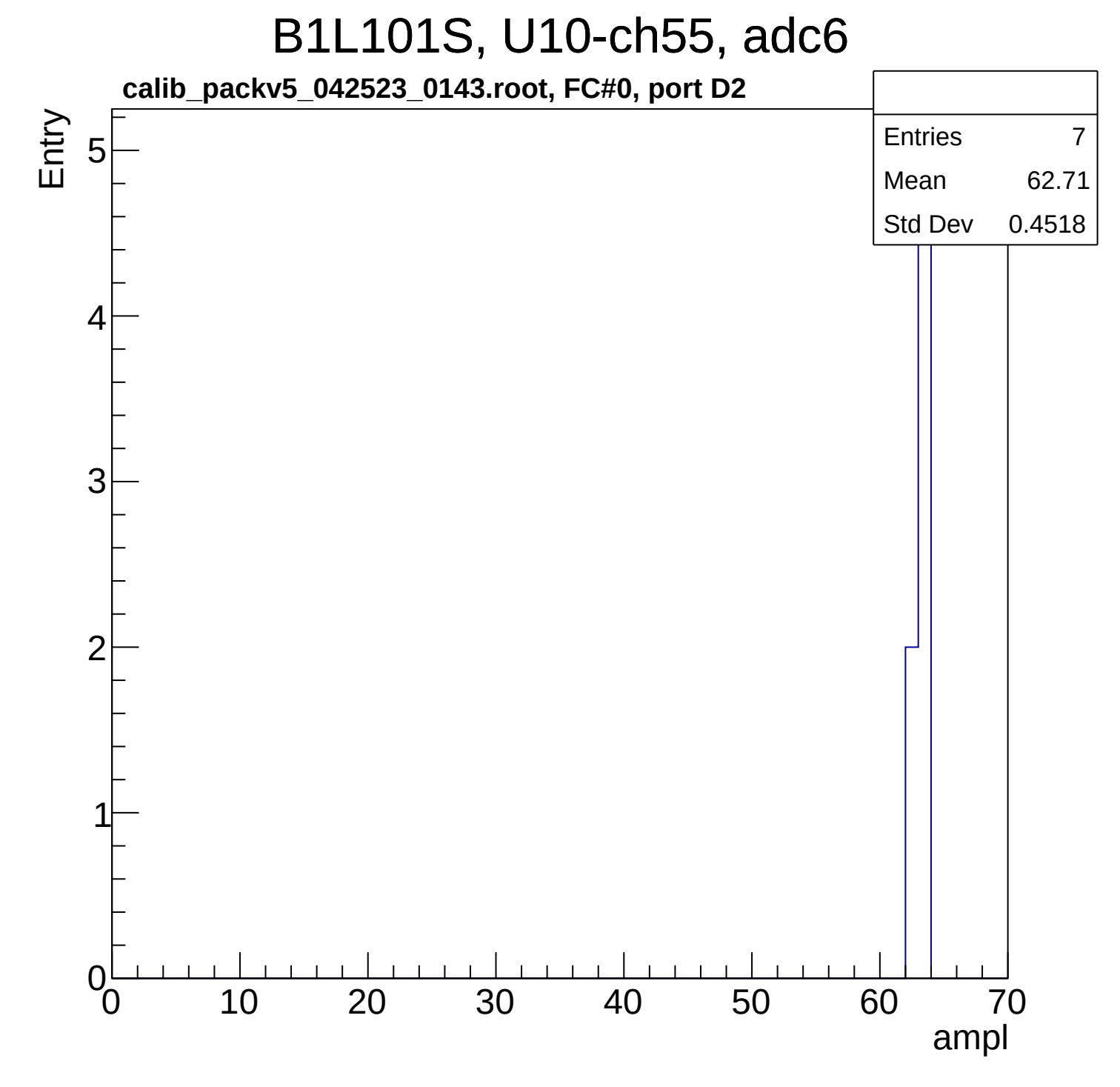

B1L101S, U10-ch55, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 58.07
Std Dev 8.054
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch55, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 62.71
Std Dev 0.4518
Entry
ampl
0
1
2
3
4
5
0
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20
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40
50
60
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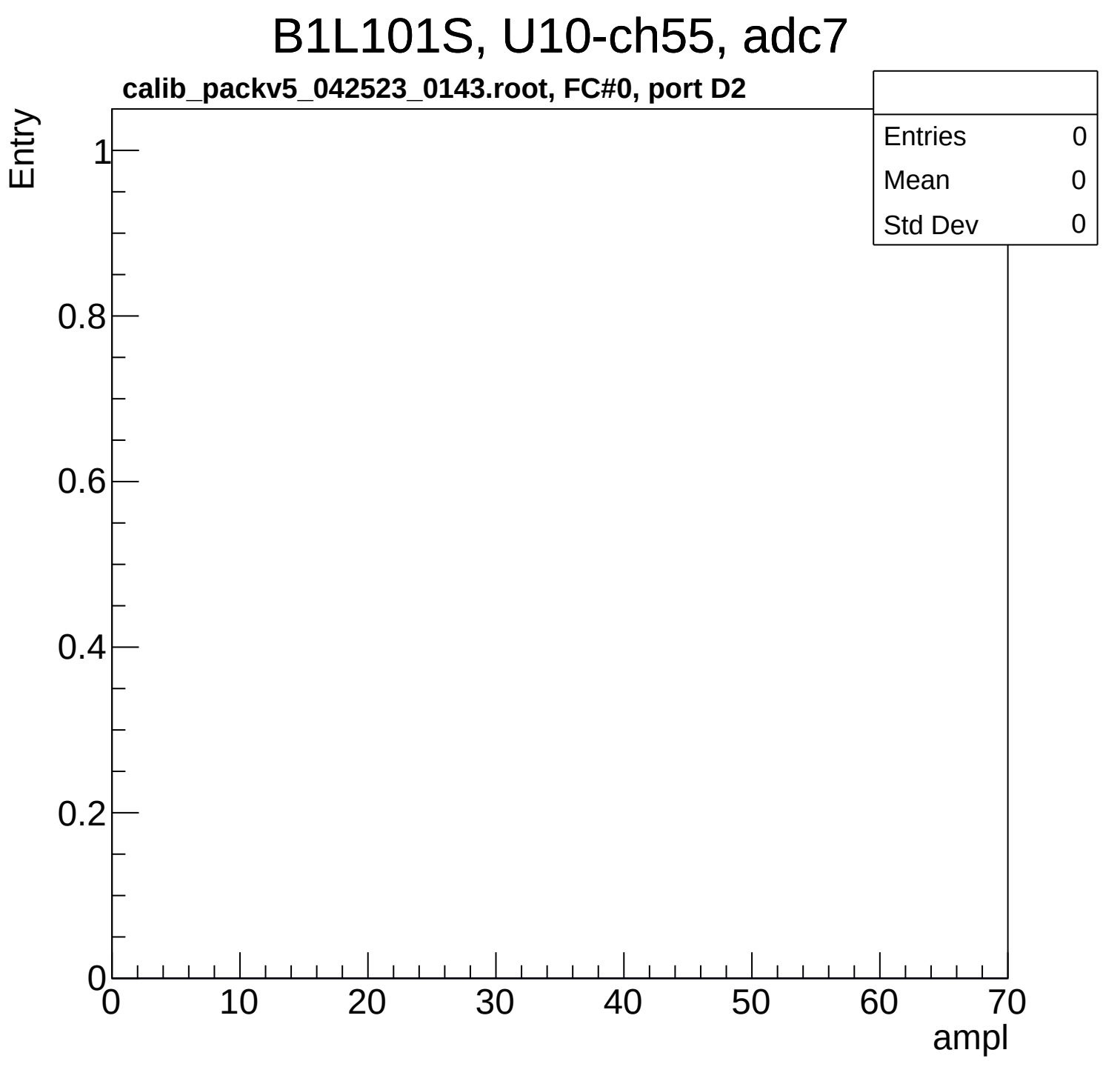
B1L101S, U10-ch55, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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0.8
0.6
0.4
0.2
0
0
10
20
30
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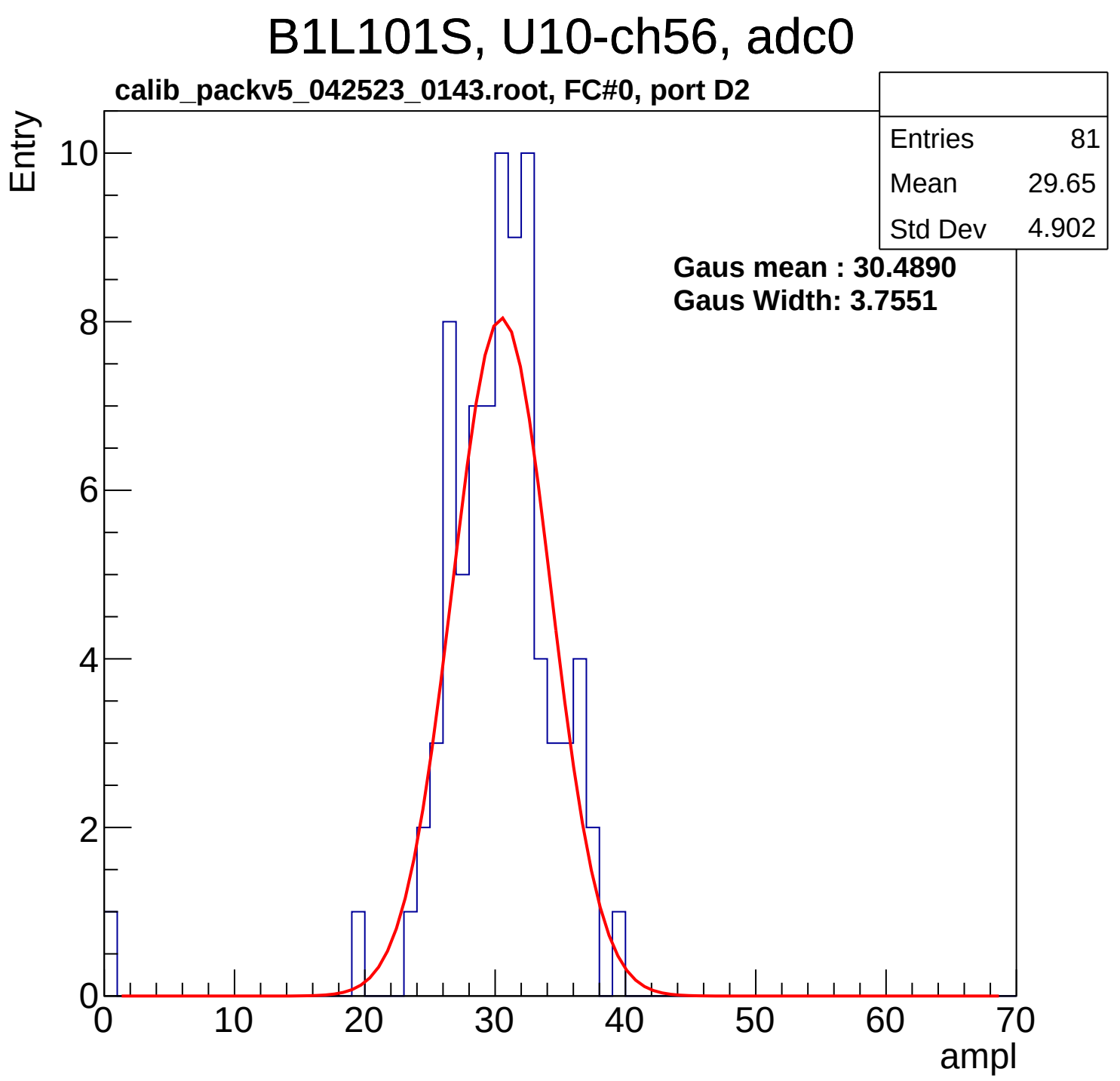
50
60
70
ampl


B1L101S, U10-ch56, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 81
Mean 29.65
Std Dev 4.902
Gaus mean : 30.4890
Gaus Width: 3.7551
Entry
ampl
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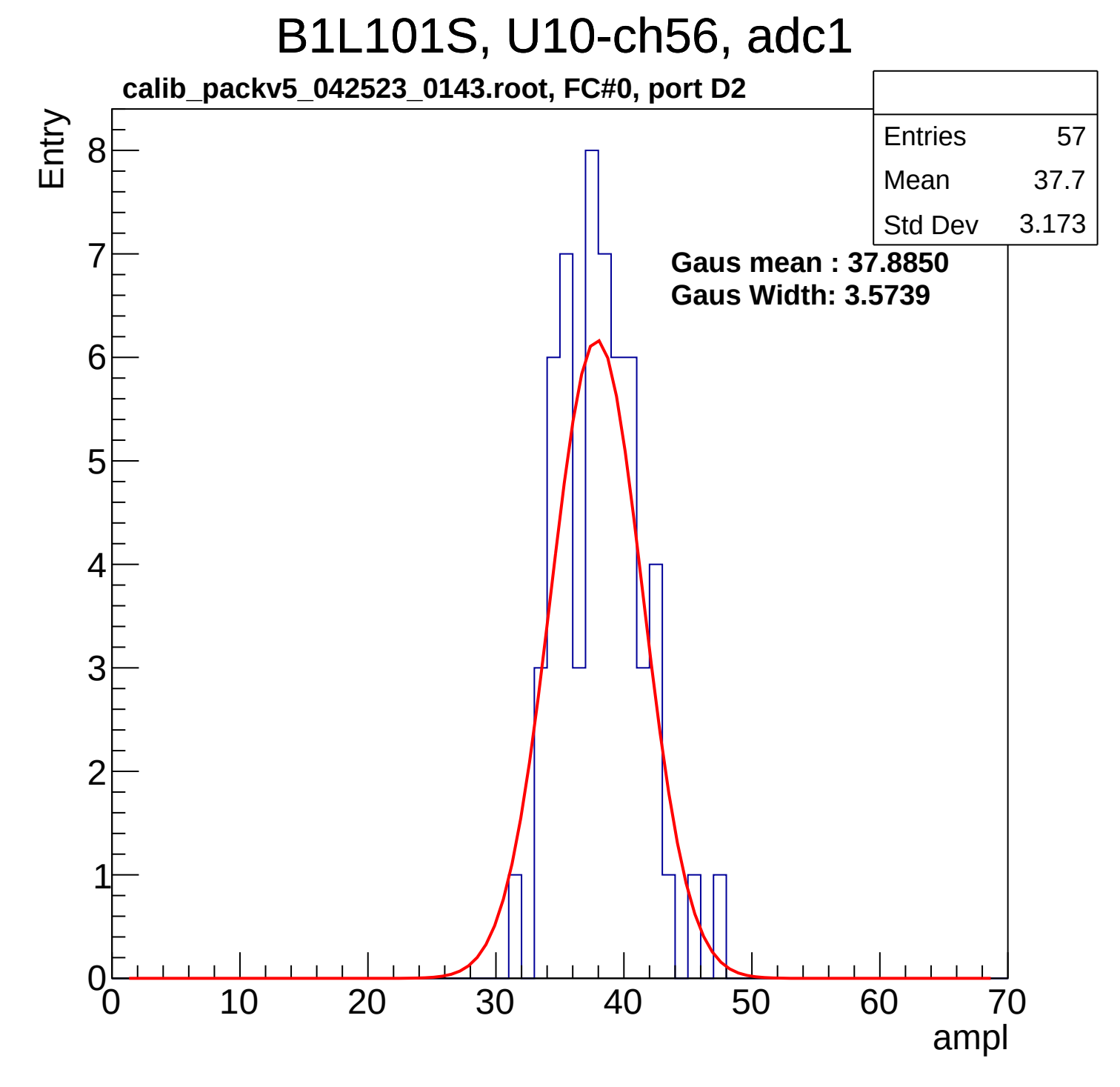
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch56, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 37.7
Std Dev 3.173
Gaus mean : 37.8850
Gaus Width: 3.5739
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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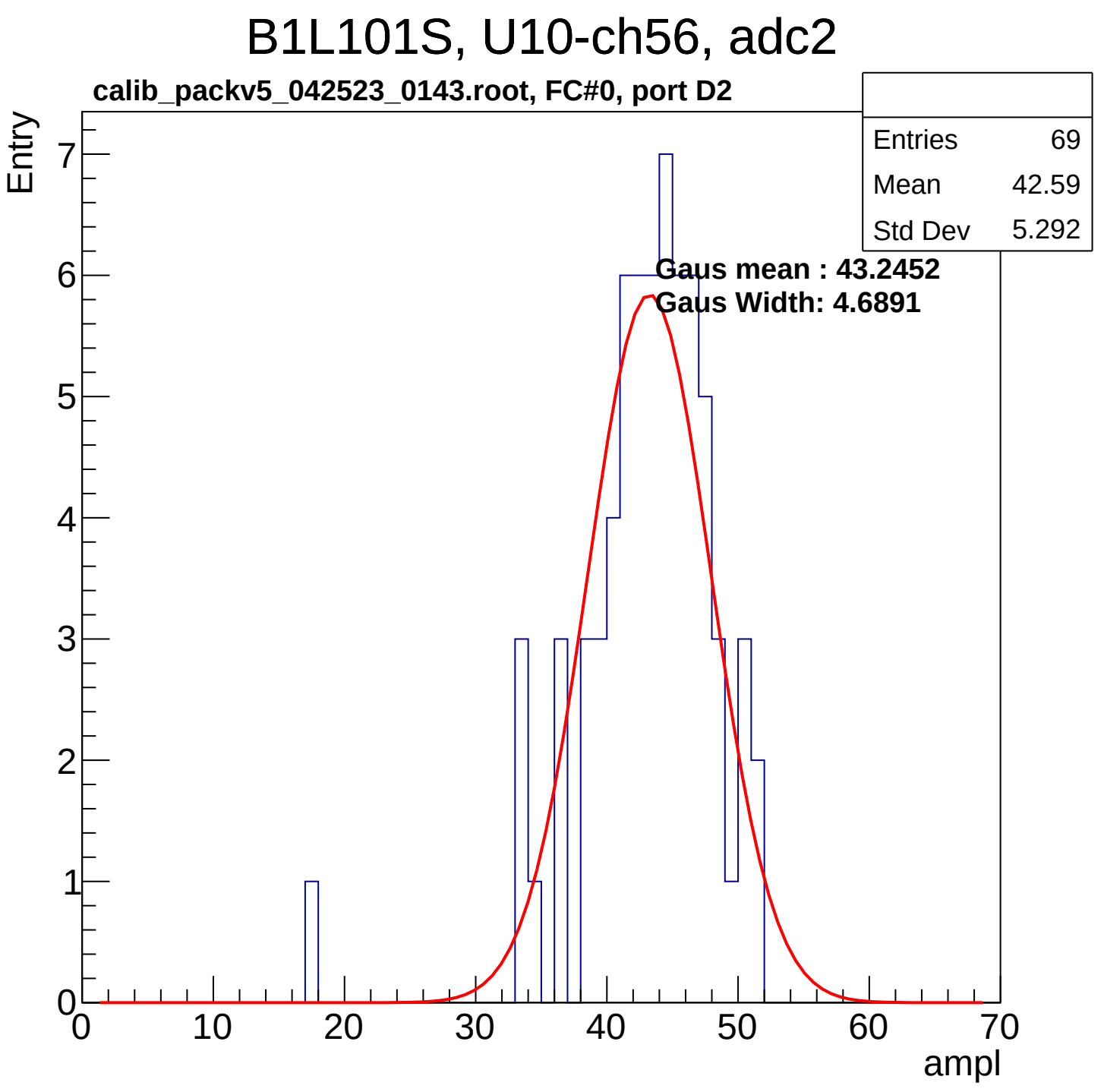
B1L101S, U10-ch56, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 42.59
Std Dev 5.292
Gaus mean : 43.2452
Gaus Width: 4.6891
Entry
ampl
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3
4
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6
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0
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60
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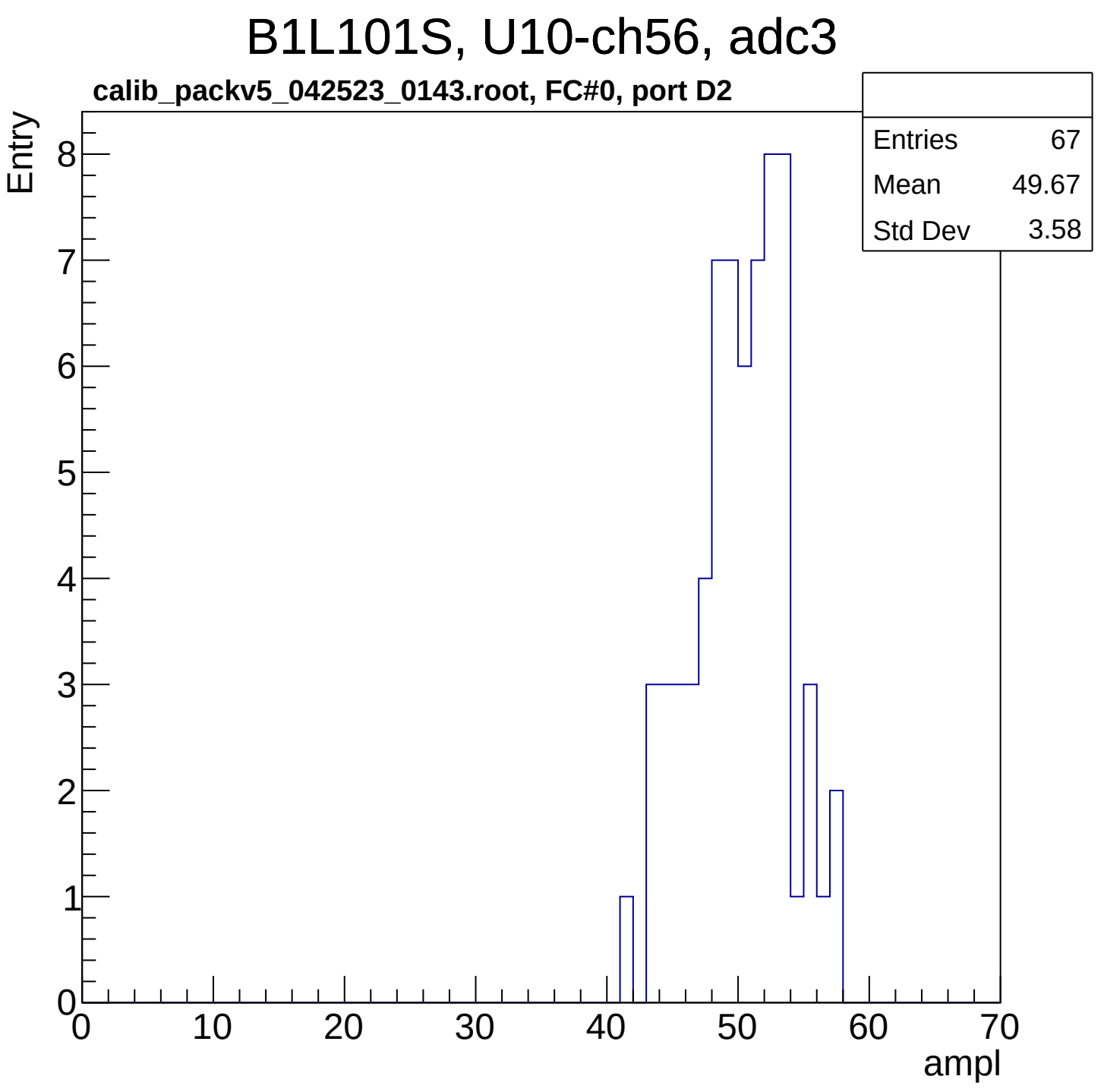
B1L101S, U10-ch56, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 49.67
Std Dev 3.58
Entry
ampl
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60
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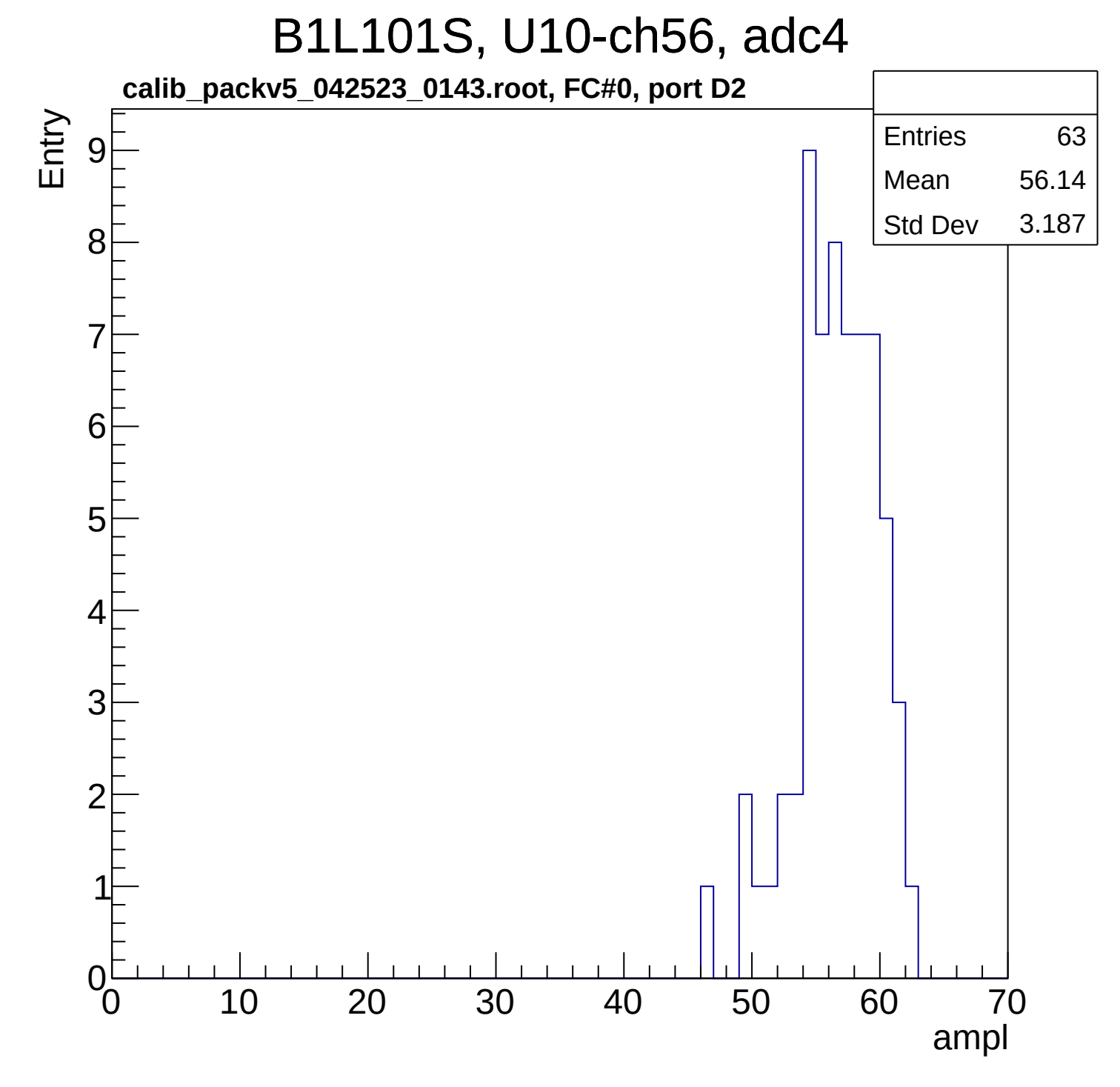
B1L101S, U10-ch56, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 56.14
Std Dev 3.187
Entry
ampl
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6
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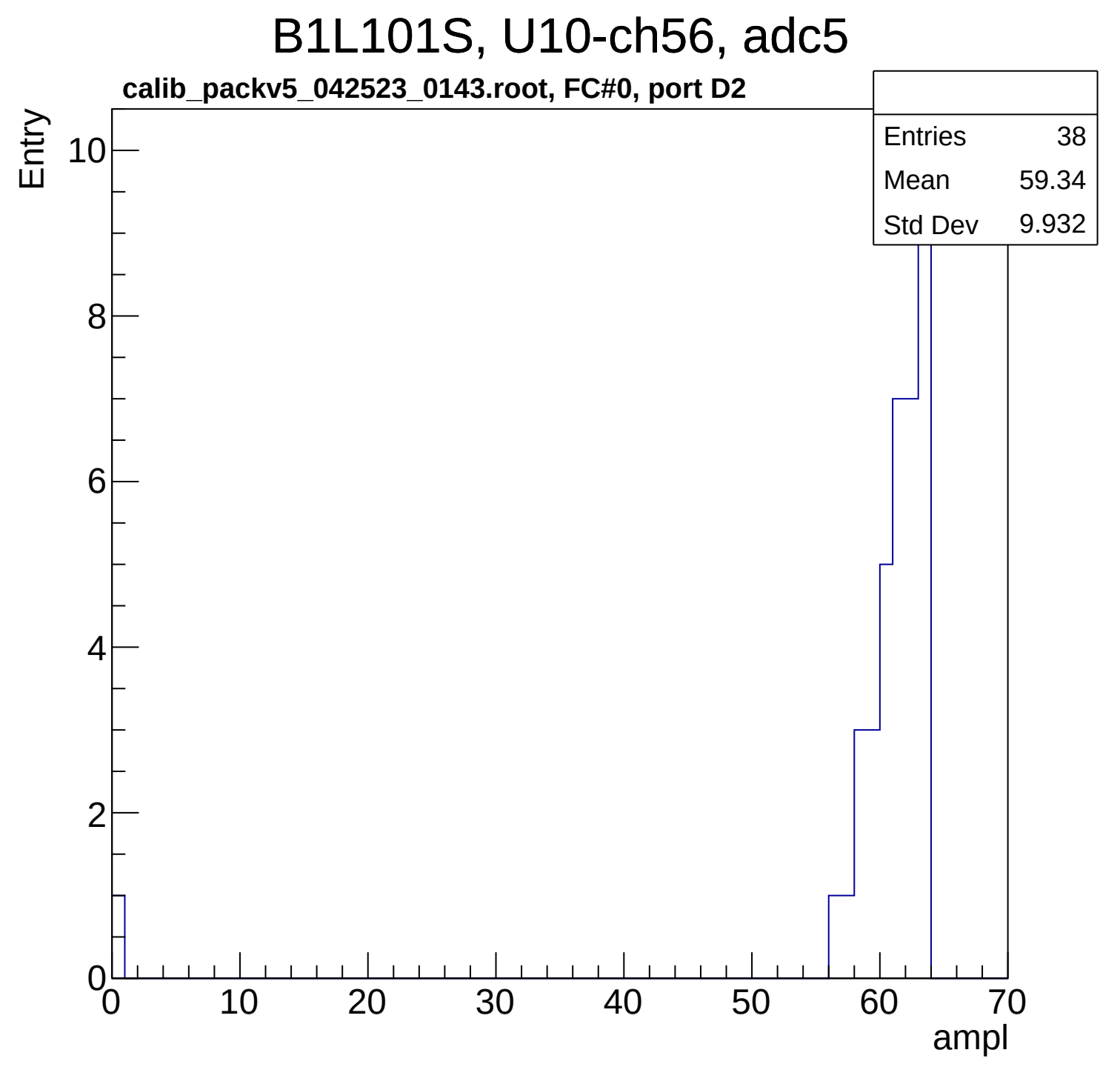
B1L101S, U10-ch56, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 38
Mean 59.34
Std Dev 9.932
Entry
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2
4
6
8
10
0
10
20
30
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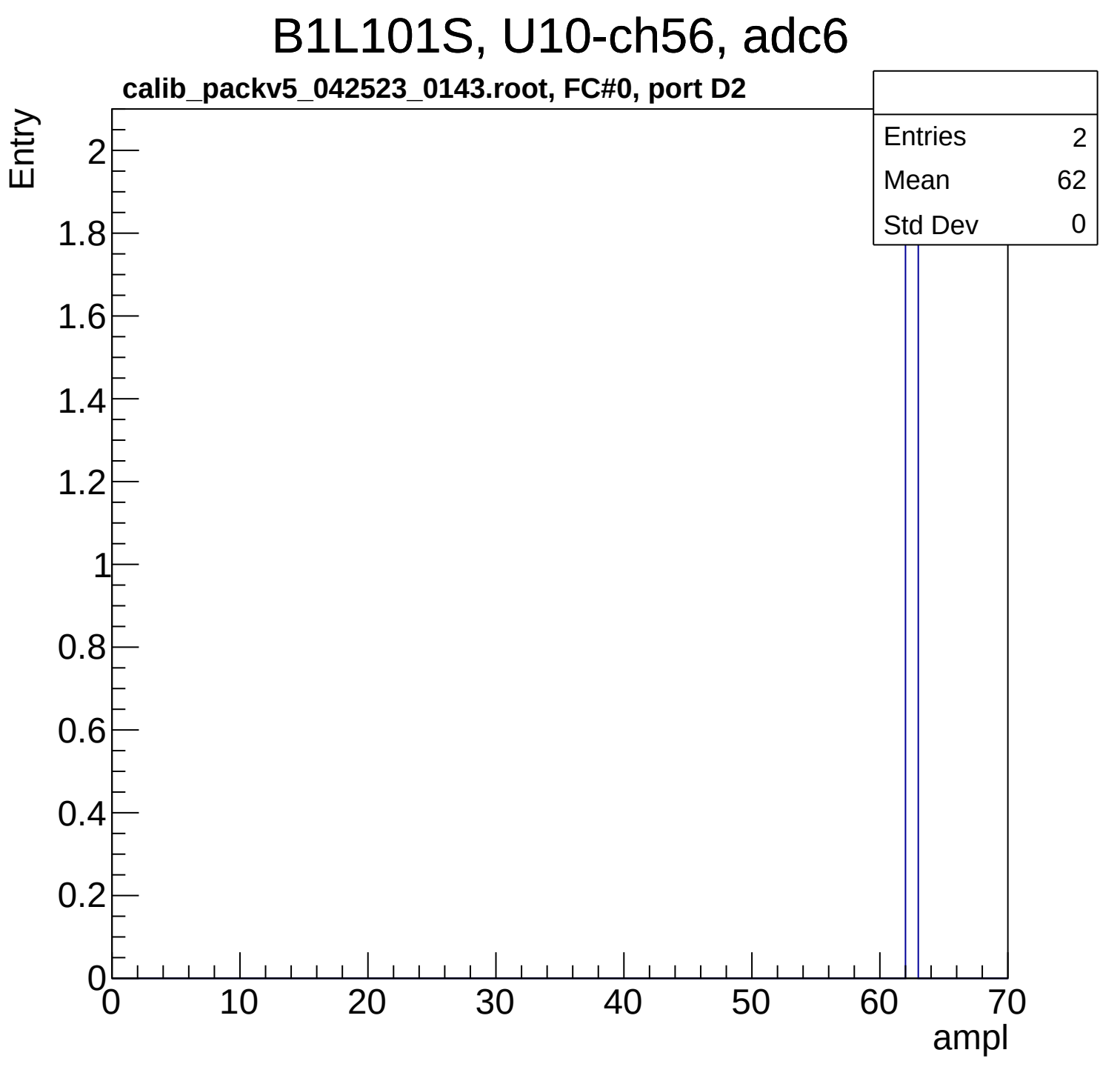
50
60
70
ampl


B1L101S, U10-ch56, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 62
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
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1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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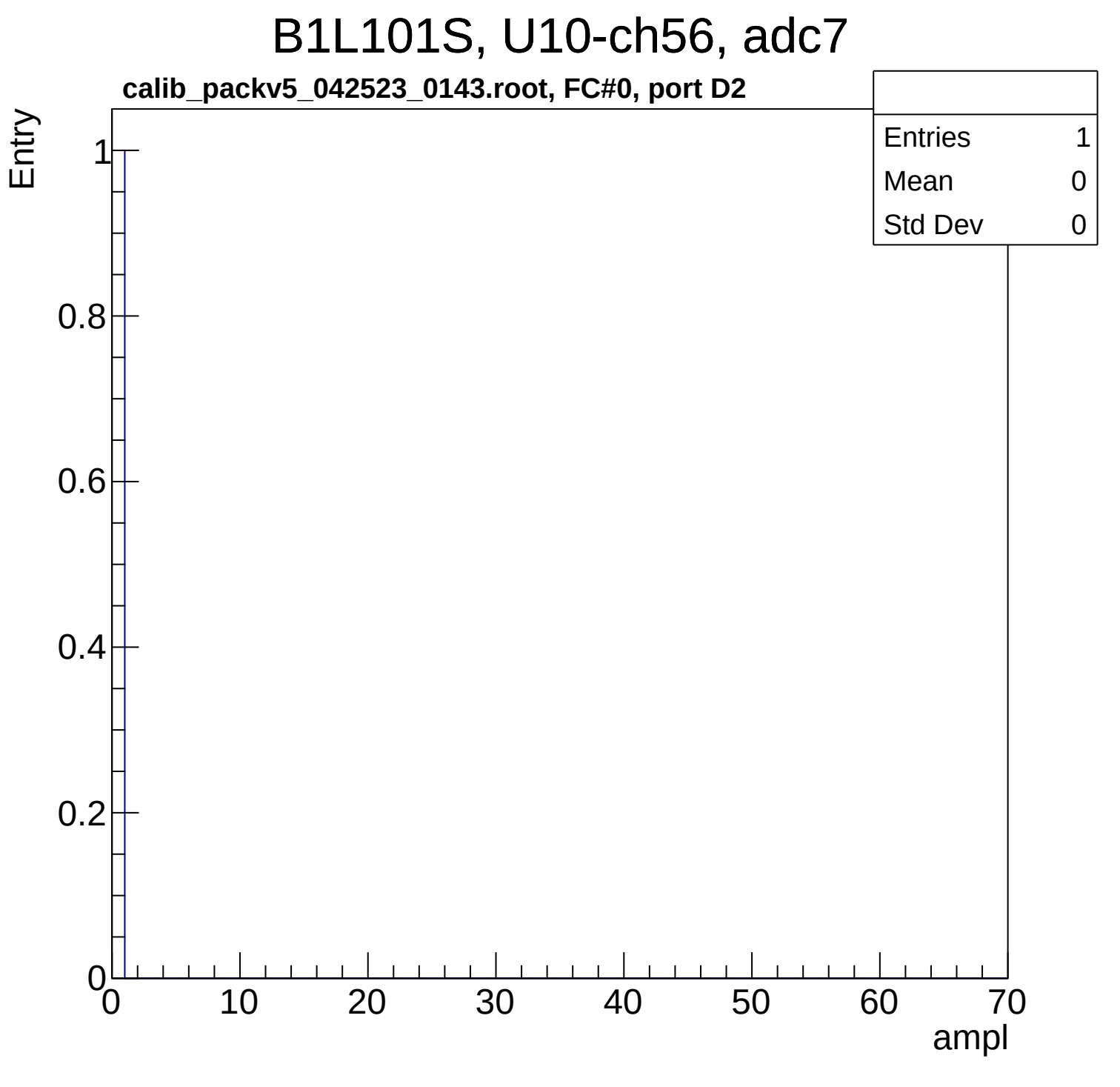
B1L101S, U10-ch56, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
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0.6
0.4
0.2
0
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10
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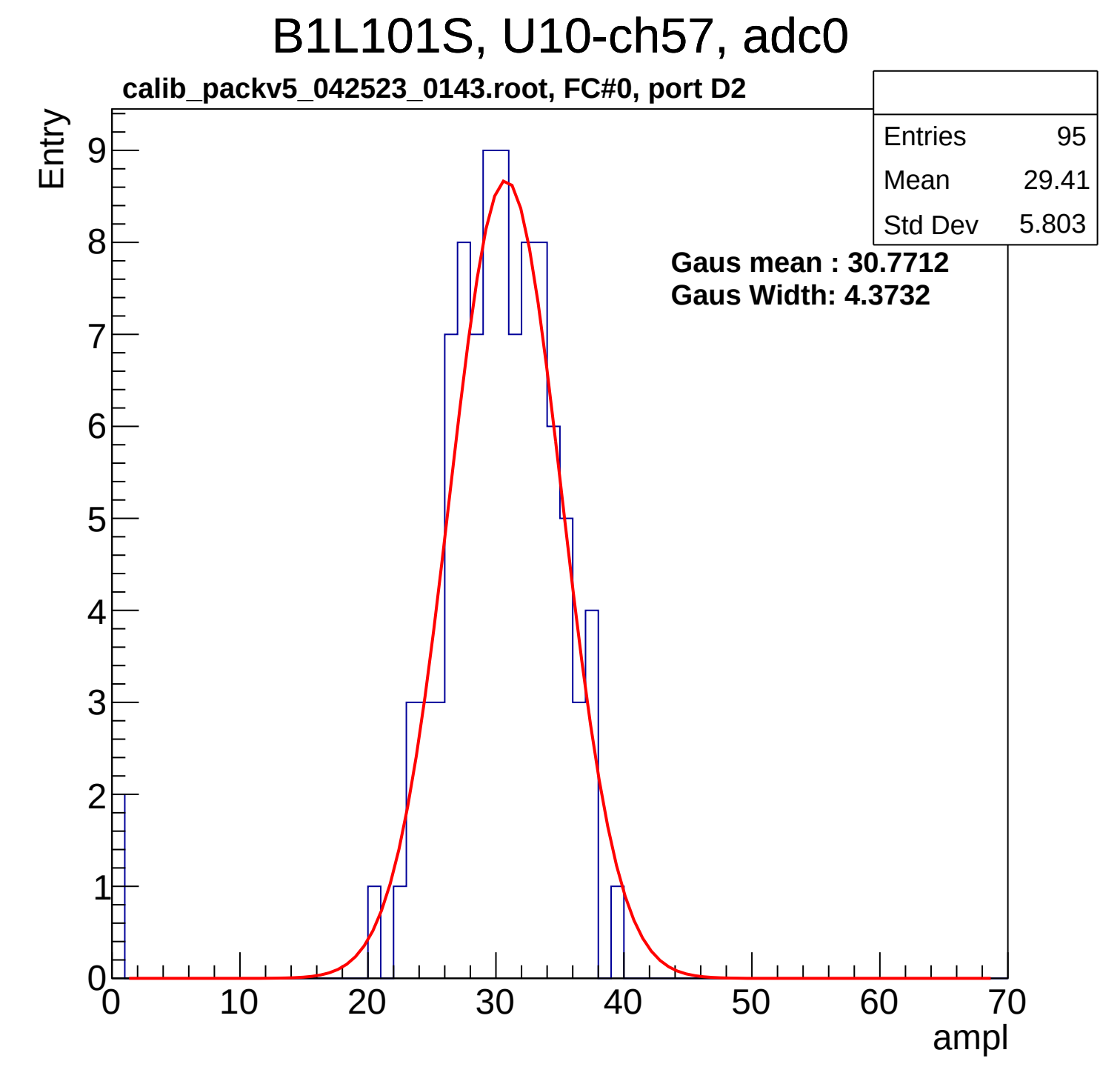
50
60
70
ampl


B1L101S, U10-ch57, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 95
Mean 29.41
Std Dev 5.803
Gaus mean : 30.7712
Gaus Width: 4.3732
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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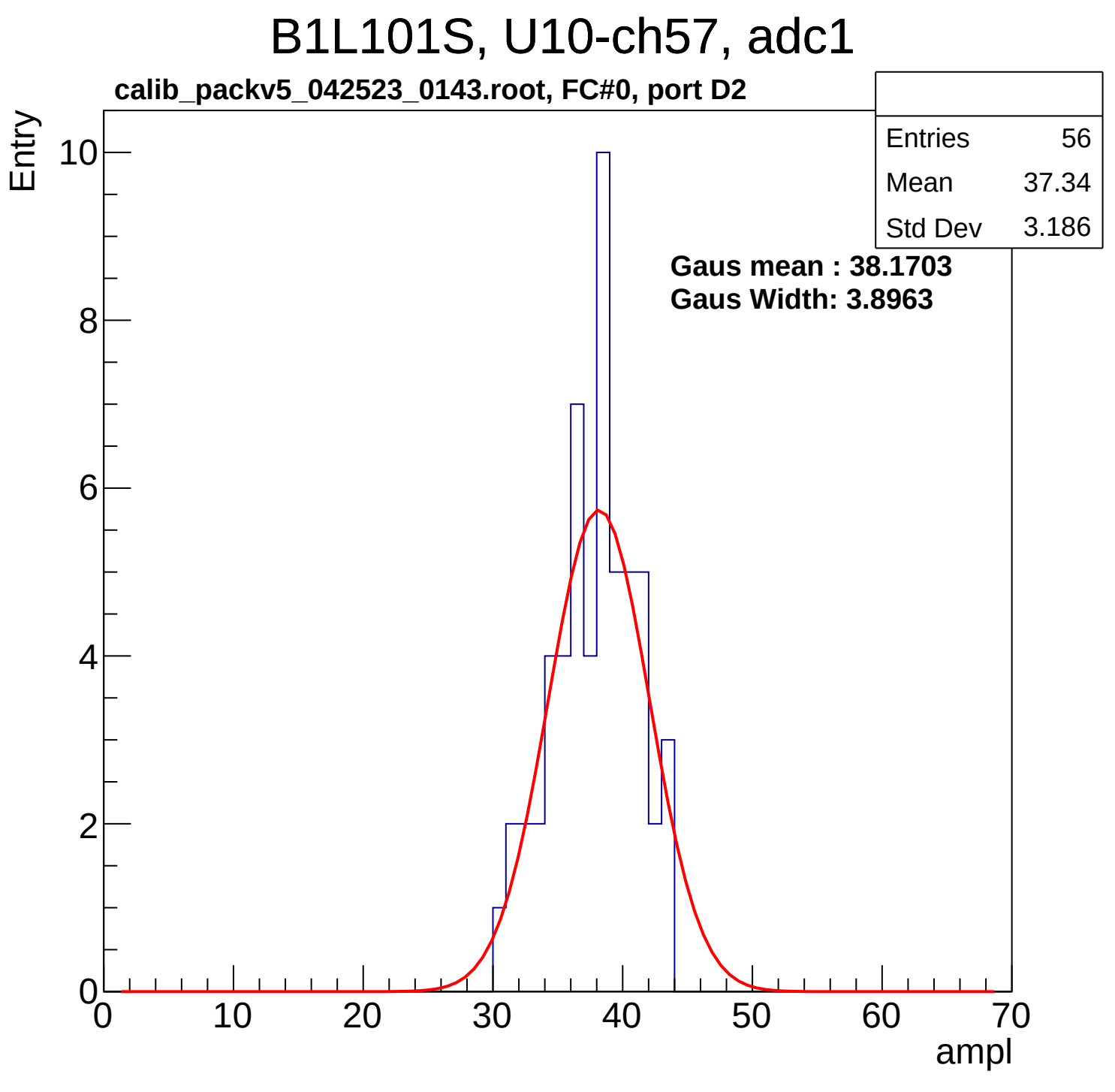
B1L101S, U10-ch57, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 37.34
Std Dev 3.186
Gaus mean : 38.1703
Gaus Width: 3.8963
Entry
ampl
0
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6
8
10
0
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20
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40
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60
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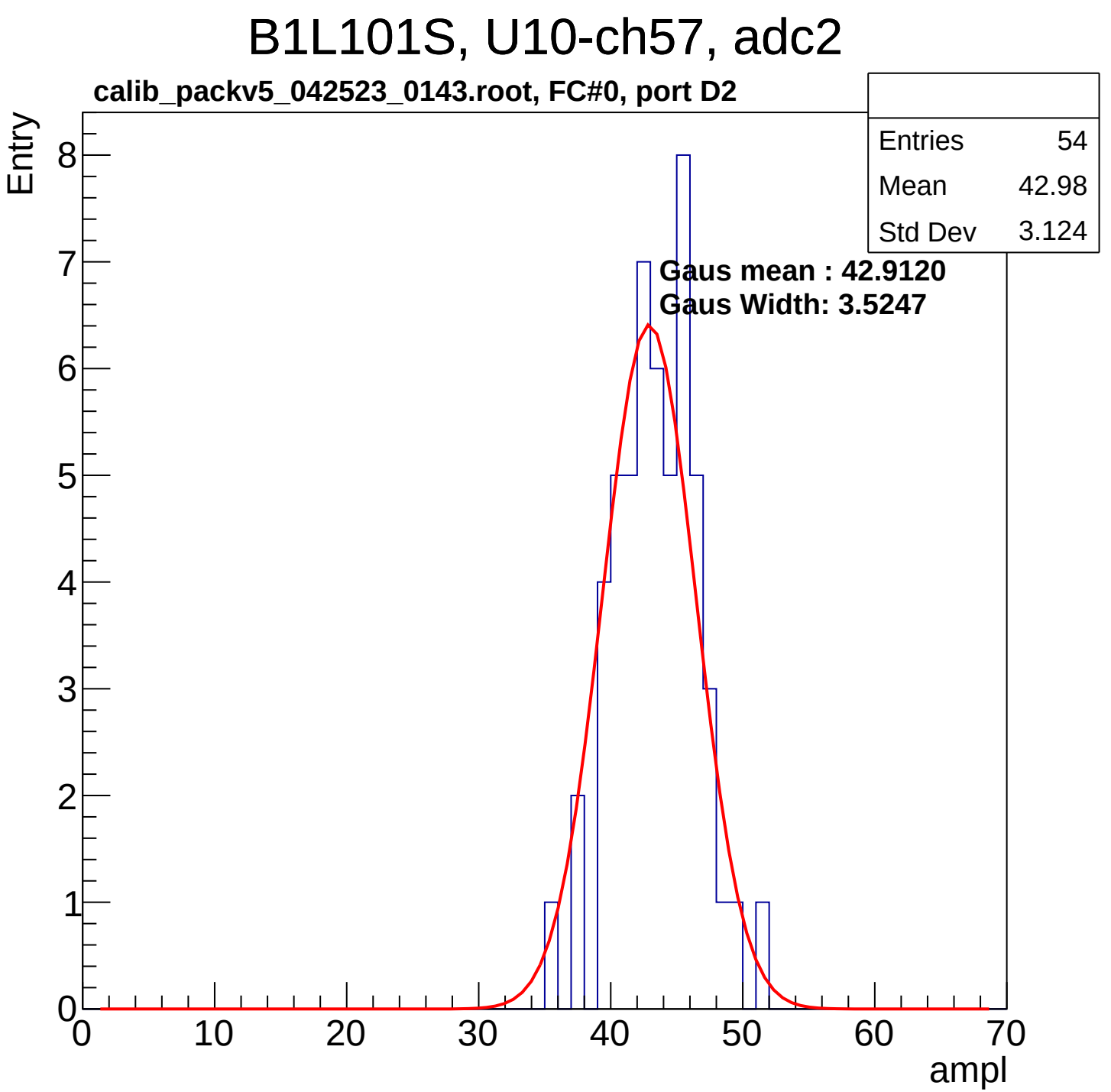
B1L101S, U10-ch57, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 42.98
Std Dev 3.124
Gaus mean : 42.9120
Gaus Width: 3.5247
Entry
ampl
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1
2
3
4
5
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7
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0
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40
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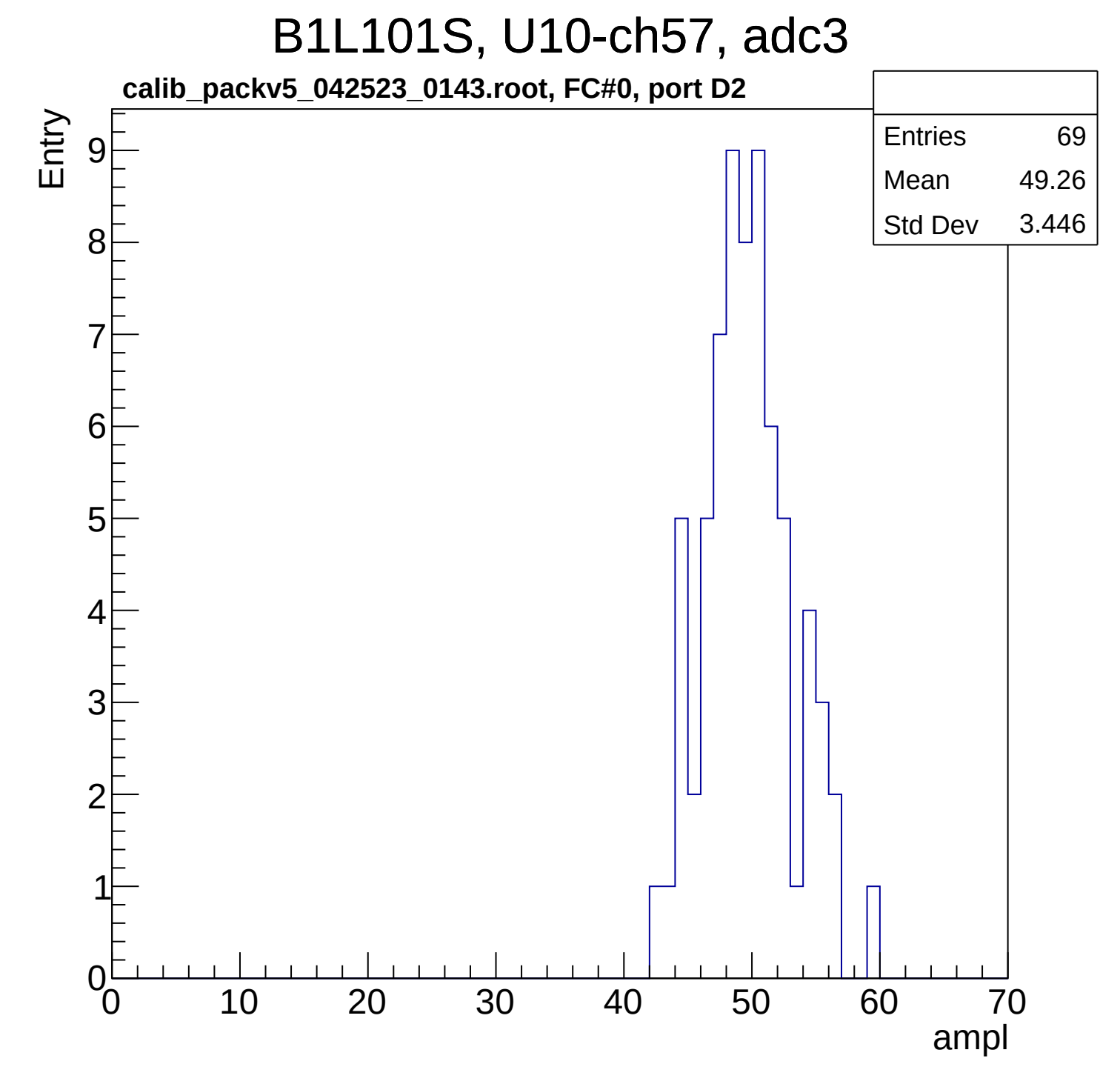
B1L101S, U10-ch57, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 49.26
Std Dev 3.446
Entry
ampl
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6
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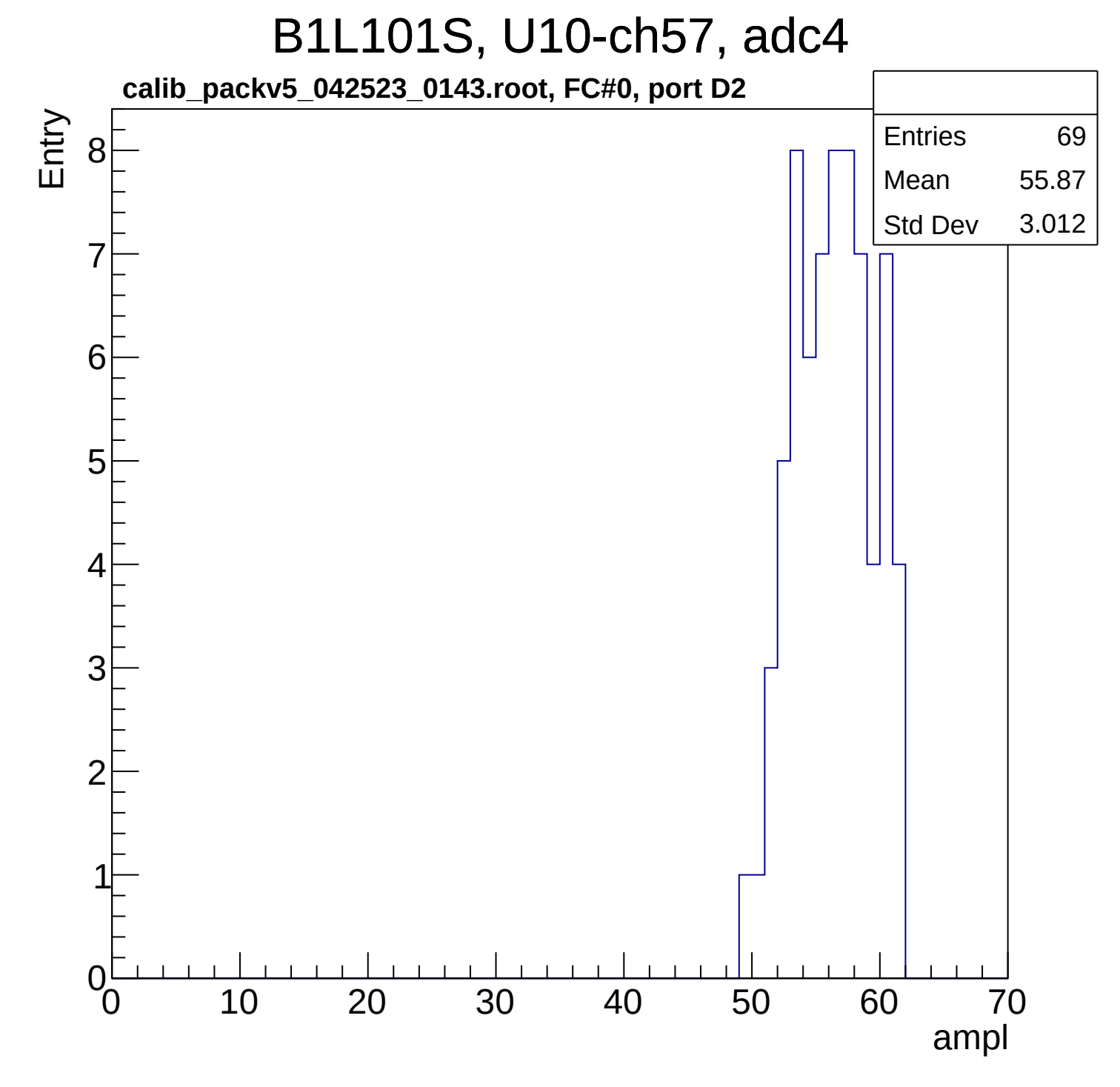
B1L101S, U10-ch57, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 55.87
Std Dev 3.012
Entry
ampl
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3
4
5
6
7
8
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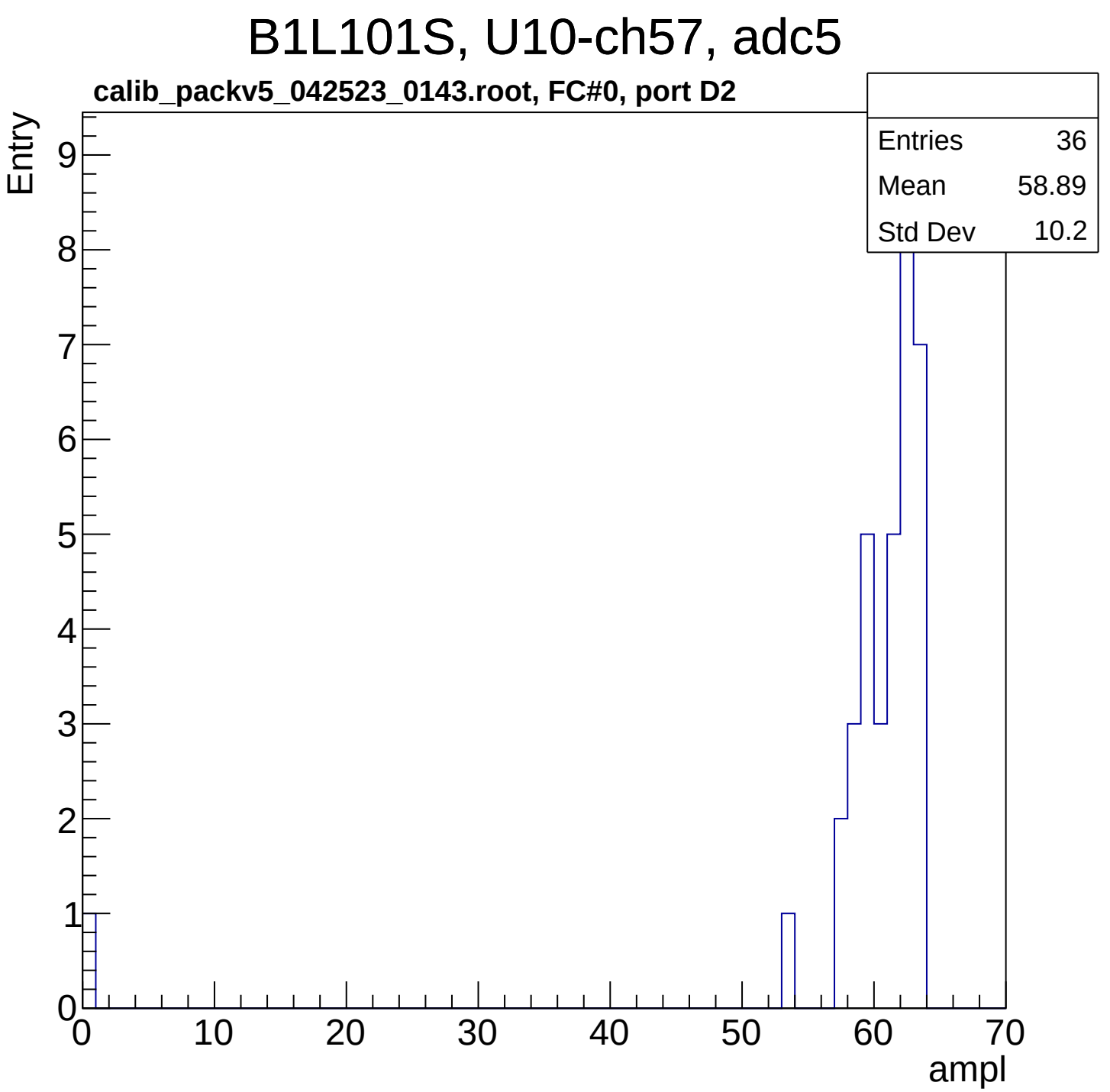
B1L101S, U10-ch57, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 36
Mean 58.89
Std Dev 10.2
Entry
ampl
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3
4
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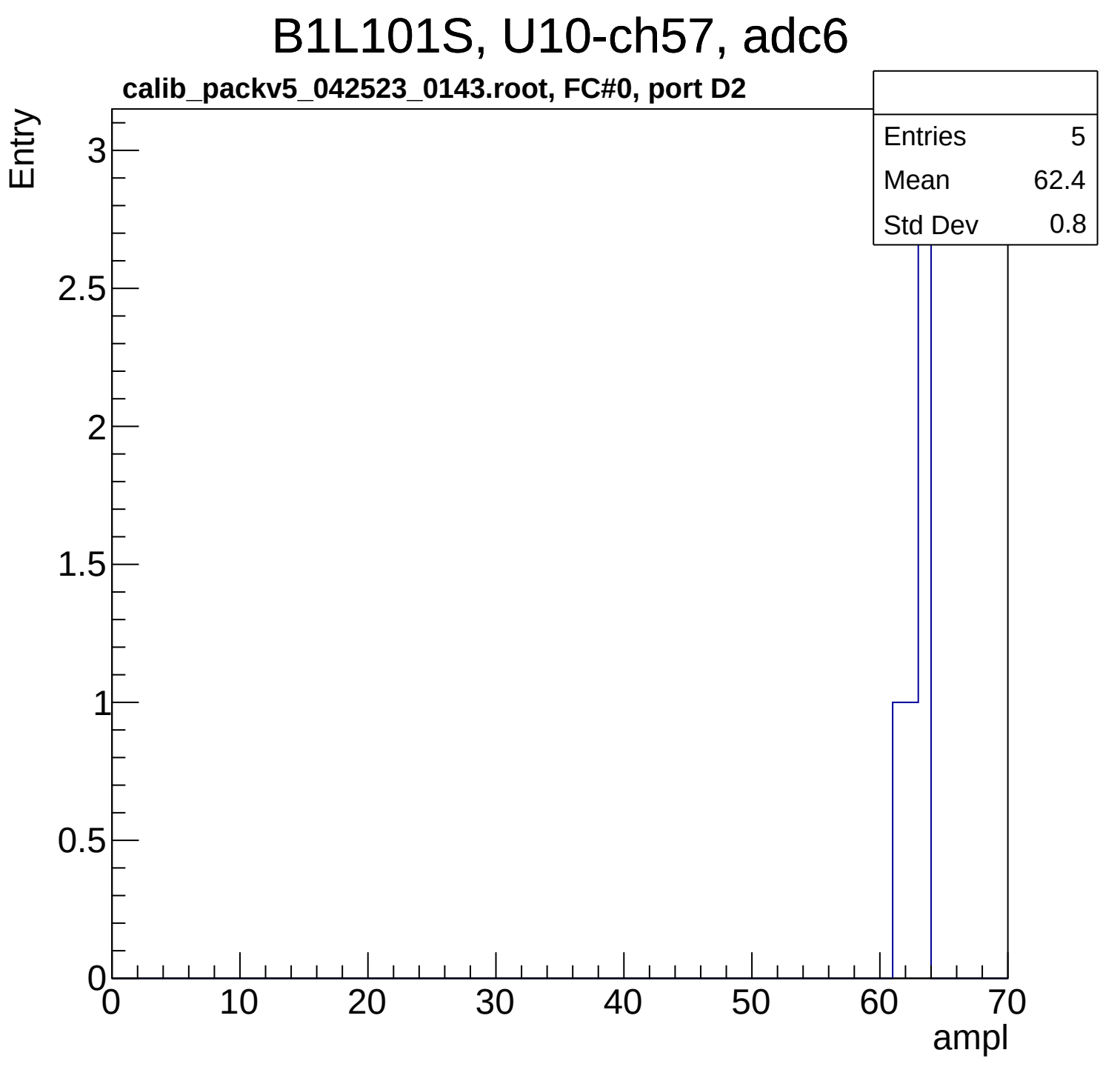
B1L101S, U10-ch57, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 62.4
Std Dev 0.8
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
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20
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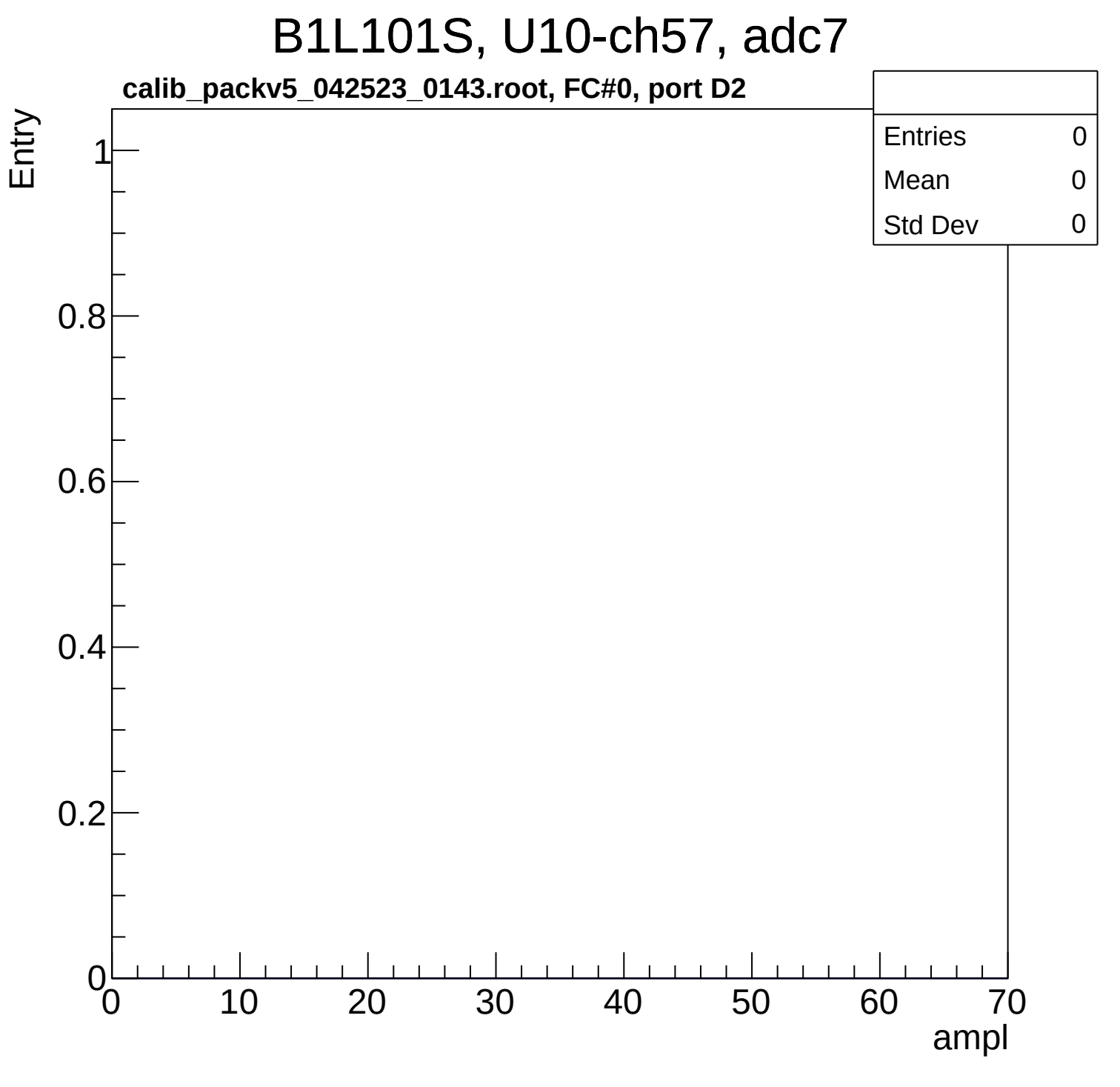
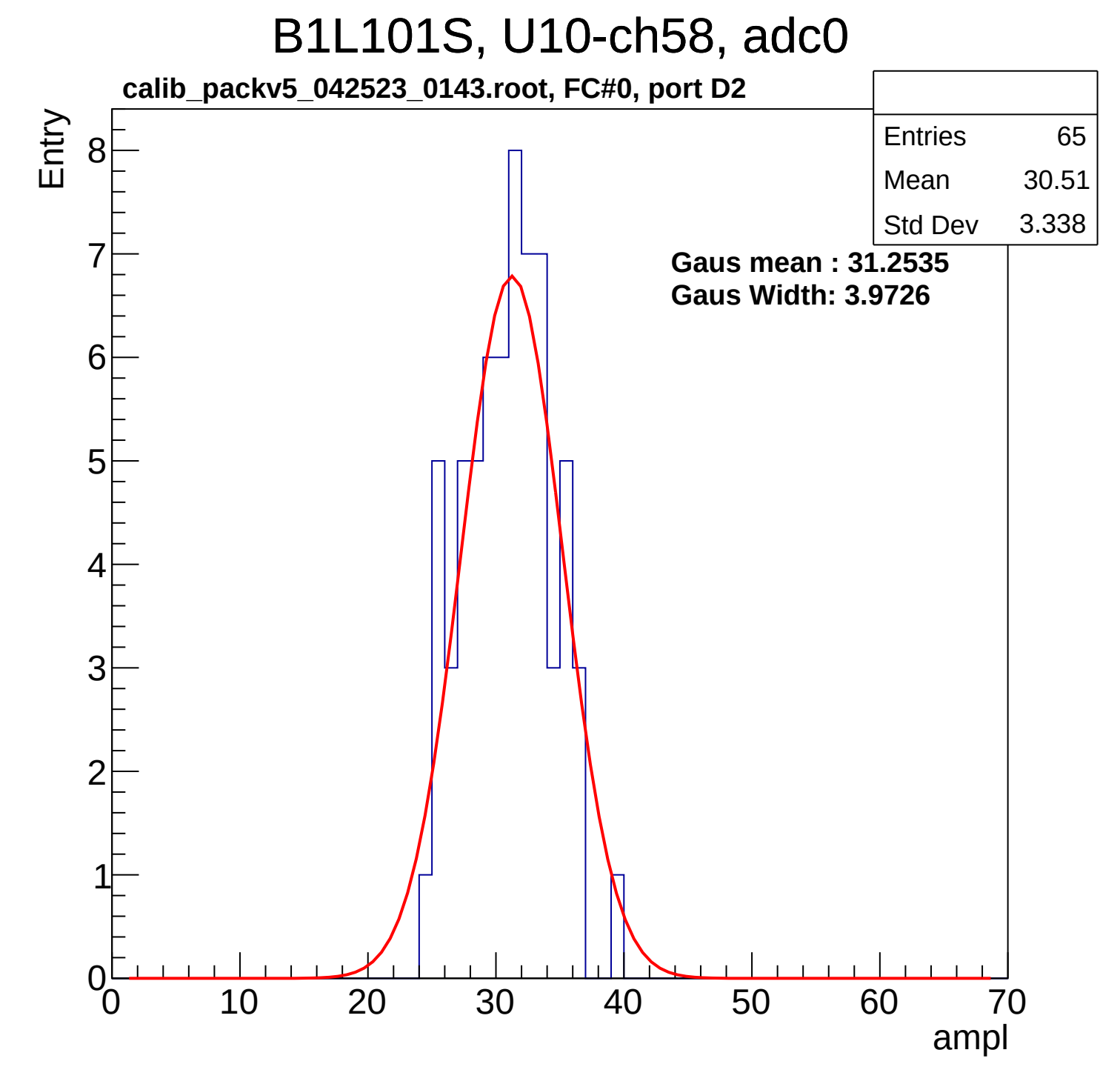
40
50
60
70


B1L101S, U10-ch57, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch58, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 30.51
Std Dev 3.338
Gaus mean : 31.2535
Gaus Width: 3.9726
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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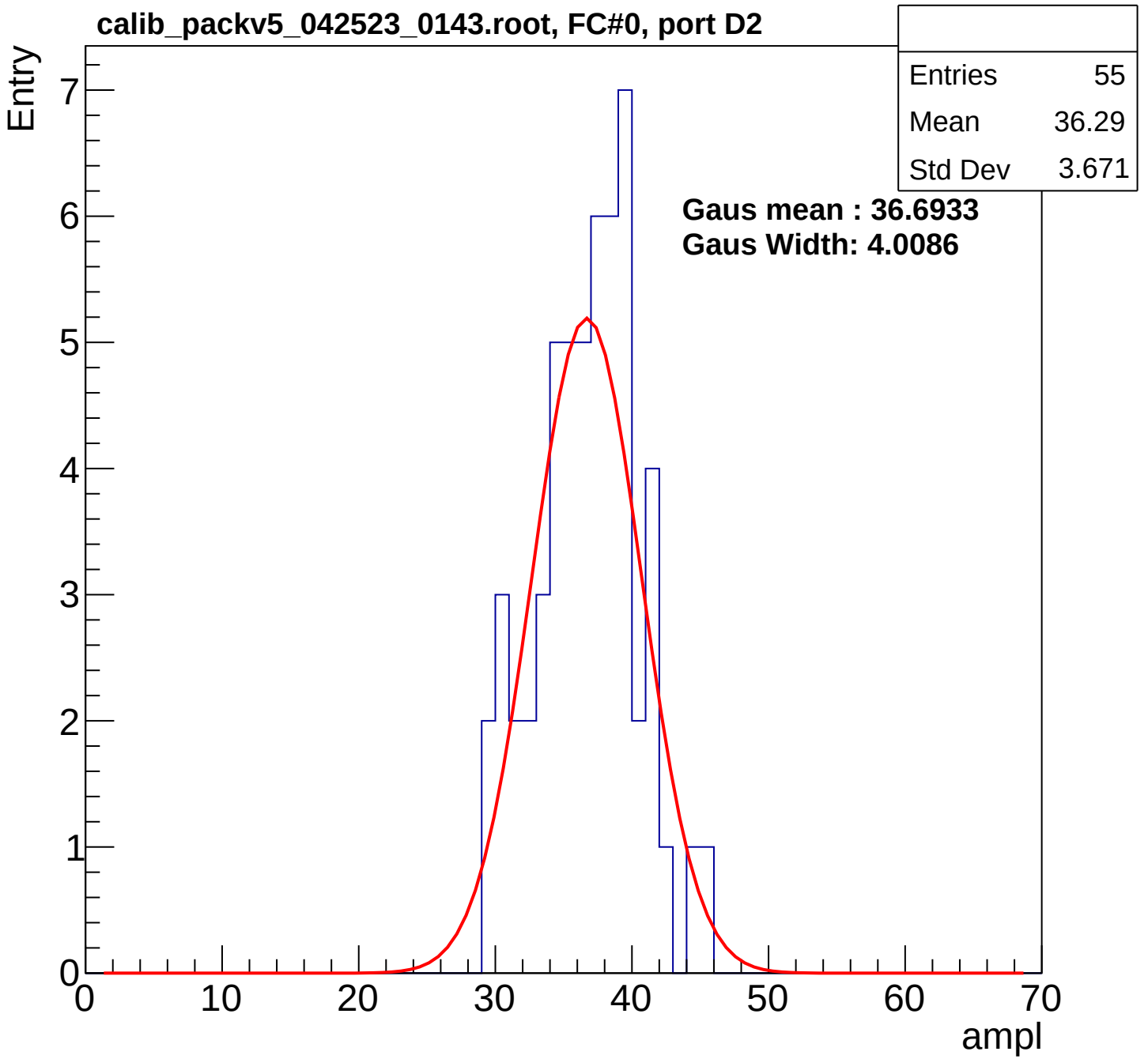
B1L101S, U10-ch58, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 36.29
Std Dev 3.671
Gaus mean : 36.6933
Gaus Width: 4.0086
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
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60
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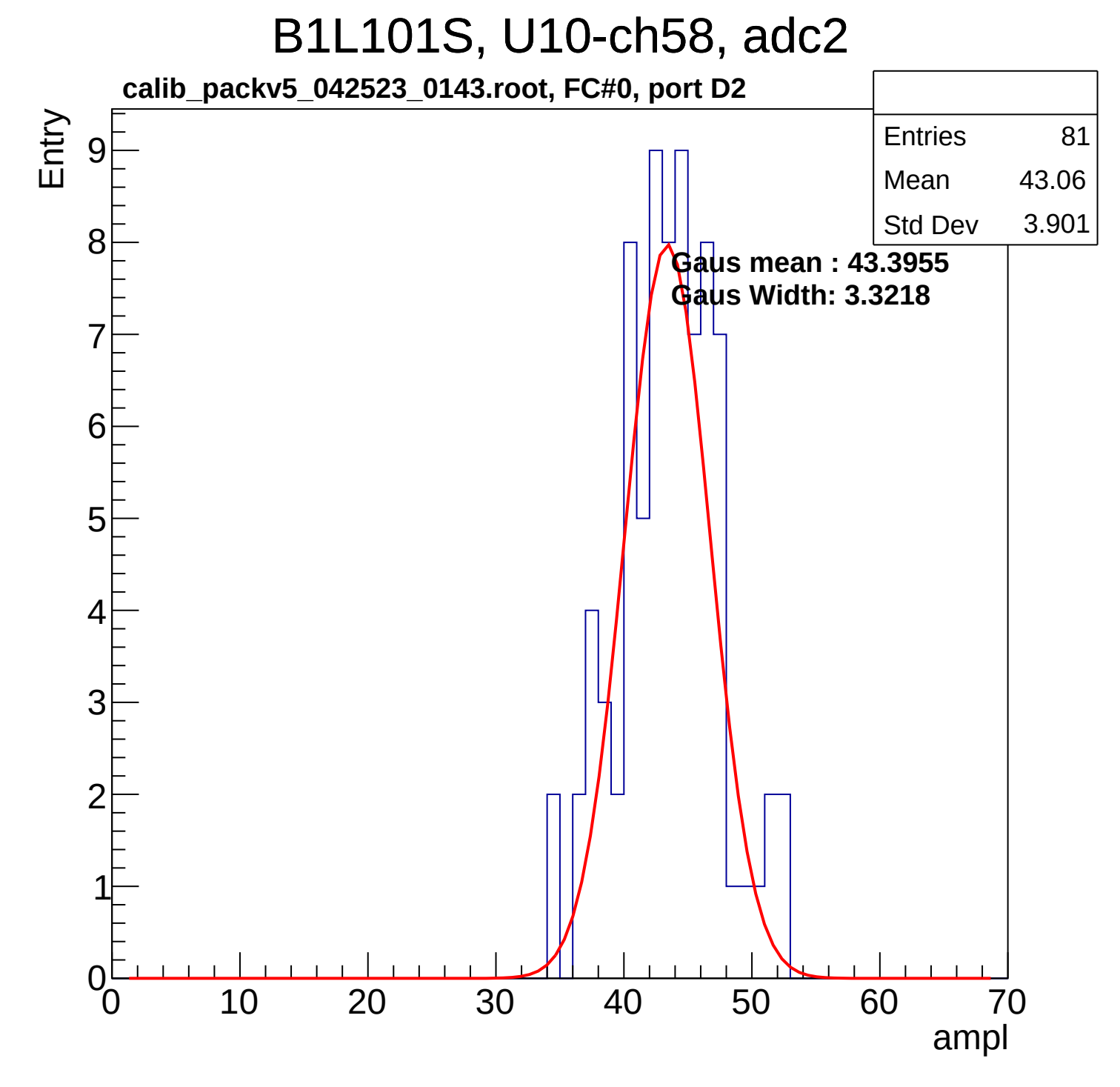
B1L101S, U10-ch58, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 81
Mean 43.06
Std Dev 3.901
Gaus mean : 43.3955
Gaus Width: 3.3218
Entry
ampl
0
10
20
30
40
50
60
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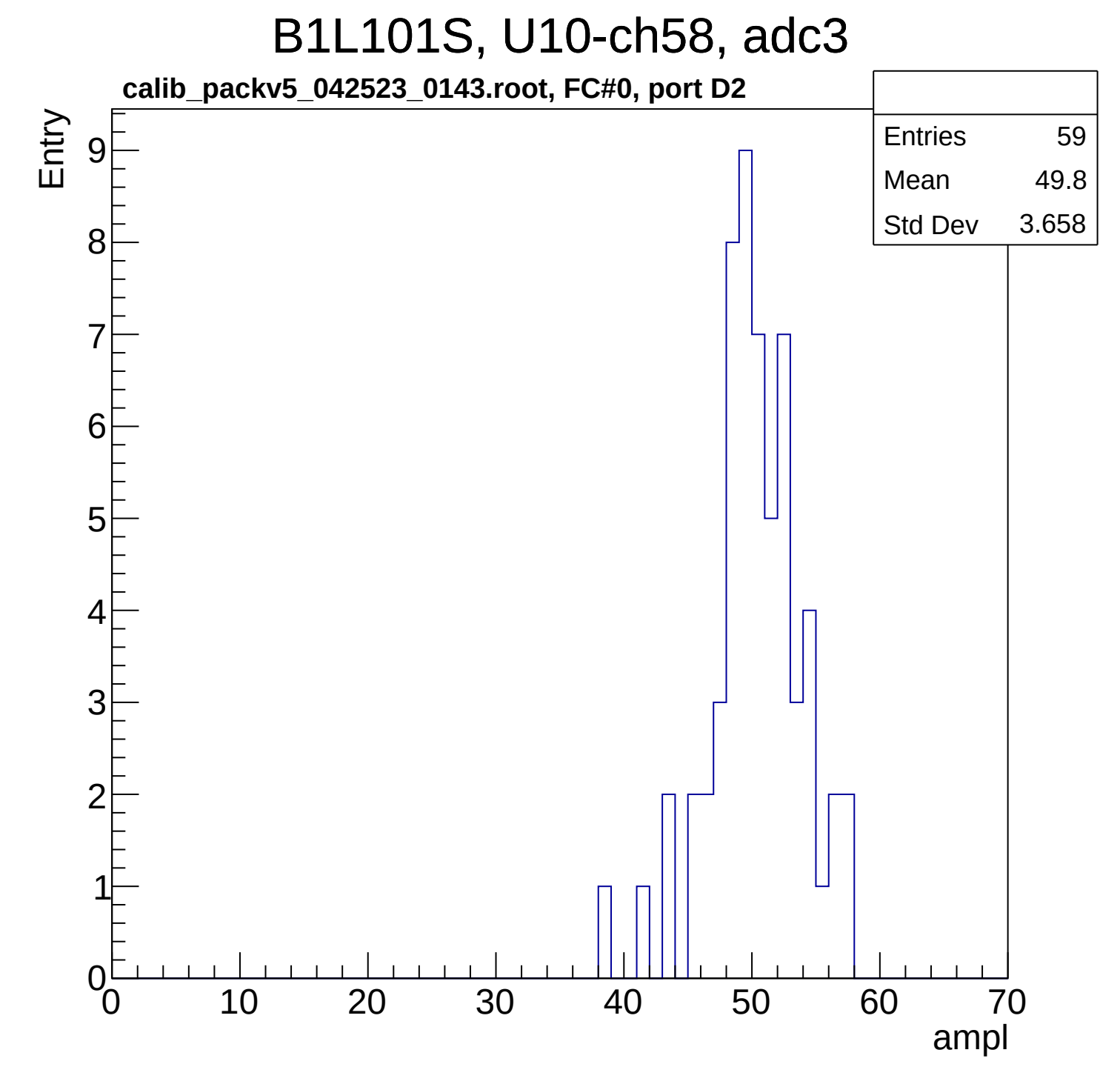
1
2
3
4
5
6
7
8
9


B1L101S, U10-ch58, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 49.8
Std Dev 3.658
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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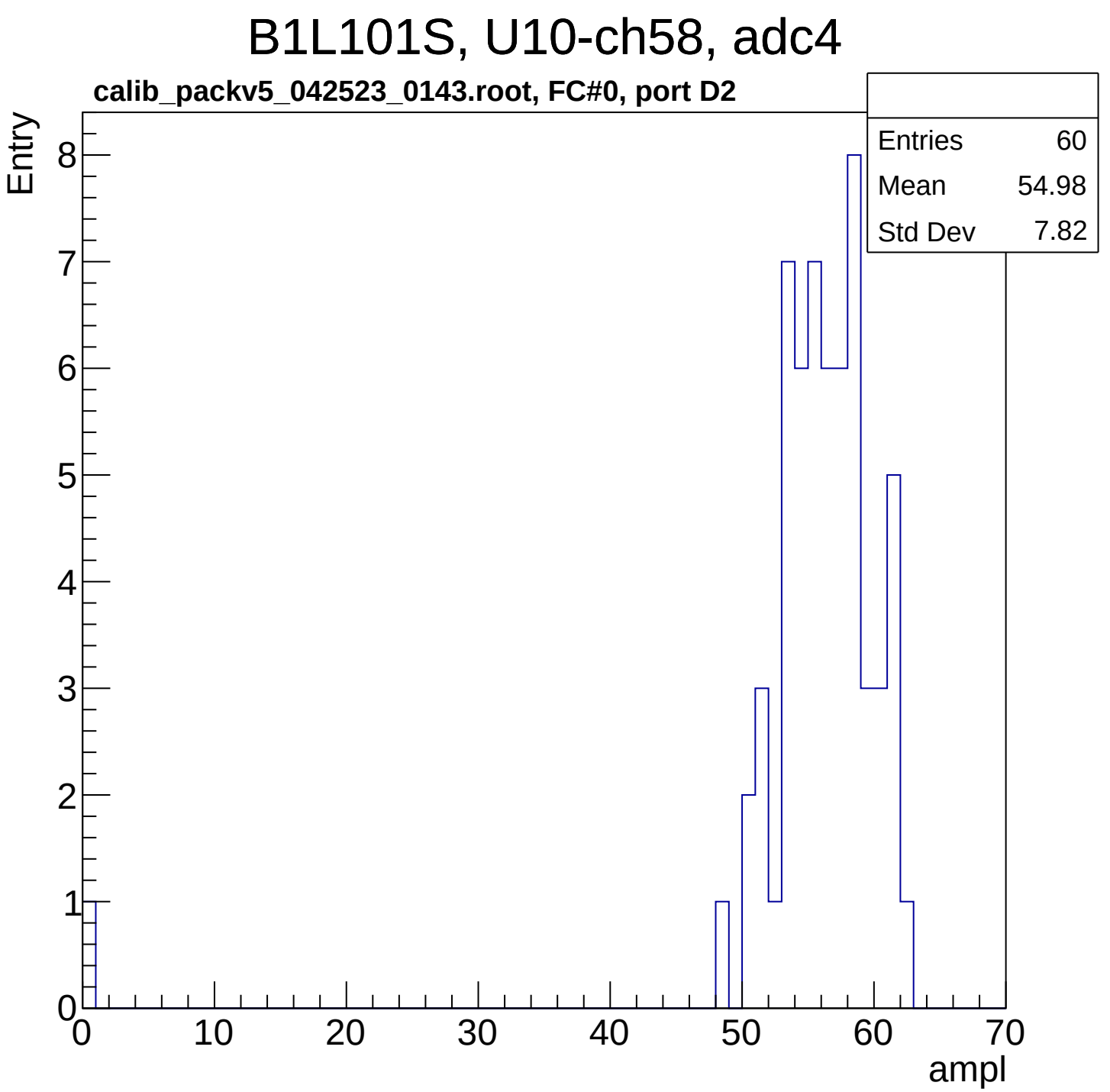
B1L101S, U10-ch58, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 54.98
Std Dev 7.82
Entry
ampl
0
1
2
3
4
5
6
7
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0
10
20
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40
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60
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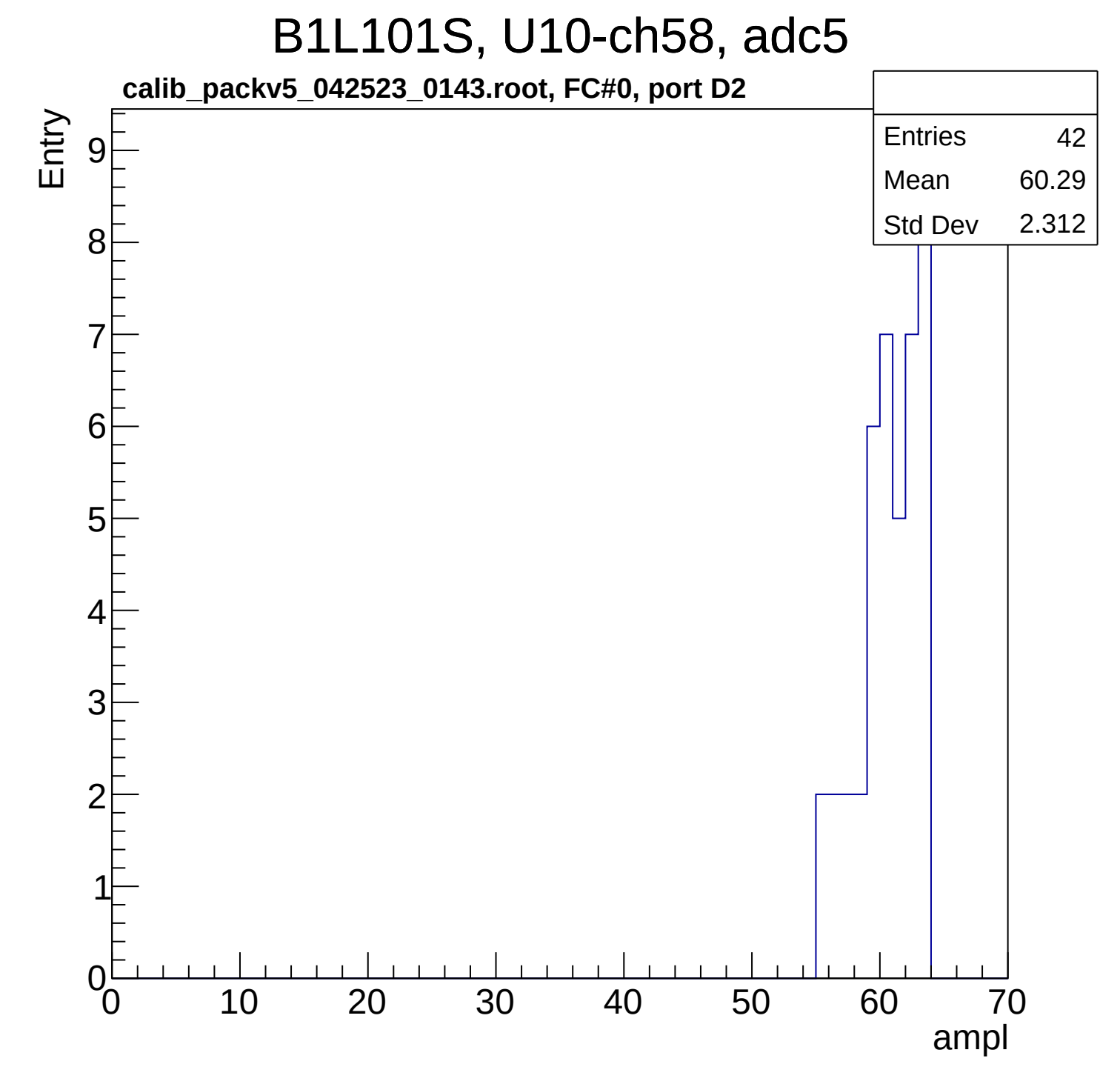
B1L101S, U10-ch58, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 60.29
Std Dev 2.312
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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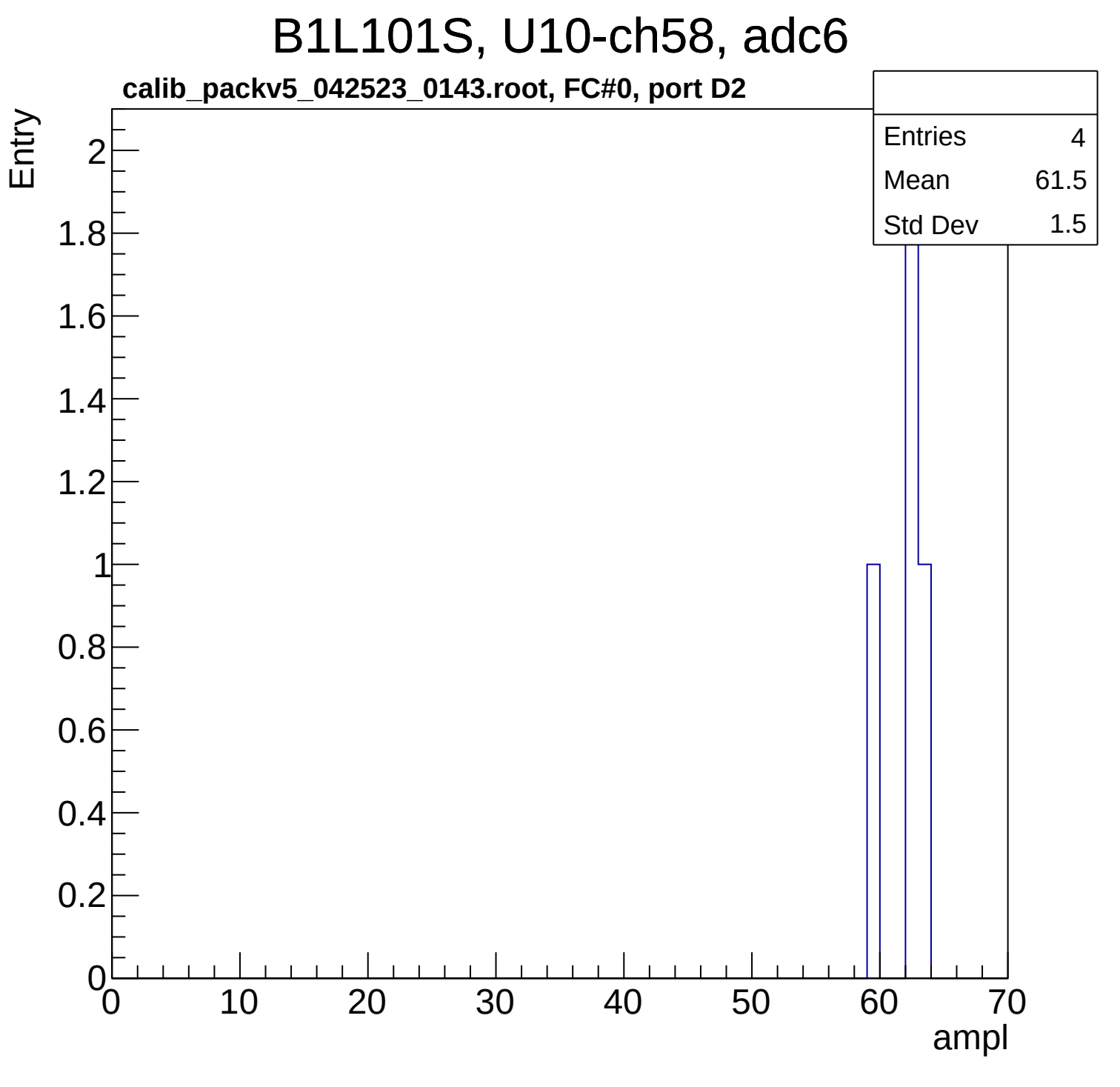
B1L101S, U10-ch58, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 61.5
Std Dev 1.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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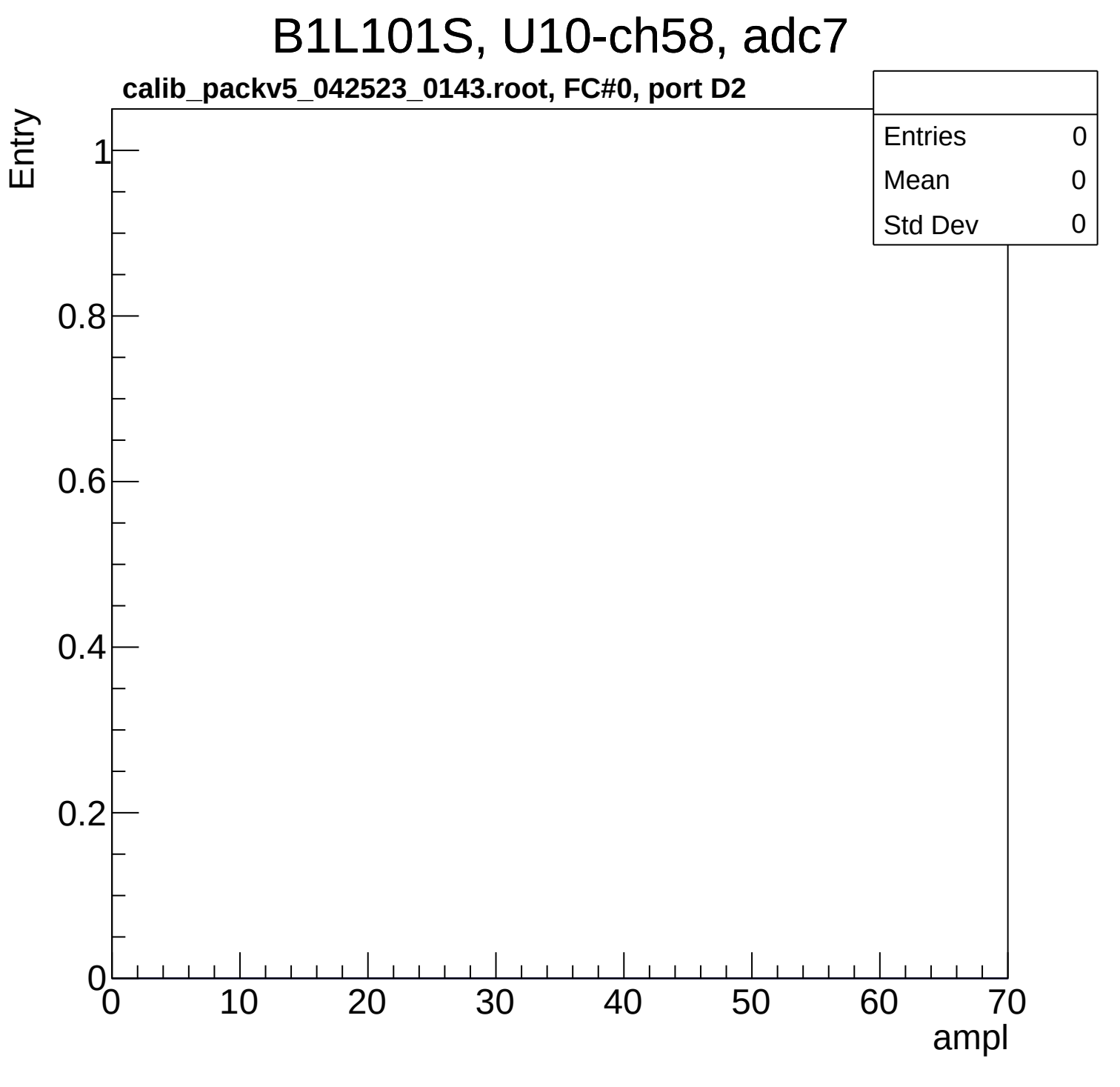
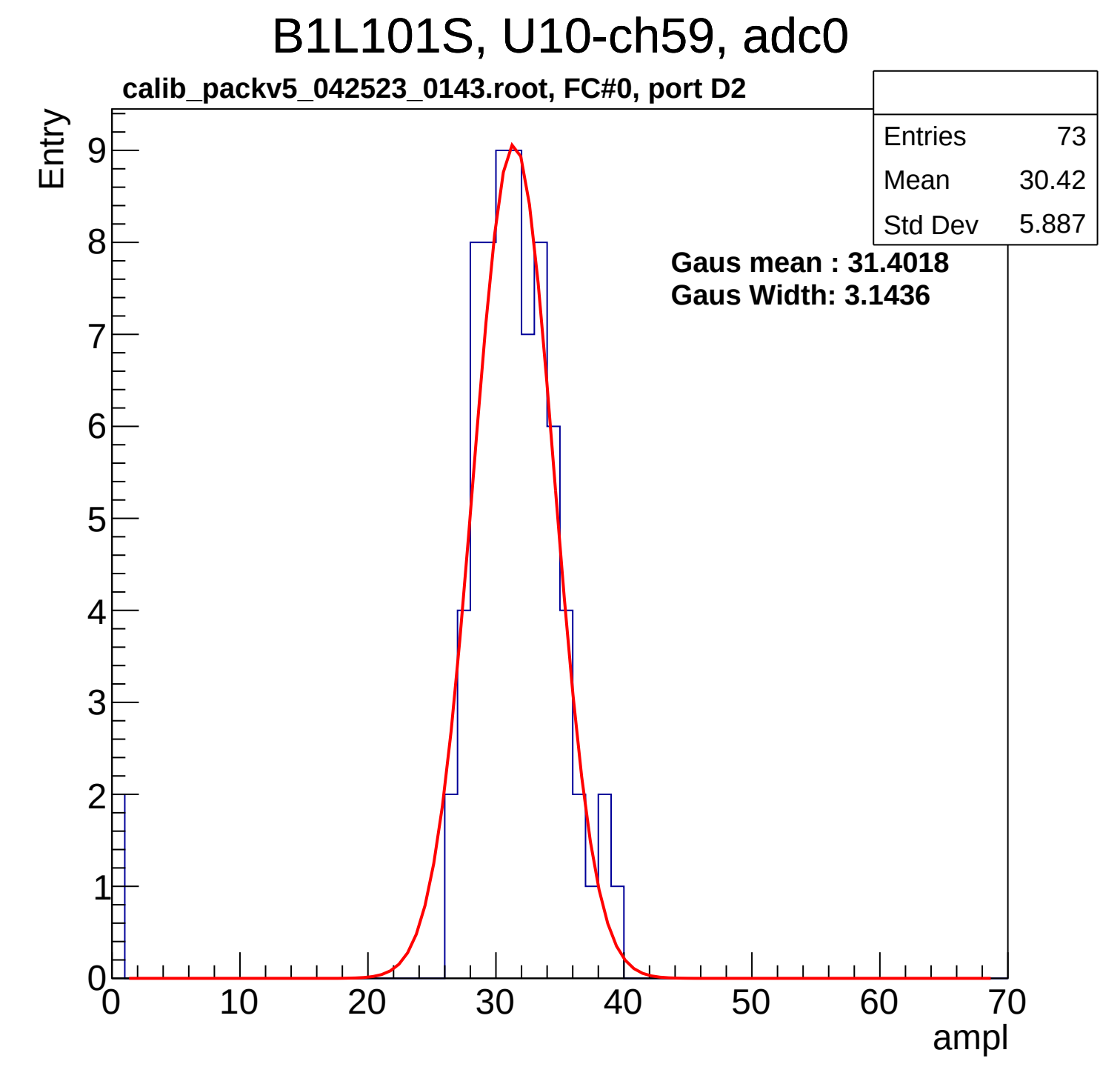
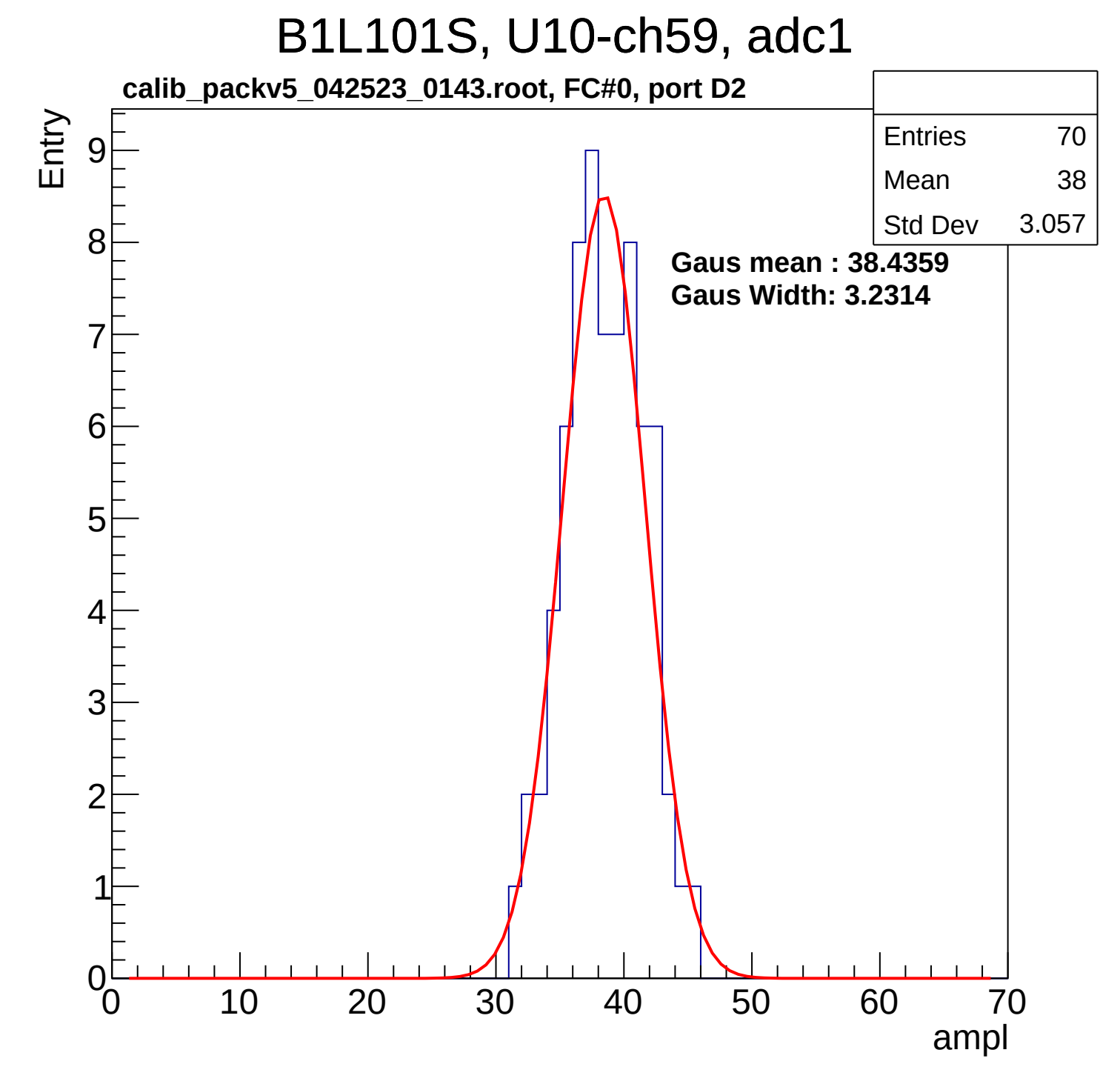

B1L101S, U10-ch58, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch59, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 30.42
Std Dev 5.887
Gaus mean : 31.4018
Gaus Width: 3.1436
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch59, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 38
Std Dev 3.057
Gaus mean : 38.4359
Gaus Width: 3.2314
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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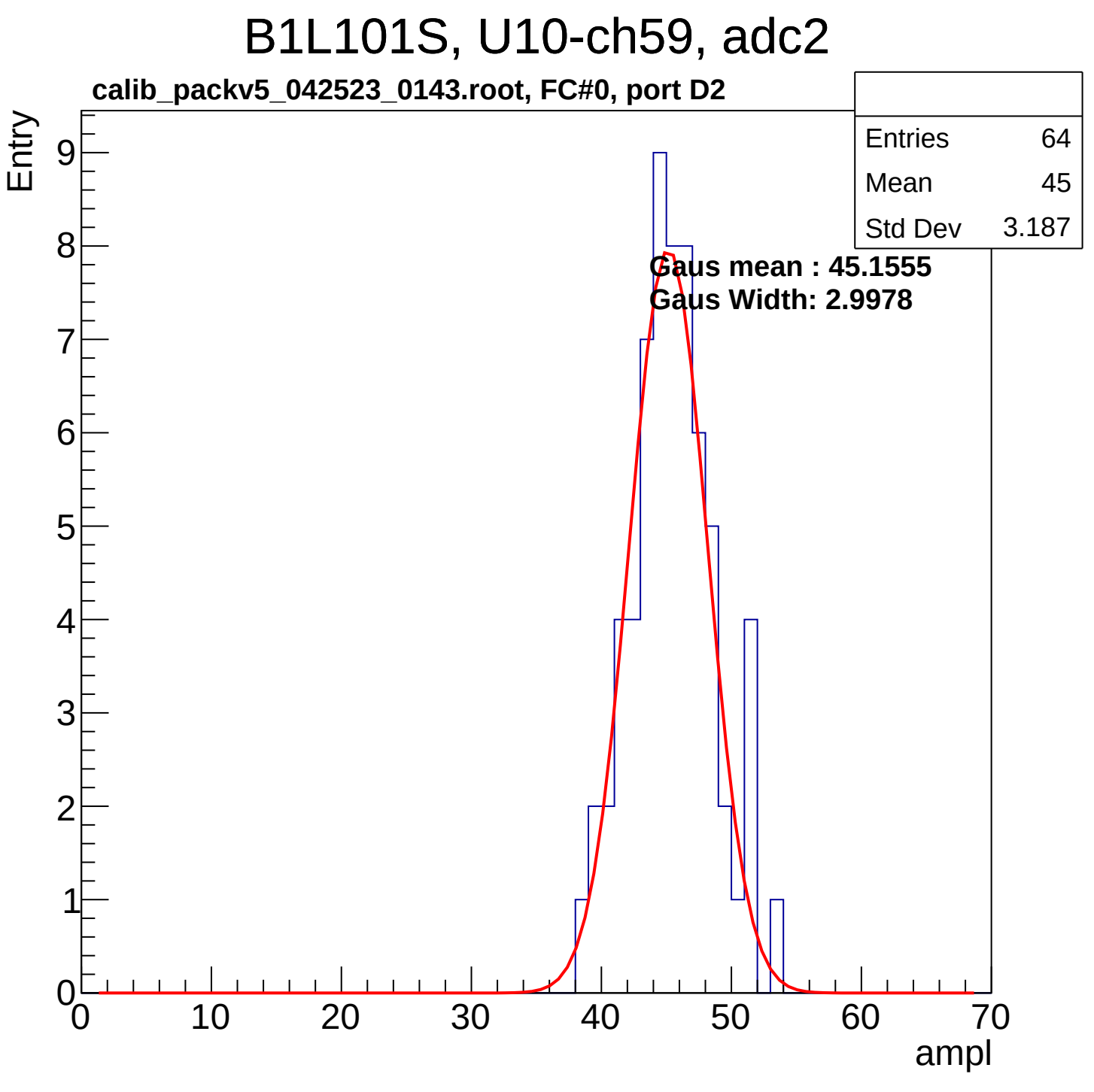
B1L101S, U10-ch59, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 45
Std Dev 3.187
Gaus mean : 45.1555
Gaus Width: 2.9978
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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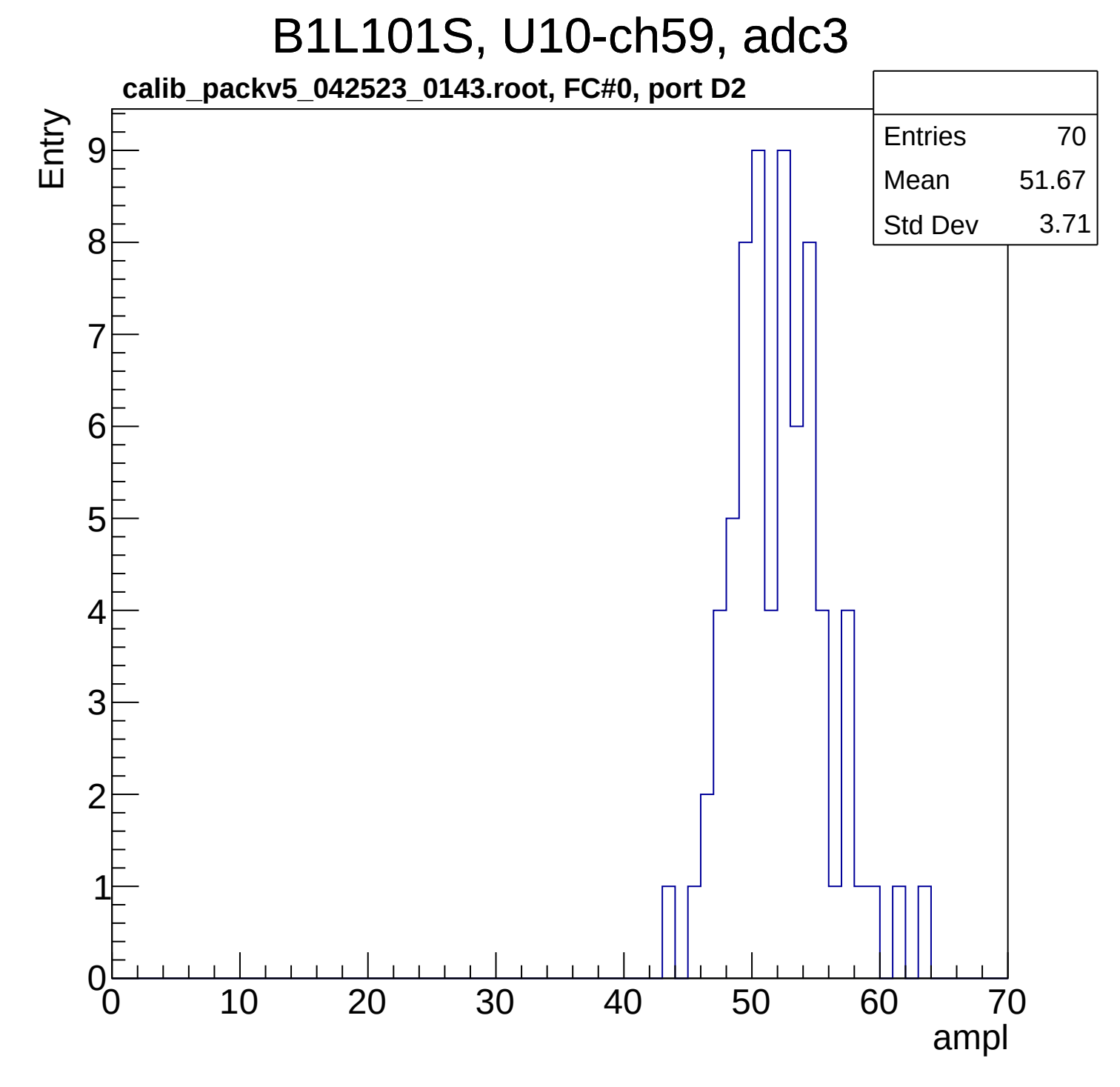
B1L101S, U10-ch59, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 51.67
Std Dev 3.71
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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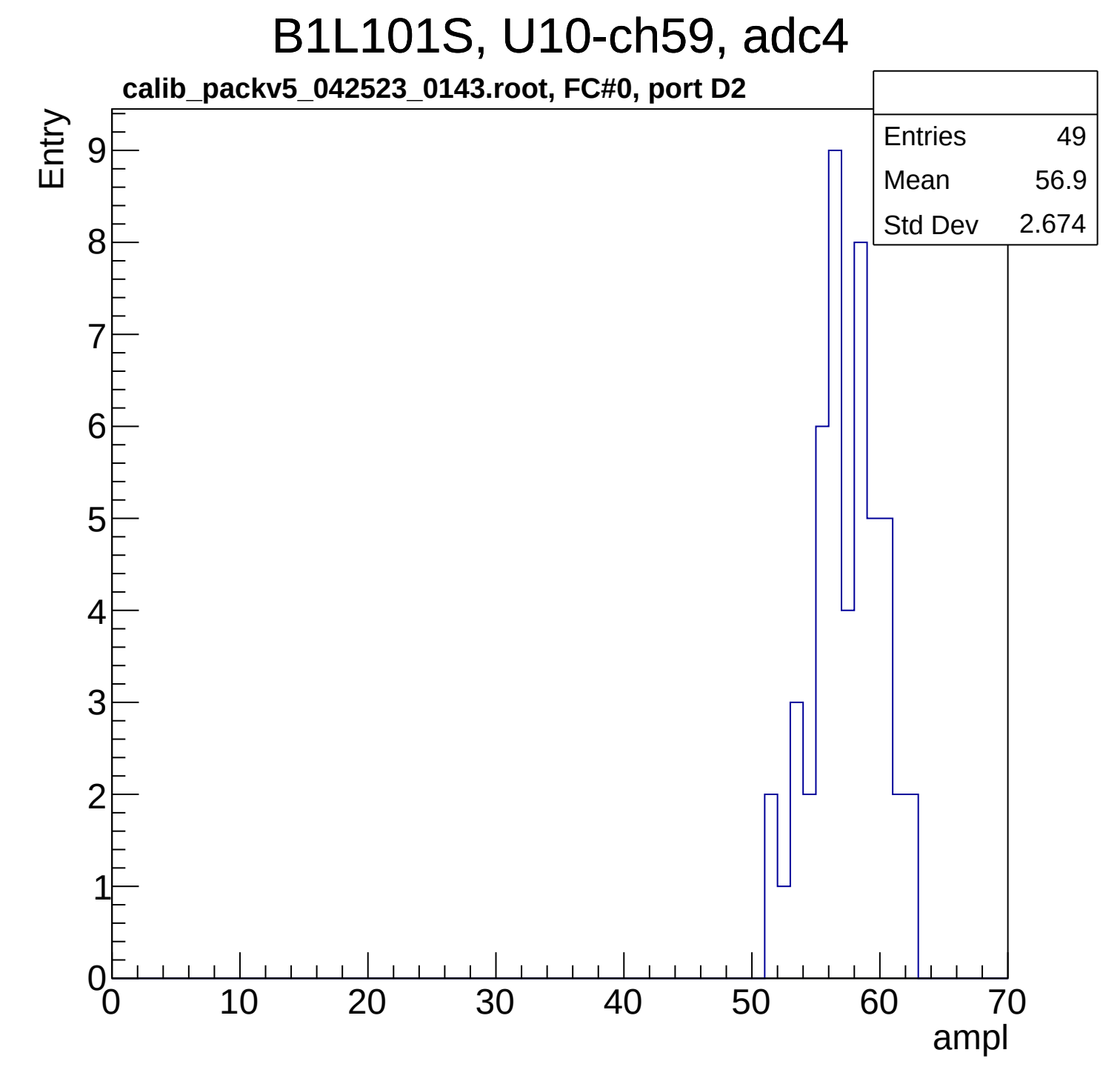
B1L101S, U10-ch59, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 56.9
Std Dev 2.674
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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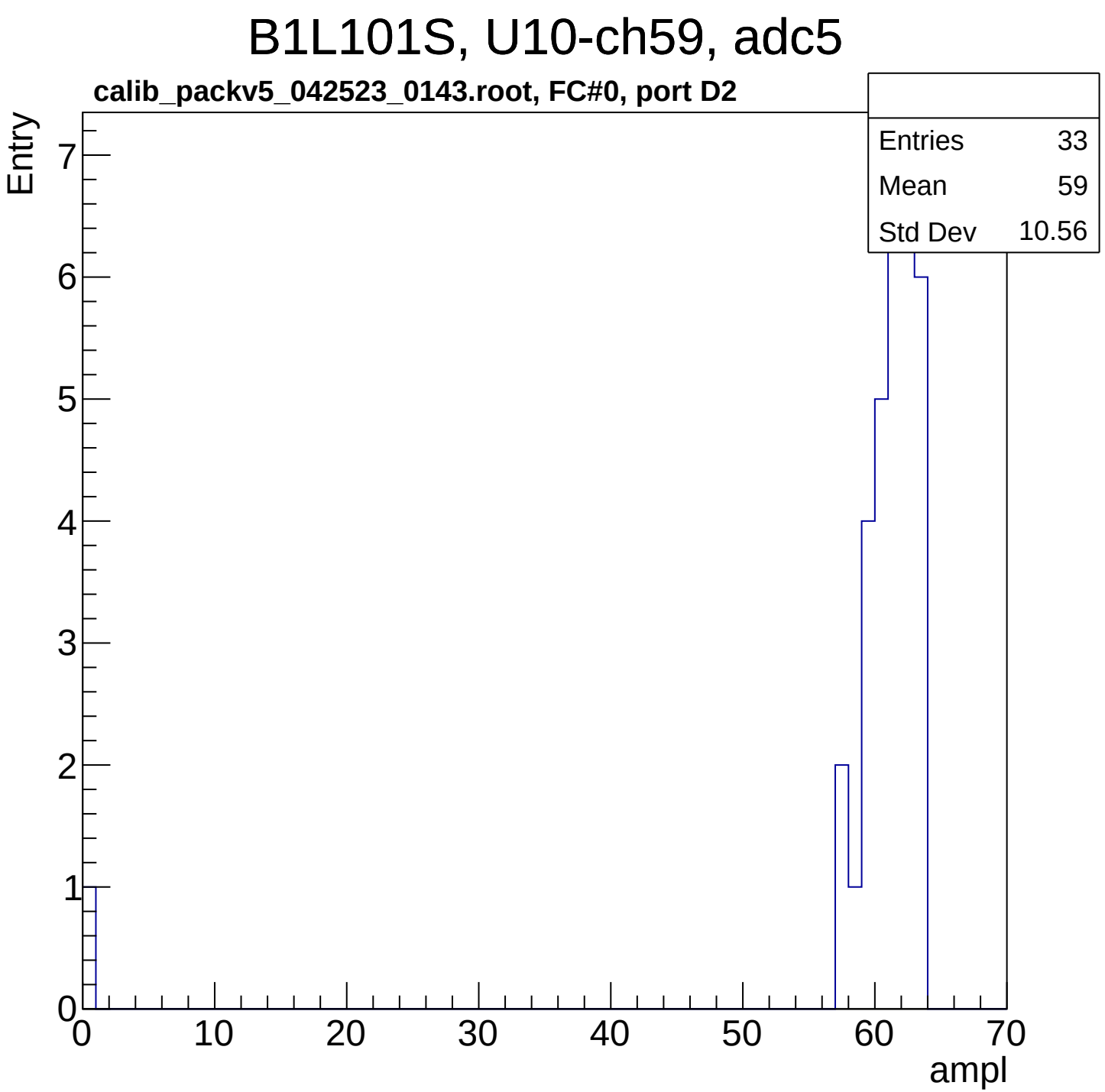
B1L101S, U10-ch59, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 33
Mean 59
Std Dev 10.56
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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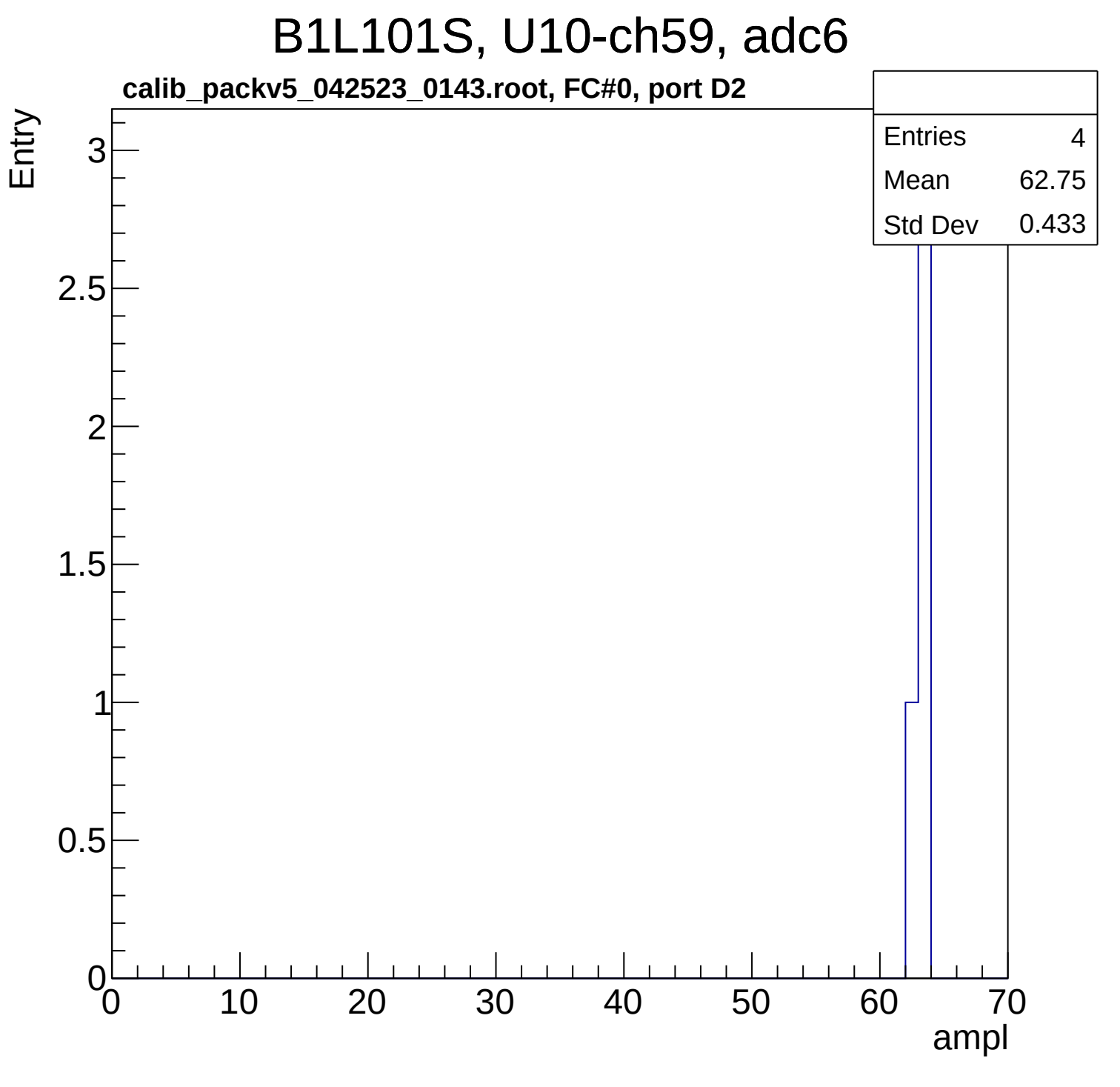
50
60
70


B1L101S, U10-ch59, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 62.75
Std Dev 0.433
Entry
ampl
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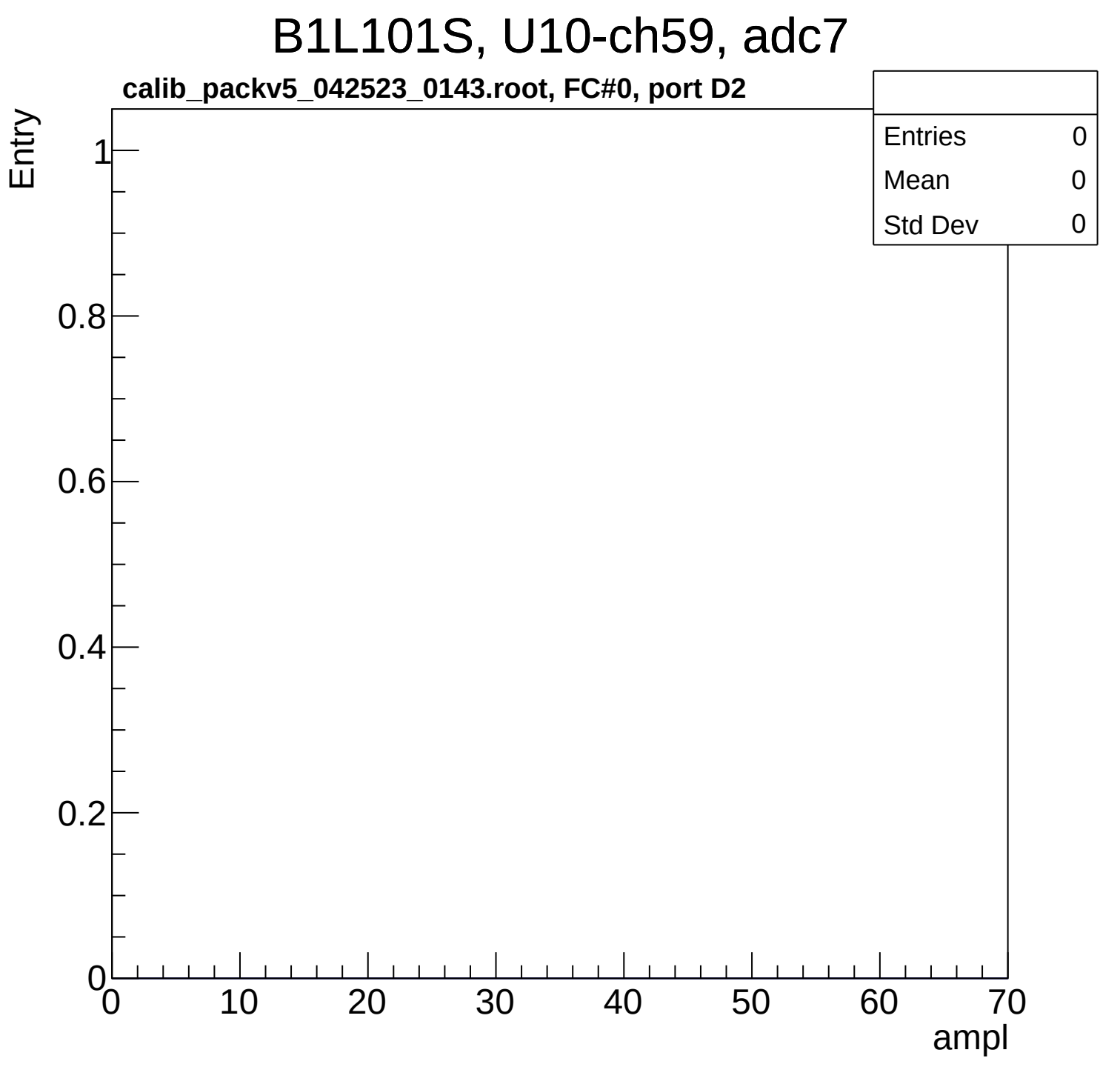
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U10-ch59, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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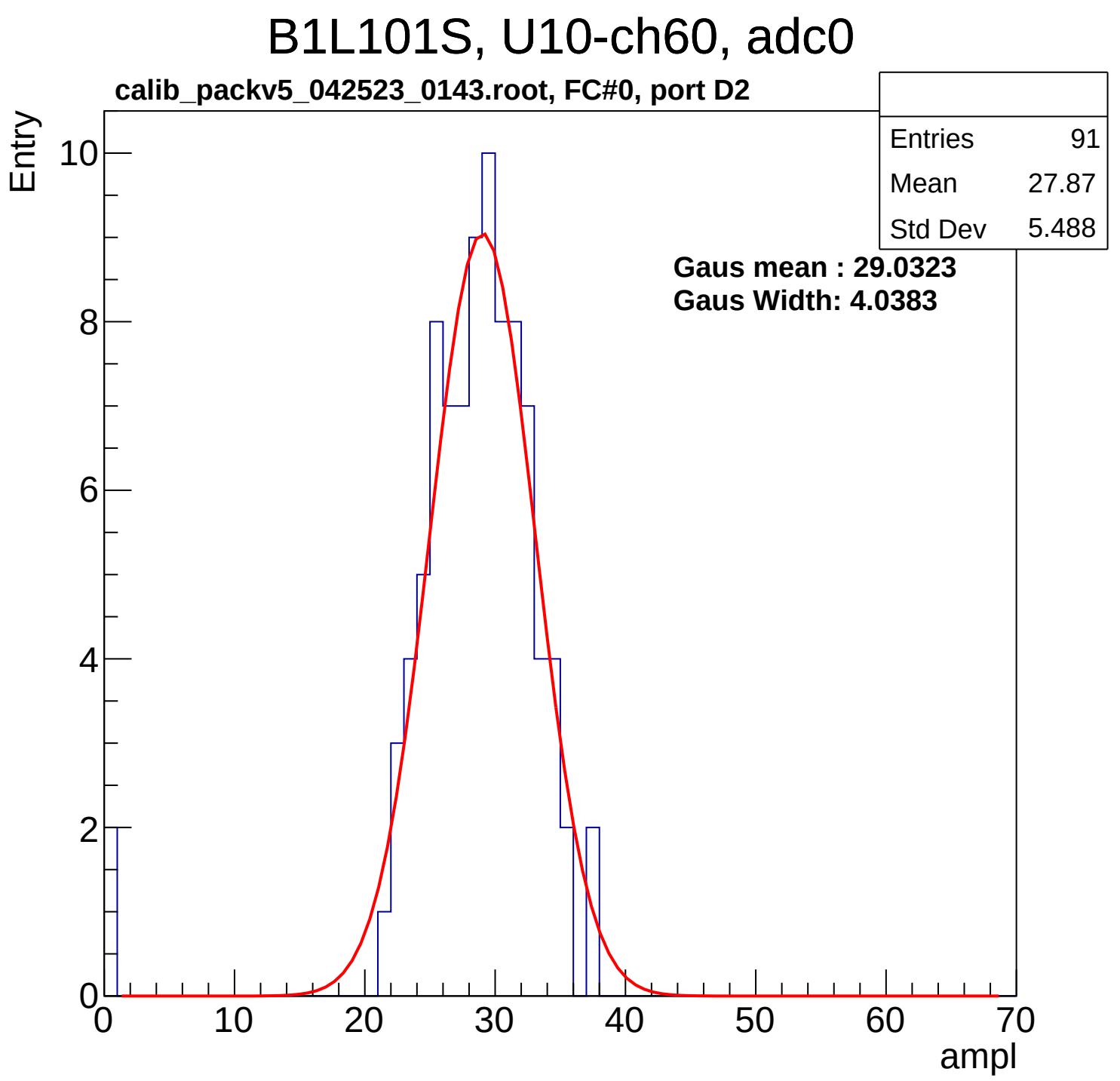
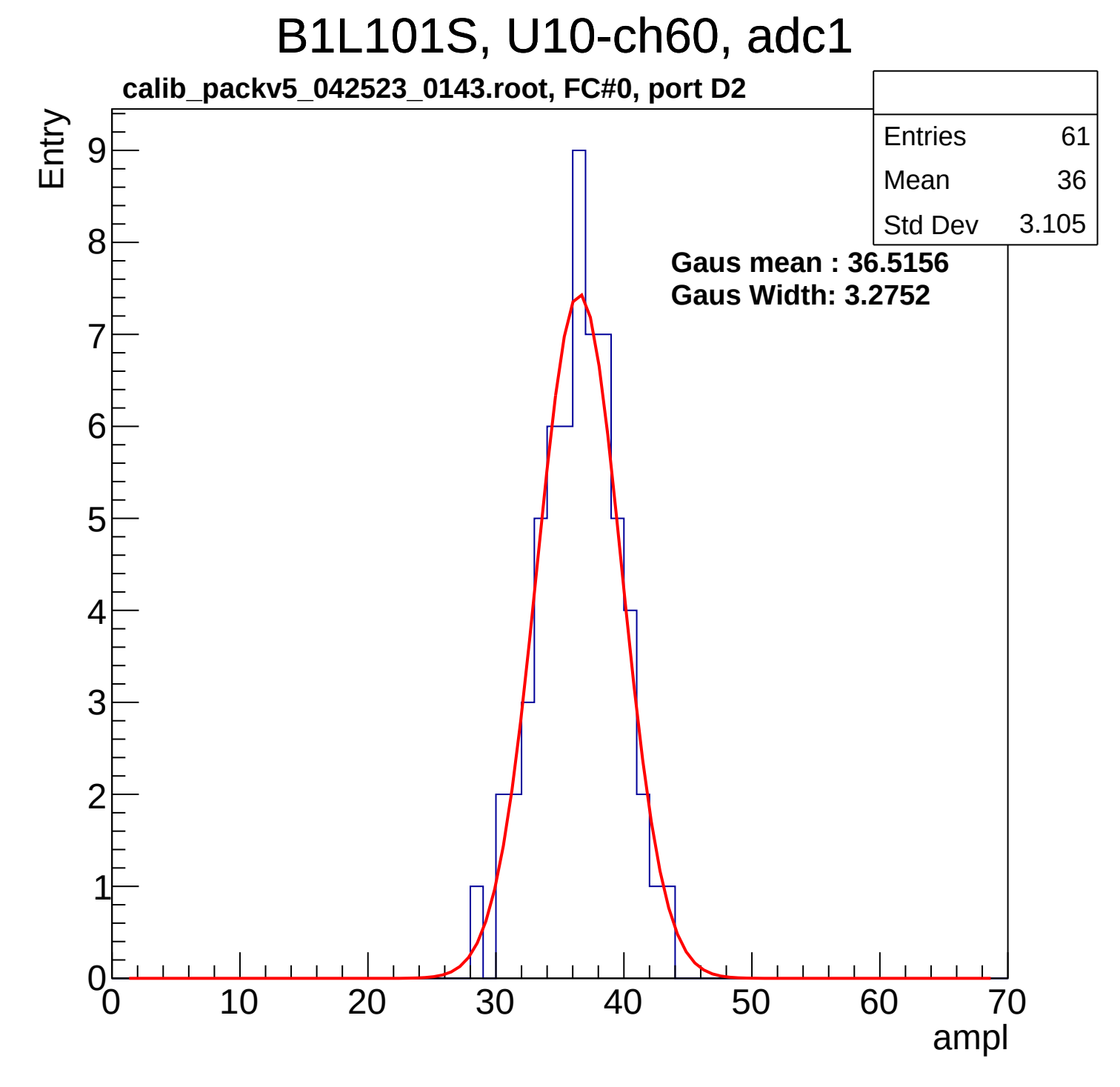
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch60, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 91
Mean 27.87
Std Dev 5.488
Gaus mean : 29.0323
Gaus Width: 4.0383
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch60, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 36
Std Dev 3.105
Gaus mean : 36.5156
Gaus Width: 3.2752
Entry
ampl
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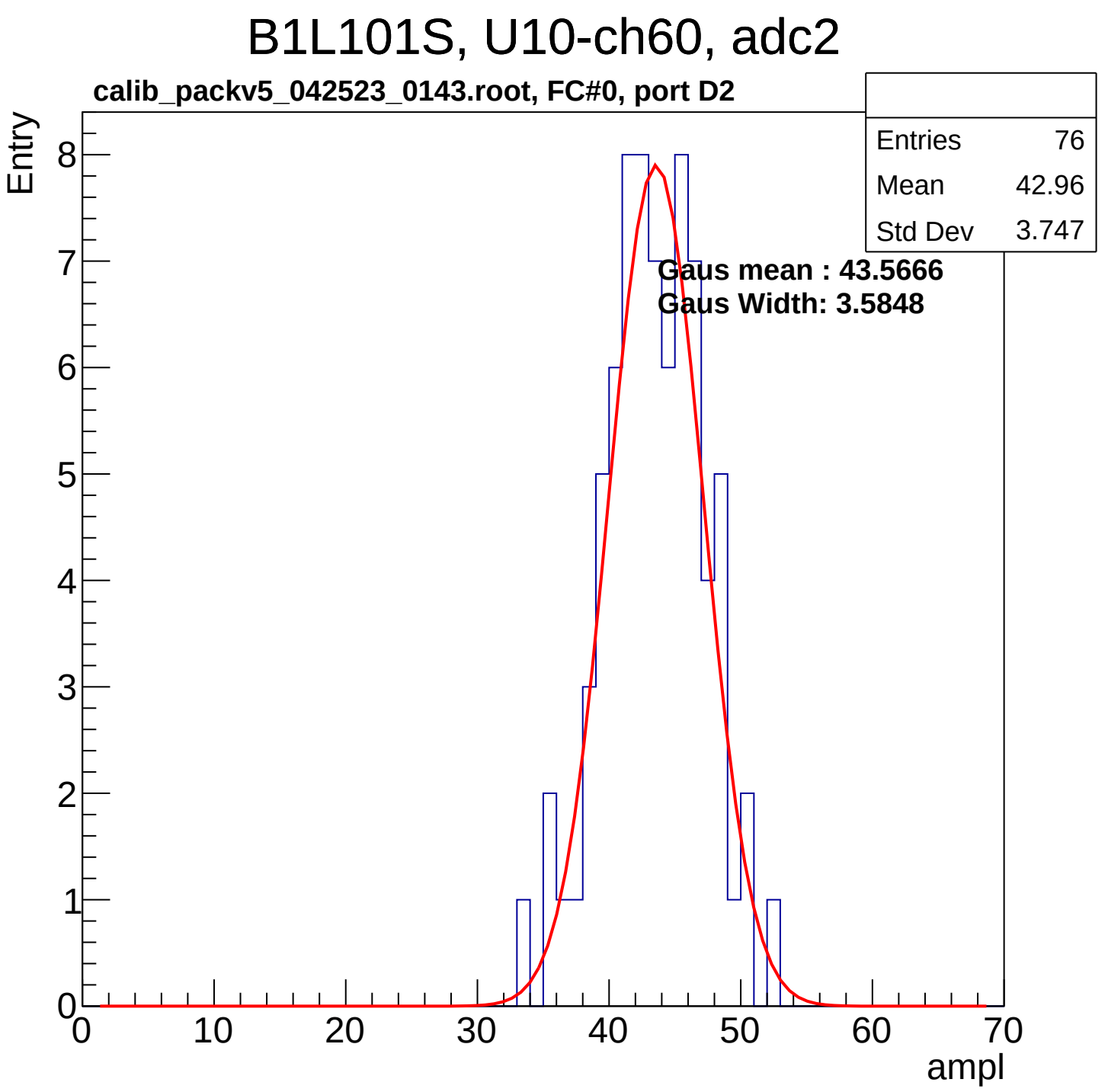
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch60, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 42.96
Std Dev 3.747
Gaus mean : 43.5666
Gaus Width: 3.5848
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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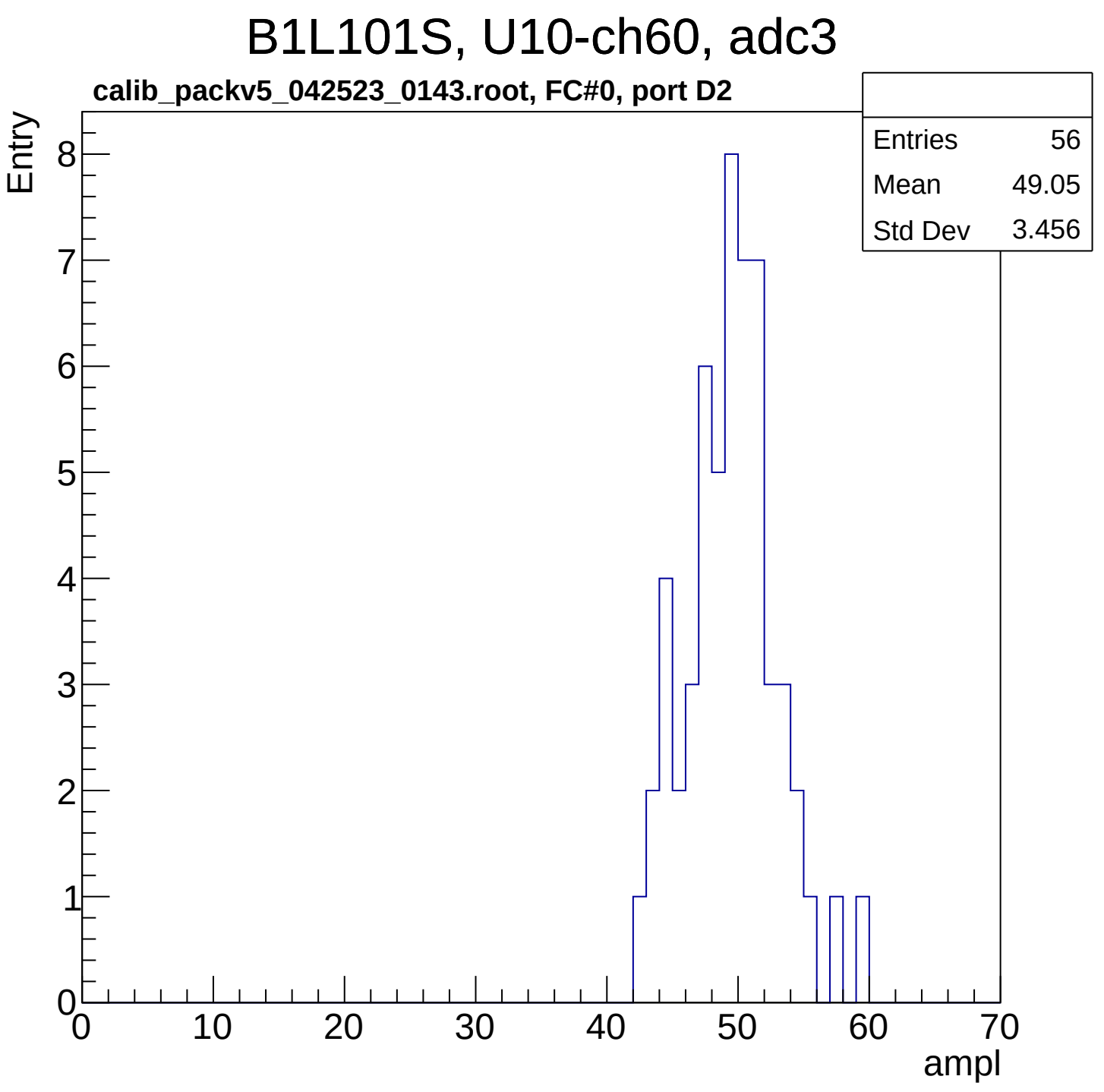
B1L101S, U10-ch60, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 49.05
Std Dev 3.456
Entry
ampl
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4
5
6
7
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0
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50
60
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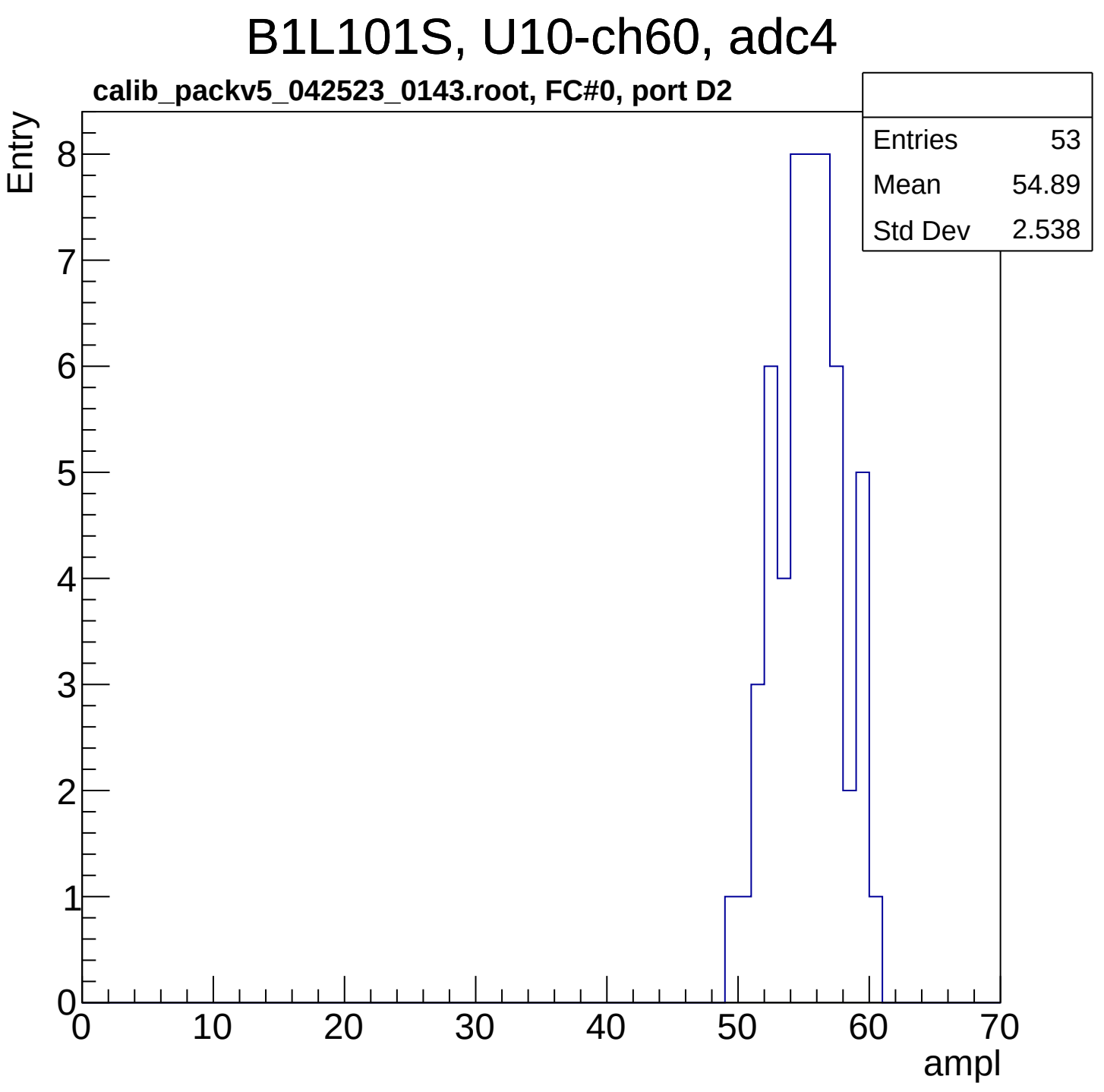
B1L101S, U10-ch60, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 54.89
Std Dev 2.538
Entry
ampl
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1
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4
5
6
7
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0
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40
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60
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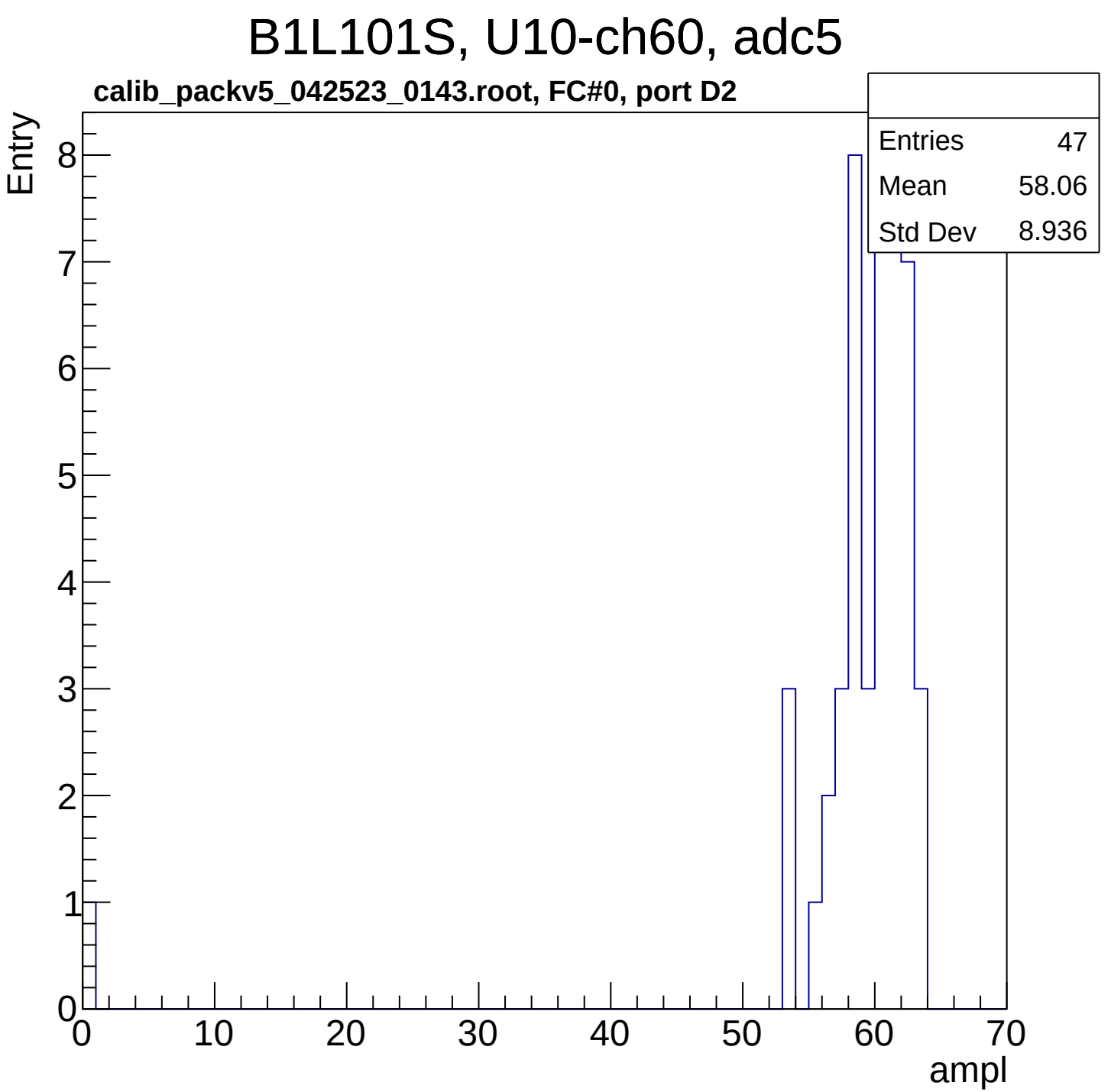
B1L101S, U10-ch60, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 58.06
Std Dev 8.936
Entry
ampl
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4
5
6
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0
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20
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40
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60
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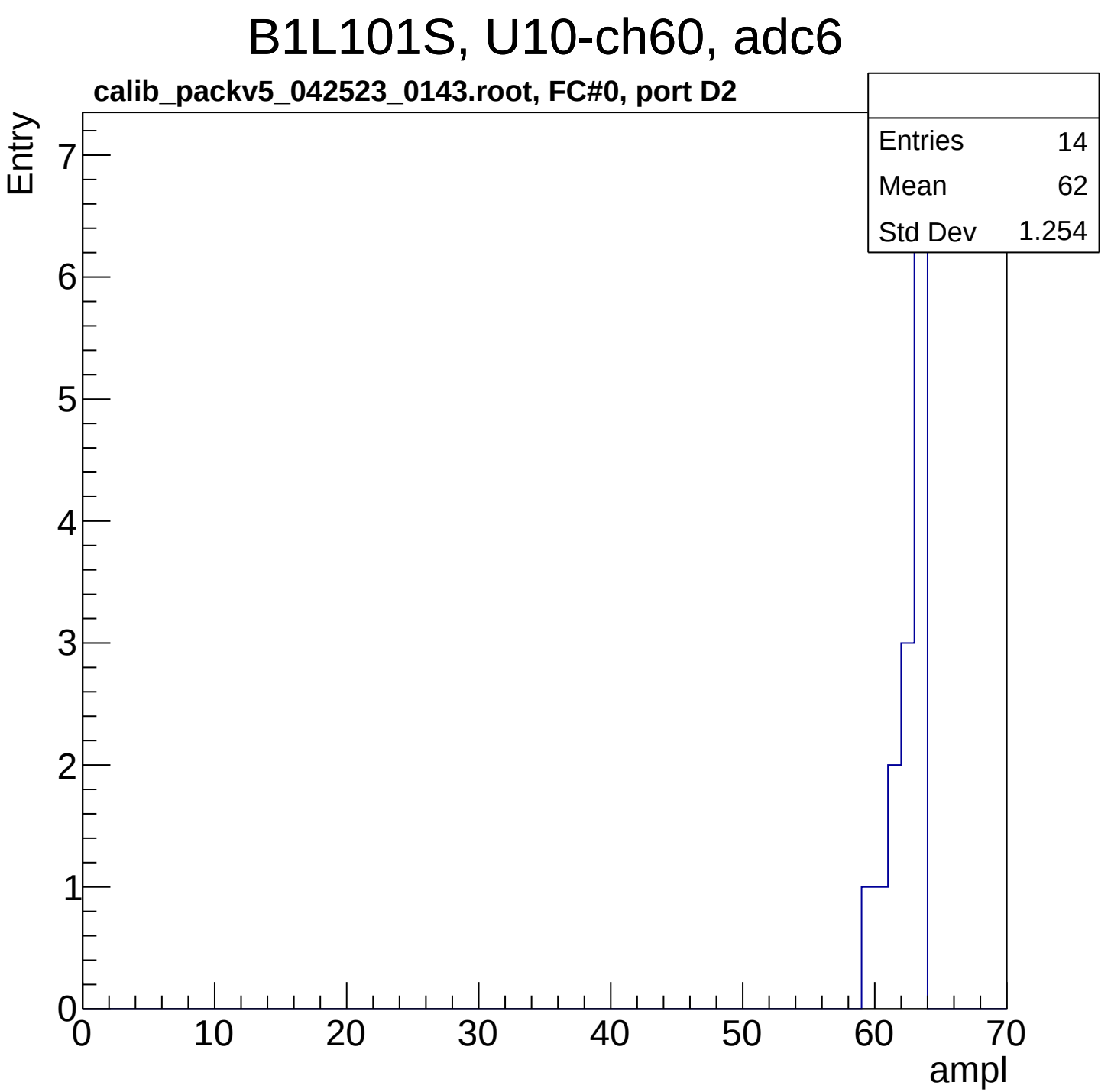
B1L101S, U10-ch60, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 14
Mean 62
Std Dev 1.254
Entry
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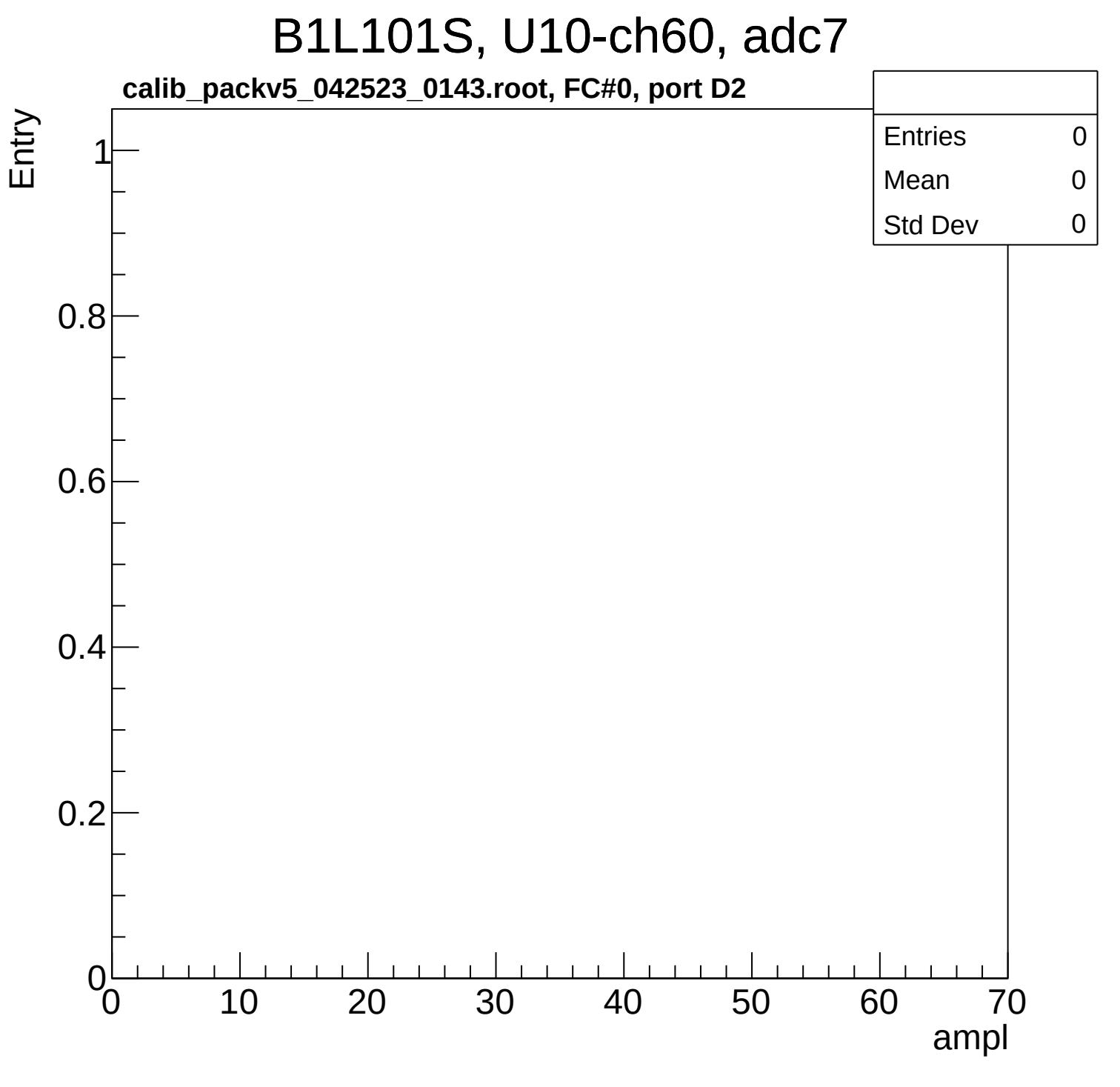
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch60, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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0.6
0.4
0.2
0
0
10
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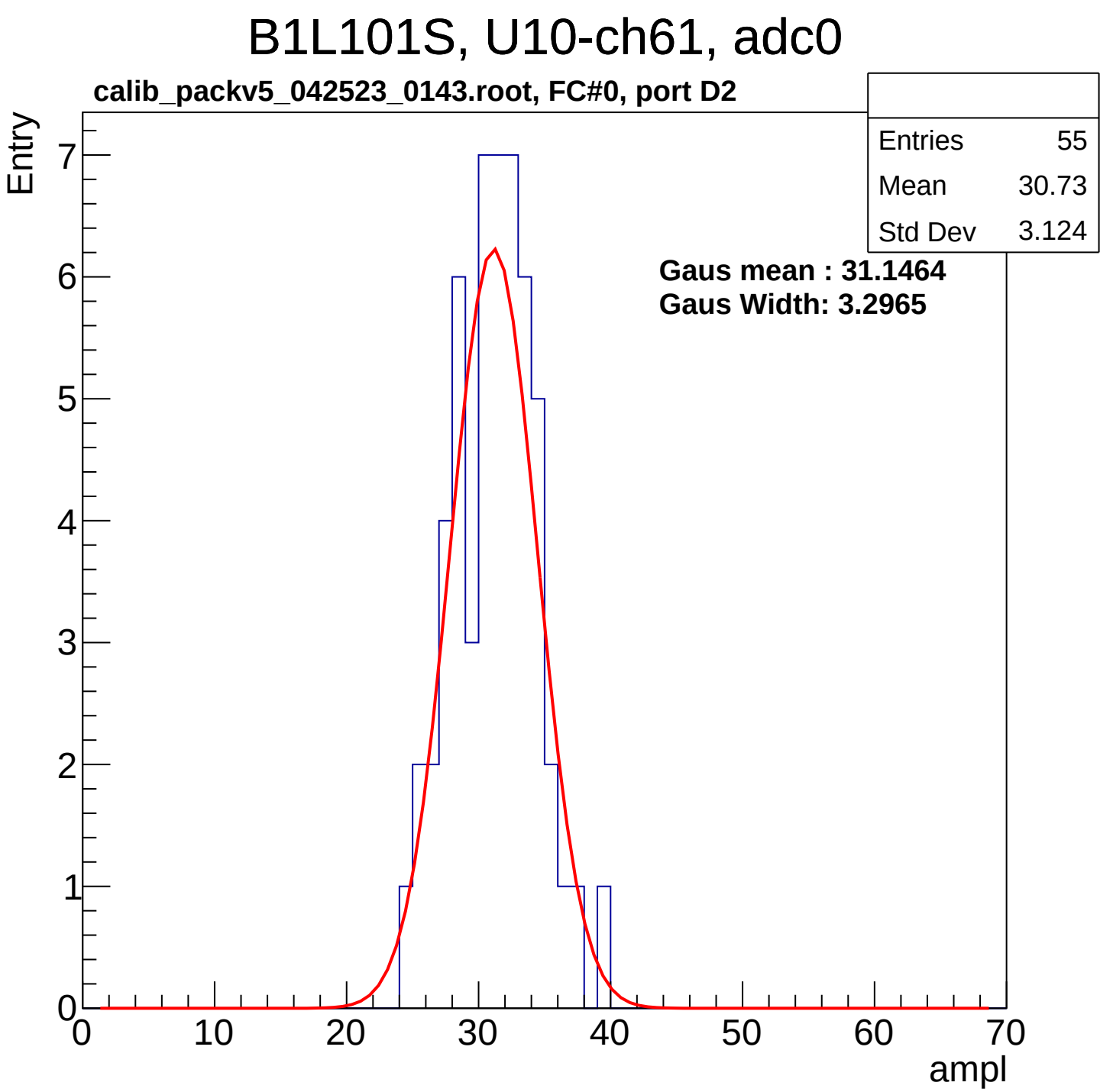
30
40
50
60
70
ampl


B1L101S, U10-ch61, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 30.73
Std Dev 3.124
Gaus mean : 31.1464
Gaus Width: 3.2965
Entry
ampl
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1
2
3
4
5
6
7
0
10
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40
50
60
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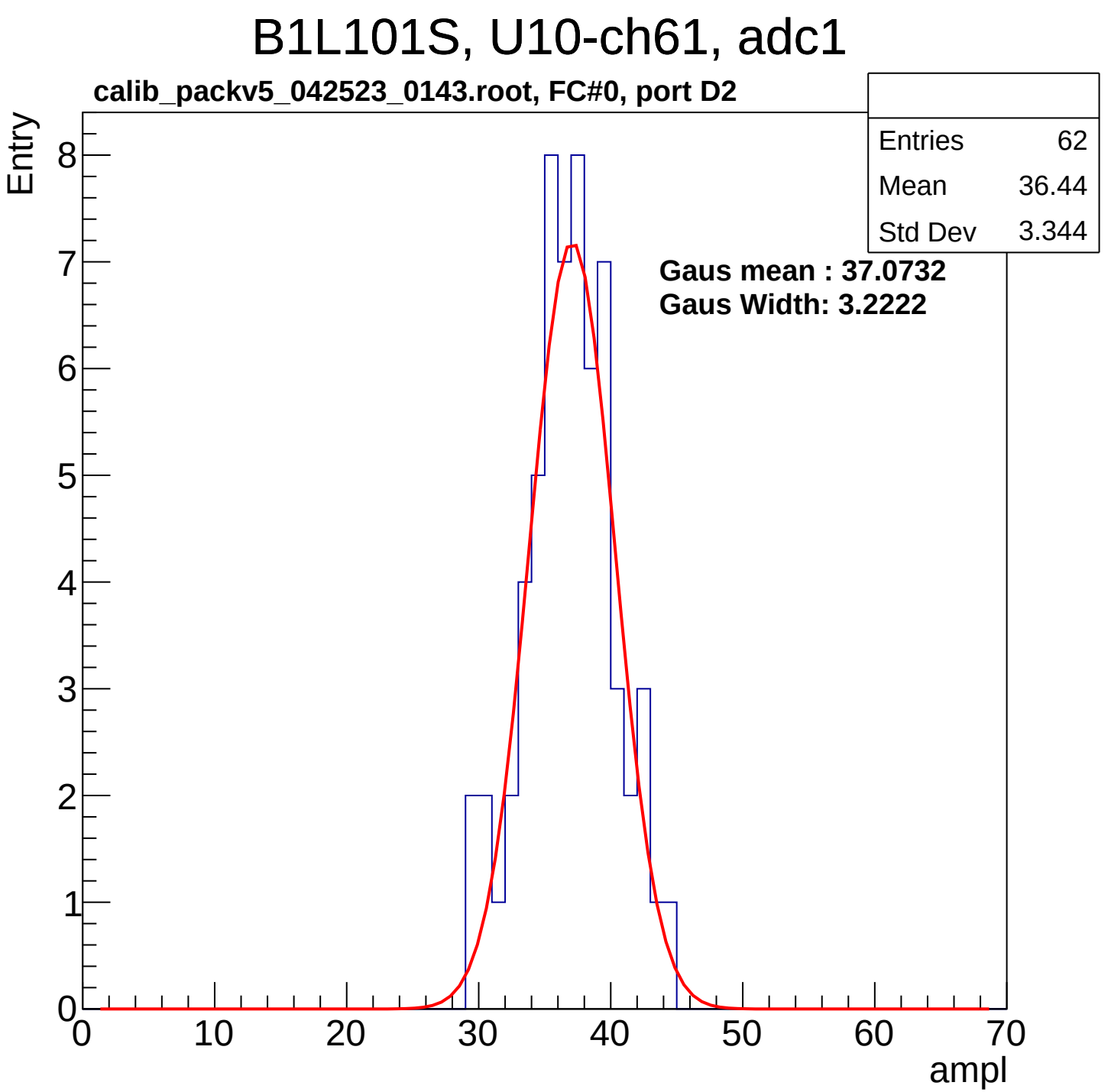
B1L101S, U10-ch61, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 36.44
Std Dev 3.344
Gaus mean : 37.0732
Gaus Width: 3.2222
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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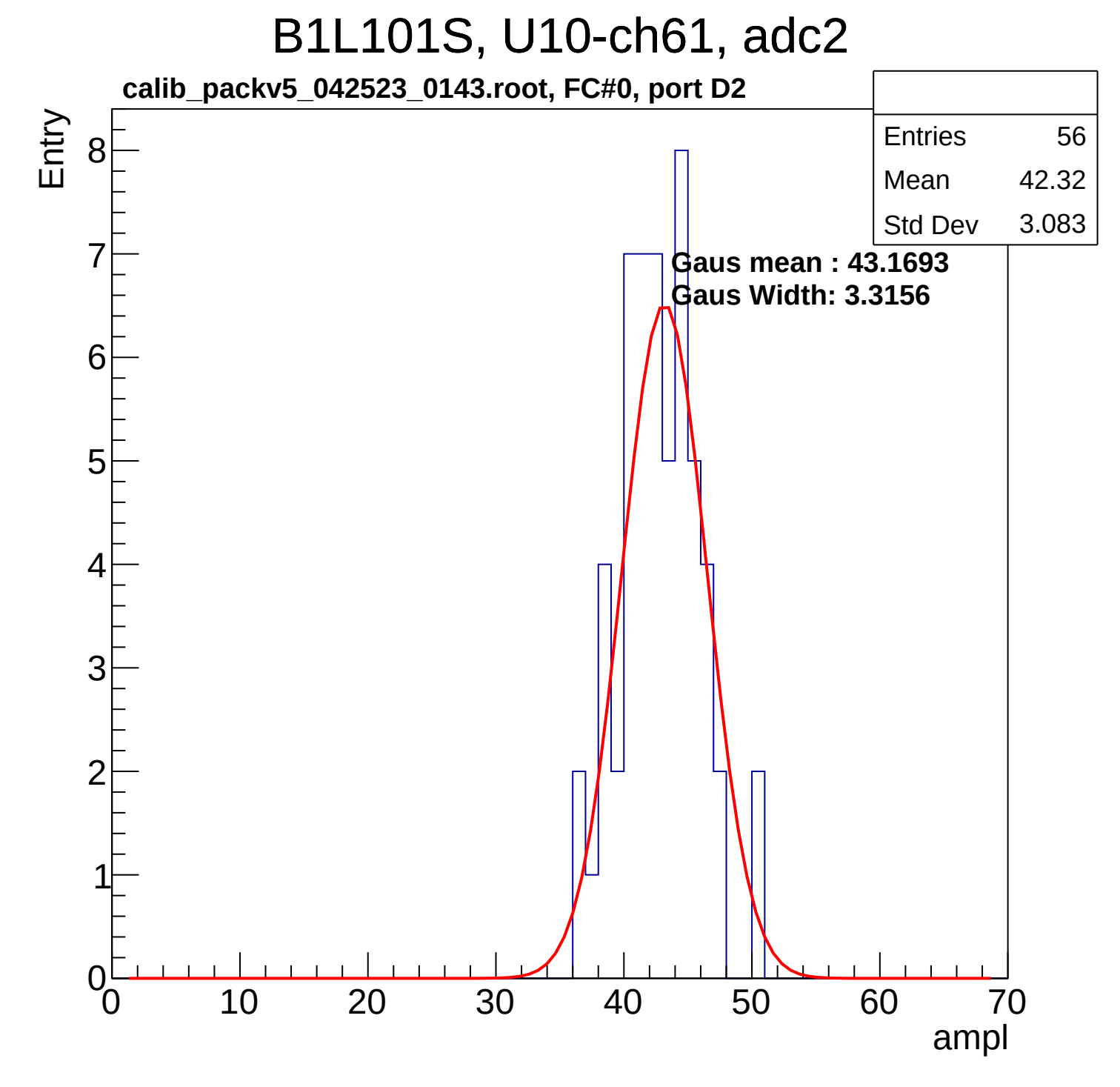
B1L101S, U10-ch61, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 42.32
Std Dev 3.083
Gaus mean : 43.1693
Gaus Width: 3.3156
Entry
ampl
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4
5
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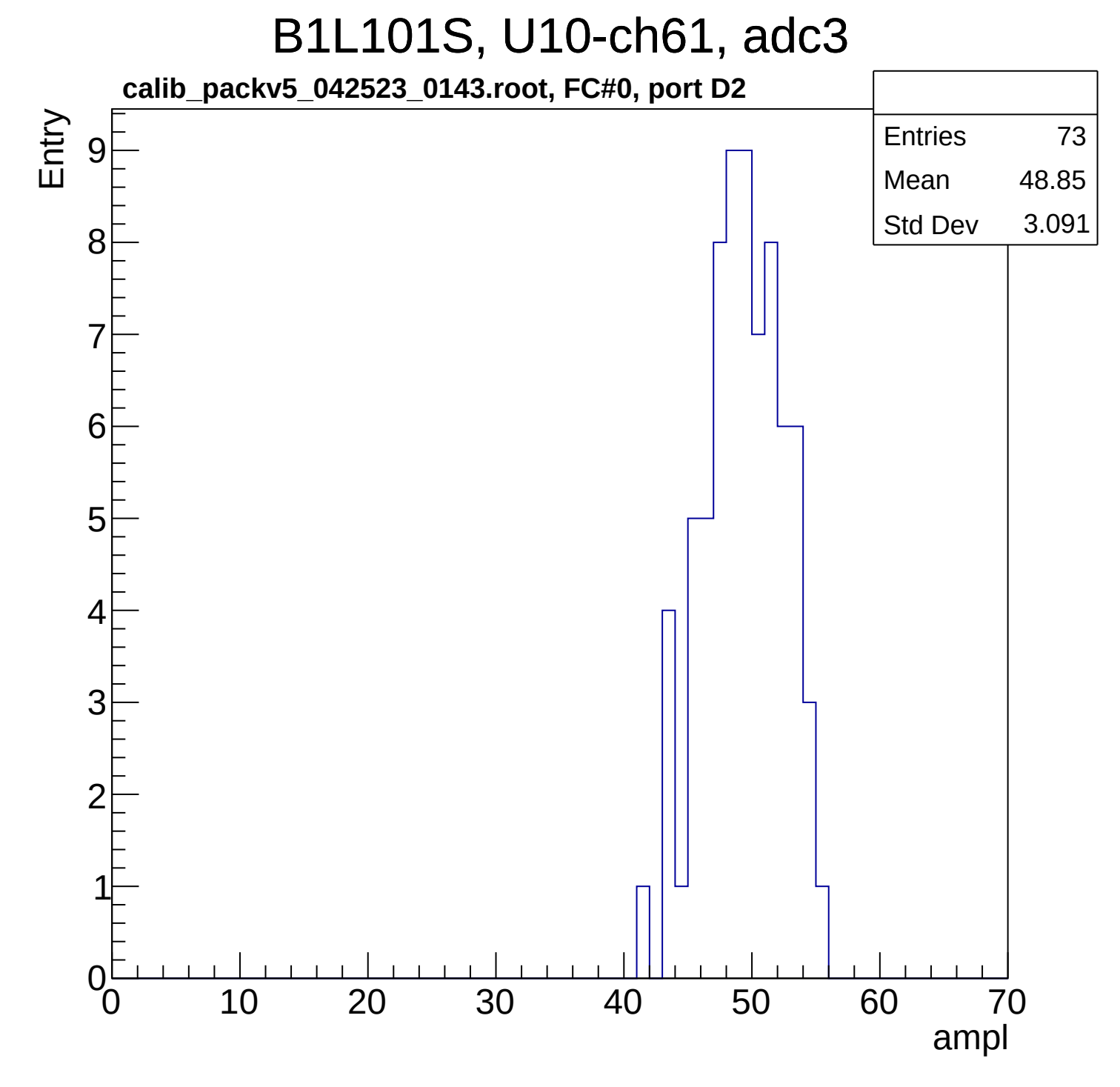
B1L101S, U10-ch61, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 48.85
Std Dev 3.091
Entry
ampl
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4
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7
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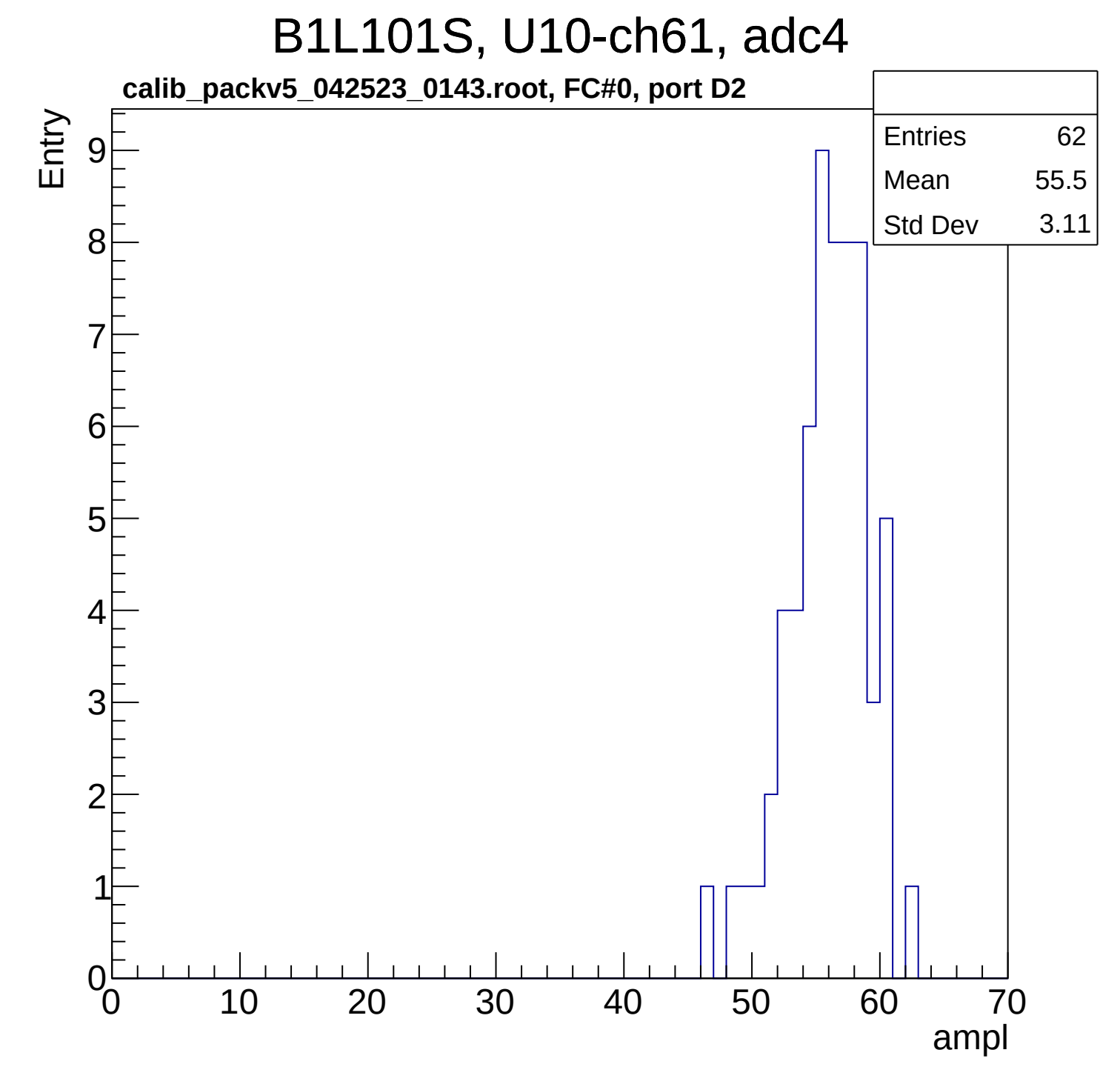
B1L101S, U10-ch61, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 55.5
Std Dev 3.11
Entry
ampl
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0
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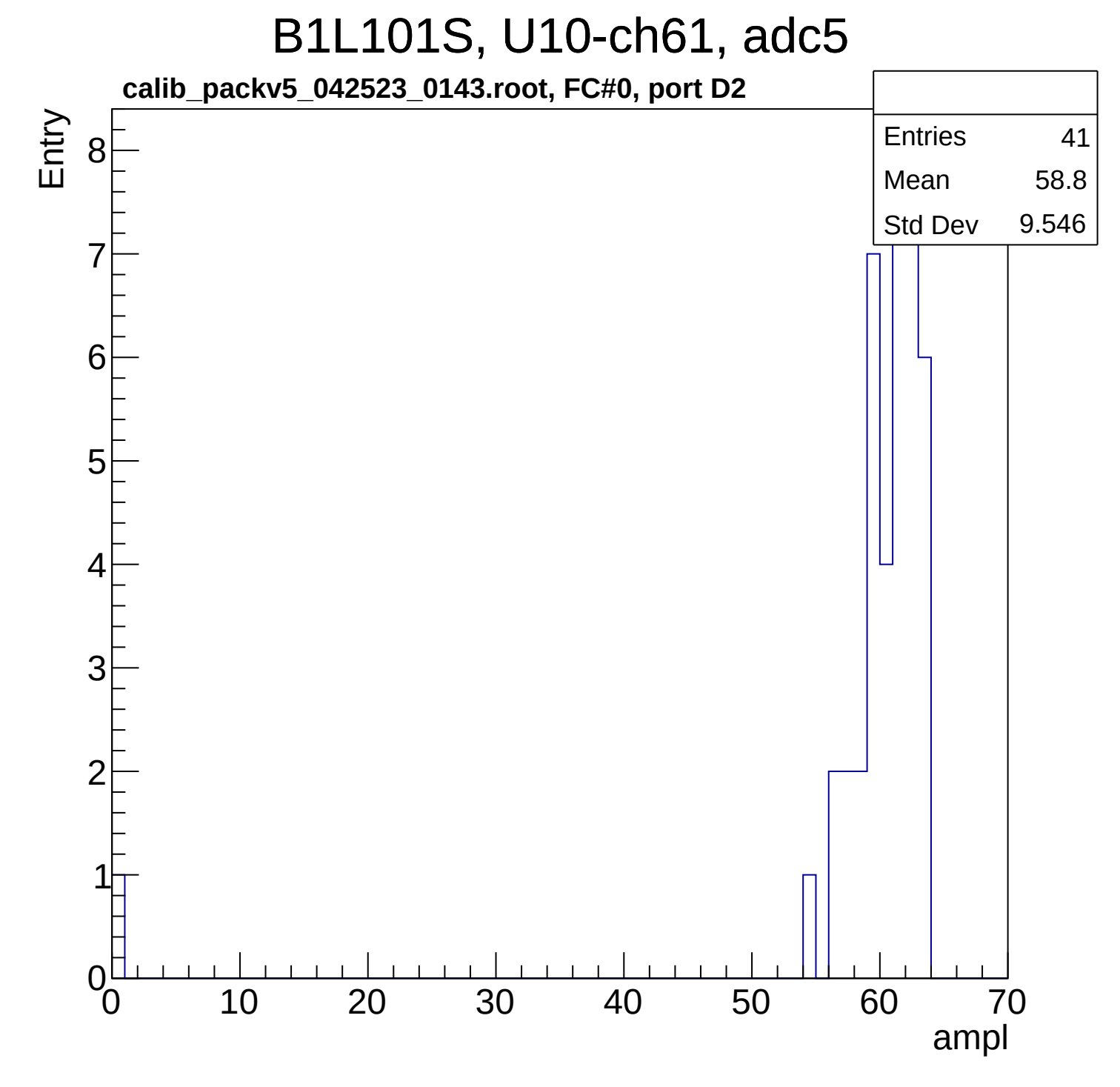
B1L101S, U10-ch61, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 41
Mean 58.8
Std Dev 9.546
Entry
ampl
0
1
2
3
4
5
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7
8
0
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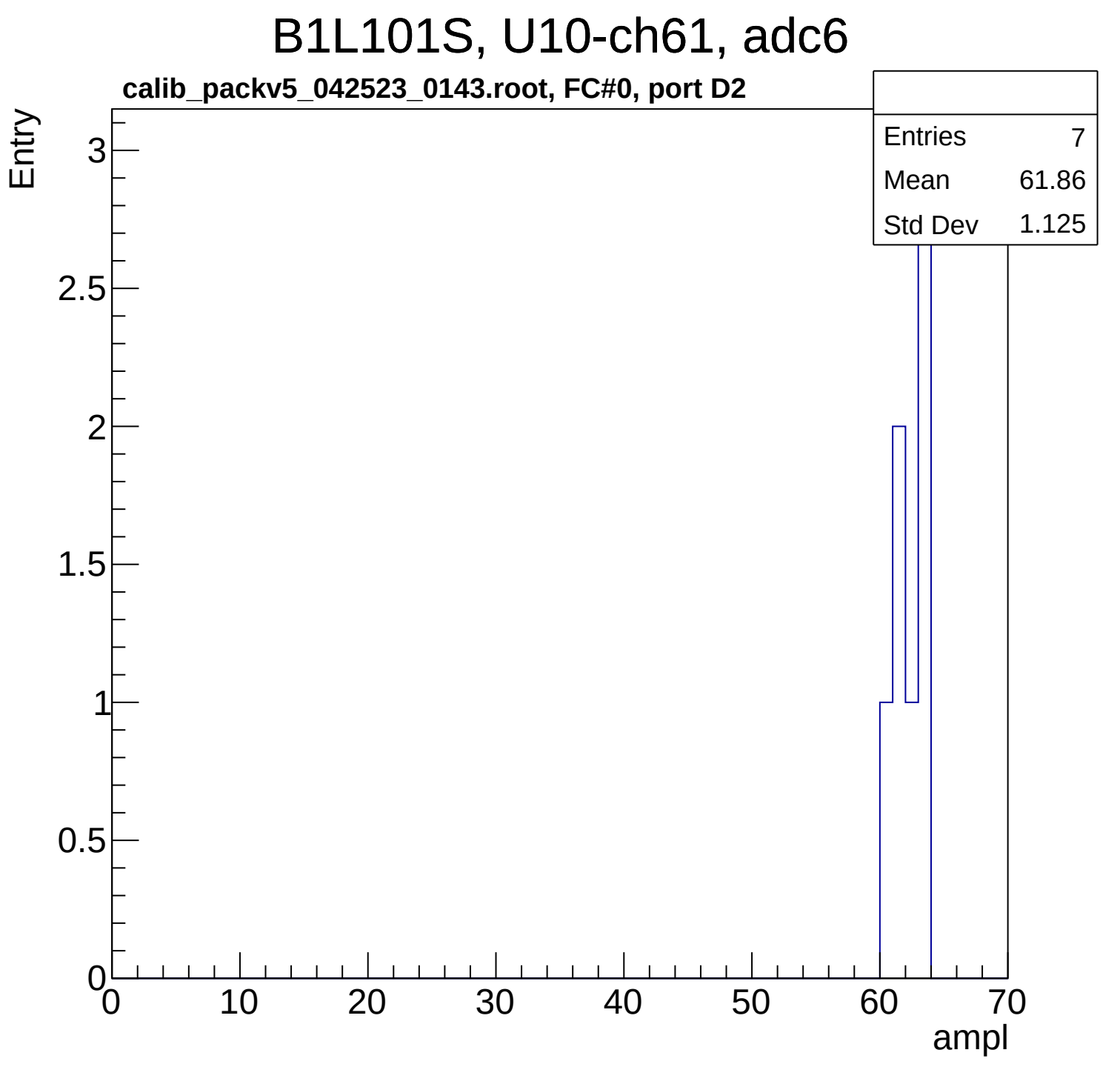
60
70


B1L101S, U10-ch61, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 61.86
Std Dev 1.125
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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60
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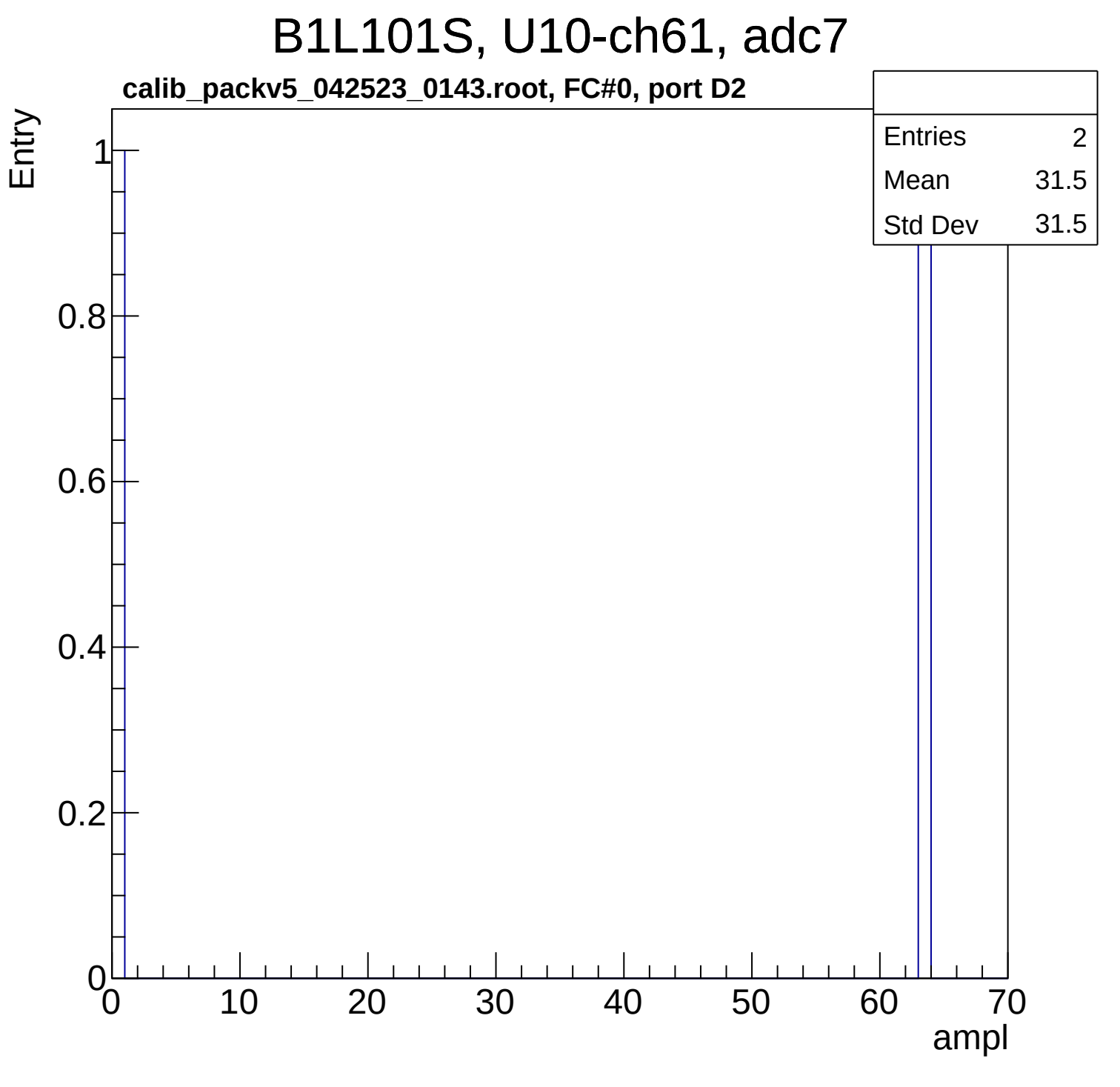
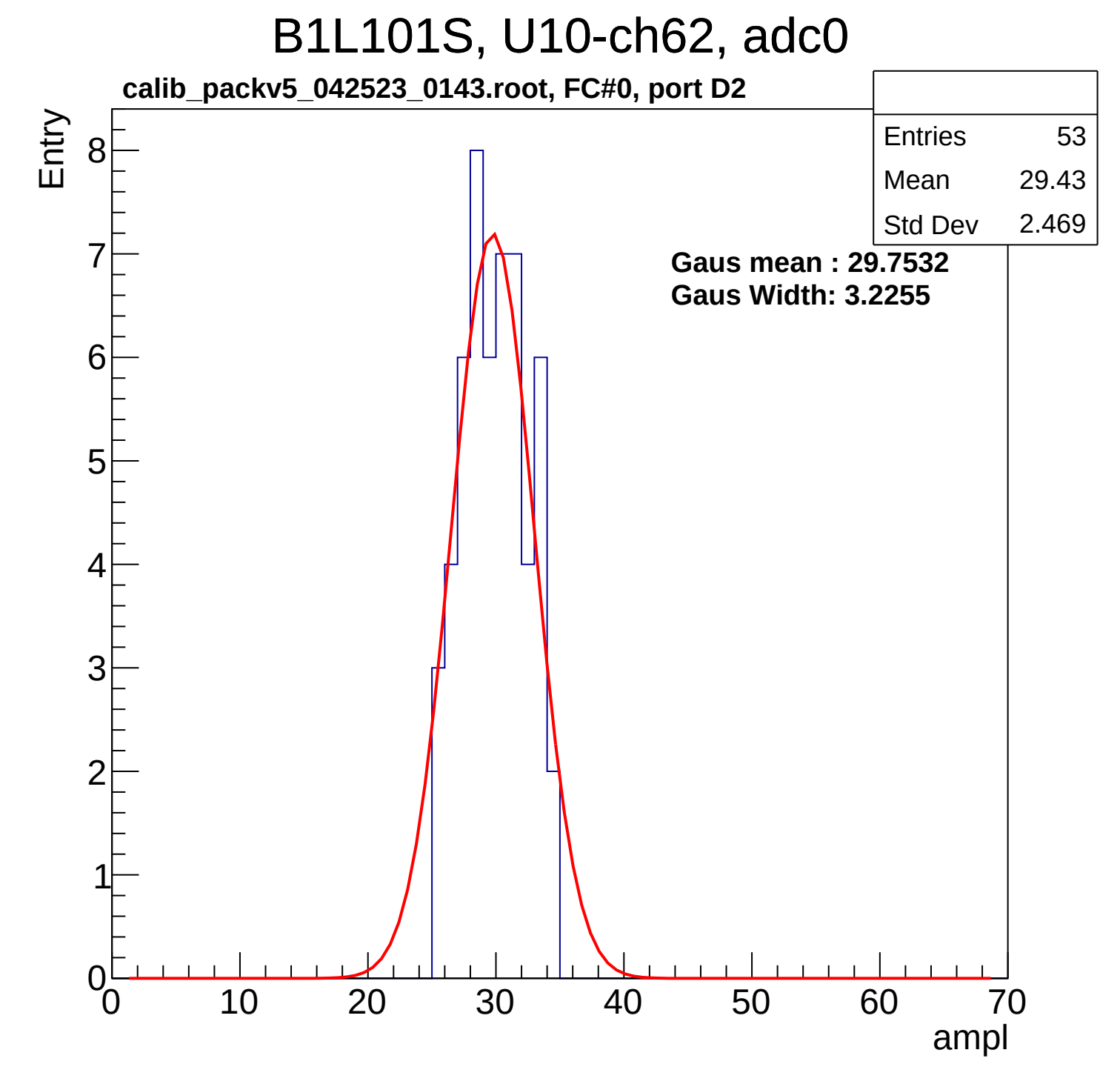

B1L101S, U10-ch61, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch62, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 29.43
Std Dev 2.469
Gaus mean : 29.7532
Gaus Width: 3.2255
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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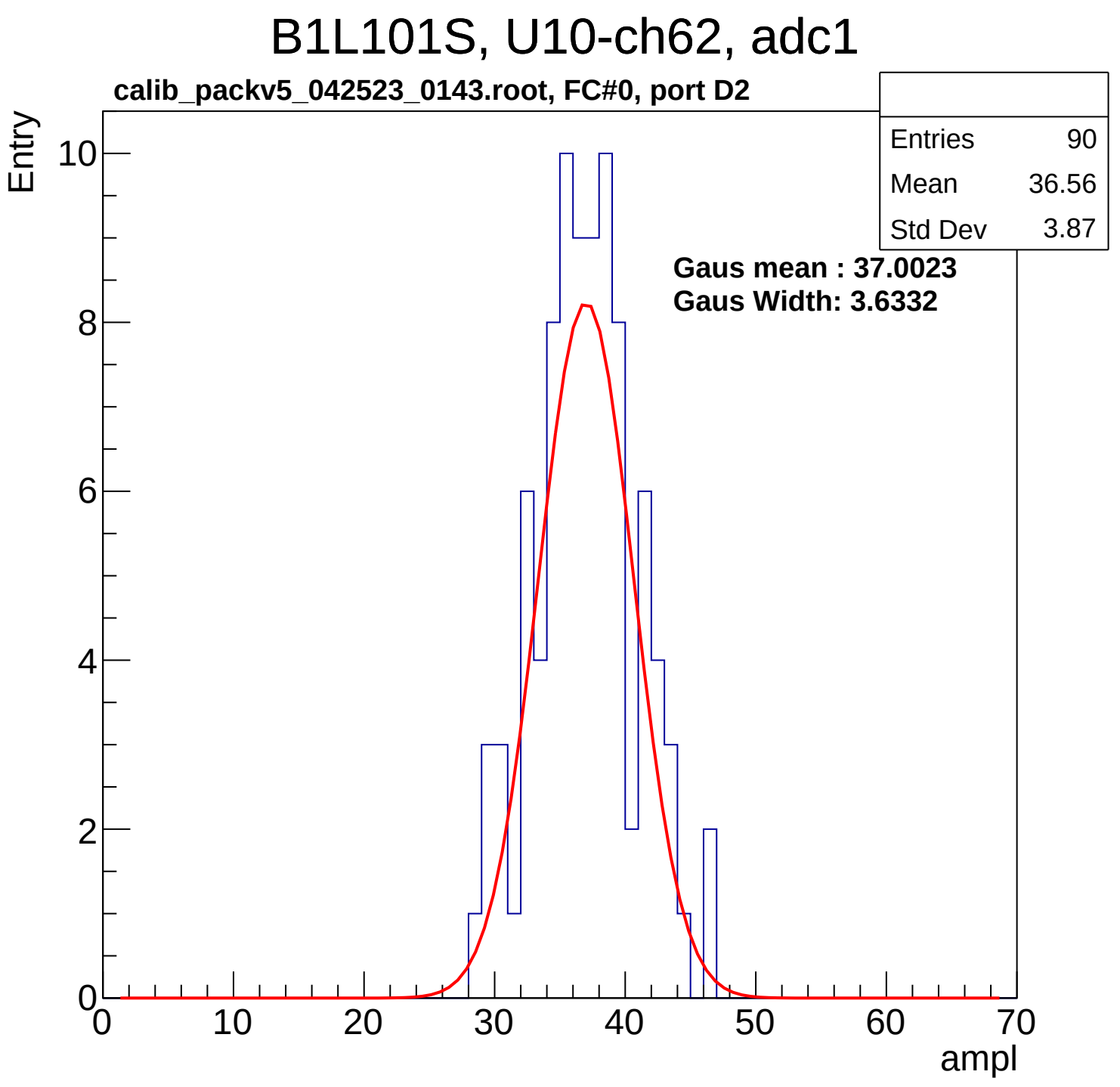
B1L101S, U10-ch62, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 90
Mean 36.56
Std Dev 3.87
Gaus mean : 37.0023
Gaus Width: 3.6332
Entry
ampl
0
2
4
6
8
10
0
10
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30
40
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60
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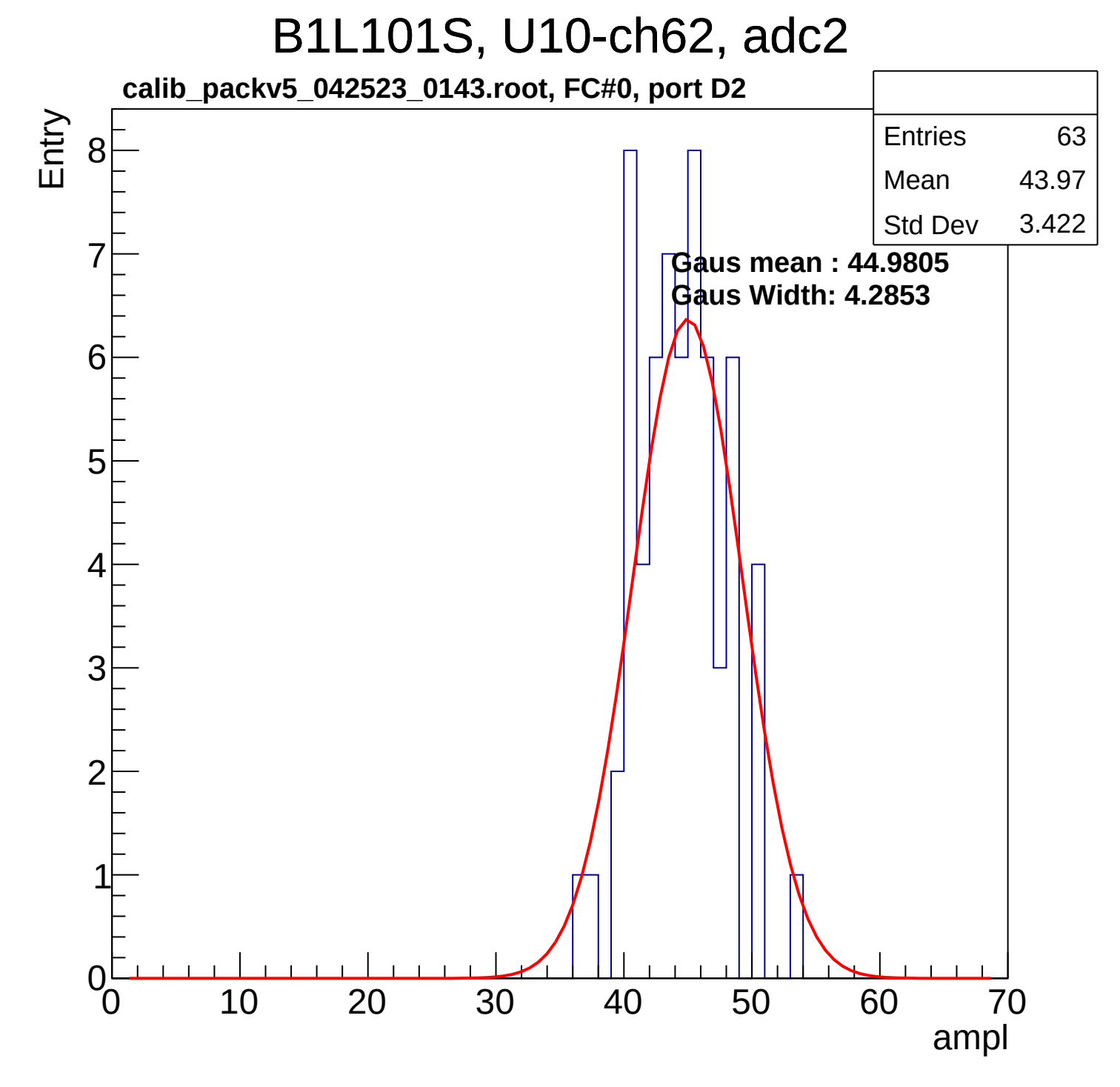
B1L101S, U10-ch62, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 43.97
Std Dev 3.422
Gaus mean : 44.9805
Gaus Width: 4.2853
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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40
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60
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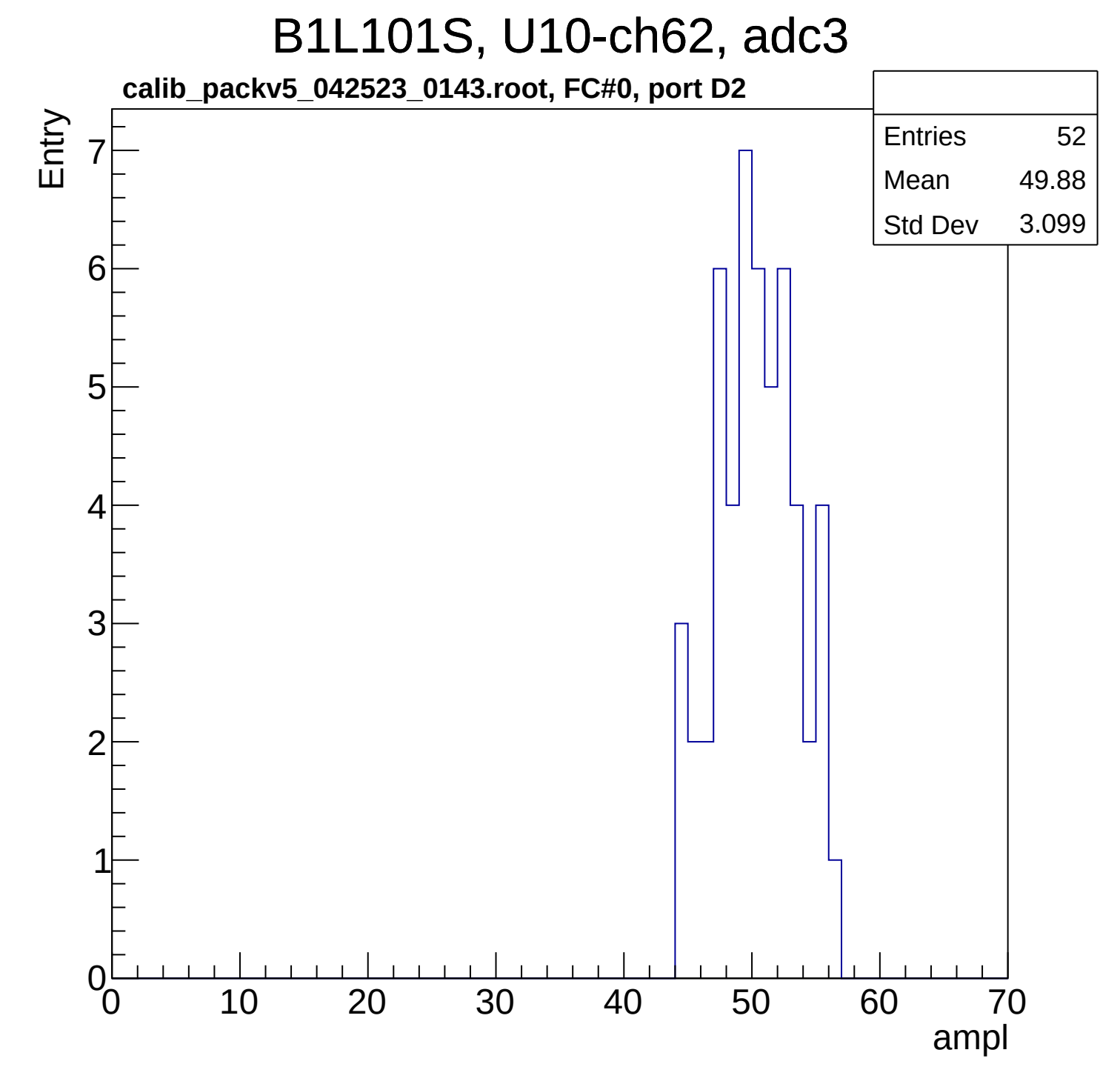
B1L101S, U10-ch62, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 49.88
Std Dev 3.099
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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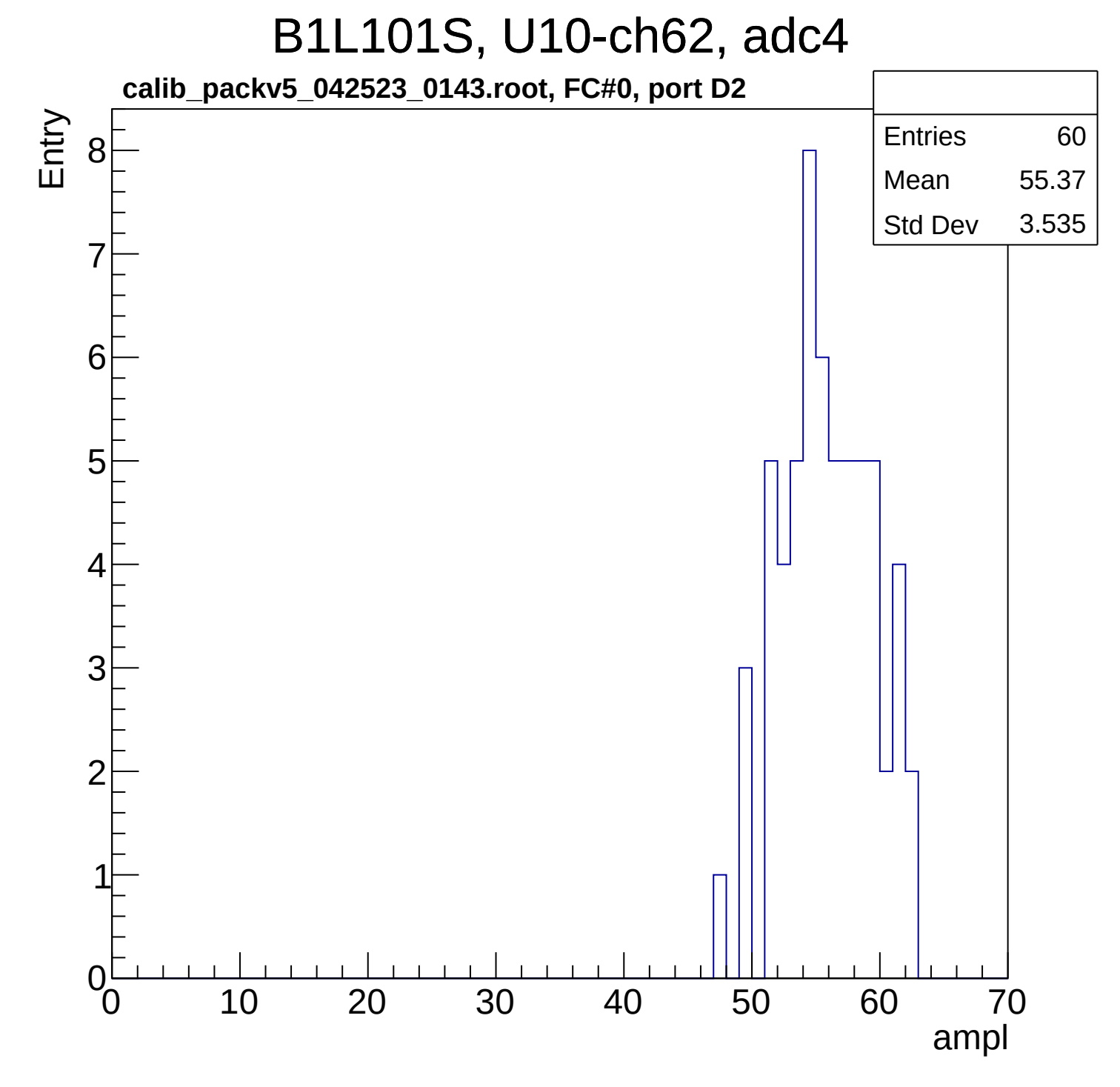
B1L101S, U10-ch62, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 55.37
Std Dev 3.535
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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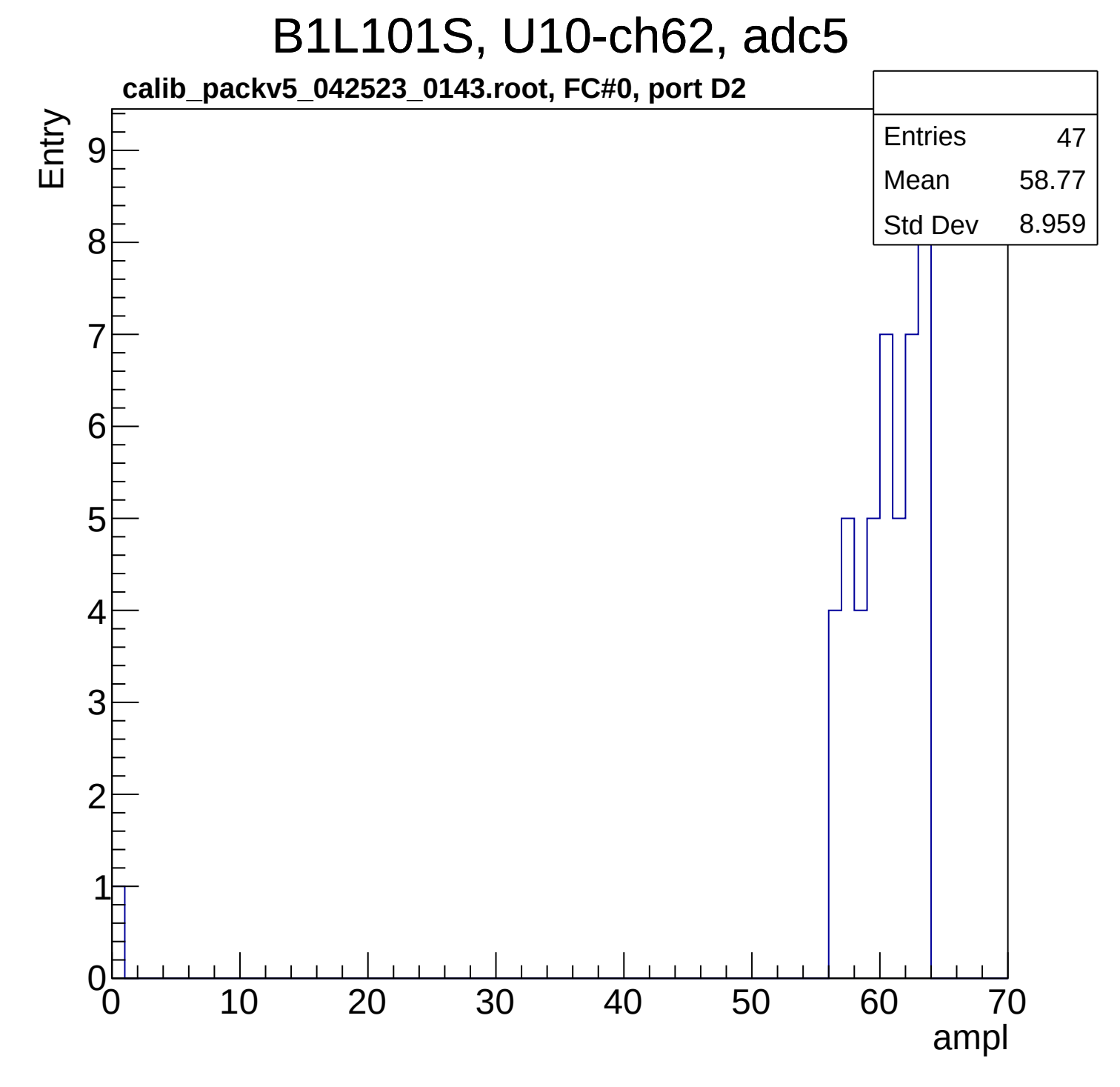
B1L101S, U10-ch62, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 58.77
Std Dev 8.959
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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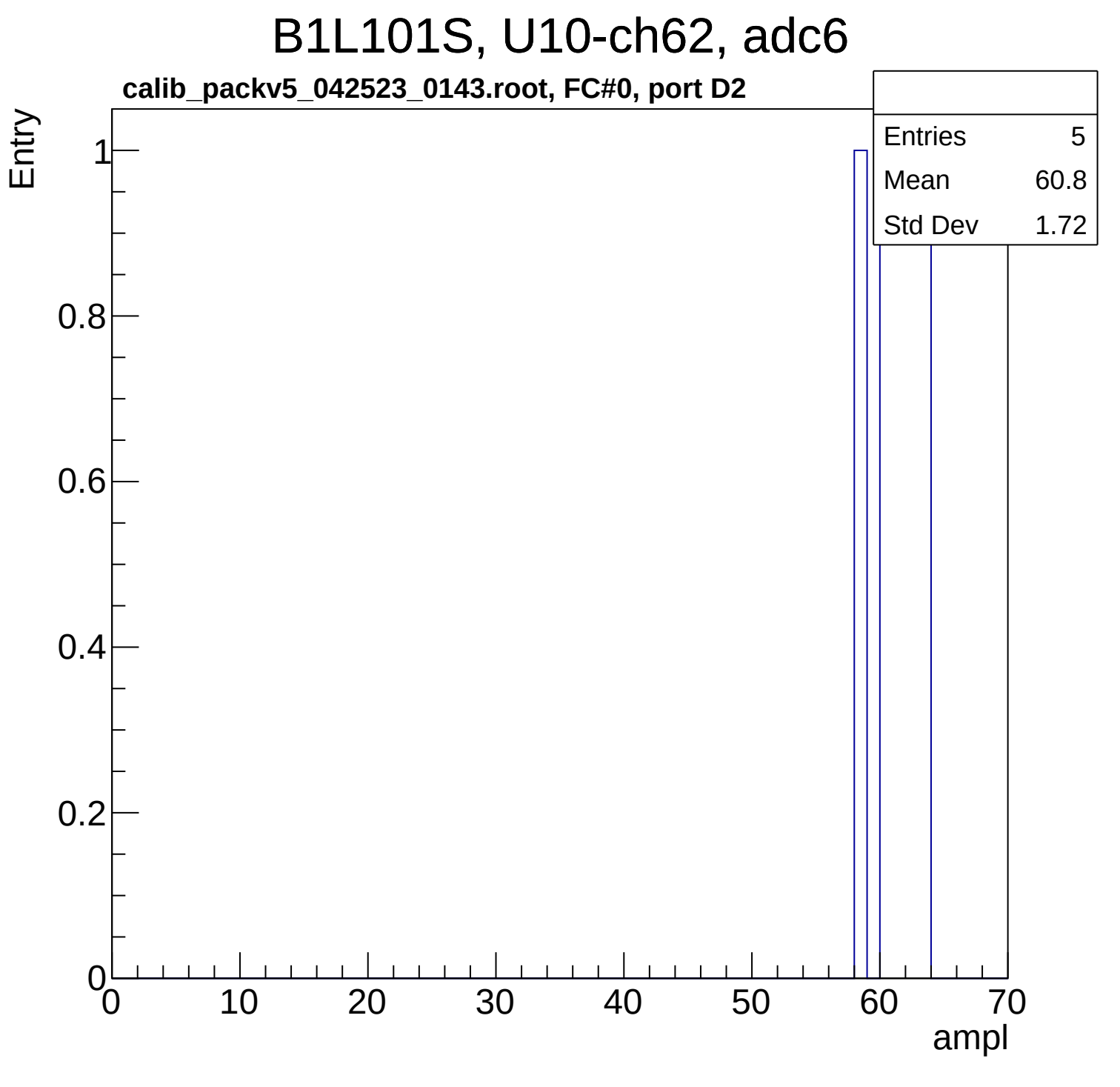
B1L101S, U10-ch62, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 60.8
Std Dev 1.72
Entry
1
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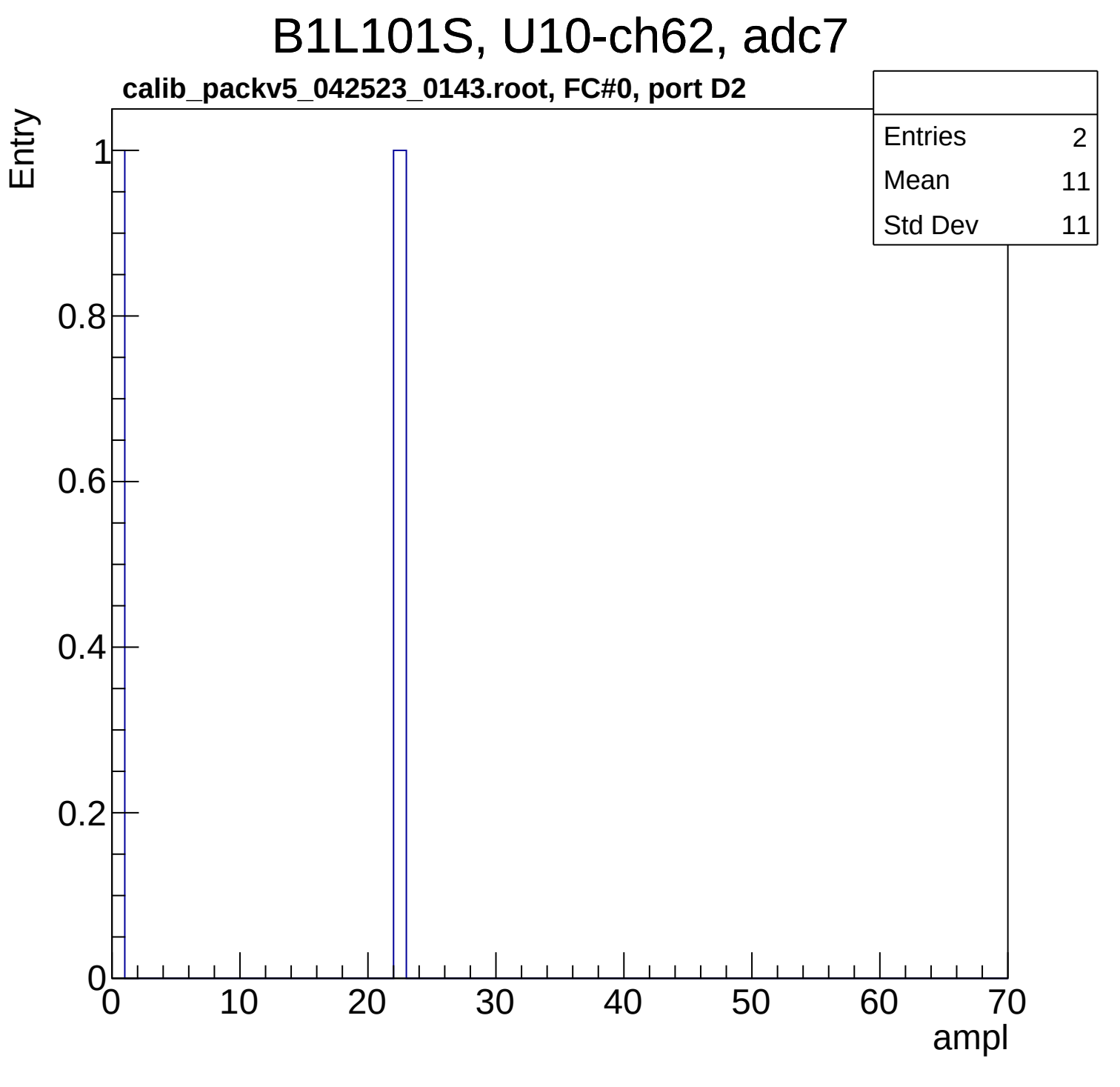
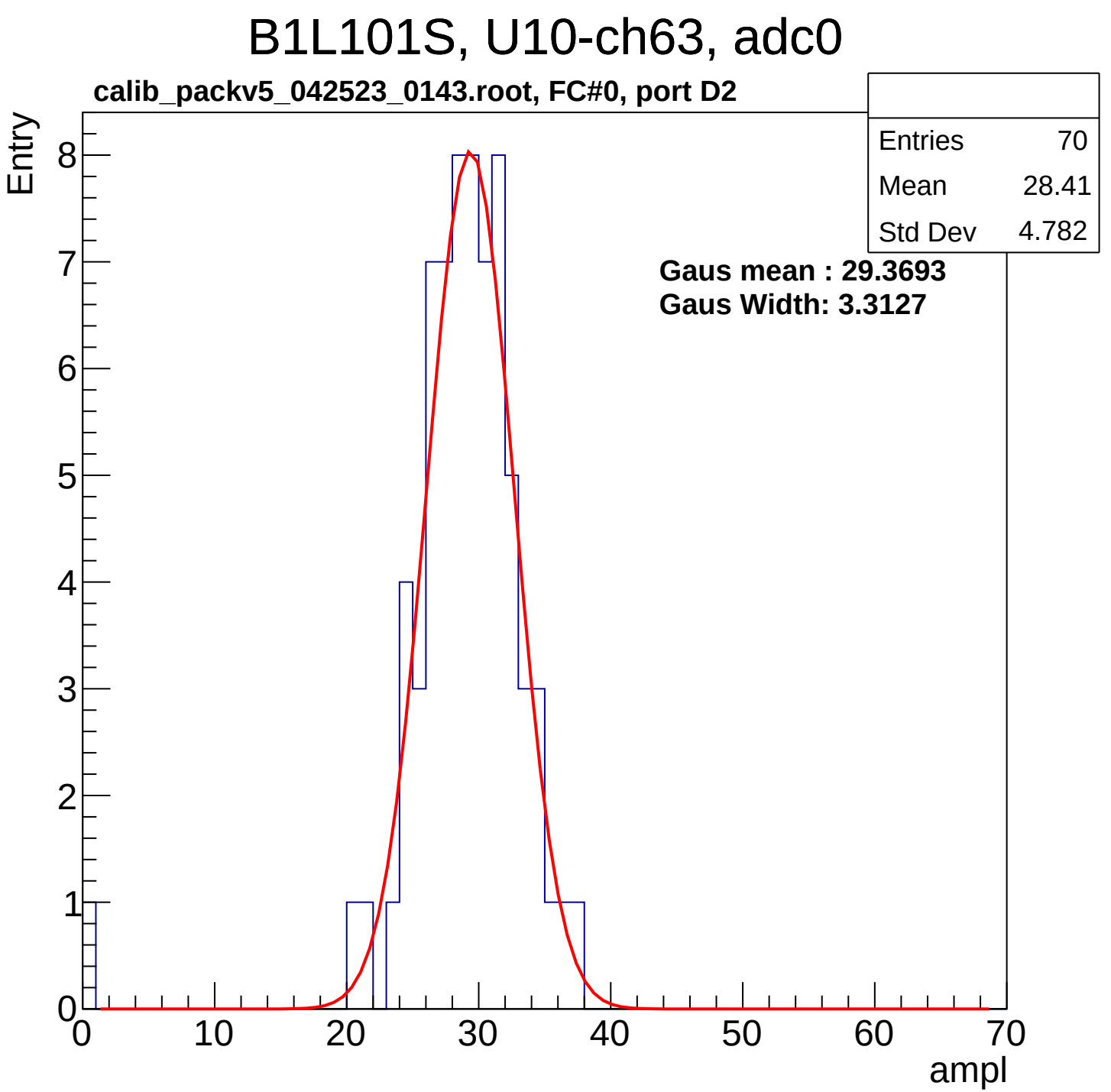
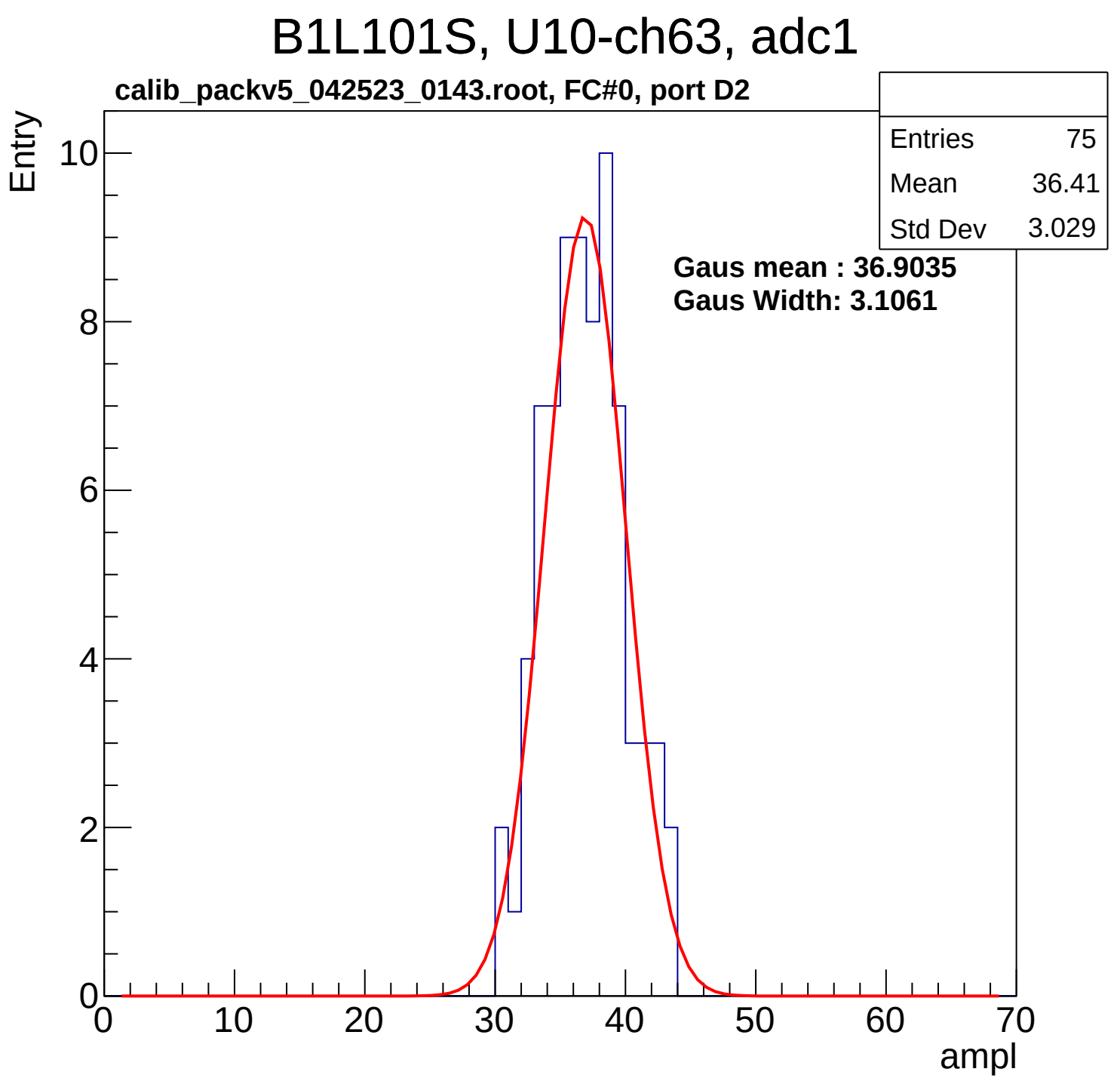
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch62, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 11
Std Dev 11
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch63, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 28.41
Std Dev 4.782
Gaus mean : 29.3693
Gaus Width: 3.3127
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch63, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 36.41
Std Dev 3.029
Gaus mean : 36.9035
Gaus Width: 3.1061
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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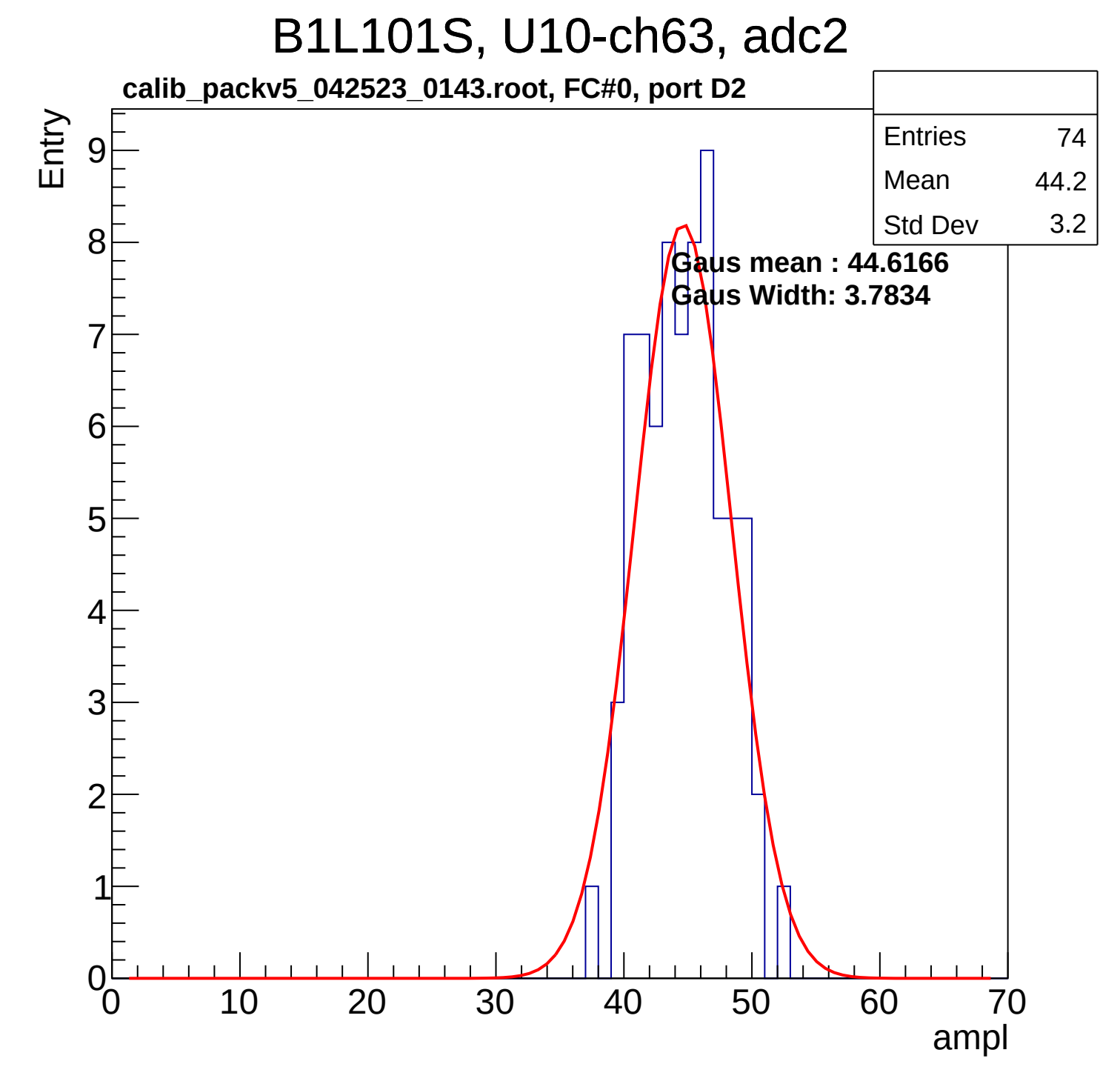
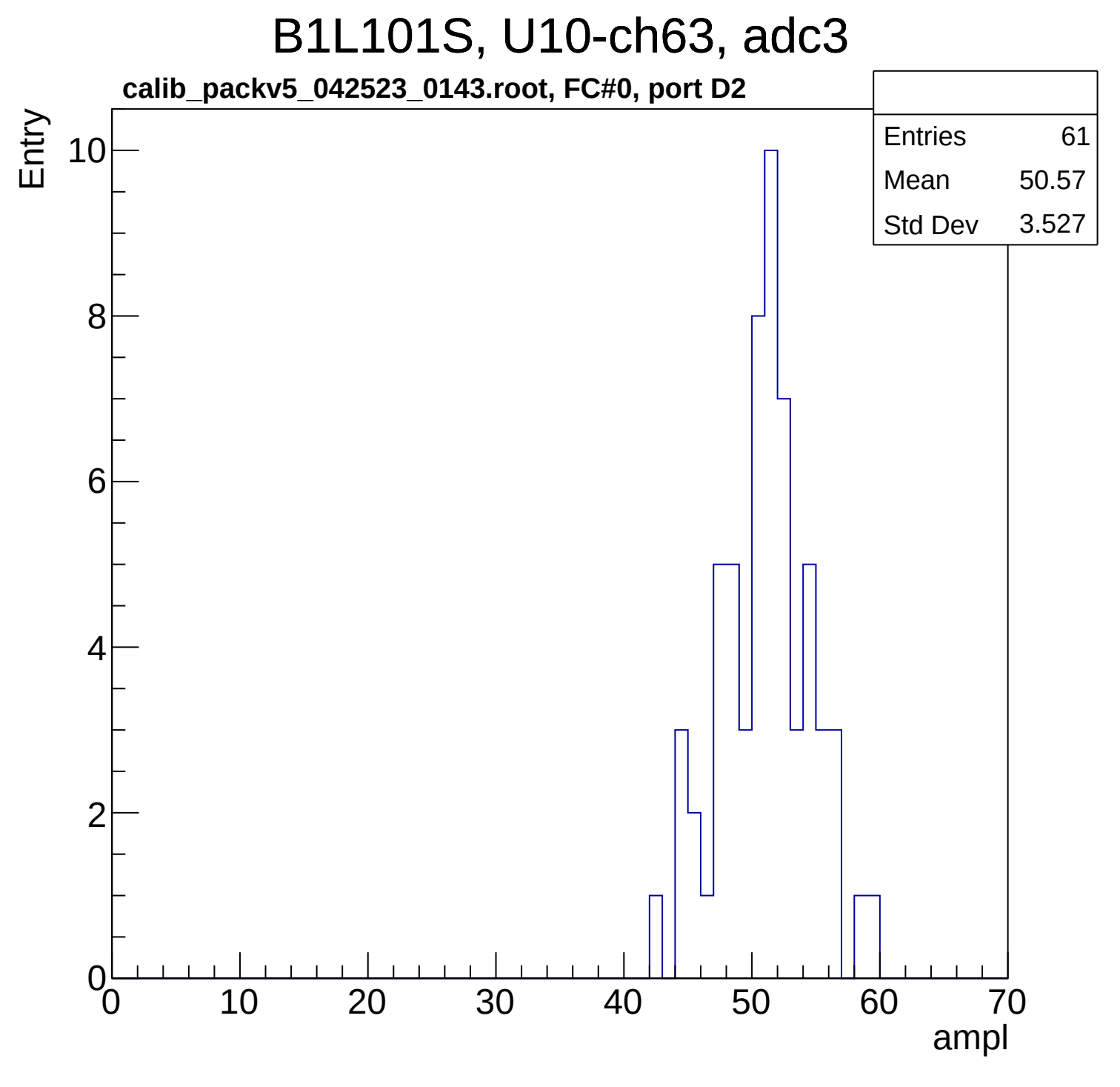
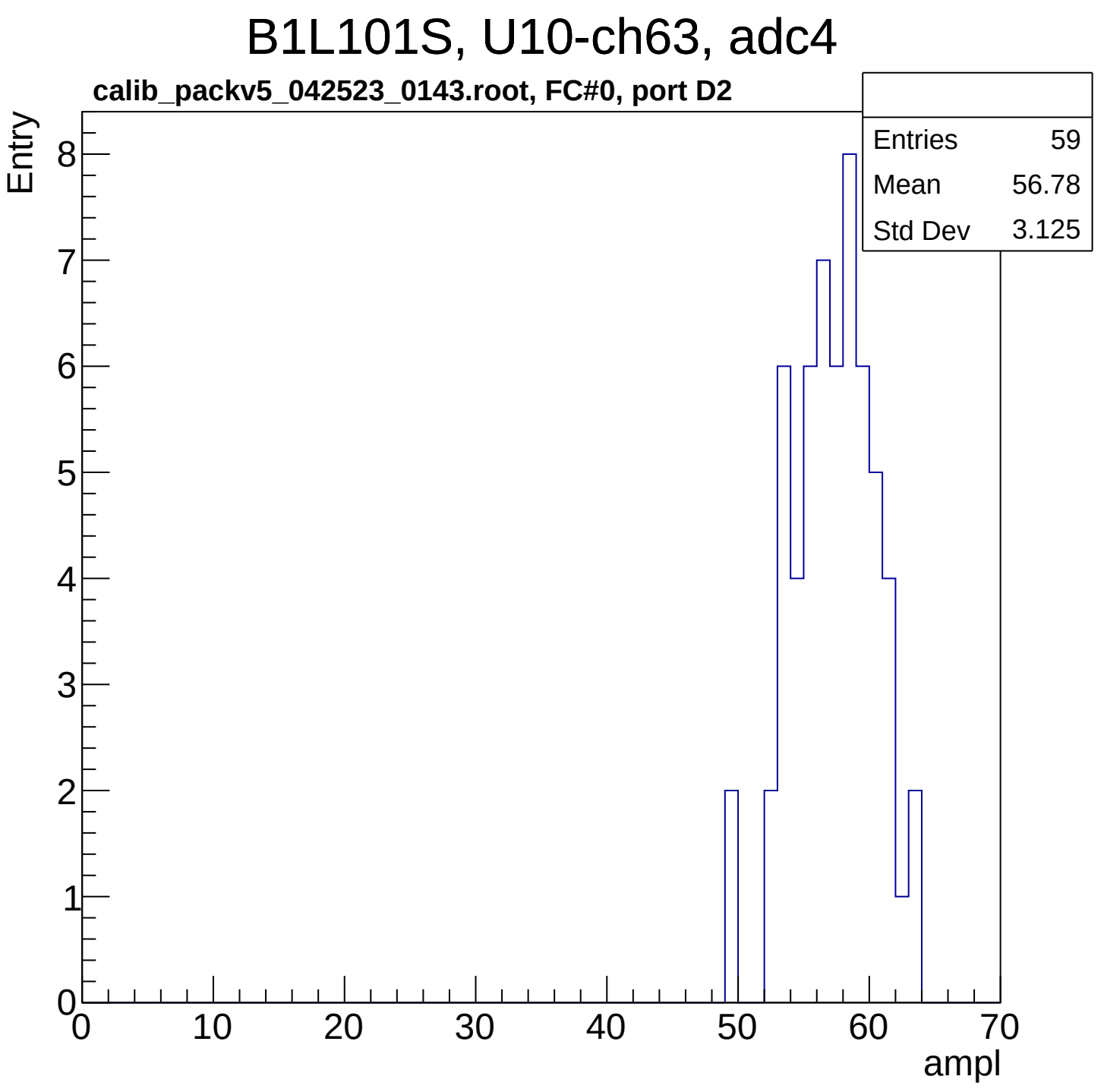
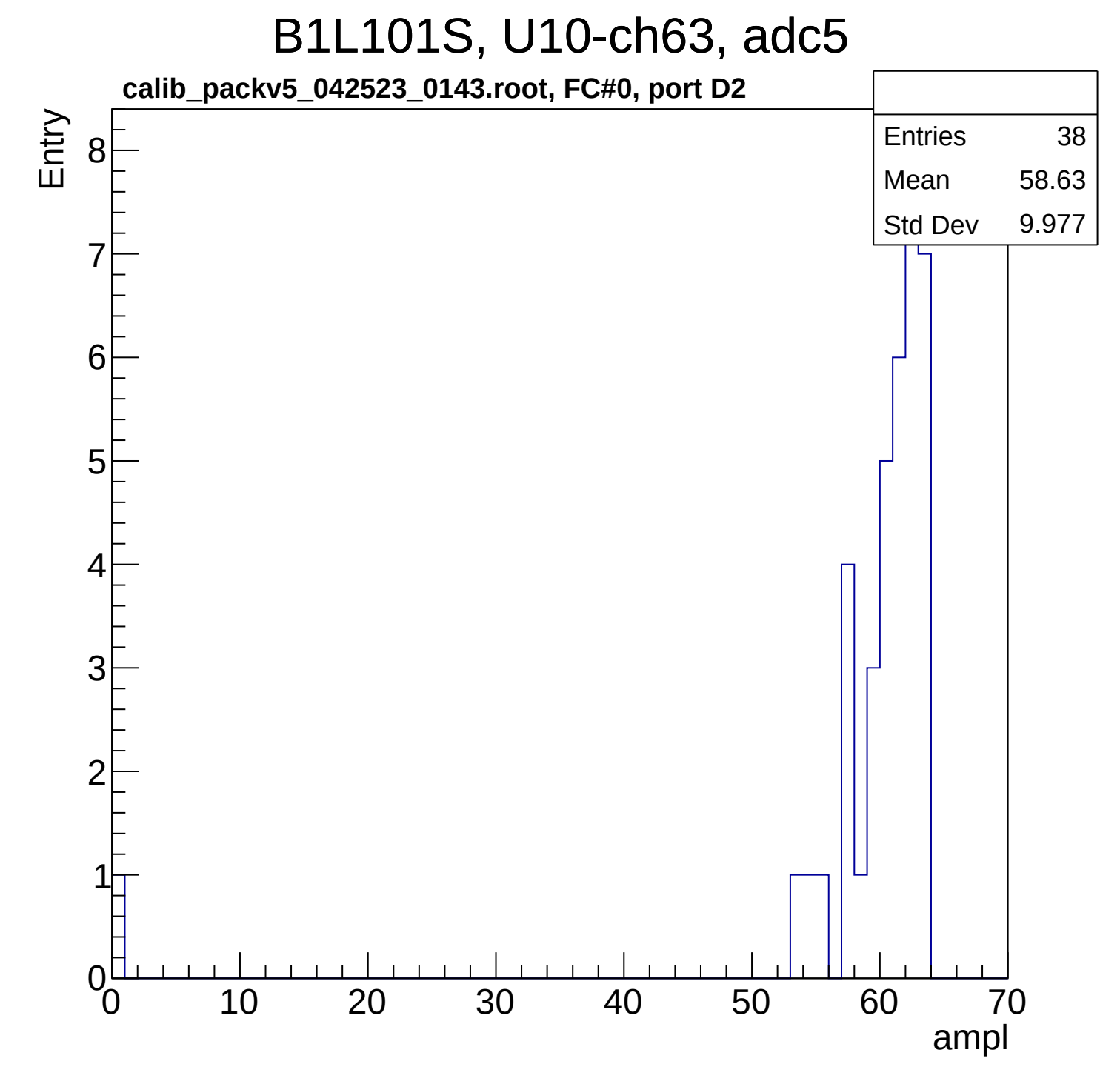

B1L101S, U10-ch63, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 44.2
Std Dev 3.2
Gaus mean : 44.6166
Gaus Width: 3.7834
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch63, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 50.57
Std Dev 3.527
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch63, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 56.78
Std Dev 3.125
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch63, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 38
Mean 58.63
Std Dev 9.977
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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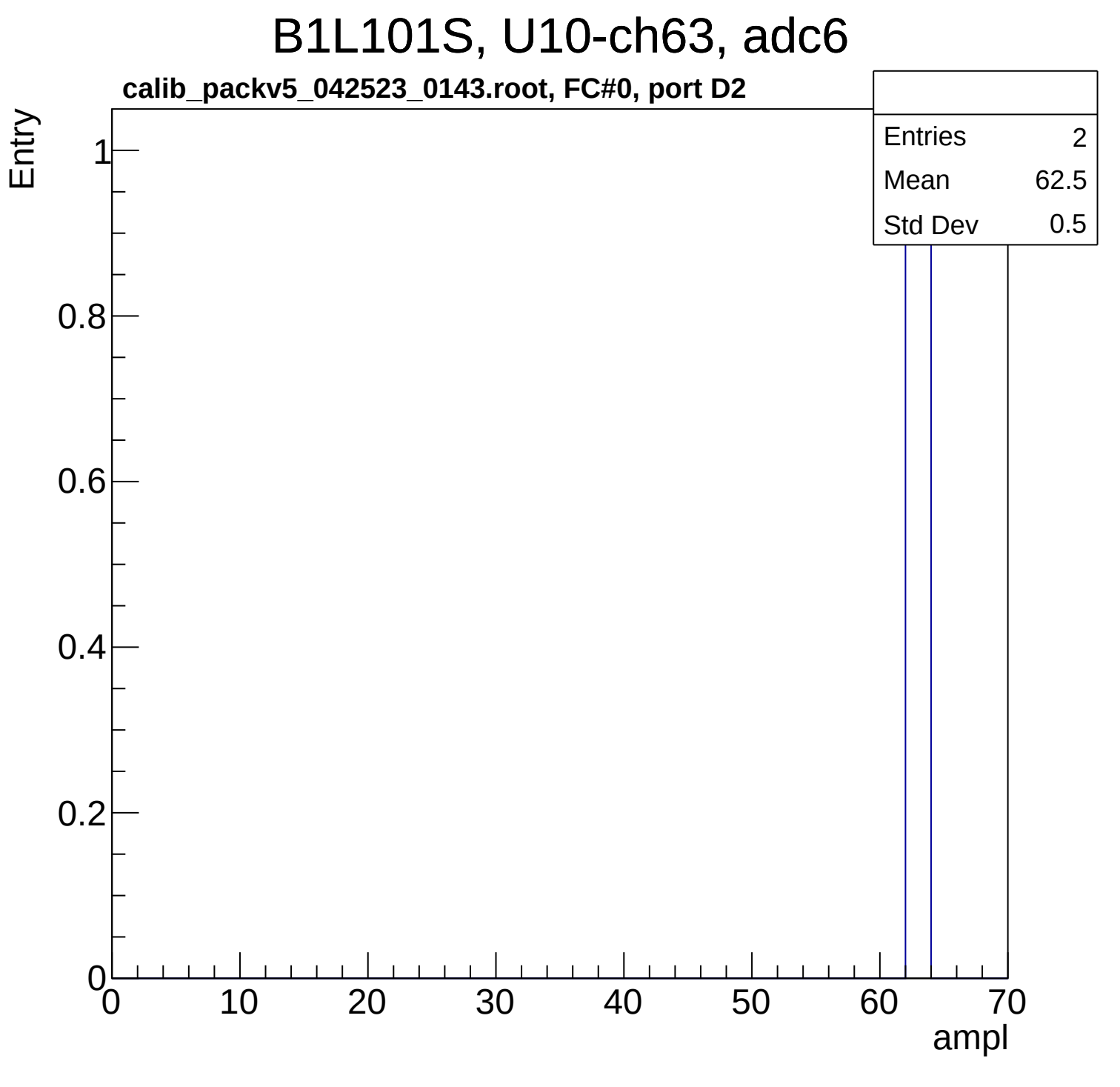
B1L101S, U10-ch63, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
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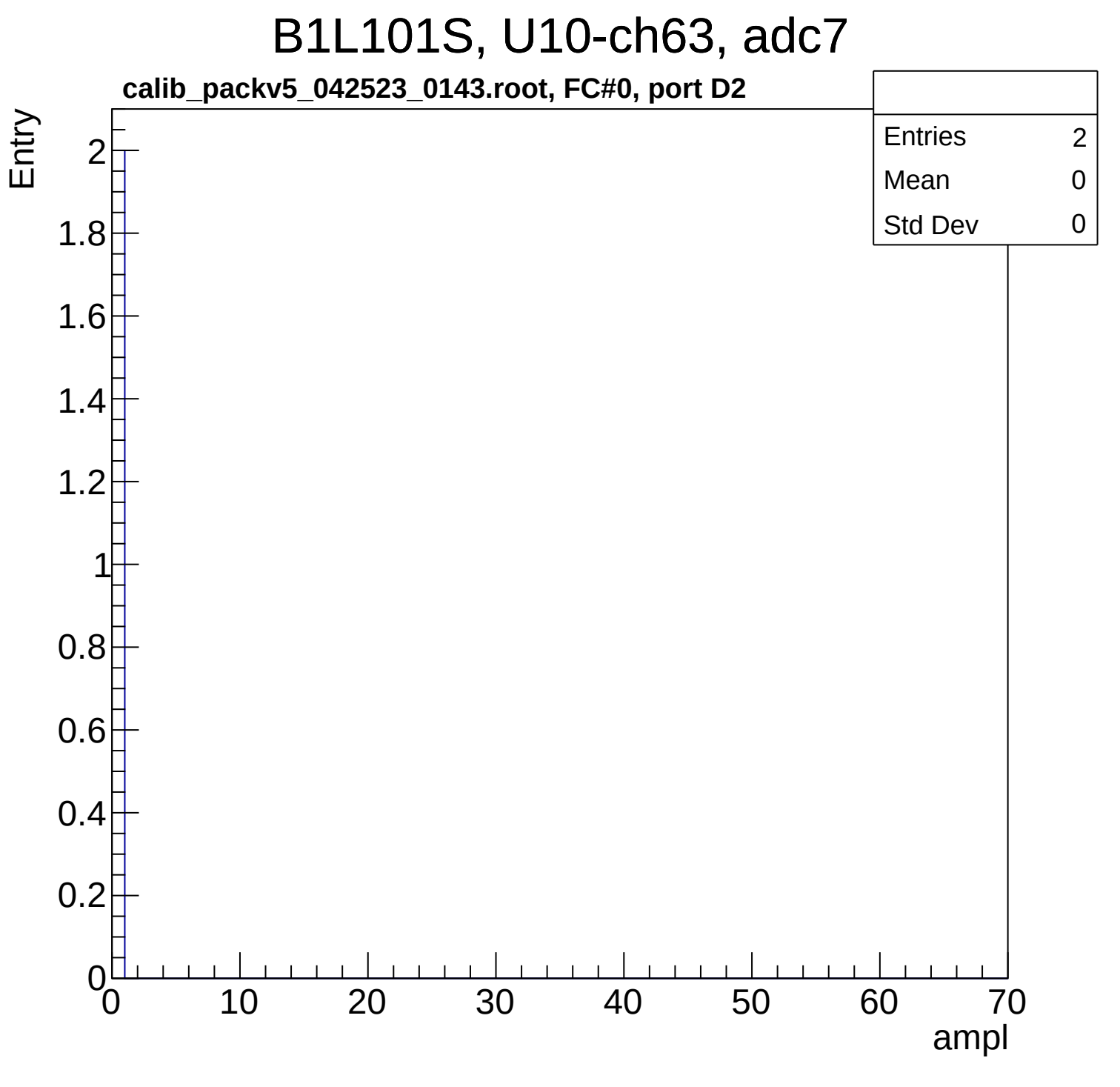
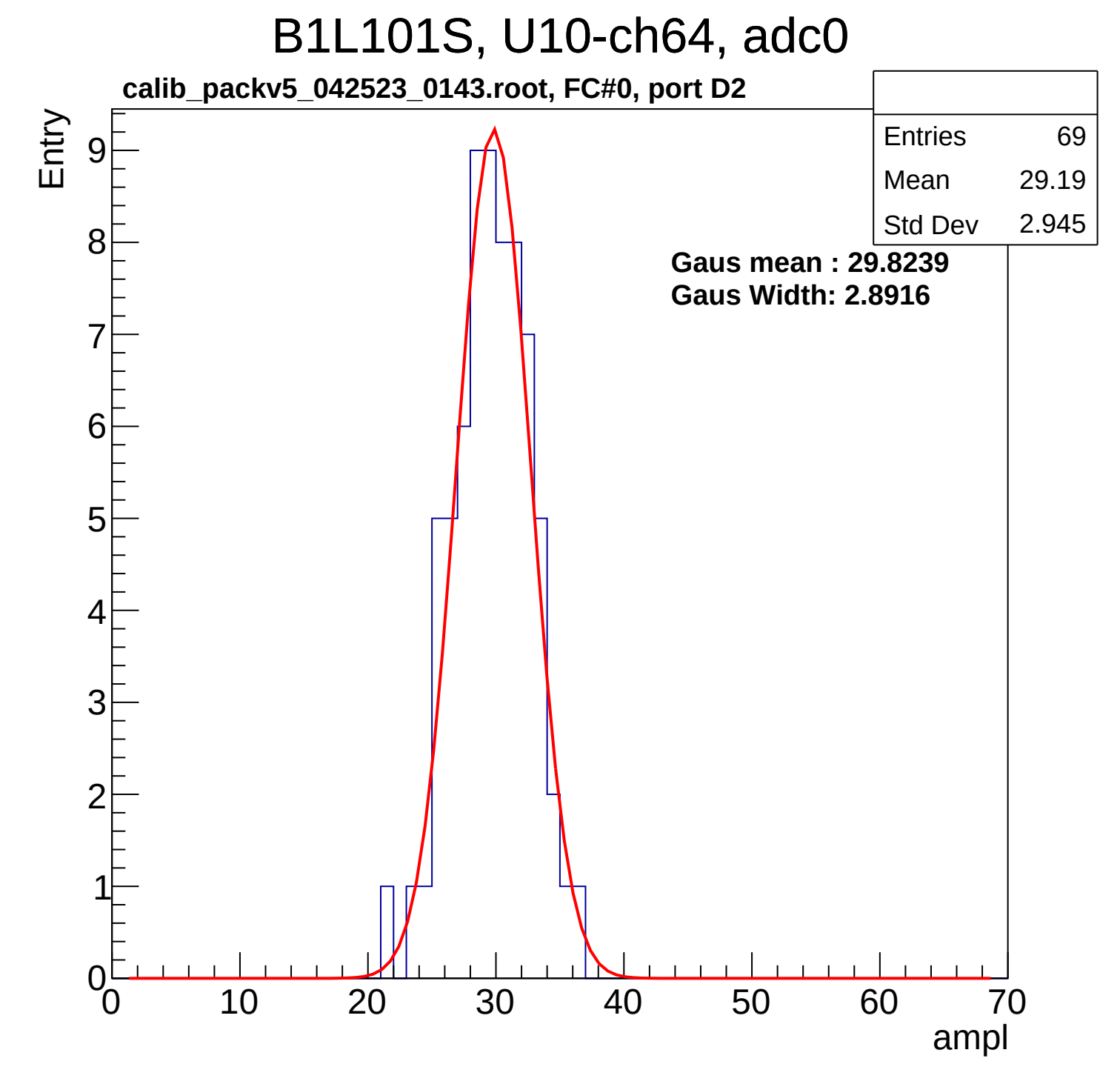
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch63, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch64, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 29.19
Std Dev 2.945
Gaus mean : 29.8239
Gaus Width: 2.8916
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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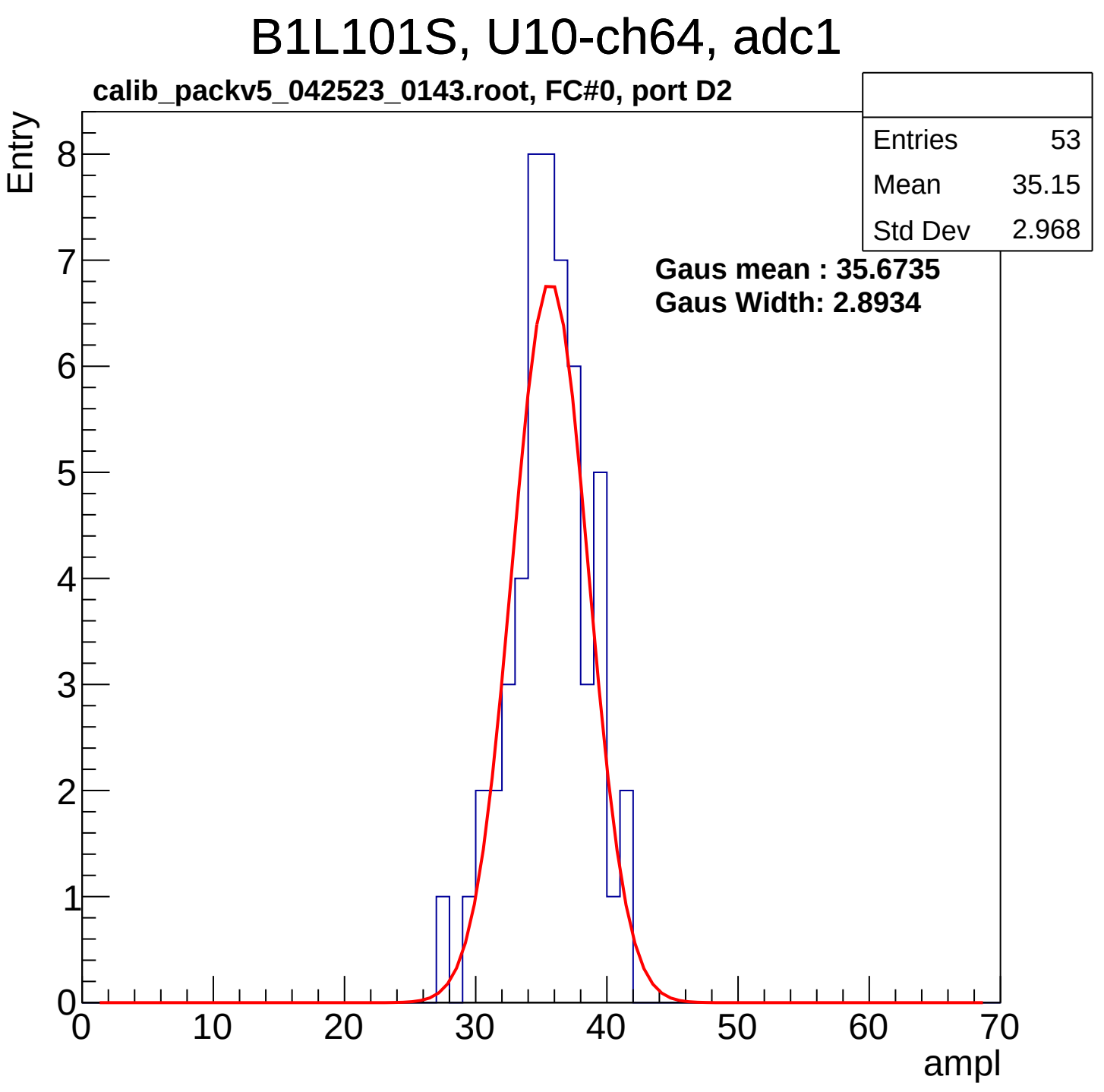
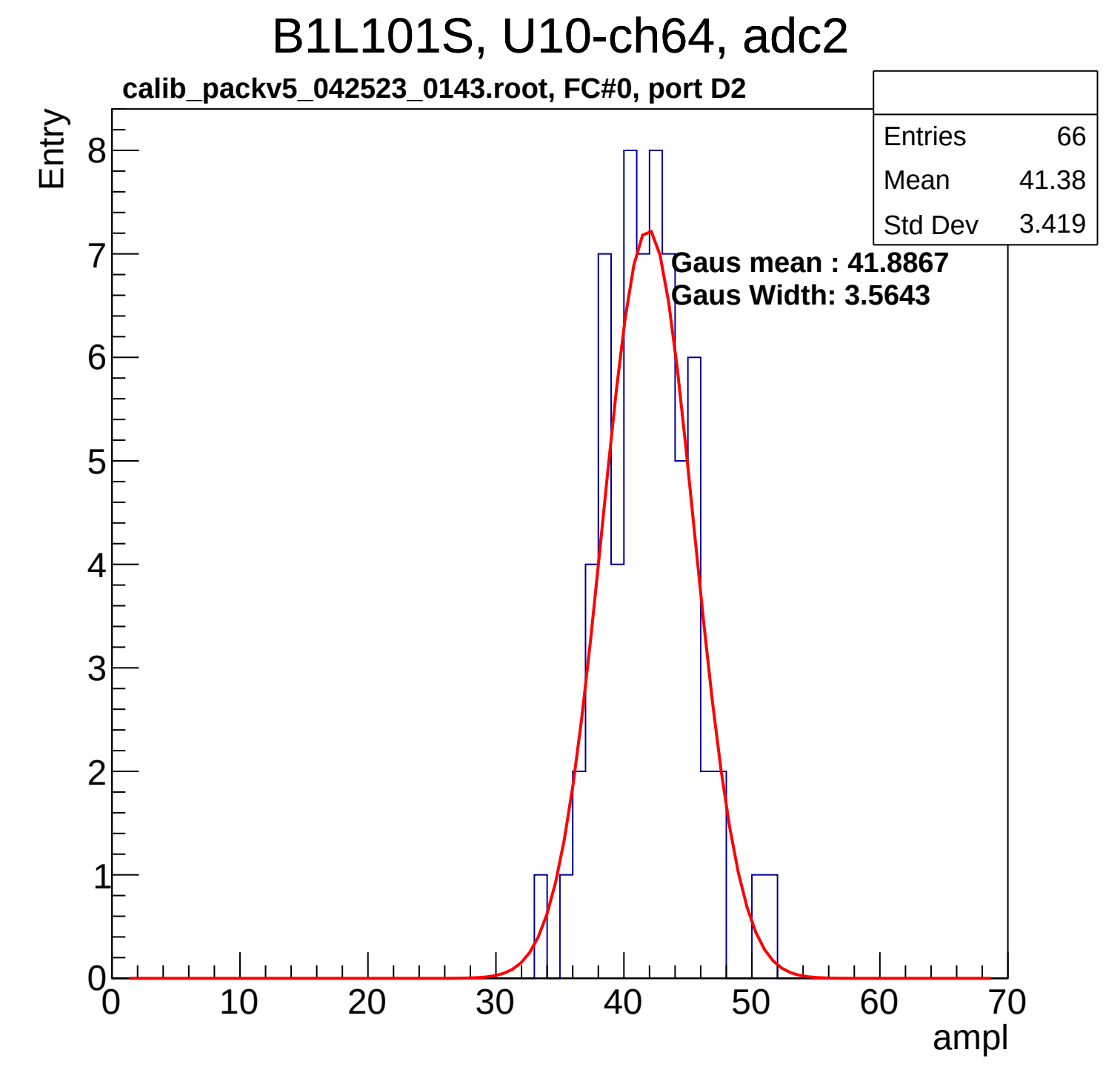

B1L101S, U10-ch64, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 35.15
Std Dev 2.968
Gaus mean : 35.6735
Gaus Width: 2.8934
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch64, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 41.38
Std Dev 3.419
Gaus mean : 41.8867
Gaus Width: 3.5643
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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60
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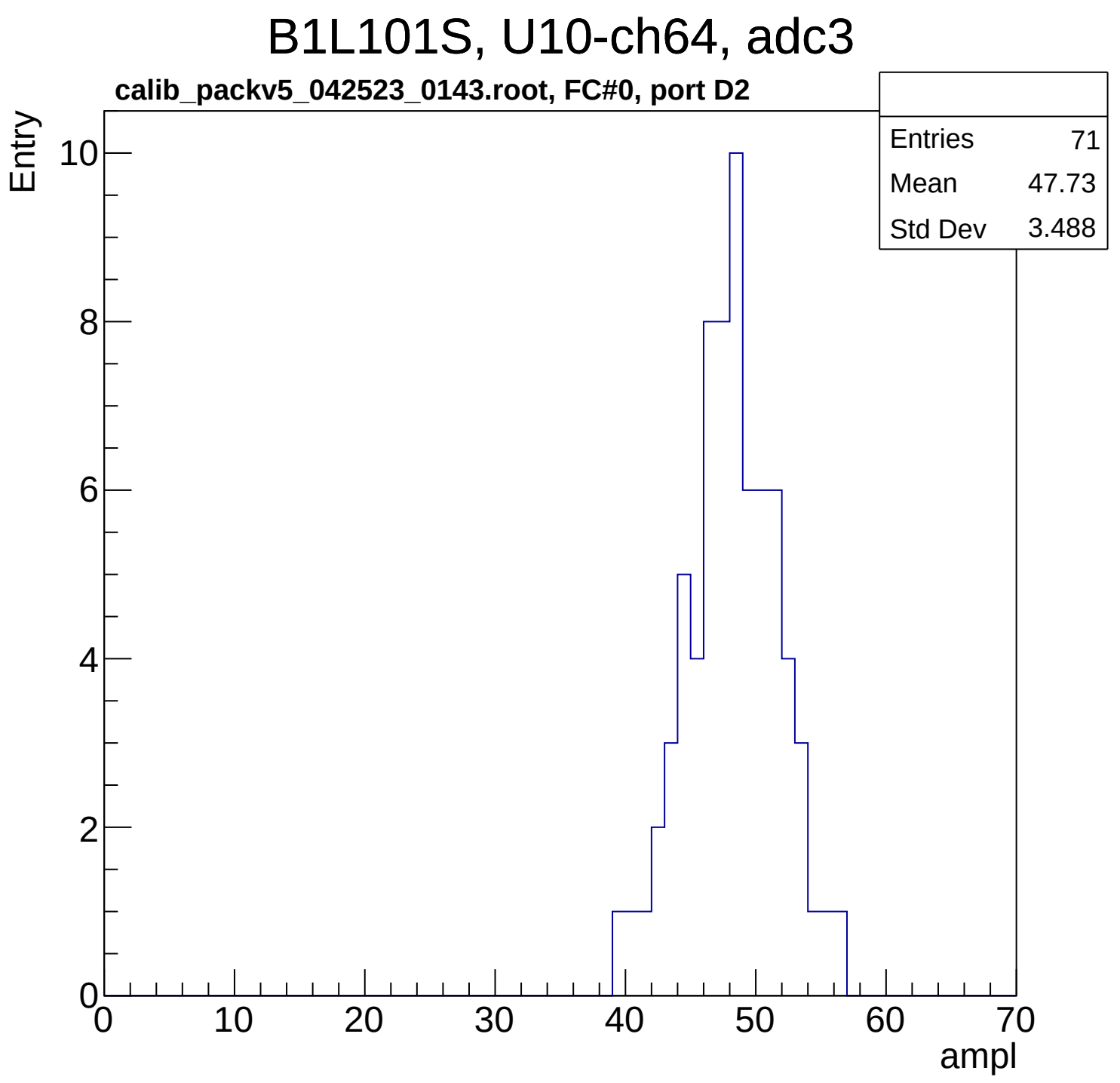
B1L101S, U10-ch64, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 47.73
Std Dev 3.488
Entry
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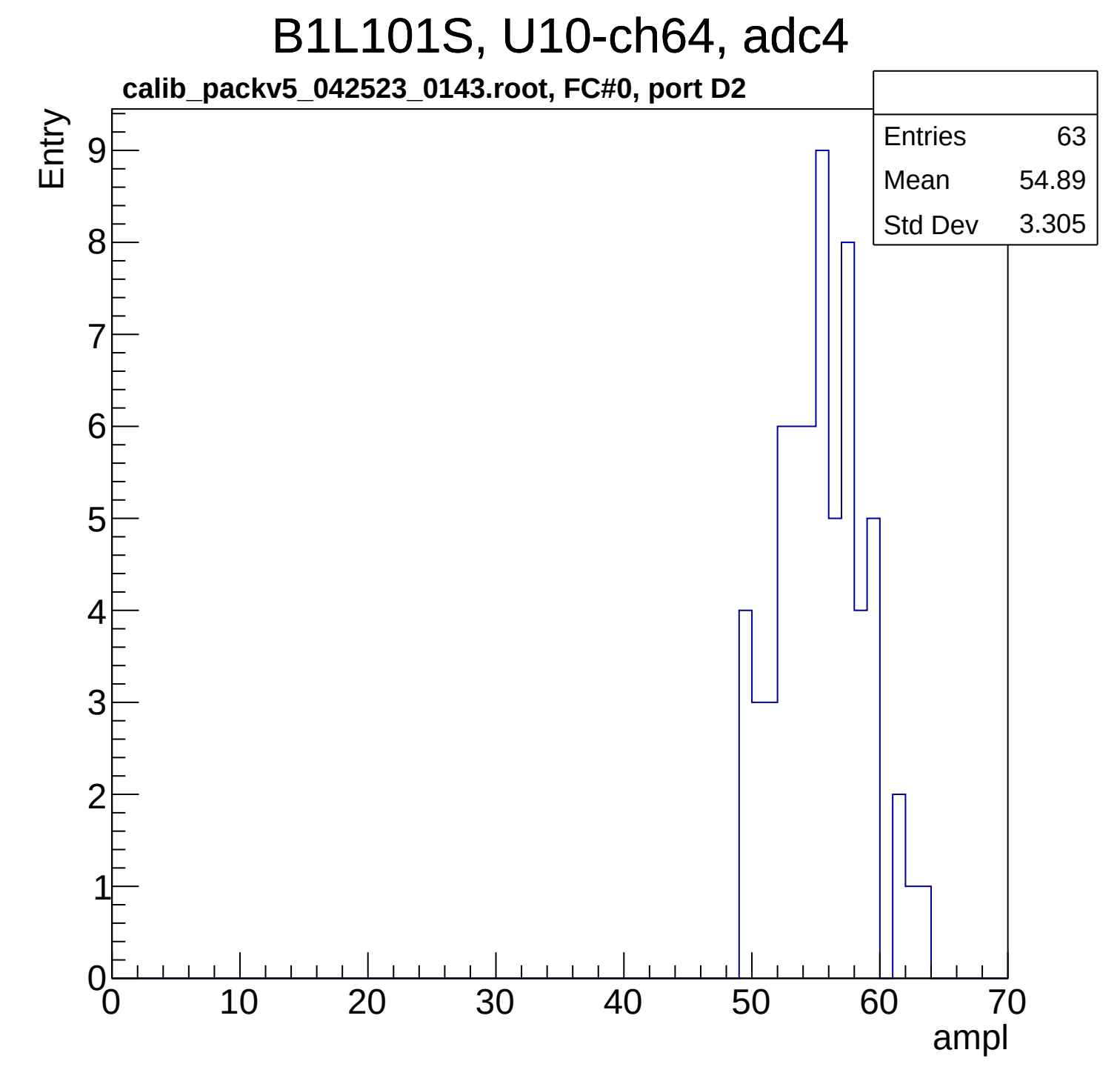
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch64, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 54.89
Std Dev 3.305
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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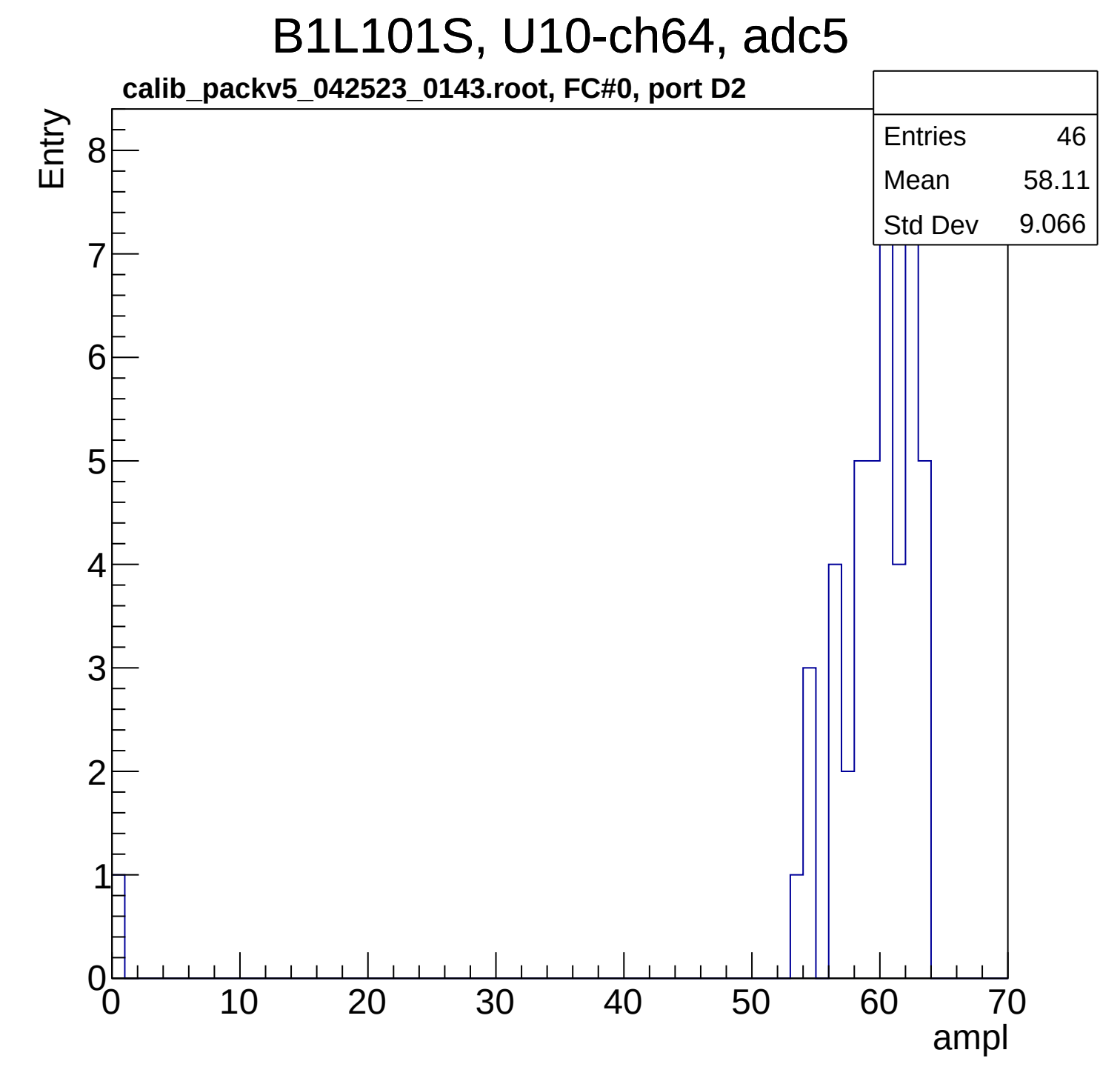
B1L101S, U10-ch64, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 58.11
Std Dev 9.066
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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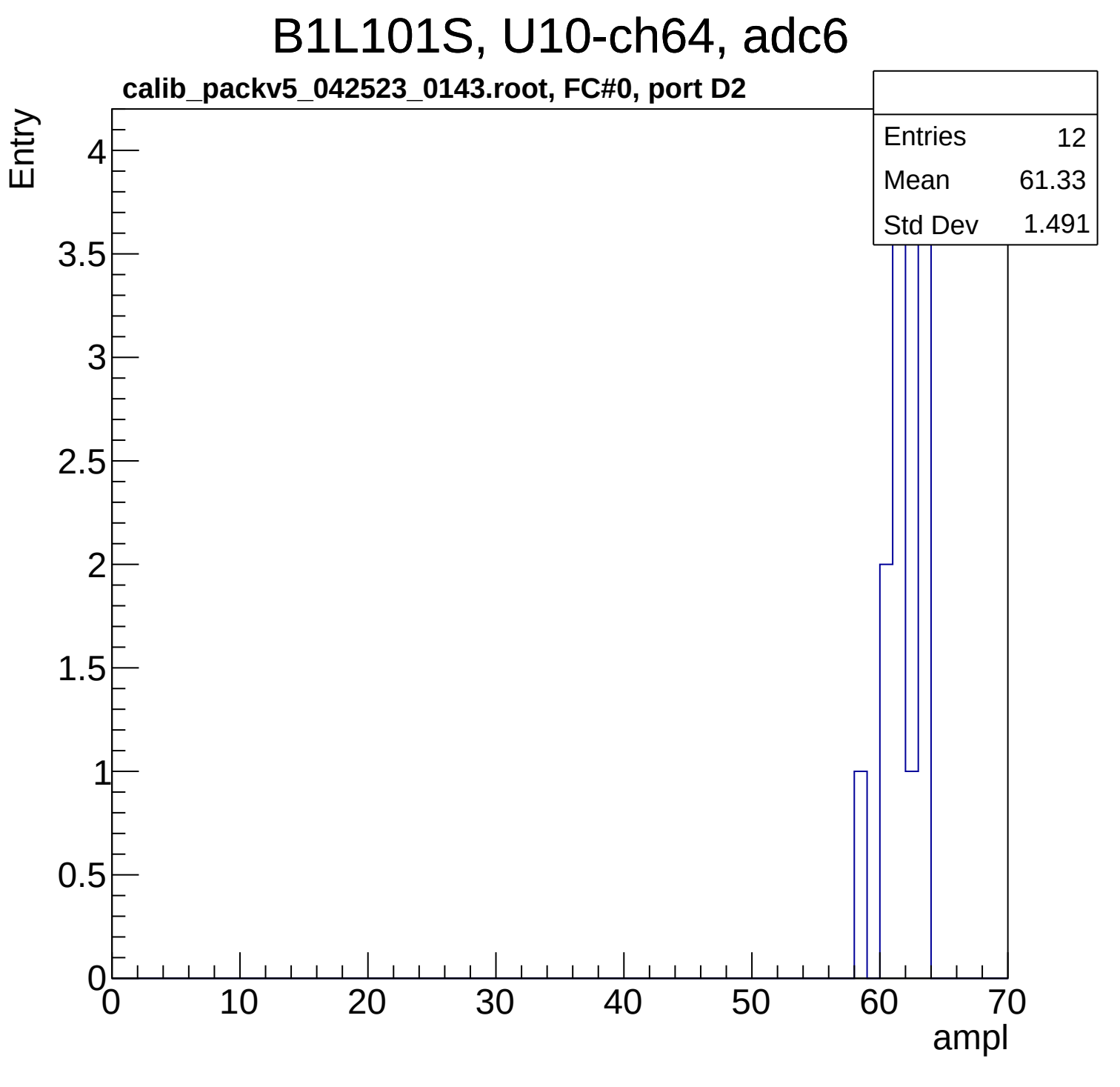
B1L101S, U10-ch64, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 12
Mean 61.33
Std Dev 1.491
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
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60
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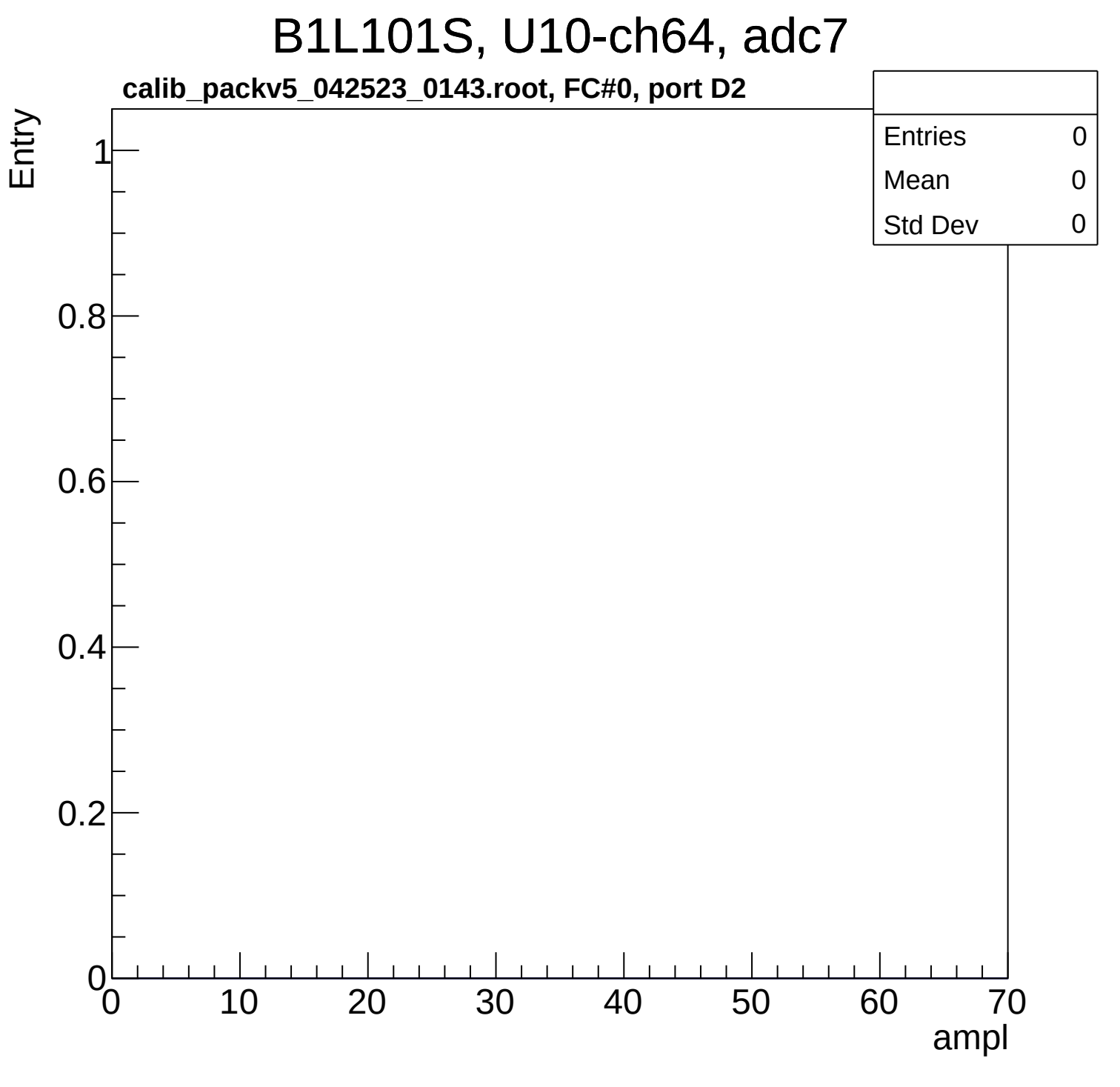
B1L101S, U10-ch64, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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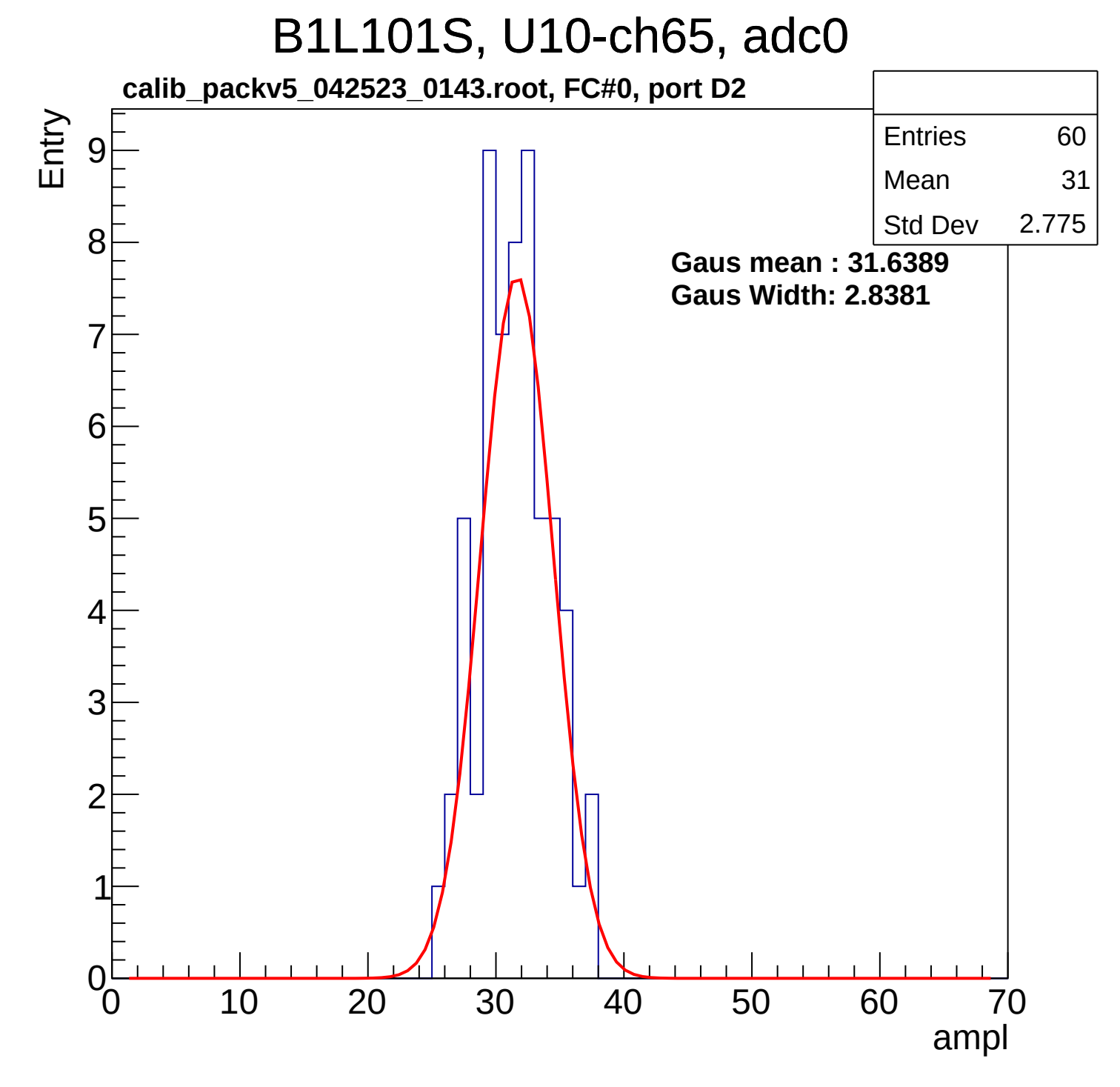
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch65, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 31
Std Dev 2.775
Gaus mean : 31.6389
Gaus Width: 2.8381
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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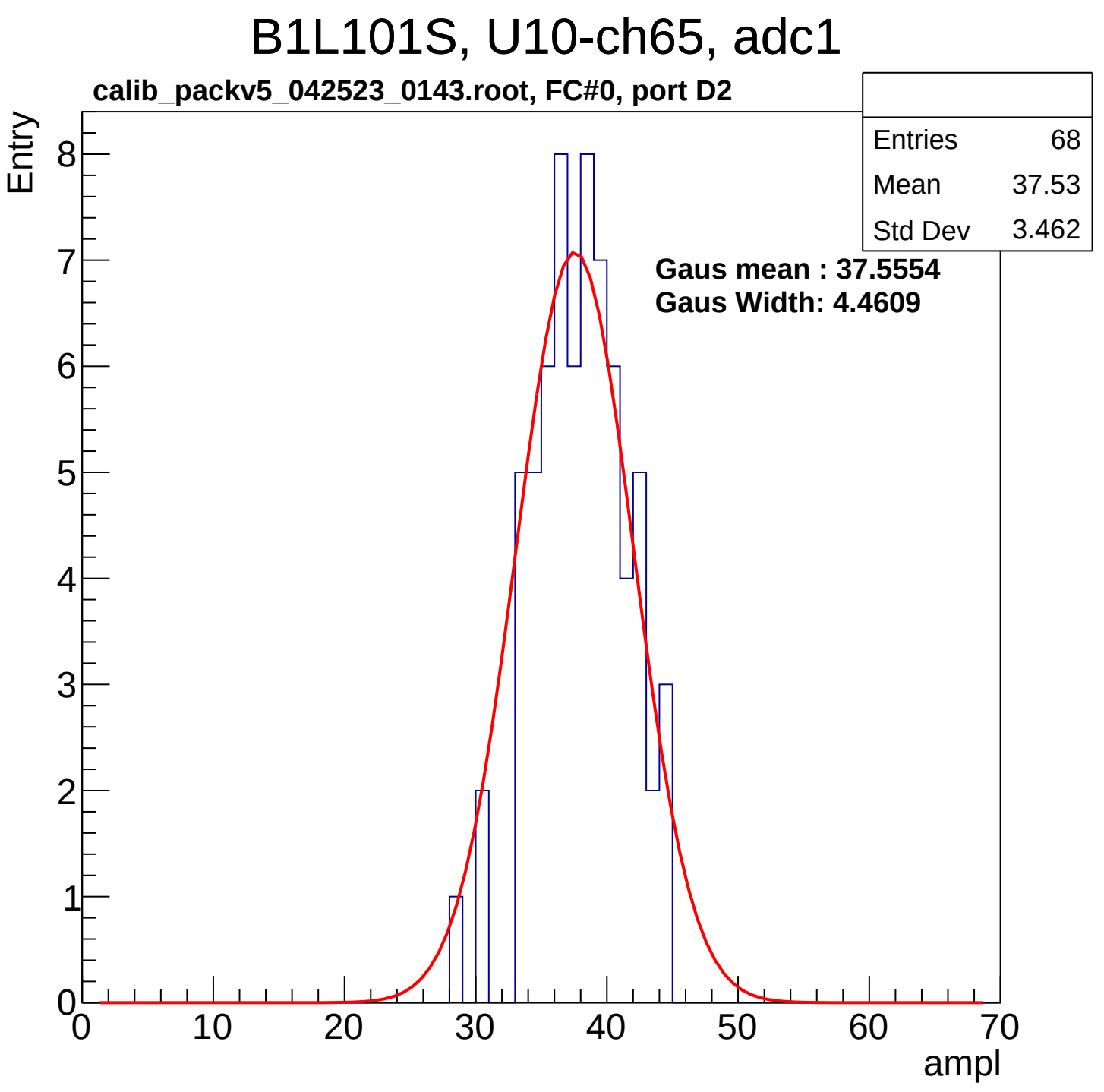
B1L101S, U10-ch65, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 37.53
Std Dev 3.462
Gaus mean : 37.5554
Gaus Width: 4.4609
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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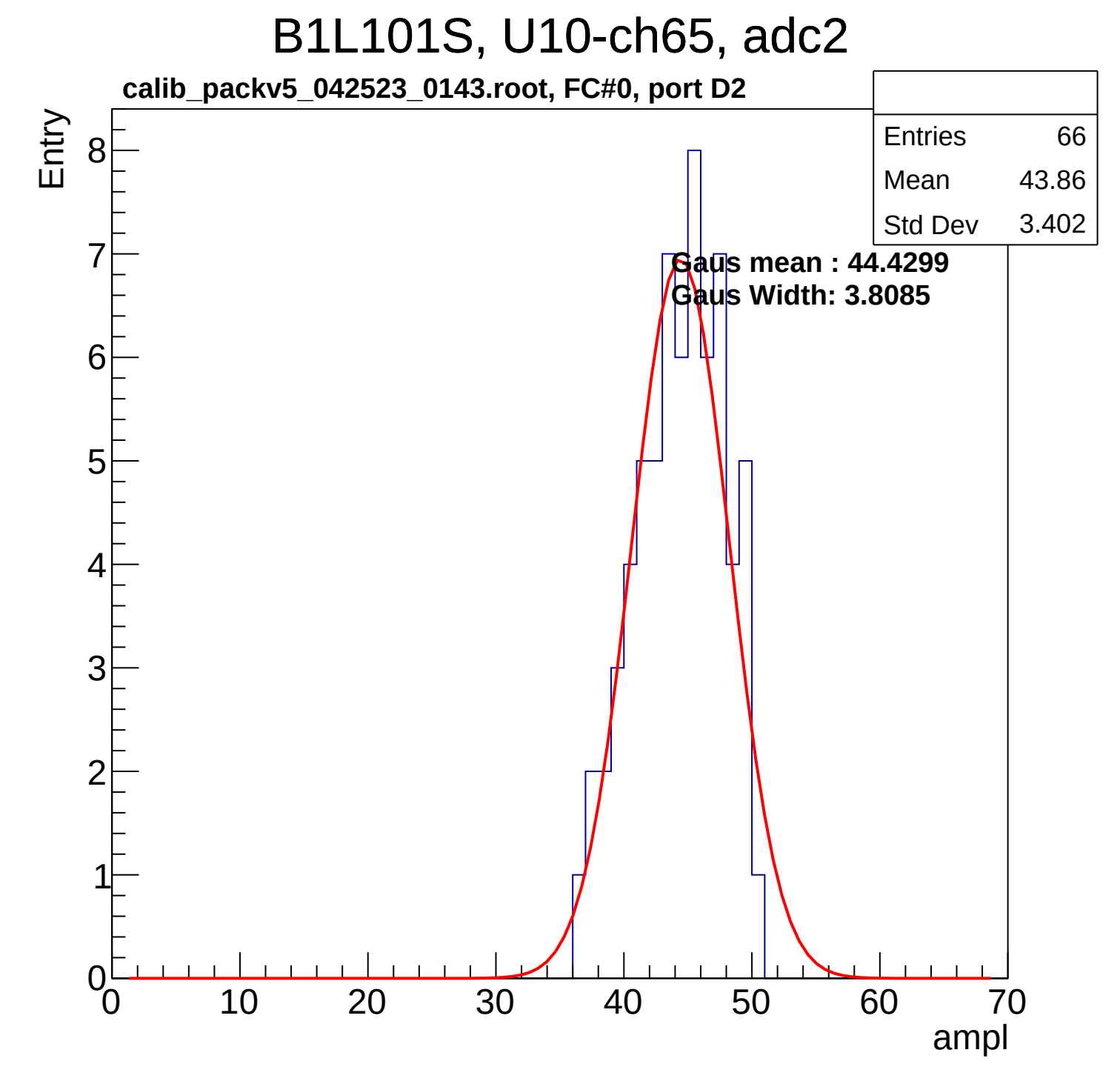
B1L101S, U10-ch65, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 43.86
Std Dev 3.402
Gaus mean : 44.4299
Gaus Width: 3.8085
Entry
ampl
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2
3
4
5
6
7
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0
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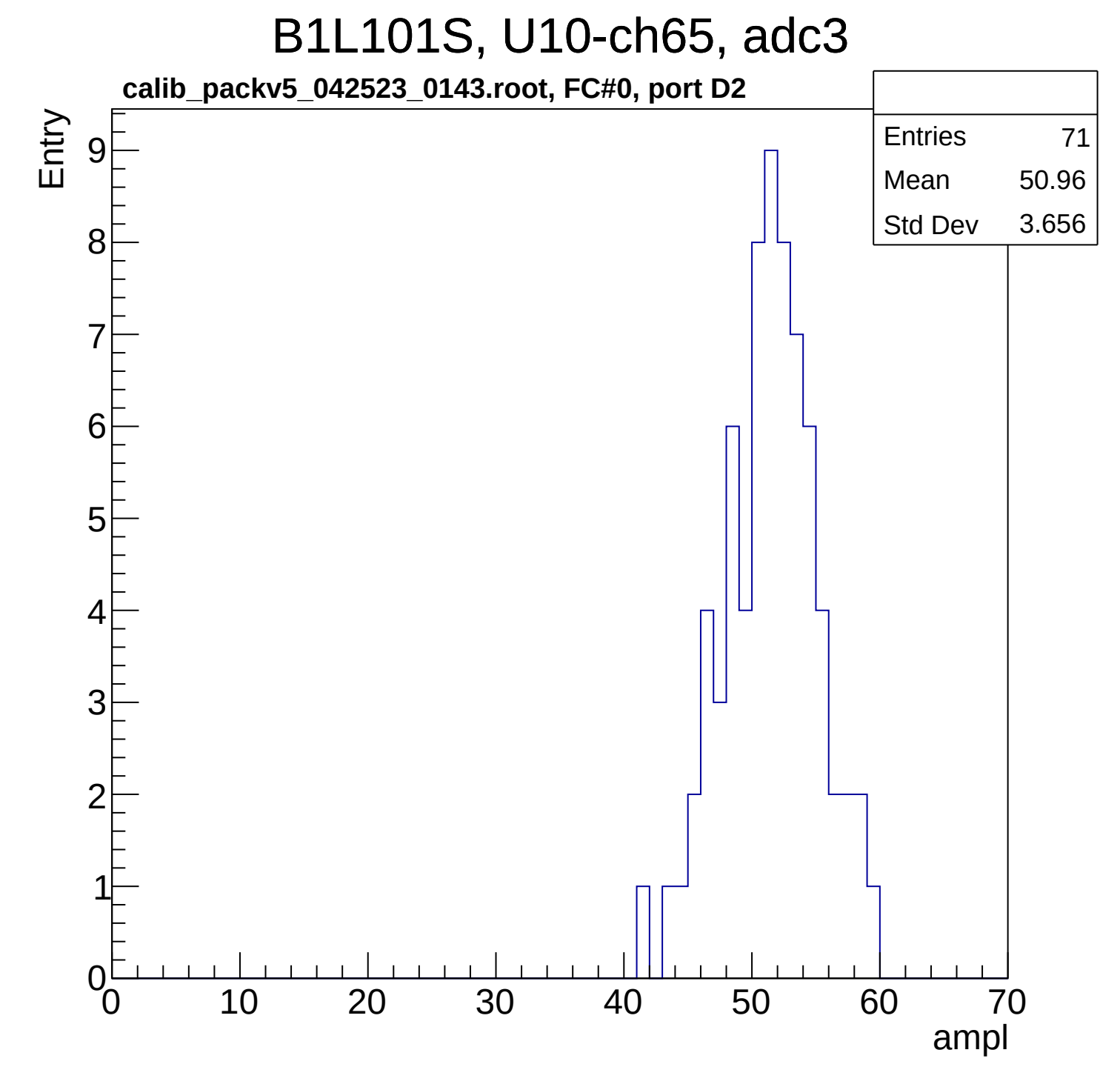
B1L101S, U10-ch65, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 50.96
Std Dev 3.656
Entry
ampl
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3
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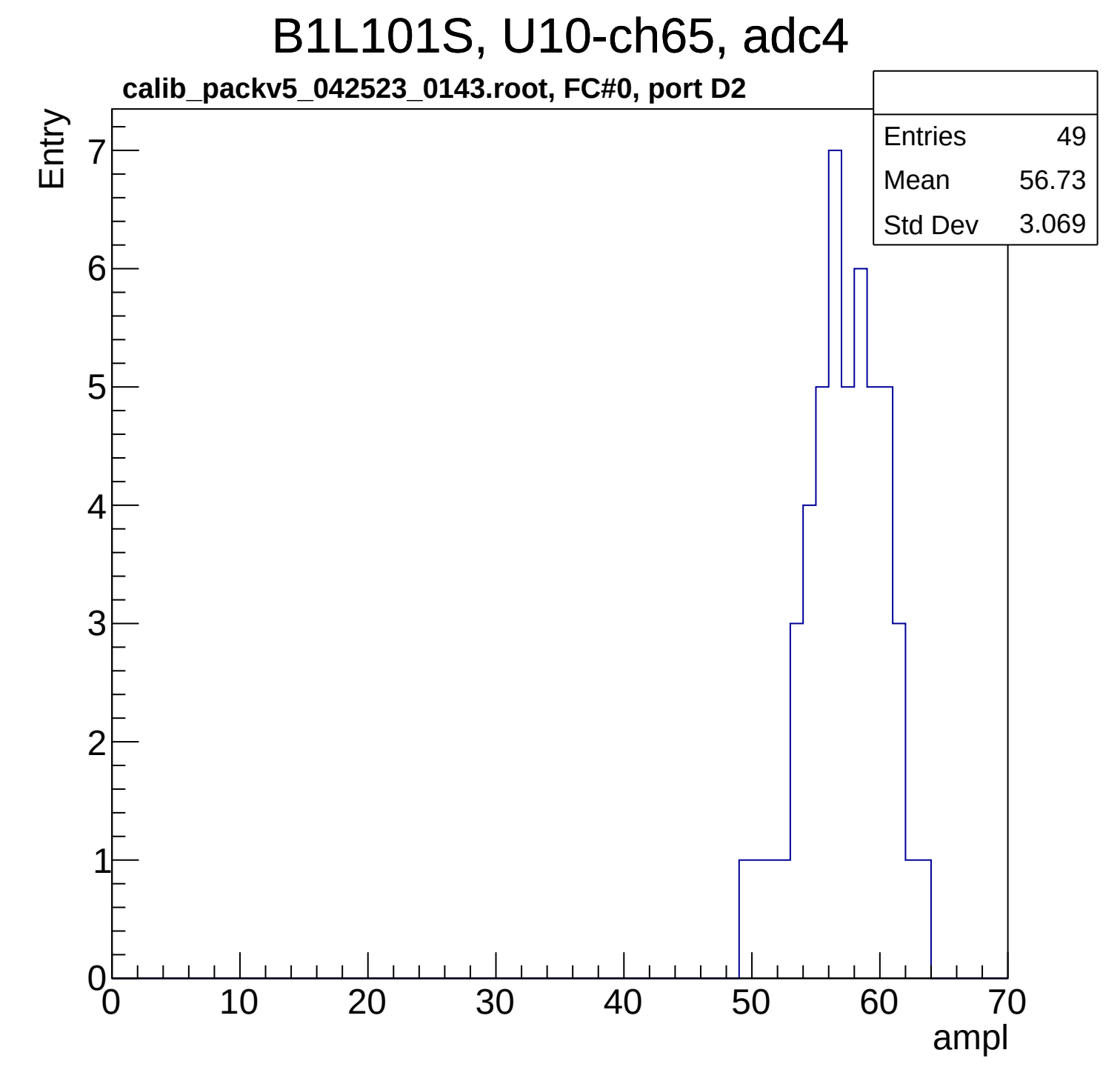
B1L101S, U10-ch65, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 56.73
Std Dev 3.069
Entry
ampl
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1
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4
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0
10
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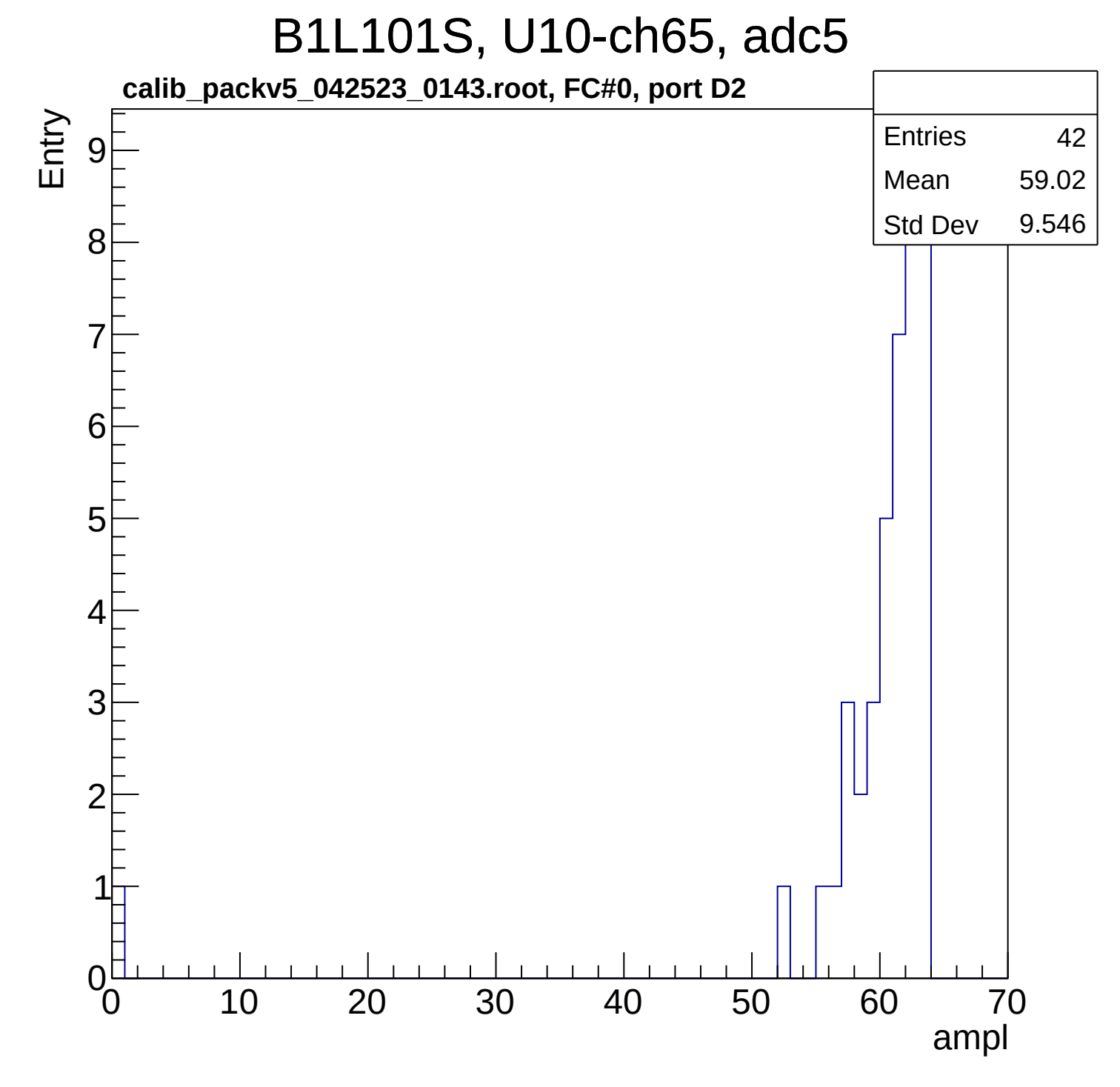
40
50
60
70


B1L101S, U10-ch65, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 59.02
Std Dev 9.546
Entry
ampl
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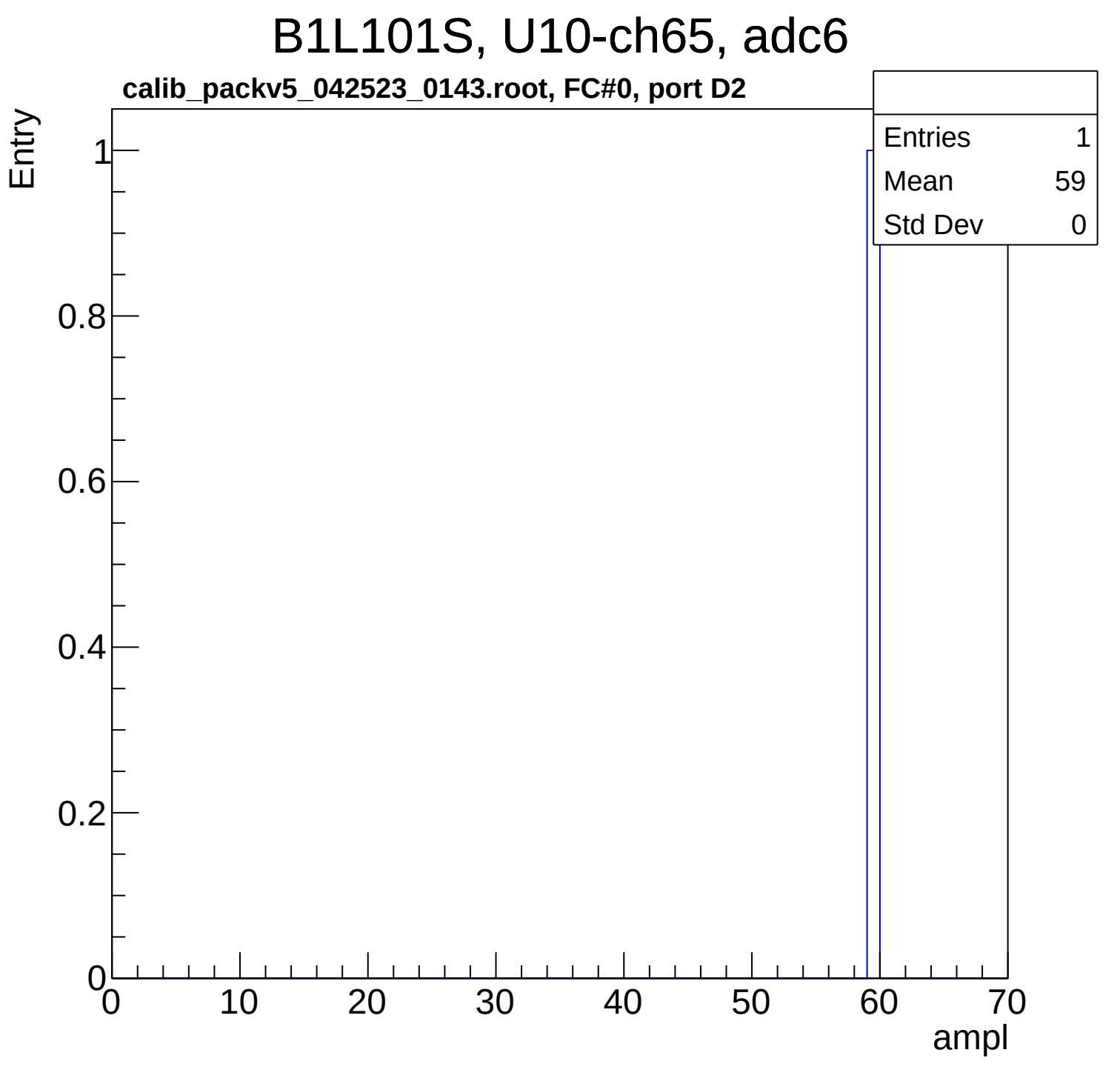
B1L101S, U10-ch65, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 59
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
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10
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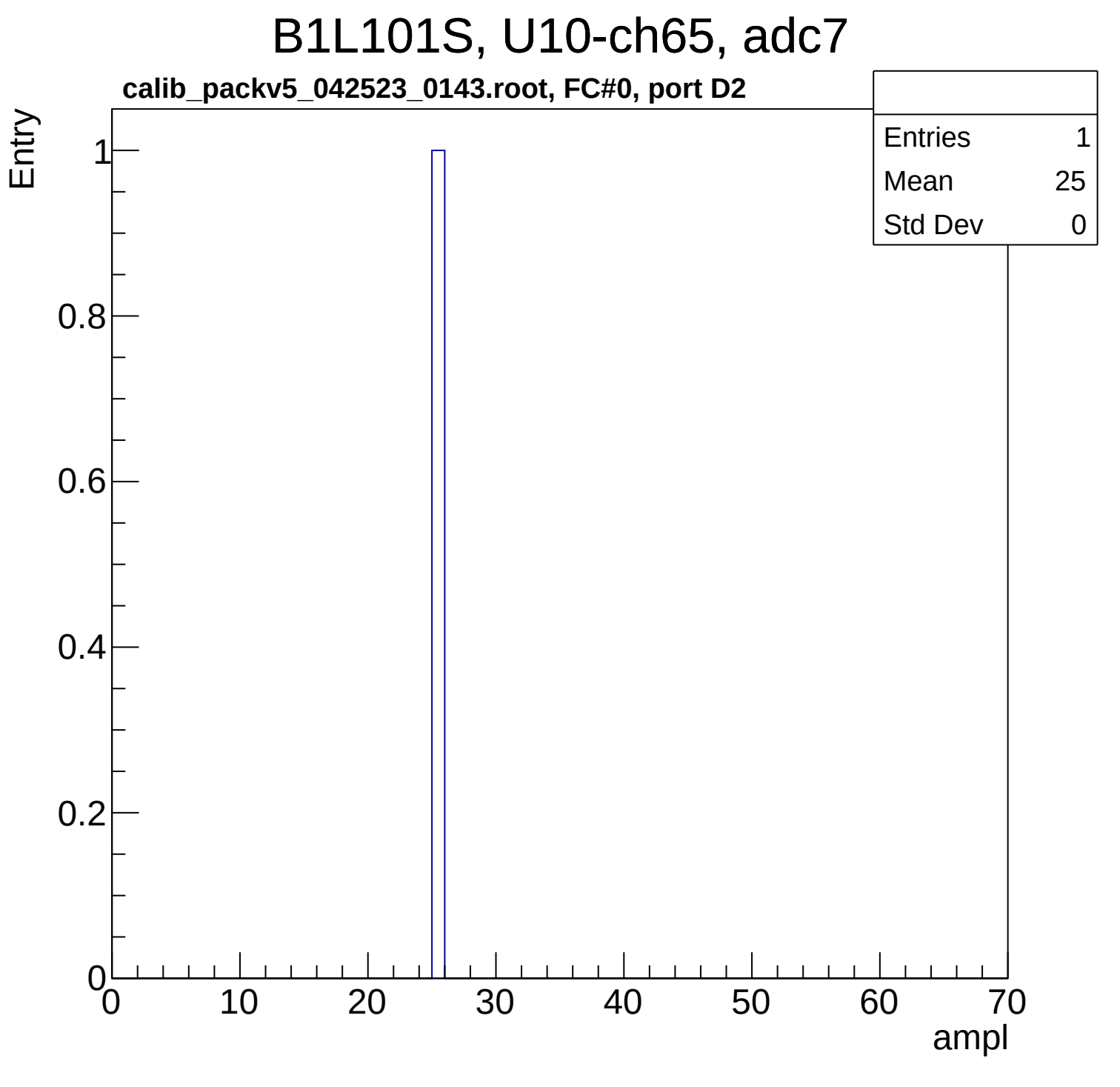
50
60
70
ampl


B1L101S, U10-ch65, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 25
Std Dev 0
Entry
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0.8
0.6
0.4
0.2
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10
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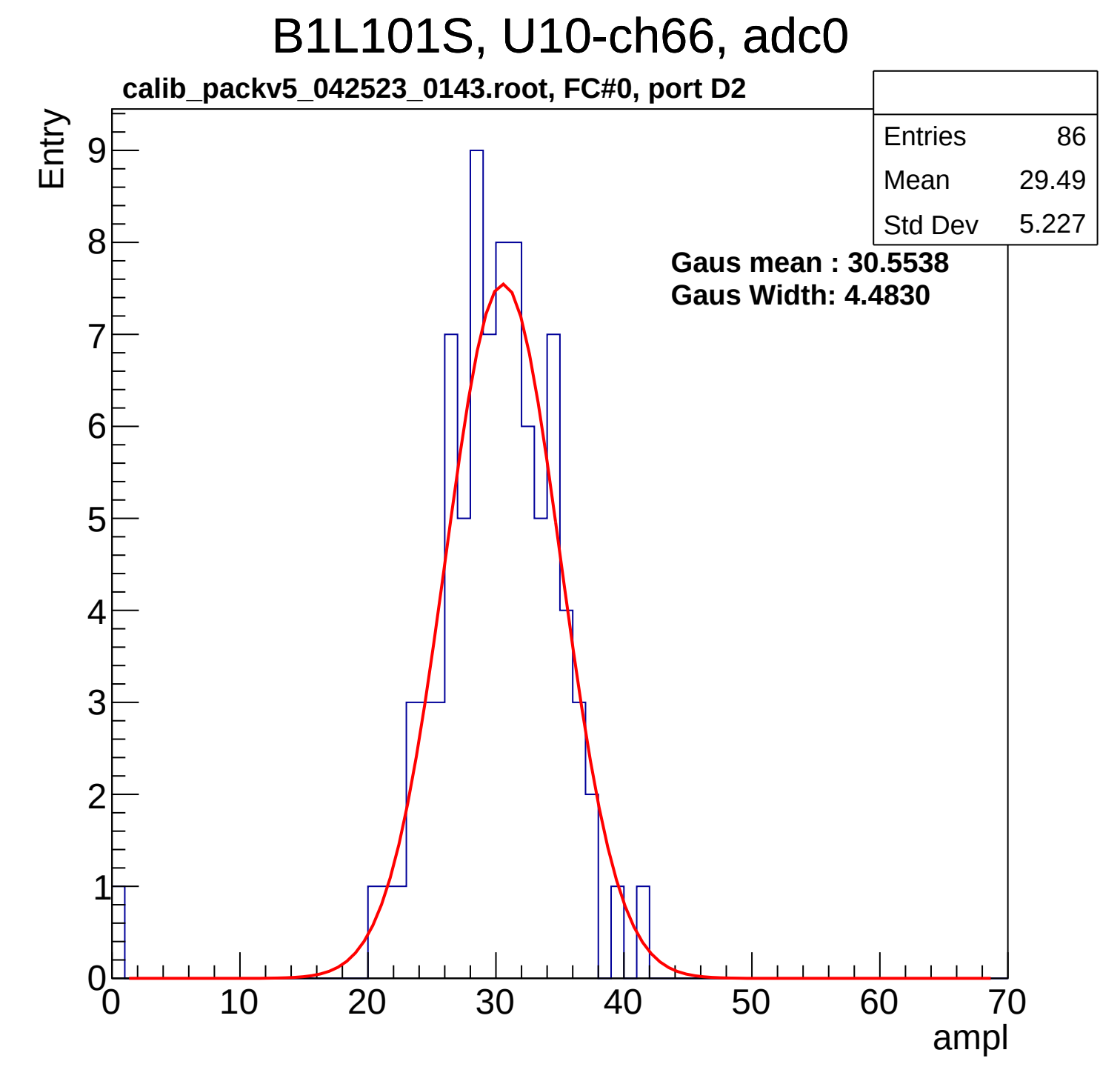
50
60
70
ampl


B1L101S, U10-ch66, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 86
Mean 29.49
Std Dev 5.227
Gaus mean : 30.5538
Gaus Width: 4.4830
Entry
ampl
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1
2
3
4
5
6
7
8
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0
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60
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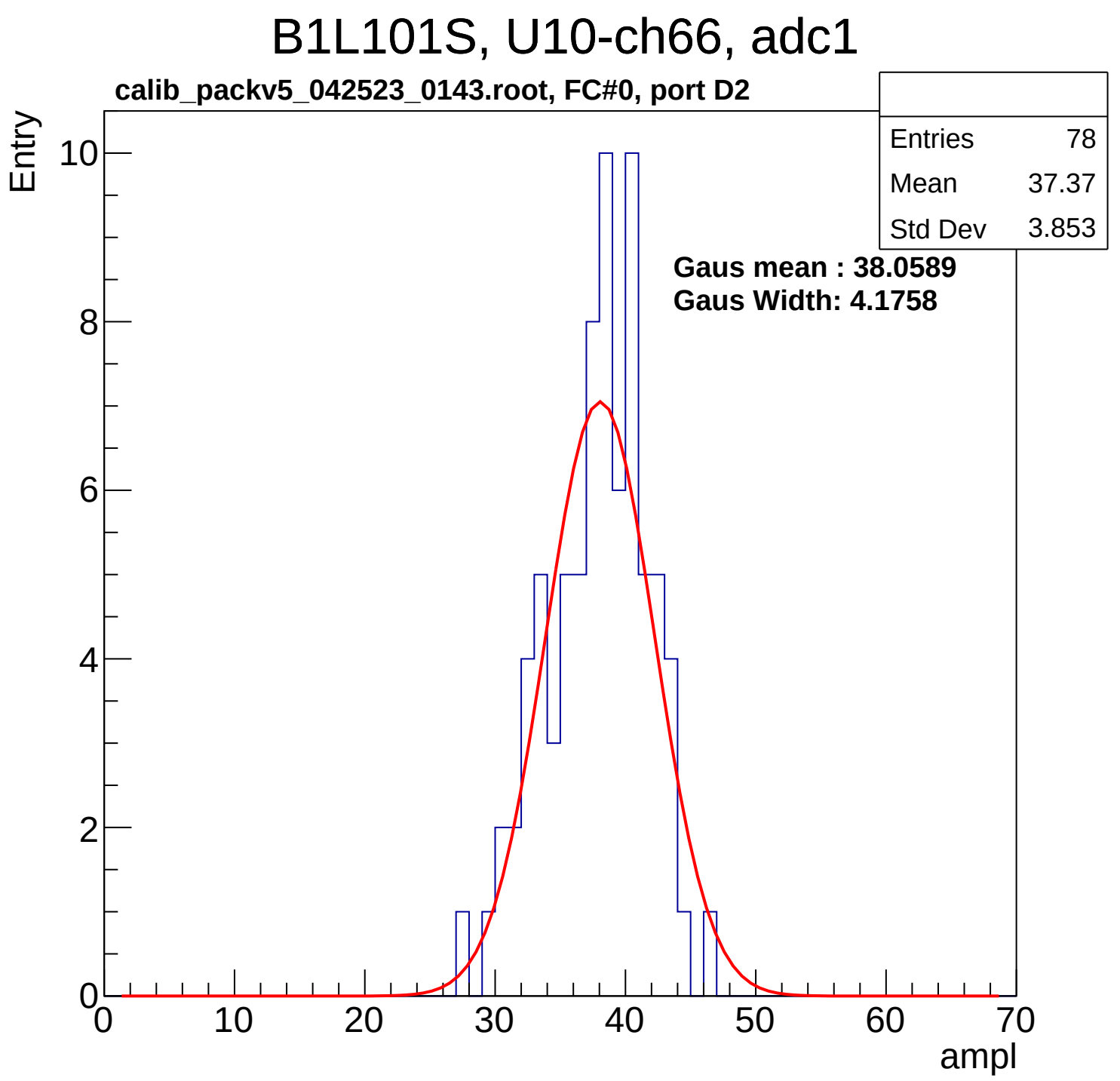
B1L101S, U10-ch66, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 37.37
Std Dev 3.853
Gaus mean : 38.0589
Gaus Width: 4.1758
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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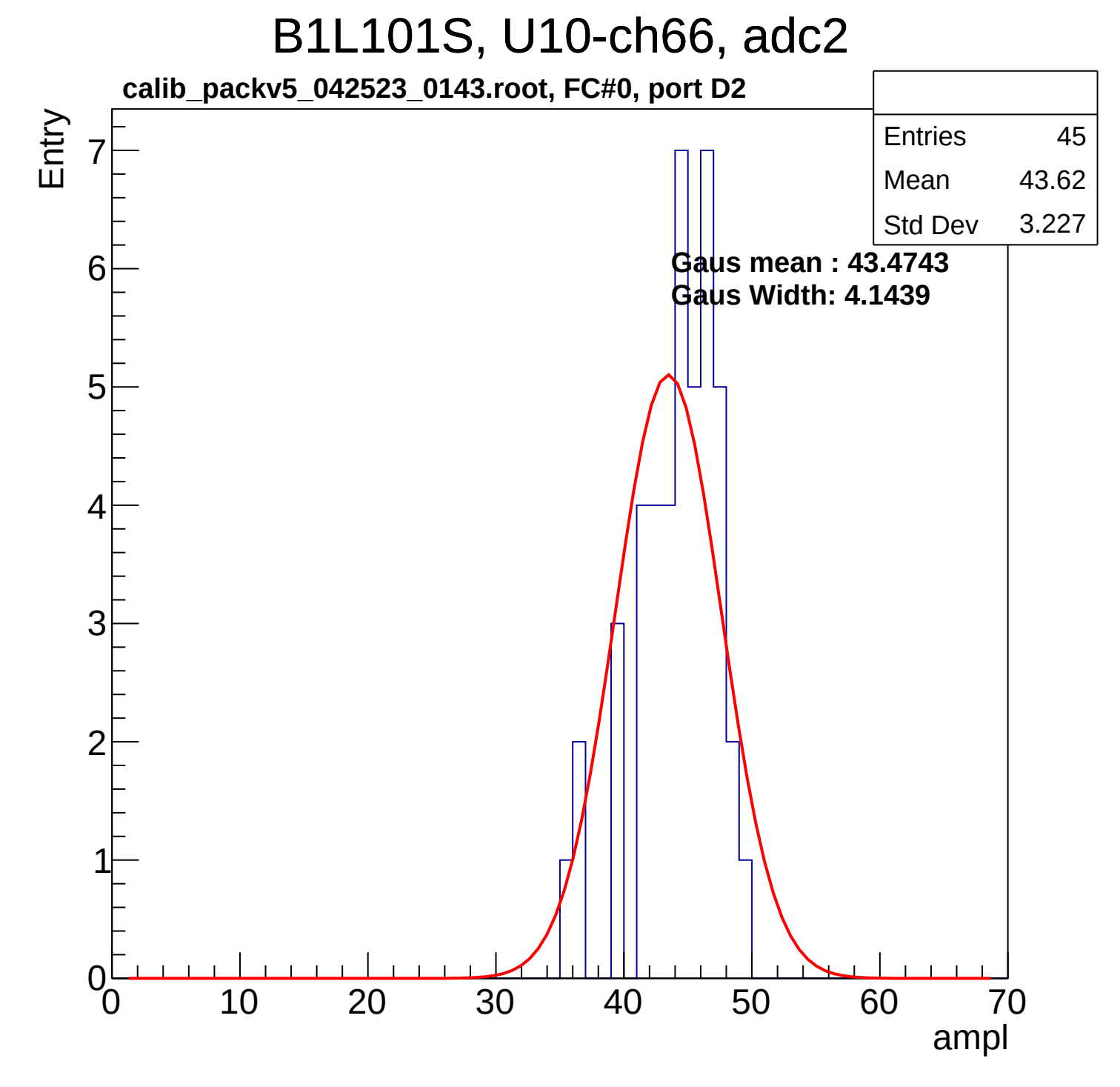
B1L101S, U10-ch66, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 43.62
Std Dev 3.227
Gaus mean : 43.4743
Gaus Width: 4.1439
Entry
ampl
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1
2
3
4
5
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0
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60
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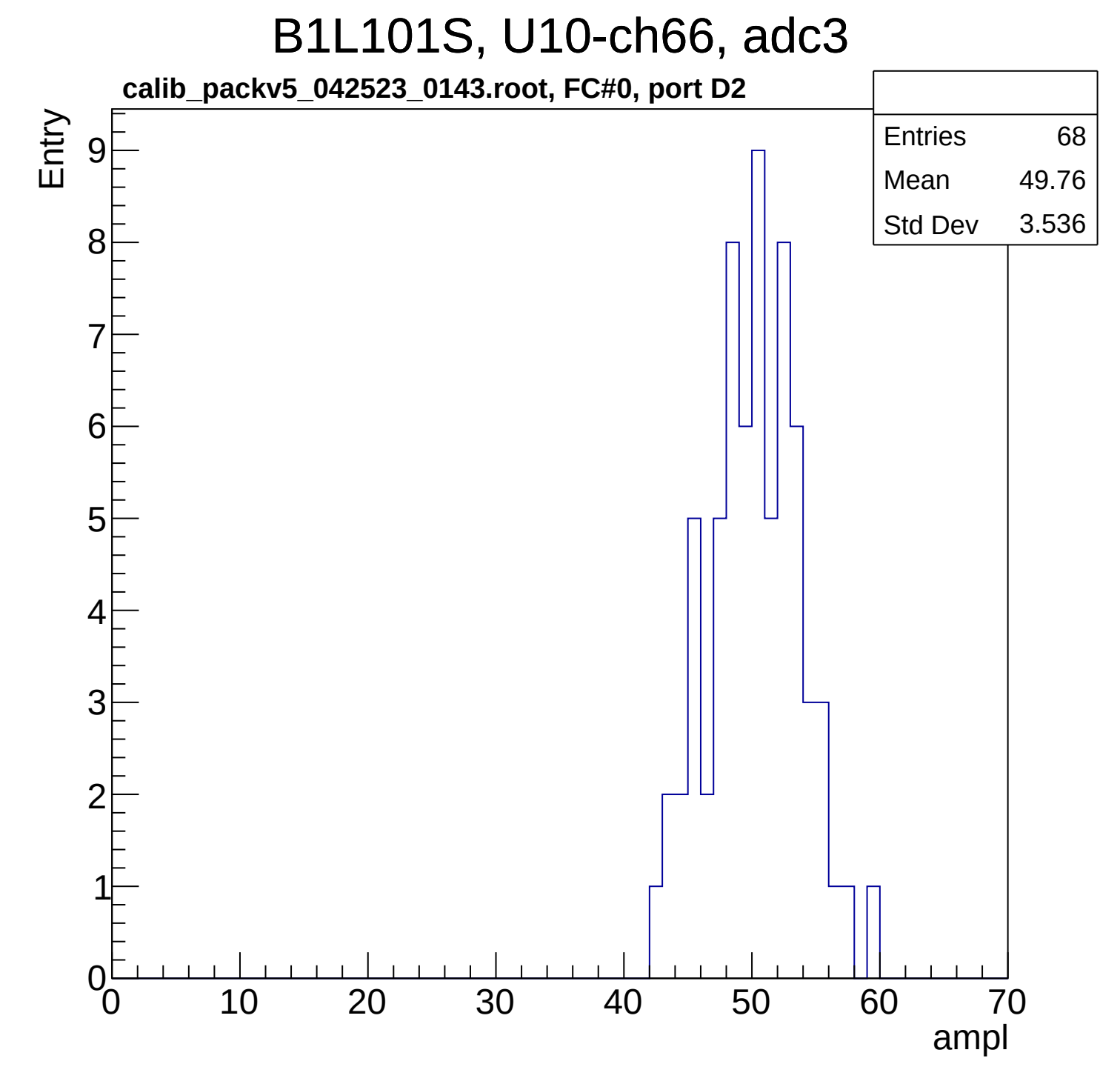
B1L101S, U10-ch66, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 49.76
Std Dev 3.536
Entry
ampl
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1
2
3
4
5
6
7
8
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0
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40
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60
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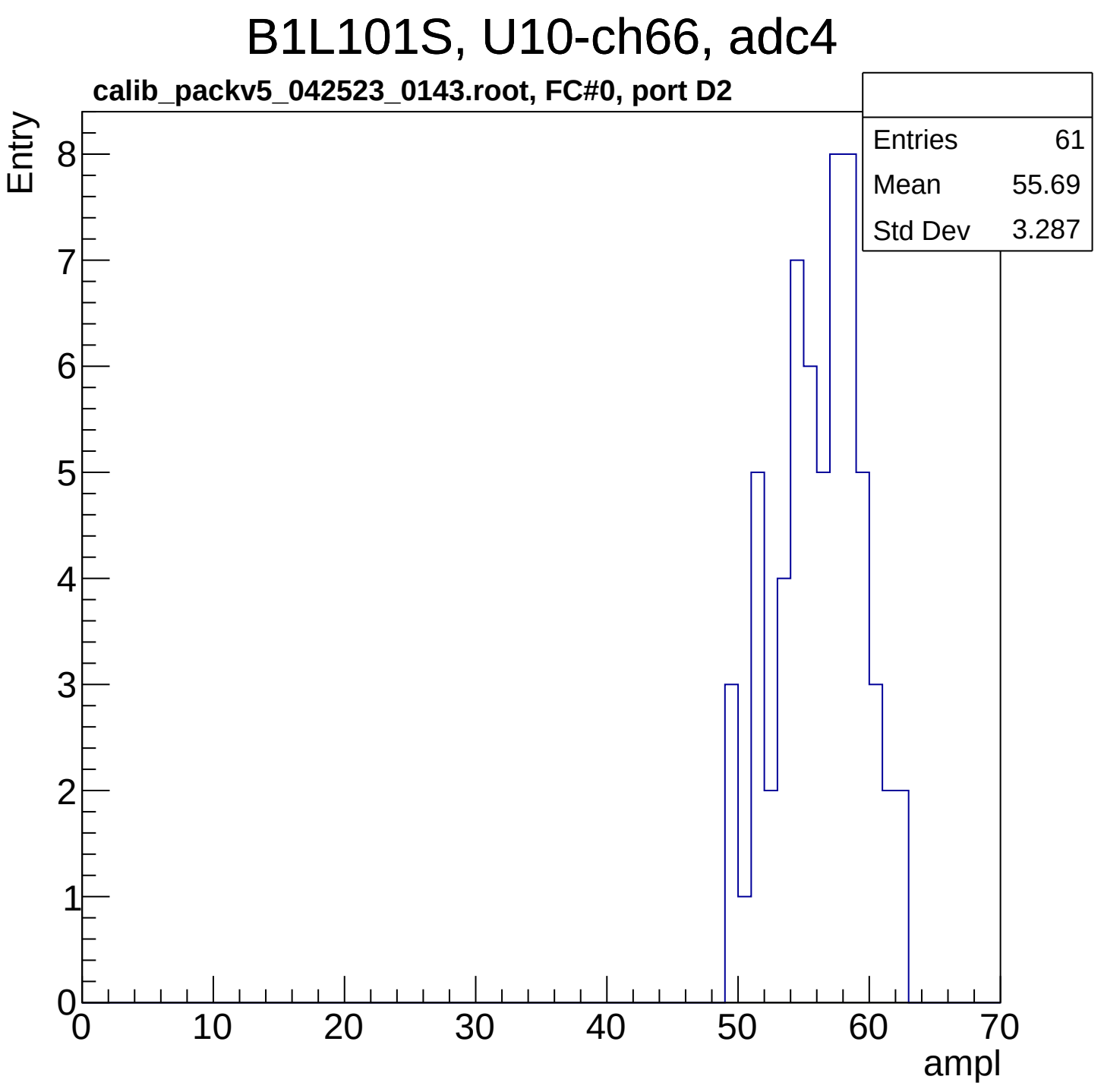
B1L101S, U10-ch66, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 55.69
Std Dev 3.287
Entry
ampl
0
1
2
3
4
5
6
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0
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60
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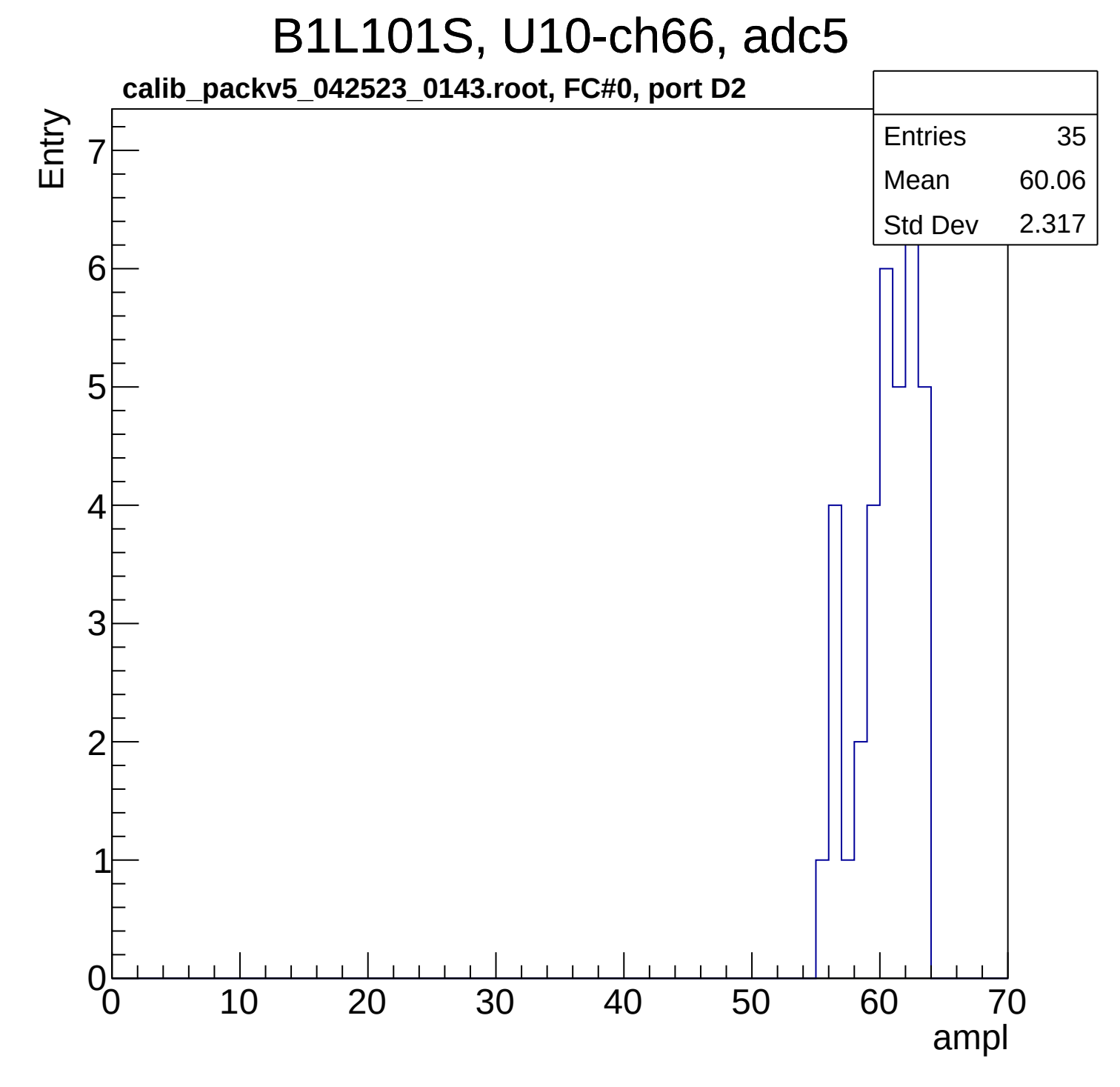
B1L101S, U10-ch66, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 35
Mean 60.06
Std Dev 2.317
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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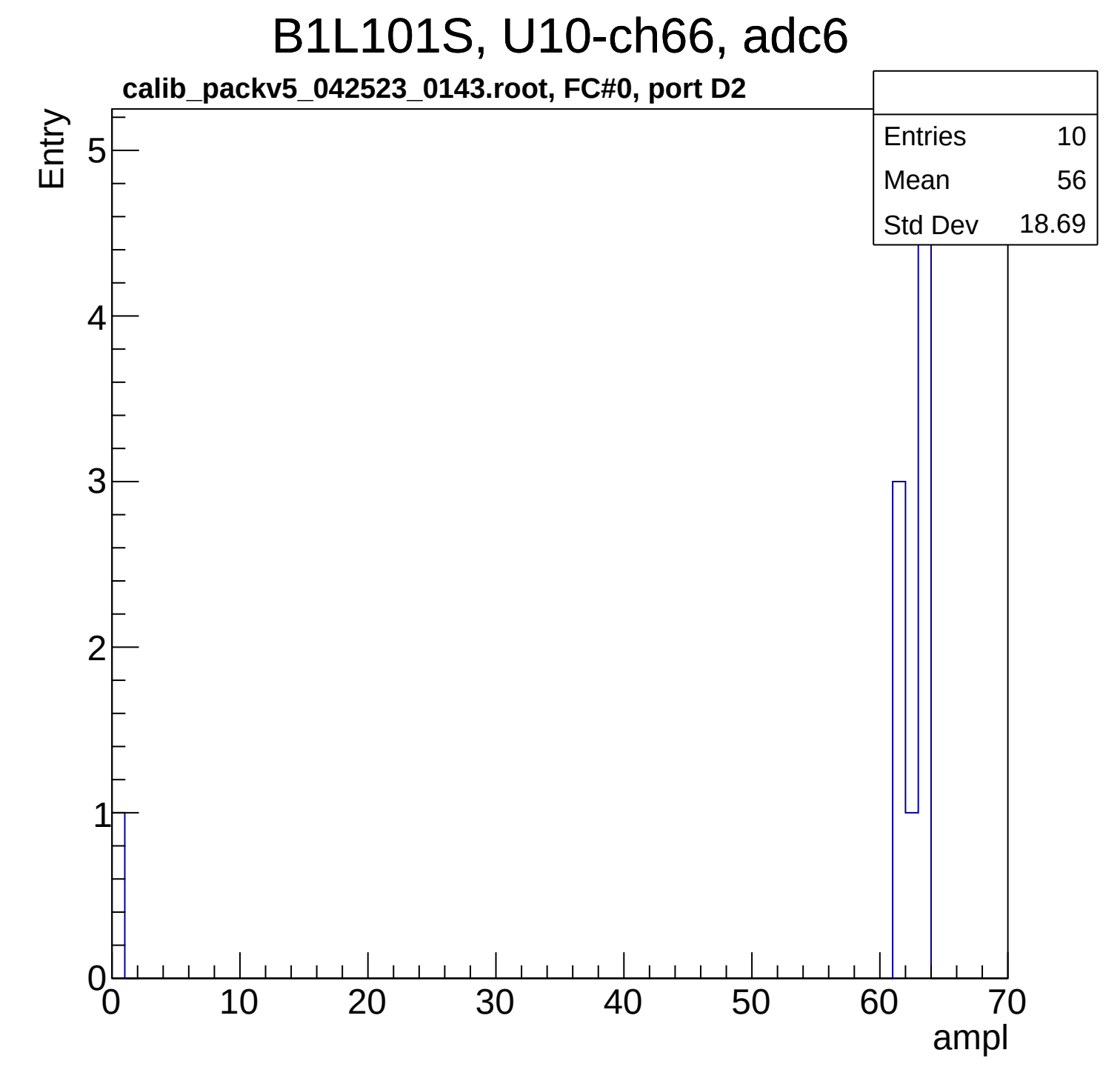
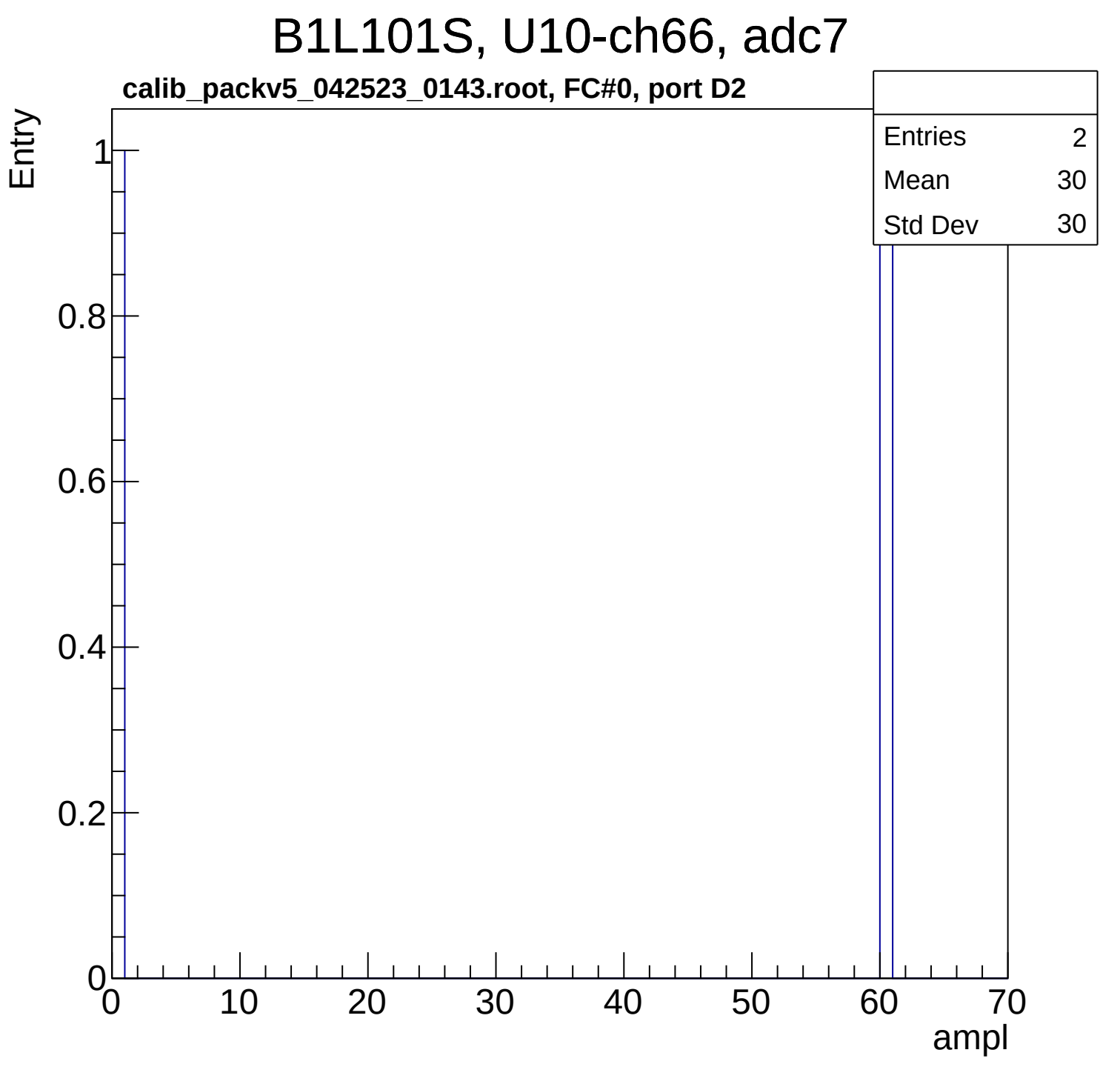

B1L101S, U10-ch66, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 56
Std Dev 18.69
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch66, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 30
Std Dev 30
Entry
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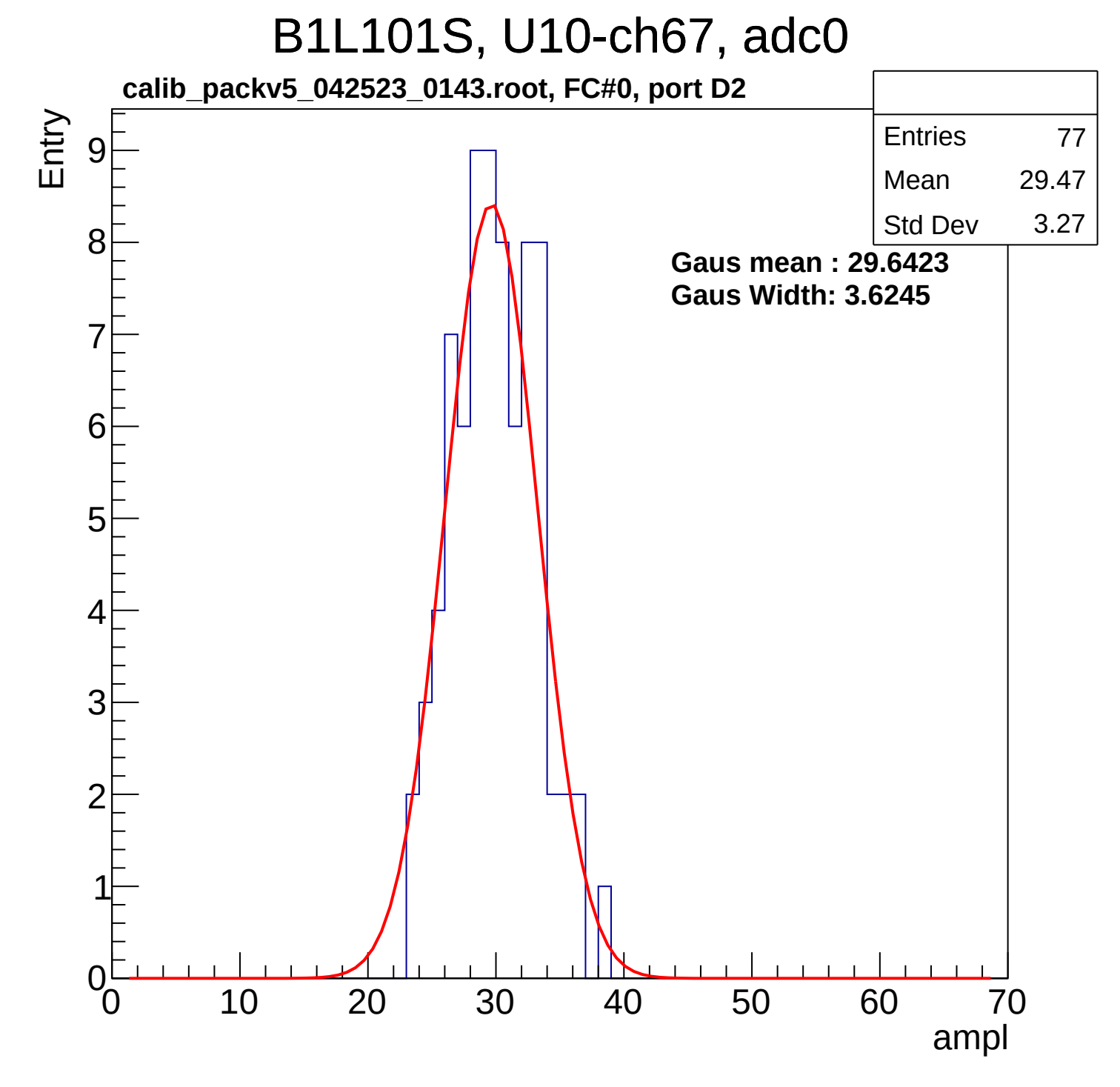
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch67, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 29.47
Std Dev 3.27
Gaus mean : 29.6423
Gaus Width: 3.6245
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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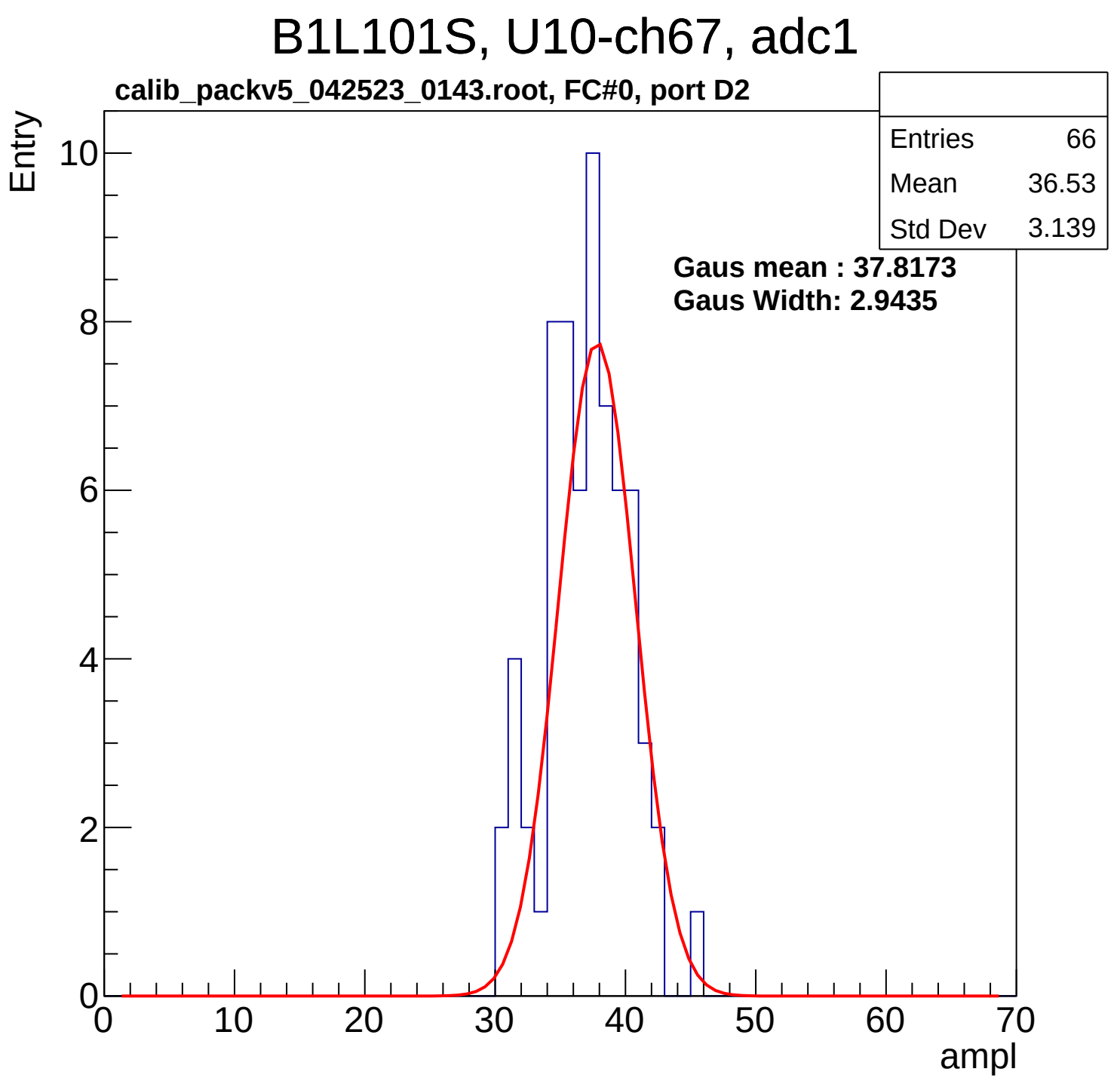
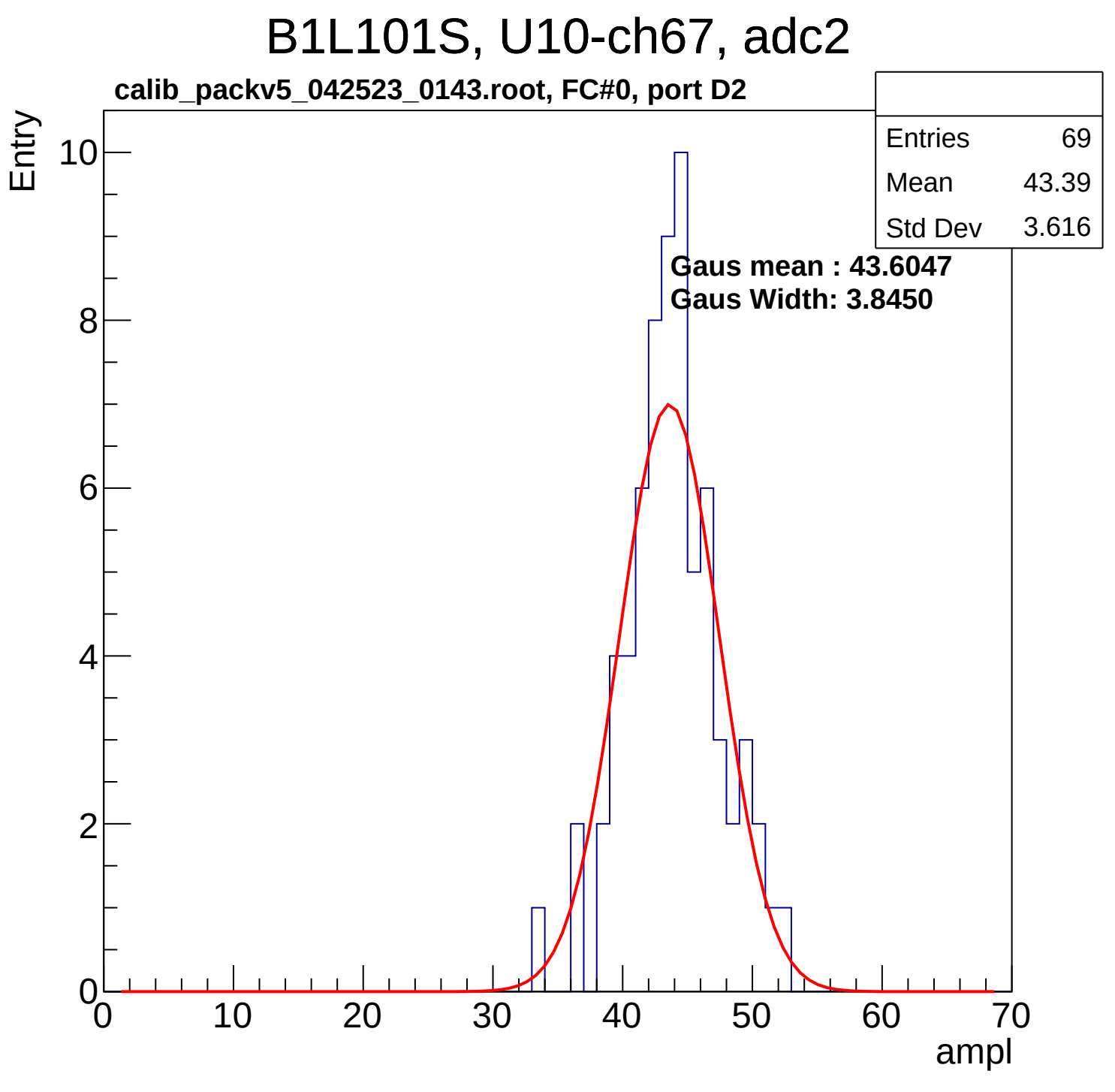
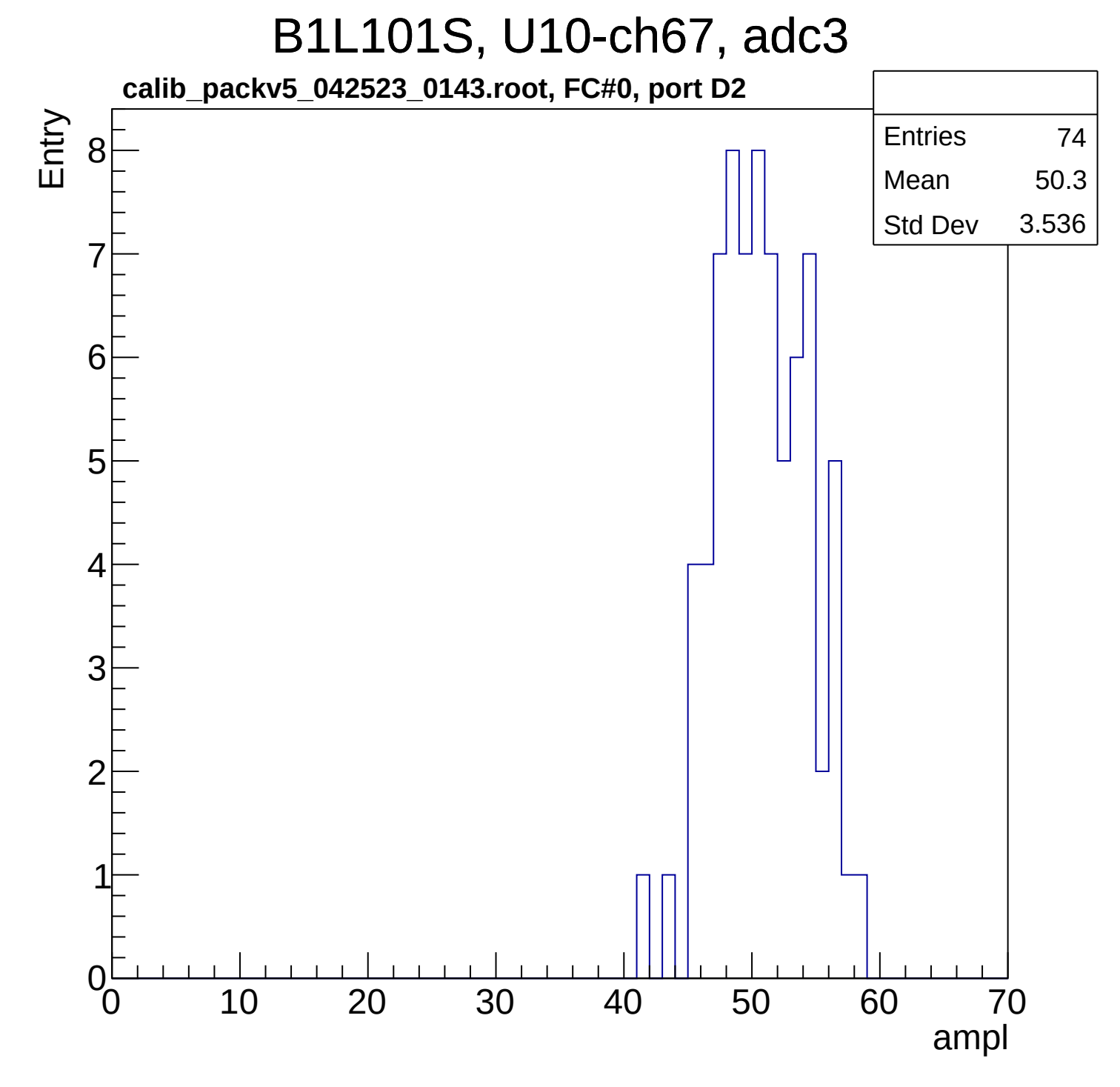

B1L101S, U10-ch67, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 36.53
Std Dev 3.139
Gaus mean : 37.8173
Gaus Width: 2.9435
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch67, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 43.39
Std Dev 3.616
Gaus mean : 43.6047
Gaus Width: 3.8450
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch67, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 50.3
Std Dev 3.536
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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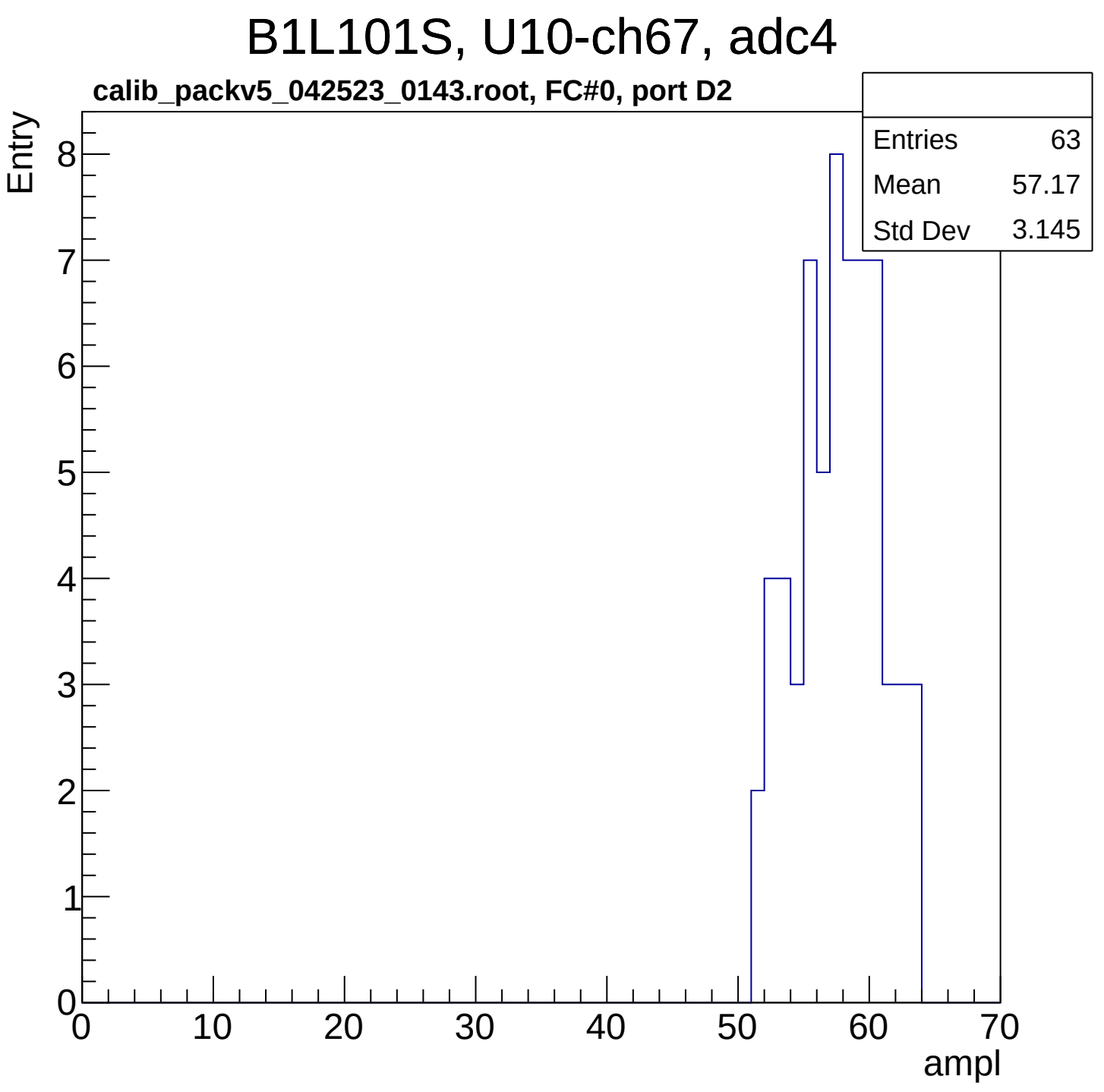
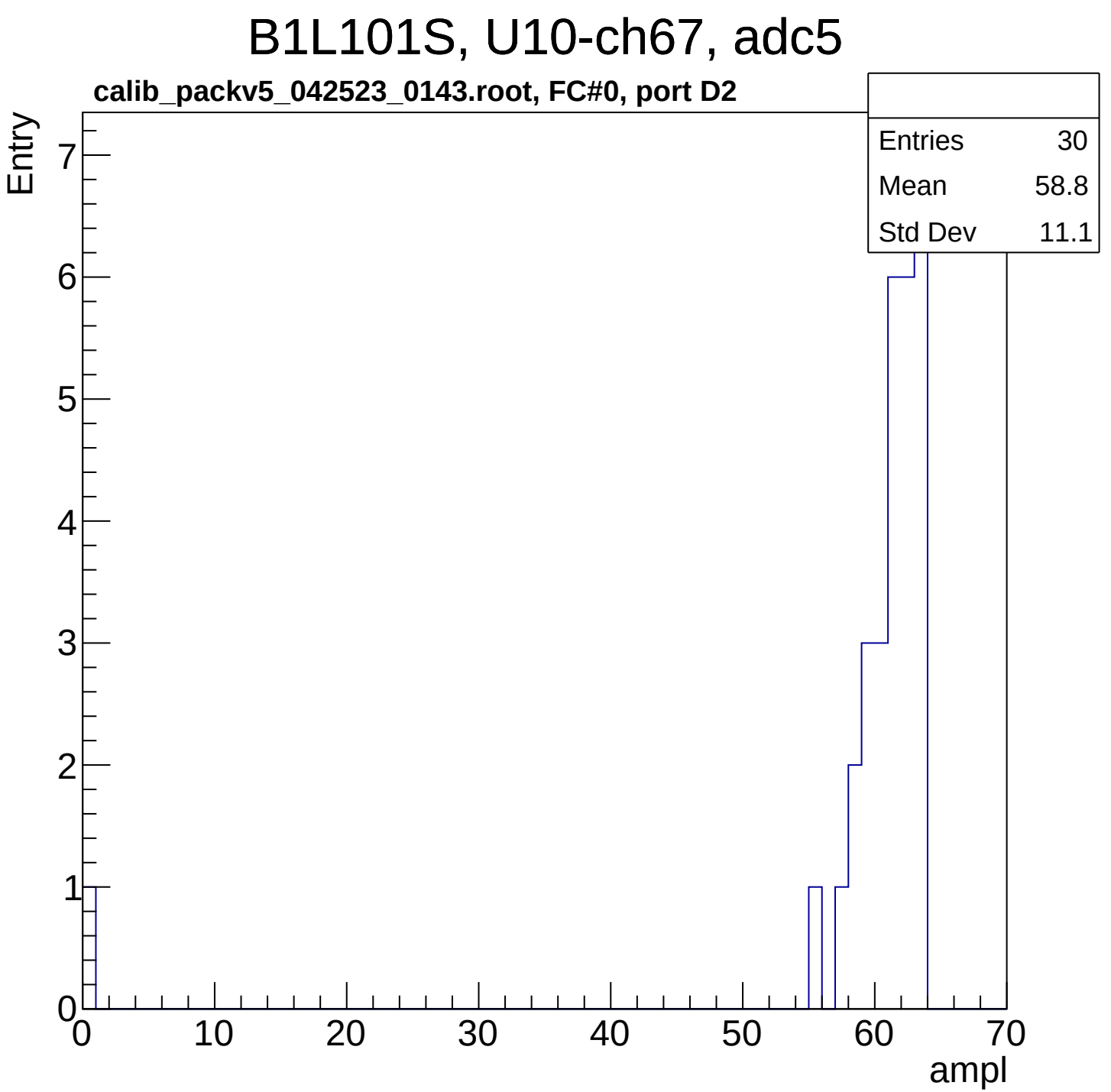

B1L101S, U10-ch67, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 57.17
Std Dev 3.145
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch67, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 30
Mean 58.8
Std Dev 11.1
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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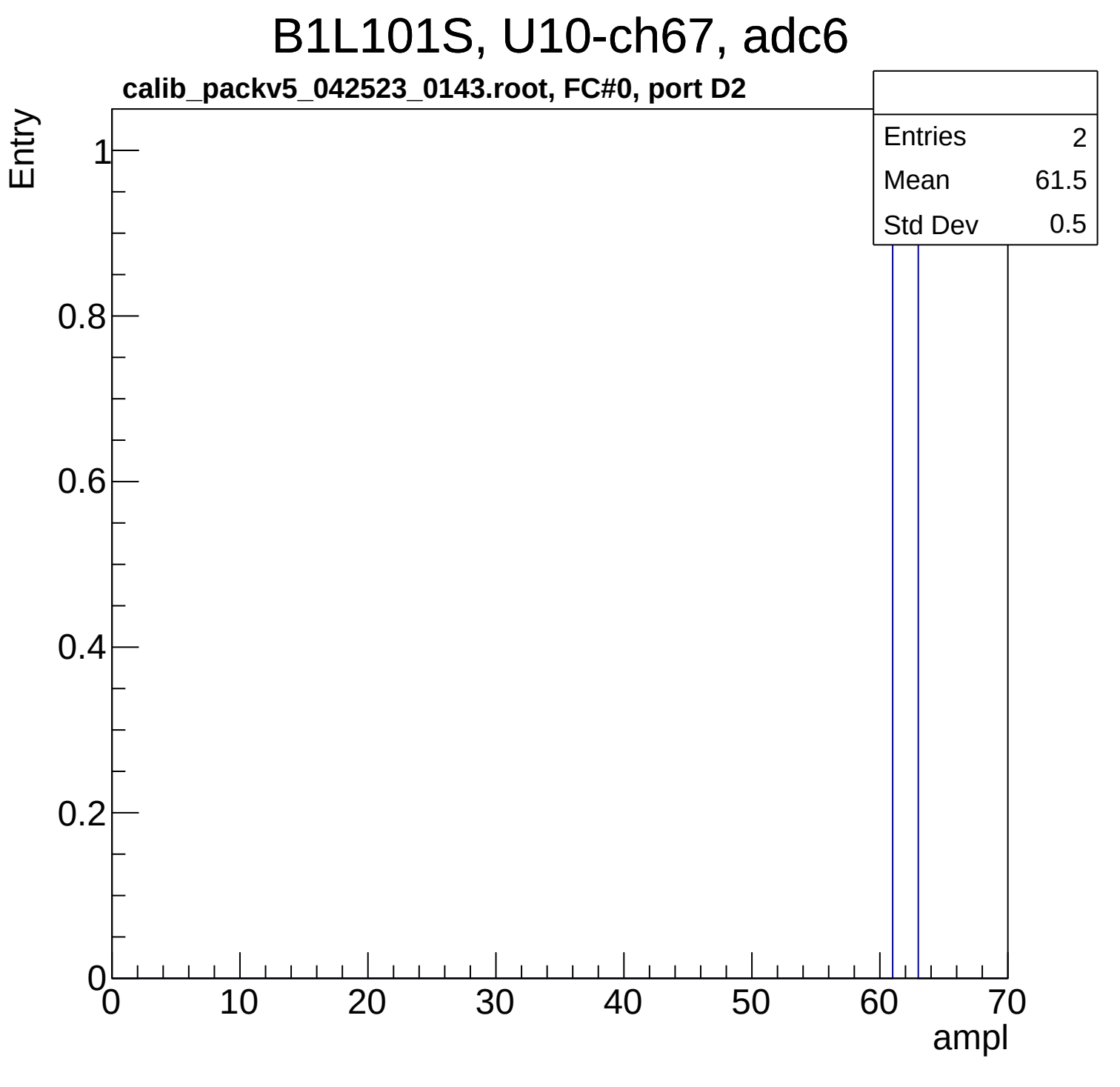
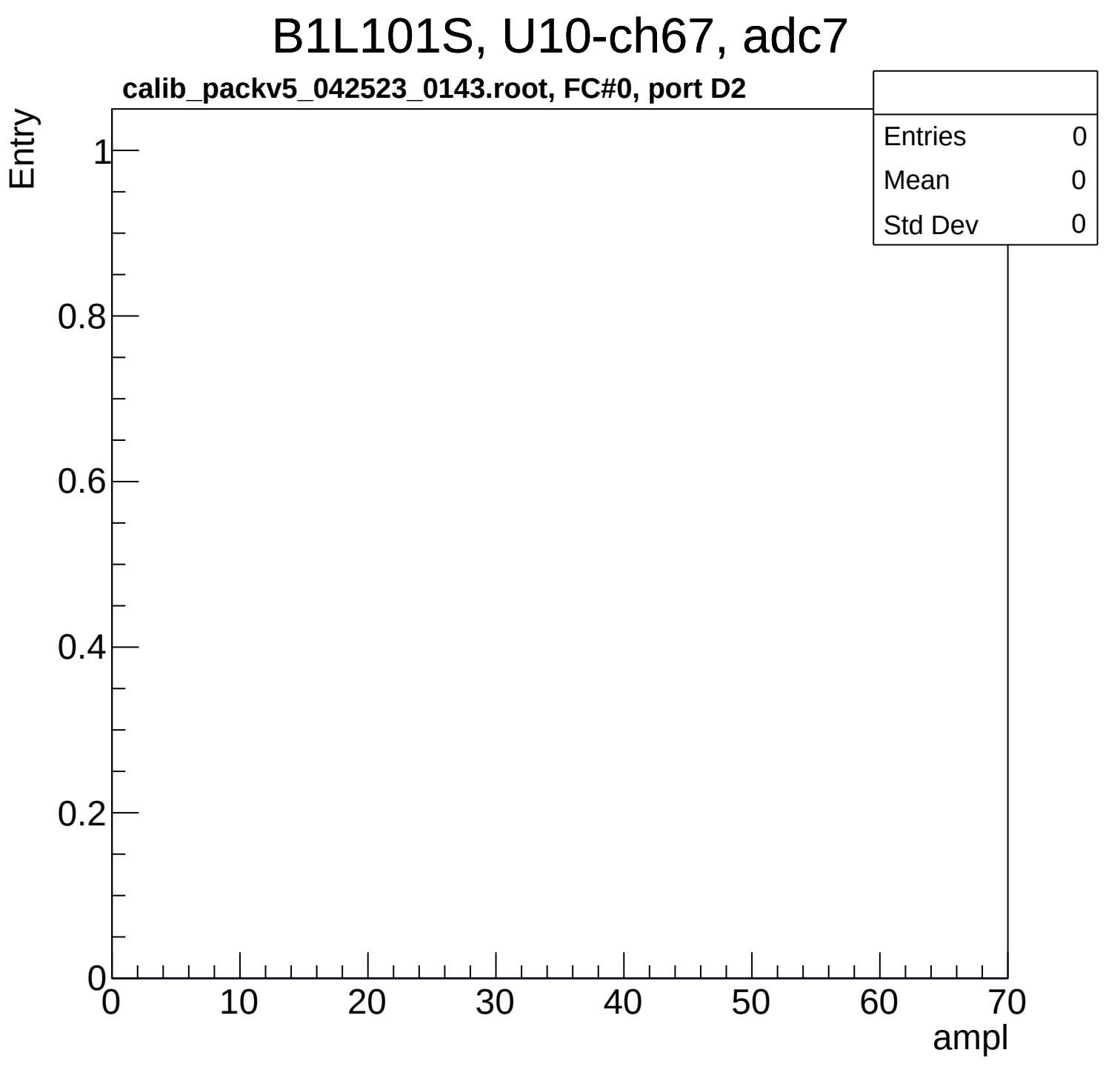

B1L101S, U10-ch67, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 61.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch67, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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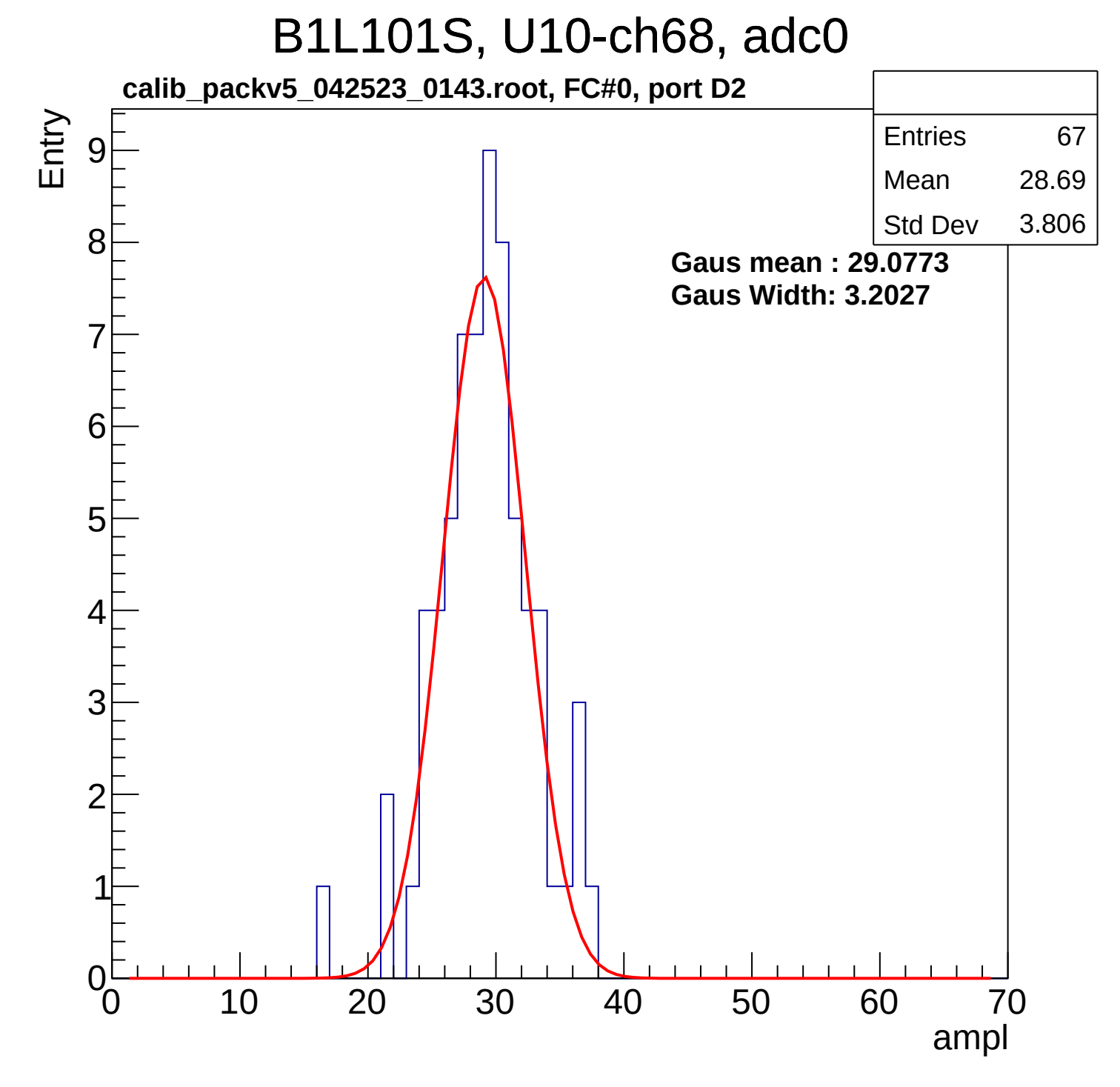
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch68, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 28.69
Std Dev 3.806
Gaus mean : 29.0773
Gaus Width: 3.2027
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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60
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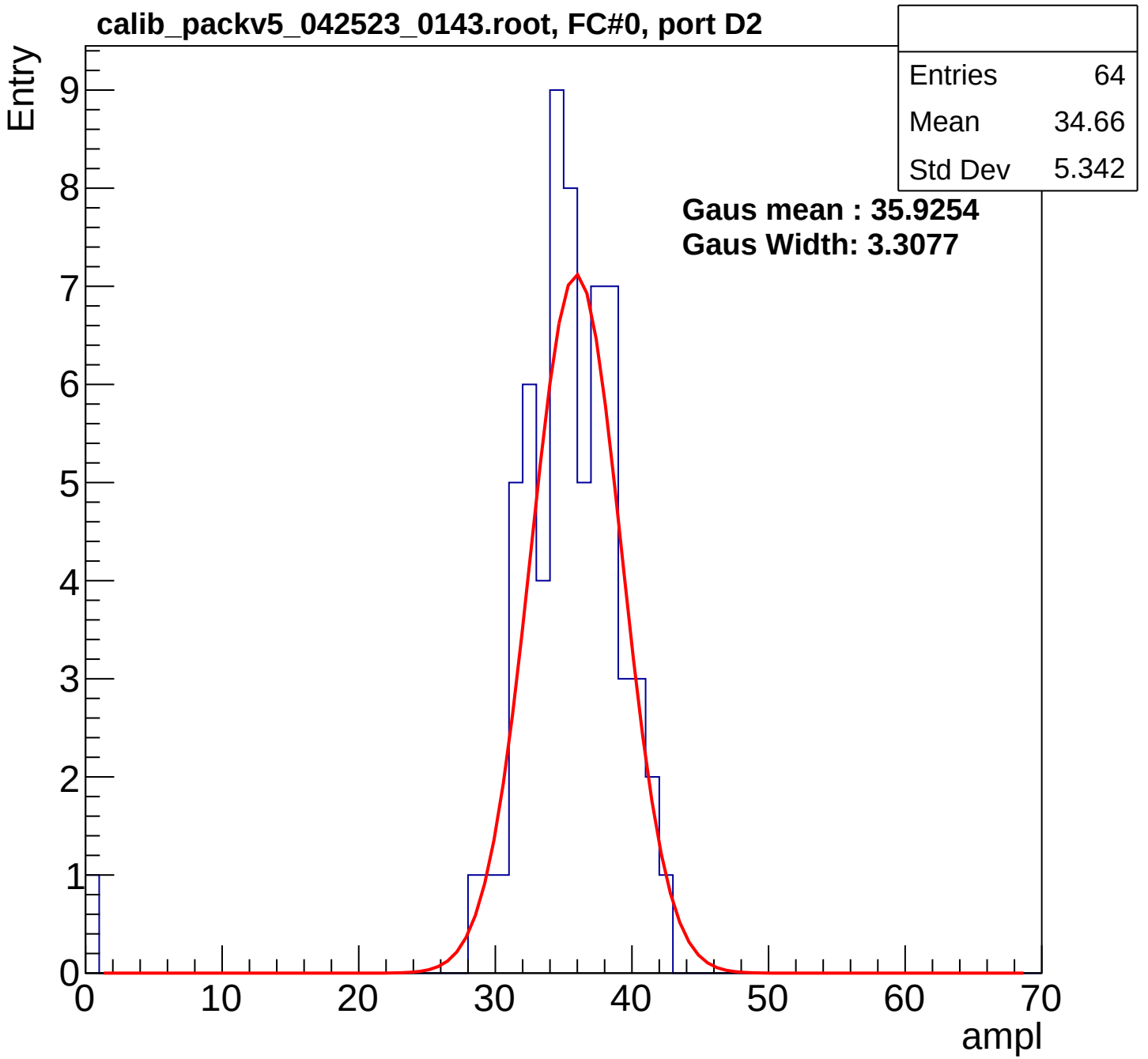
B1L101S, U10-ch68, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 34.66
Std Dev 5.342
Gaus mean : 35.9254
Gaus Width: 3.3077
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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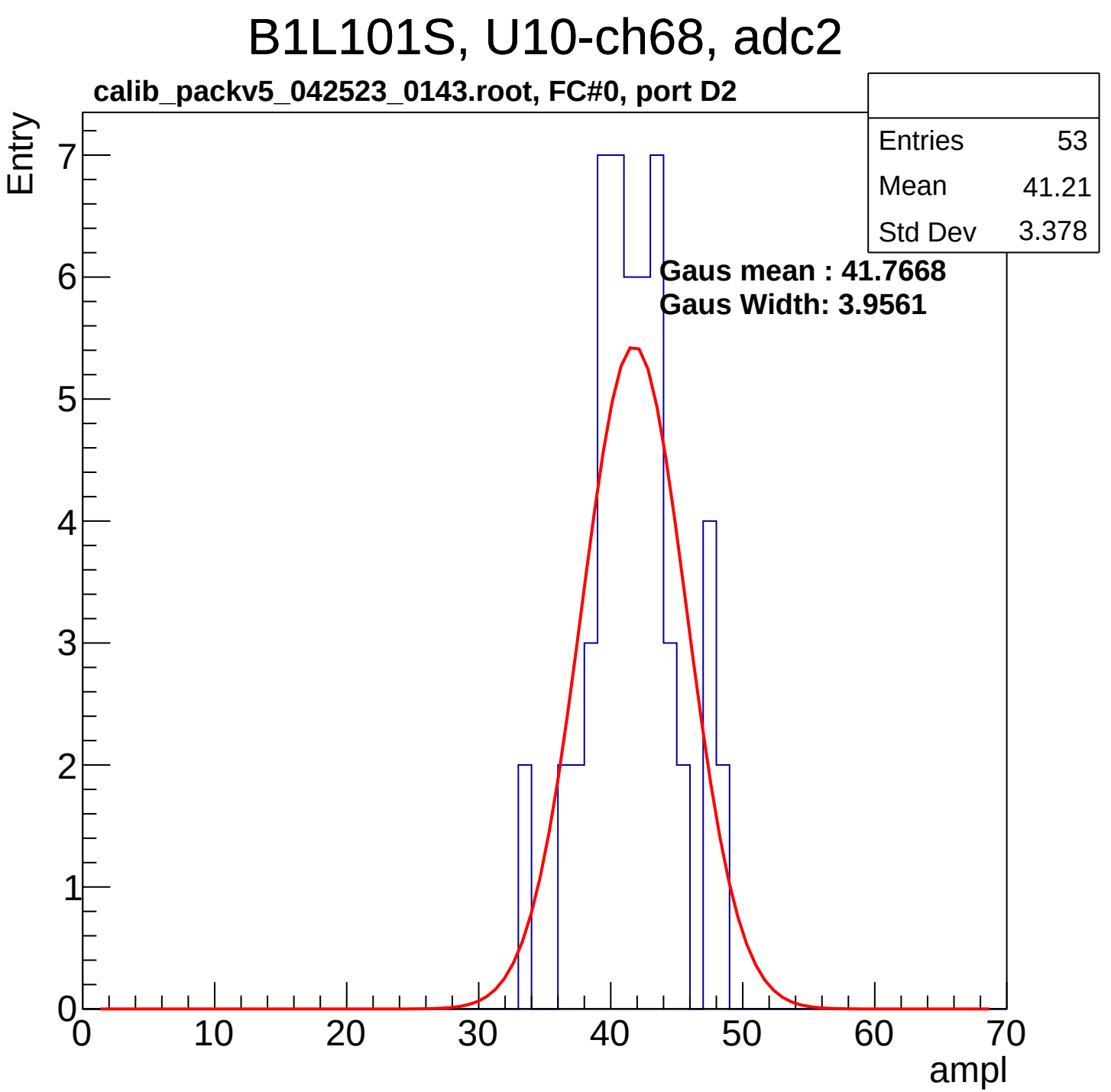
B1L101S, U10-ch68, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 41.21
Std Dev 3.378
Gaus mean : 41.7668
Gaus Width: 3.9561
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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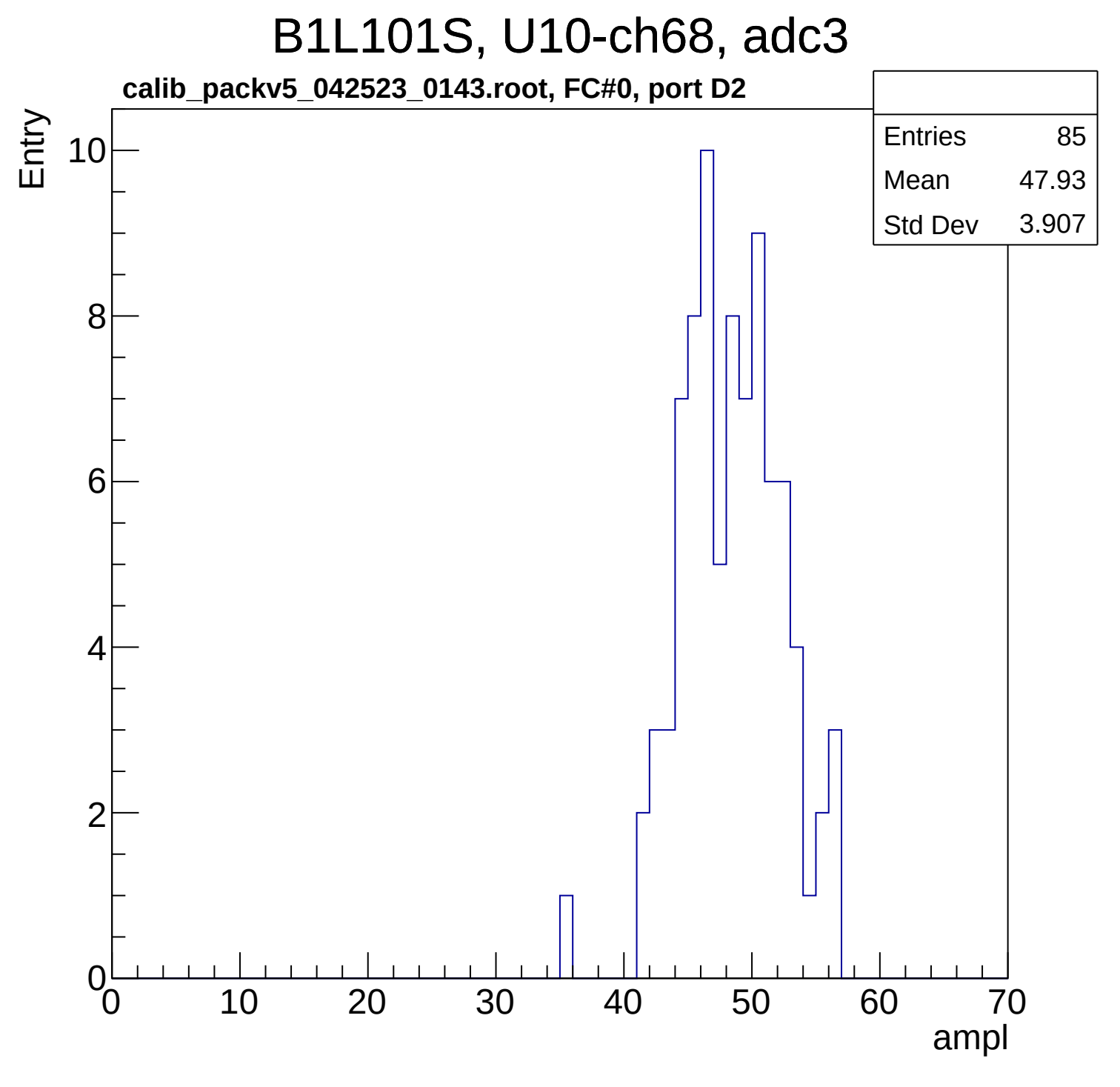
B1L101S, U10-ch68, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 85
Mean 47.93
Std Dev 3.907
Entry
ampl
0
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4
6
8
10
0
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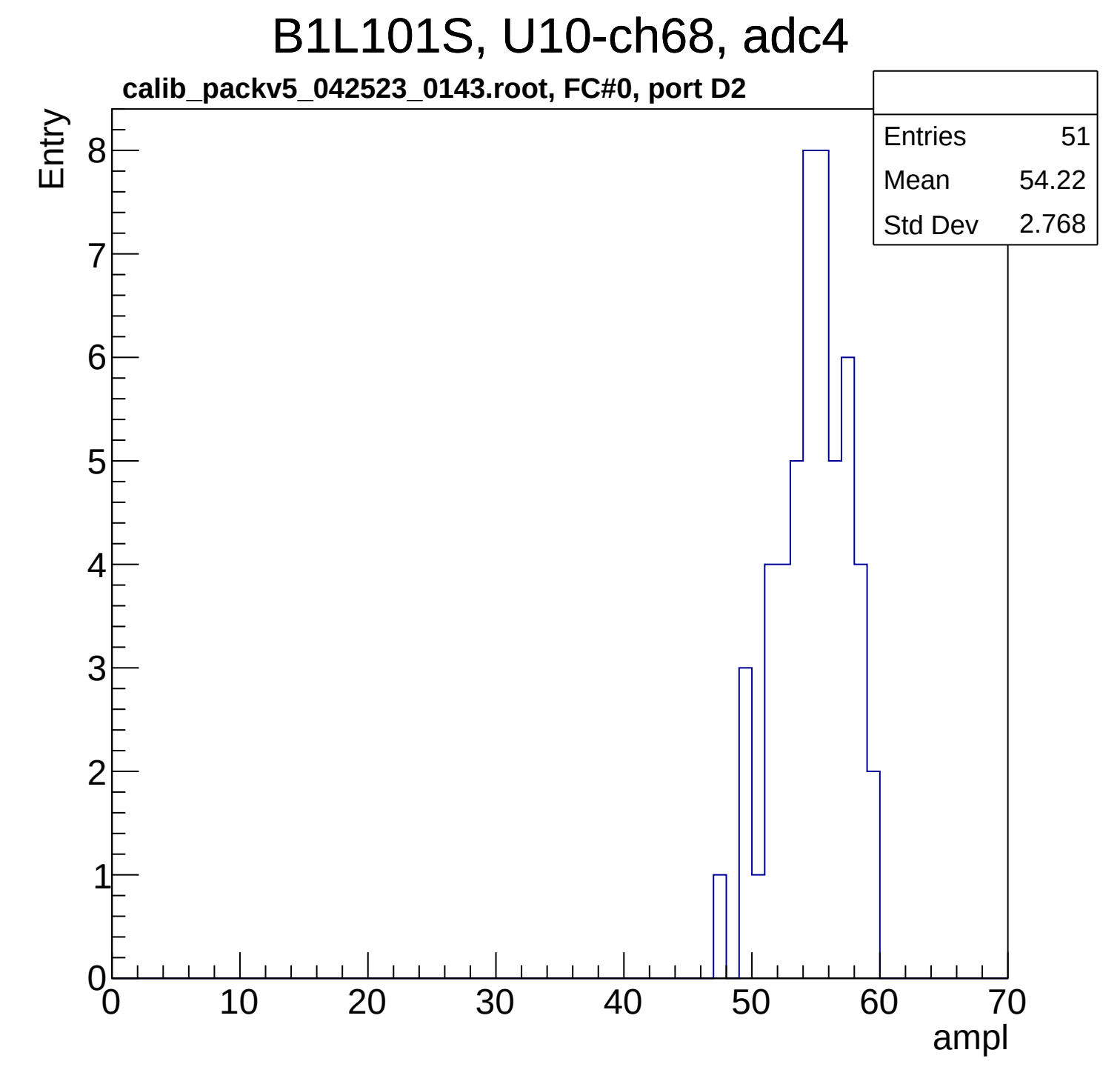
20
30
40
50
60
70


B1L101S, U10-ch68, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 54.22
Std Dev 2.768
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
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60
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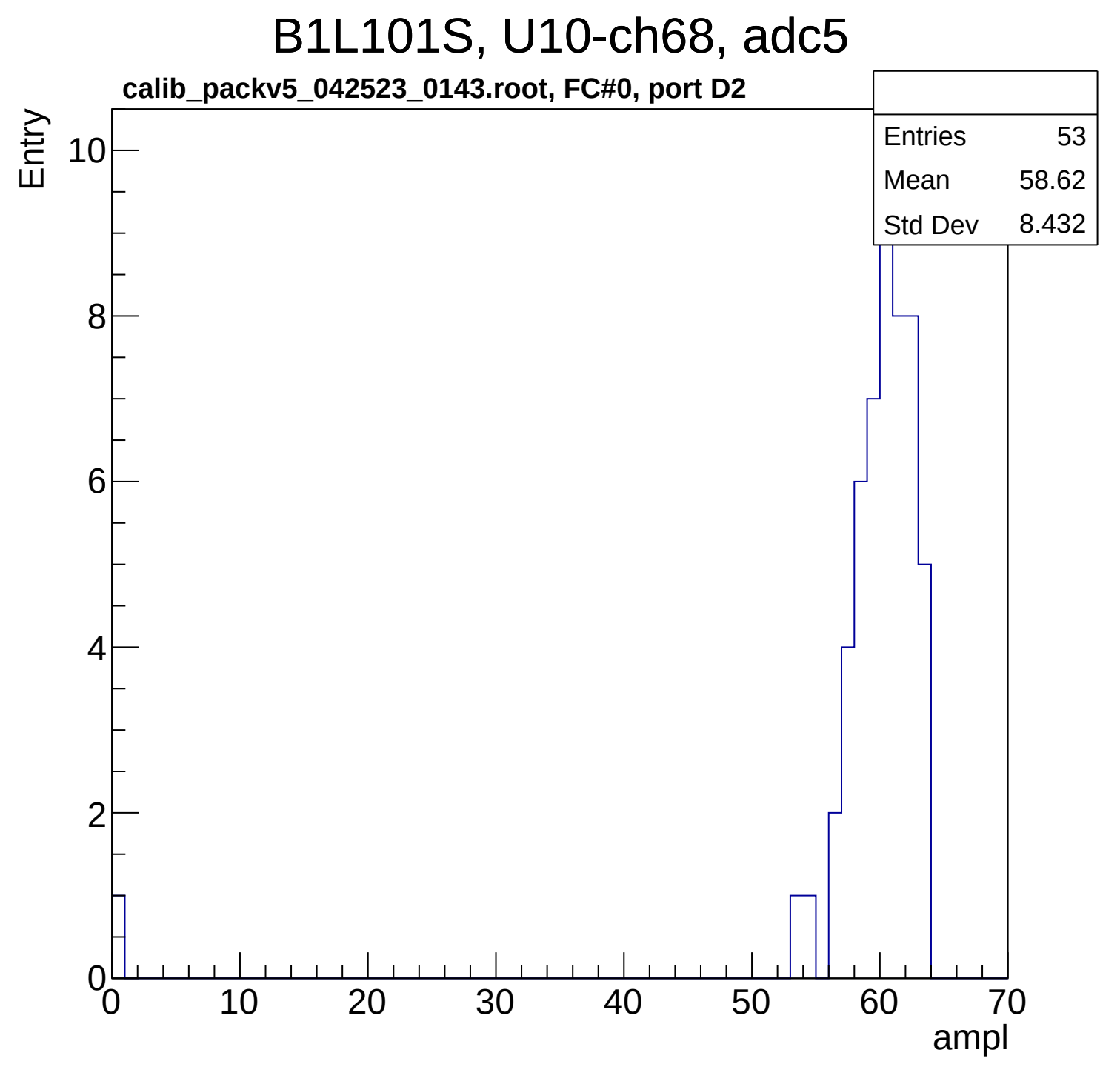
B1L101S, U10-ch68, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 58.62
Std Dev 8.432
Entry
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6
8
10
0
10
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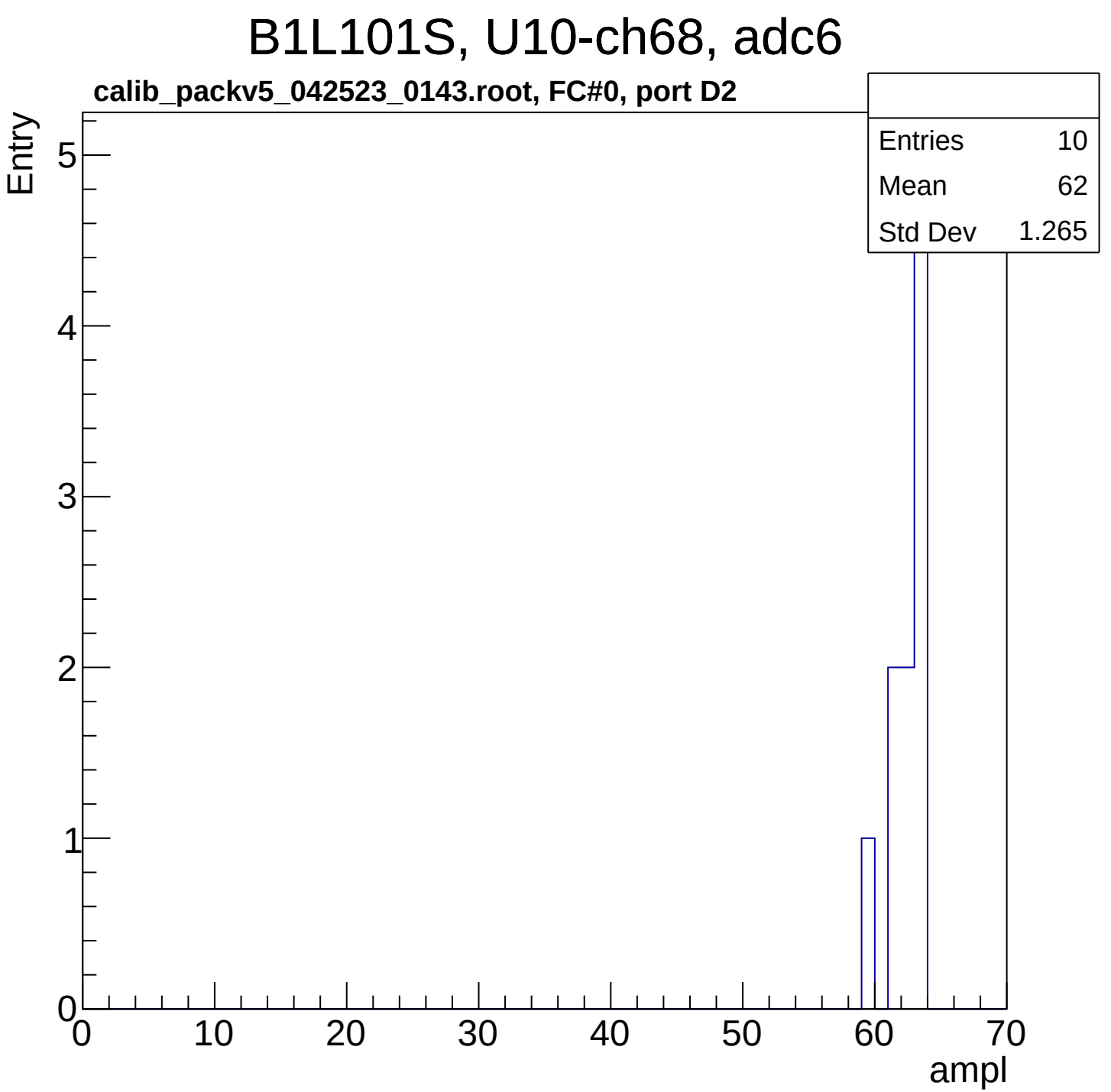
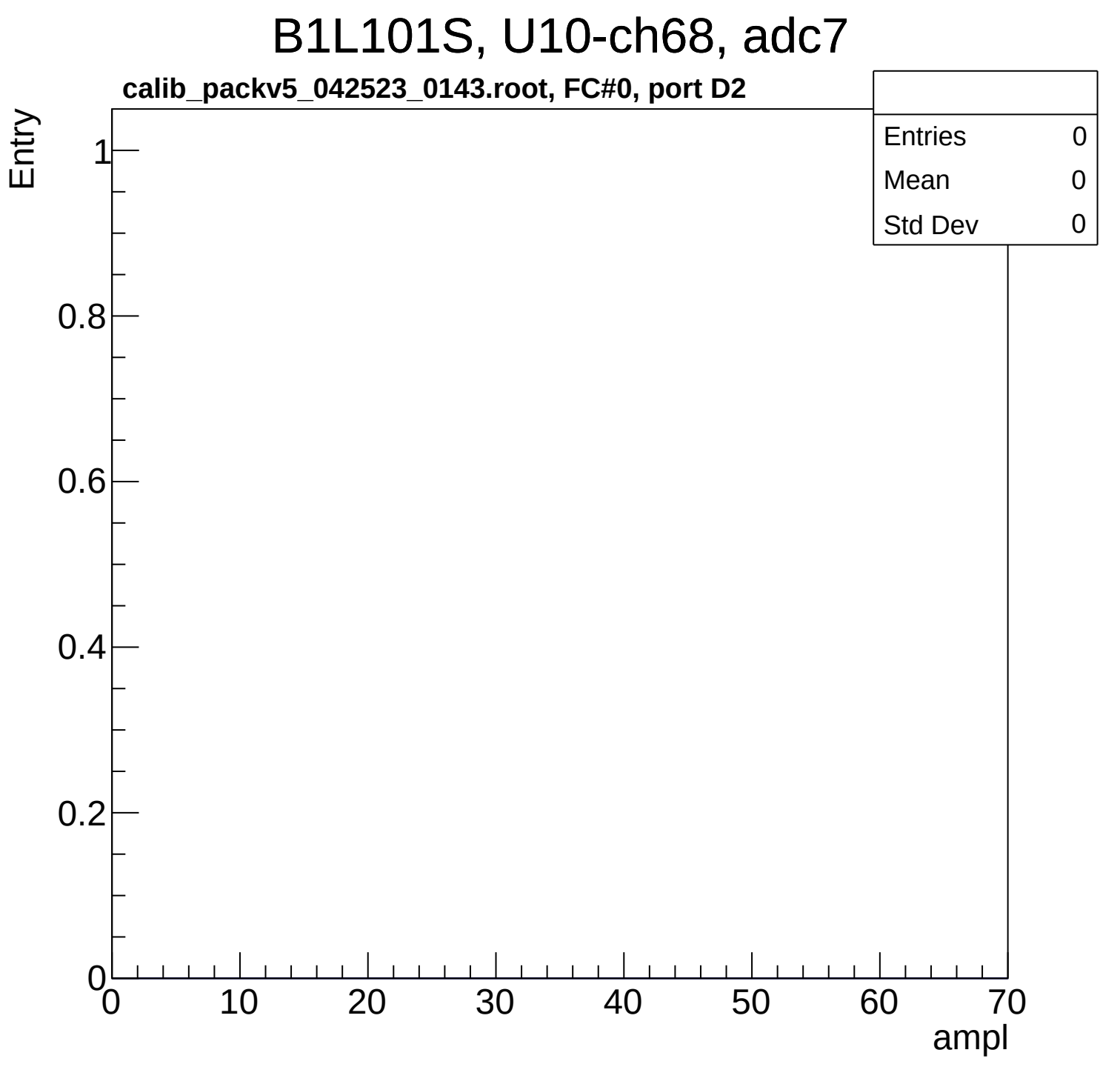
50
60
70
ampl


B1L101S, U10-ch68, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 62
Std Dev 1.265
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch68, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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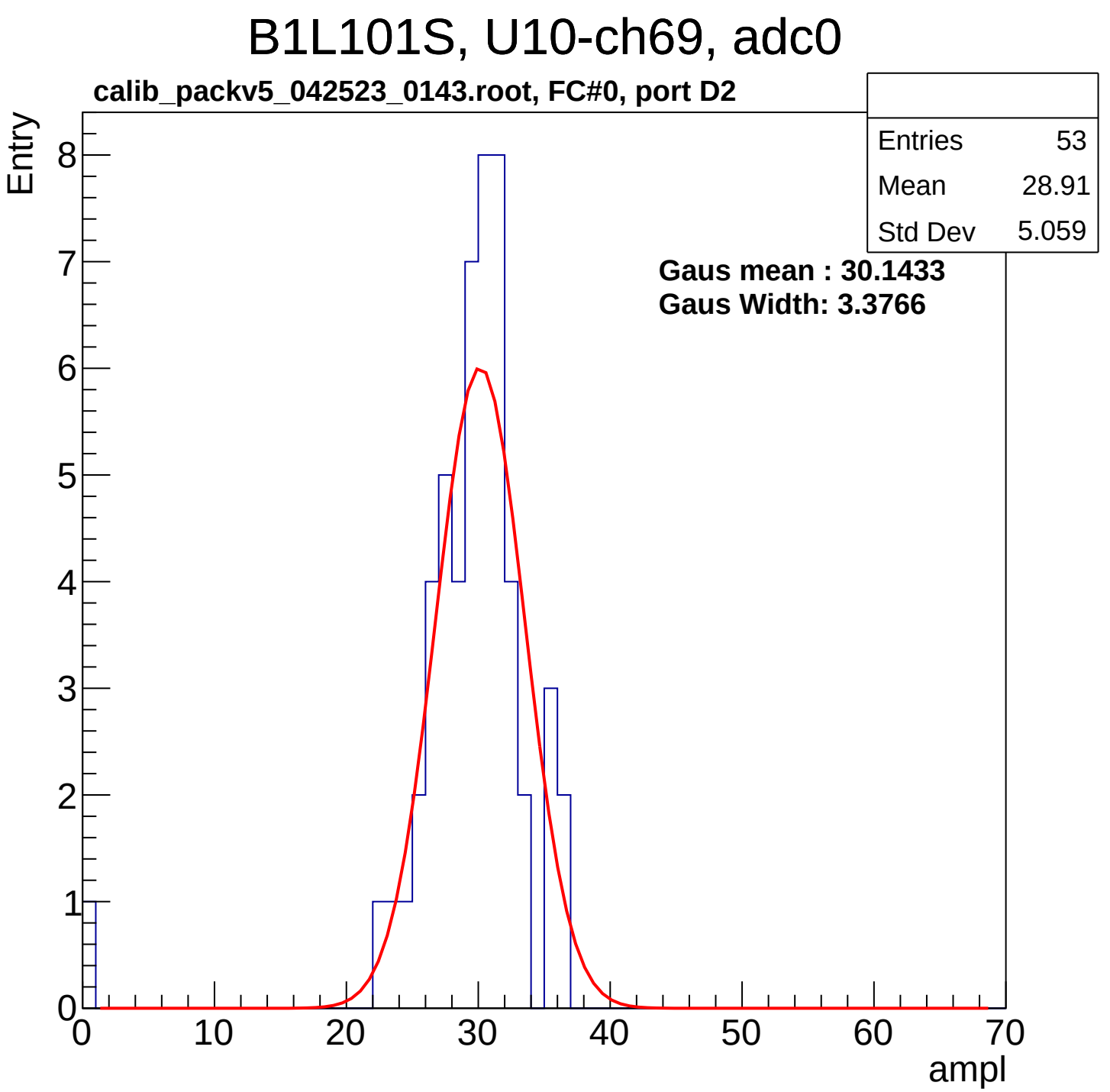
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch69, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 28.91
Std Dev 5.059
Gaus mean : 30.1433
Gaus Width: 3.3766
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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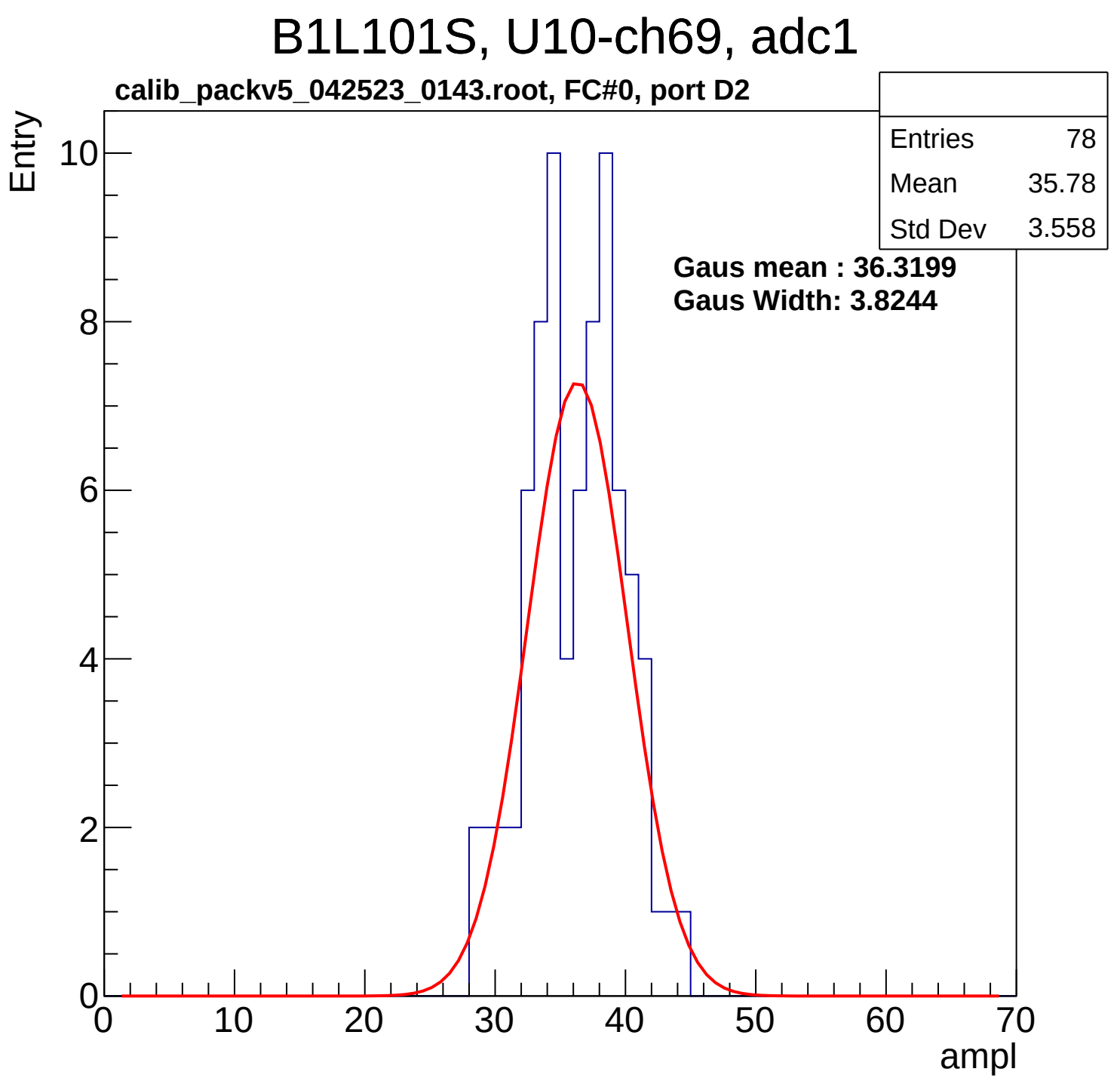
B1L101S, U10-ch69, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 35.78
Std Dev 3.558
Gaus mean : 36.3199
Gaus Width: 3.8244
Entry
ampl
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0
10
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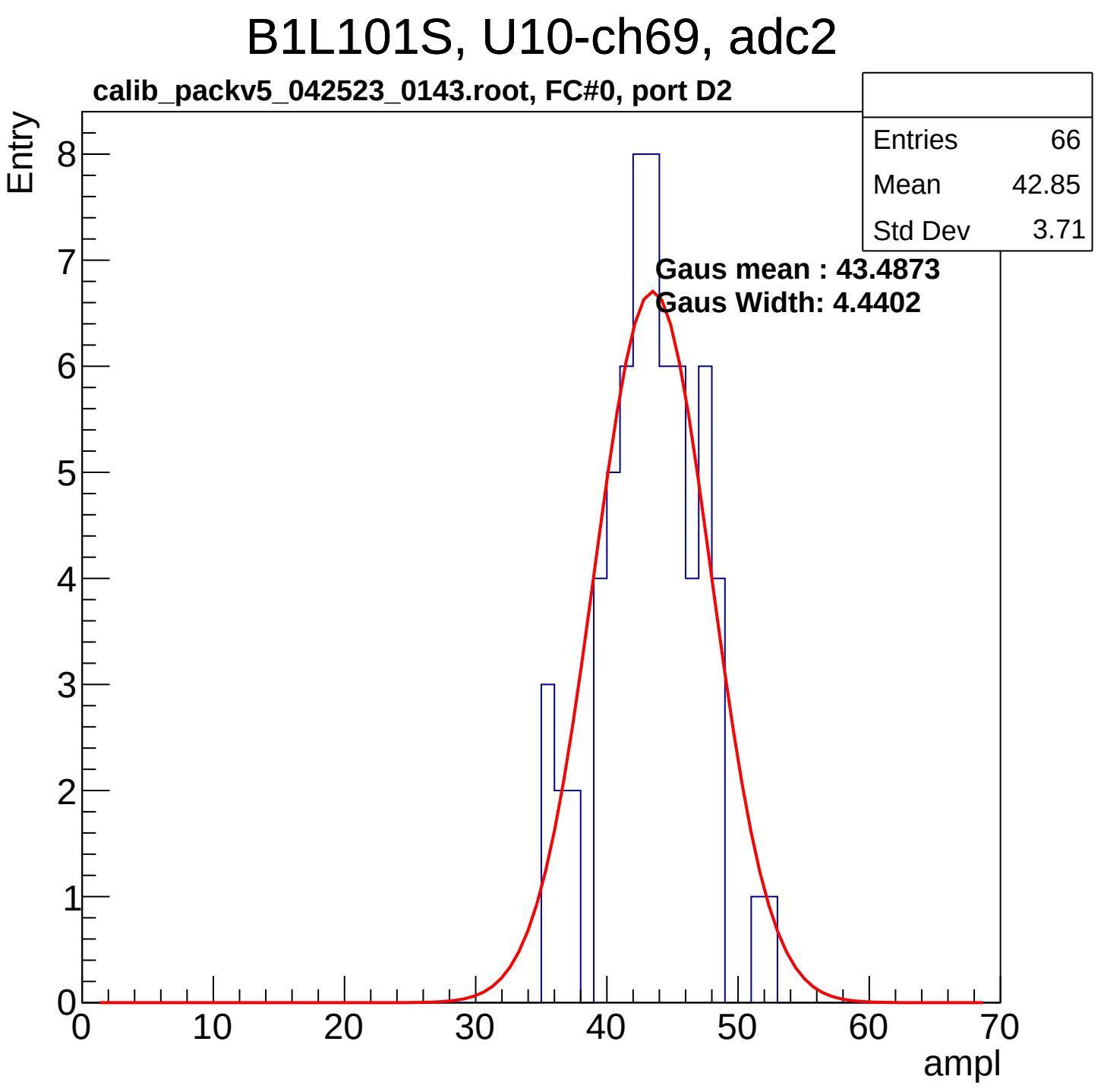
B1L101S, U10-ch69, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 42.85
Std Dev 3.71
Gaus mean : 43.4873
Gaus Width: 4.4402
Entry
ampl
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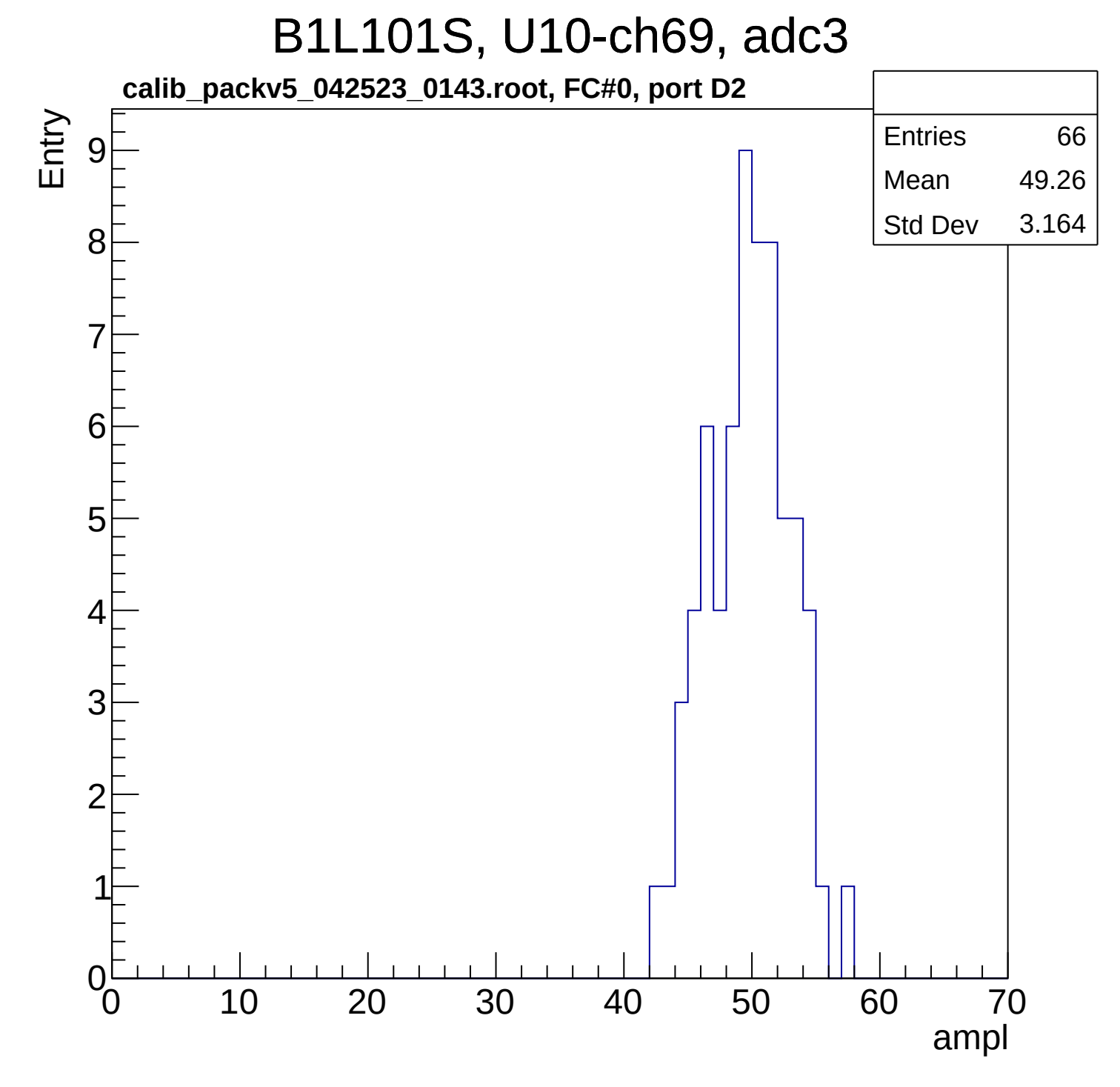
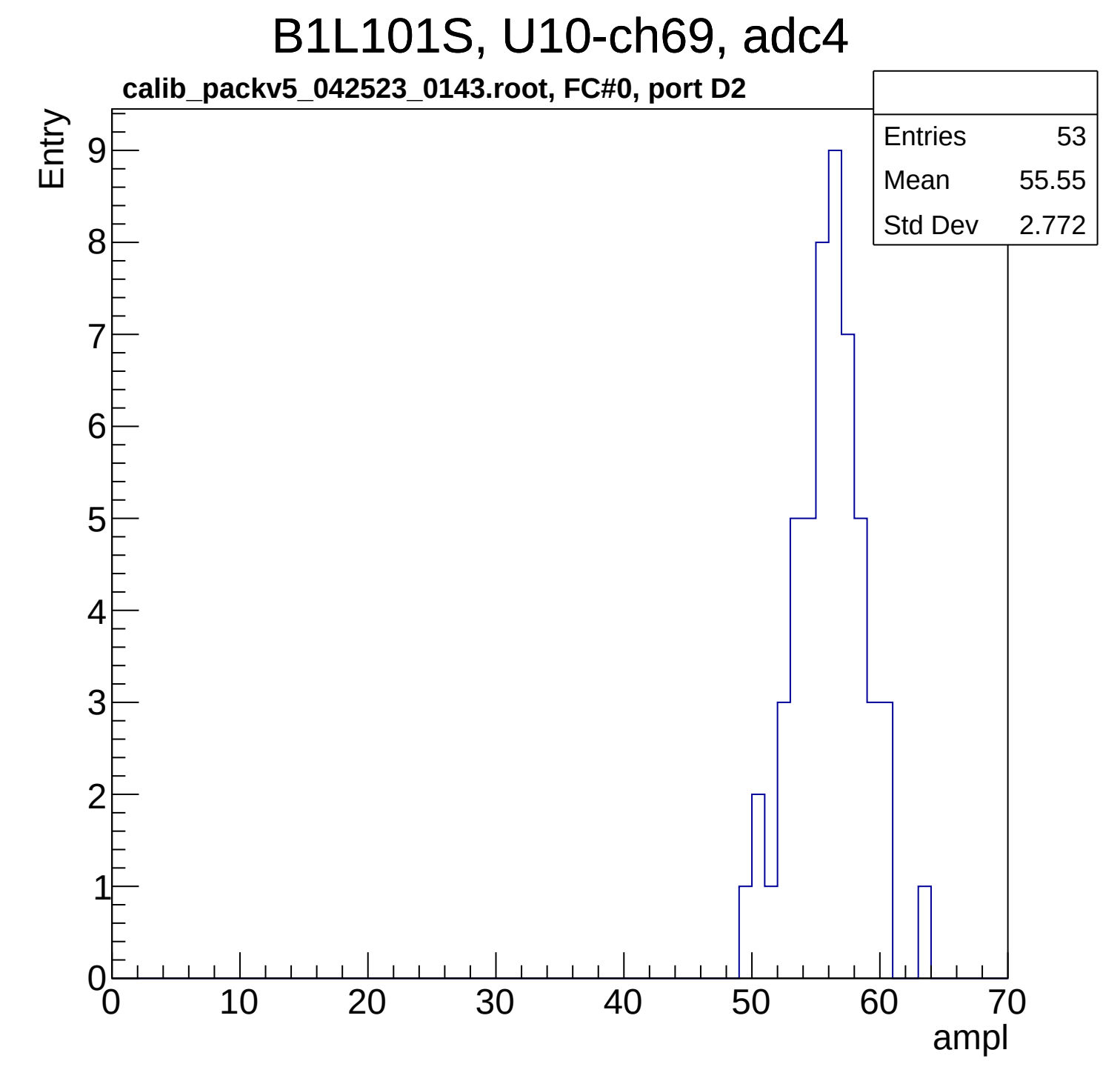
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch69, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 49.26
Std Dev 3.164
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch69, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 55.55
Std Dev 2.772
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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40
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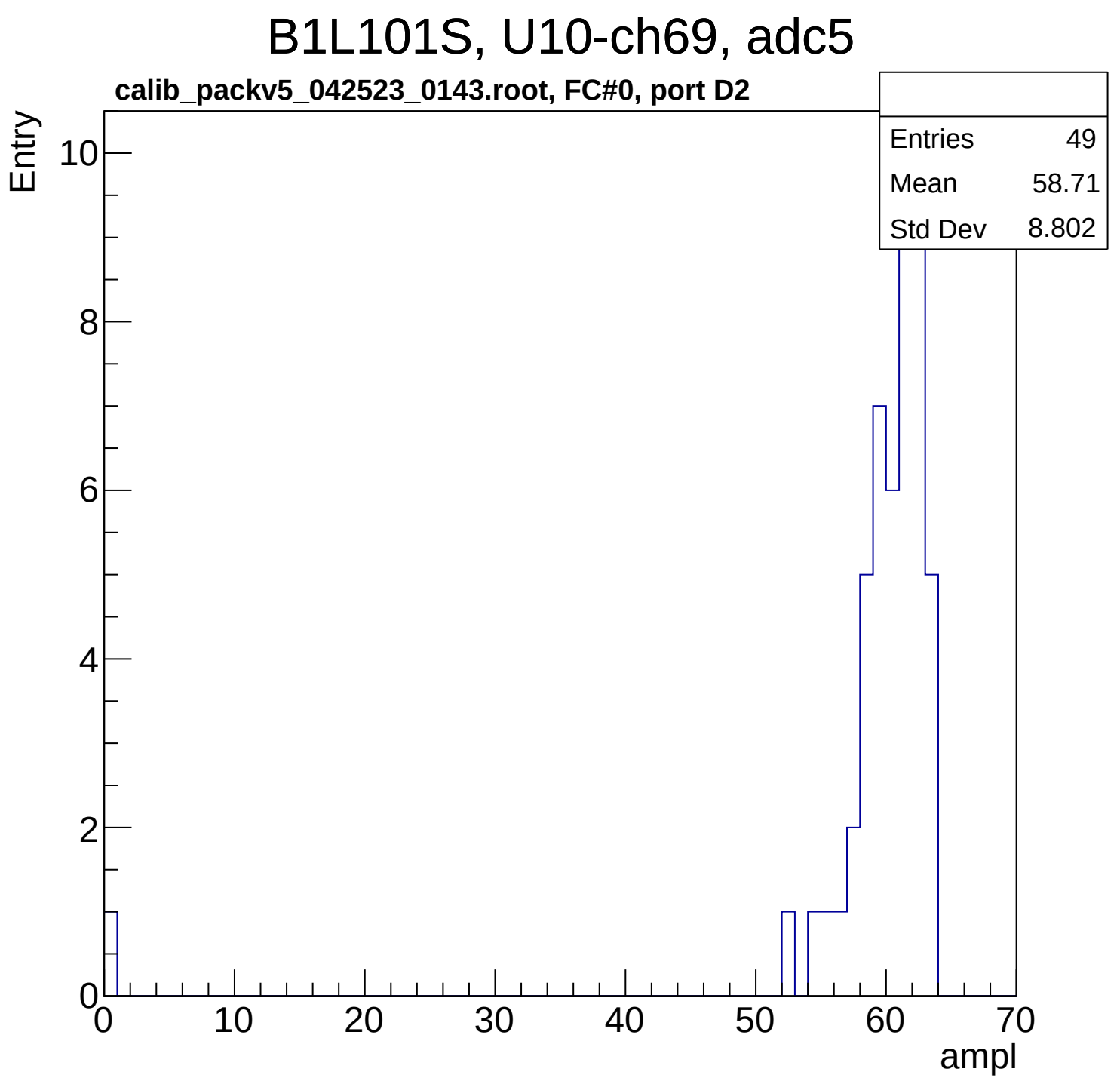
60
70


B1L101S, U10-ch69, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 58.71
Std Dev 8.802
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
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60
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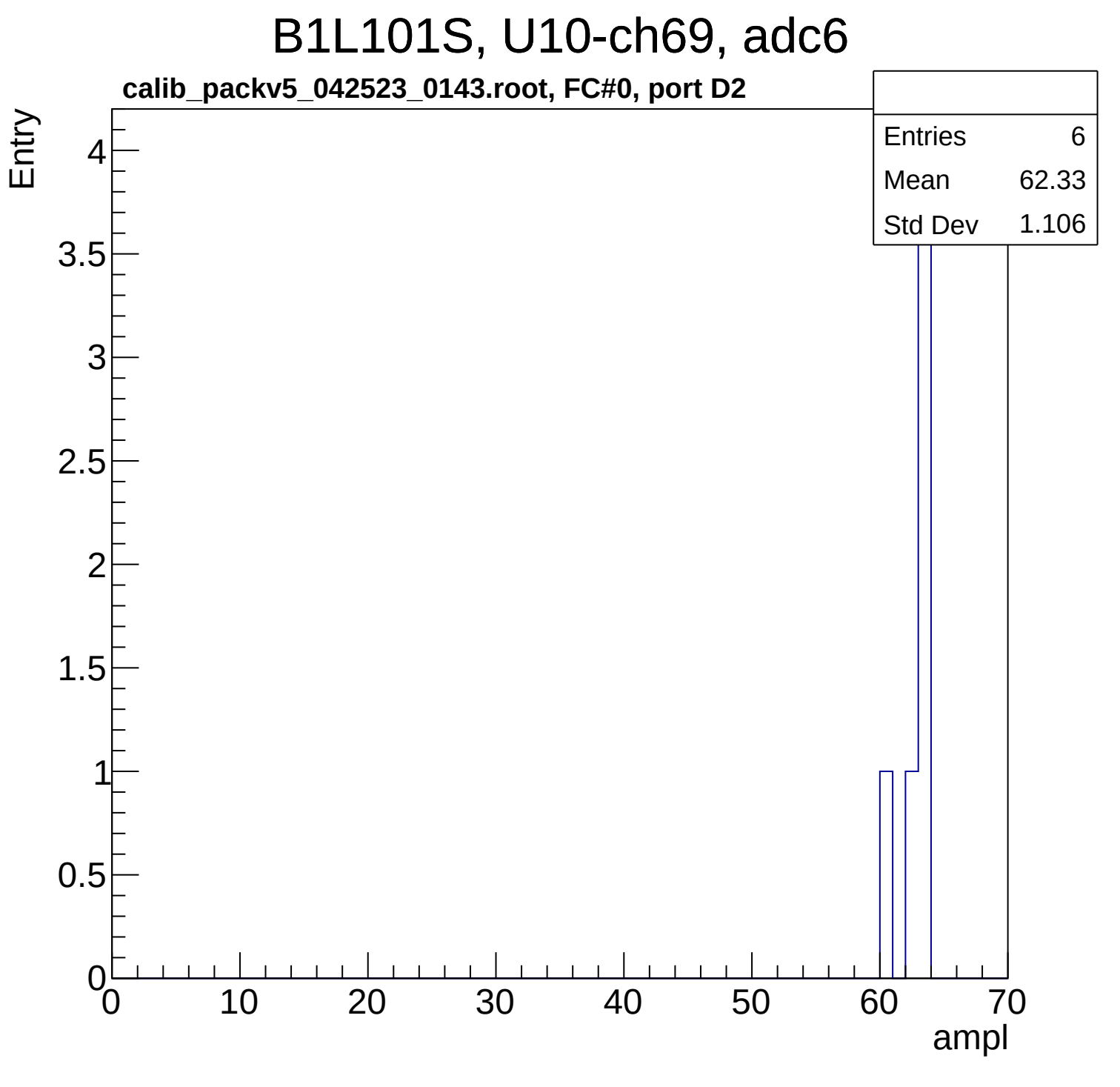
B1L101S, U10-ch69, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 62.33
Std Dev 1.106
Entry
ampl
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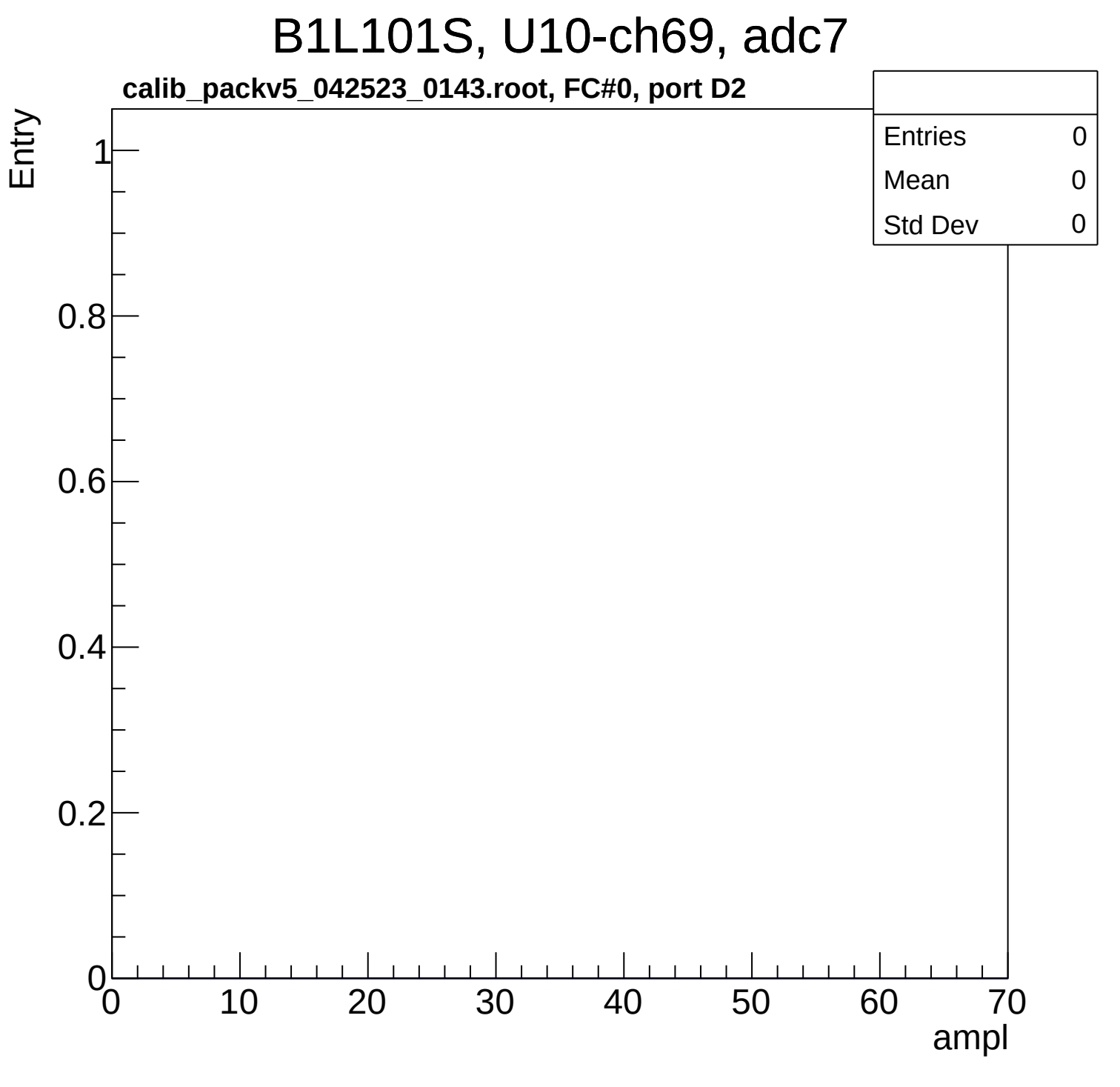
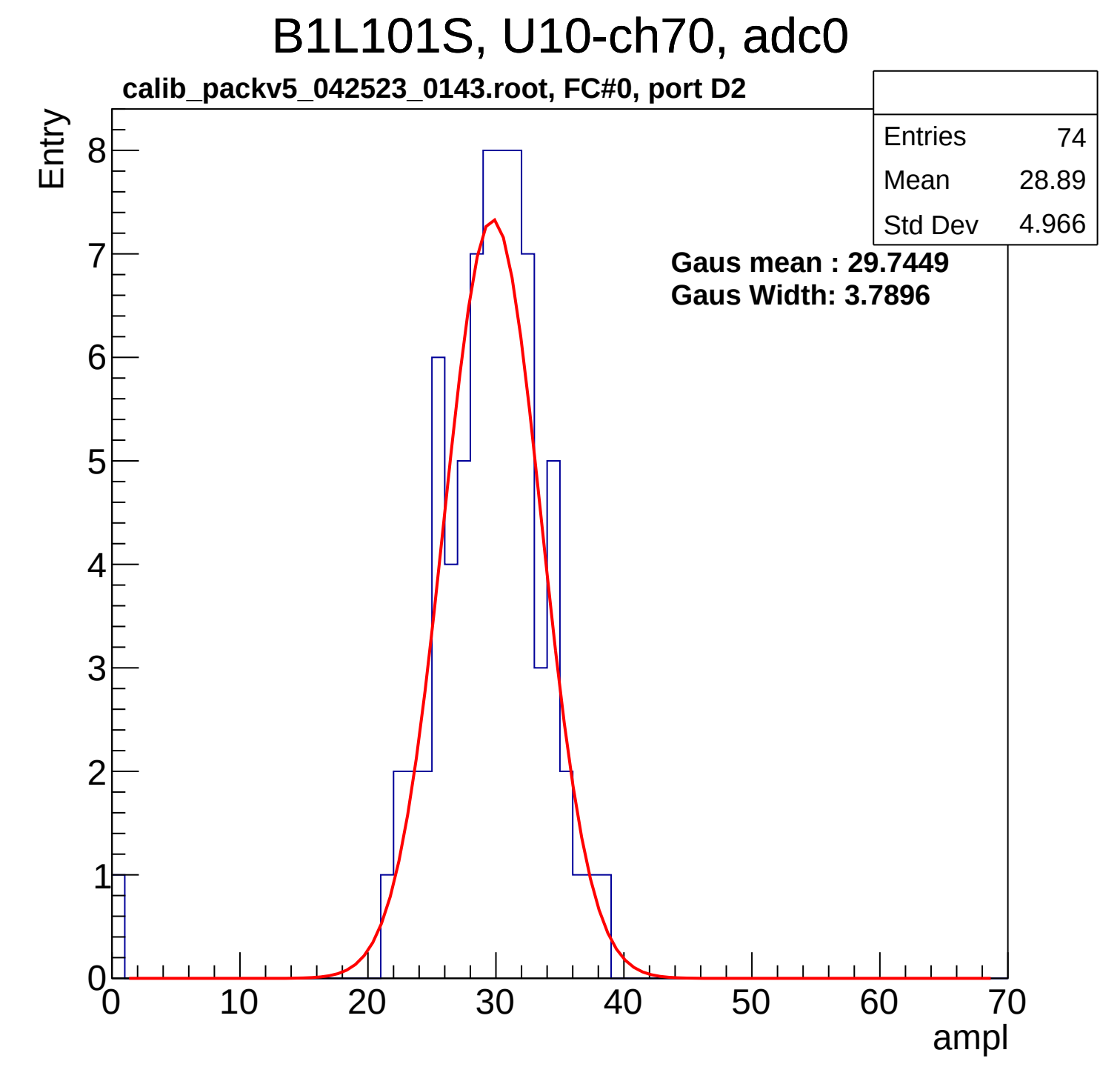
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L101S, U10-ch69, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch70, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 28.89
Std Dev 4.966
Gaus mean : 29.7449
Gaus Width: 3.7896
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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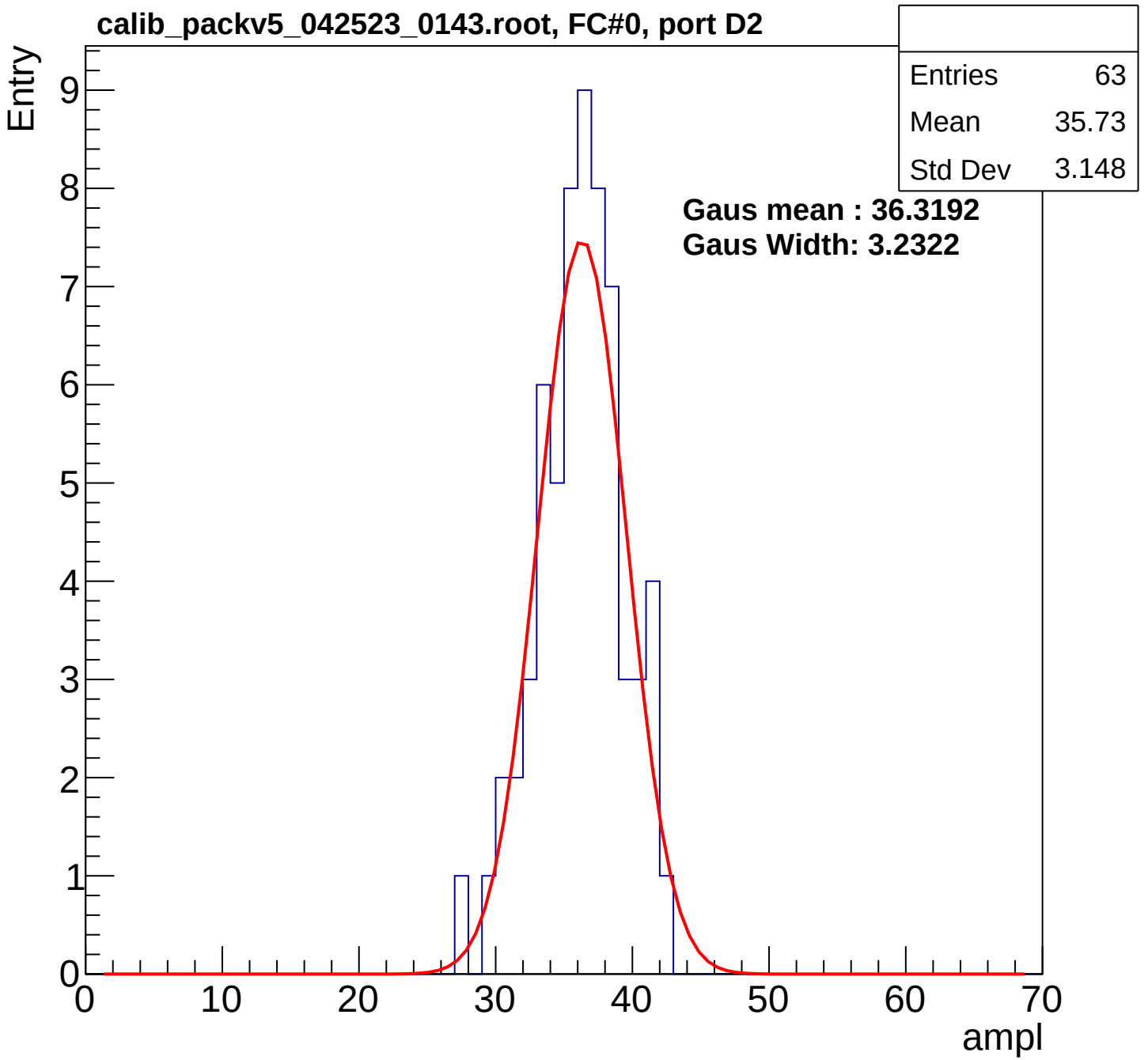
B1L101S, U10-ch70, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 35.73
Std Dev 3.148
Gaus mean : 36.3192
Gaus Width: 3.2322
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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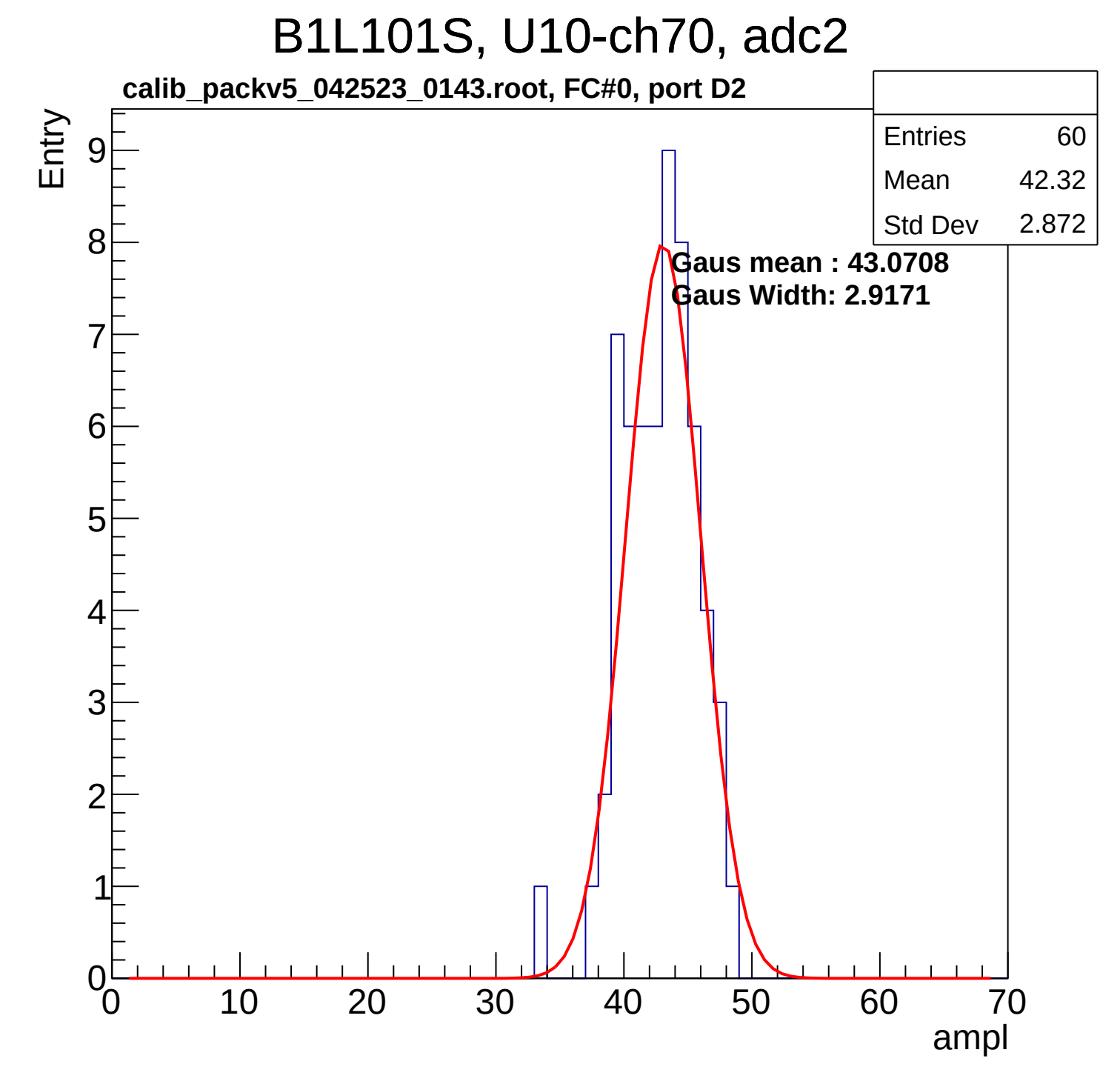
B1L101S, U10-ch70, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 42.32
Std Dev 2.872
Gaus mean : 43.0708
Gaus Width: 2.9171
Entry
ampl
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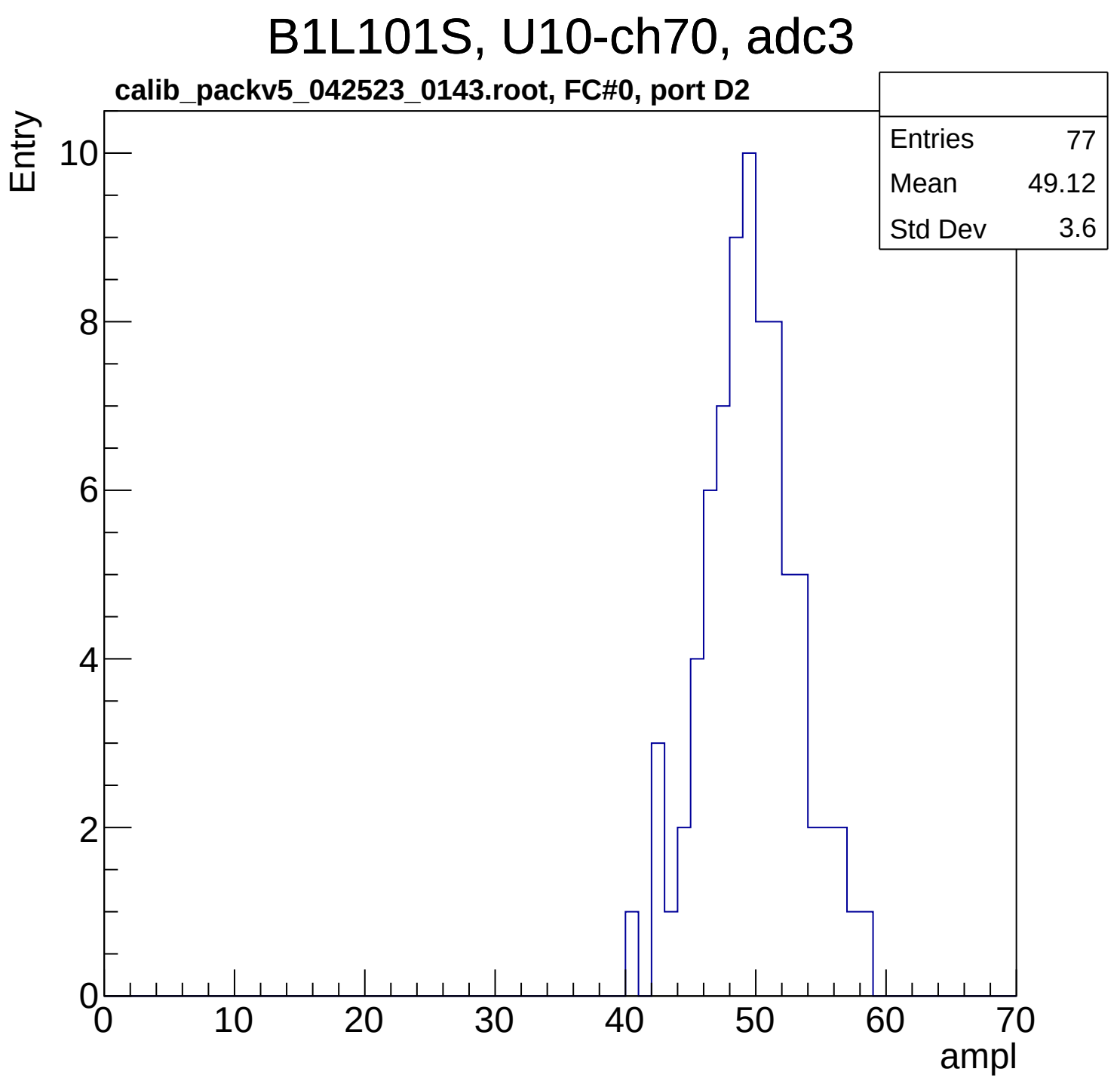
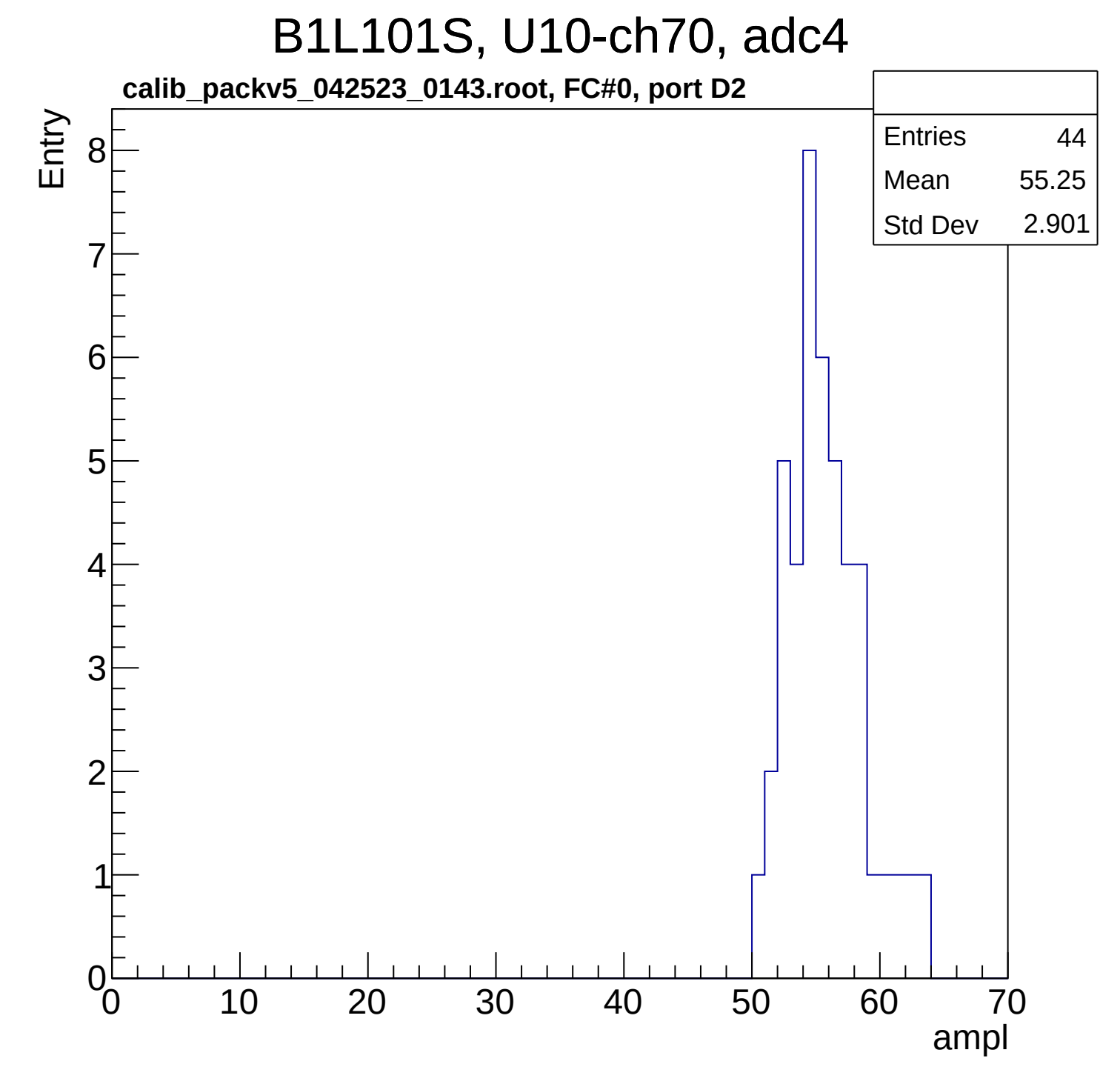
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L101S, U10-ch70, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 49.12
Std Dev 3.6
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch70, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 44
Mean 55.25
Std Dev 2.901
Entry
ampl
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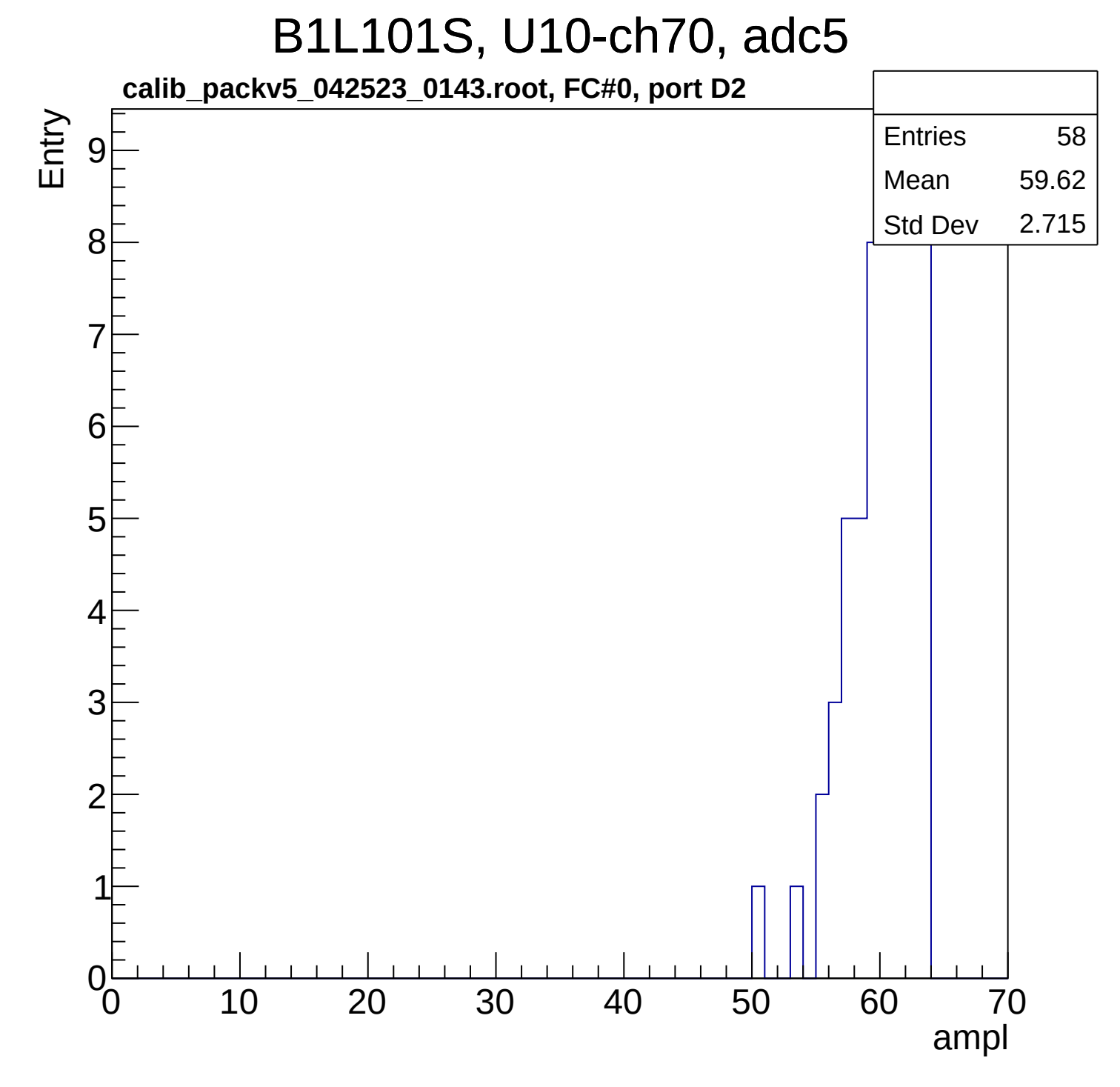
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch70, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 59.62
Std Dev 2.715
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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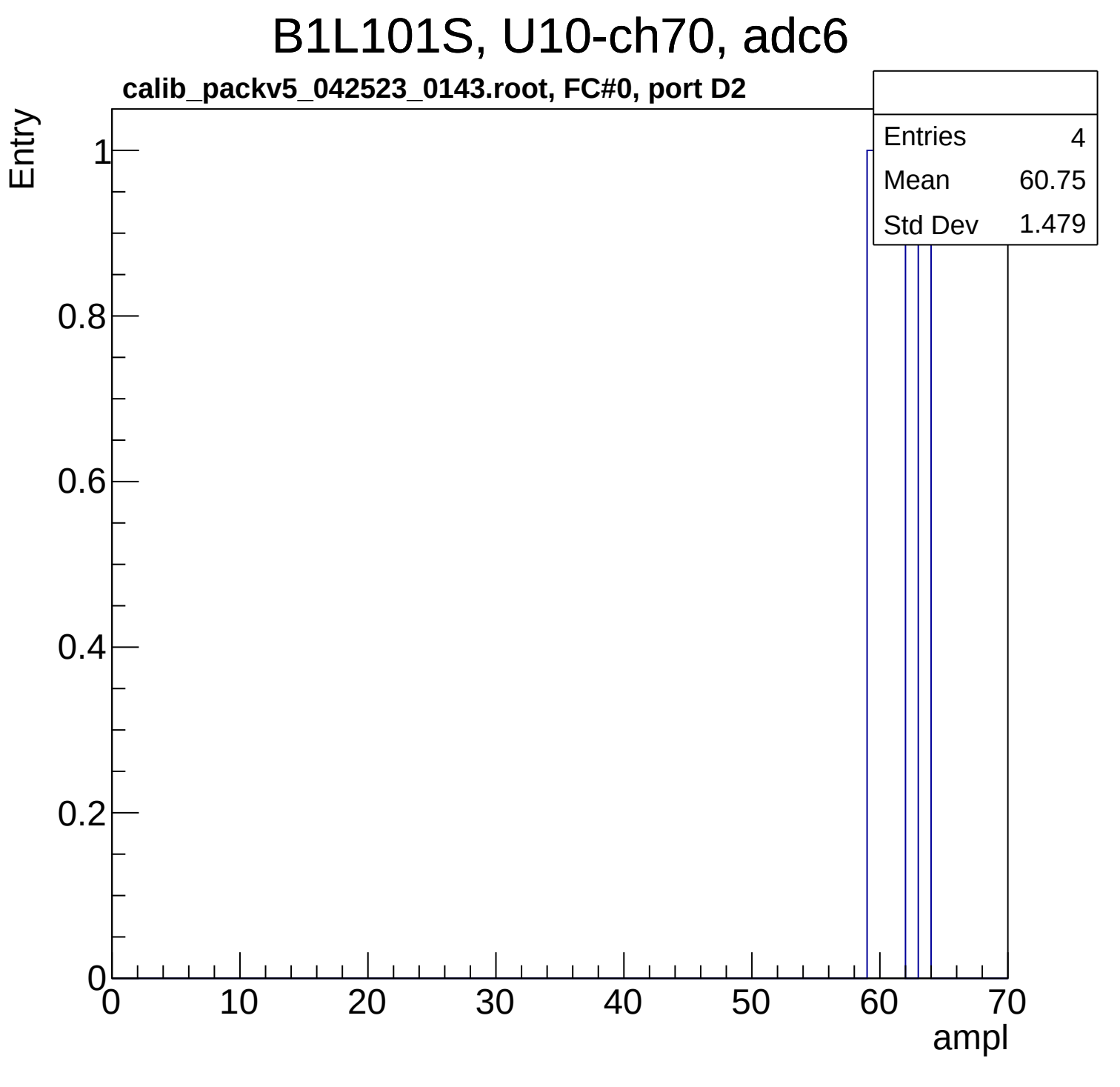
B1L101S, U10-ch70, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 60.75
Std Dev 1.479
Entry
ampl
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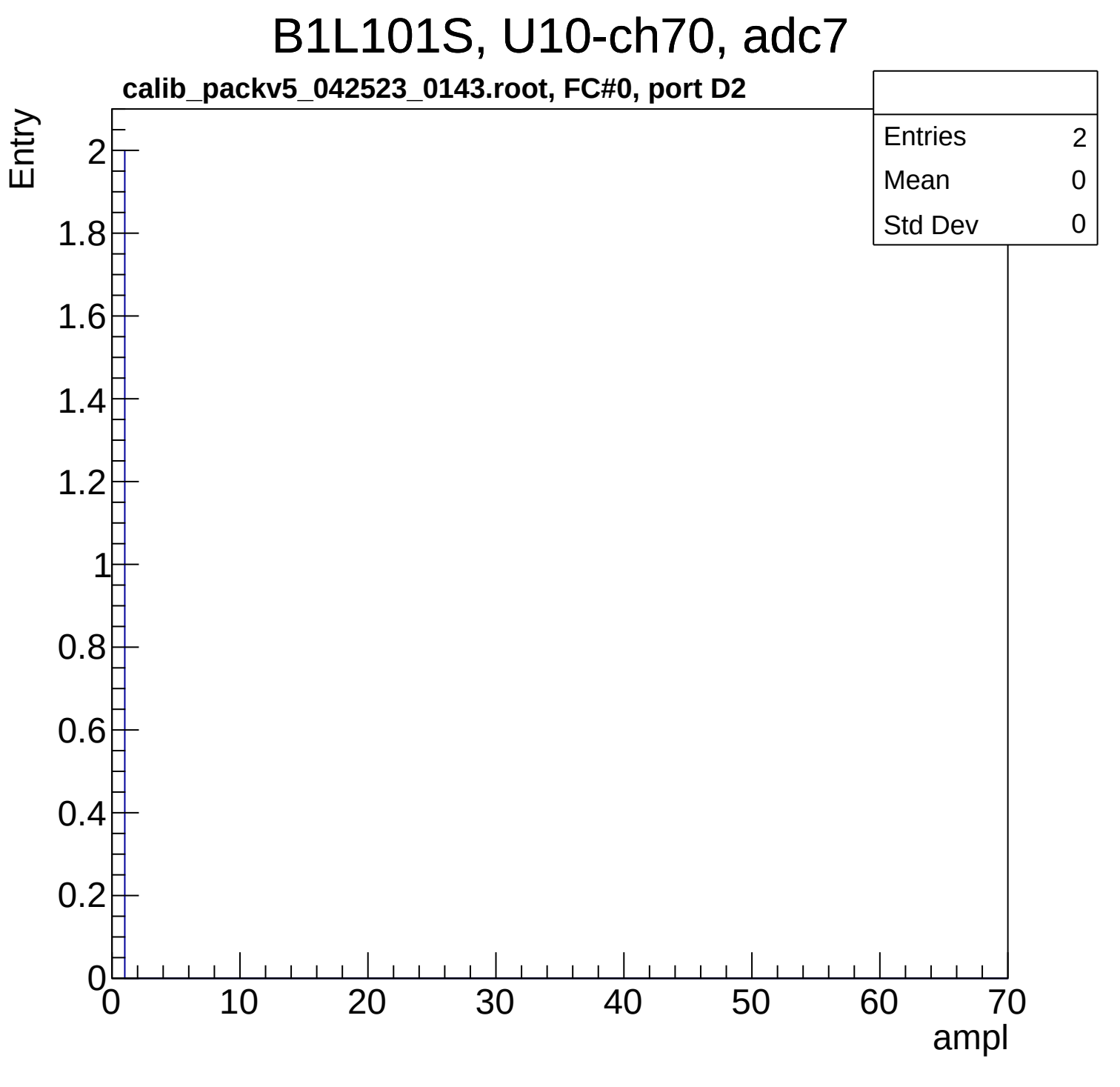
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L101S, U10-ch70, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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20
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40
50
60
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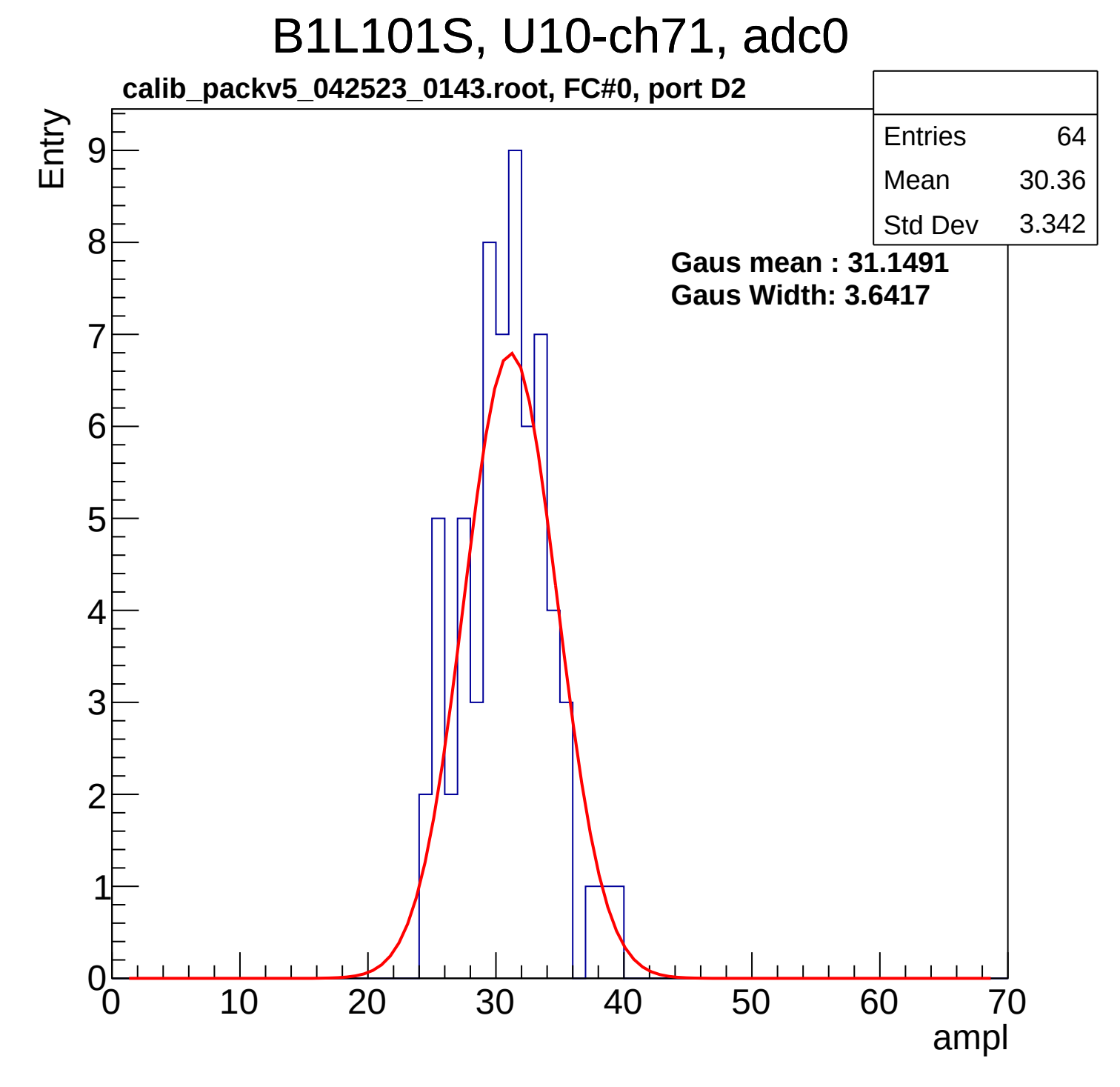
B1L101S, U10-ch71, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 30.36
Std Dev 3.342
Gaus mean : 31.1491
Gaus Width: 3.6417
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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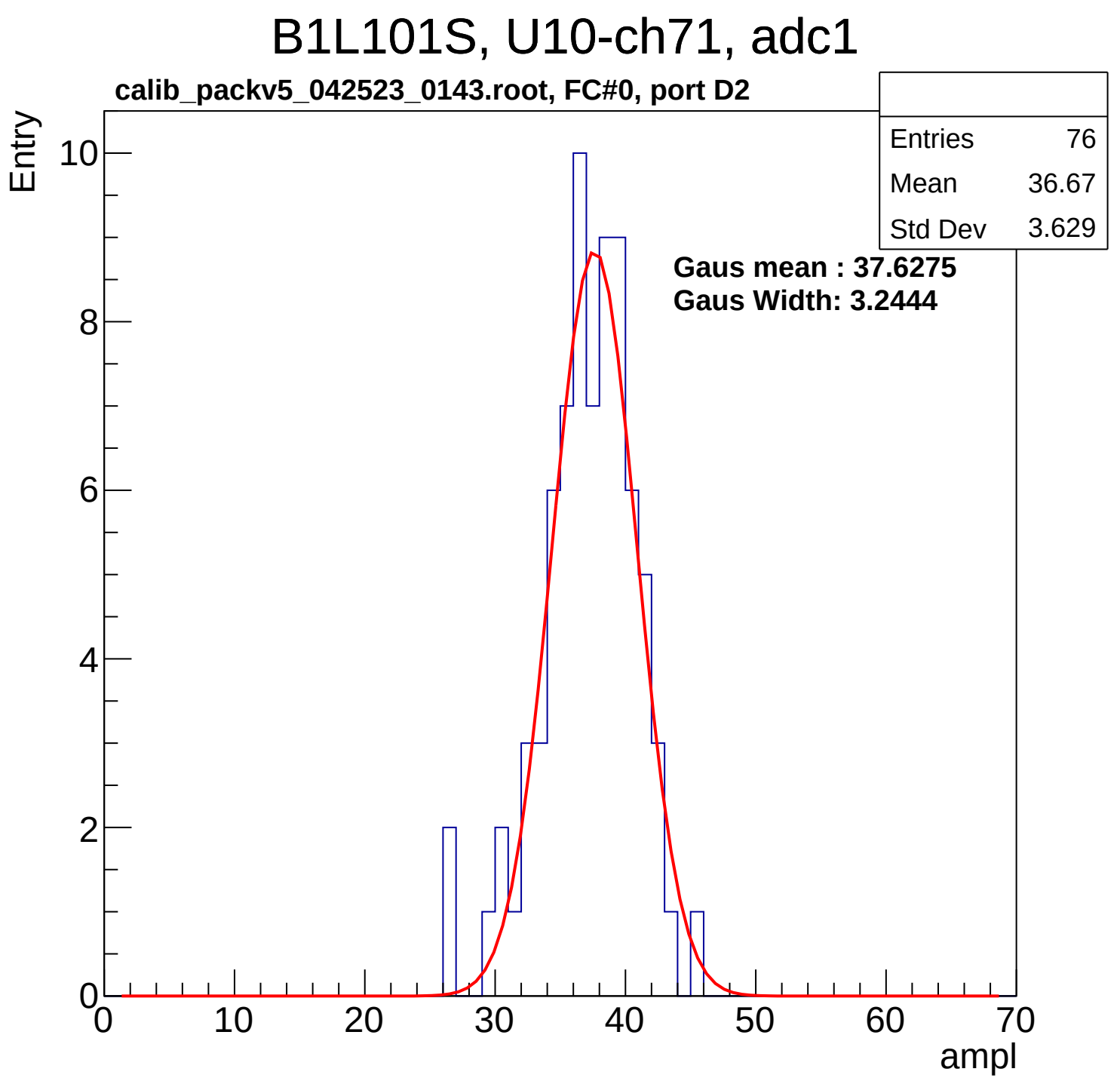
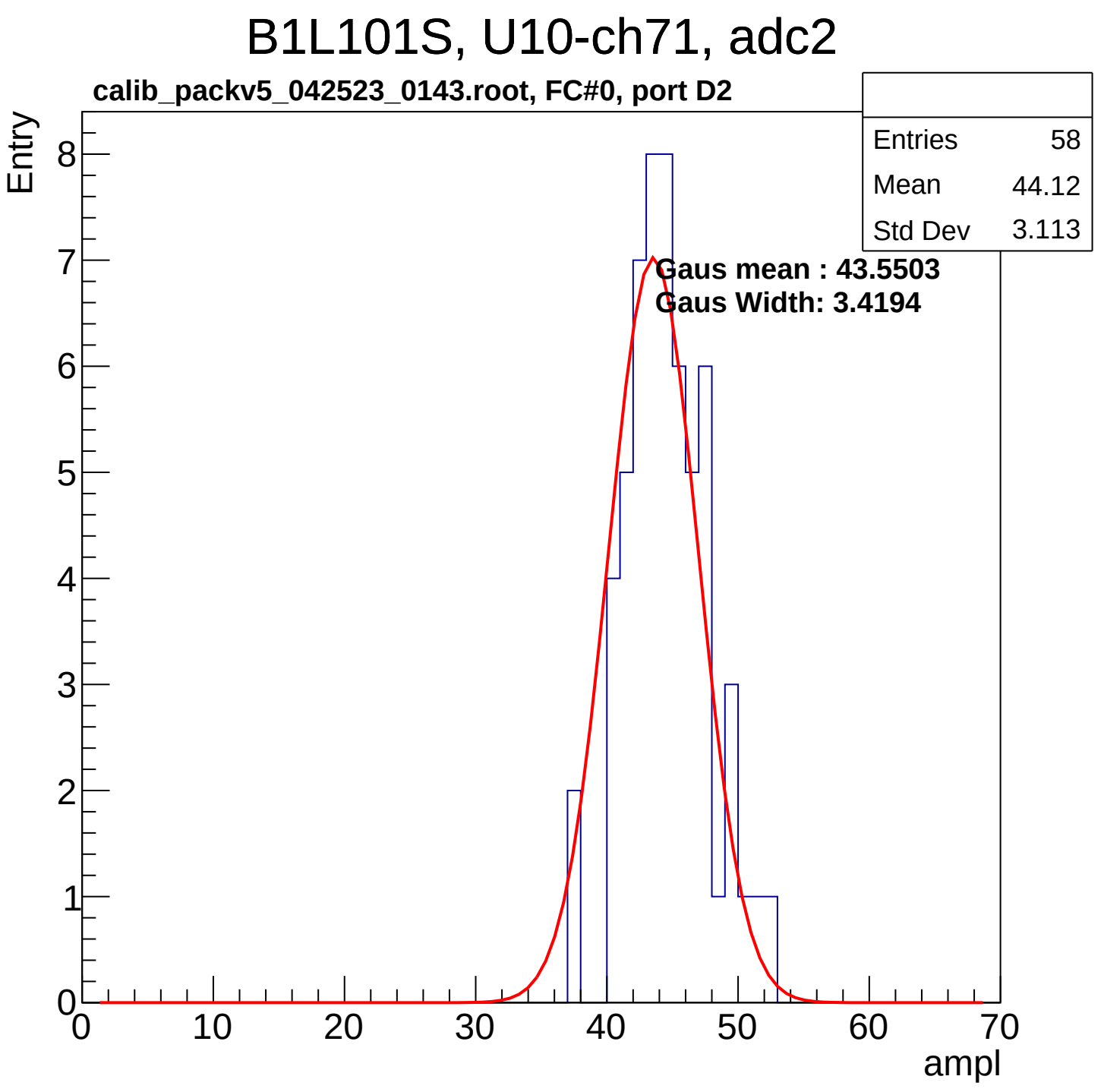
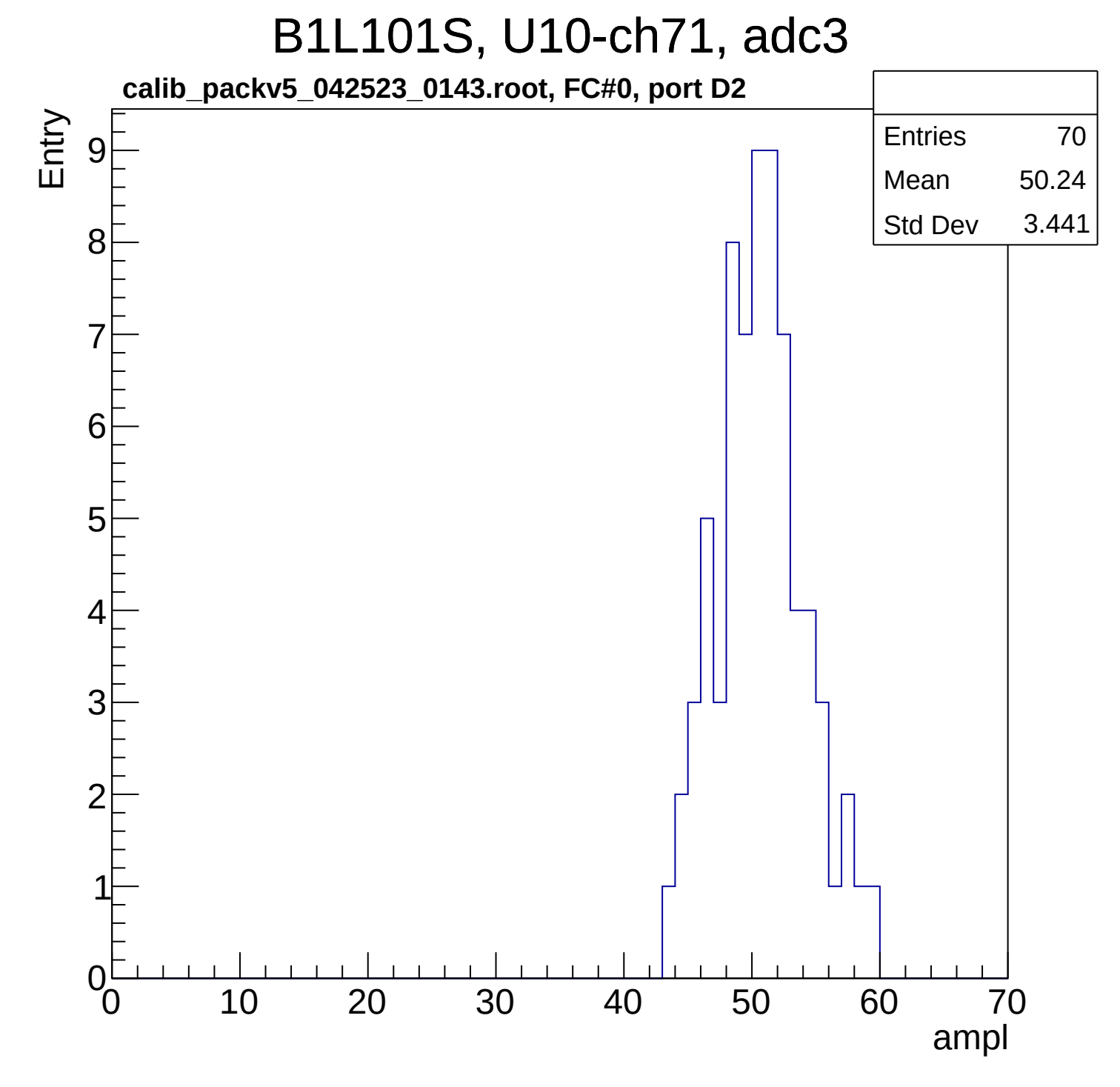

B1L101S, U10-ch71, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 36.67
Std Dev 3.629
Gaus mean : 37.6275
Gaus Width: 3.2444
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch71, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 44.12
Std Dev 3.113
Gaus mean : 43.5503
Gaus Width: 3.4194
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch71, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 50.24
Std Dev 3.441
Entry
ampl
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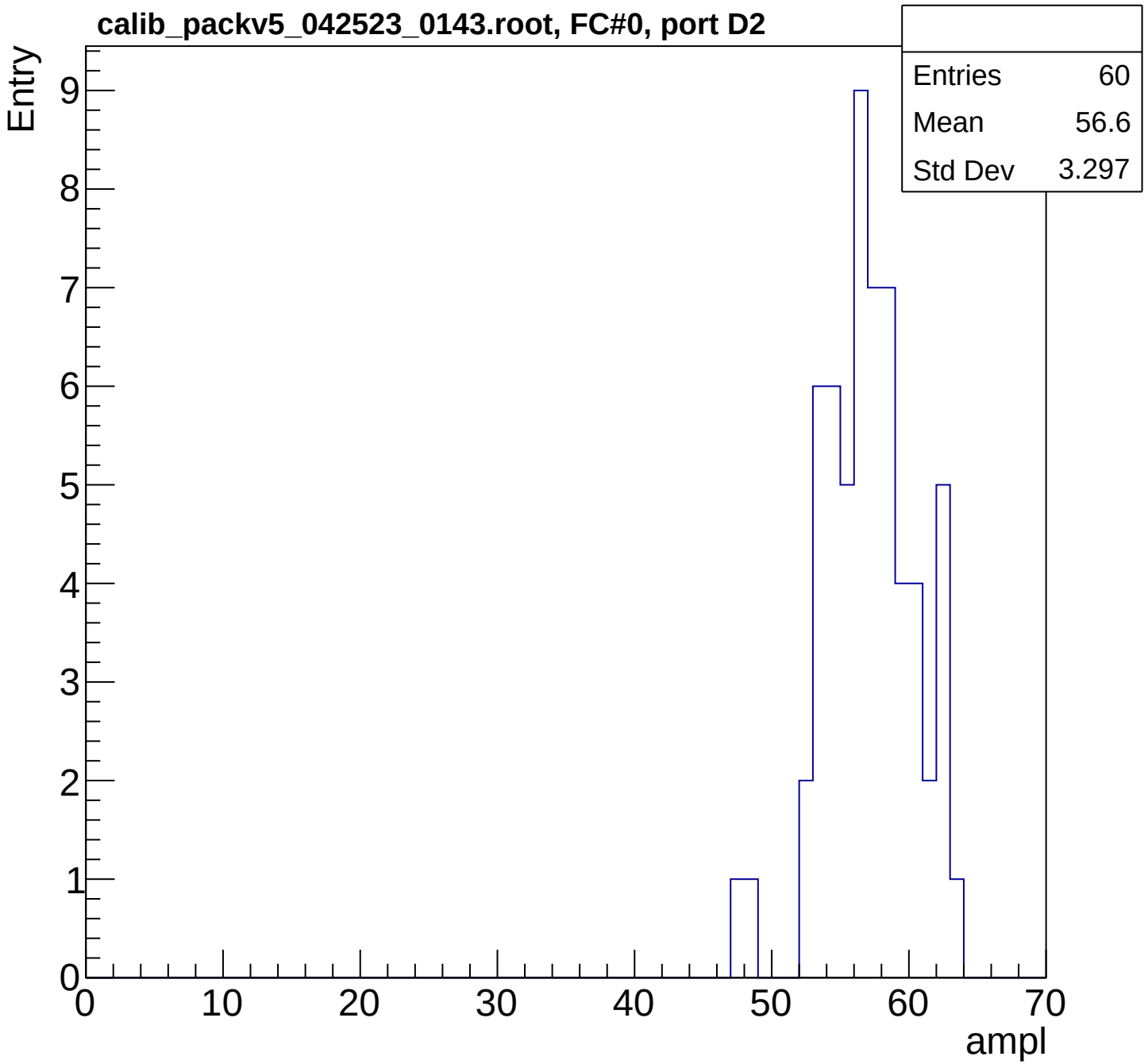
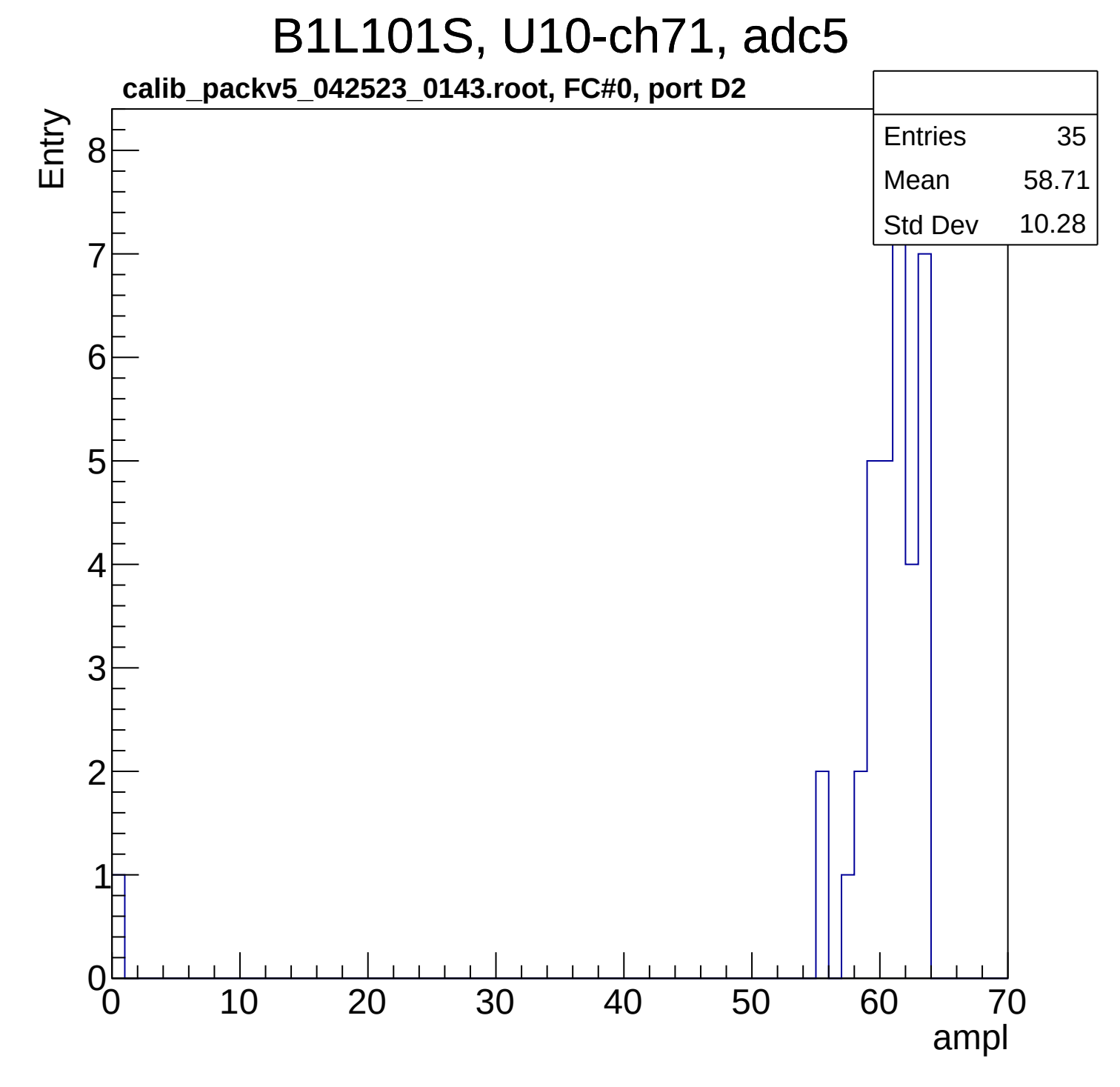
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch71, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 56.6
Std Dev 3.297
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch71, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 35
Mean 58.71
Std Dev 10.28
Entry
ampl
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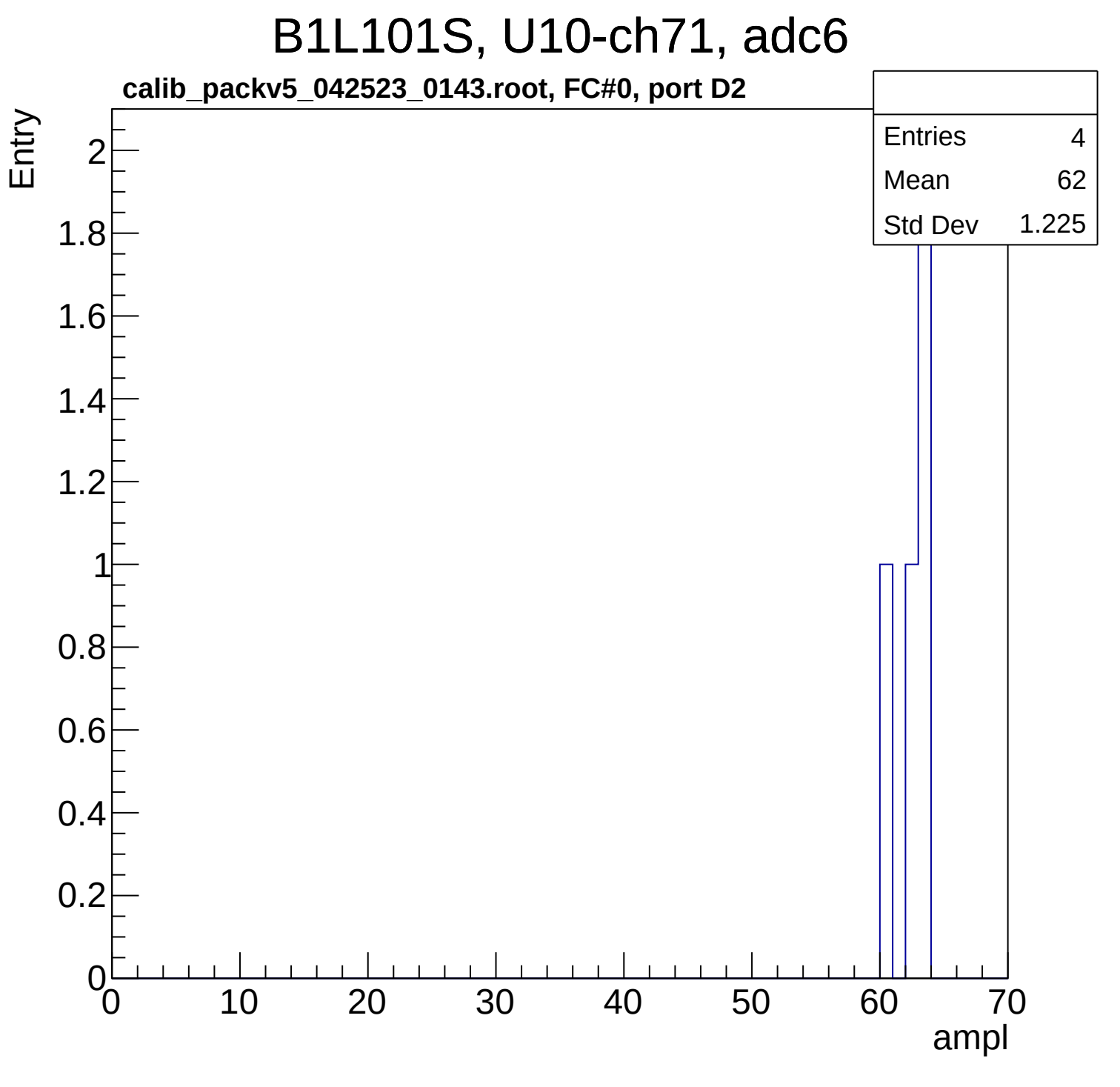
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch71, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 62
Std Dev 1.225
Entry
ampl
0
0.2
0.4
0.6
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1.2
1.4
1.6
1.8
2
0
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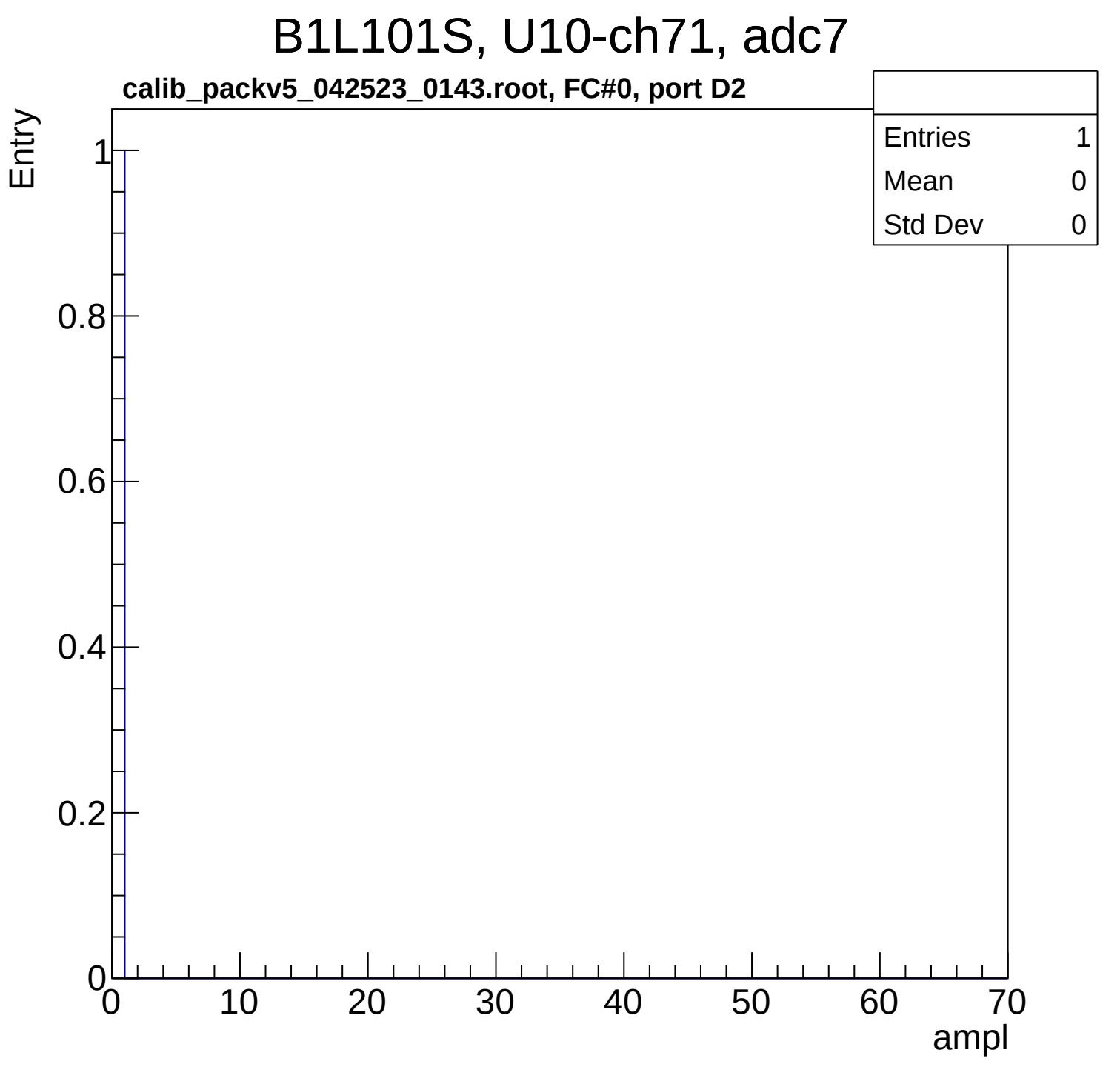
30
40
50
60
70


B1L101S, U10-ch71, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
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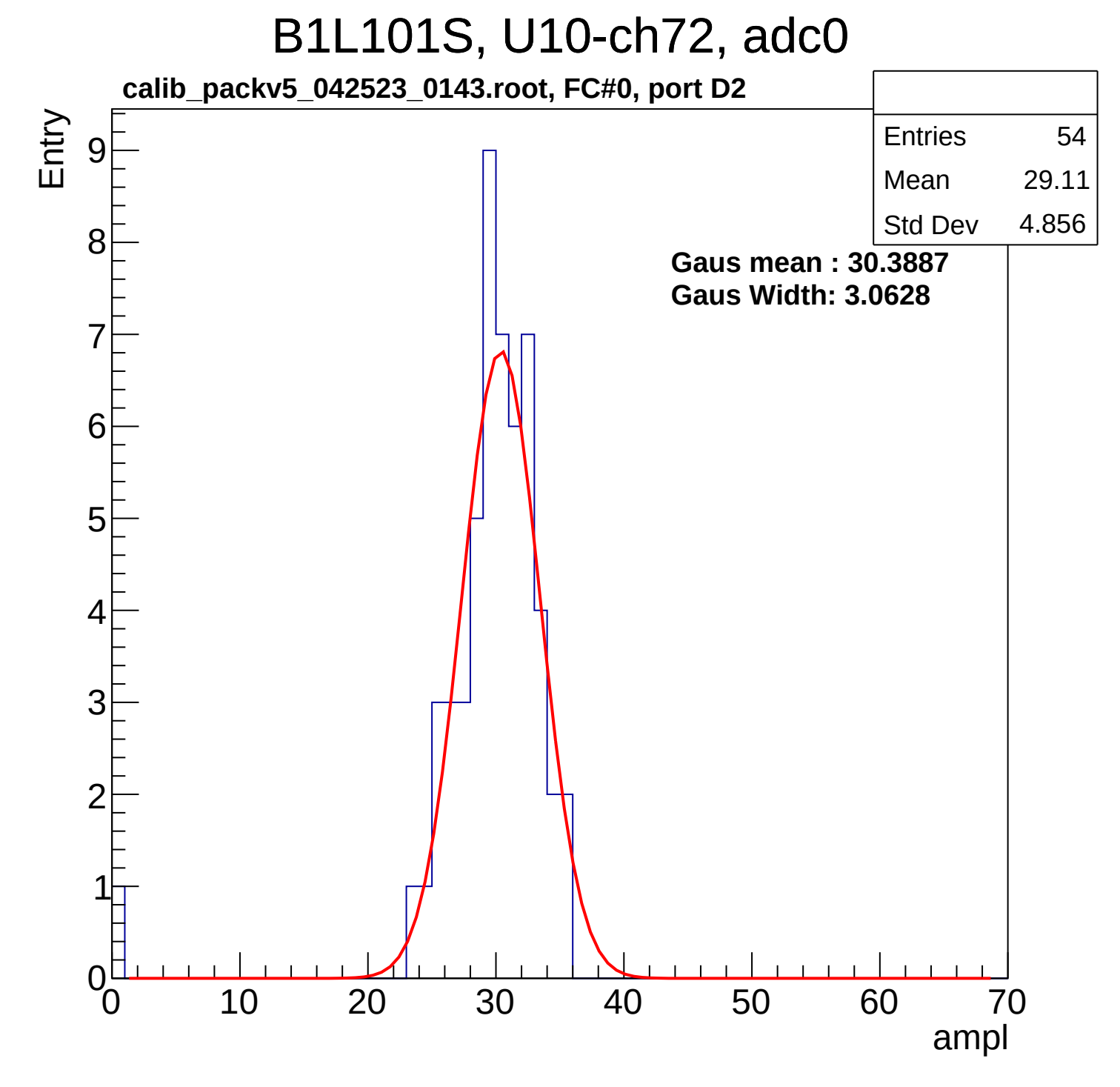
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch72, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 29.11
Std Dev 4.856
Gaus mean : 30.3887
Gaus Width: 3.0628
Entry
ampl
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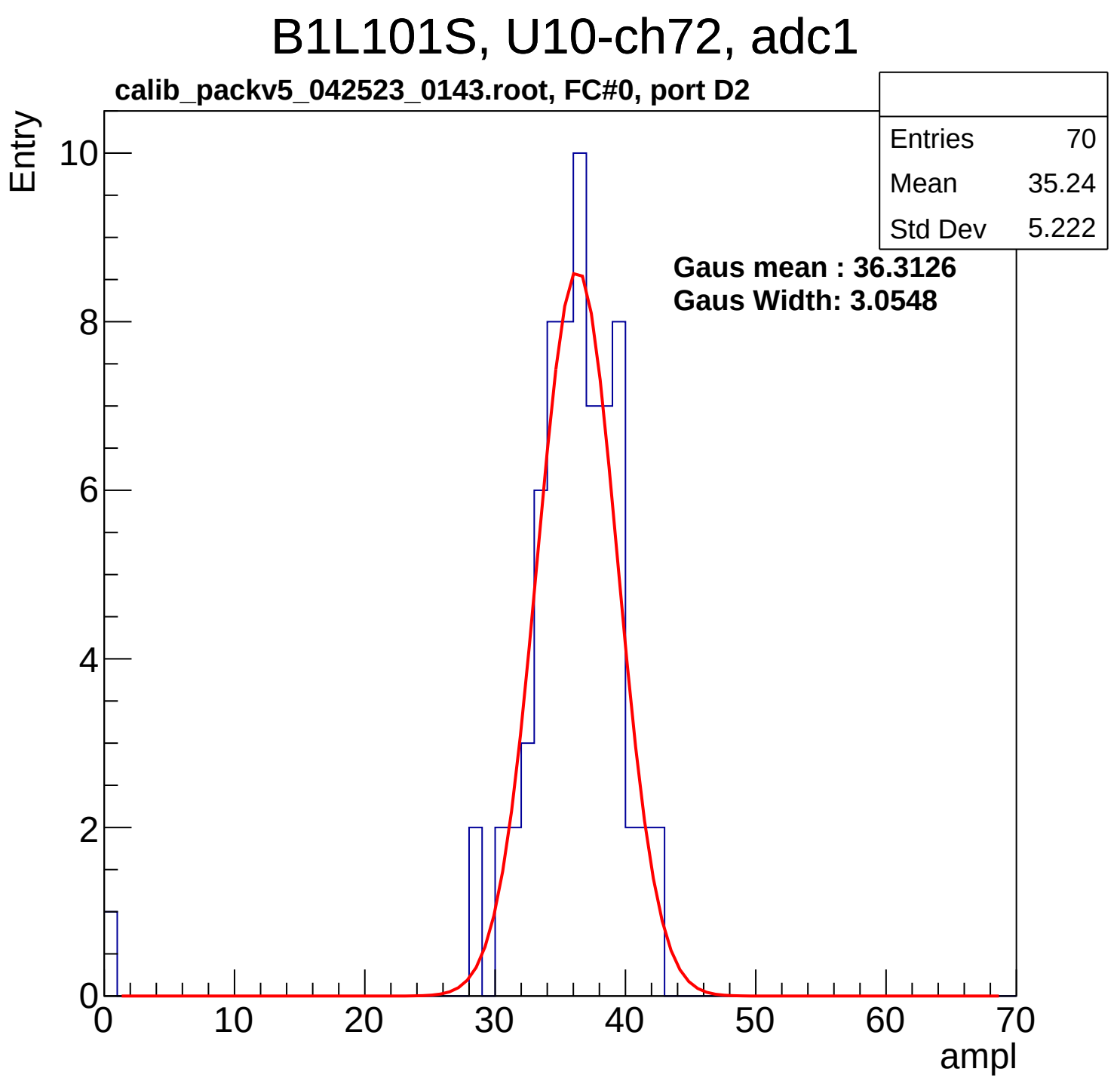
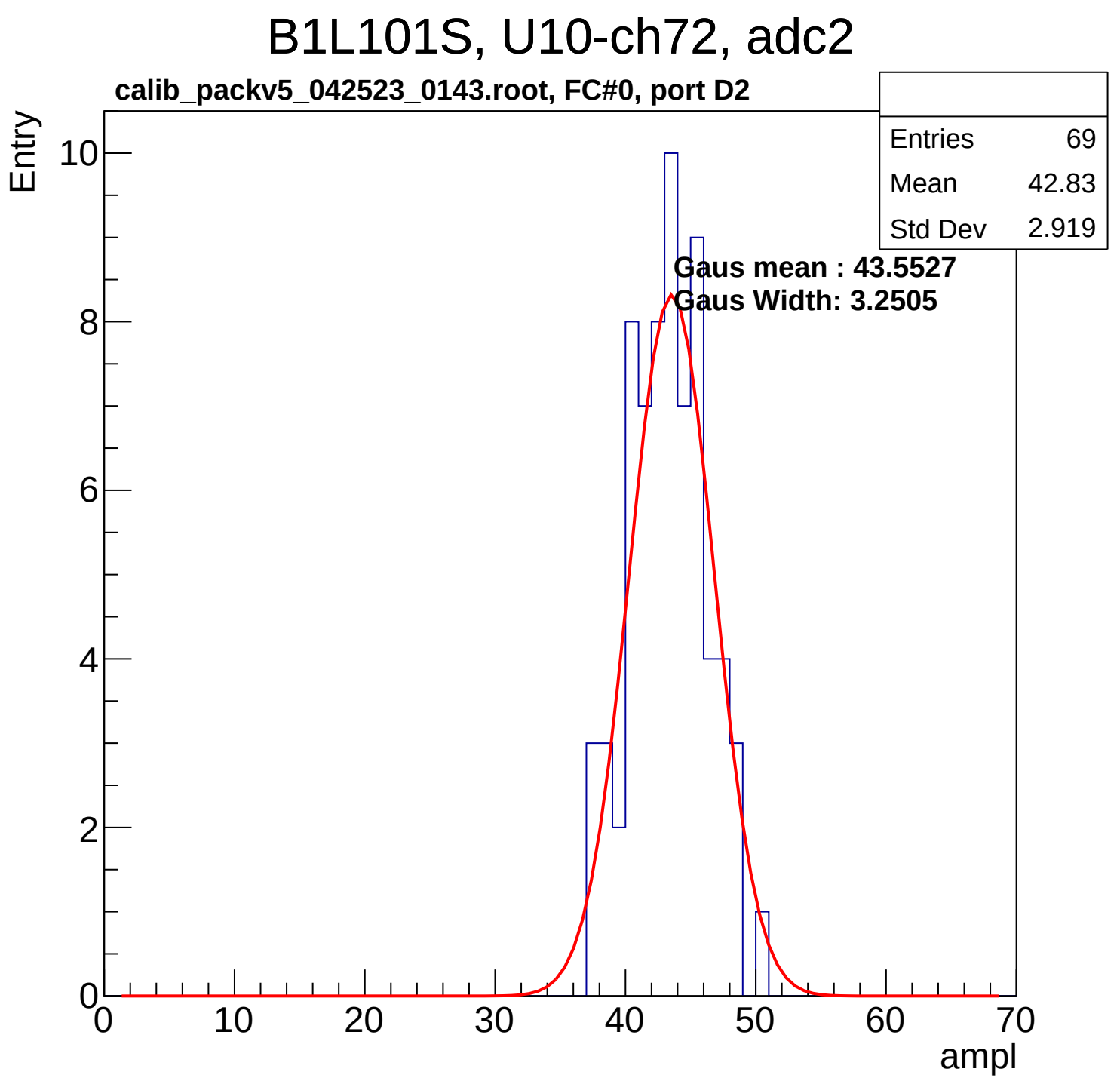
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch72, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 35.24
Std Dev 5.222
Gaus mean : 36.3126
Gaus Width: 3.0548
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch72, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 42.83
Std Dev 2.919
Gaus mean : 43.5527
Gaus Width: 3.2505
Entry
ampl
0
2
4
6
8
10
0
10
20
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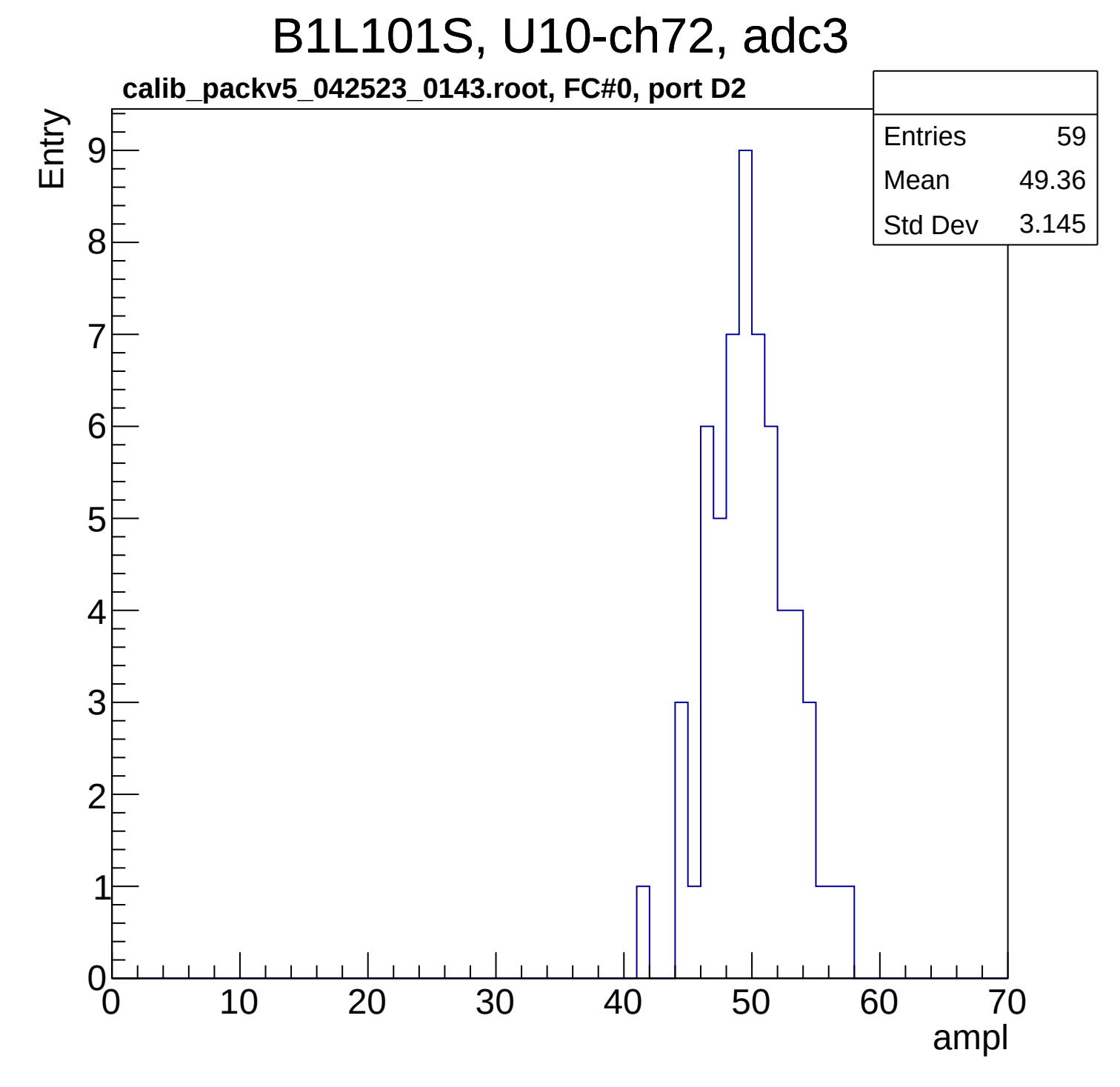
40
50
60
70


B1L101S, U10-ch72, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 49.36
Std Dev 3.145
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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60
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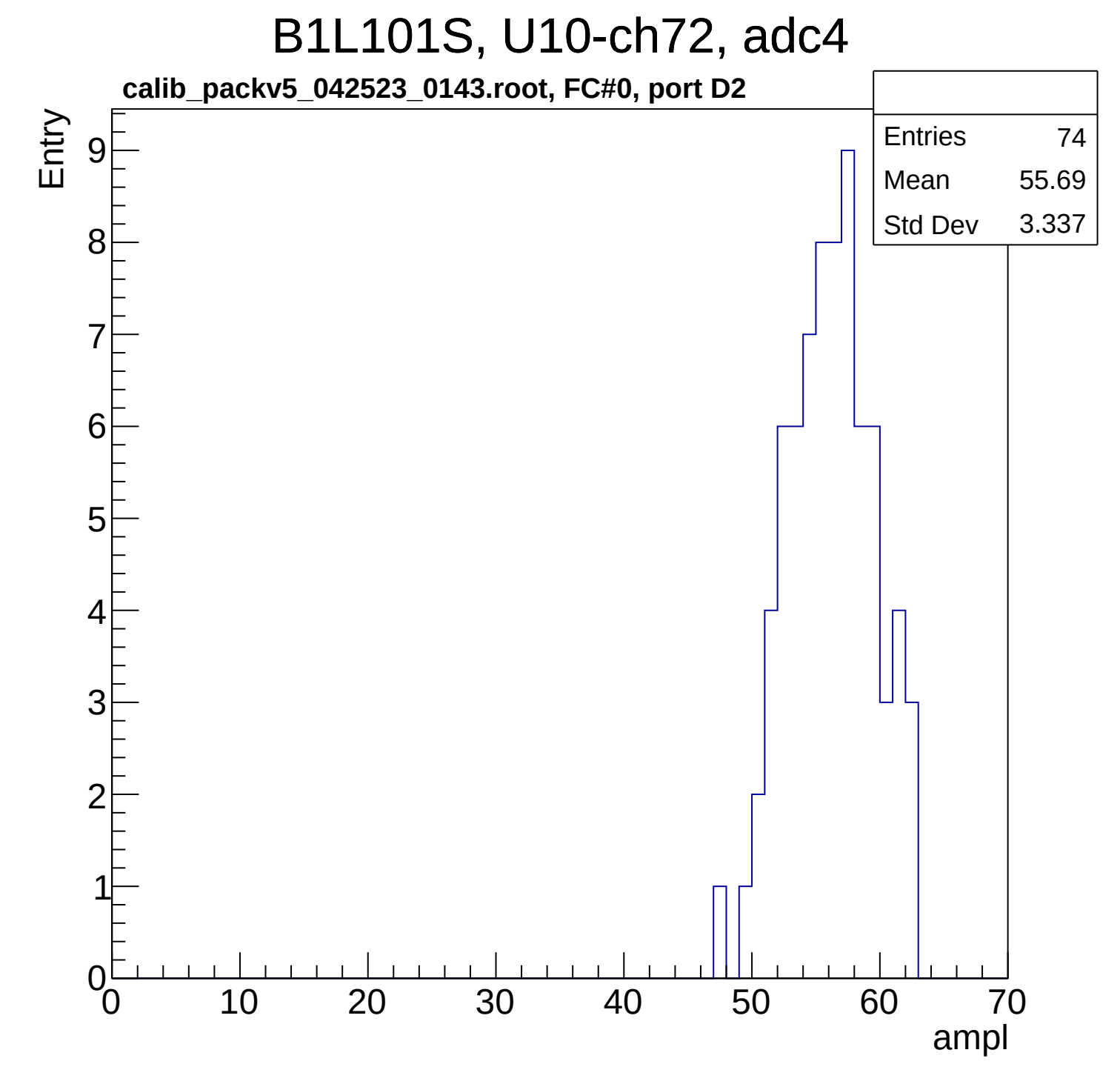
B1L101S, U10-ch72, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 55.69
Std Dev 3.337
Entry
ampl
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2
3
4
5
6
7
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0
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60
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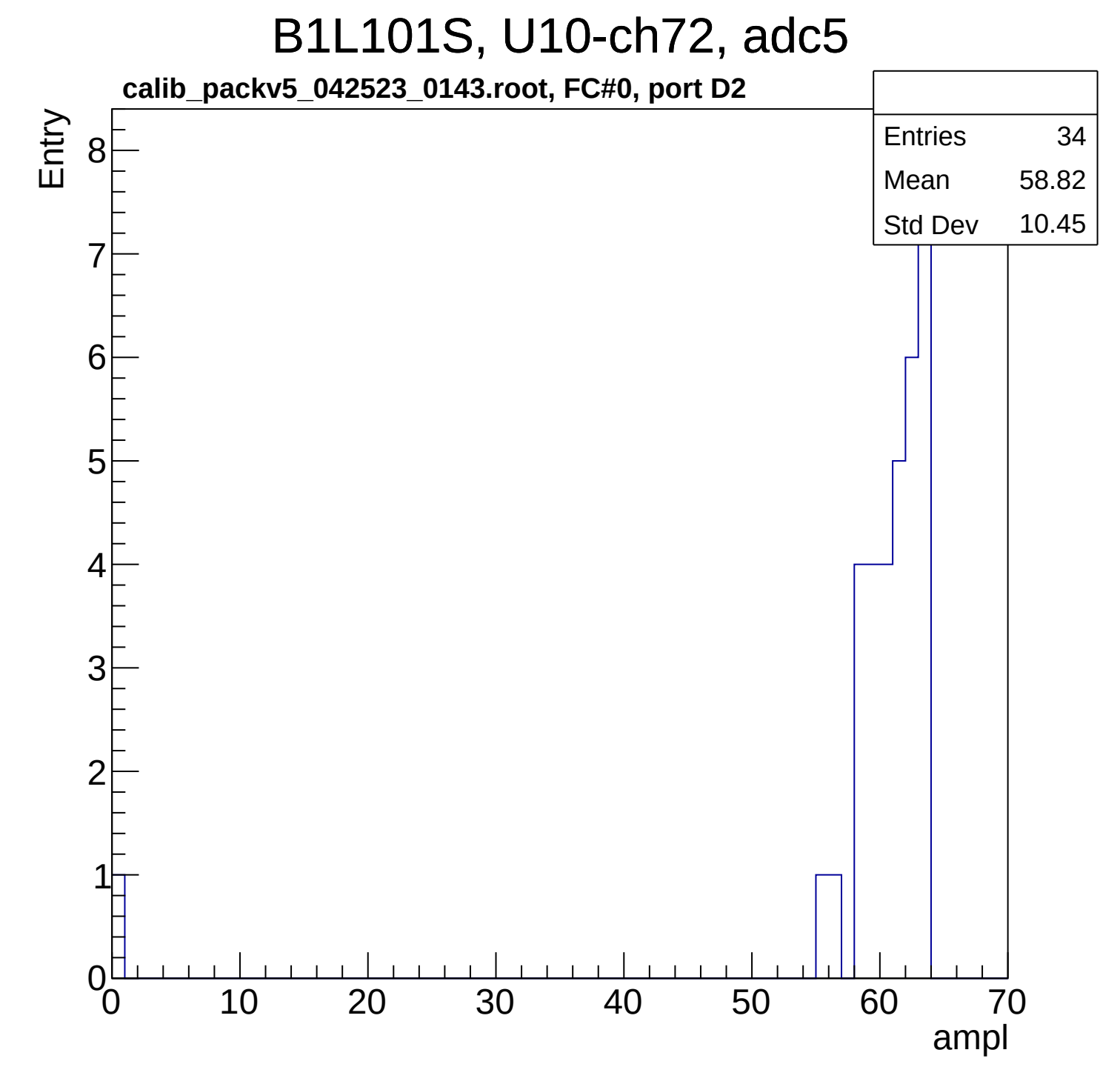
B1L101S, U10-ch72, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 34
Mean 58.82
Std Dev 10.45
Entry
ampl
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1
2
3
4
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6
7
8
0
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40
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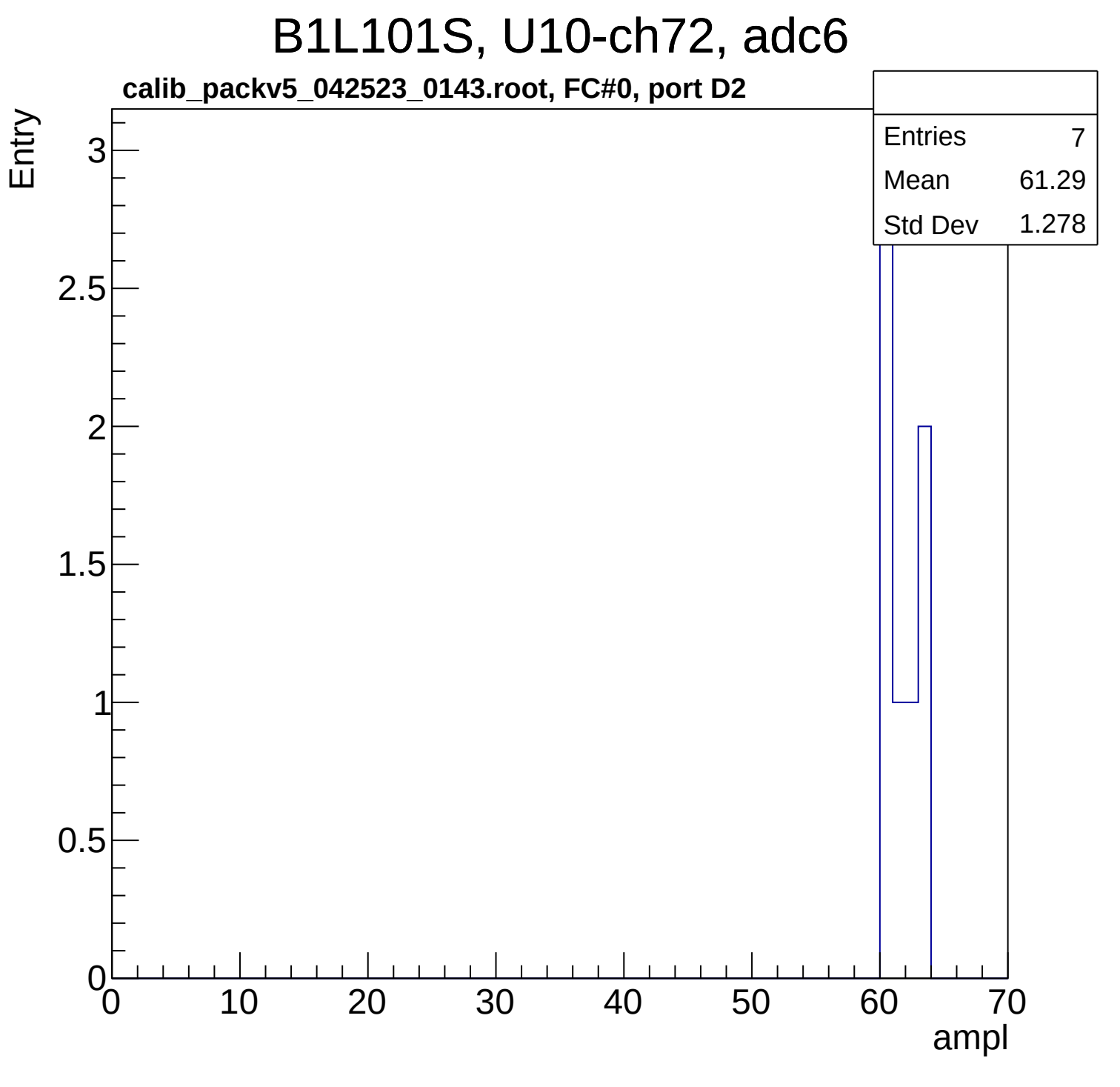
60
70


B1L101S, U10-ch72, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 61.29
Std Dev 1.278
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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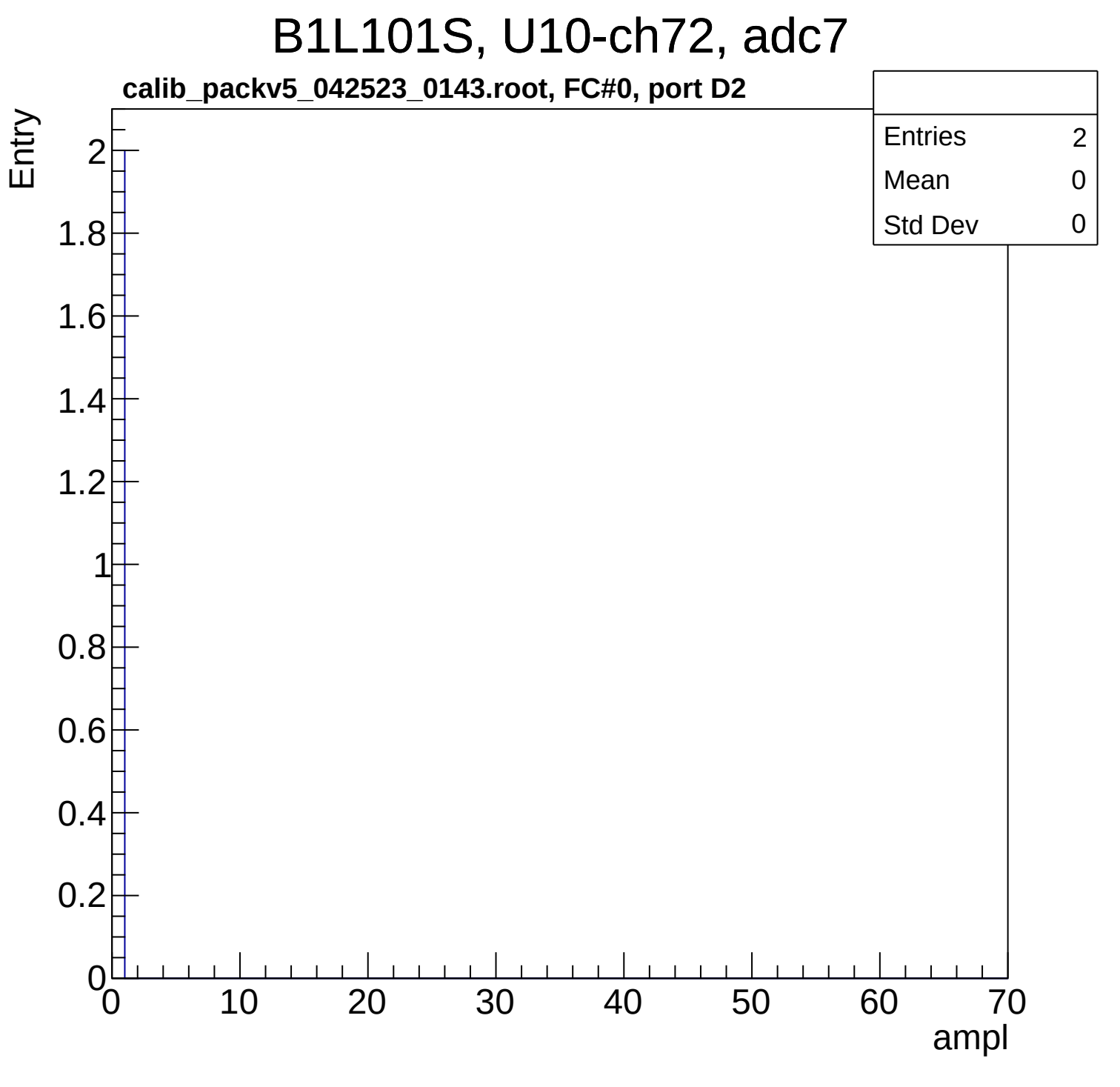
20
30
40
50
60
70


B1L101S, U10-ch72, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
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1.2
1.4
1.6
1.8
2
0
10
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40
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60
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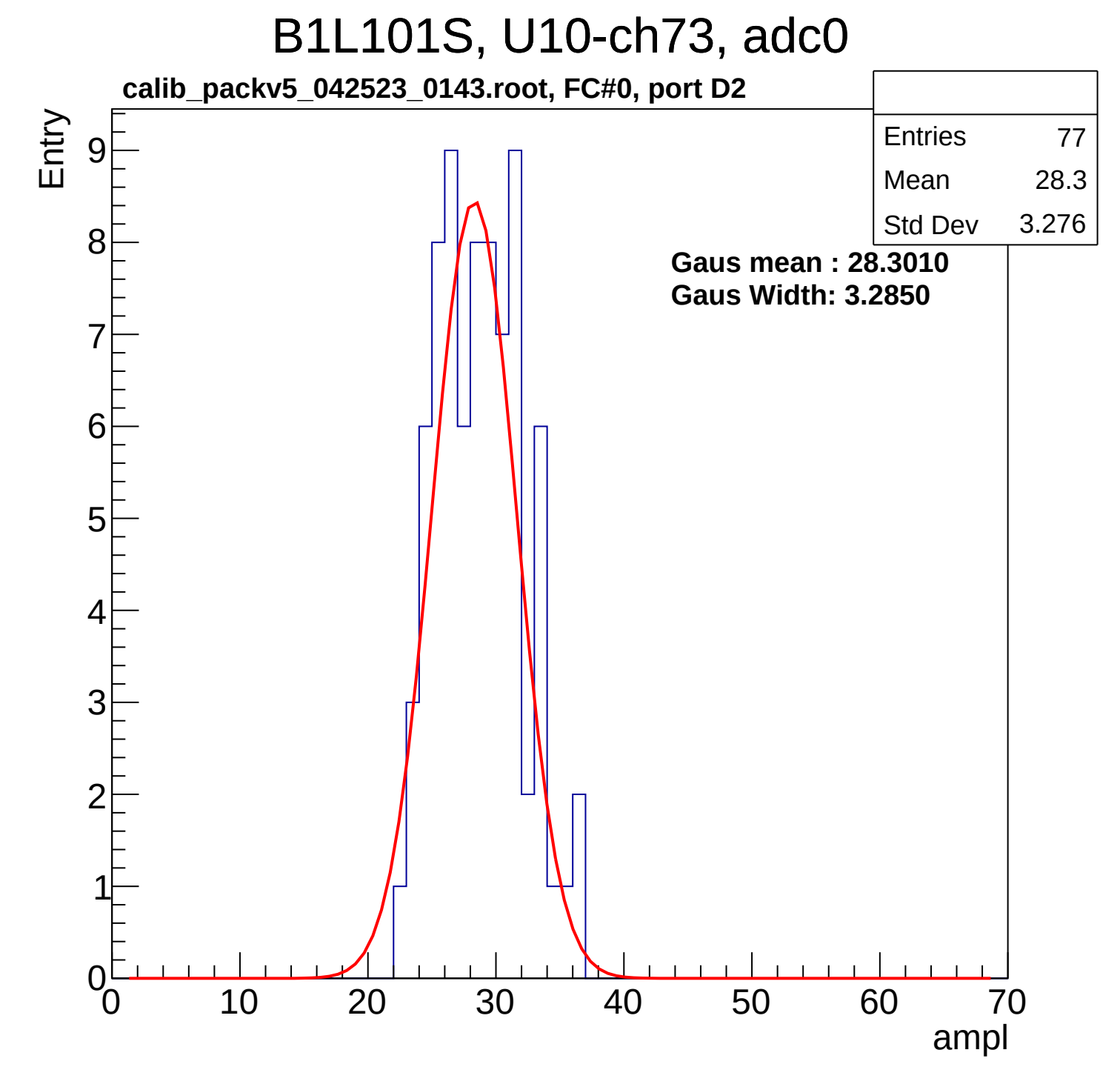
B1L101S, U10-ch73, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 28.3
Std Dev 3.276
Gaus mean : 28.3010
Gaus Width: 3.2850
Entry
ampl
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2
3
4
5
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7
8
9
0
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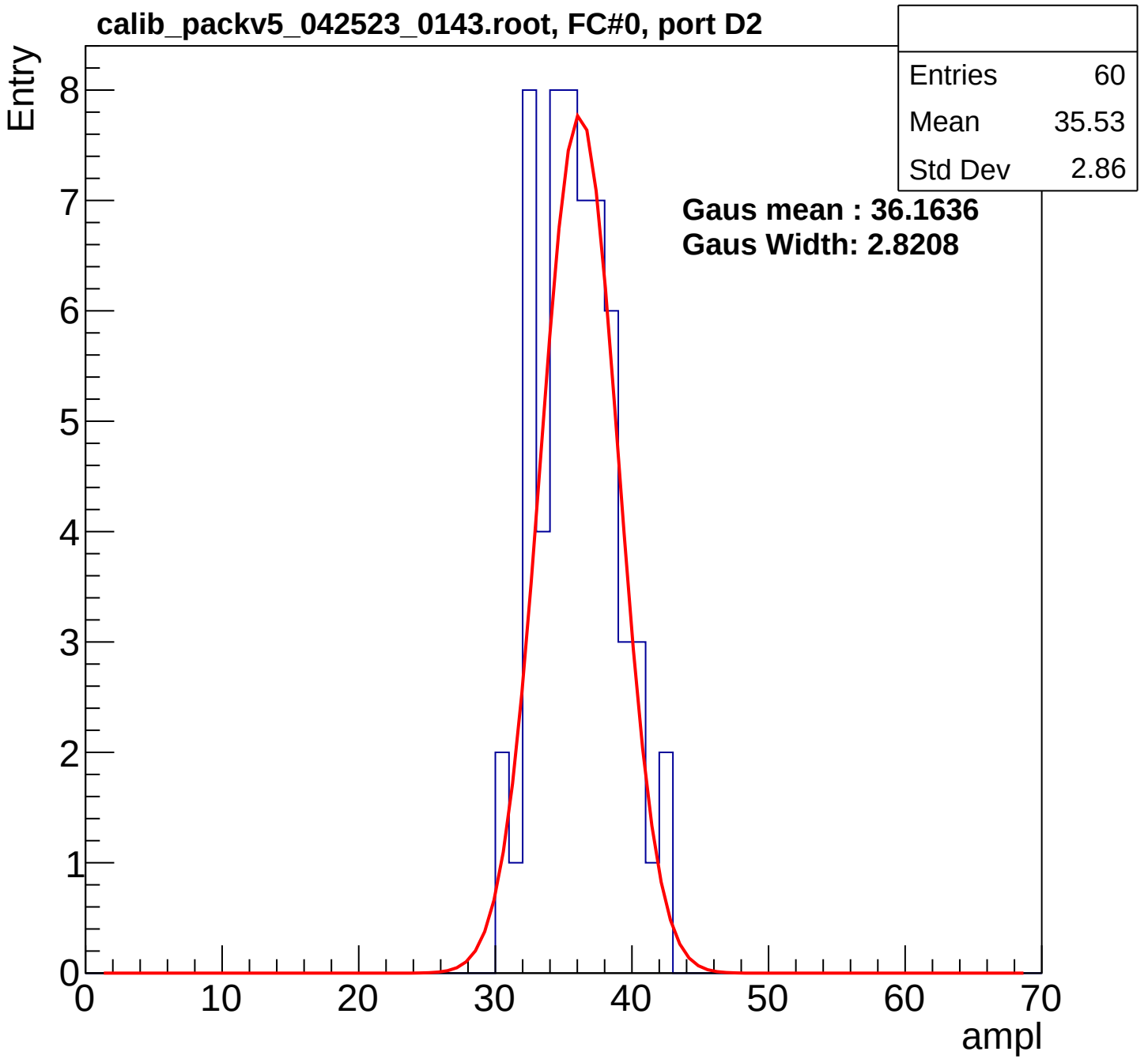
B1L101S, U10-ch73, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 35.53
Std Dev 2.86
Gaus mean : 36.1636
Gaus Width: 2.8208
Entry
ampl
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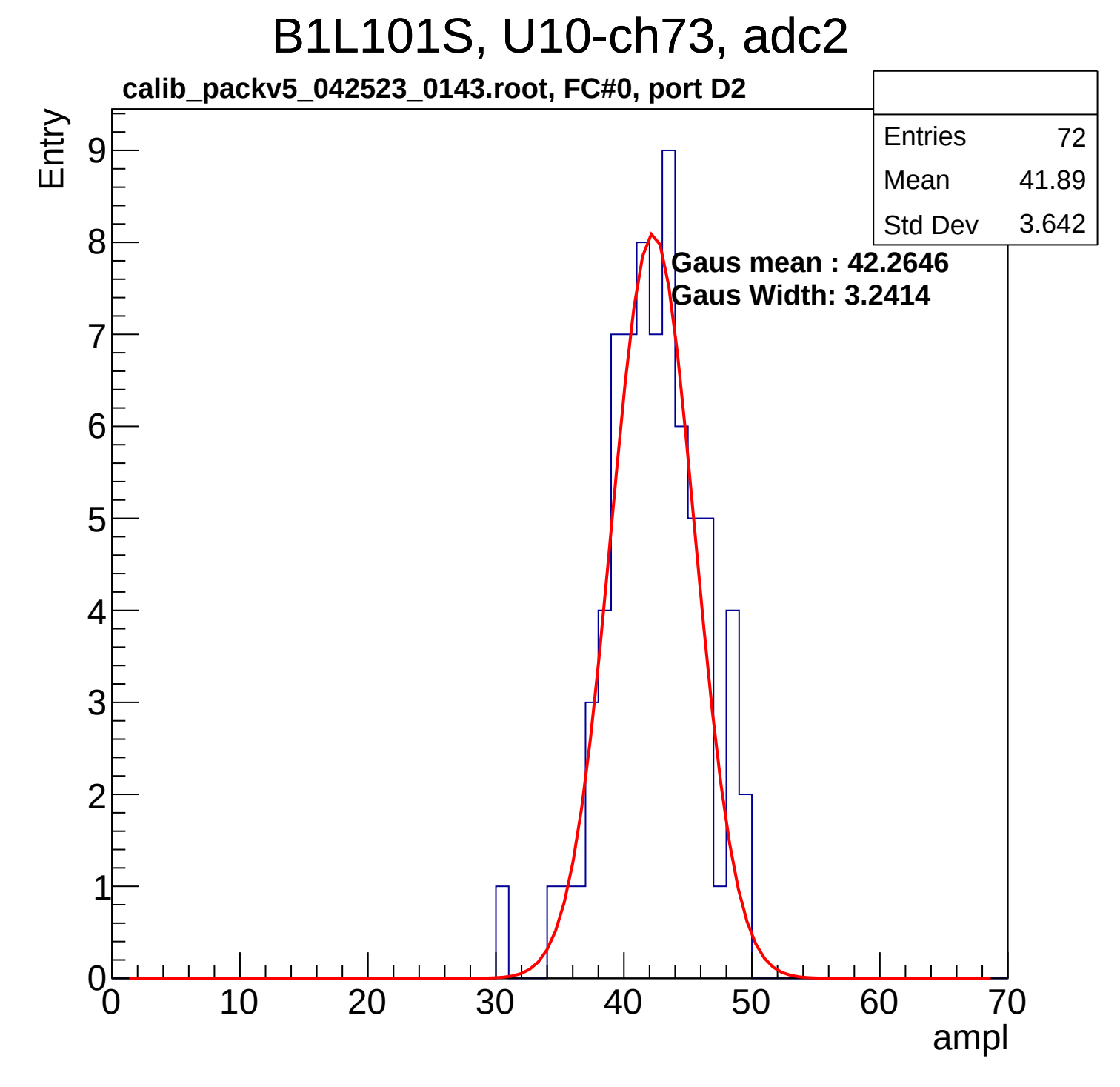
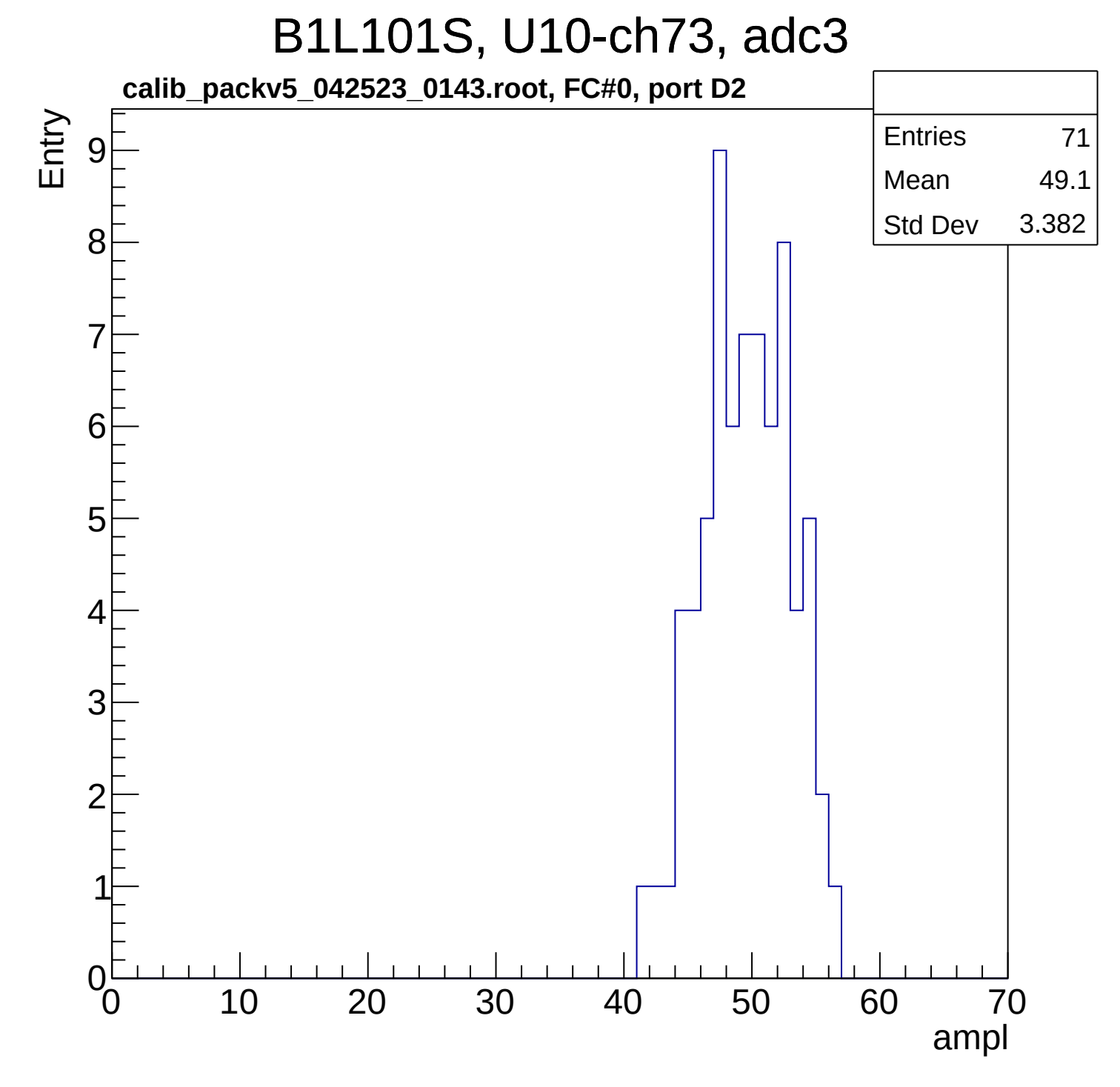
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch73, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 41.89
Std Dev 3.642
Gaus mean : 42.2646
Gaus Width: 3.2414
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch73, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 49.1
Std Dev 3.382
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
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60
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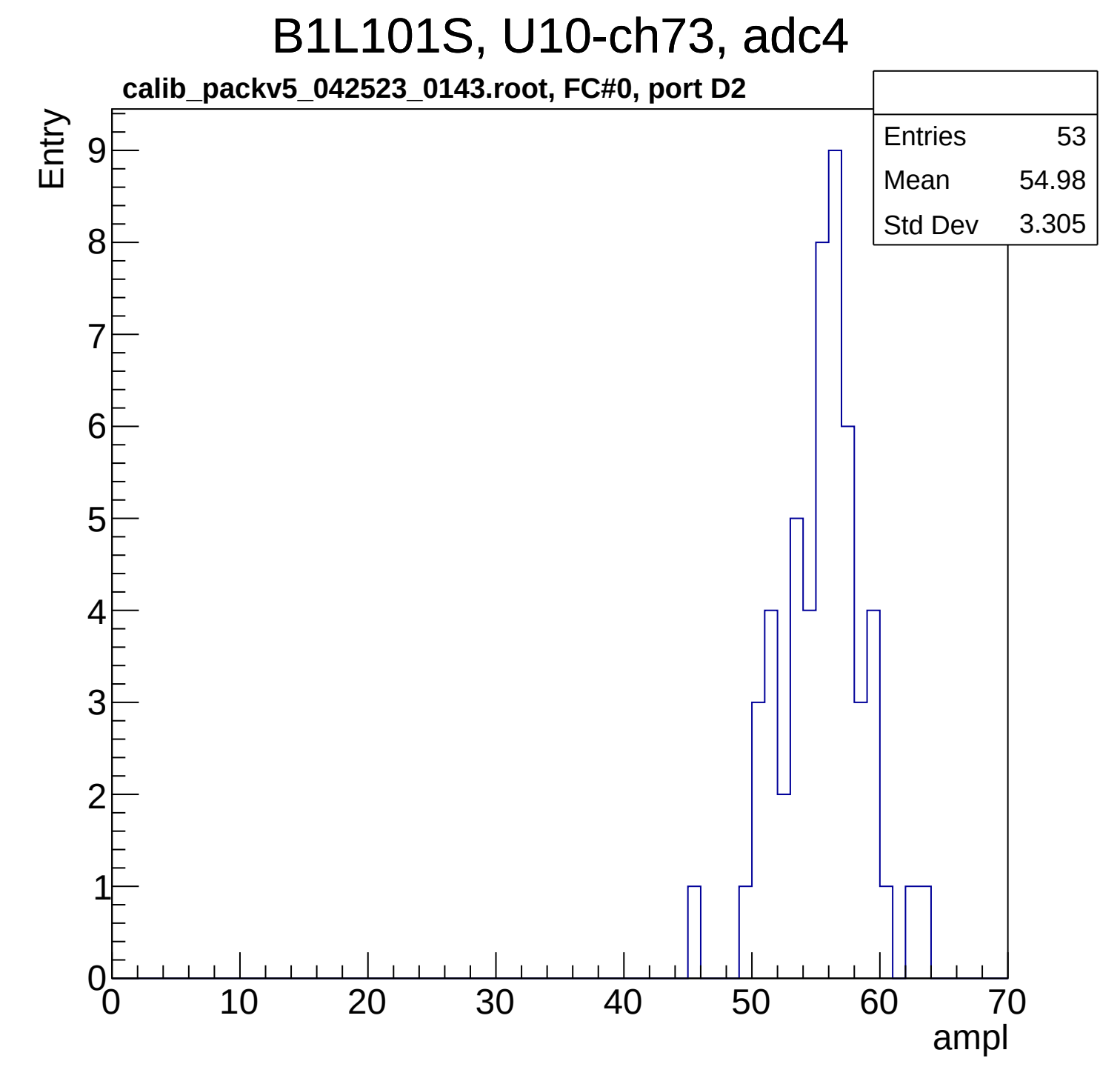
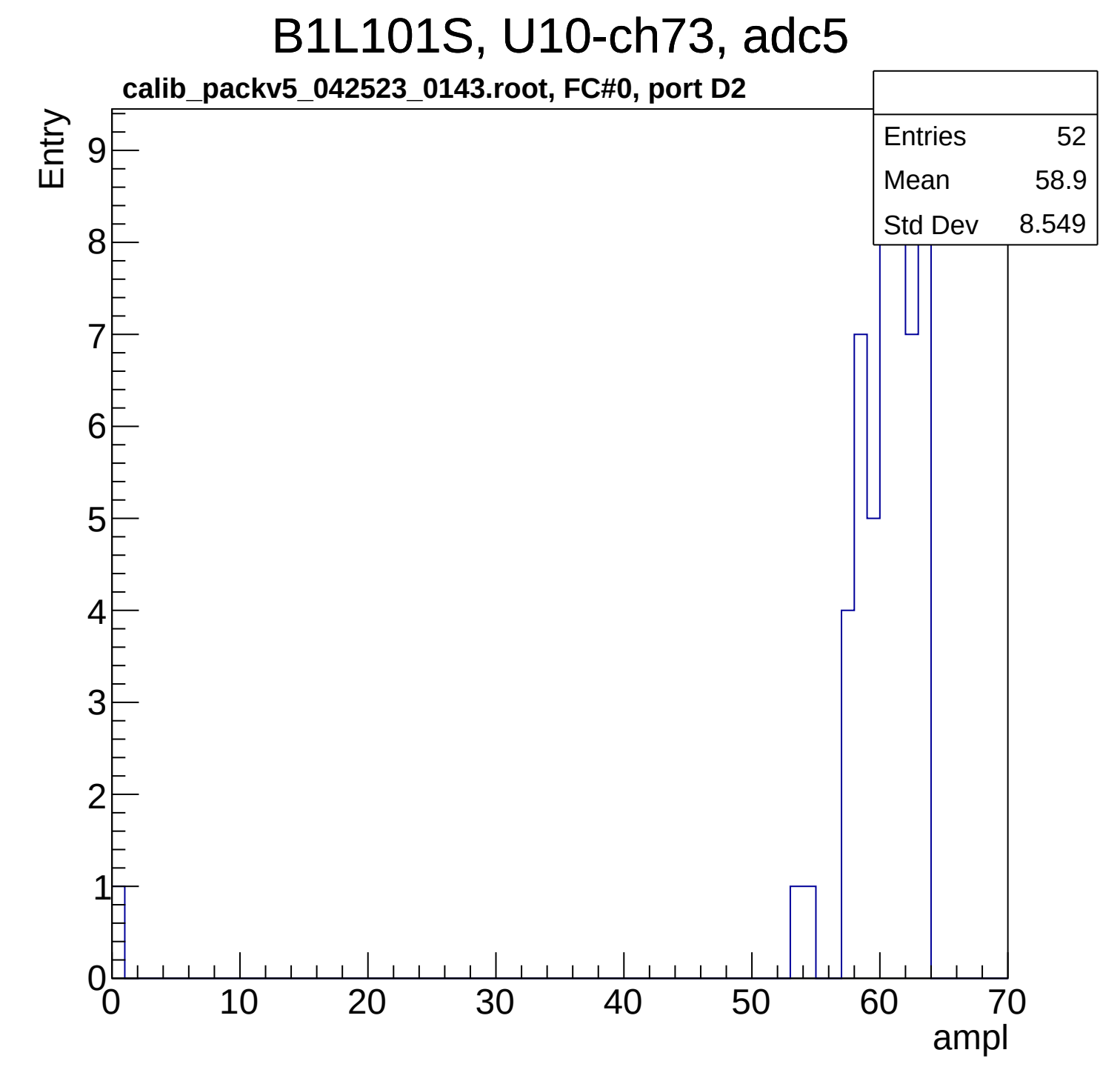
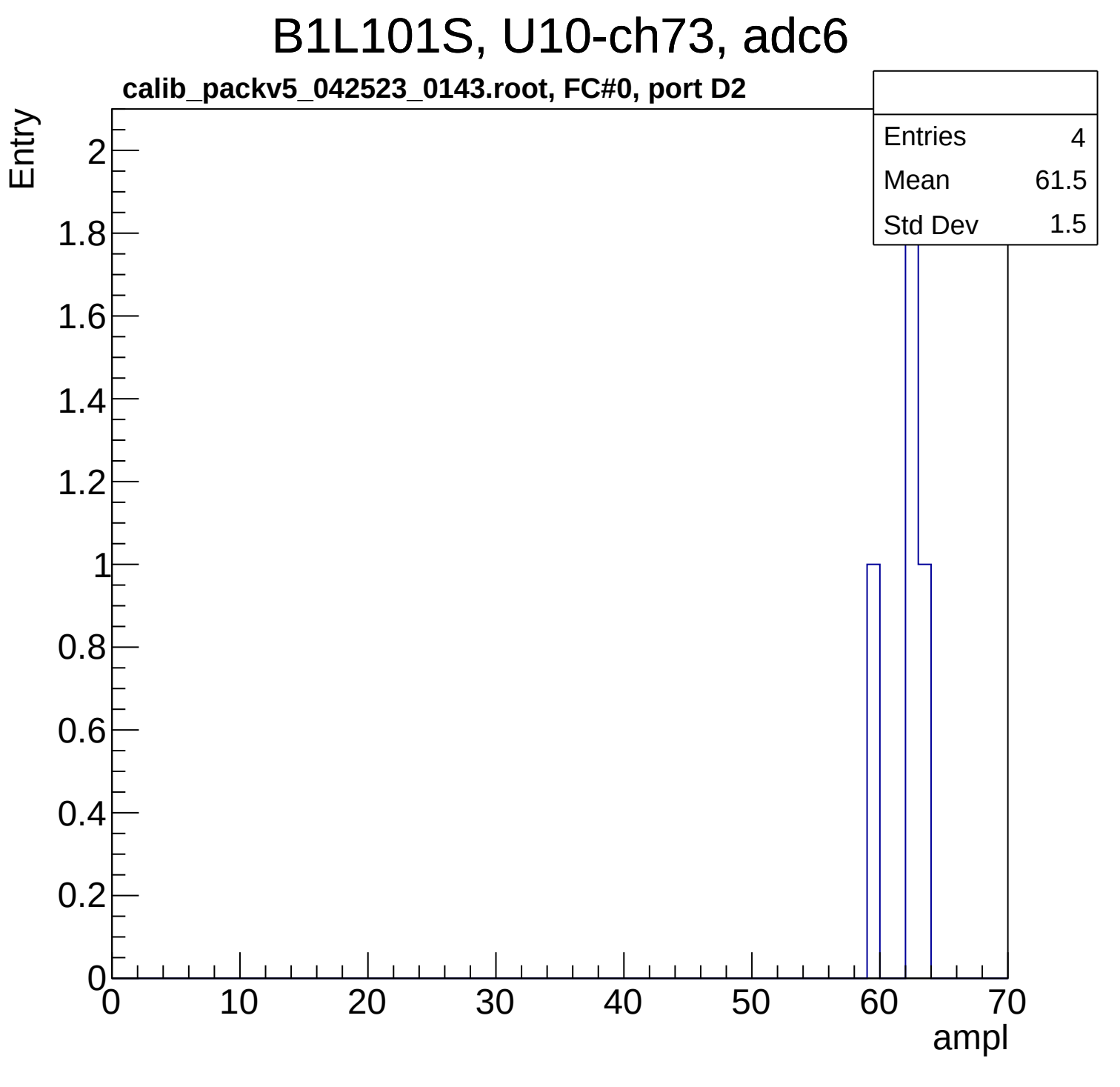
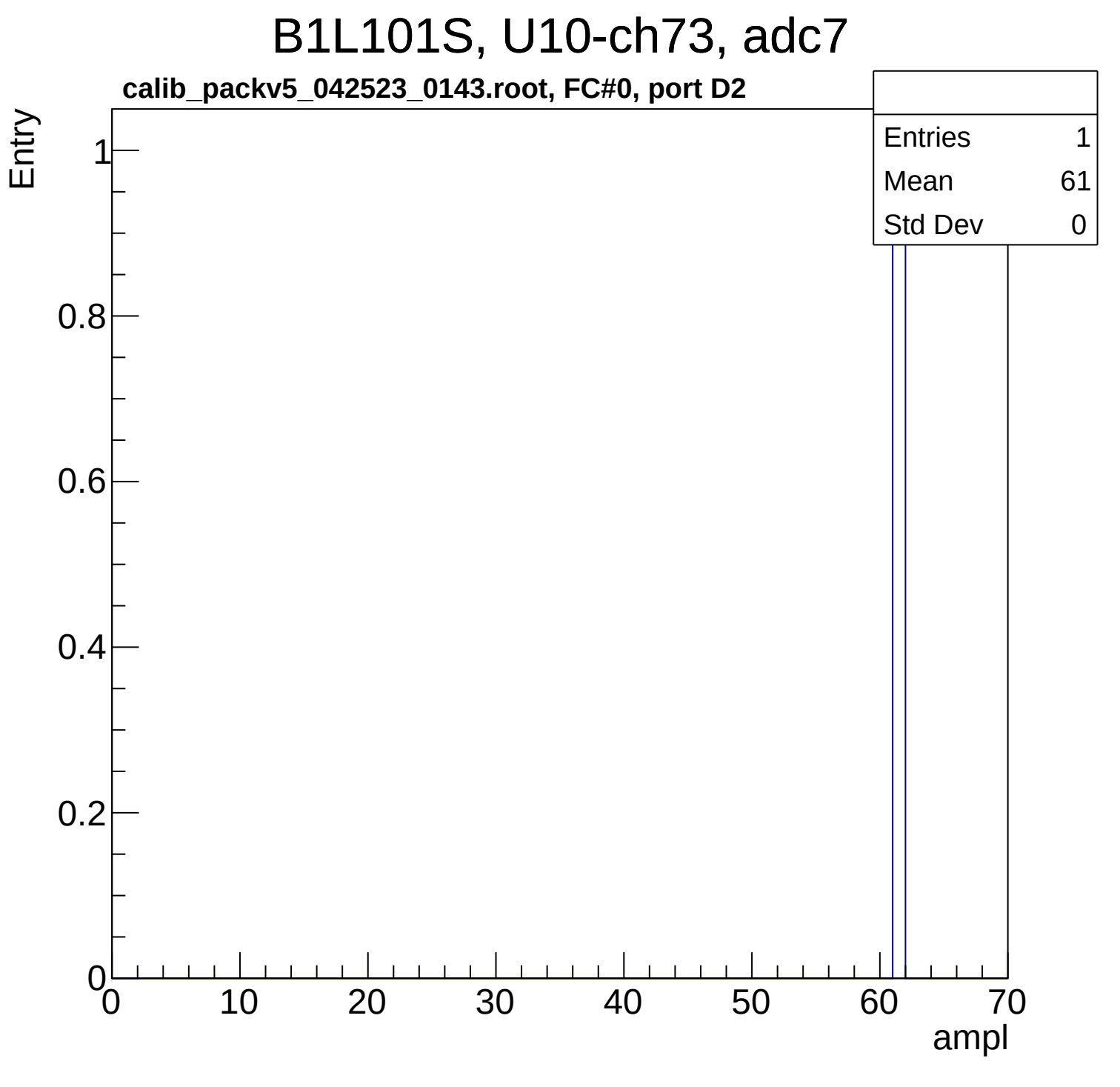
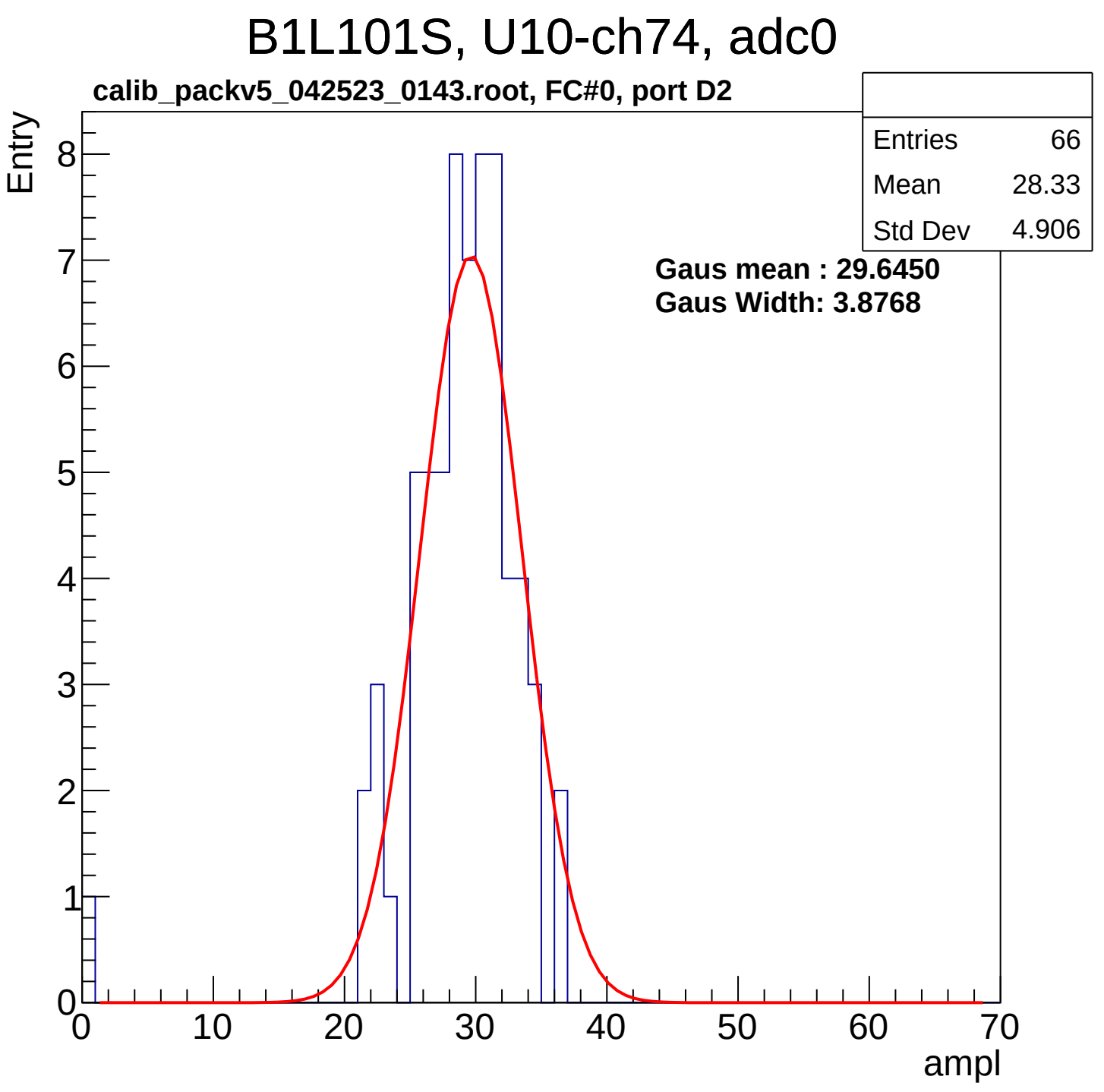
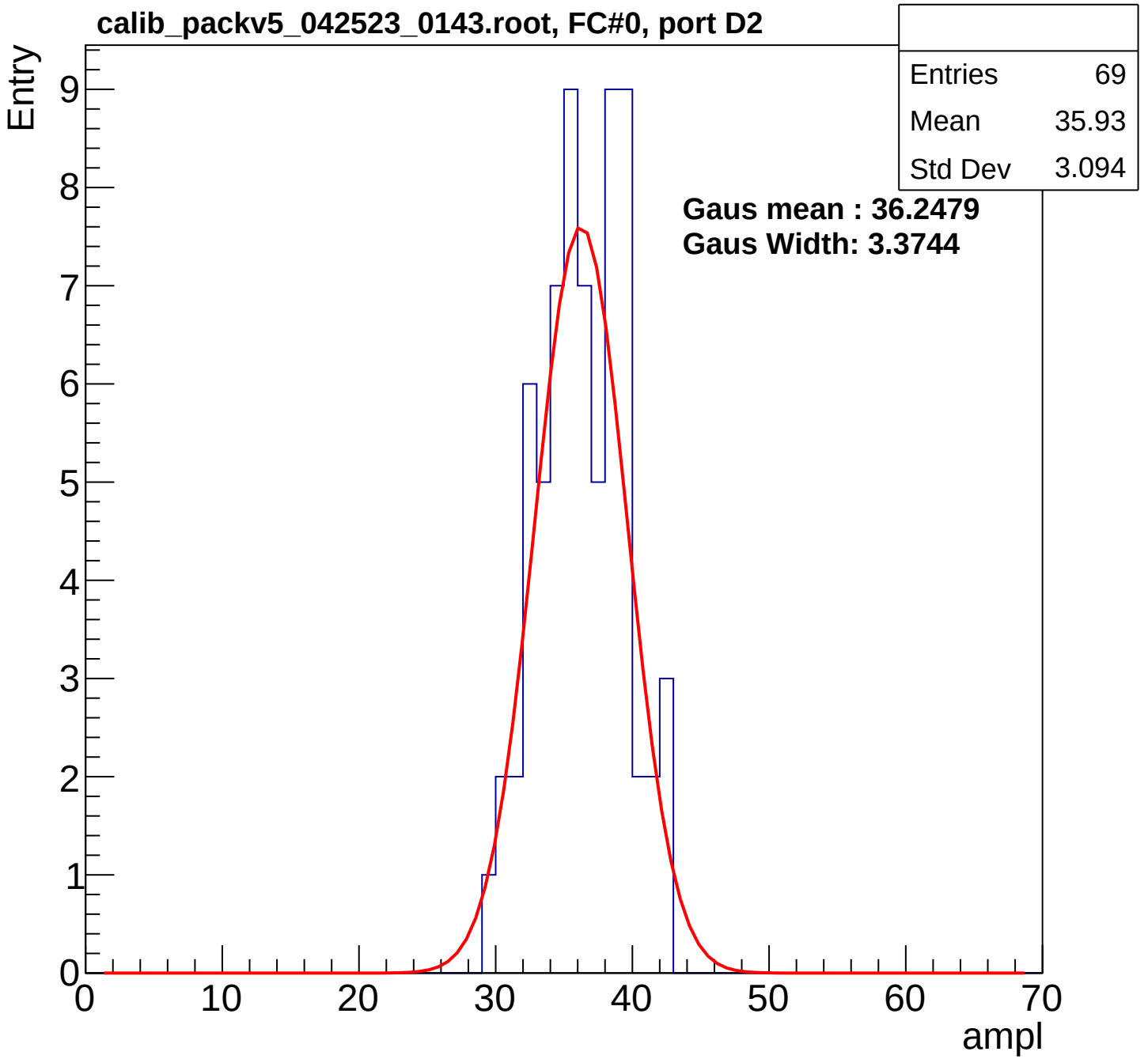

B1L101S, U10-ch73, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 54.98
Std Dev 3.305
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch73, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 58.9
Std Dev 8.549
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch73, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 61.5
Std Dev 1.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U10-ch73, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 61
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch74, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 28.33
Std Dev 4.906
Gaus mean : 29.6450
Gaus Width: 3.8768
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch74, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 35.93
Std Dev 3.094
Gaus mean : 36.2479
Gaus Width: 3.3744
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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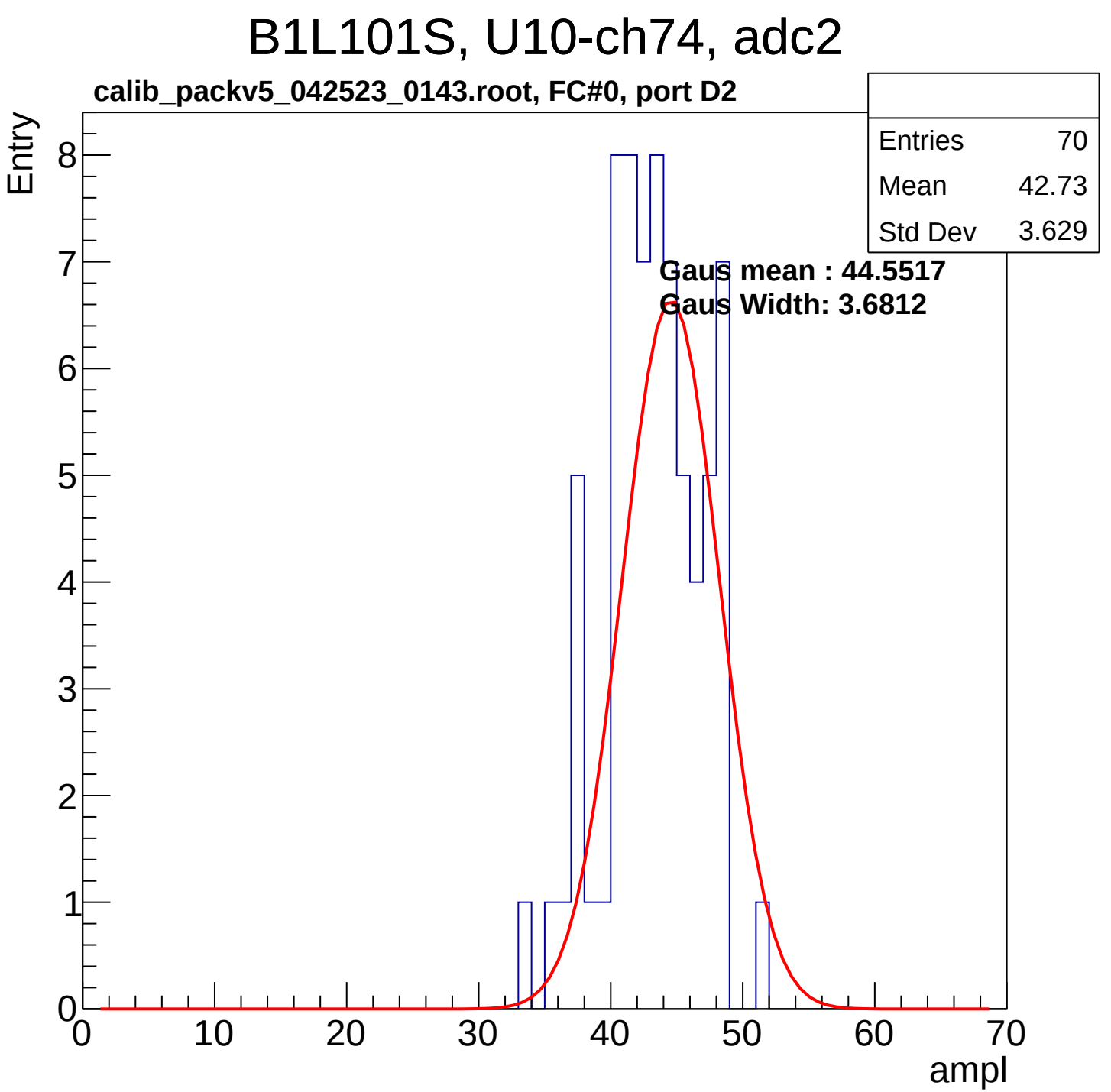
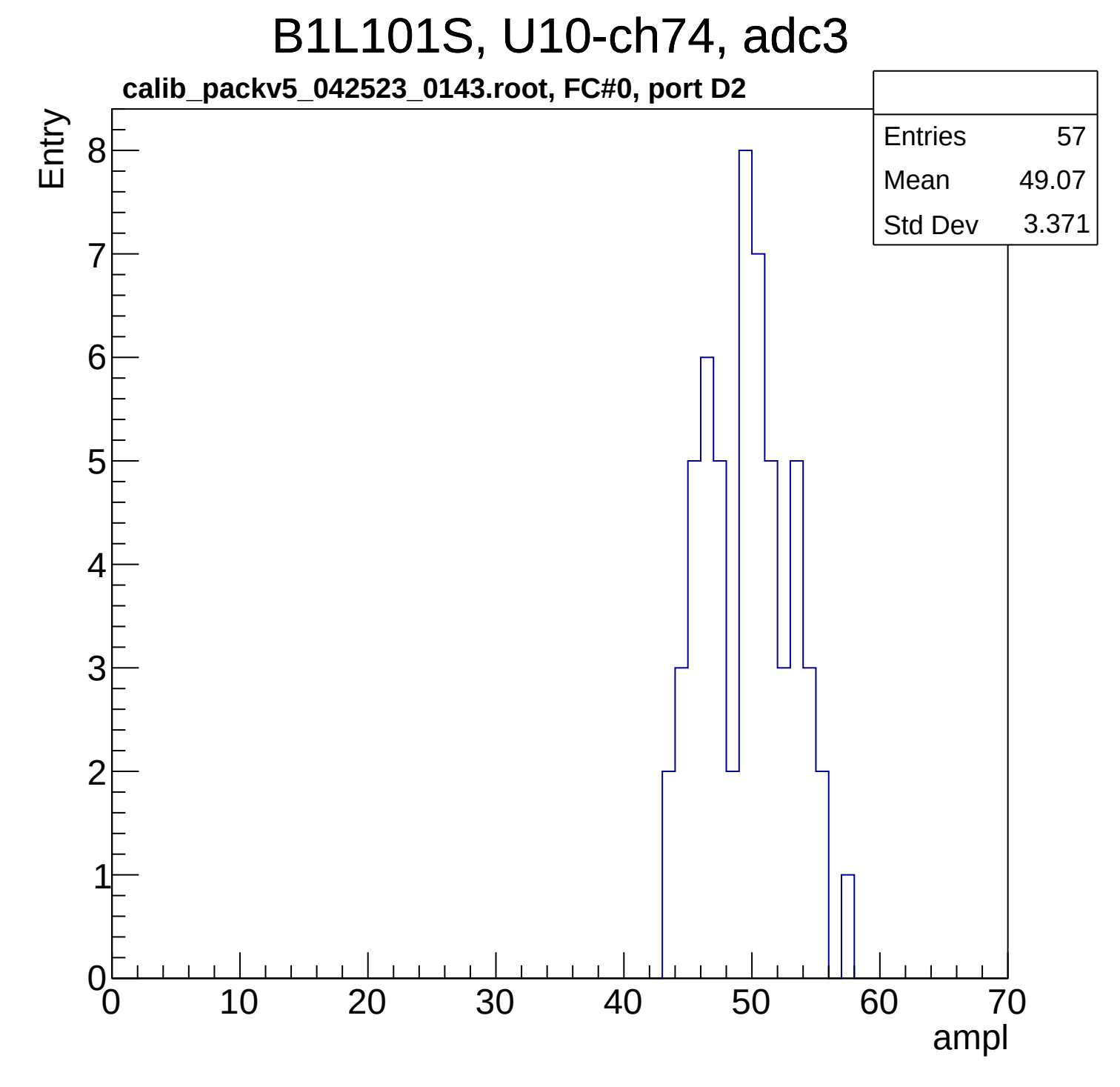
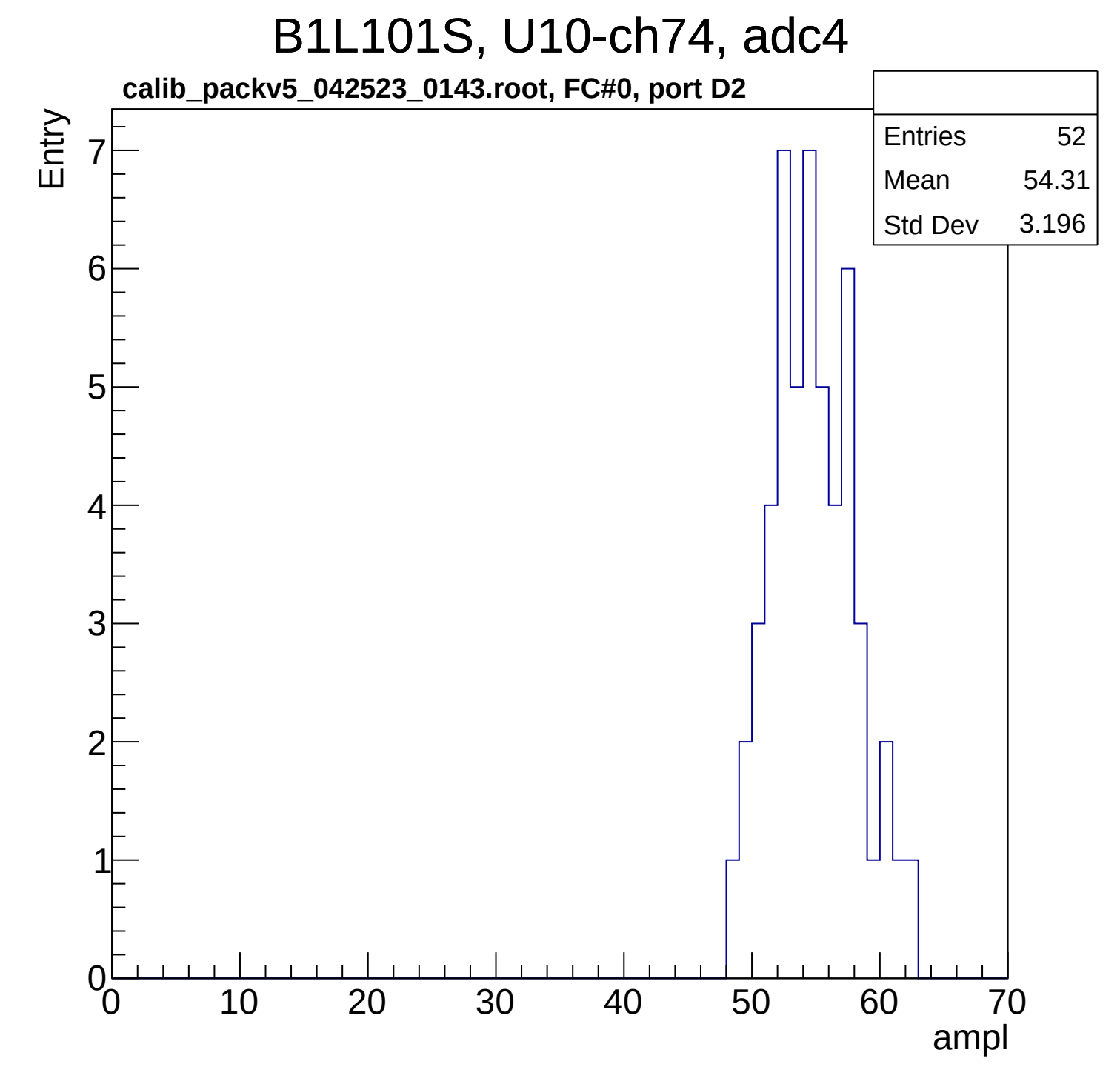
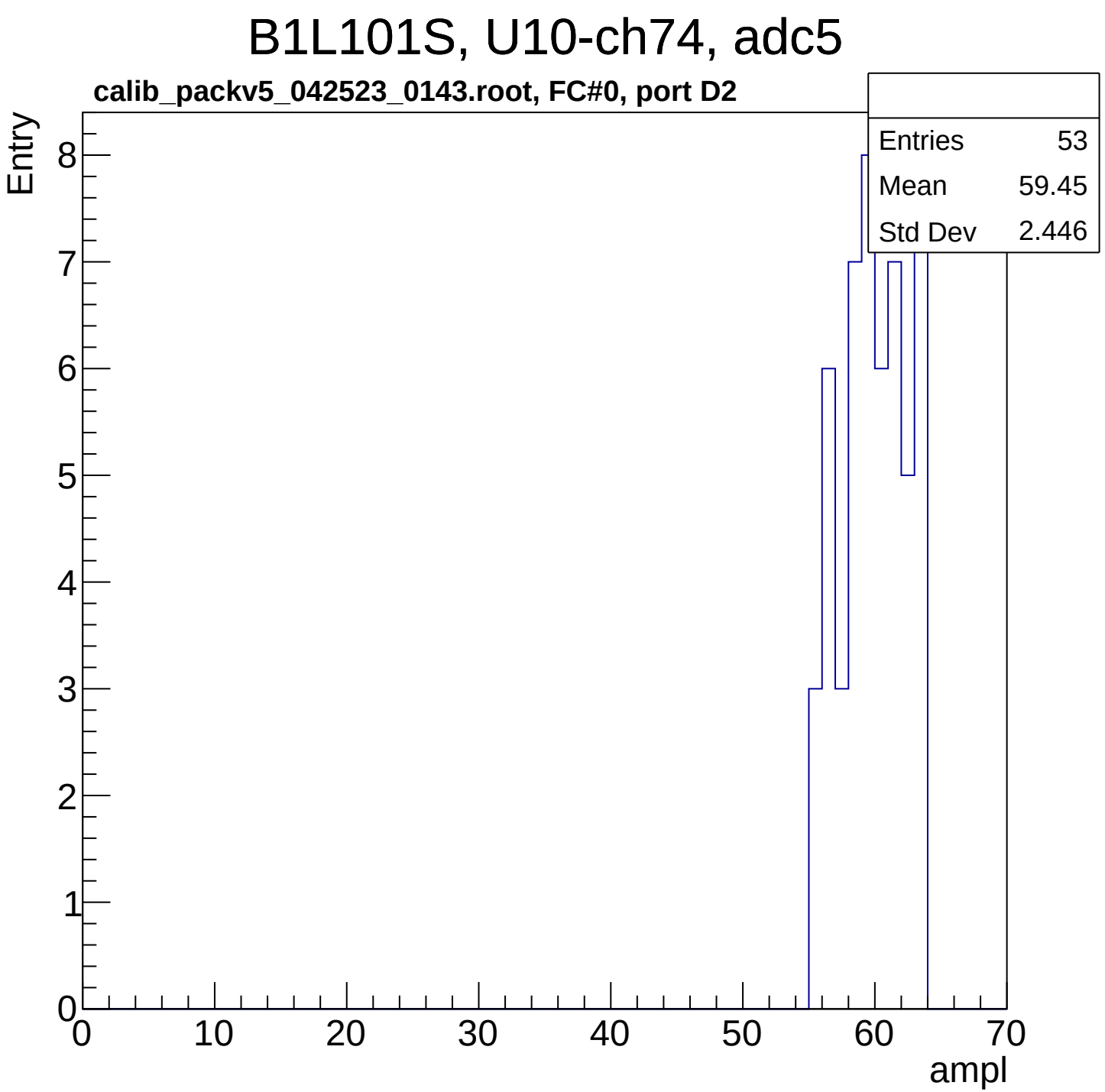

B1L101S, U10-ch74, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 42.73
Std Dev 3.629
Gaus mean : 44.5517
Gaus Width: 3.6812
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch74, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 49.07
Std Dev 3.371
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch74, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 54.31
Std Dev 3.196
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U10-ch74, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 59.45
Std Dev 2.446
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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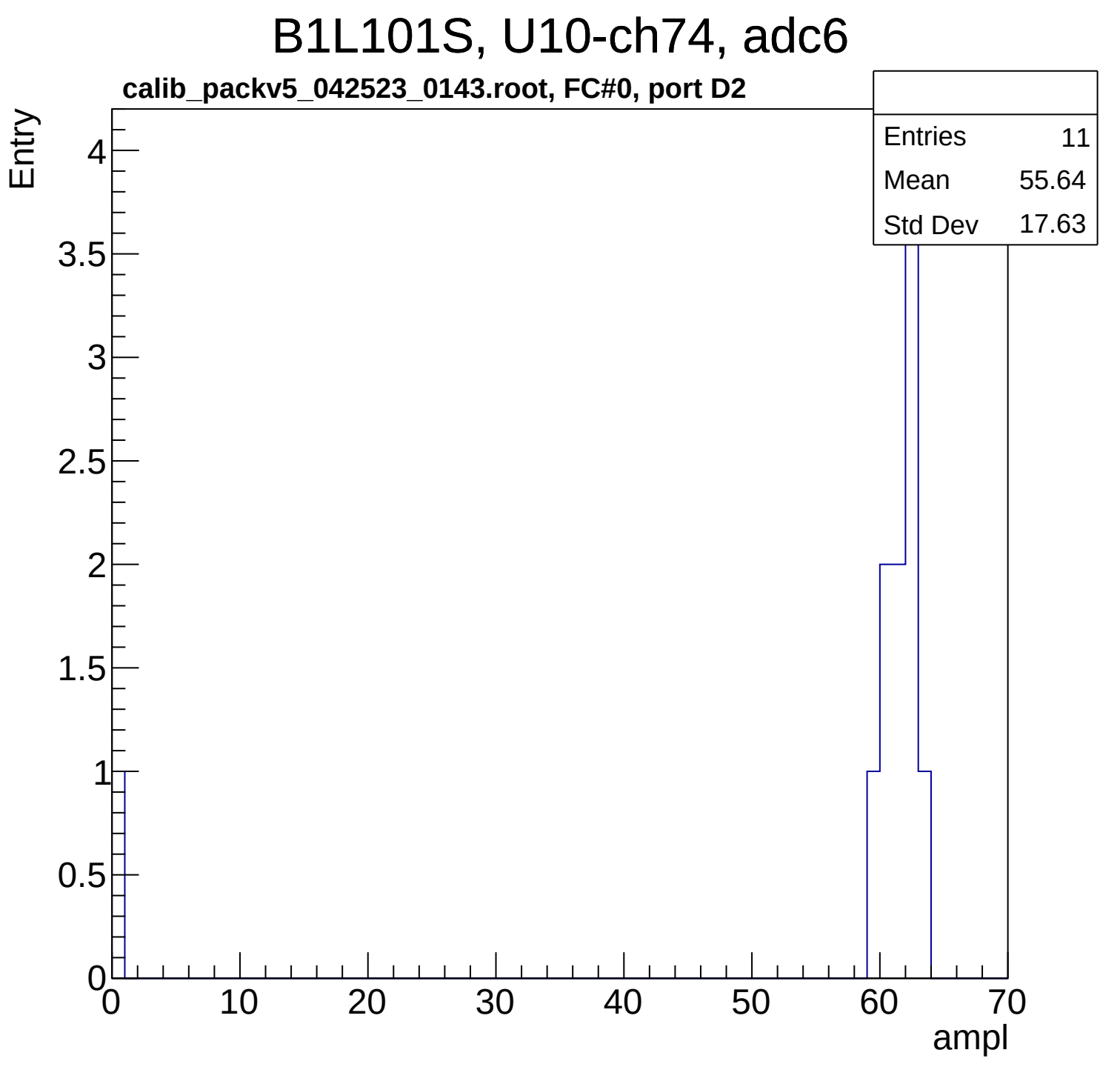
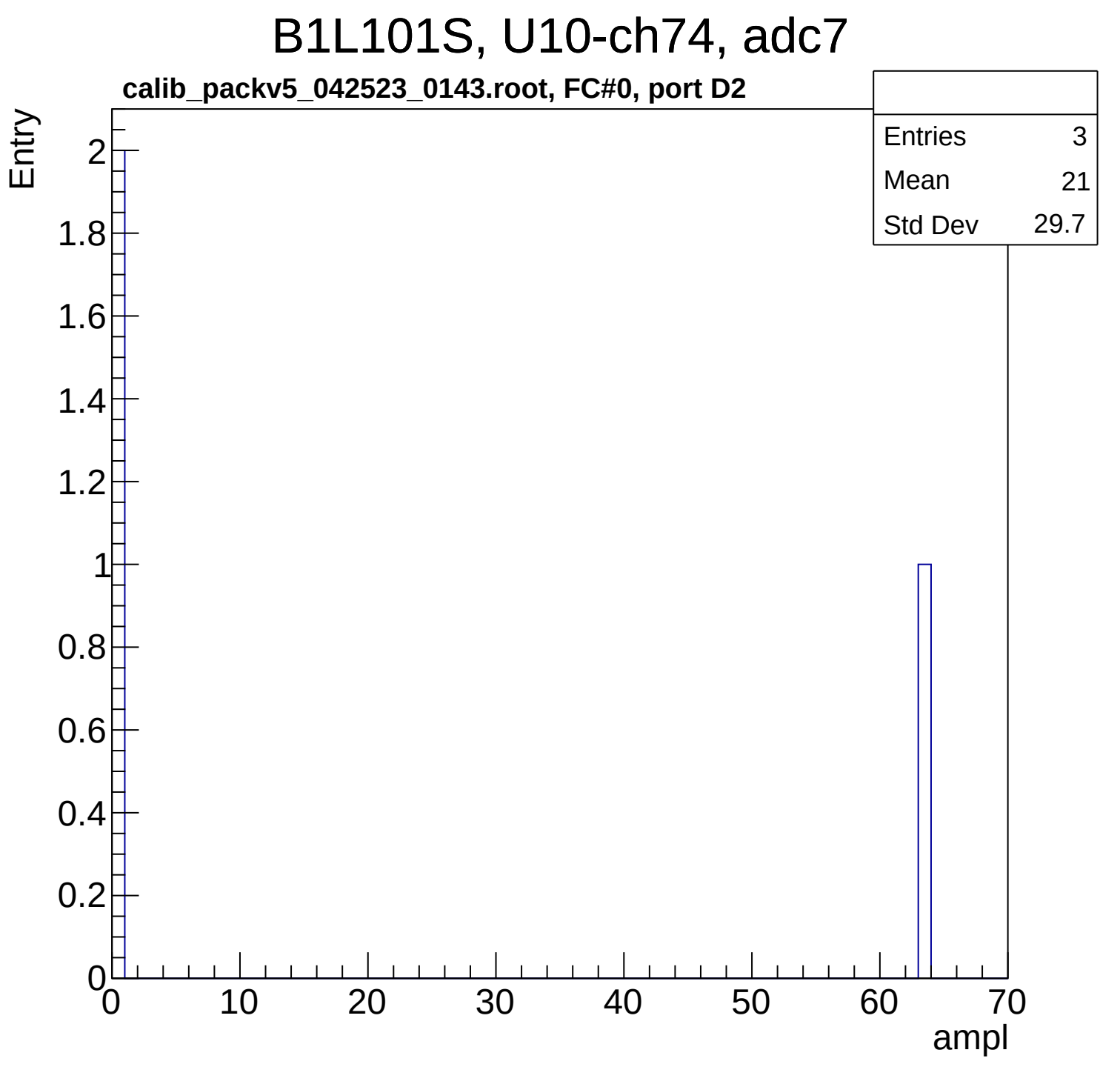

B1L101S, U10-ch74, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 11
Mean 55.64
Std Dev 17.63
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L101S, U10-ch74, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 21
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
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60
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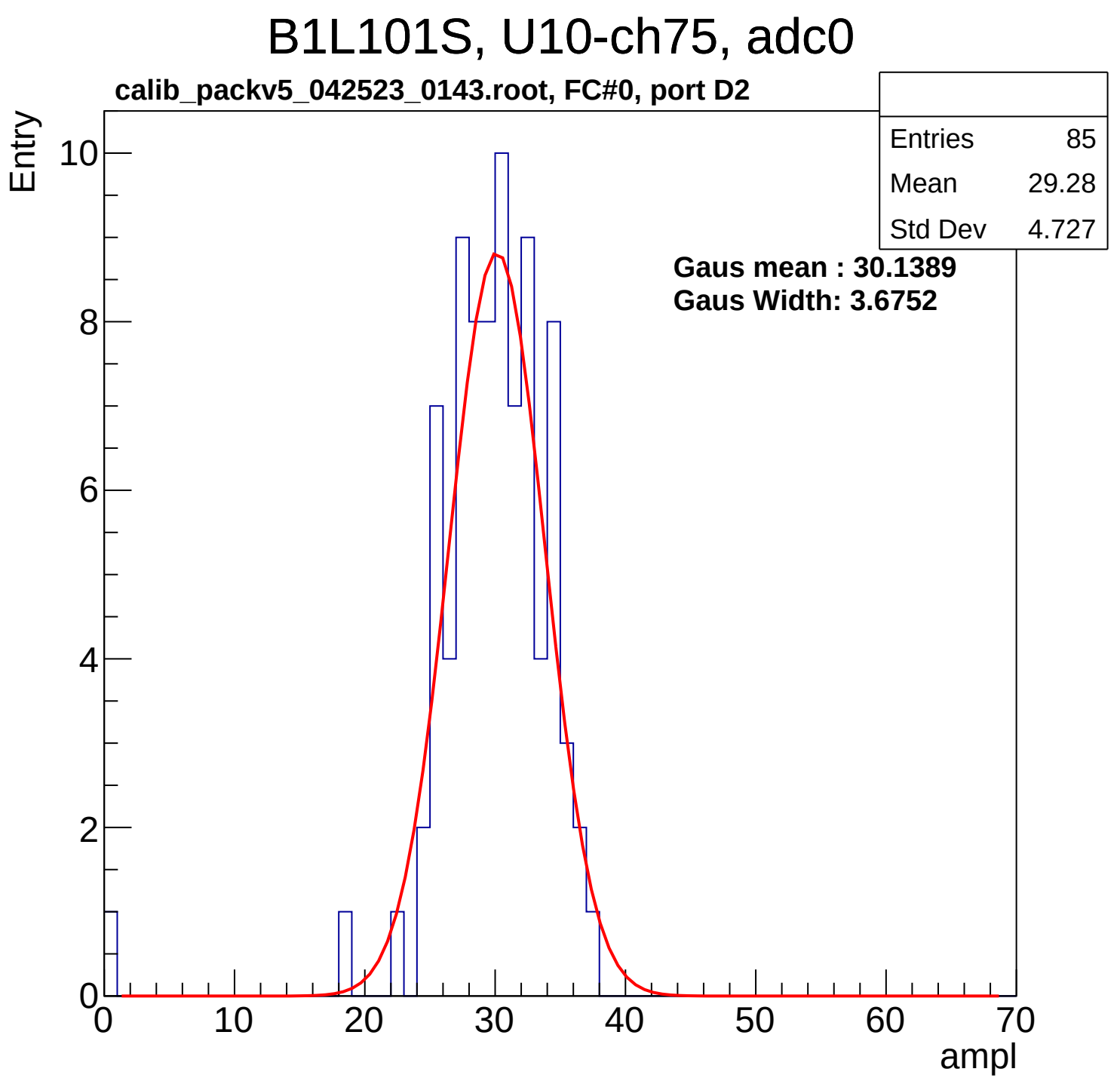
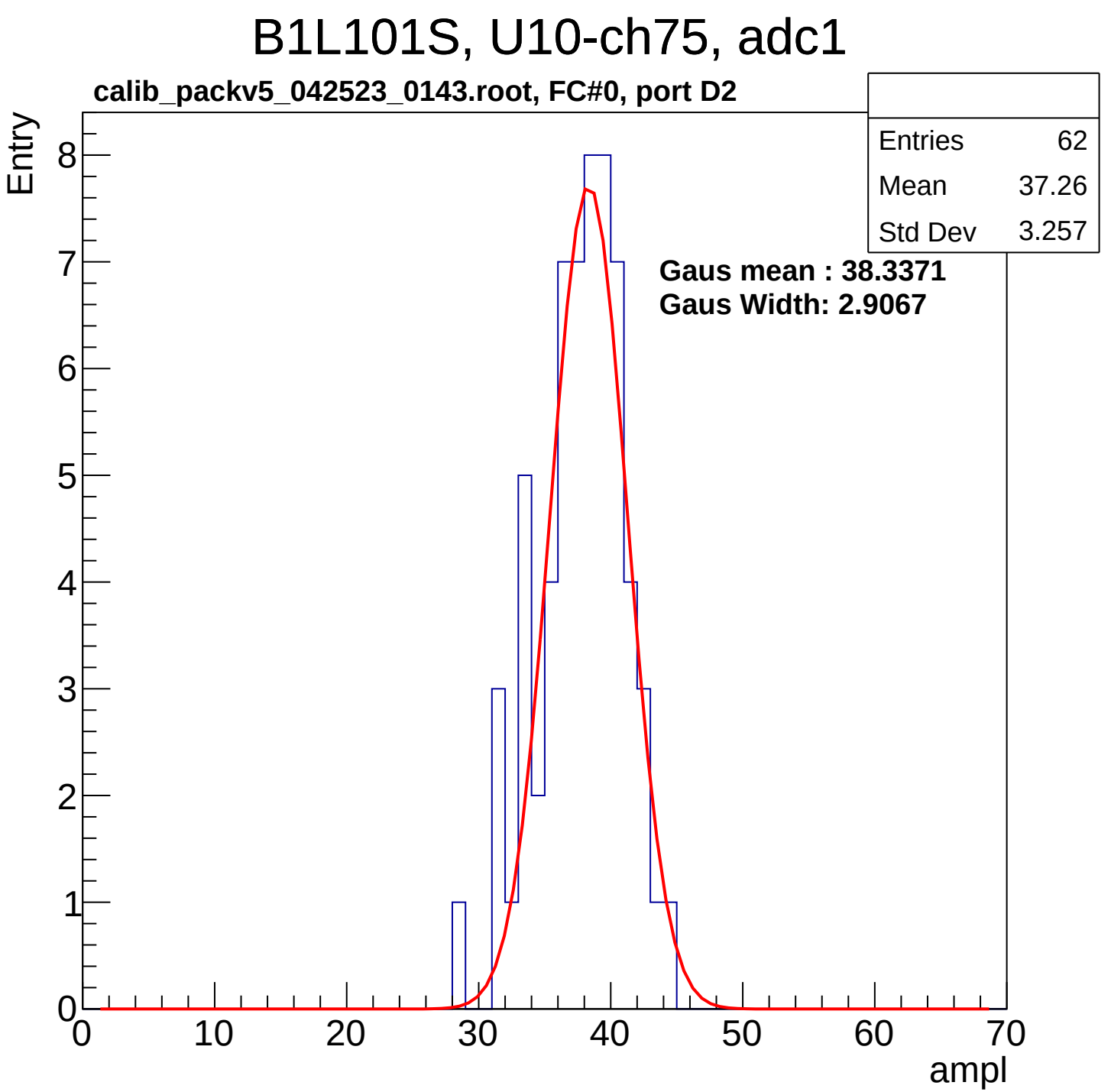
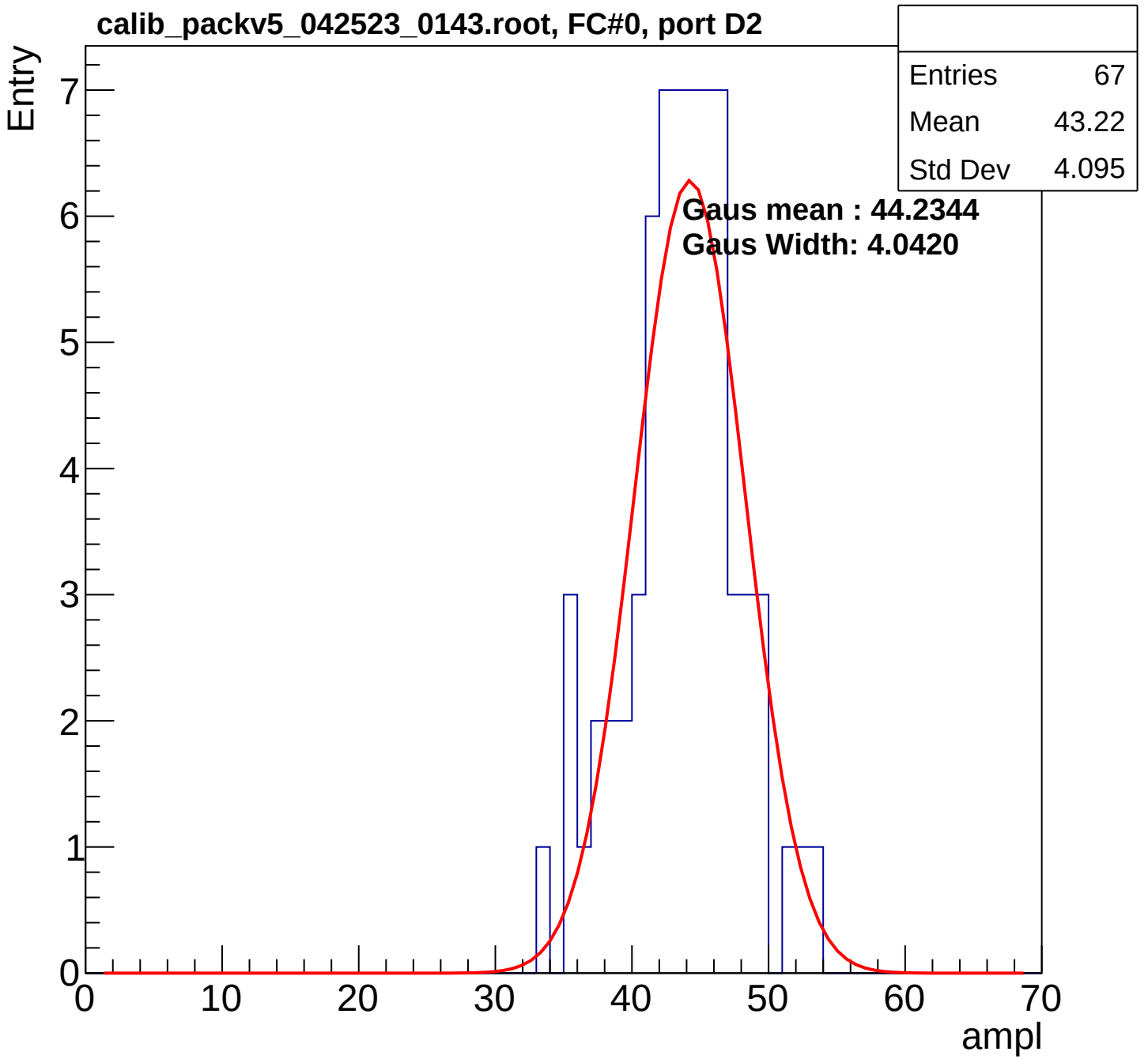
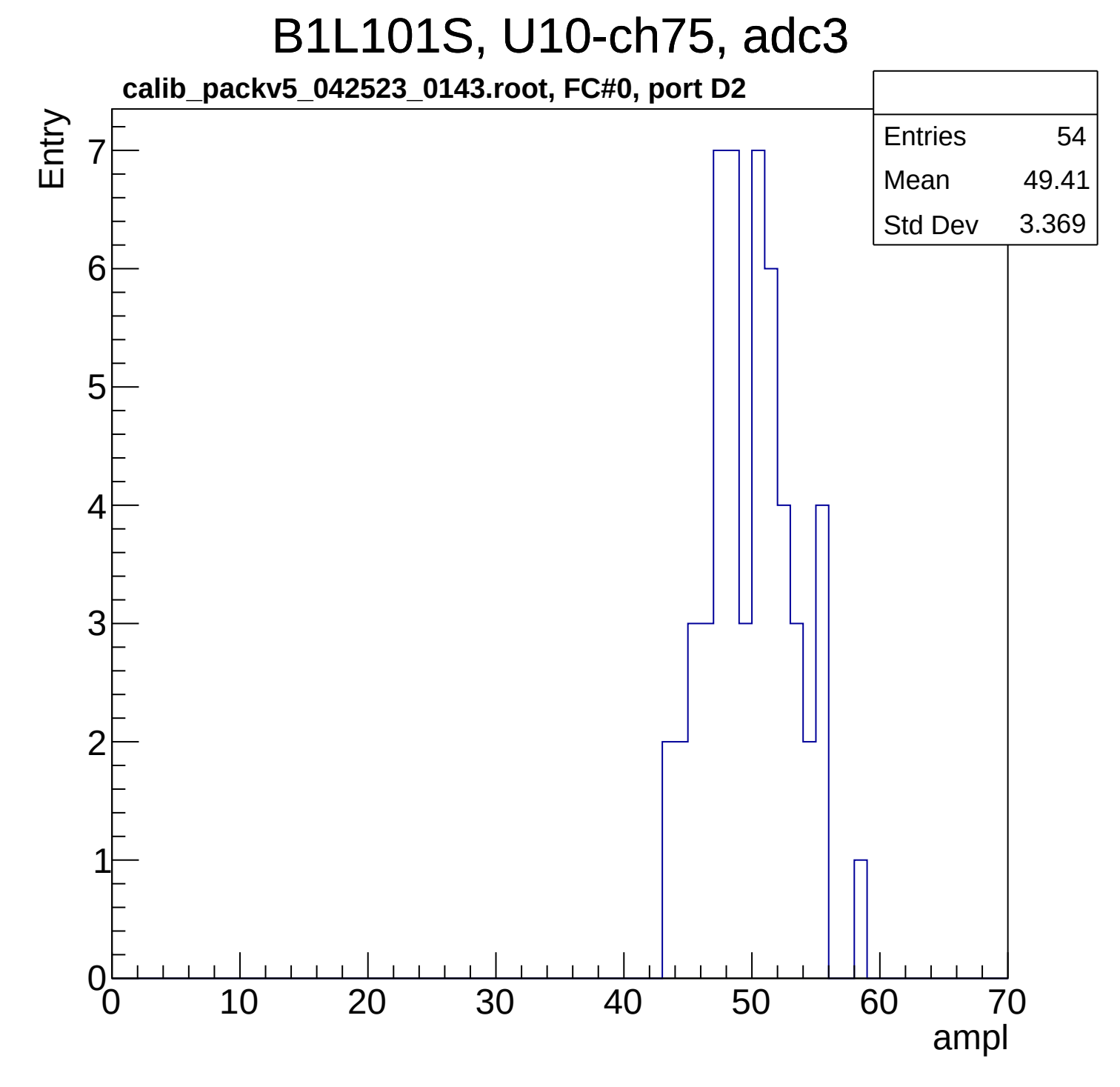
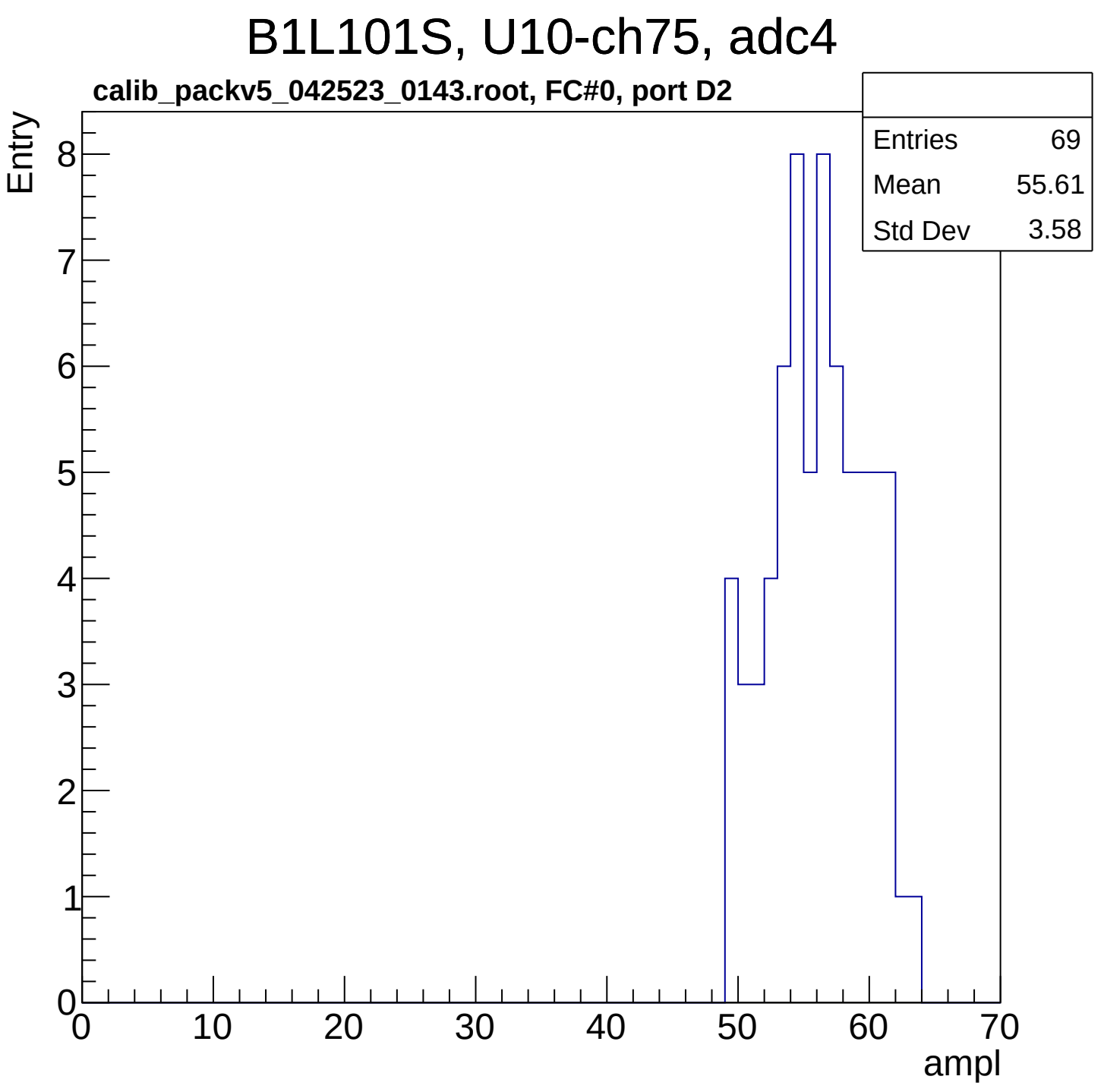

B1L101S, U10-ch75, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 85
Mean 29.28
Std Dev 4.727
Gaus mean : 30.1389
Gaus Width: 3.6752
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch75, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 37.26
Std Dev 3.257
Gaus mean : 38.3371
Gaus Width: 2.9067
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch75, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 43.22
Std Dev 4.095
Gaus mean : 44.2344
Gaus Width: 4.0420
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U10-ch75, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 49.41
Std Dev 3.369
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U10-ch75, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 55.61
Std Dev 3.58
Entry
ampl
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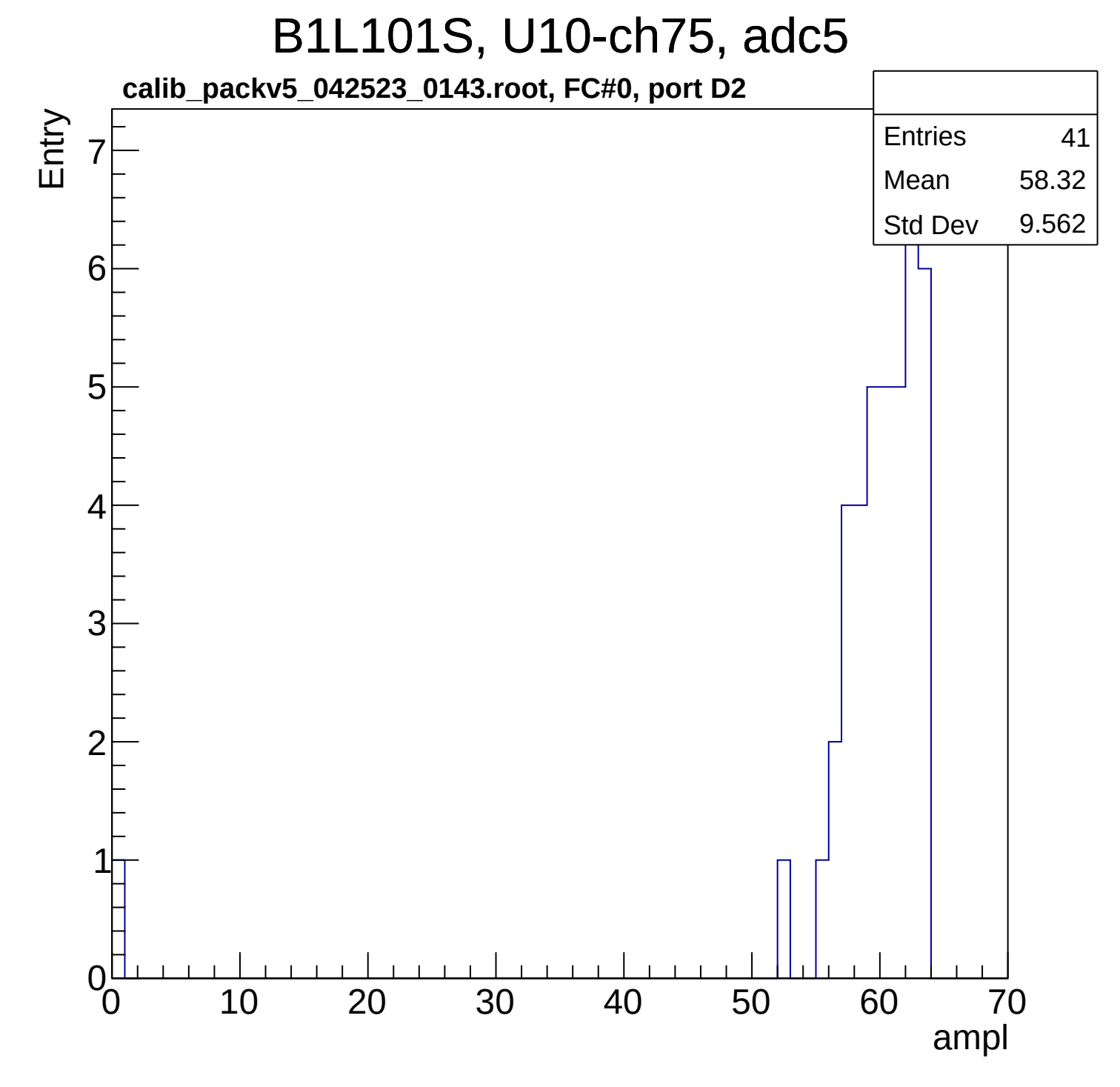
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch75, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 41
Mean 58.32
Std Dev 9.562
Entry
ampl
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1
2
3
4
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7
0
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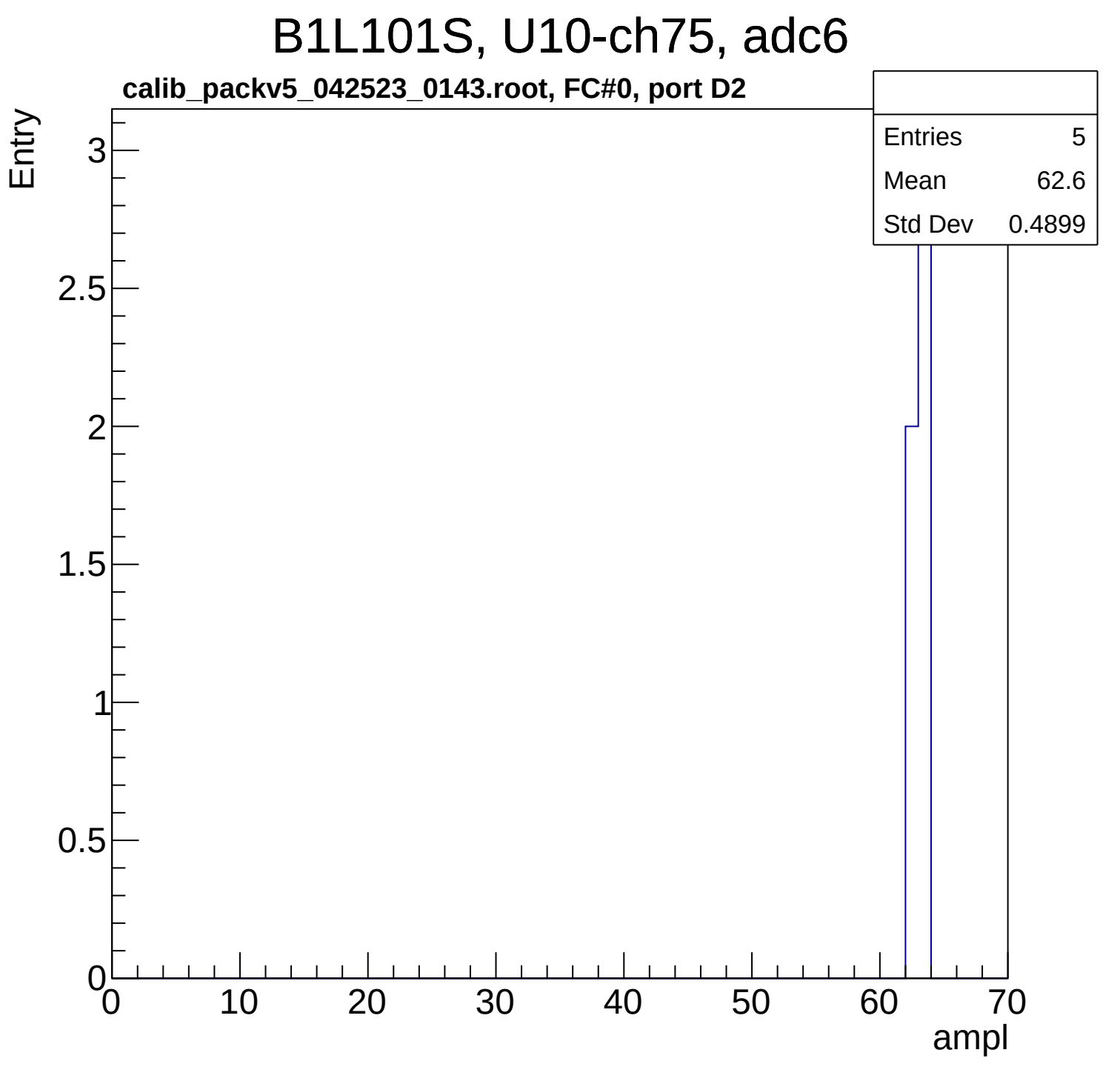
20
30
40
50
60
70


B1L101S, U10-ch75, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 62.6
Std Dev 0.4899
Entry
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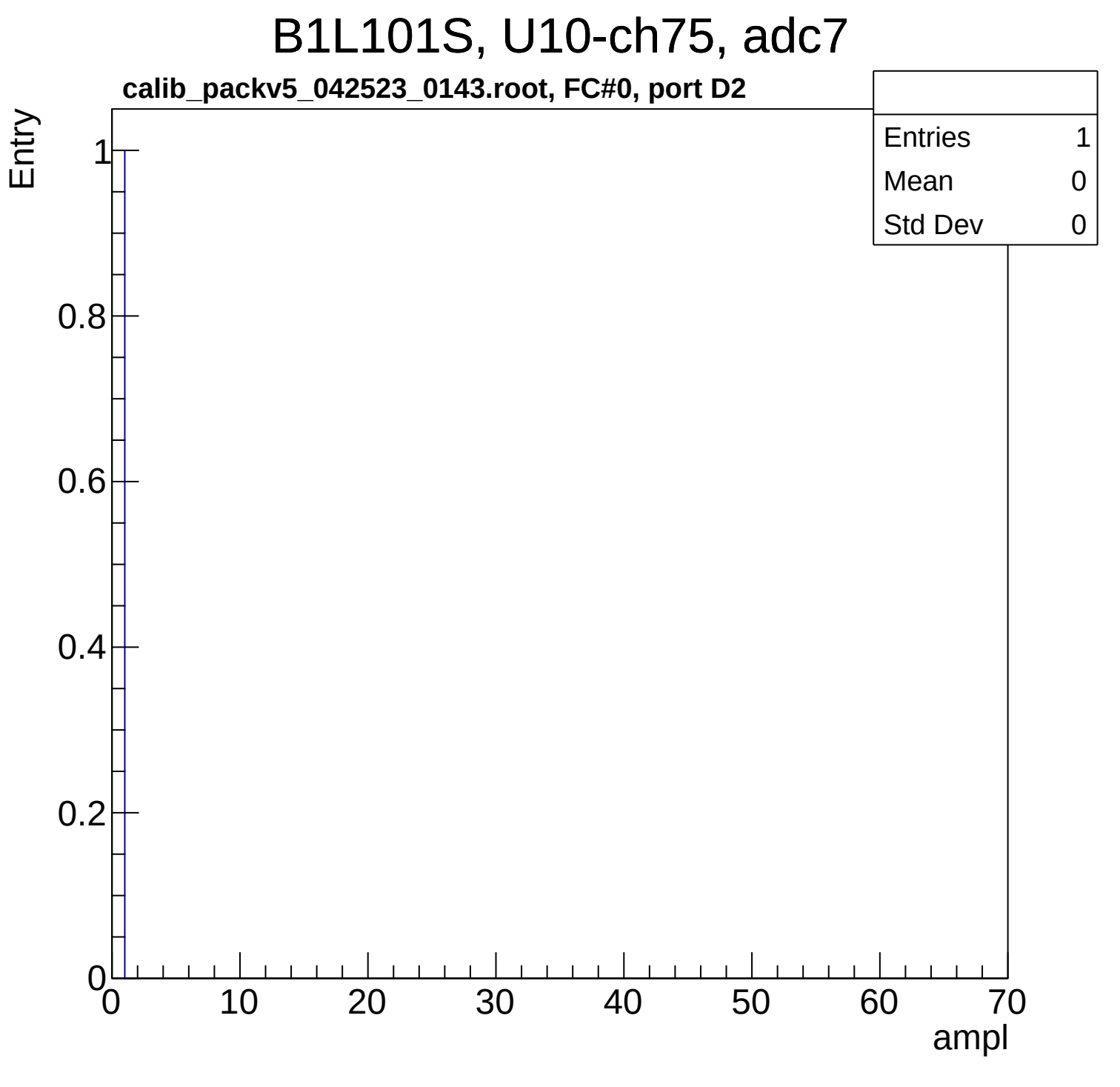
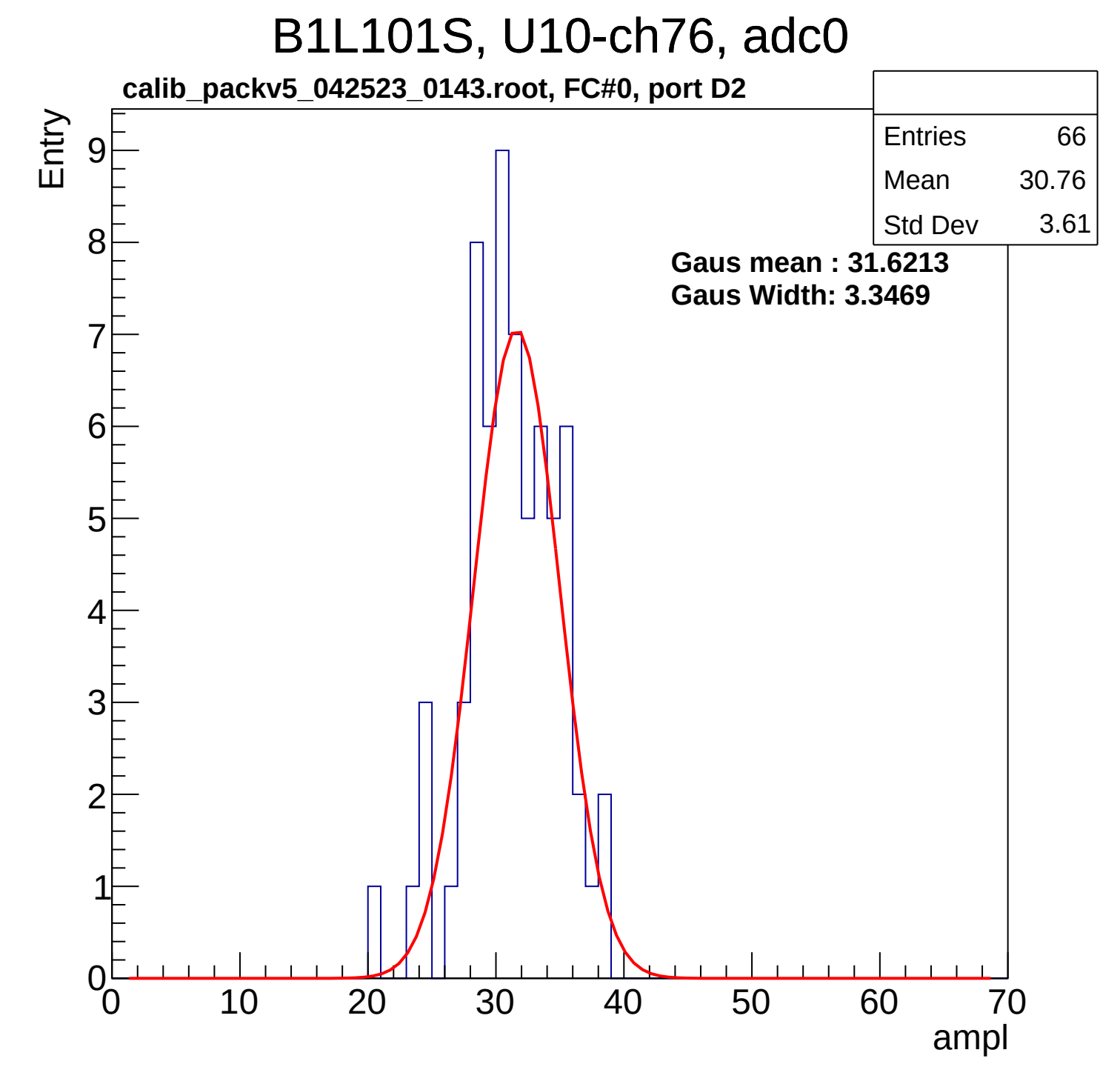
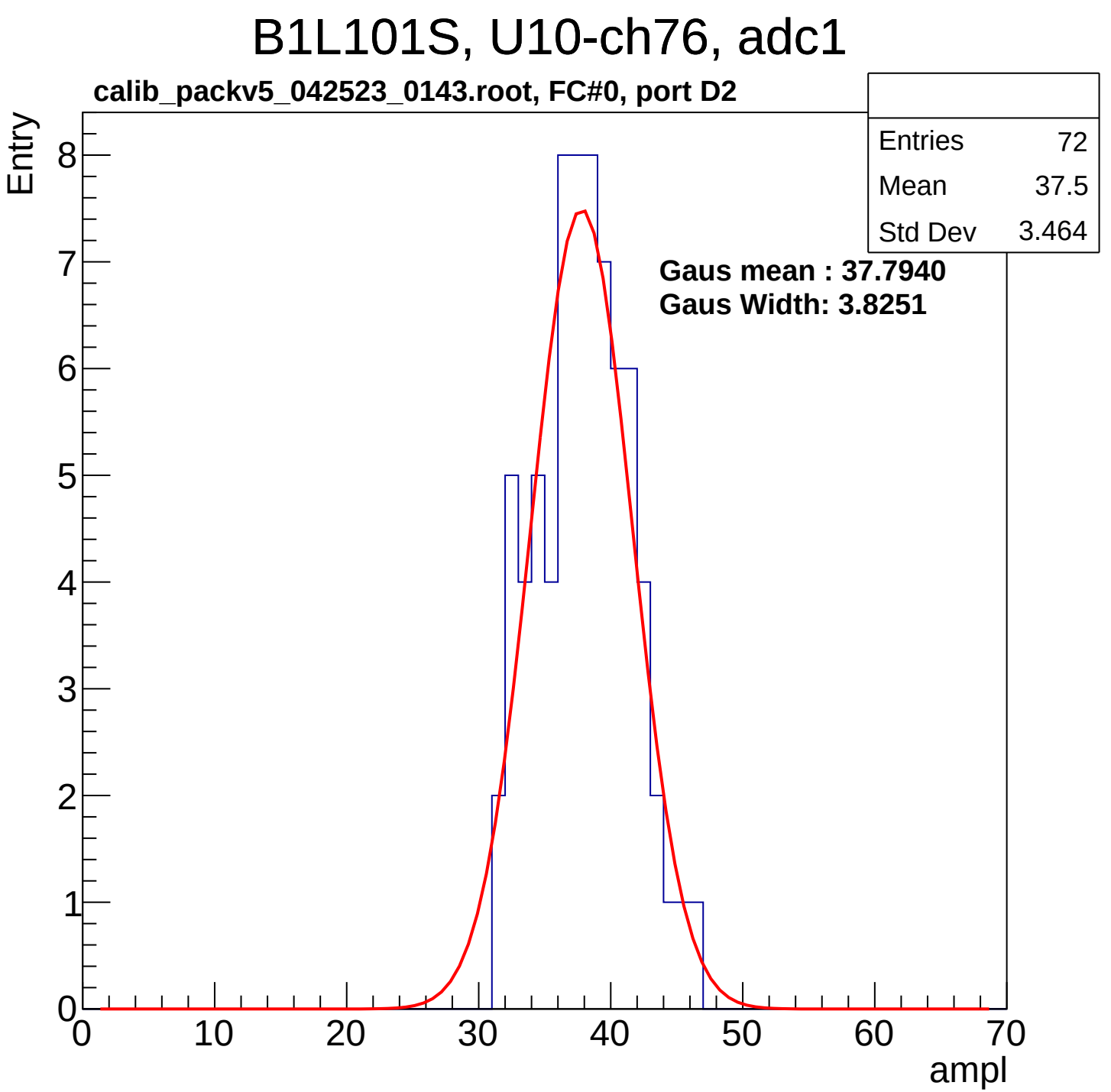
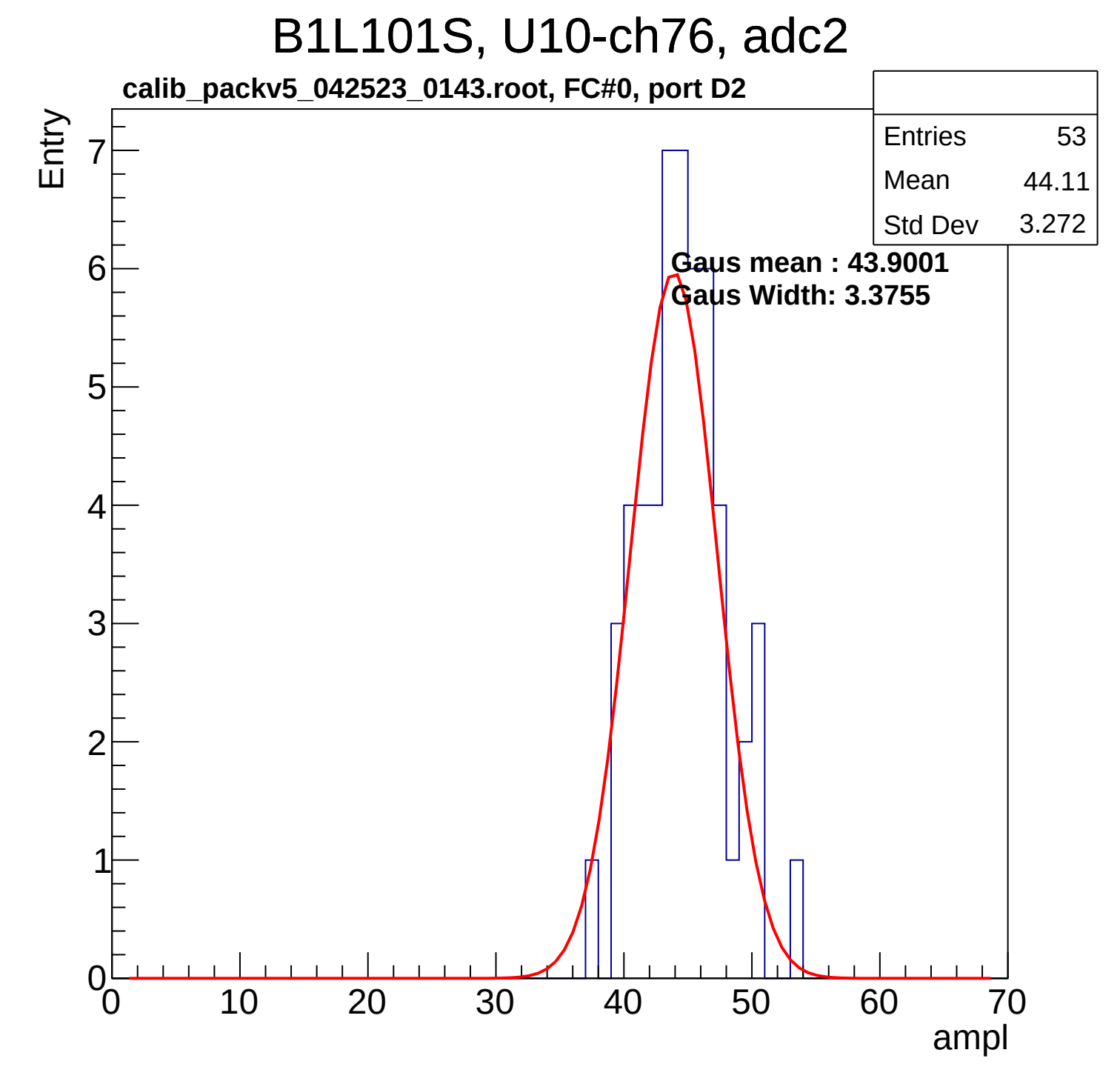
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch75, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch76, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 30.76
Std Dev 3.61
Gaus mean : 31.6213
Gaus Width: 3.3469
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch76, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 37.5
Std Dev 3.464
Gaus mean : 37.7940
Gaus Width: 3.8251
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch76, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 44.11
Std Dev 3.272
Gaus mean : 43.9001
Gaus Width: 3.3755
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
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60
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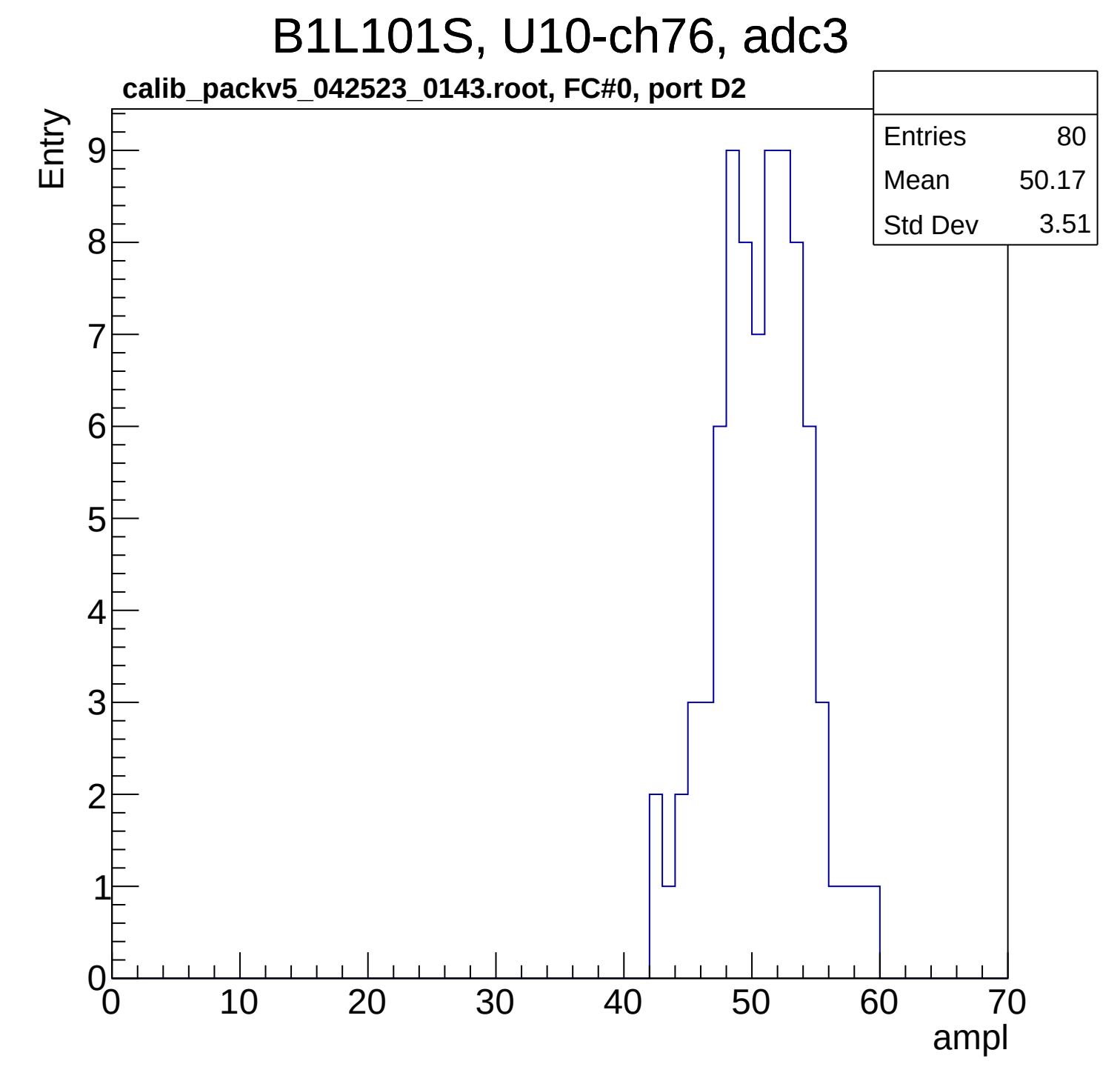
B1L101S, U10-ch76, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 80
Mean 50.17
Std Dev 3.51
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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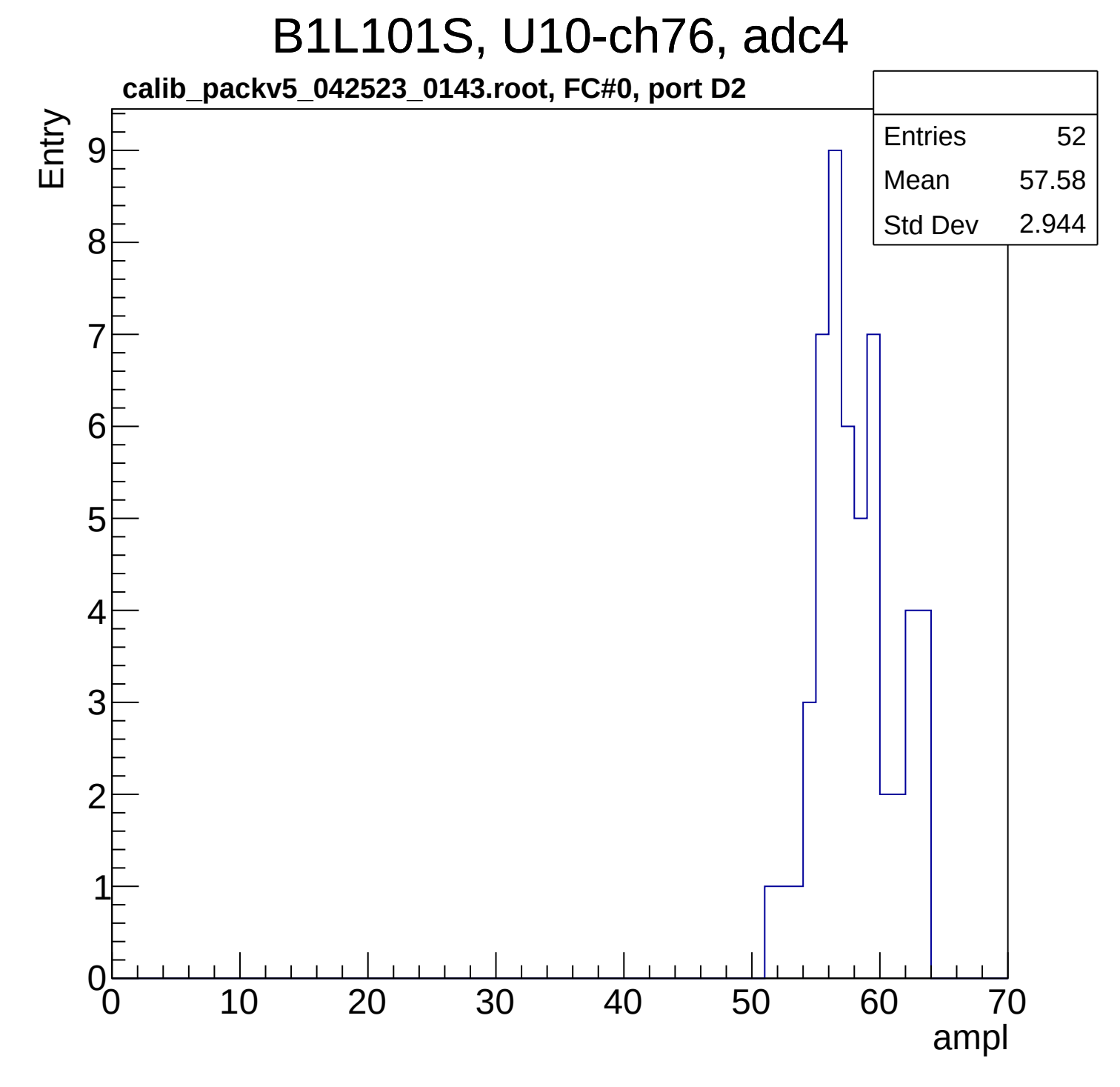
B1L101S, U10-ch76, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 57.58
Std Dev 2.944
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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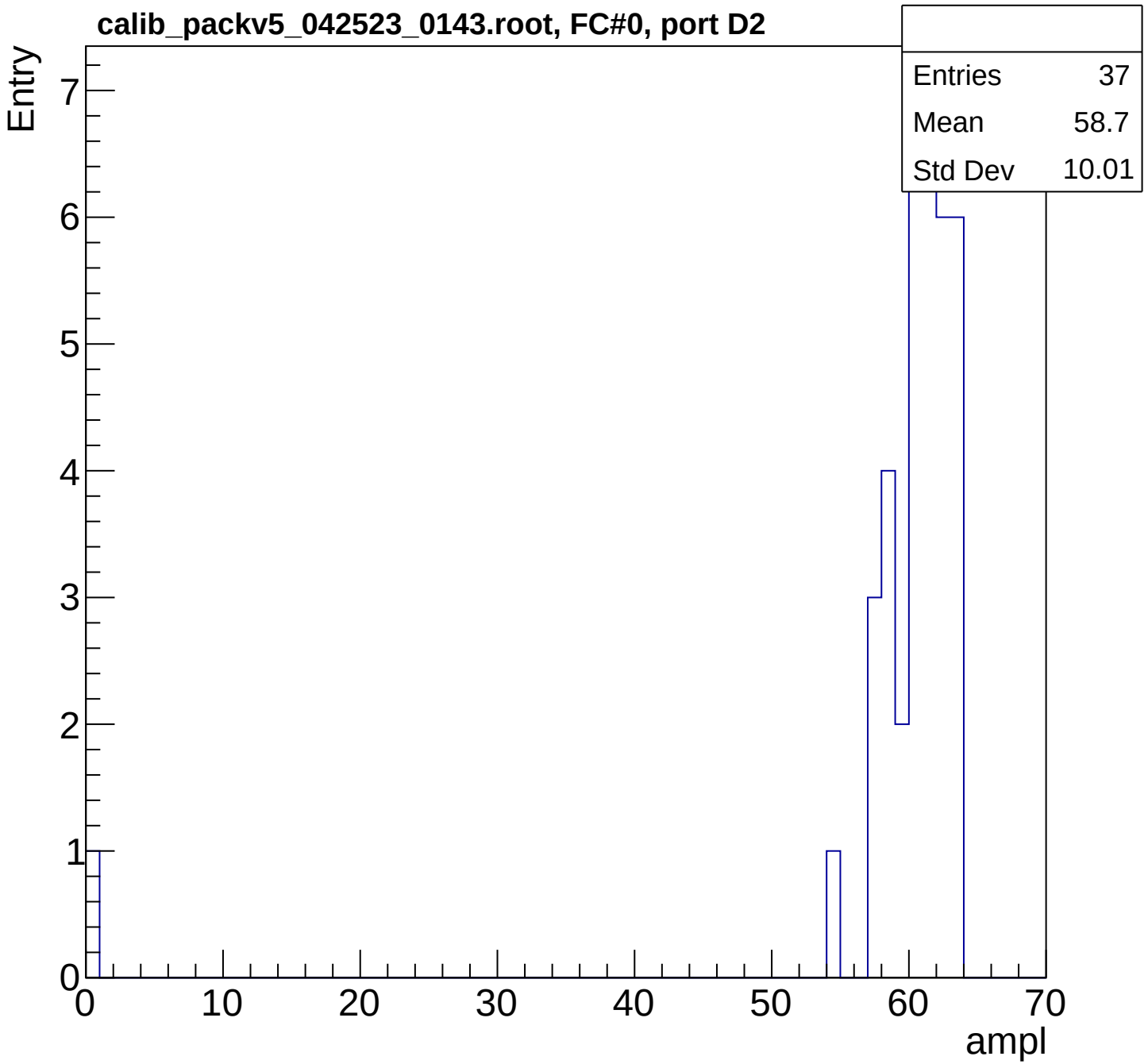
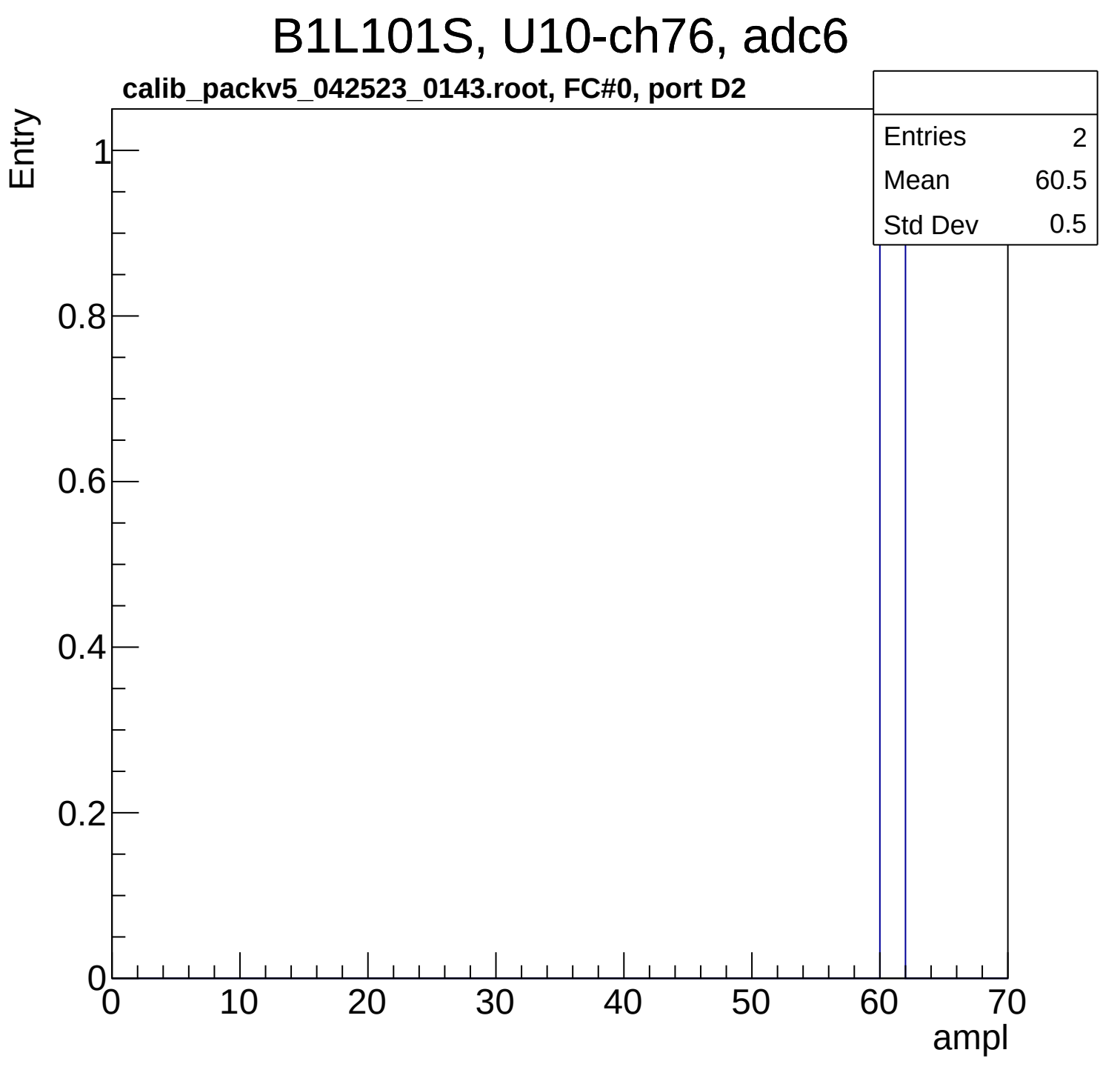

B1L101S, U10-ch76, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 37
Mean 58.7
Std Dev 10.01
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U10-ch76, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 60.5
Std Dev 0.5
Entry
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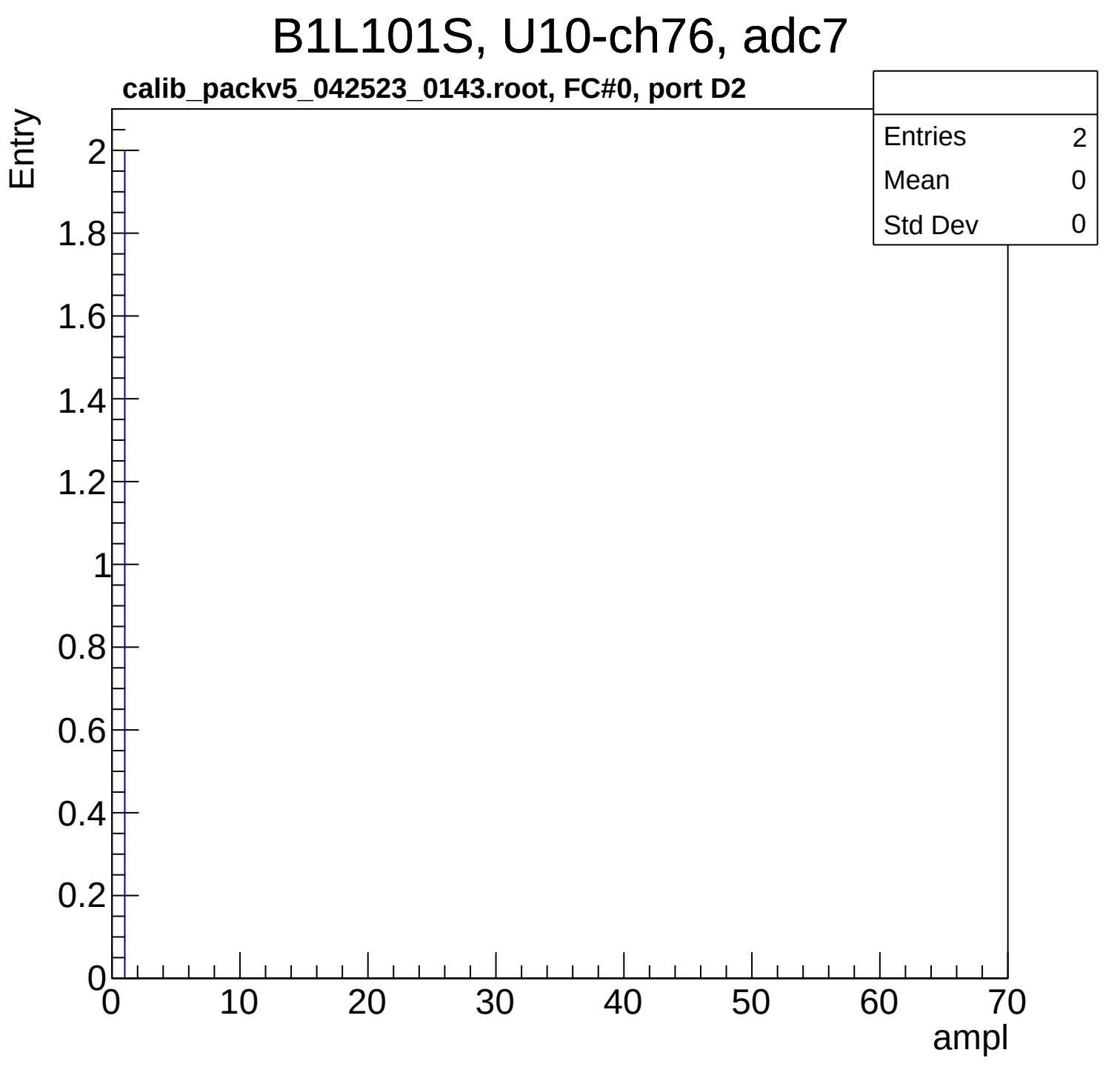
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch76, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
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1.2
1.4
1.6
1.8
2
0
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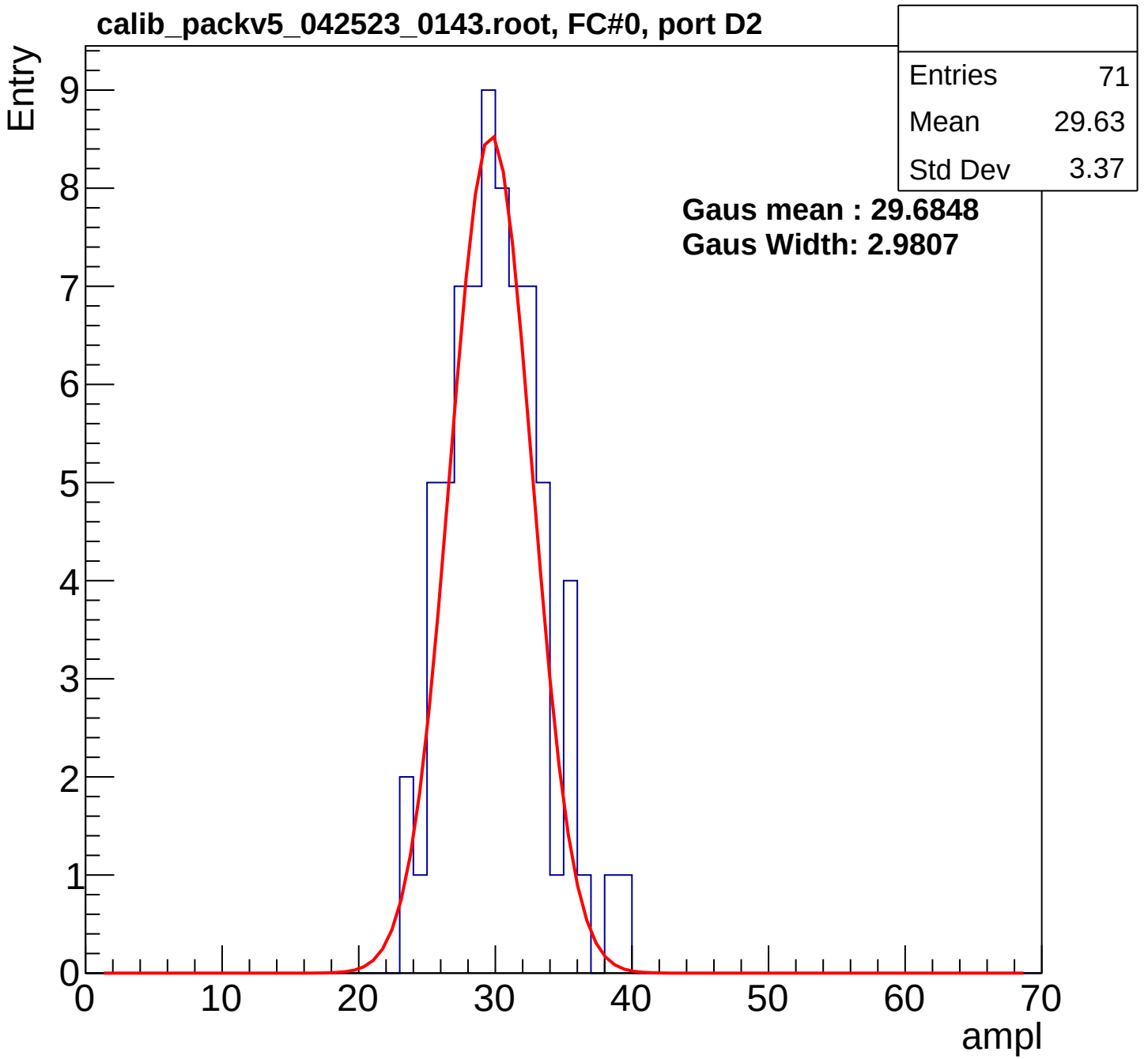
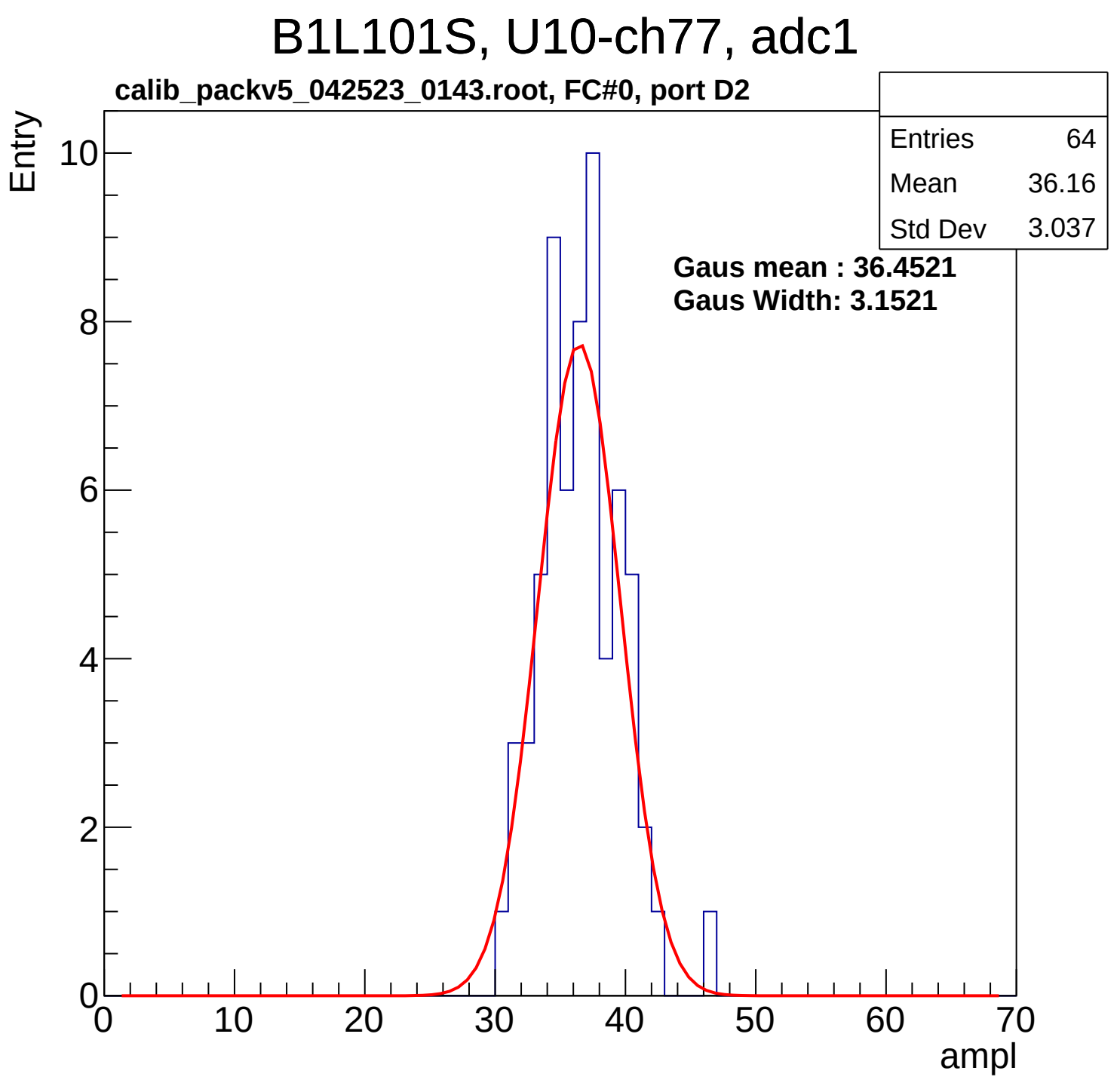
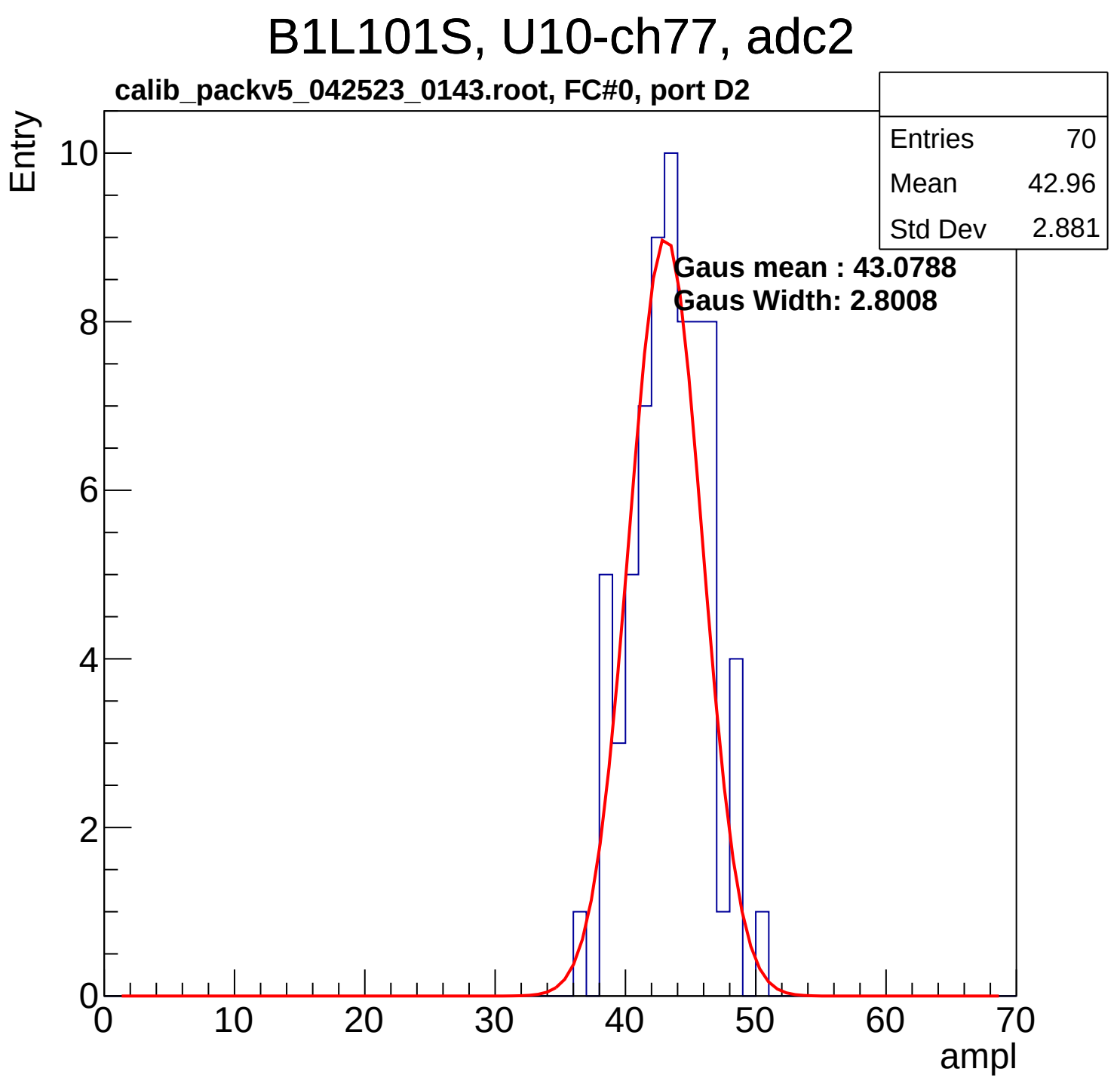
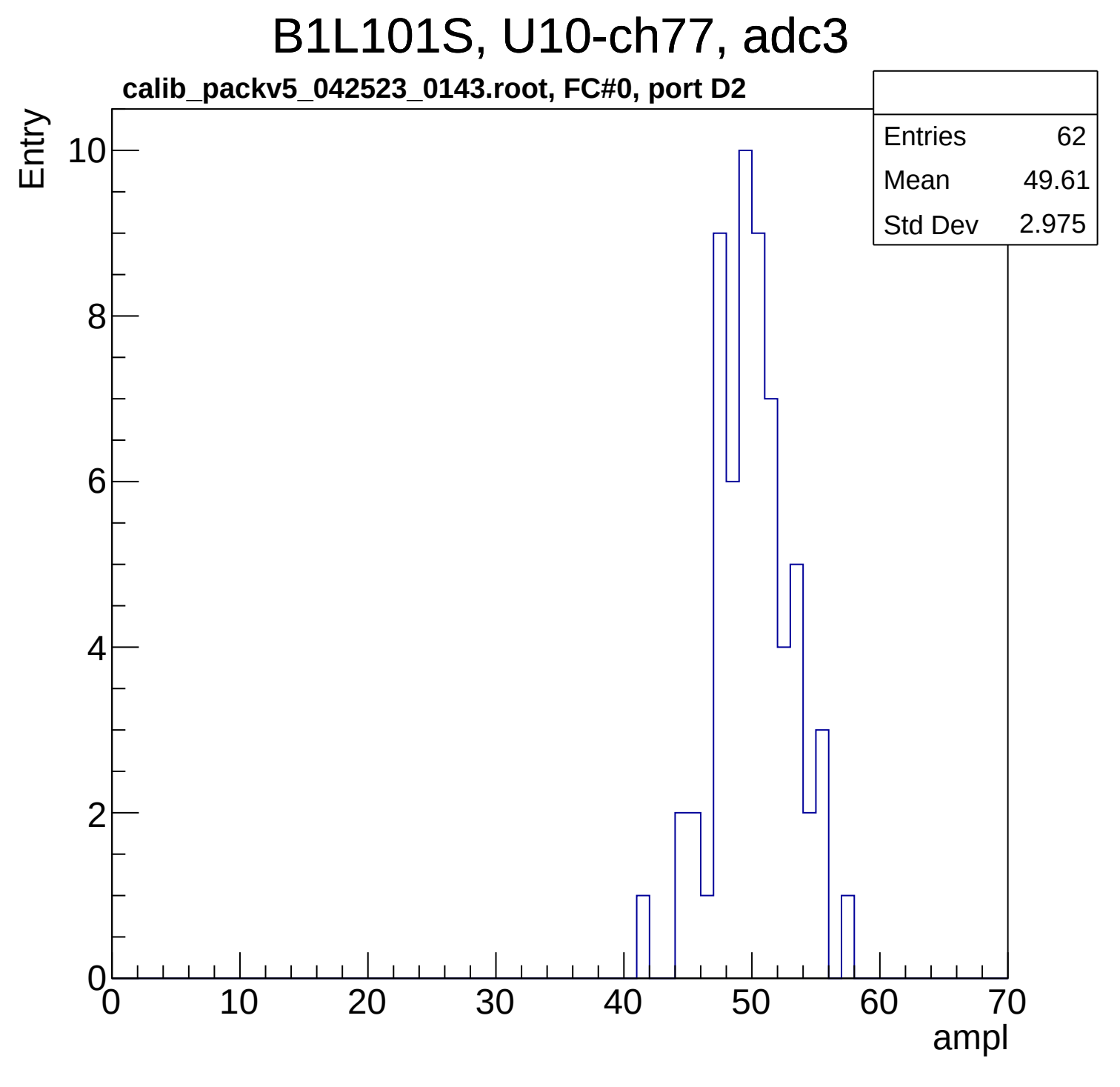
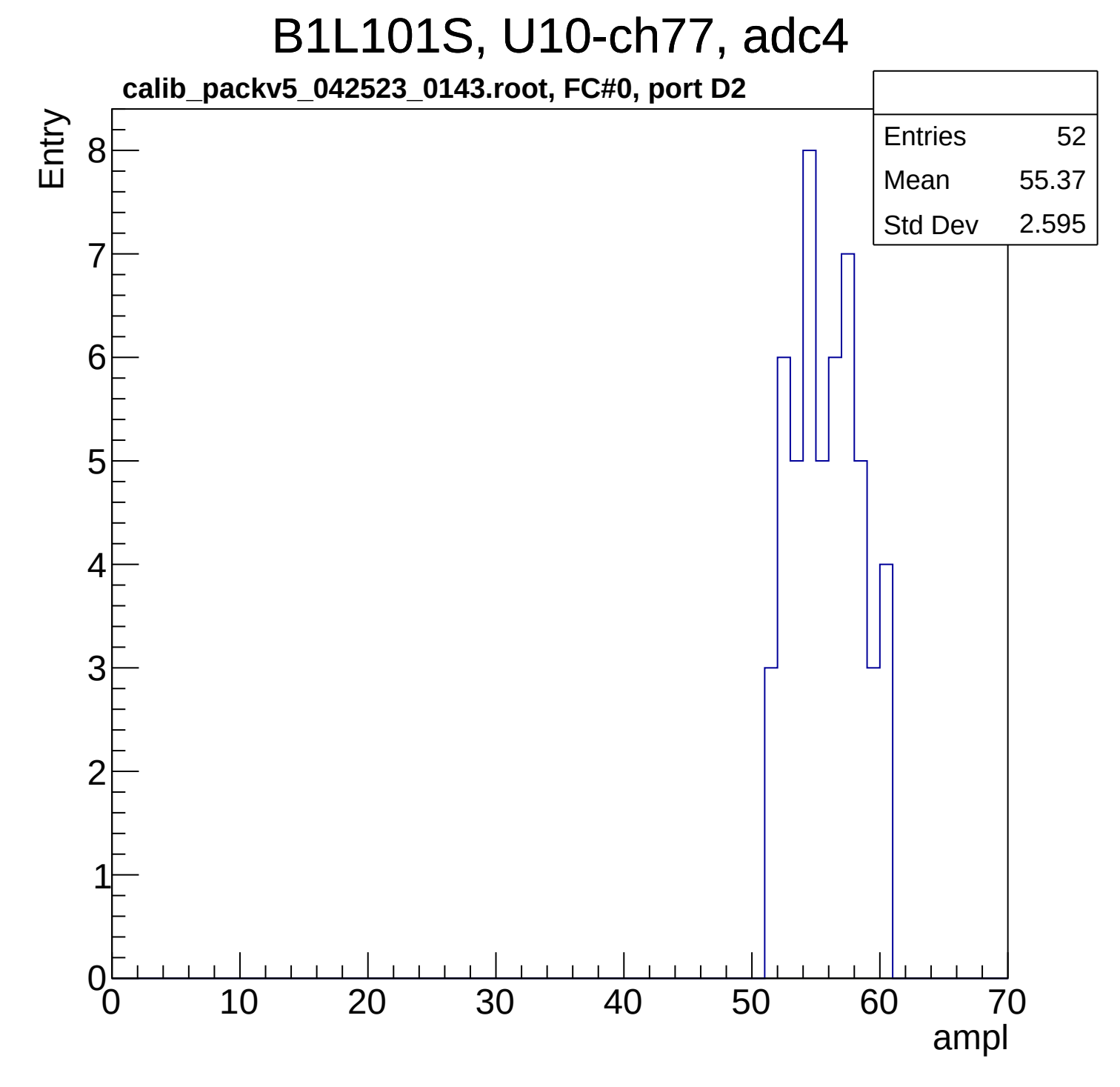
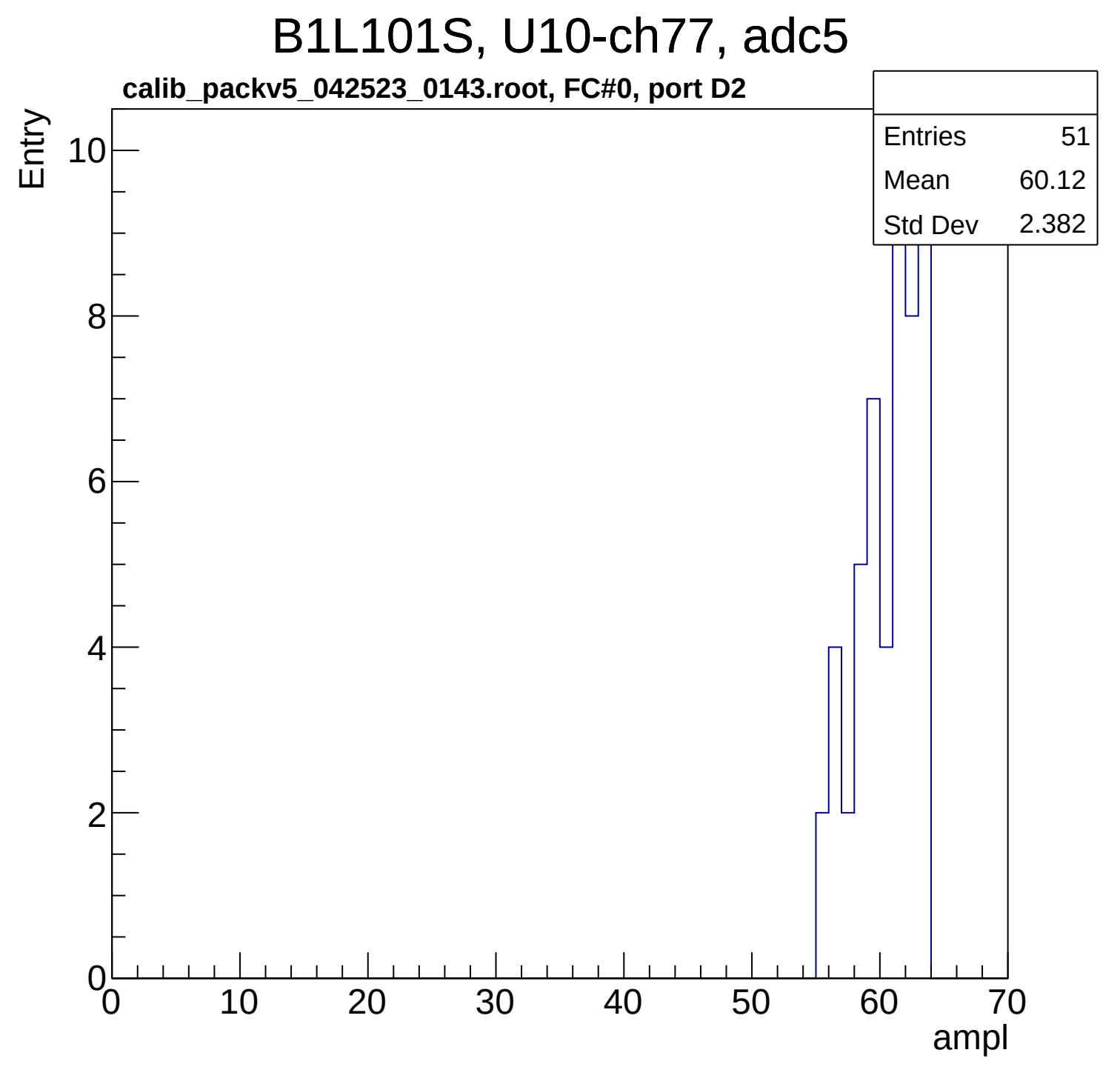

B1L101S, U10-ch77, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 29.63
Std Dev 3.37
Gaus mean : 29.6848
Gaus Width: 2.9807
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

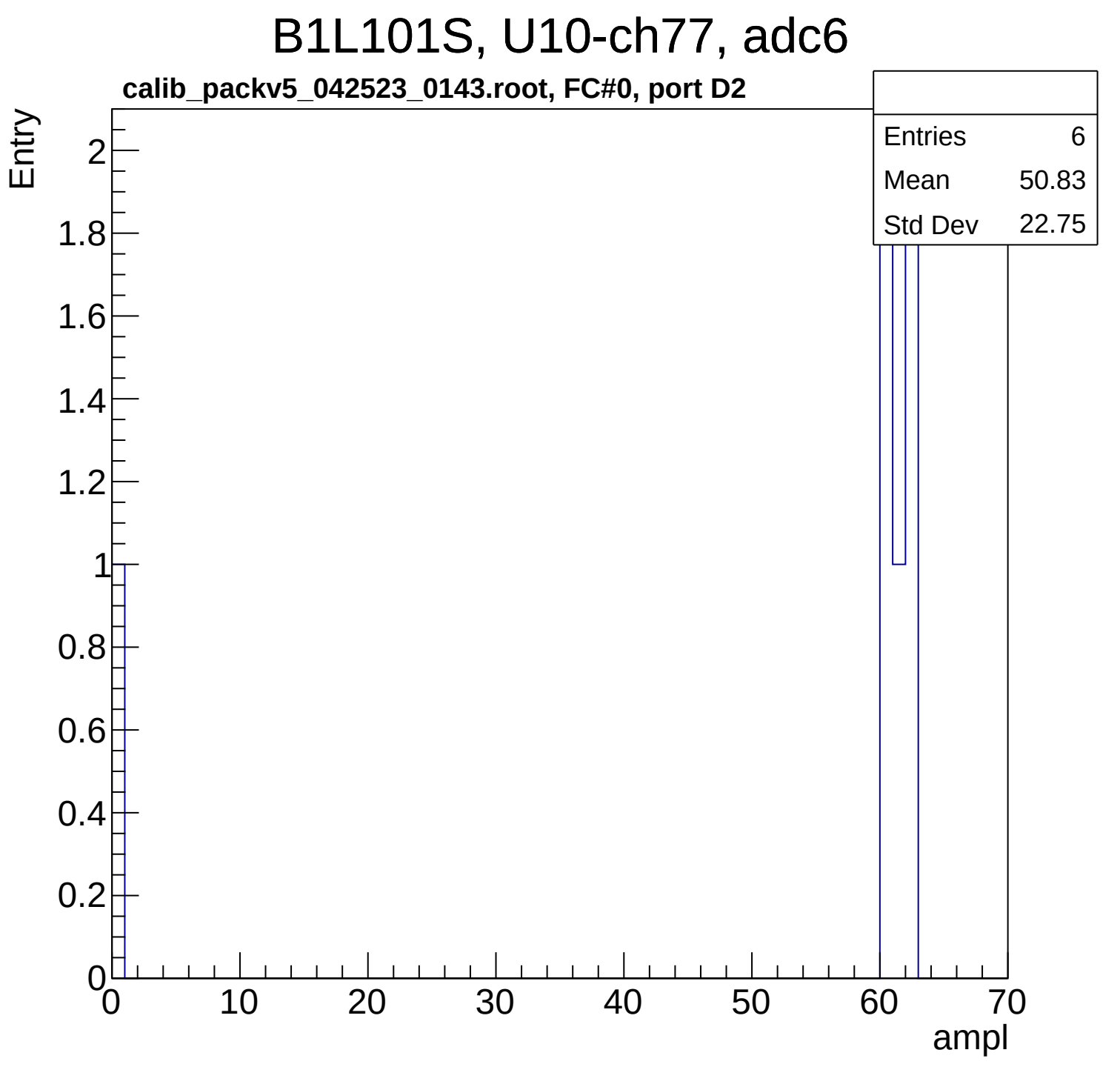

B1L101S, U10-ch77, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 36.16
Std Dev 3.037
Gaus mean : 36.4521
Gaus Width: 3.1521
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

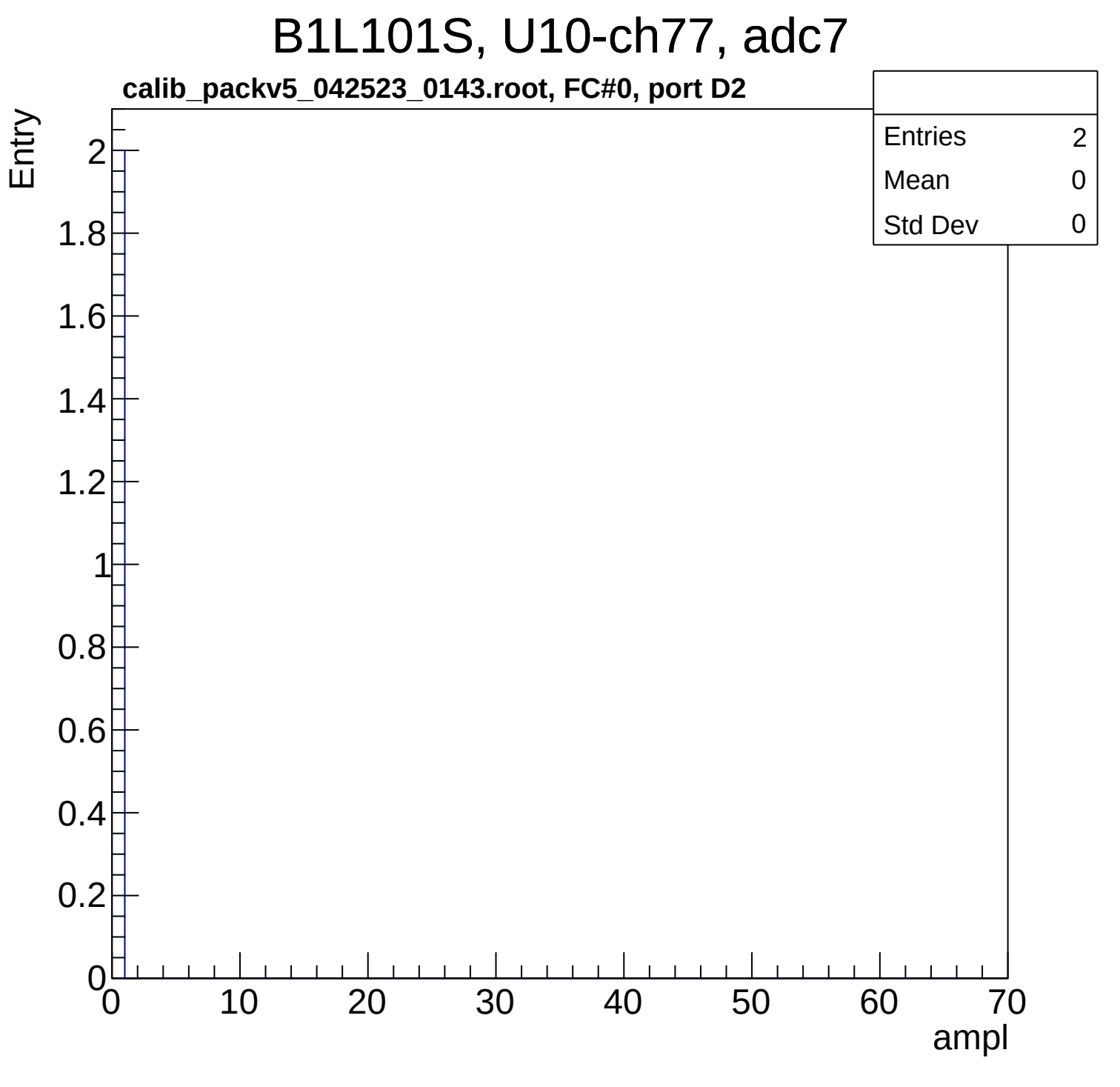

B1L101S, U10-ch77, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 42.96
Std Dev 2.881
Gaus mean : 43.0788
Gaus Width: 2.8008
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

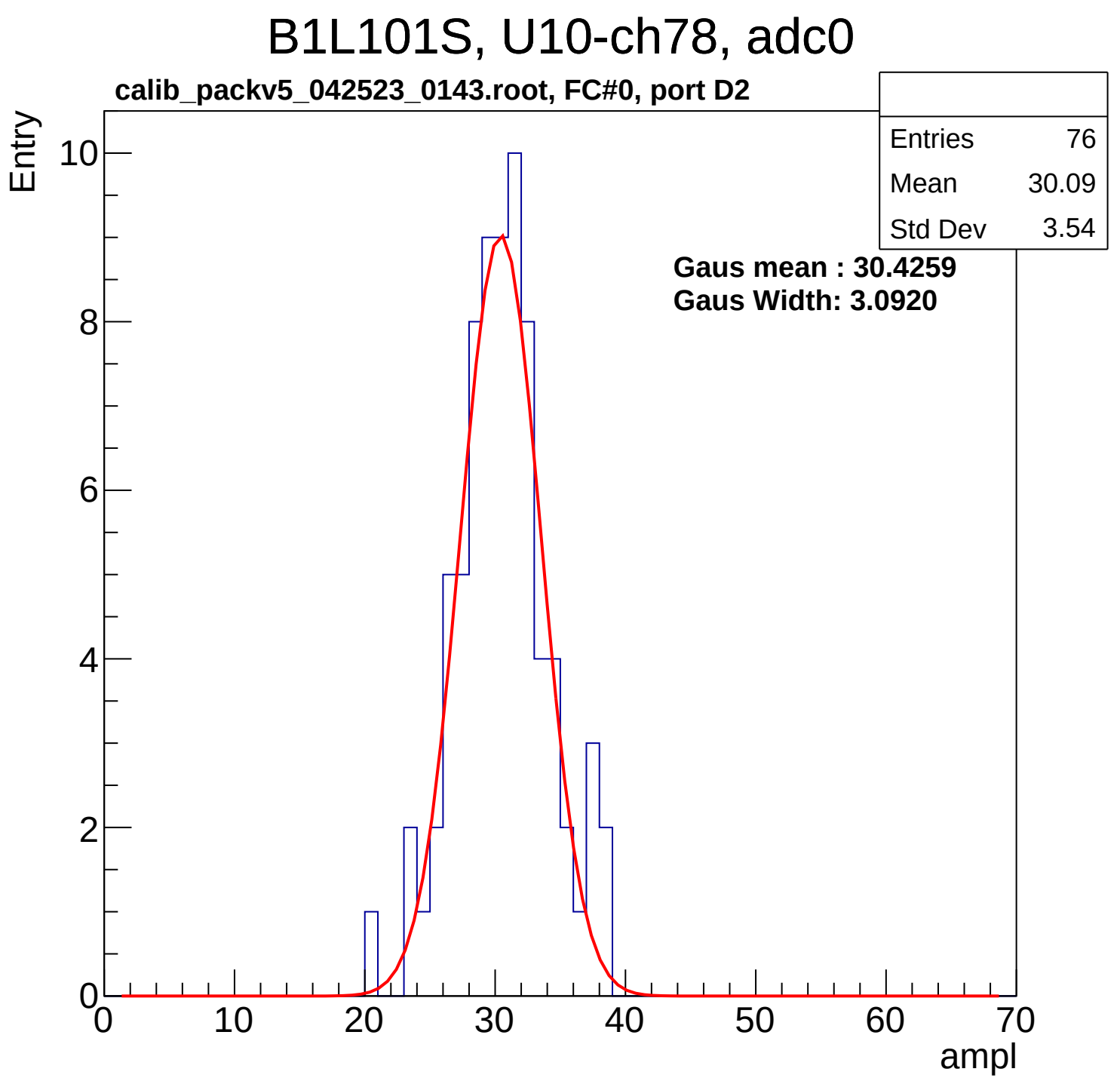

B1L101S, U10-ch77, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 49.61
Std Dev 2.975
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

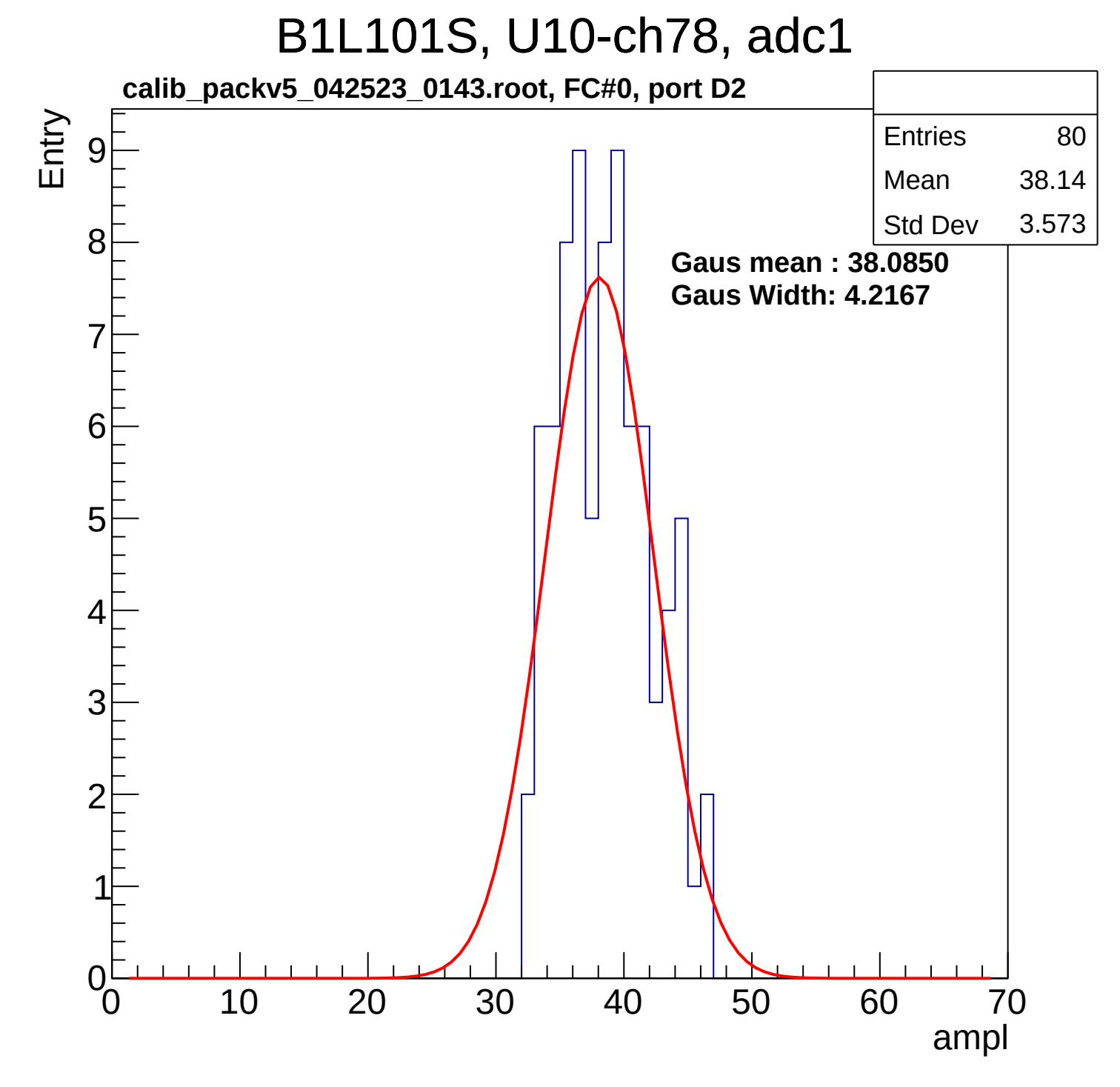

B1L101S, U10-ch77, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 55.37
Std Dev 2.595
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

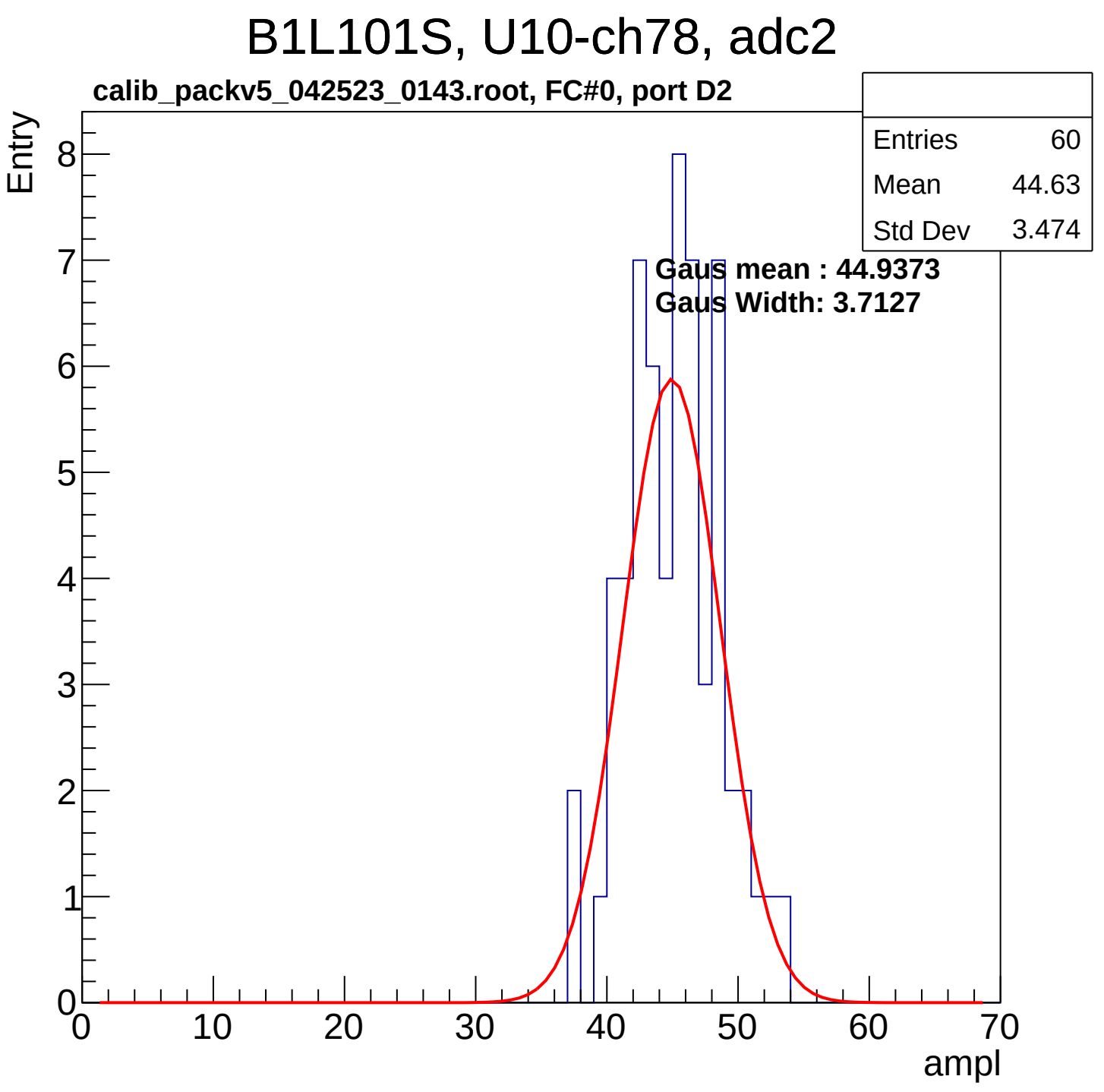

B1L101S, U10-ch77, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 60.12
Std Dev 2.382
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

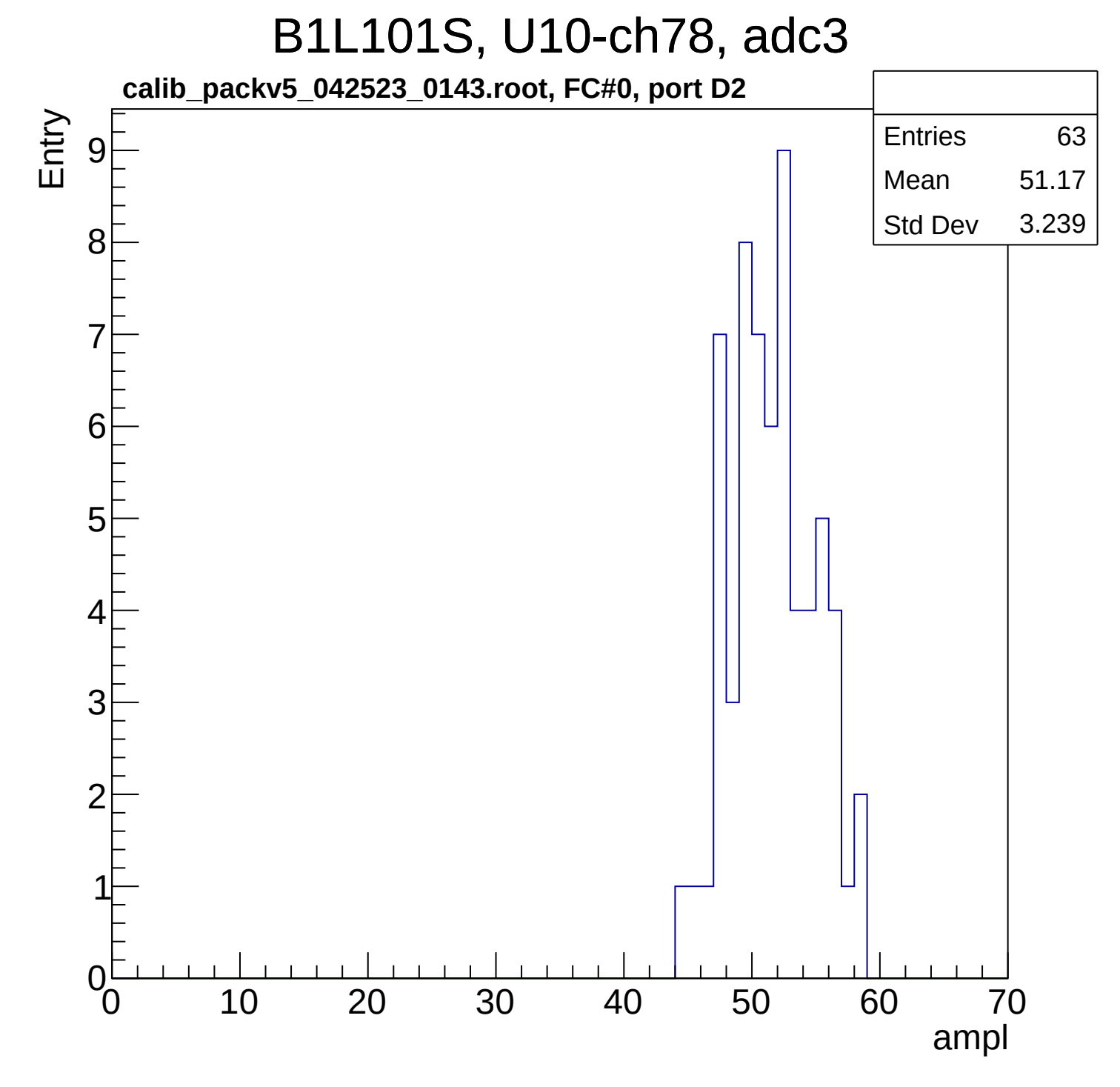

B1L101S, U10-ch77, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 50.83
Std Dev 22.75
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U10-ch77, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch78, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 30.09
Std Dev 3.54
Gaus mean : 30.4259
Gaus Width: 3.0920
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch78, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 80
Mean 38.14
Std Dev 3.573
Gaus mean : 38.0850
Gaus Width: 4.2167
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch78, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 44.63
Std Dev 3.474
Gaus mean : 44.9373
Gaus Width: 3.7127
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch78, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 51.17
Std Dev 3.239
Entry
ampl
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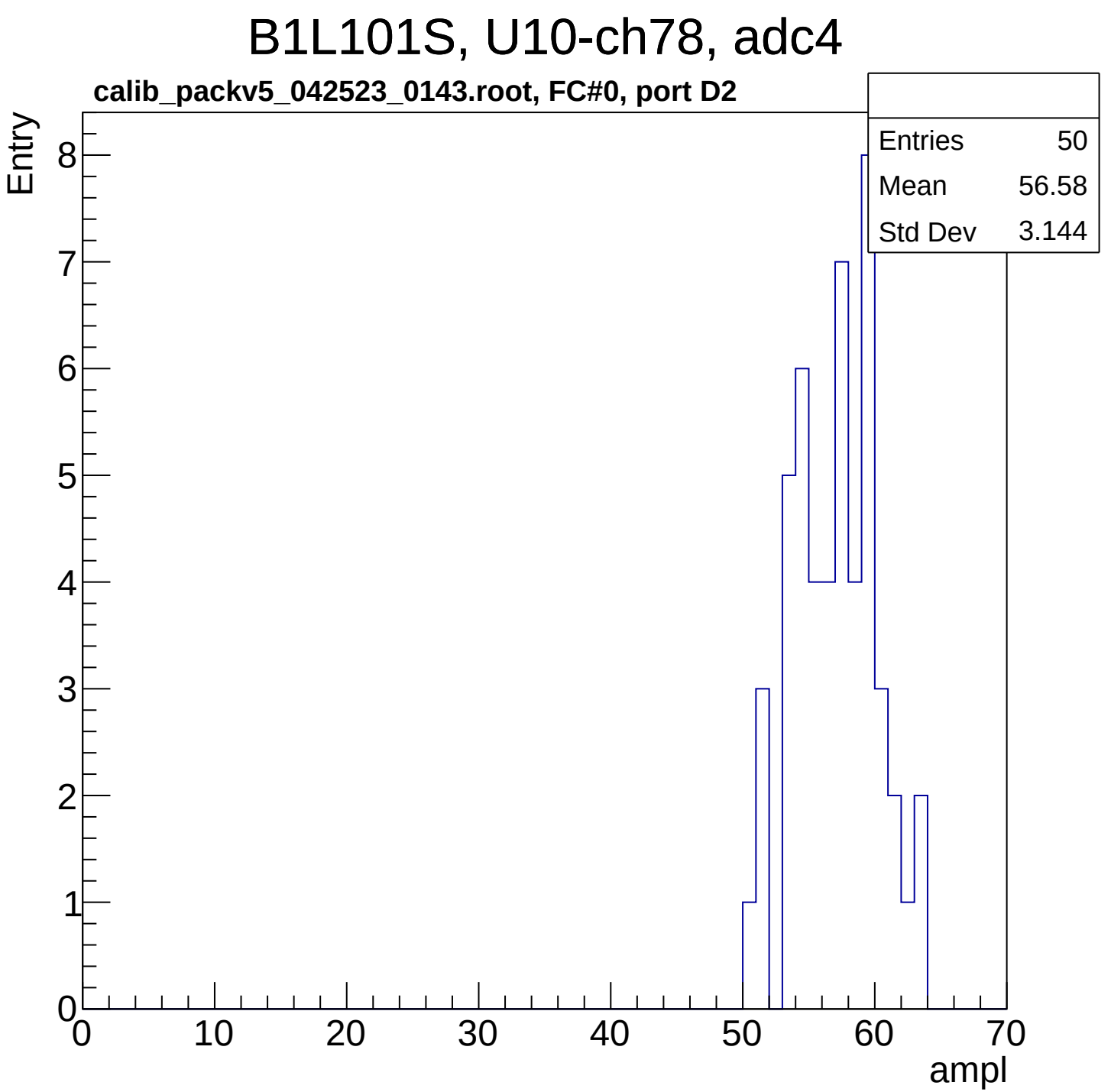
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch78, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 56.58
Std Dev 3.144
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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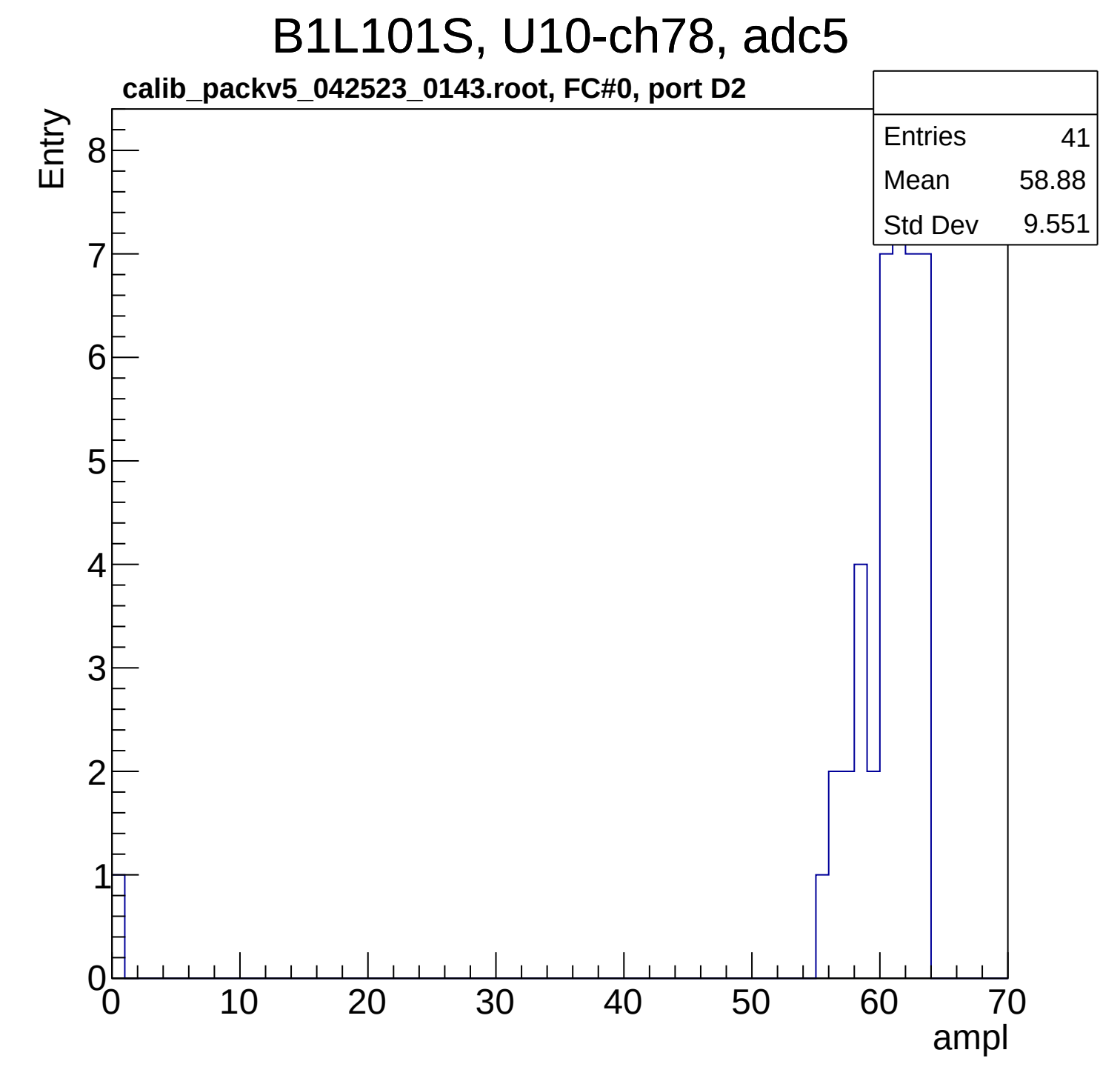
B1L101S, U10-ch78, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 41
Mean 58.88
Std Dev 9.551
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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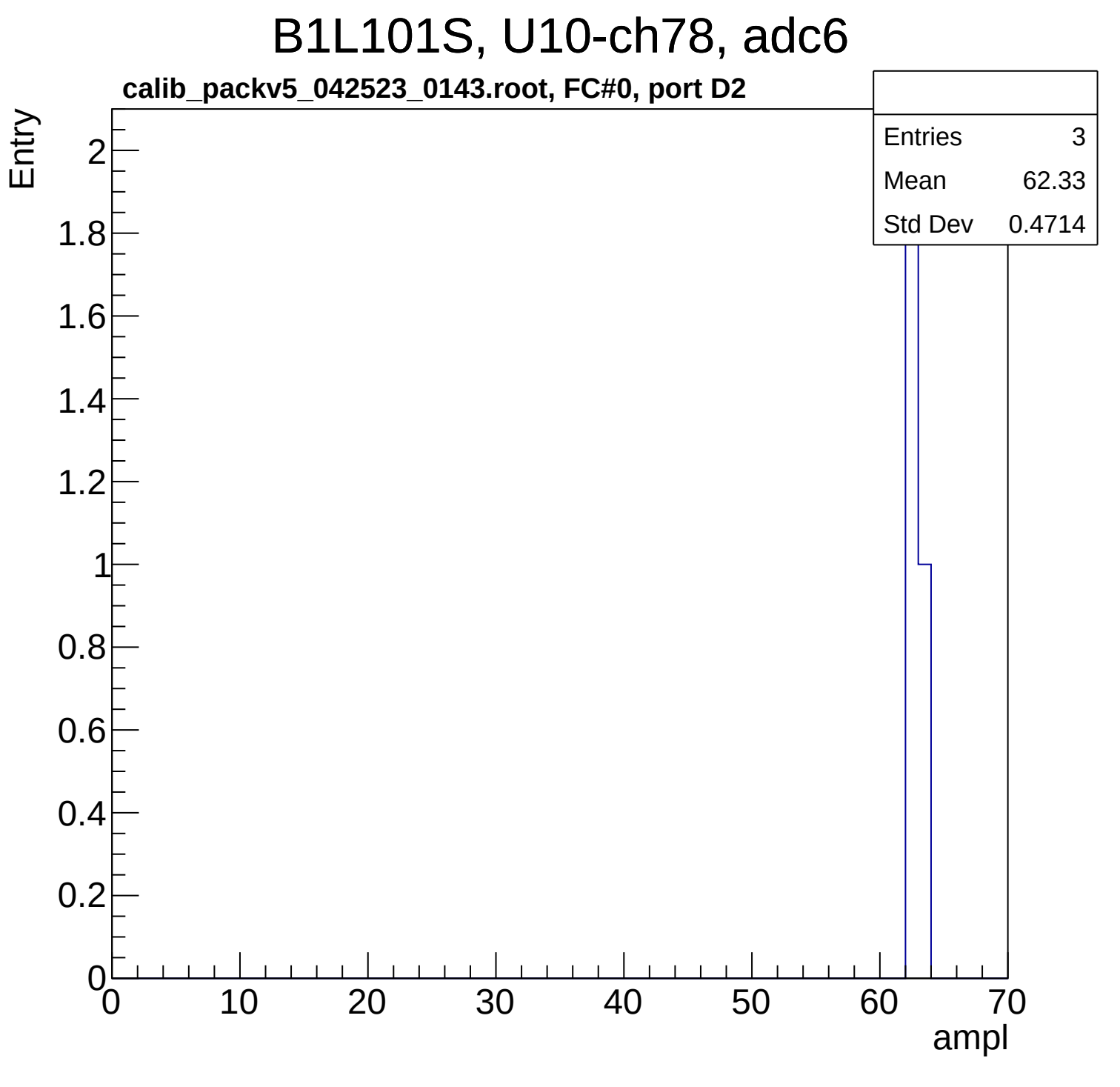
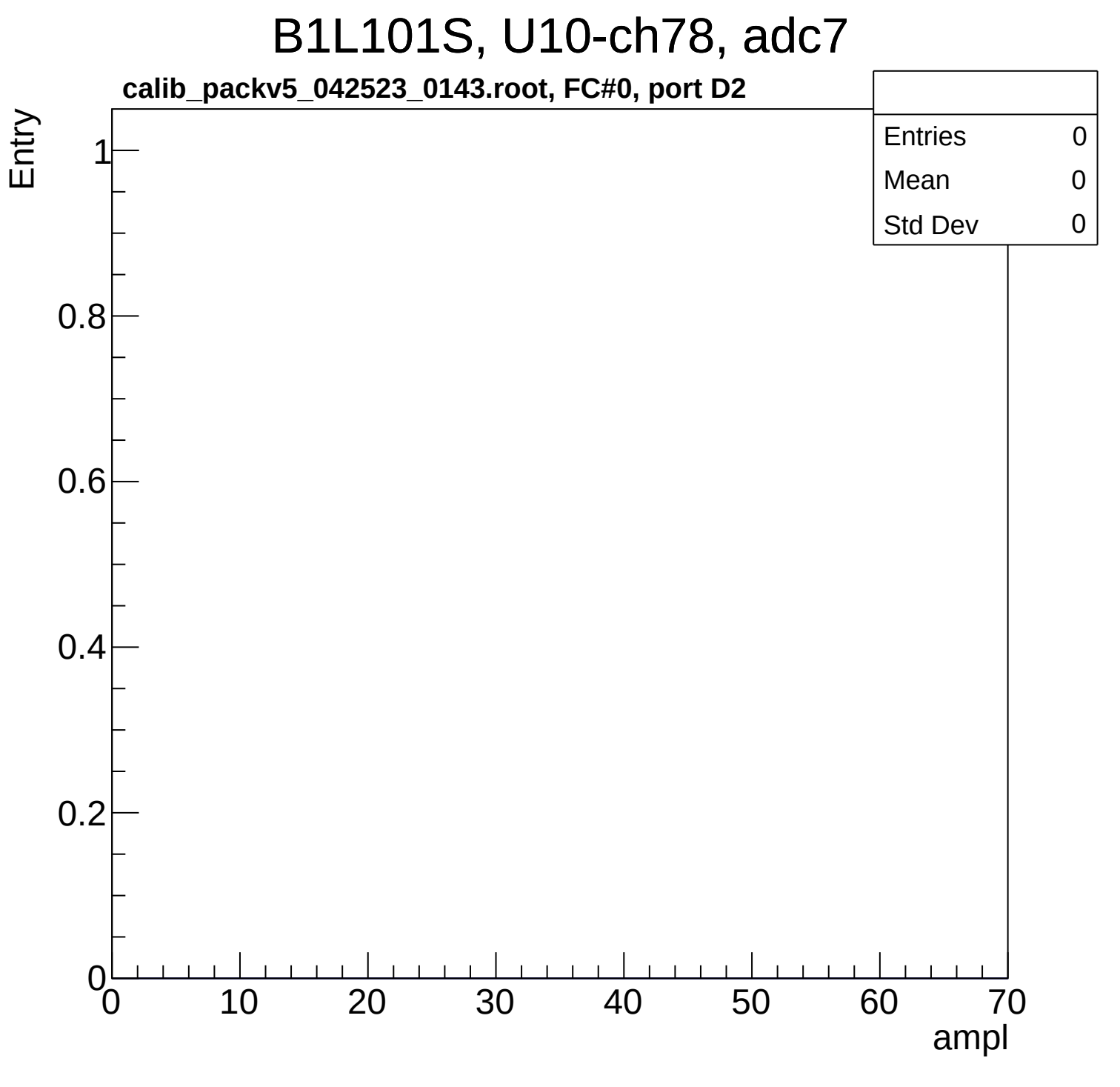
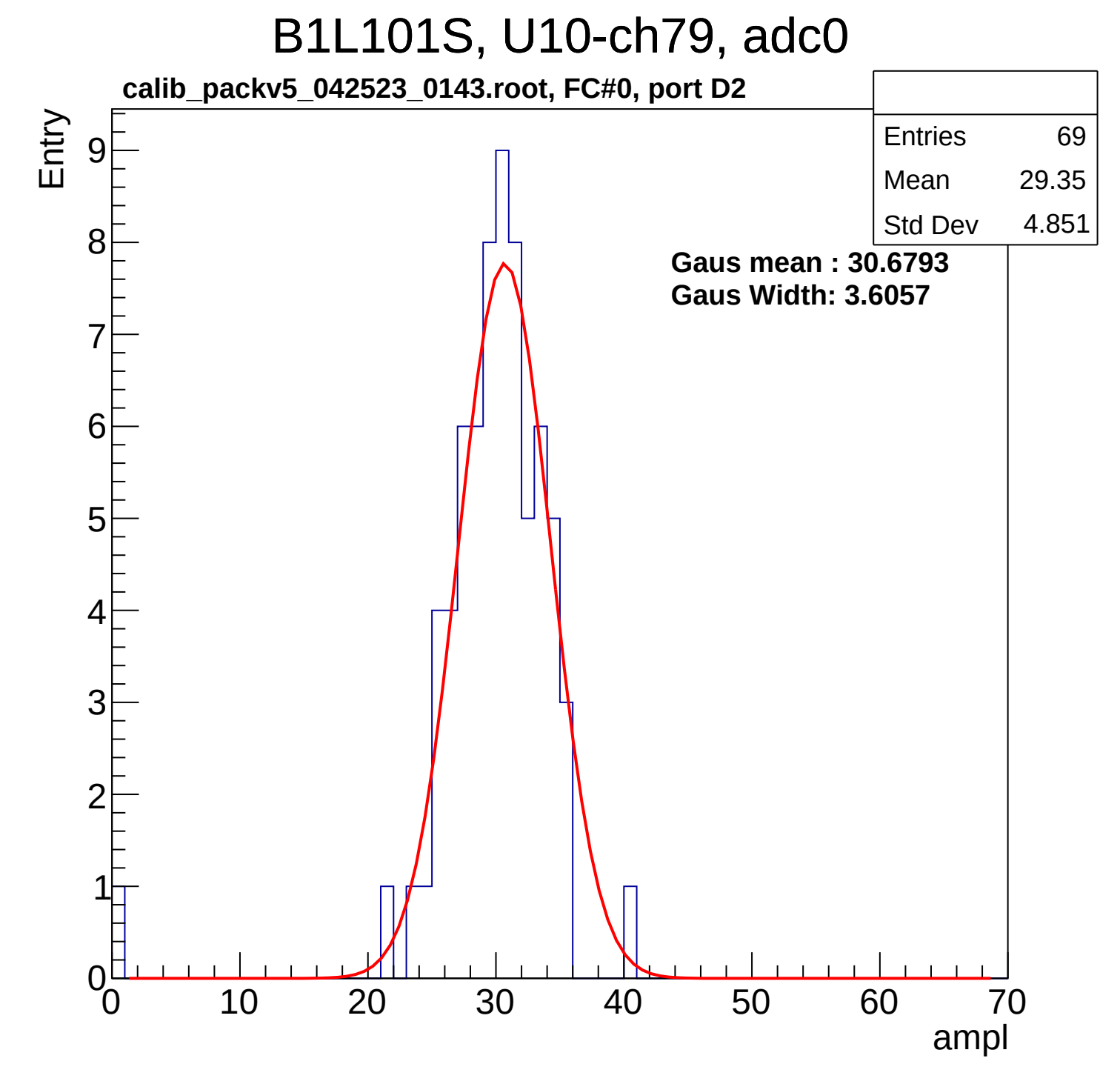

B1L101S, U10-ch78, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U10-ch78, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch79, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 29.35
Std Dev 4.851
Gaus mean : 30.6793
Gaus Width: 3.6057
Entry
ampl
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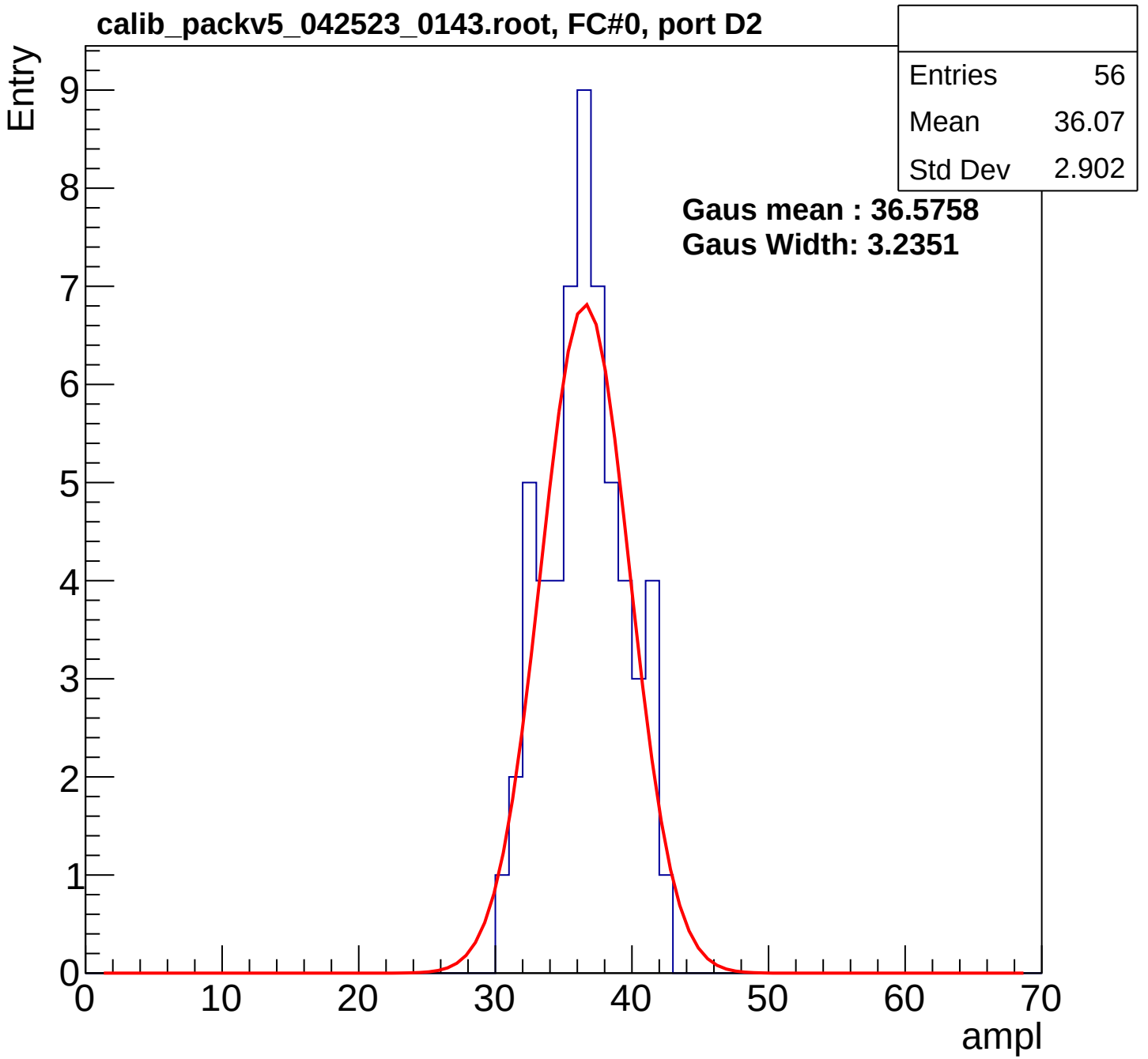
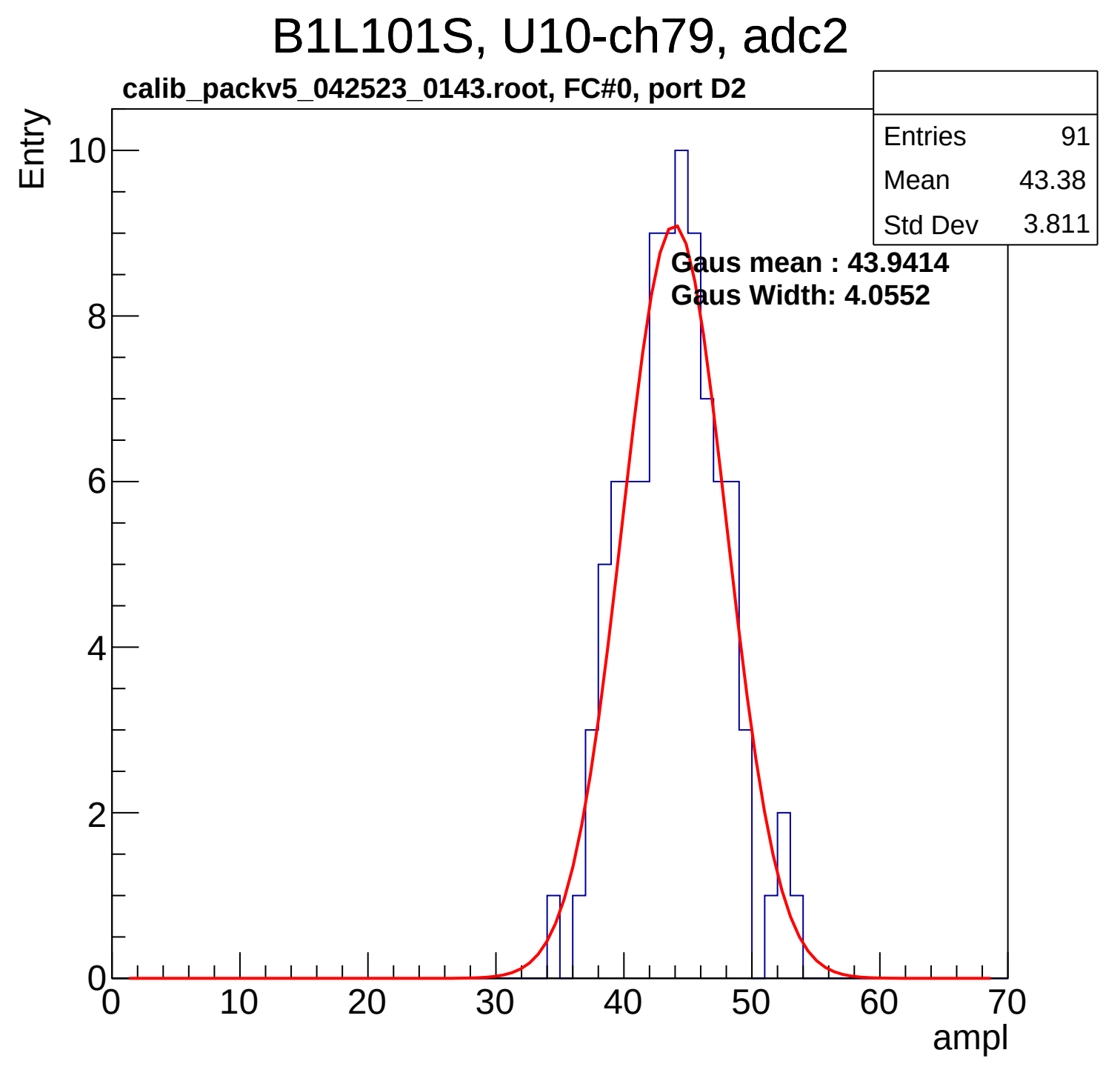
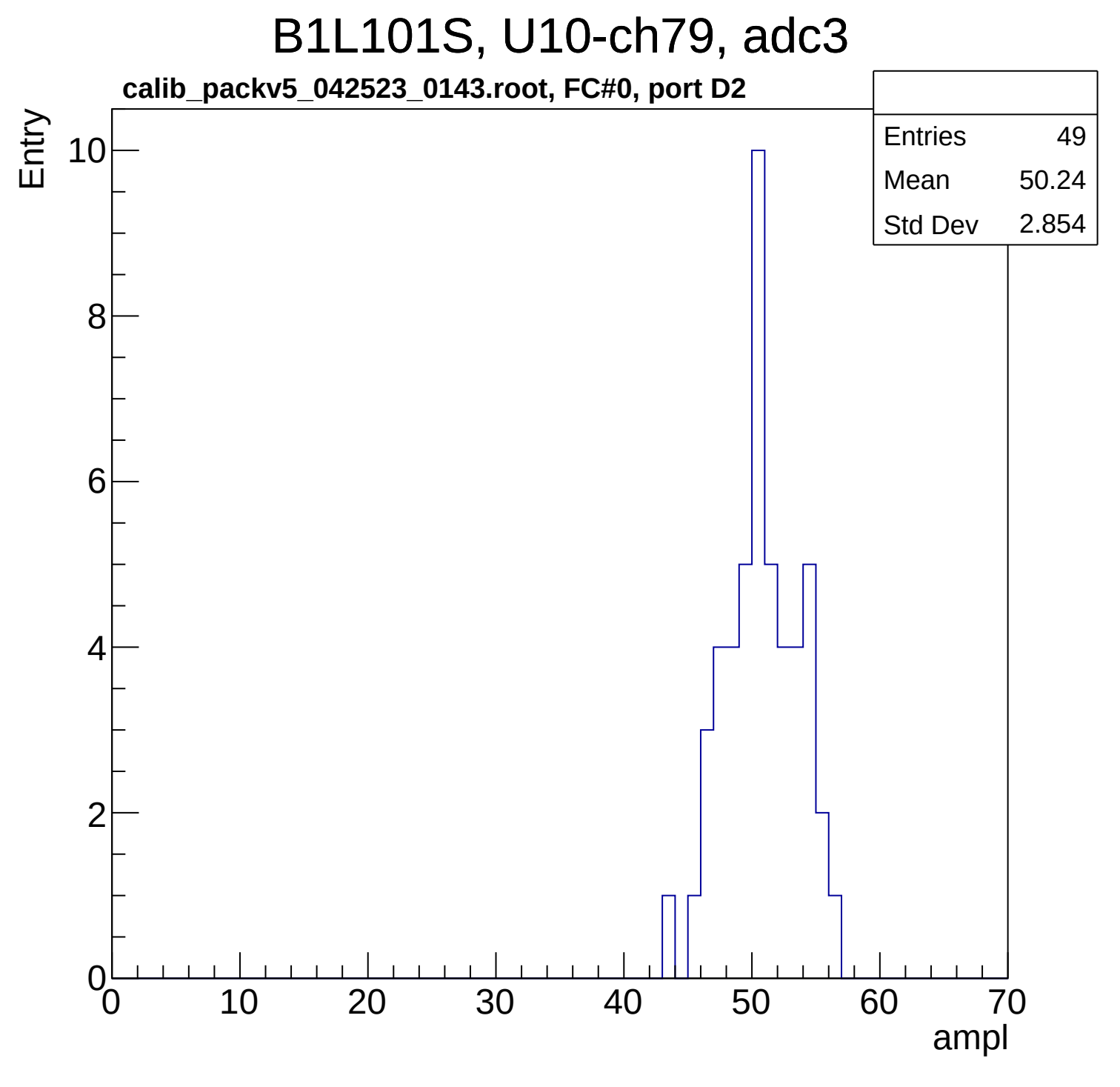
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch79, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 36.07
Std Dev 2.902
Gaus mean : 36.5758
Gaus Width: 3.2351
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch79, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 91
Mean 43.38
Std Dev 3.811
Gaus mean : 43.9414
Gaus Width: 4.0552
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch79, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 50.24
Std Dev 2.854
Entry
ampl
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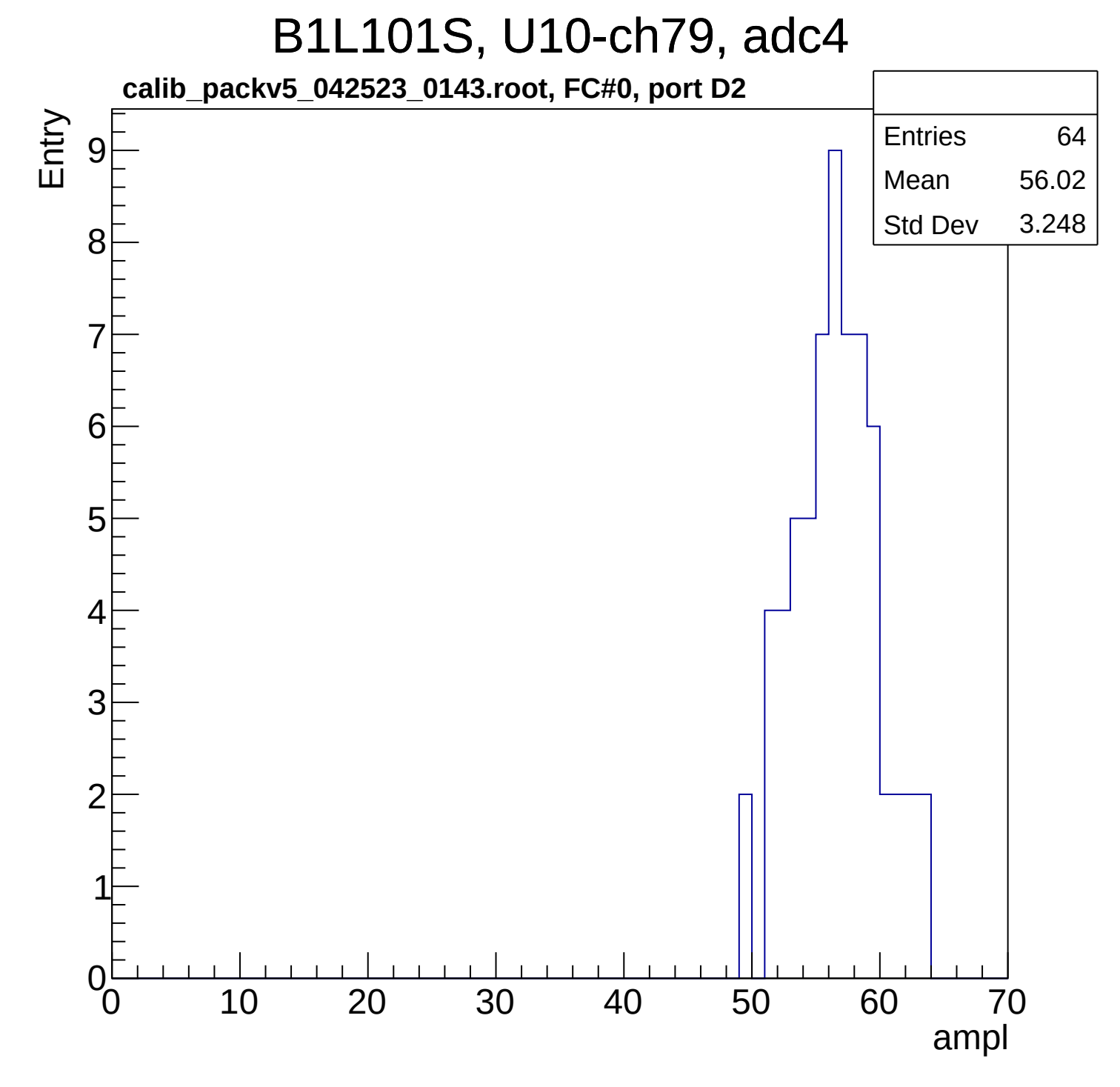
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch79, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 56.02
Std Dev 3.248
Entry
ampl
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5
6
7
8
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0
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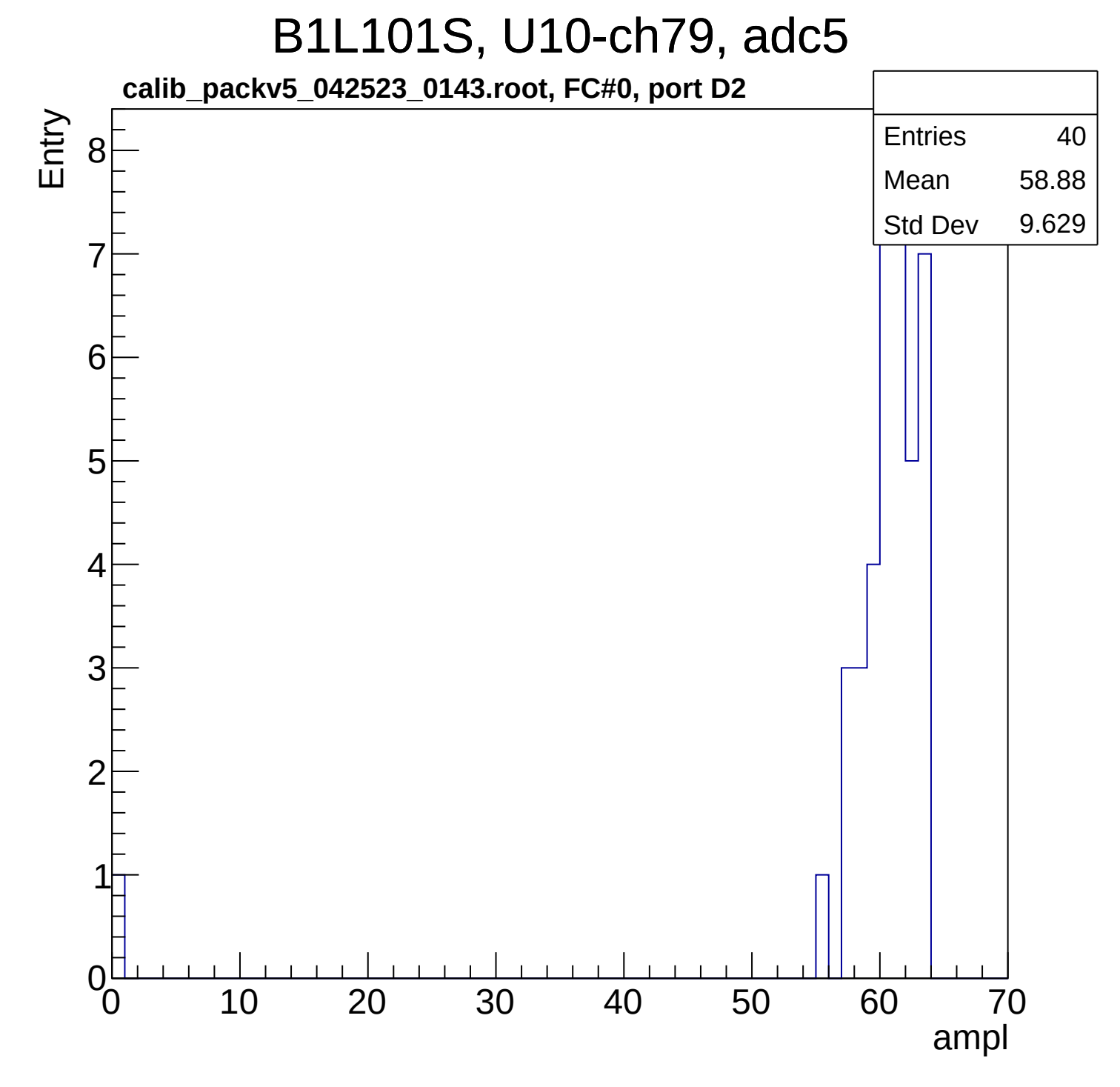
60
70


B1L101S, U10-ch79, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 40
Mean 58.88
Std Dev 9.629
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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40
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60
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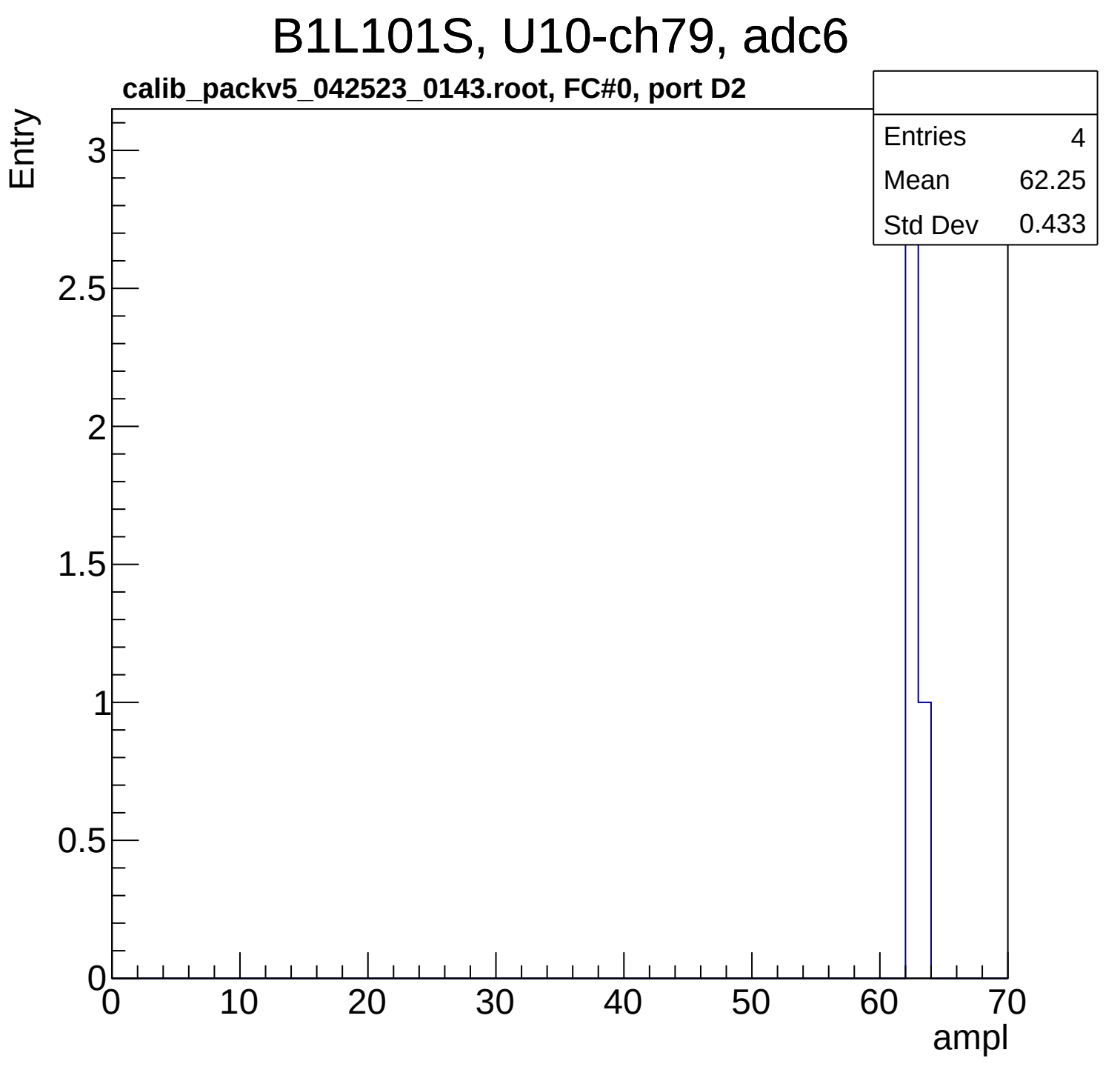
B1L101S, U10-ch79, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 62.25
Std Dev 0.433
Entry
ampl
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0.5
1
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2
2.5
3
0
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20
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40
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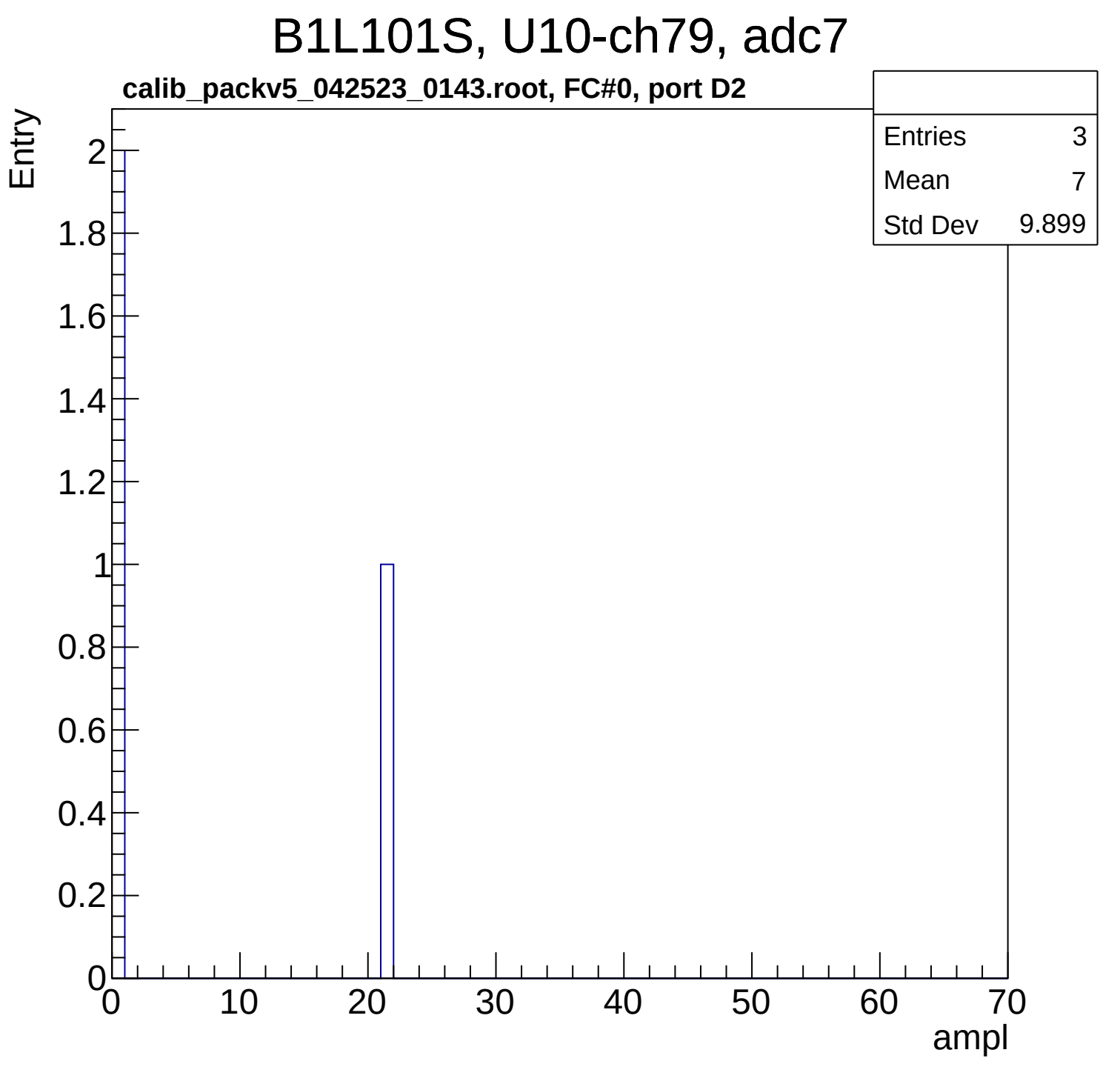
60
70


B1L101S, U10-ch79, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 7
Std Dev 9.899
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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20
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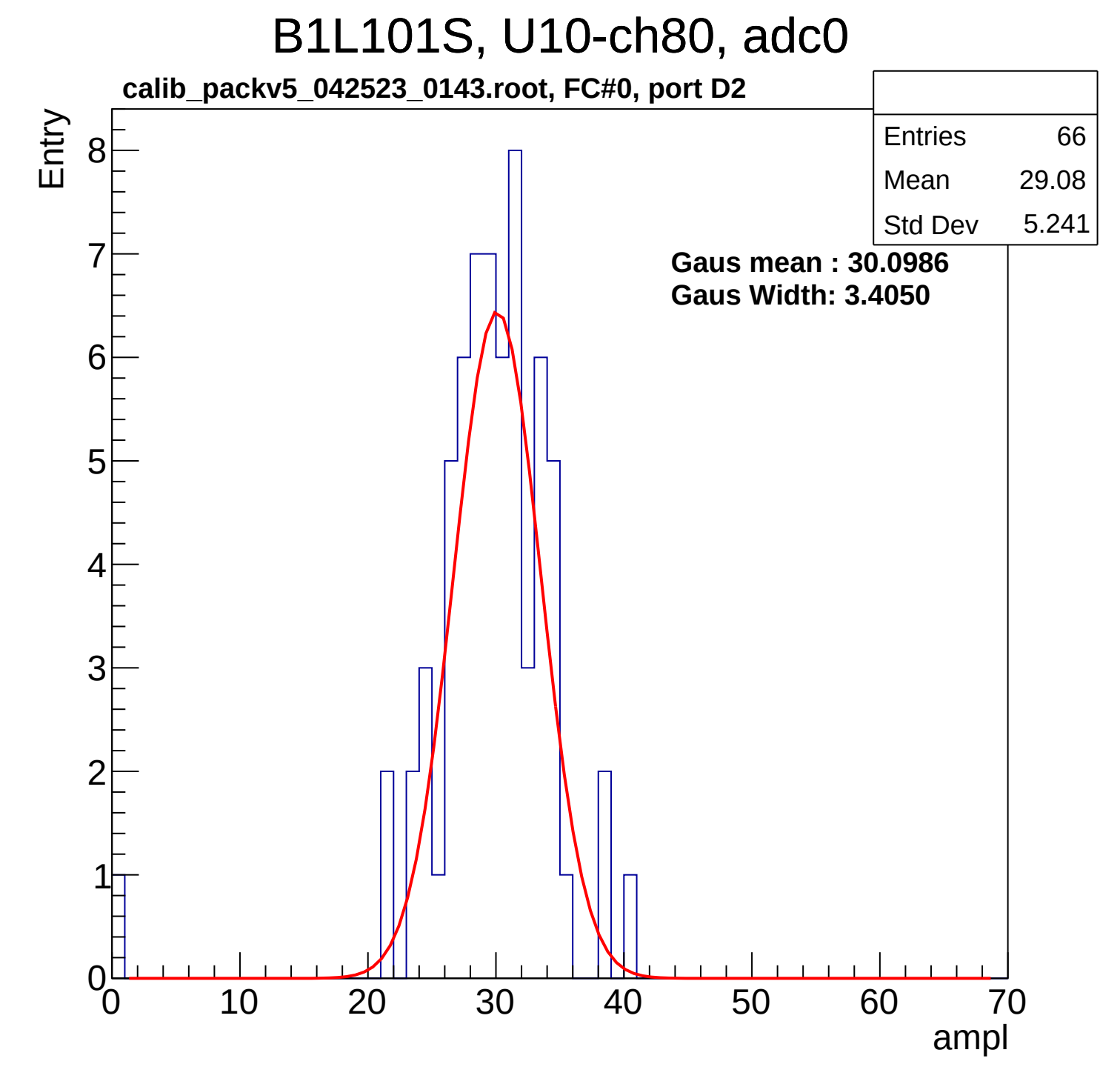
40
50
60
70


B1L101S, U10-ch80, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 29.08
Std Dev 5.241
Gaus mean : 30.0986
Gaus Width: 3.4050
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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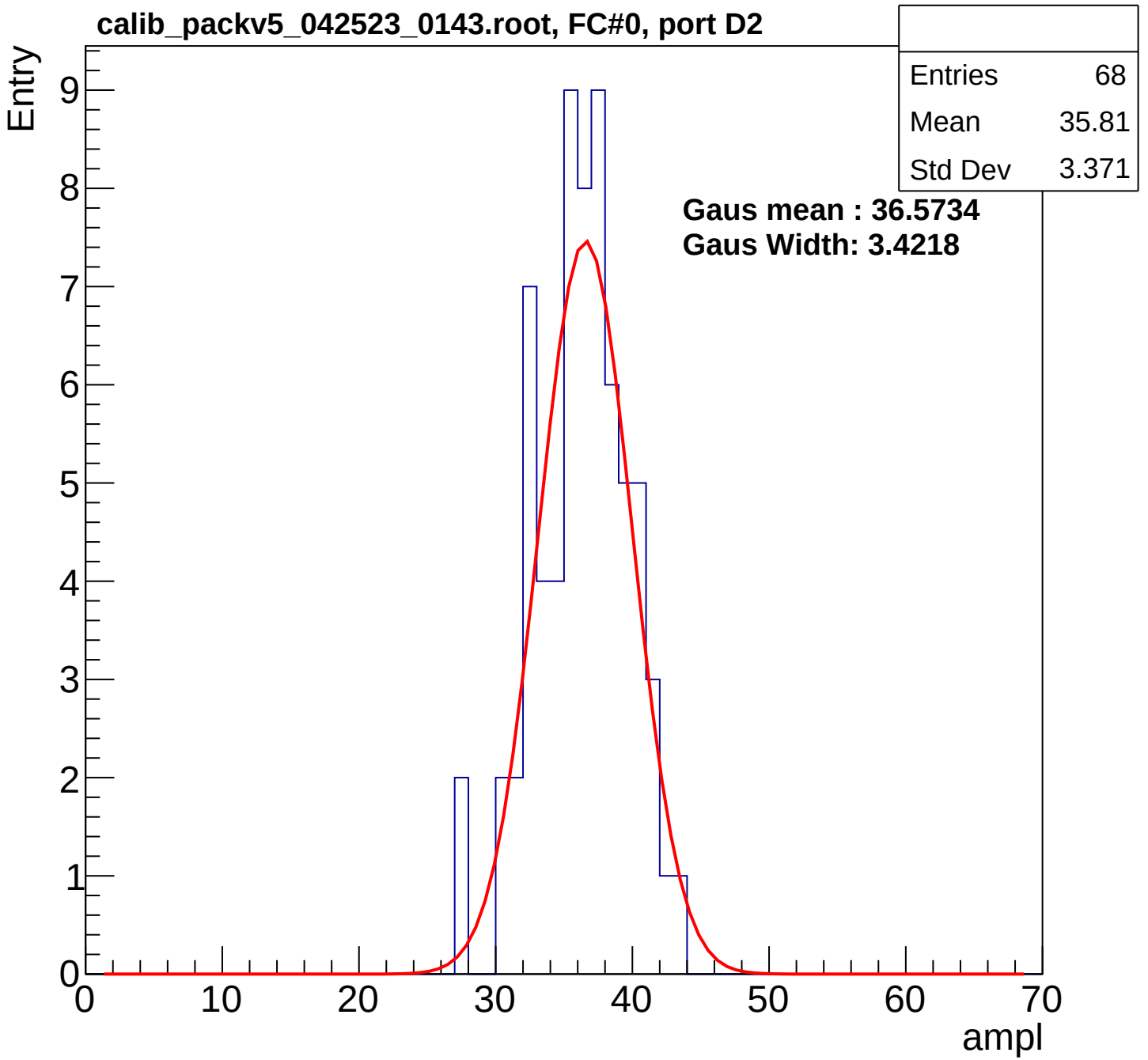
B1L101S, U10-ch80, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 35.81
Std Dev 3.371
Gaus mean : 36.5734
Gaus Width: 3.4218
Entry
ampl
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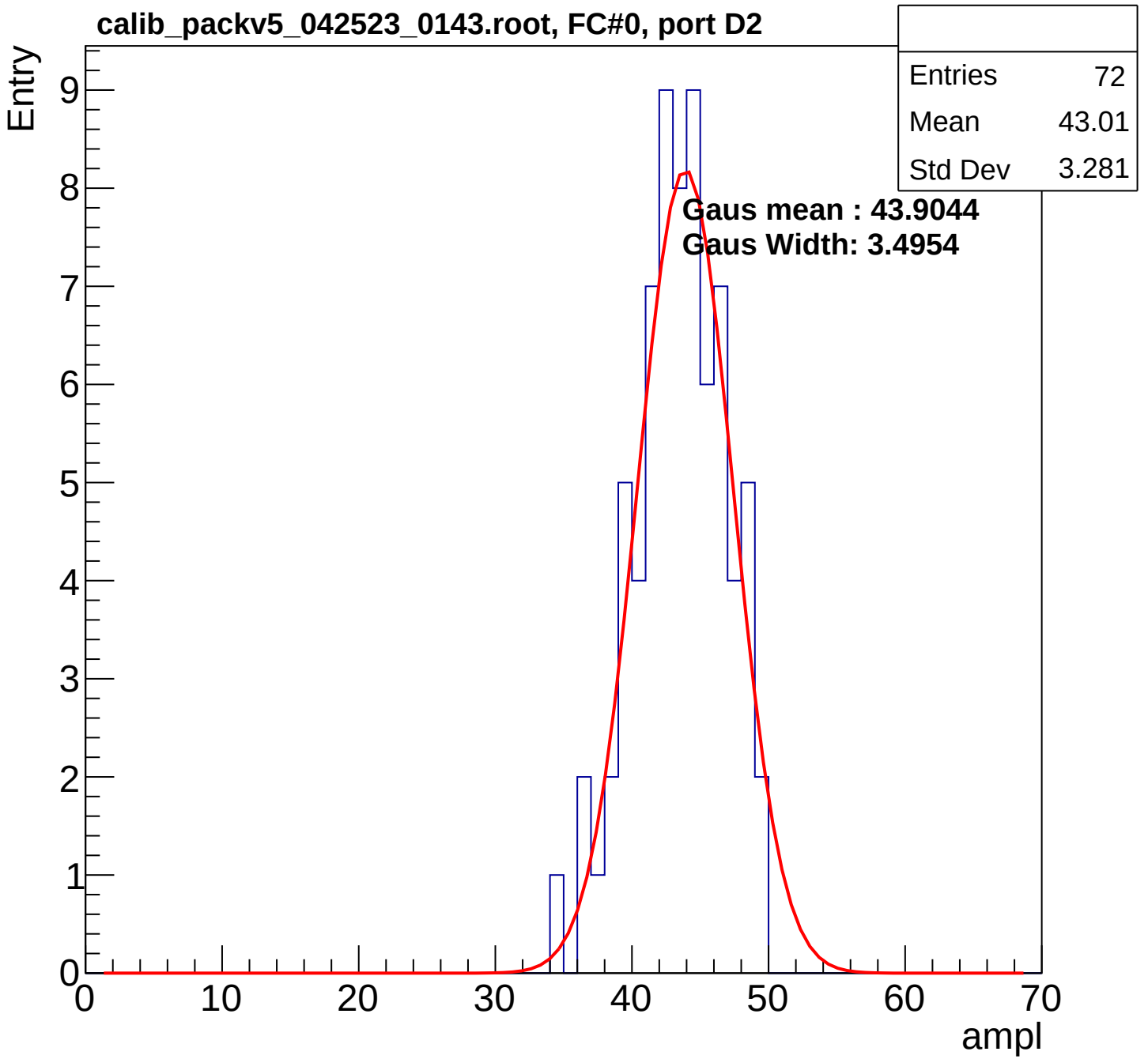
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch80, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 43.01
Std Dev 3.281
Gaus mean : 43.9044
Gaus Width: 3.4954
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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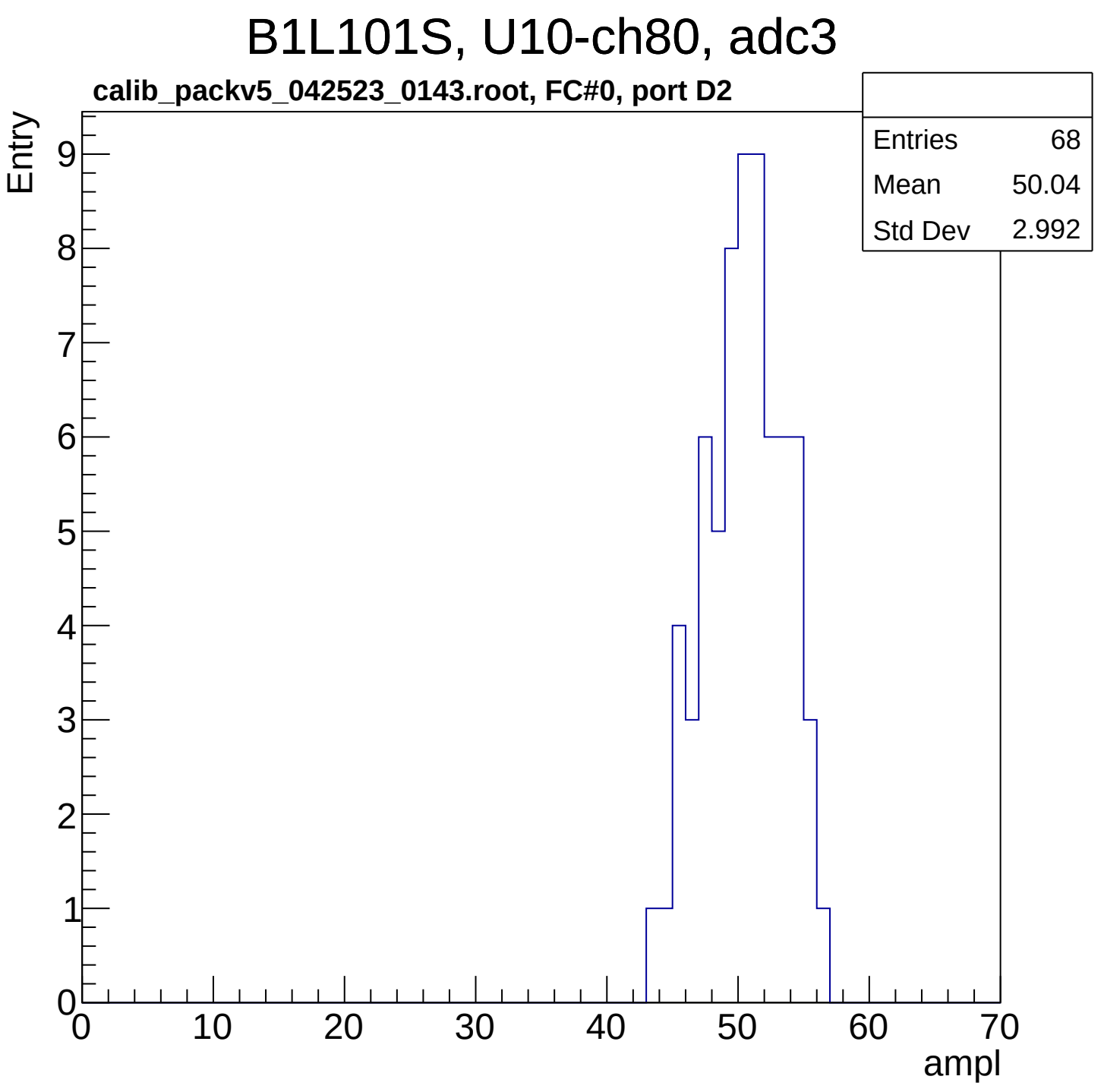
B1L101S, U10-ch80, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 50.04
Std Dev 2.992
Entry
ampl
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3
4
5
6
7
8
9
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20
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40
50
60
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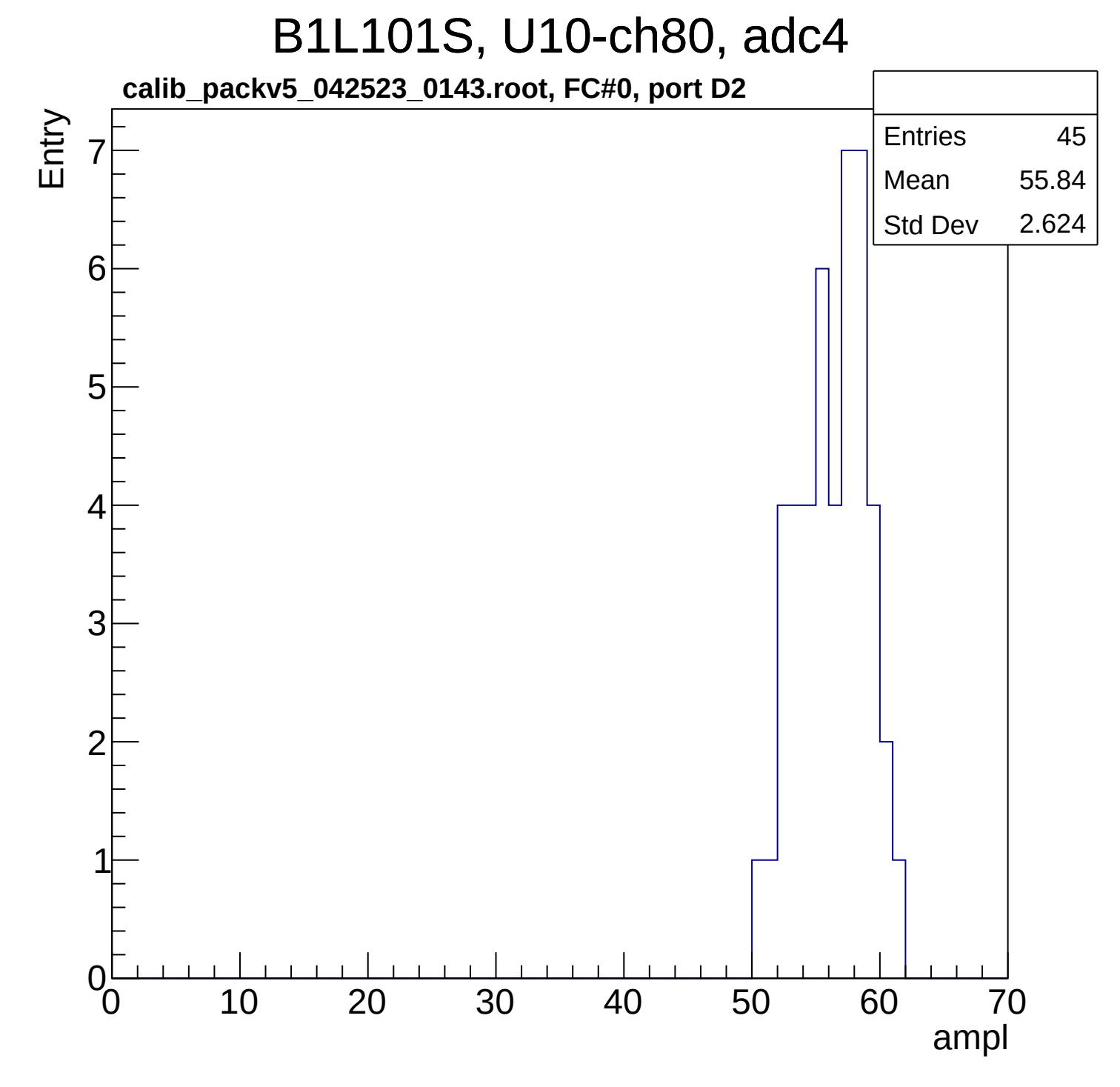
B1L101S, U10-ch80, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 55.84
Std Dev 2.624
Entry
ampl
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1
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3
4
5
6
7
0
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20
30
40
50
60
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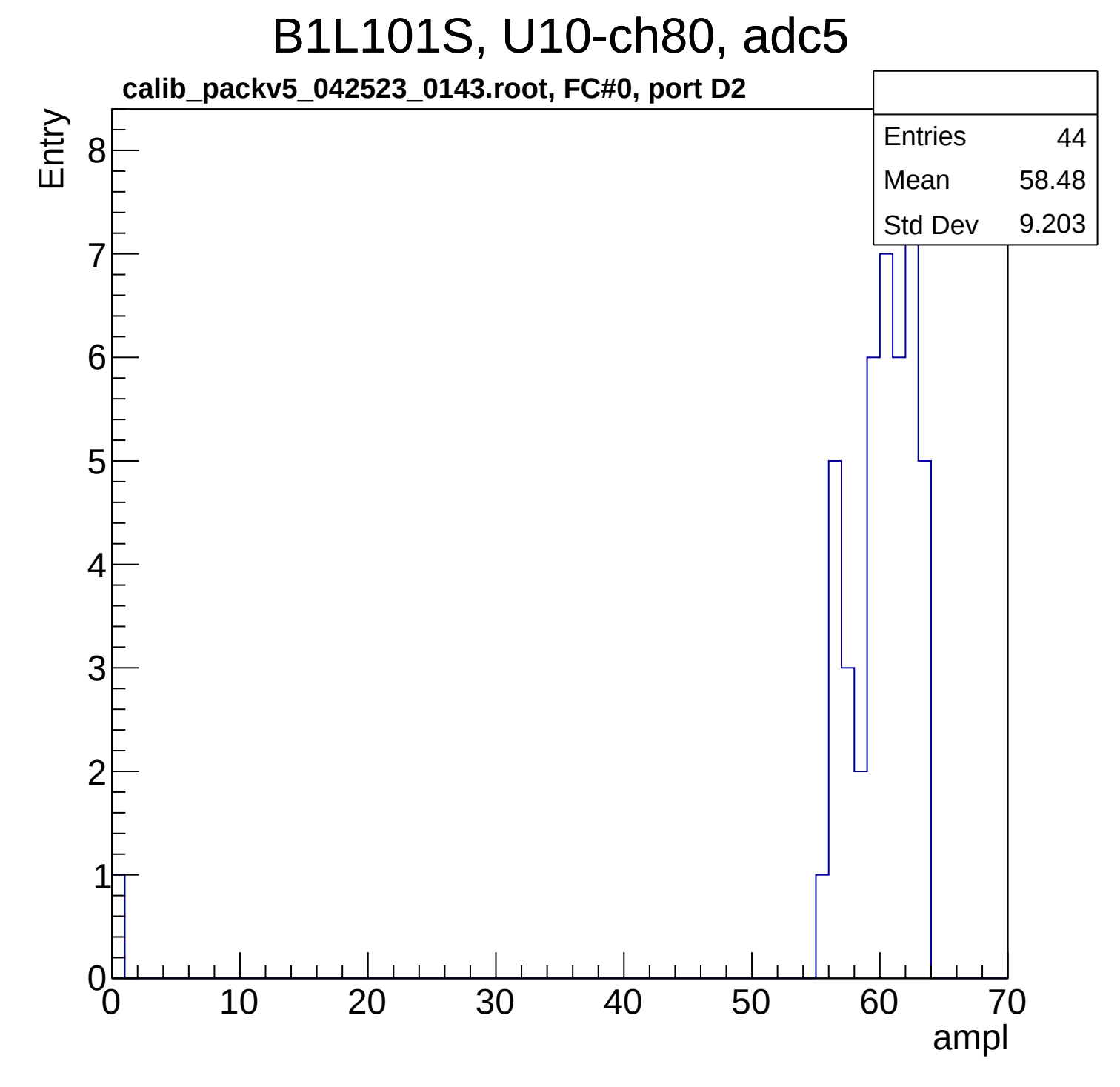
B1L101S, U10-ch80, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 44
Mean 58.48
Std Dev 9.203
Entry
ampl
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2
3
4
5
6
7
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20
30
40
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60
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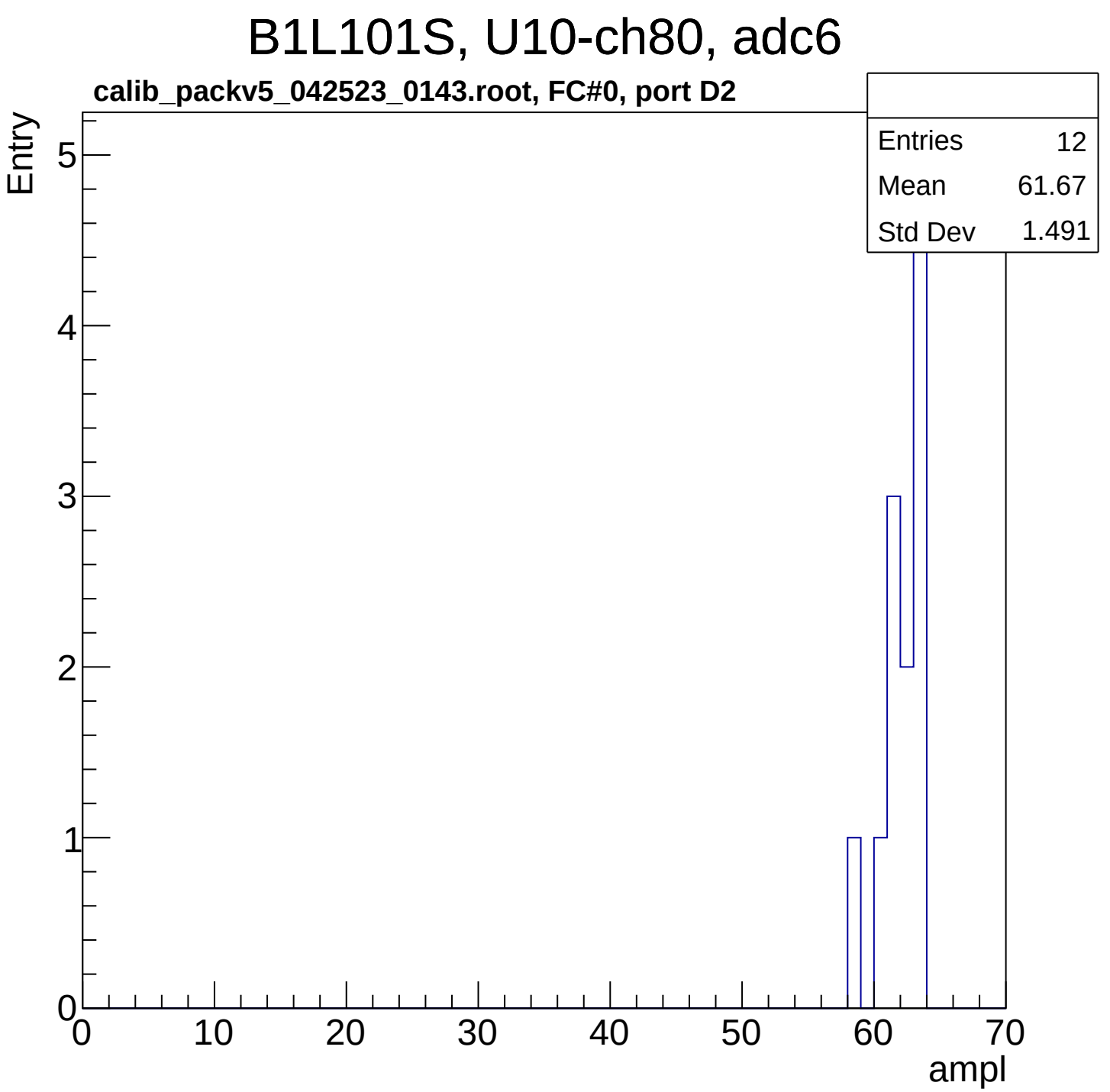
B1L101S, U10-ch80, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 12
Mean 61.67
Std Dev 1.491
Entry
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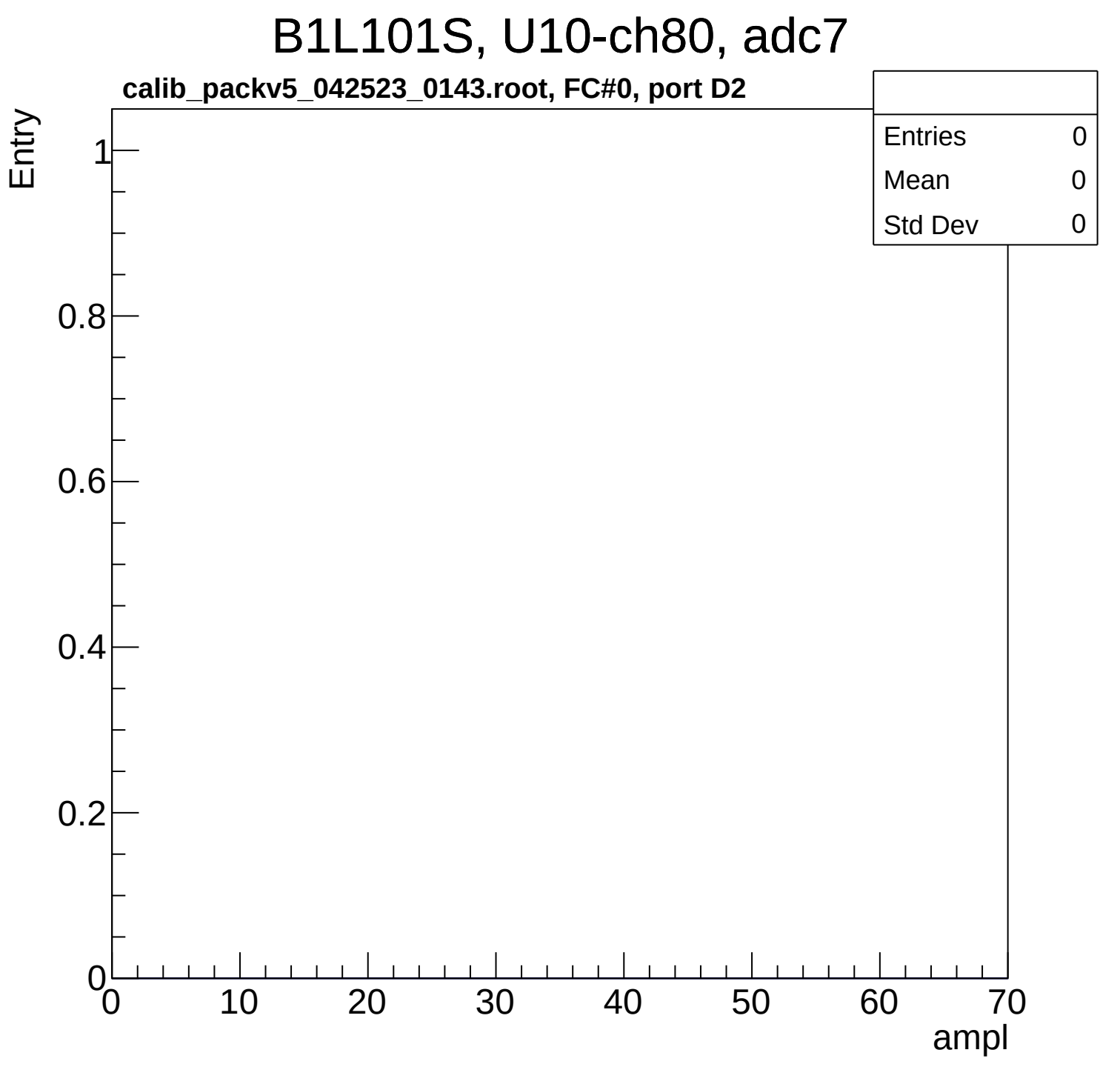
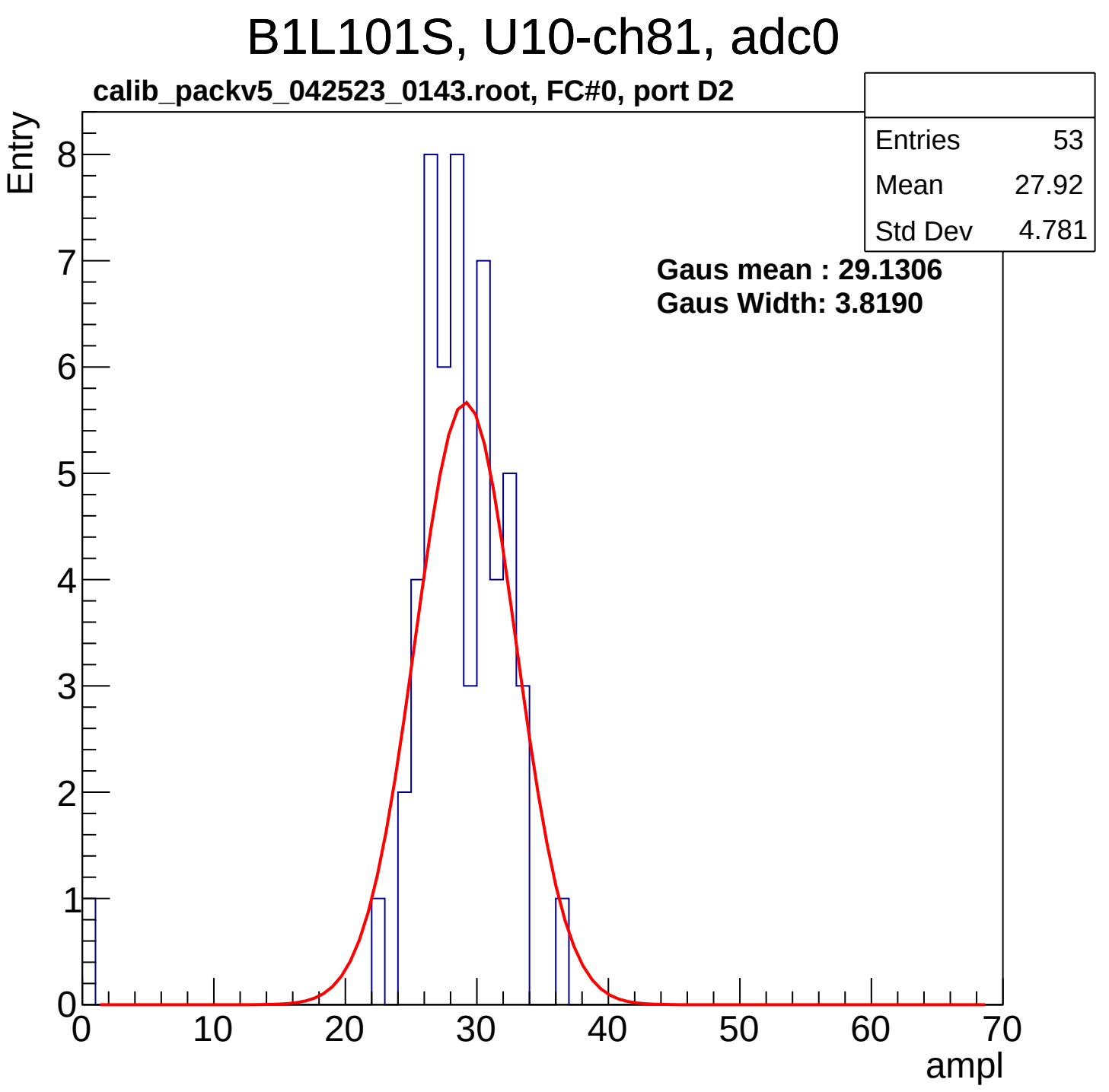
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch80, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch81, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 27.92
Std Dev 4.781
Gaus mean : 29.1306
Gaus Width: 3.8190
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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40
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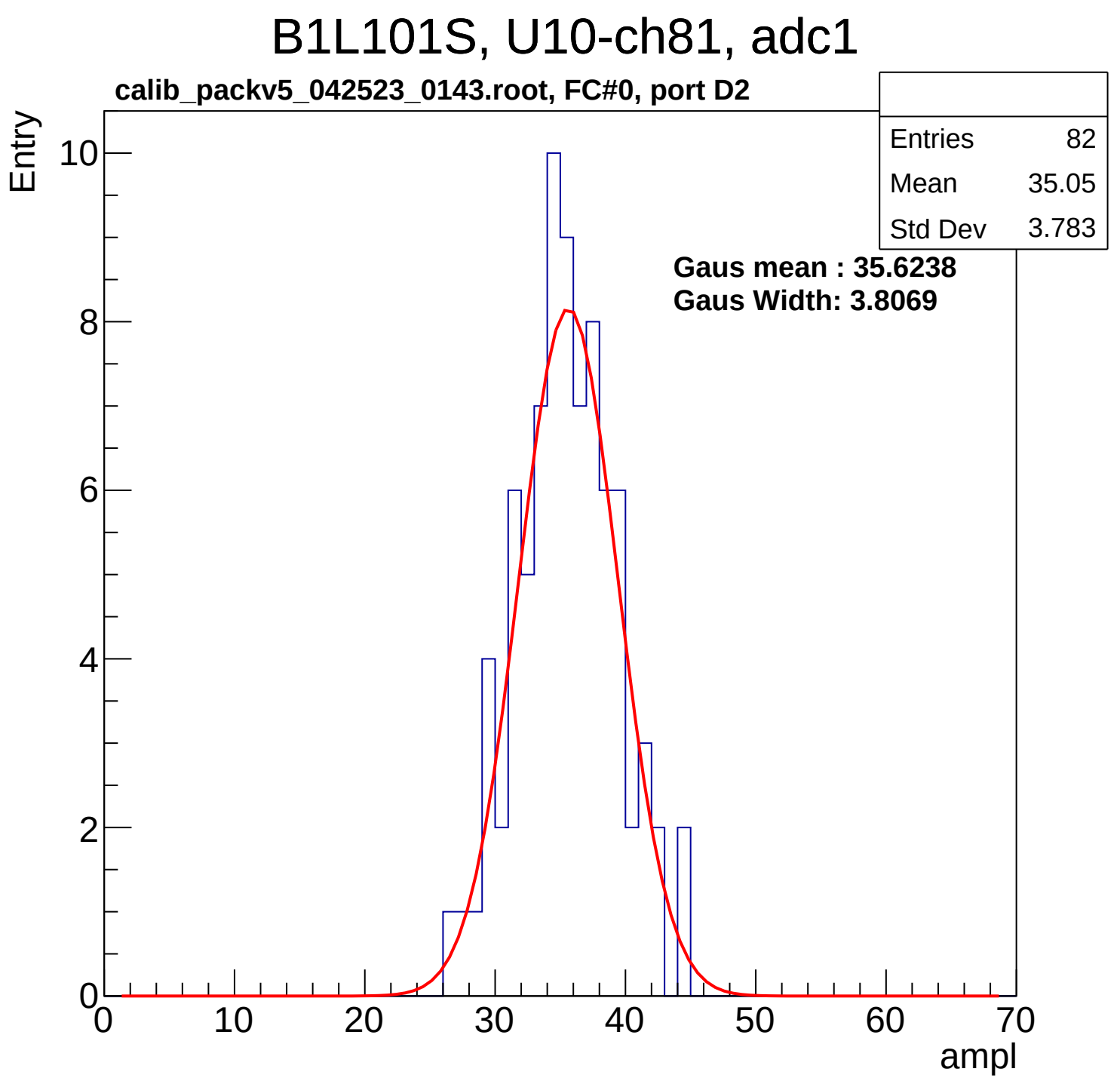
B1L101S, U10-ch81, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 82
Mean 35.05
Std Dev 3.783
Gaus mean : 35.6238
Gaus Width: 3.8069
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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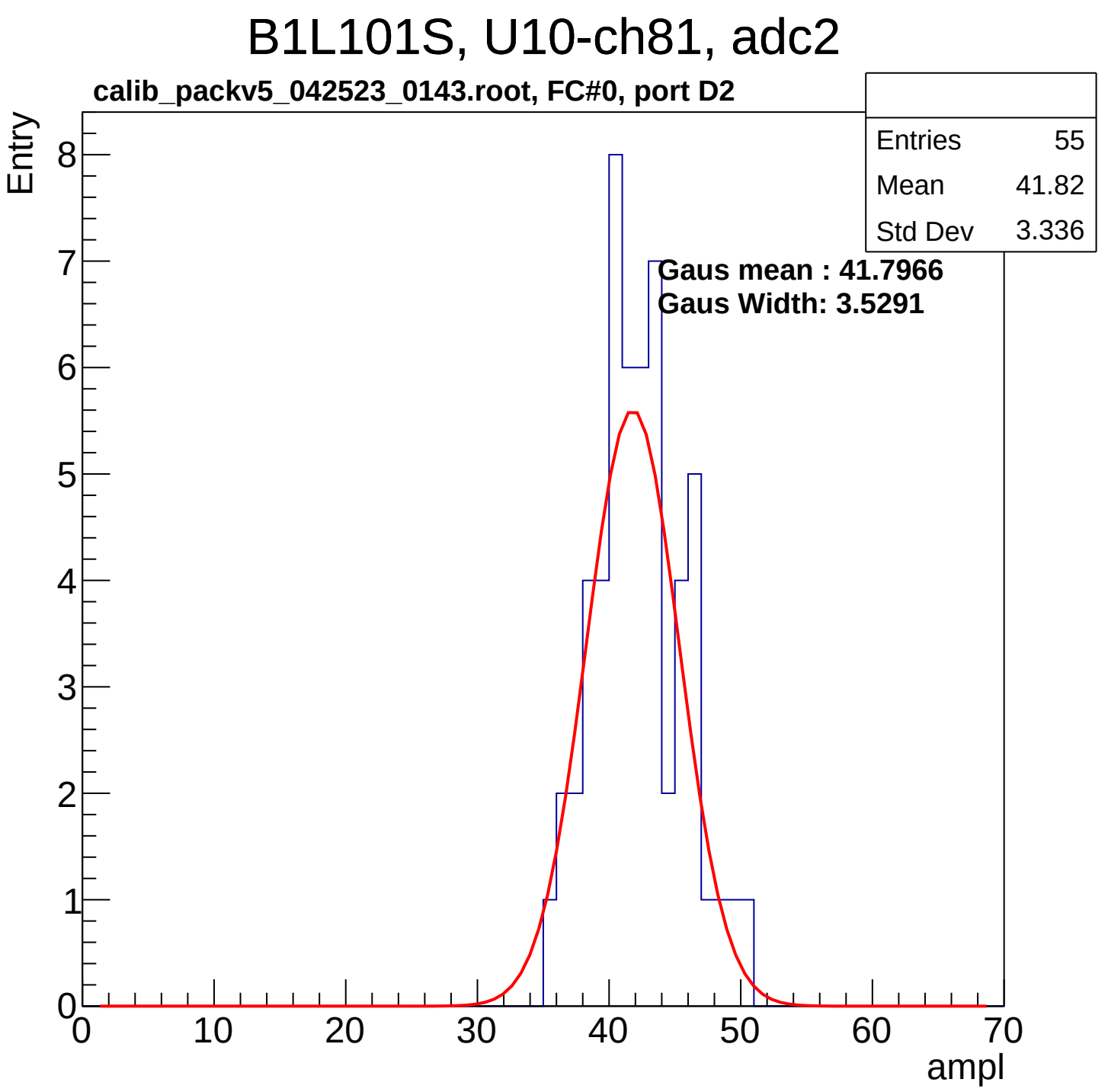
B1L101S, U10-ch81, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 41.82
Std Dev 3.336
Gaus mean : 41.7966
Gaus Width: 3.5291
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
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40
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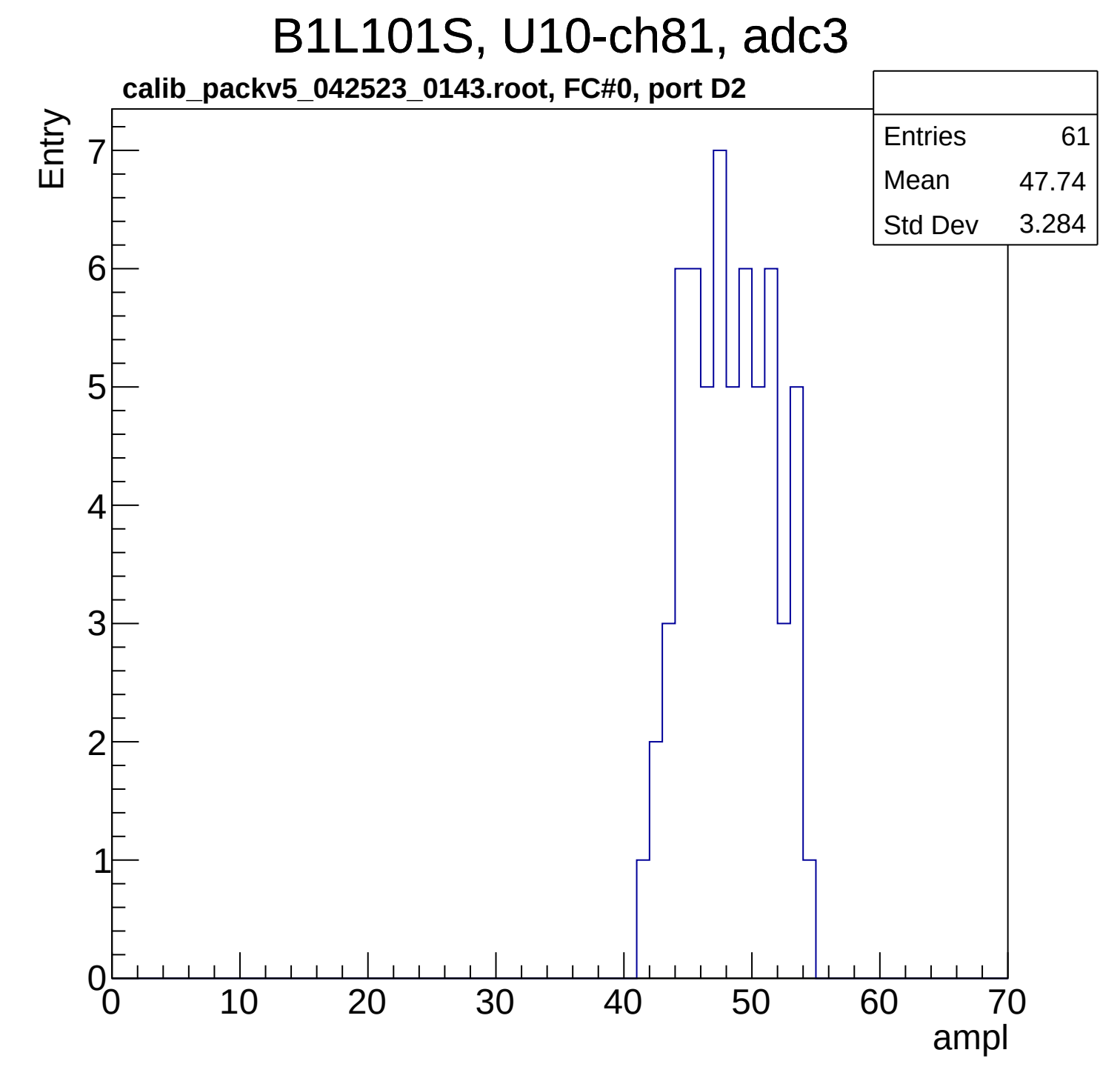
B1L101S, U10-ch81, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 47.74
Std Dev 3.284
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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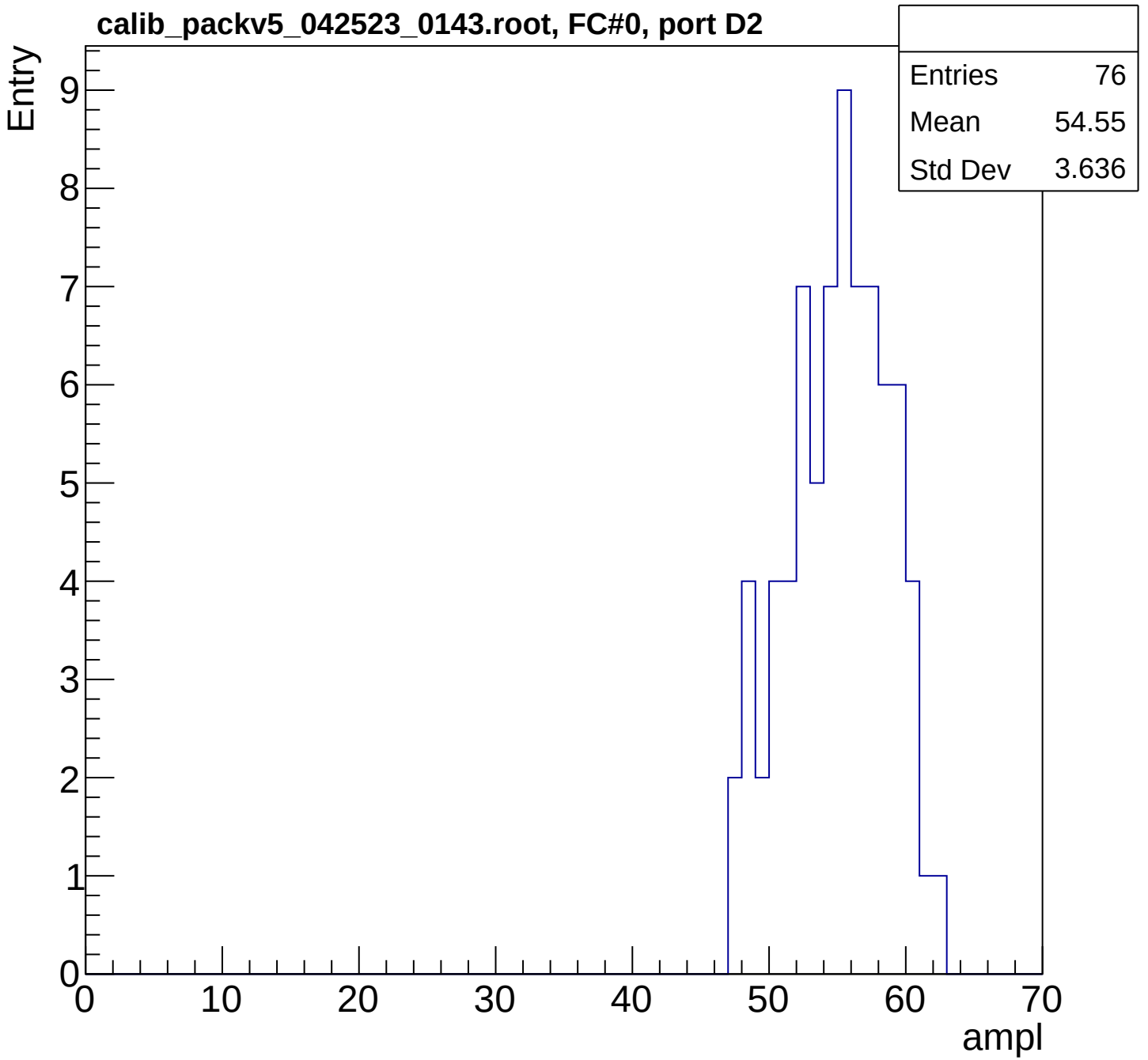
B1L101S, U10-ch81, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 54.55
Std Dev 3.636
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
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40
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60
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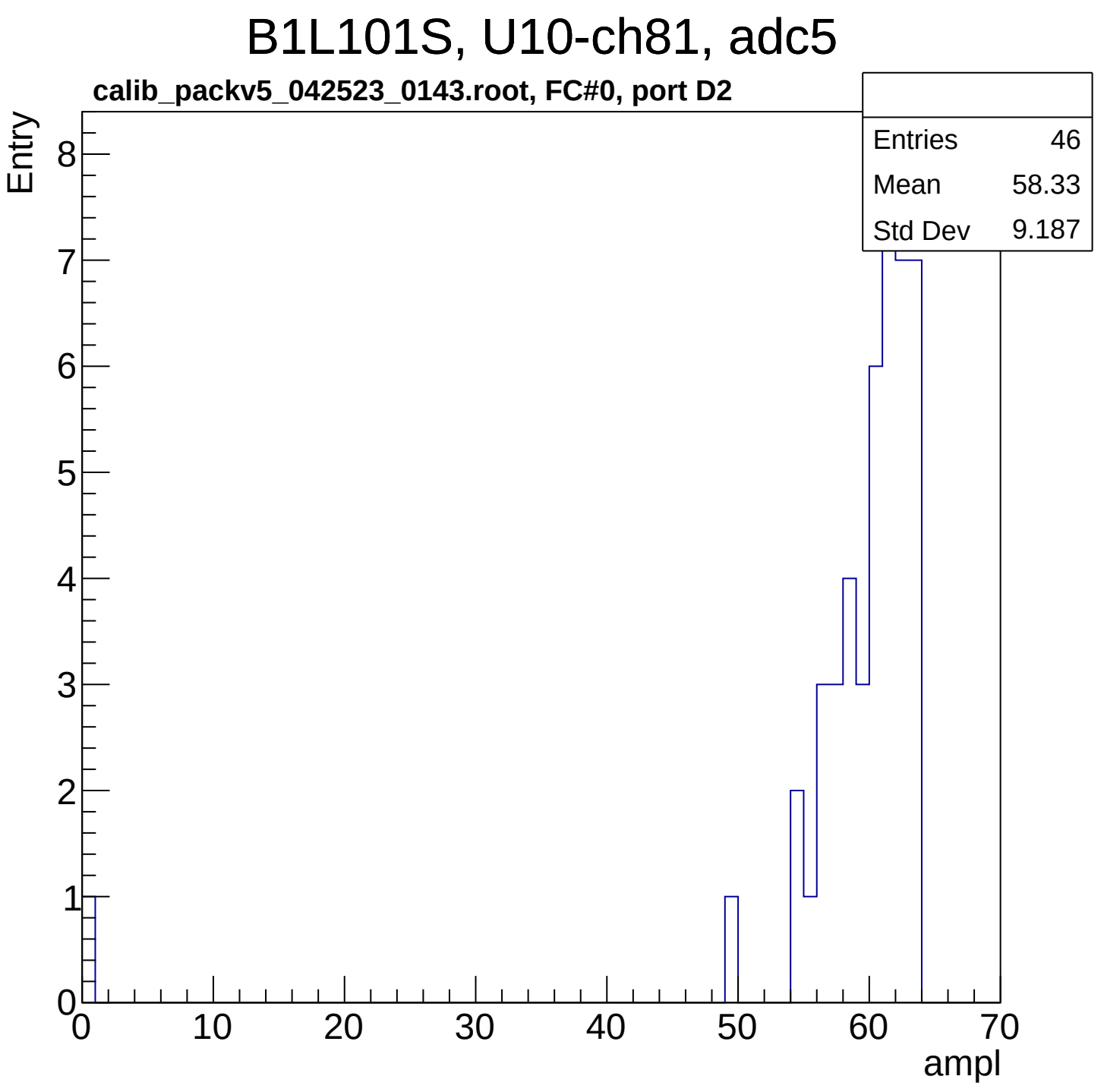
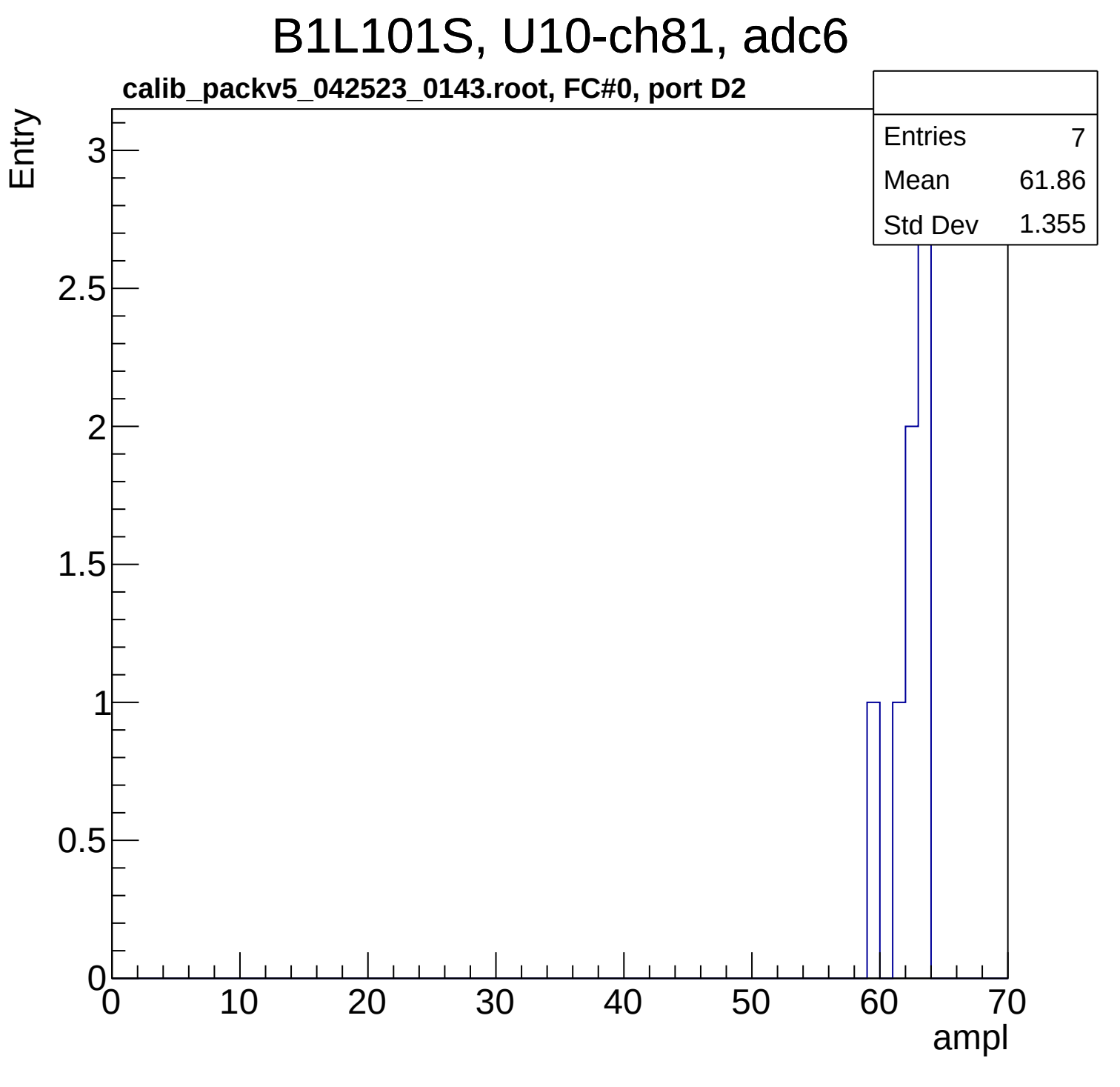

B1L101S, U10-ch81, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 58.33
Std Dev 9.187
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch81, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 61.86
Std Dev 1.355
Entry
ampl
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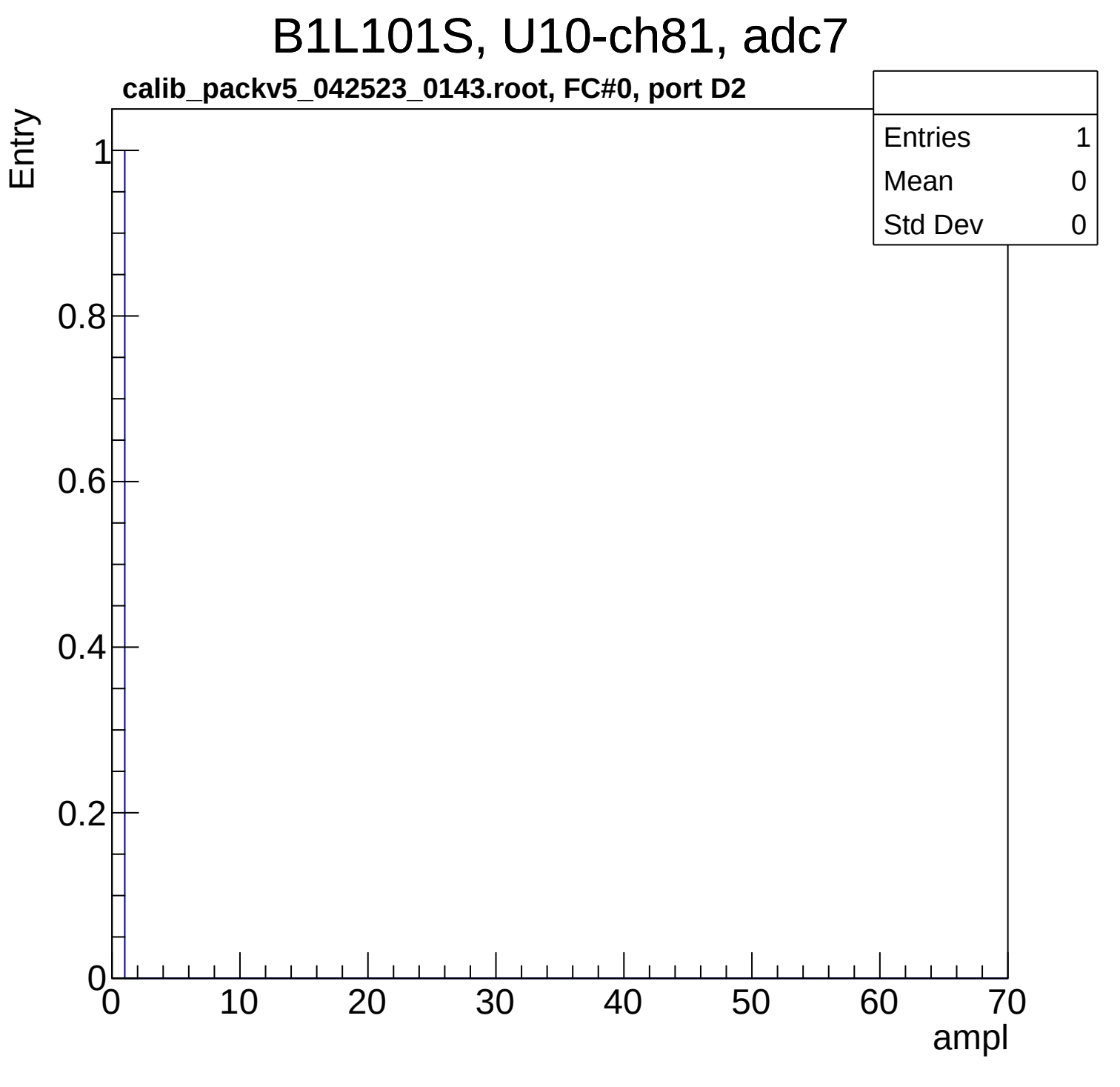
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U10-ch81, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
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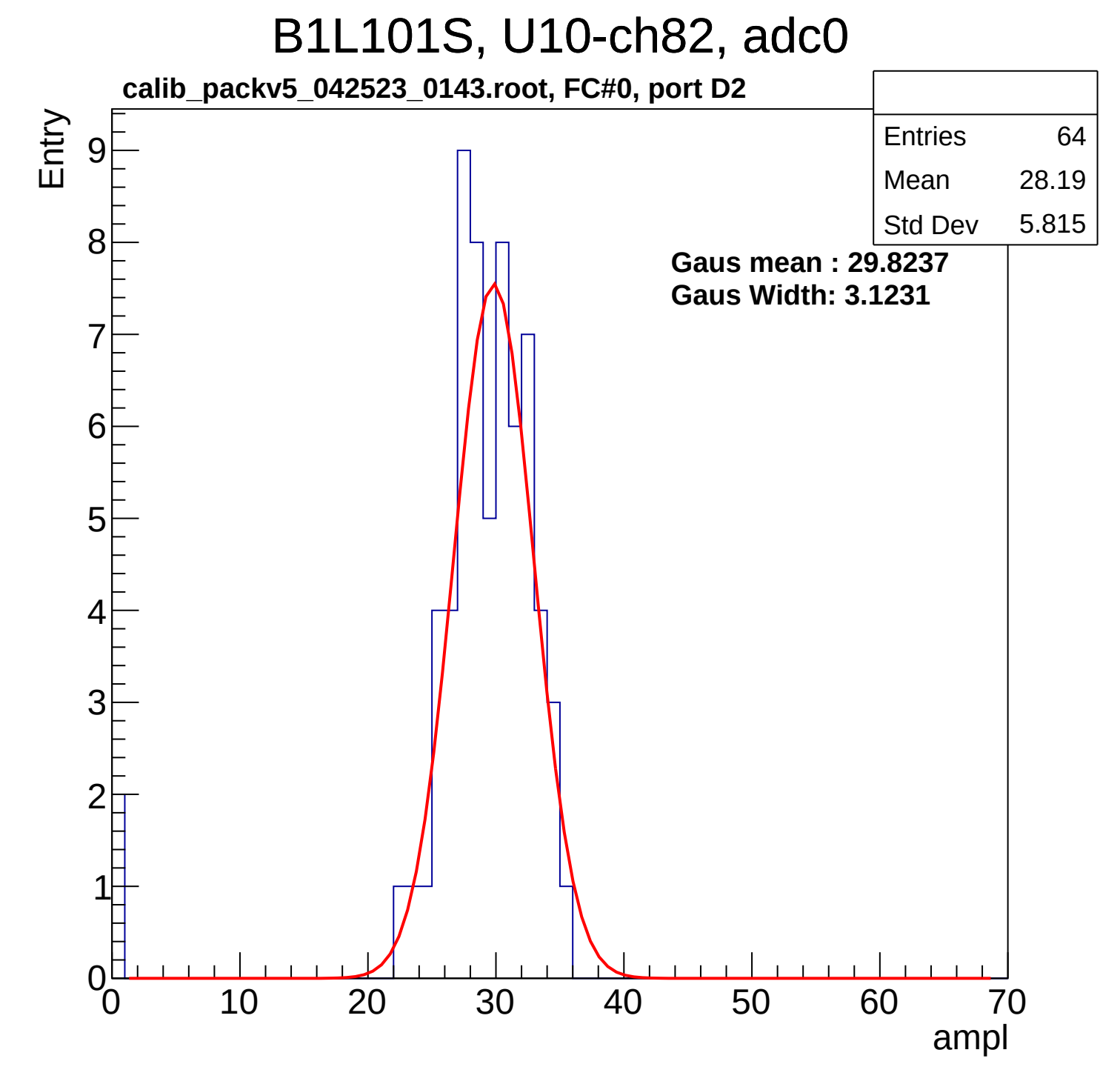
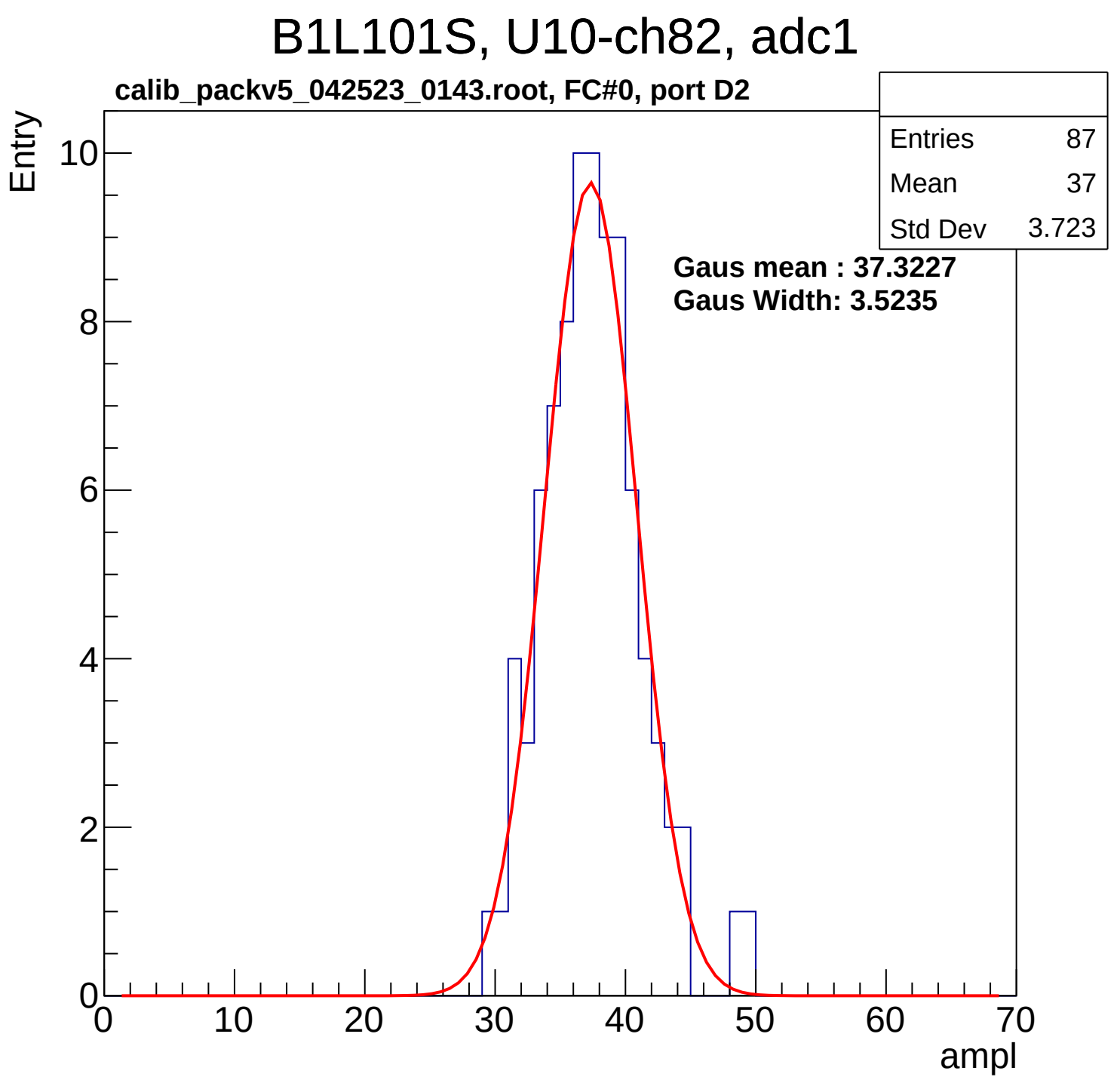
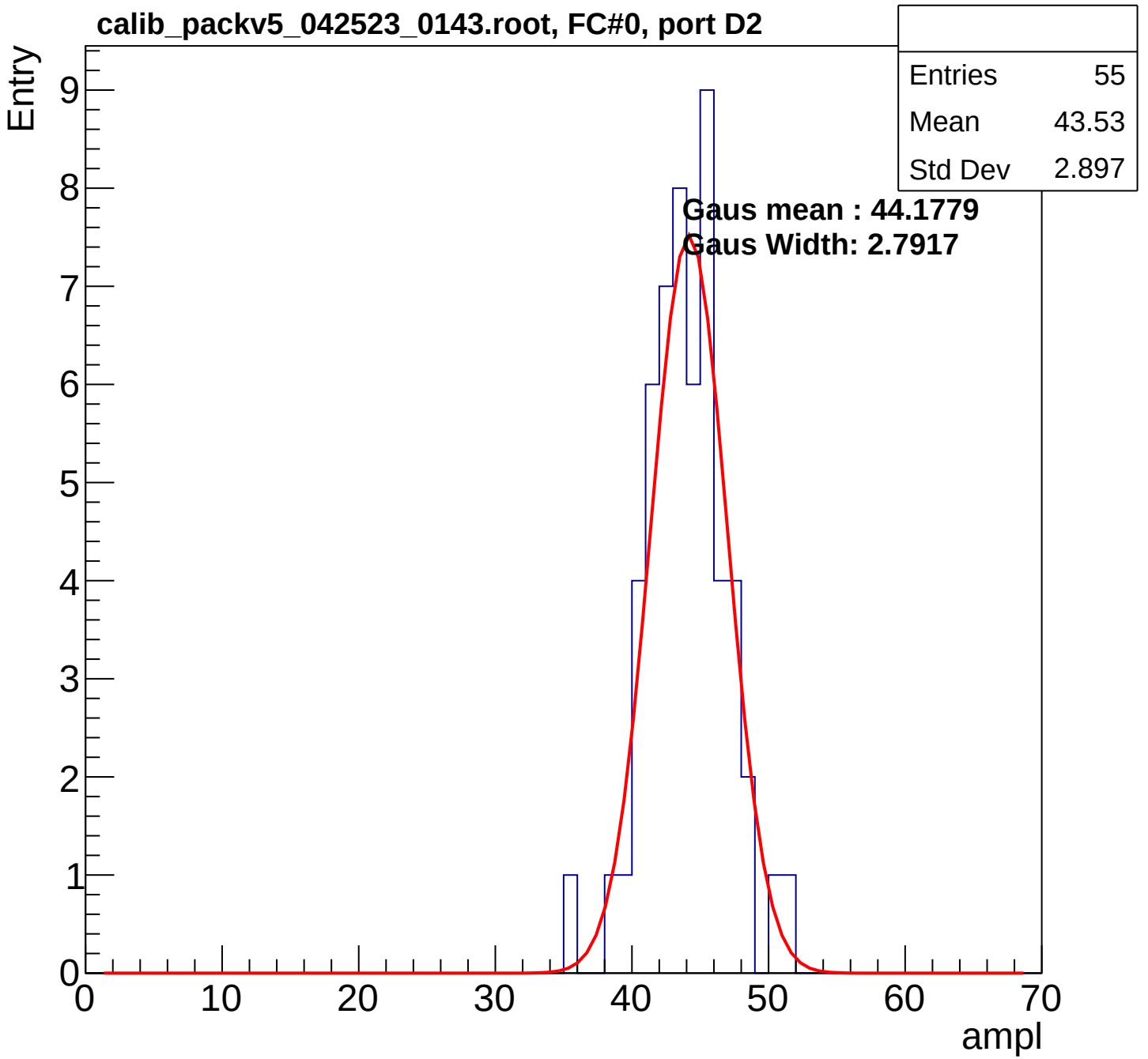
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch82, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 28.19
Std Dev 5.815
Gaus mean : 29.8237
Gaus Width: 3.1231
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch82, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 87
Mean 37
Std Dev 3.723
Gaus mean : 37.3227
Gaus Width: 3.5235
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch82, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 43.53
Std Dev 2.897
Gaus mean : 44.1779
Gaus Width: 2.7917
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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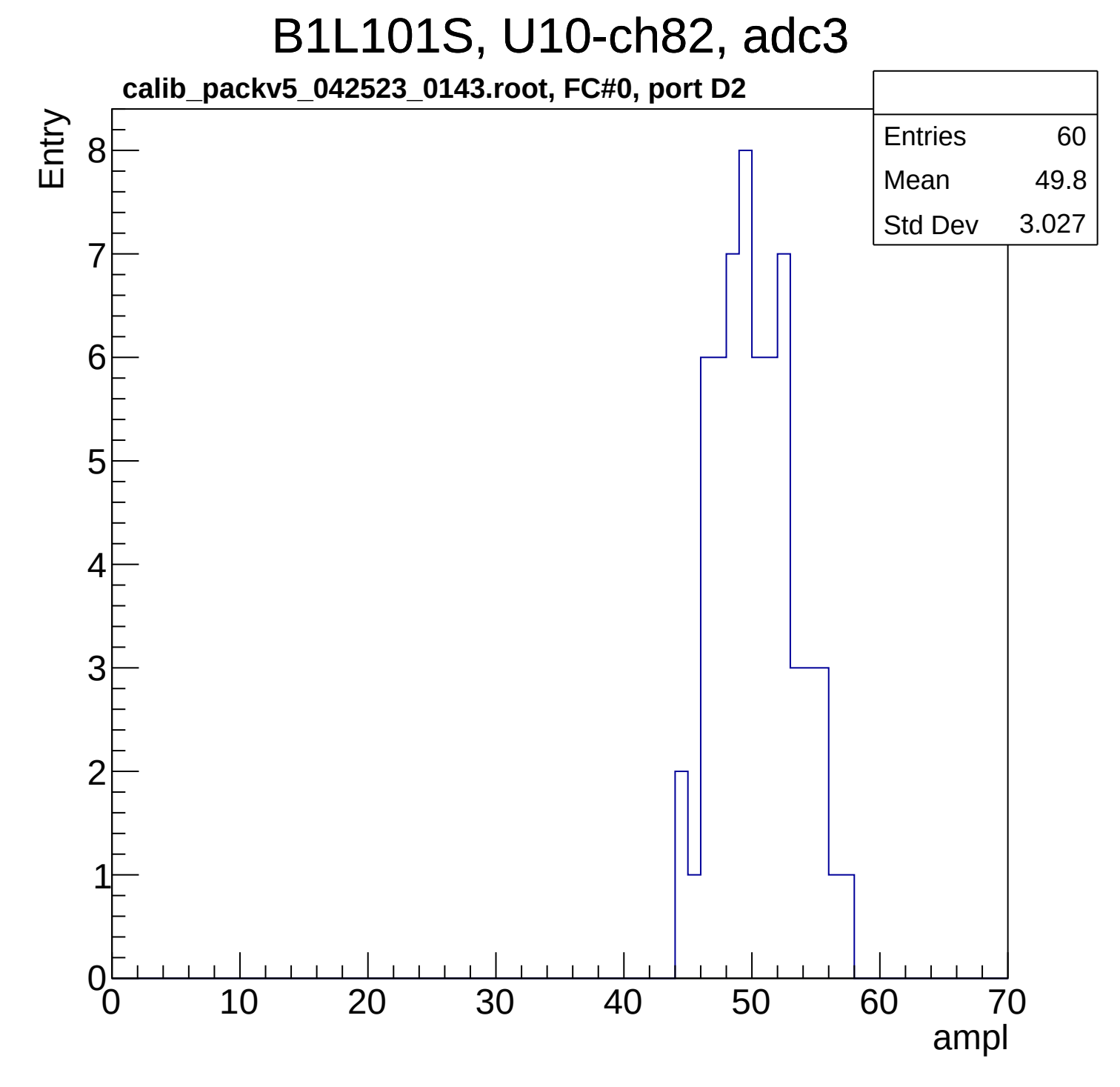
B1L101S, U10-ch82, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 49.8
Std Dev 3.027
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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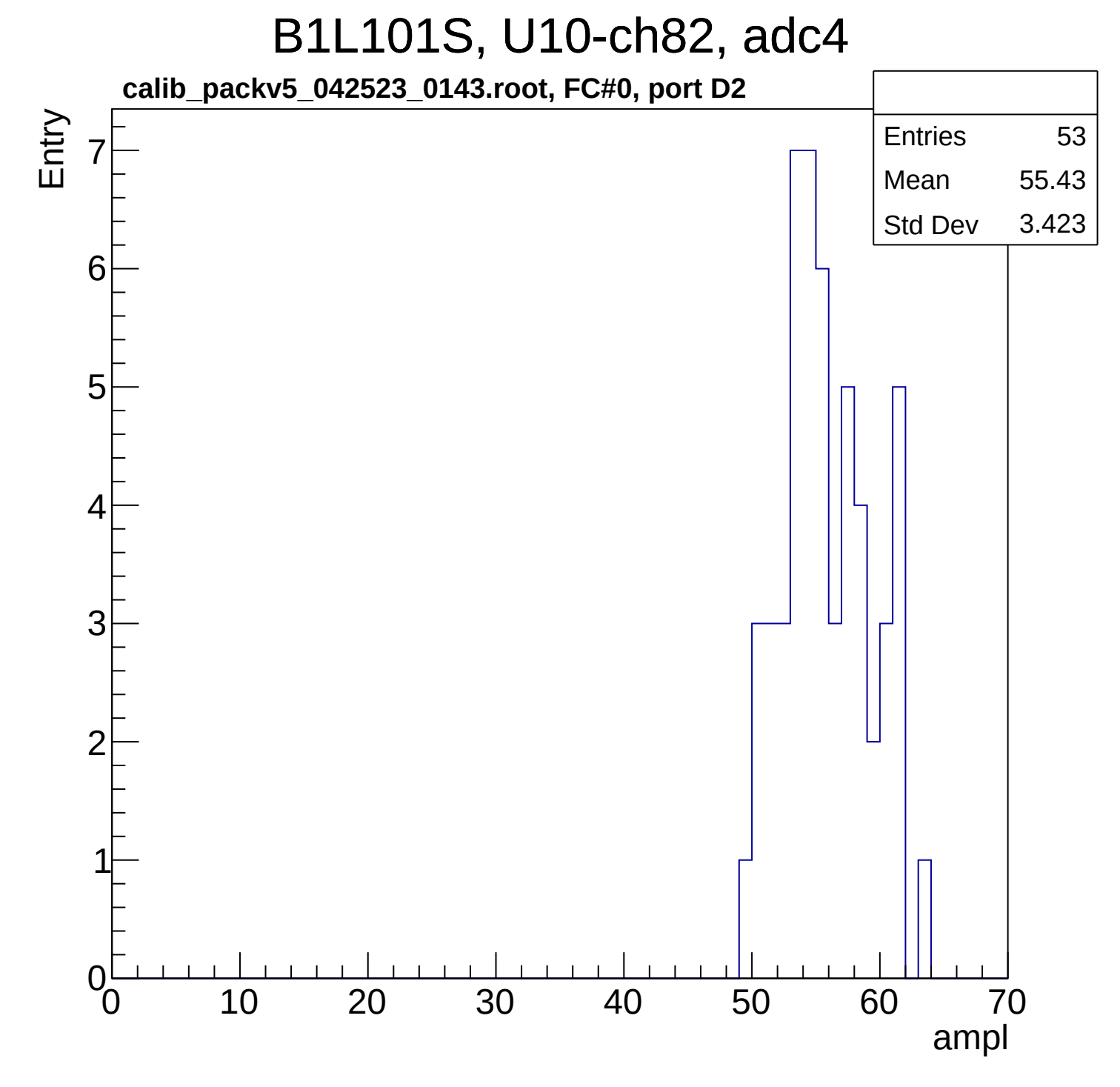
B1L101S, U10-ch82, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 55.43
Std Dev 3.423
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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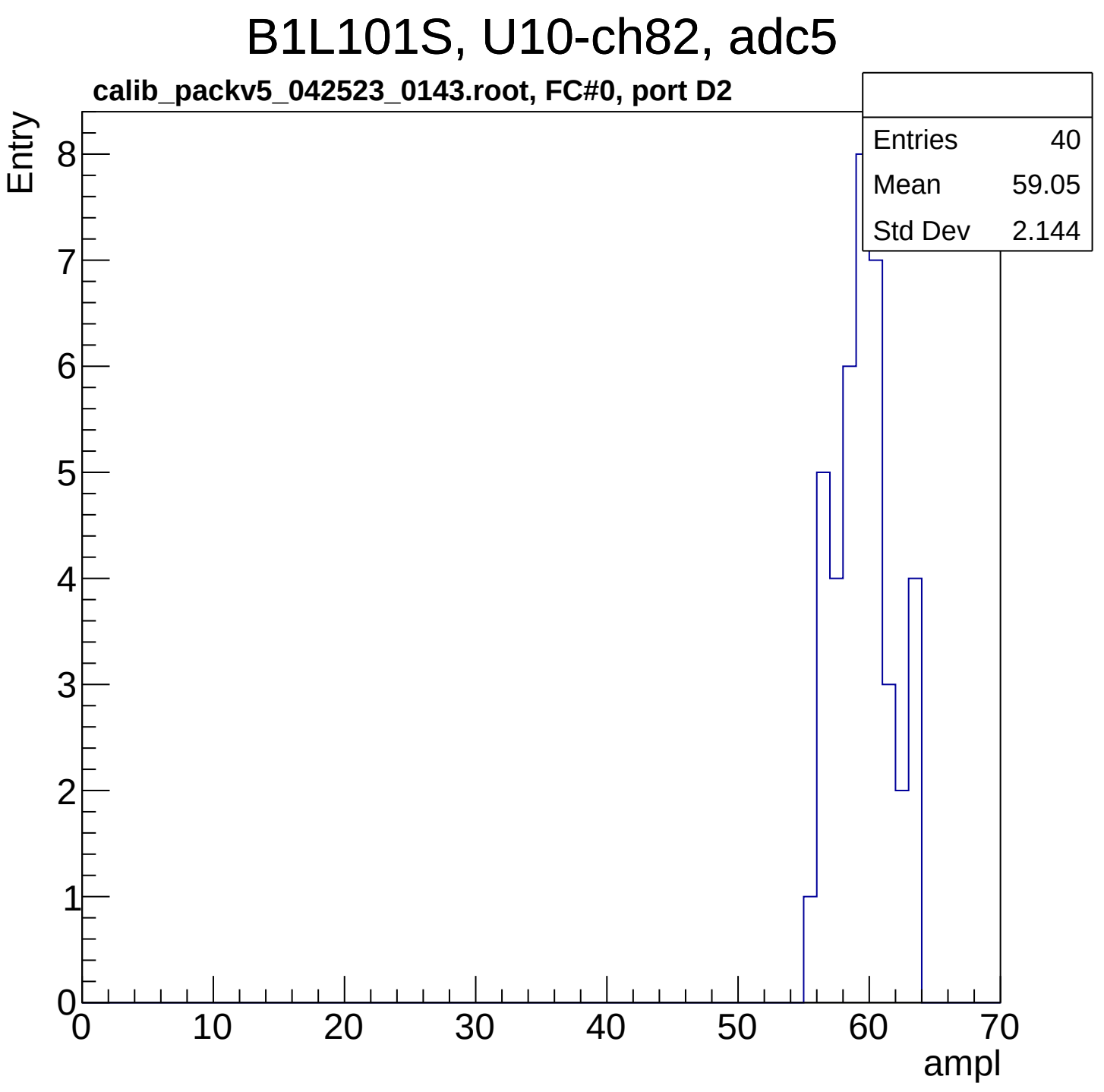
B1L101S, U10-ch82, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 40
Mean 59.05
Std Dev 2.144
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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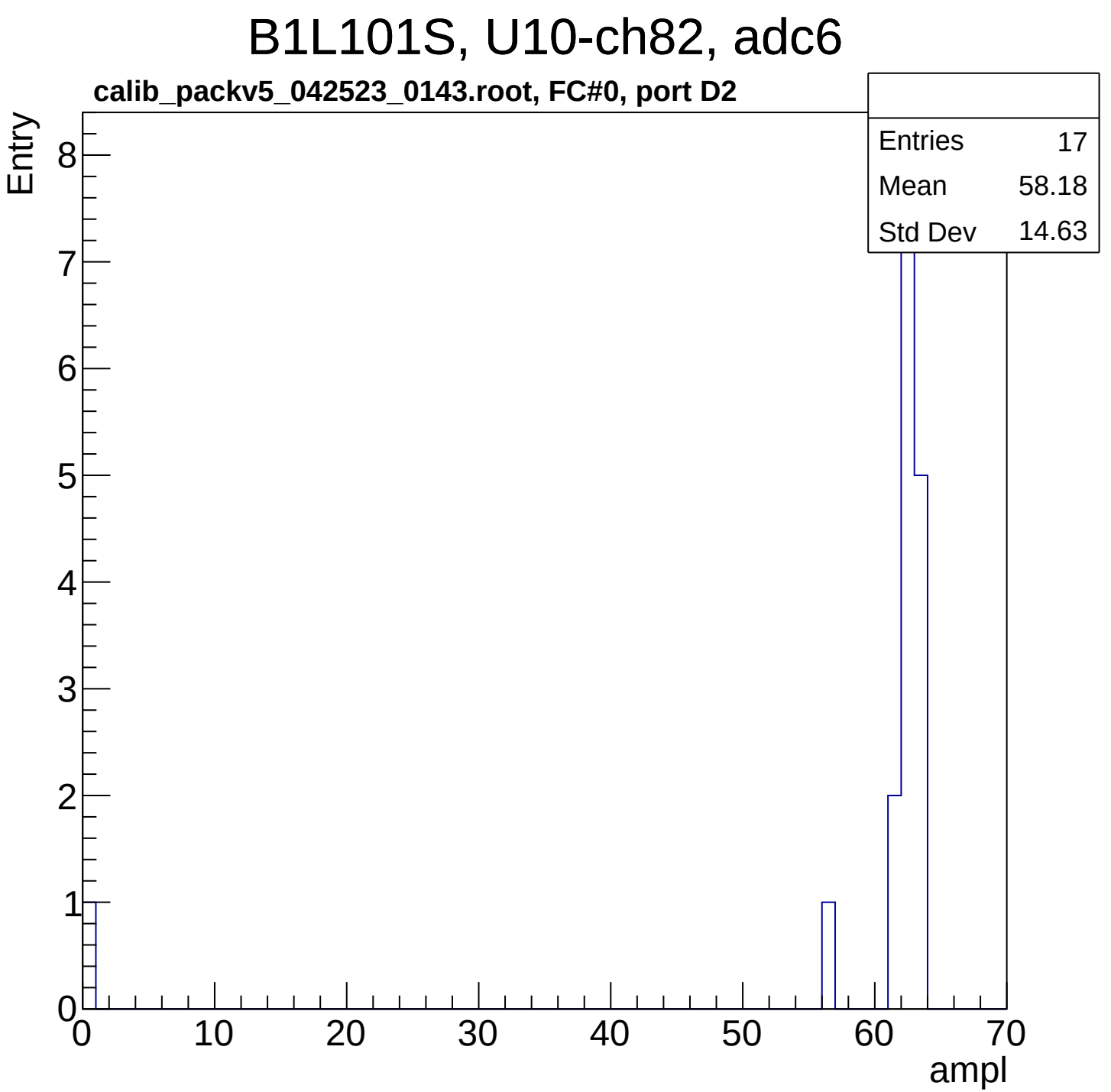
B1L101S, U10-ch82, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 17
Mean 58.18
Std Dev 14.63
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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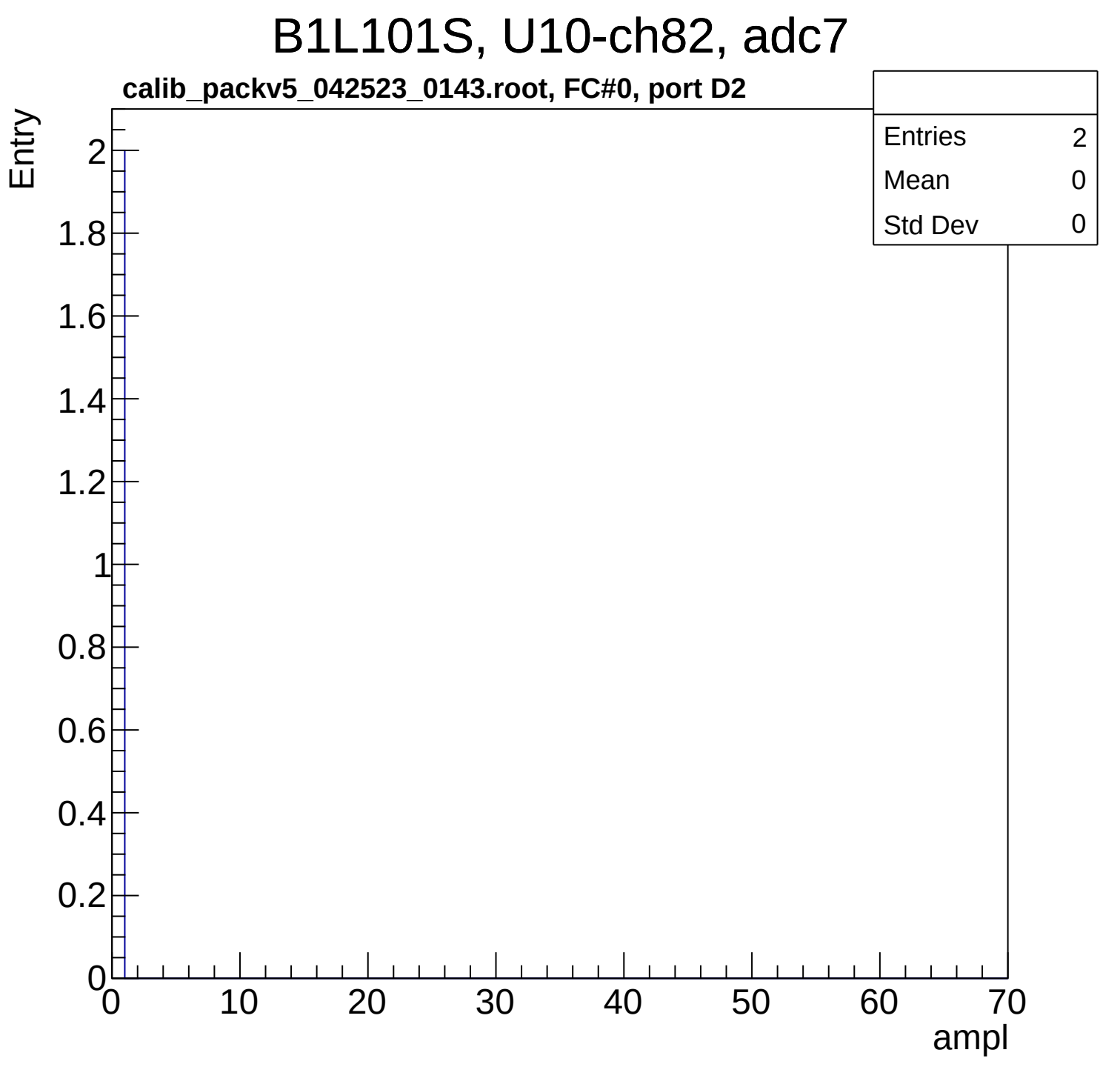
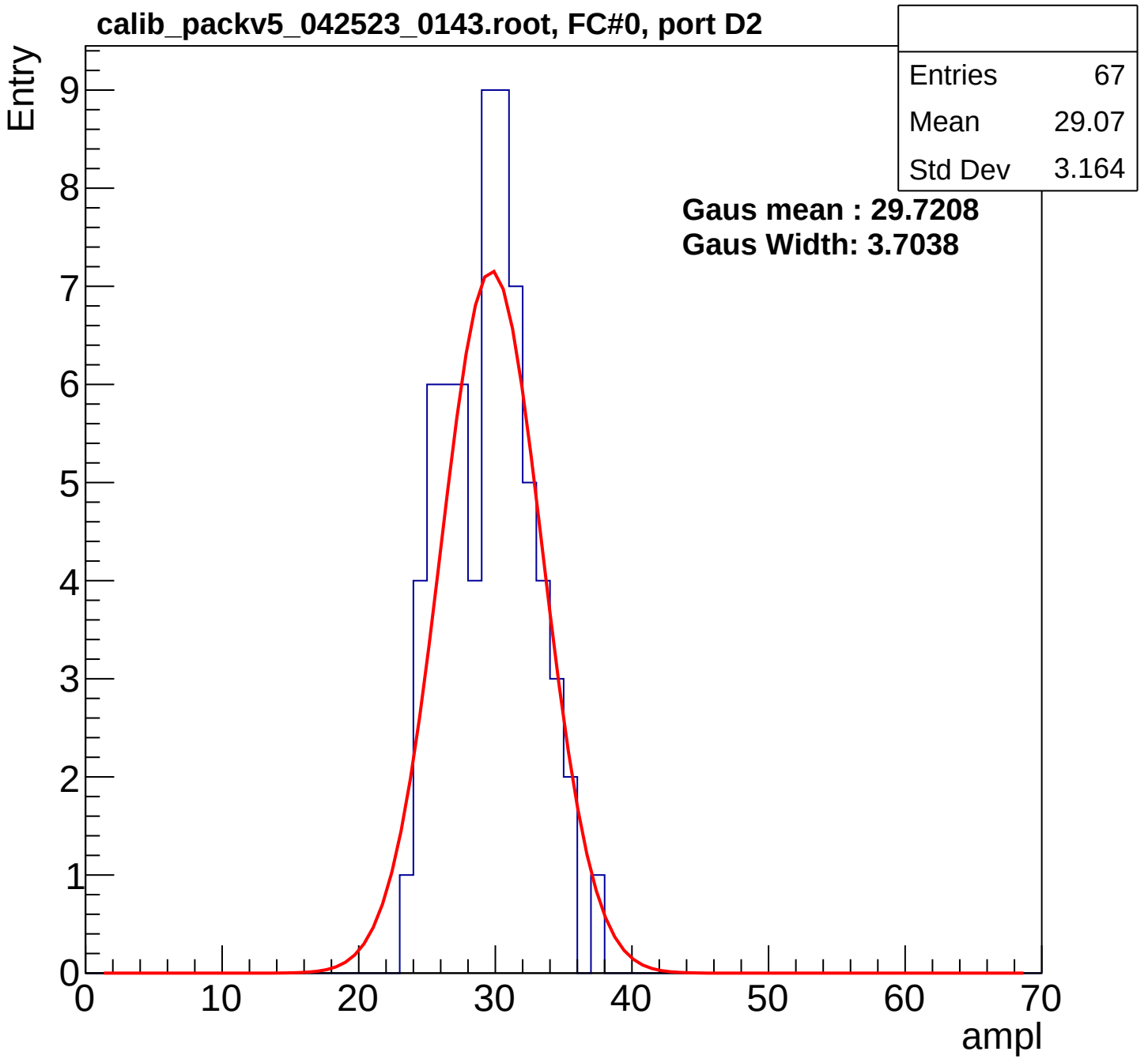

B1L101S, U10-ch82, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U10-ch83, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 29.07
Std Dev 3.164
Gaus mean : 29.7208
Gaus Width: 3.7038
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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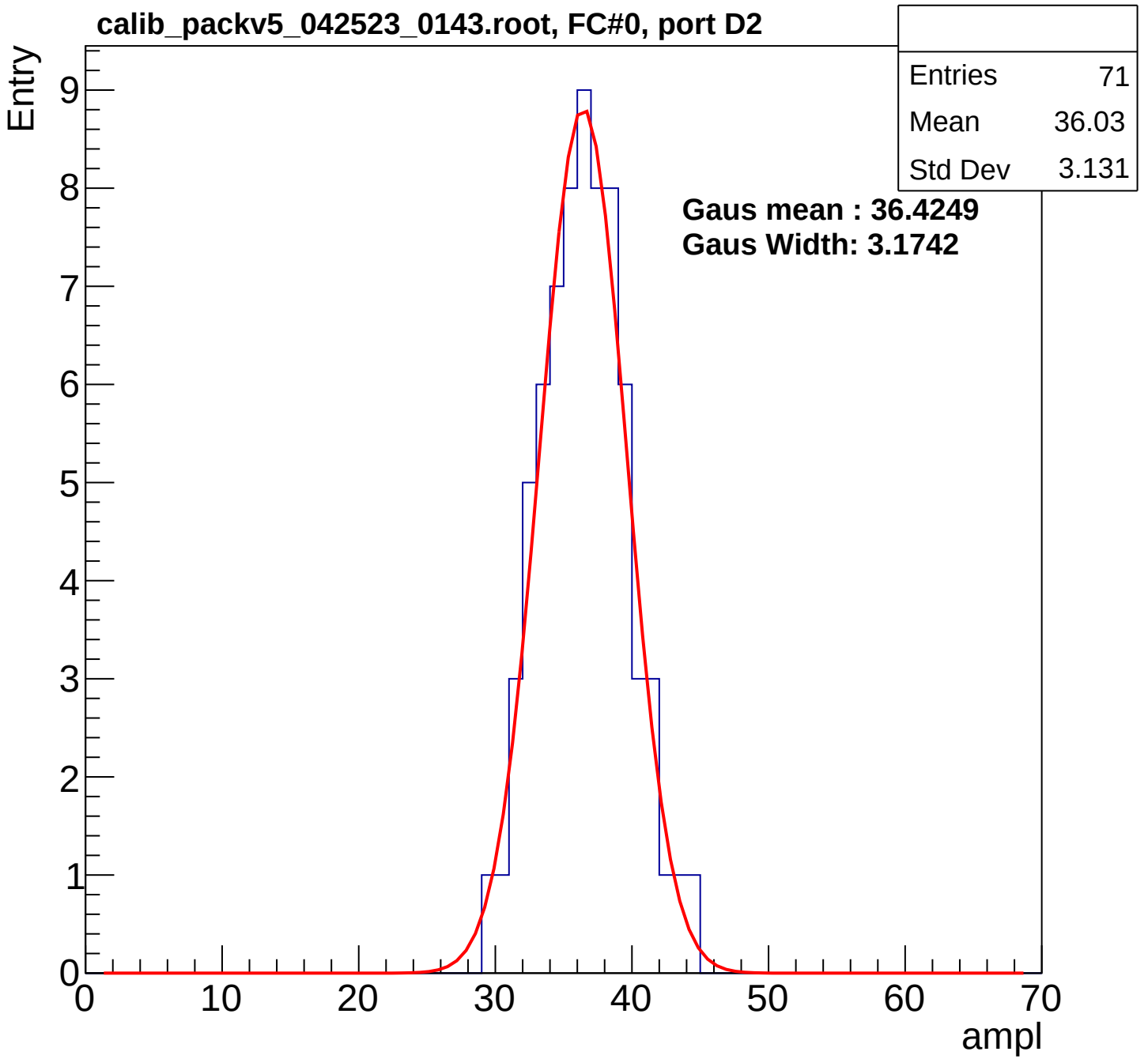
B1L101S, U10-ch83, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 36.03
Std Dev 3.131
Gaus mean : 36.4249
Gaus Width: 3.1742
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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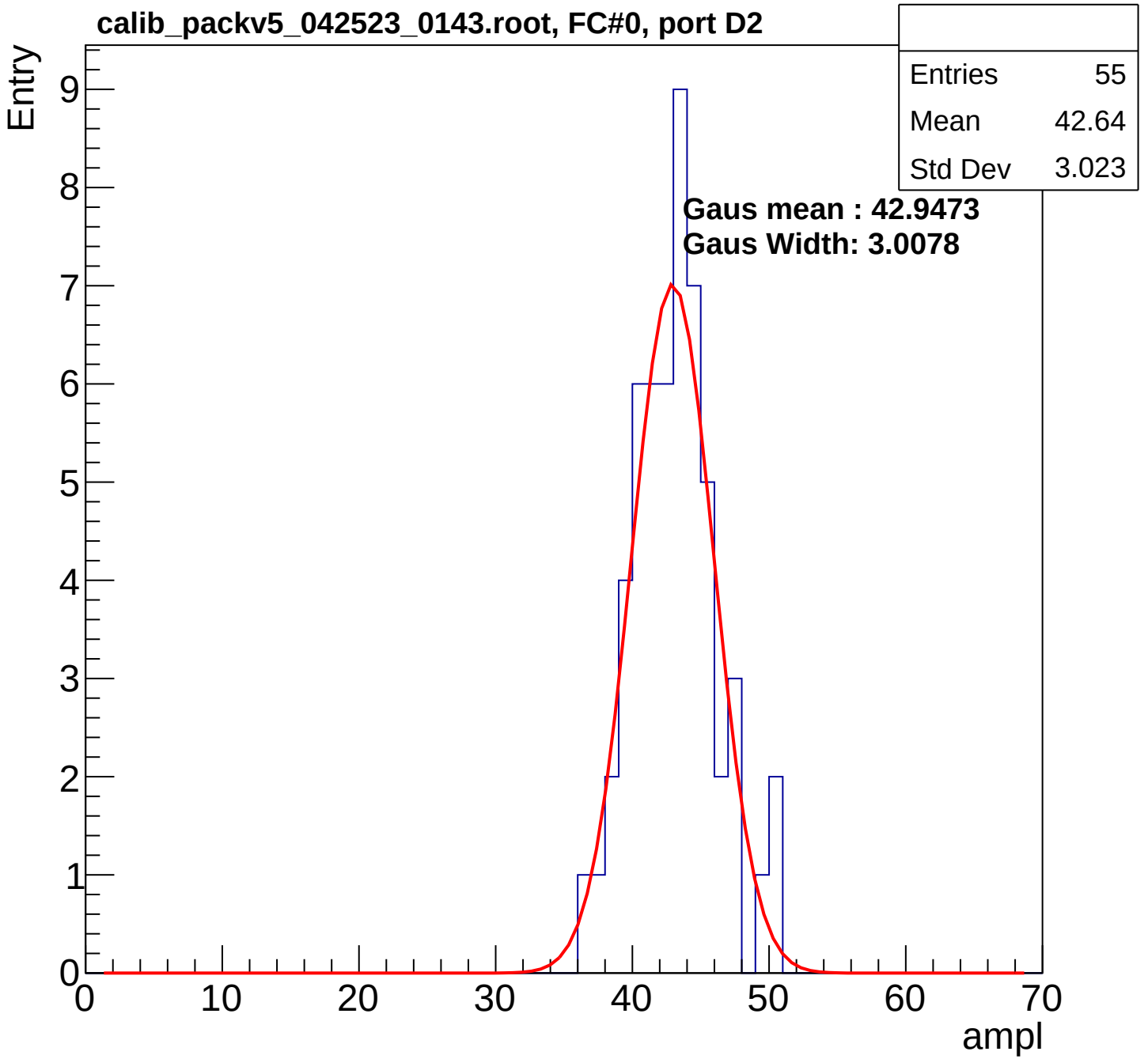
B1L101S, U10-ch83, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 42.64
Std Dev 3.023
Gaus mean : 42.9473
Gaus Width: 3.0078
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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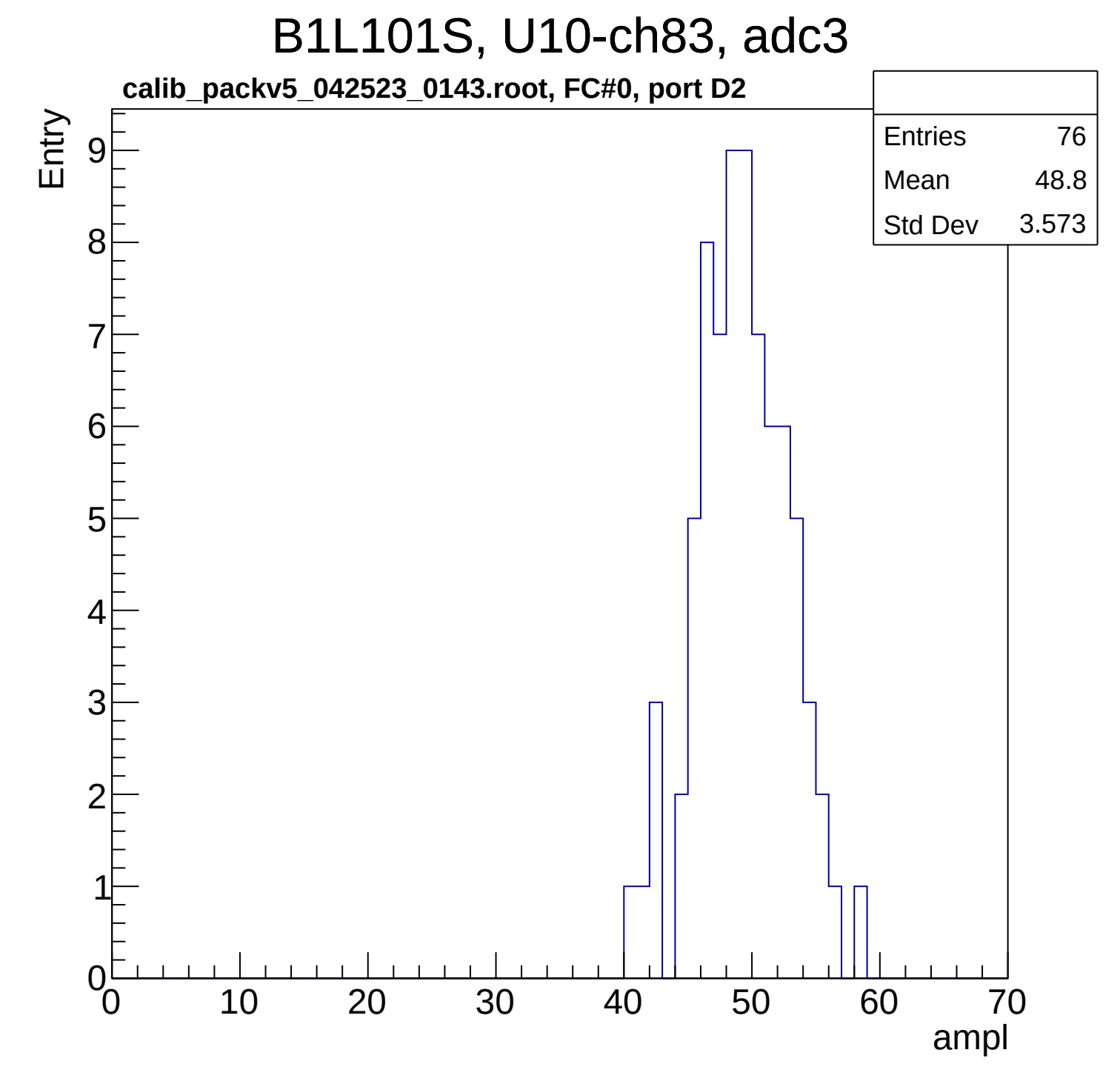
B1L101S, U10-ch83, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 48.8
Std Dev 3.573
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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60
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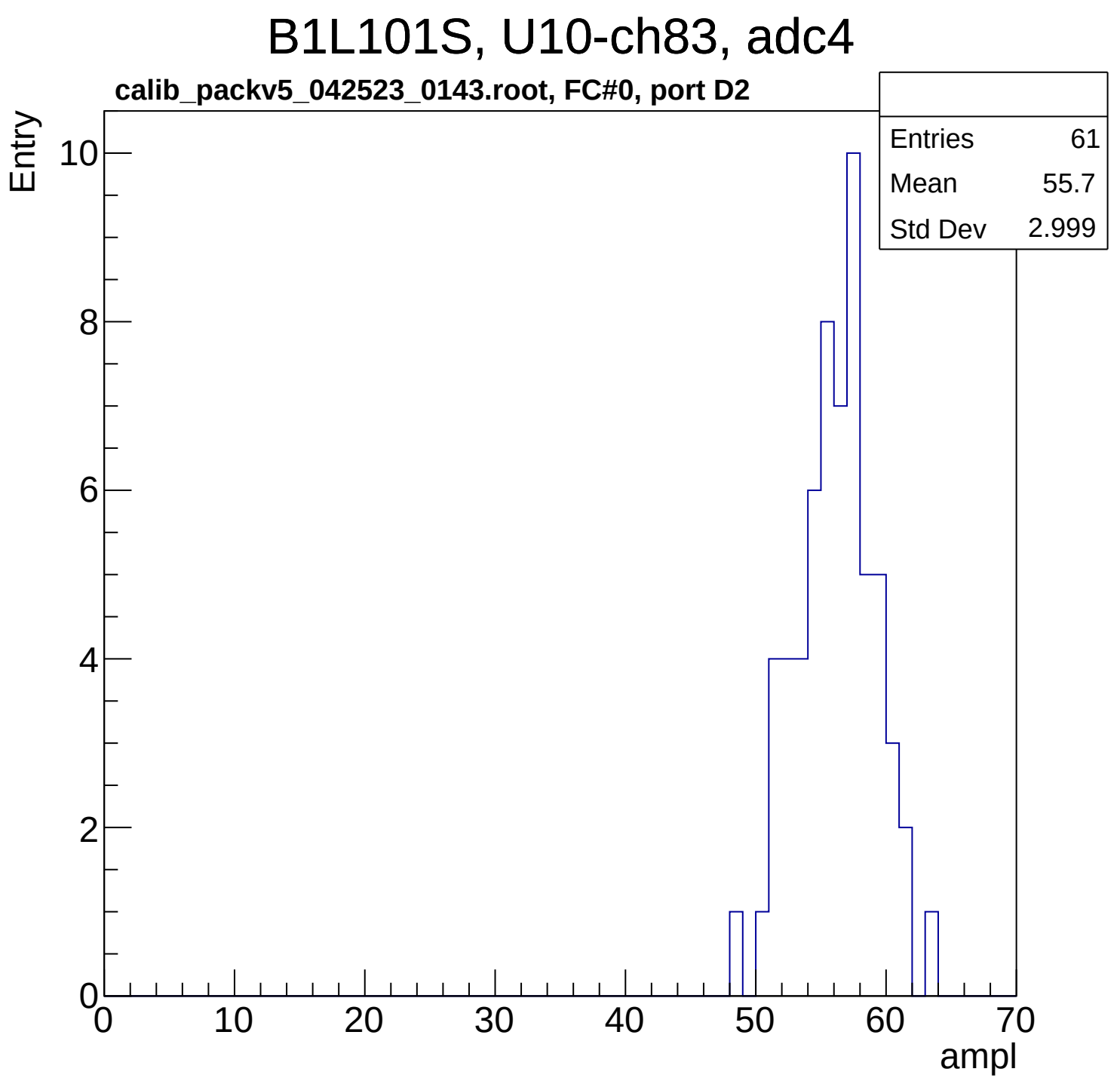
B1L101S, U10-ch83, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 55.7
Std Dev 2.999
Entry
ampl
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2
4
6
8
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0
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20
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40
50
60
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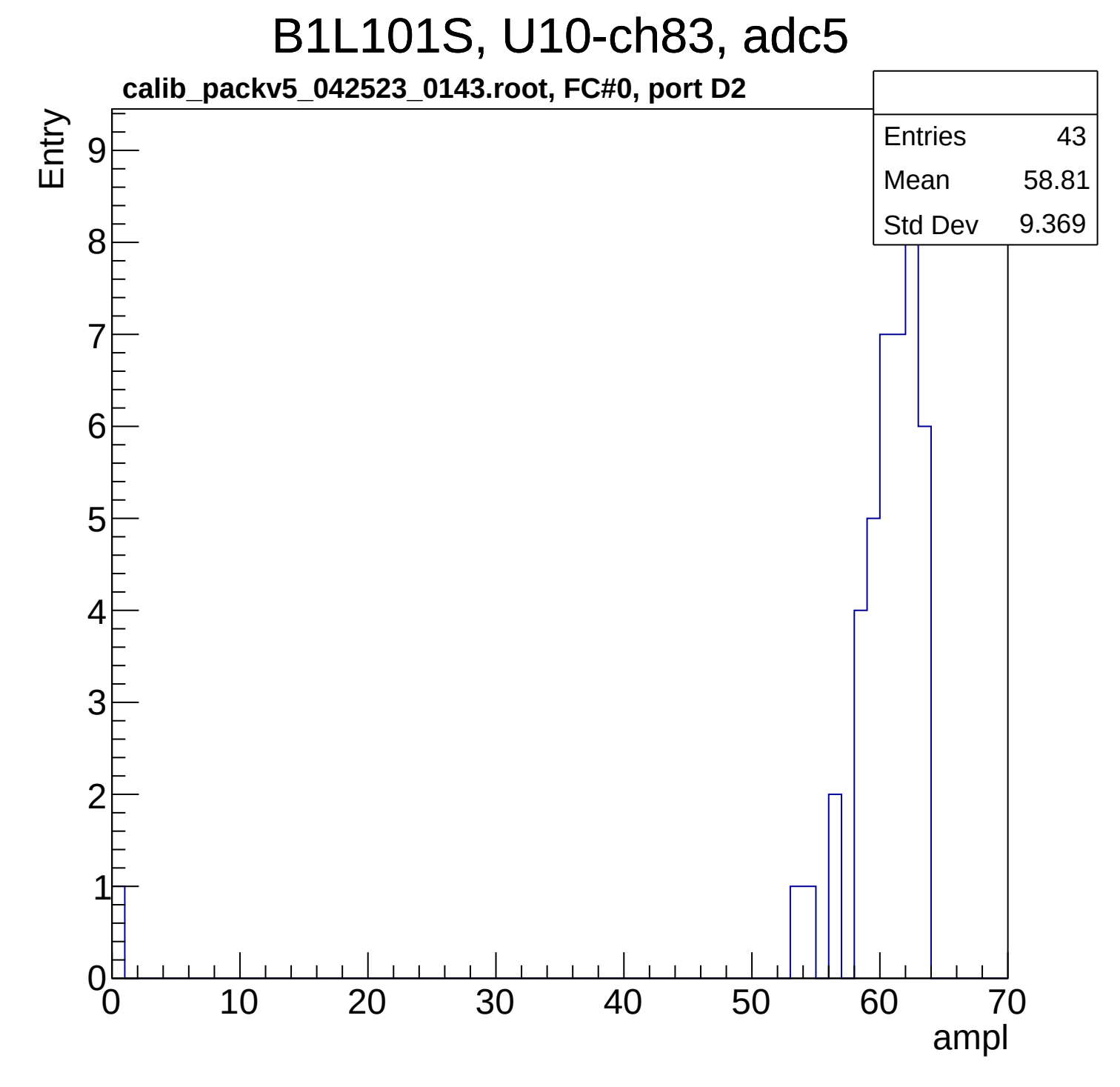
B1L101S, U10-ch83, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 43
Mean 58.81
Std Dev 9.369
Entry
ampl
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3
4
5
6
7
8
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0
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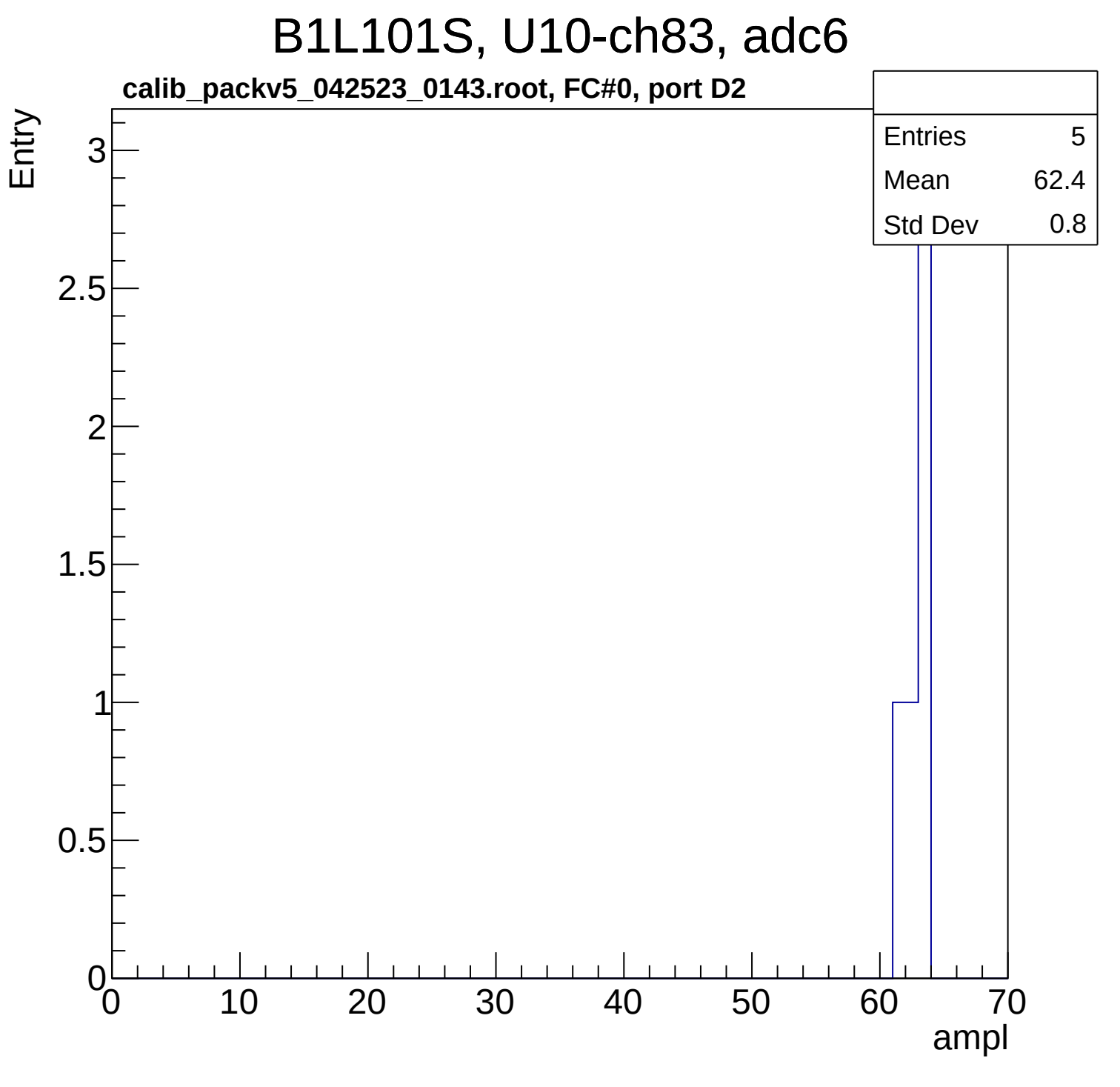
B1L101S, U10-ch83, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 62.4
Std Dev 0.8
Entry
ampl
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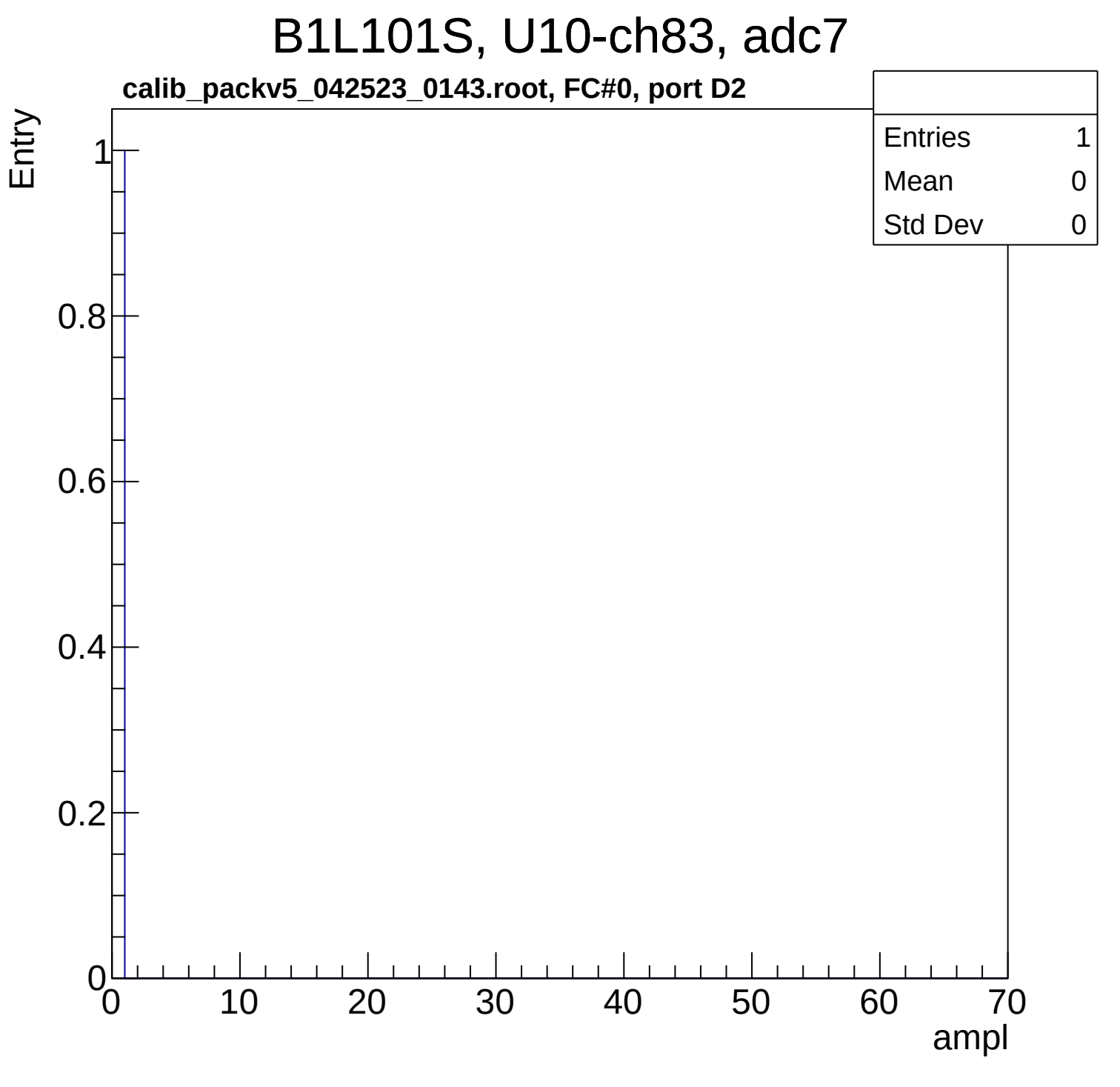
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U10-ch83, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
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0.6
0.4
0.2
0
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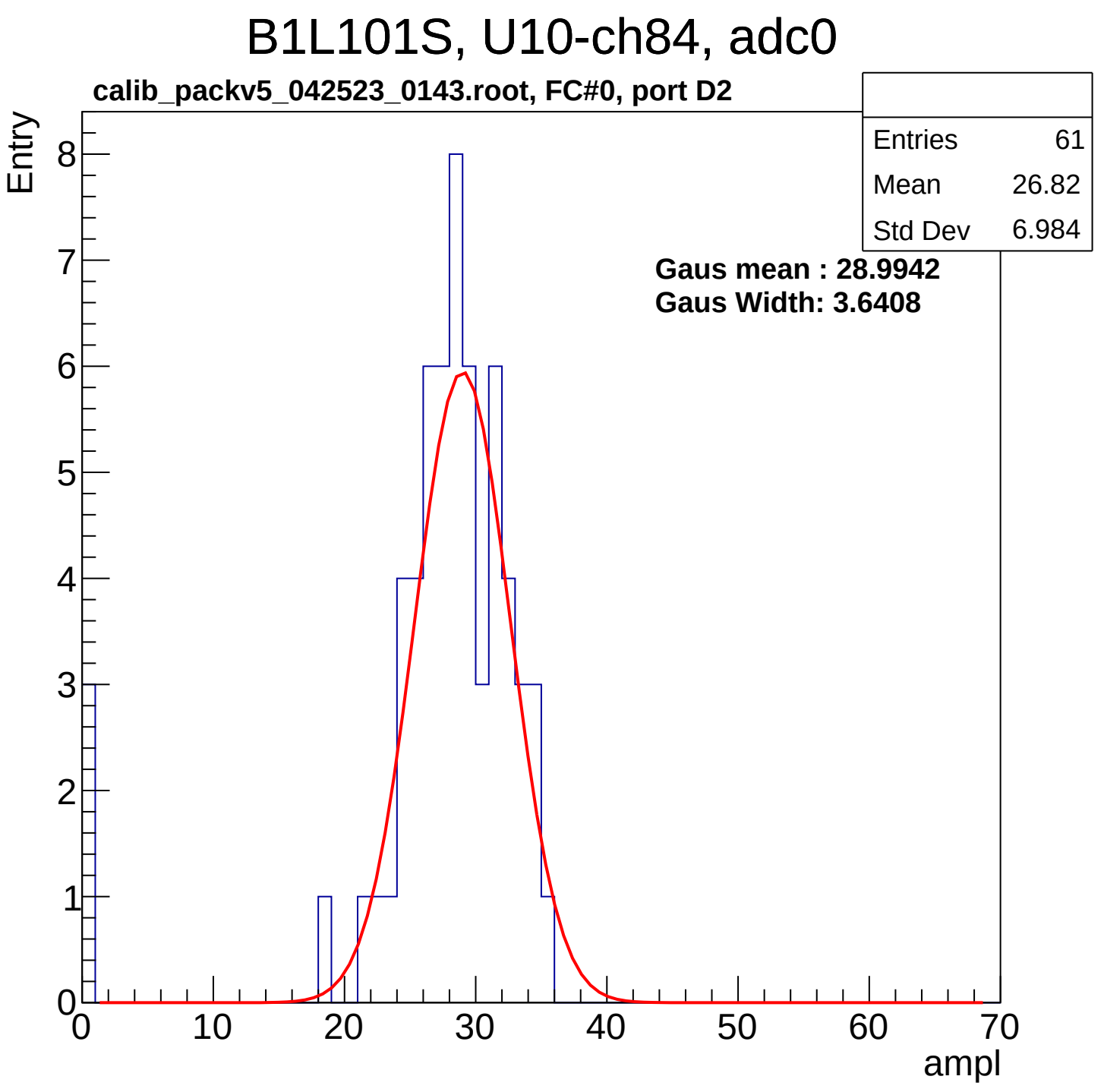
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch84, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 26.82
Std Dev 6.984
Gaus mean : 28.9942
Gaus Width: 3.6408
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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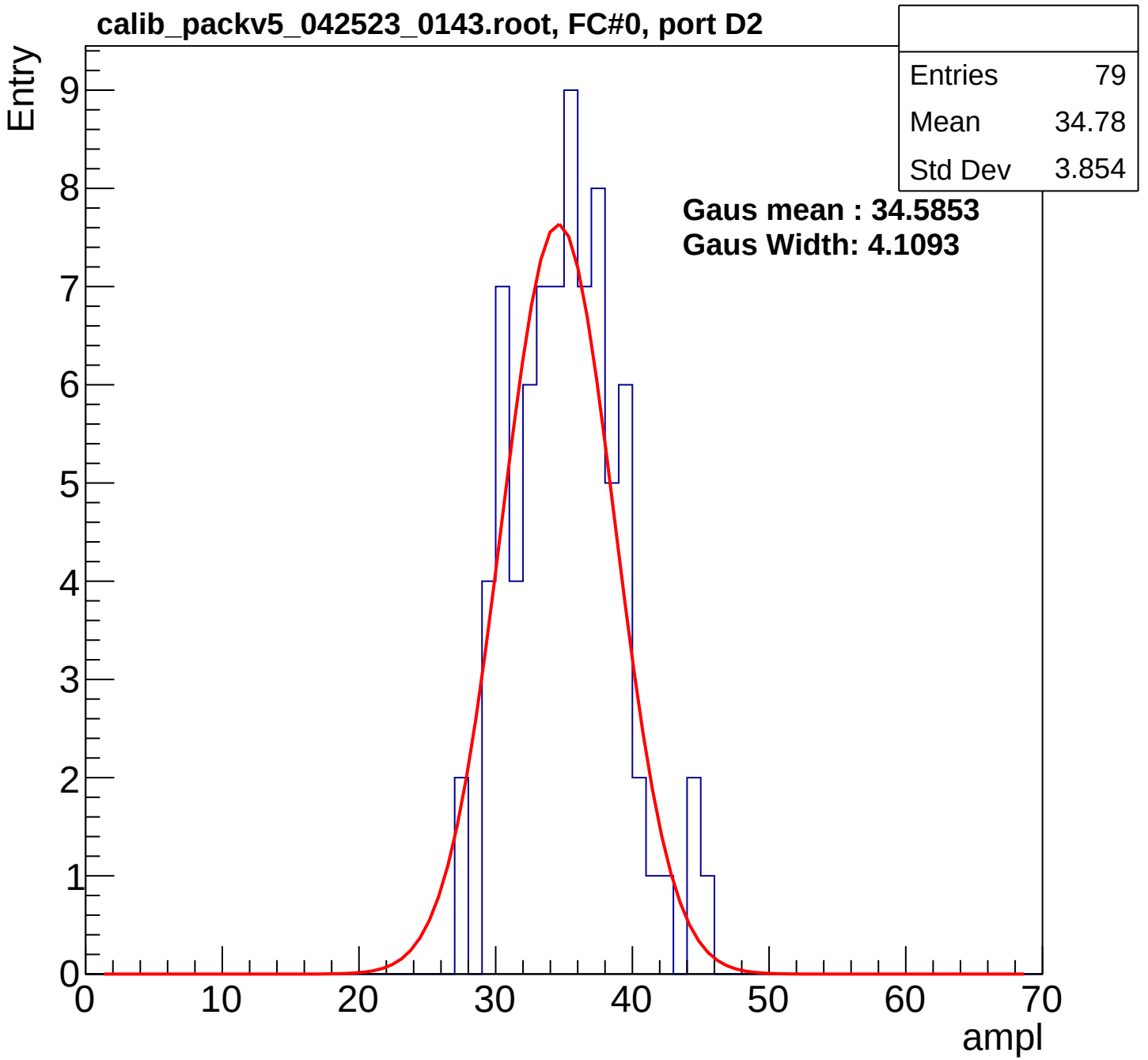
B1L101S, U10-ch84, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 34.78
Std Dev 3.854
Gaus mean : 34.5853
Gaus Width: 4.1093
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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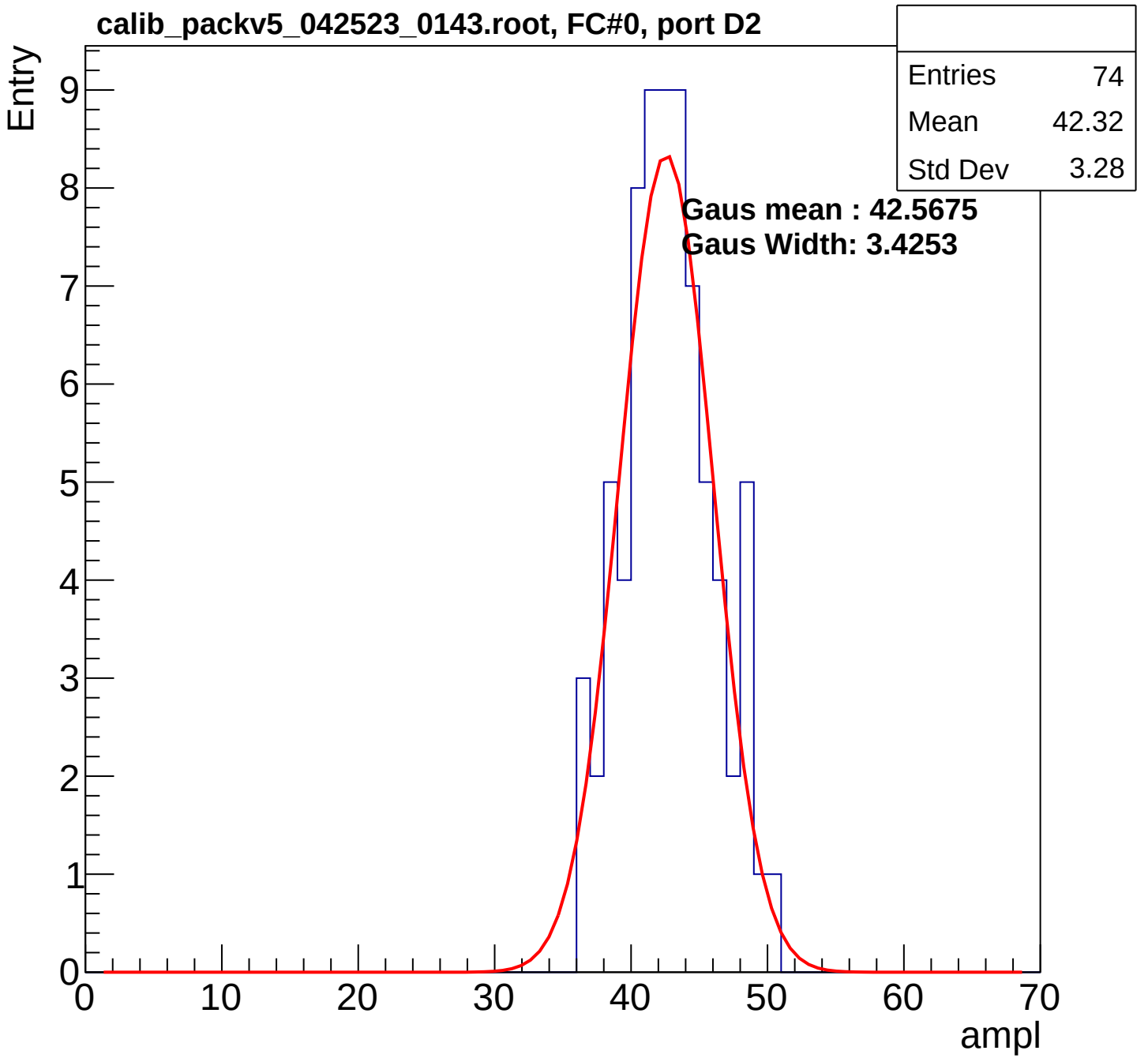
B1L101S, U10-ch84, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 42.32
Std Dev 3.28
Gaus mean : 42.5675
Gaus Width: 3.4253
Entry
ampl
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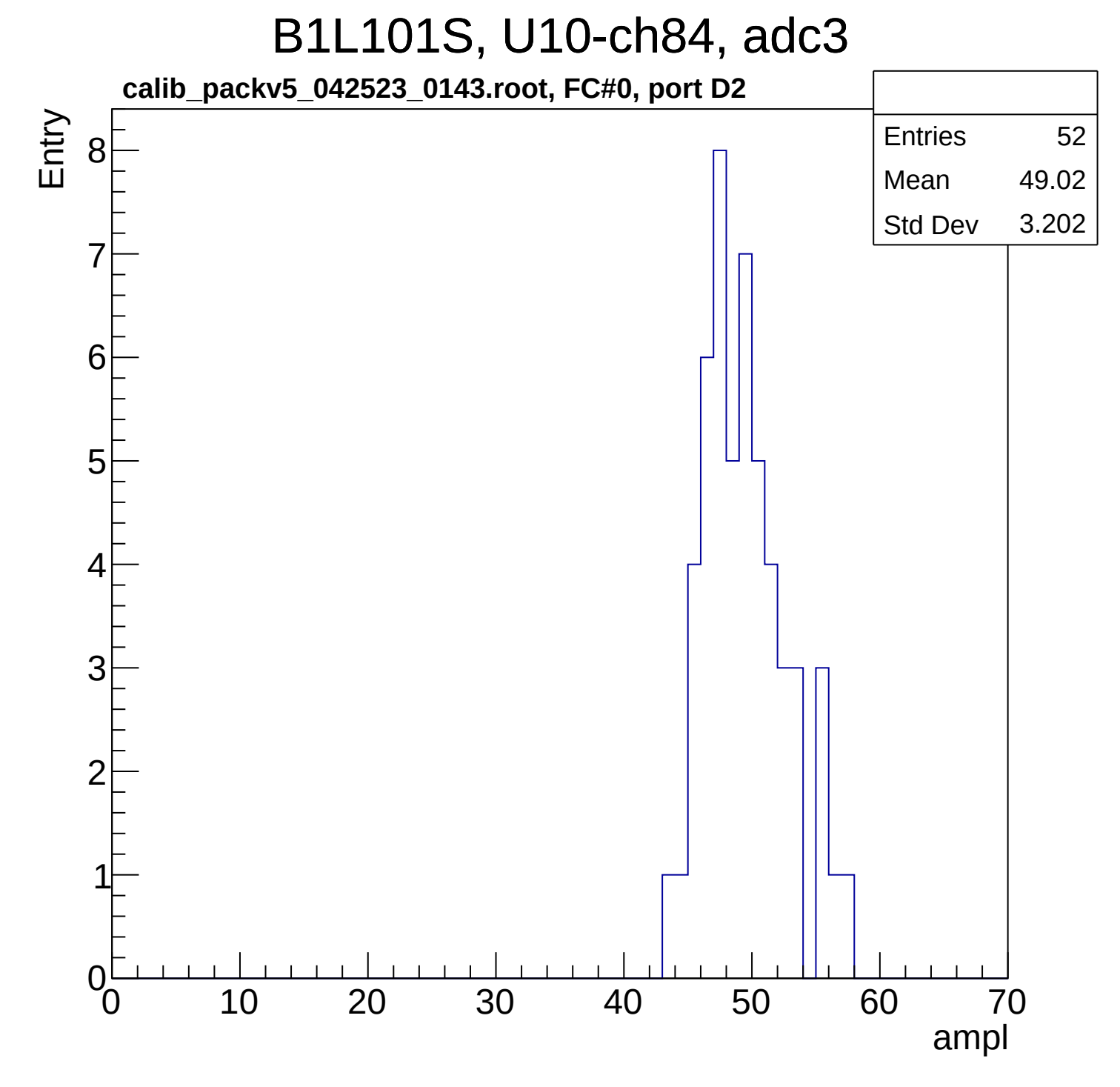
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L101S, U10-ch84, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 49.02
Std Dev 3.202
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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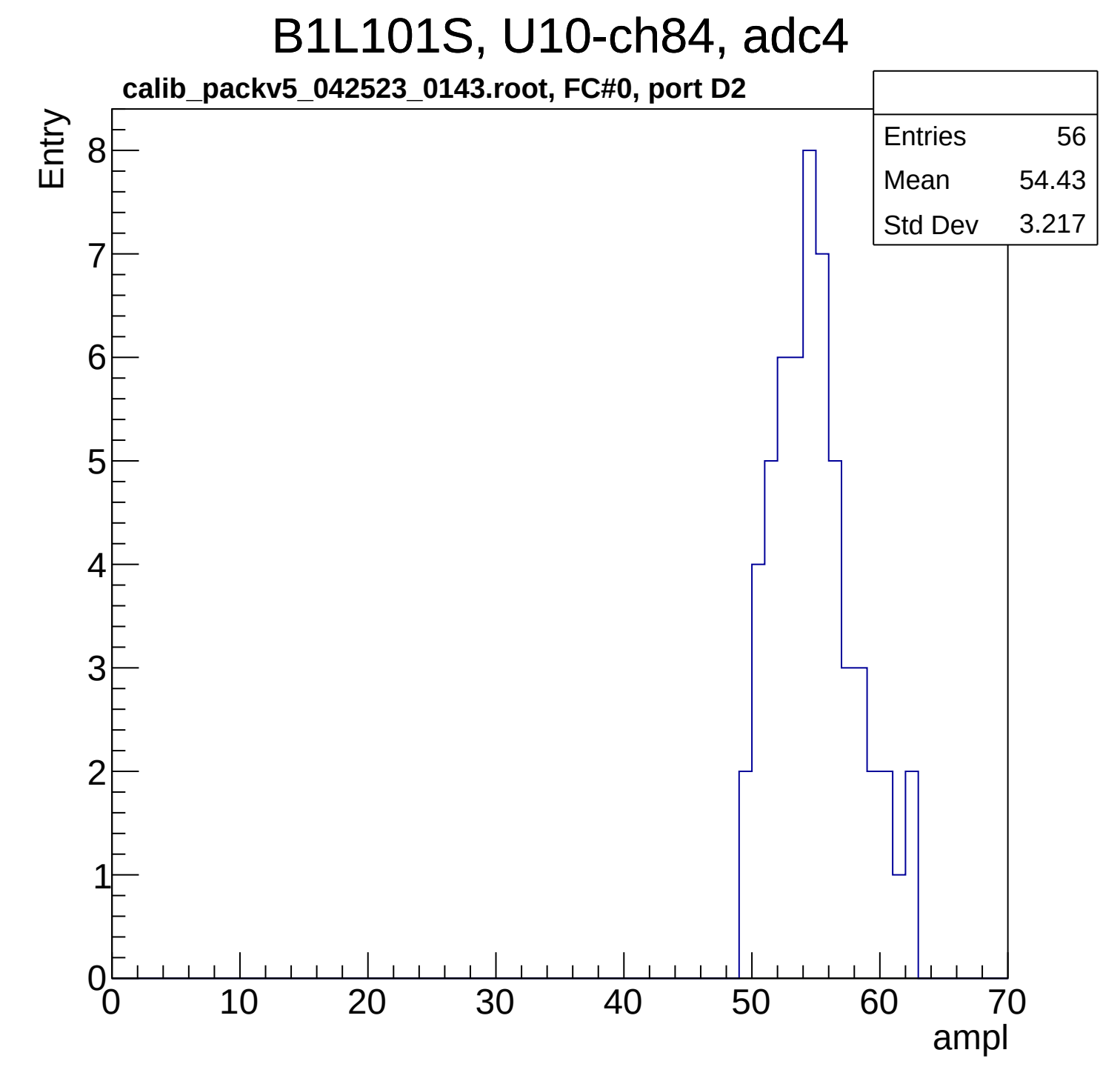
B1L101S, U10-ch84, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 54.43
Std Dev 3.217
Entry
ampl
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3
4
5
6
7
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60
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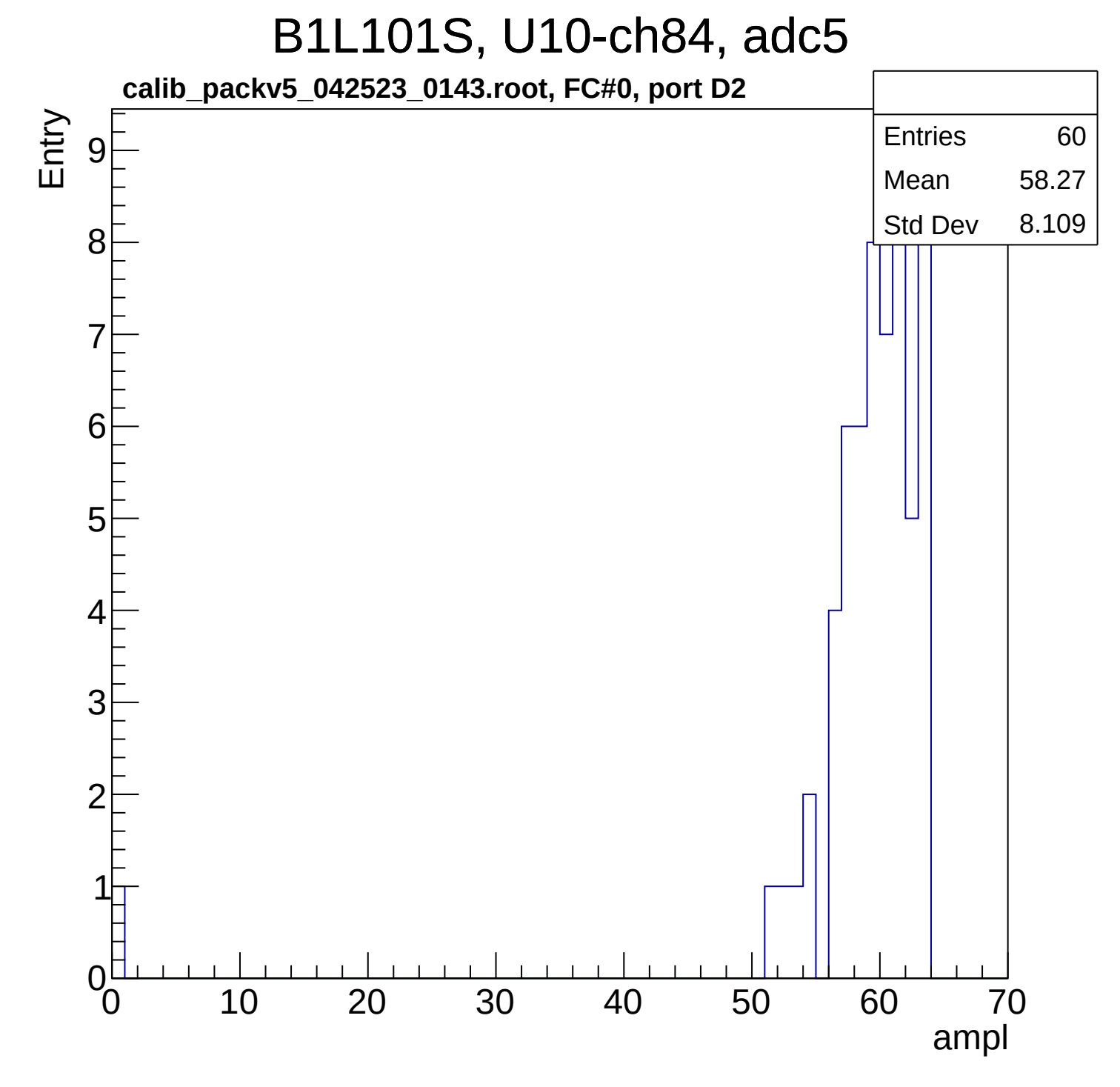
B1L101S, U10-ch84, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 58.27
Std Dev 8.109
Entry
ampl
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3
4
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6
7
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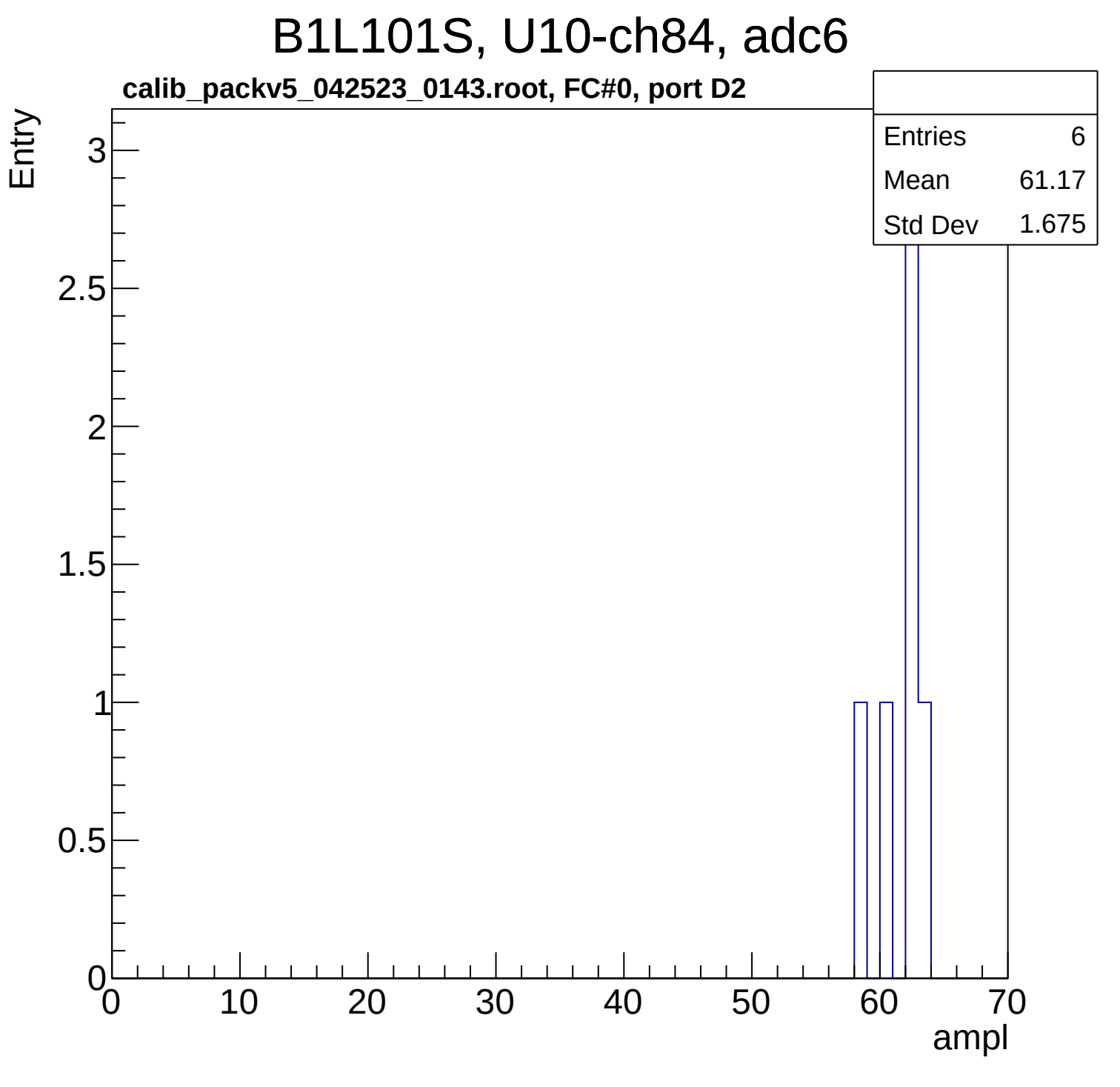
B1L101S, U10-ch84, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 61.17
Std Dev 1.675
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
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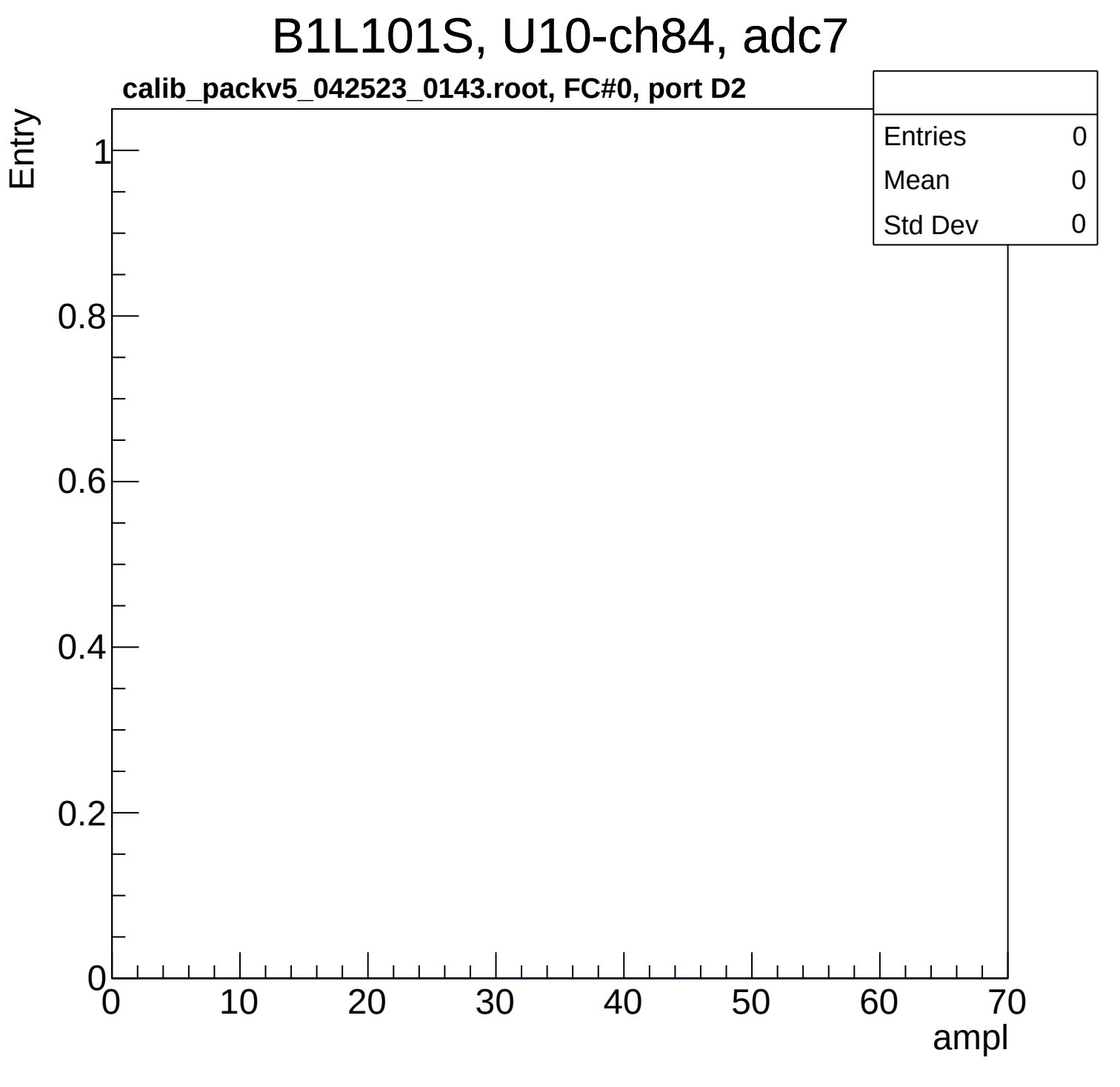
B1L101S, U10-ch84, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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0.8
0.6
0.4
0.2
0
0
10
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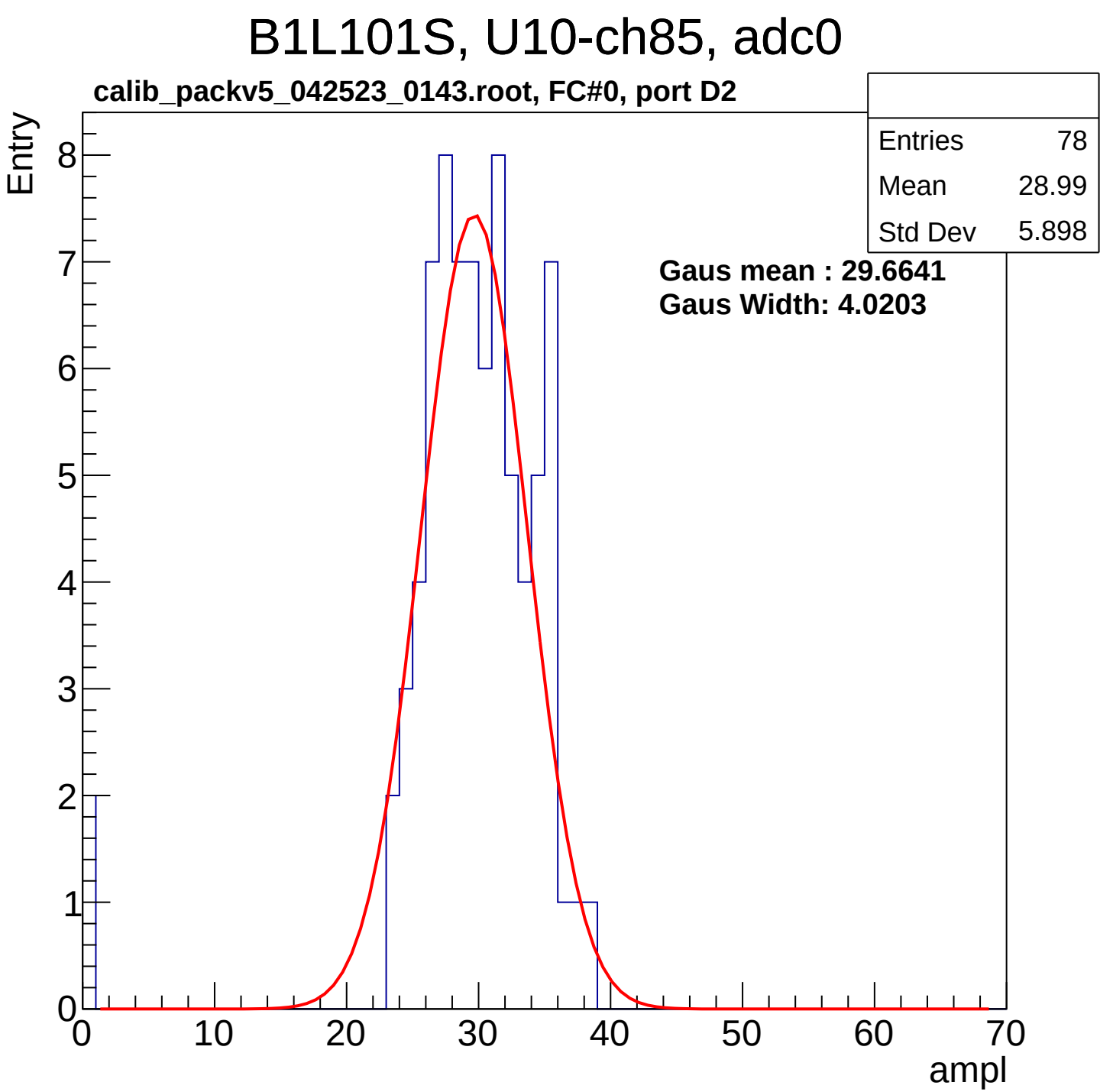
40
50
60
70
ampl


B1L101S, U10-ch85, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 28.99
Std Dev 5.898
Gaus mean : 29.6641
Gaus Width: 4.0203
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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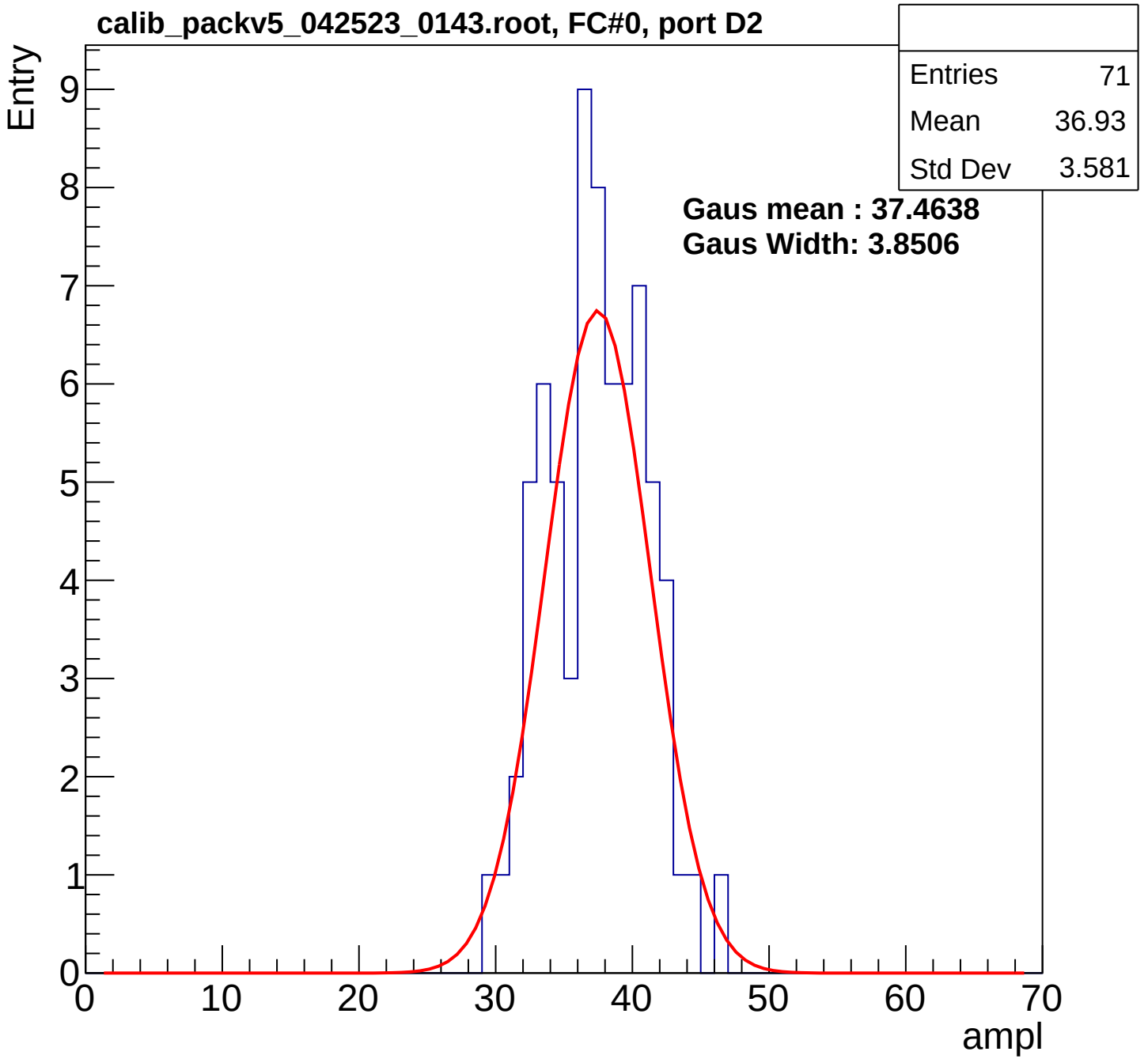
B1L101S, U10-ch85, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 36.93
Std Dev 3.581
Gaus mean : 37.4638
Gaus Width: 3.8506
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
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60
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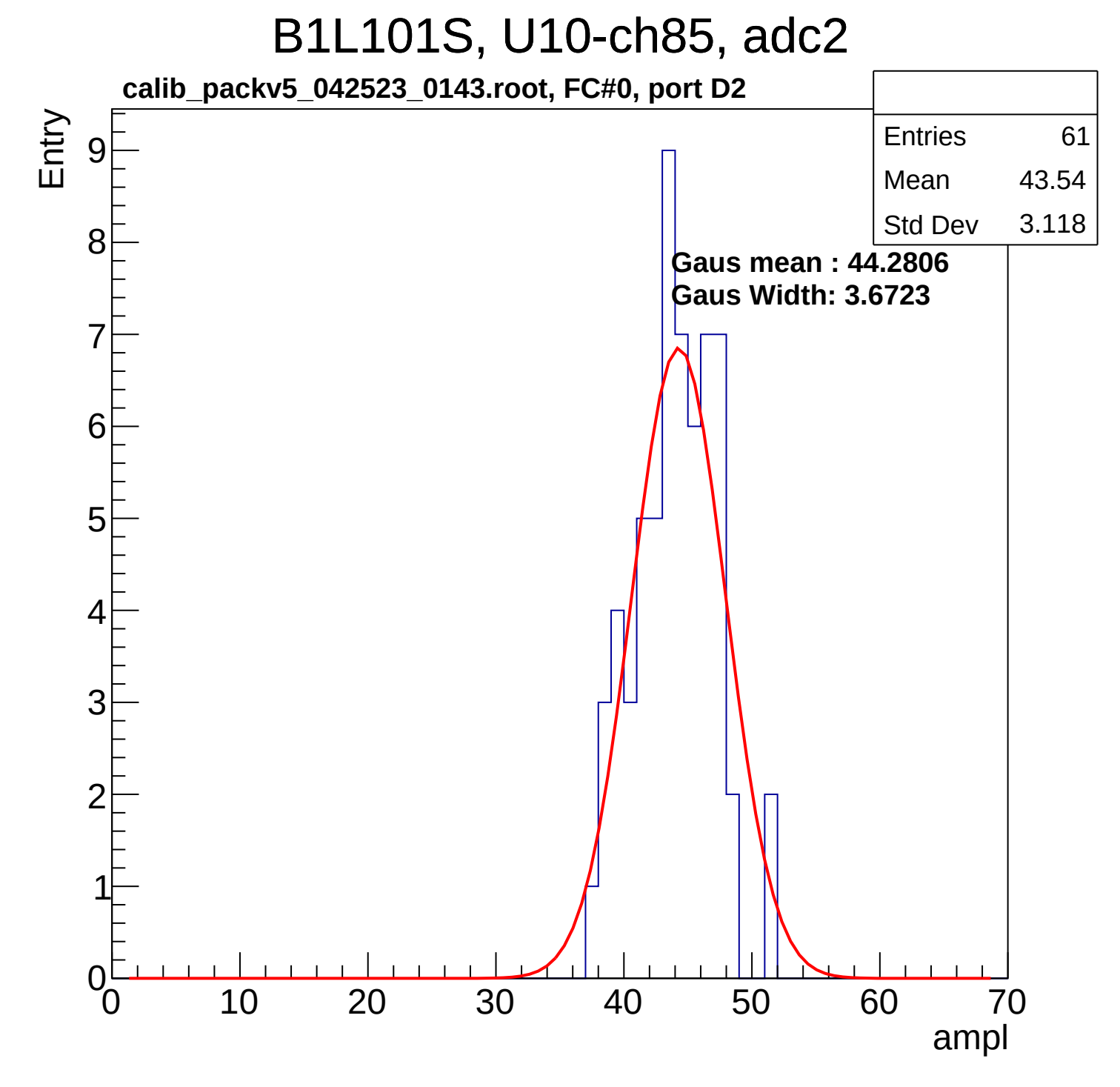
B1L101S, U10-ch85, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 43.54
Std Dev 3.118
Gaus mean : 44.2806
Gaus Width: 3.6723
Entry
ampl
0
1
2
3
4
5
6
7
8
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0
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40
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60
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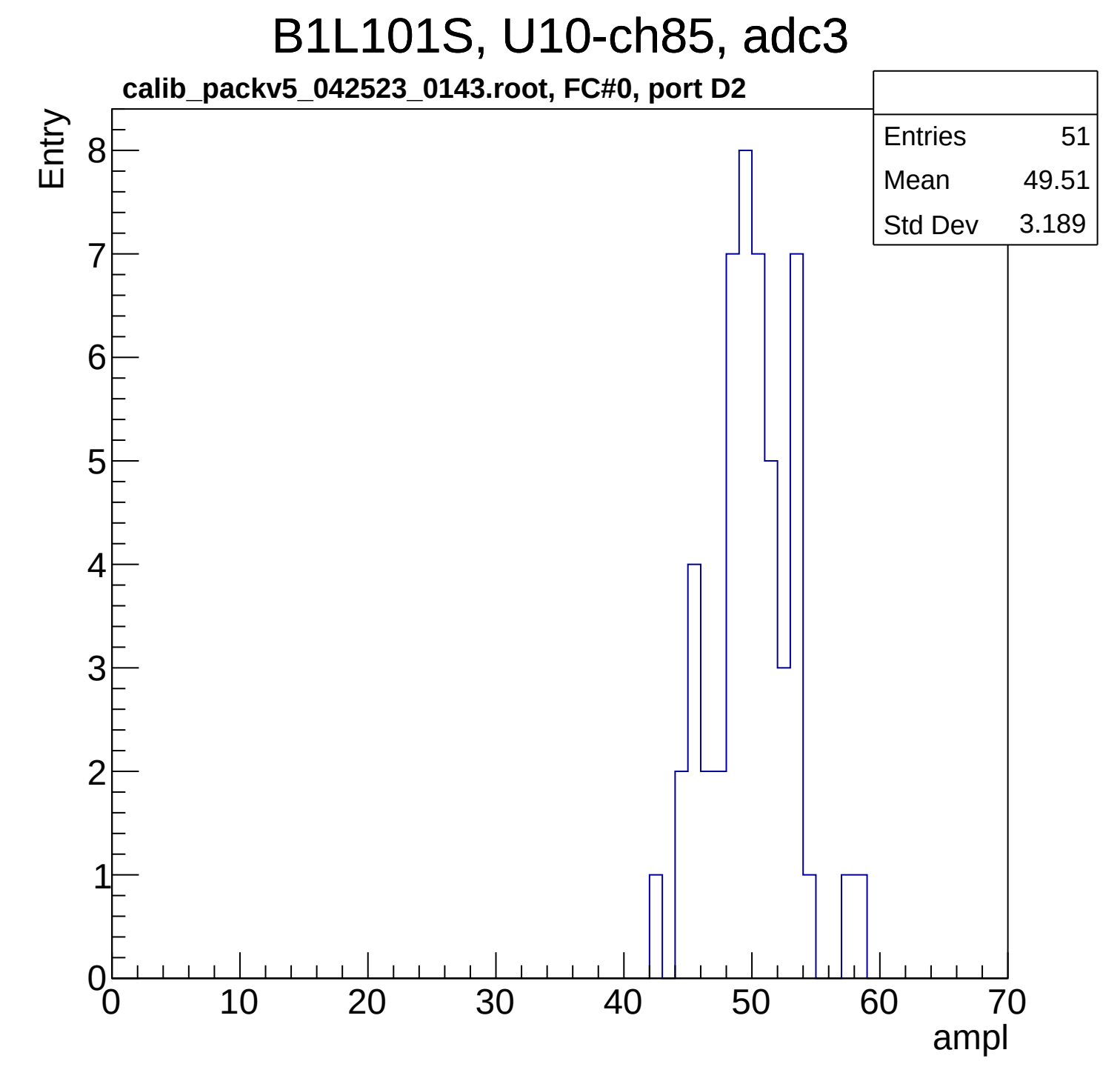
B1L101S, U10-ch85, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 49.51
Std Dev 3.189
Entry
ampl
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1
2
3
4
5
6
7
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0
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60
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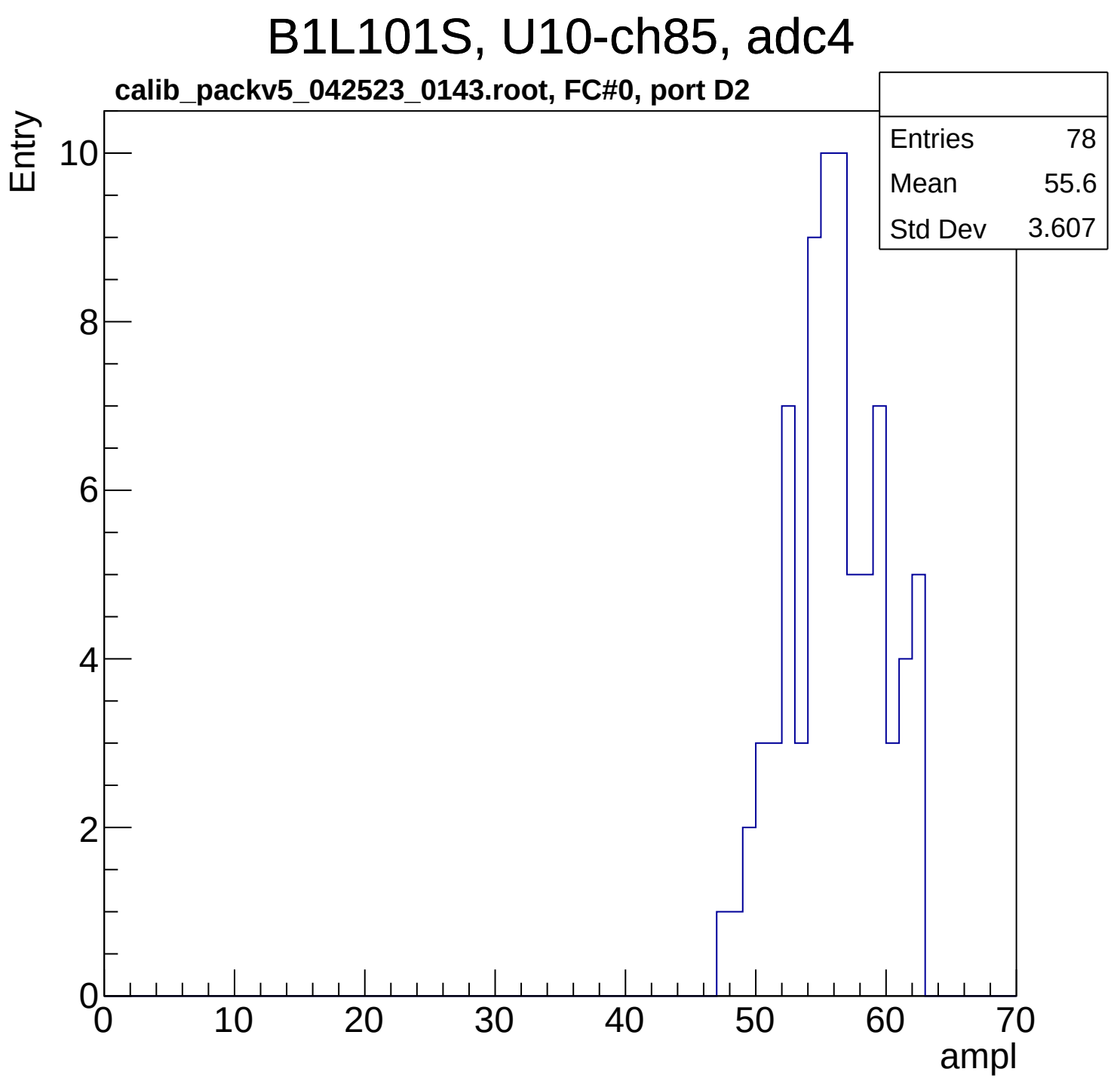
B1L101S, U10-ch85, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 55.6
Std Dev 3.607
Entry
ampl
0
2
4
6
8
10
0
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20
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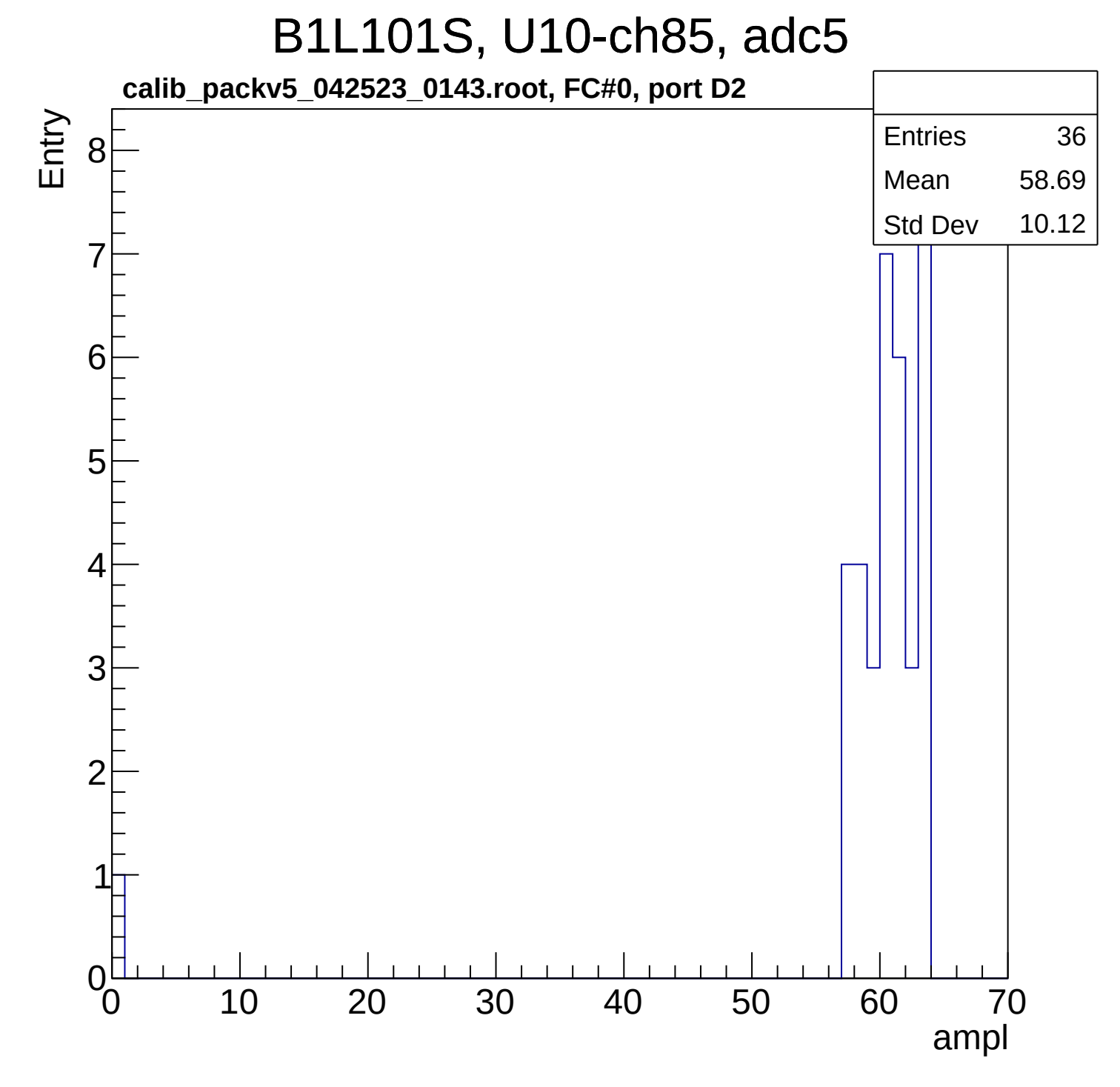
B1L101S, U10-ch85, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 36
Mean 58.69
Std Dev 10.12
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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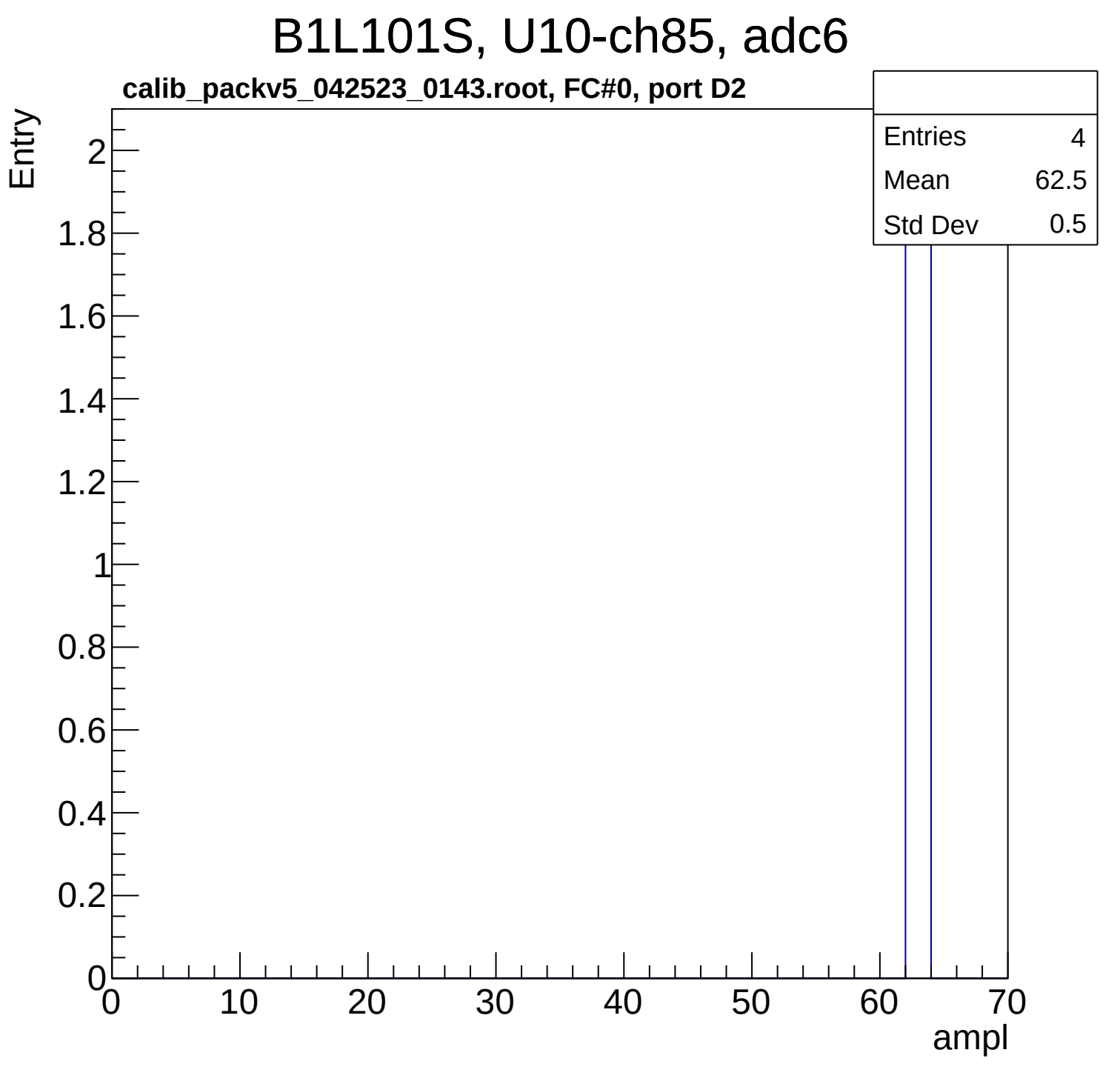
B1L101S, U10-ch85, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 62.5
Std Dev 0.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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40
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60
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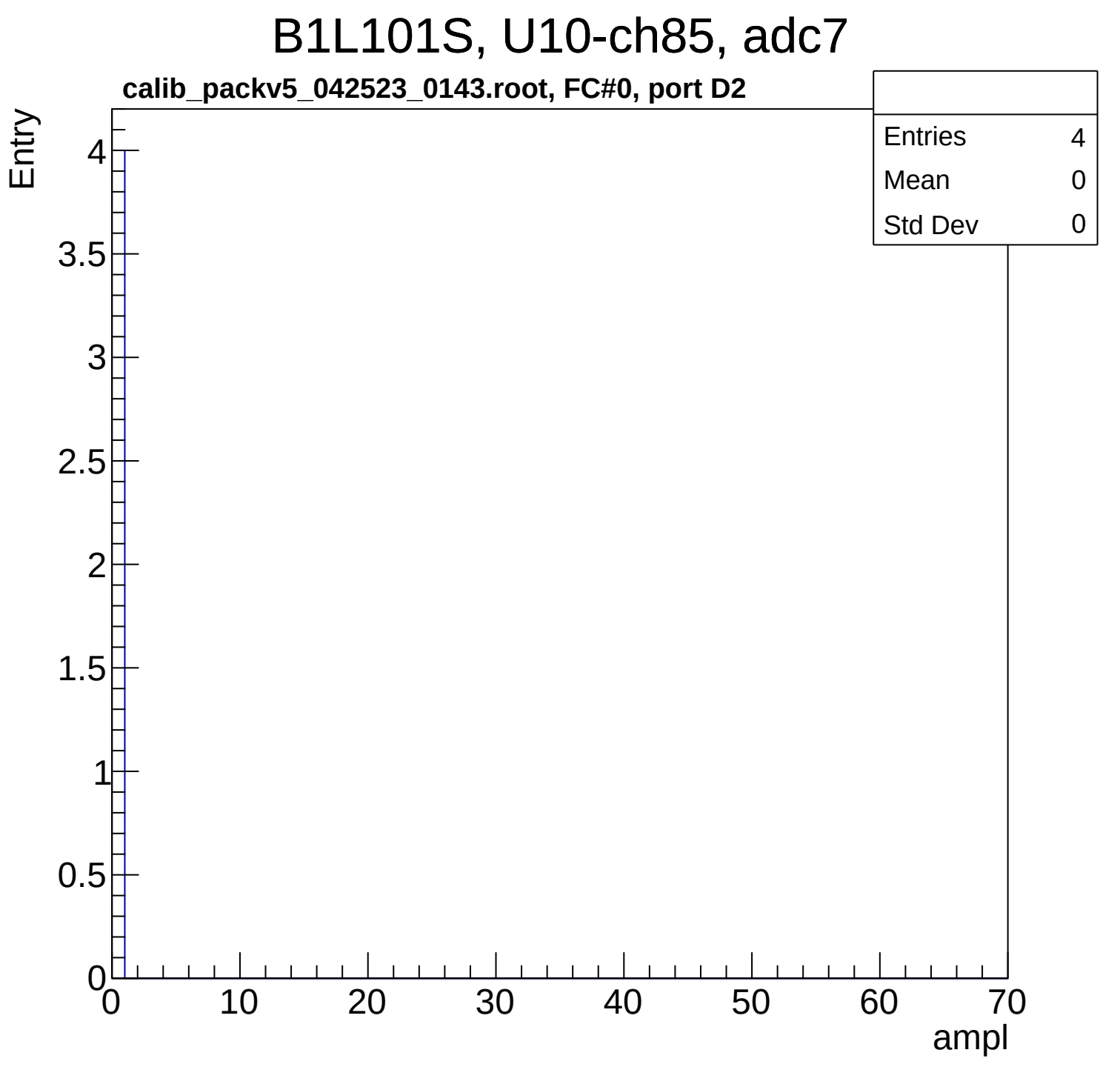
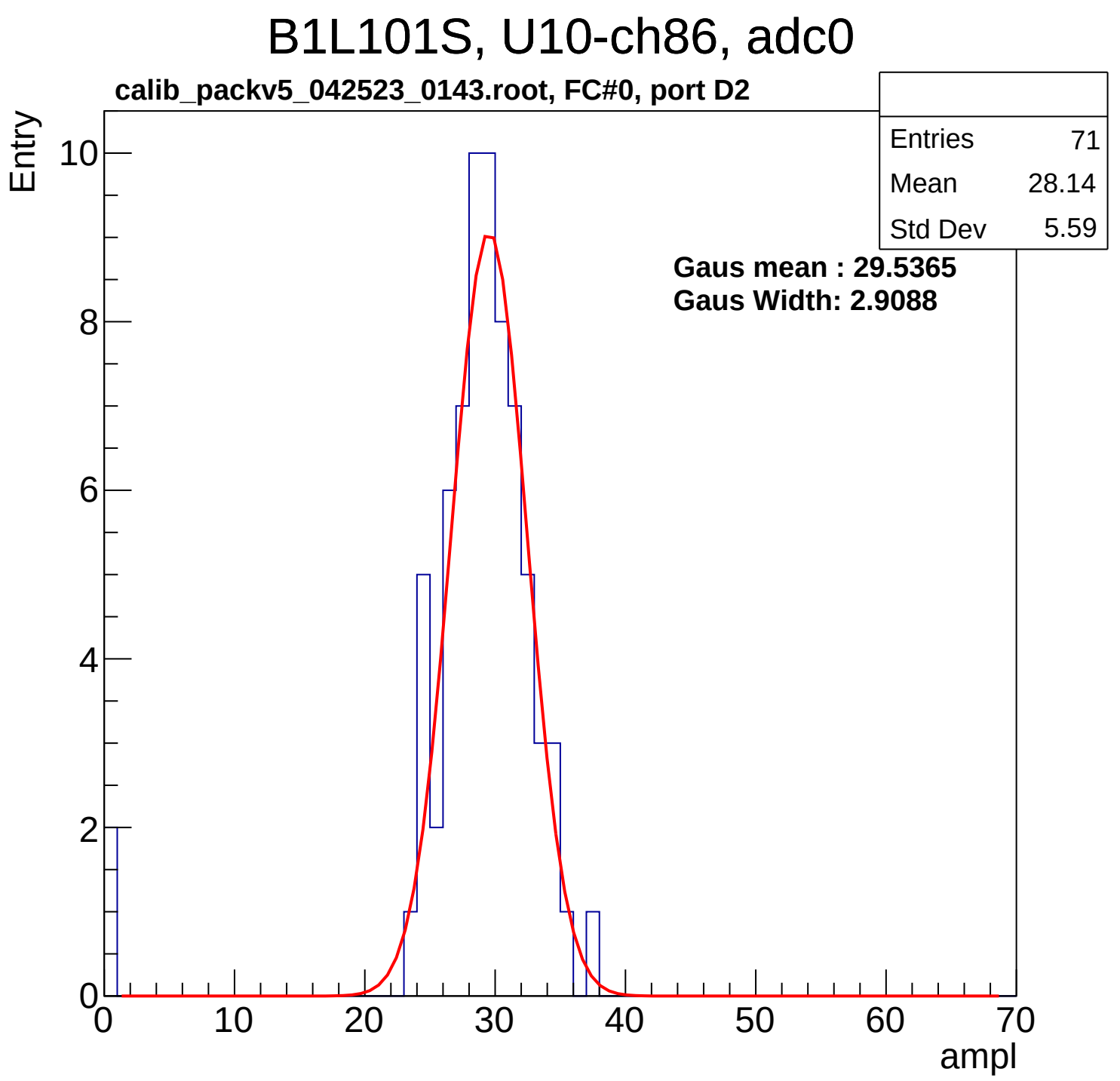
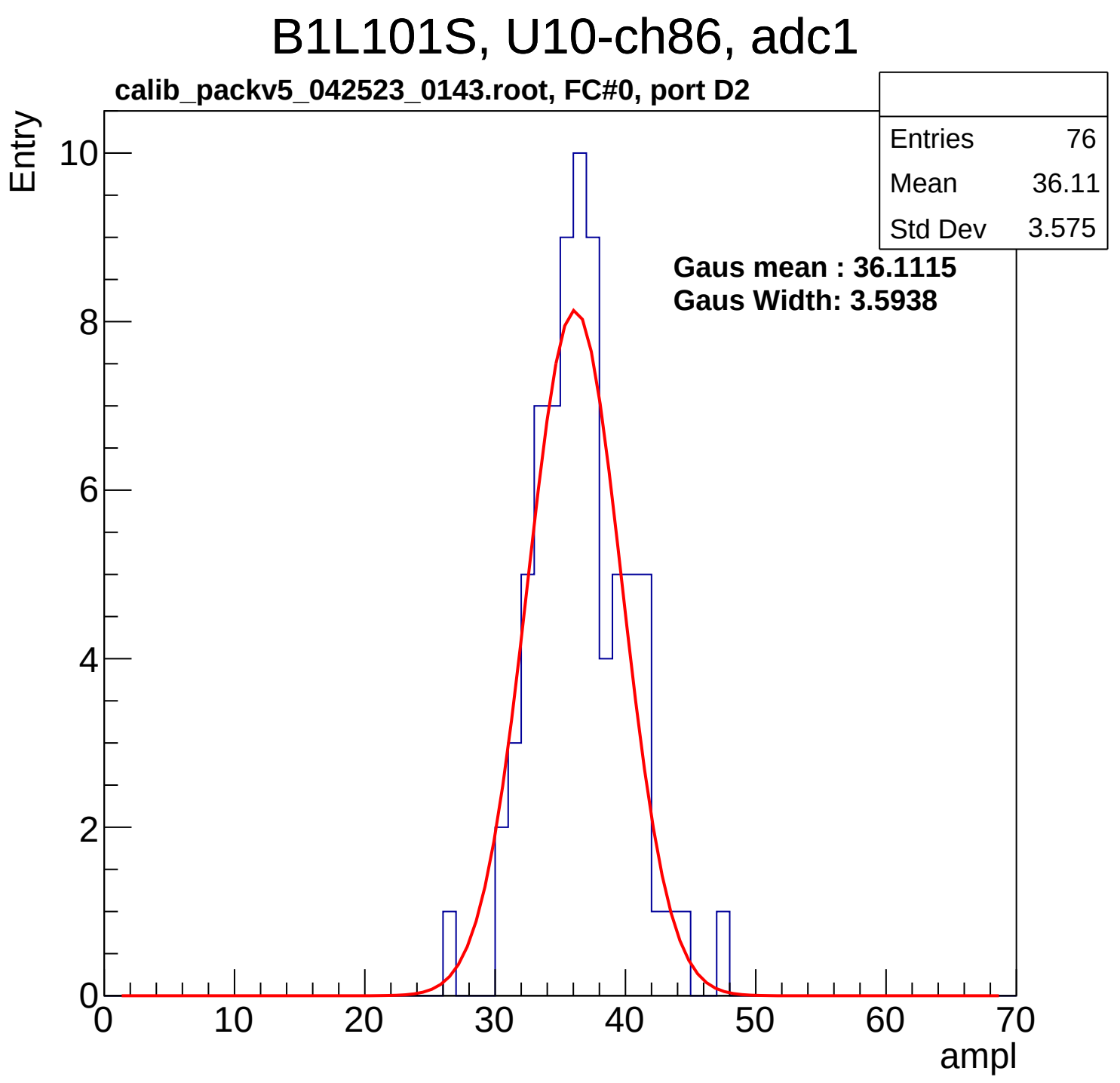

B1L101S, U10-ch85, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 0
Std Dev 0
Entry
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch86, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 28.14
Std Dev 5.59
Gaus mean : 29.5365
Gaus Width: 2.9088
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch86, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 36.11
Std Dev 3.575
Gaus mean : 36.1115
Gaus Width: 3.5938
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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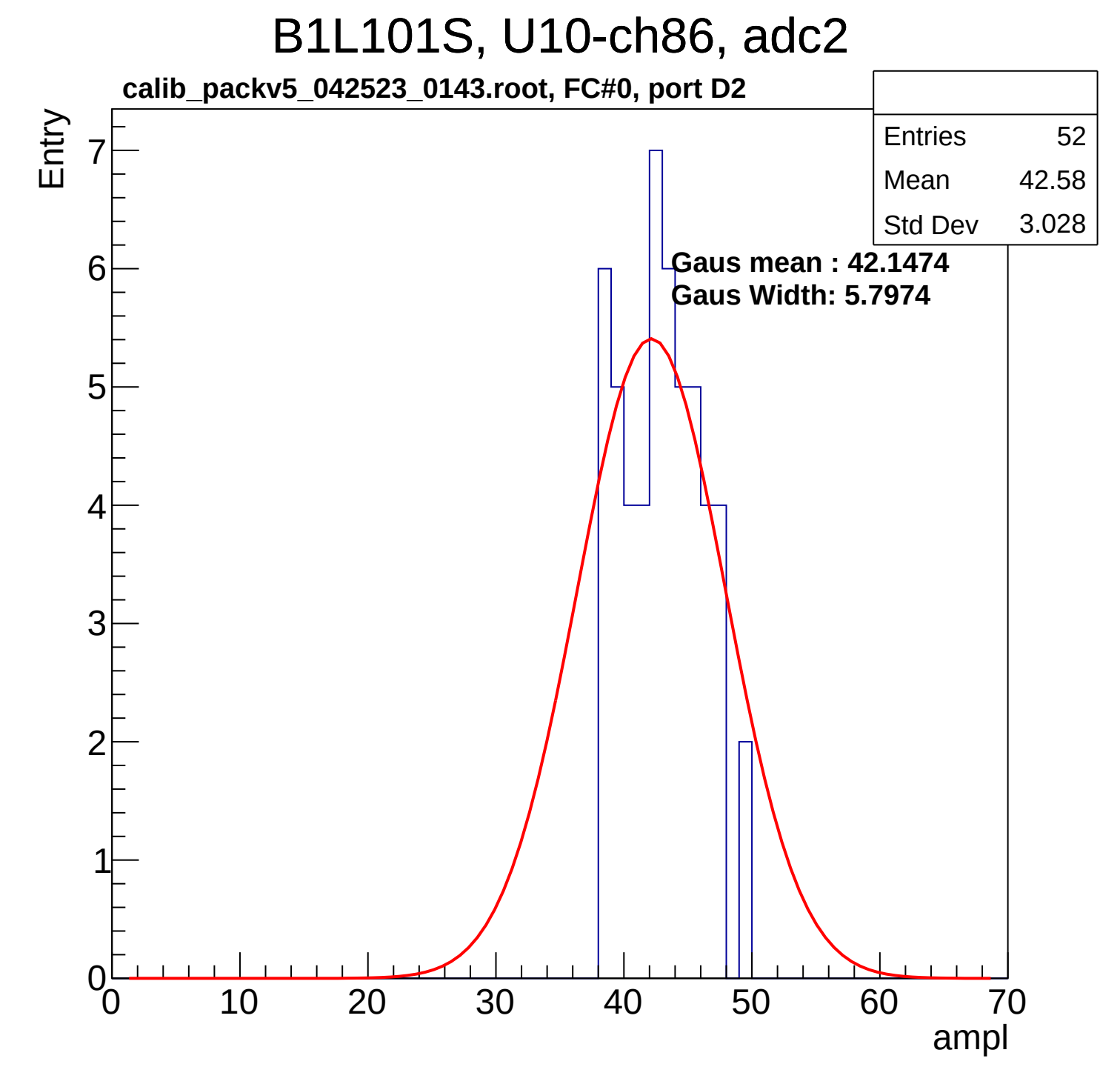
B1L101S, U10-ch86, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 42.58
Std Dev 3.028
Gaus mean : 42.1474
Gaus Width: 5.7974
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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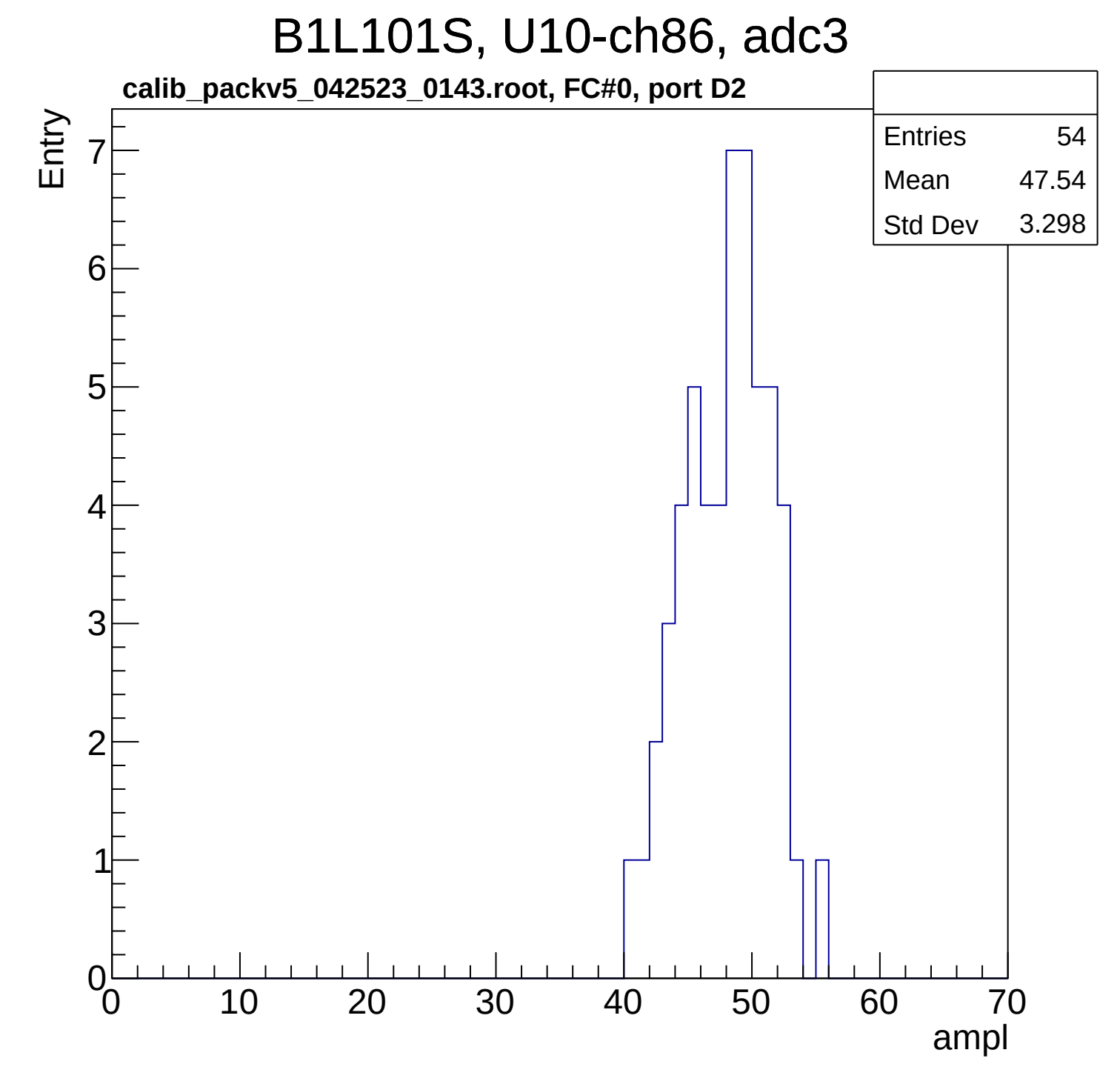
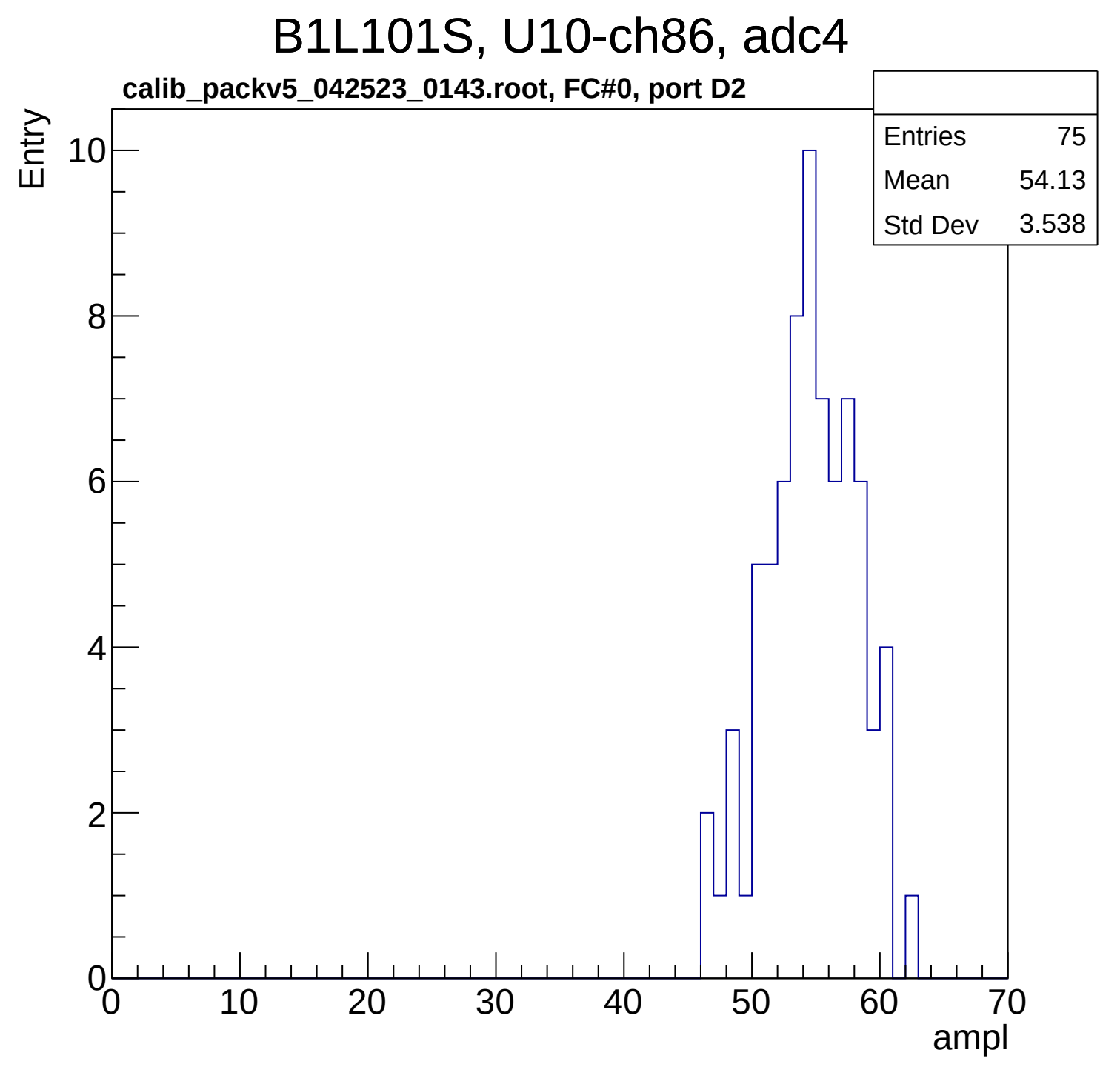
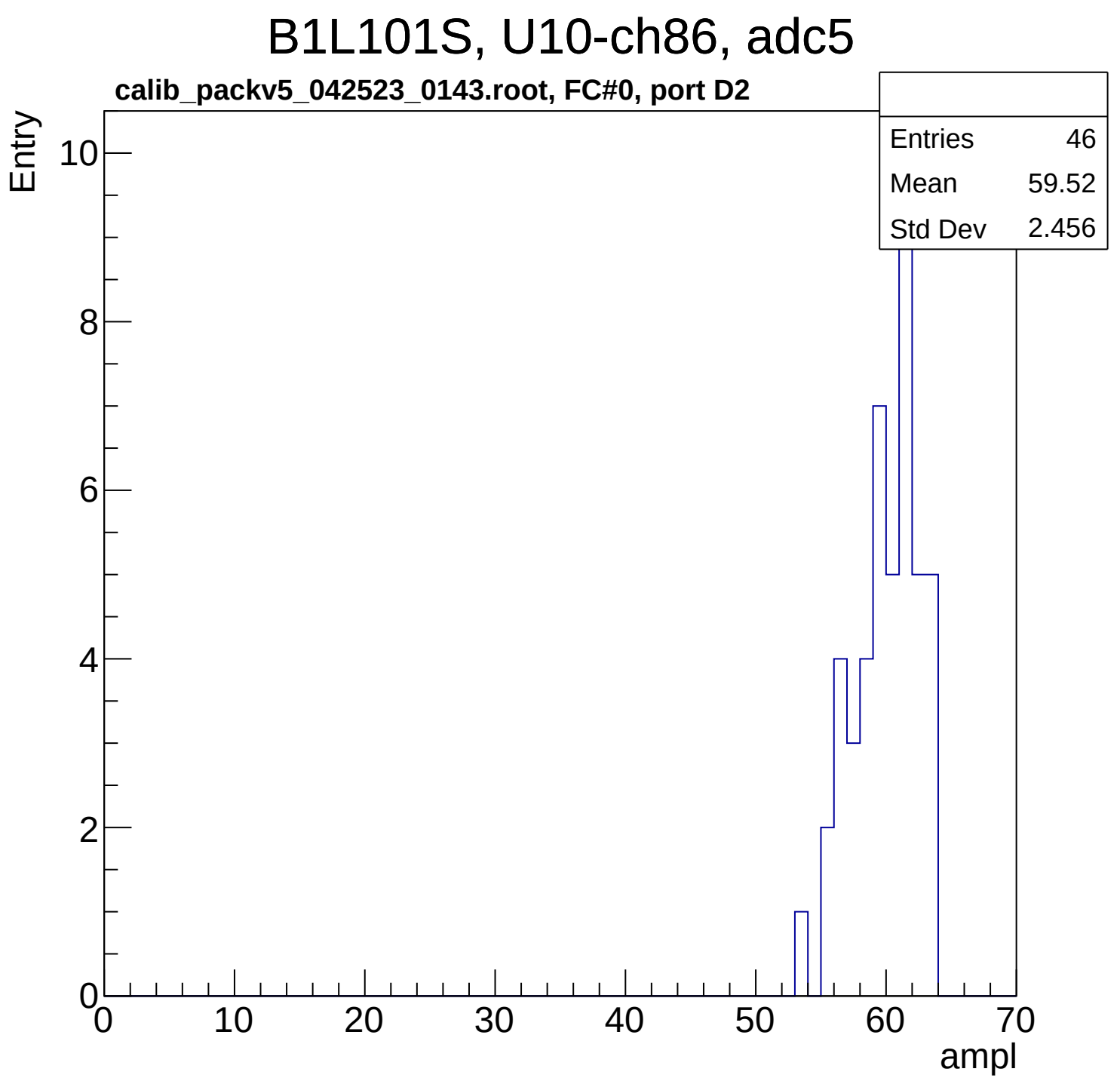
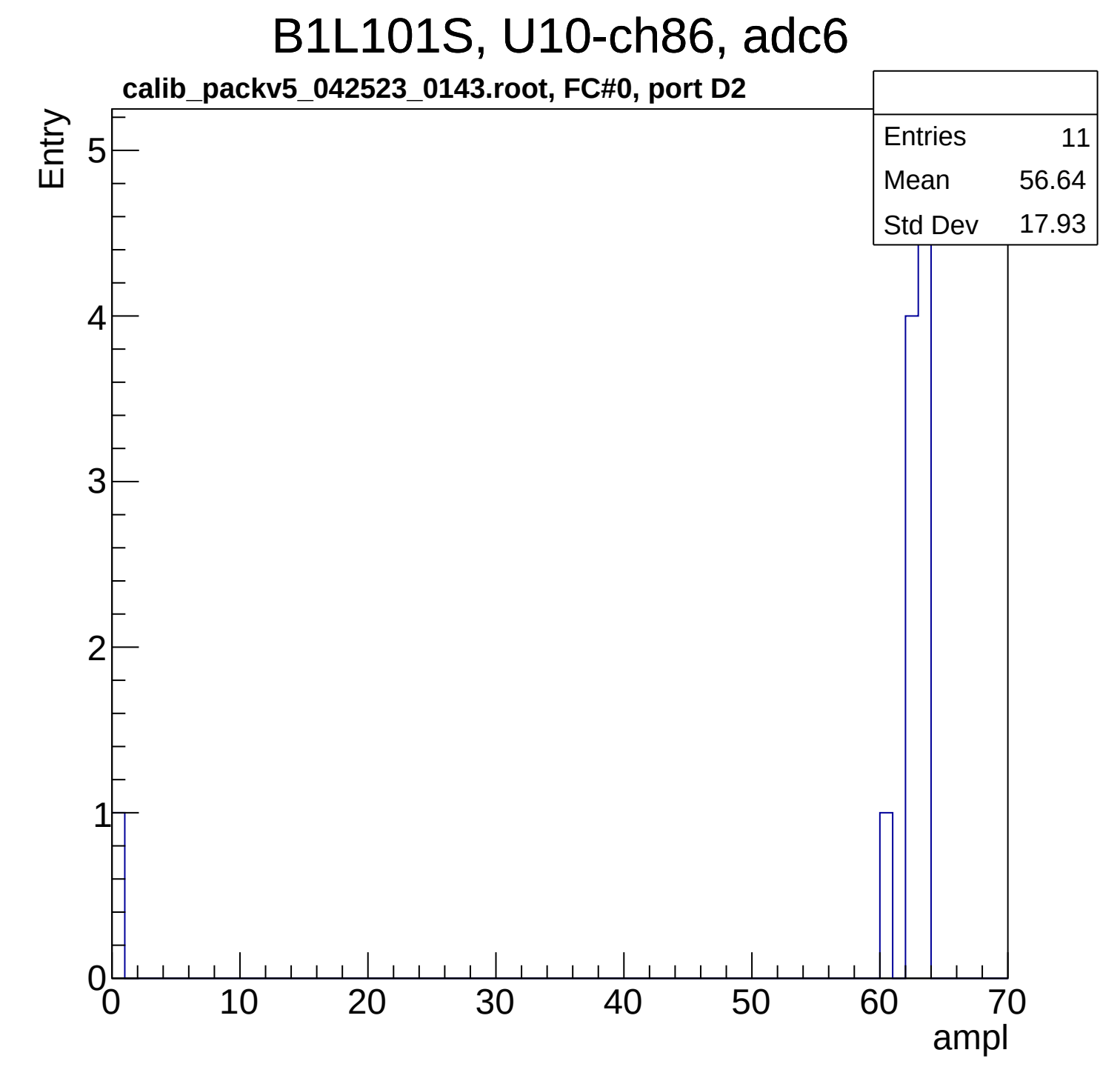
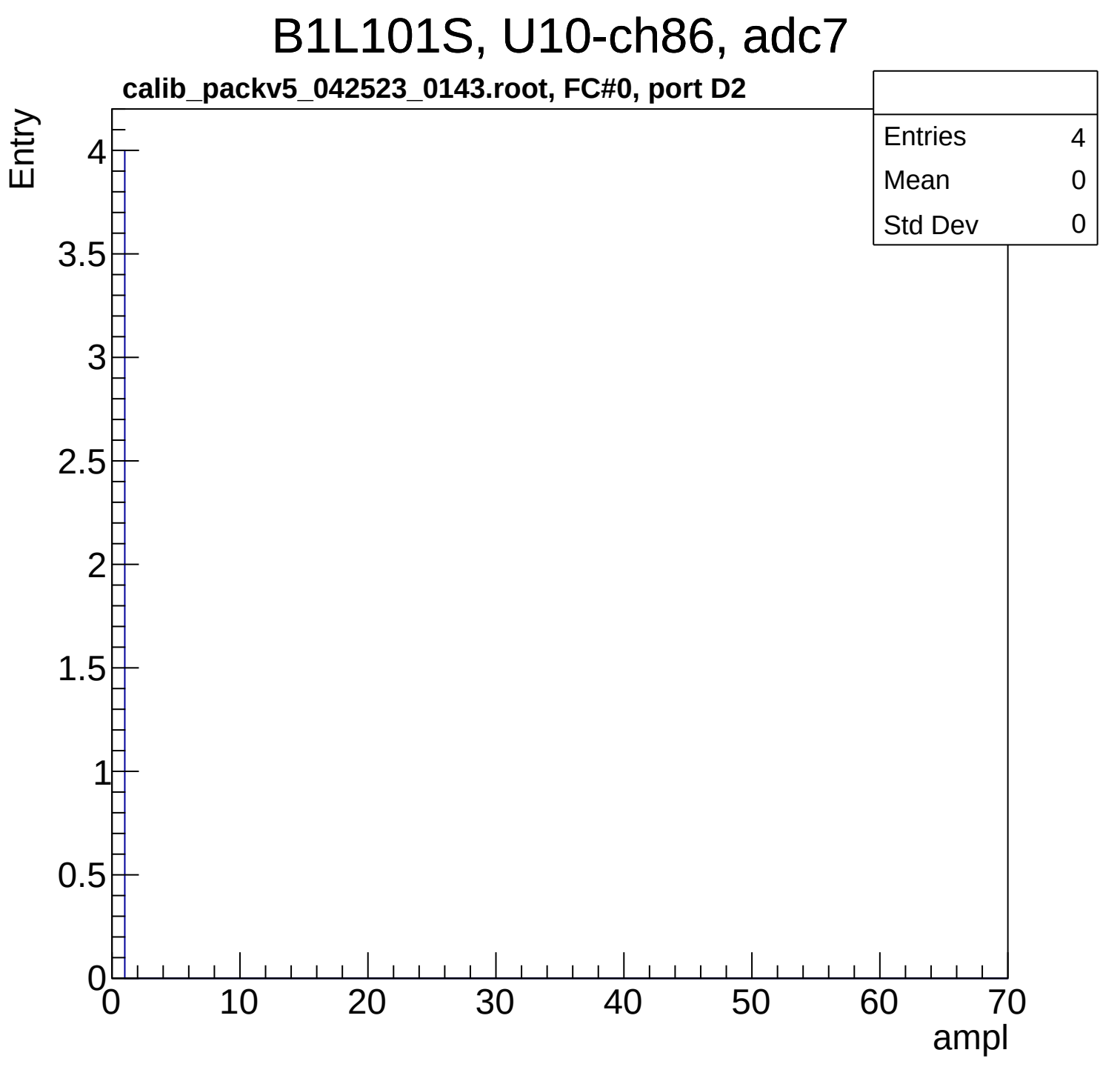
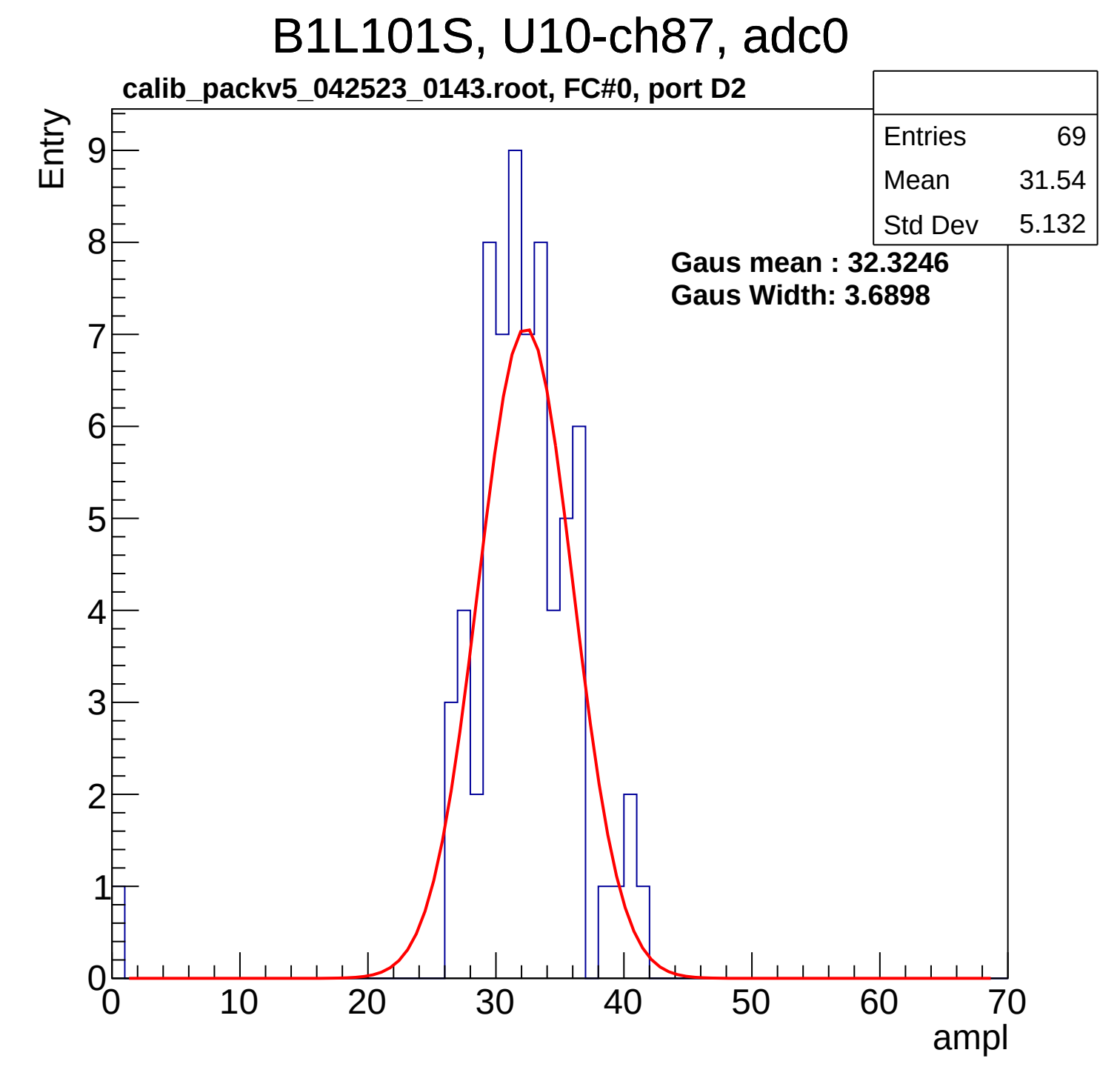

B1L101S, U10-ch86, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 47.54
Std Dev 3.298
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U10-ch86, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 54.13
Std Dev 3.538
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch86, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 59.52
Std Dev 2.456
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch86, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 11
Mean 56.64
Std Dev 17.93
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch86, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 0
Std Dev 0
Entry
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch87, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 31.54
Std Dev 5.132
Gaus mean : 32.3246
Gaus Width: 3.6898
Entry
ampl
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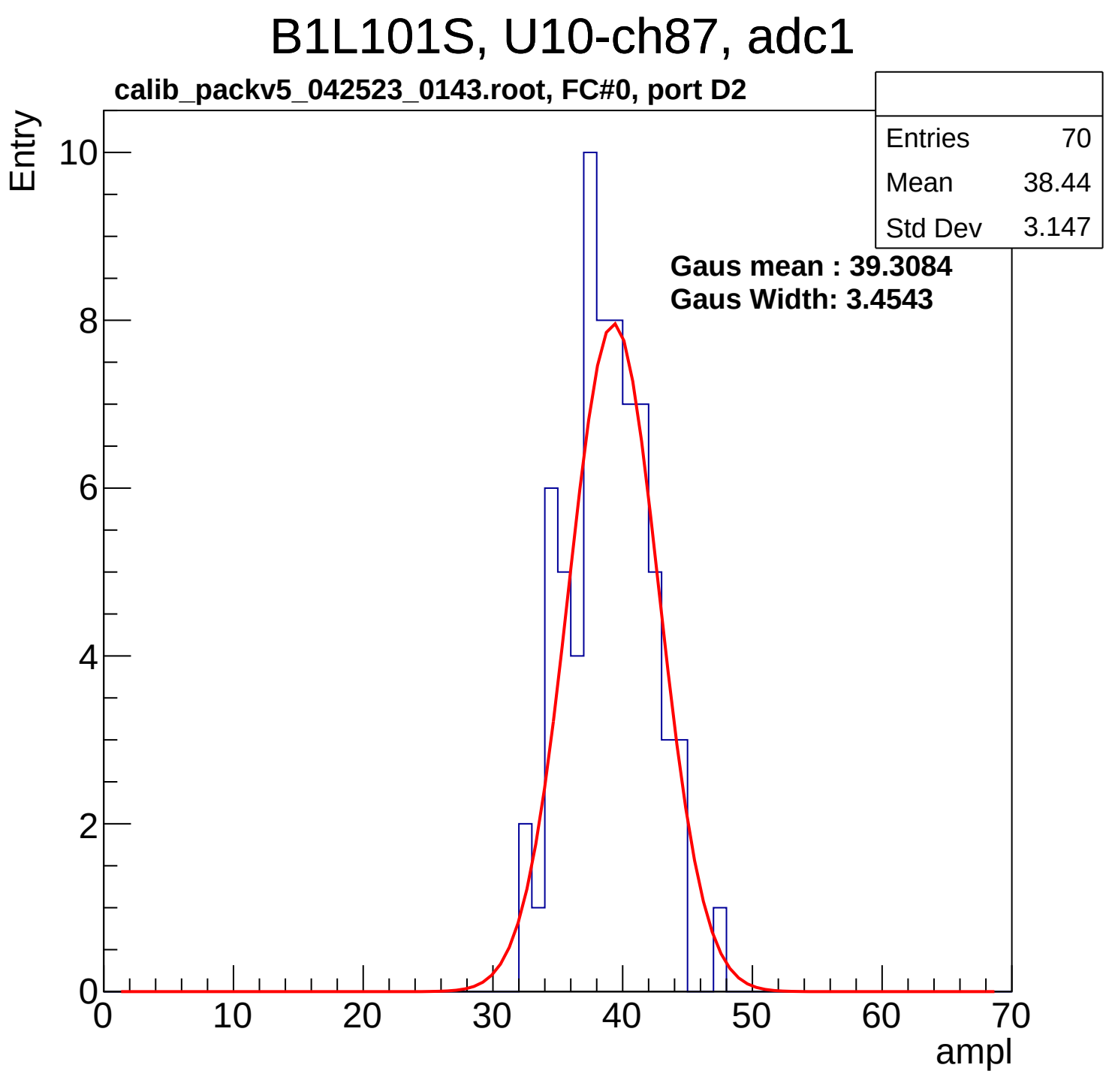
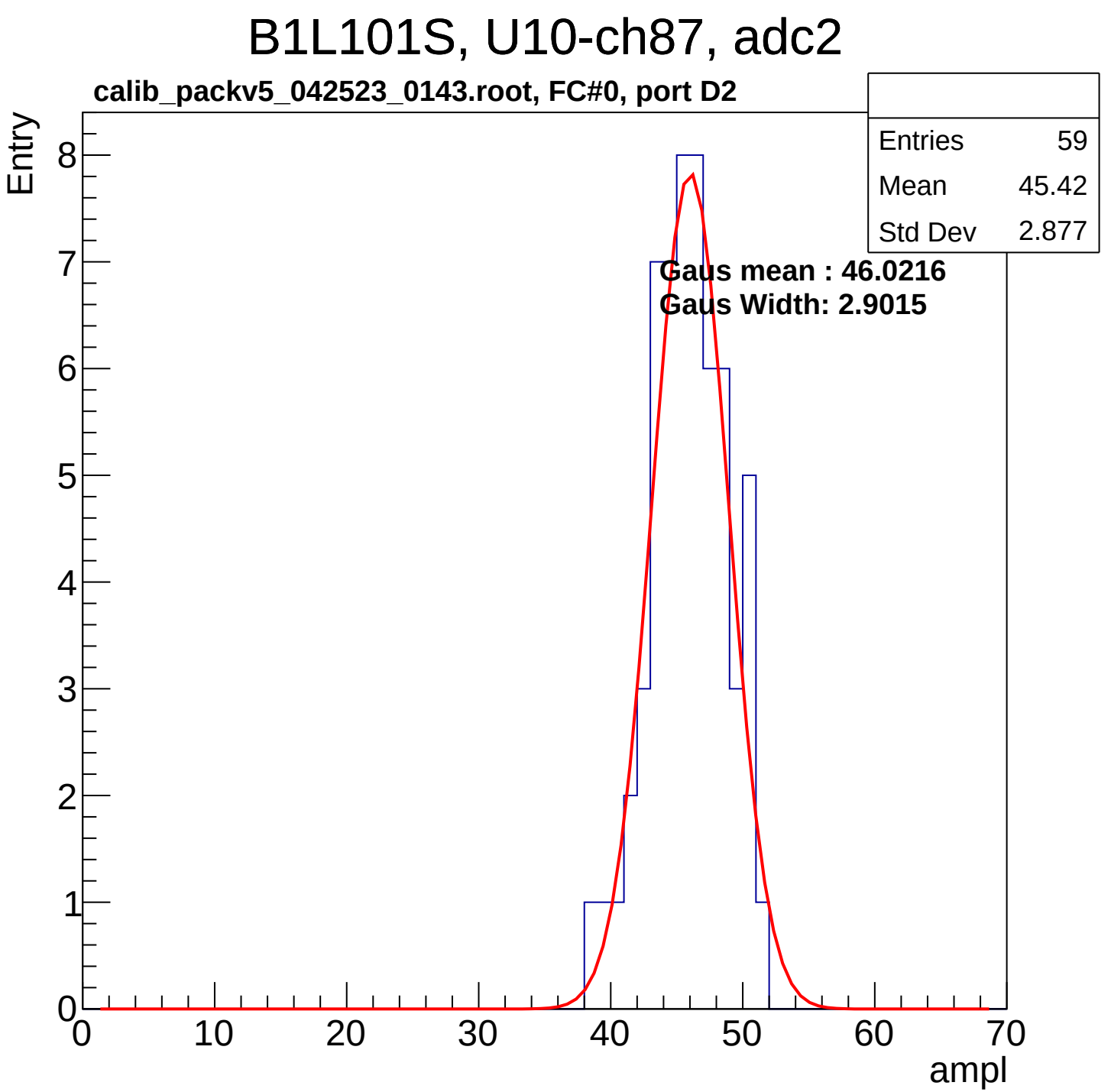
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch87, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 38.44
Std Dev 3.147
Gaus mean : 39.3084
Gaus Width: 3.4543
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch87, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 45.42
Std Dev 2.877
Gaus mean : 46.0216
Gaus Width: 2.9015
Entry
ampl
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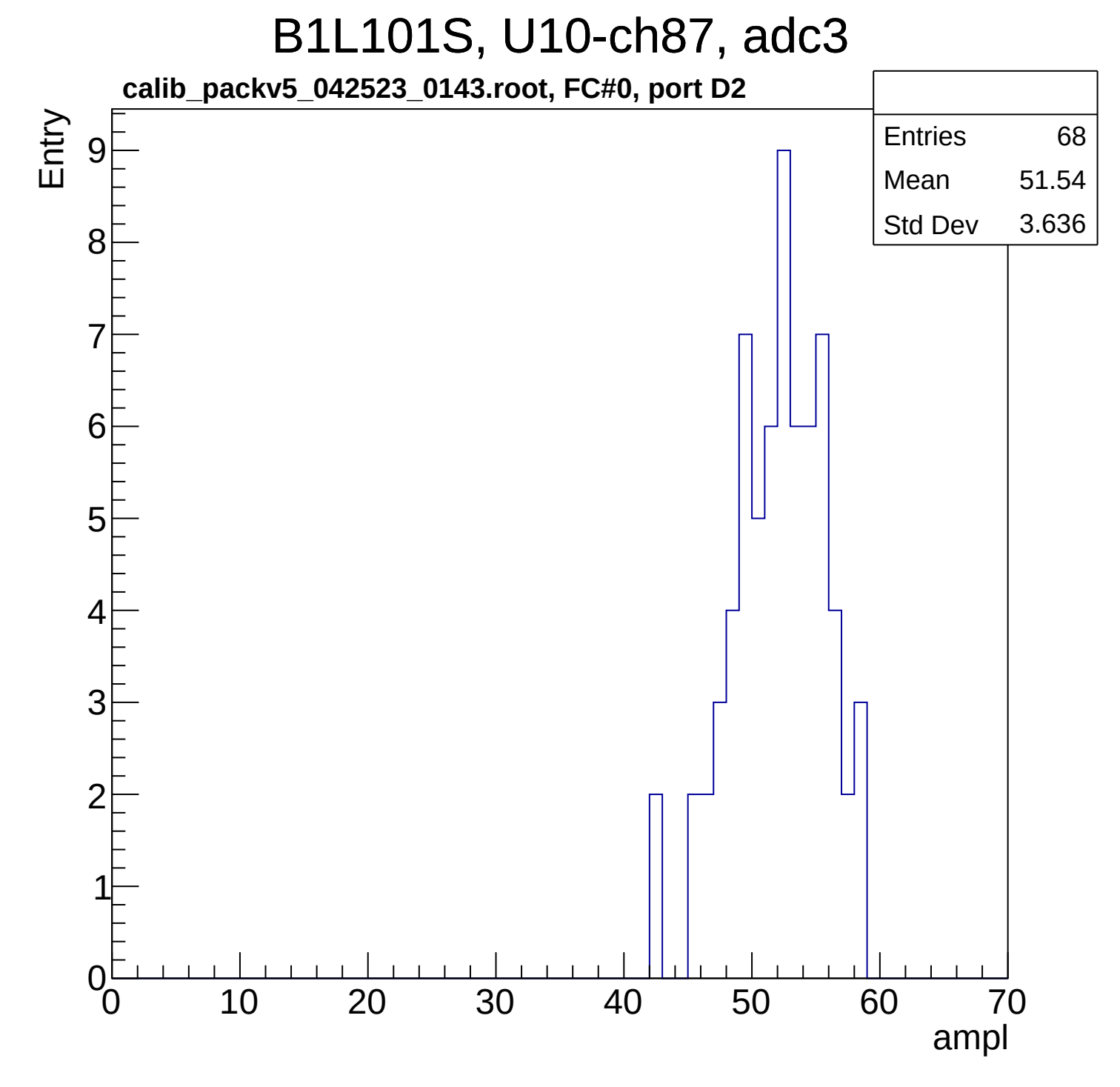
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch87, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 51.54
Std Dev 3.636
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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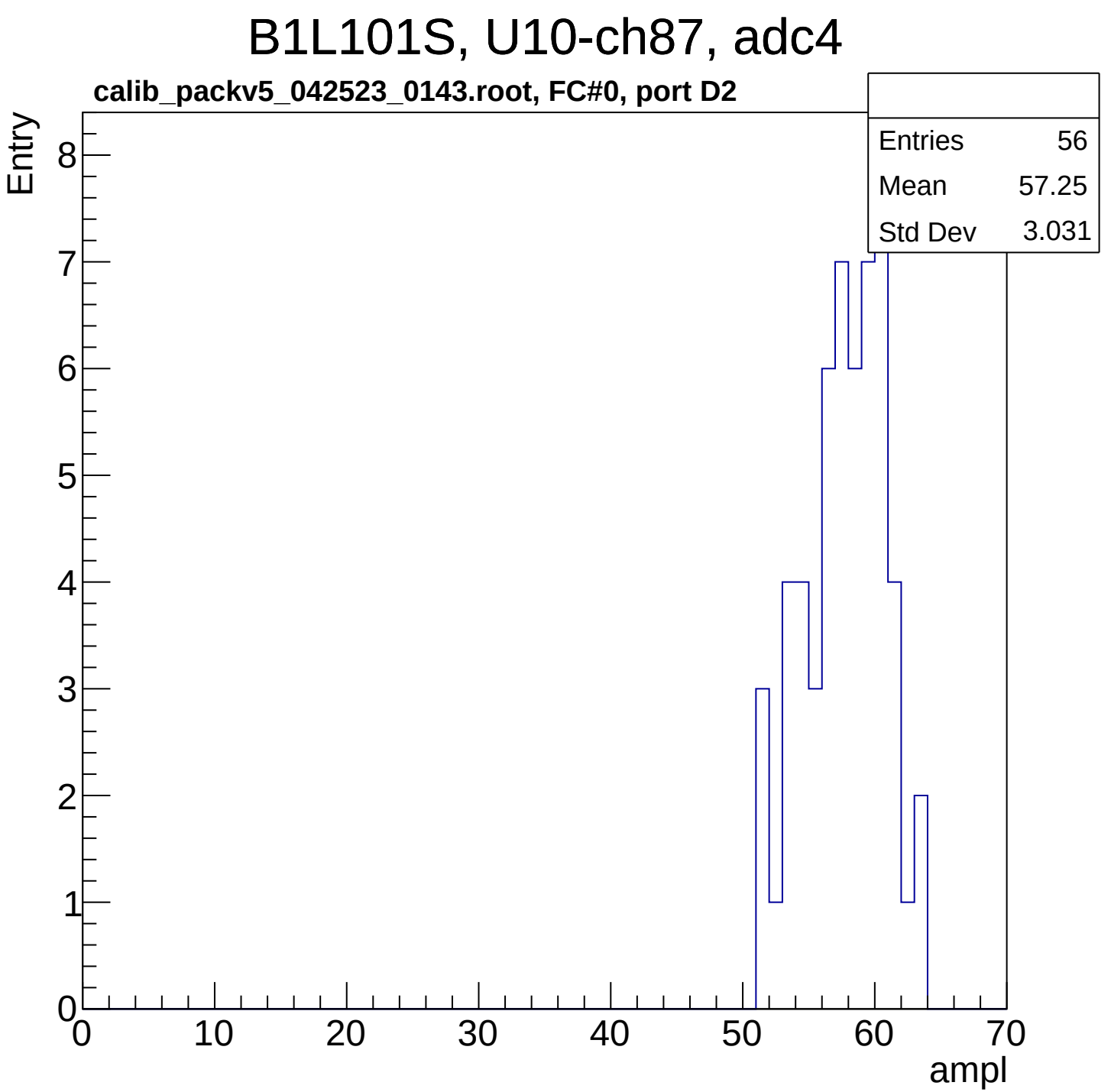
B1L101S, U10-ch87, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 57.25
Std Dev 3.031
Entry
ampl
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2
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5
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7
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0
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20
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40
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60
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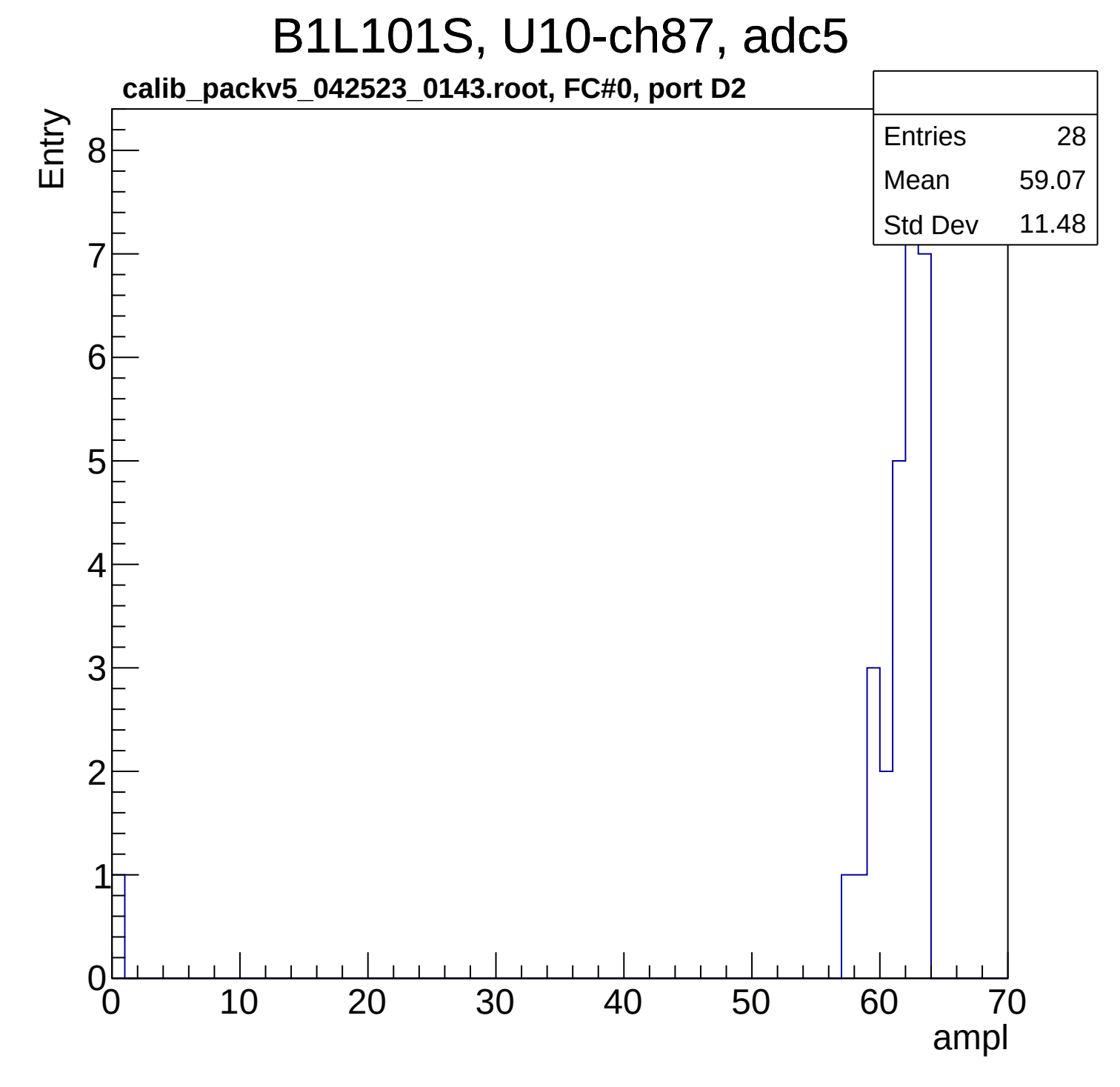
B1L101S, U10-ch87, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 28
Mean 59.07
Std Dev 11.48
Entry
ampl
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2
3
4
5
6
7
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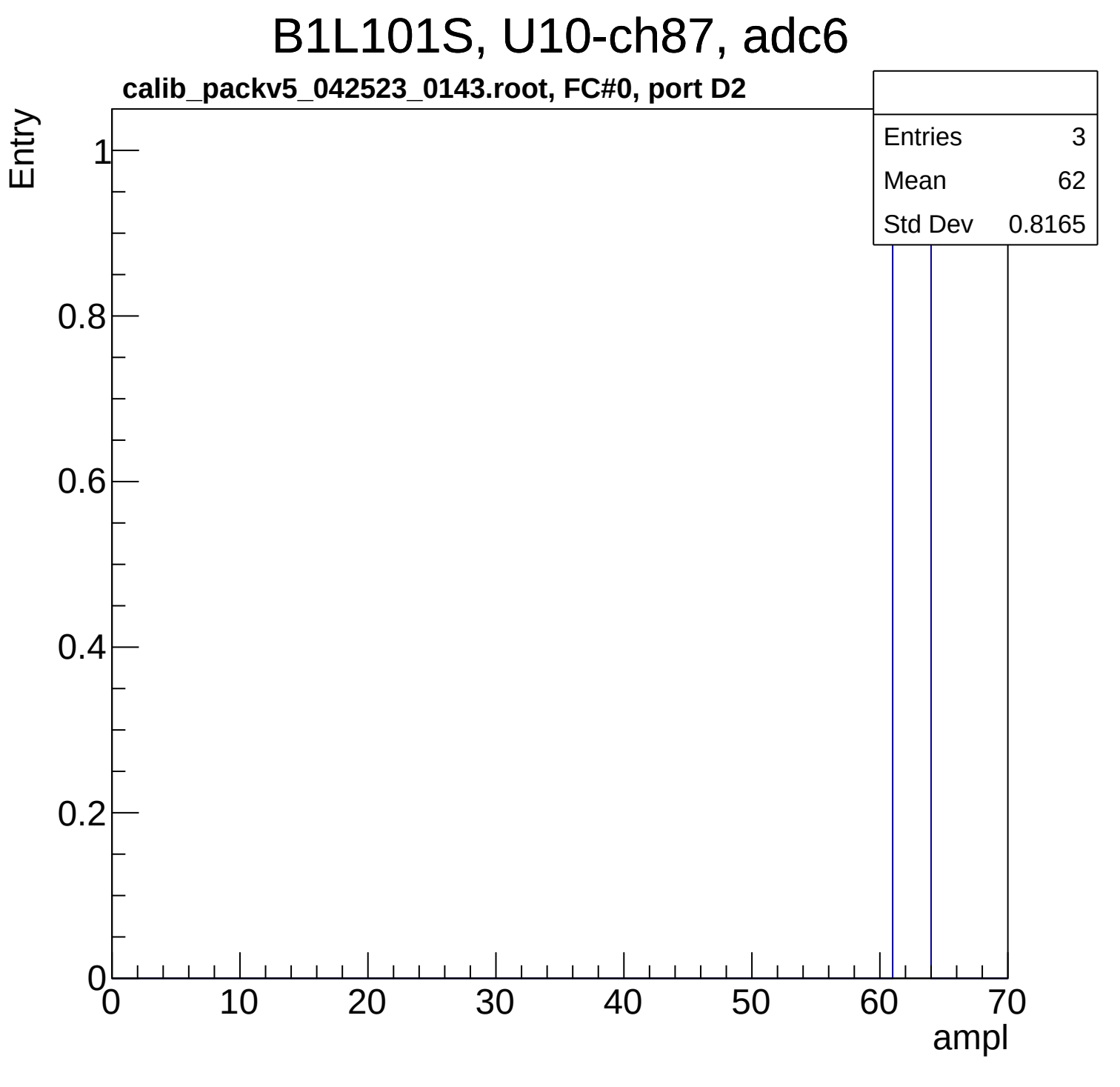
0
10
20
30
40
50
60
70


B1L101S, U10-ch87, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 62
Std Dev 0.8165
Entry
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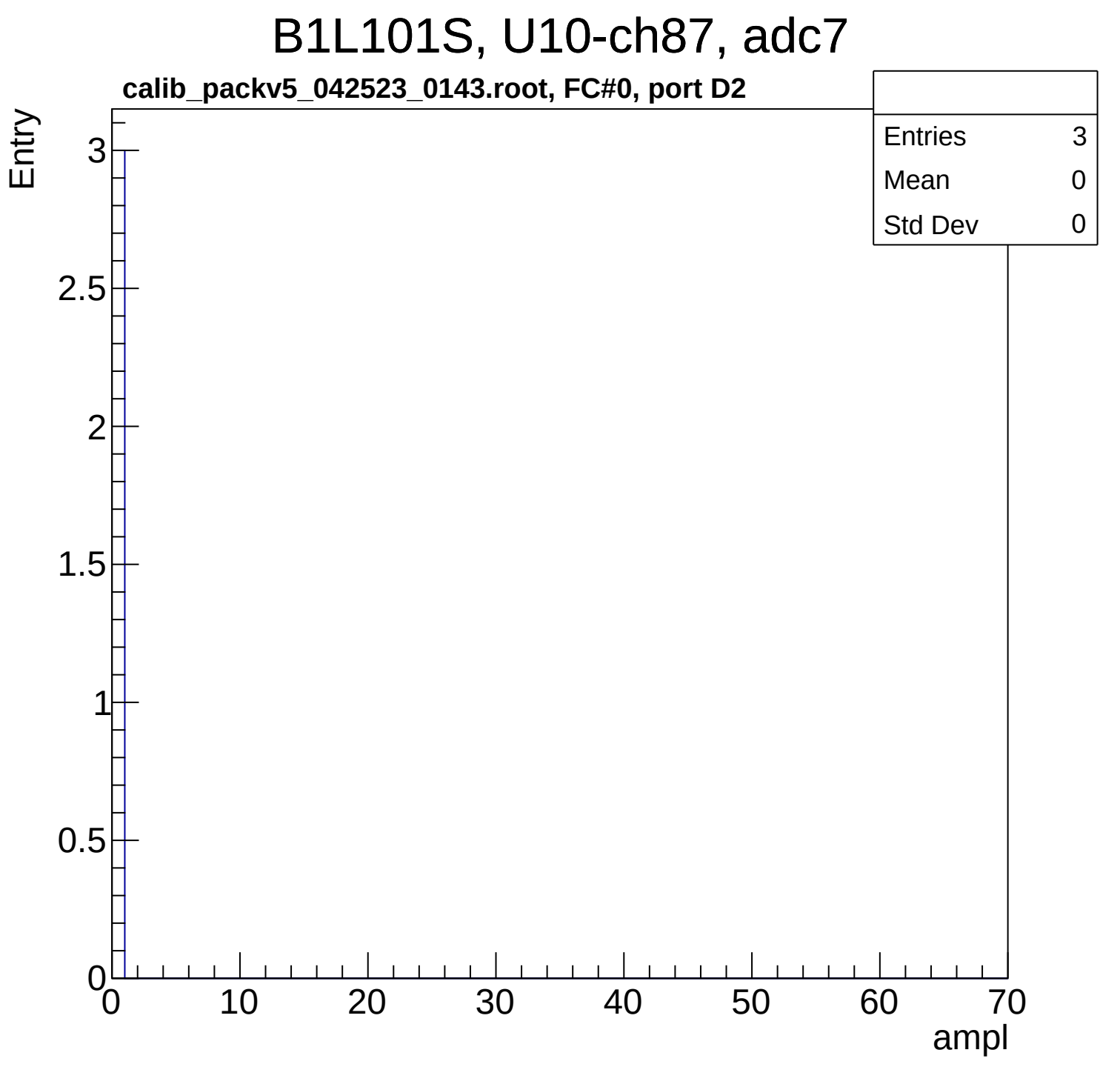
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch87, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 0
Std Dev 0
Entry
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2.5
2
1.5
1
0.5
0
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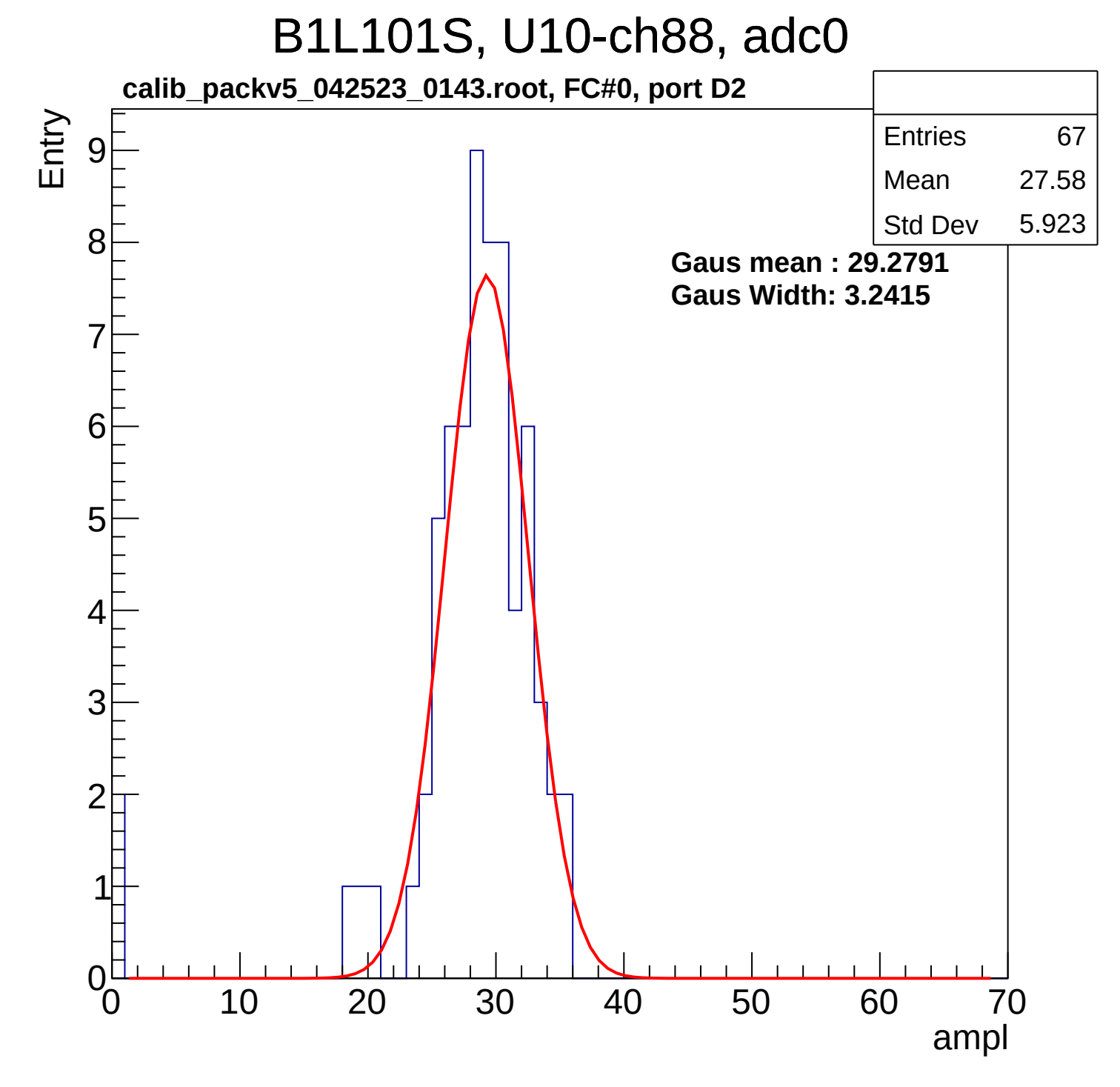
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch88, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 27.58
Std Dev 5.923
Gaus mean : 29.2791
Gaus Width: 3.2415
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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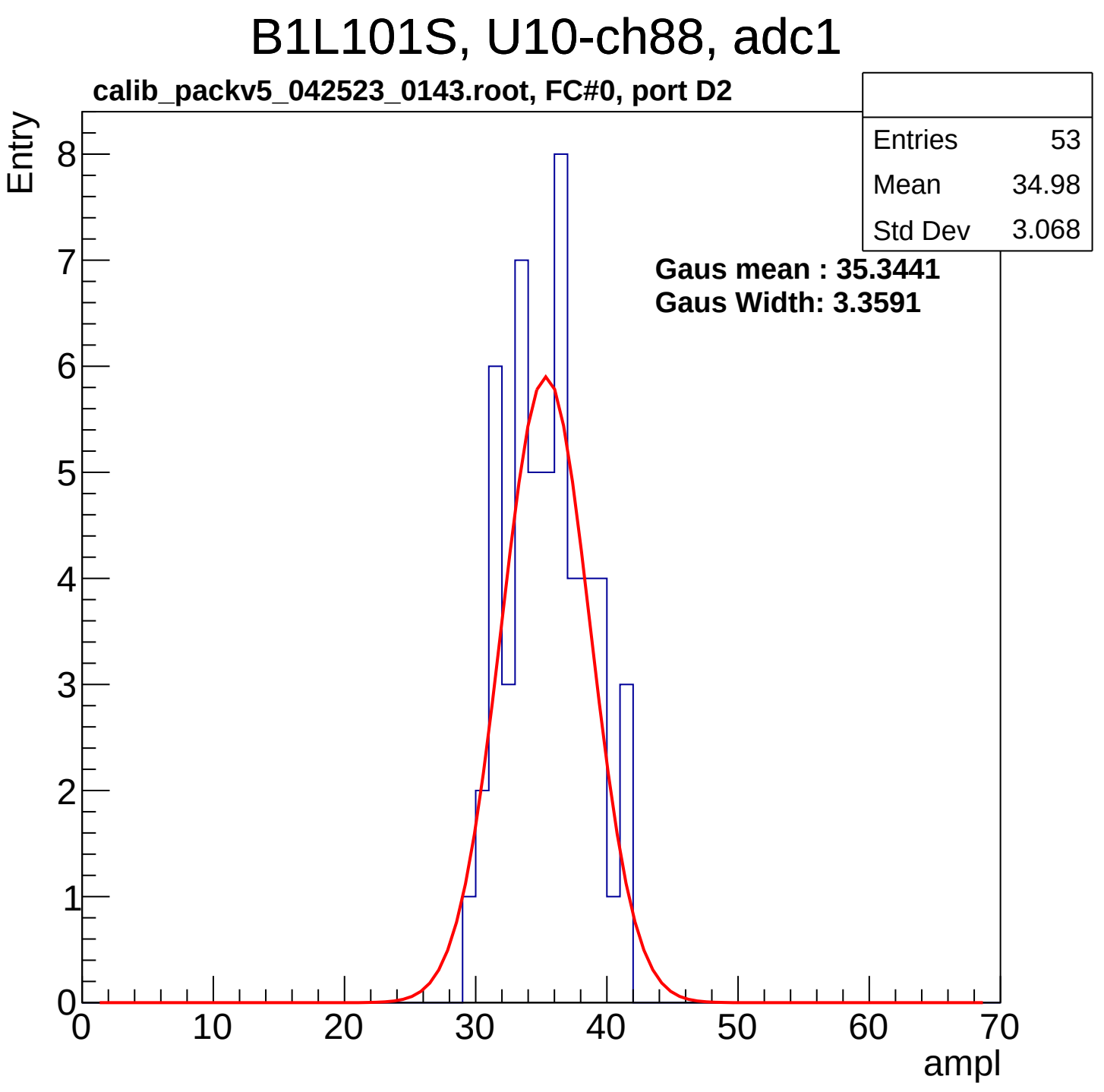
B1L101S, U10-ch88, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 34.98
Std Dev 3.068
Gaus mean : 35.3441
Gaus Width: 3.3591
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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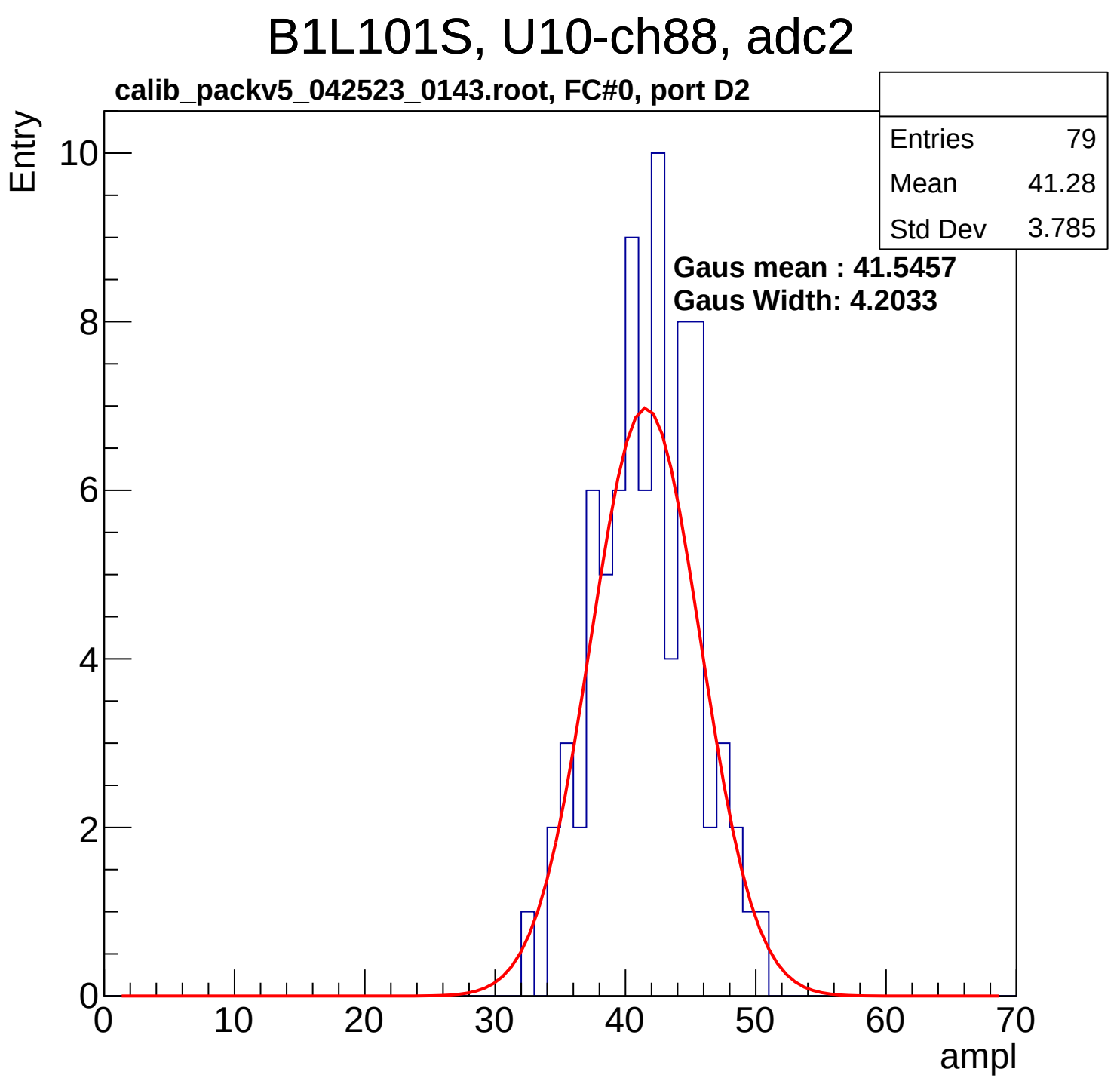
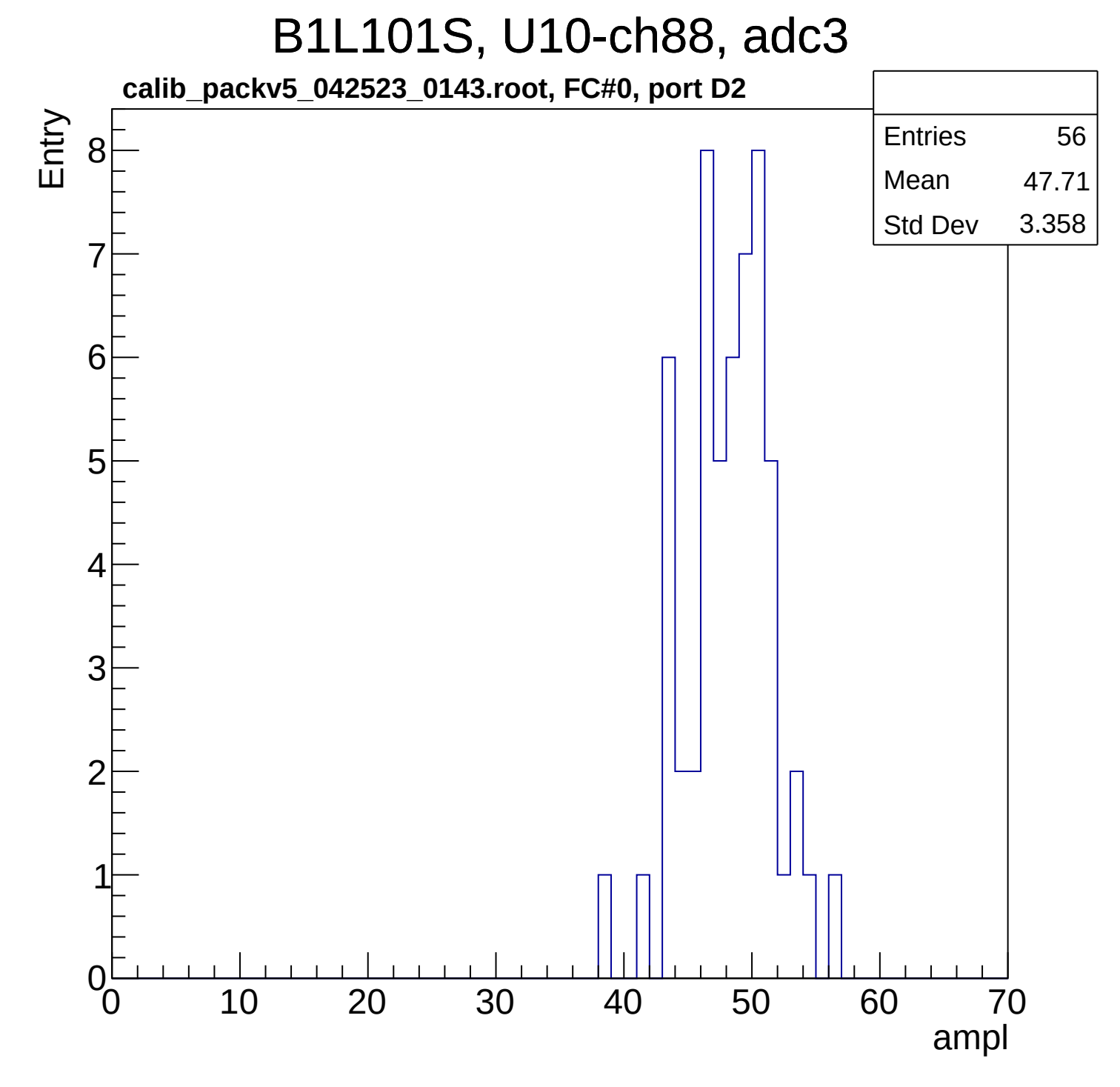

B1L101S, U10-ch88, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 41.28
Std Dev 3.785
Gaus mean : 41.5457
Gaus Width: 4.2033
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch88, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 47.71
Std Dev 3.358
Entry
ampl
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1
2
3
4
5
6
7
8
0
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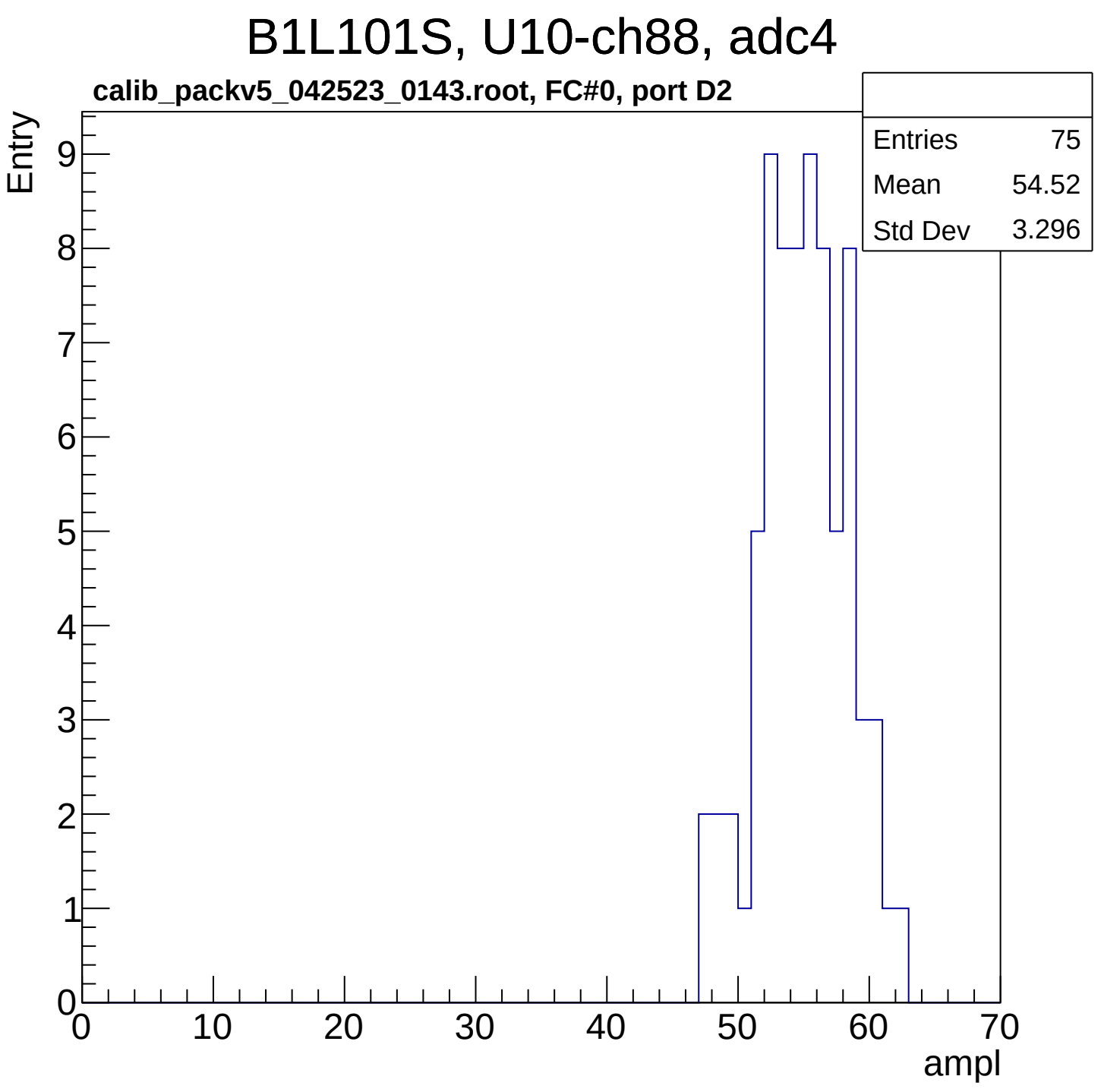
B1L101S, U10-ch88, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 54.52
Std Dev 3.296
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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60
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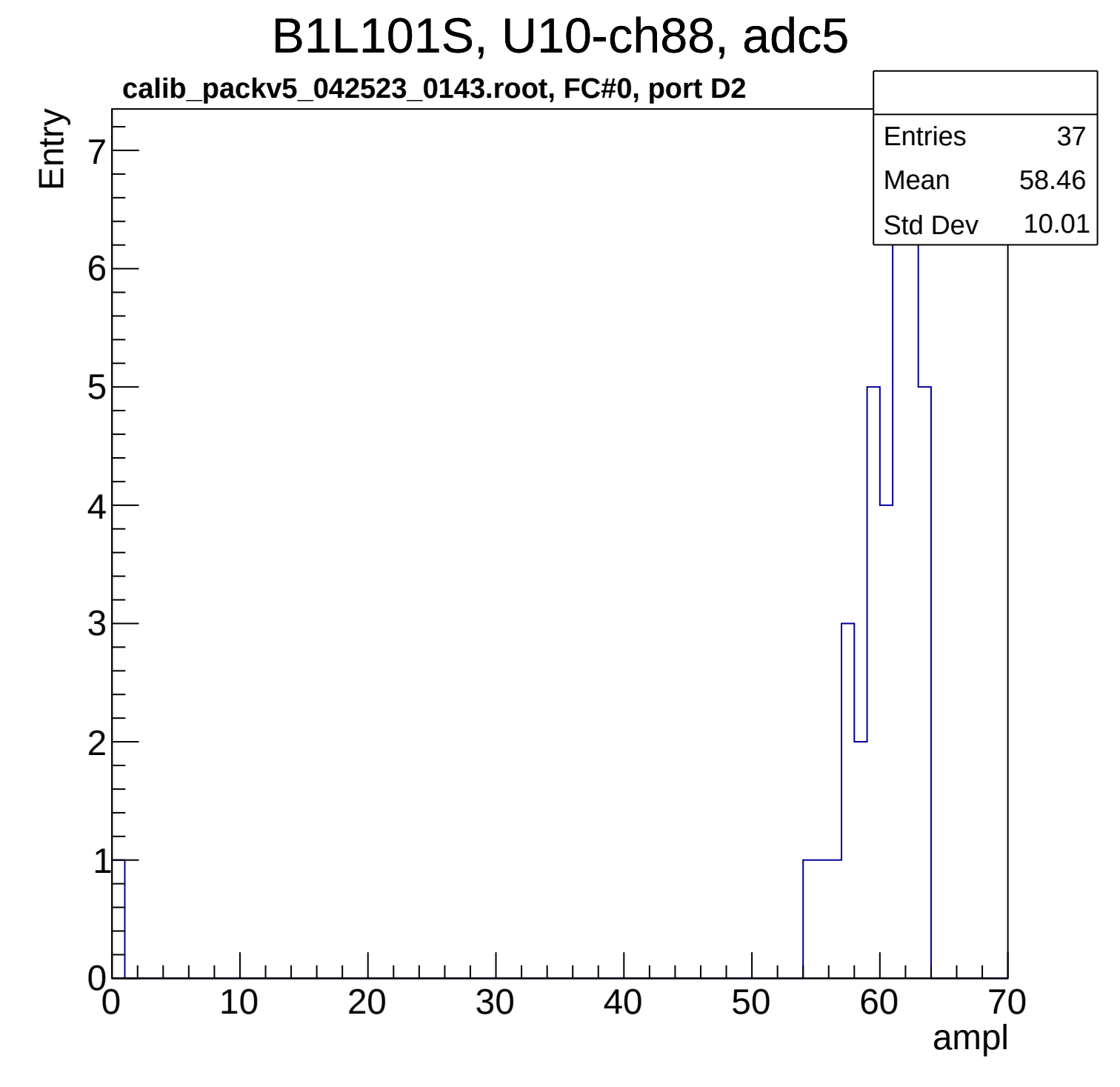
B1L101S, U10-ch88, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 37
Mean 58.46
Std Dev 10.01
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
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60
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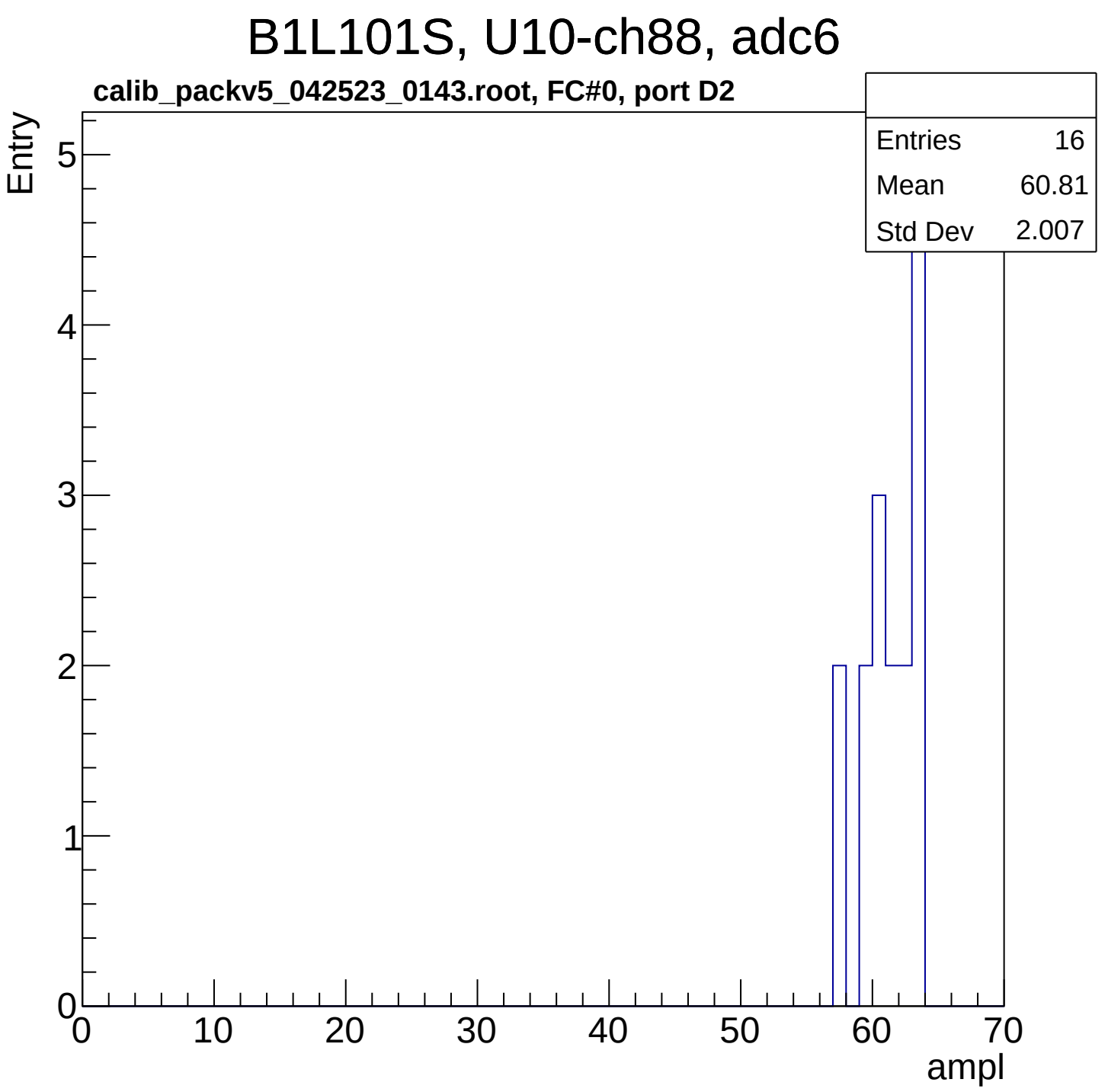
B1L101S, U10-ch88, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 16
Mean 60.81
Std Dev 2.007
Entry
ampl
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1
2
3
4
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0
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40
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60
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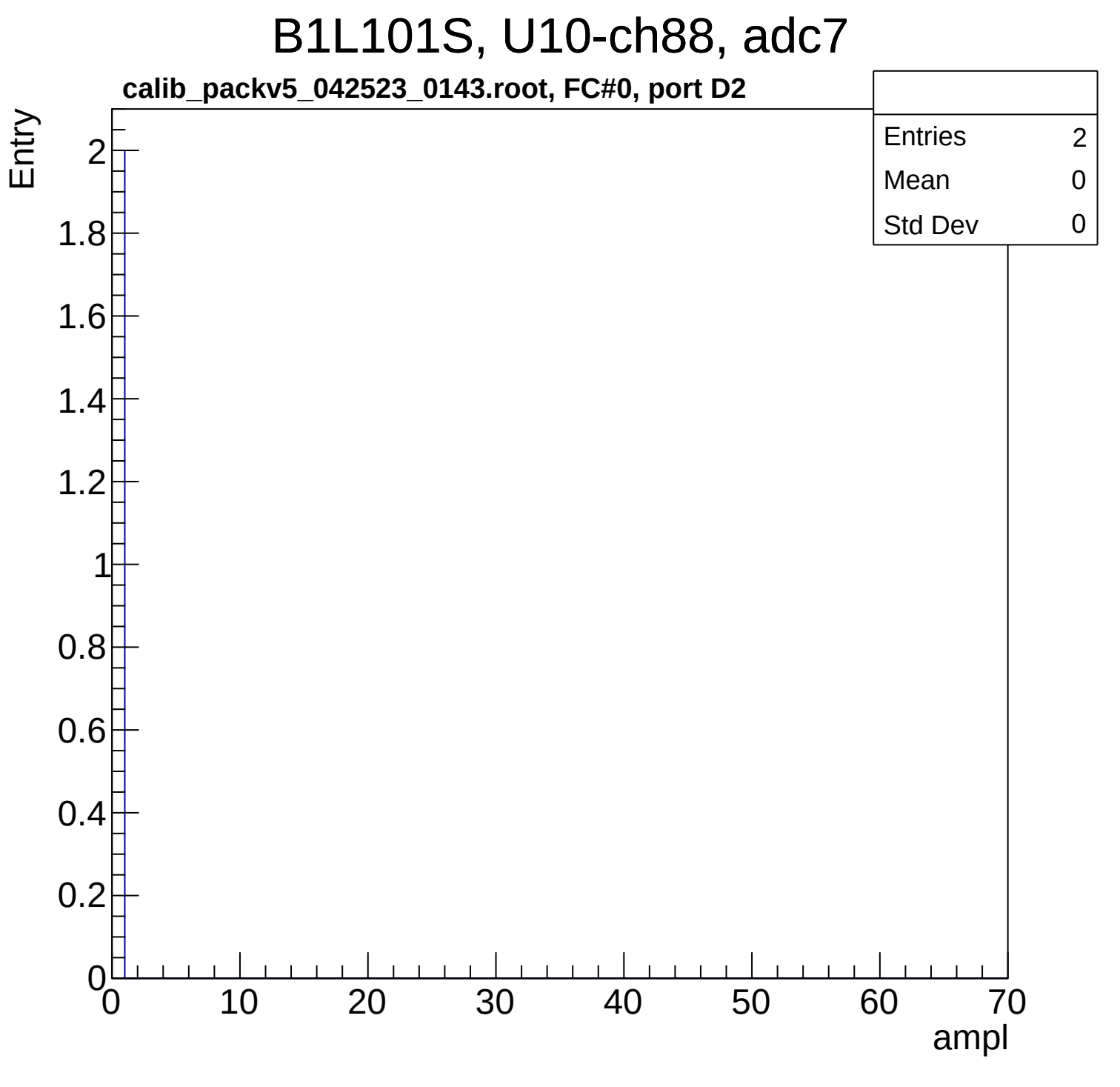
B1L101S, U10-ch88, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
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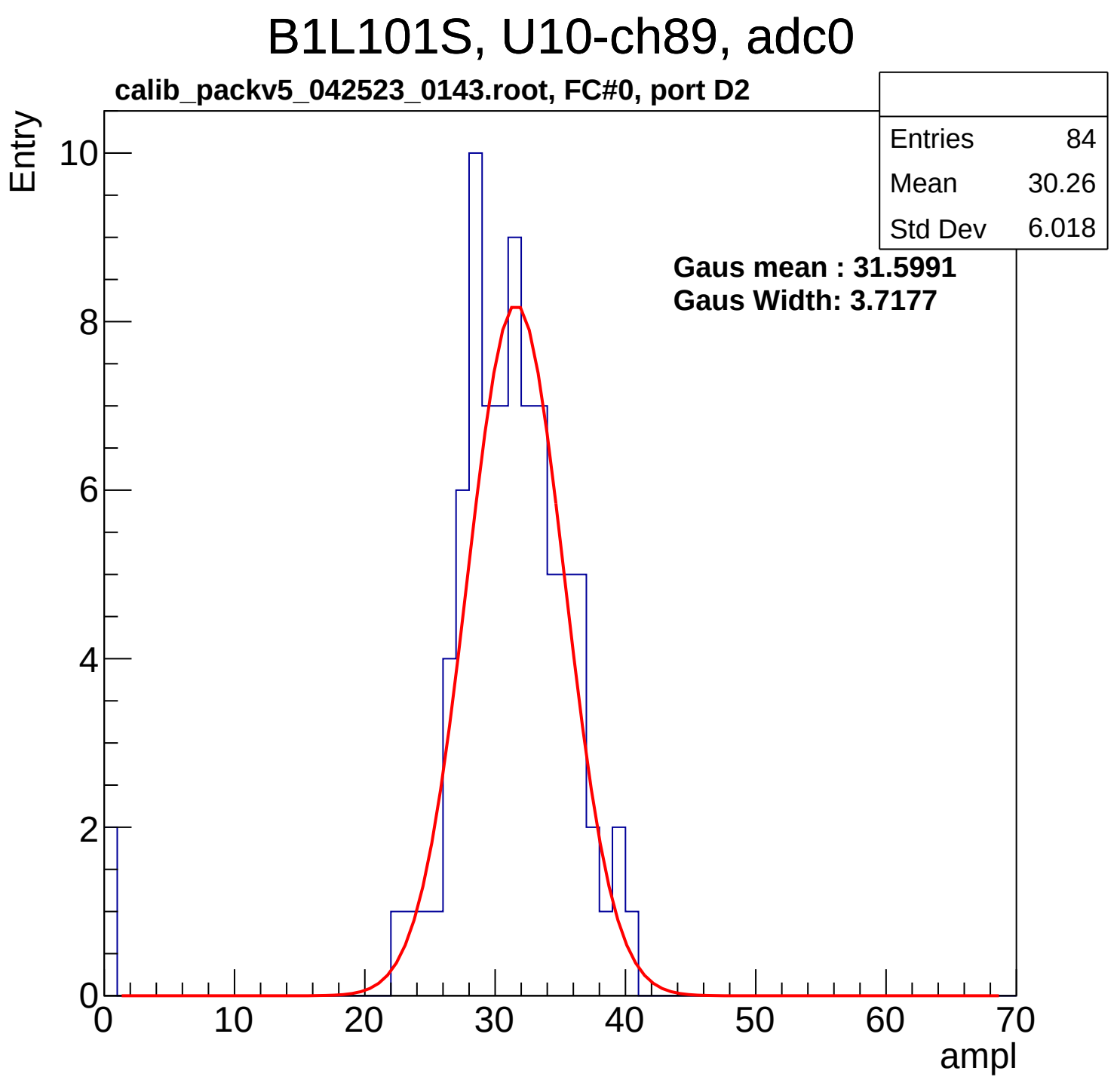
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch89, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 84
Mean 30.26
Std Dev 6.018
Gaus mean : 31.5991
Gaus Width: 3.7177
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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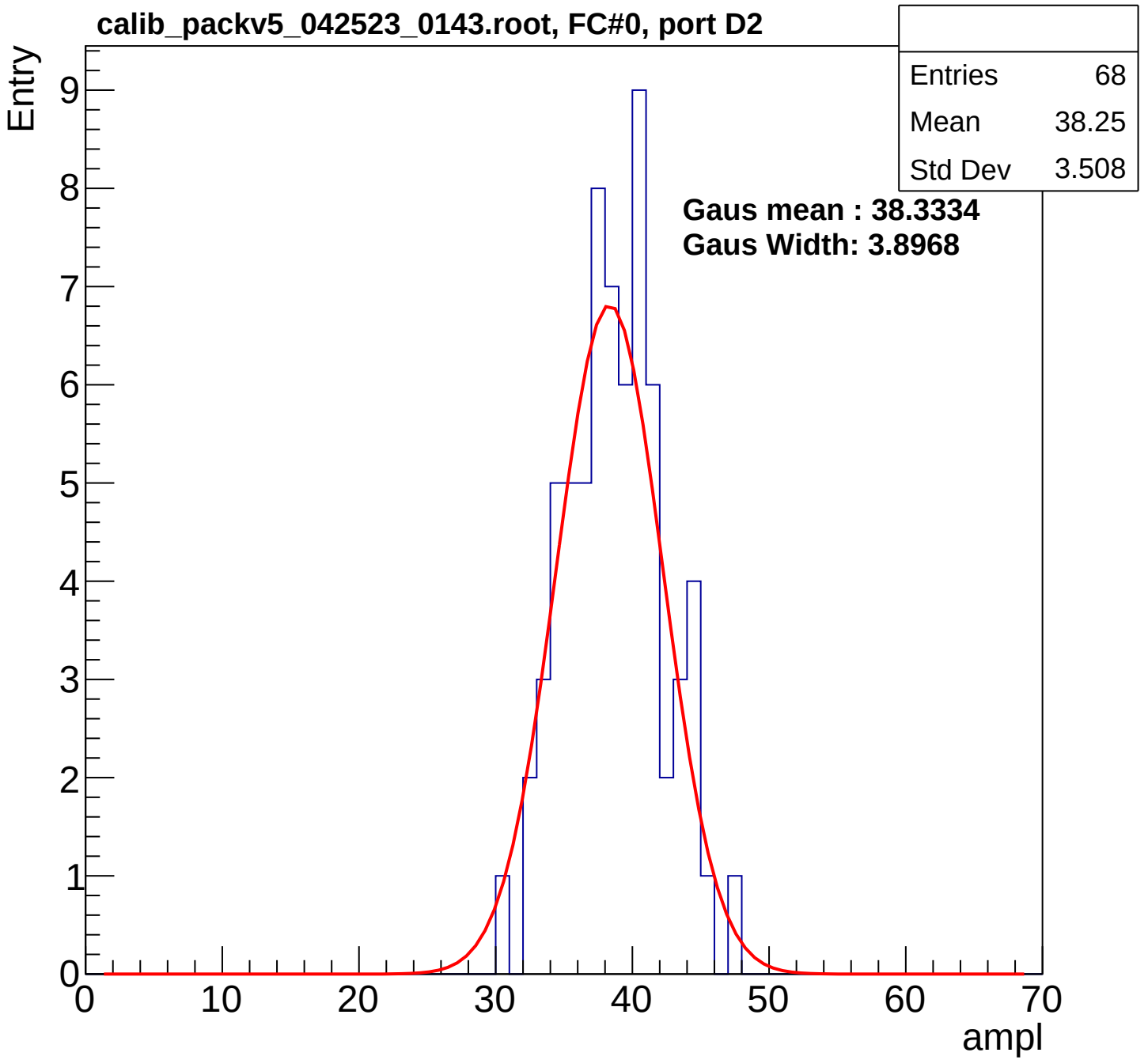
B1L101S, U10-ch89, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 38.25
Std Dev 3.508
Gaus mean : 38.3334
Gaus Width: 3.8968
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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40
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60
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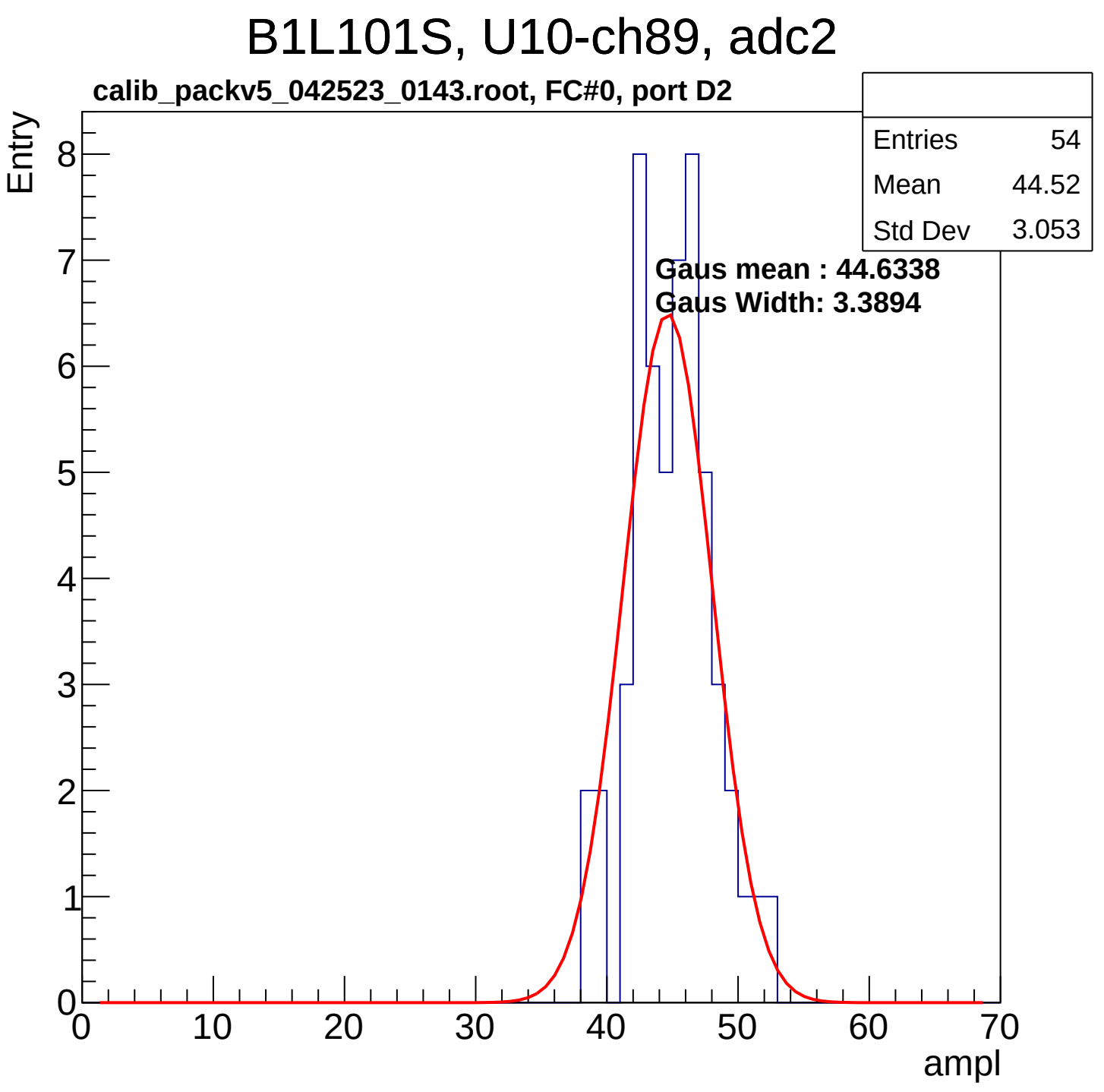
B1L101S, U10-ch89, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 44.52
Std Dev 3.053
Gaus mean : 44.6338
Gaus Width: 3.3894
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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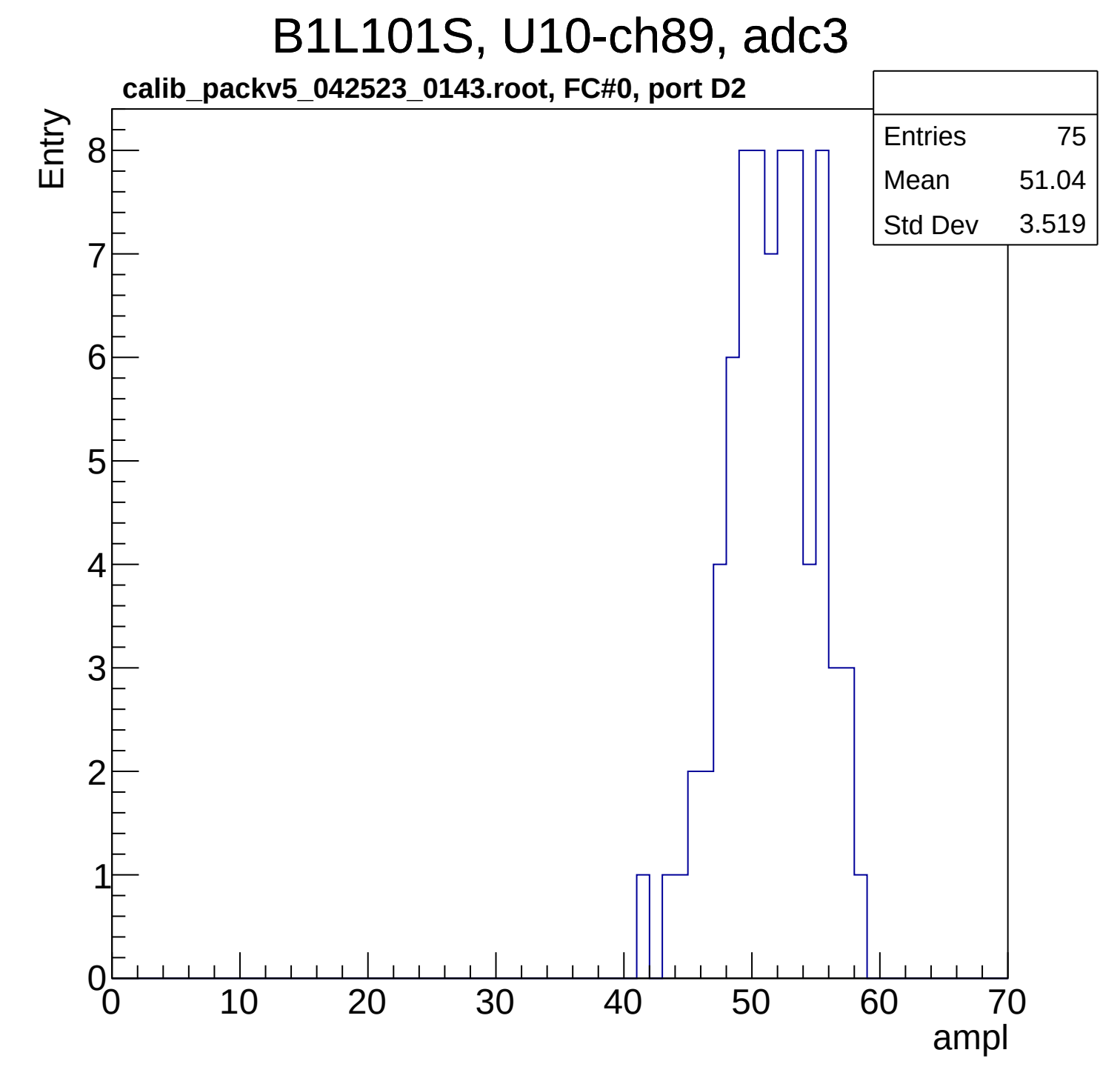
B1L101S, U10-ch89, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 51.04
Std Dev 3.519
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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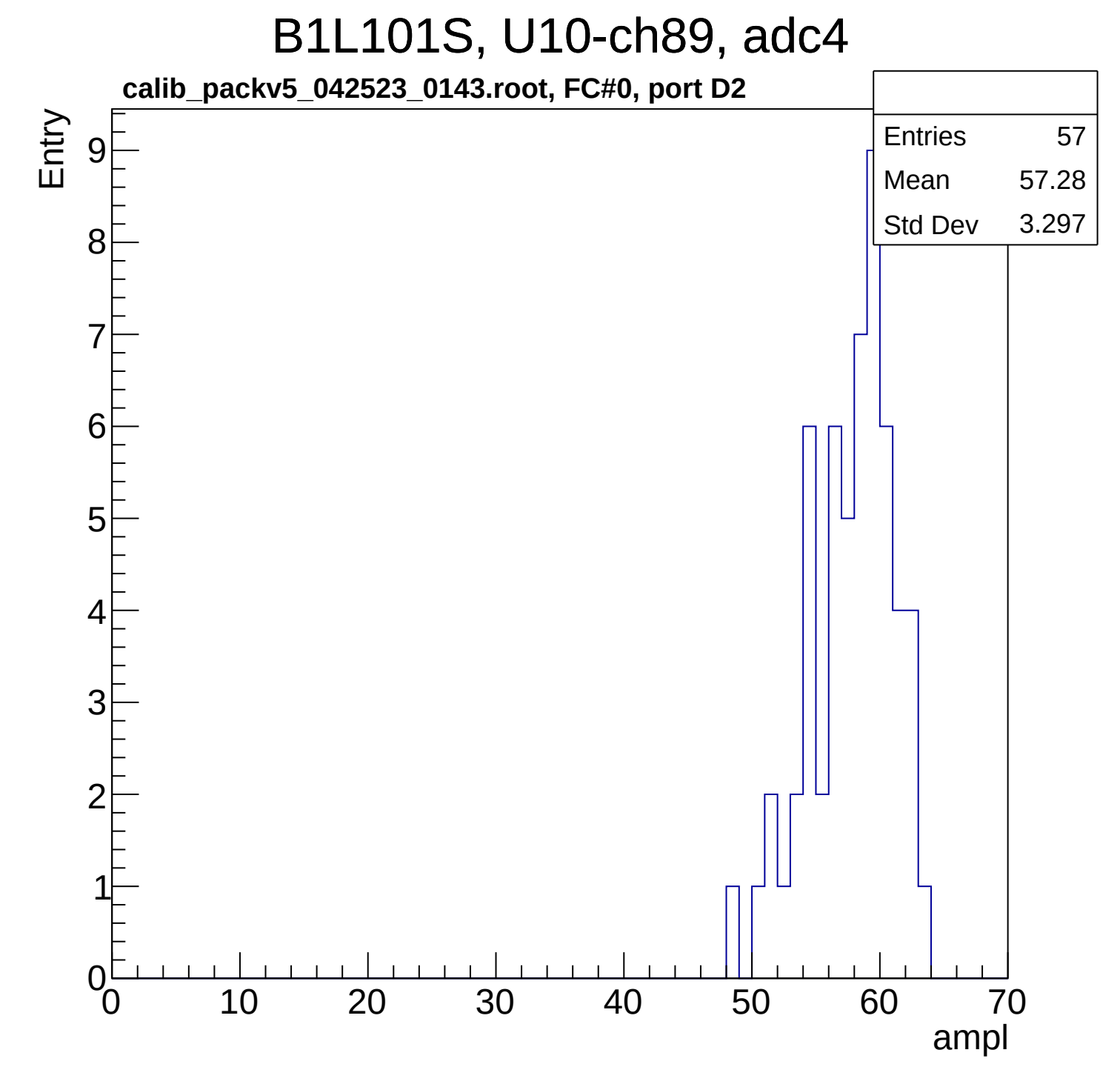
B1L101S, U10-ch89, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 57.28
Std Dev 3.297
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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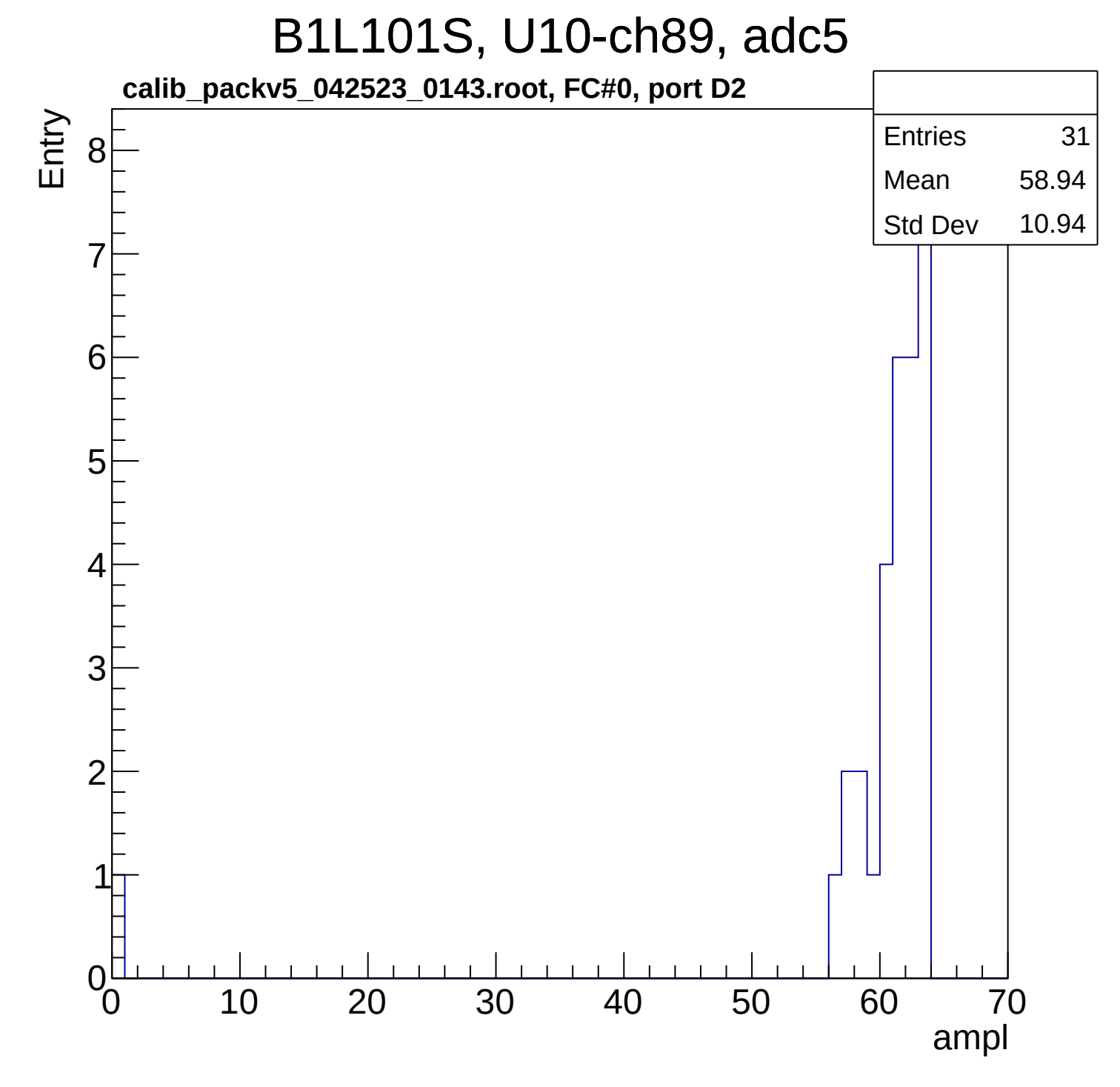
B1L101S, U10-ch89, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 31
Mean 58.94
Std Dev 10.94
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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60
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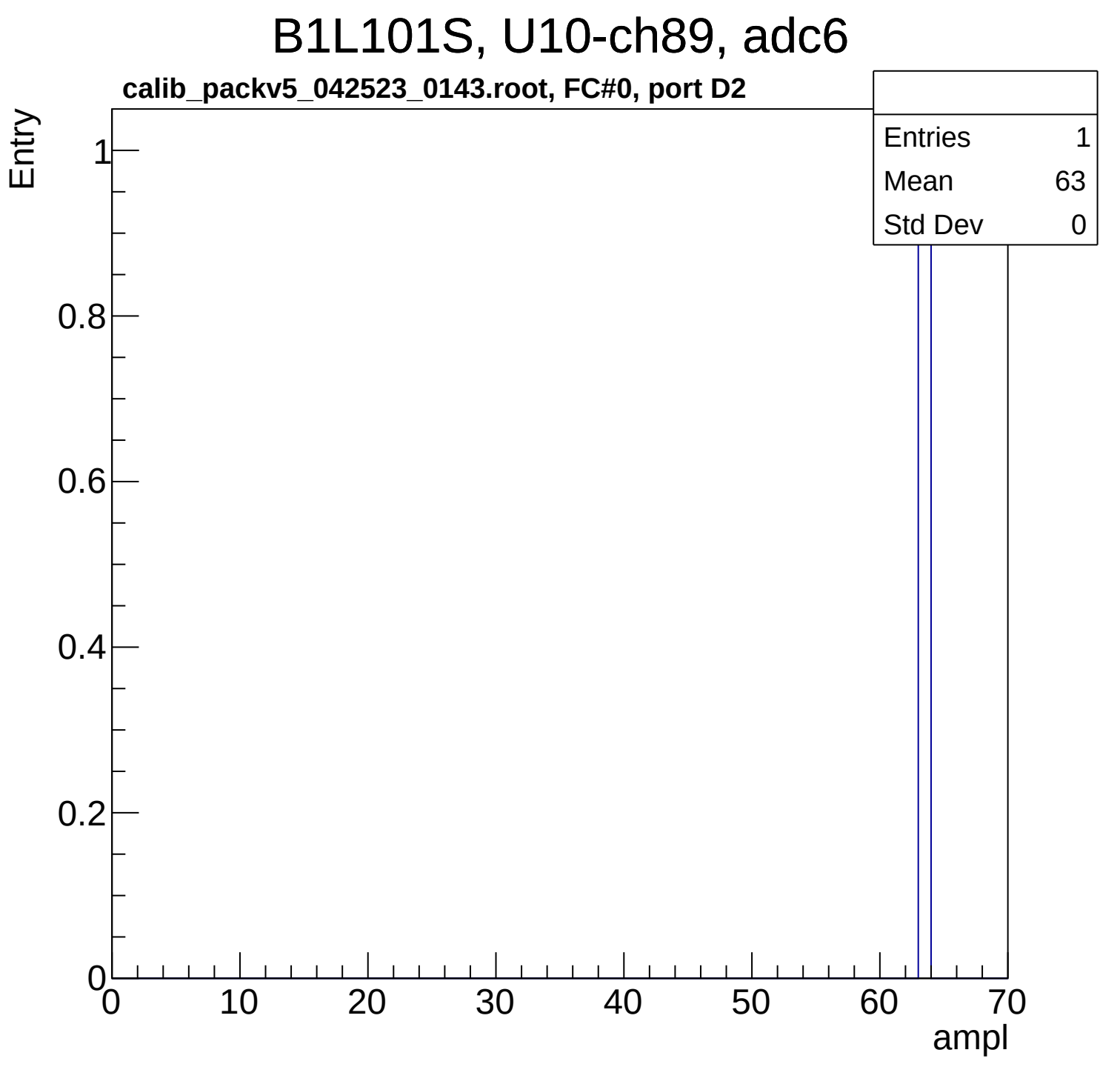
B1L101S, U10-ch89, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 63
Std Dev 0
Entry
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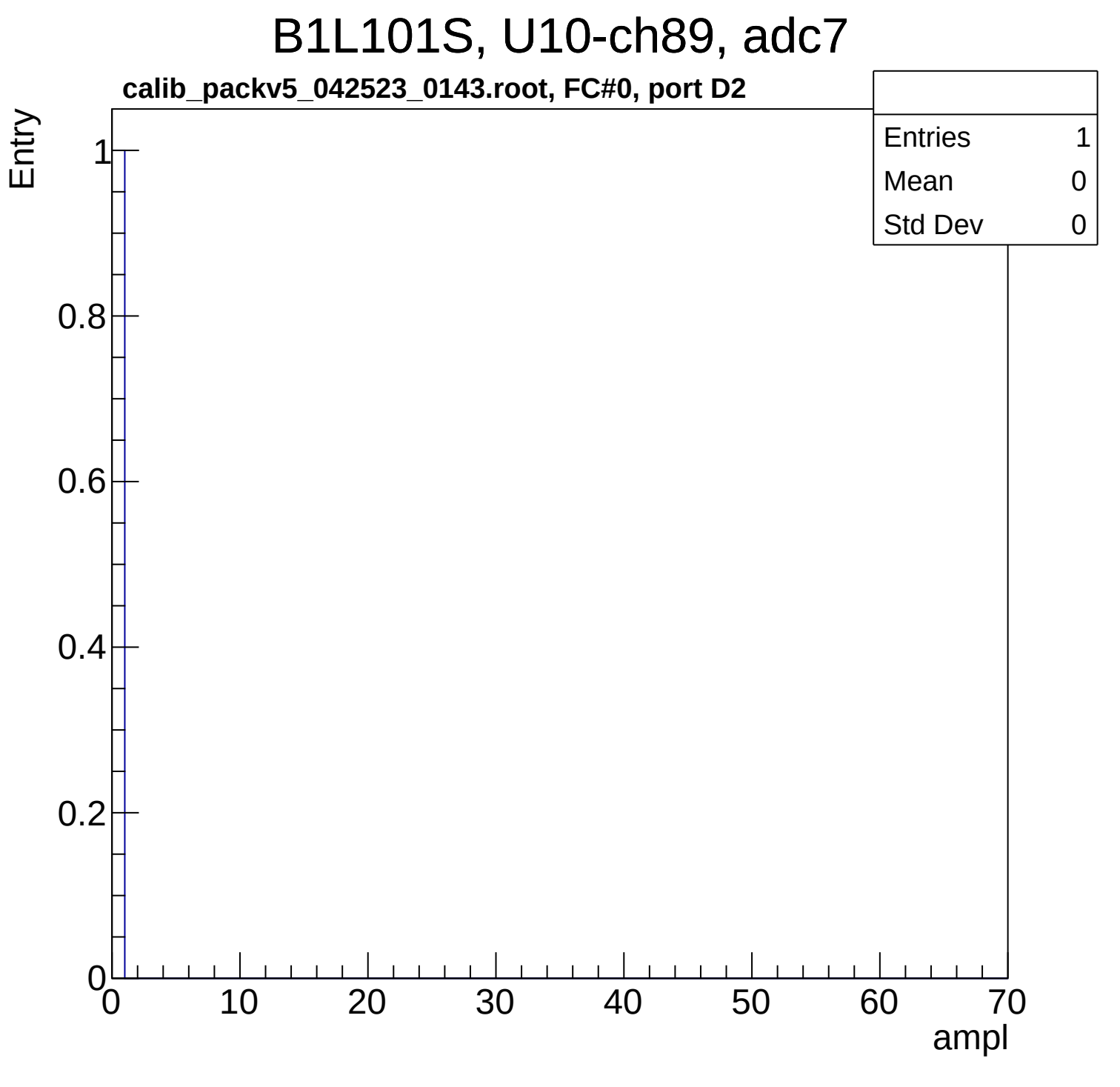
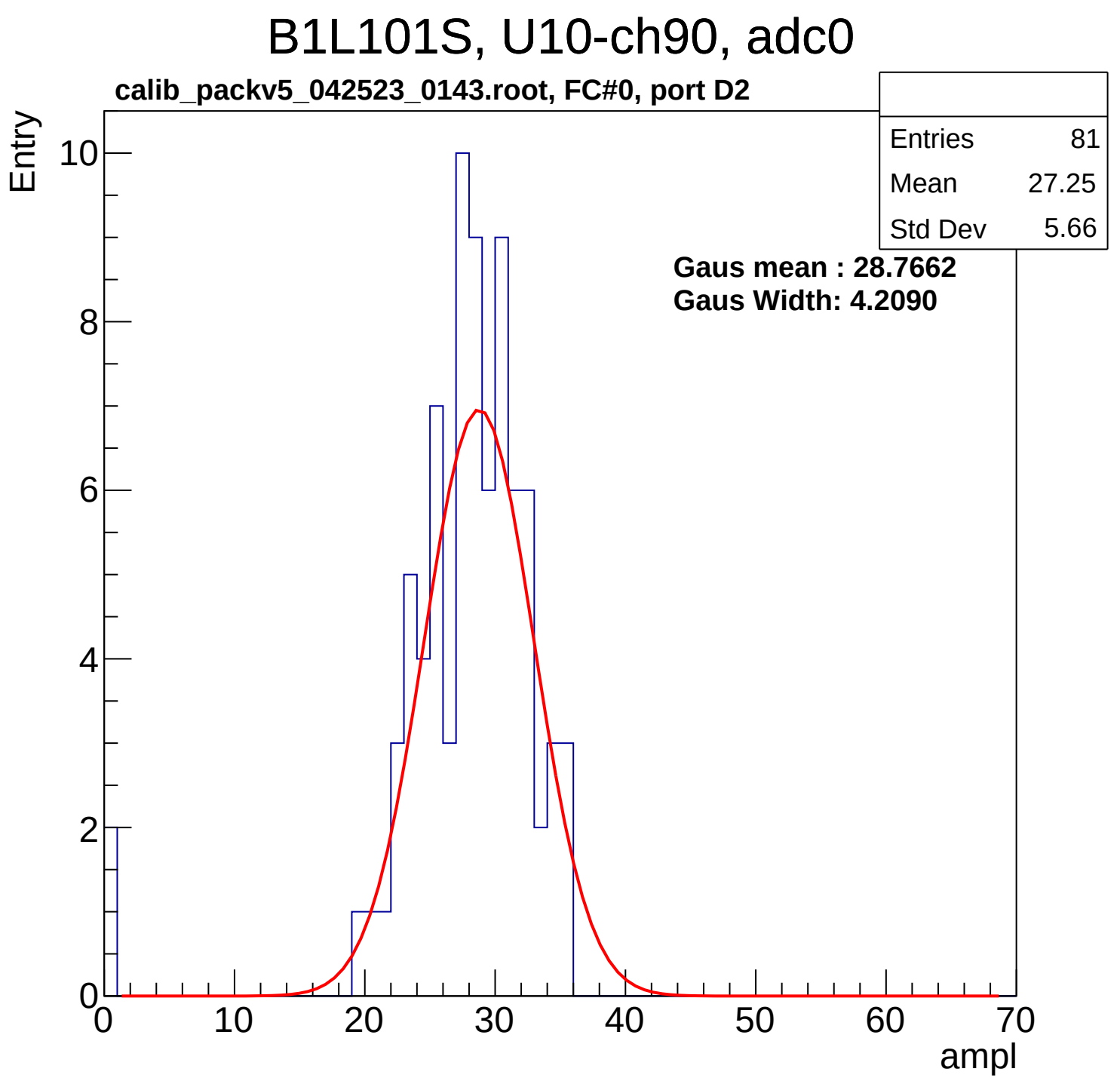
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch89, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch90, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 81
Mean 27.25
Std Dev 5.66
Gaus mean : 28.7662
Gaus Width: 4.2090
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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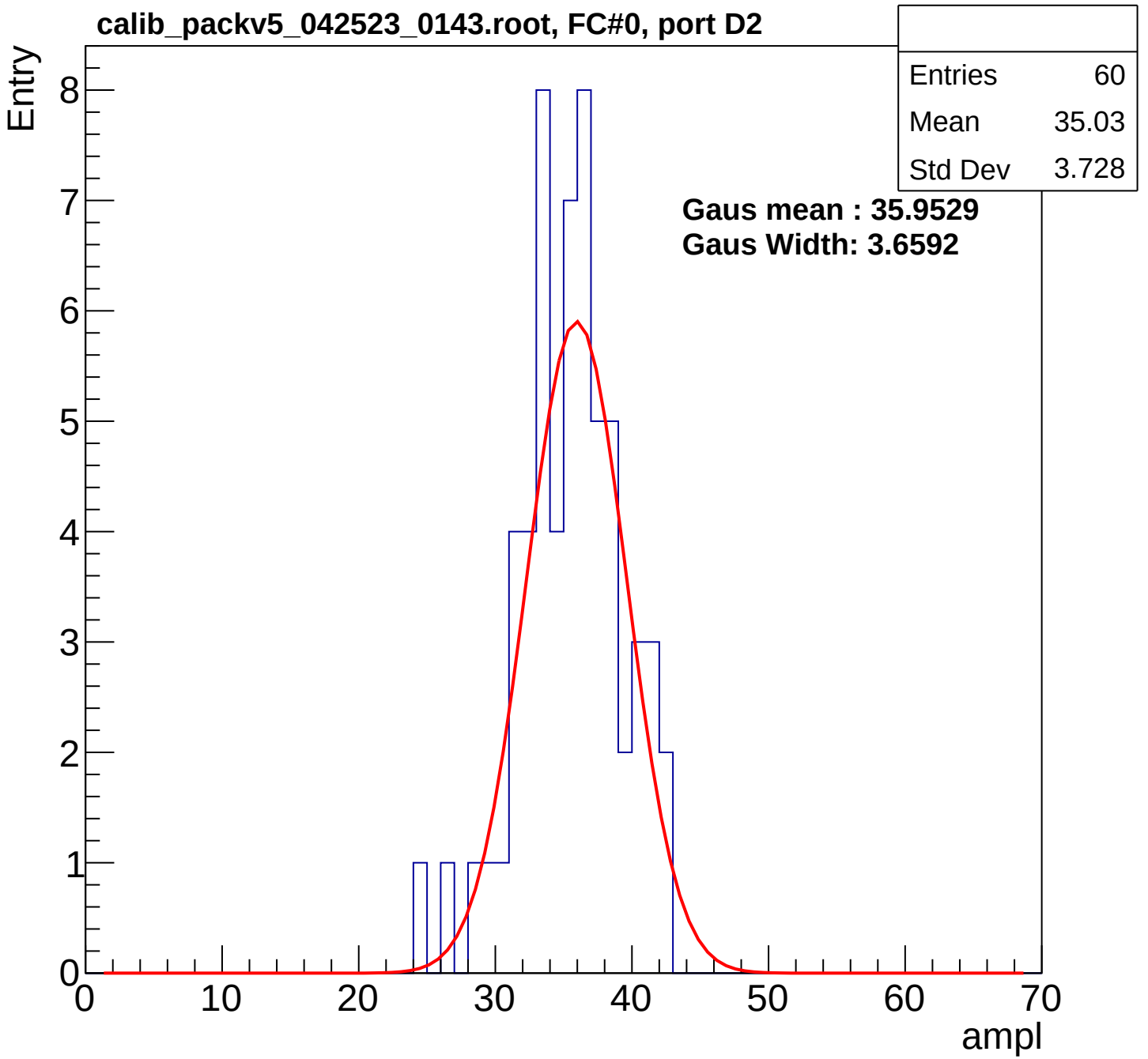
B1L101S, U10-ch90, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 35.03
Std Dev 3.728
Gaus mean : 35.9529
Gaus Width: 3.6592
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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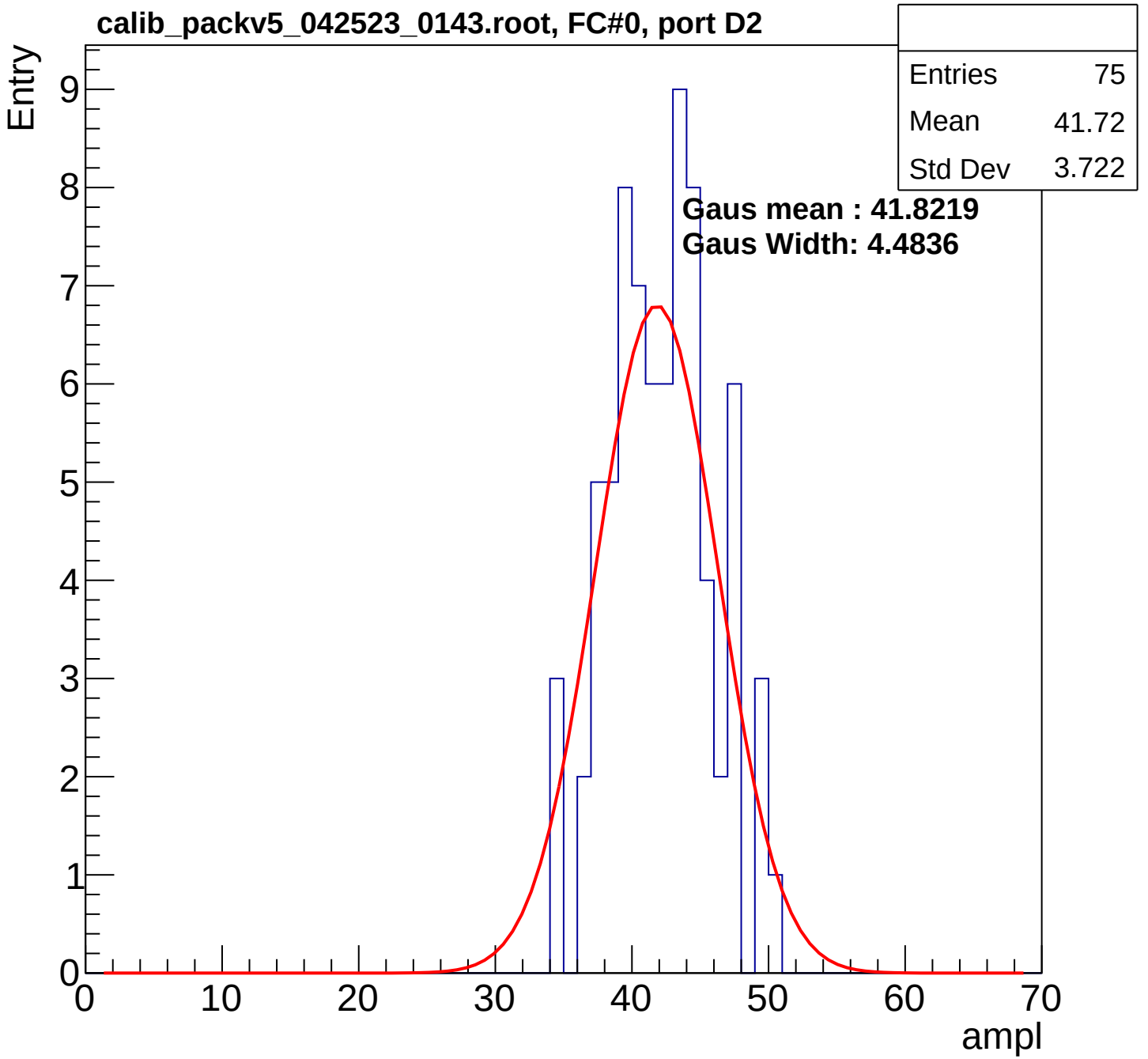
B1L101S, U10-ch90, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 41.72
Std Dev 3.722
Gaus mean : 41.8219
Gaus Width: 4.4836
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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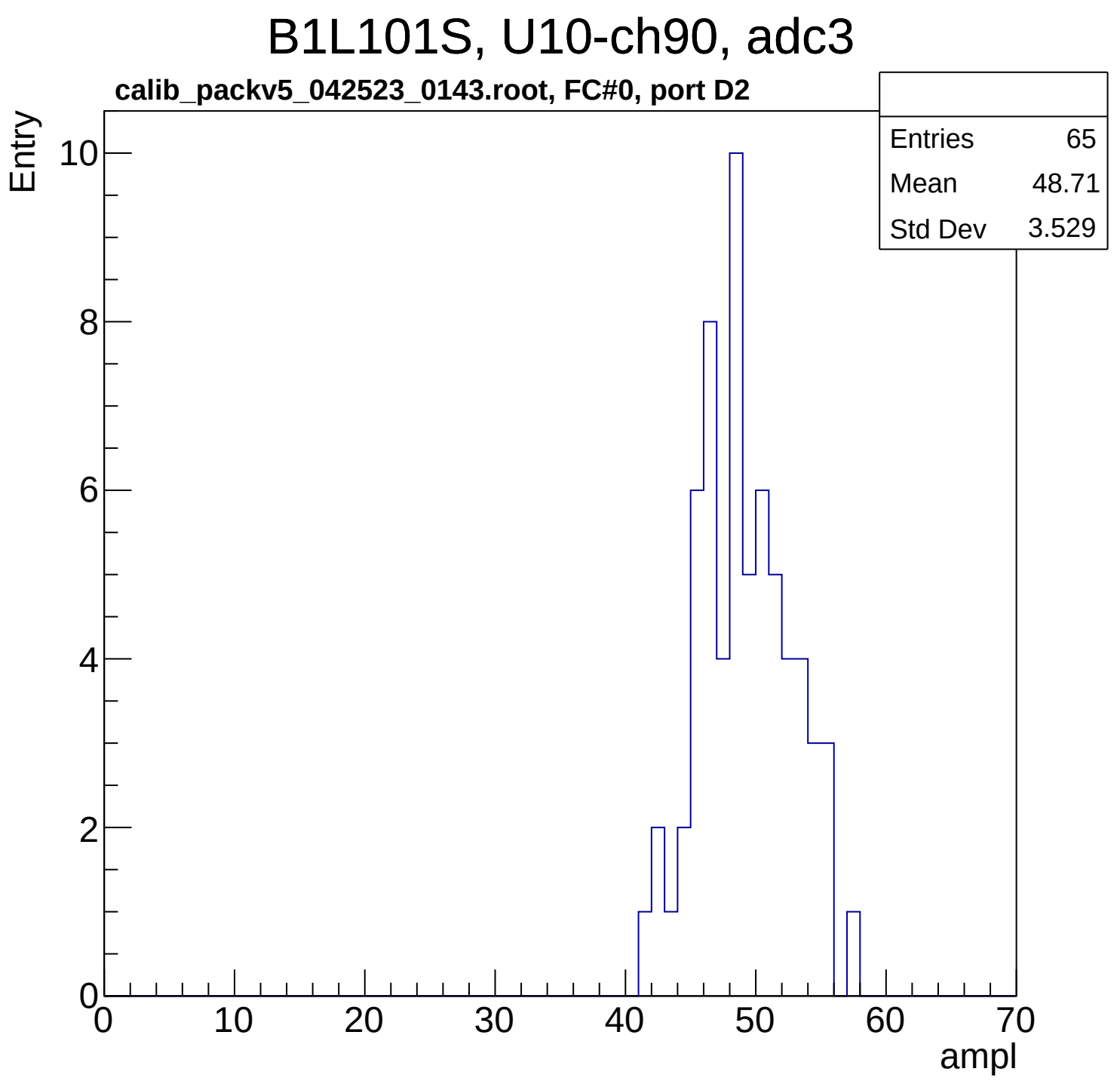
B1L101S, U10-ch90, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 48.71
Std Dev 3.529
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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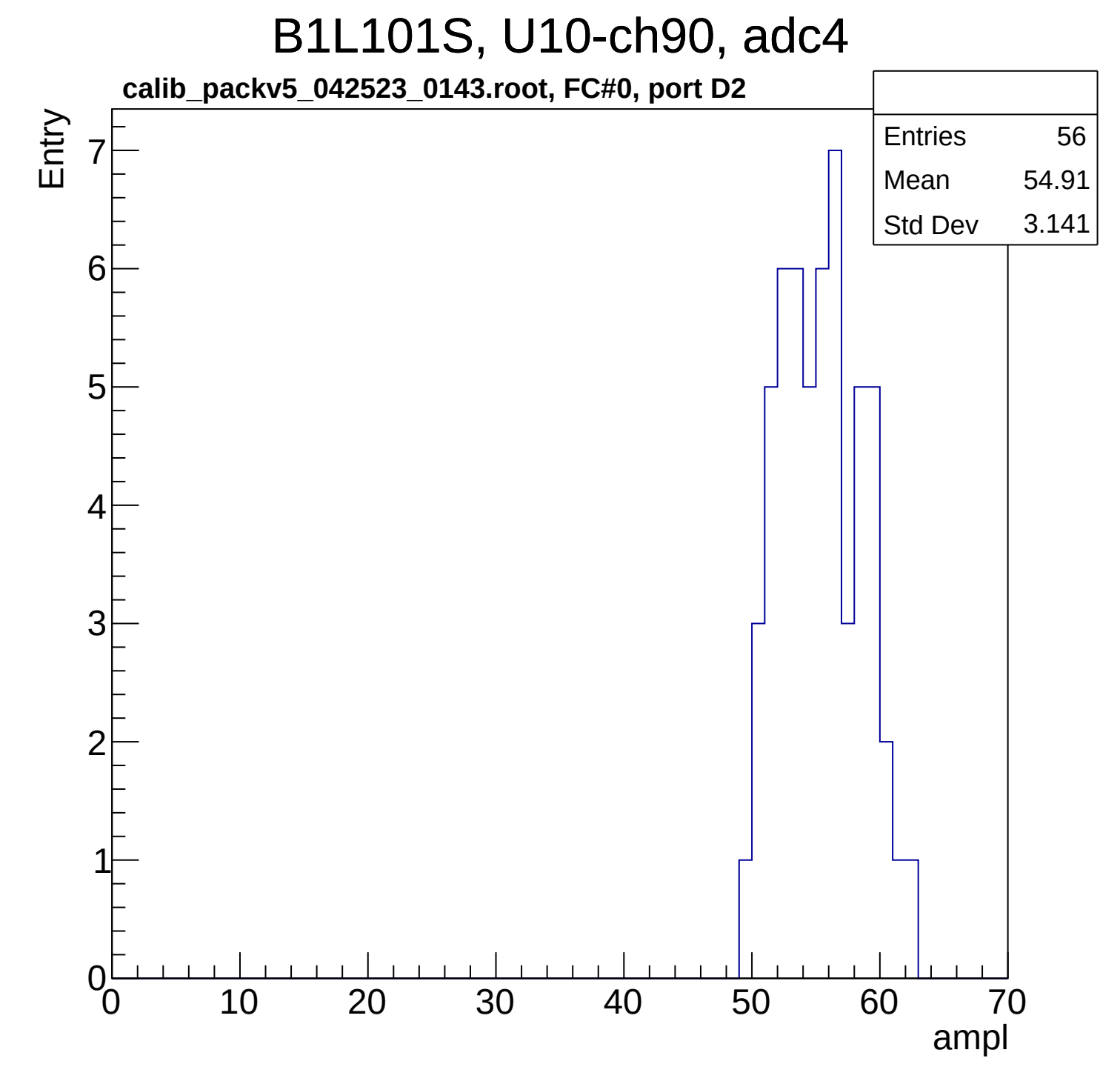
B1L101S, U10-ch90, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 54.91
Std Dev 3.141
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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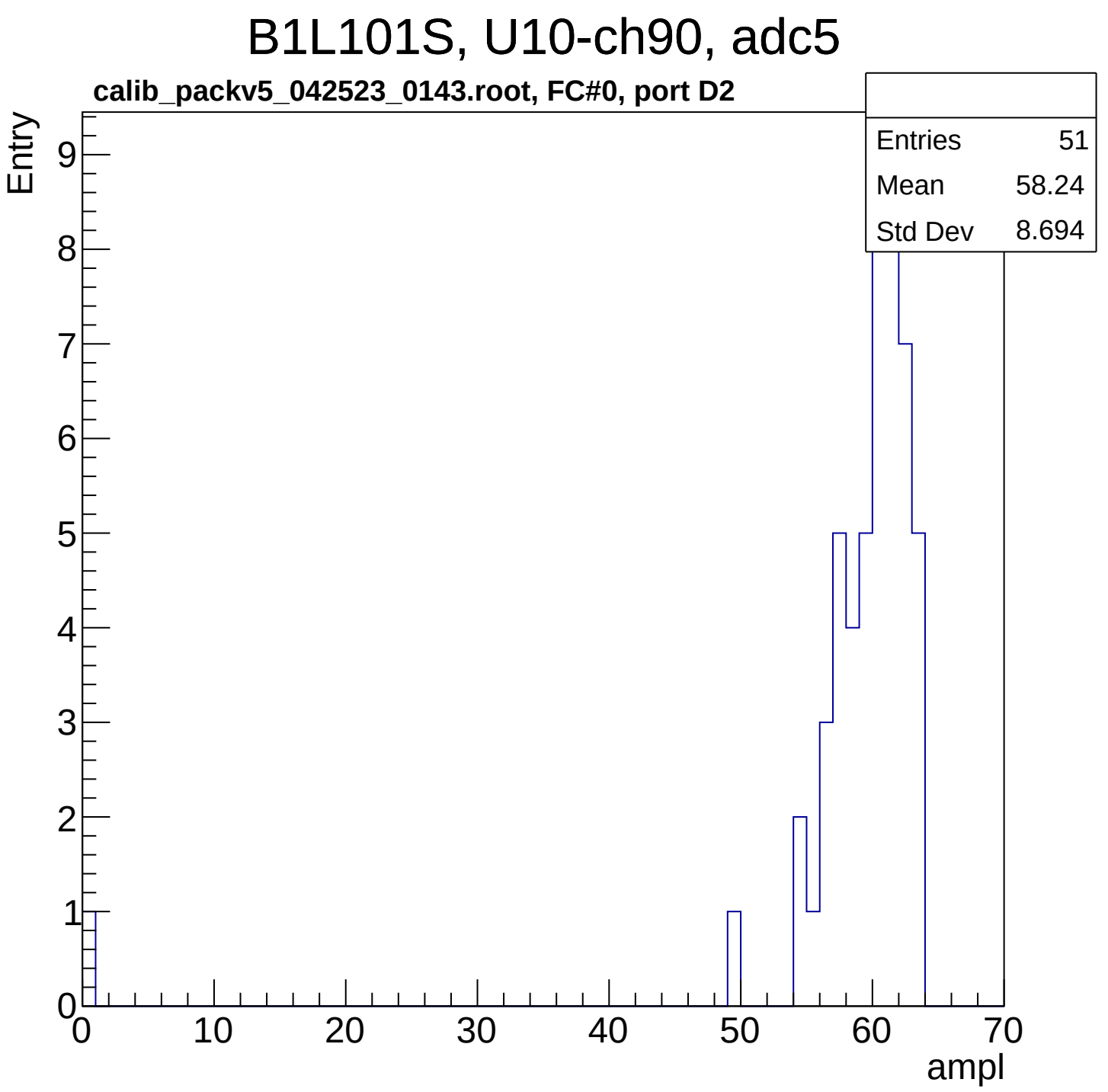
40
50
60
70


B1L101S, U10-ch90, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 58.24
Std Dev 8.694
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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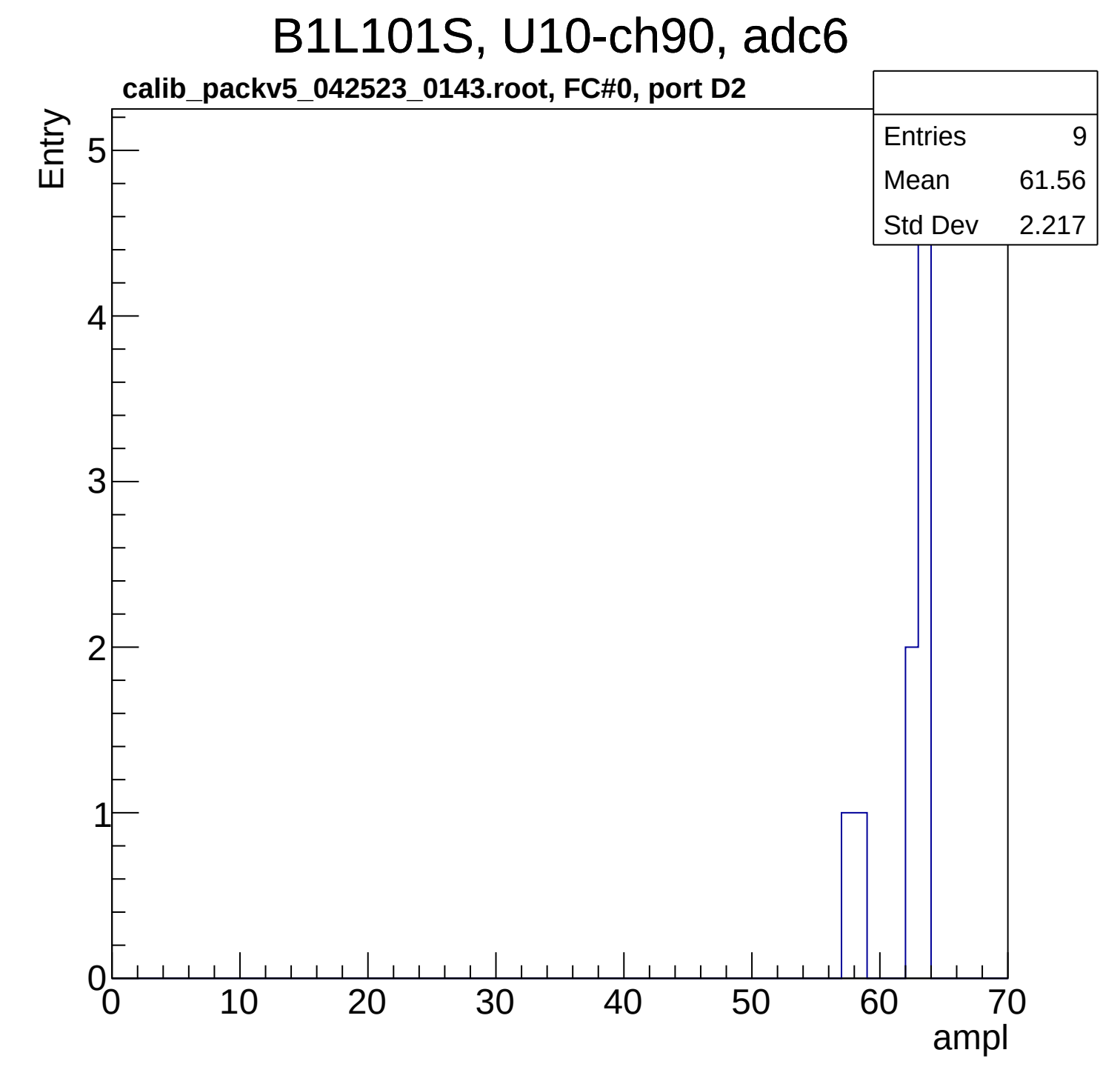
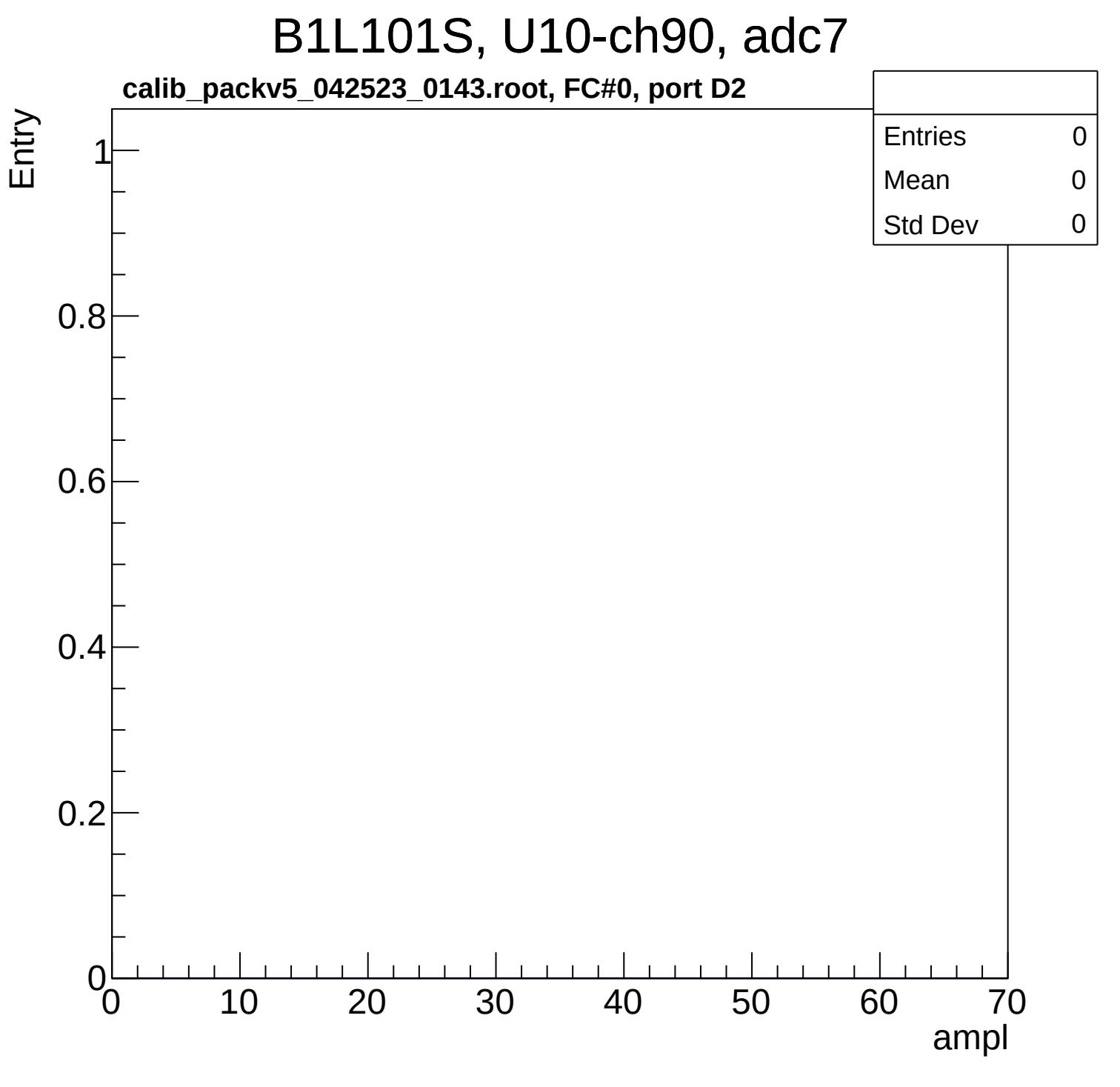

B1L101S, U10-ch90, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 61.56
Std Dev 2.217
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L101S, U10-ch90, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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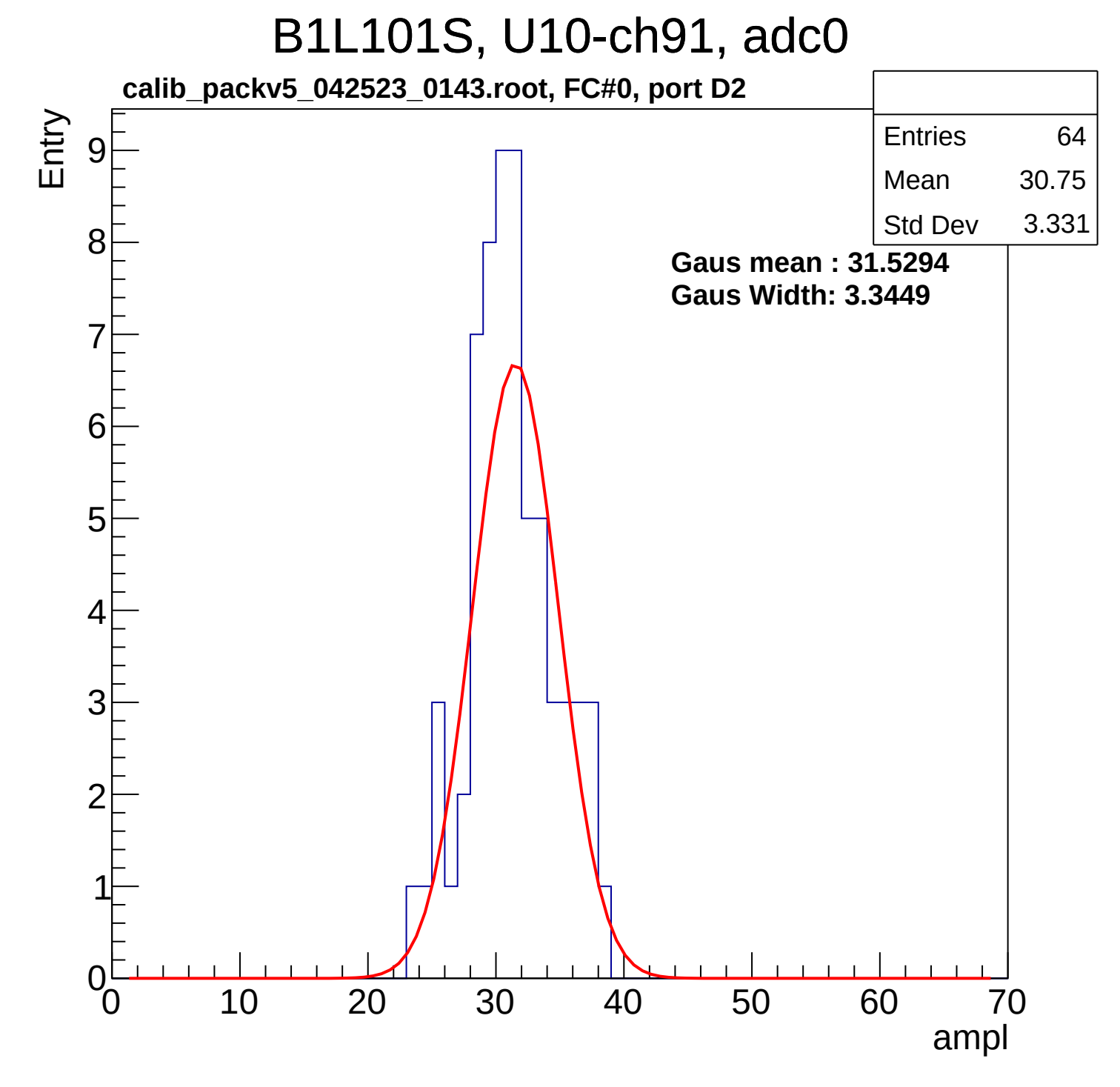
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch91, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 30.75
Std Dev 3.331
Gaus mean : 31.5294
Gaus Width: 3.3449
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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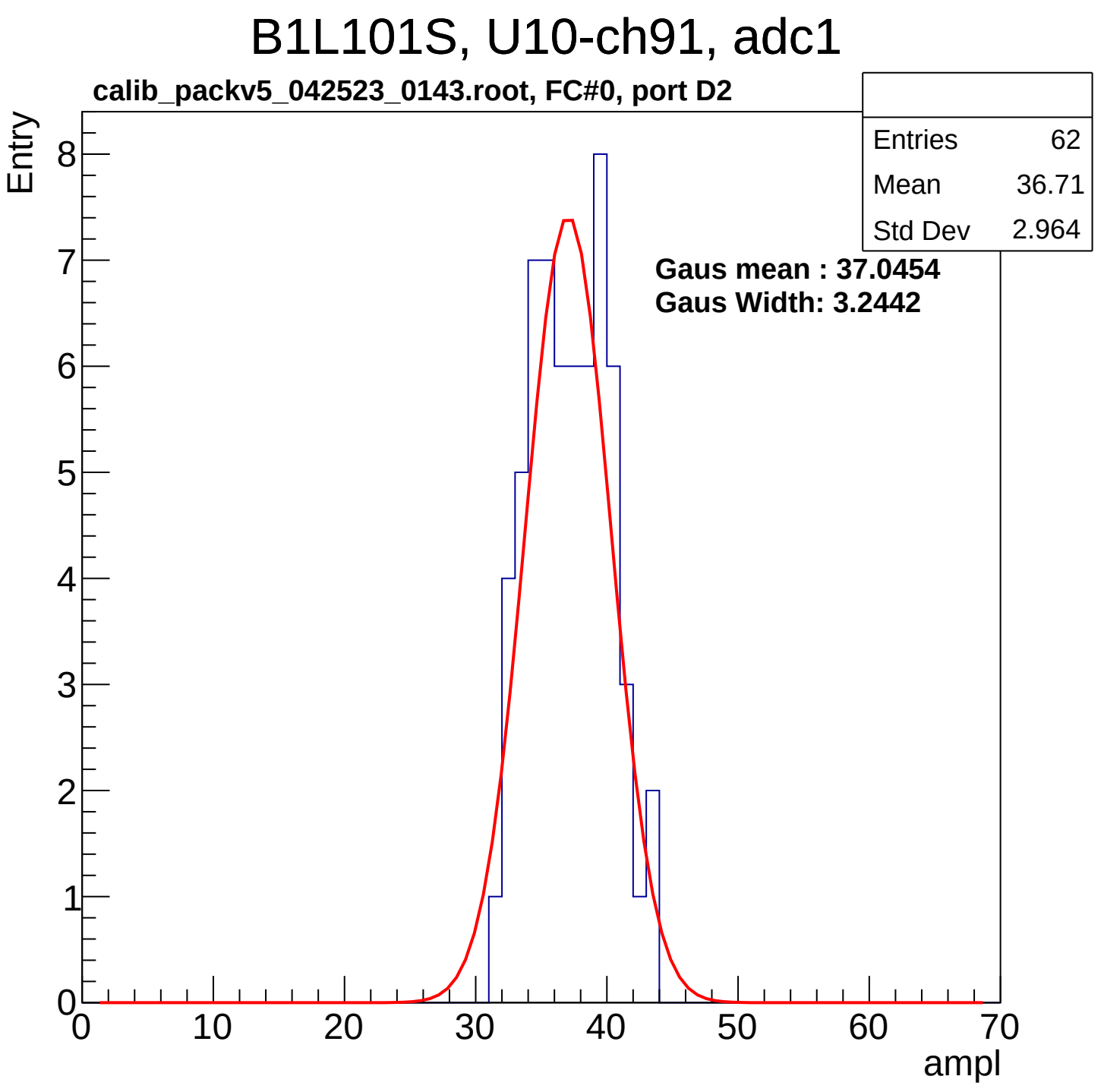
B1L101S, U10-ch91, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 36.71
Std Dev 2.964
Gaus mean : 37.0454
Gaus Width: 3.2442
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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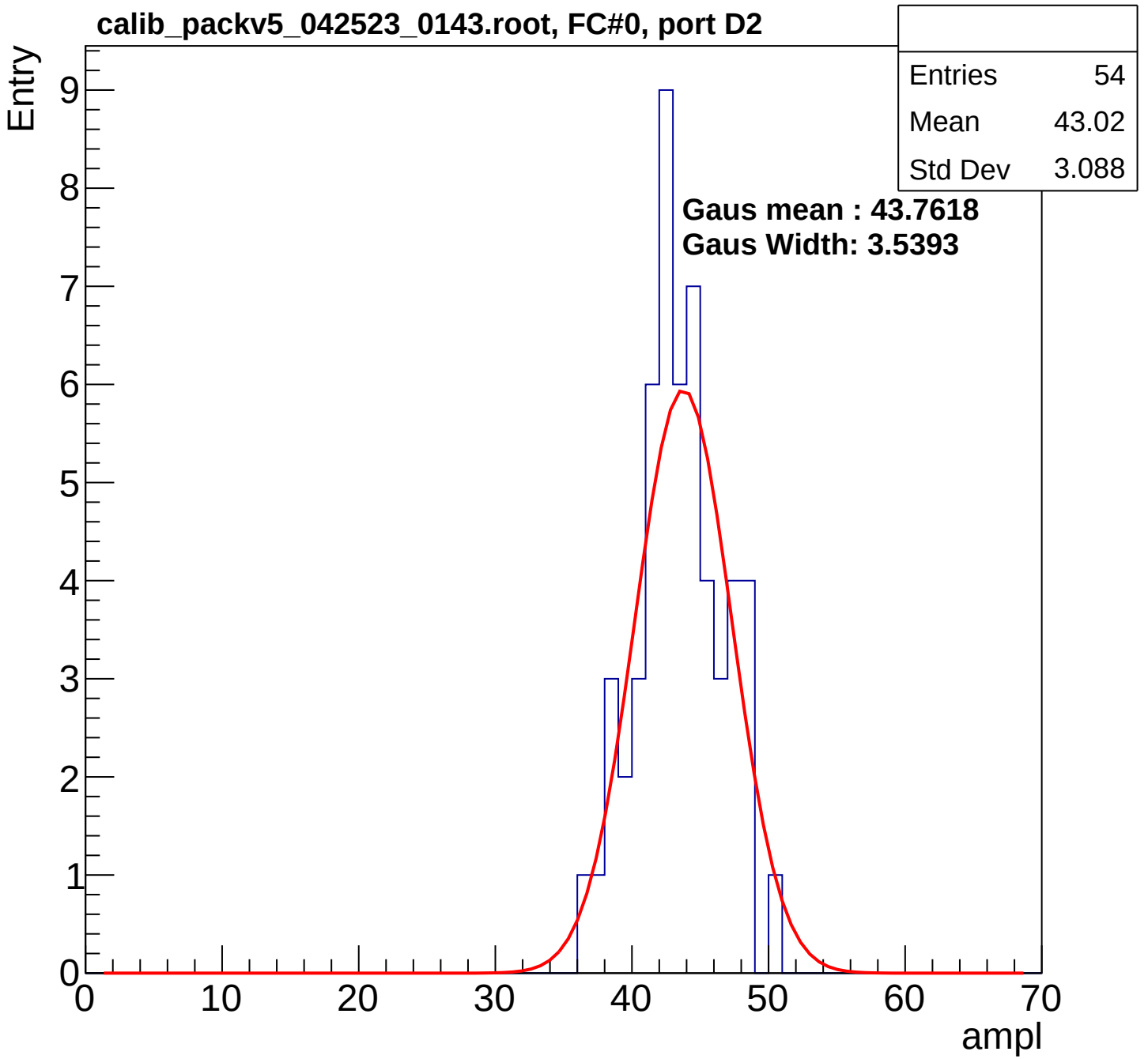
B1L101S, U10-ch91, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 43.02
Std Dev 3.088
Gaus mean : 43.7618
Gaus Width: 3.5393
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
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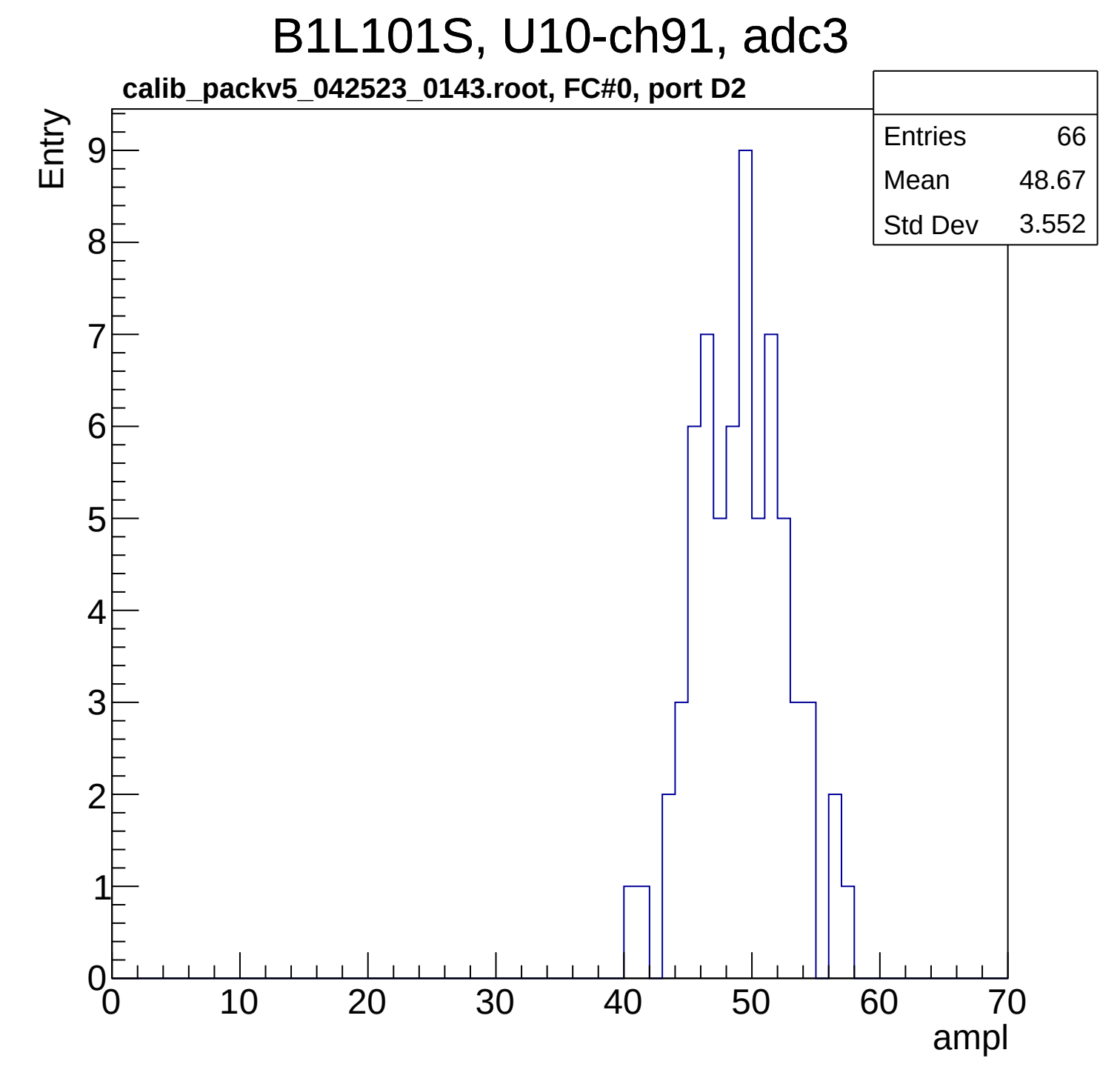
60
70


B1L101S, U10-ch91, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 48.67
Std Dev 3.552
Entry
ampl
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6
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0
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60
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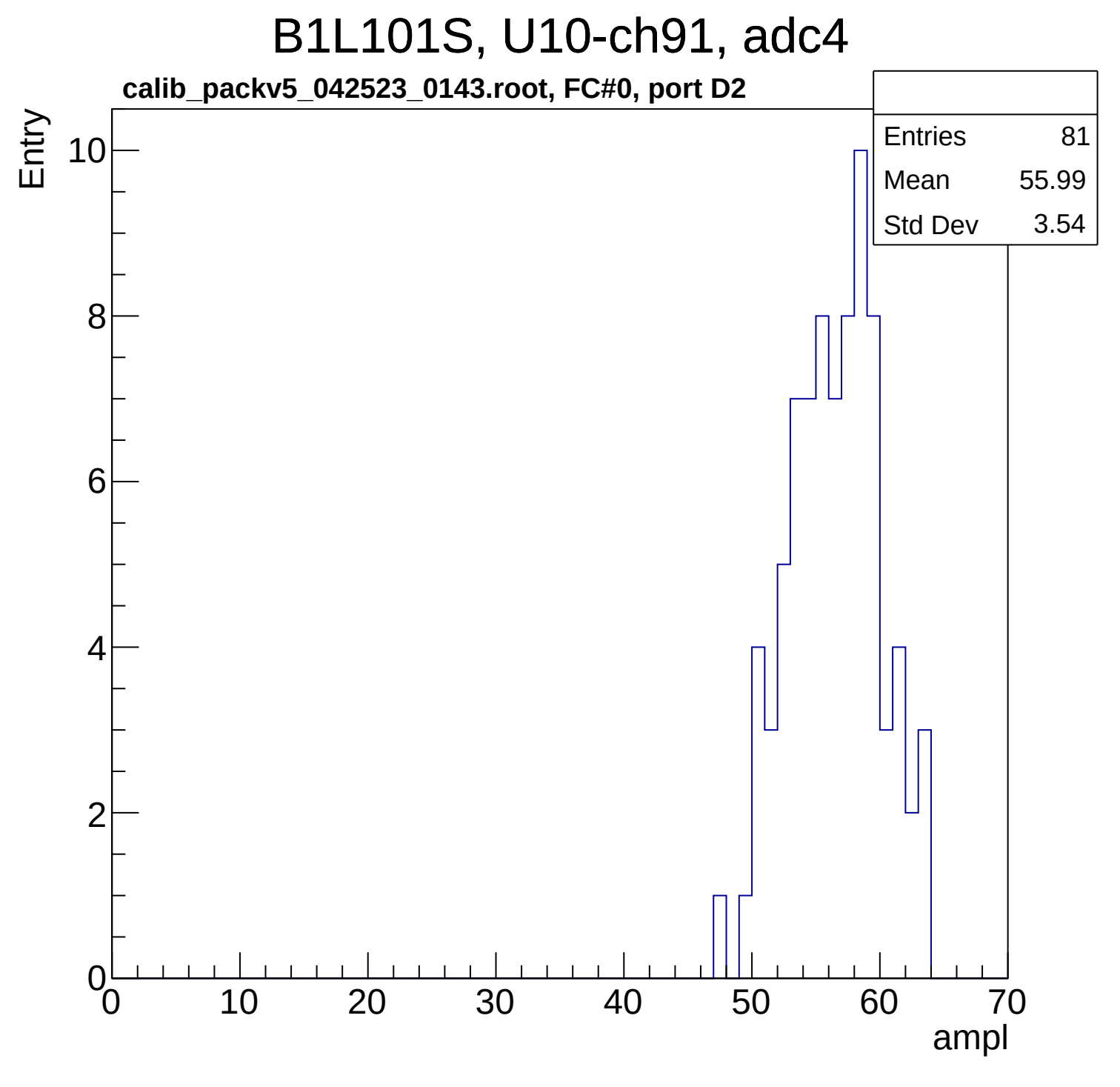
B1L101S, U10-ch91, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 81
Mean 55.99
Std Dev 3.54
Entry
ampl
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4
6
8
10
0
10
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60
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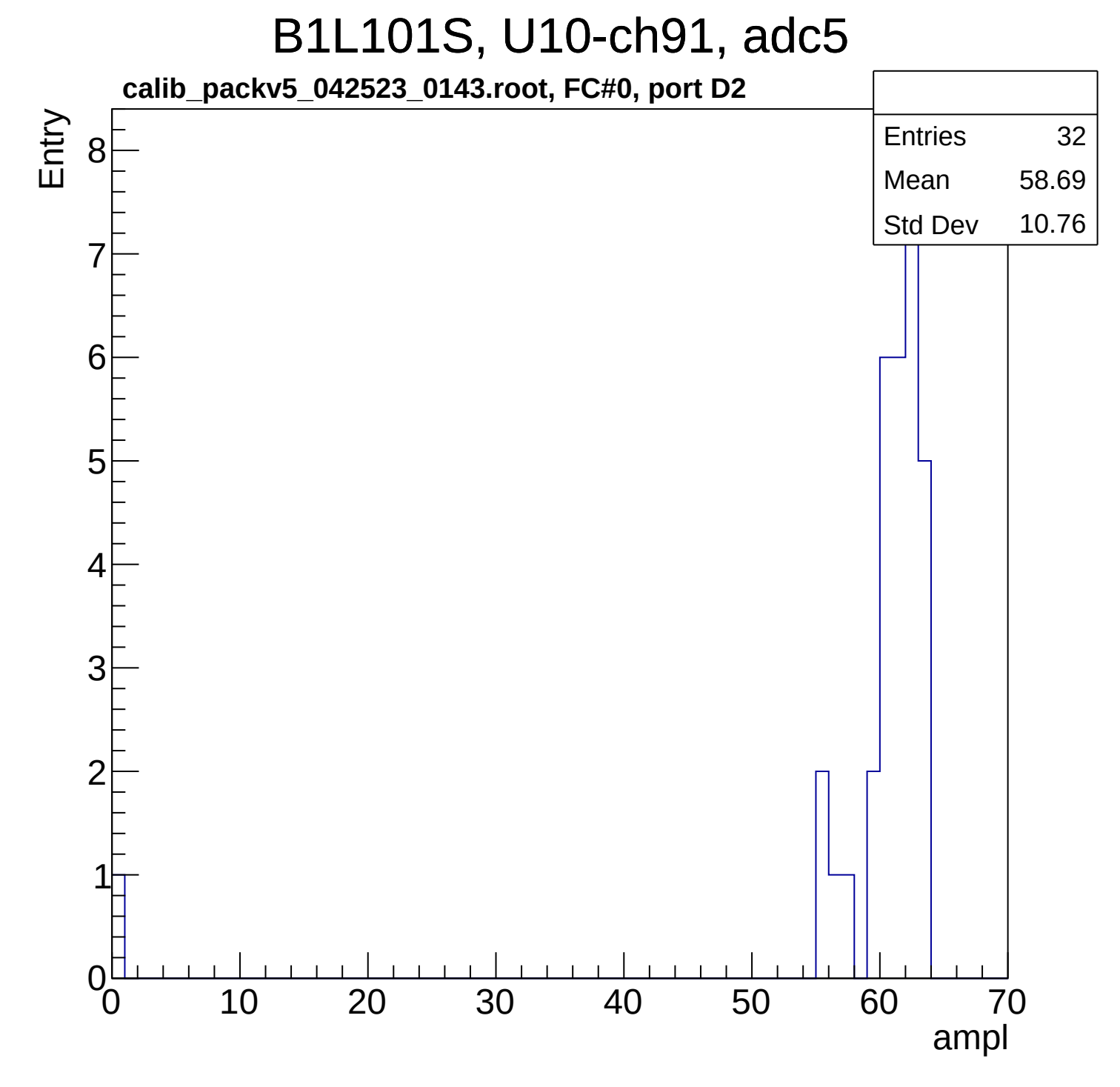
B1L101S, U10-ch91, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 32
Mean 58.69
Std Dev 10.76
Entry
ampl
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3
4
5
6
7
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0
10
20
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40
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60
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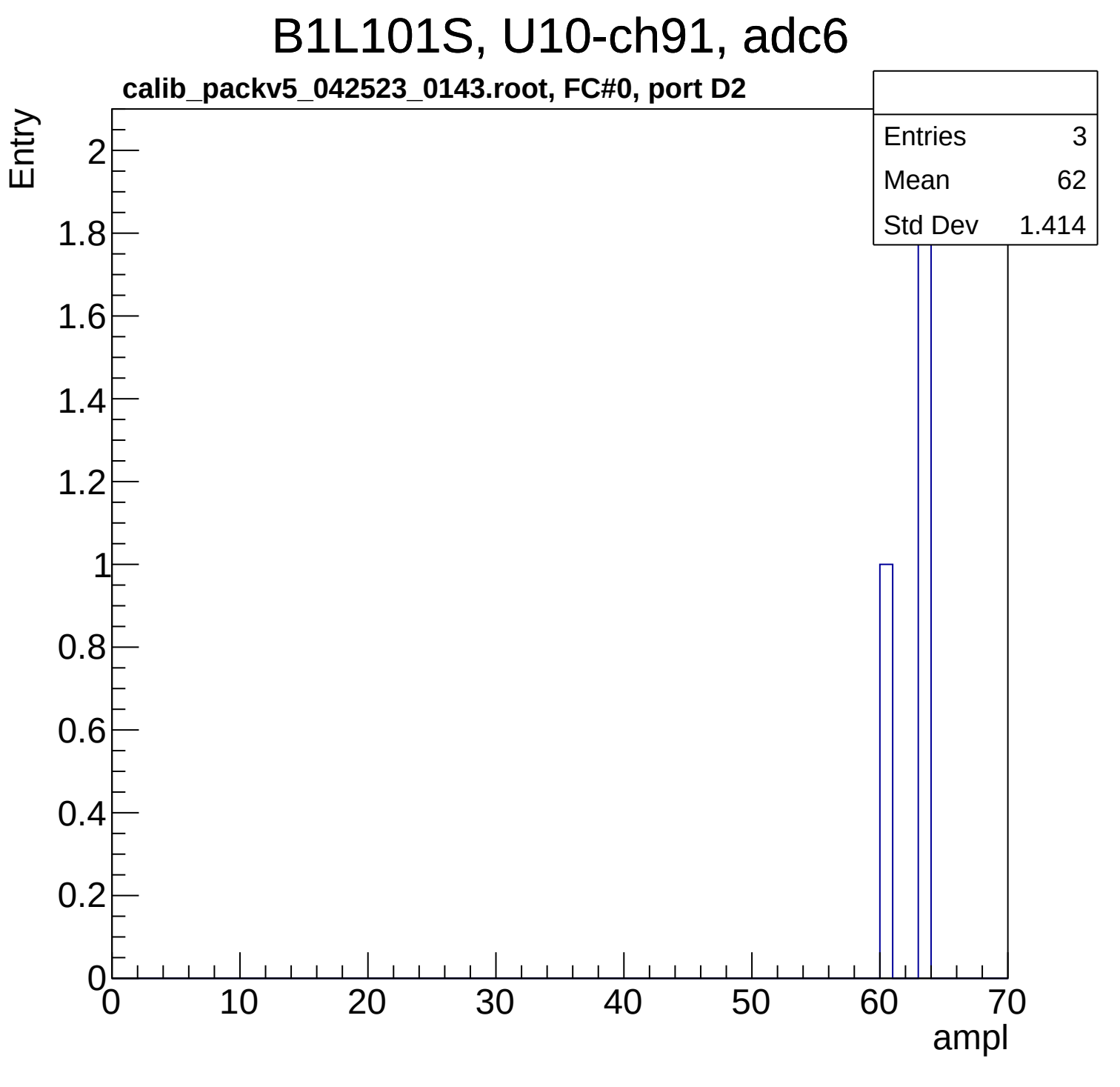
B1L101S, U10-ch91, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 62
Std Dev 1.414
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
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40
50
60
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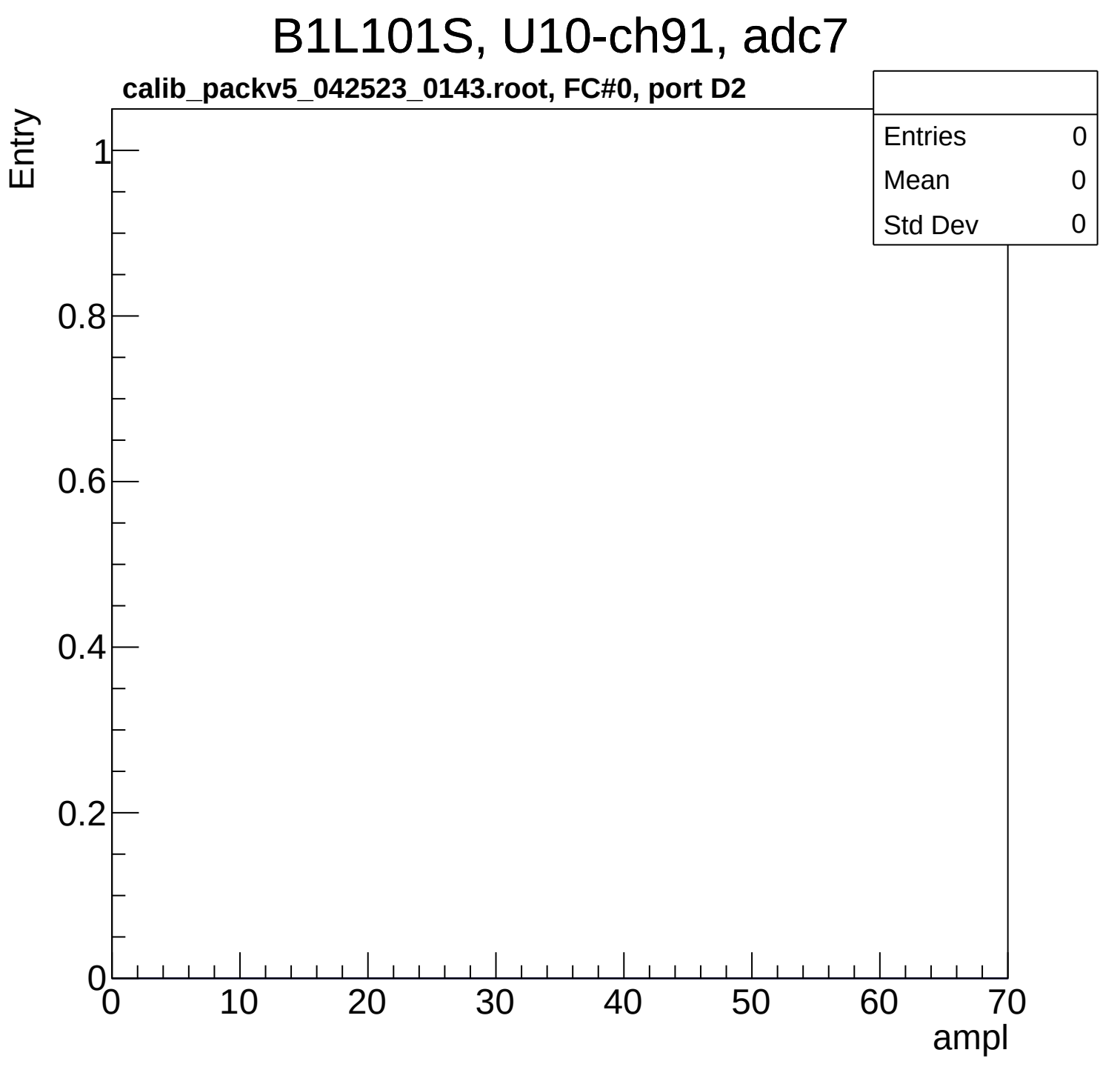
B1L101S, U10-ch91, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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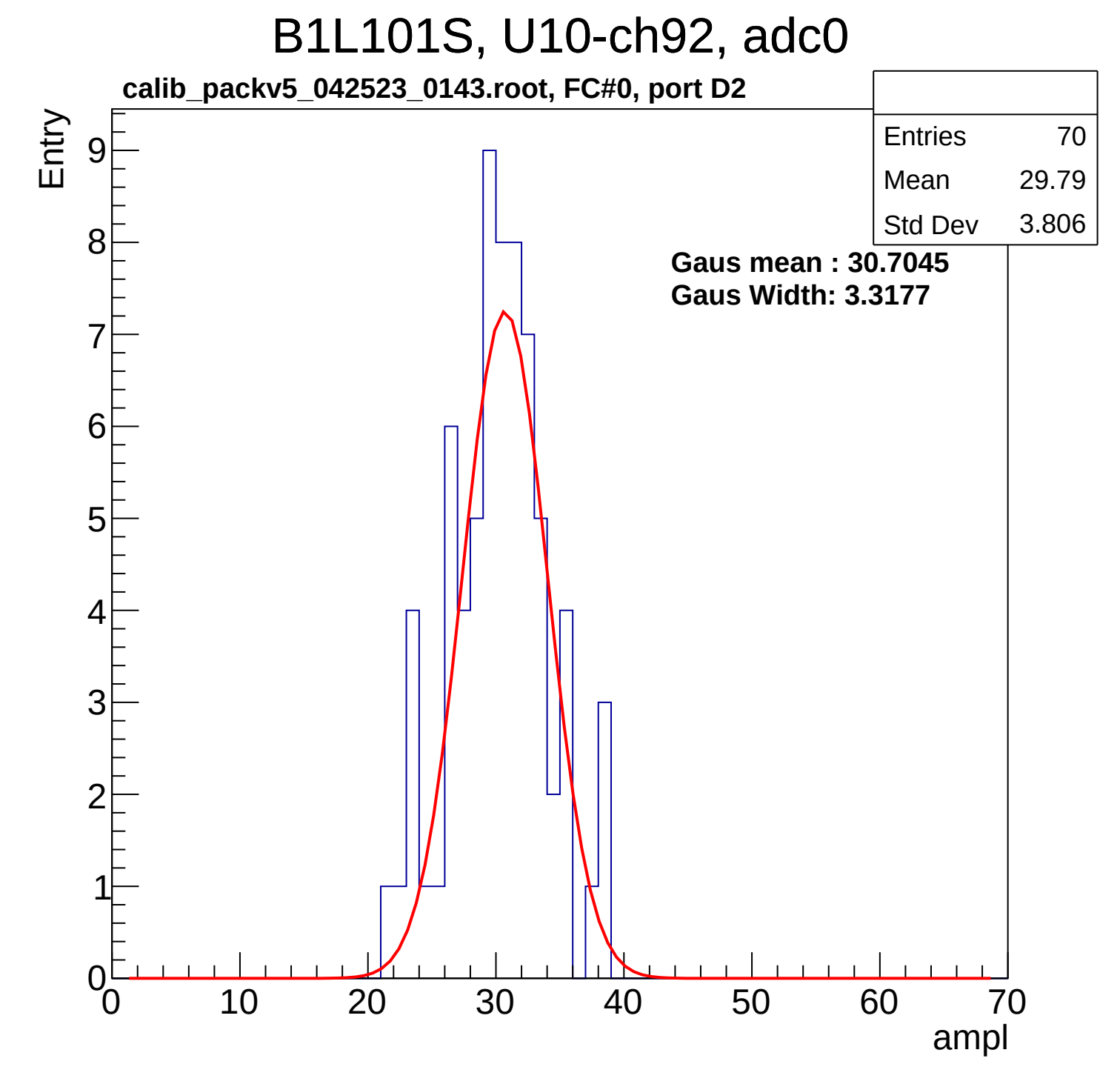
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch92, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 29.79
Std Dev 3.806
Gaus mean : 30.7045
Gaus Width: 3.3177
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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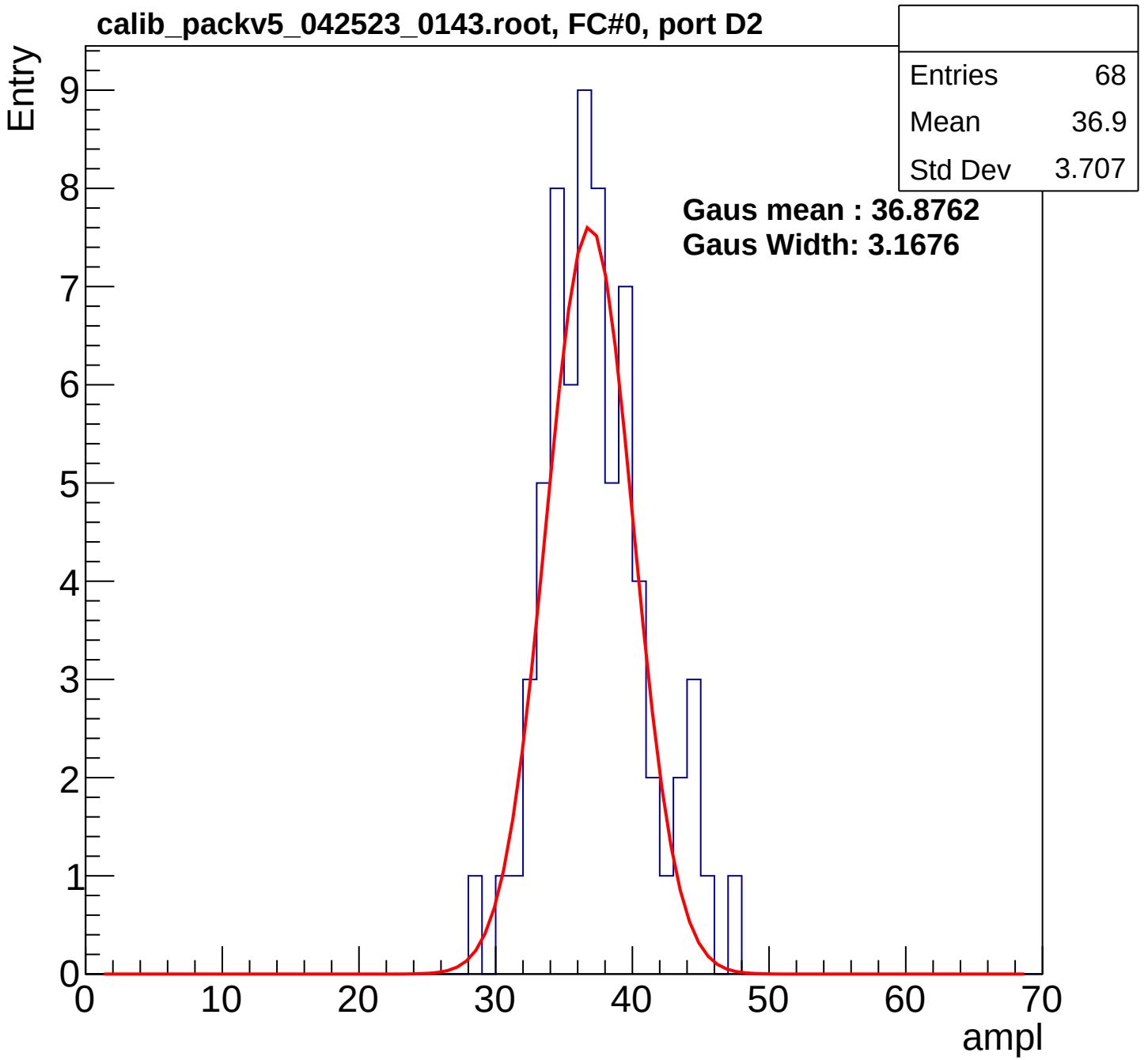
B1L101S, U10-ch92, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 36.9
Std Dev 3.707
Gaus mean : 36.8762
Gaus Width: 3.1676
Entry
ampl
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2
3
4
5
6
7
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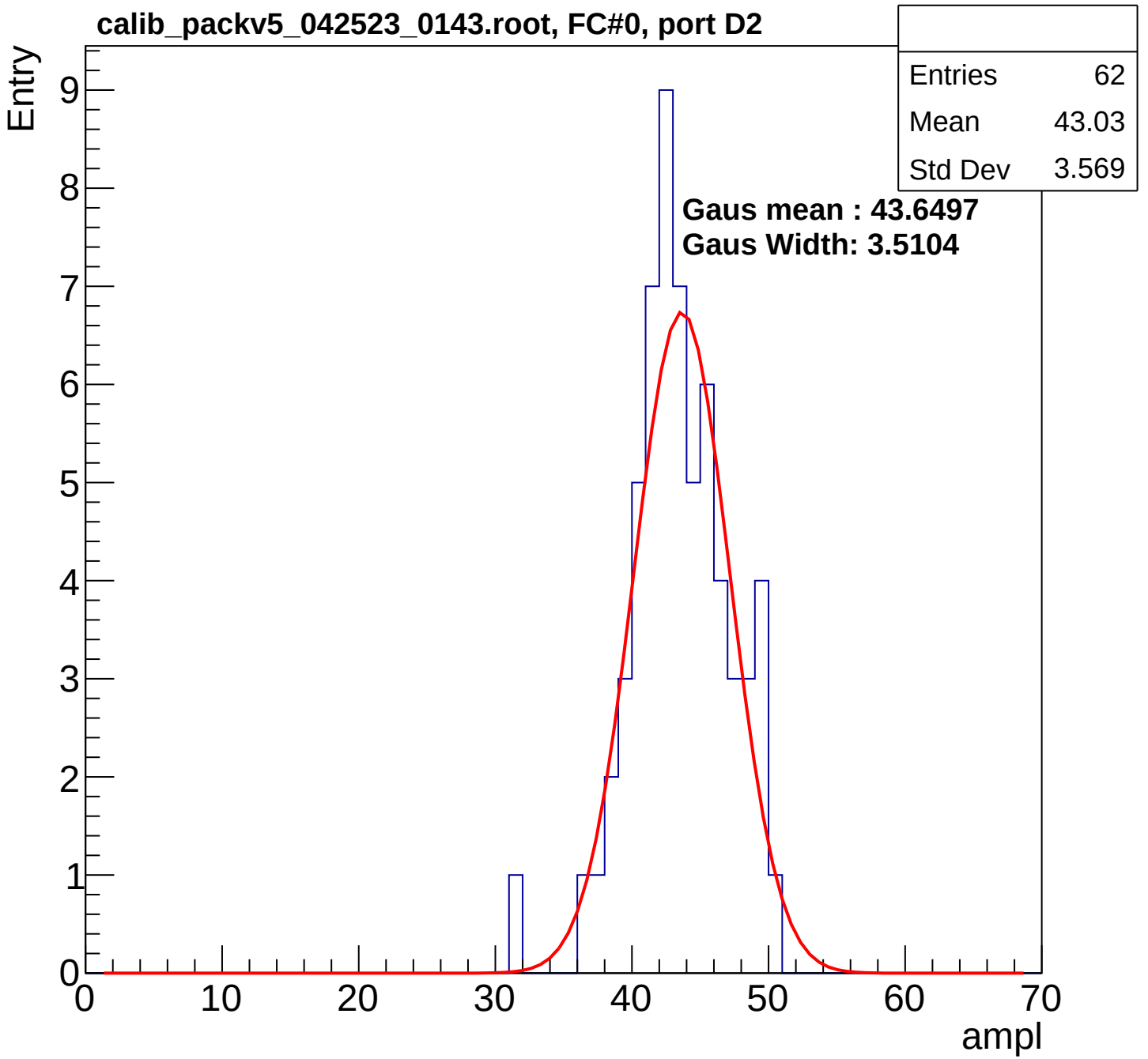
B1L101S, U10-ch92, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 43.03
Std Dev 3.569
Gaus mean : 43.6497
Gaus Width: 3.5104
Entry
ampl
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2
3
4
5
6
7
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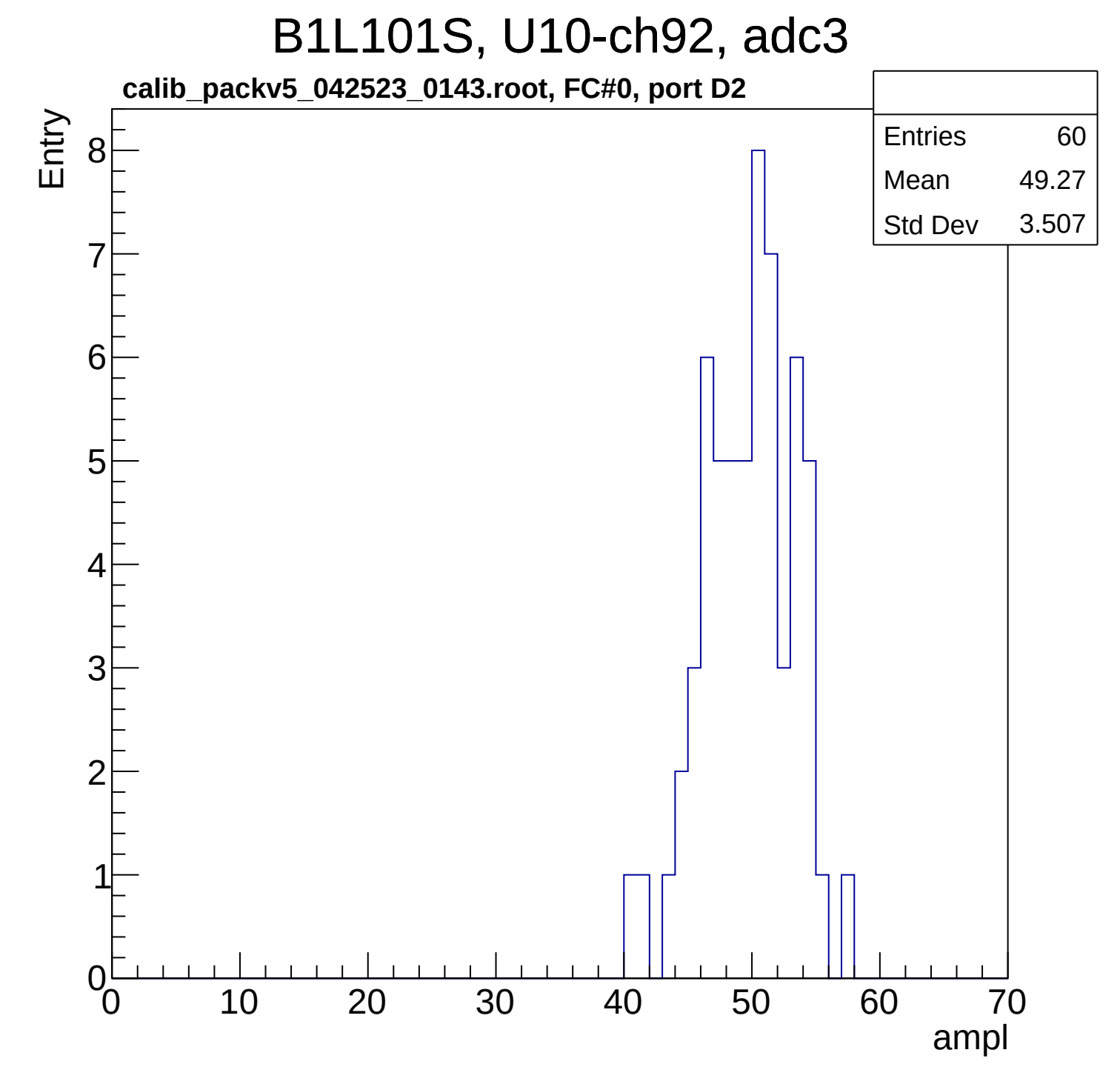
B1L101S, U10-ch92, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 49.27
Std Dev 3.507
Entry
ampl
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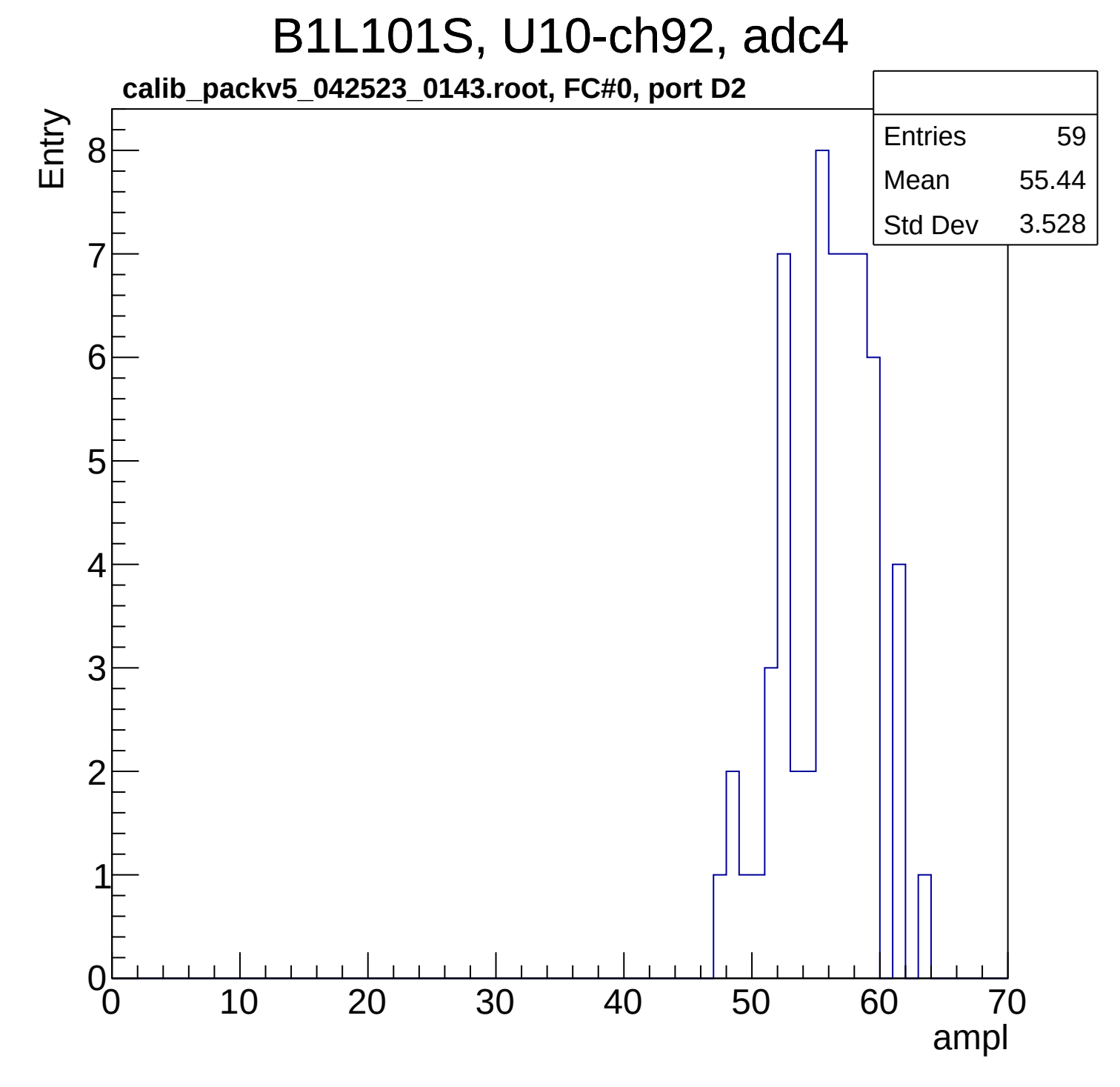
B1L101S, U10-ch92, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 55.44
Std Dev 3.528
Entry
ampl
0
1
2
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5
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0
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60
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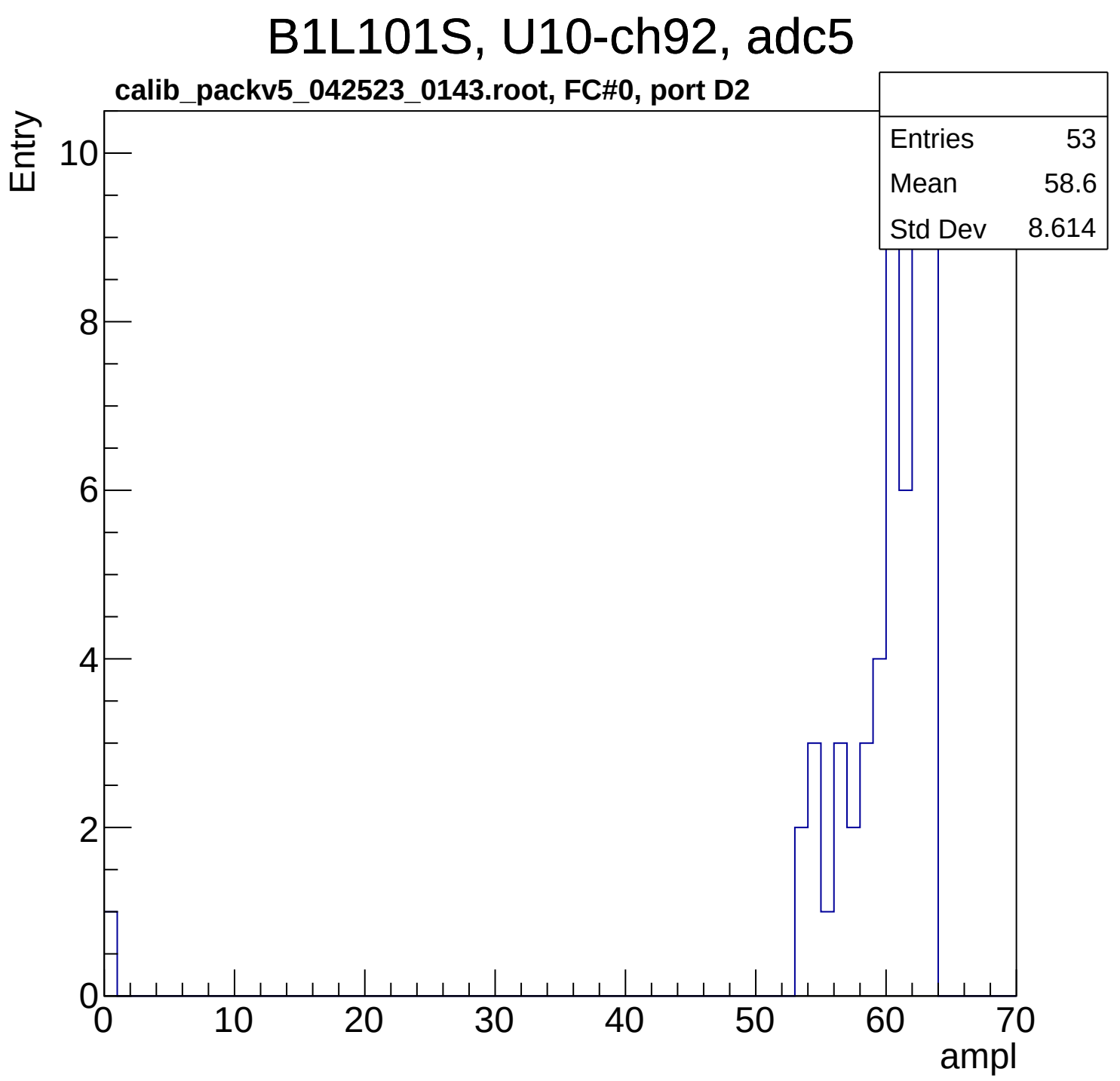
B1L101S, U10-ch92, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 58.6
Std Dev 8.614
Entry
ampl
0
2
4
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8
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0
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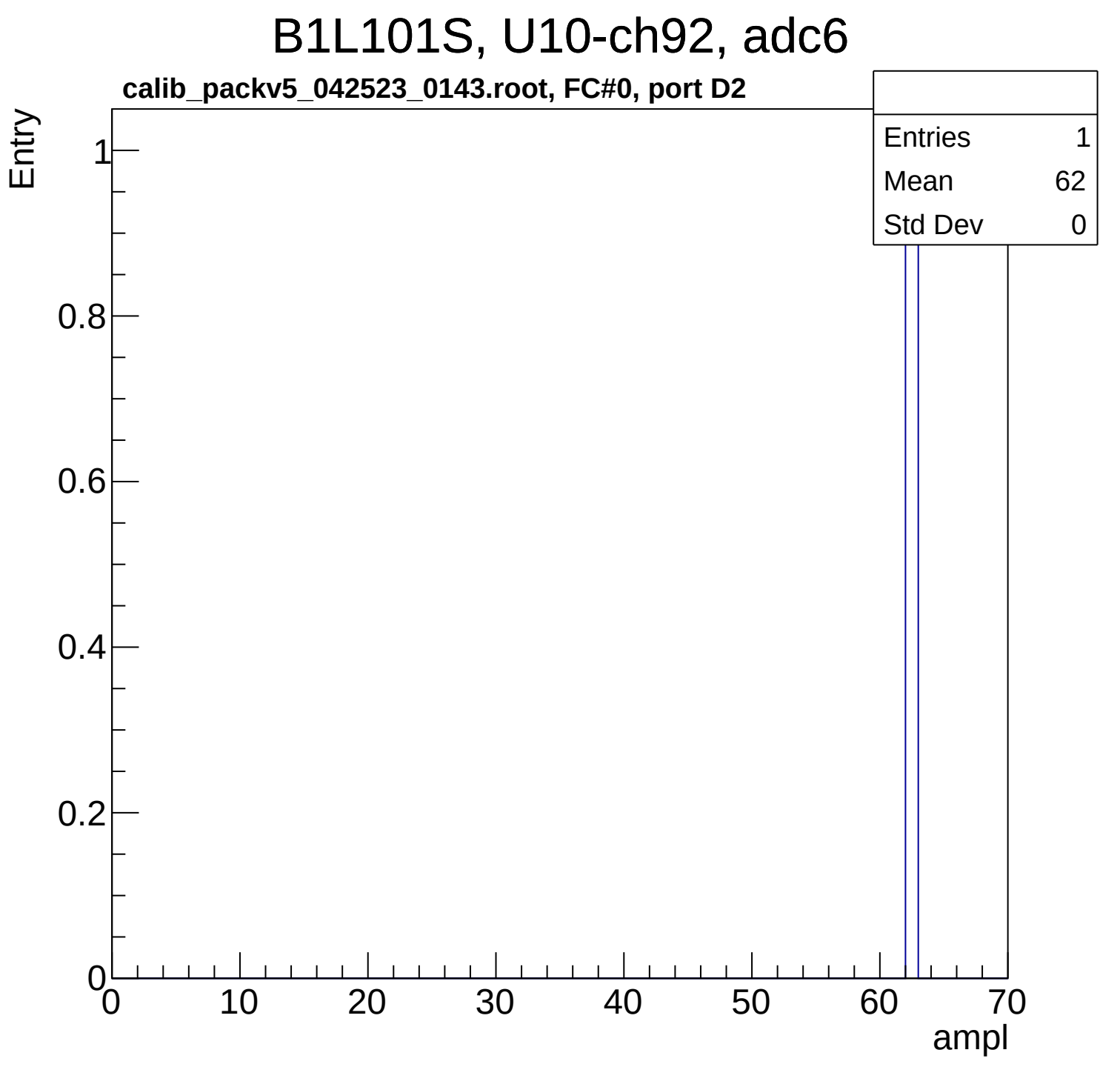
B1L101S, U10-ch92, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 62
Std Dev 0
Entry
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0.6
0.4
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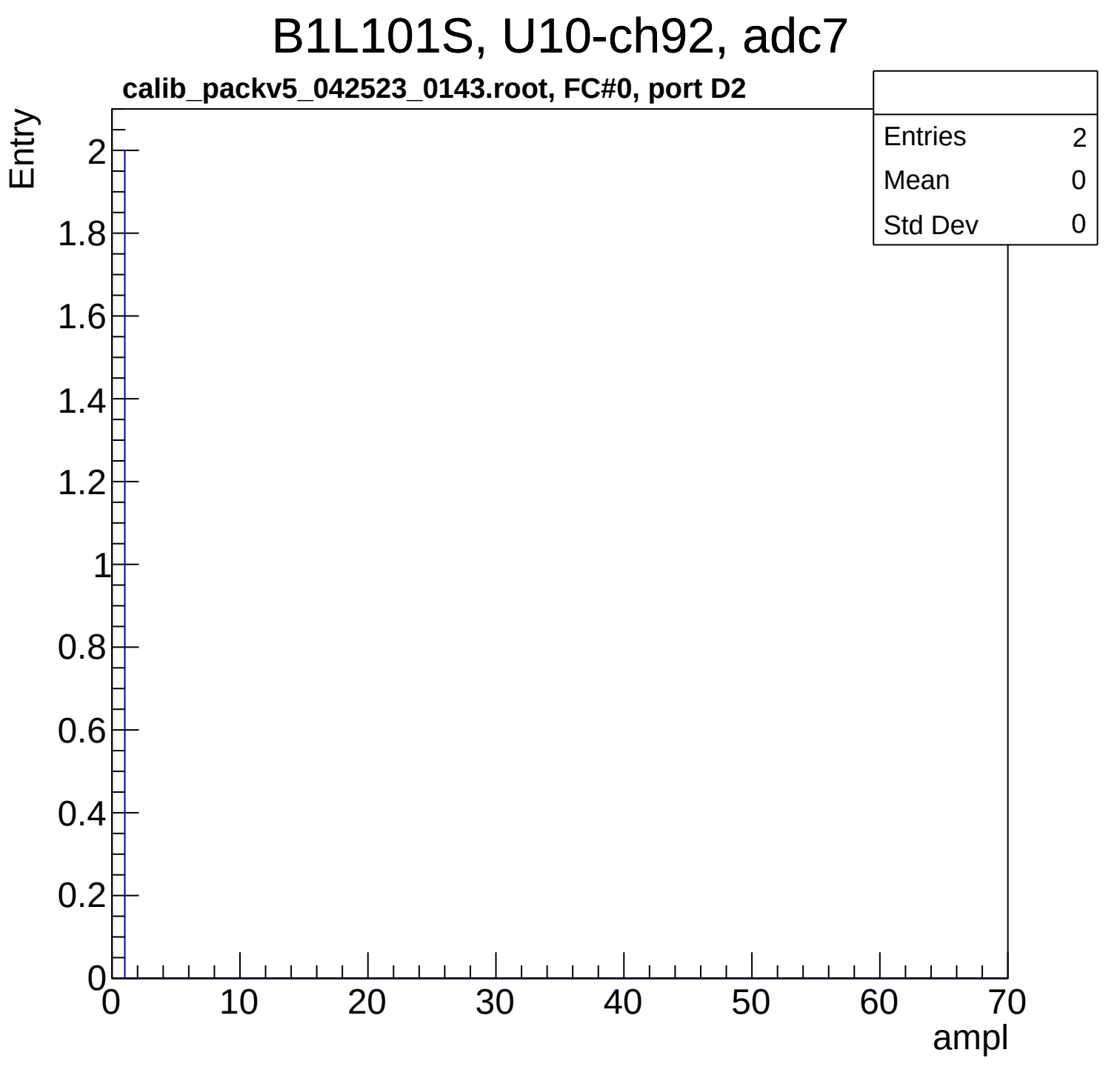
70
ampl


B1L101S, U10-ch92, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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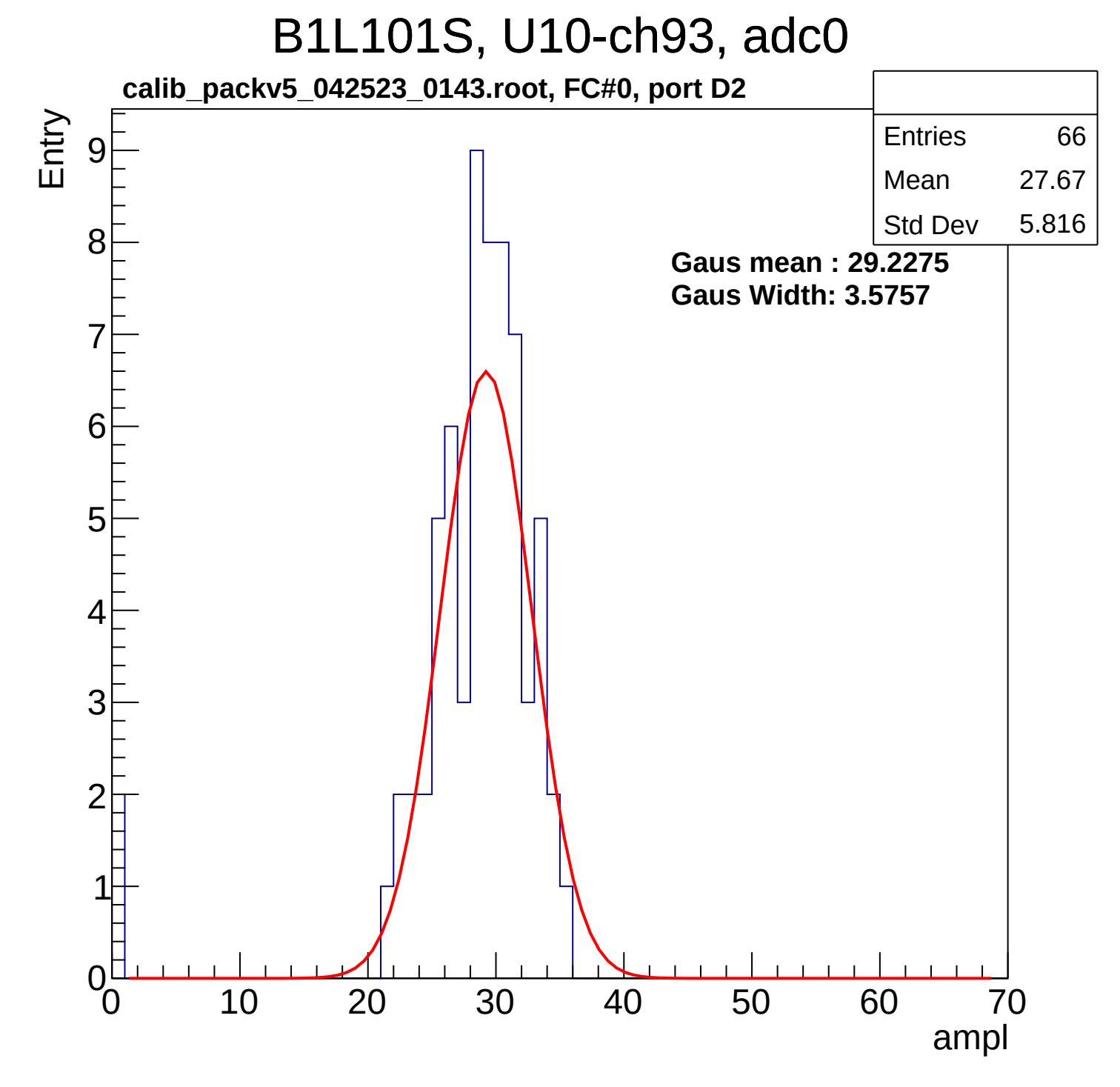
B1L101S, U10-ch93, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 27.67
Std Dev 5.816
Gaus mean : 29.2275
Gaus Width: 3.5757
Entry
ampl
0
1
2
3
4
5
6
7
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0
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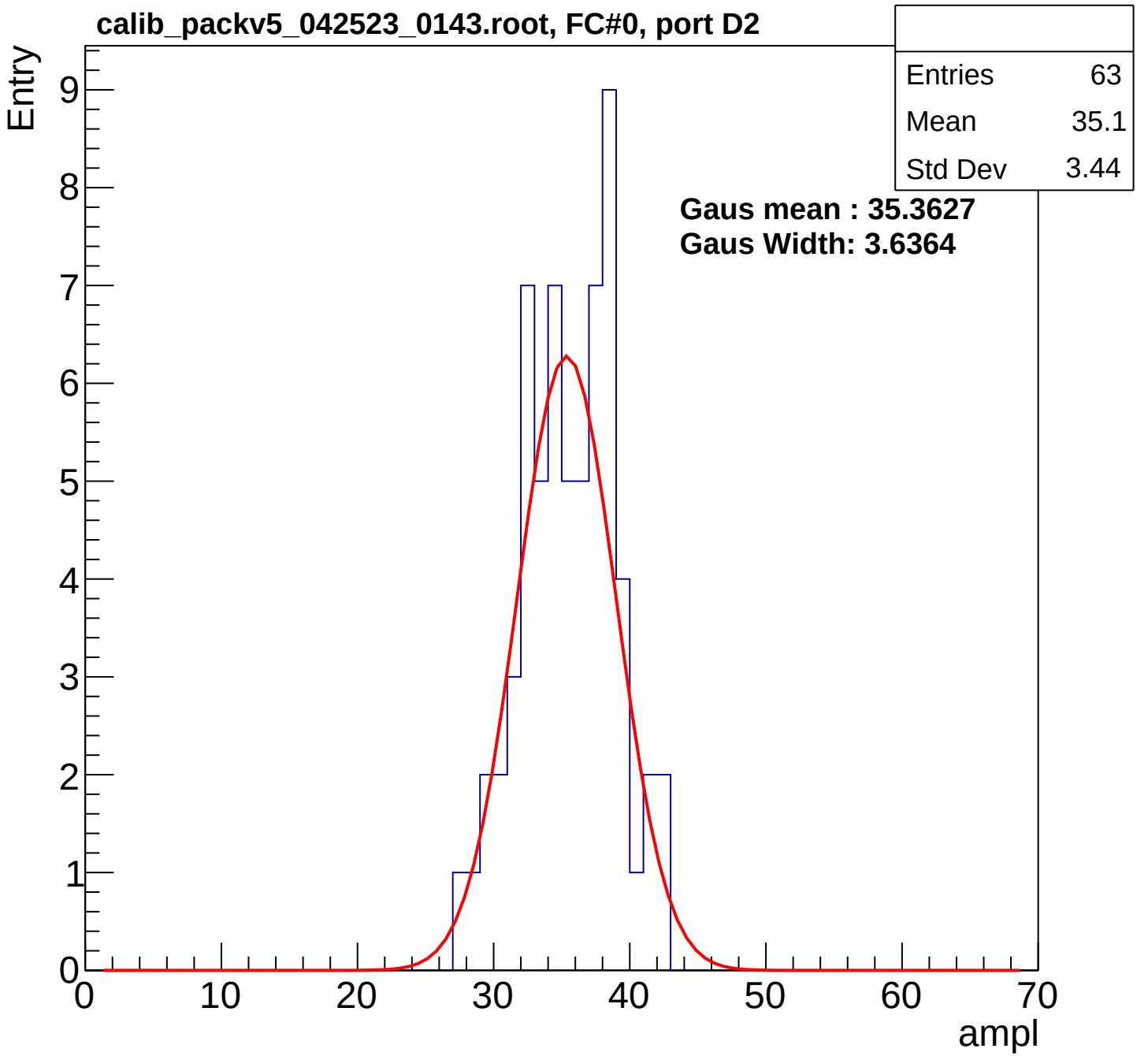
B1L101S, U10-ch93, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 35.1
Std Dev 3.44
Gaus mean : 35.3627
Gaus Width: 3.6364
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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40
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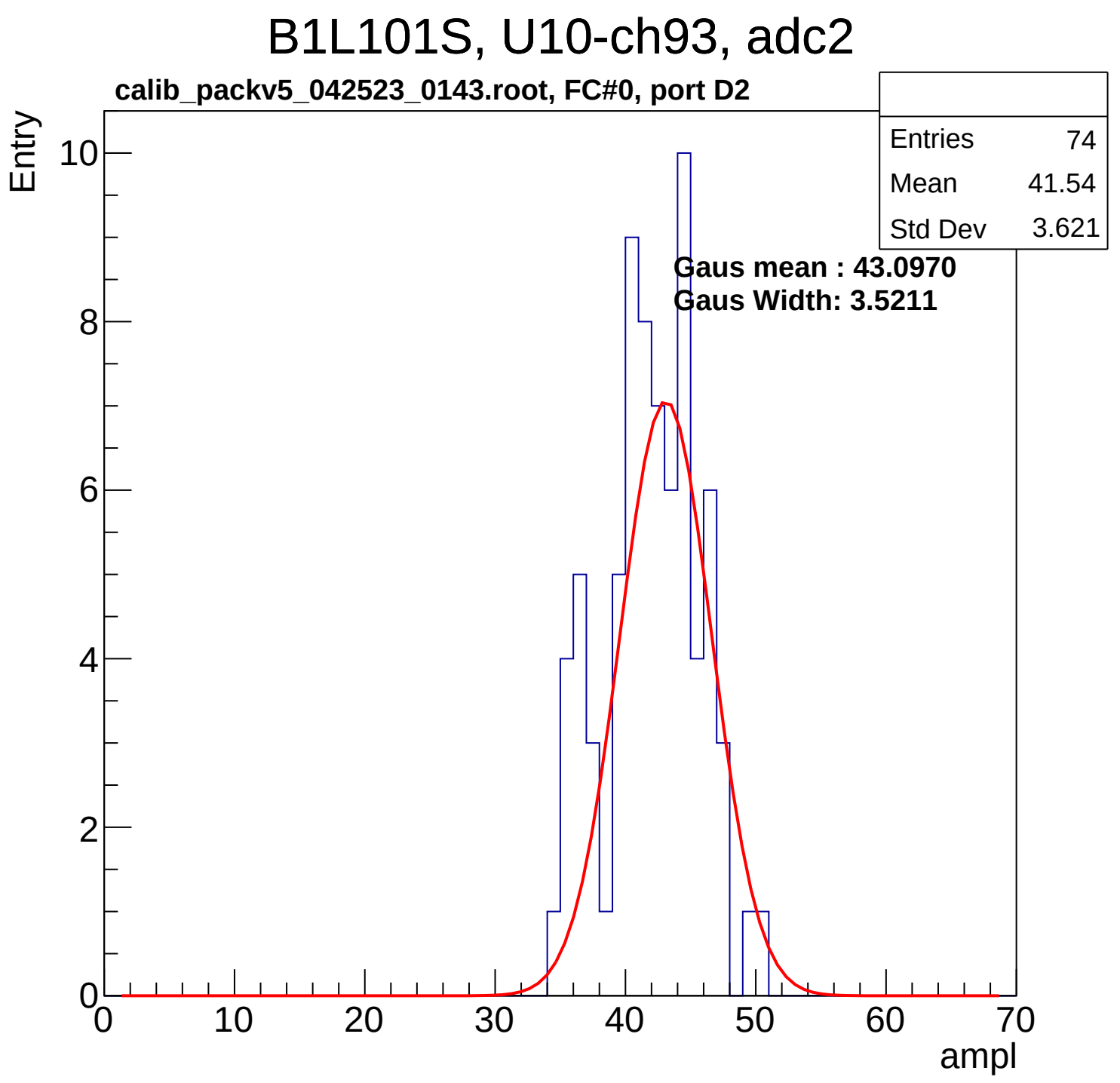
B1L101S, U10-ch93, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 41.54
Std Dev 3.621
Gaus mean : 43.0970
Gaus Width: 3.5211
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
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60
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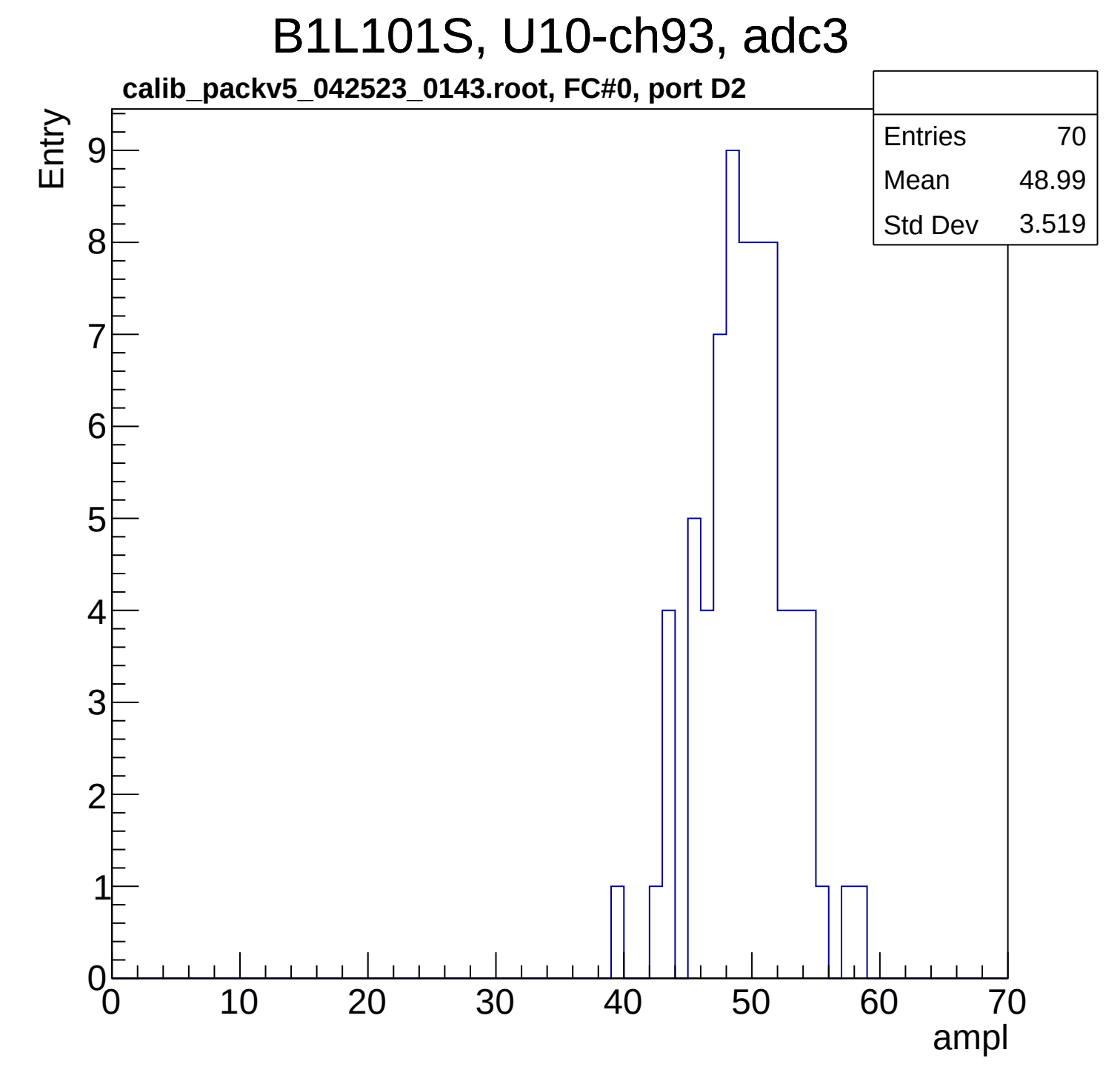
B1L101S, U10-ch93, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 48.99
Std Dev 3.519
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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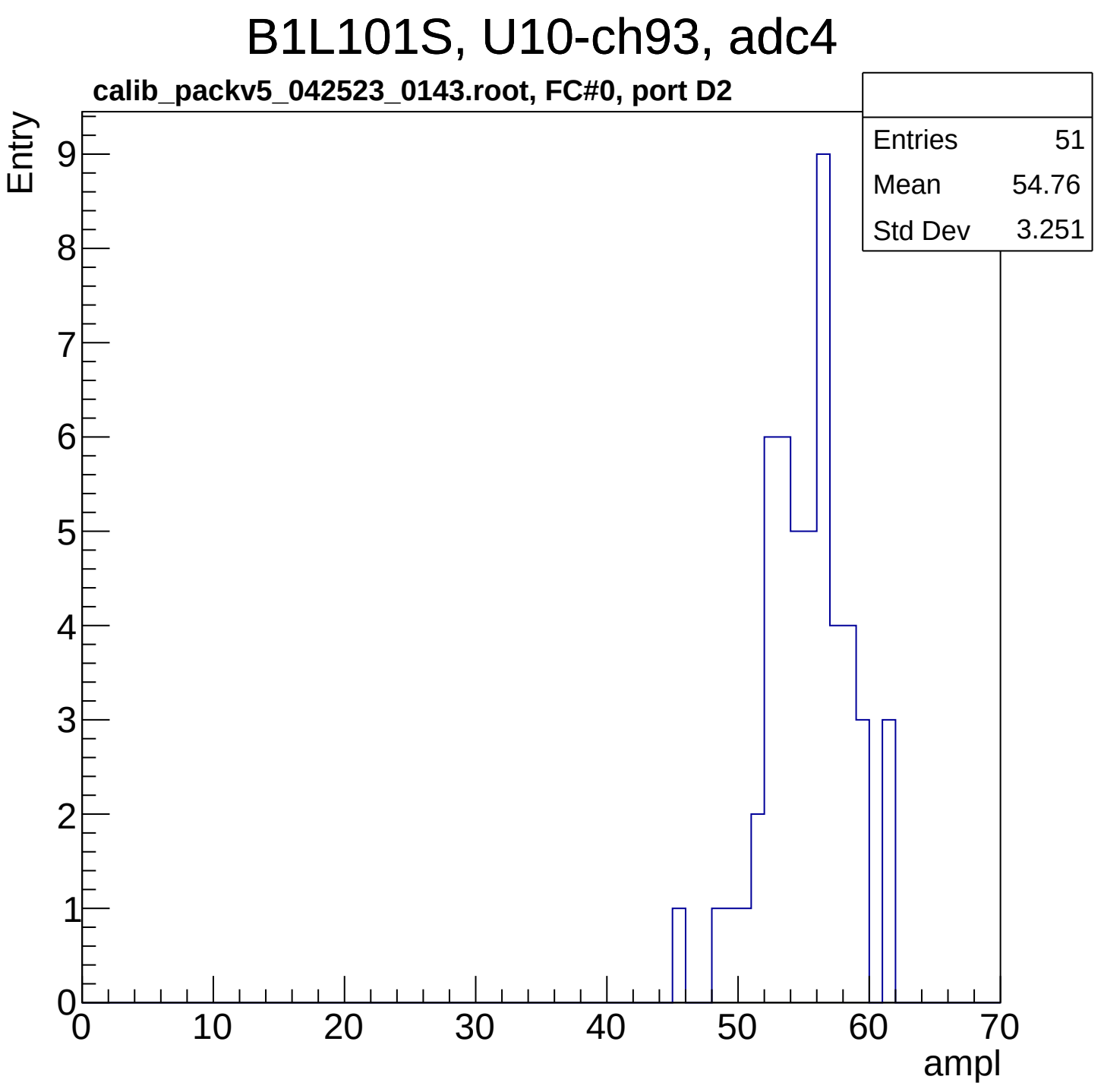
B1L101S, U10-ch93, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 54.76
Std Dev 3.251
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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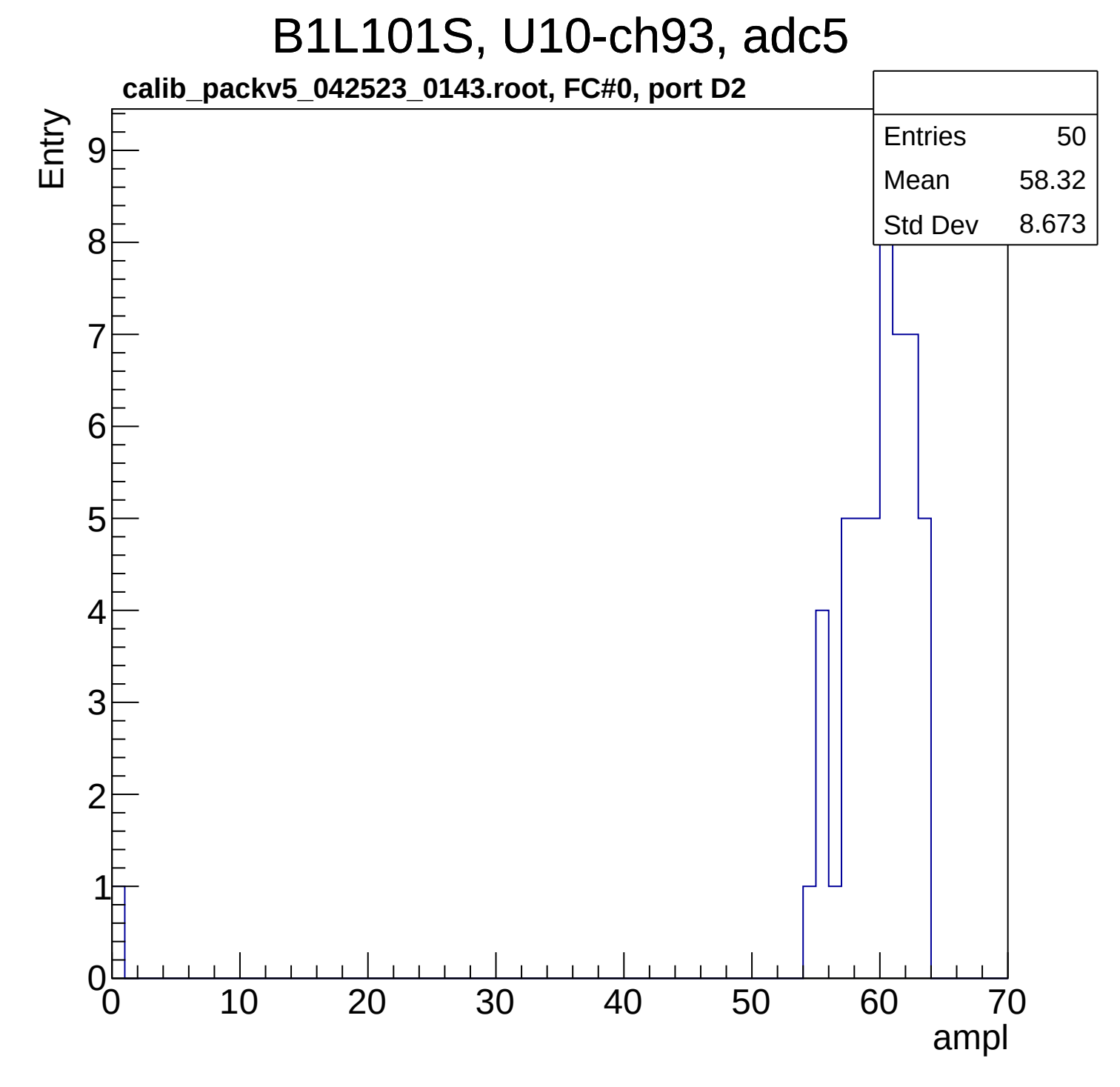
B1L101S, U10-ch93, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 58.32
Std Dev 8.673
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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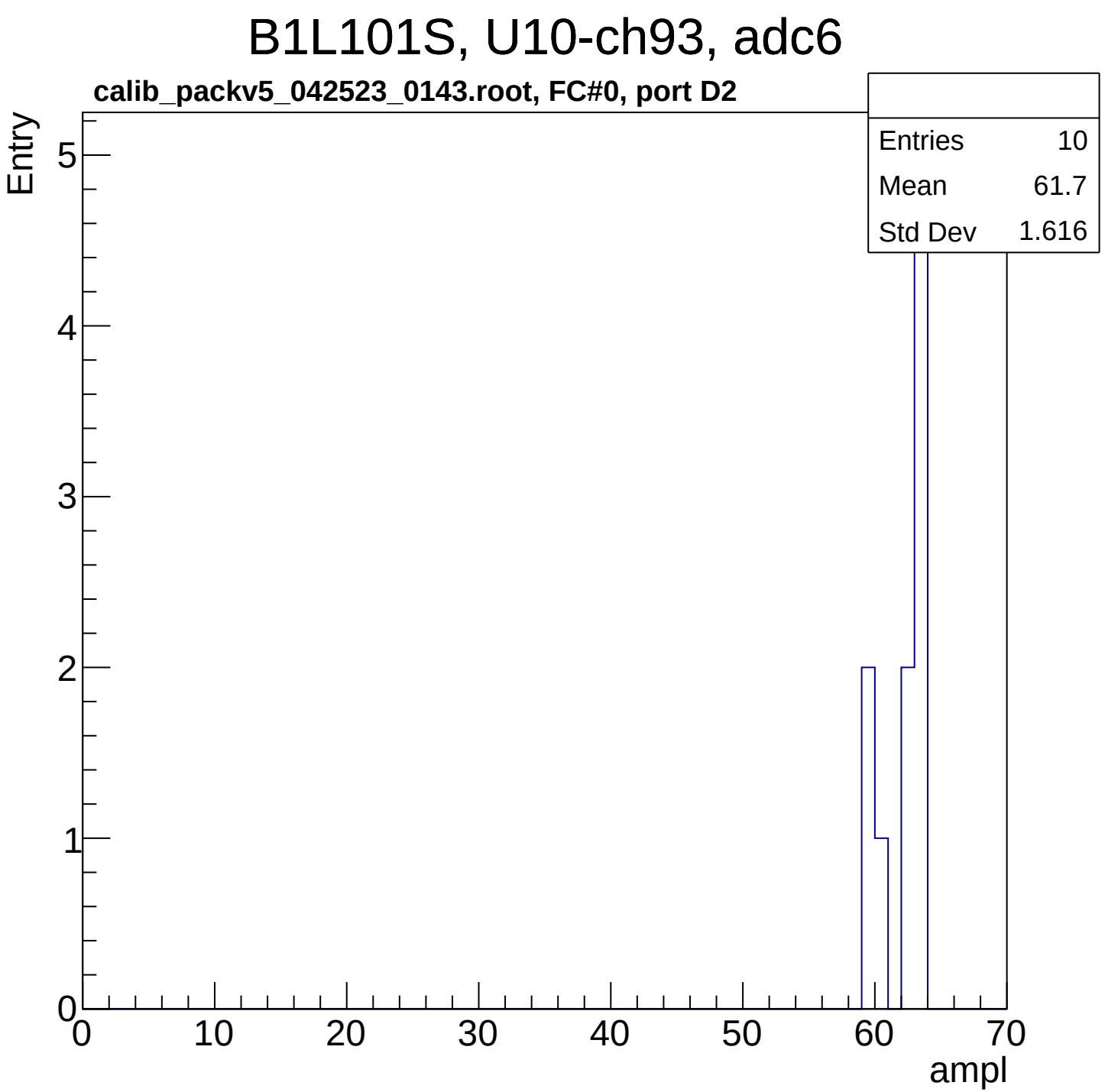
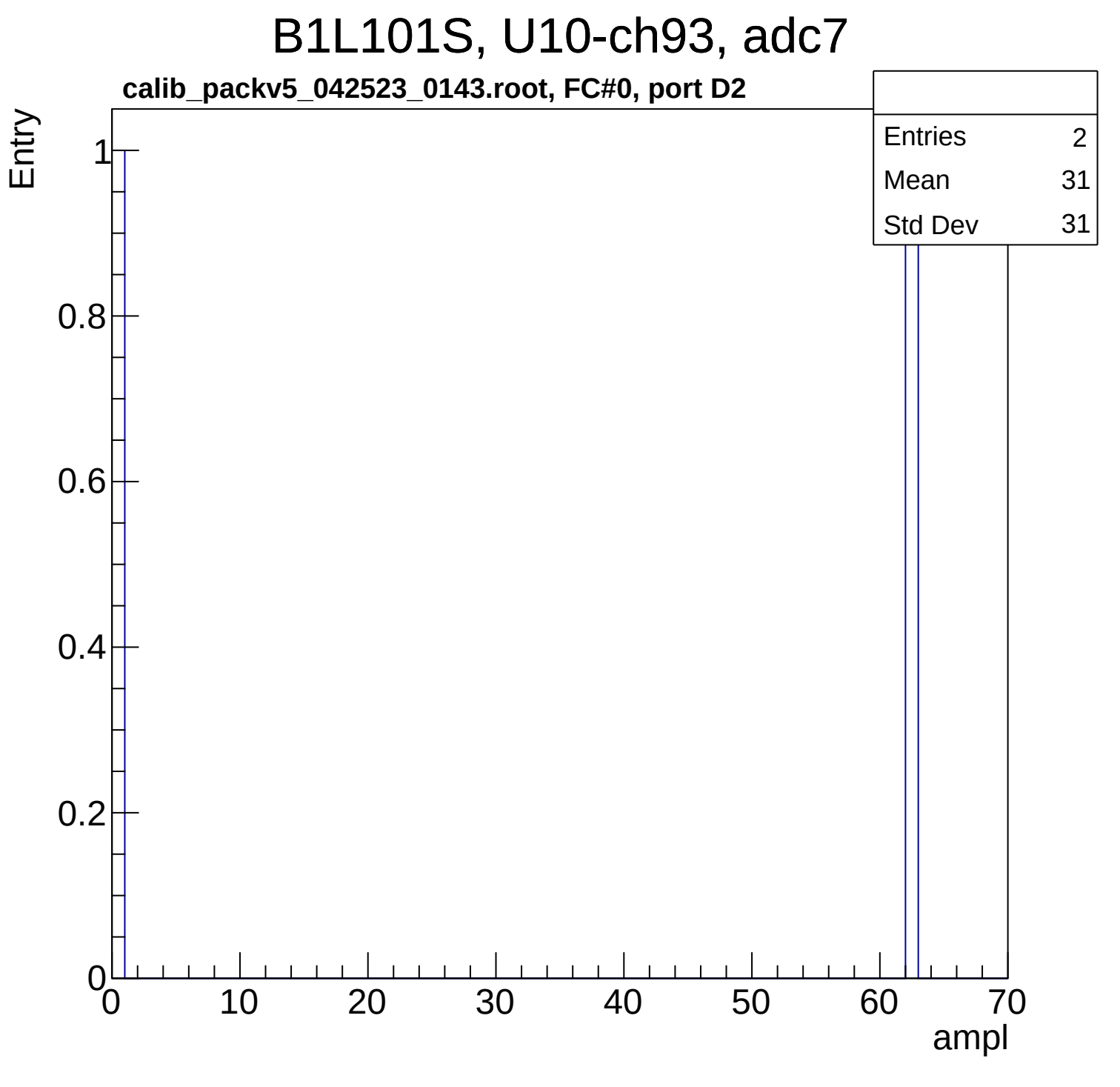

B1L101S, U10-ch93, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 61.7
Std Dev 1.616
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch93, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 31
Std Dev 31
Entry
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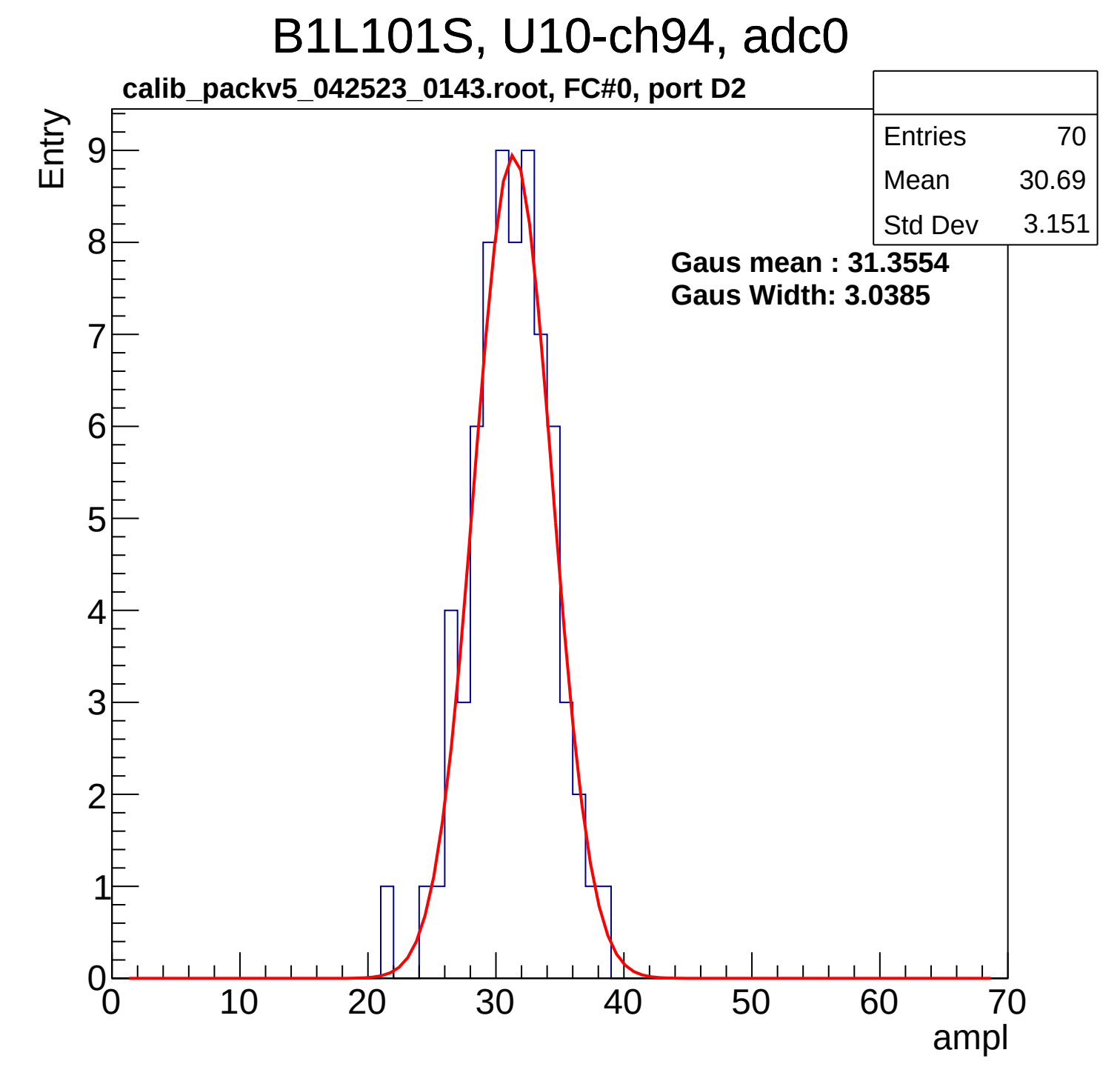
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch94, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 30.69
Std Dev 3.151
Gaus mean : 31.3554
Gaus Width: 3.0385
Entry
ampl
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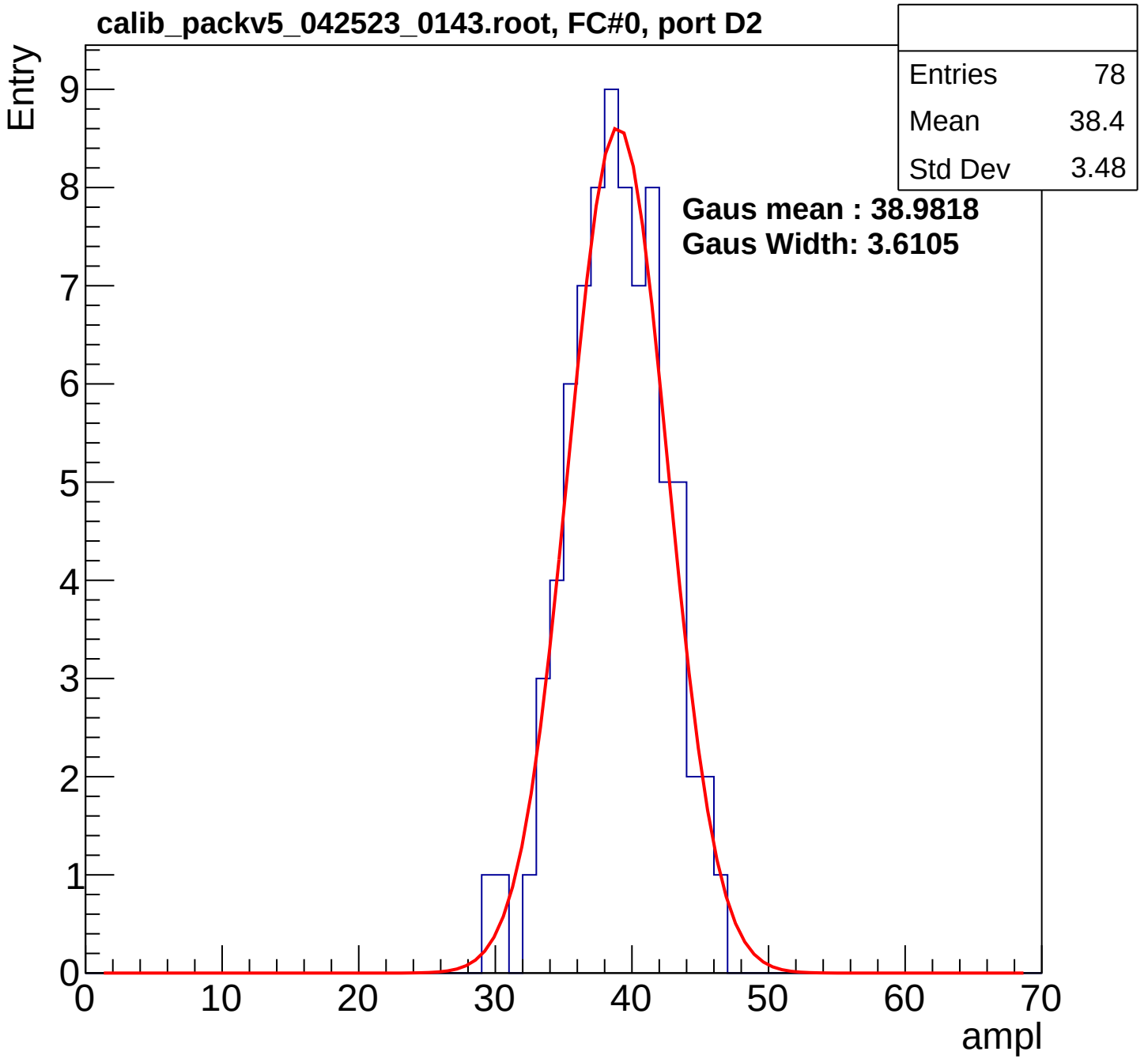
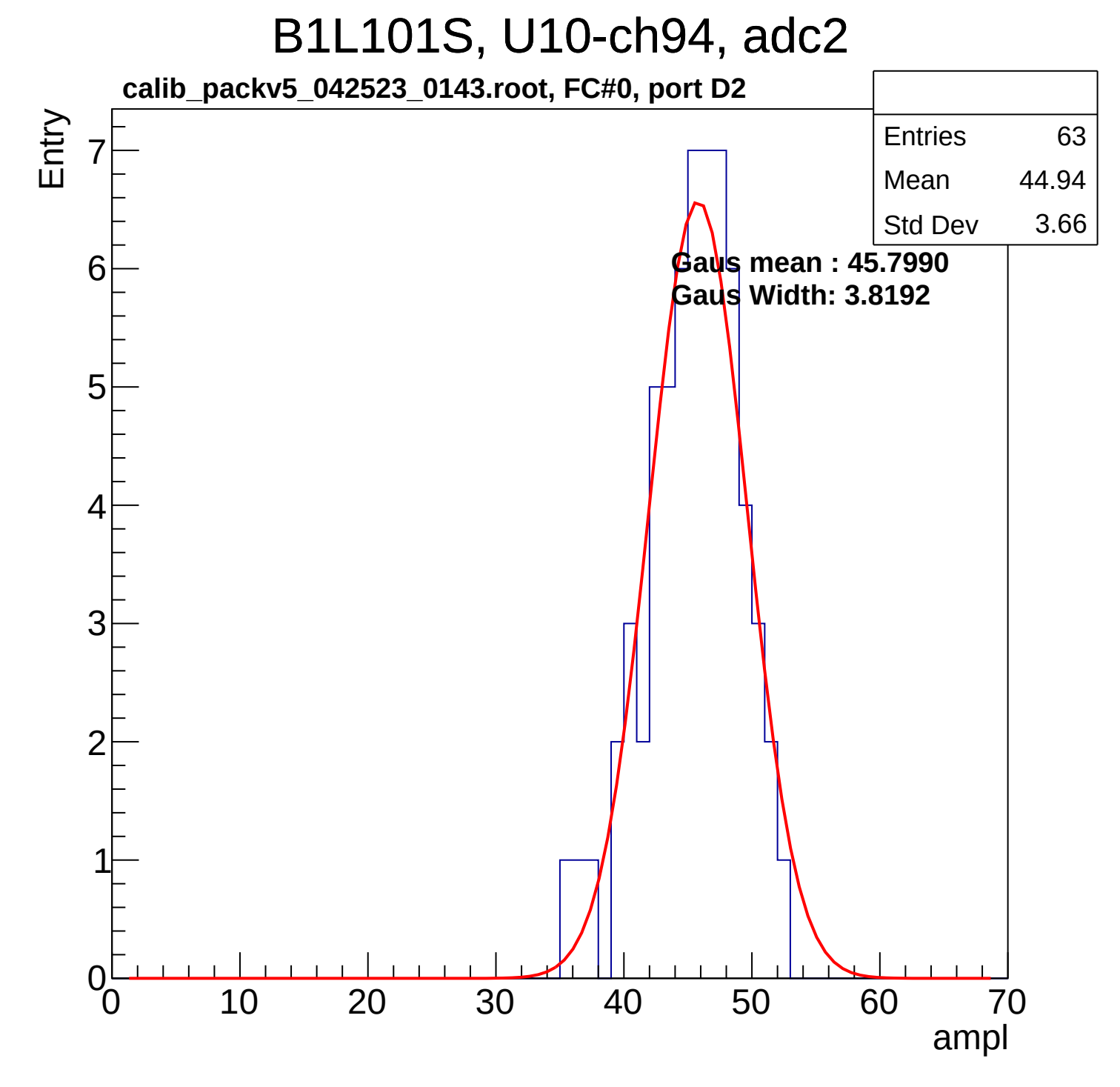
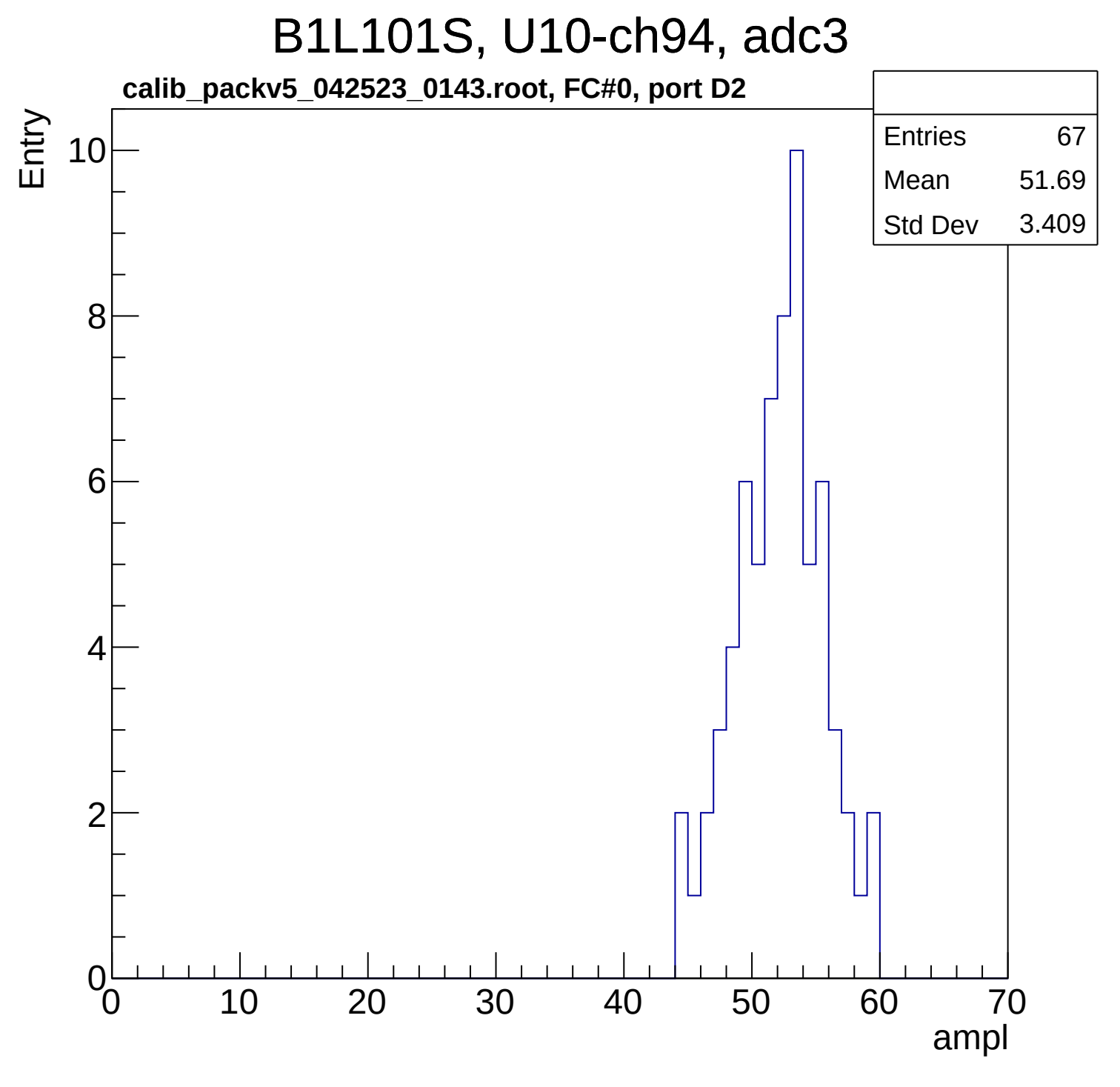
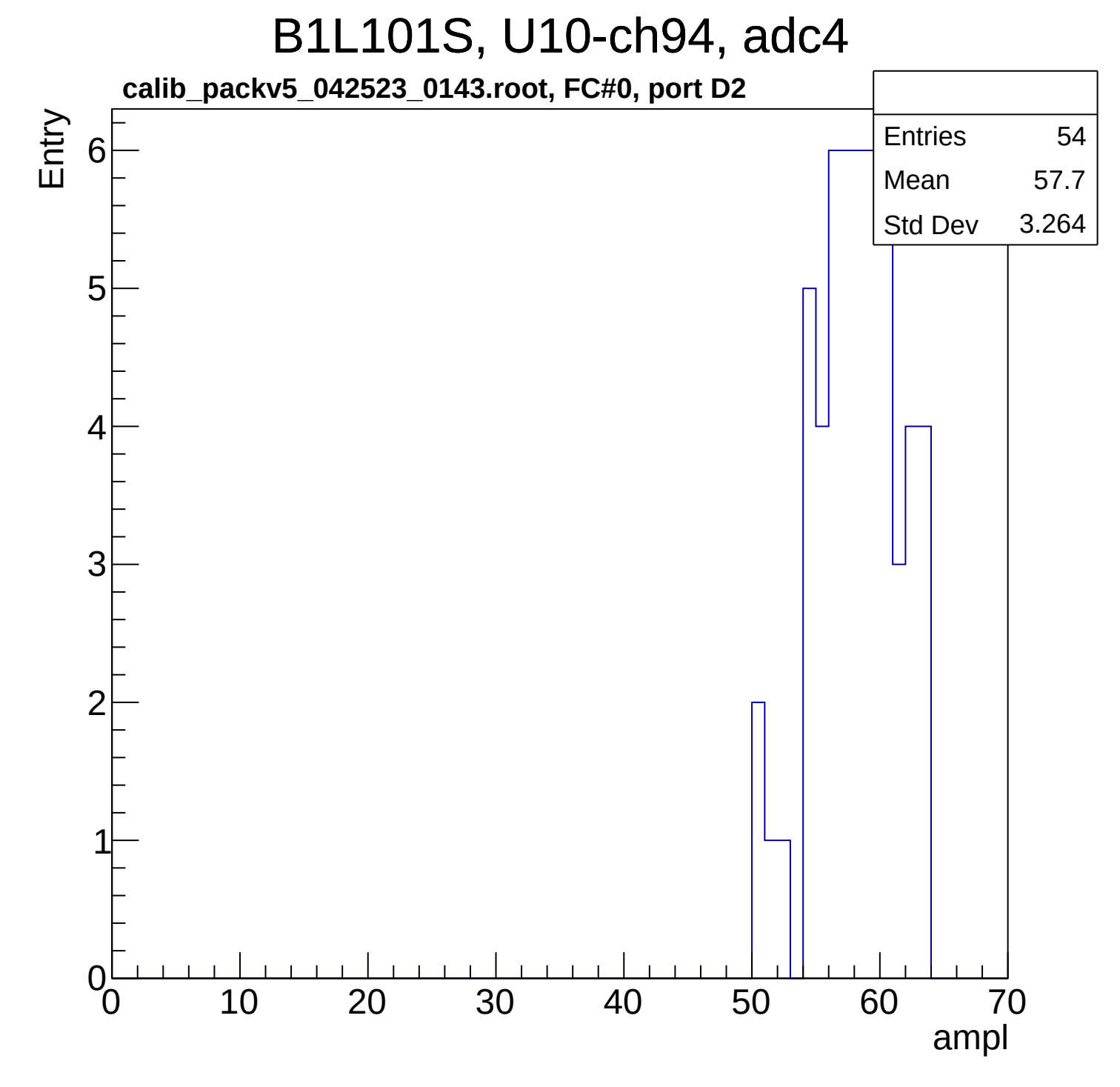
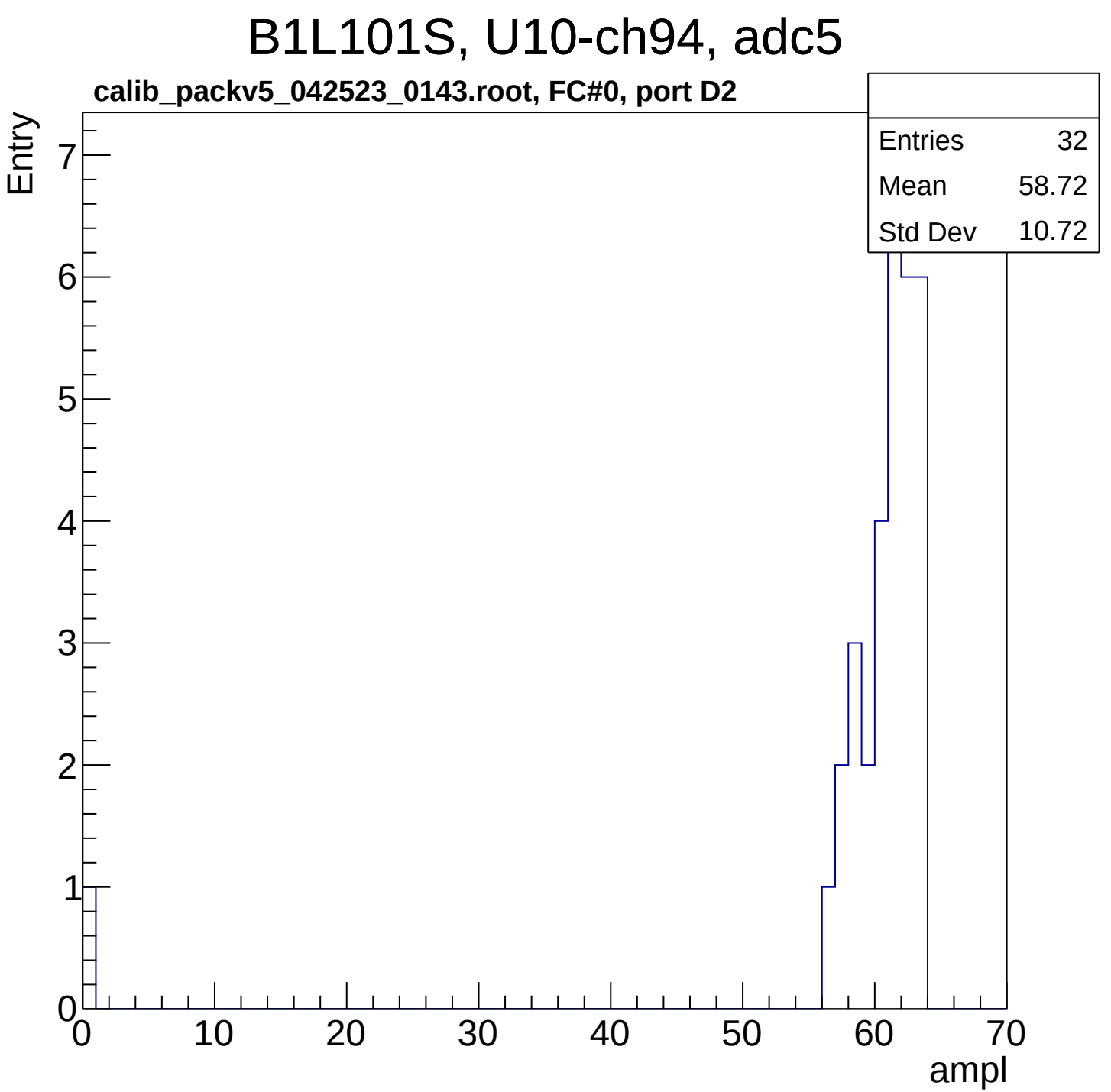
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch94, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 38.4
Std Dev 3.48
Gaus mean : 38.9818
Gaus Width: 3.6105
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch94, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 44.94
Std Dev 3.66
Gaus mean : 45.7990
Gaus Width: 3.8192
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U10-ch94, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 51.69
Std Dev 3.409
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch94, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 57.7
Std Dev 3.264
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L101S, U10-ch94, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 32
Mean 58.72
Std Dev 10.72
Entry
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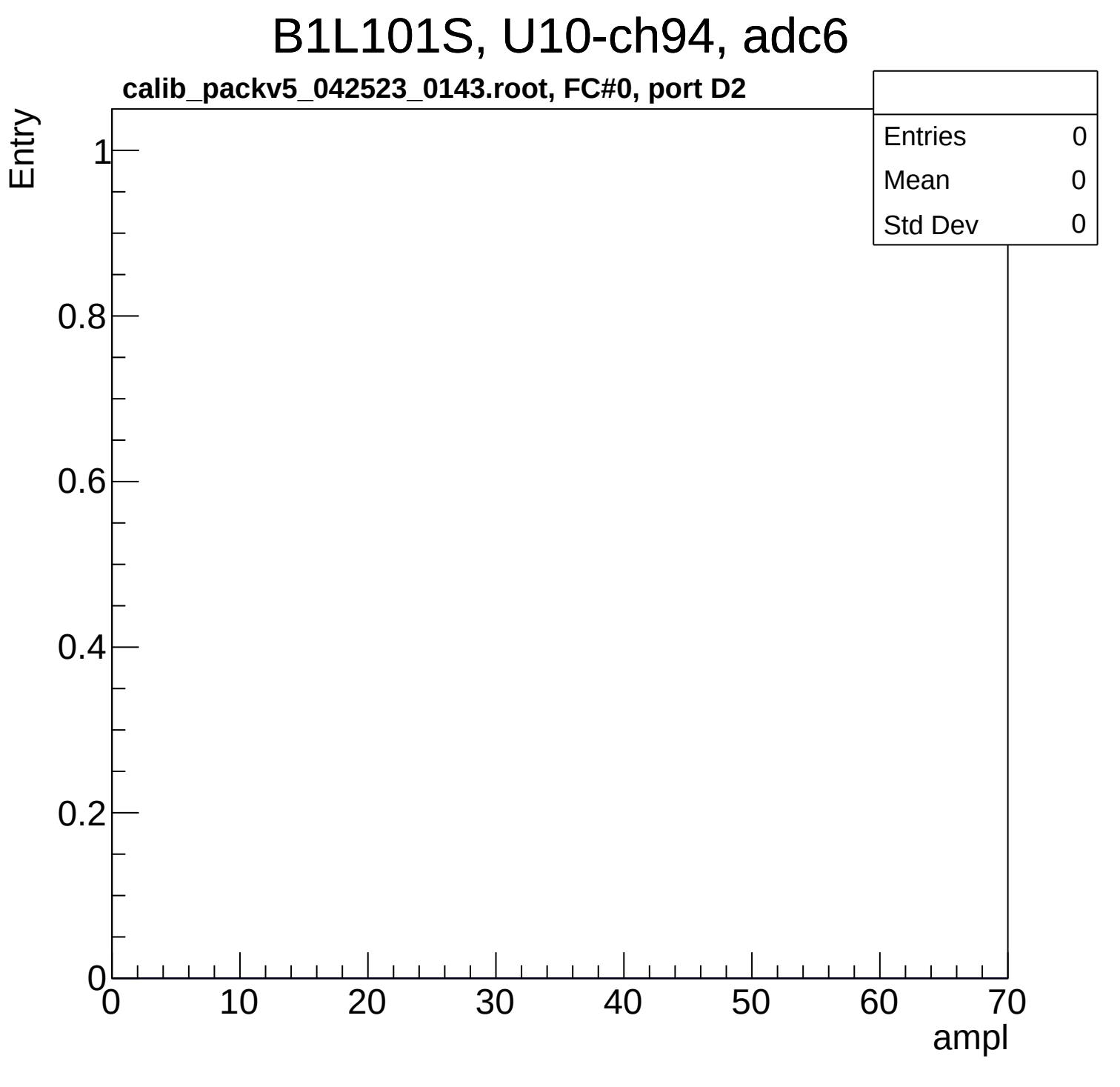
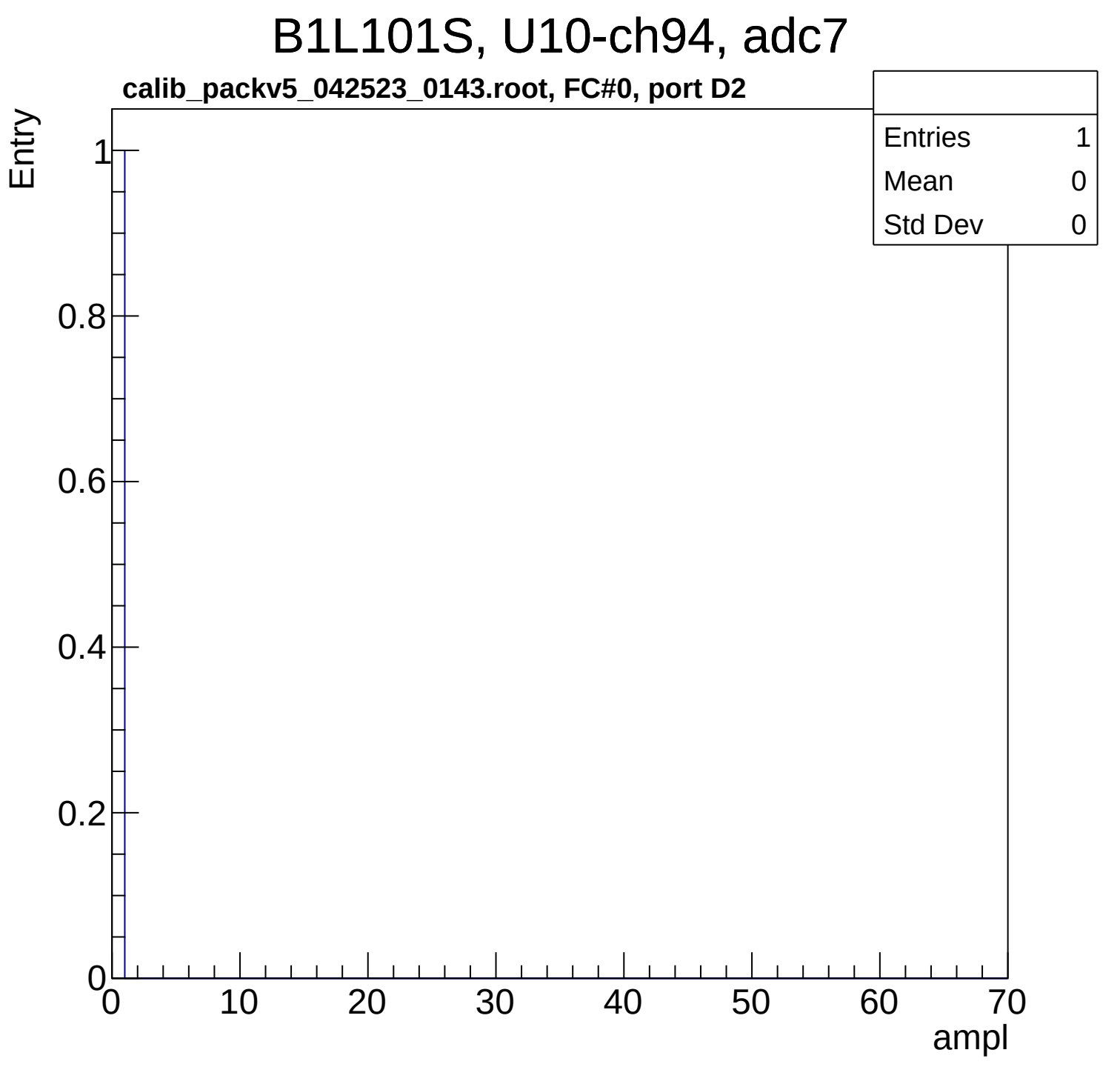
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch94, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch94, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
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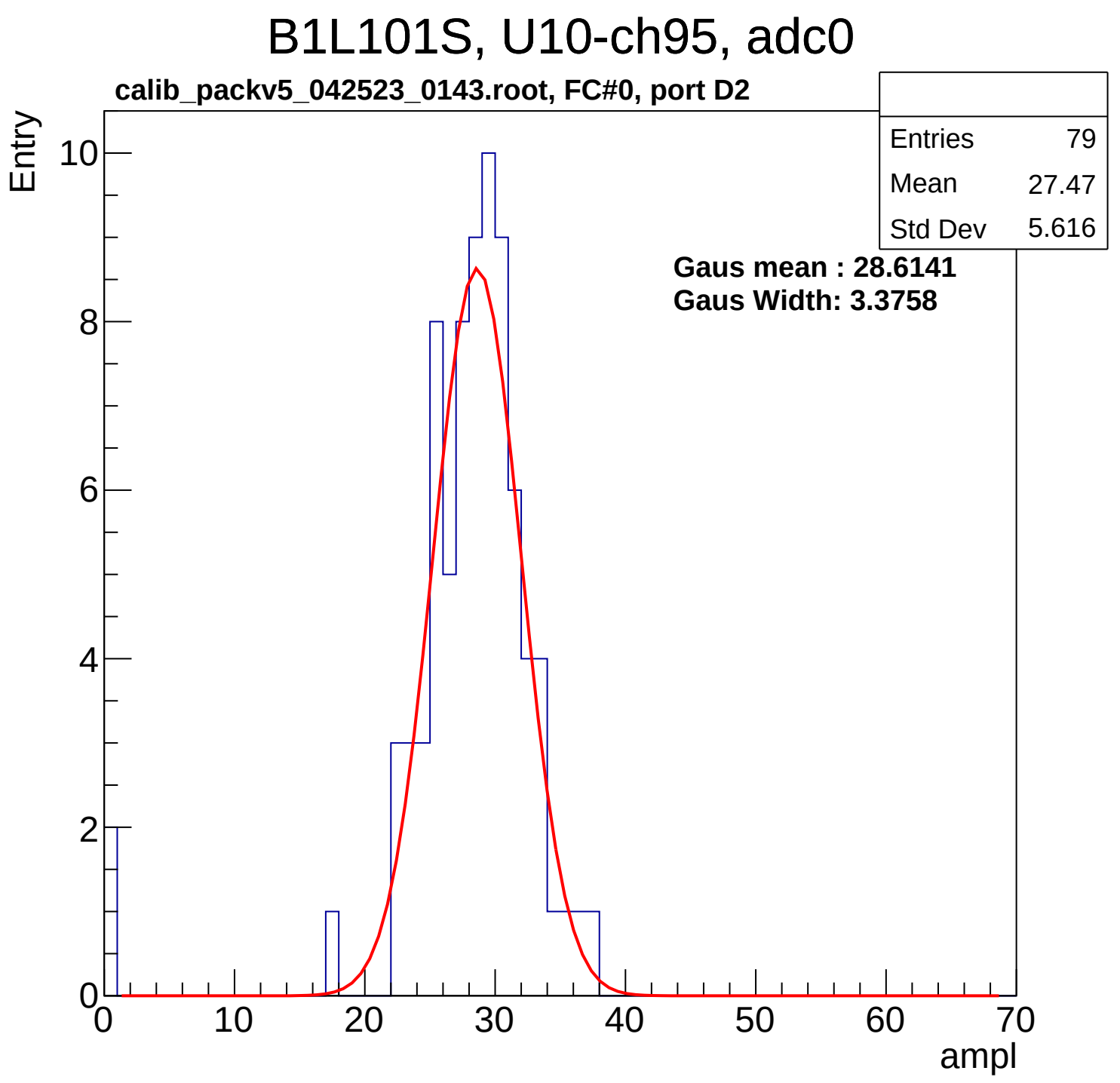
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch95, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 27.47
Std Dev 5.616
Gaus mean : 28.6141
Gaus Width: 3.3758
Entry
ampl
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2
4
6
8
10
0
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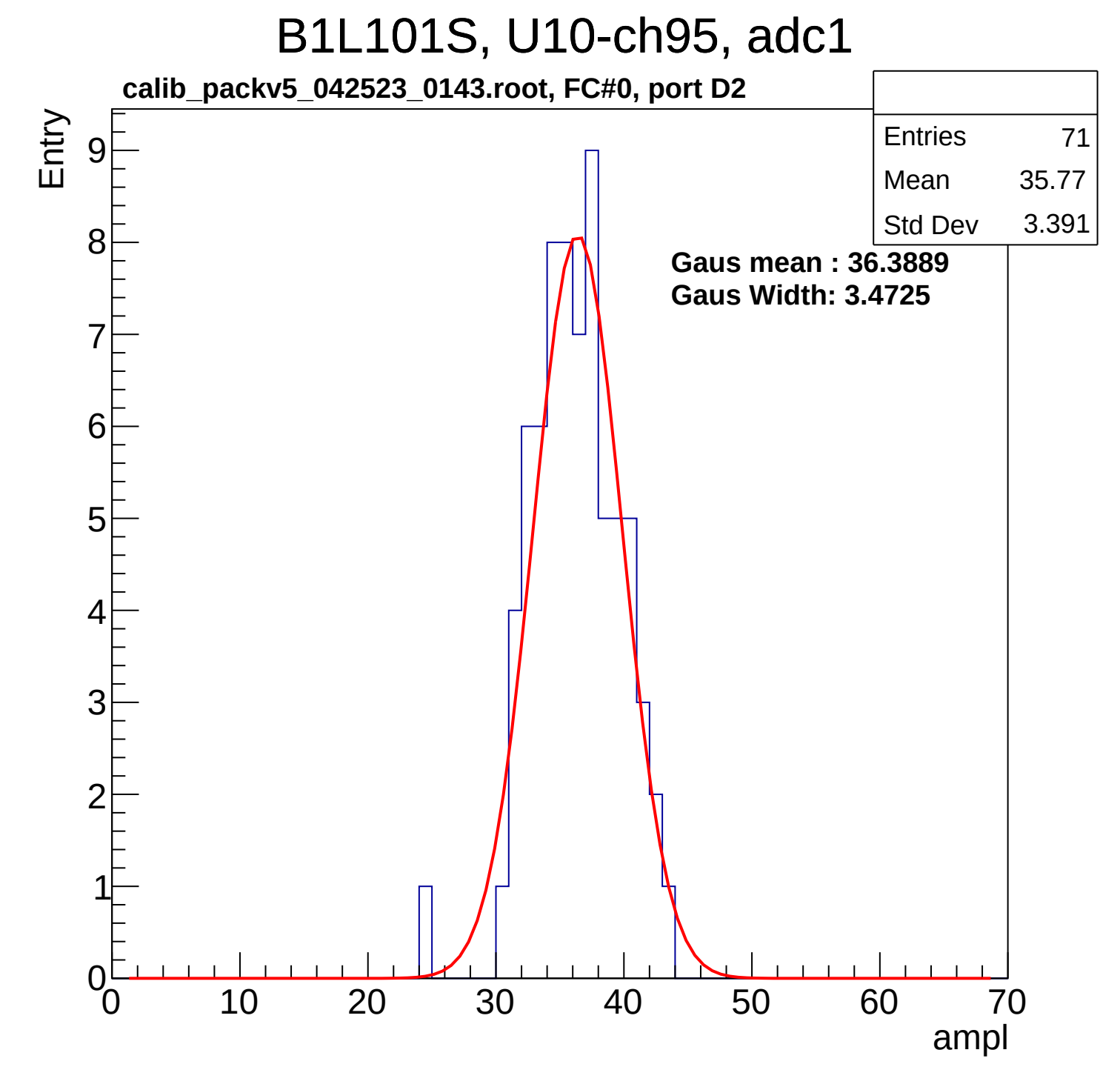
20
30
40
50
60
70


B1L101S, U10-ch95, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 35.77
Std Dev 3.391
Gaus mean : 36.3889
Gaus Width: 3.4725
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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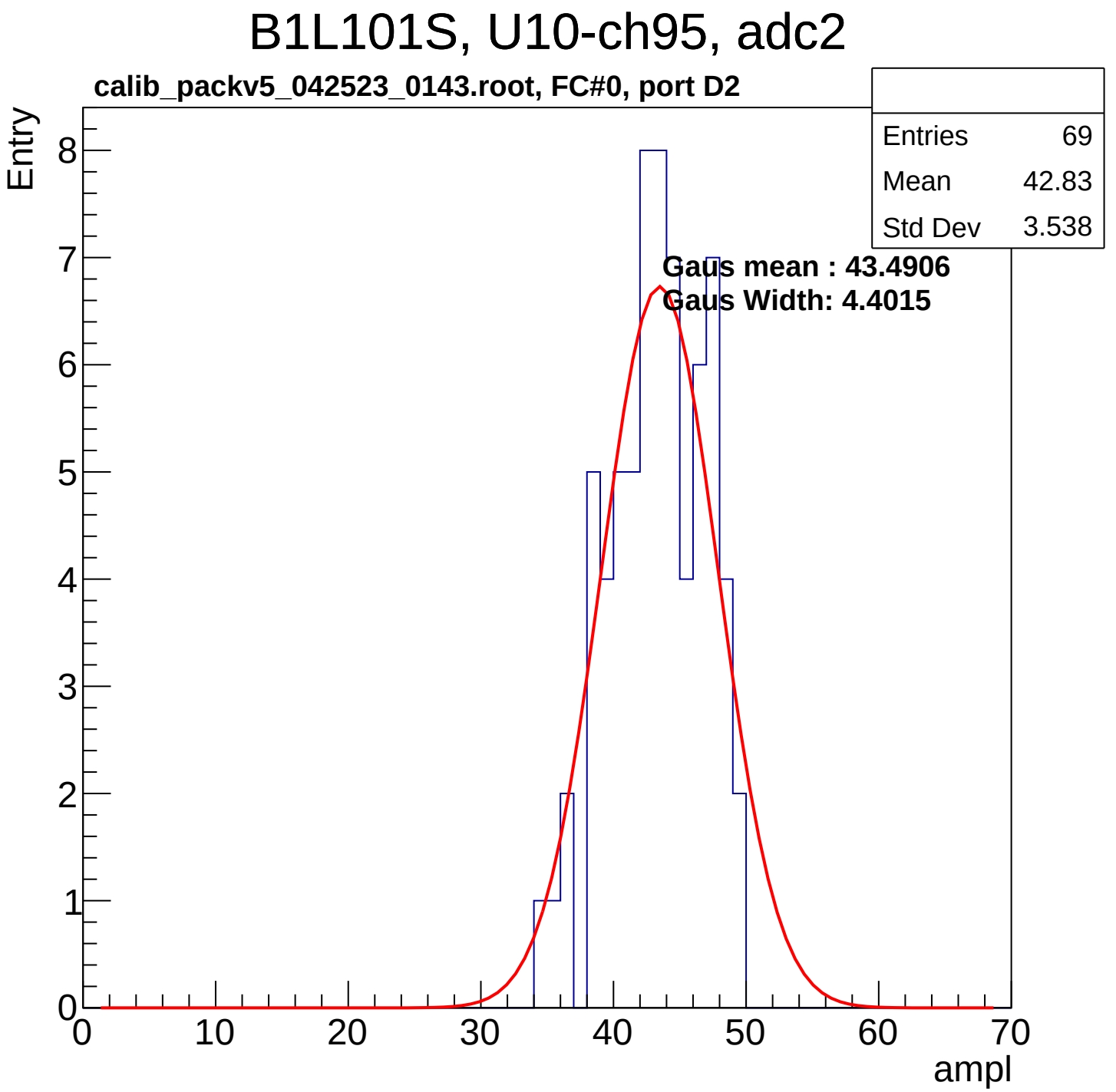
B1L101S, U10-ch95, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 42.83
Std Dev 3.538
Gaus mean : 43.4906
Gaus Width: 4.4015
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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60
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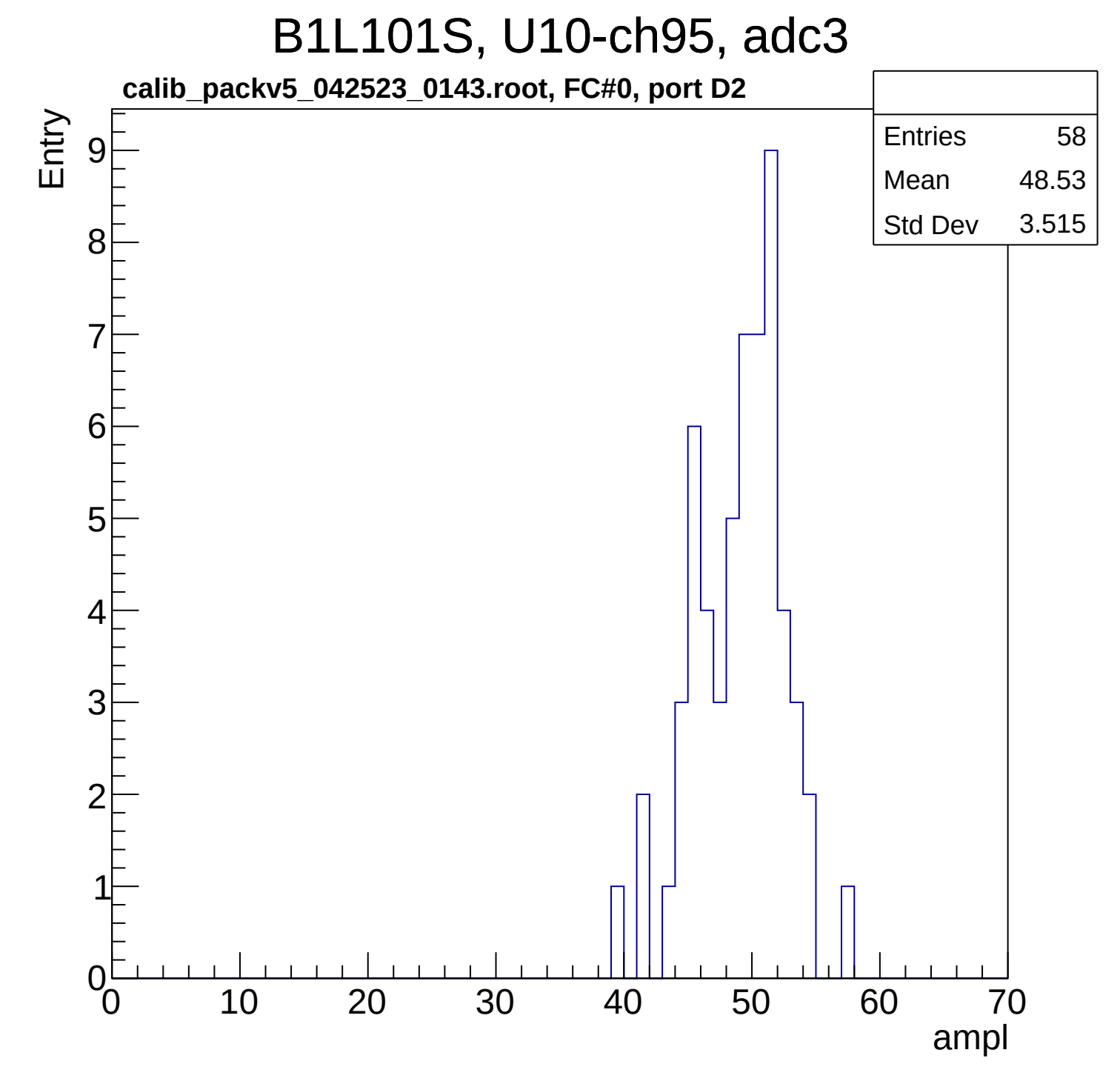
B1L101S, U10-ch95, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 48.53
Std Dev 3.515
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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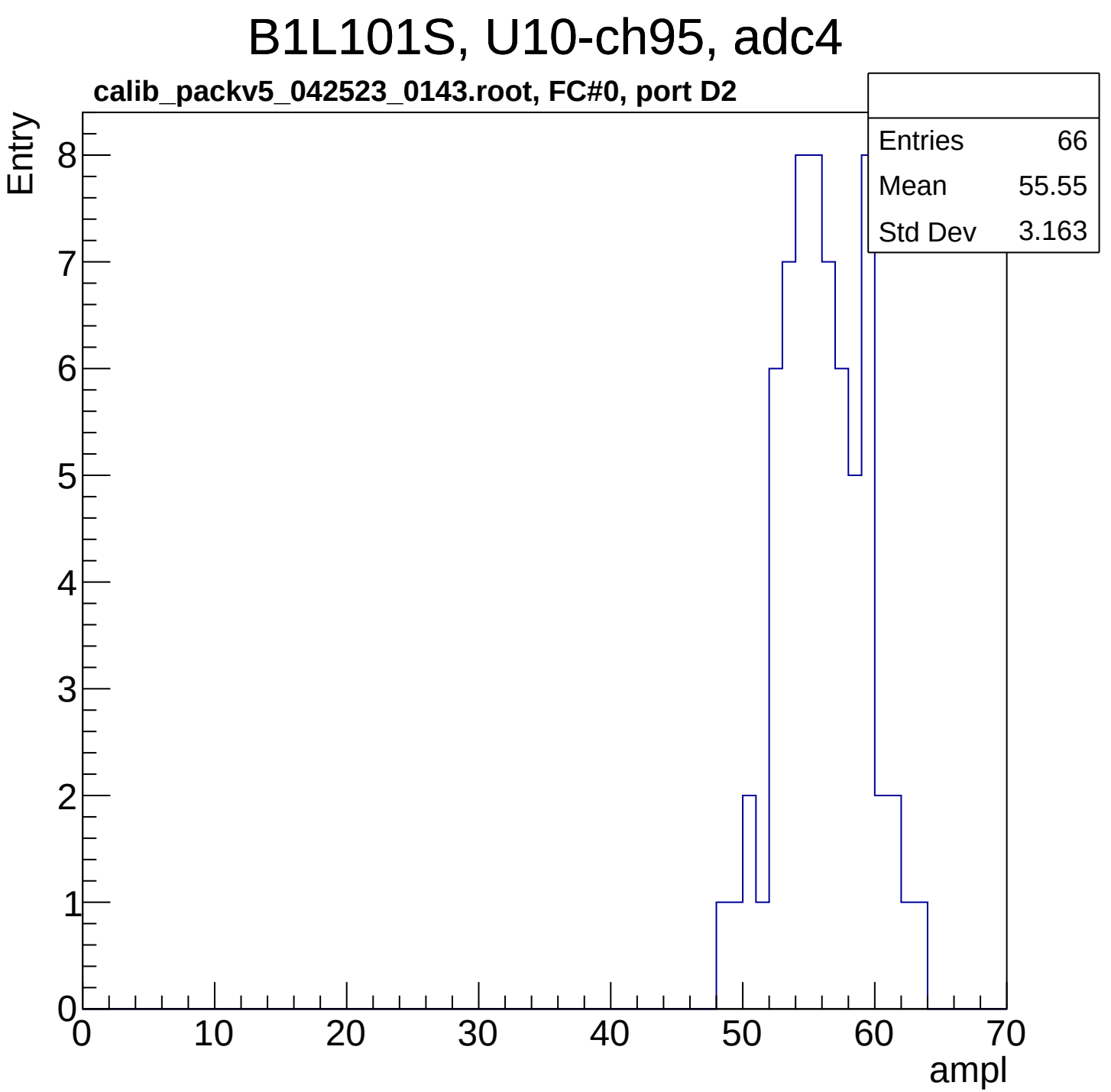
60
70


B1L101S, U10-ch95, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 55.55
Std Dev 3.163
Entry
ampl
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7
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0
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40
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60
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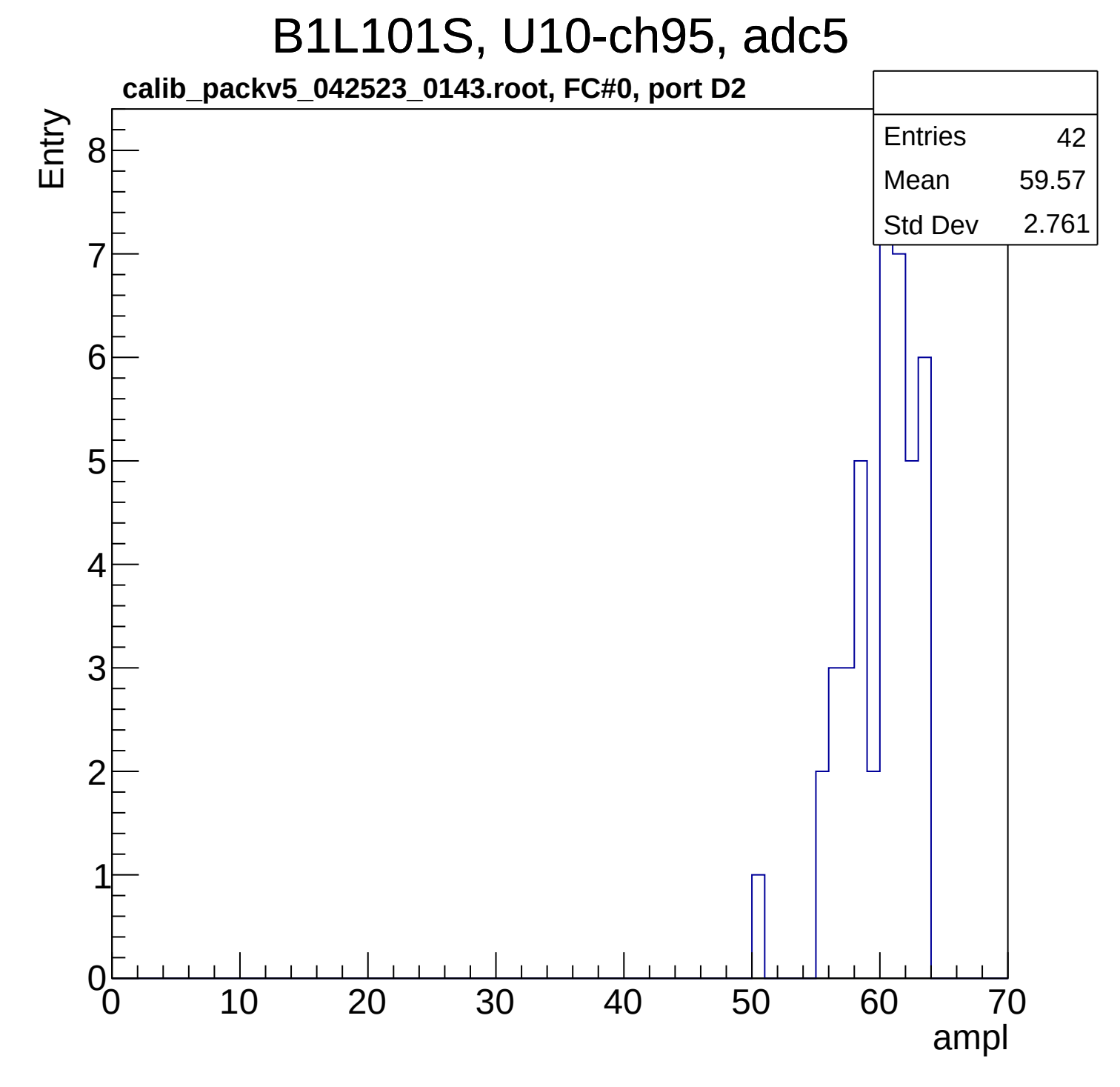
B1L101S, U10-ch95, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 59.57
Std Dev 2.761
Entry
ampl
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2
3
4
5
6
7
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0
10
20
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40
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60
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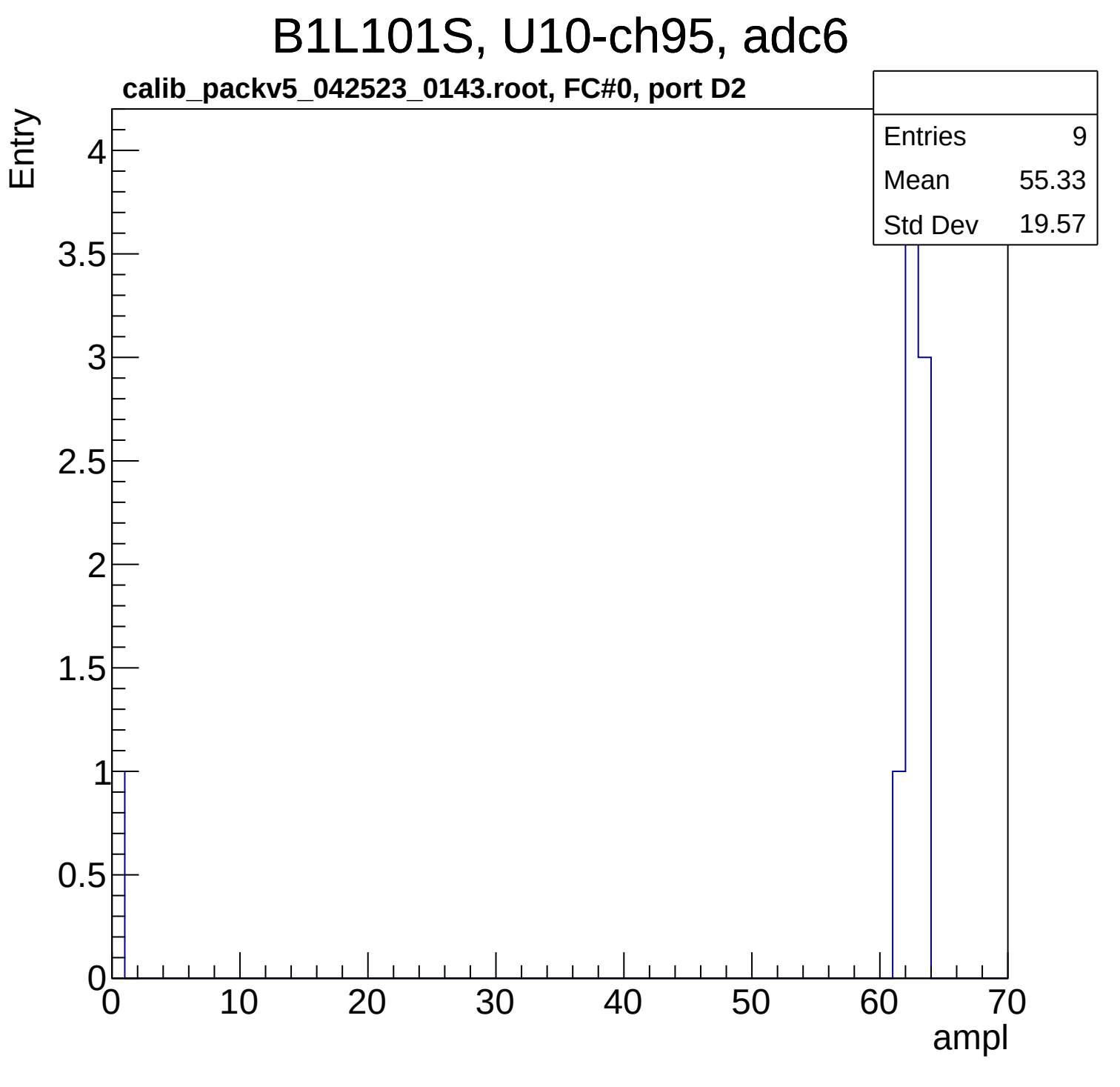
B1L101S, U10-ch95, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 55.33
Std Dev 19.57
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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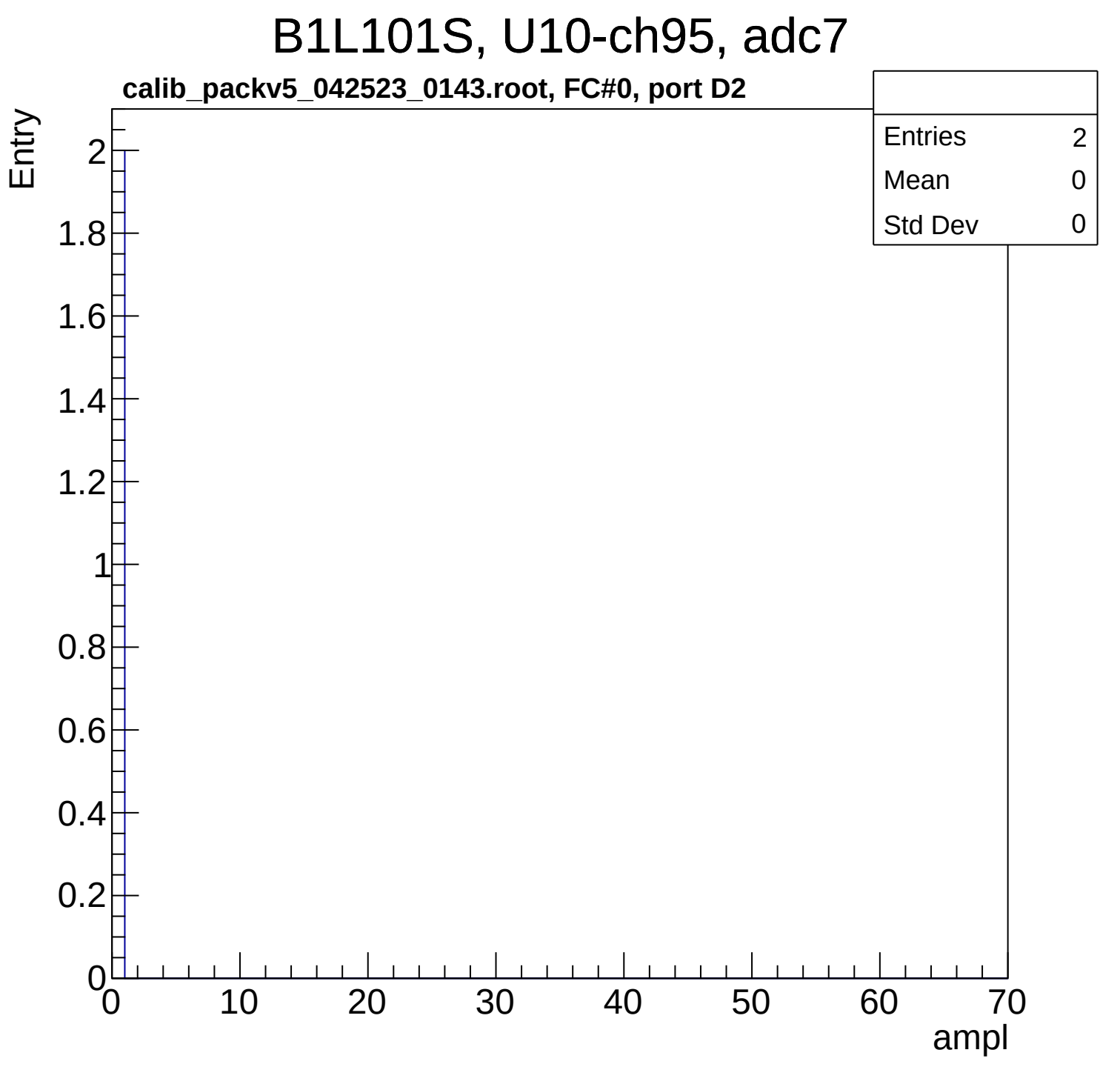
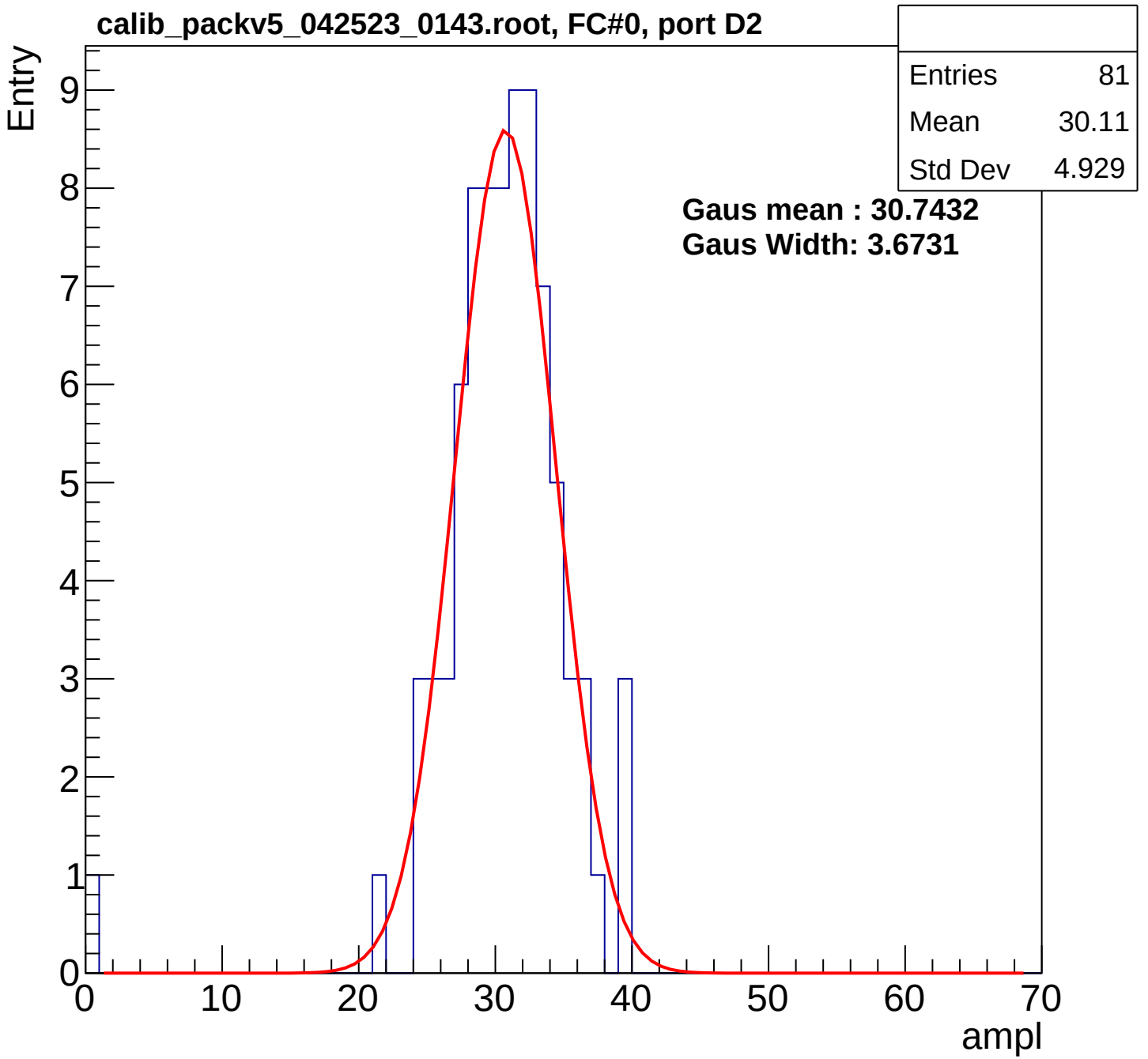

B1L101S, U10-ch95, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch96, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 81
Mean 30.11
Std Dev 4.929
Gaus mean : 30.7432
Gaus Width: 3.6731
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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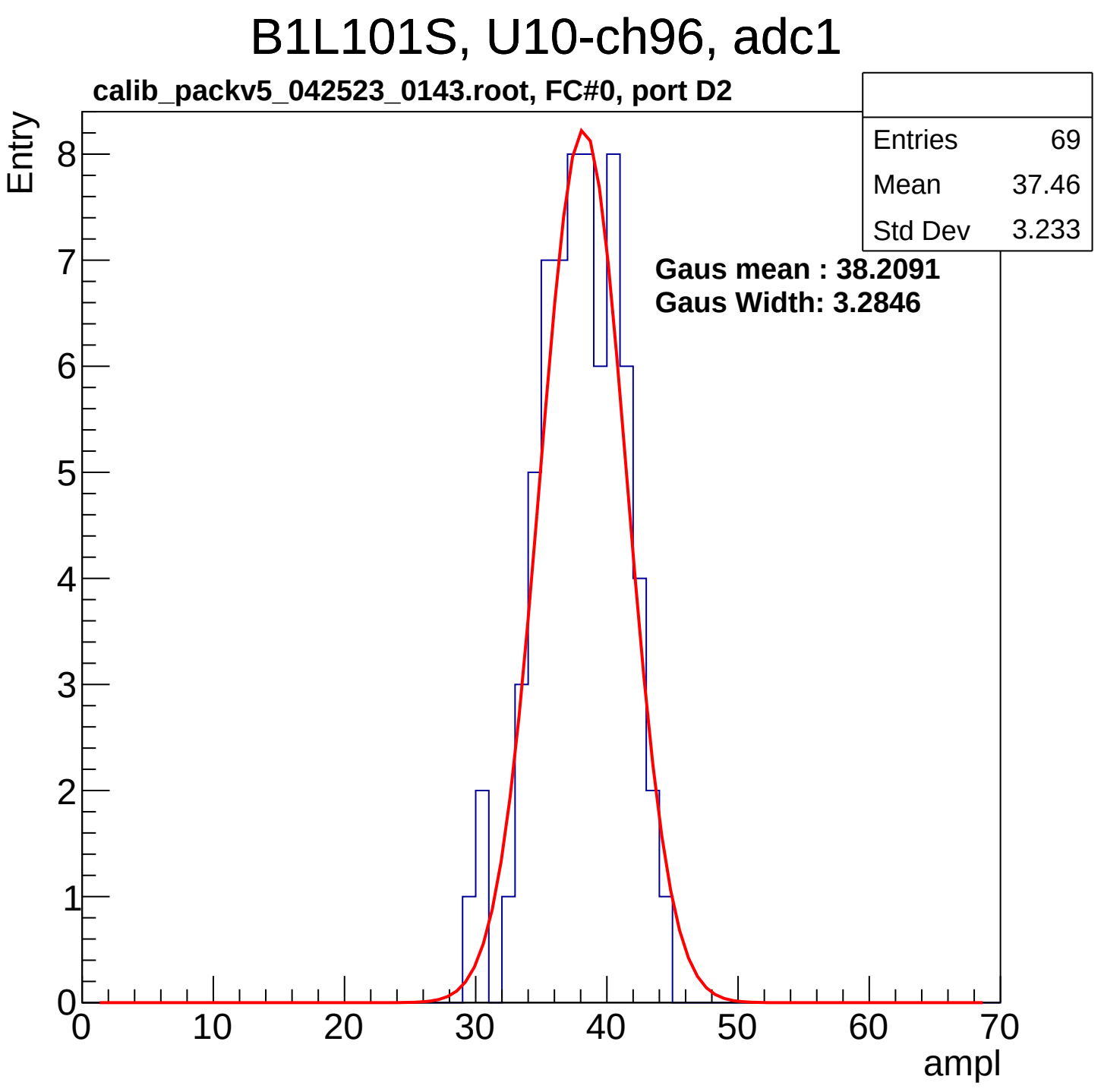
B1L101S, U10-ch96, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 37.46
Std Dev 3.233
Gaus mean : 38.2091
Gaus Width: 3.2846
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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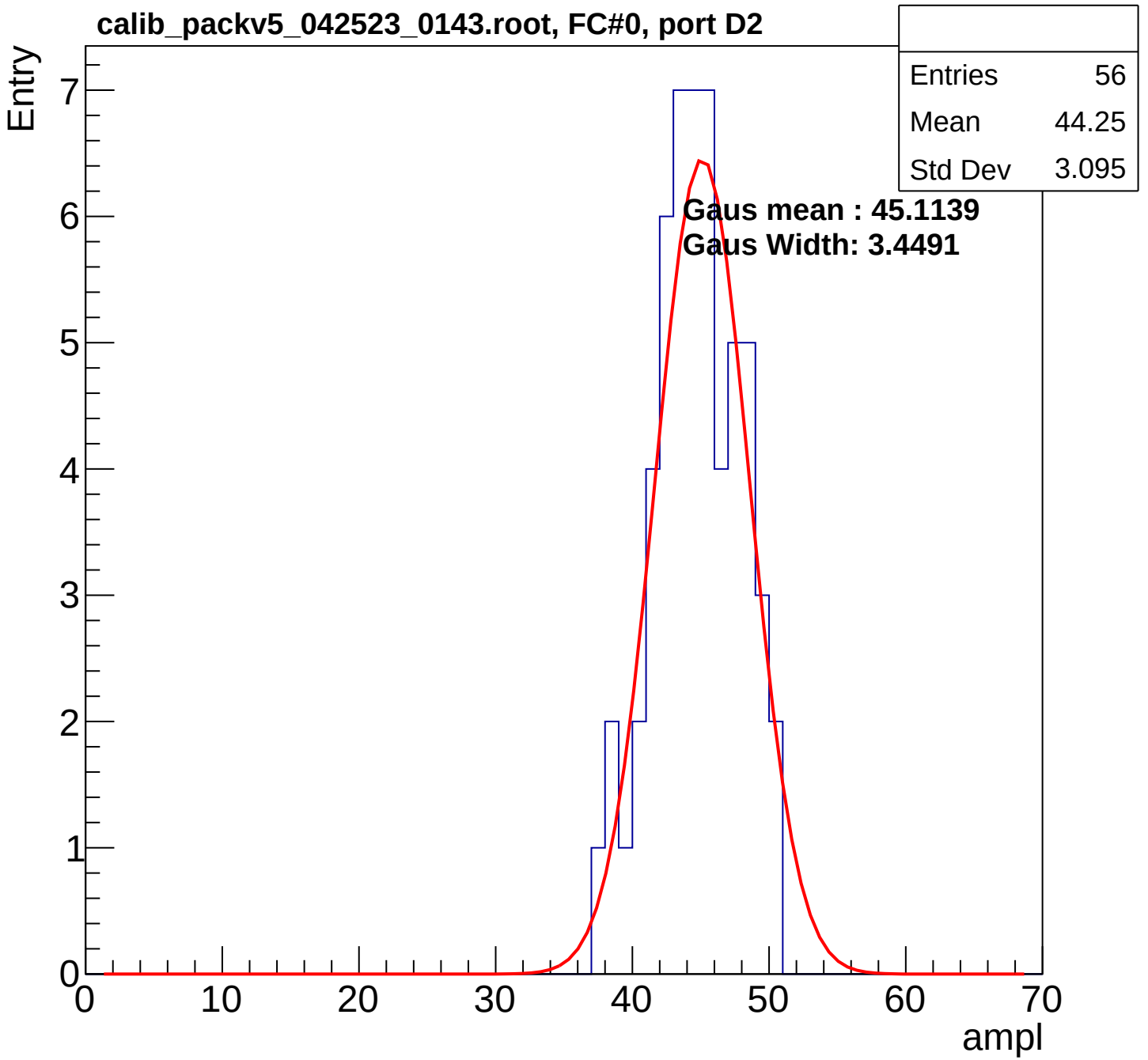
B1L101S, U10-ch96, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 44.25
Std Dev 3.095
Gaus mean : 45.1139
Gaus Width: 3.4491
Entry
ampl
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3
4
5
6
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0
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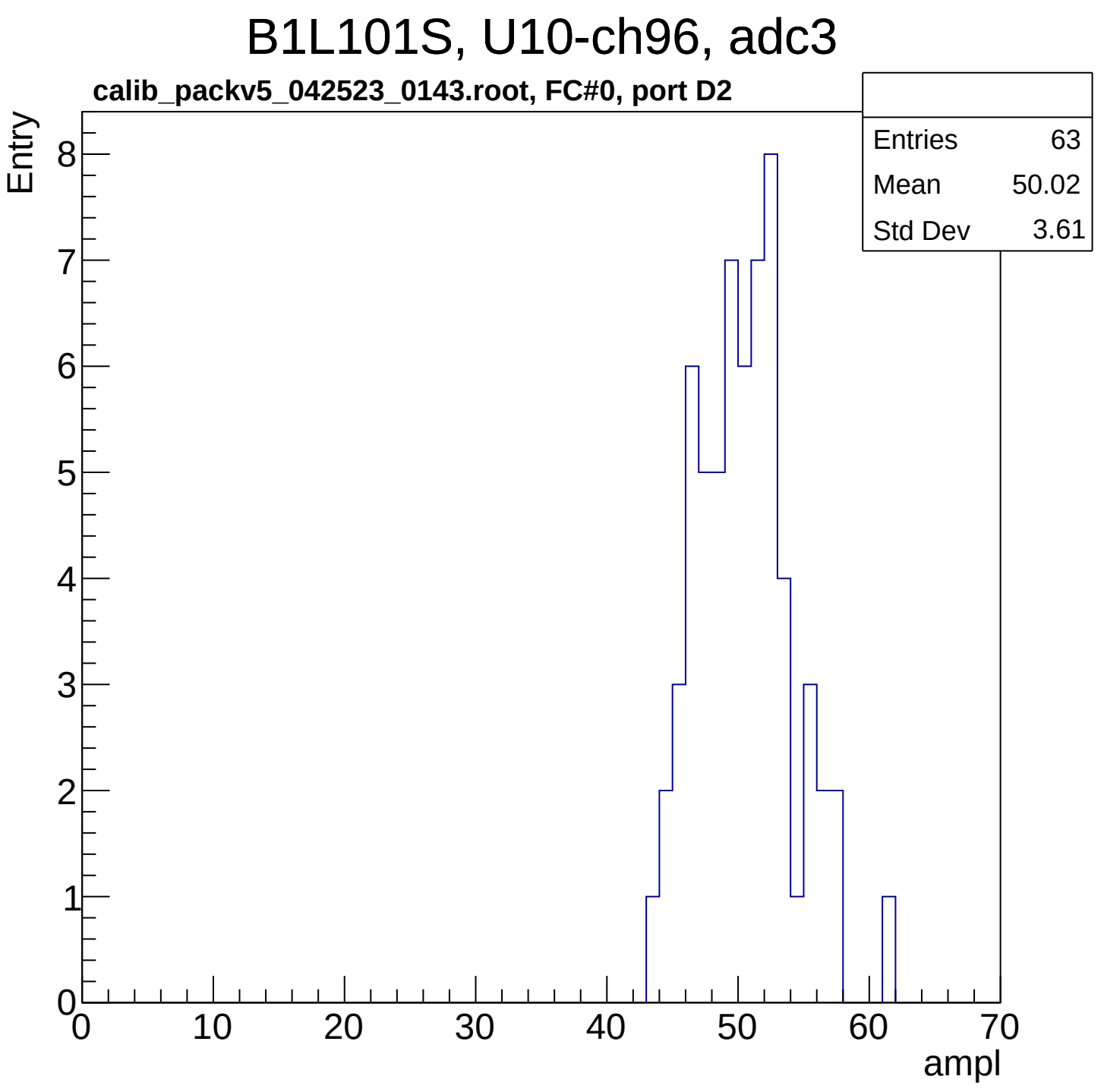
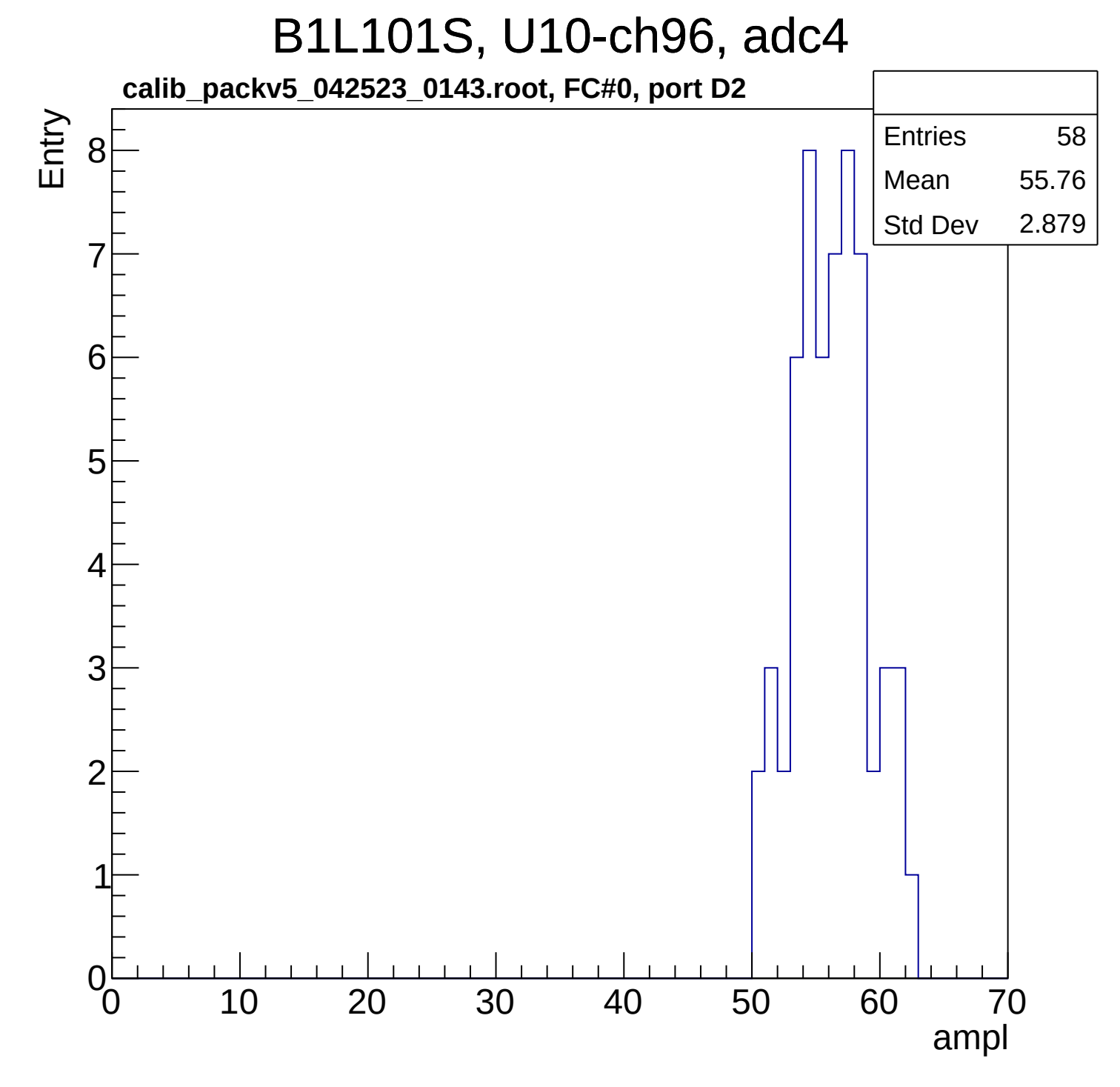

B1L101S, U10-ch96, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 50.02
Std Dev 3.61
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch96, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 55.76
Std Dev 2.879
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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40
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60
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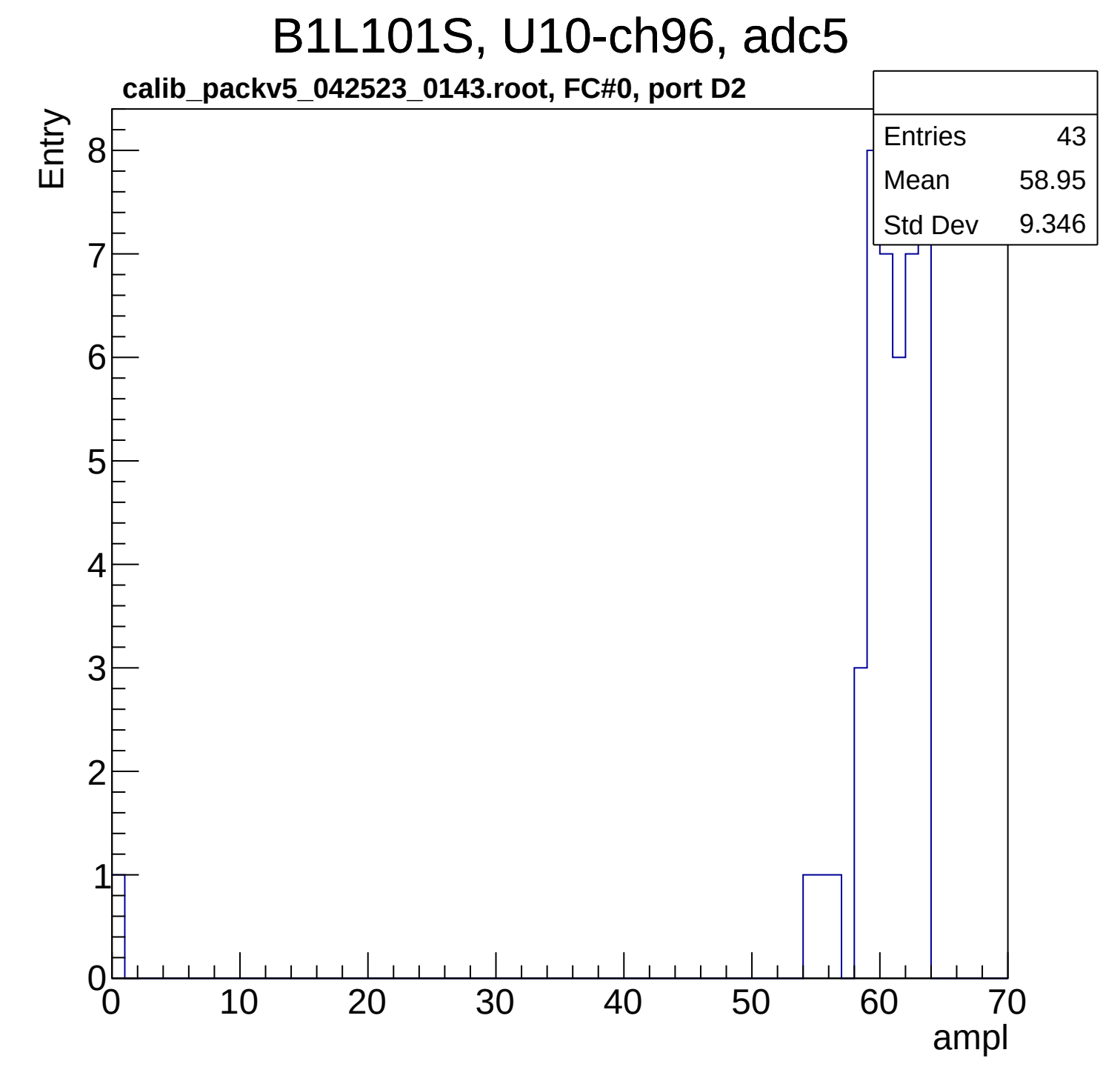
B1L101S, U10-ch96, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 43
Mean 58.95
Std Dev 9.346
Entry
ampl
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1
2
3
4
5
6
7
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0
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60
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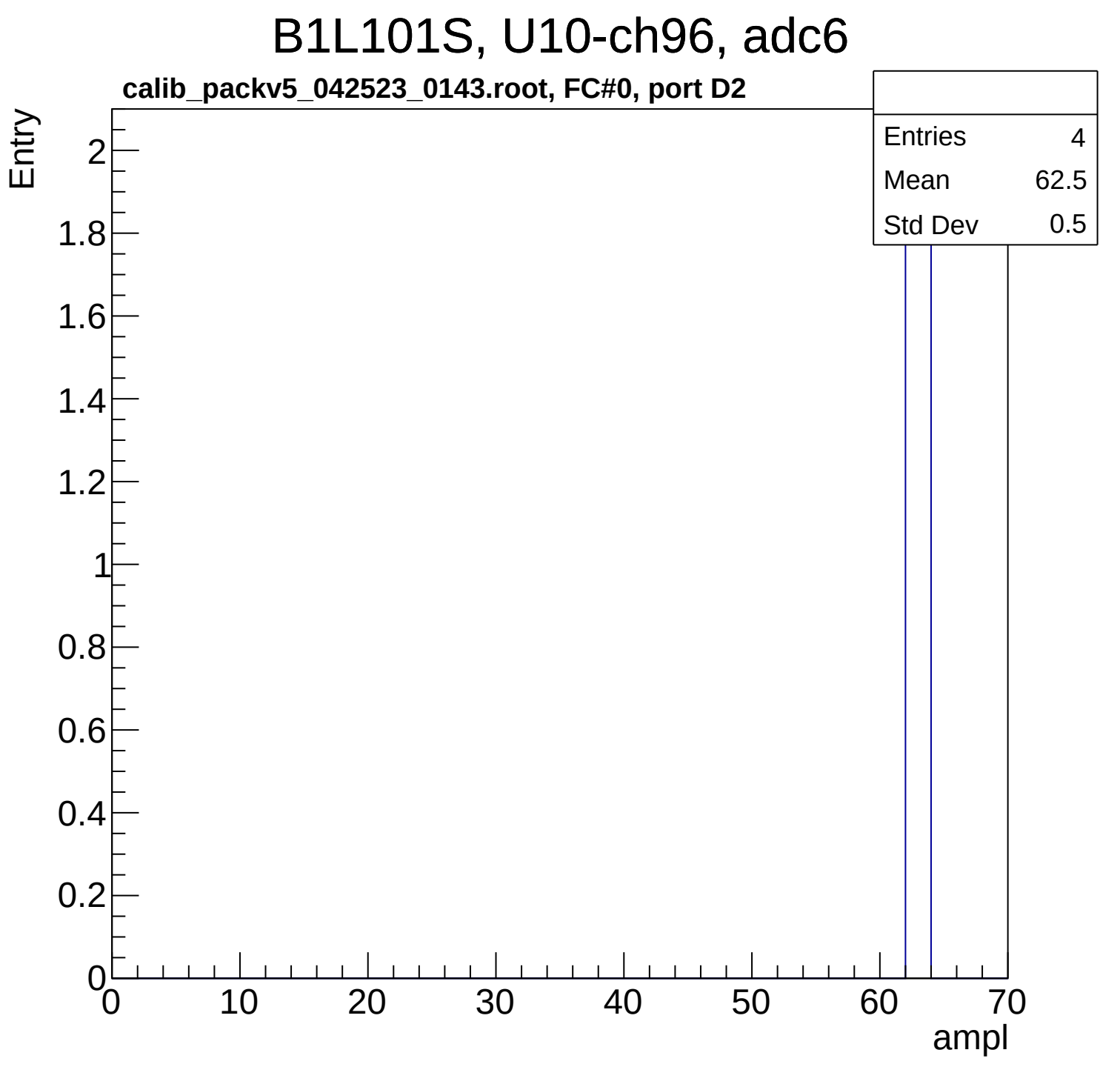
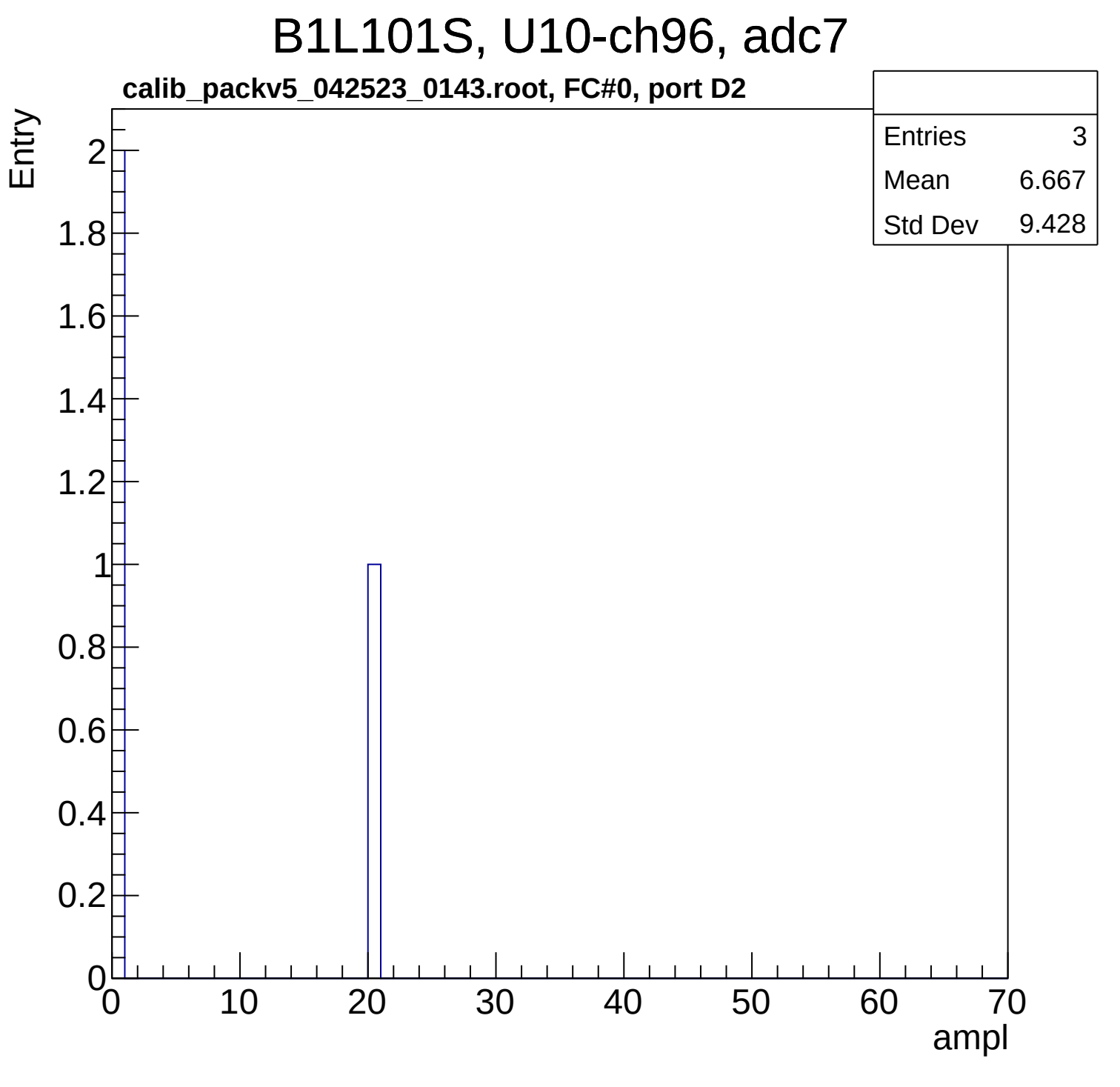

B1L101S, U10-ch96, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 62.5
Std Dev 0.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U10-ch96, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 6.667
Std Dev 9.428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
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60
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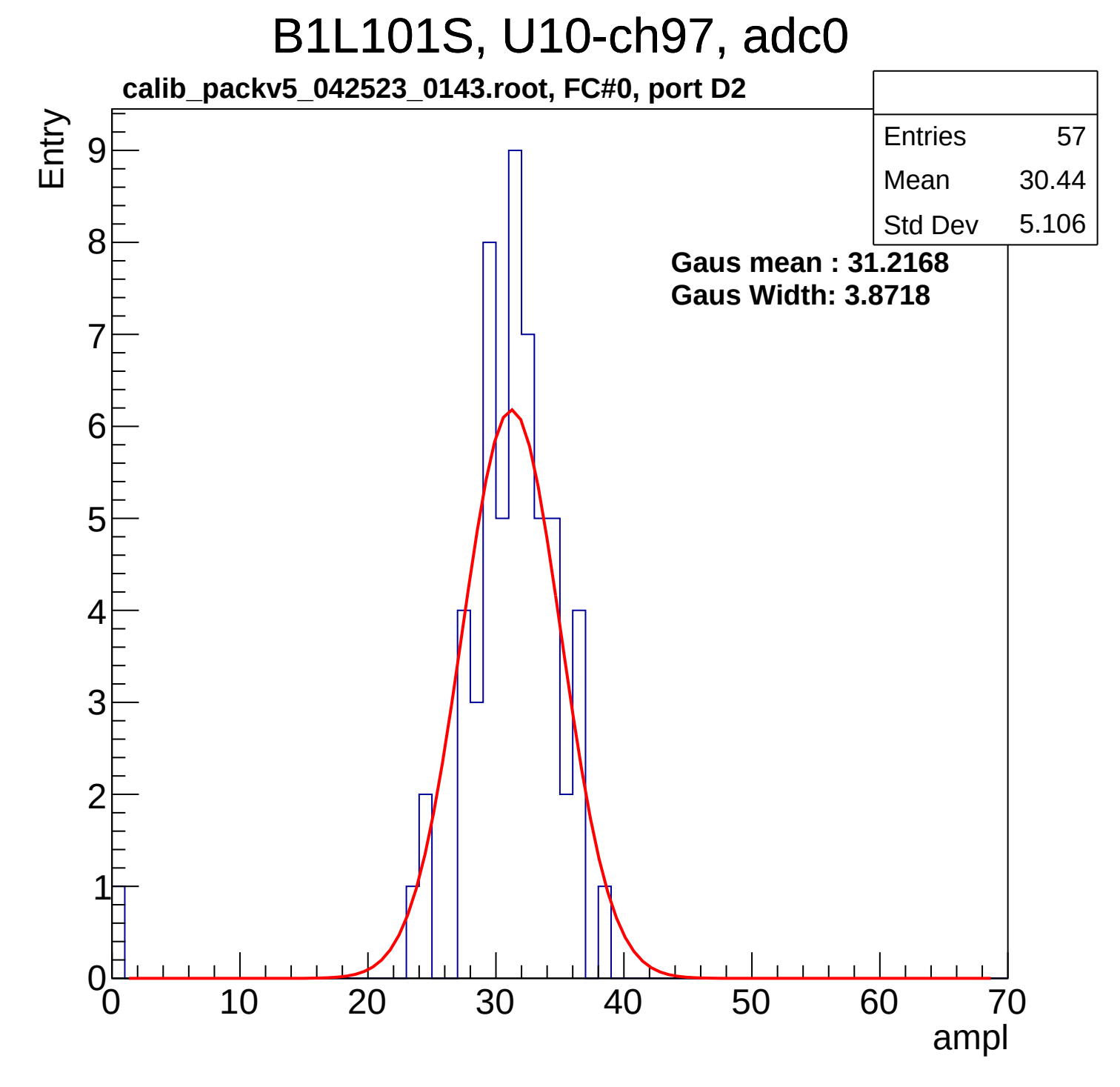
B1L101S, U10-ch97, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 30.44
Std Dev 5.106
Gaus mean : 31.2168
Gaus Width: 3.8718
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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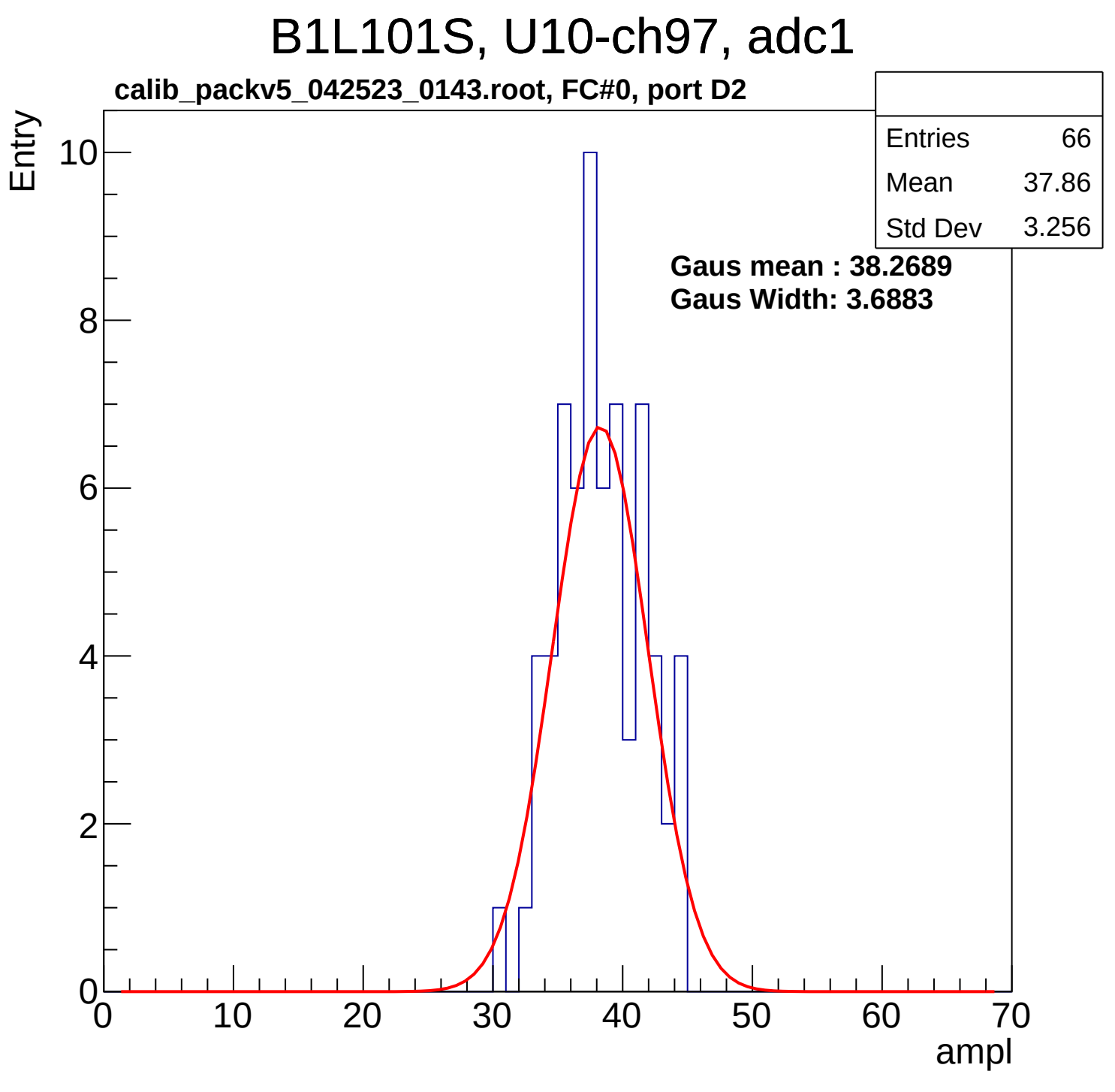
B1L101S, U10-ch97, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 37.86
Std Dev 3.256
Gaus mean : 38.2689
Gaus Width: 3.6883
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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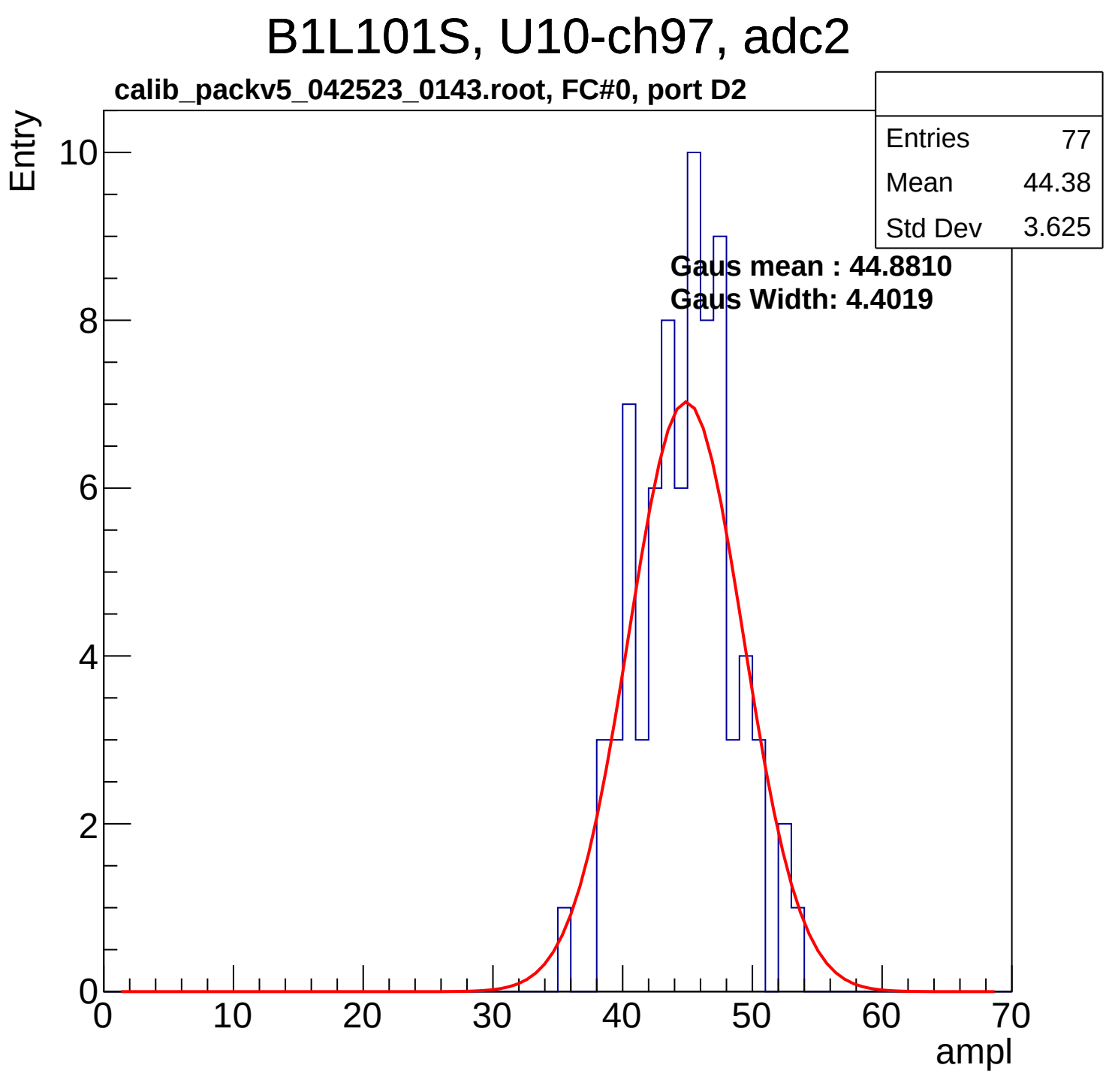
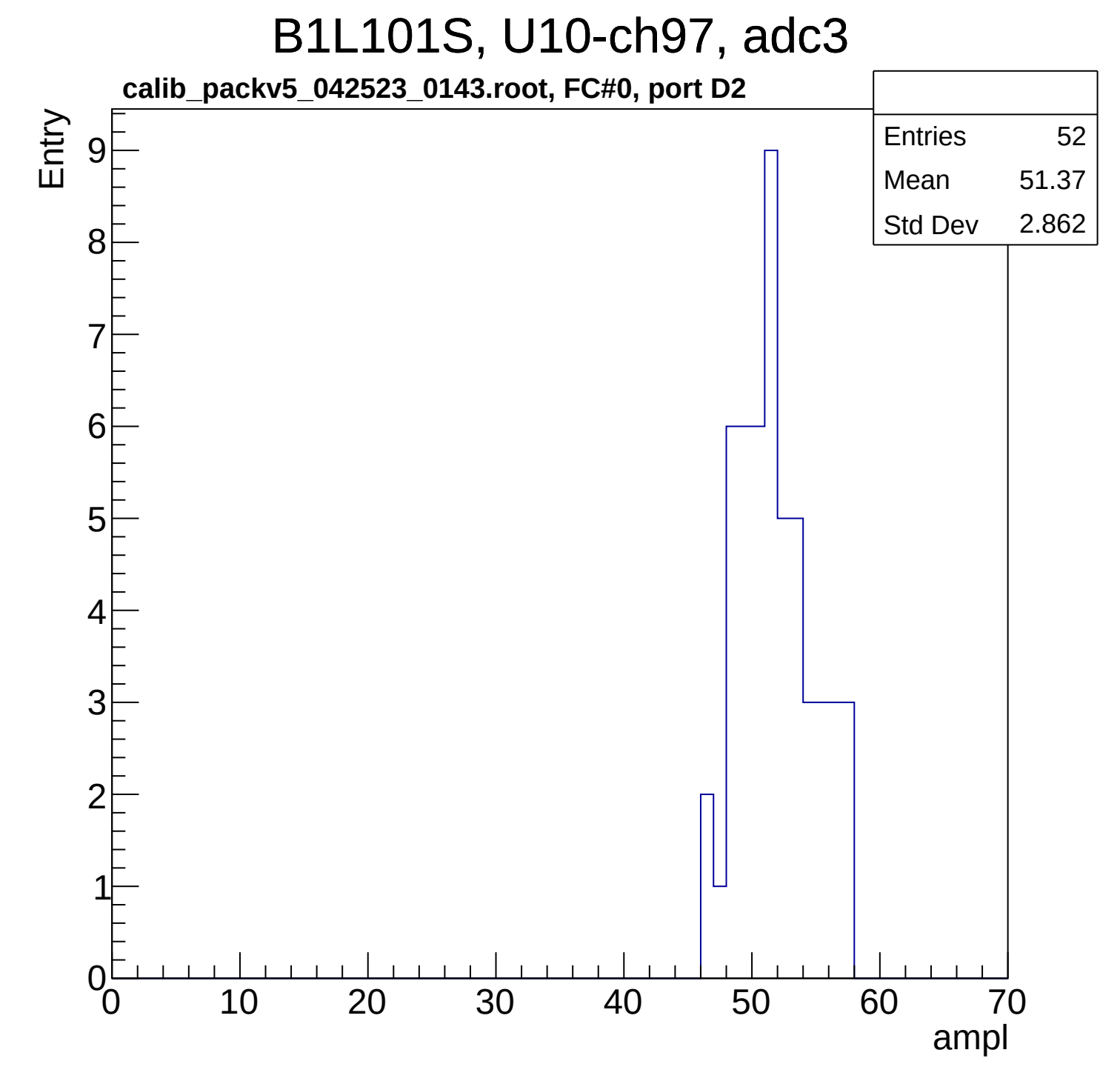

B1L101S, U10-ch97, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 44.38
Std Dev 3.625
Gaus mean : 44.8810
Gaus Width: 4.4019
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch97, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 51.37
Std Dev 2.862
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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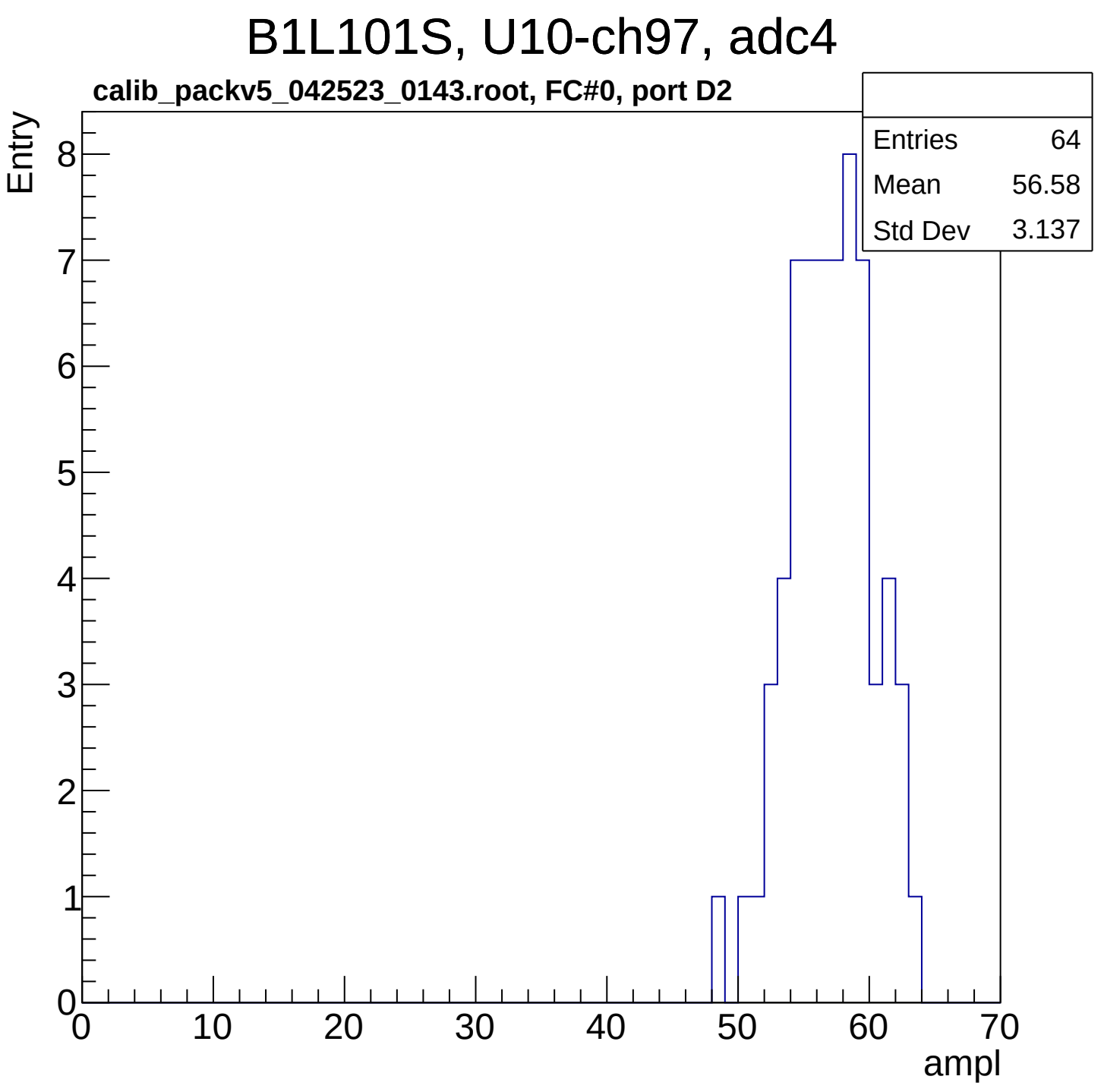
B1L101S, U10-ch97, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 56.58
Std Dev 3.137
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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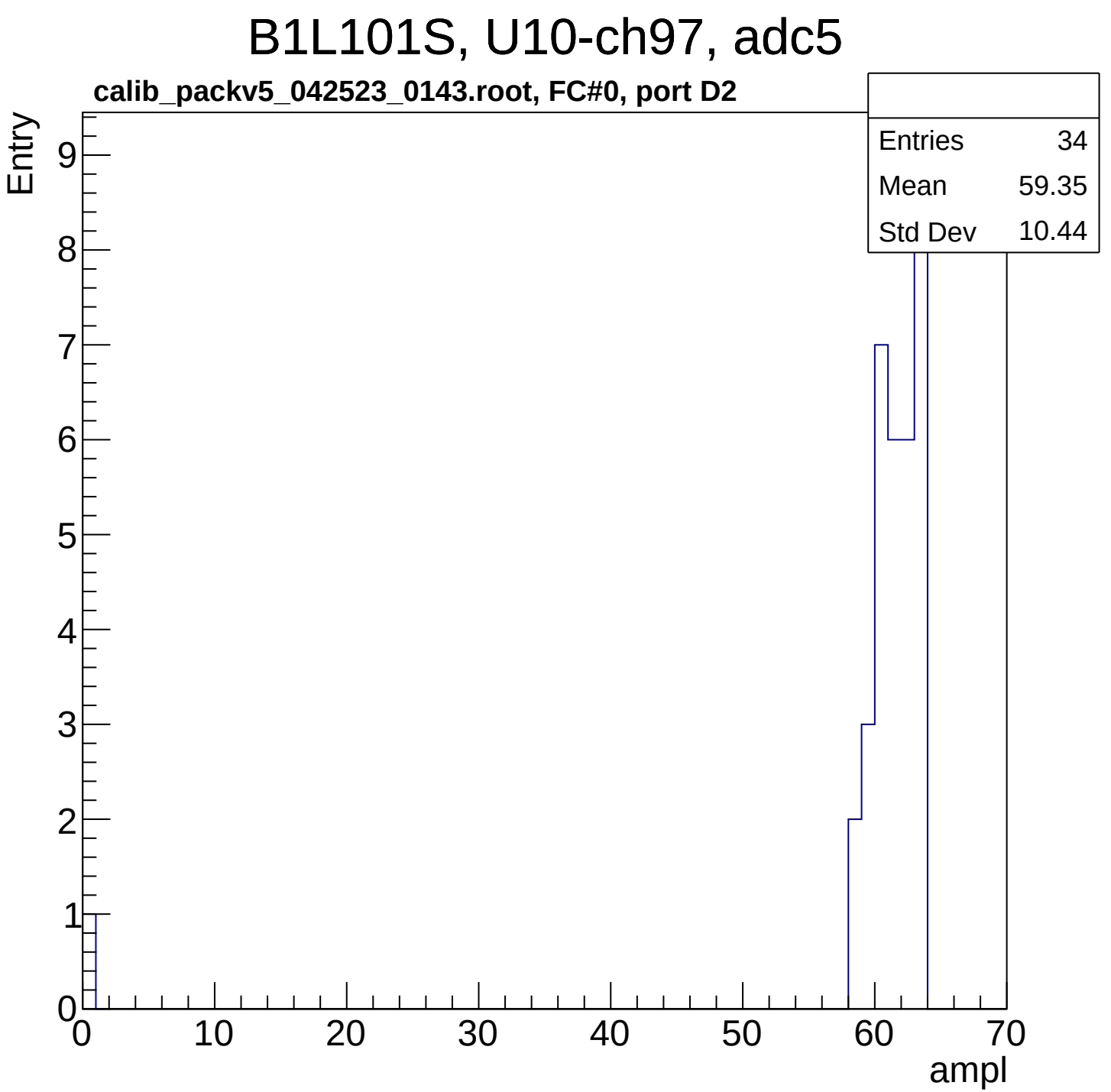
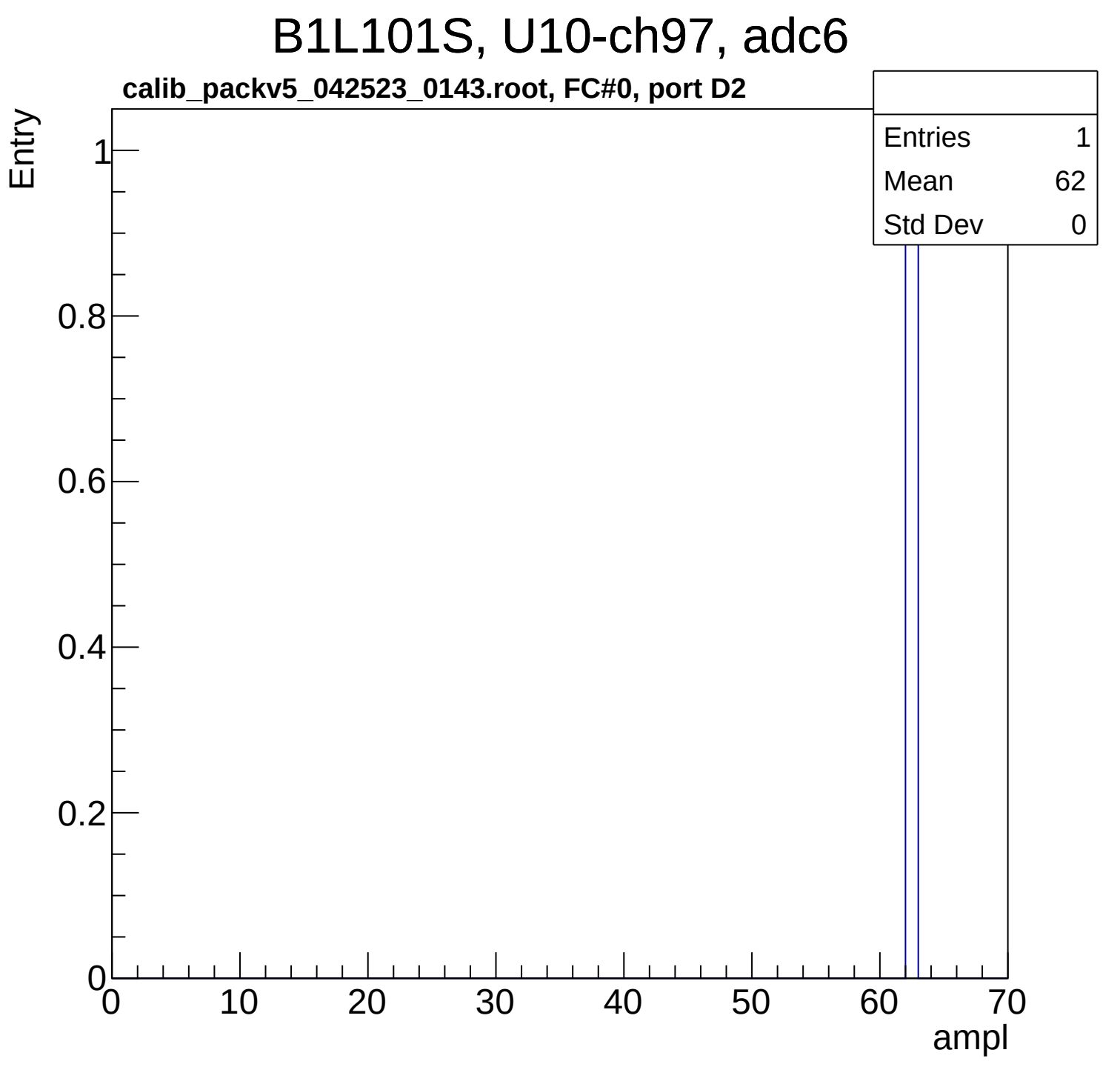
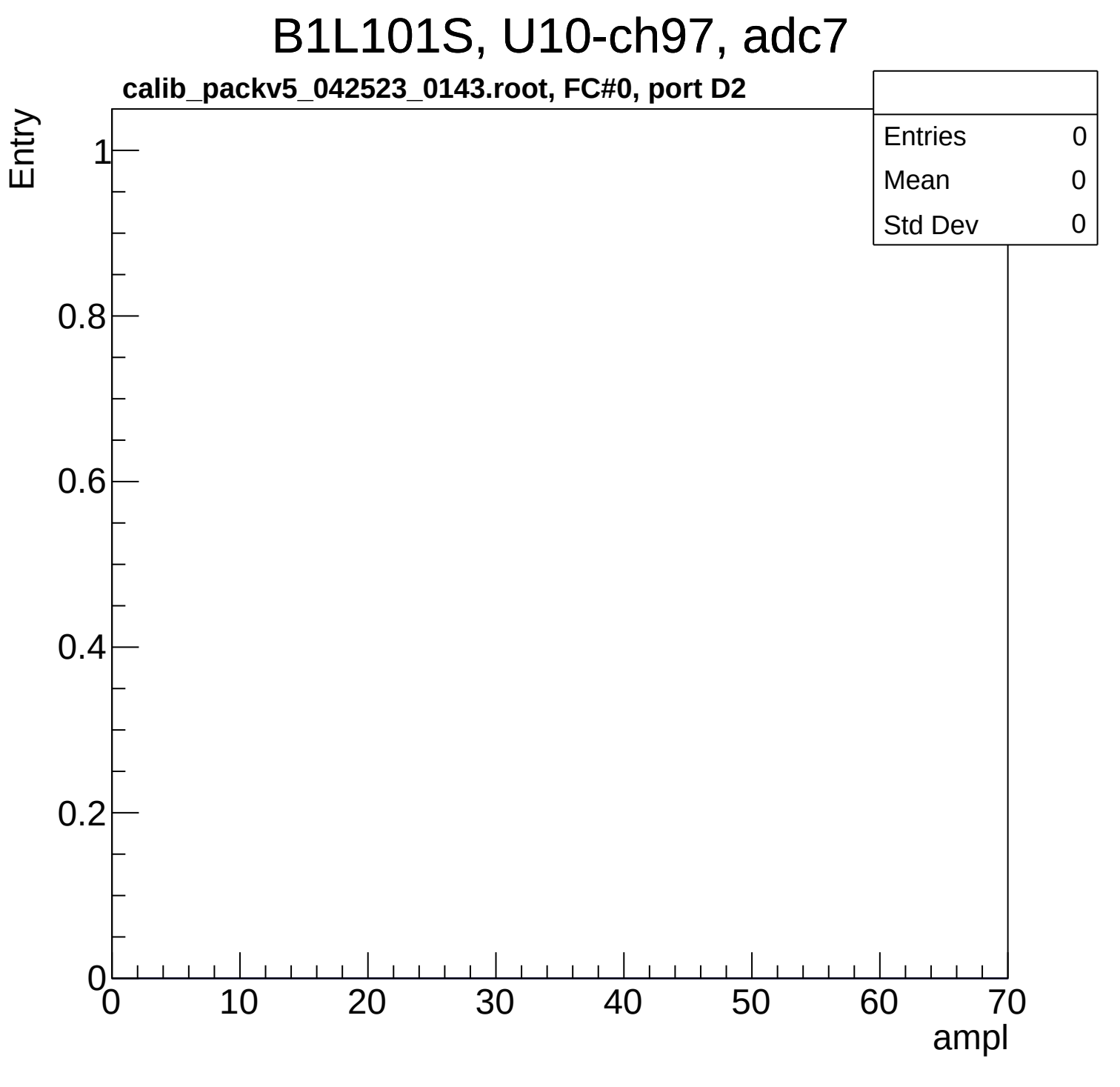
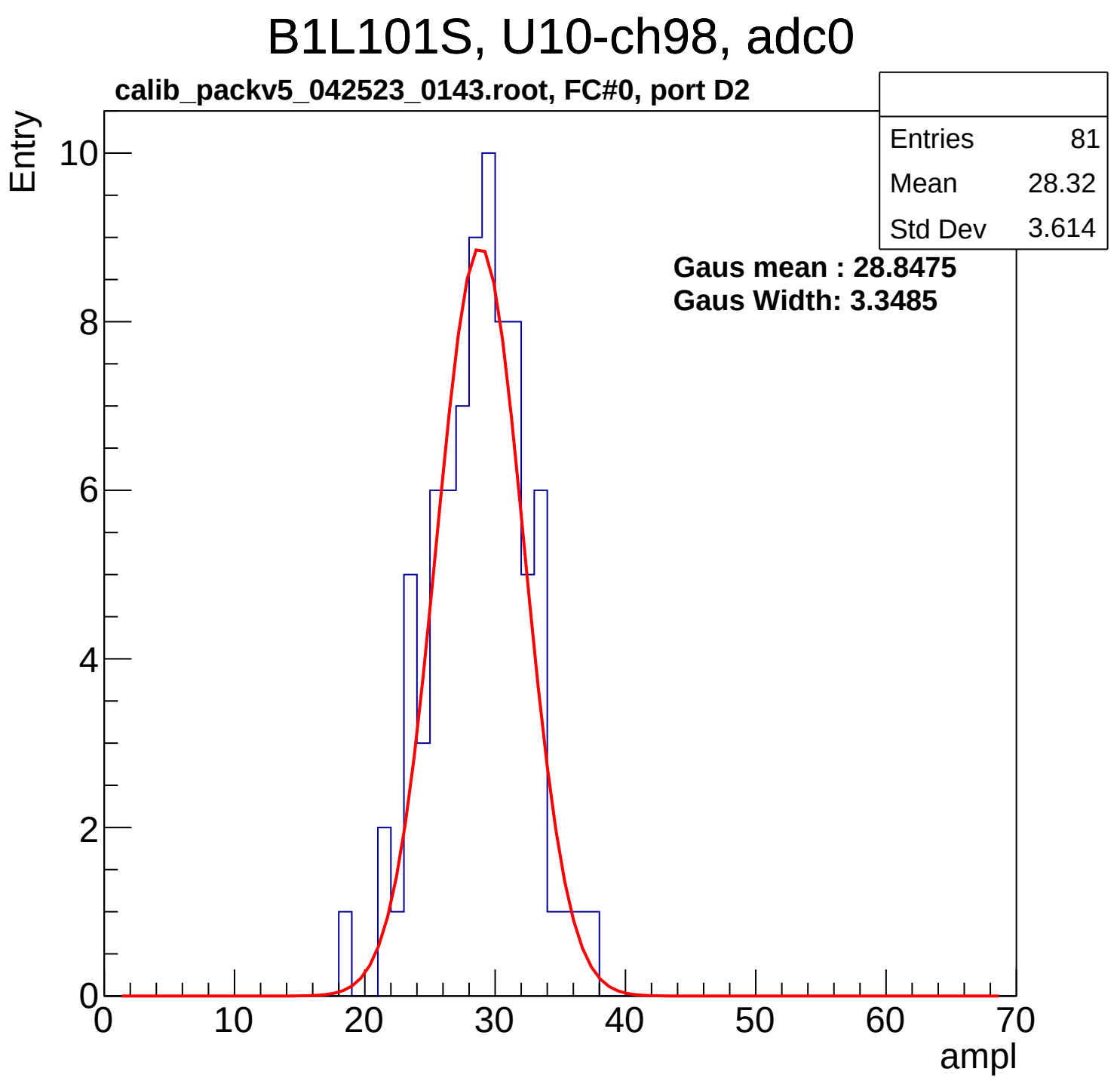
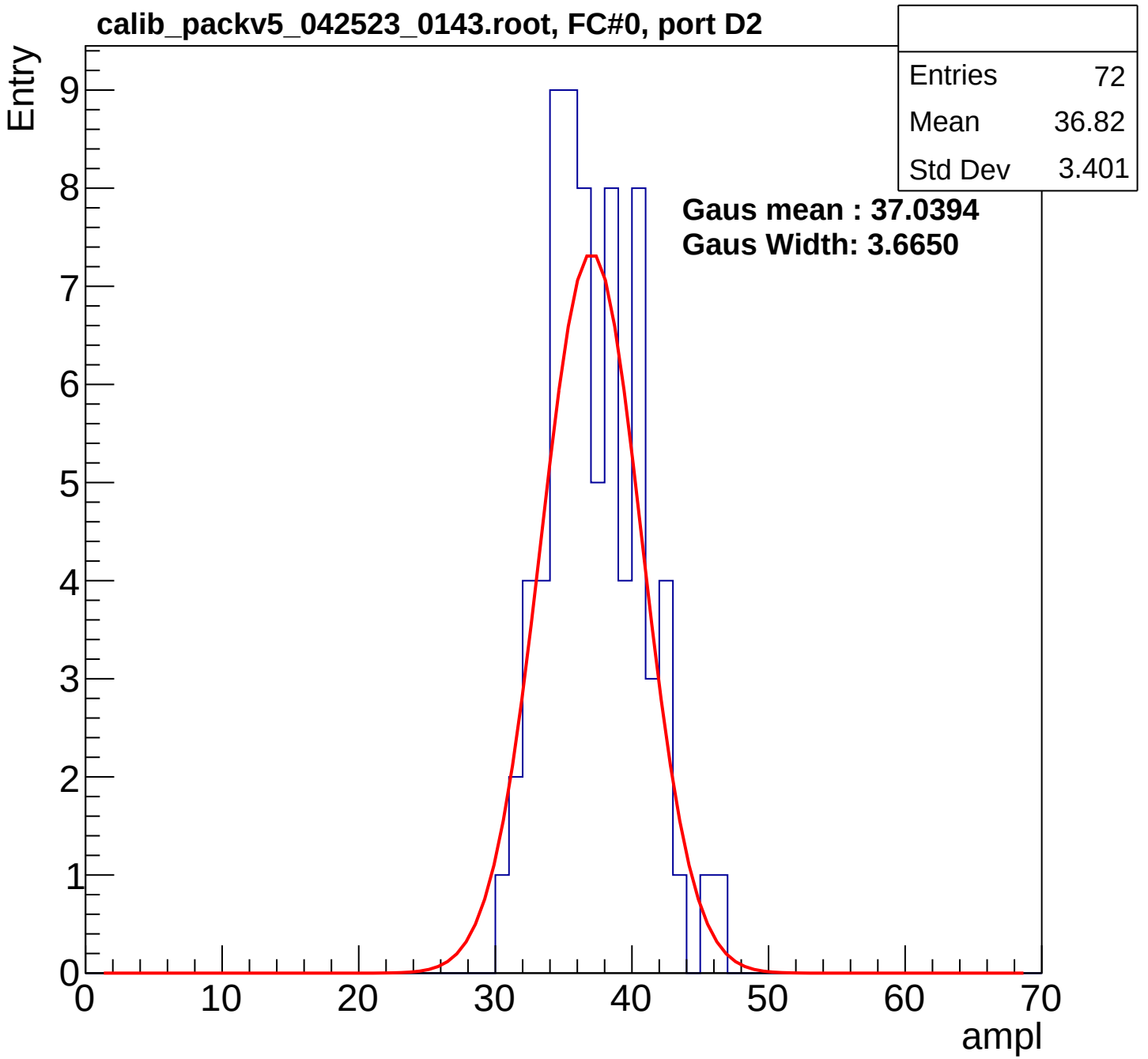
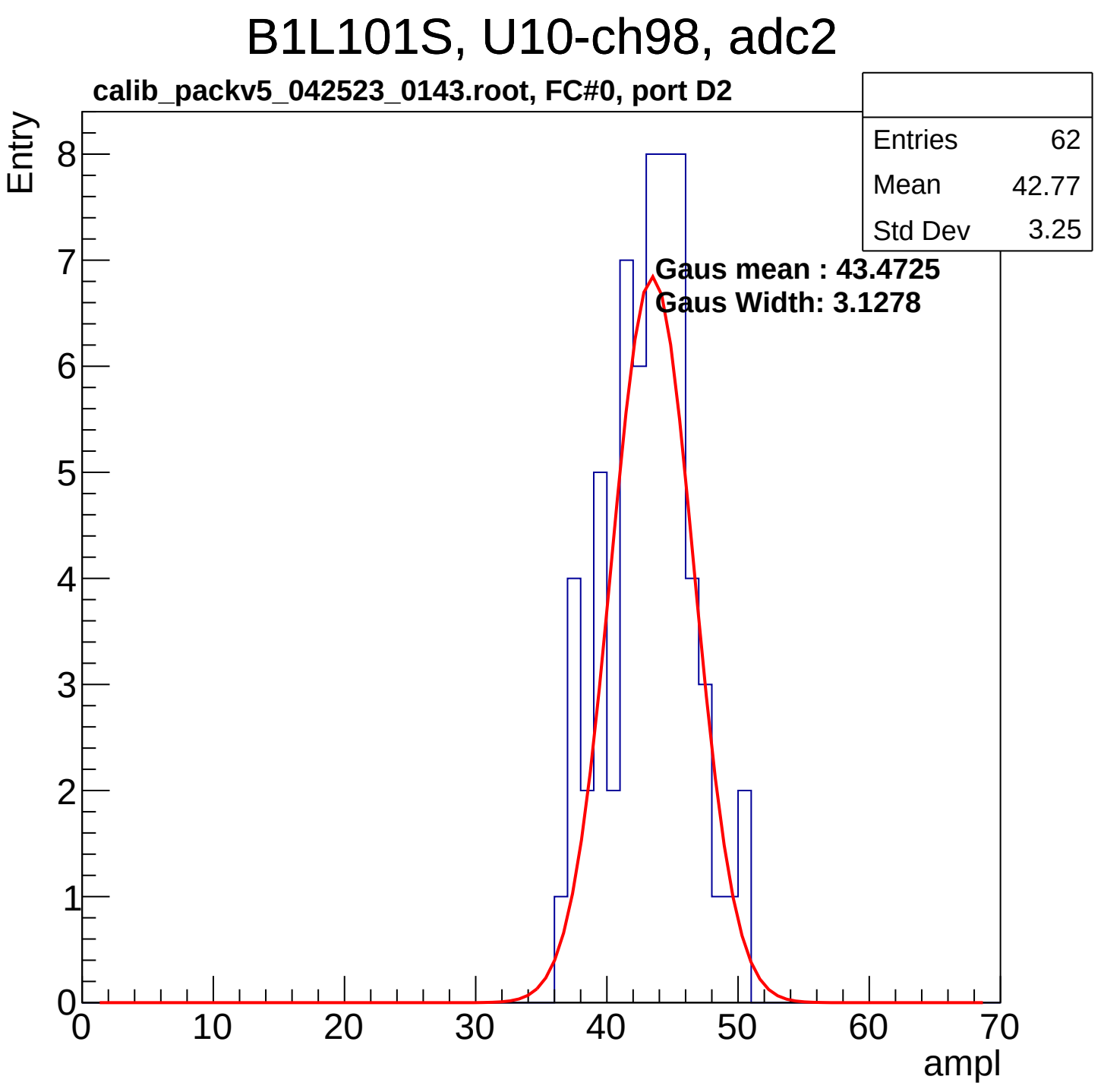

B1L101S, U10-ch97, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 34
Mean 59.35
Std Dev 10.44
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch97, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch97, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch98, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 81
Mean 28.32
Std Dev 3.614
Gaus mean : 28.8475
Gaus Width: 3.3485
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch98, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 36.82
Std Dev 3.401
Gaus mean : 37.0394
Gaus Width: 3.6650
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch98, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 42.77
Std Dev 3.25
Gaus mean : 43.4725
Gaus Width: 3.1278
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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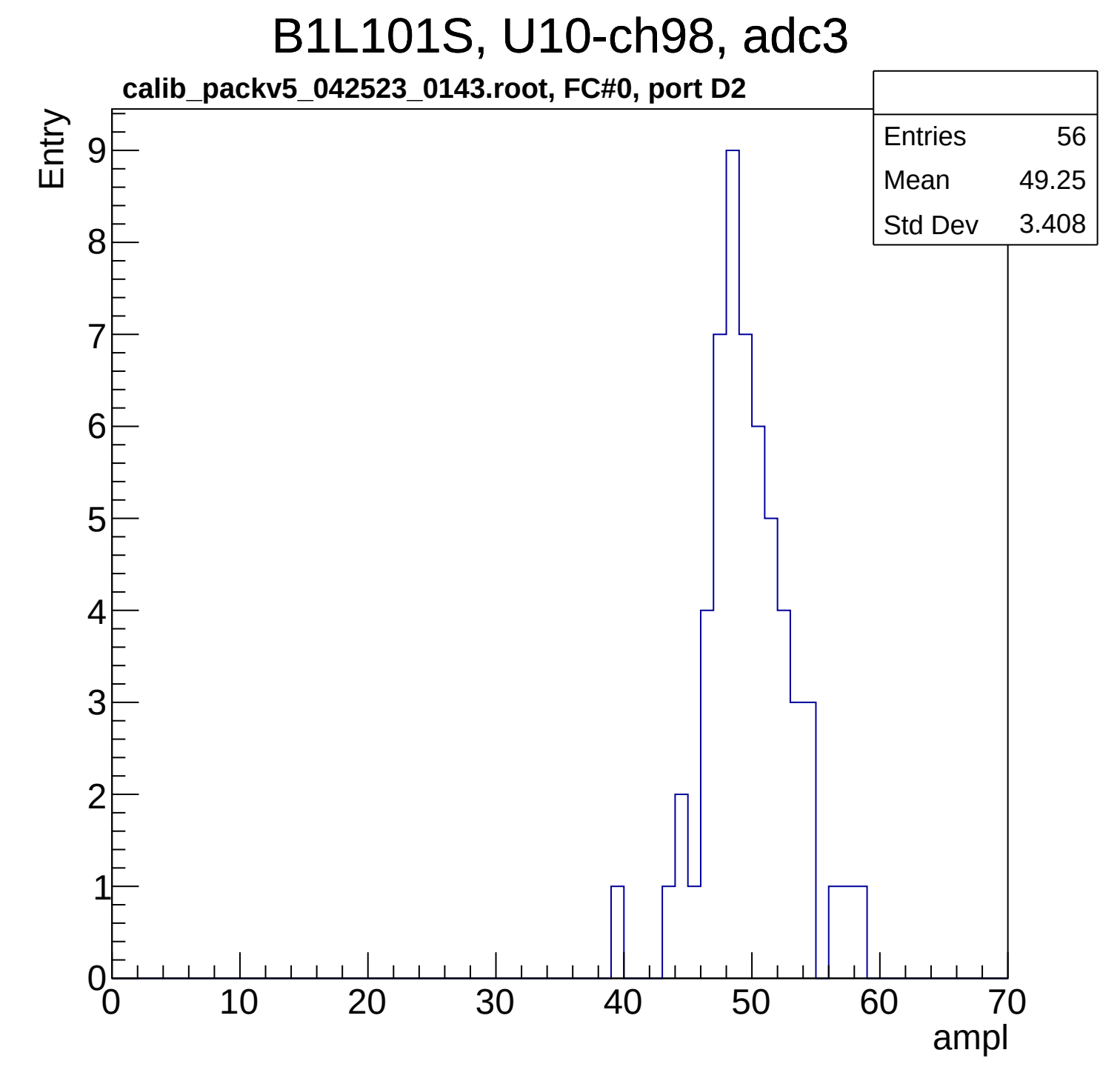
B1L101S, U10-ch98, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 49.25
Std Dev 3.408
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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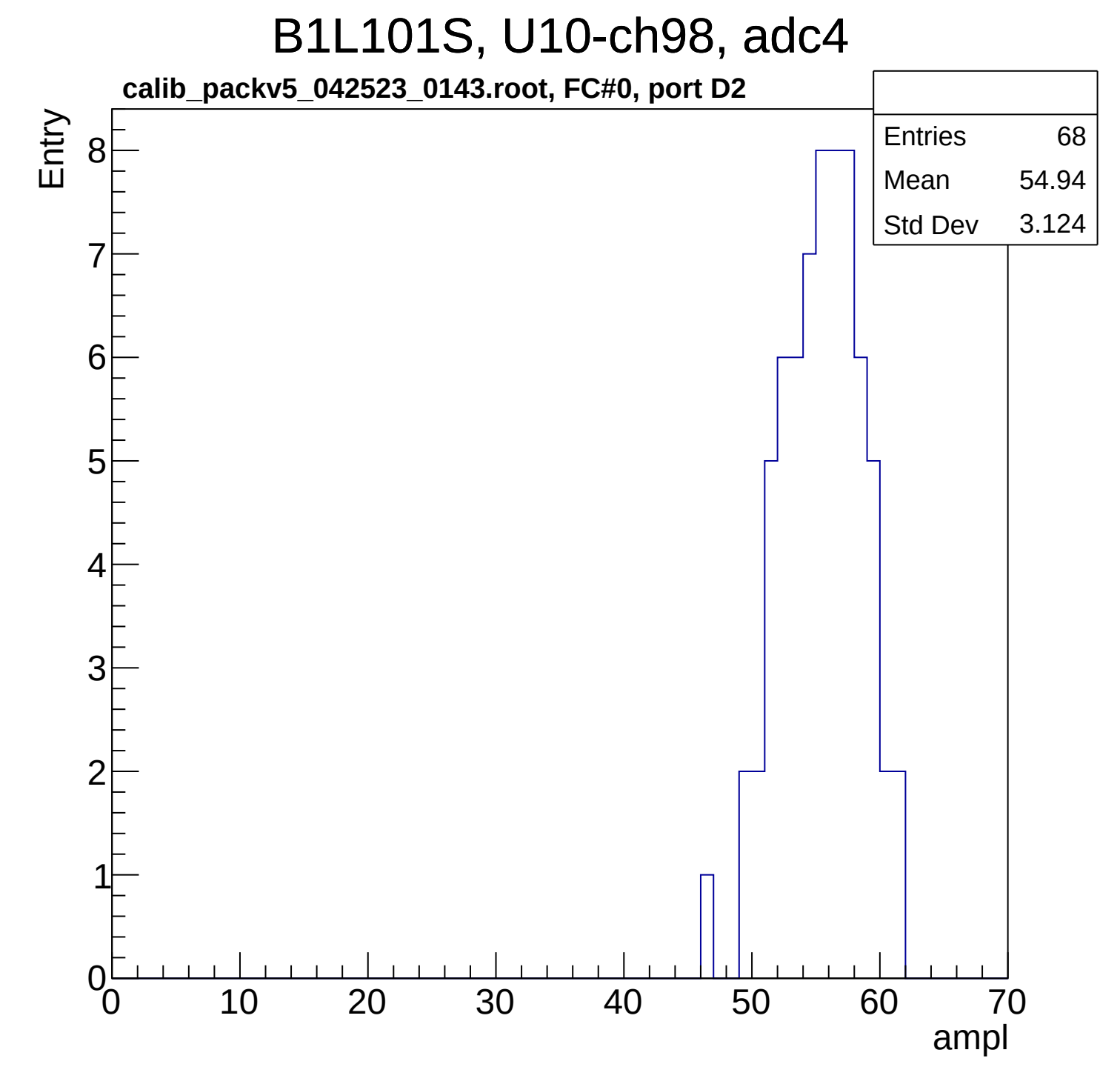
B1L101S, U10-ch98, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 54.94
Std Dev 3.124
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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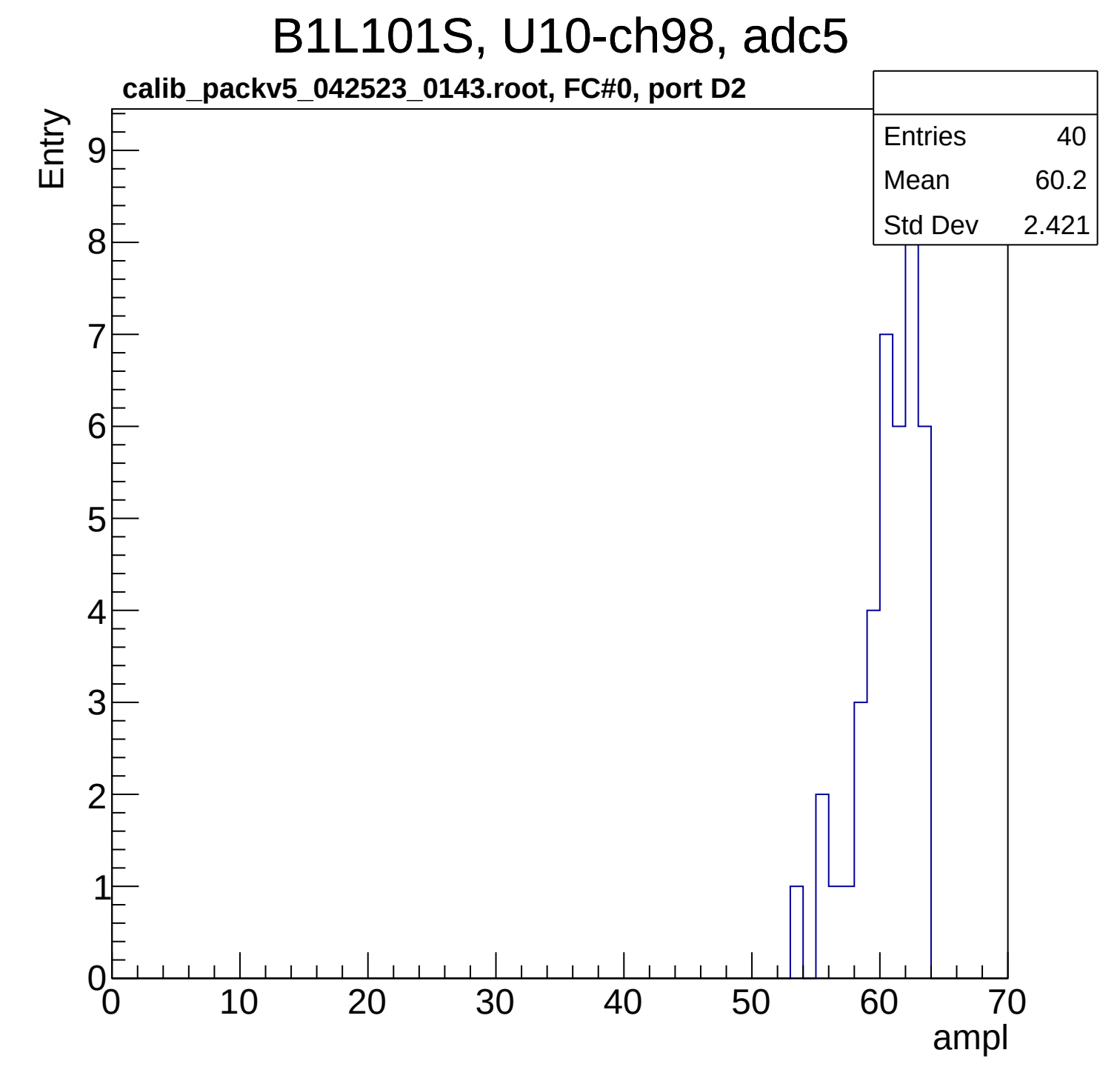
B1L101S, U10-ch98, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 40
Mean 60.2
Std Dev 2.421
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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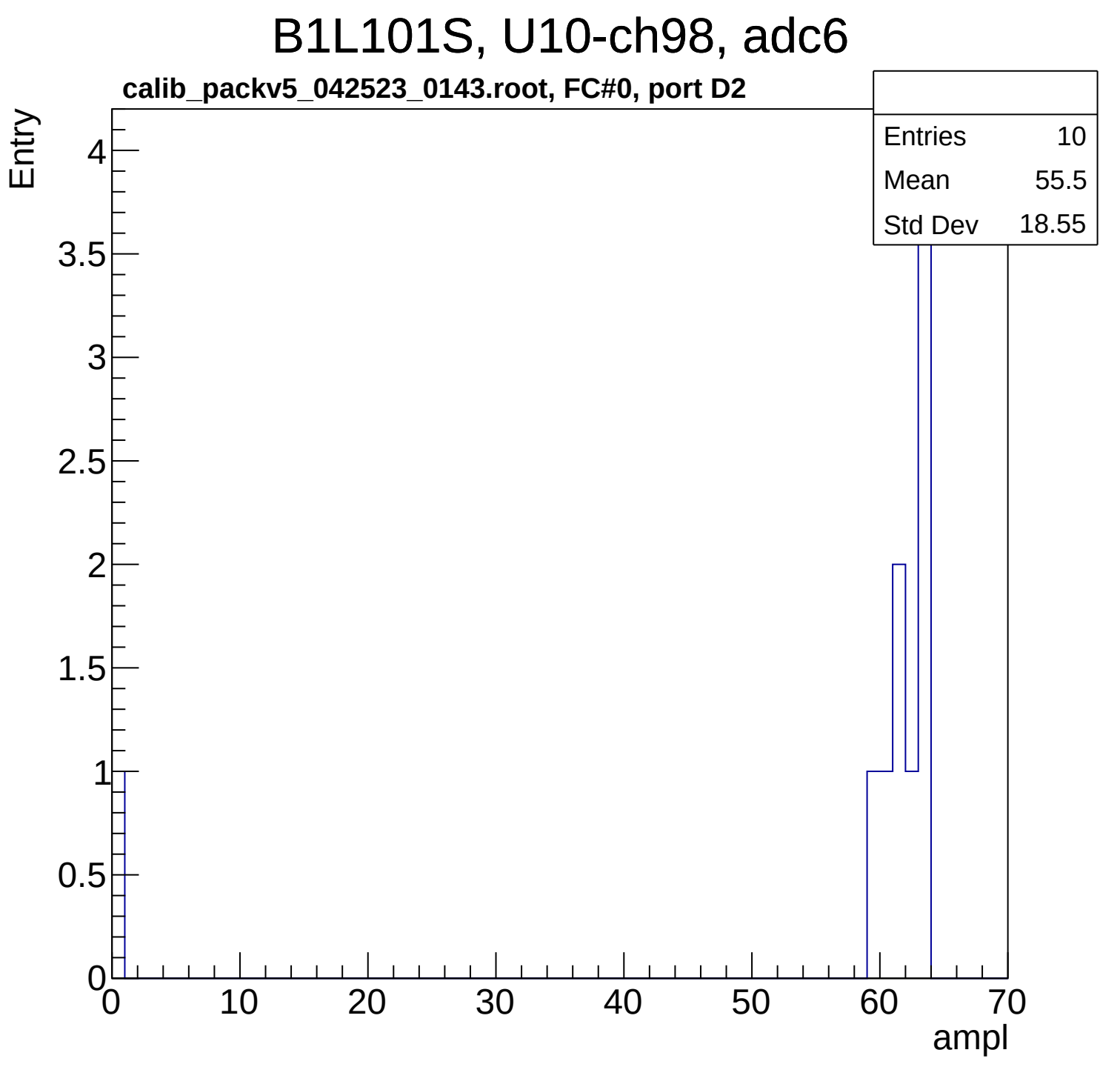
B1L101S, U10-ch98, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 55.5
Std Dev 18.55
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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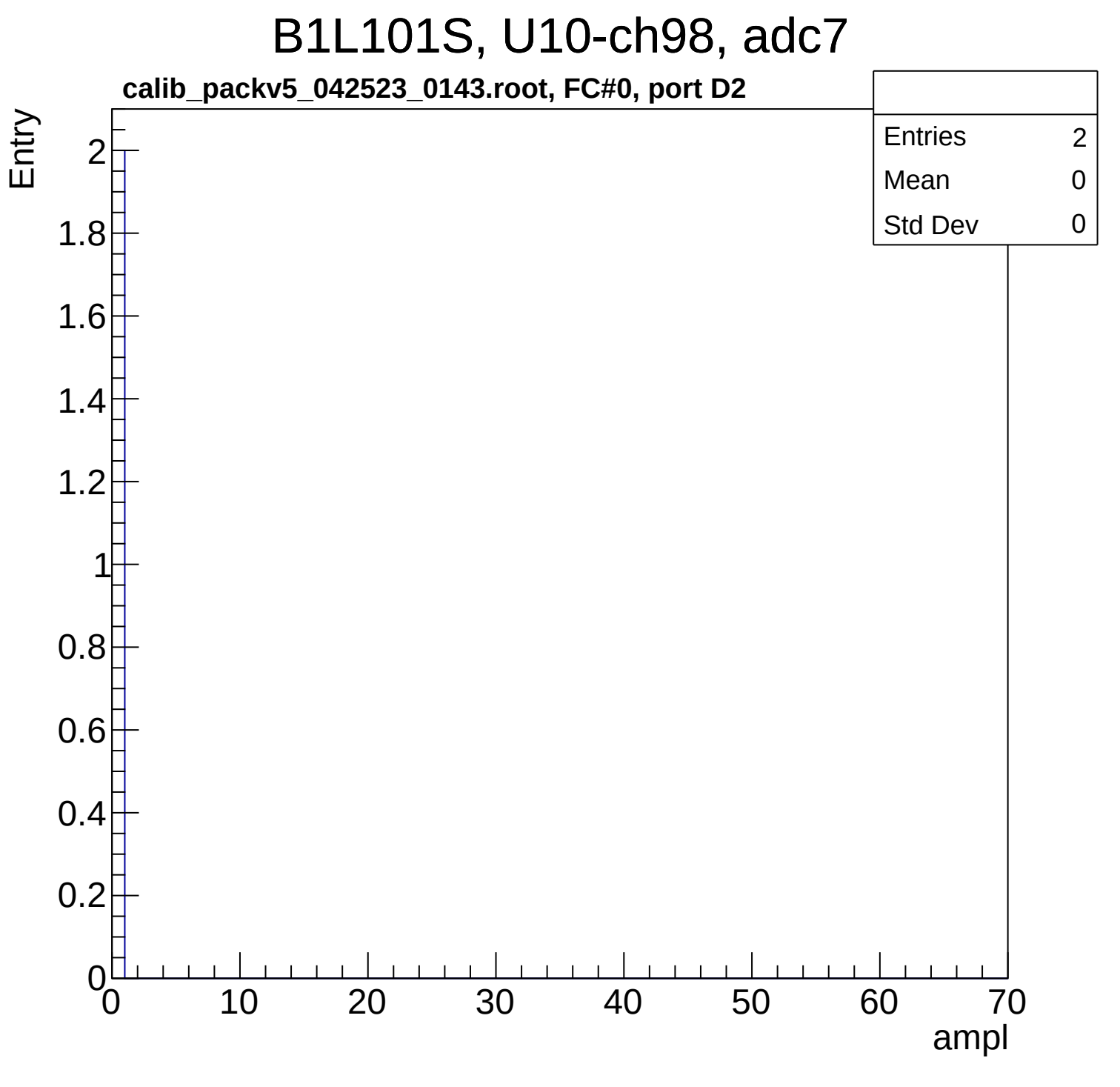
B1L101S, U10-ch98, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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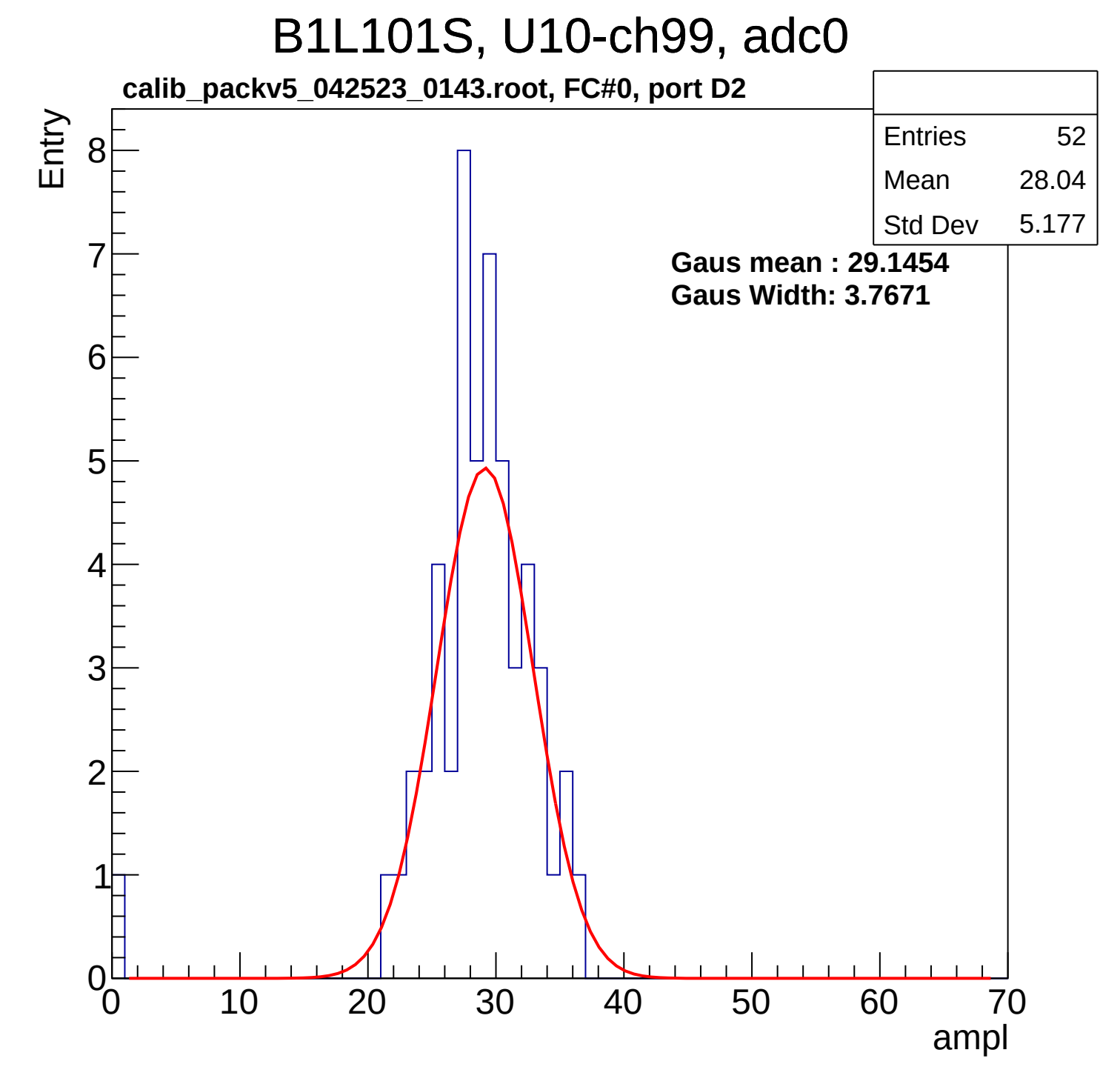
B1L101S, U10-ch99, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 28.04
Std Dev 5.177
Gaus mean : 29.1454
Gaus Width: 3.7671
Entry
ampl
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1
2
3
4
5
6
7
8
0
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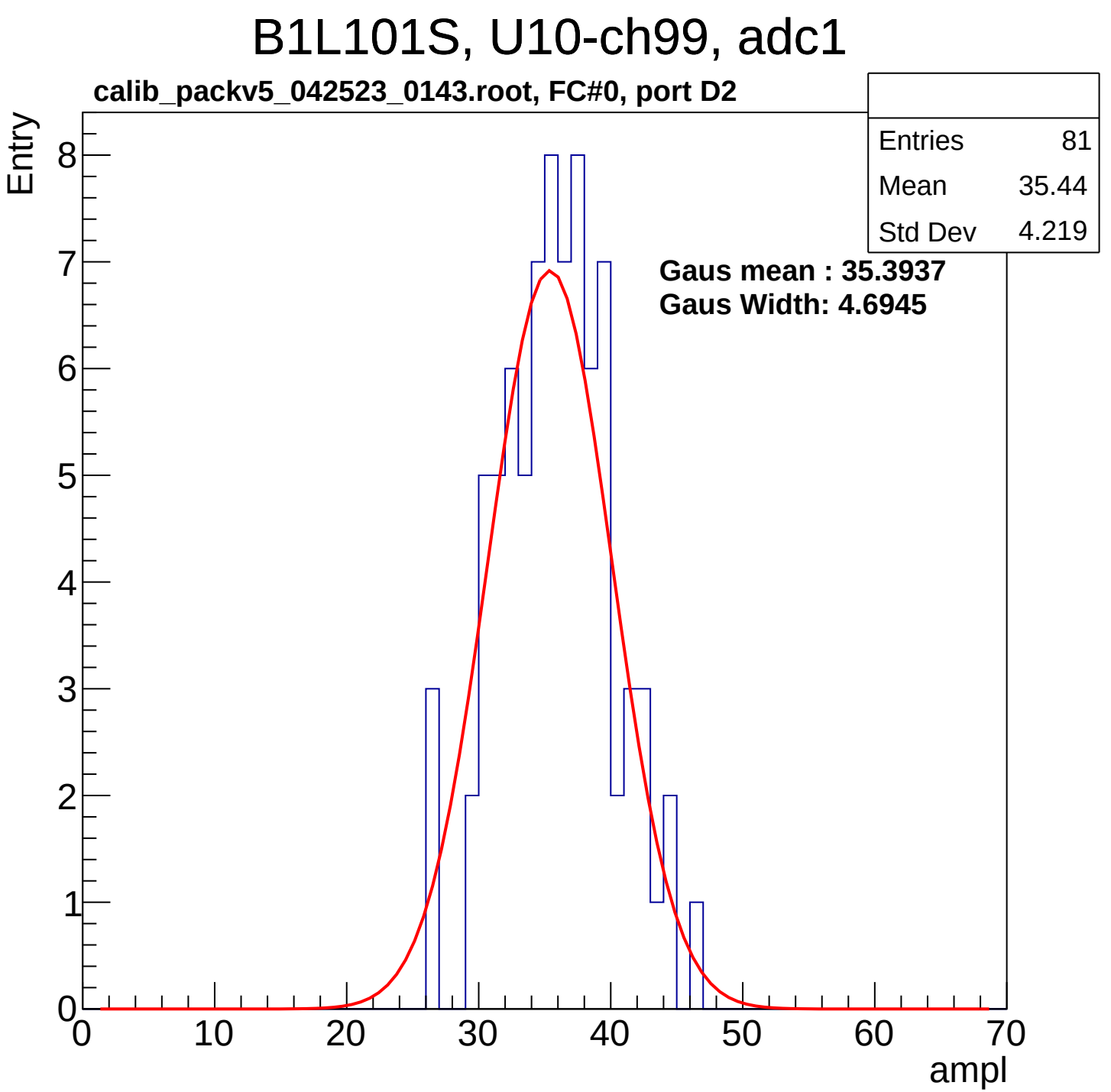
20
30
40
50
60
70


B1L101S, U10-ch99, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 81
Mean 35.44
Std Dev 4.219
Gaus mean : 35.3937
Gaus Width: 4.6945
Entry
ampl
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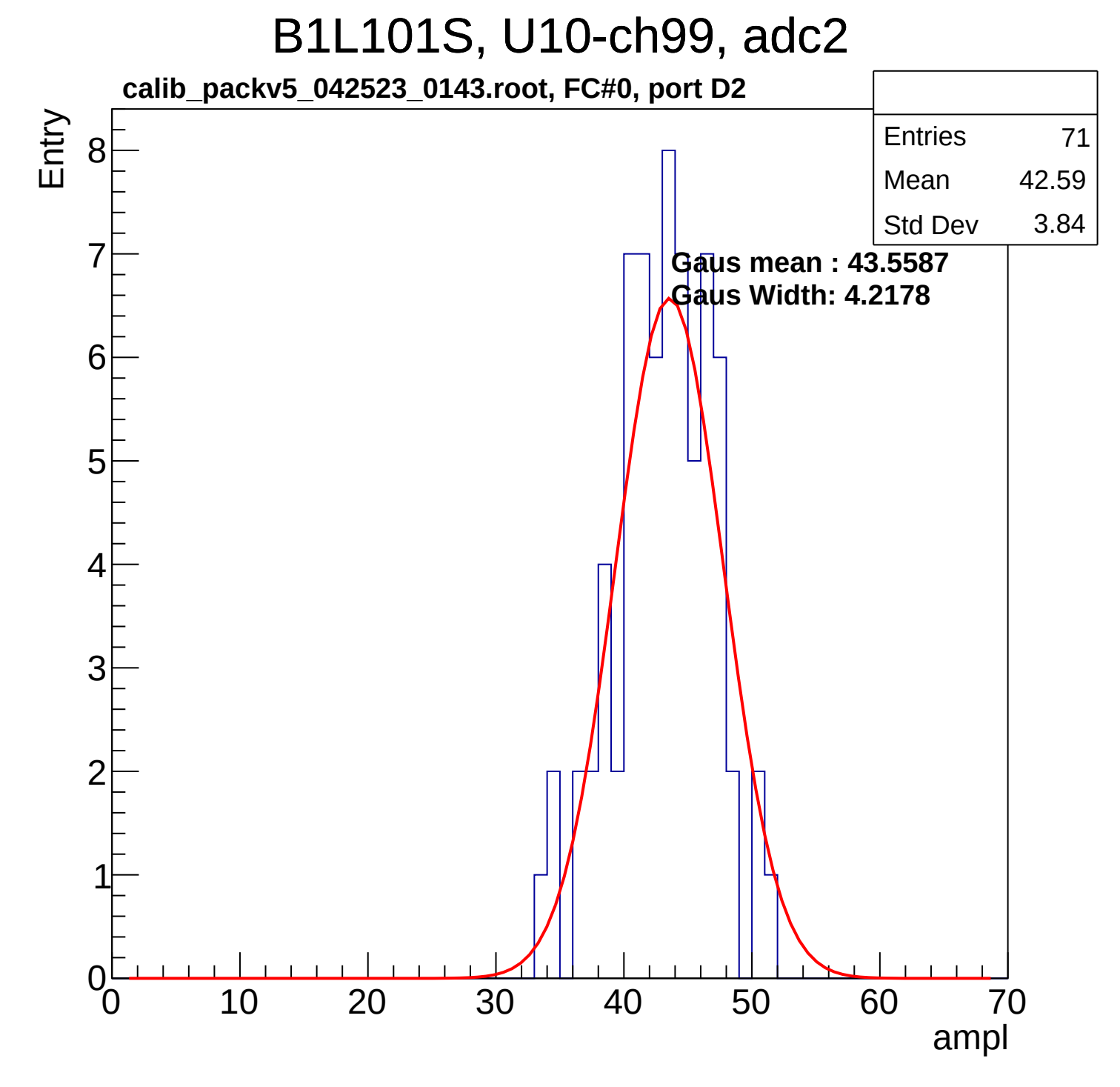
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch99, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 42.59
Std Dev 3.84
Gaus mean : 43.5587
Gaus Width: 4.2178
Entry
ampl
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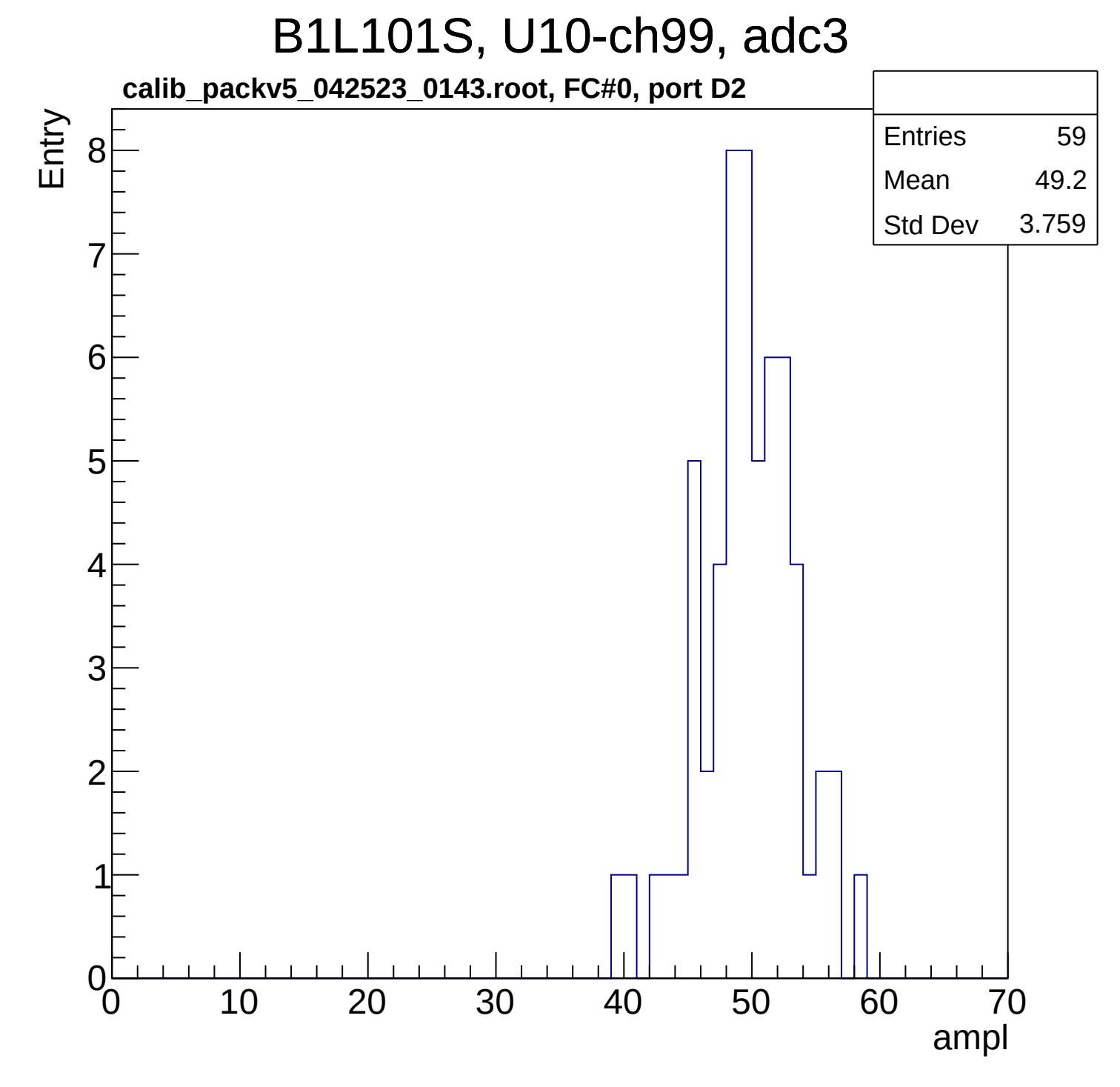
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch99, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 49.2
Std Dev 3.759
Entry
ampl
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1
2
3
4
5
6
7
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0
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60
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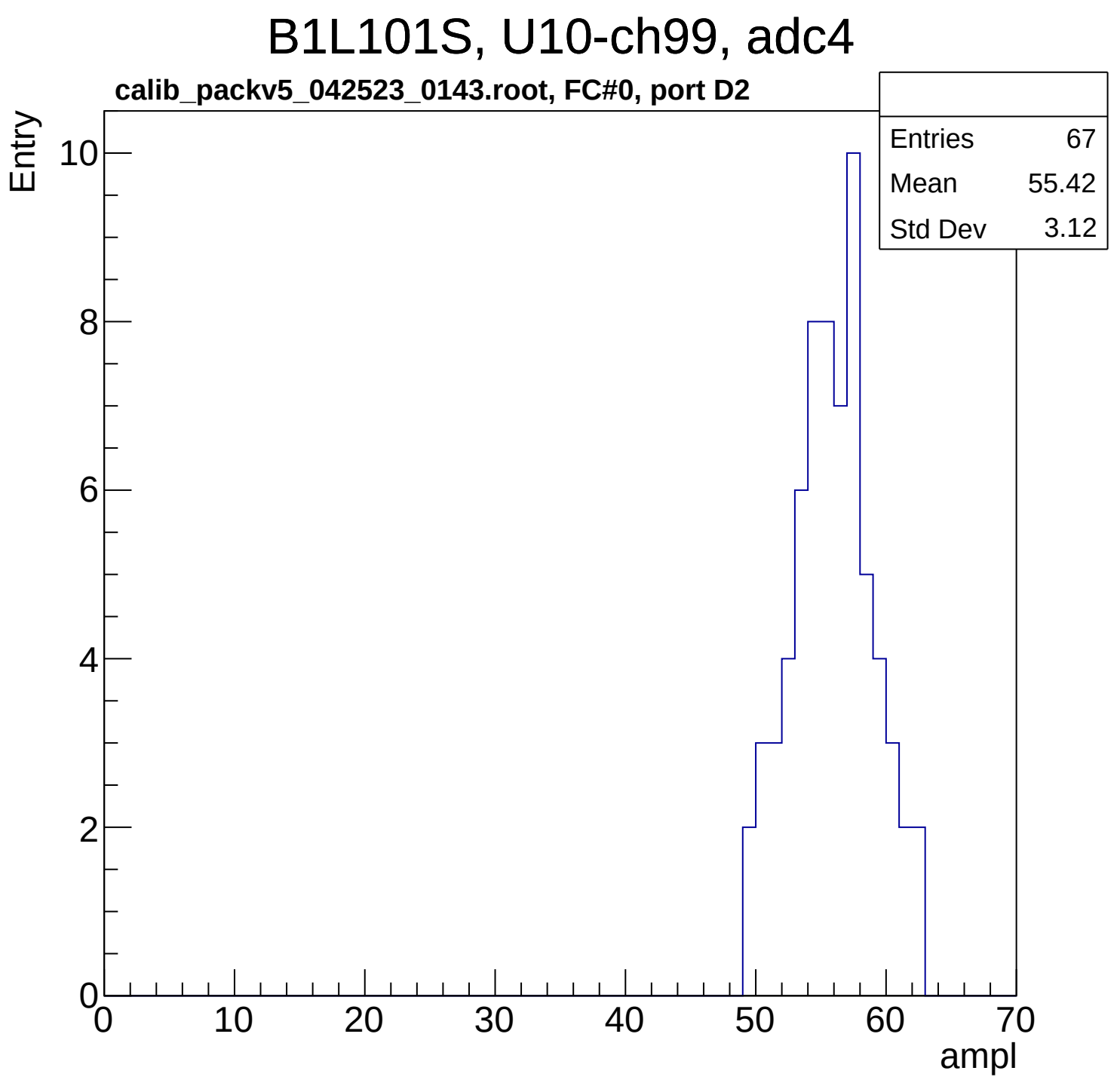
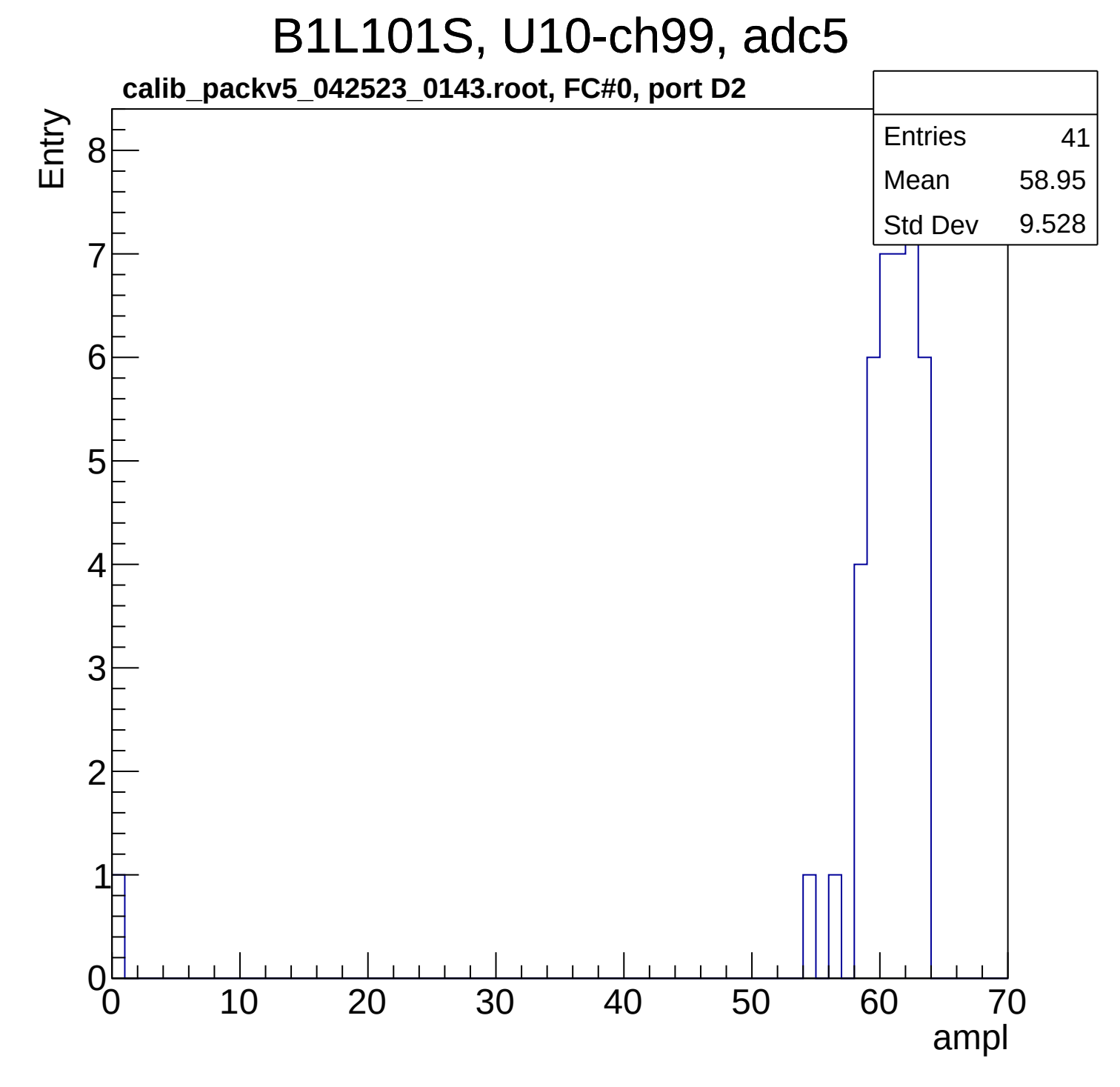
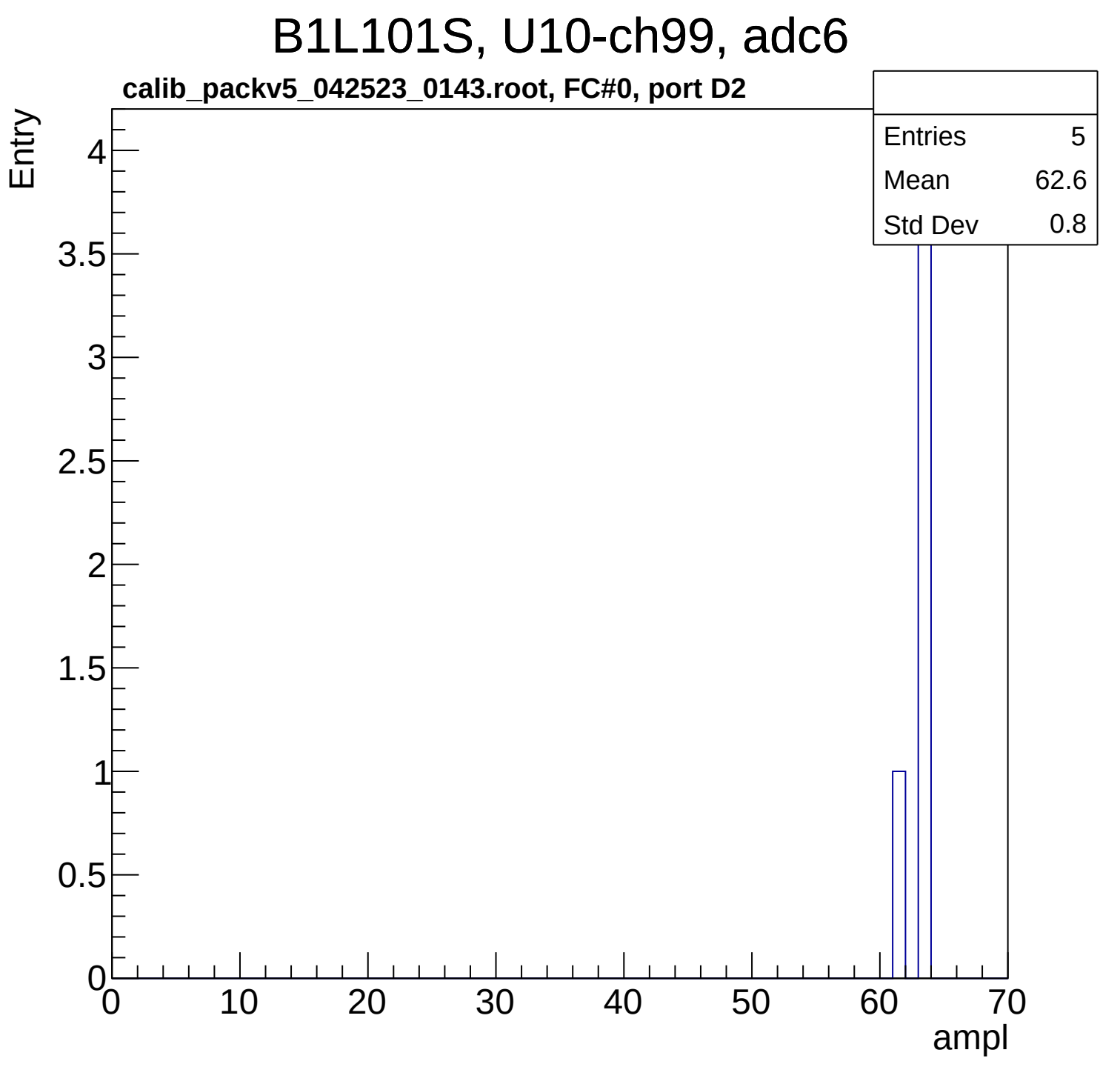

B1L101S, U10-ch99, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 55.42
Std Dev 3.12
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch99, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 41
Mean 58.95
Std Dev 9.528
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch99, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 62.6
Std Dev 0.8
Entry
ampl
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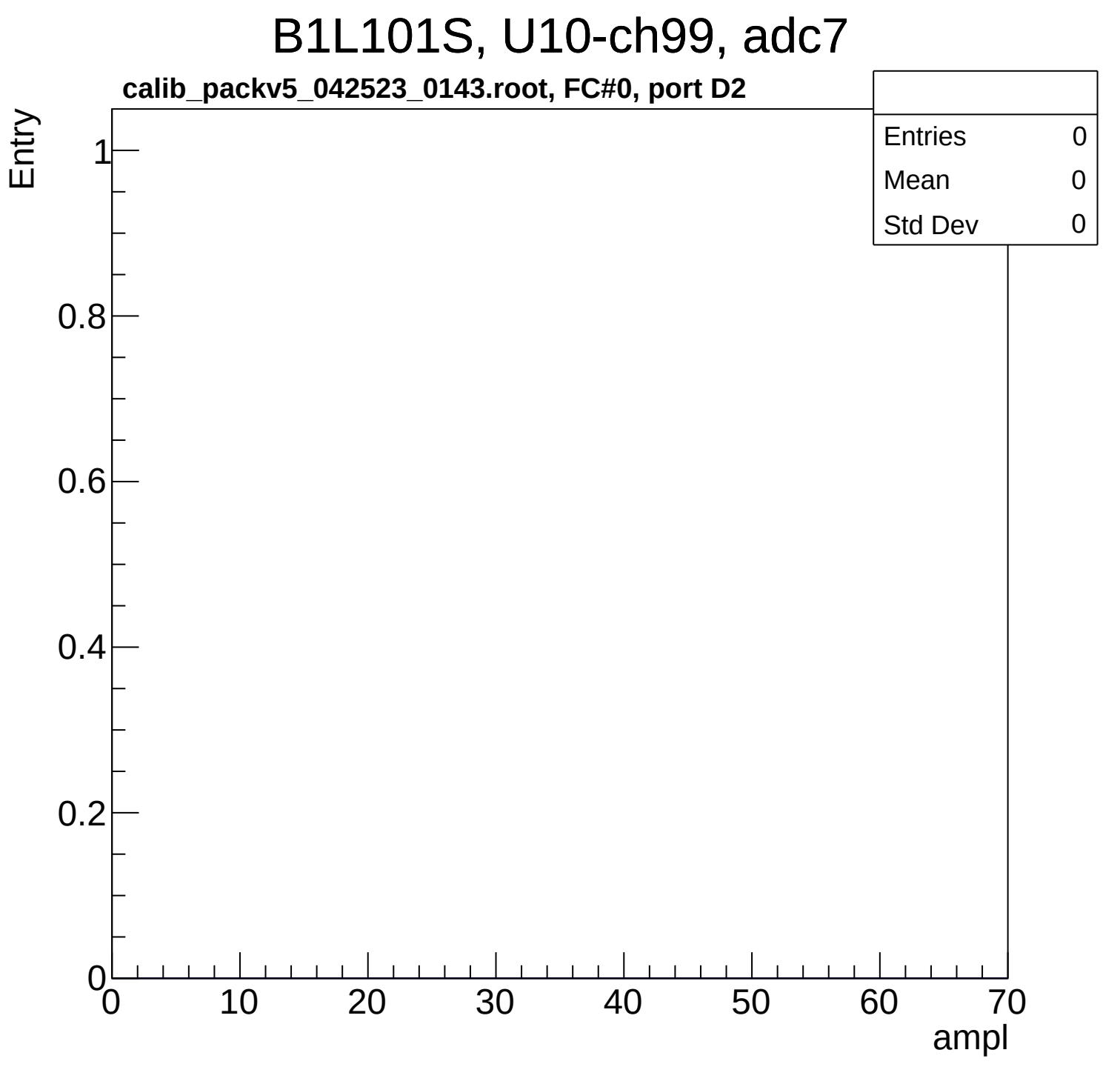
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L101S, U10-ch99, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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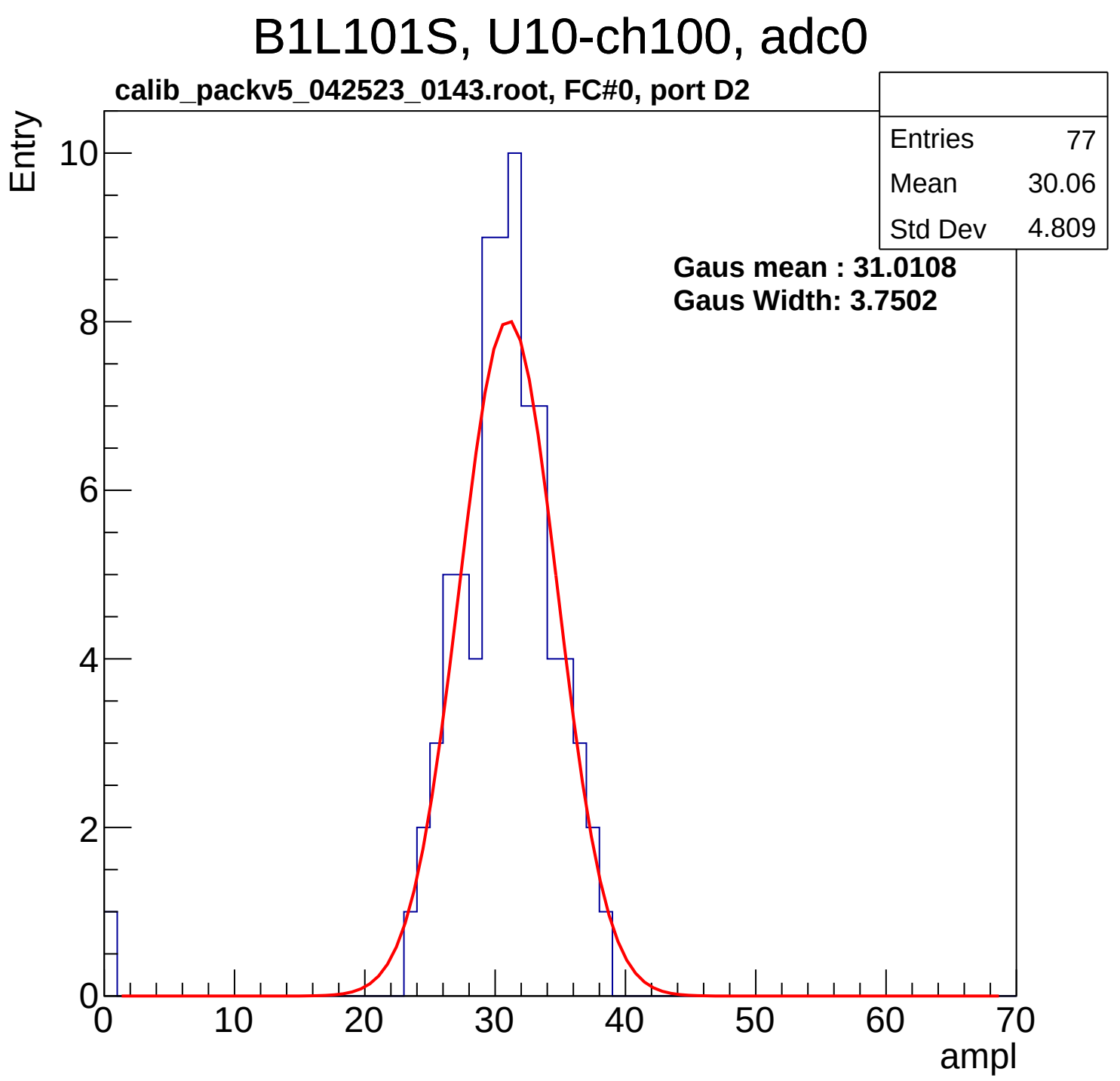
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch100, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 30.06
Std Dev 4.809
Gaus mean : 31.0108
Gaus Width: 3.7502
Entry
ampl
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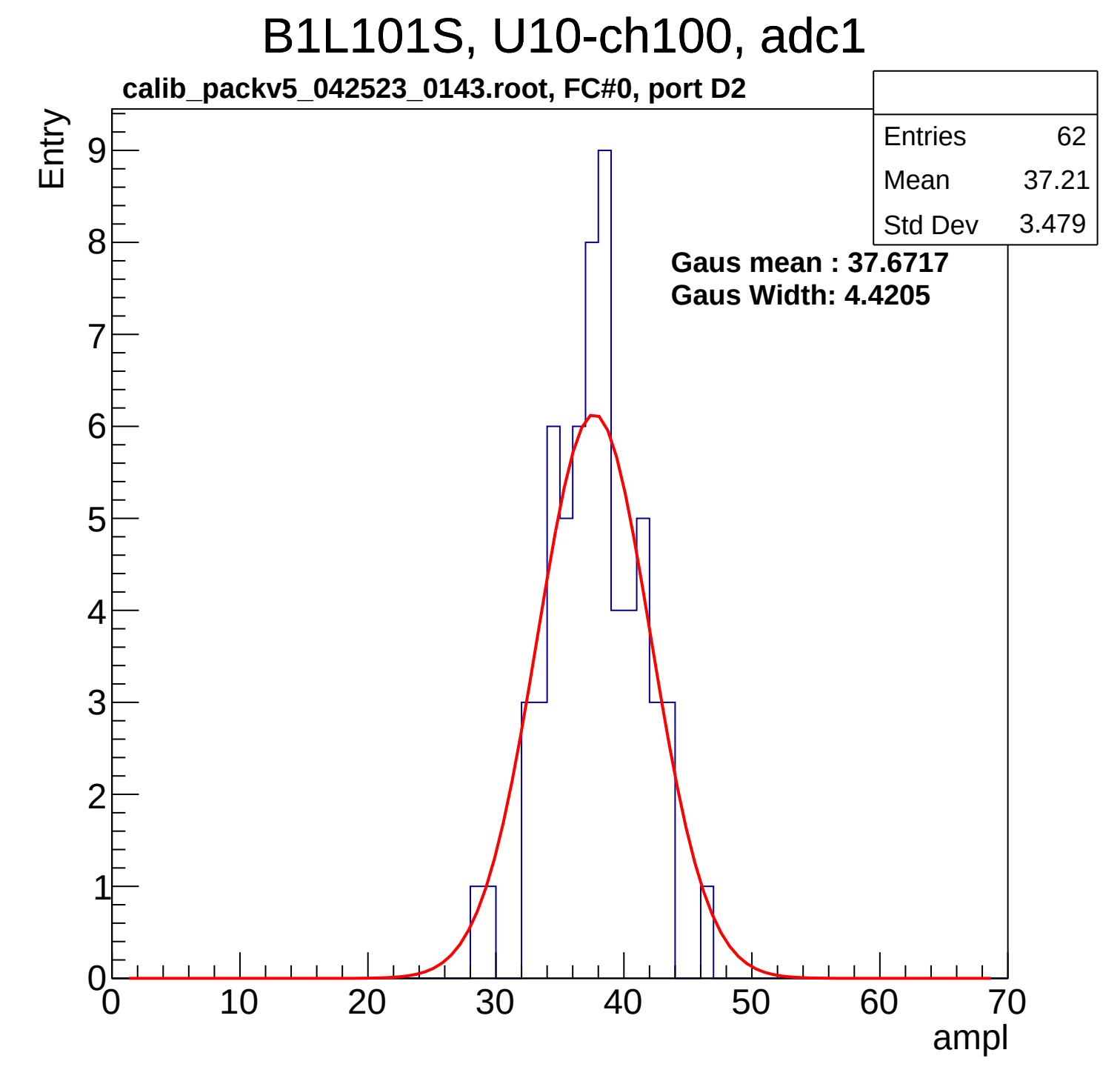
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch100, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 37.21
Std Dev 3.479
Gaus mean : 37.6717
Gaus Width: 4.4205
Entry
ampl
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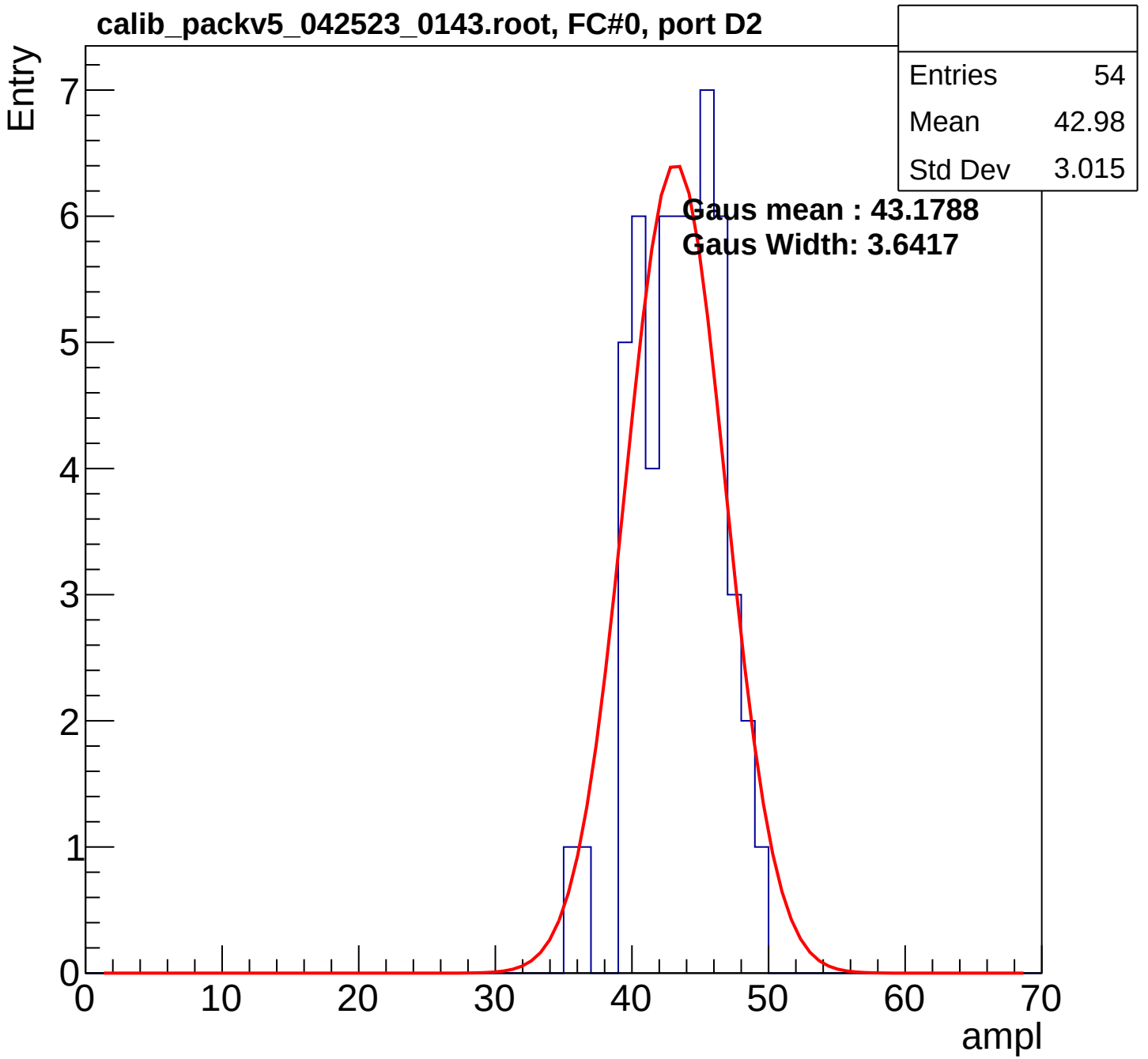
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch100, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 42.98
Std Dev 3.015
Gaus mean : 43.1788
Gaus Width: 3.6417
Entry
ampl
0
1
2
3
4
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6
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0
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60
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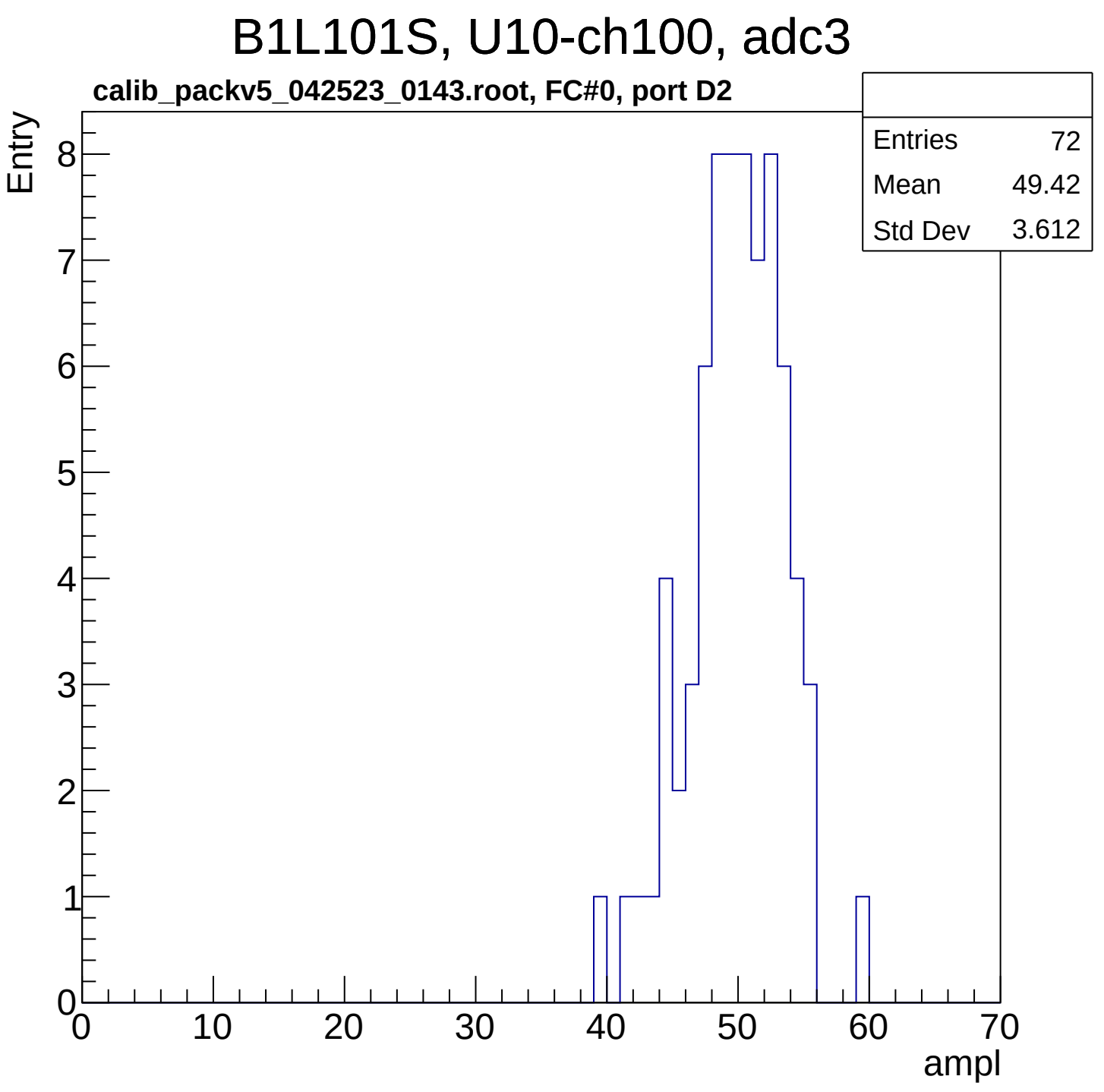
B1L101S, U10-ch100, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 49.42
Std Dev 3.612
Entry
ampl
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1
2
3
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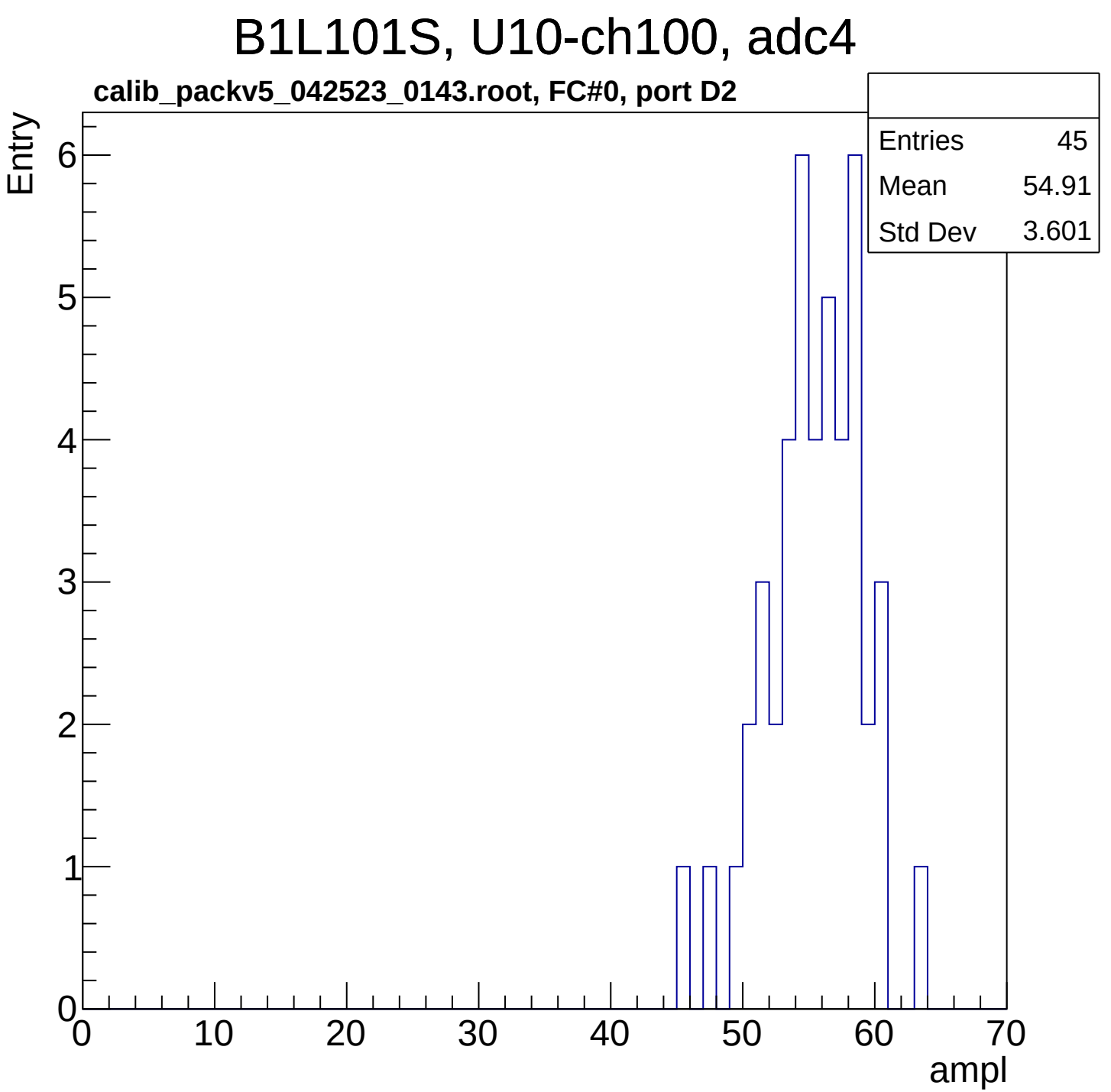
B1L101S, U10-ch100, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 54.91
Std Dev 3.601
Entry
ampl
0
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2
3
4
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0
10
20
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40
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60
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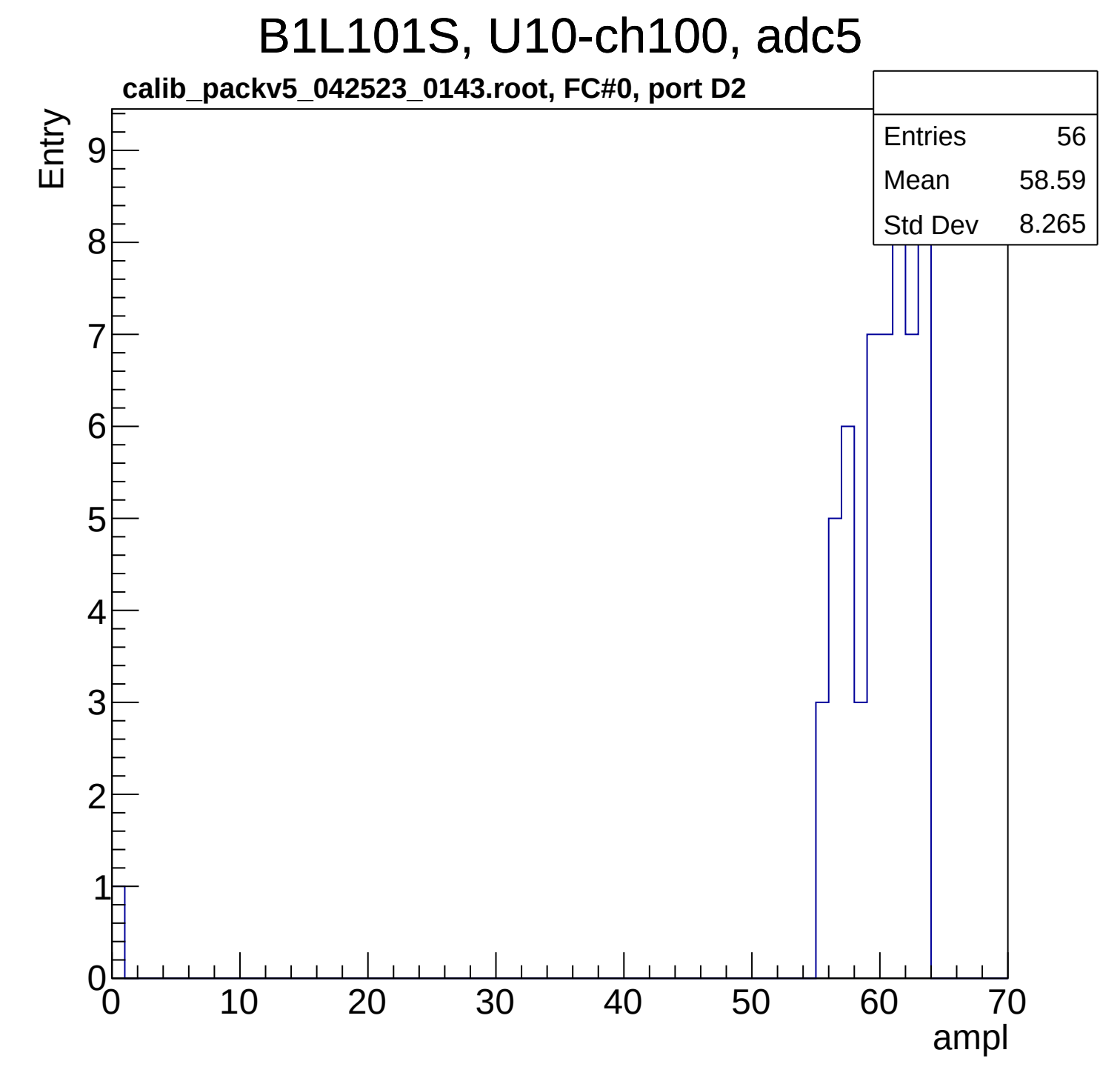
B1L101S, U10-ch100, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 58.59
Std Dev 8.265
Entry
ampl
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2
3
4
5
6
7
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0
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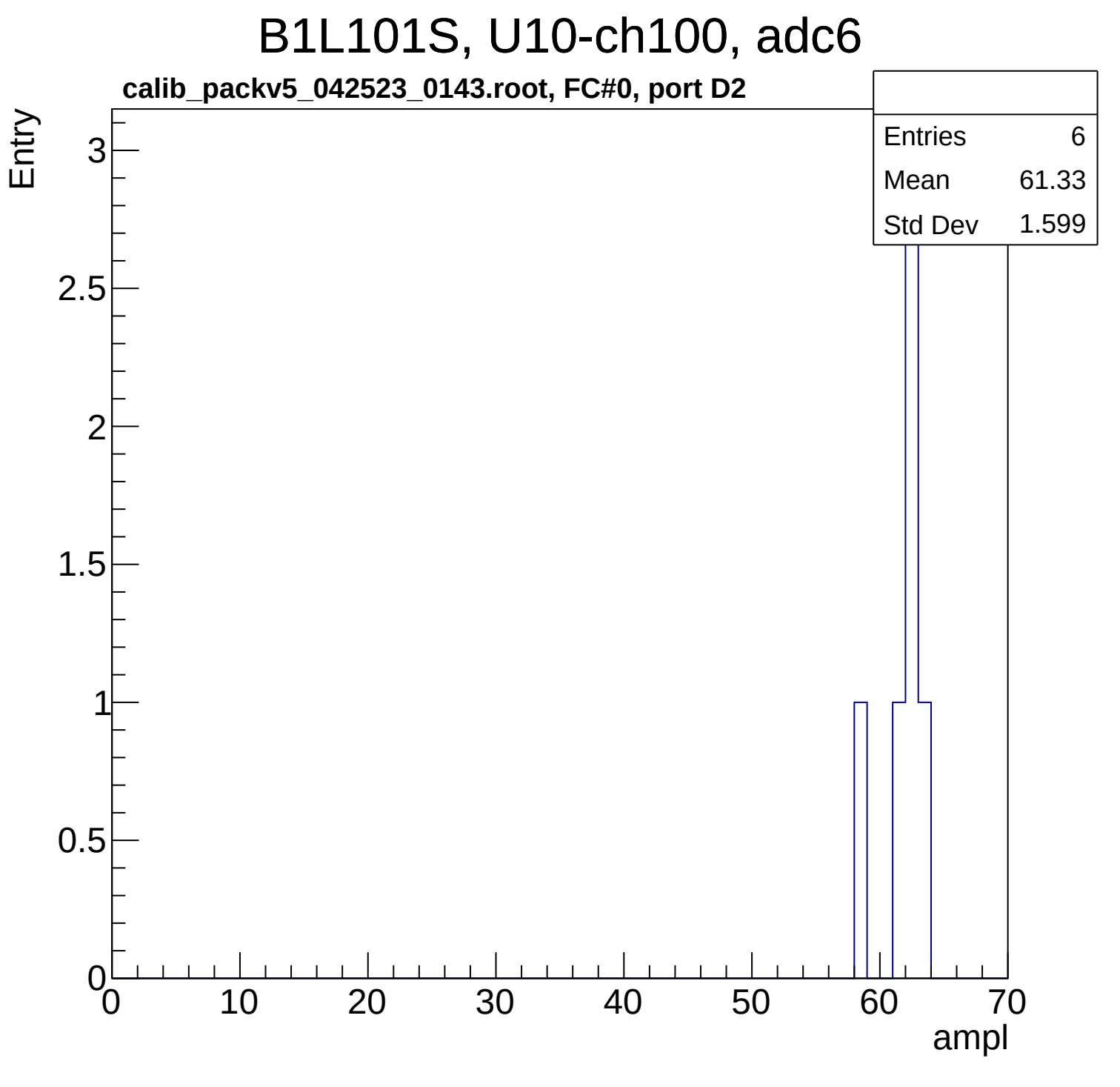
B1L101S, U10-ch100, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 61.33
Std Dev 1.599
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
30
40
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60
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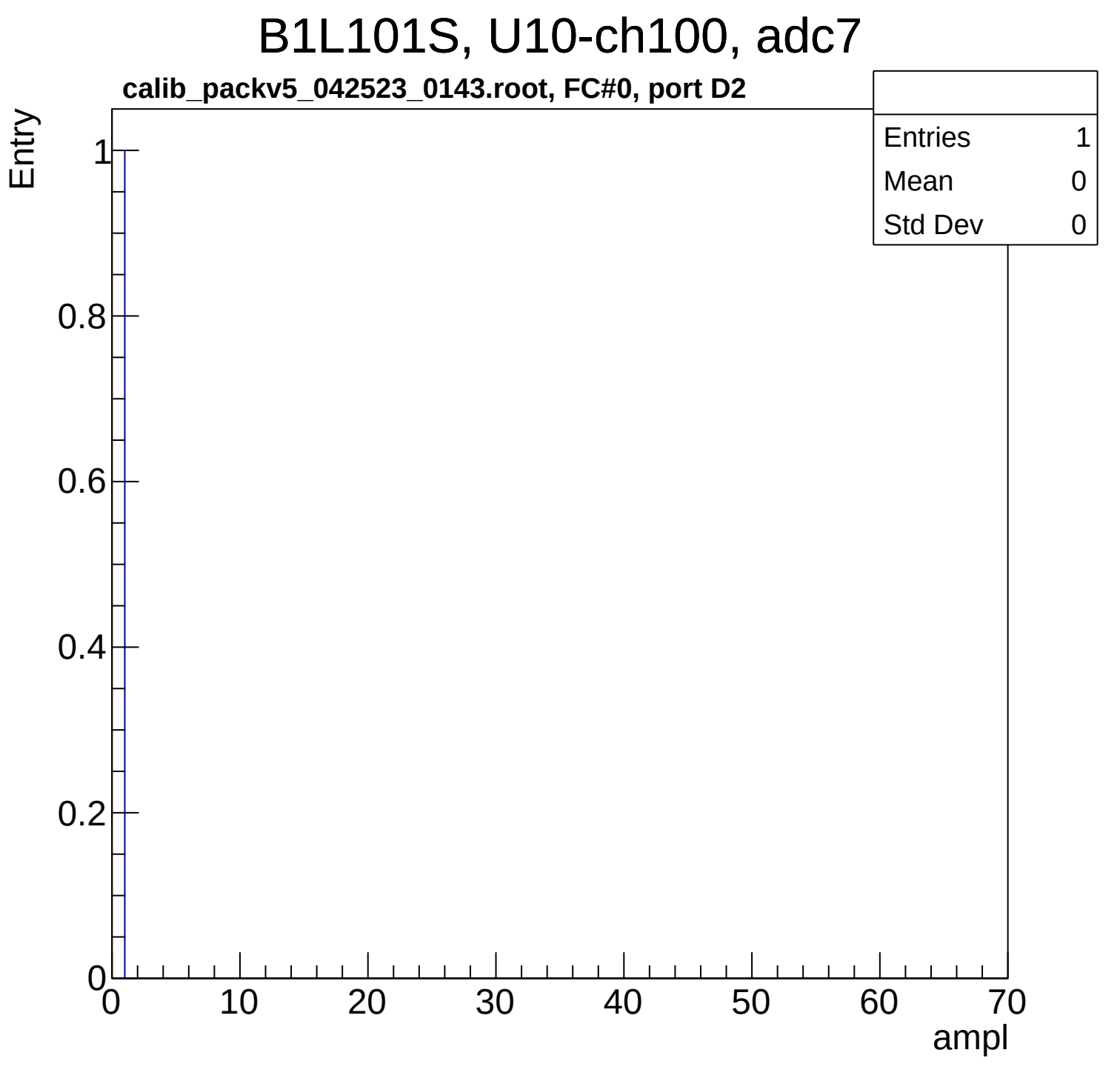
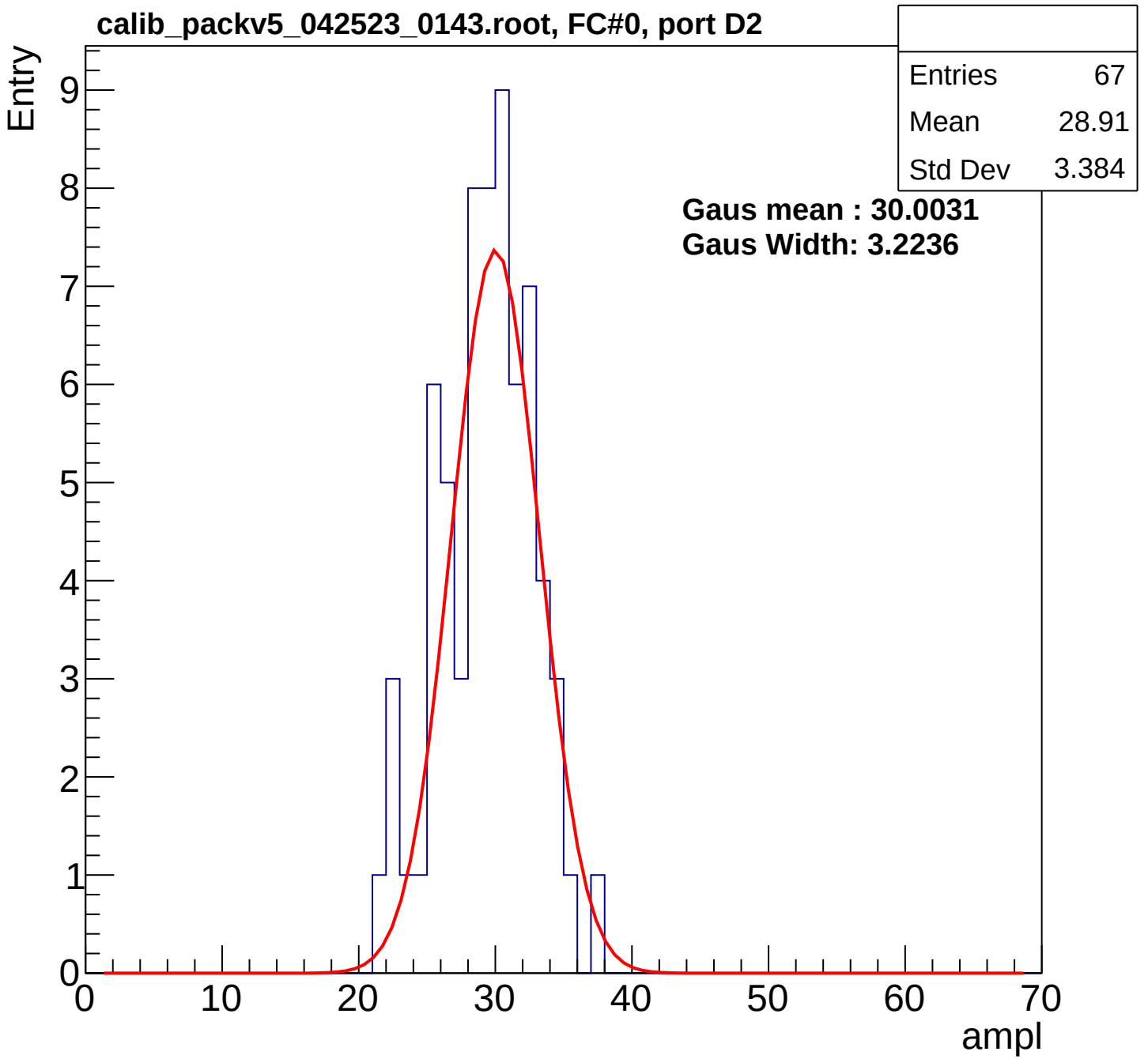

B1L101S, U10-ch100, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch101, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 28.91
Std Dev 3.384
Gaus mean : 30.0031
Gaus Width: 3.2236
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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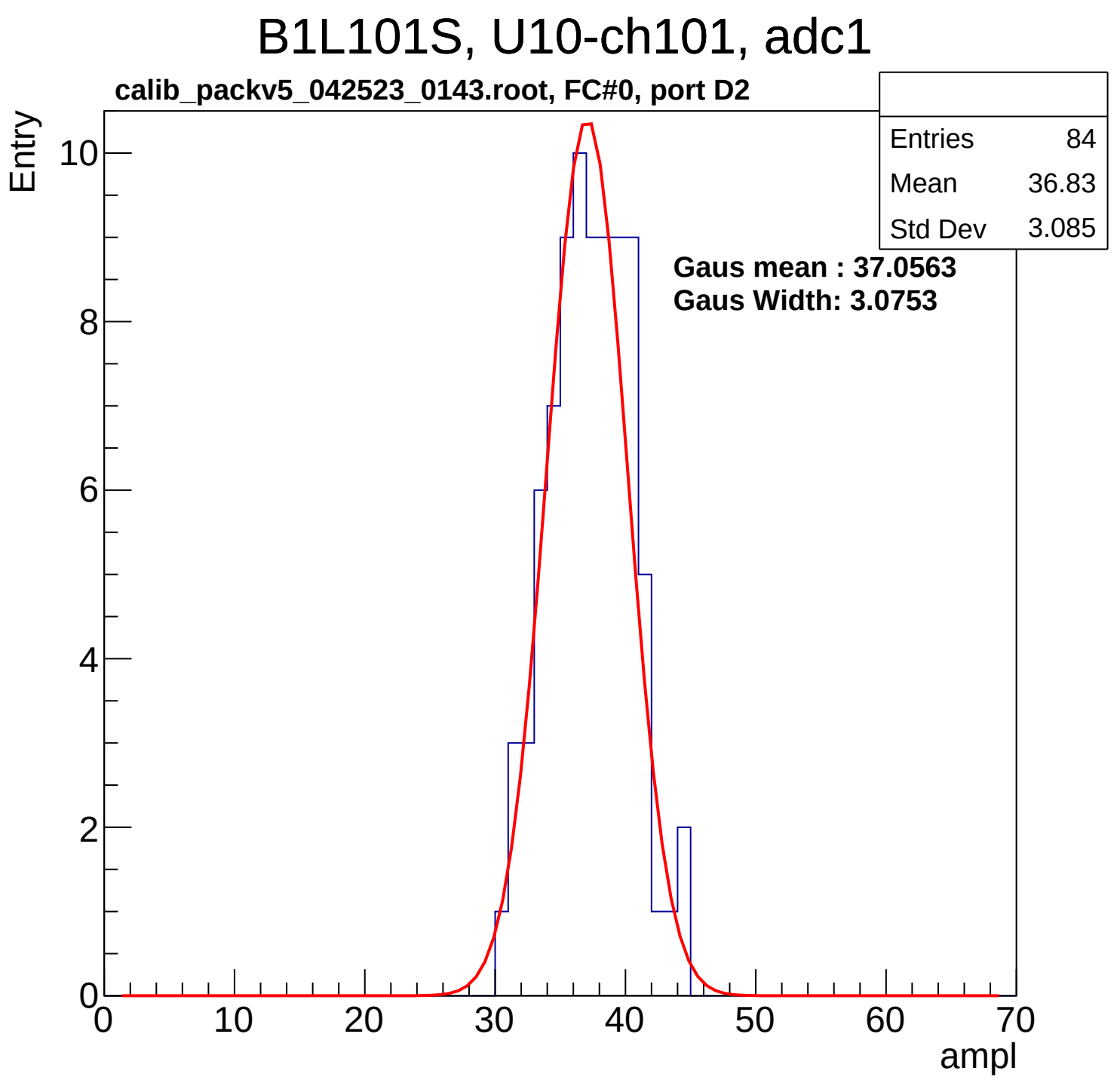
B1L101S, U10-ch101, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 84
Mean 36.83
Std Dev 3.085
Gaus mean : 37.0563
Gaus Width: 3.0753
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
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60
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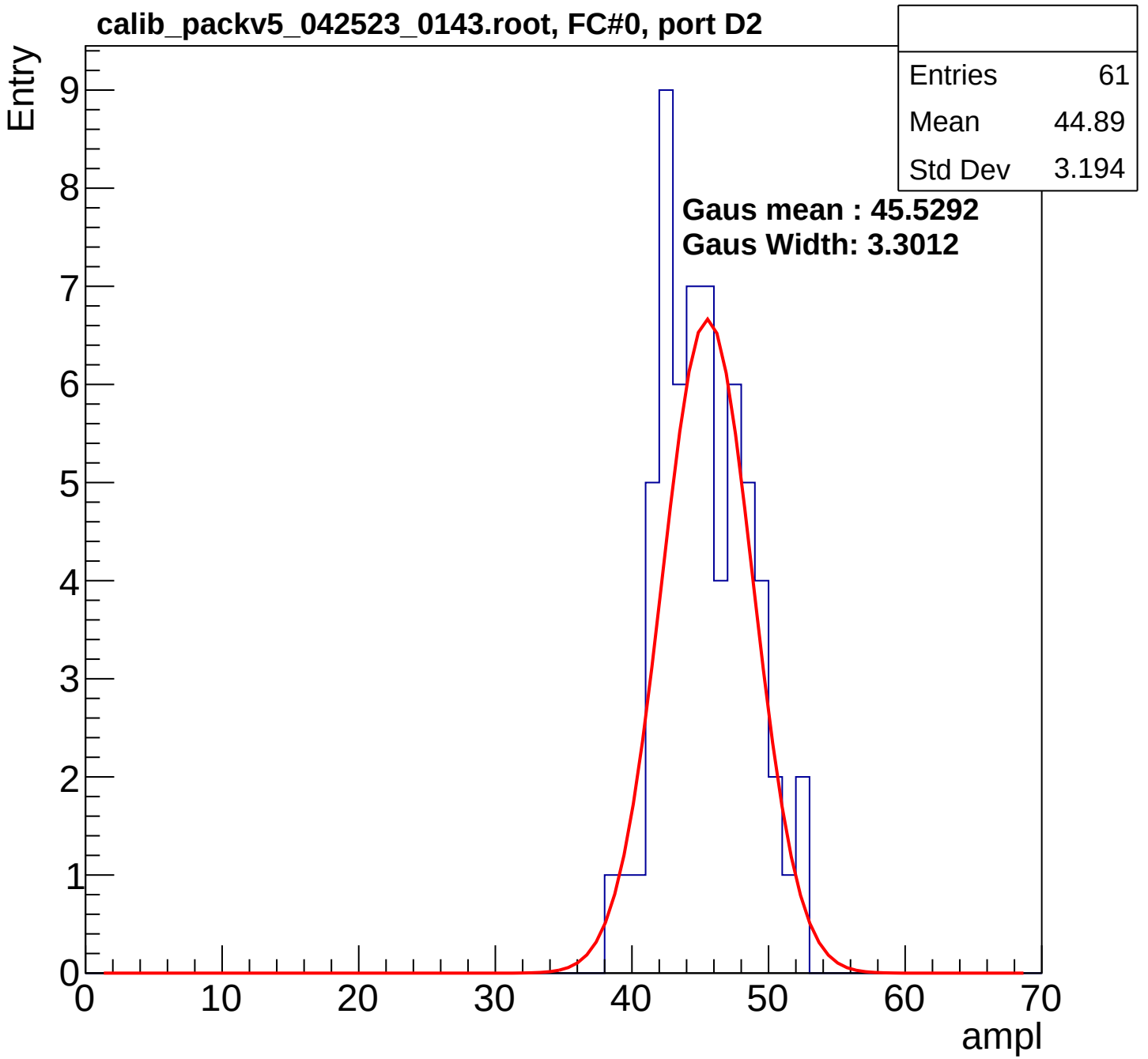
B1L101S, U10-ch101, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 44.89
Std Dev 3.194
Gaus mean : 45.5292
Gaus Width: 3.3012
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
30
40
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60
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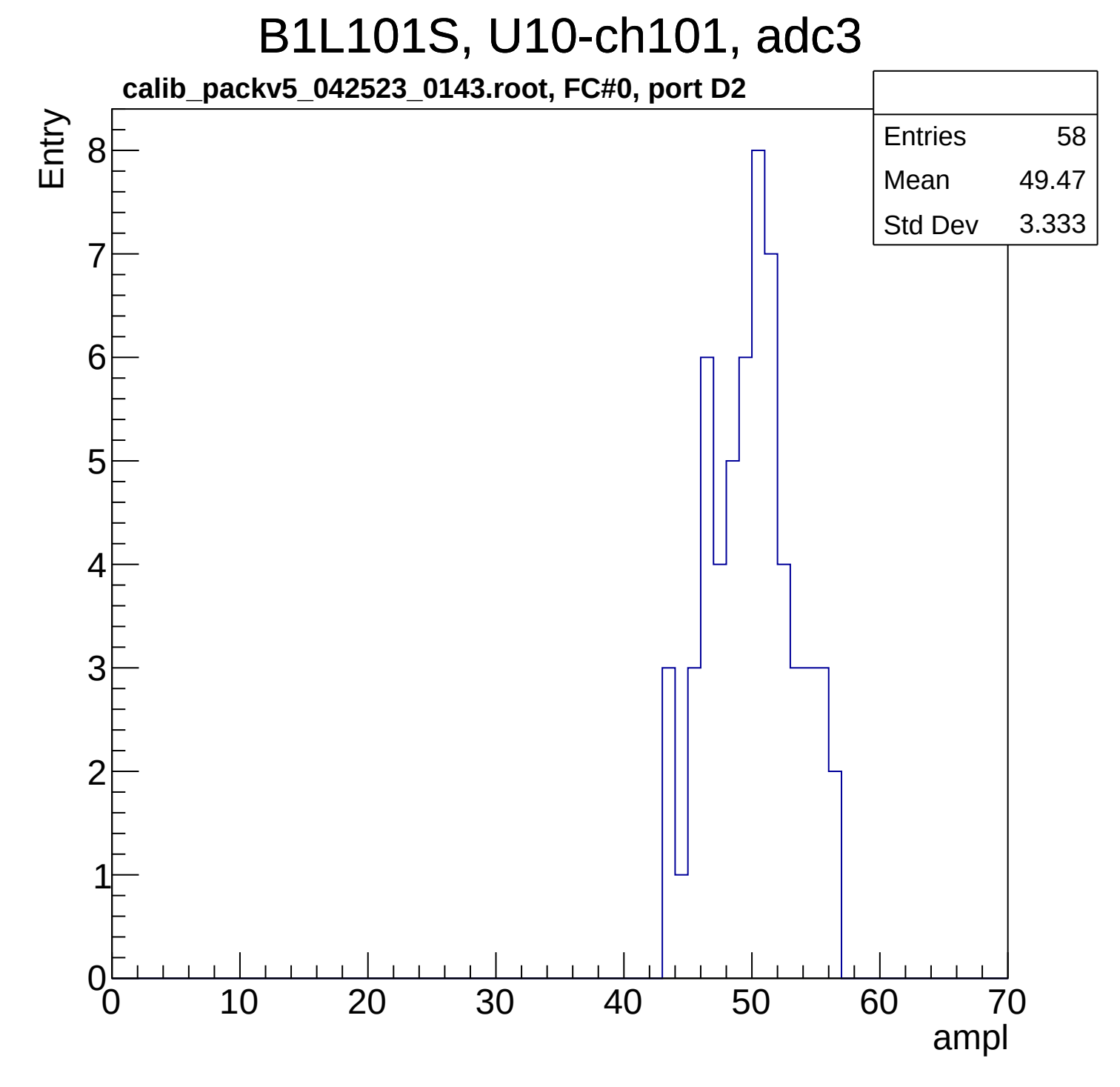
B1L101S, U10-ch101, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 49.47
Std Dev 3.333
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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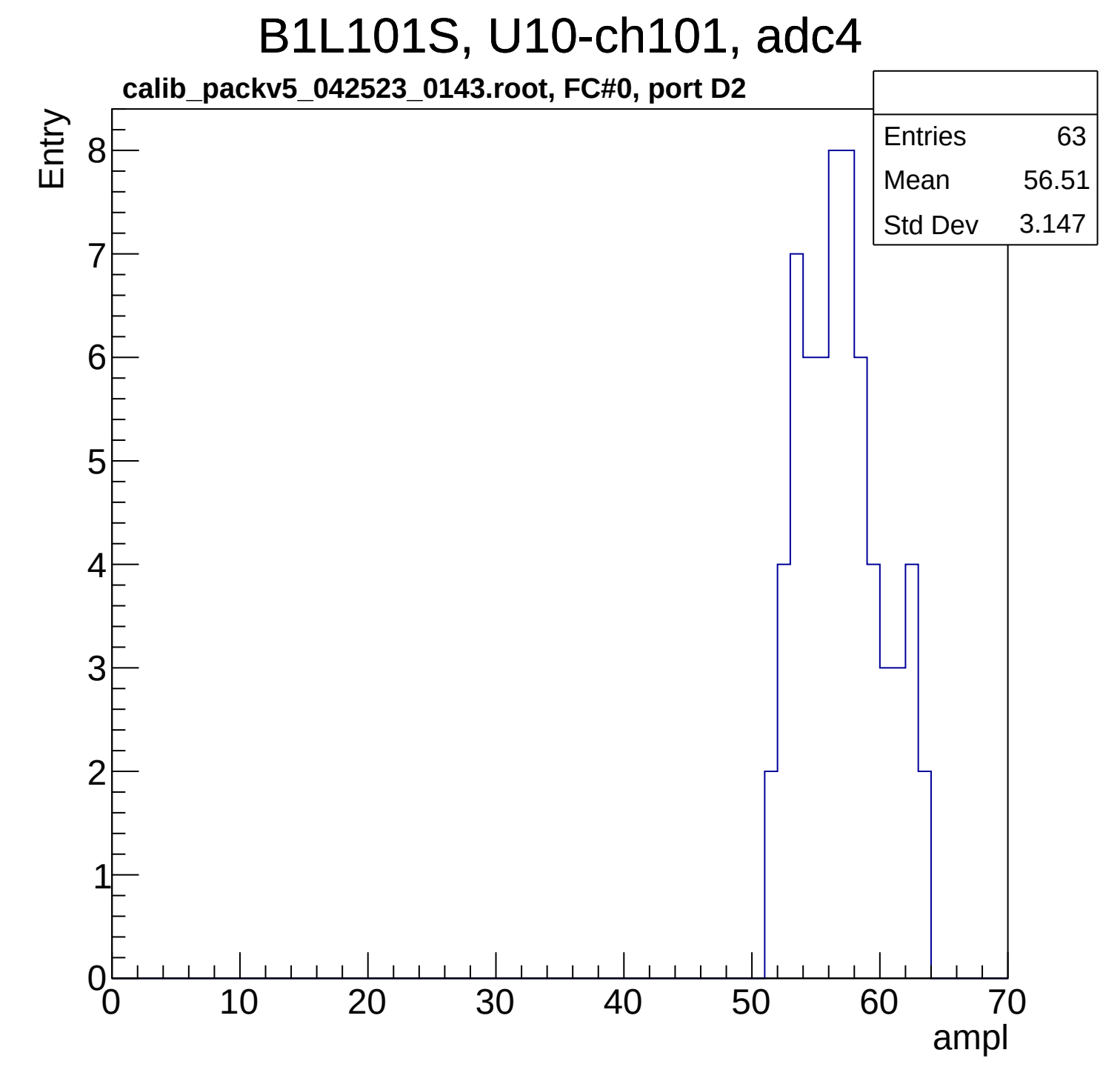
B1L101S, U10-ch101, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 56.51
Std Dev 3.147
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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20
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40
50
60
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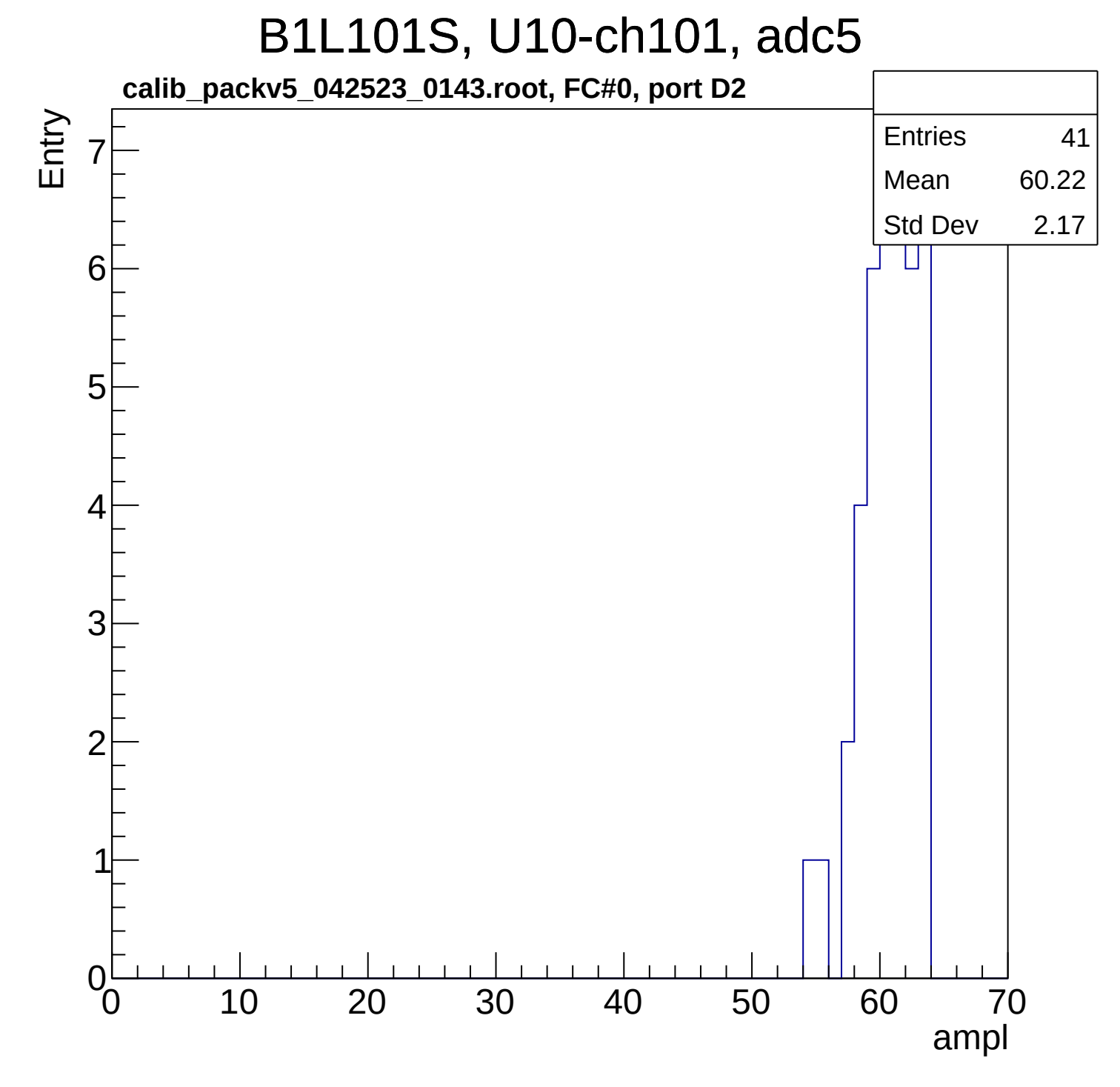
B1L101S, U10-ch101, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 41
Mean 60.22
Std Dev 2.17
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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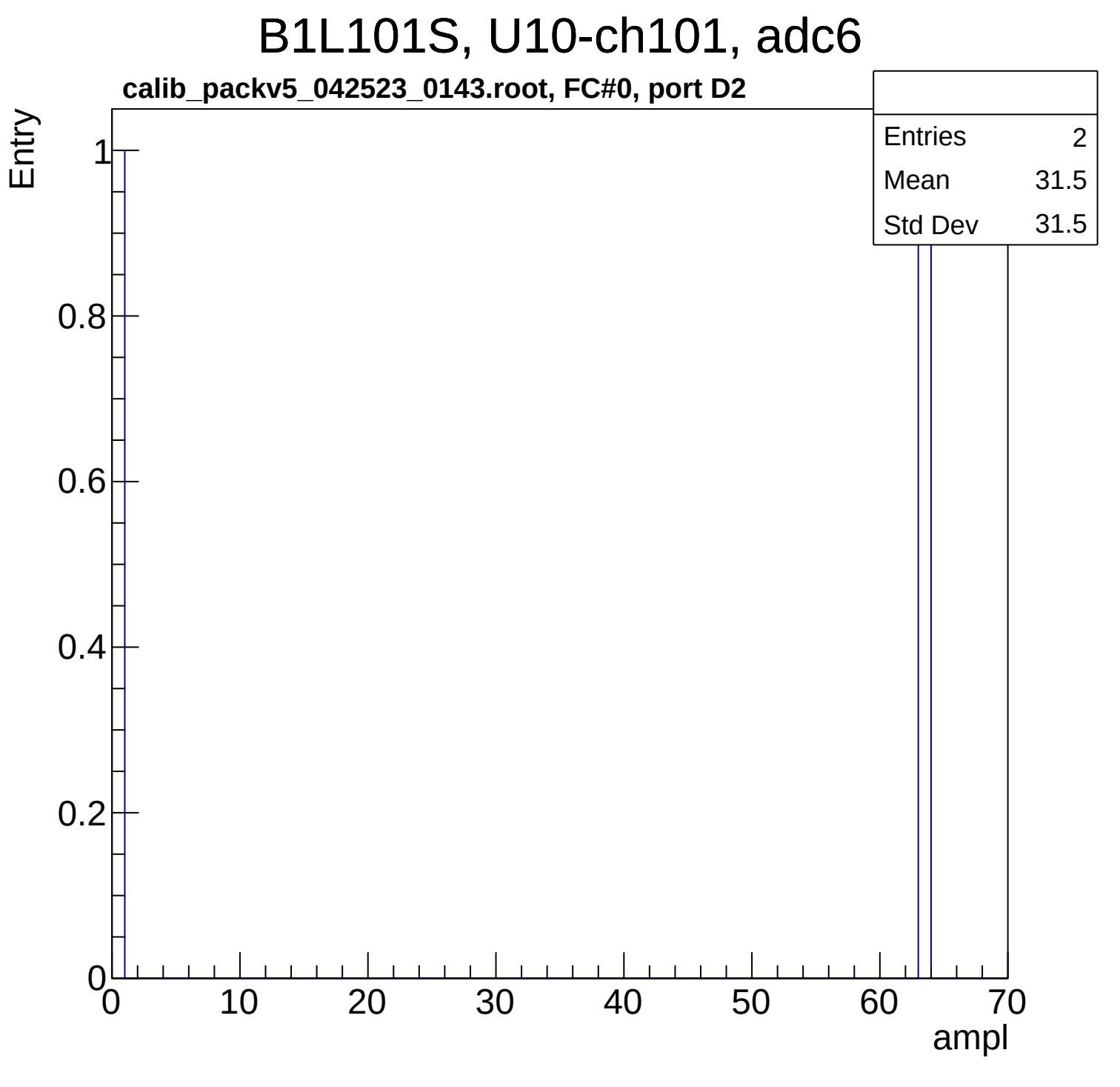
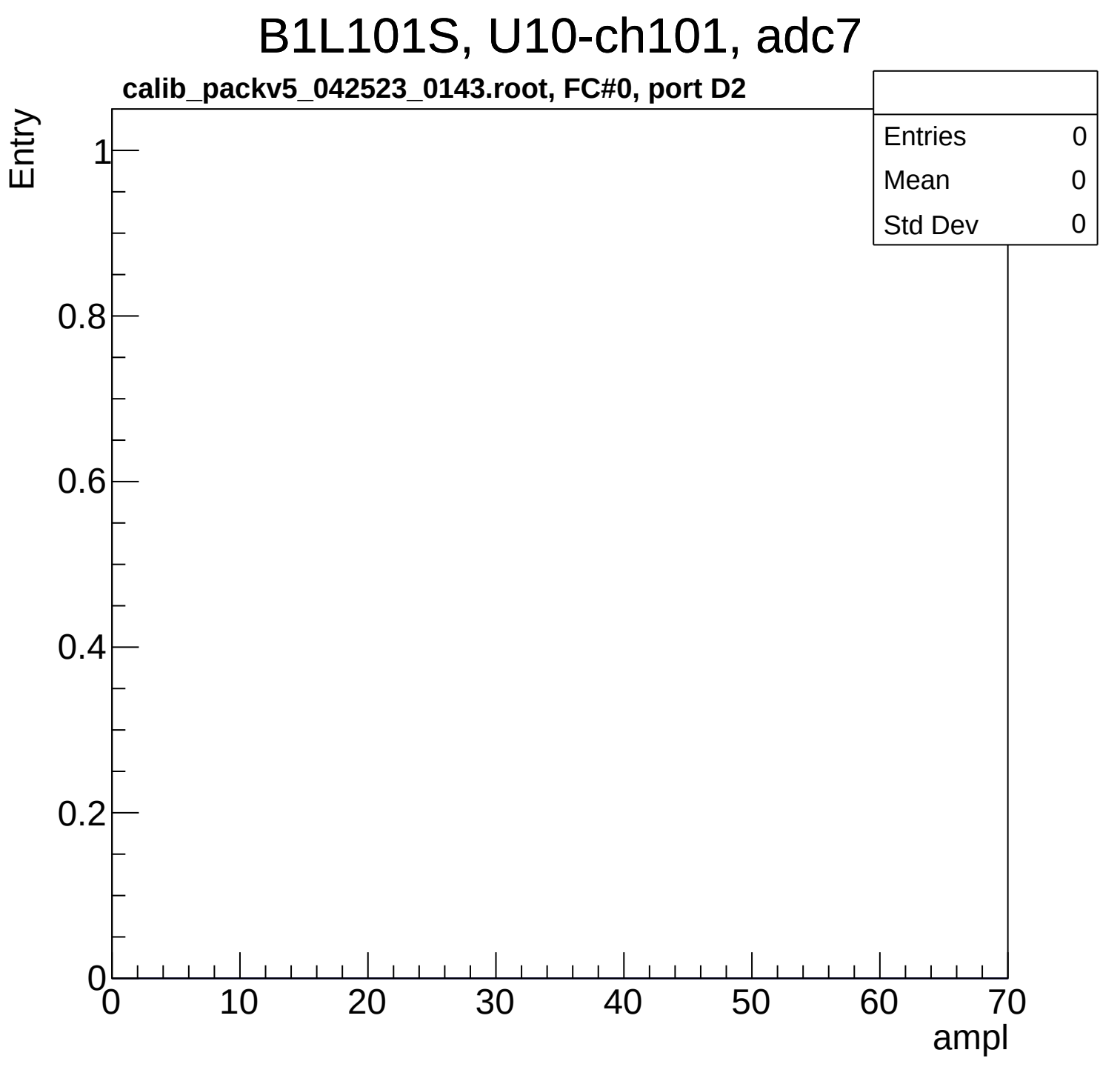

B1L101S, U10-ch101, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch101, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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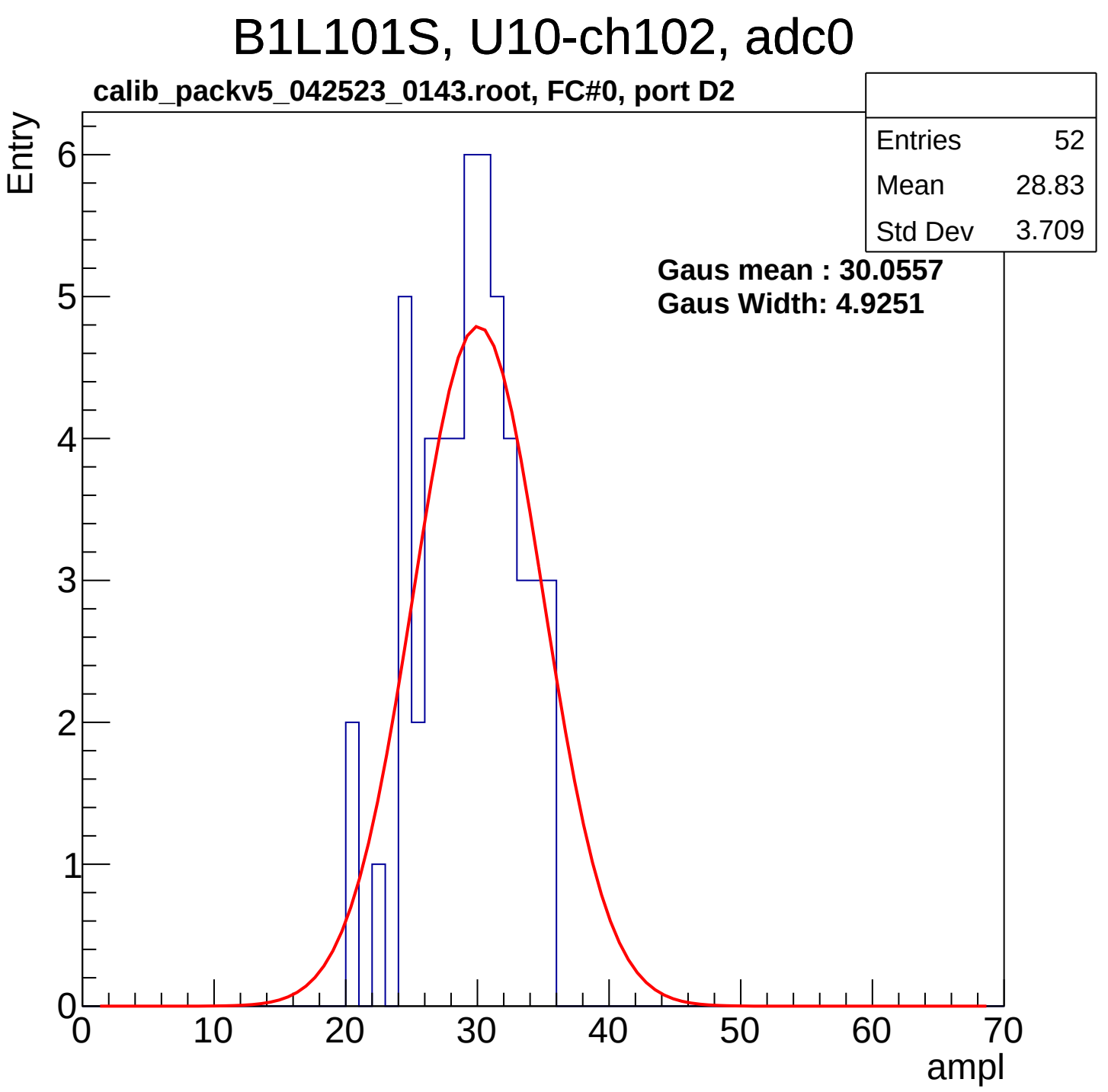
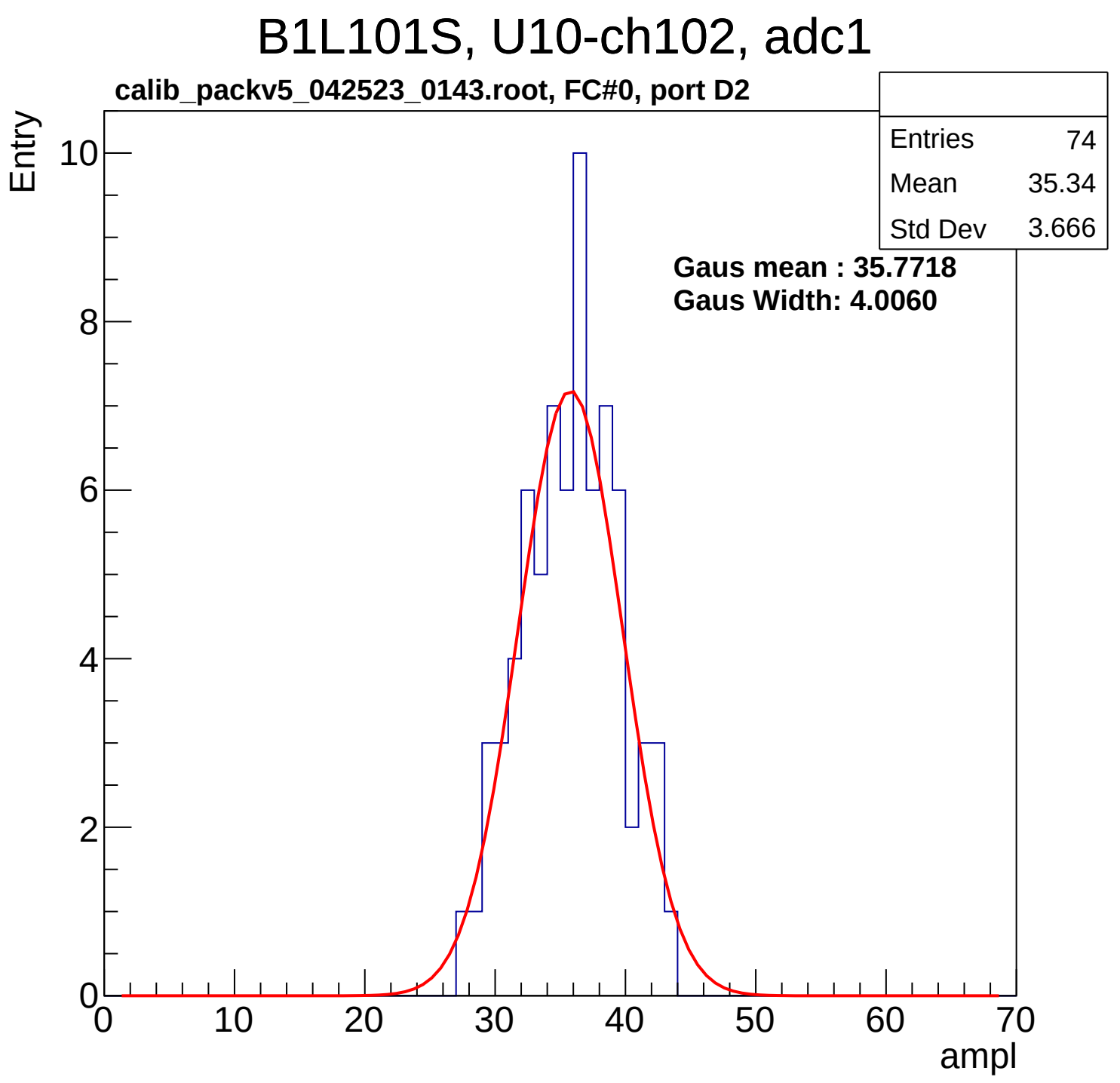
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch102, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 28.83
Std Dev 3.709
Gaus mean : 30.0557
Gaus Width: 4.9251
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L101S, U10-ch102, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 35.34
Std Dev 3.666
Gaus mean : 35.7718
Gaus Width: 4.0060
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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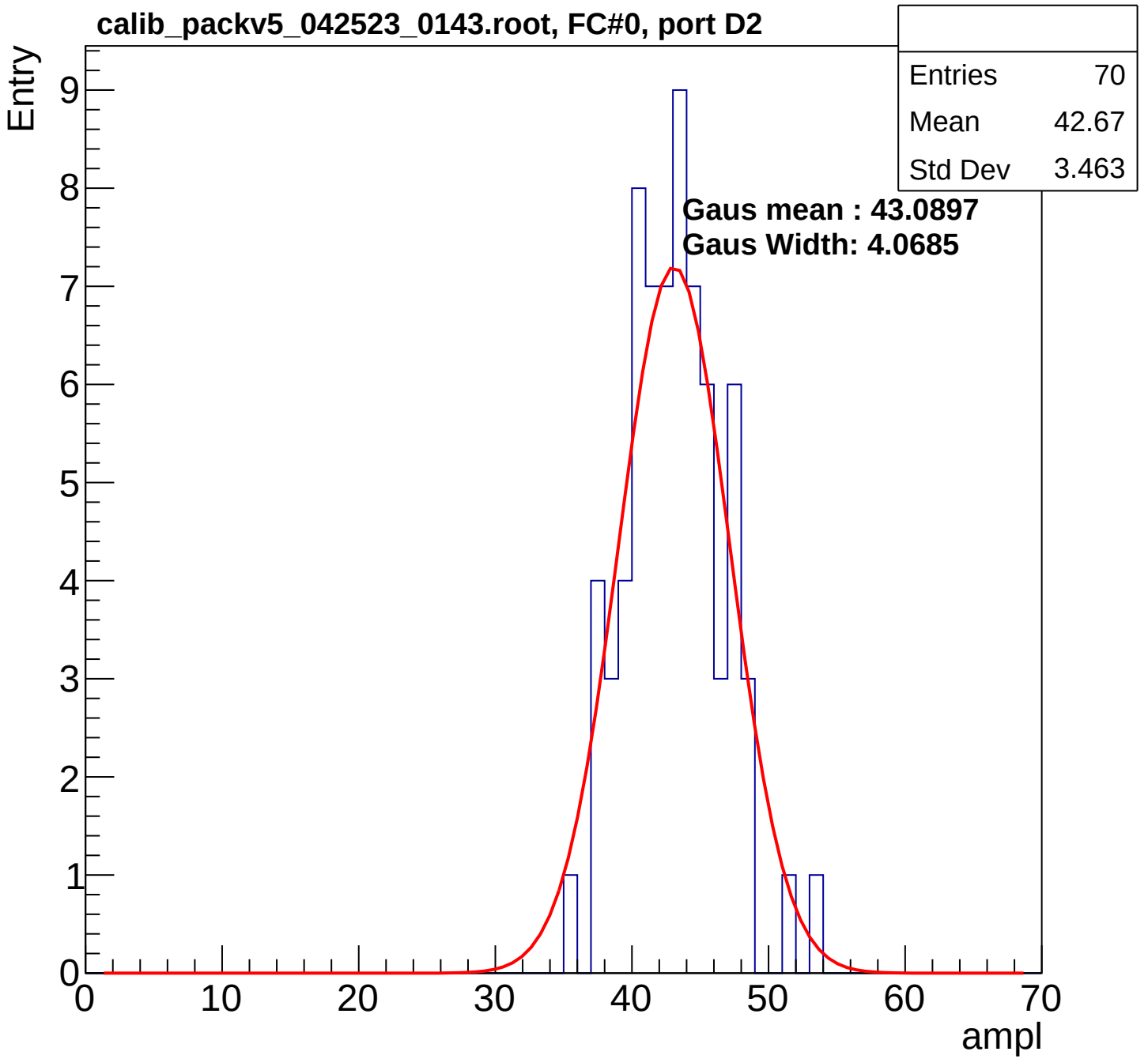
B1L101S, U10-ch102, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 42.67
Std Dev 3.463
Gaus mean : 43.0897
Gaus Width: 4.0685
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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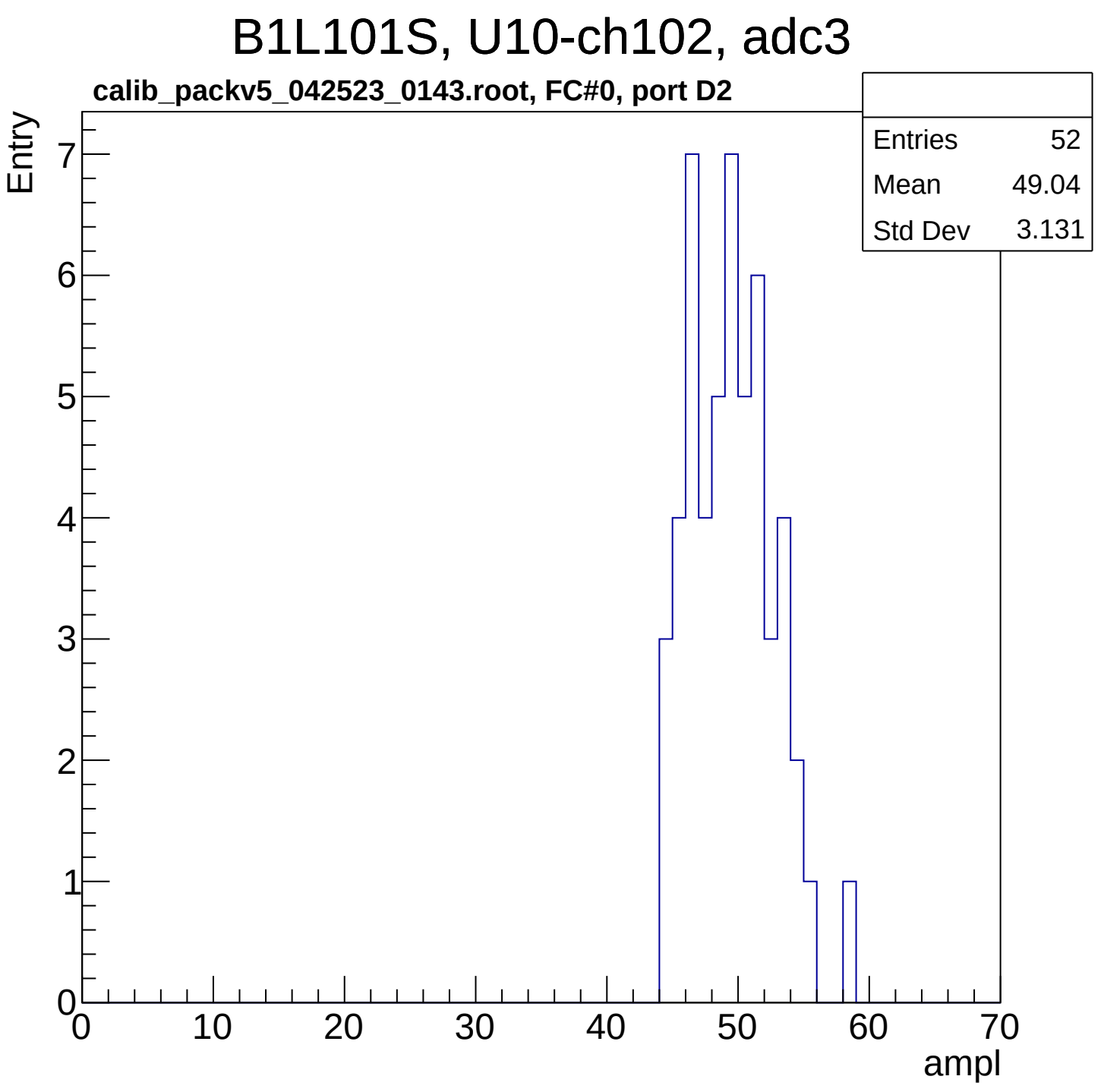
B1L101S, U10-ch102, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 49.04
Std Dev 3.131
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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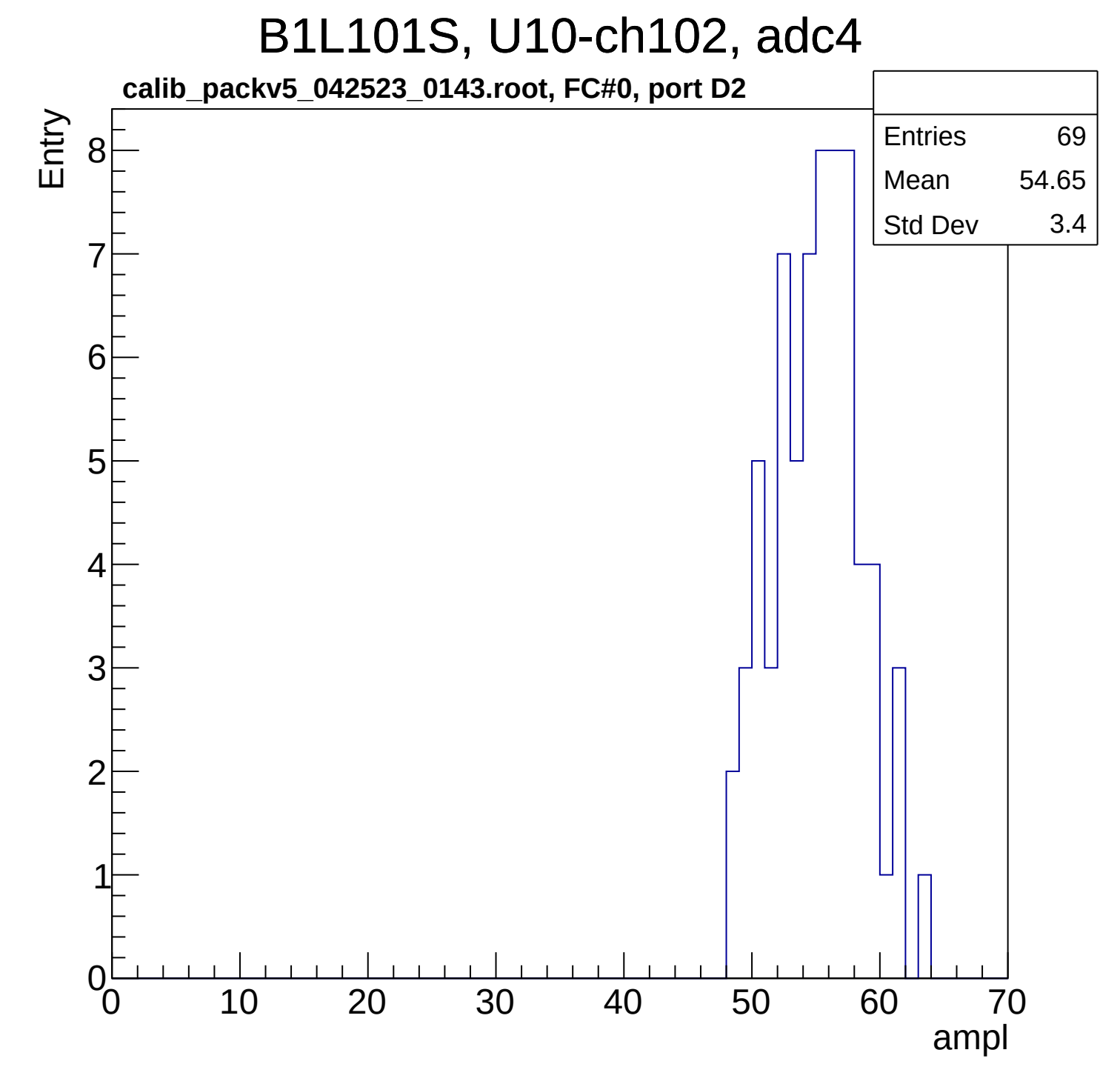
B1L101S, U10-ch102, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 54.65
Std Dev 3.4
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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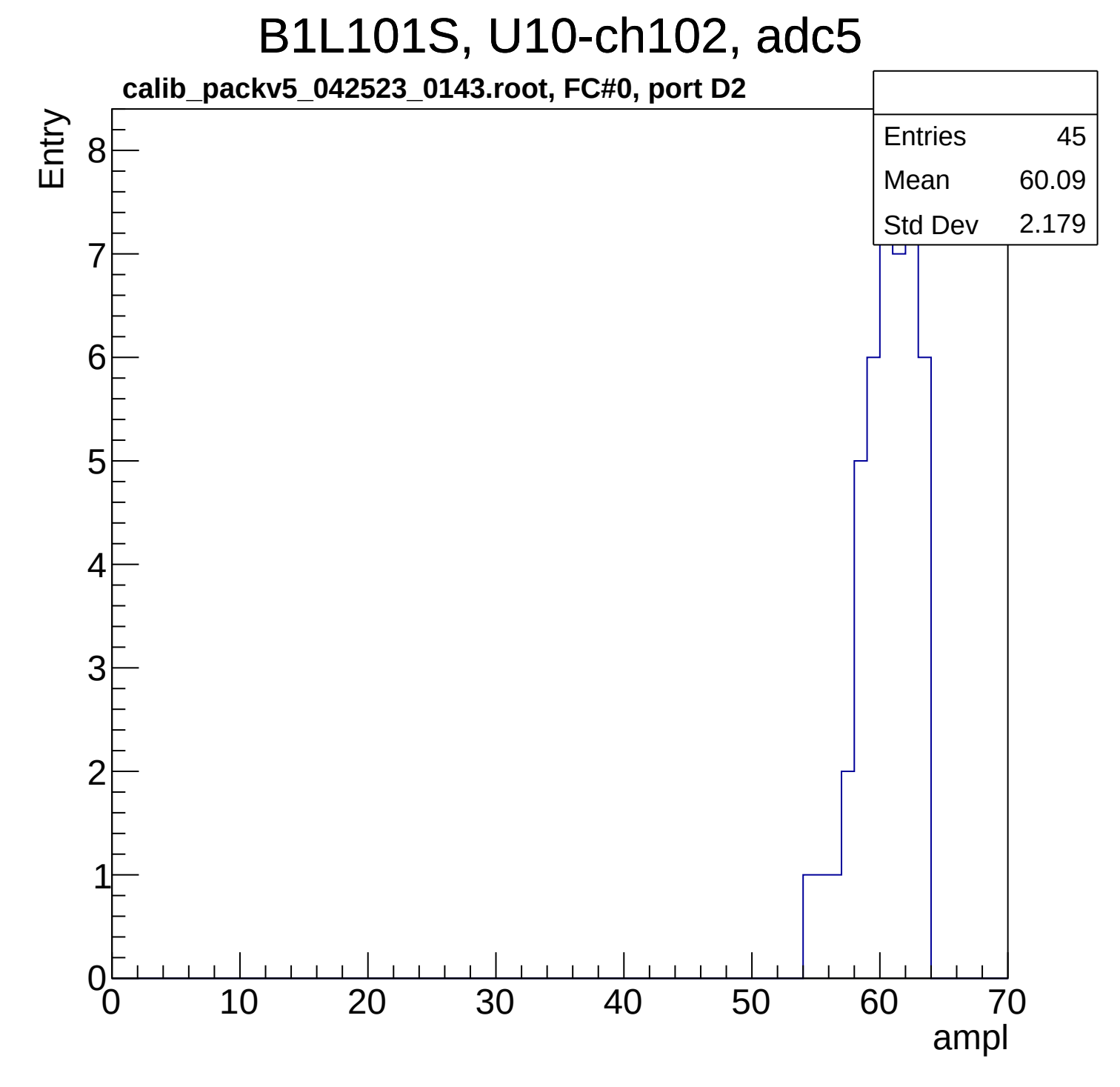
B1L101S, U10-ch102, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 60.09
Std Dev 2.179
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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60
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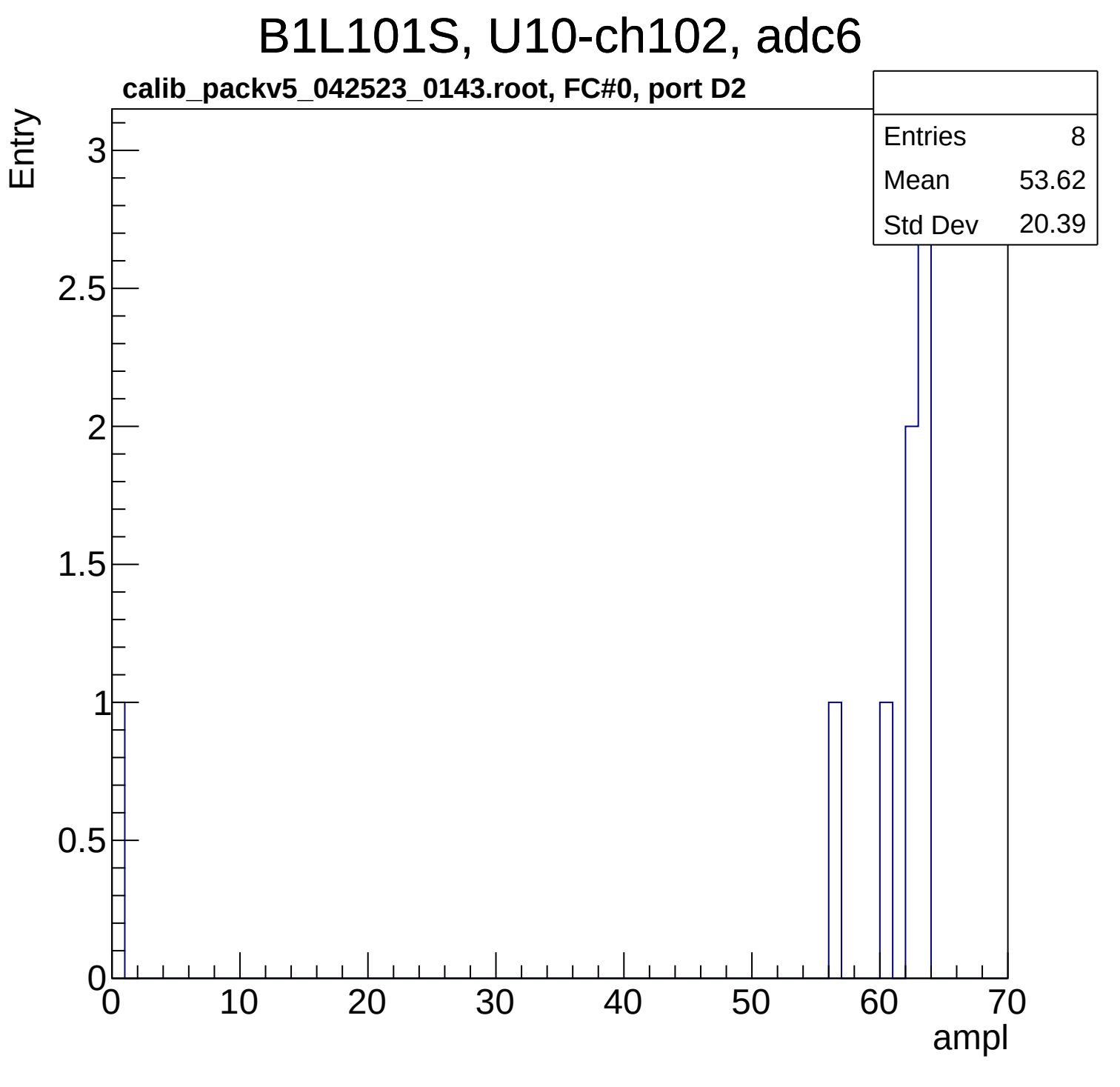
B1L101S, U10-ch102, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 53.62
Std Dev 20.39
Entry
ampl
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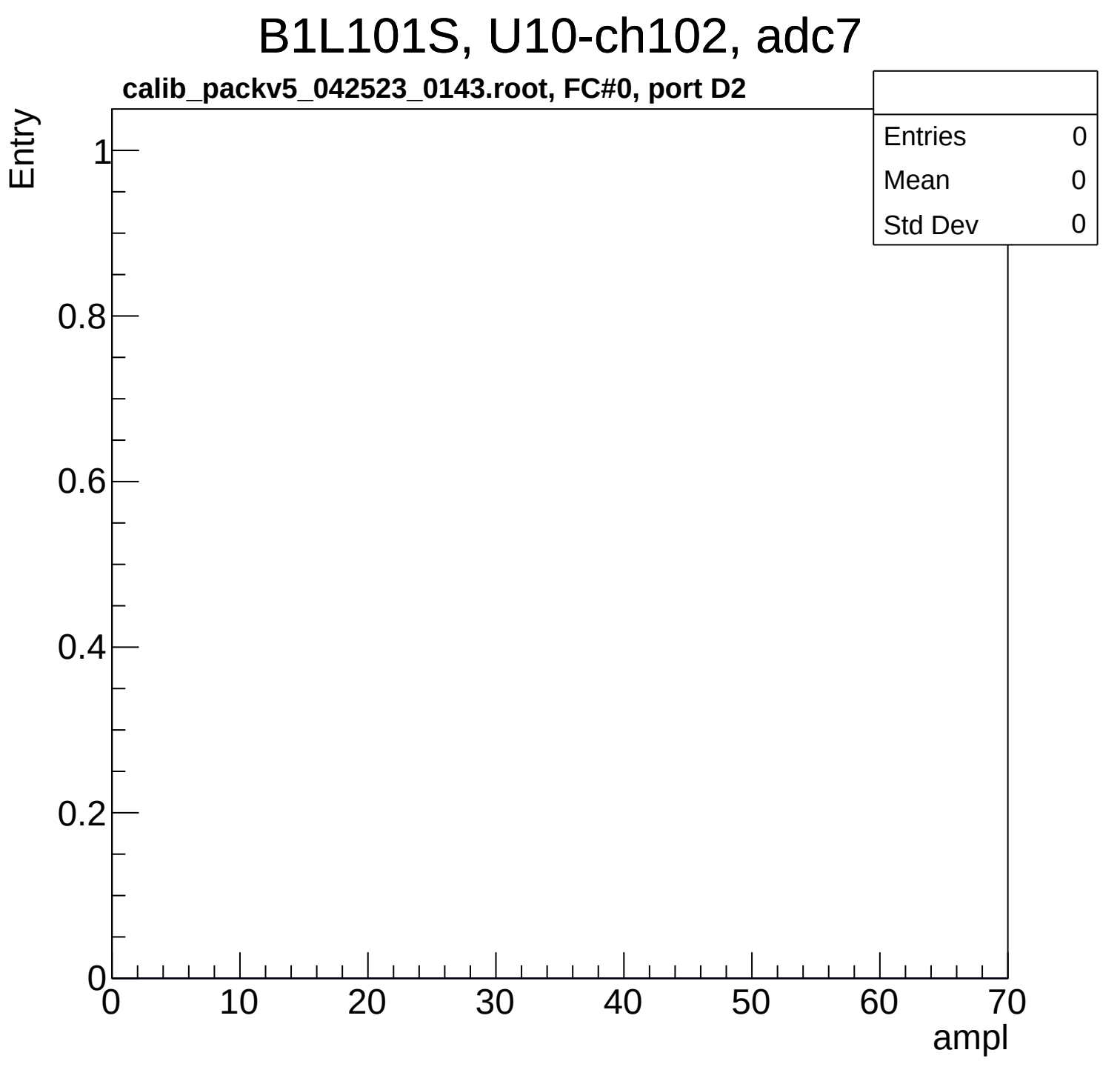
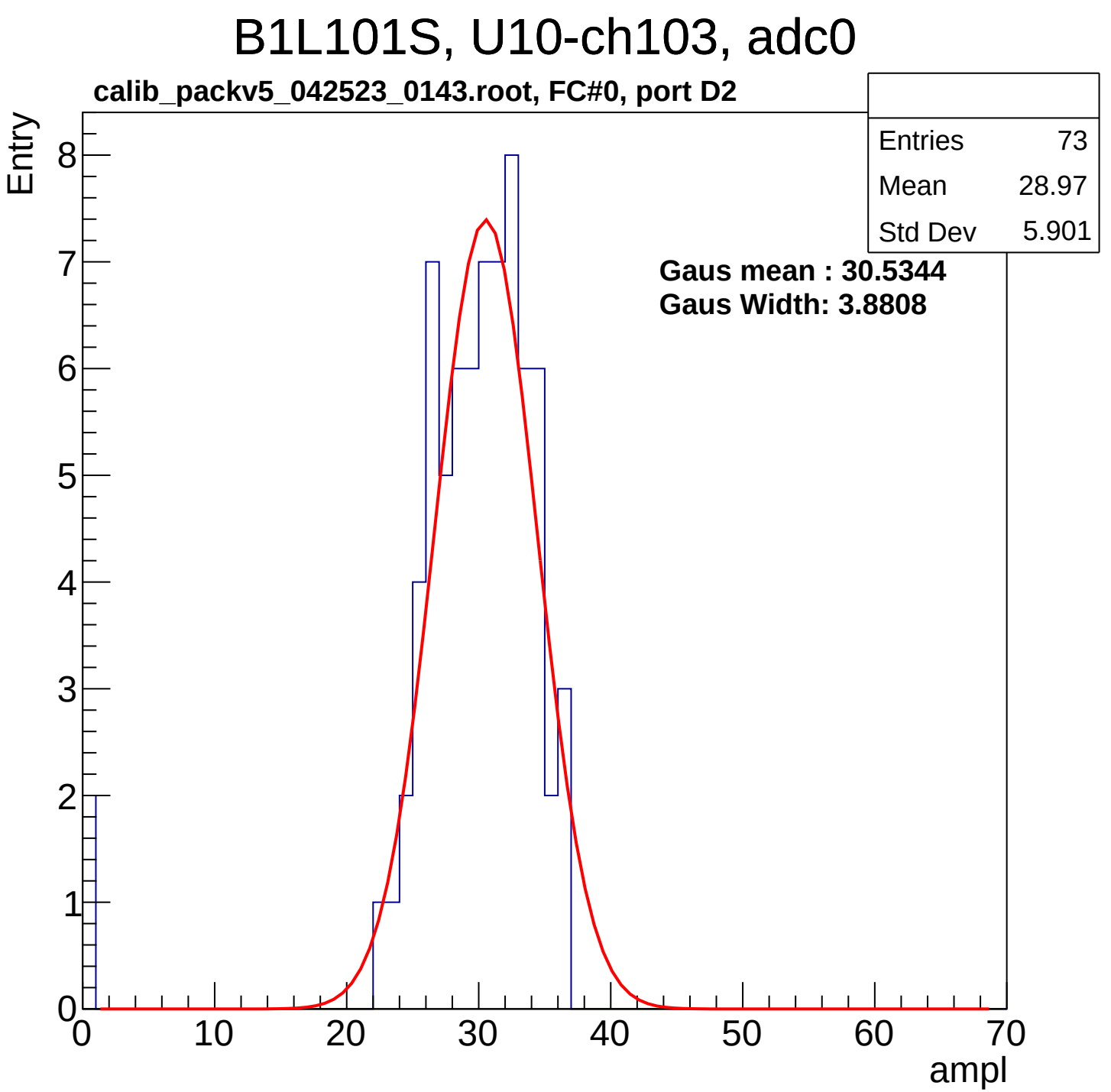
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U10-ch102, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch103, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 28.97
Std Dev 5.901
Gaus mean : 30.5344
Gaus Width: 3.8808
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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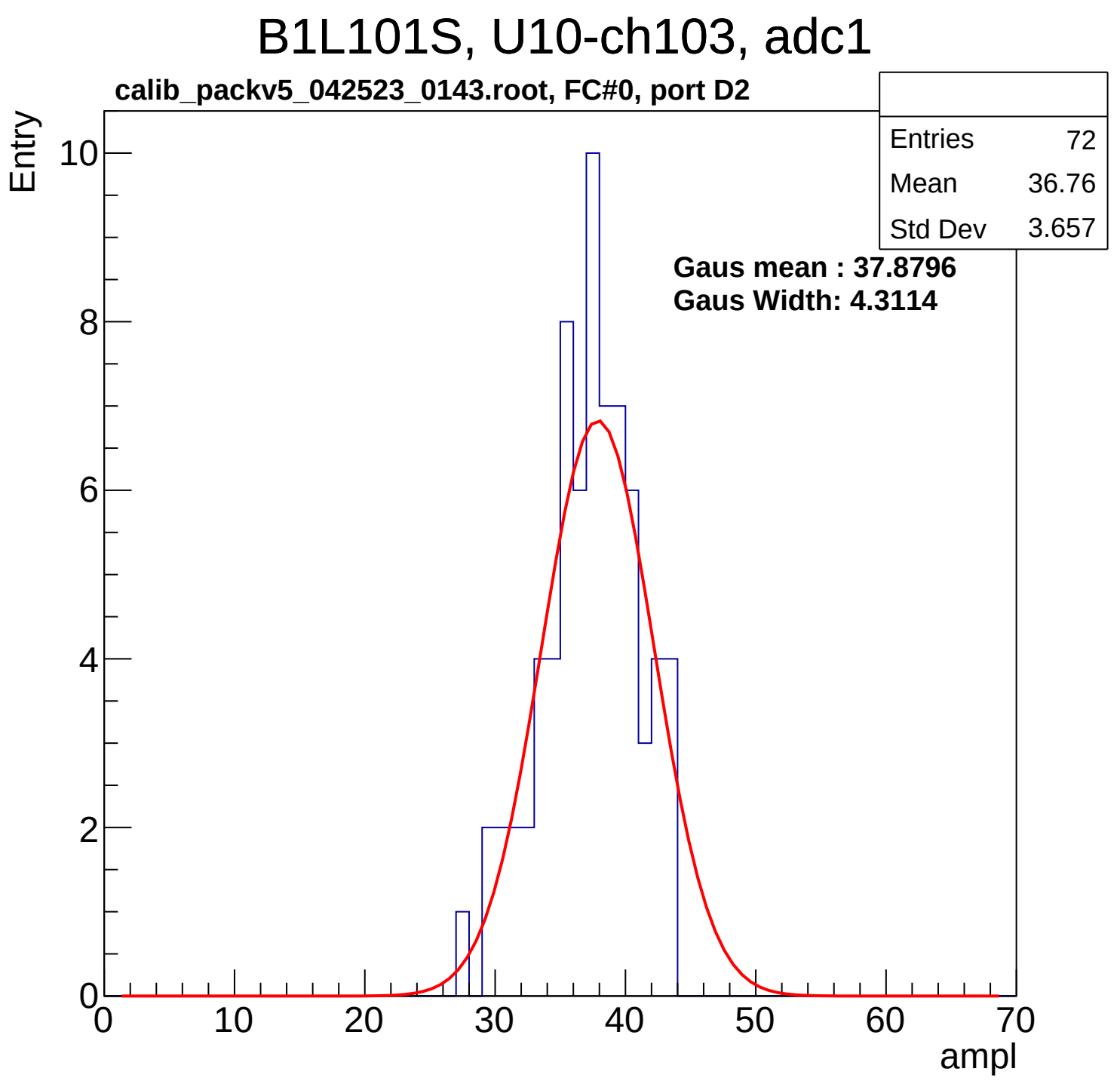
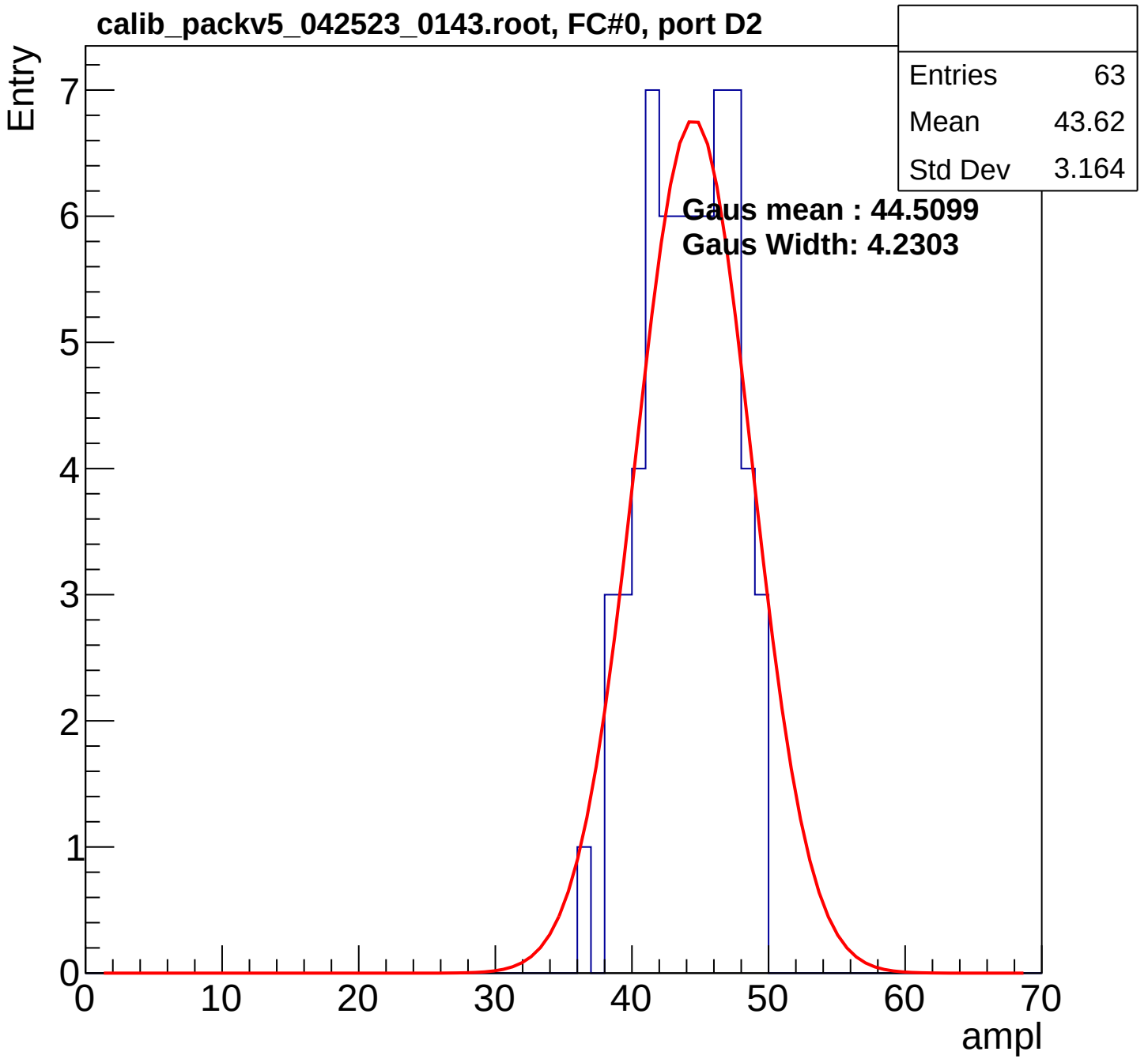
40
50
60
70


B1L101S, U10-ch103, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 36.76
Std Dev 3.657
Gaus mean : 37.8796
Gaus Width: 4.3114
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch103, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 43.62
Std Dev 3.164
Gaus mean : 44.5099
Gaus Width: 4.2303
Entry
ampl
0
1
2
3
4
5
6
7
0
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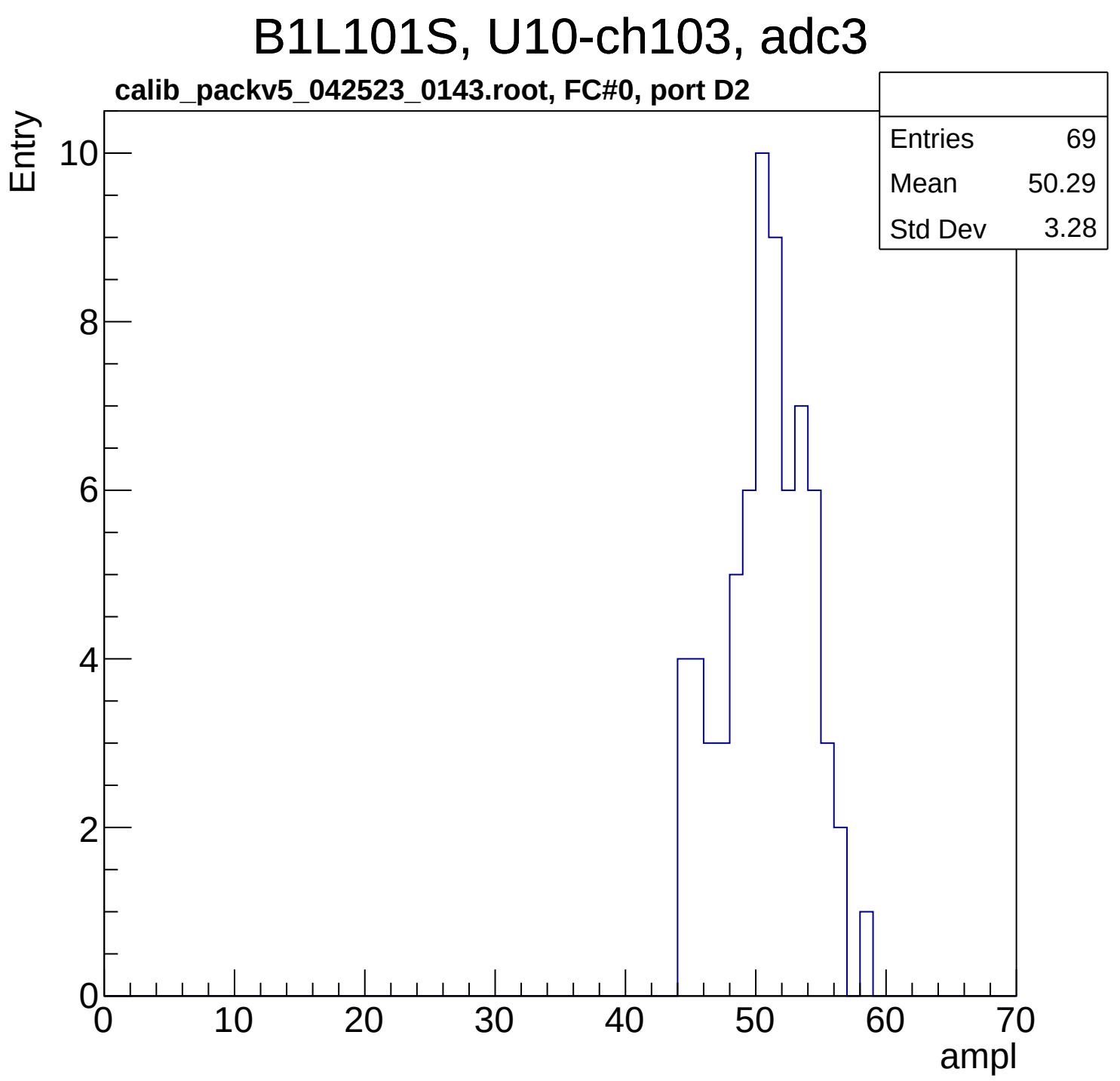
60
70


B1L101S, U10-ch103, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 50.29
Std Dev 3.28
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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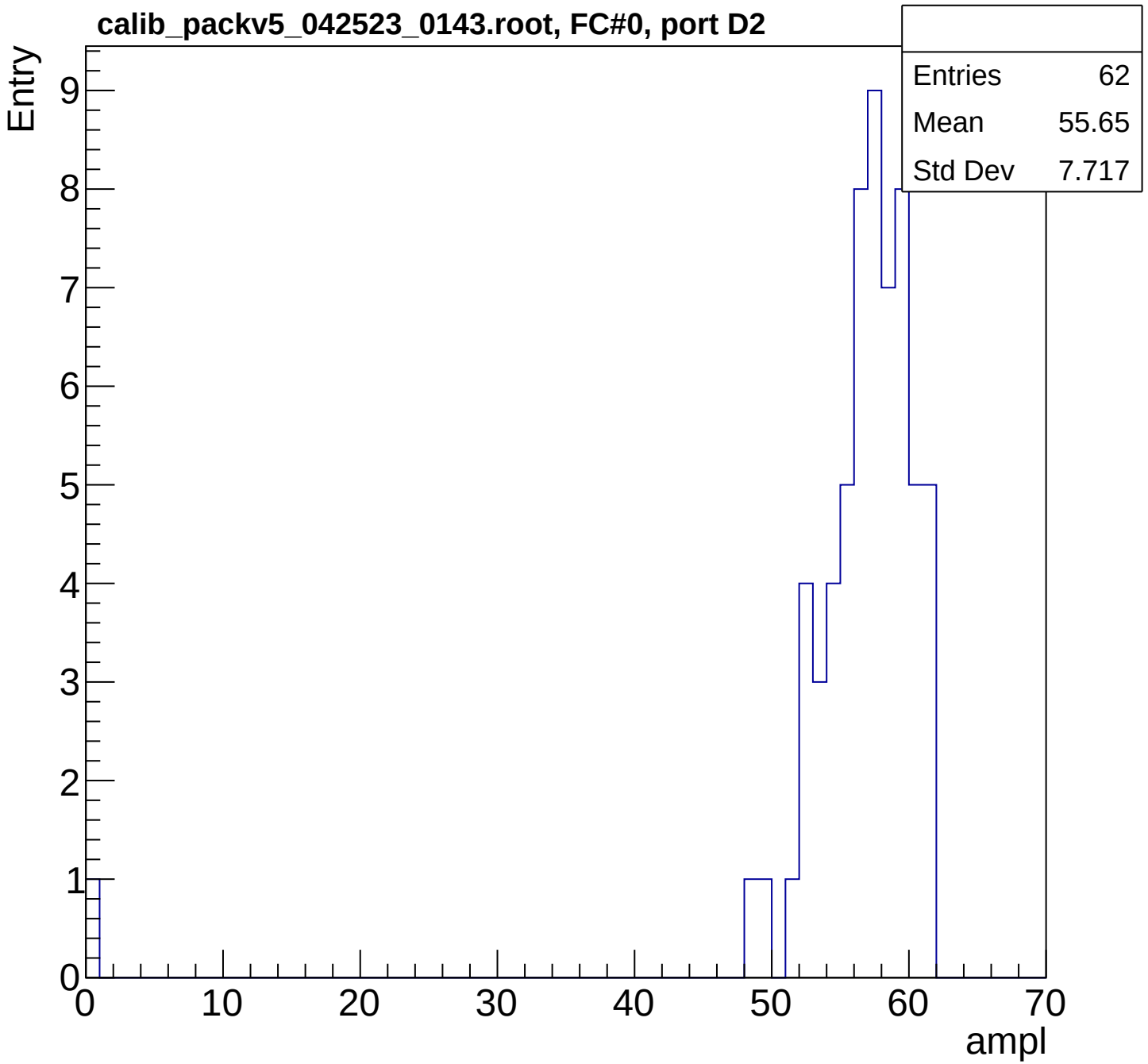
B1L101S, U10-ch103, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 55.65
Std Dev 7.717
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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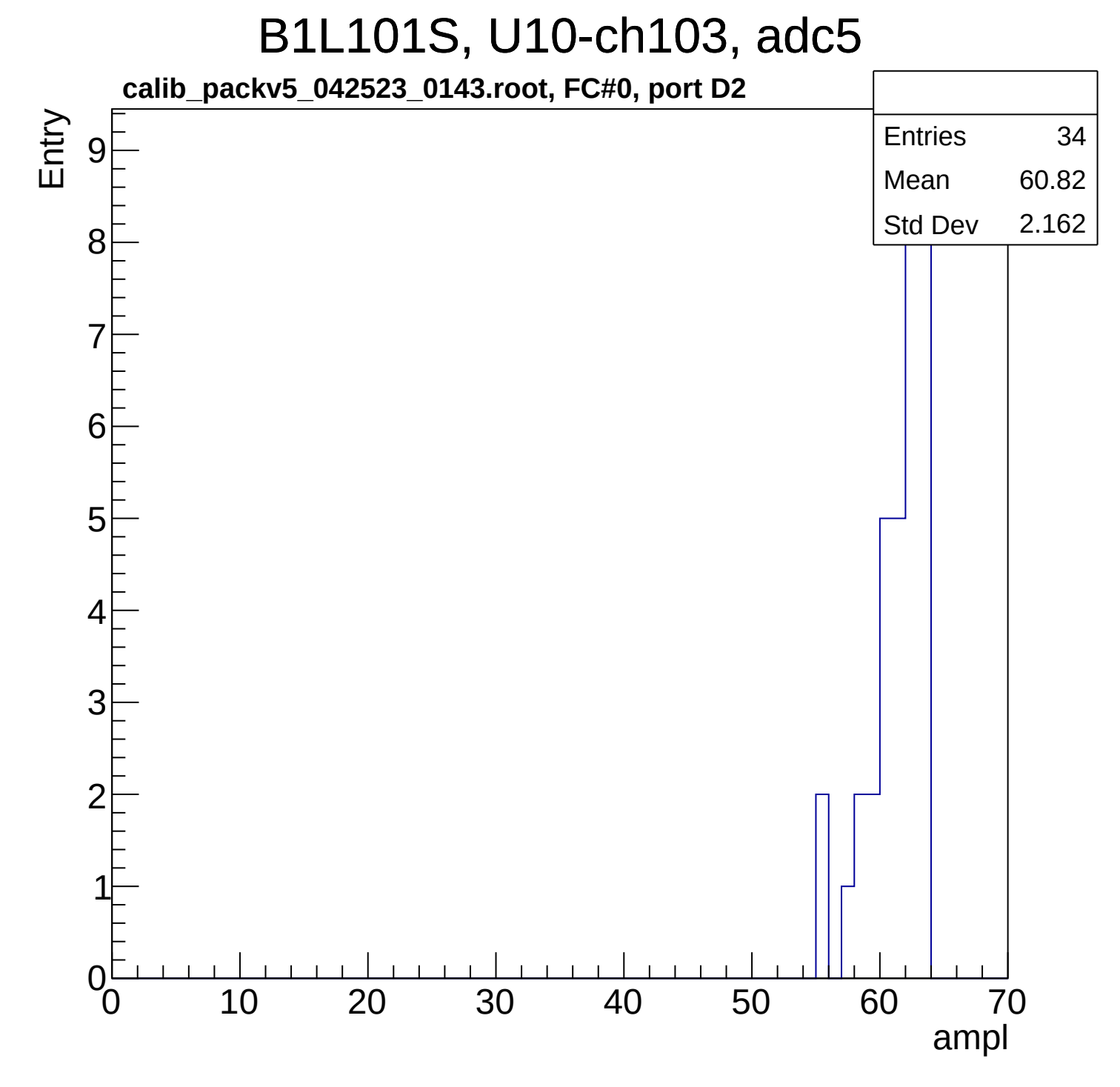
B1L101S, U10-ch103, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 34
Mean 60.82
Std Dev 2.162
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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60
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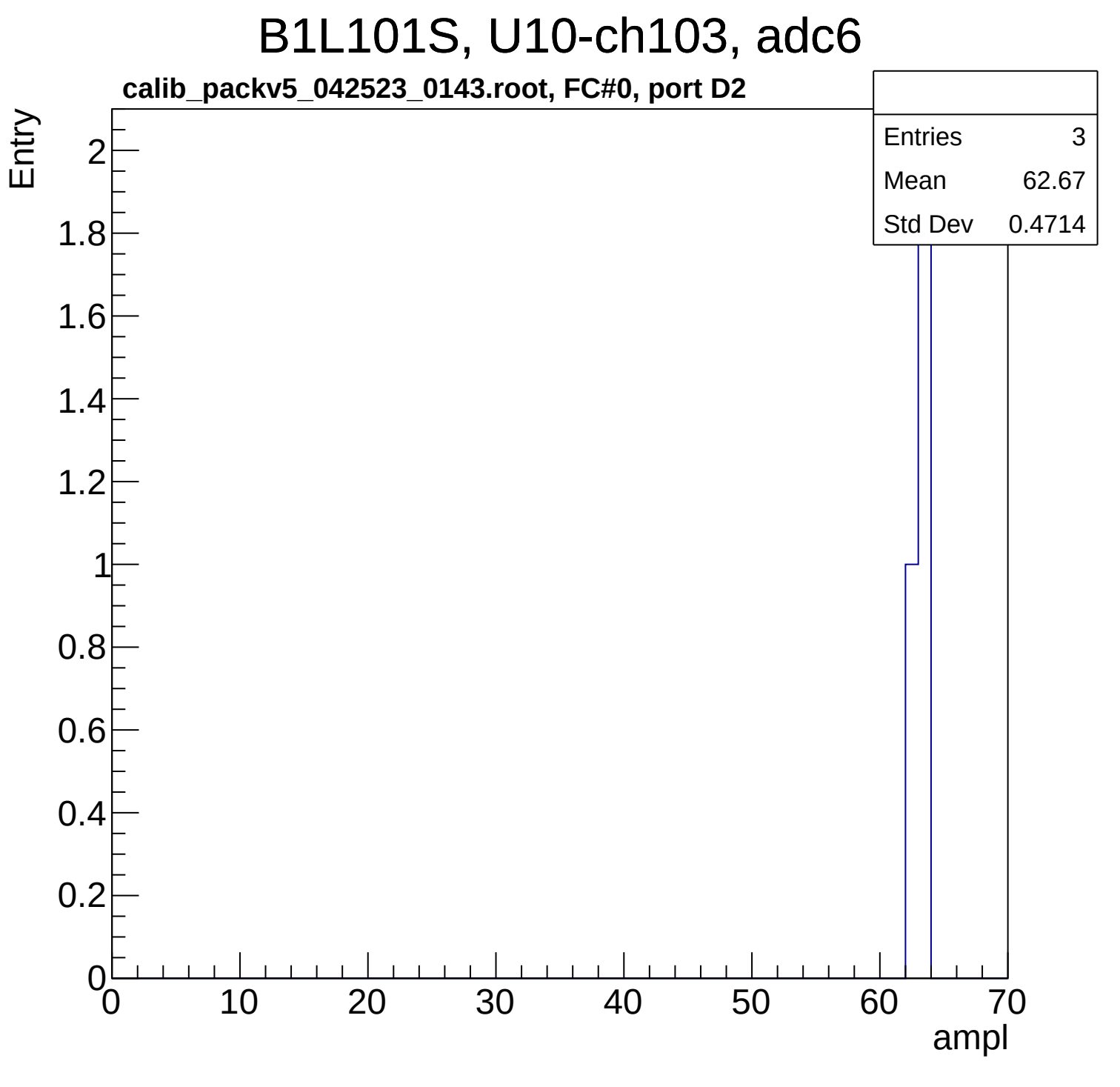
B1L101S, U10-ch103, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
50
60
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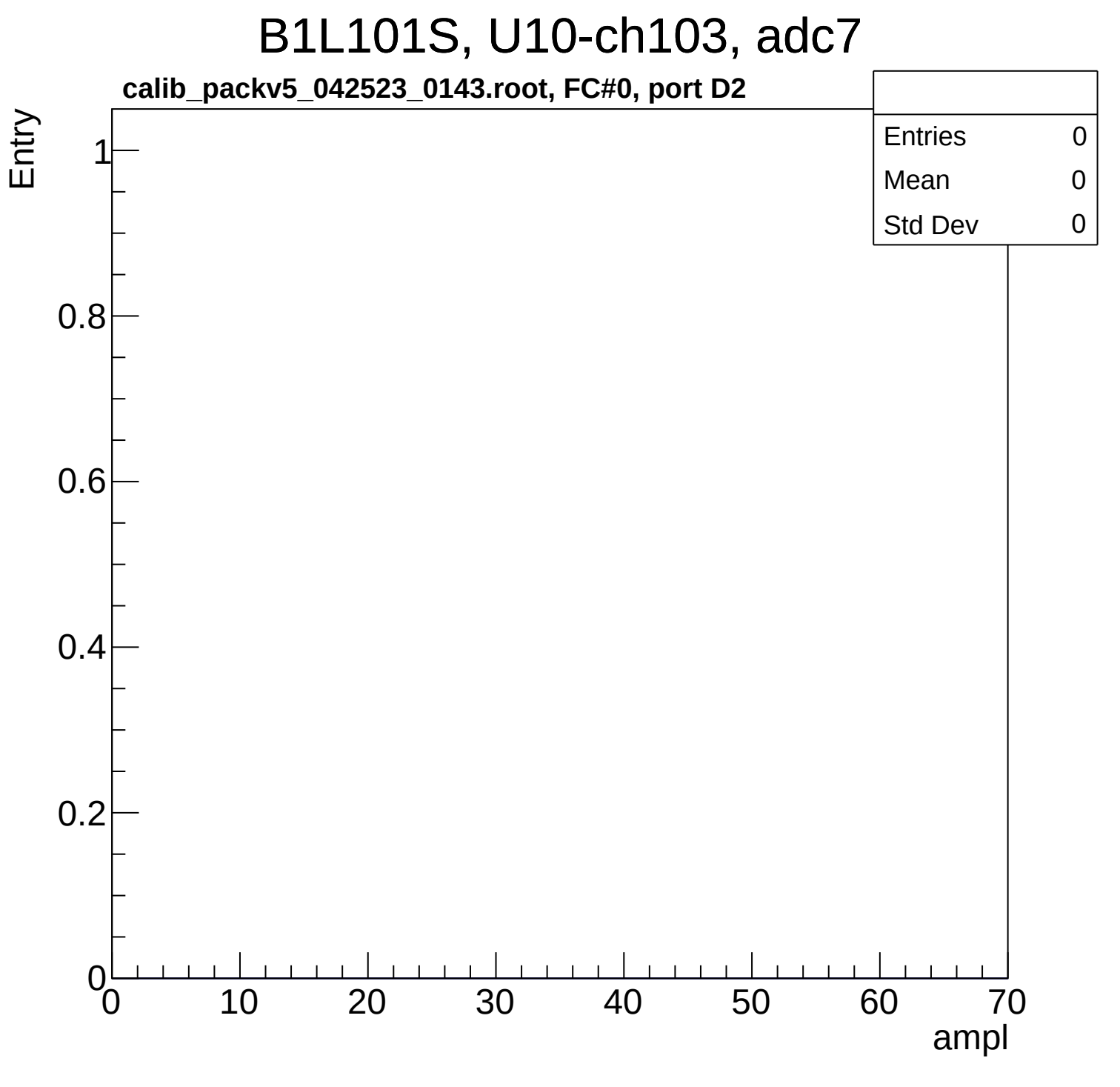
B1L101S, U10-ch103, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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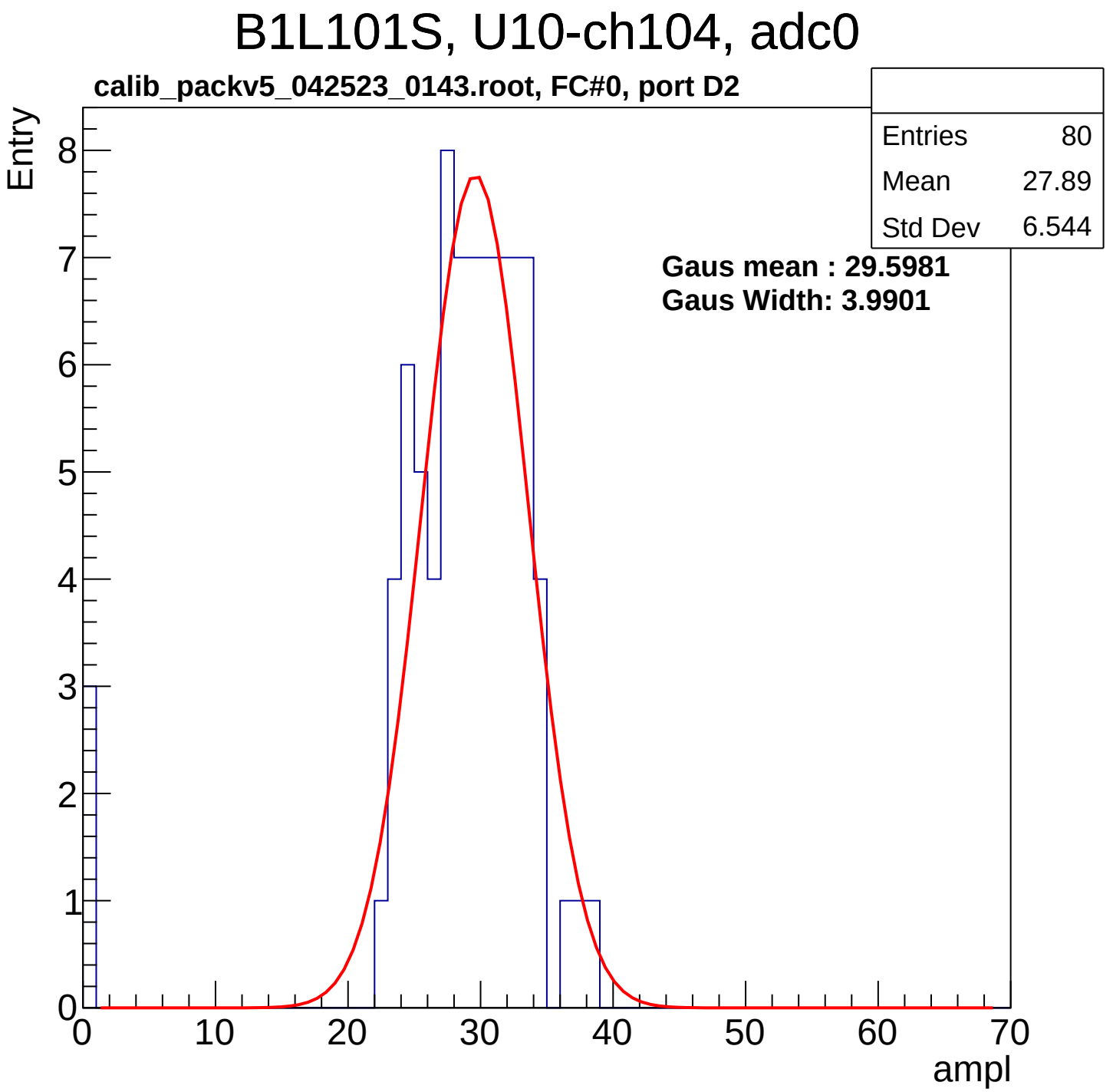
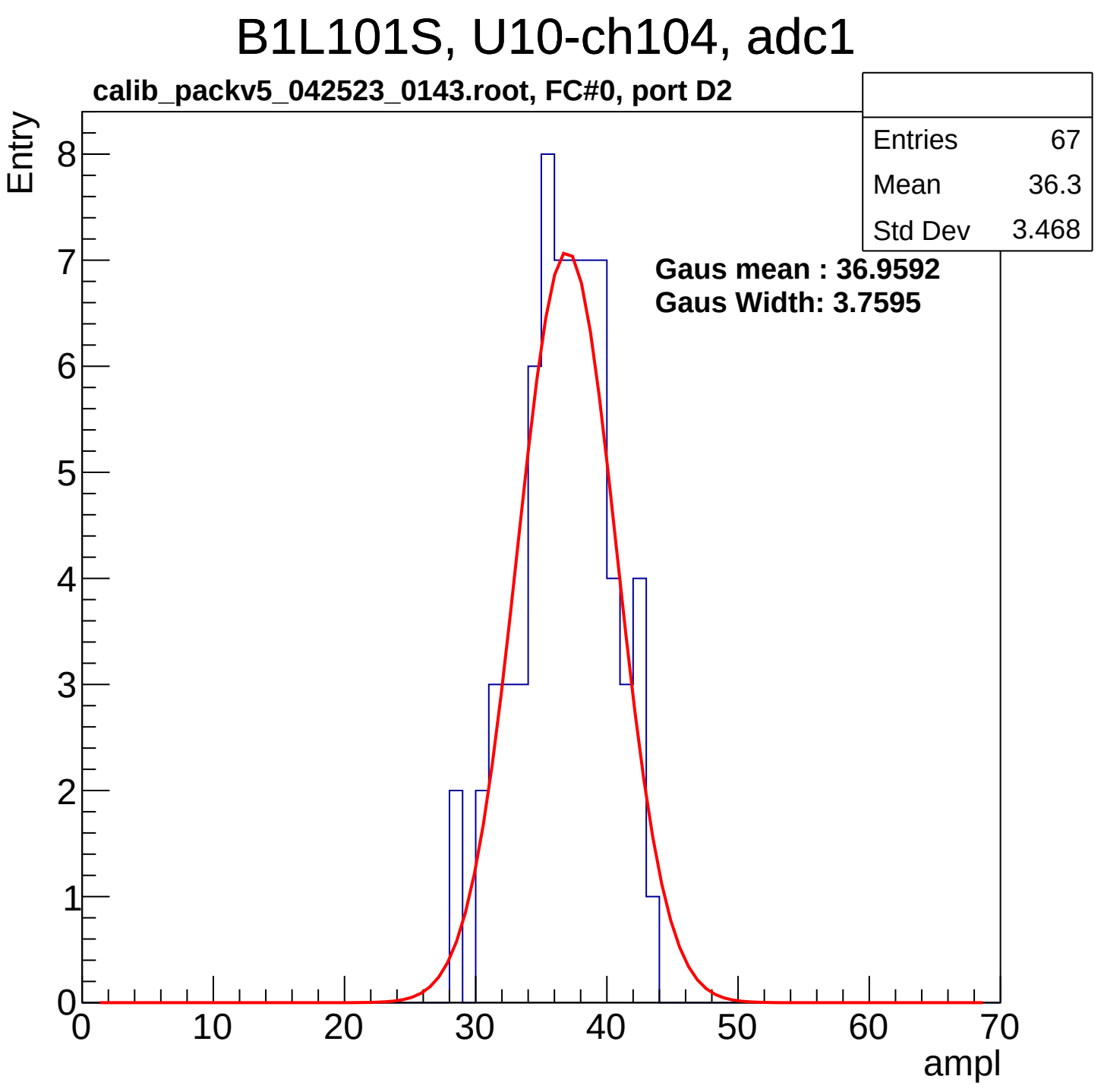
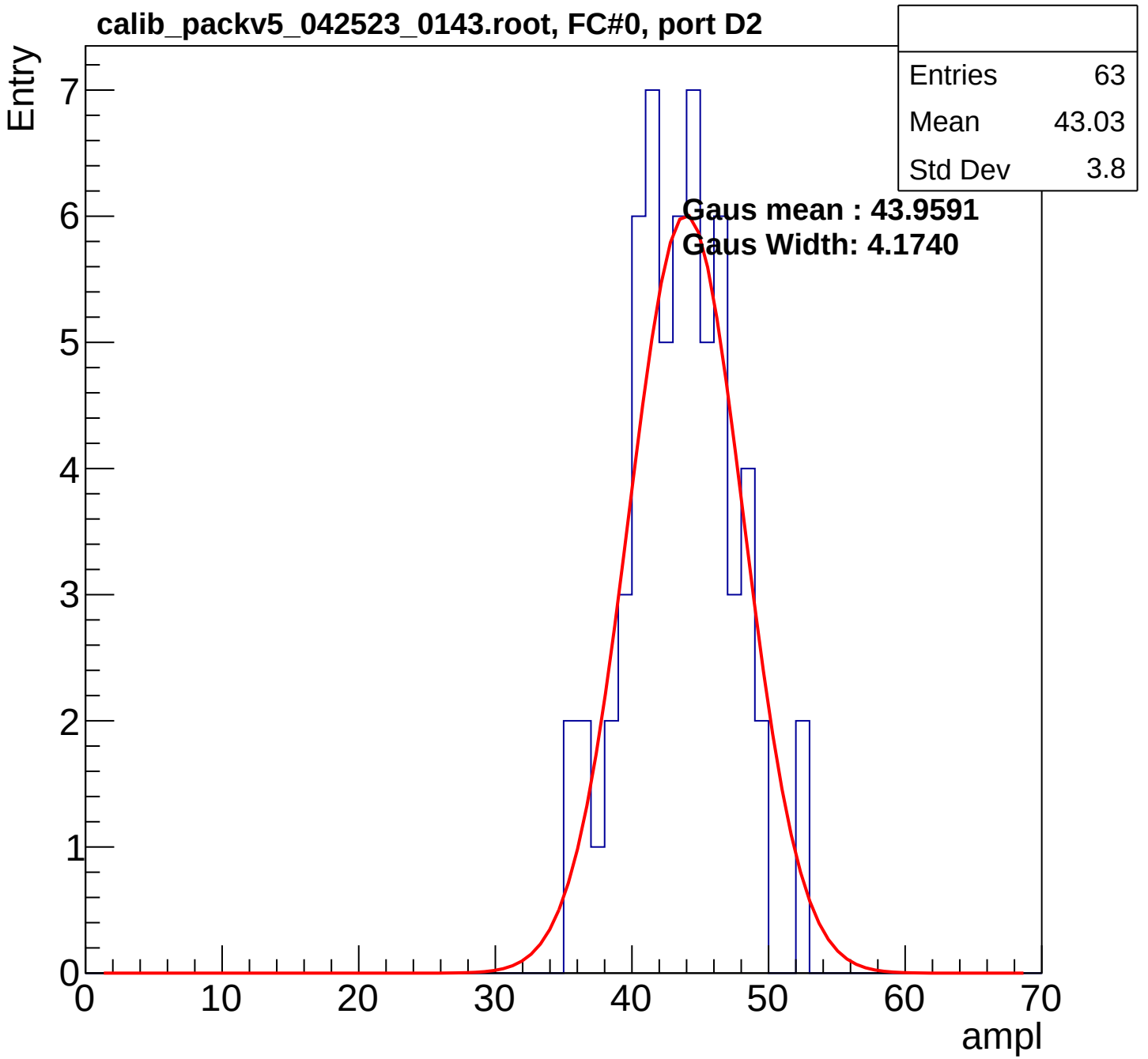
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch104, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 80
Mean 27.89
Std Dev 6.544
Gaus mean : 29.5981
Gaus Width: 3.9901
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch104, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 36.3
Std Dev 3.468
Gaus mean : 36.9592
Gaus Width: 3.7595
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch104, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 43.03
Std Dev 3.8
Gaus mean : 43.9591
Gaus Width: 4.1740
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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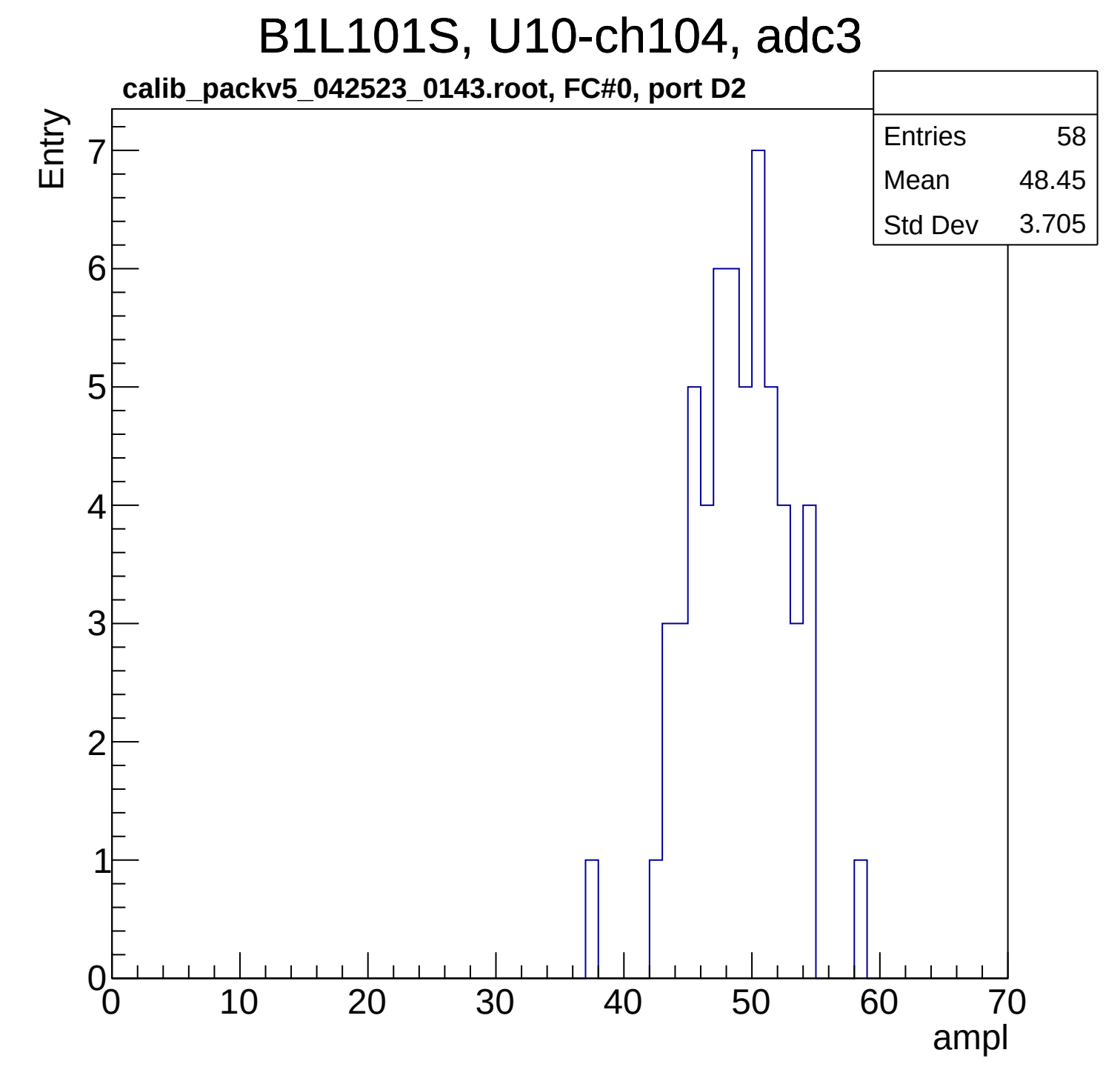
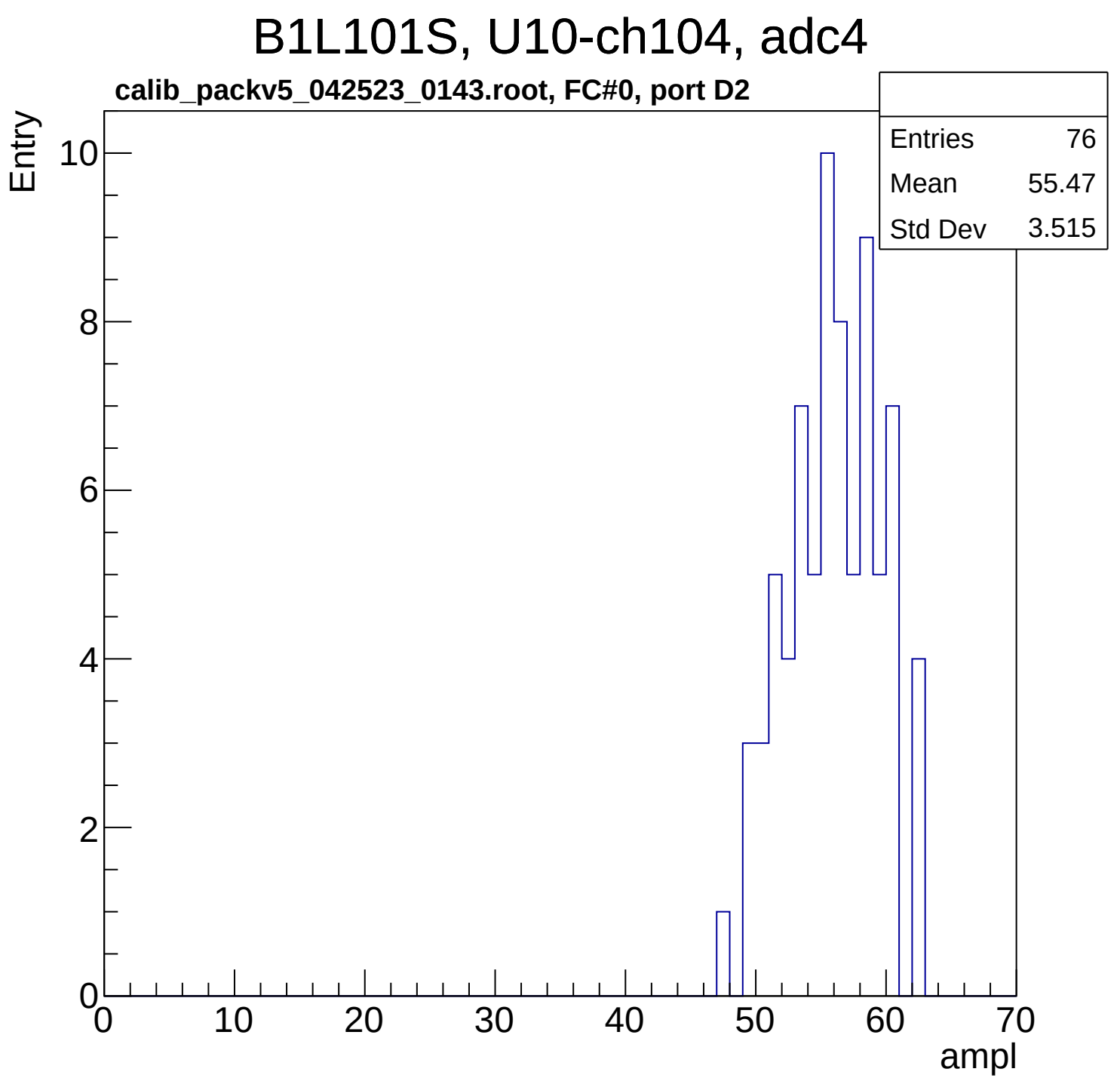
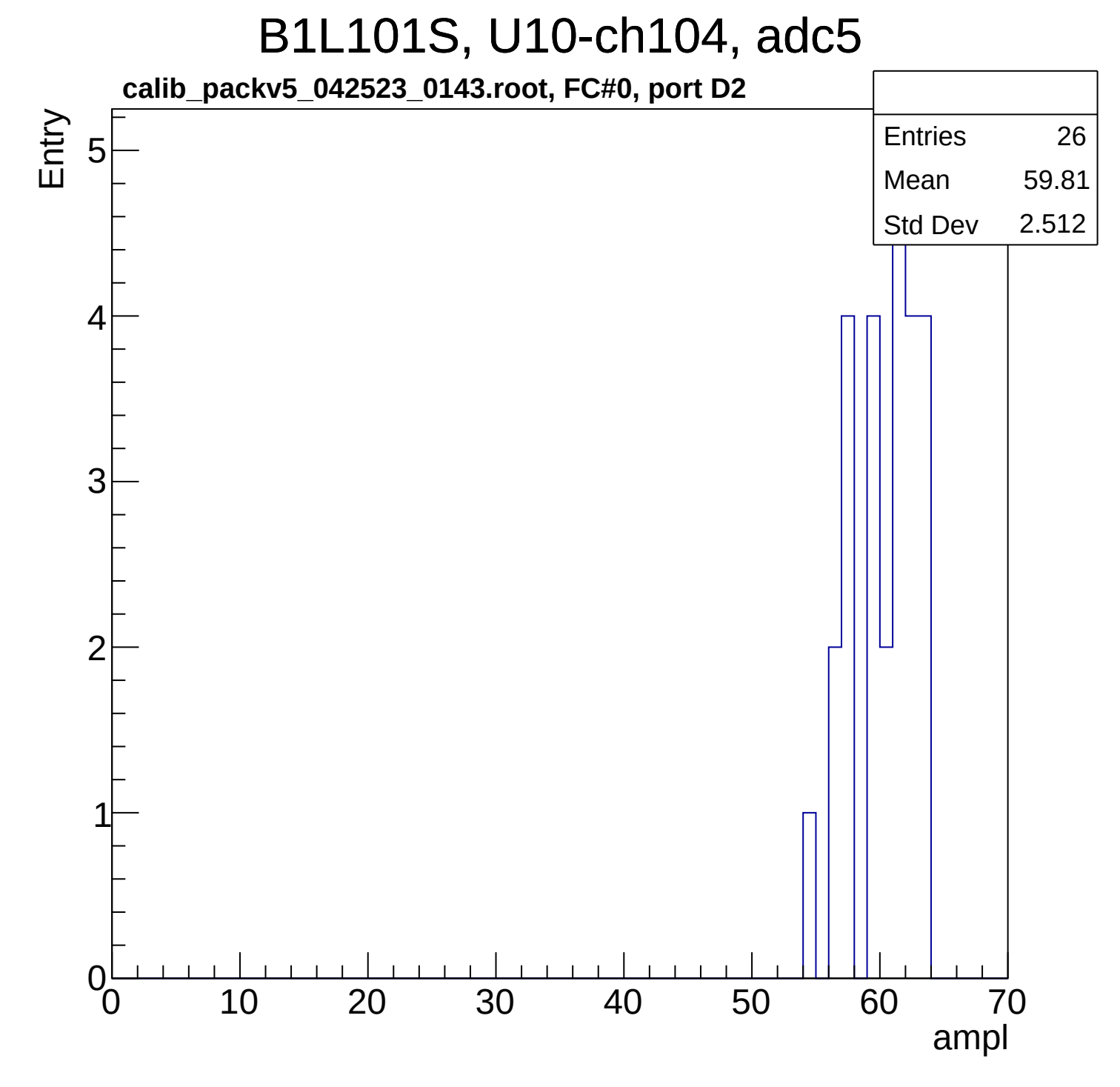
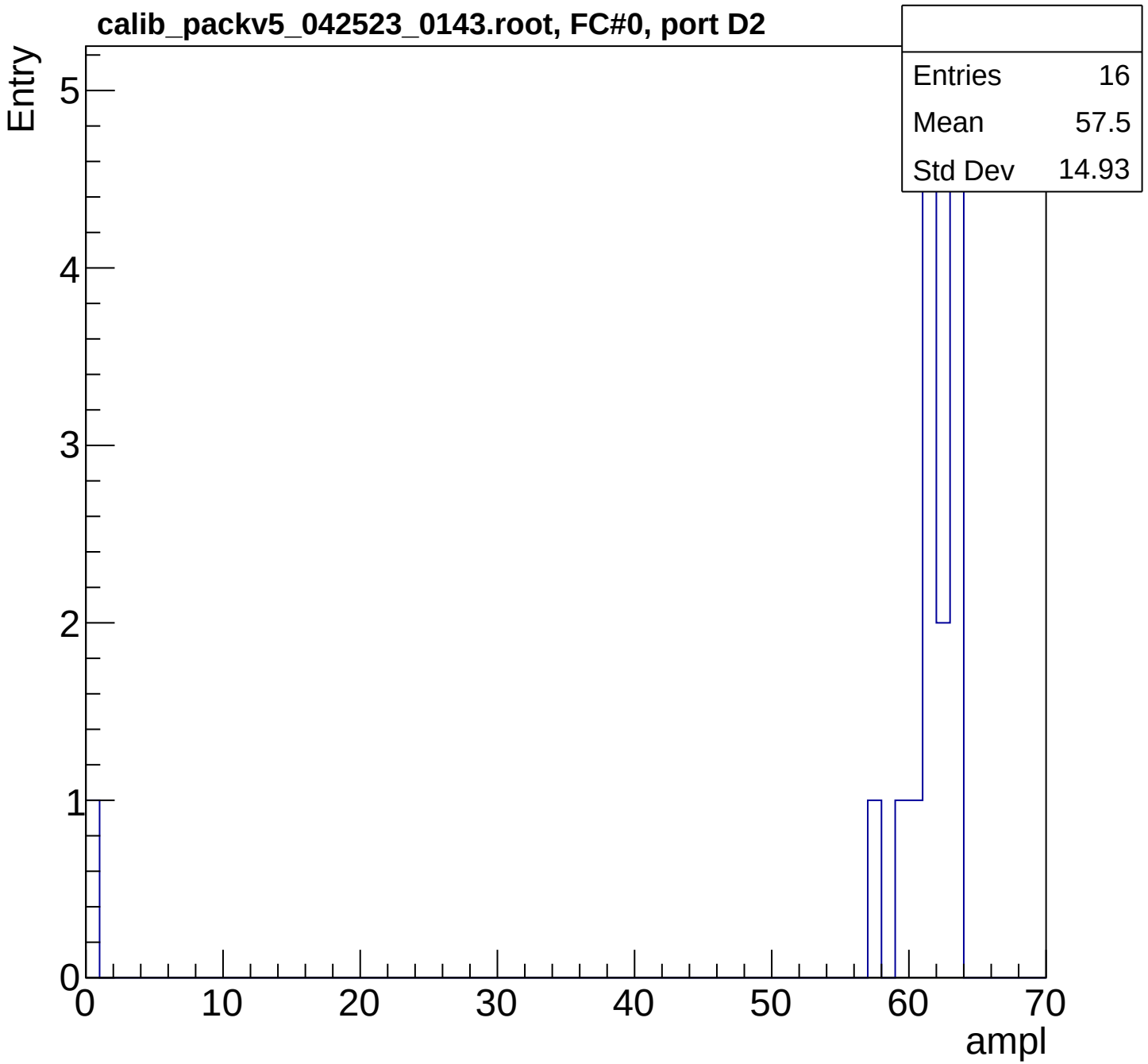
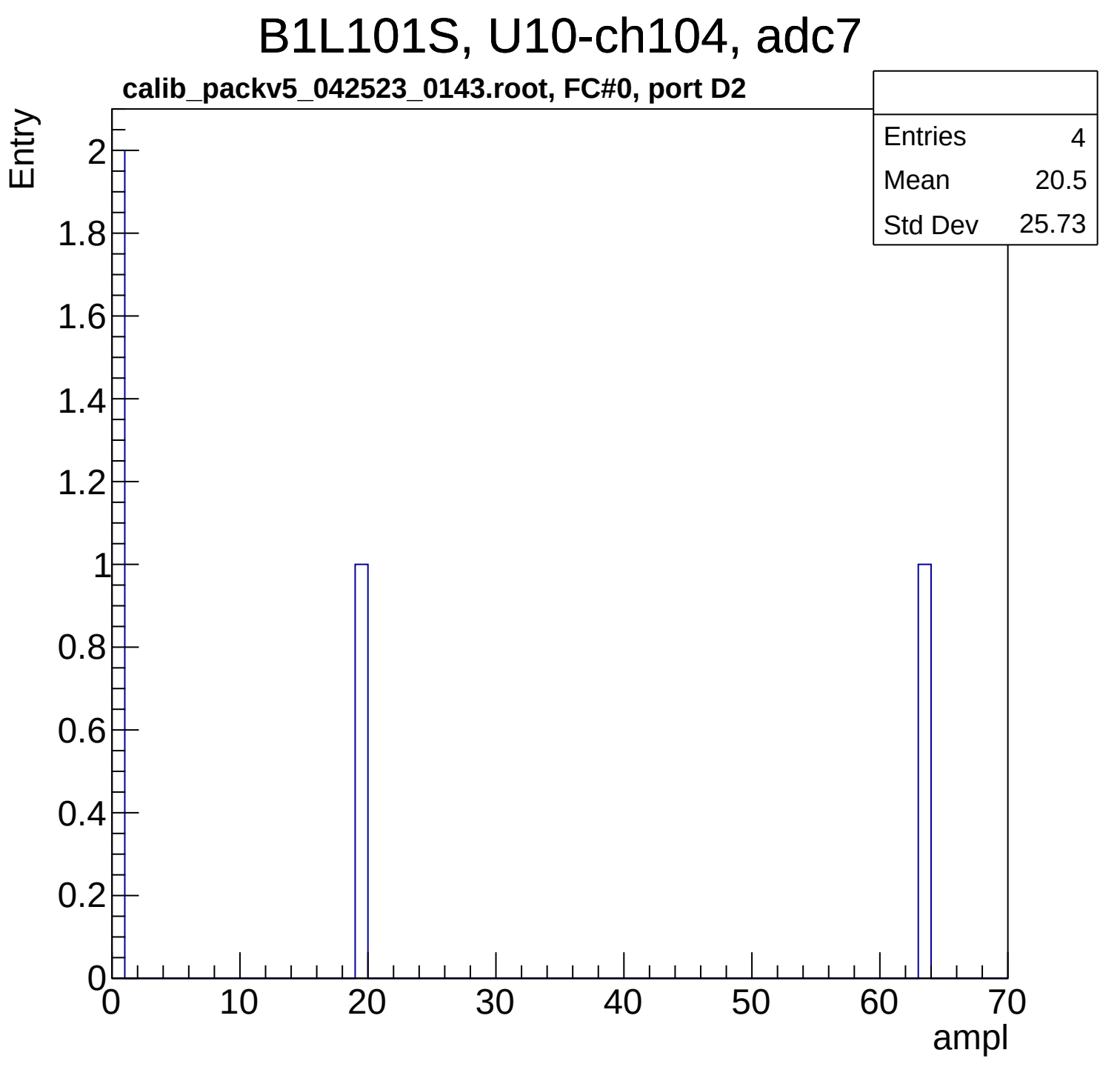
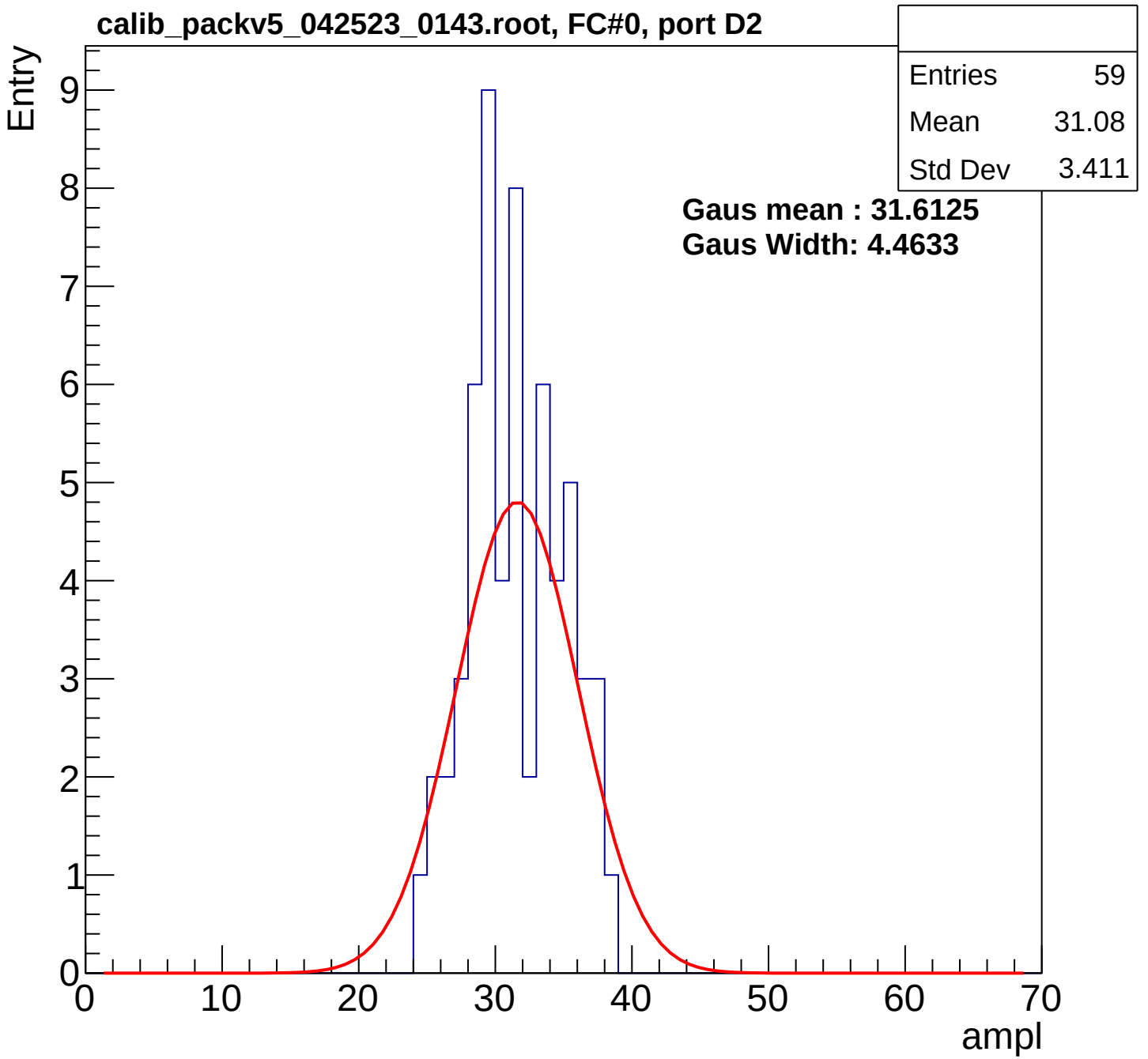

B1L101S, U10-ch104, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 48.45
Std Dev 3.705
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

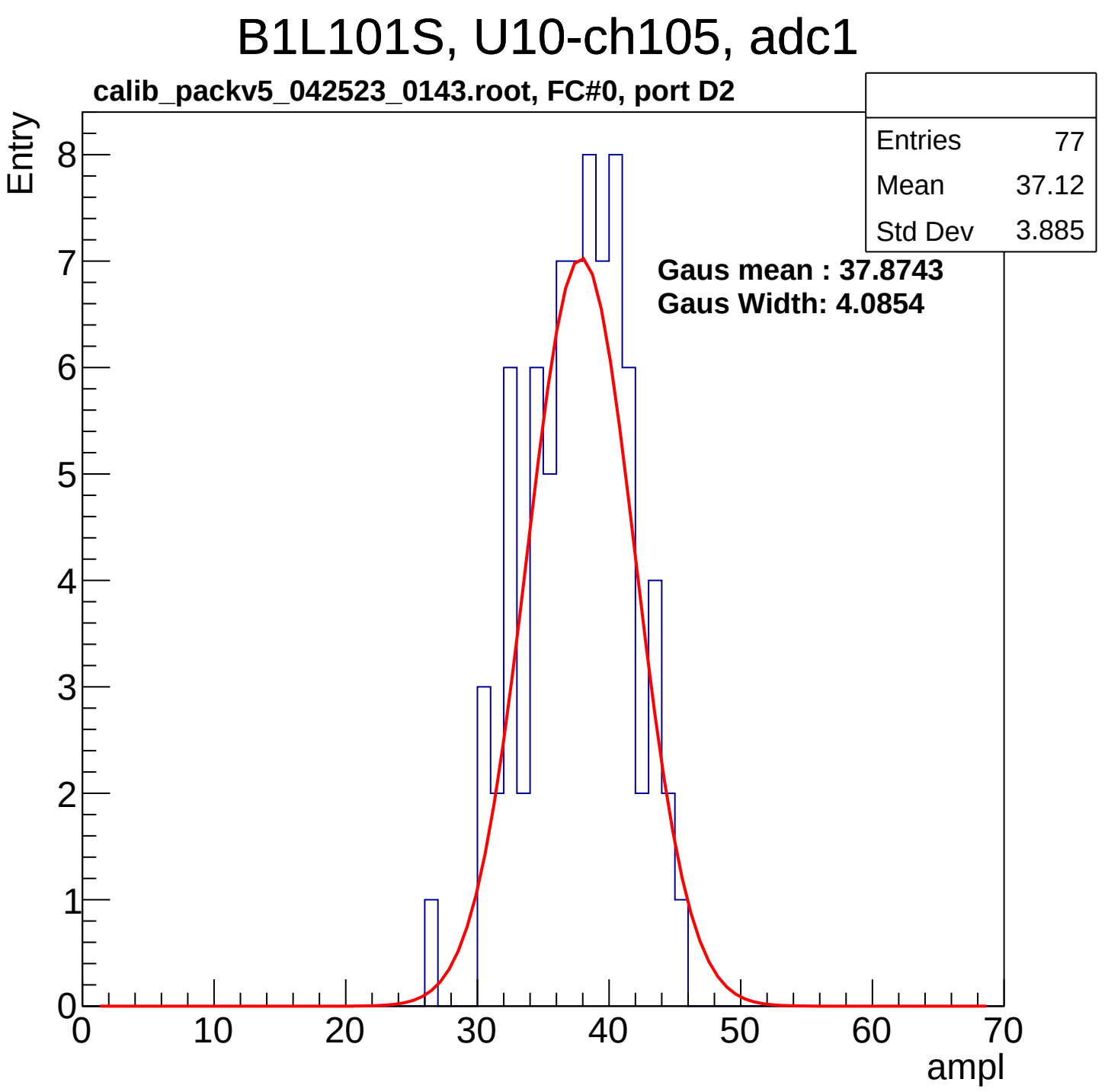

B1L101S, U10-ch104, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 55.47
Std Dev 3.515
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

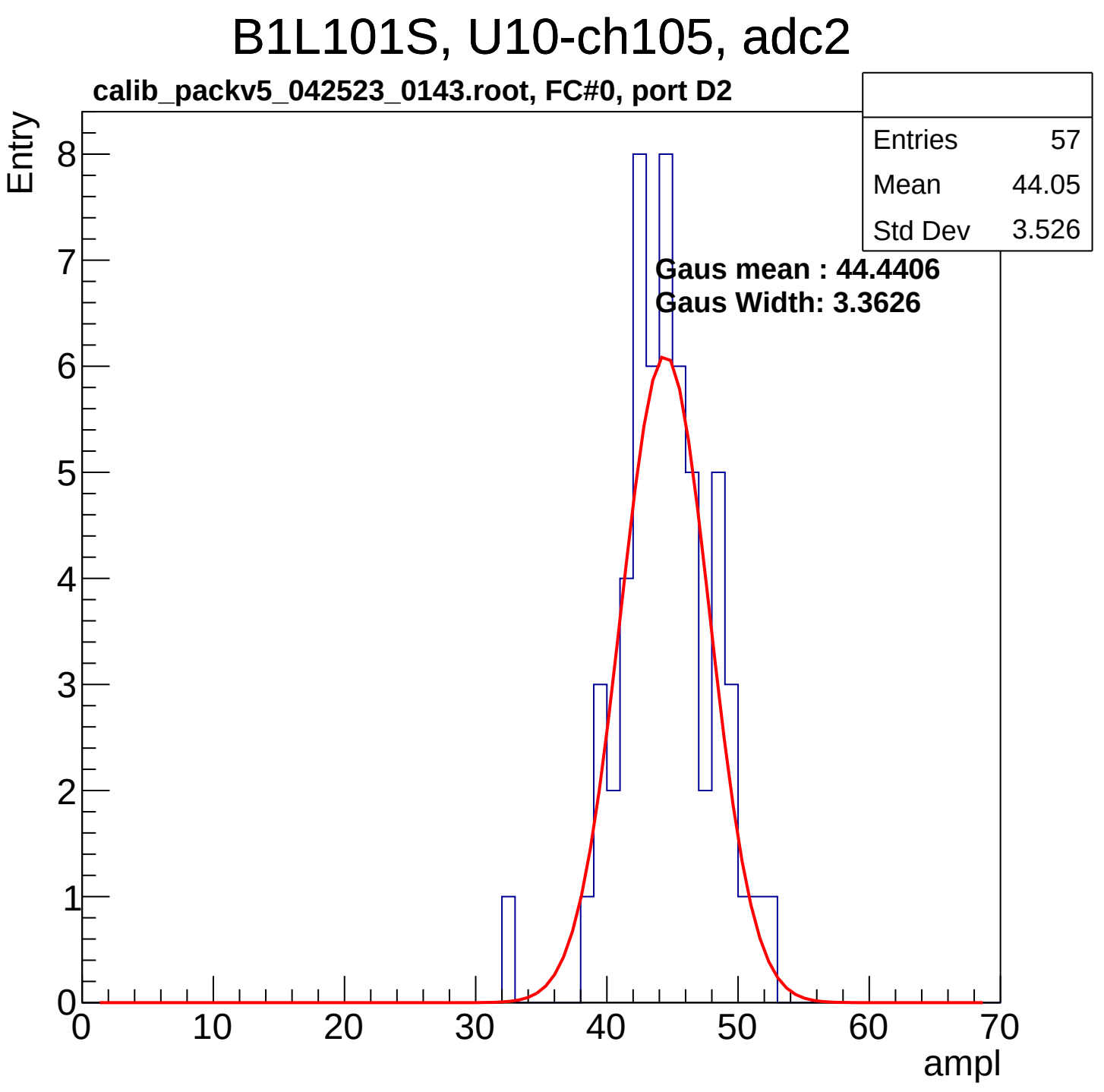

B1L101S, U10-ch104, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 26
Mean 59.81
Std Dev 2.512
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

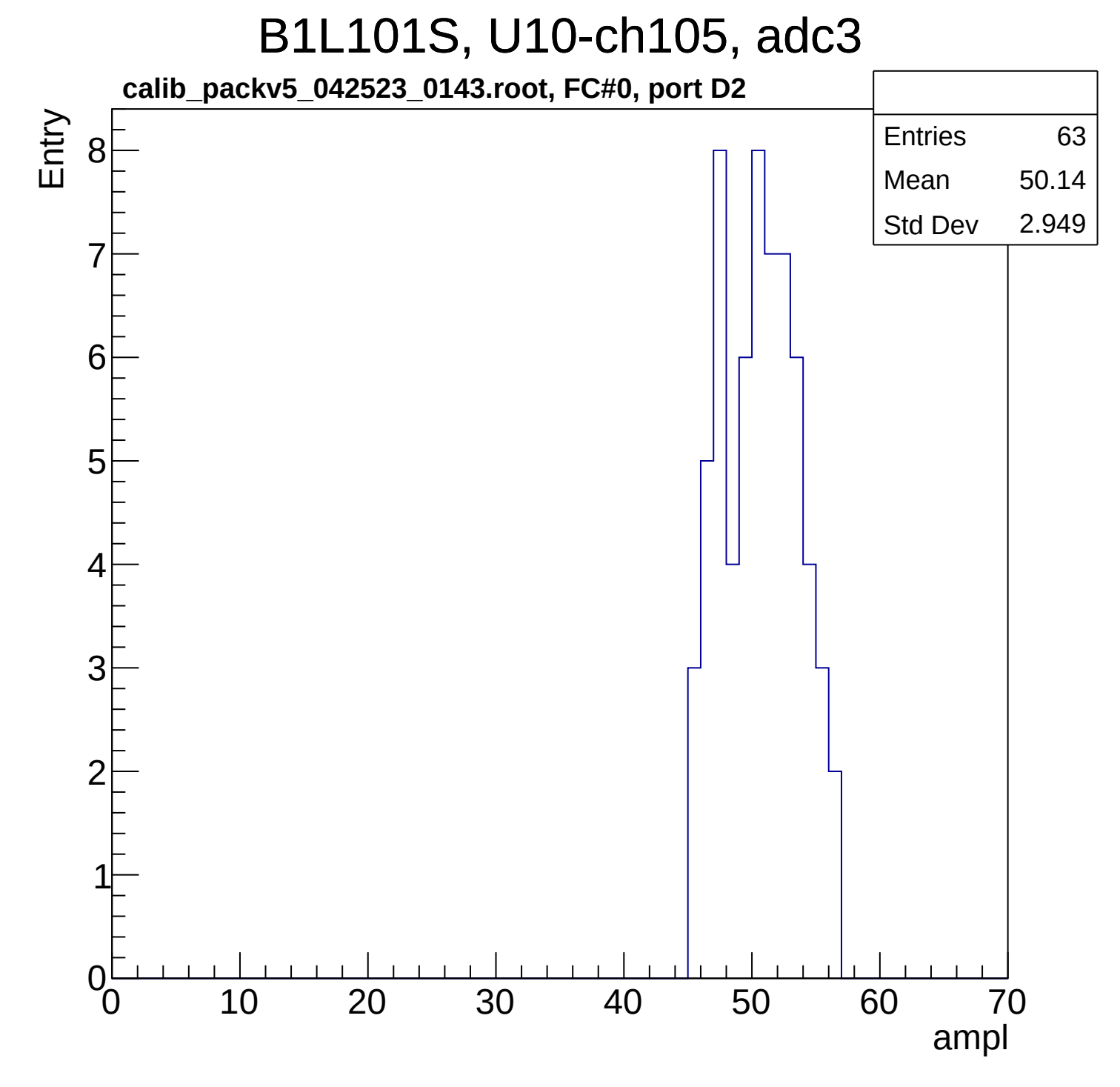

B1L101S, U10-ch104, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 16
Mean 57.5
Std Dev 14.93
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

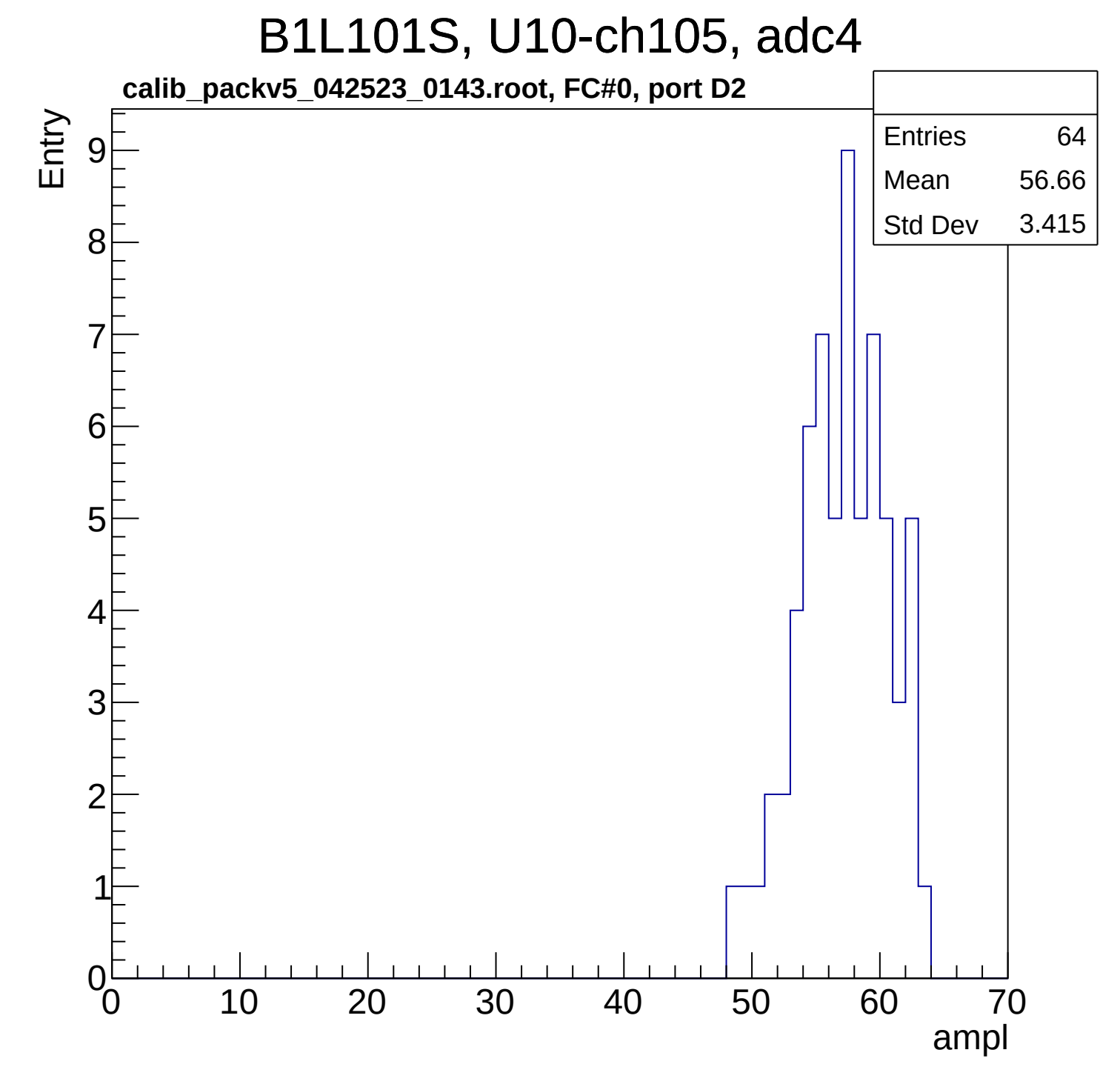

B1L101S, U10-ch104, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 20.5
Std Dev 25.73
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

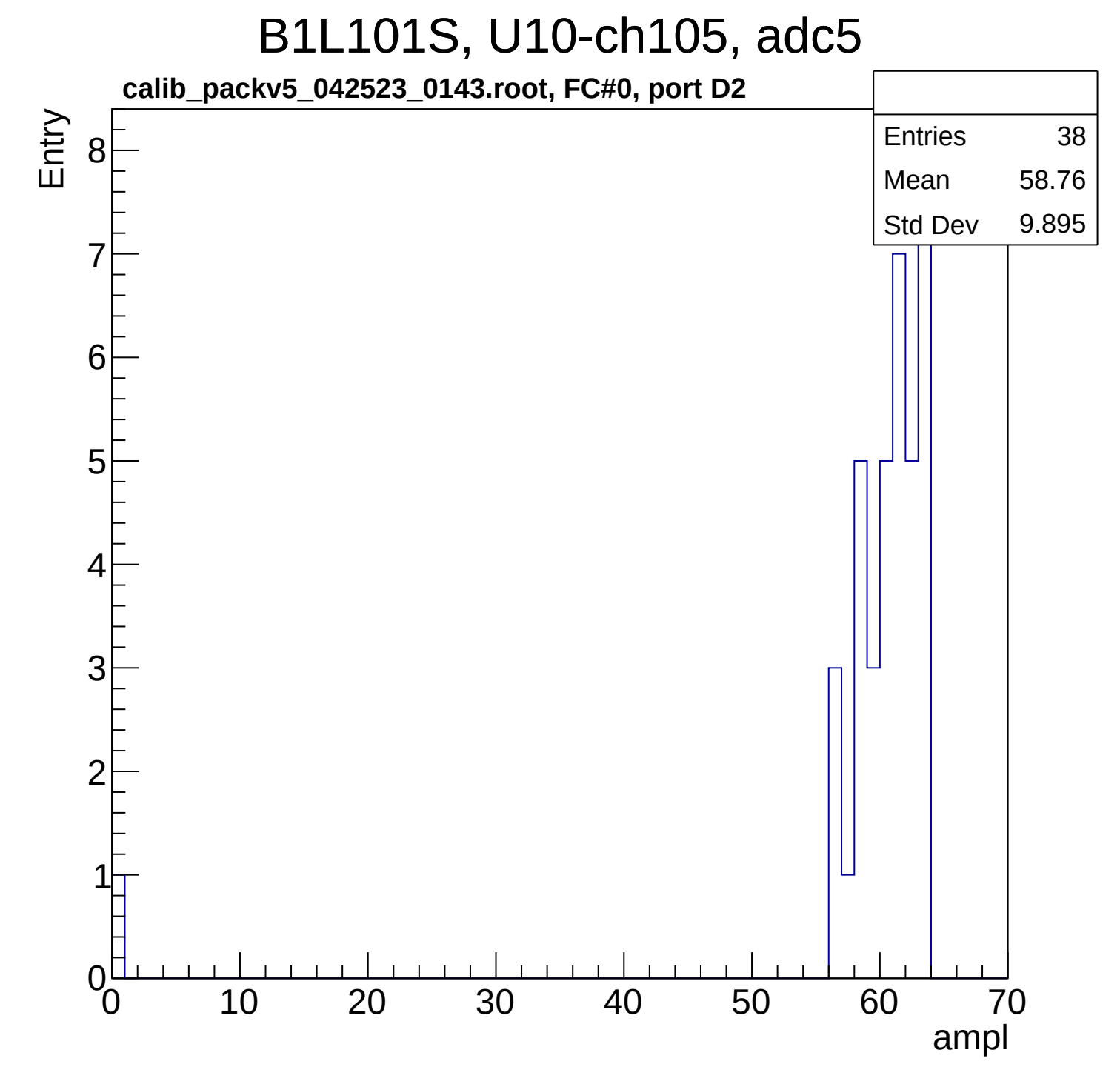

B1L101S, U10-ch105, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 31.08
Std Dev 3.411
Gaus mean : 31.6125
Gaus Width: 4.4633
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

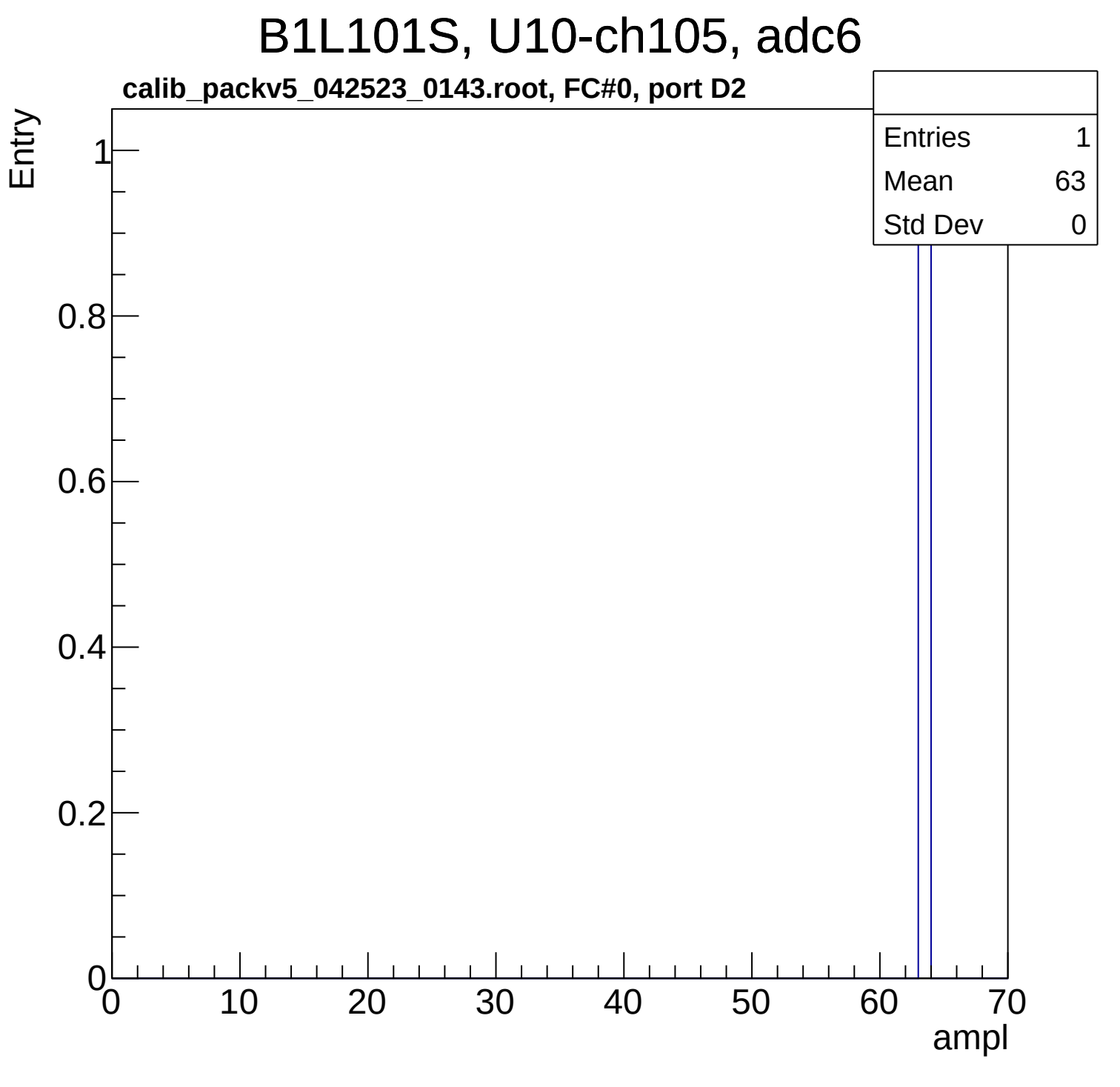

B1L101S, U10-ch105, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 37.12
Std Dev 3.885
Gaus mean : 37.8743
Gaus Width: 4.0854
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

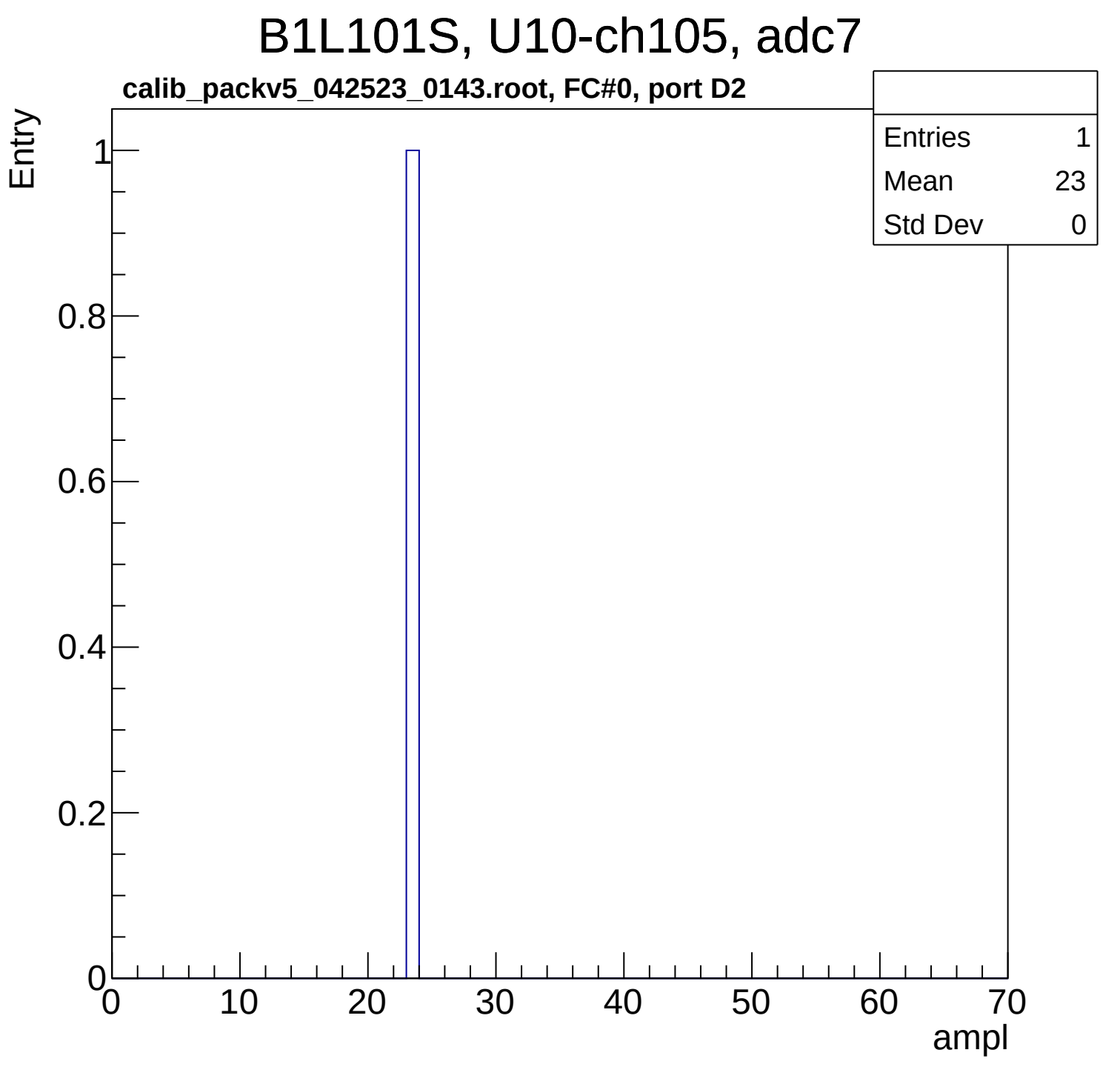

B1L101S, U10-ch105, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 44.05
Std Dev 3.526
Gaus mean : 44.4406
Gaus Width: 3.3626
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

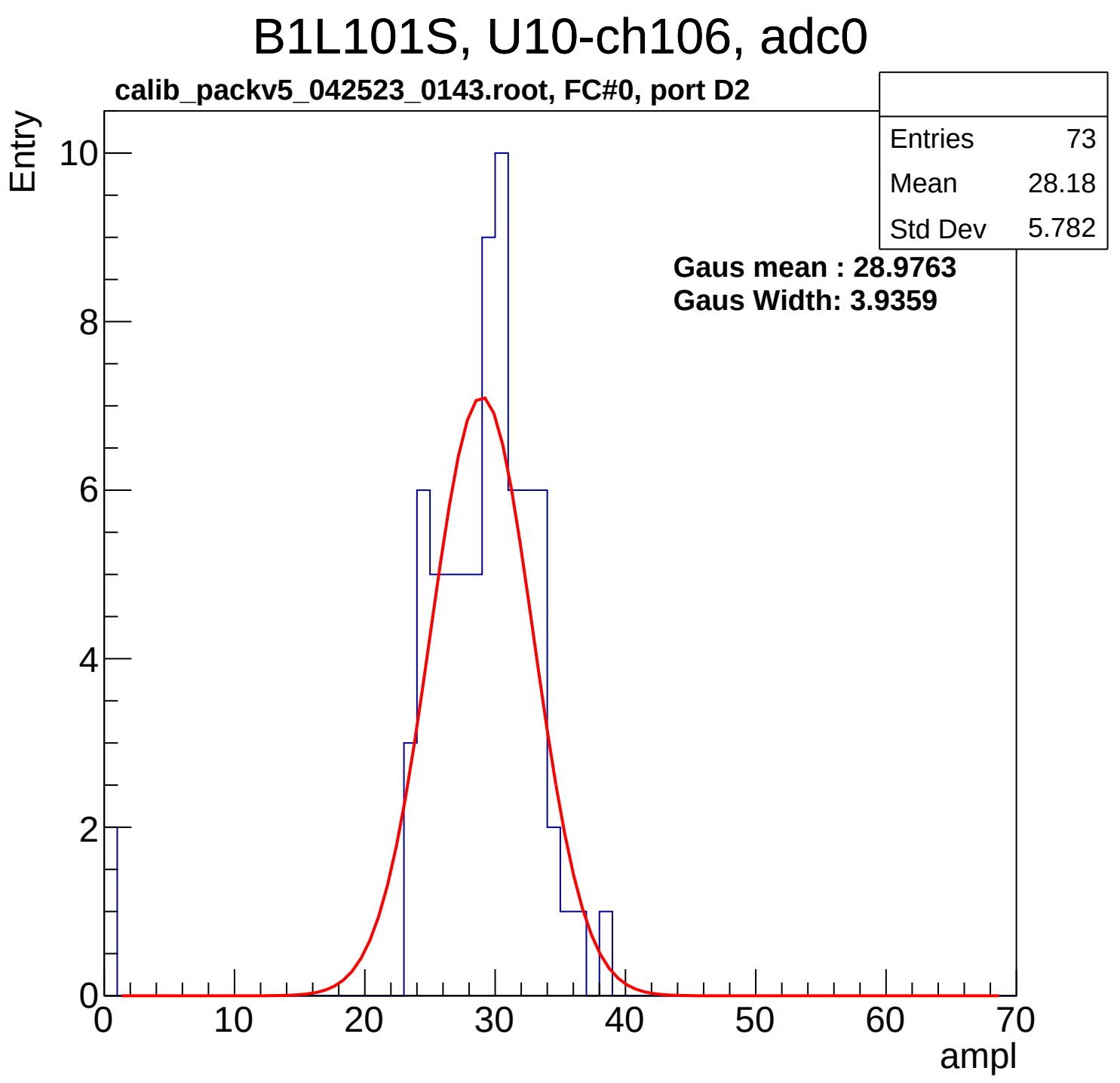

B1L101S, U10-ch105, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 50.14
Std Dev 2.949
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

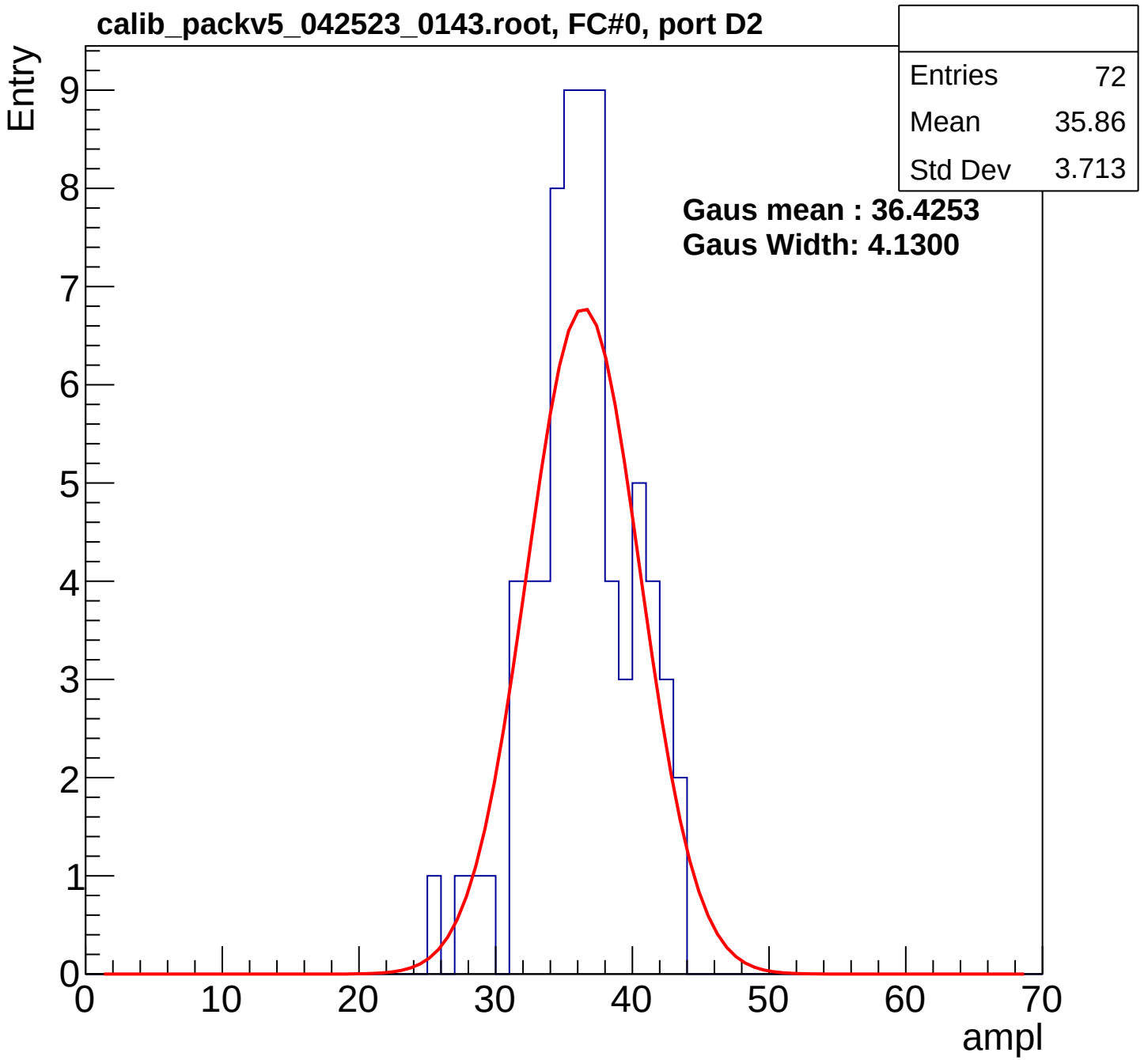

B1L101S, U10-ch105, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 56.66
Std Dev 3.415
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

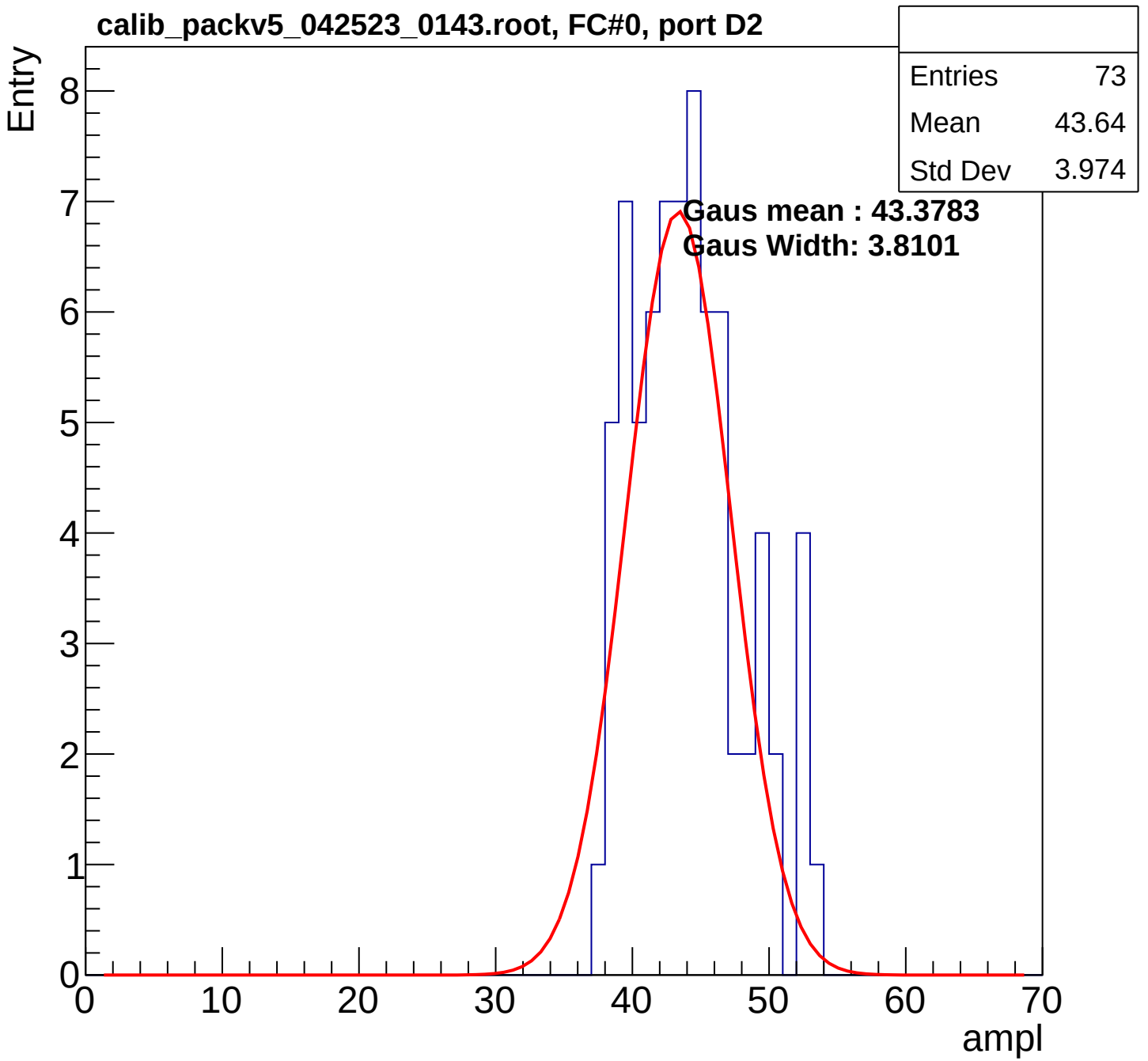

B1L101S, U10-ch105, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 38
Mean 58.76
Std Dev 9.895
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

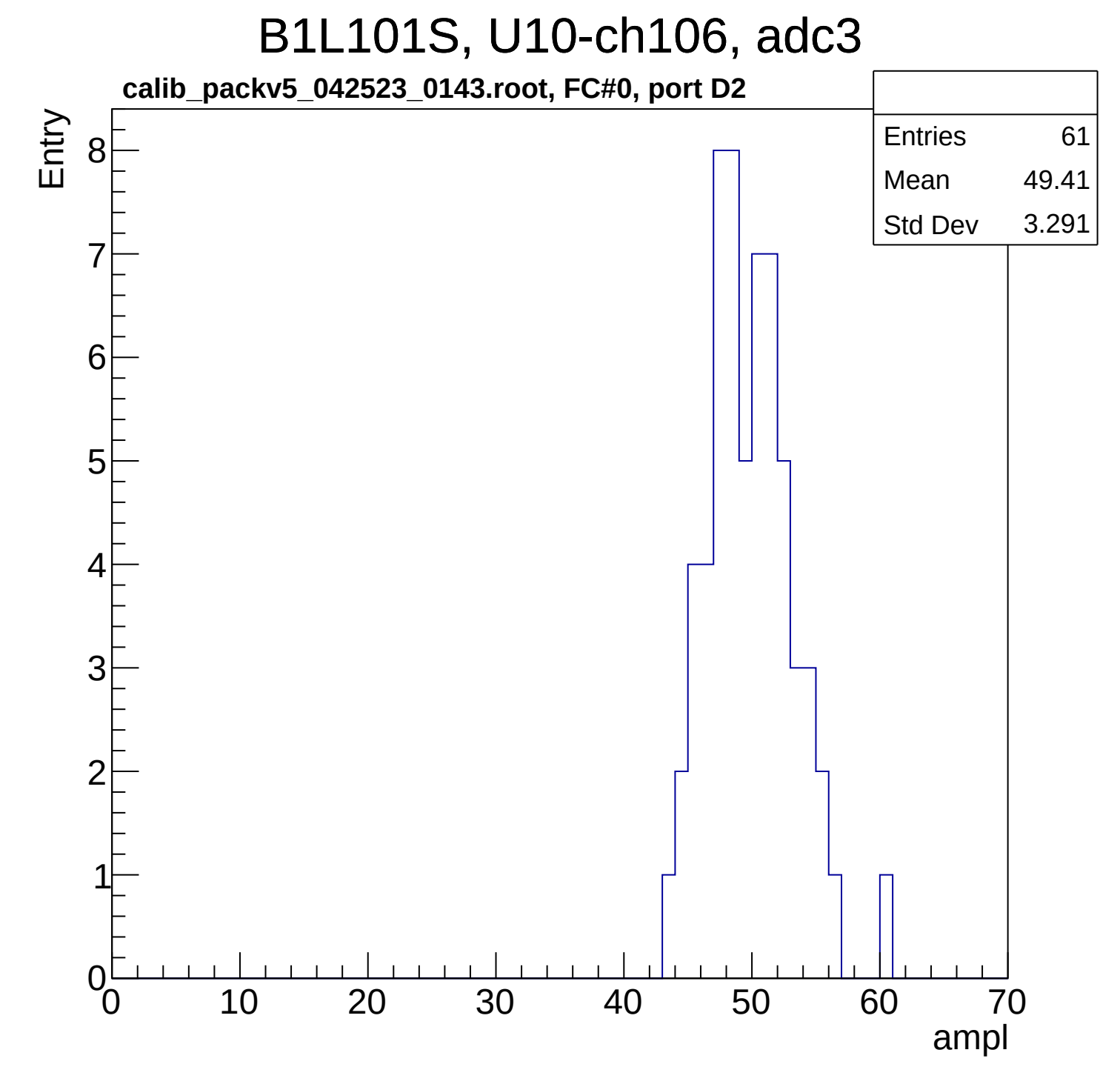

B1L101S, U10-ch105, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch105, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 23
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch106, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 28.18
Std Dev 5.782
Gaus mean : 28.9763
Gaus Width: 3.9359
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch106, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 35.86
Std Dev 3.713
Gaus mean : 36.4253
Gaus Width: 4.1300
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch106, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 43.64
Std Dev 3.974
Gaus mean : 43.3783
Gaus Width: 3.8101
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch106, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 49.41
Std Dev 3.291
Entry
ampl
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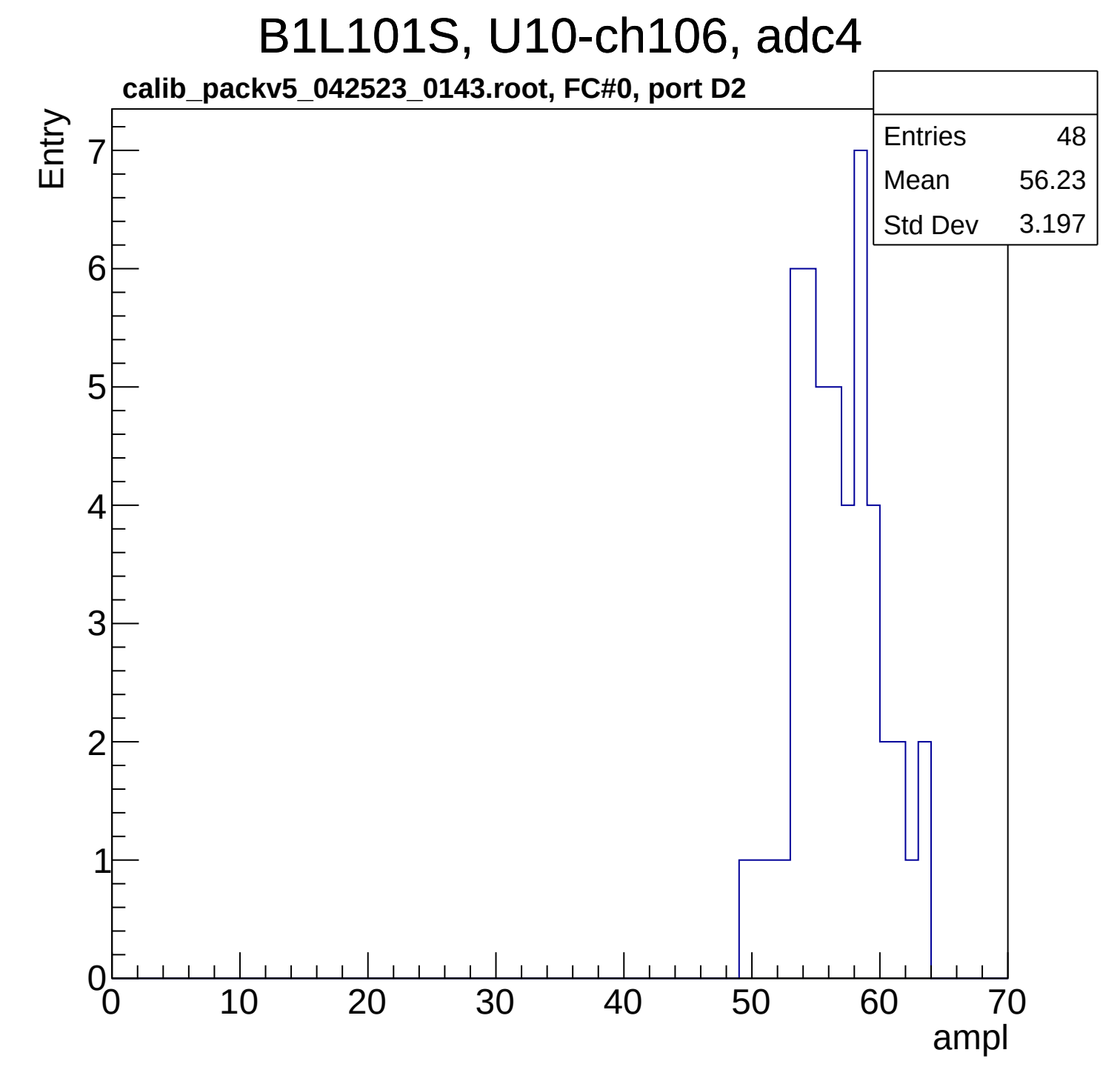
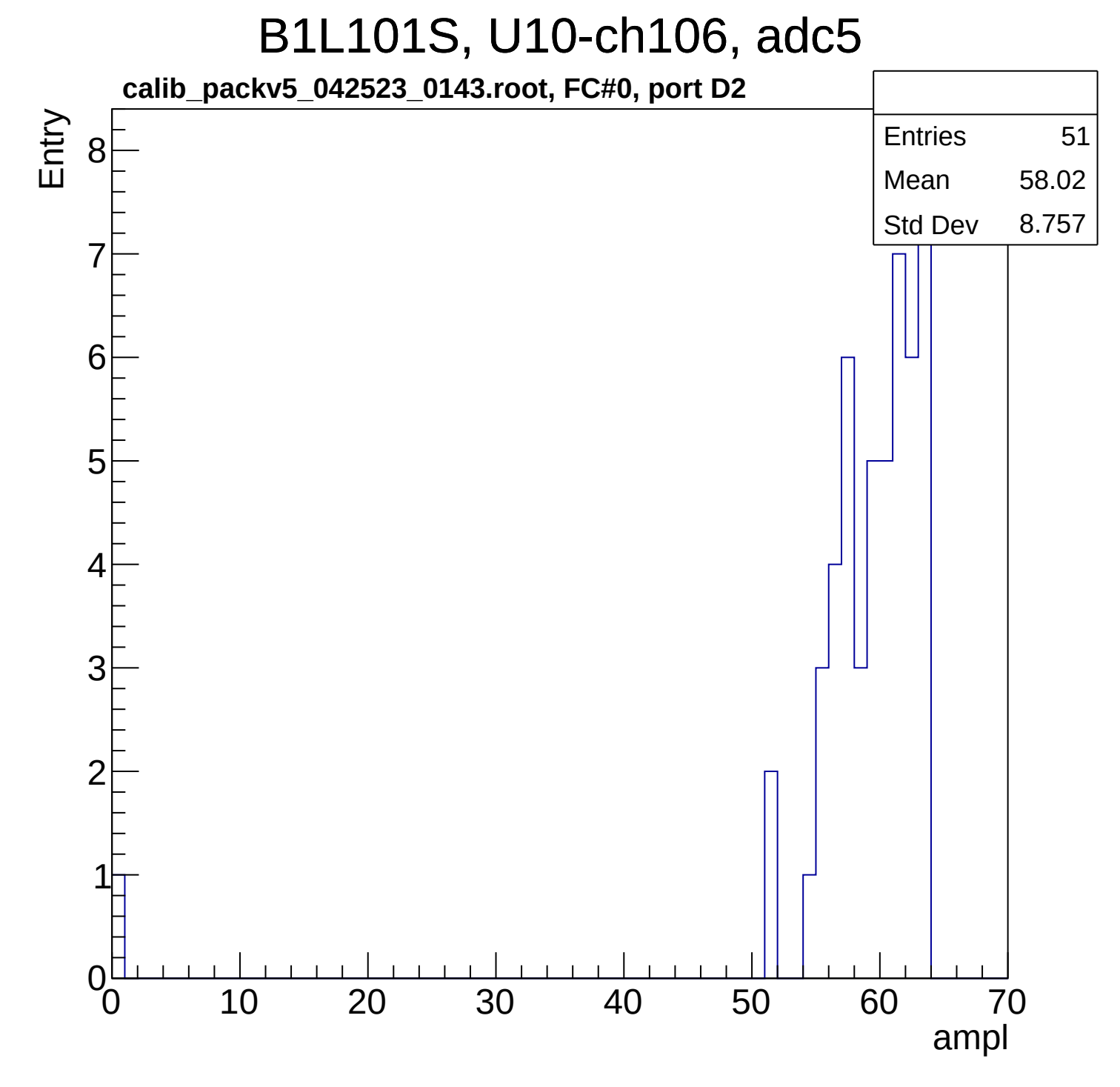
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch106, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 56.23
Std Dev 3.197
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U10-ch106, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 58.02
Std Dev 8.757
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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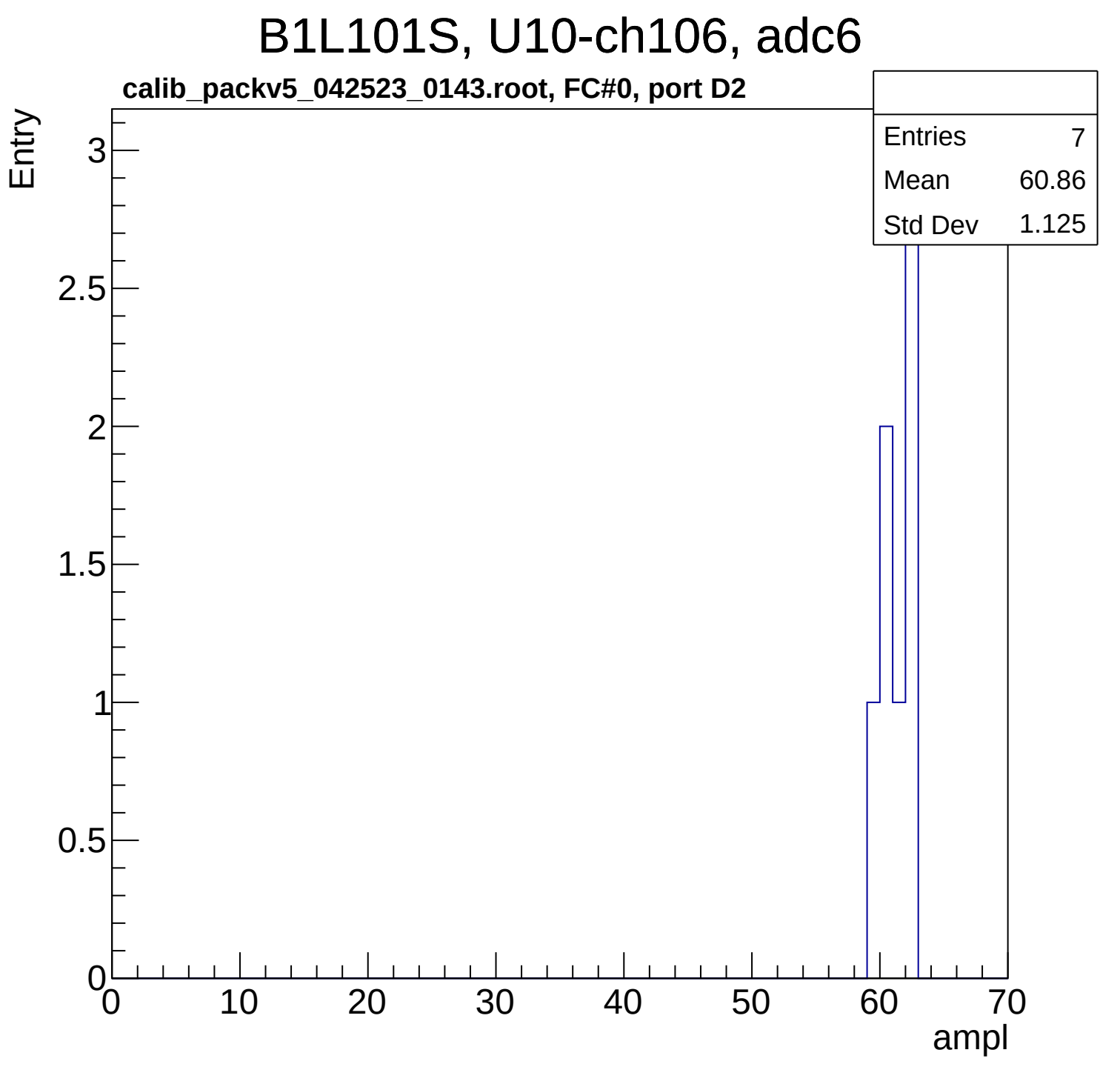
60
70


B1L101S, U10-ch106, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 60.86
Std Dev 1.125
Entry
ampl
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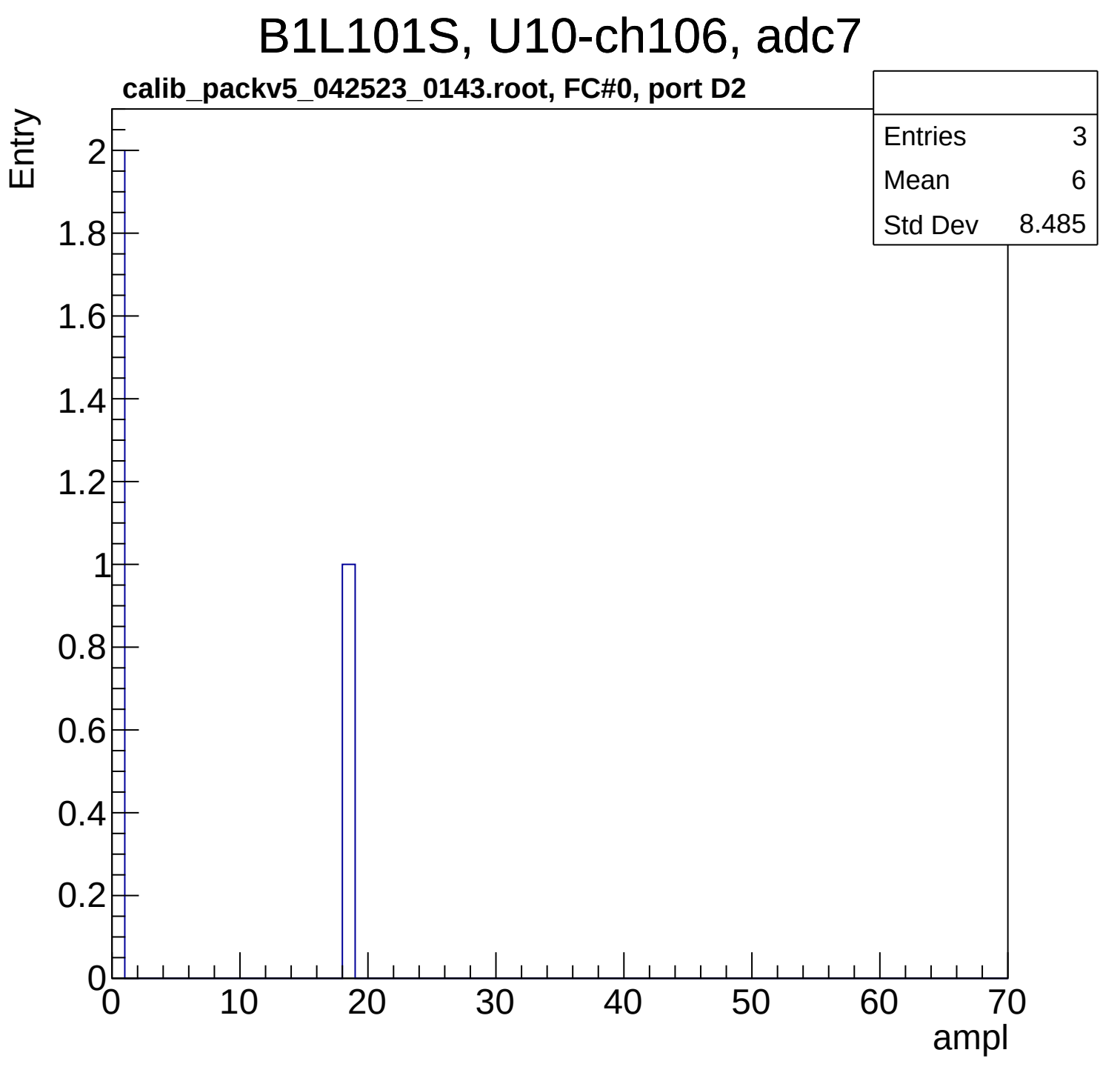
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U10-ch106, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 6
Std Dev 8.485
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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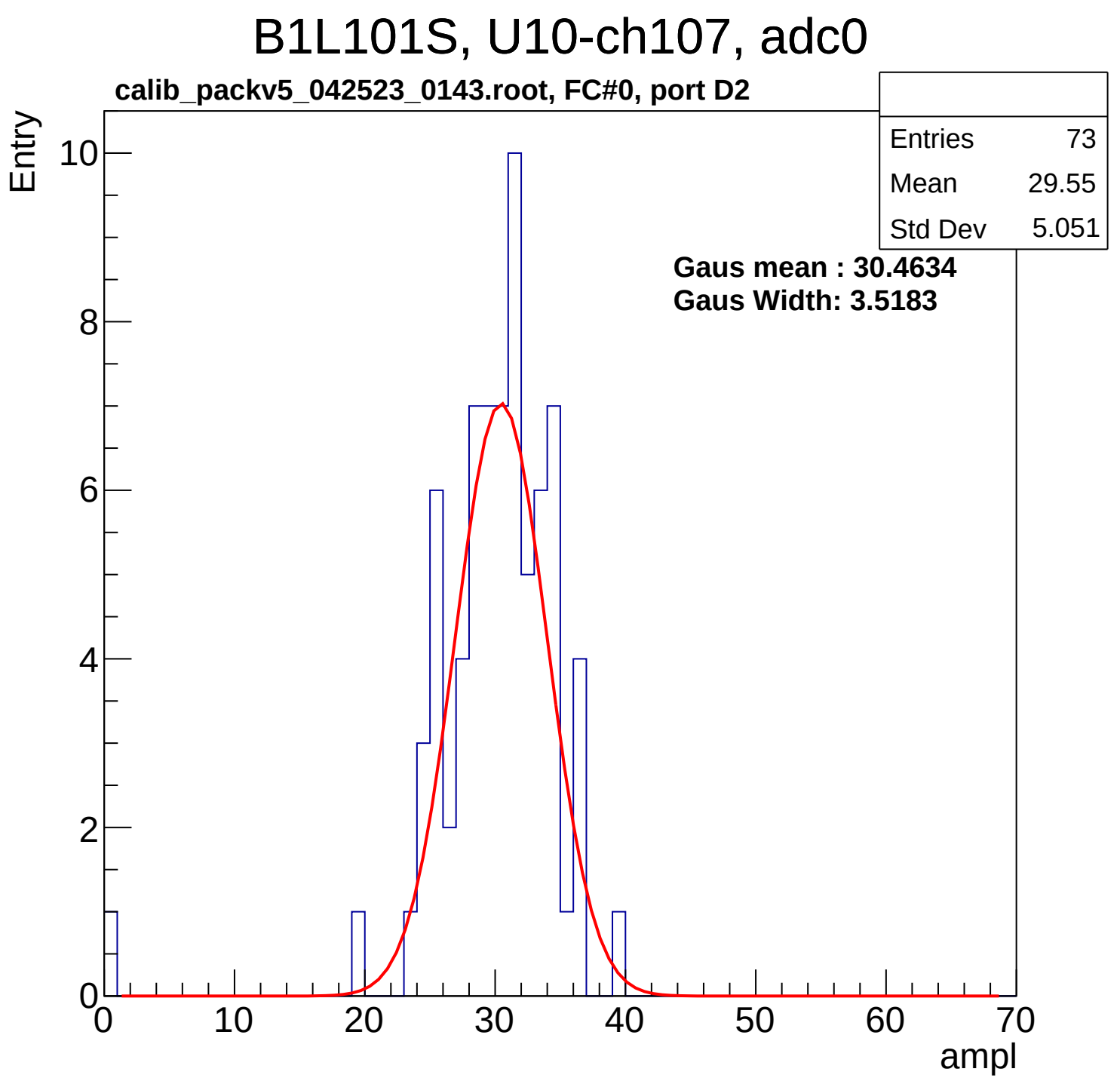
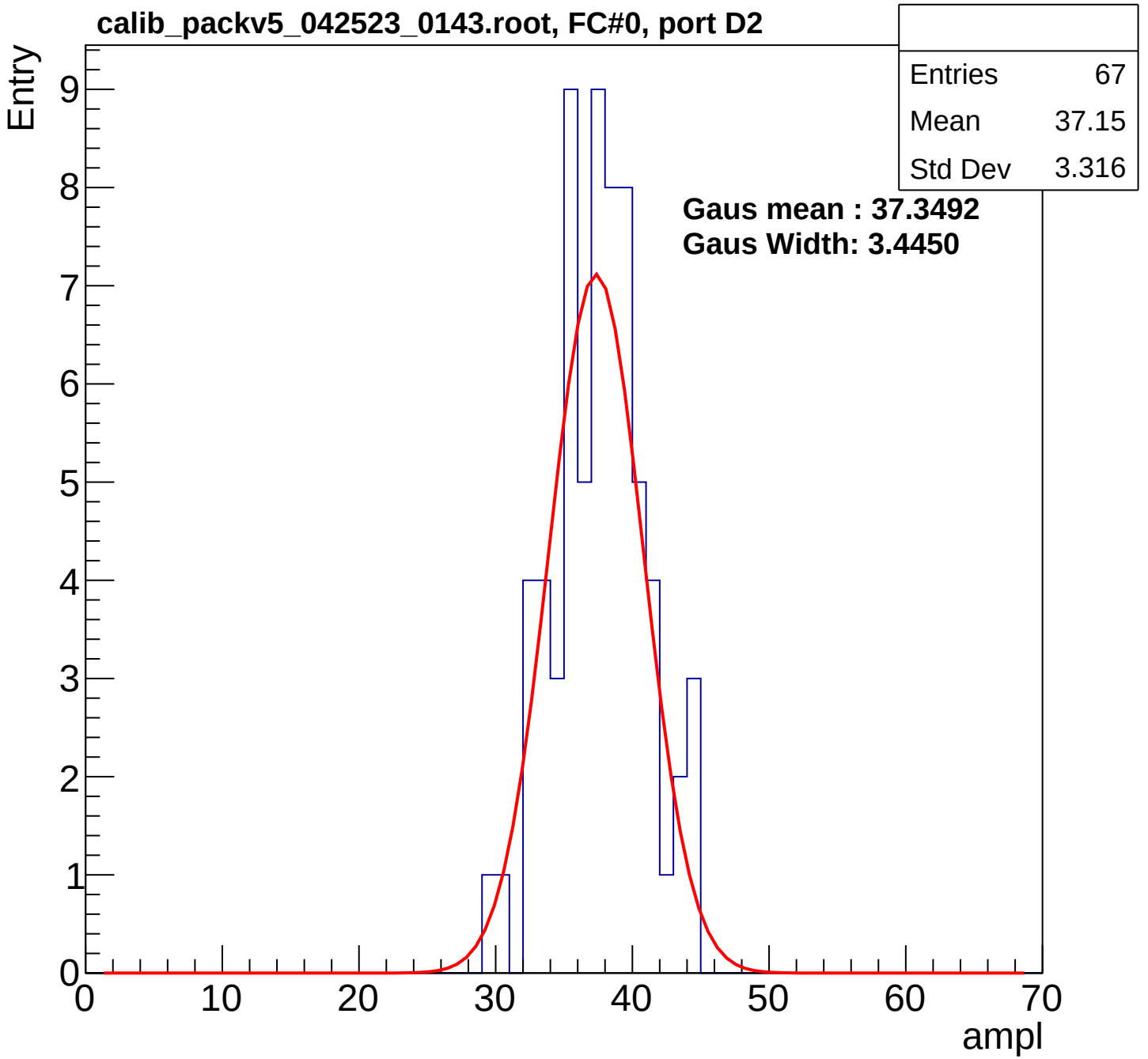
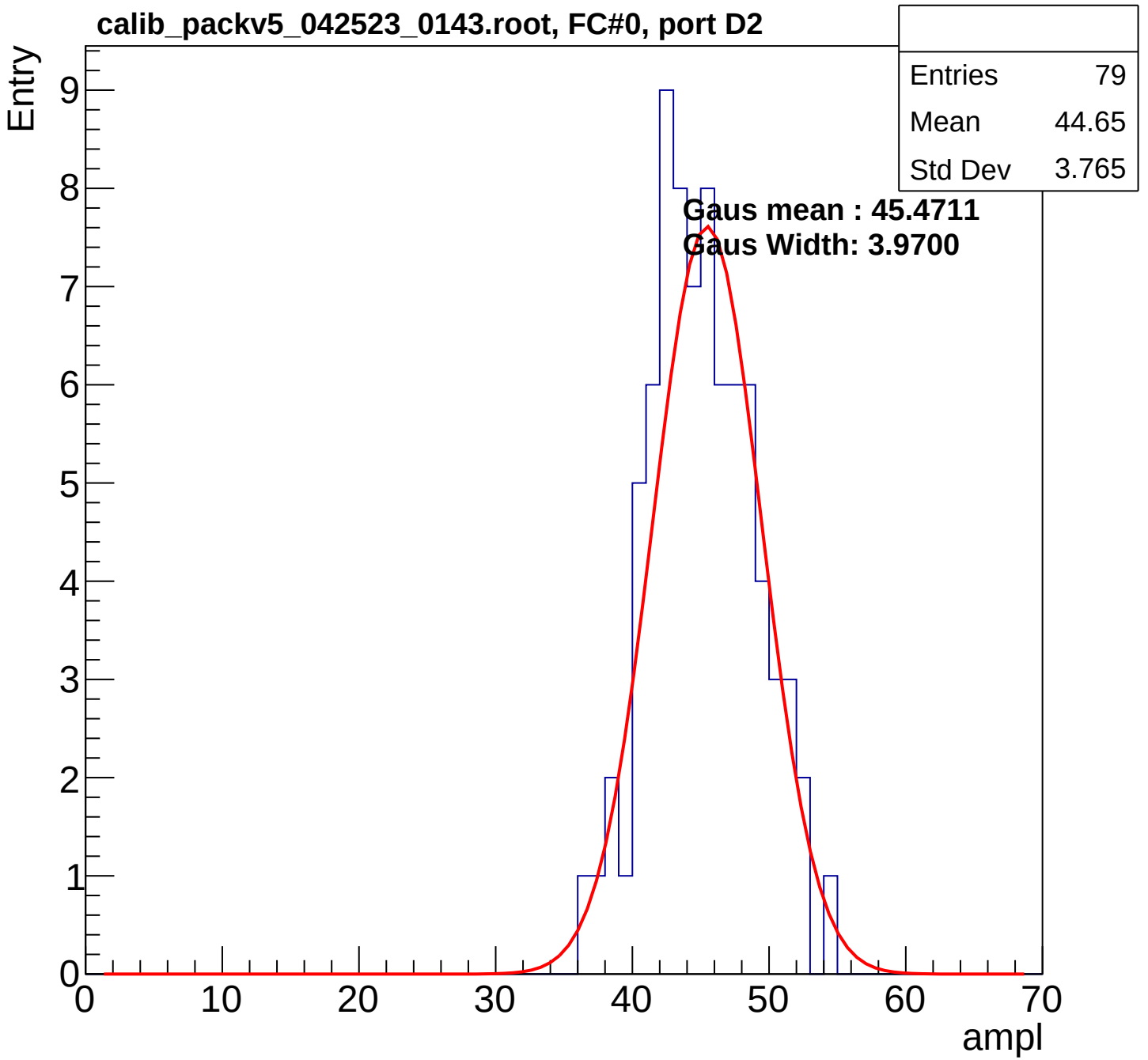
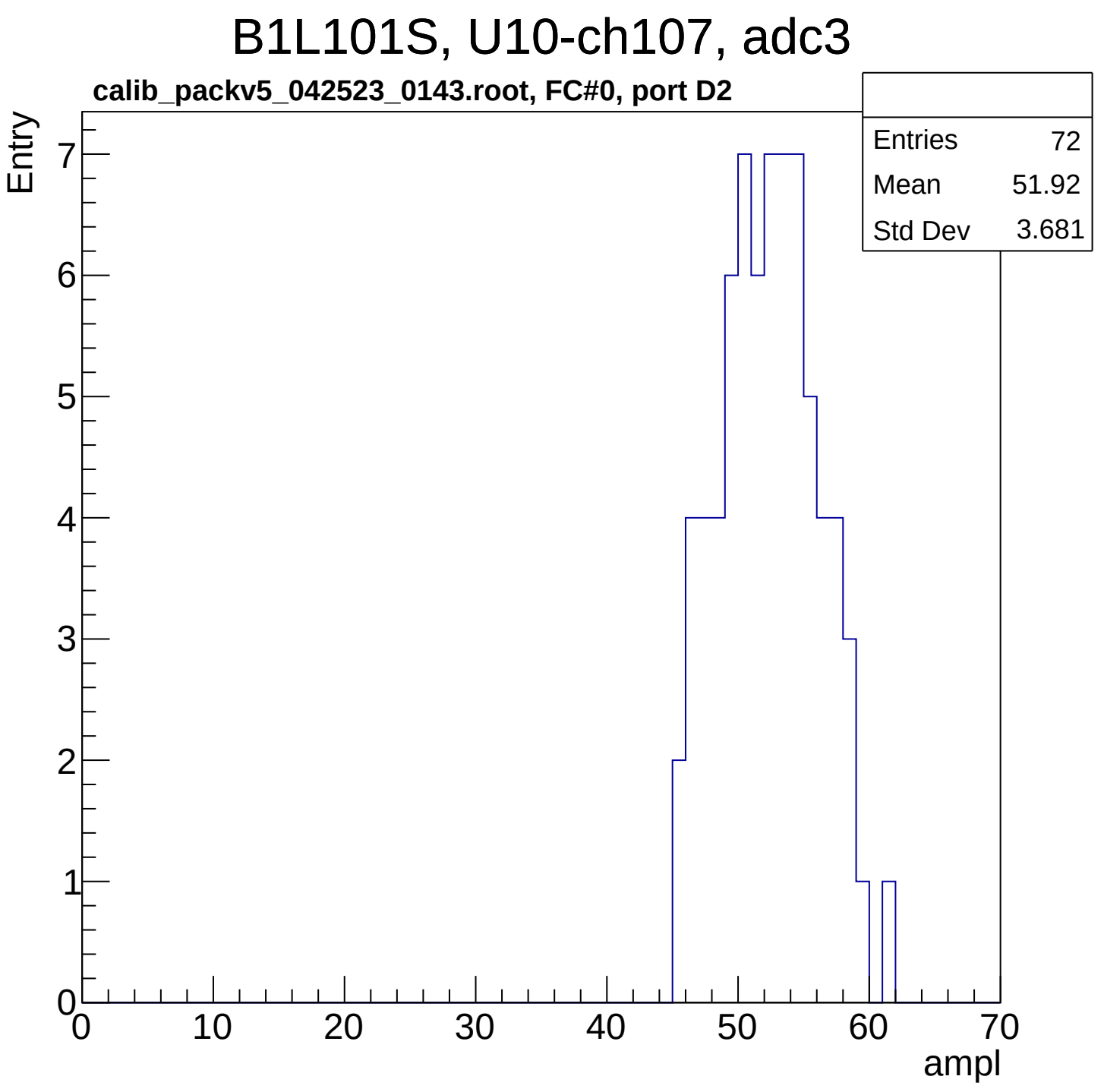
20
30
40
50
60
70


B1L101S, U10-ch107, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 29.55
Std Dev 5.051
Gaus mean : 30.4634
Gaus Width: 3.5183
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch107, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 37.15
Std Dev 3.316
Gaus mean : 37.3492
Gaus Width: 3.4450
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch107, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 44.65
Std Dev 3.765
Gaus mean : 45.4711
Gaus Width: 3.9700
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch107, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 51.92
Std Dev 3.681
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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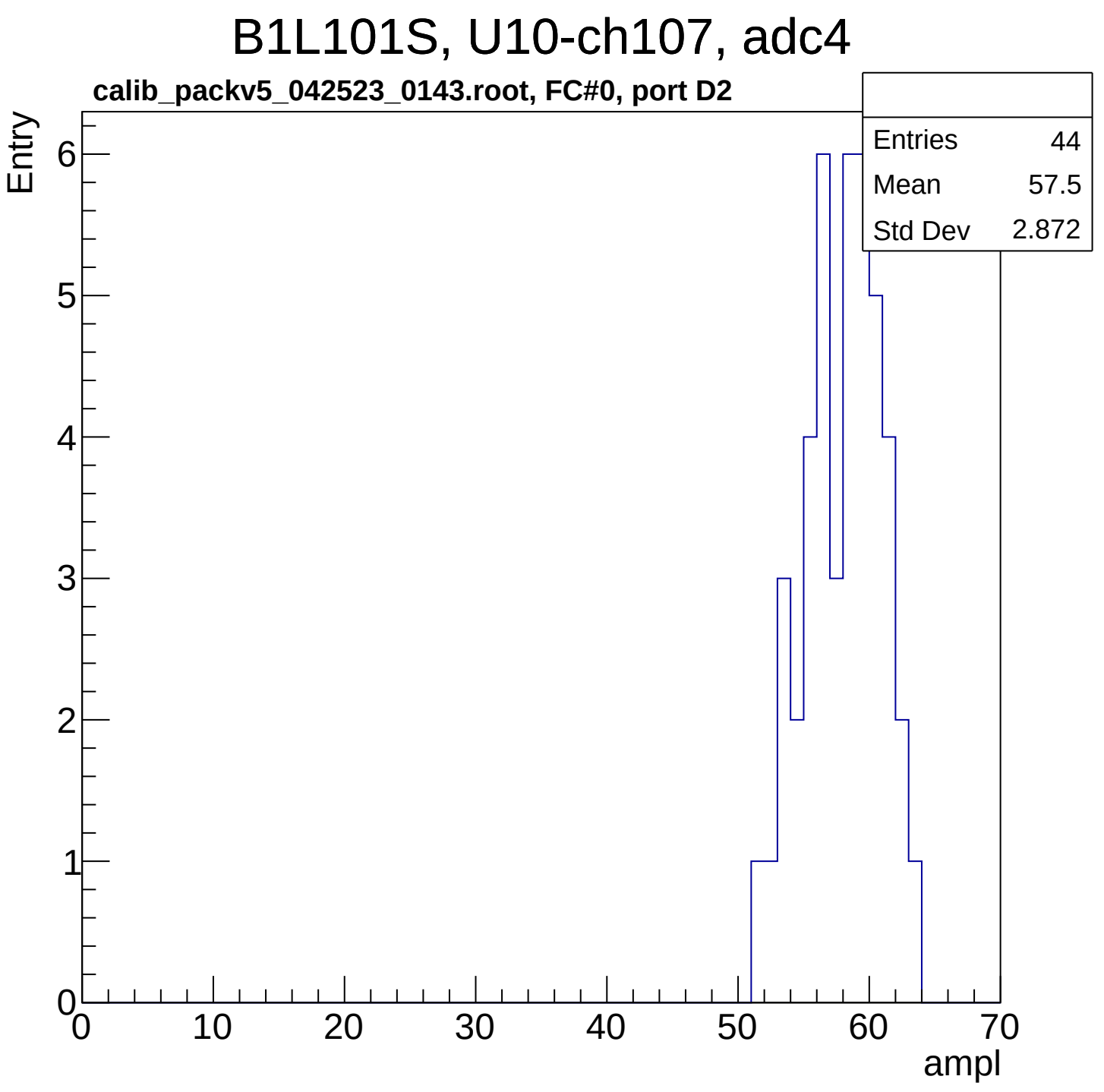
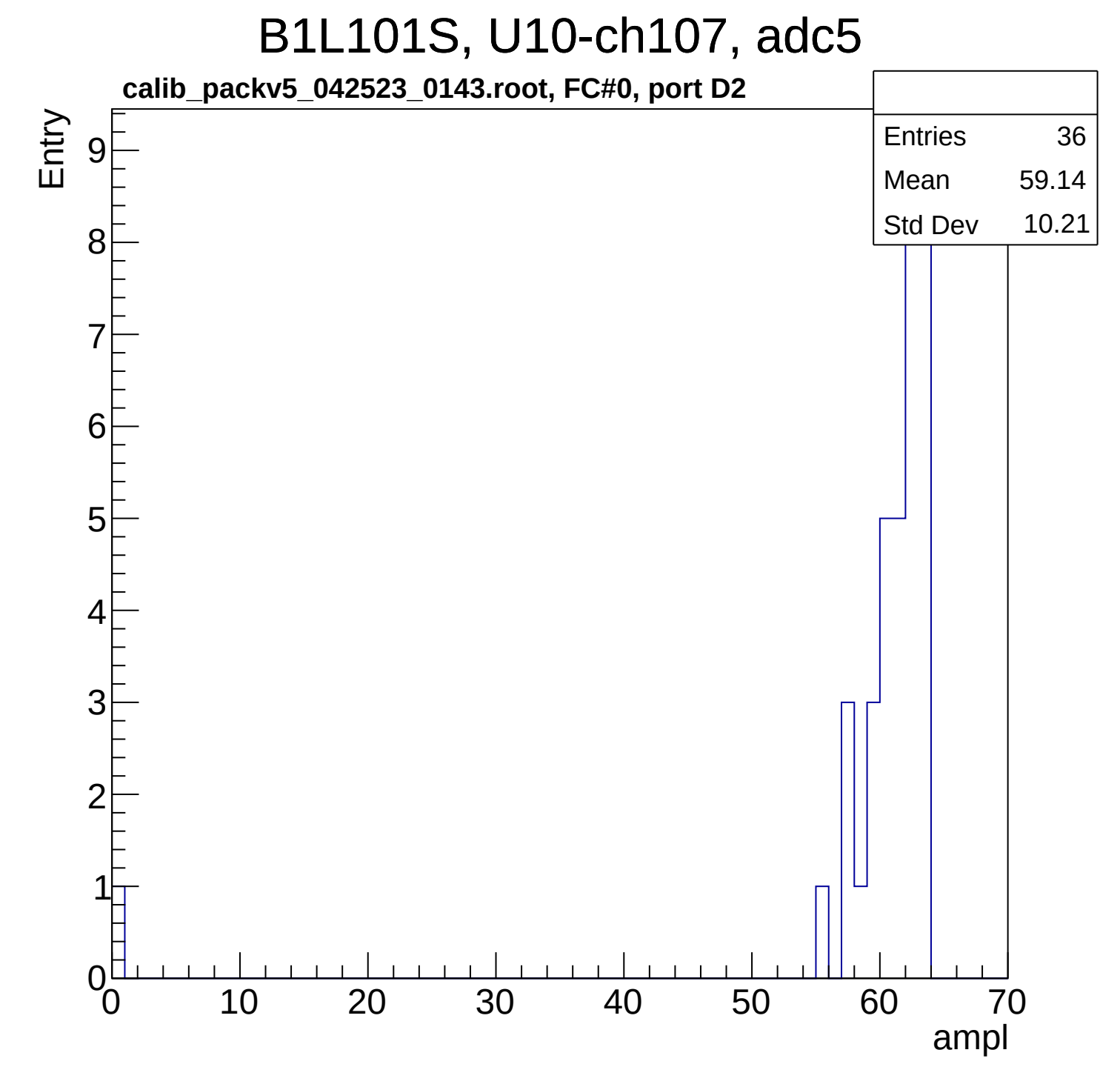

B1L101S, U10-ch107, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 44
Mean 57.5
Std Dev 2.872
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch107, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 36
Mean 59.14
Std Dev 10.21
Entry
ampl
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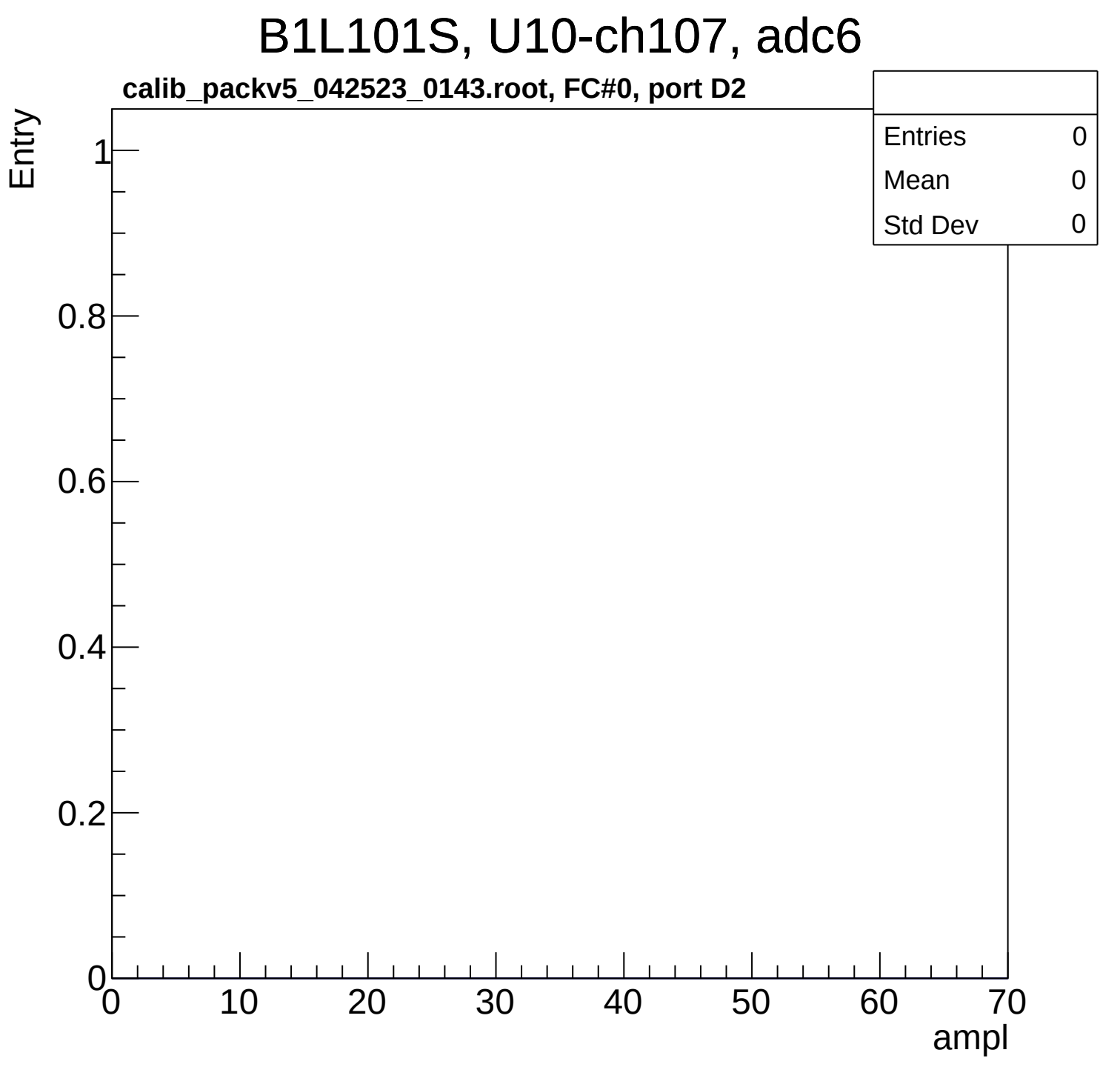
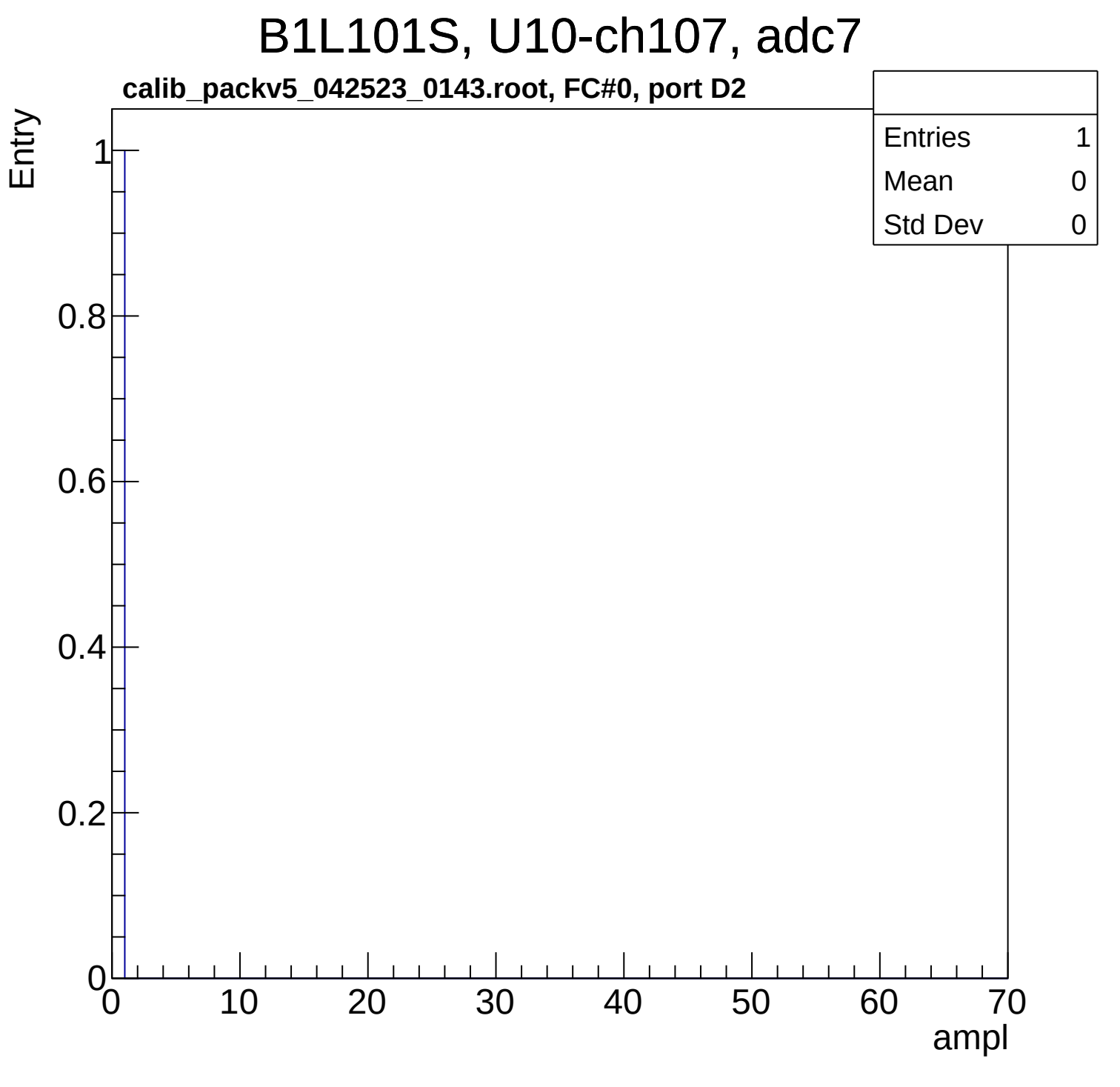
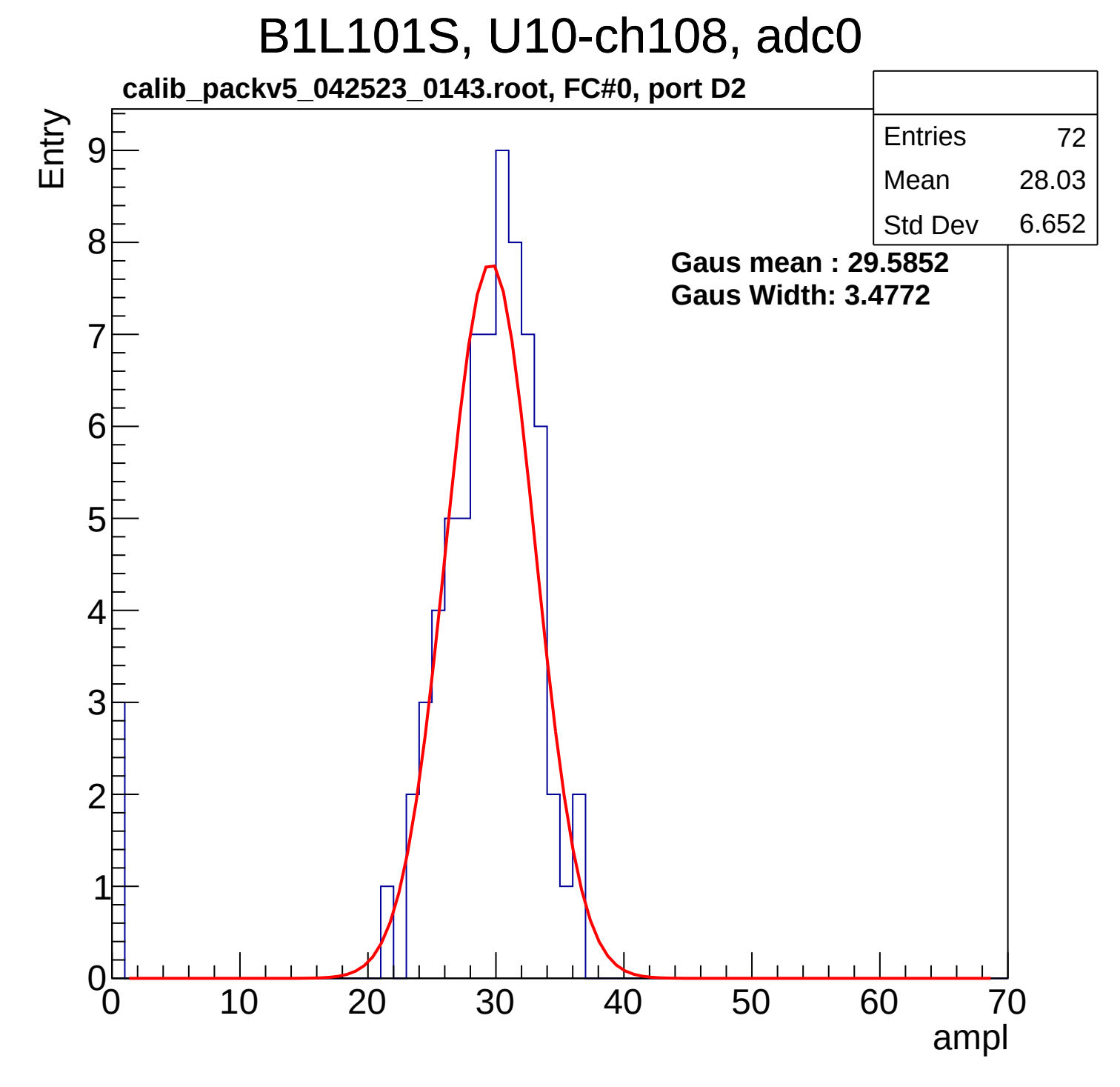
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch107, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch107, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch108, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 28.03
Std Dev 6.652
Gaus mean : 29.5852
Gaus Width: 3.4772
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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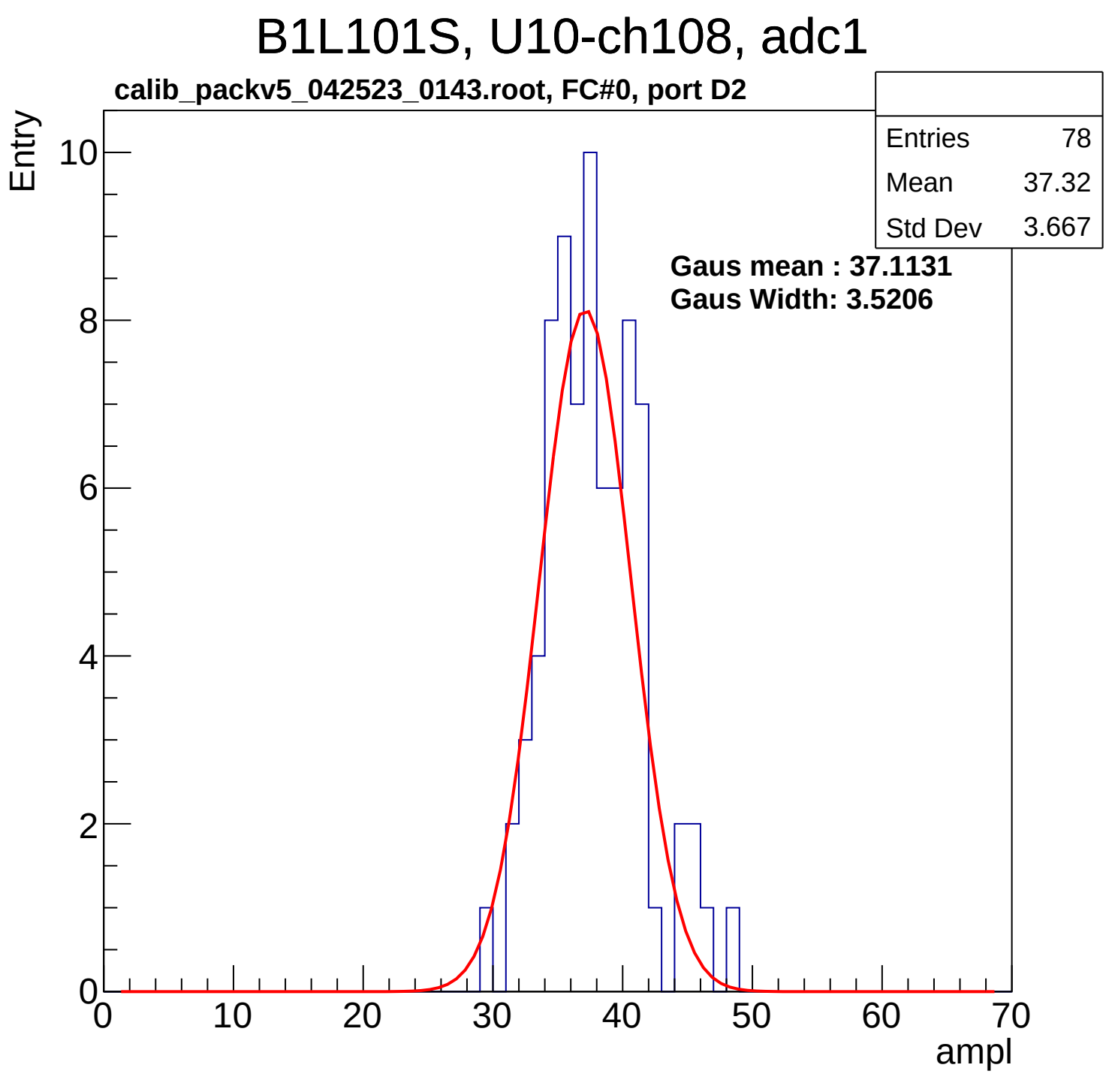
B1L101S, U10-ch108, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 37.32
Std Dev 3.667
Gaus mean : 37.1131
Gaus Width: 3.5206
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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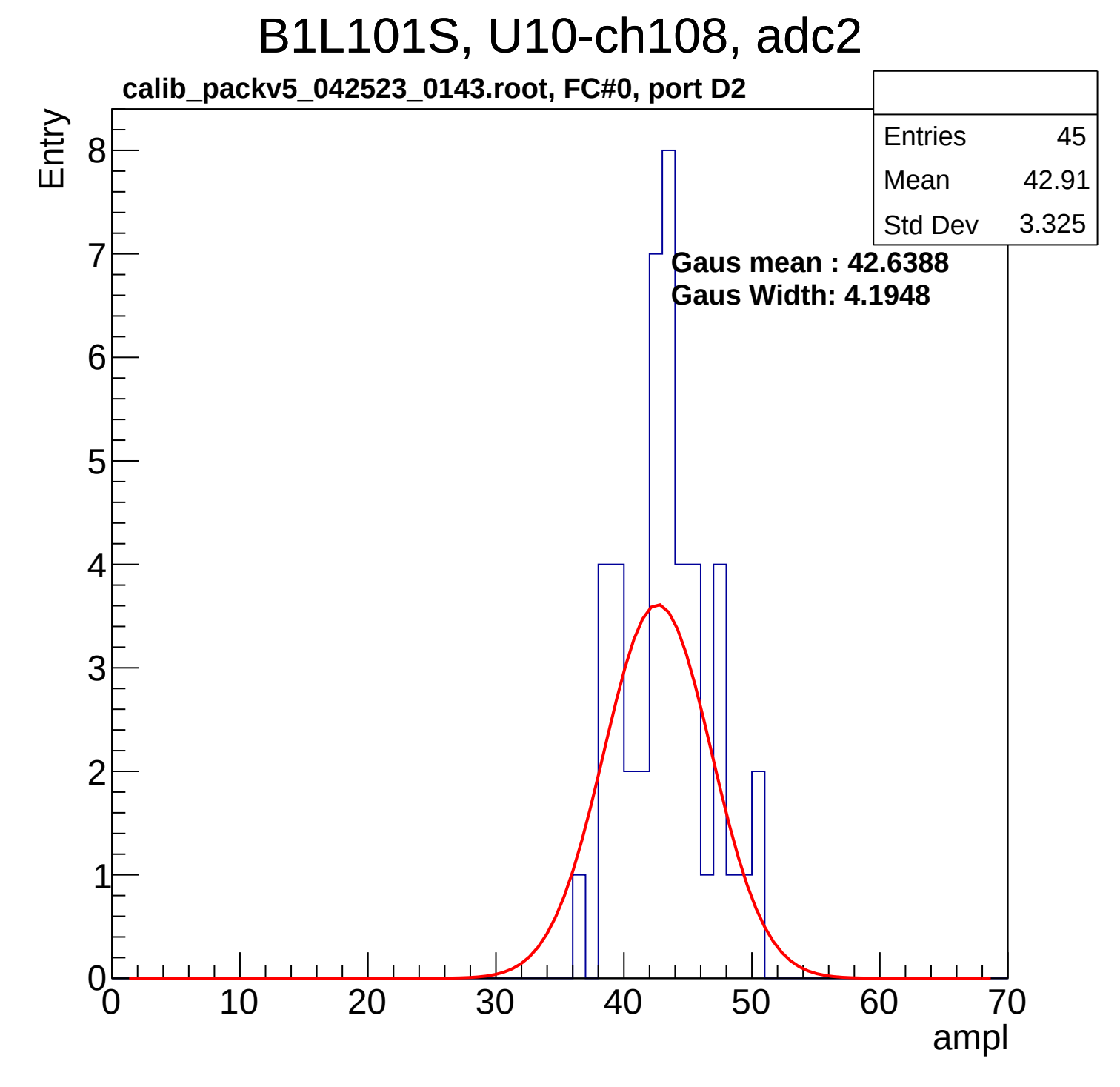
B1L101S, U10-ch108, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 42.91
Std Dev 3.325
Gaus mean : 42.6388
Gaus Width: 4.1948
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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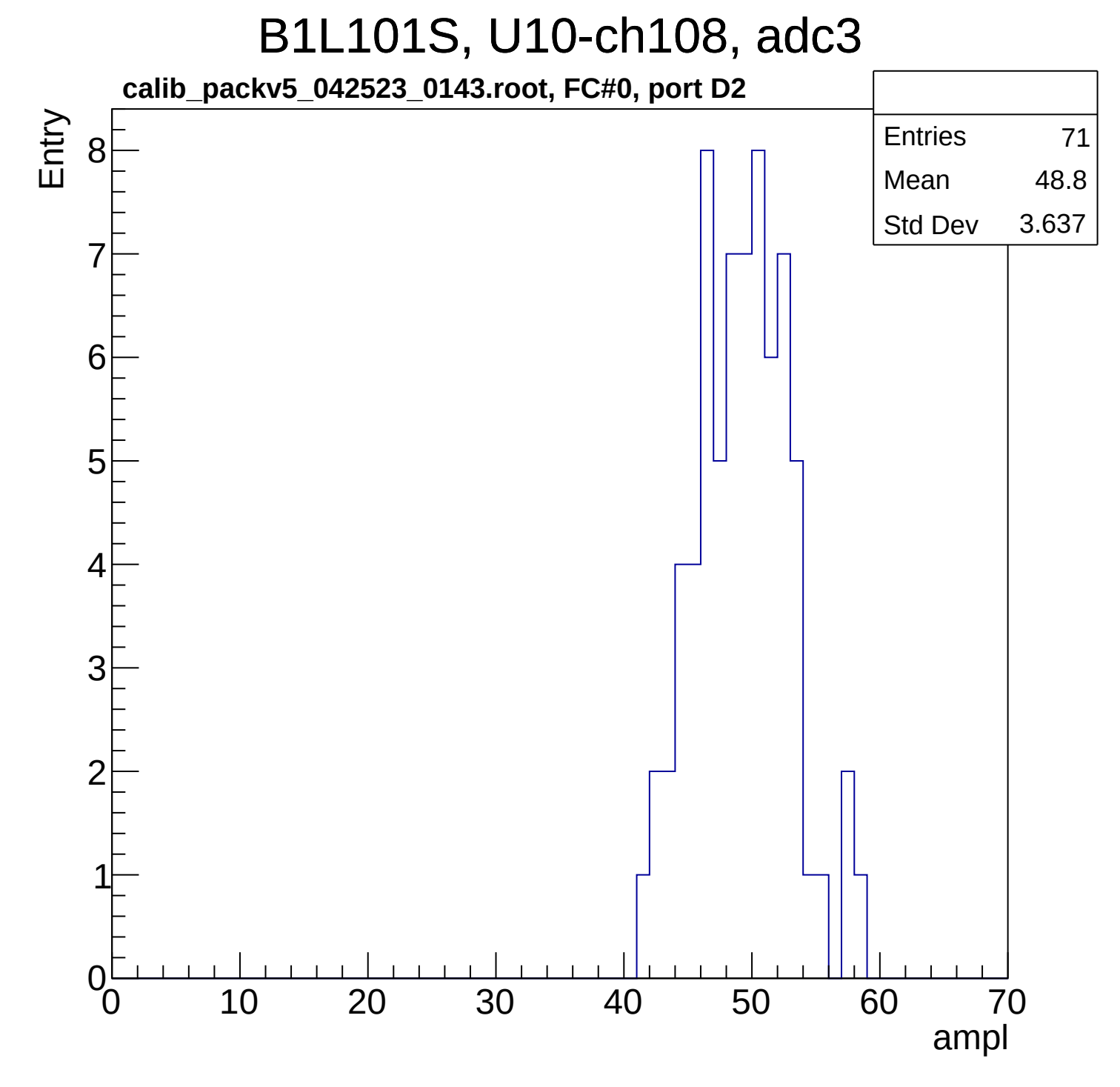
B1L101S, U10-ch108, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 48.8
Std Dev 3.637
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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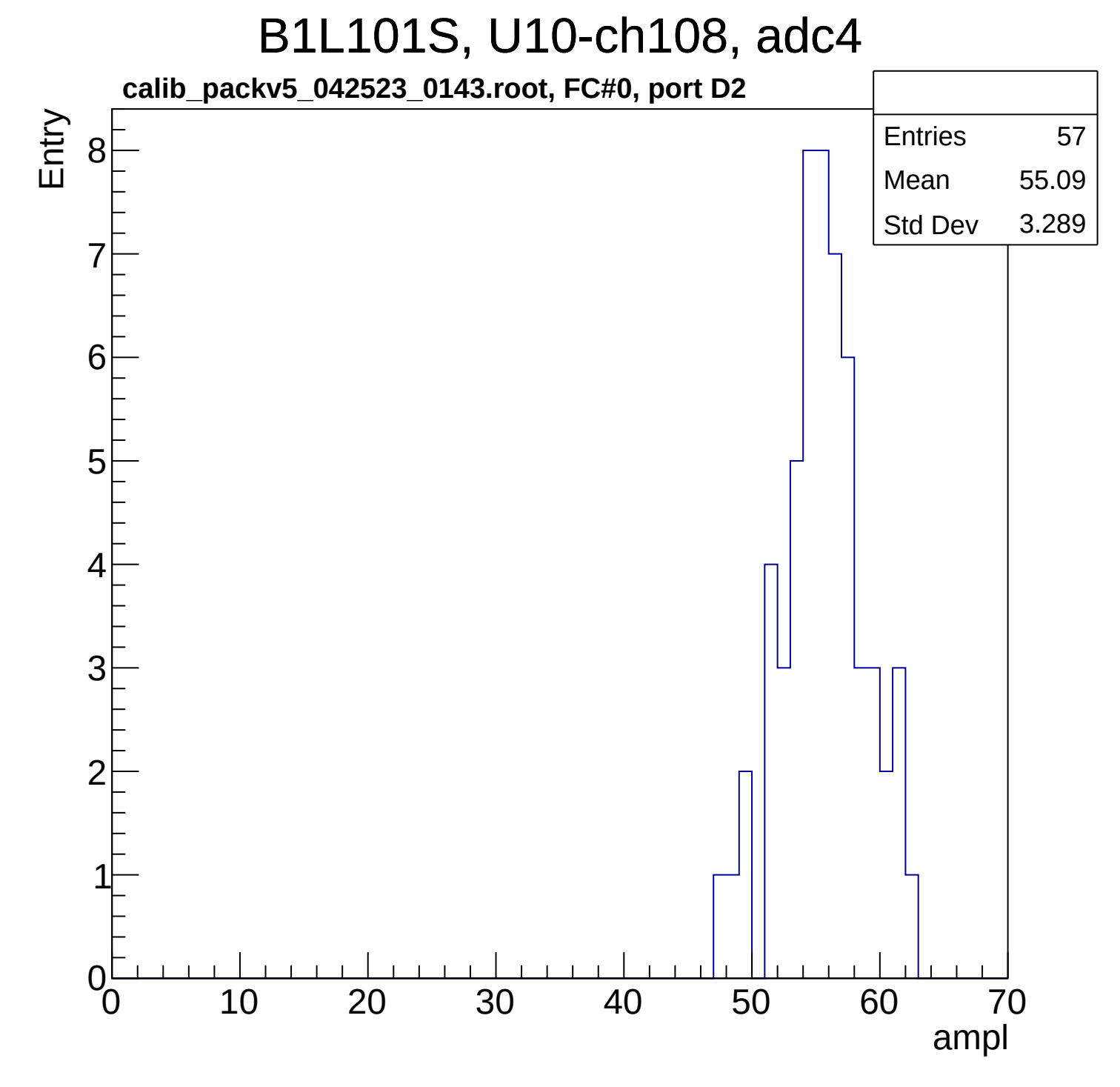
B1L101S, U10-ch108, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 55.09
Std Dev 3.289
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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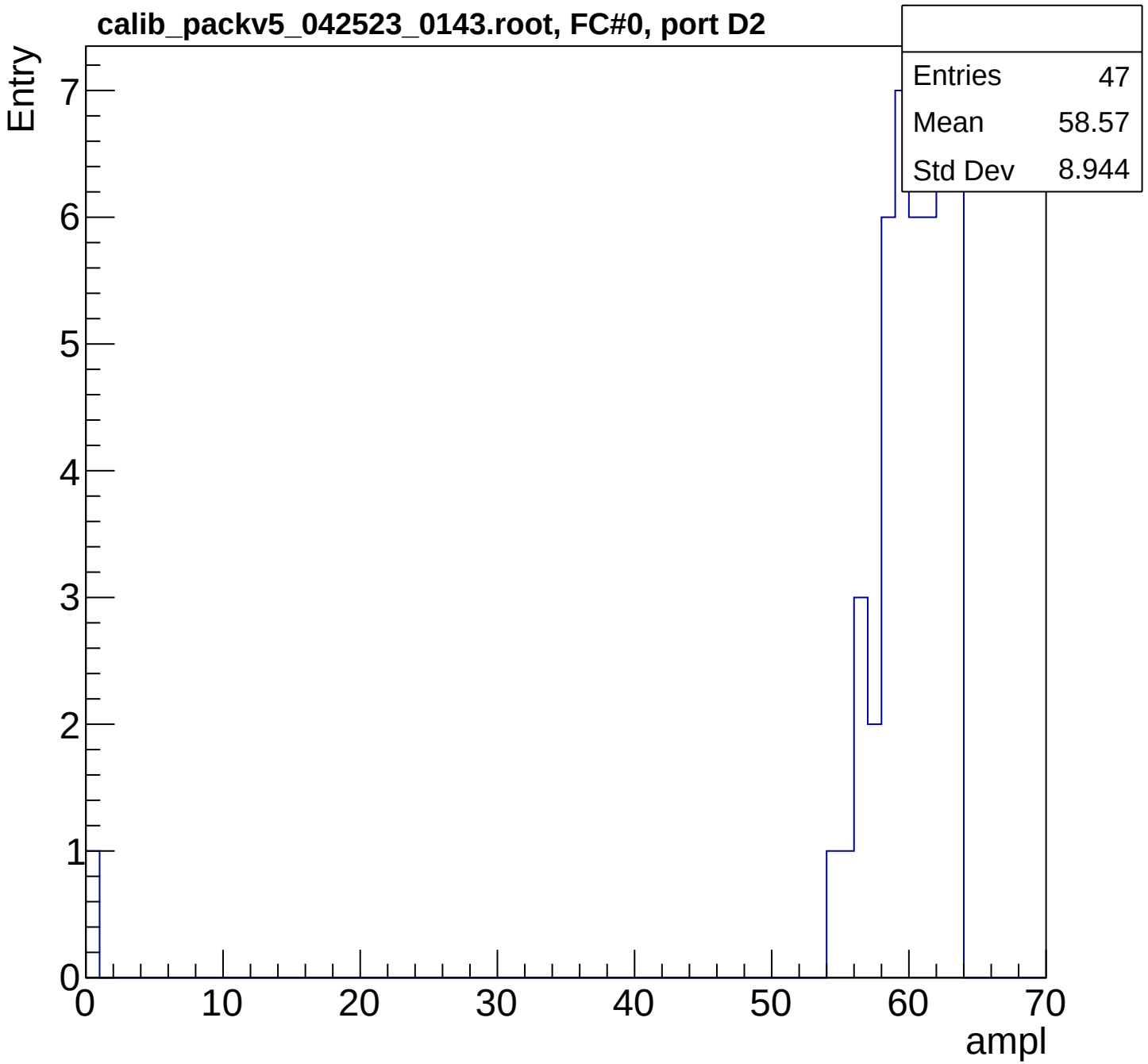
B1L101S, U10-ch108, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 58.57
Std Dev 8.944
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
50
60
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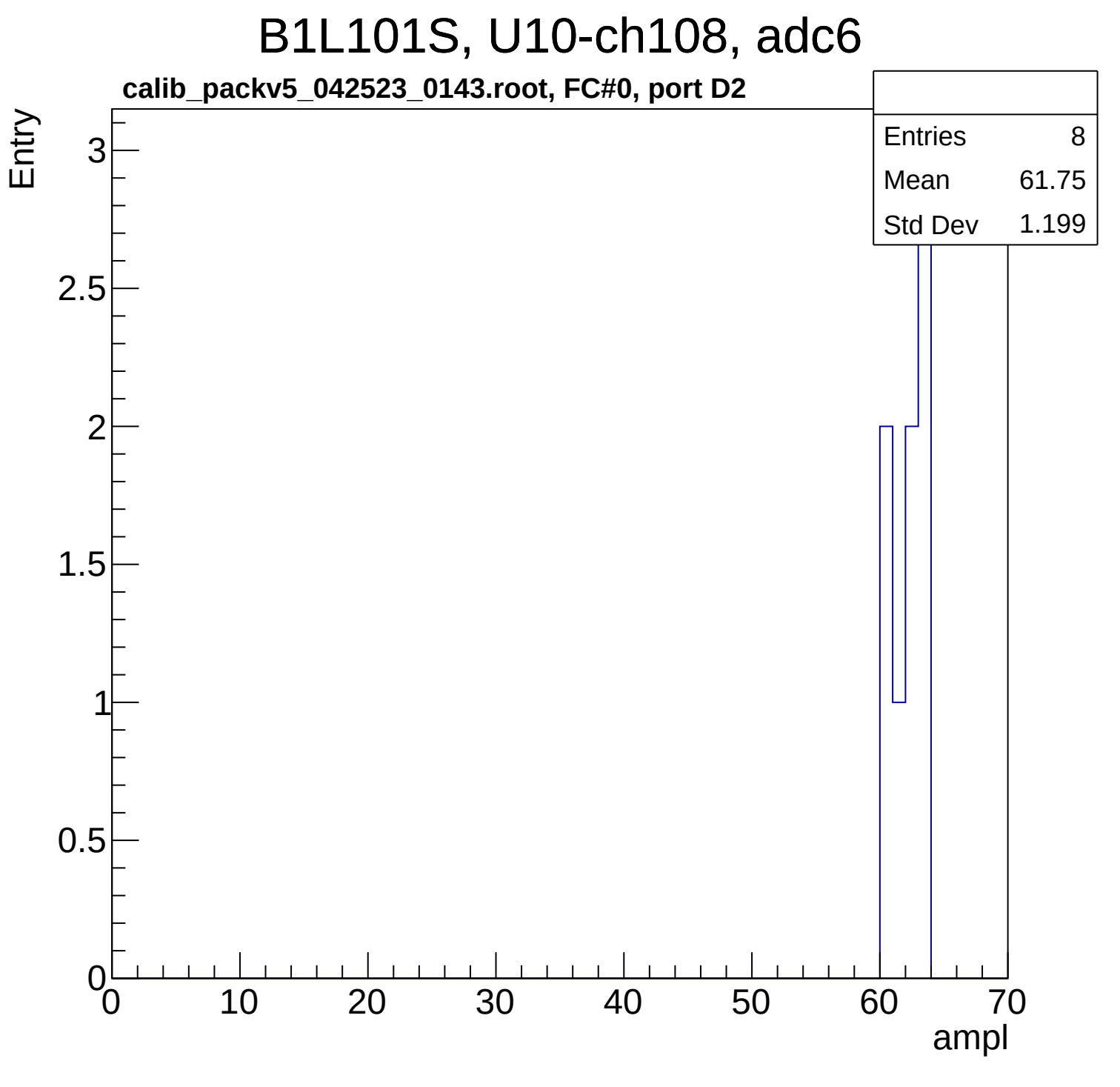
B1L101S, U10-ch108, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 61.75
Std Dev 1.199
Entry
ampl
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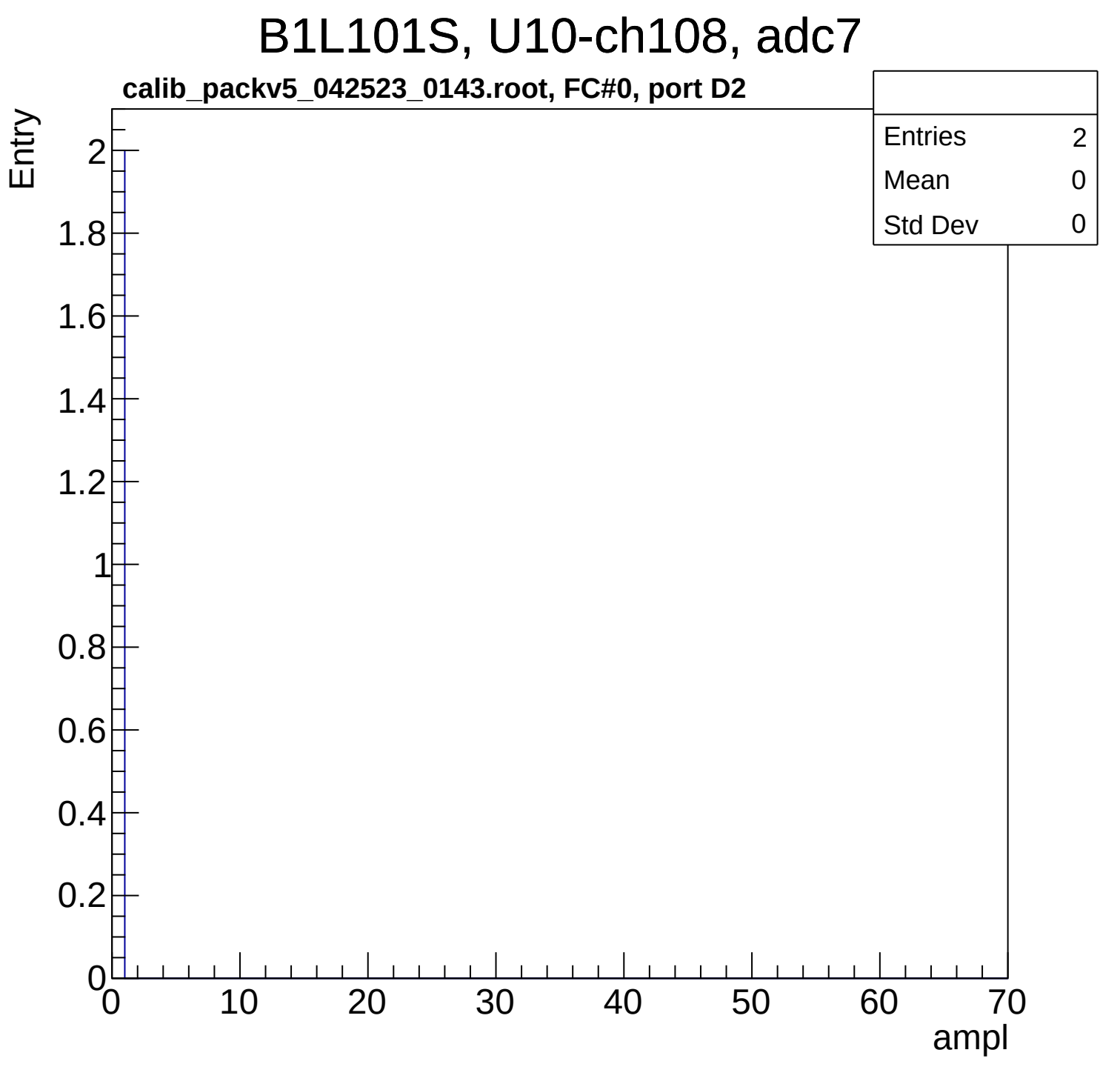
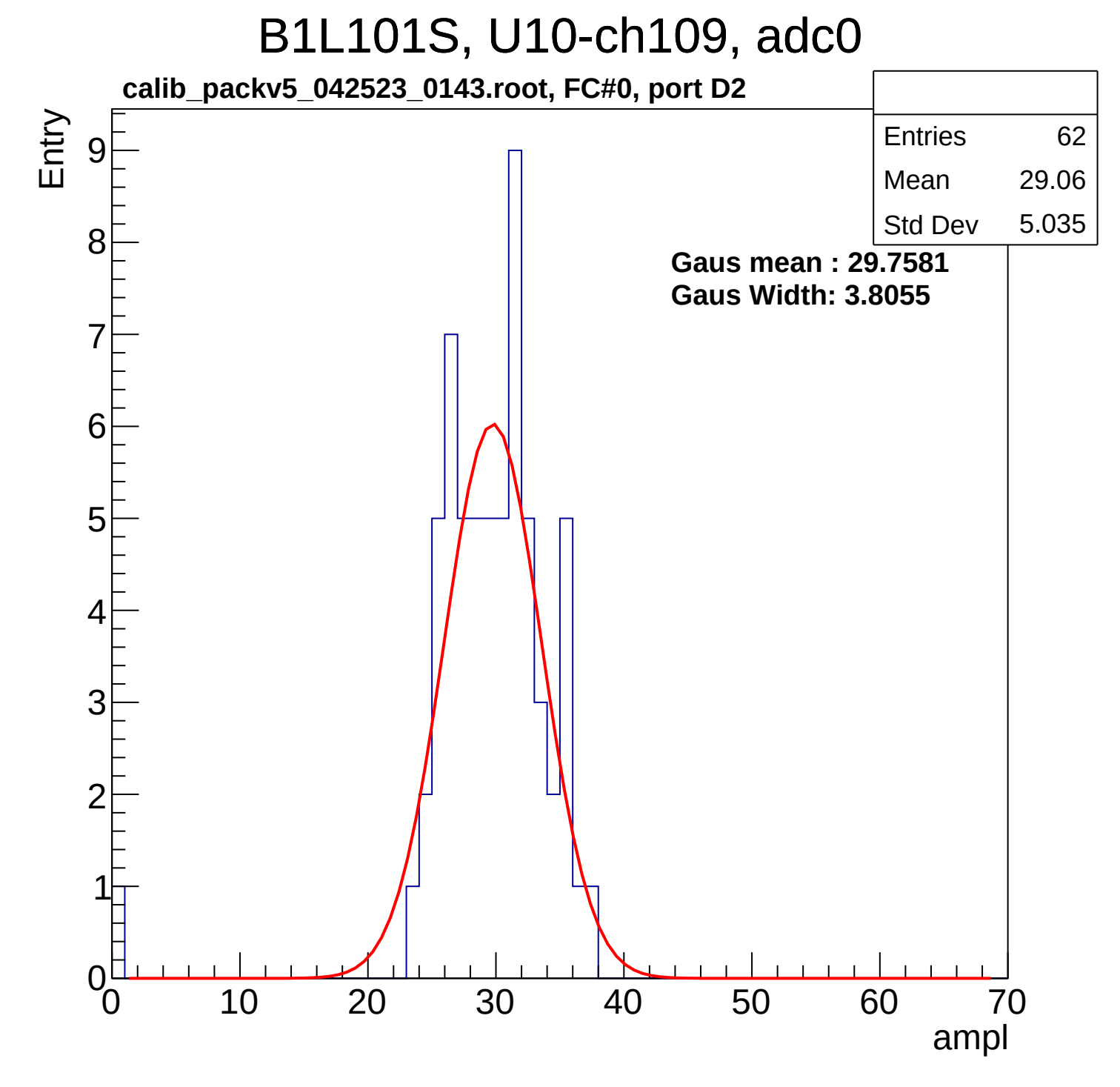
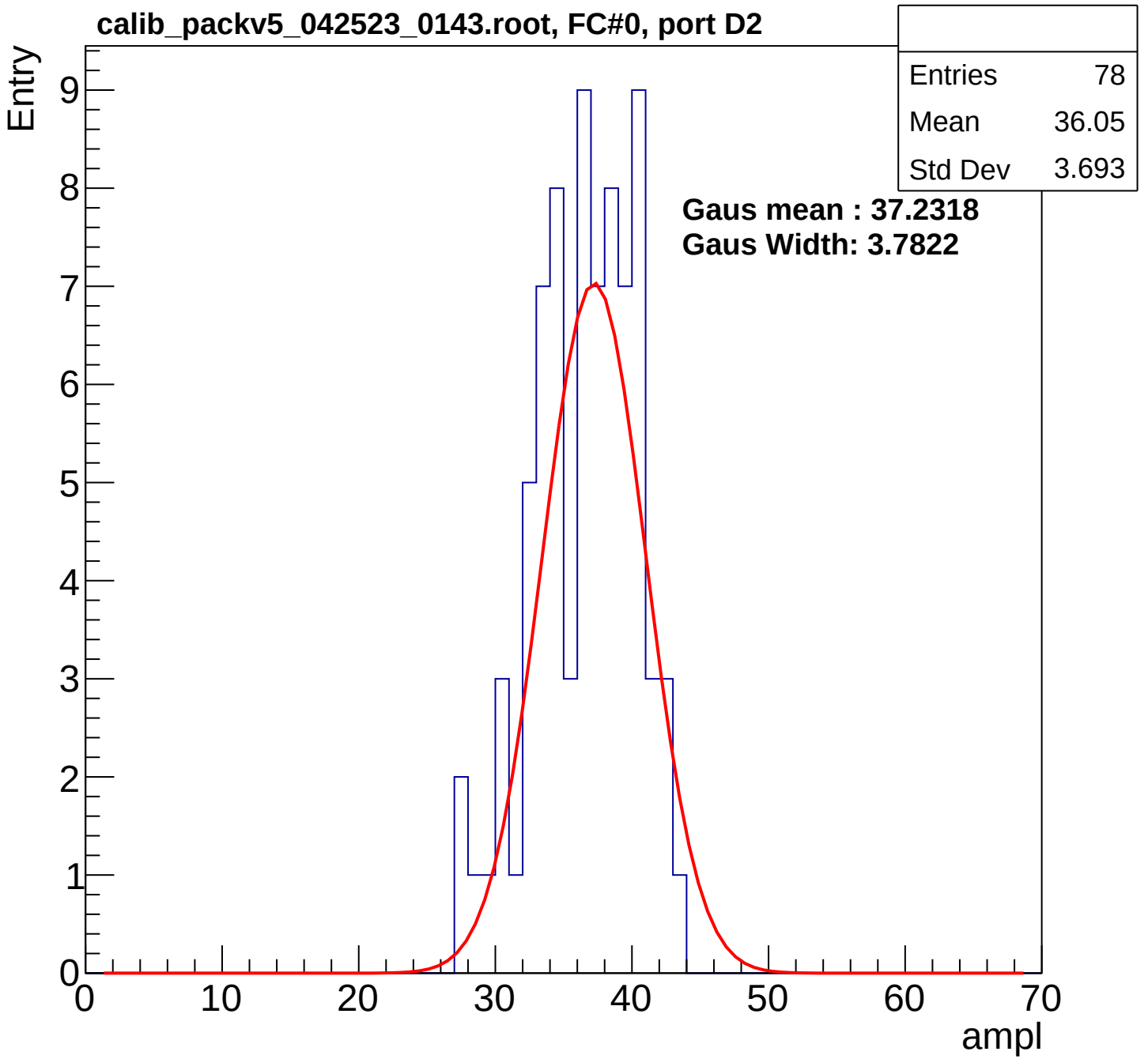
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U10-ch108, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch109, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 29.06
Std Dev 5.035
Gaus mean : 29.7581
Gaus Width: 3.8055
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch109, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 36.05
Std Dev 3.693
Gaus mean : 37.2318
Gaus Width: 3.7822
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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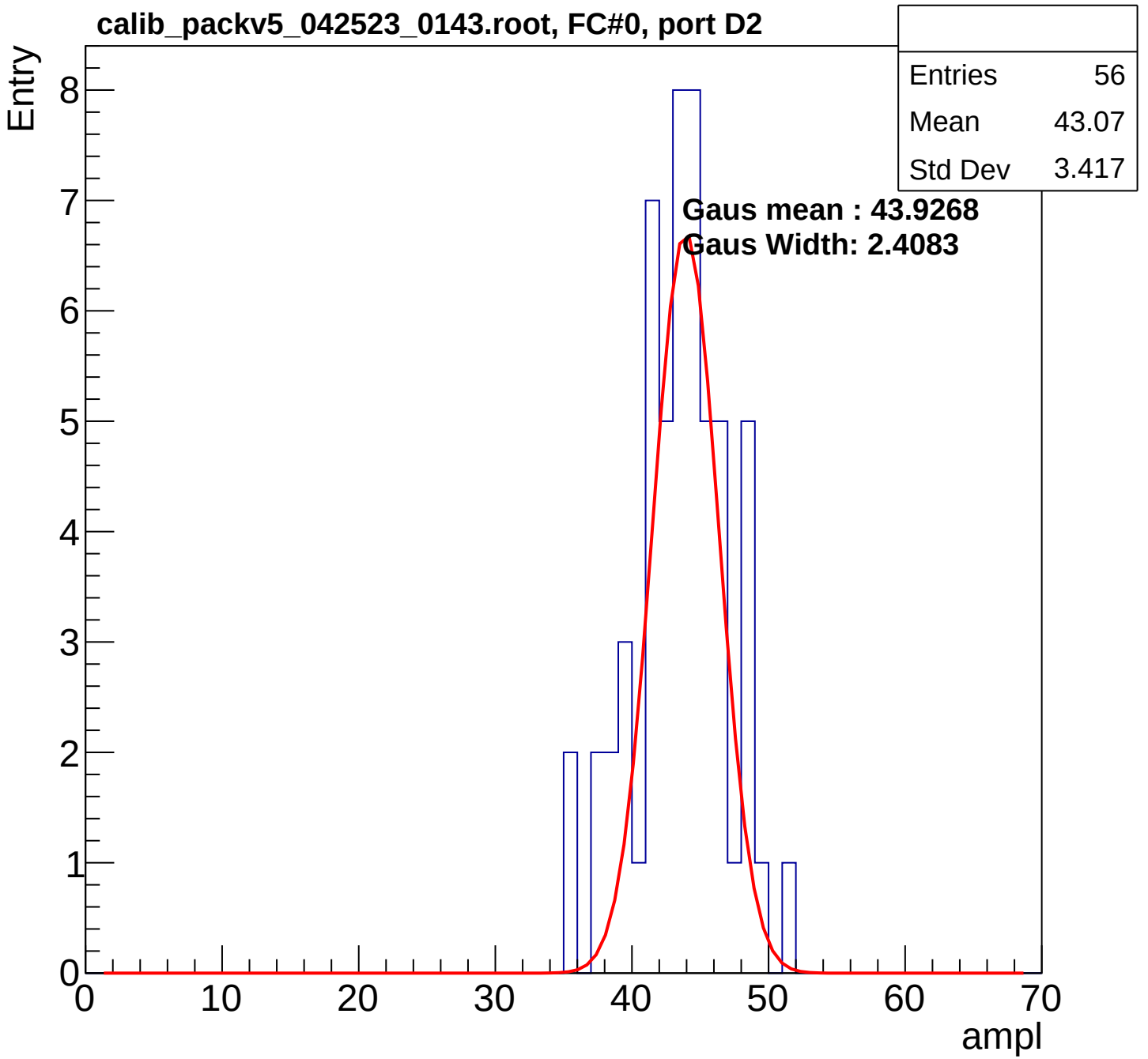
B1L101S, U10-ch109, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 43.07
Std Dev 3.417
Gaus mean : 43.9268
Gaus Width: 2.4083
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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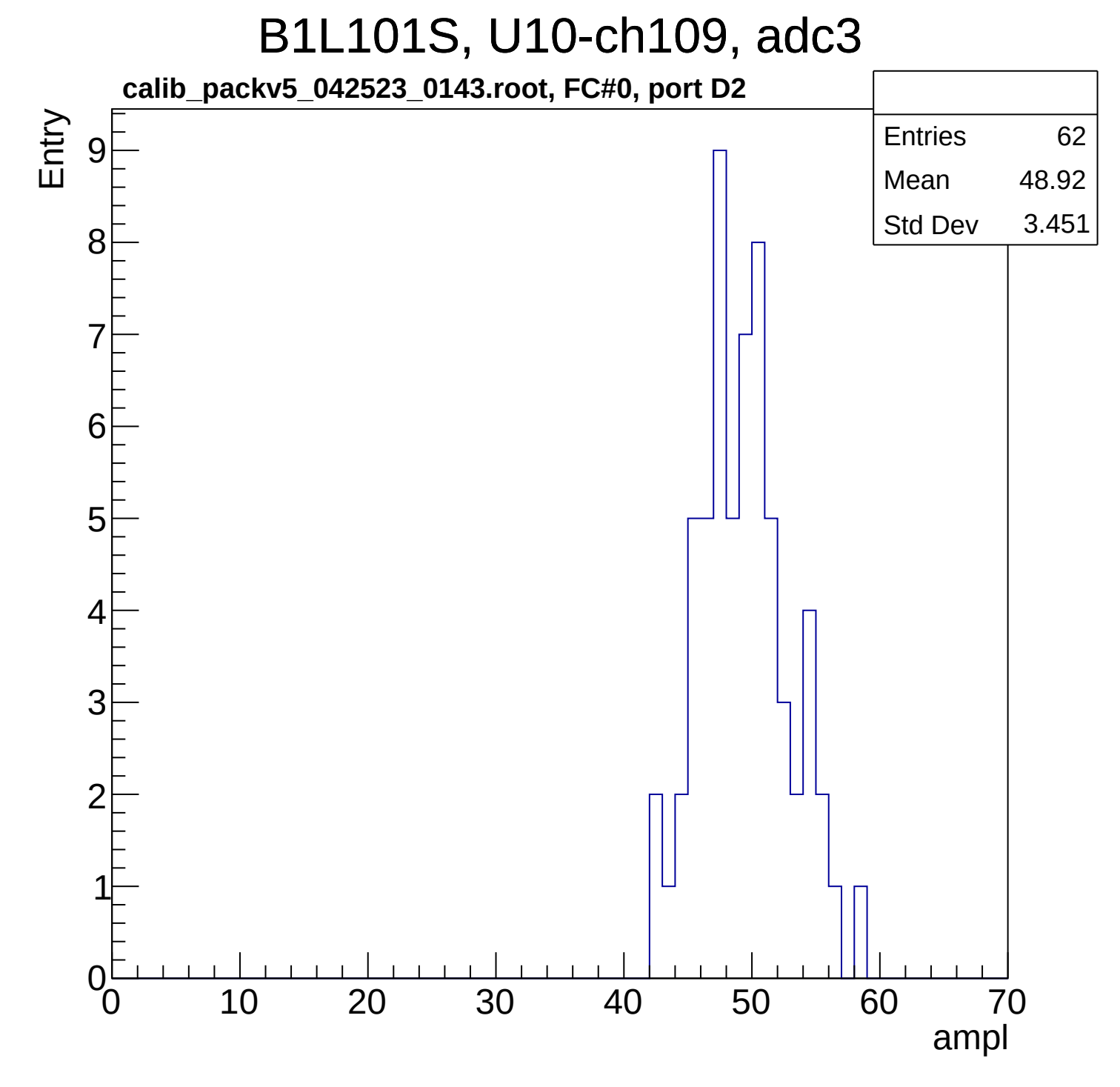
B1L101S, U10-ch109, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 48.92
Std Dev 3.451
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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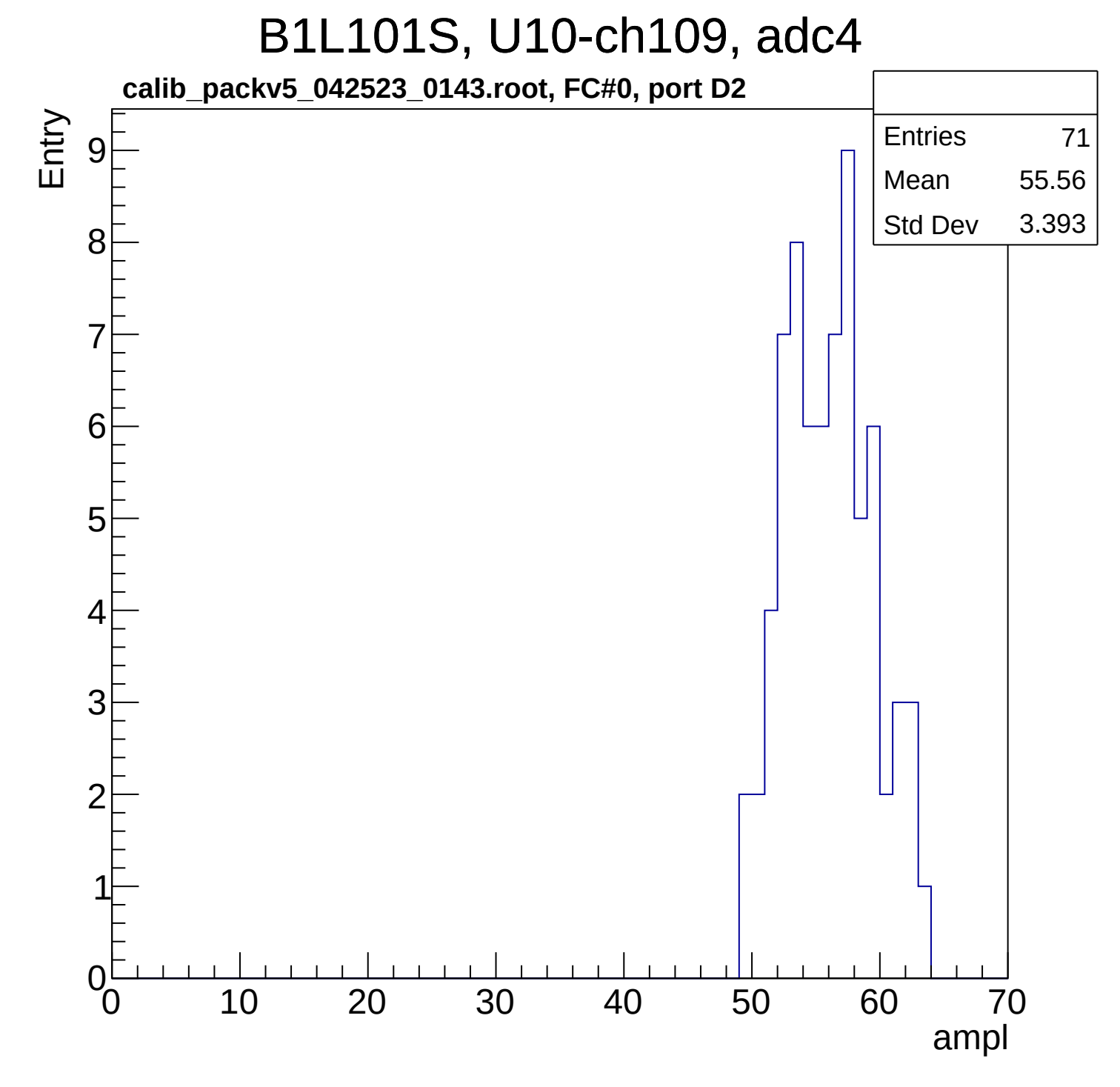
B1L101S, U10-ch109, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 55.56
Std Dev 3.393
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
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40
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60
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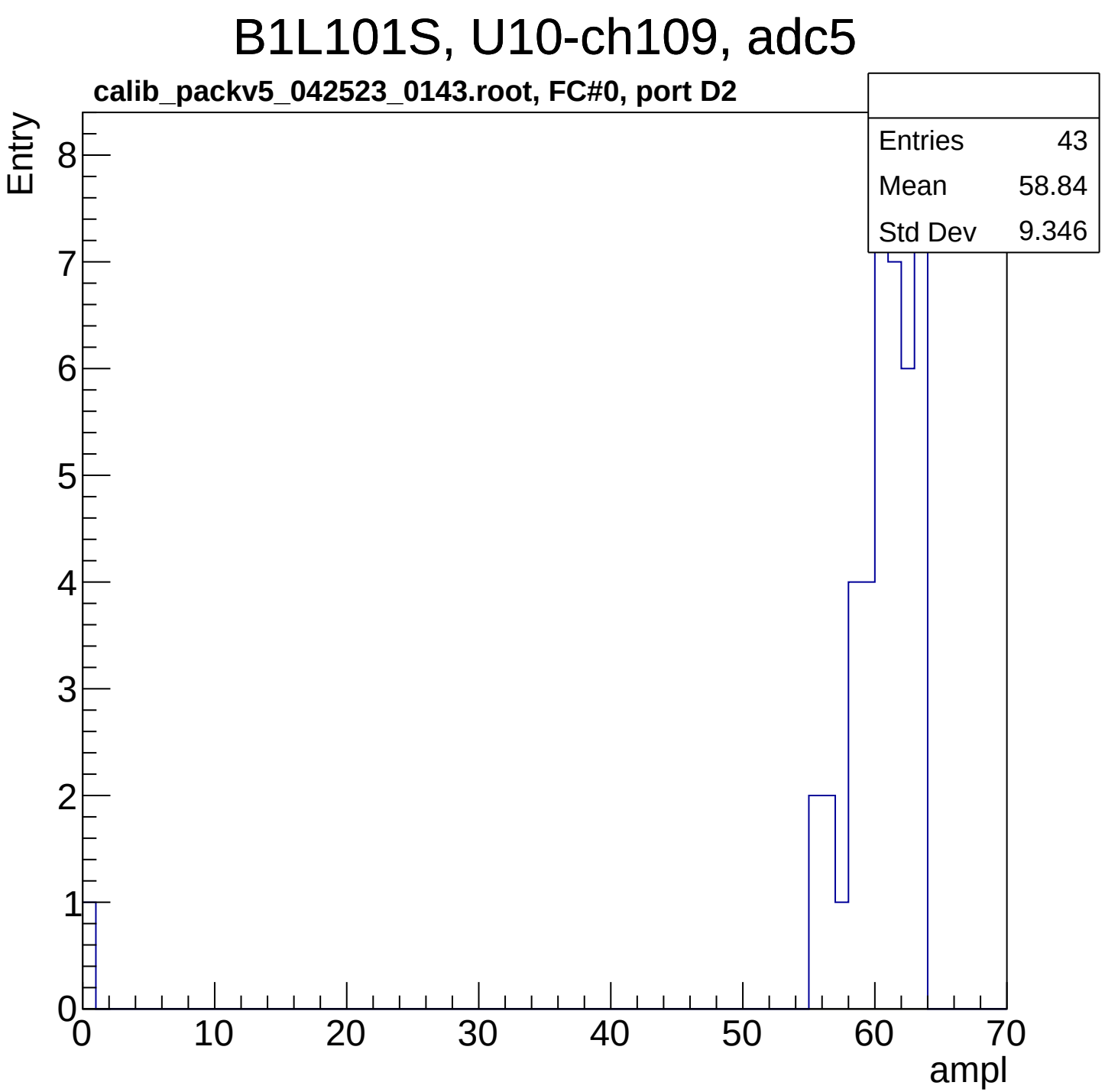
B1L101S, U10-ch109, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 43
Mean 58.84
Std Dev 9.346
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
50
60
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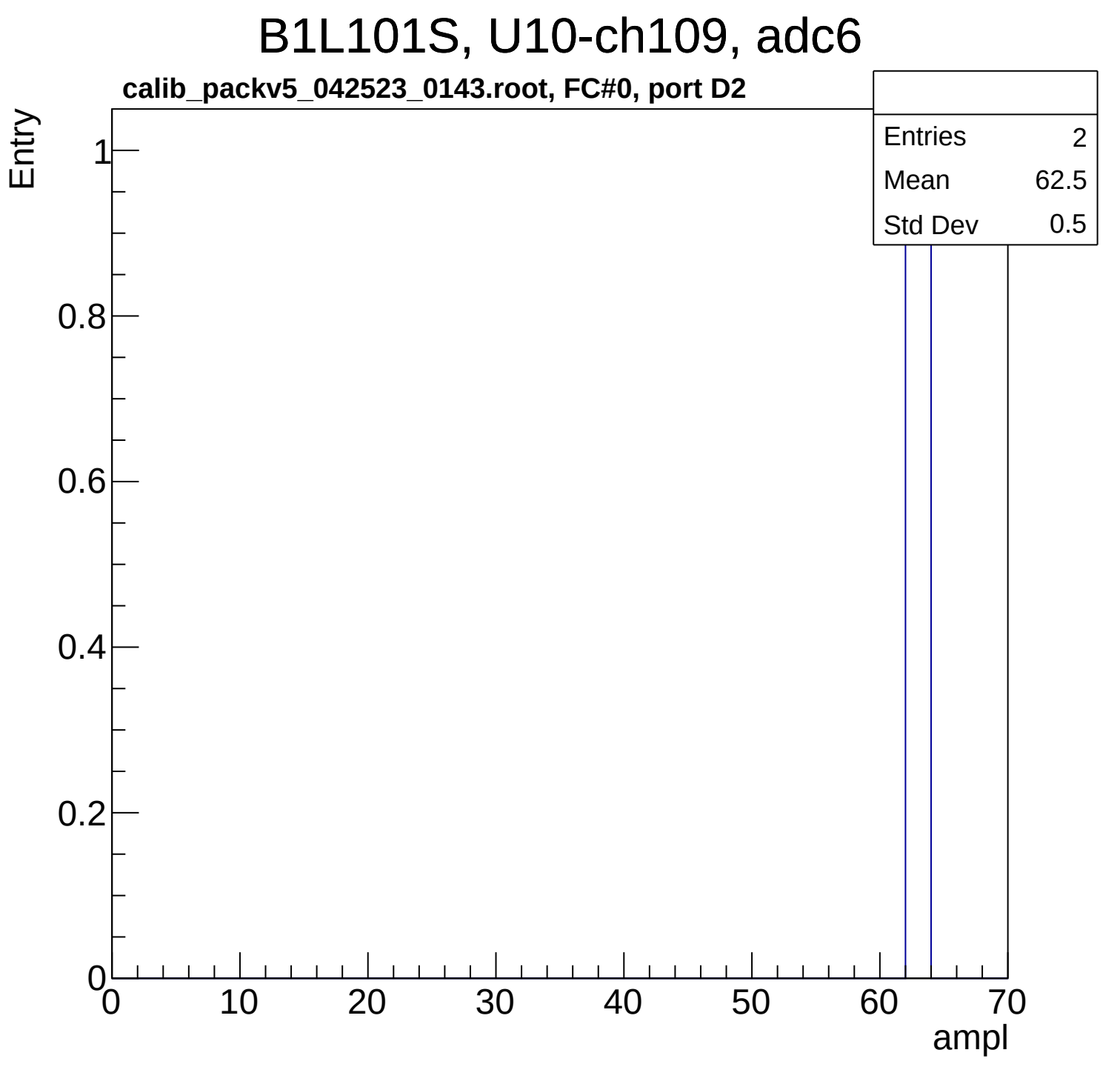
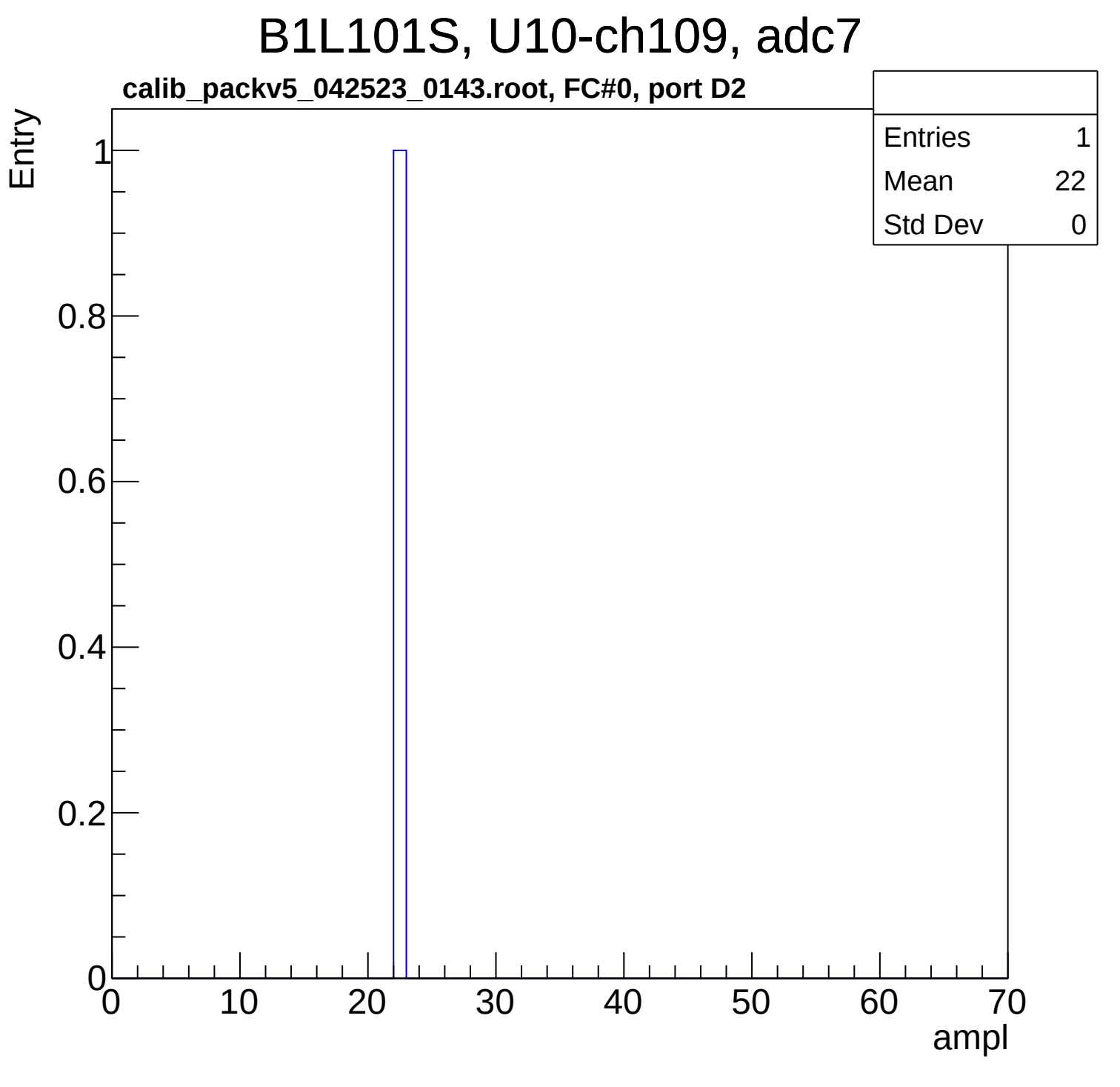

B1L101S, U10-ch109, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch109, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 22
Std Dev 0
Entry
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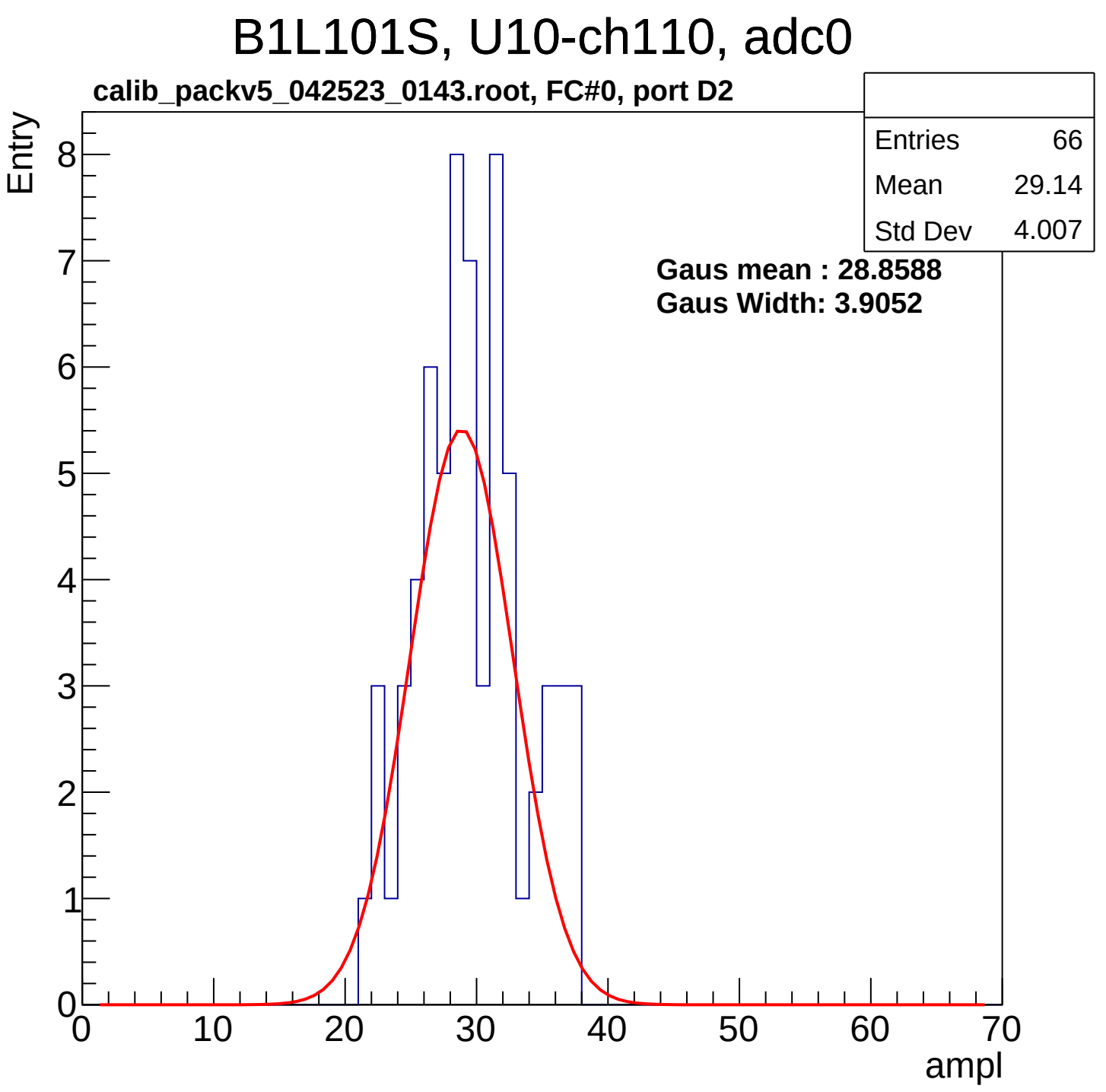
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch110, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 29.14
Std Dev 4.007
Gaus mean : 28.8588
Gaus Width: 3.9052
Entry
ampl
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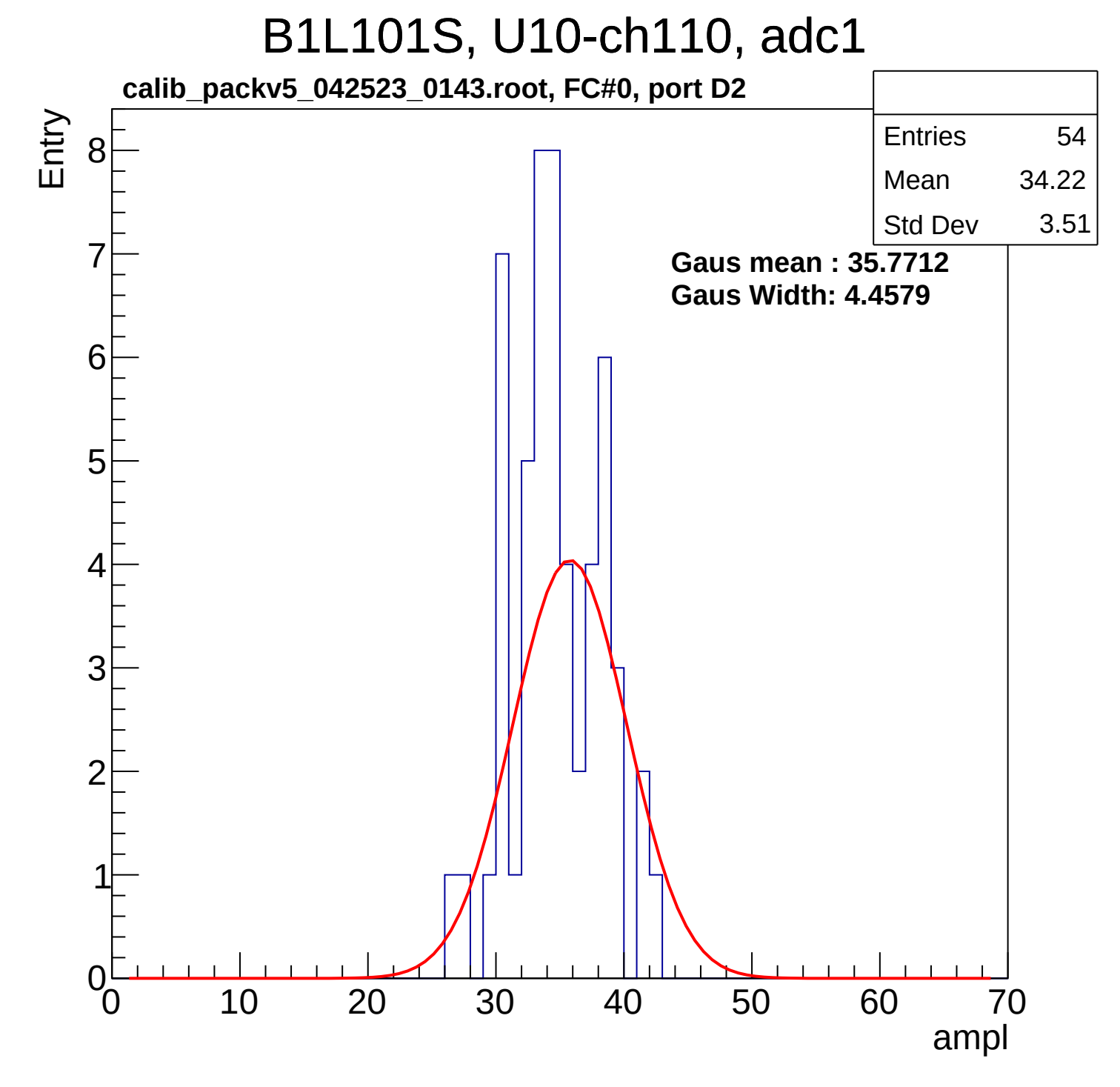
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch110, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 34.22
Std Dev 3.51
Gaus mean : 35.7712
Gaus Width: 4.4579
Entry
ampl
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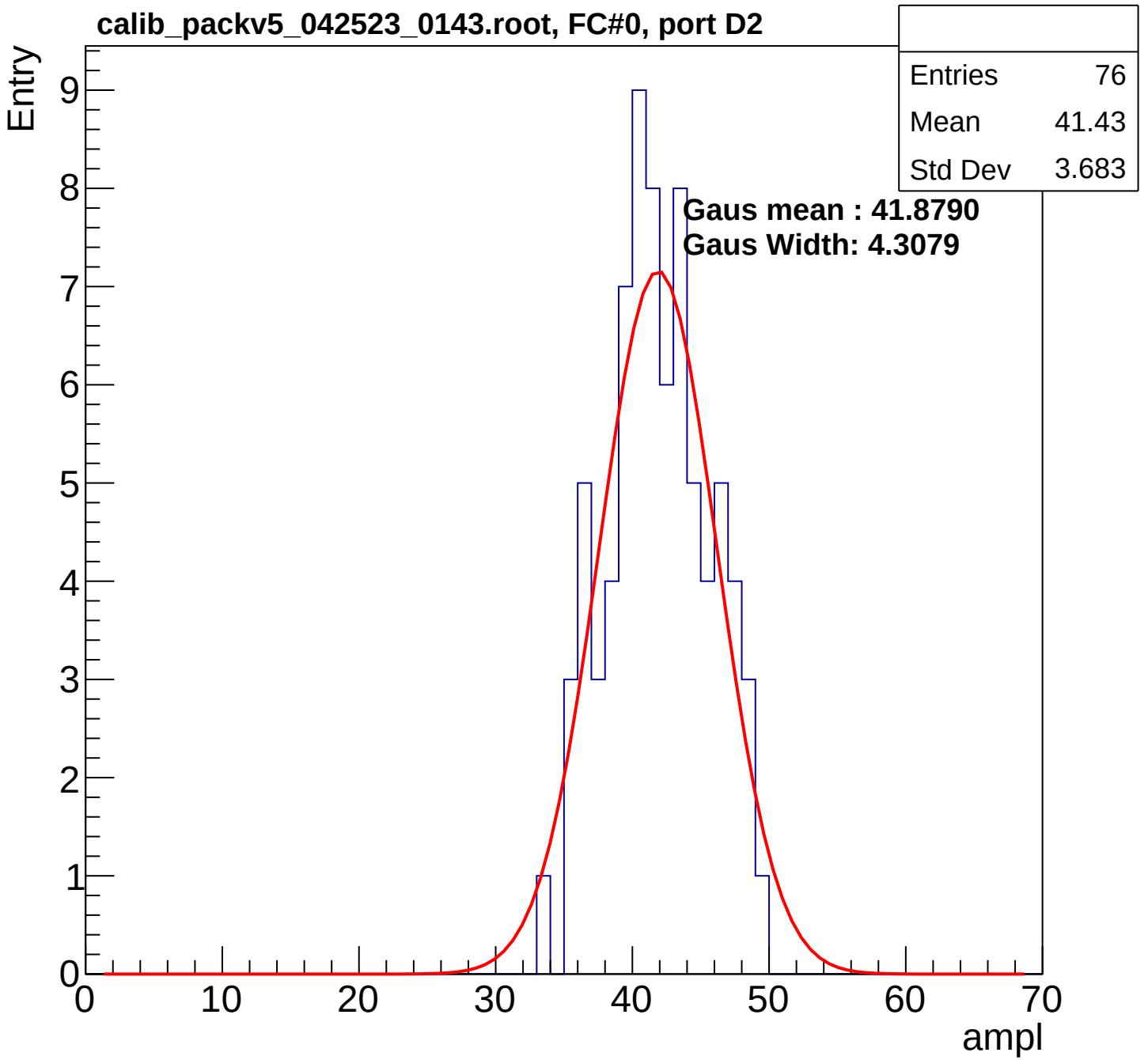
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch110, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 41.43
Std Dev 3.683
Gaus mean : 41.8790
Gaus Width: 4.3079
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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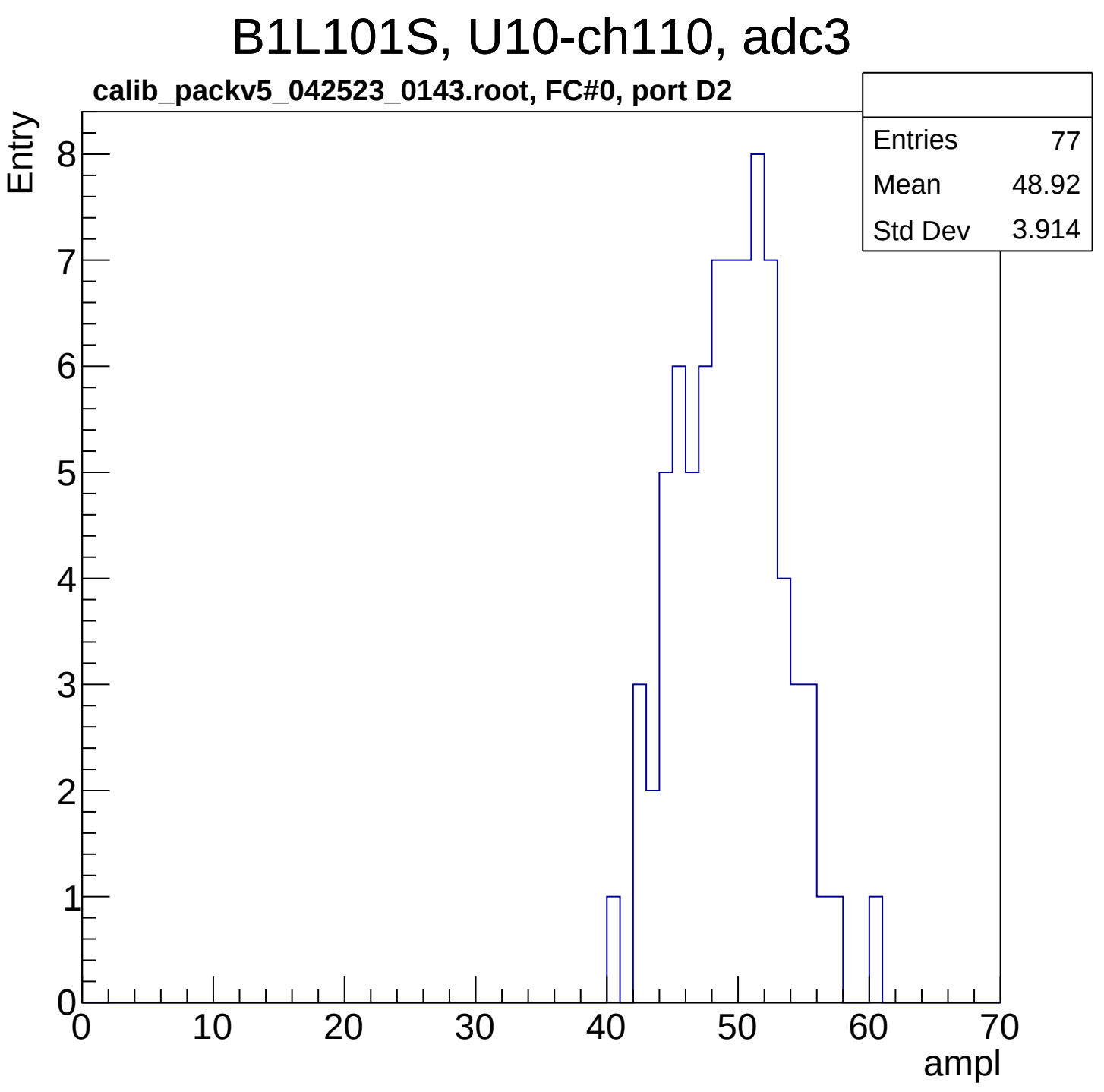
B1L101S, U10-ch110, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 48.92
Std Dev 3.914
Entry
ampl
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6
7
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40
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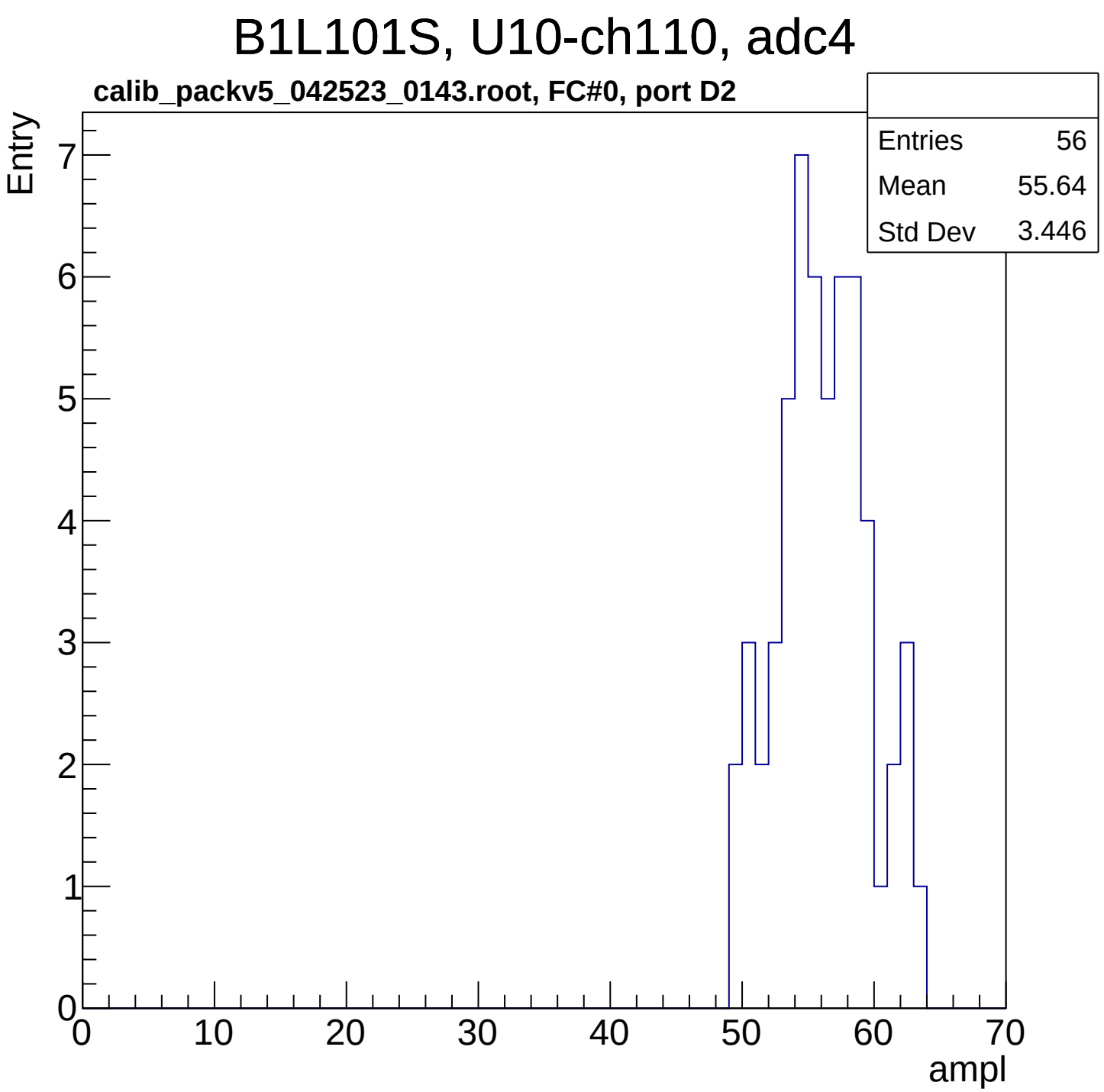
60
70


B1L101S, U10-ch110, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 55.64
Std Dev 3.446
Entry
ampl
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3
4
5
6
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0
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20
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40
50
60
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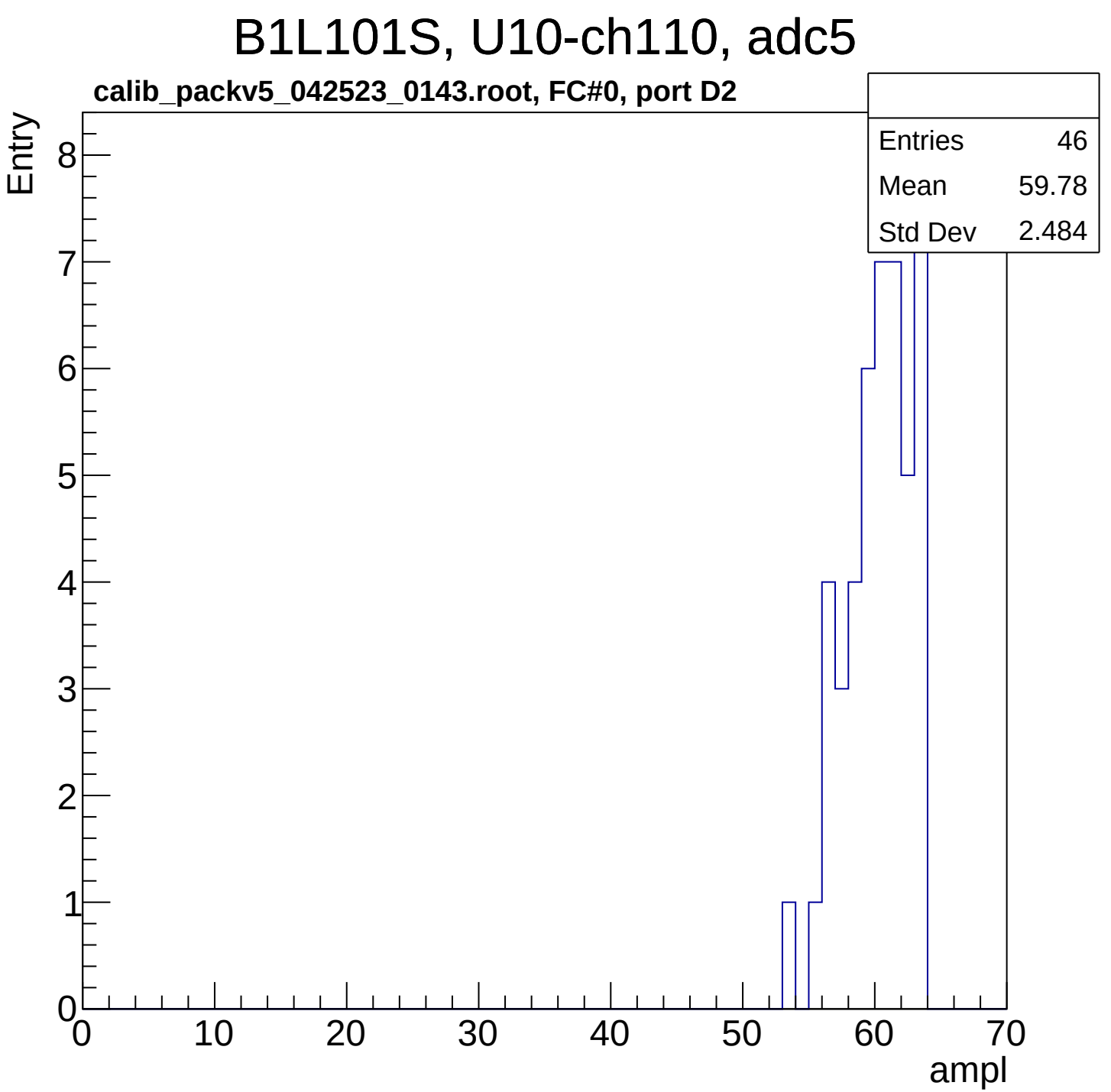
B1L101S, U10-ch110, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 59.78
Std Dev 2.484
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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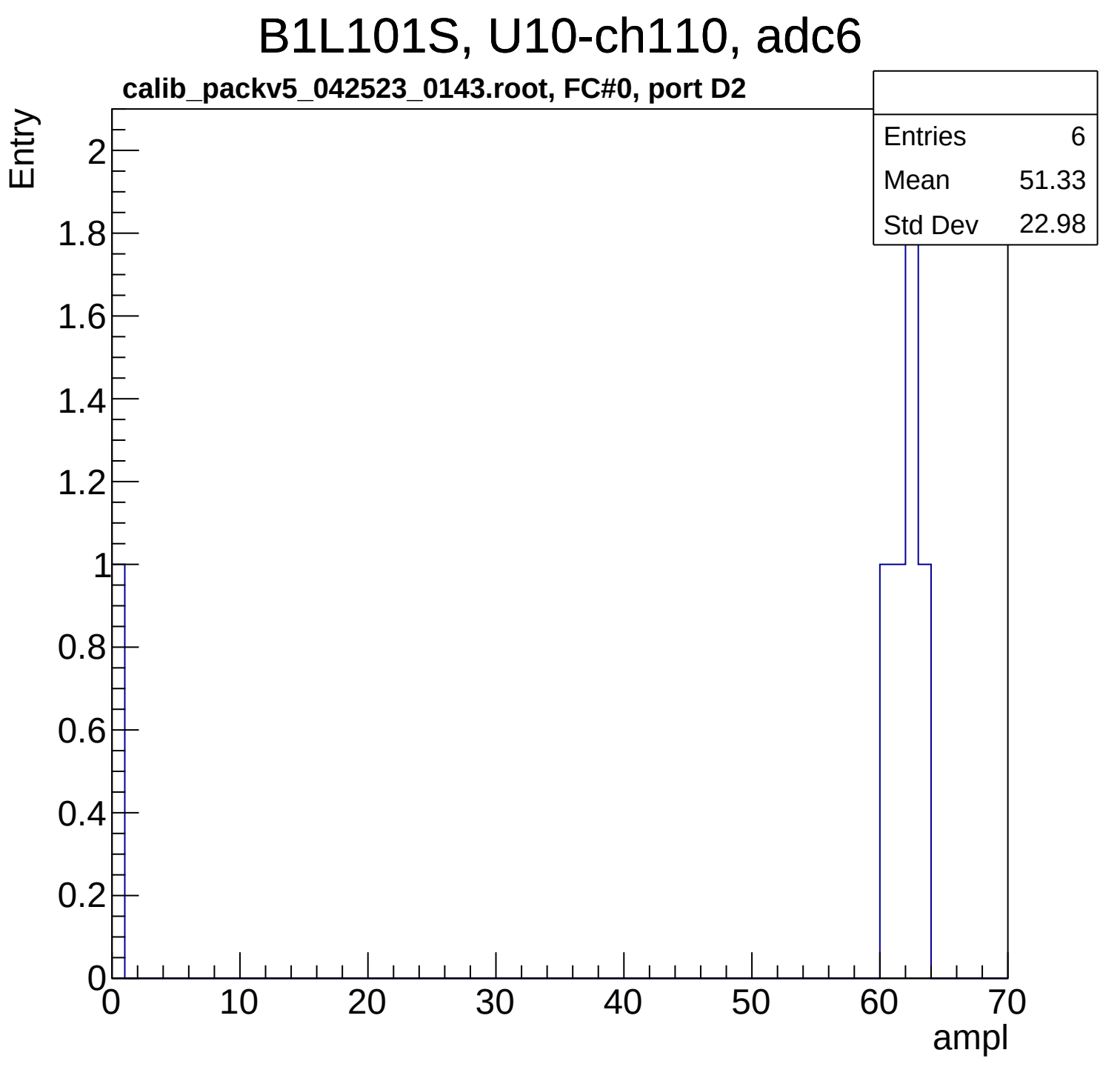
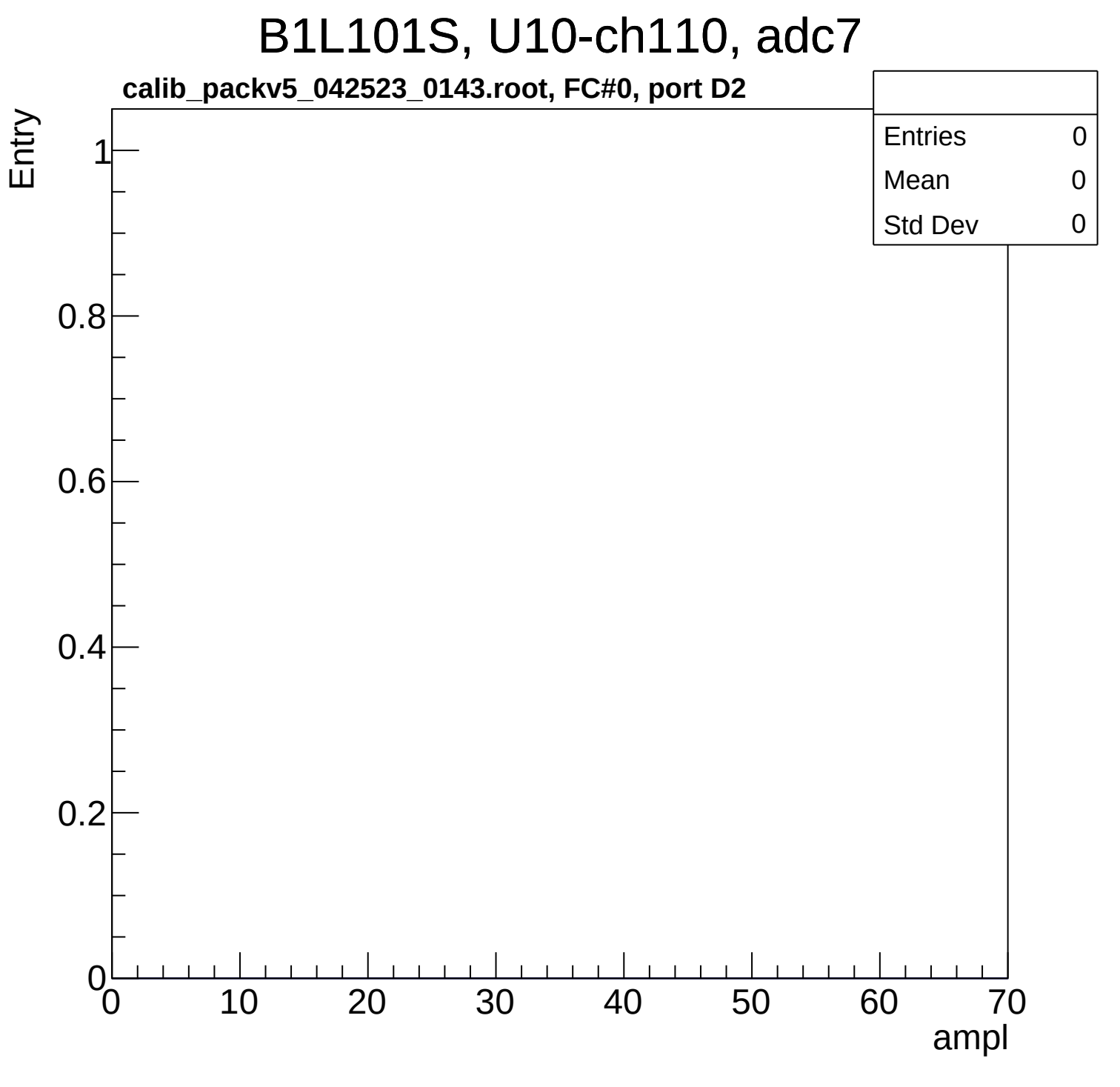
40
50
60
70


B1L101S, U10-ch110, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 51.33
Std Dev 22.98
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U10-ch110, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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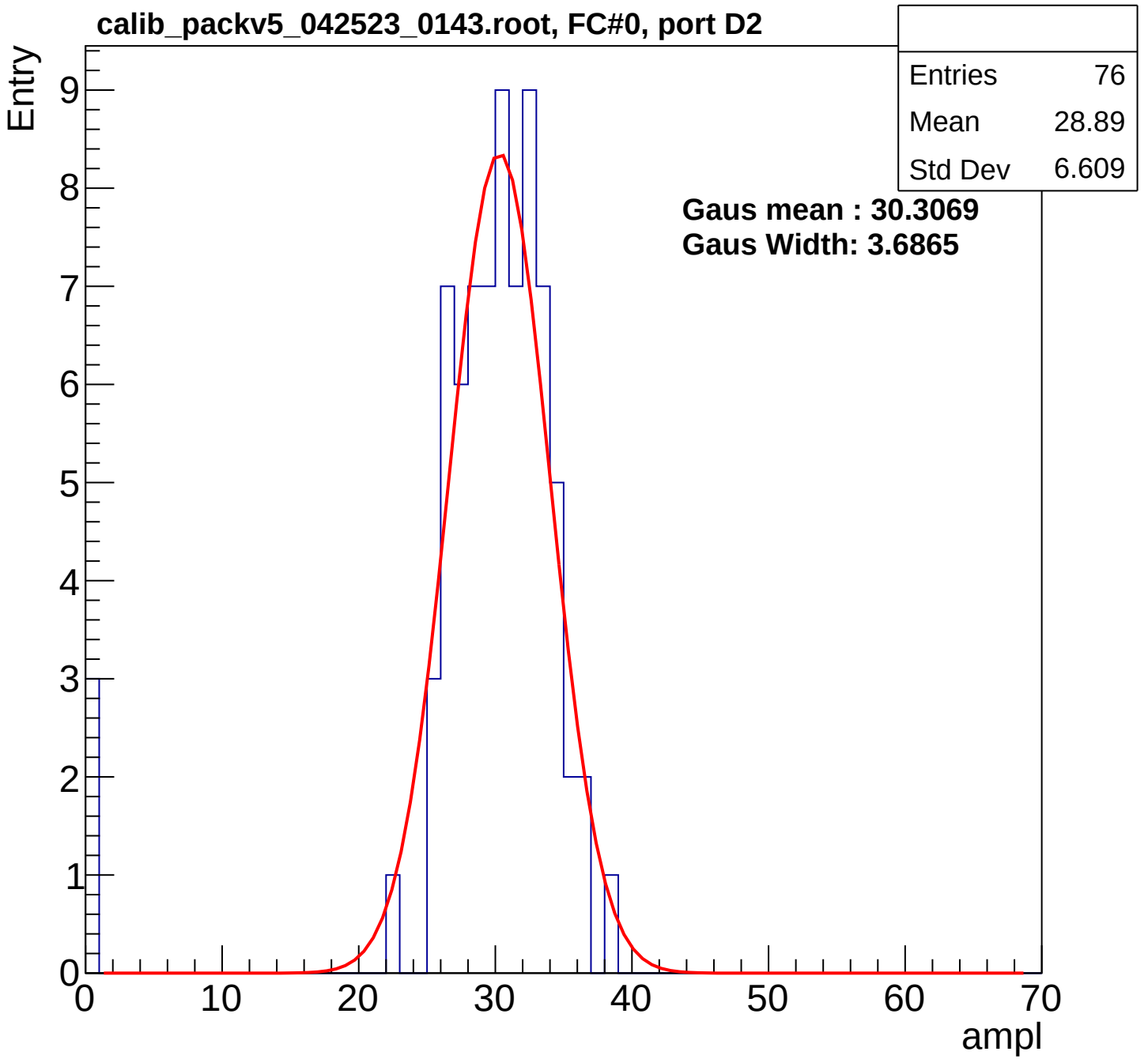
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch111, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 28.89
Std Dev 6.609
Gaus mean : 30.3069
Gaus Width: 3.6865
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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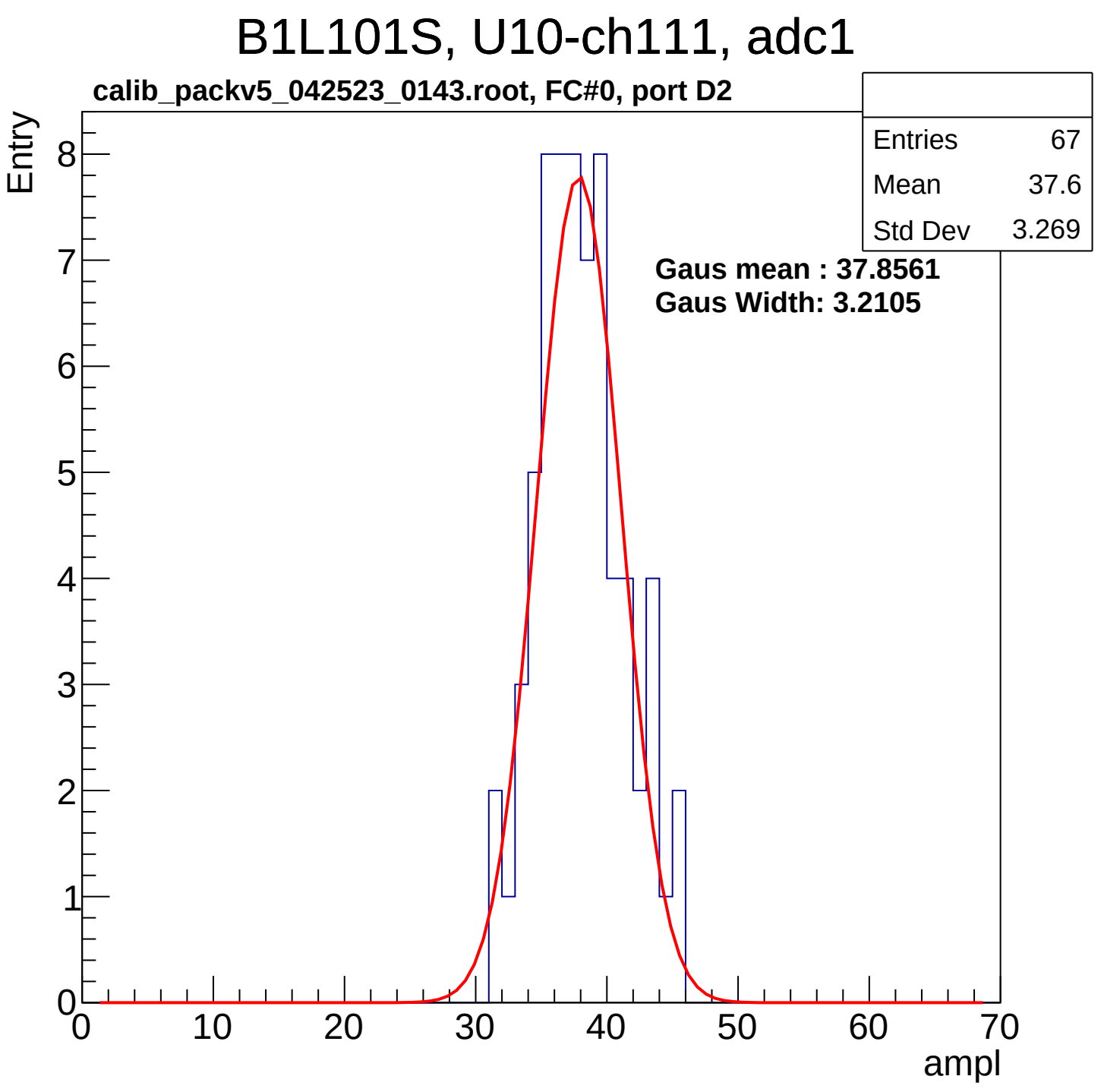
B1L101S, U10-ch111, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 37.6
Std Dev 3.269
Gaus mean : 37.8561
Gaus Width: 3.2105
Entry
ampl
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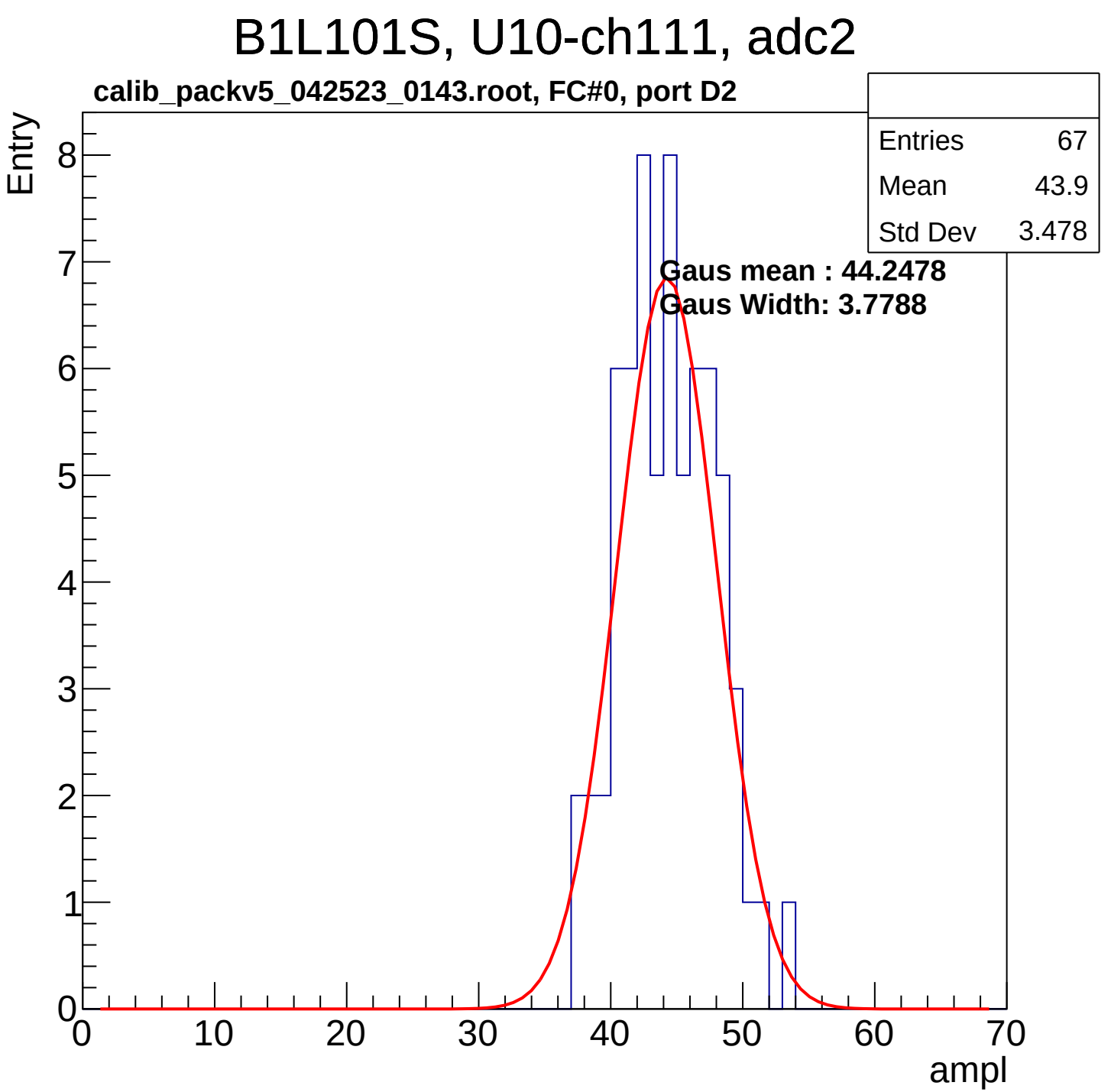
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch111, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 43.9
Std Dev 3.478
Gaus mean : 44.2478
Gaus Width: 3.7788
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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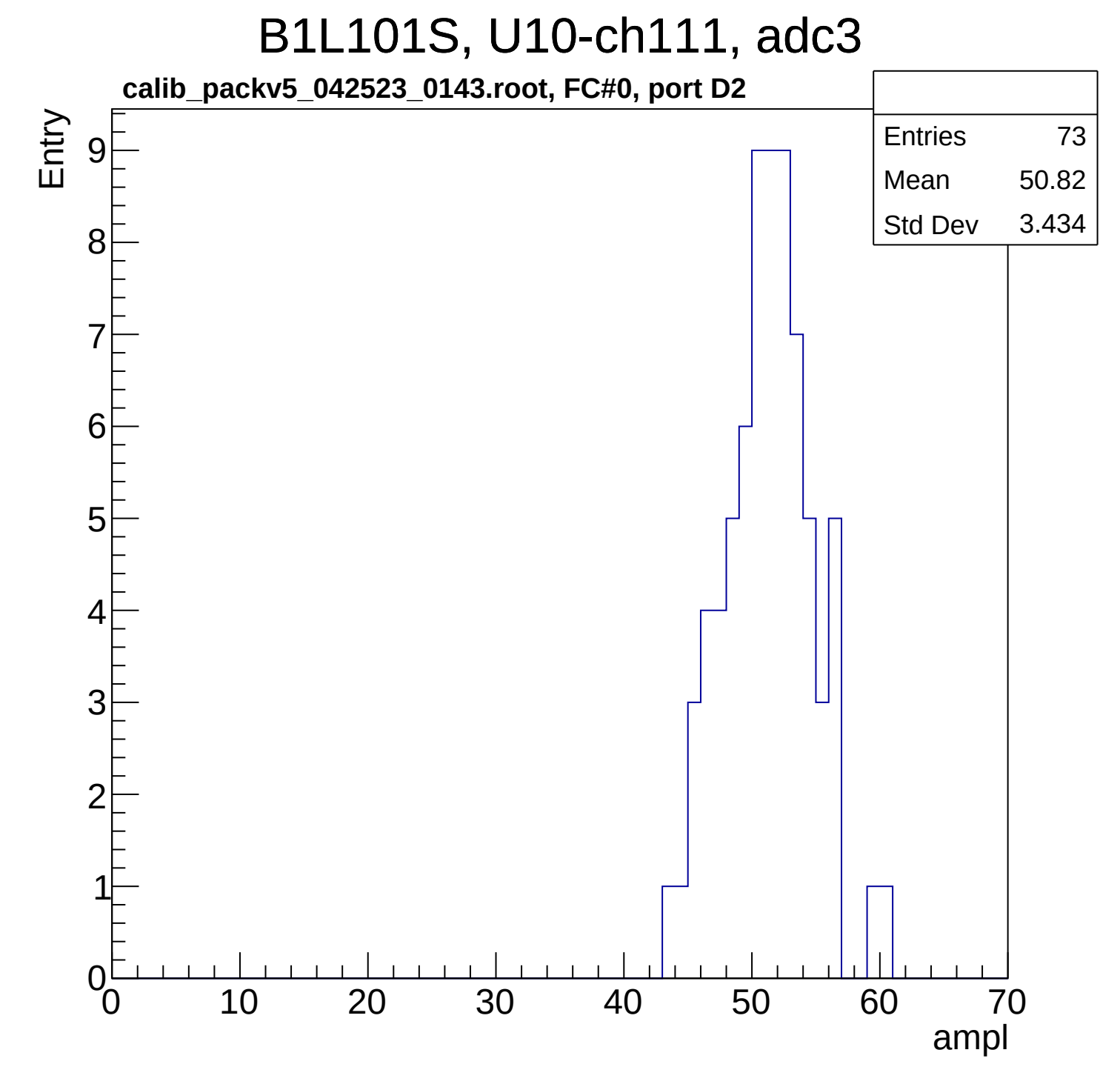
B1L101S, U10-ch111, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 50.82
Std Dev 3.434
Entry
ampl
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3
4
5
6
7
8
9
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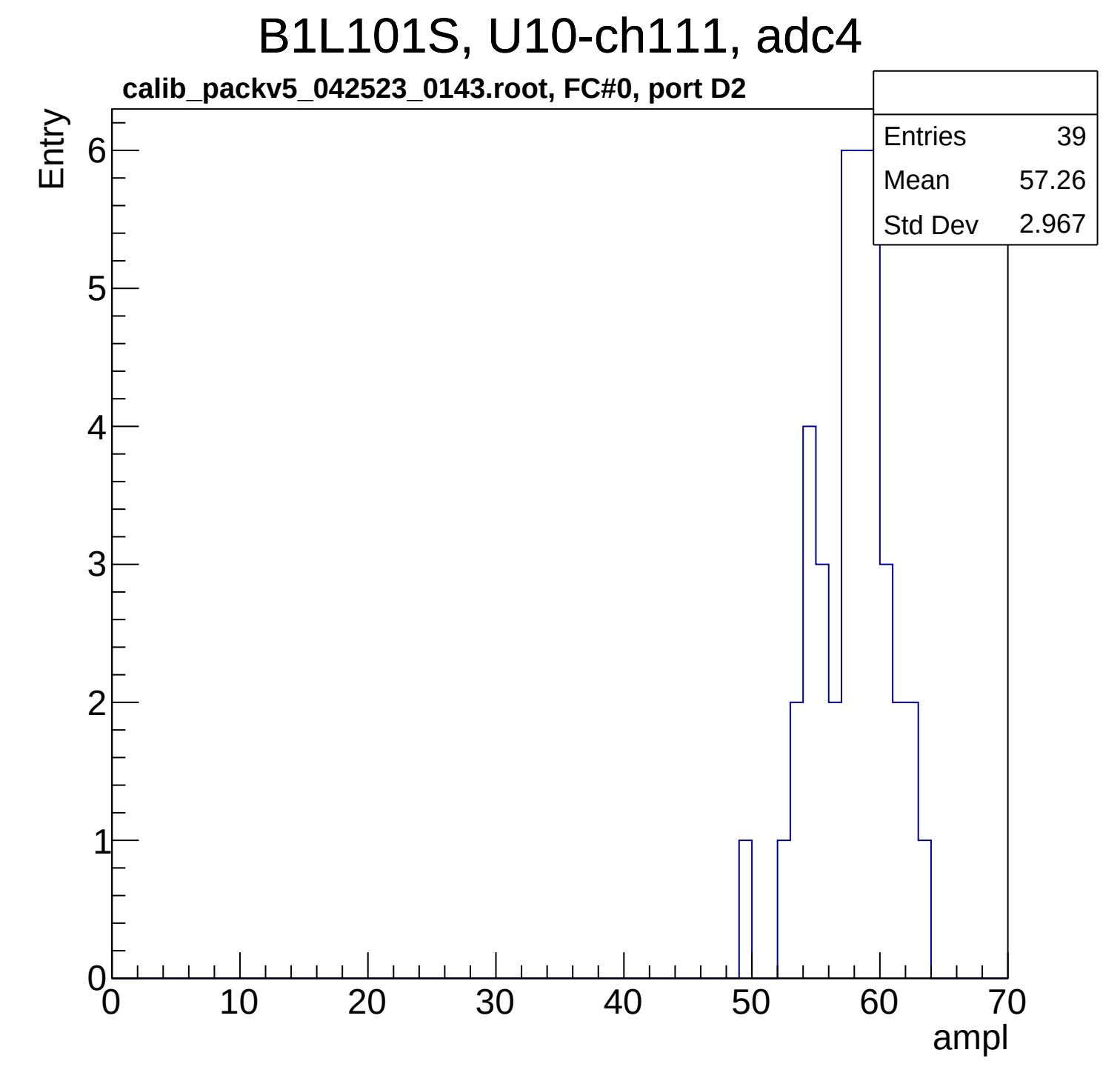
B1L101S, U10-ch111, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 39
Mean 57.26
Std Dev 2.967
Entry
ampl
0
1
2
3
4
5
6
0
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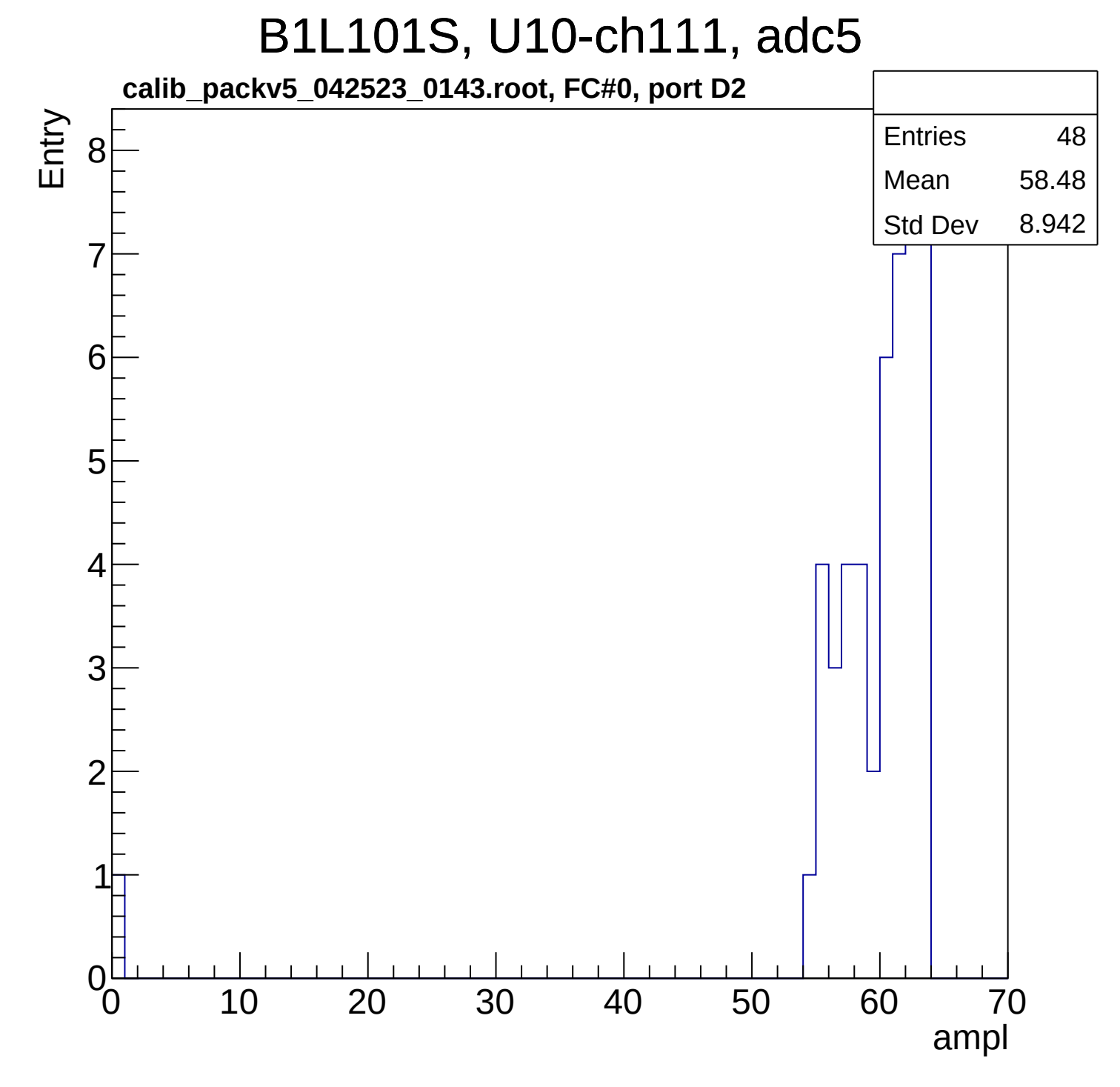
40
50
60
70


B1L101S, U10-ch111, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 58.48
Std Dev 8.942
Entry
ampl
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3
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5
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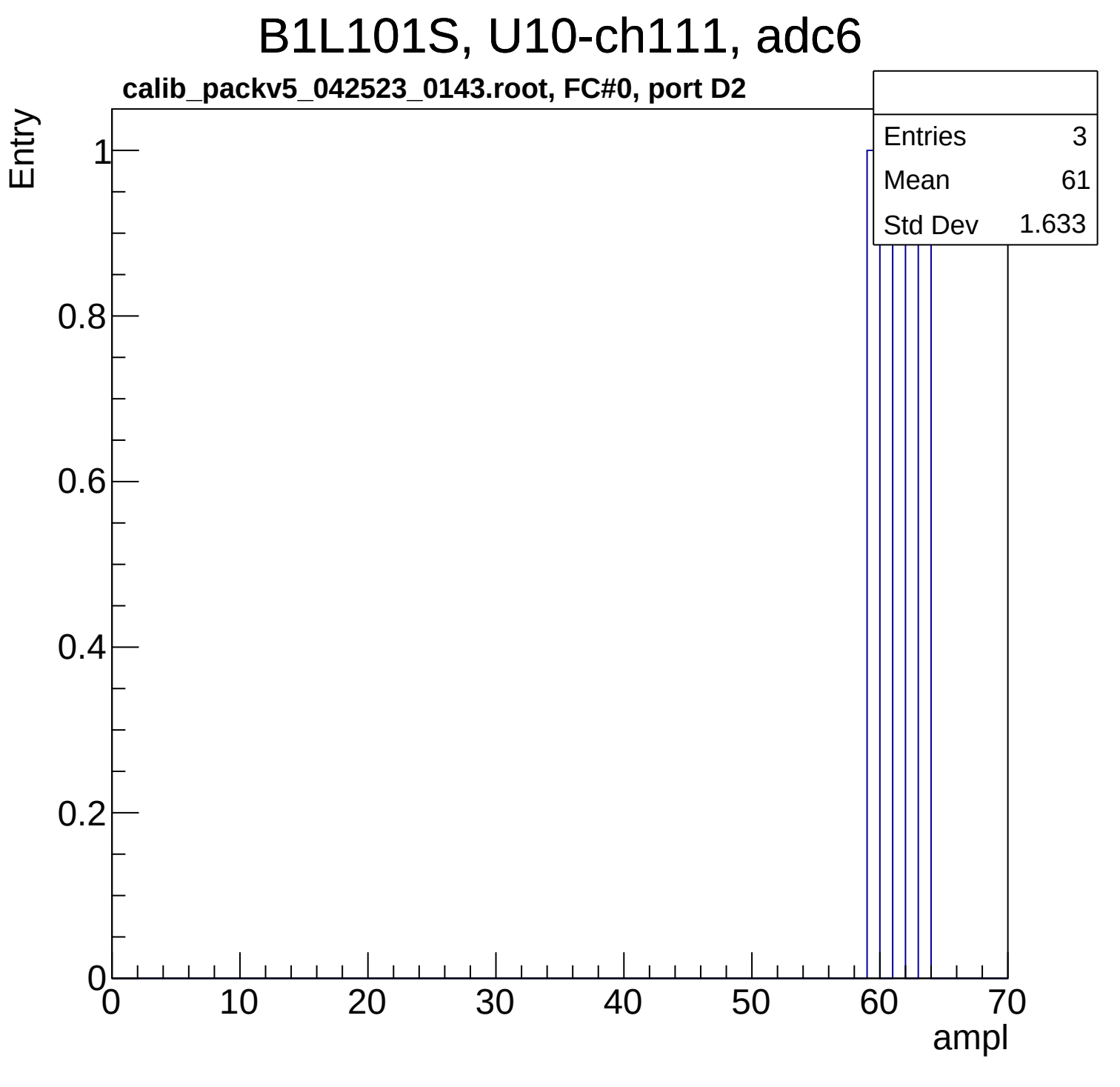
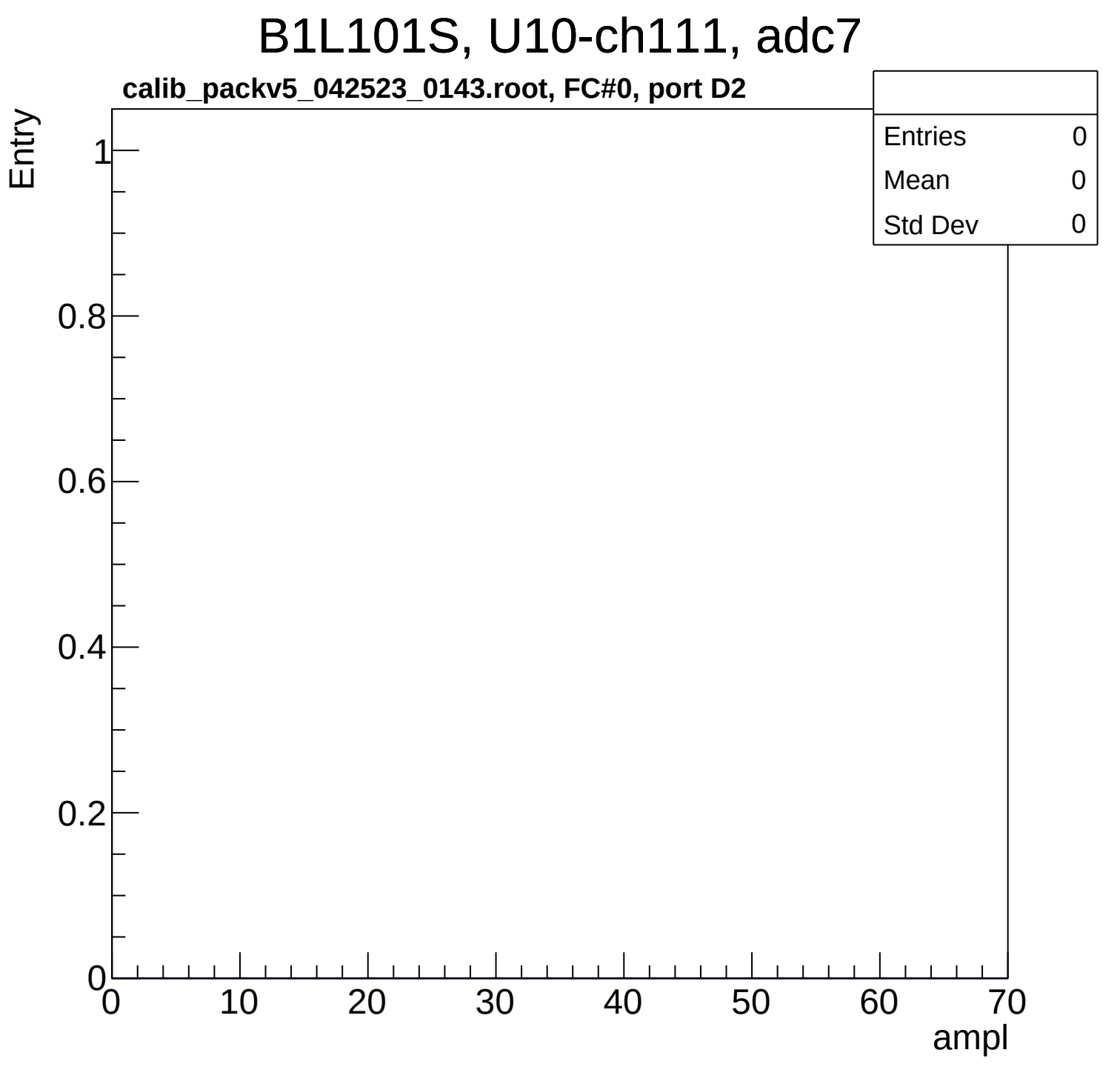

B1L101S, U10-ch111, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 61
Std Dev 1.633
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L101S, U10-ch111, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
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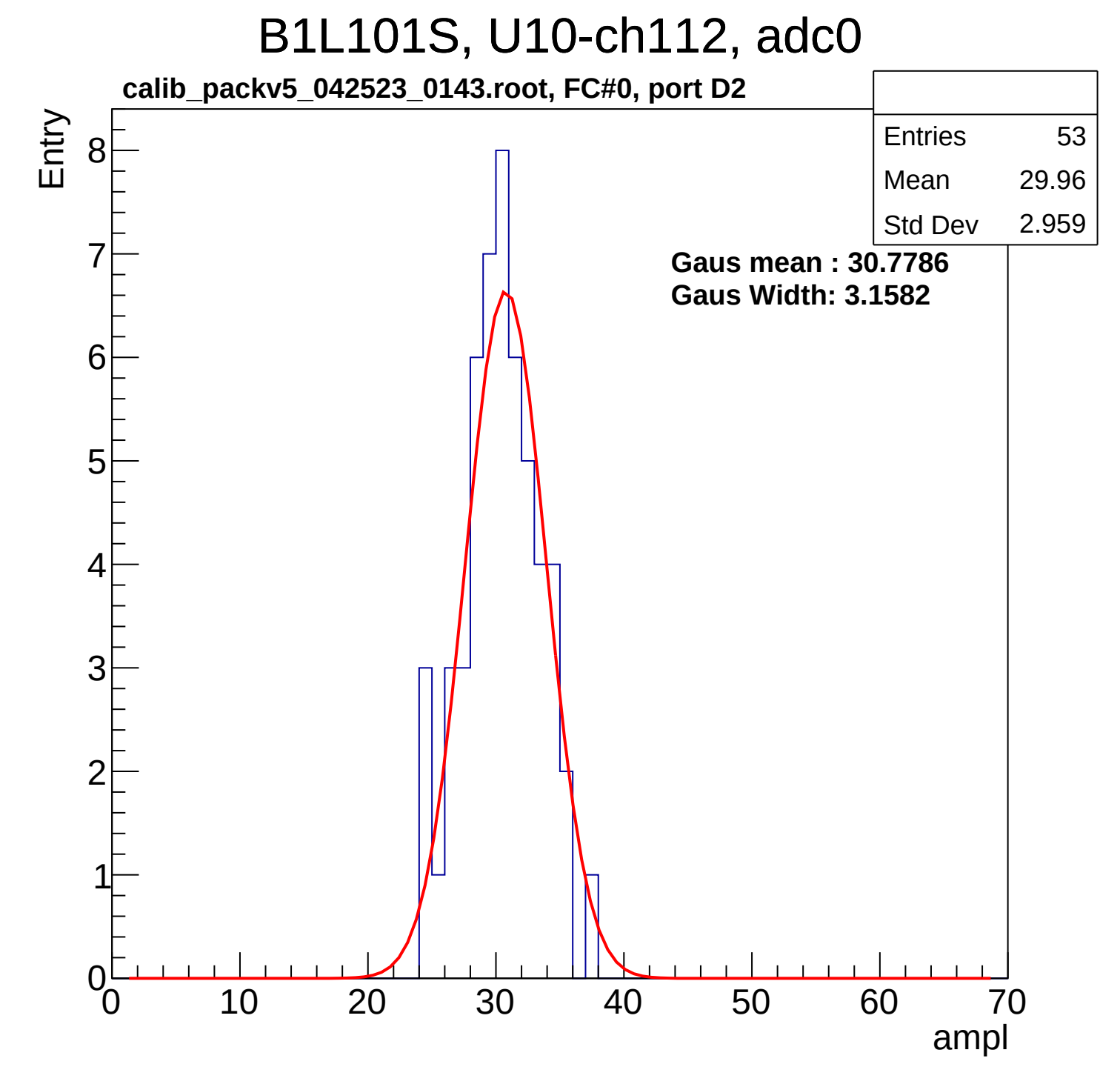
50
60
70
ampl


B1L101S, U10-ch112, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 29.96
Std Dev 2.959
Gaus mean : 30.7786
Gaus Width: 3.1582
Entry
ampl
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1
2
3
4
5
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7
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0
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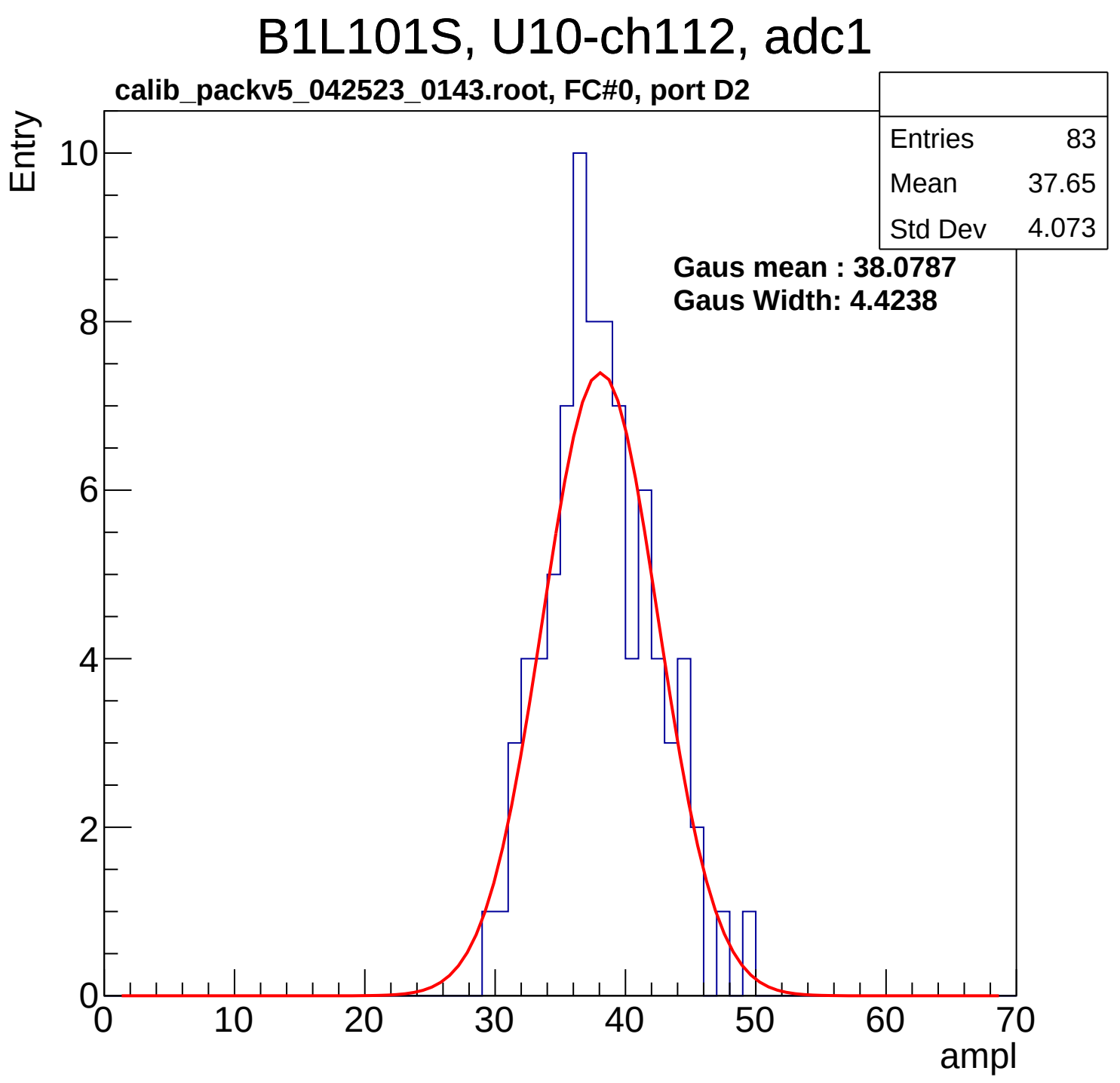
B1L101S, U10-ch112, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 83
Mean 37.65
Std Dev 4.073
Gaus mean : 38.0787
Gaus Width: 4.4238
Entry
ampl
0
2
4
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8
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0
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60
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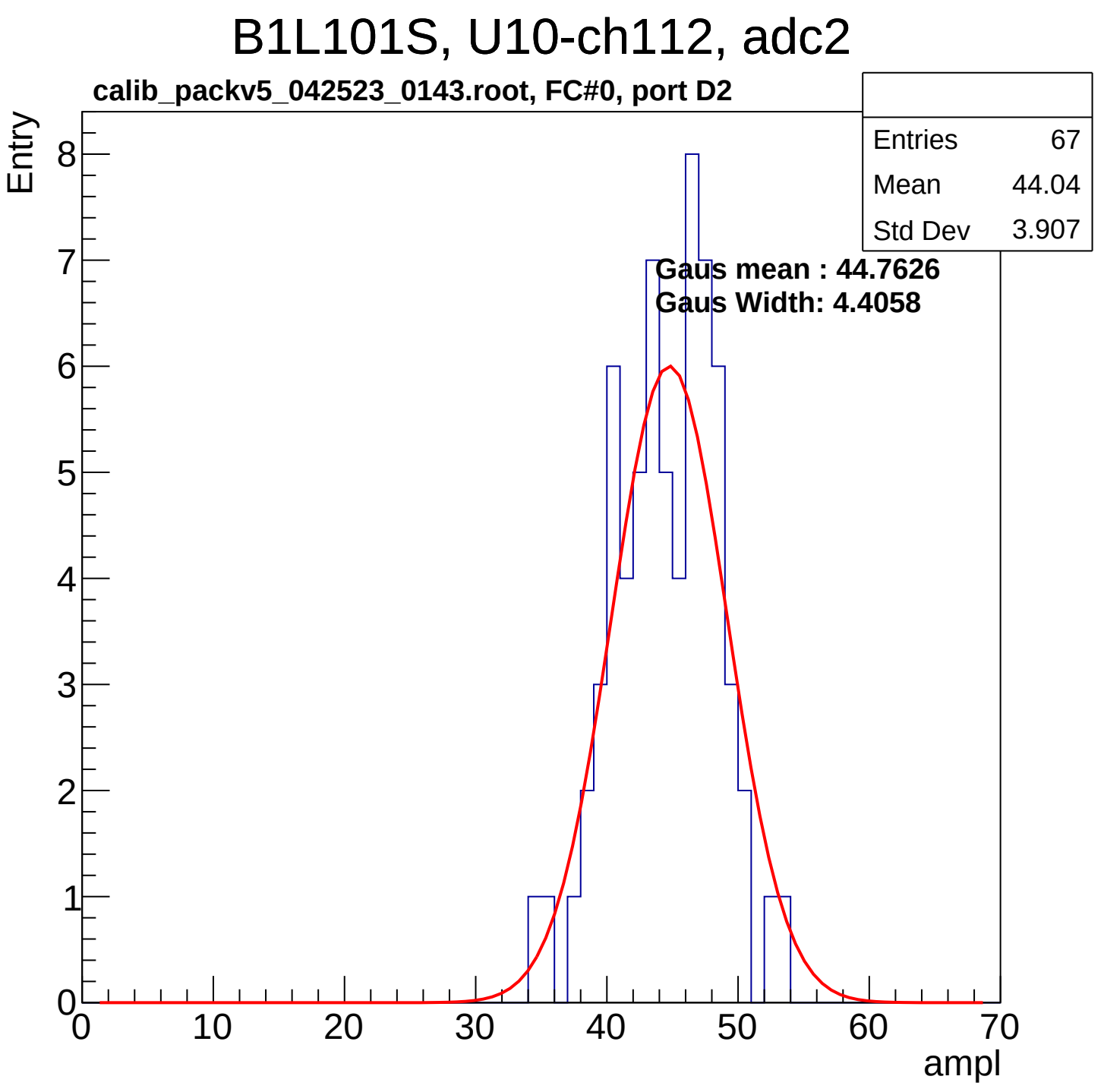
B1L101S, U10-ch112, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 44.04
Std Dev 3.907
Gaus mean : 44.7626
Gaus Width: 4.4058
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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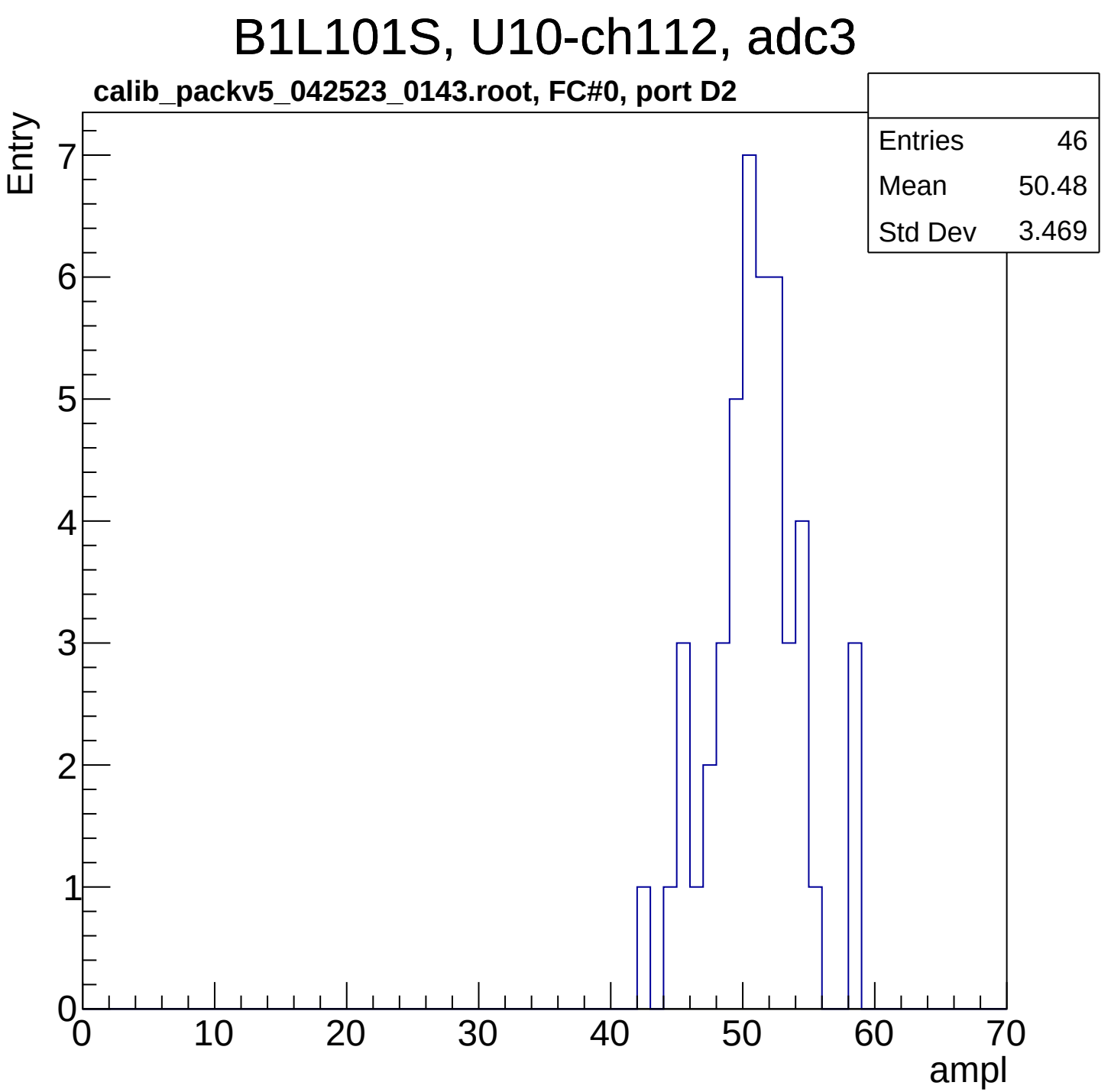
B1L101S, U10-ch112, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 50.48
Std Dev 3.469
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
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60
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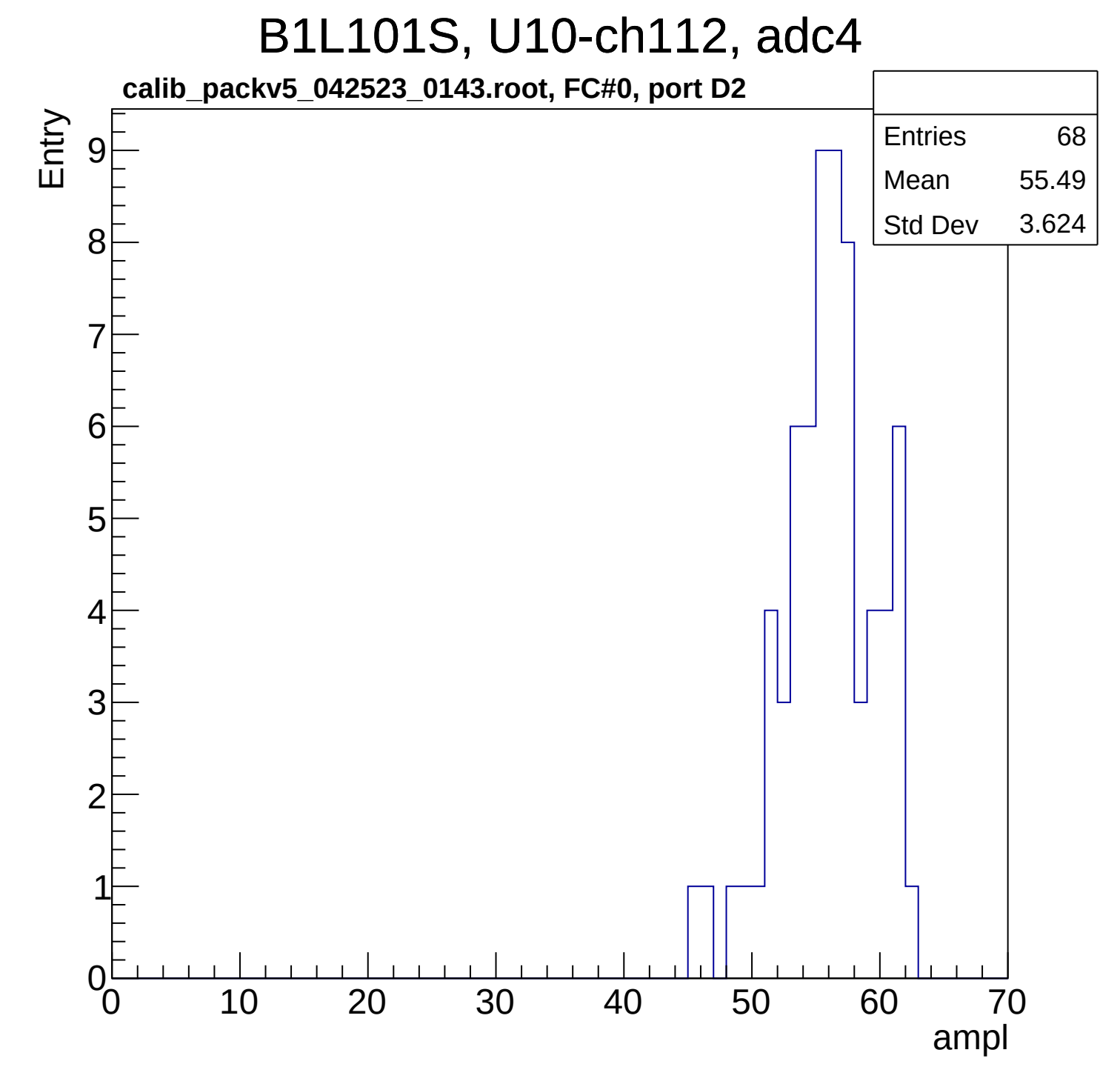
B1L101S, U10-ch112, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 55.49
Std Dev 3.624
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
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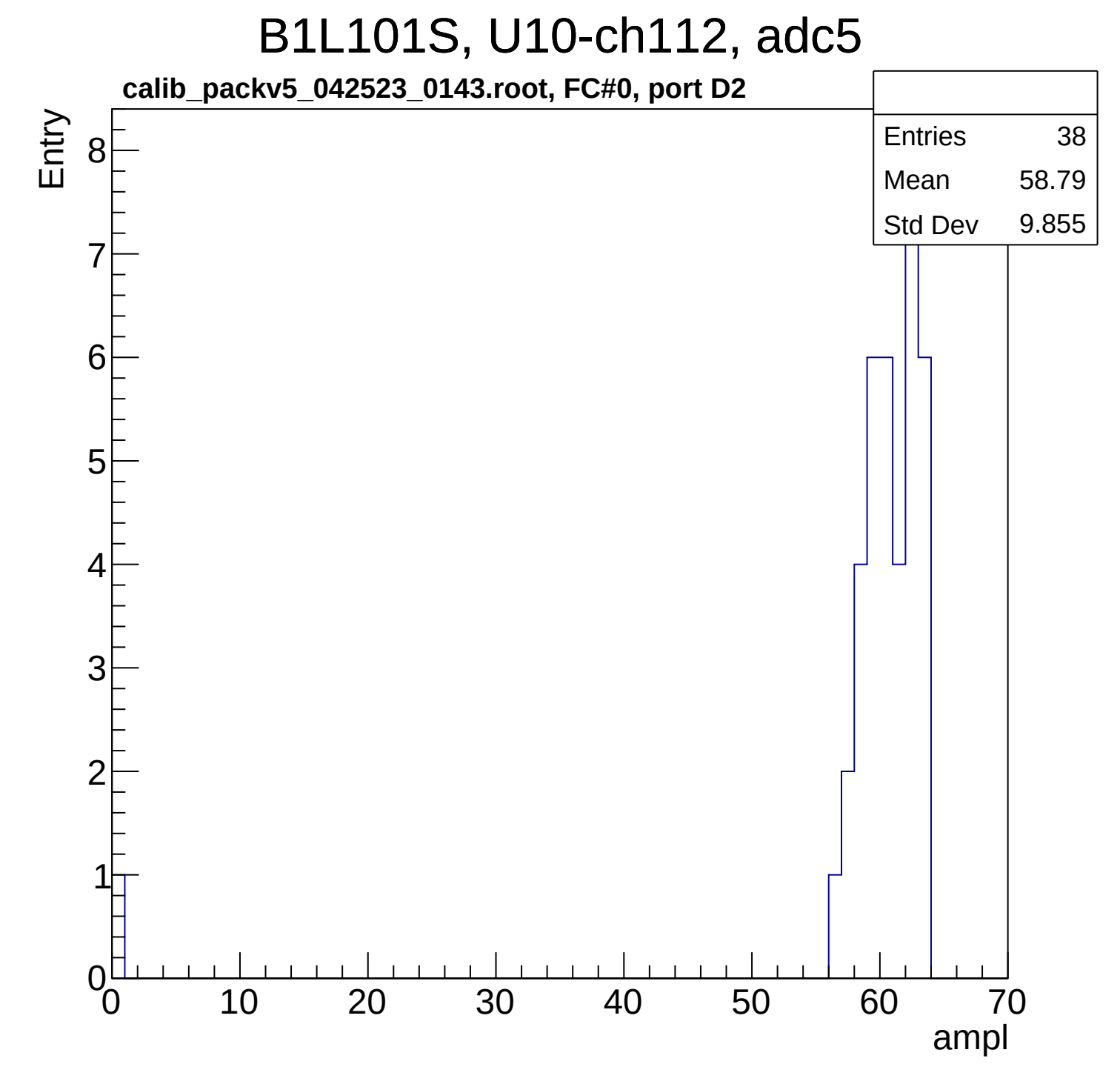
B1L101S, U10-ch112, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 38
Mean 58.79
Std Dev 9.855
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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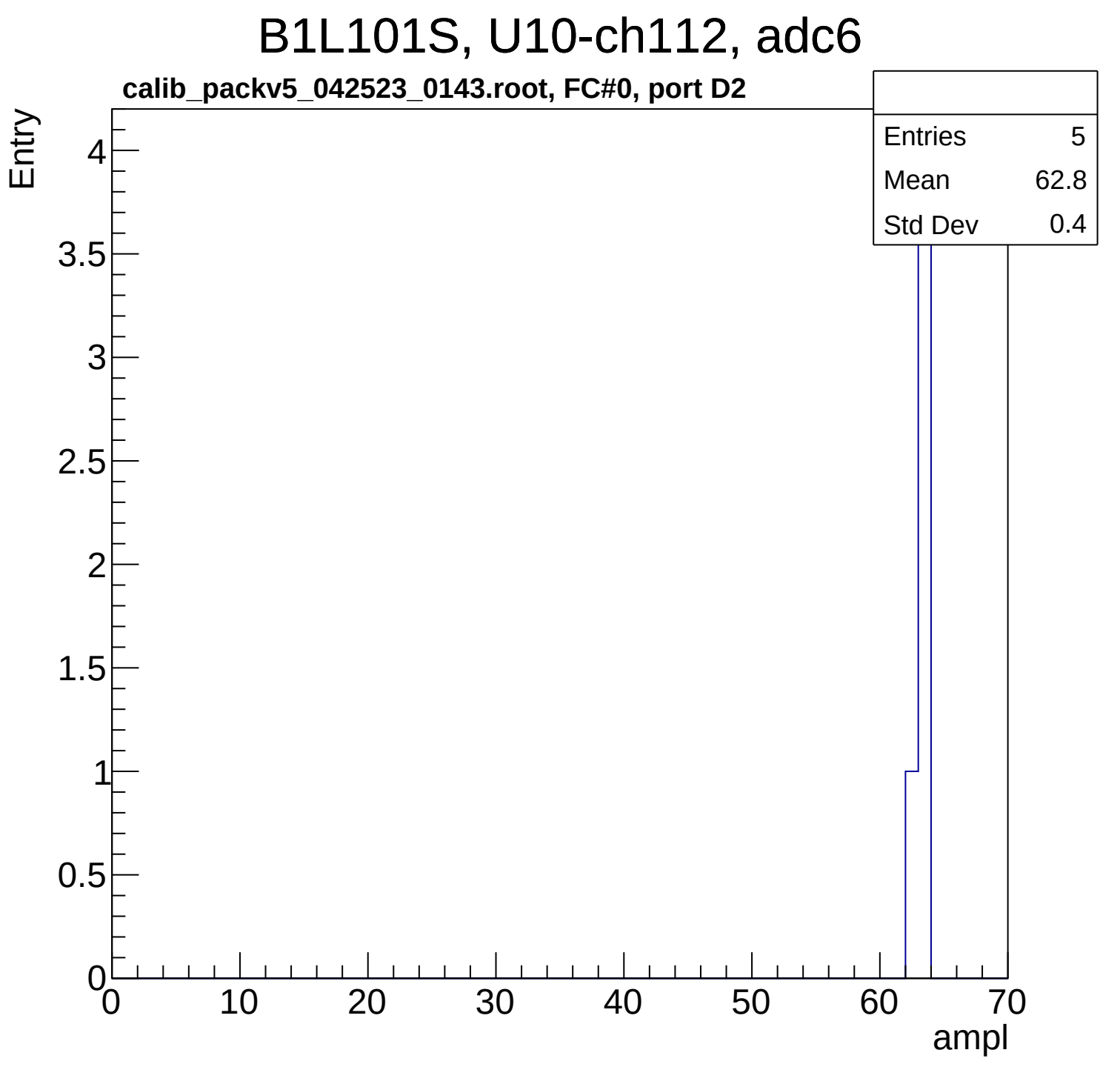
B1L101S, U10-ch112, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 62.8
Std Dev 0.4
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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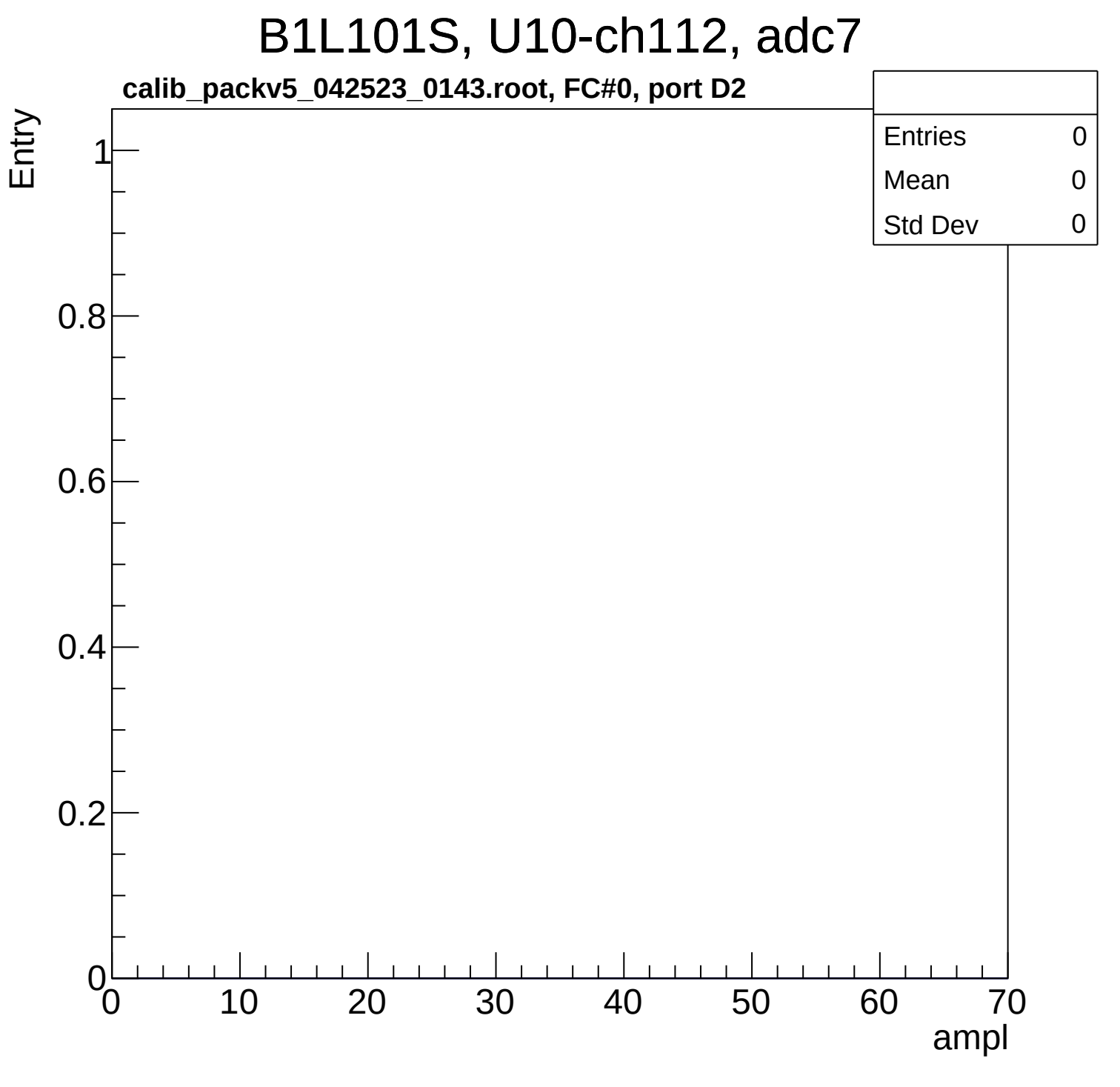
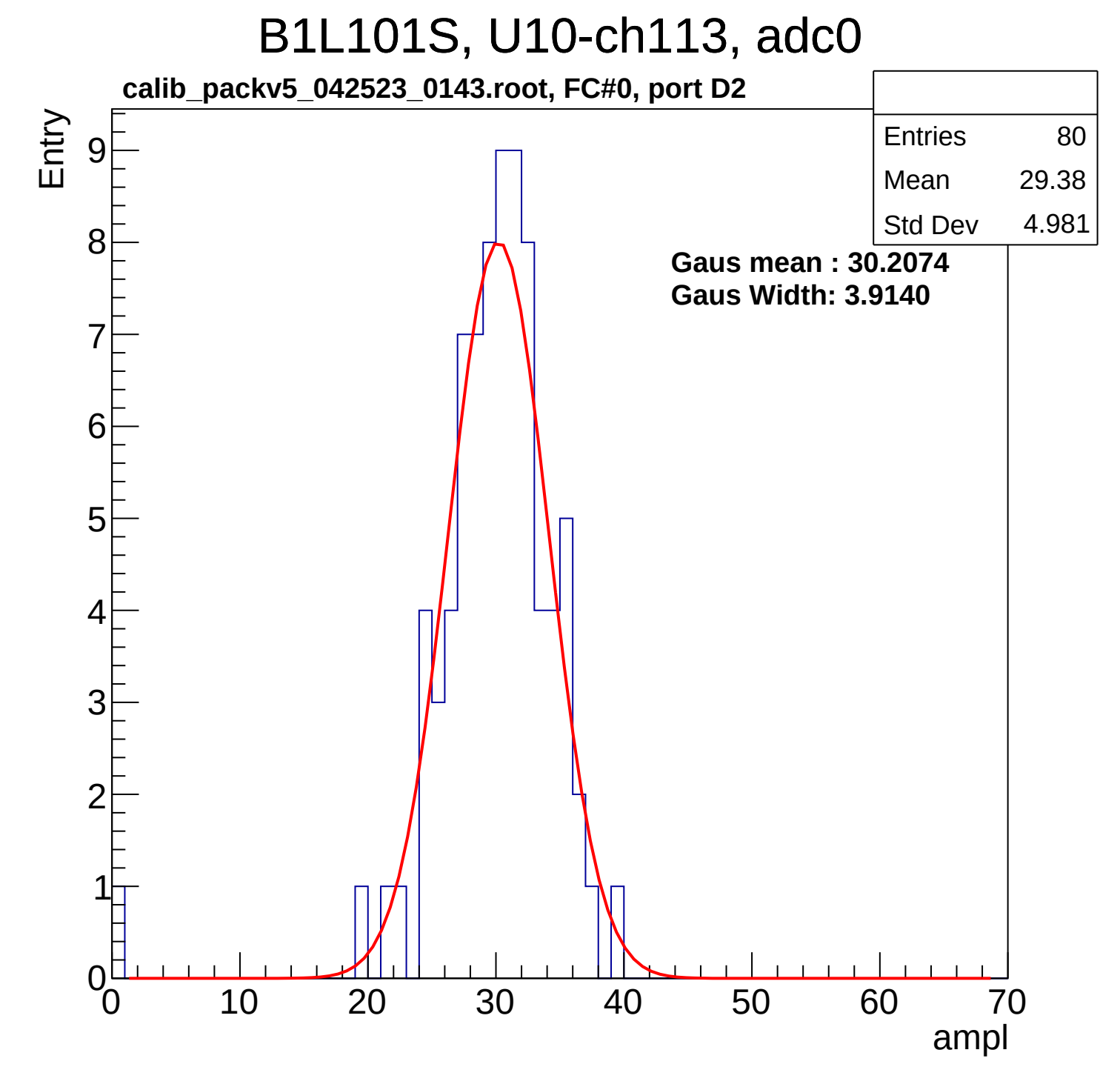
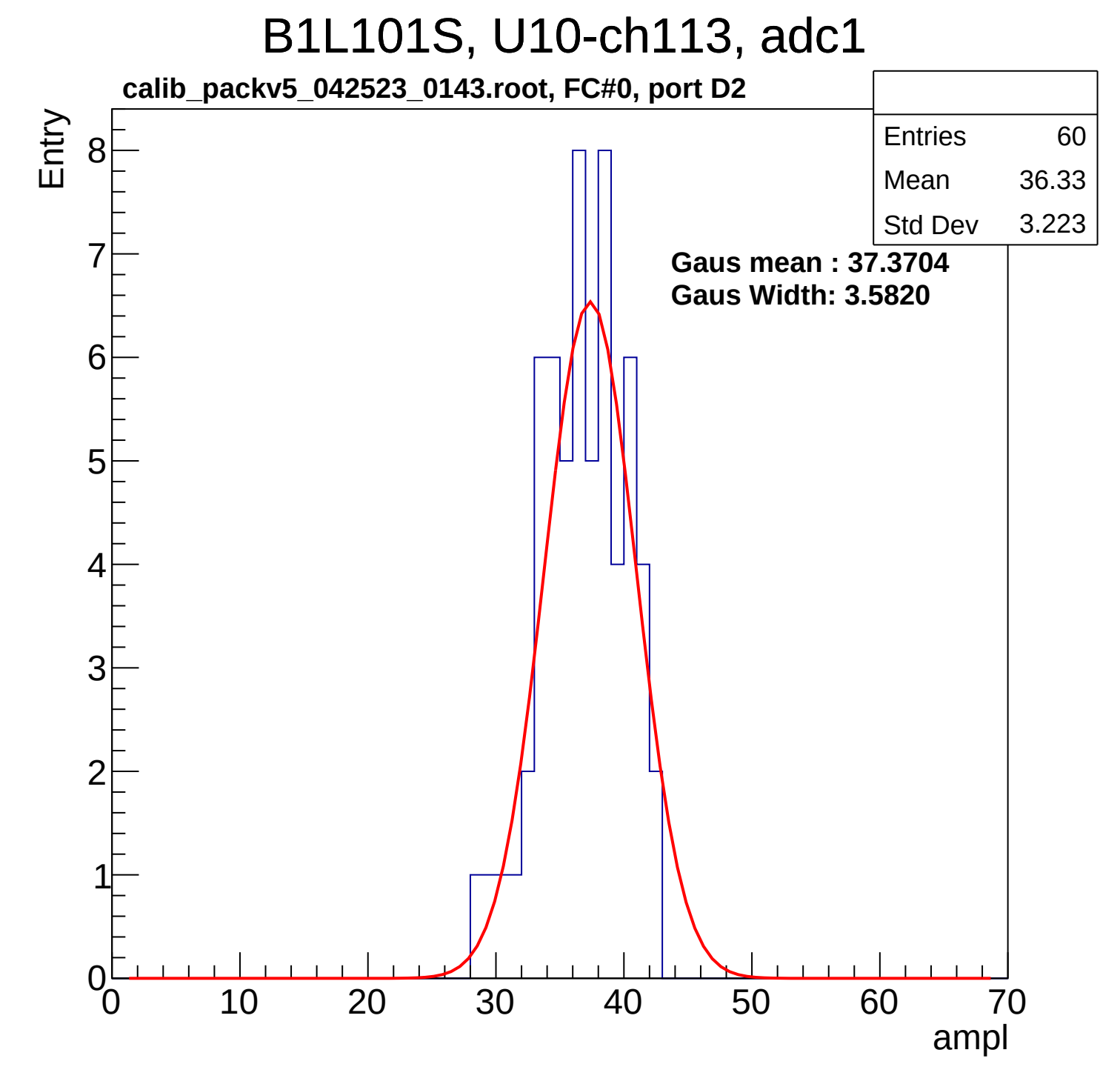

B1L101S, U10-ch112, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch113, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 80
Mean 29.38
Std Dev 4.981
Gaus mean : 30.2074
Gaus Width: 3.9140
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch113, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 36.33
Std Dev 3.223
Gaus mean : 37.3704
Gaus Width: 3.5820
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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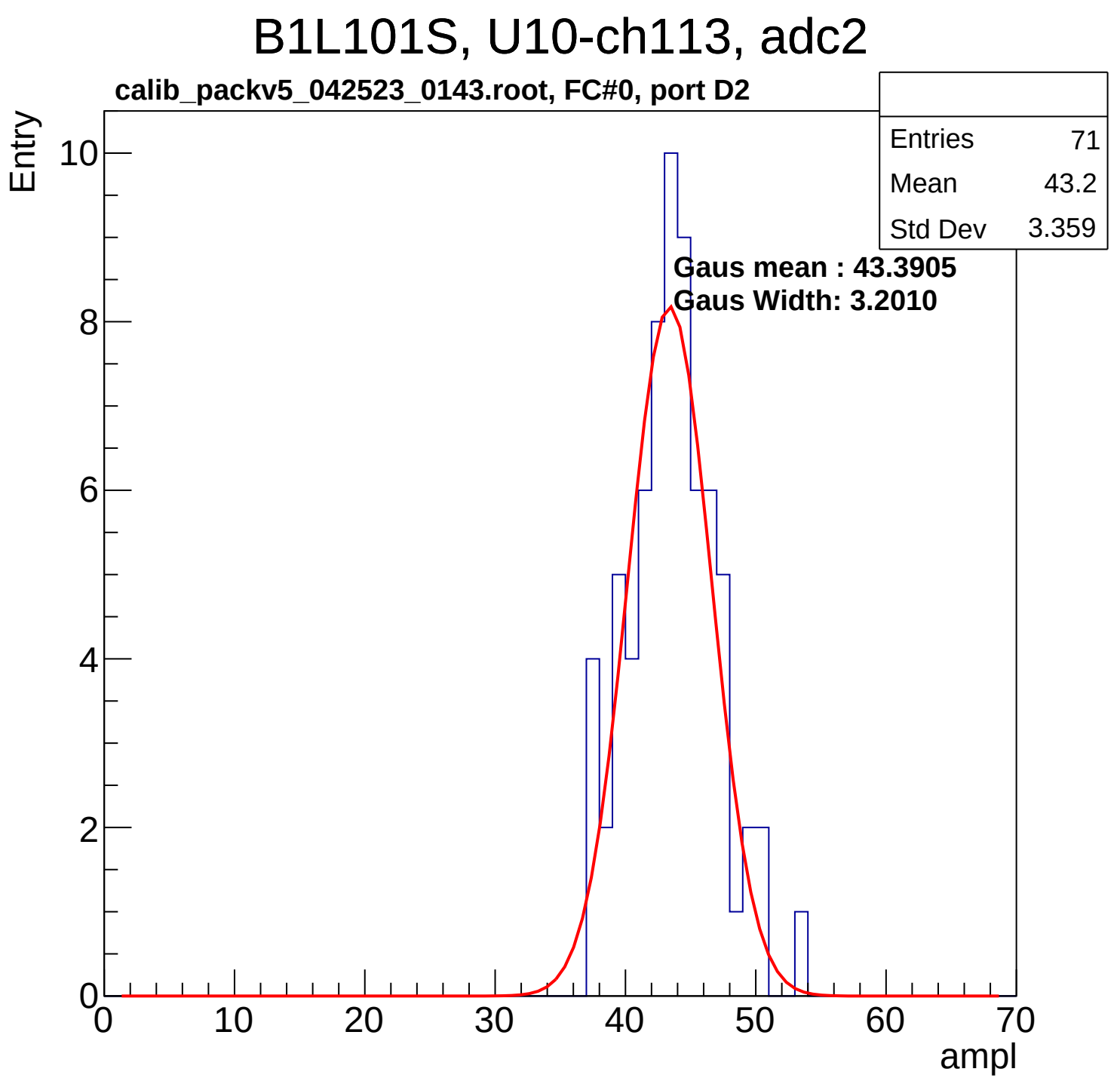
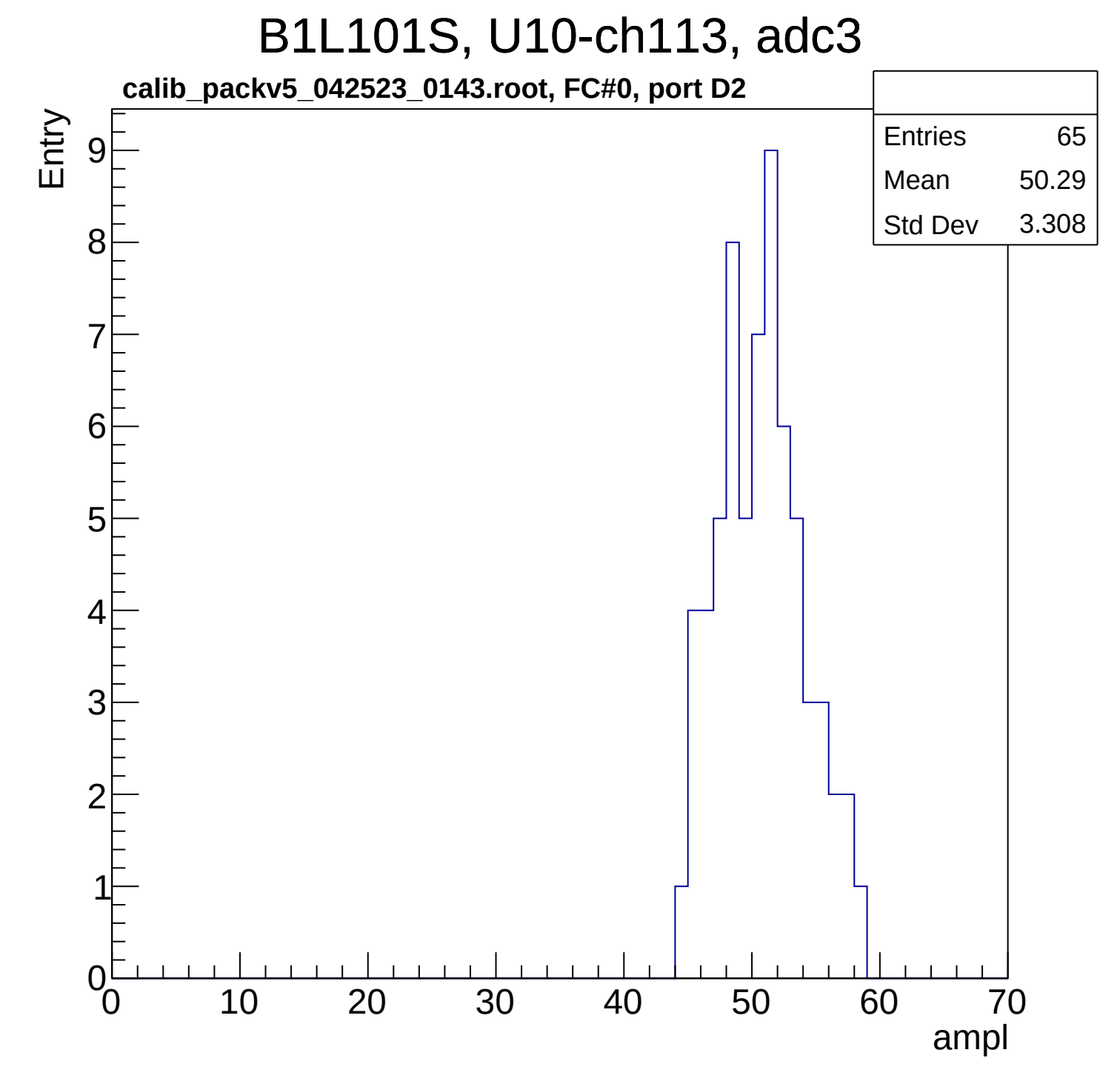

B1L101S, U10-ch113, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 43.2
Std Dev 3.359
Gaus mean : 43.3905
Gaus Width: 3.2010
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch113, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 50.29
Std Dev 3.308
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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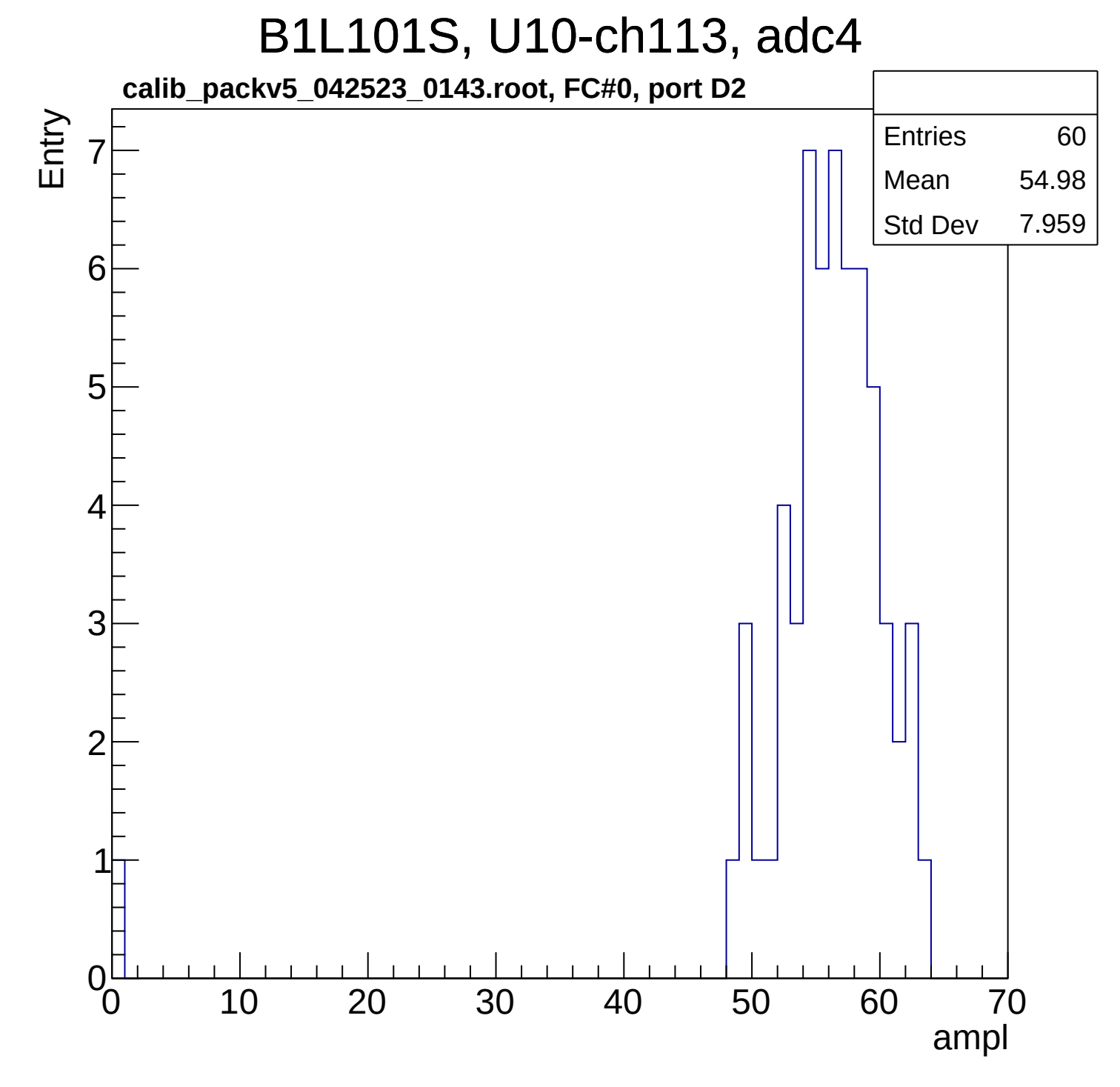
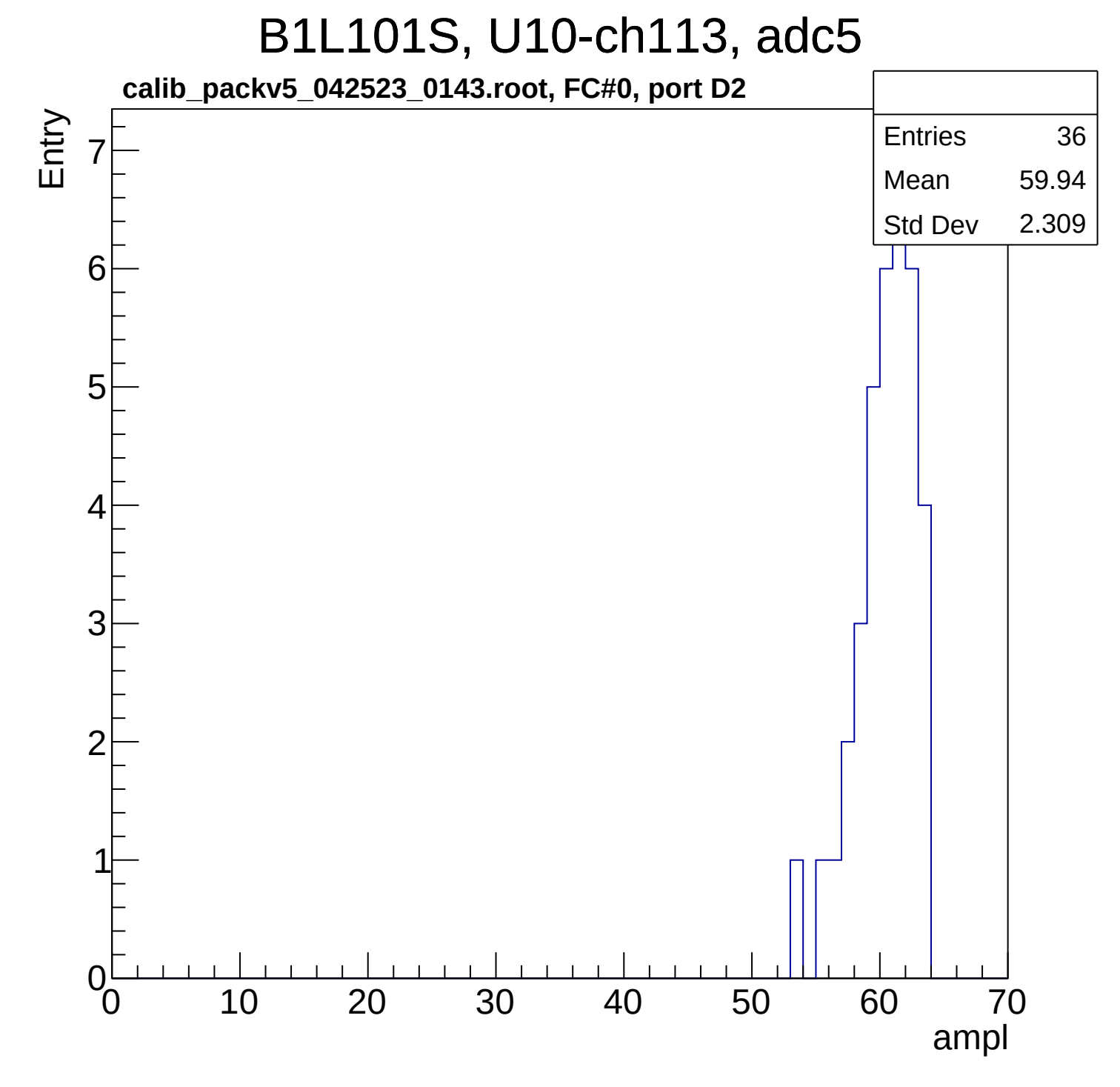
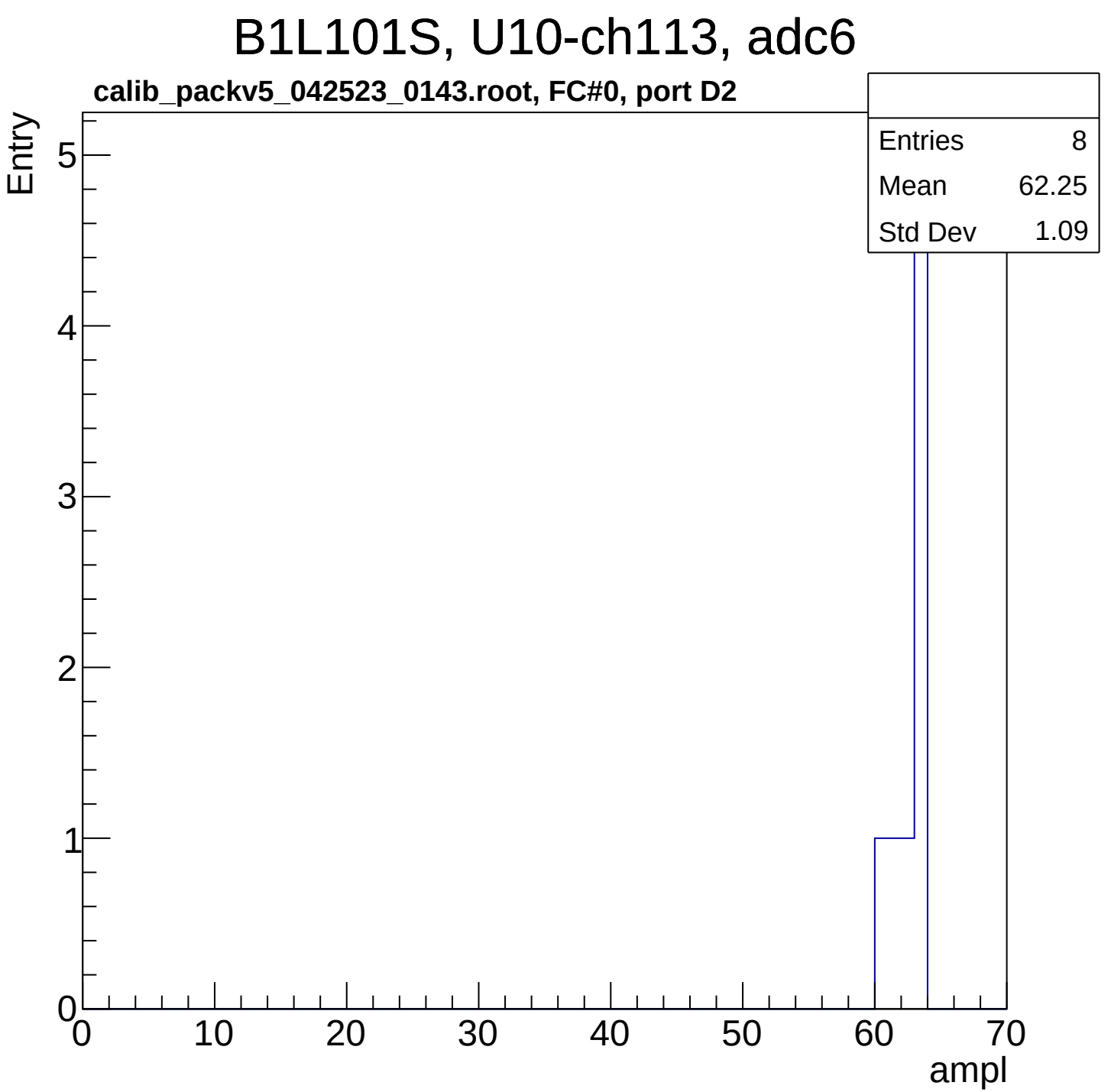
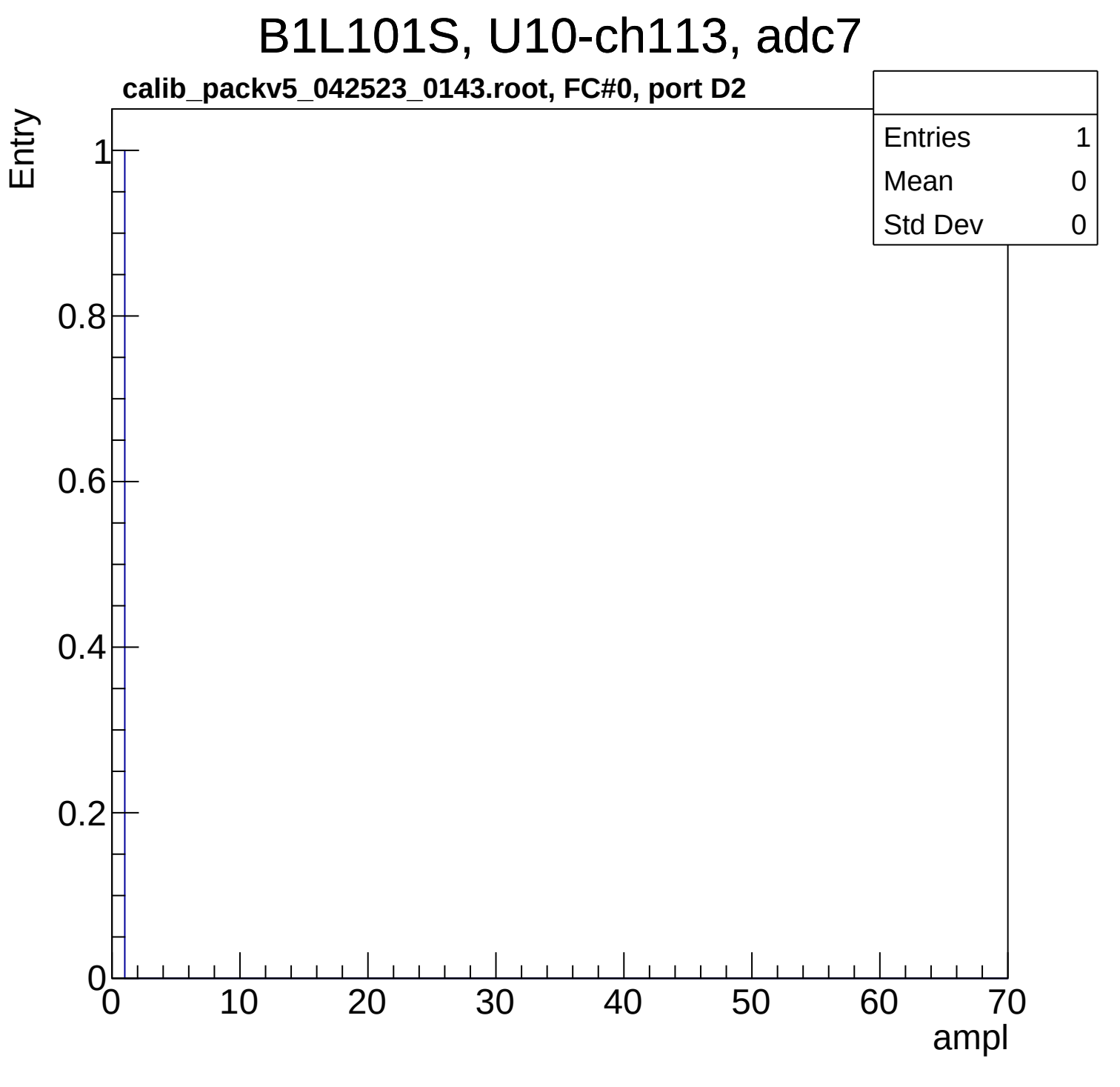
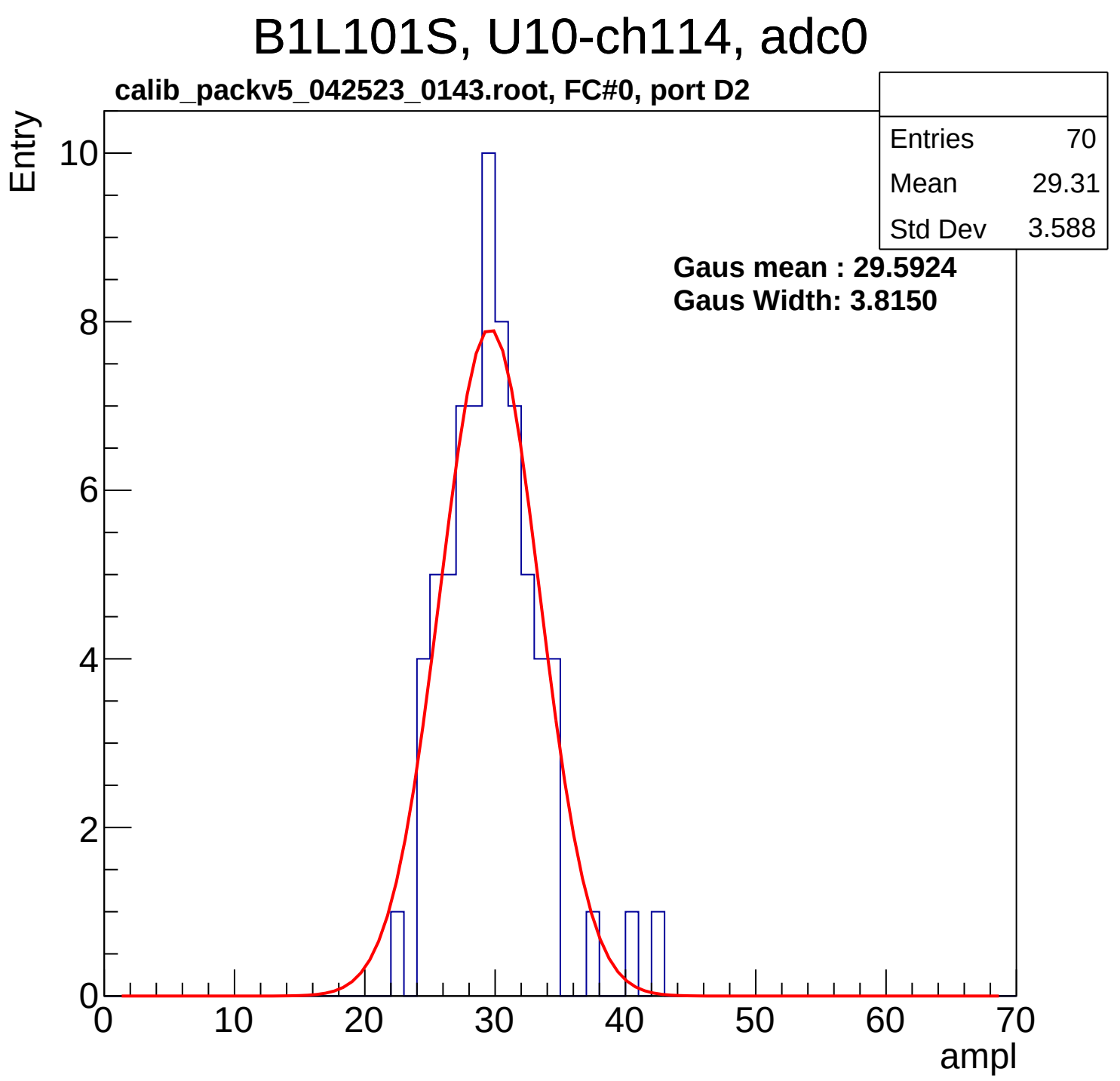
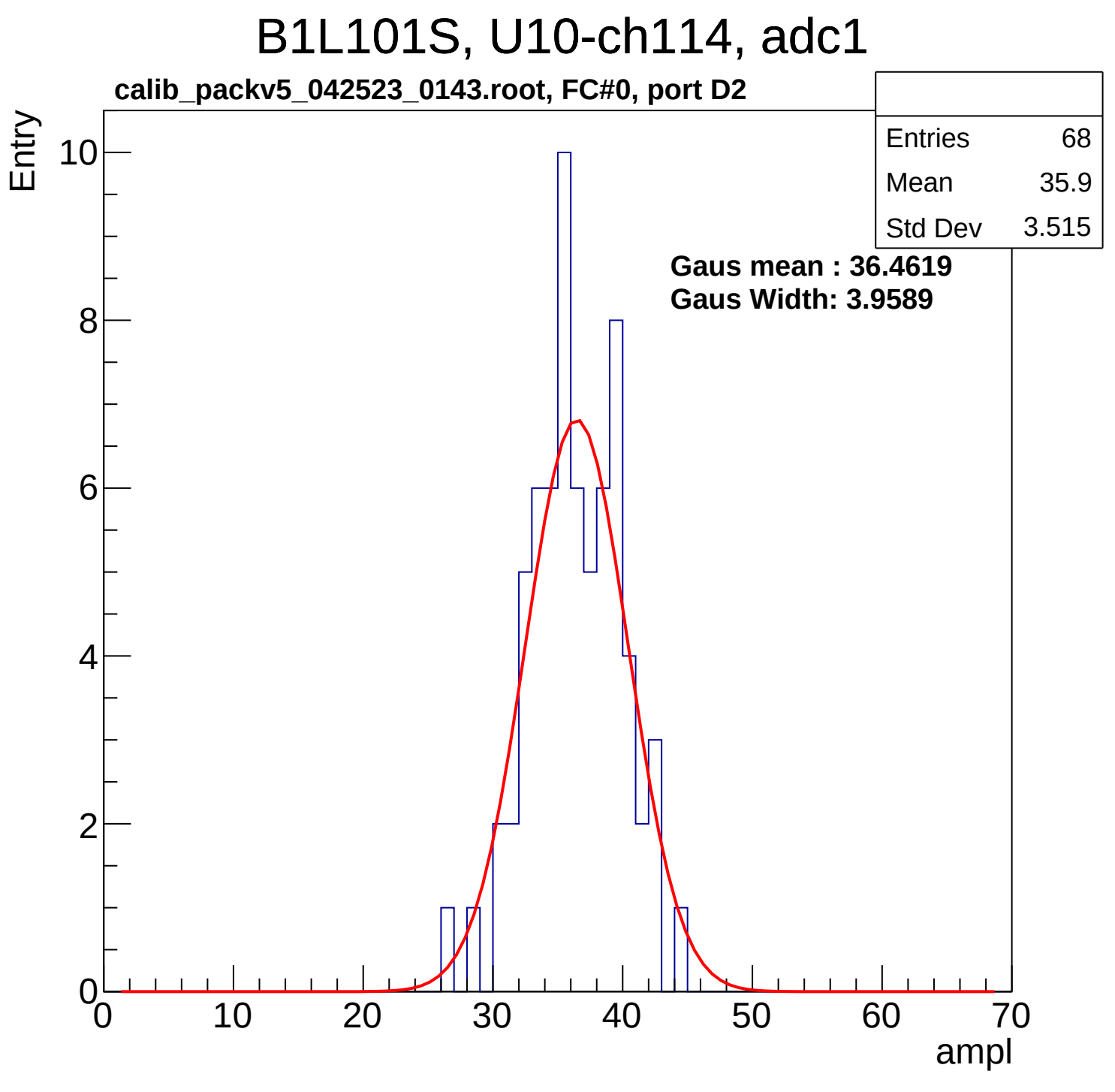

B1L101S, U10-ch113, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 54.98
Std Dev 7.959
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U10-ch113, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 36
Mean 59.94
Std Dev 2.309
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U10-ch113, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 62.25
Std Dev 1.09
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch113, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch114, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 29.31
Std Dev 3.588
Gaus mean : 29.5924
Gaus Width: 3.8150
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch114, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 35.9
Std Dev 3.515
Gaus mean : 36.4619
Gaus Width: 3.9589
Entry
ampl
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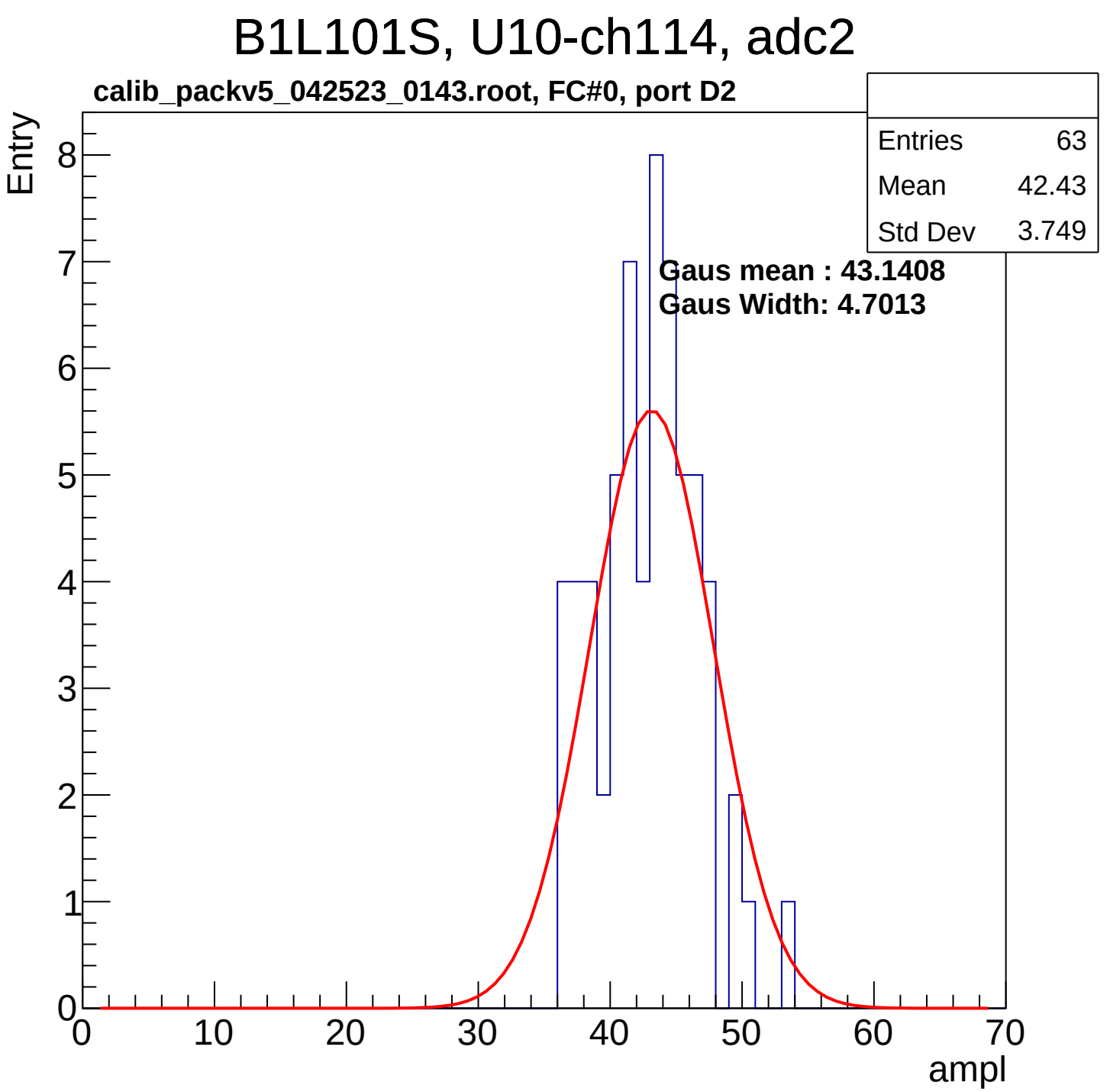
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch114, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 42.43
Std Dev 3.749
Gaus mean : 43.1408
Gaus Width: 4.7013
Entry
ampl
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1
2
3
4
5
6
7
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0
10
20
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40
50
60
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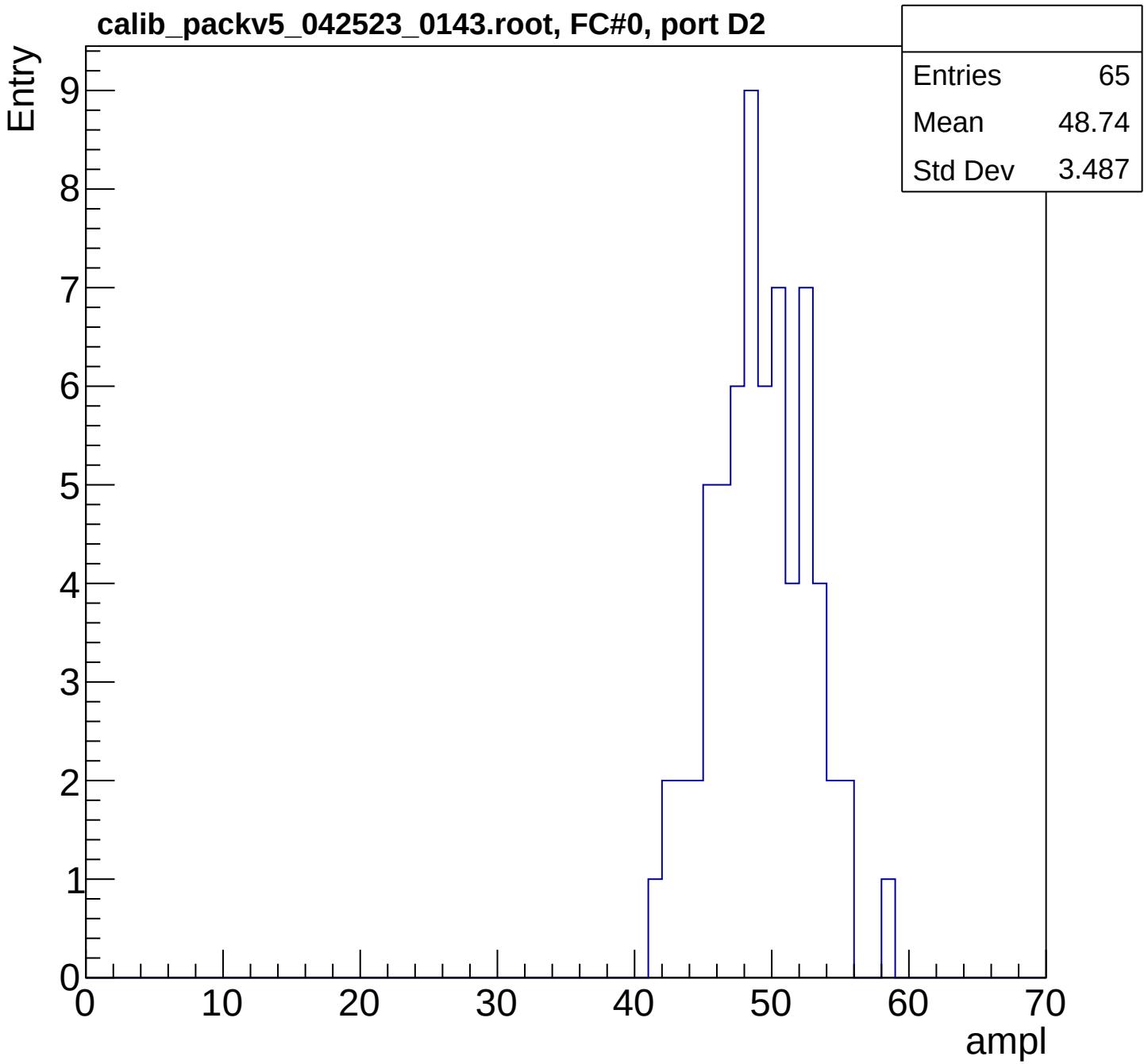
B1L101S, U10-ch114, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 48.74
Std Dev 3.487
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
50
60
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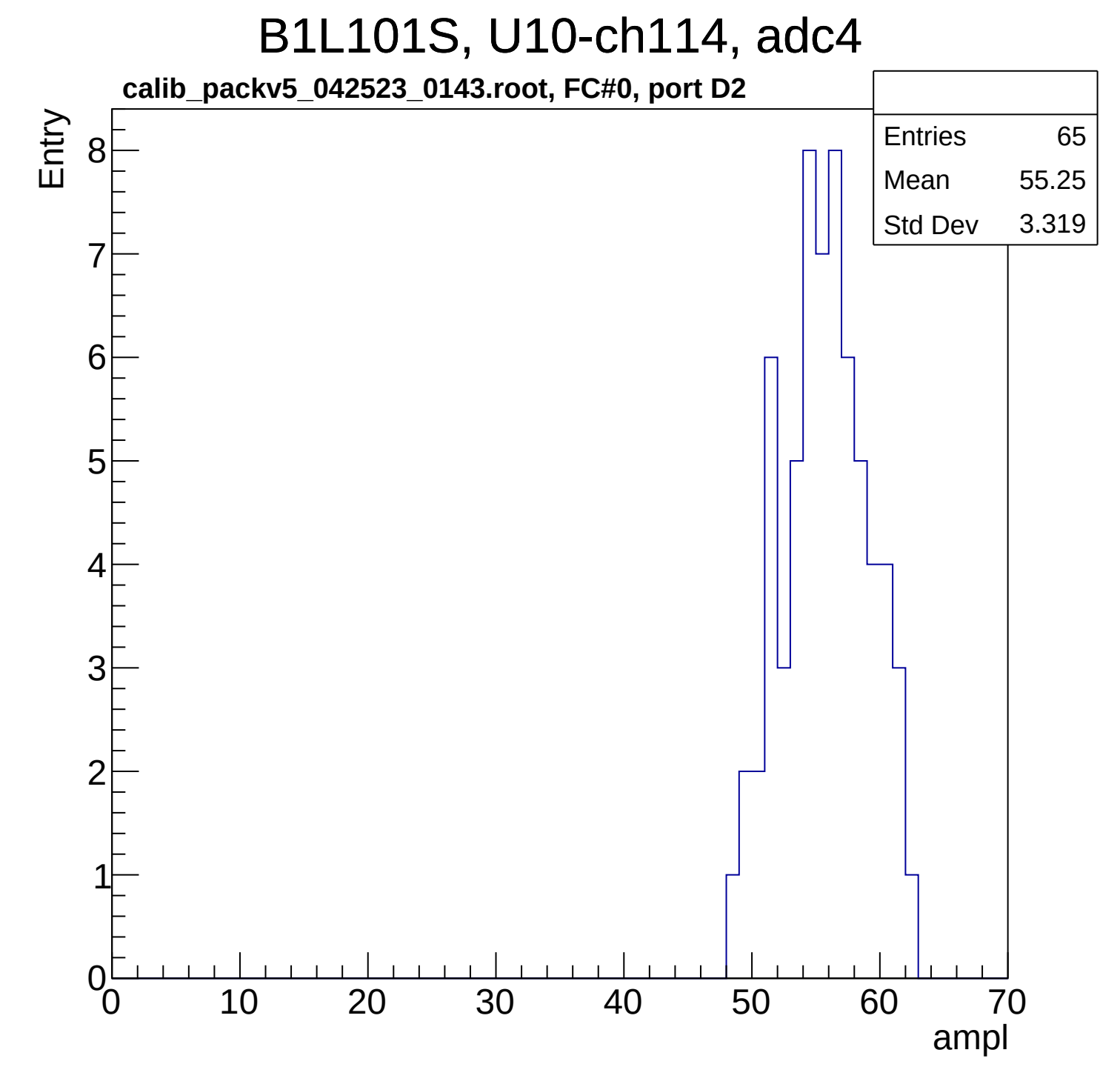
B1L101S, U10-ch114, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 55.25
Std Dev 3.319
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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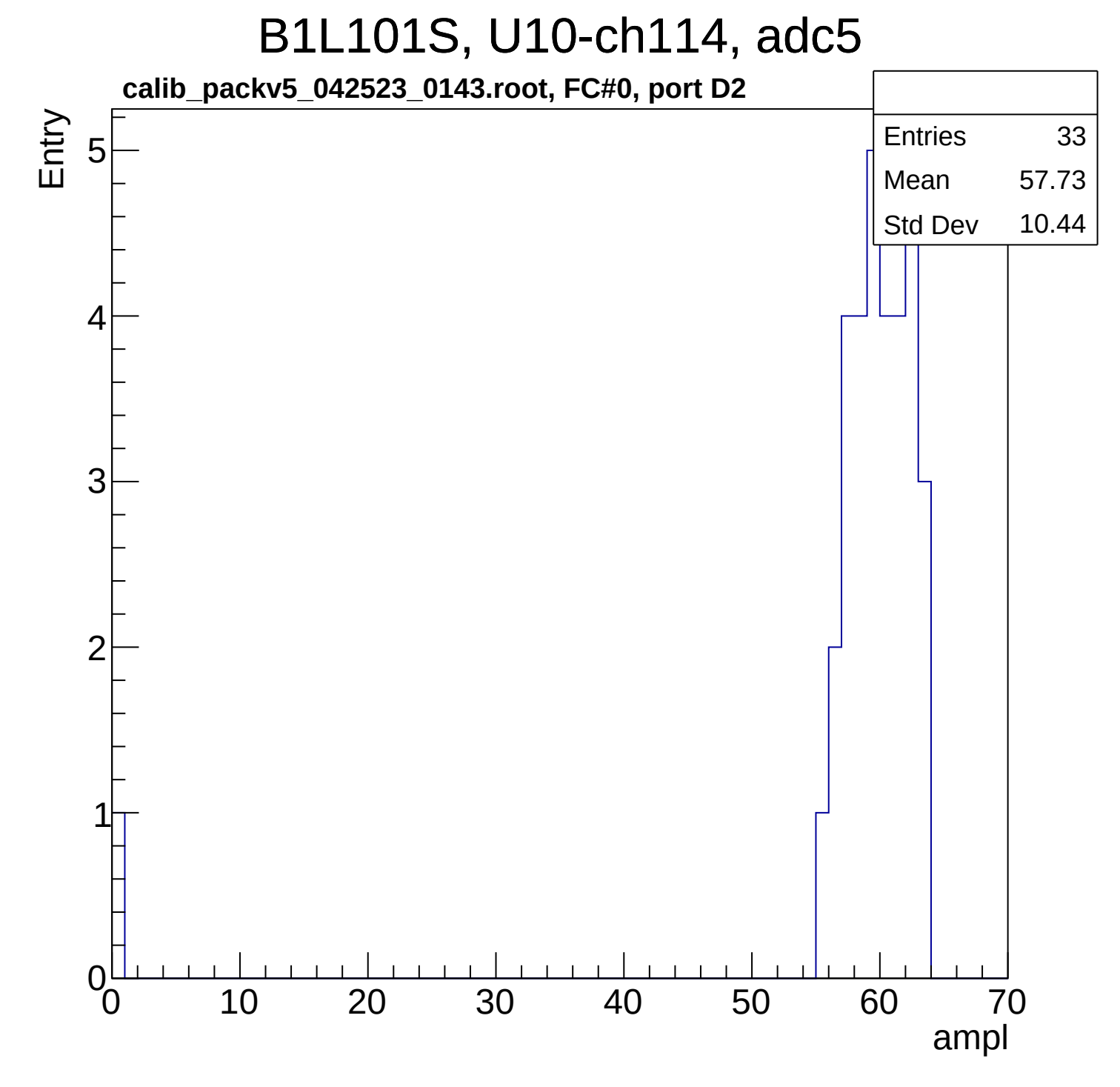
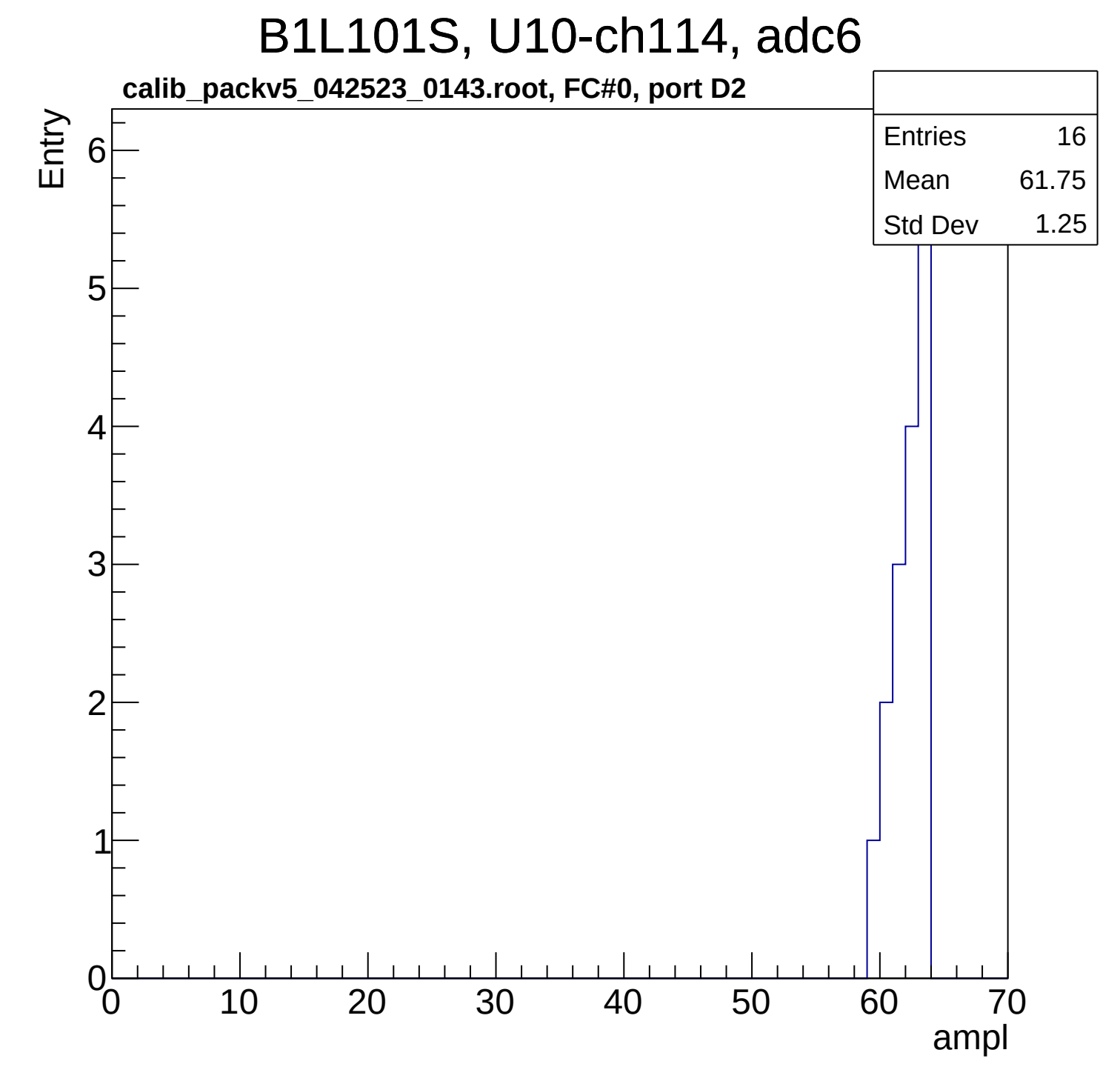

B1L101S, U10-ch114, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 33
Mean 57.73
Std Dev 10.44
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch114, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 16
Mean 61.75
Std Dev 1.25
Entry
ampl
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0
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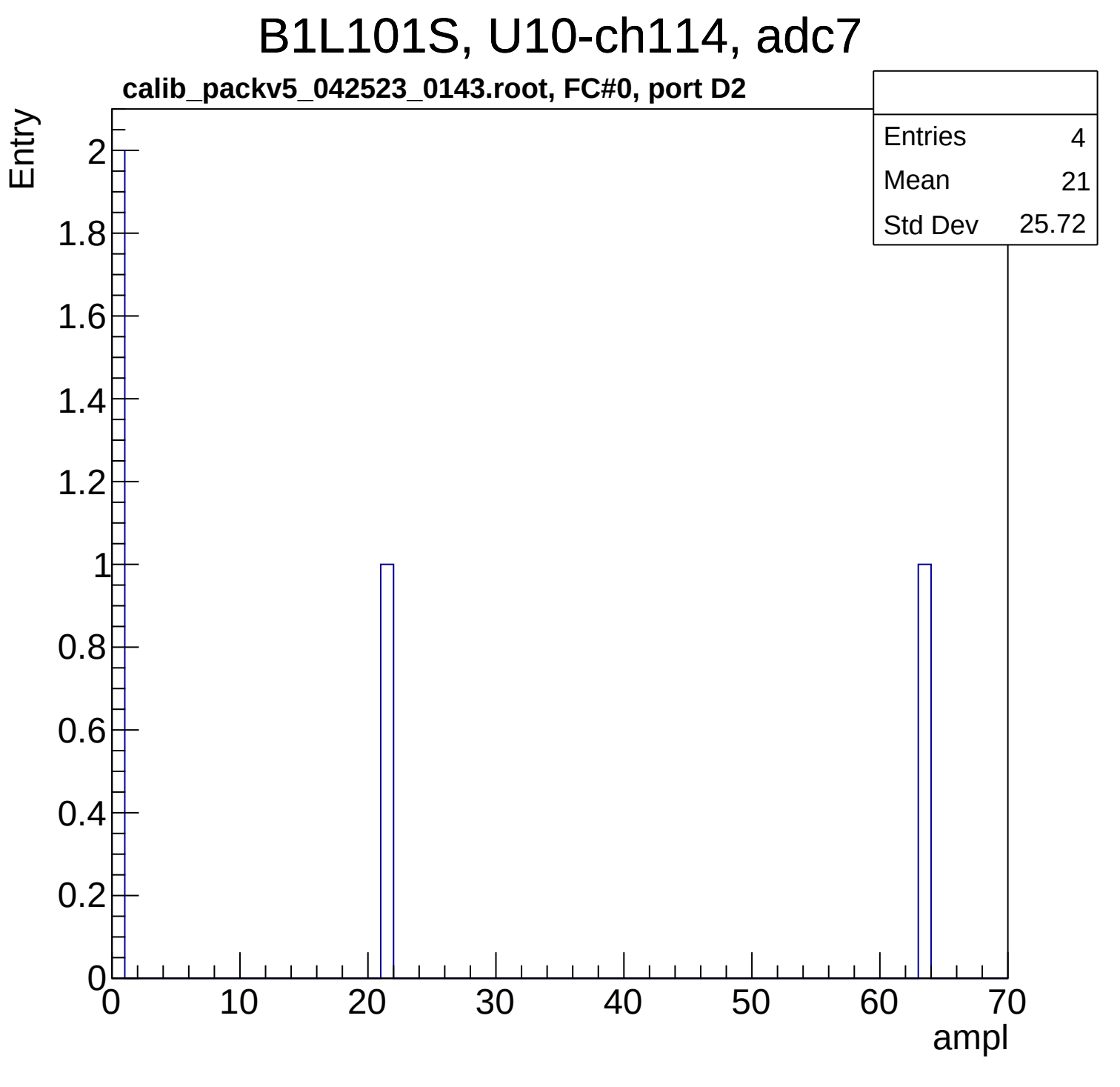
40
50
60
70


B1L101S, U10-ch114, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 21
Std Dev 25.72
Entry
ampl
0
0.2
0.4
0.6
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1.2
1.4
1.6
1.8
2
0
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40
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60
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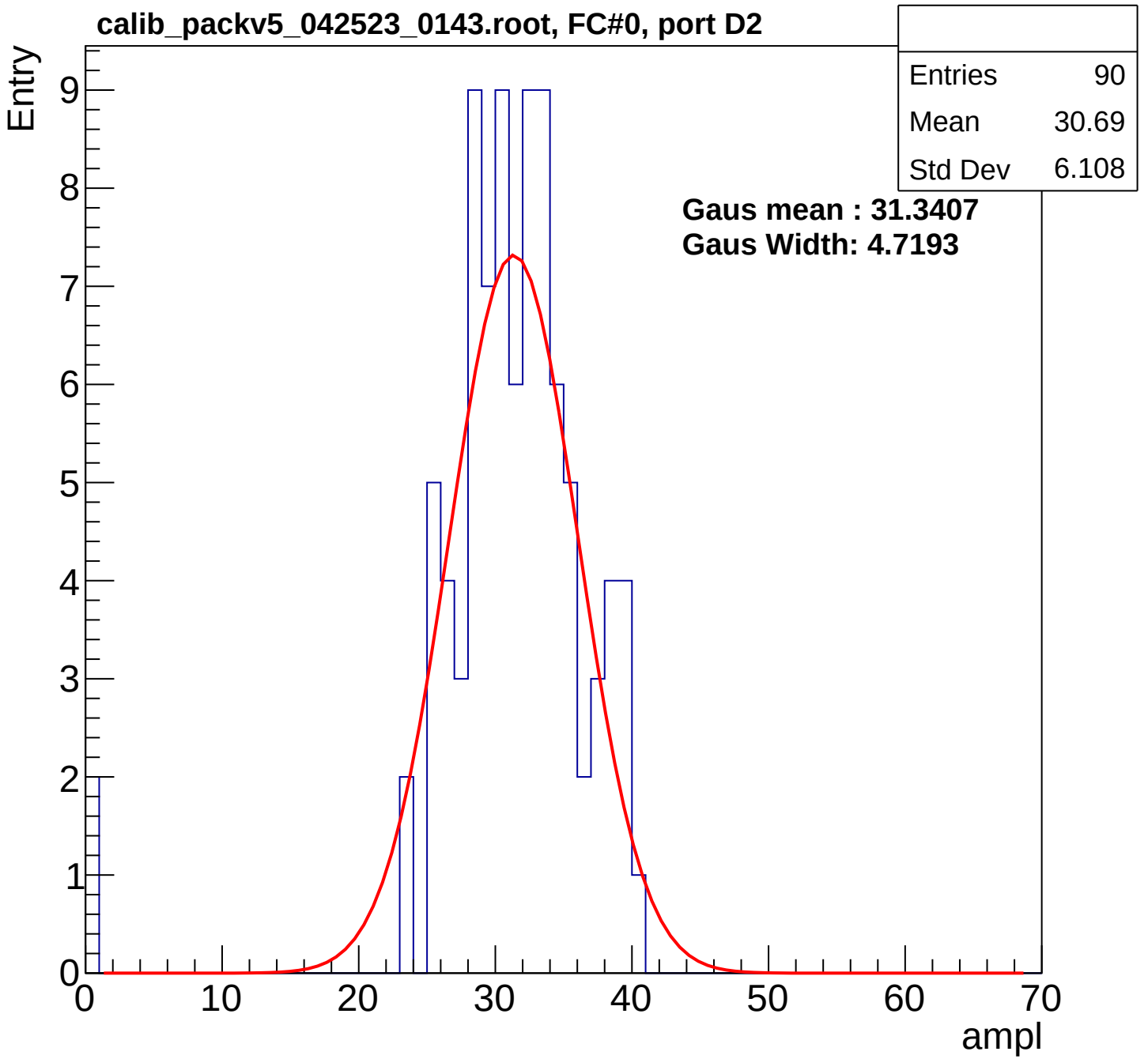
B1L101S, U10-ch115, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 90
Mean 30.69
Std Dev 6.108
Gaus mean : 31.3407
Gaus Width: 4.7193
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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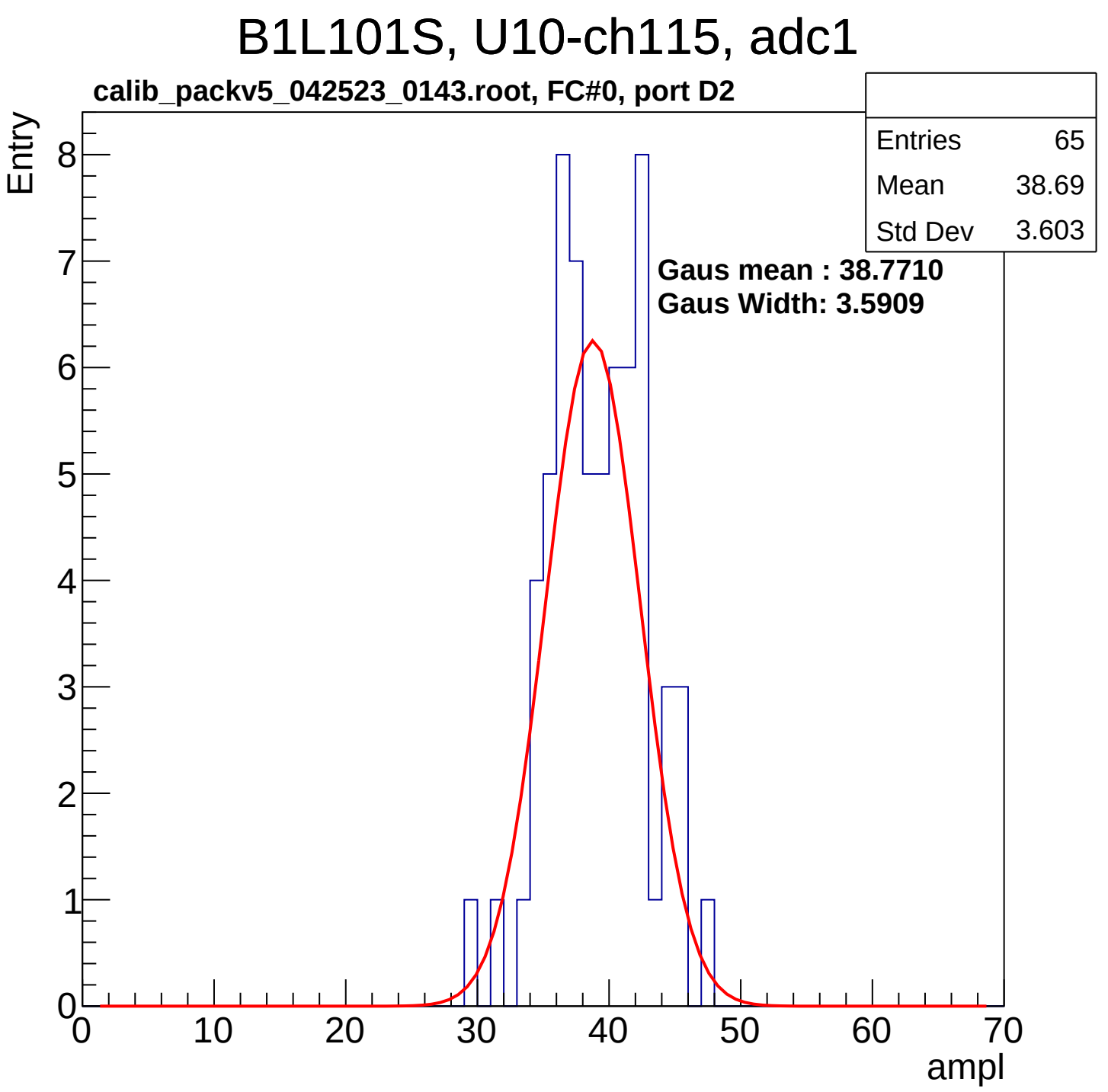
B1L101S, U10-ch115, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 38.69
Std Dev 3.603
Gaus mean : 38.7710
Gaus Width: 3.5909
Entry
ampl
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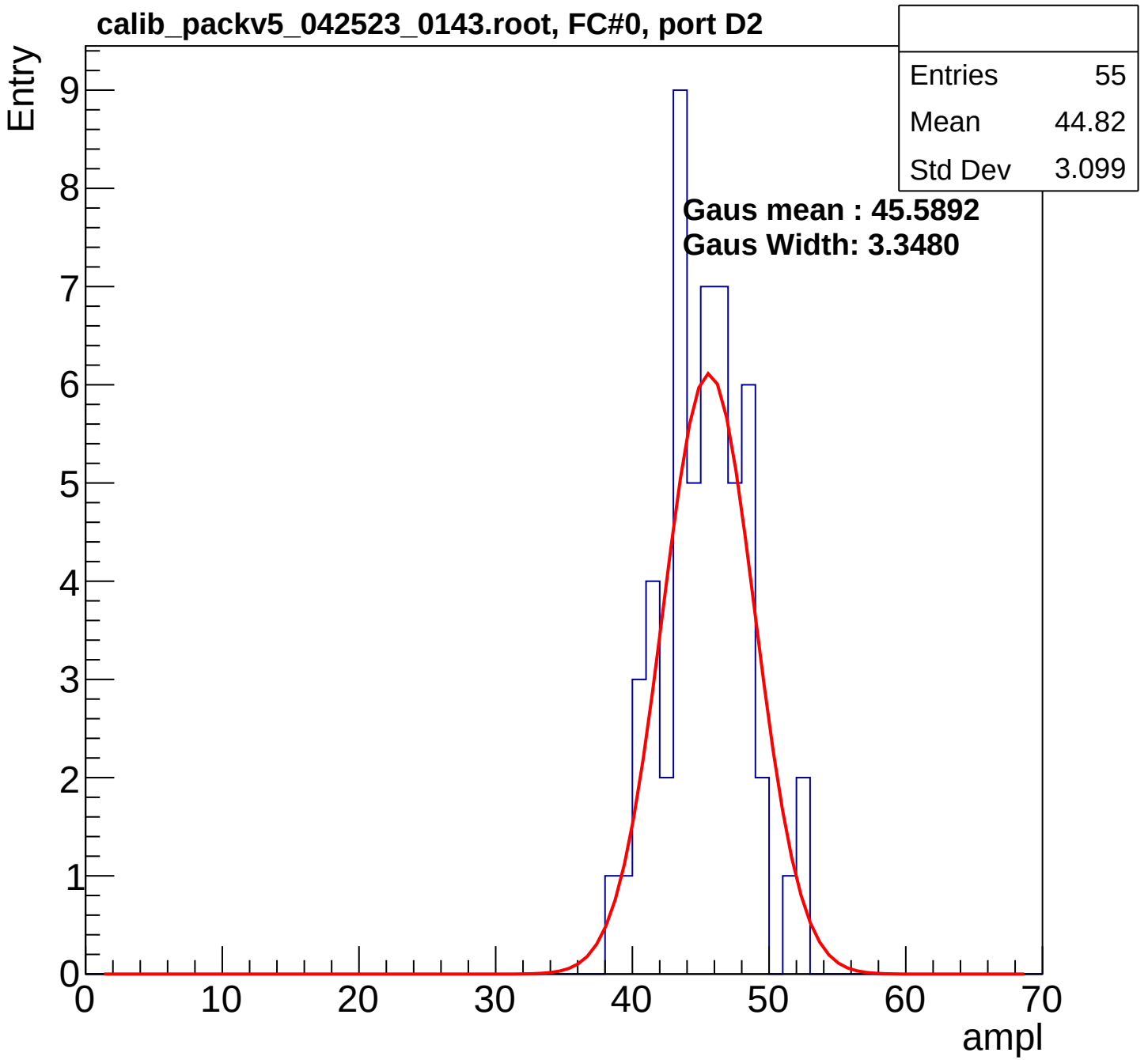
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch115, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 44.82
Std Dev 3.099
Gaus mean : 45.5892
Gaus Width: 3.3480
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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40
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60
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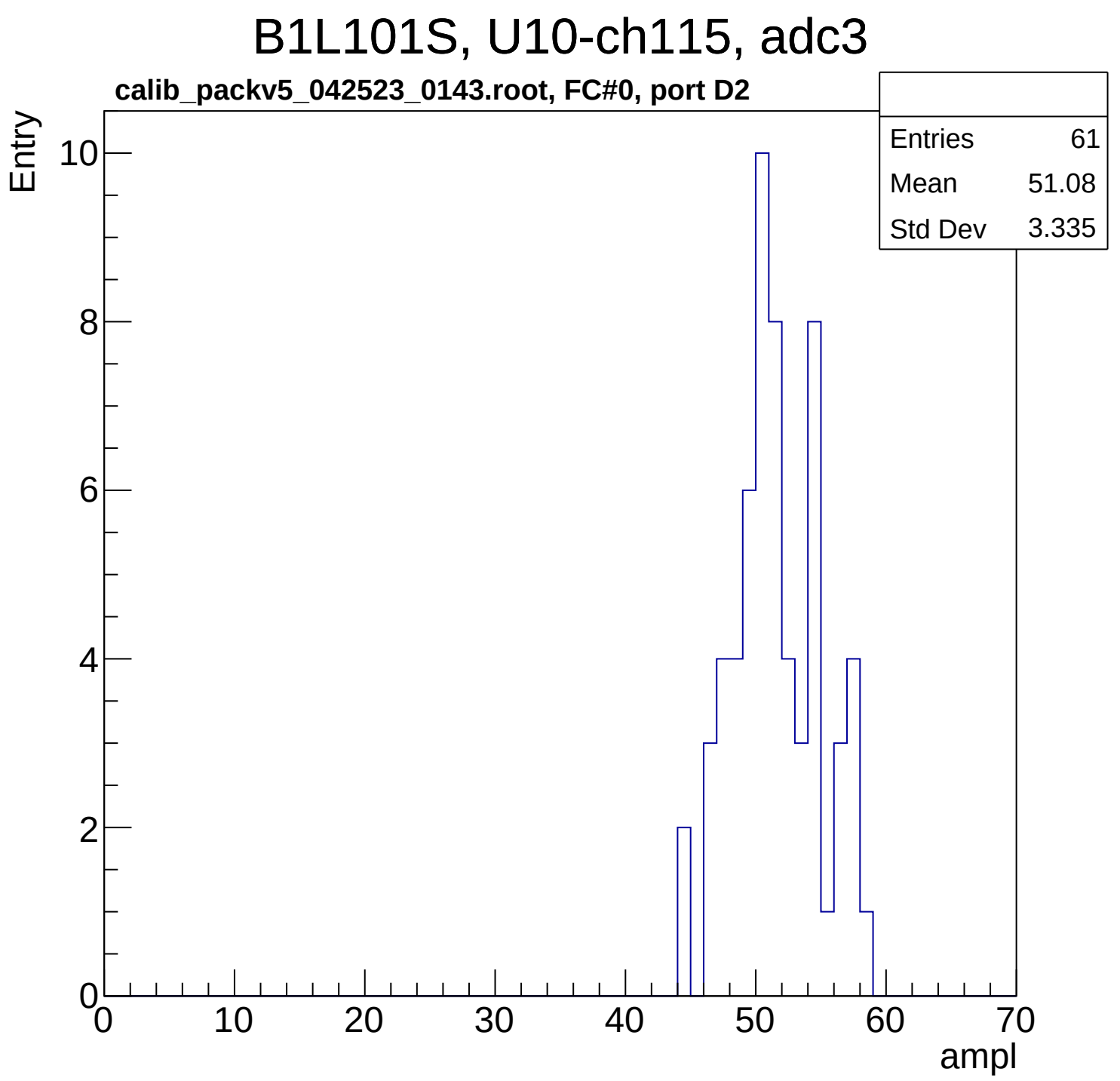
B1L101S, U10-ch115, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 51.08
Std Dev 3.335
Entry
ampl
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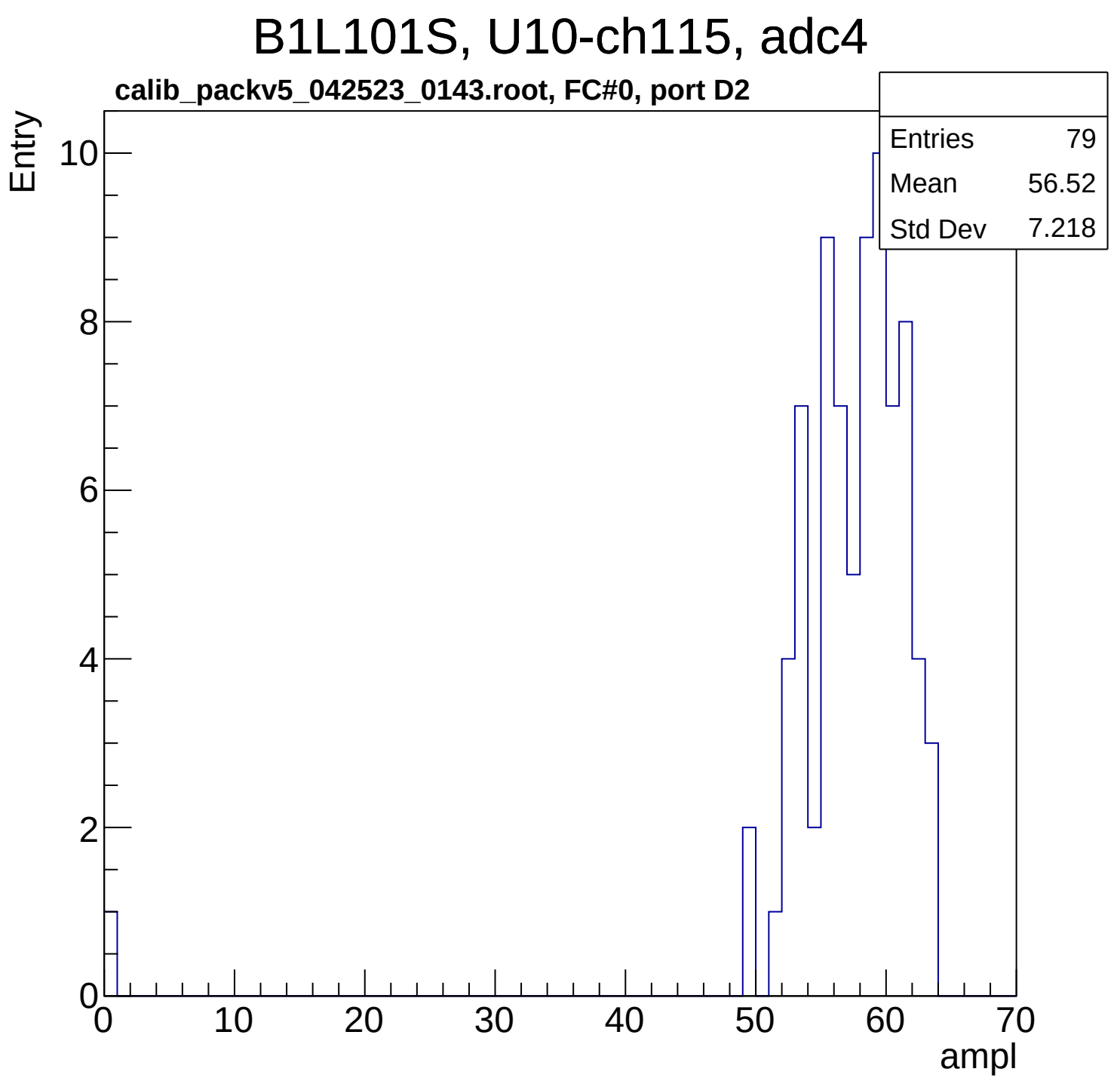
50
60
70


B1L101S, U10-ch115, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 56.52
Std Dev 7.218
Entry
ampl
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0
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60
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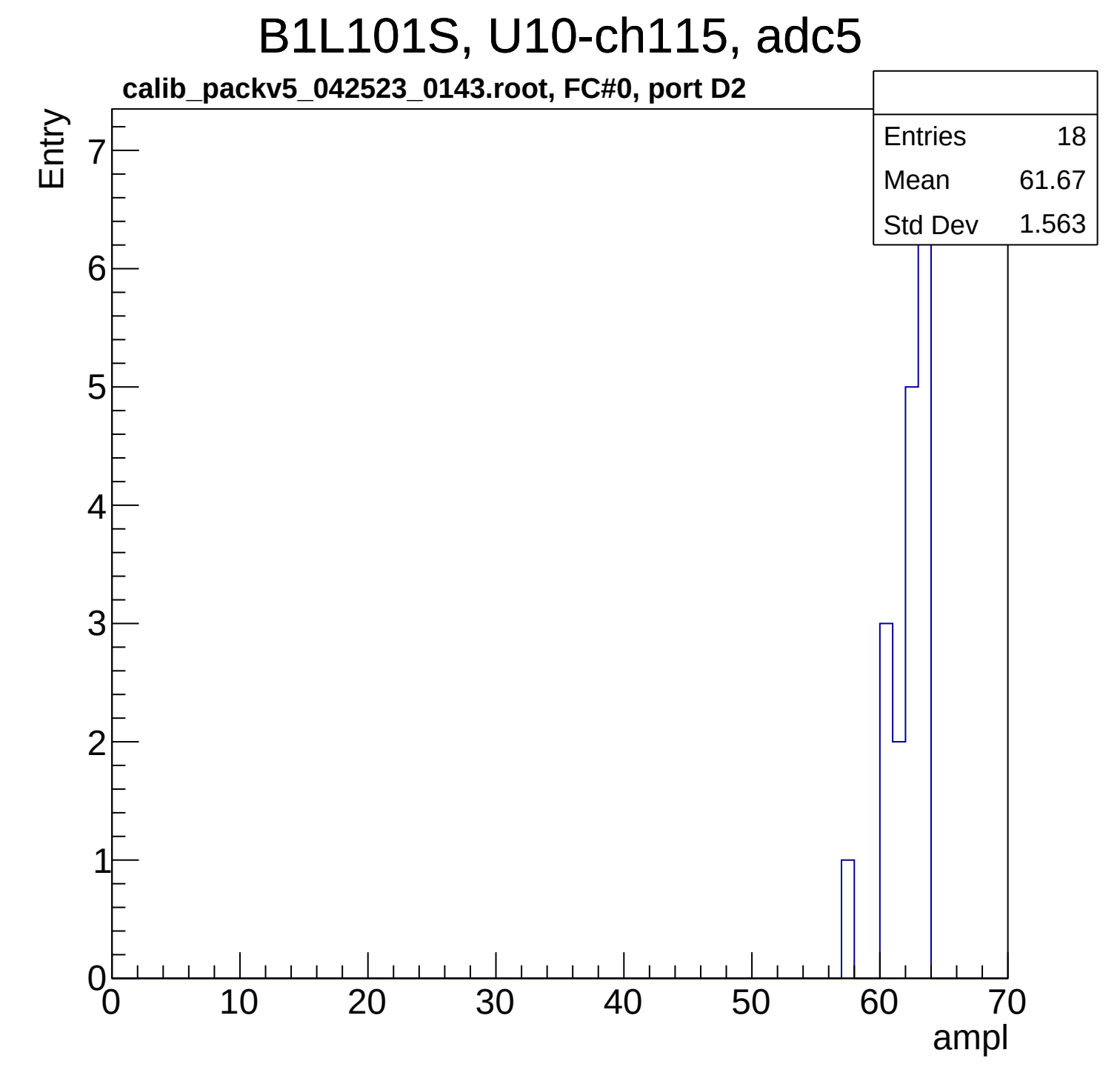
B1L101S, U10-ch115, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 18
Mean 61.67
Std Dev 1.563
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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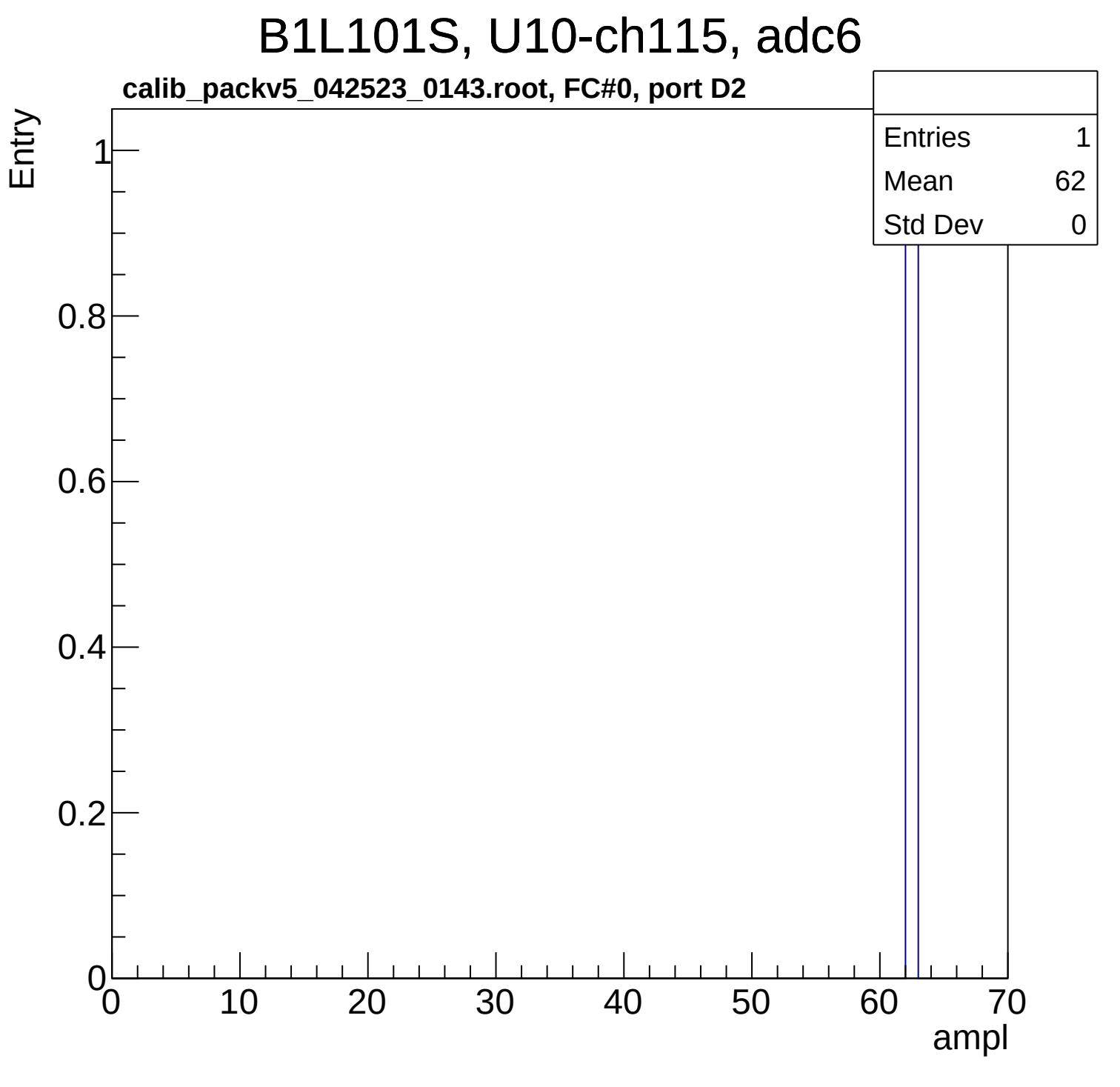
60
70


B1L101S, U10-ch115, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 62
Std Dev 0
Entry
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0.8
0.6
0.4
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10
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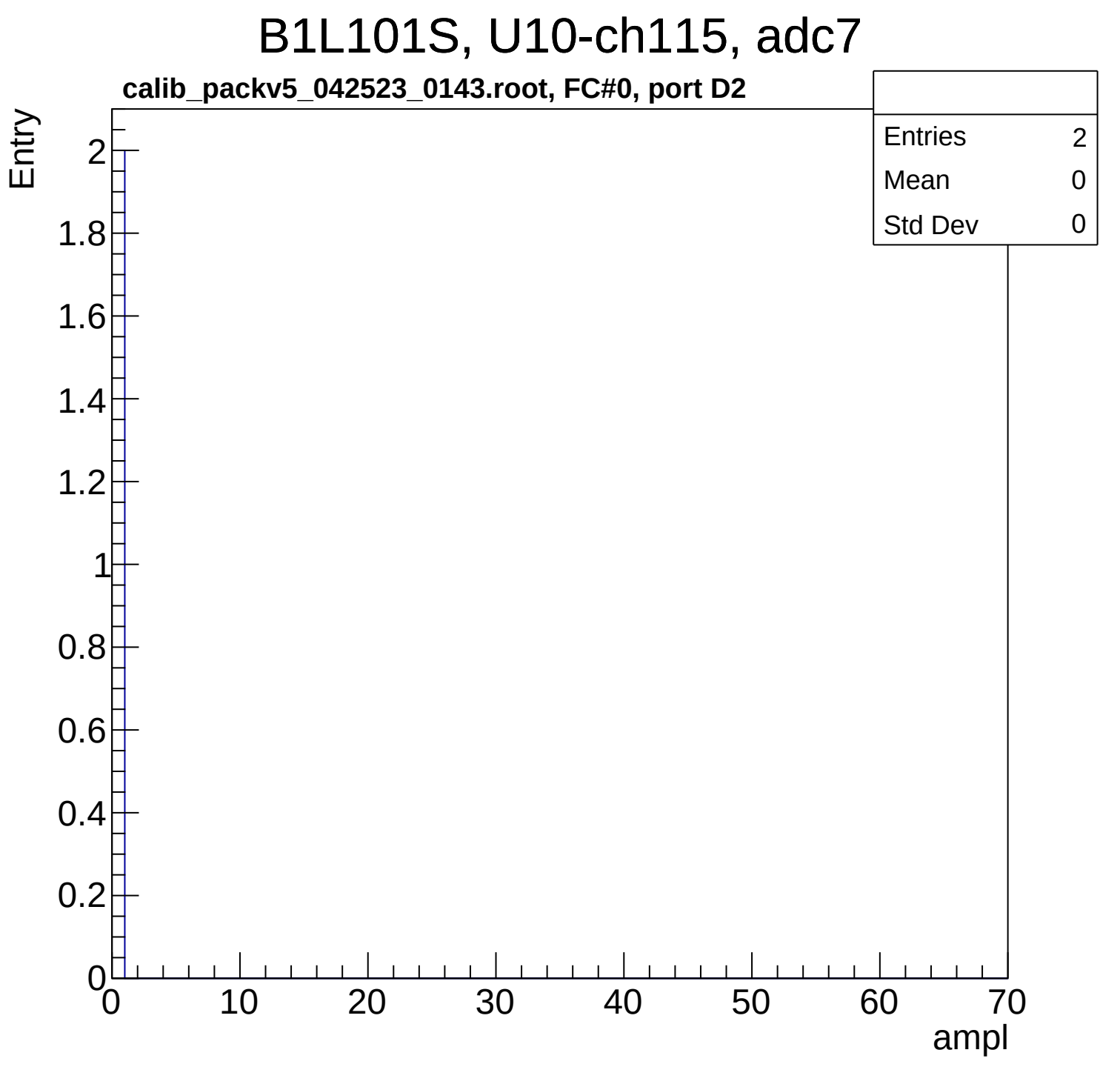
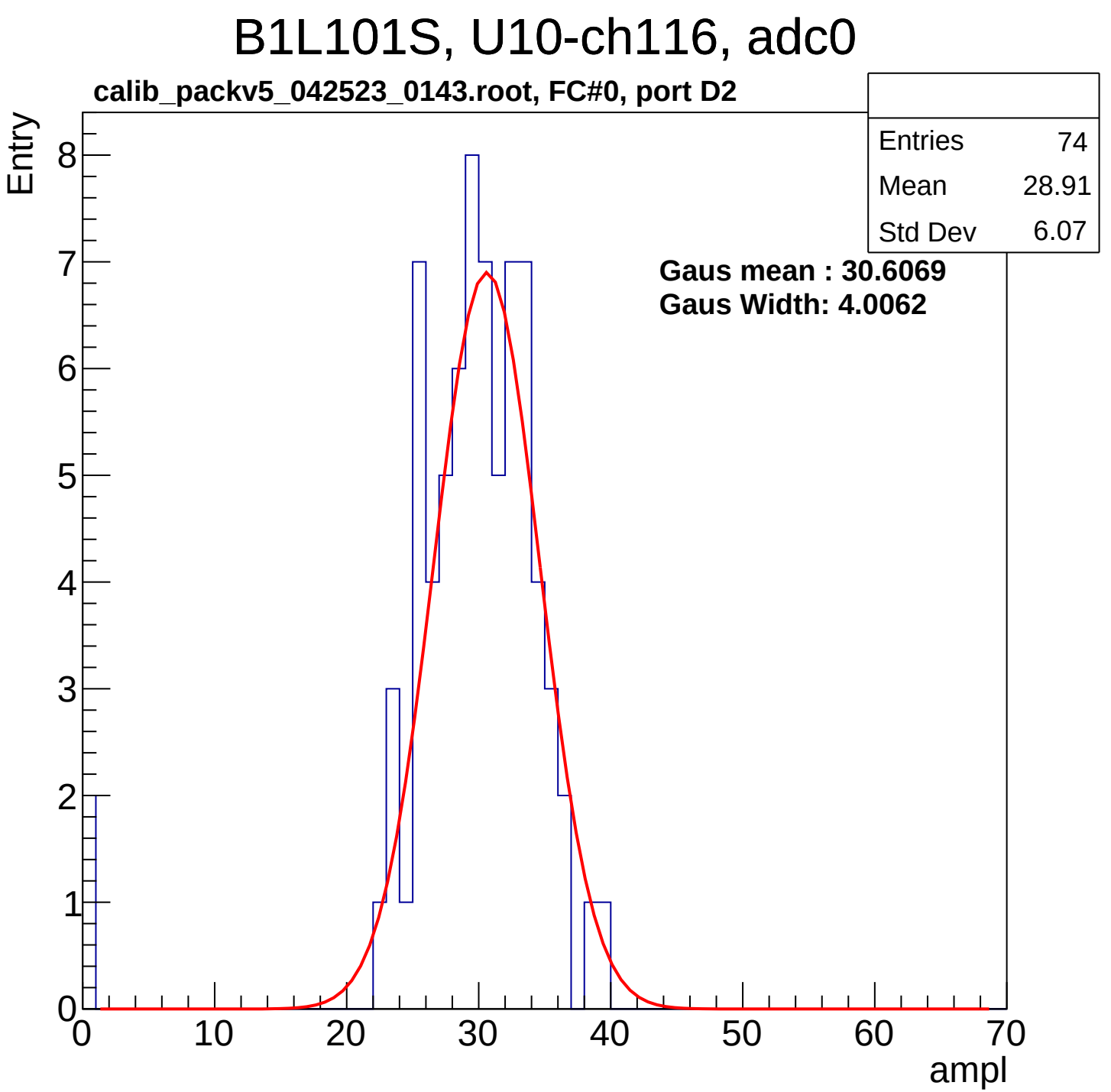
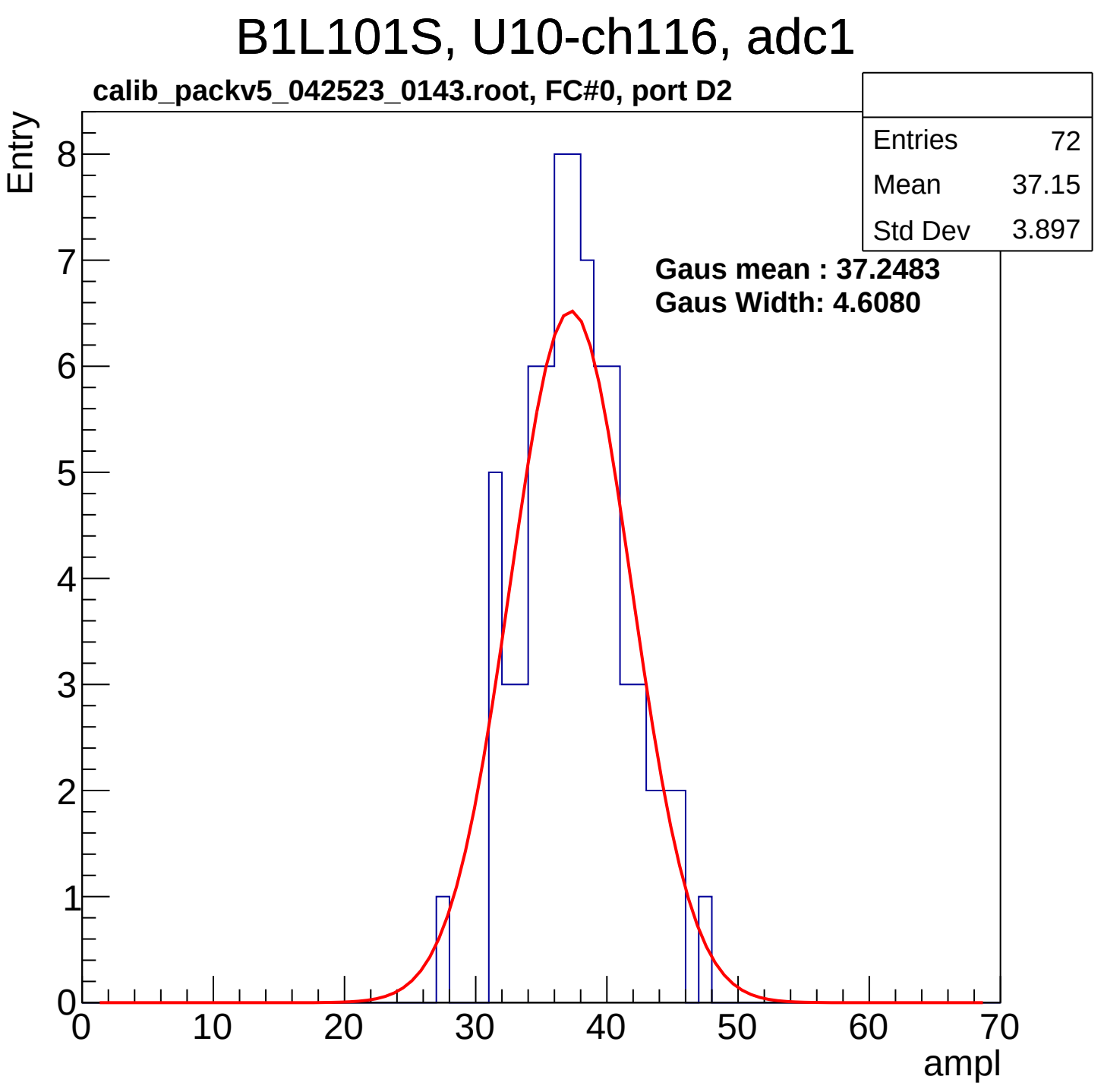
60
70
ampl


B1L101S, U10-ch115, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch116, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 28.91
Std Dev 6.07
Gaus mean : 30.6069
Gaus Width: 4.0062
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch116, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 37.15
Std Dev 3.897
Gaus mean : 37.2483
Gaus Width: 4.6080
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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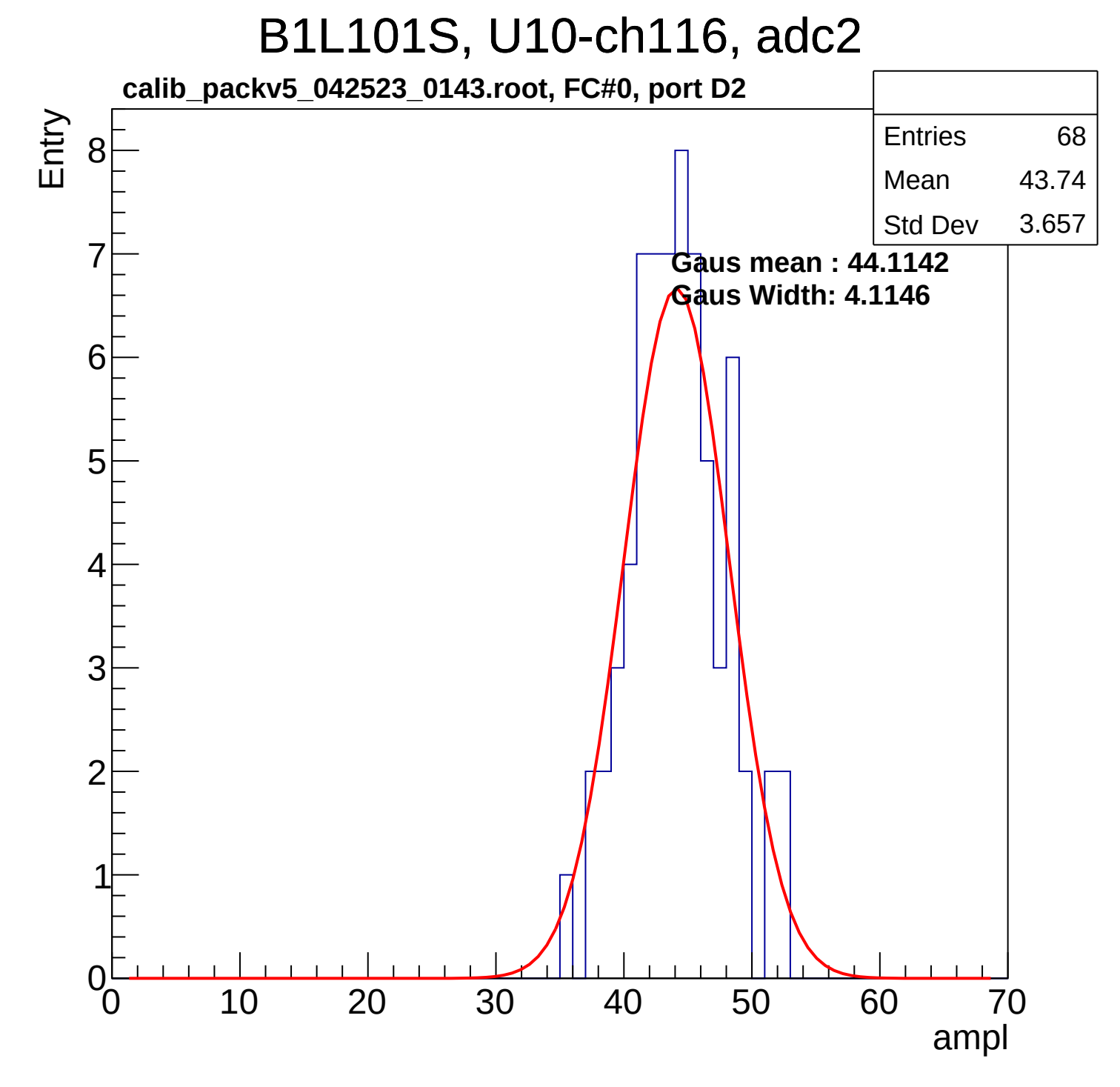
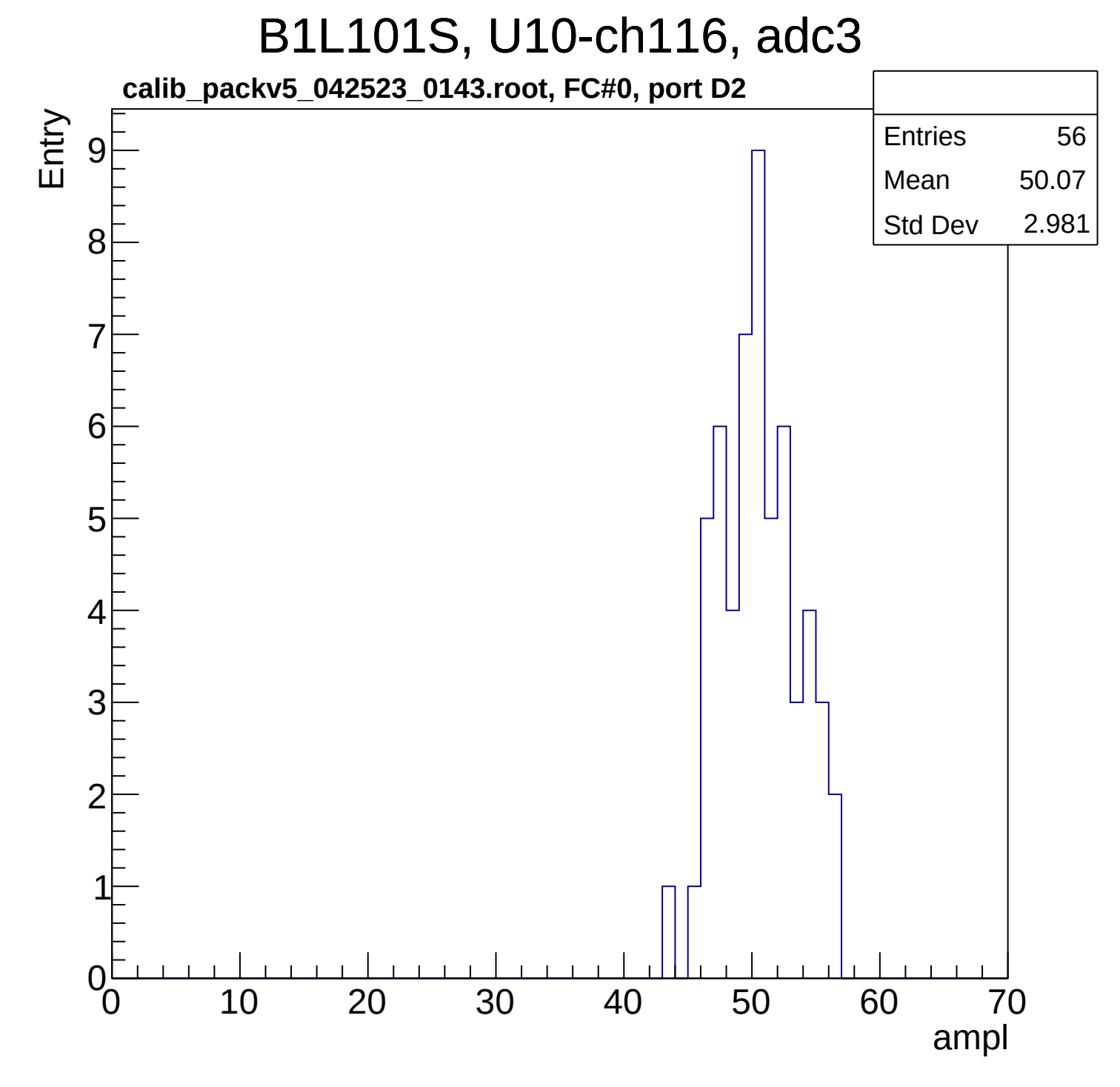
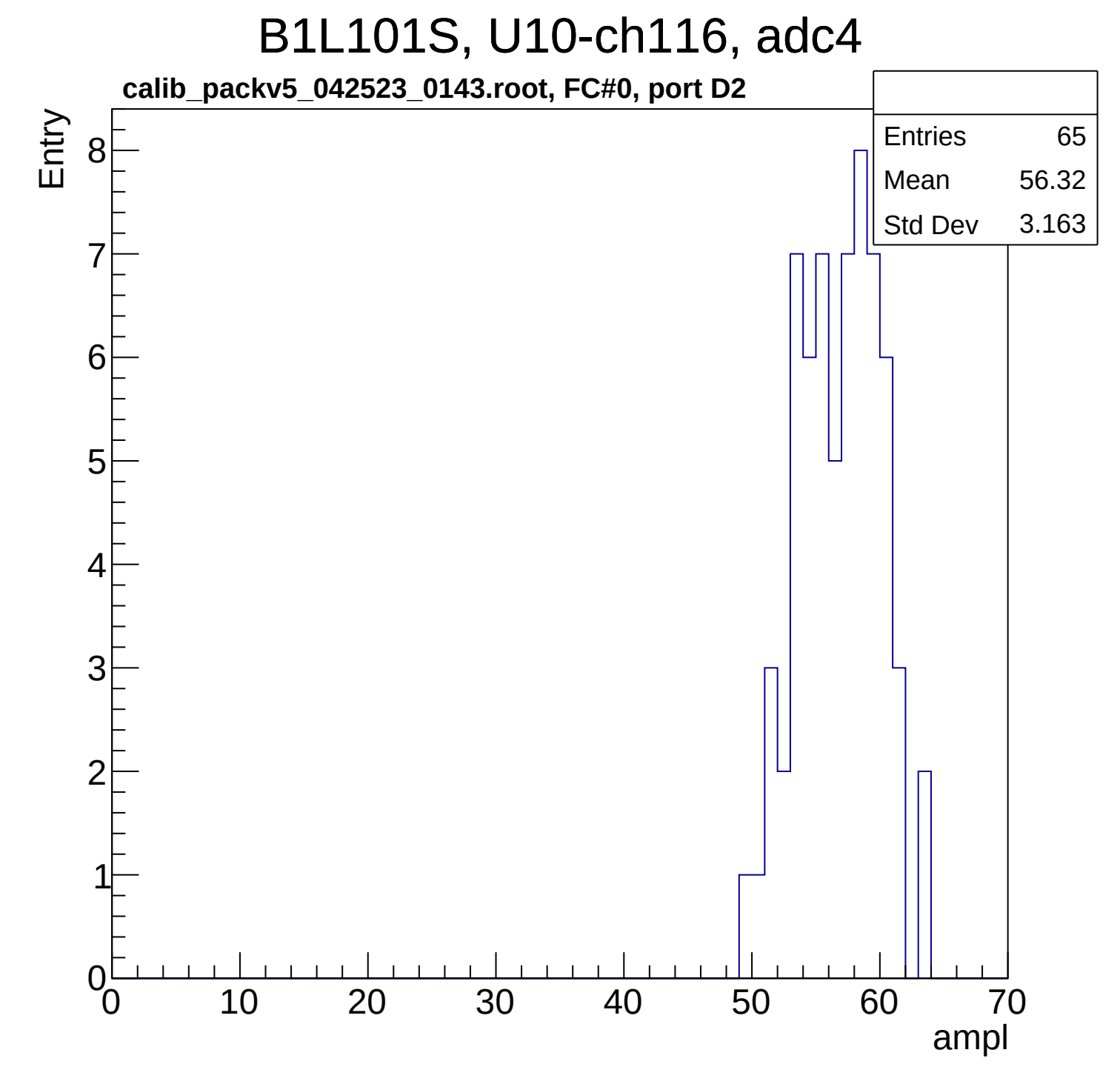

B1L101S, U10-ch116, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 43.74
Std Dev 3.657
Gaus mean : 44.1142
Gaus Width: 4.1146
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch116, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 50.07
Std Dev 2.981
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch116, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 56.32
Std Dev 3.163
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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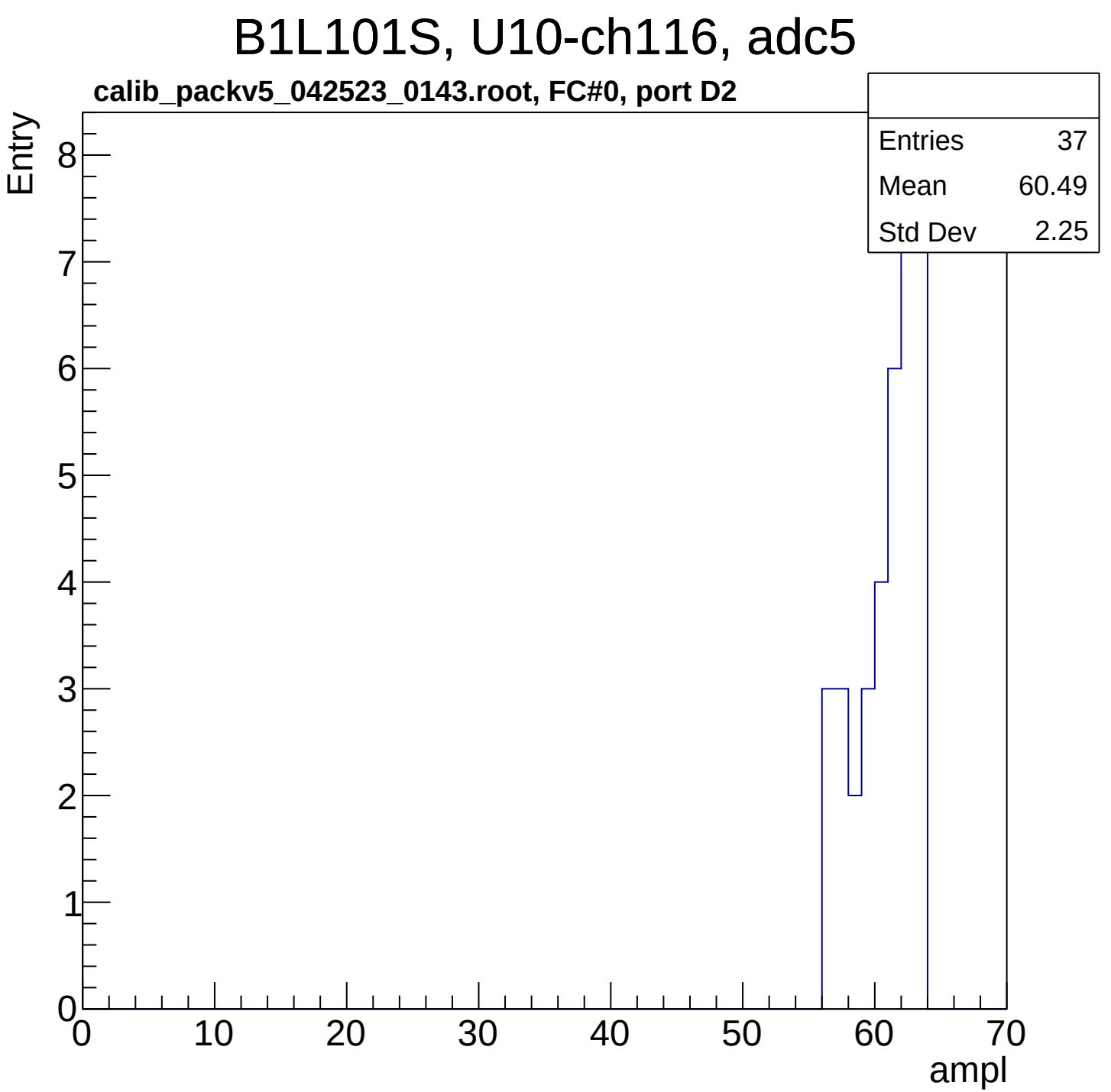
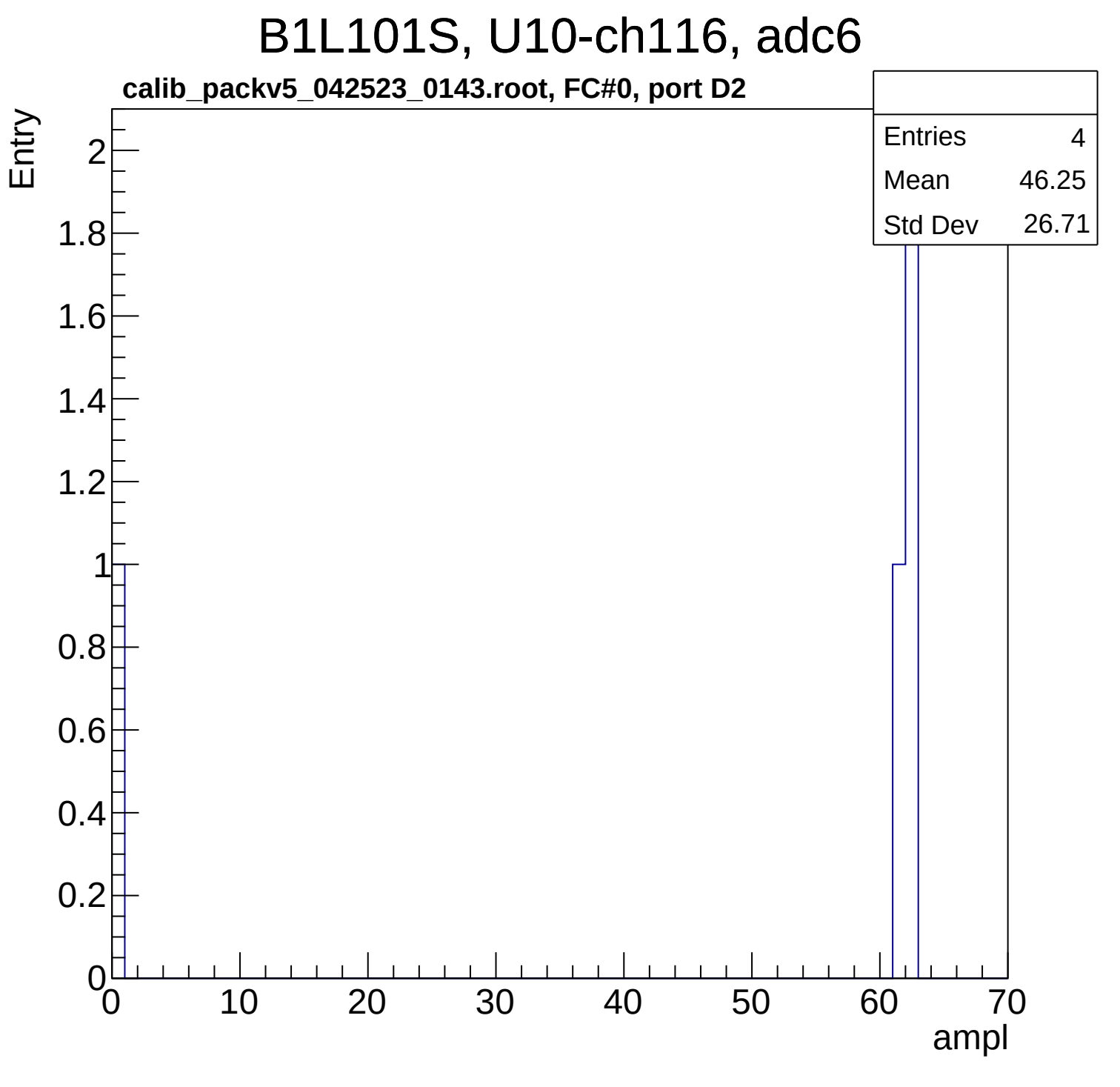
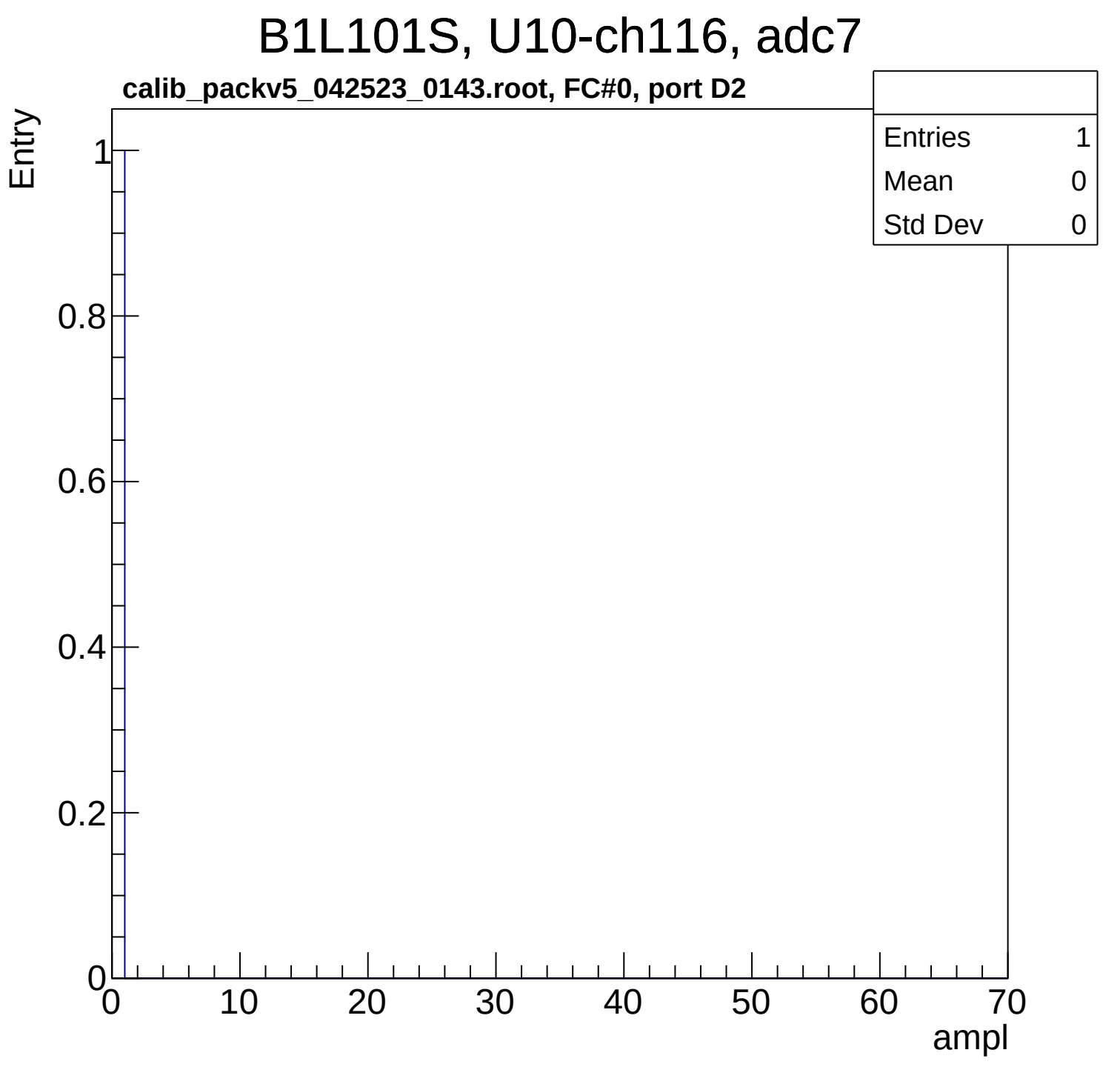
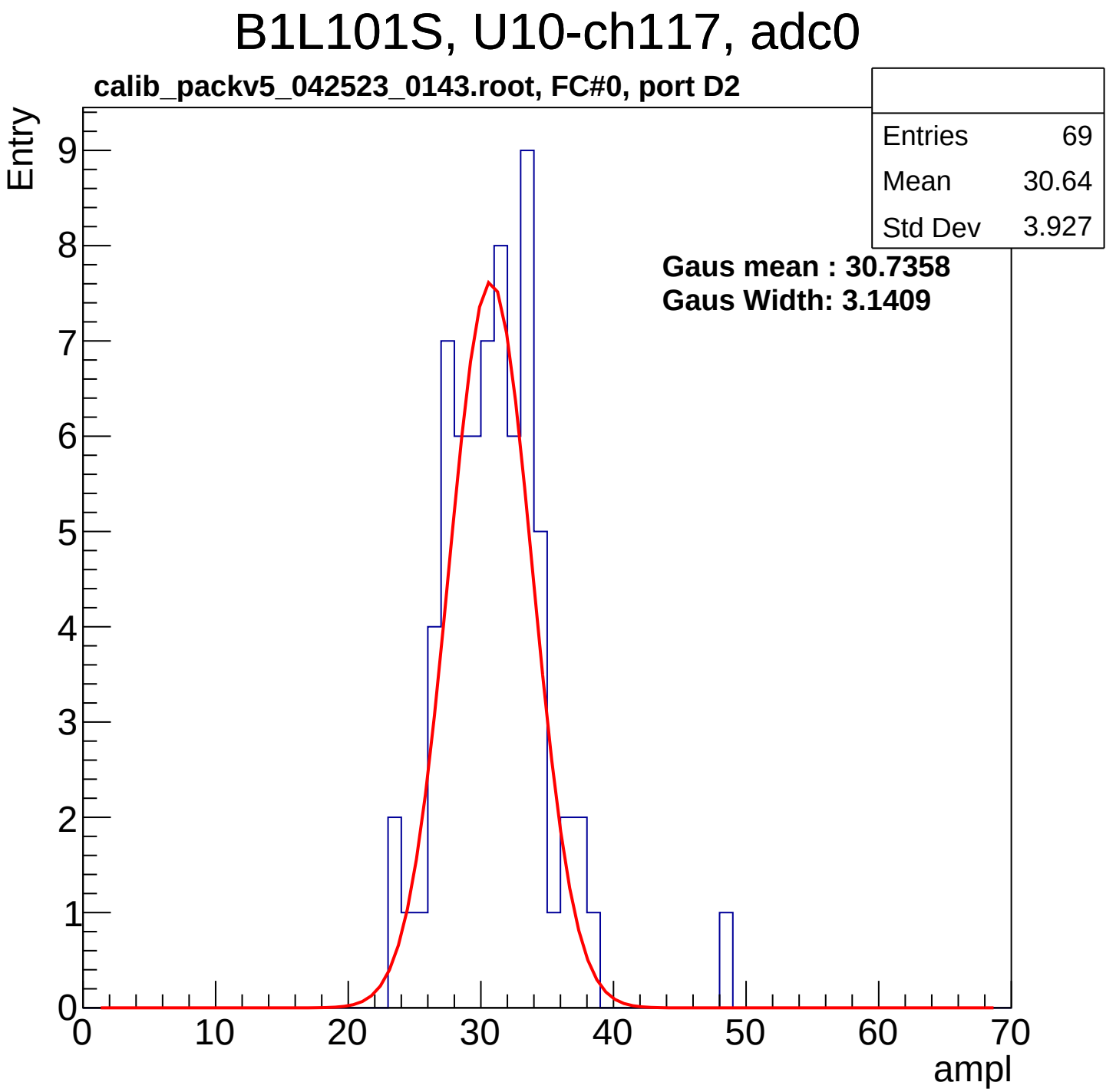

B1L101S, U10-ch116, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 37
Mean 60.49
Std Dev 2.25
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch116, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 46.25
Std Dev 26.71
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U10-ch116, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch117, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 30.64
Std Dev 3.927
Gaus mean : 30.7358
Gaus Width: 3.1409
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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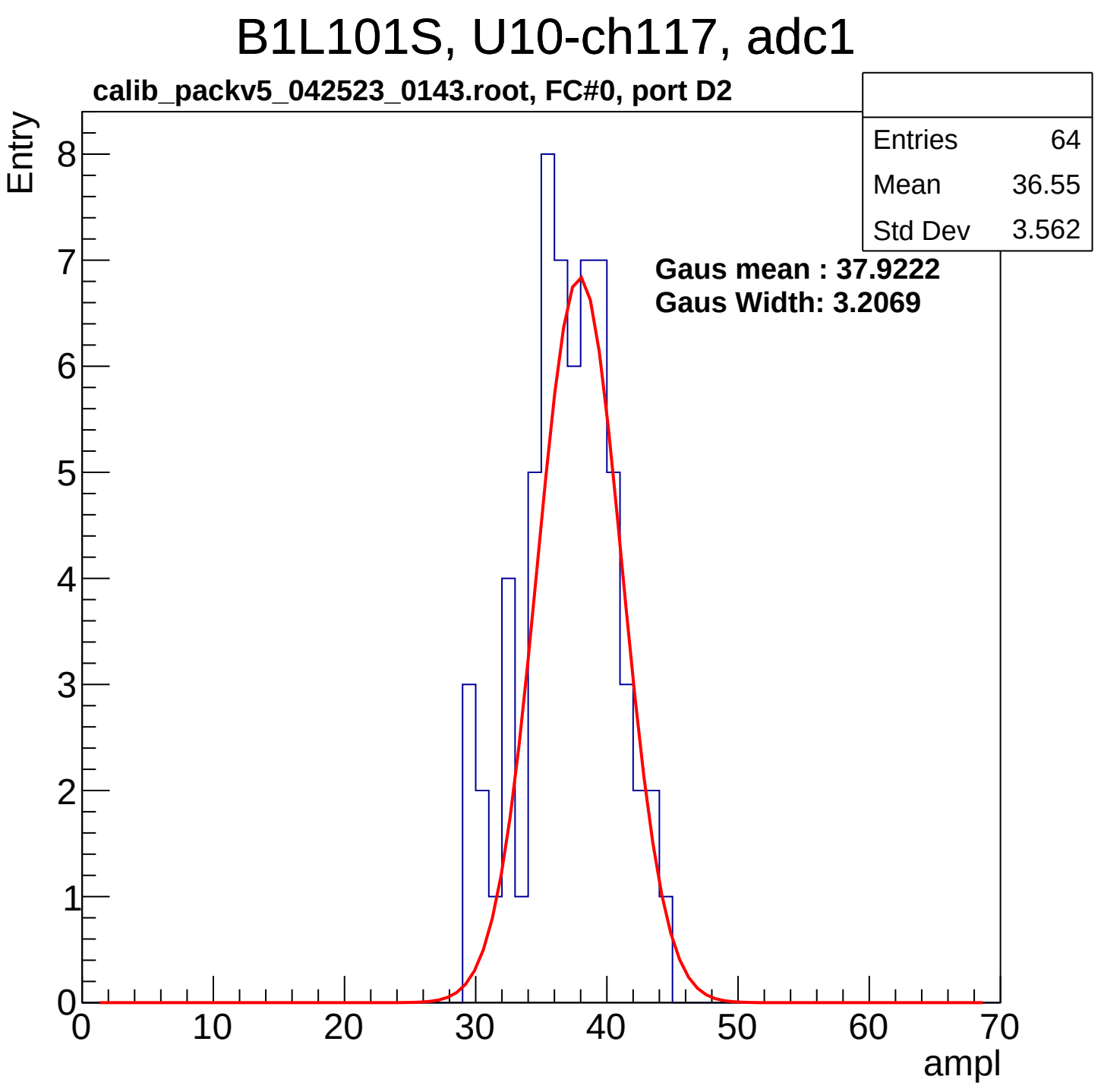
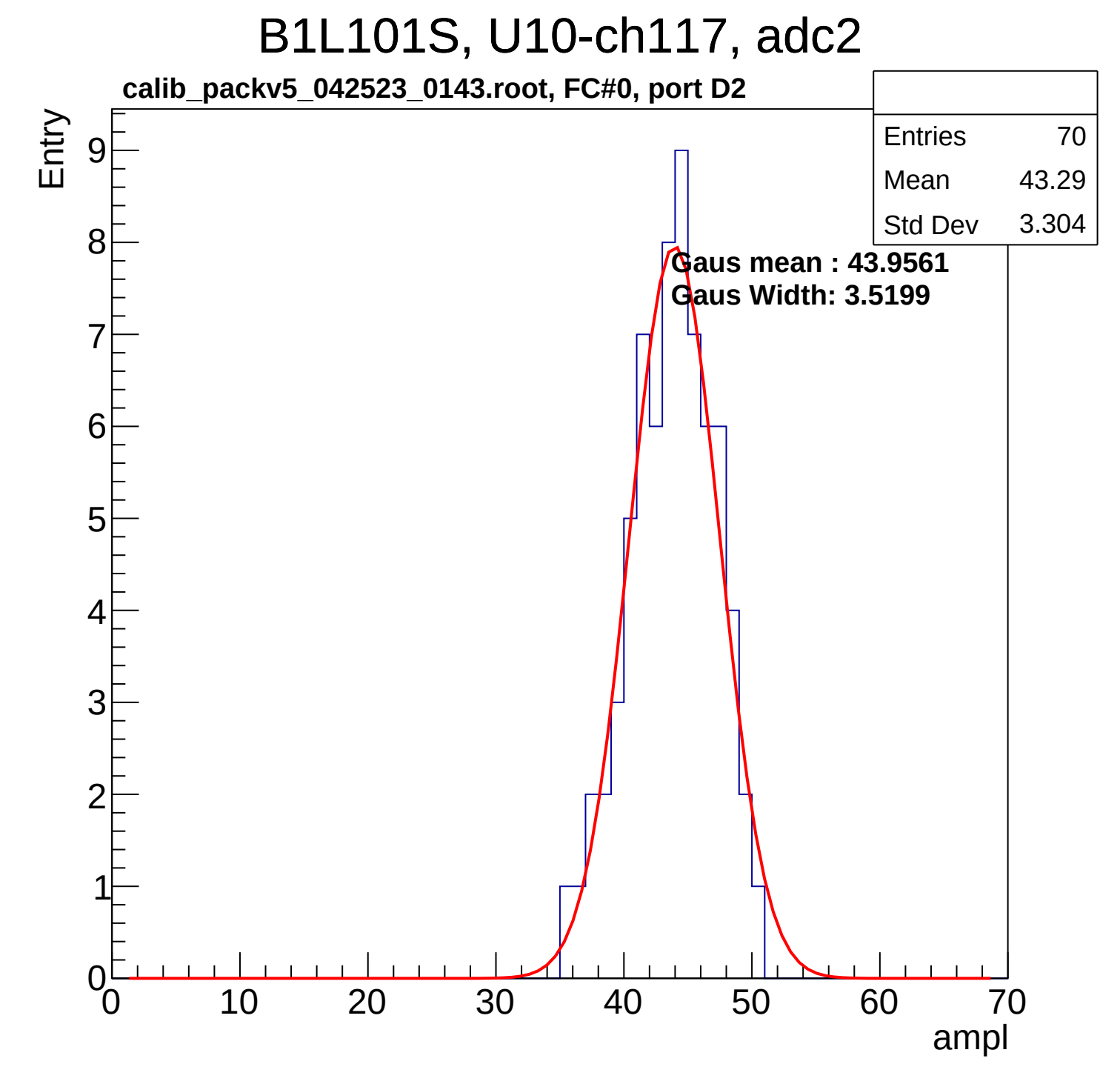
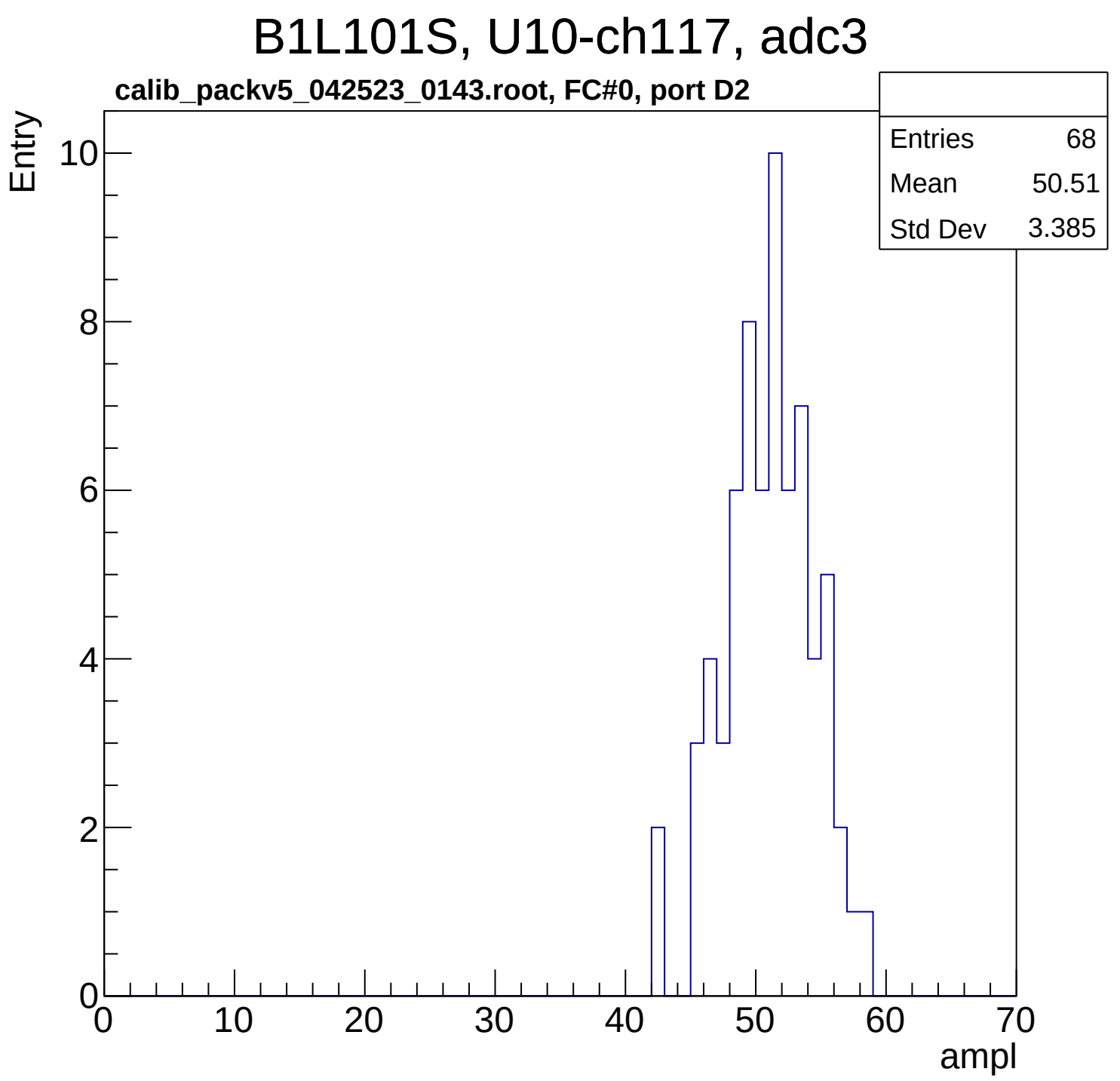
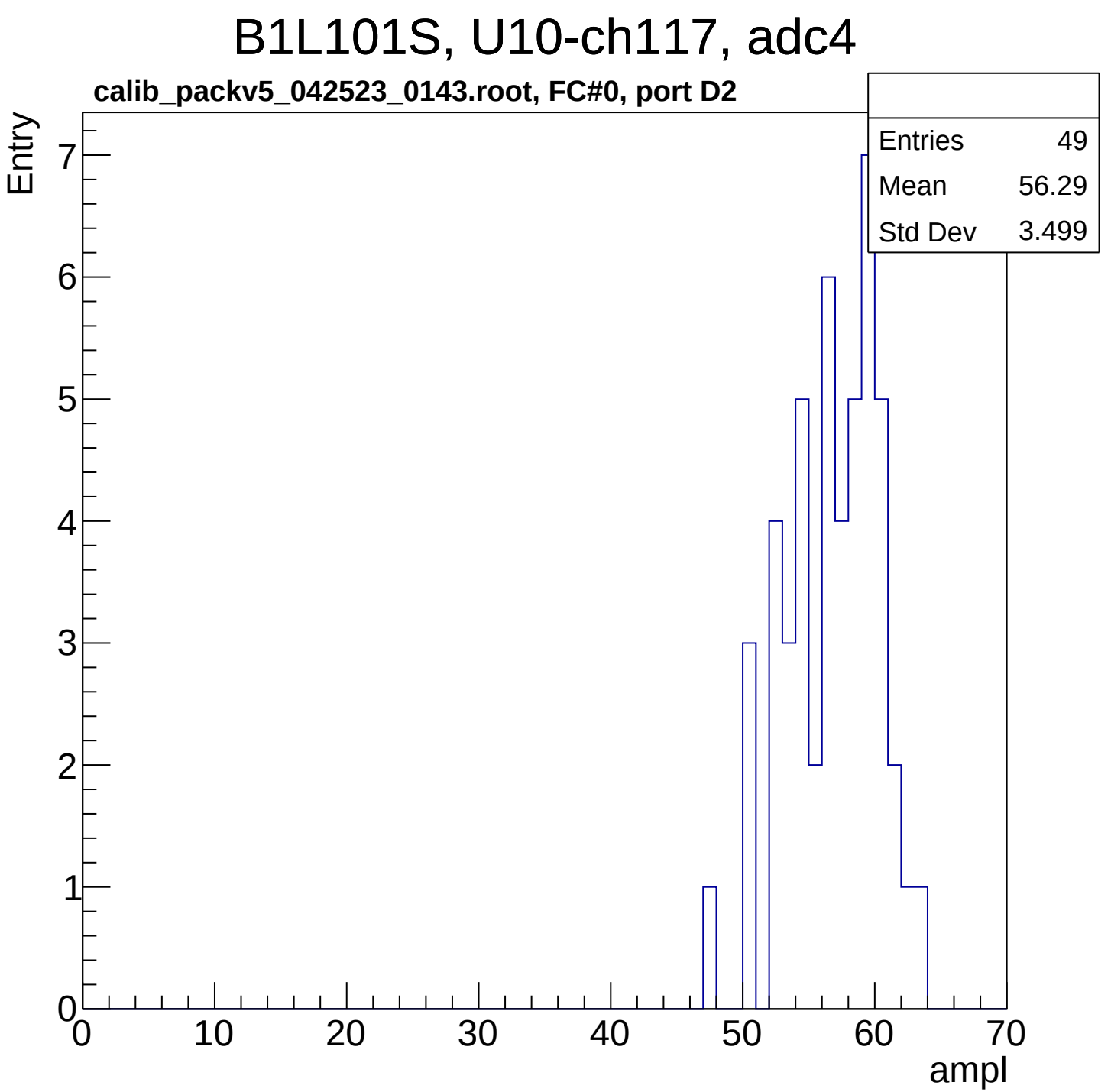

B1L101S, U10-ch117, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 36.55
Std Dev 3.562
Gaus mean : 37.9222
Gaus Width: 3.2069
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch117, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 43.29
Std Dev 3.304
Gaus mean : 43.9561
Gaus Width: 3.5199
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch117, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 50.51
Std Dev 3.385
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch117, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 56.29
Std Dev 3.499
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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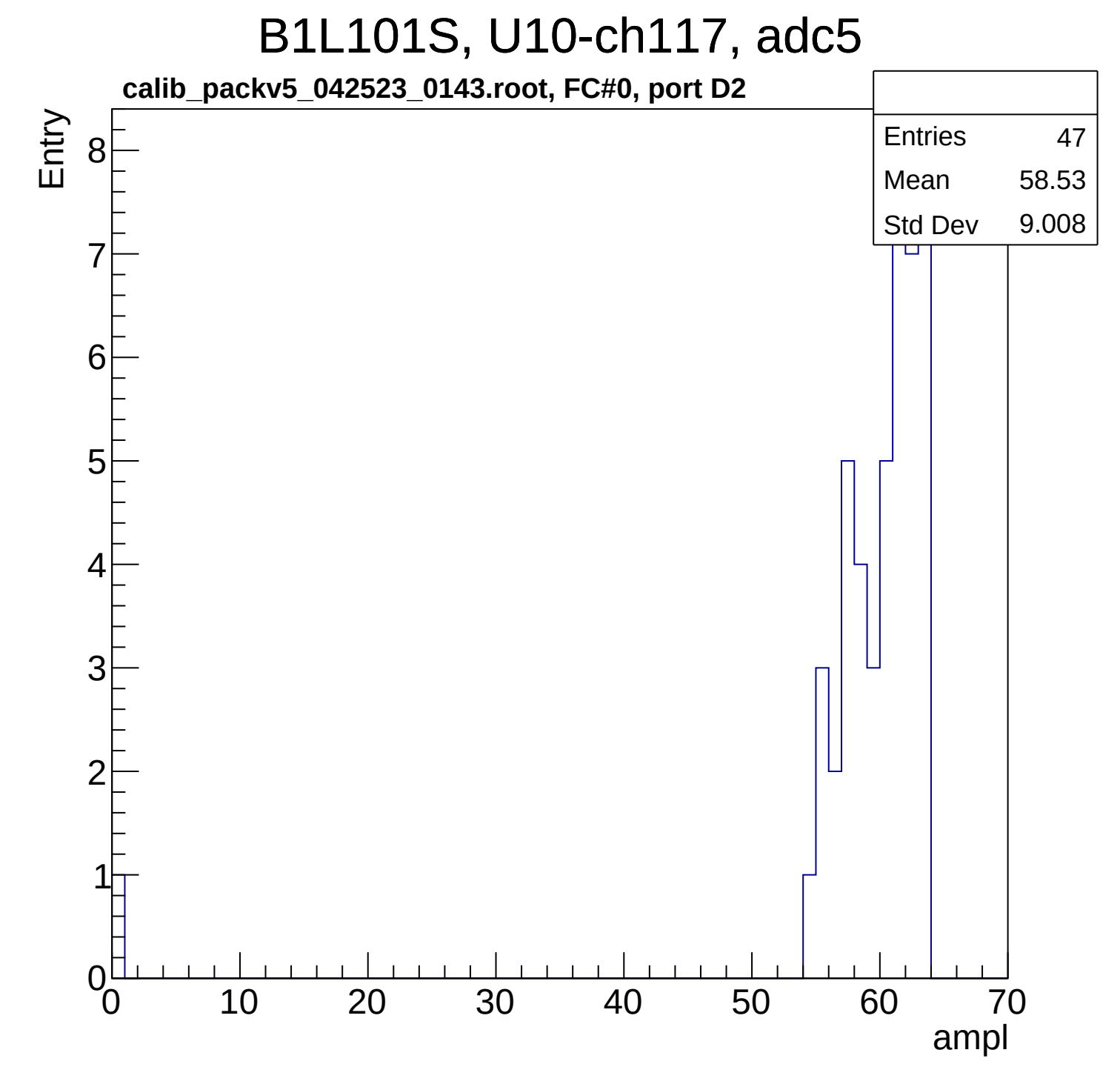
B1L101S, U10-ch117, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 58.53
Std Dev 9.008
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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60
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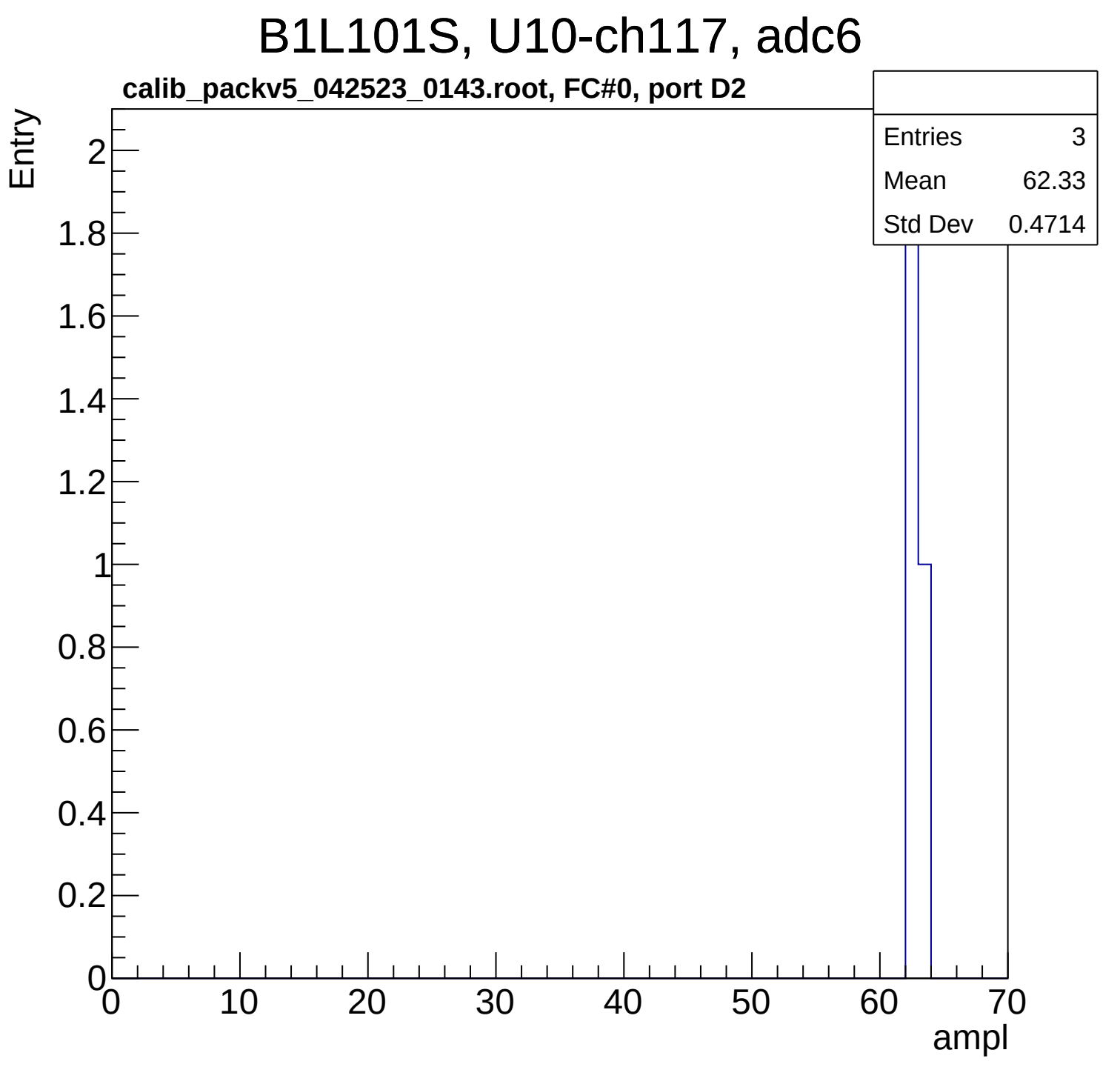
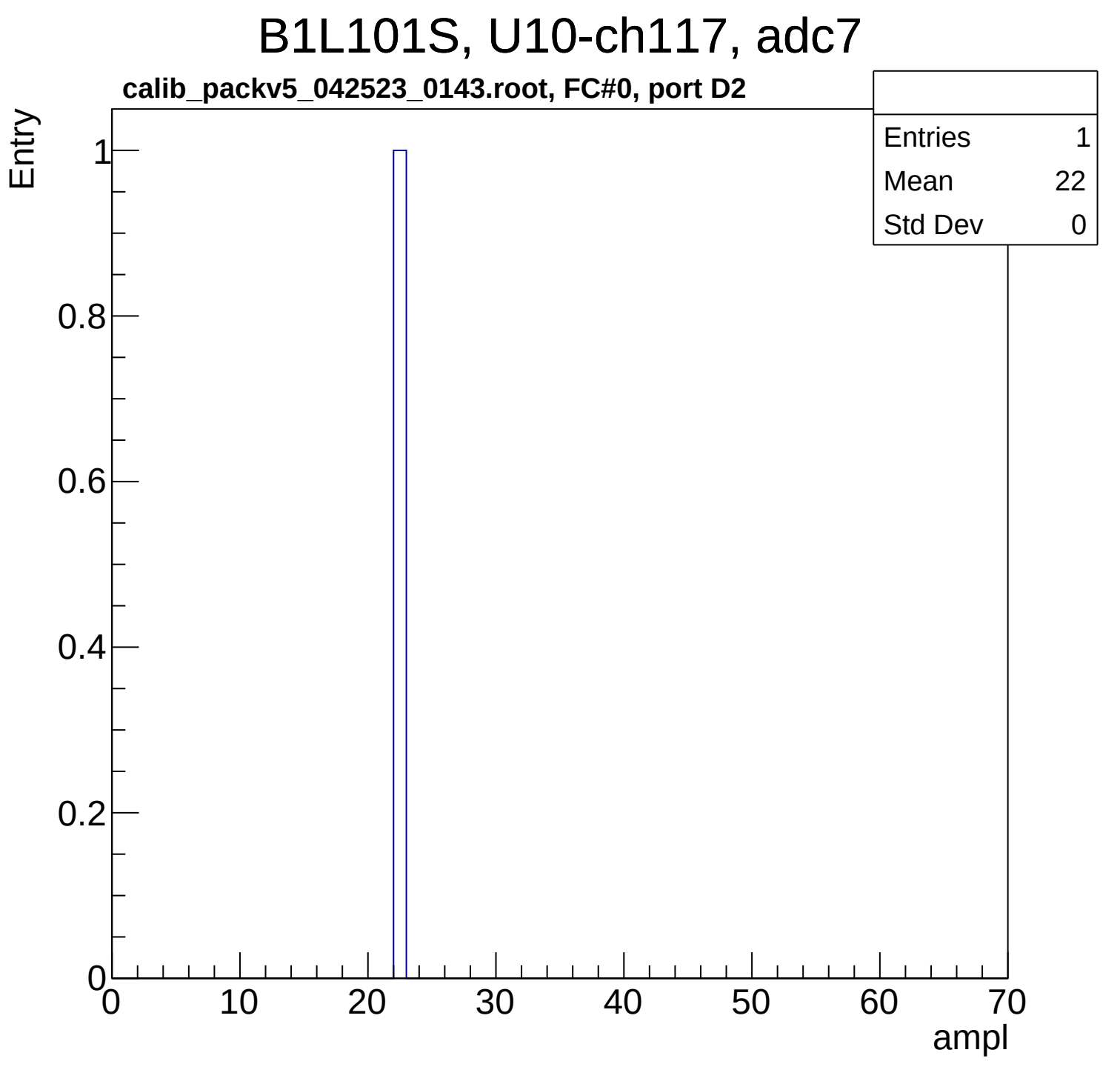

B1L101S, U10-ch117, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U10-ch117, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 22
Std Dev 0
Entry
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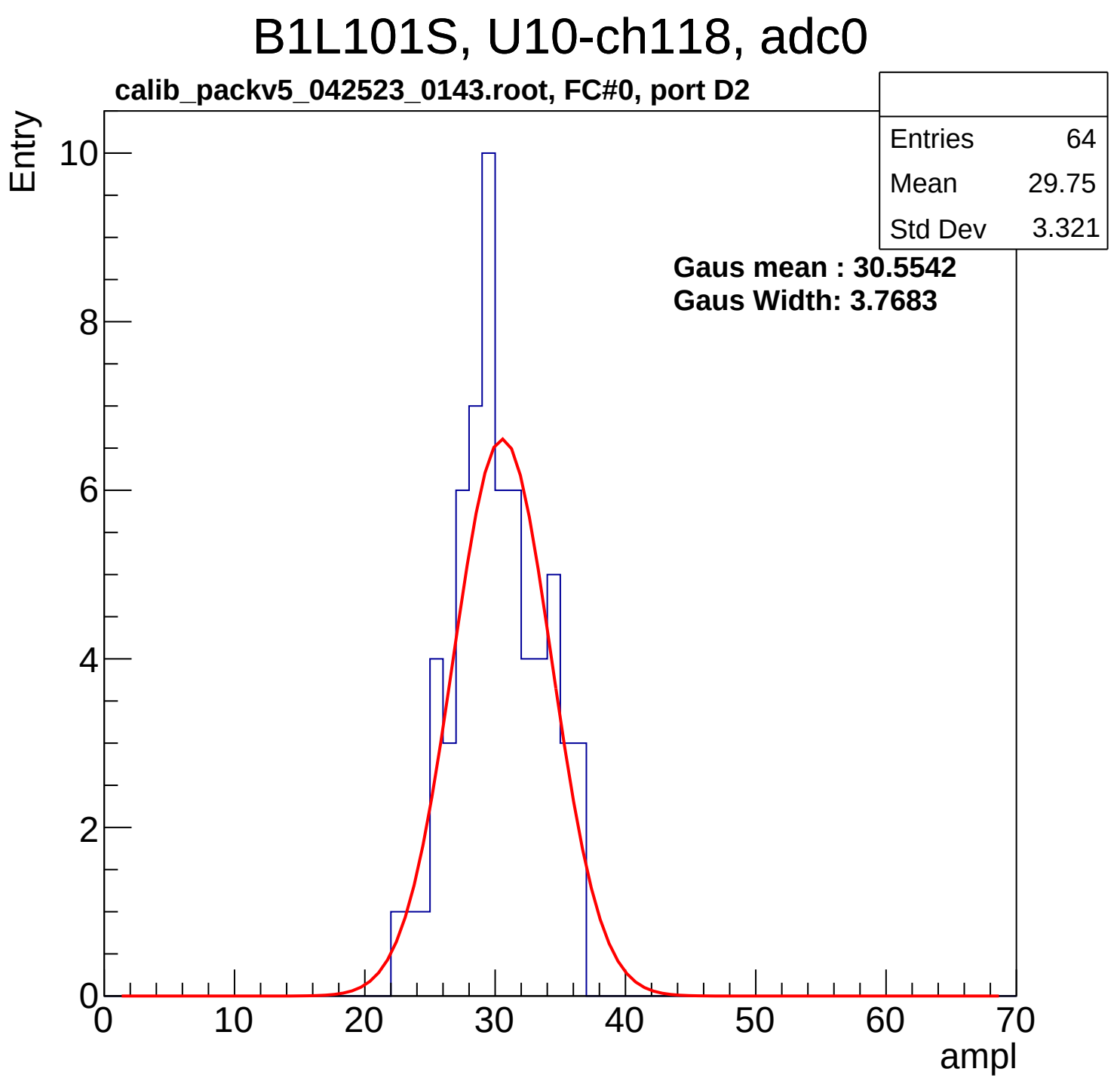
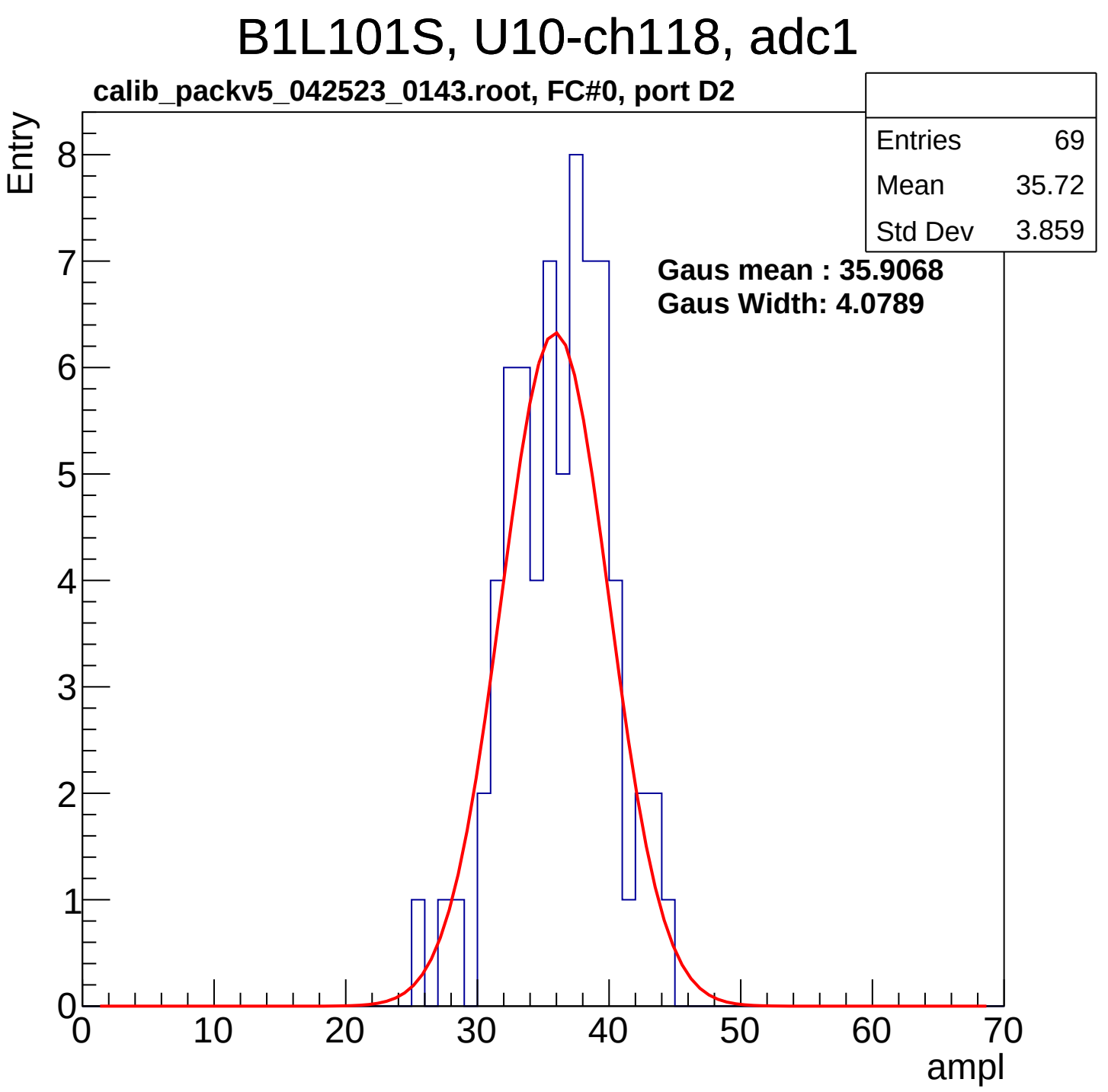
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch118, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 29.75
Std Dev 3.321
Gaus mean : 30.5542
Gaus Width: 3.7683
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch118, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 35.72
Std Dev 3.859
Gaus mean : 35.9068
Gaus Width: 4.0789
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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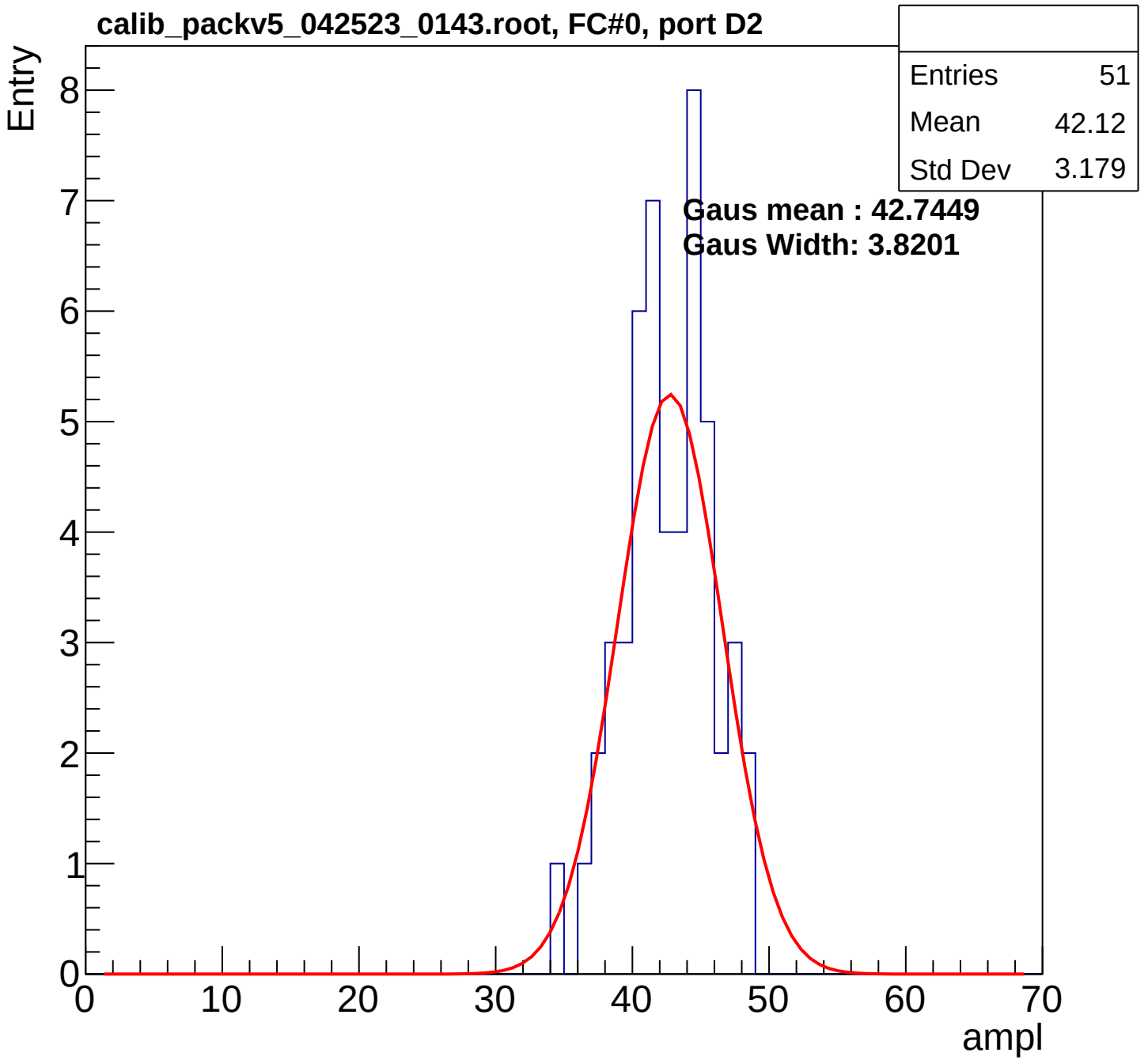
B1L101S, U10-ch118, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 42.12
Std Dev 3.179
Gaus mean : 42.7449
Gaus Width: 3.8201
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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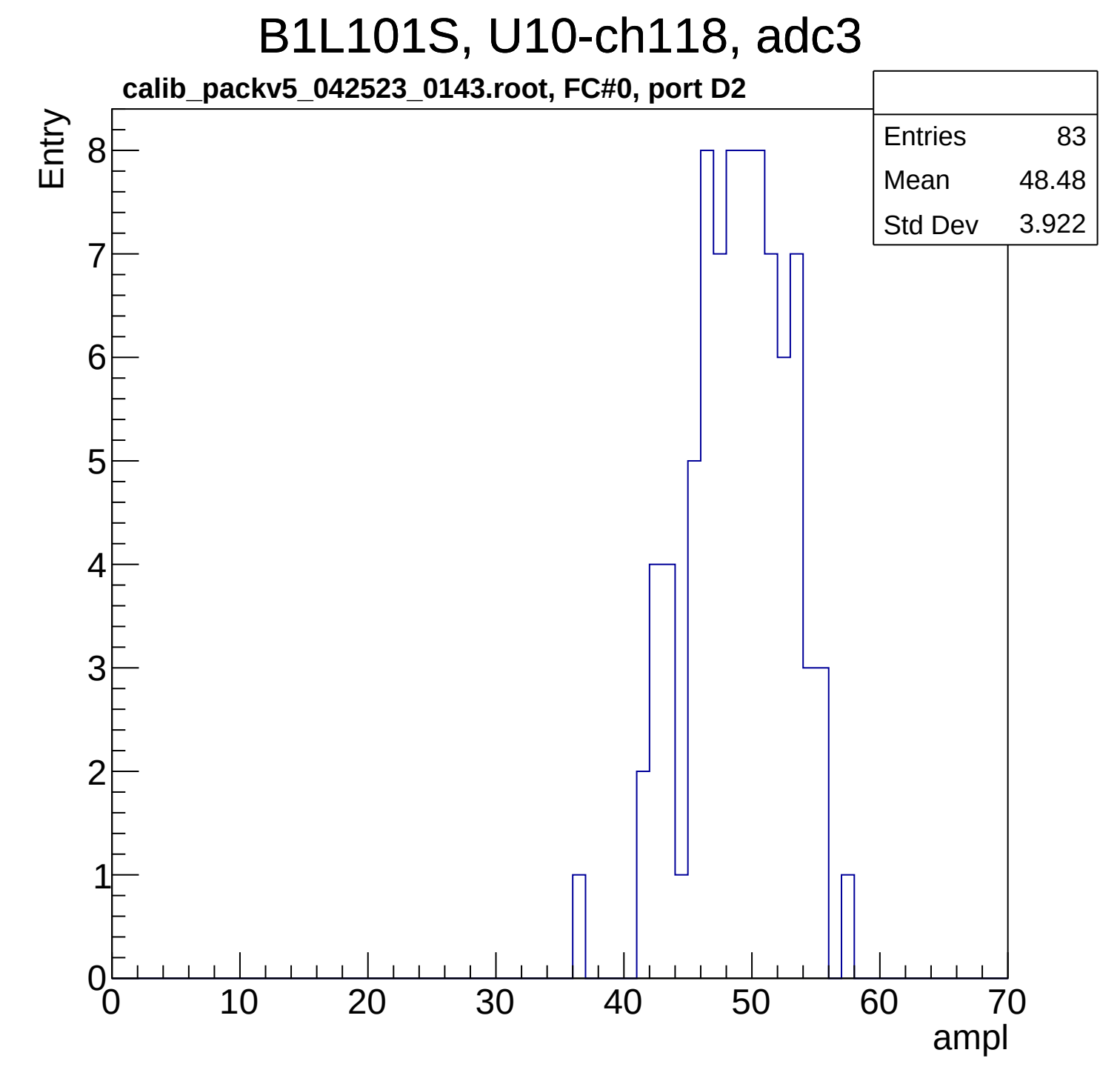
B1L101S, U10-ch118, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 83
Mean 48.48
Std Dev 3.922
Entry
ampl
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4
5
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7
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0
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20
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40
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60
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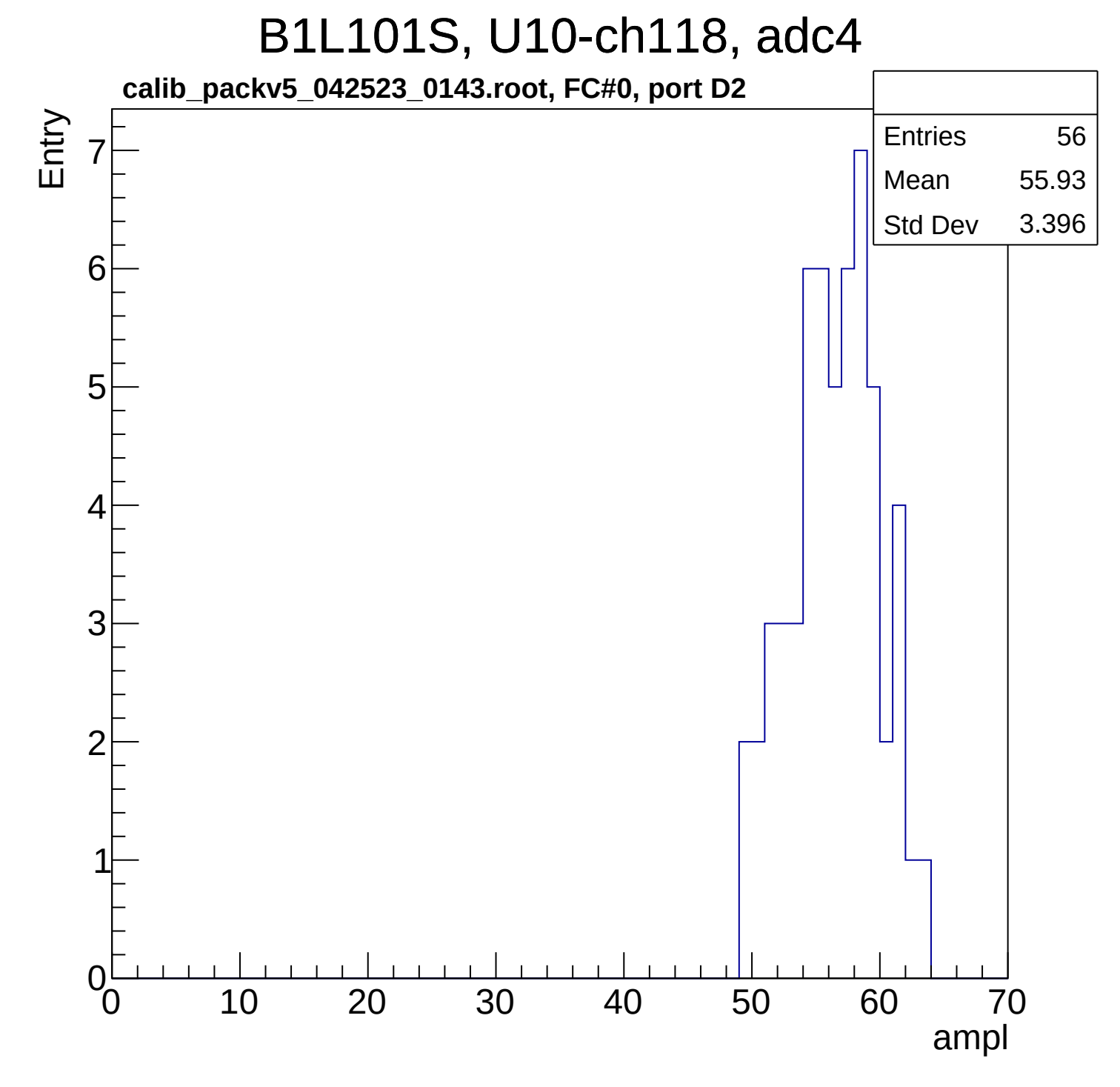
B1L101S, U10-ch118, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 55.93
Std Dev 3.396
Entry
ampl
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4
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0
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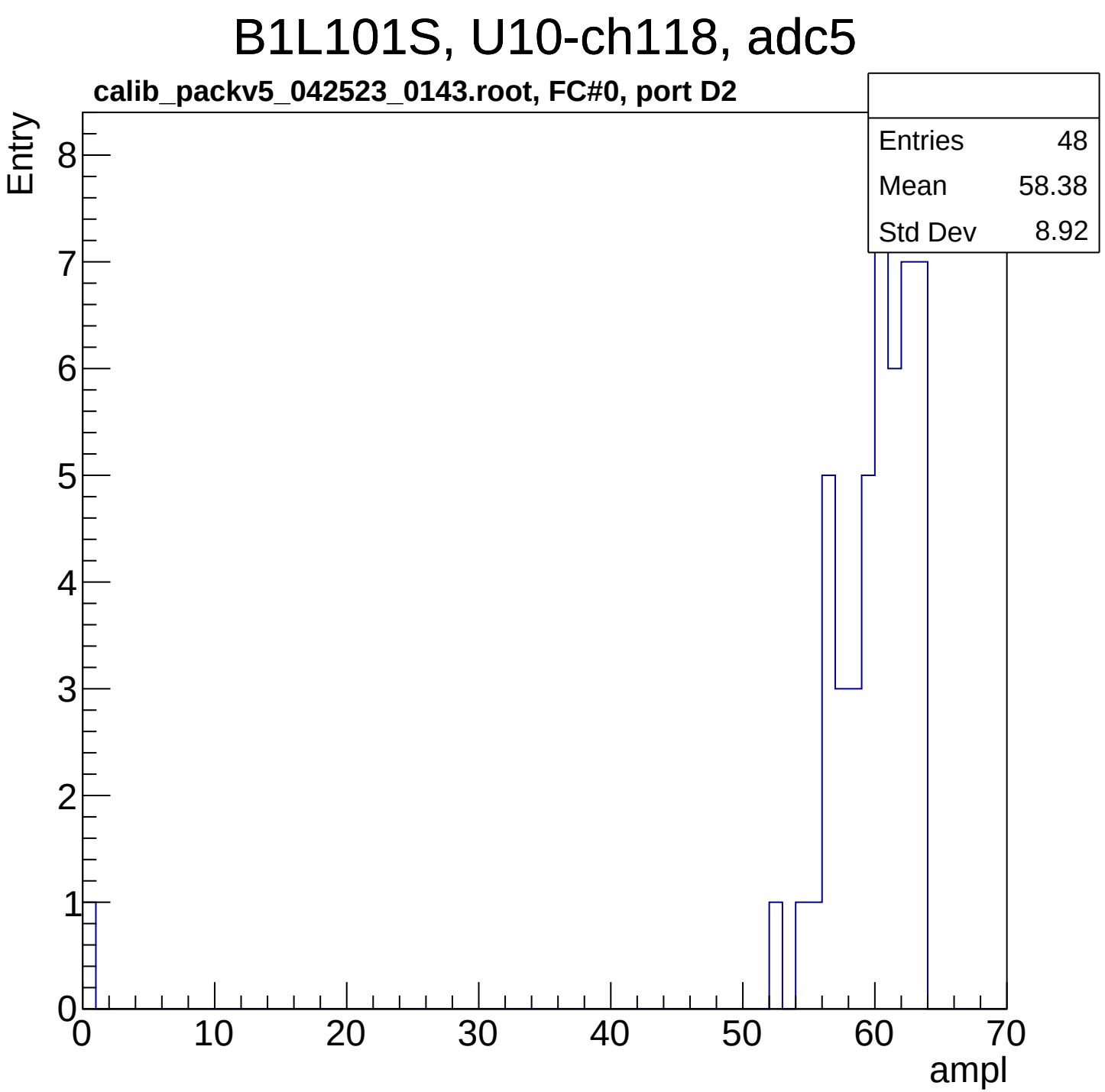
50
60
70


B1L101S, U10-ch118, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 58.38
Std Dev 8.92
Entry
ampl
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1
2
3
4
5
6
7
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0
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40
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60
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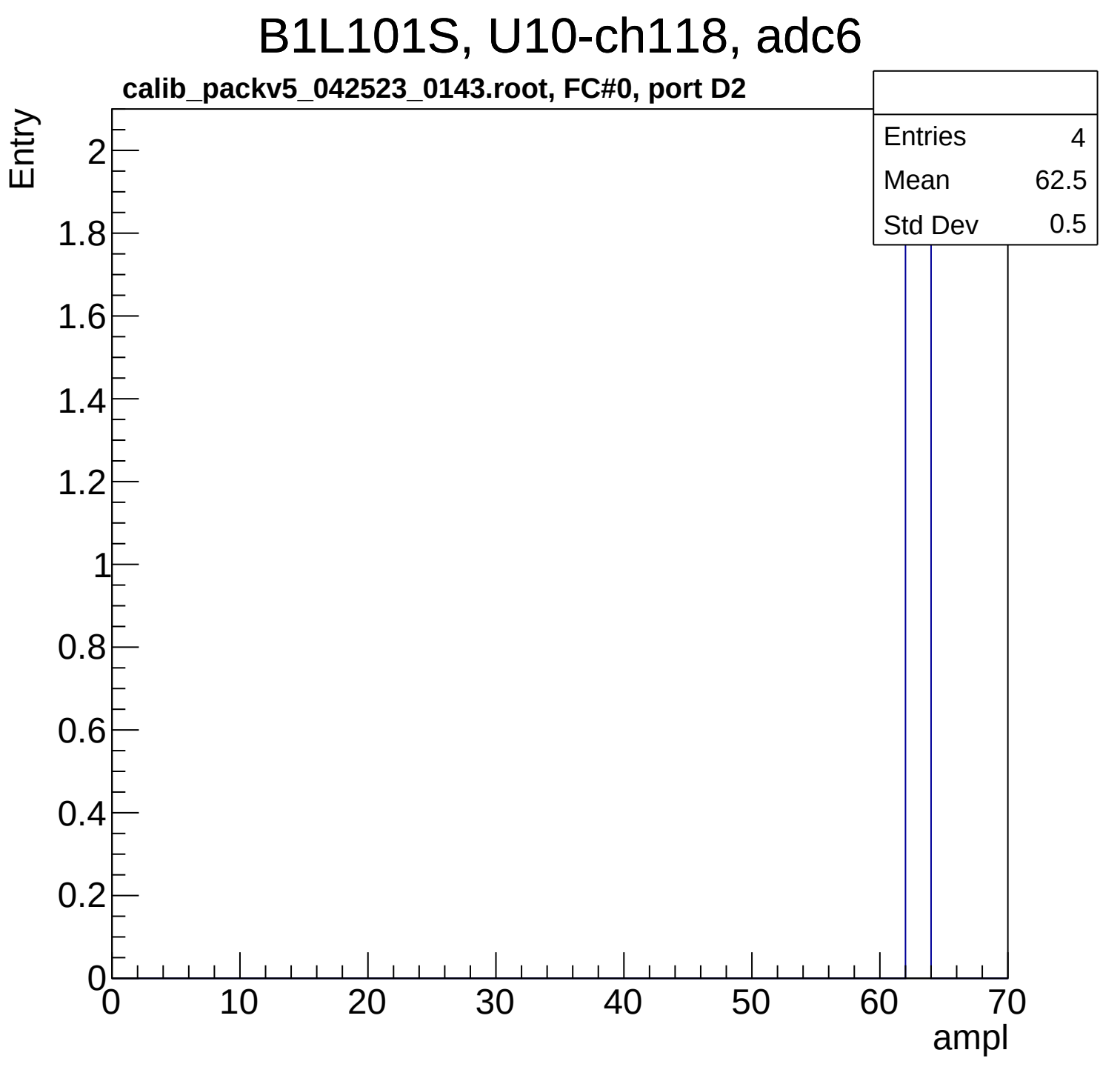
B1L101S, U10-ch118, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 62.5
Std Dev 0.5
Entry
ampl
0
0.2
0.4
0.6
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1.2
1.4
1.6
1.8
2
0
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20
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40
50
60
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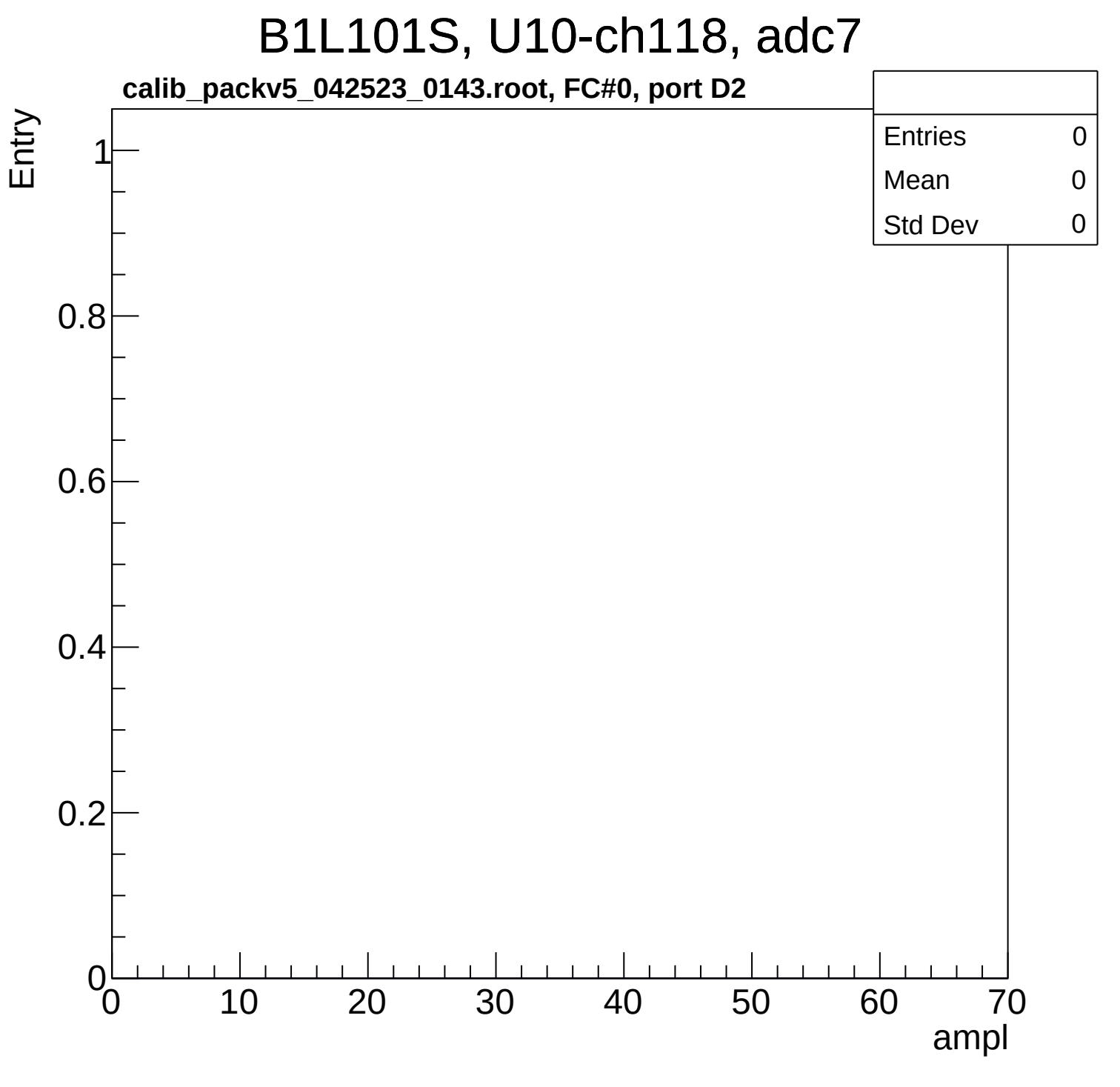
B1L101S, U10-ch118, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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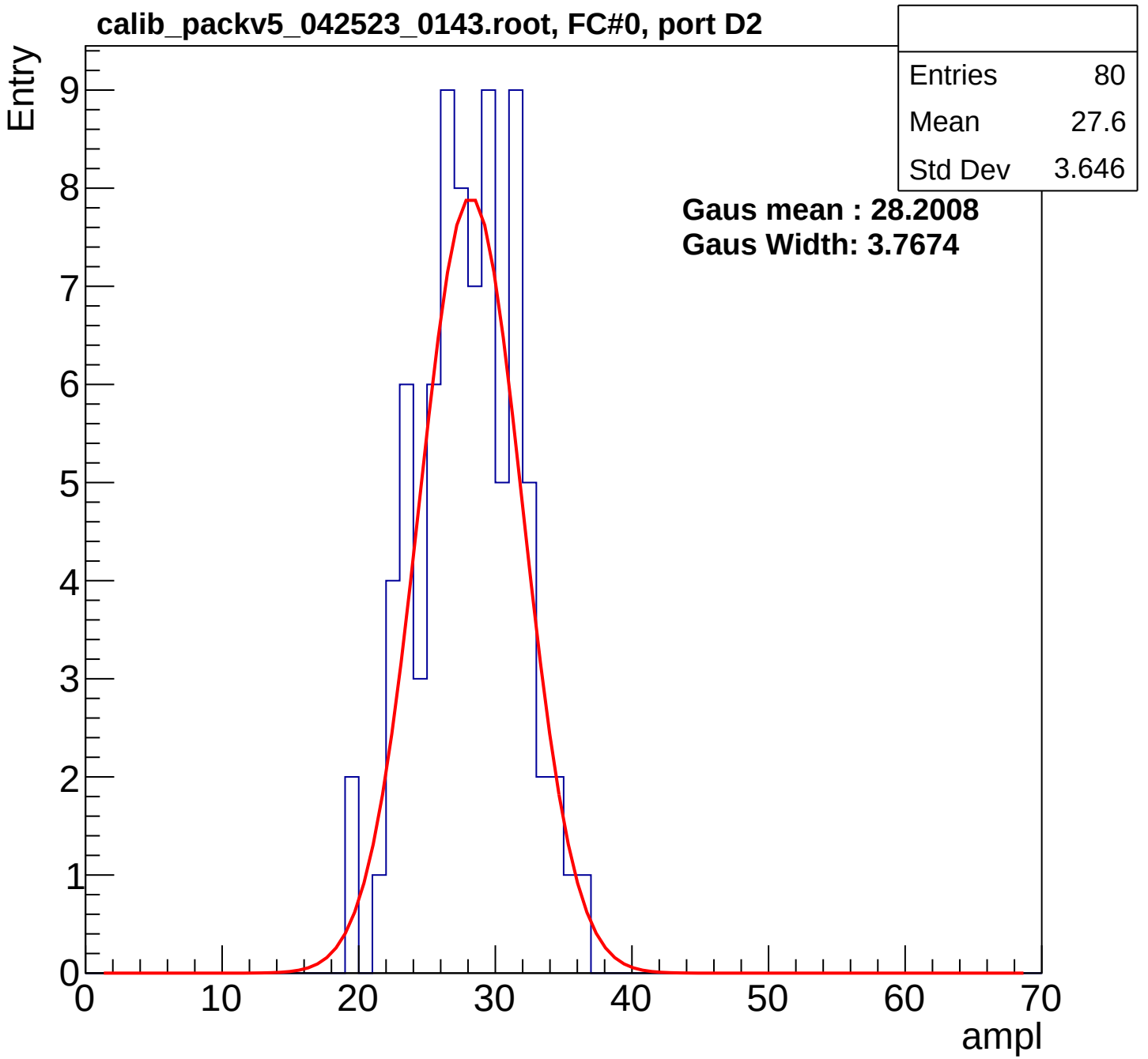
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch119, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 80
Mean 27.6
Std Dev 3.646
Gaus mean : 28.2008
Gaus Width: 3.7674
Entry
ampl
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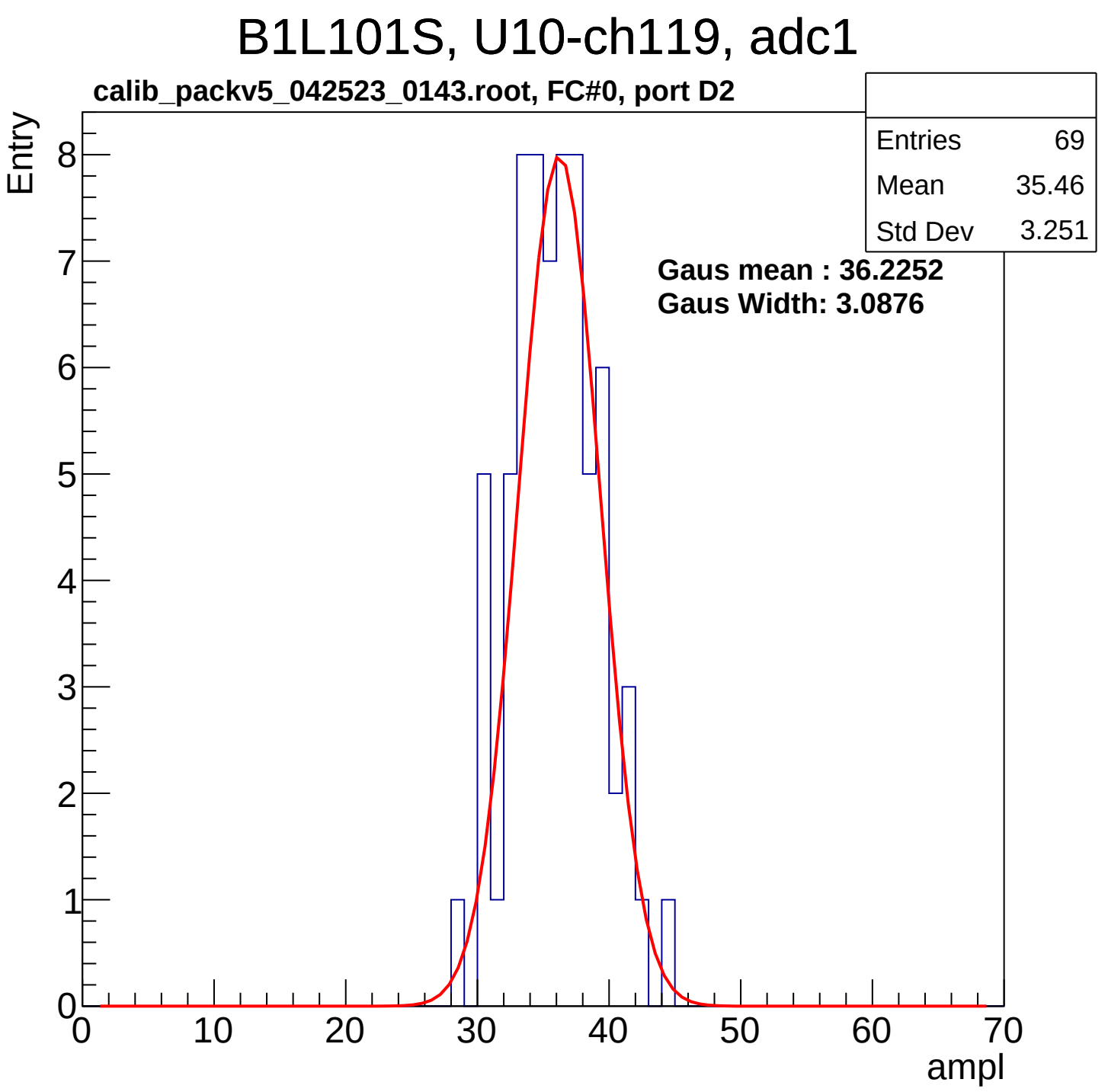
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch119, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 35.46
Std Dev 3.251
Gaus mean : 36.2252
Gaus Width: 3.0876
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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60
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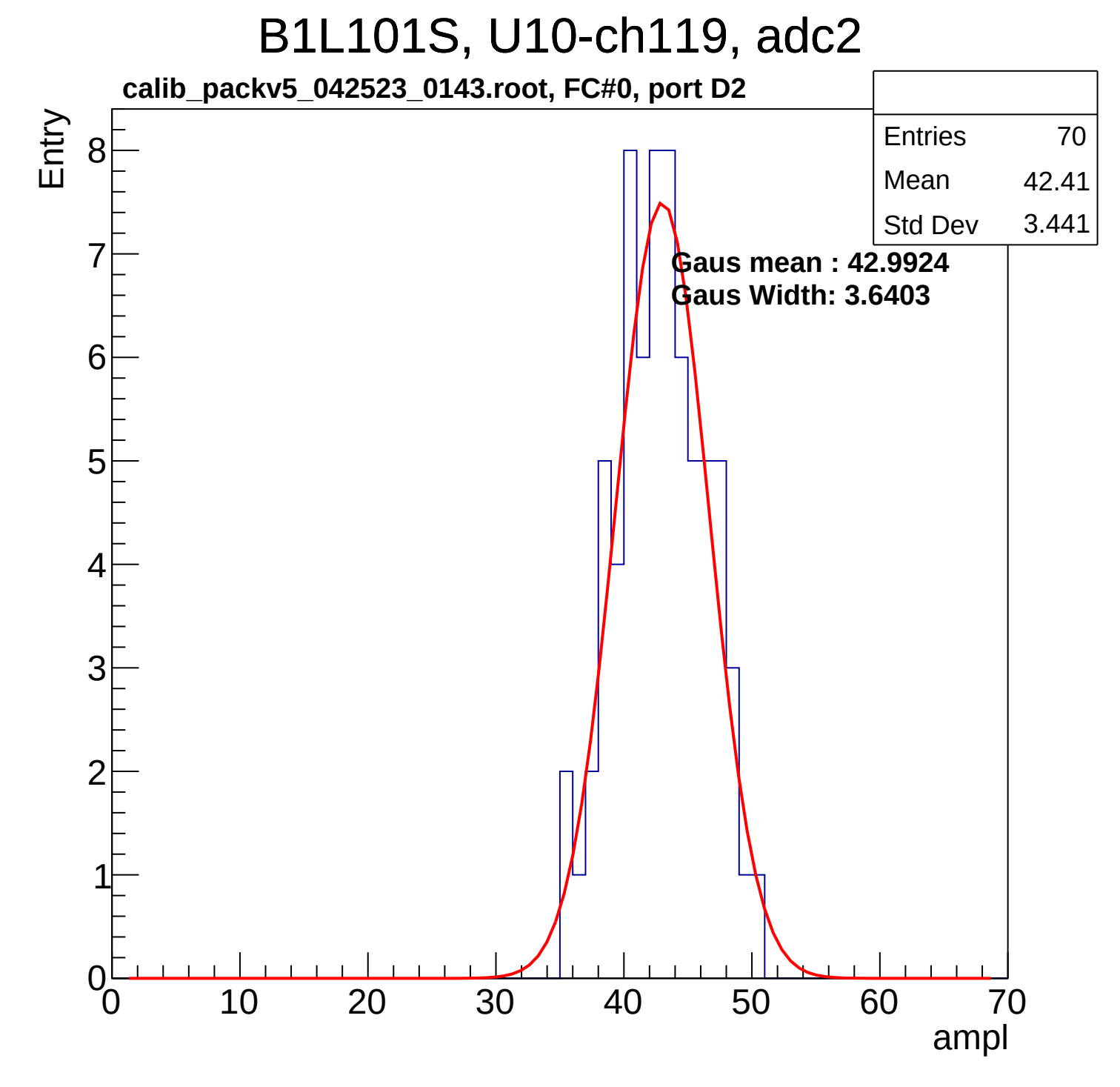
B1L101S, U10-ch119, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 42.41
Std Dev 3.441
Gaus mean : 42.9924
Gaus Width: 3.6403
Entry
ampl
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1
2
3
4
5
6
7
8
0
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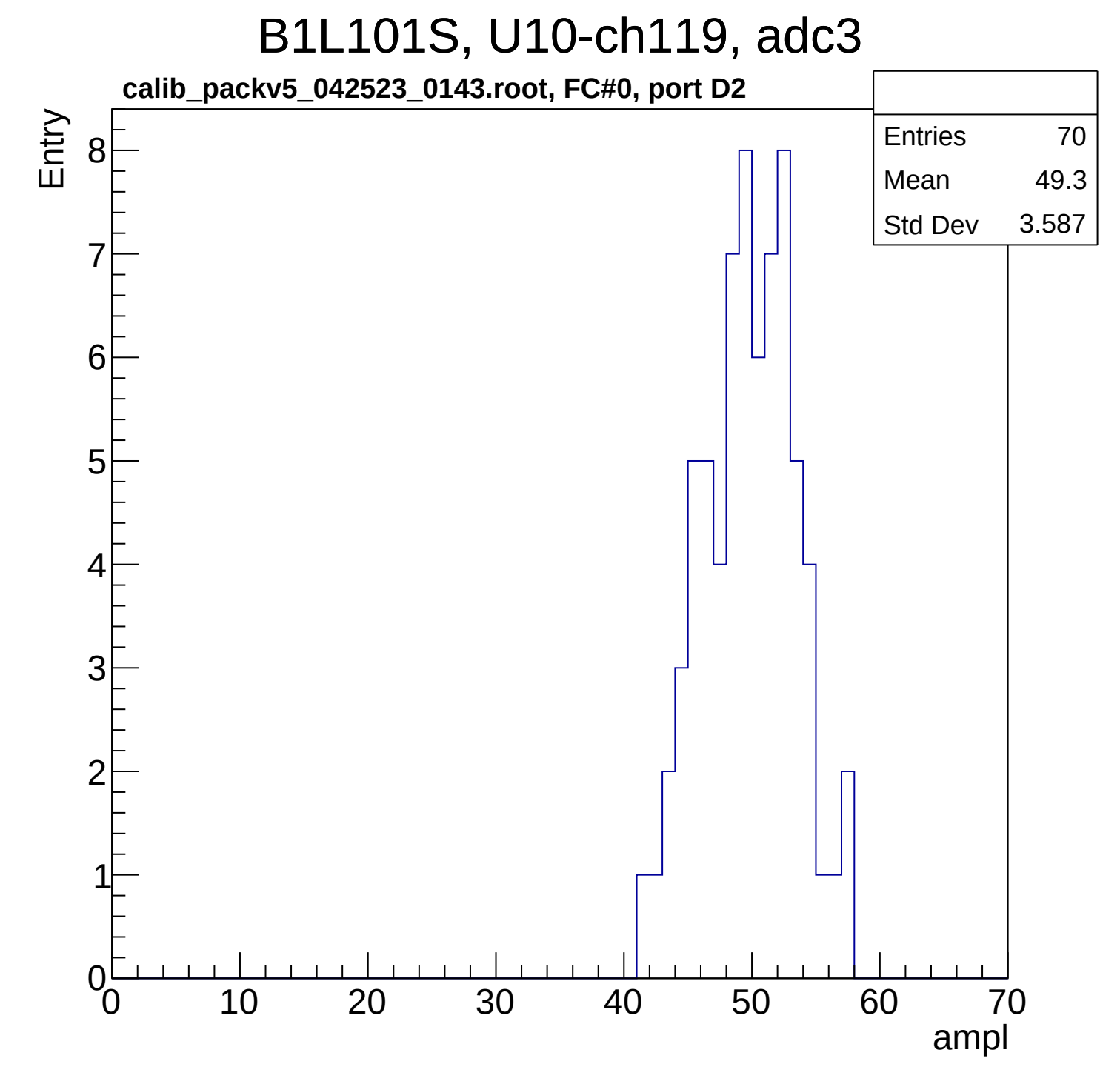
B1L101S, U10-ch119, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 49.3
Std Dev 3.587
Entry
ampl
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3
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10
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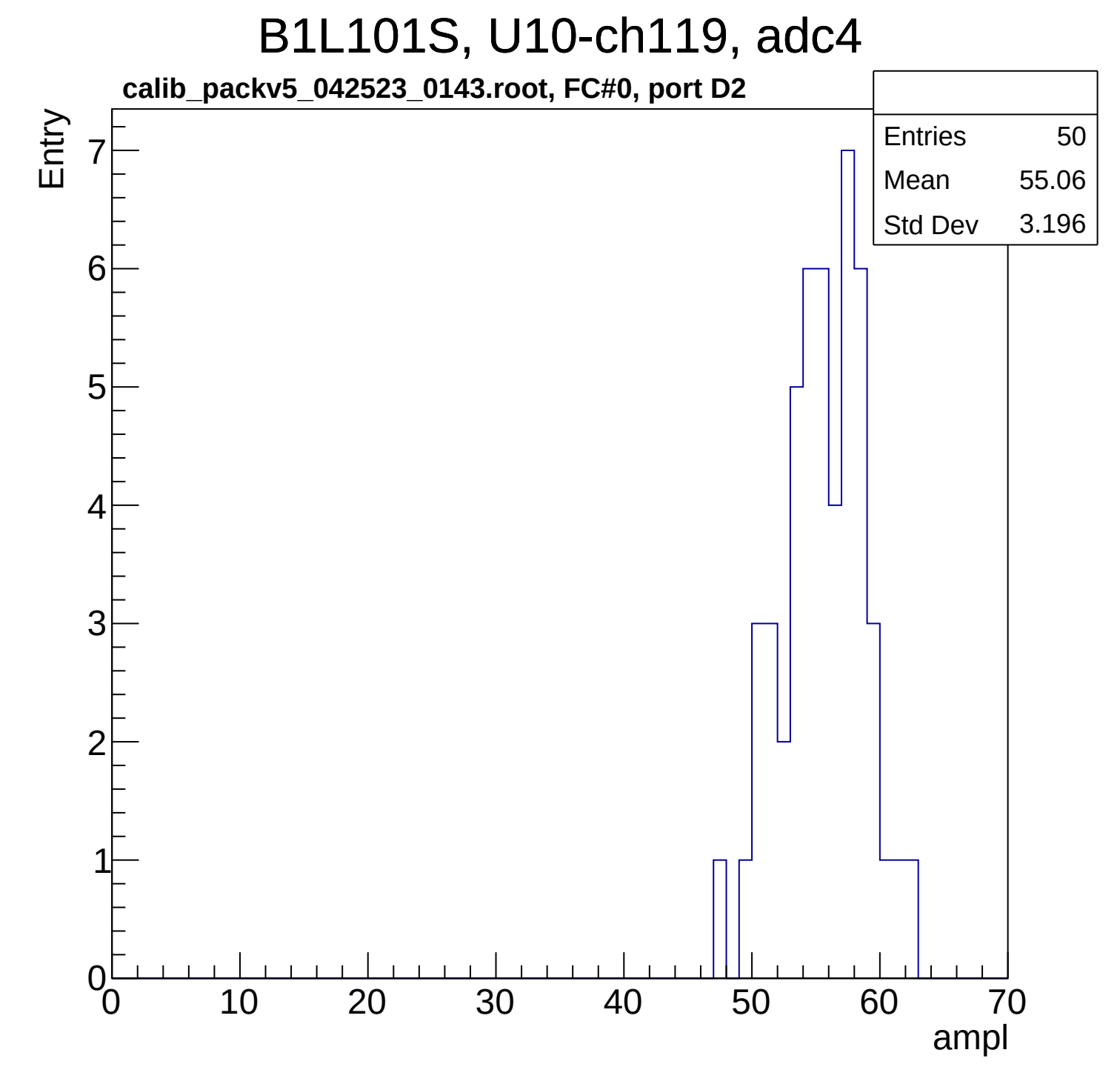
70


B1L101S, U10-ch119, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 55.06
Std Dev 3.196
Entry
ampl
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2
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4
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0
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60
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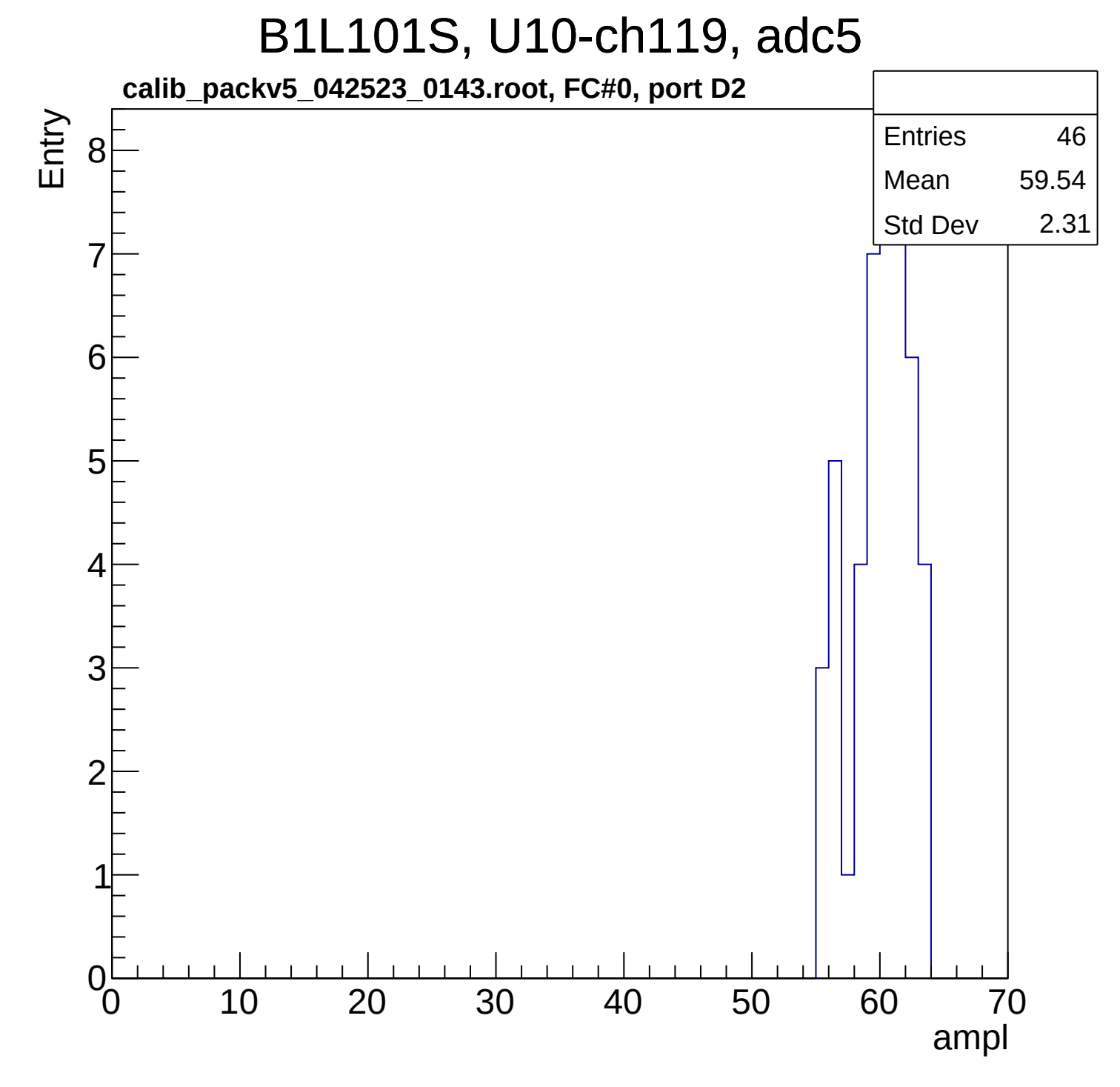
B1L101S, U10-ch119, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 59.54
Std Dev 2.31
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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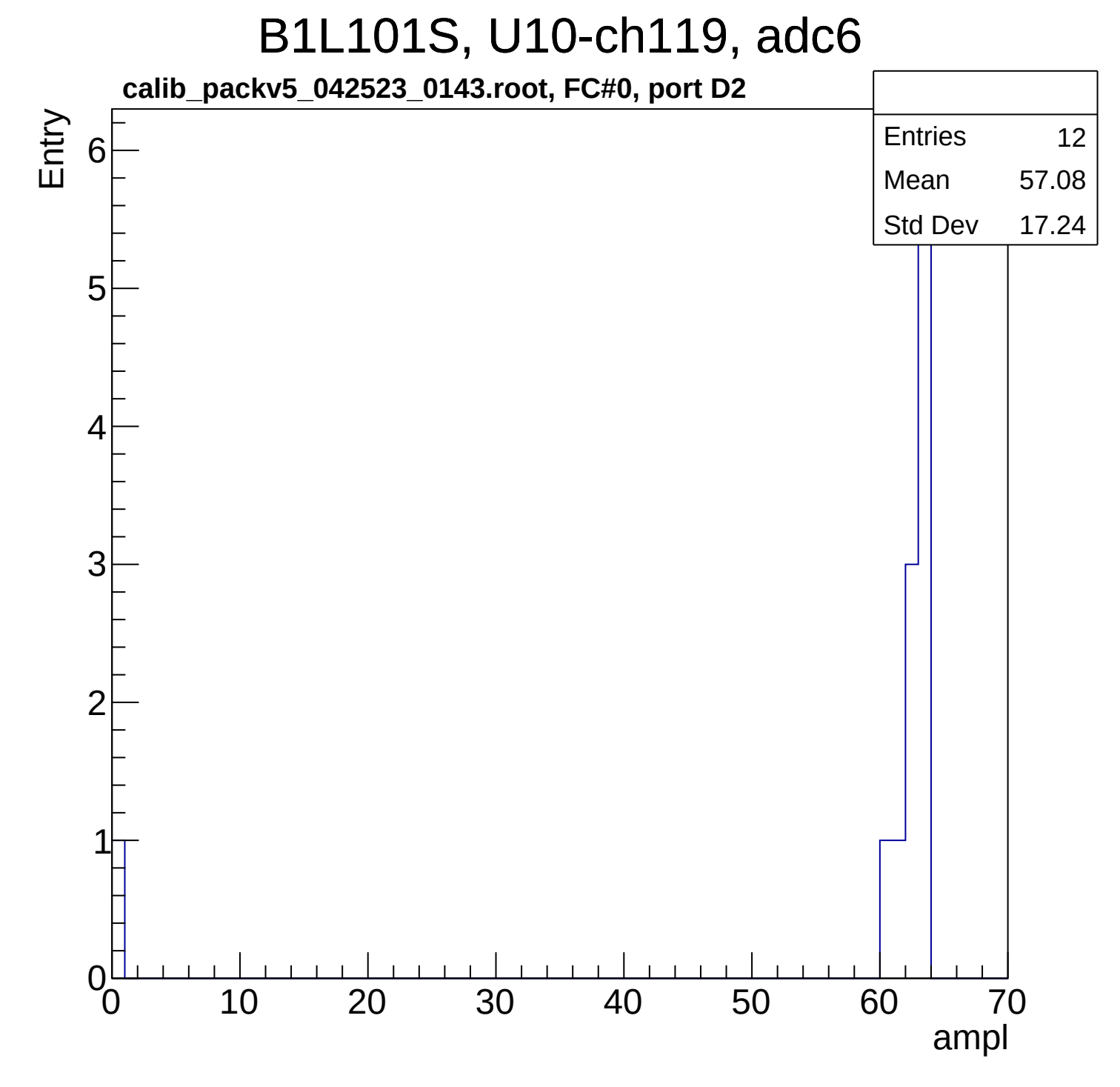
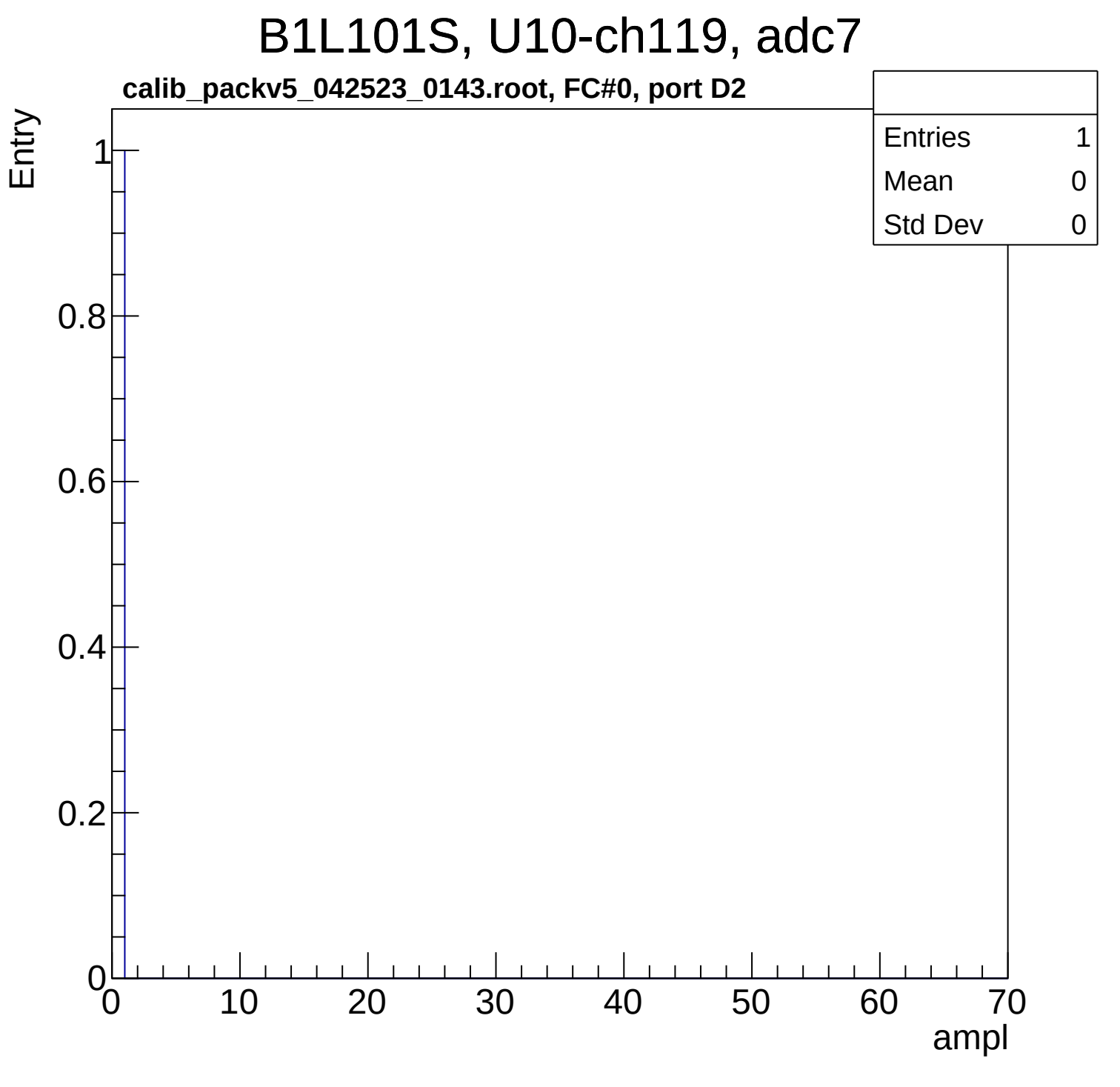
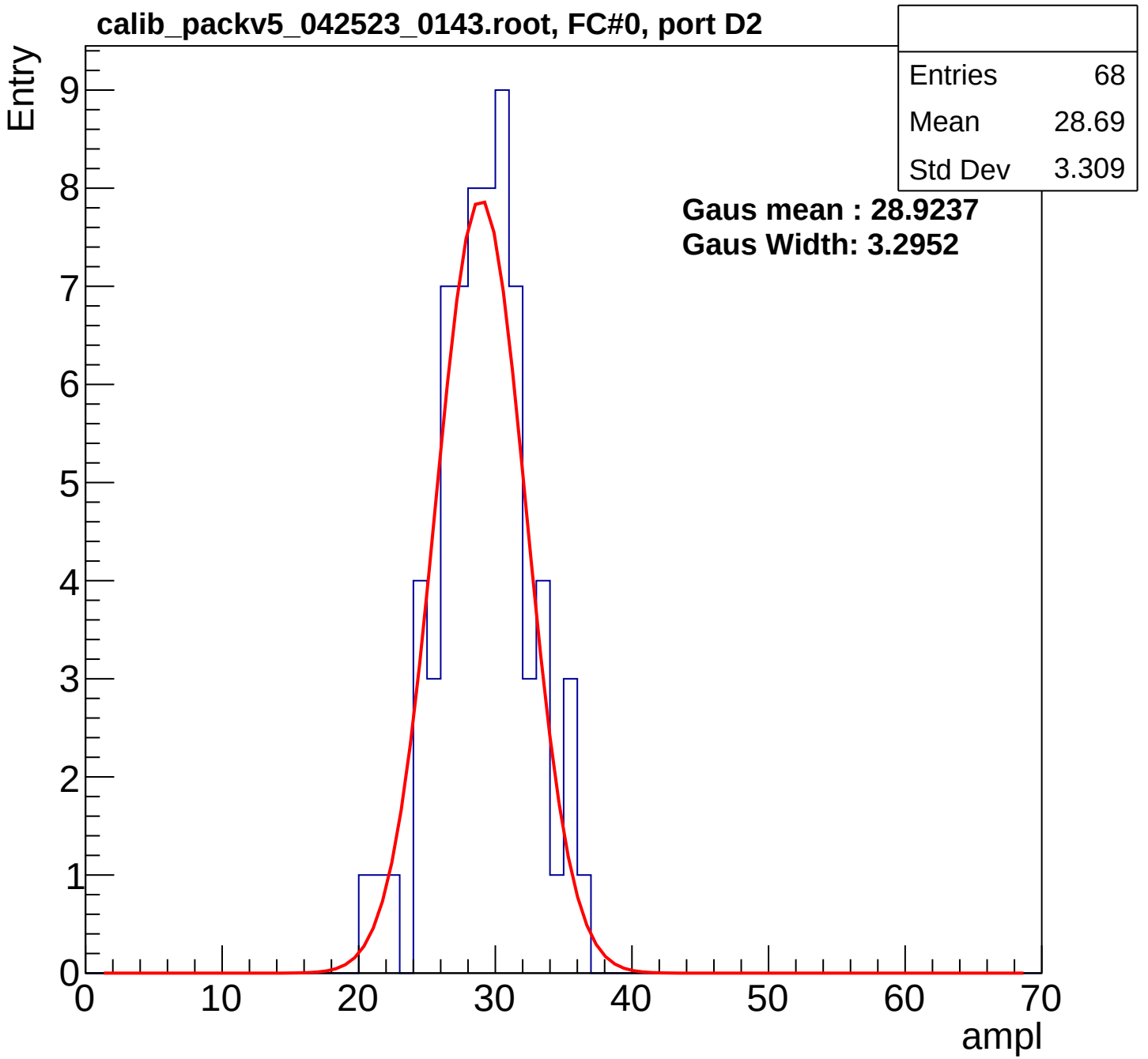

B1L101S, U10-ch119, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 12
Mean 57.08
Std Dev 17.24
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch119, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch120, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 28.69
Std Dev 3.309
Gaus mean : 28.9237
Gaus Width: 3.2952
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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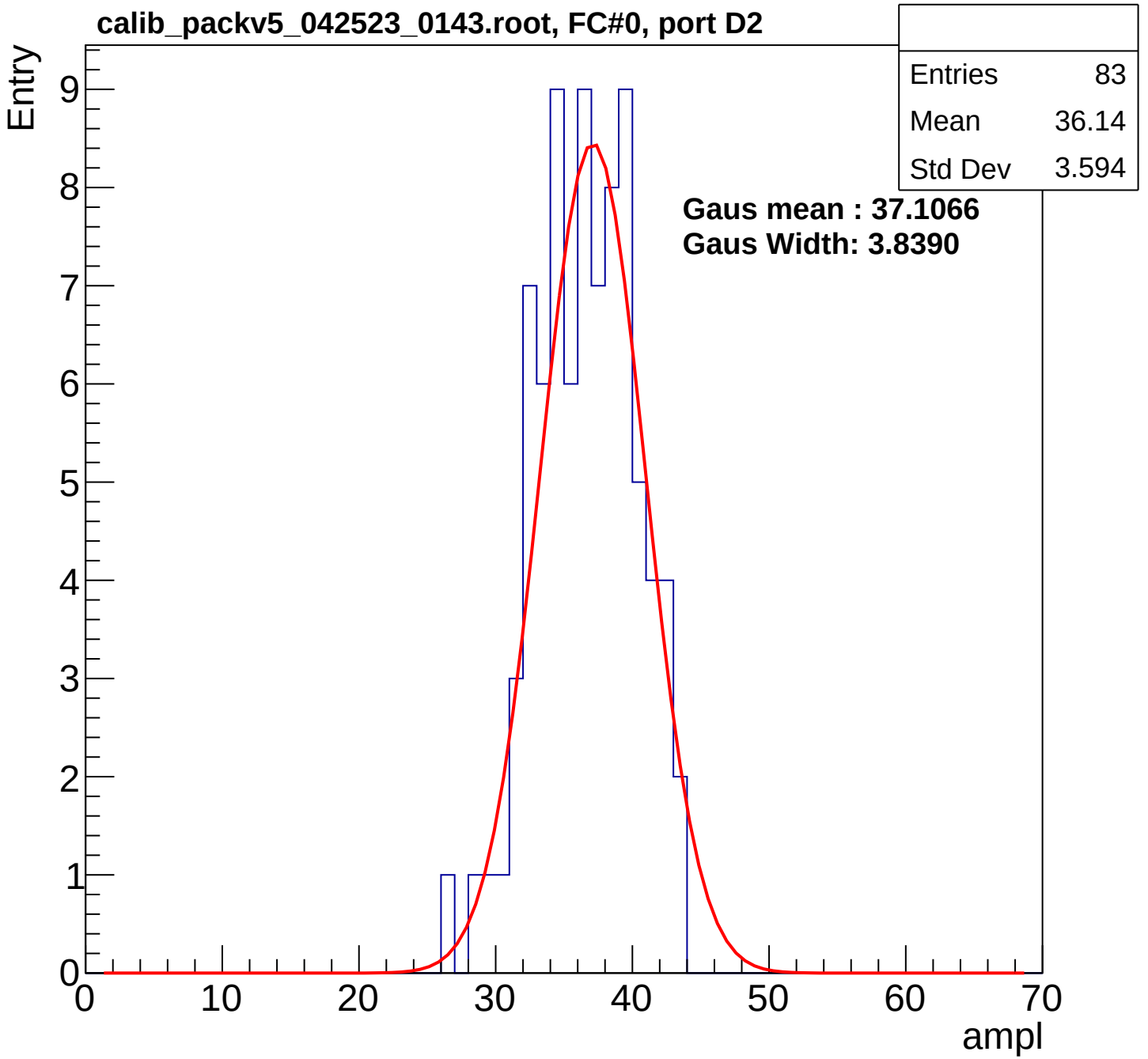
B1L101S, U10-ch120, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 83
Mean 36.14
Std Dev 3.594
Gaus mean : 37.1066
Gaus Width: 3.8390
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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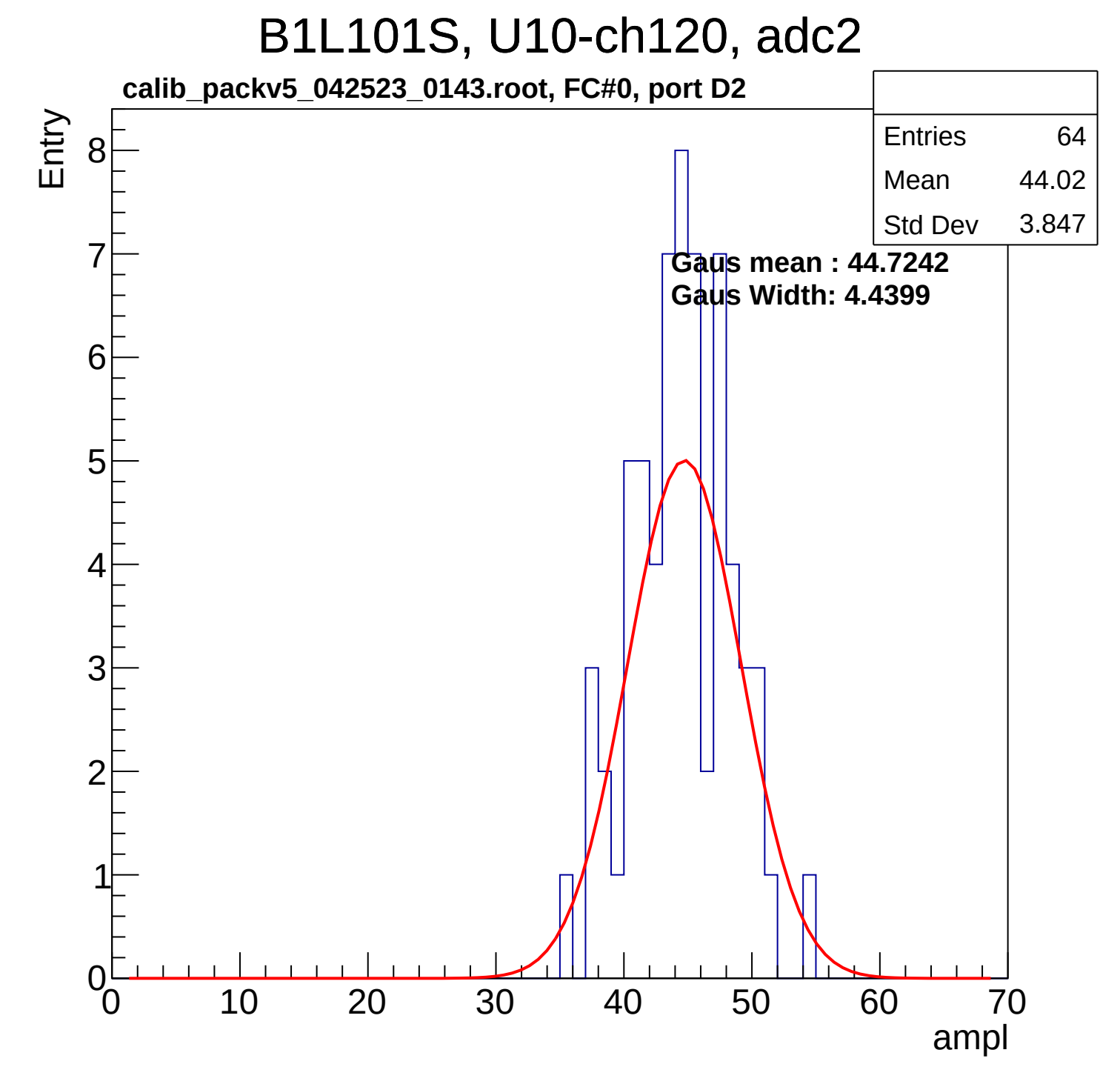
B1L101S, U10-ch120, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 44.02
Std Dev 3.847
Gaus mean : 44.7242
Gaus Width: 4.4399
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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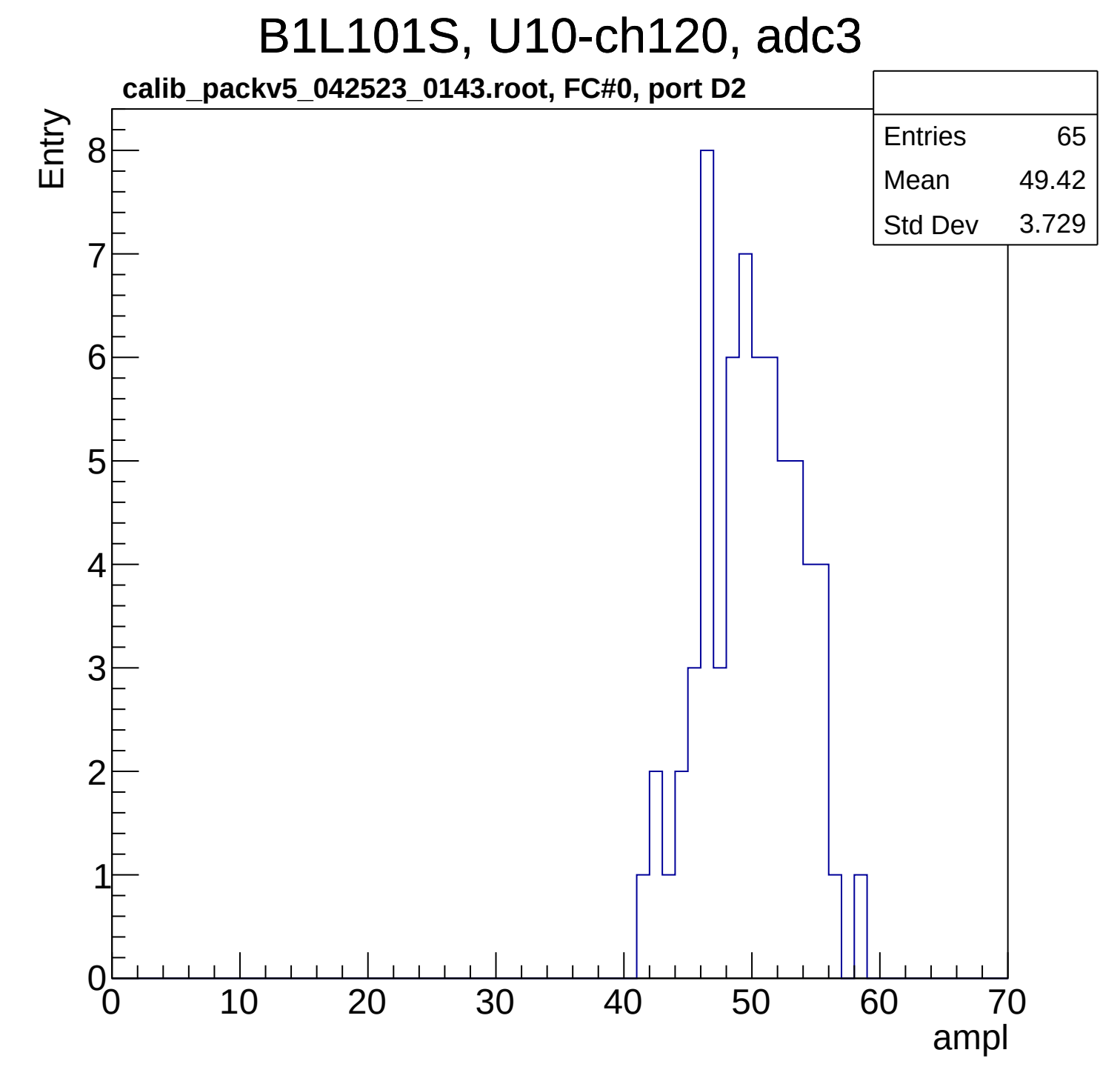
B1L101S, U10-ch120, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 49.42
Std Dev 3.729
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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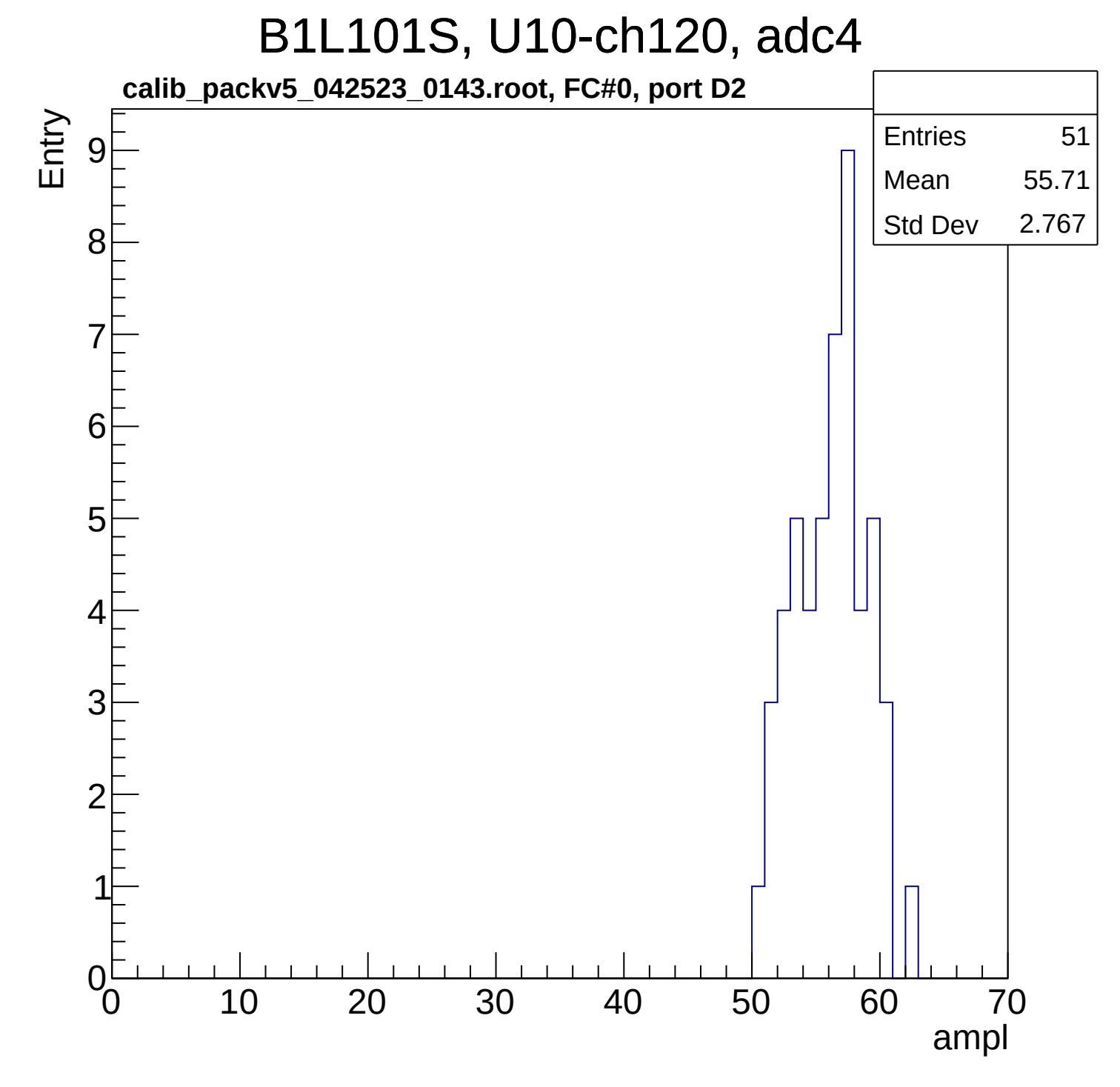
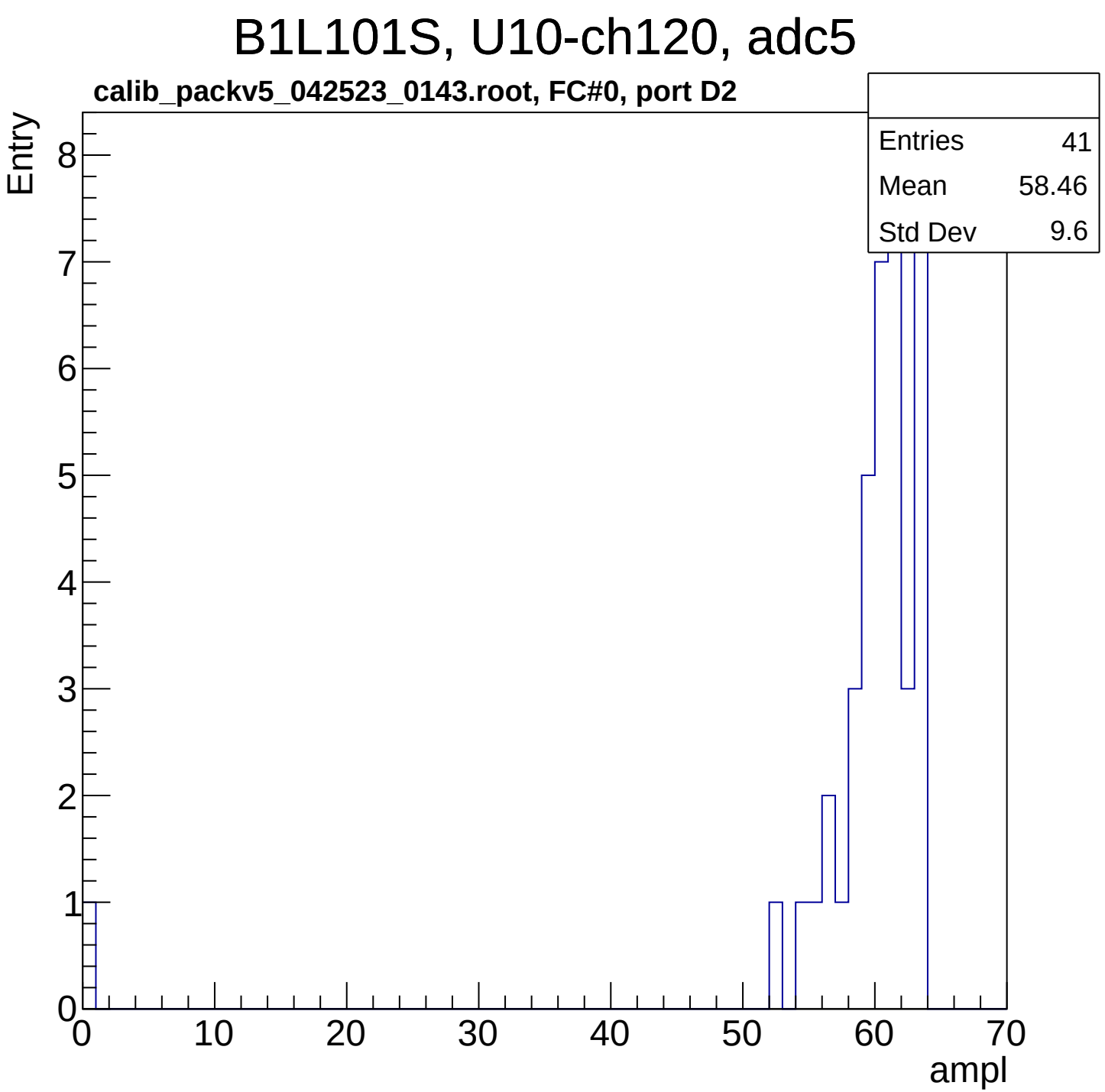

B1L101S, U10-ch120, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 55.71
Std Dev 2.767
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch120, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 41
Mean 58.46
Std Dev 9.6
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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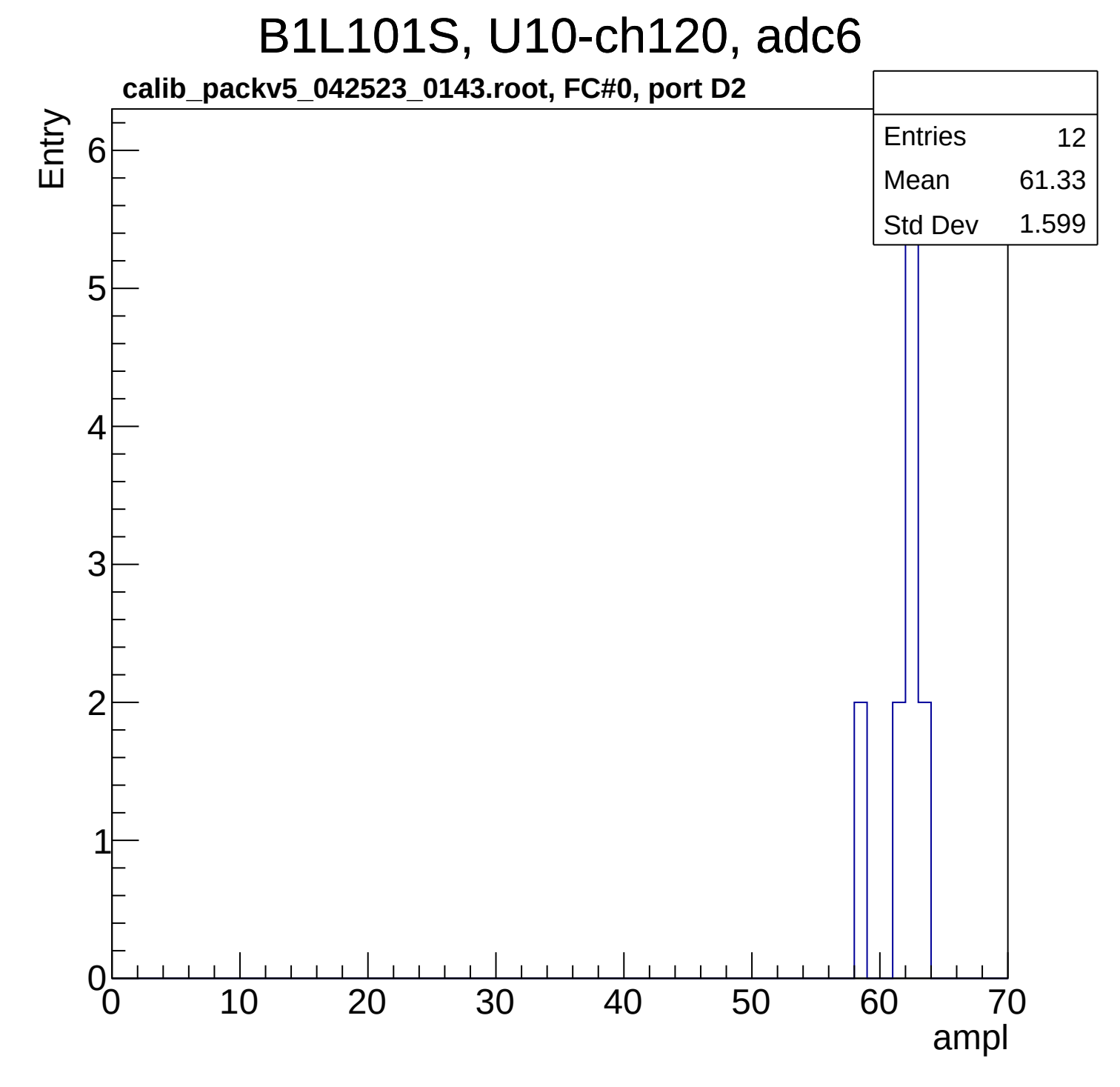
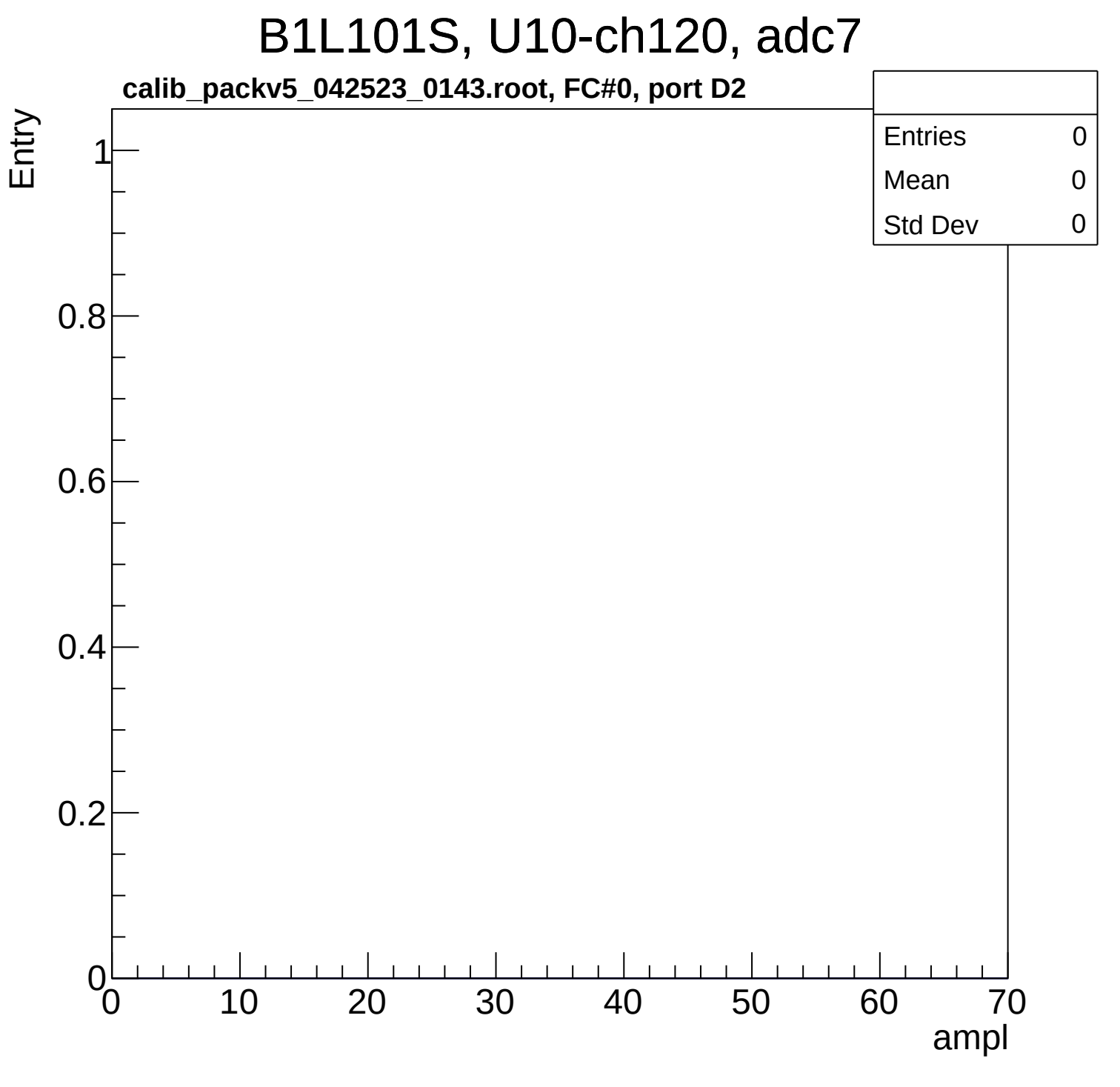
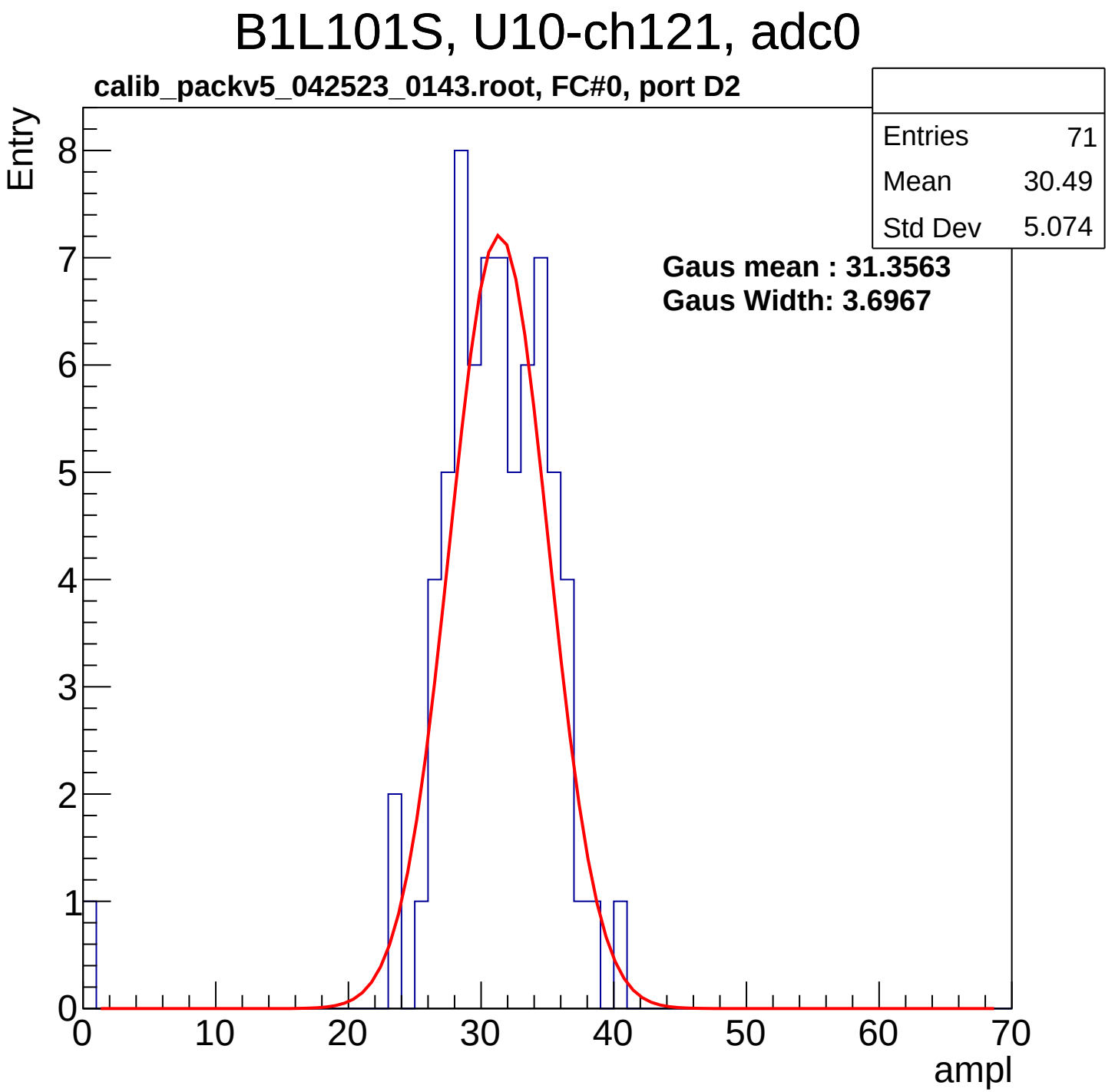
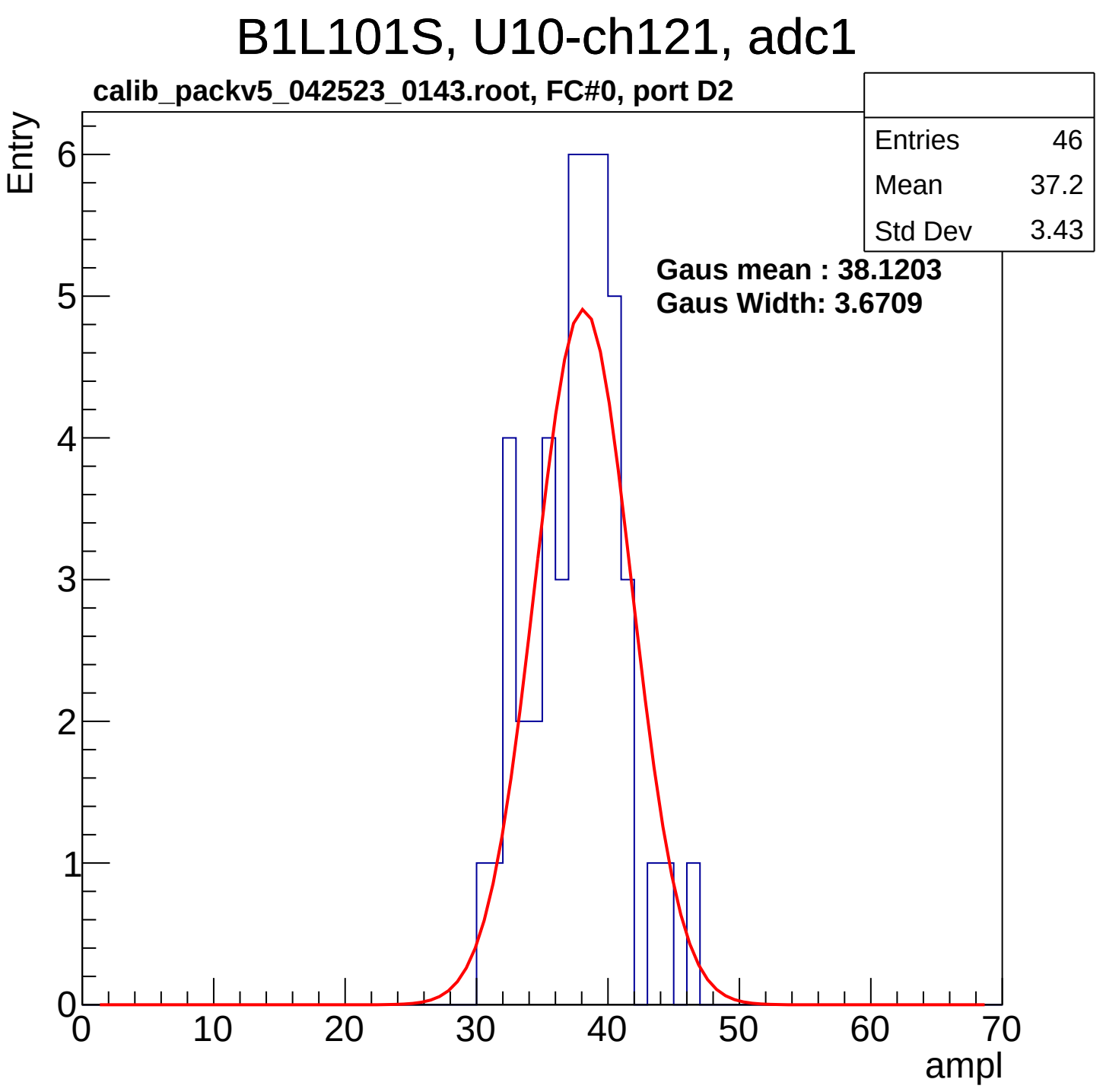

B1L101S, U10-ch120, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 12
Mean 61.33
Std Dev 1.599
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L101S, U10-ch120, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch121, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 30.49
Std Dev 5.074
Gaus mean : 31.3563
Gaus Width: 3.6967
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch121, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 37.2
Std Dev 3.43
Gaus mean : 38.1203
Gaus Width: 3.6709
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
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60
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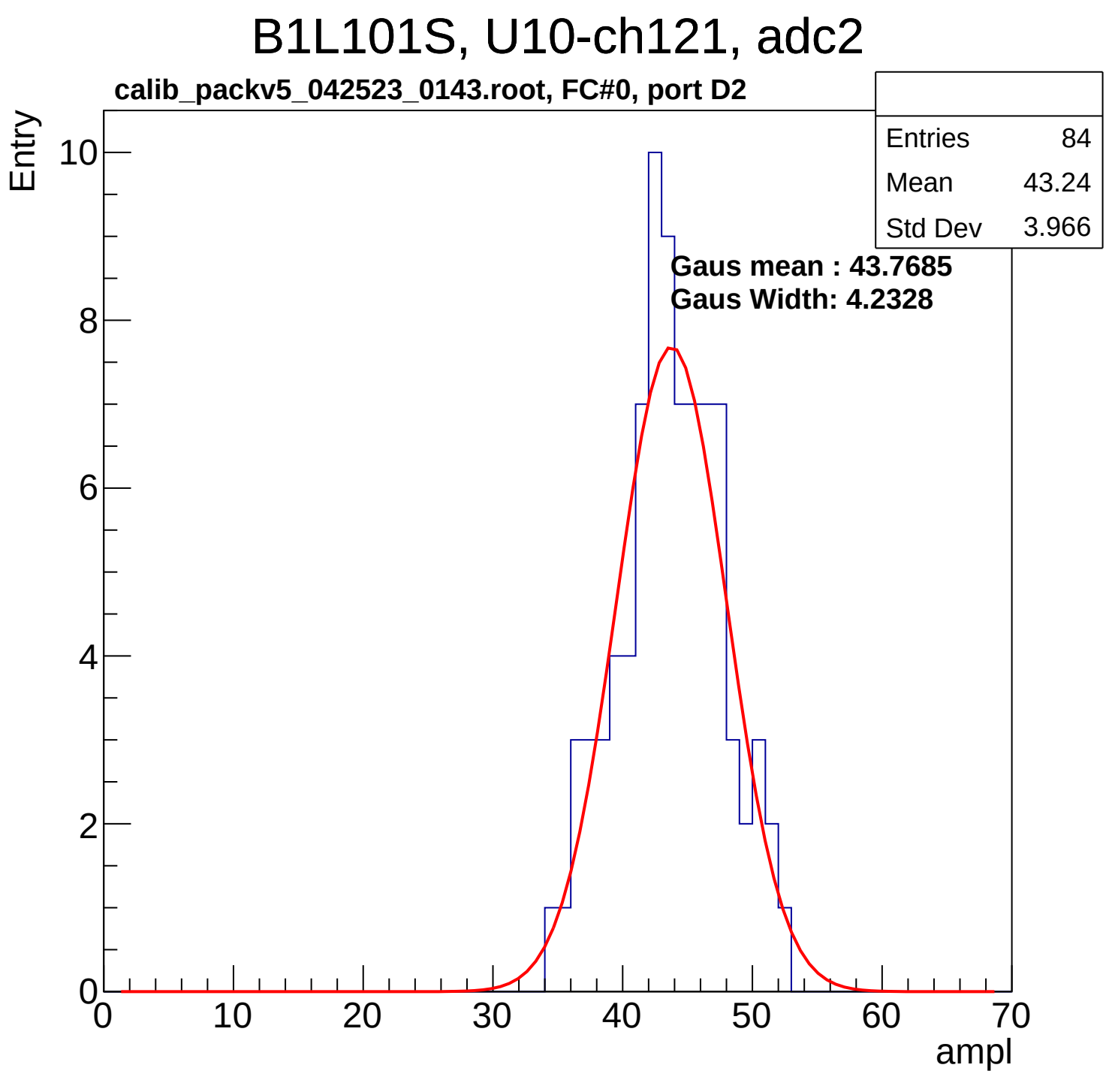
B1L101S, U10-ch121, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 84
Mean 43.24
Std Dev 3.966
Gaus mean : 43.7685
Gaus Width: 4.2328
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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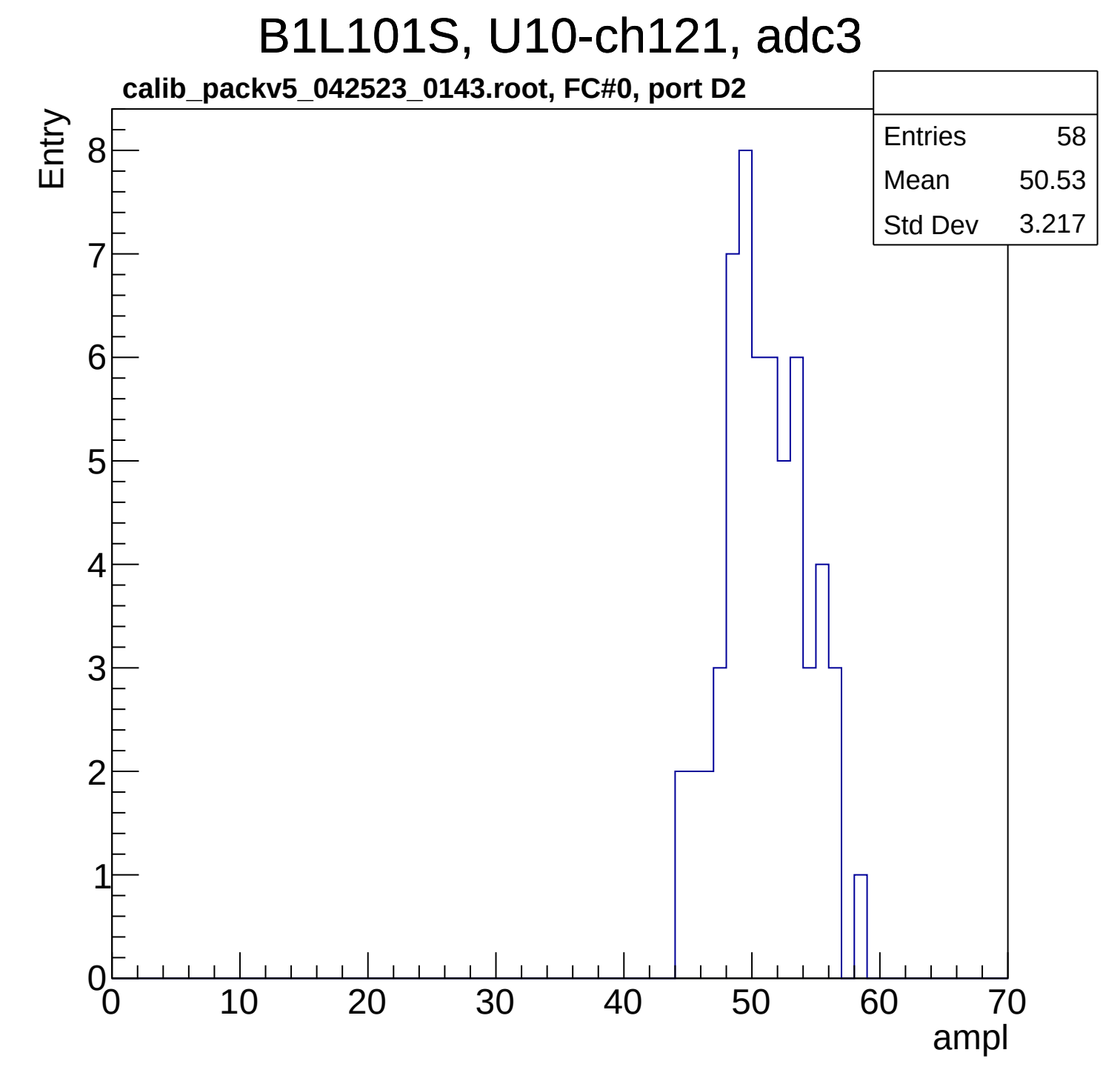
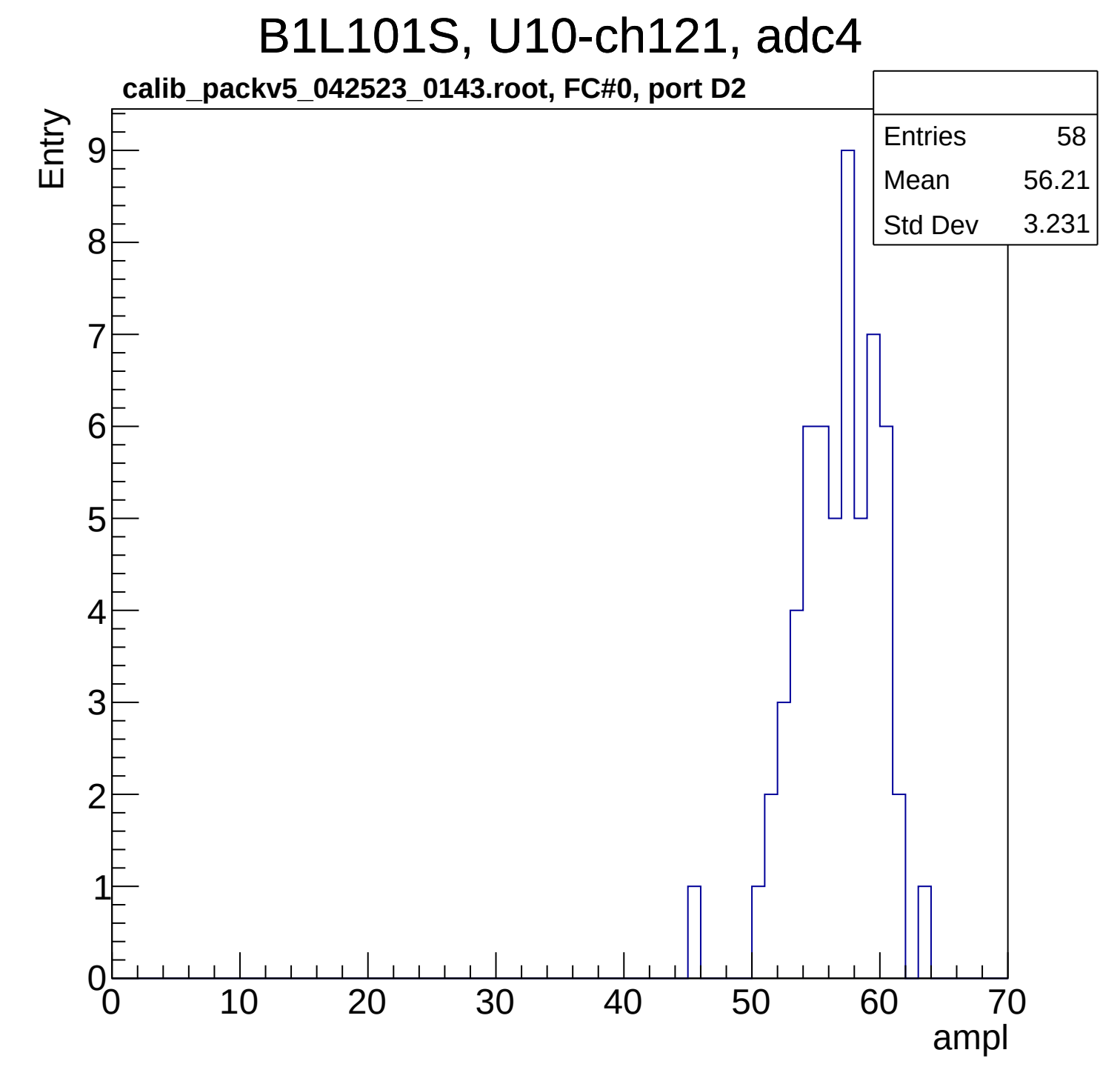

B1L101S, U10-ch121, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 50.53
Std Dev 3.217
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch121, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 56.21
Std Dev 3.231
Entry
ampl
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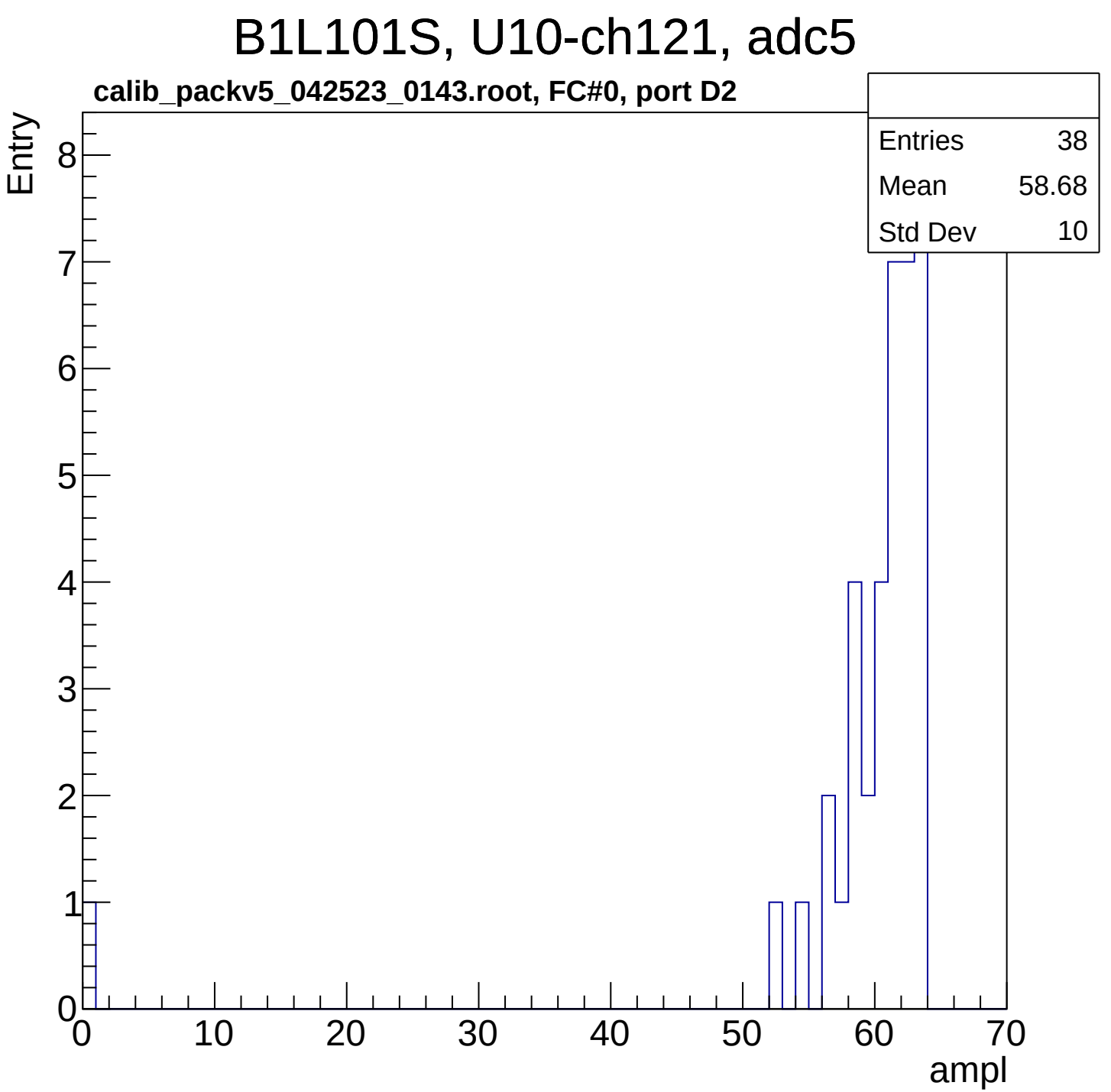
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch121, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 38
Mean 58.68
Std Dev 10
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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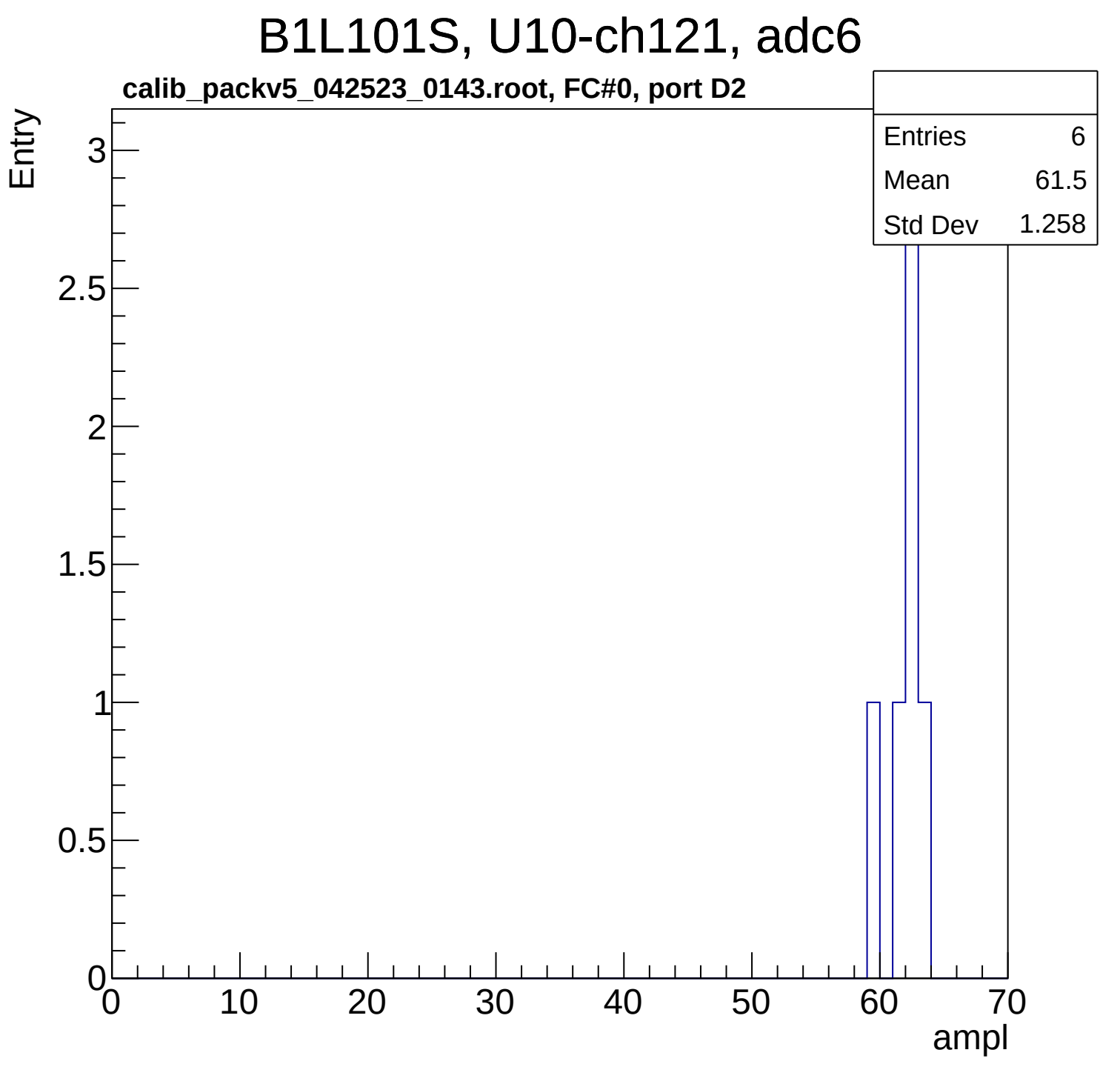
B1L101S, U10-ch121, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 61.5
Std Dev 1.258
Entry
ampl
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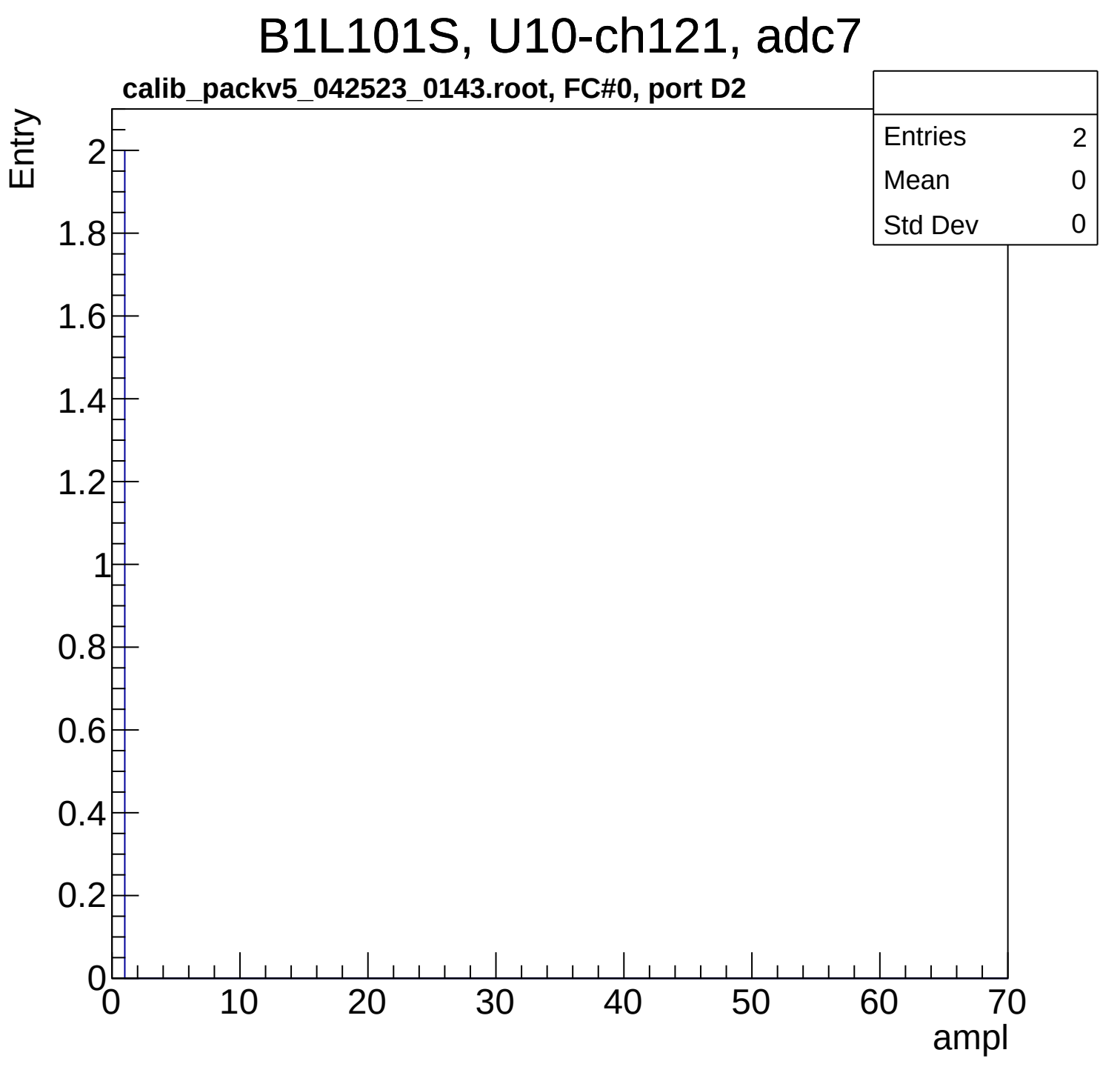
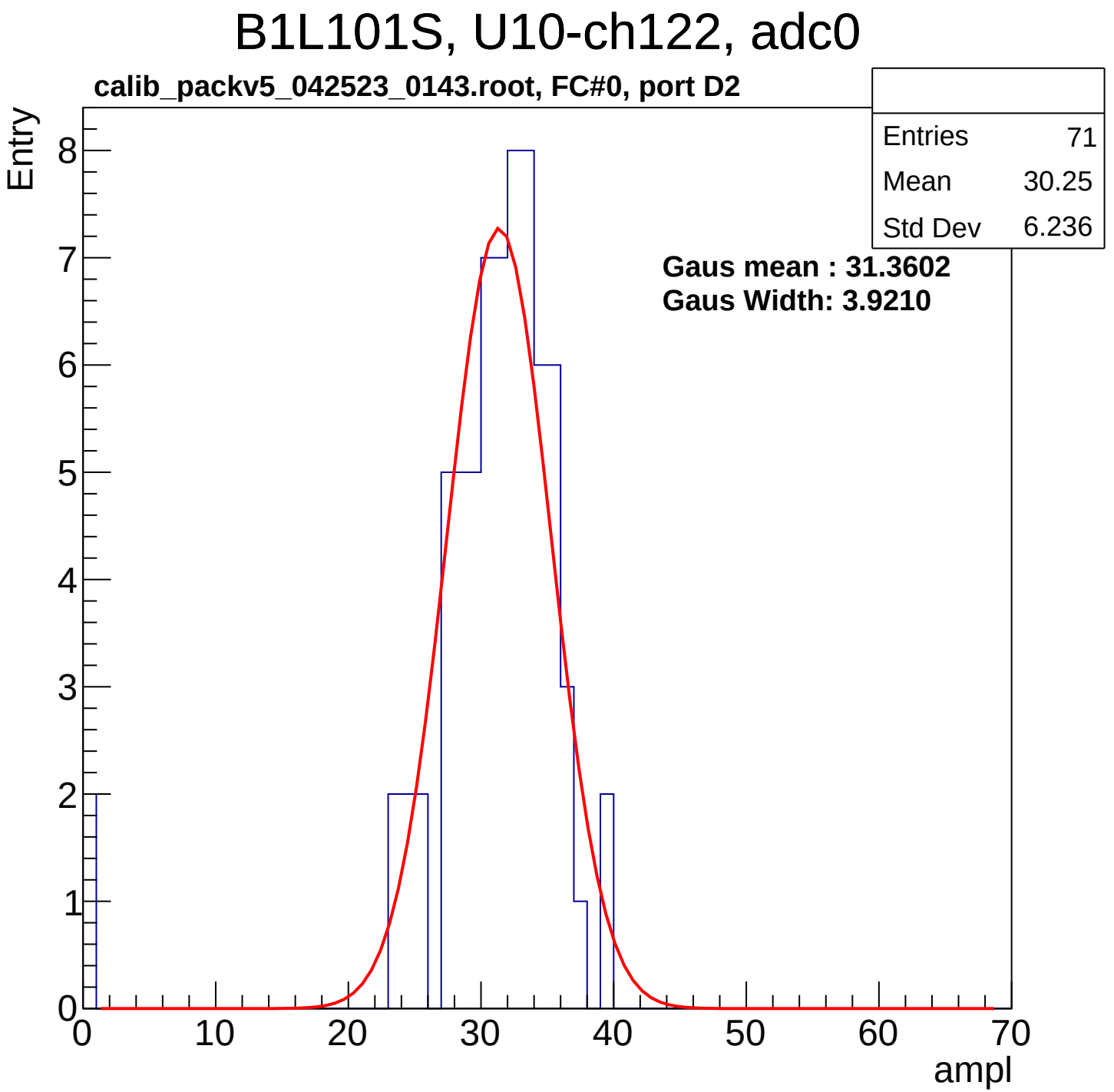
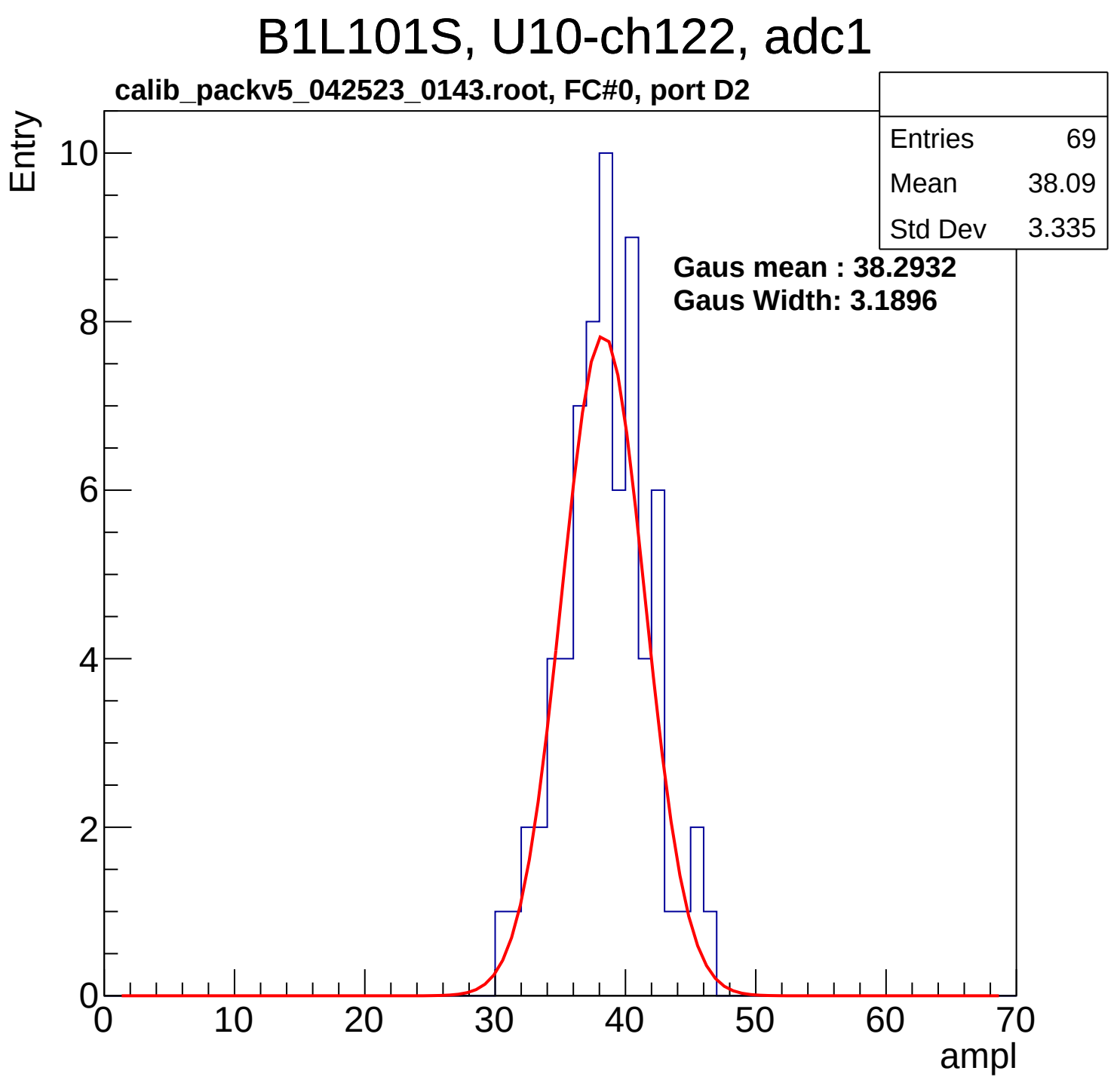
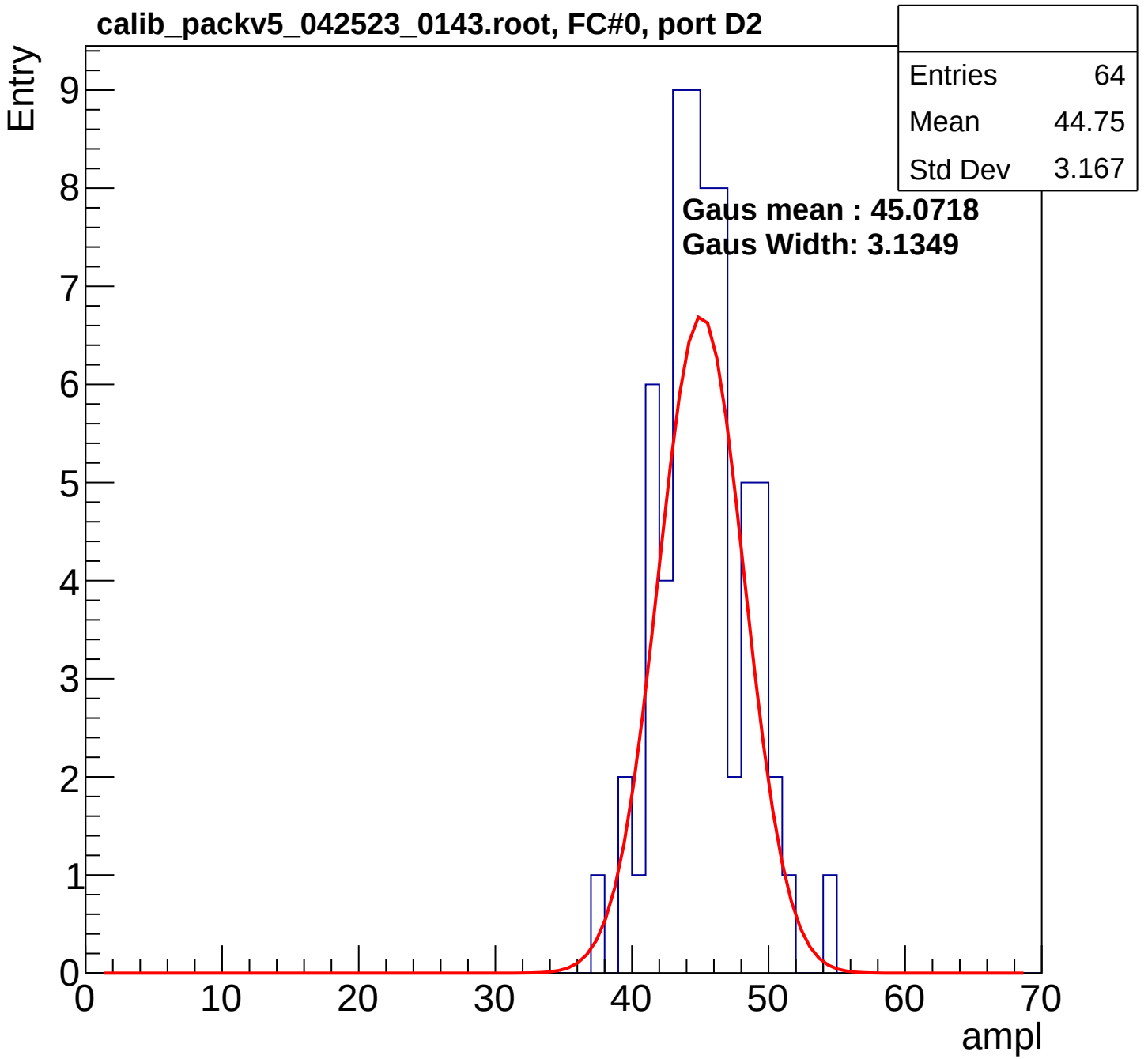
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U10-ch121, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch122, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 30.25
Std Dev 6.236
Gaus mean : 31.3602
Gaus Width: 3.9210
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch122, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 38.09
Std Dev 3.335
Gaus mean : 38.2932
Gaus Width: 3.1896
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch122, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 44.75
Std Dev 3.167
Gaus mean : 45.0718
Gaus Width: 3.1349
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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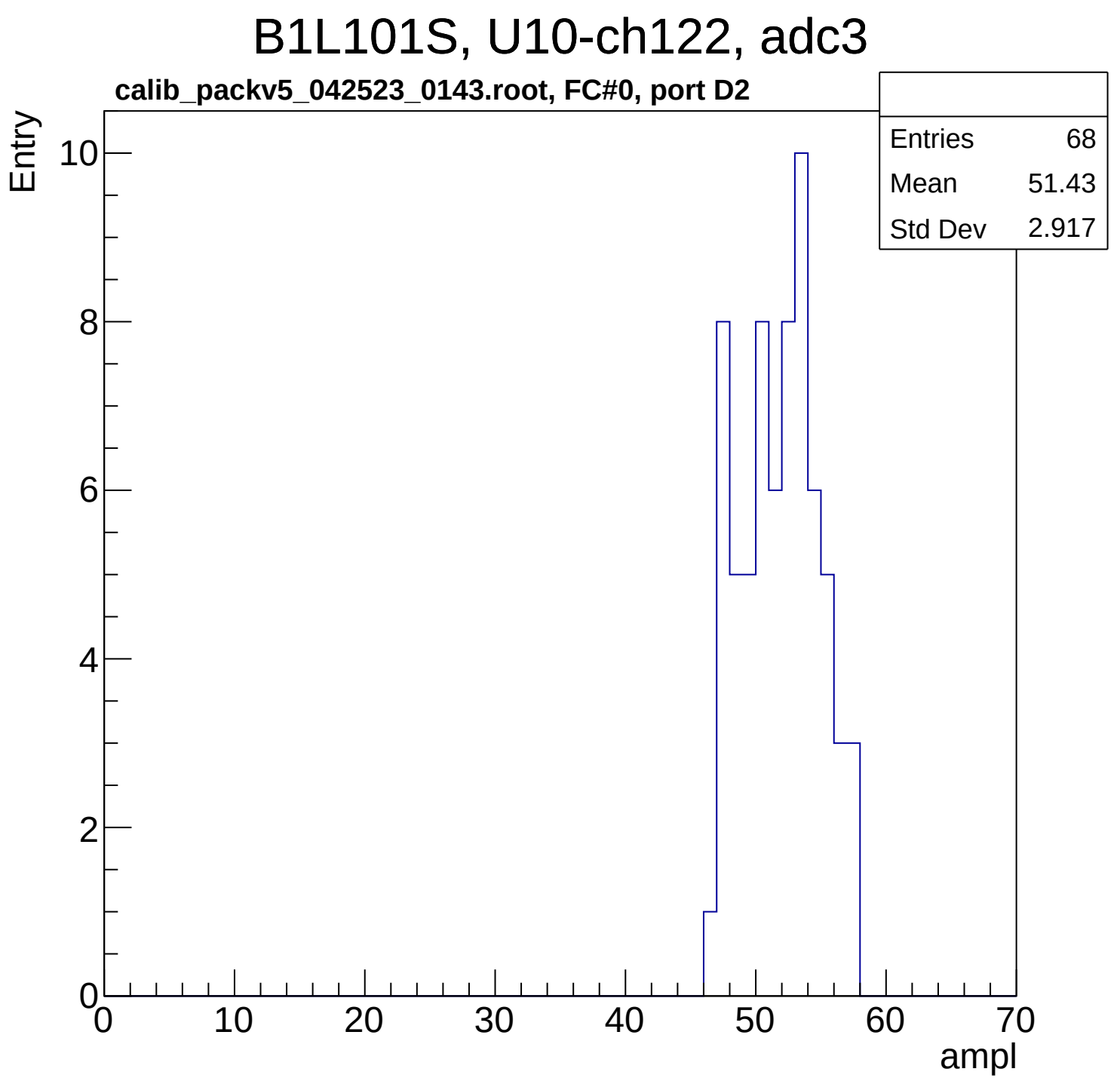
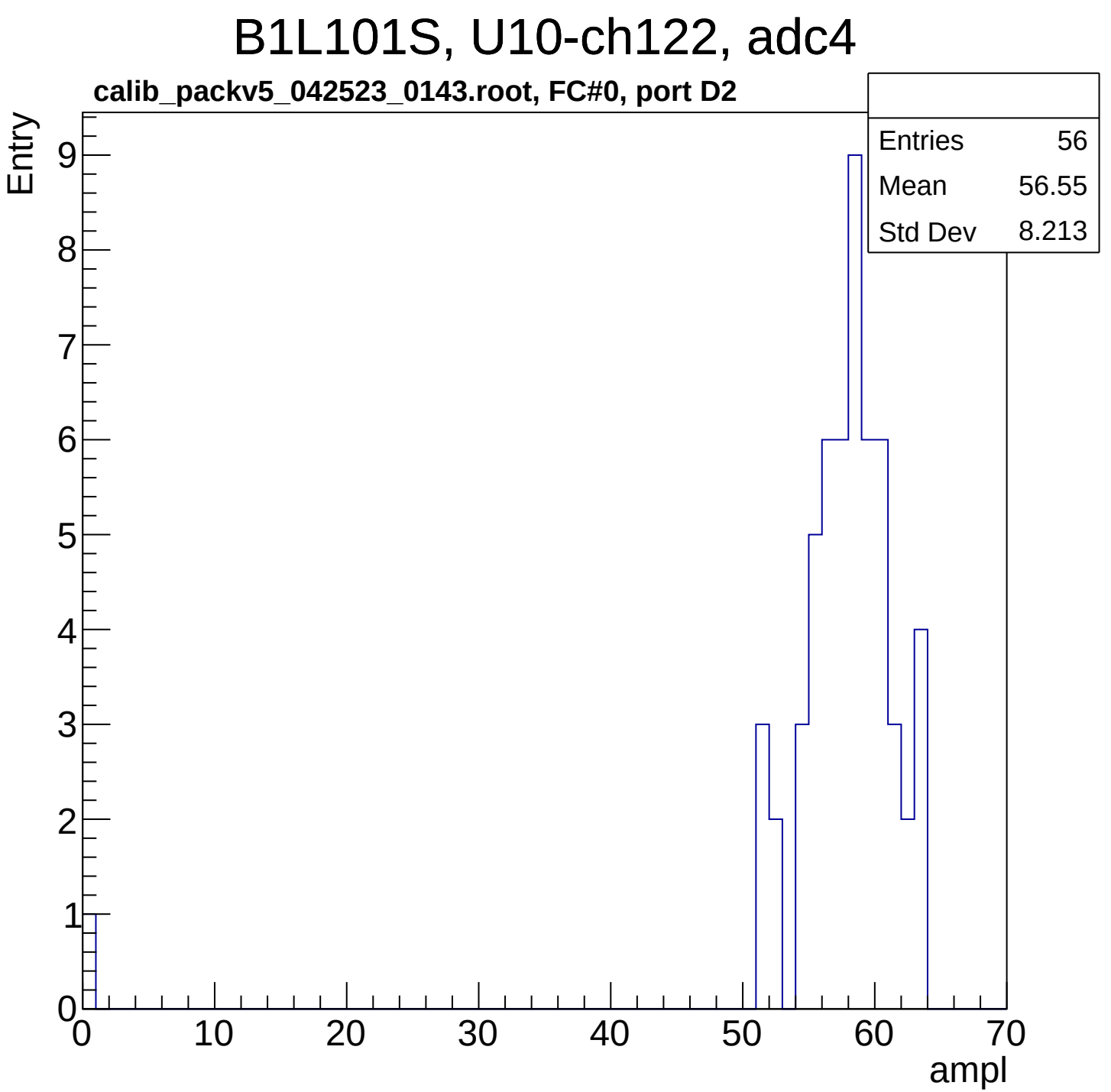

B1L101S, U10-ch122, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 51.43
Std Dev 2.917
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch122, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 56.55
Std Dev 8.213
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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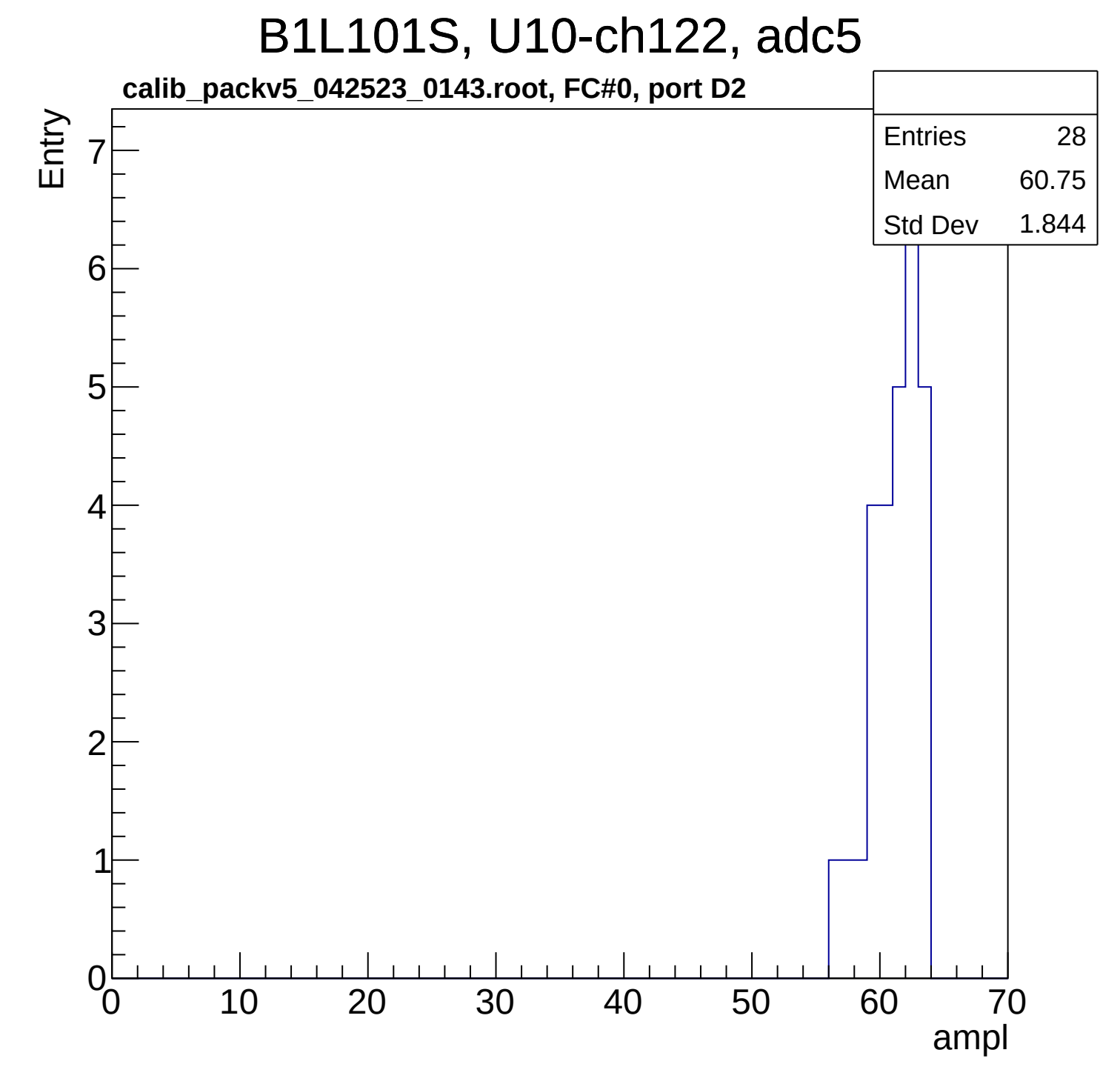
B1L101S, U10-ch122, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 28
Mean 60.75
Std Dev 1.844
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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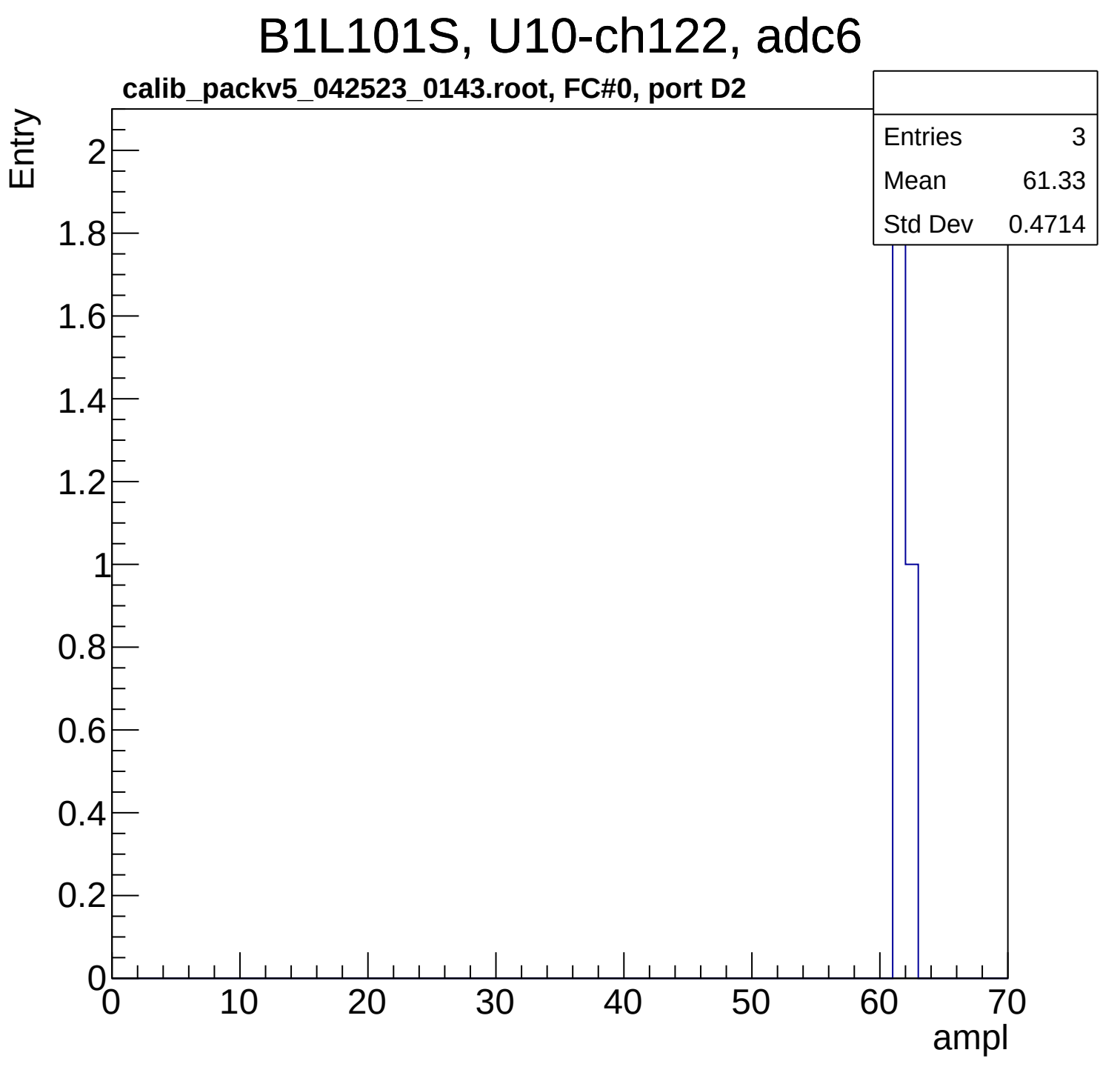
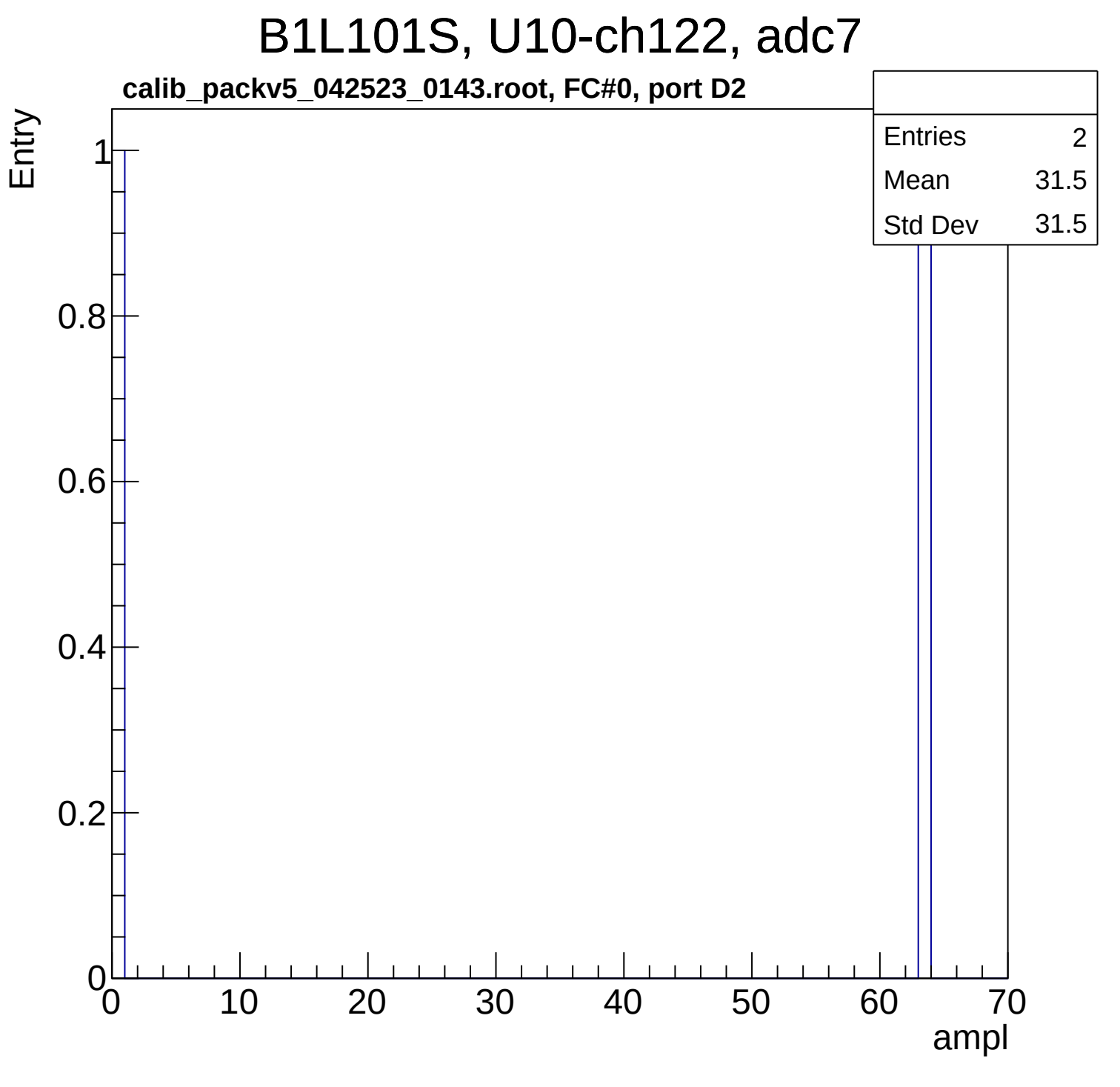

B1L101S, U10-ch122, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 61.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U10-ch122, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
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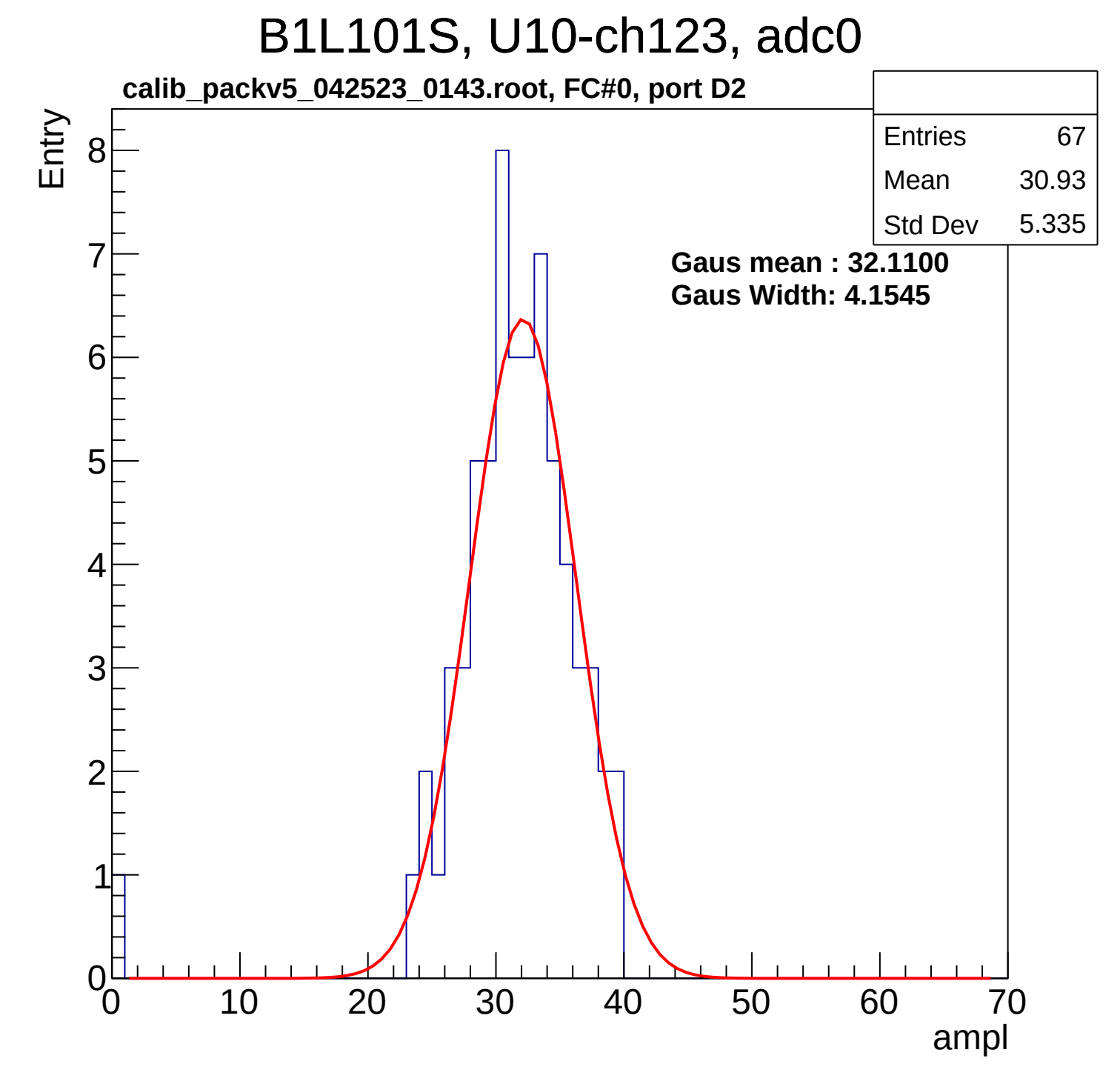
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch123, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 30.93
Std Dev 5.335
Gaus mean : 32.1100
Gaus Width: 4.1545
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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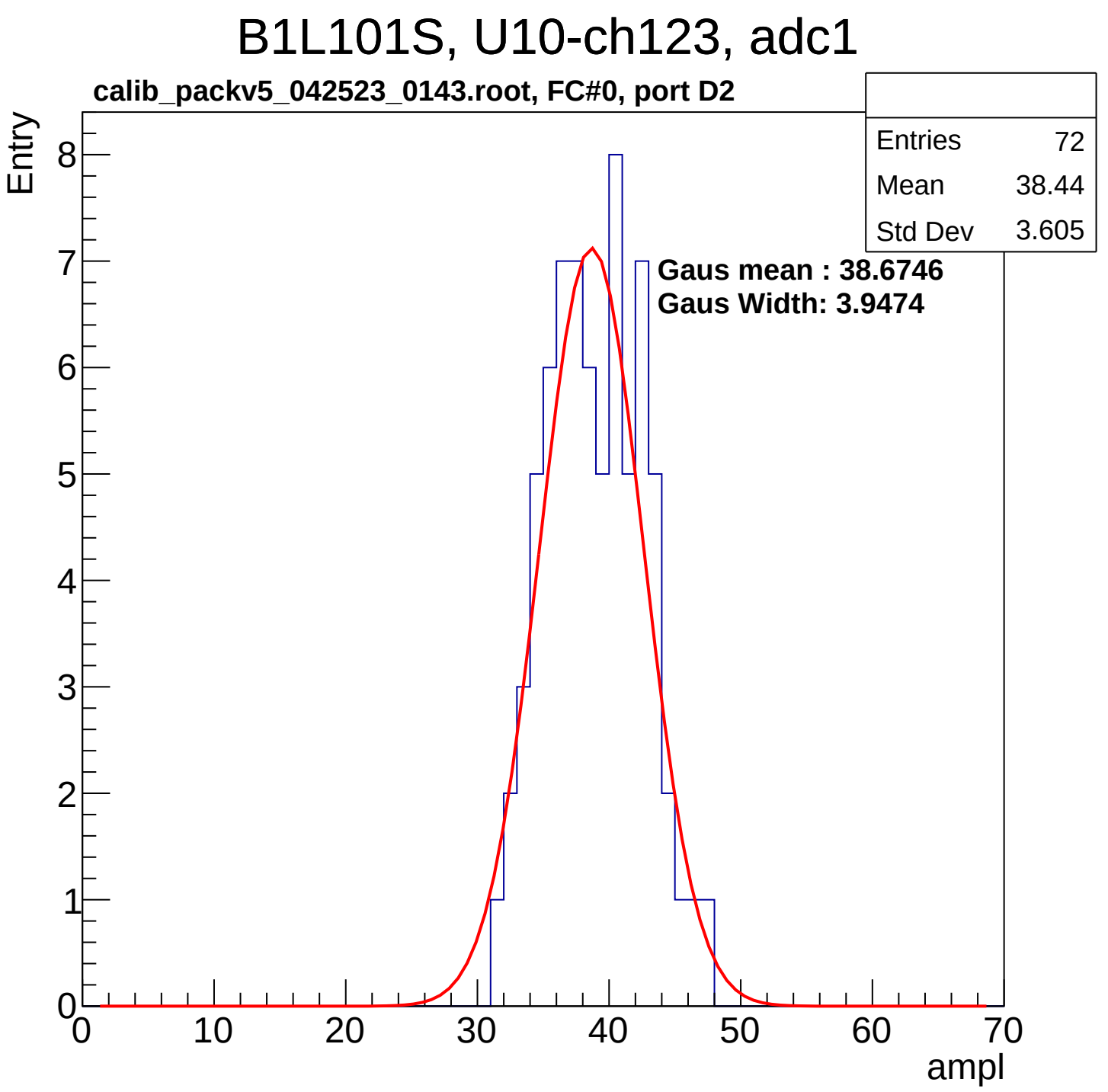
B1L101S, U10-ch123, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 38.44
Std Dev 3.605
Gaus mean : 38.6746
Gaus Width: 3.9474
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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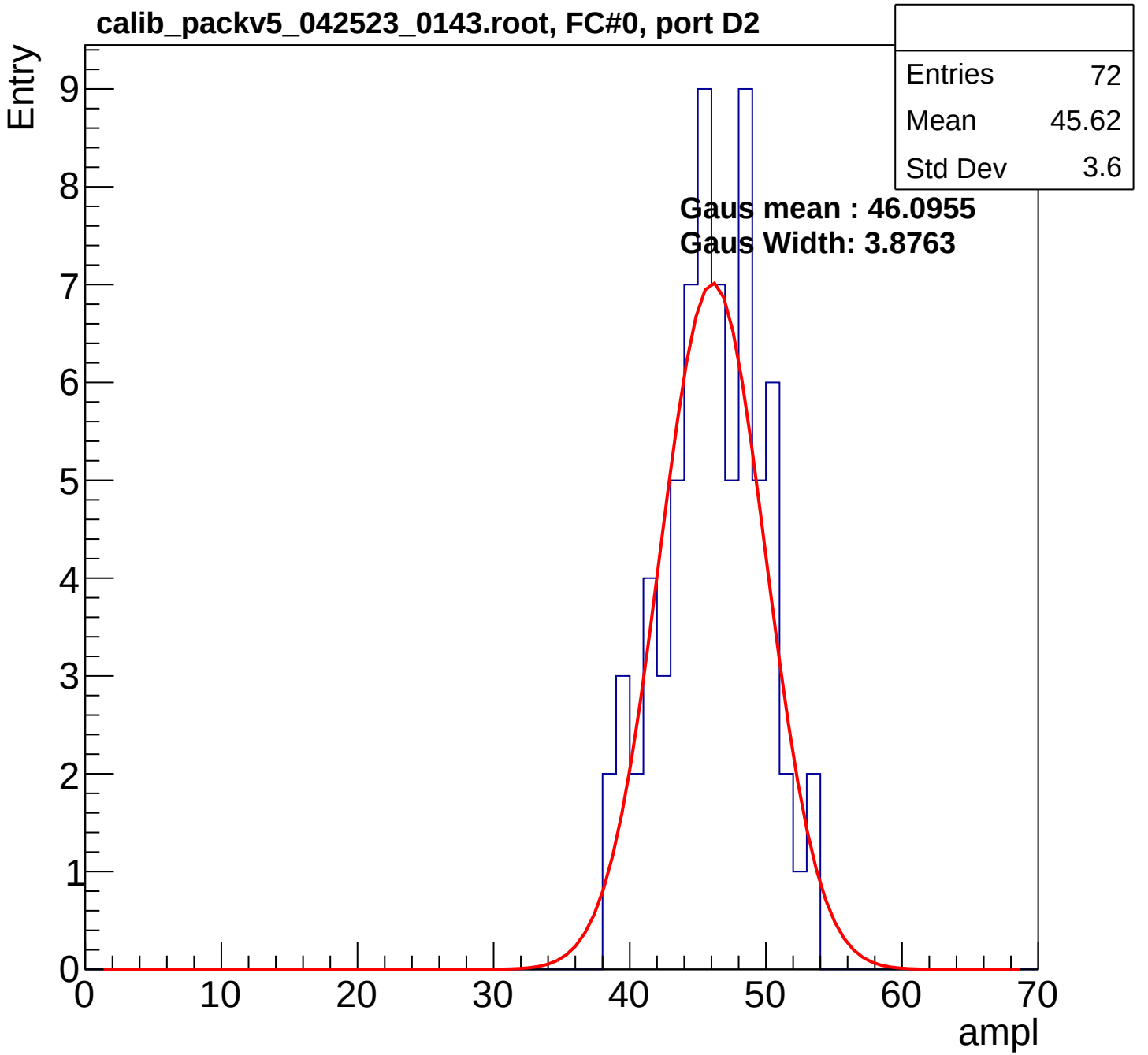
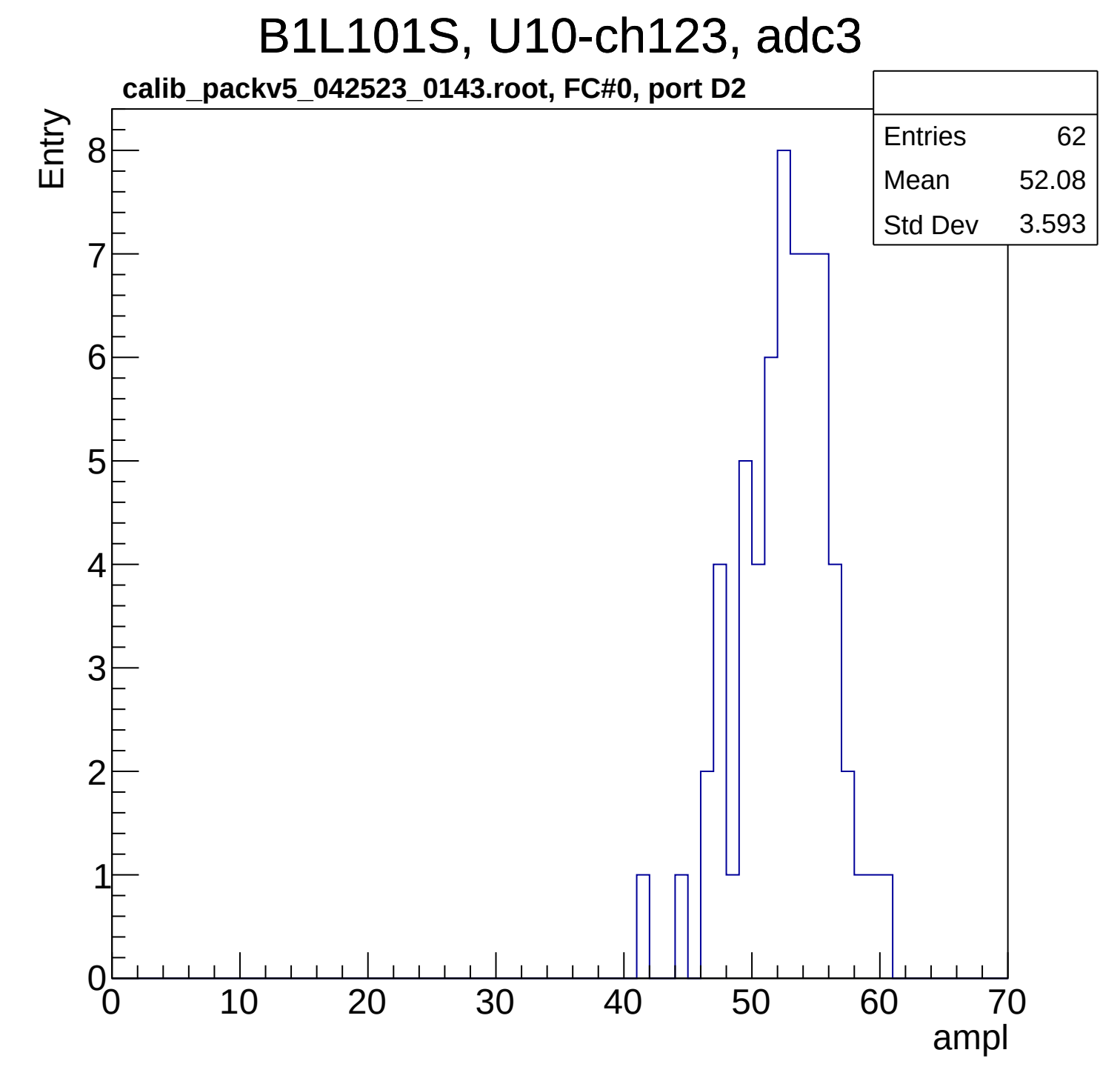
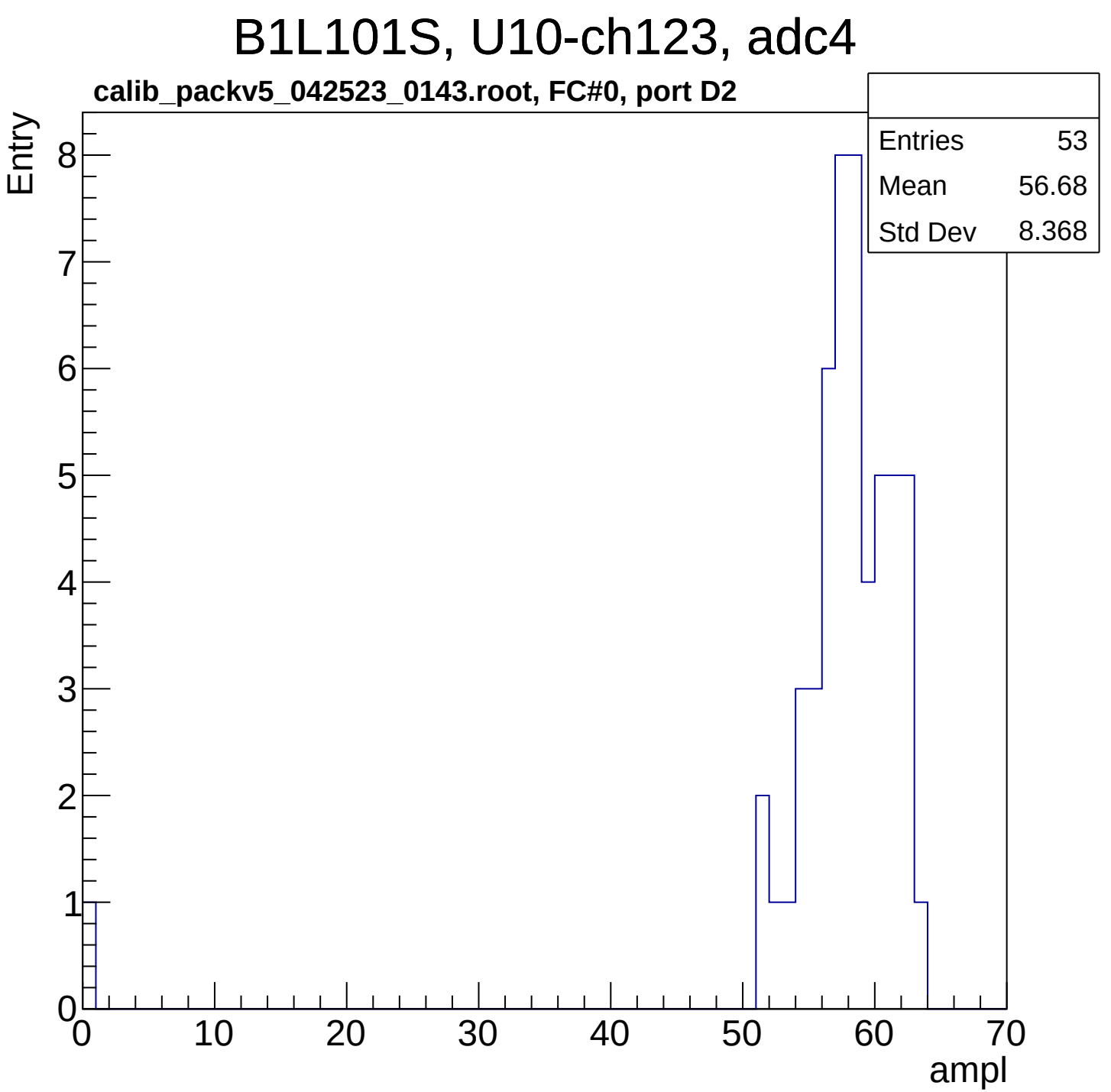

B1L101S, U10-ch123, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 45.62
Std Dev 3.6
Gaus mean : 46.0955
Gaus Width: 3.8763
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch123, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 52.08
Std Dev 3.593
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch123, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 56.68
Std Dev 8.368
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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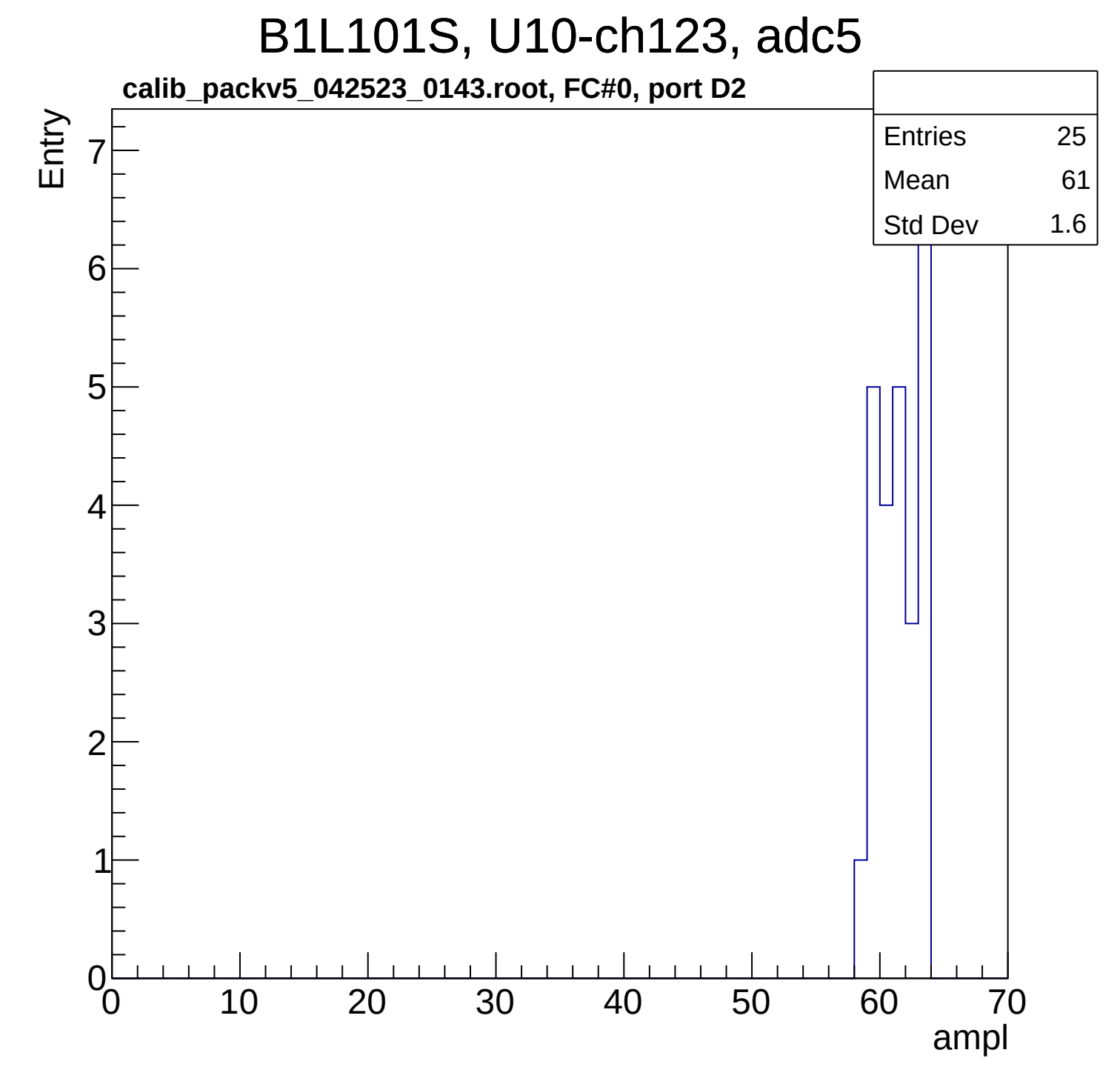
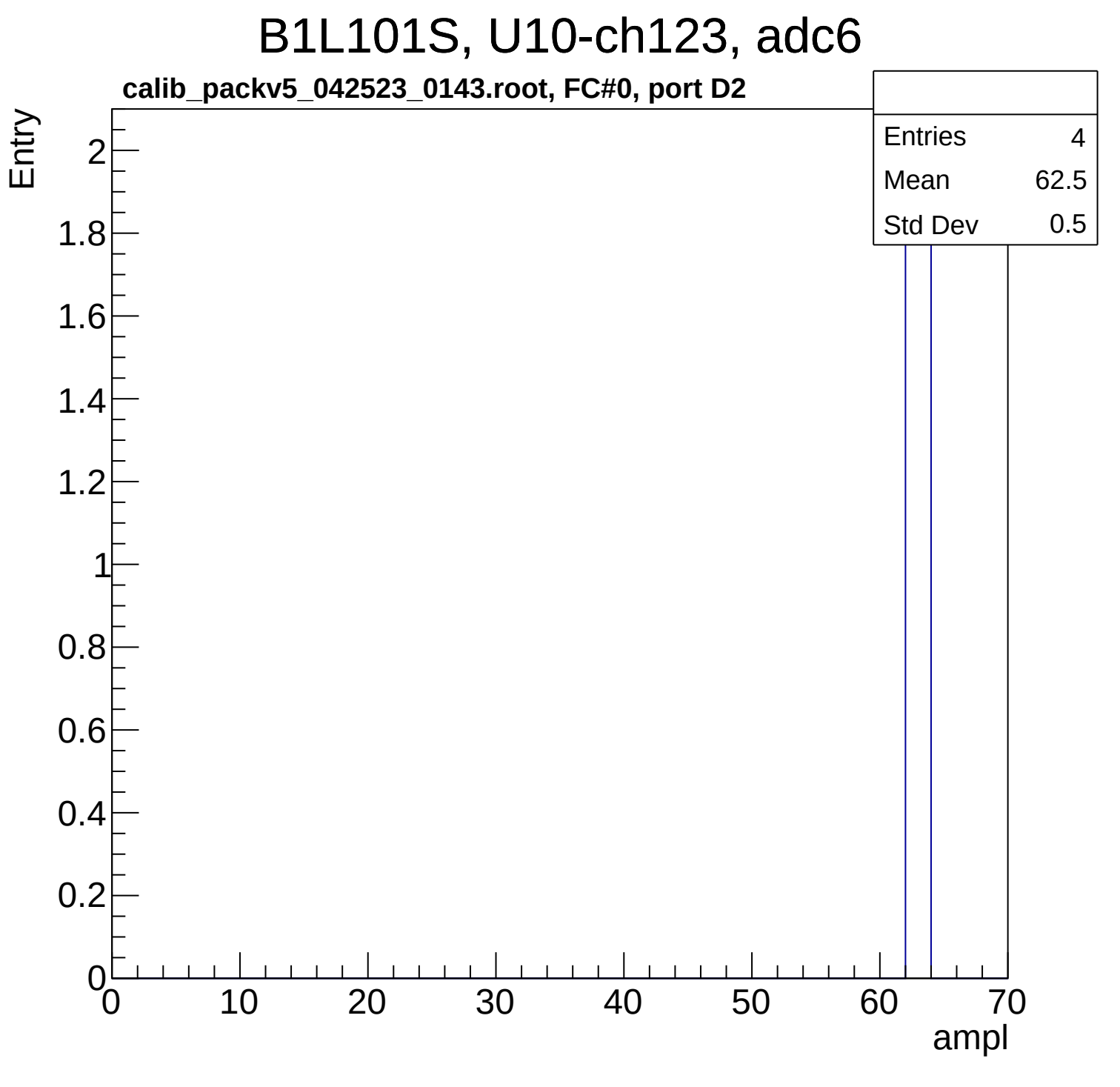
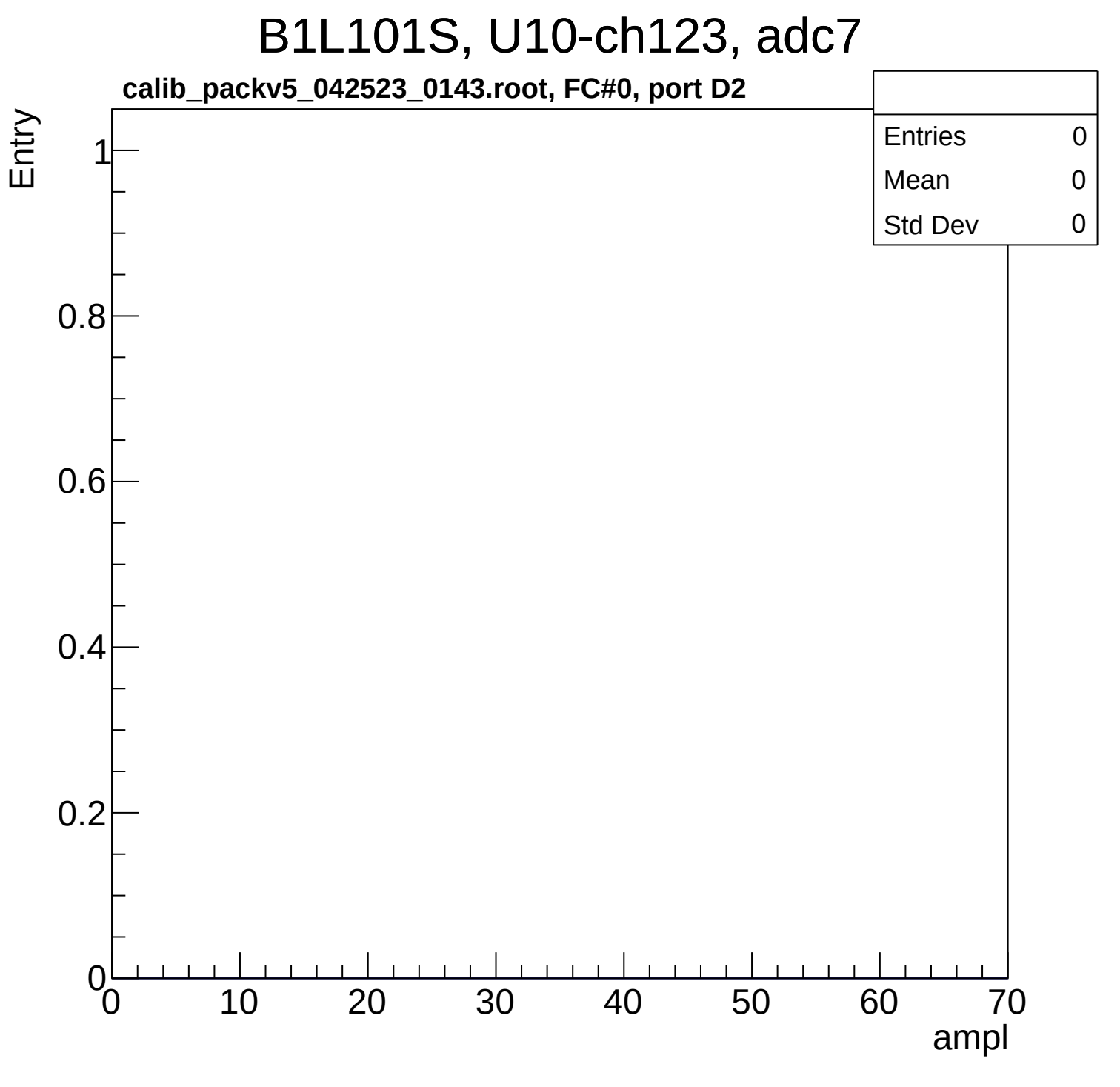
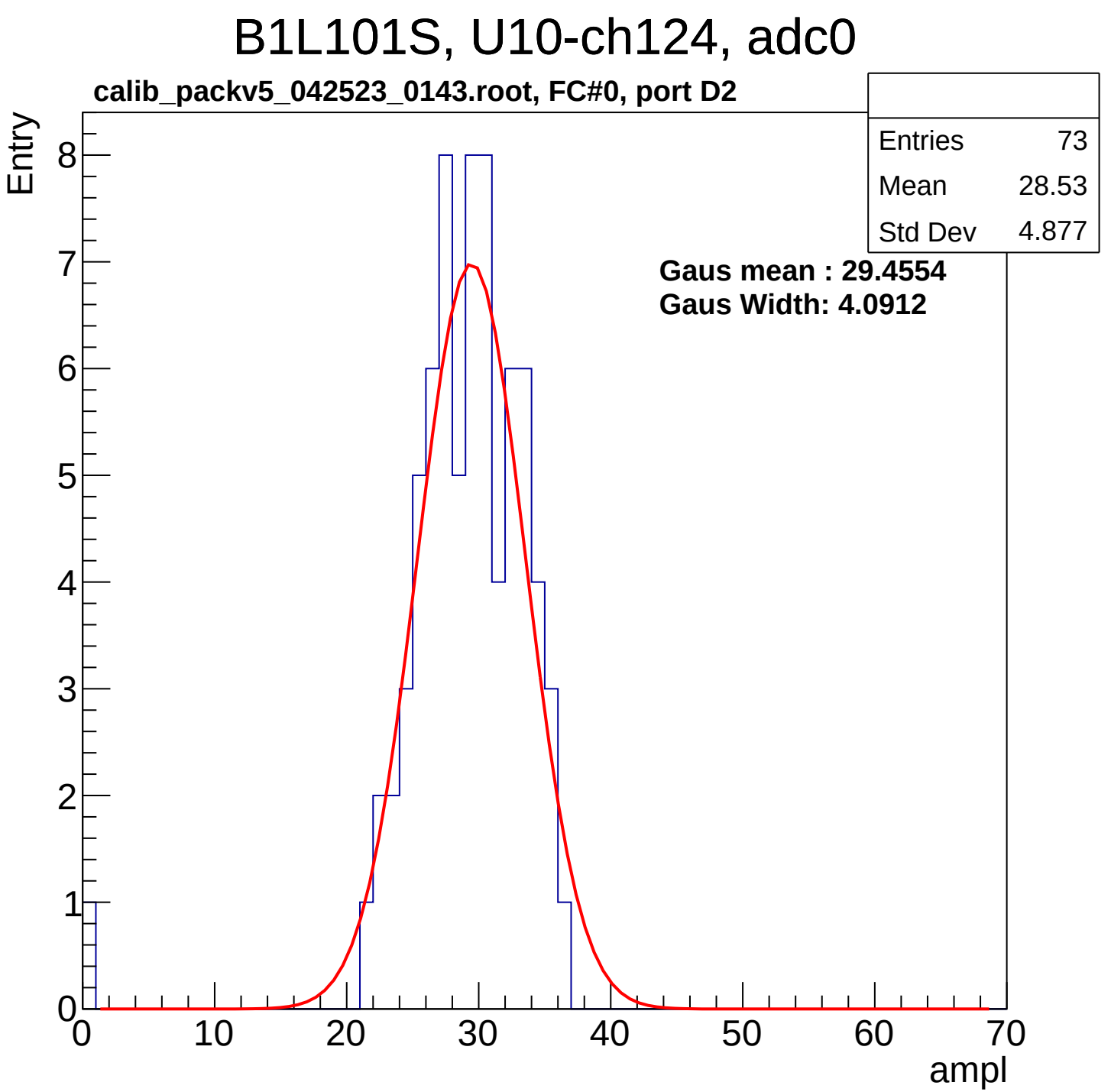
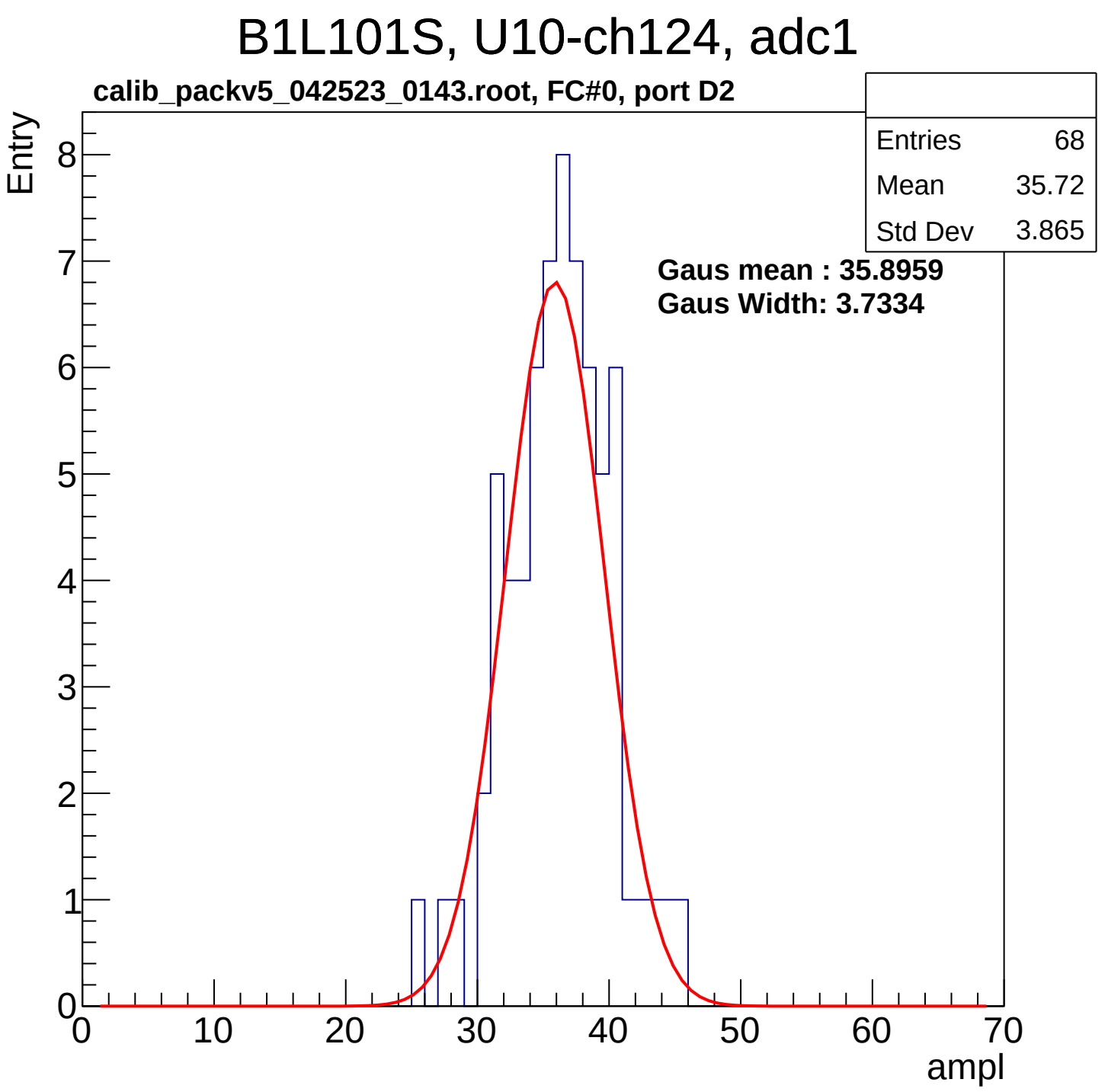
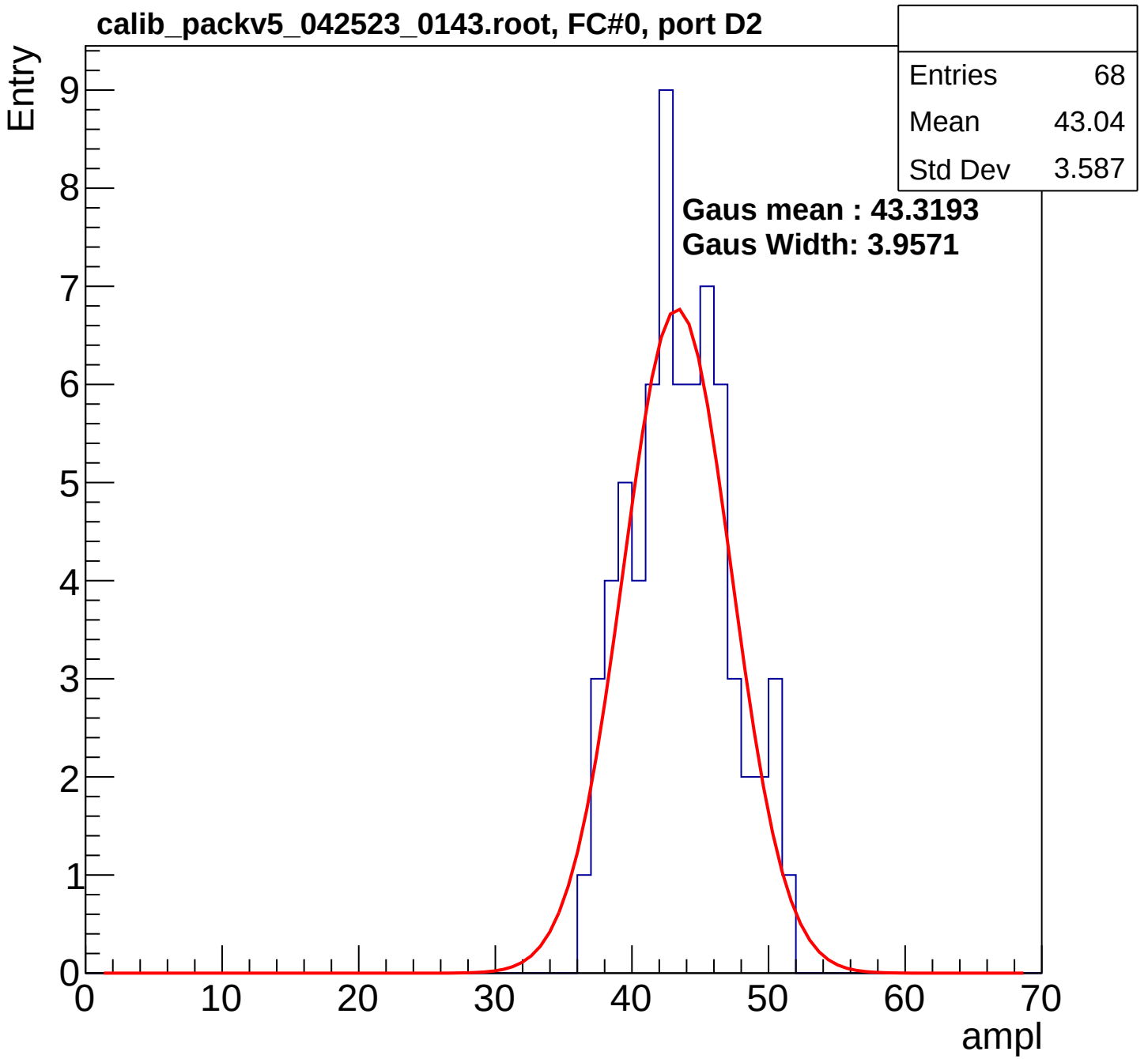

B1L101S, U10-ch123, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 25
Mean 61
Std Dev 1.6
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

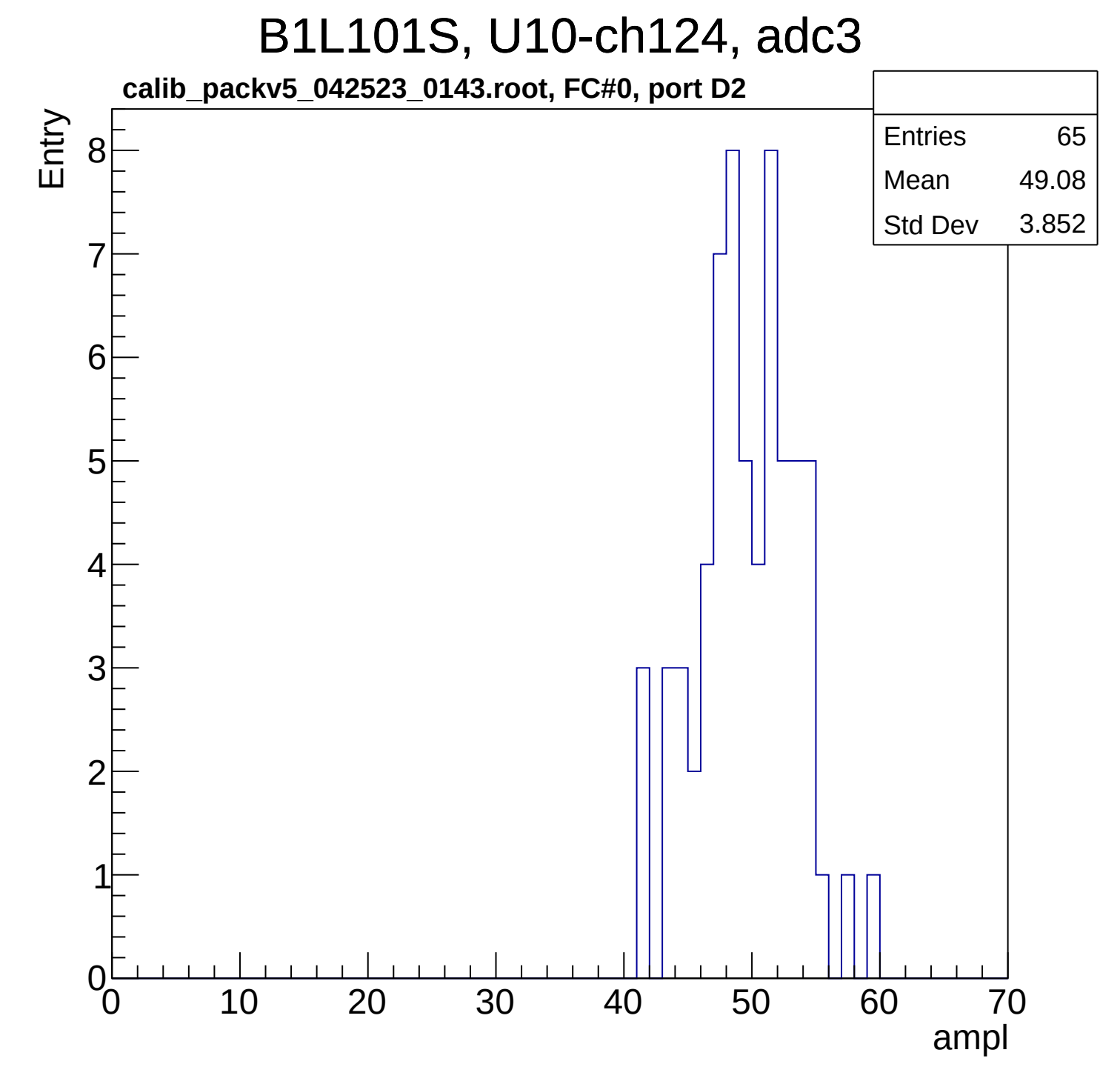

B1L101S, U10-ch123, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 62.5
Std Dev 0.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

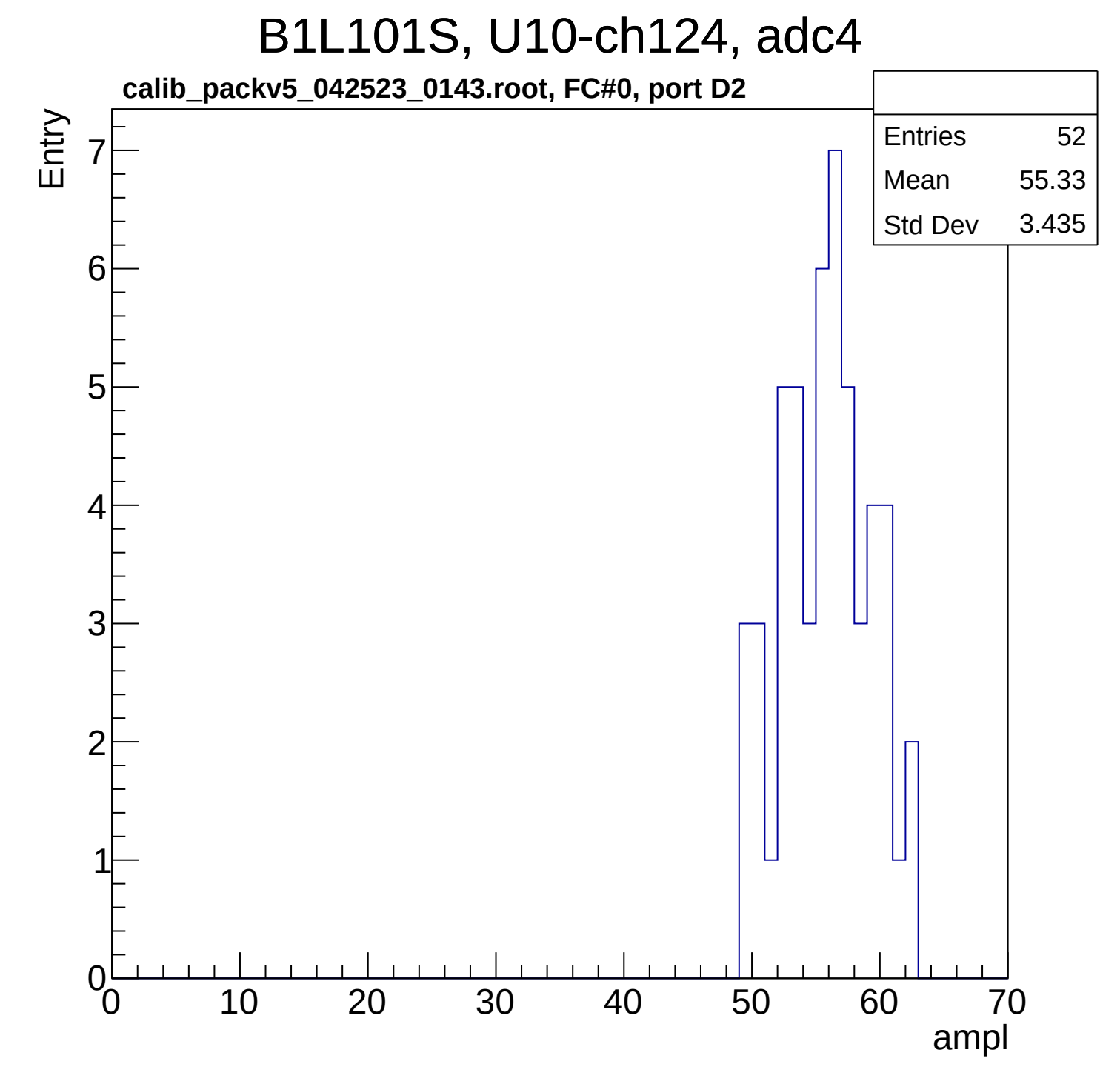

B1L101S, U10-ch123, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

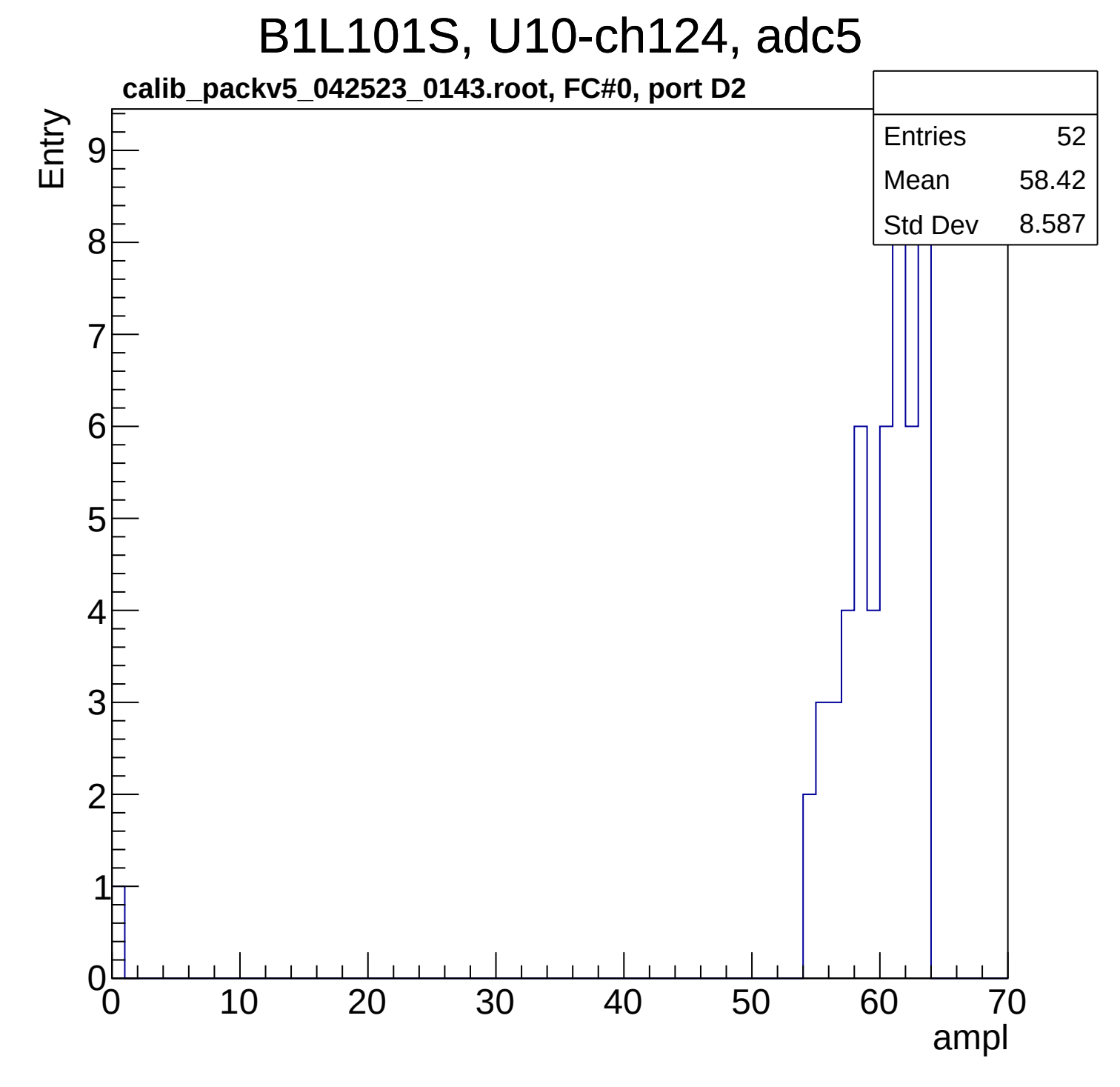

B1L101S, U10-ch124, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 28.53
Std Dev 4.877
Gaus mean : 29.4554
Gaus Width: 4.0912
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

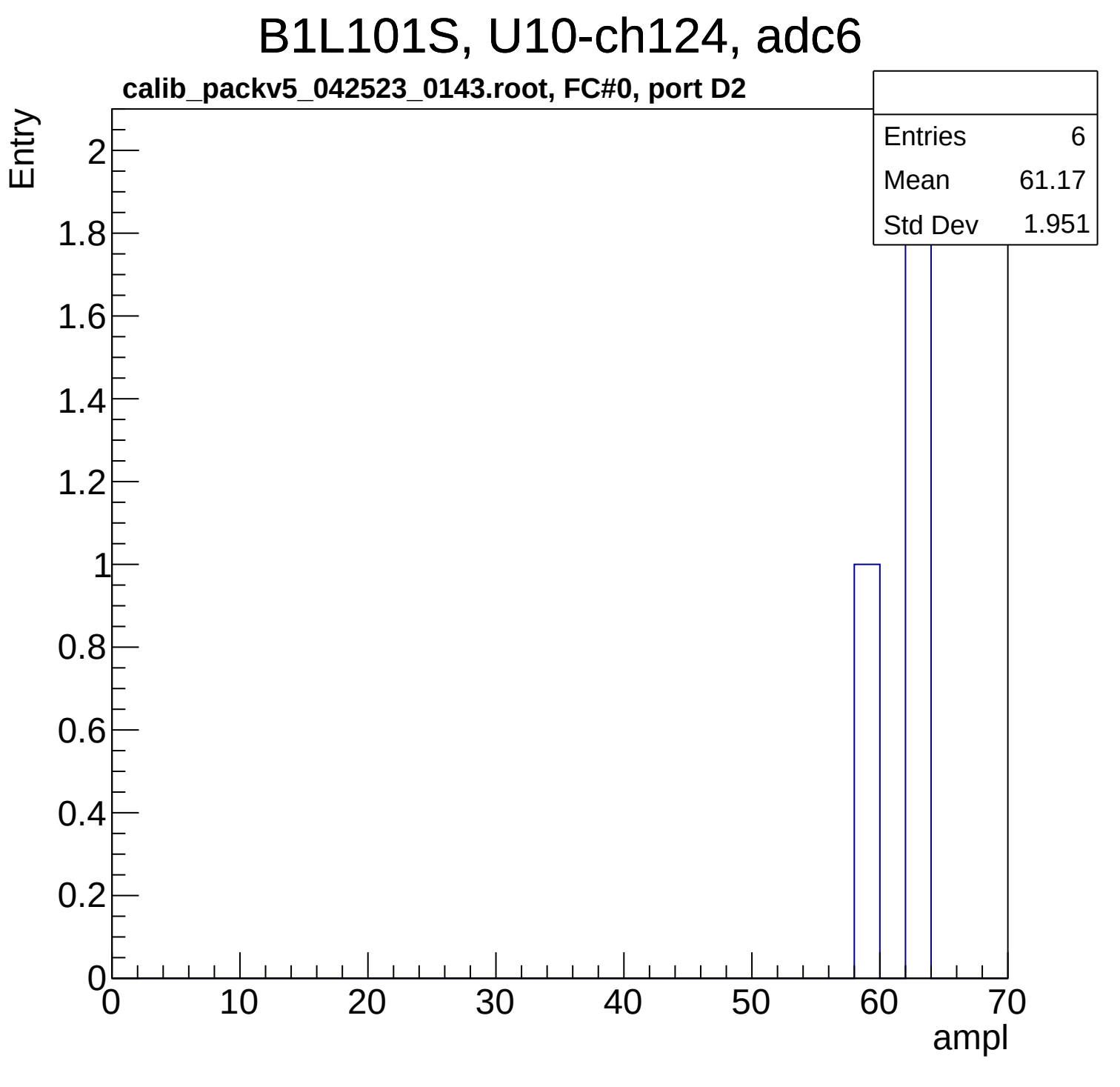

B1L101S, U10-ch124, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 35.72
Std Dev 3.865
Gaus mean : 35.8959
Gaus Width: 3.7334
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

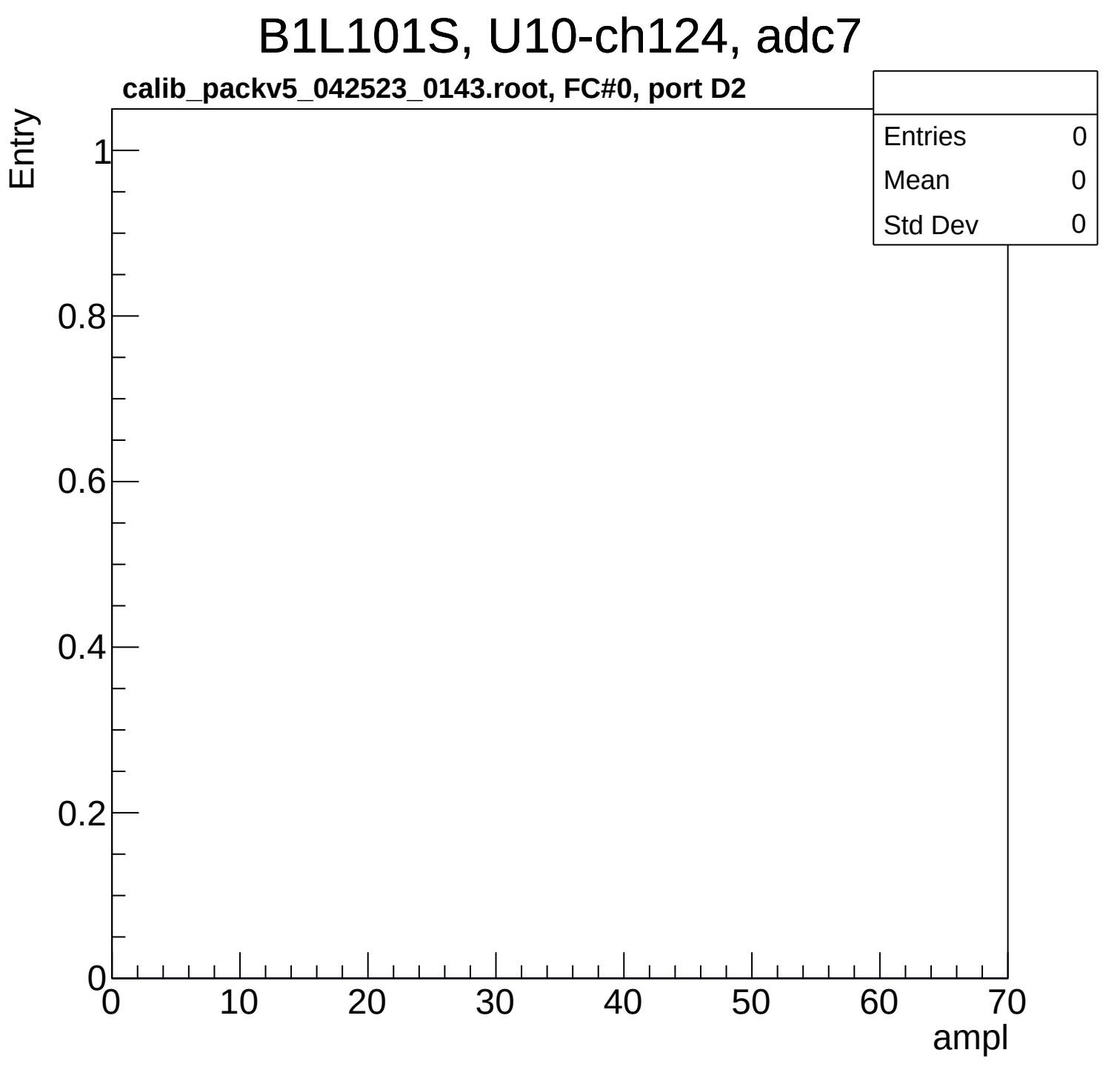

B1L101S, U10-ch124, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 43.04
Std Dev 3.587
Gaus mean : 43.3193
Gaus Width: 3.9571
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

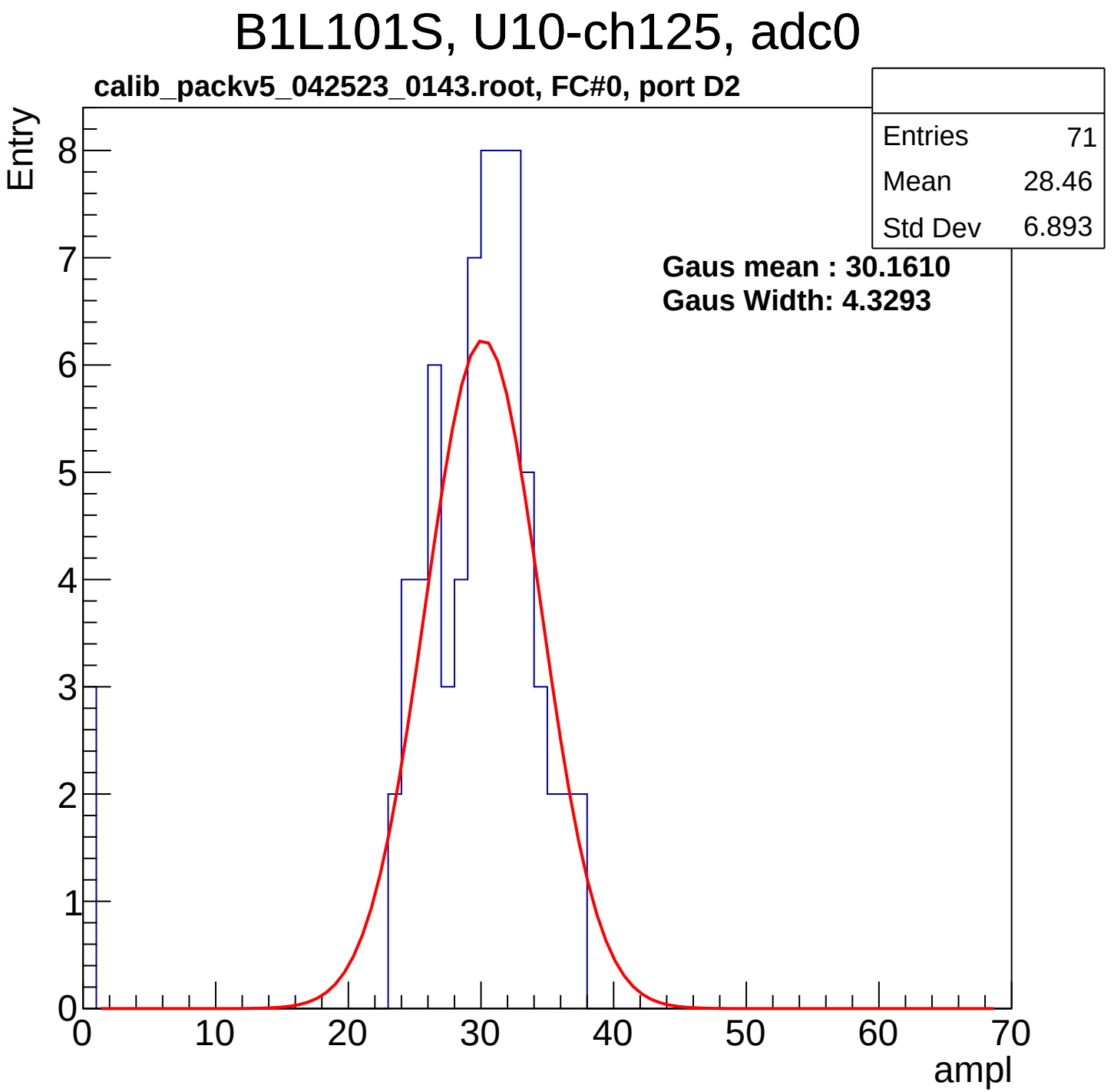

B1L101S, U10-ch124, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 49.08
Std Dev 3.852
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

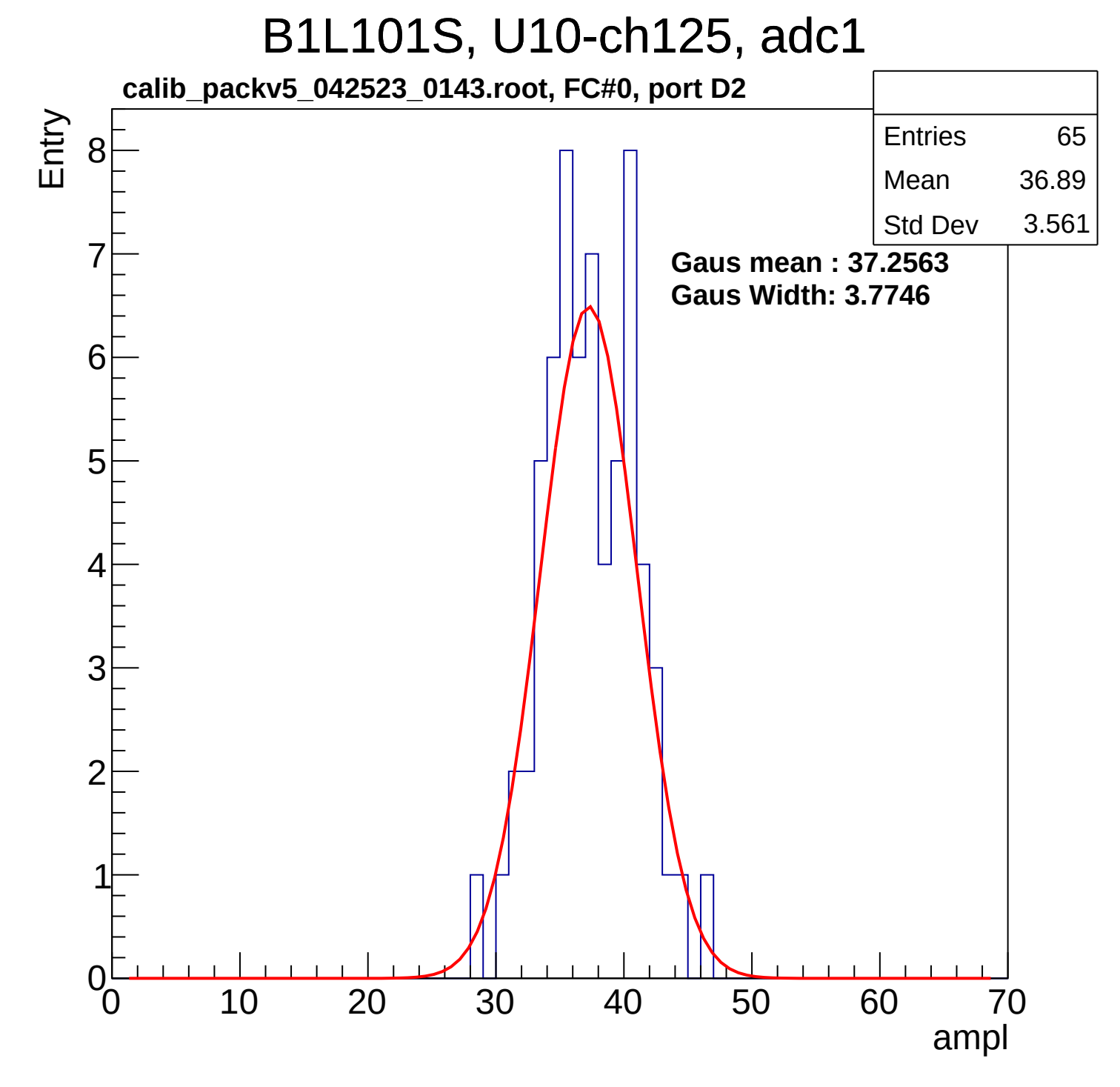

B1L101S, U10-ch124, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 55.33
Std Dev 3.435
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

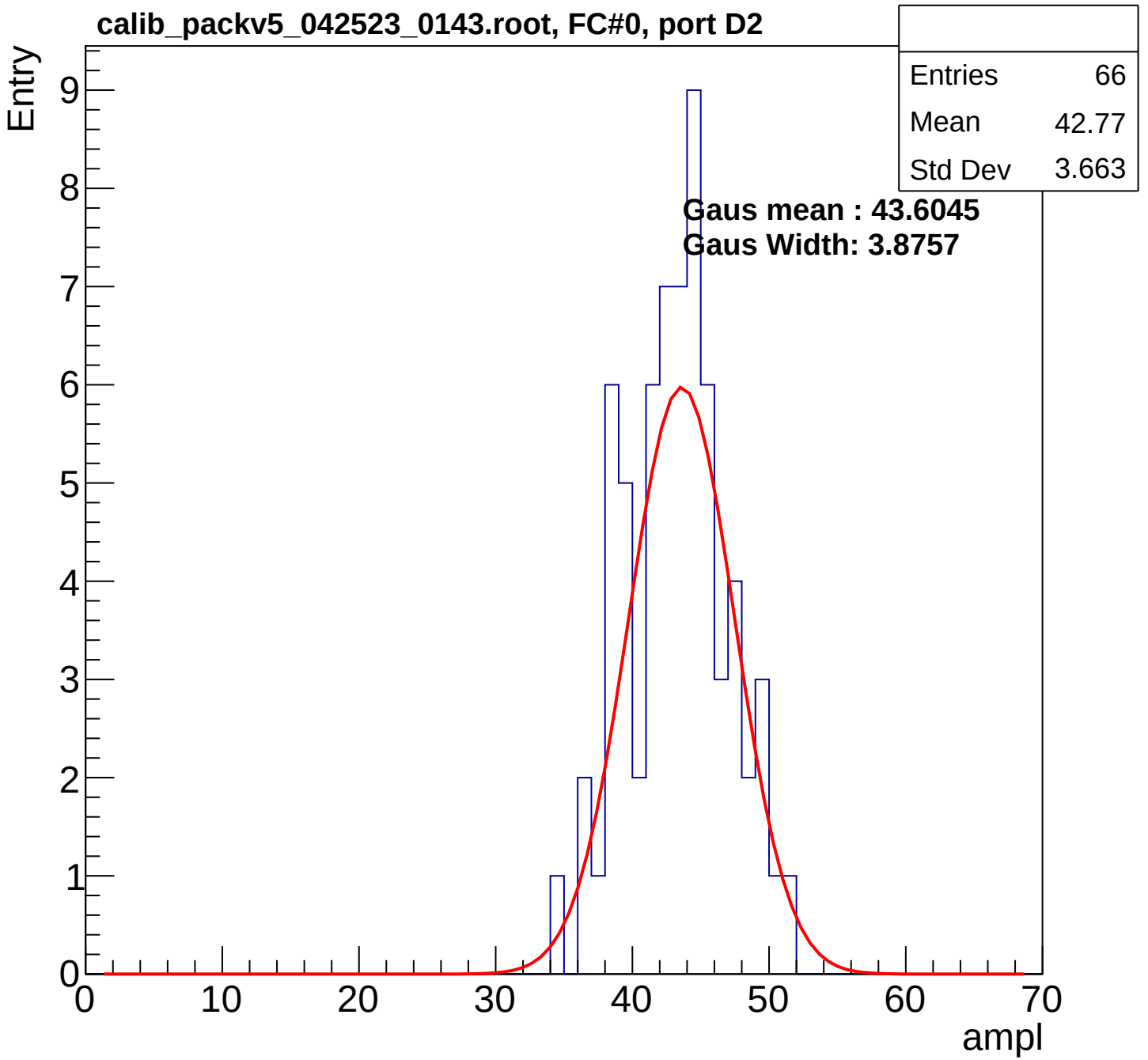

B1L101S, U10-ch124, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 58.42
Std Dev 8.587
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

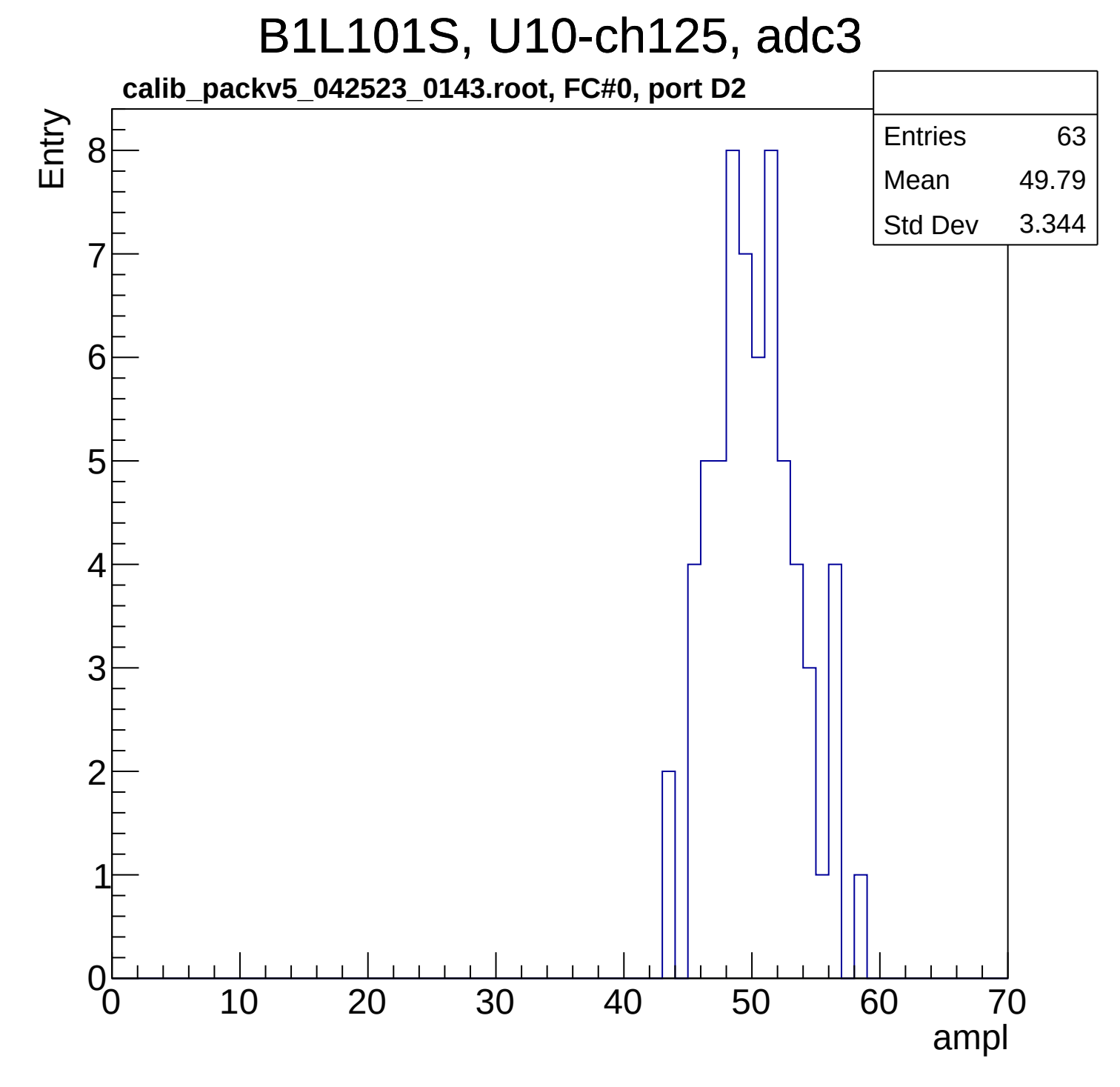

B1L101S, U10-ch124, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 61.17
Std Dev 1.951
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

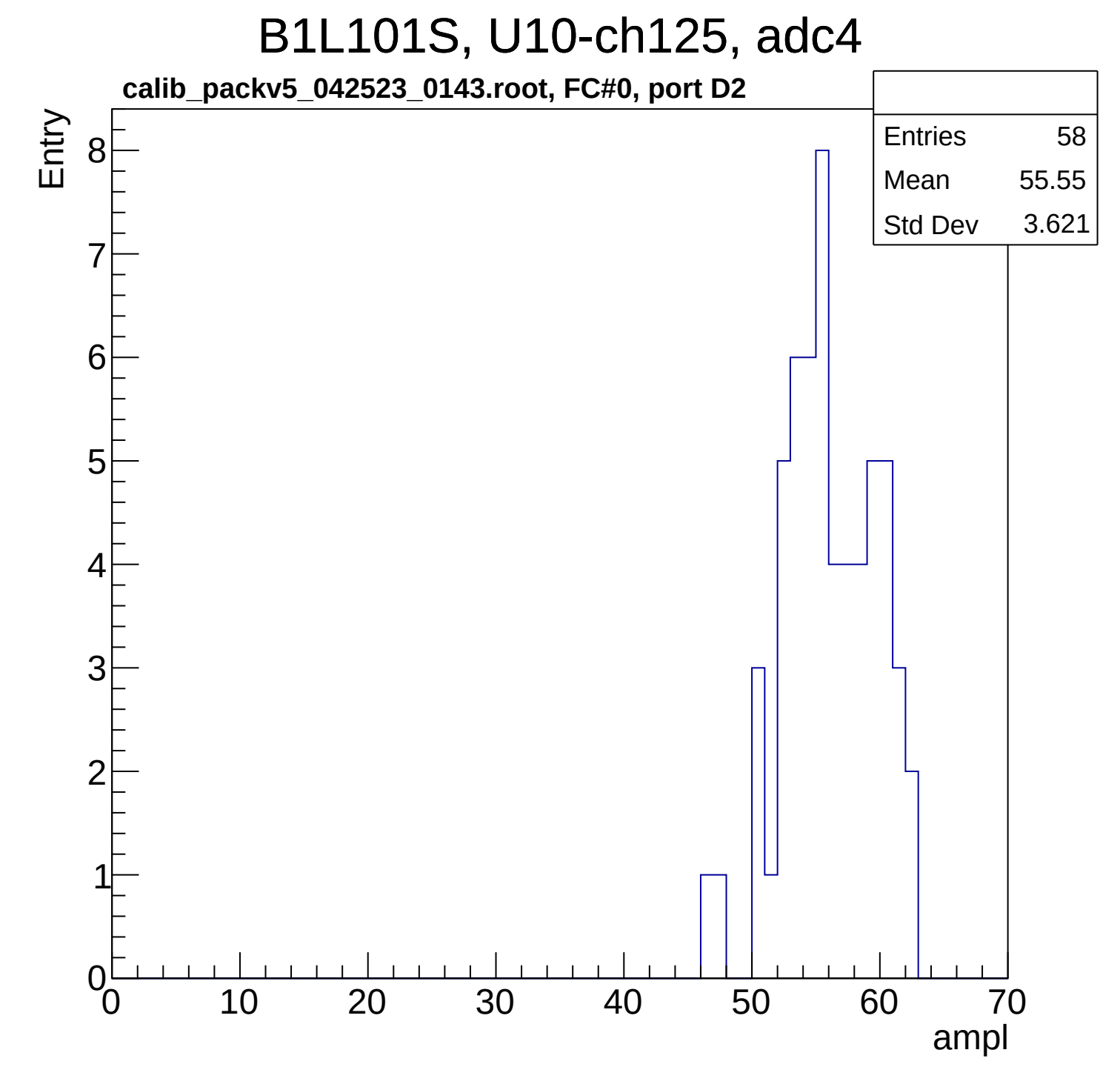

B1L101S, U10-ch124, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

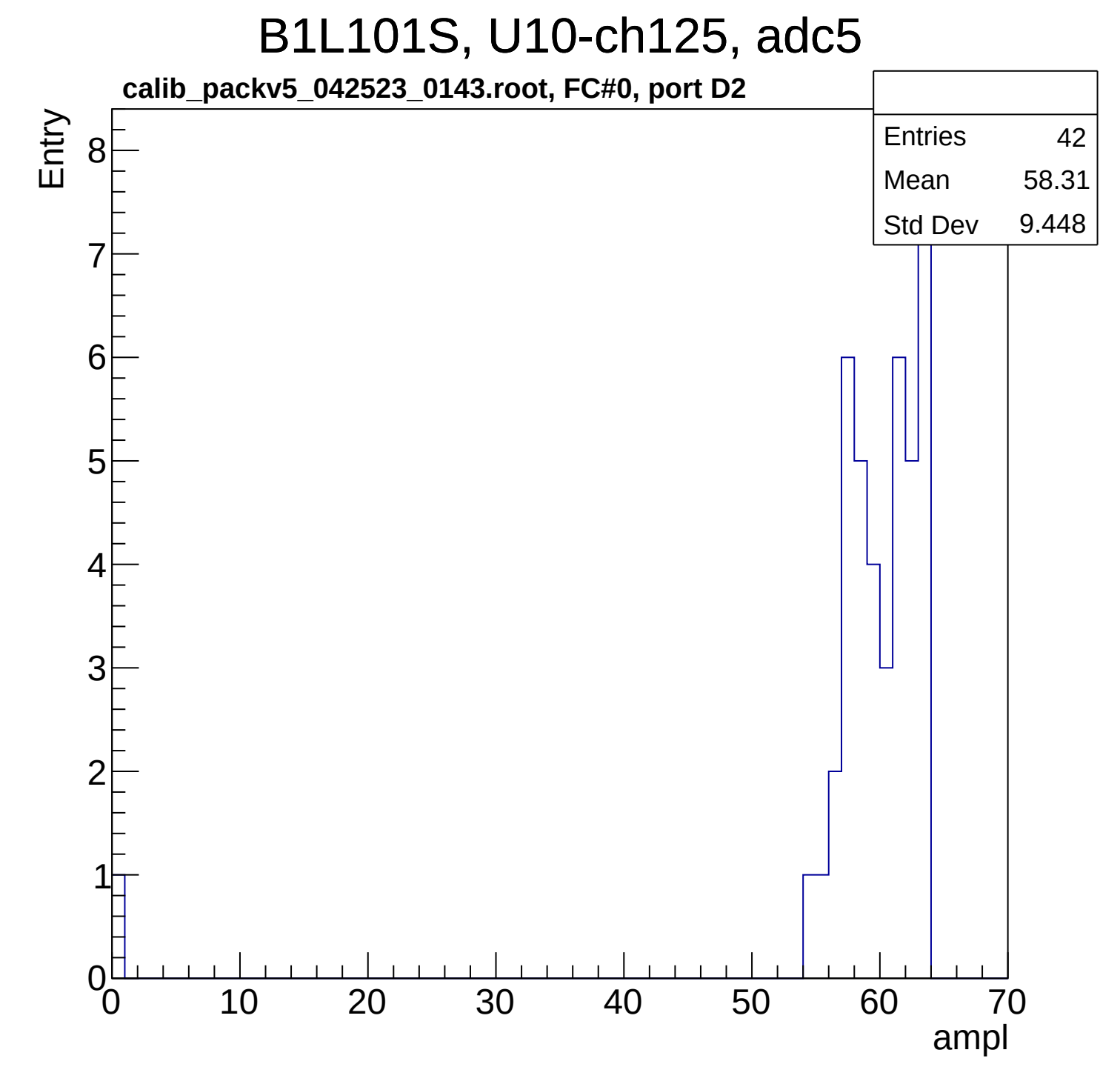

B1L101S, U10-ch125, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 28.46
Std Dev 6.893
Gaus mean : 30.1610
Gaus Width: 4.3293
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch125, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 36.89
Std Dev 3.561
Gaus mean : 37.2563
Gaus Width: 3.7746
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch125, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 42.77
Std Dev 3.663
Gaus mean : 43.6045
Gaus Width: 3.8757
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U10-ch125, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 49.79
Std Dev 3.344
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch125, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 55.55
Std Dev 3.621
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch125, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 58.31
Std Dev 9.448
Entry
ampl
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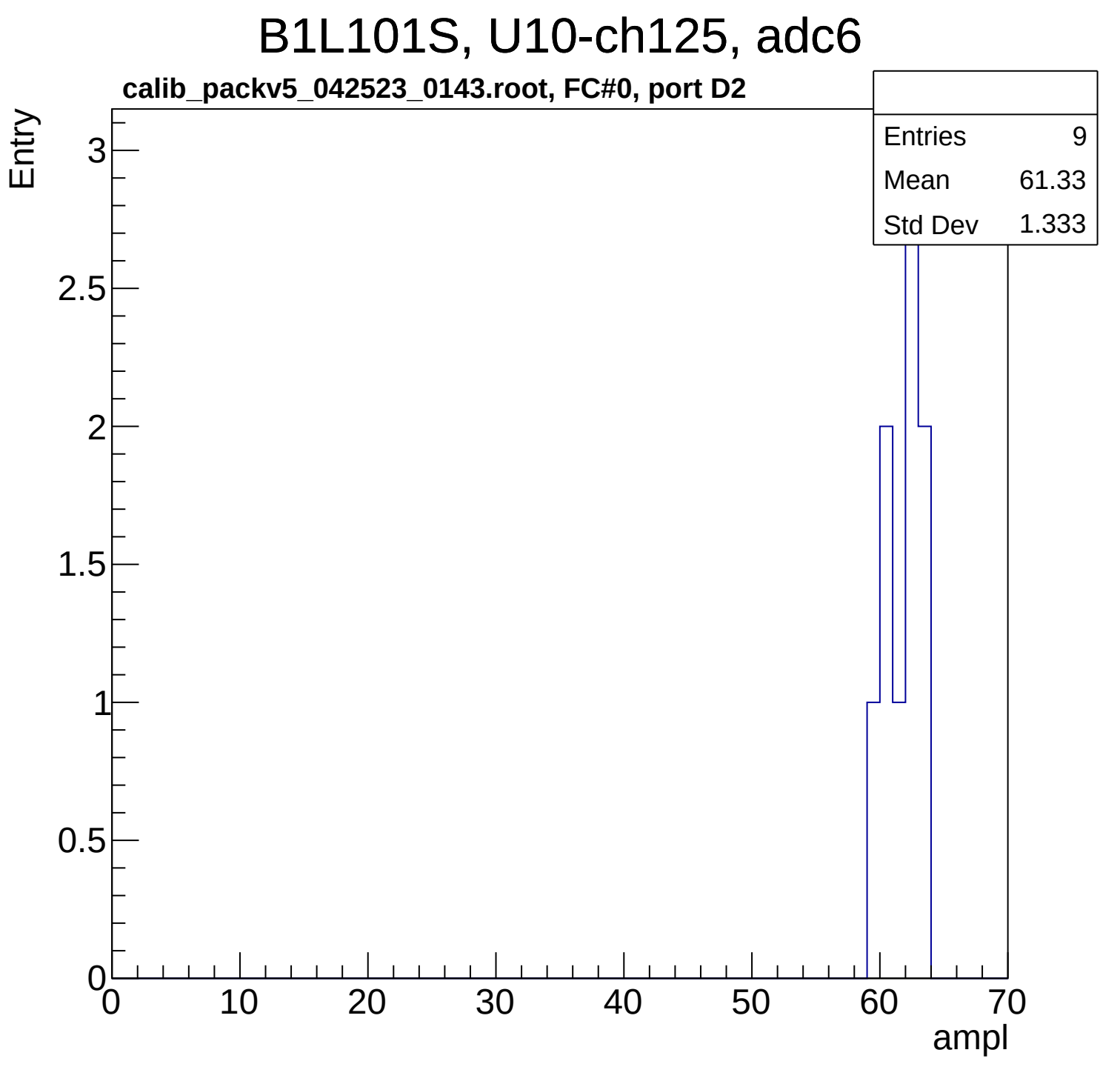
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch125, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 61.33
Std Dev 1.333
Entry
ampl
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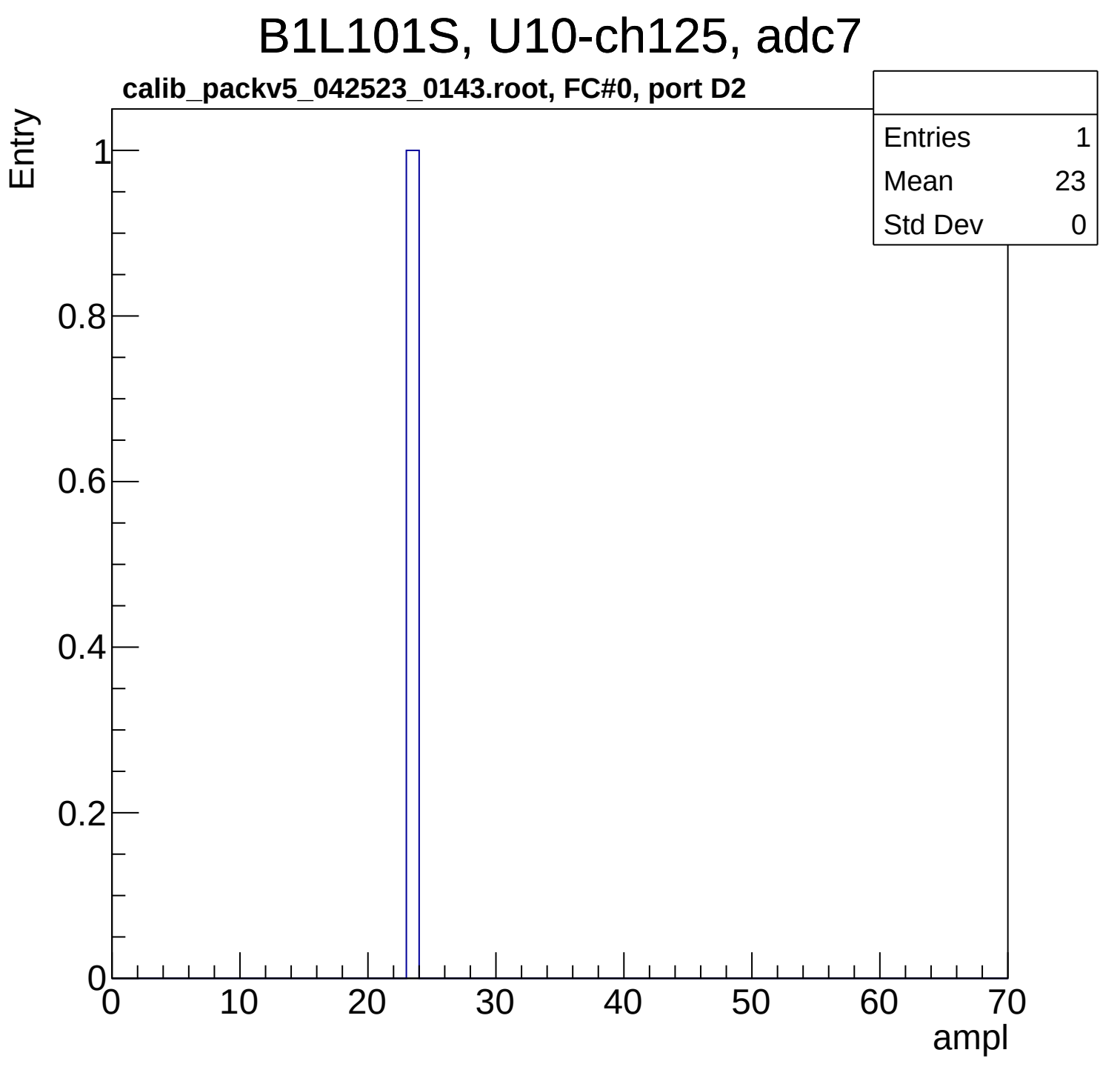
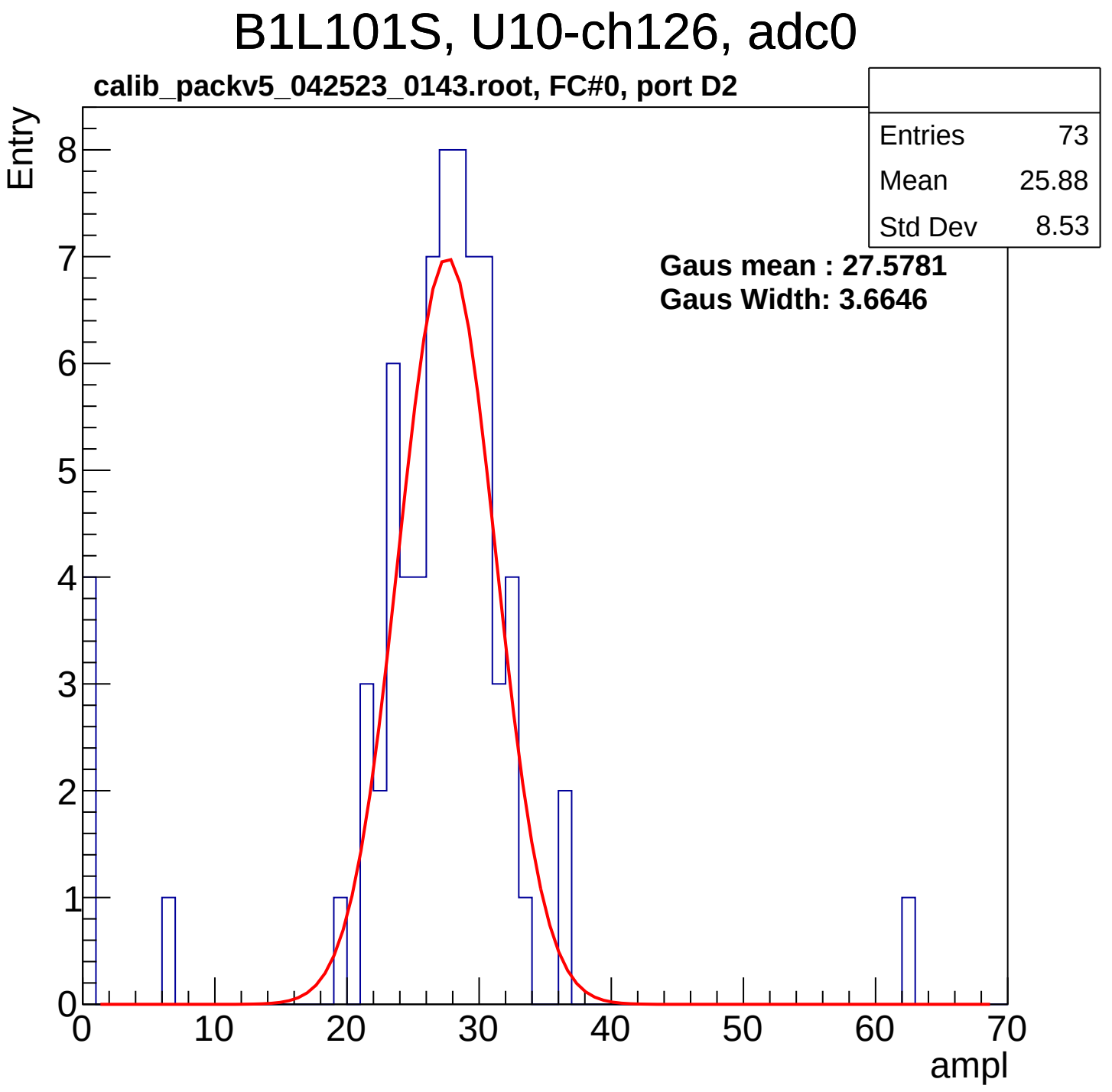
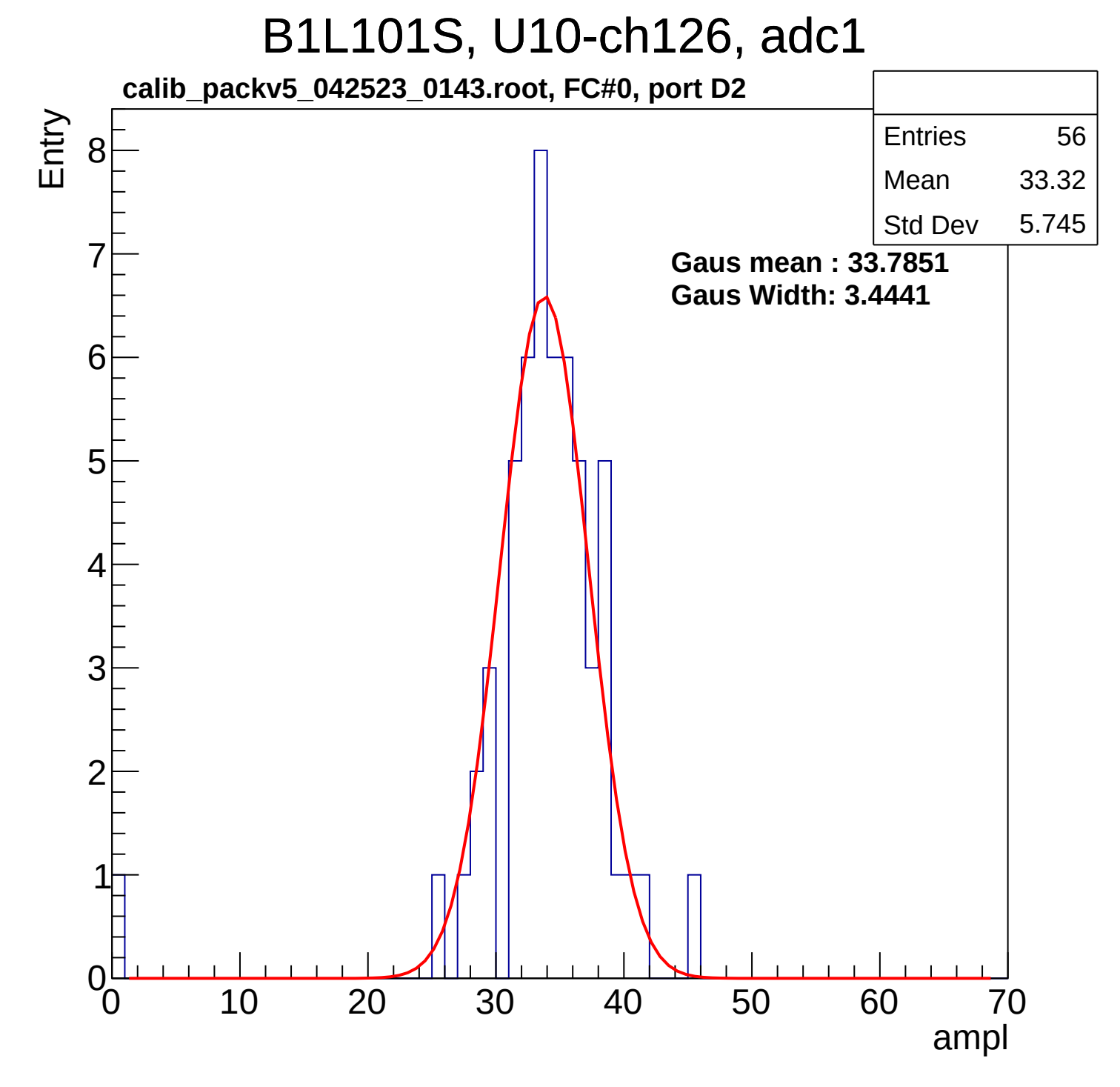
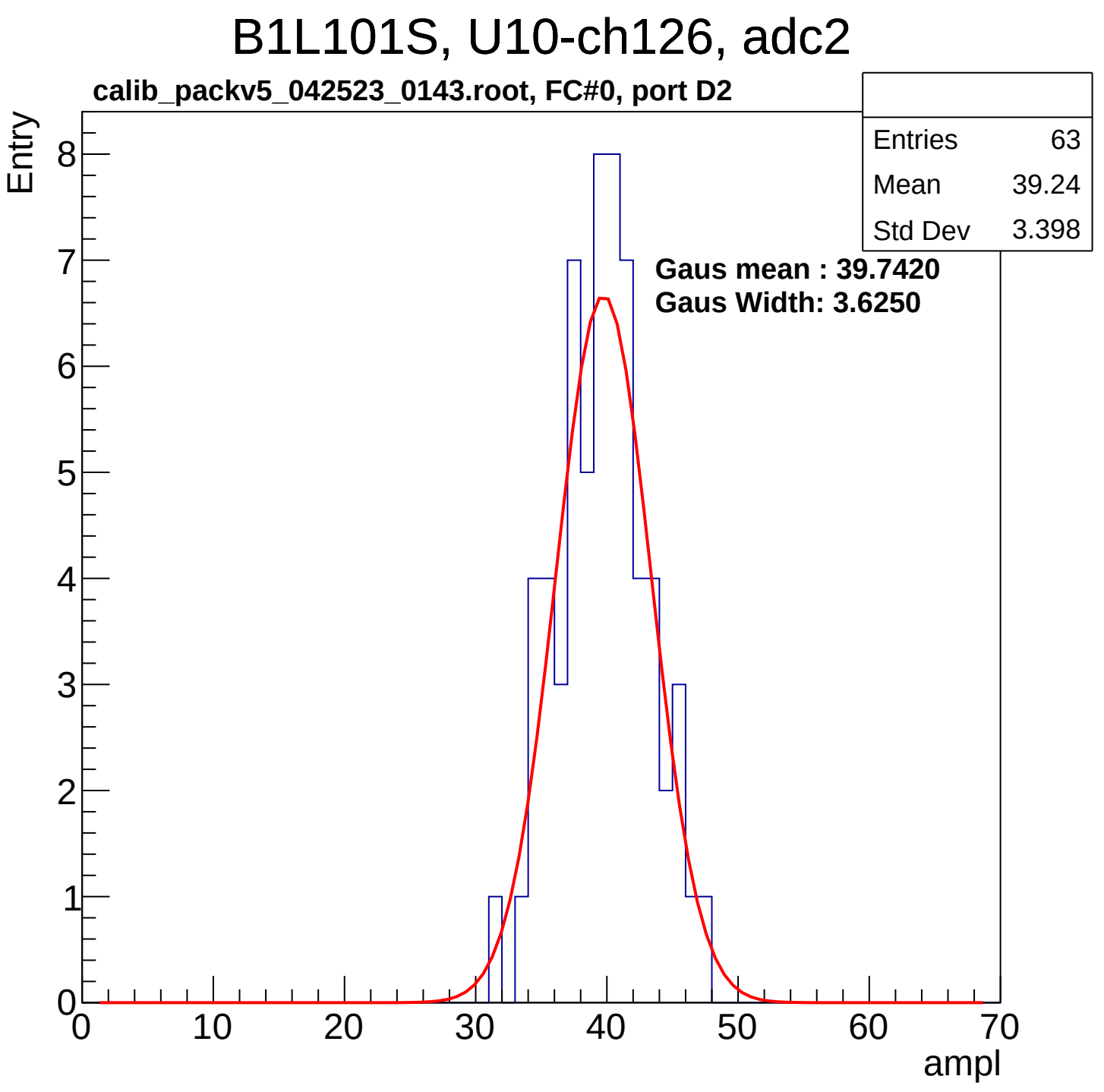
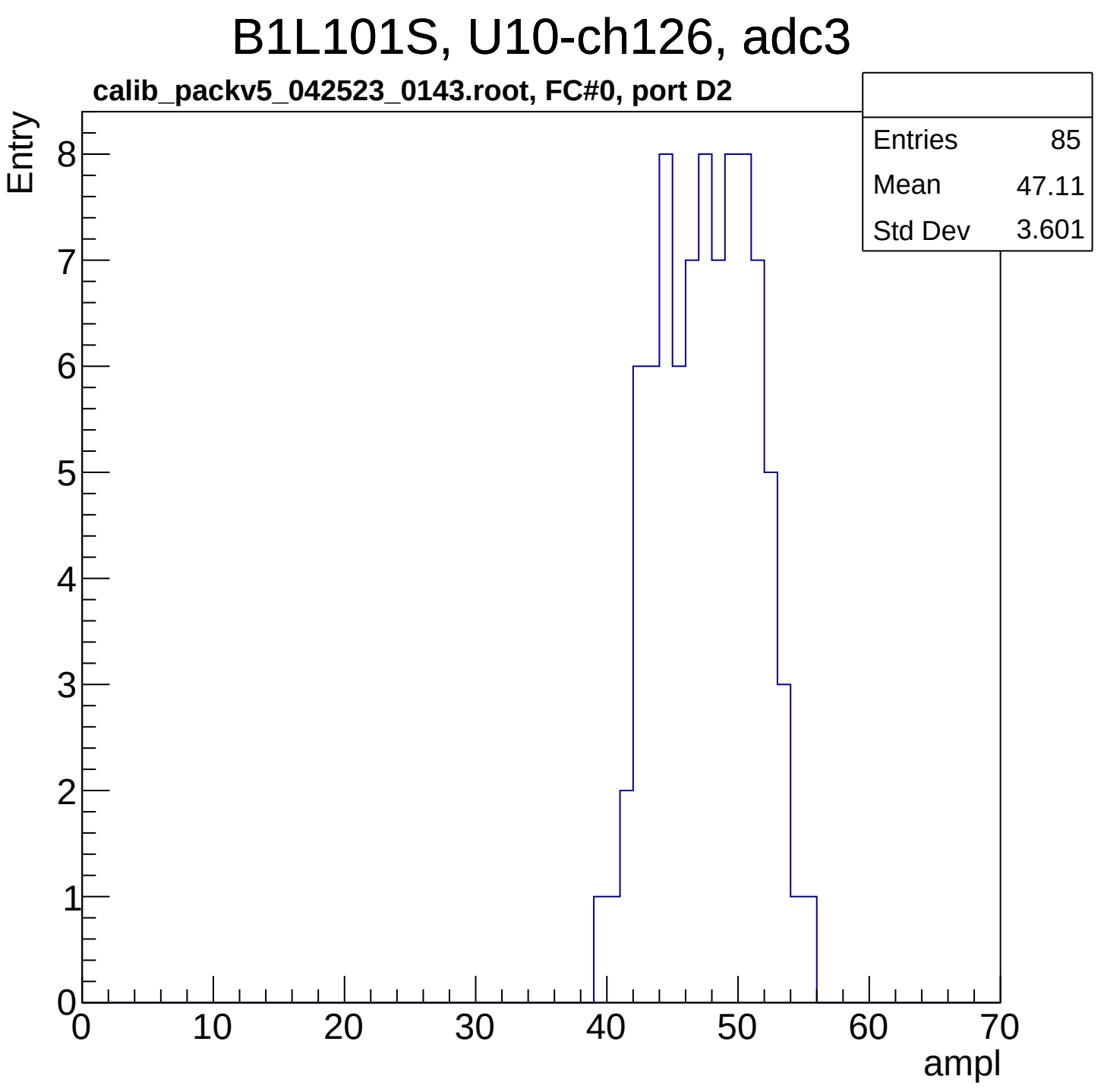
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

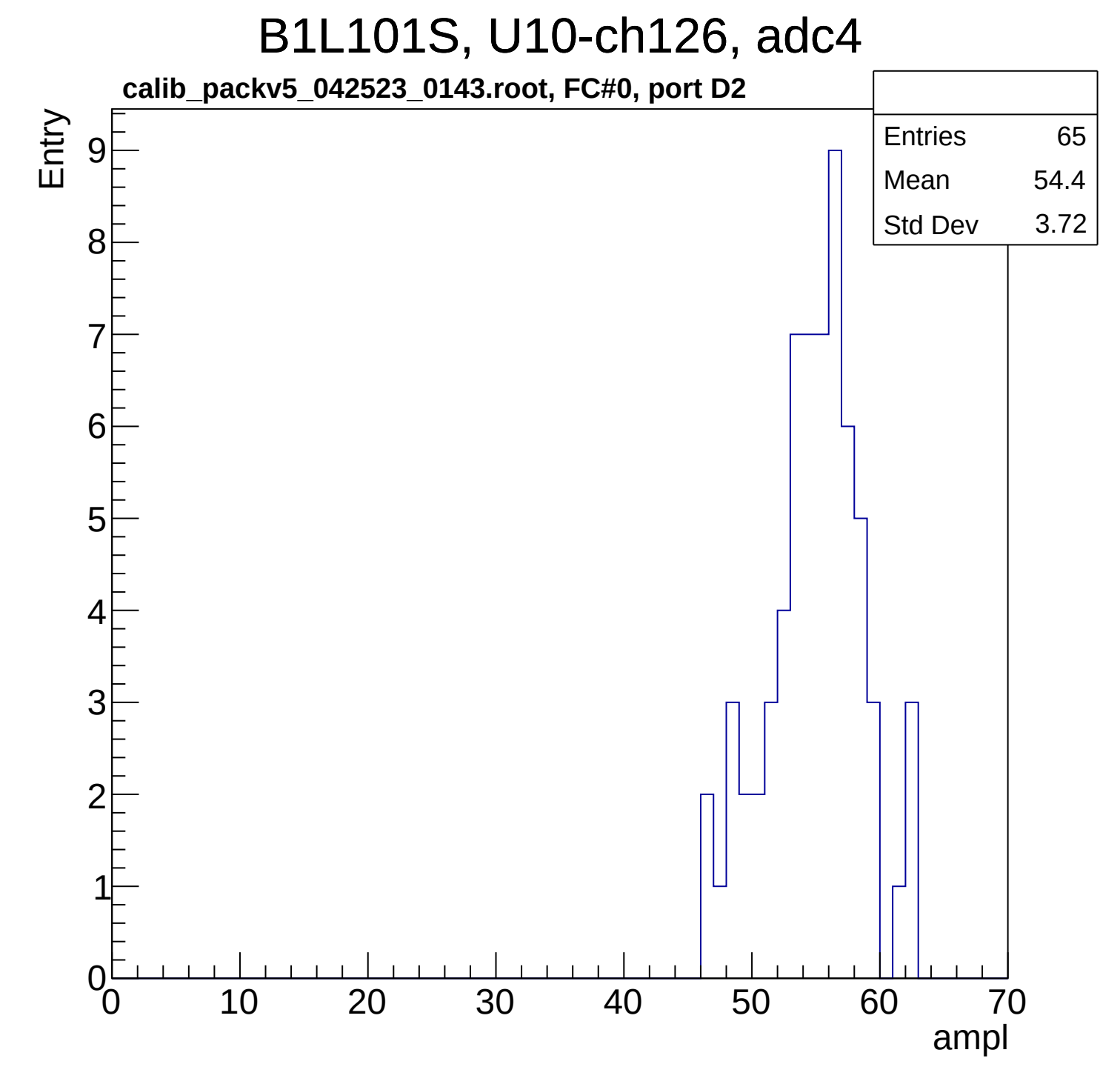

B1L101S, U10-ch125, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 23
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

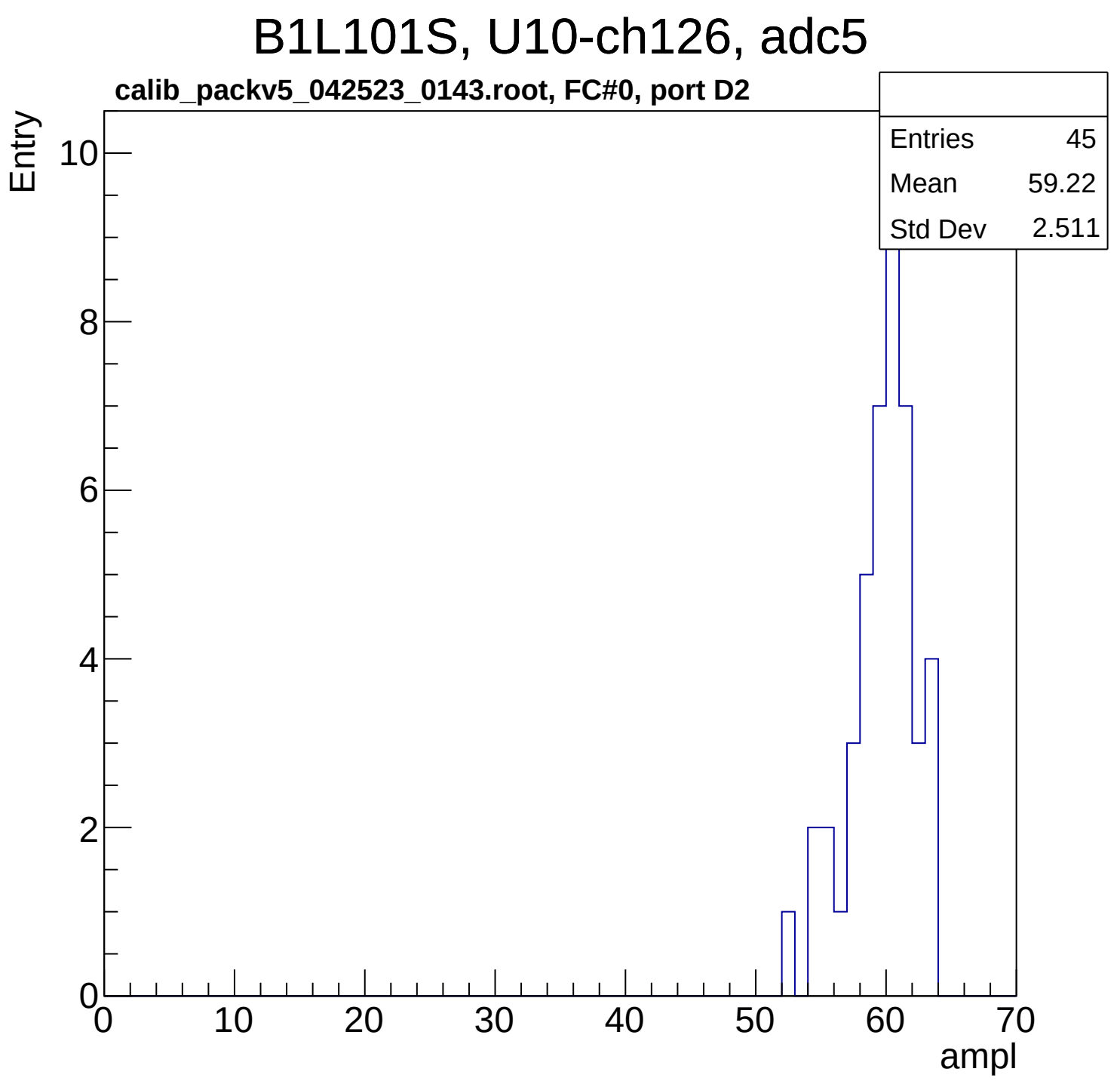

B1L101S, U10-ch126, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 25.88
Std Dev 8.53
Gaus mean : 27.5781
Gaus Width: 3.6646
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

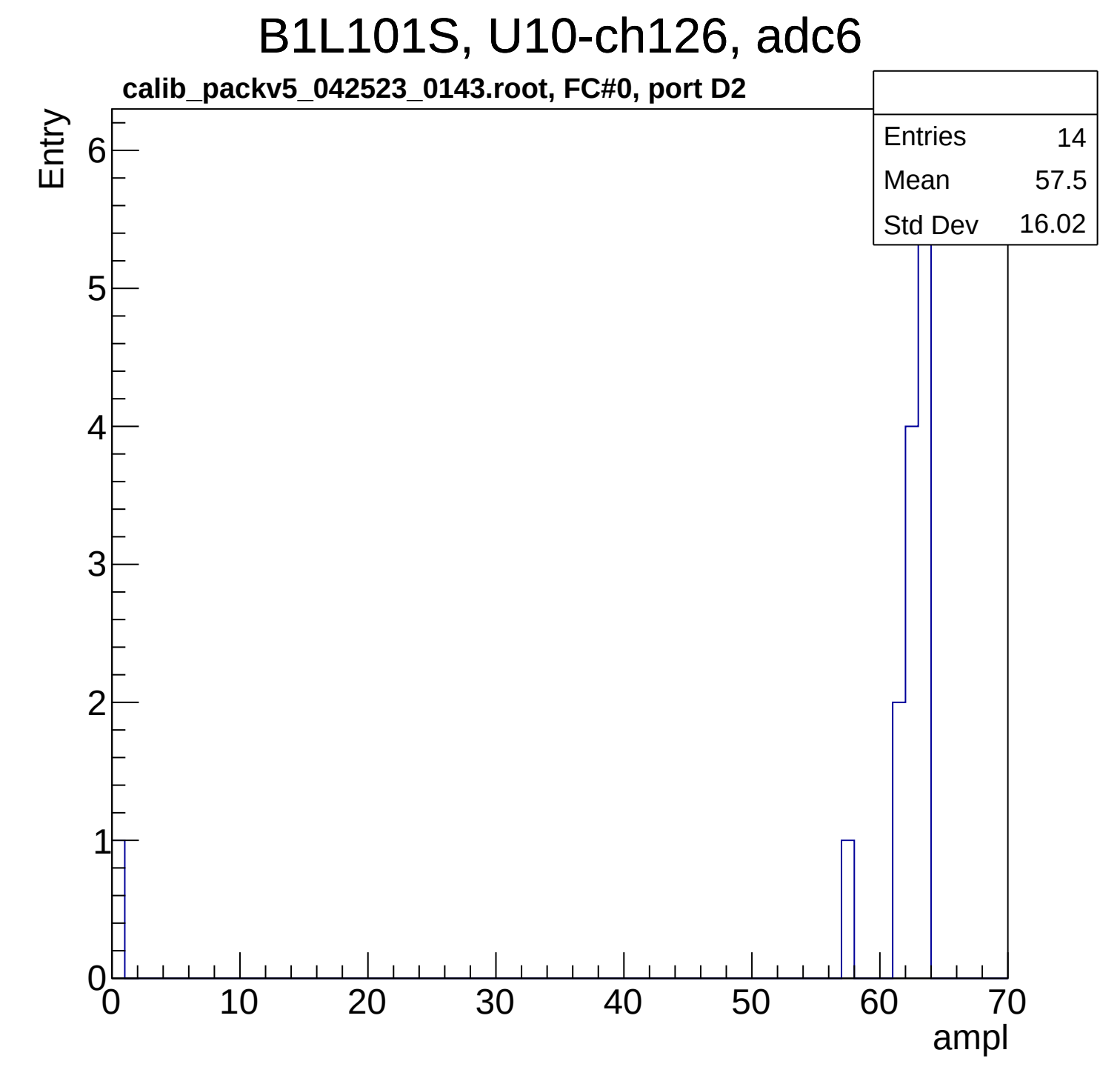

B1L101S, U10-ch126, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 33.32
Std Dev 5.745
Gaus mean : 33.7851
Gaus Width: 3.4441
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

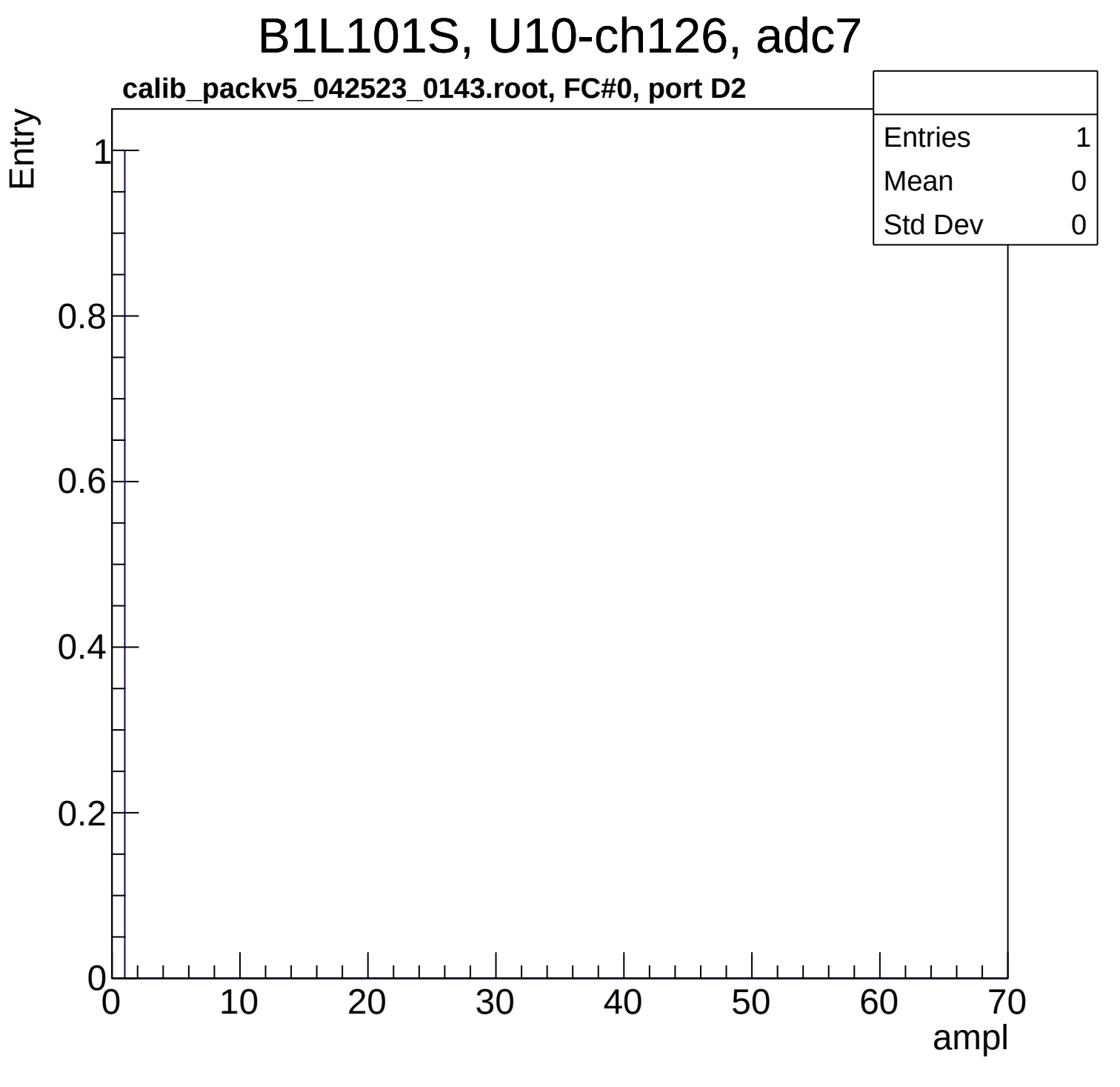

B1L101S, U10-ch126, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 39.24
Std Dev 3.398
Gaus mean : 39.7420
Gaus Width: 3.6250
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

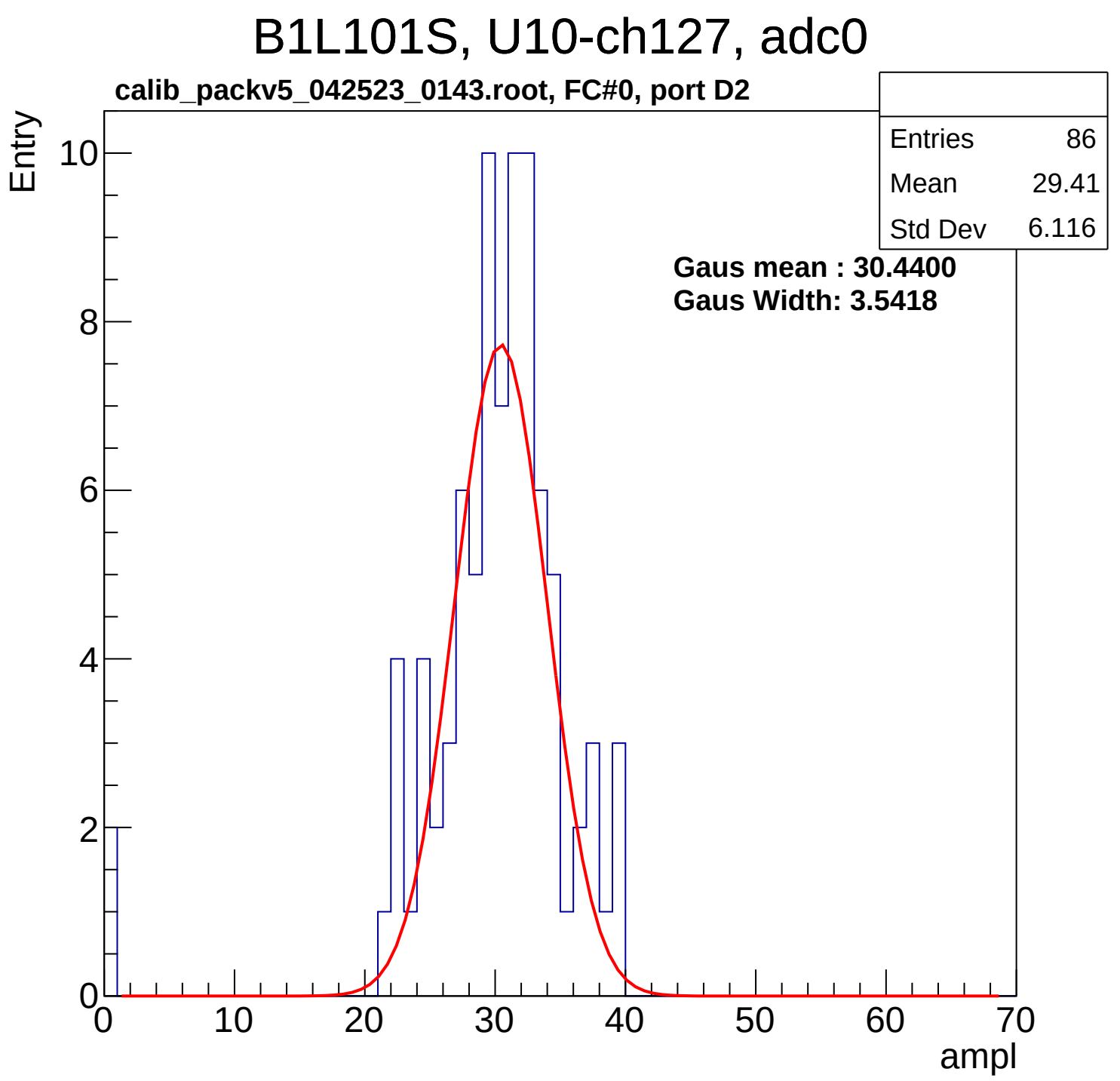

B1L101S, U10-ch126, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 85
Mean 47.11
Std Dev 3.601
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

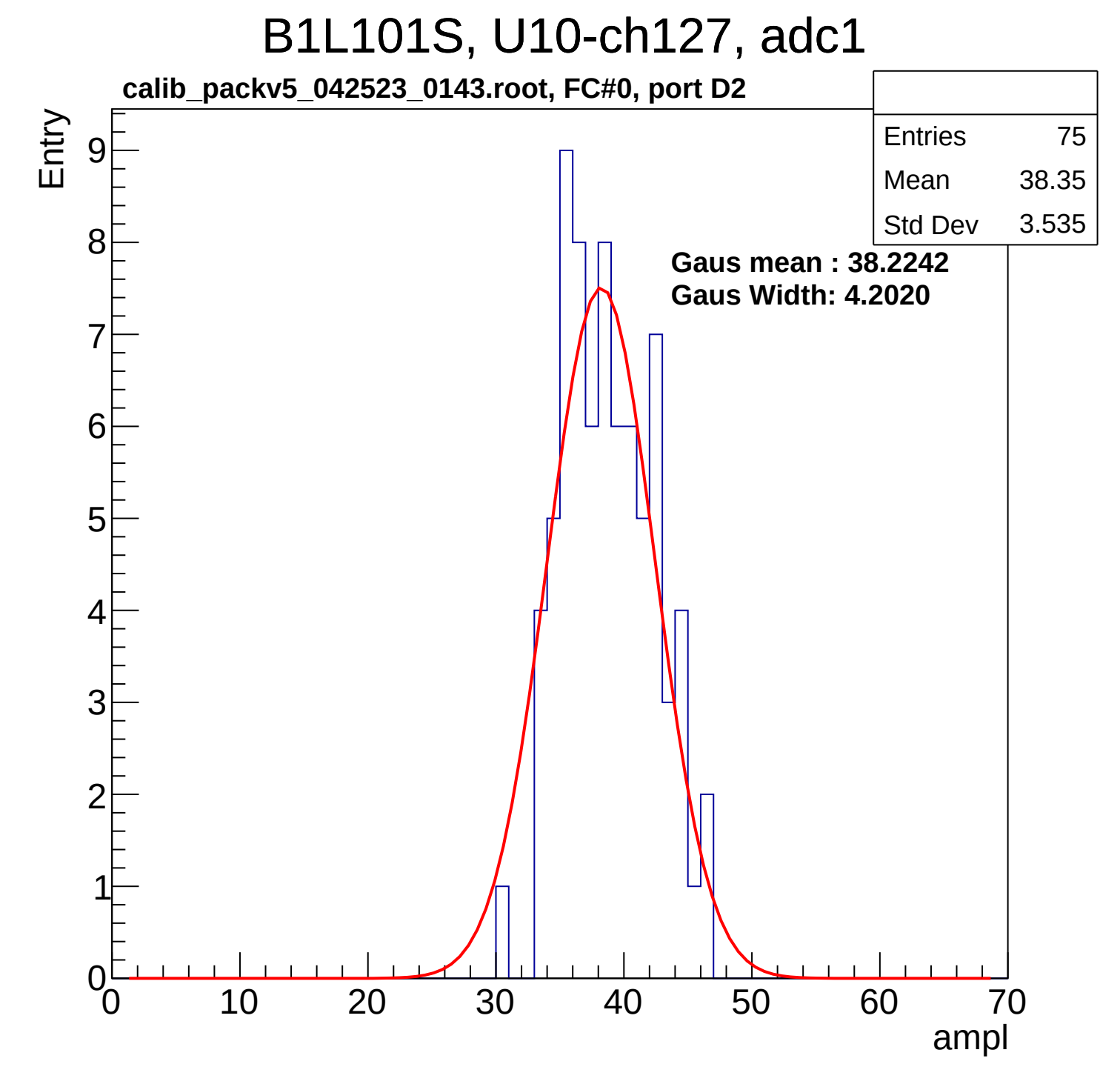

B1L101S, U10-ch126, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 54.4
Std Dev 3.72
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

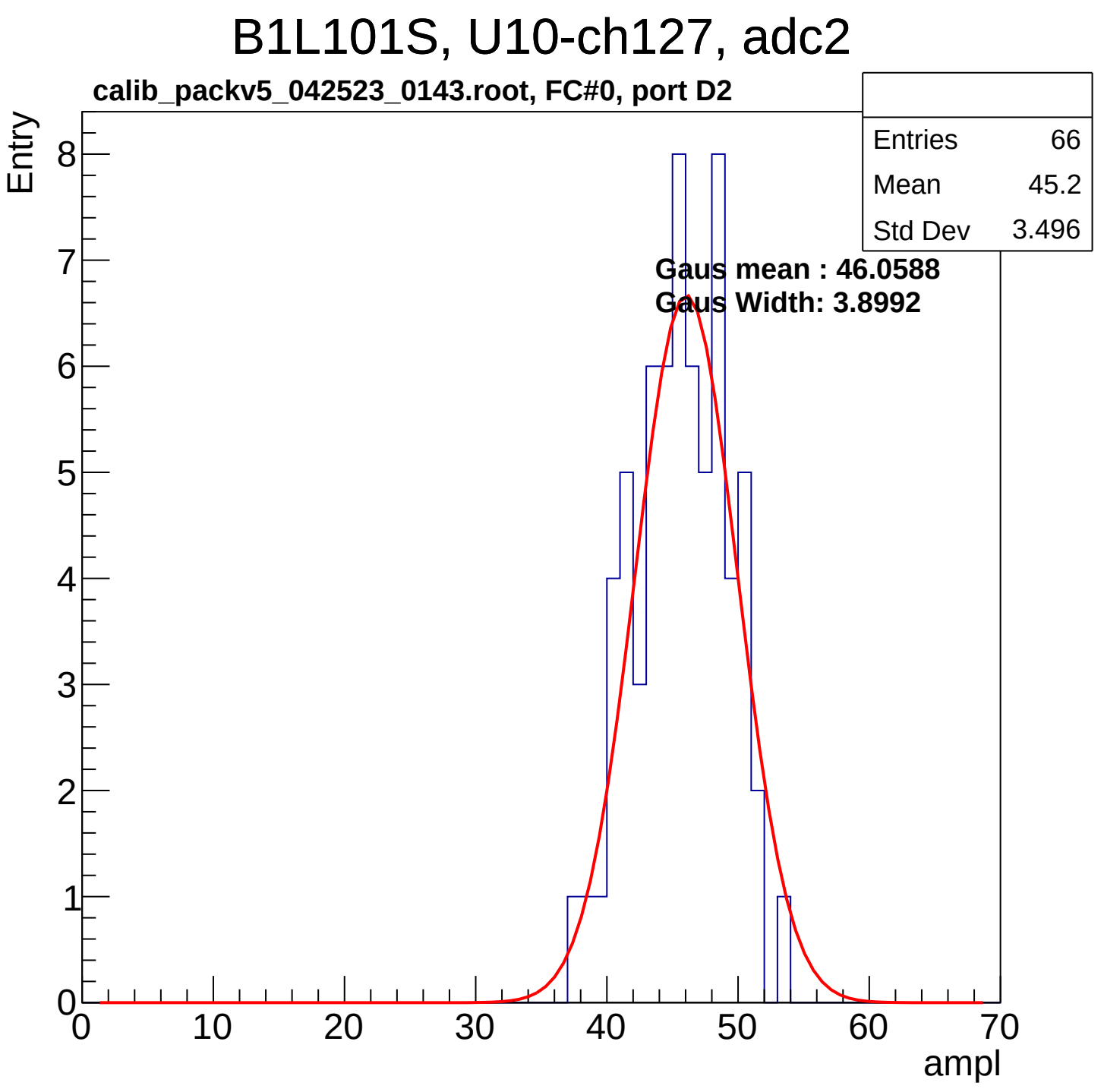

B1L101S, U10-ch126, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 59.22
Std Dev 2.511
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

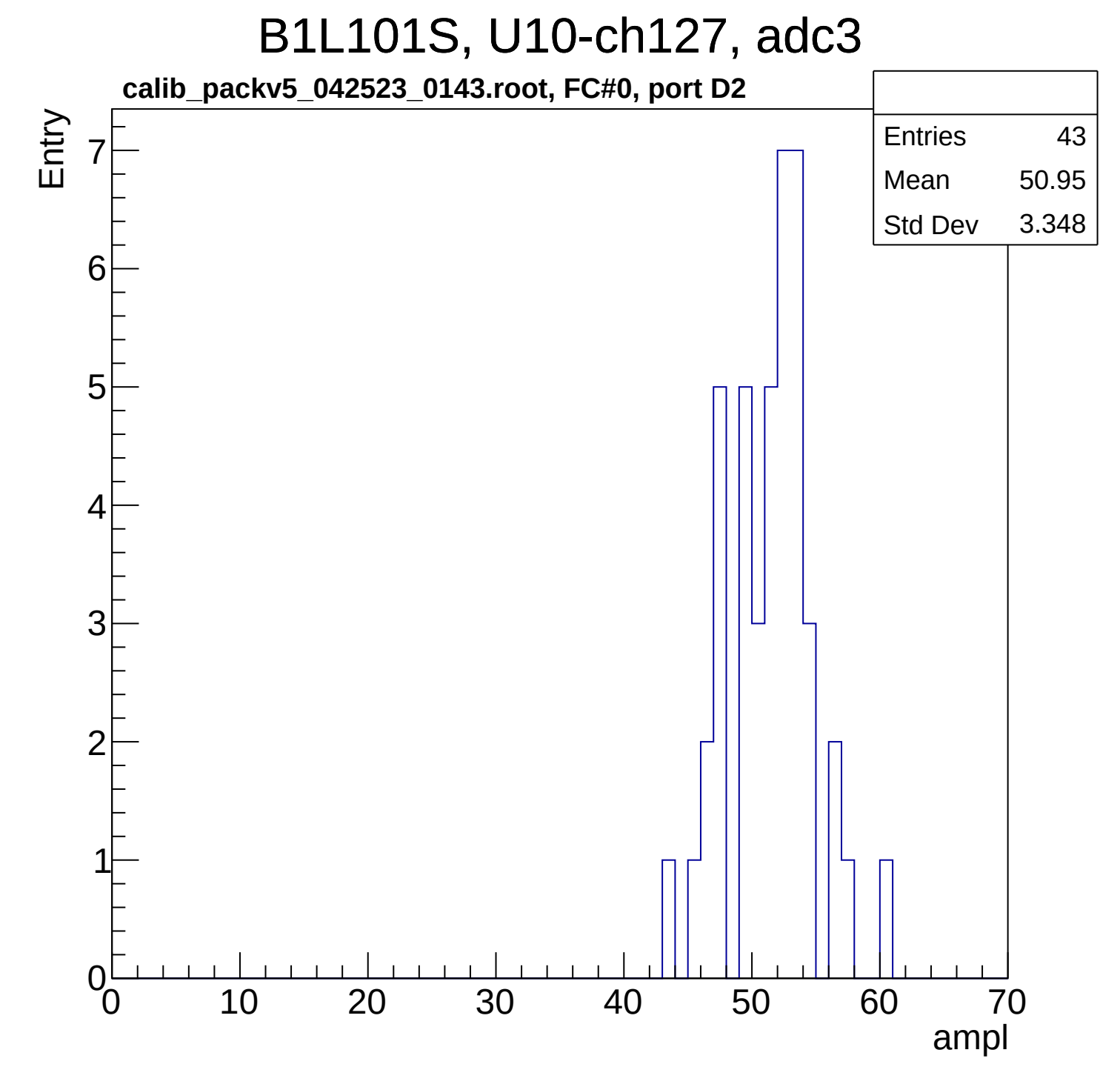

B1L101S, U10-ch126, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 14
Mean 57.5
Std Dev 16.02
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

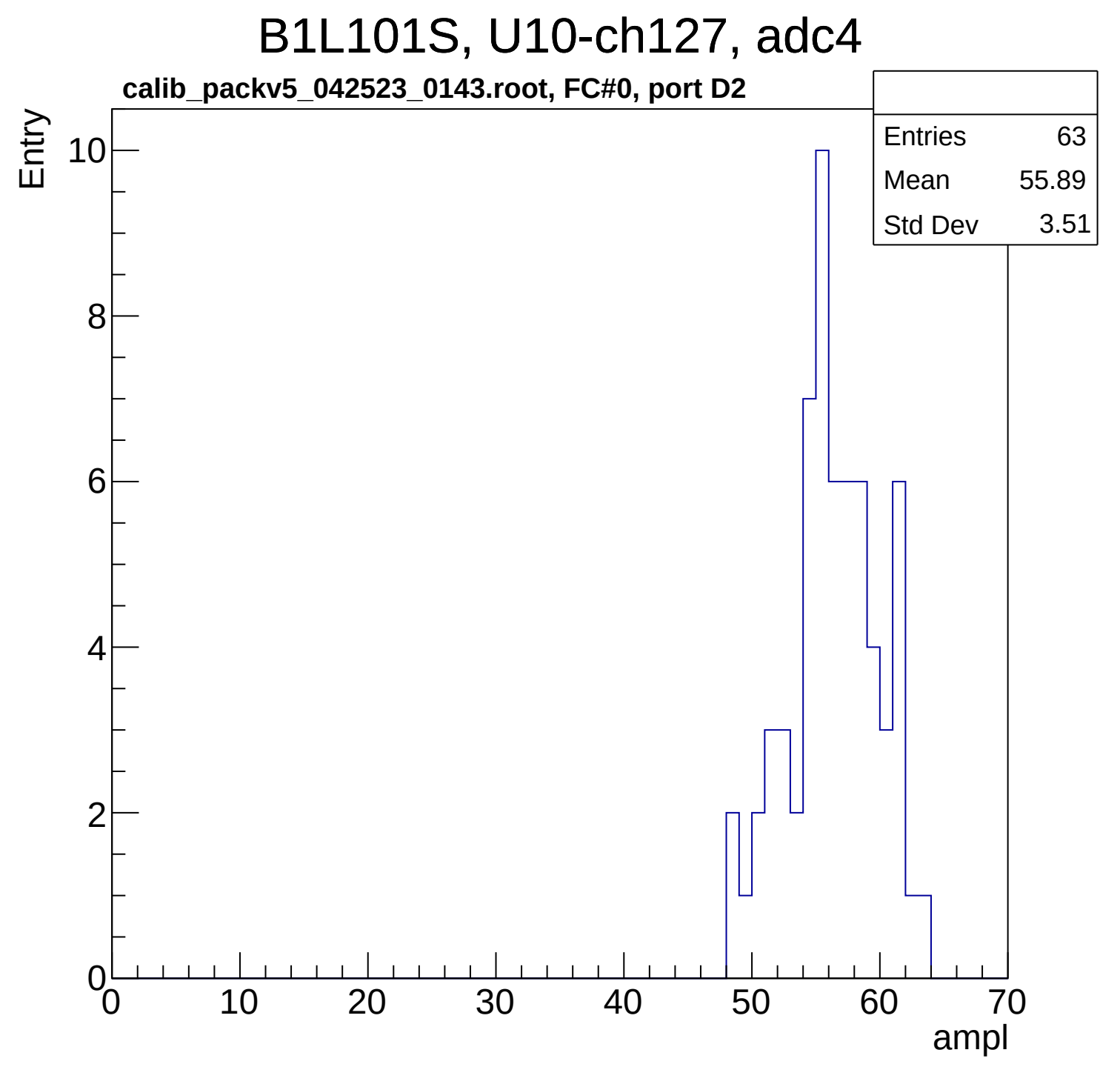

B1L101S, U10-ch126, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

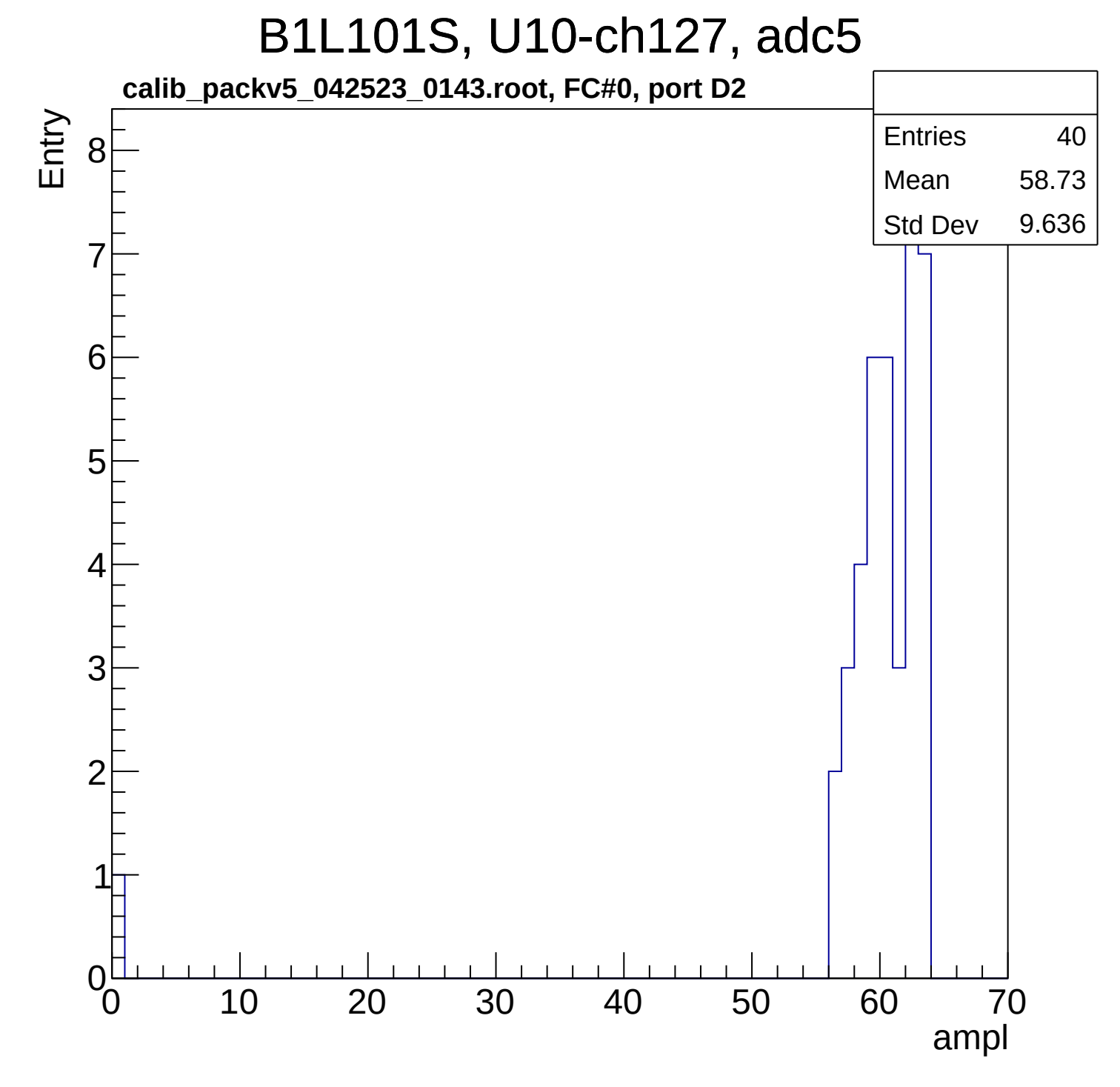

B1L101S, U10-ch127, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 86
Mean 29.41
Std Dev 6.116
Gaus mean : 30.4400
Gaus Width: 3.5418
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

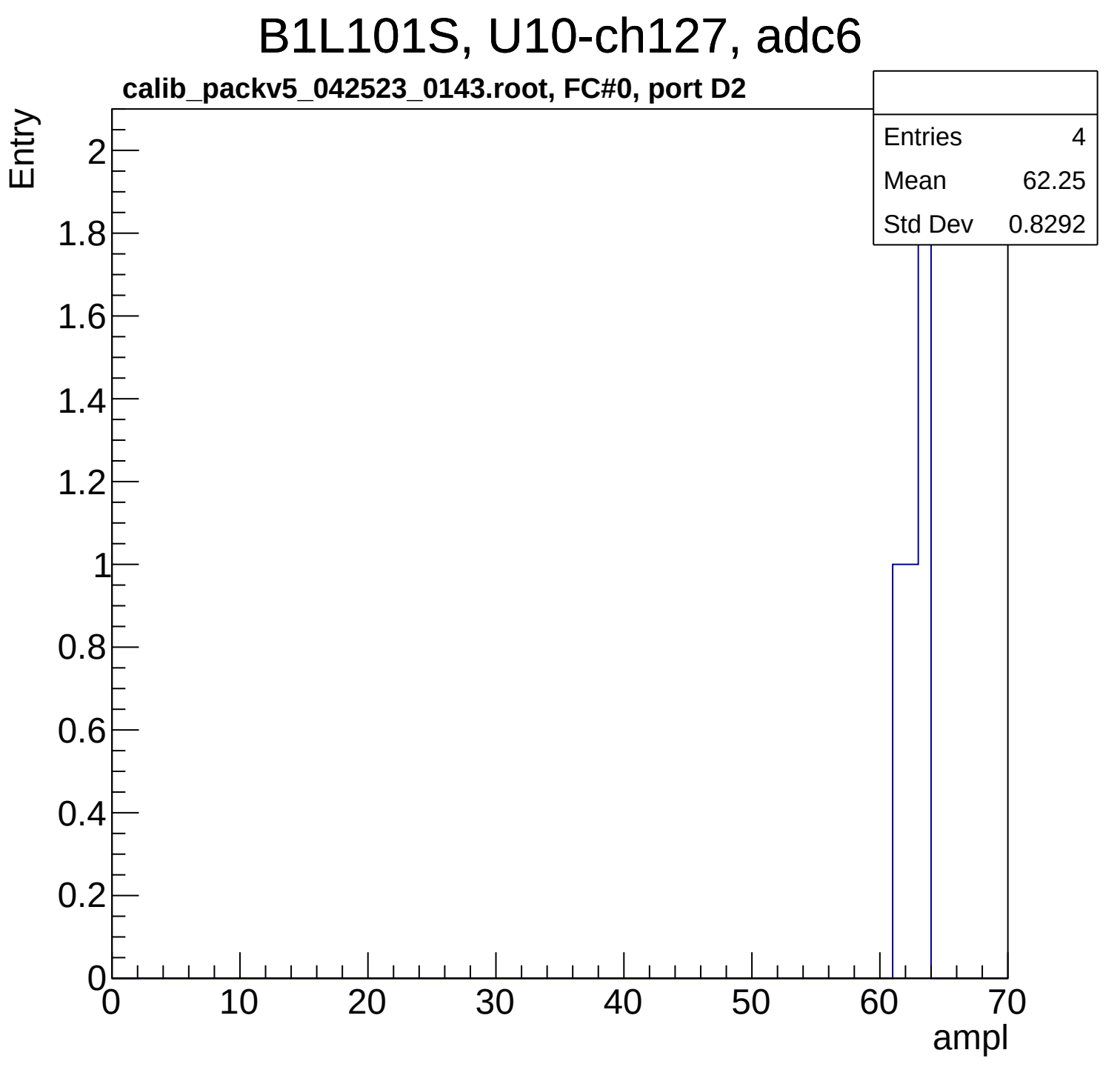

B1L101S, U10-ch127, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 38.35
Std Dev 3.535
Gaus mean : 38.2242
Gaus Width: 4.2020
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

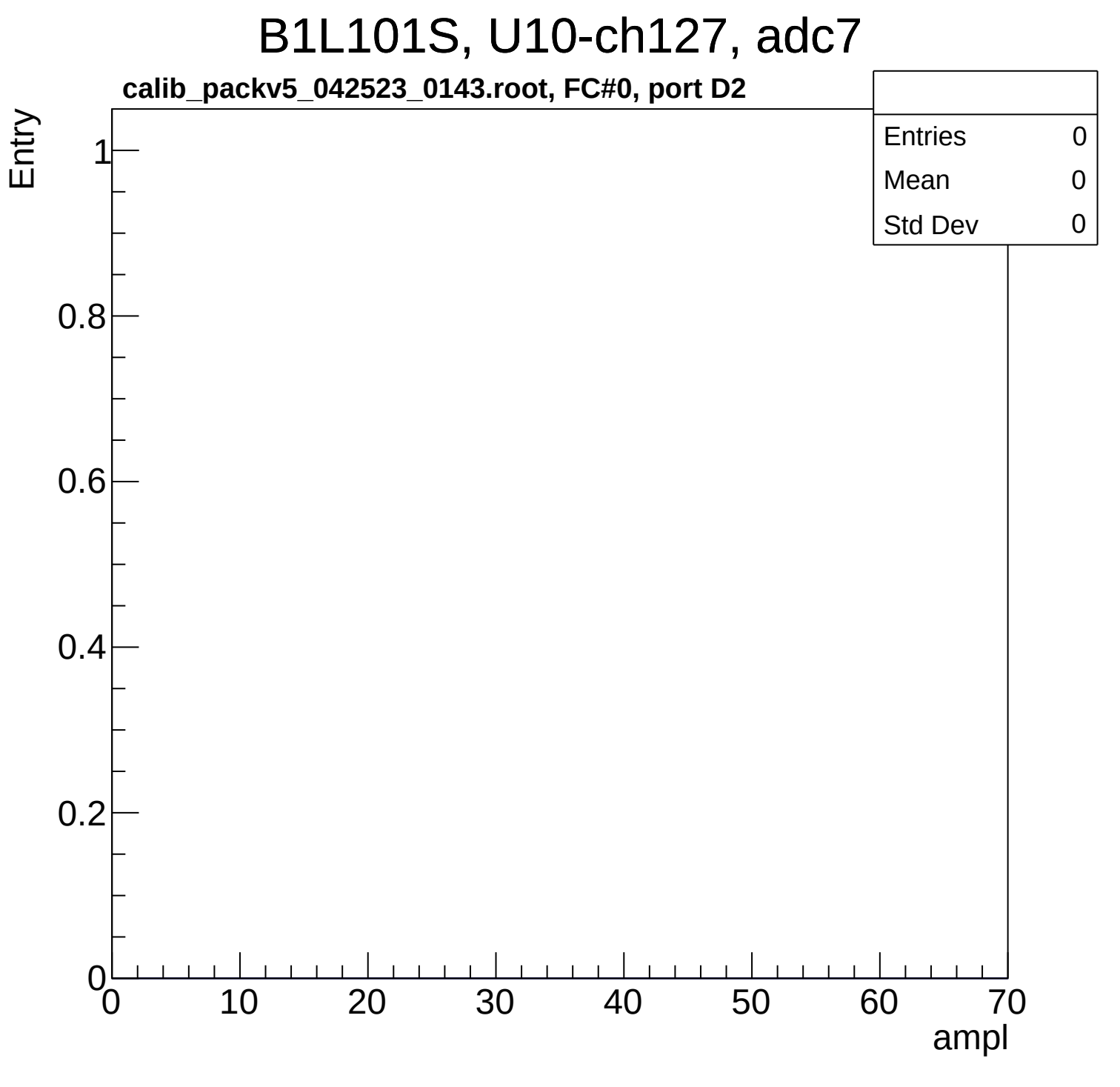

B1L101S, U10-ch127, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 45.2
Std Dev 3.496
Gaus mean : 46.0588
Gaus Width: 3.8992
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

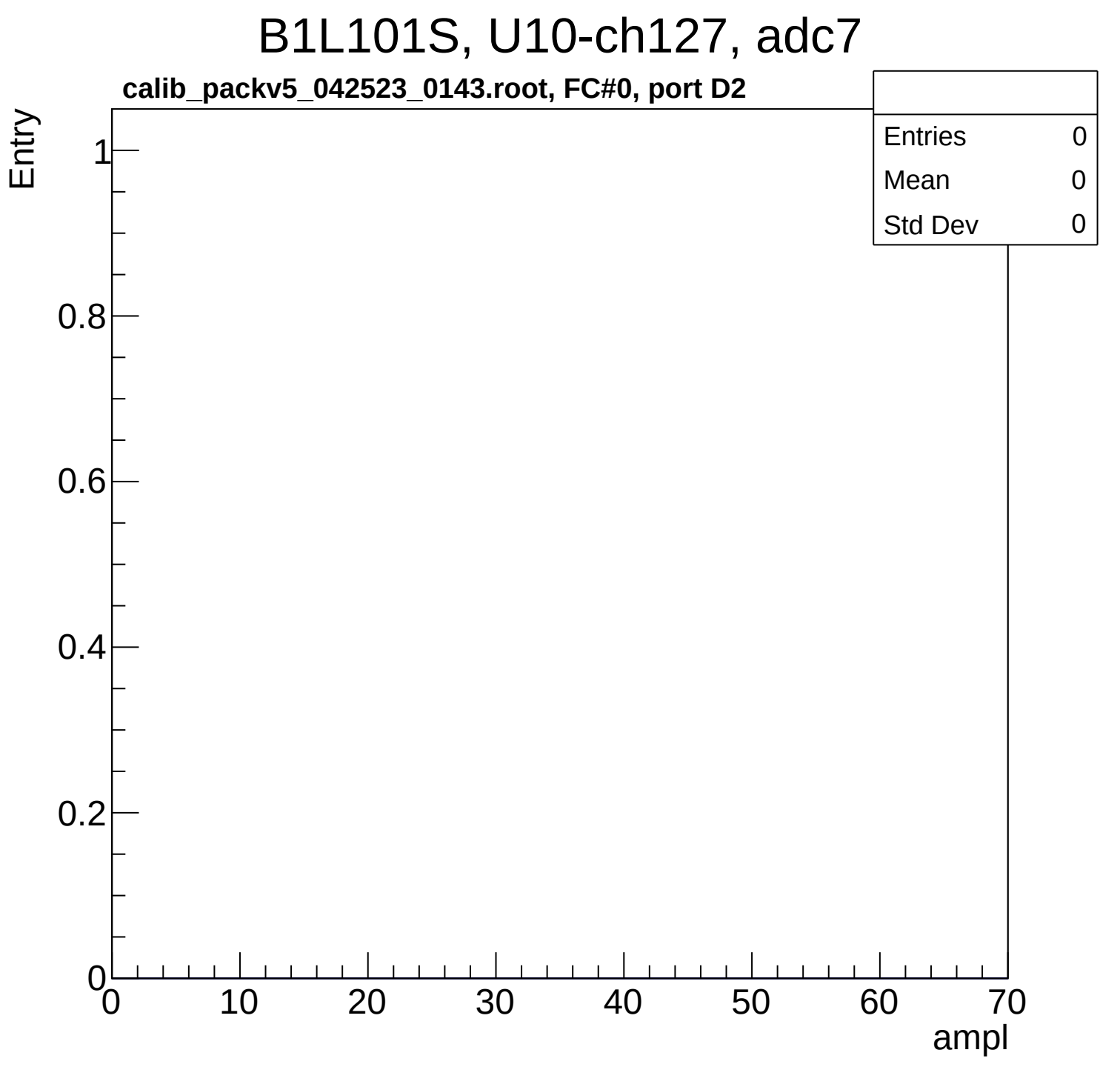

B1L101S, U10-ch127, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 43
Mean 50.95
Std Dev 3.348
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U10-ch127, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 55.89
Std Dev 3.51
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U10-ch127, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 40
Mean 58.73
Std Dev 9.636
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U10-ch127, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U10-ch127, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U10-ch127, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl