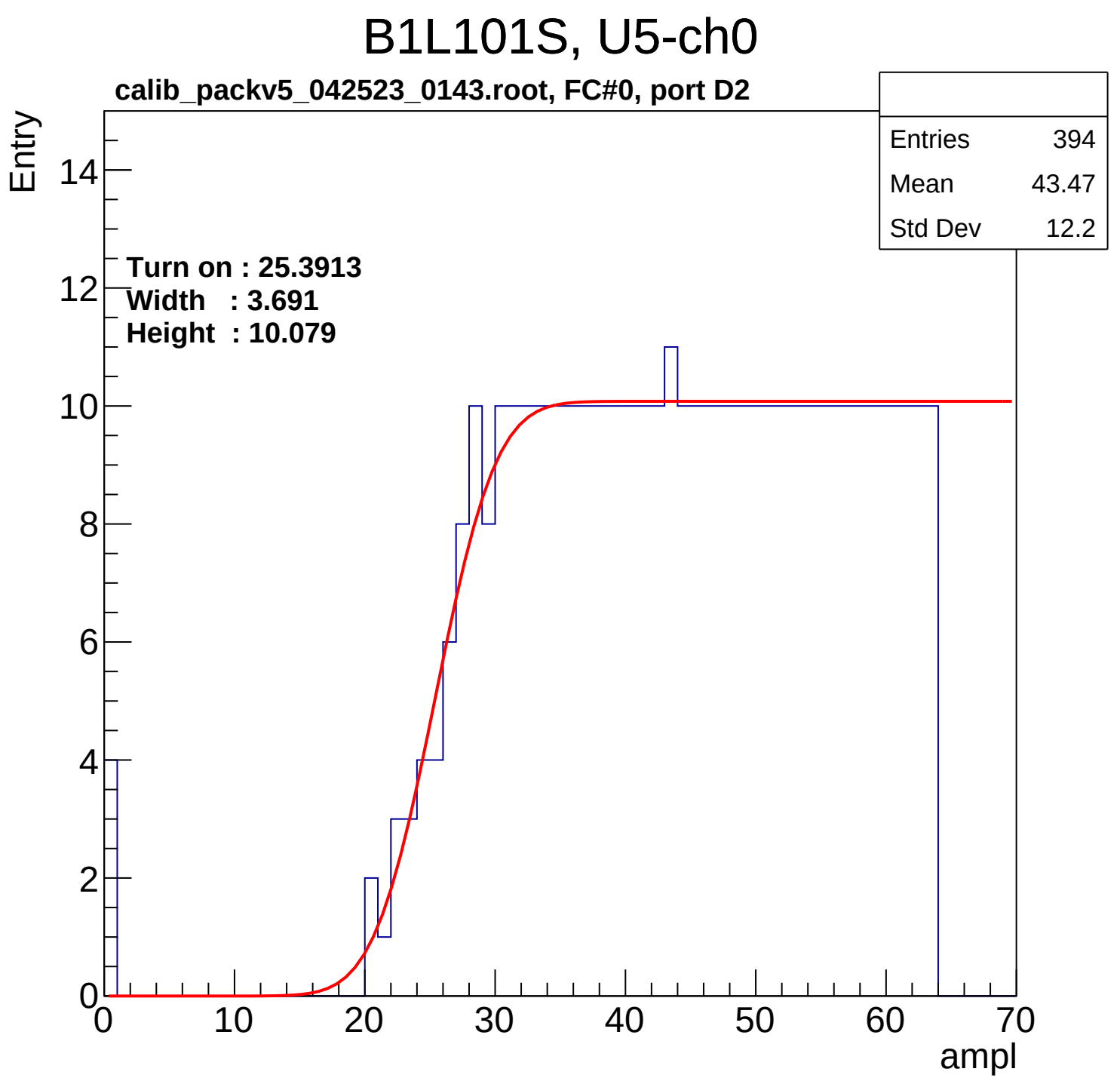
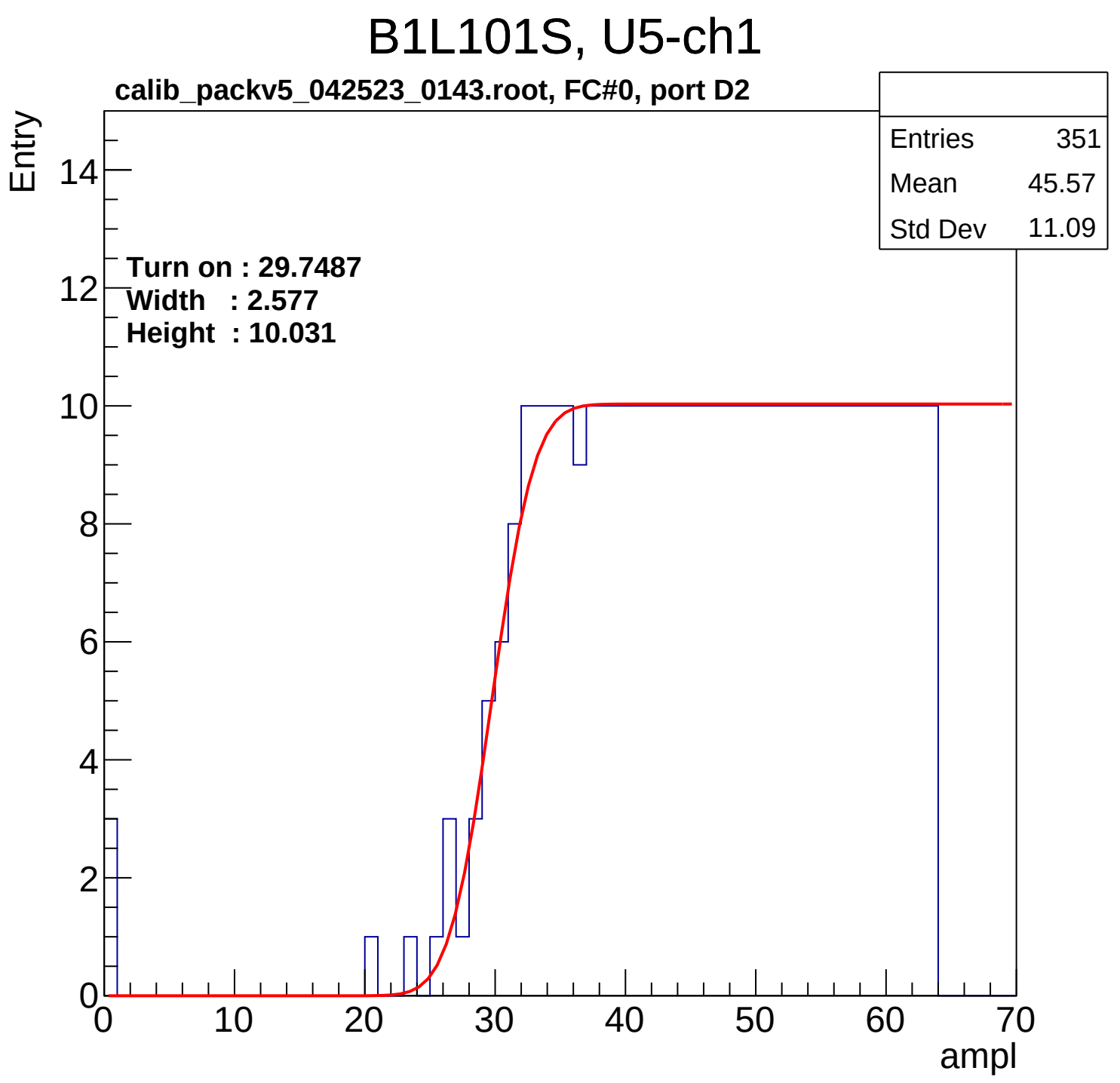
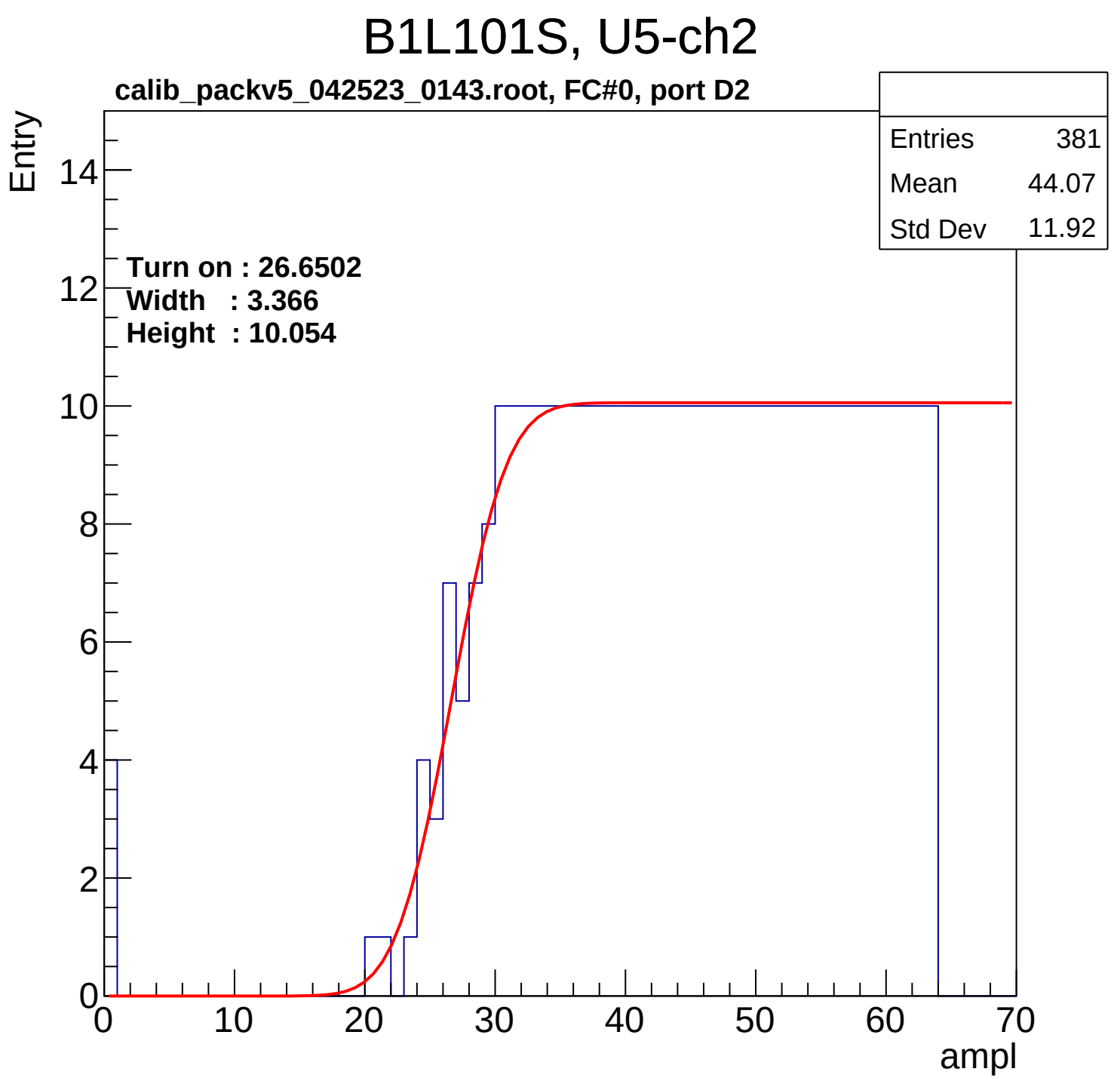
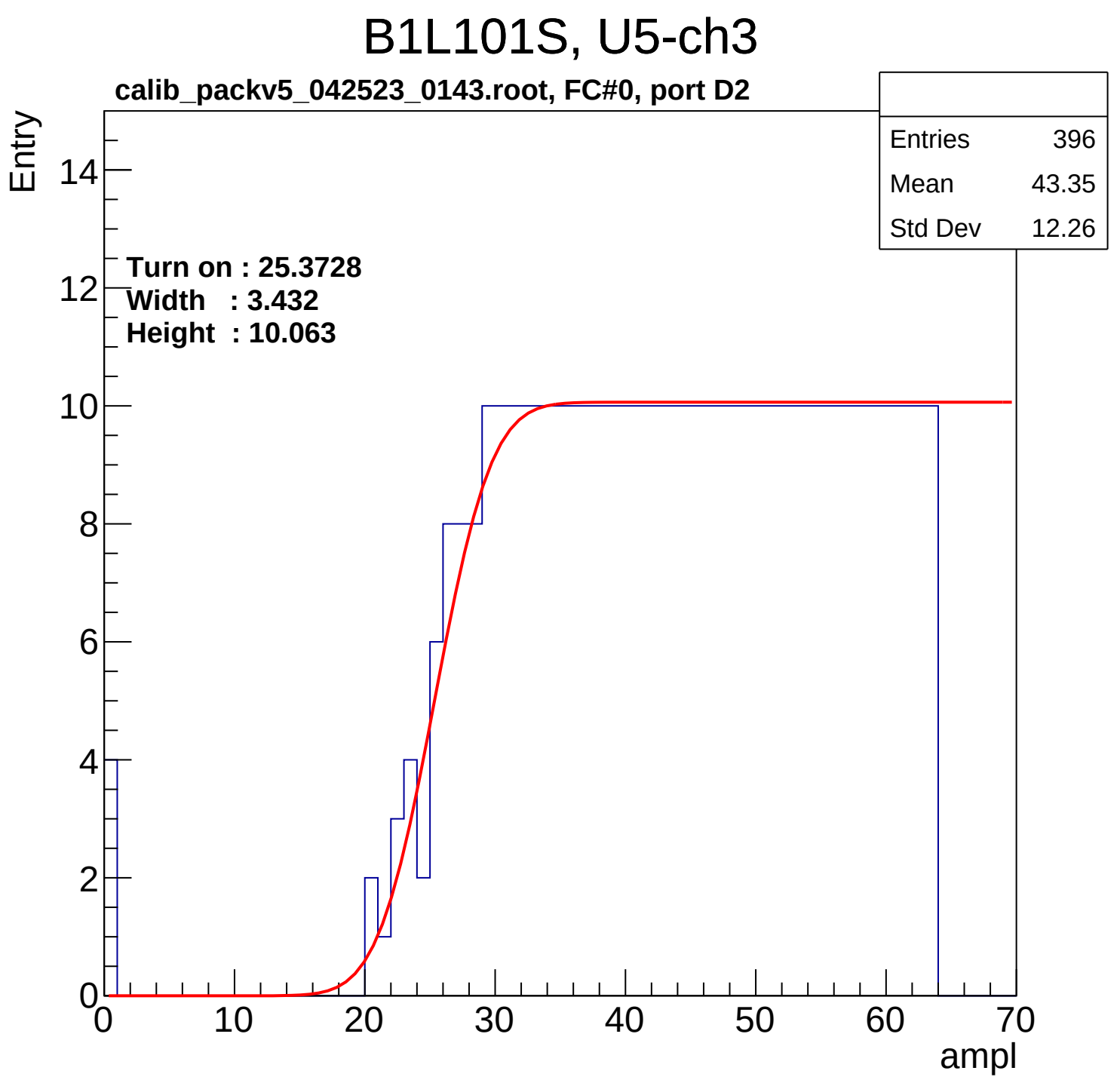
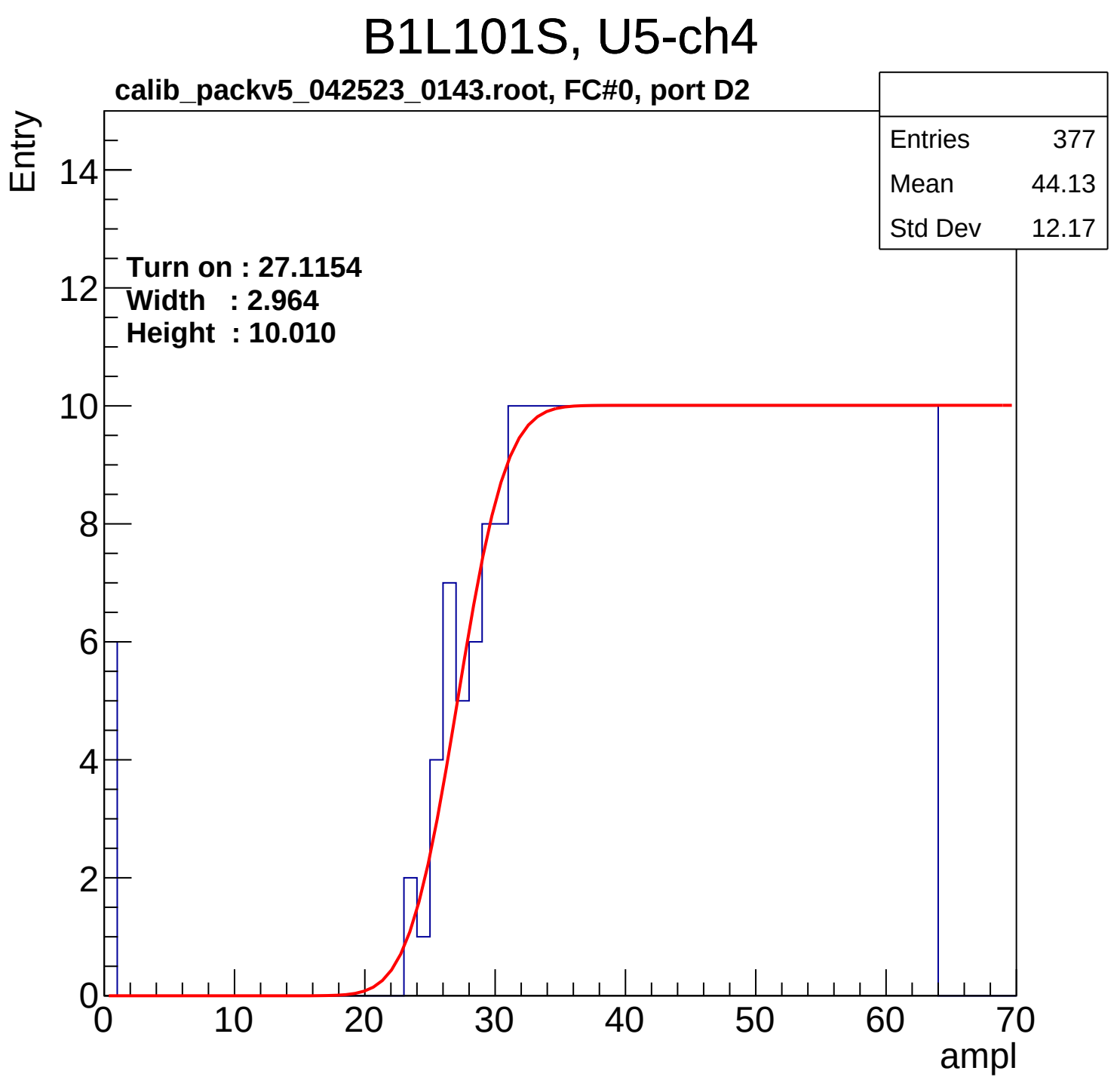
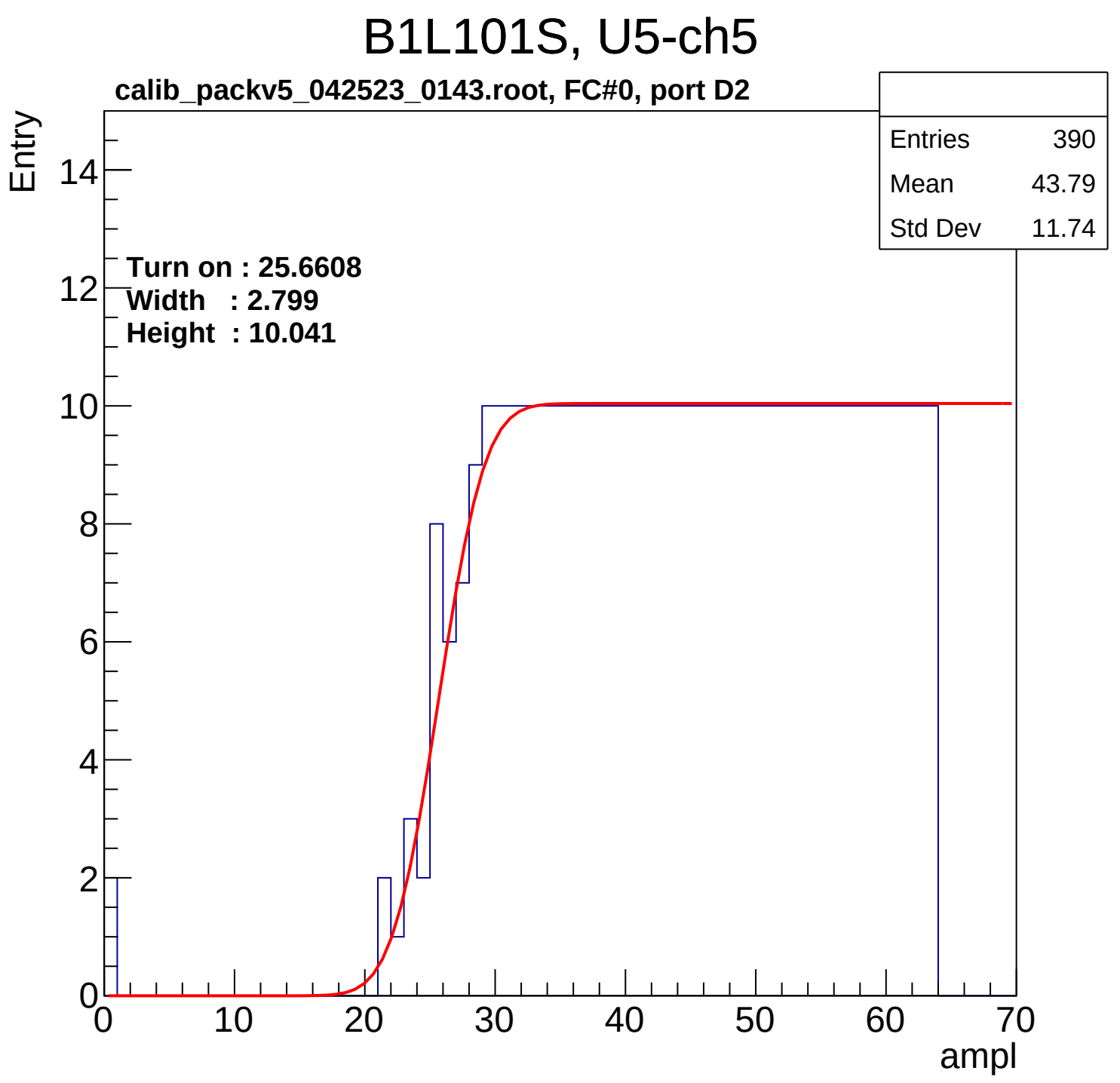

B1L101S, U5-ch0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 394
Mean 43.47
Std Dev 12.2
Turn on : 25.3913
Width : 3.691
Height : 10.079
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

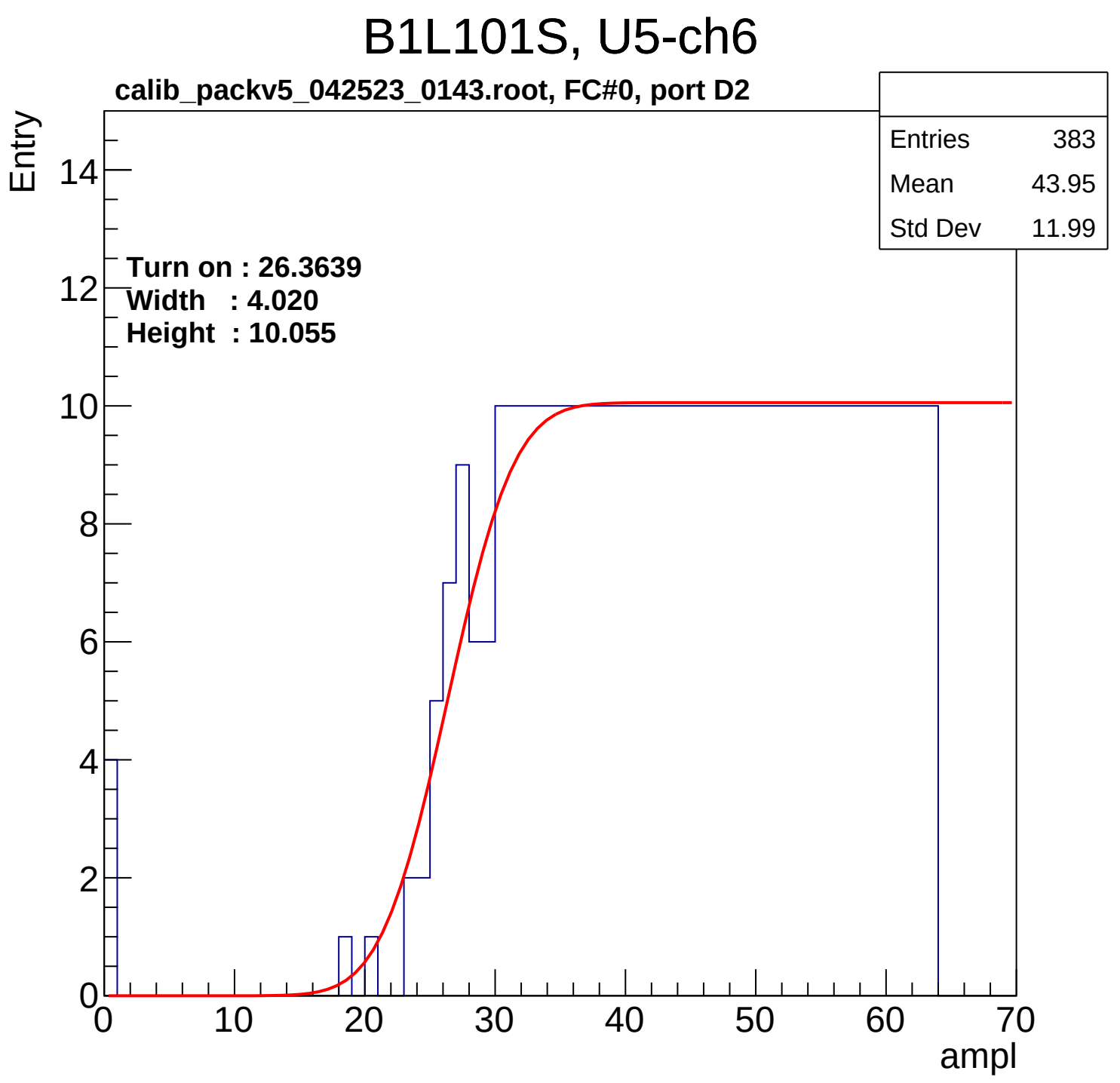

B1L101S, U5-ch1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 351
Mean 45.57
Std Dev 11.09
Turn on : 29.7487
Width : 2.577
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

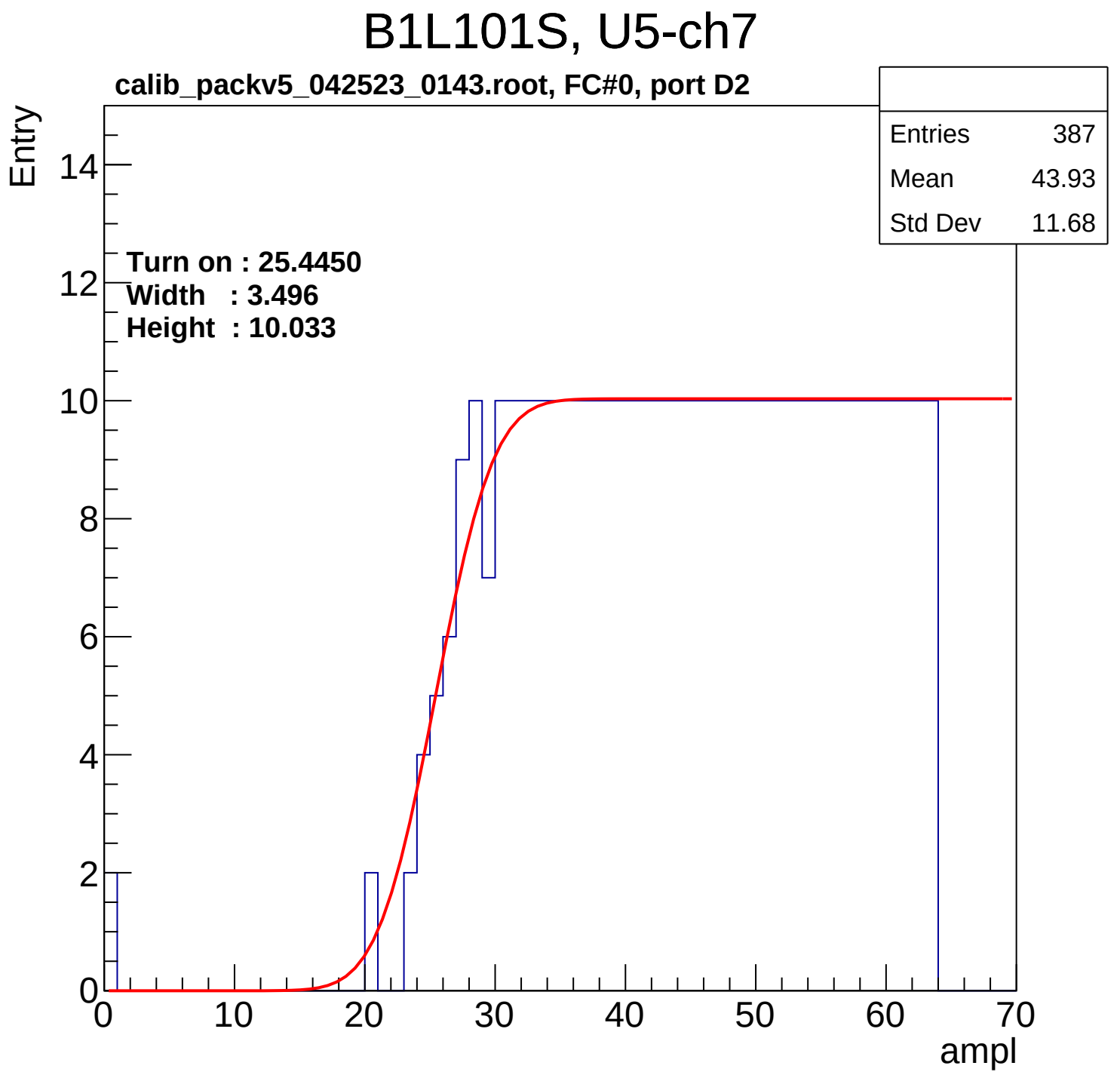

B1L101S, U5-ch2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 381
Mean 44.07
Std Dev 11.92
Turn on : 26.6502
Width : 3.366
Height : 10.054
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

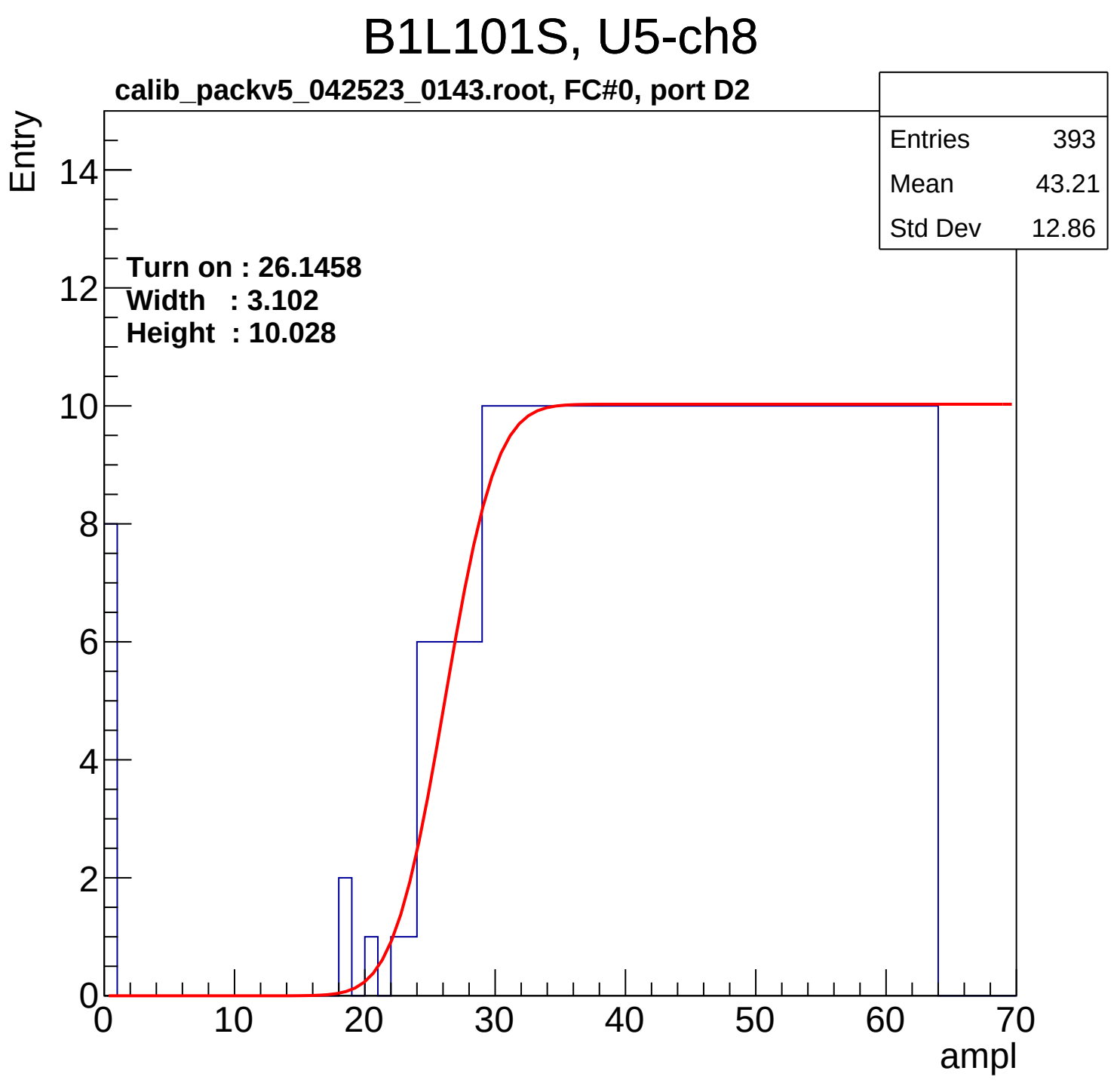

B1L101S, U5-ch3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 396
Mean 43.35
Std Dev 12.26
Turn on : 25.3728
Width : 3.432
Height : 10.063
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

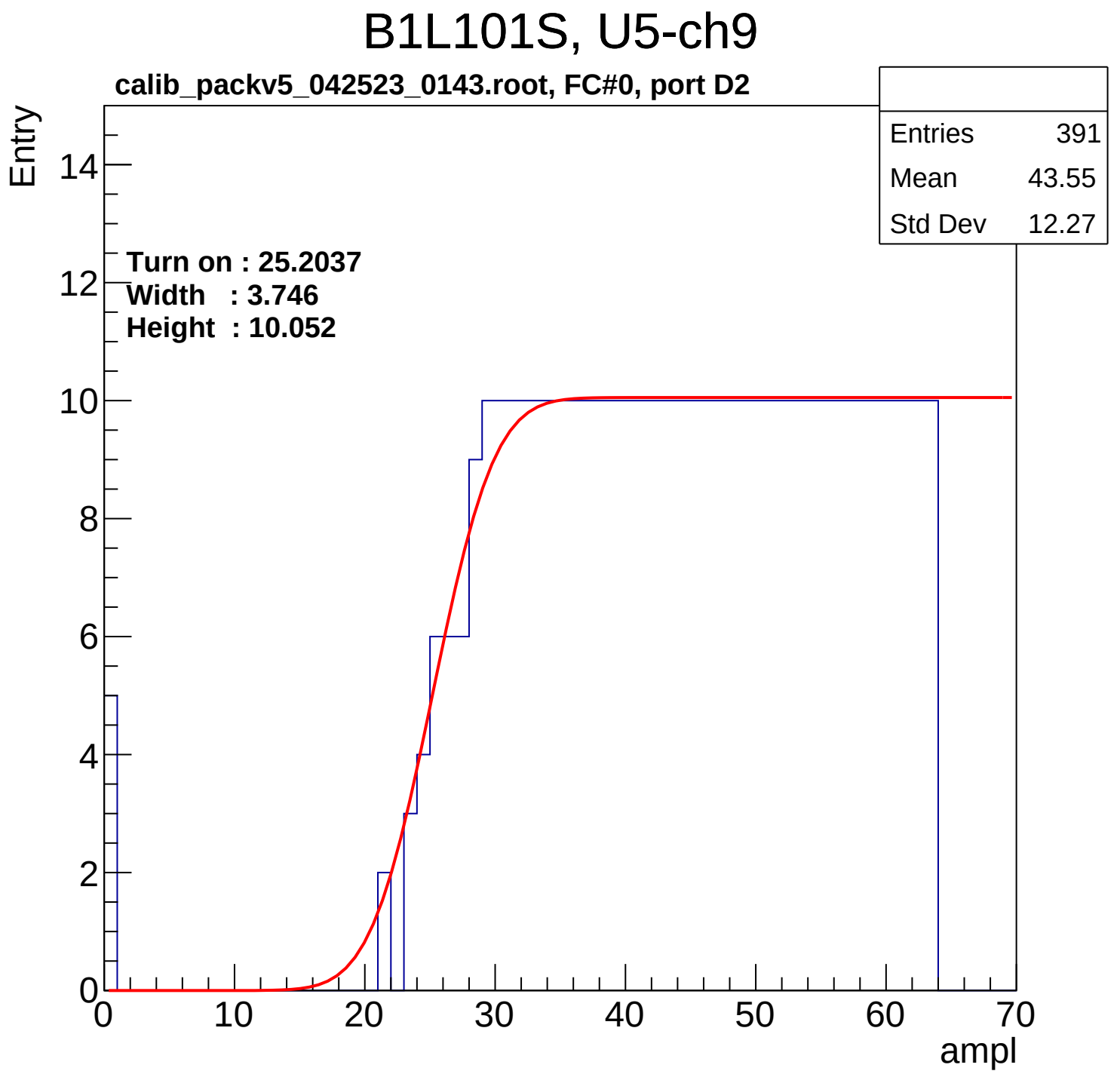

B1L101S, U5-ch4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 377
Mean 44.13
Std Dev 12.17
Turn on : 27.1154
Width : 2.964
Height : 10.010
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

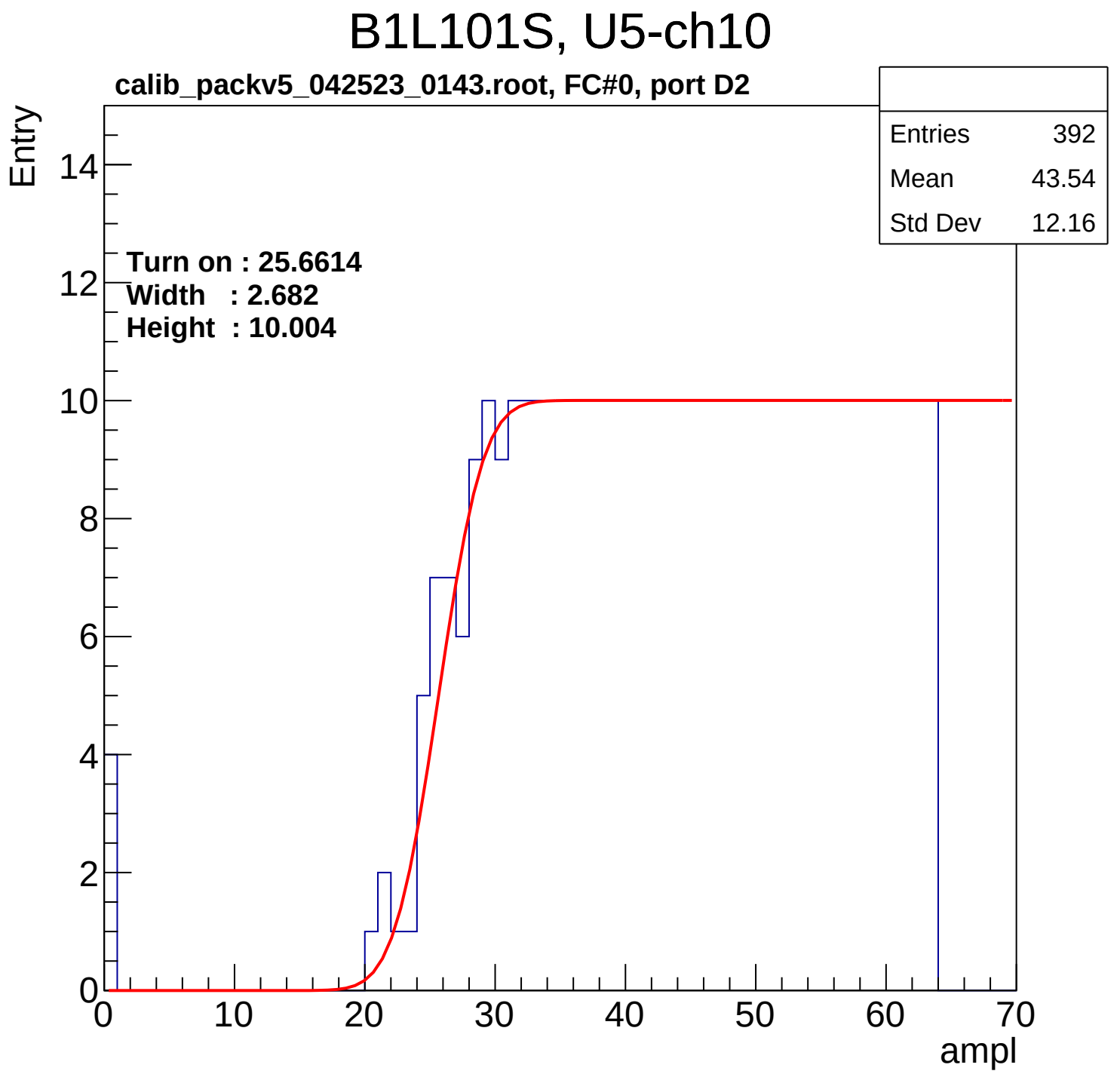

B1L101S, U5-ch5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 390
Mean 43.79
Std Dev 11.74
Turn on : 25.6608
Width : 2.799
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

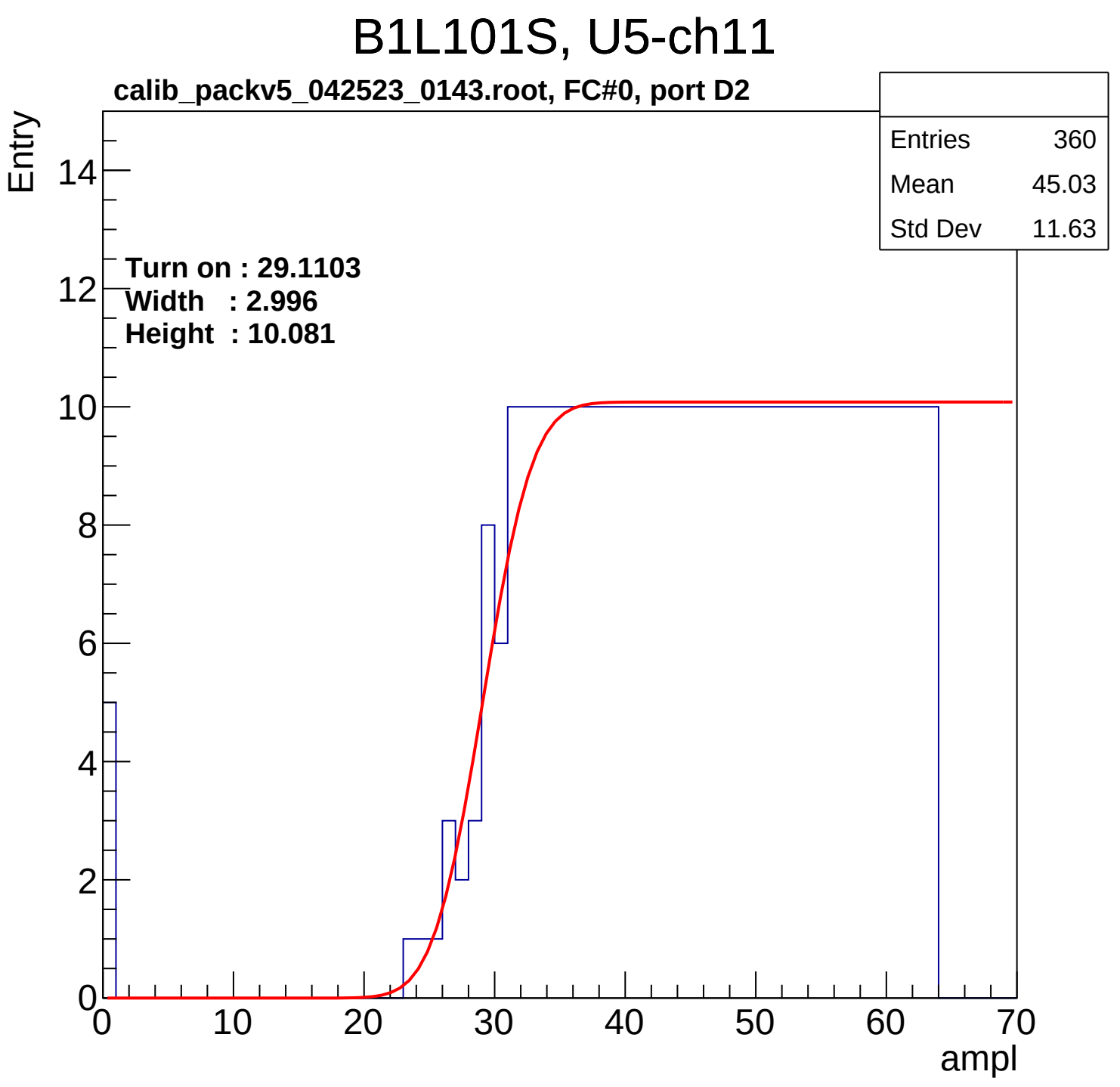

B1L101S, U5-ch6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 43.95
Std Dev 11.99
Turn on : 26.3639
Width : 4.020
Height : 10.055
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

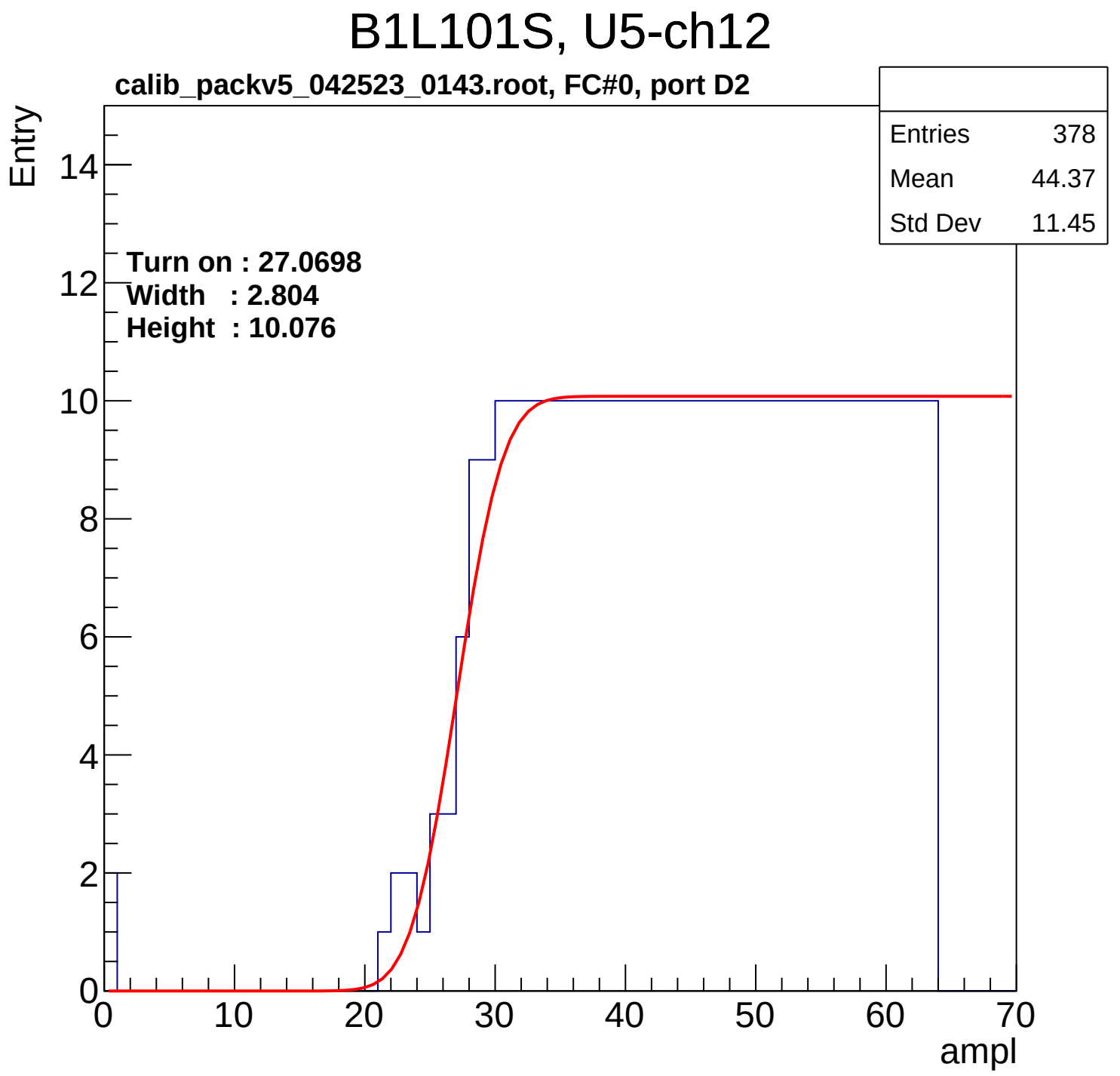

B1L101S, U5-ch7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.93
Std Dev 11.68
Turn on : 25.4450
Width : 3.496
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

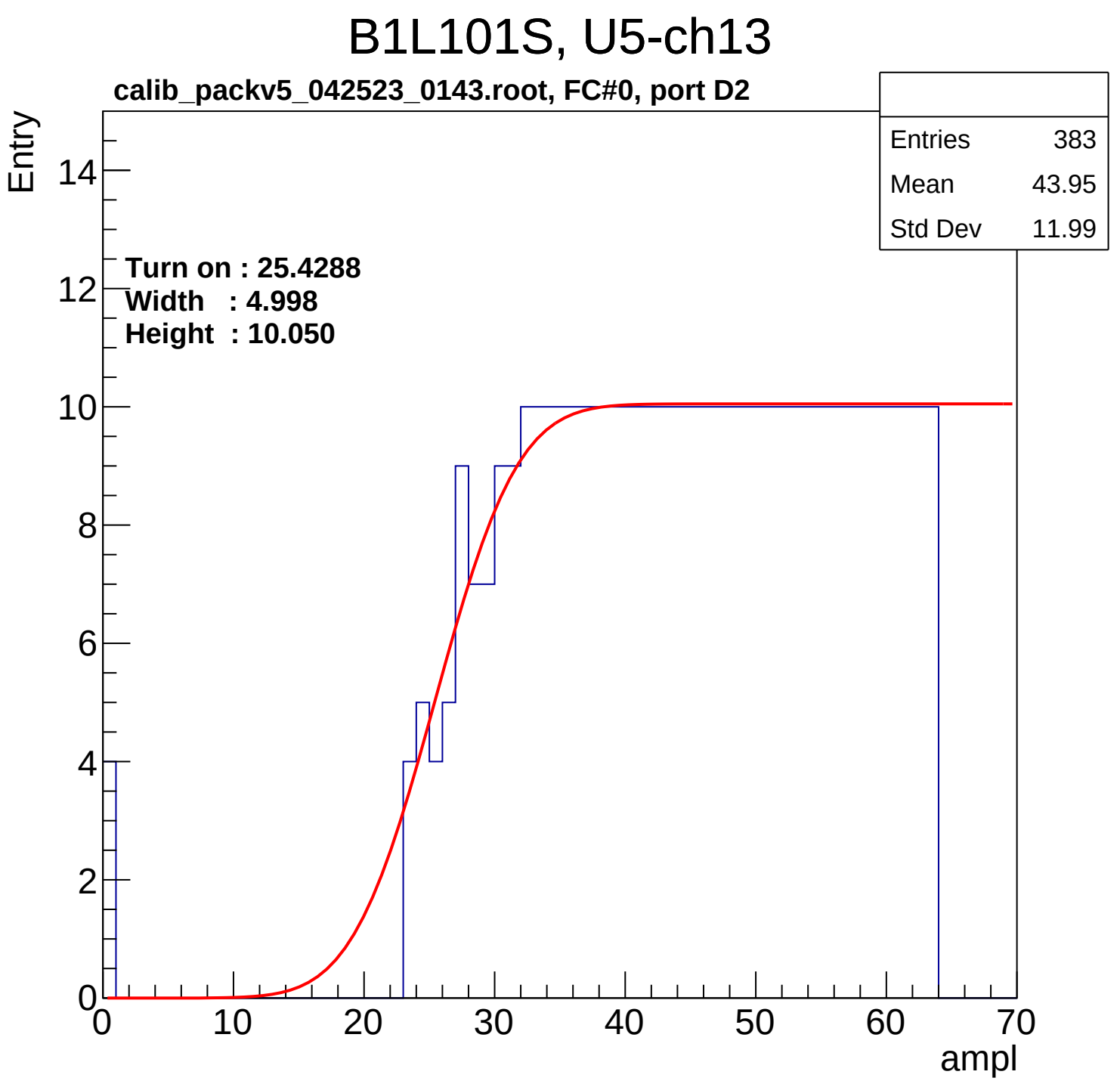

B1L101S, U5-ch8
calib_packv5_042523_0143.root, FC#0, port D2
Entries 393
Mean 43.21
Std Dev 12.86
Turn on : 26.1458
Width : 3.102
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

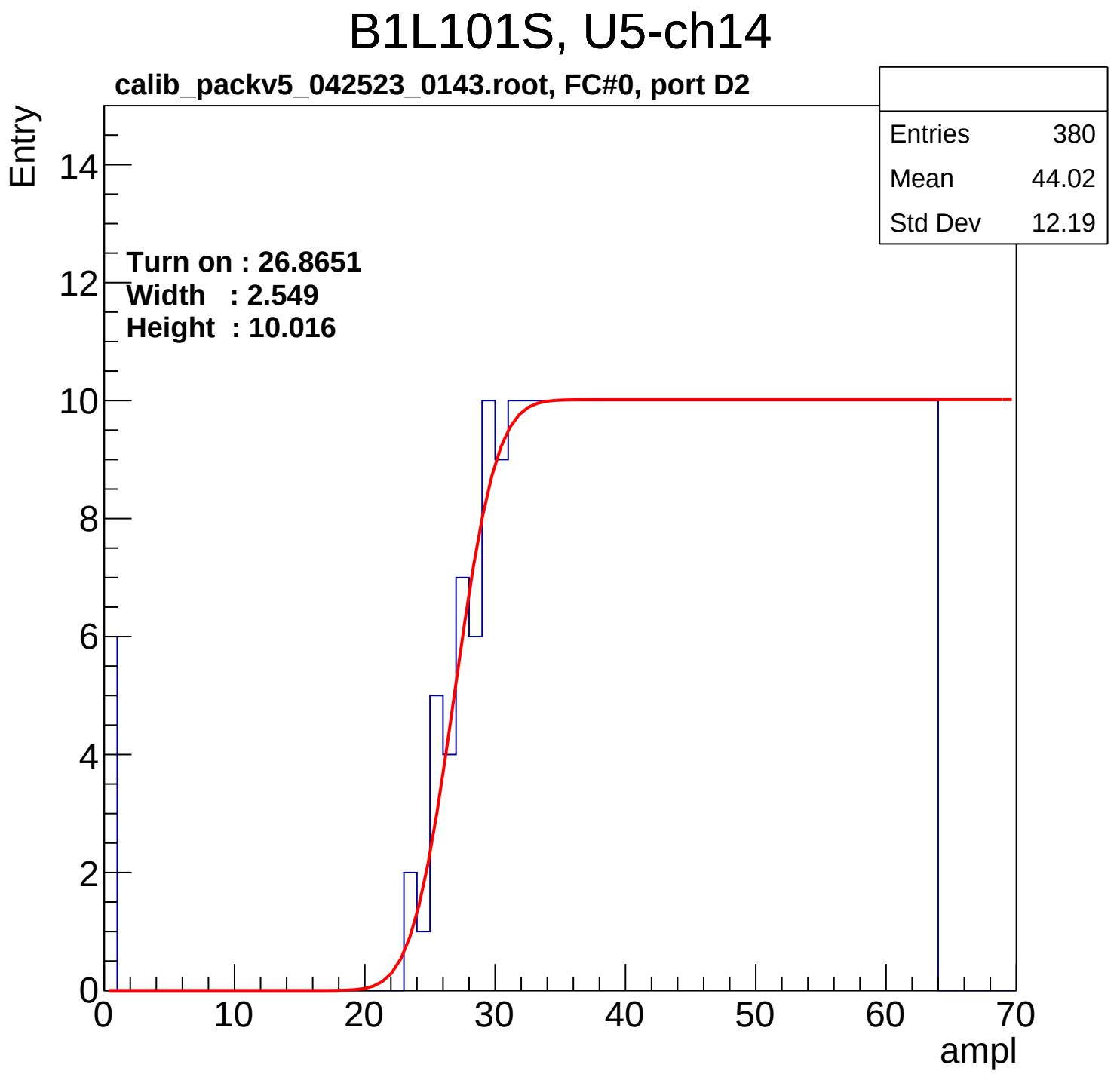

B1L101S, U5-ch9
calib_packv5_042523_0143.root, FC#0, port D2
Entries 391
Mean 43.55
Std Dev 12.27
Turn on : 25.2037
Width : 3.746
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

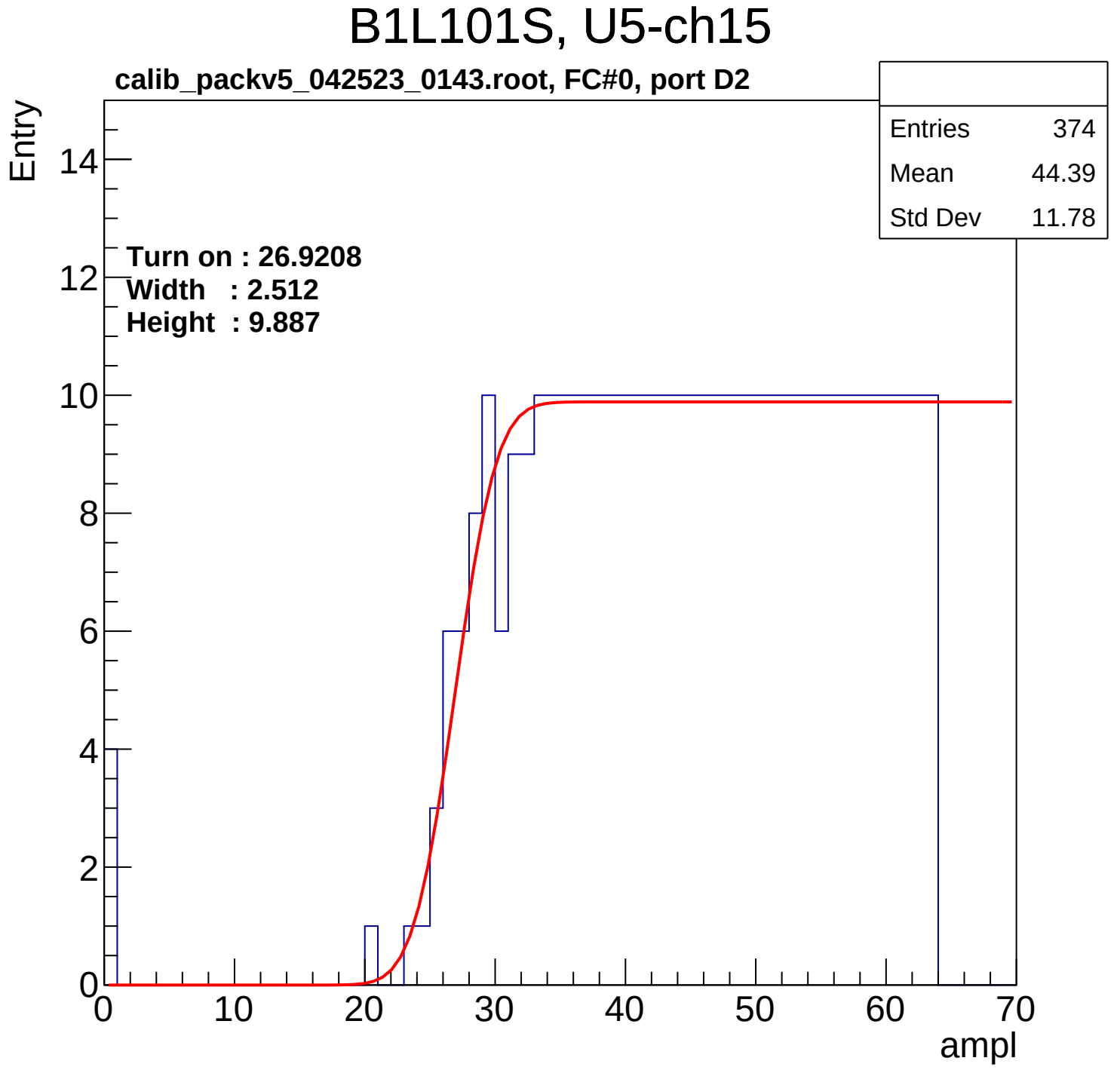

B1L101S, U5-ch10
calib_packv5_042523_0143.root, FC#0, port D2
Entries 392
Mean 43.54
Std Dev 12.16
Turn on : 25.6614
Width : 2.682
Height : 10.004
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

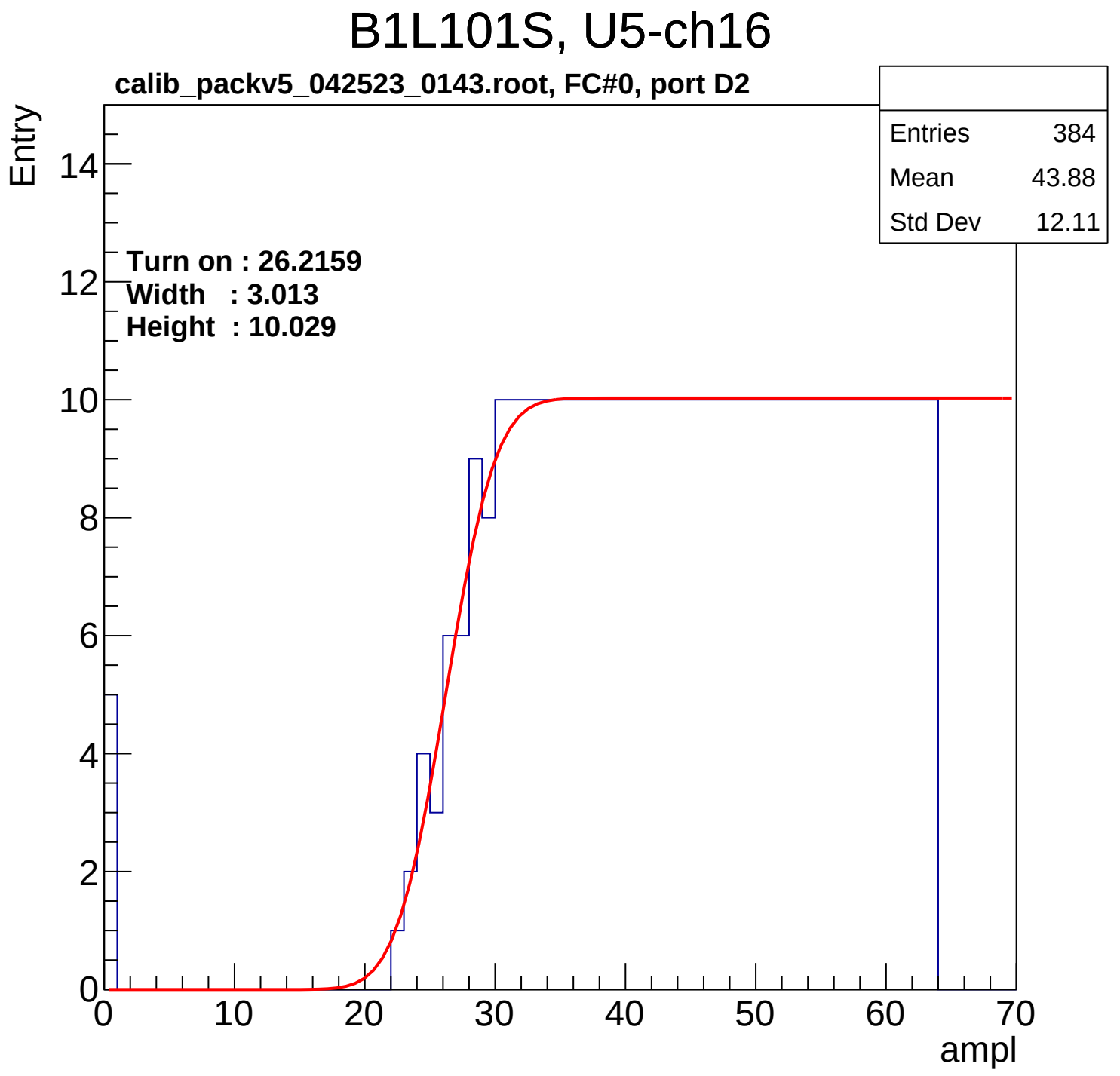

B1L101S, U5-ch11
calib_packv5_042523_0143.root, FC#0, port D2
Entries 360
Mean 45.03
Std Dev 11.63
Turn on : 29.1103
Width : 2.996
Height : 10.081
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

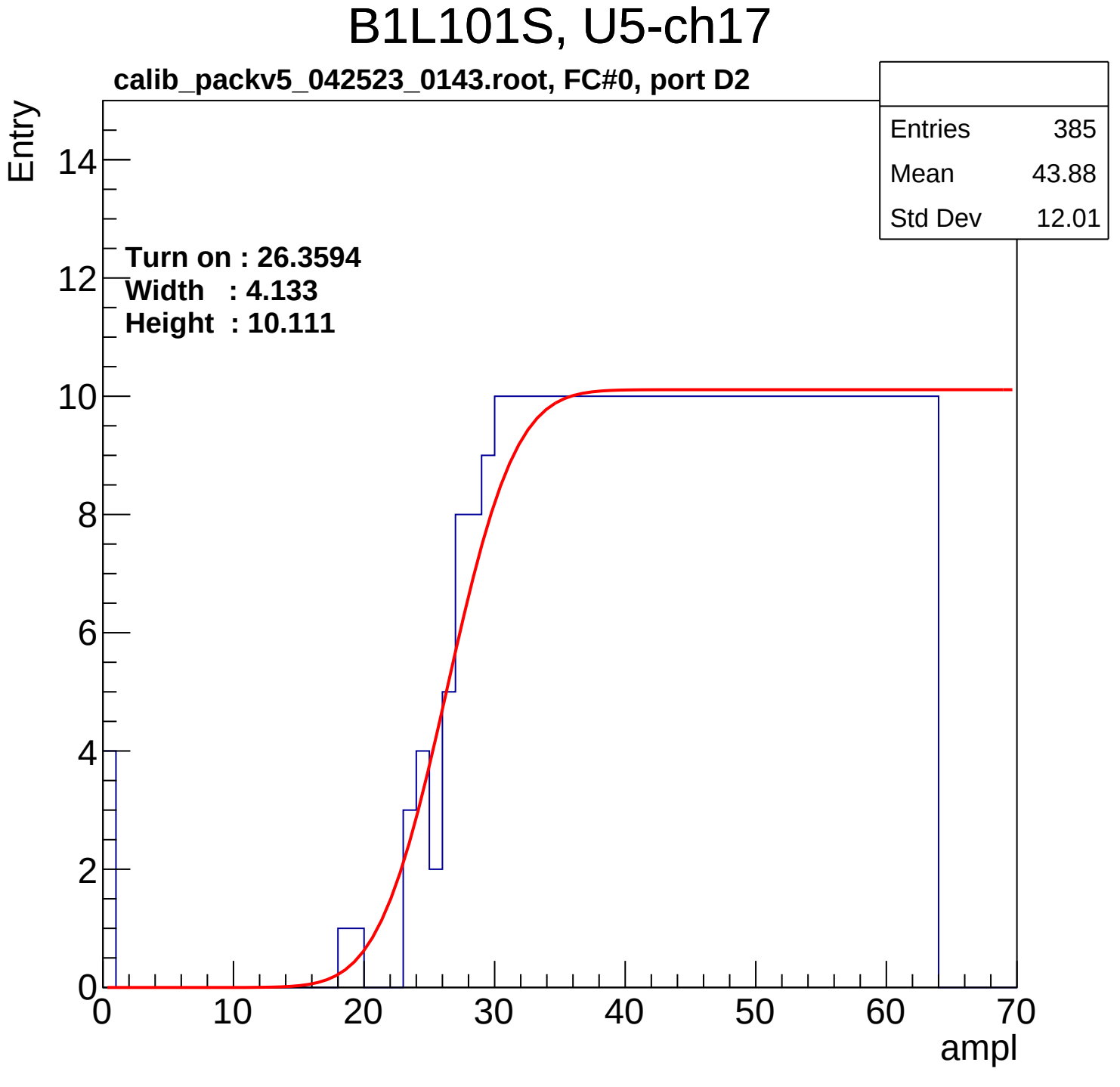

B1L101S, U5-ch12
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.37
Std Dev 11.45
Turn on : 27.0698
Width : 2.804
Height : 10.076
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

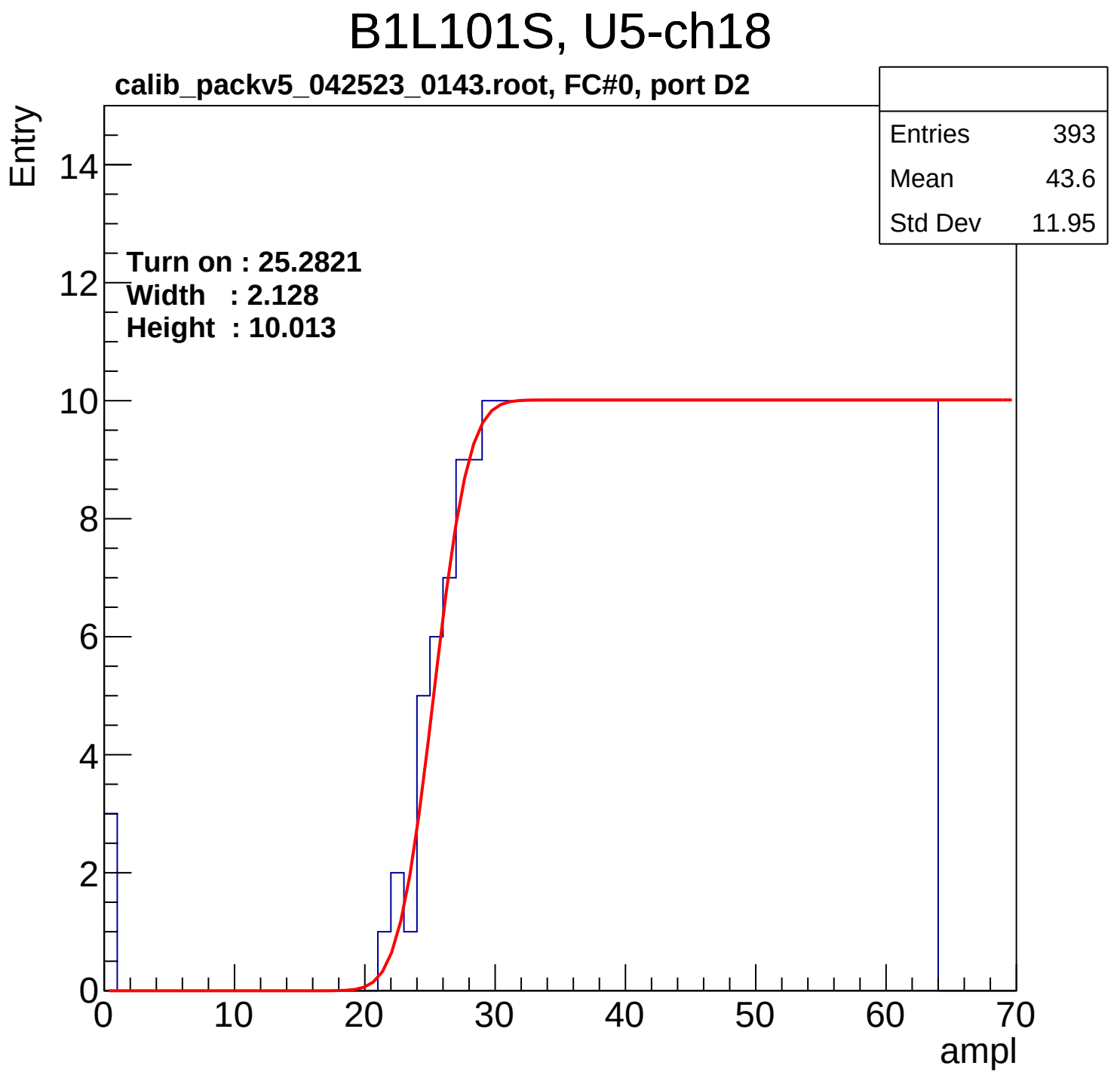

B1L101S, U5-ch13
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 43.95
Std Dev 11.99
Turn on : 25.4288
Width : 4.998
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

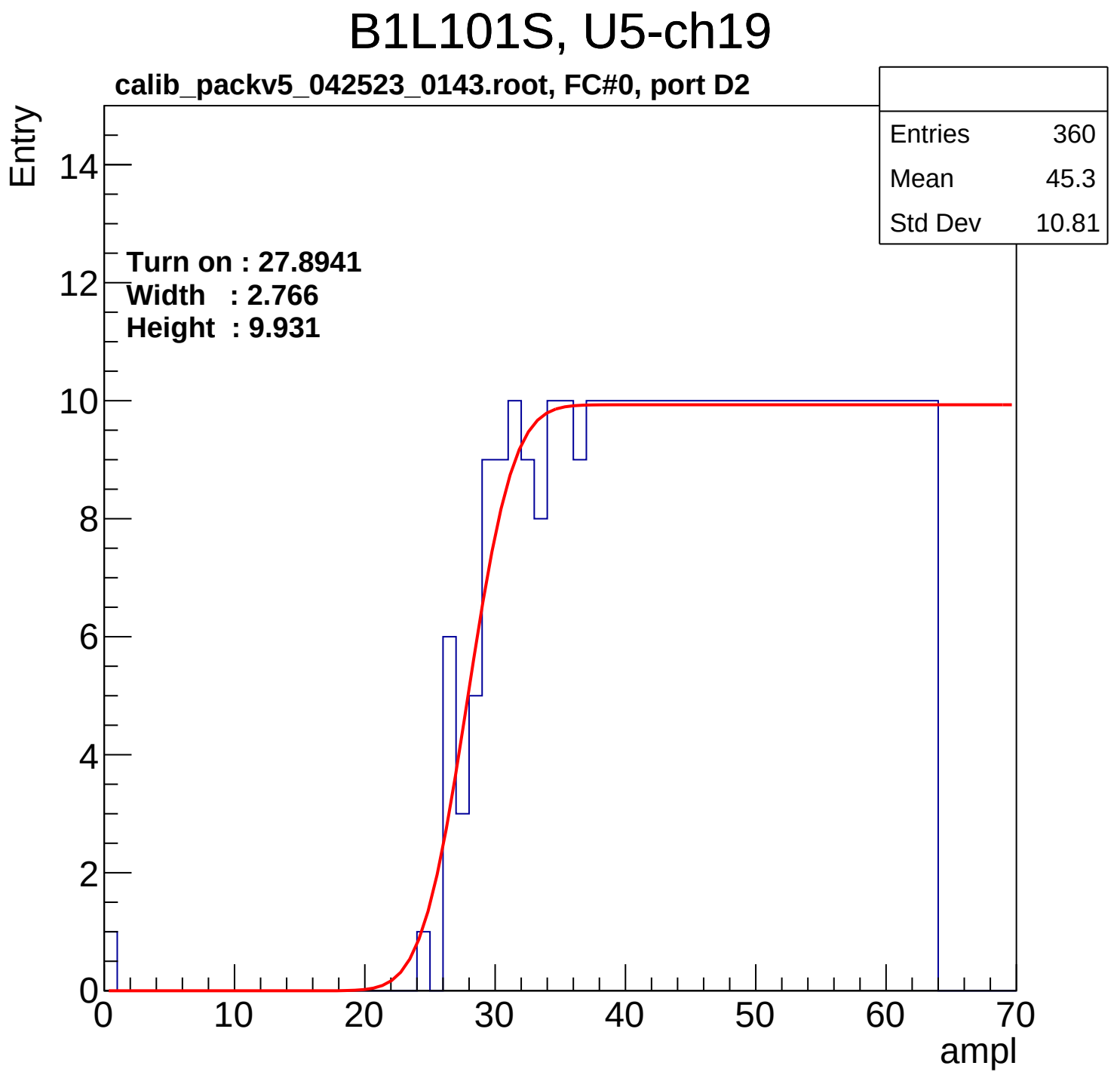

B1L101S, U5-ch14
calib_packv5_042523_0143.root, FC#0, port D2
Entries 380
Mean 44.02
Std Dev 12.19
Turn on : 26.8651
Width : 2.549
Height : 10.016
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

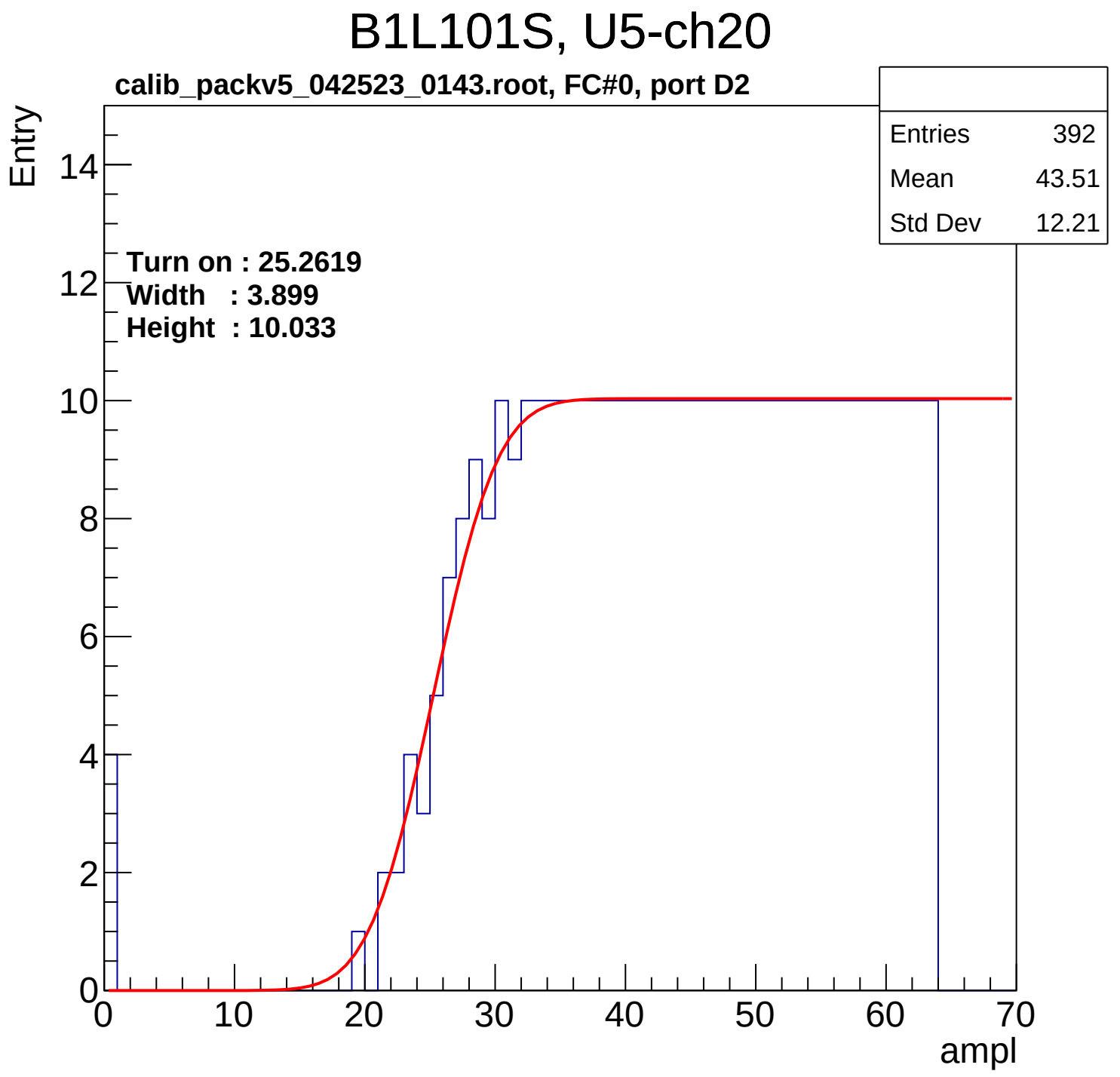

B1L101S, U5-ch15
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.39
Std Dev 11.78
Turn on : 26.9208
Width : 2.512
Height : 9.887
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

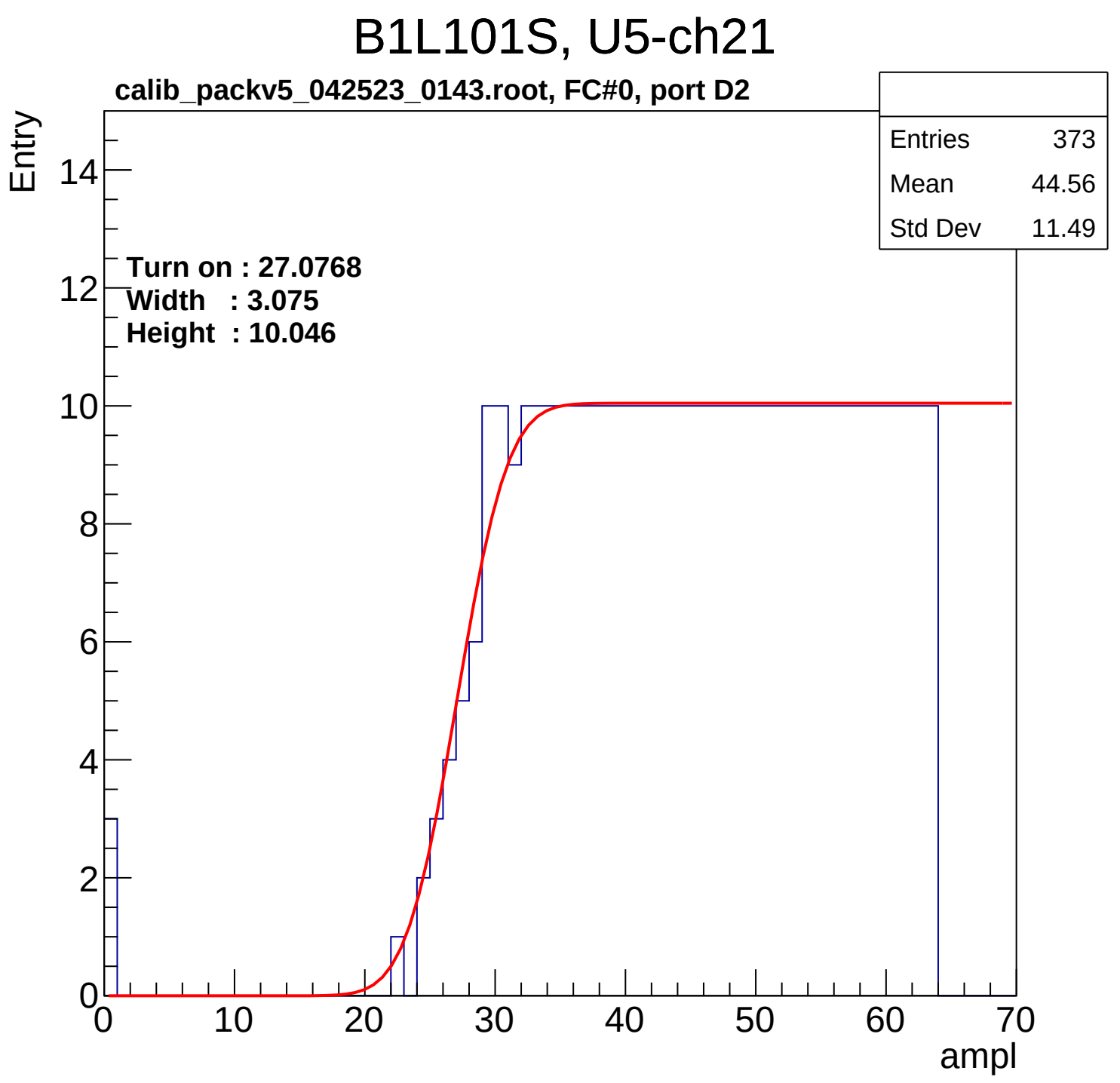

B1L101S, U5-ch16
calib_packv5_042523_0143.root, FC#0, port D2
Entries 384
Mean 43.88
Std Dev 12.11
Turn on : 26.2159
Width : 3.013
Height : 10.029
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

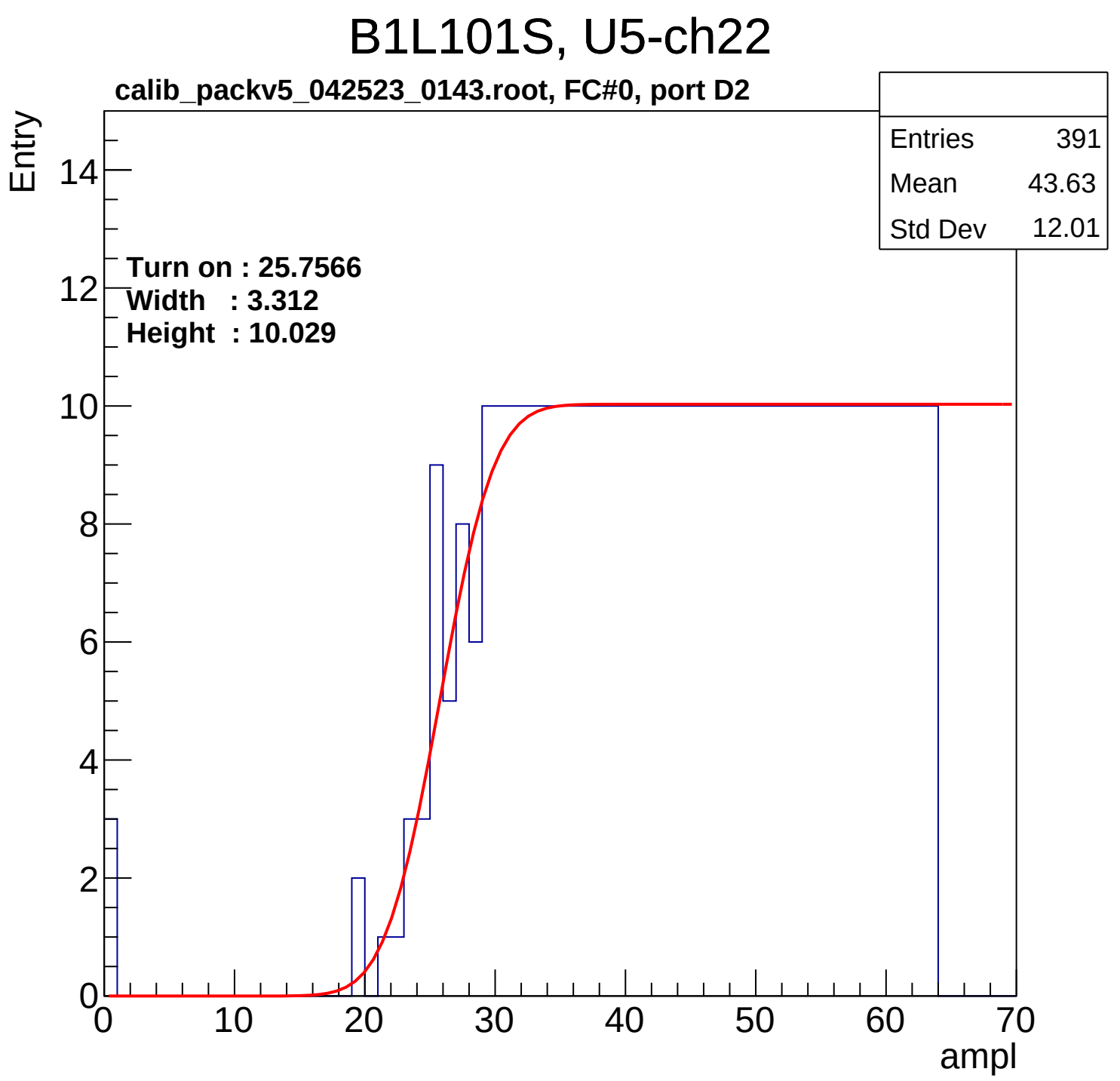

B1L101S, U5-ch17
calib_packv5_042523_0143.root, FC#0, port D2
Entries 385
Mean 43.88
Std Dev 12.01
Turn on : 26.3594
Width : 4.133
Height : 10.111
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

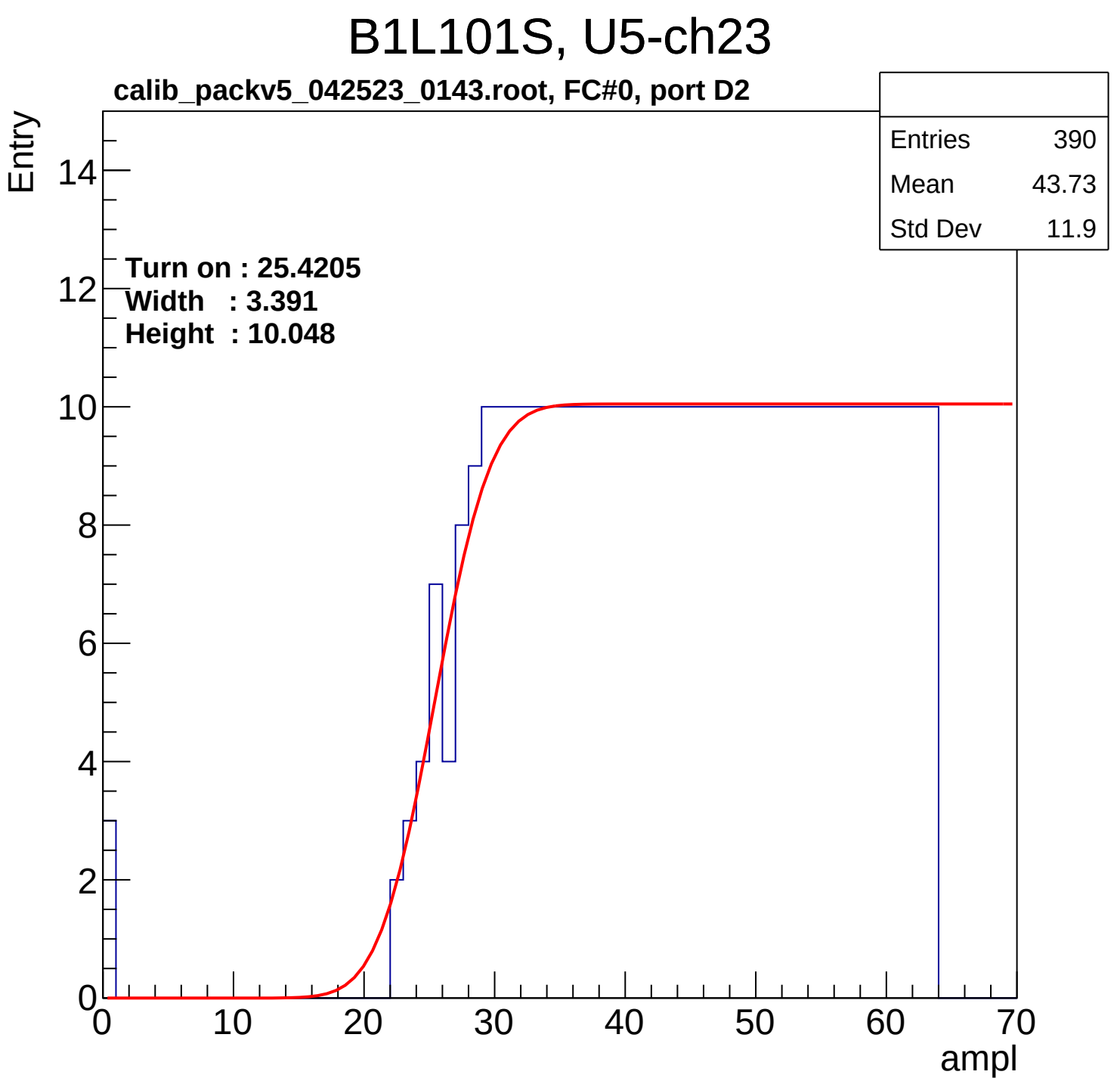

B1L101S, U5-ch18
calib_packv5_042523_0143.root, FC#0, port D2
Entries 393
Mean 43.6
Std Dev 11.95
Turn on : 25.2821
Width : 2.128
Height : 10.013
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

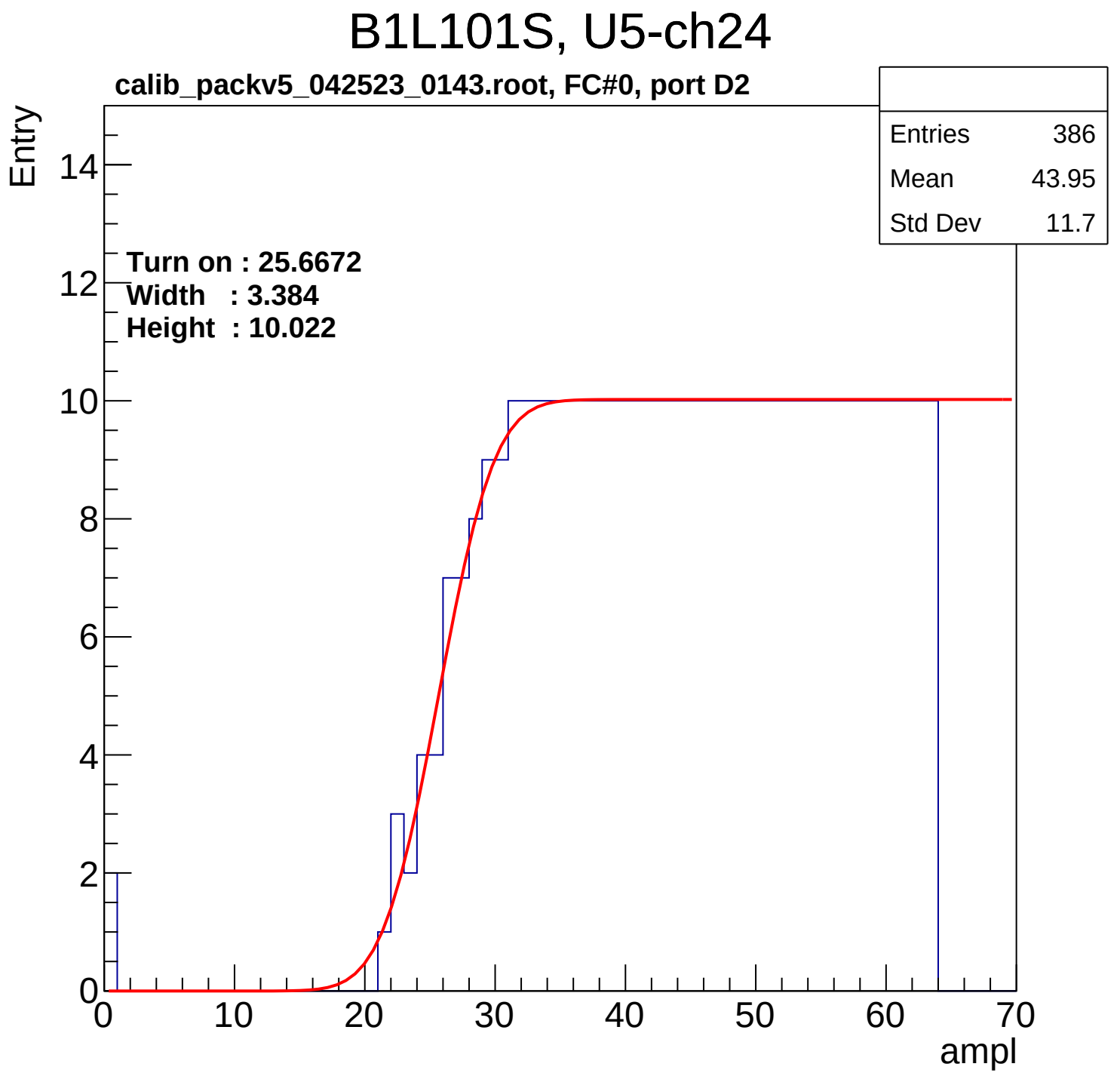

B1L101S, U5-ch19
calib_packv5_042523_0143.root, FC#0, port D2
Entries 360
Mean 45.3
Std Dev 10.81
Turn on : 27.8941
Width : 2.766
Height : 9.931
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

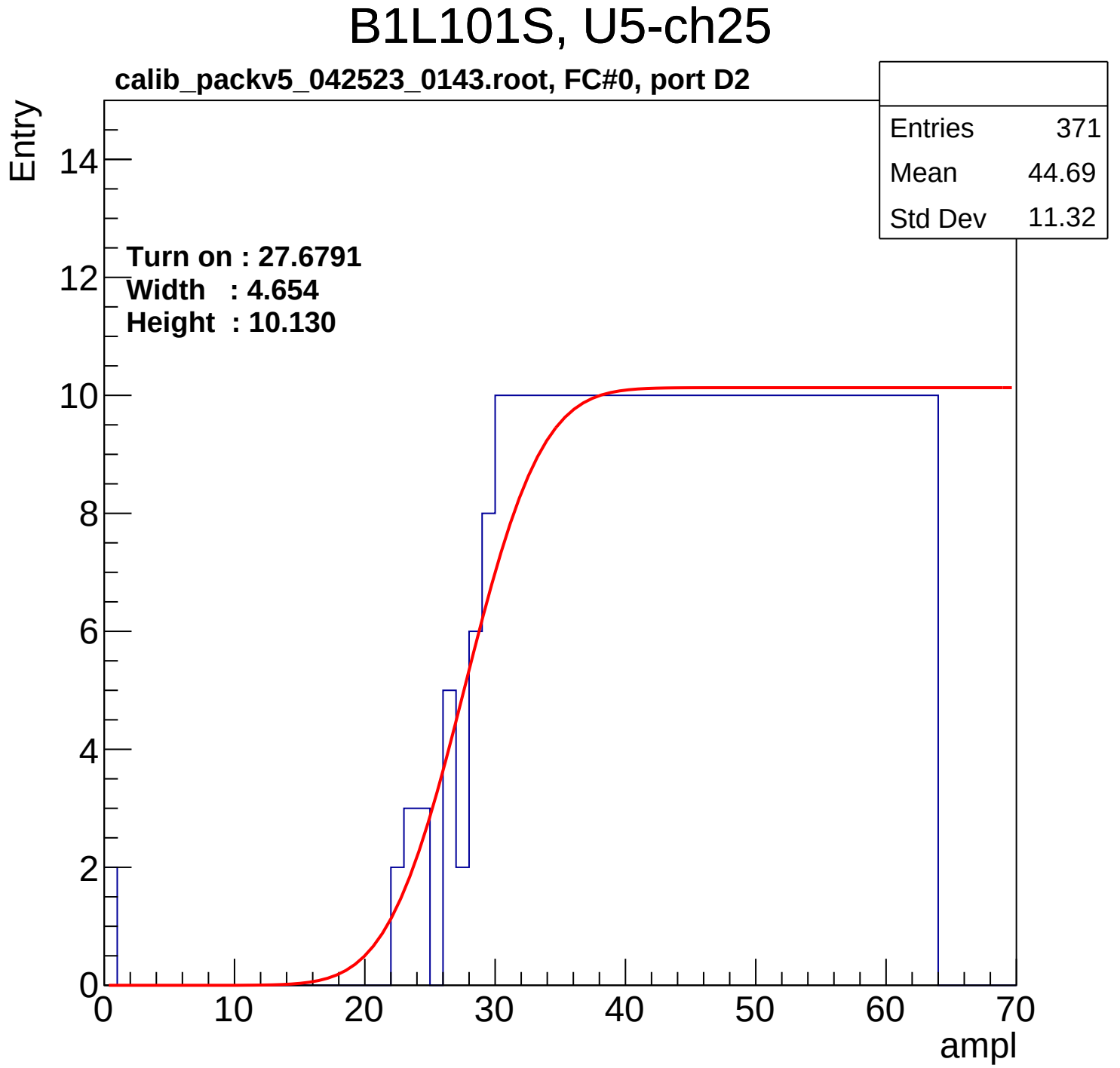

B1L101S, U5-ch20
calib_packv5_042523_0143.root, FC#0, port D2
Entries 392
Mean 43.51
Std Dev 12.21
Turn on : 25.2619
Width : 3.899
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

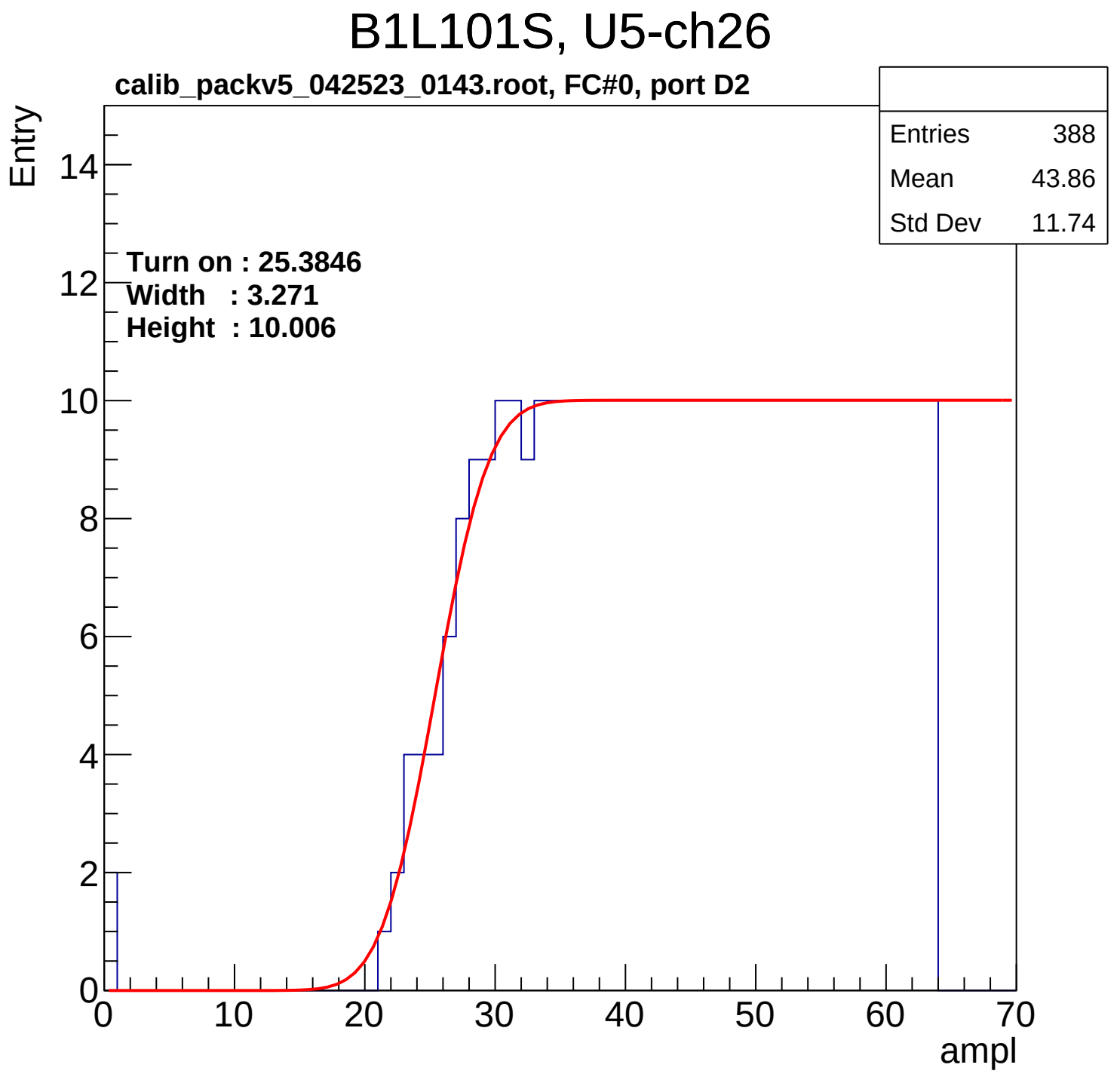

B1L101S, U5-ch21
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.56
Std Dev 11.49
Turn on : 27.0768
Width : 3.075
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

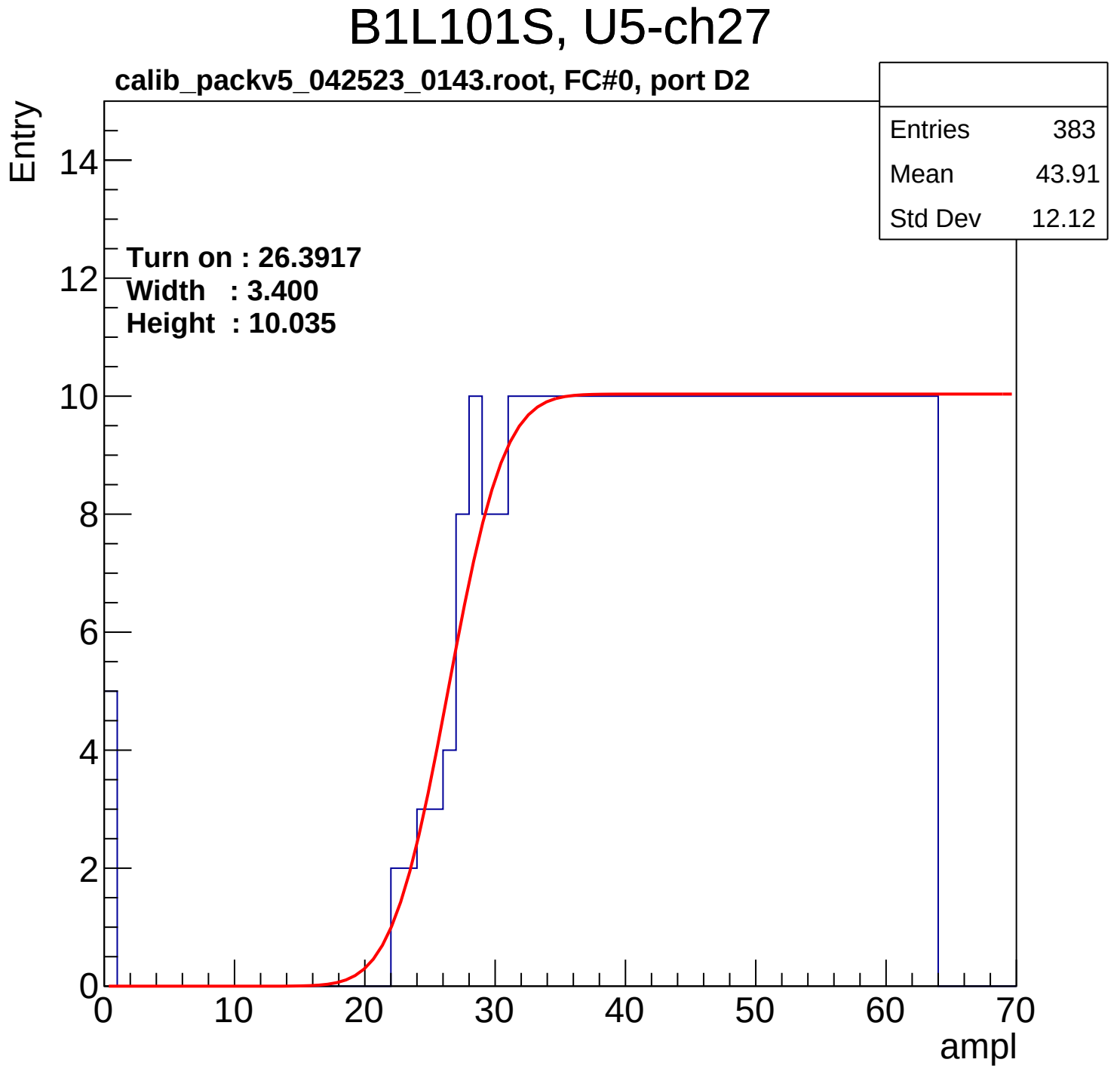

B1L101S, U5-ch22
calib_packv5_042523_0143.root, FC#0, port D2
Entries 391
Mean 43.63
Std Dev 12.01
Turn on : 25.7566
Width : 3.312
Height : 10.029
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

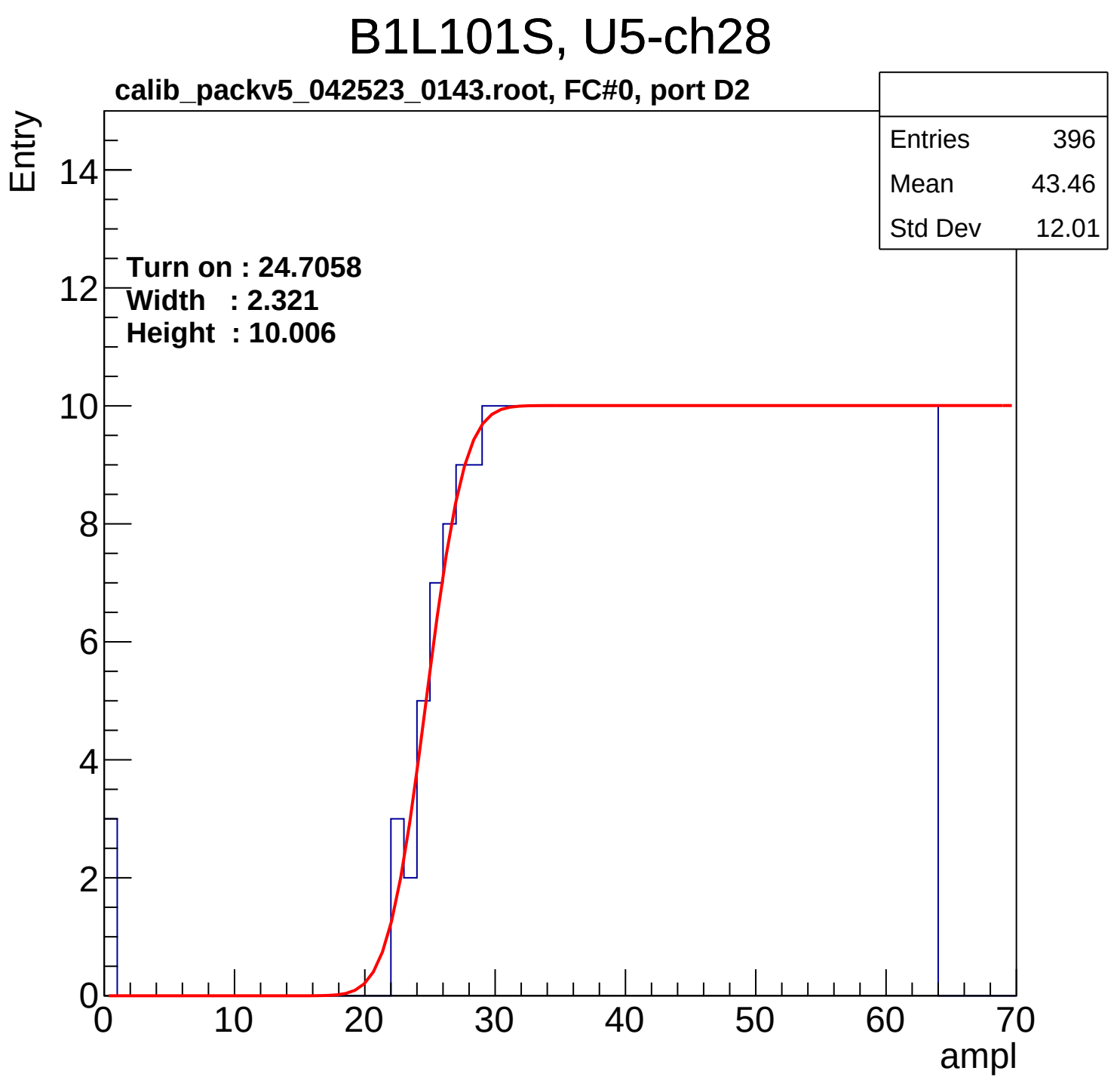

B1L101S, U5-ch23
calib_packv5_042523_0143.root, FC#0, port D2
Entries 390
Mean 43.73
Std Dev 11.9
Turn on : 25.4205
Width : 3.391
Height : 10.048
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

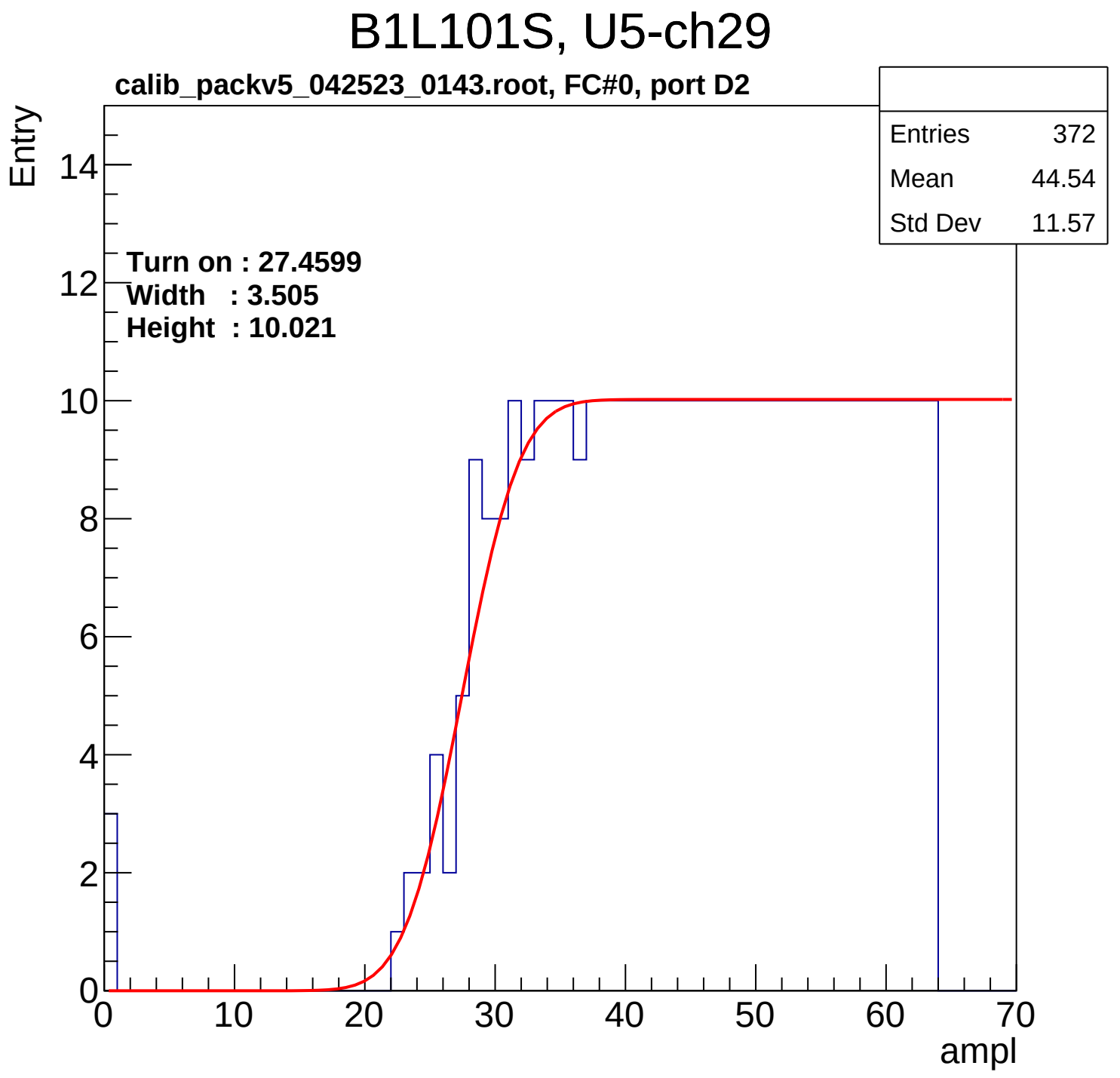

B1L101S, U5-ch24
calib_packv5_042523_0143.root, FC#0, port D2
Entries 386
Mean 43.95
Std Dev 11.7
Turn on : 25.6672
Width : 3.384
Height : 10.022
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

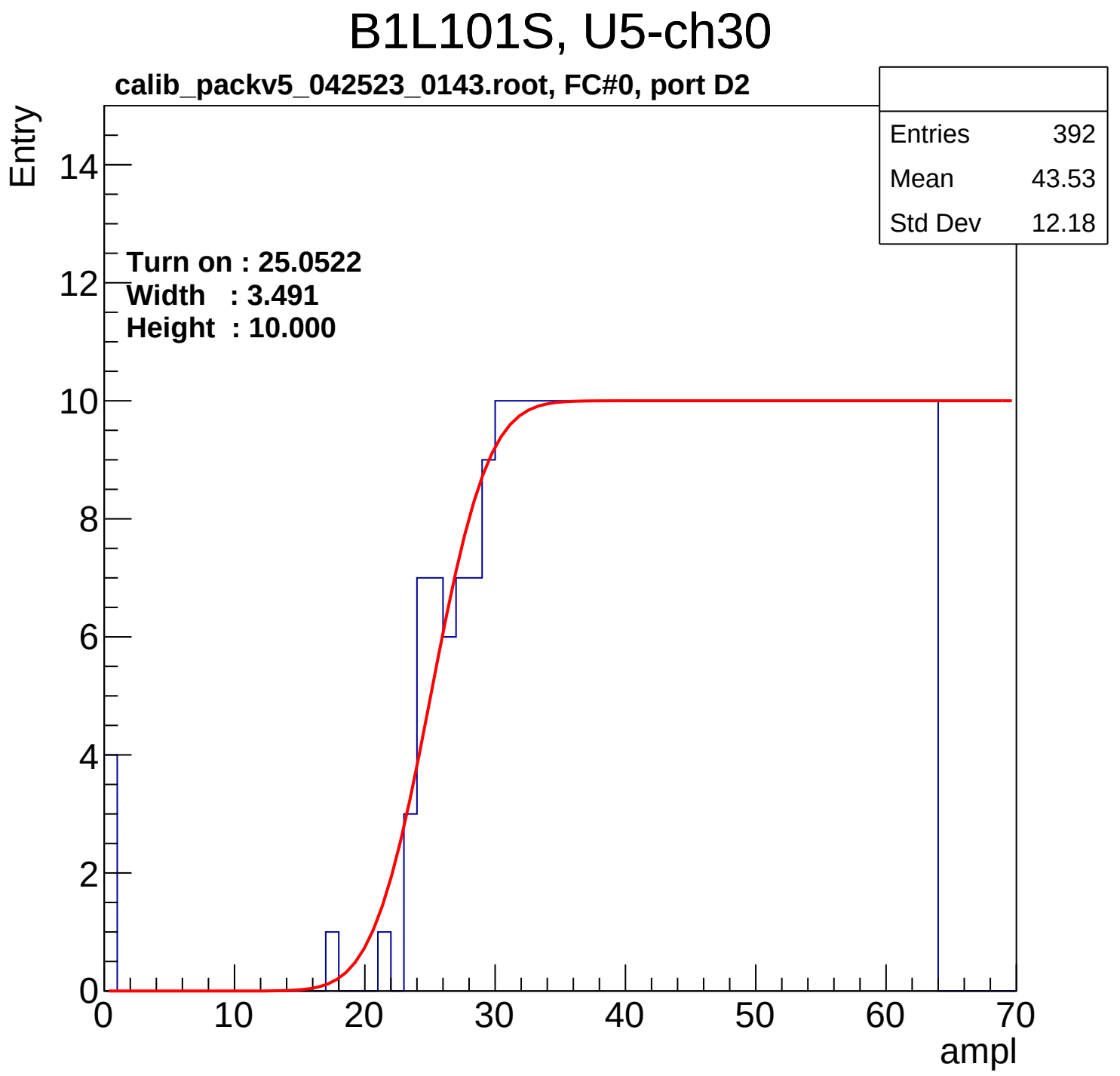

B1L101S, U5-ch25
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.69
Std Dev 11.32
Turn on : 27.6791
Width : 4.654
Height : 10.130
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

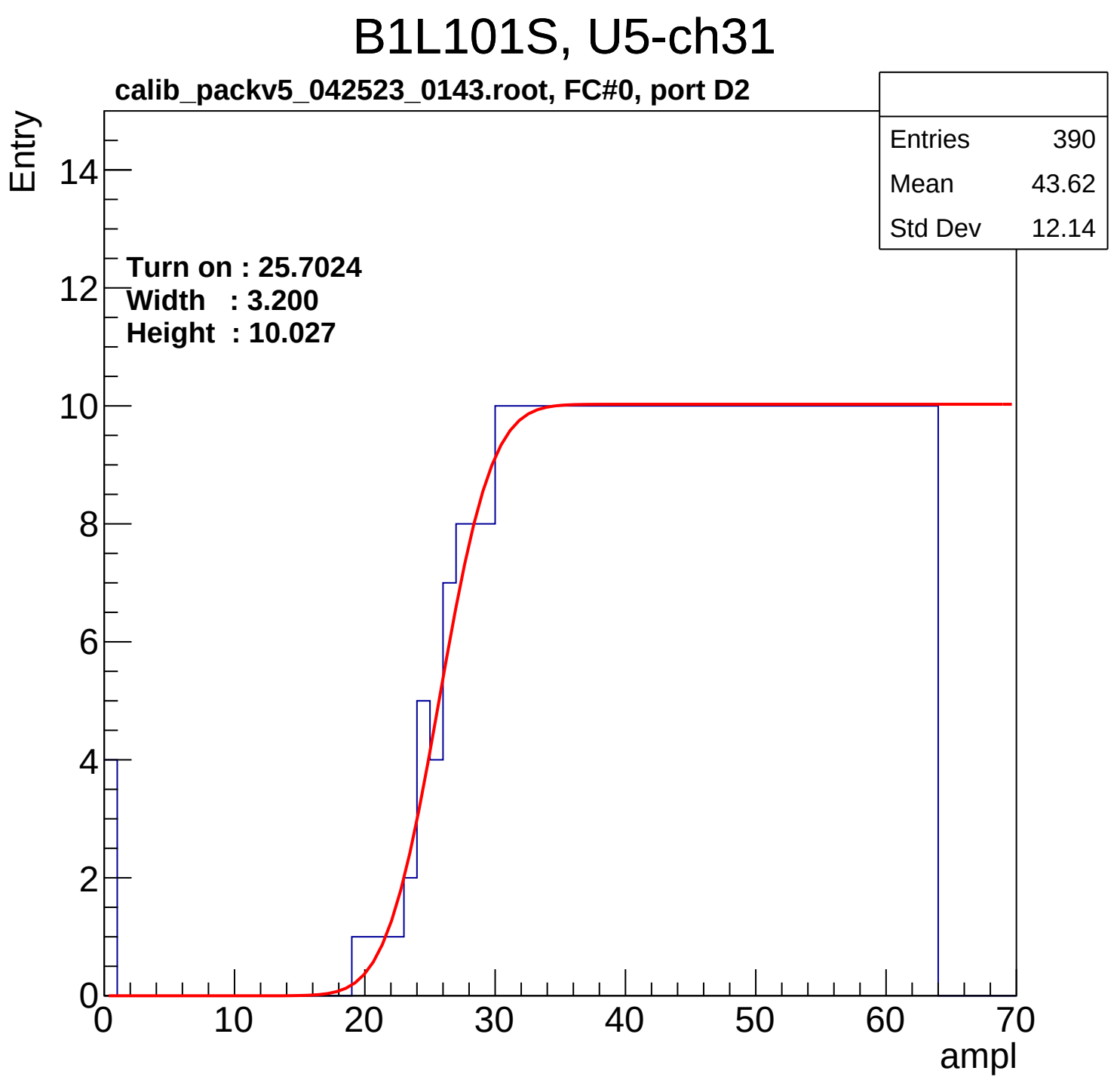

B1L101S, U5-ch26
calib_packv5_042523_0143.root, FC#0, port D2
Entries 388
Mean 43.86
Std Dev 11.74
Turn on : 25.3846
Width : 3.271
Height : 10.006
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

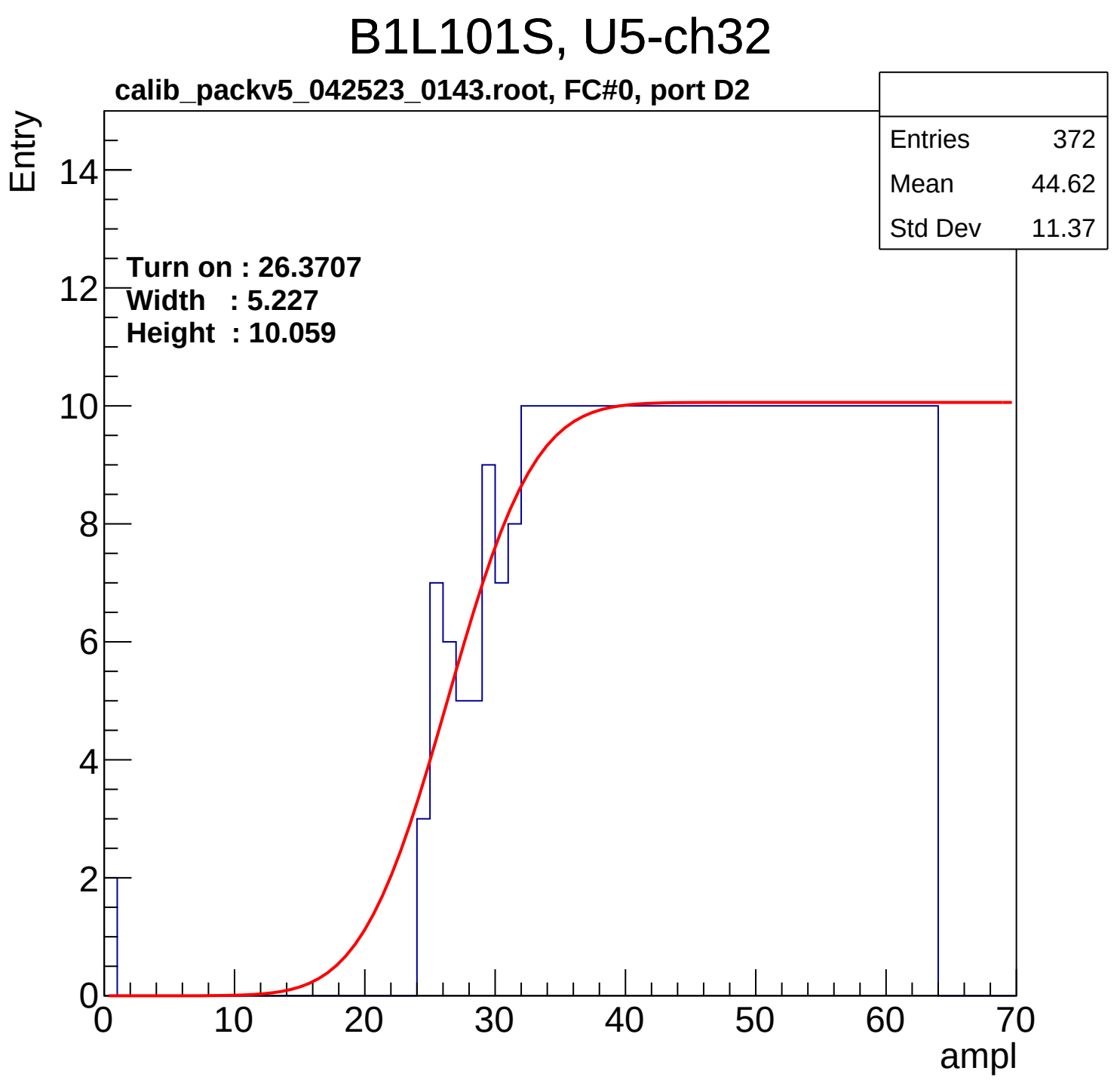

B1L101S, U5-ch27
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 43.91
Std Dev 12.12
Turn on : 26.3917
Width : 3.400
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

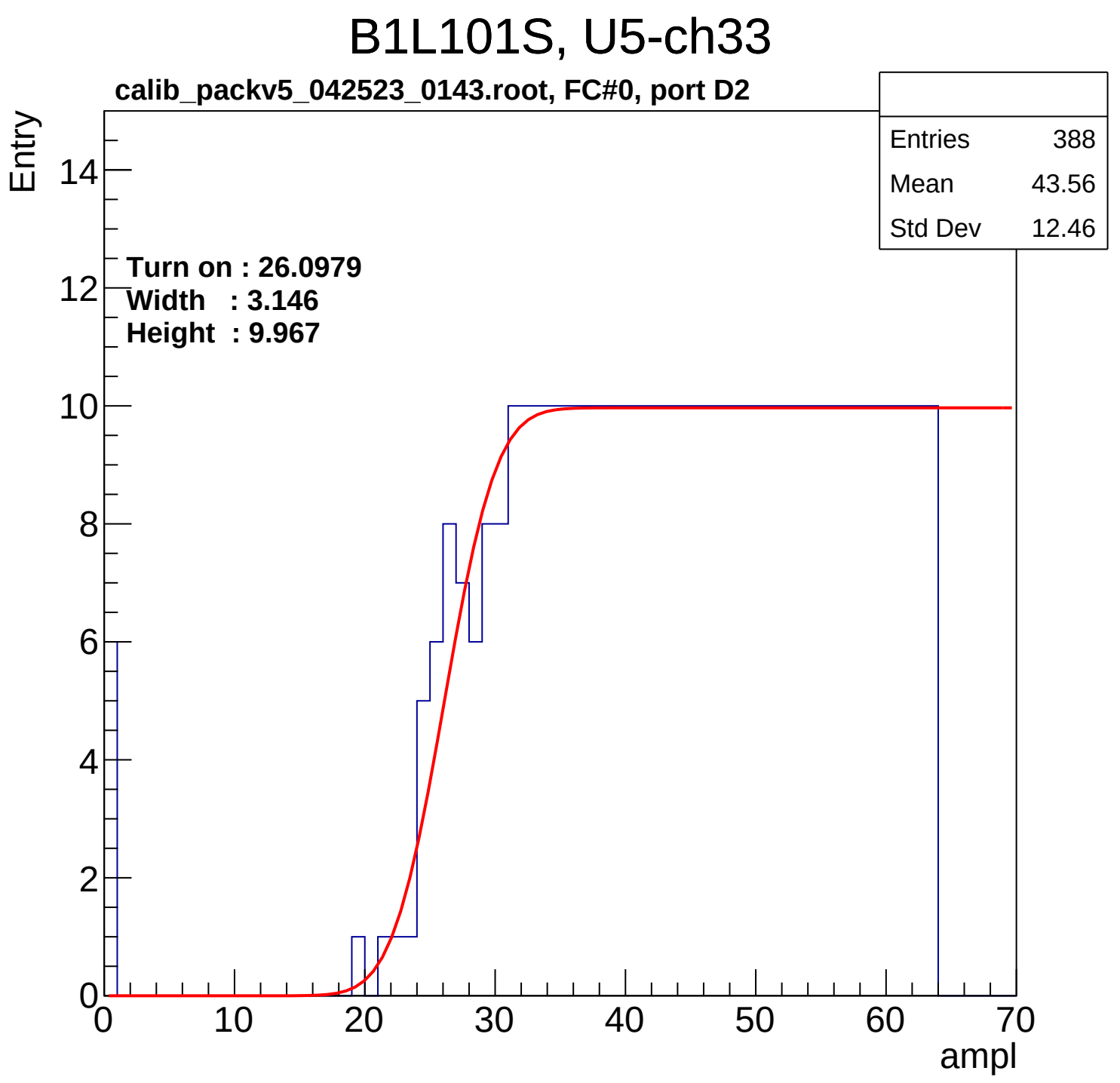

B1L101S, U5-ch28
calib_packv5_042523_0143.root, FC#0, port D2
Entries 396
Mean 43.46
Std Dev 12.01
Turn on : 24.7058
Width : 2.321
Height : 10.006
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

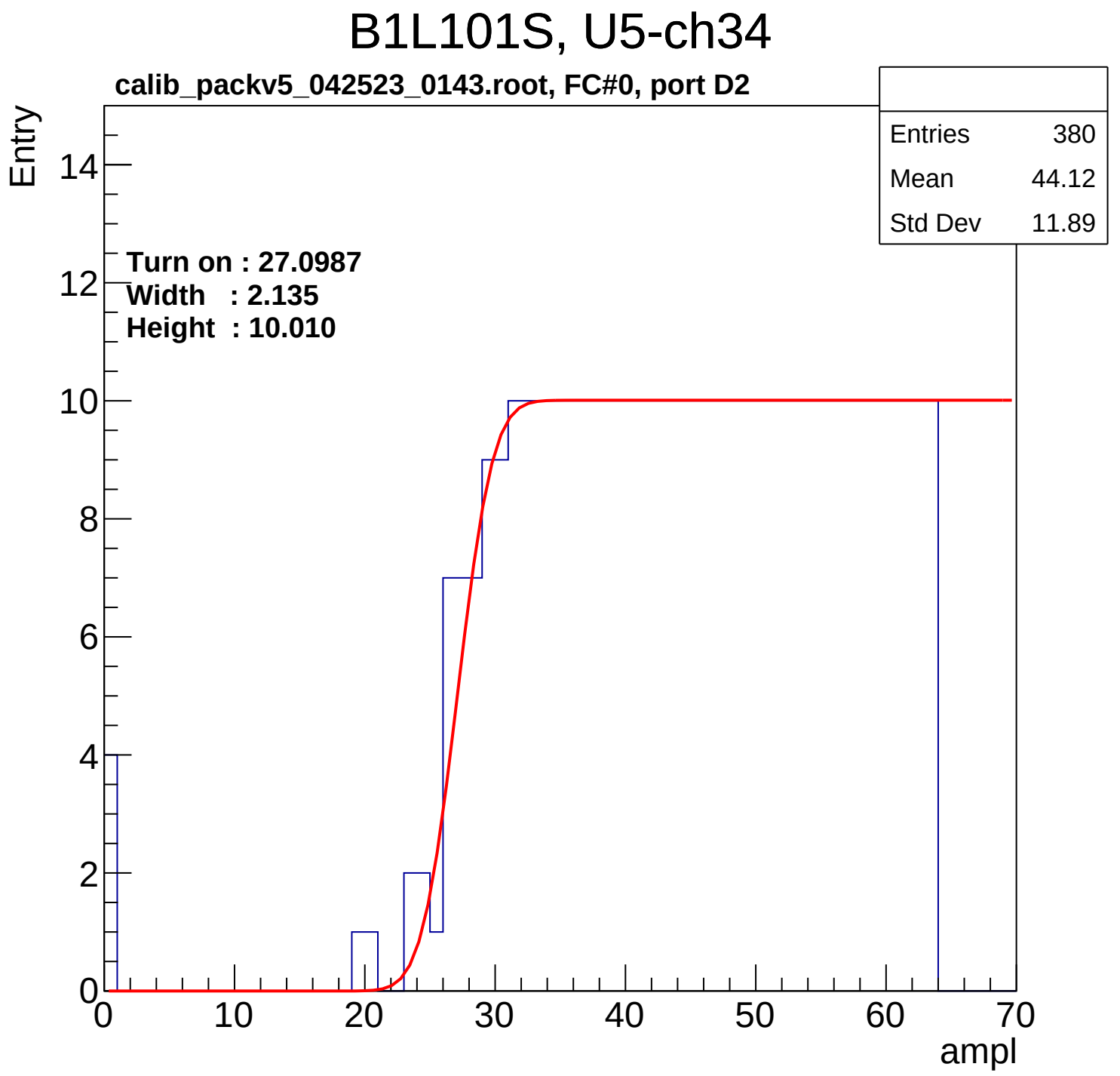

B1L101S, U5-ch29
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.54
Std Dev 11.57
Turn on : 27.4599
Width : 3.505
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

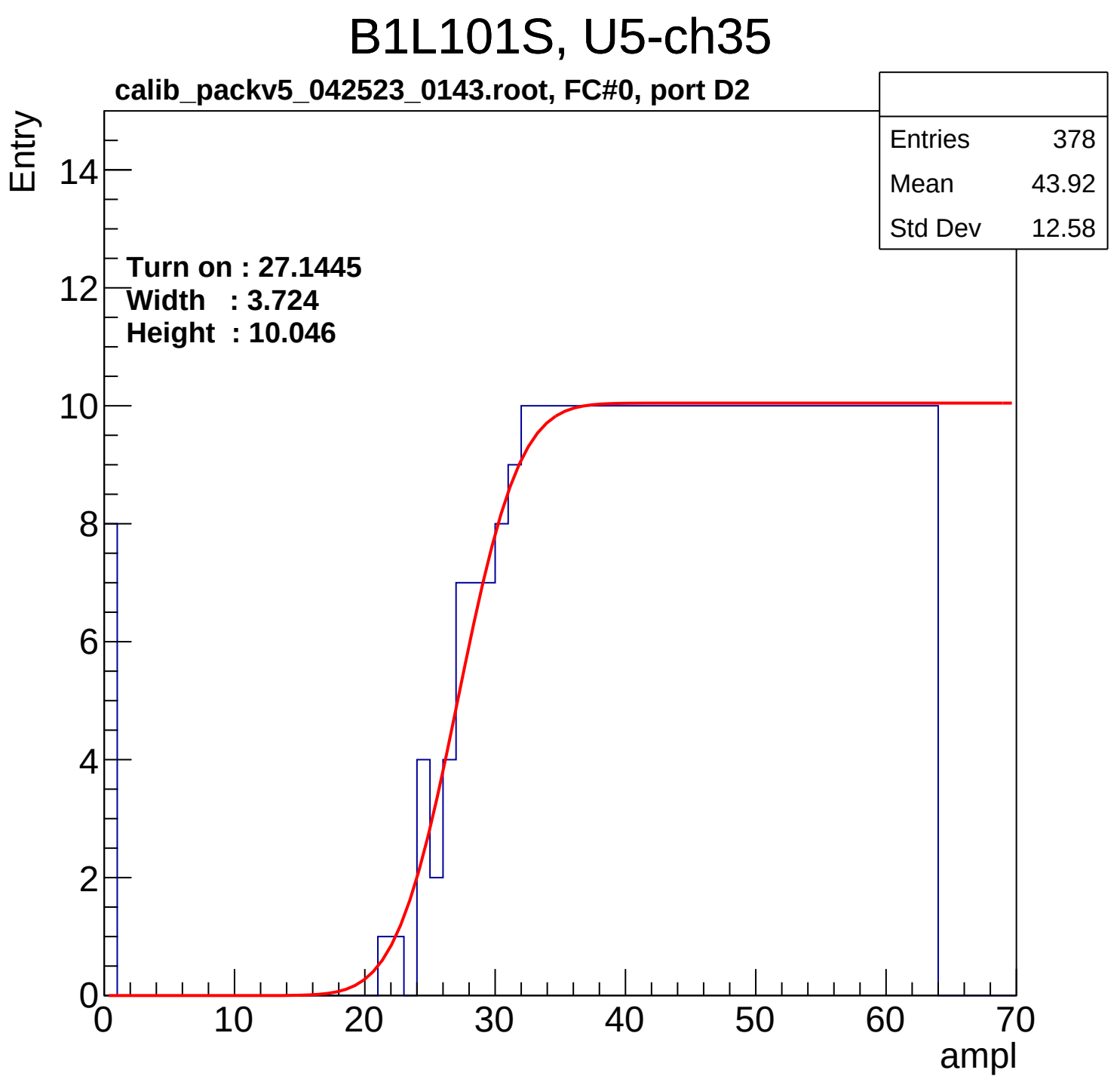

B1L101S, U5-ch30
calib_packv5_042523_0143.root, FC#0, port D2
Entries 392
Mean 43.53
Std Dev 12.18
Turn on : 25.0522
Width : 3.491
Height : 10.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

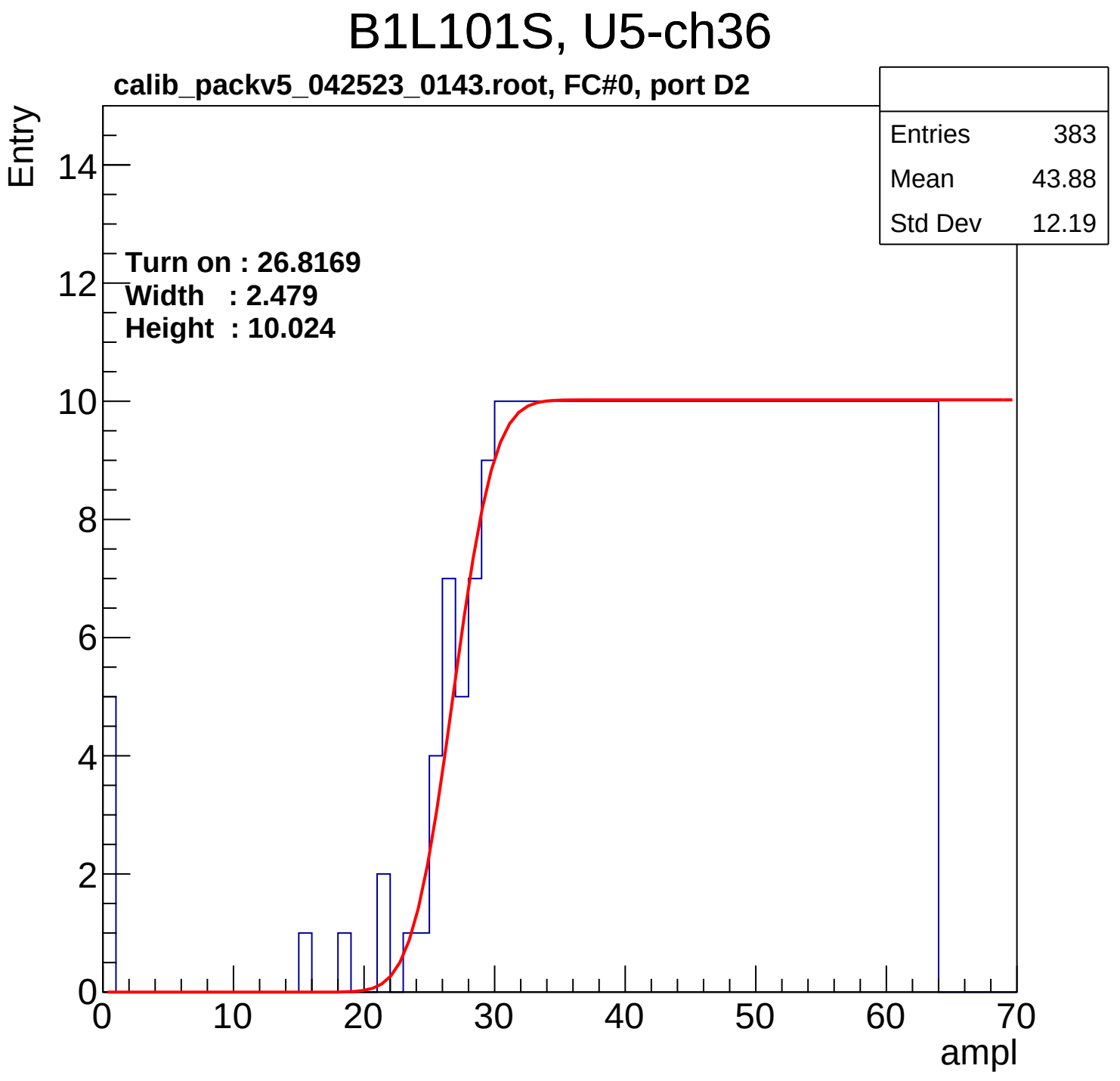

B1L101S, U5-ch31
calib_packv5_042523_0143.root, FC#0, port D2
Entries 390
Mean 43.62
Std Dev 12.14
Turn on : 25.7024
Width : 3.200
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

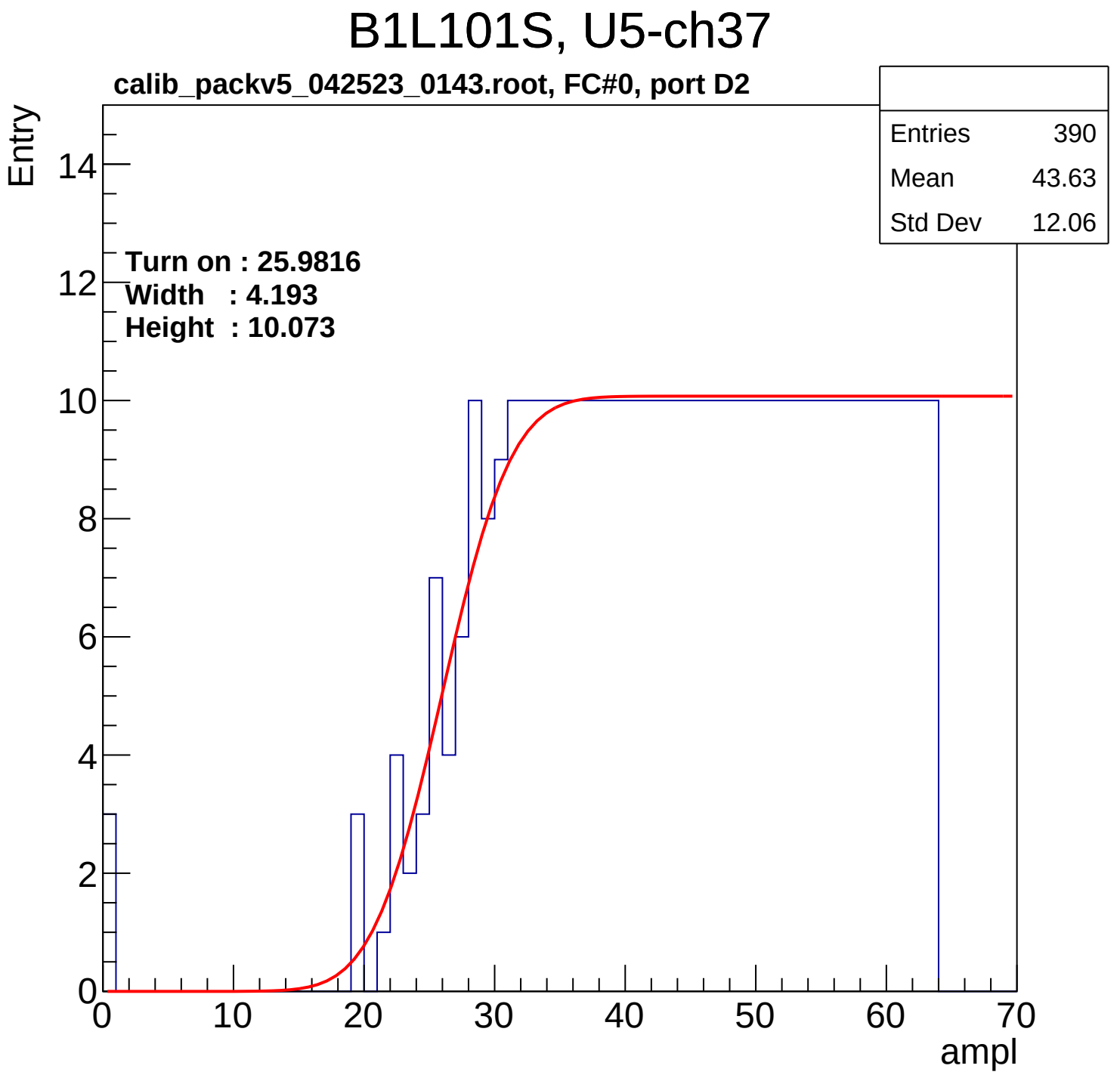

B1L101S, U5-ch32
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.62
Std Dev 11.37
Turn on : 26.3707
Width : 5.227
Height : 10.059
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

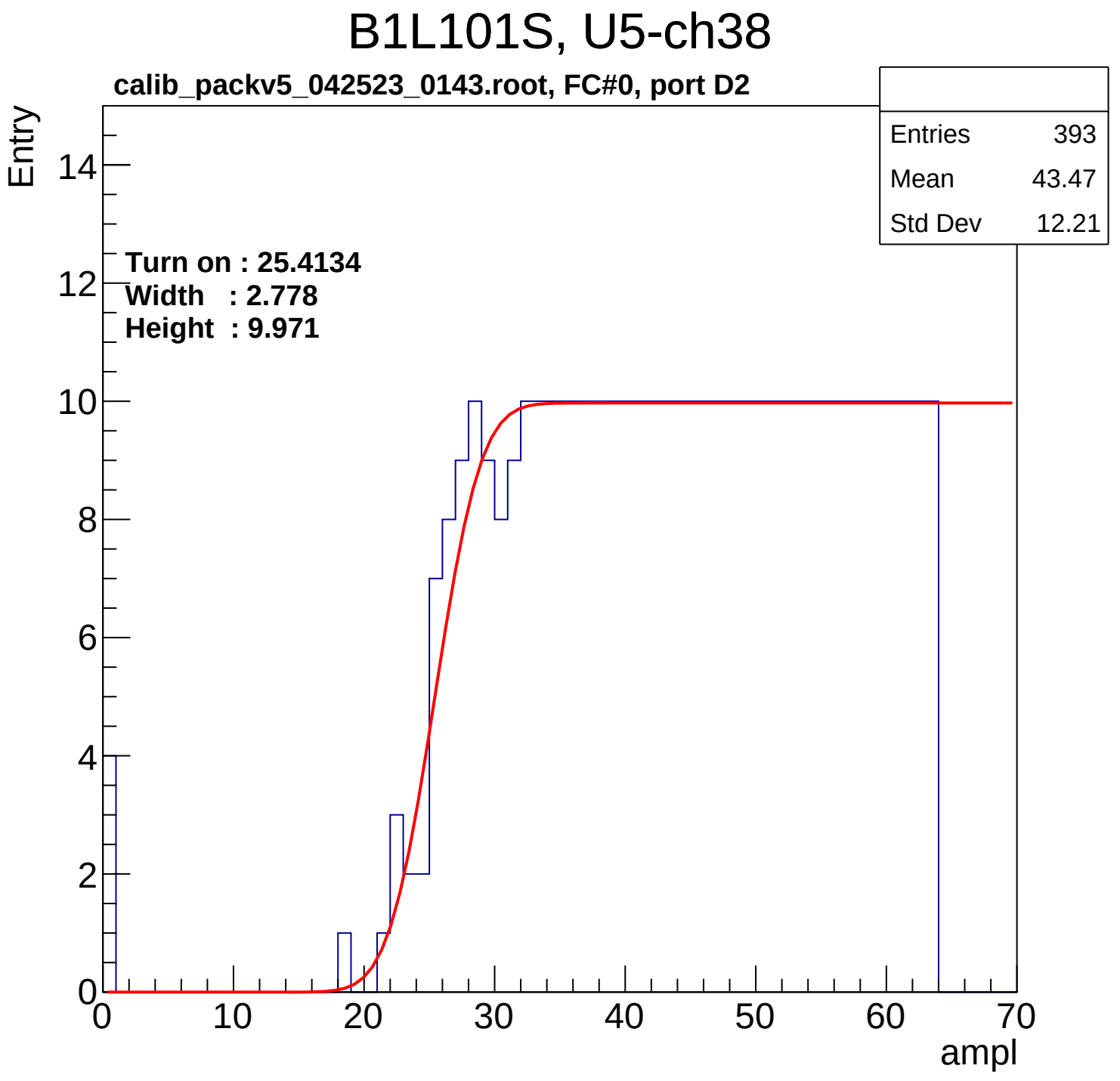

B1L101S, U5-ch33
calib_packv5_042523_0143.root, FC#0, port D2
Entries 388
Mean 43.56
Std Dev 12.46
Turn on : 26.0979
Width : 3.146
Height : 9.967
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

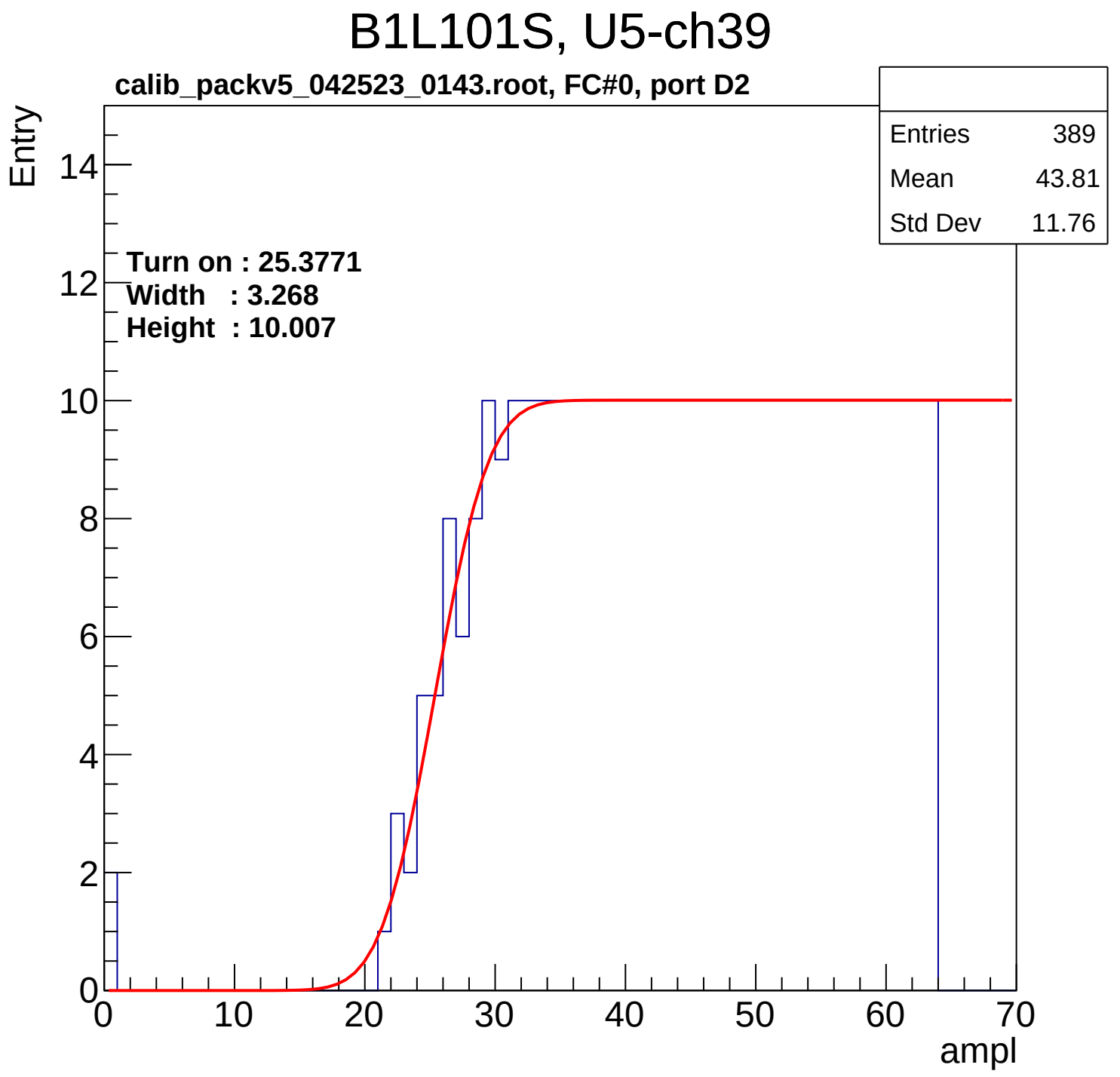

B1L101S, U5-ch34
calib_packv5_042523_0143.root, FC#0, port D2
Entries 380
Mean 44.12
Std Dev 11.89
Turn on : 27.0987
Width : 2.135
Height : 10.010
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

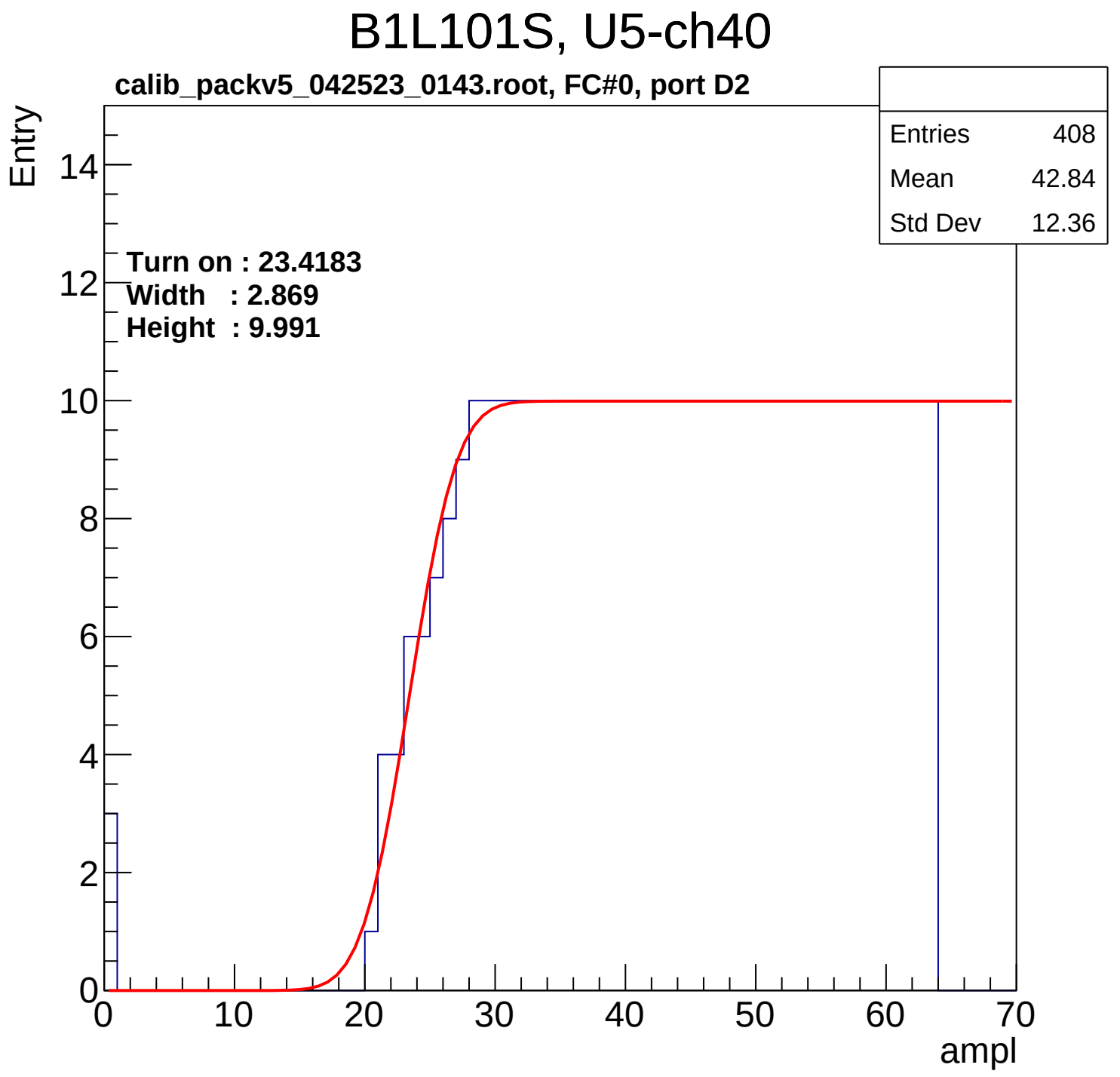

B1L101S, U5-ch35
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 43.92
Std Dev 12.58
Turn on : 27.1445
Width : 3.724
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

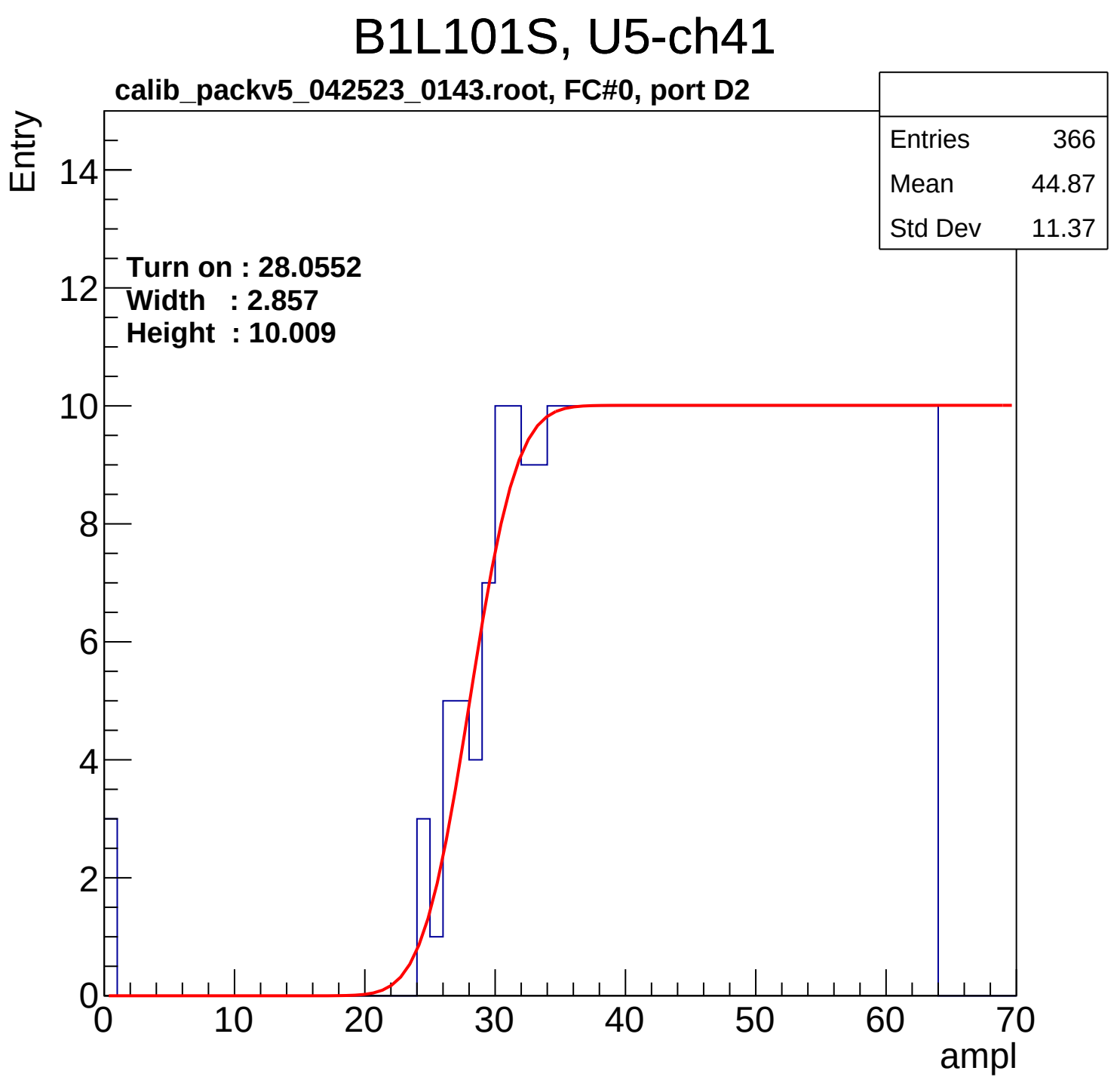

B1L101S, U5-ch36
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 43.88
Std Dev 12.19
Turn on : 26.8169
Width : 2.479
Height : 10.024
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

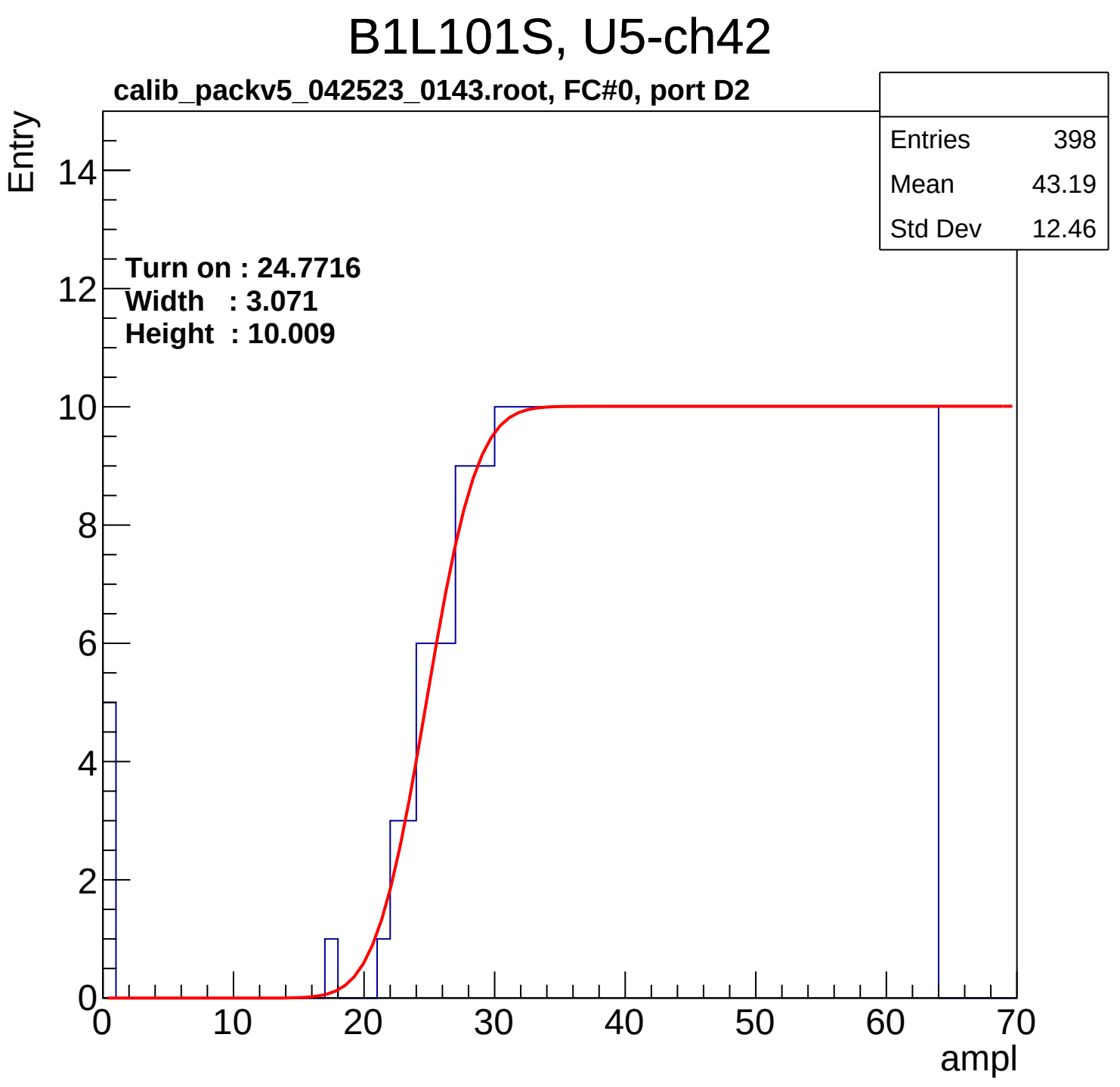

B1L101S, U5-ch37
calib_packv5_042523_0143.root, FC#0, port D2
Entries 390
Mean 43.63
Std Dev 12.06
Turn on : 25.9816
Width : 4.193
Height : 10.073
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

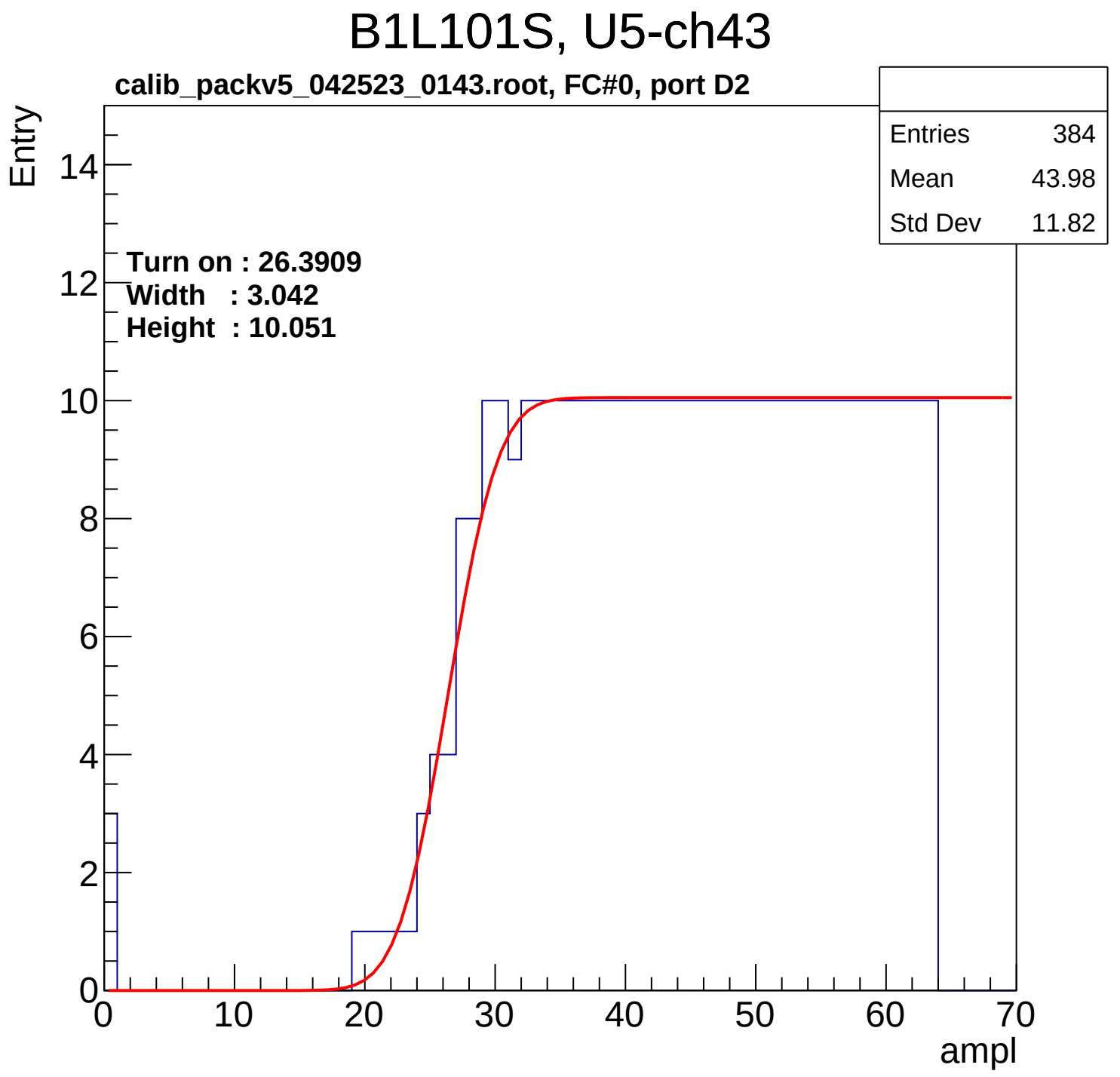

B1L101S, U5-ch38
calib_packv5_042523_0143.root, FC#0, port D2
Entries 393
Mean 43.47
Std Dev 12.21
Turn on : 25.4134
Width : 2.778
Height : 9.971
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

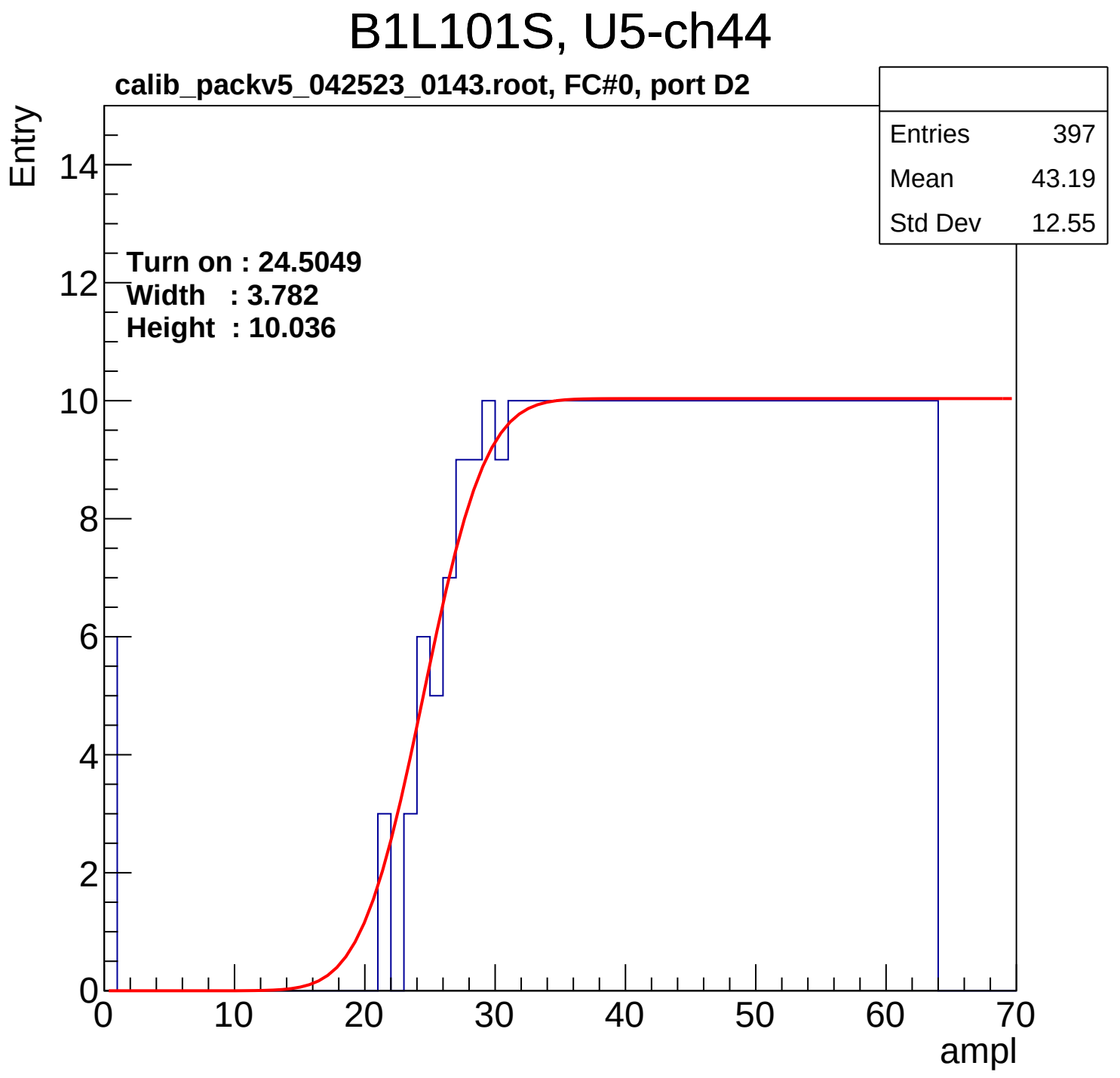

B1L101S, U5-ch39
calib_packv5_042523_0143.root, FC#0, port D2
Entries 389
Mean 43.81
Std Dev 11.76
Turn on : 25.3771
Width : 3.268
Height : 10.007
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

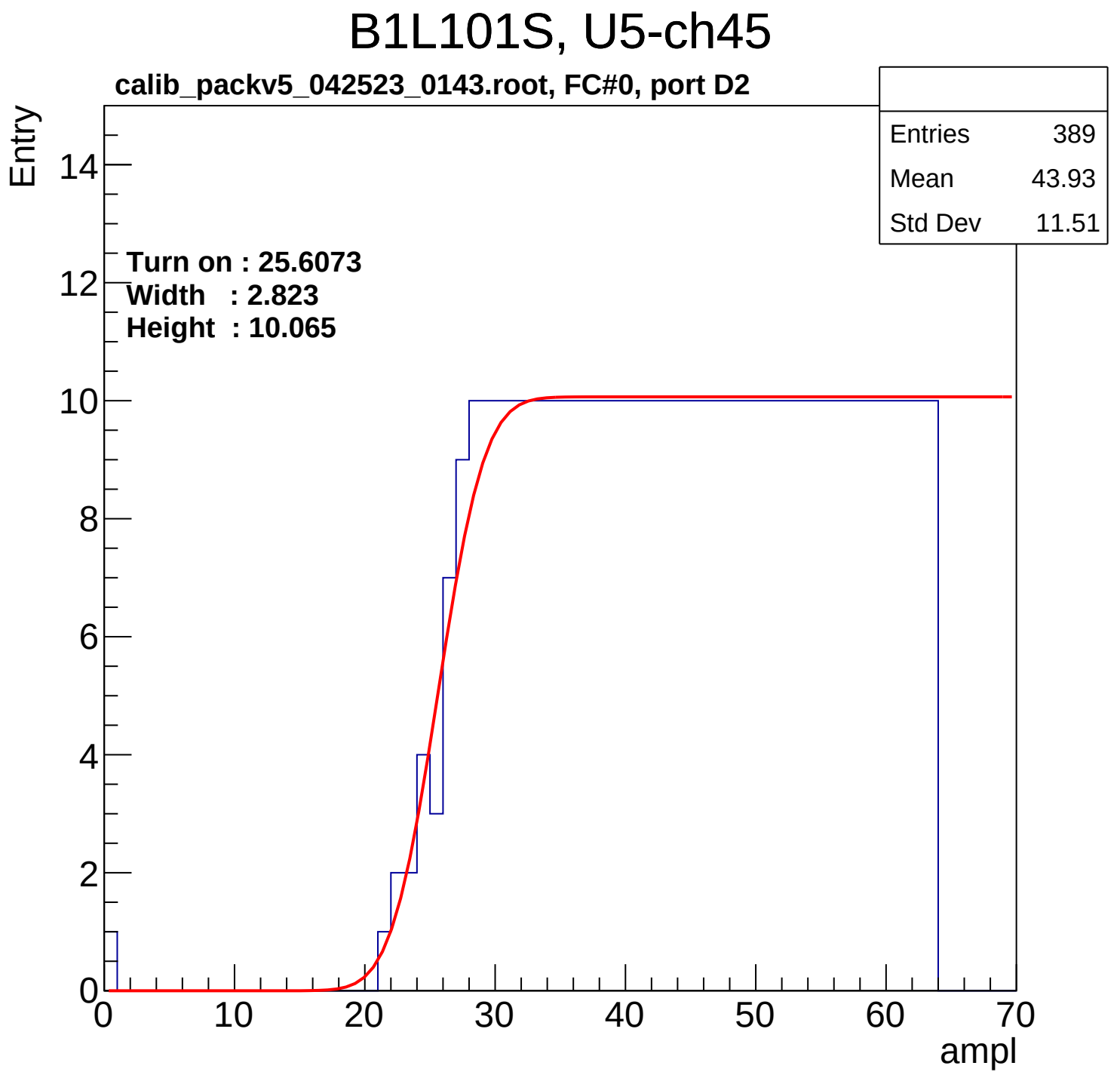

B1L101S, U5-ch40
calib_packv5_042523_0143.root, FC#0, port D2
Entries 408
Mean 42.84
Std Dev 12.36
Turn on : 23.4183
Width : 2.869
Height : 9.991
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

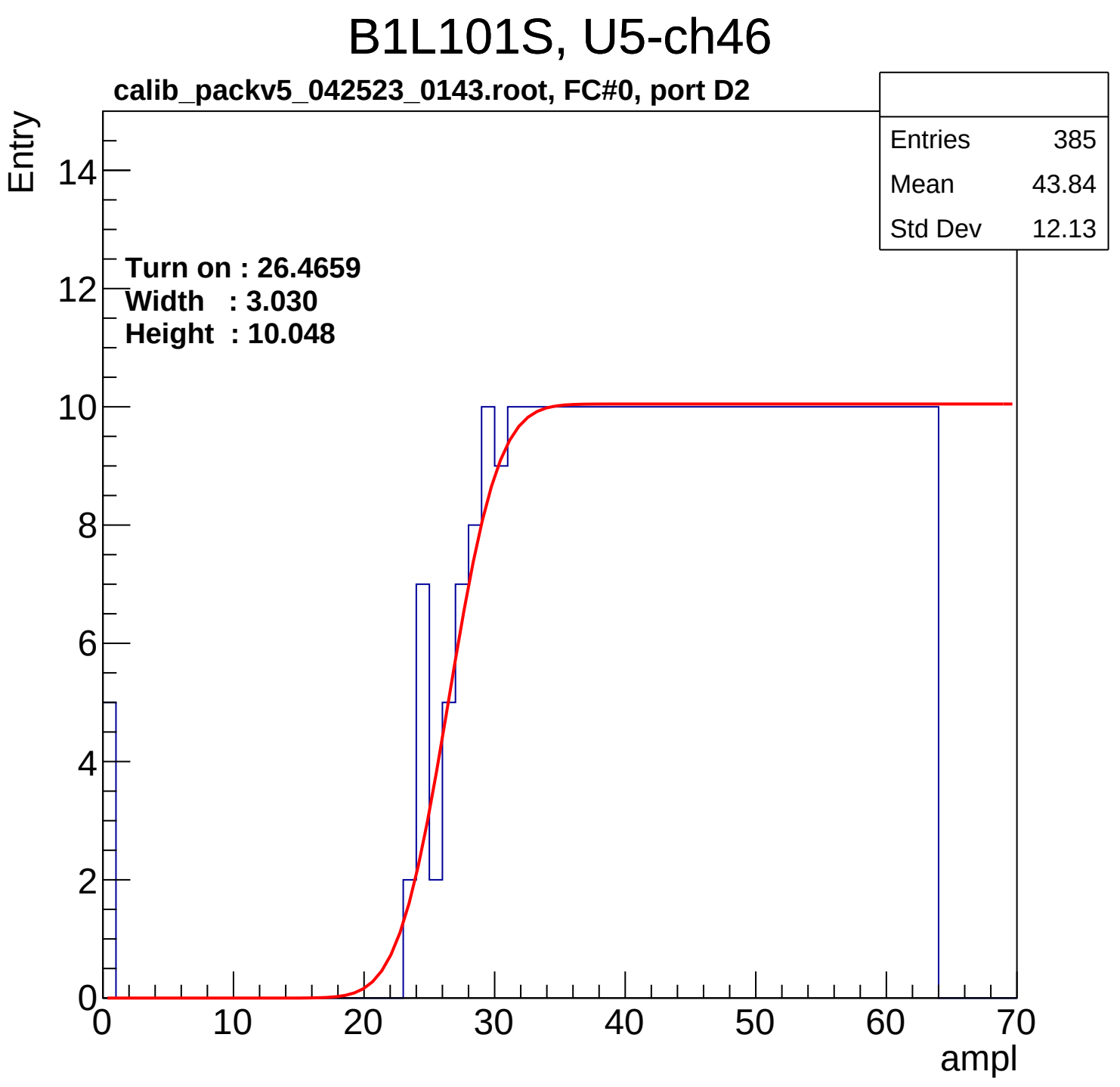

B1L101S, U5-ch41
calib_packv5_042523_0143.root, FC#0, port D2
Entries 366
Mean 44.87
Std Dev 11.37
Turn on : 28.0552
Width : 2.857
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

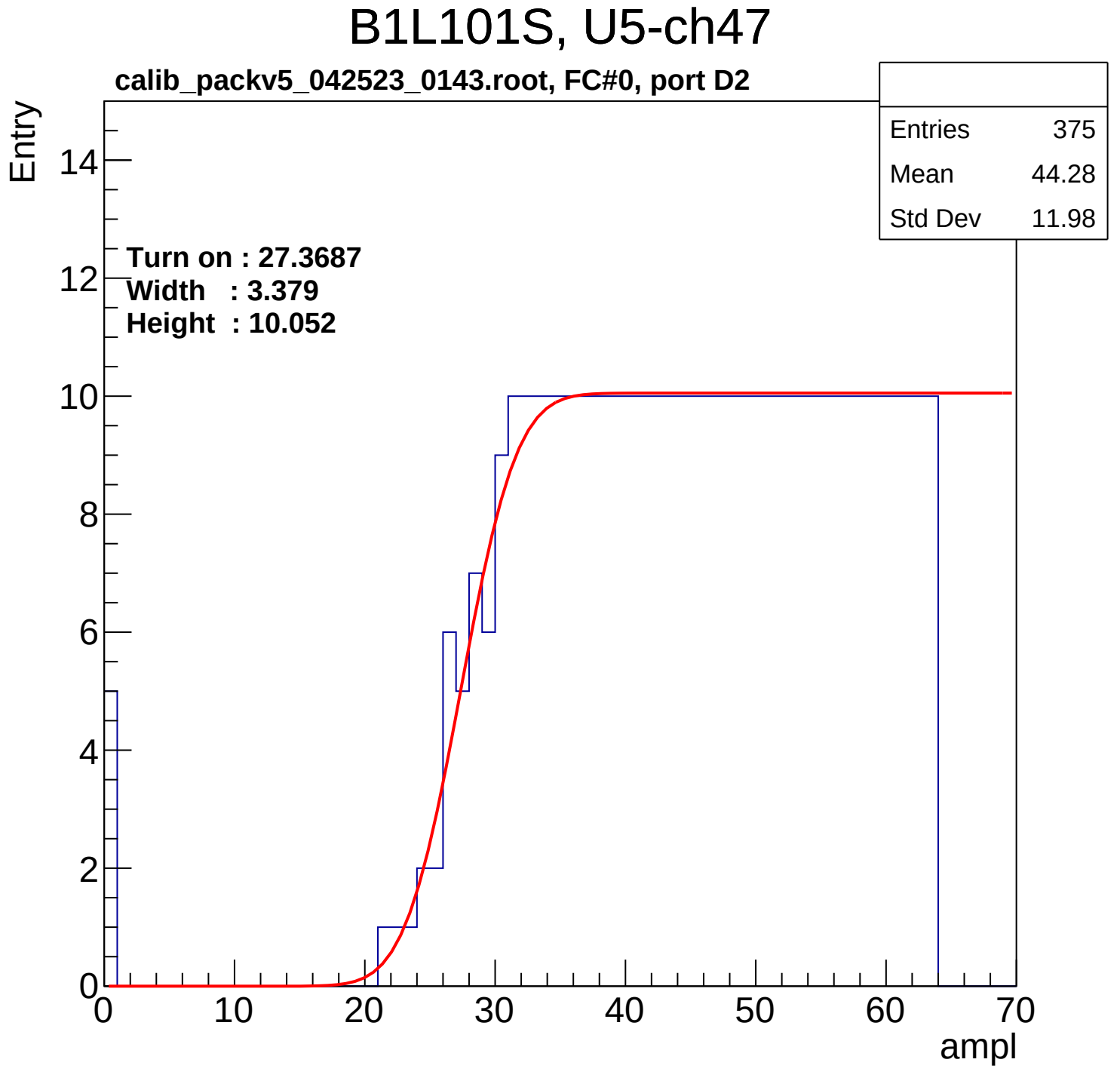

B1L101S, U5-ch42
calib_packv5_042523_0143.root, FC#0, port D2
Entries 398
Mean 43.19
Std Dev 12.46
Turn on : 24.7716
Width : 3.071
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

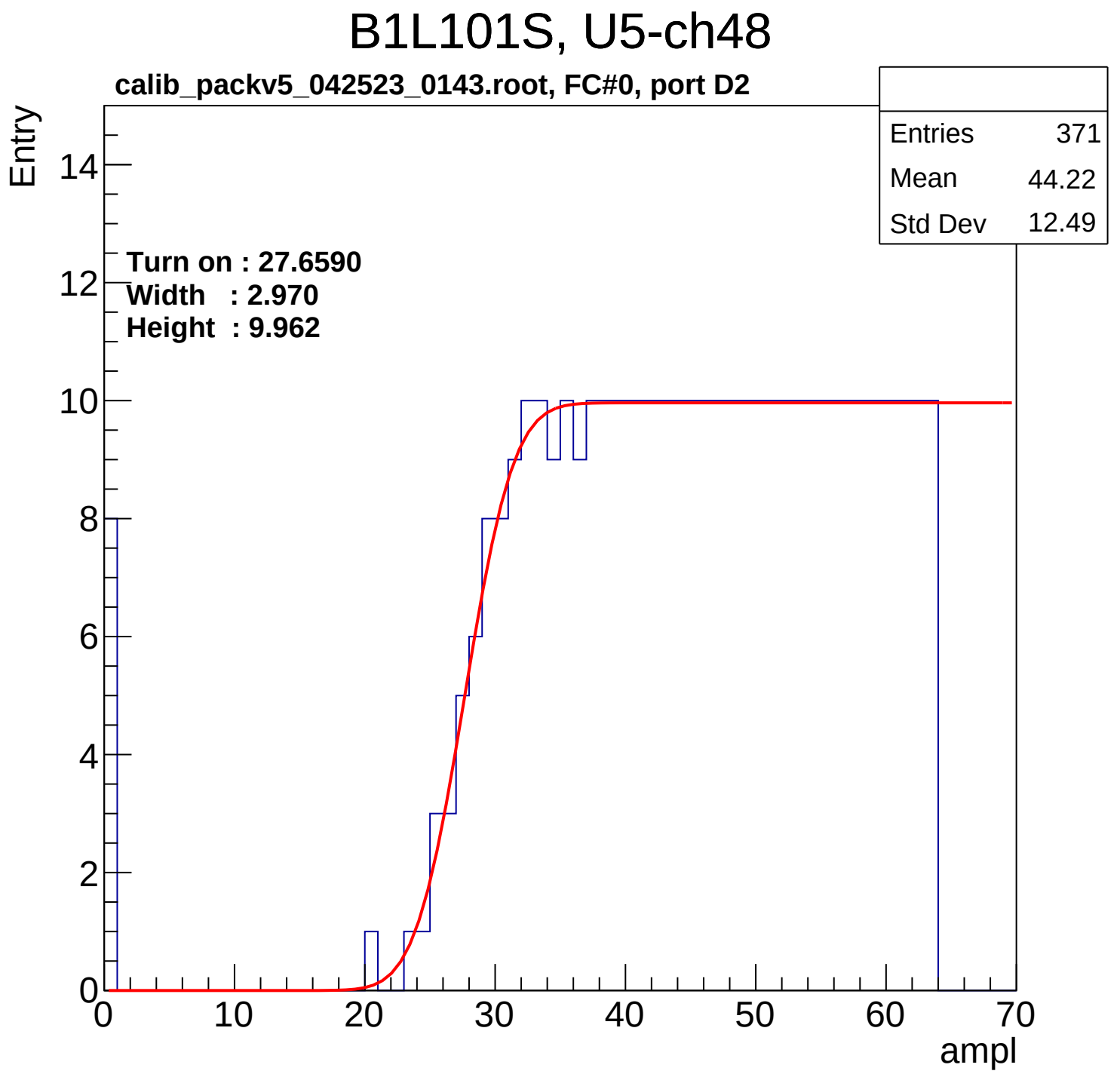

B1L101S, U5-ch43
calib_packv5_042523_0143.root, FC#0, port D2
Entries 384
Mean 43.98
Std Dev 11.82
Turn on : 26.3909
Width : 3.042
Height : 10.051
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

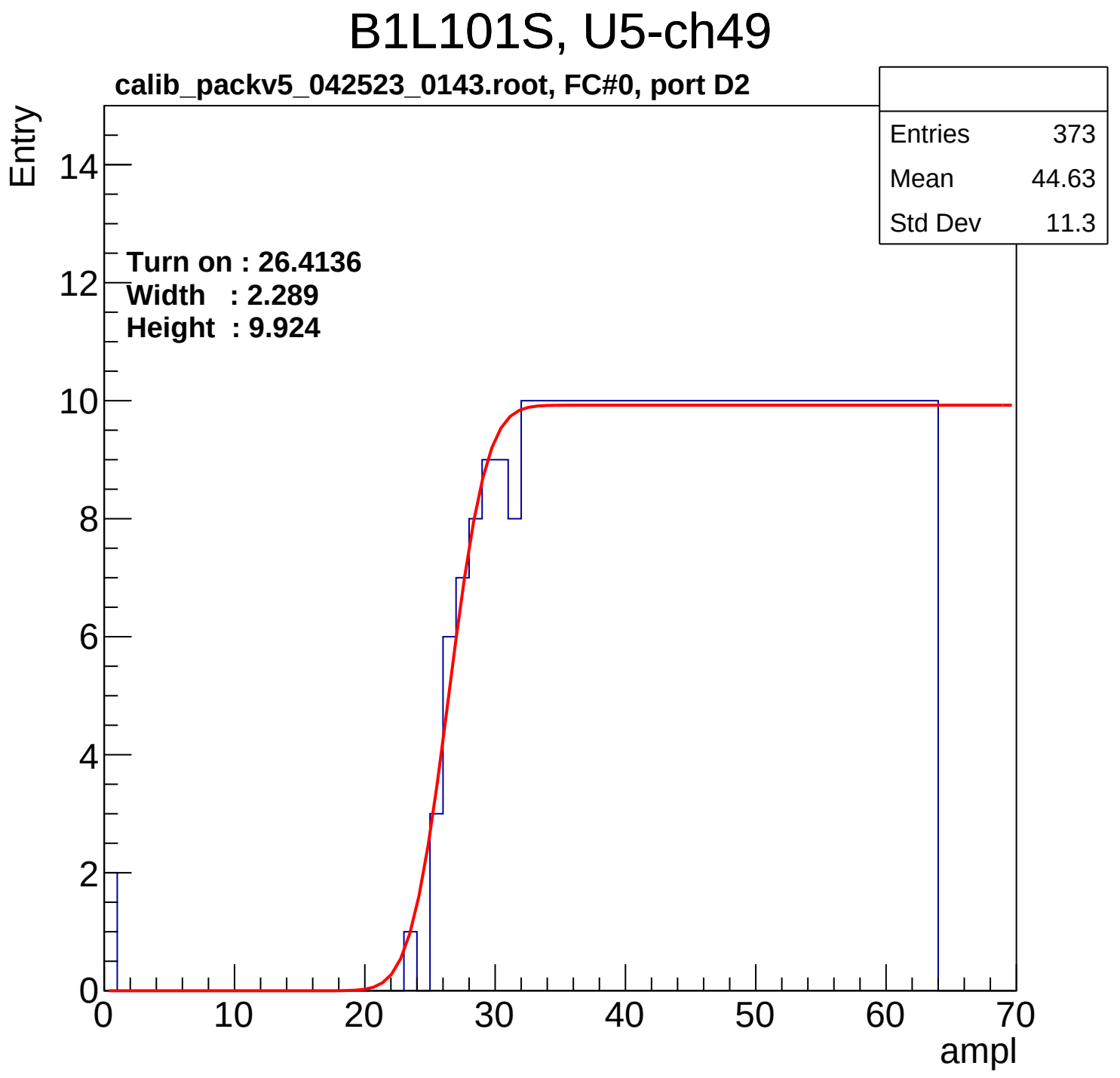

B1L101S, U5-ch44
calib_packv5_042523_0143.root, FC#0, port D2
Entries 397
Mean 43.19
Std Dev 12.55
Turn on : 24.5049
Width : 3.782
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

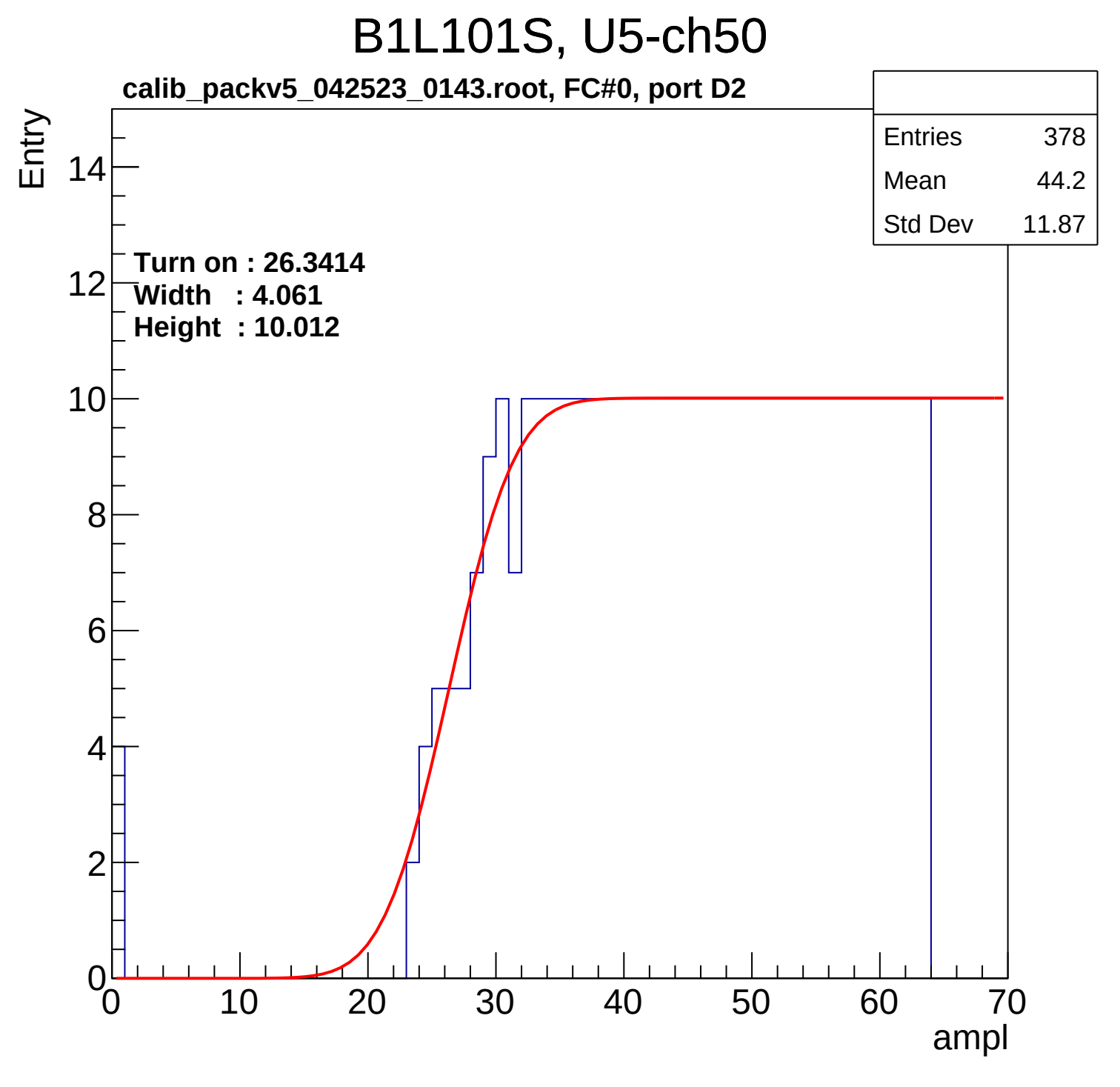

B1L101S, U5-ch45
calib_packv5_042523_0143.root, FC#0, port D2
Entries 389
Mean 43.93
Std Dev 11.51
Turn on : 25.6073
Width : 2.823
Height : 10.065
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

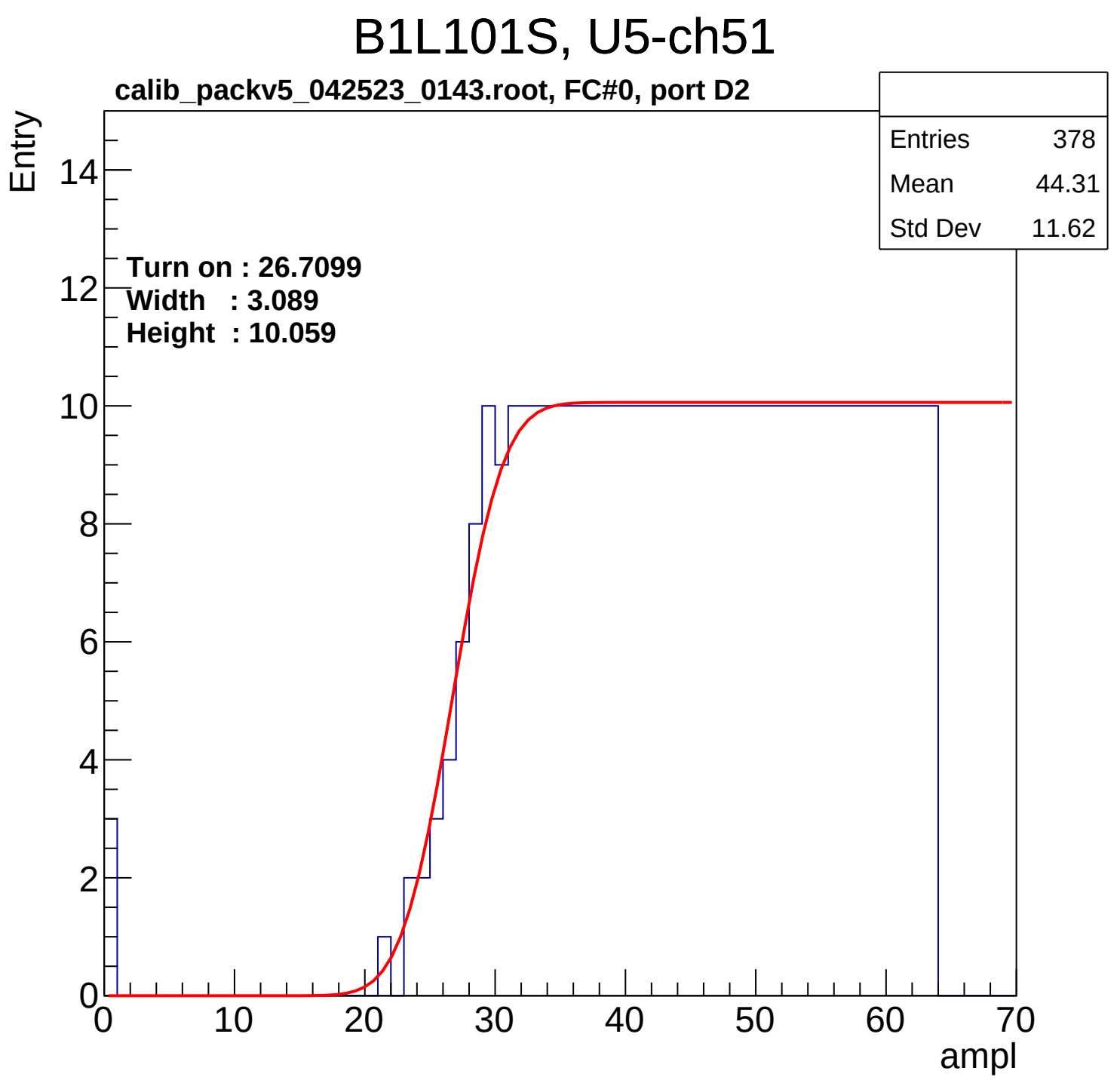

B1L101S, U5-ch46
calib_packv5_042523_0143.root, FC#0, port D2
Entries 385
Mean 43.84
Std Dev 12.13
Turn on : 26.4659
Width : 3.030
Height : 10.048
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

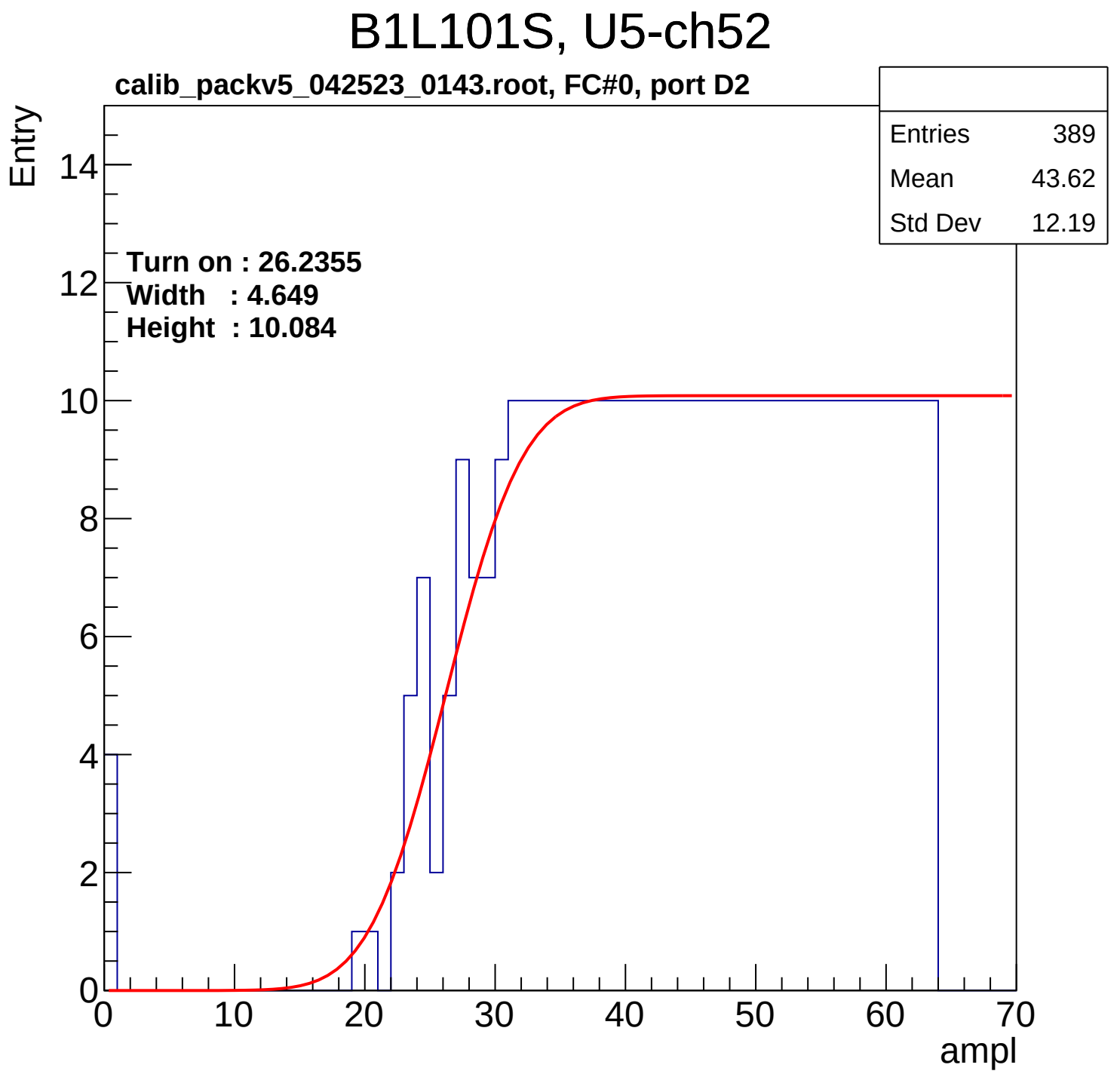

B1L101S, U5-ch47
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.28
Std Dev 11.98
Turn on : 27.3687
Width : 3.379
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

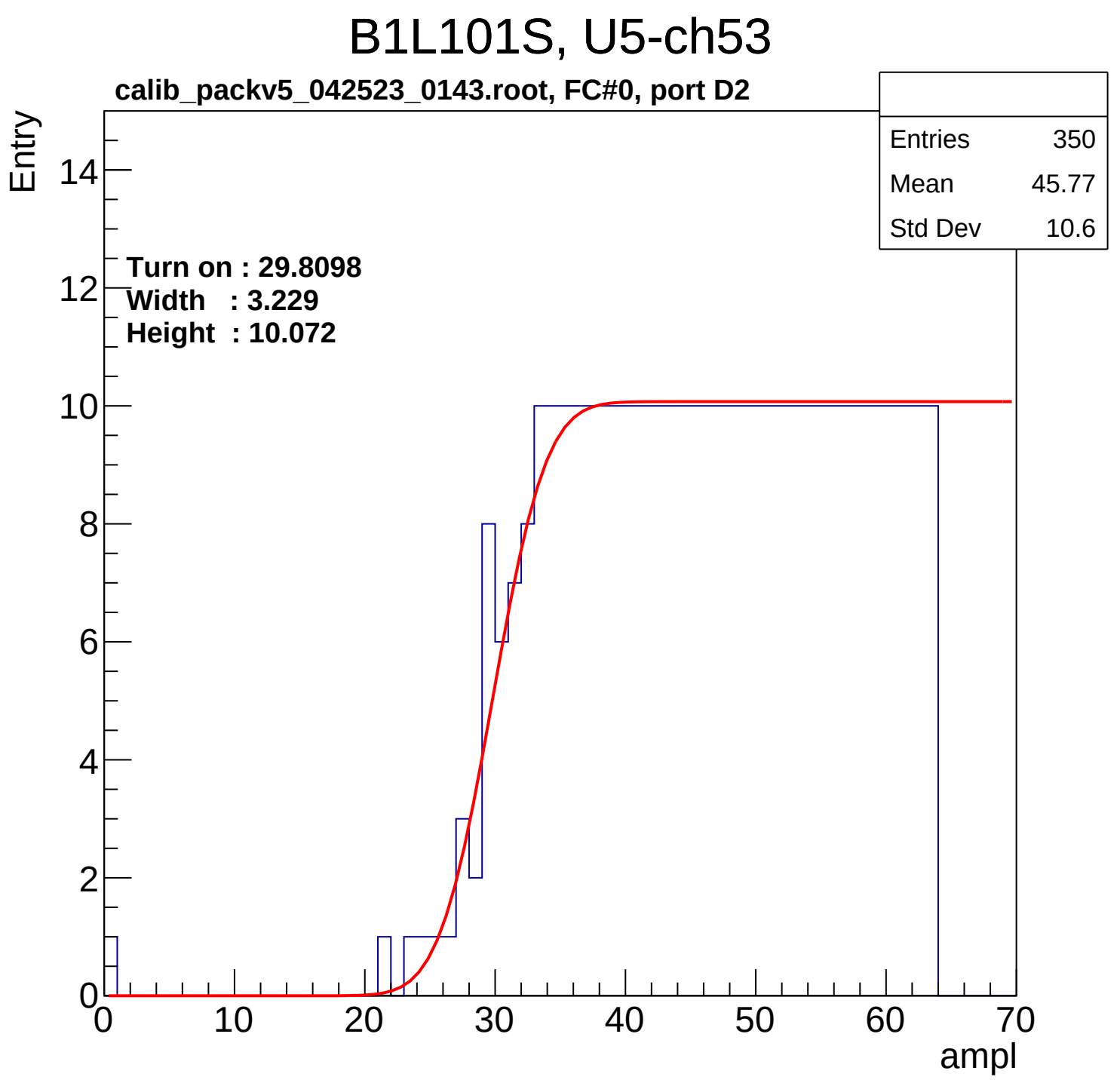

B1L101S, U5-ch48
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.22
Std Dev 12.49
Turn on : 27.6590
Width : 2.970
Height : 9.962
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

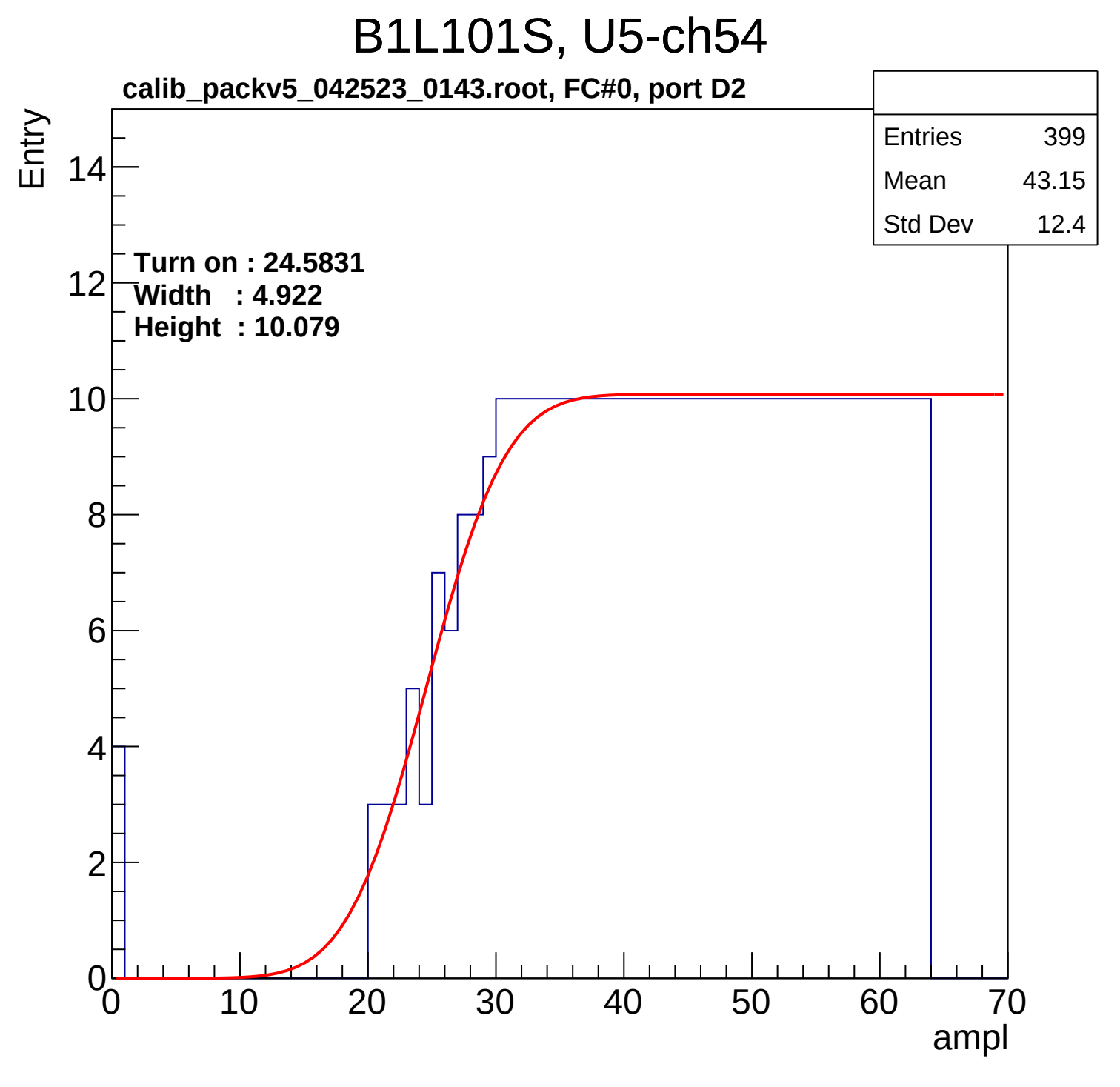

B1L101S, U5-ch49
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.63
Std Dev 11.3
Turn on : 26.4136
Width : 2.289
Height : 9.924
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

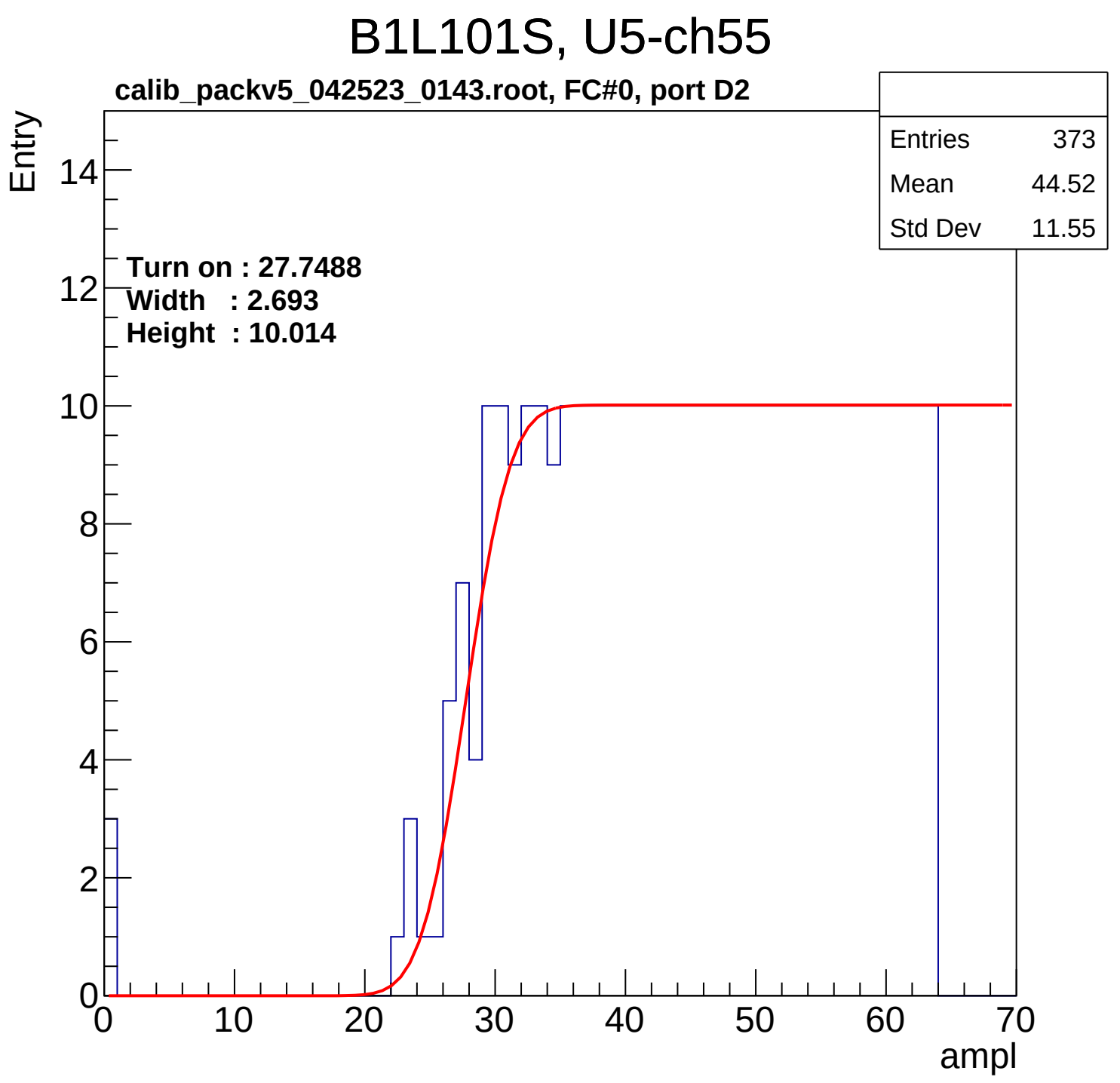

B1L101S, U5-ch50
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.2
Std Dev 11.87
Turn on : 26.3414
Width : 4.061
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

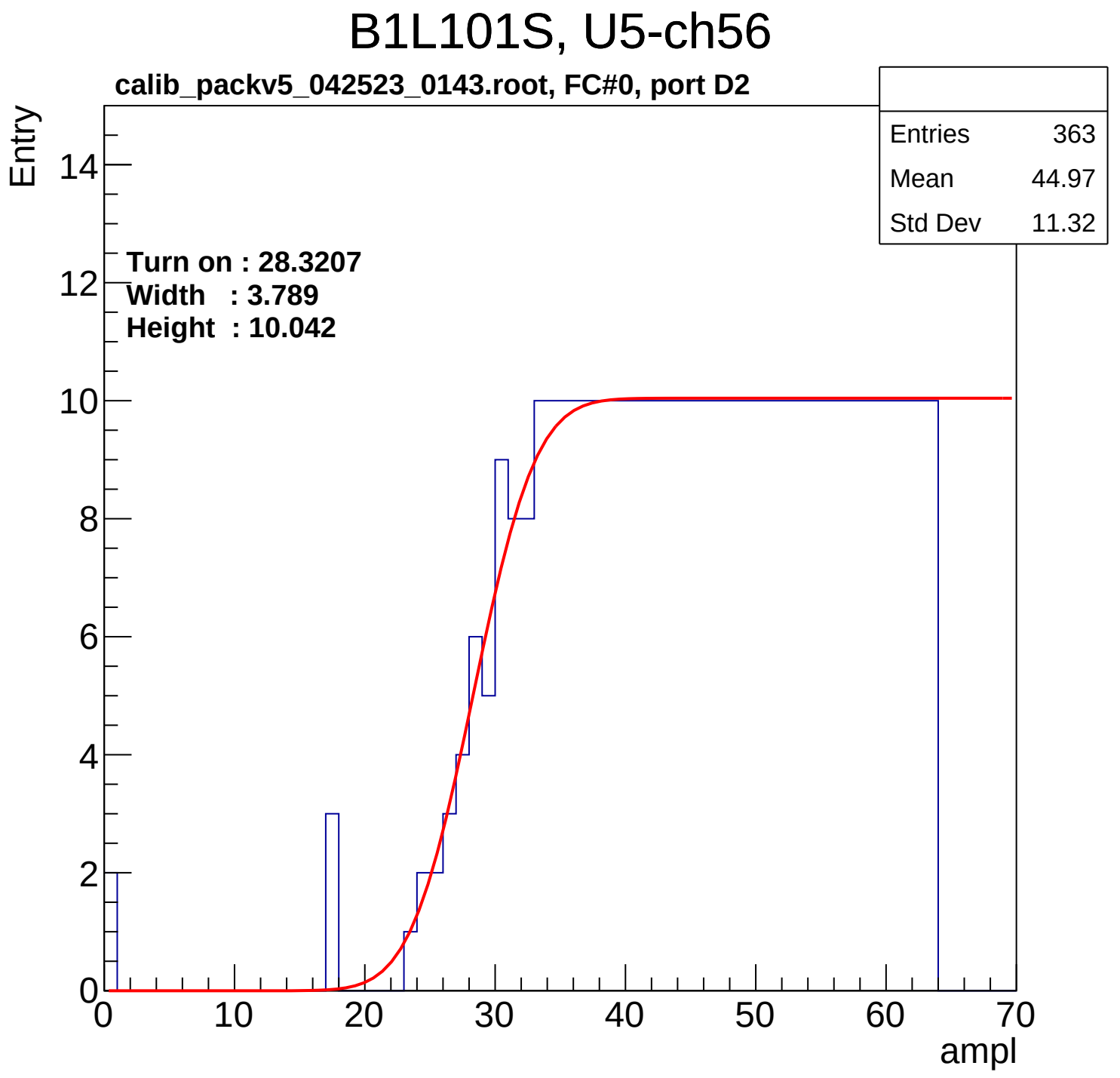

B1L101S, U5-ch51
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.31
Std Dev 11.62
Turn on : 26.7099
Width : 3.089
Height : 10.059
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

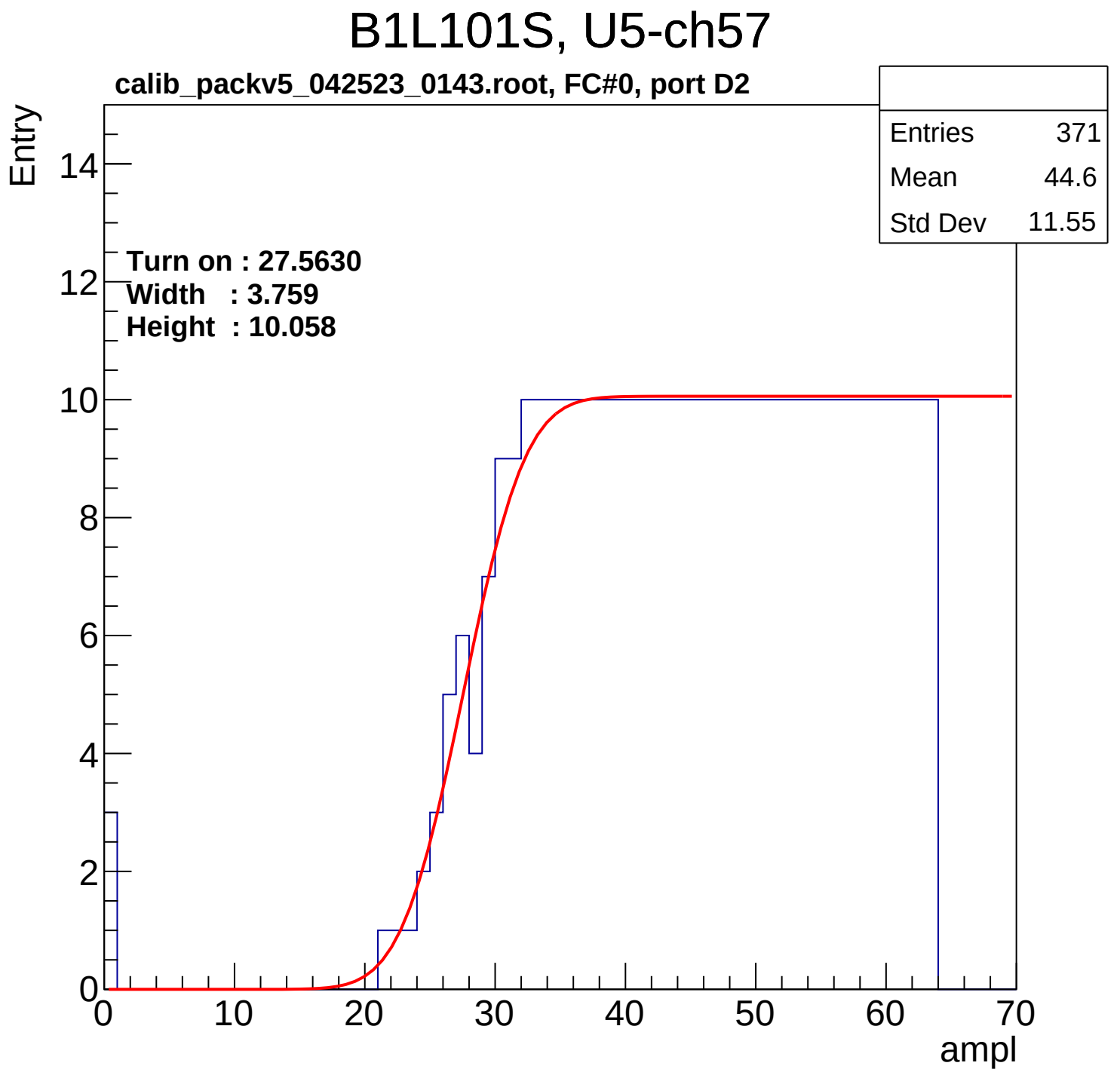

B1L101S, U5-ch52
calib_packv5_042523_0143.root, FC#0, port D2
Entries 389
Mean 43.62
Std Dev 12.19
Turn on : 26.2355
Width : 4.649
Height : 10.084
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

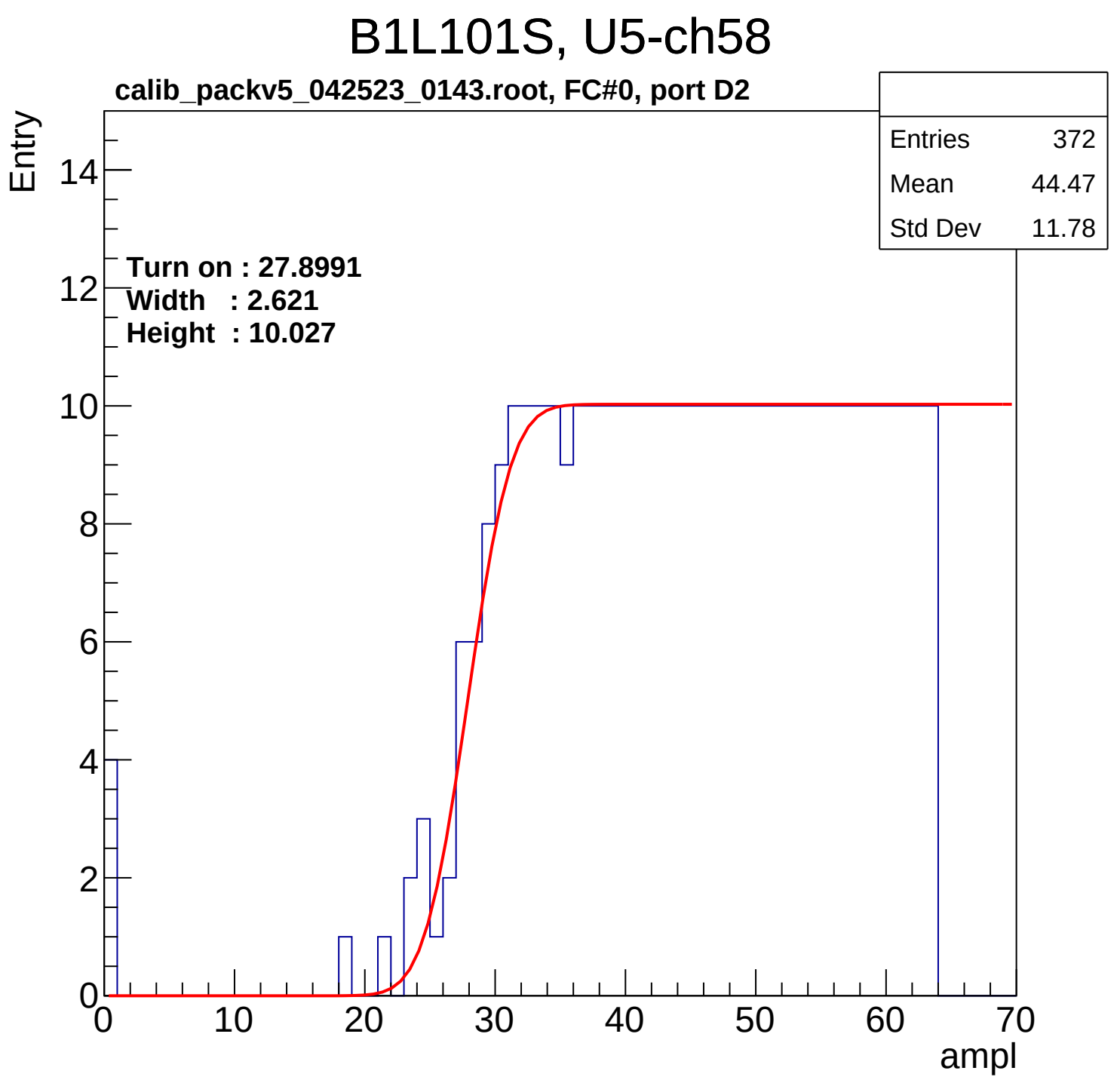

B1L101S, U5-ch53
calib_packv5_042523_0143.root, FC#0, port D2
Entries 350
Mean 45.77
Std Dev 10.6
Turn on : 29.8098
Width : 3.229
Height : 10.072
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

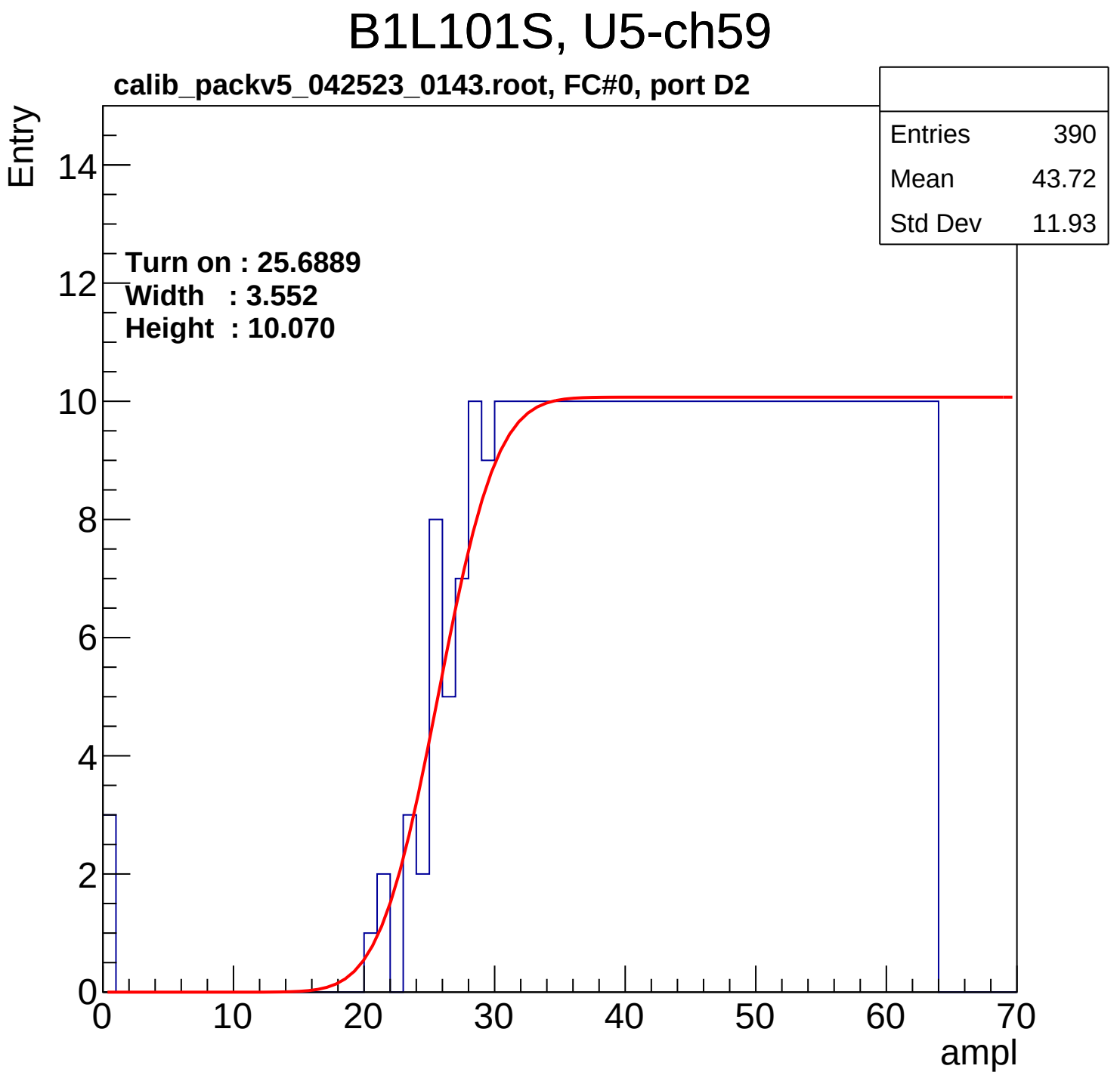

B1L101S, U5-ch54
calib_packv5_042523_0143.root, FC#0, port D2
Entries 399
Mean 43.15
Std Dev 12.4
Turn on : 24.5831
Width : 4.922
Height : 10.079
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

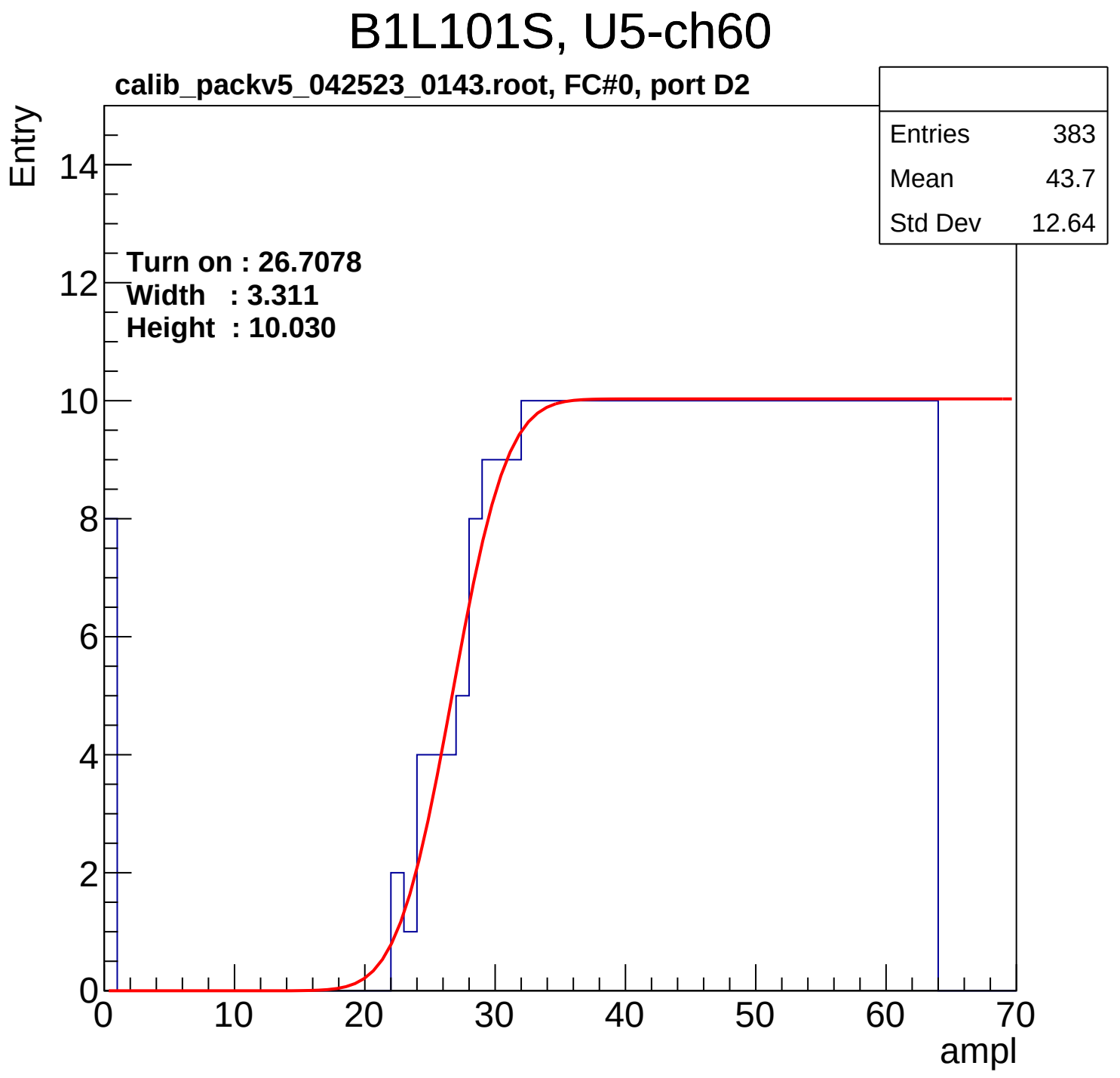

B1L101S, U5-ch55
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.52
Std Dev 11.55
Turn on : 27.7488
Width : 2.693
Height : 10.014
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

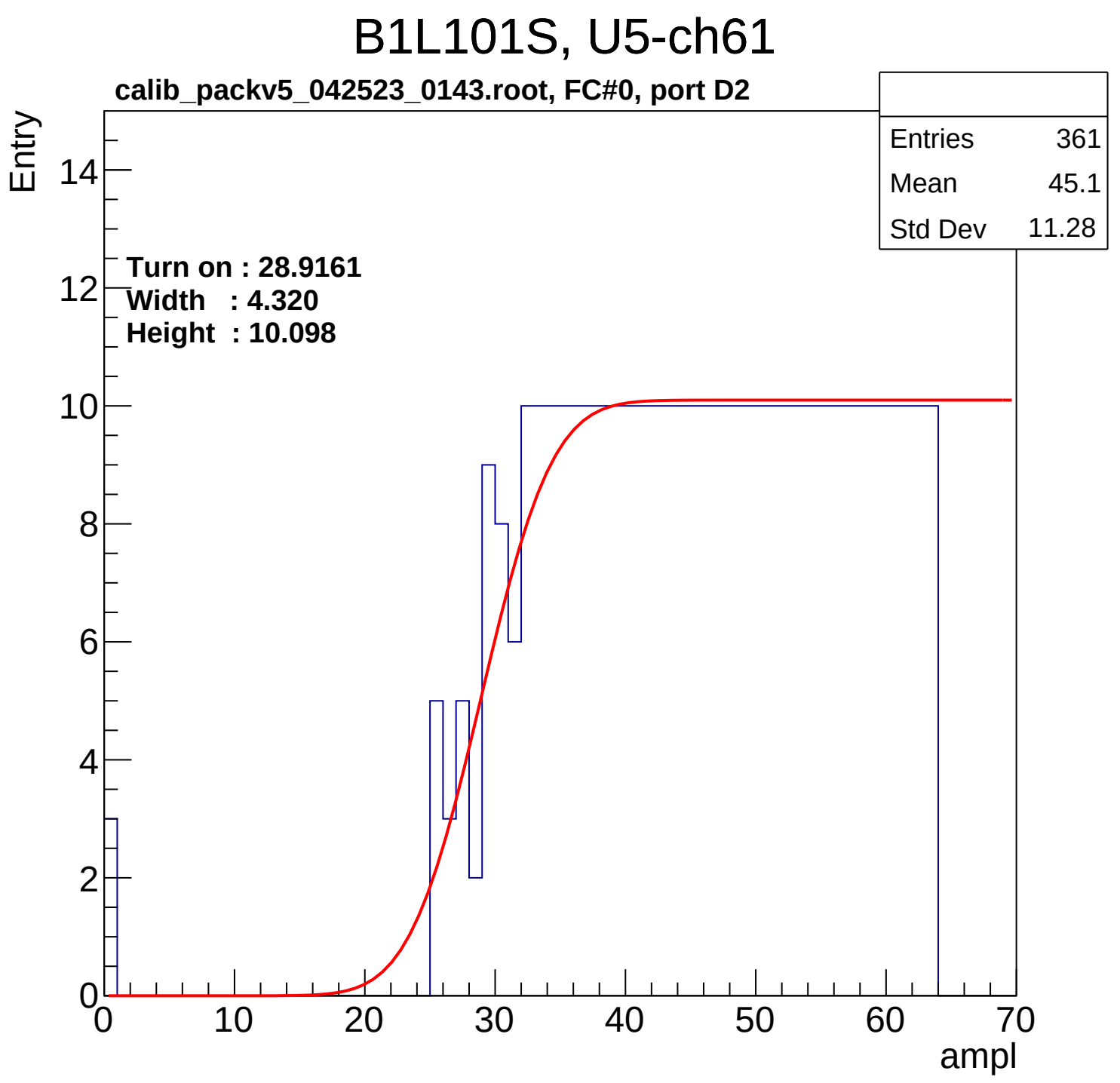

B1L101S, U5-ch56
calib_packv5_042523_0143.root, FC#0, port D2
Entries 363
Mean 44.97
Std Dev 11.32
Turn on : 28.3207
Width : 3.789
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

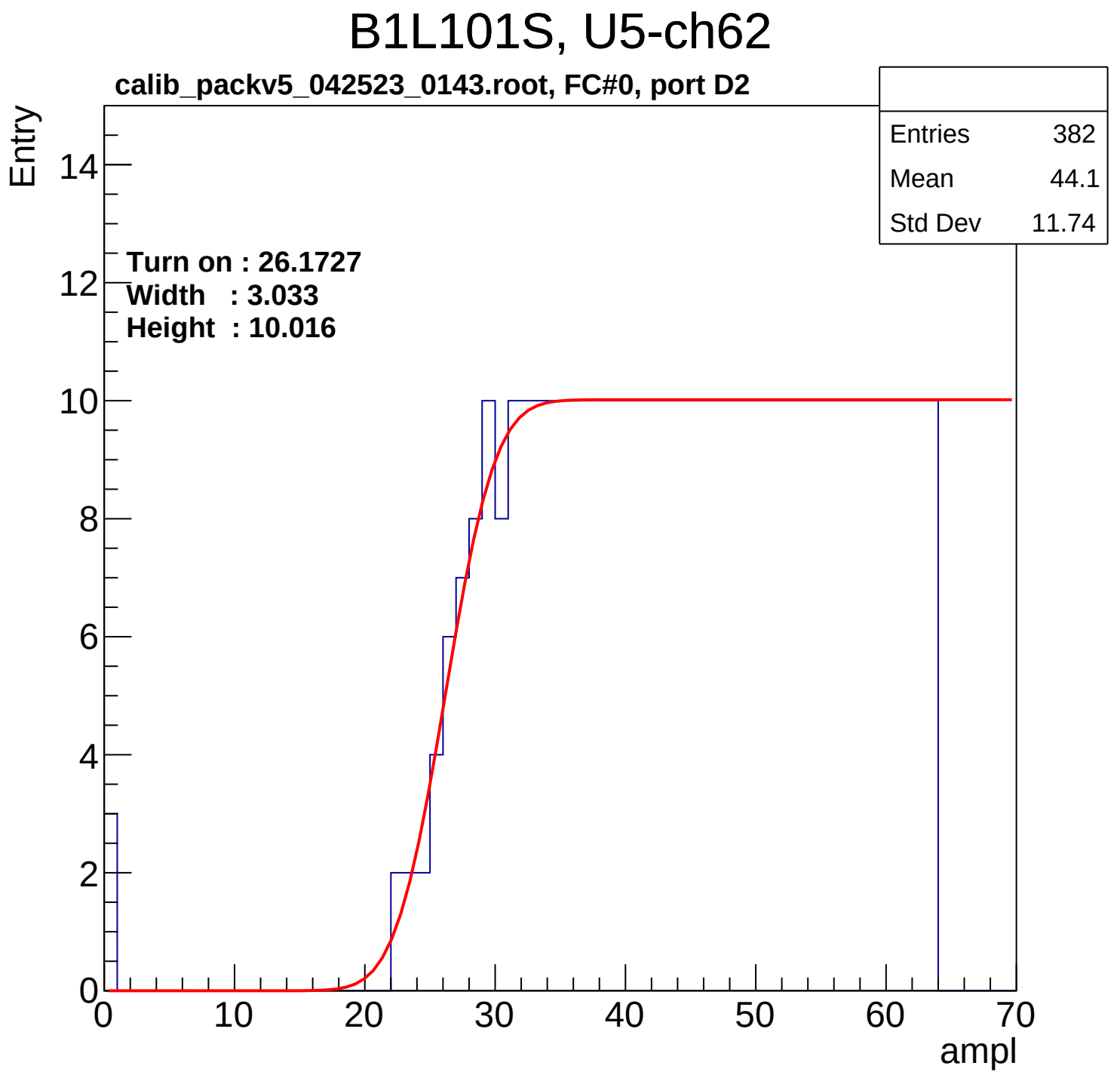

B1L101S, U5-ch57
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.6
Std Dev 11.55
Turn on : 27.5630
Width : 3.759
Height : 10.058
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

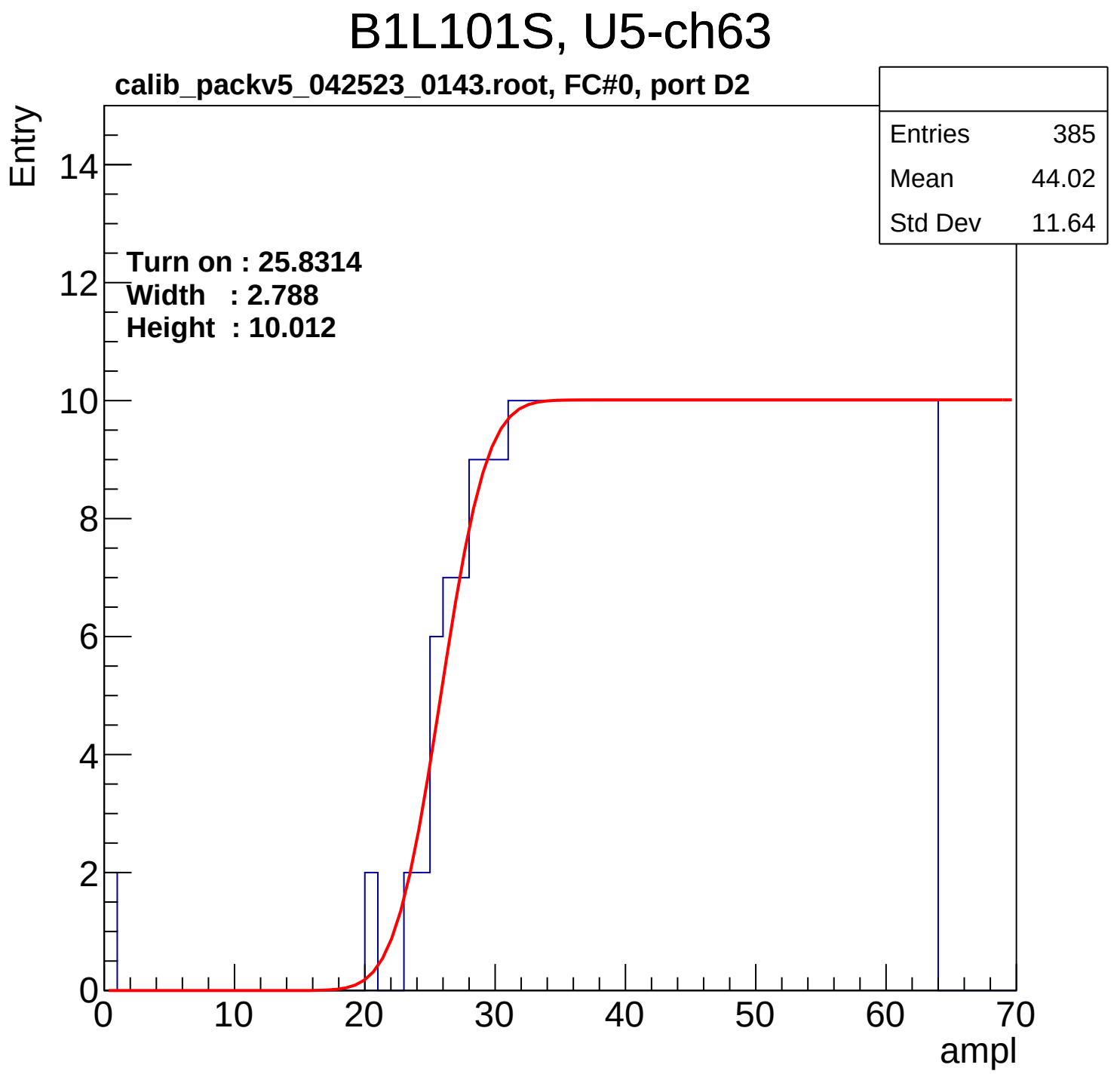

B1L101S, U5-ch58
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.47
Std Dev 11.78
Turn on : 27.8991
Width : 2.621
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

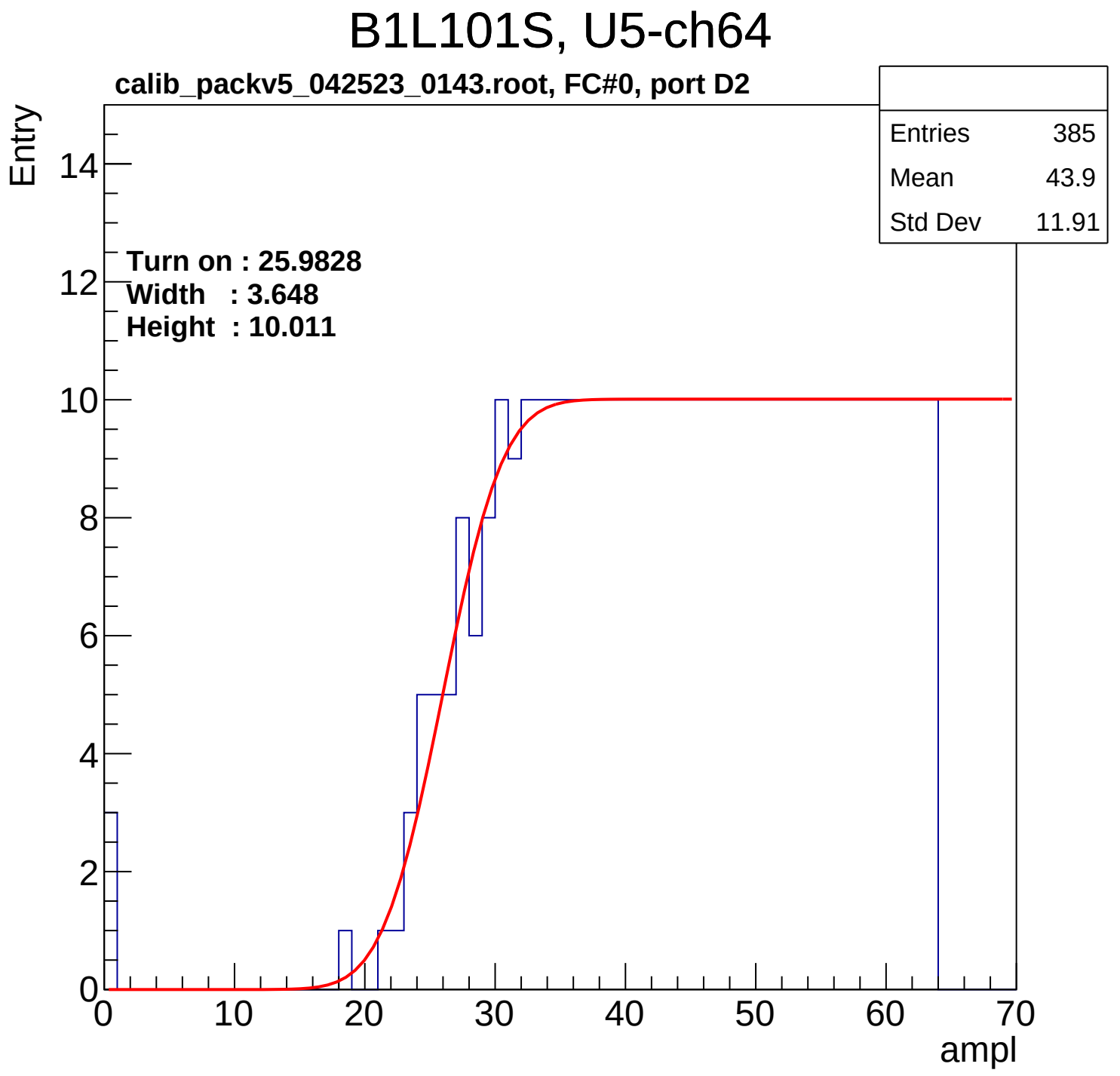

B1L101S, U5-ch59
calib_packv5_042523_0143.root, FC#0, port D2
Entries 390
Mean 43.72
Std Dev 11.93
Turn on : 25.6889
Width : 3.552
Height : 10.070
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

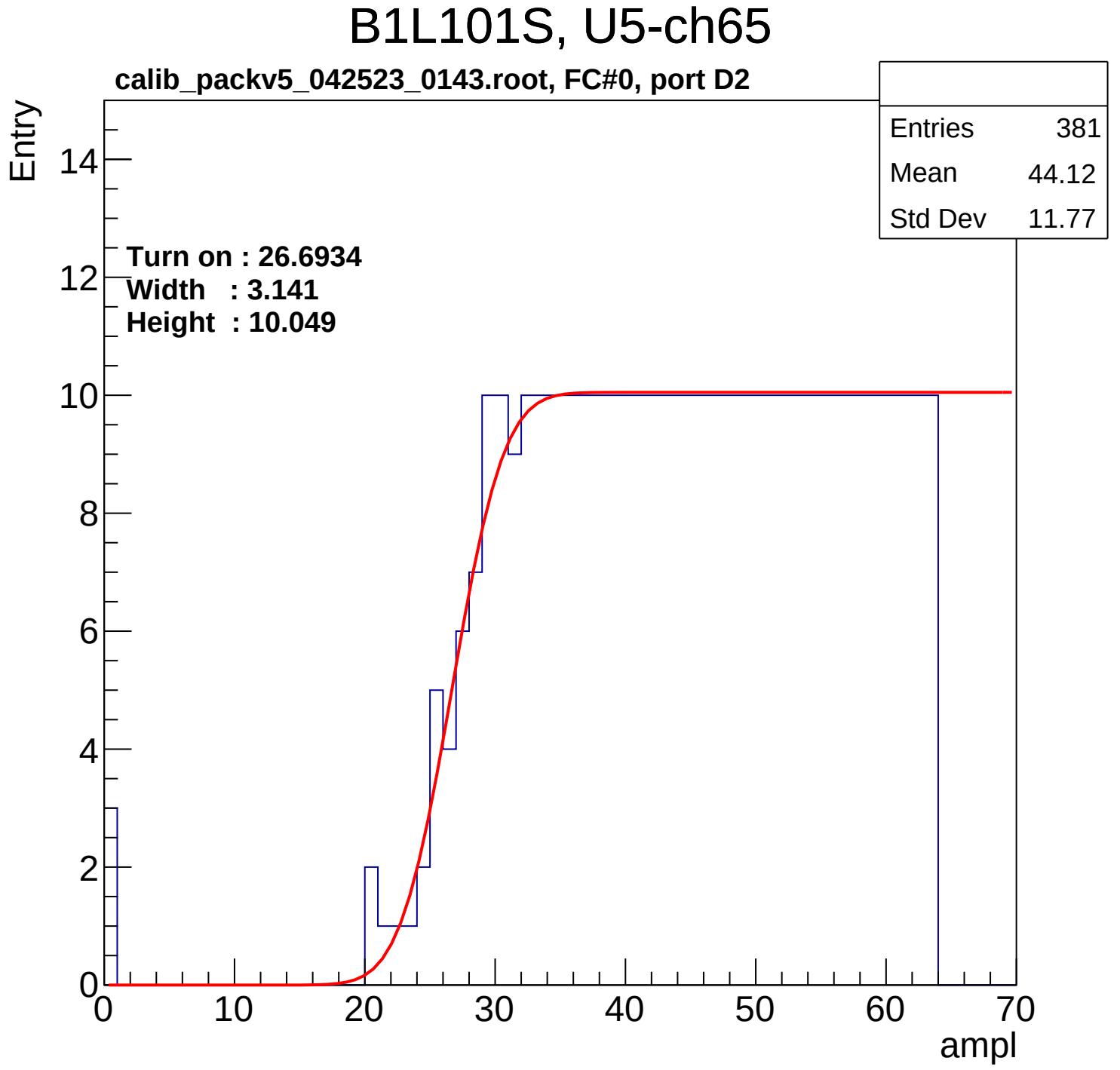

B1L101S, U5-ch60
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 43.7
Std Dev 12.64
Turn on : 26.7078
Width : 3.311
Height : 10.030
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

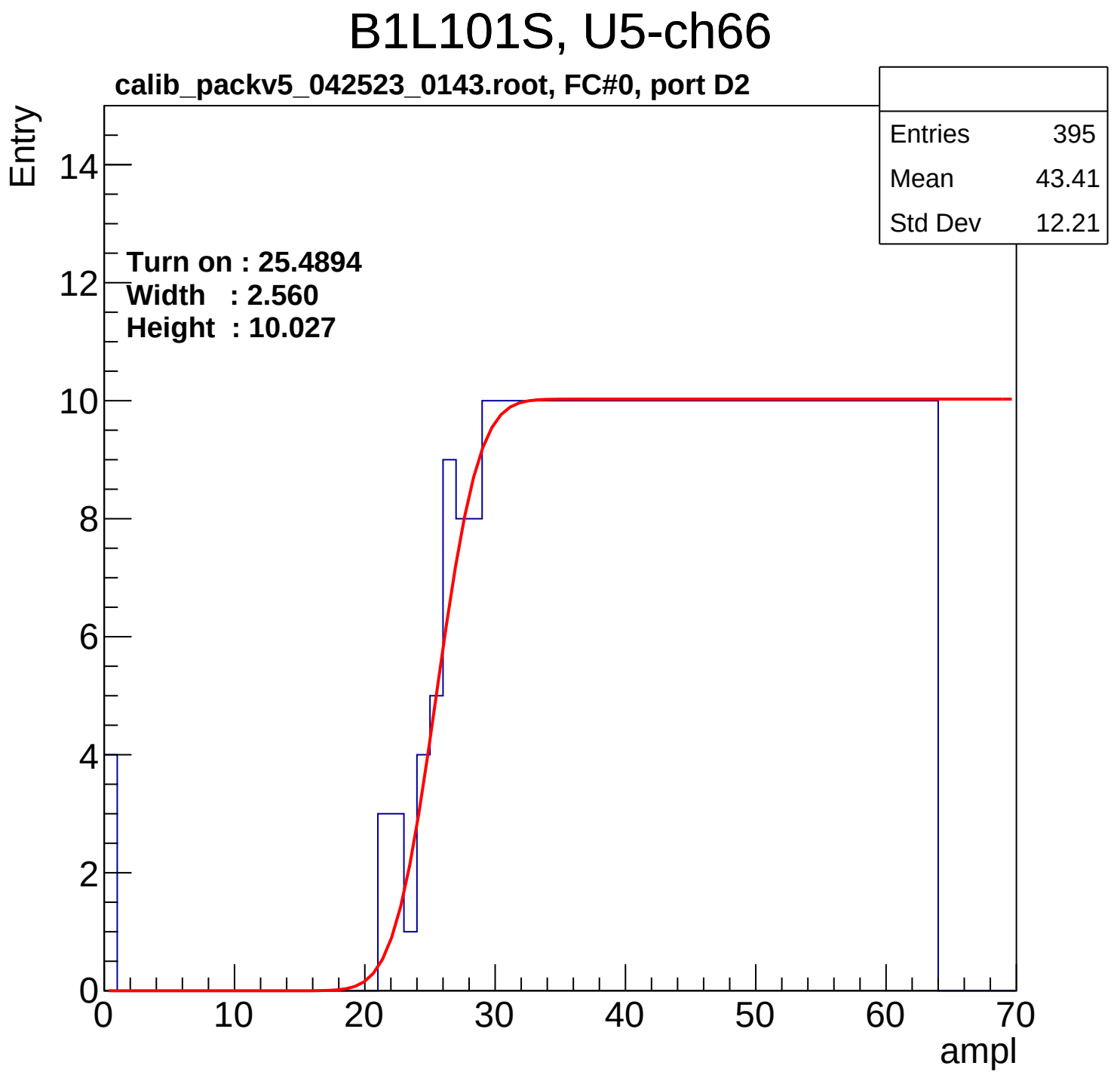

B1L101S, U5-ch61
calib_packv5_042523_0143.root, FC#0, port D2
Entries 361
Mean 45.1
Std Dev 11.28
Turn on : 28.9161
Width : 4.320
Height : 10.098
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

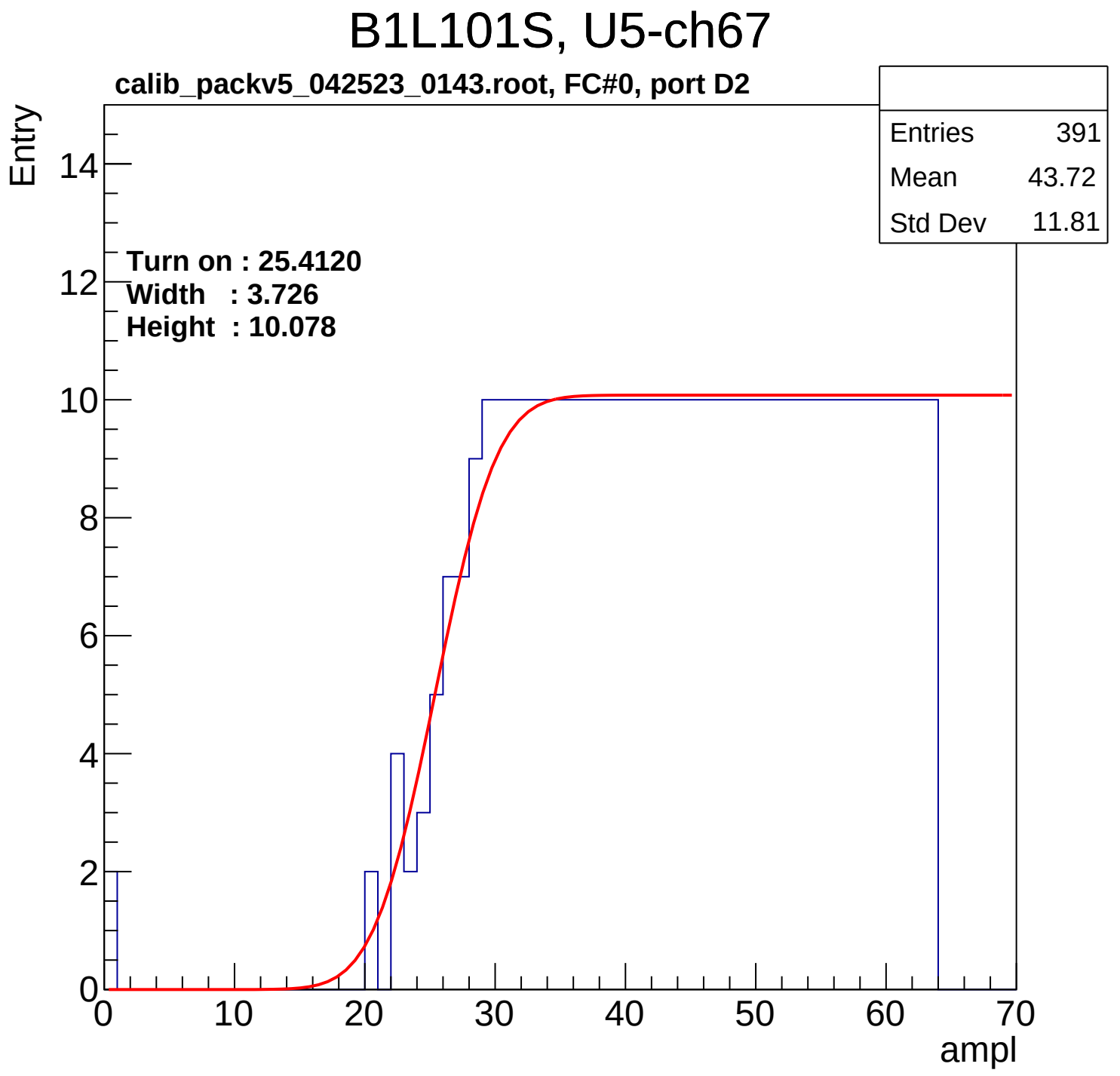

B1L101S, U5-ch62
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 44.1
Std Dev 11.74
Turn on : 26.1727
Width : 3.033
Height : 10.016
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

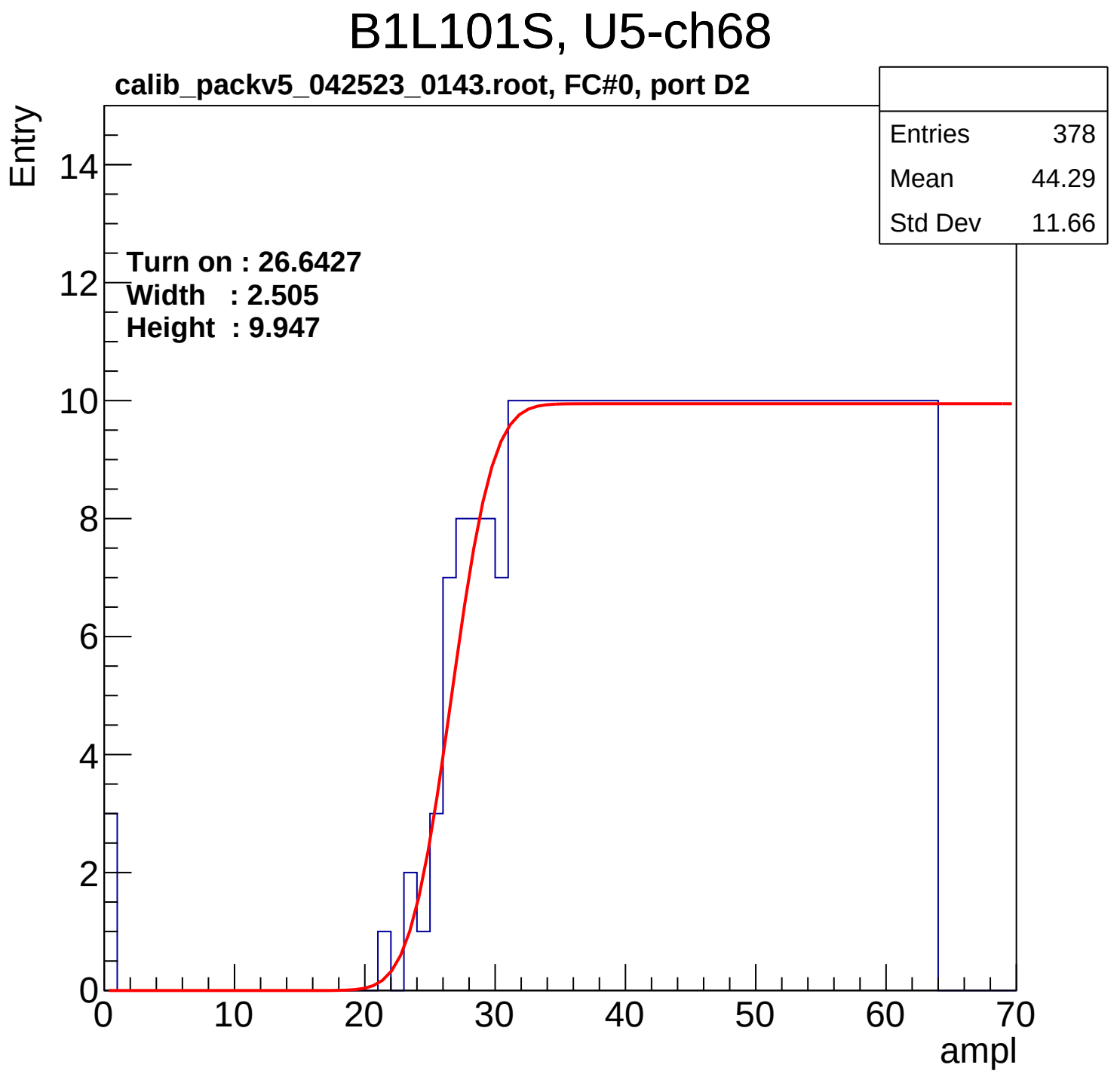

B1L101S, U5-ch63
calib_packv5_042523_0143.root, FC#0, port D2
Entries 385
Mean 44.02
Std Dev 11.64
Turn on : 25.8314
Width : 2.788
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

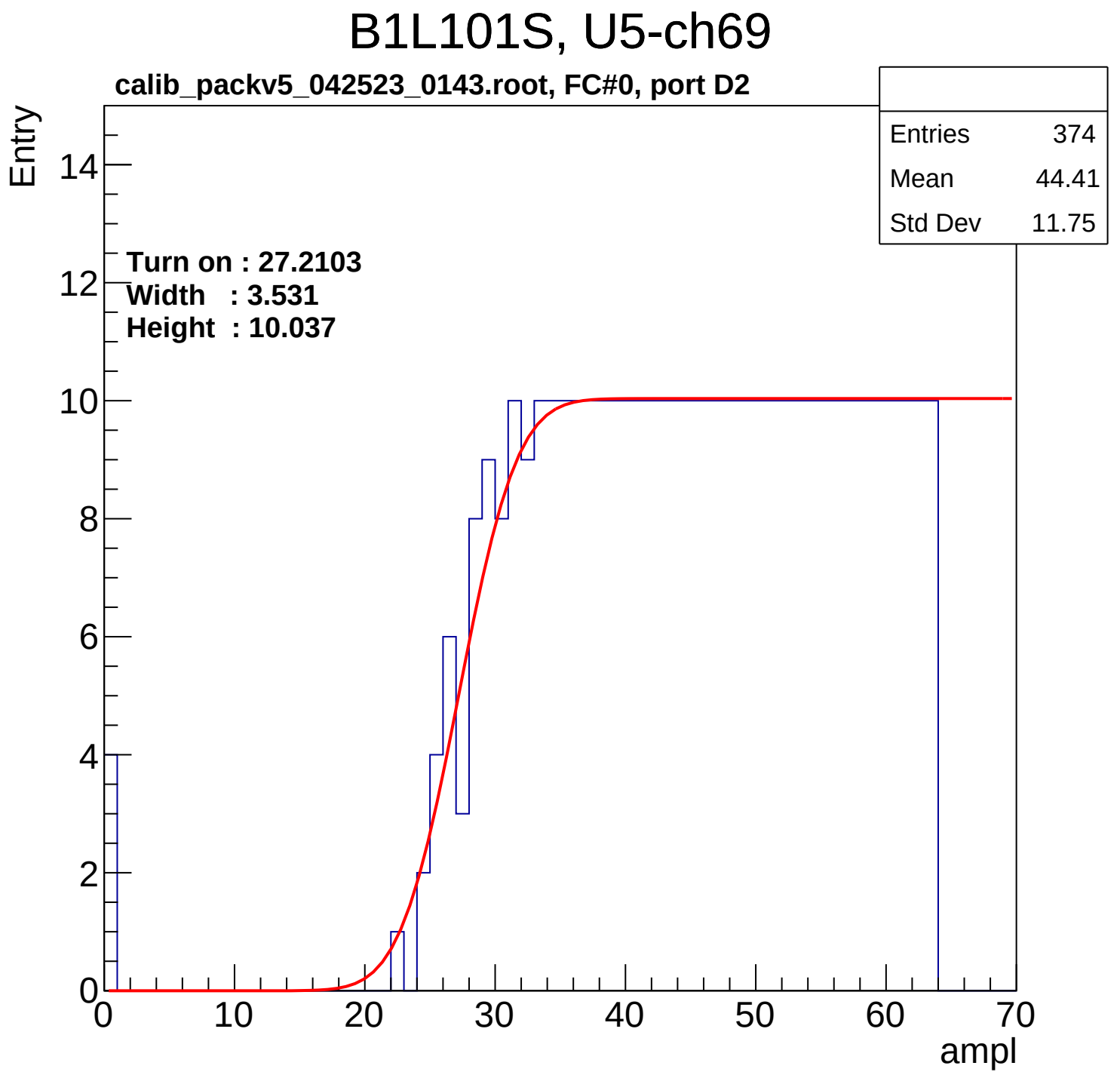

B1L101S, U5-ch64
calib_packv5_042523_0143.root, FC#0, port D2
Entries 385
Mean 43.9
Std Dev 11.91
Turn on : 25.9828
Width : 3.648
Height : 10.011
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

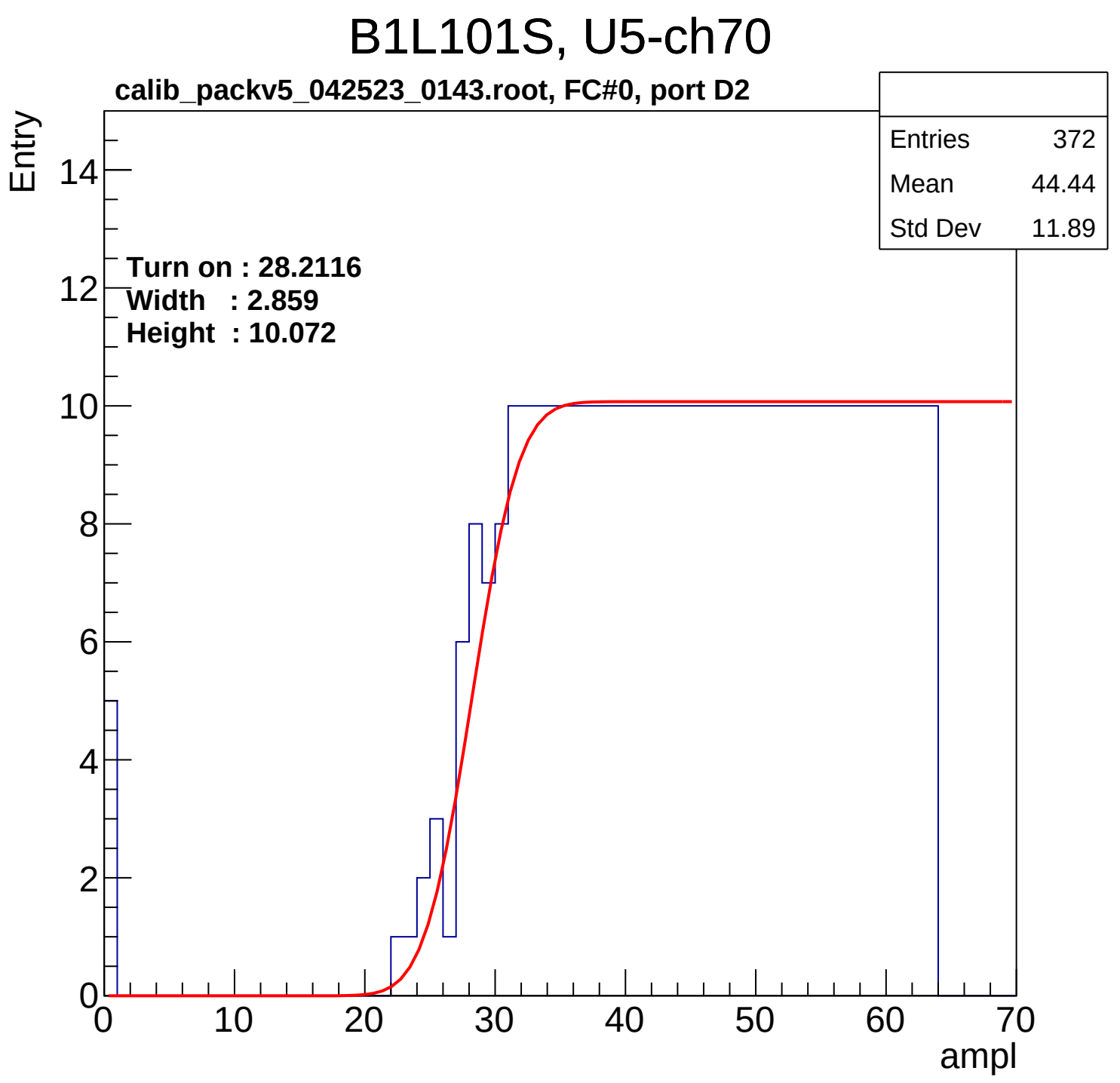

B1L101S, U5-ch65
calib_packv5_042523_0143.root, FC#0, port D2
Entries 381
Mean 44.12
Std Dev 11.77
Turn on : 26.6934
Width : 3.141
Height : 10.049
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

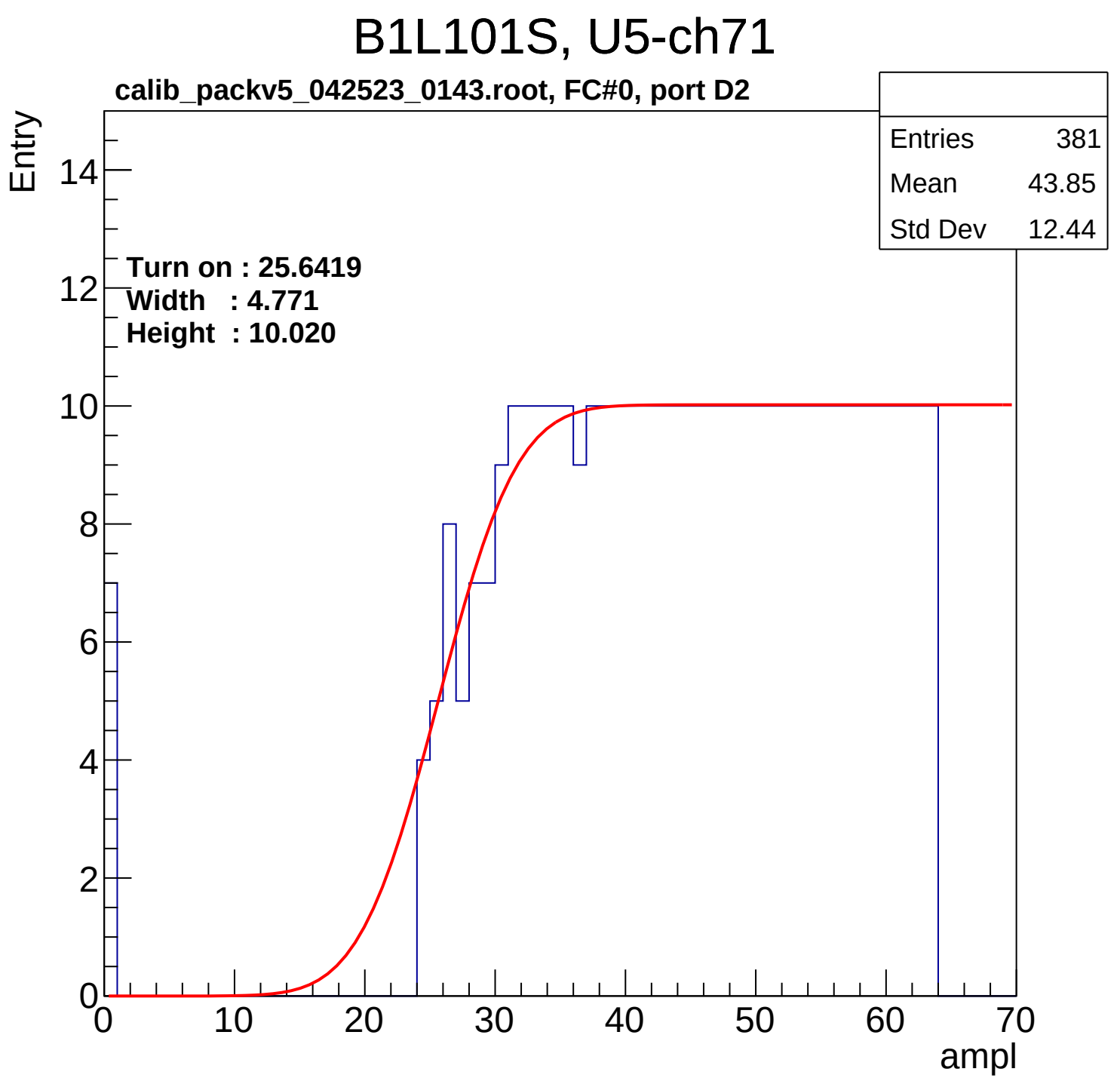

B1L101S, U5-ch66
calib_packv5_042523_0143.root, FC#0, port D2
Entries 395
Mean 43.41
Std Dev 12.21
Turn on : 25.4894
Width : 2.560
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

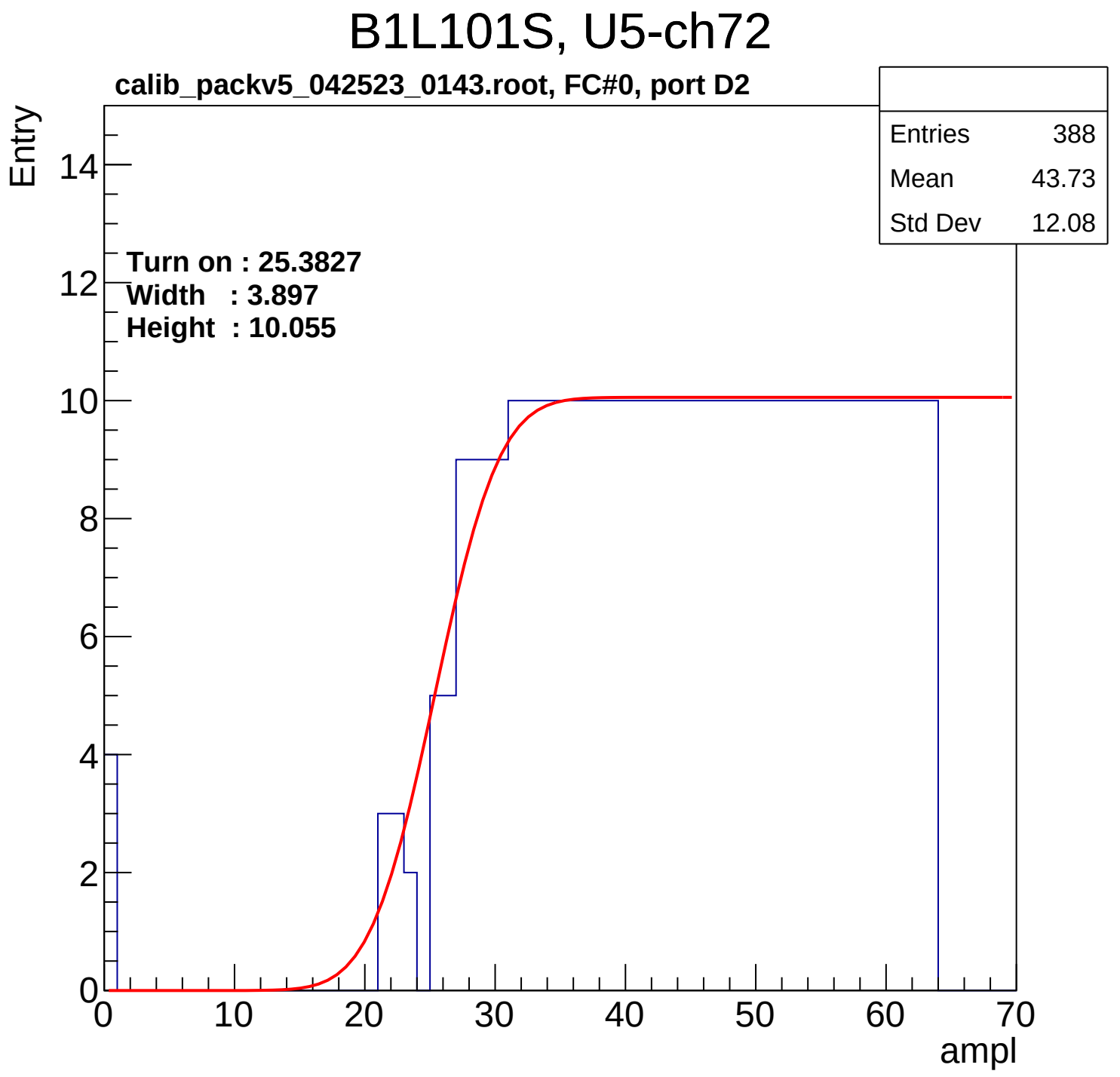

B1L101S, U5-ch67
calib_packv5_042523_0143.root, FC#0, port D2
Entries 391
Mean 43.72
Std Dev 11.81
Turn on : 25.4120
Width : 3.726
Height : 10.078
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

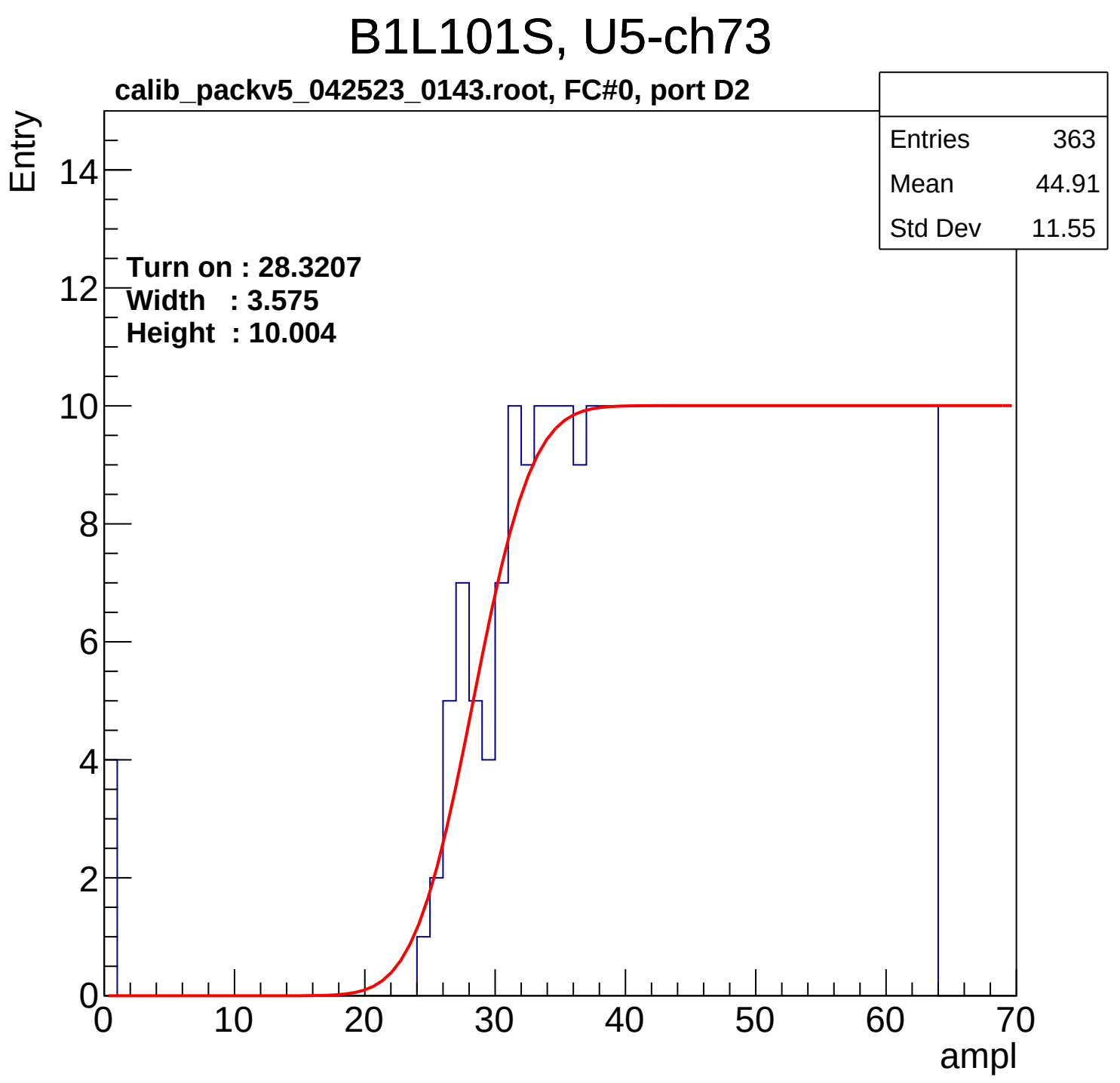

B1L101S, U5-ch68
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.29
Std Dev 11.66
Turn on : 26.6427
Width : 2.505
Height : 9.947
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

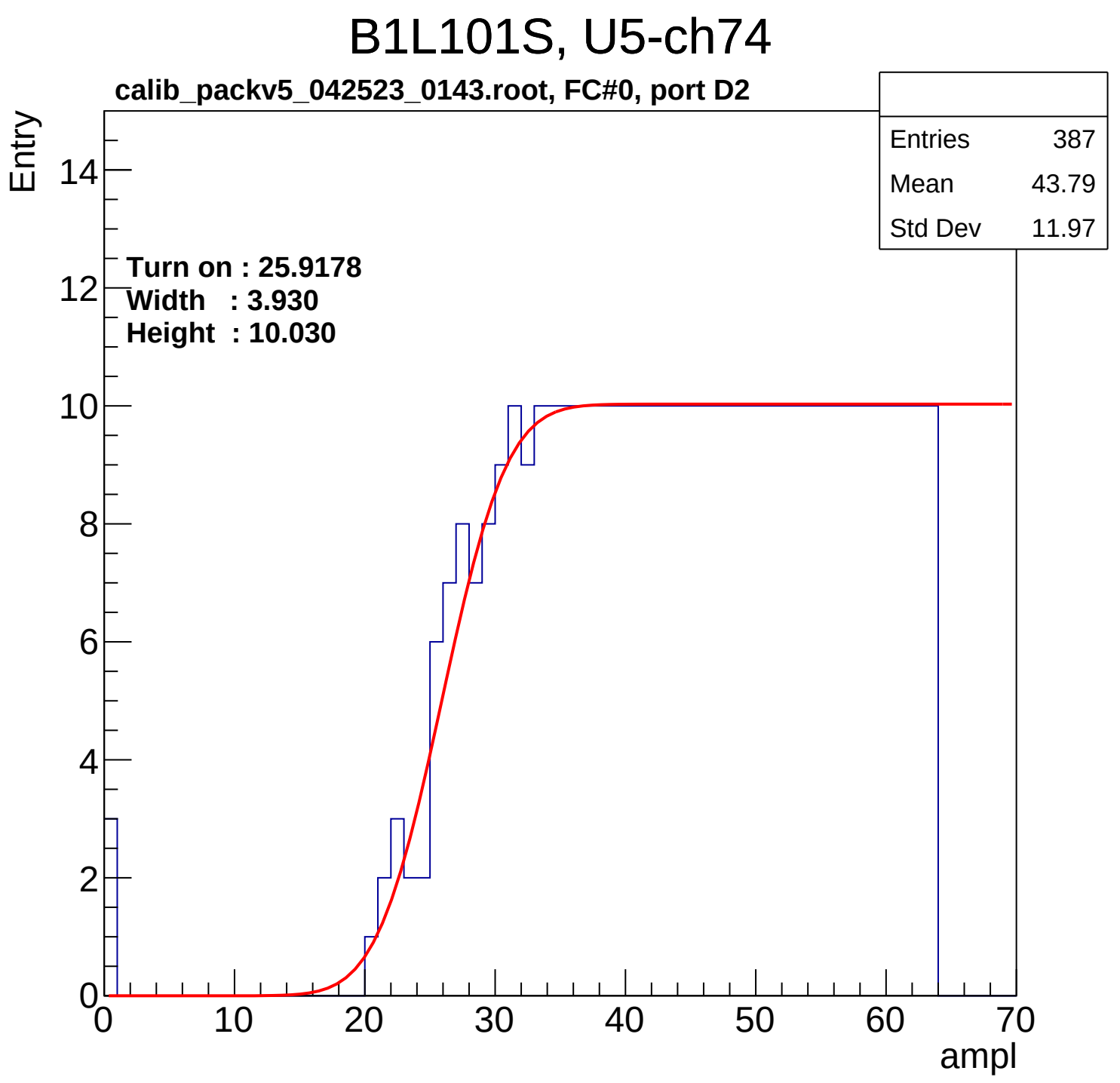

B1L101S, U5-ch69
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.41
Std Dev 11.75
Turn on : 27.2103
Width : 3.531
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

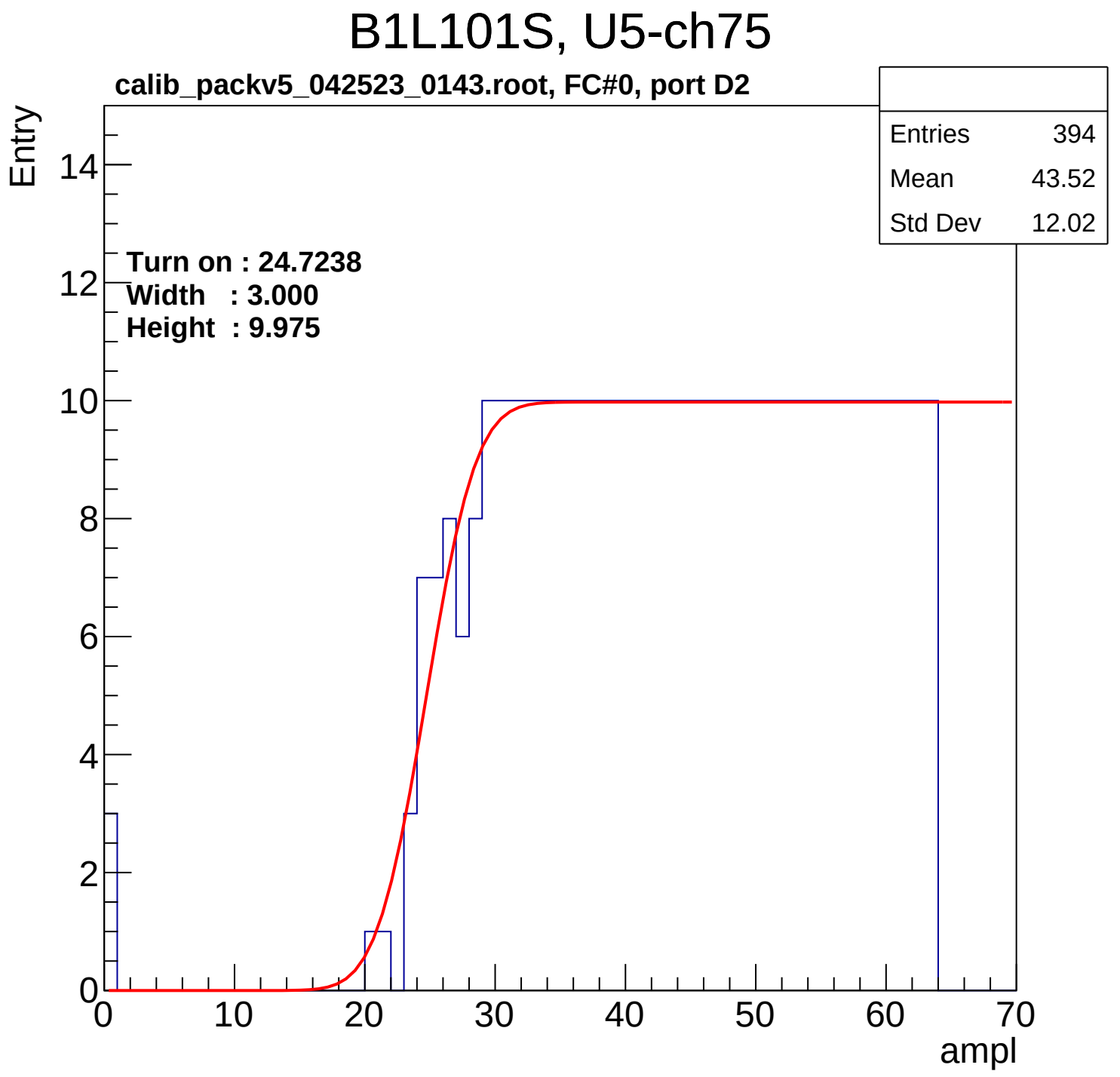

B1L101S, U5-ch70
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.44
Std Dev 11.89
Turn on : 28.2116
Width : 2.859
Height : 10.072
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

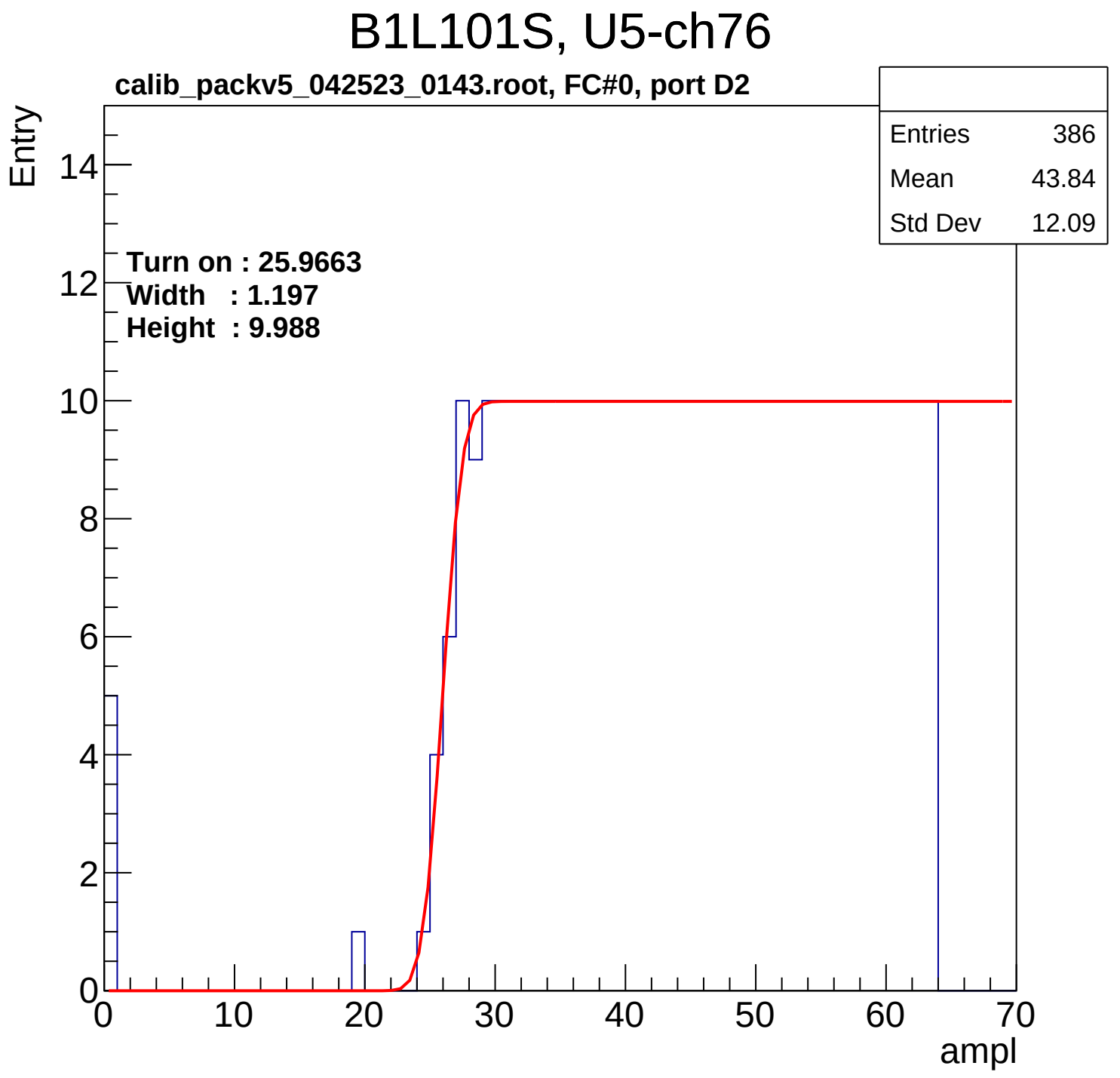

B1L101S, U5-ch71
calib_packv5_042523_0143.root, FC#0, port D2
Entries 381
Mean 43.85
Std Dev 12.44
Turn on : 25.6419
Width : 4.771
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

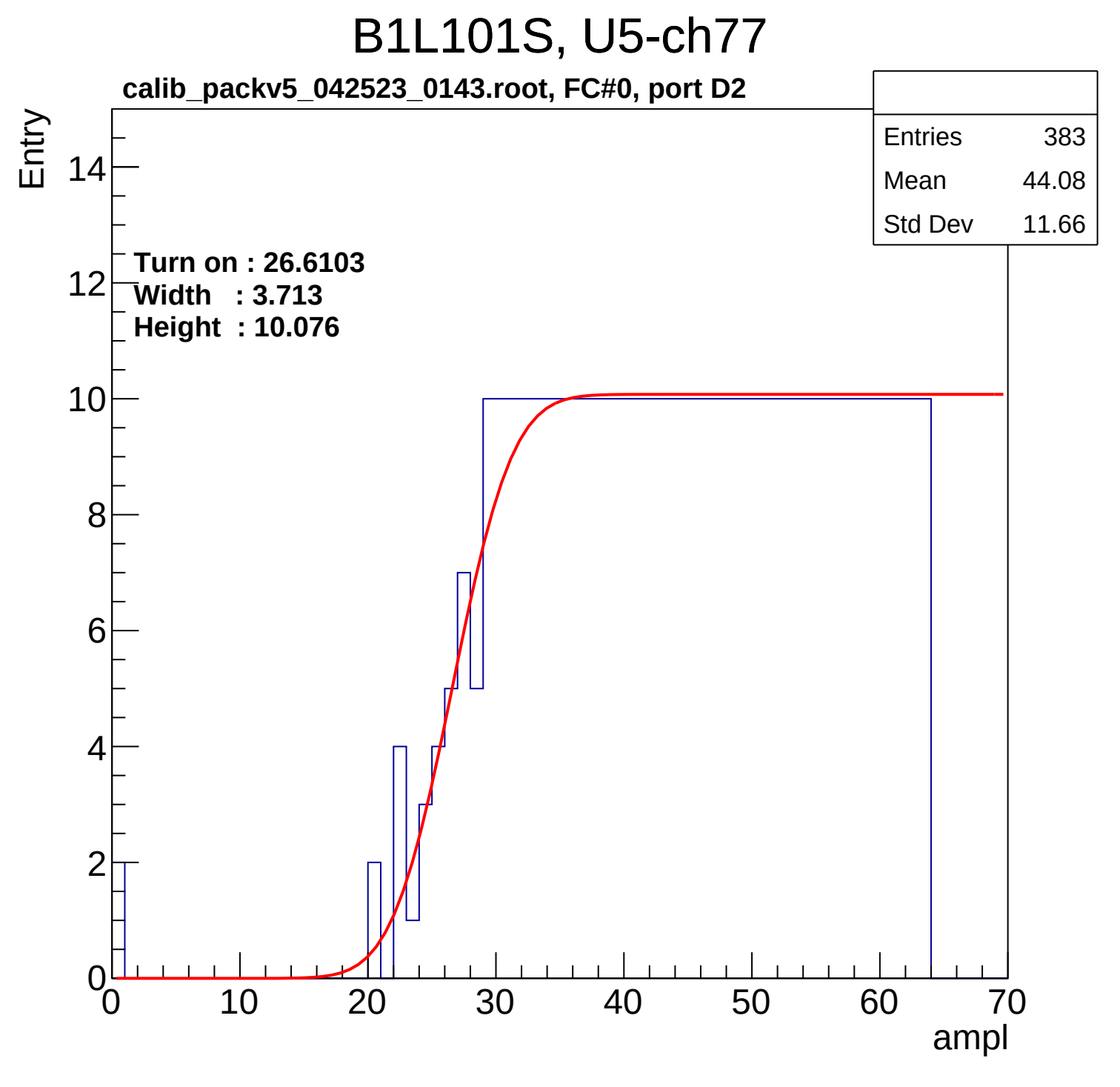

B1L101S, U5-ch72
calib_packv5_042523_0143.root, FC#0, port D2
Entries 388
Mean 43.73
Std Dev 12.08
Turn on : 25.3827
Width : 3.897
Height : 10.055
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

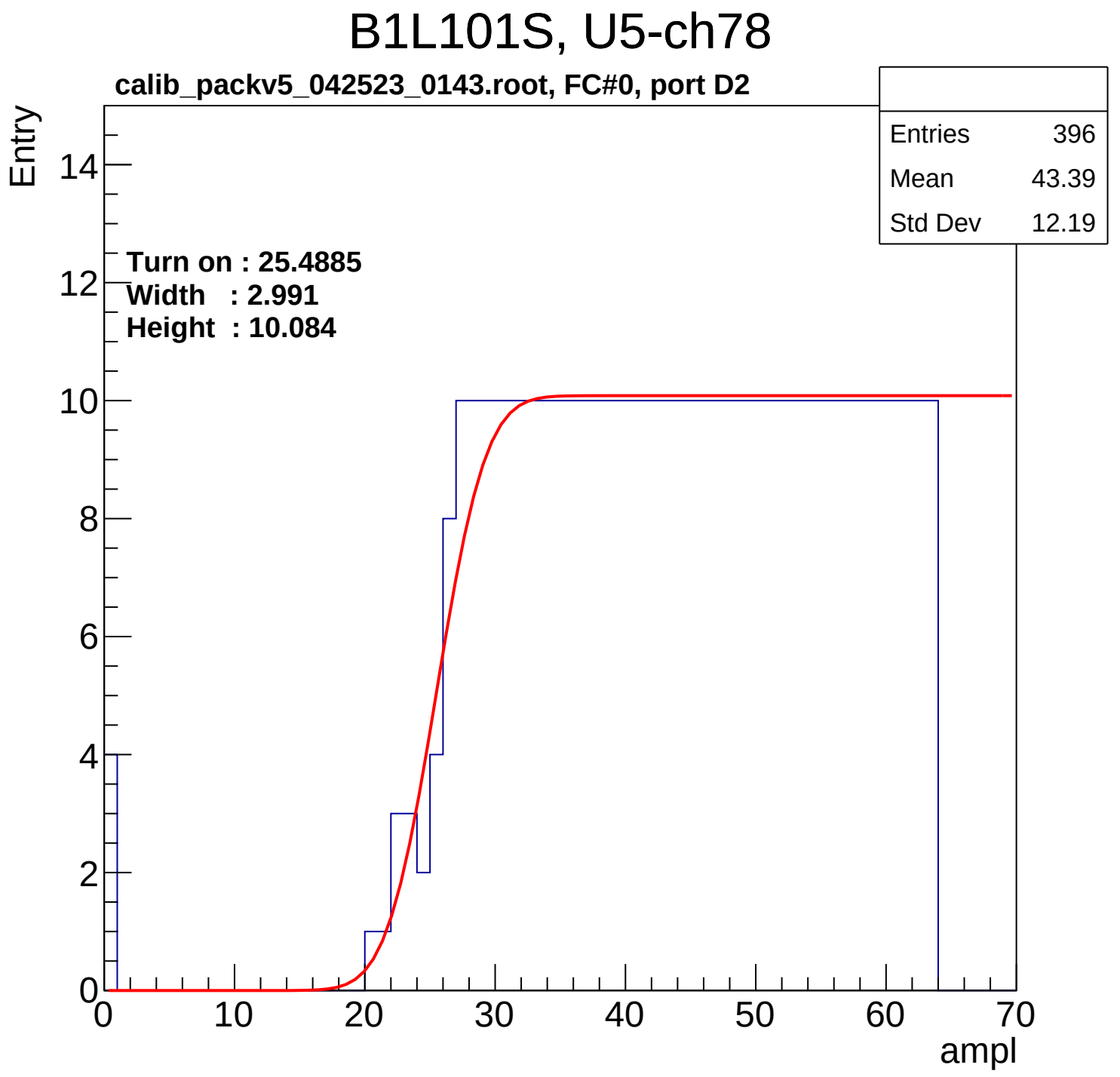

B1L101S, U5-ch73
calib_packv5_042523_0143.root, FC#0, port D2
Entries 363
Mean 44.91
Std Dev 11.55
Turn on : 28.3207
Width : 3.575
Height : 10.004
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

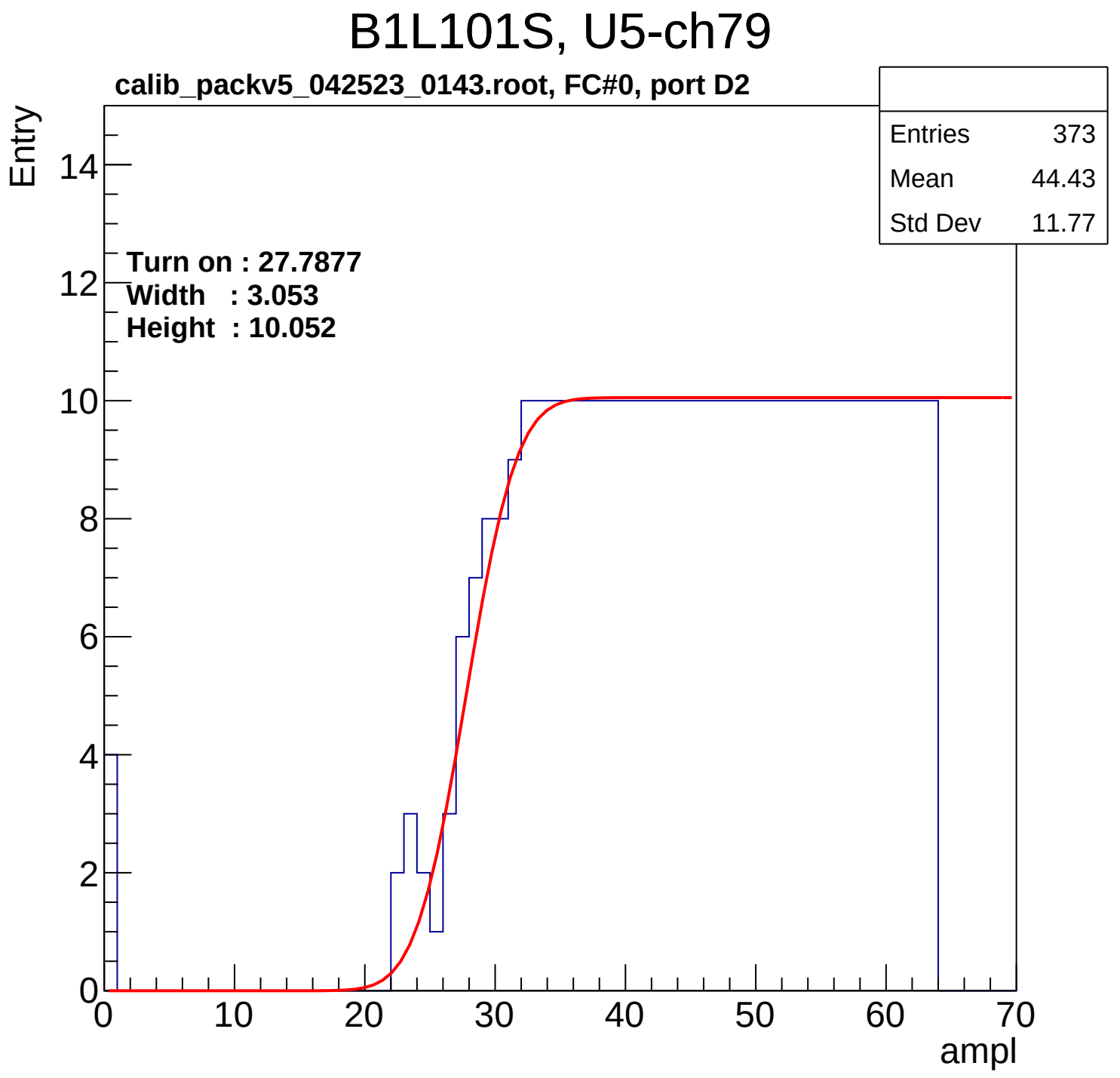

B1L101S, U5-ch74
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.79
Std Dev 11.97
Turn on : 25.9178
Width : 3.930
Height : 10.030
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

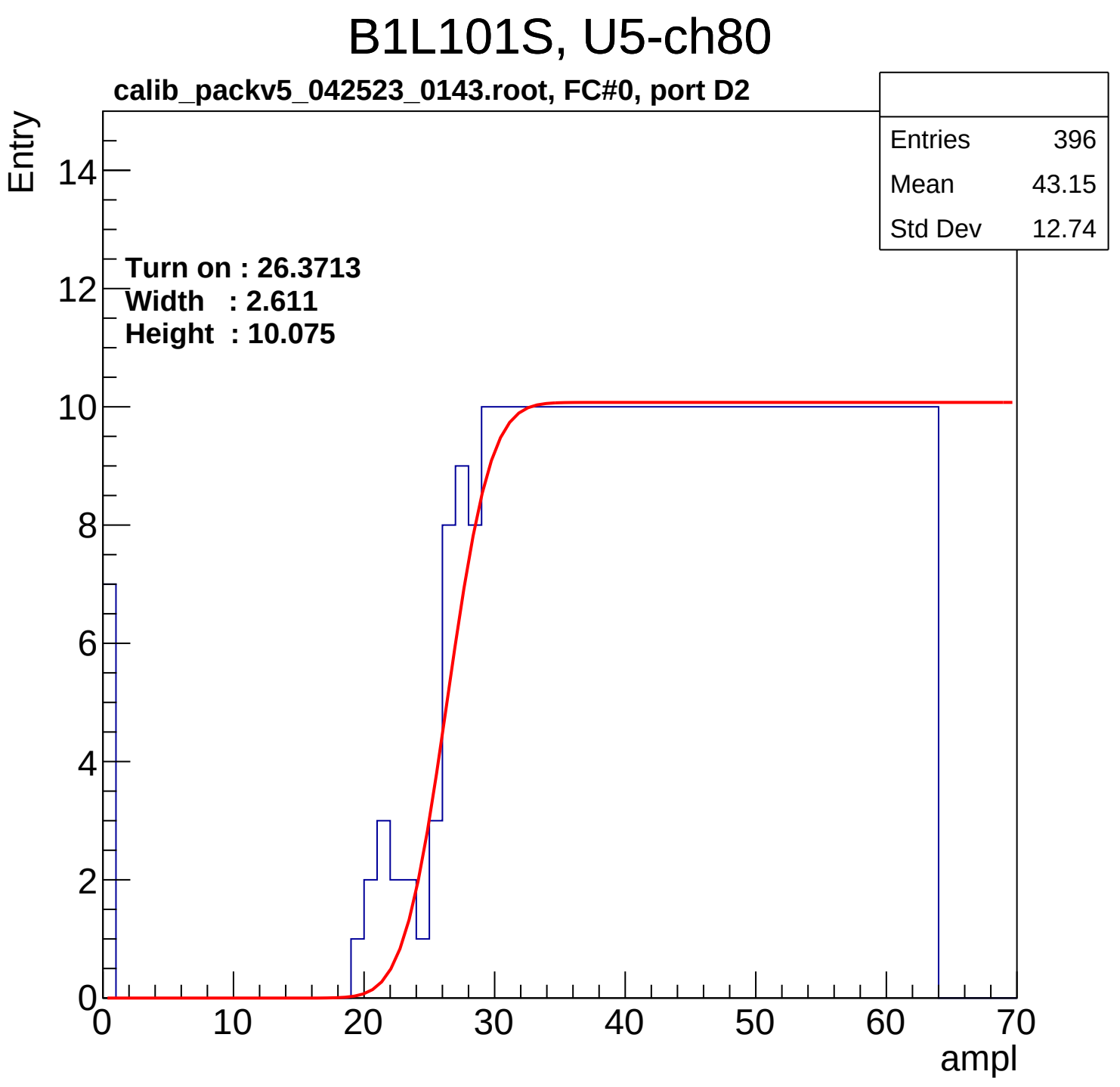

B1L101S, U5-ch75
calib_packv5_042523_0143.root, FC#0, port D2
Entries 394
Mean 43.52
Std Dev 12.02
Turn on : 24.7238
Width : 3.000
Height : 9.975
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

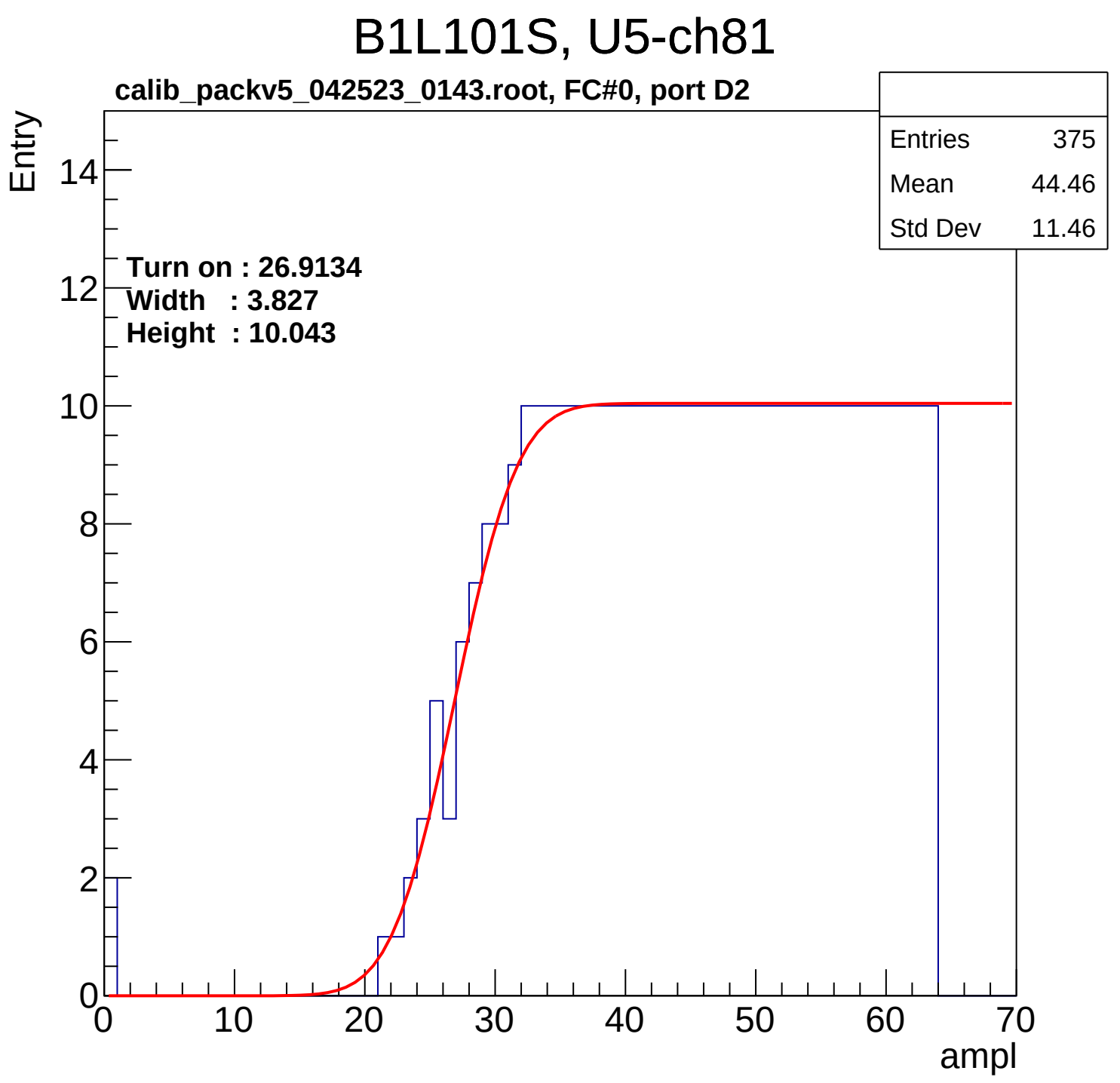

B1L101S, U5-ch76
calib_packv5_042523_0143.root, FC#0, port D2
Entries 386
Mean 43.84
Std Dev 12.09
Turn on : 25.9663
Width : 1.197
Height : 9.988
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

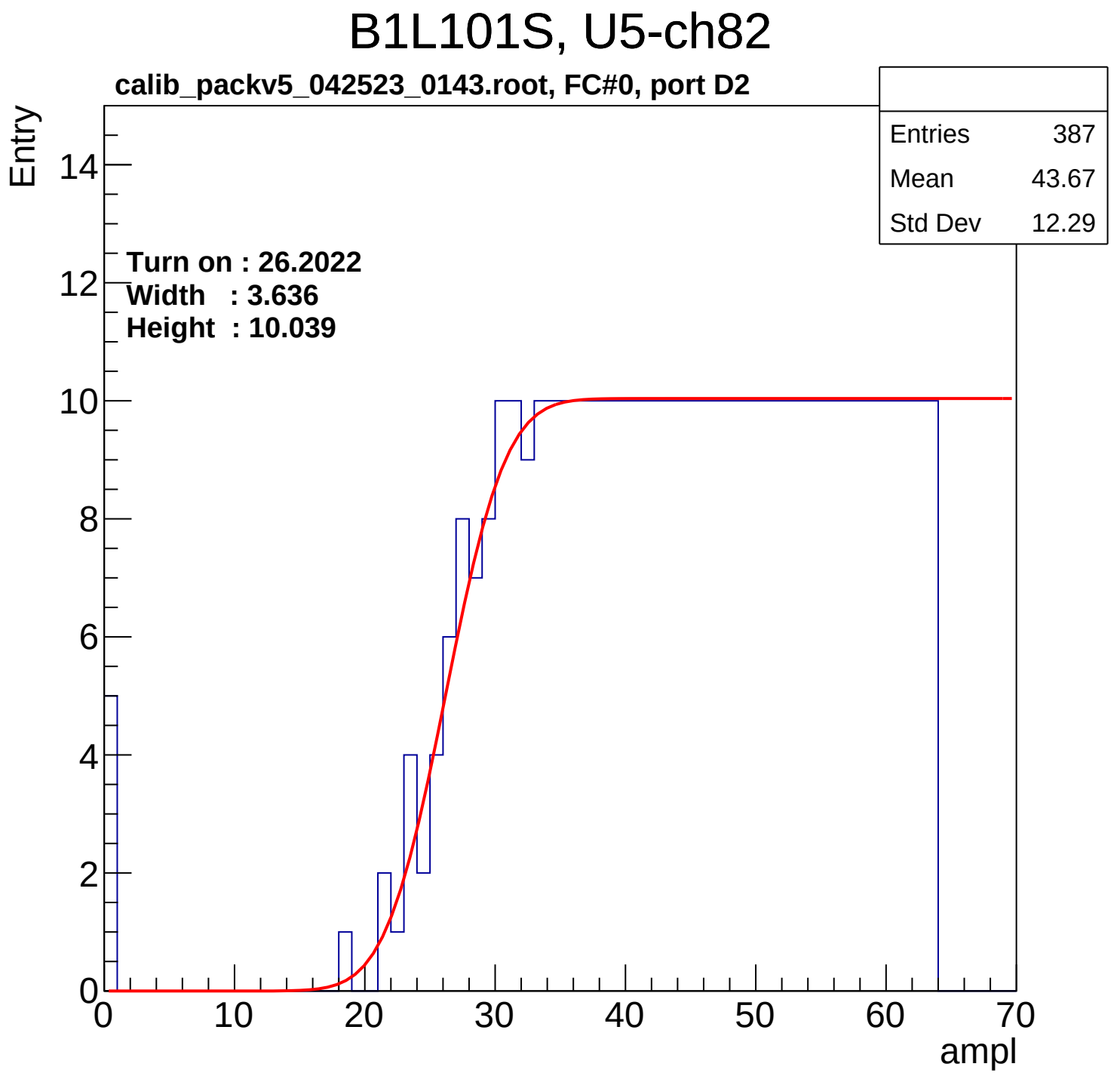

B1L101S, U5-ch77
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 44.08
Std Dev 11.66
Turn on : 26.6103
Width : 3.713
Height : 10.076
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

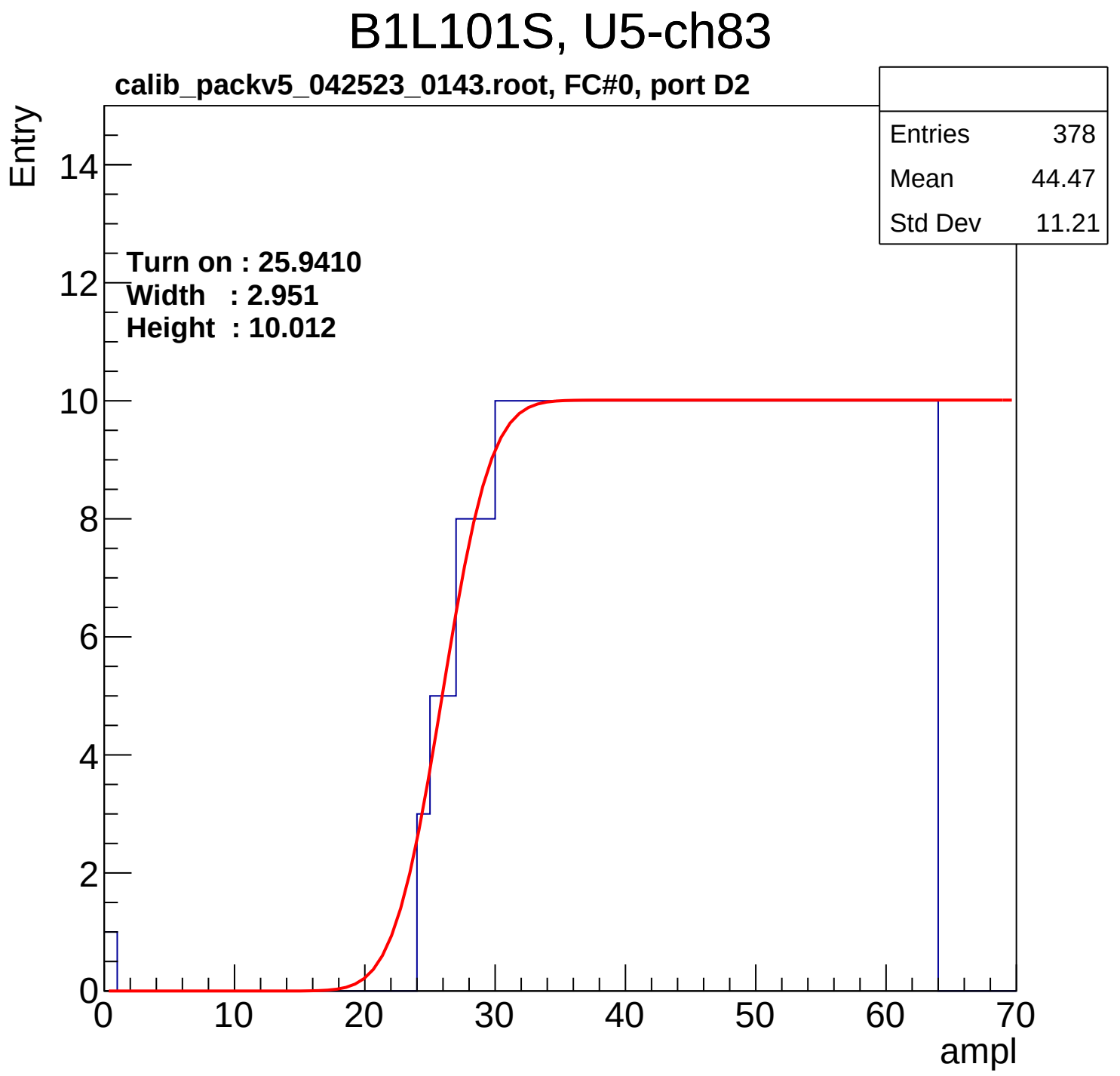

B1L101S, U5-ch78
calib_packv5_042523_0143.root, FC#0, port D2
Entries 396
Mean 43.39
Std Dev 12.19
Turn on : 25.4885
Width : 2.991
Height : 10.084
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

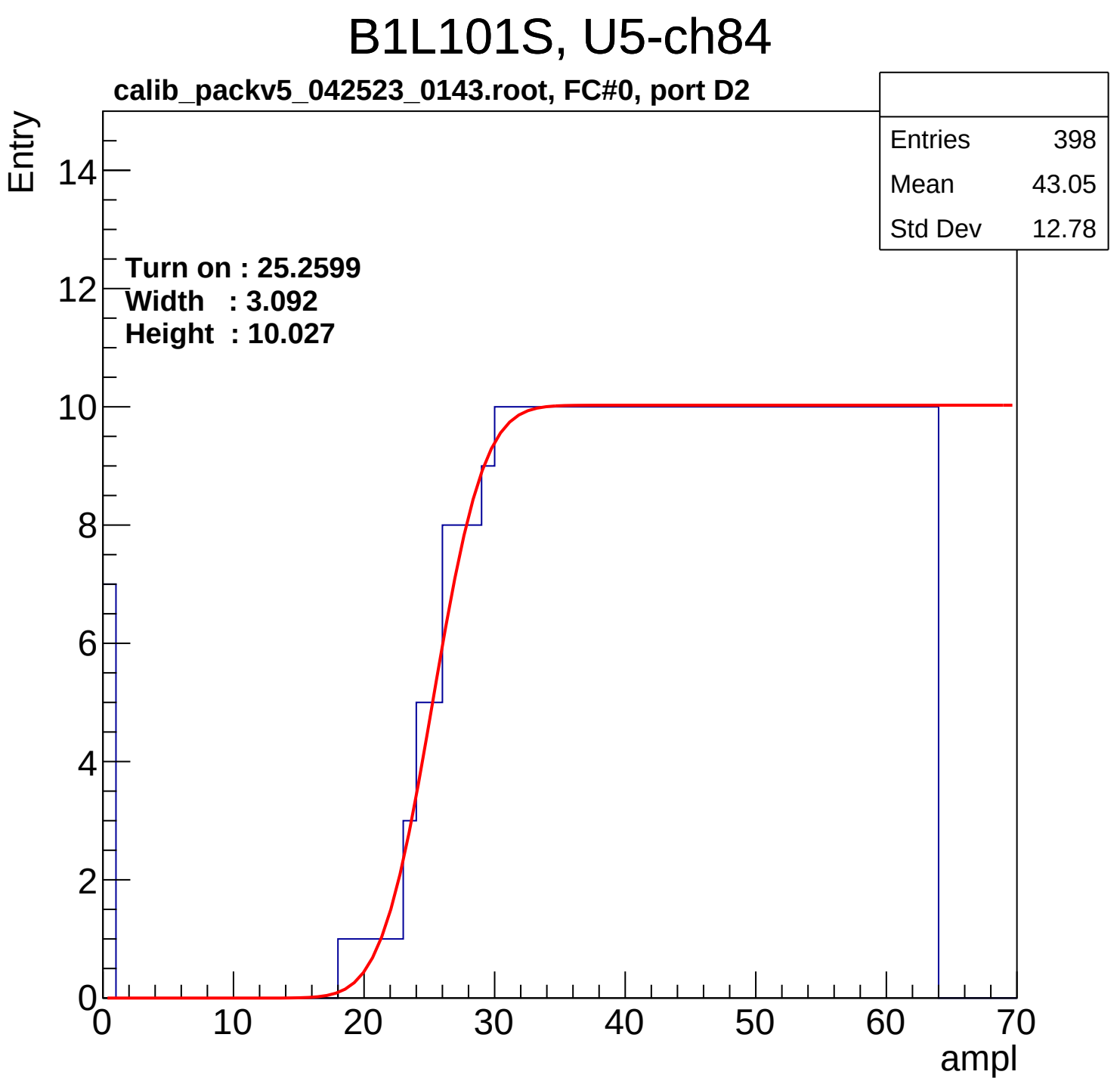

B1L101S, U5-ch79
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.43
Std Dev 11.77
Turn on : 27.7877
Width : 3.053
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

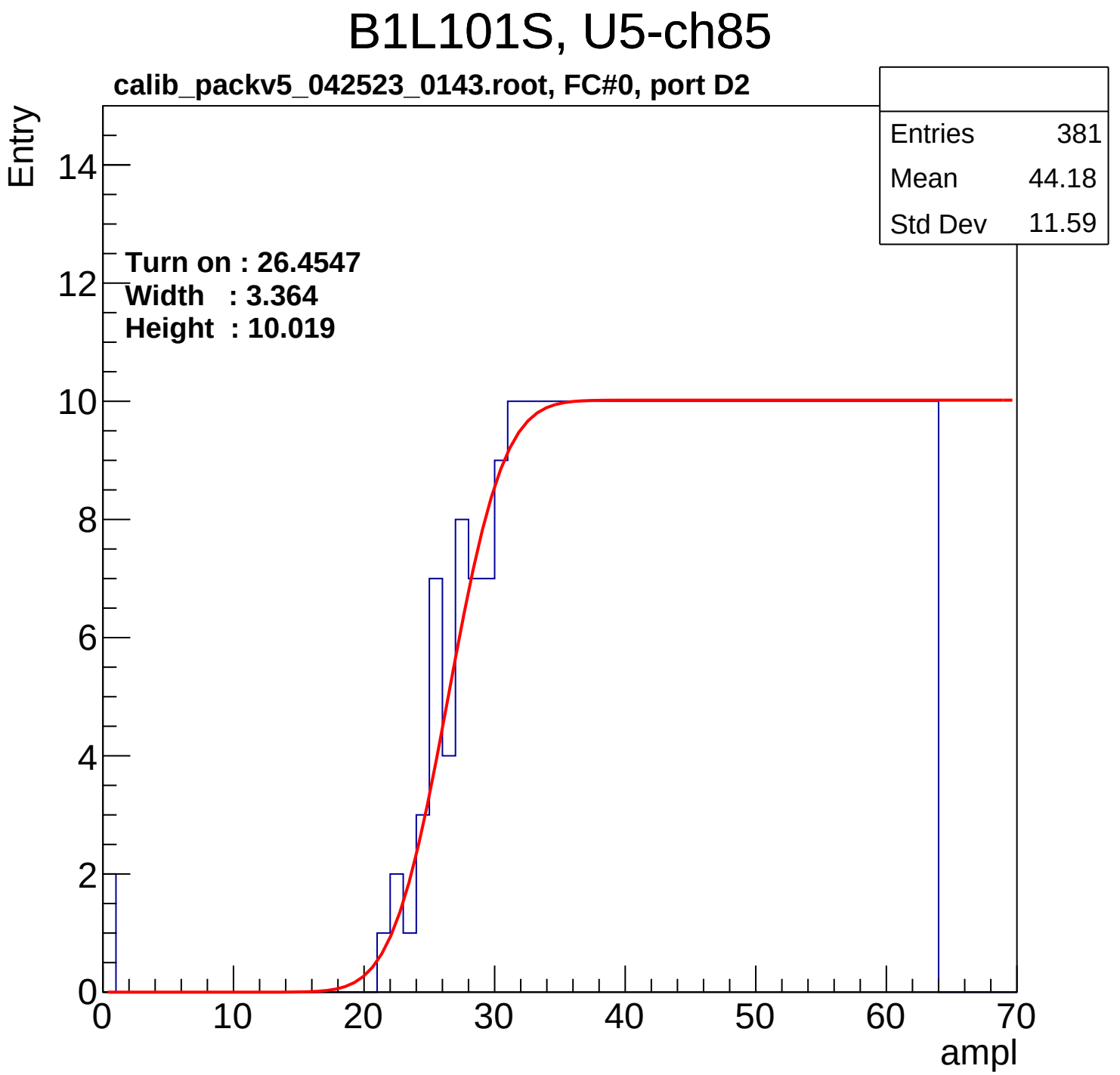

B1L101S, U5-ch80
calib_packv5_042523_0143.root, FC#0, port D2
Entries 396
Mean 43.15
Std Dev 12.74
Turn on : 26.3713
Width : 2.611
Height : 10.075
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

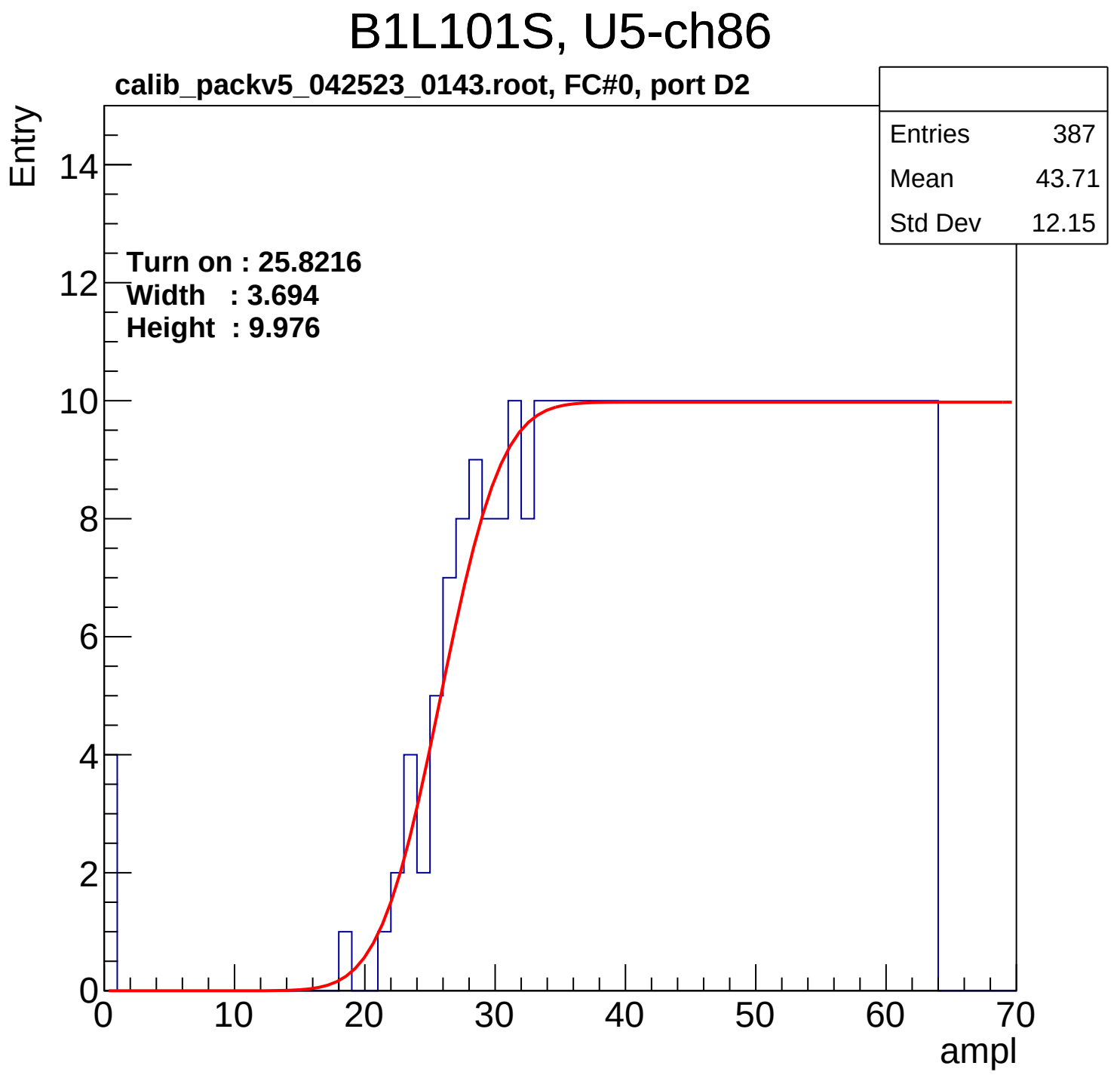

B1L101S, U5-ch81
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.46
Std Dev 11.46
Turn on : 26.9134
Width : 3.827
Height : 10.043
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

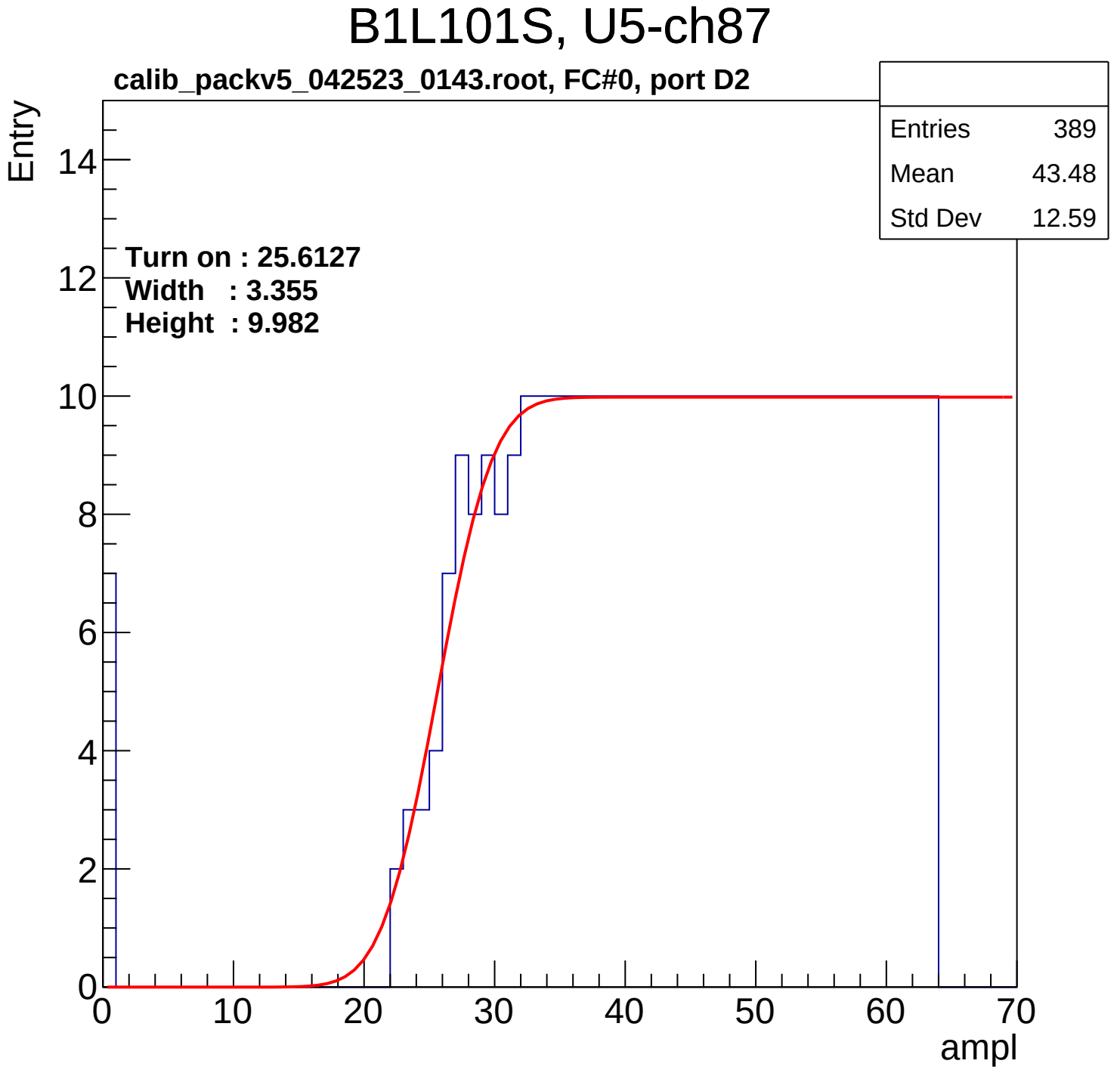

B1L101S, U5-ch82
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.67
Std Dev 12.29
Turn on : 26.2022
Width : 3.636
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

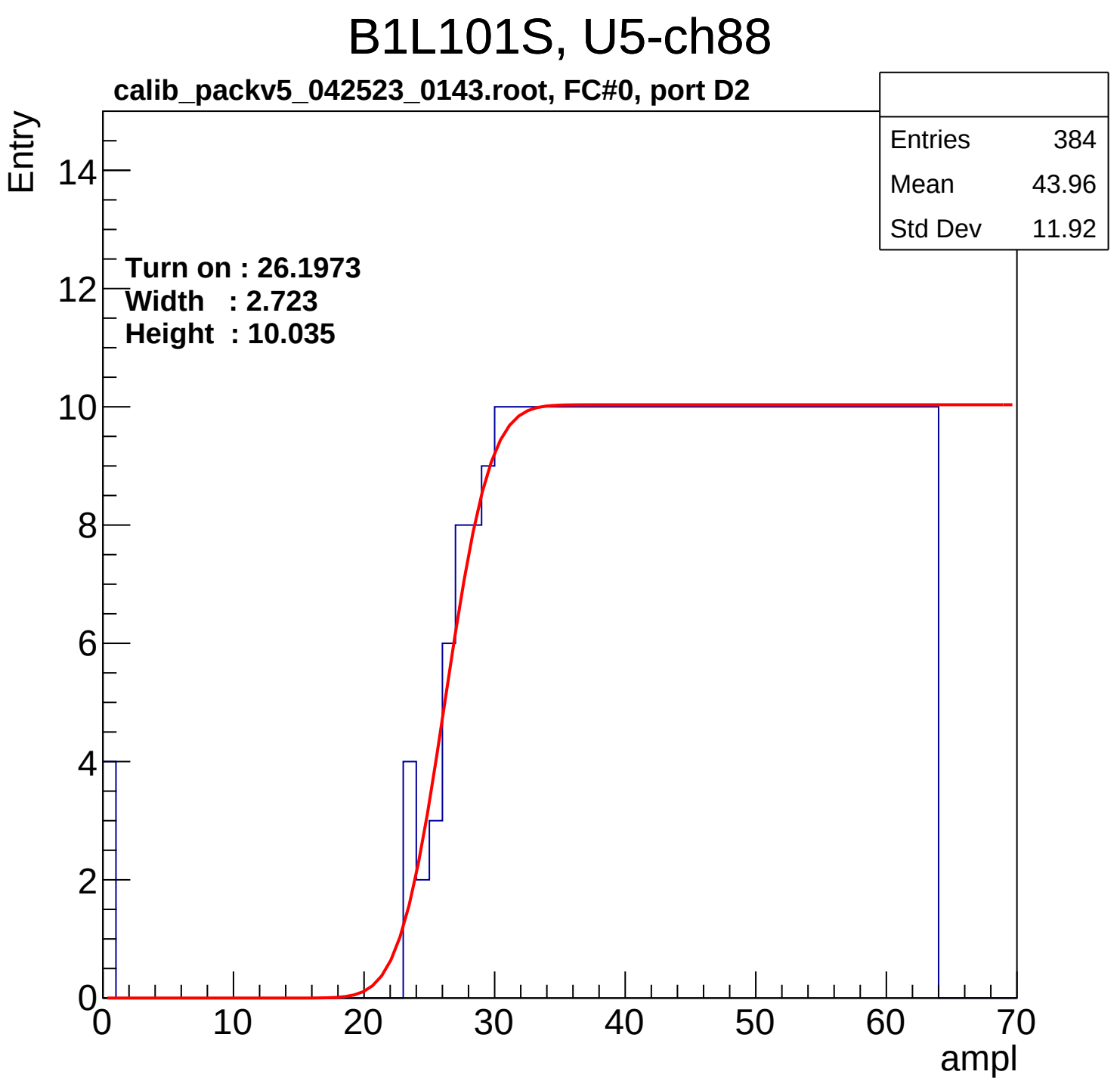

B1L101S, U5-ch83
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.47
Std Dev 11.21
Turn on : 25.9410
Width : 2.951
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

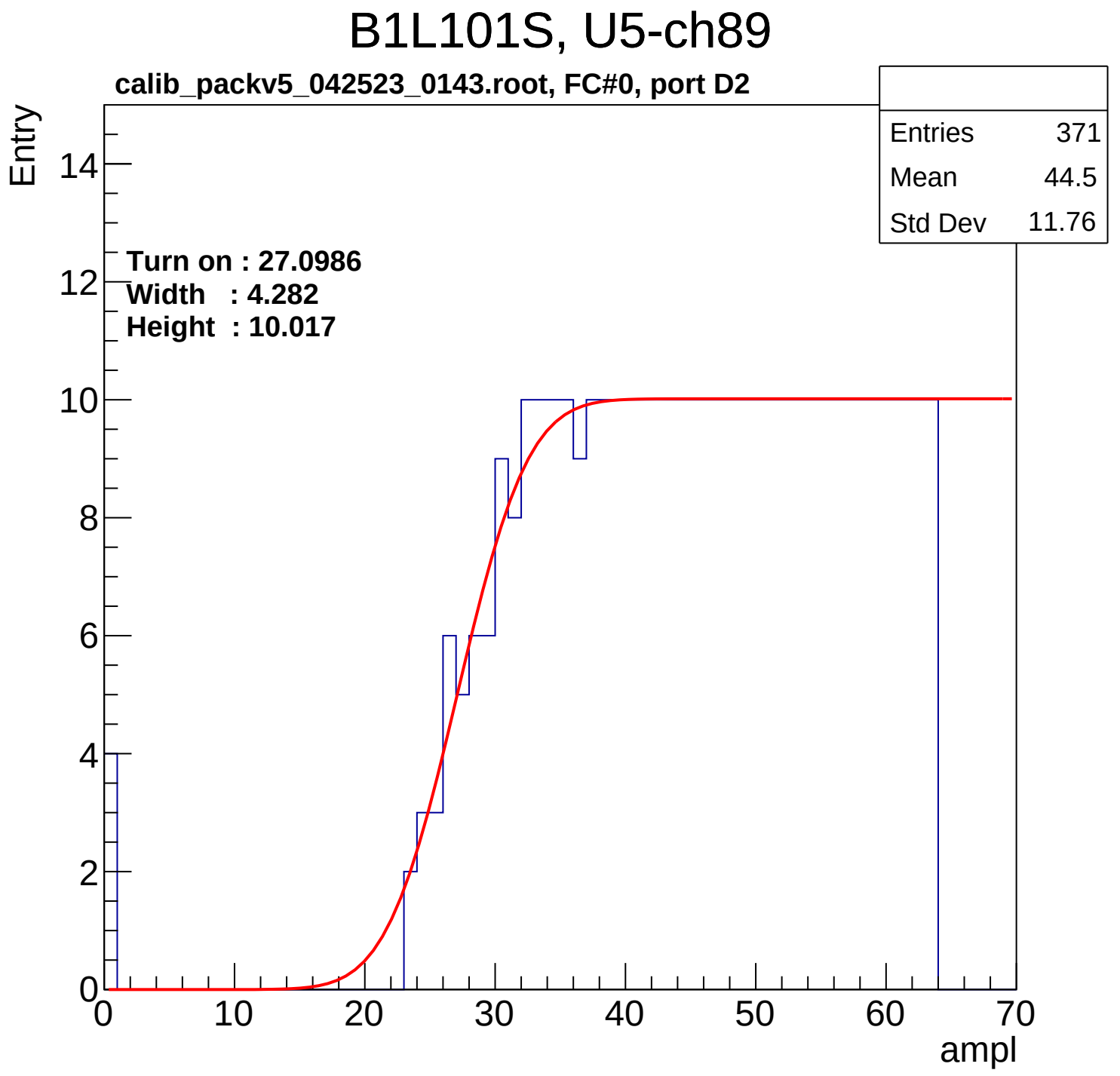

B1L101S, U5-ch84
calib_packv5_042523_0143.root, FC#0, port D2
Entries 398
Mean 43.05
Std Dev 12.78
Turn on : 25.2599
Width : 3.092
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

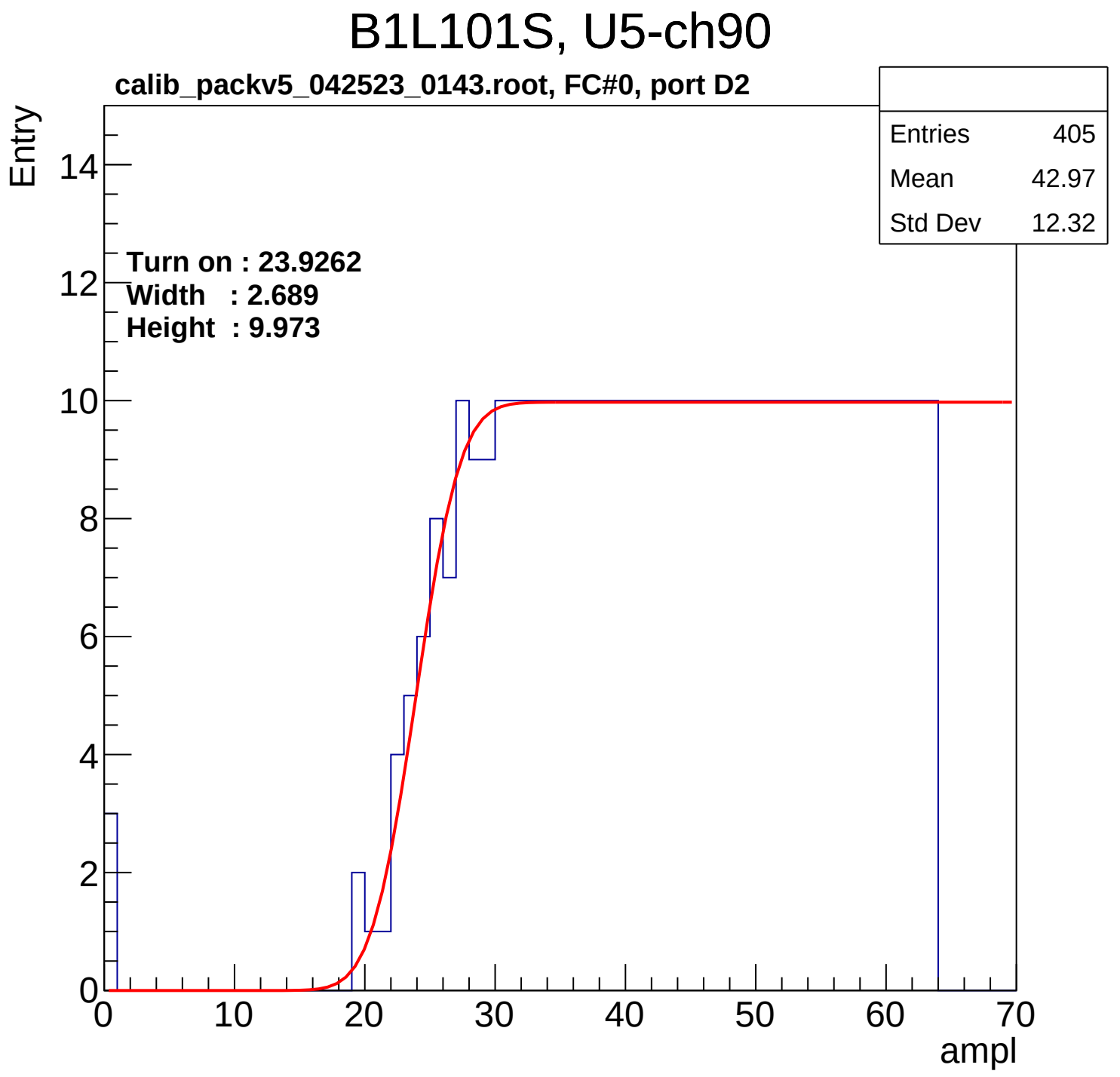

B1L101S, U5-ch85
calib_packv5_042523_0143.root, FC#0, port D2
Entries 381
Mean 44.18
Std Dev 11.59
Turn on : 26.4547
Width : 3.364
Height : 10.019
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

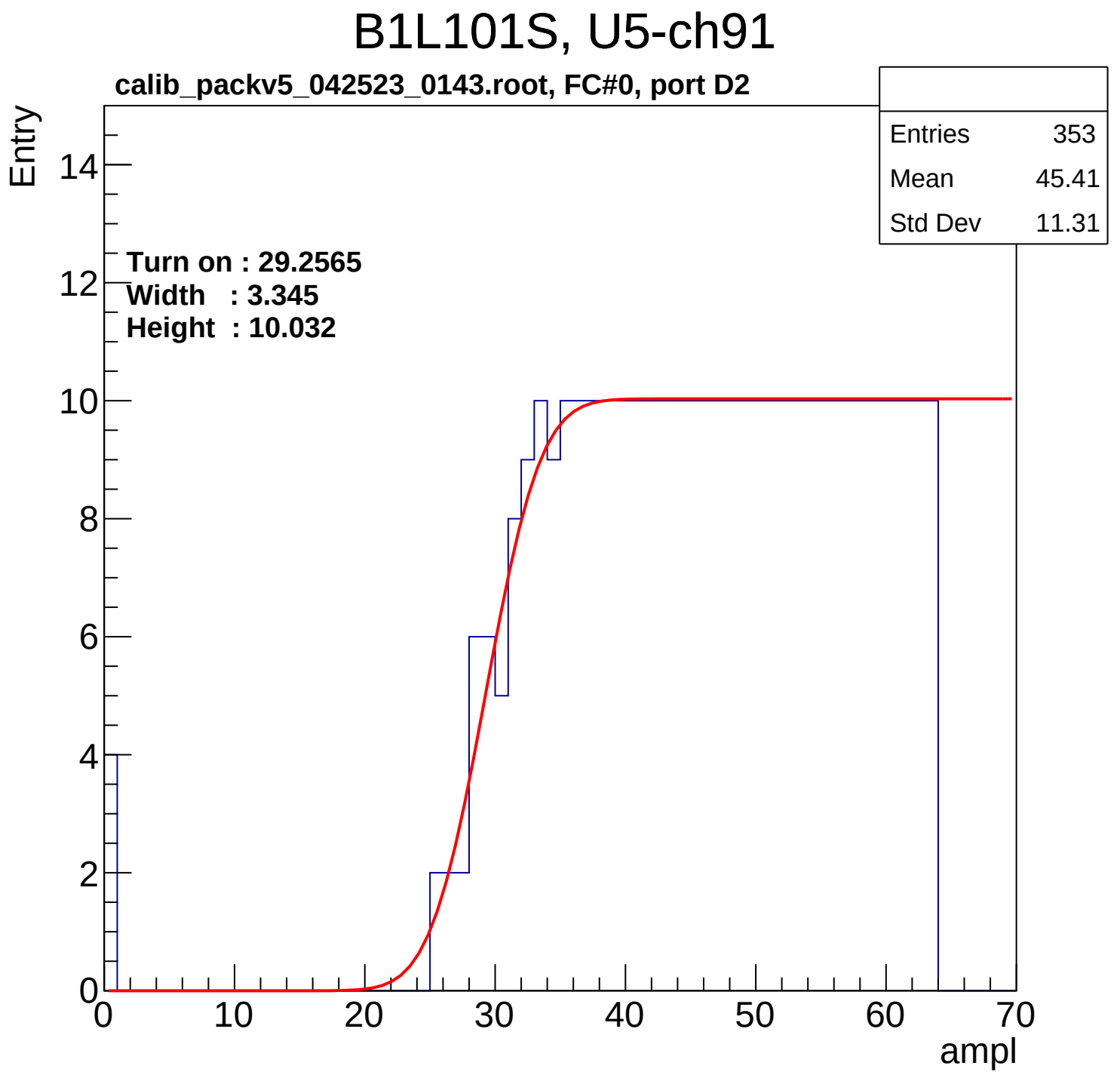

B1L101S, U5-ch86
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.71
Std Dev 12.15
Turn on : 25.8216
Width : 3.694
Height : 9.976
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

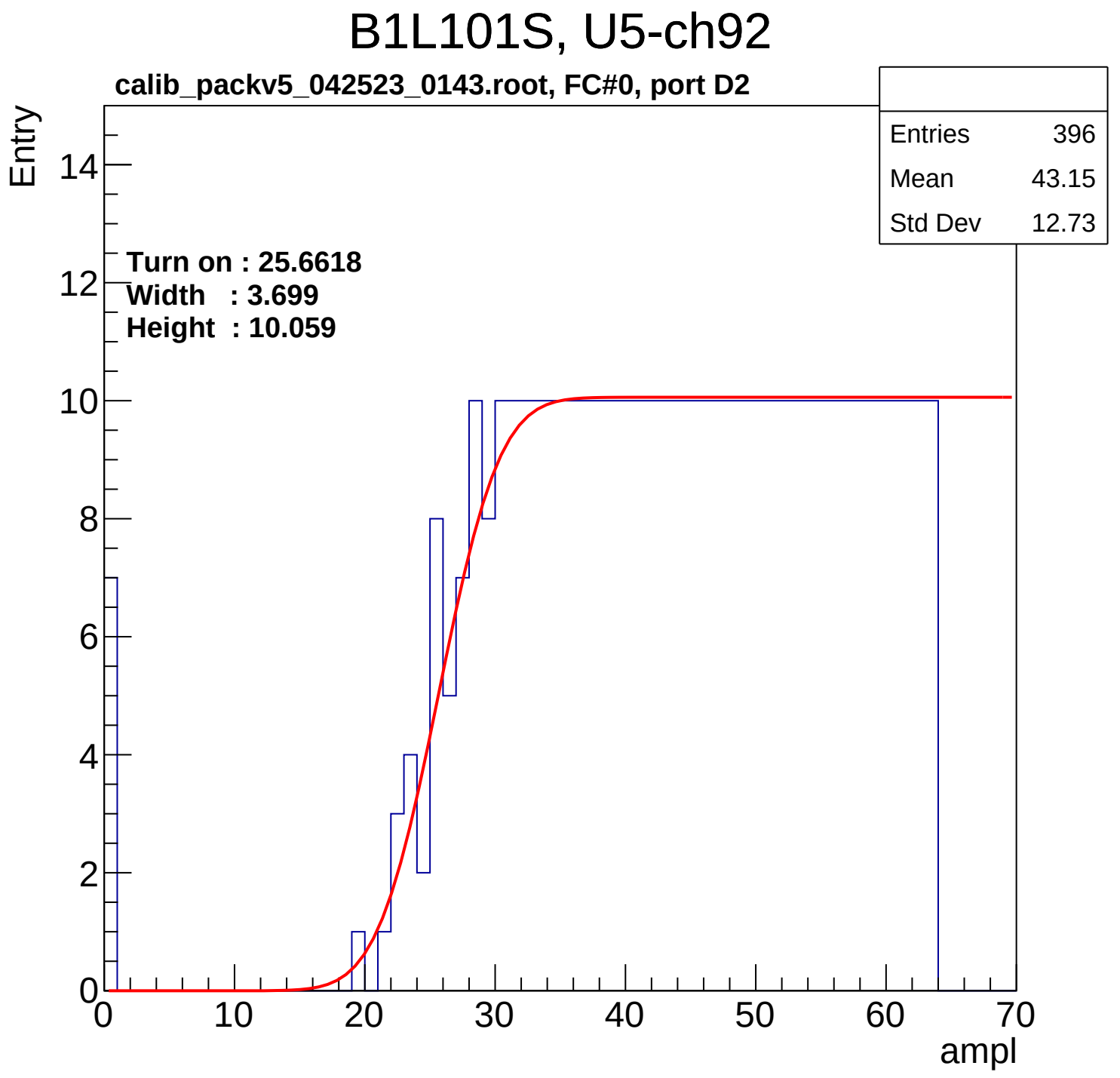

B1L101S, U5-ch87
calib_packv5_042523_0143.root, FC#0, port D2
Entries 389
Mean 43.48
Std Dev 12.59
Turn on : 25.6127
Width : 3.355
Height : 9.982
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

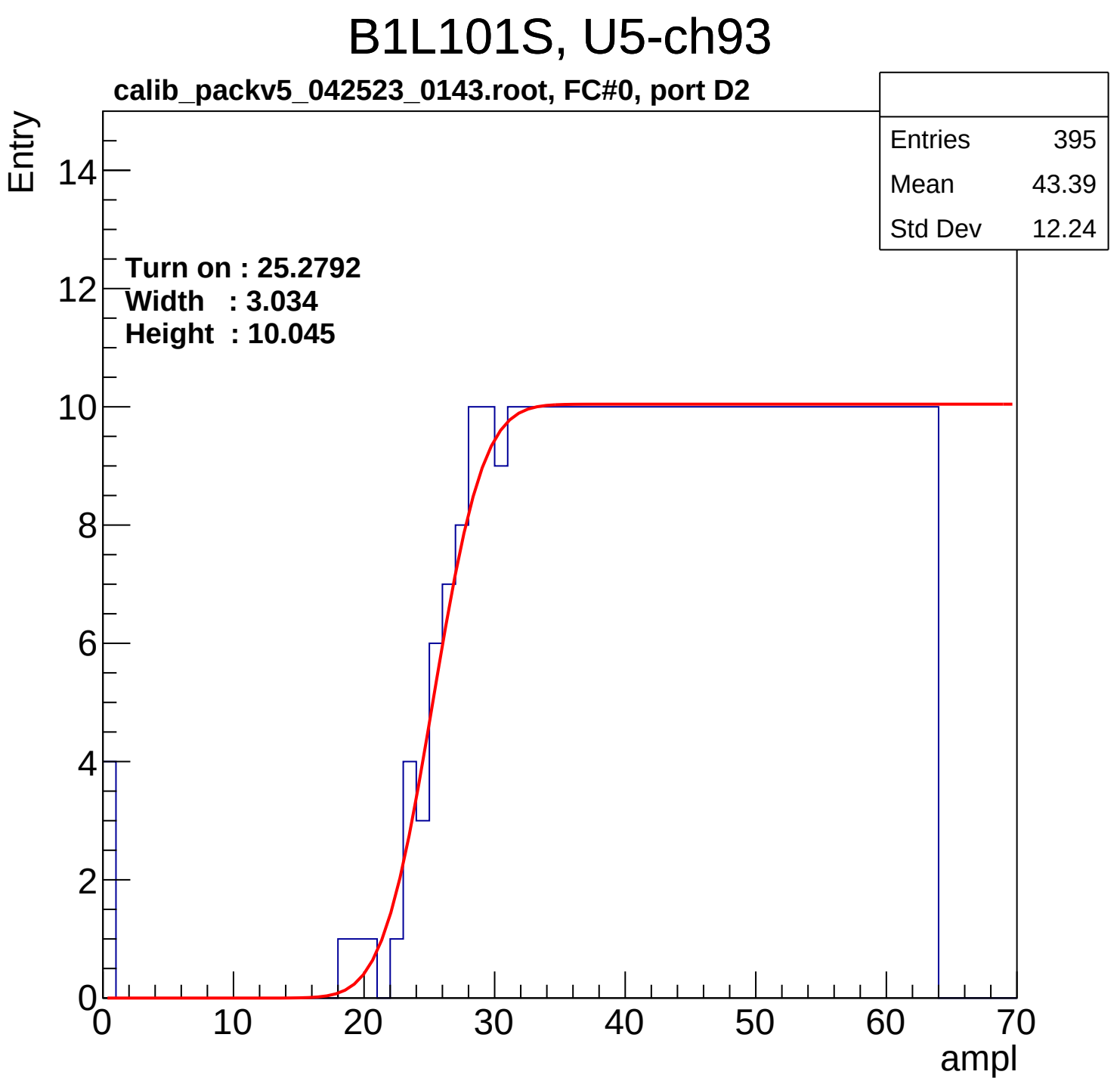

B1L101S, U5-ch88
calib_packv5_042523_0143.root, FC#0, port D2
Entries 384
Mean 43.96
Std Dev 11.92
Turn on : 26.1973
Width : 2.723
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

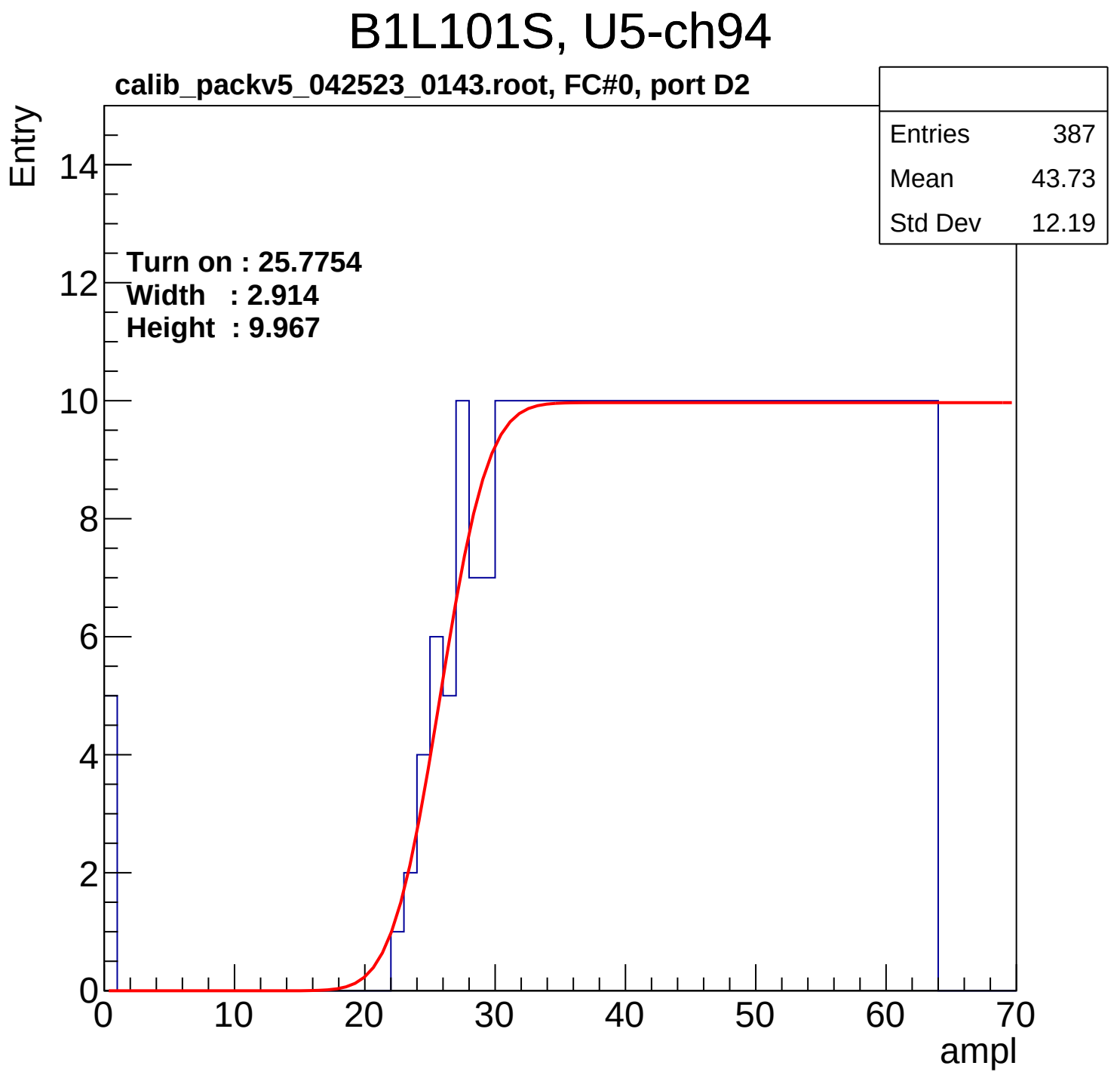

B1L101S, U5-ch89
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.5
Std Dev 11.76
Turn on : 27.0986
Width : 4.282
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

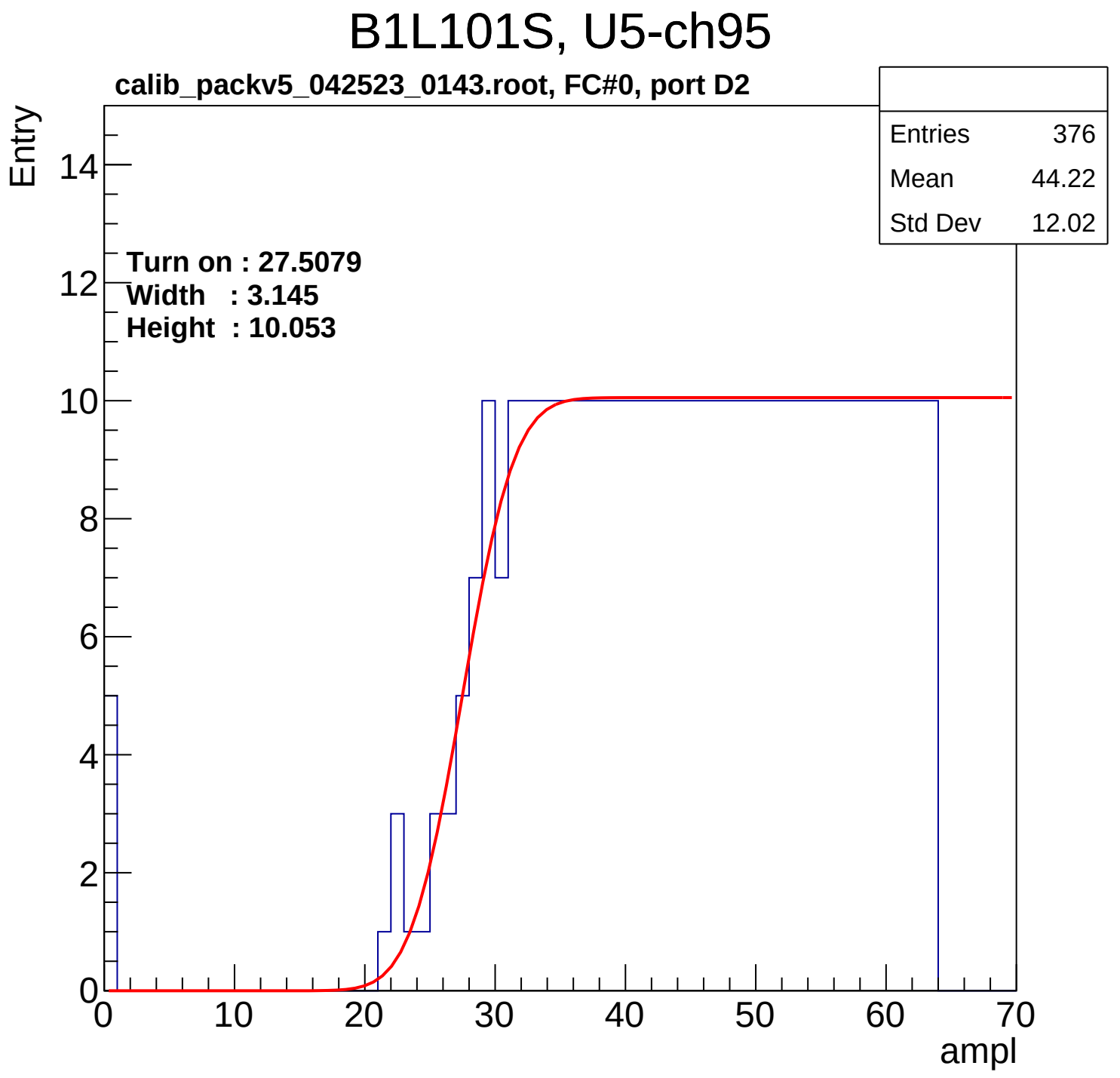

B1L101S, U5-ch90
calib_packv5_042523_0143.root, FC#0, port D2
Entries 405
Mean 42.97
Std Dev 12.32
Turn on : 23.9262
Width : 2.689
Height : 9.973
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

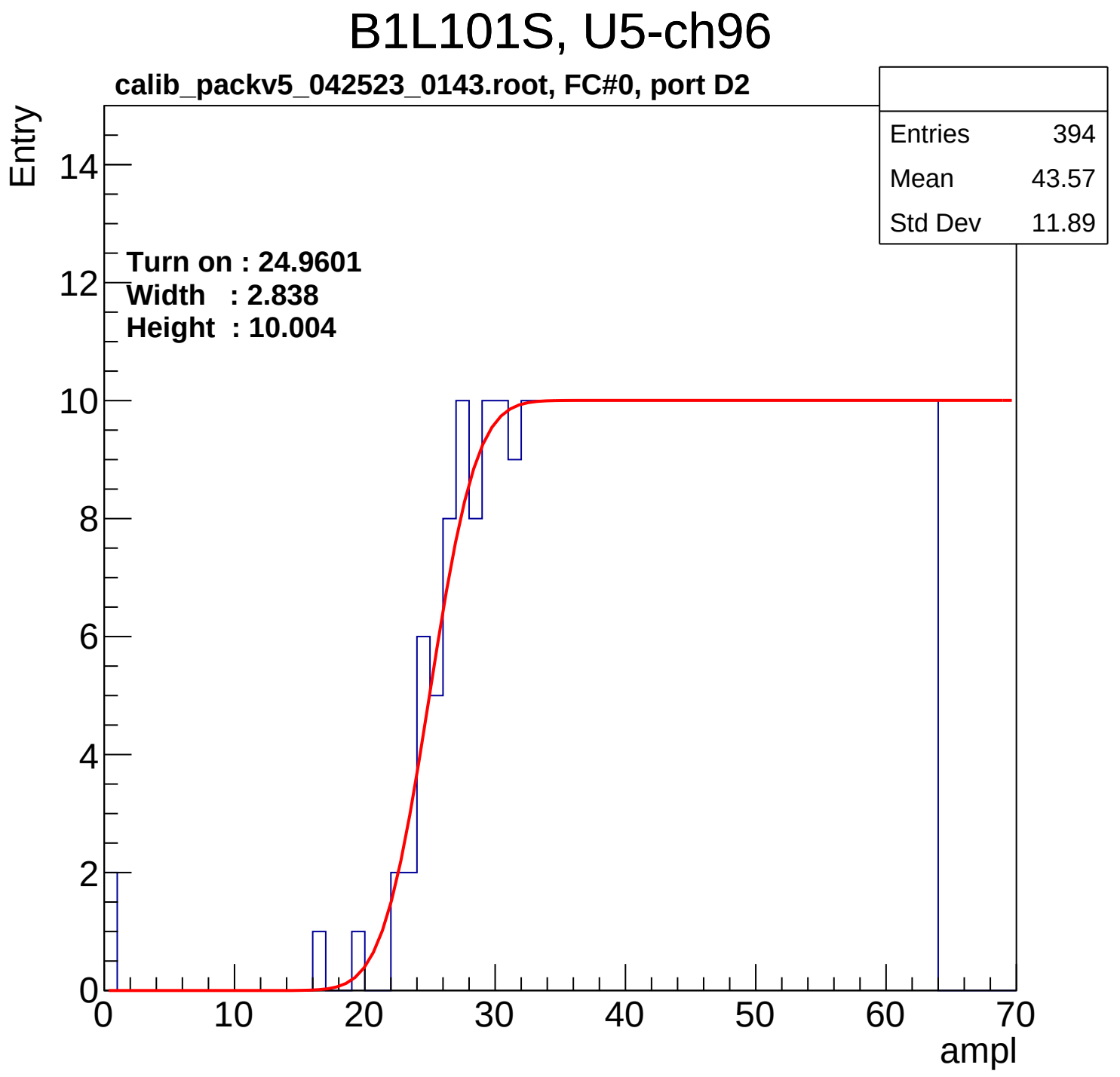

B1L101S, U5-ch91
calib_packv5_042523_0143.root, FC#0, port D2
Entries 353
Mean 45.41
Std Dev 11.31
Turn on : 29.2565
Width : 3.345
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

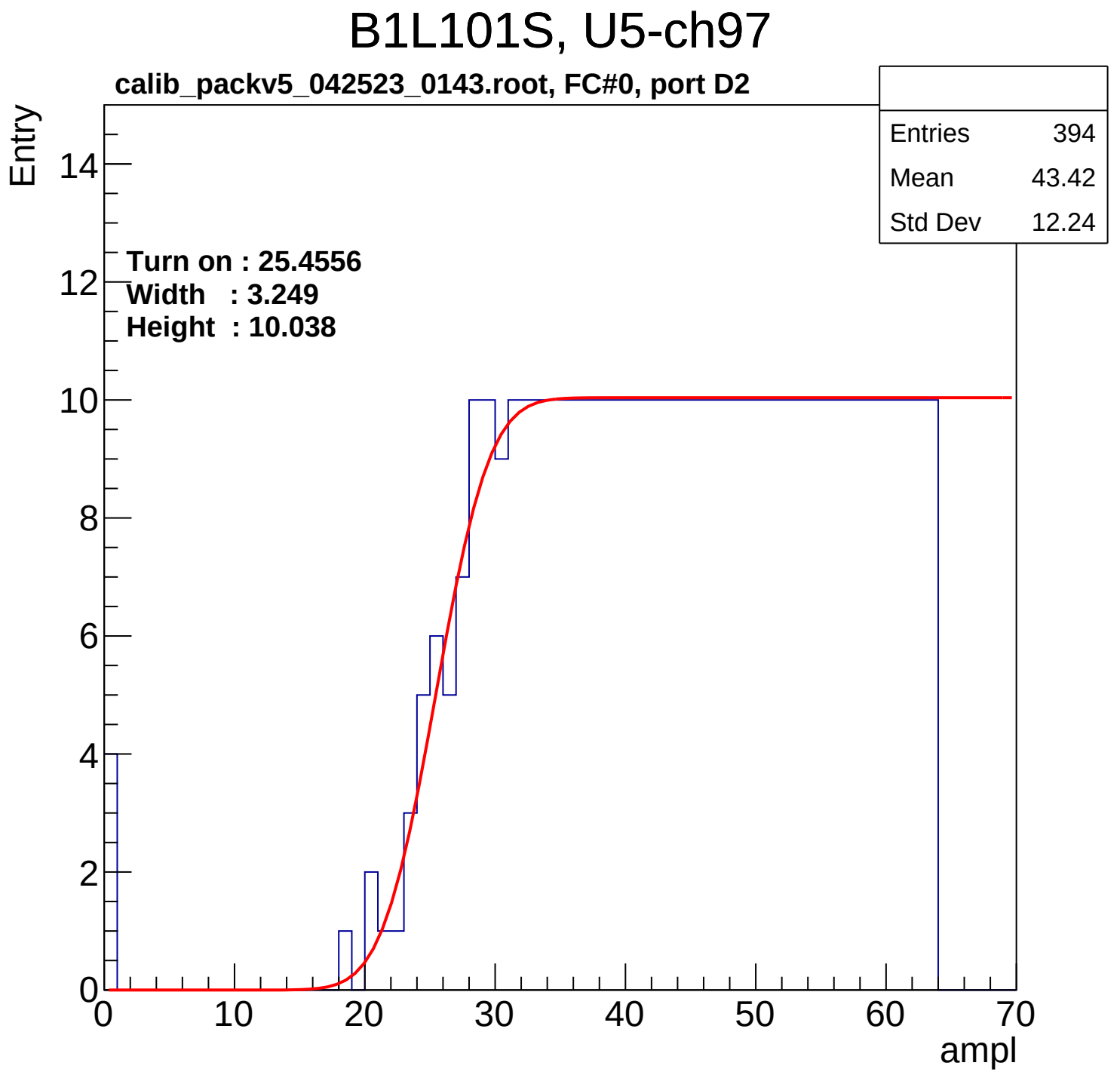

B1L101S, U5-ch92
calib_packv5_042523_0143.root, FC#0, port D2
Entries 396
Mean 43.15
Std Dev 12.73
Turn on : 25.6618
Width : 3.699
Height : 10.059
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

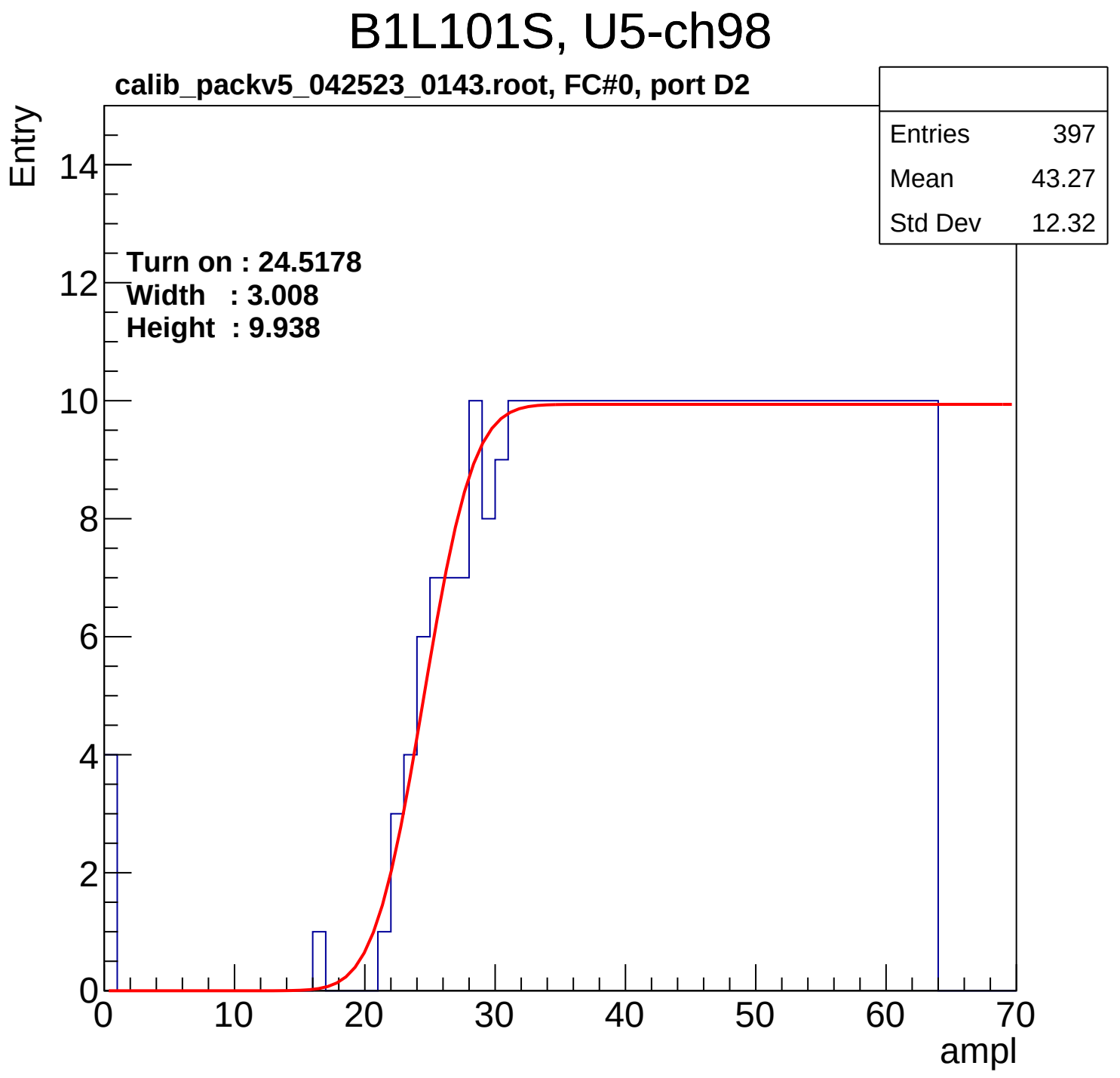

B1L101S, U5-ch93
calib_packv5_042523_0143.root, FC#0, port D2
Entries 395
Mean 43.39
Std Dev 12.24
Turn on : 25.2792
Width : 3.034
Height : 10.045
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

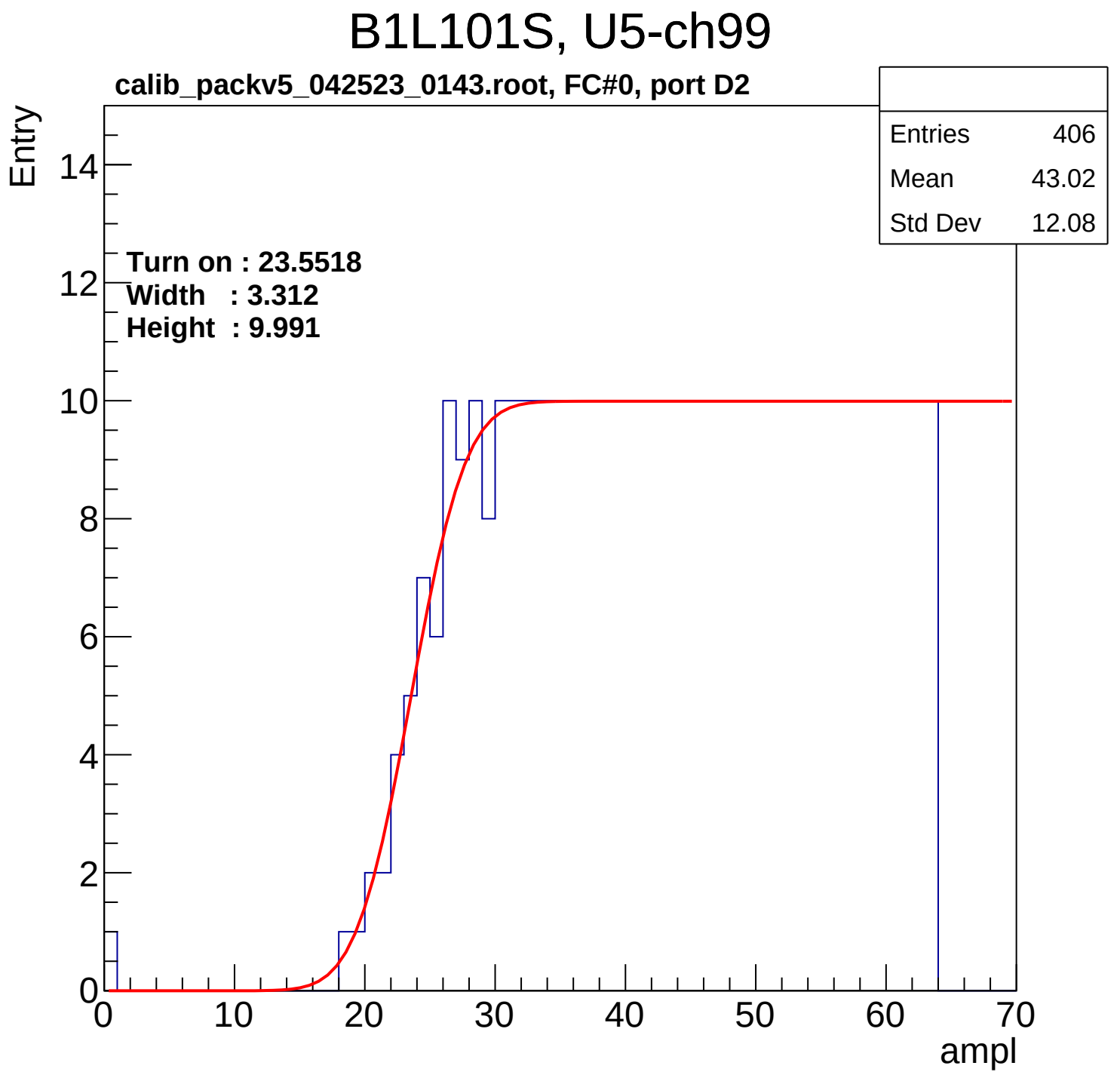

B1L101S, U5-ch94
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.73
Std Dev 12.19
Turn on : 25.7754
Width : 2.914
Height : 9.967
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

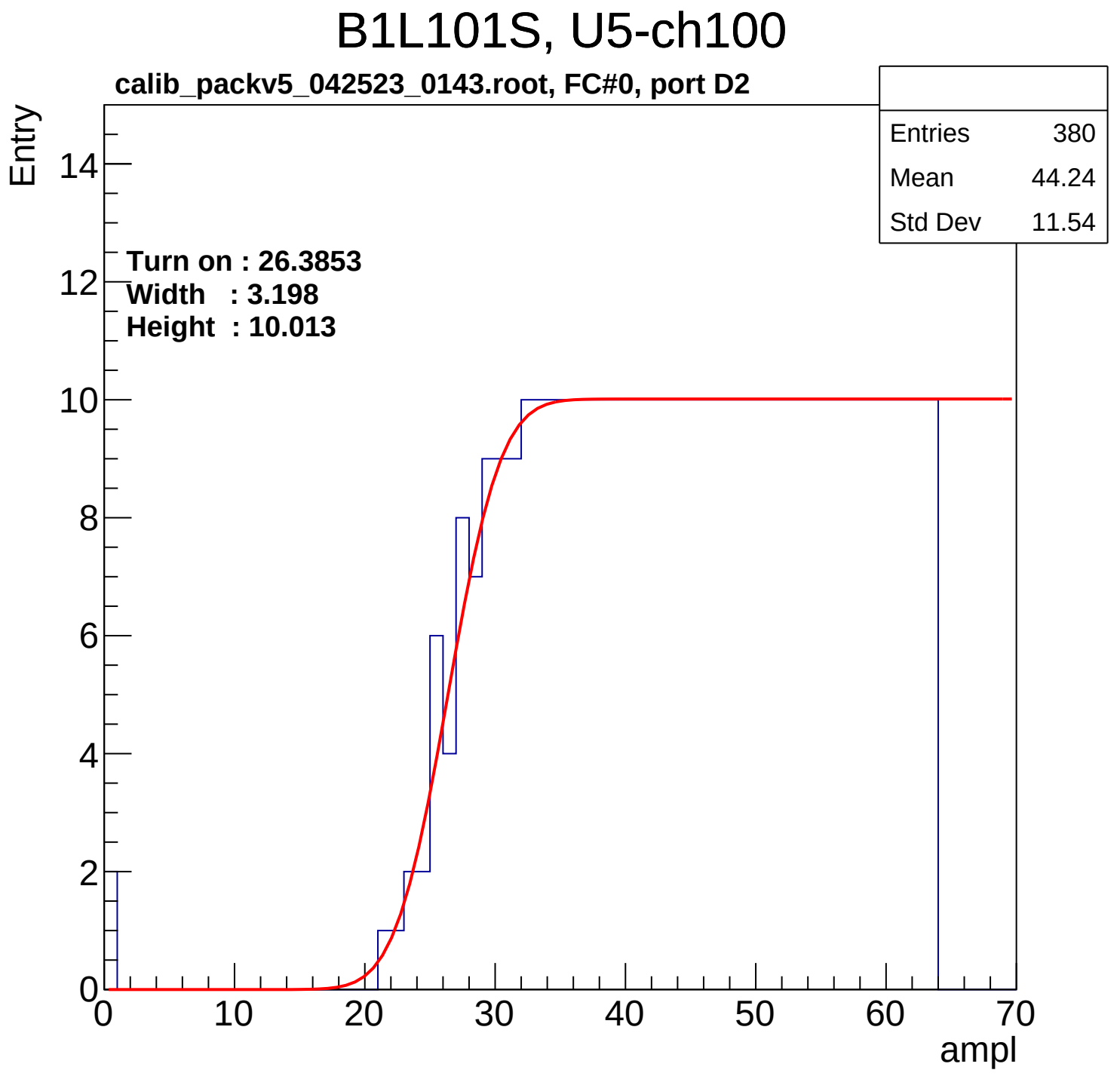

B1L101S, U5-ch95
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.22
Std Dev 12.02
Turn on : 27.5079
Width : 3.145
Height : 10.053
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

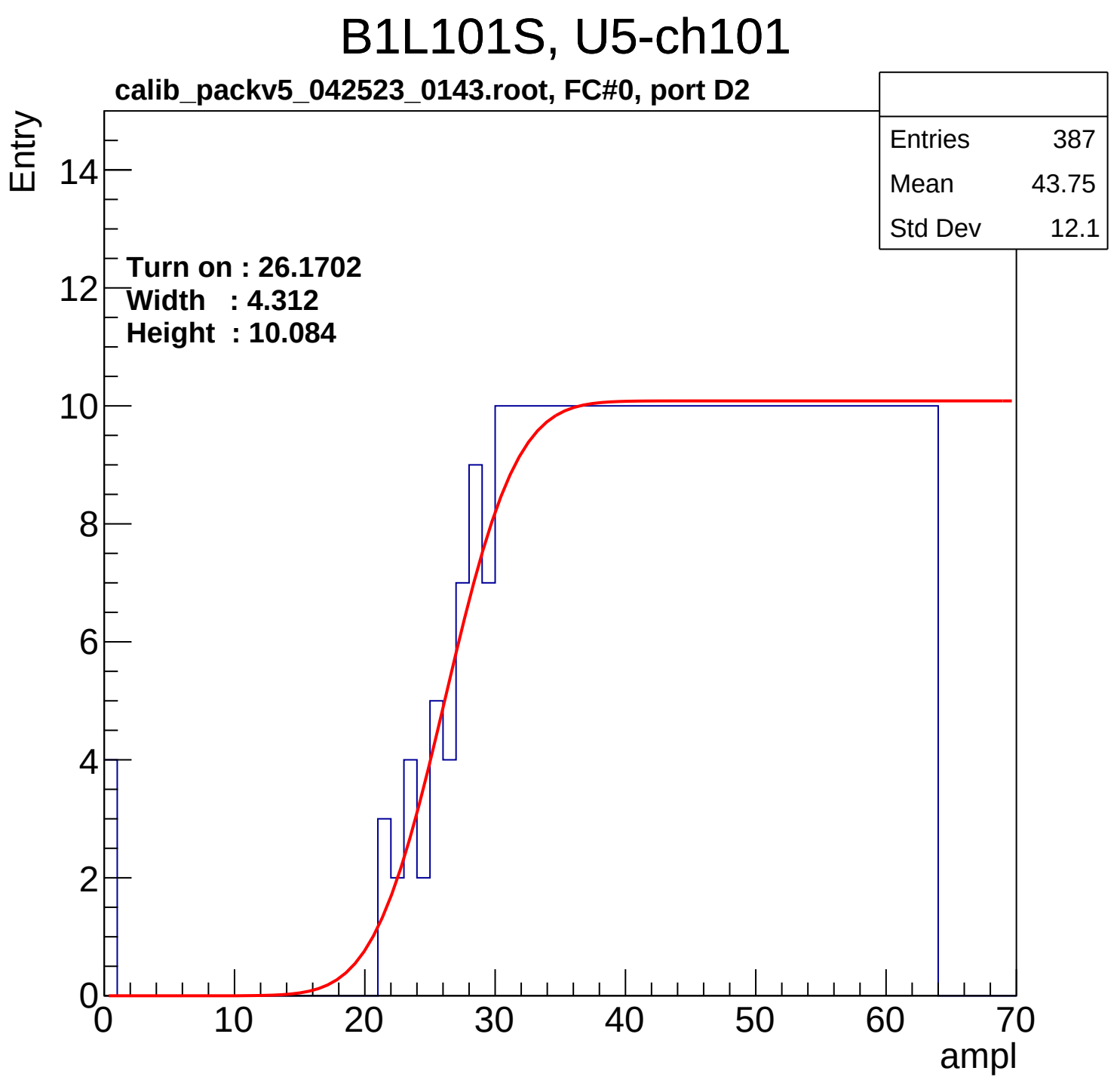

B1L101S, U5-ch96
calib_packv5_042523_0143.root, FC#0, port D2
Entries 394
Mean 43.57
Std Dev 11.89
Turn on : 24.9601
Width : 2.838
Height : 10.004
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

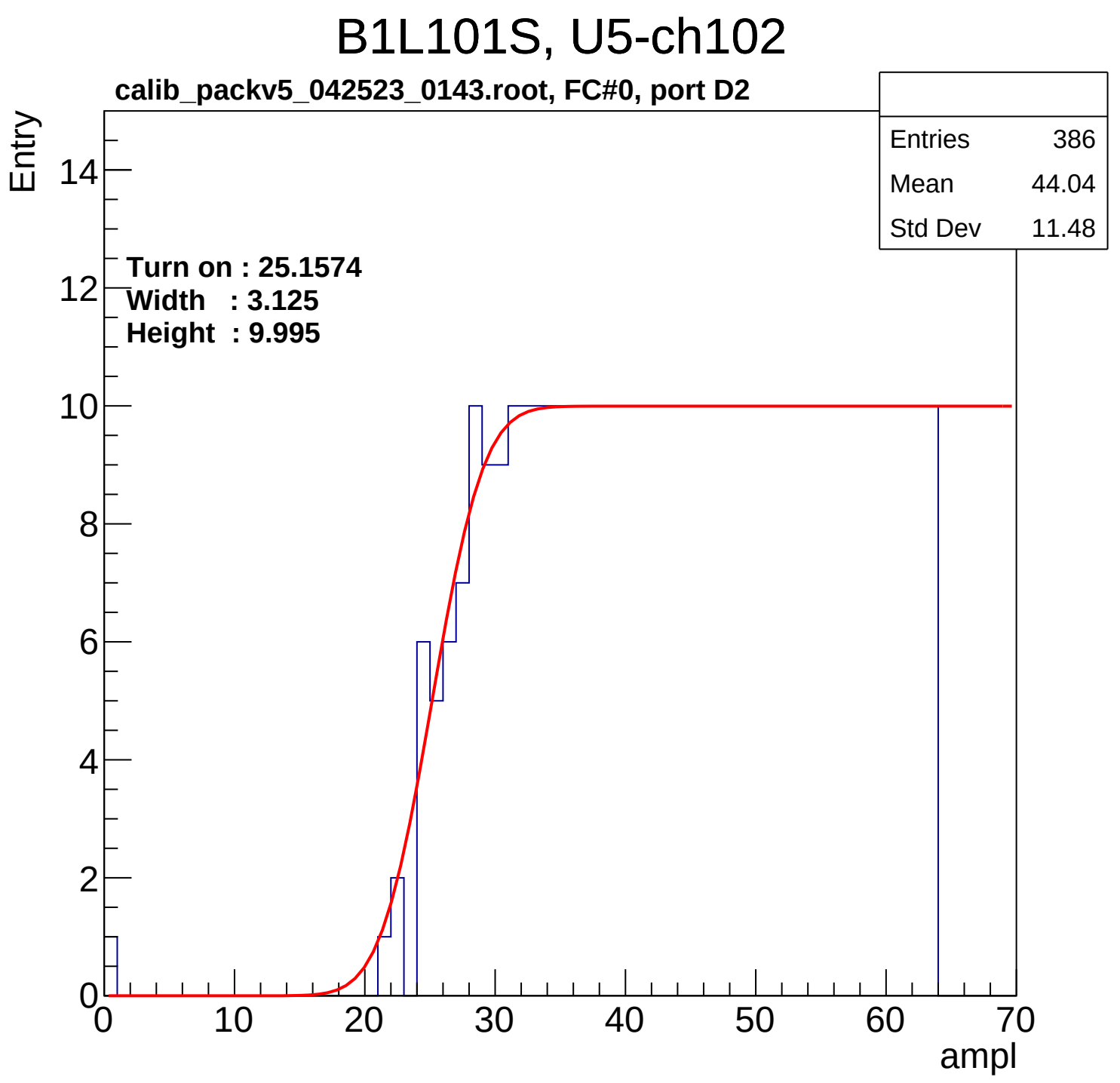

B1L101S, U5-ch97
calib_packv5_042523_0143.root, FC#0, port D2
Entries 394
Mean 43.42
Std Dev 12.24
Turn on : 25.4556
Width : 3.249
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

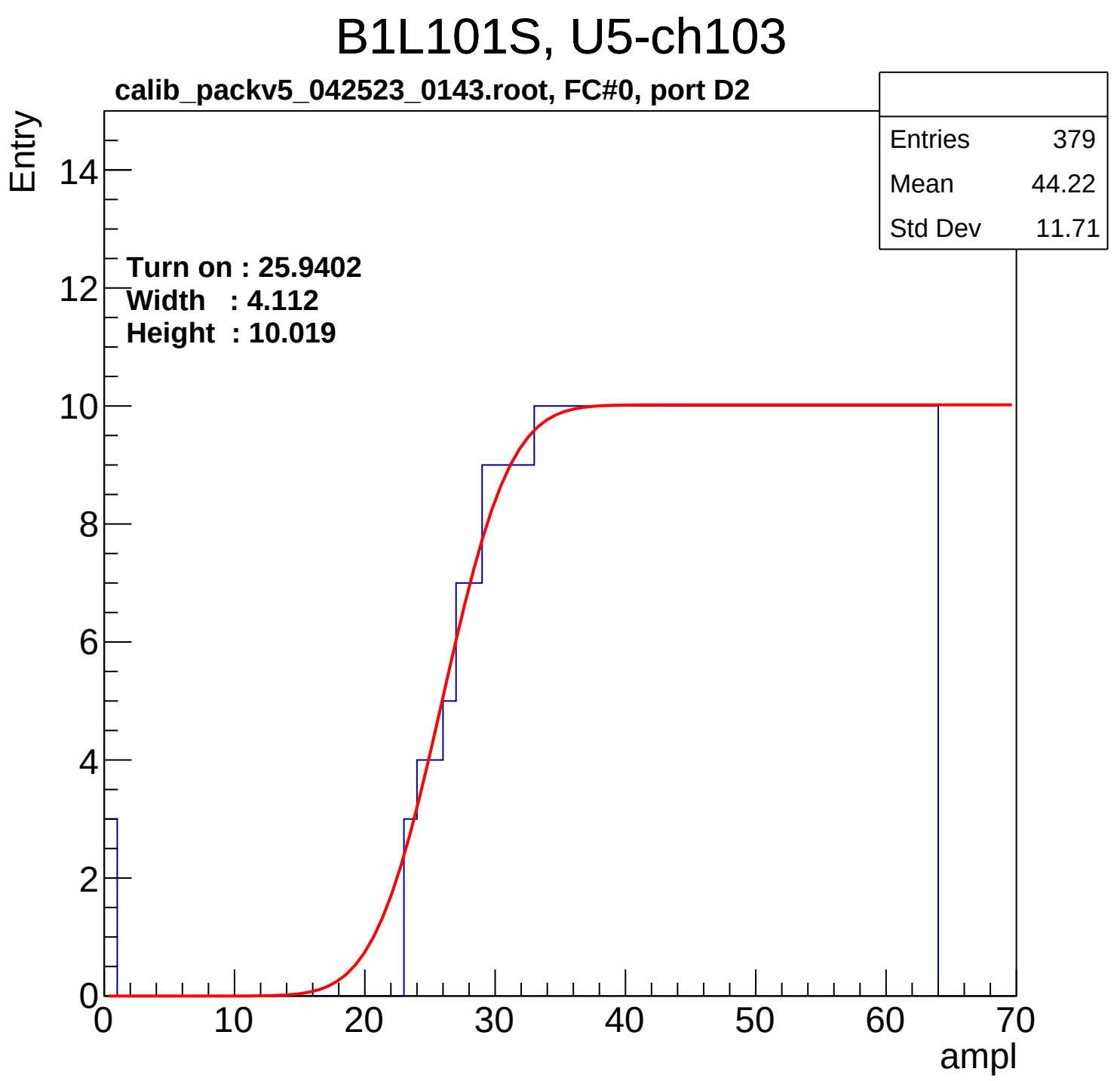

B1L101S, U5-ch98
calib_packv5_042523_0143.root, FC#0, port D2
Entries 397
Mean 43.27
Std Dev 12.32
Turn on : 24.5178
Width : 3.008
Height : 9.938
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

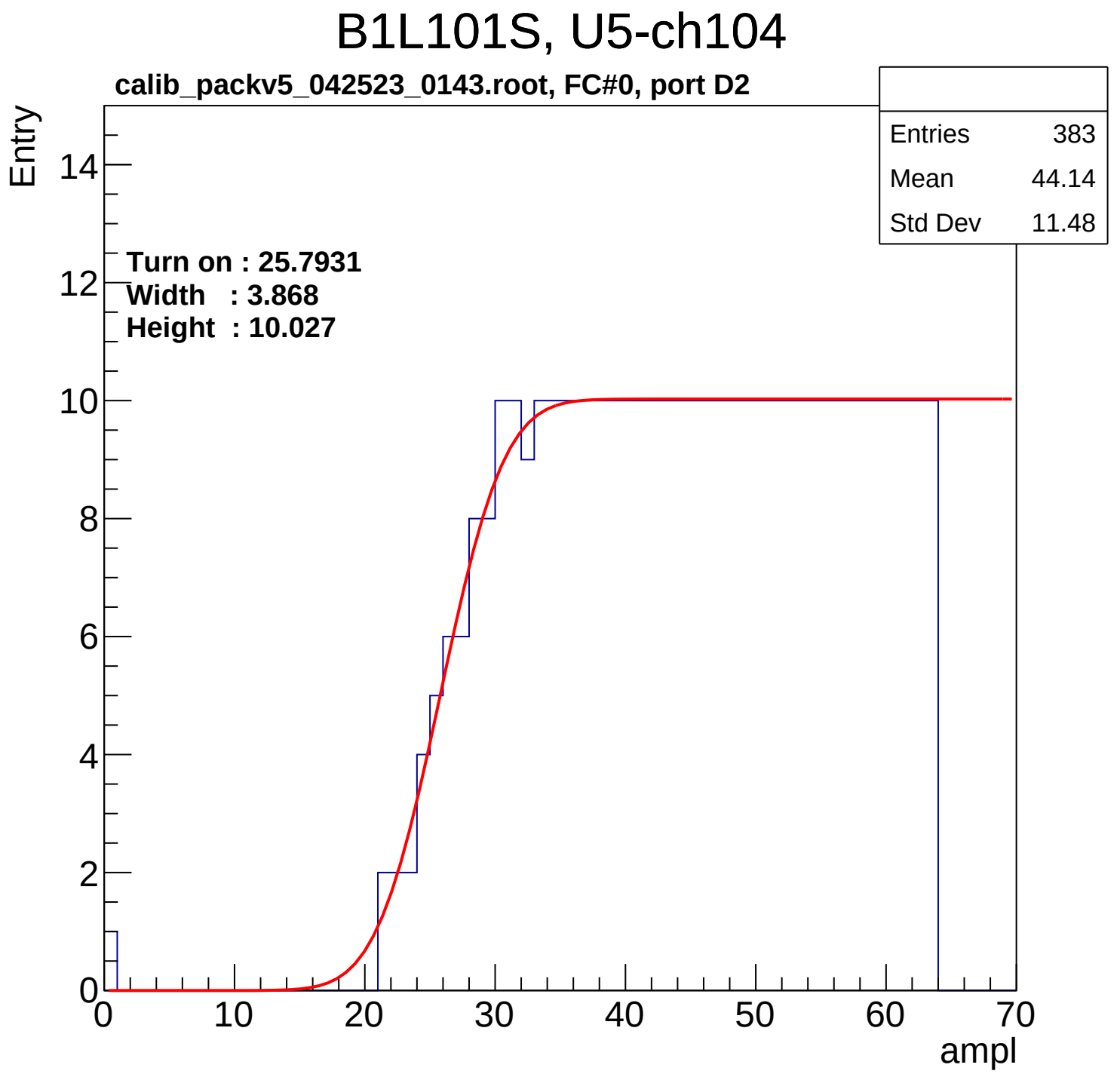

B1L101S, U5-ch99
calib_packv5_042523_0143.root, FC#0, port D2
Entries 406
Mean 43.02
Std Dev 12.08
Turn on : 23.5518
Width : 3.312
Height : 9.991
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

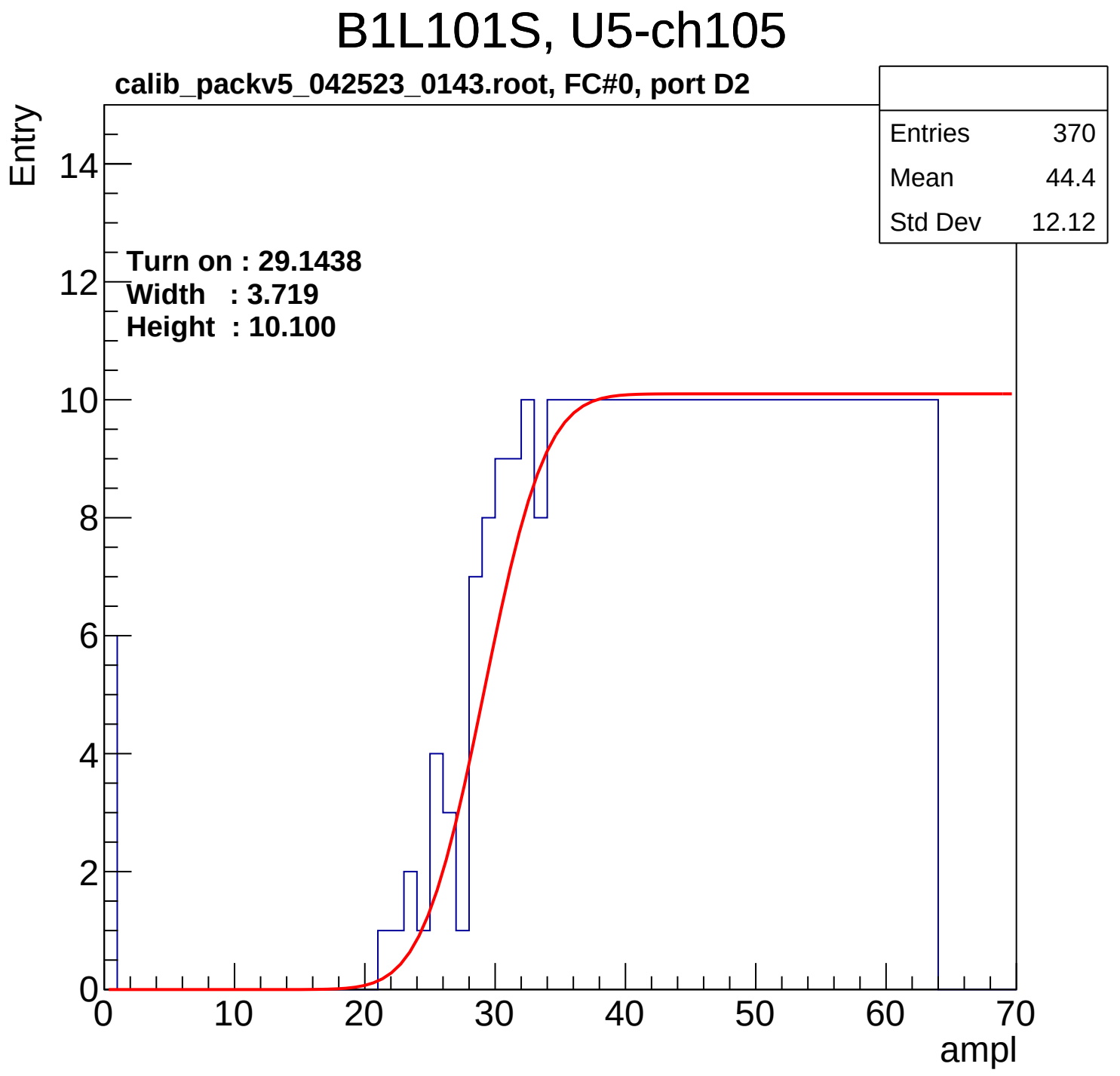

B1L101S, U5-ch100
calib_packv5_042523_0143.root, FC#0, port D2
Entries 380
Mean 44.24
Std Dev 11.54
Turn on : 26.3853
Width : 3.198
Height : 10.013
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

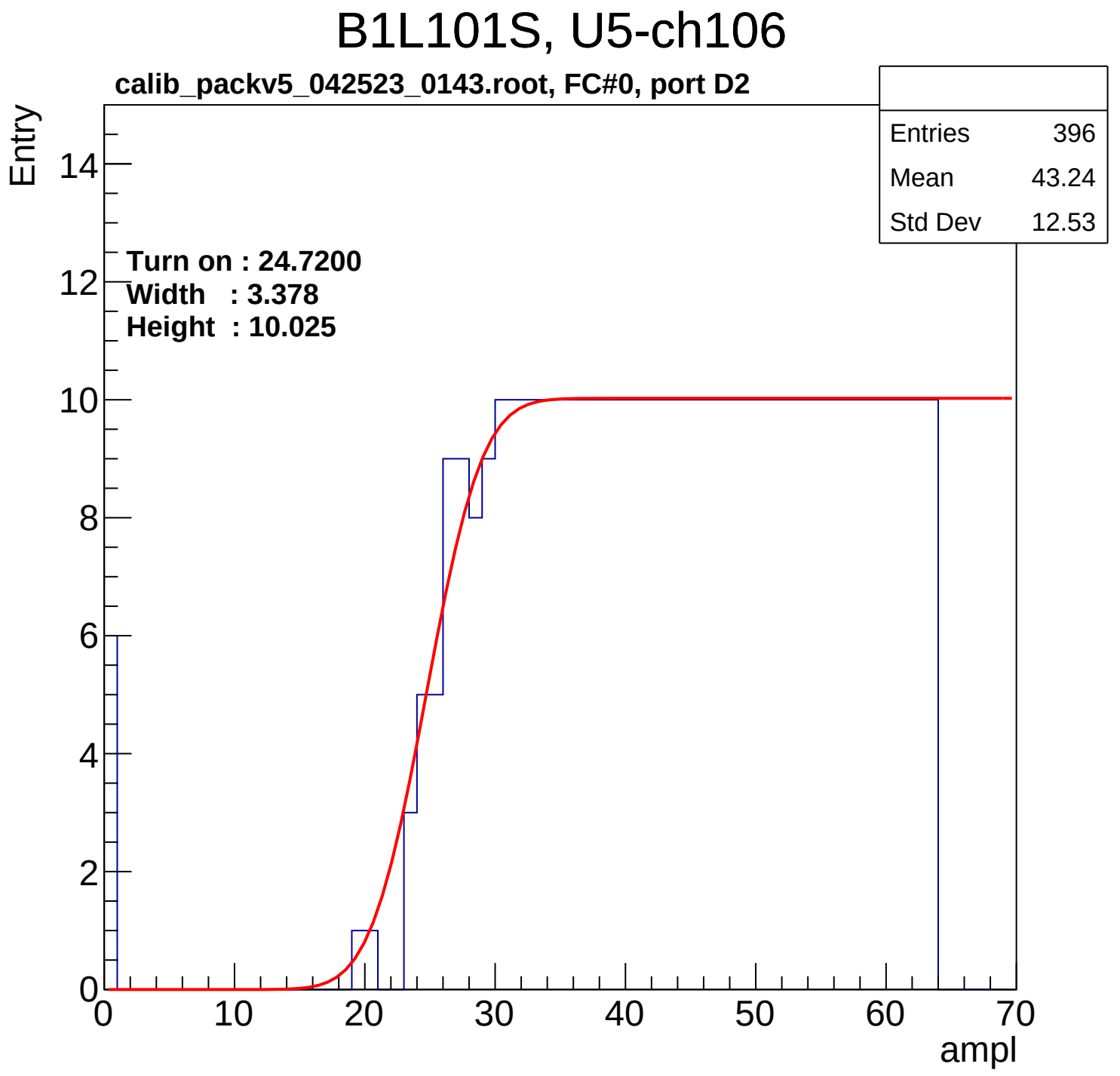

B1L101S, U5-ch101
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.75
Std Dev 12.1
Turn on : 26.1702
Width : 4.312
Height : 10.084
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

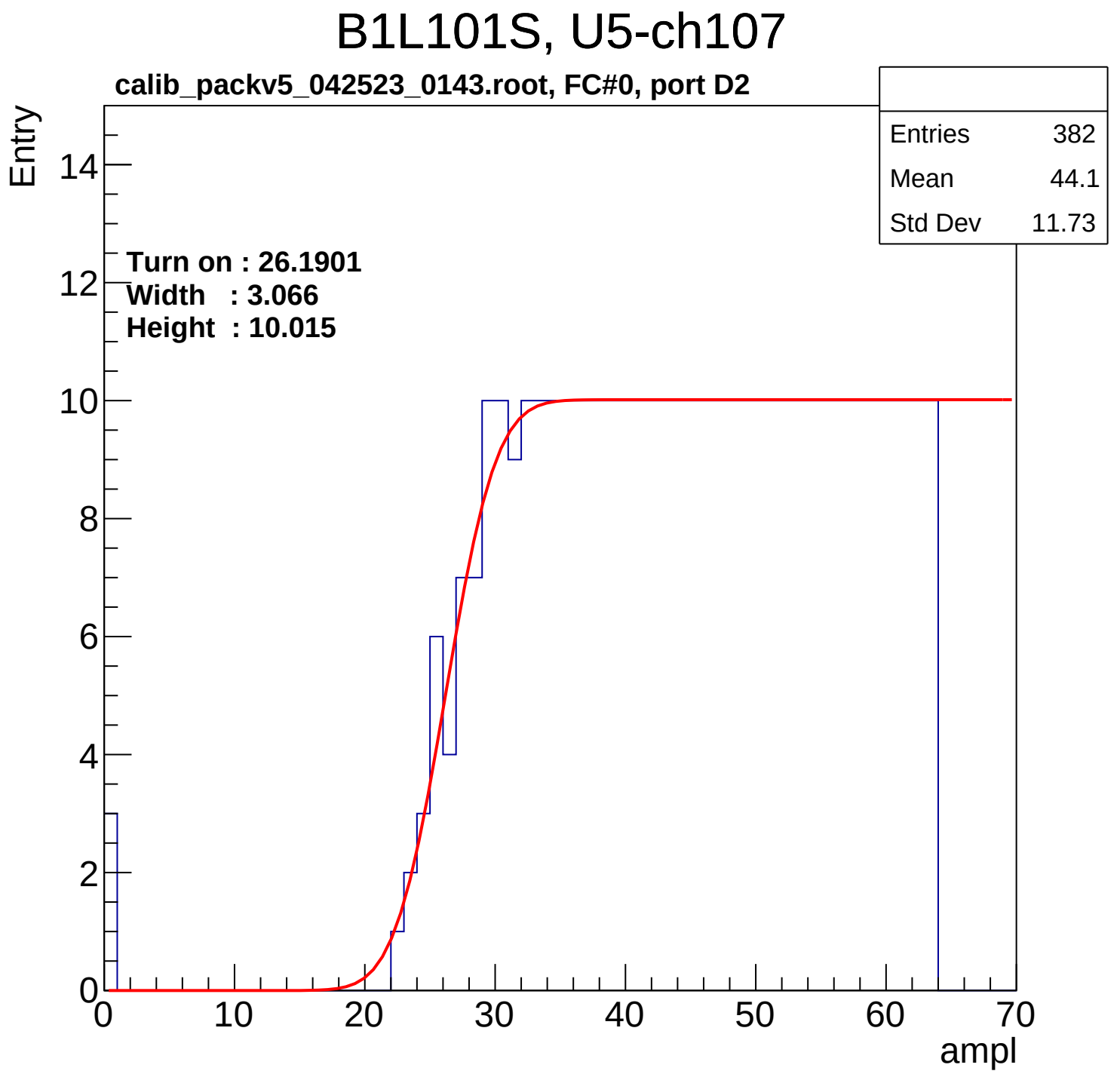

B1L101S, U5-ch102
calib_packv5_042523_0143.root, FC#0, port D2
Entries 386
Mean 44.04
Std Dev 11.48
Turn on : 25.1574
Width : 3.125
Height : 9.995
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

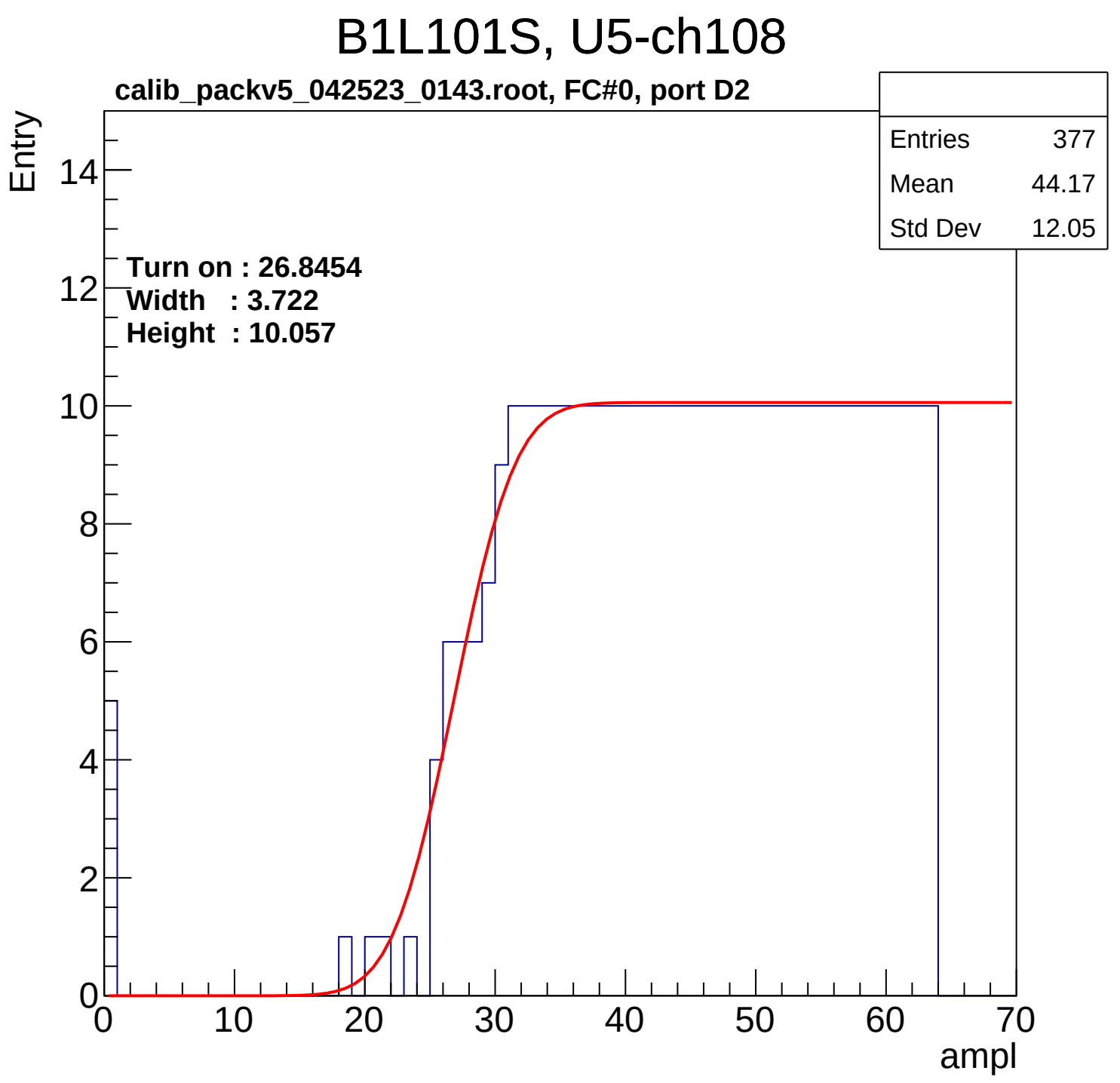

B1L101S, U5-ch103
calib_packv5_042523_0143.root, FC#0, port D2
Entries 379
Mean 44.22
Std Dev 11.71
Turn on : 25.9402
Width : 4.112
Height : 10.019
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

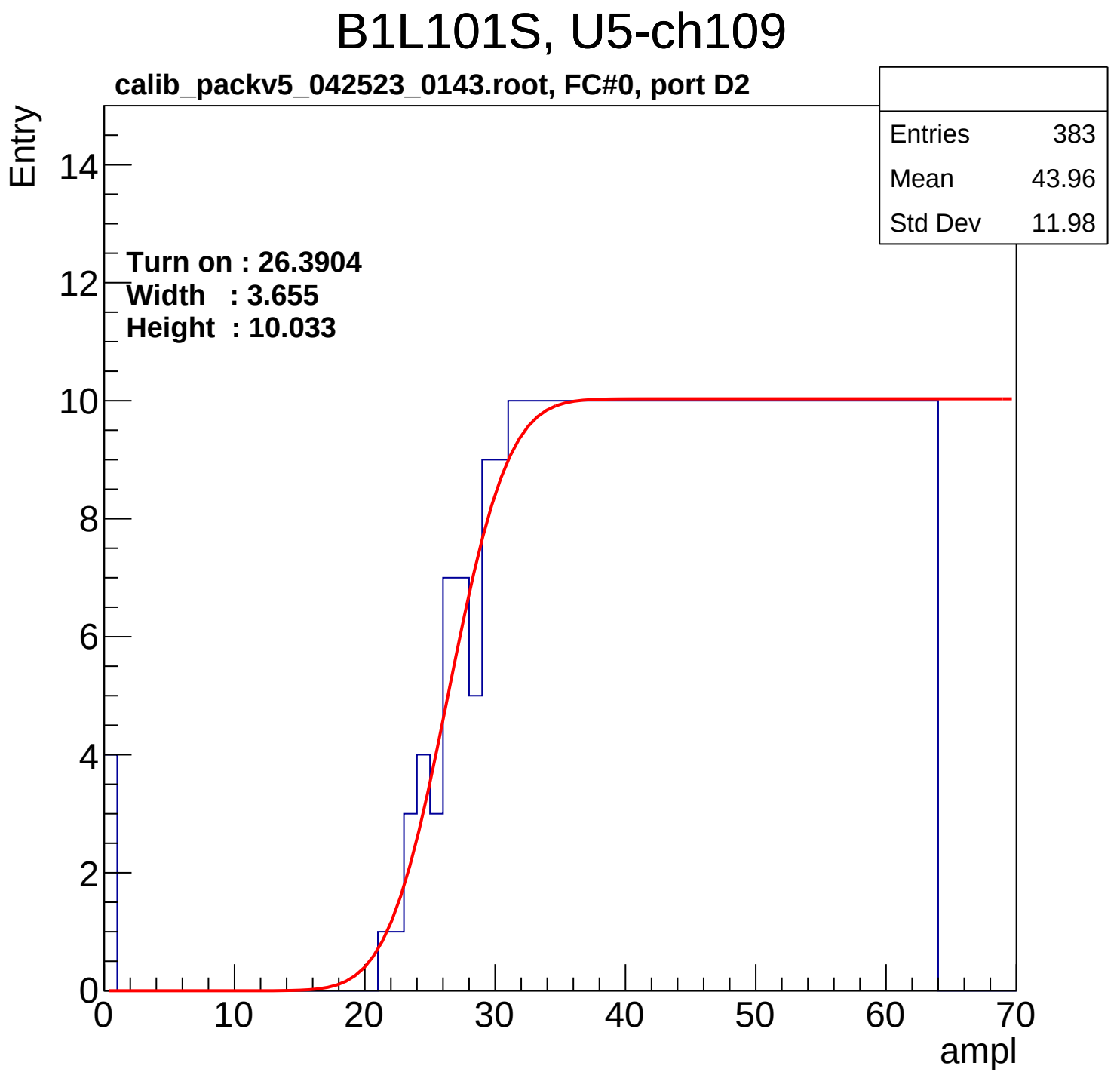

B1L101S, U5-ch104
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 44.14
Std Dev 11.48
Turn on : 25.7931
Width : 3.868
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

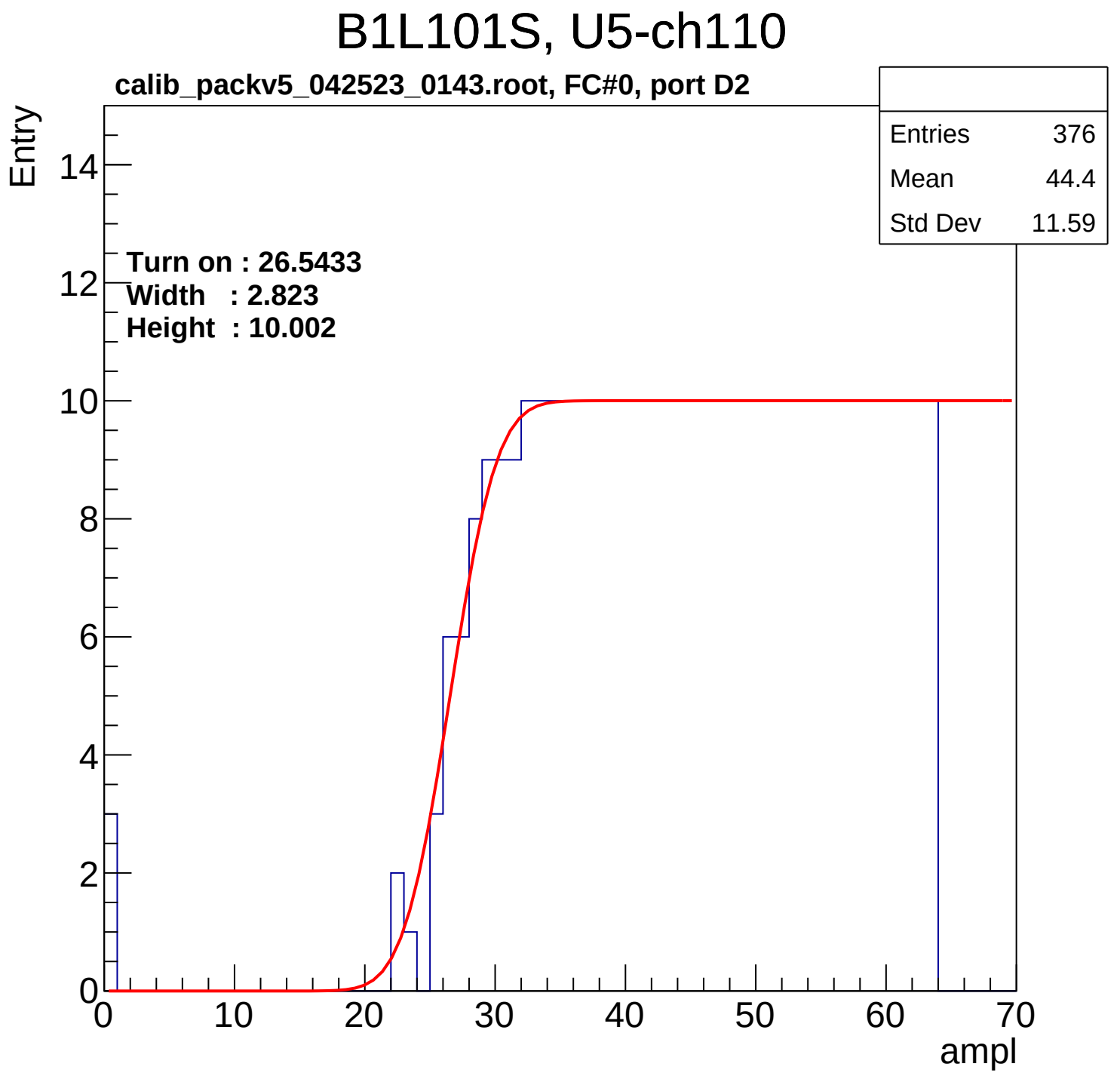

B1L101S, U5-ch105
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.4
Std Dev 12.12
Turn on : 29.1438
Width : 3.719
Height : 10.100
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

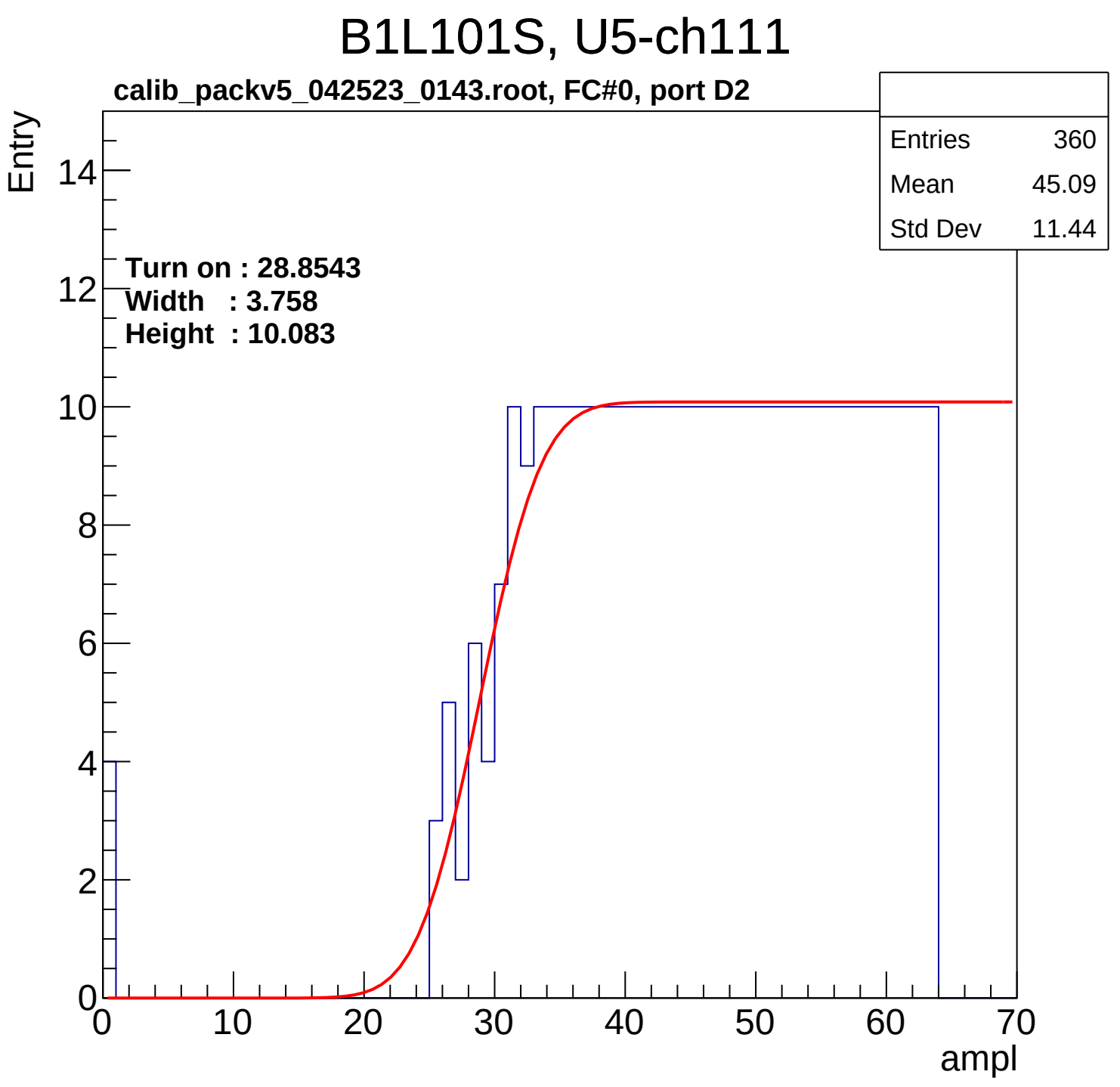

B1L101S, U5-ch106
calib_packv5_042523_0143.root, FC#0, port D2
Entries 396
Mean 43.24
Std Dev 12.53
Turn on : 24.7200
Width : 3.378
Height : 10.025
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

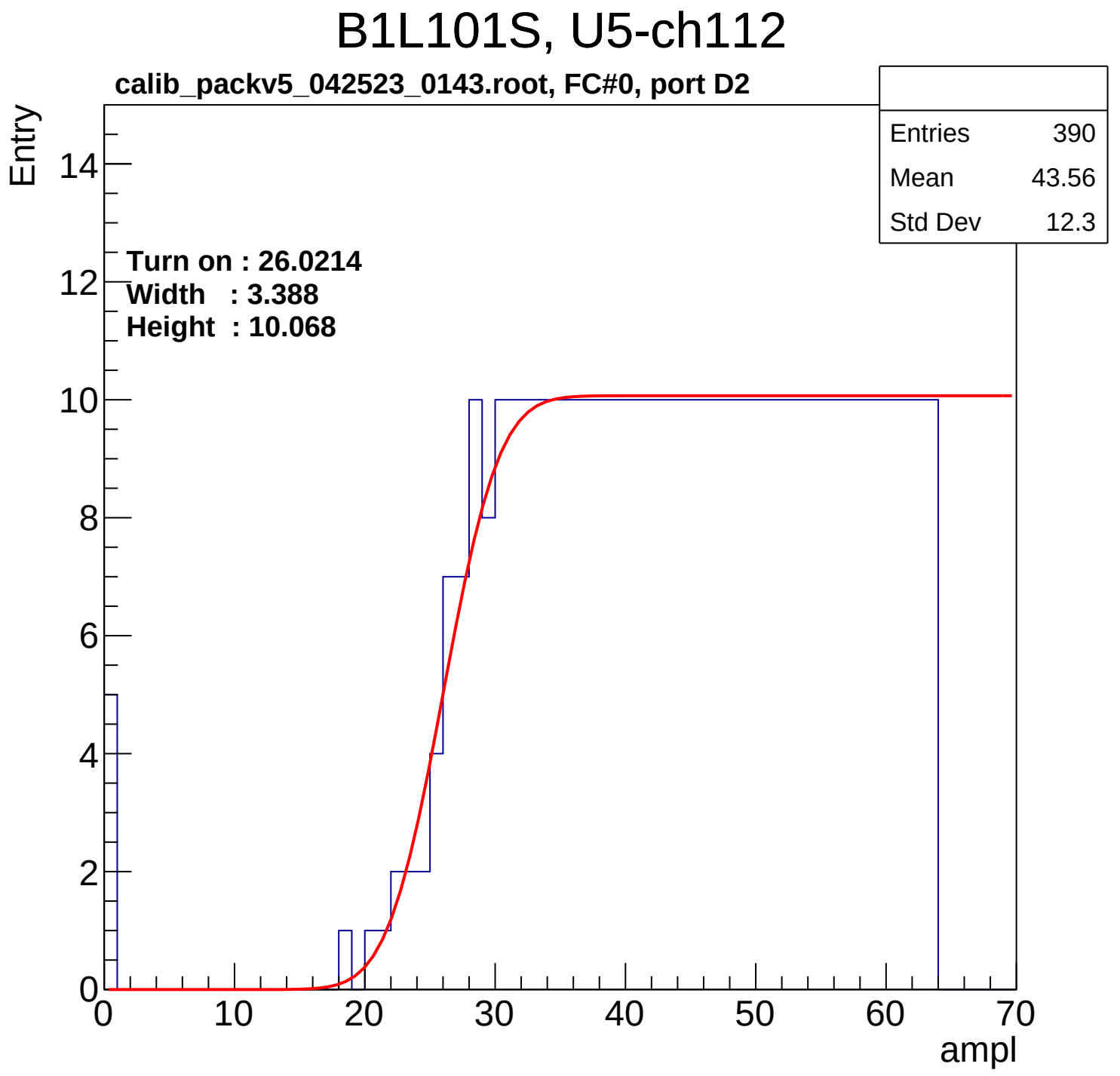

B1L101S, U5-ch107
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 44.1
Std Dev 11.73
Turn on : 26.1901
Width : 3.066
Height : 10.015
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

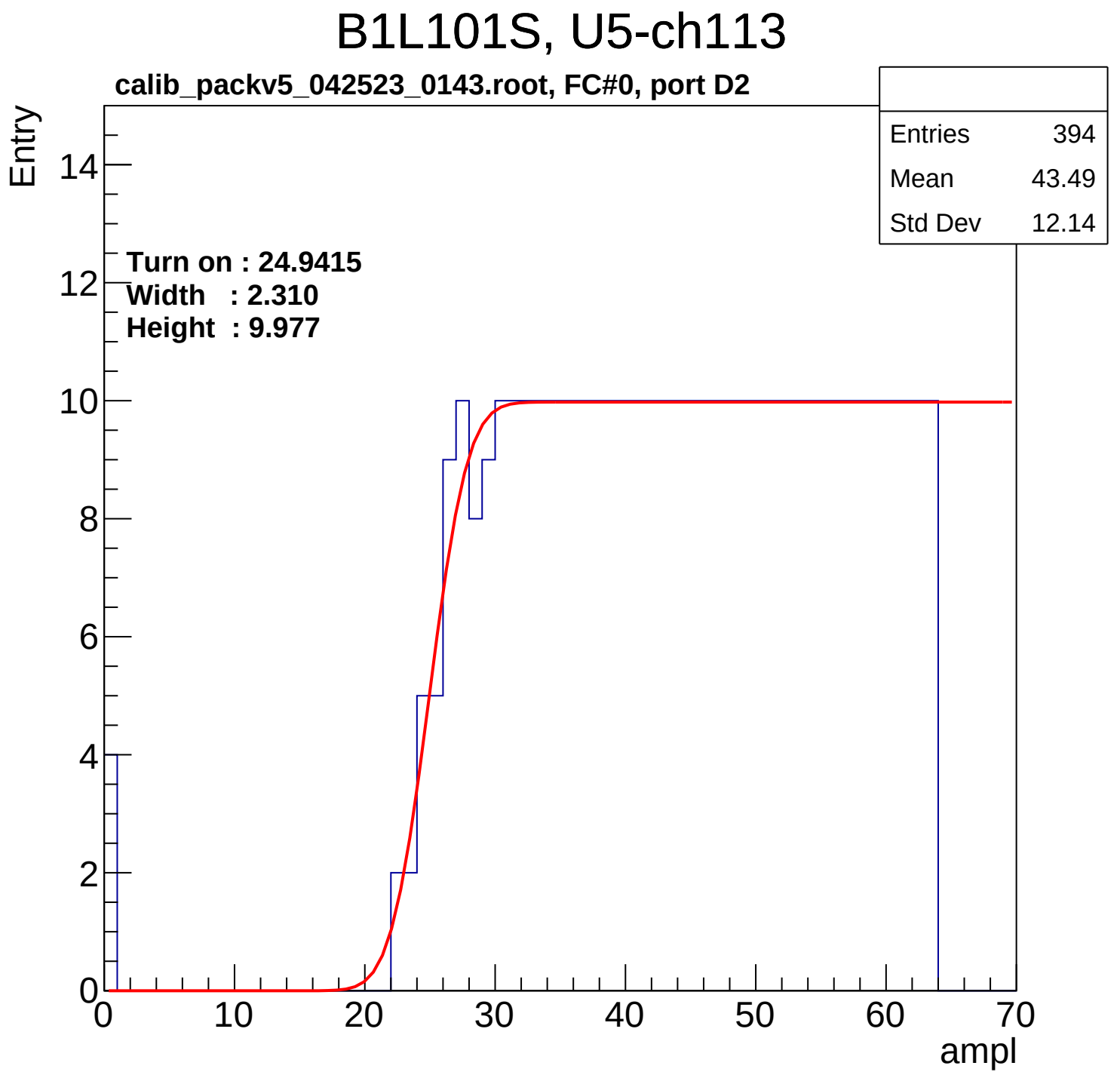

B1L101S, U5-ch108
calib_packv5_042523_0143.root, FC#0, port D2
Entries 377
Mean 44.17
Std Dev 12.05
Turn on : 26.8454
Width : 3.722
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

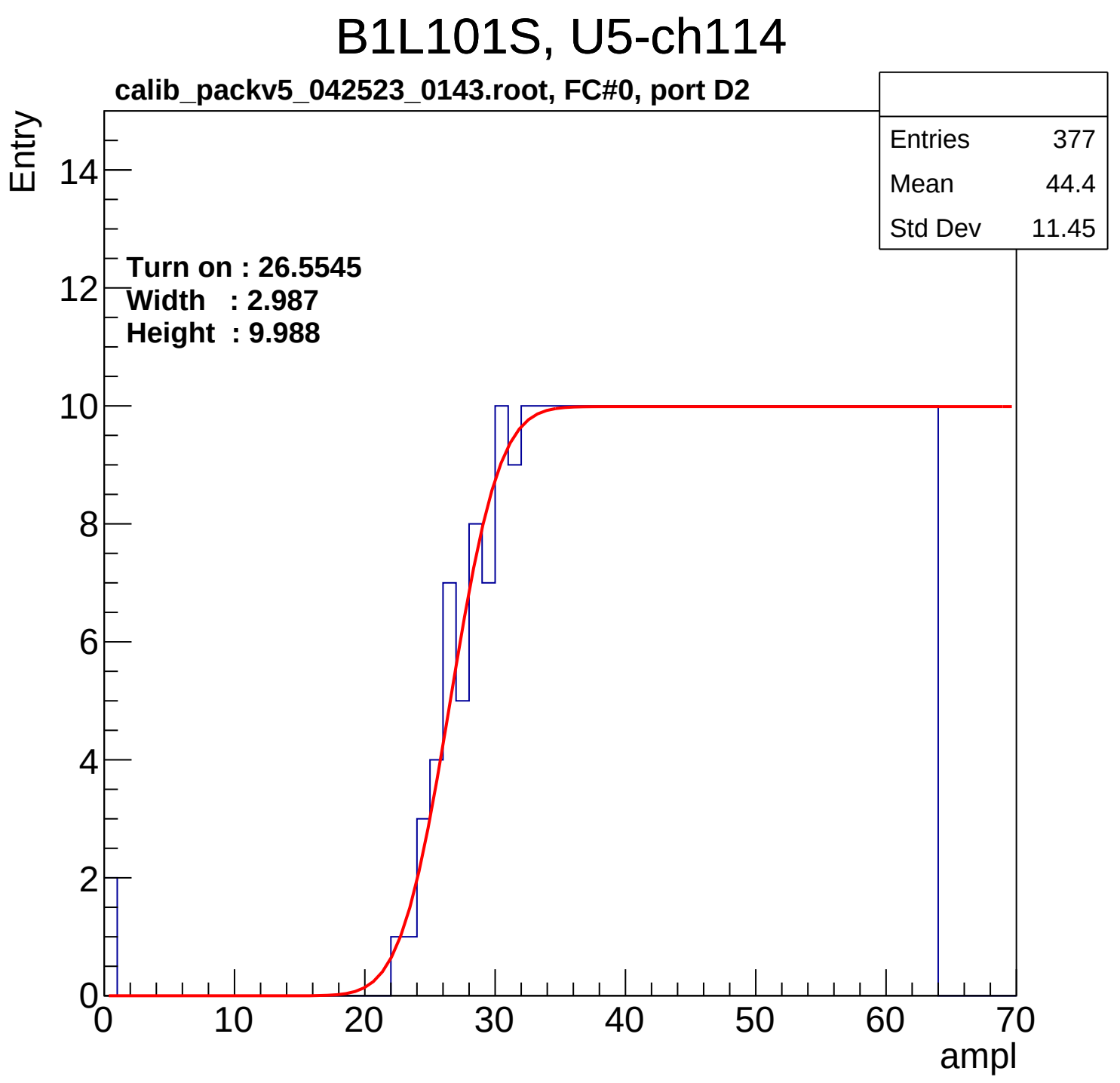

B1L101S, U5-ch109
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 43.96
Std Dev 11.98
Turn on : 26.3904
Width : 3.655
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

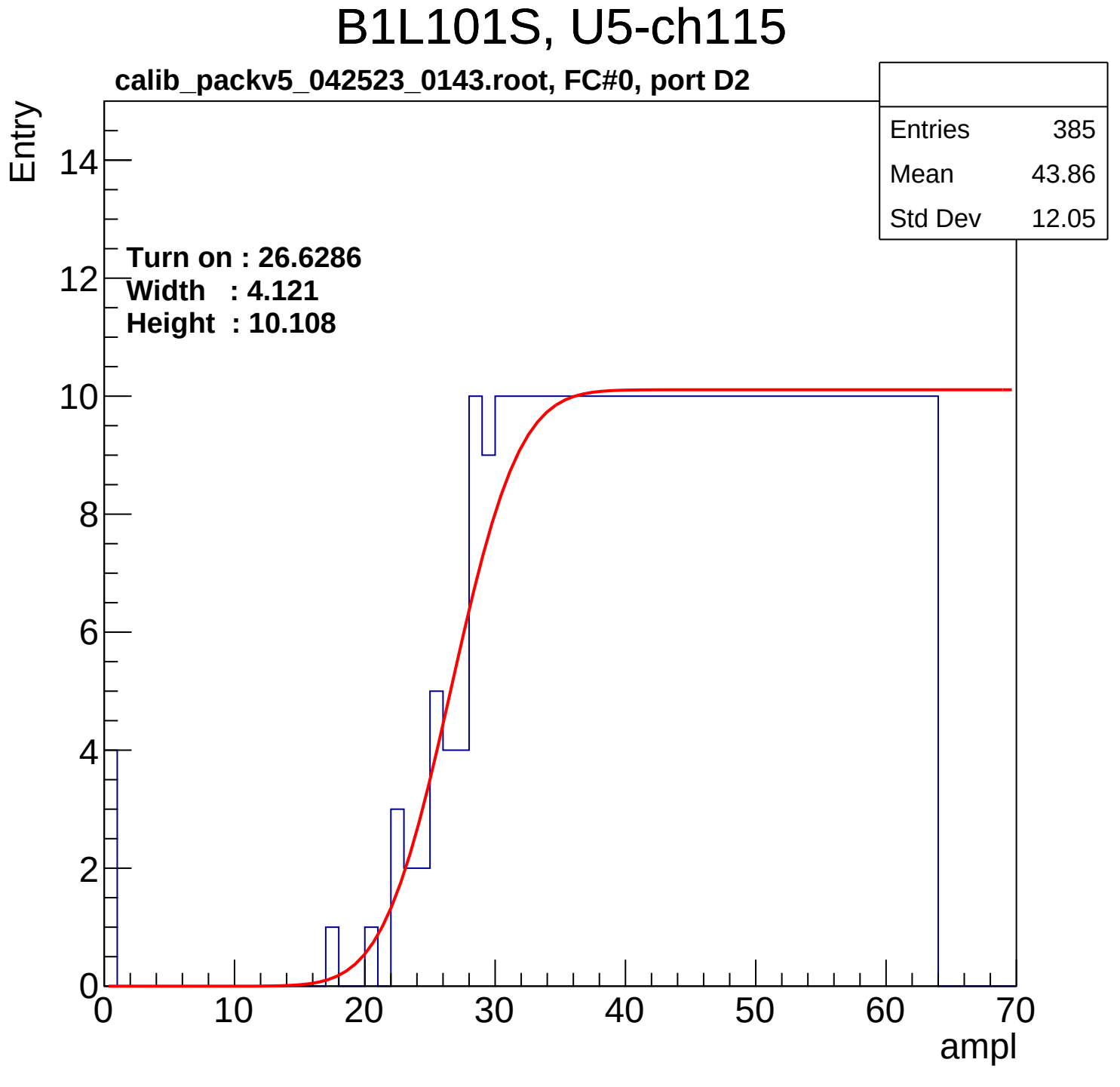

B1L101S, U5-ch110
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.4
Std Dev 11.59
Turn on : 26.5433
Width : 2.823
Height : 10.002
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

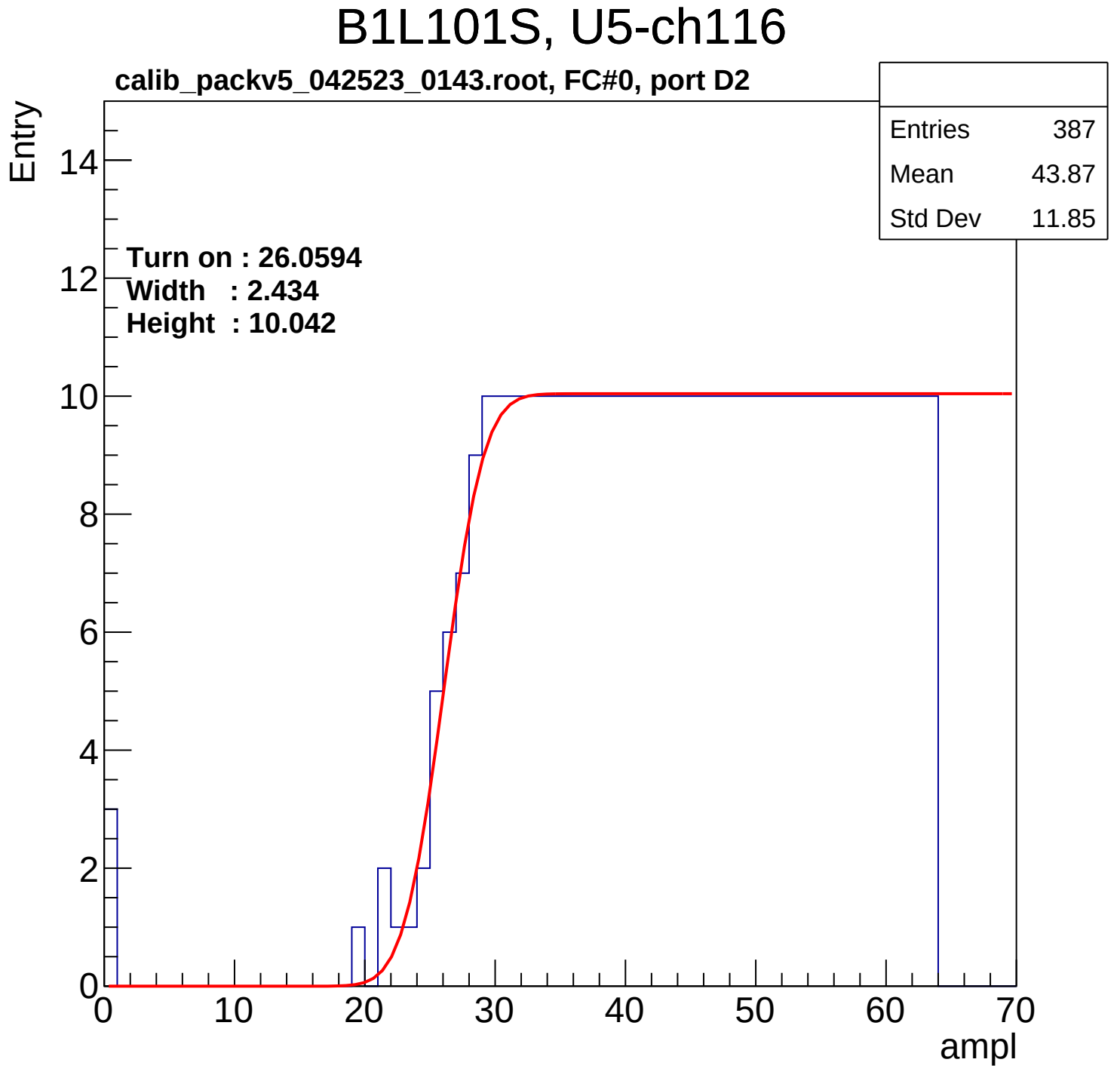

B1L101S, U5-ch111
calib_packv5_042523_0143.root, FC#0, port D2
Entries 360
Mean 45.09
Std Dev 11.44
Turn on : 28.8543
Width : 3.758
Height : 10.083
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

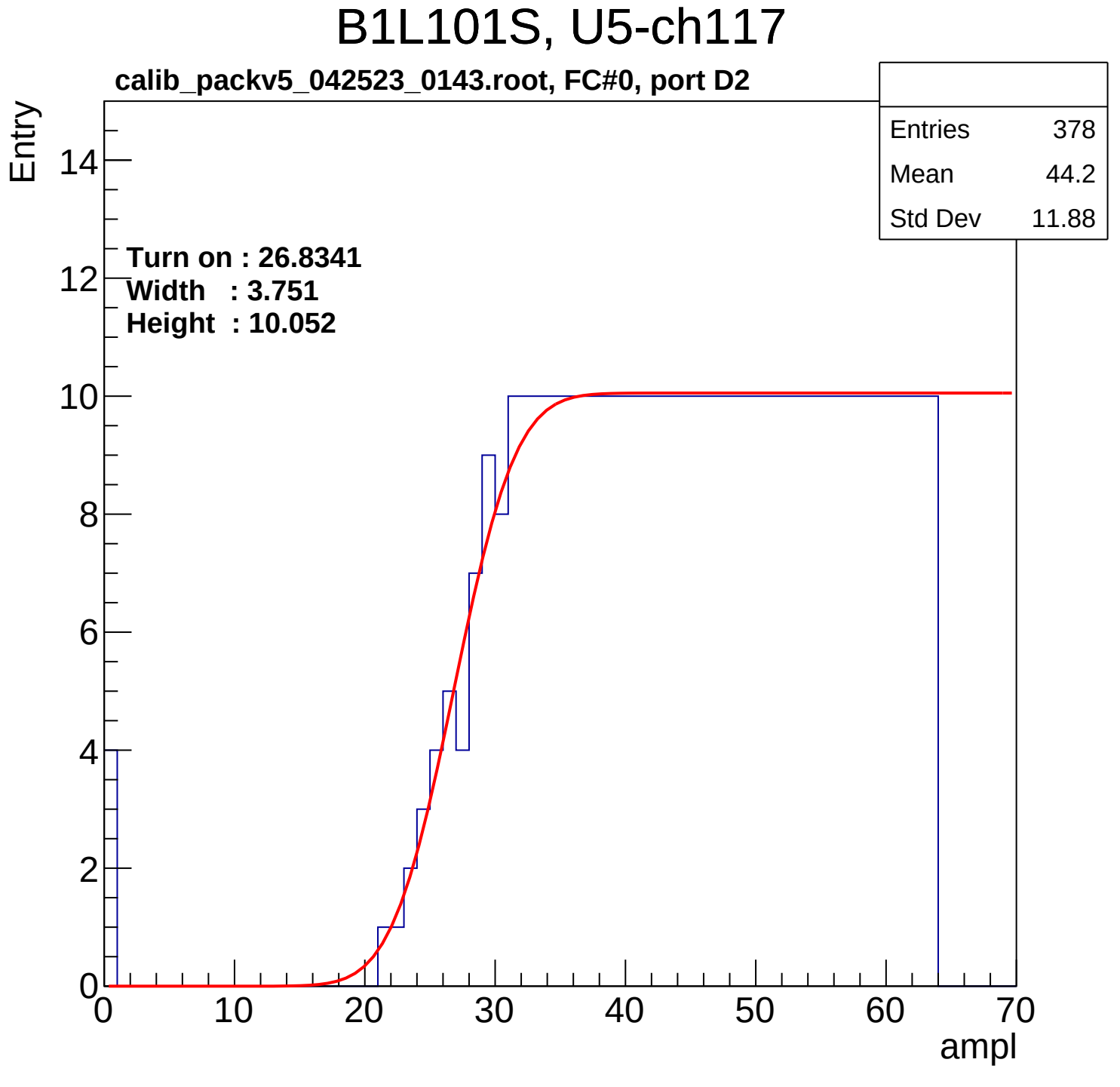

B1L101S, U5-ch112
calib_packv5_042523_0143.root, FC#0, port D2
Entries 390
Mean 43.56
Std Dev 12.3
Turn on : 26.0214
Width : 3.388
Height : 10.068
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

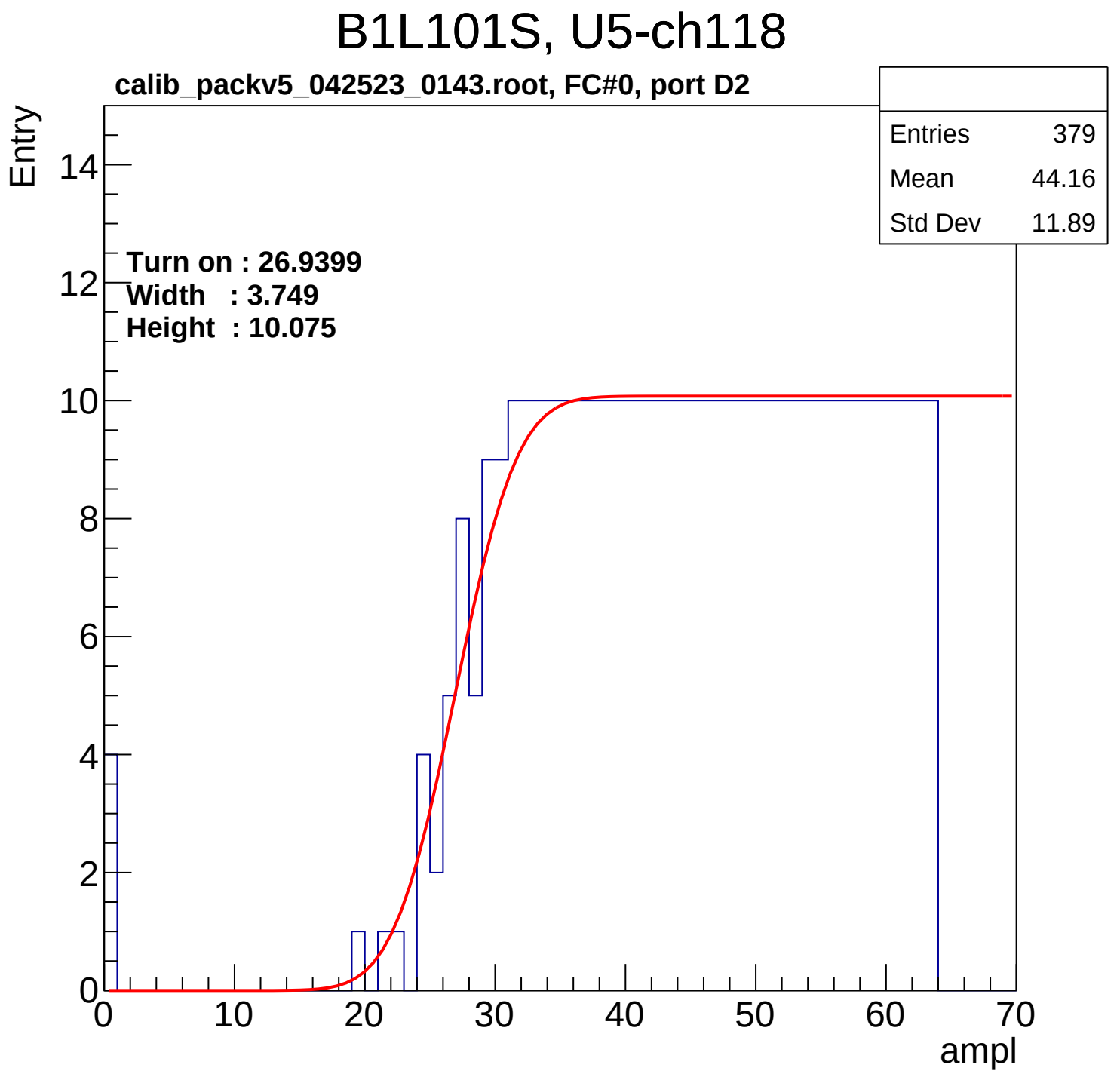

B1L101S, U5-ch113
calib_packv5_042523_0143.root, FC#0, port D2
Entries 394
Mean 43.49
Std Dev 12.14
Turn on : 24.9415
Width : 2.310
Height : 9.977
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

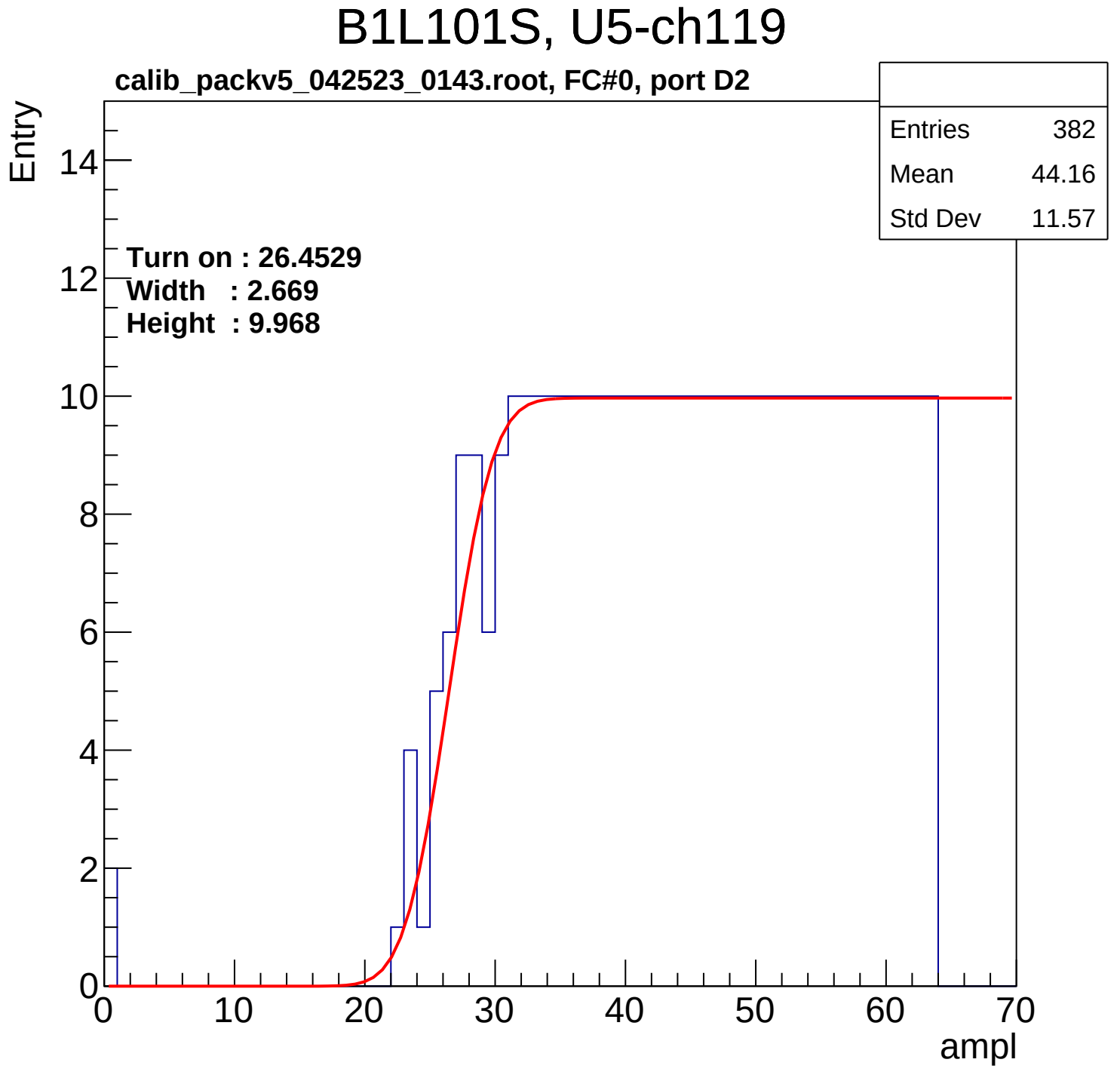

B1L101S, U5-ch114
calib_packv5_042523_0143.root, FC#0, port D2
Entries 377
Mean 44.4
Std Dev 11.45
Turn on : 26.5545
Width : 2.987
Height : 9.988
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

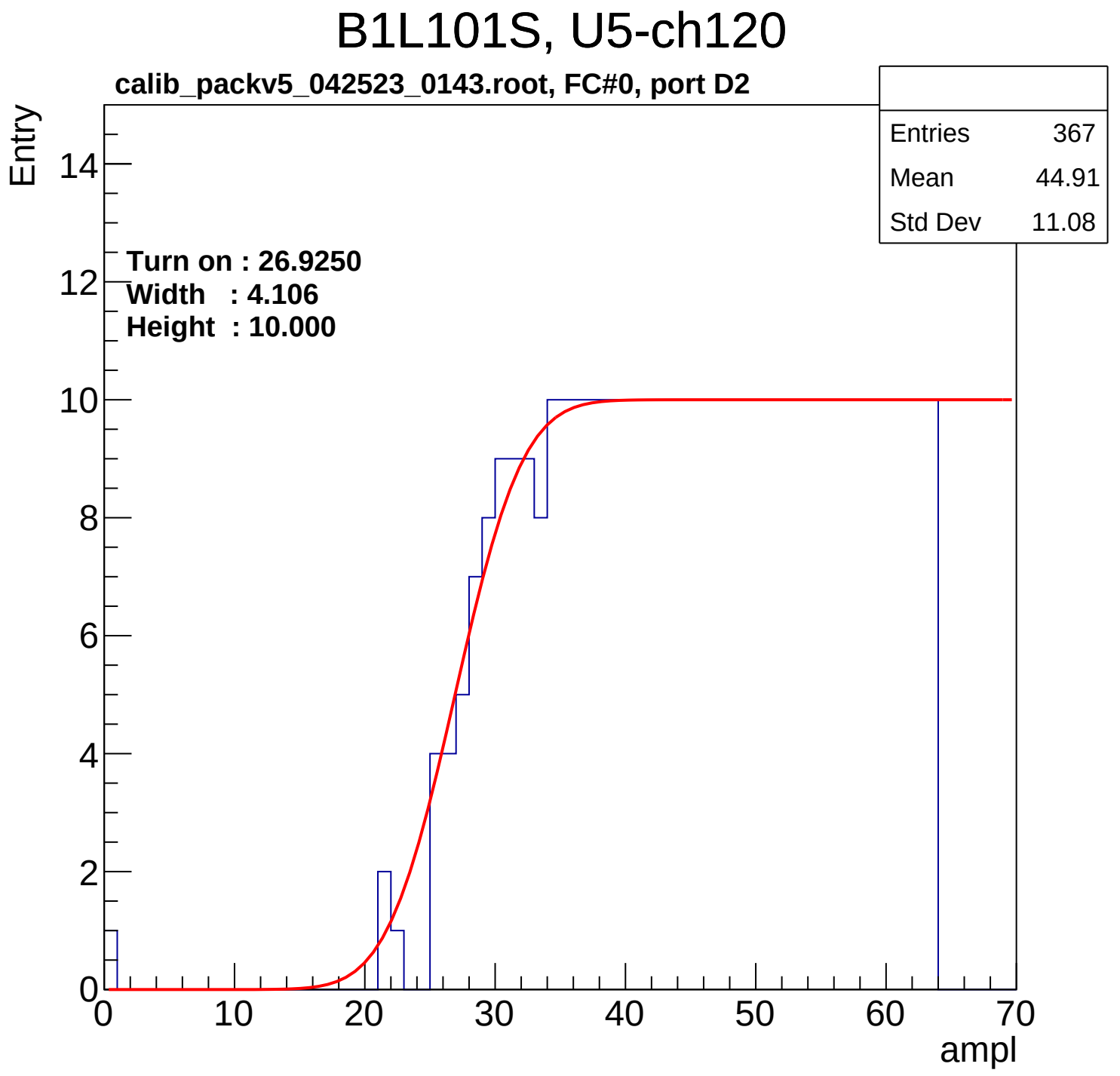

B1L101S, U5-ch115
calib_packv5_042523_0143.root, FC#0, port D2
Entries 385
Mean 43.86
Std Dev 12.05
Turn on : 26.6286
Width : 4.121
Height : 10.108
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

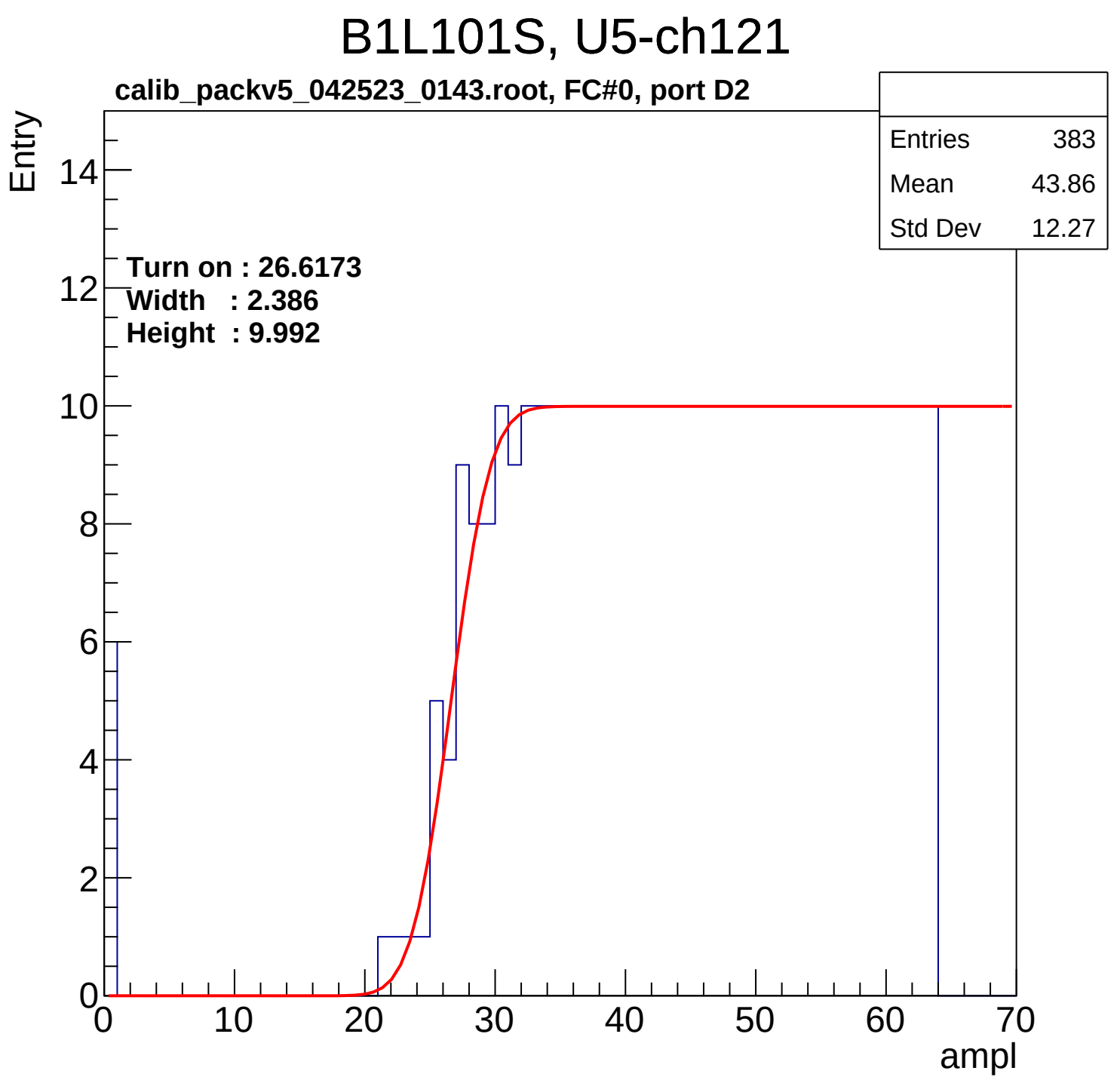

B1L101S, U5-ch116
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.87
Std Dev 11.85
Turn on : 26.0594
Width : 2.434
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

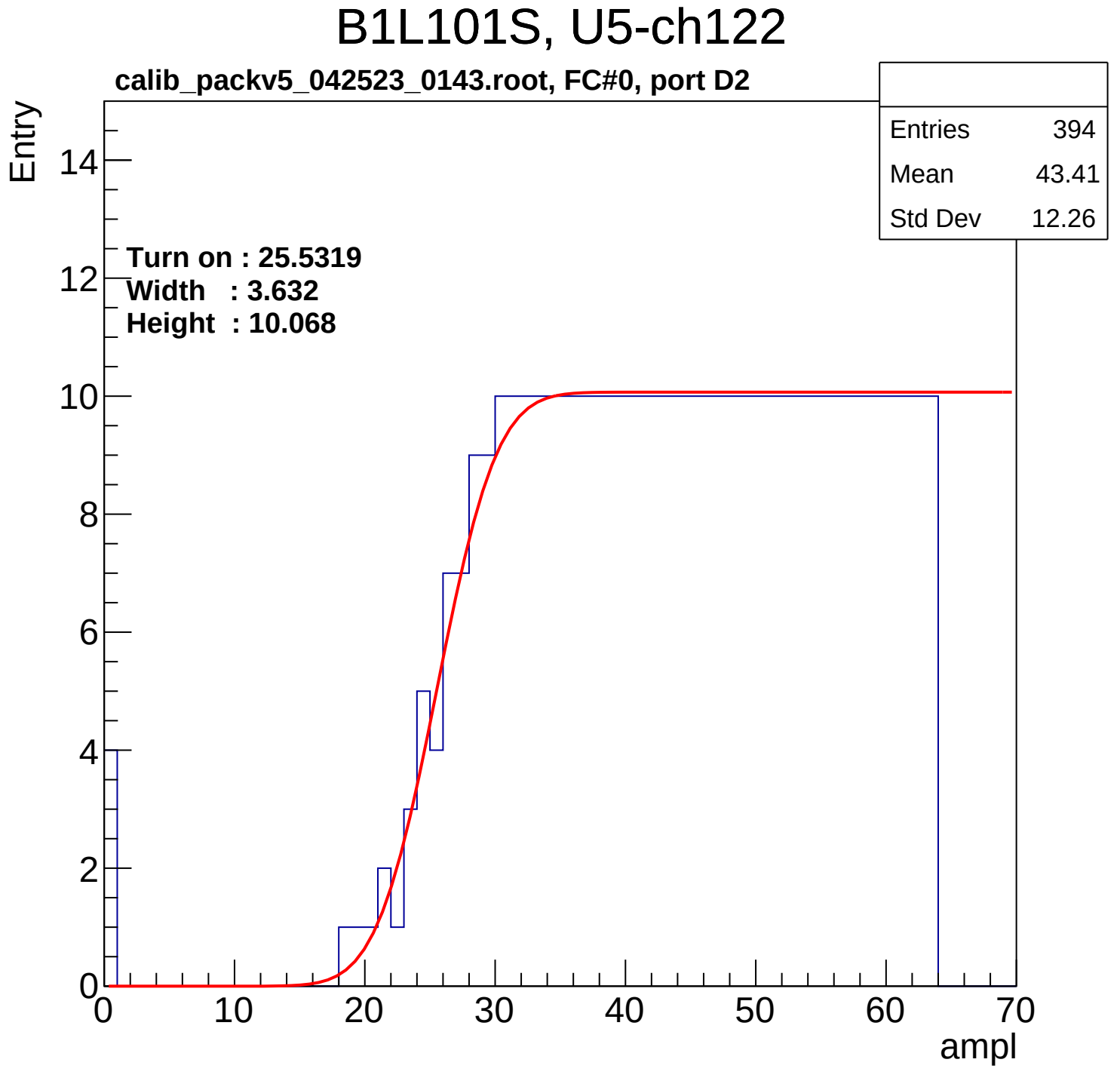

B1L101S, U5-ch117
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.2
Std Dev 11.88
Turn on : 26.8341
Width : 3.751
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

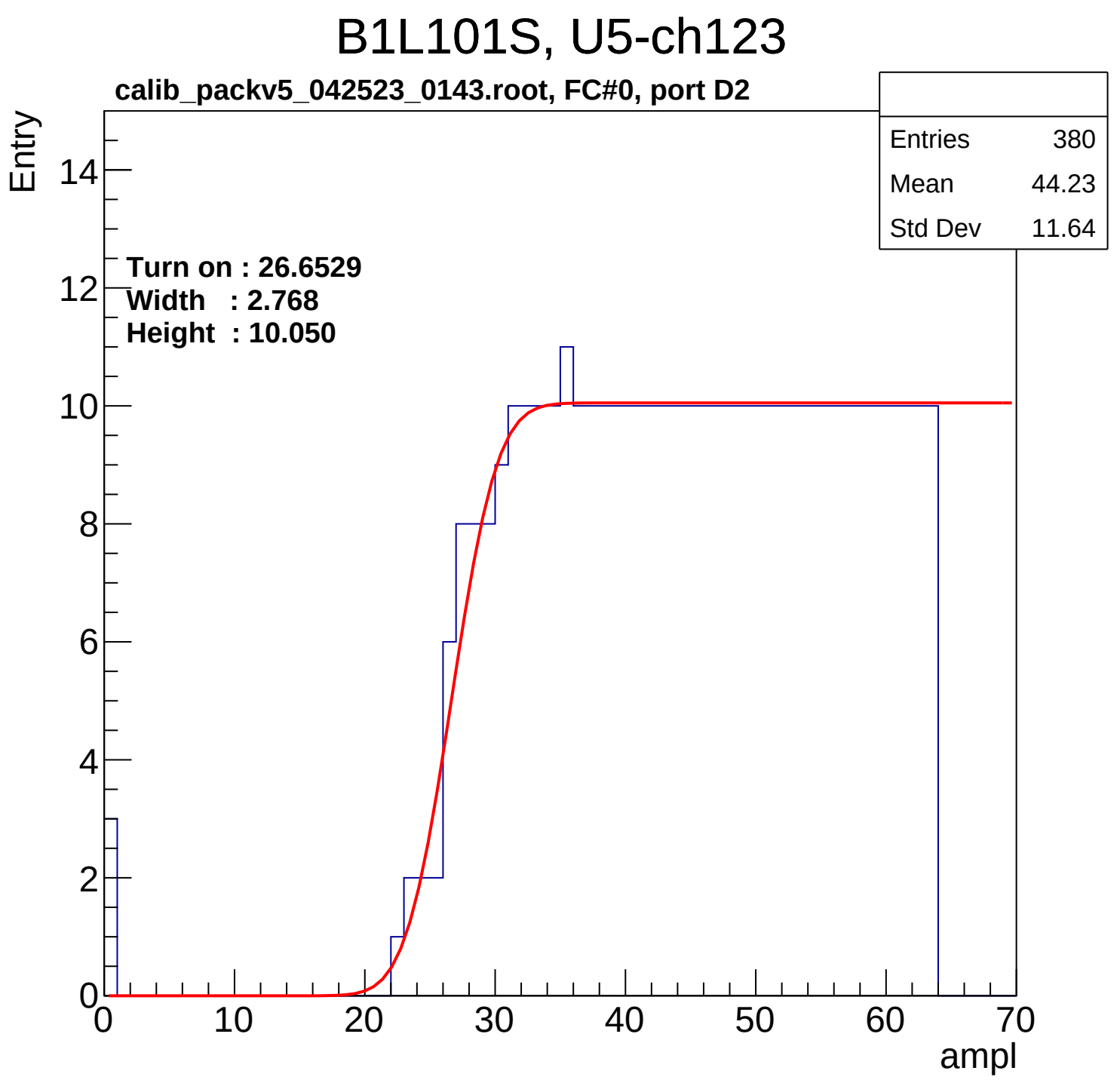

B1L101S, U5-ch118
calib_packv5_042523_0143.root, FC#0, port D2
Entries 379
Mean 44.16
Std Dev 11.89
Turn on : 26.9399
Width : 3.749
Height : 10.075
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

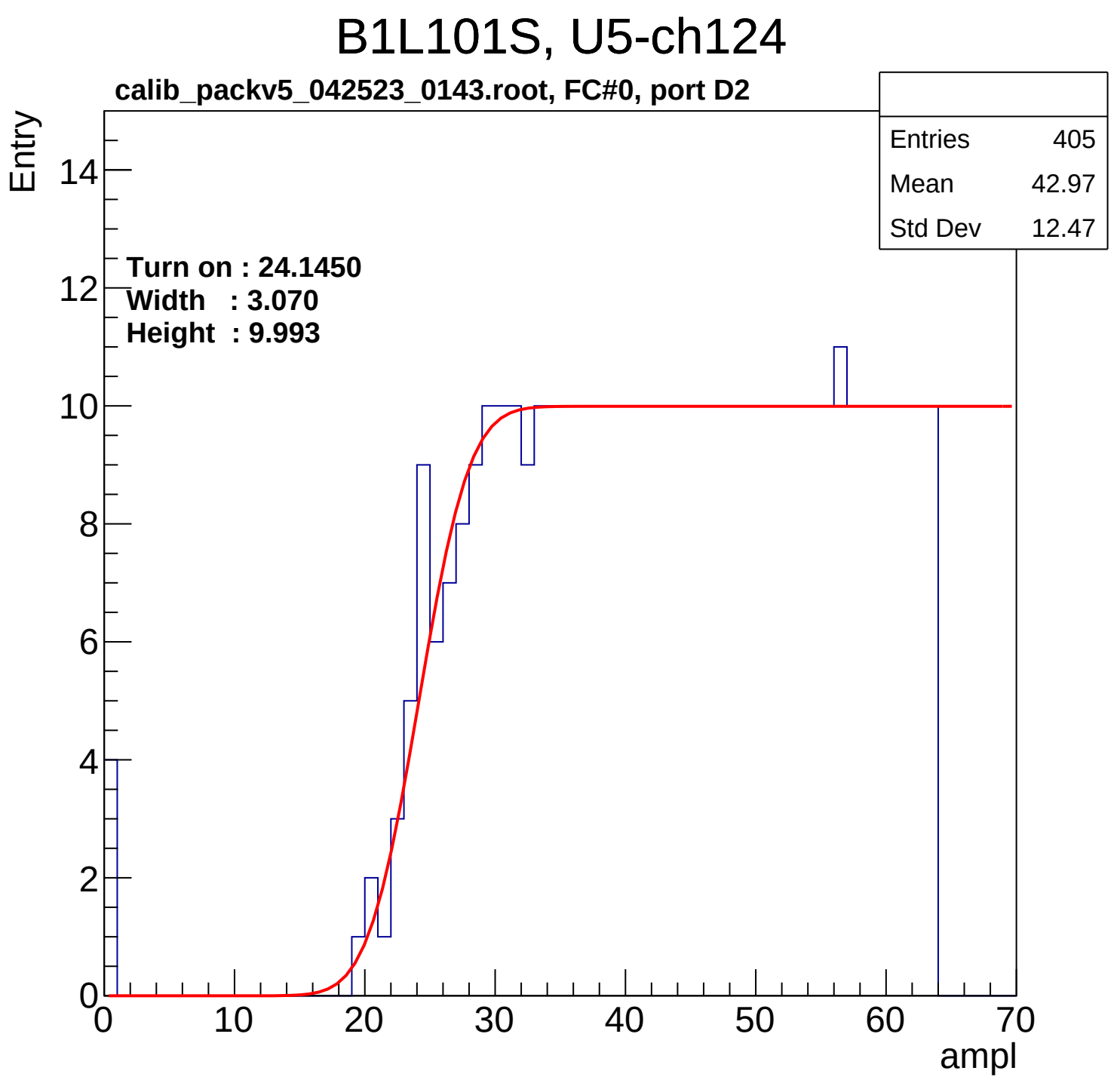

B1L101S, U5-ch119
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 44.16
Std Dev 11.57
Turn on : 26.4529
Width : 2.669
Height : 9.968
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

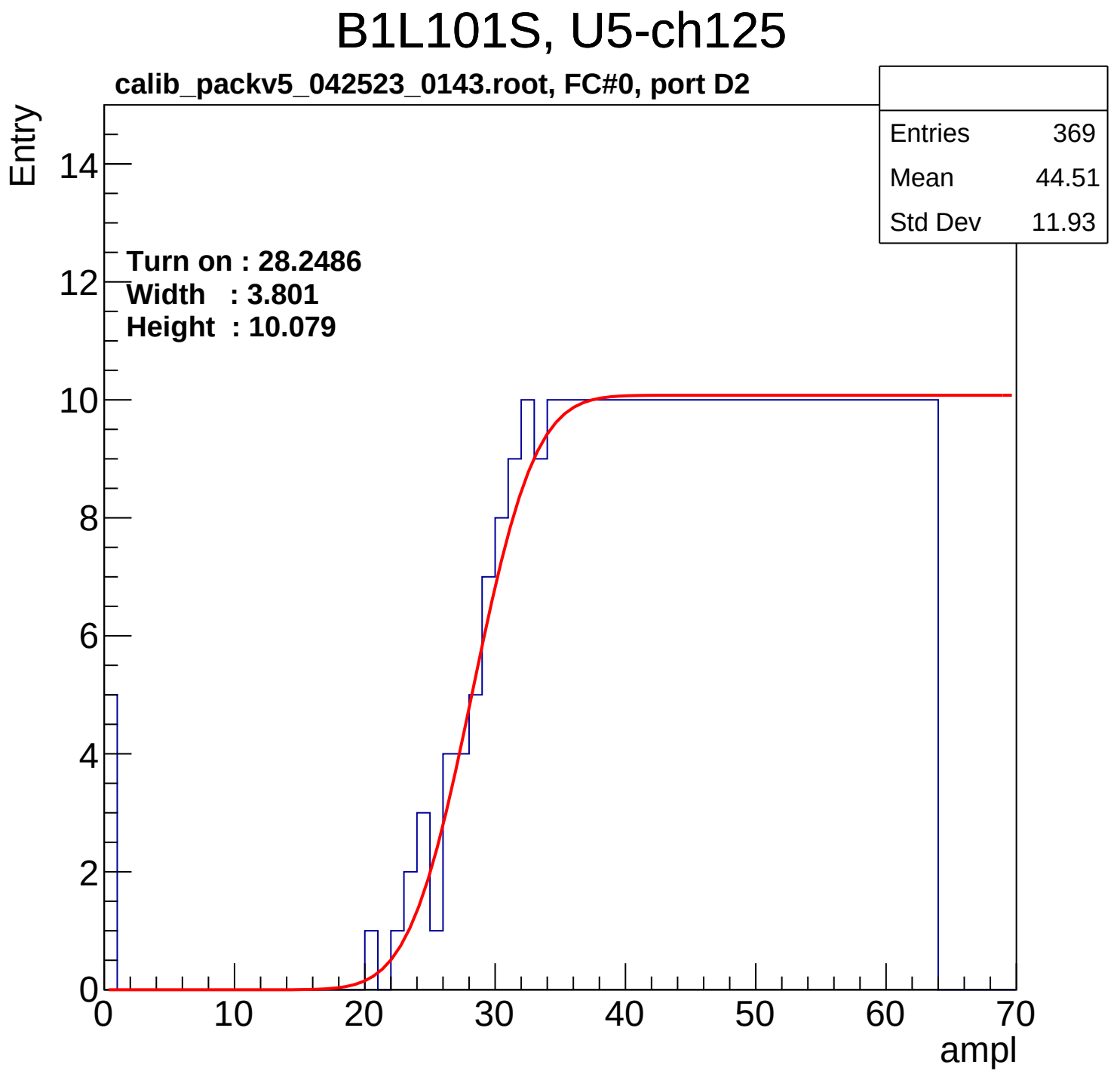

B1L101S, U5-ch120
calib_packv5_042523_0143.root, FC#0, port D2
Entries 367
Mean 44.91
Std Dev 11.08
Turn on : 26.9250
Width : 4.106
Height : 10.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

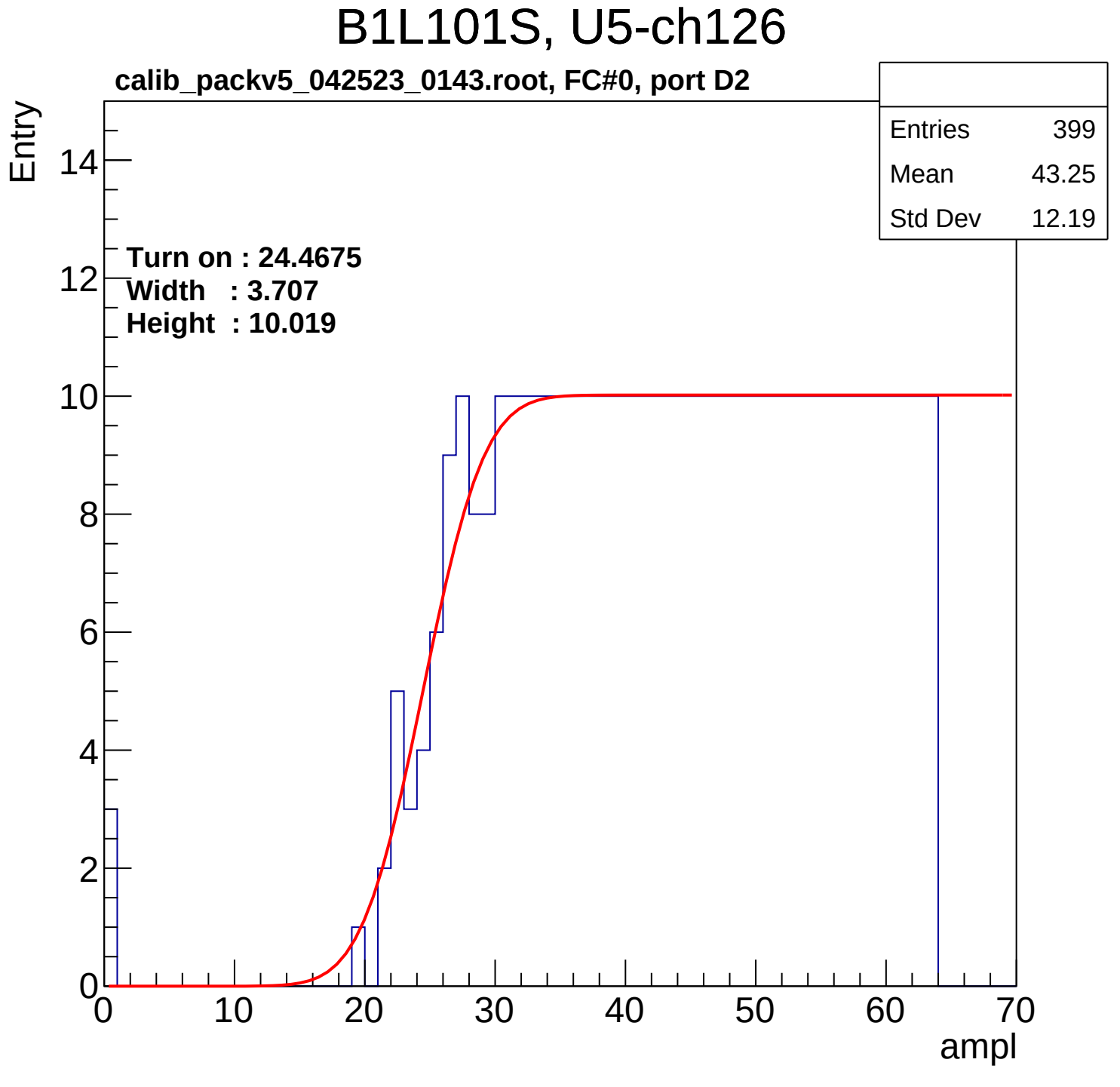

B1L101S, U5-ch121
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 43.86
Std Dev 12.27
Turn on : 26.6173
Width : 2.386
Height : 9.992
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

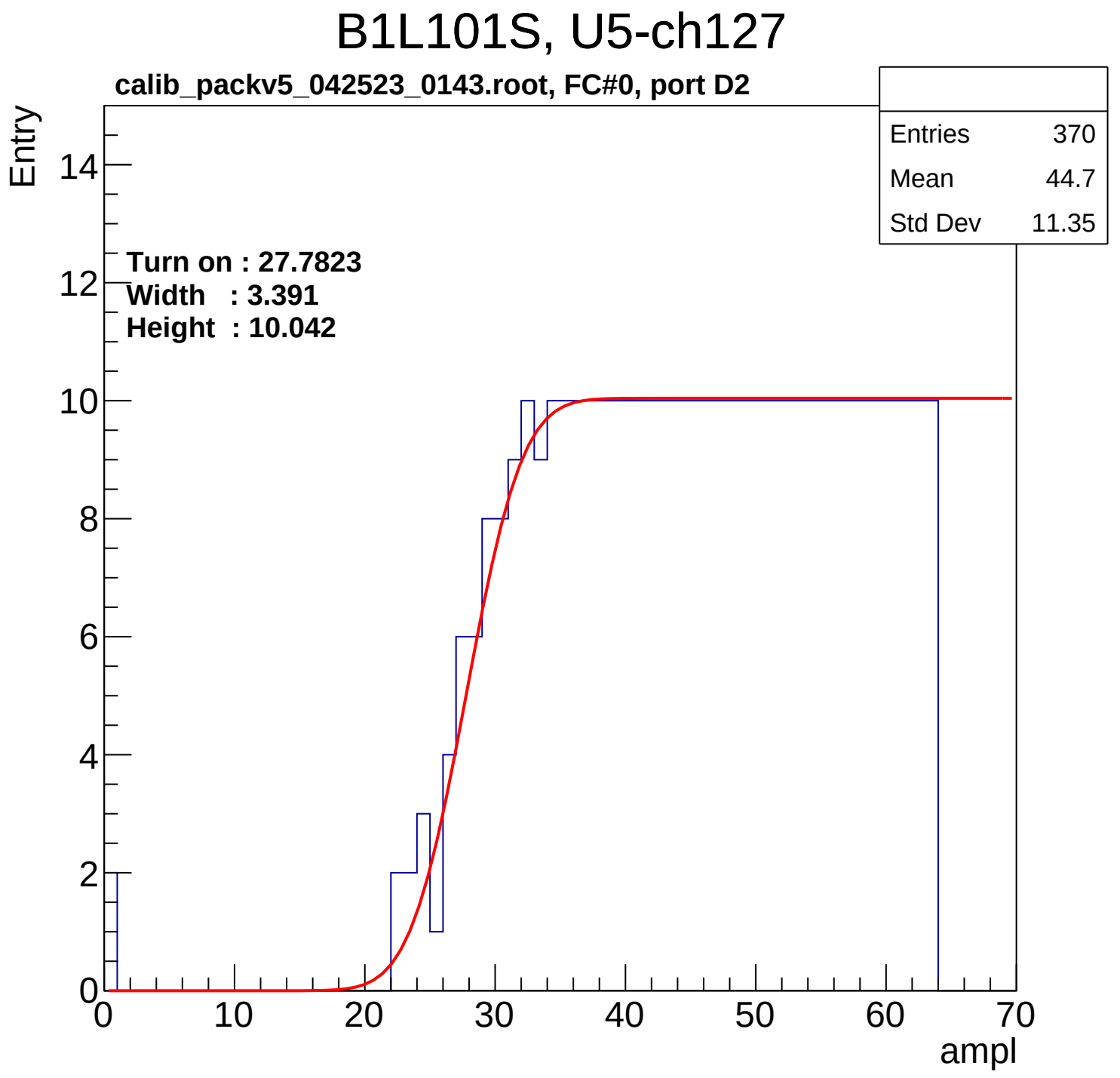

B1L101S, U5-ch122
calib_packv5_042523_0143.root, FC#0, port D2
Entries 394
Mean 43.41
Std Dev 12.26
Turn on : 25.5319
Width : 3.632
Height : 10.068
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

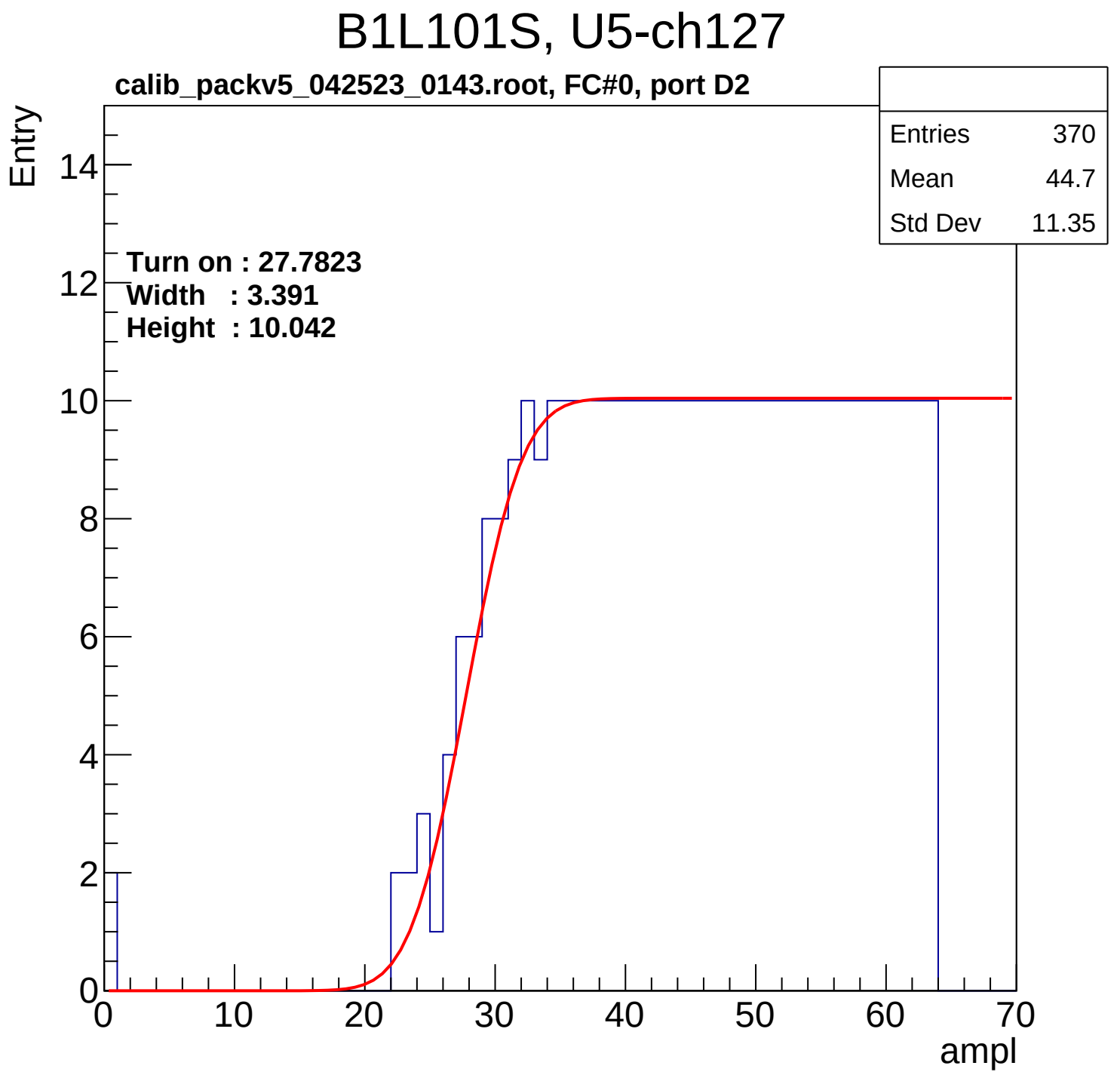

B1L101S, U5-ch123
calib_packv5_042523_0143.root, FC#0, port D2
Entries 380
Mean 44.23
Std Dev 11.64
Turn on : 26.6529
Width : 2.768
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U5-ch124
calib_packv5_042523_0143.root, FC#0, port D2
Entries 405
Mean 42.97
Std Dev 12.47
Turn on : 24.1450
Width : 3.070
Height : 9.993
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U5-ch125
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.51
Std Dev 11.93
Turn on : 28.2486
Width : 3.801
Height : 10.079
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U5-ch126
calib_packv5_042523_0143.root, FC#0, port D2
Entries 399
Mean 43.25
Std Dev 12.19
Turn on : 24.4675
Width : 3.707
Height : 10.019
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U5-ch127
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.7
Std Dev 11.35
Turn on : 27.7823
Width : 3.391
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U5-ch127
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.7
Std Dev 11.35
Turn on : 27.7823
Width : 3.391
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70