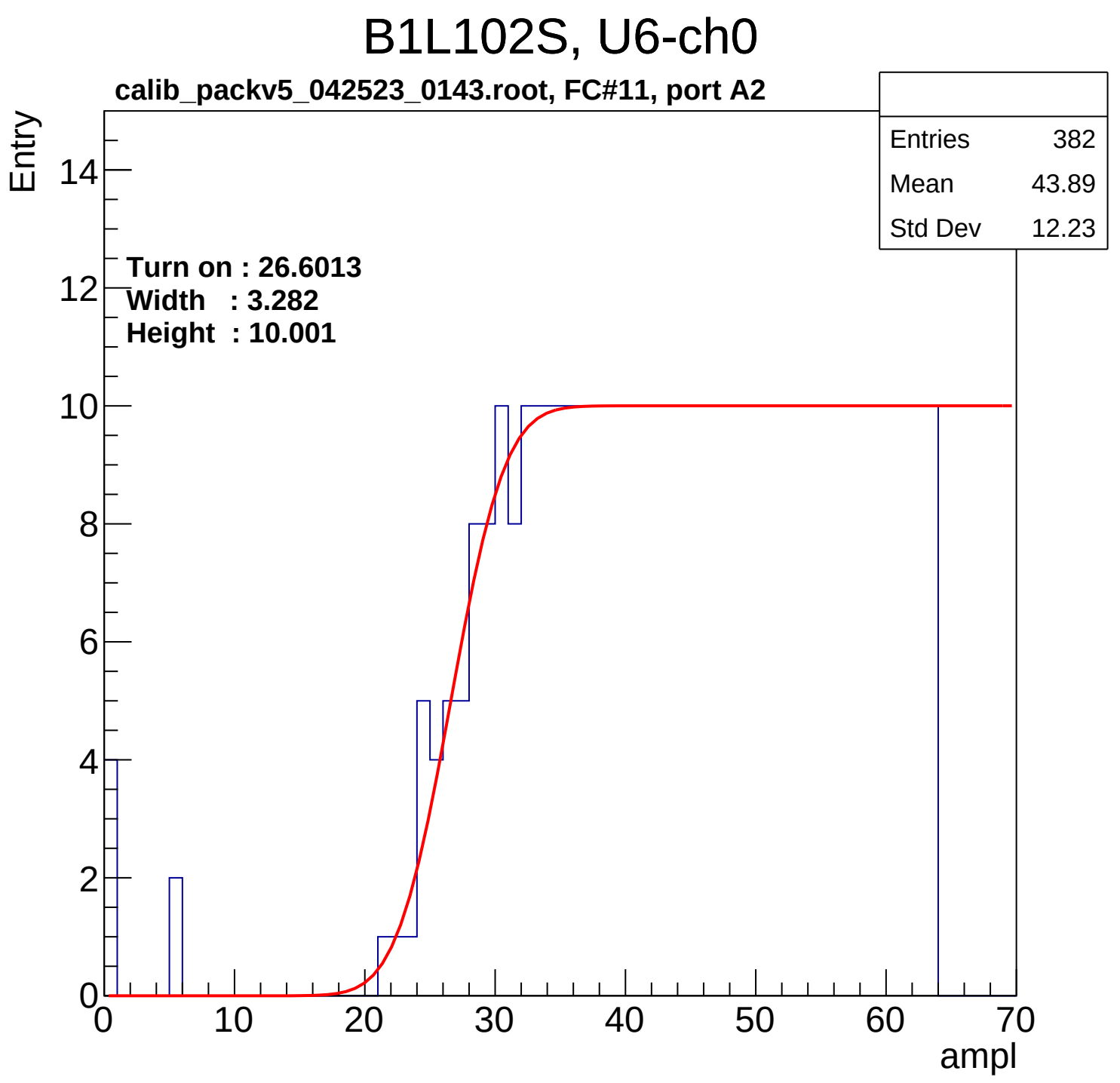
B1L102S, U6-ch0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 43.89
Std Dev 12.23
Turn on : 26.6013
Width : 3.282
Height : 10.001
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ampl
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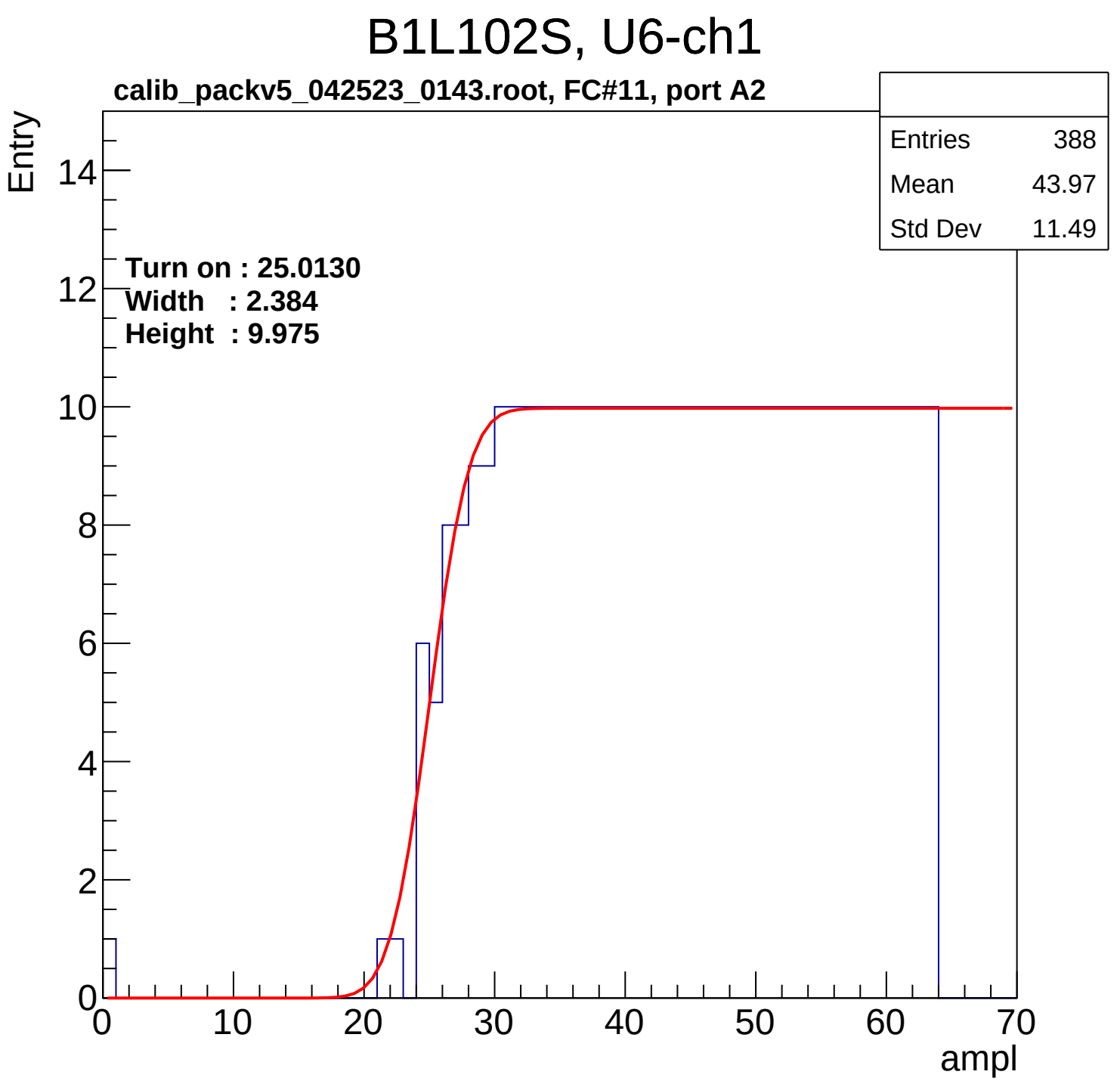
B1L102S, U6-ch1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.97
Std Dev 11.49
Turn on : 25.0130
Width : 2.384
Height : 9.975
Entry
ampl
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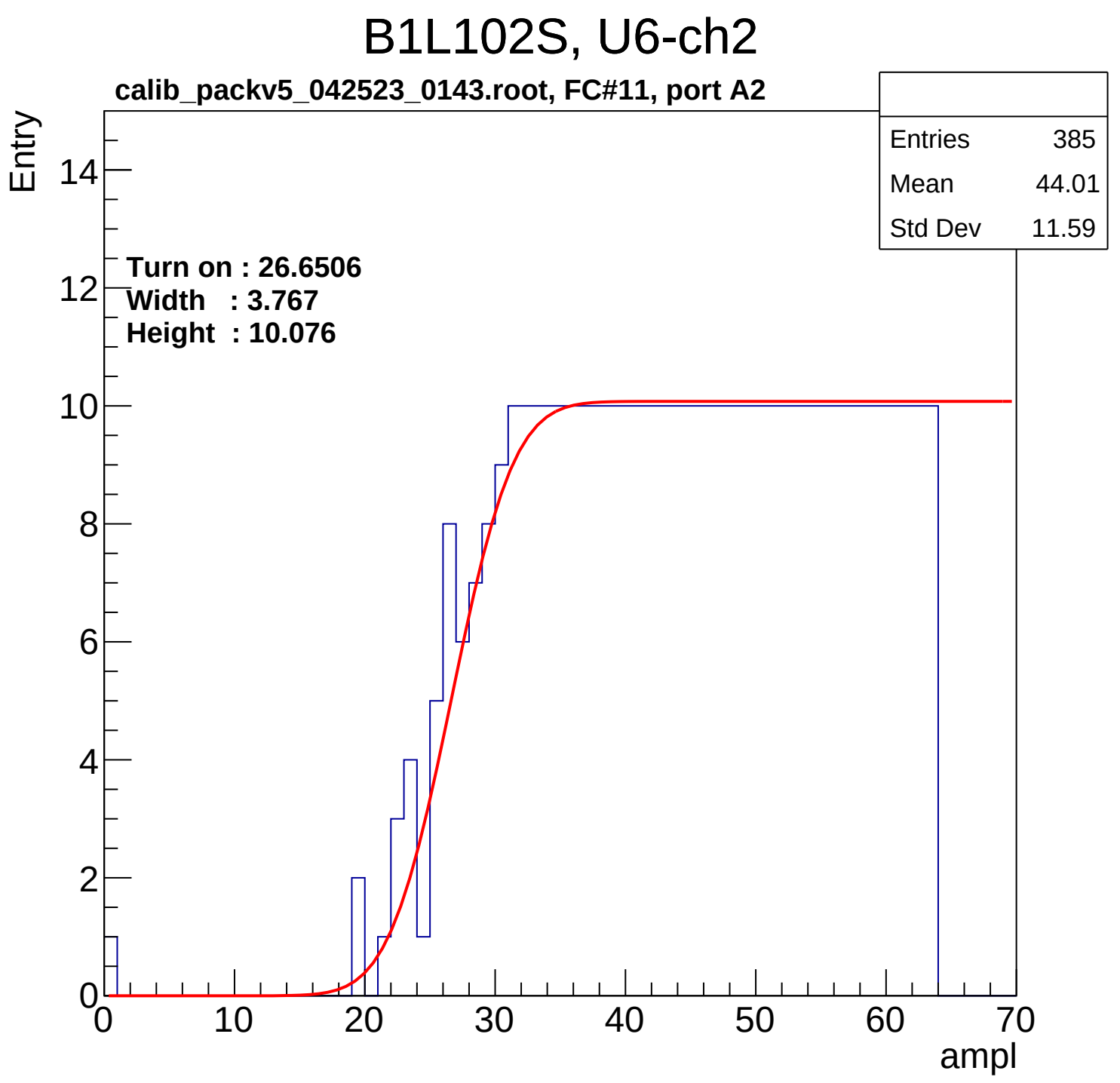
B1L102S, U6-ch2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 44.01
Std Dev 11.59
Turn on : 26.6506
Width : 3.767
Height : 10.076
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ampl
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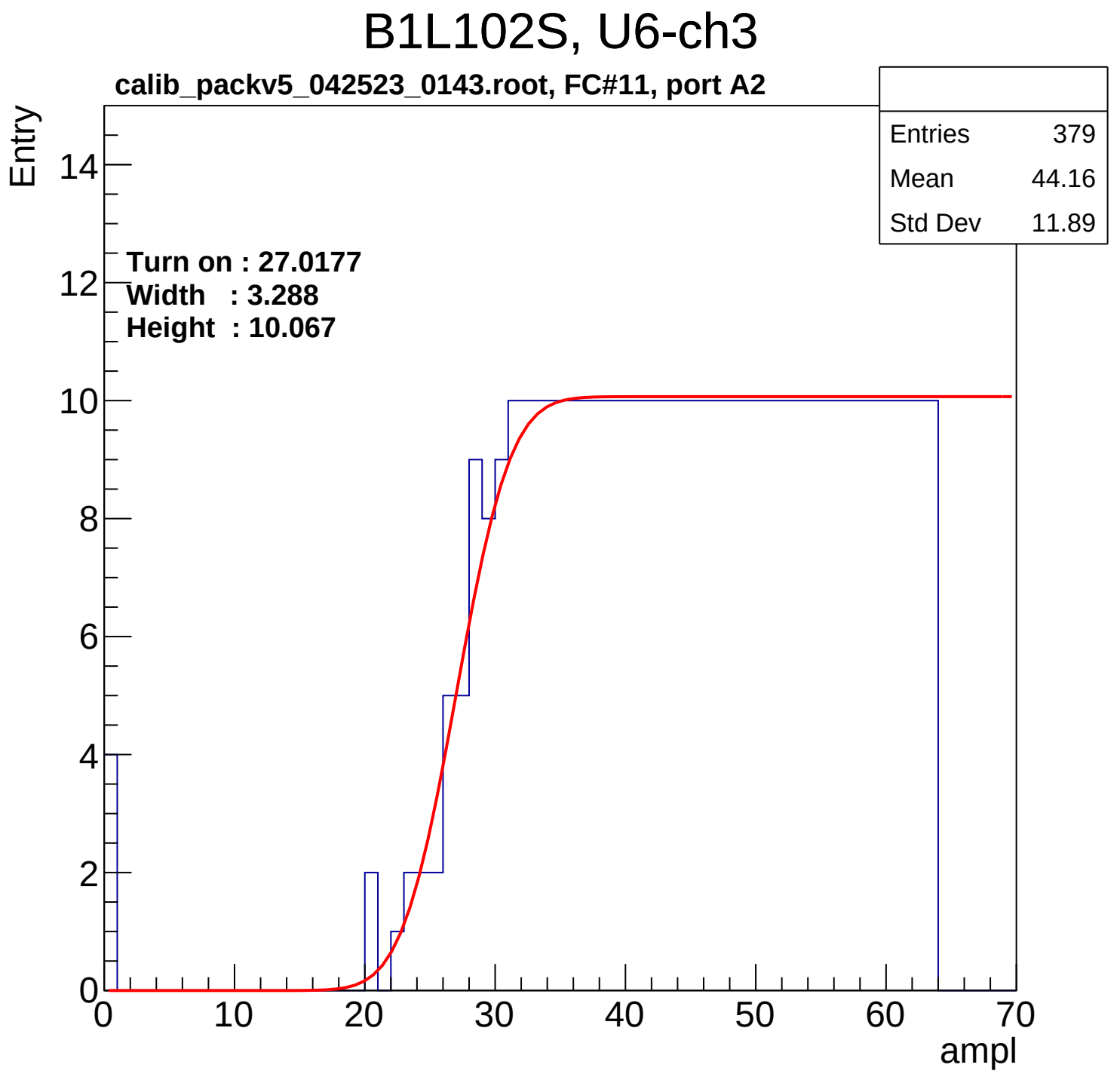
B1L102S, U6-ch3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.16
Std Dev 11.89
Turn on : 27.0177
Width : 3.288
Height : 10.067
Entry
ampl
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4
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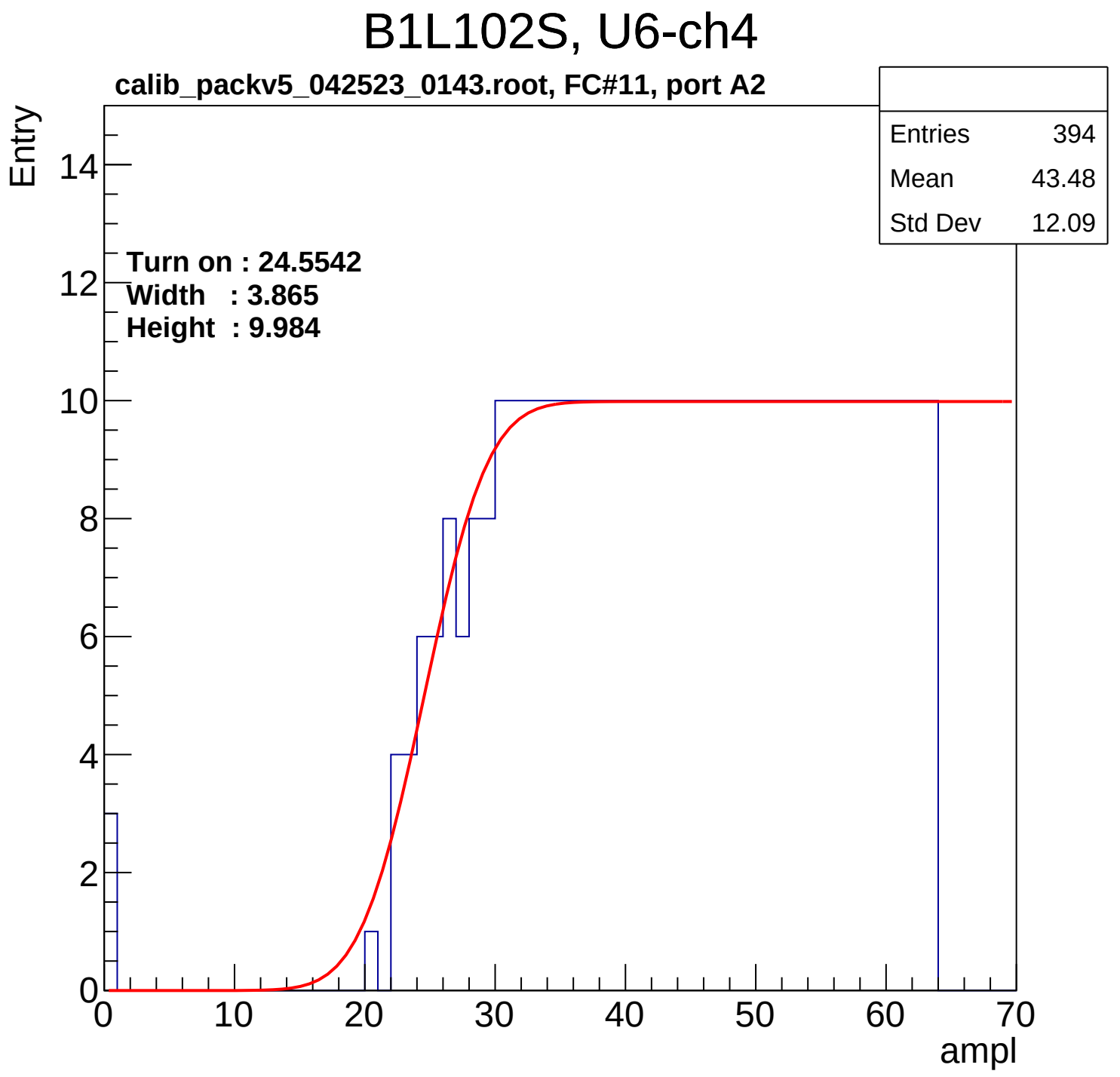
B1L102S, U6-ch4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 394
Mean 43.48
Std Dev 12.09
Turn on : 24.5542
Width : 3.865
Height : 9.984
Entry
ampl
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2
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6
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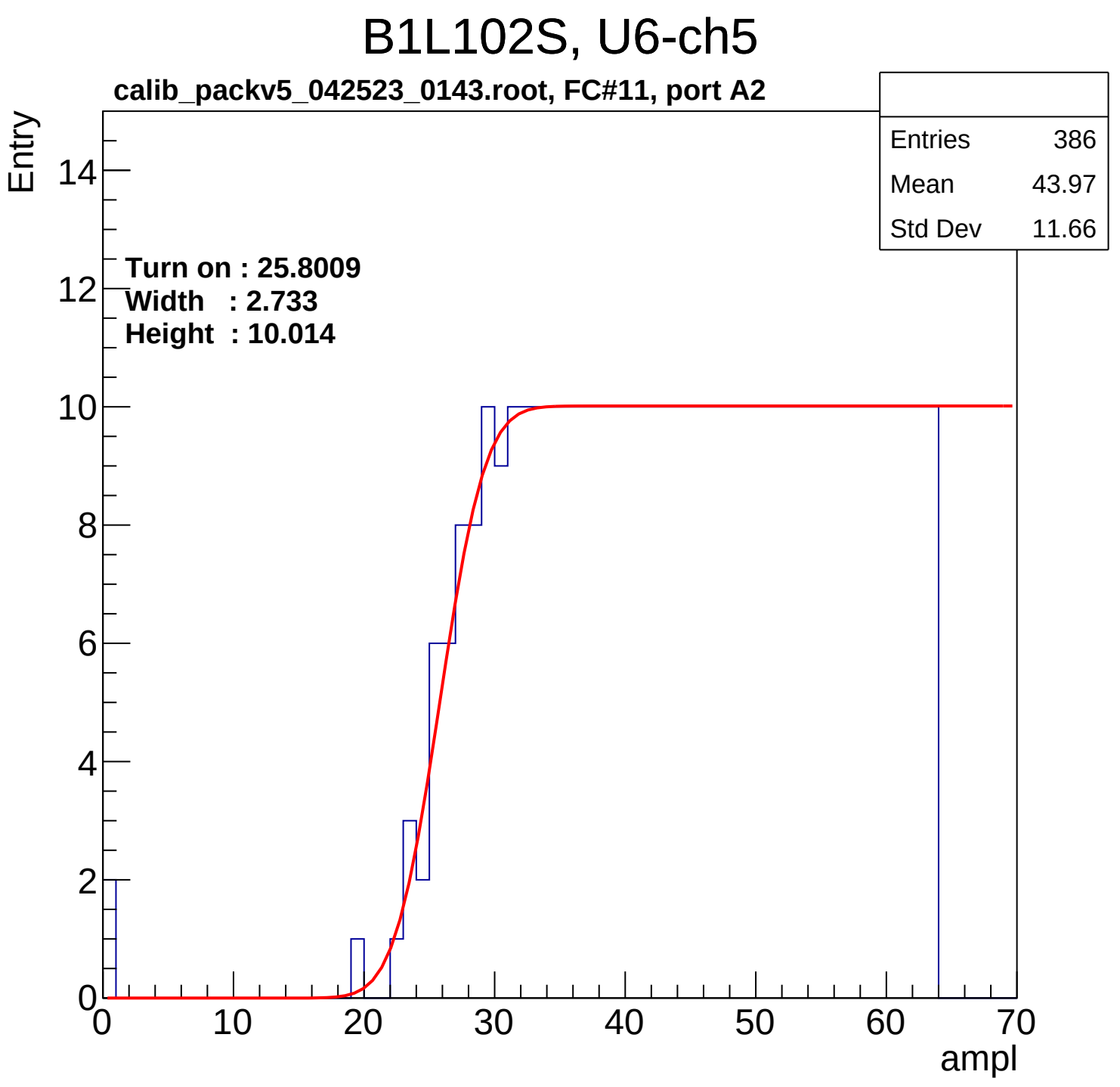
B1L102S, U6-ch5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.97
Std Dev 11.66
Turn on : 25.8009
Width : 2.733
Height : 10.014
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ampl
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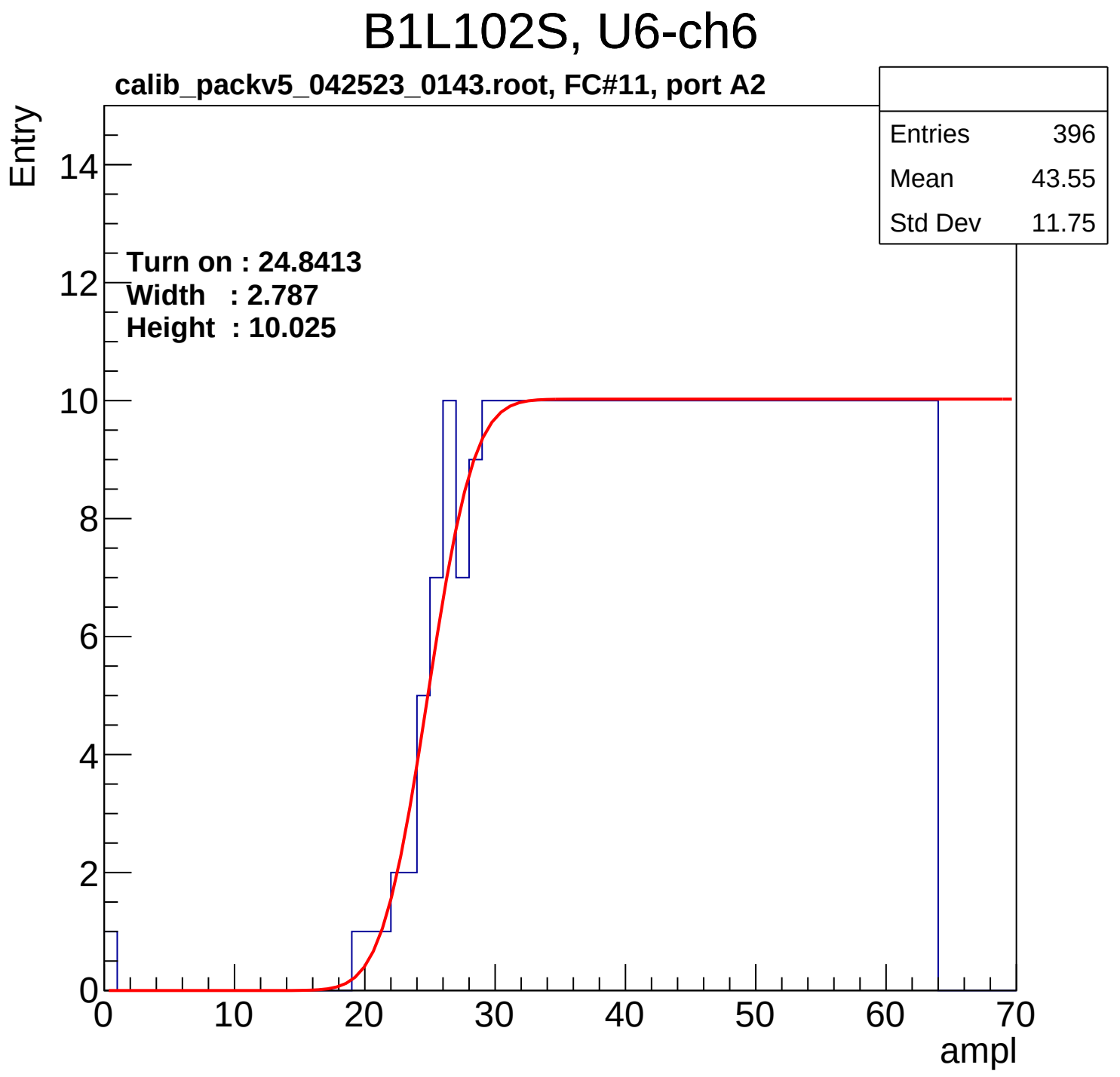
B1L102S, U6-ch6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.55
Std Dev 11.75
Turn on : 24.8413
Width : 2.787
Height : 10.025
Entry
ampl
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4
6
8
10
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0
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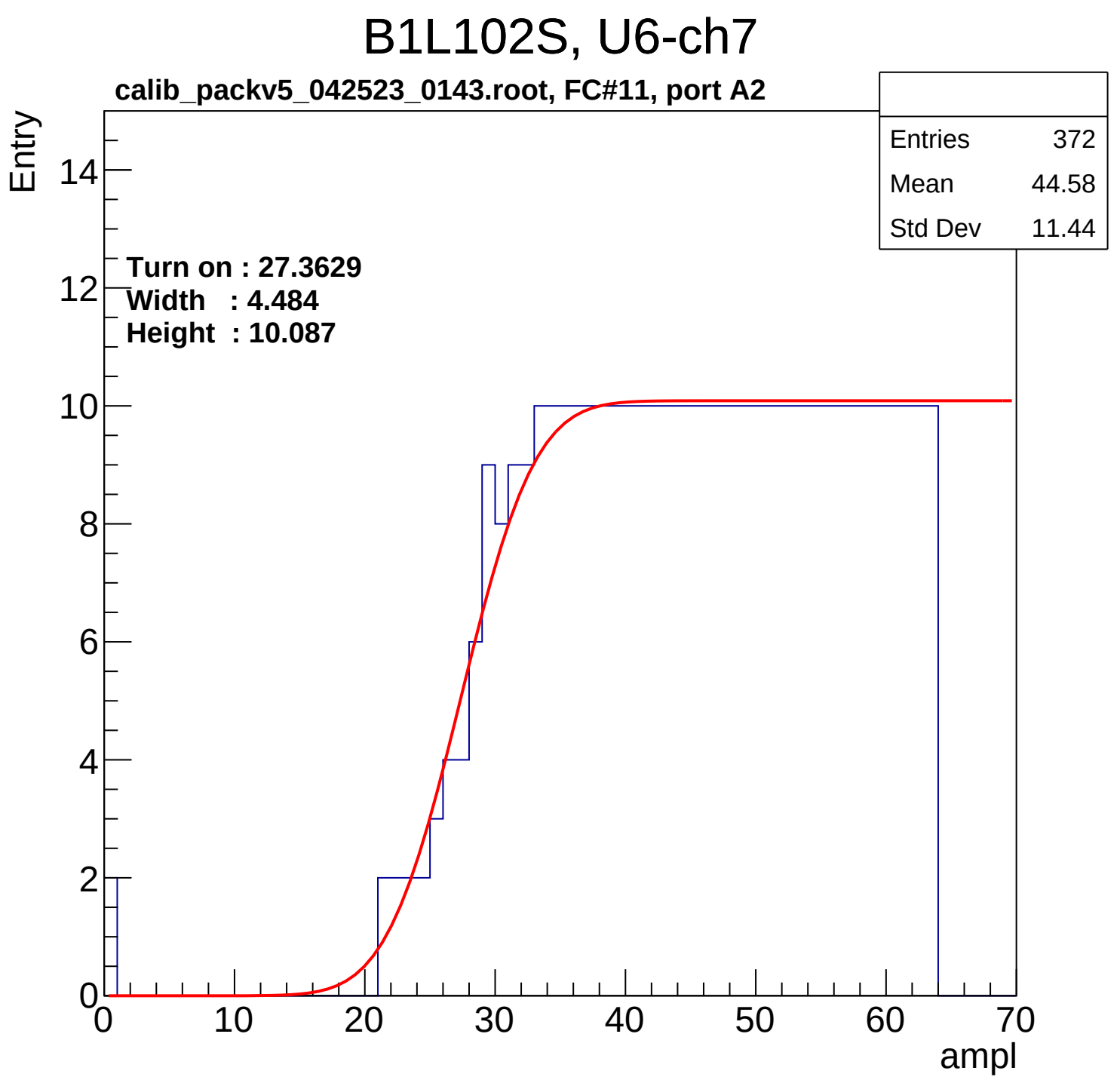
B1L102S, U6-ch7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 372
Mean 44.58
Std Dev 11.44
Turn on : 27.3629
Width : 4.484
Height : 10.087
Entry
ampl
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2
4
6
8
10
12
14
0
10
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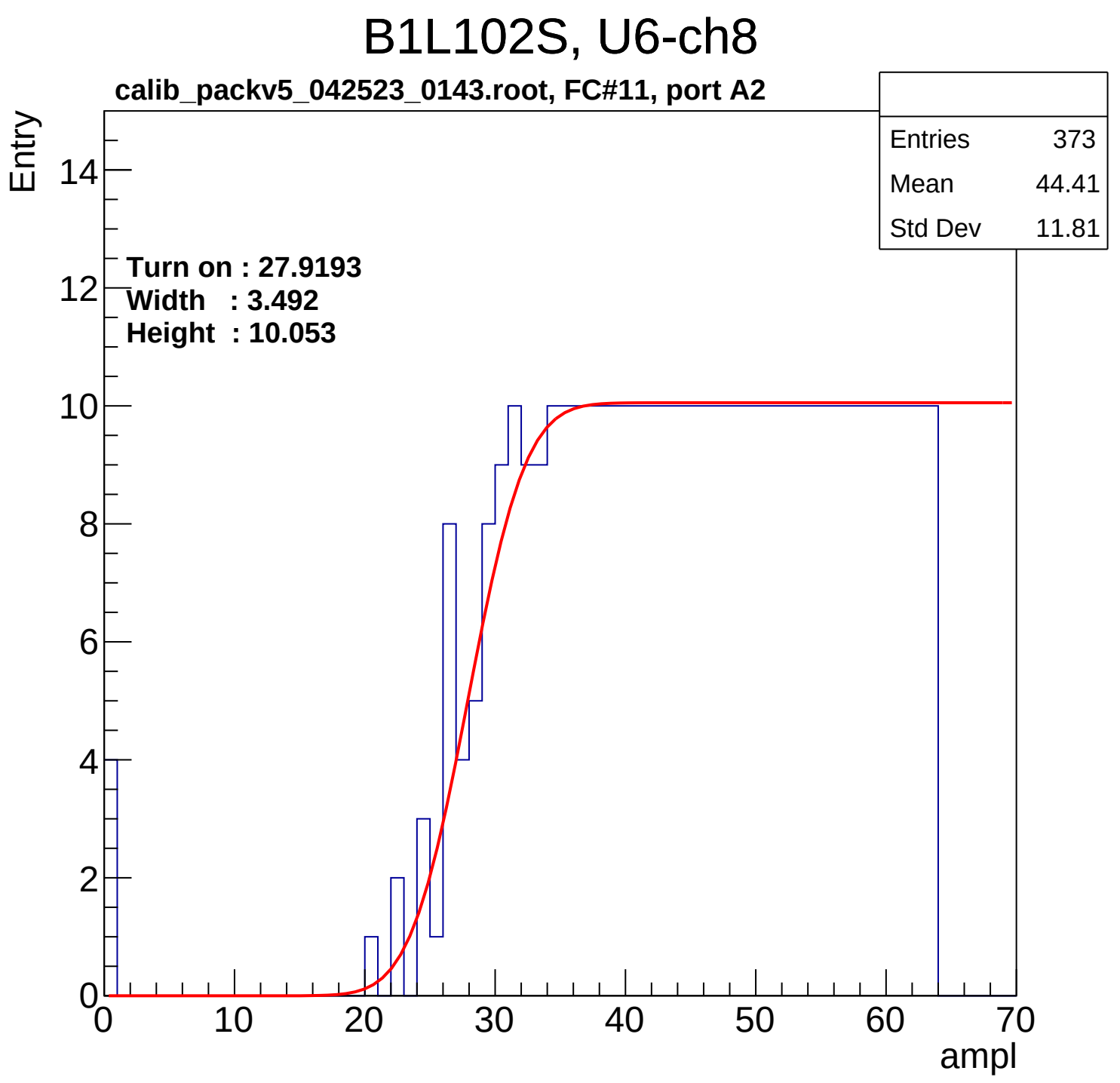
B1L102S, U6-ch8
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.41
Std Dev 11.81
Turn on : 27.9193
Width : 3.492
Height : 10.053
Entry
ampl
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6
8
10
12
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0
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60
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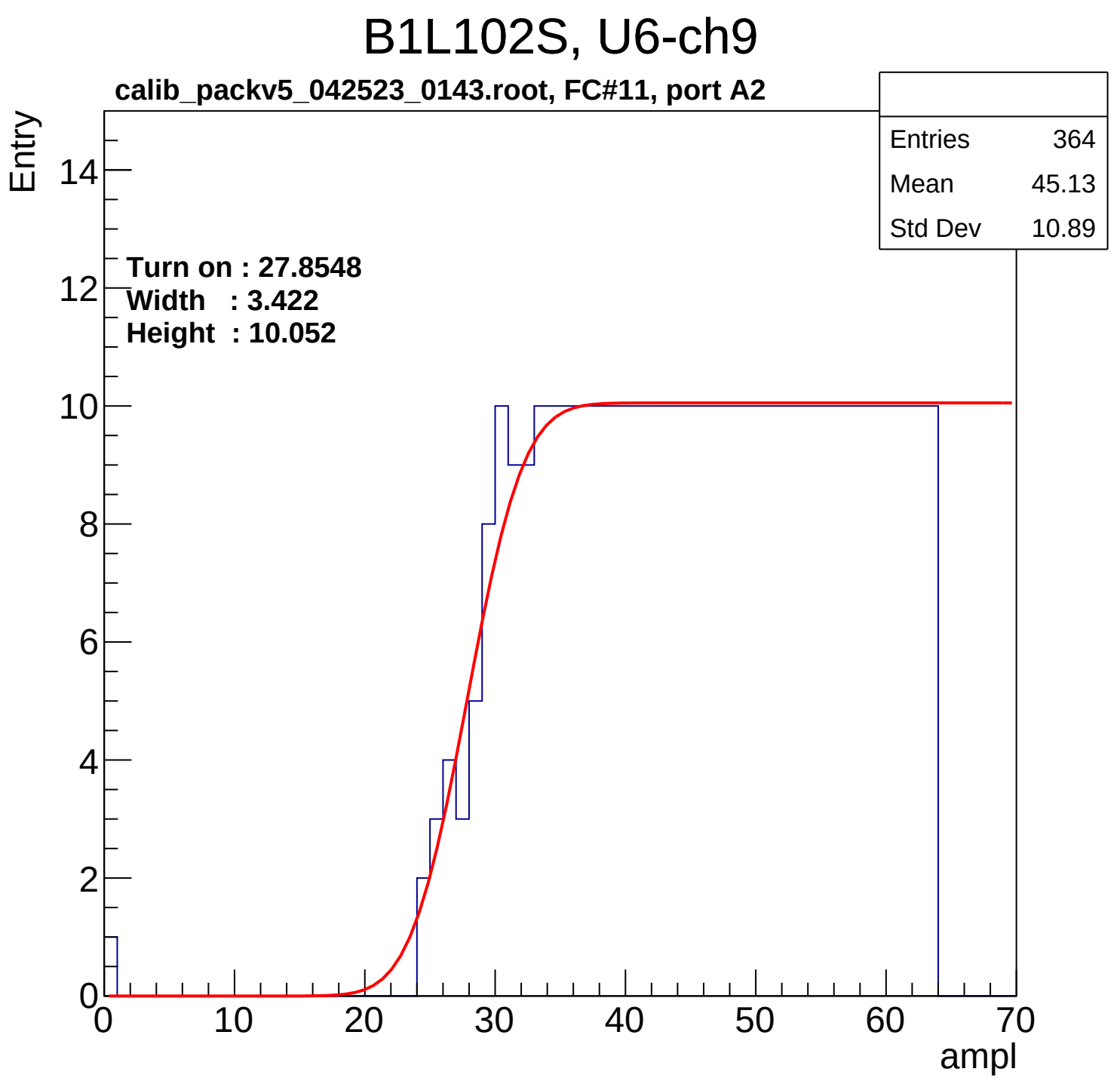
B1L102S, U6-ch9
calib_packv5_042523_0143.root, FC#11, port A2
Entries 364
Mean 45.13
Std Dev 10.89
Turn on : 27.8548
Width : 3.422
Height : 10.052
Entry
ampl
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6
8
10
12
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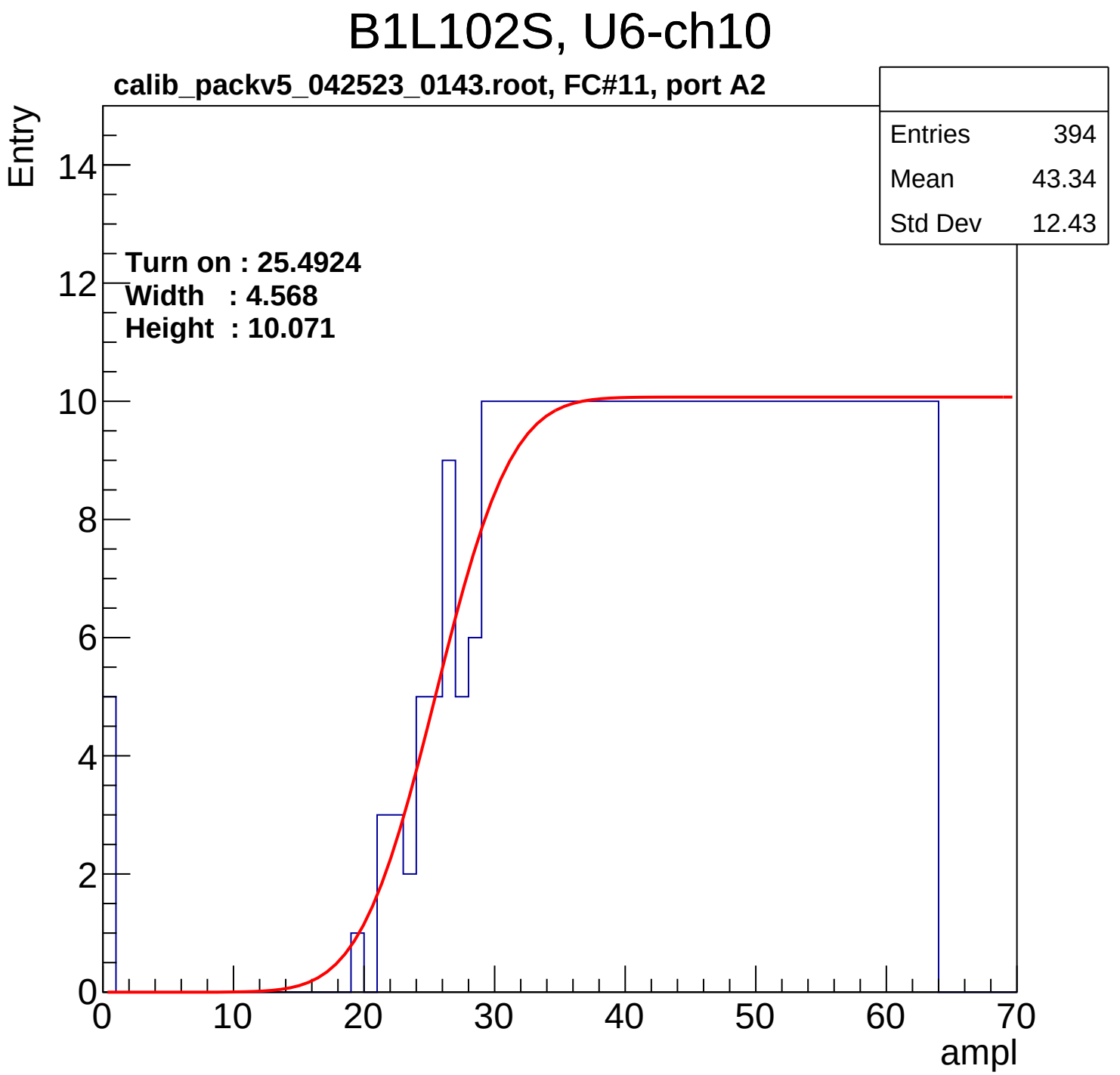
B1L102S, U6-ch10
calib_packv5_042523_0143.root, FC#11, port A2
Entries 394
Mean 43.34
Std Dev 12.43
Turn on : 25.4924
Width : 4.568
Height : 10.071
Entry
ampl
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4
6
8
10
12
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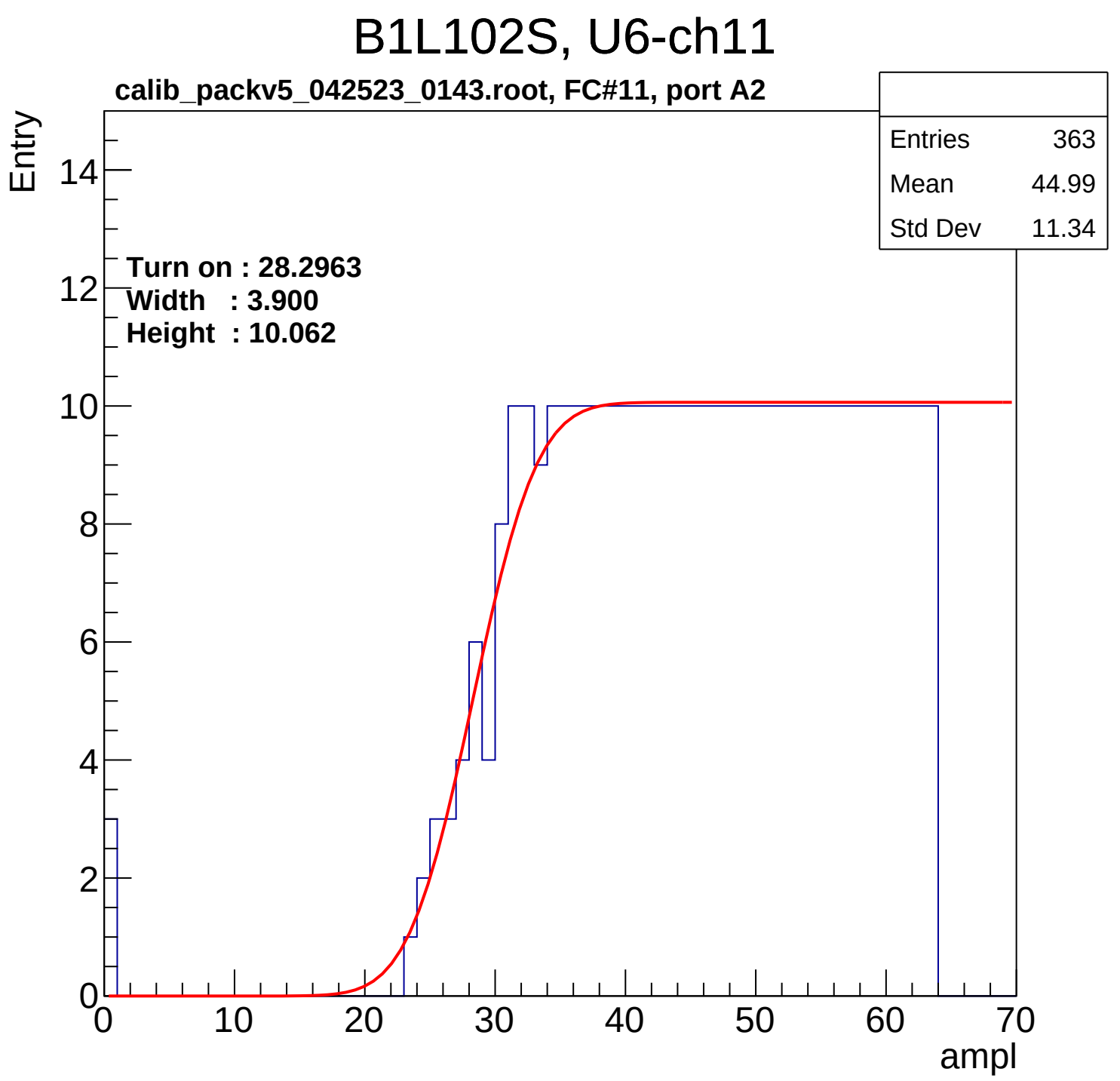
B1L102S, U6-ch11
calib_packv5_042523_0143.root, FC#11, port A2
Entries 363
Mean 44.99
Std Dev 11.34
Turn on : 28.2963
Width : 3.900
Height : 10.062
Entry
ampl
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8
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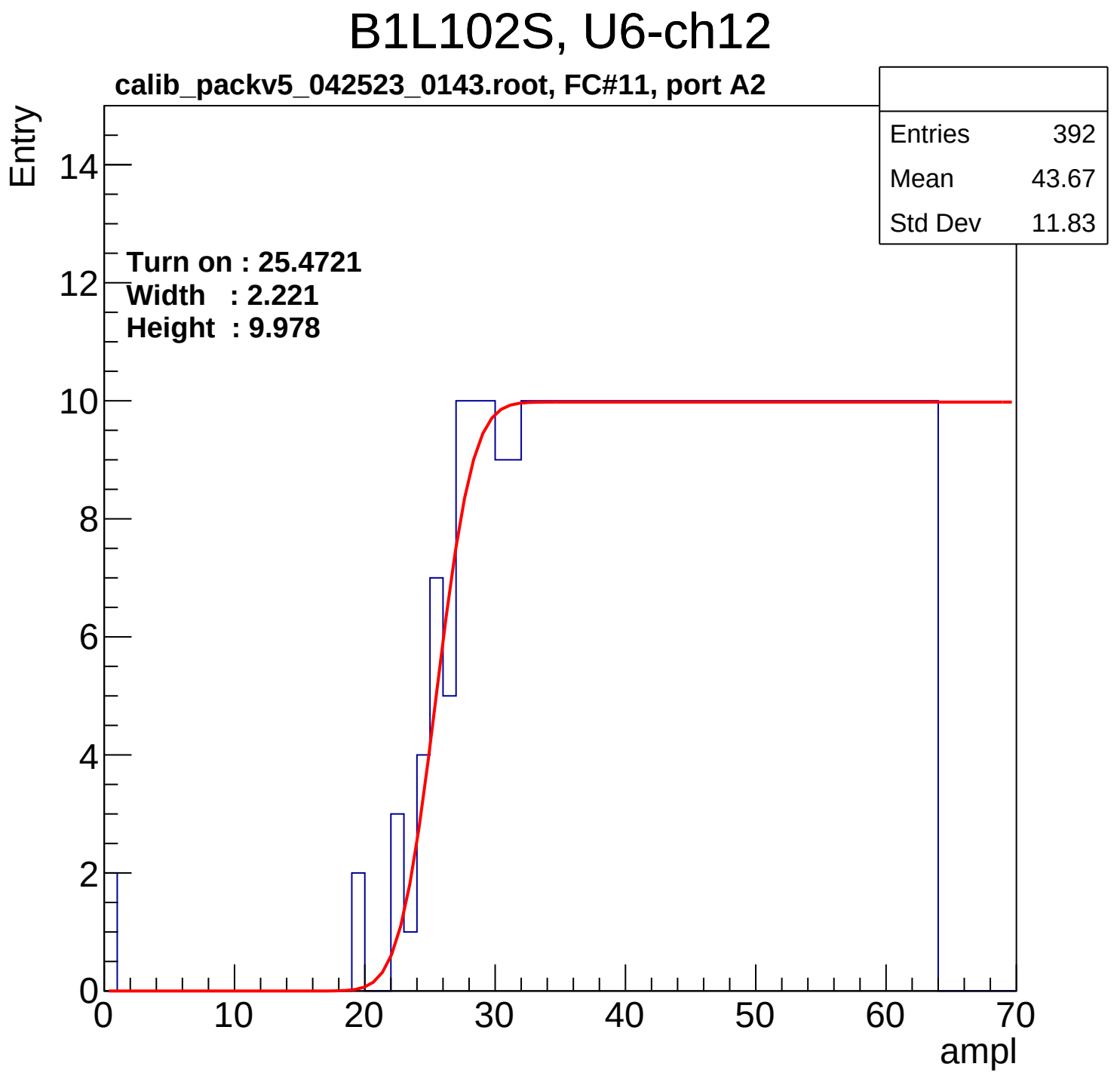
B1L102S, U6-ch12
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.67
Std Dev 11.83
Turn on : 25.4721
Width : 2.221
Height : 9.978
Entry
ampl
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2
4
6
8
10
12
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0
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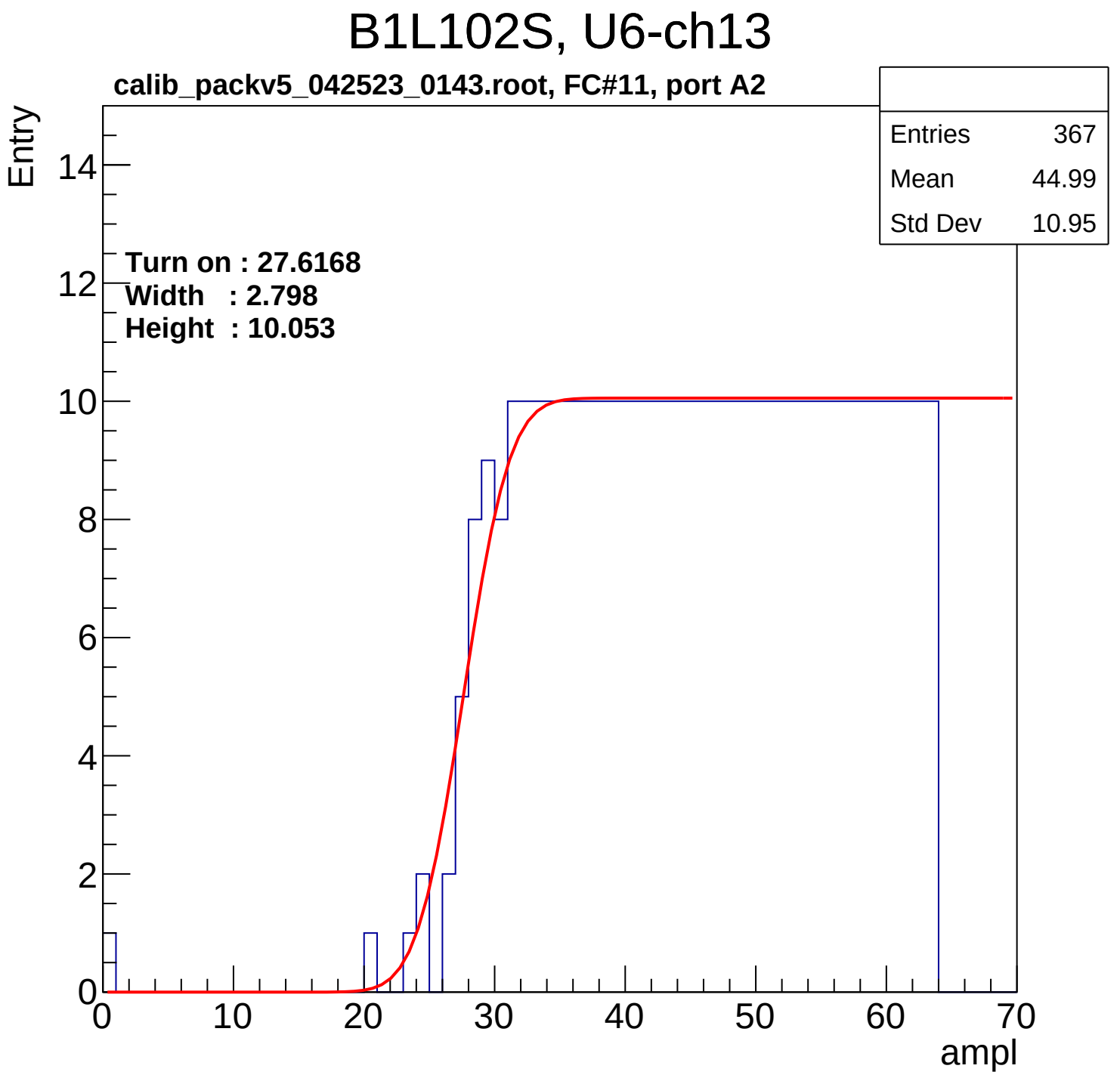
B1L102S, U6-ch13
calib_packv5_042523_0143.root, FC#11, port A2
Entries 367
Mean 44.99
Std Dev 10.95
Turn on : 27.6168
Width : 2.798
Height : 10.053
Entry
ampl
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6
8
10
12
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60
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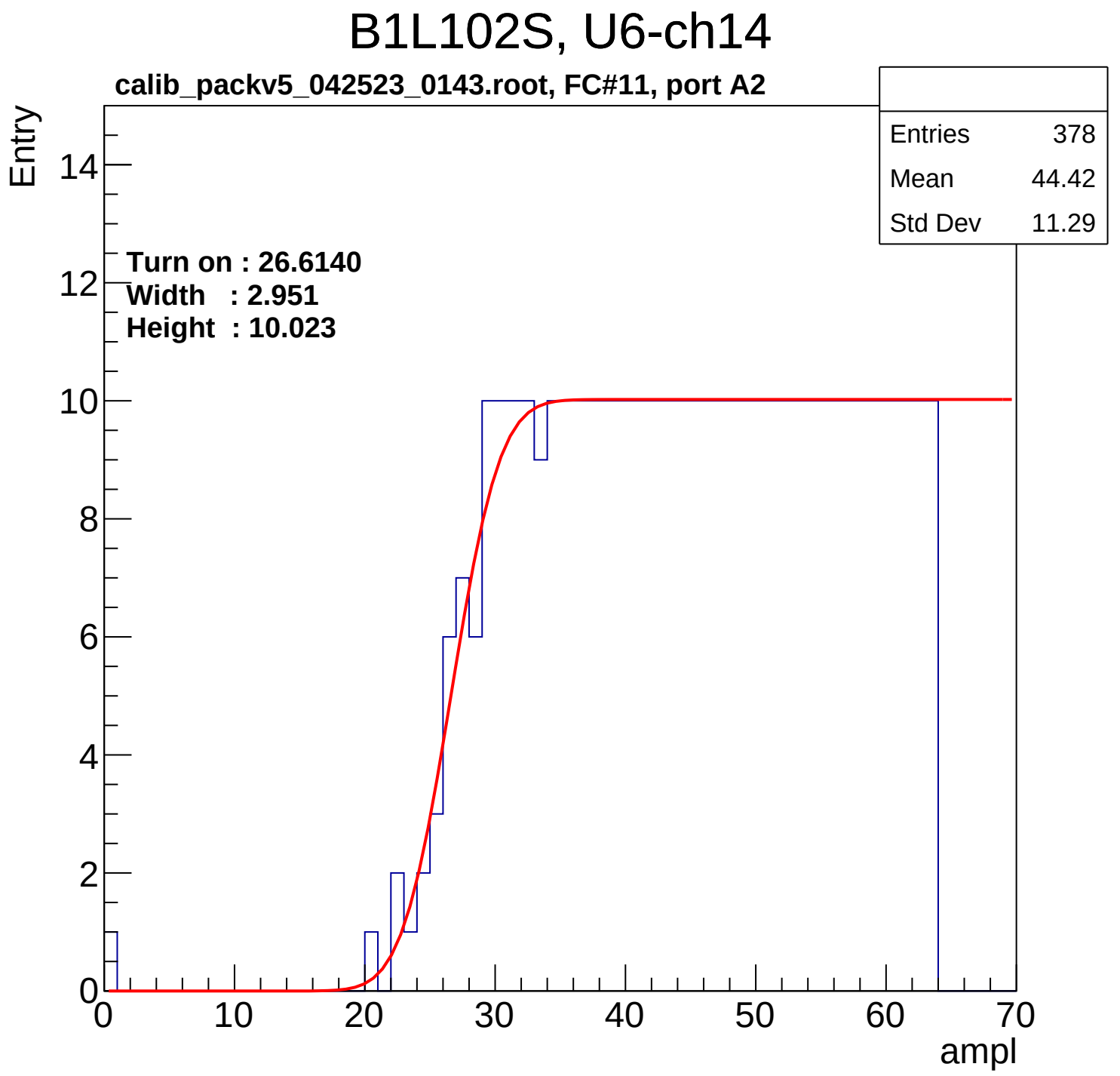
B1L102S, U6-ch14
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.42
Std Dev 11.29
Turn on : 26.6140
Width : 2.951
Height : 10.023
Entry
ampl
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6
8
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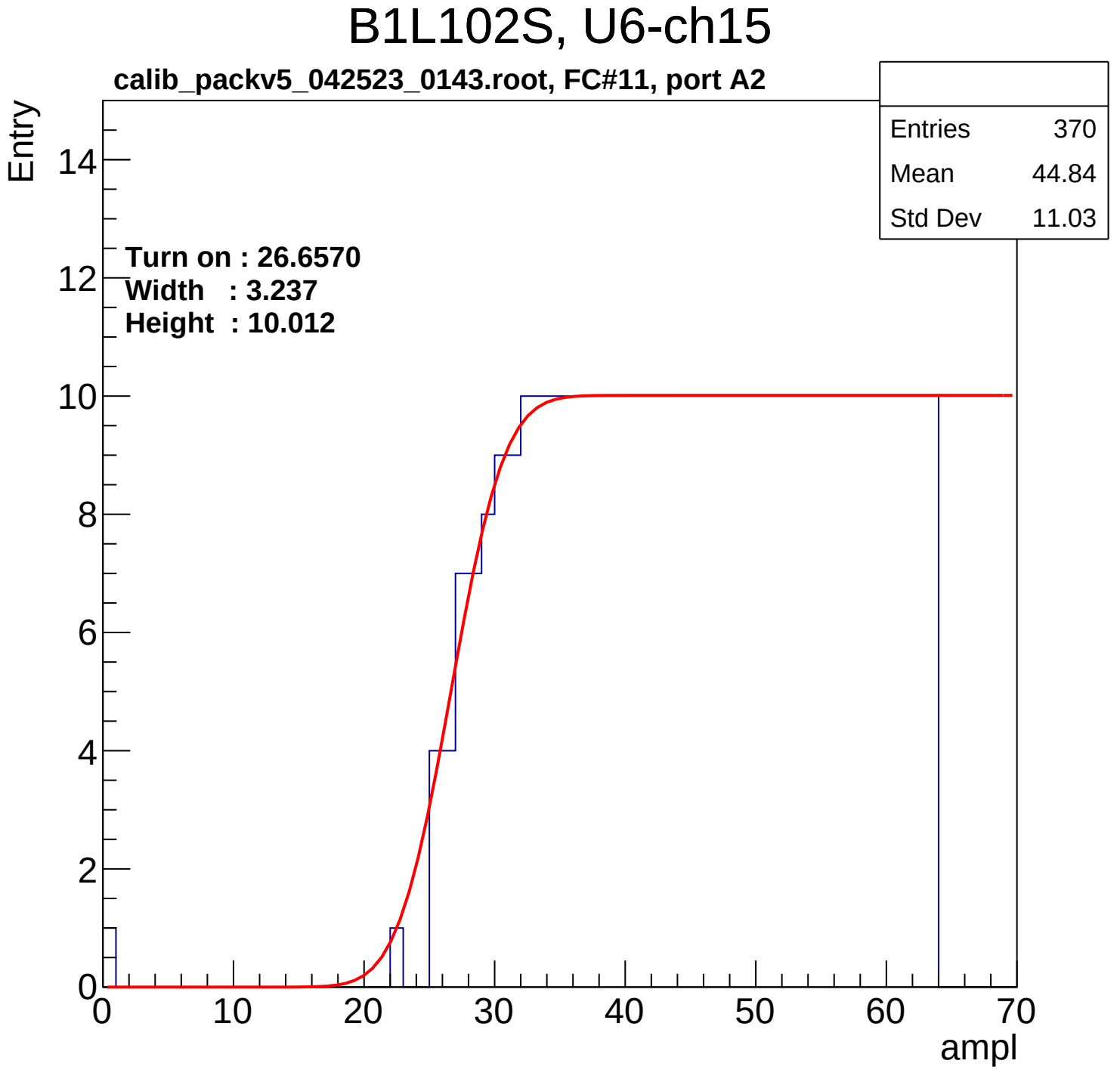
B1L102S, U6-ch15
calib_packv5_042523_0143.root, FC#11, port A2
Entries 370
Mean 44.84
Std Dev 11.03
Turn on : 26.6570
Width : 3.237
Height : 10.012
Entry
ampl
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4
6
8
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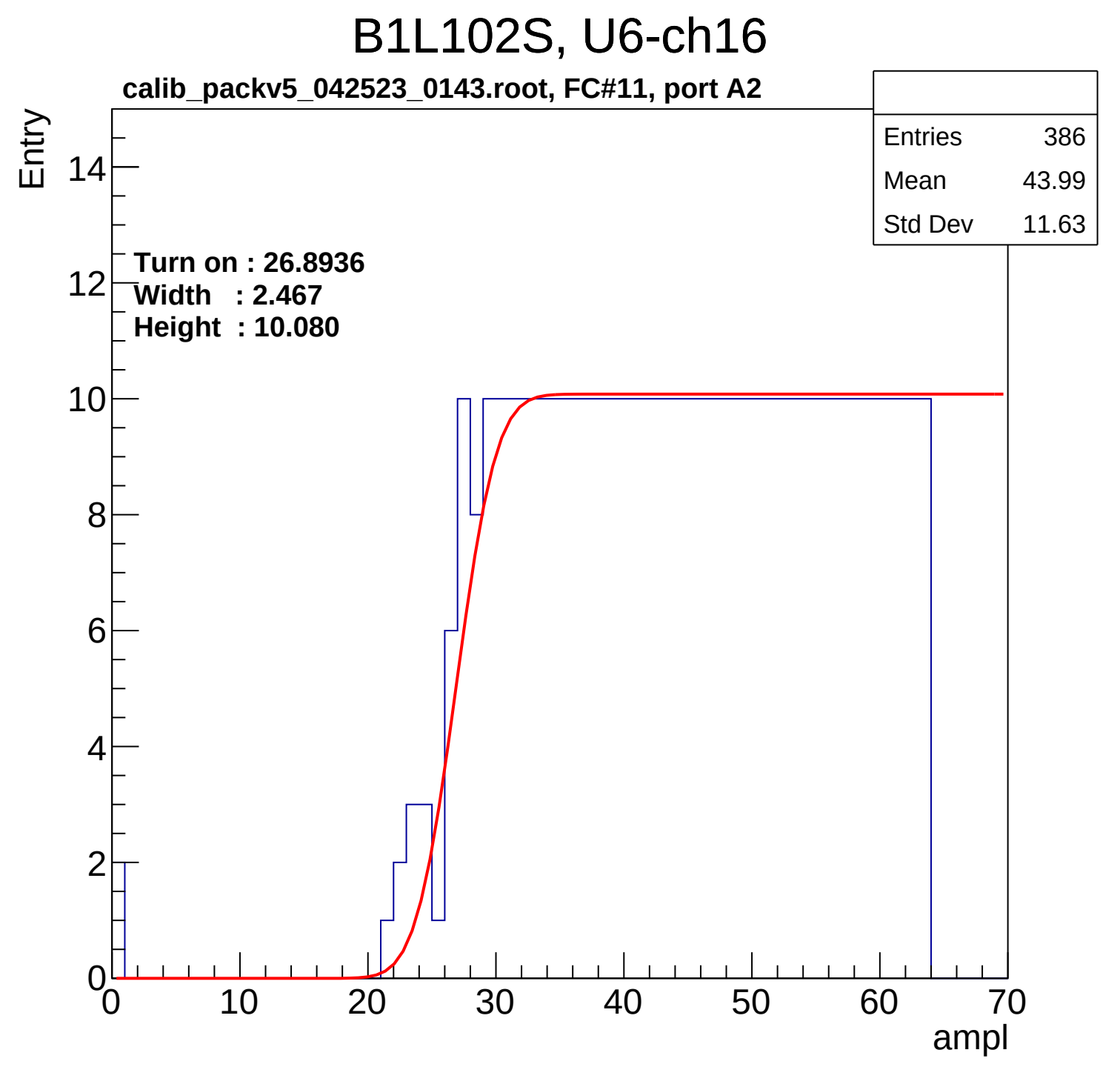
B1L102S, U6-ch16
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.99
Std Dev 11.63
Turn on : 26.8936
Width : 2.467
Height : 10.080
Entry
ampl
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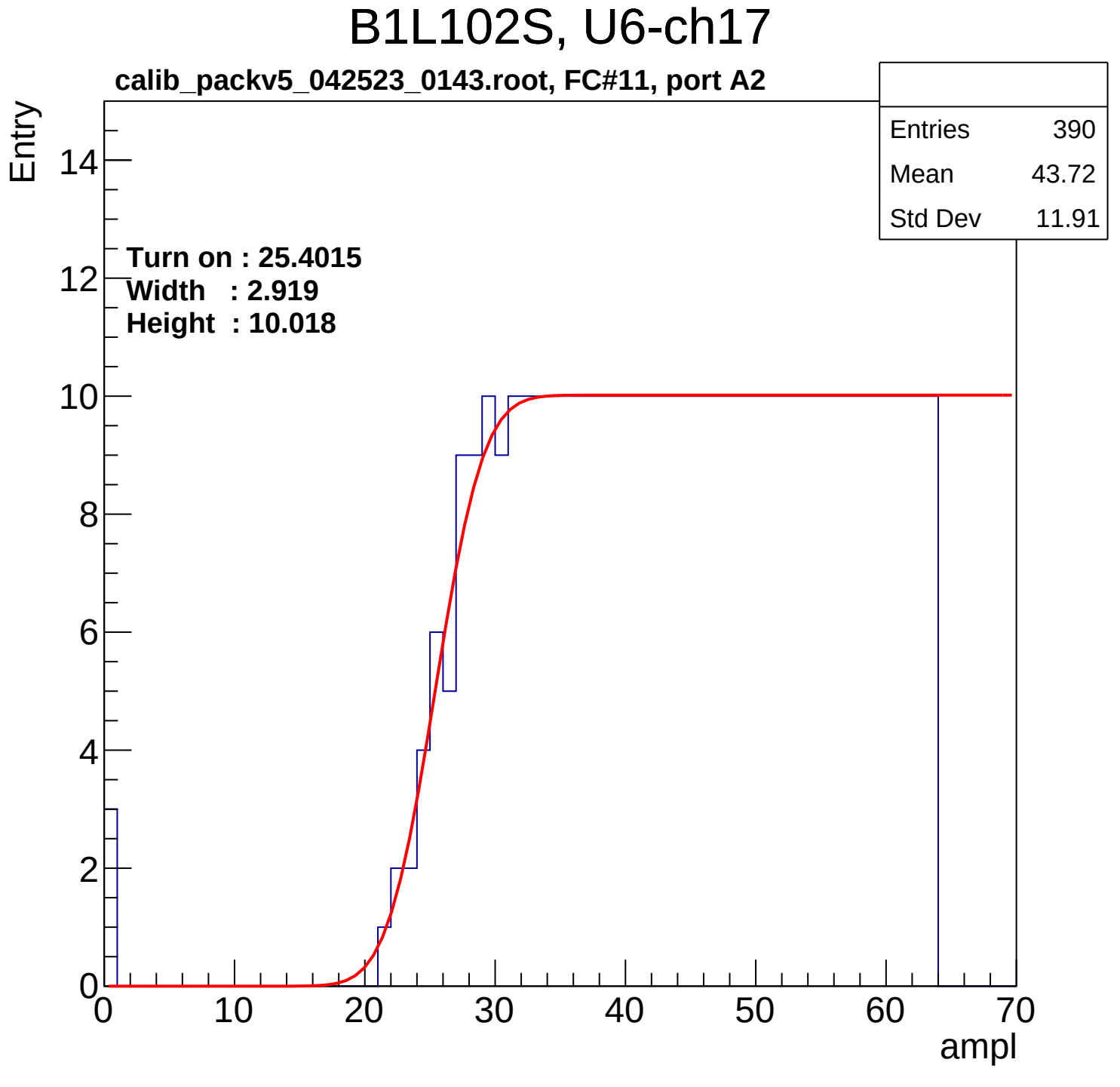
B1L102S, U6-ch17
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.72
Std Dev 11.91
Turn on : 25.4015
Width : 2.919
Height : 10.018
Entry
ampl
0
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8
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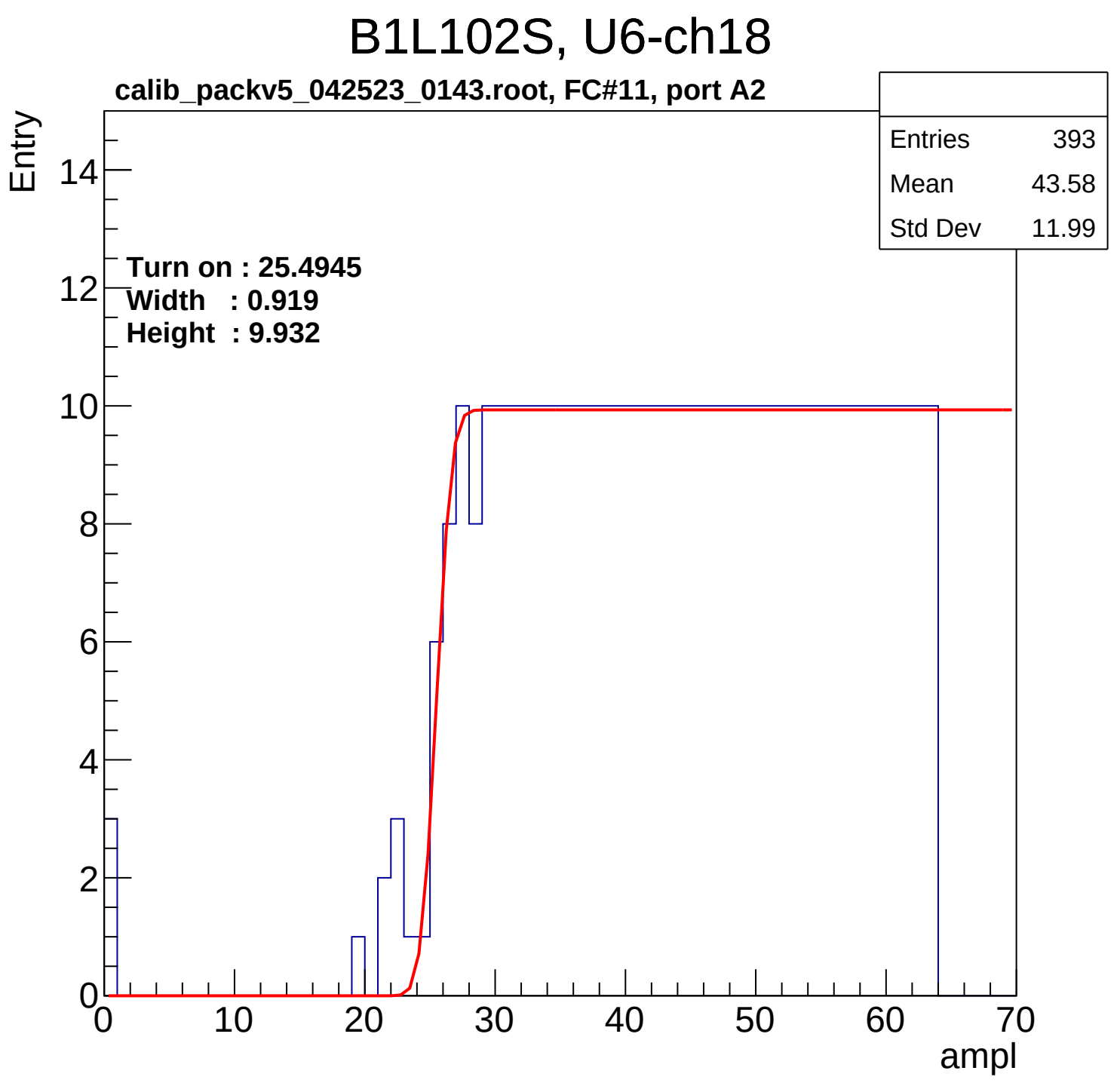
B1L102S, U6-ch18
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.58
Std Dev 11.99
Turn on : 25.4945
Width : 0.919
Height : 9.932
Entry
ampl
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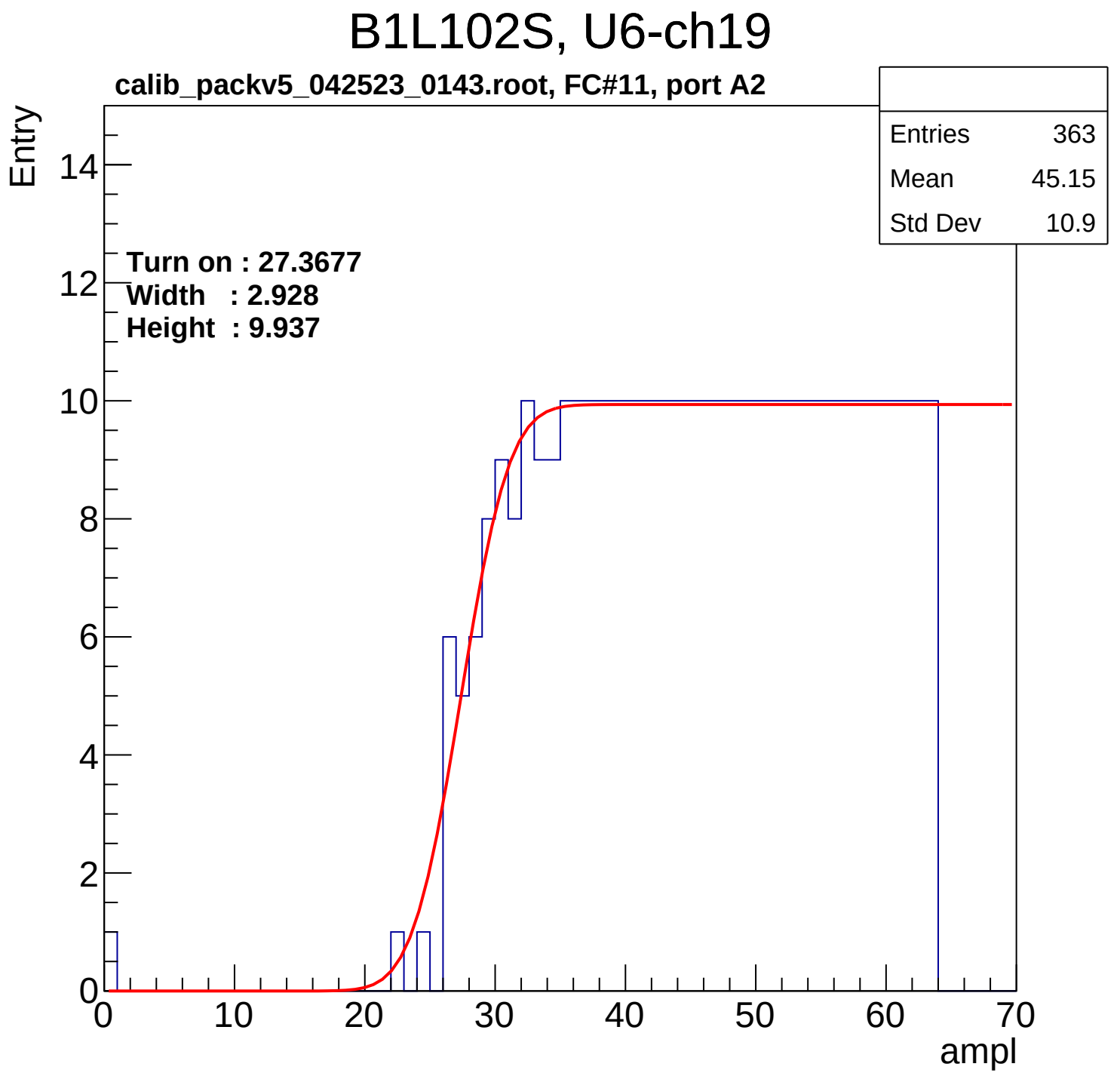
B1L102S, U6-ch19
calib_packv5_042523_0143.root, FC#11, port A2
Entries 363
Mean 45.15
Std Dev 10.9
Turn on : 27.3677
Width : 2.928
Height : 9.937
Entry
ampl
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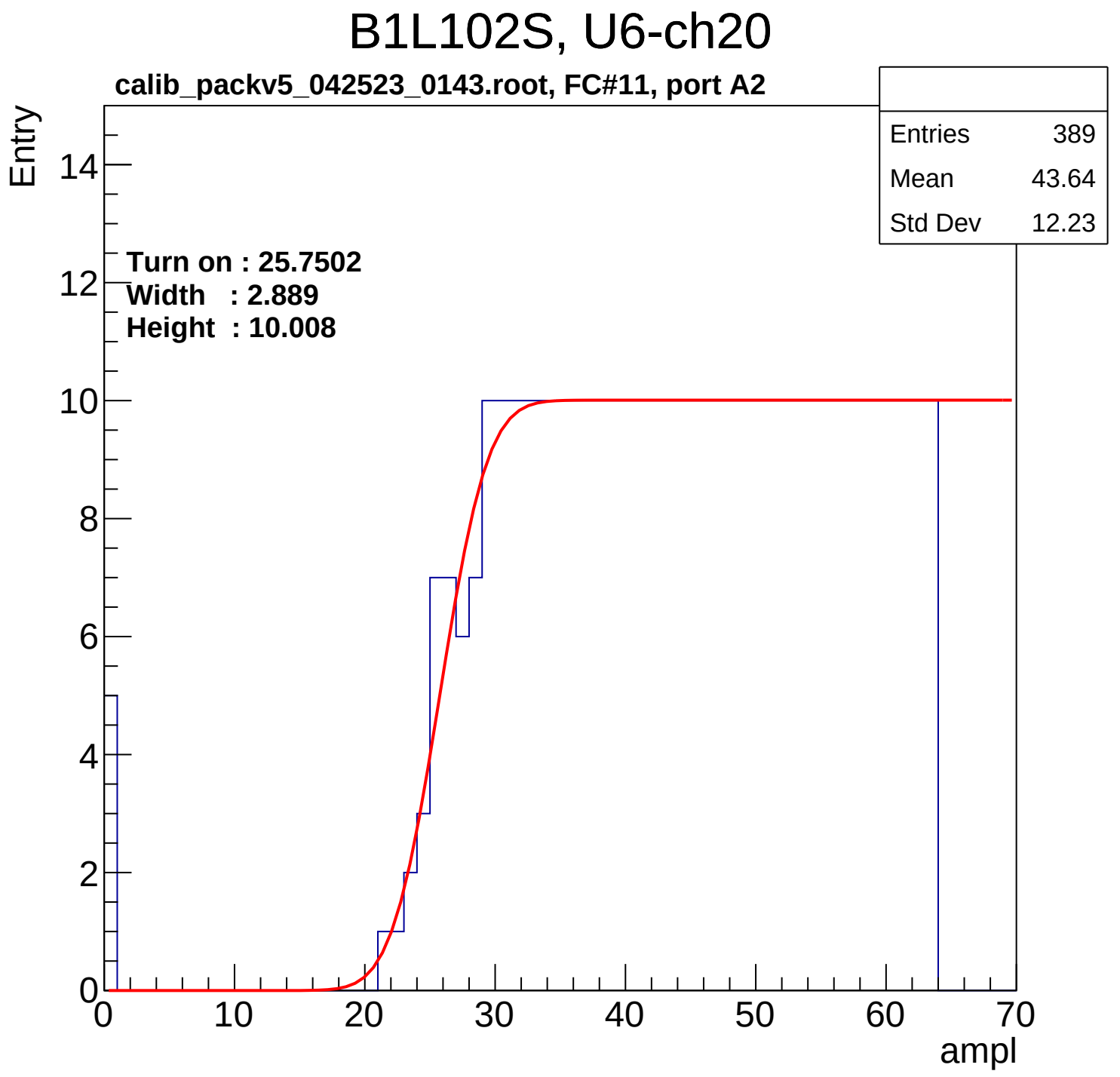
B1L102S, U6-ch20
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.64
Std Dev 12.23
Turn on : 25.7502
Width : 2.889
Height : 10.008
Entry
ampl
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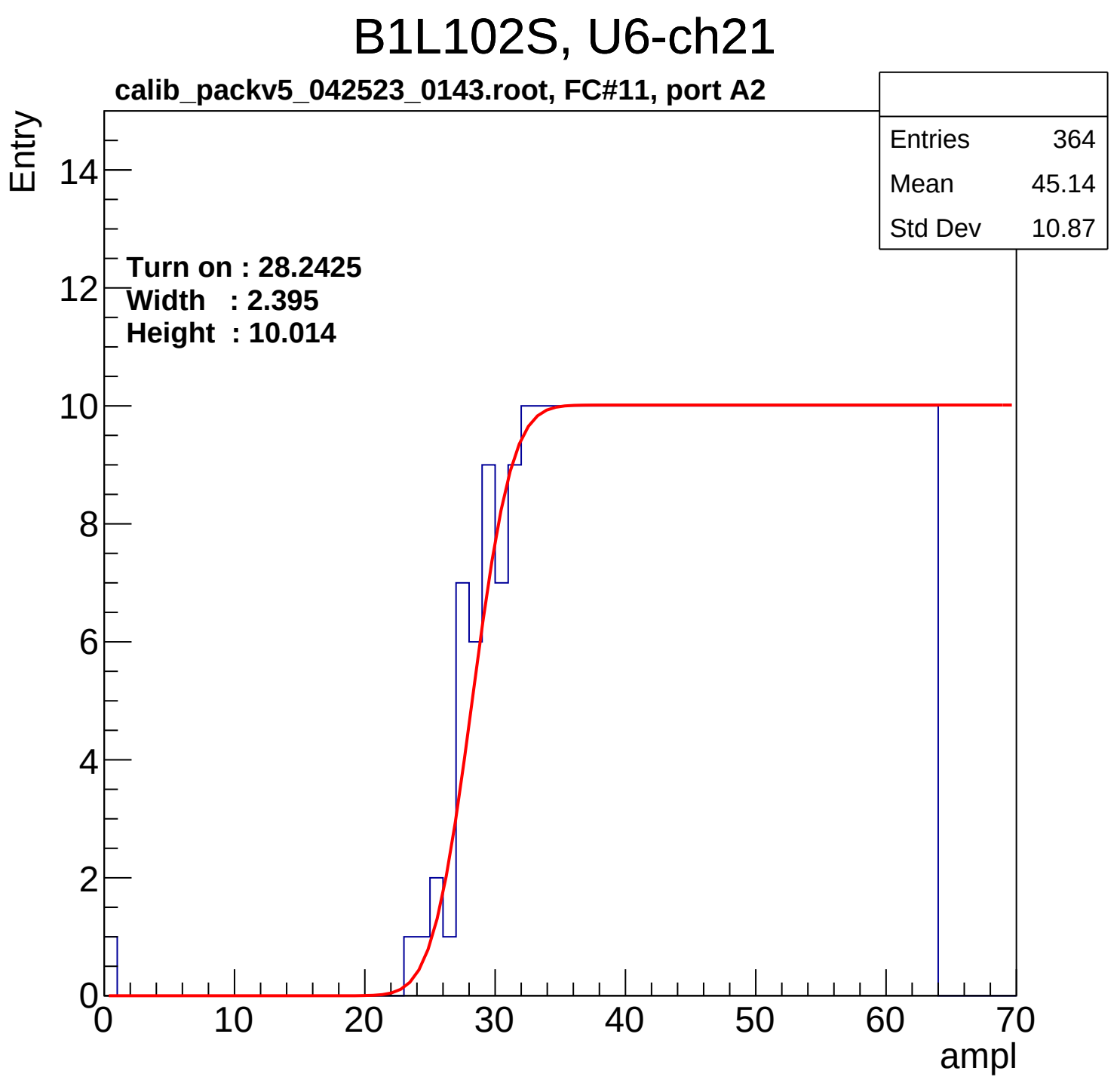
B1L102S, U6-ch21
calib_packv5_042523_0143.root, FC#11, port A2
Entries 364
Mean 45.14
Std Dev 10.87
Turn on : 28.2425
Width : 2.395
Height : 10.014
Entry
ampl
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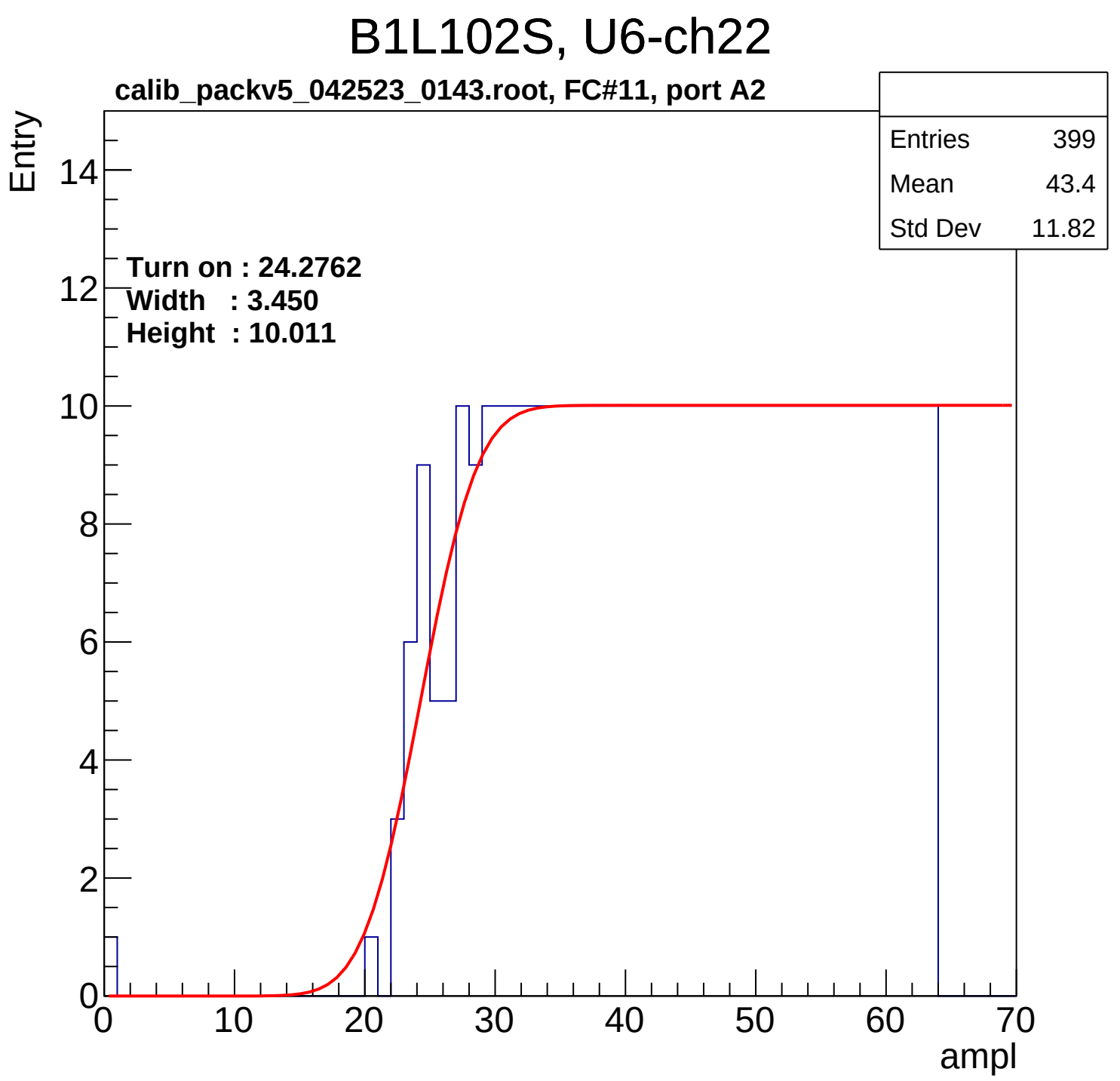
B1L102S, U6-ch22
calib_packv5_042523_0143.root, FC#11, port A2
Entries 399
Mean 43.4
Std Dev 11.82
Turn on : 24.2762
Width : 3.450
Height : 10.011
Entry
ampl
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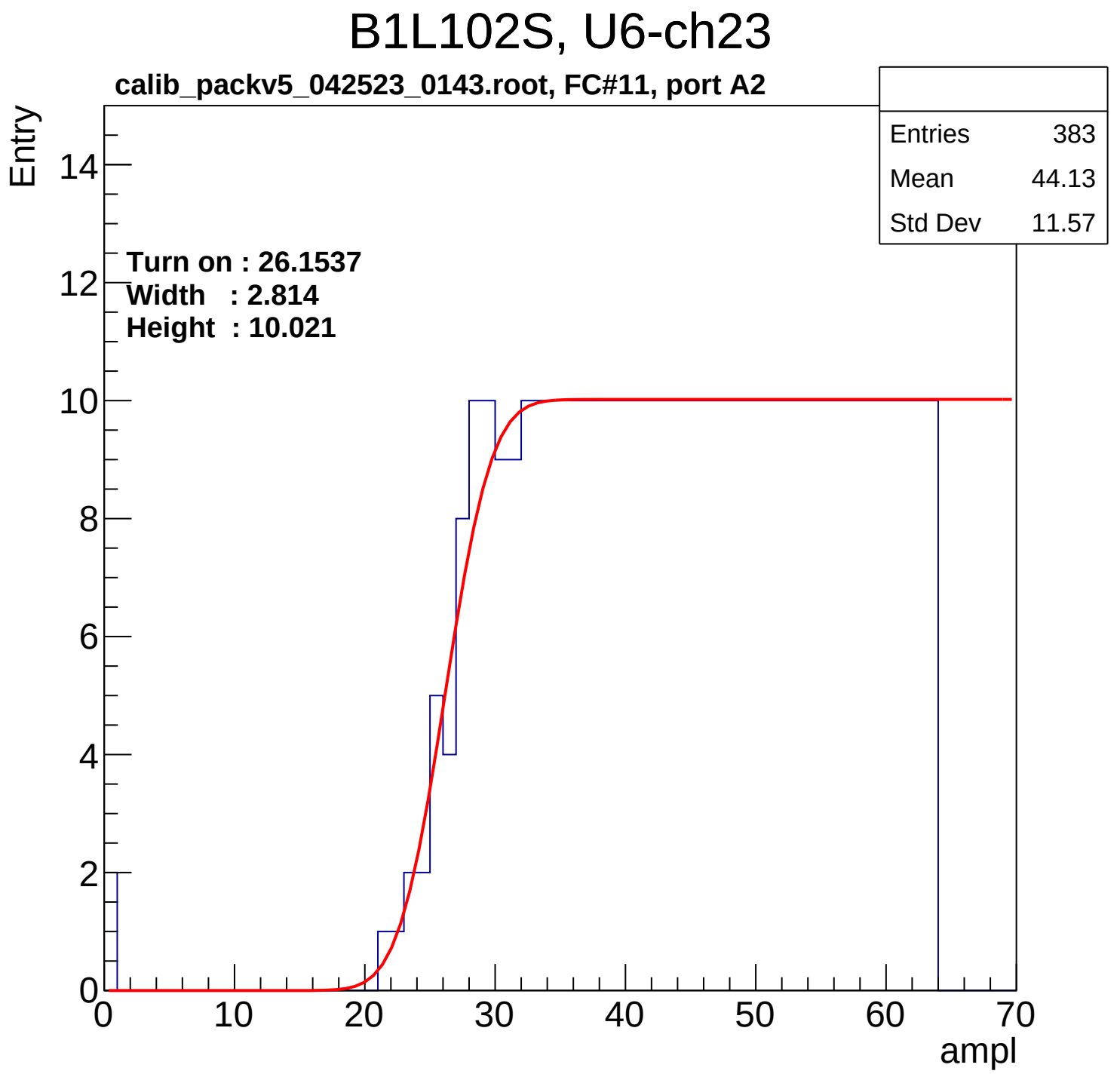
B1L102S, U6-ch23
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.13
Std Dev 11.57
Turn on : 26.1537
Width : 2.814
Height : 10.021
Entry
ampl
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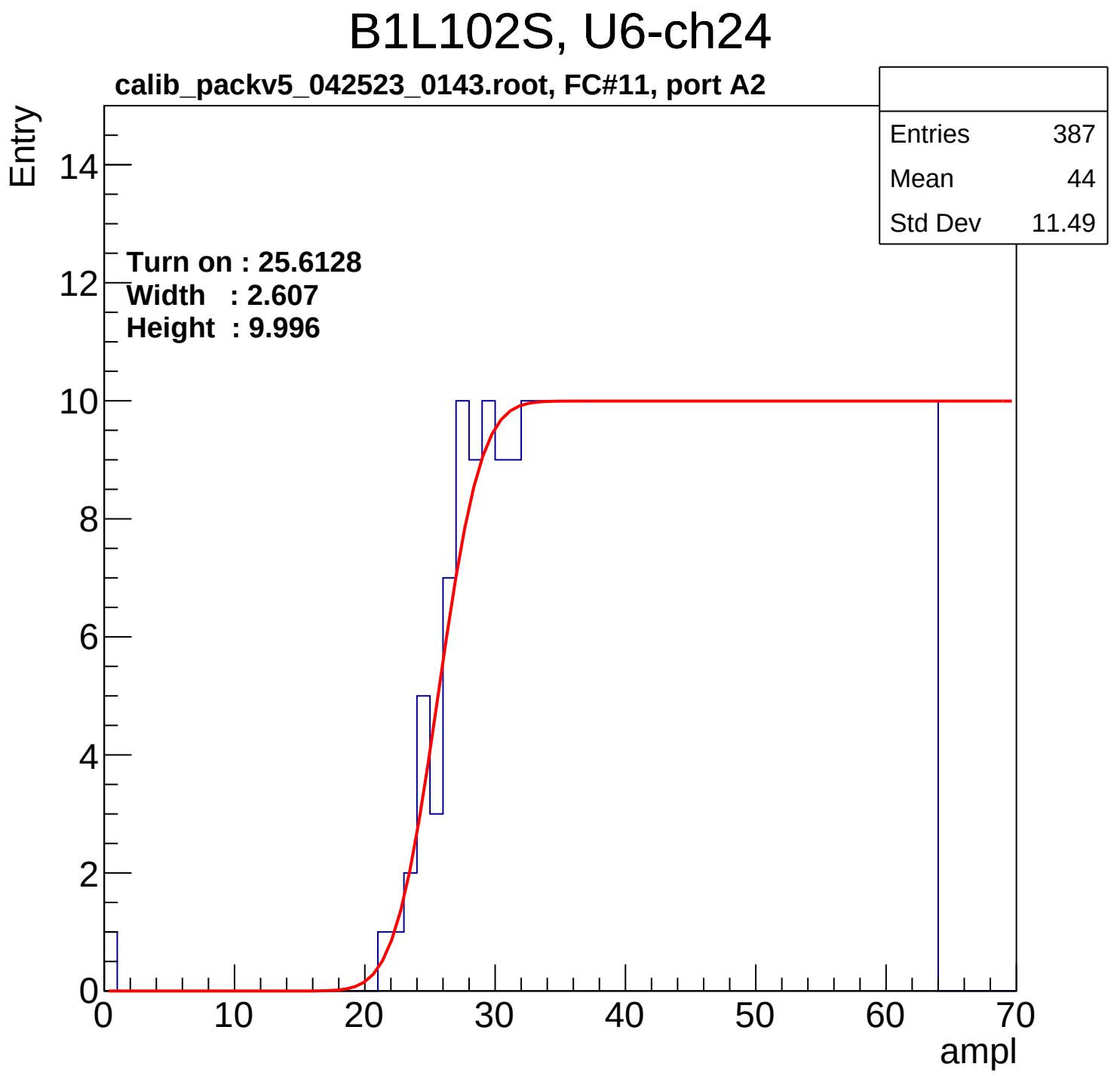
B1L102S, U6-ch24
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 44
Std Dev 11.49
Turn on : 25.6128
Width : 2.607
Height : 9.996
Entry
ampl
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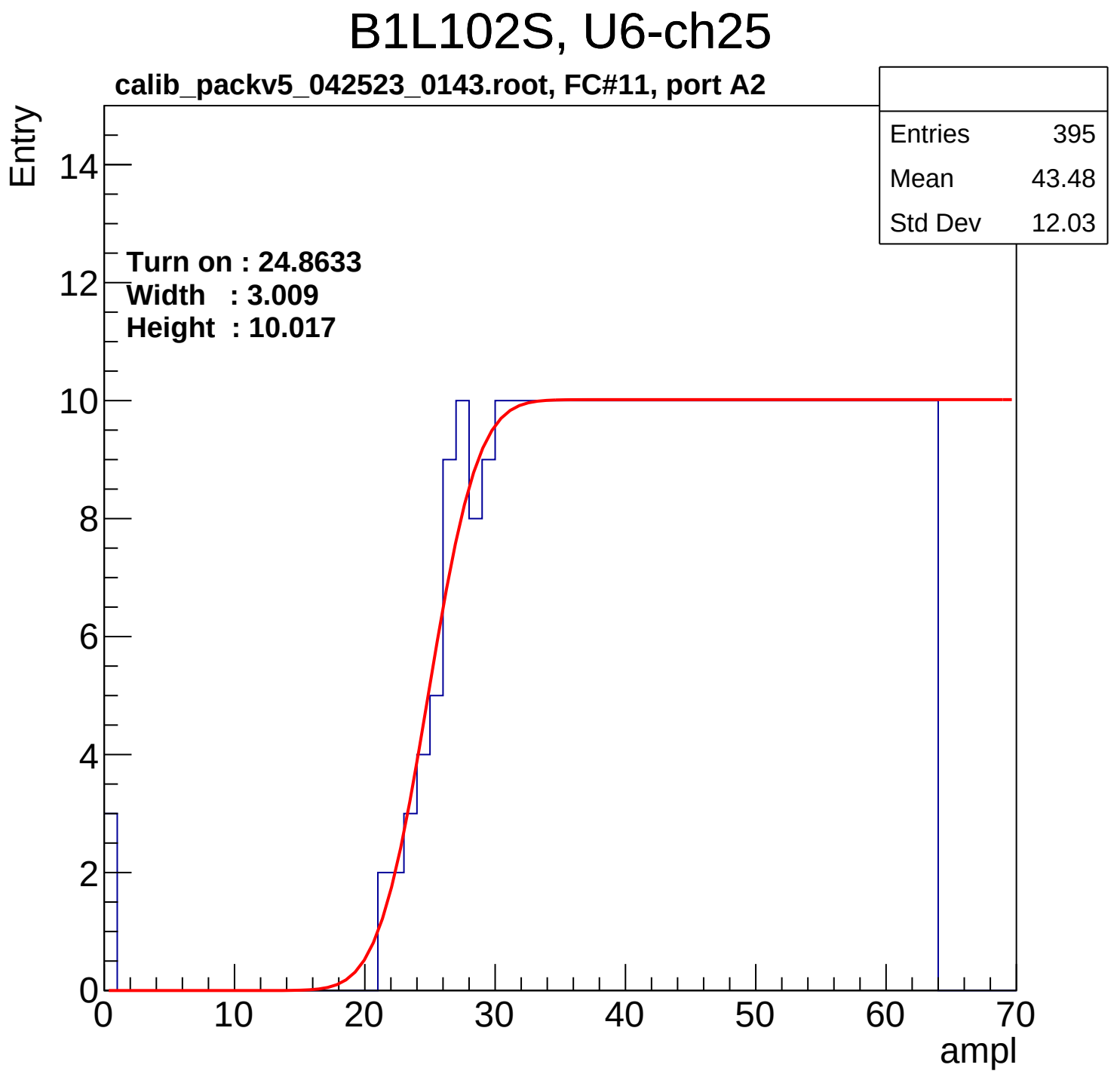
B1L102S, U6-ch25
calib_packv5_042523_0143.root, FC#11, port A2
Entries 395
Mean 43.48
Std Dev 12.03
Turn on : 24.8633
Width : 3.009
Height : 10.017
Entry
ampl
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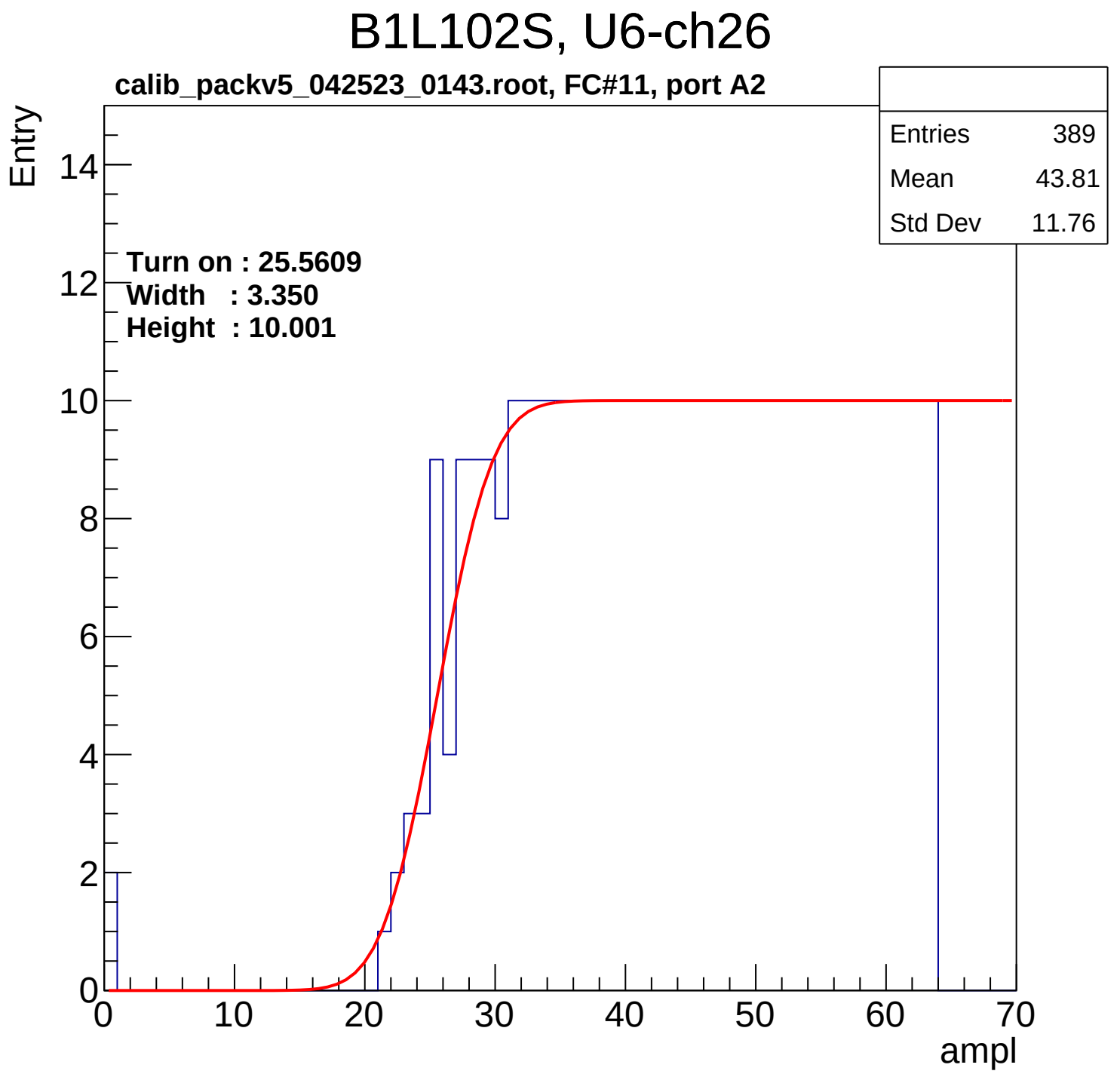
B1L102S, U6-ch26
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.81
Std Dev 11.76
Turn on : 25.5609
Width : 3.350
Height : 10.001
Entry
ampl
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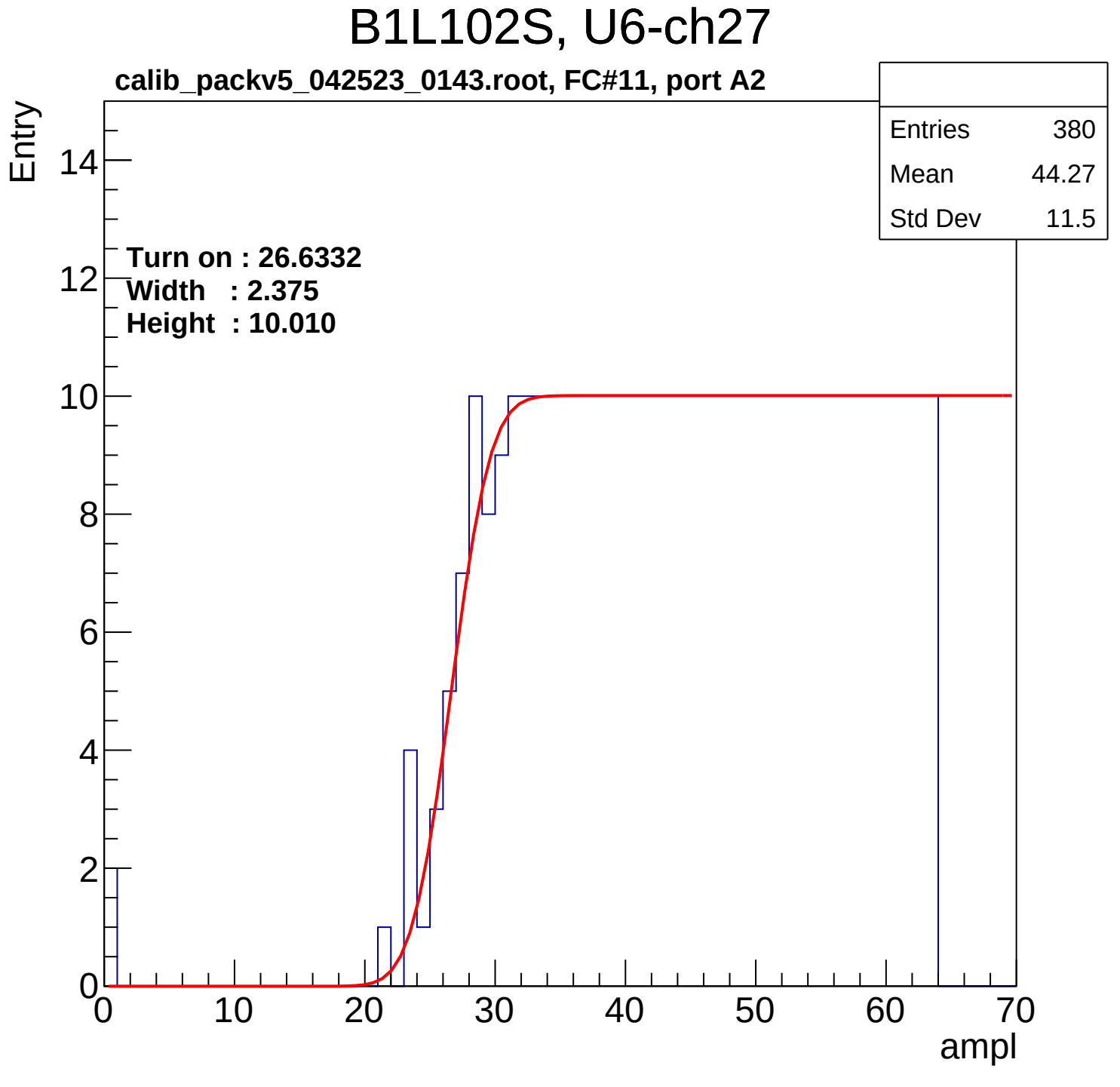
B1L102S, U6-ch27
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.27
Std Dev 11.5
Turn on : 26.6332
Width : 2.375
Height : 10.010
Entry
ampl
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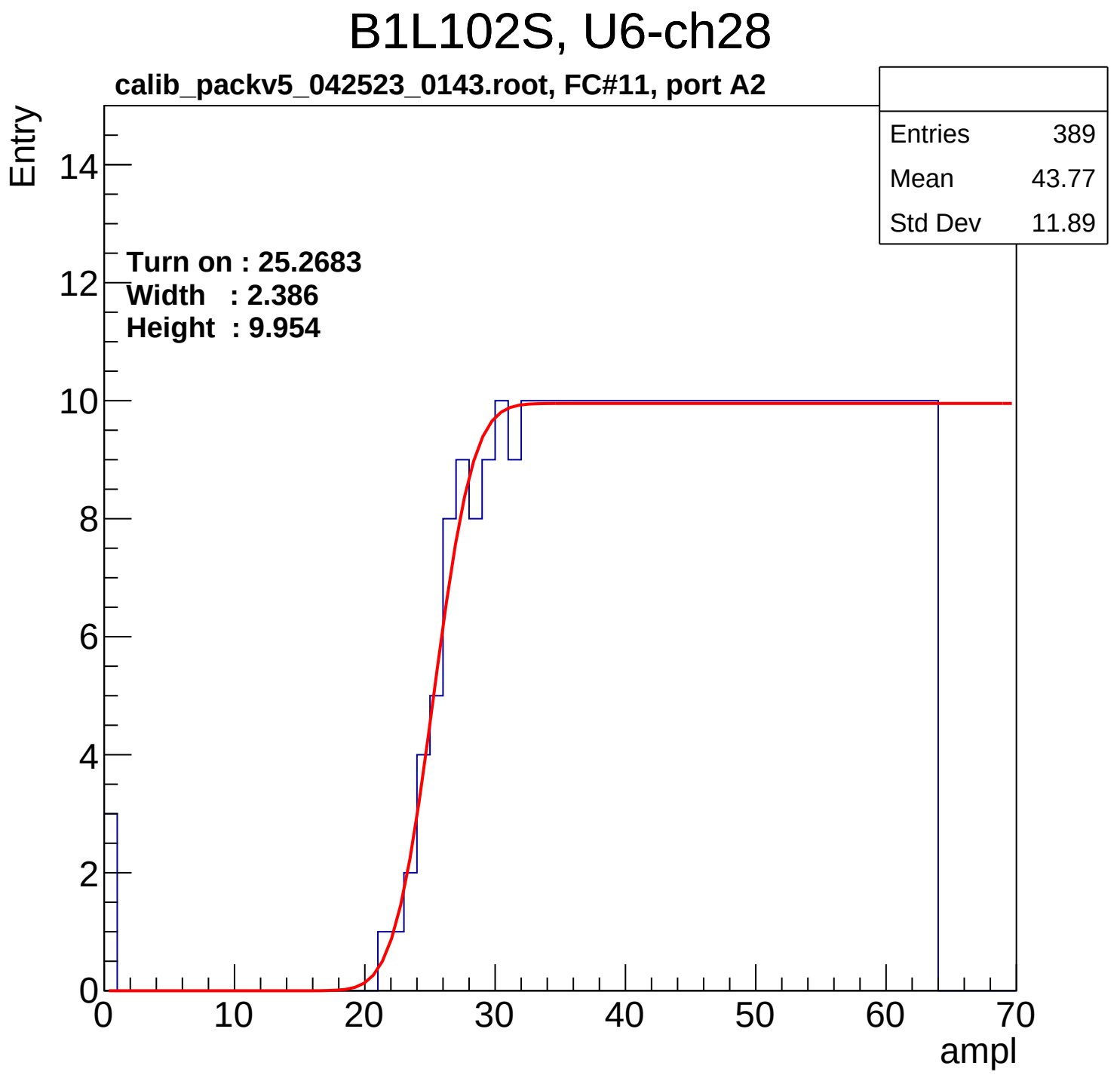
B1L102S, U6-ch28
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.77
Std Dev 11.89
Turn on : 25.2683
Width : 2.386
Height : 9.954
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
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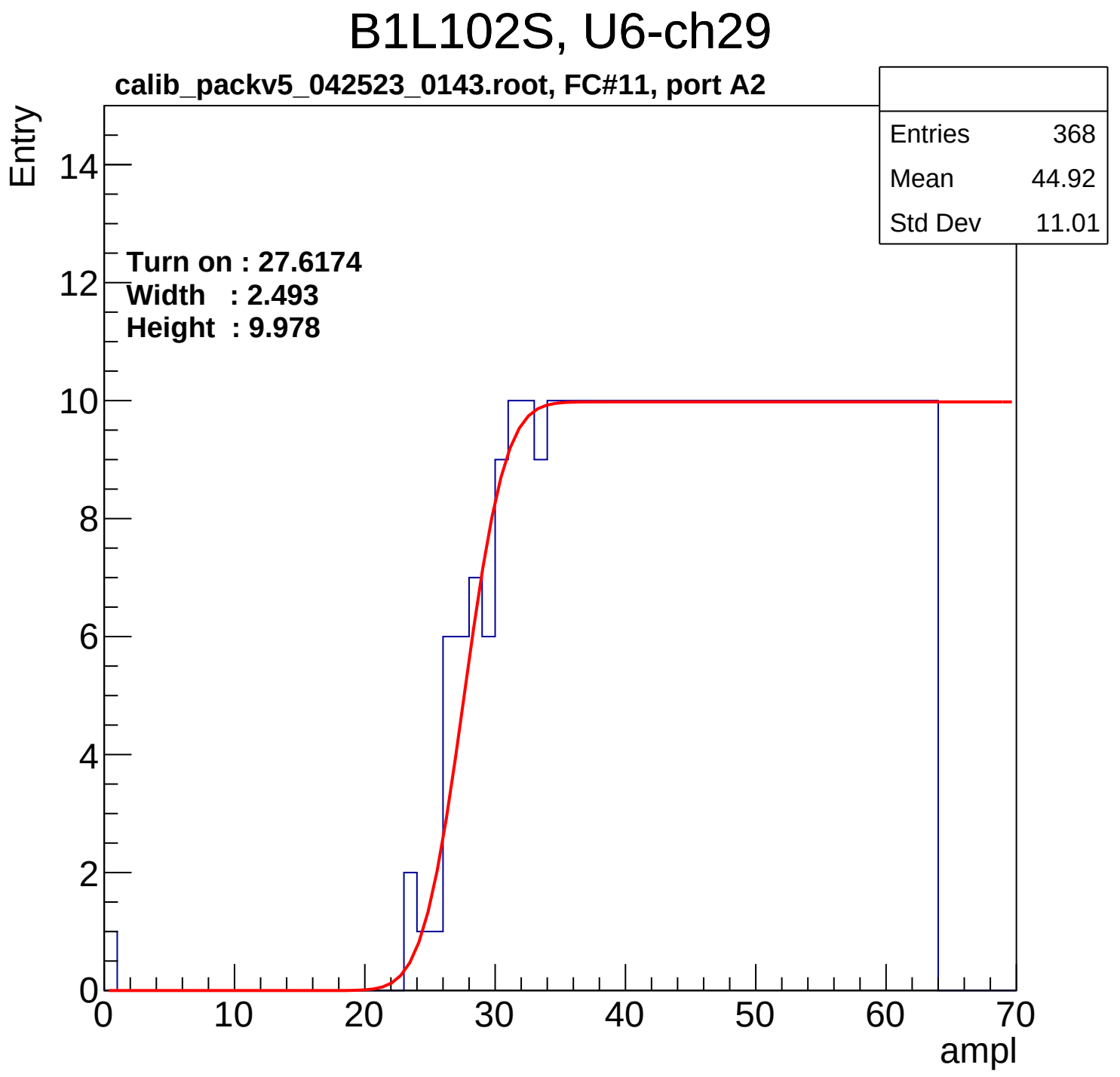
B1L102S, U6-ch29
calib_packv5_042523_0143.root, FC#11, port A2
Entries 368
Mean 44.92
Std Dev 11.01
Turn on : 27.6174
Width : 2.493
Height : 9.978
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ampl
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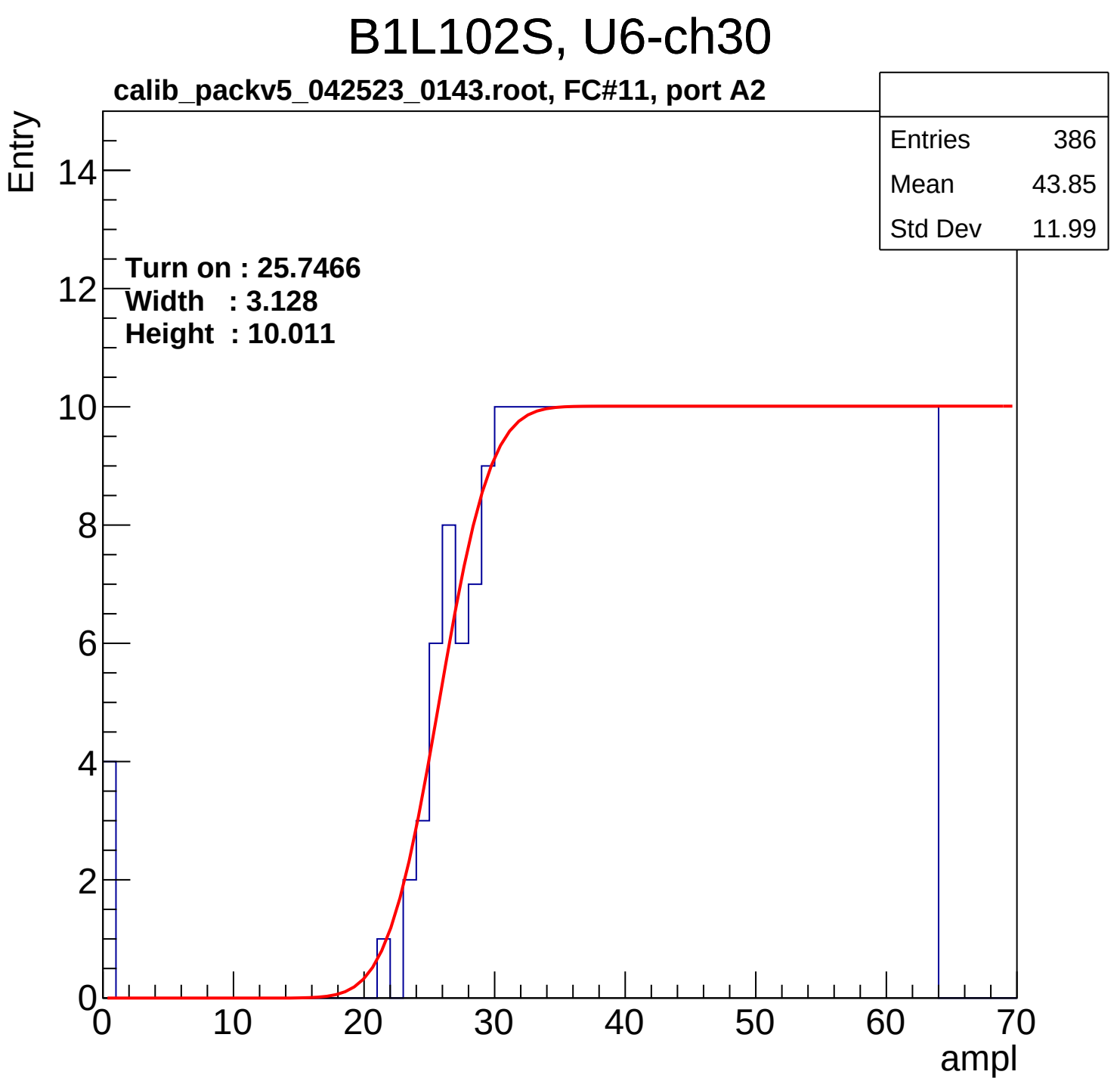
B1L102S, U6-ch30
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.85
Std Dev 11.99
Turn on : 25.7466
Width : 3.128
Height : 10.011
Entry
ampl
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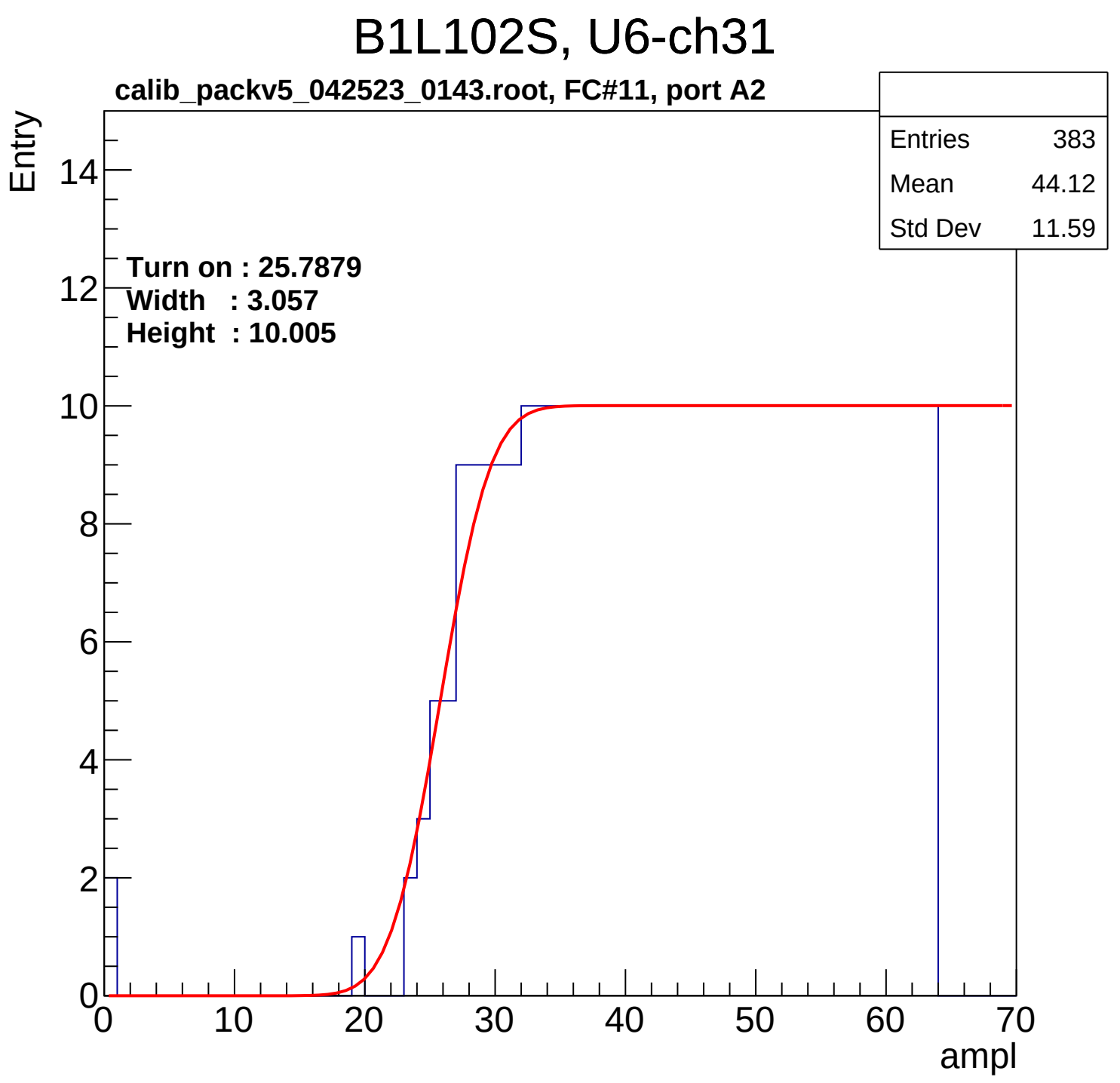
B1L102S, U6-ch31
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.12
Std Dev 11.59
Turn on : 25.7879
Width : 3.057
Height : 10.005
Entry
ampl
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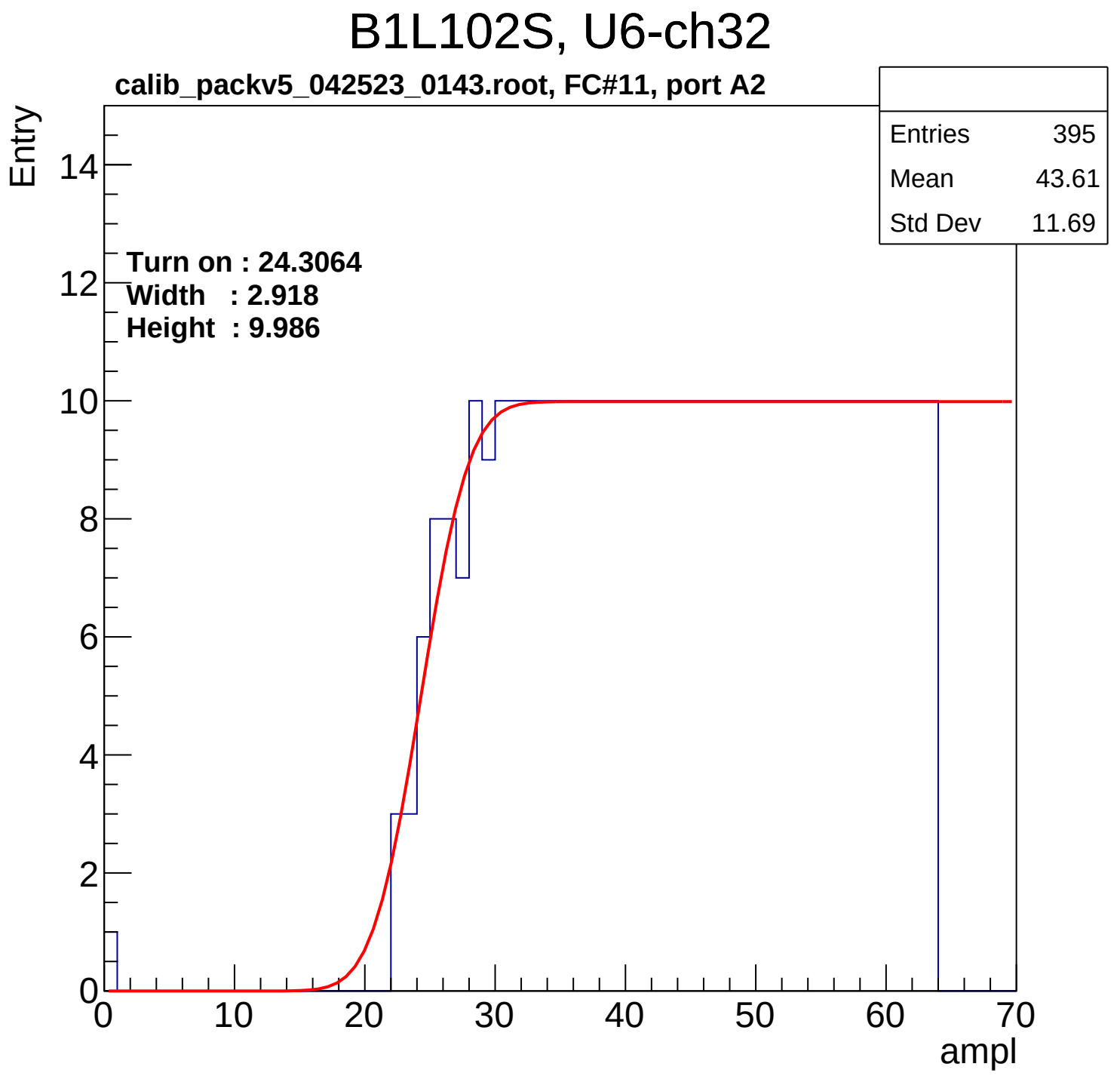
B1L102S, U6-ch32
calib_packv5_042523_0143.root, FC#11, port A2
Entries 395
Mean 43.61
Std Dev 11.69
Turn on : 24.3064
Width : 2.918
Height : 9.986
Entry
ampl
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2
4
6
8
10
12
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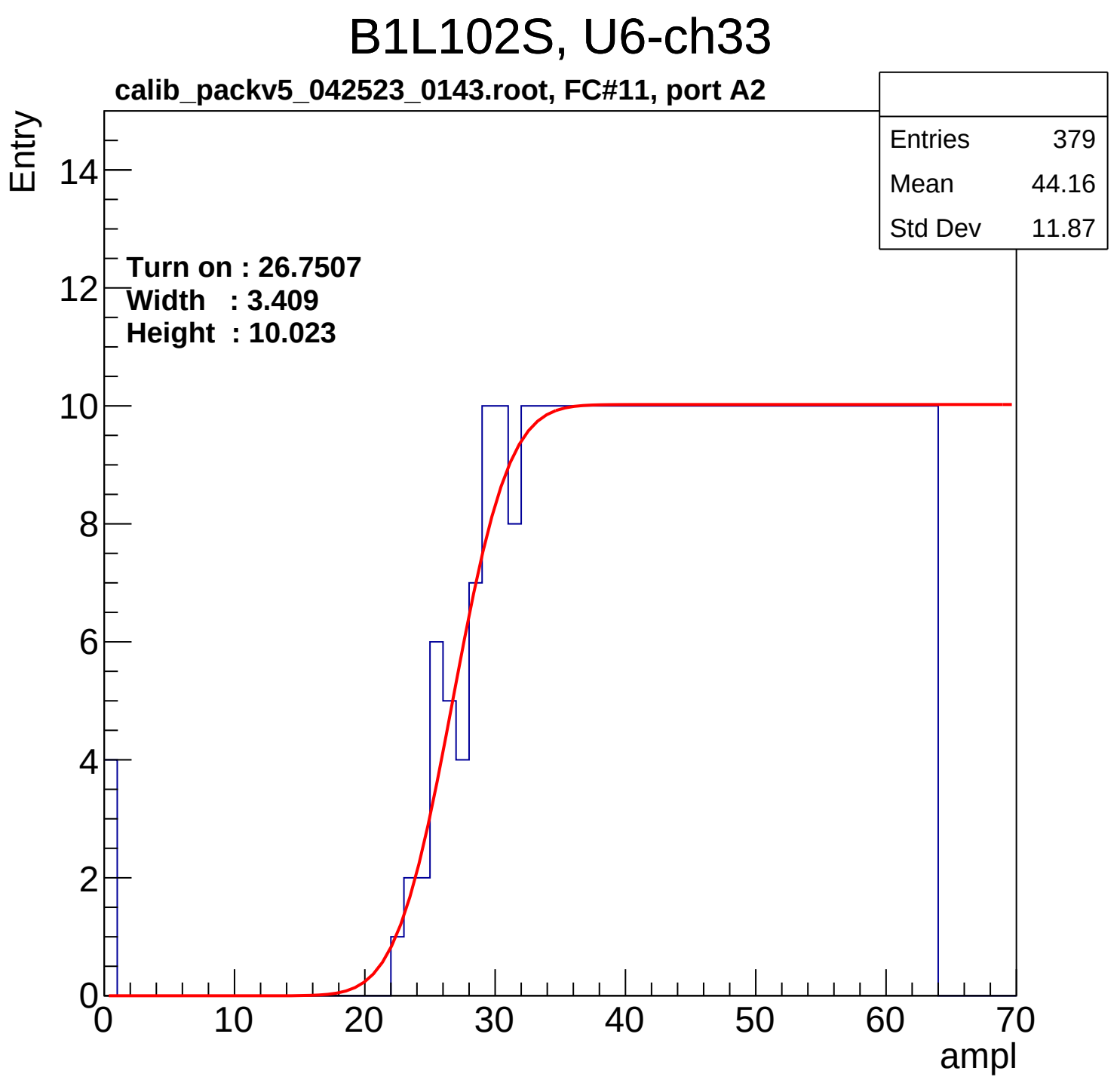
B1L102S, U6-ch33
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.16
Std Dev 11.87
Turn on : 26.7507
Width : 3.409
Height : 10.023
Entry
ampl
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2
4
6
8
10
12
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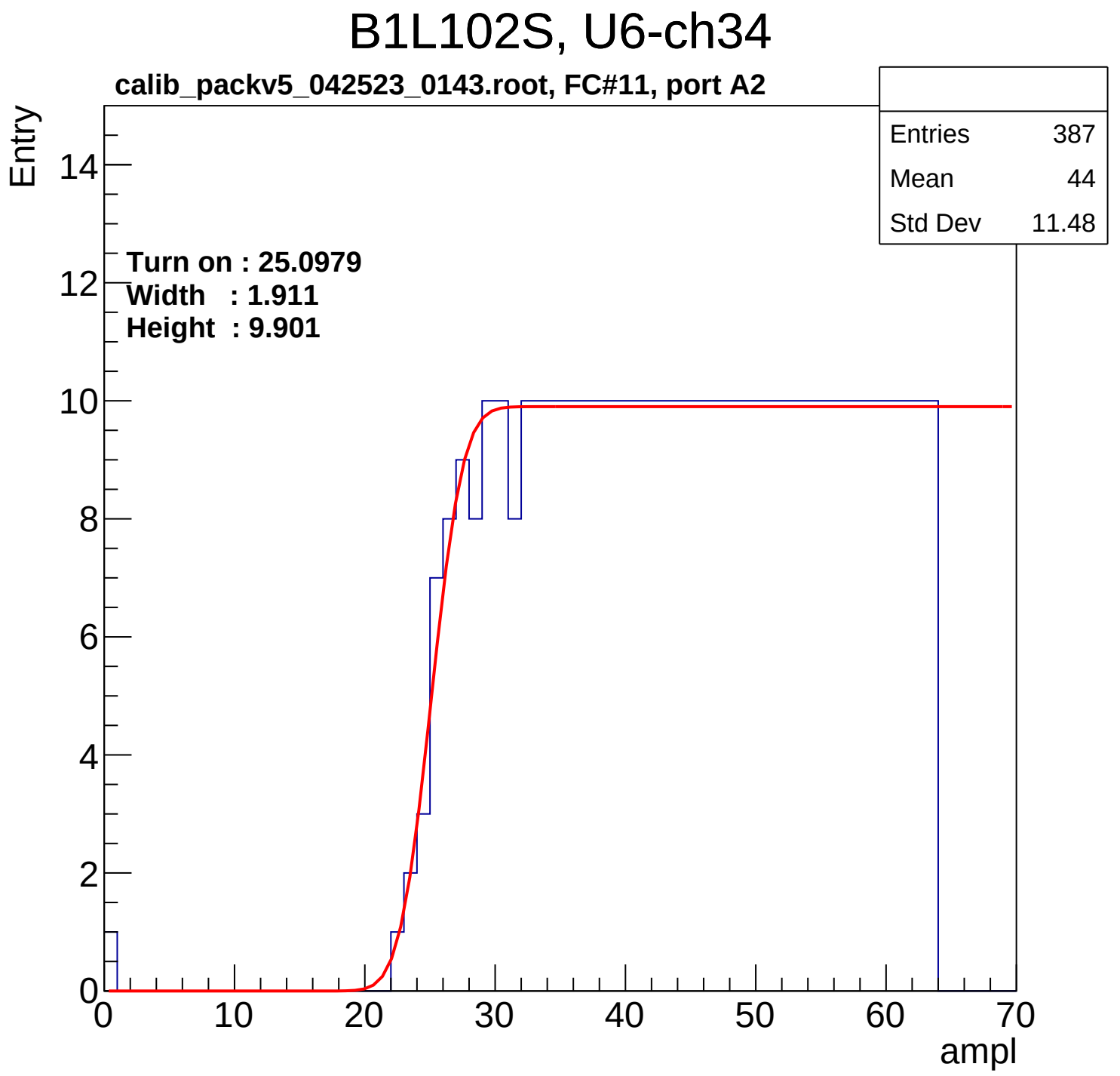
B1L102S, U6-ch34
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 44
Std Dev 11.48
Turn on : 25.0979
Width : 1.911
Height : 9.901
Entry
ampl
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2
4
6
8
10
12
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0
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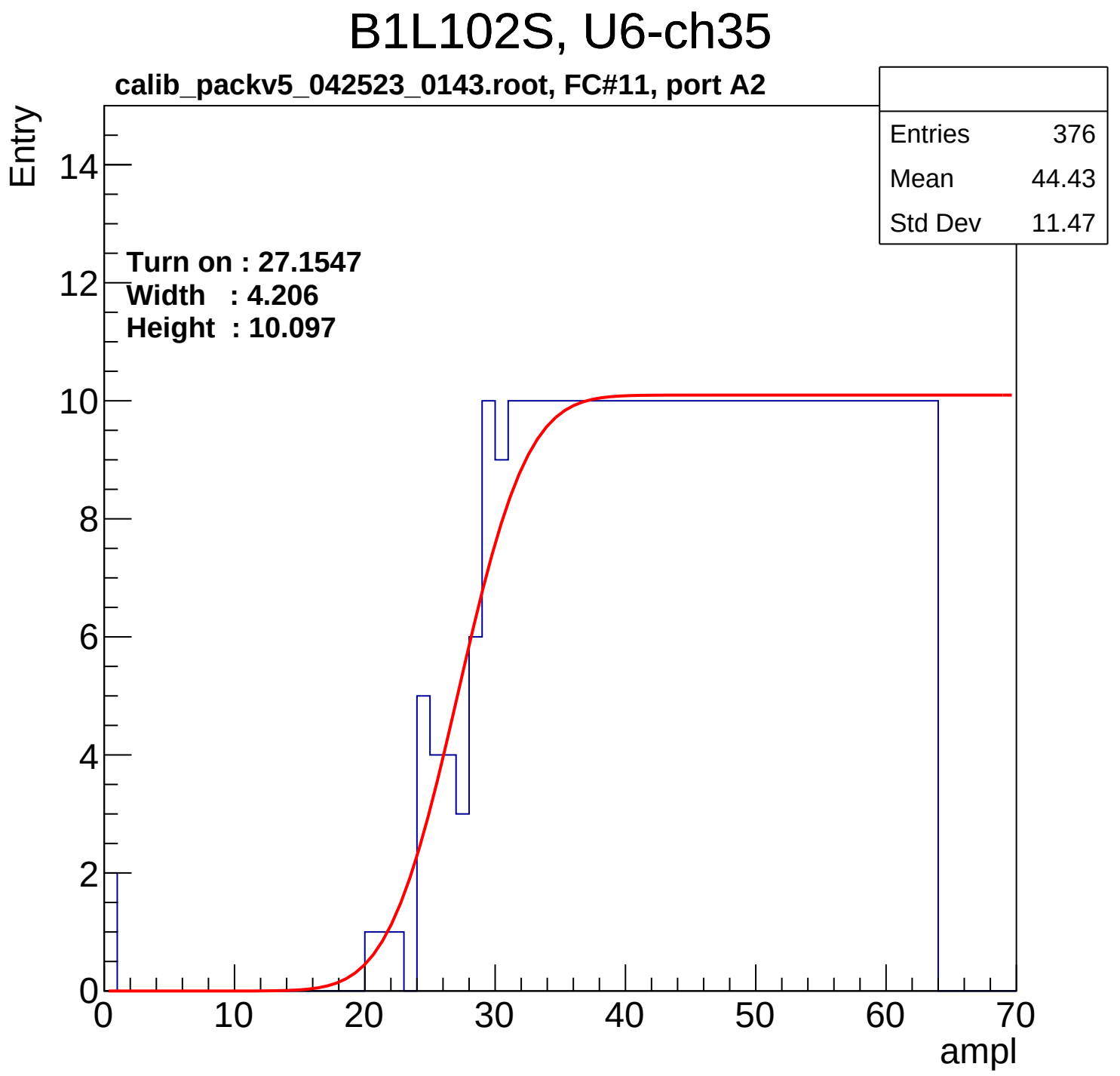
B1L102S, U6-ch35
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.43
Std Dev 11.47
Turn on : 27.1547
Width : 4.206
Height : 10.097
Entry
ampl
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4
6
8
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12
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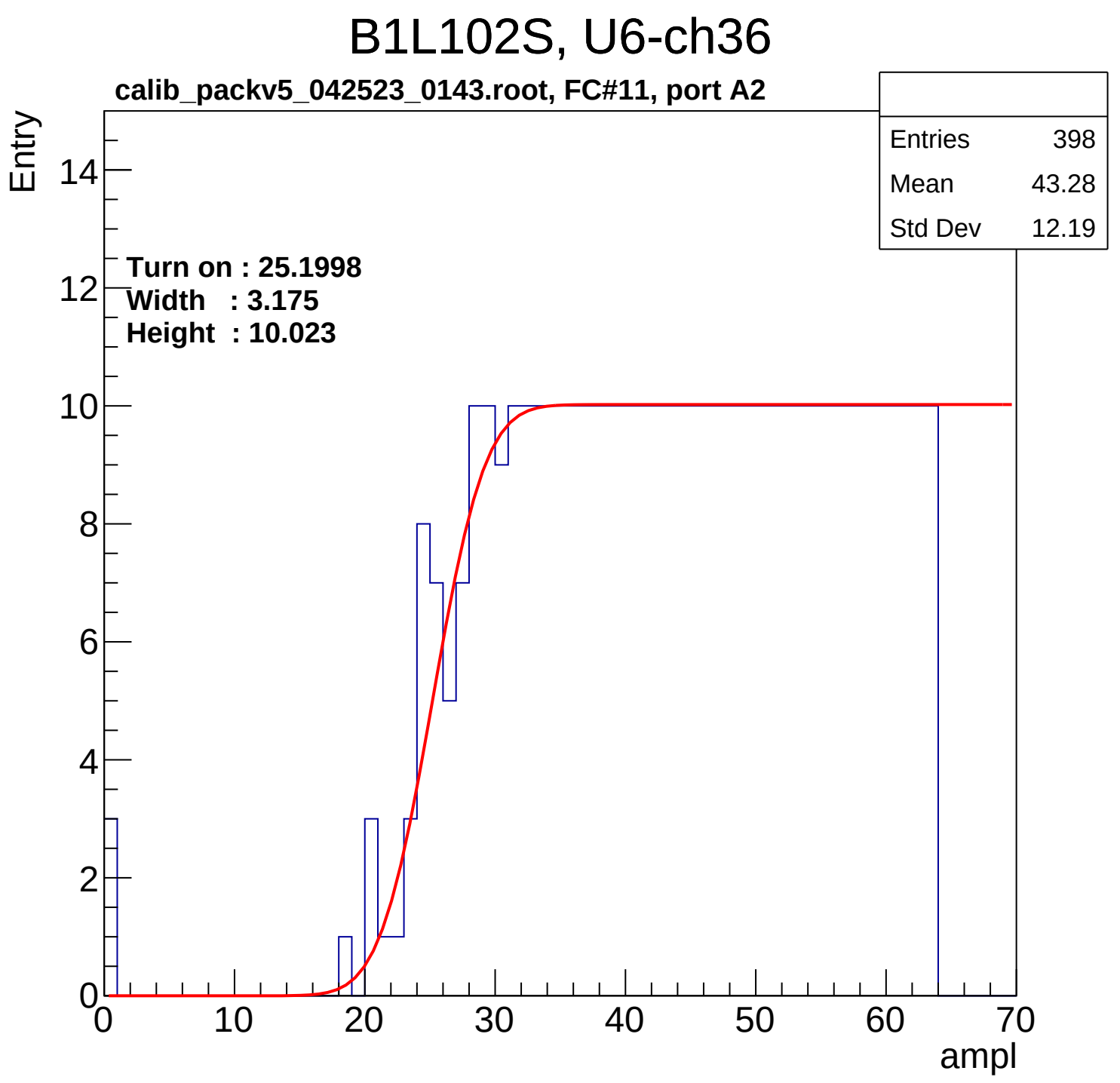
B1L102S, U6-ch36
calib_packv5_042523_0143.root, FC#11, port A2
Entries 398
Mean 43.28
Std Dev 12.19
Turn on : 25.1998
Width : 3.175
Height : 10.023
Entry
ampl
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4
6
8
10
12
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60
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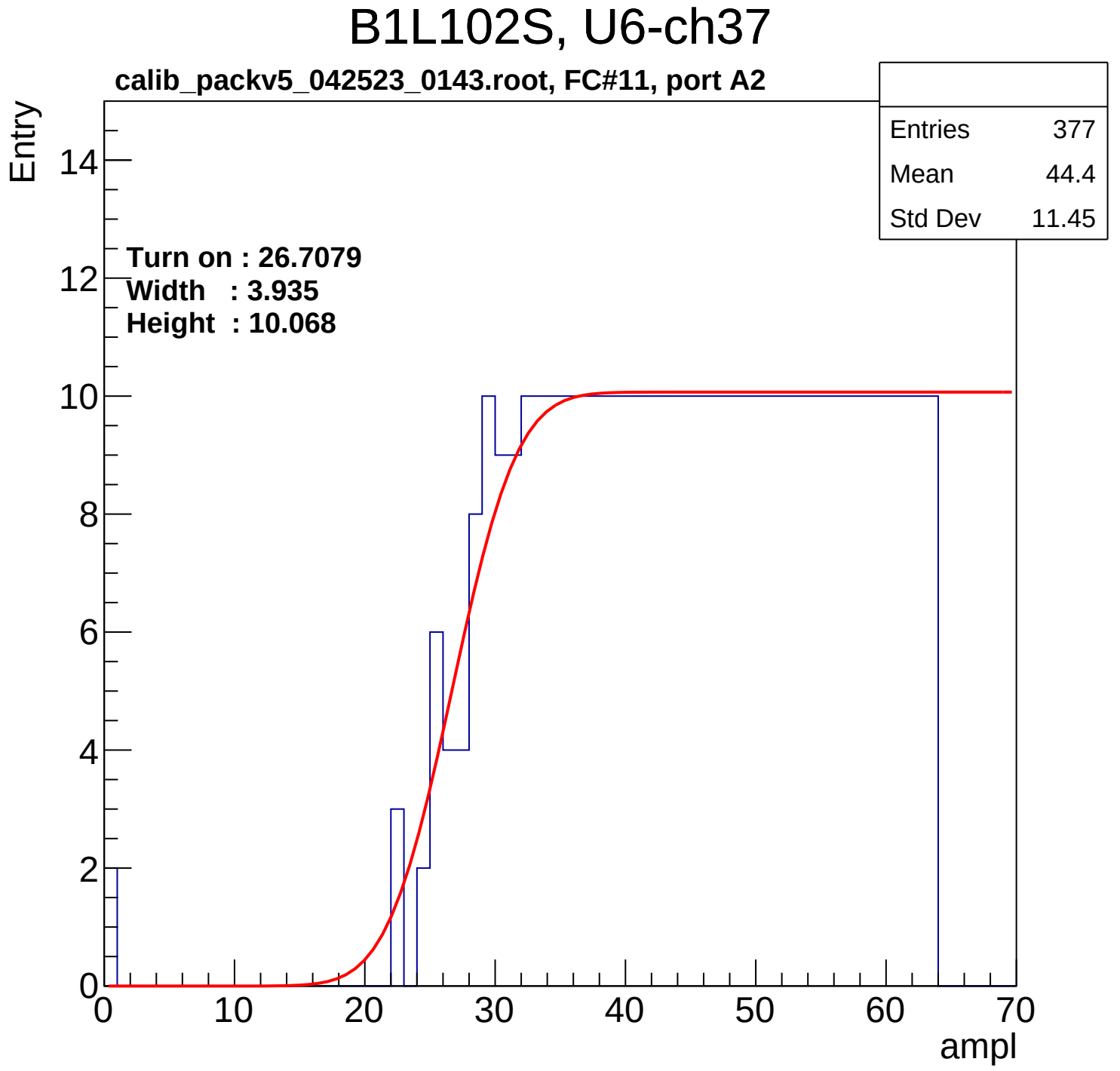
B1L102S, U6-ch37
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.4
Std Dev 11.45
Turn on : 26.7079
Width : 3.935
Height : 10.068
Entry
ampl
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4
6
8
10
12
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0
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20
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60
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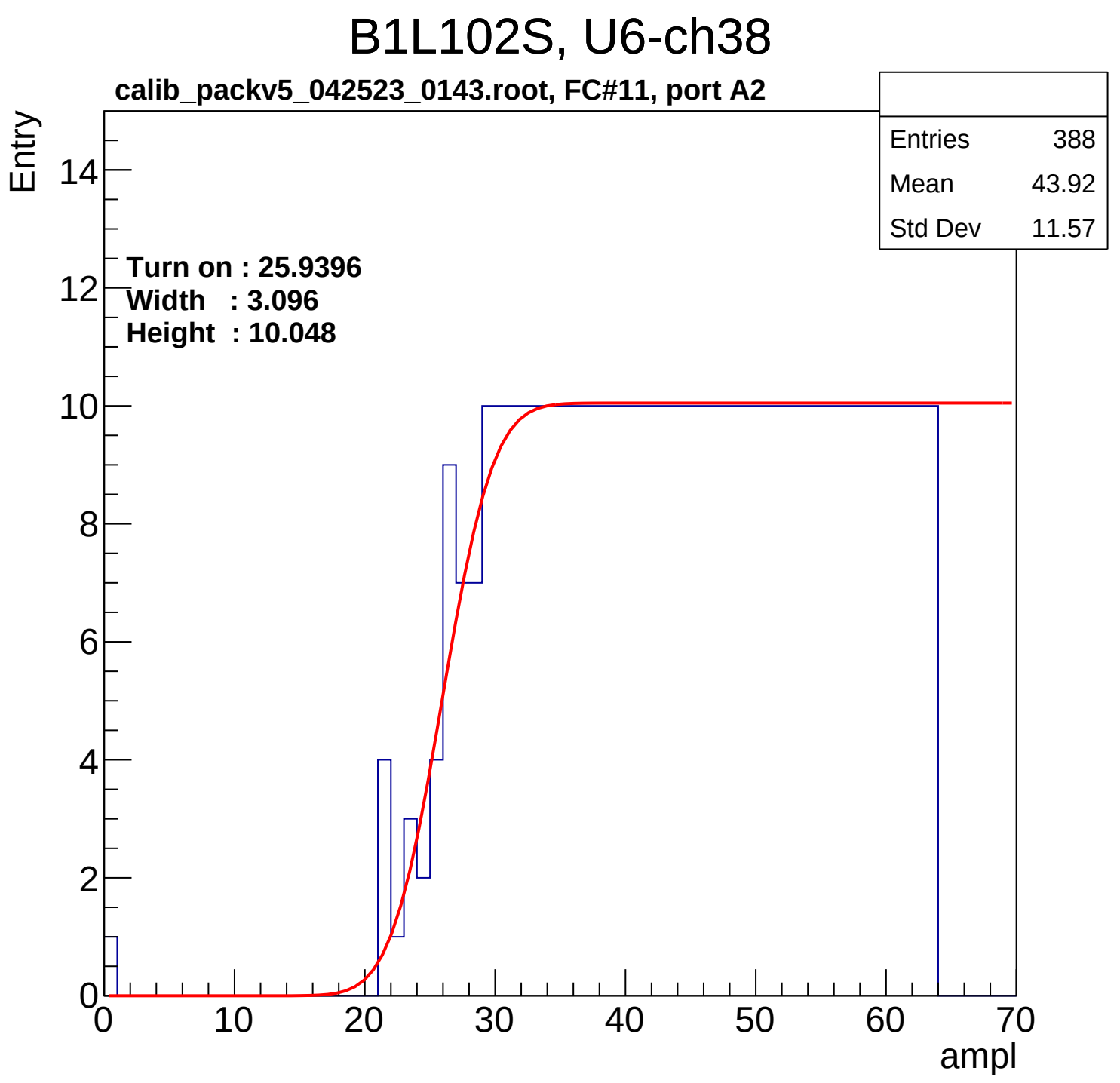
B1L102S, U6-ch38
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.92
Std Dev 11.57
Turn on : 25.9396
Width : 3.096
Height : 10.048
Entry
ampl
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2
4
6
8
10
12
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60
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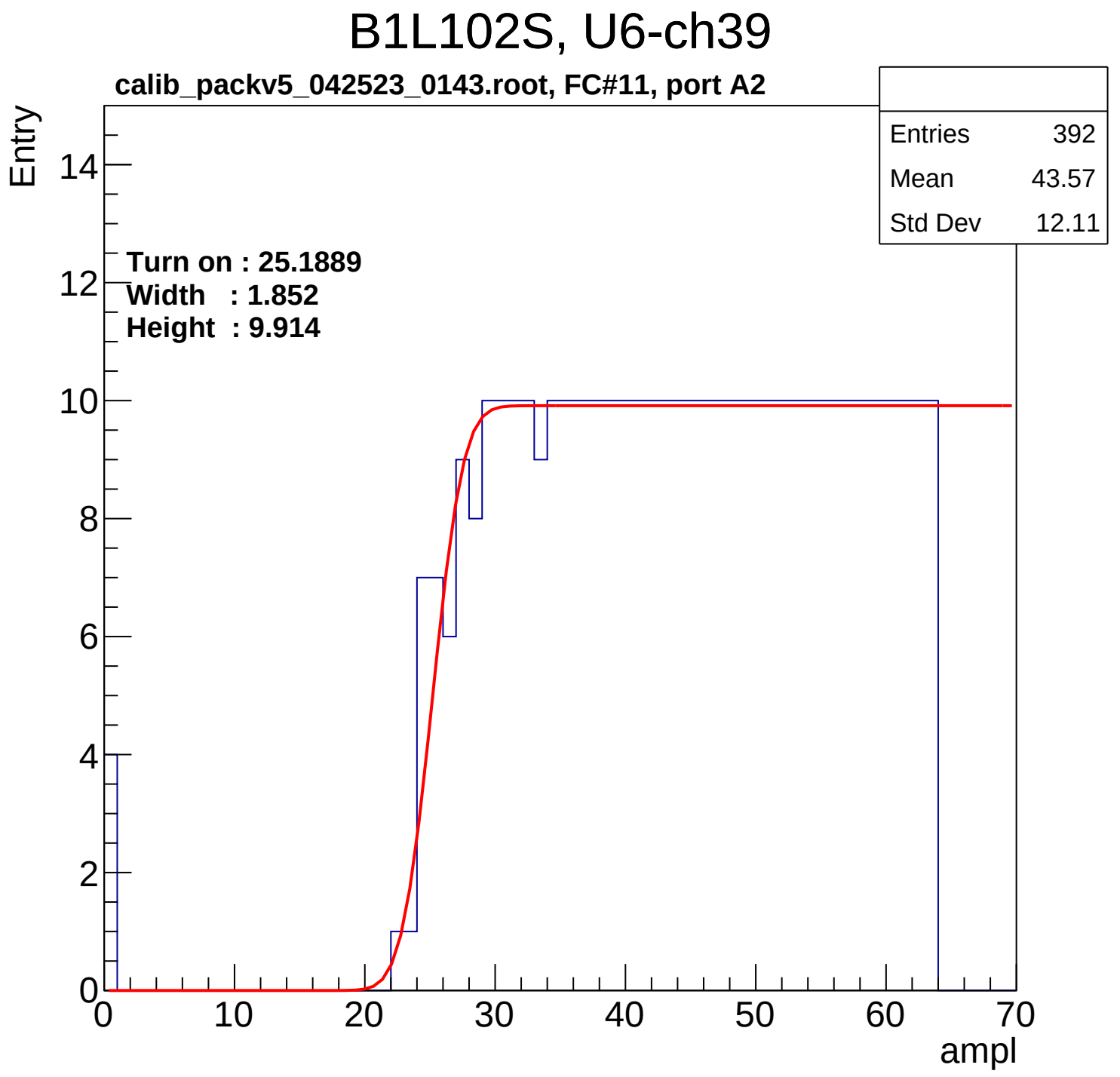
B1L102S, U6-ch39
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.57
Std Dev 12.11
Turn on : 25.1889
Width : 1.852
Height : 9.914
Entry
ampl
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4
6
8
10
12
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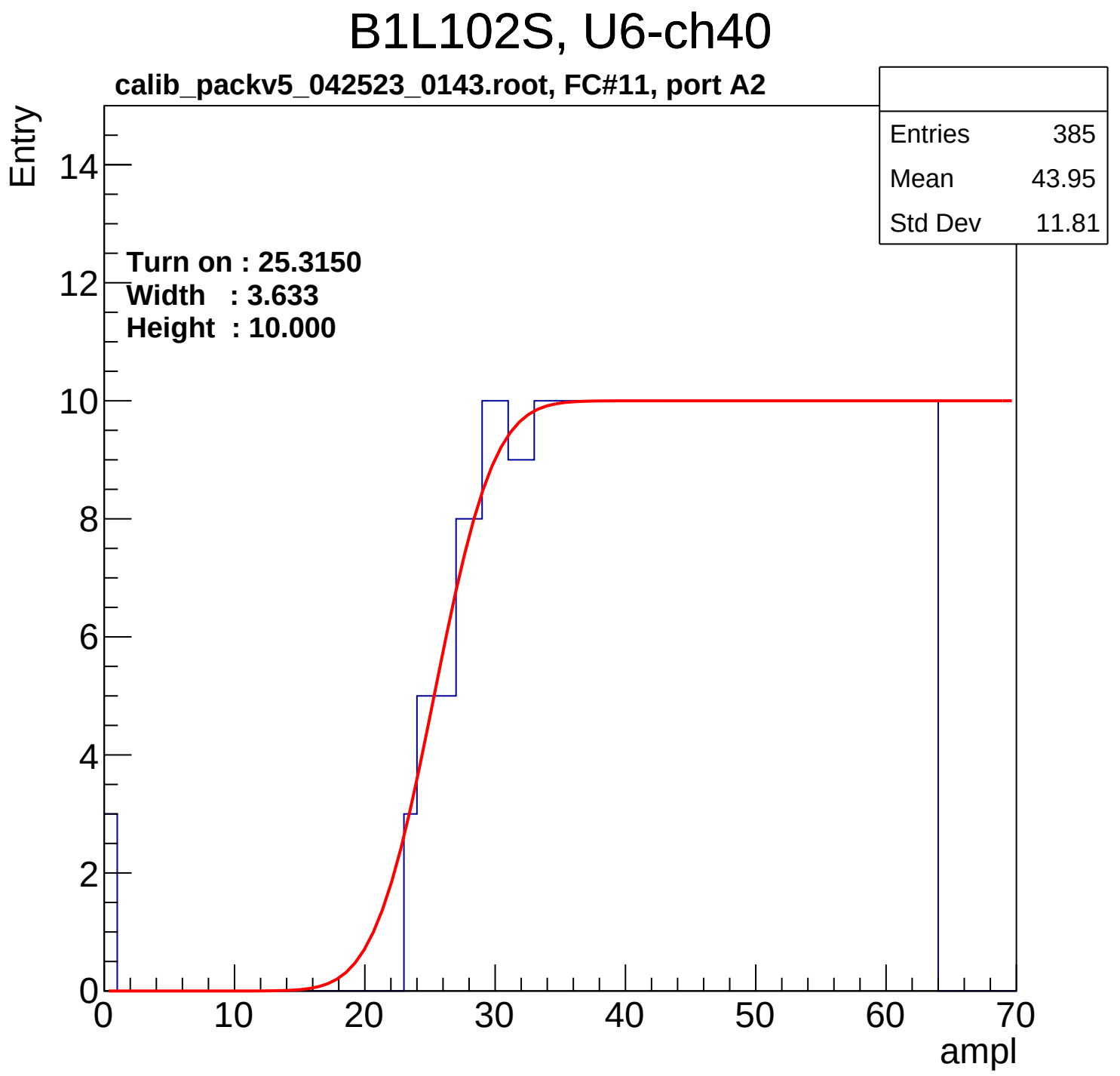
B1L102S, U6-ch40
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.95
Std Dev 11.81
Turn on : 25.3150
Width : 3.633
Height : 10.000
Entry
ampl
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6
8
10
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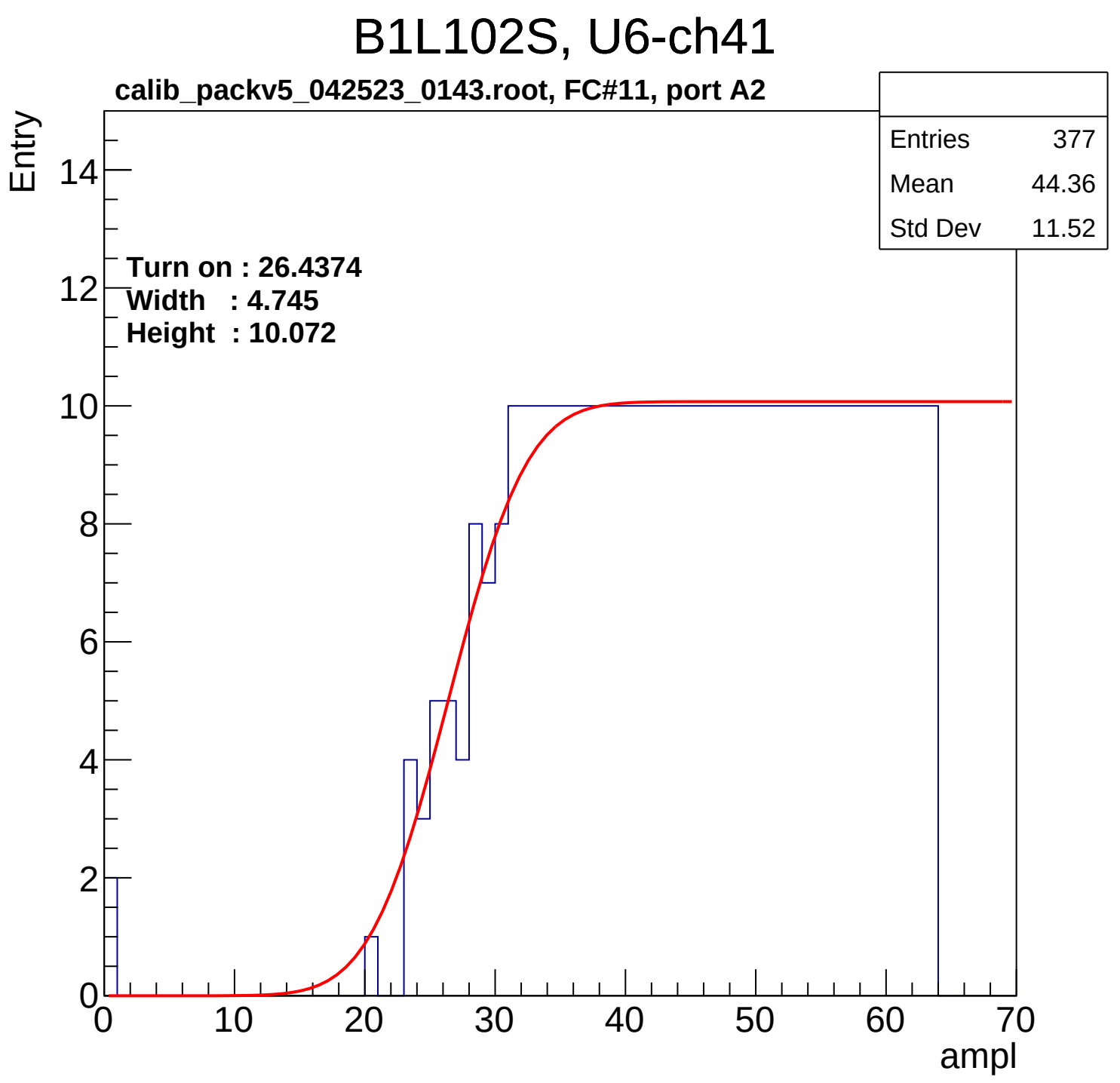
B1L102S, U6-ch41
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.36
Std Dev 11.52
Turn on : 26.4374
Width : 4.745
Height : 10.072
Entry
ampl
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4
6
8
10
12
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0
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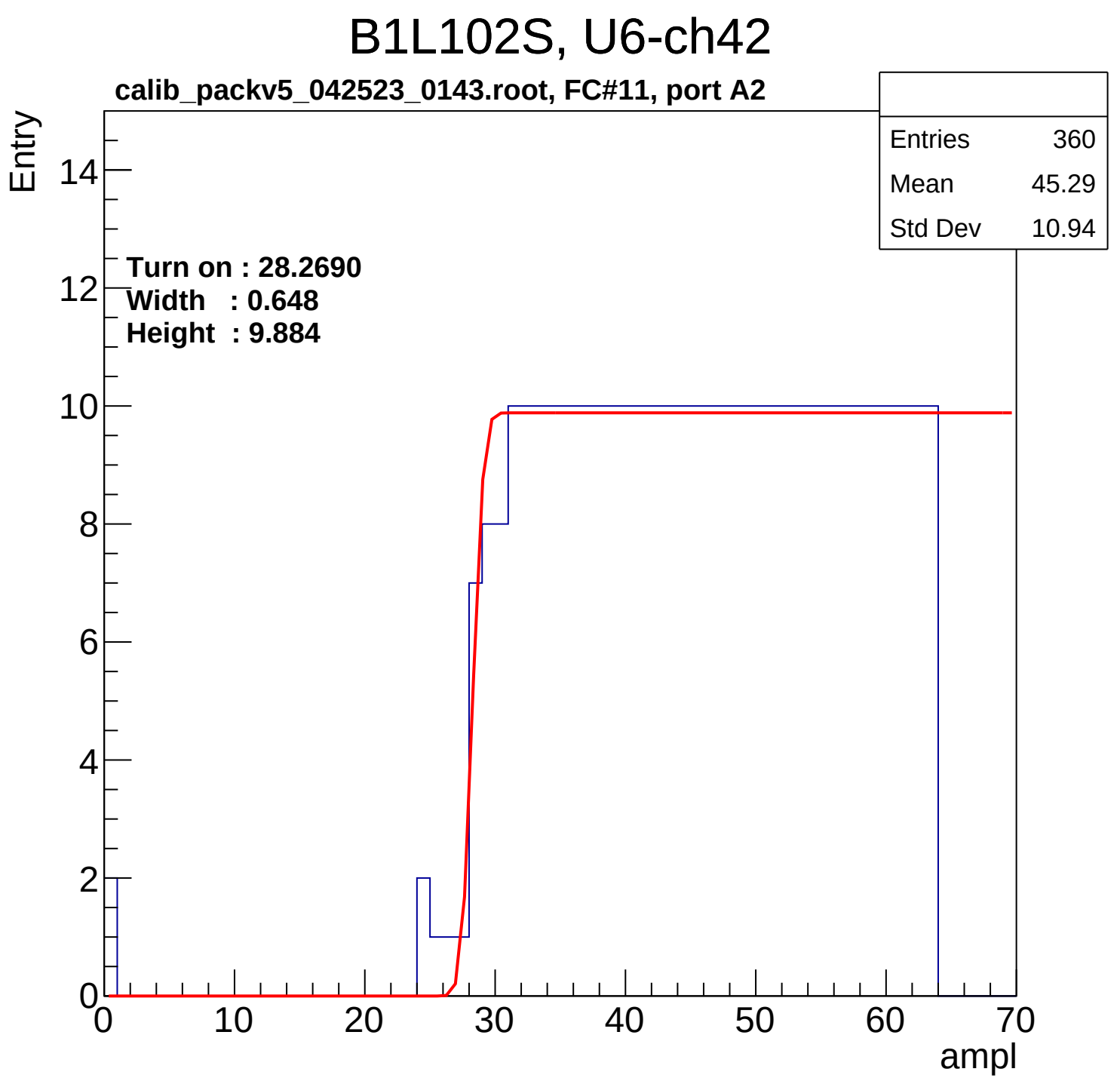
B1L102S, U6-ch42
calib_packv5_042523_0143.root, FC#11, port A2
Entries 360
Mean 45.29
Std Dev 10.94
Turn on : 28.2690
Width : 0.648
Height : 9.884
Entry
ampl
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2
4
6
8
10
12
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0
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20
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60
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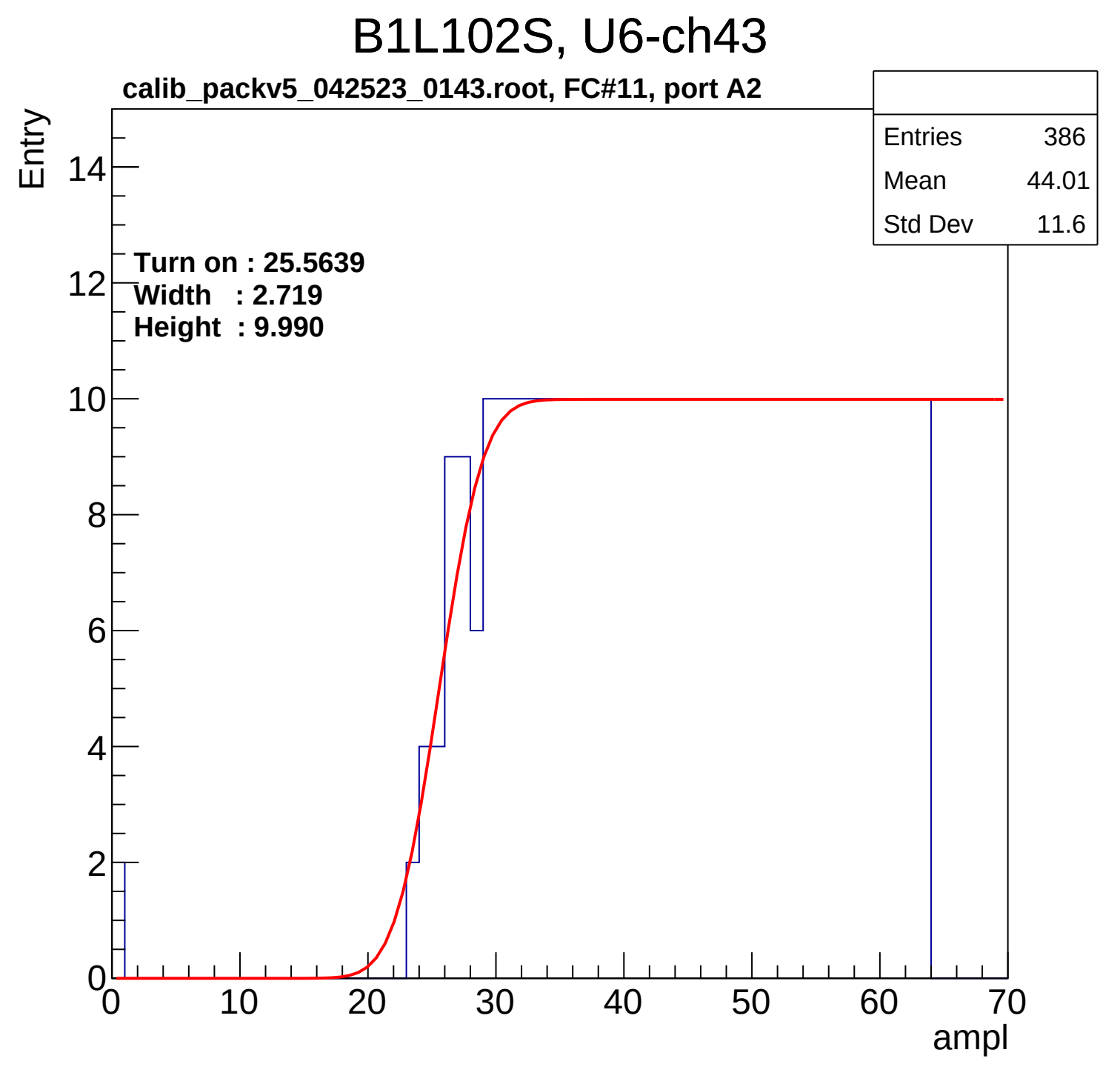
B1L102S, U6-ch43
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 44.01
Std Dev 11.6
Turn on : 25.5639
Width : 2.719
Height : 9.990
Entry
ampl
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6
8
10
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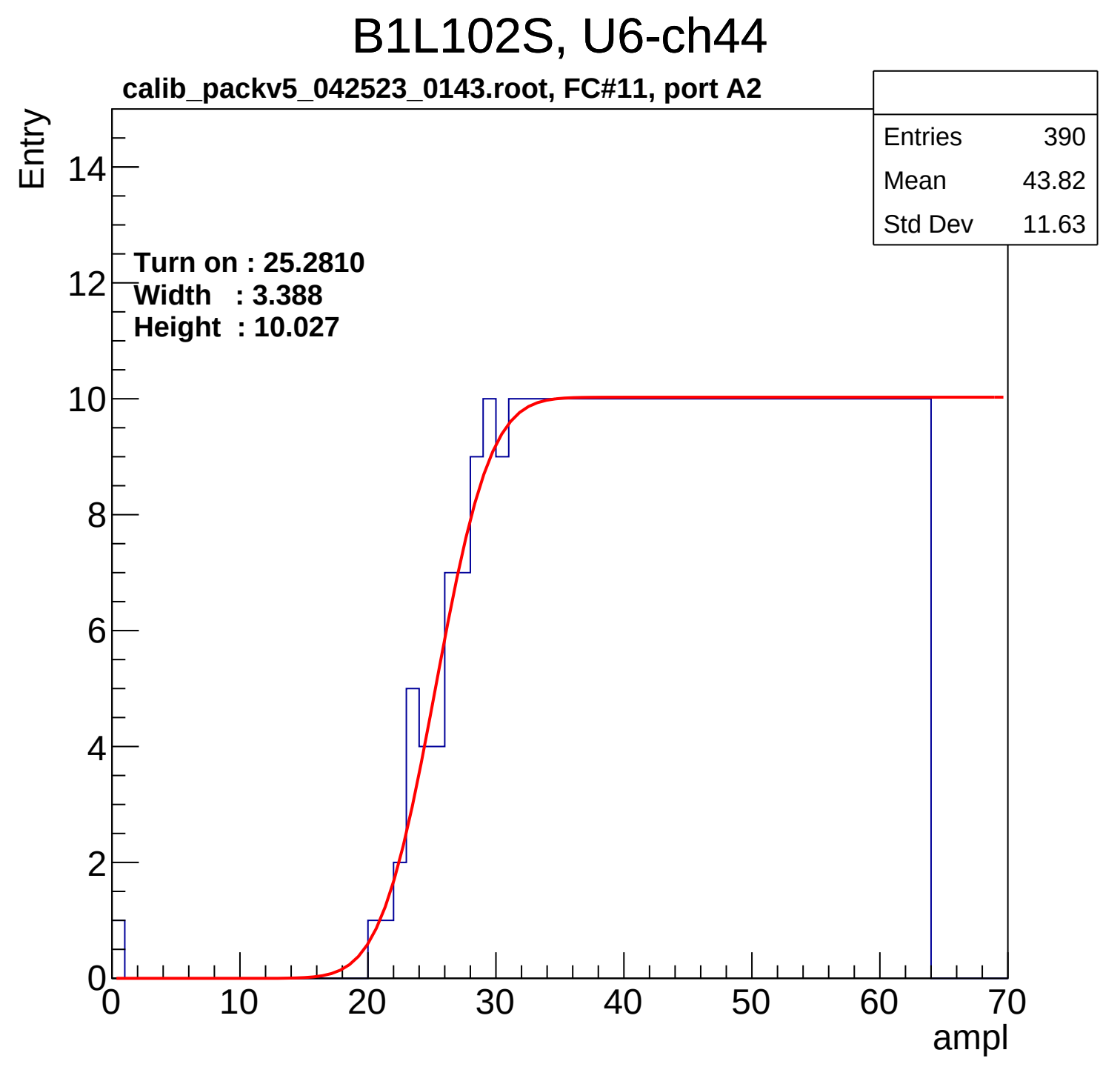
B1L102S, U6-ch44
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.82
Std Dev 11.63
Turn on : 25.2810
Width : 3.388
Height : 10.027
Entry
ampl
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6
8
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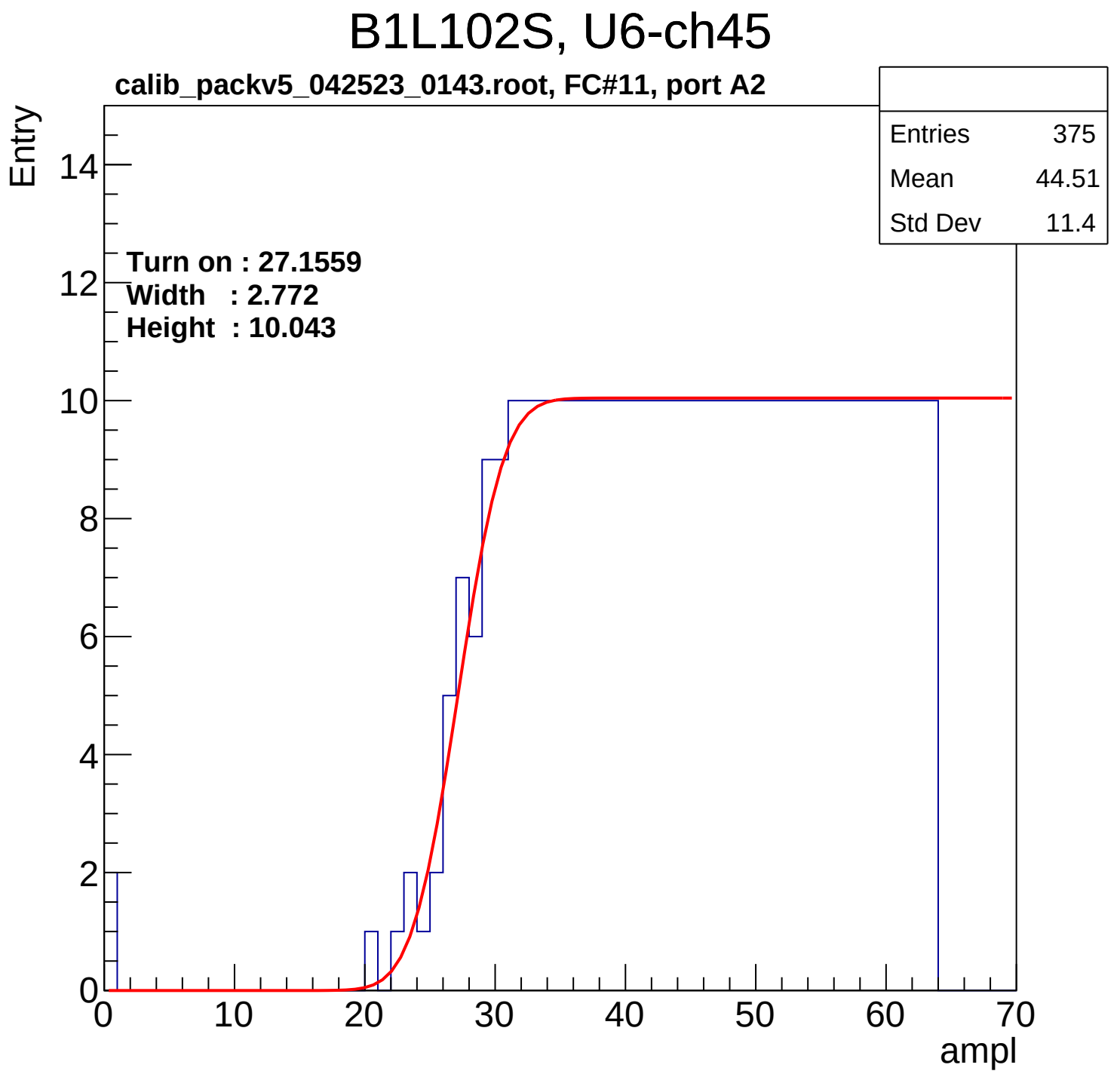
B1L102S, U6-ch45
calib_packv5_042523_0143.root, FC#11, port A2
Entries 375
Mean 44.51
Std Dev 11.4
Turn on : 27.1559
Width : 2.772
Height : 10.043
Entry
ampl
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8
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60
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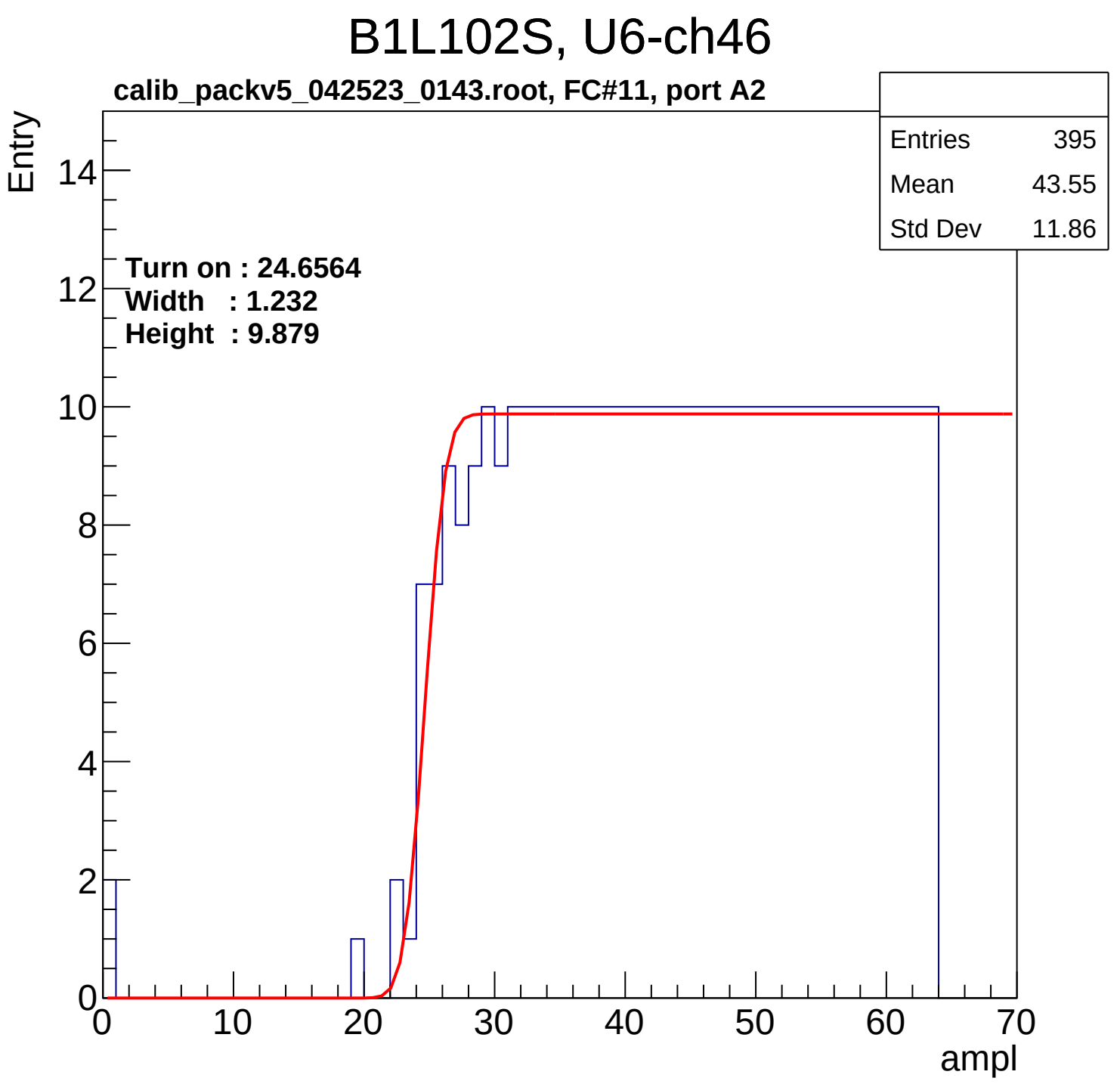
B1L102S, U6-ch46
calib_packv5_042523_0143.root, FC#11, port A2
Entries 395
Mean 43.55
Std Dev 11.86
Turn on : 24.6564
Width : 1.232
Height : 9.879
Entry
ampl
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10
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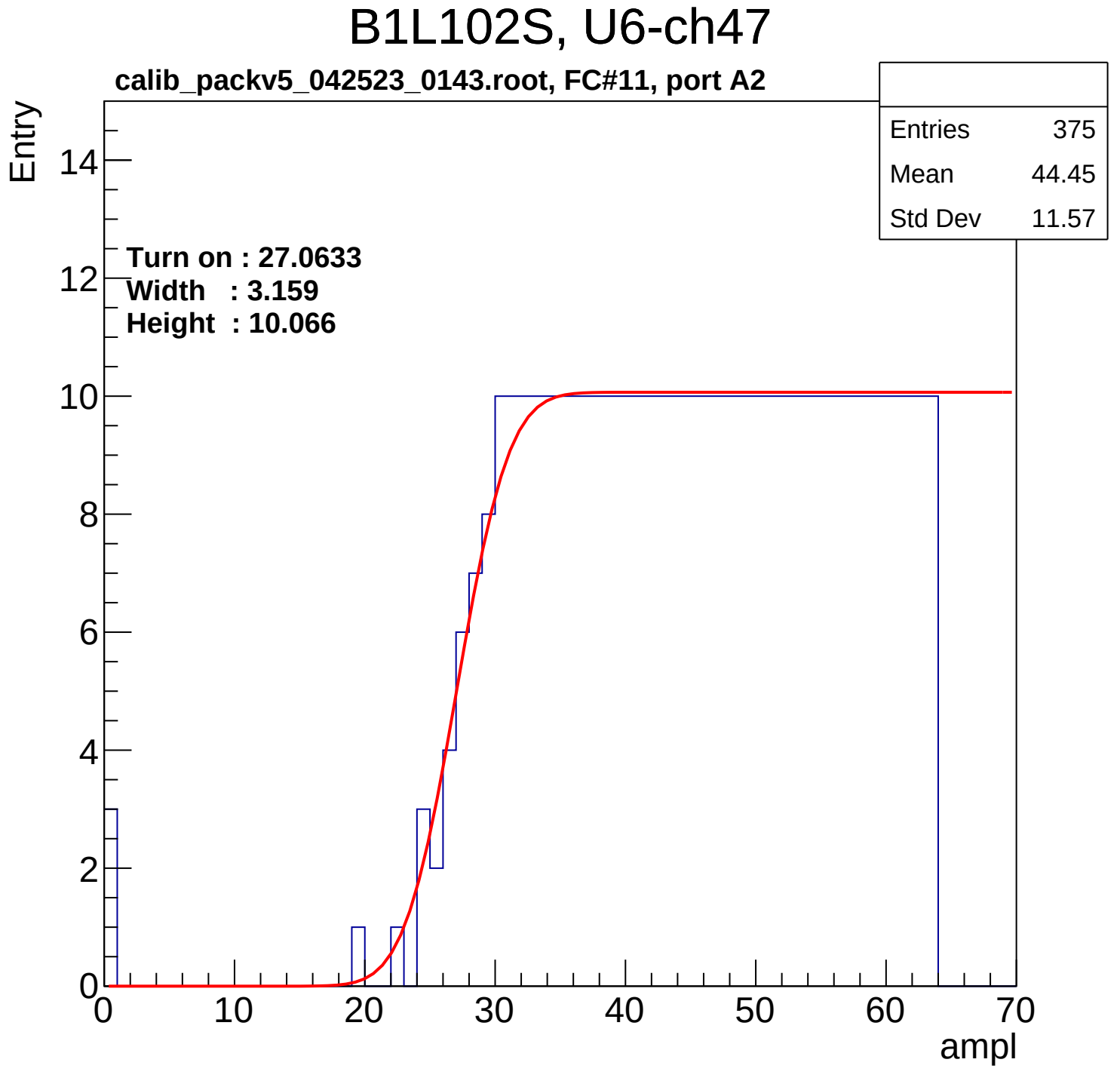
B1L102S, U6-ch47
calib_packv5_042523_0143.root, FC#11, port A2
Entries 375
Mean 44.45
Std Dev 11.57
Turn on : 27.0633
Width : 3.159
Height : 10.066
Entry
ampl
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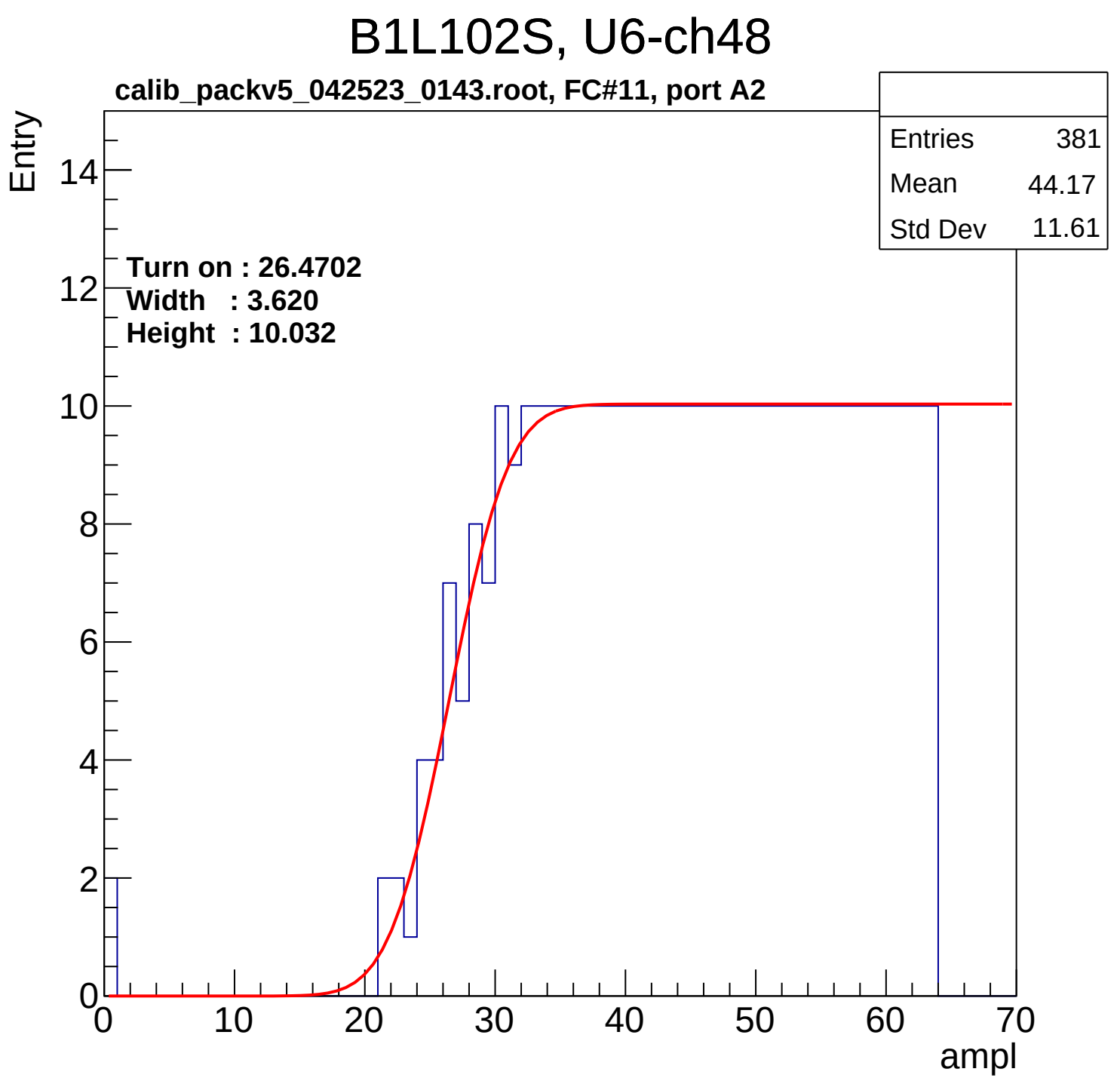
B1L102S, U6-ch48
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.17
Std Dev 11.61
Turn on : 26.4702
Width : 3.620
Height : 10.032
Entry
ampl
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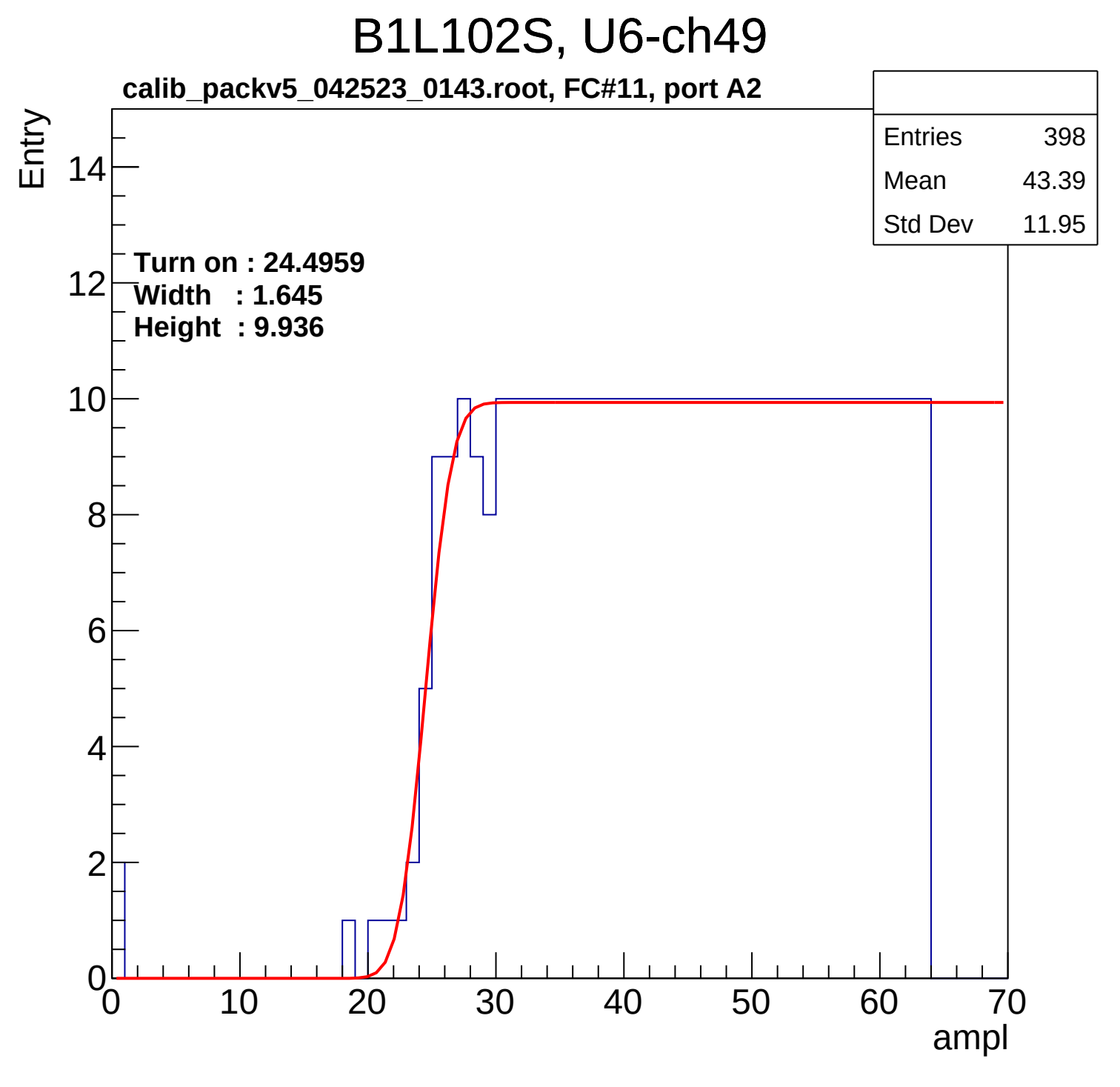
B1L102S, U6-ch49
calib_packv5_042523_0143.root, FC#11, port A2
Entries 398
Mean 43.39
Std Dev 11.95
Turn on : 24.4959
Width : 1.645
Height : 9.936
Entry
ampl
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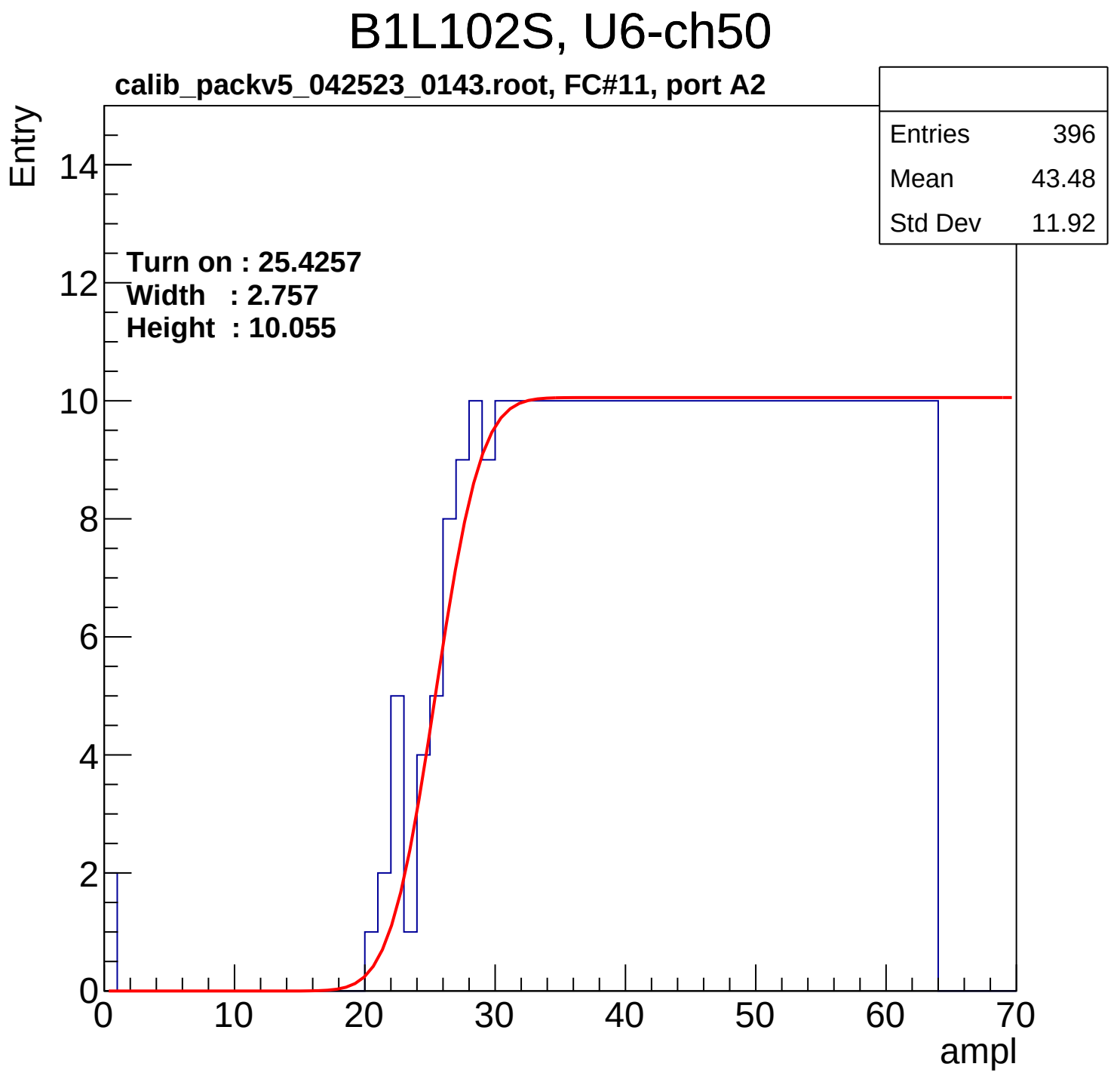
B1L102S, U6-ch50
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.48
Std Dev 11.92
Turn on : 25.4257
Width : 2.757
Height : 10.055
Entry
ampl
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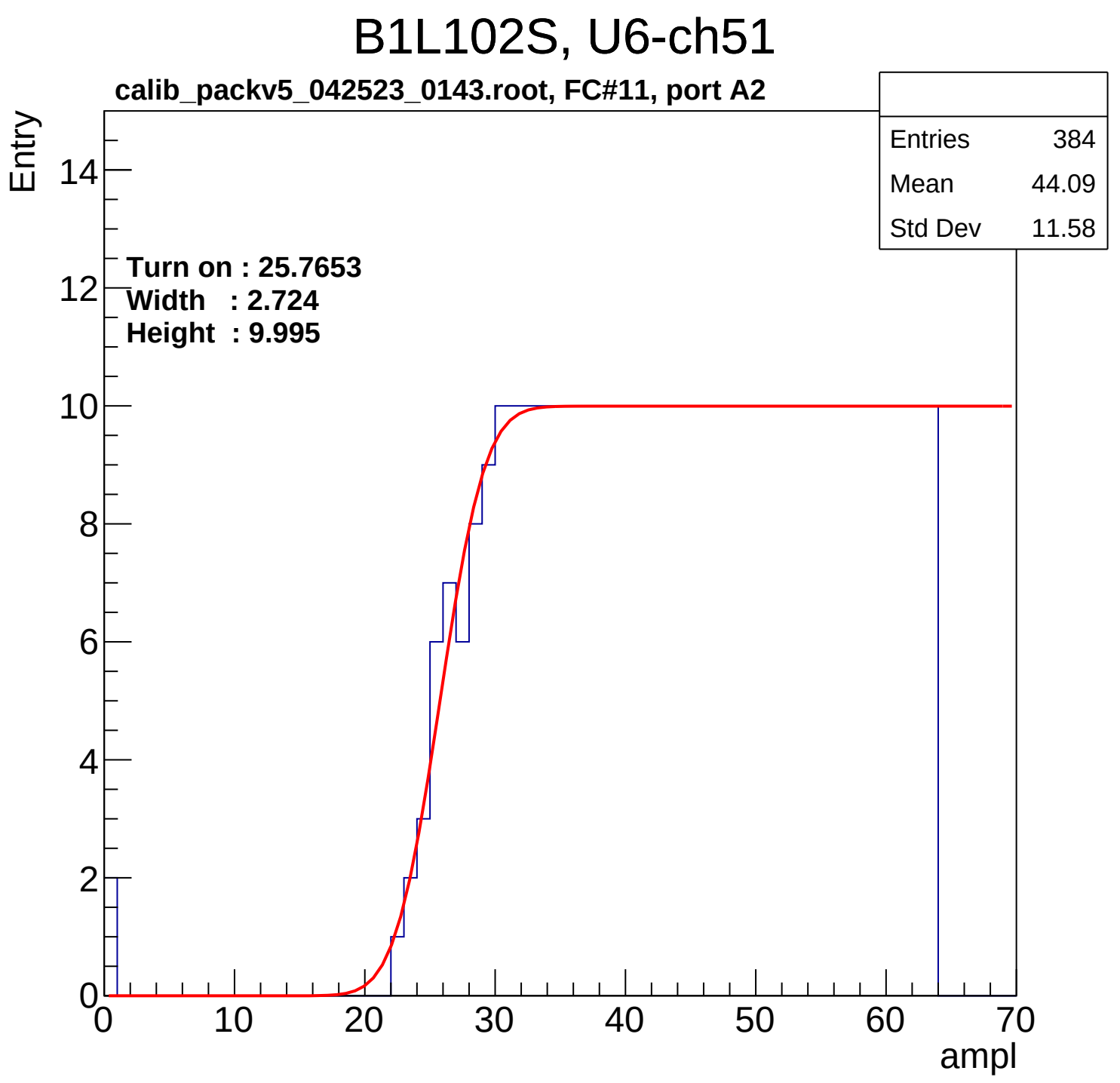
B1L102S, U6-ch51
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.09
Std Dev 11.58
Turn on : 25.7653
Width : 2.724
Height : 9.995
Entry
ampl
0
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4
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8
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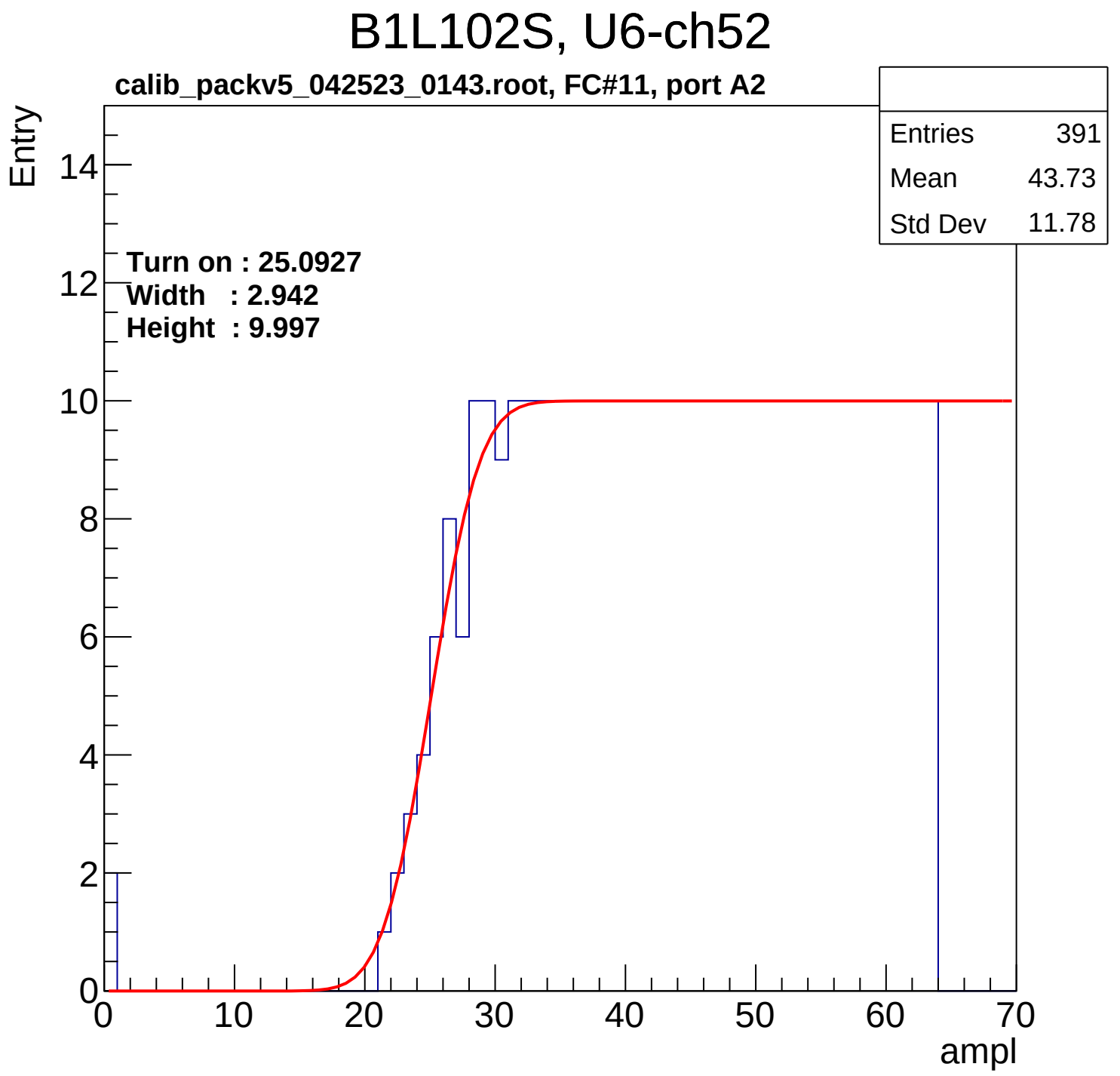
B1L102S, U6-ch52
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.73
Std Dev 11.78
Turn on : 25.0927
Width : 2.942
Height : 9.997
Entry
ampl
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4
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8
10
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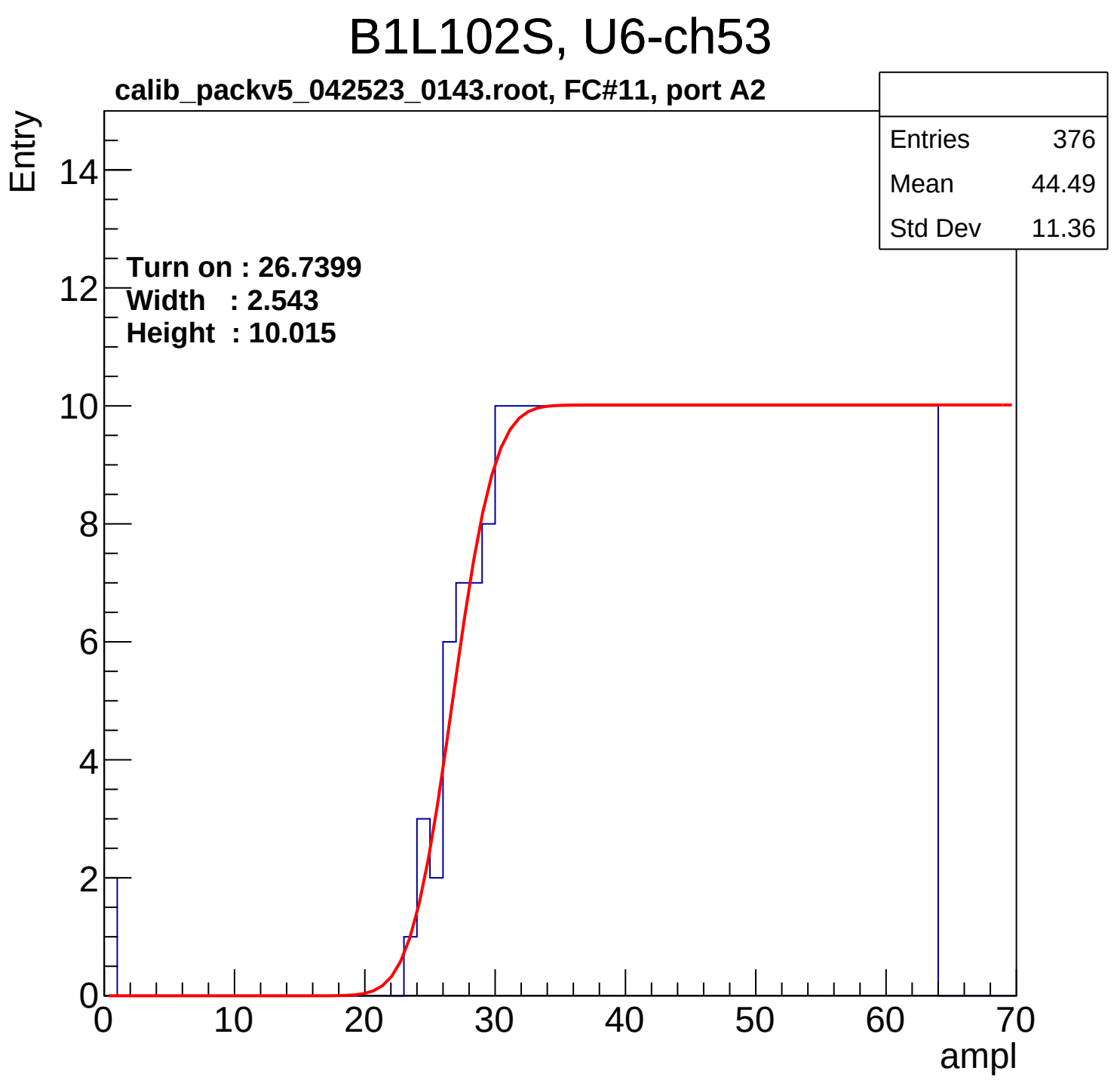
B1L102S, U6-ch53
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.49
Std Dev 11.36
Turn on : 26.7399
Width : 2.543
Height : 10.015
Entry
ampl
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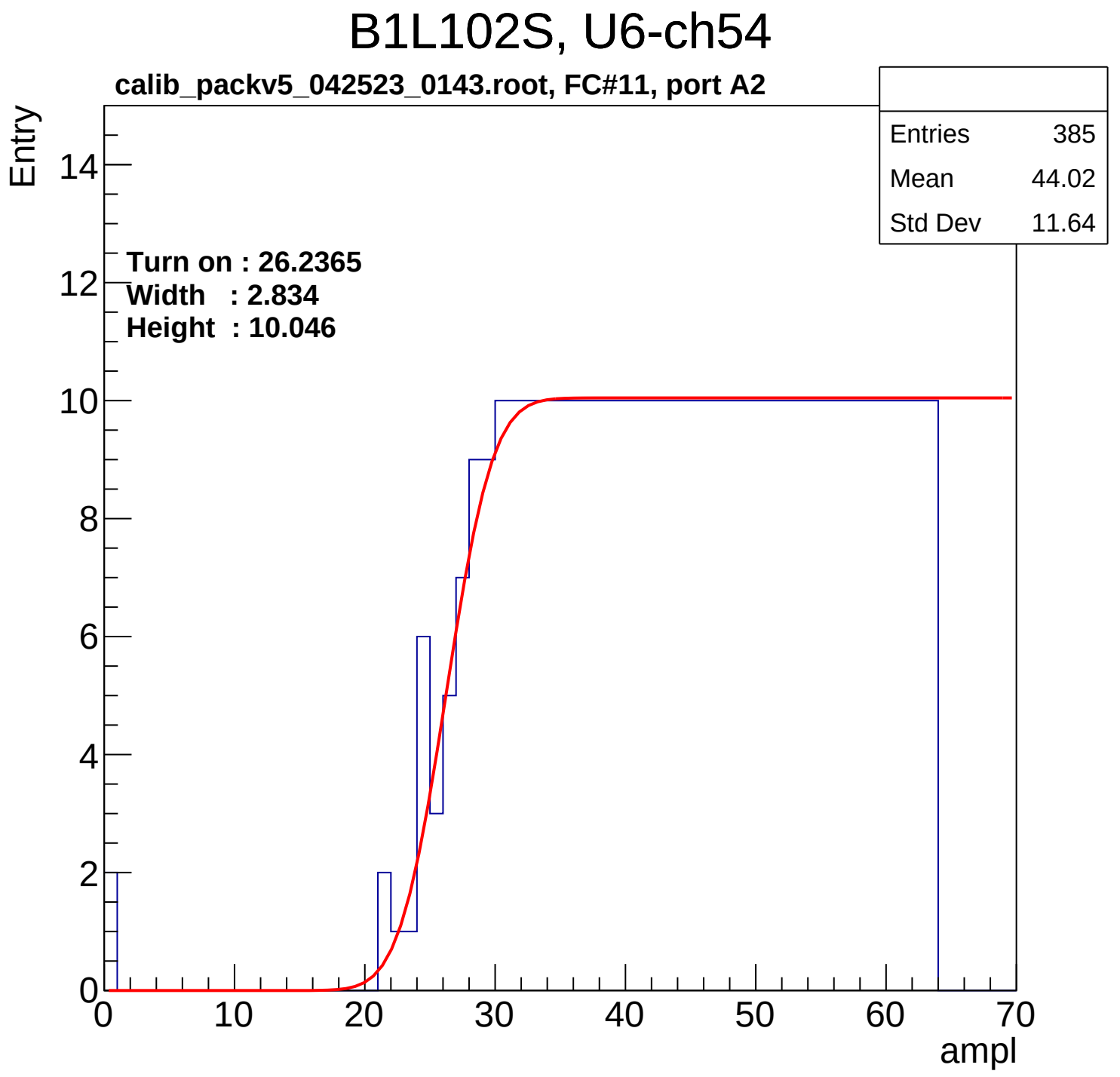
B1L102S, U6-ch54
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 44.02
Std Dev 11.64
Turn on : 26.2365
Width : 2.834
Height : 10.046
Entry
ampl
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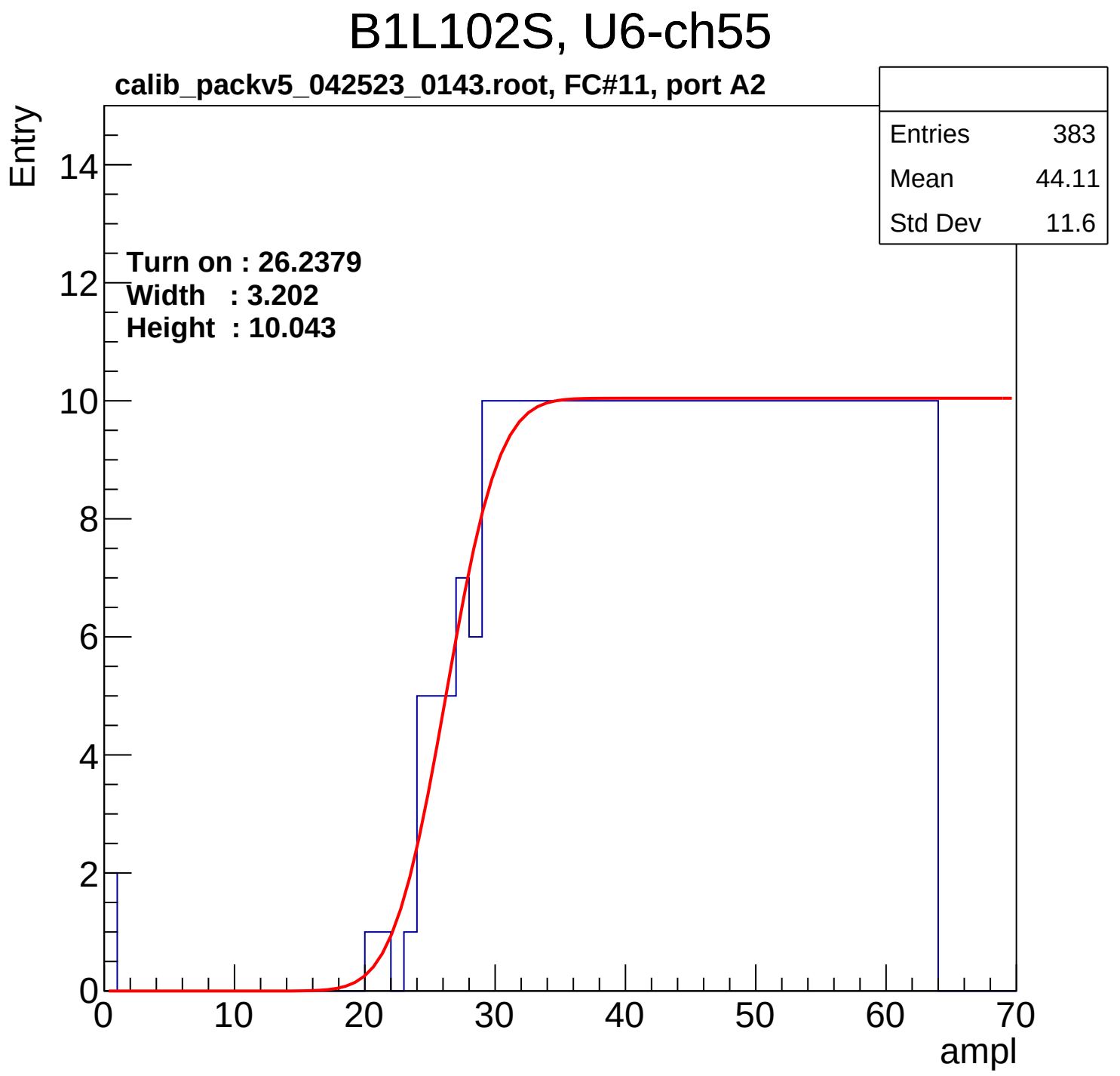
B1L102S, U6-ch55
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.11
Std Dev 11.6
Turn on : 26.2379
Width : 3.202
Height : 10.043
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ampl
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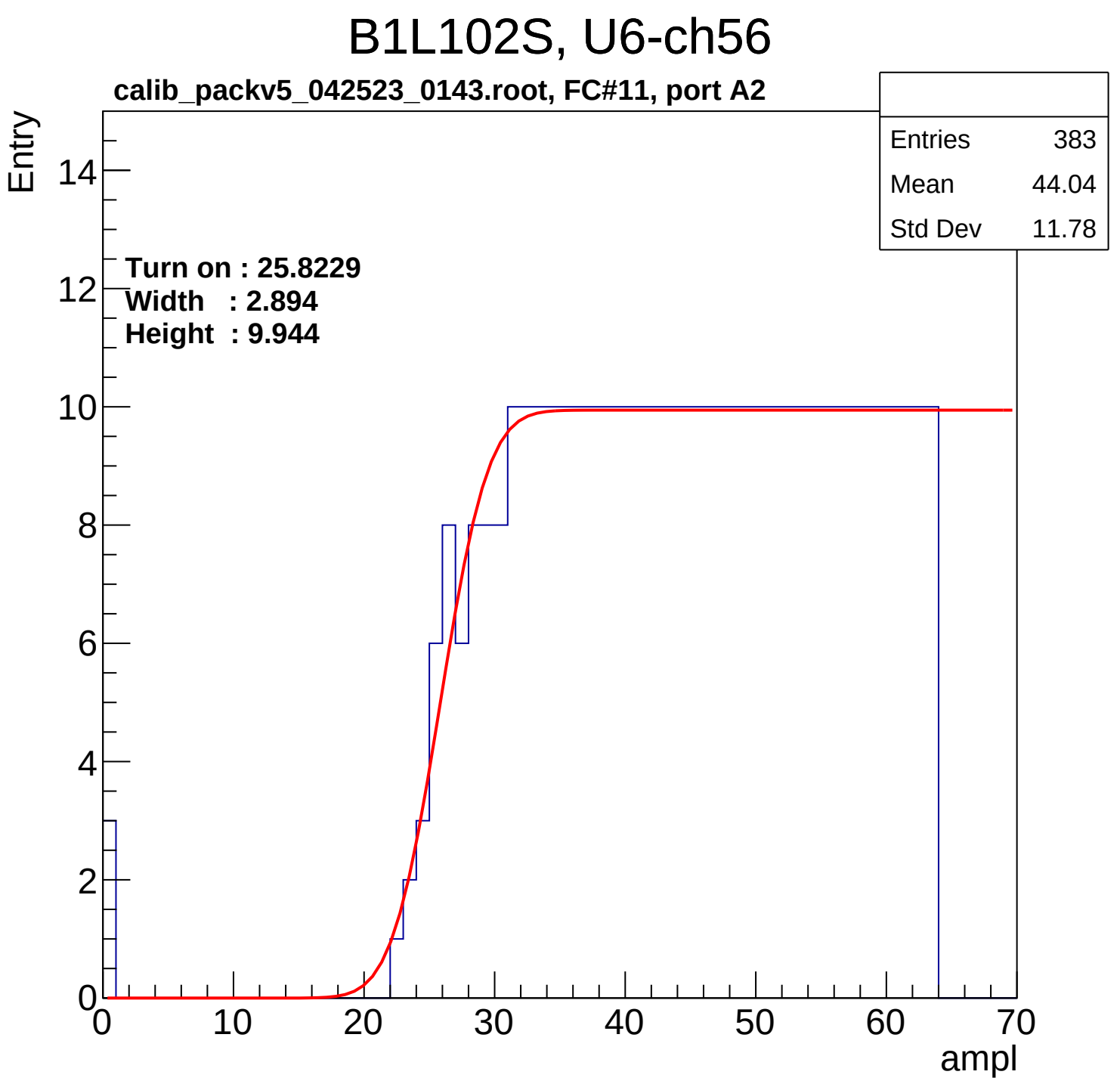
B1L102S, U6-ch56
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.04
Std Dev 11.78
Turn on : 25.8229
Width : 2.894
Height : 9.944
Entry
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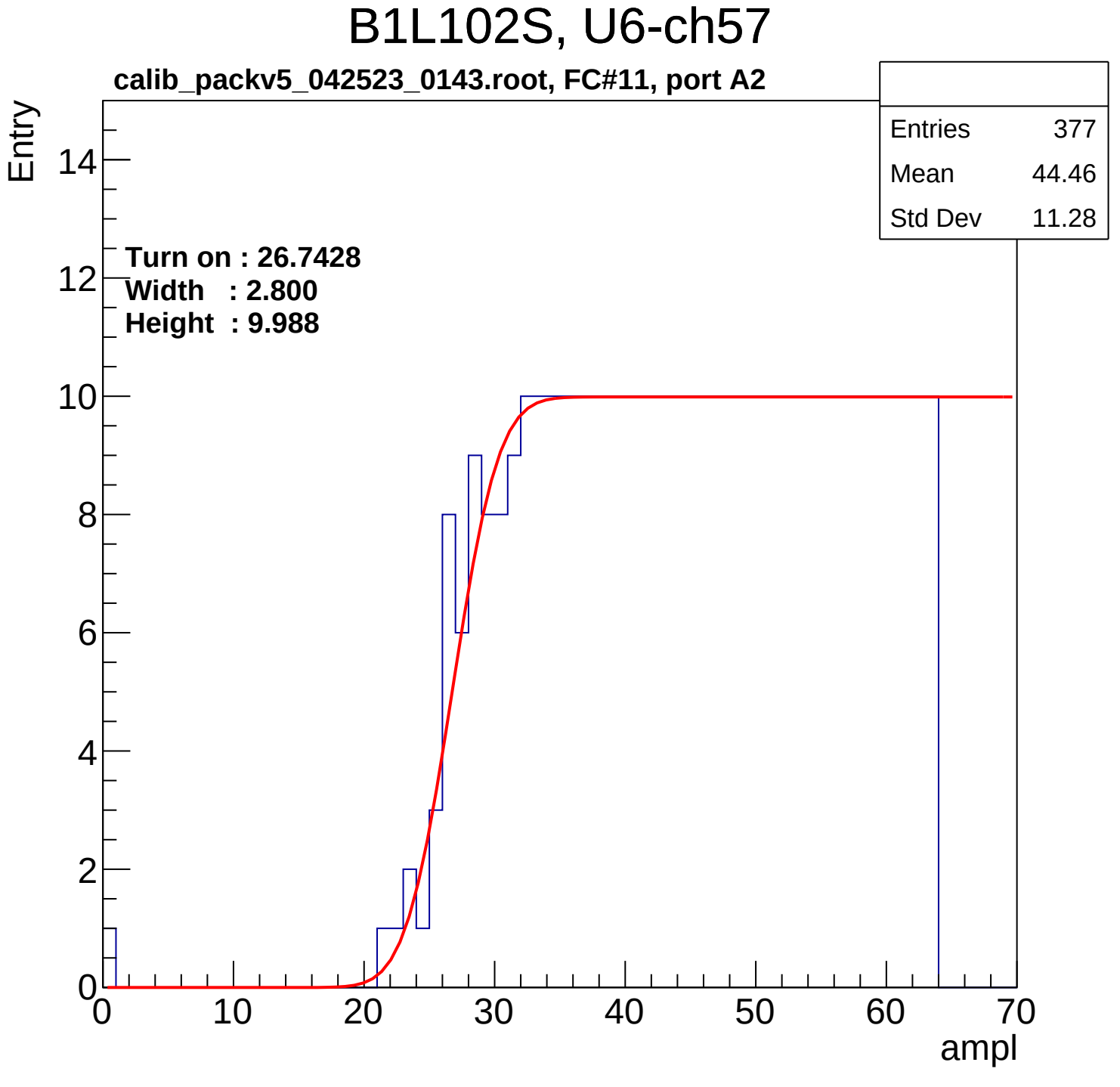
B1L102S, U6-ch57
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.46
Std Dev 11.28
Turn on : 26.7428
Width : 2.800
Height : 9.988
Entry
ampl
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4
6
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12
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20
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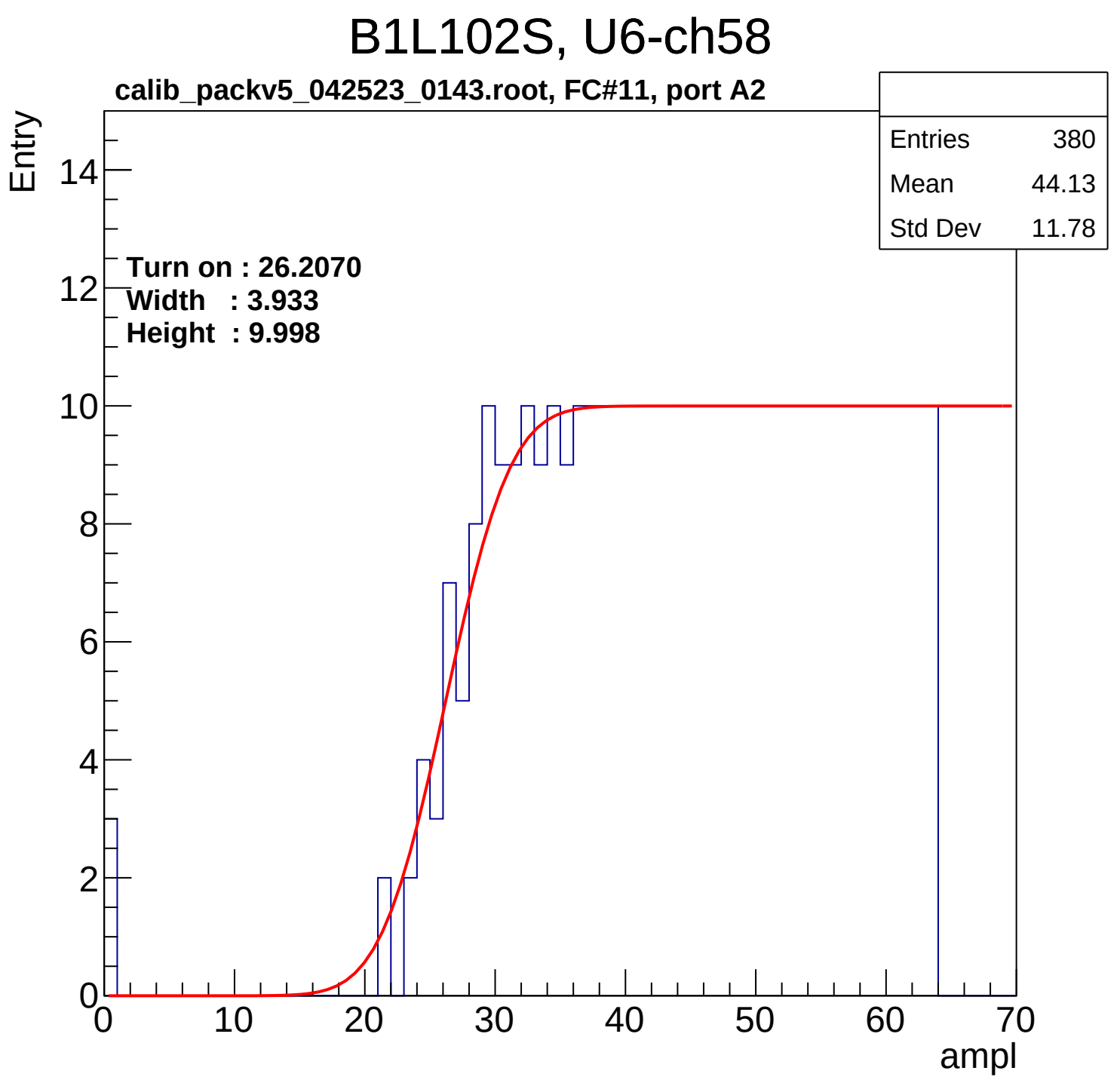
B1L102S, U6-ch58
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.13
Std Dev 11.78
Turn on : 26.2070
Width : 3.933
Height : 9.998
Entry
ampl
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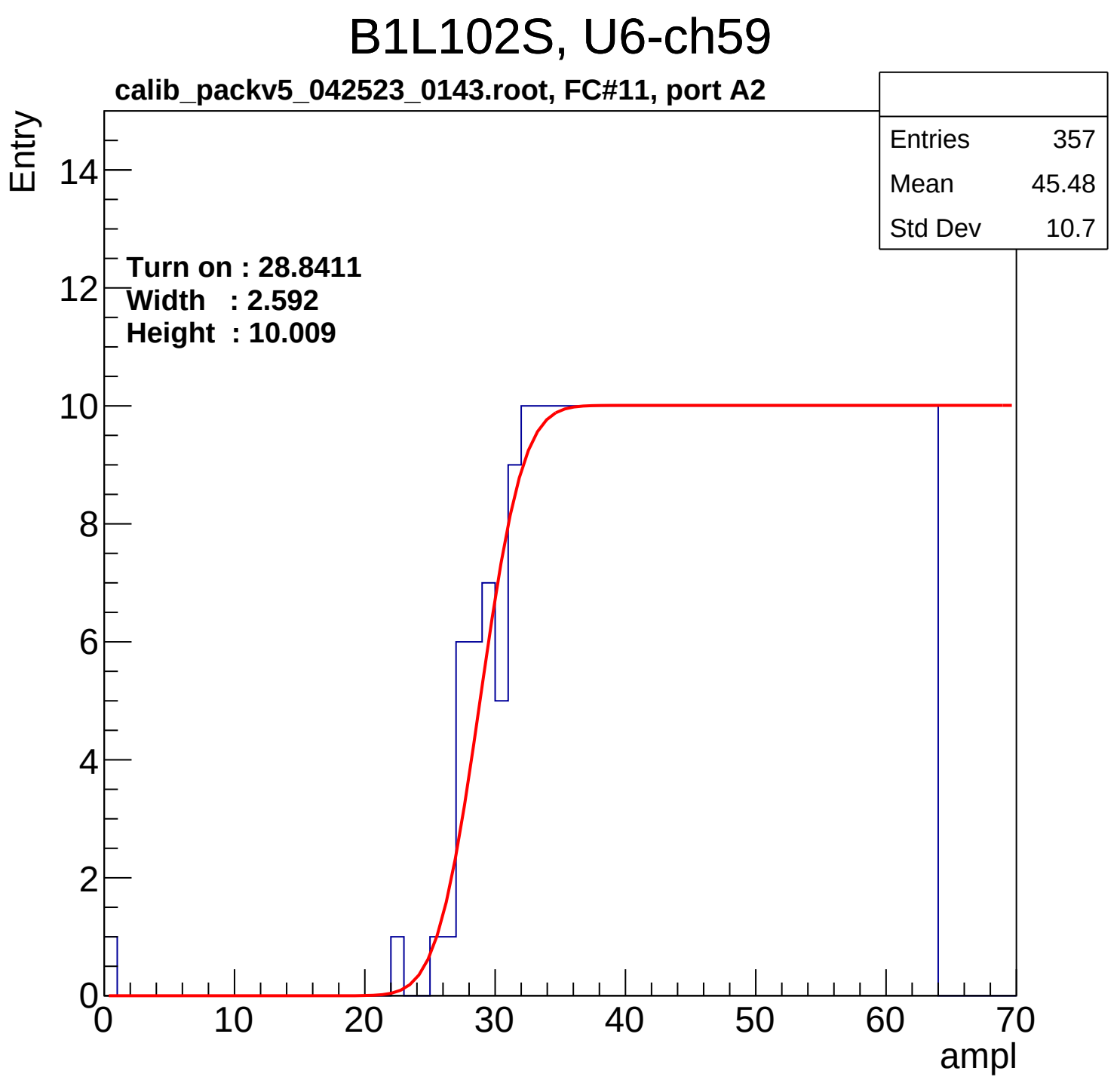
B1L102S, U6-ch59
calib_packv5_042523_0143.root, FC#11, port A2
Entries 357
Mean 45.48
Std Dev 10.7
Turn on : 28.8411
Width : 2.592
Height : 10.009
Entry
ampl
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4
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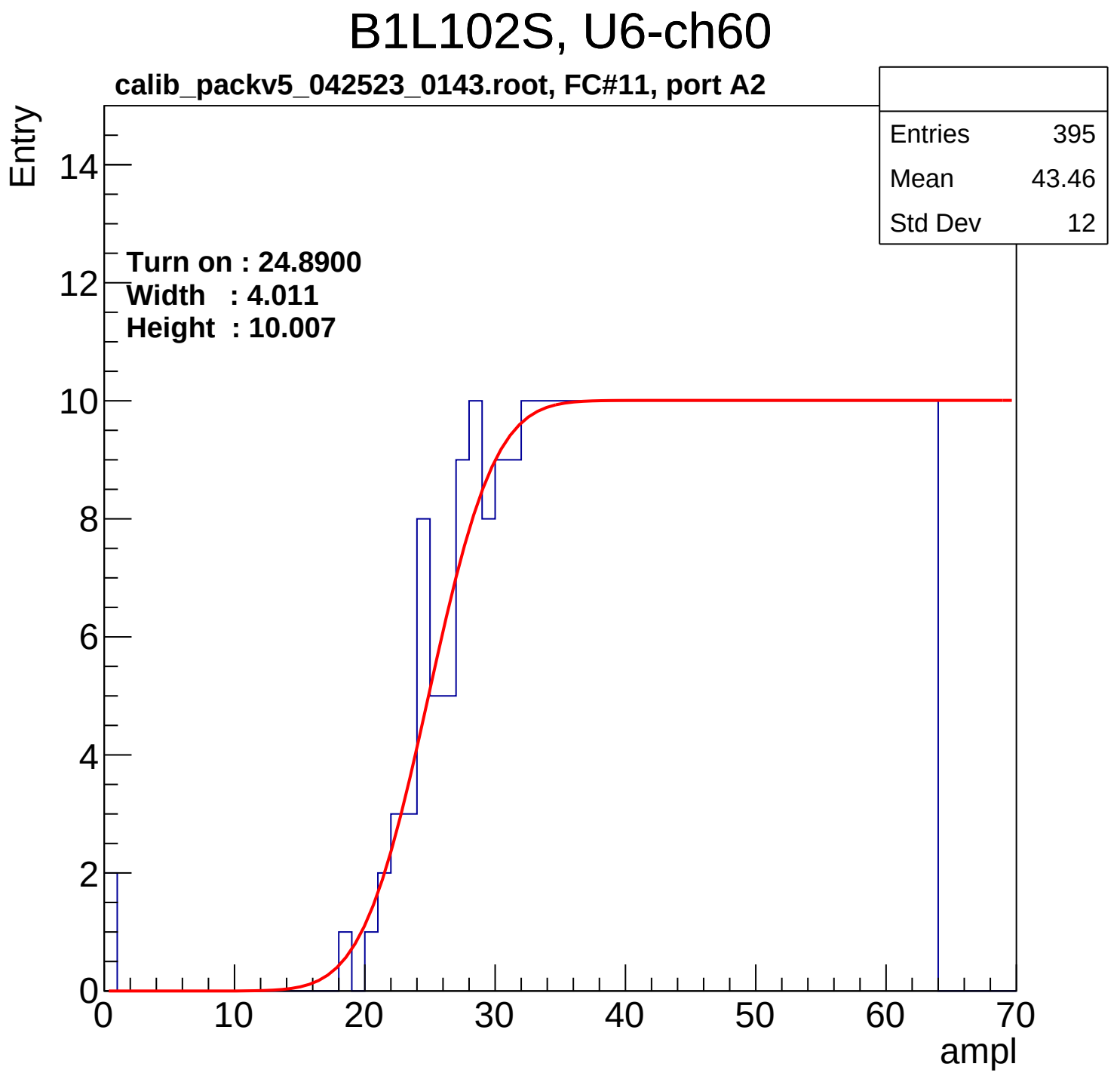
B1L102S, U6-ch60
calib_packv5_042523_0143.root, FC#11, port A2
Entries 395
Mean 43.46
Std Dev 12
Turn on : 24.8900
Width : 4.011
Height : 10.007
Entry
ampl
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2
4
6
8
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12
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0
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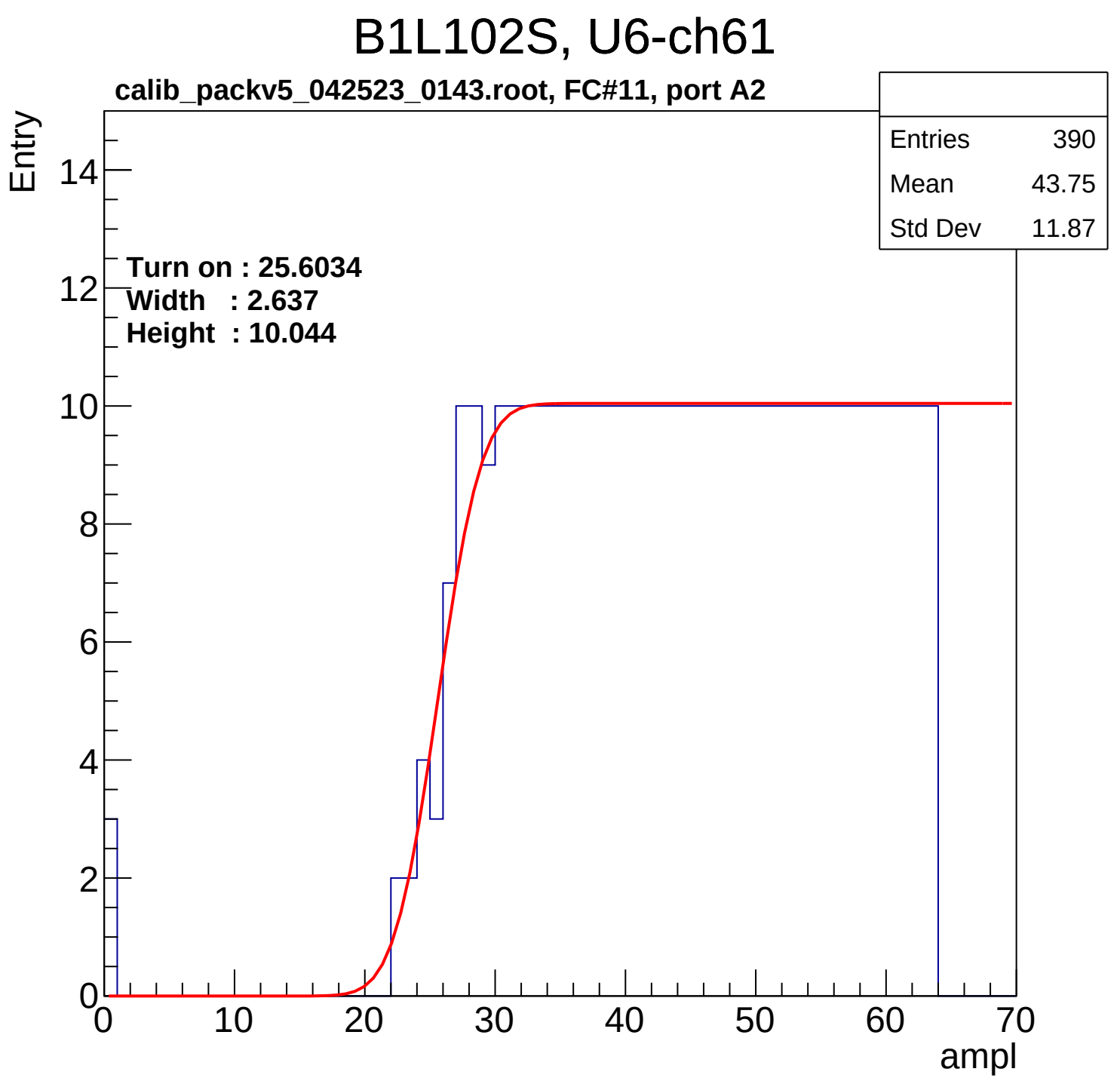
B1L102S, U6-ch61
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.75
Std Dev 11.87
Turn on : 25.6034
Width : 2.637
Height : 10.044
Entry
ampl
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2
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6
8
10
12
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0
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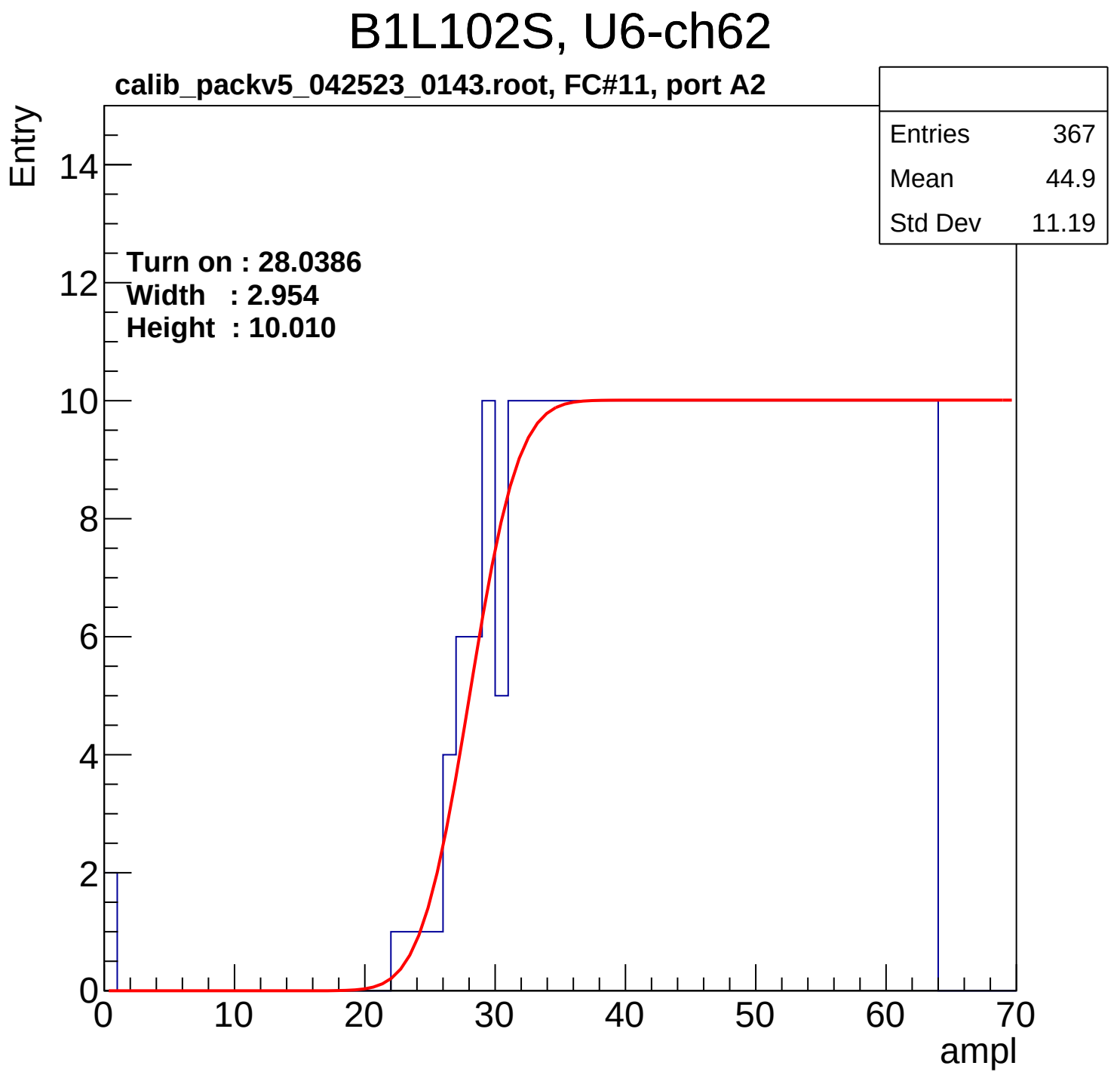
B1L102S, U6-ch62
calib_packv5_042523_0143.root, FC#11, port A2
Entries 367
Mean 44.9
Std Dev 11.19
Turn on : 28.0386
Width : 2.954
Height : 10.010
Entry
ampl
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2
4
6
8
10
12
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0
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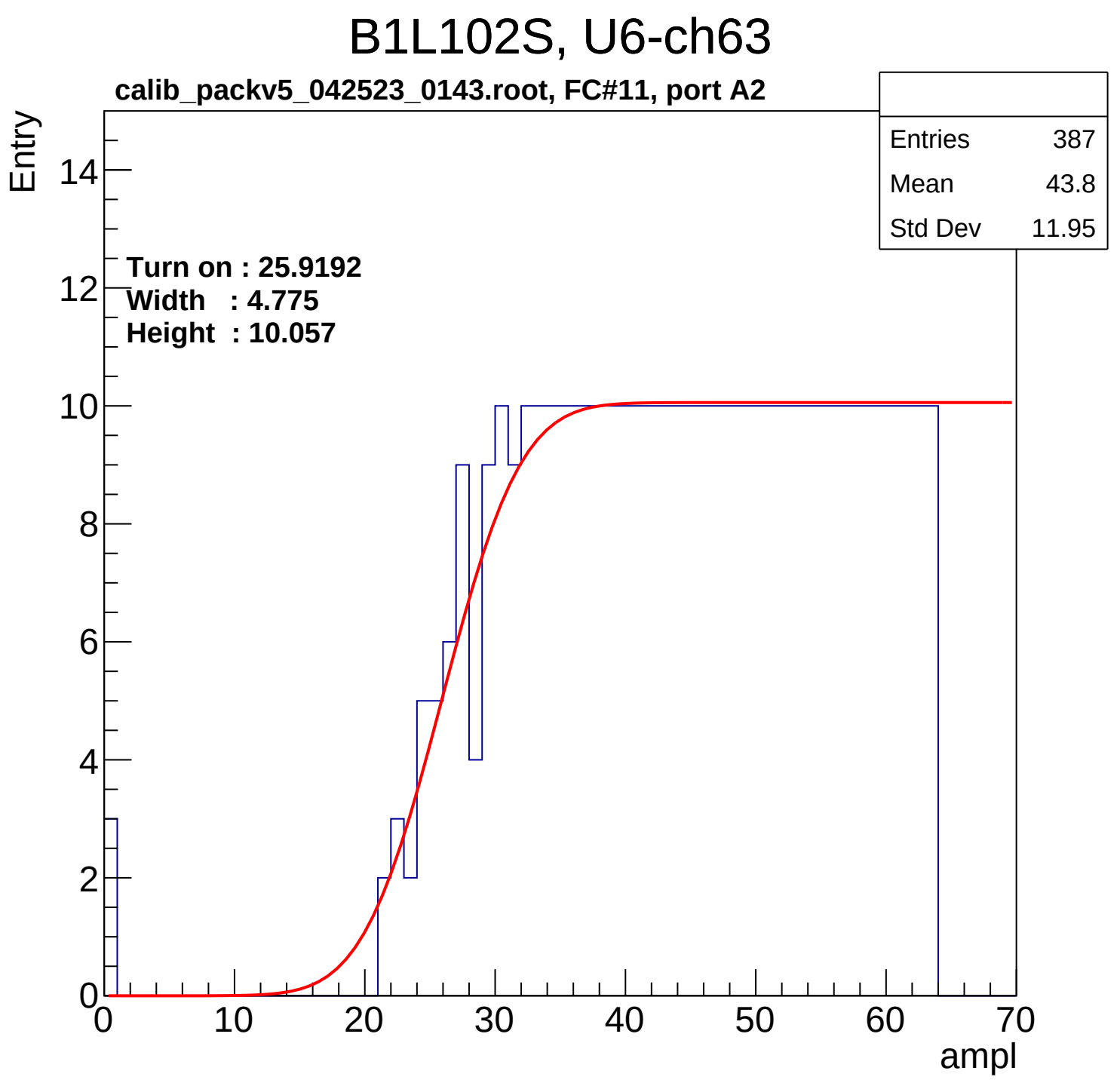
B1L102S, U6-ch63
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.8
Std Dev 11.95
Turn on : 25.9192
Width : 4.775
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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60
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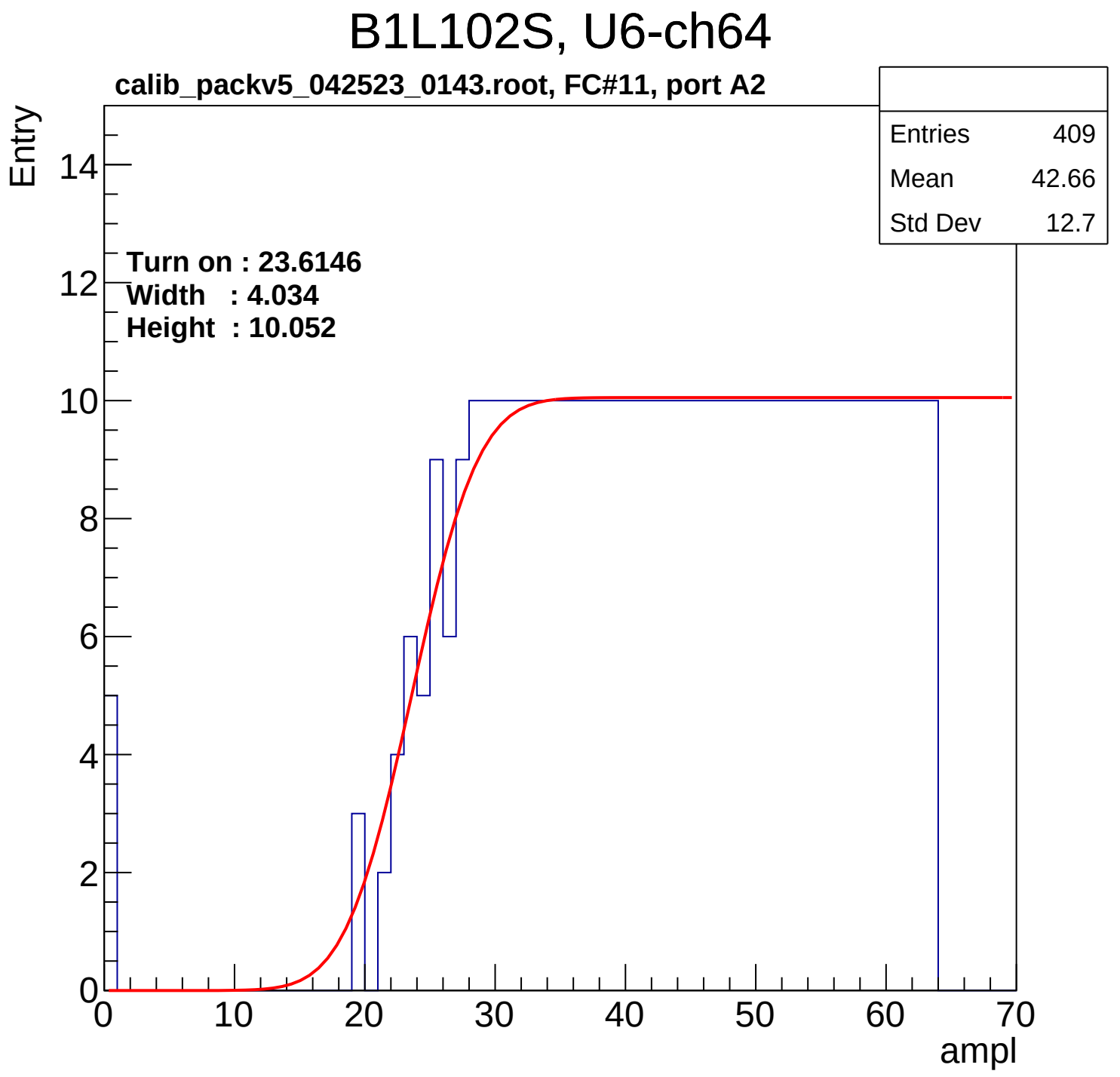
B1L102S, U6-ch64
calib_packv5_042523_0143.root, FC#11, port A2
Entries 409
Mean 42.66
Std Dev 12.7
Turn on : 23.6146
Width : 4.034
Height : 10.052
Entry
ampl
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6
8
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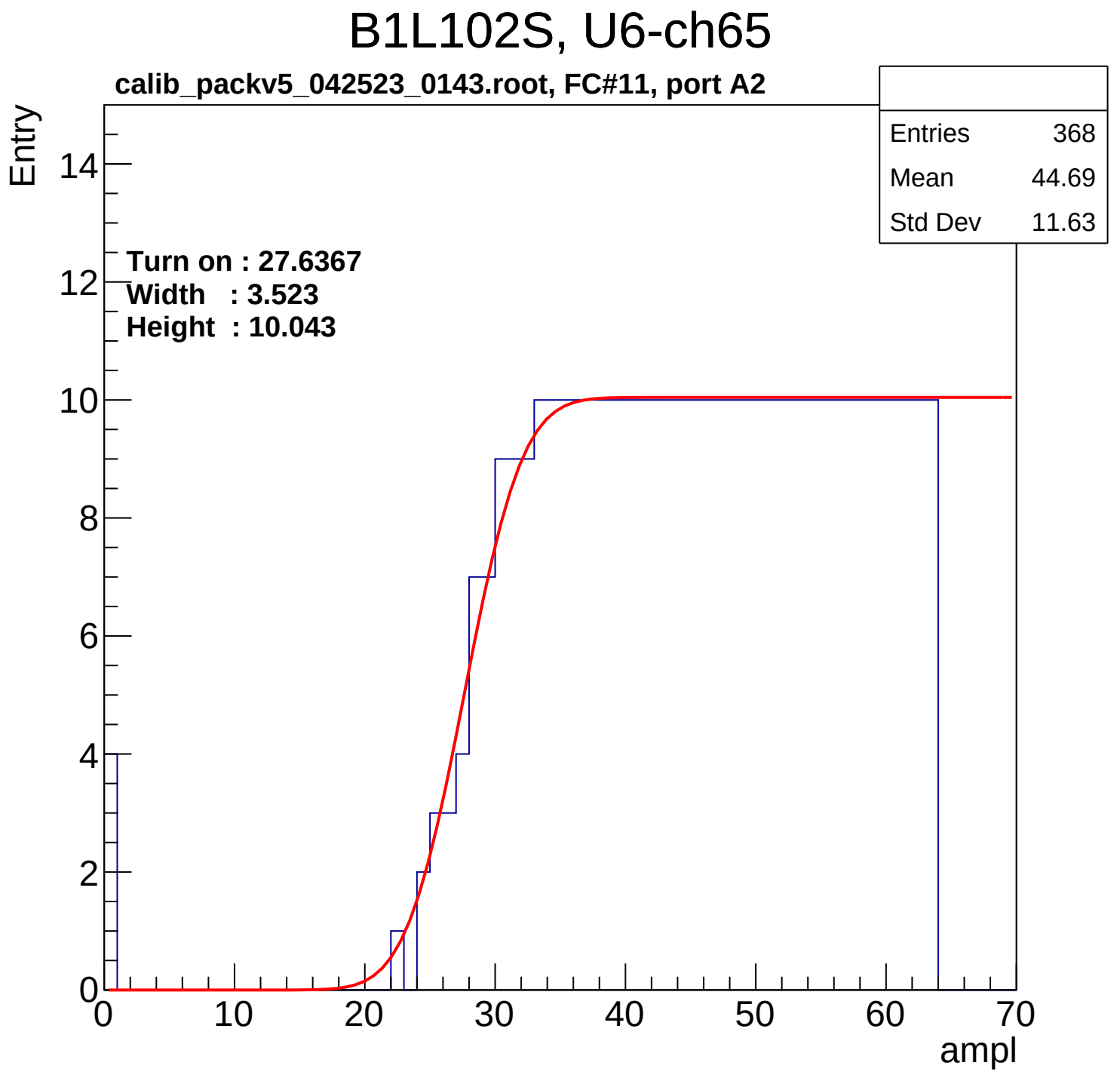
B1L102S, U6-ch65
calib_packv5_042523_0143.root, FC#11, port A2
Entries 368
Mean 44.69
Std Dev 11.63
Turn on : 27.6367
Width : 3.523
Height : 10.043
Entry
ampl
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2
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6
8
10
12
14
0
10
20
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60
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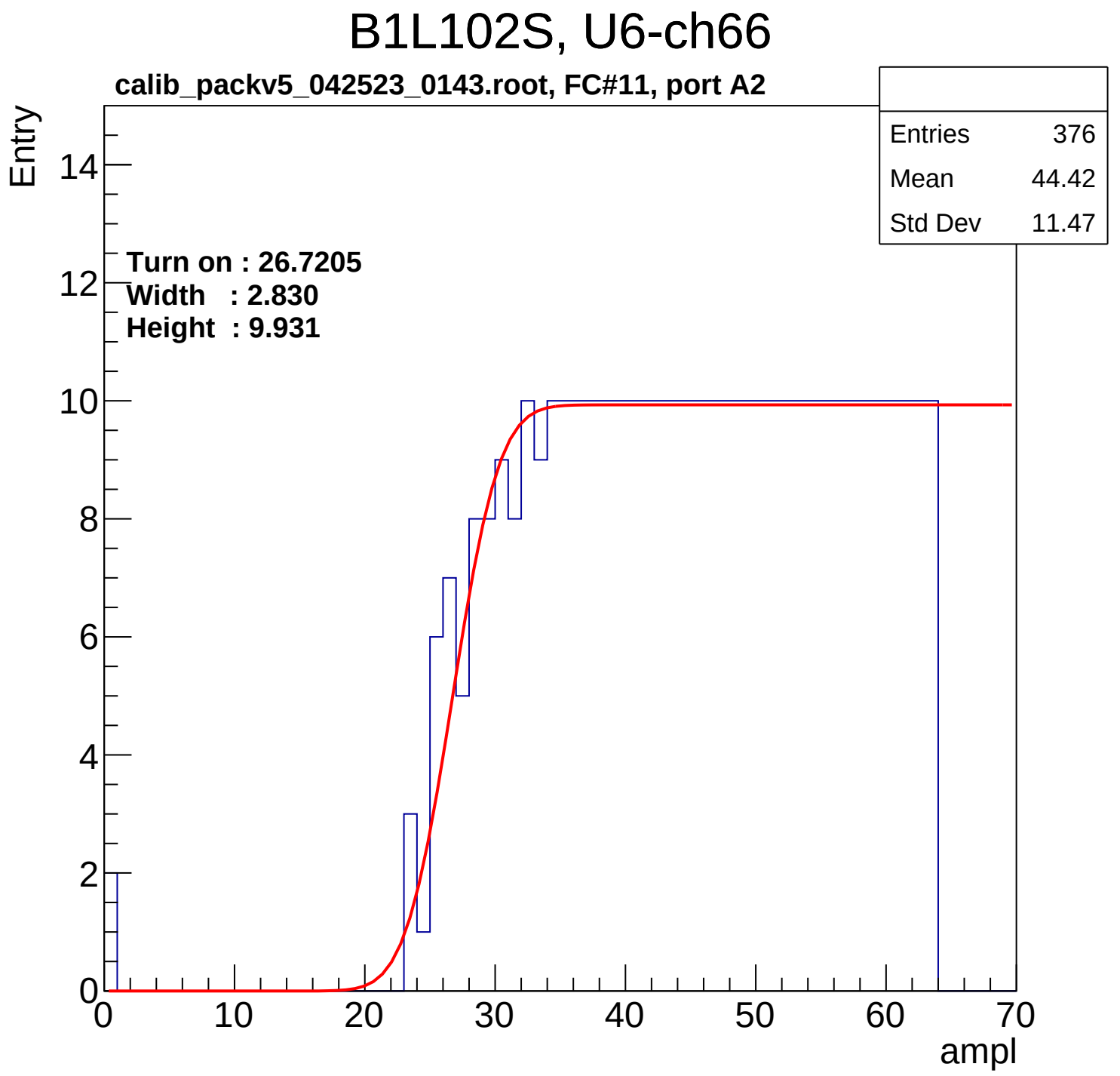
B1L102S, U6-ch66
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.42
Std Dev 11.47
Turn on : 26.7205
Width : 2.830
Height : 9.931
Entry
ampl
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8
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0
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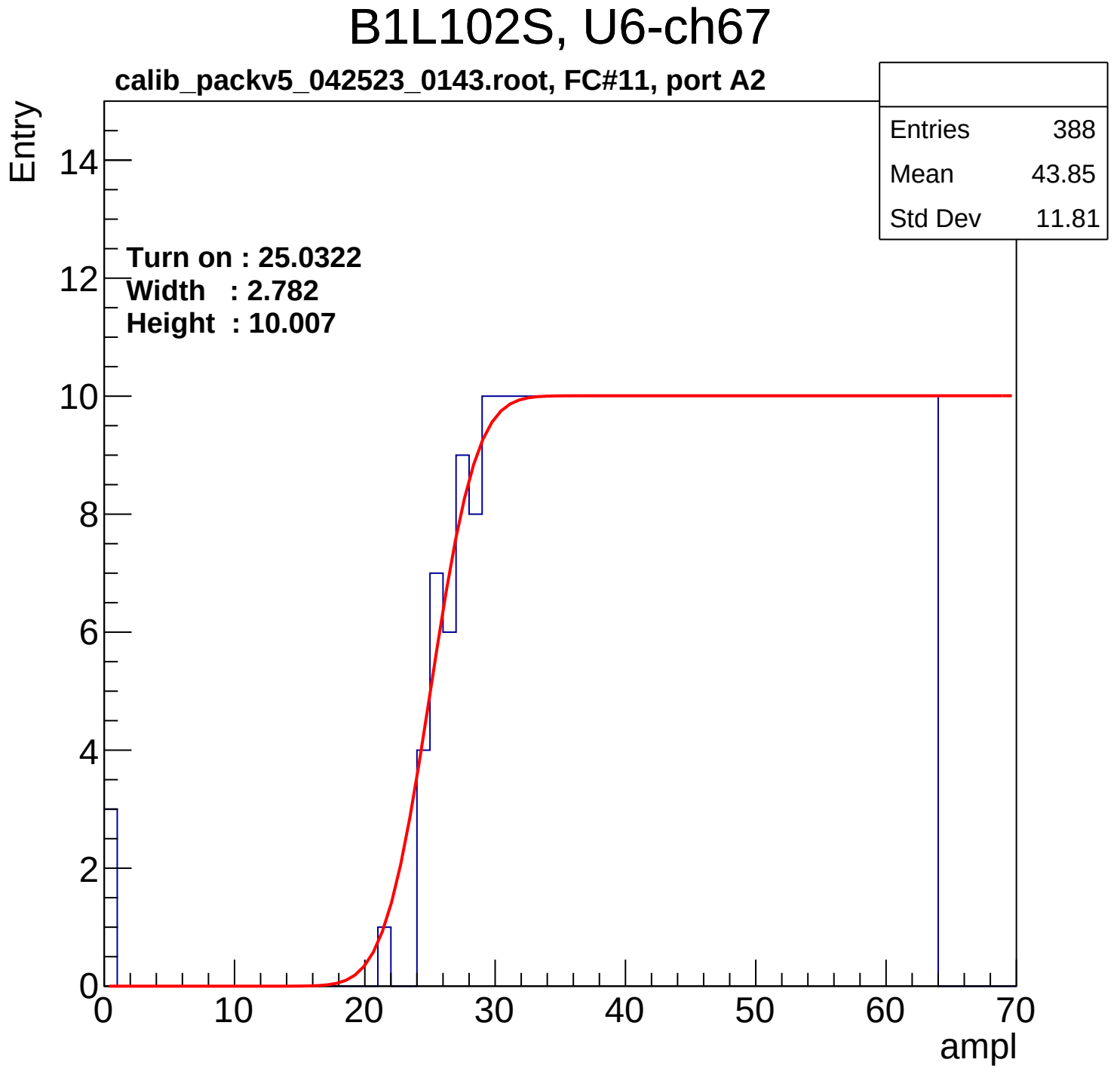
B1L102S, U6-ch67
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.85
Std Dev 11.81
Turn on : 25.0322
Width : 2.782
Height : 10.007
Entry
ampl
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4
6
8
10
12
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0
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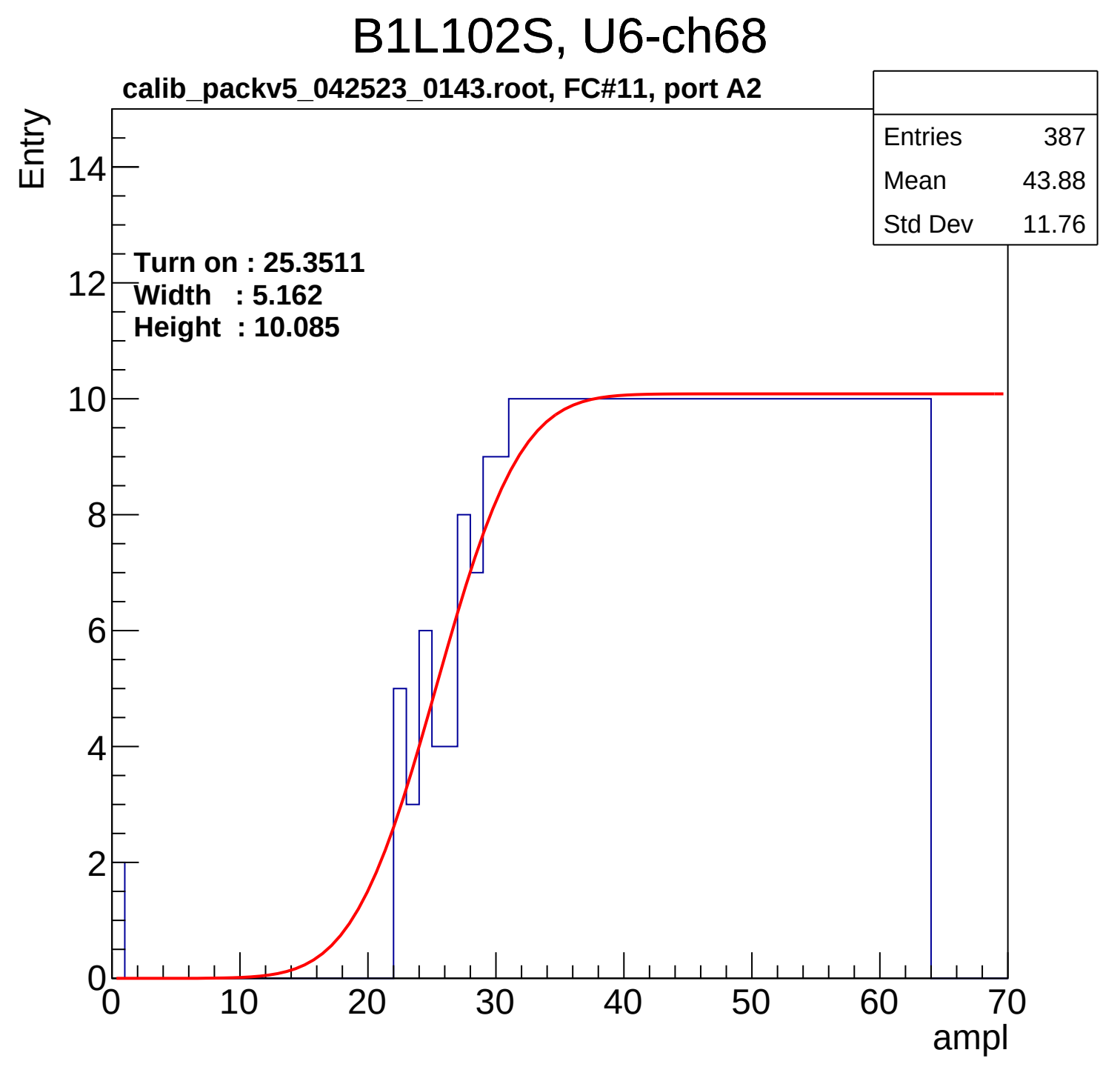
B1L102S, U6-ch68
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.88
Std Dev 11.76
Turn on : 25.3511
Width : 5.162
Height : 10.085
Entry
ampl
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4
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8
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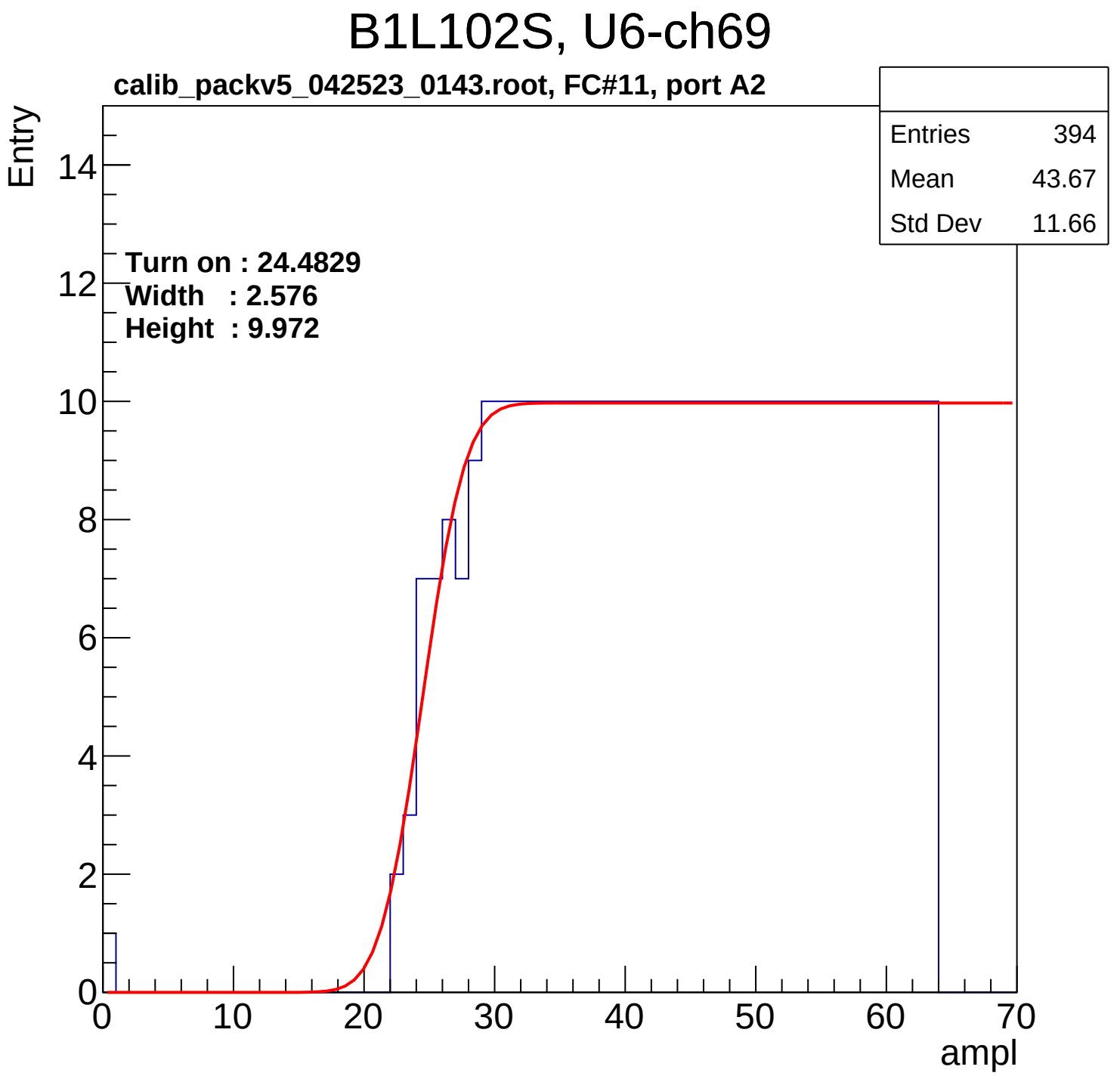
B1L102S, U6-ch69
calib_packv5_042523_0143.root, FC#11, port A2
Entries 394
Mean 43.67
Std Dev 11.66
Turn on : 24.4829
Width : 2.576
Height : 9.972
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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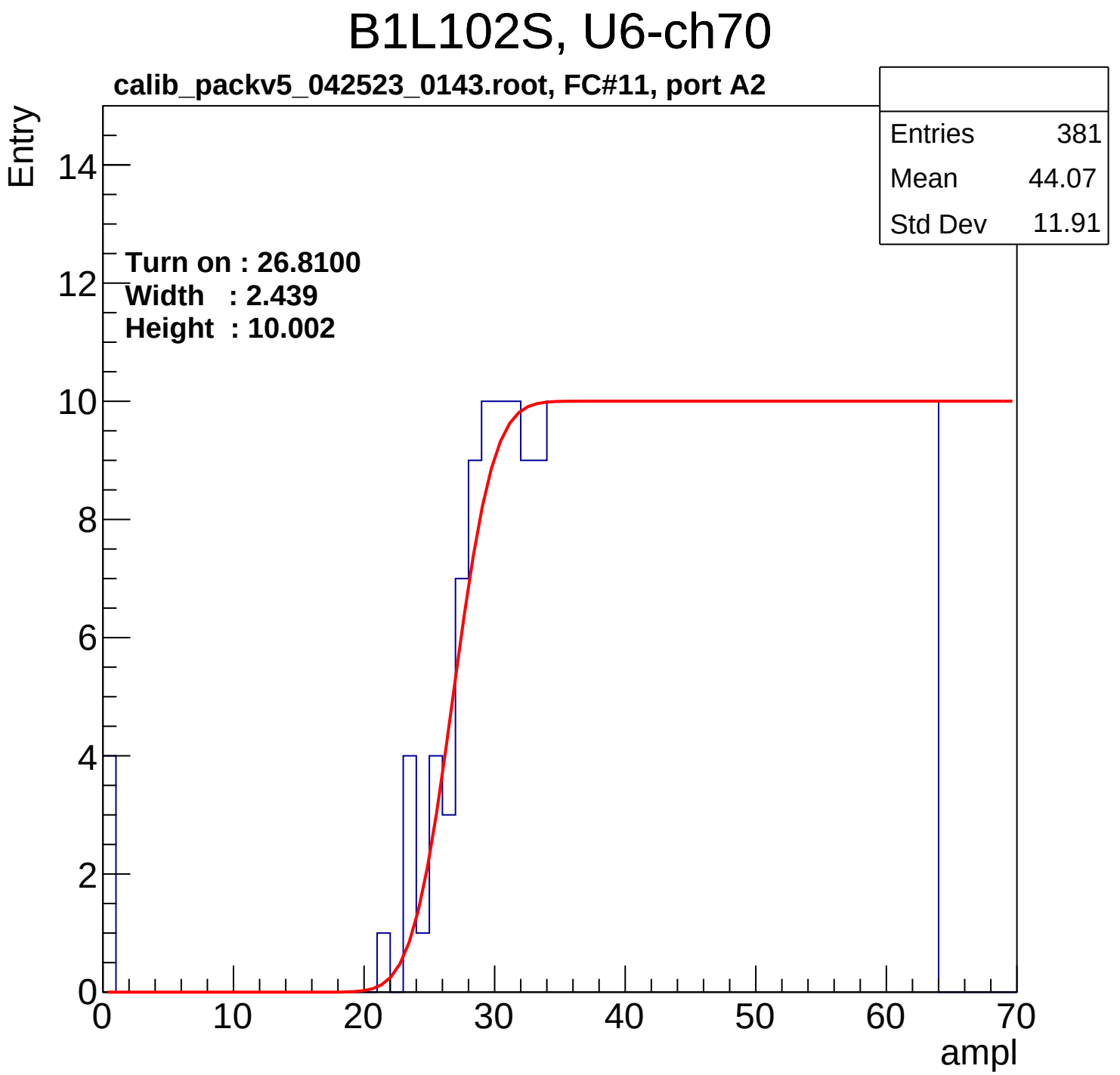
B1L102S, U6-ch70
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.07
Std Dev 11.91
Turn on : 26.8100
Width : 2.439
Height : 10.002
Entry
ampl
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6
8
10
12
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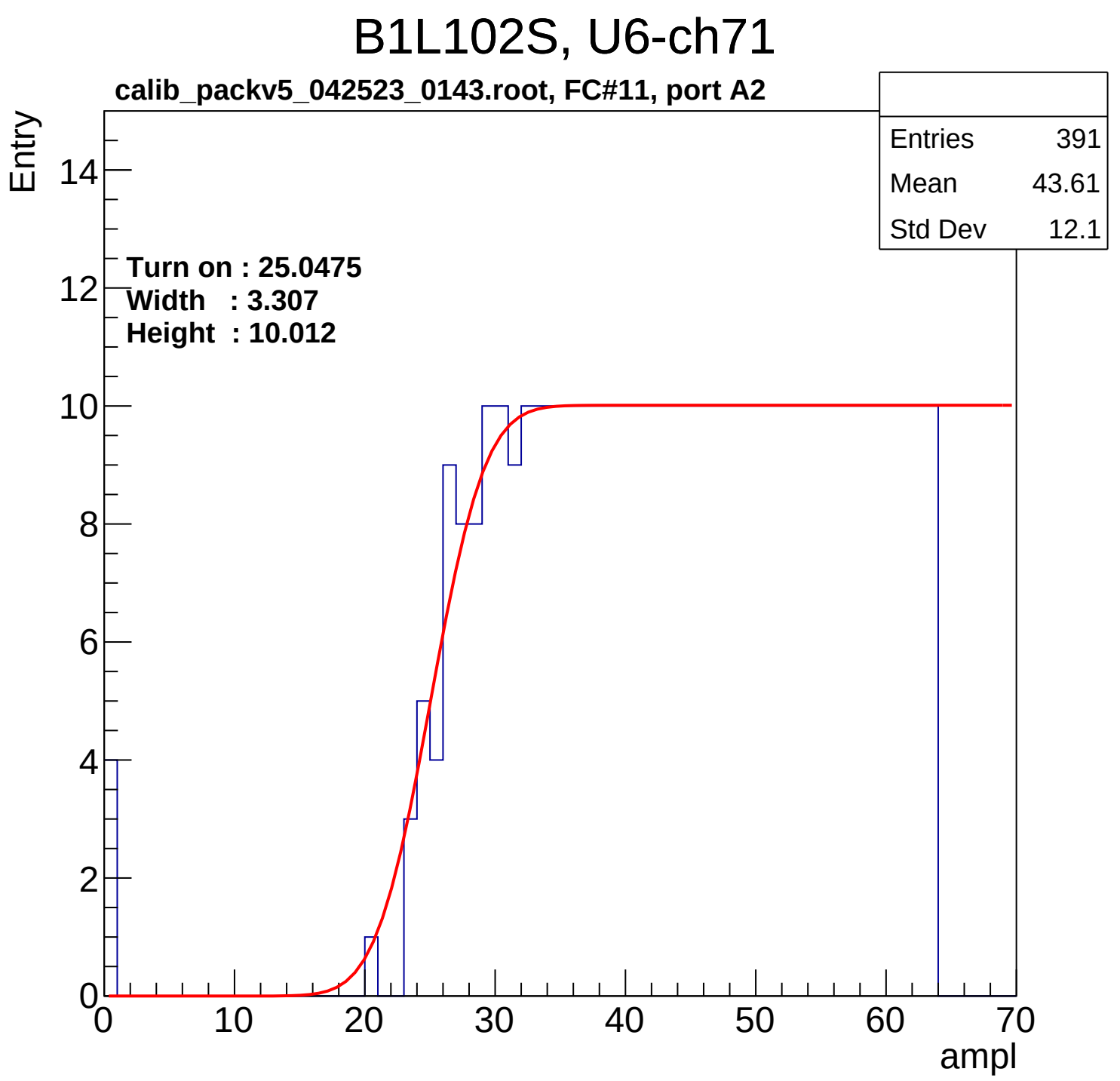
B1L102S, U6-ch71
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.61
Std Dev 12.1
Turn on : 25.0475
Width : 3.307
Height : 10.012
Entry
ampl
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6
8
10
12
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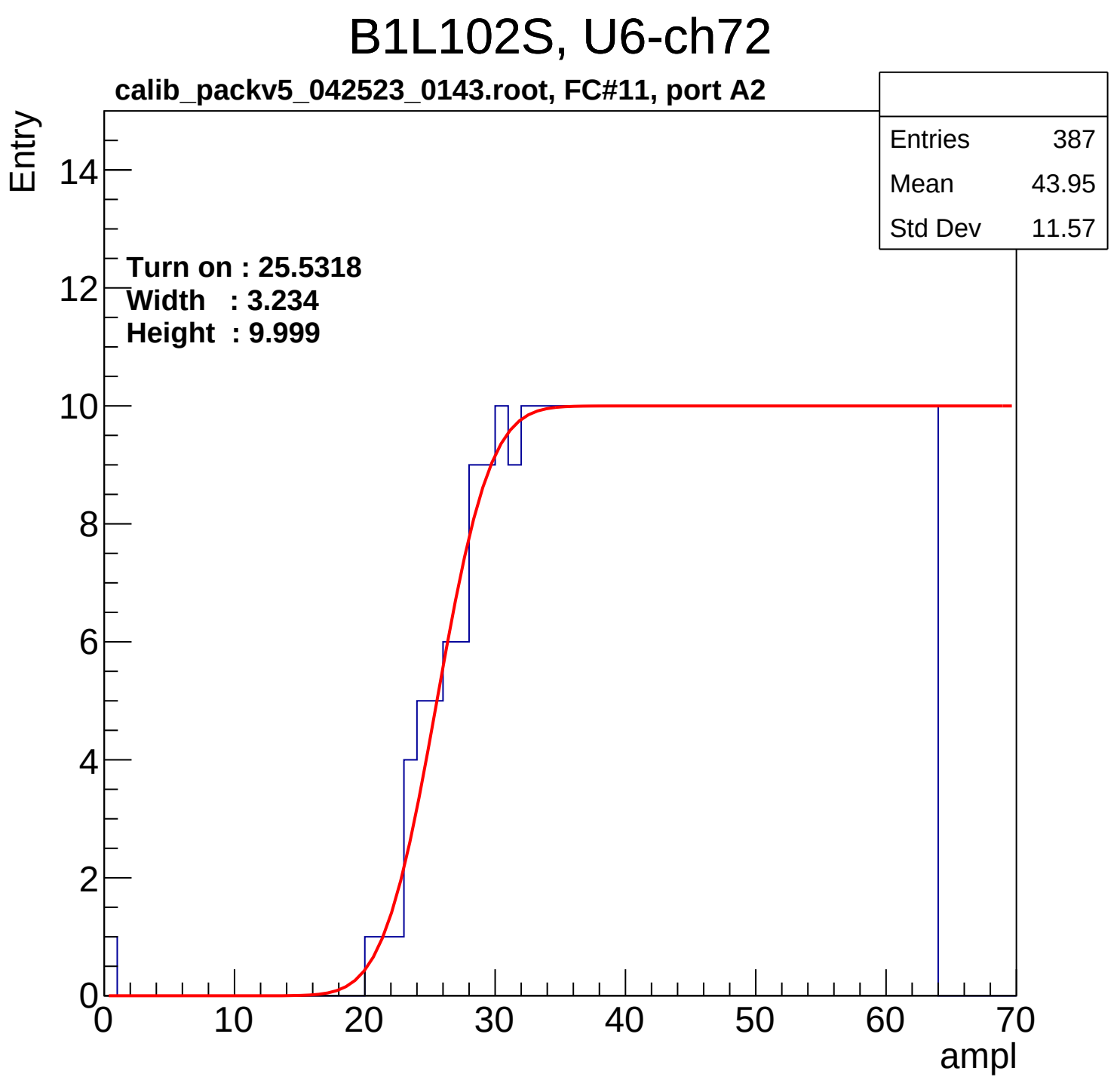
B1L102S, U6-ch72
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.95
Std Dev 11.57
Turn on : 25.5318
Width : 3.234
Height : 9.999
Entry
ampl
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6
8
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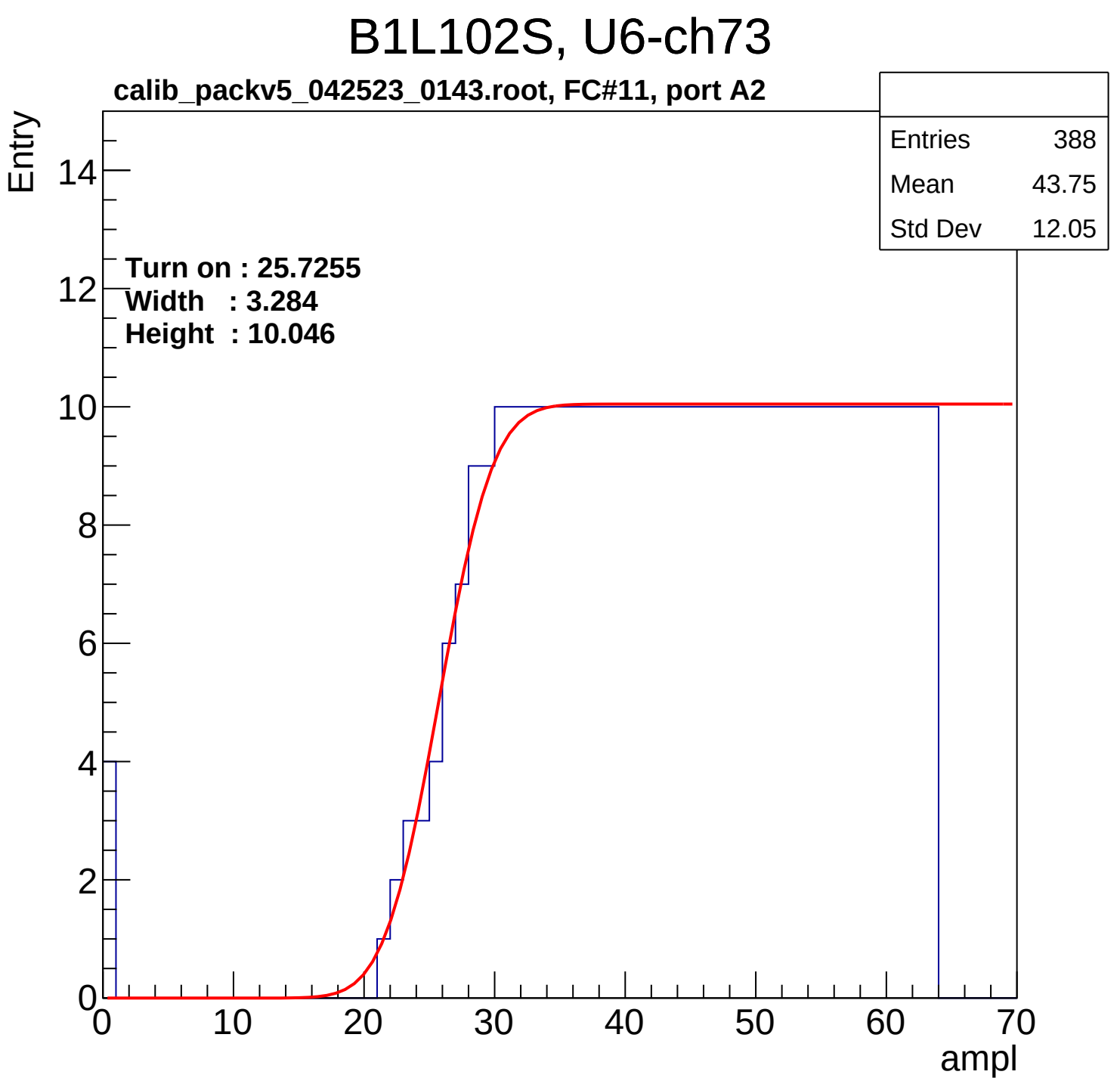
B1L102S, U6-ch73
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.75
Std Dev 12.05
Turn on : 25.7255
Width : 3.284
Height : 10.046
Entry
ampl
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10
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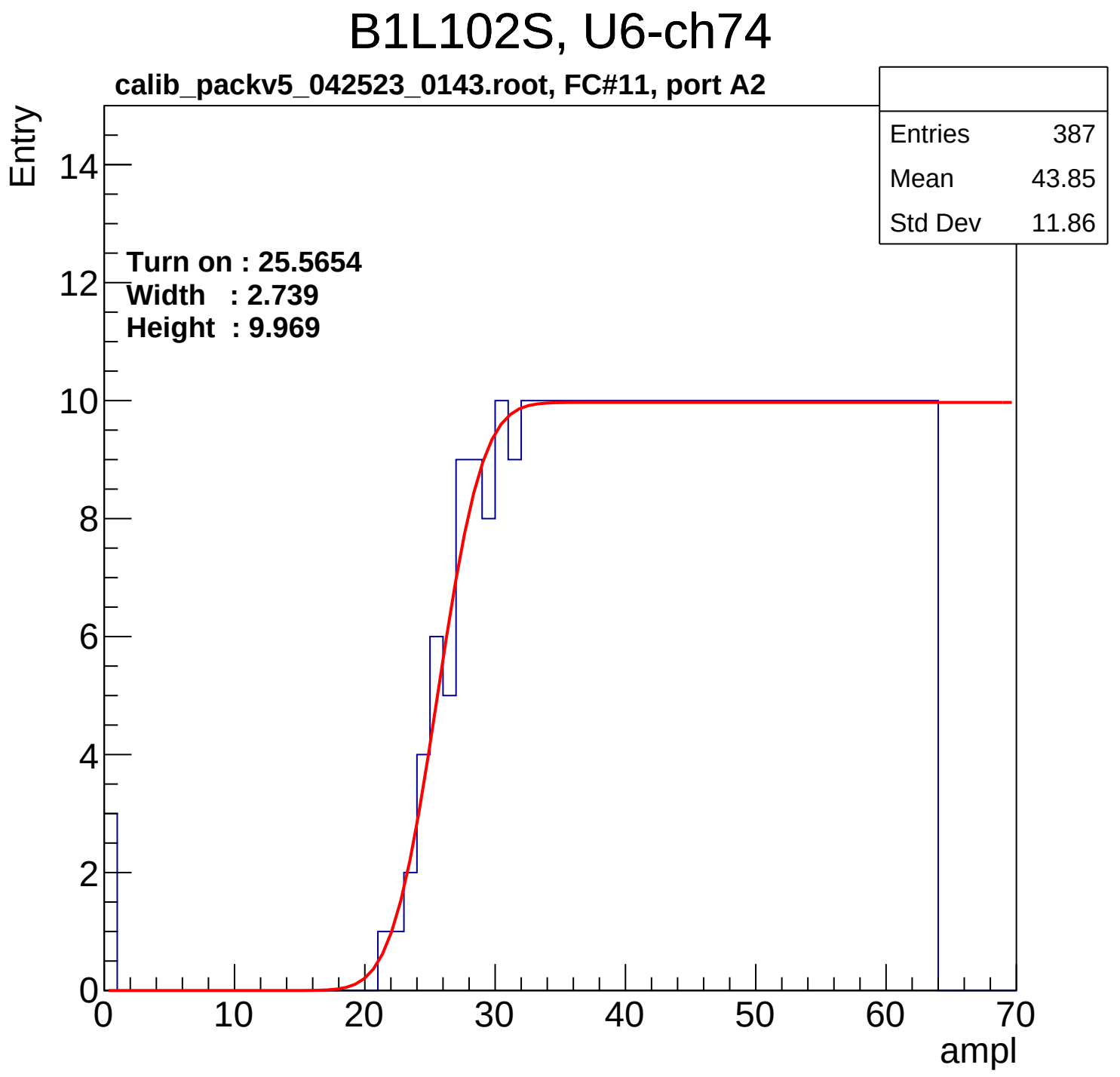
B1L102S, U6-ch74
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.85
Std Dev 11.86
Turn on : 25.5654
Width : 2.739
Height : 9.969
Entry
ampl
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8
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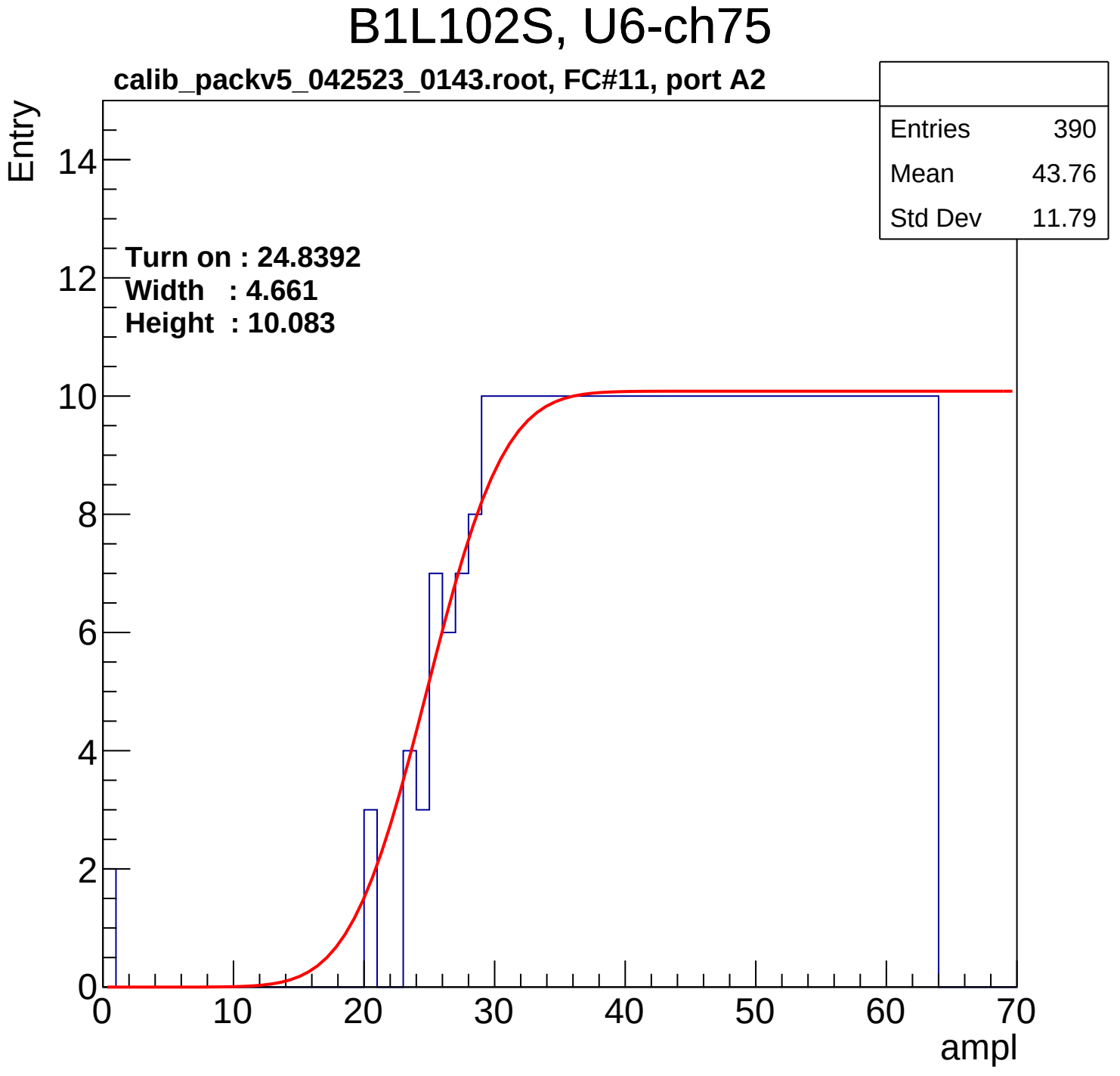
B1L102S, U6-ch75
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.76
Std Dev 11.79
Turn on : 24.8392
Width : 4.661
Height : 10.083
Entry
ampl
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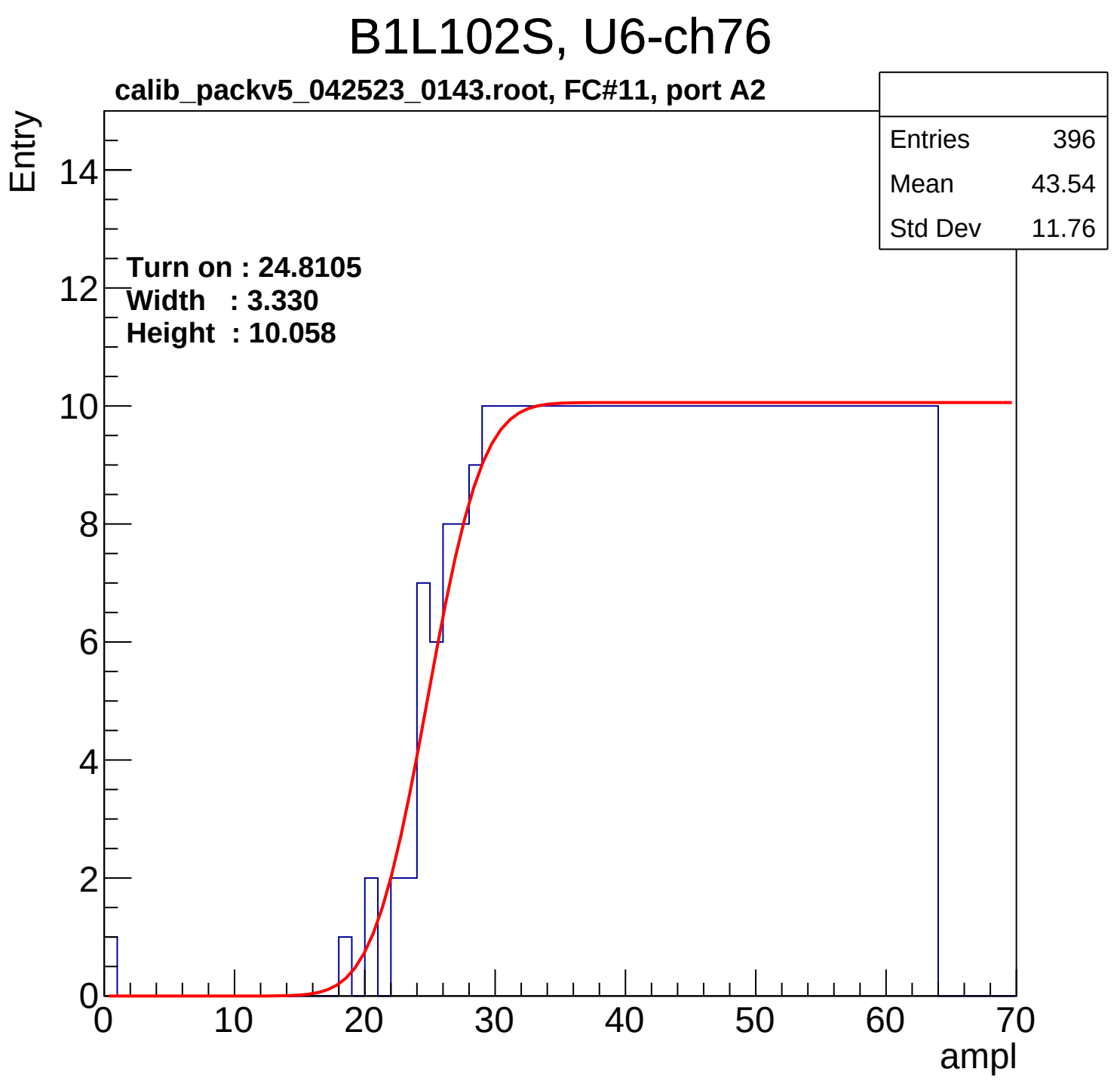
B1L102S, U6-ch76
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.54
Std Dev 11.76
Turn on : 24.8105
Width : 3.330
Height : 10.058
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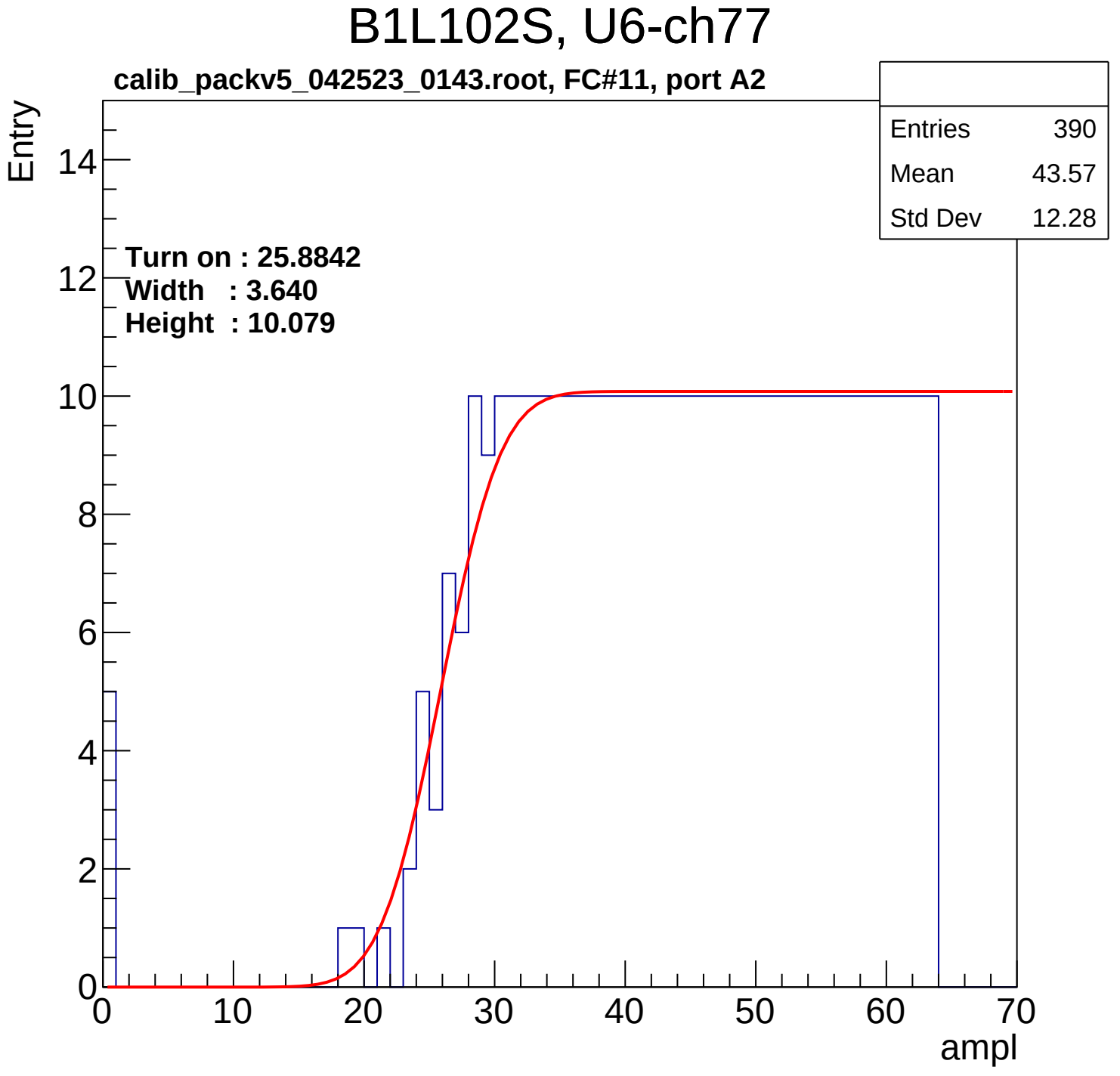
B1L102S, U6-ch77
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.57
Std Dev 12.28
Turn on : 25.8842
Width : 3.640
Height : 10.079
Entry
ampl
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8
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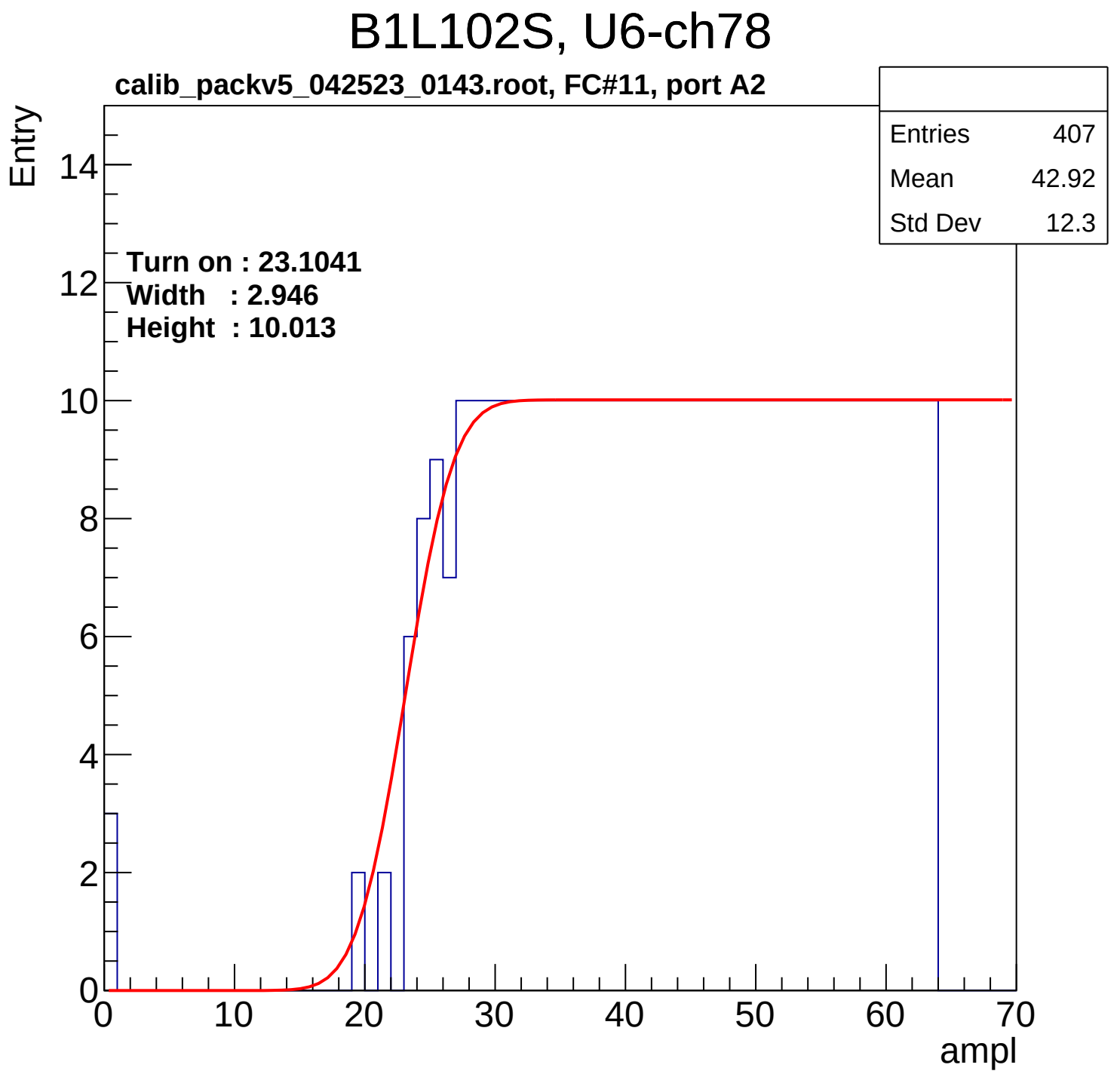
B1L102S, U6-ch78
calib_packv5_042523_0143.root, FC#11, port A2
Entries 407
Mean 42.92
Std Dev 12.3
Turn on : 23.1041
Width : 2.946
Height : 10.013
Entry
ampl
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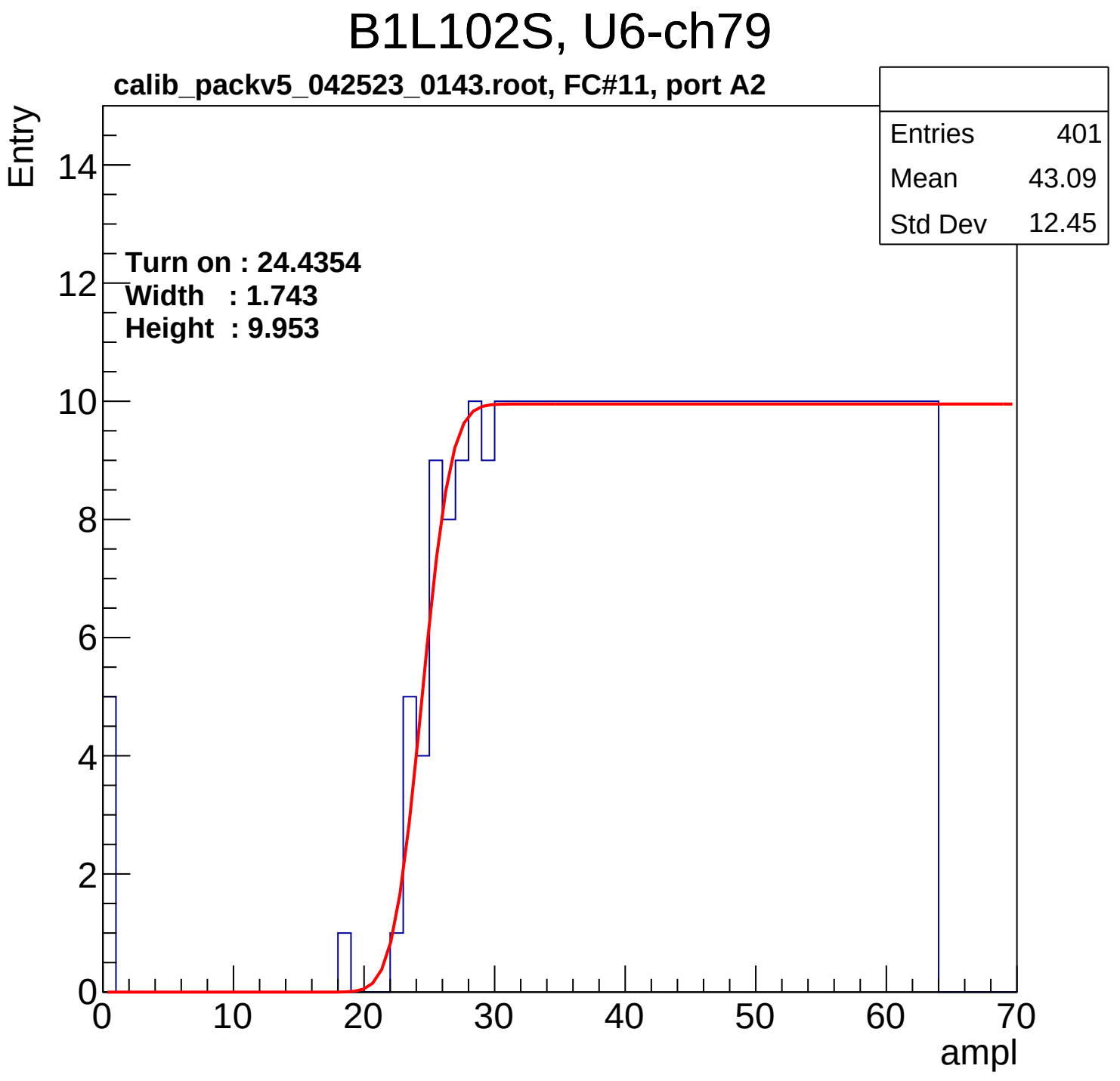
B1L102S, U6-ch79
calib_packv5_042523_0143.root, FC#11, port A2
Entries 401
Mean 43.09
Std Dev 12.45
Turn on : 24.4354
Width : 1.743
Height : 9.953
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ampl
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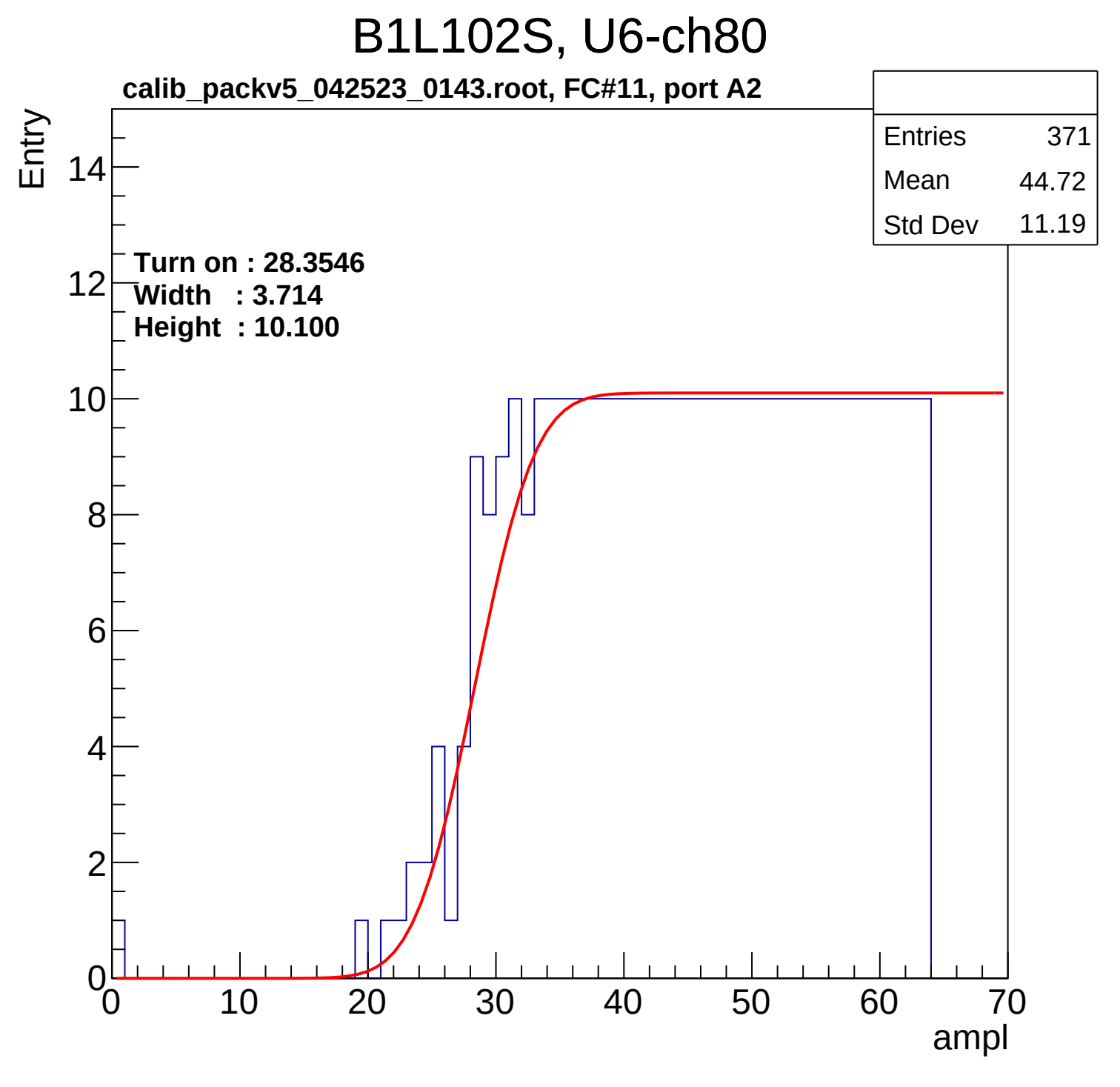
B1L102S, U6-ch80
calib_packv5_042523_0143.root, FC#11, port A2
Entries 371
Mean 44.72
Std Dev 11.19
Turn on : 28.3546
Width : 3.714
Height : 10.100
Entry
ampl
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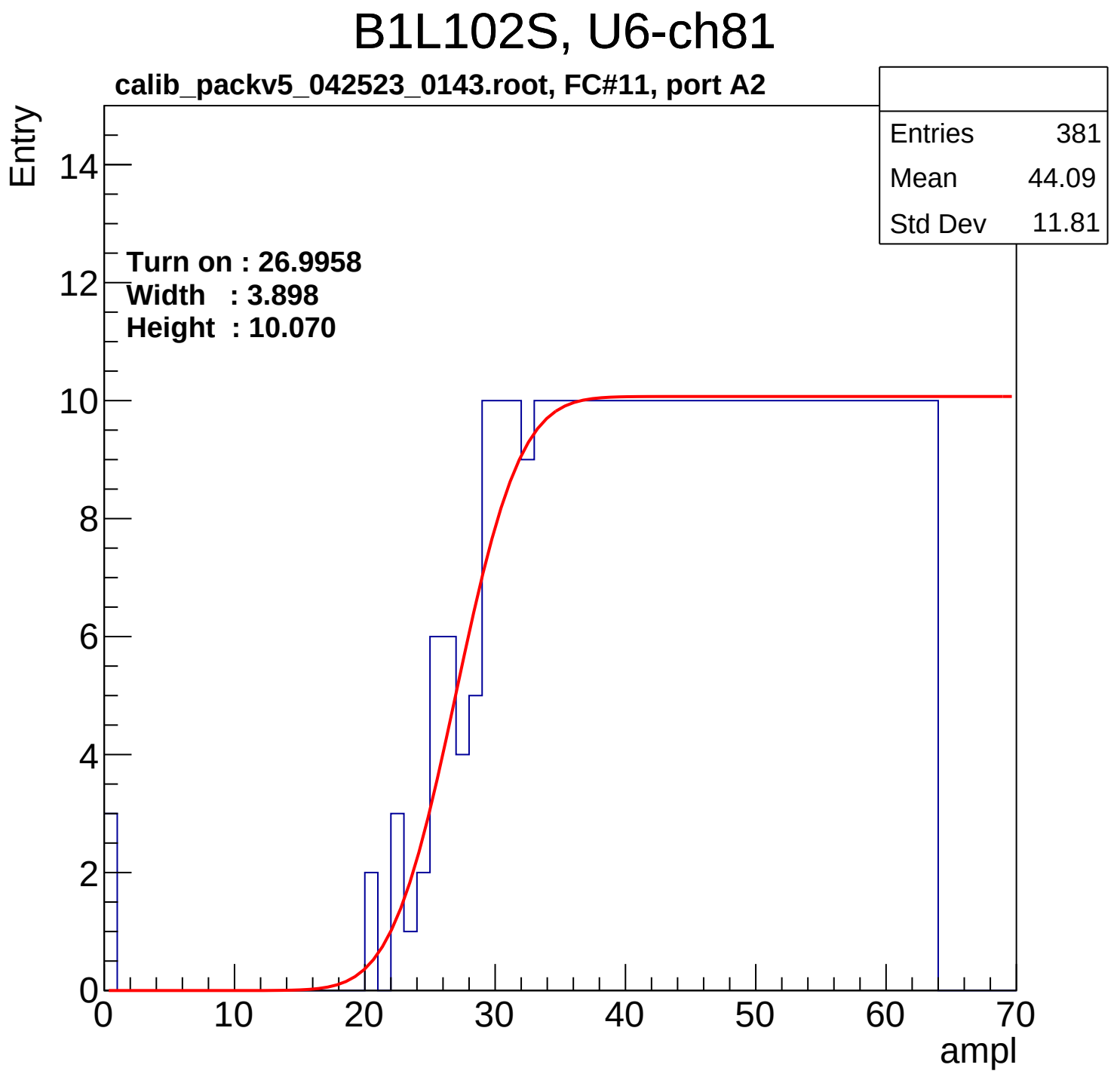
B1L102S, U6-ch81
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.09
Std Dev 11.81
Turn on : 26.9958
Width : 3.898
Height : 10.070
Entry
ampl
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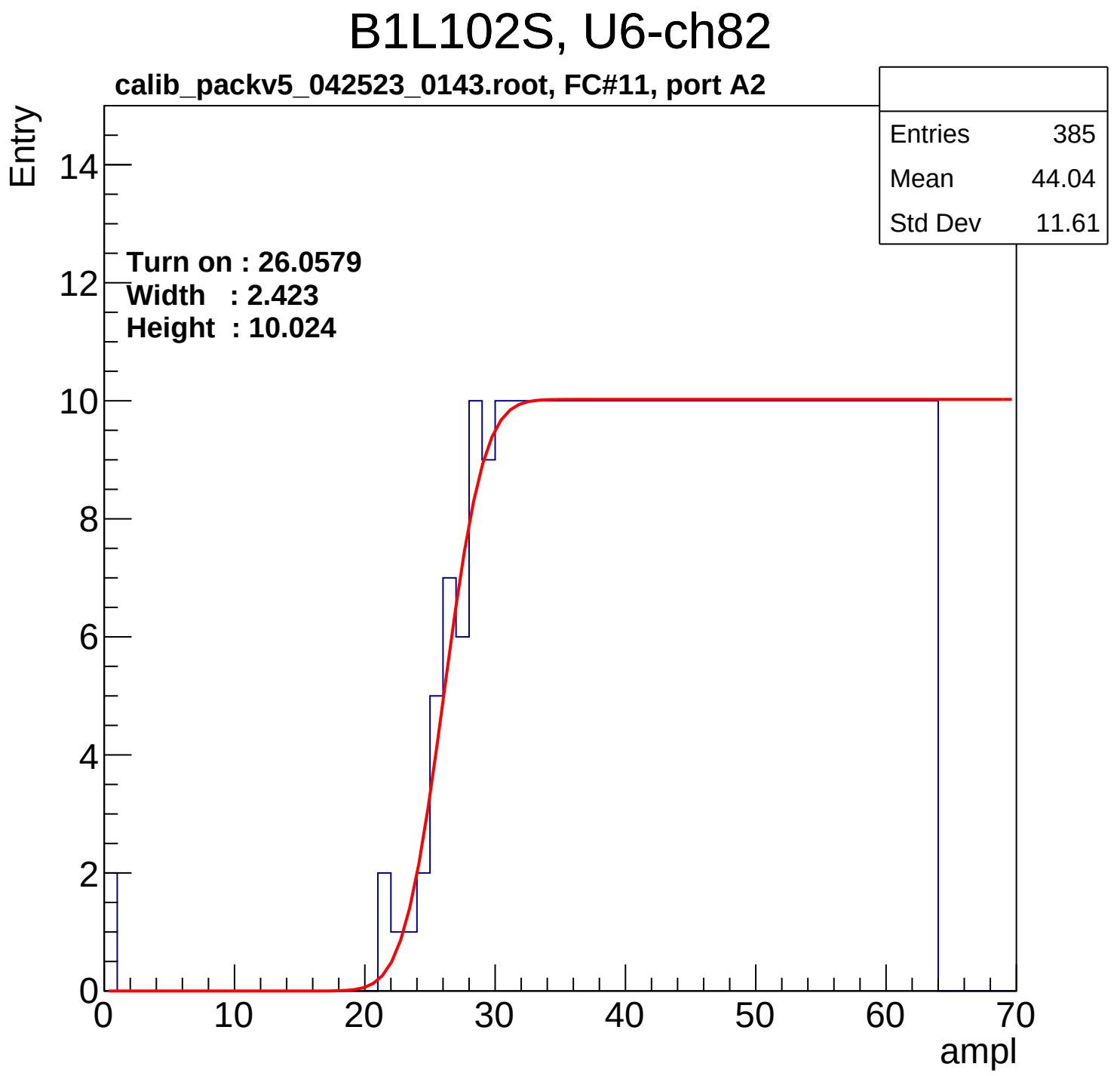
B1L102S, U6-ch82
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 44.04
Std Dev 11.61
Turn on : 26.0579
Width : 2.423
Height : 10.024
Entry
ampl
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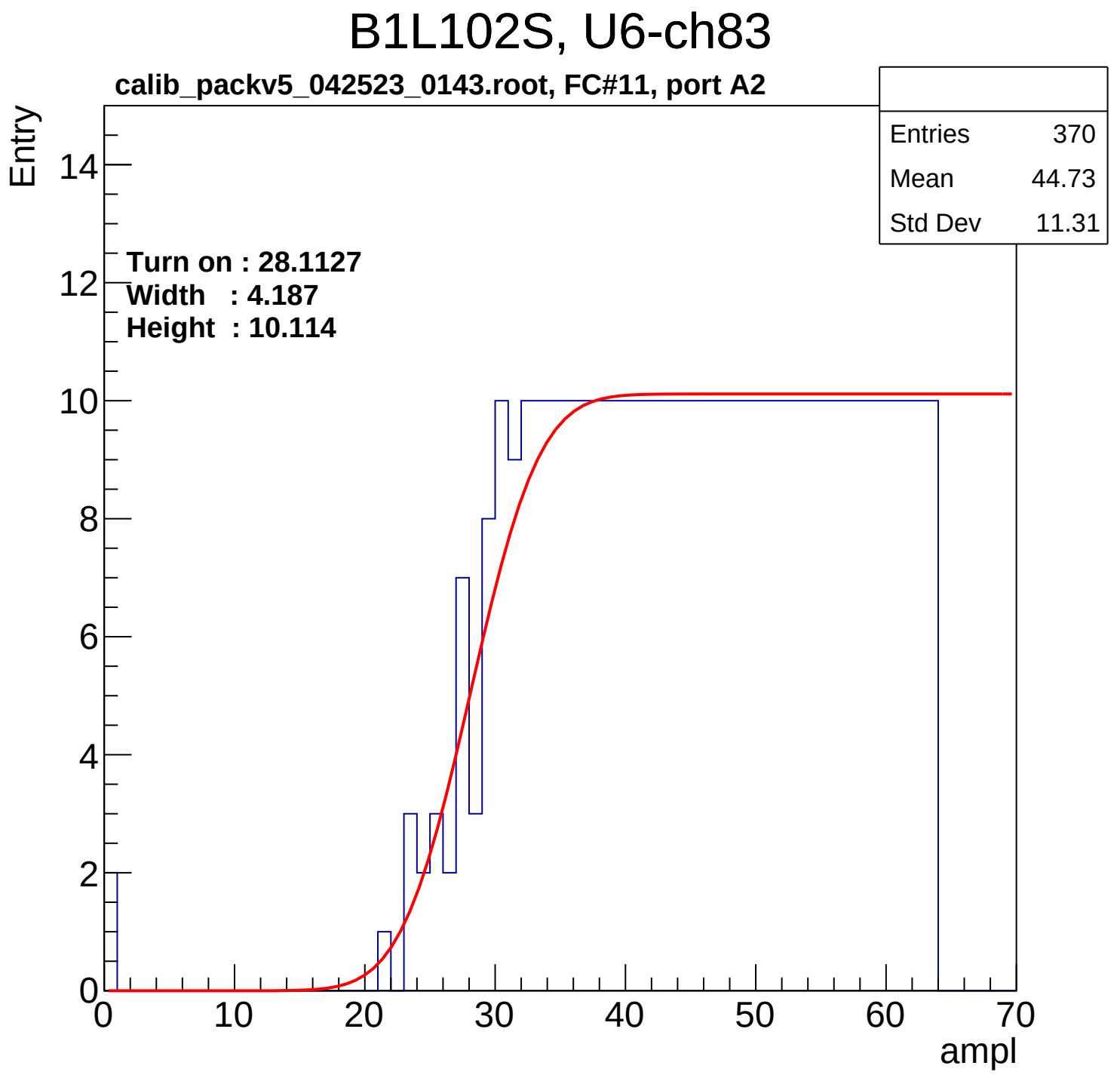
B1L102S, U6-ch83
calib_packv5_042523_0143.root, FC#11, port A2
Entries 370
Mean 44.73
Std Dev 11.31
Turn on : 28.1127
Width : 4.187
Height : 10.114
Entry
ampl
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6
8
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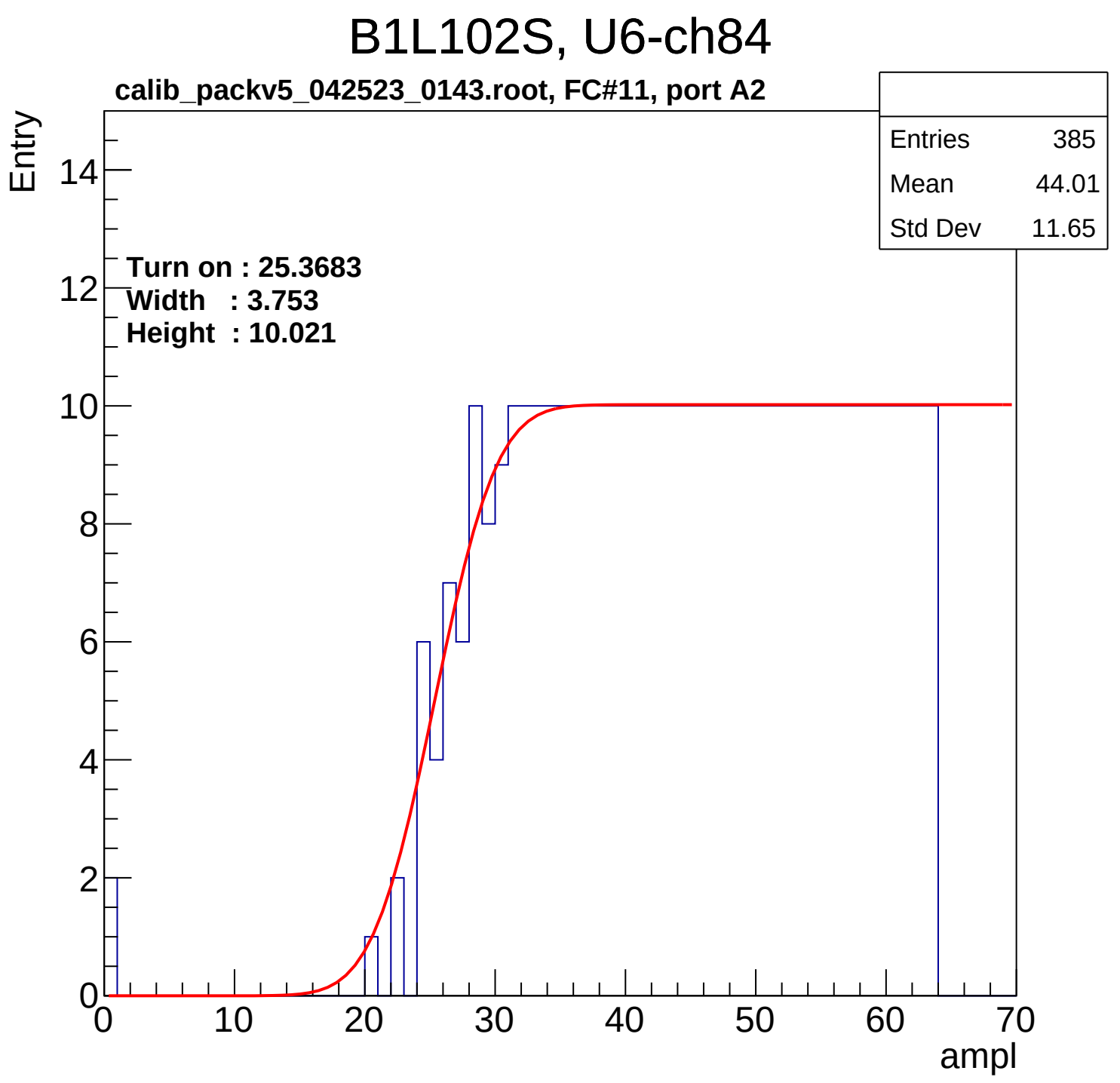
B1L102S, U6-ch84
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 44.01
Std Dev 11.65
Turn on : 25.3683
Width : 3.753
Height : 10.021
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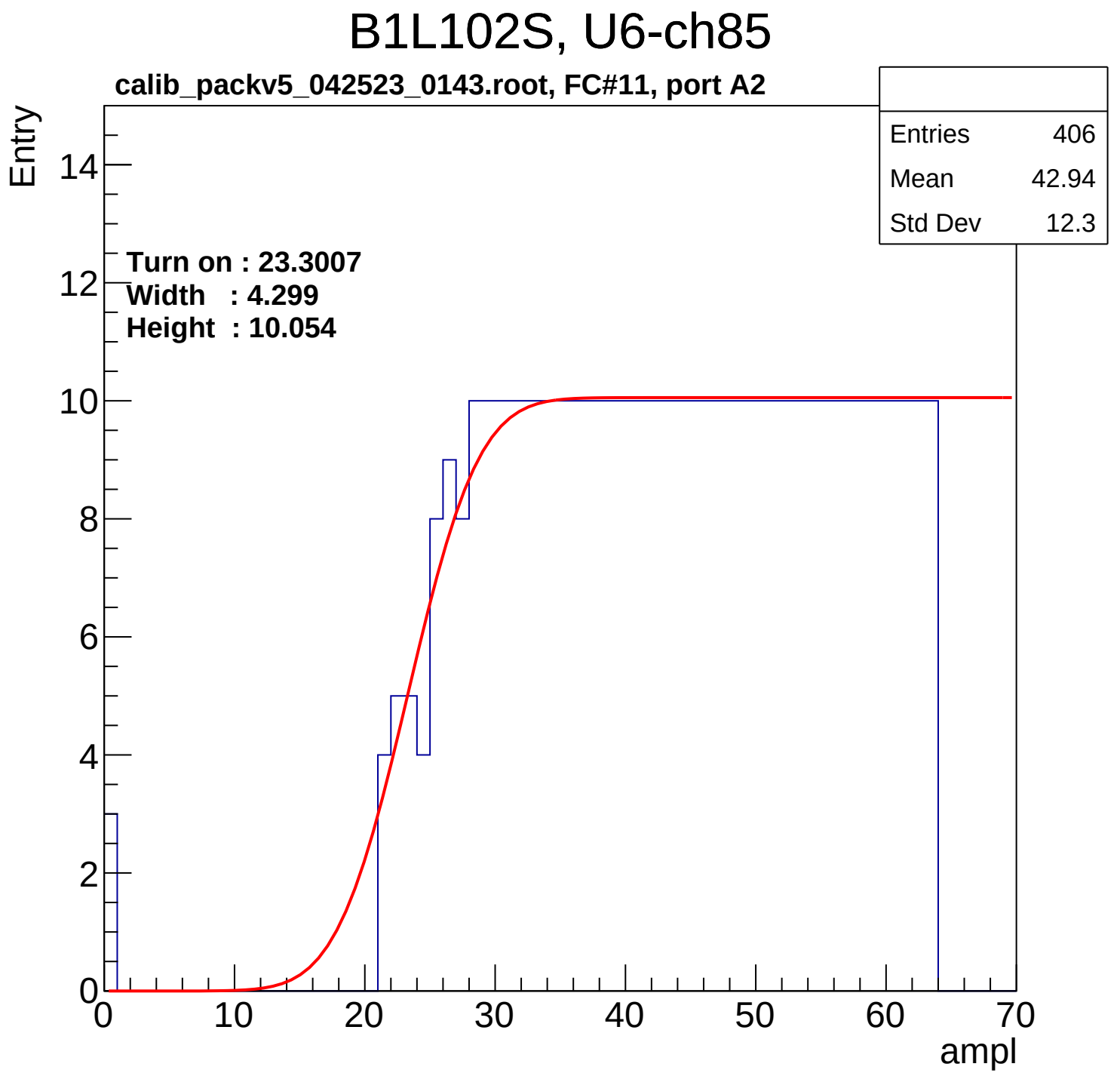
B1L102S, U6-ch85
calib_packv5_042523_0143.root, FC#11, port A2
Entries 406
Mean 42.94
Std Dev 12.3
Turn on : 23.3007
Width : 4.299
Height : 10.054
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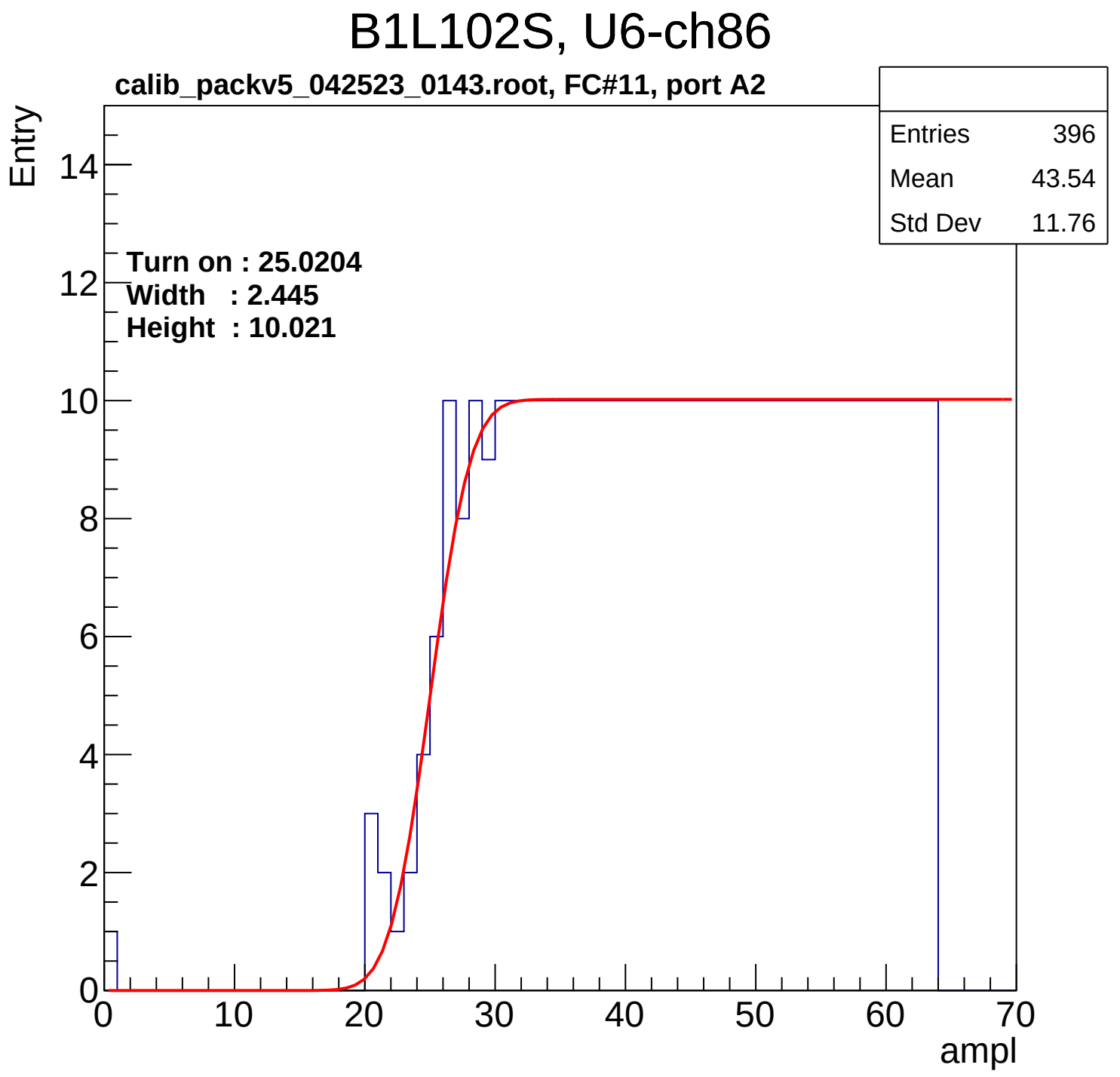
B1L102S, U6-ch86
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.54
Std Dev 11.76
Turn on : 25.0204
Width : 2.445
Height : 10.021
Entry
ampl
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4
6
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10
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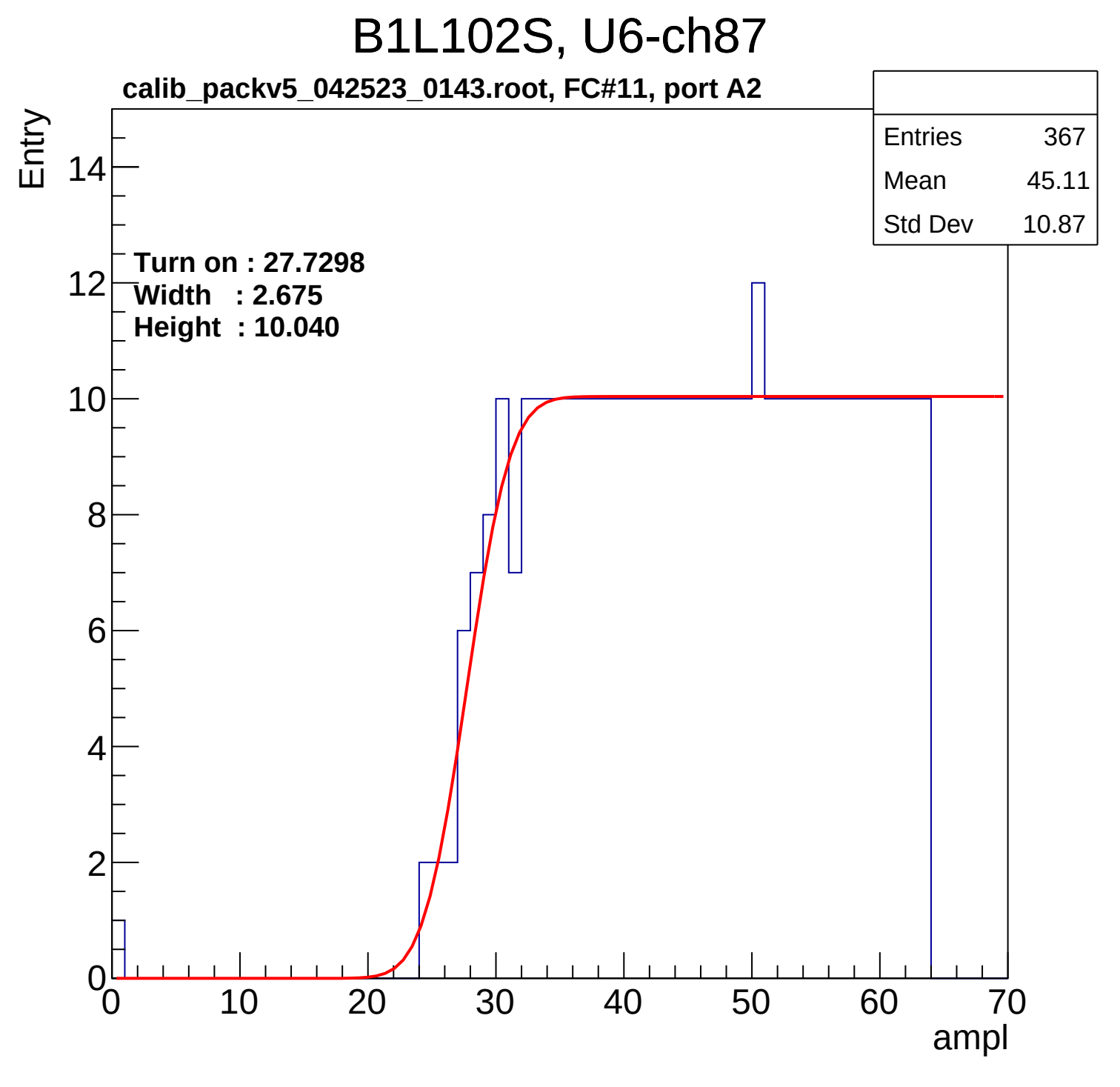
B1L102S, U6-ch87
calib_packv5_042523_0143.root, FC#11, port A2
Entries 367
Mean 45.11
Std Dev 10.87
Turn on : 27.7298
Width : 2.675
Height : 10.040
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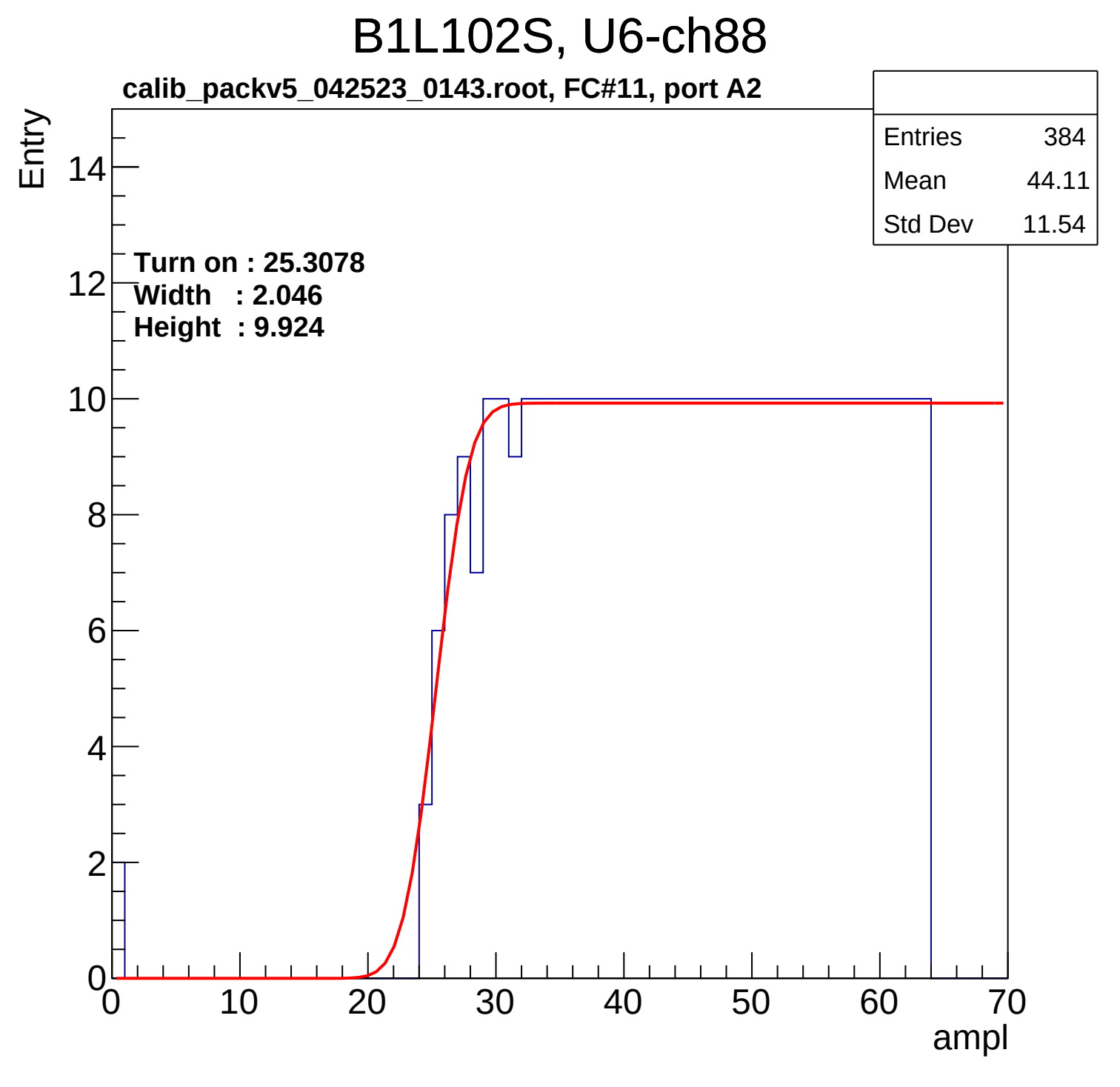
B1L102S, U6-ch88
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.11
Std Dev 11.54
Turn on : 25.3078
Width : 2.046
Height : 9.924
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ampl
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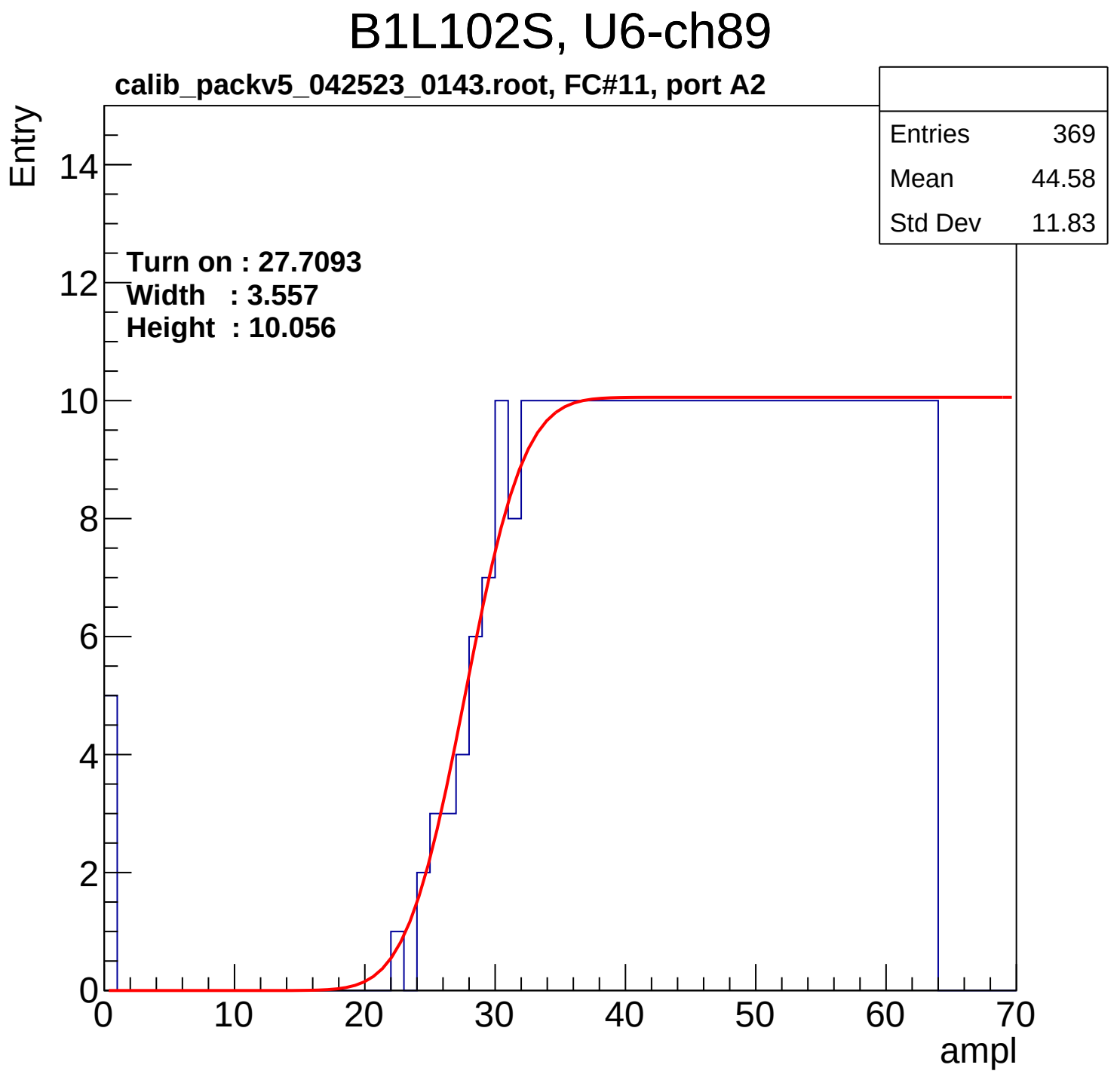
B1L102S, U6-ch89
calib_packv5_042523_0143.root, FC#11, port A2
Entries 369
Mean 44.58
Std Dev 11.83
Turn on : 27.7093
Width : 3.557
Height : 10.056
Entry
ampl
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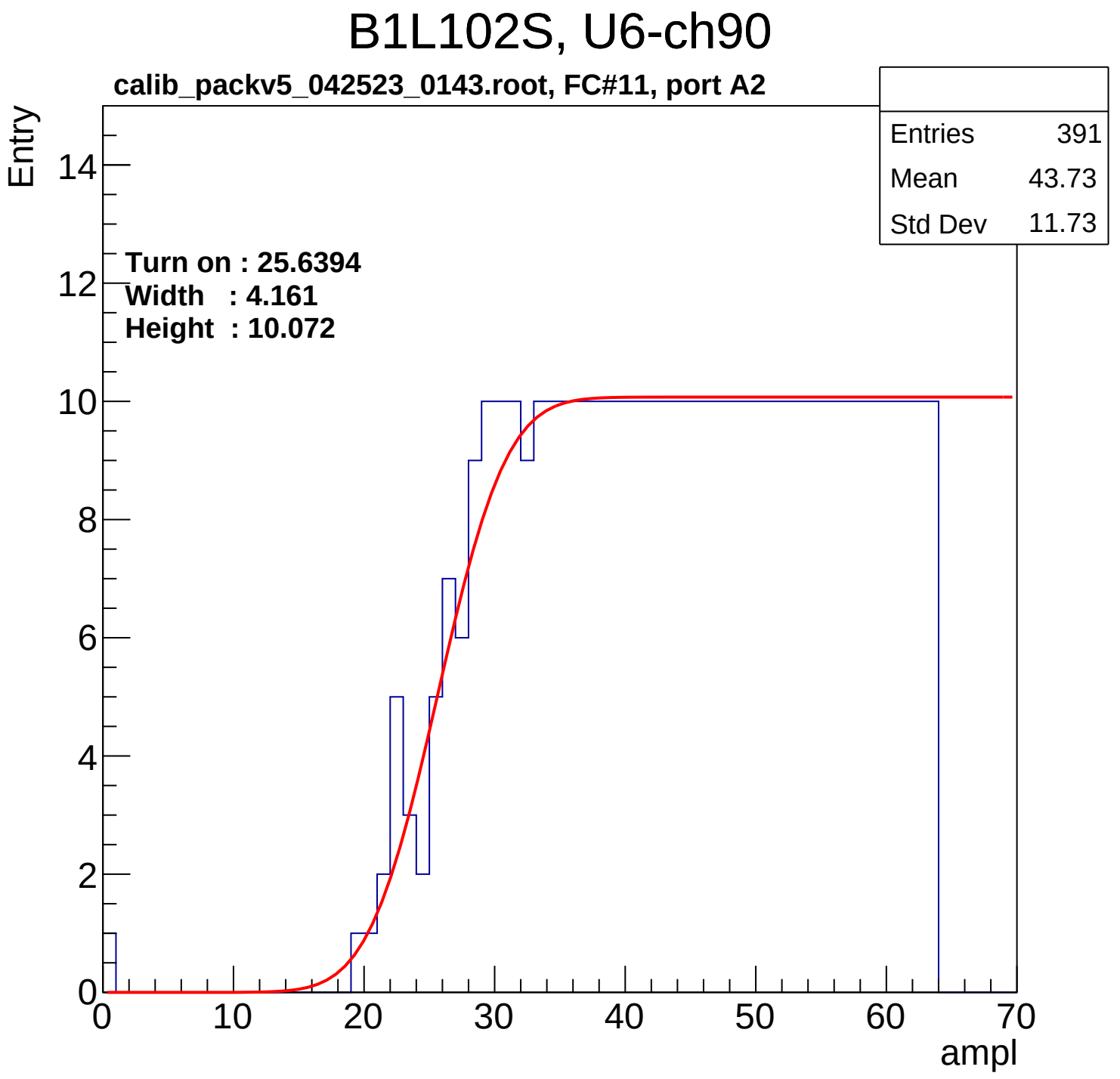
B1L102S, U6-ch90
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.73
Std Dev 11.73
Turn on : 25.6394
Width : 4.161
Height : 10.072
Entry
ampl
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2
4
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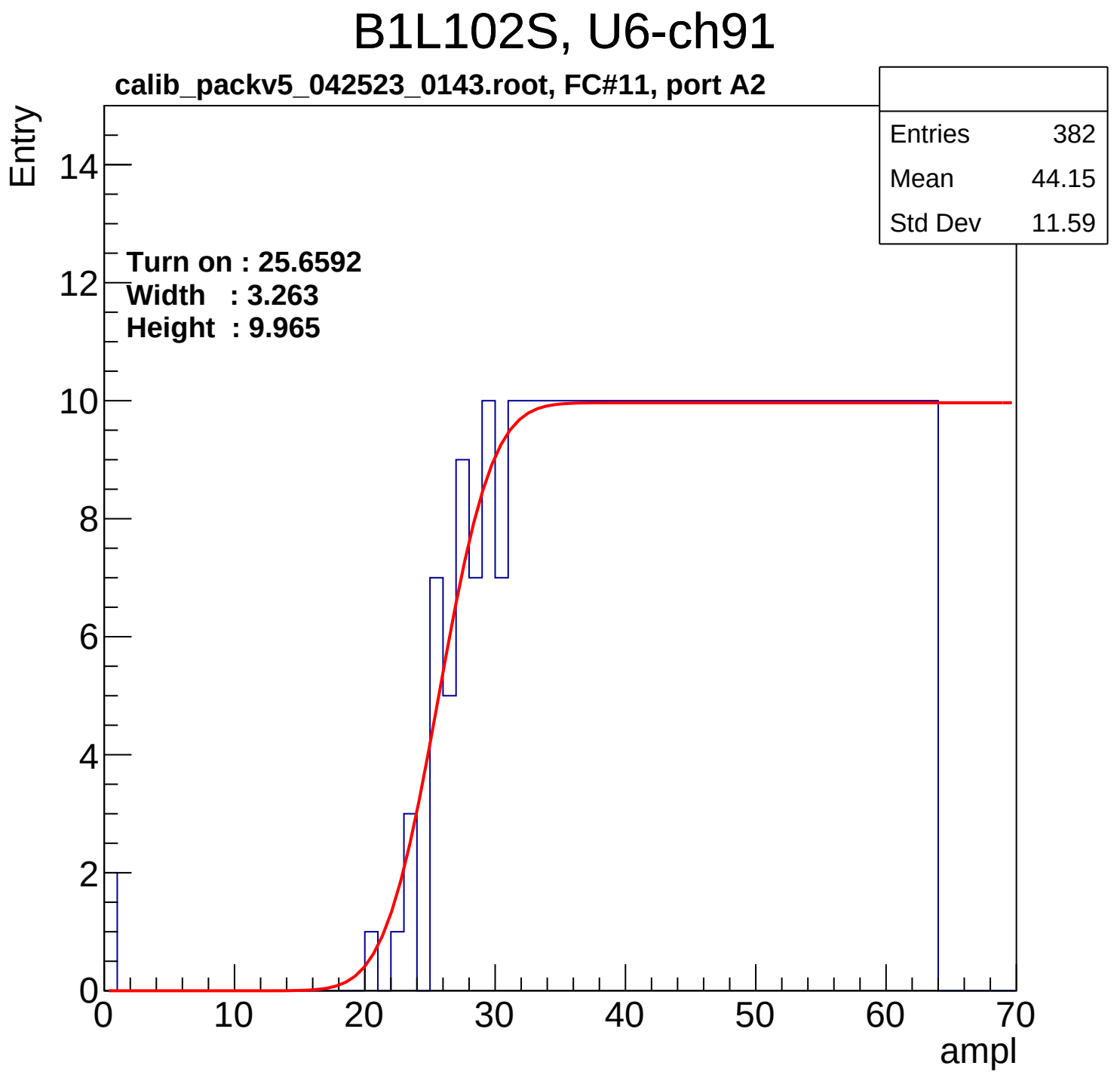
B1L102S, U6-ch91
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.15
Std Dev 11.59
Turn on : 25.6592
Width : 3.263
Height : 9.965
Entry
ampl
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8
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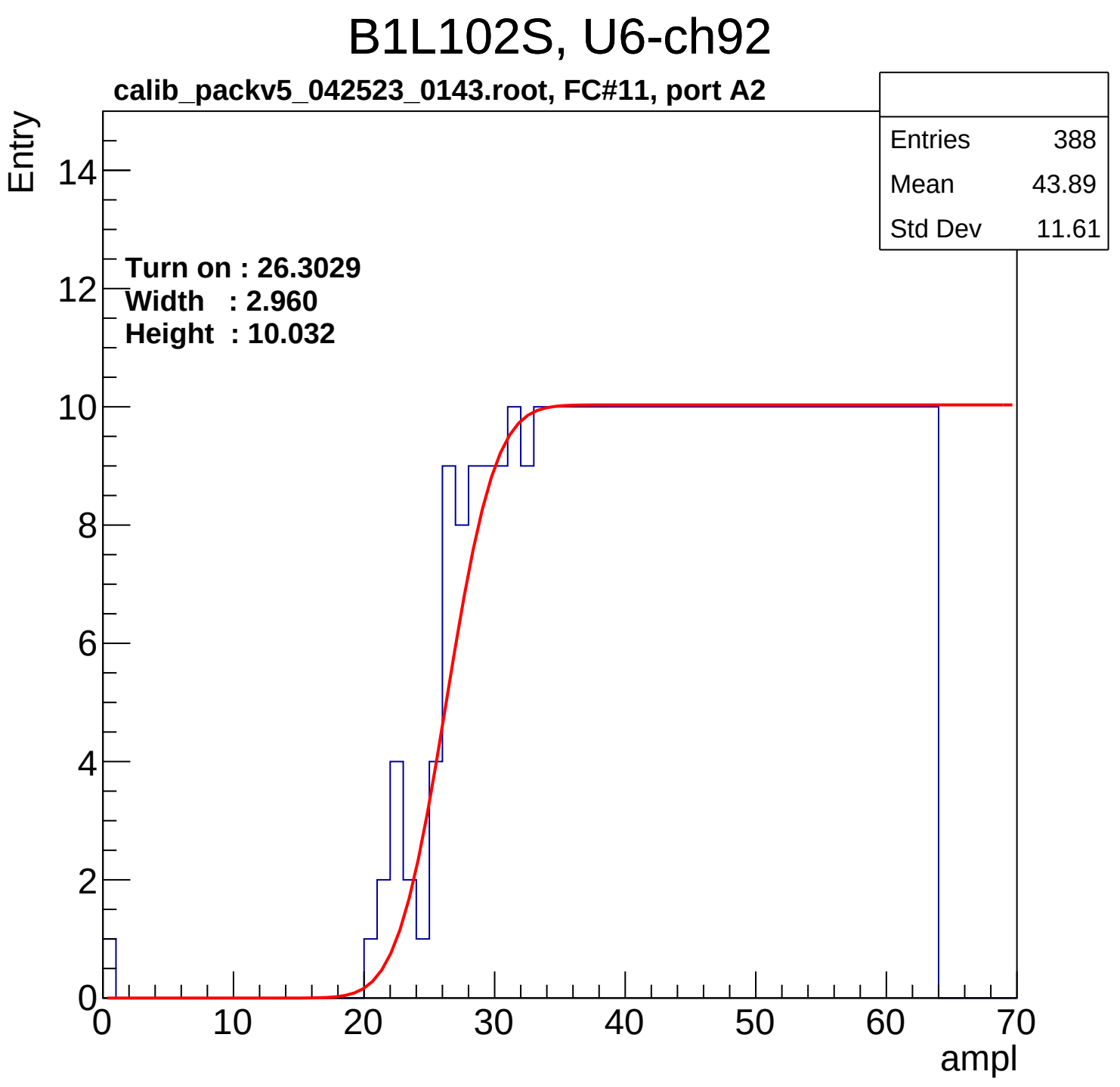
B1L102S, U6-ch92
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.89
Std Dev 11.61
Turn on : 26.3029
Width : 2.960
Height : 10.032
Entry
ampl
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6
8
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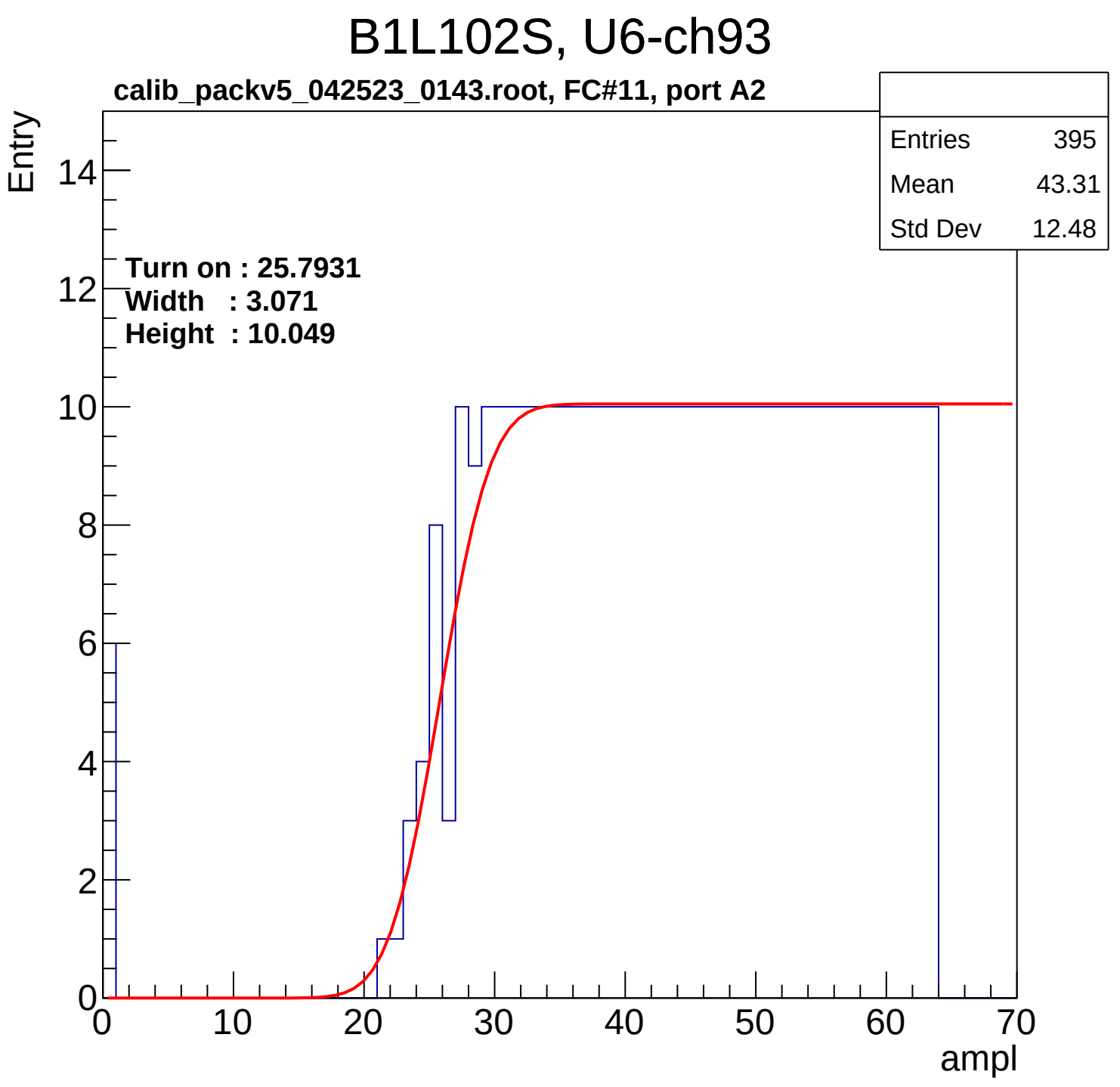
B1L102S, U6-ch93
calib_packv5_042523_0143.root, FC#11, port A2
Entries 395
Mean 43.31
Std Dev 12.48
Turn on : 25.7931
Width : 3.071
Height : 10.049
Entry
ampl
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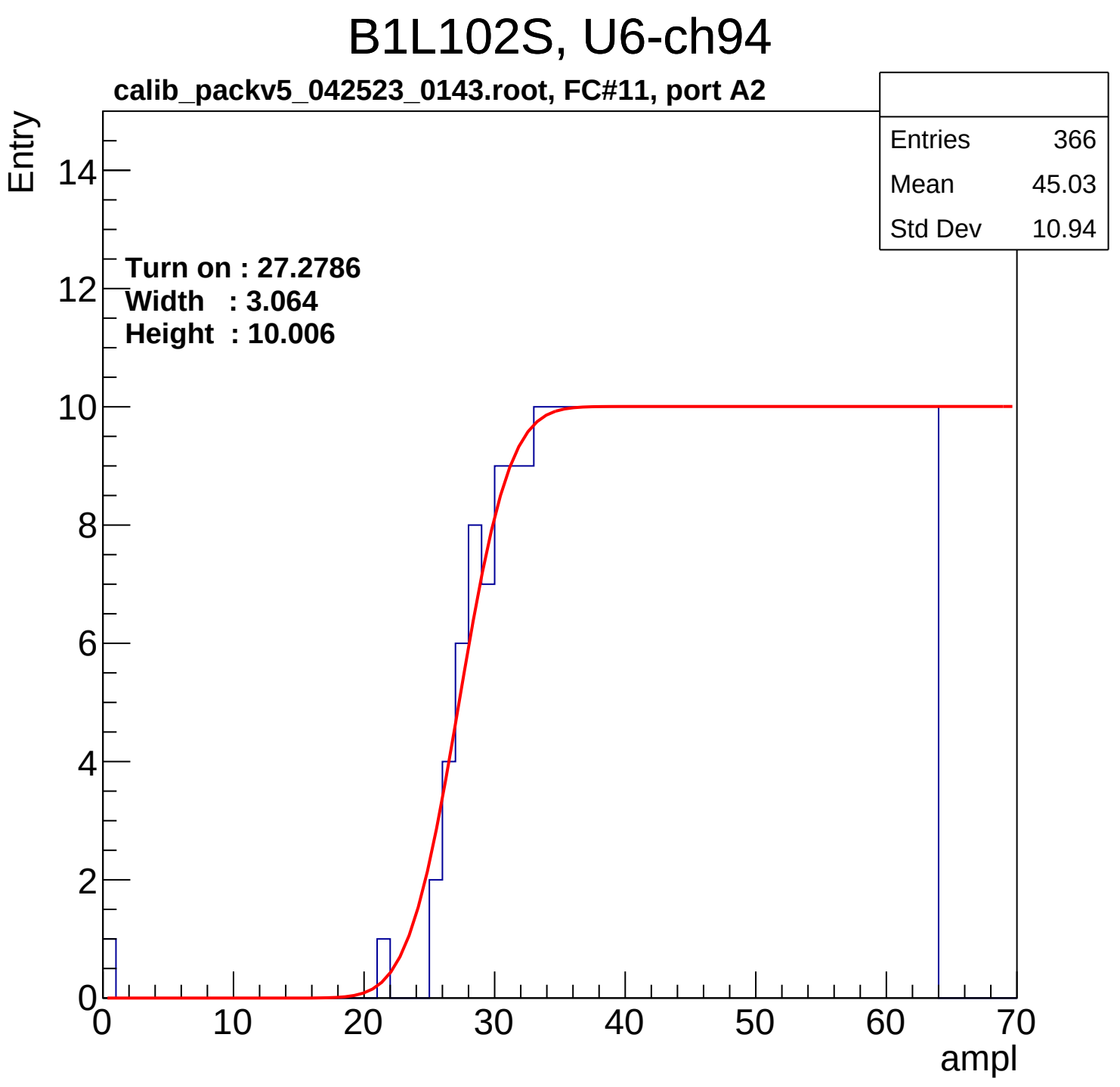
B1L102S, U6-ch94
calib_packv5_042523_0143.root, FC#11, port A2
Entries 366
Mean 45.03
Std Dev 10.94
Turn on : 27.2786
Width : 3.064
Height : 10.006
Entry
ampl
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8
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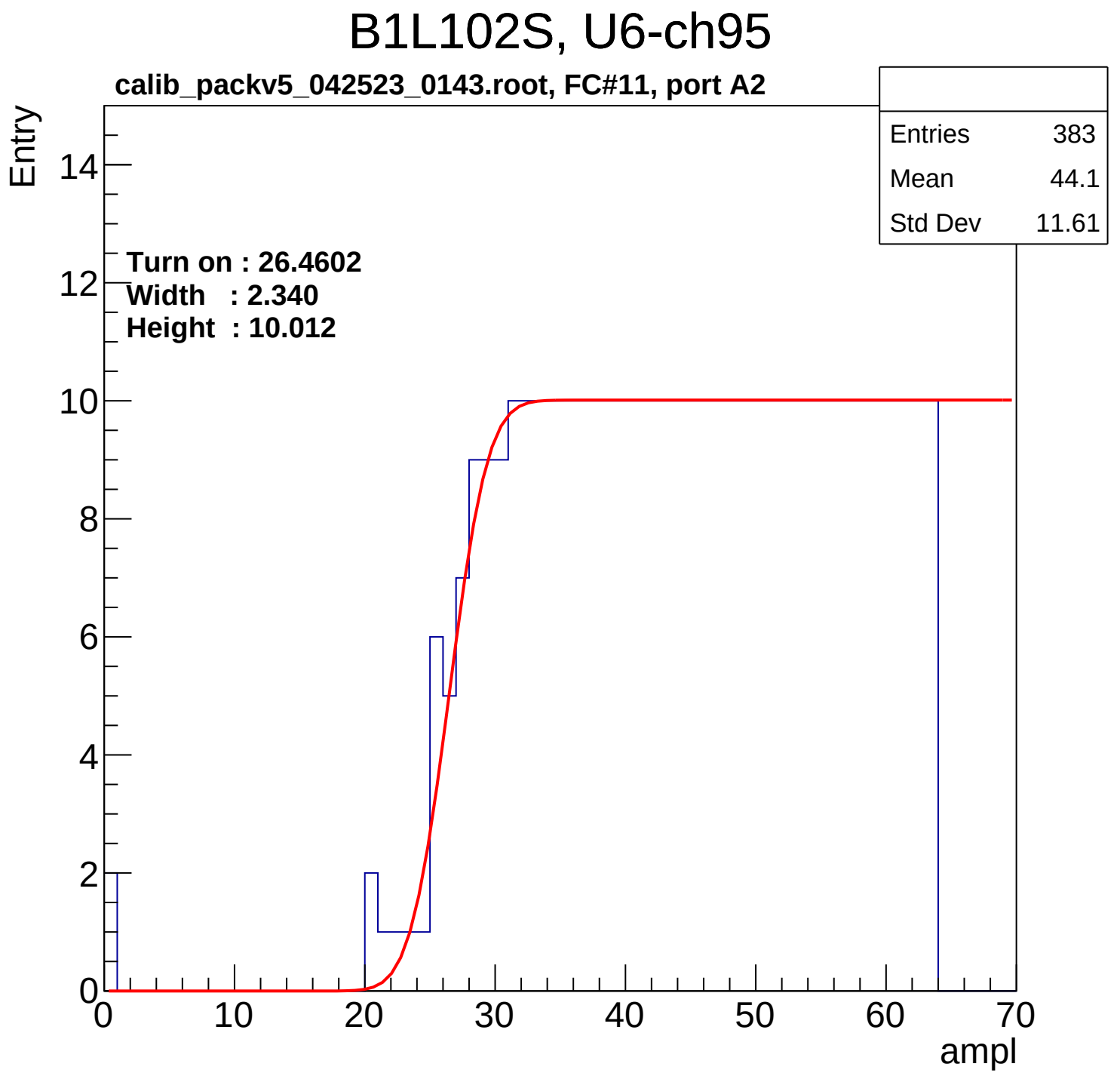
B1L102S, U6-ch95
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.1
Std Dev 11.61
Turn on : 26.4602
Width : 2.340
Height : 10.012
Entry
ampl
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6
8
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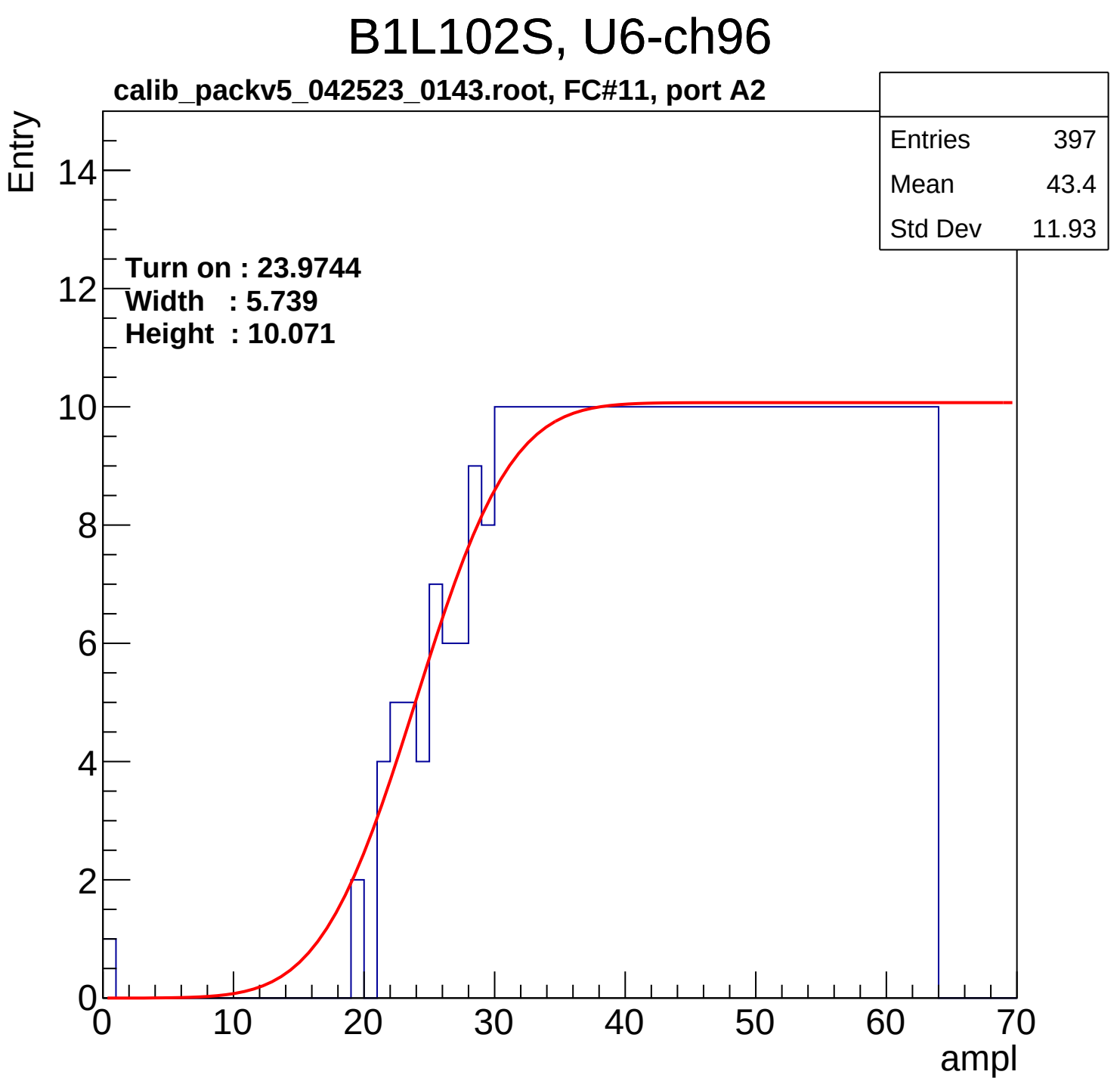
B1L102S, U6-ch96
calib_packv5_042523_0143.root, FC#11, port A2
Entries 397
Mean 43.4
Std Dev 11.93
Turn on : 23.9744
Width : 5.739
Height : 10.071
Entry
ampl
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4
6
8
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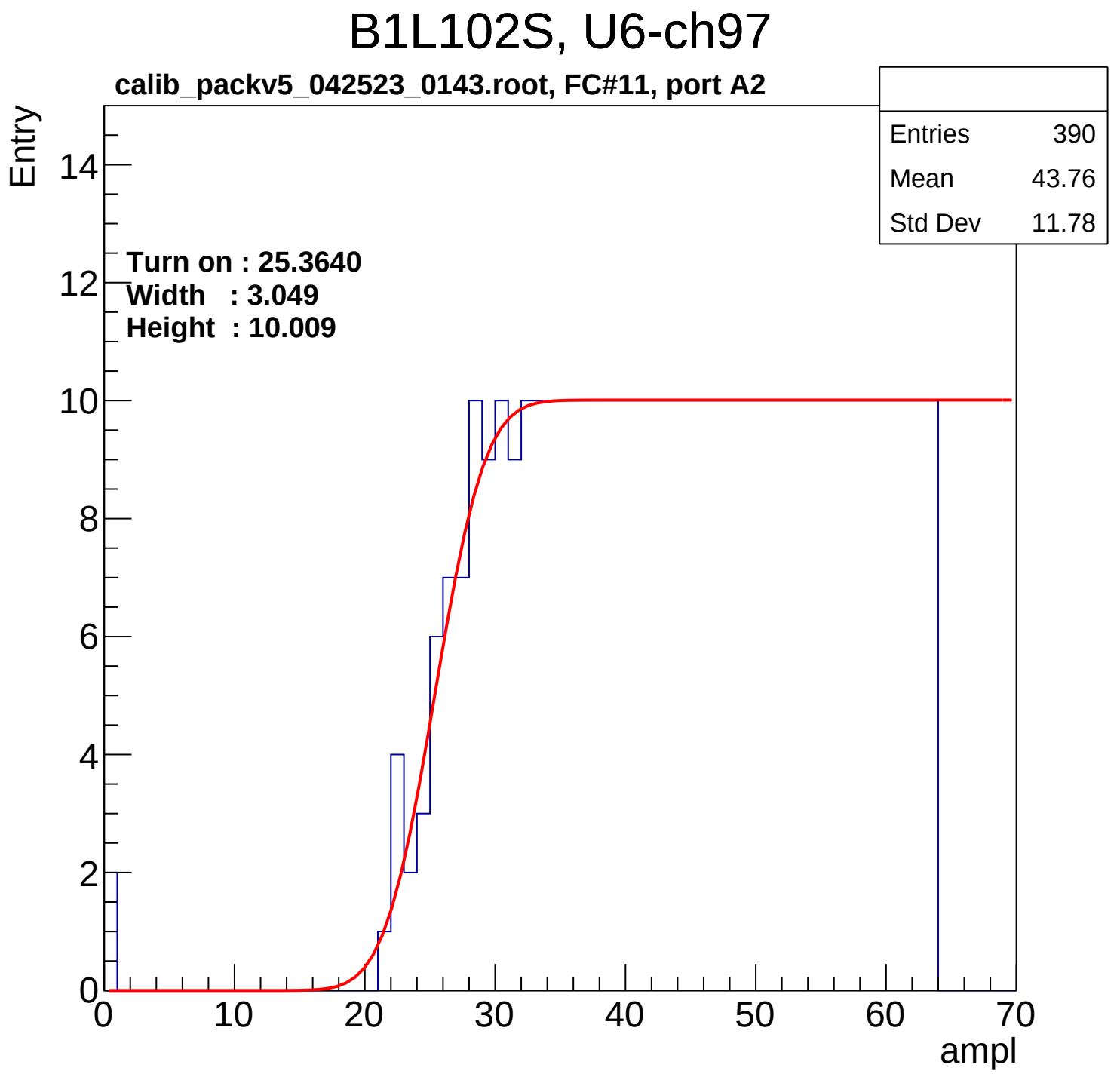
B1L102S, U6-ch97
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.76
Std Dev 11.78
Turn on : 25.3640
Width : 3.049
Height : 10.009
Entry
ampl
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6
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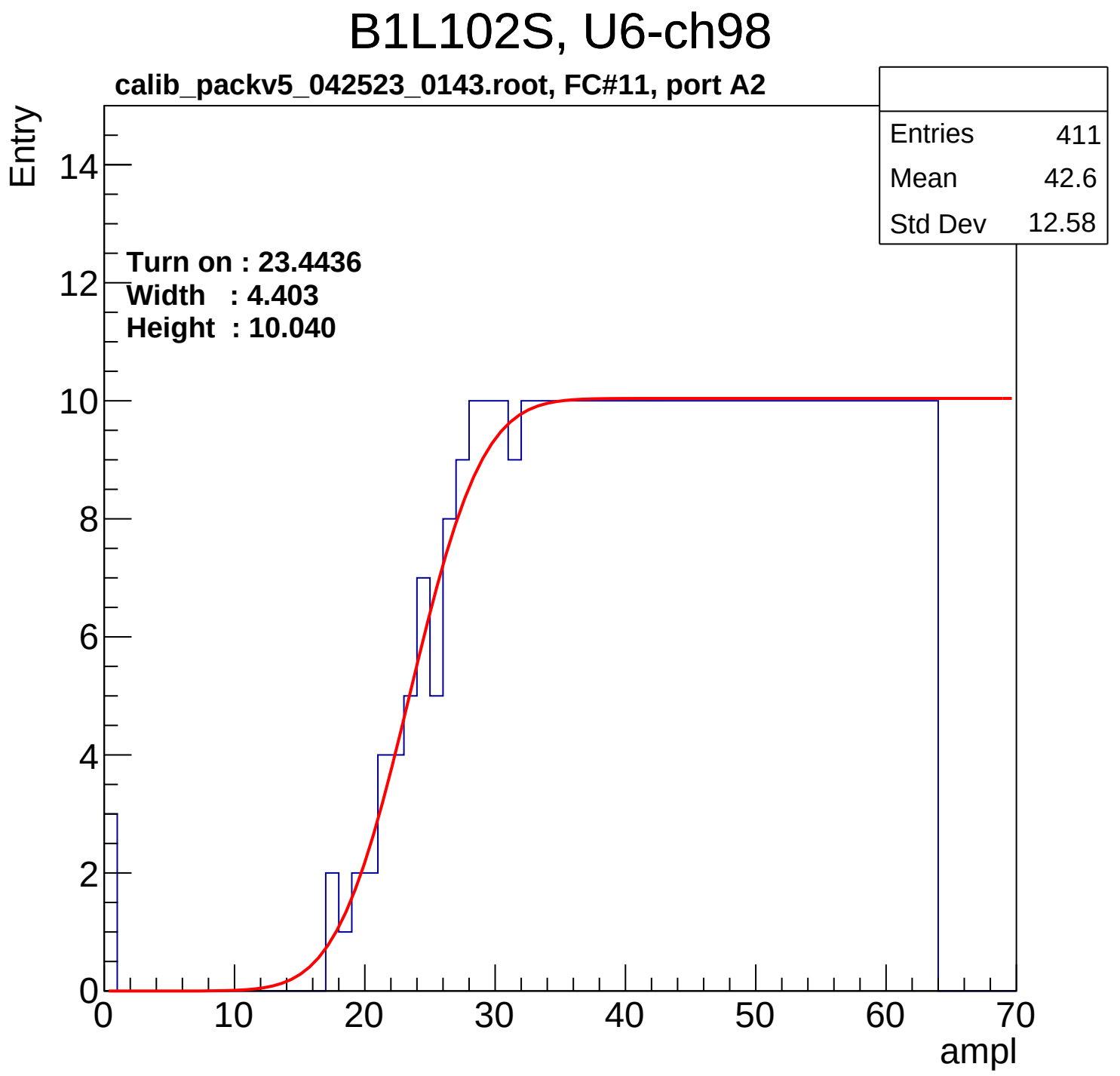
B1L102S, U6-ch98
calib_packv5_042523_0143.root, FC#11, port A2
Entries 411
Mean 42.6
Std Dev 12.58
Turn on : 23.4436
Width : 4.403
Height : 10.040
Entry
ampl
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6
8
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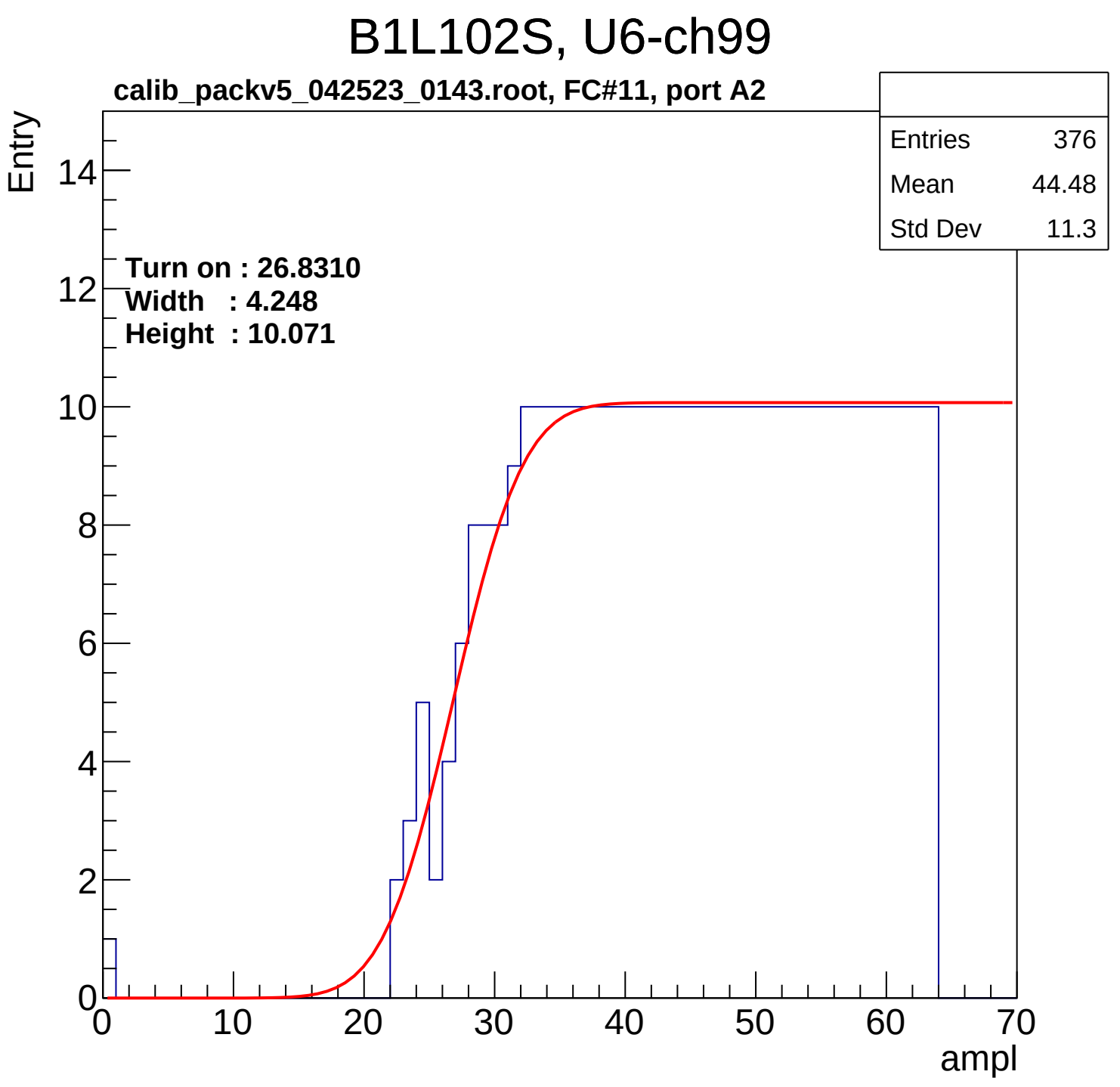
B1L102S, U6-ch99
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.48
Std Dev 11.3
Turn on : 26.8310
Width : 4.248
Height : 10.071
Entry
ampl
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8
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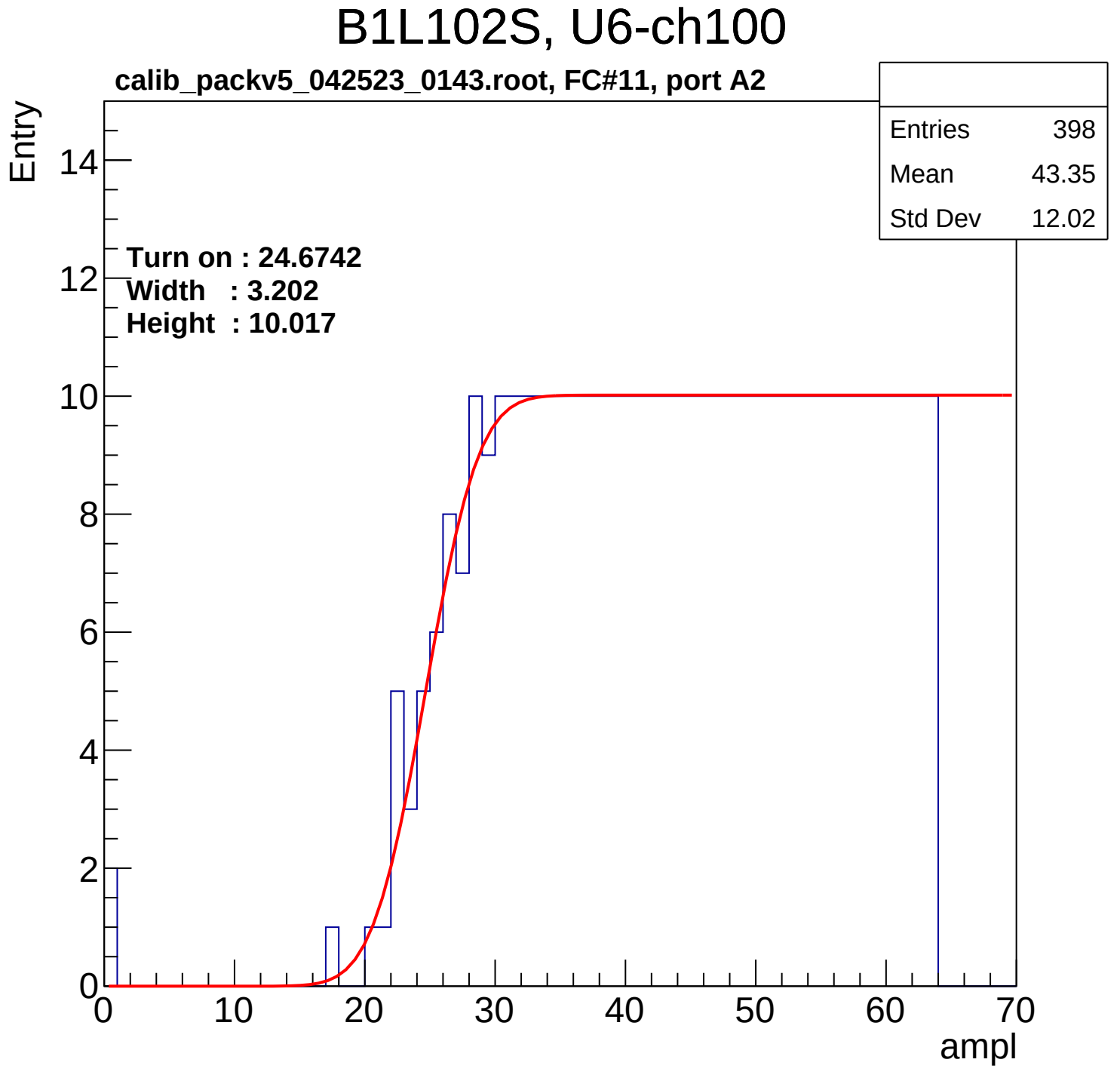
B1L102S, U6-ch100
calib_packv5_042523_0143.root, FC#11, port A2
Entries 398
Mean 43.35
Std Dev 12.02
Turn on : 24.6742
Width : 3.202
Height : 10.017
Entry
ampl
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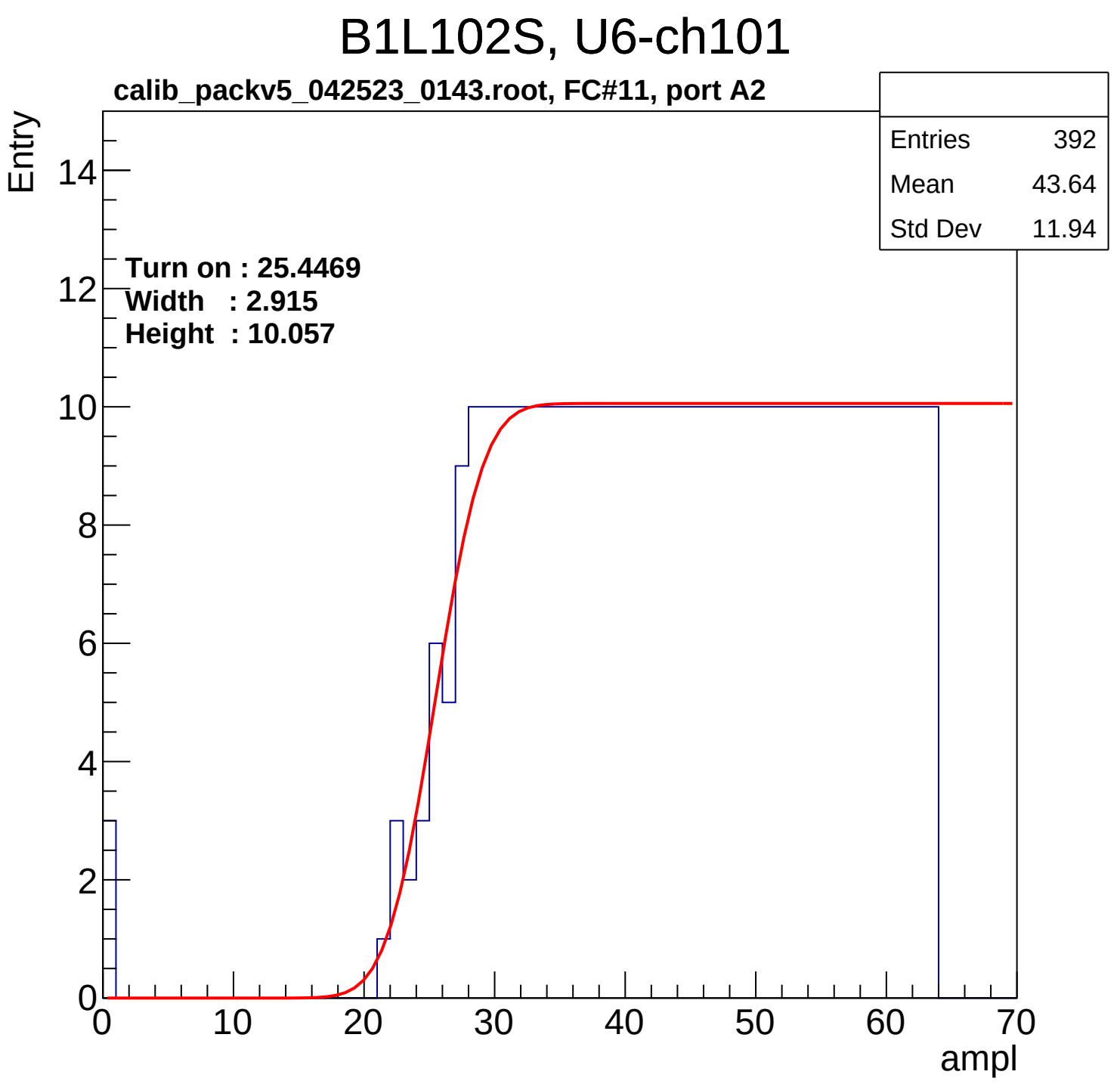
B1L102S, U6-ch101
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.64
Std Dev 11.94
Turn on : 25.4469
Width : 2.915
Height : 10.057
Entry
ampl
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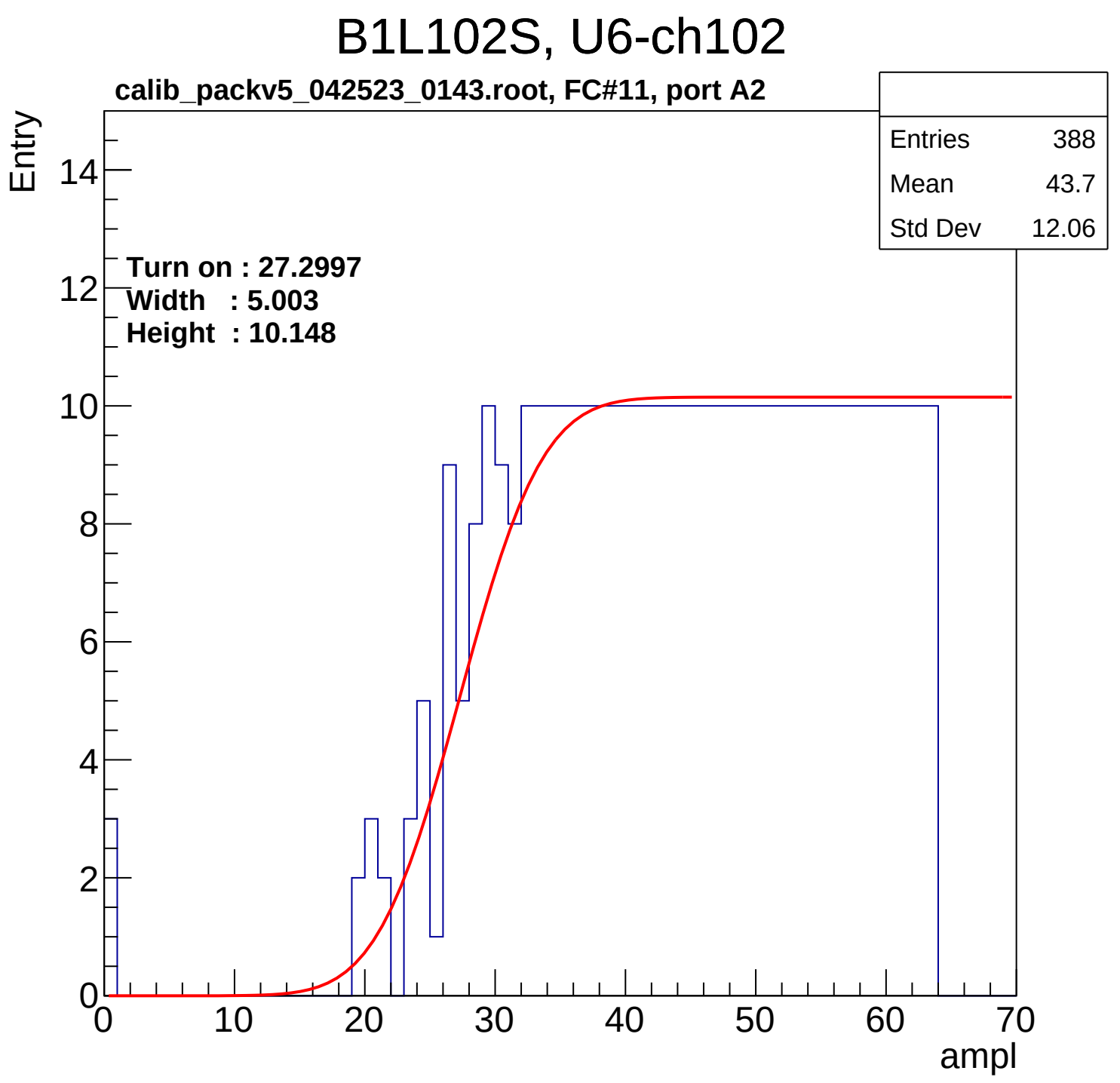
B1L102S, U6-ch102
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.7
Std Dev 12.06
Turn on : 27.2997
Width : 5.003
Height : 10.148
Entry
ampl
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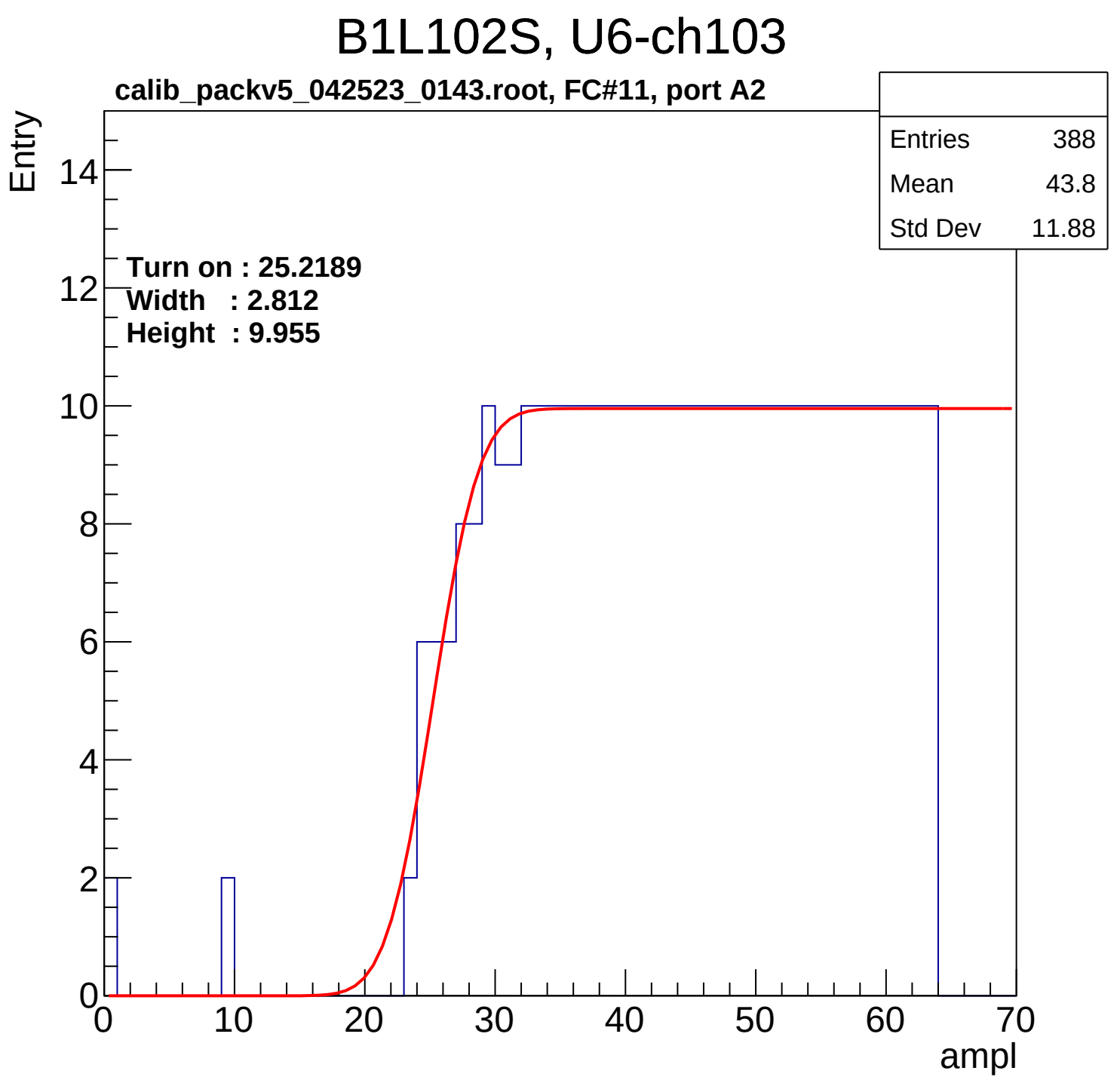
B1L102S, U6-ch103
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.8
Std Dev 11.88
Turn on : 25.2189
Width : 2.812
Height : 9.955
Entry
ampl
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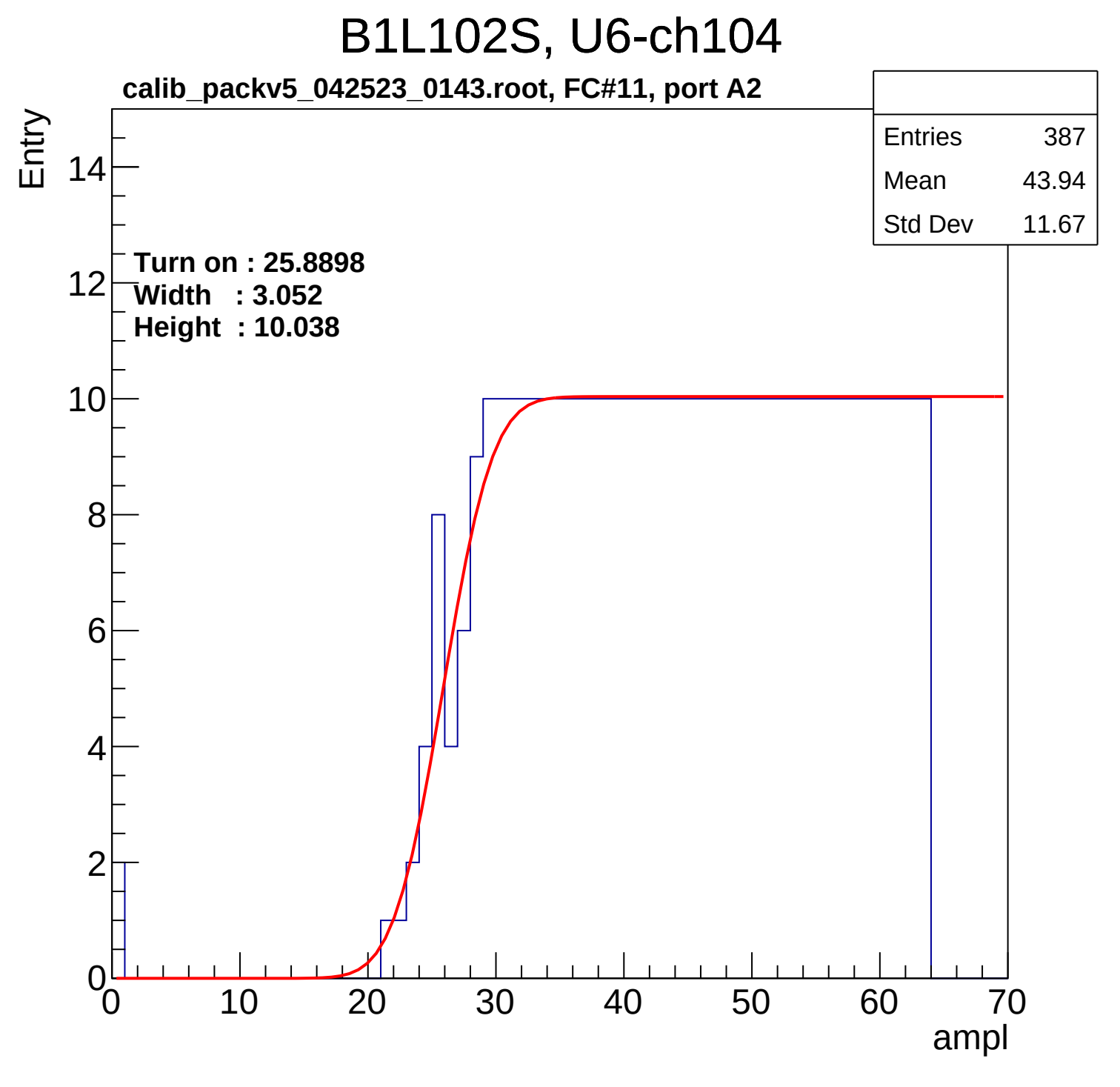
B1L102S, U6-ch104
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.94
Std Dev 11.67
Turn on : 25.8898
Width : 3.052
Height : 10.038
Entry
ampl
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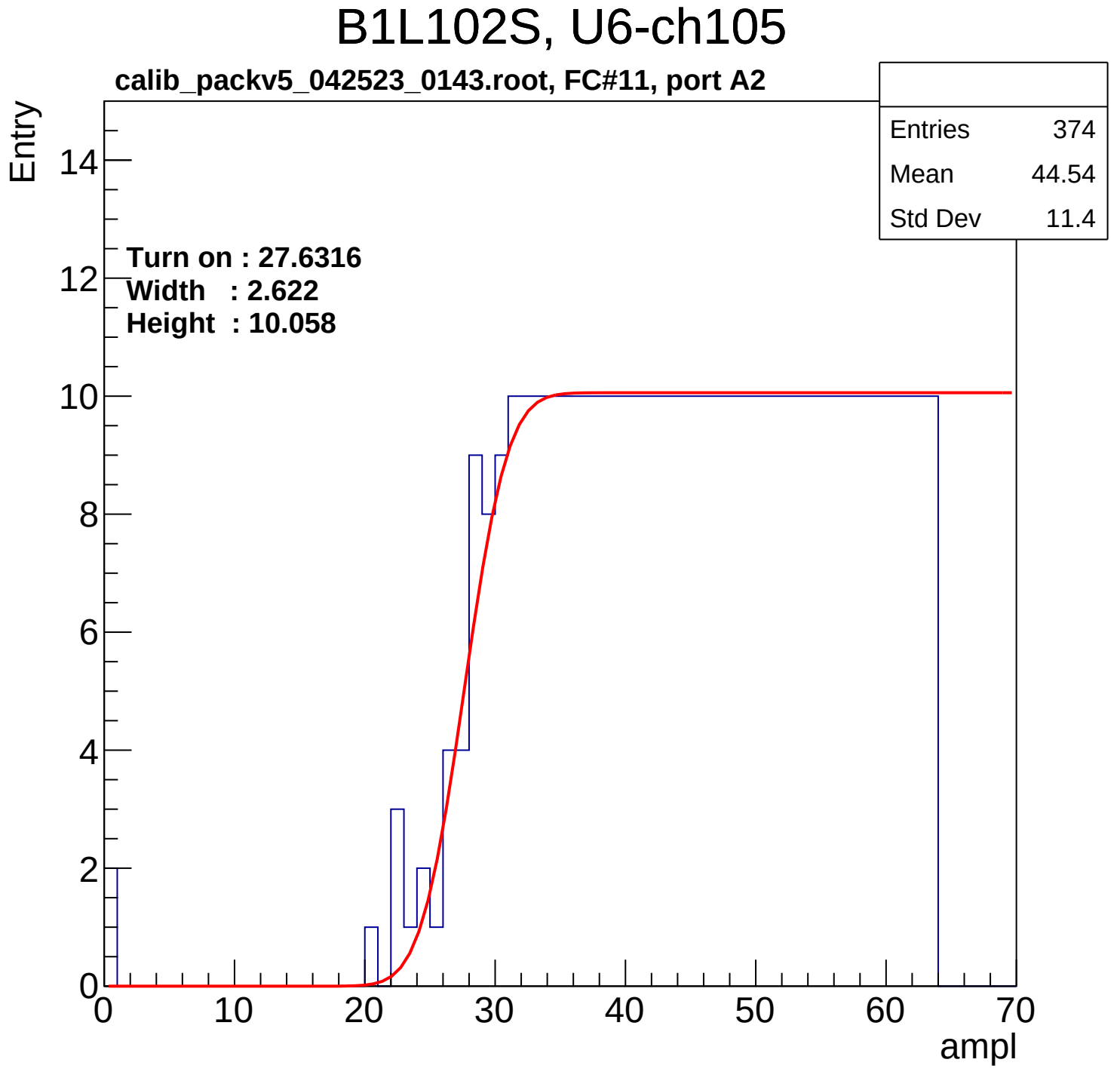
B1L102S, U6-ch105
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.54
Std Dev 11.4
Turn on : 27.6316
Width : 2.622
Height : 10.058
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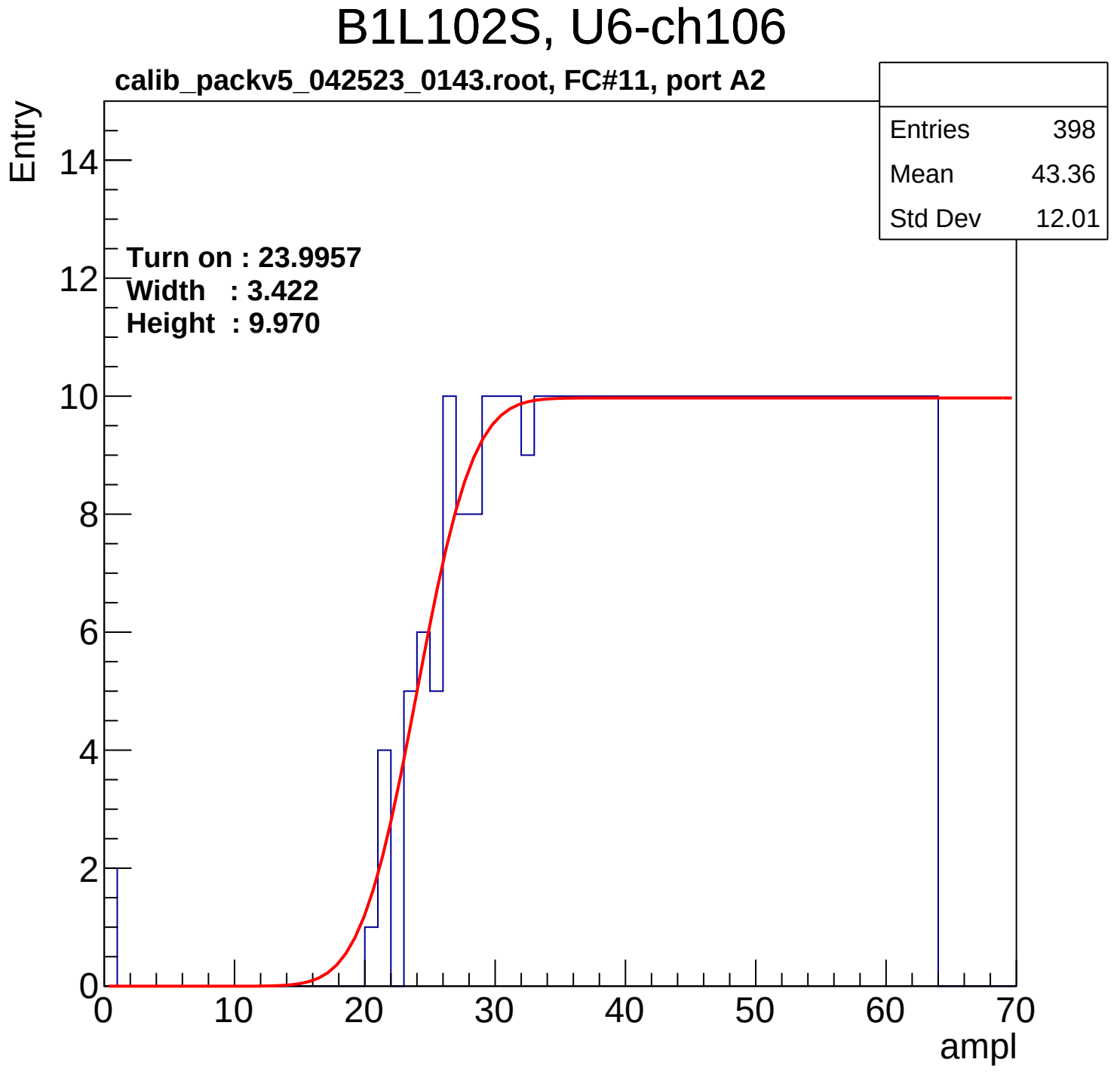
B1L102S, U6-ch106
calib_packv5_042523_0143.root, FC#11, port A2
Entries 398
Mean 43.36
Std Dev 12.01
Turn on : 23.9957
Width : 3.422
Height : 9.970
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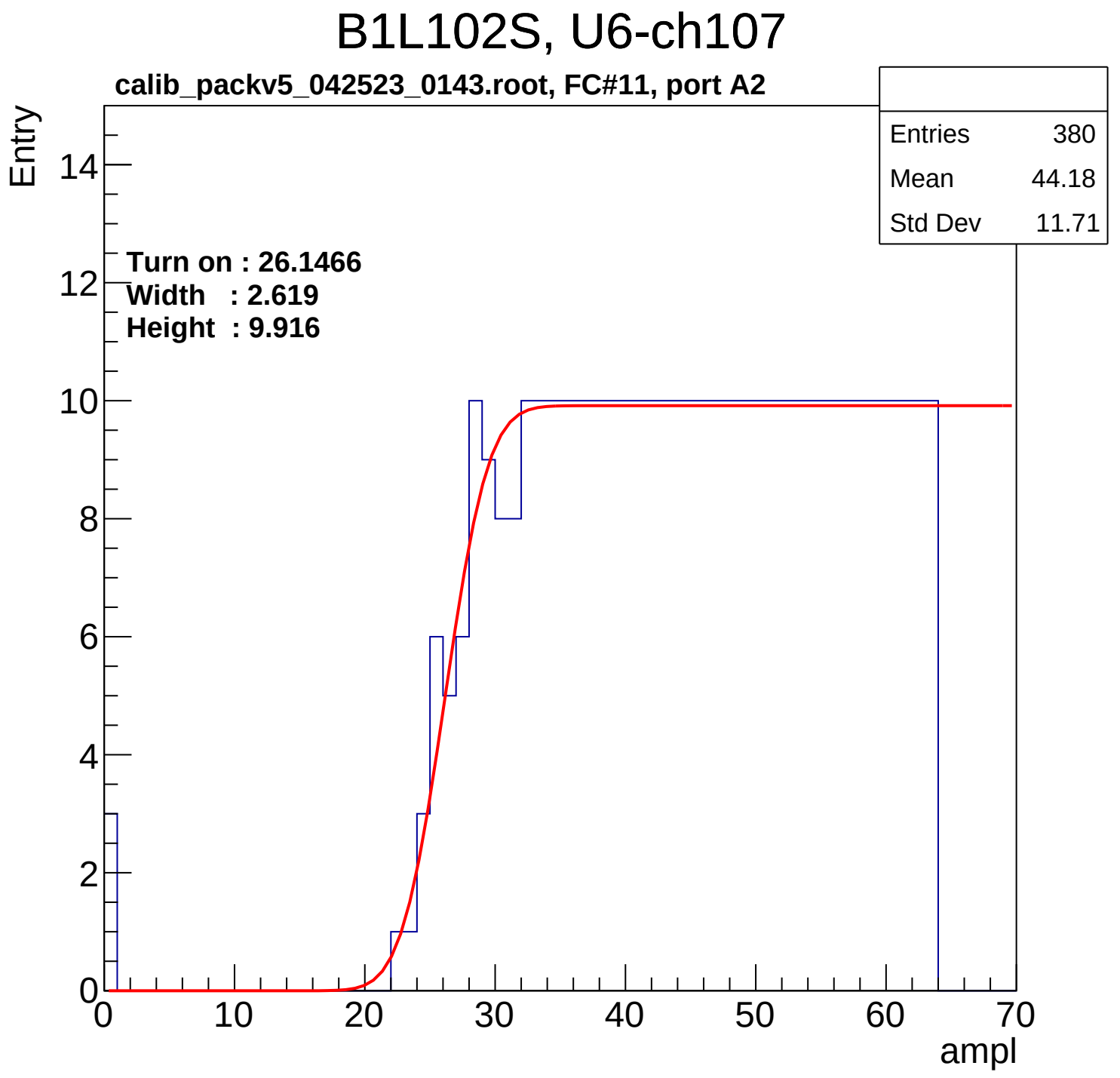
B1L102S, U6-ch107
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.18
Std Dev 11.71
Turn on : 26.1466
Width : 2.619
Height : 9.916
Entry
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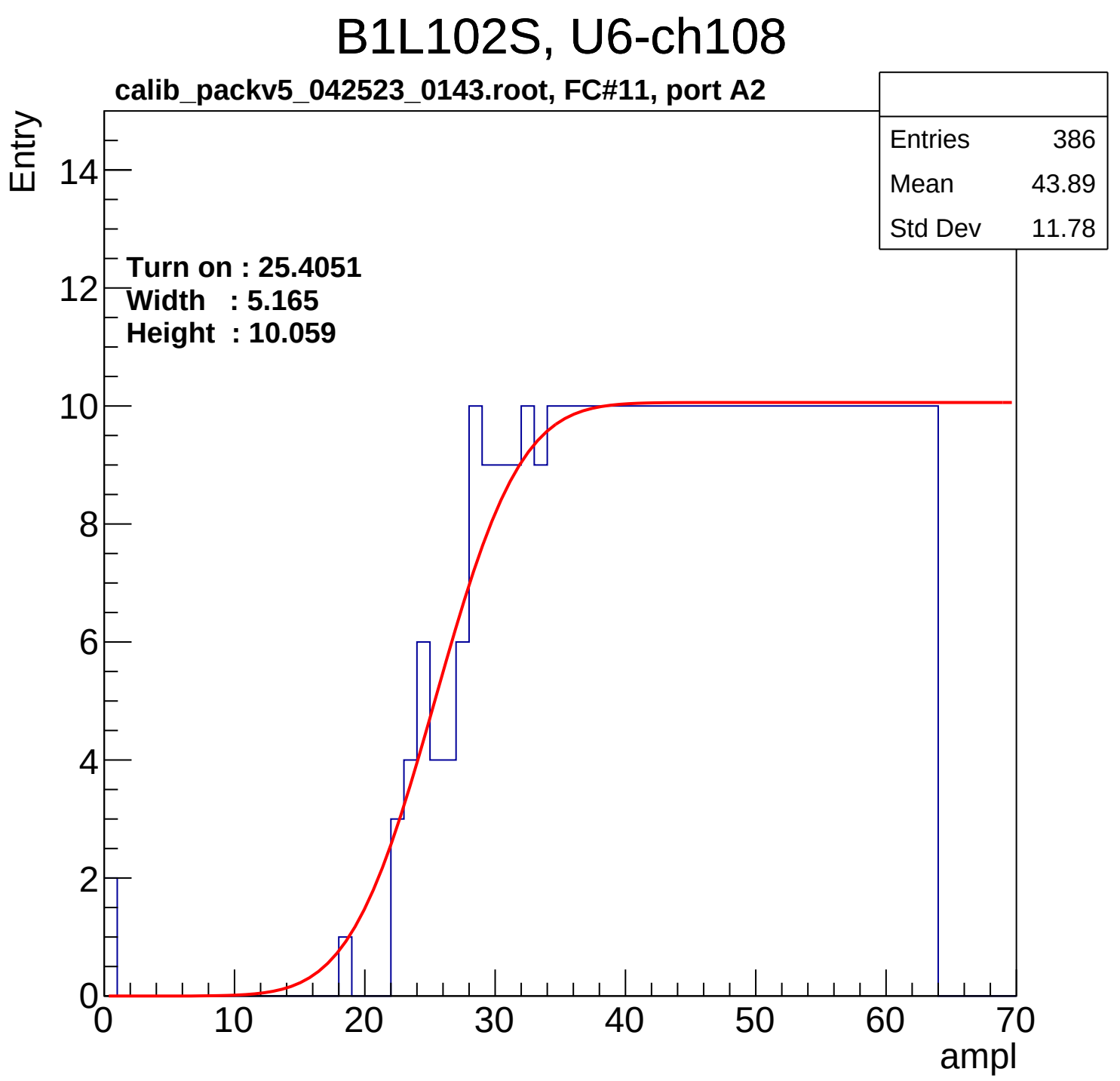
B1L102S, U6-ch108
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.89
Std Dev 11.78
Turn on : 25.4051
Width : 5.165
Height : 10.059
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ampl
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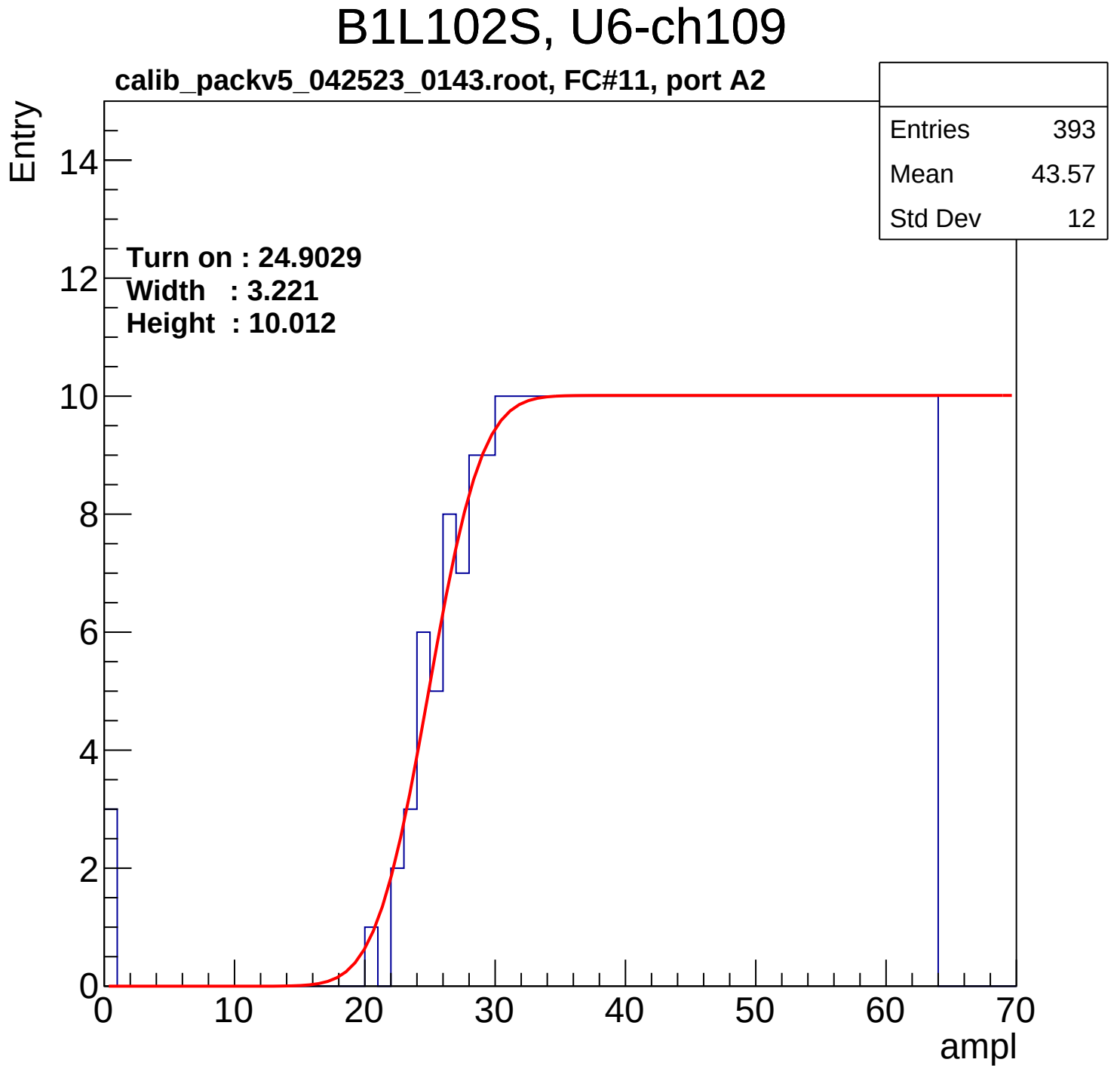
B1L102S, U6-ch109
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.57
Std Dev 12
Turn on : 24.9029
Width : 3.221
Height : 10.012
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ampl
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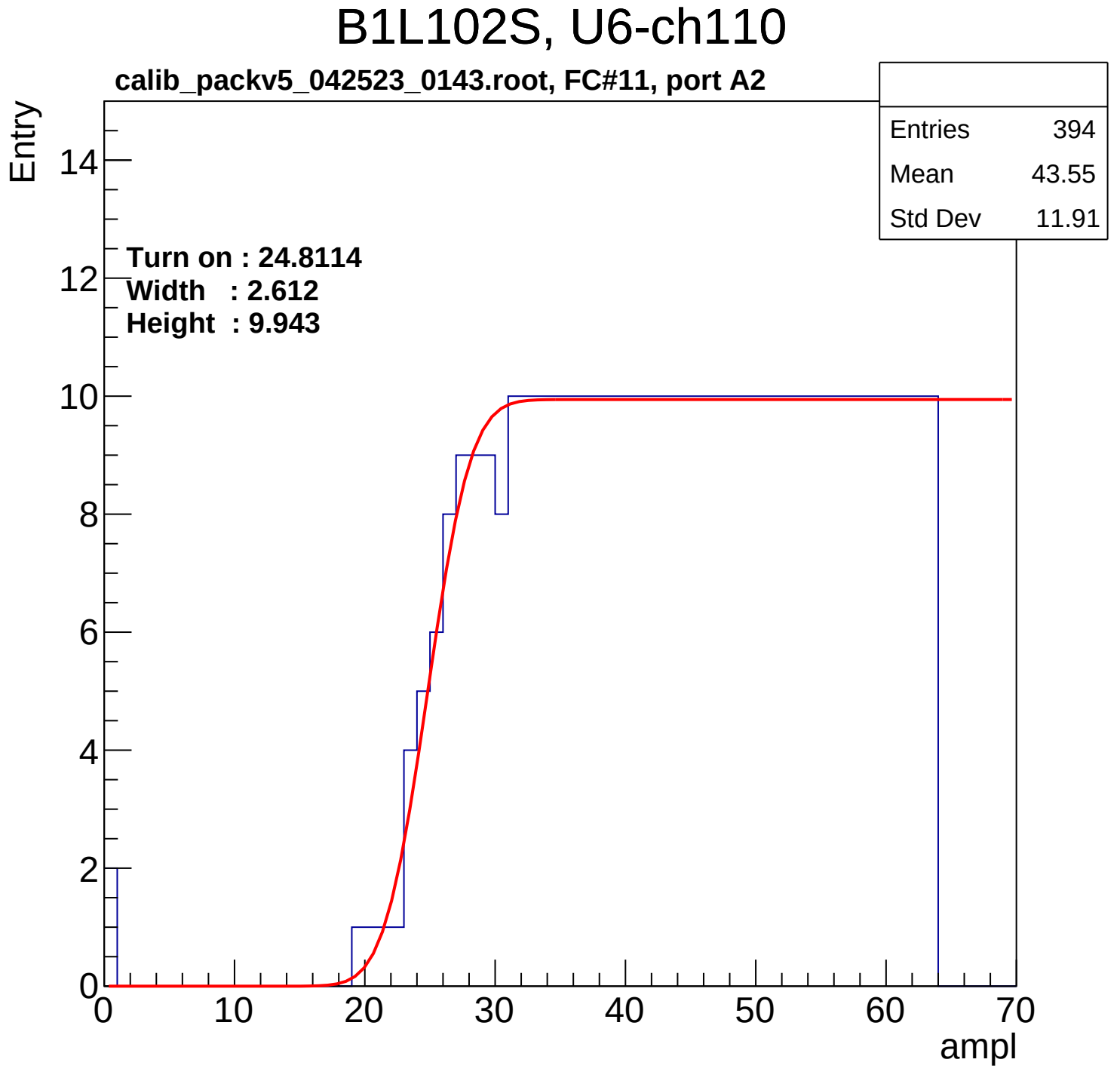
B1L102S, U6-ch110
calib_packv5_042523_0143.root, FC#11, port A2
Entries 394
Mean 43.55
Std Dev 11.91
Turn on : 24.8114
Width : 2.612
Height : 9.943
Entry
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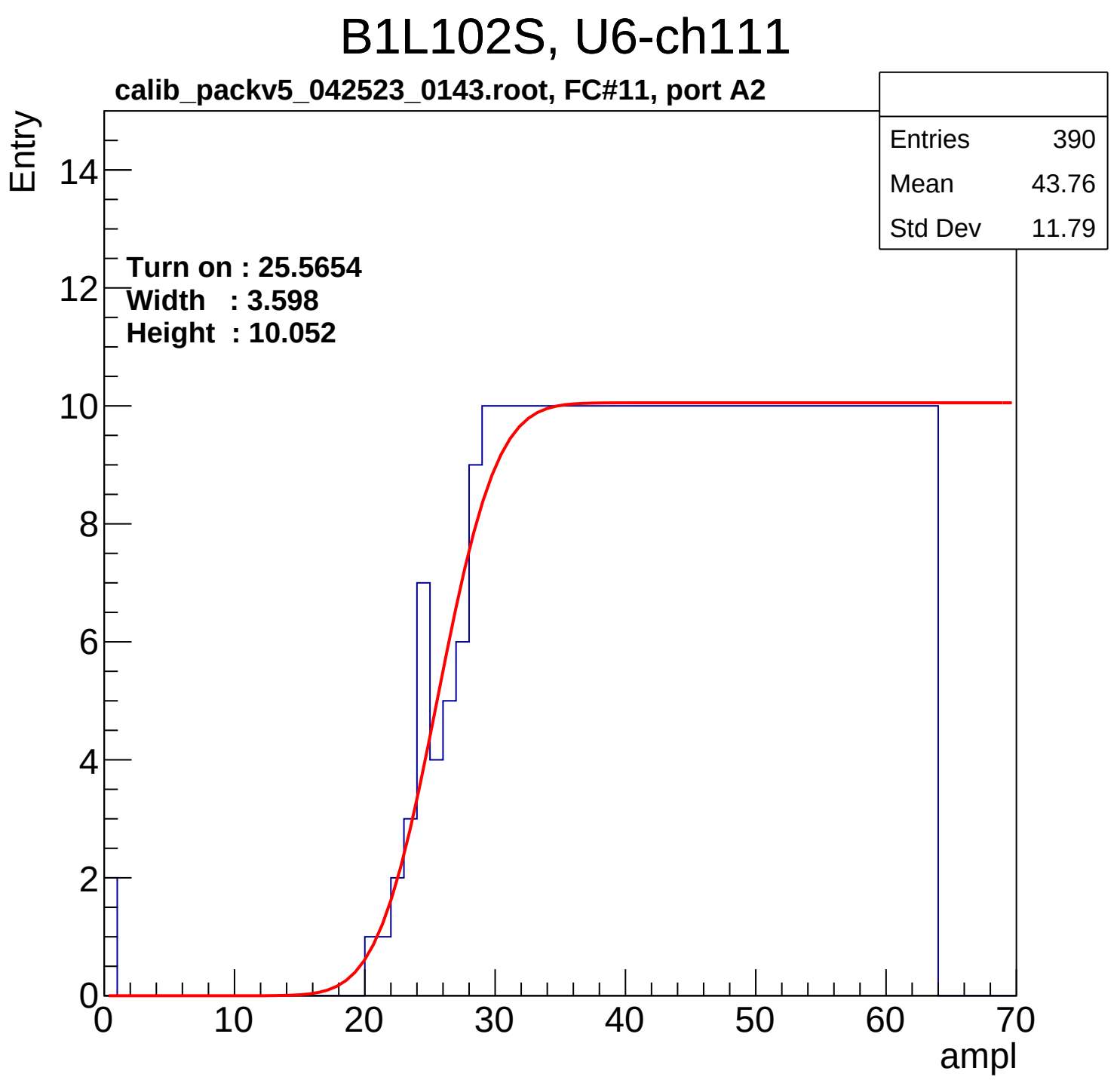
B1L102S, U6-ch111
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.76
Std Dev 11.79
Turn on : 25.5654
Width : 3.598
Height : 10.052
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ampl
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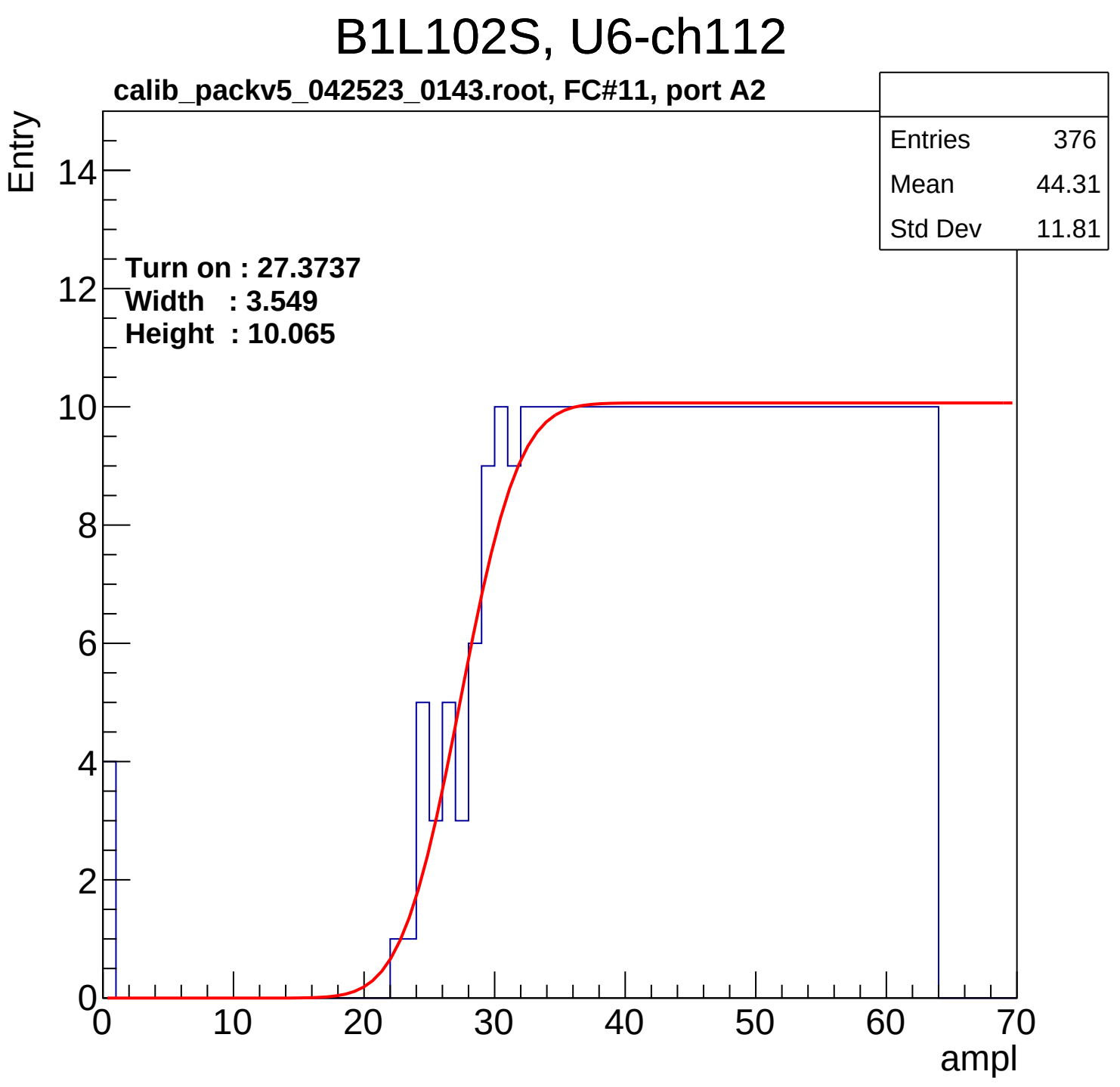
B1L102S, U6-ch112
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.31
Std Dev 11.81
Turn on : 27.3737
Width : 3.549
Height : 10.065
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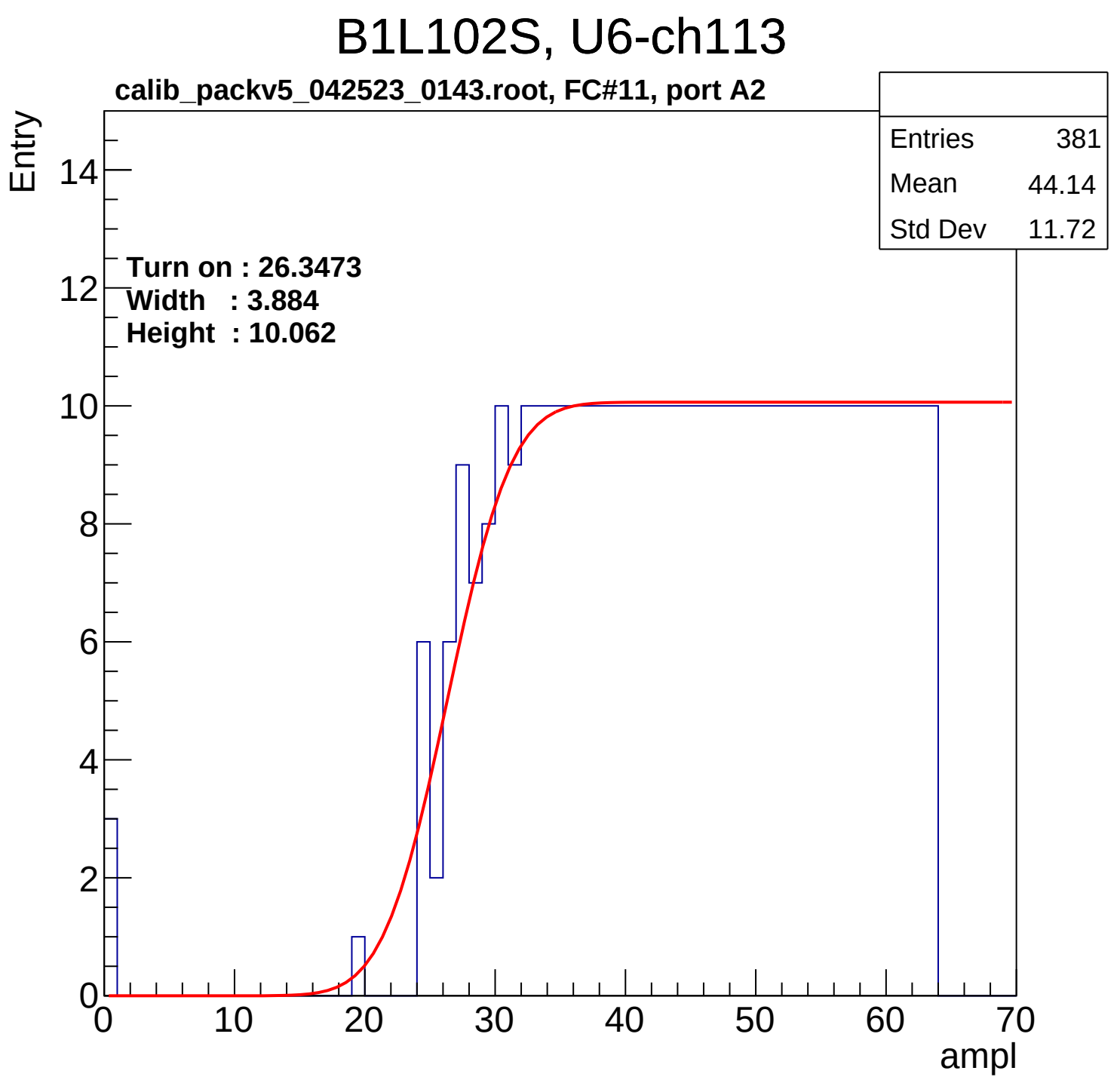
B1L102S, U6-ch113
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.14
Std Dev 11.72
Turn on : 26.3473
Width : 3.884
Height : 10.062
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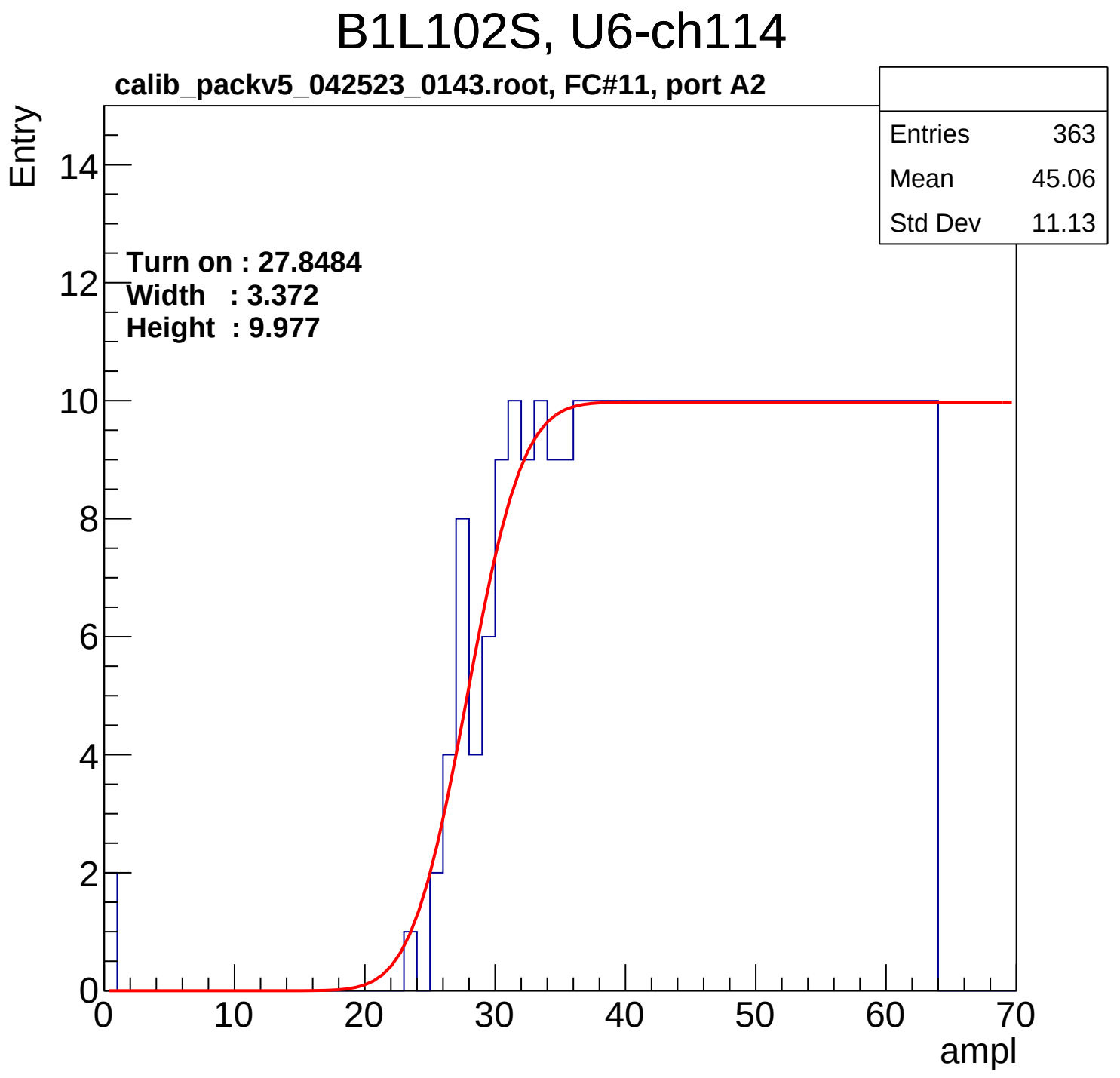
B1L102S, U6-ch114
calib_packv5_042523_0143.root, FC#11, port A2
Entries 363
Mean 45.06
Std Dev 11.13
Turn on : 27.8484
Width : 3.372
Height : 9.977
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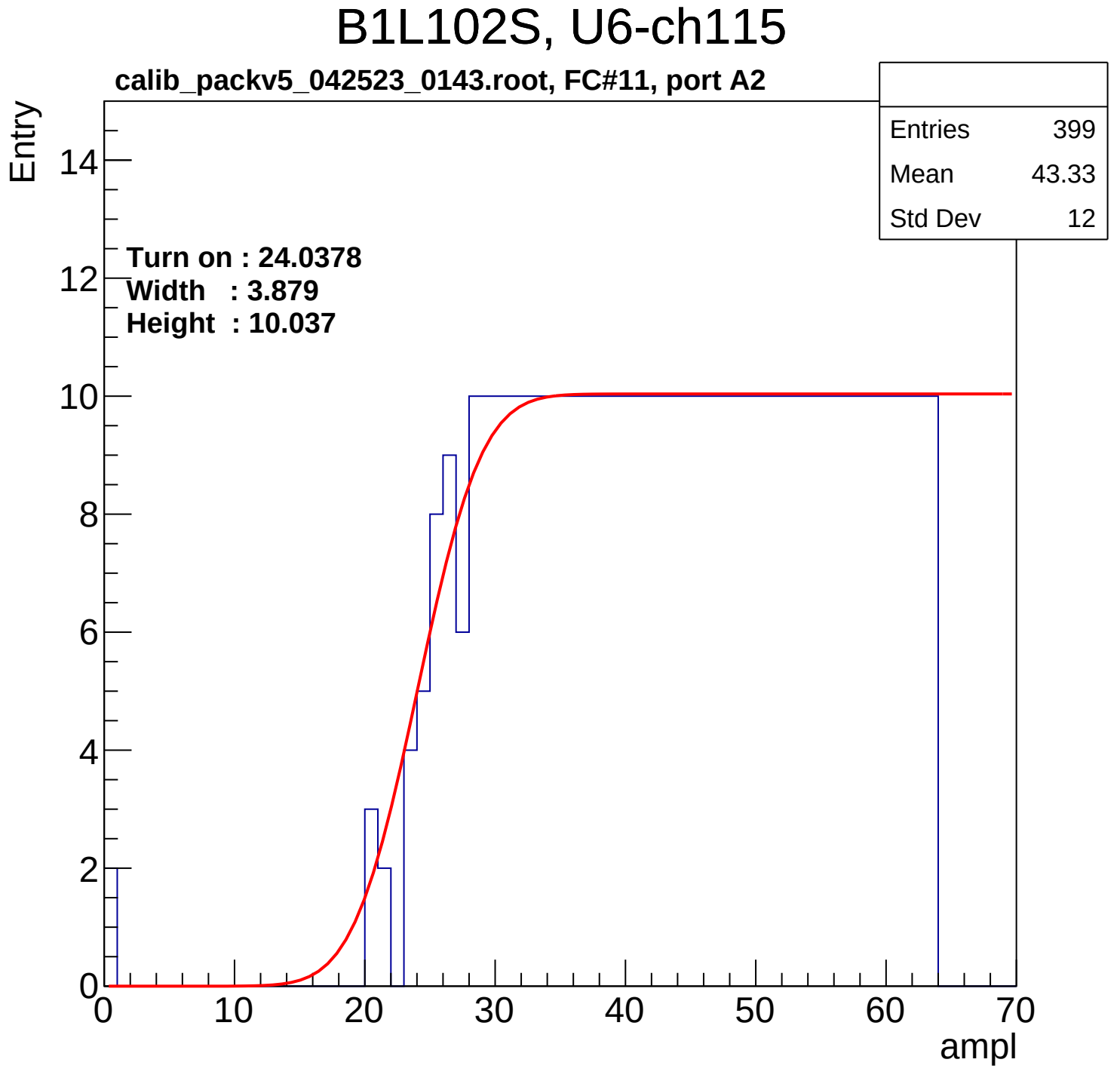
B1L102S, U6-ch115
calib_packv5_042523_0143.root, FC#11, port A2
Entries 399
Mean 43.33
Std Dev 12
Turn on : 24.0378
Width : 3.879
Height : 10.037
Entry
ampl
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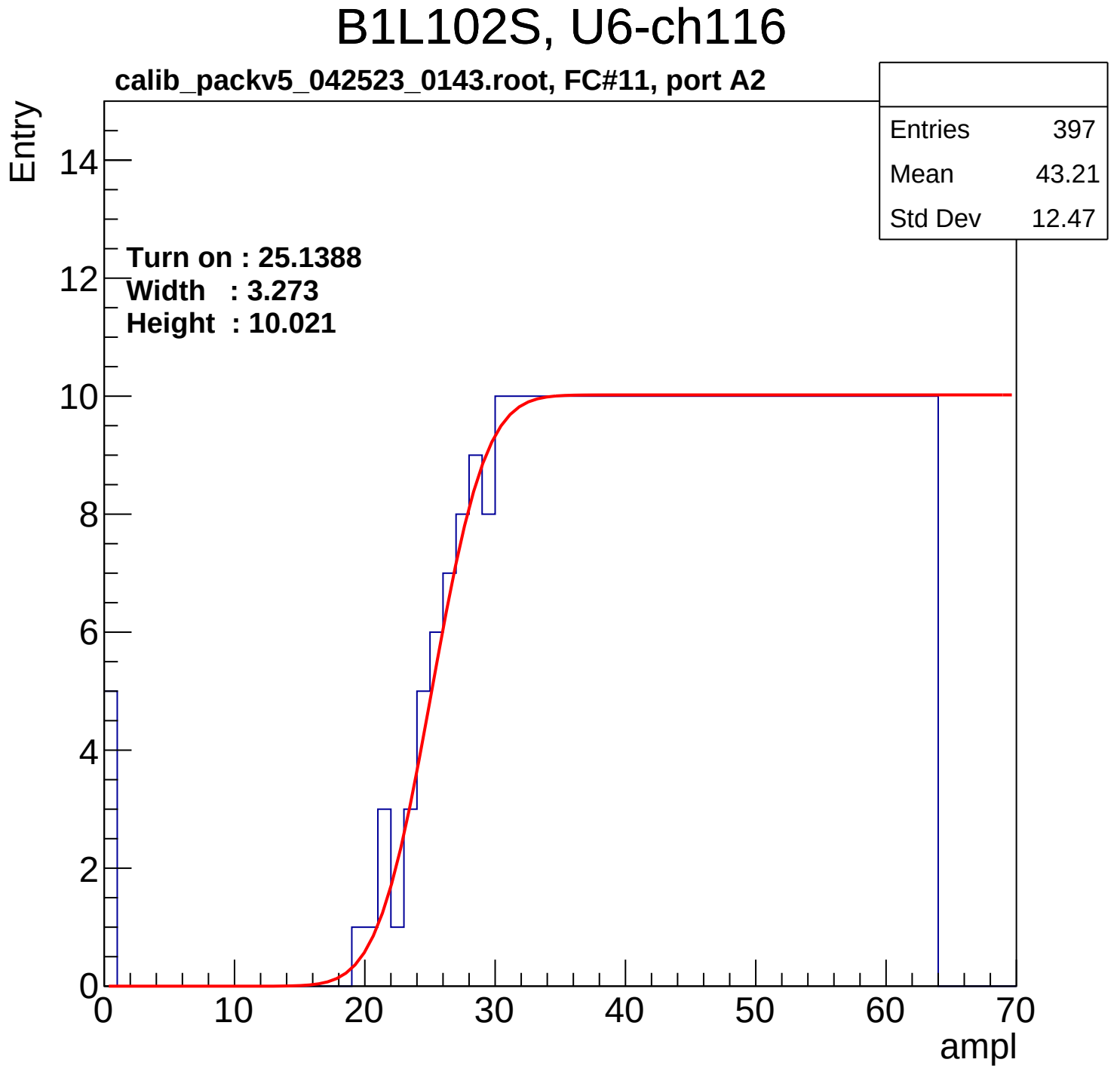
B1L102S, U6-ch116
calib_packv5_042523_0143.root, FC#11, port A2
Entries 397
Mean 43.21
Std Dev 12.47
Turn on : 25.1388
Width : 3.273
Height : 10.021
Entry
ampl
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4
6
8
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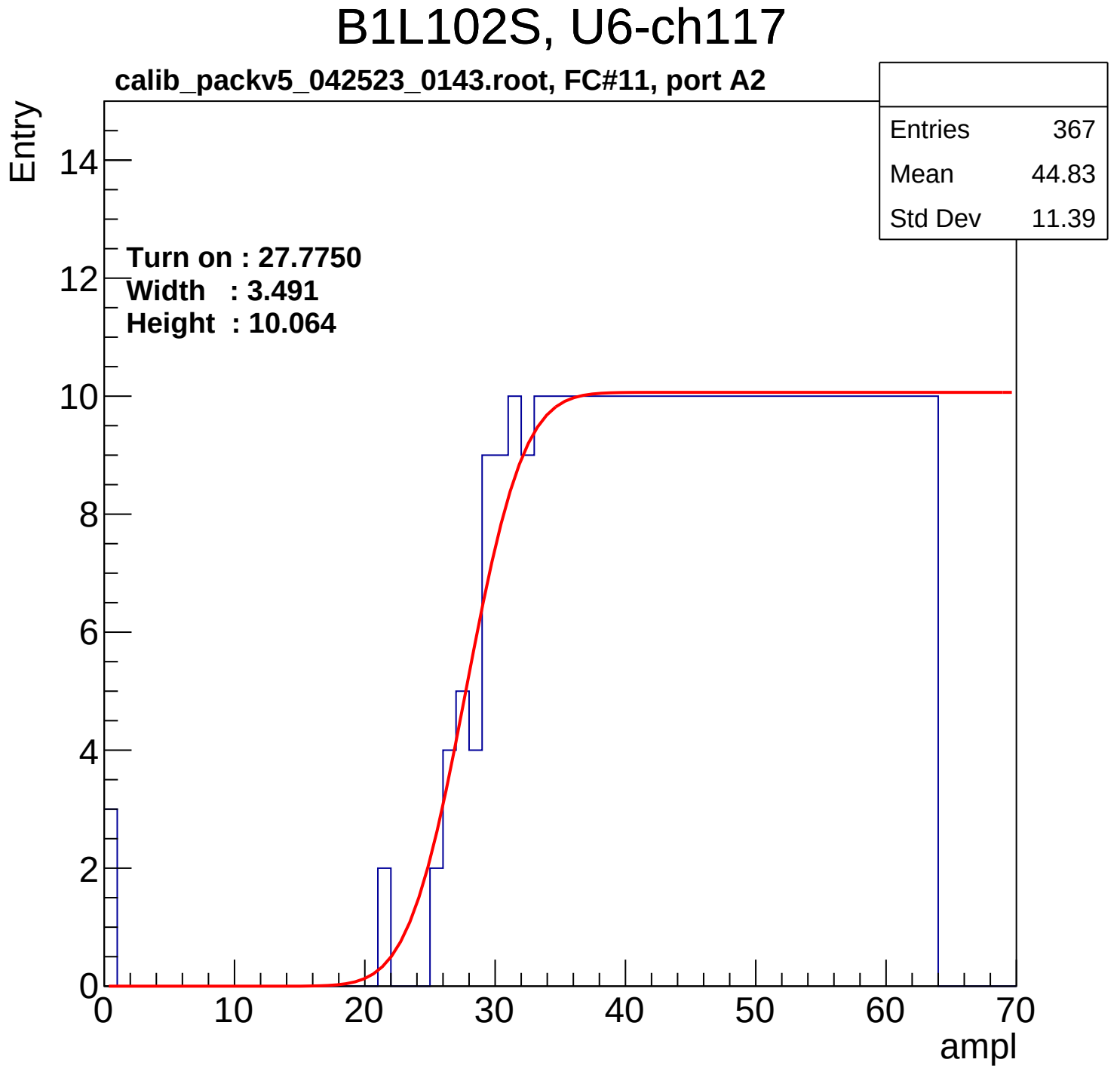
B1L102S, U6-ch117
calib_packv5_042523_0143.root, FC#11, port A2
Entries 367
Mean 44.83
Std Dev 11.39
Turn on : 27.7750
Width : 3.491
Height : 10.064
Entry
ampl
0
2
4
6
8
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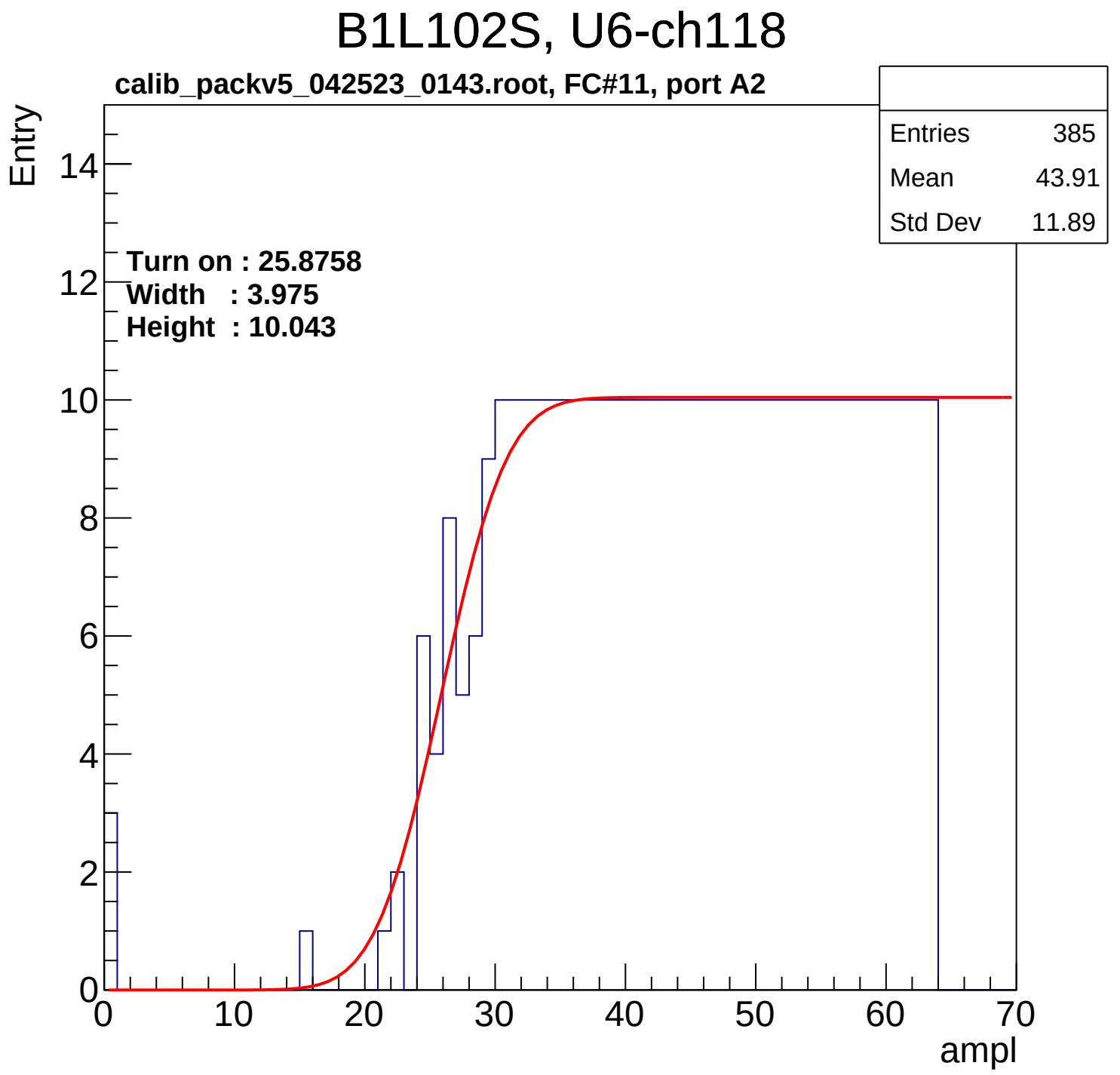
B1L102S, U6-ch118
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.91
Std Dev 11.89
Turn on : 25.8758
Width : 3.975
Height : 10.043
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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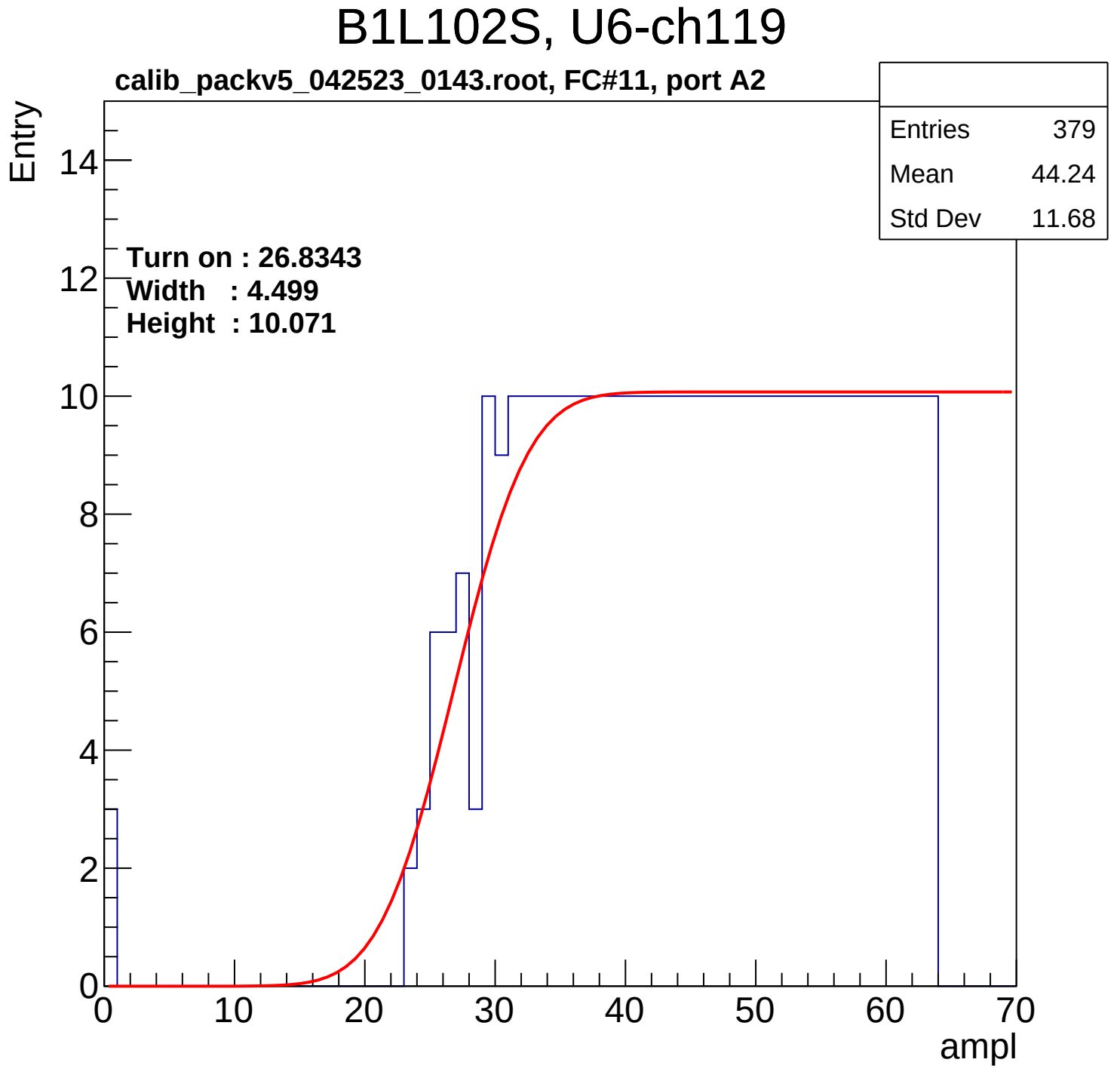
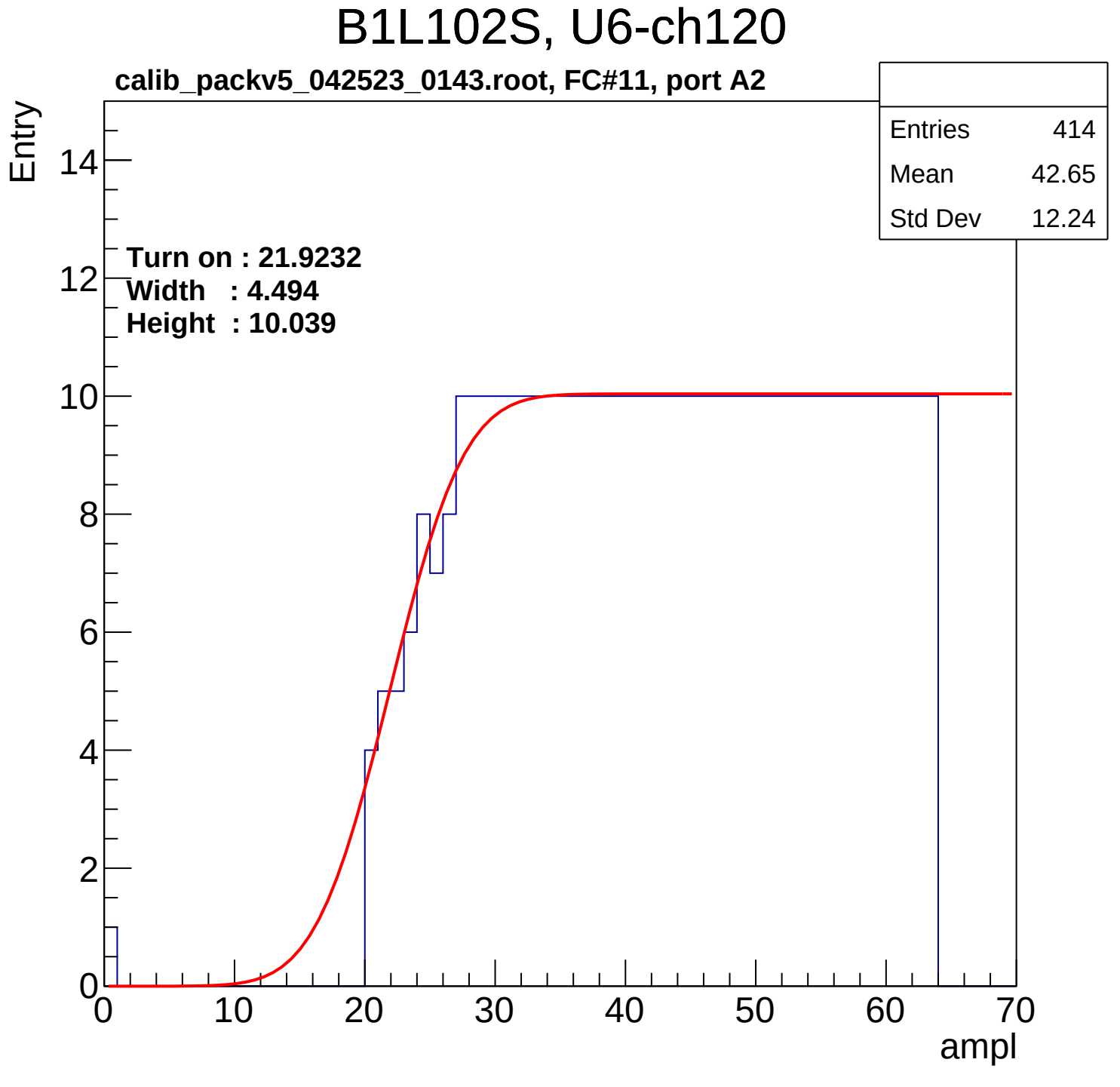

B1L102S, U6-ch119
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.24
Std Dev 11.68
Turn on : 26.8343
Width : 4.499
Height : 10.071
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U6-ch120
calib_packv5_042523_0143.root, FC#11, port A2
Entries 414
Mean 42.65
Std Dev 12.24
Turn on : 21.9232
Width : 4.494
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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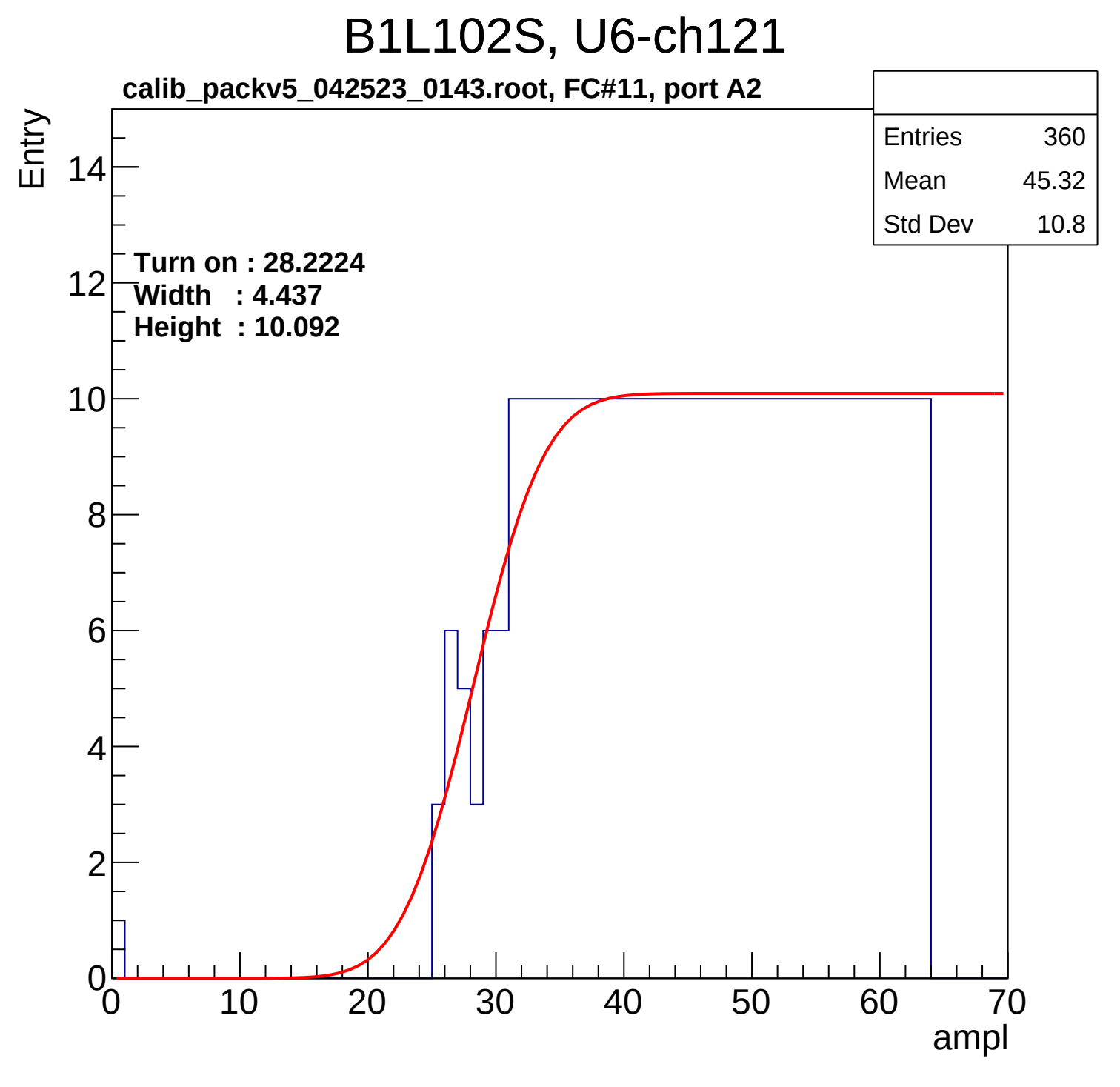
B1L102S, U6-ch121
calib_packv5_042523_0143.root, FC#11, port A2
Entries 360
Mean 45.32
Std Dev 10.8
Turn on : 28.2224
Width : 4.437
Height : 10.092
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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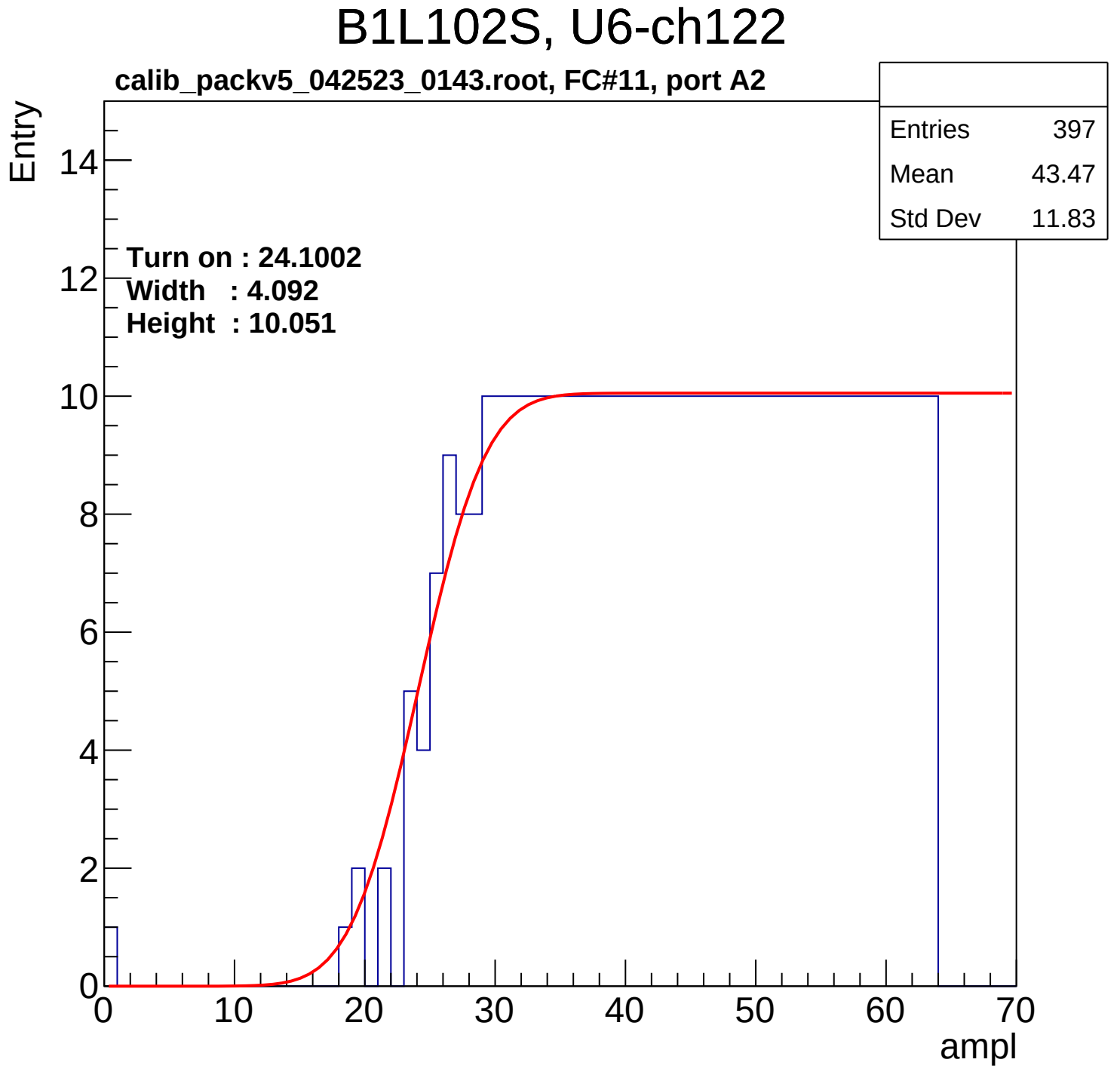
B1L102S, U6-ch122
calib_packv5_042523_0143.root, FC#11, port A2
Entries 397
Mean 43.47
Std Dev 11.83
Turn on : 24.1002
Width : 4.092
Height : 10.051
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
50
60
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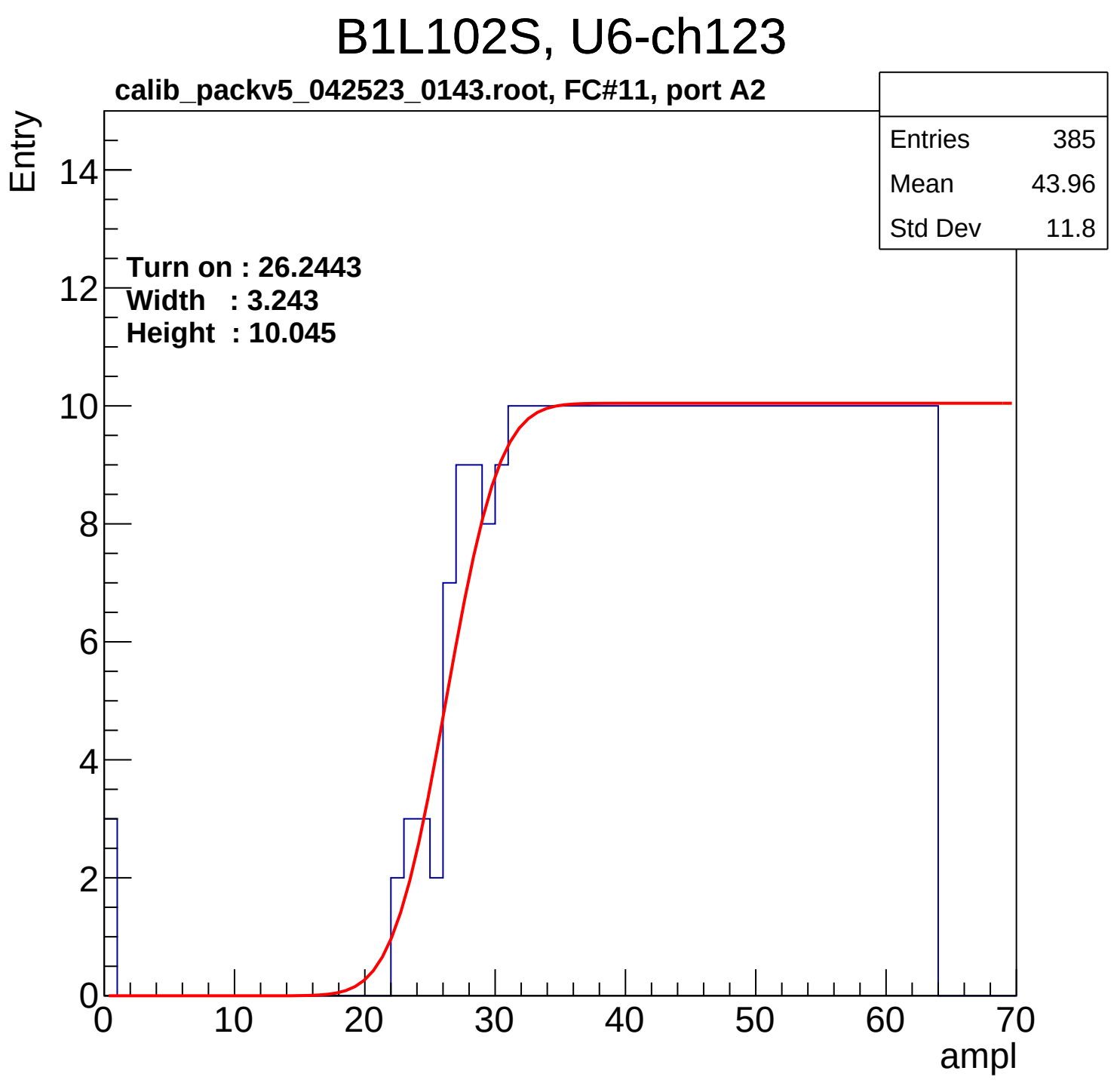
B1L102S, U6-ch123
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.96
Std Dev 11.8
Turn on : 26.2443
Width : 3.243
Height : 10.045
Entry
ampl
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4
6
8
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12
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60
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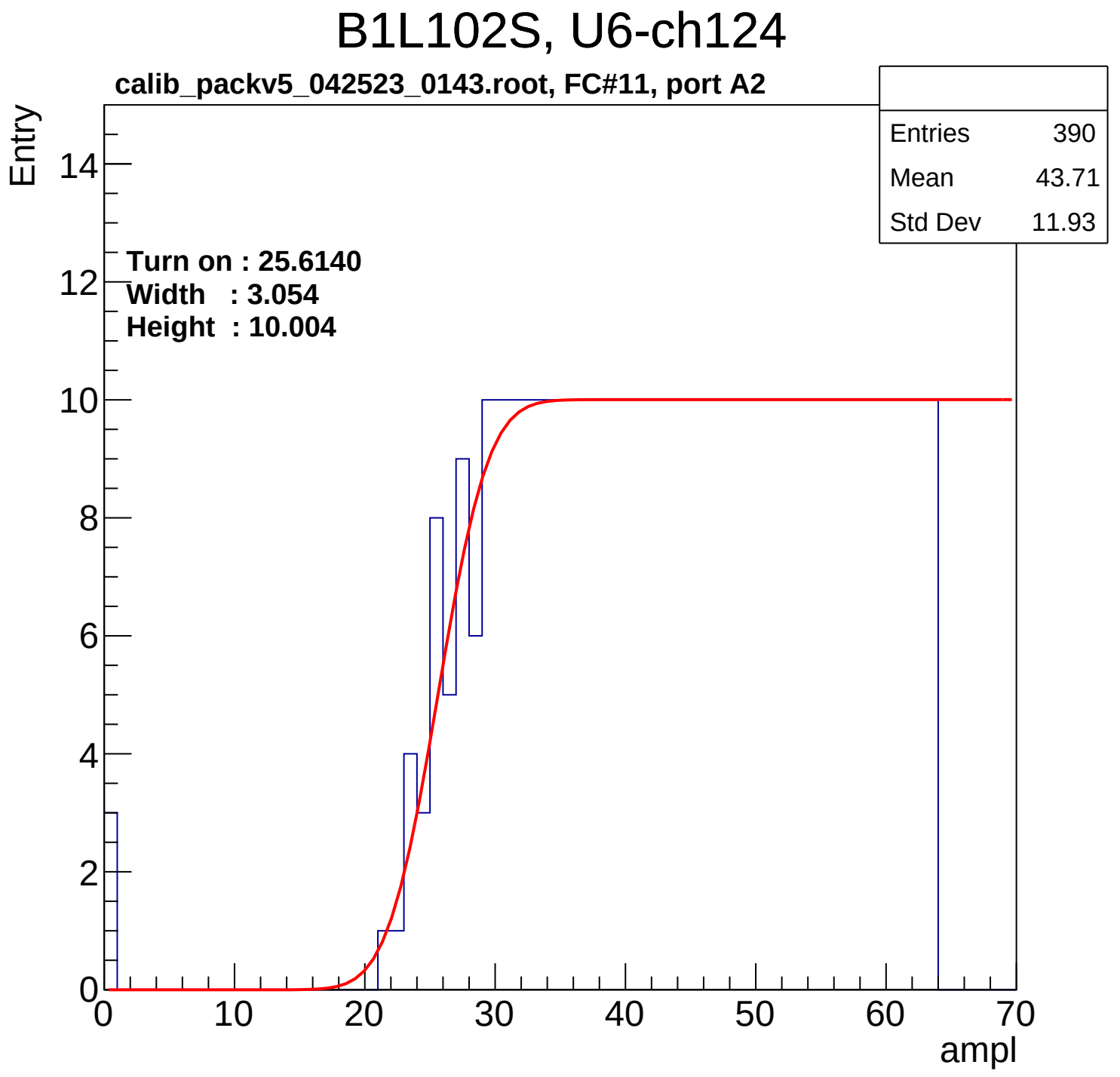
B1L102S, U6-ch124
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.71
Std Dev 11.93
Turn on : 25.6140
Width : 3.054
Height : 10.004
Entry
ampl
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2
4
6
8
10
12
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0
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20
30
40
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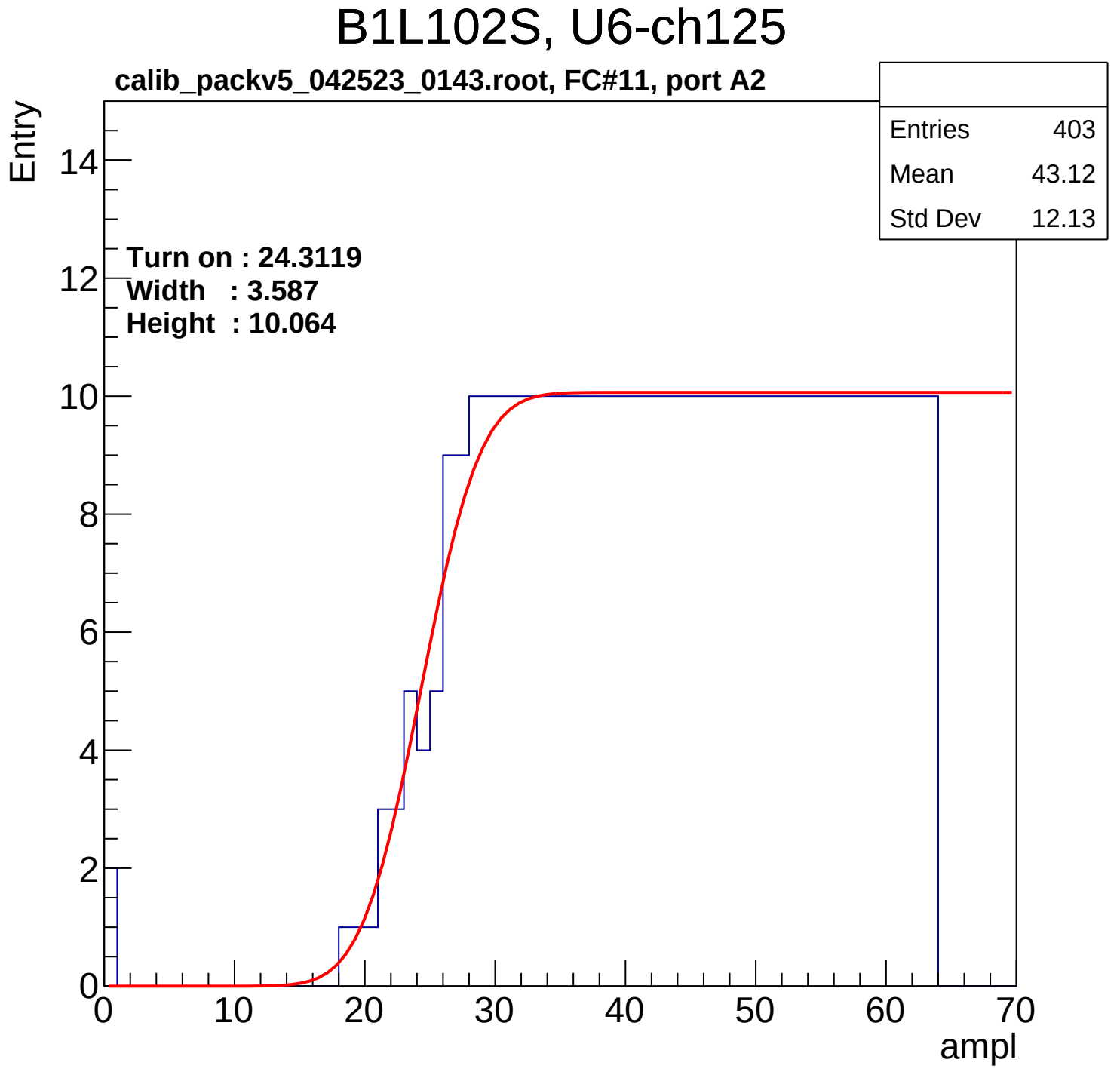
60
70


B1L102S, U6-ch125
calib_packv5_042523_0143.root, FC#11, port A2
Entries 403
Mean 43.12
Std Dev 12.13
Turn on : 24.3119
Width : 3.587
Height : 10.064
Entry
ampl
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6
8
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10
20
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40
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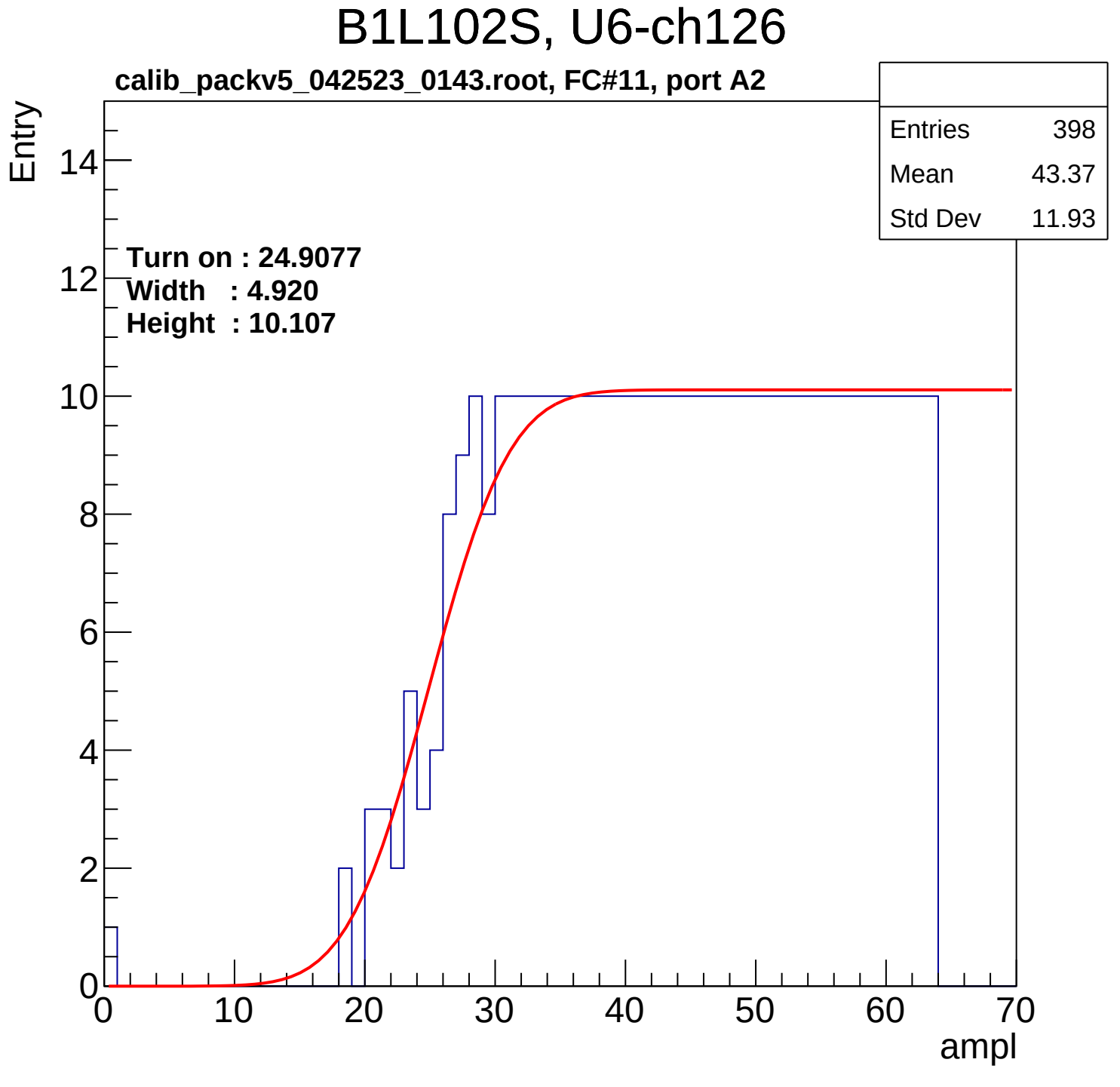
60
70


B1L102S, U6-ch126
calib_packv5_042523_0143.root, FC#11, port A2
Entries 398
Mean 43.37
Std Dev 11.93
Turn on : 24.9077
Width : 4.920
Height : 10.107
Entry
ampl
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6
8
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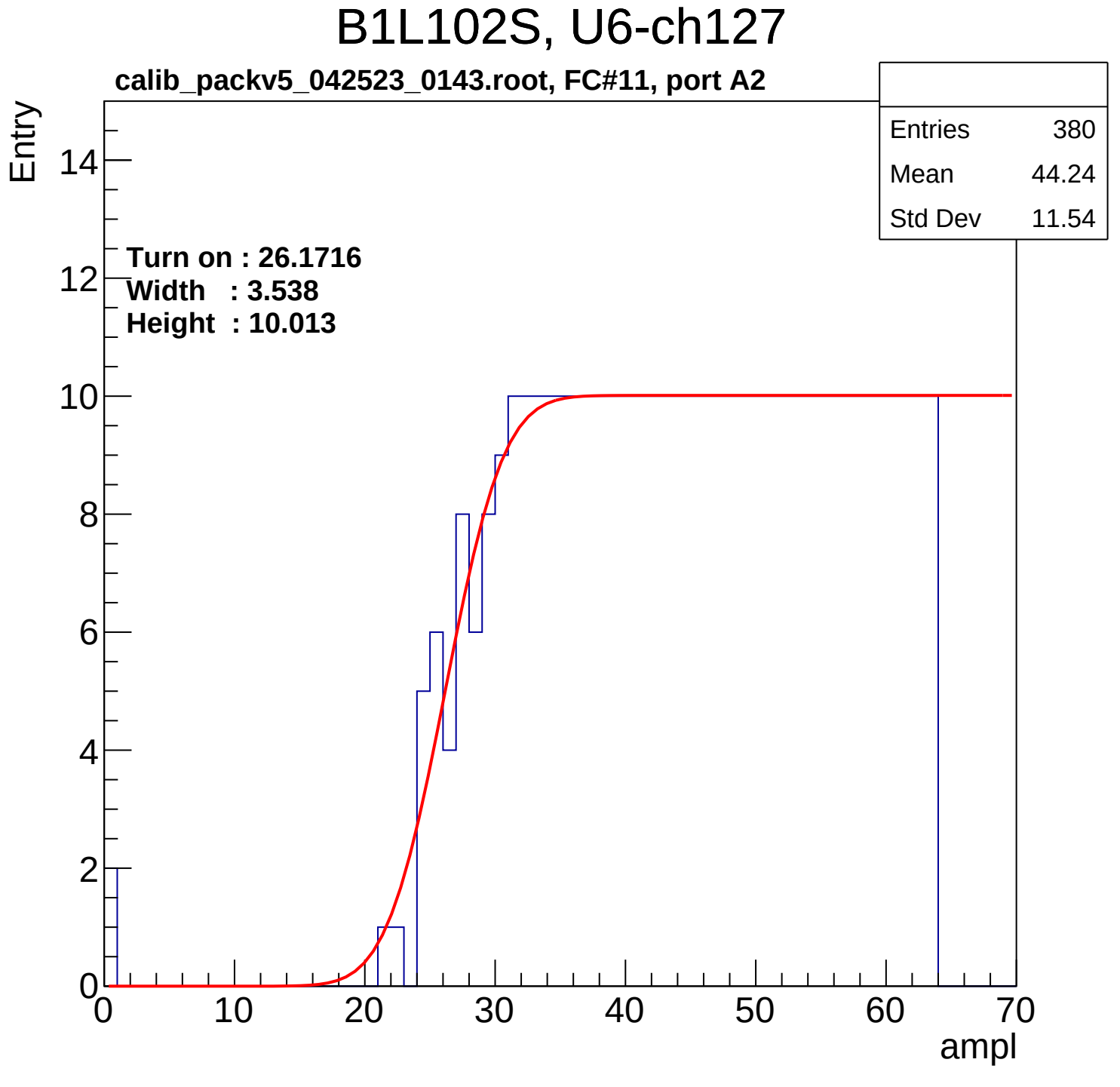
B1L102S, U6-ch127
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.24
Std Dev 11.54
Turn on : 26.1716
Width : 3.538
Height : 10.013
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
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60
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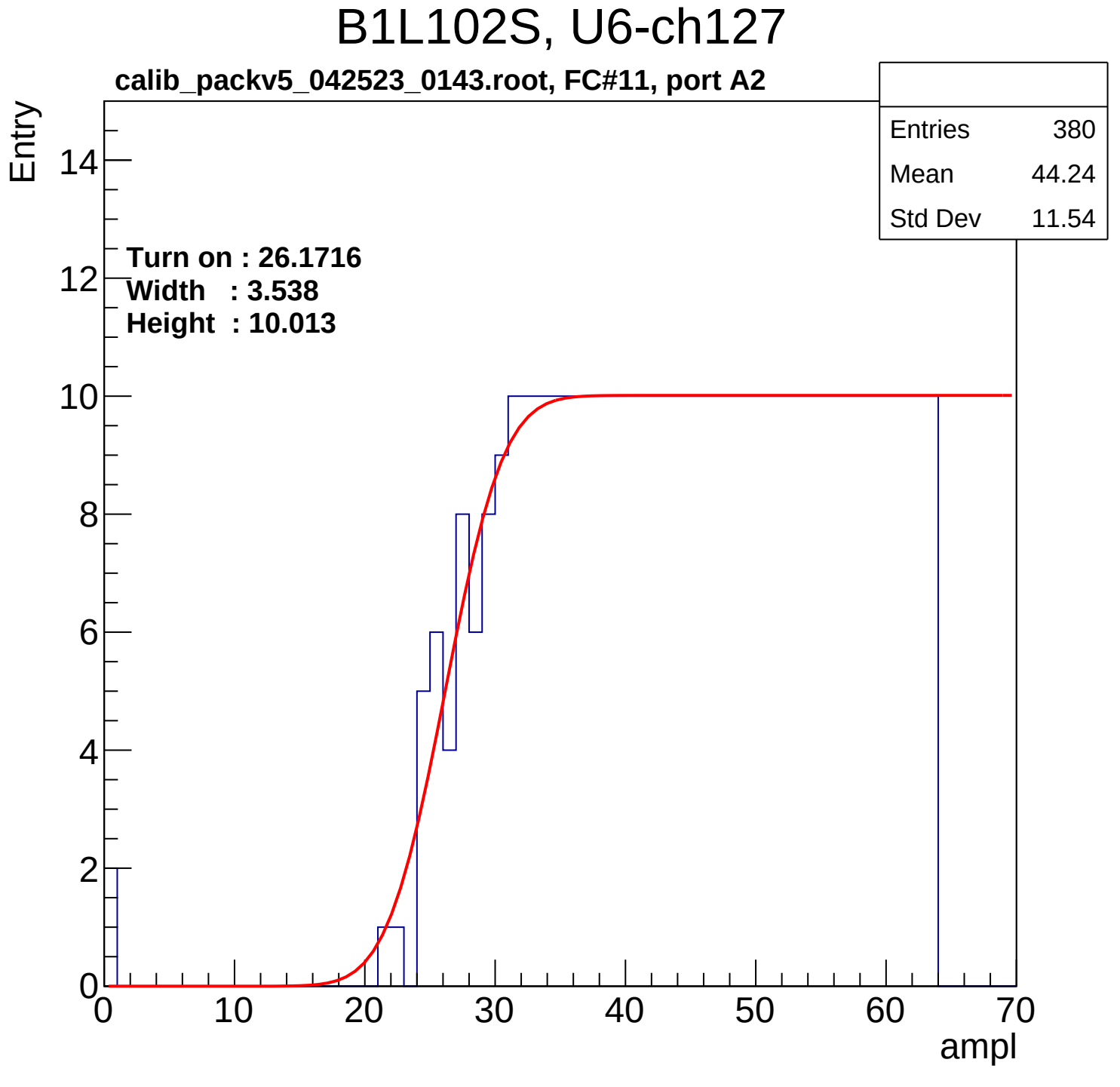
B1L102S, U6-ch127
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.24
Std Dev 11.54
Turn on : 26.1716
Width : 3.538
Height : 10.013
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
30
40
50
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70