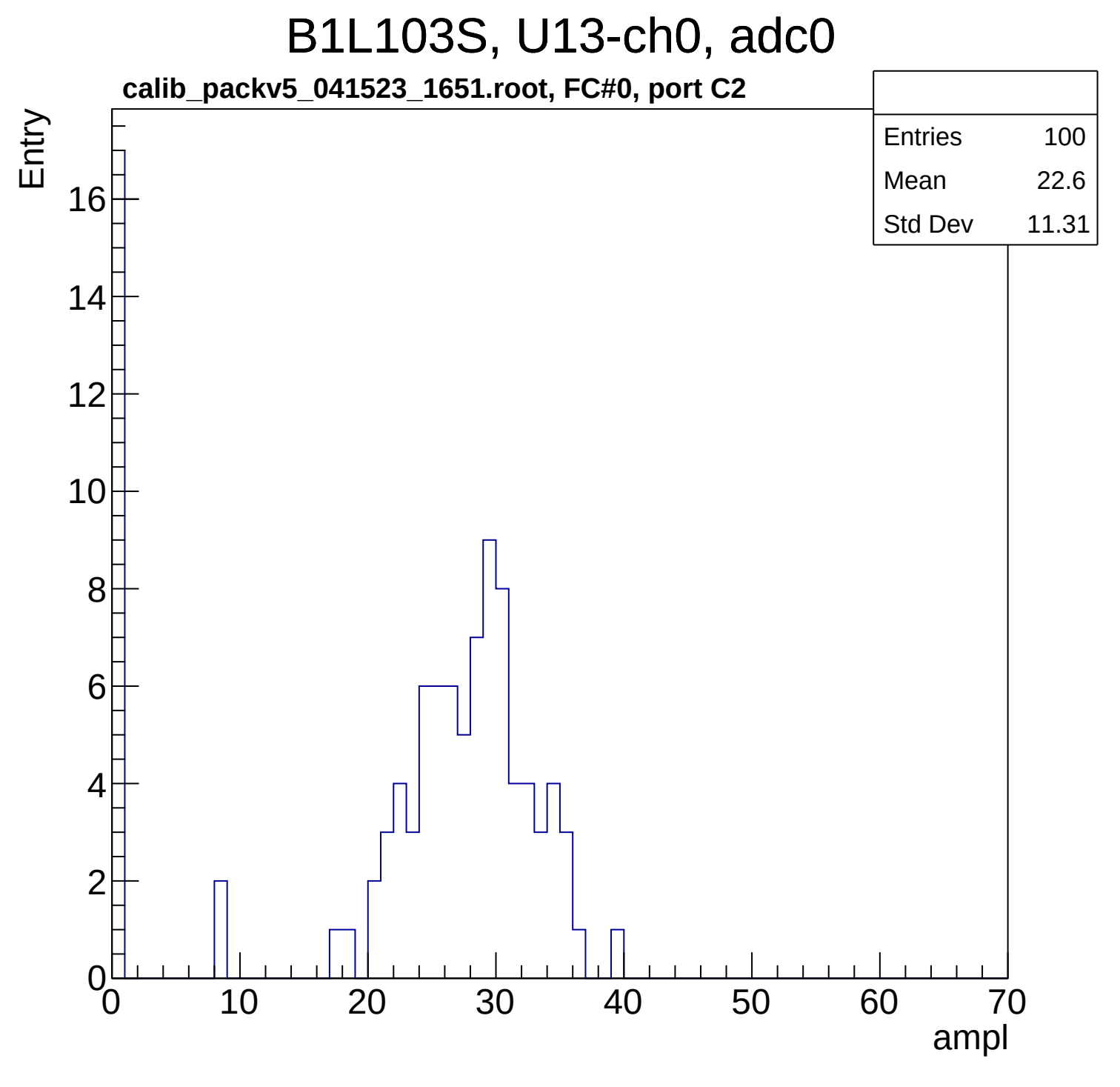
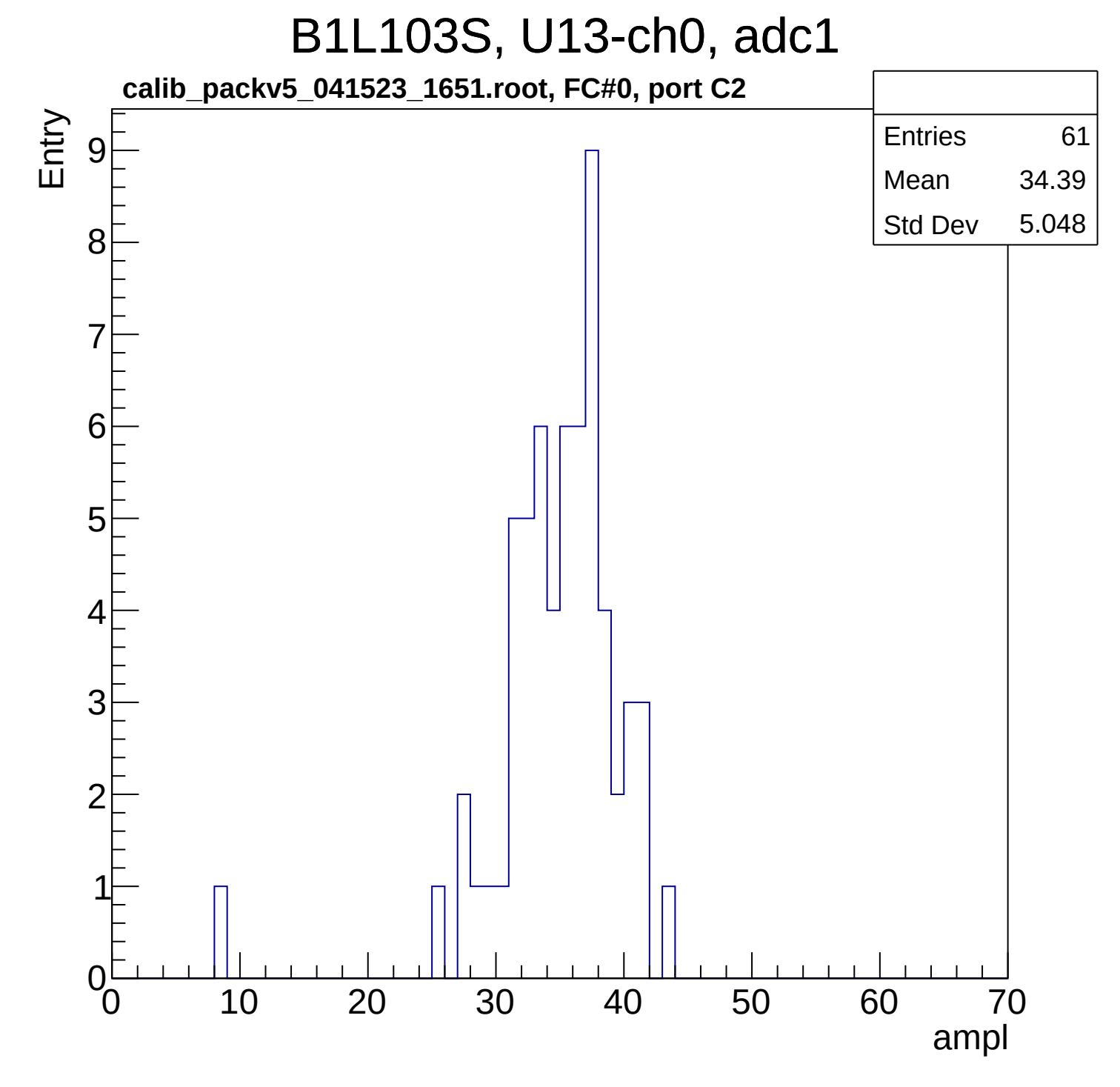

B1L103S, U13-ch0, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 22.6
Std Dev 11.31
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch0, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 34.39
Std Dev 5.048
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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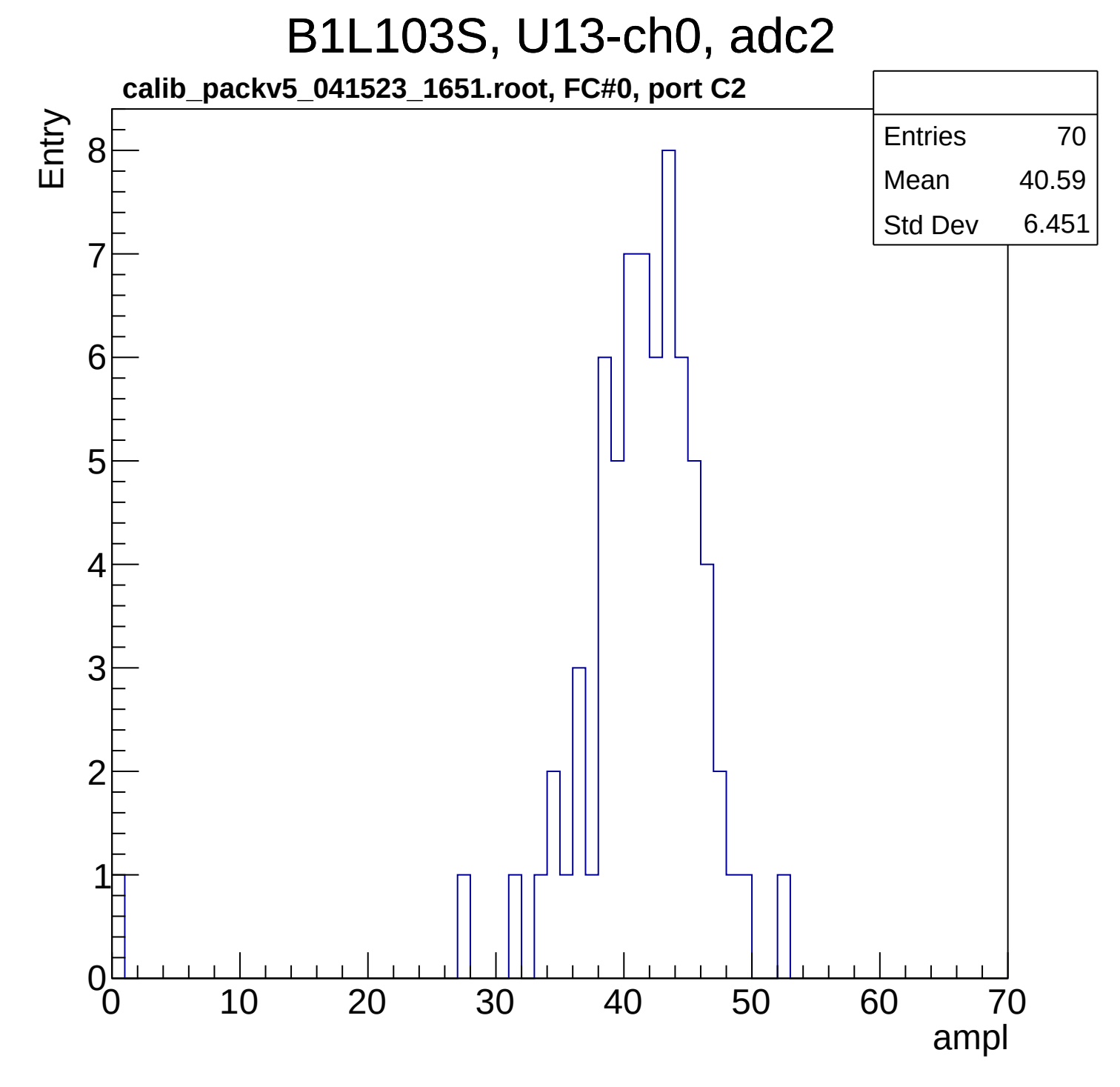
40
50
60
70


B1L103S, U13-ch0, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 40.59
Std Dev 6.451
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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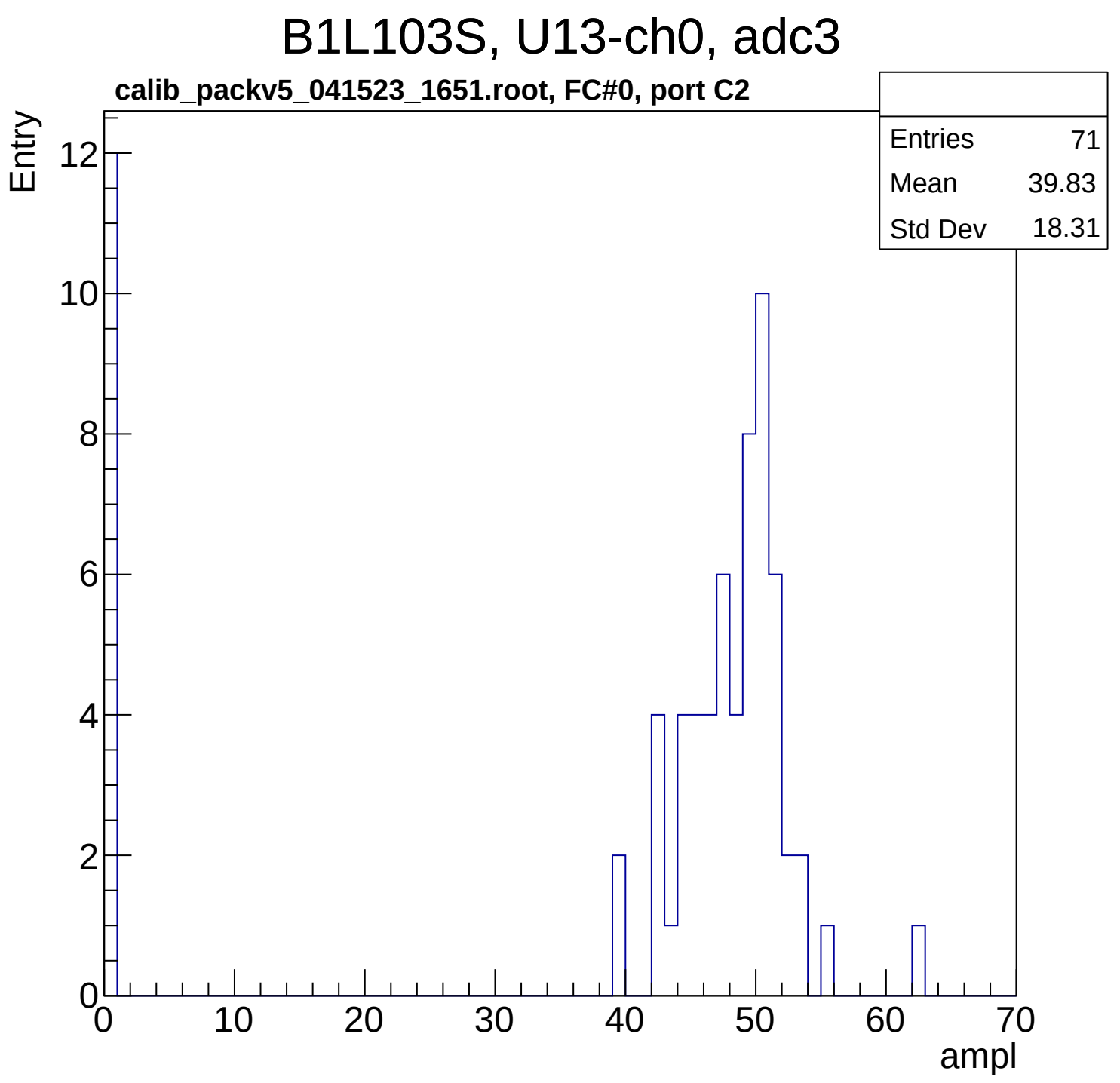
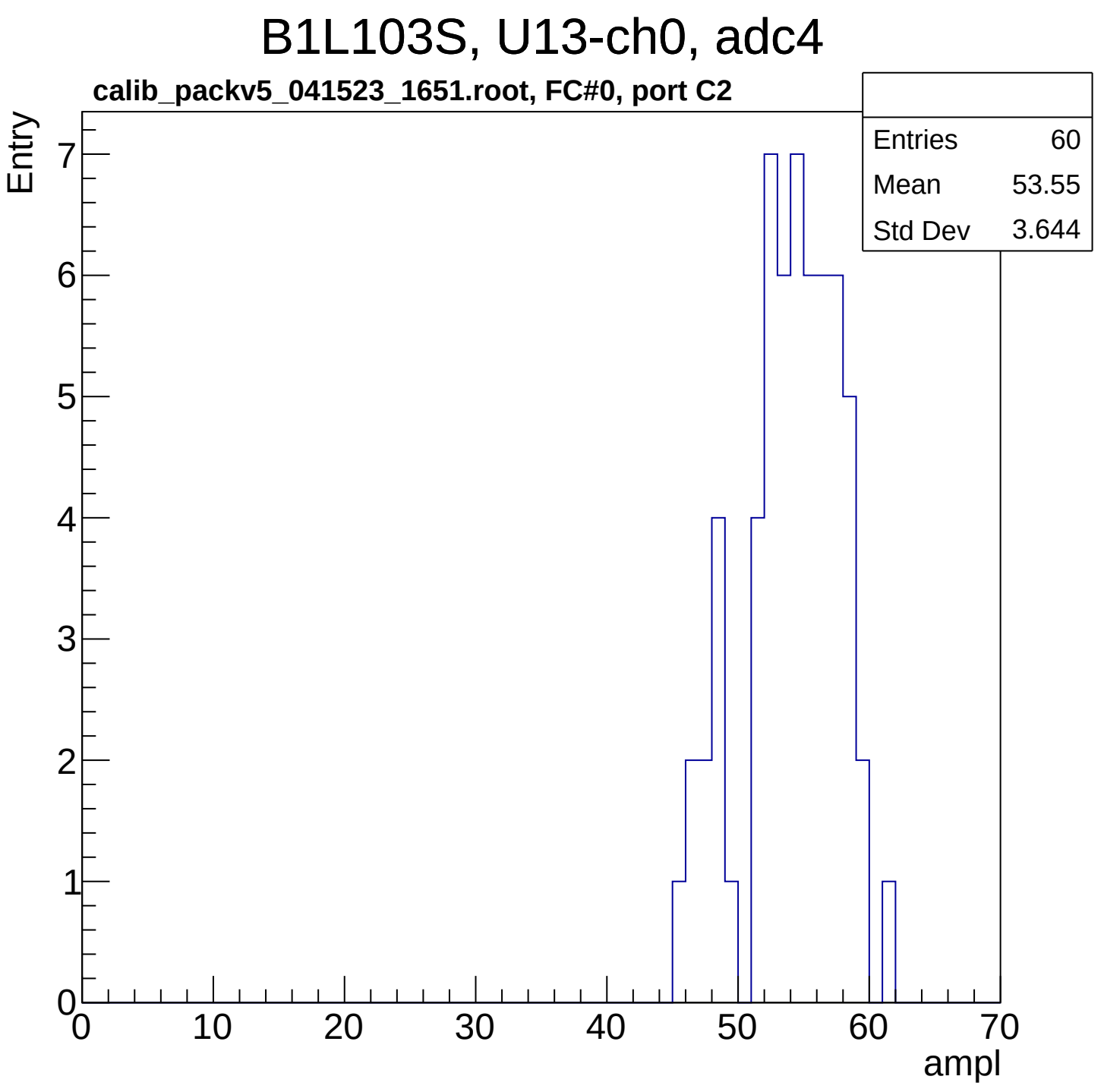
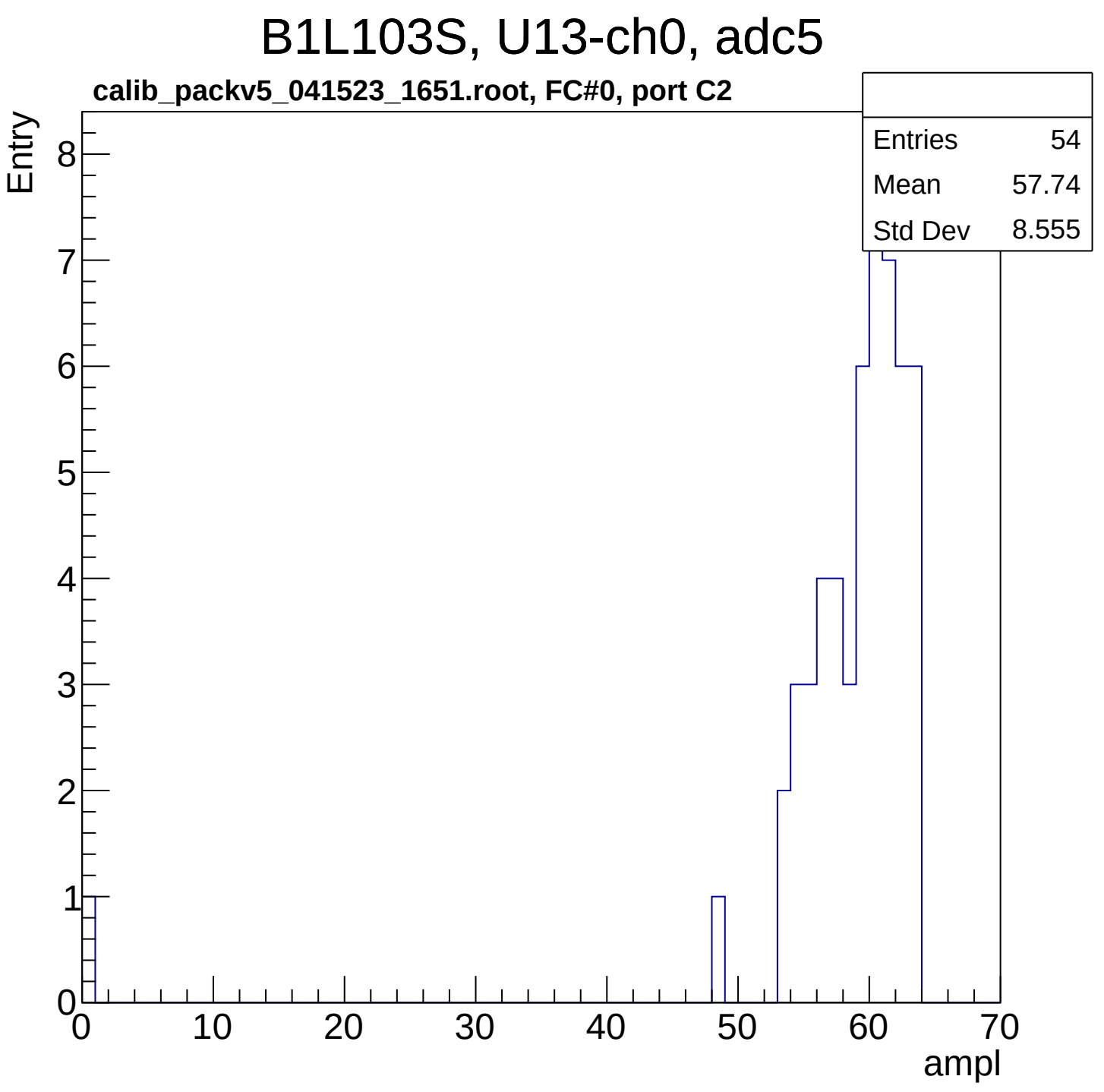

B1L103S, U13-ch0, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 39.83
Std Dev 18.31
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch0, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 53.55
Std Dev 3.644
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch0, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.74
Std Dev 8.555
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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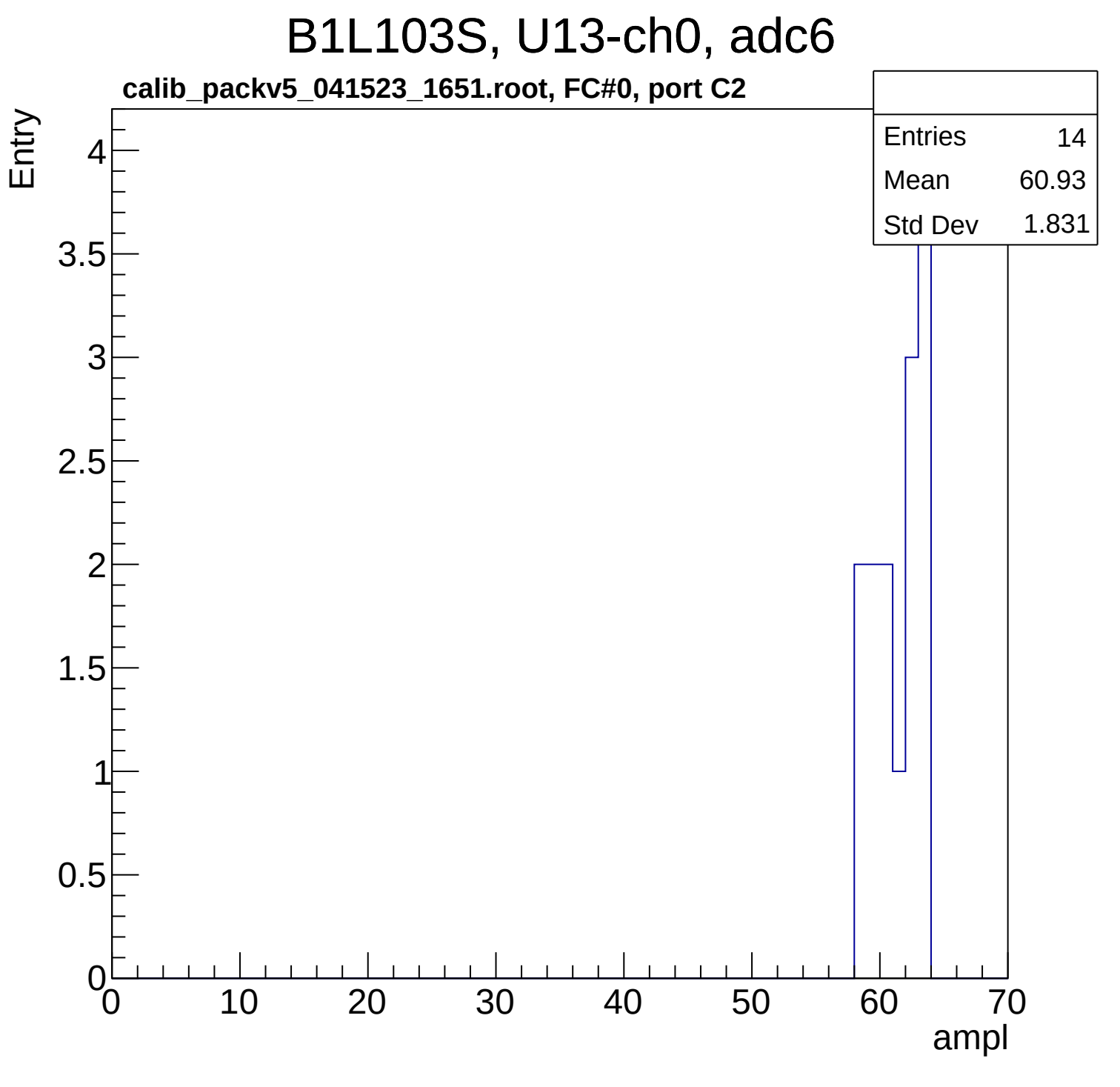
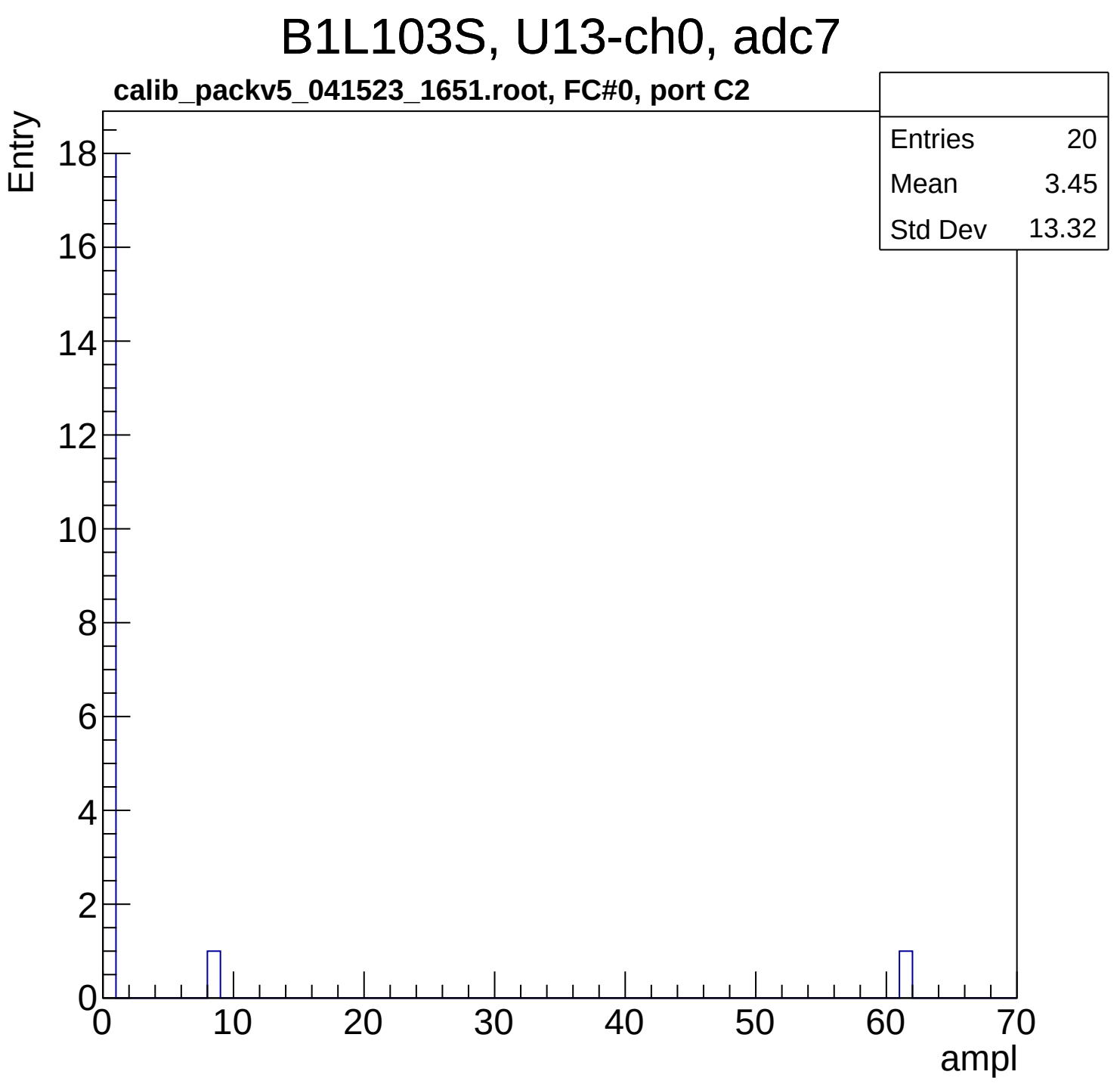

B1L103S, U13-ch0, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 60.93
Std Dev 1.831
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U13-ch0, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.45
Std Dev 13.32
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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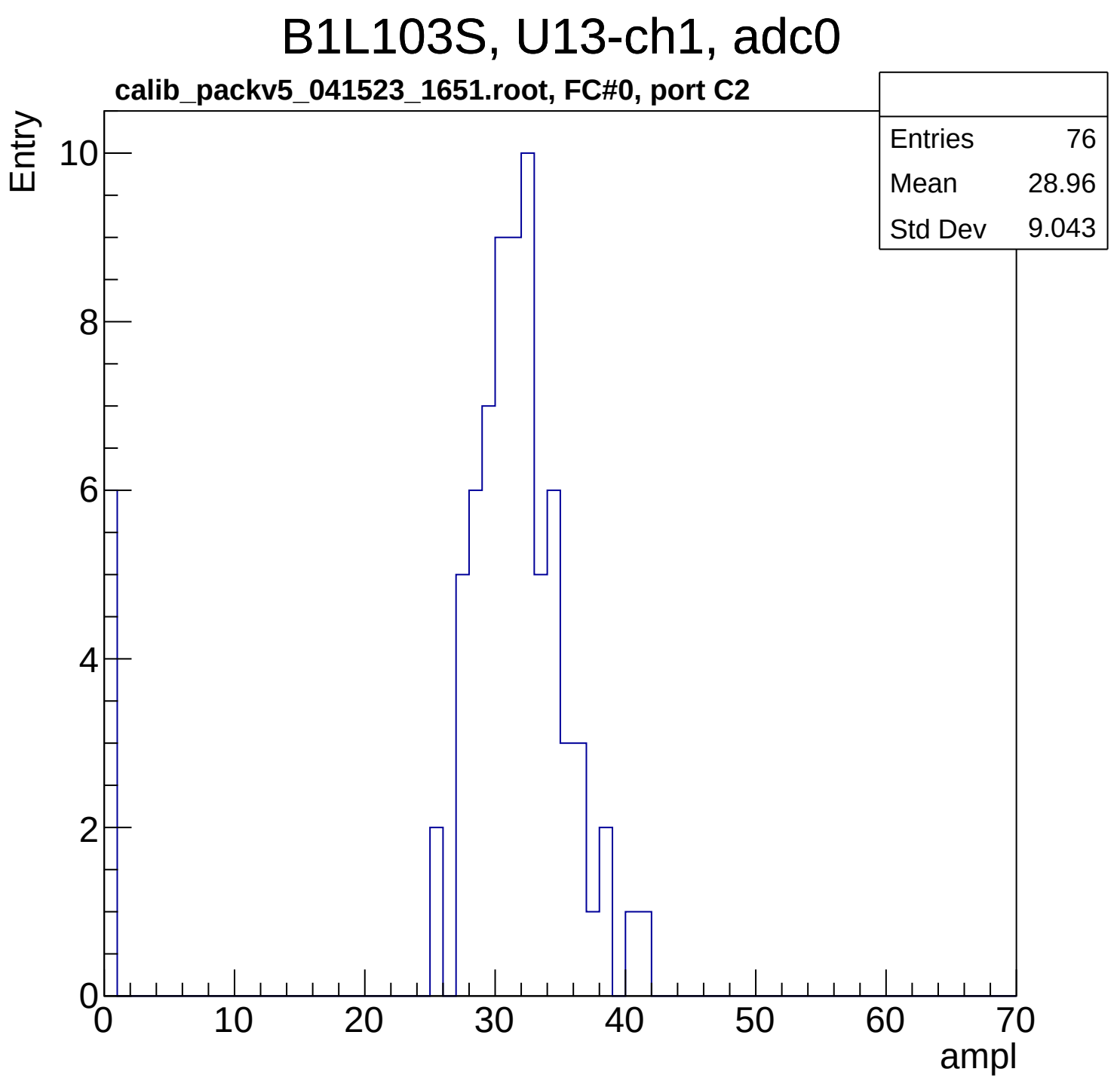
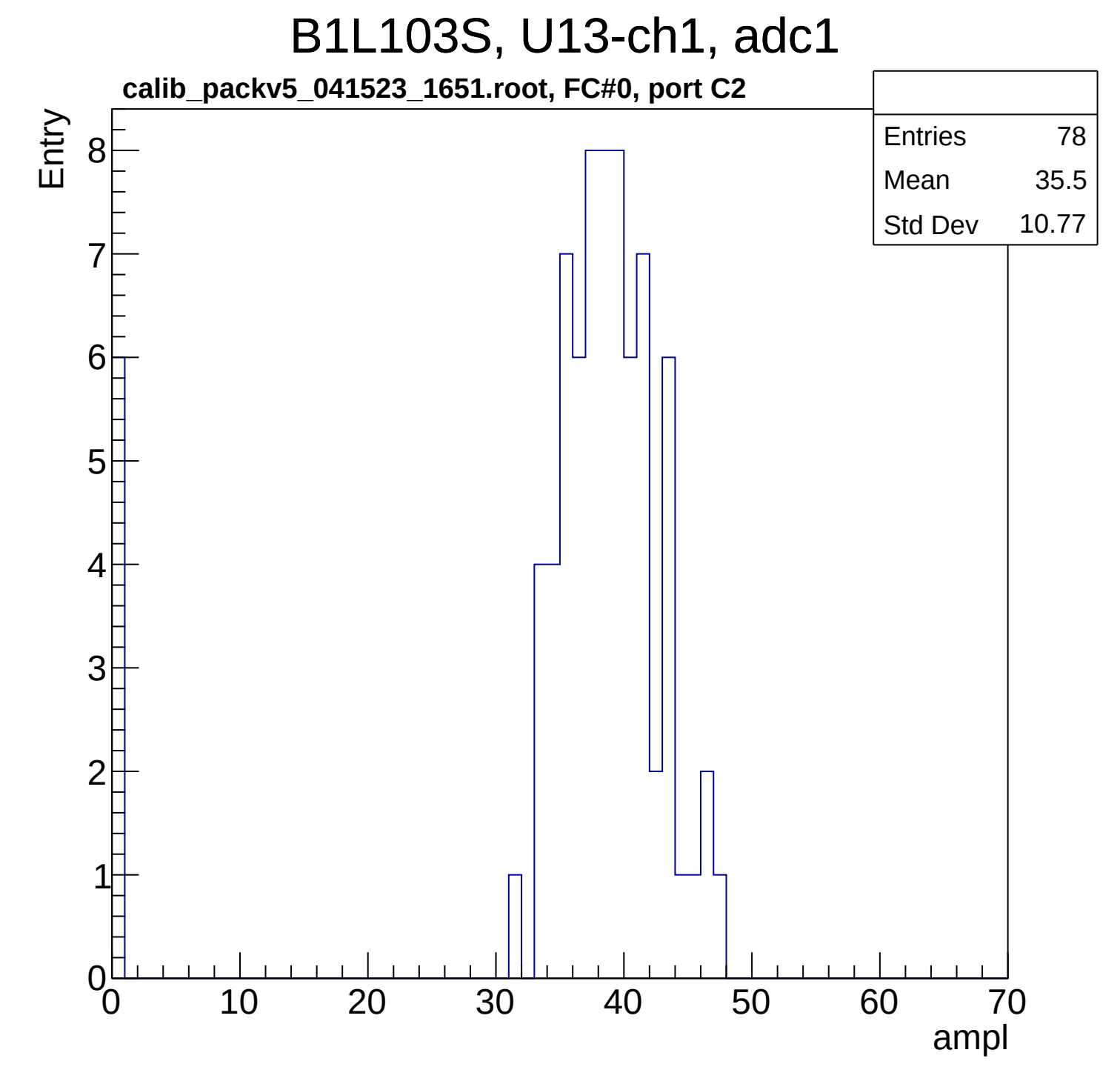
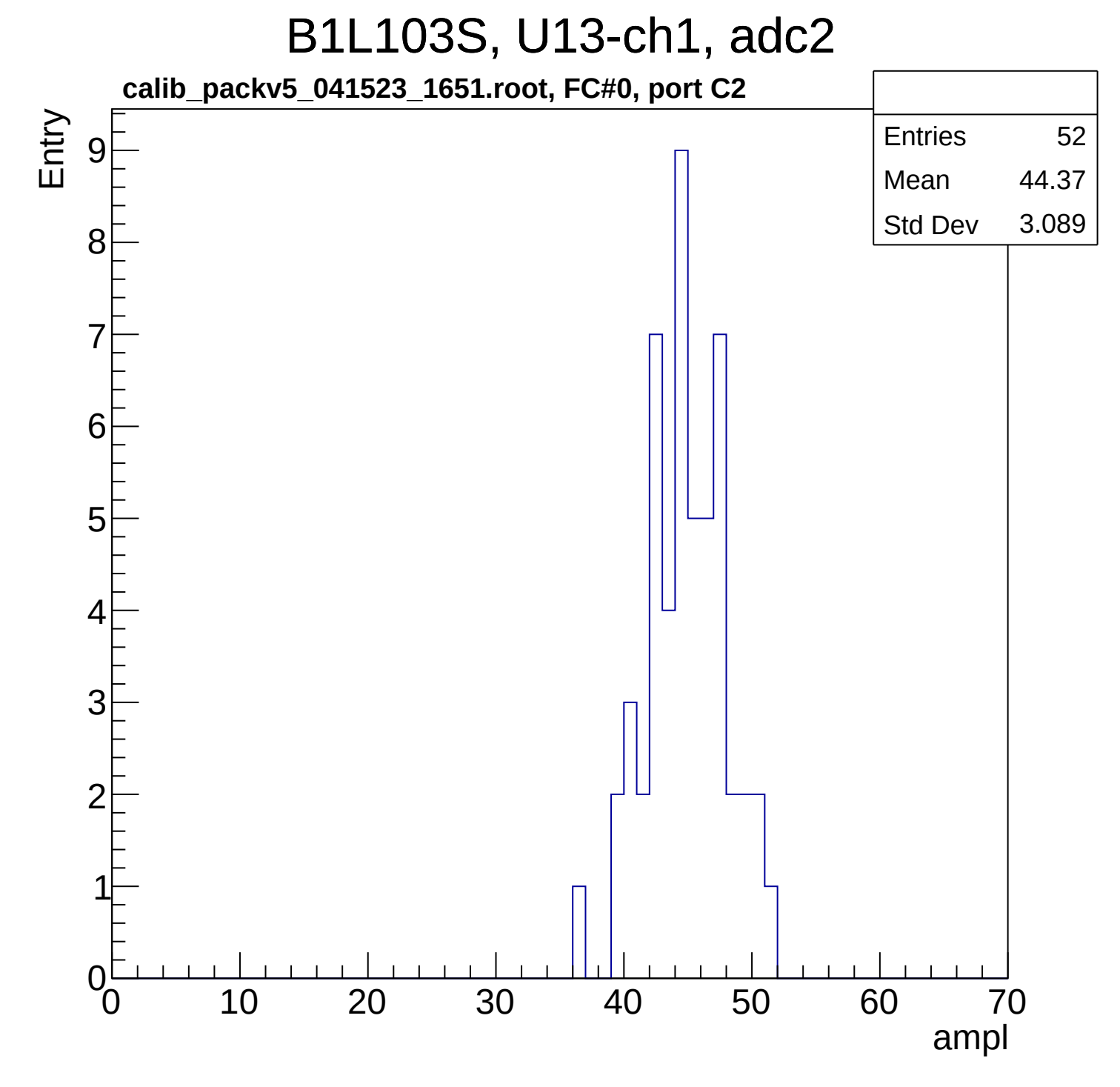
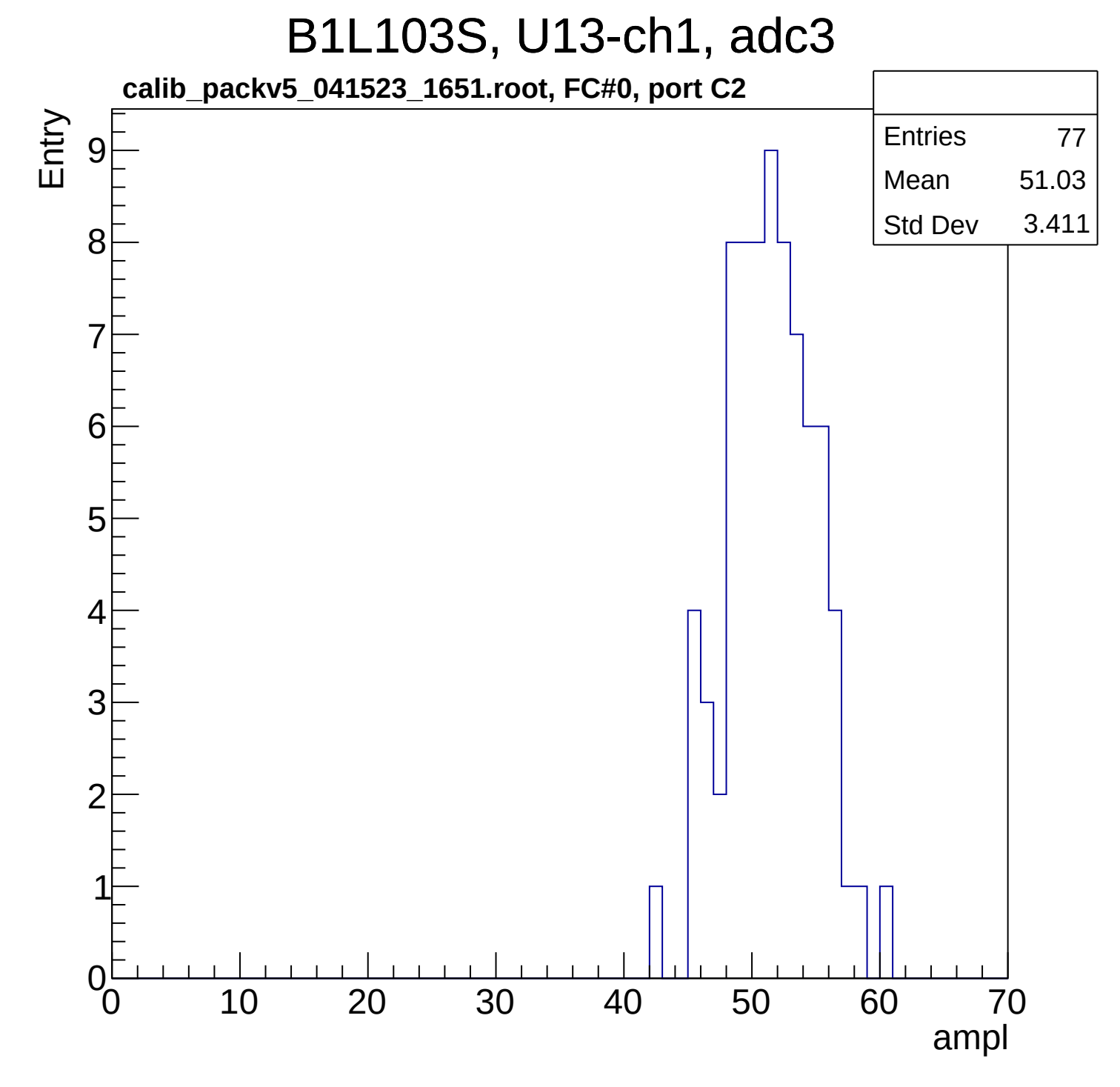
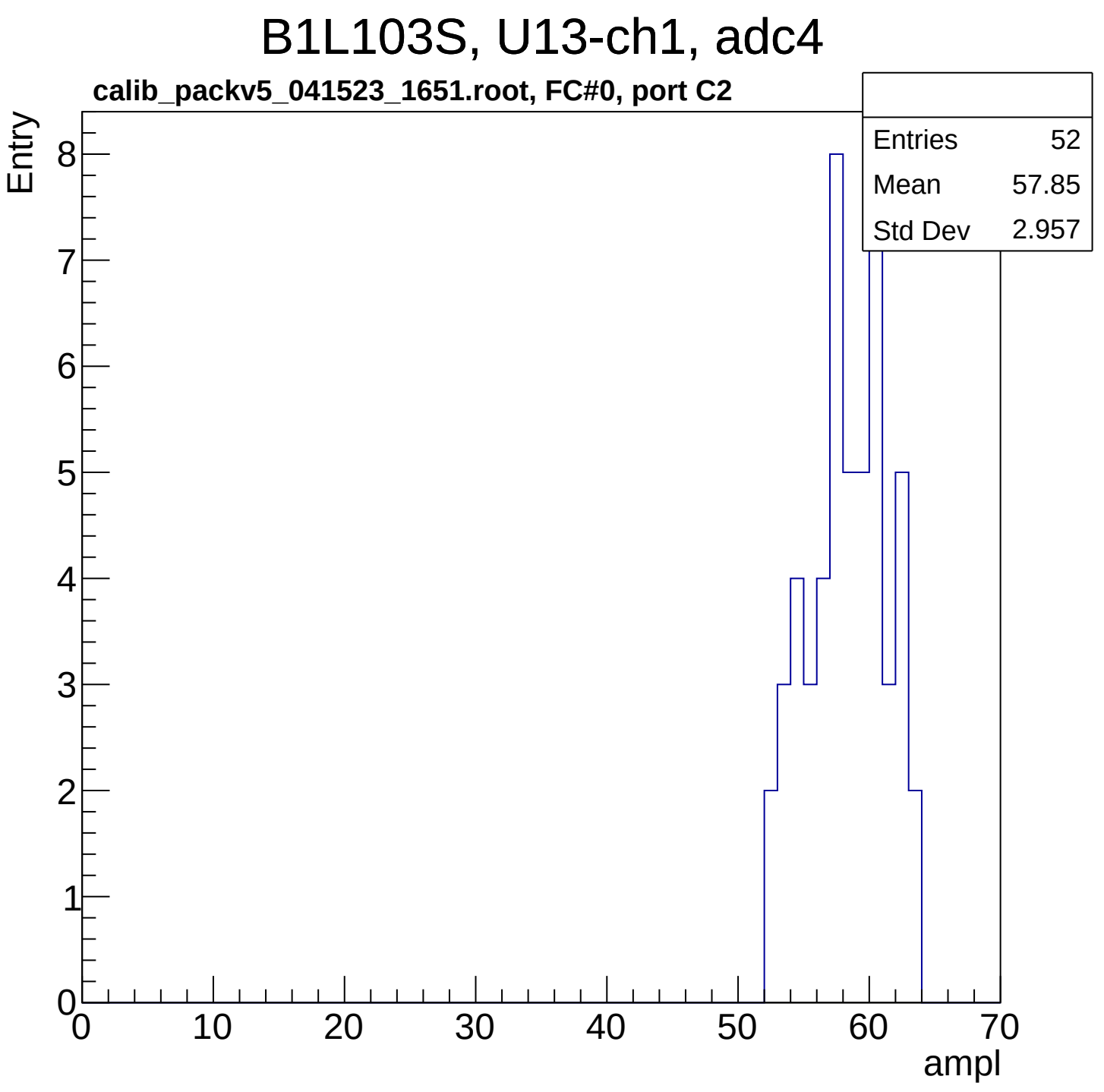
50
60
70
ampl

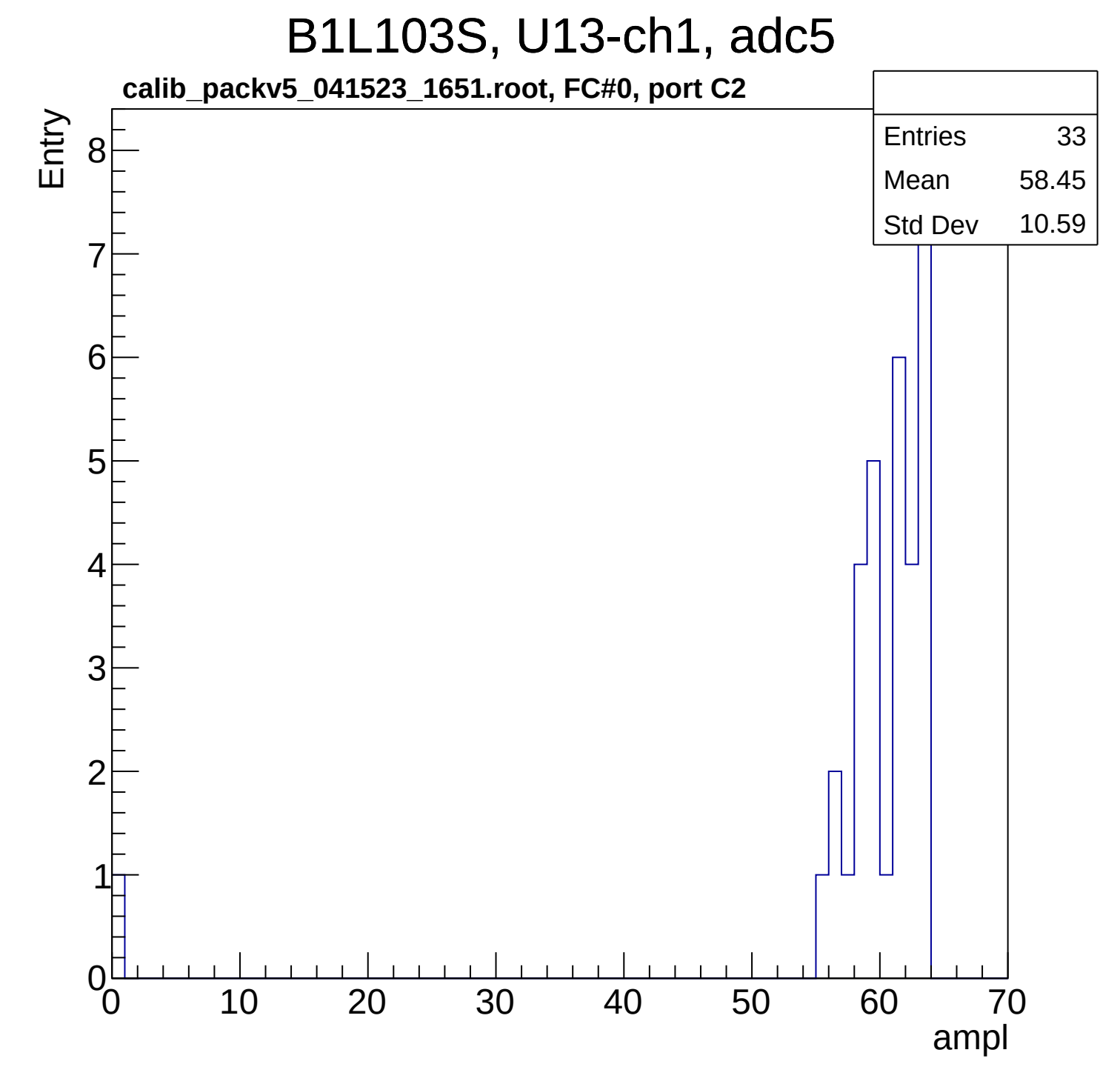

B1L103S, U13-ch1, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 28.96
Std Dev 9.043
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

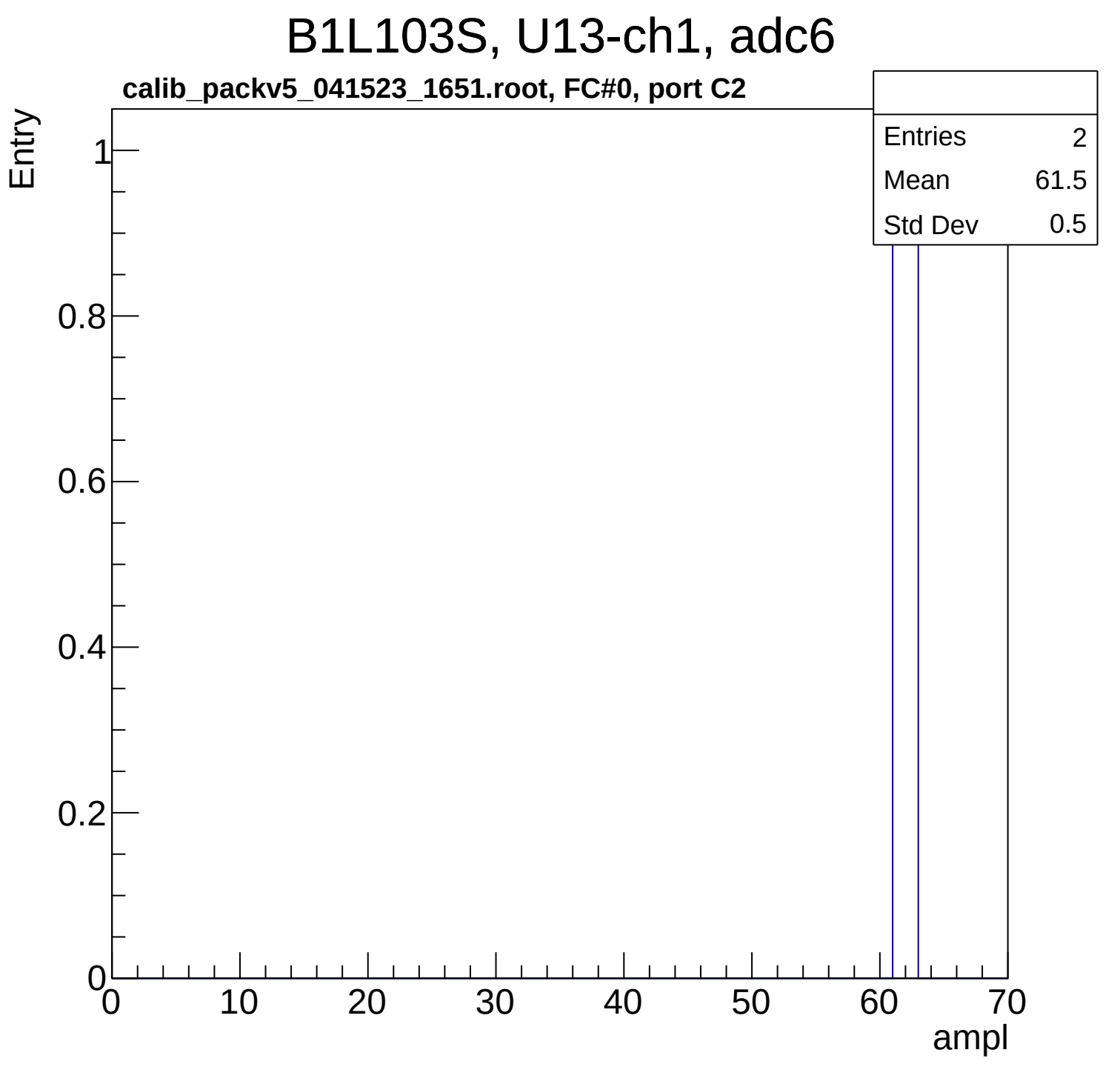

B1L103S, U13-ch1, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 35.5
Std Dev 10.77
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

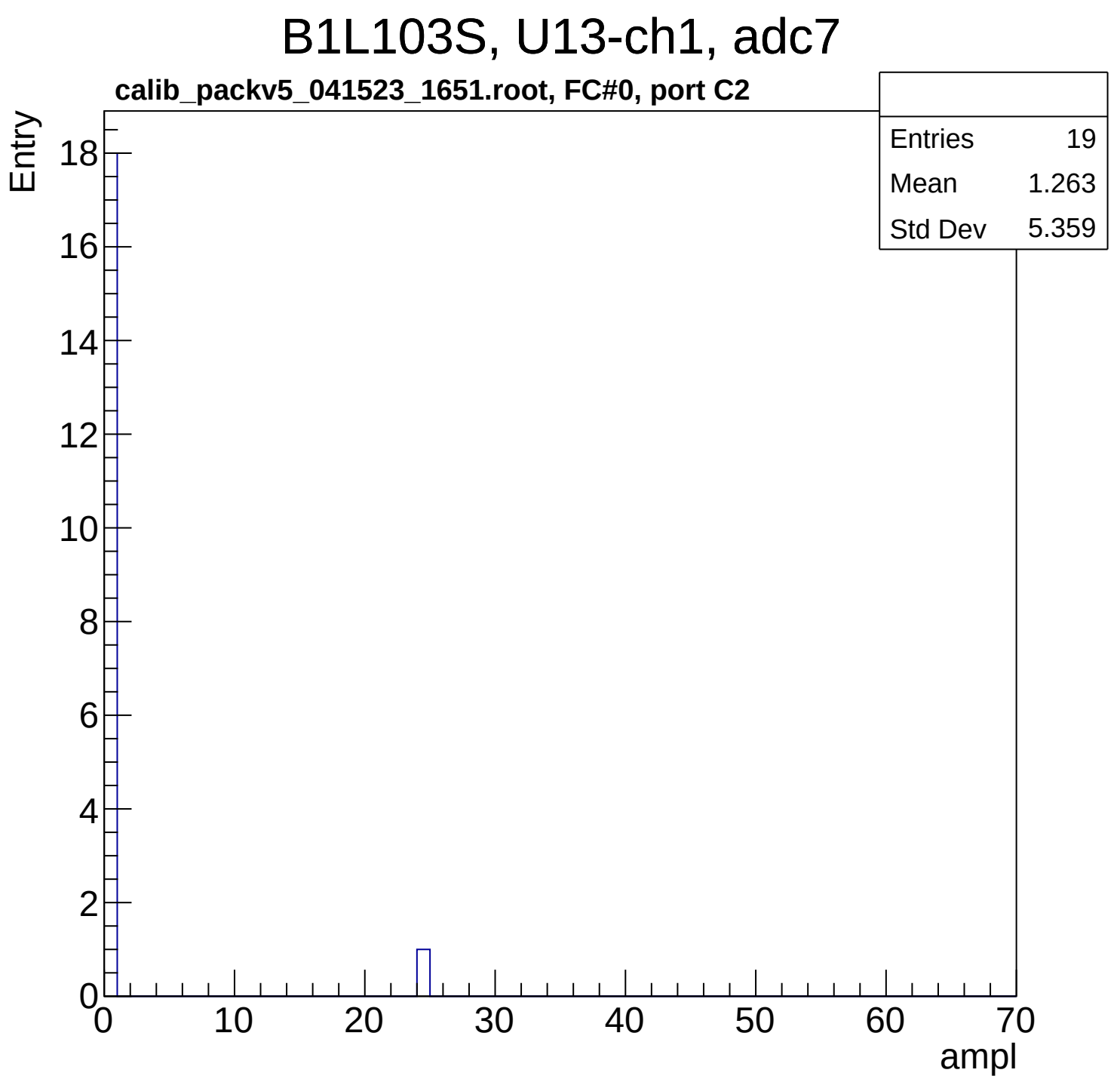

B1L103S, U13-ch1, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 44.37
Std Dev 3.089
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

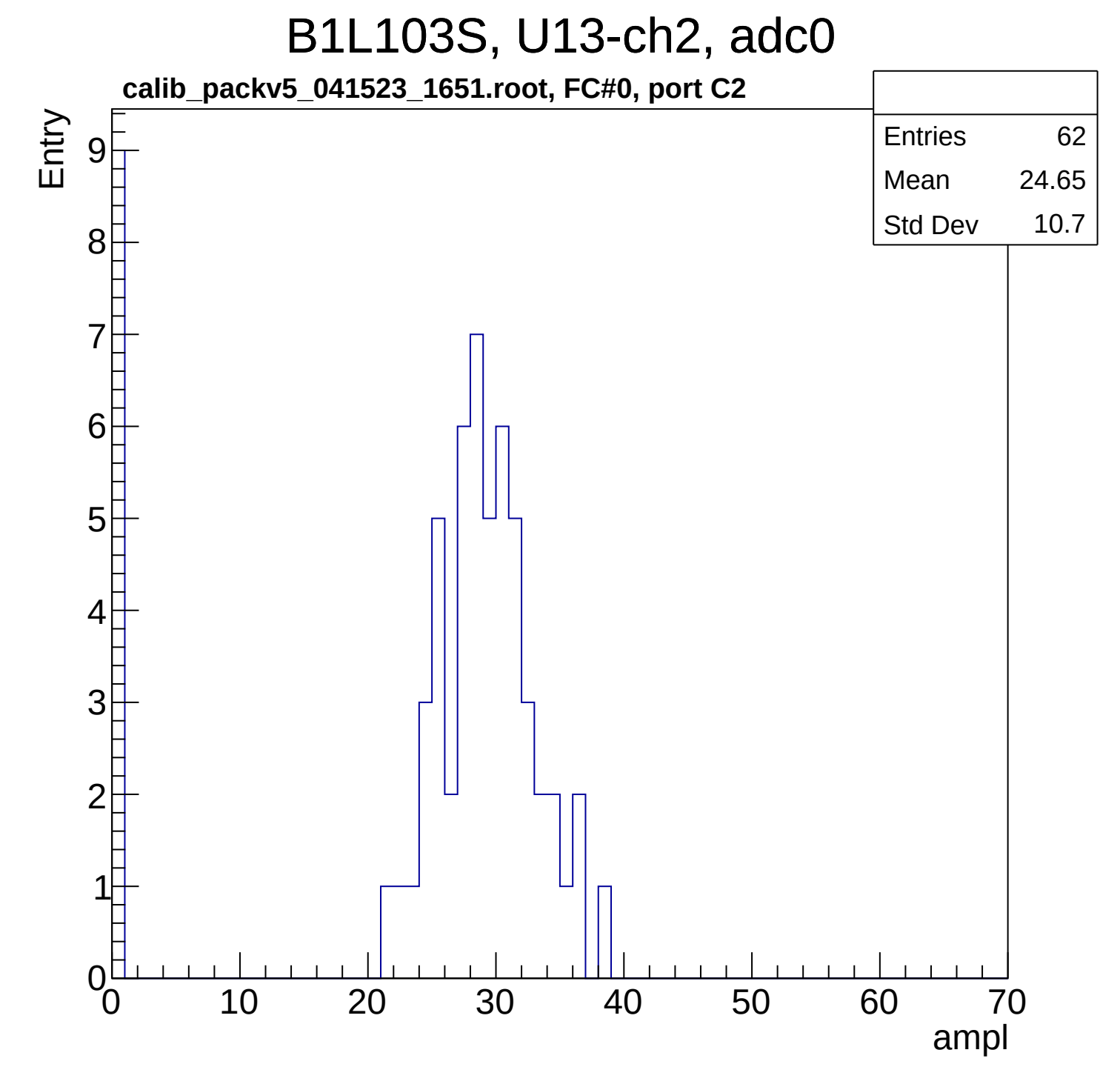

B1L103S, U13-ch1, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 51.03
Std Dev 3.411
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

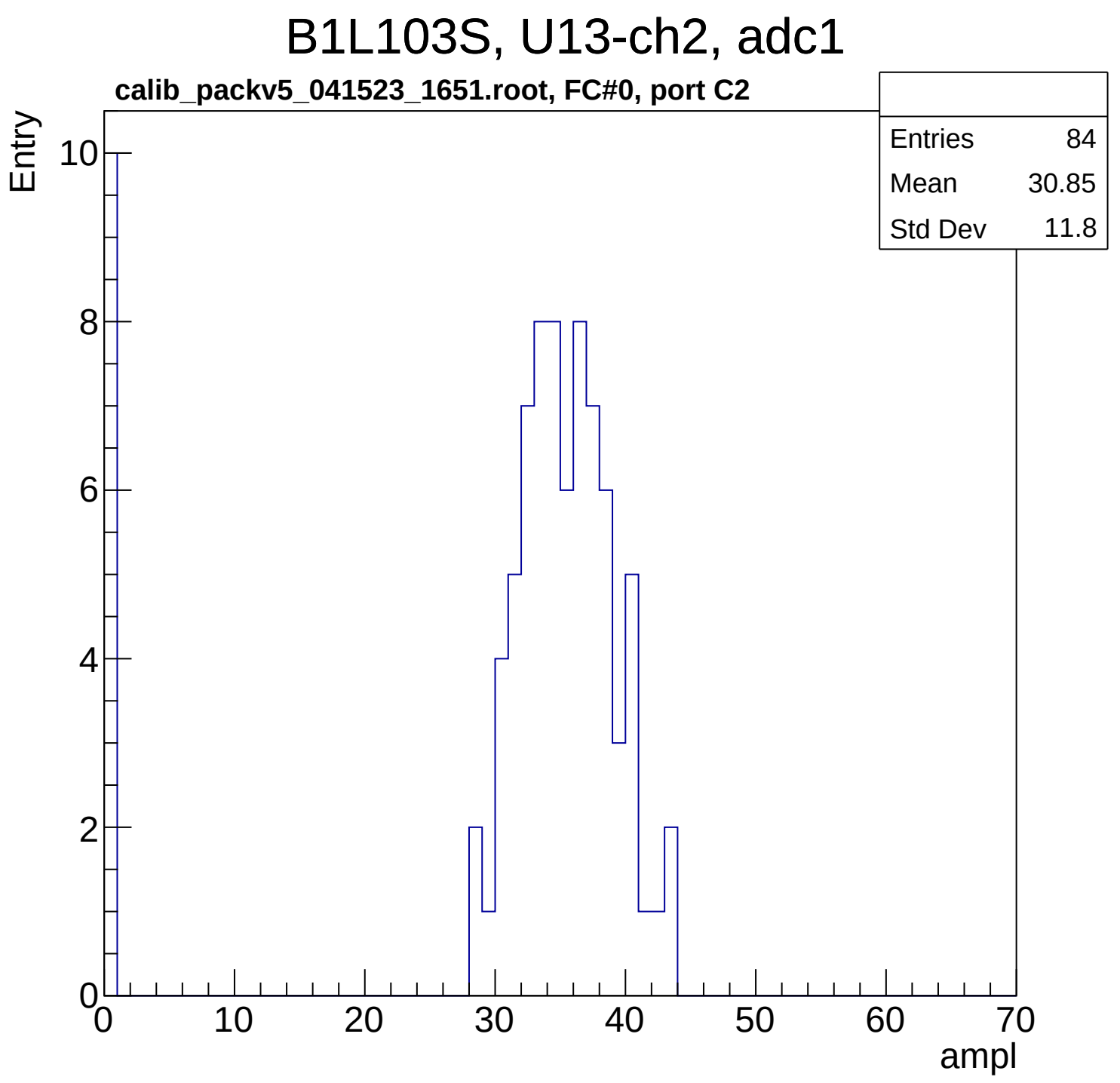

B1L103S, U13-ch1, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 57.85
Std Dev 2.957
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

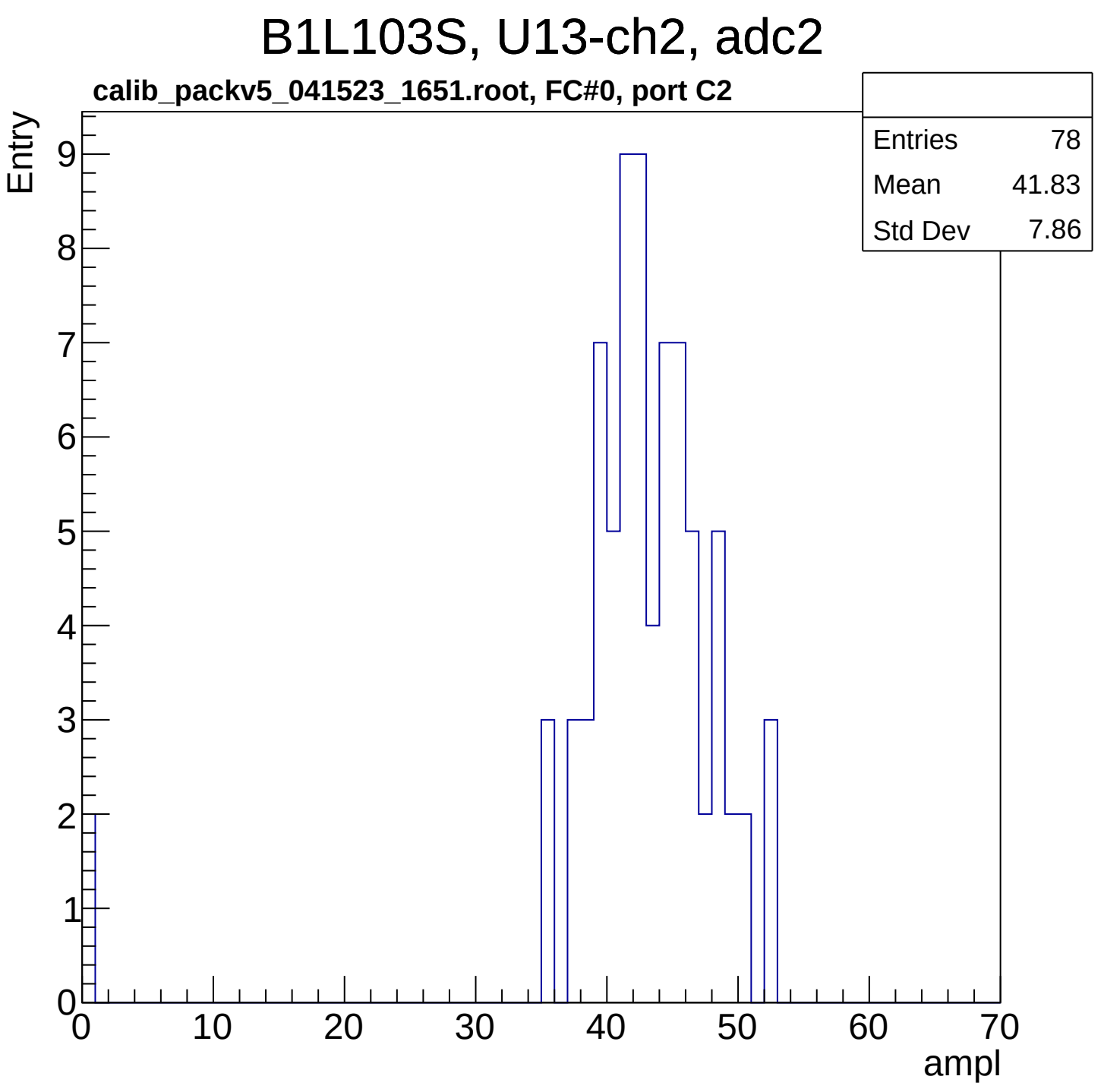

B1L103S, U13-ch1, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 58.45
Std Dev 10.59
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

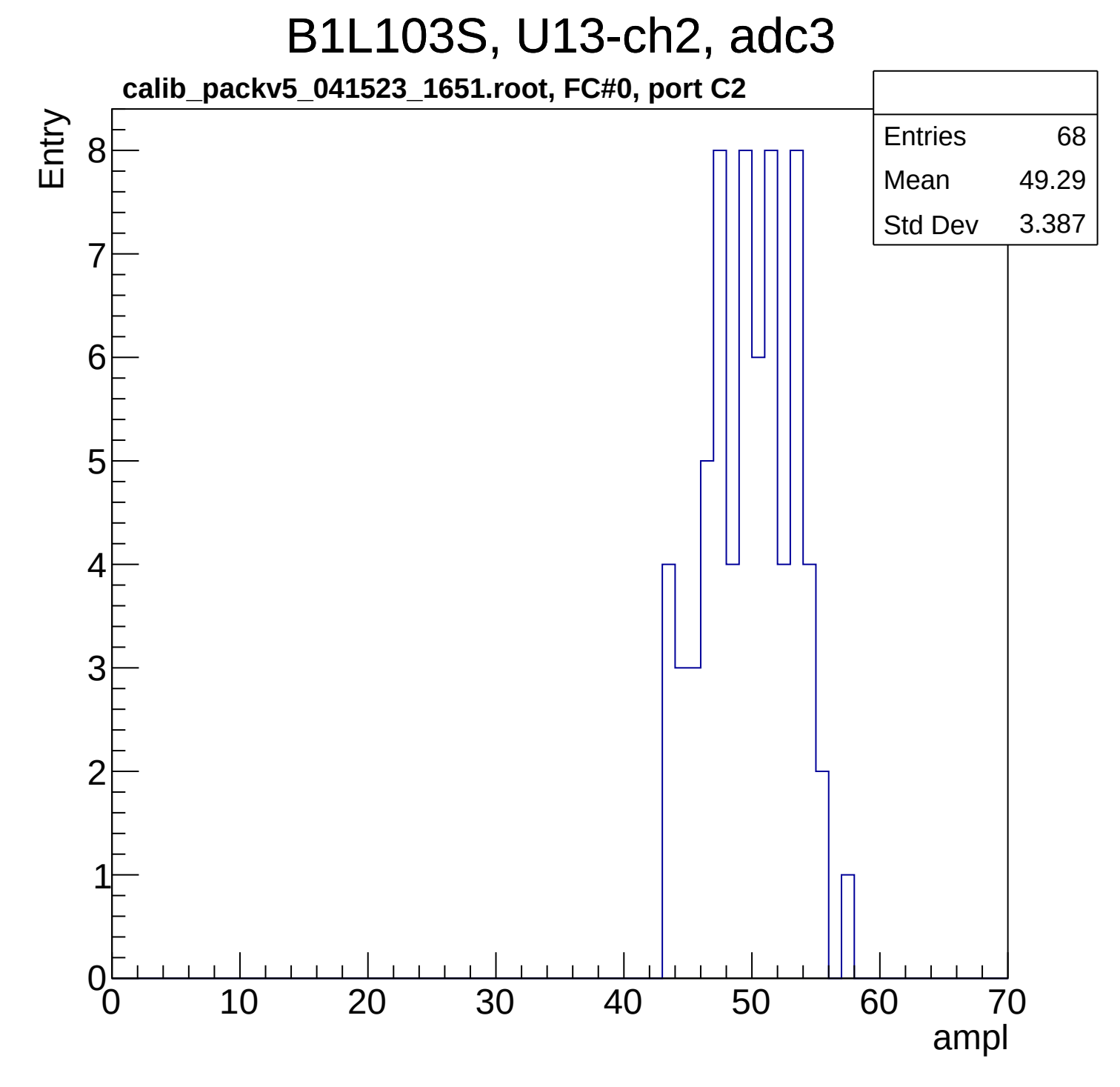

B1L103S, U13-ch1, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 61.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch1, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.263
Std Dev 5.359
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch2, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 24.65
Std Dev 10.7
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch2, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 30.85
Std Dev 11.8
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch2, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 41.83
Std Dev 7.86
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch2, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 49.29
Std Dev 3.387
Entry
ampl
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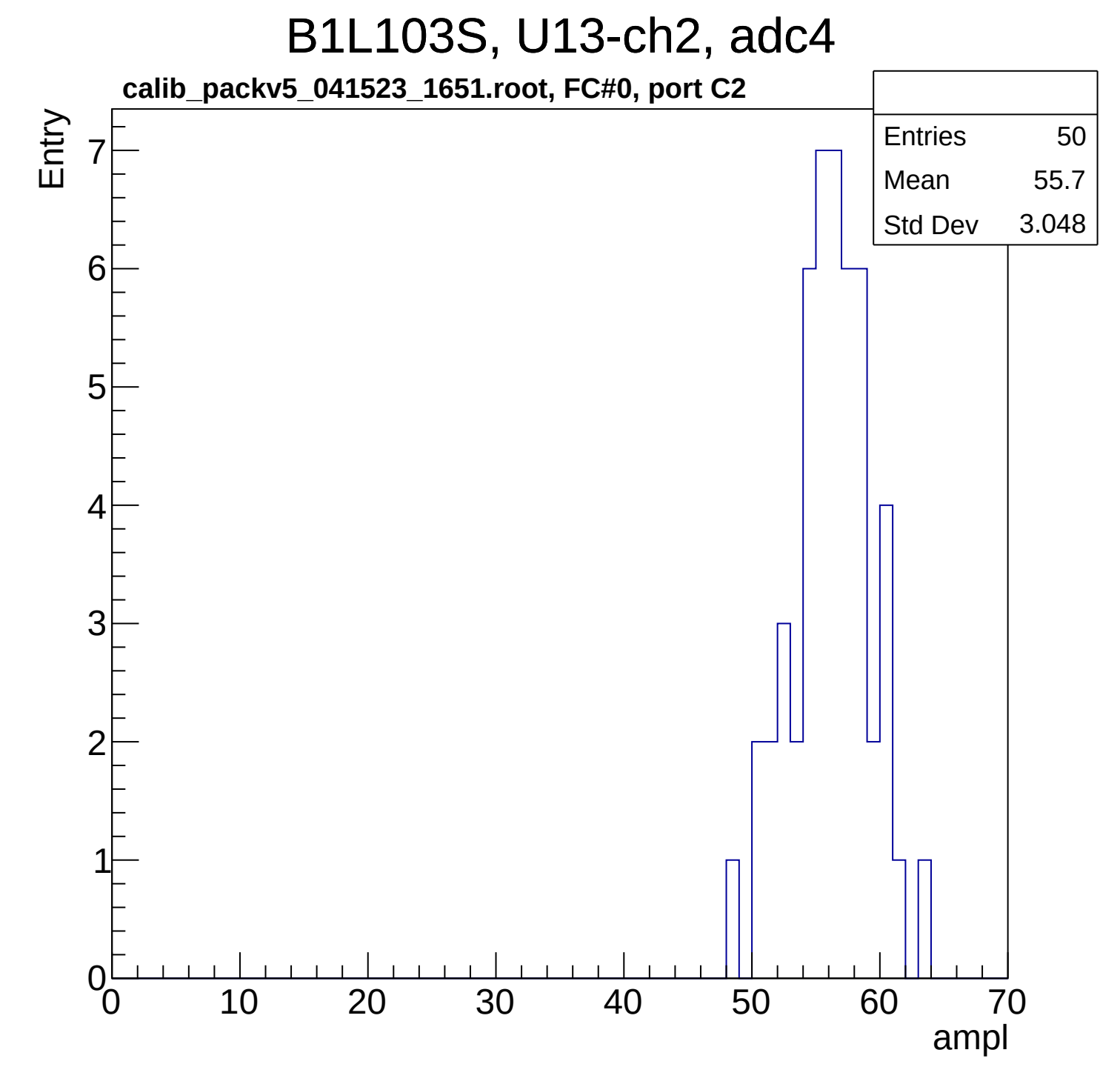
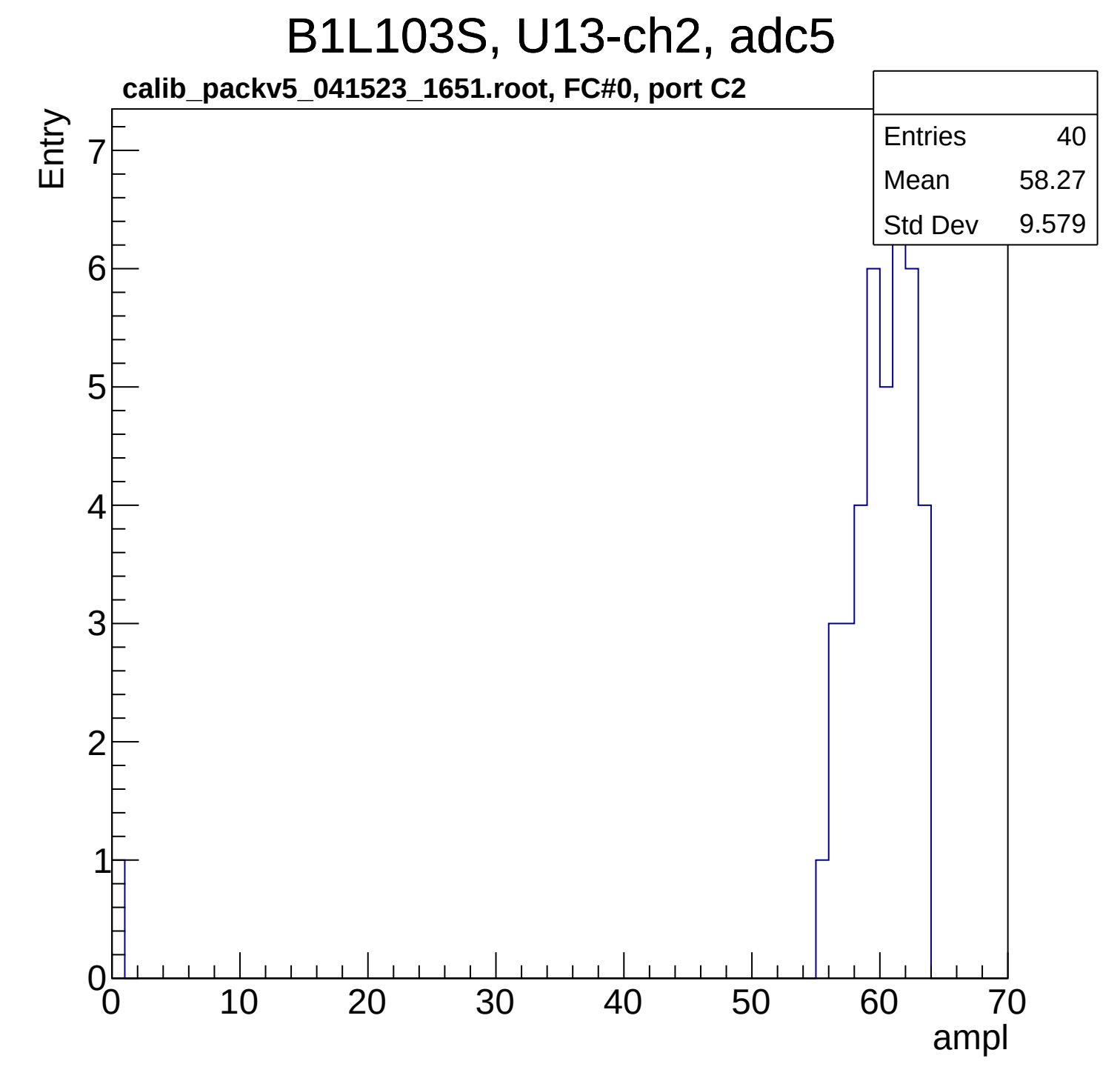
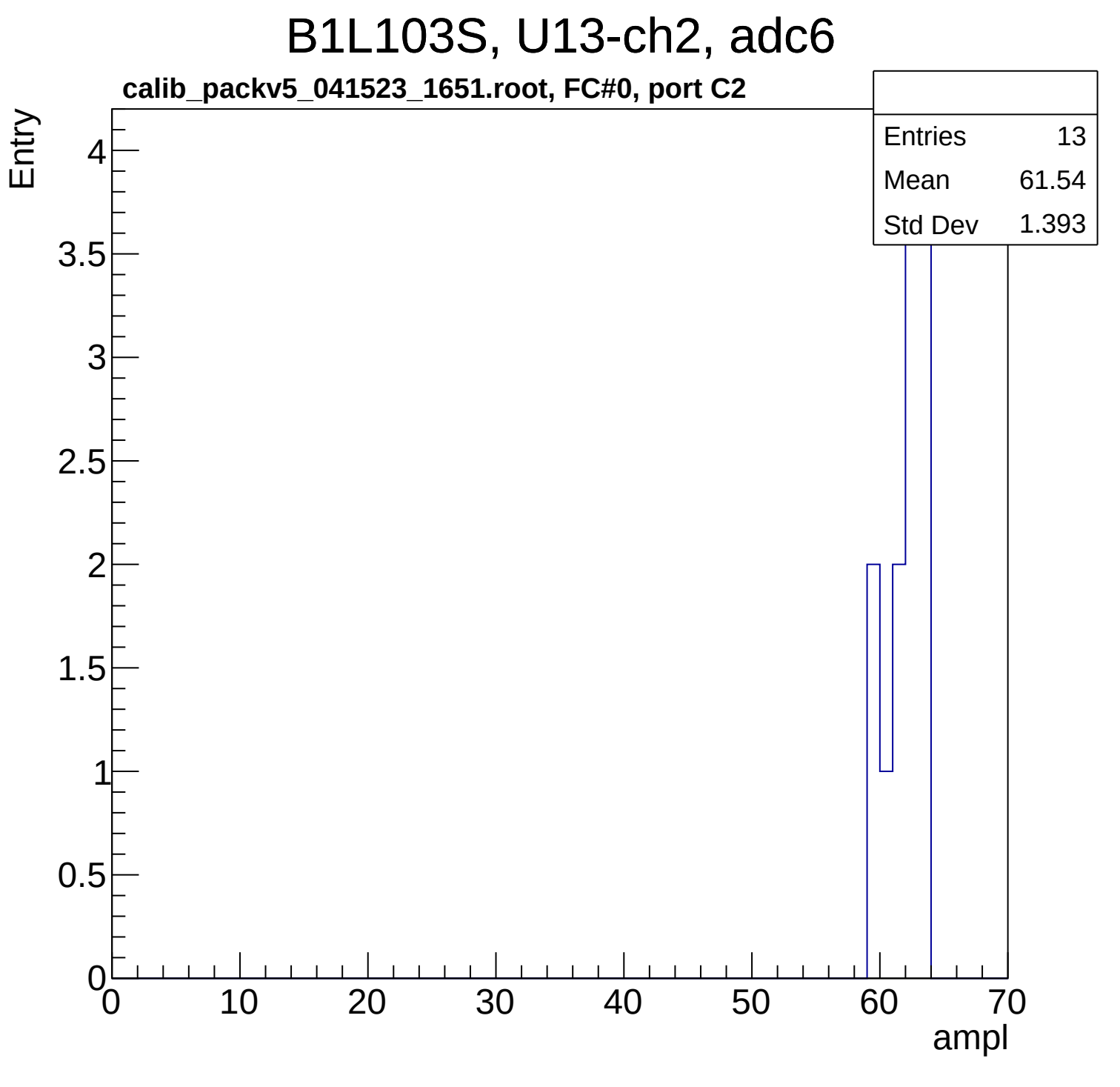
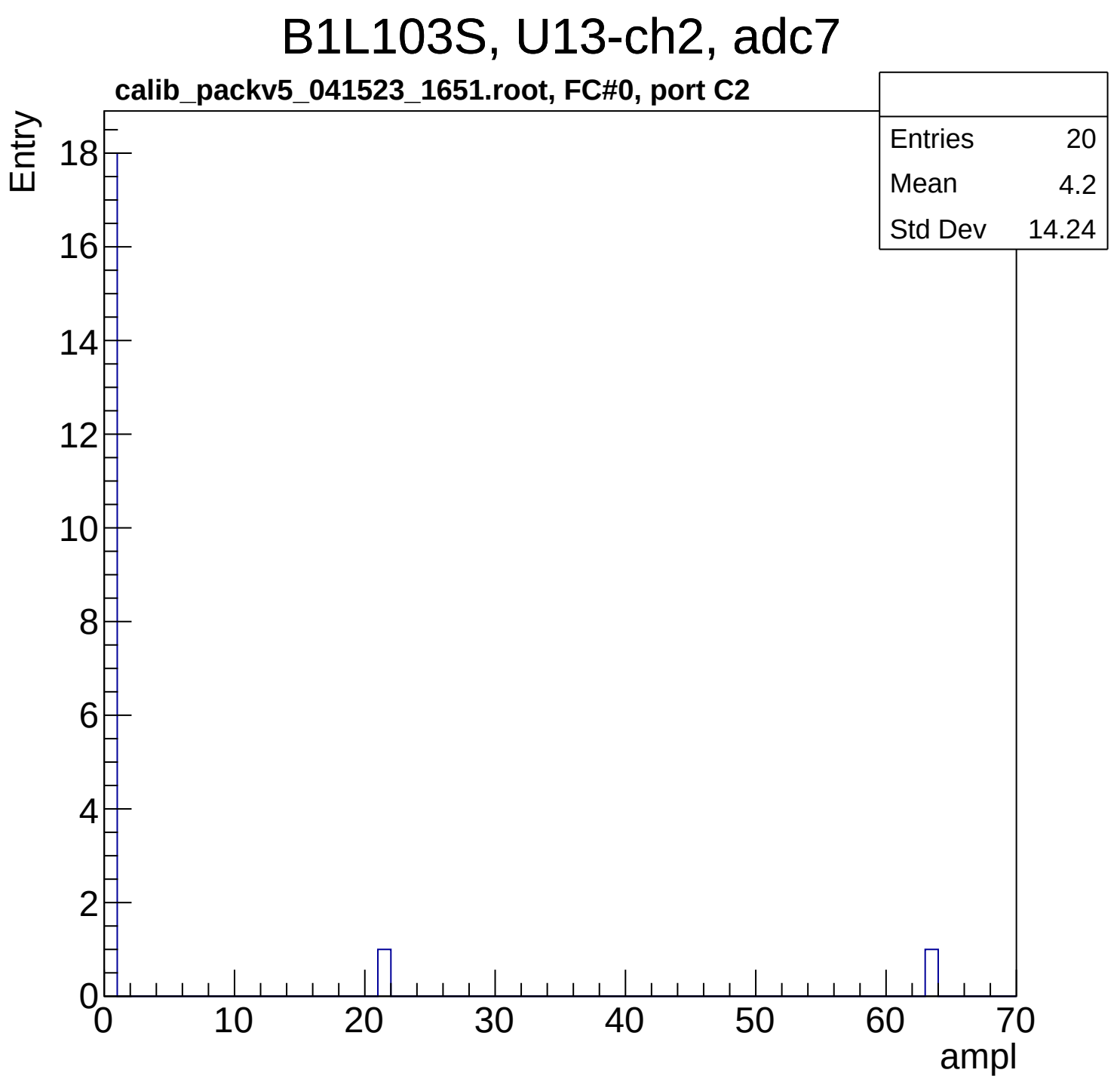
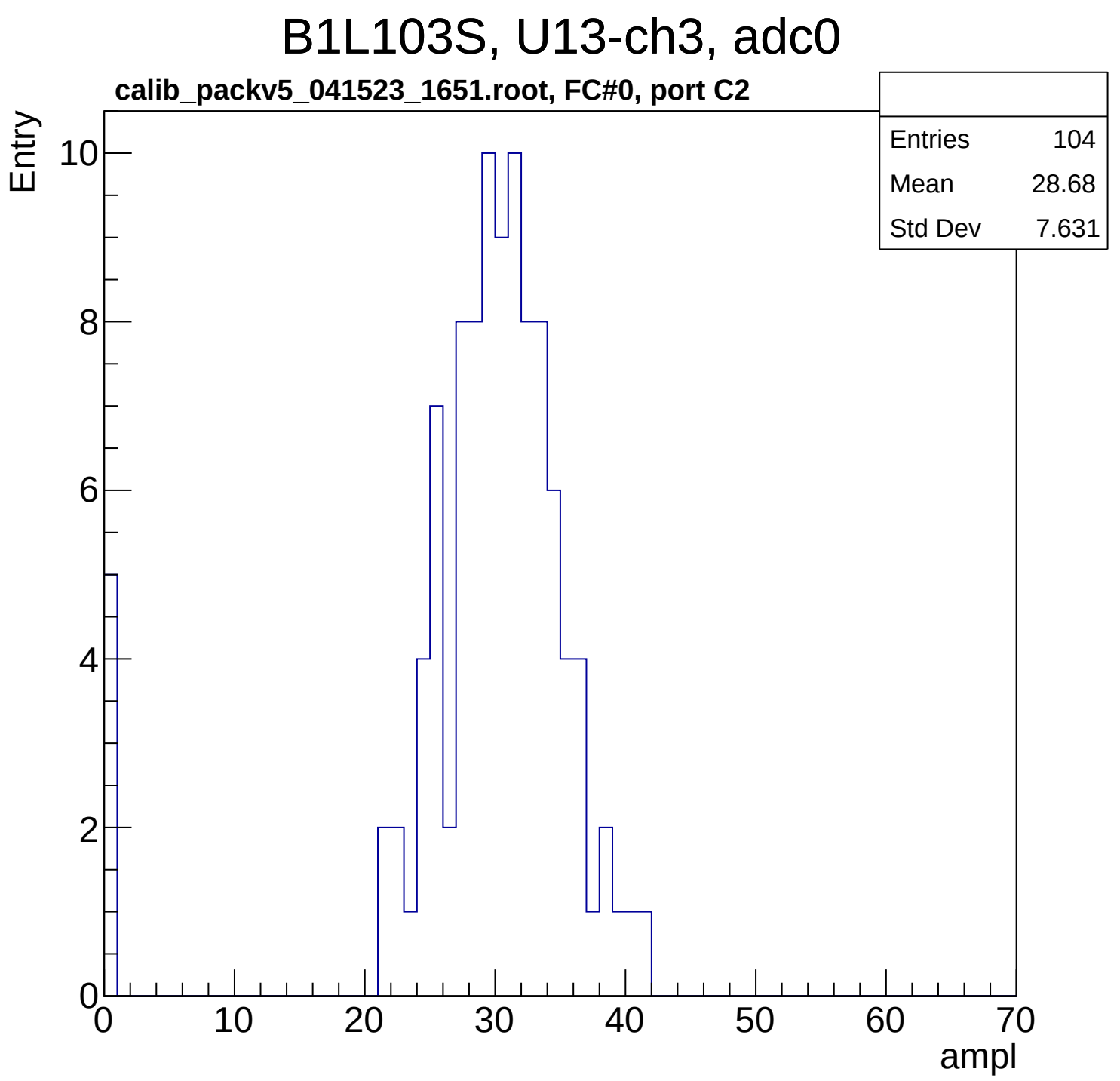
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

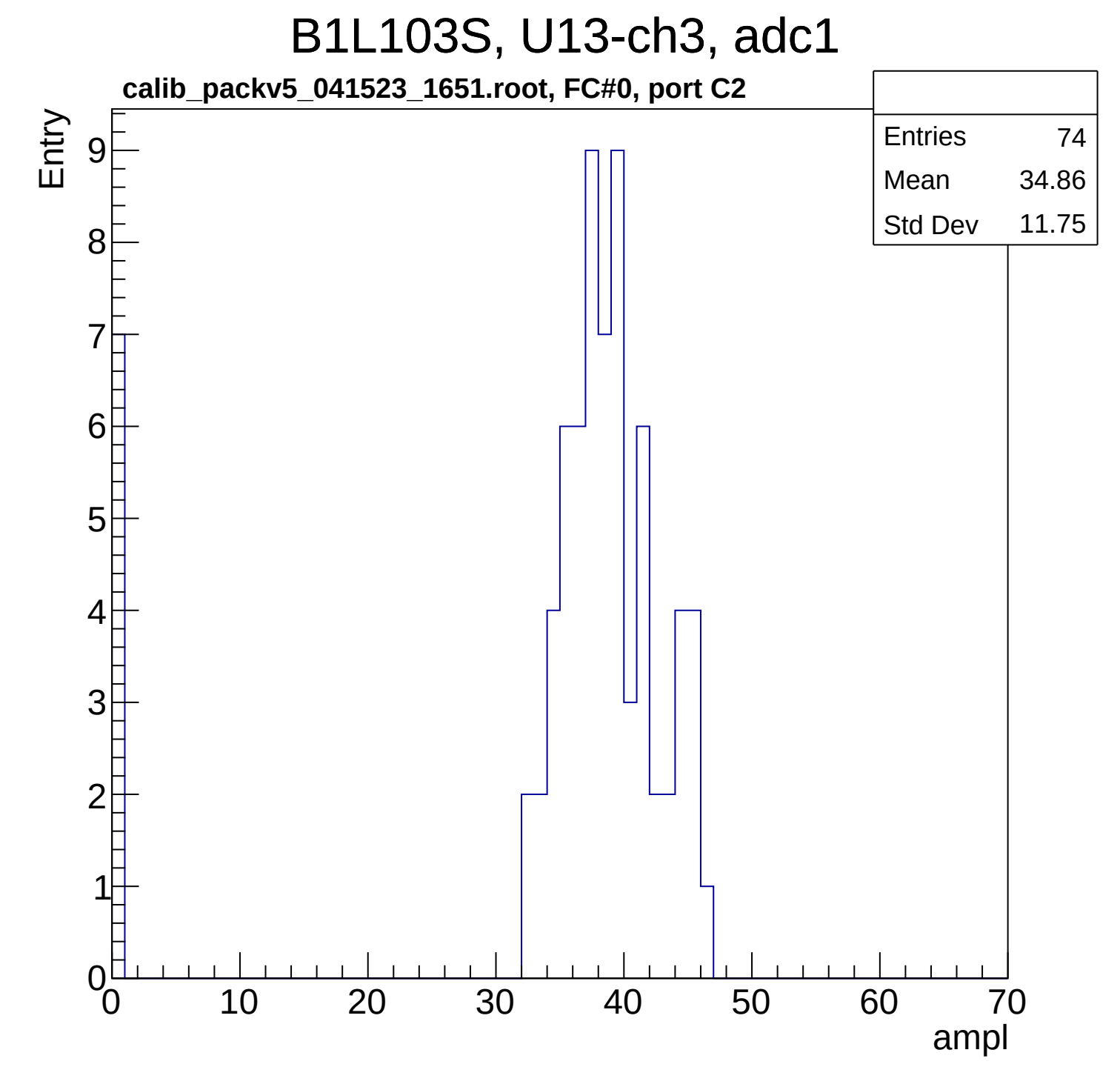

B1L103S, U13-ch2, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 55.7
Std Dev 3.048
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

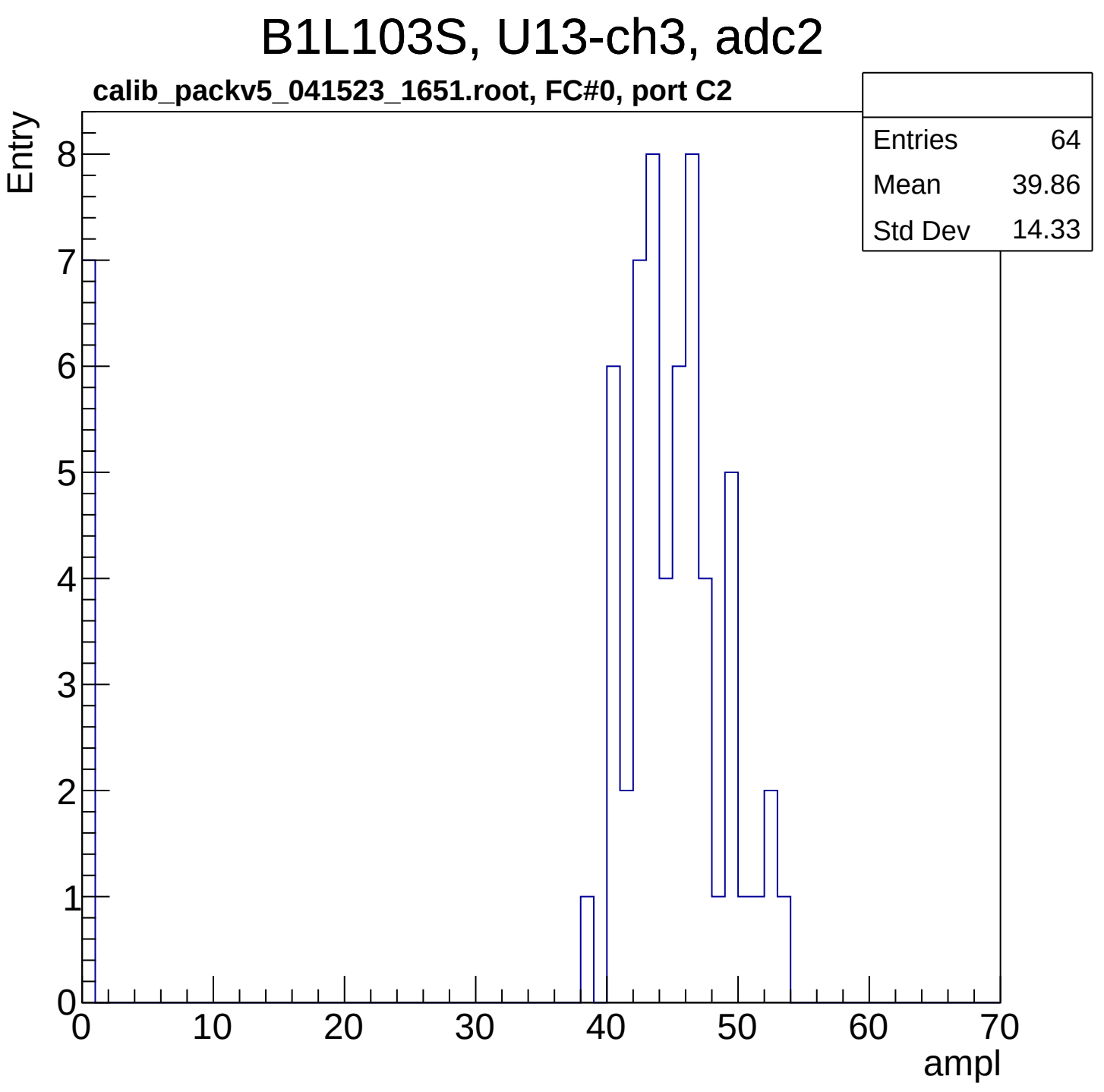

B1L103S, U13-ch2, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 58.27
Std Dev 9.579
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

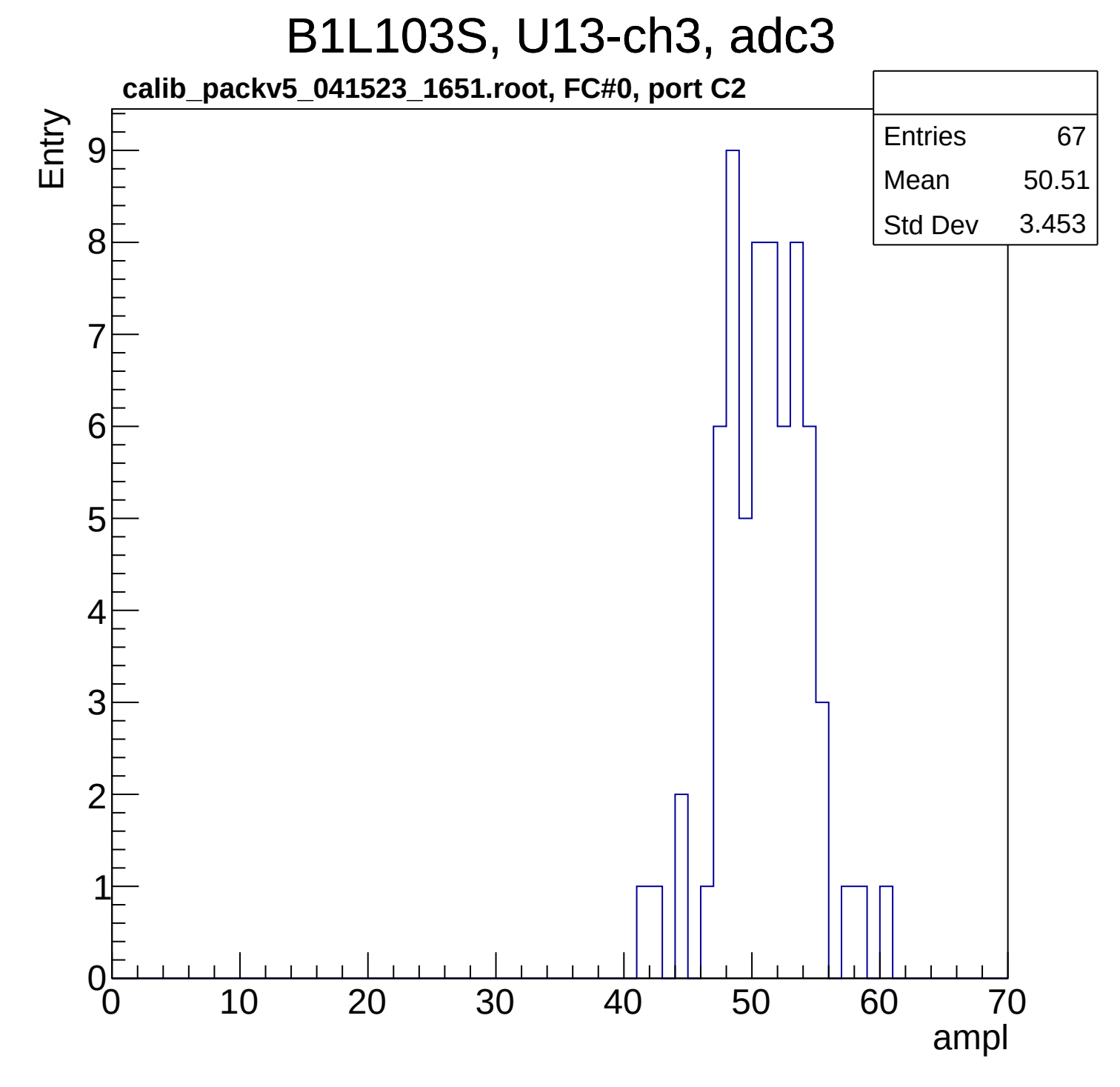

B1L103S, U13-ch2, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.54
Std Dev 1.393
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

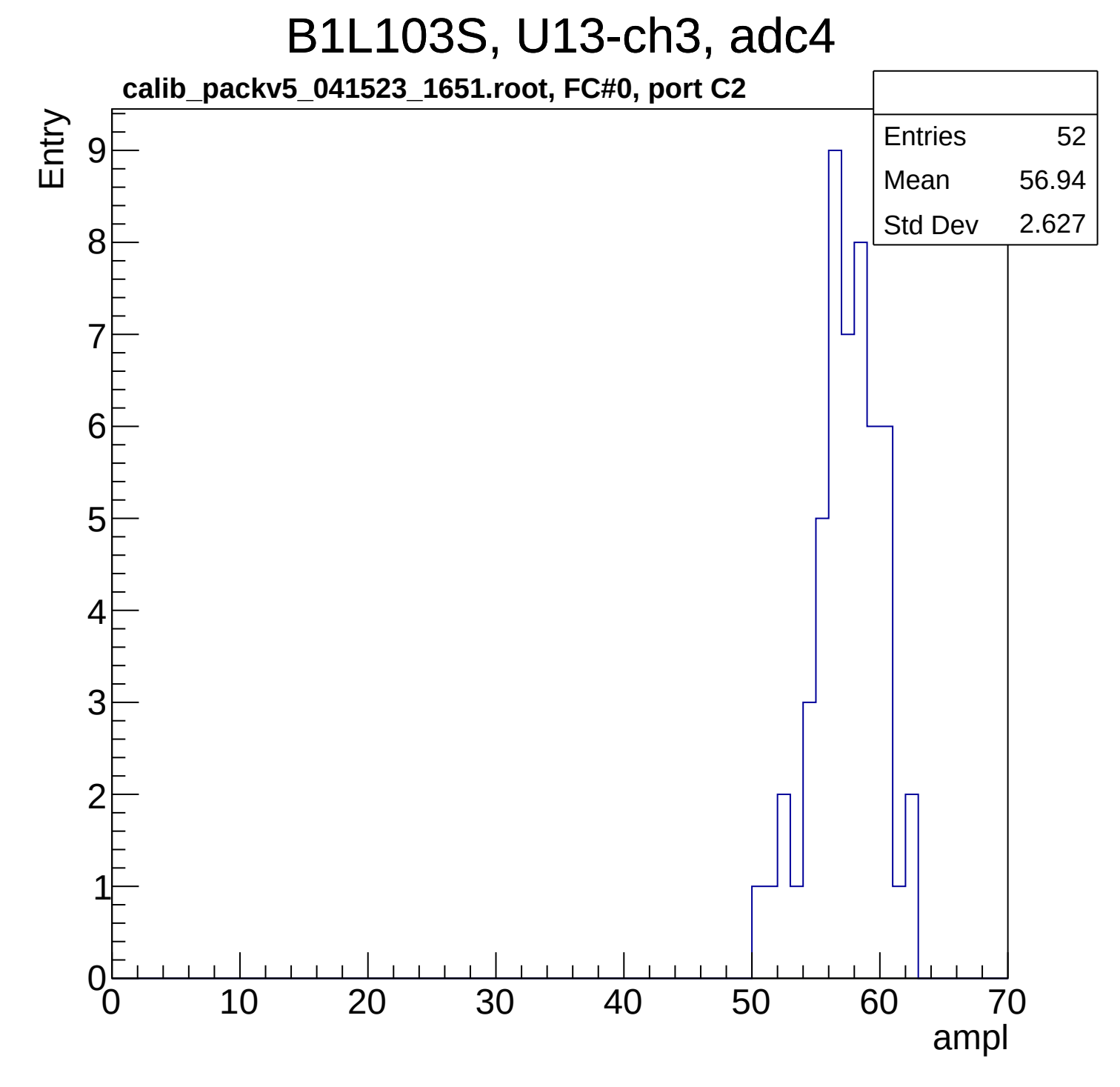

B1L103S, U13-ch2, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.2
Std Dev 14.24
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

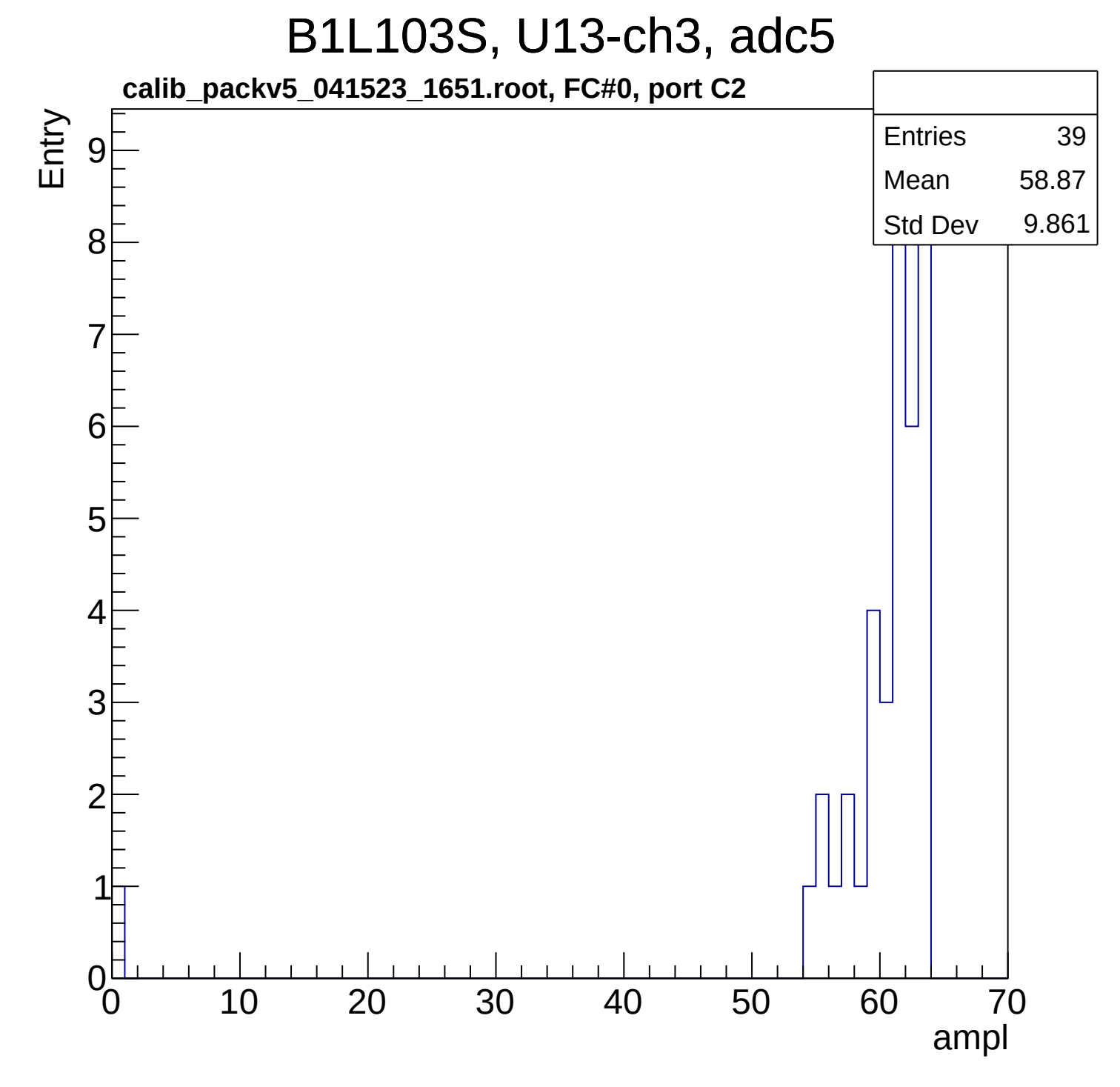

B1L103S, U13-ch3, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 28.68
Std Dev 7.631
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch3, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 34.86
Std Dev 11.75
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch3, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 39.86
Std Dev 14.33
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch3, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 50.51
Std Dev 3.453
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch3, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 56.94
Std Dev 2.627
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch3, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 58.87
Std Dev 9.861
Entry
ampl
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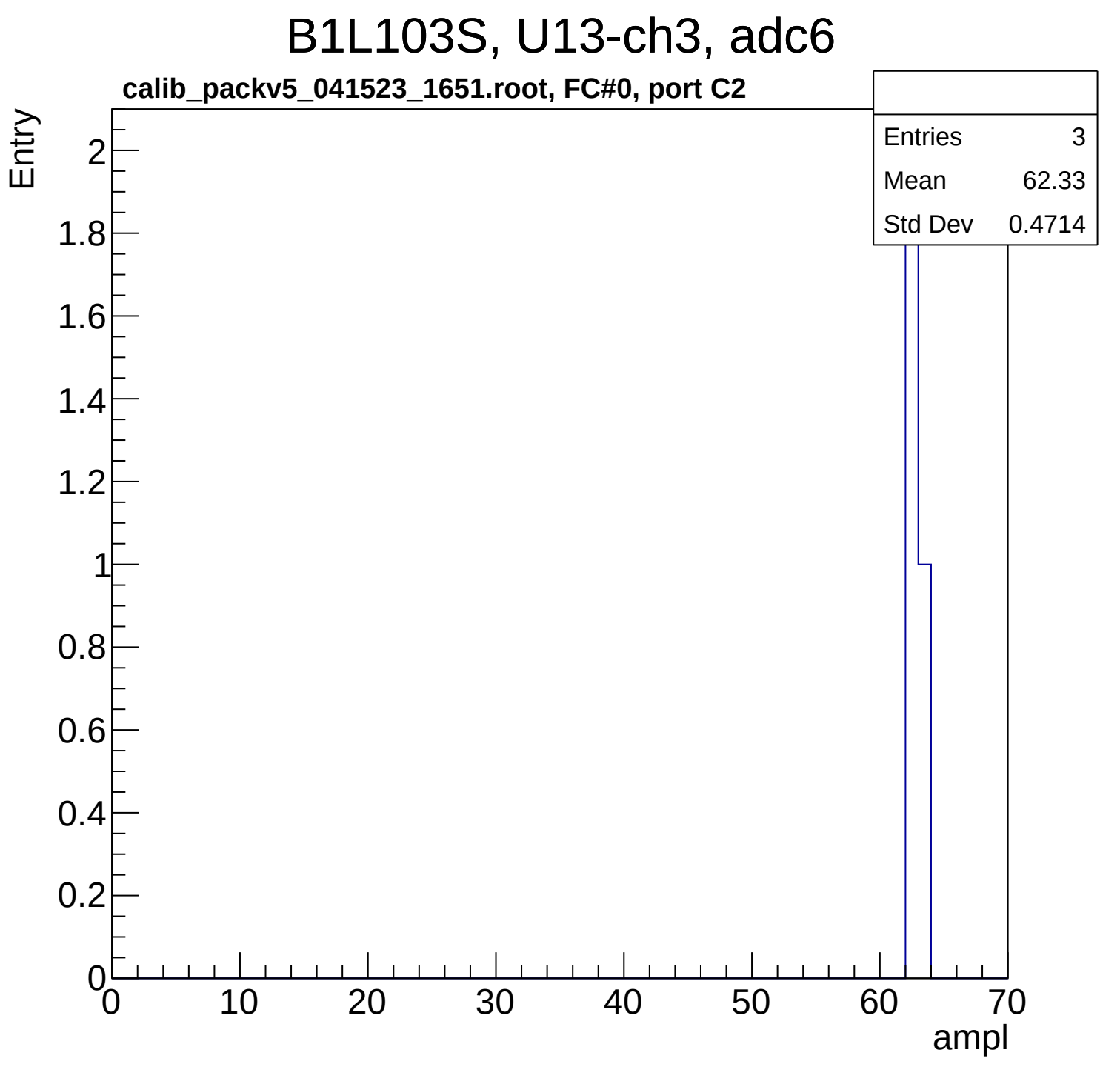
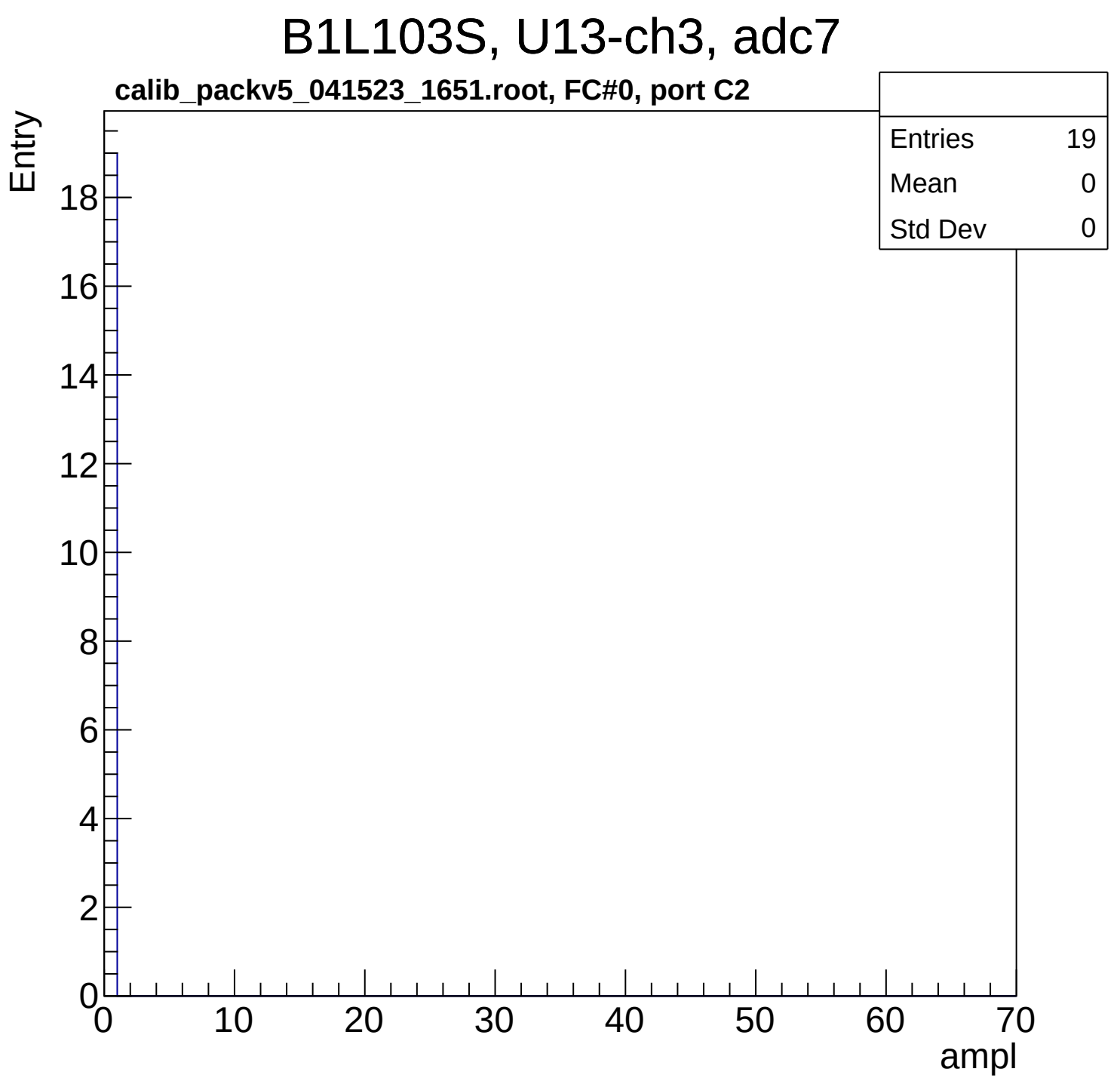
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch3, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U13-ch3, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
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6
8
10
12
14
16
18
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10
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50
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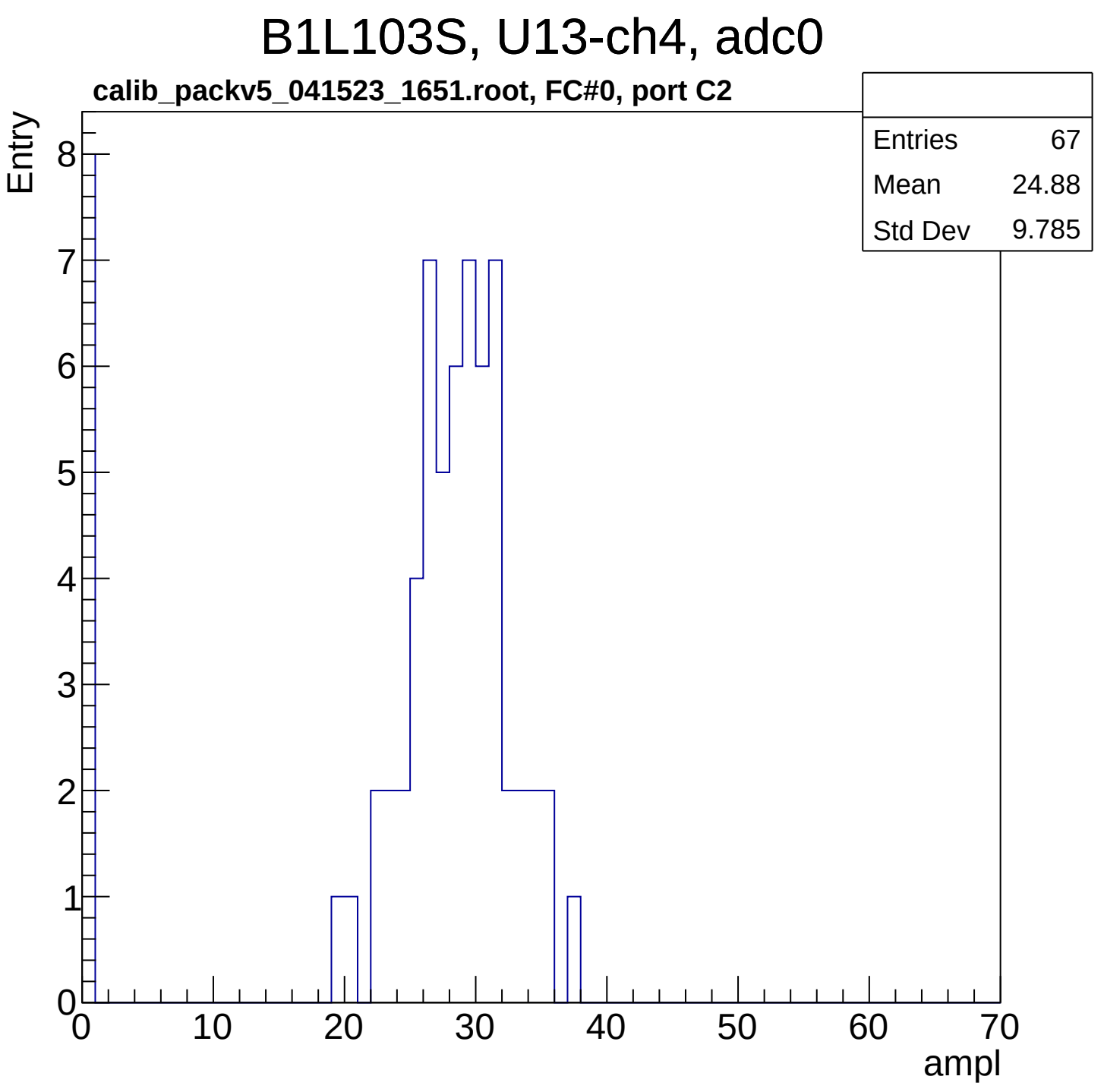
70
ampl


B1L103S, U13-ch4, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 24.88
Std Dev 9.785
Entry
ampl
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2
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7
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0
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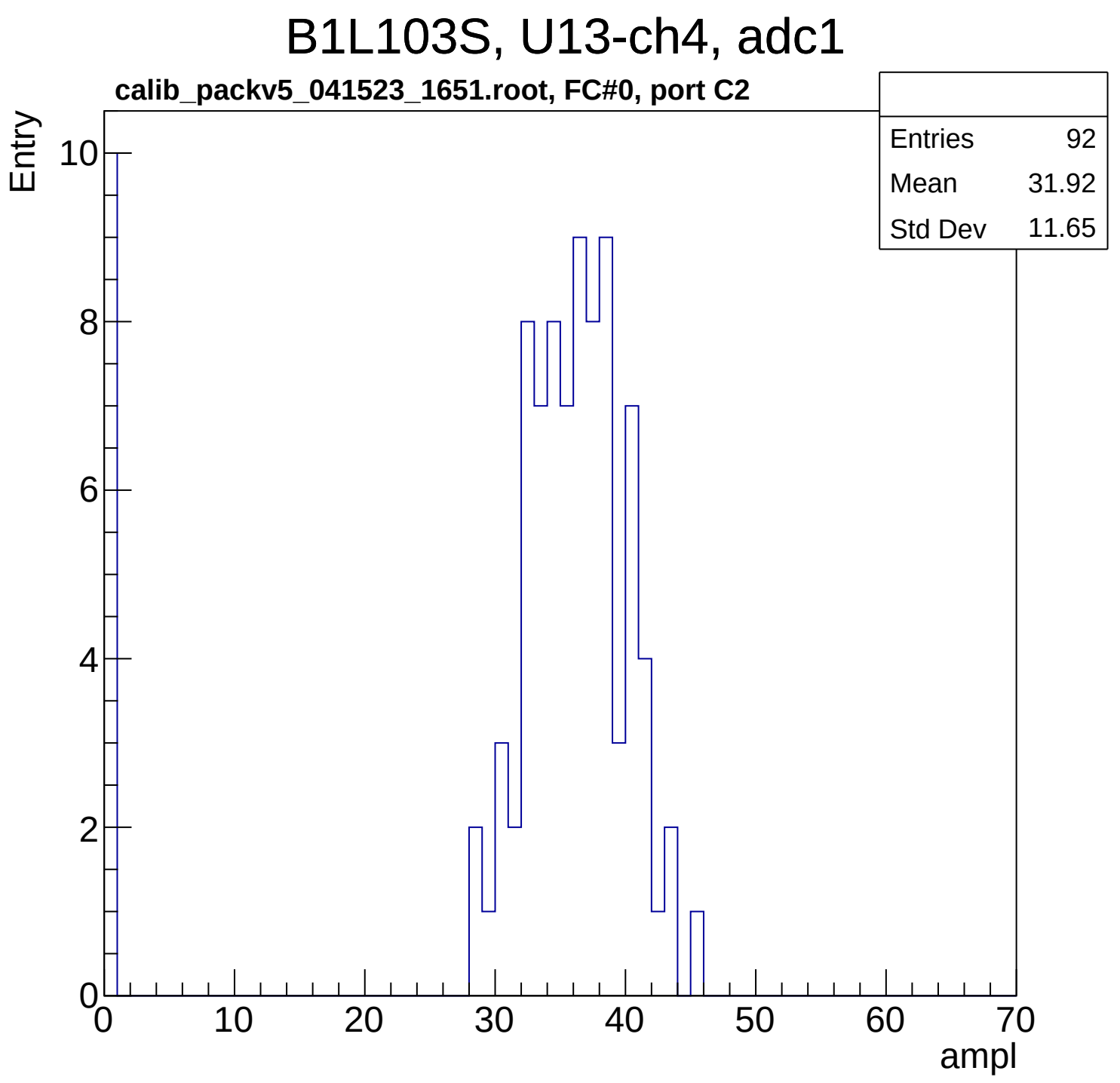
B1L103S, U13-ch4, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 31.92
Std Dev 11.65
Entry
ampl
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4
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8
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0
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40
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60
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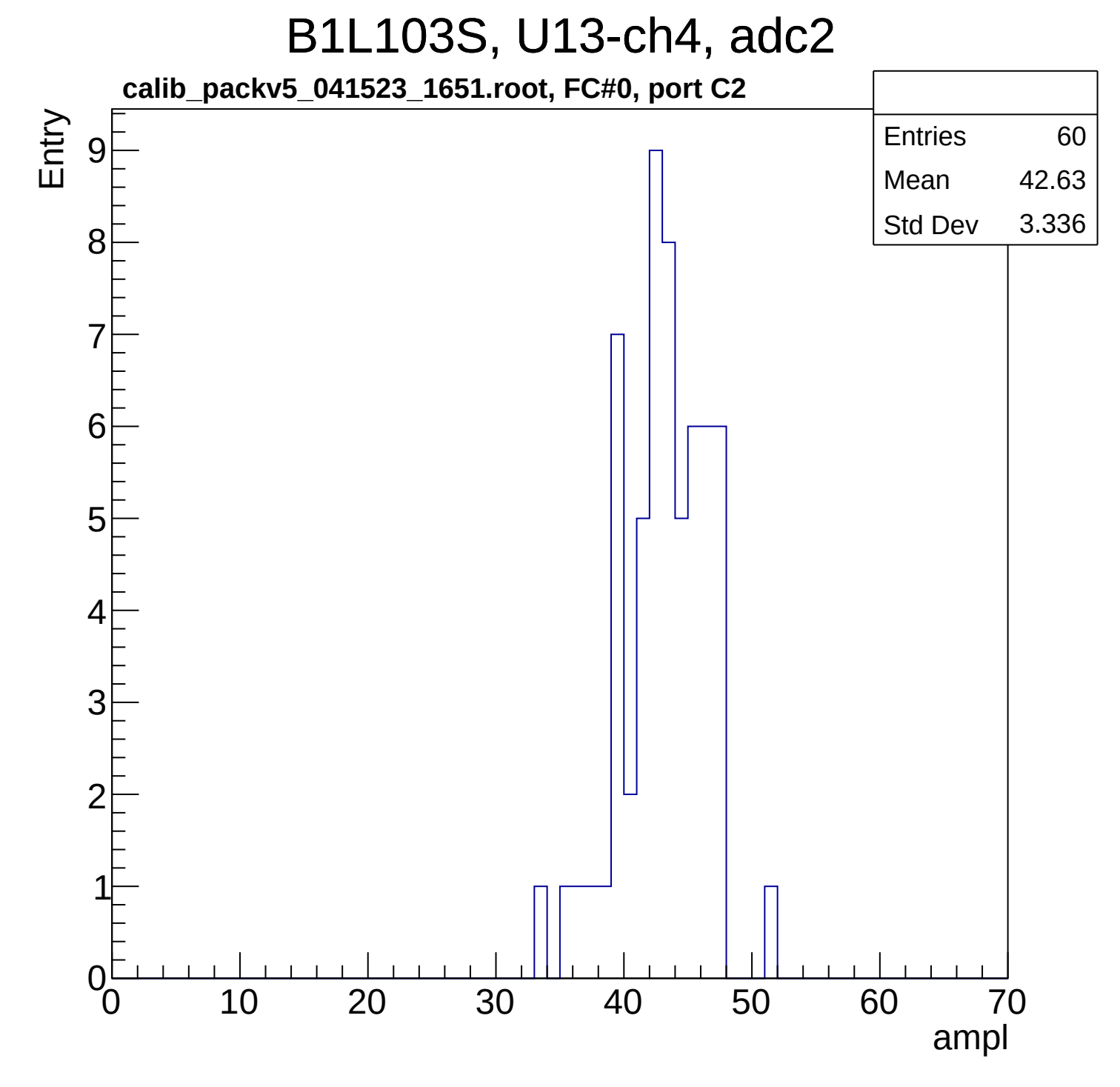
B1L103S, U13-ch4, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 42.63
Std Dev 3.336
Entry
ampl
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60
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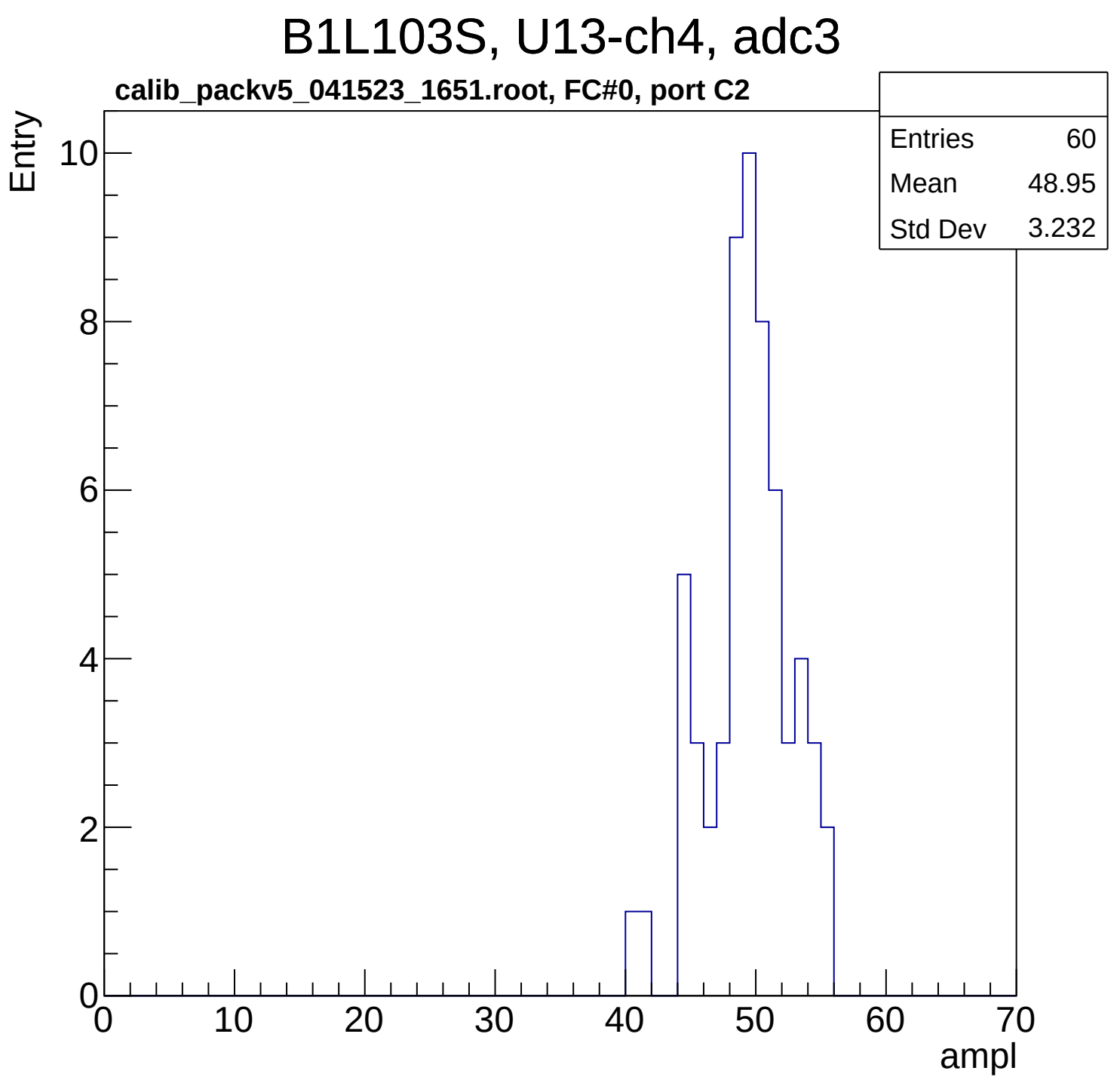
B1L103S, U13-ch4, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 48.95
Std Dev 3.232
Entry
ampl
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4
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8
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0
10
20
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40
50
60
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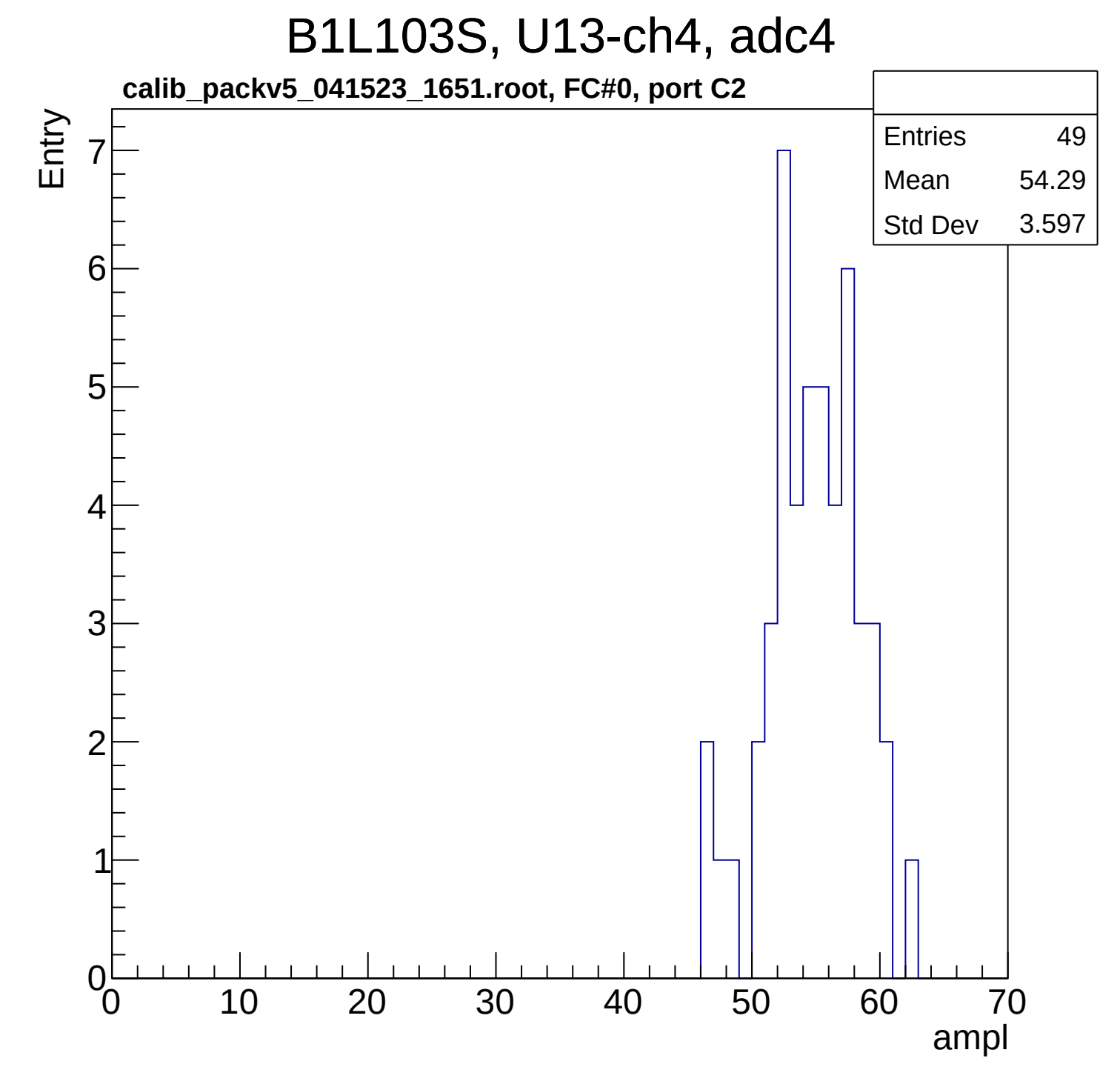
B1L103S, U13-ch4, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 54.29
Std Dev 3.597
Entry
ampl
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4
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0
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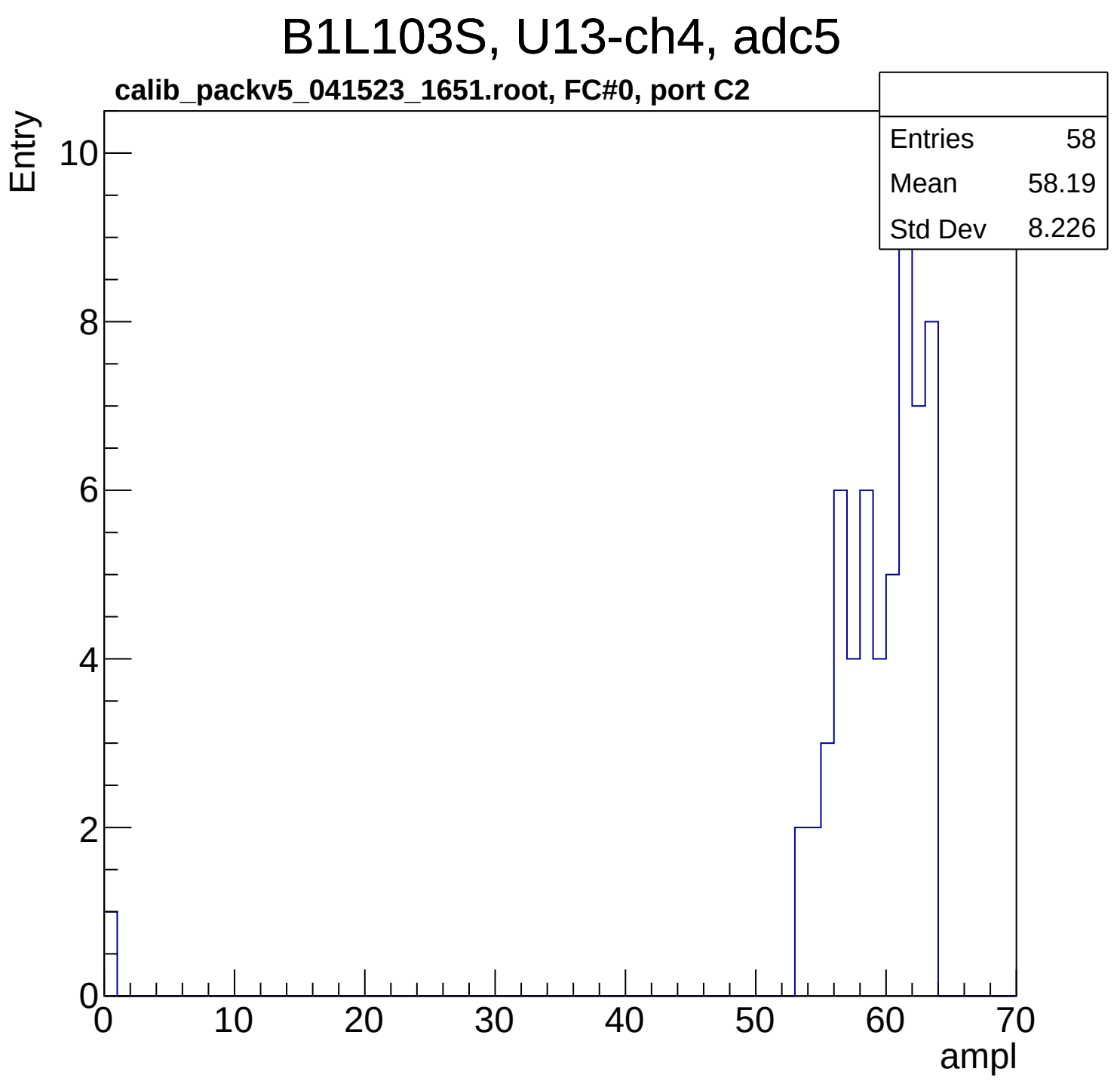
B1L103S, U13-ch4, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.19
Std Dev 8.226
Entry
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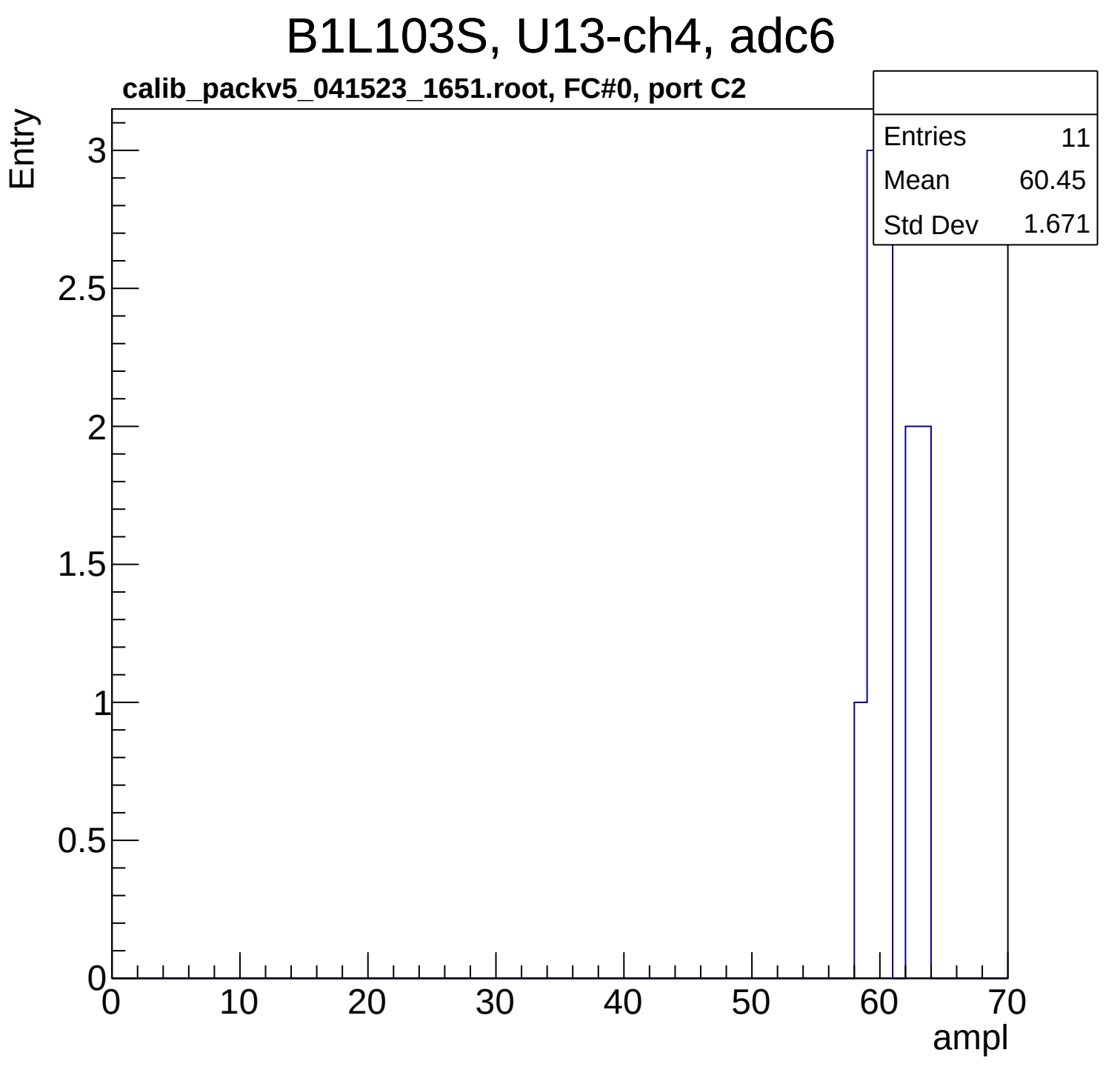
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch4, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 60.45
Std Dev 1.671
Entry
ampl
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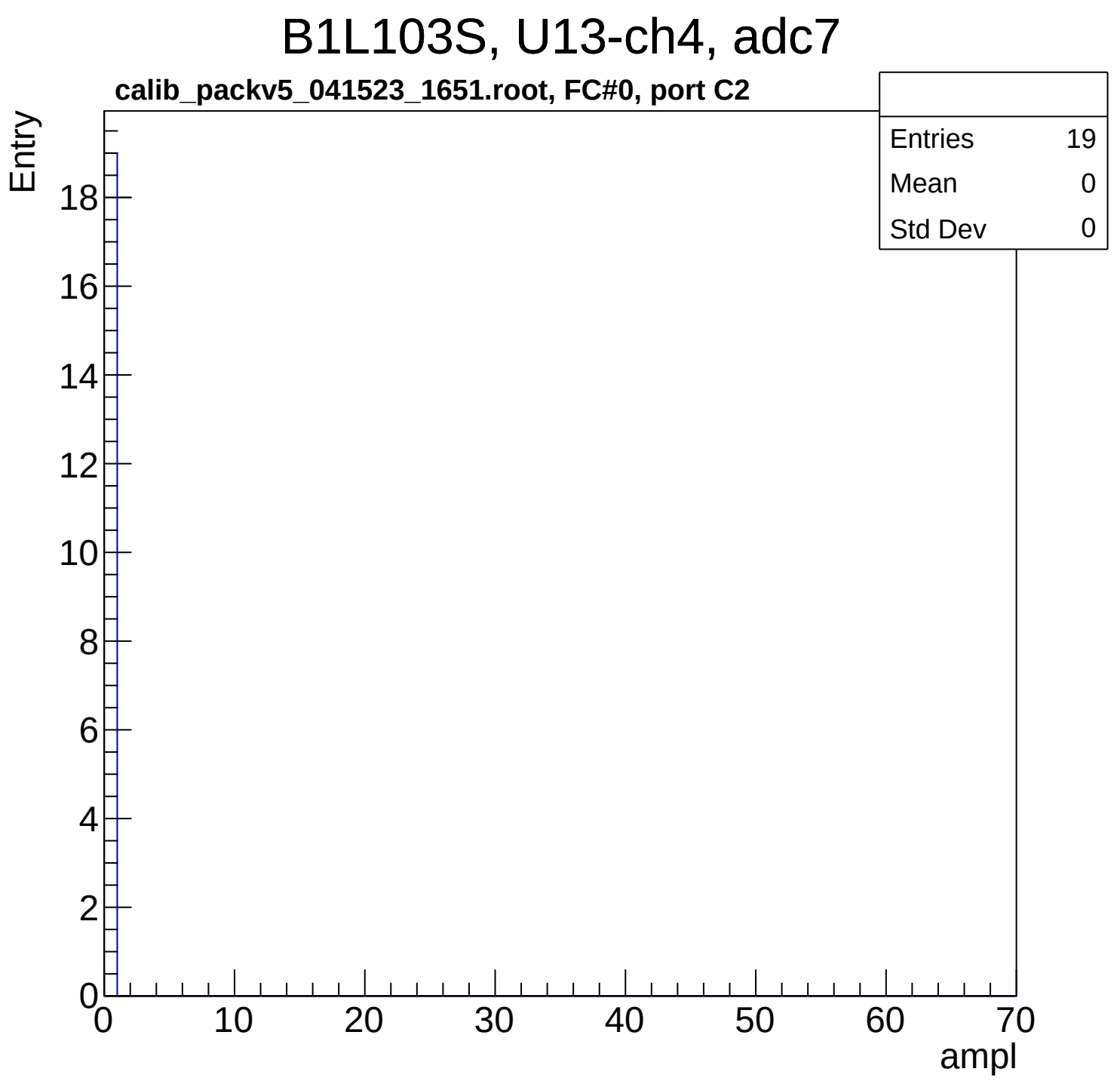
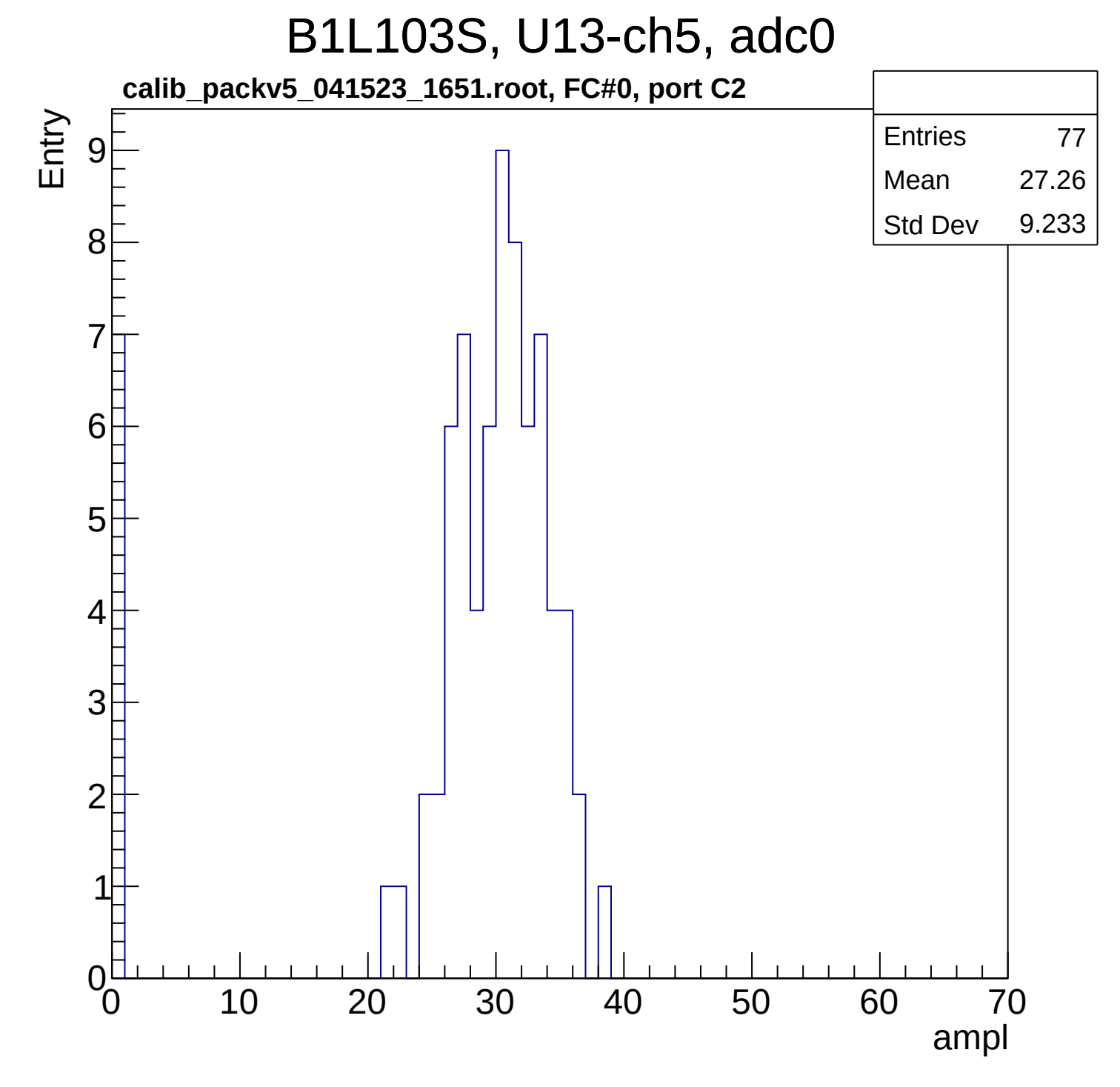
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U13-ch4, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch5, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 27.26
Std Dev 9.233
Entry
ampl
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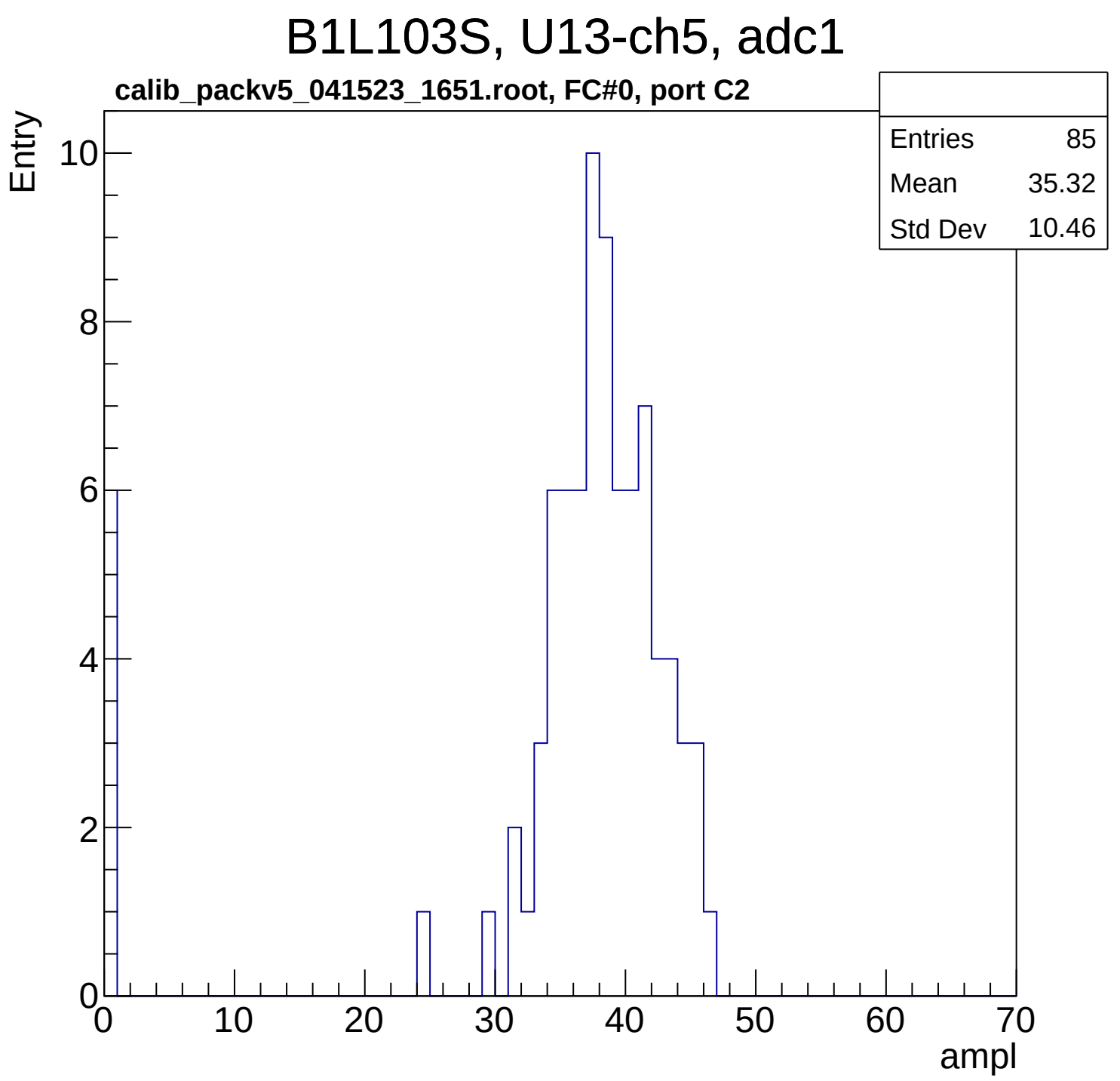
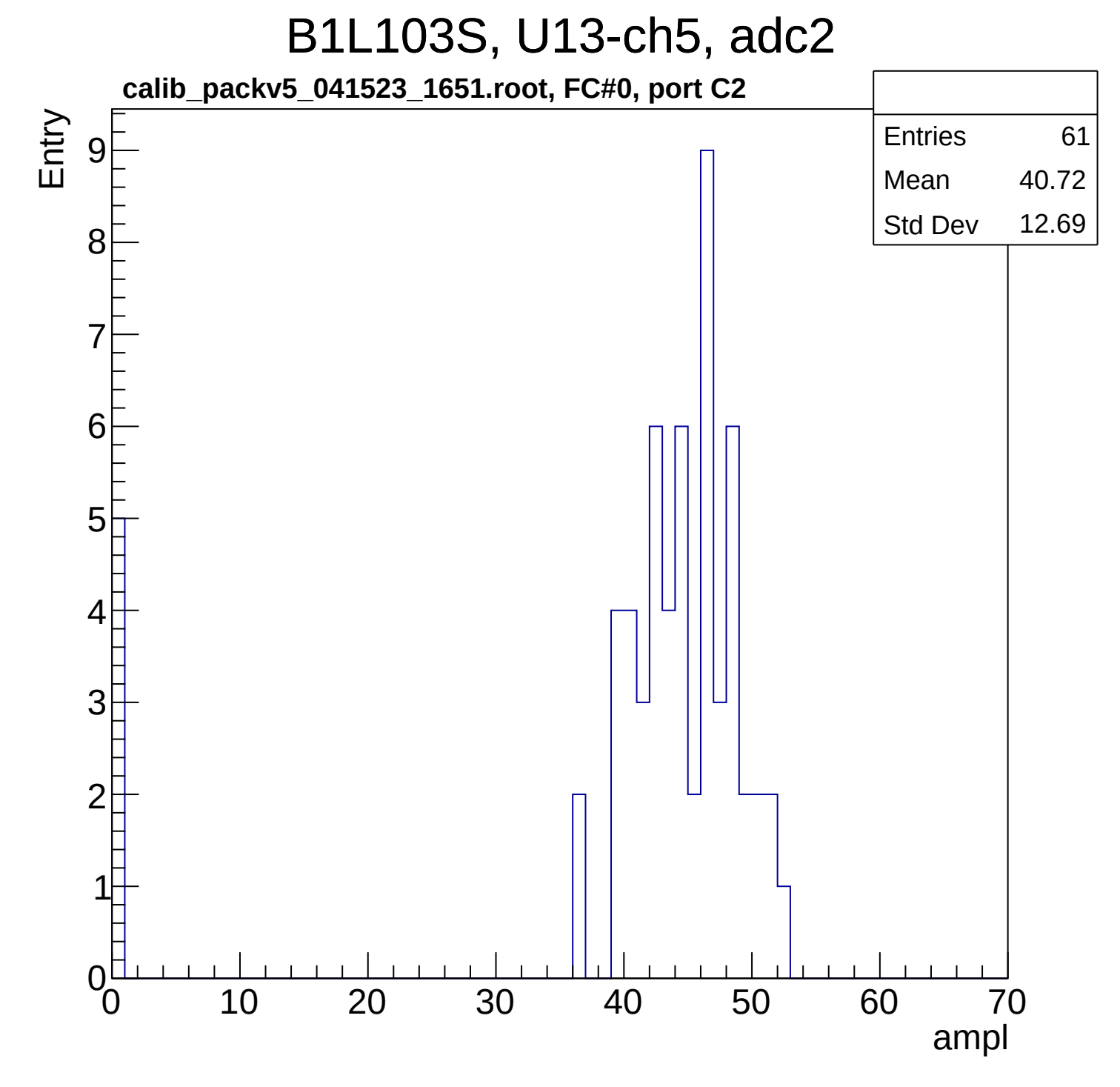
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch5, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 35.32
Std Dev 10.46
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch5, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 40.72
Std Dev 12.69
Entry
ampl
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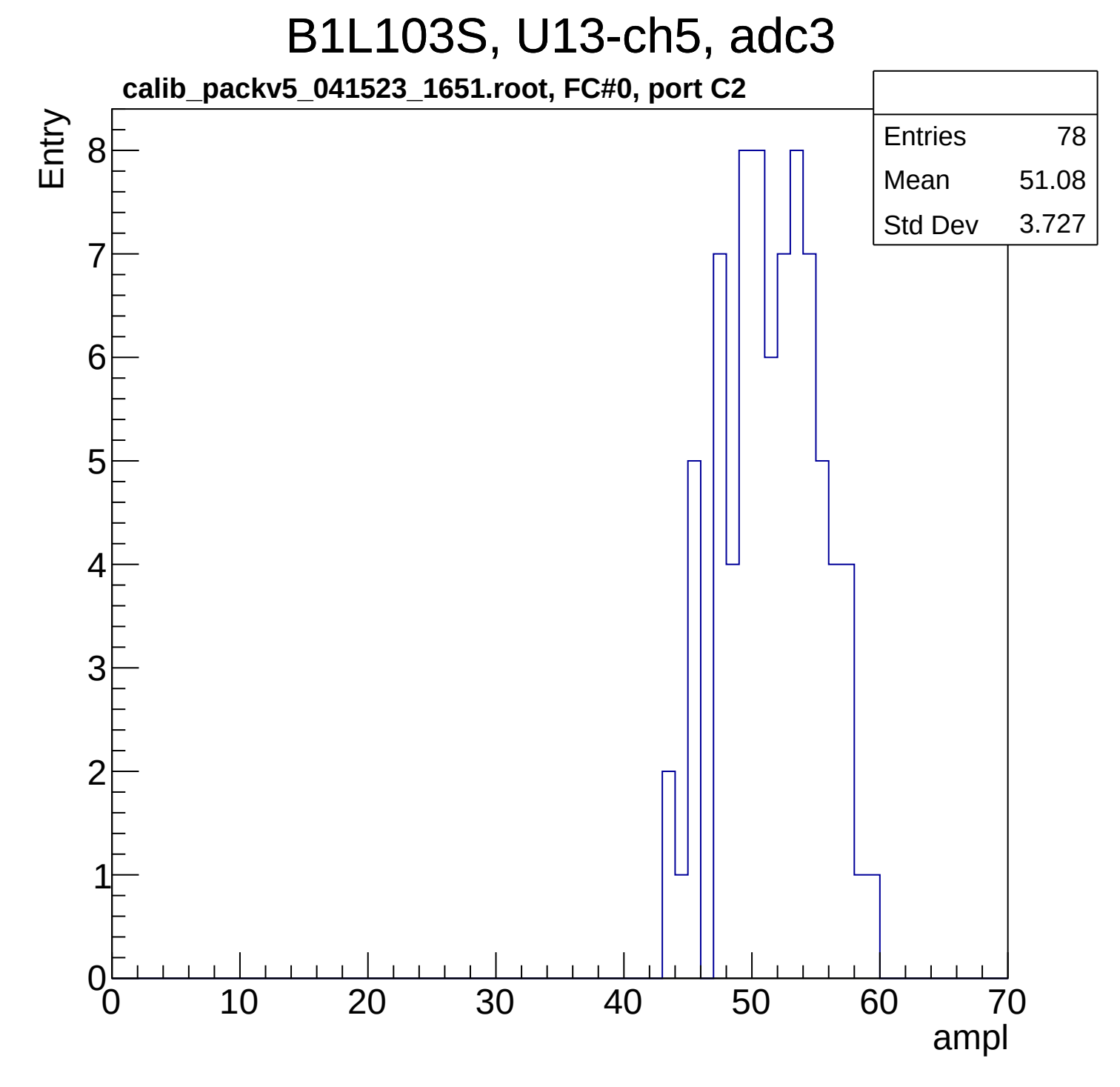
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch5, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 51.08
Std Dev 3.727
Entry
ampl
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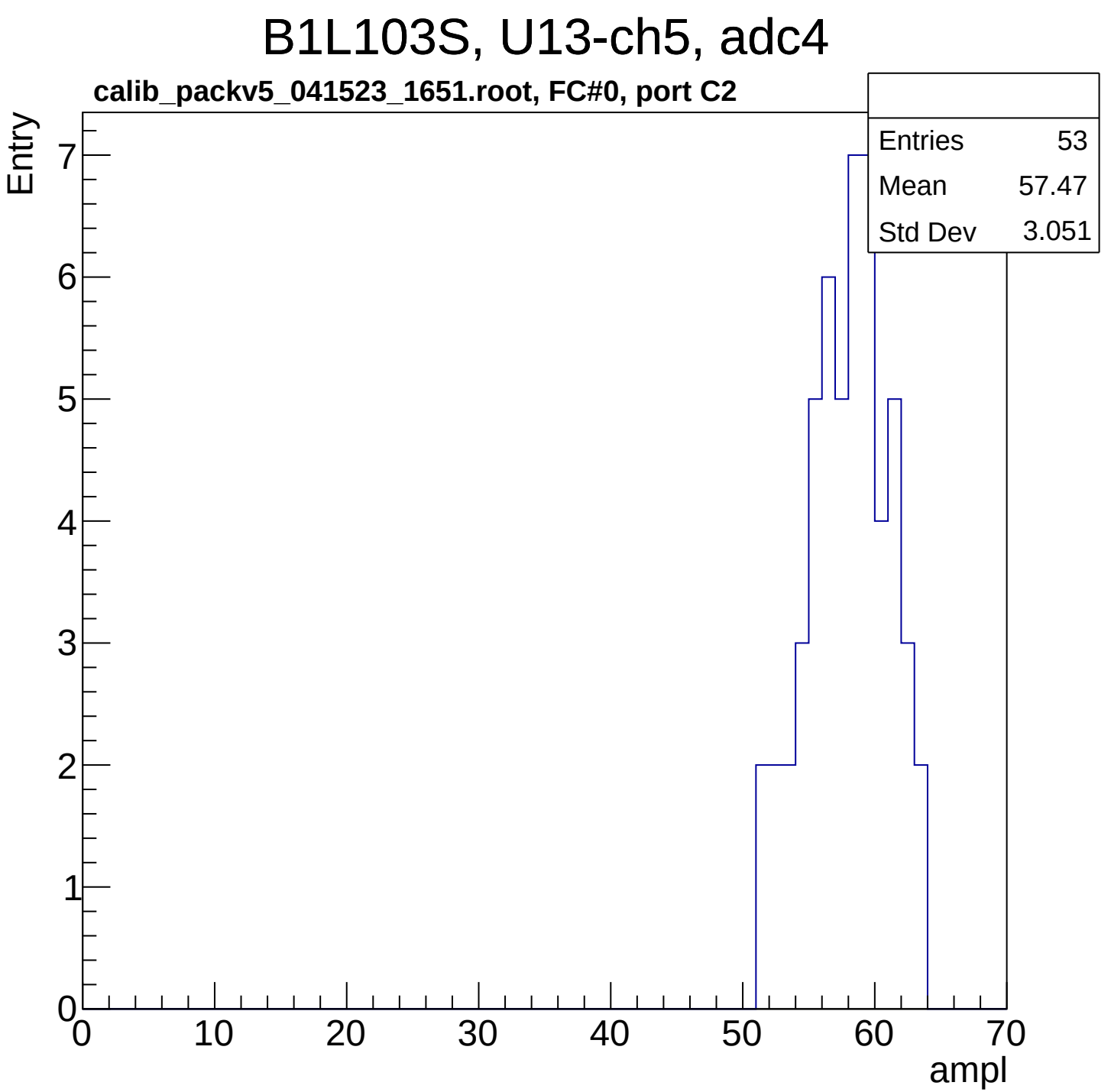
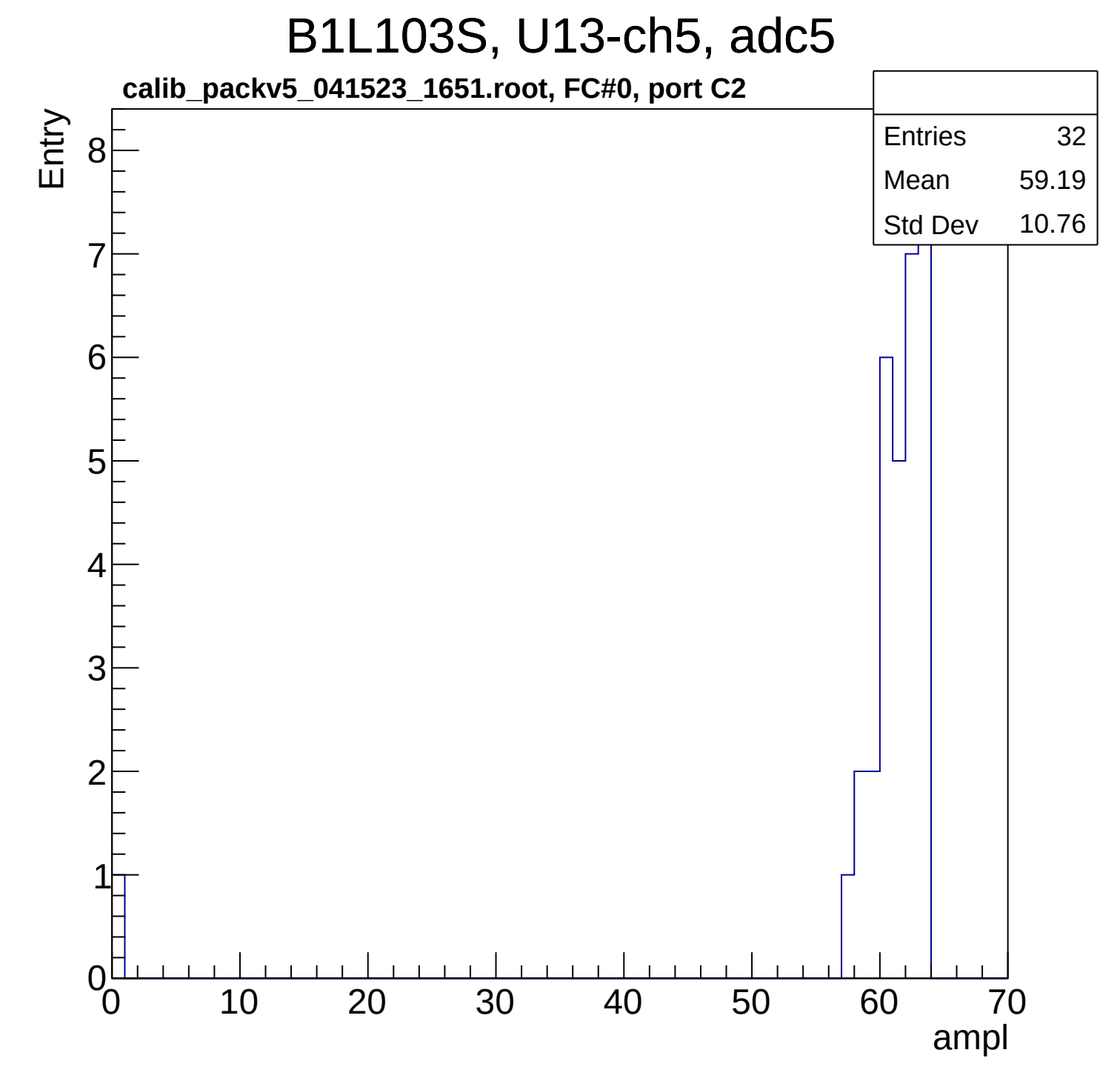
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch5, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 57.47
Std Dev 3.051
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch5, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 59.19
Std Dev 10.76
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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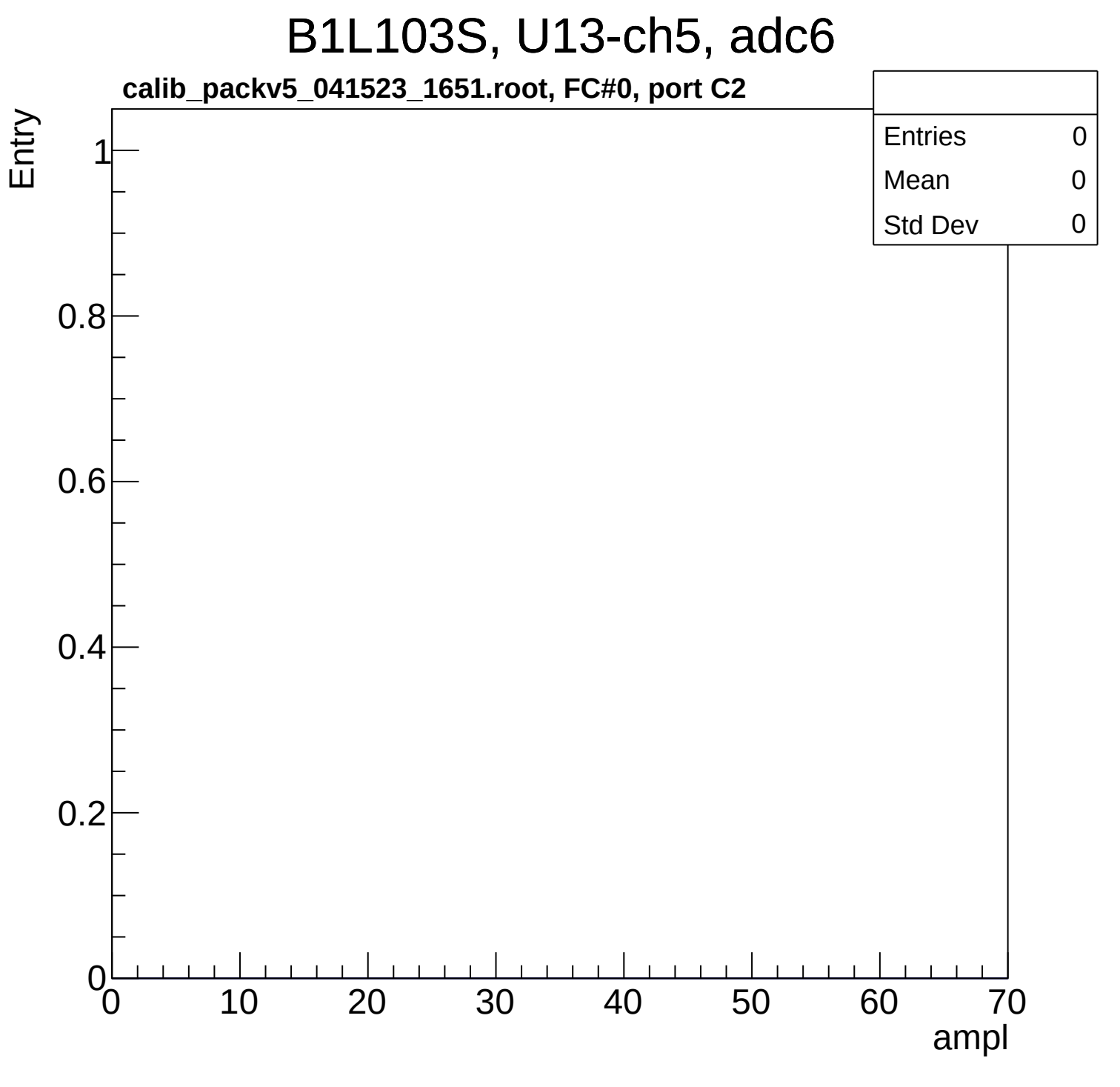
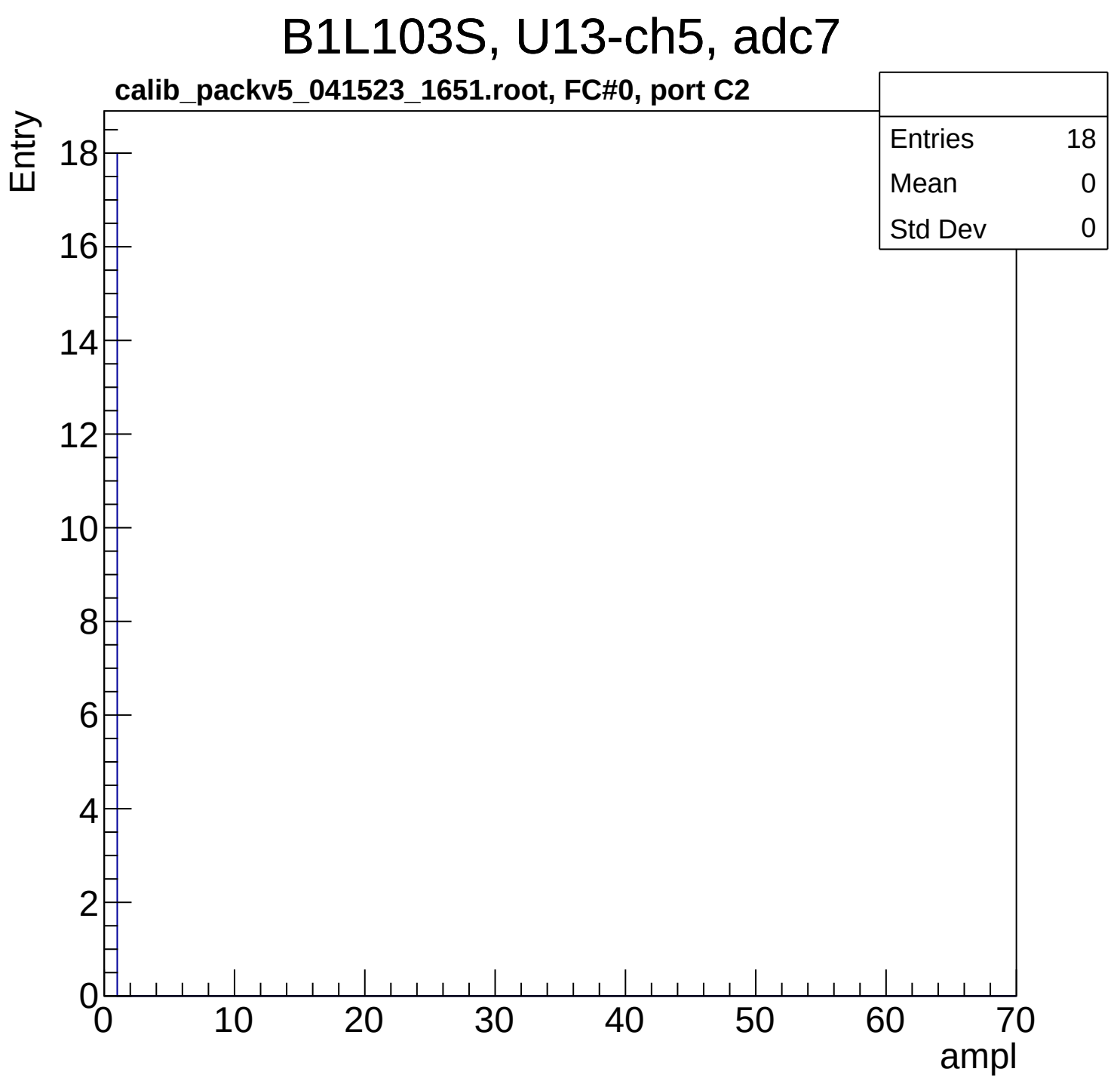
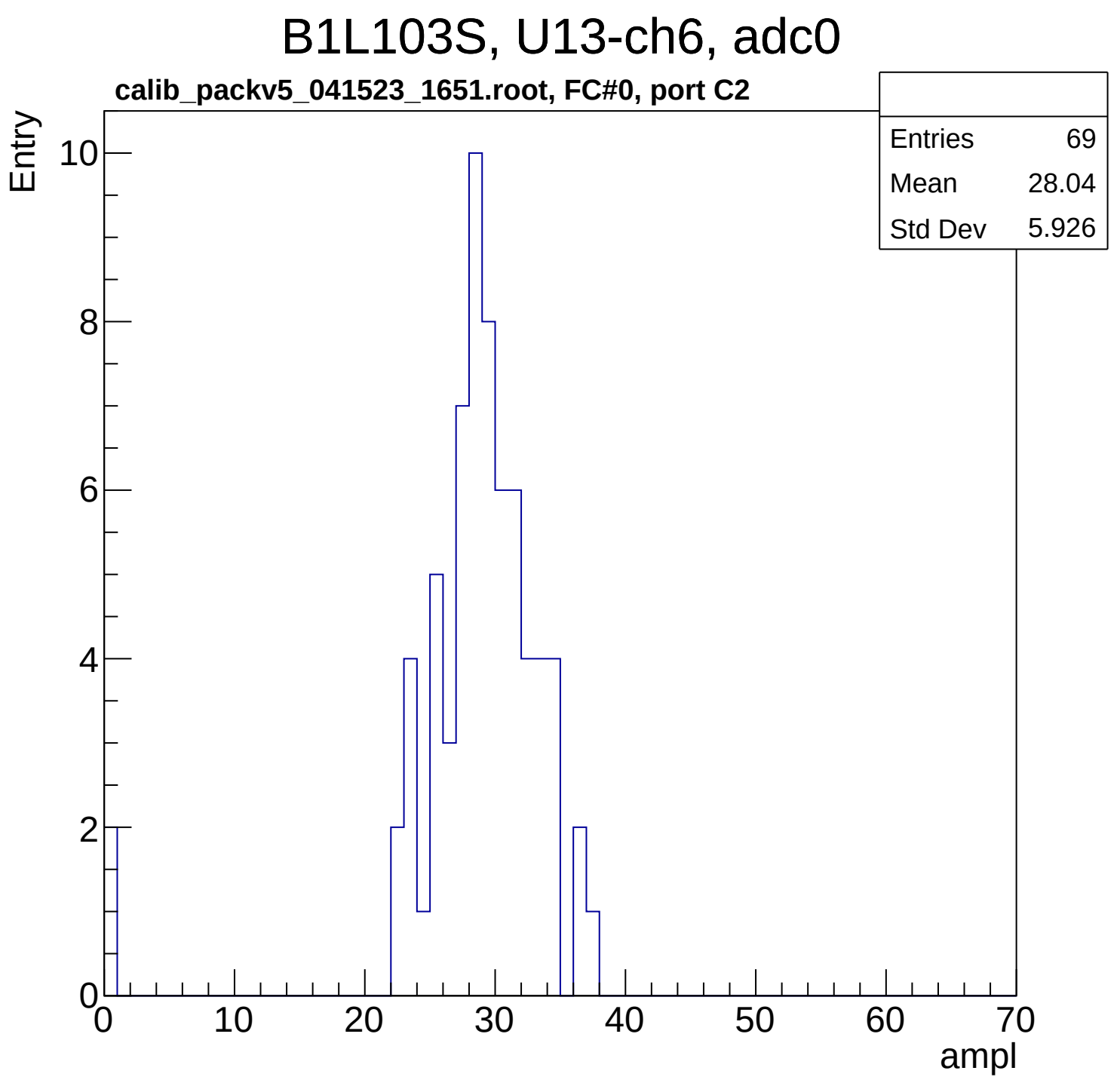

B1L103S, U13-ch5, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch5, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch6, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 28.04
Std Dev 5.926
Entry
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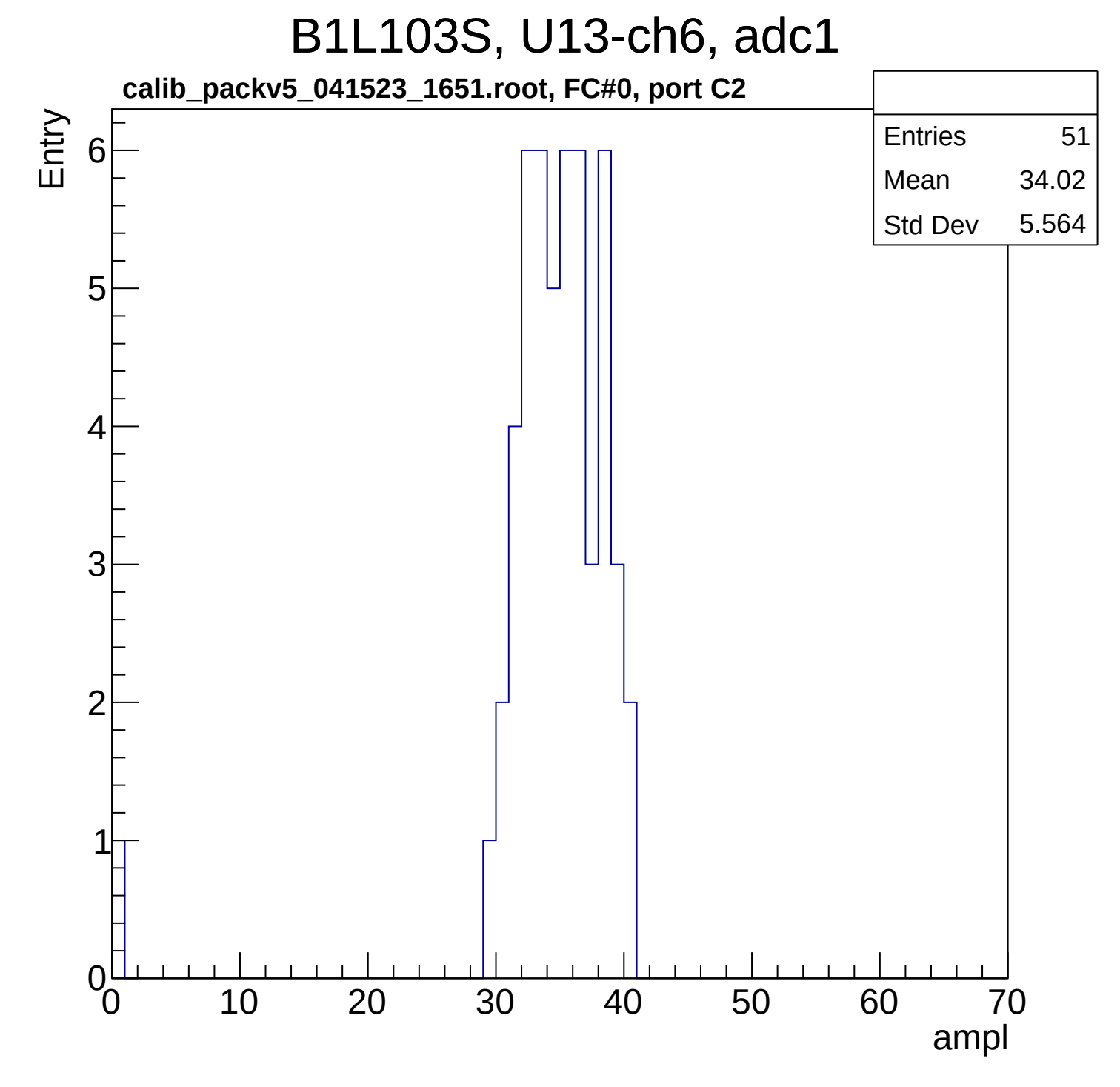
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch6, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 34.02
Std Dev 5.564
Entry
ampl
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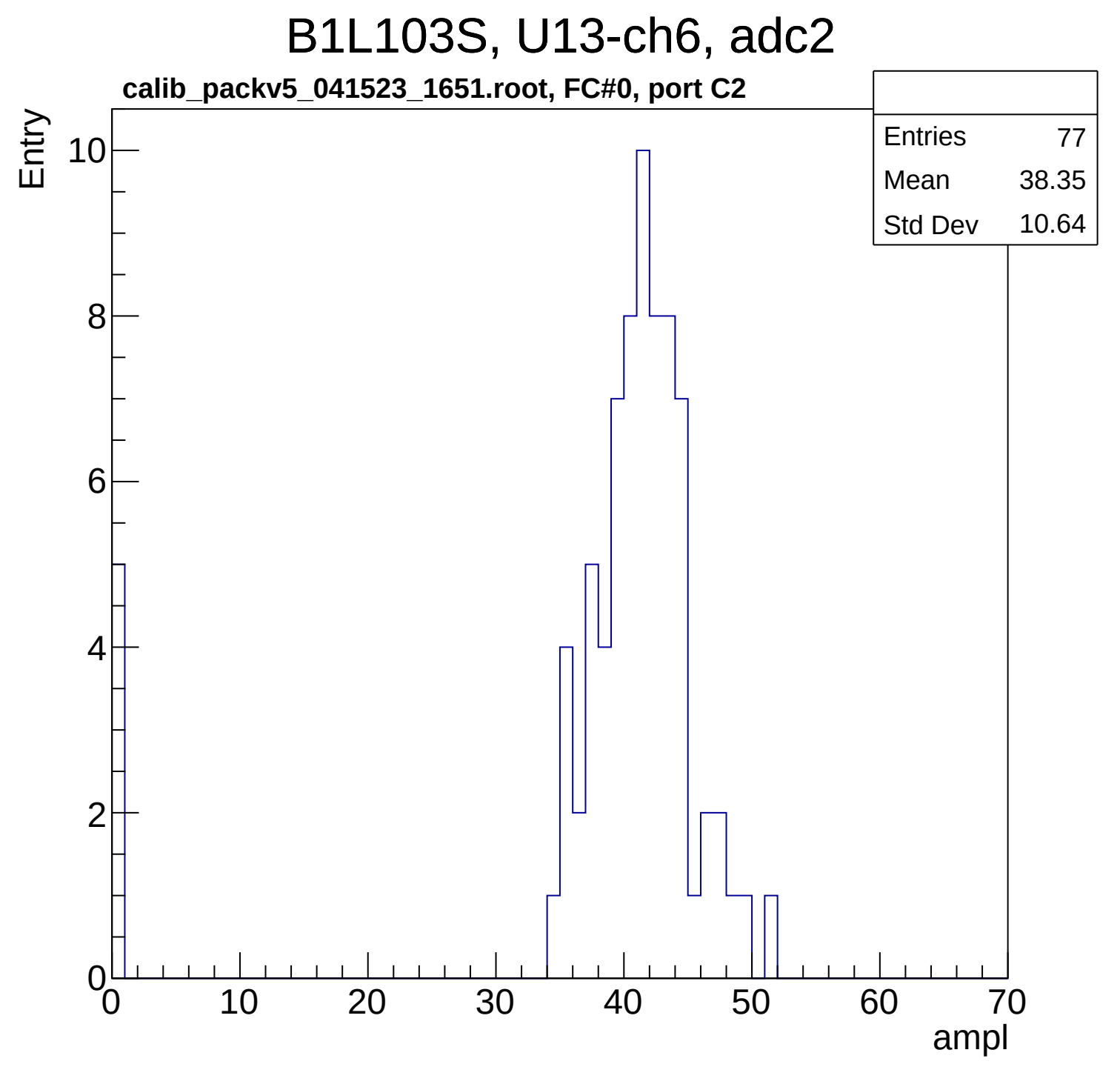
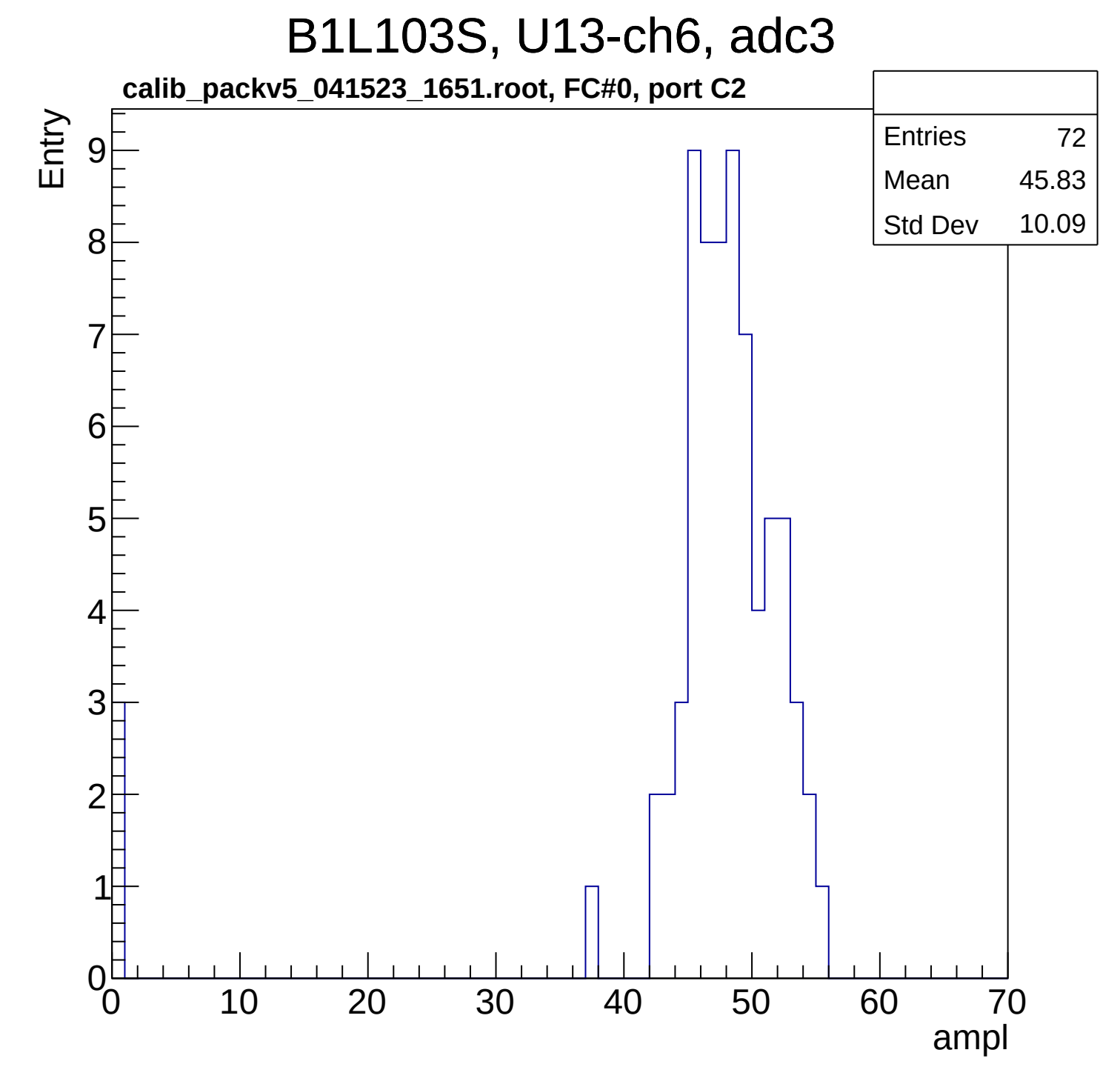
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U13-ch6, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 38.35
Std Dev 10.64
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch6, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 45.83
Std Dev 10.09
Entry
ampl
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2
3
4
5
6
7
8
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0
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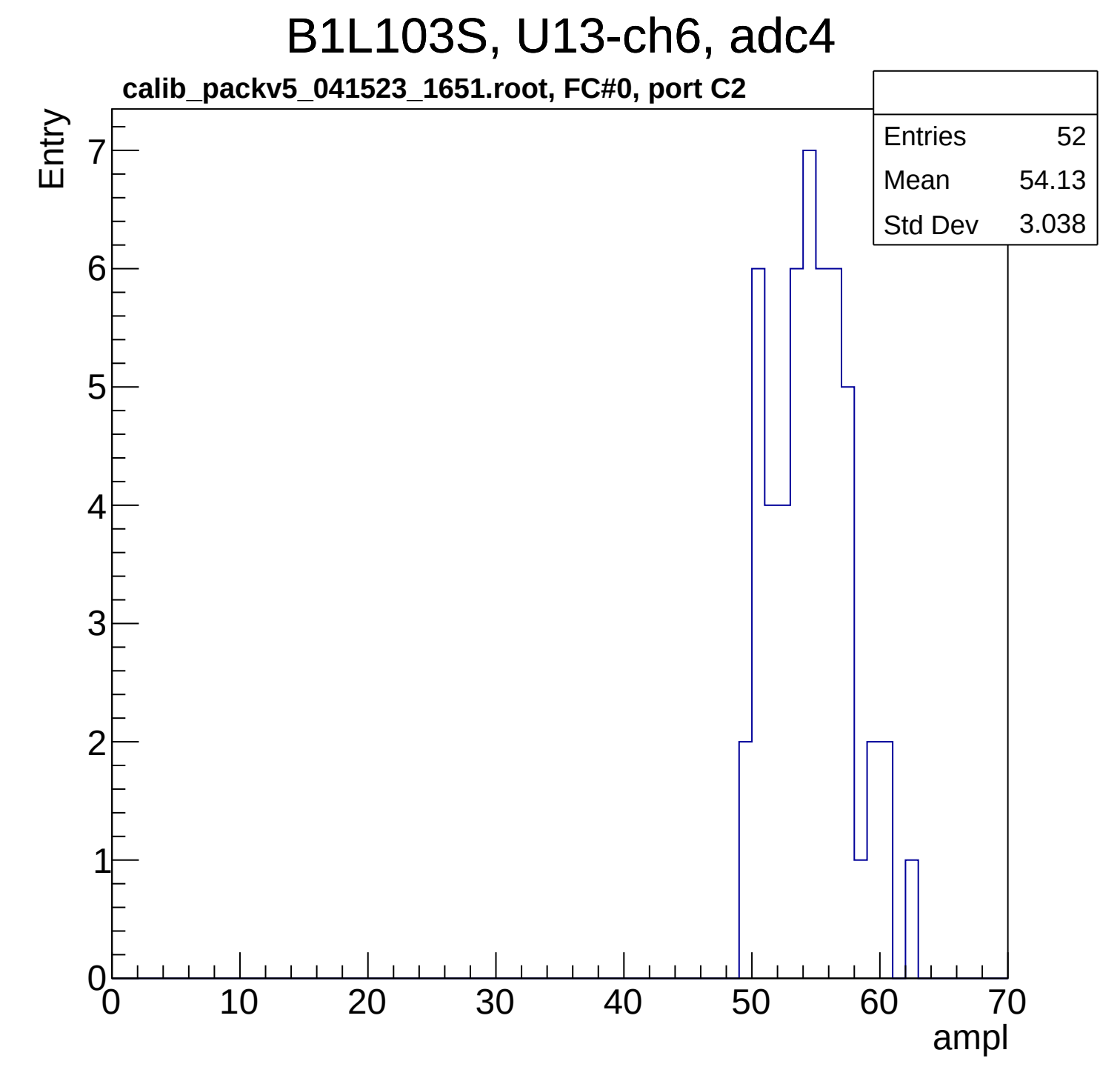
B1L103S, U13-ch6, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 54.13
Std Dev 3.038
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
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60
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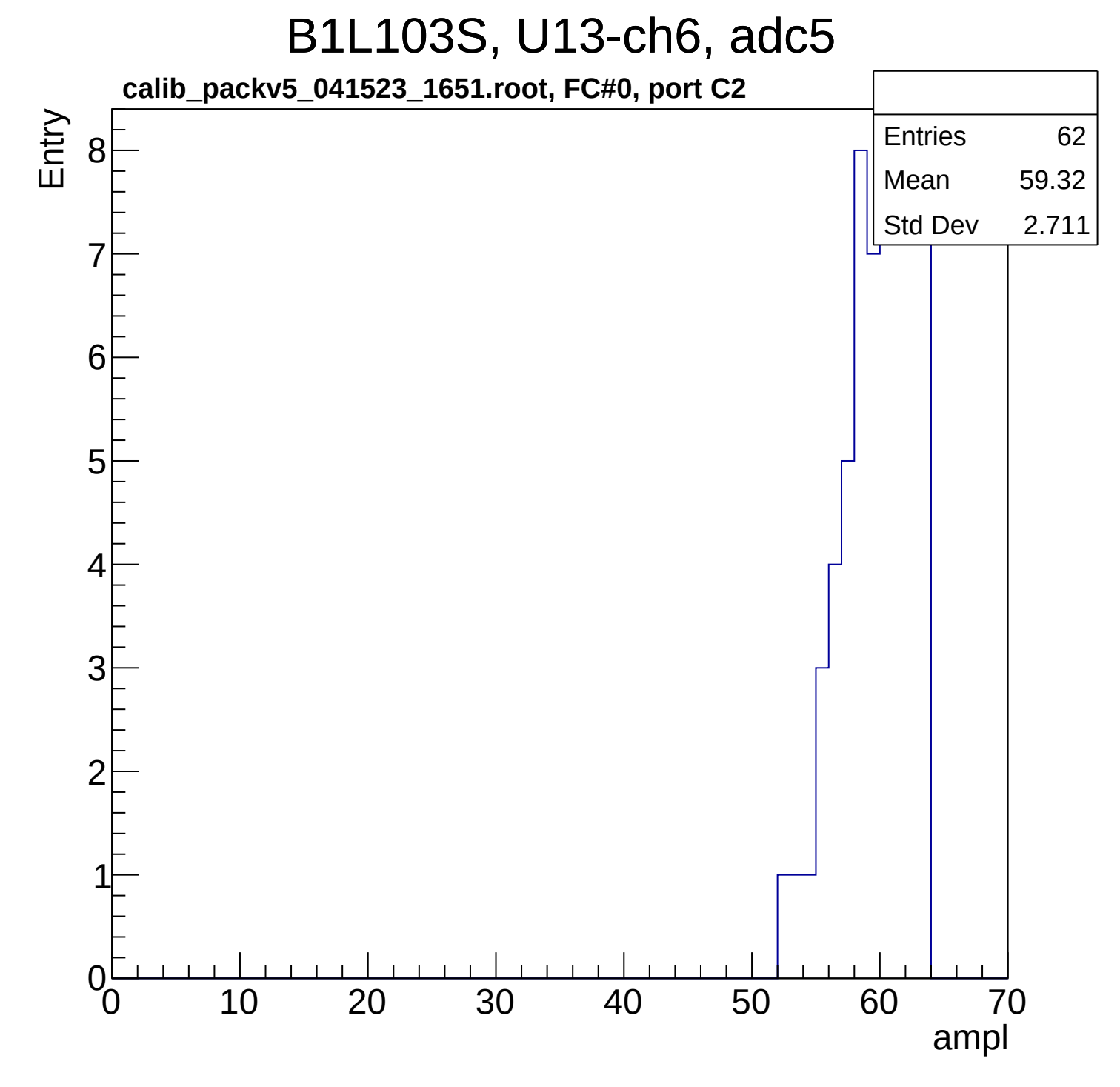
B1L103S, U13-ch6, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 59.32
Std Dev 2.711
Entry
ampl
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1
2
3
4
5
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7
8
0
10
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60
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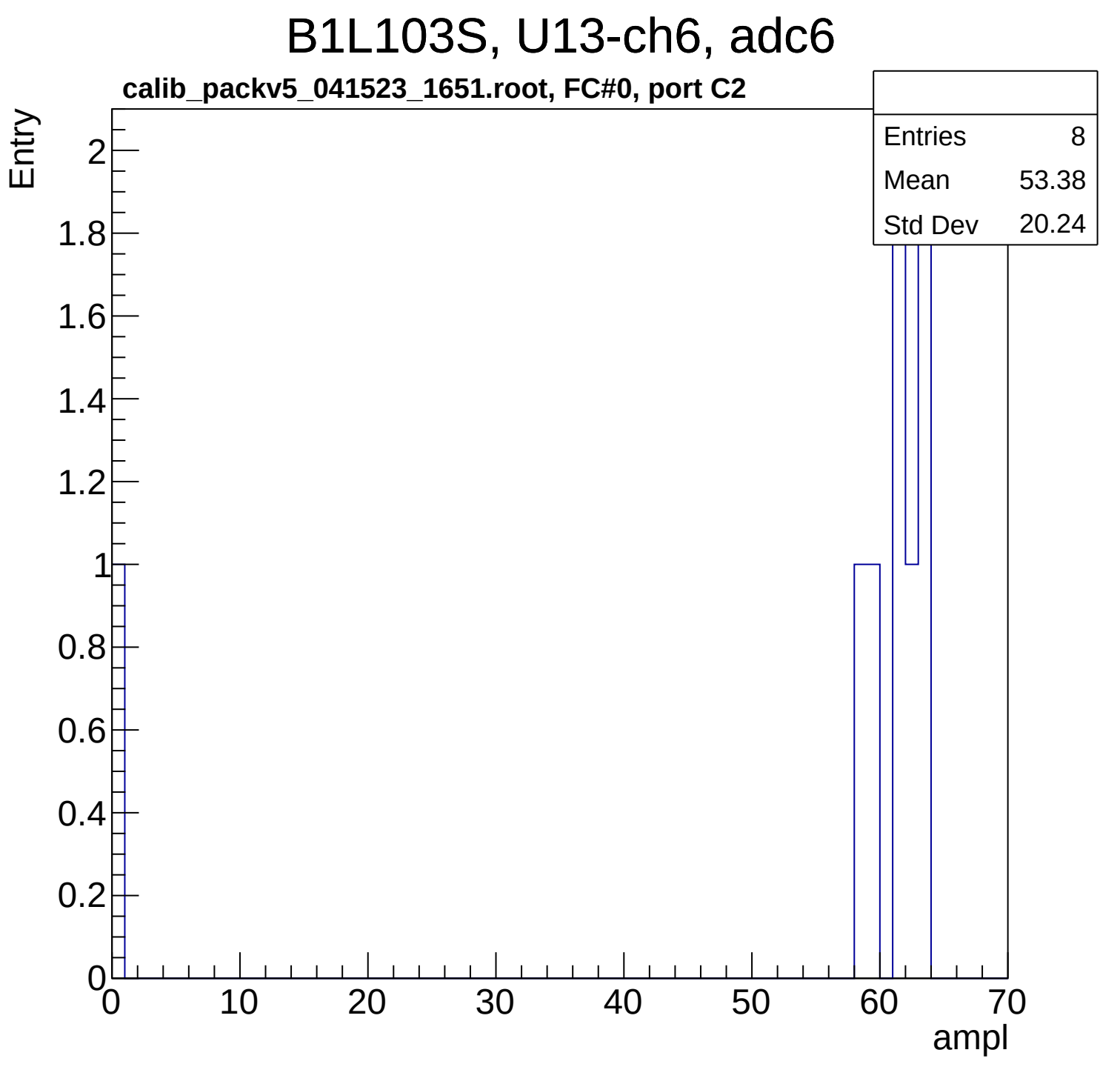
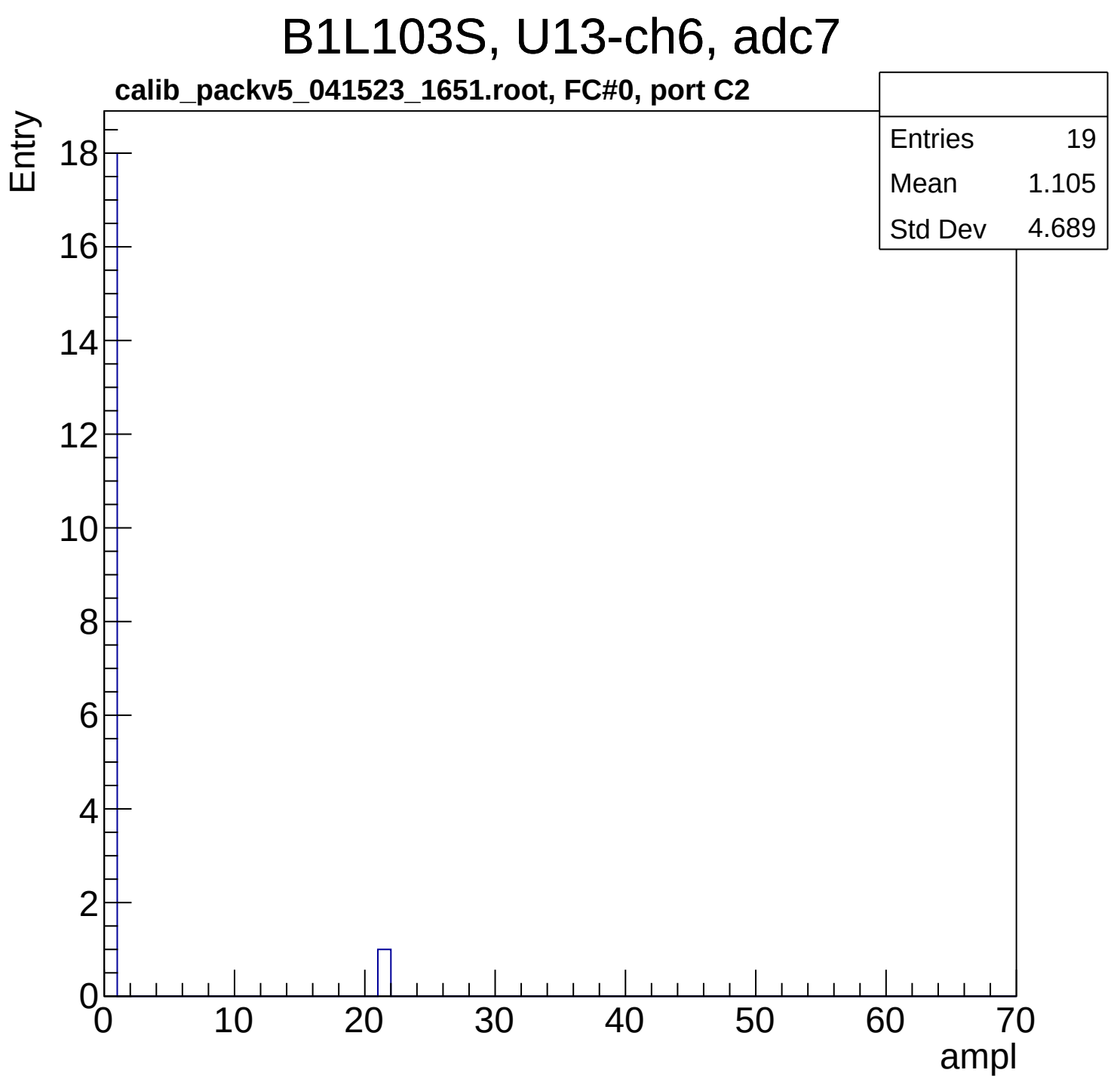

B1L103S, U13-ch6, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 53.38
Std Dev 20.24
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U13-ch6, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
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6
8
10
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14
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18
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10
20
30
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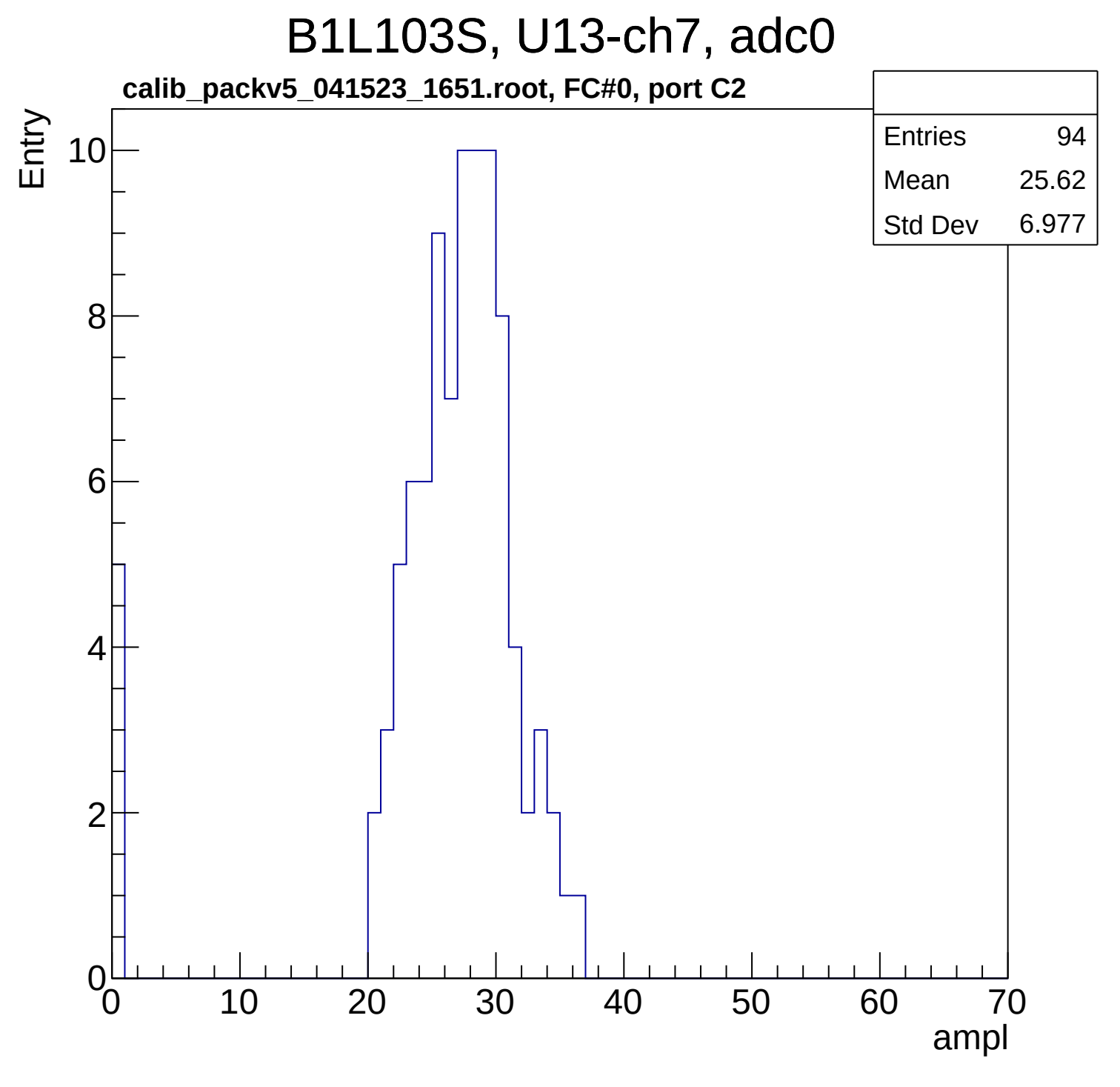
50
60
70
ampl


B1L103S, U13-ch7, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 25.62
Std Dev 6.977
Entry
ampl
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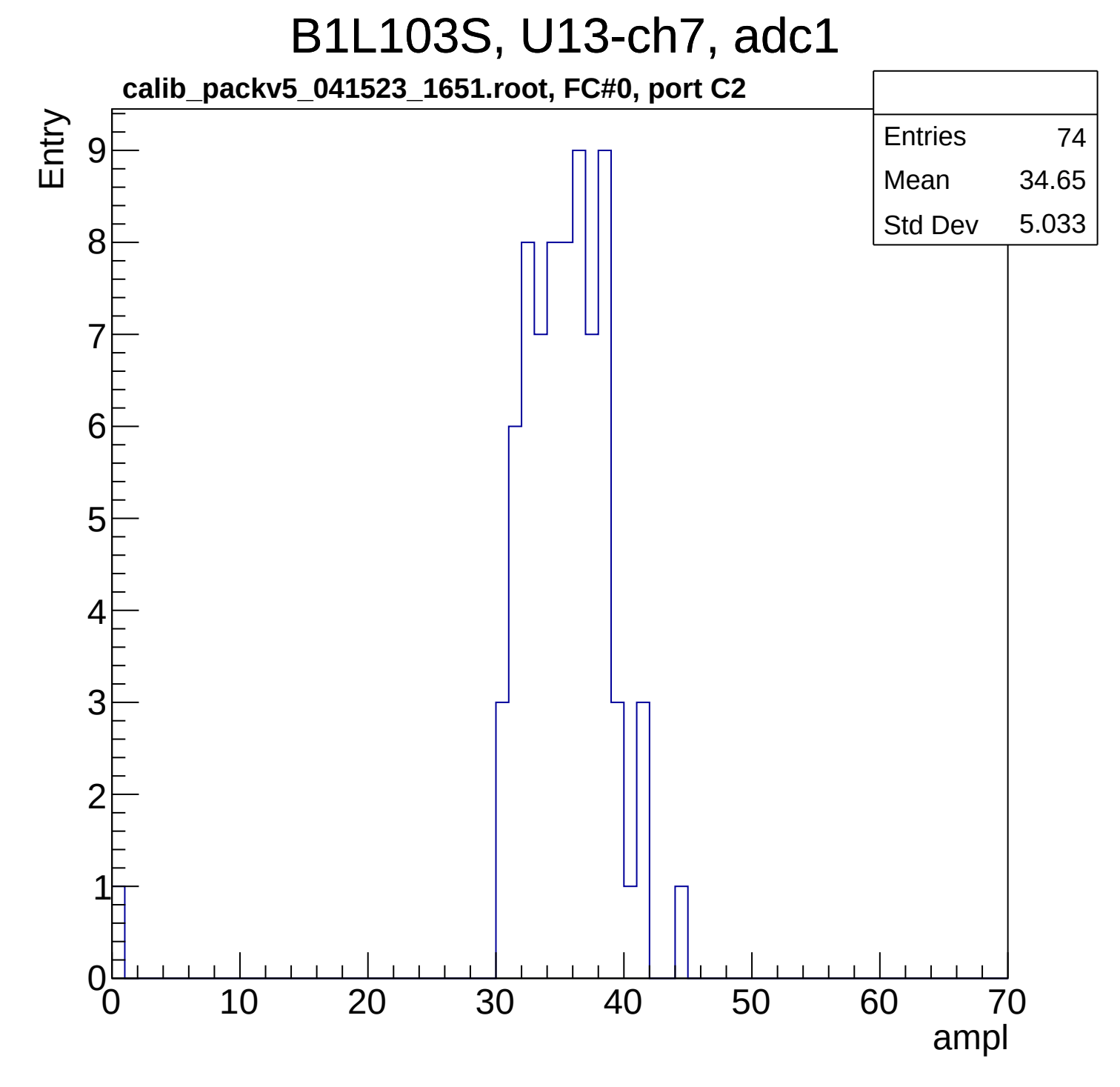
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch7, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 34.65
Std Dev 5.033
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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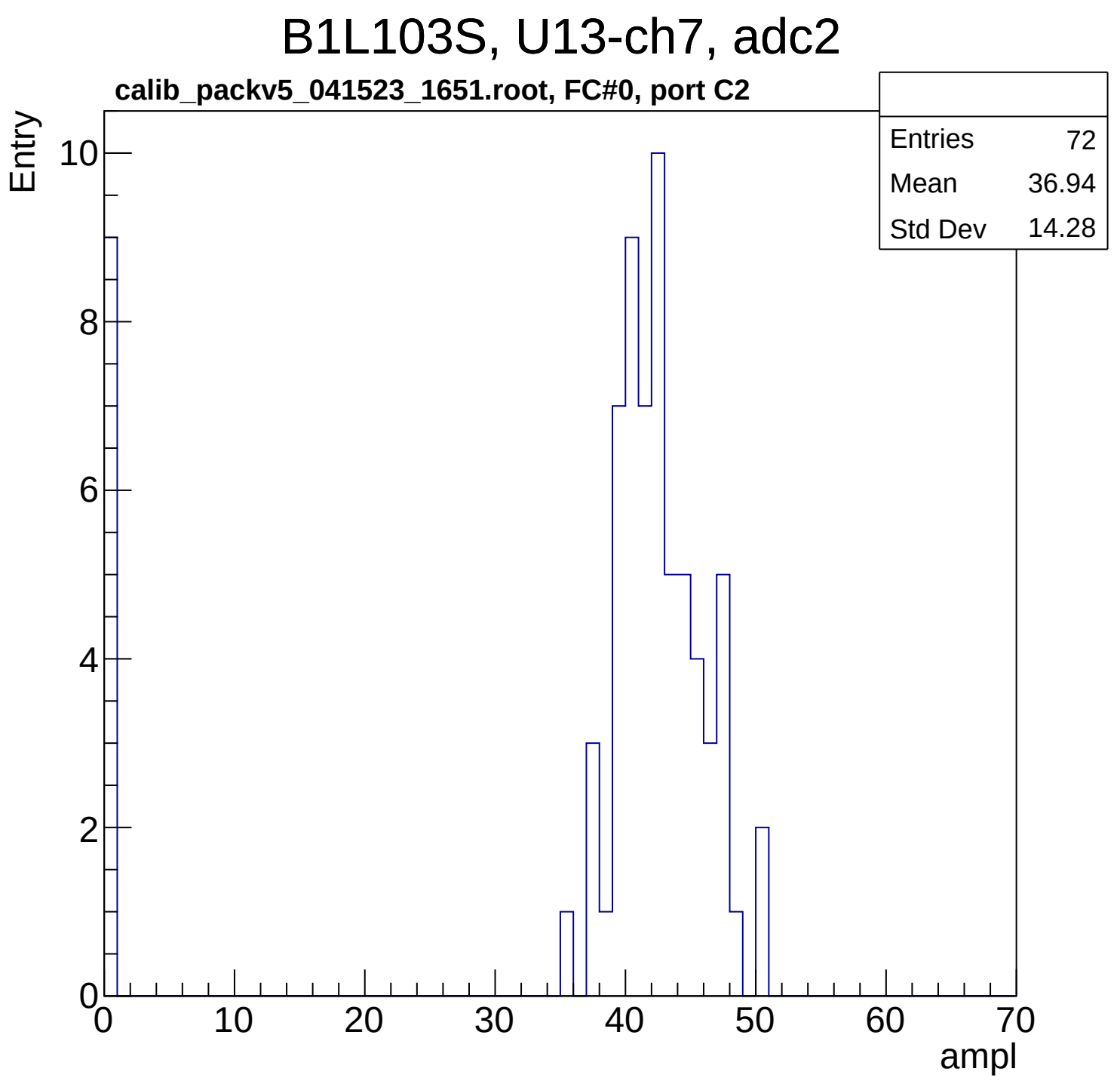
40
50
60
70


B1L103S, U13-ch7, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 36.94
Std Dev 14.28
Entry
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4
6
8
10
0
10
20
30
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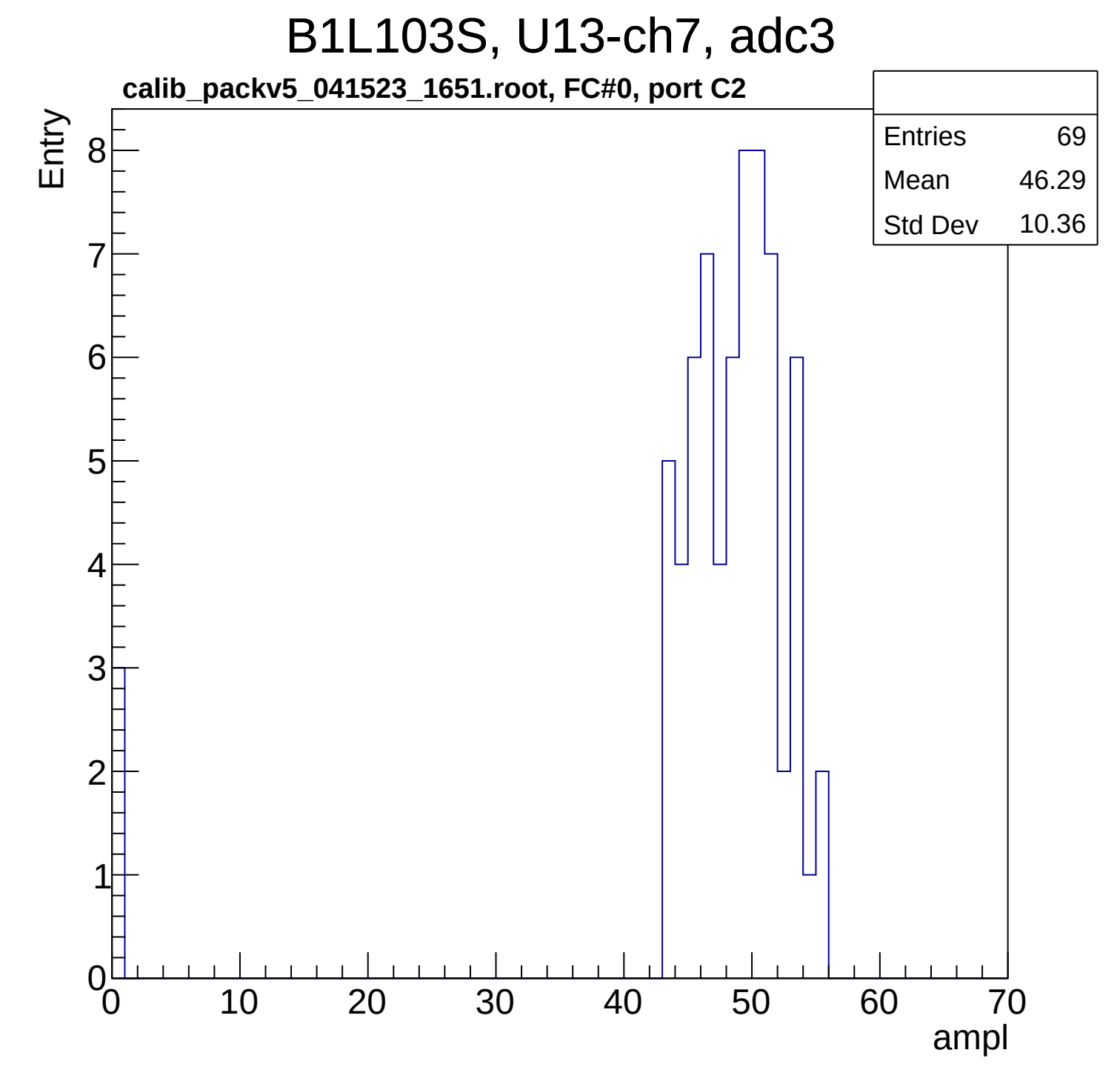
50
60
70
ampl


B1L103S, U13-ch7, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 46.29
Std Dev 10.36
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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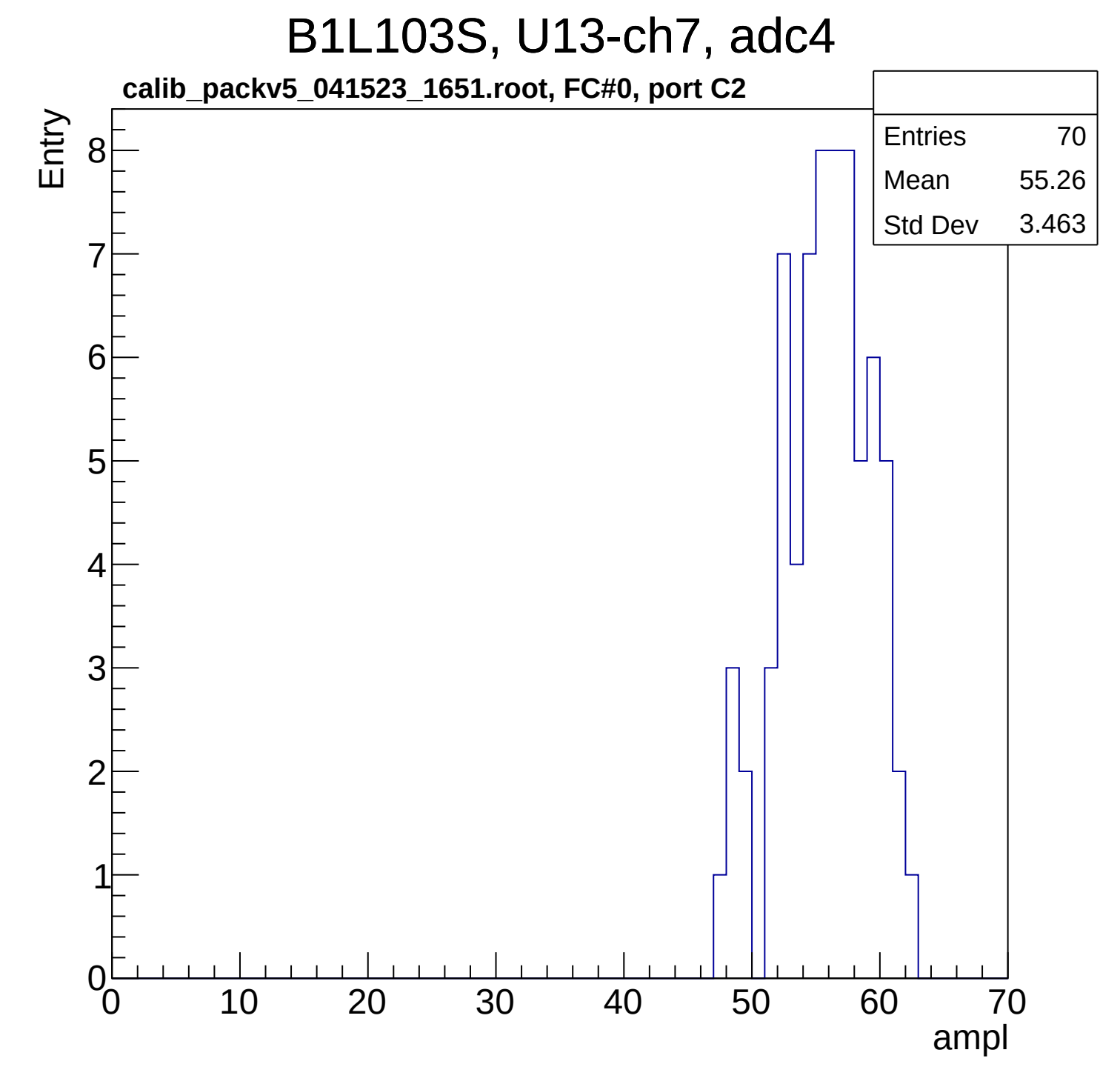
B1L103S, U13-ch7, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 55.26
Std Dev 3.463
Entry
ampl
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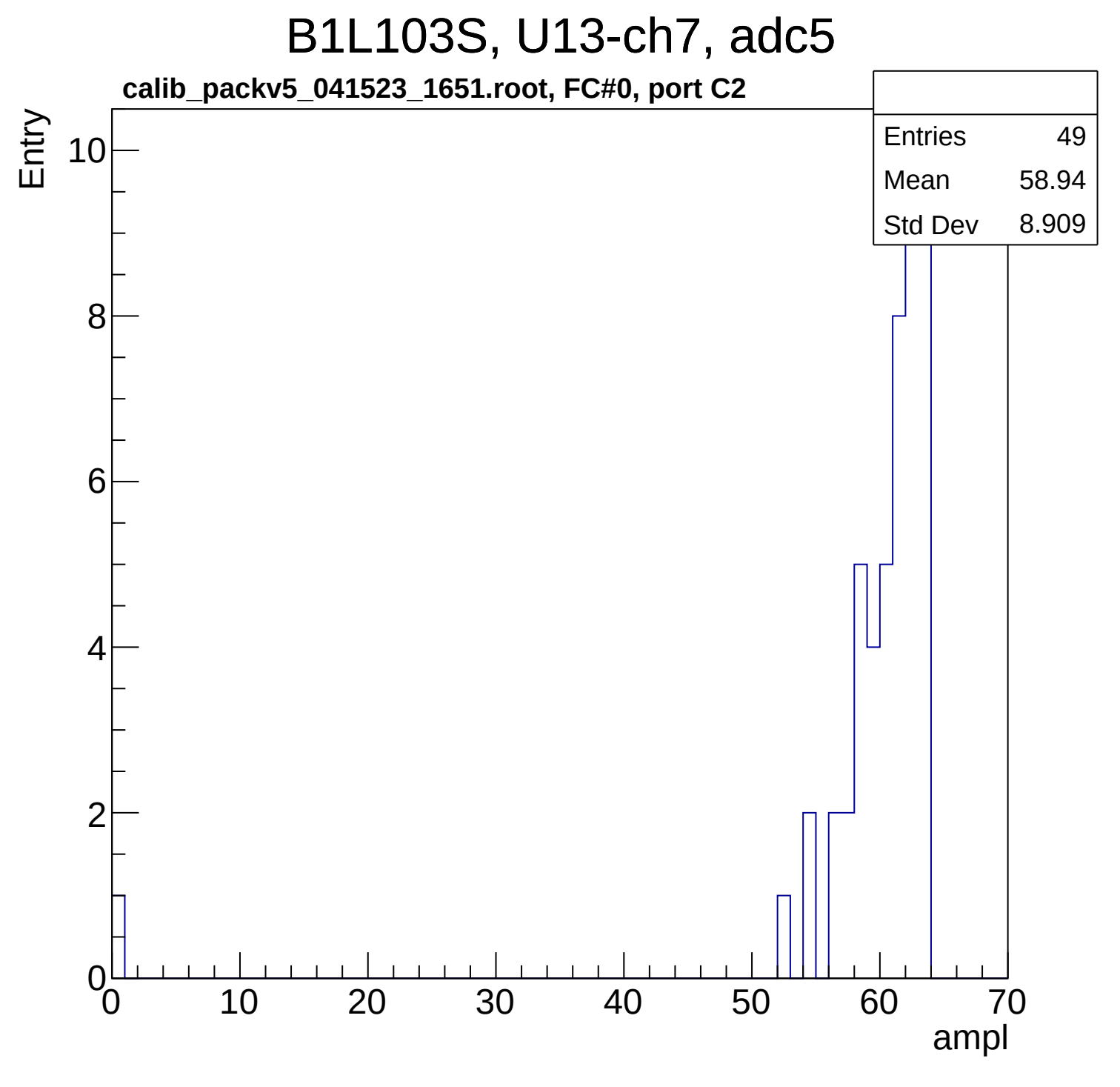
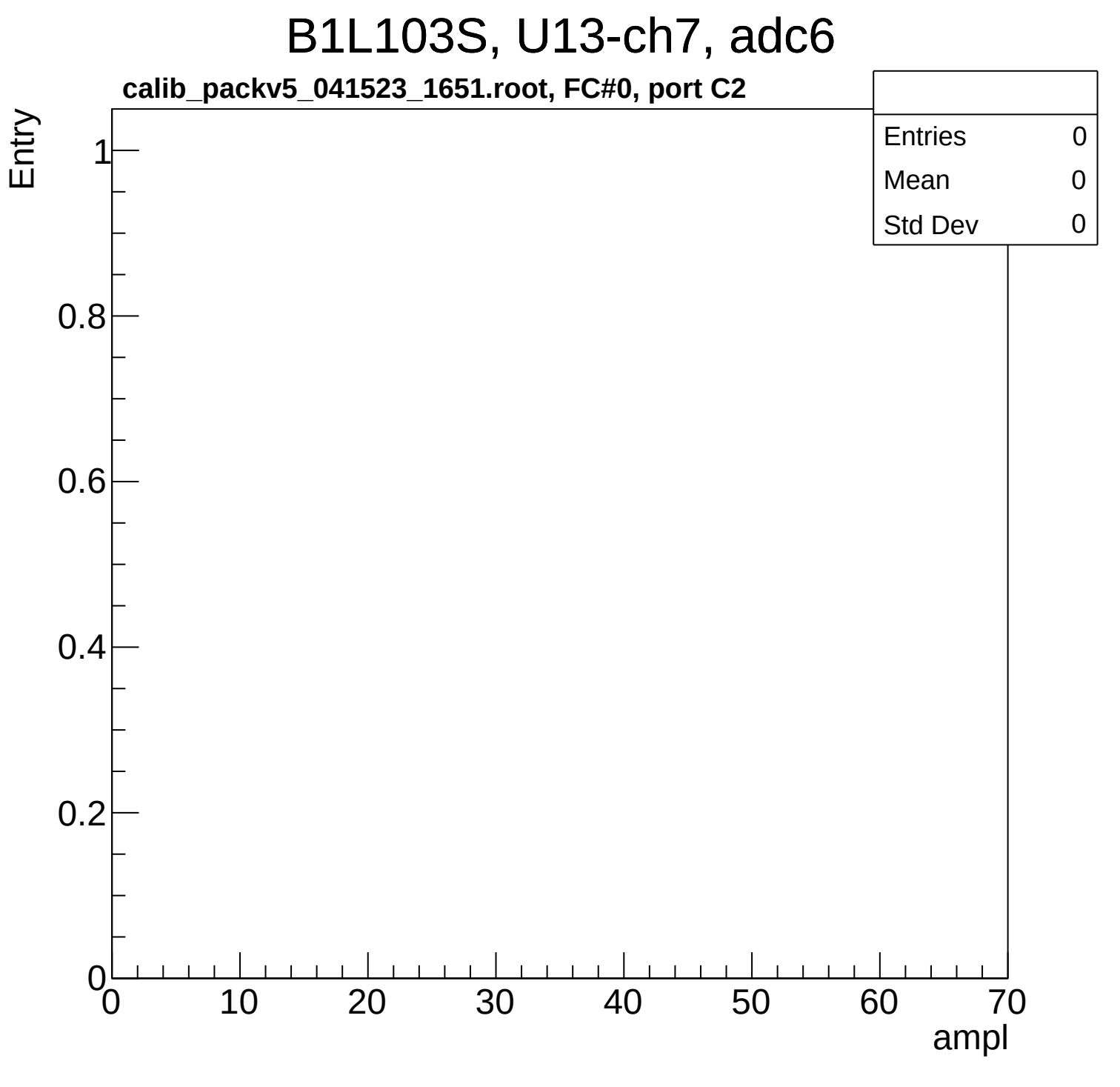
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch7, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.94
Std Dev 8.909
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch7, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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0.8
0.6
0.4
0.2
0
0
10
20
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50
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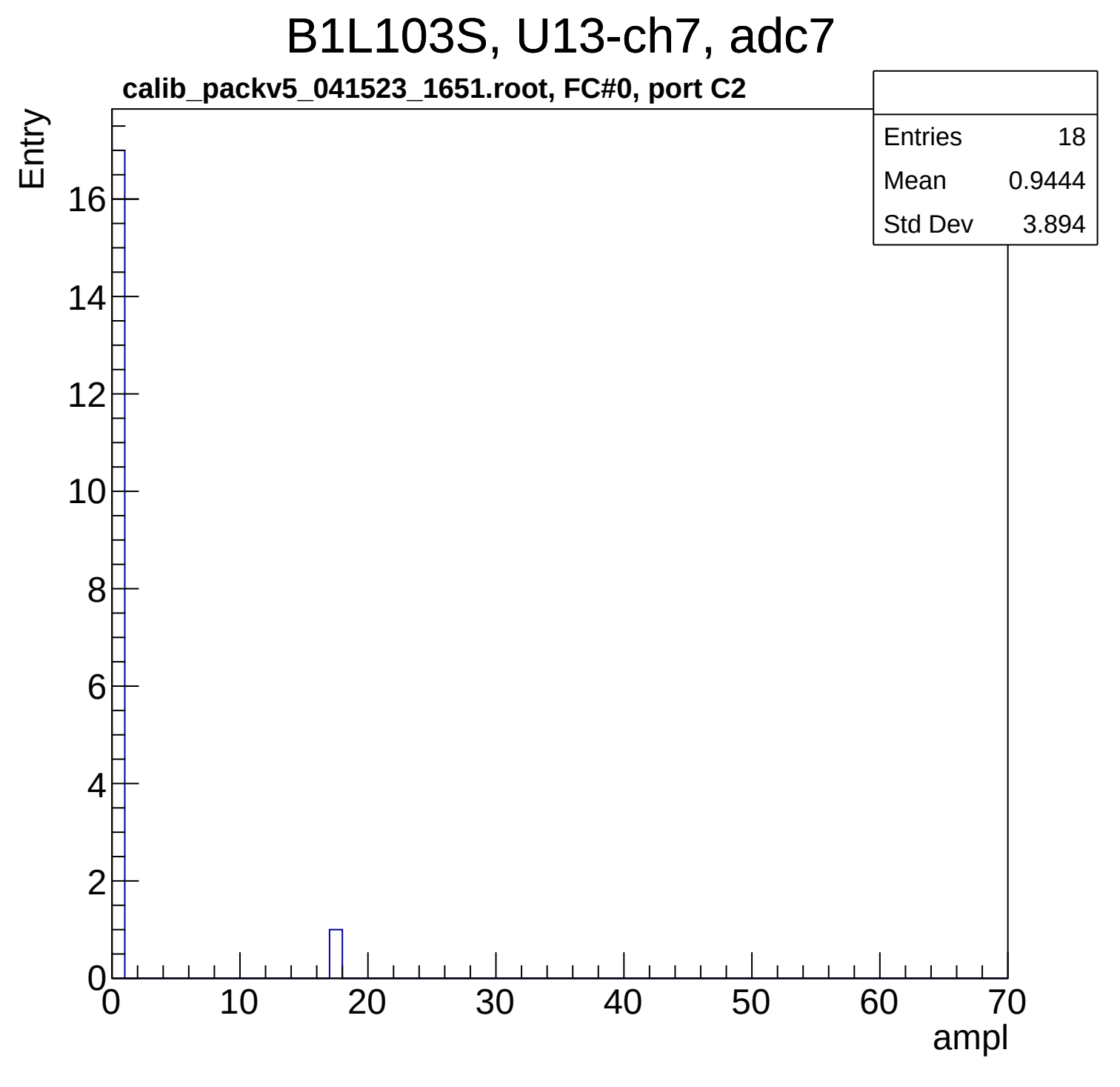
70
ampl


B1L103S, U13-ch7, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0.9444
Std Dev 3.894
Entry
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6
8
10
12
14
16
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10
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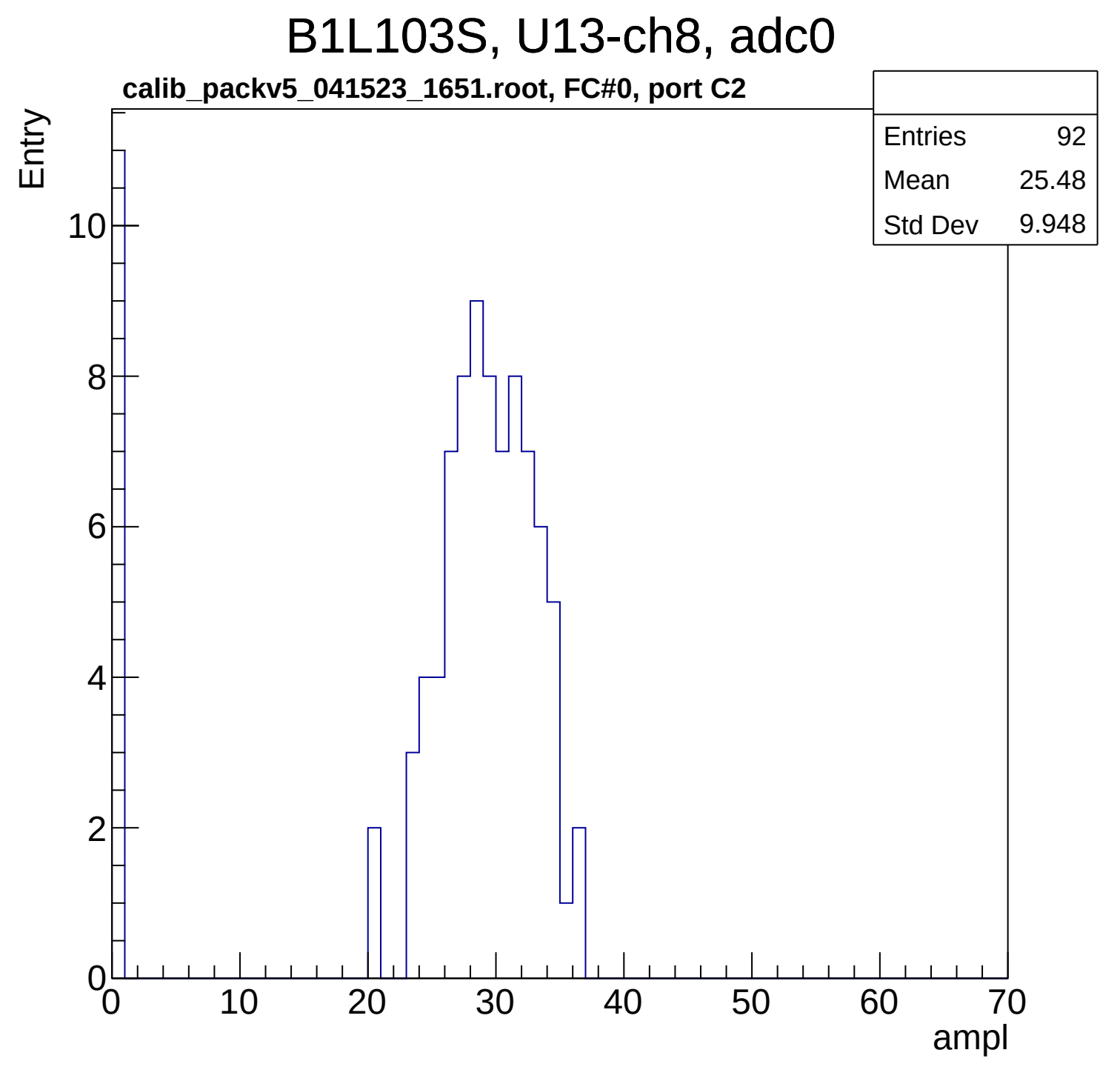
70
ampl


B1L103S, U13-ch8, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 25.48
Std Dev 9.948
Entry
0
2
4
6
8
10
0
10
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50
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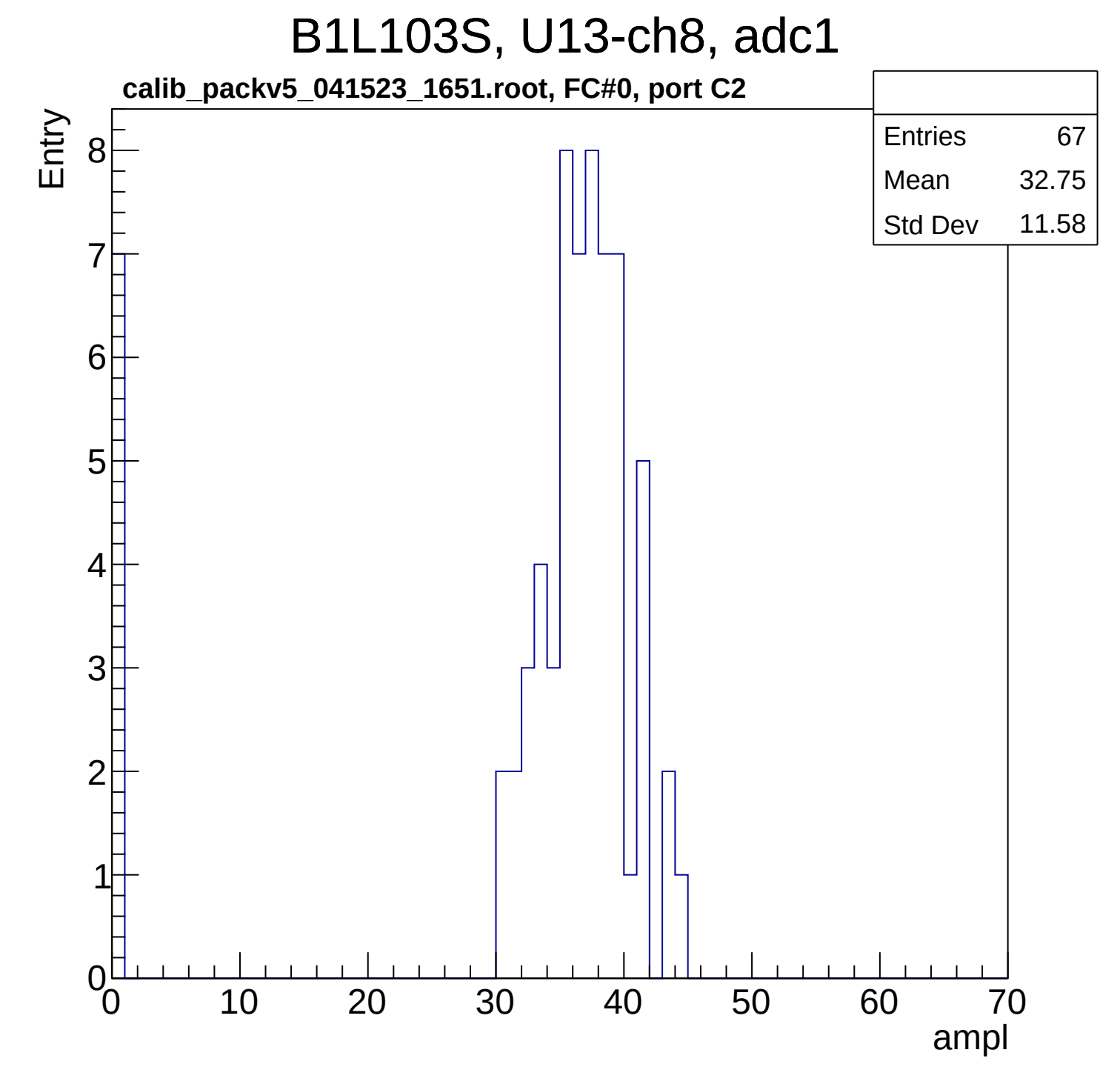
70
ampl


B1L103S, U13-ch8, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 32.75
Std Dev 11.58
Entry
ampl
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1
2
3
4
5
6
7
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0
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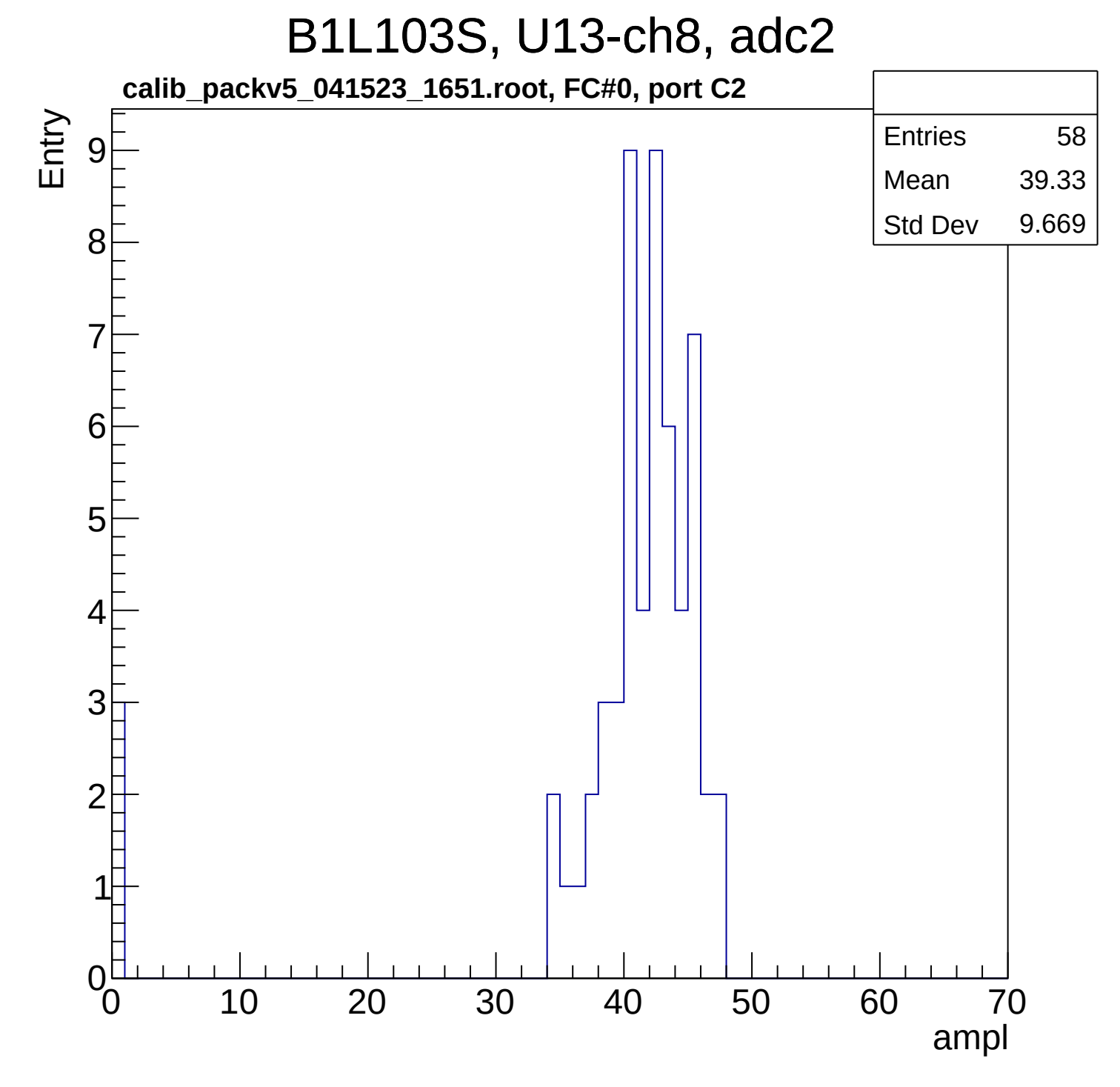
B1L103S, U13-ch8, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 39.33
Std Dev 9.669
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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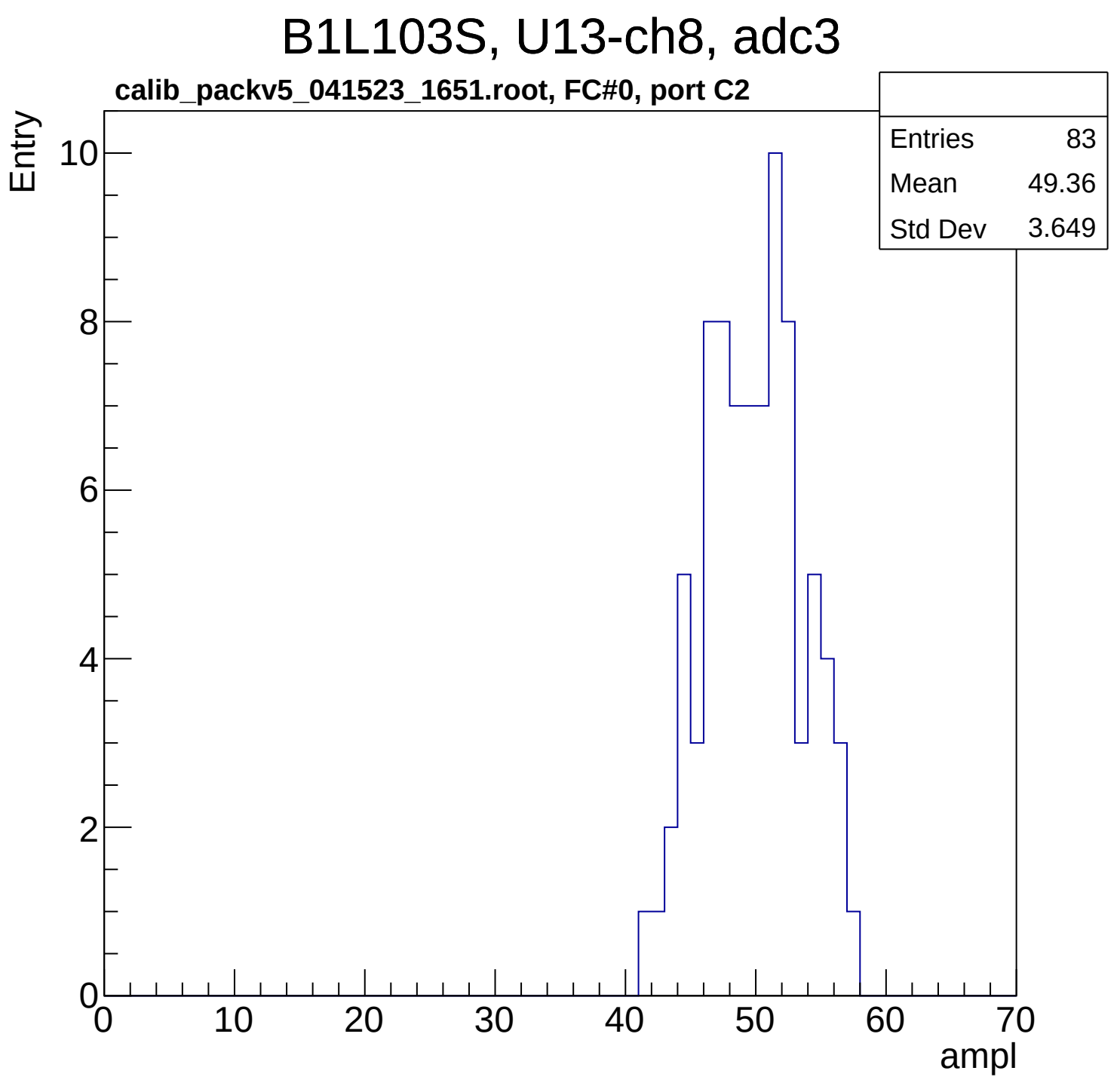
B1L103S, U13-ch8, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 49.36
Std Dev 3.649
Entry
ampl
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10
0
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40
50
60
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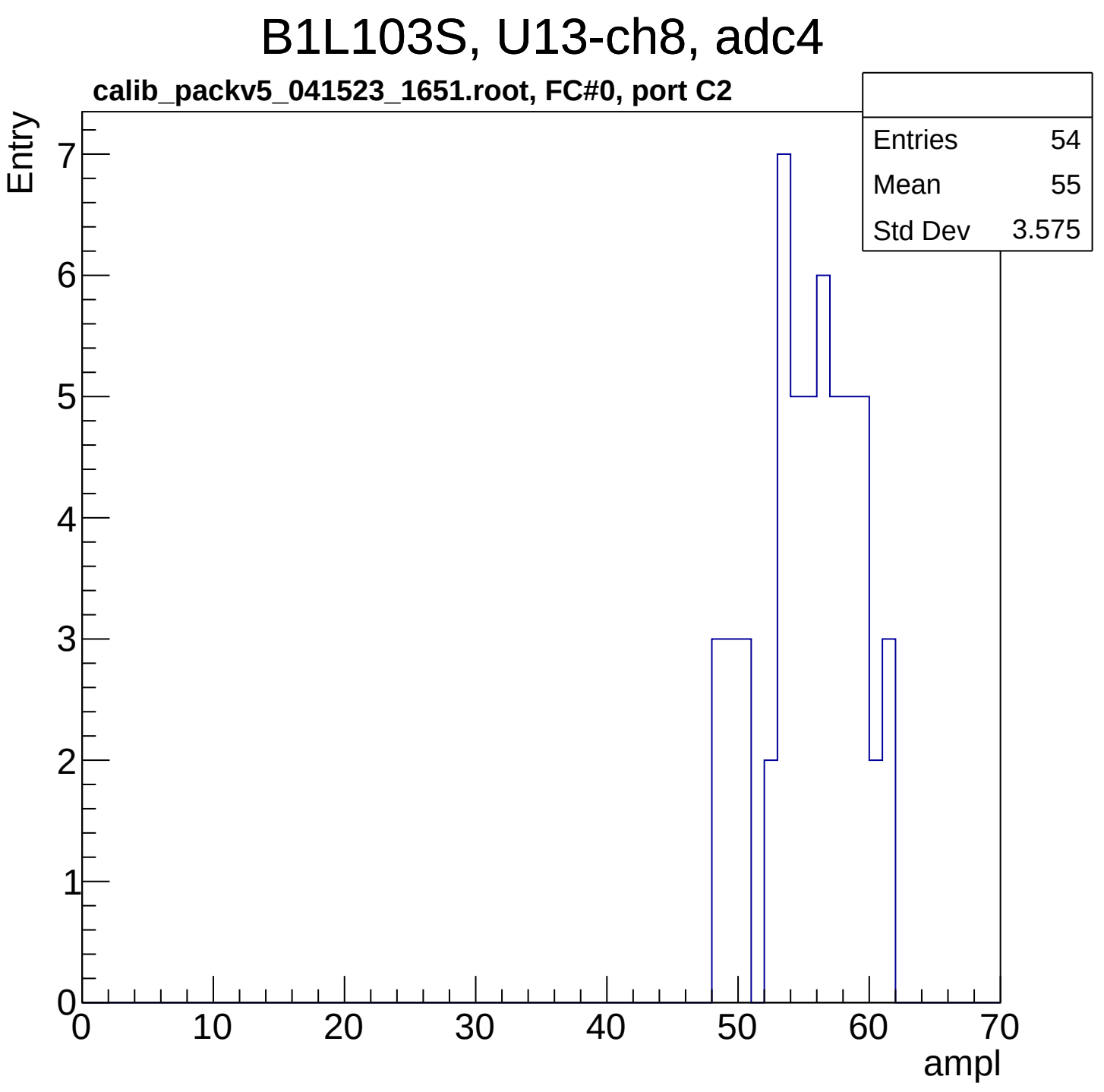
B1L103S, U13-ch8, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 55
Std Dev 3.575
Entry
ampl
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4
5
6
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0
10
20
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40
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60
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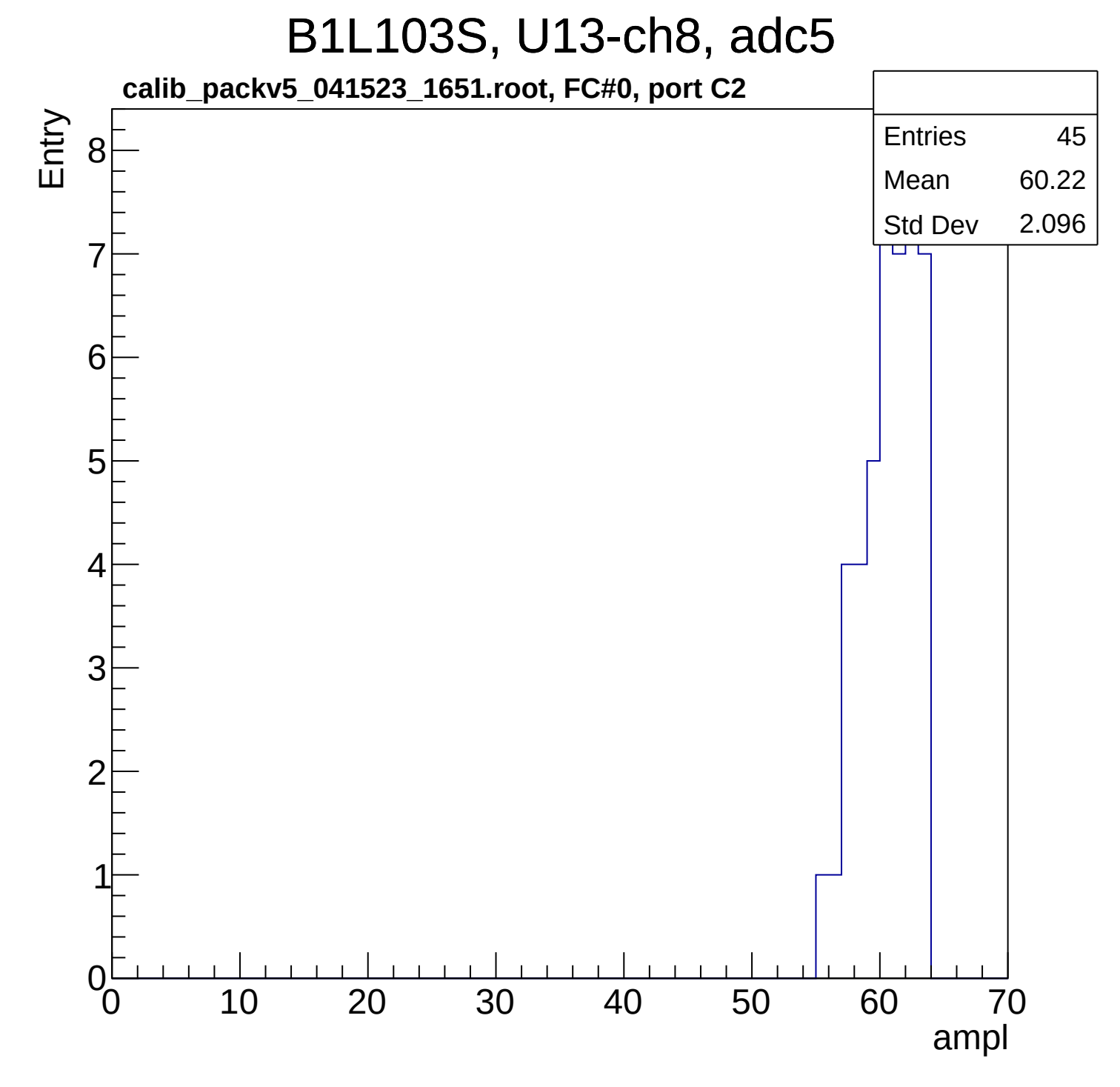
B1L103S, U13-ch8, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 60.22
Std Dev 2.096
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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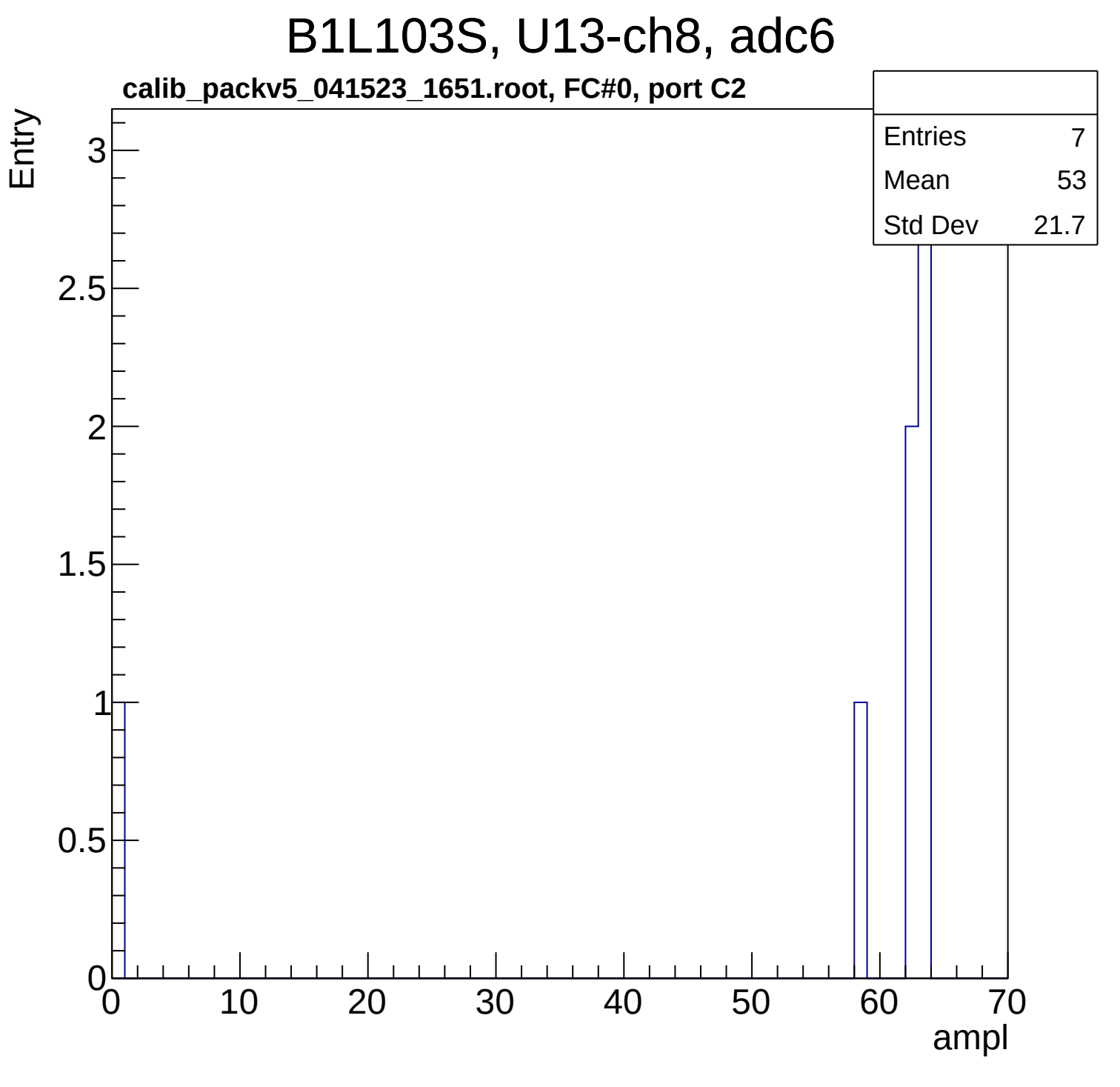
B1L103S, U13-ch8, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 53
Std Dev 21.7
Entry
ampl
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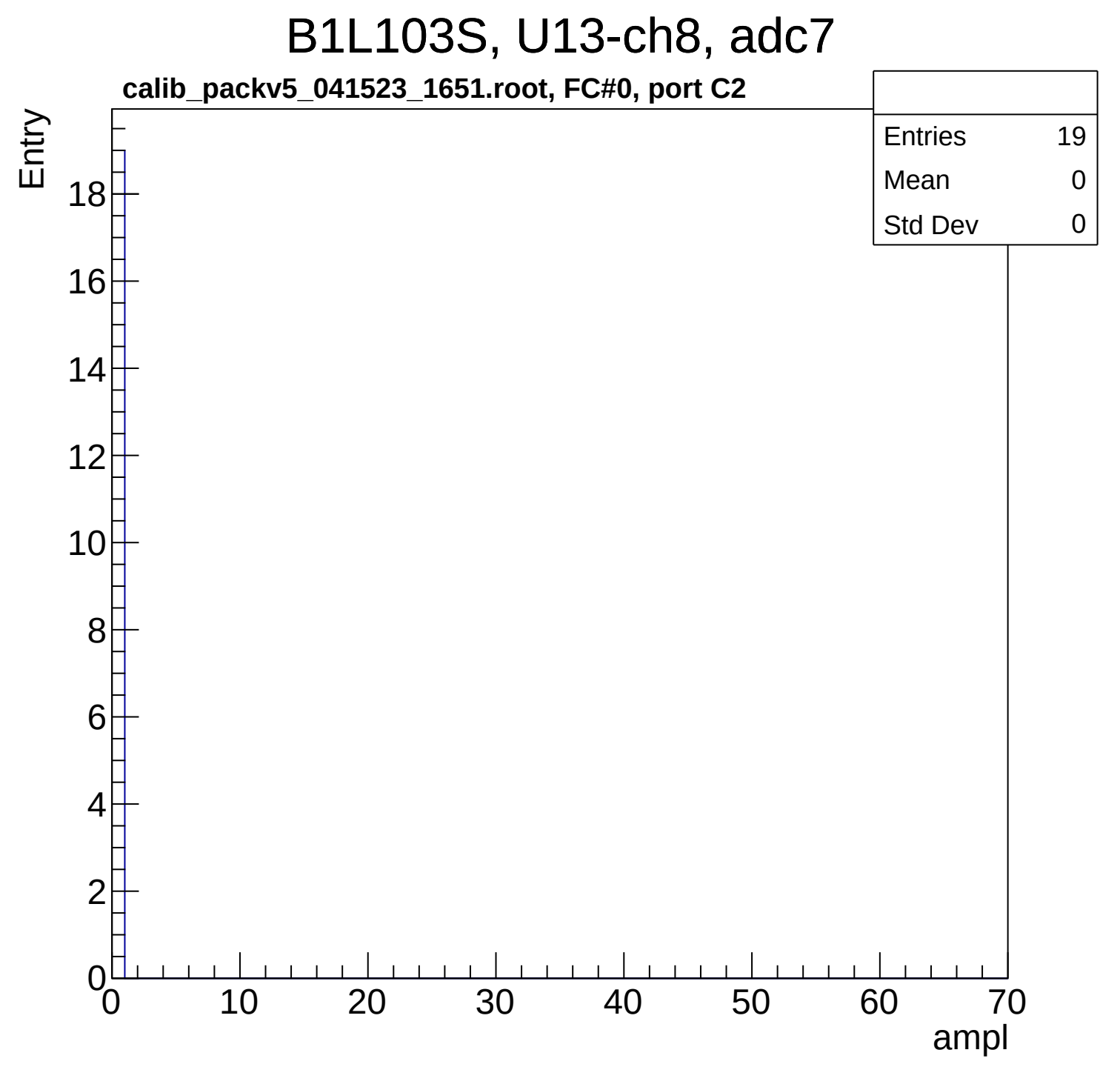
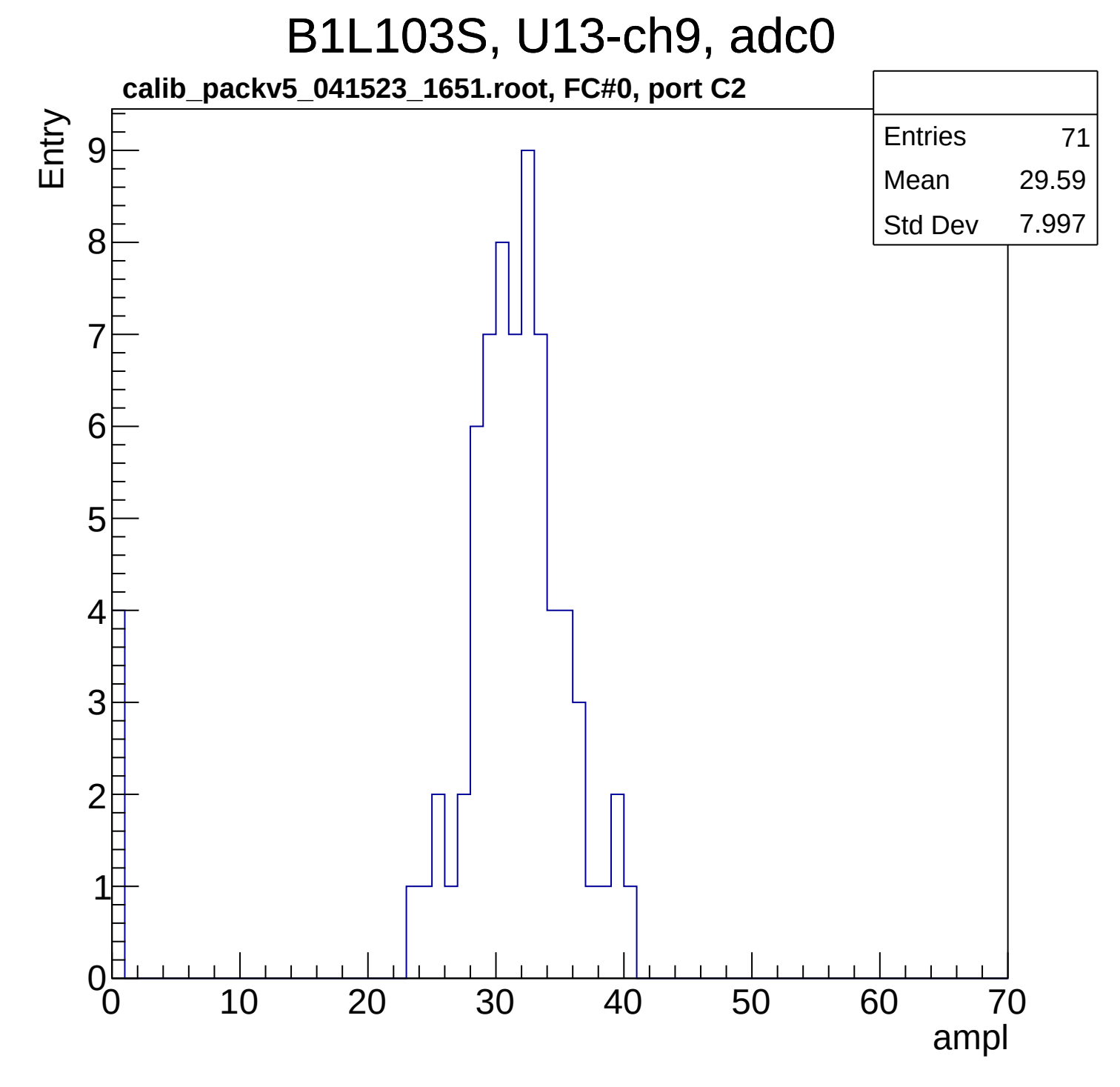
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U13-ch8, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch9, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 29.59
Std Dev 7.997
Entry
ampl
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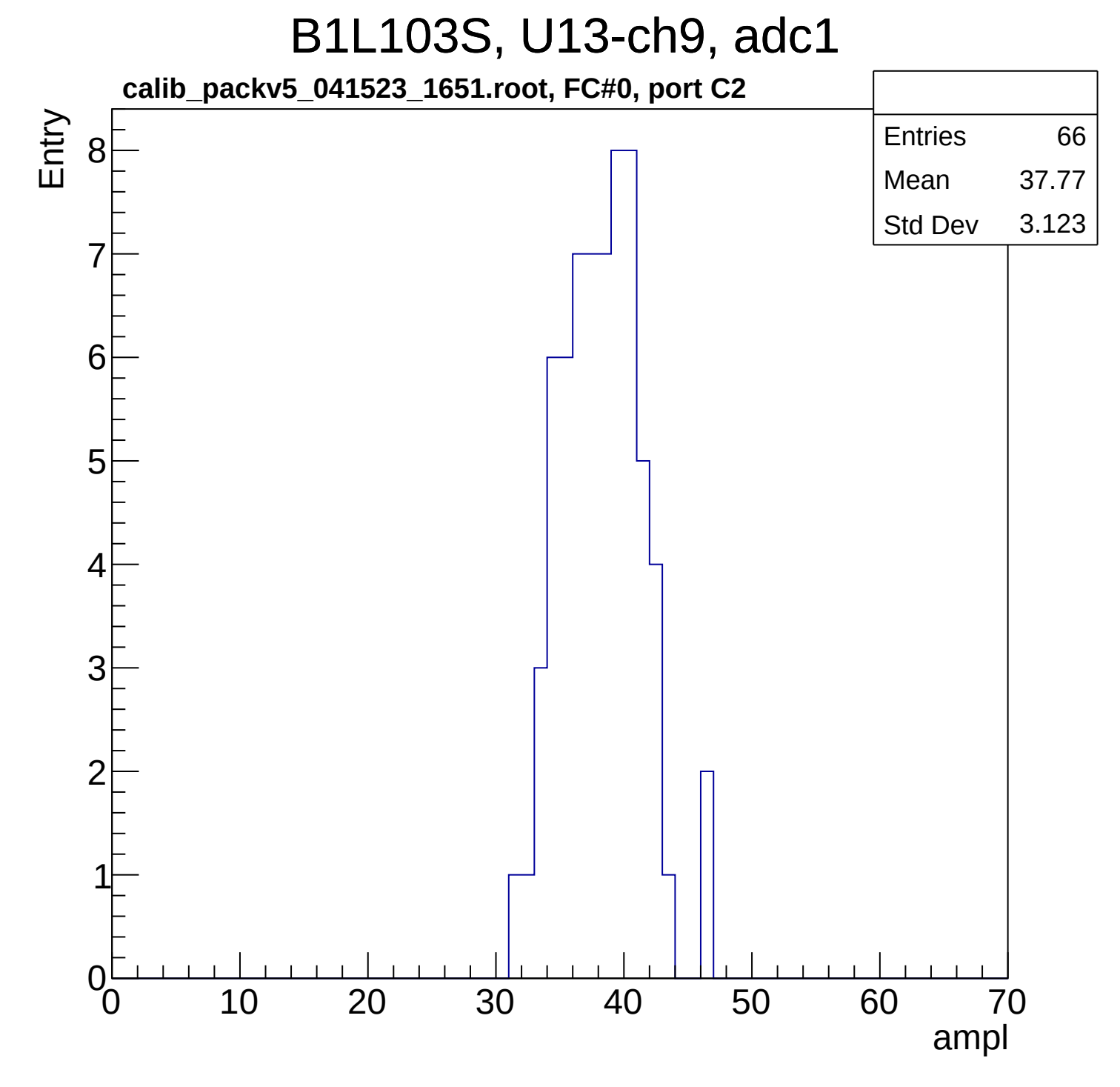
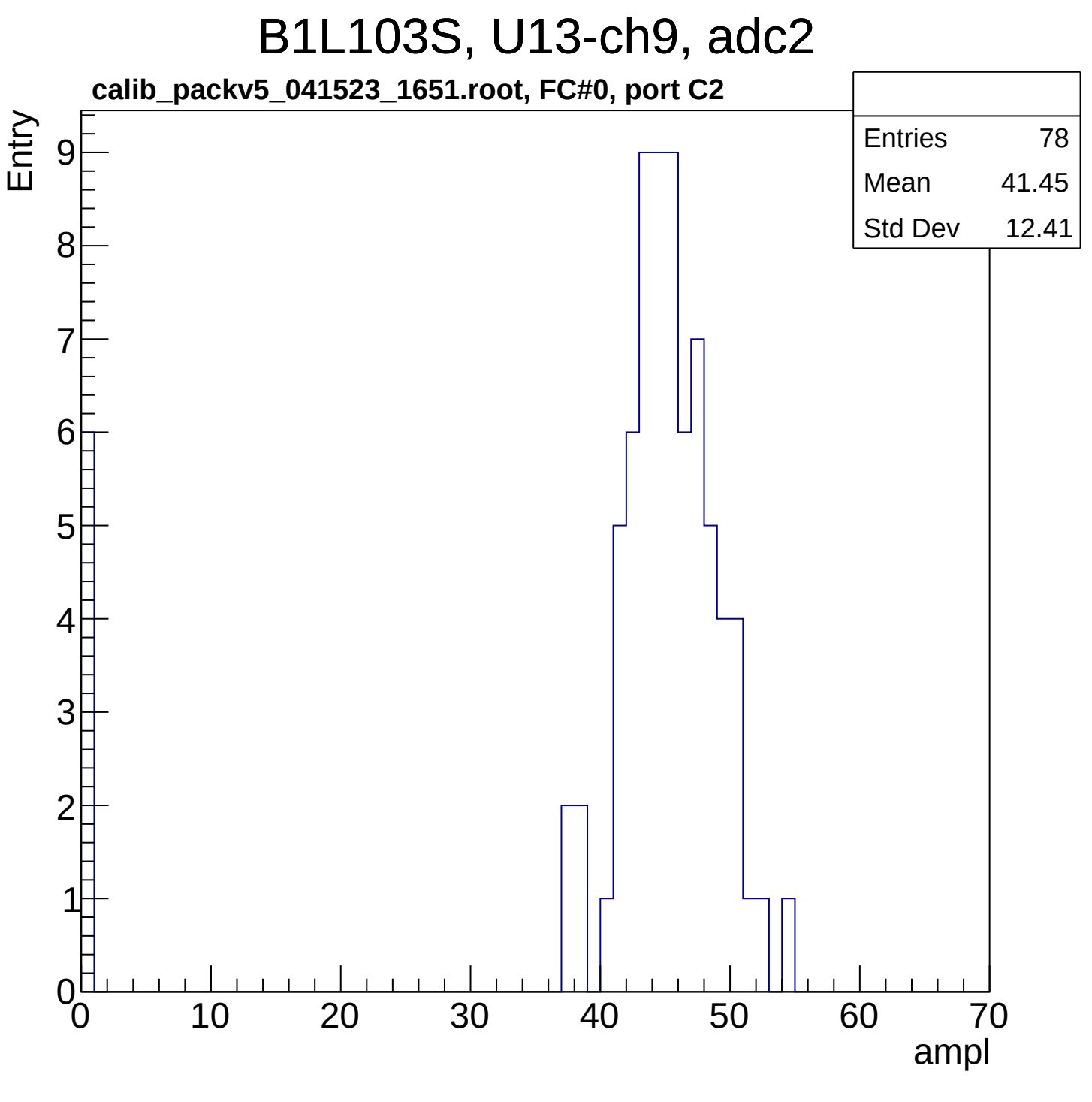
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch9, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 37.77
Std Dev 3.123
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch9, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 41.45
Std Dev 12.41
Entry
ampl
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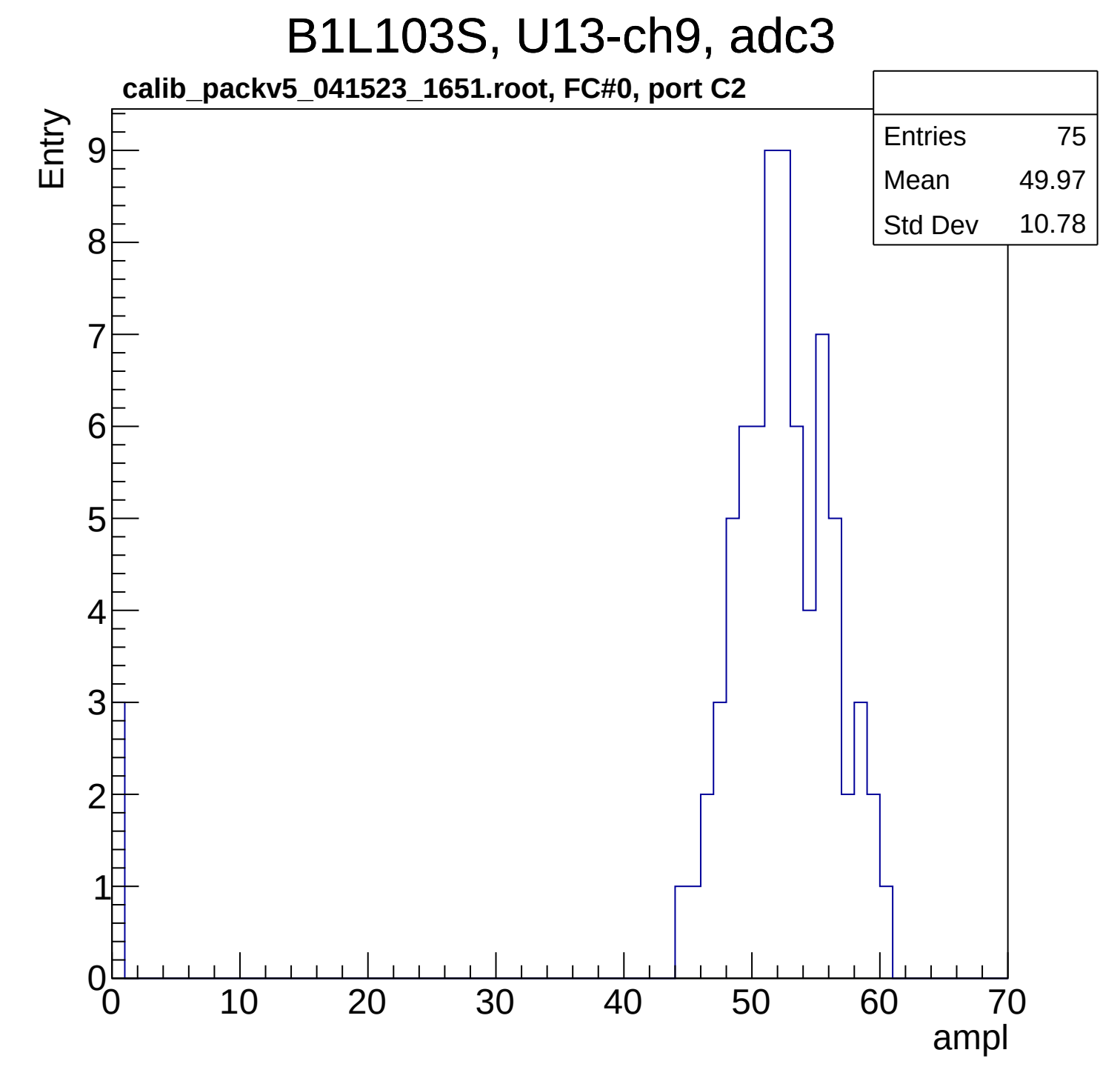
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch9, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 49.97
Std Dev 10.78
Entry
ampl
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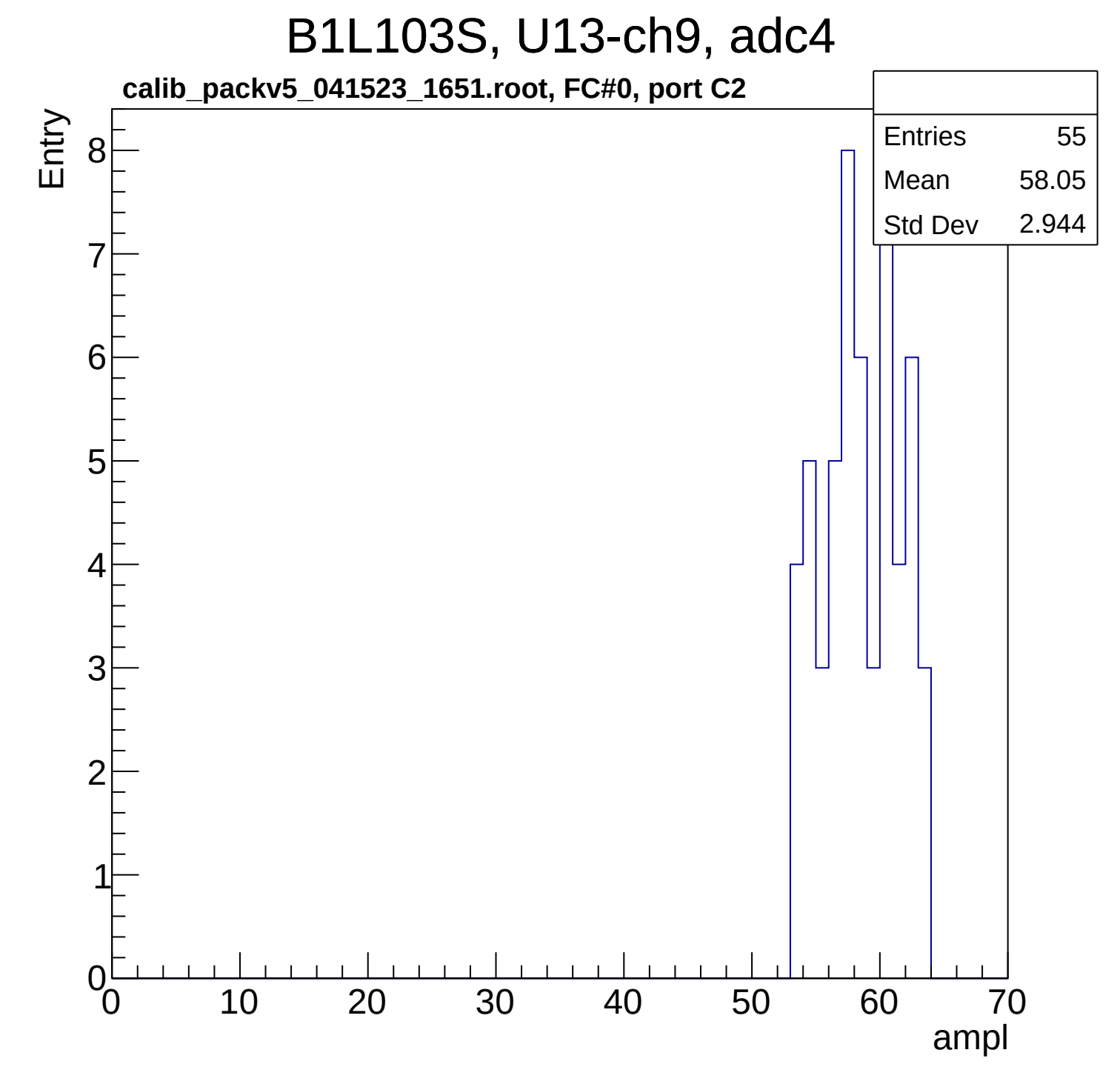
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch9, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.05
Std Dev 2.944
Entry
ampl
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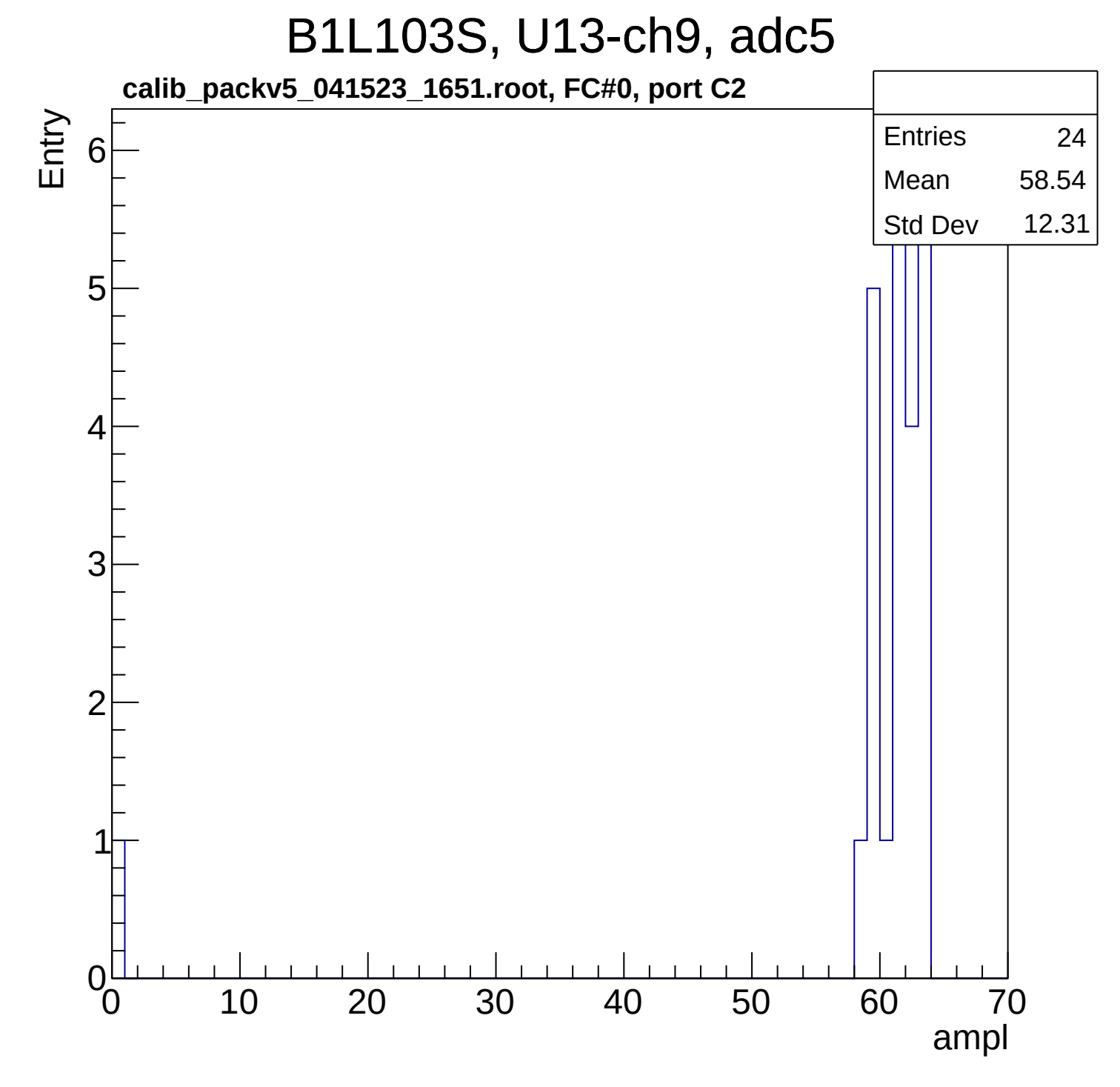
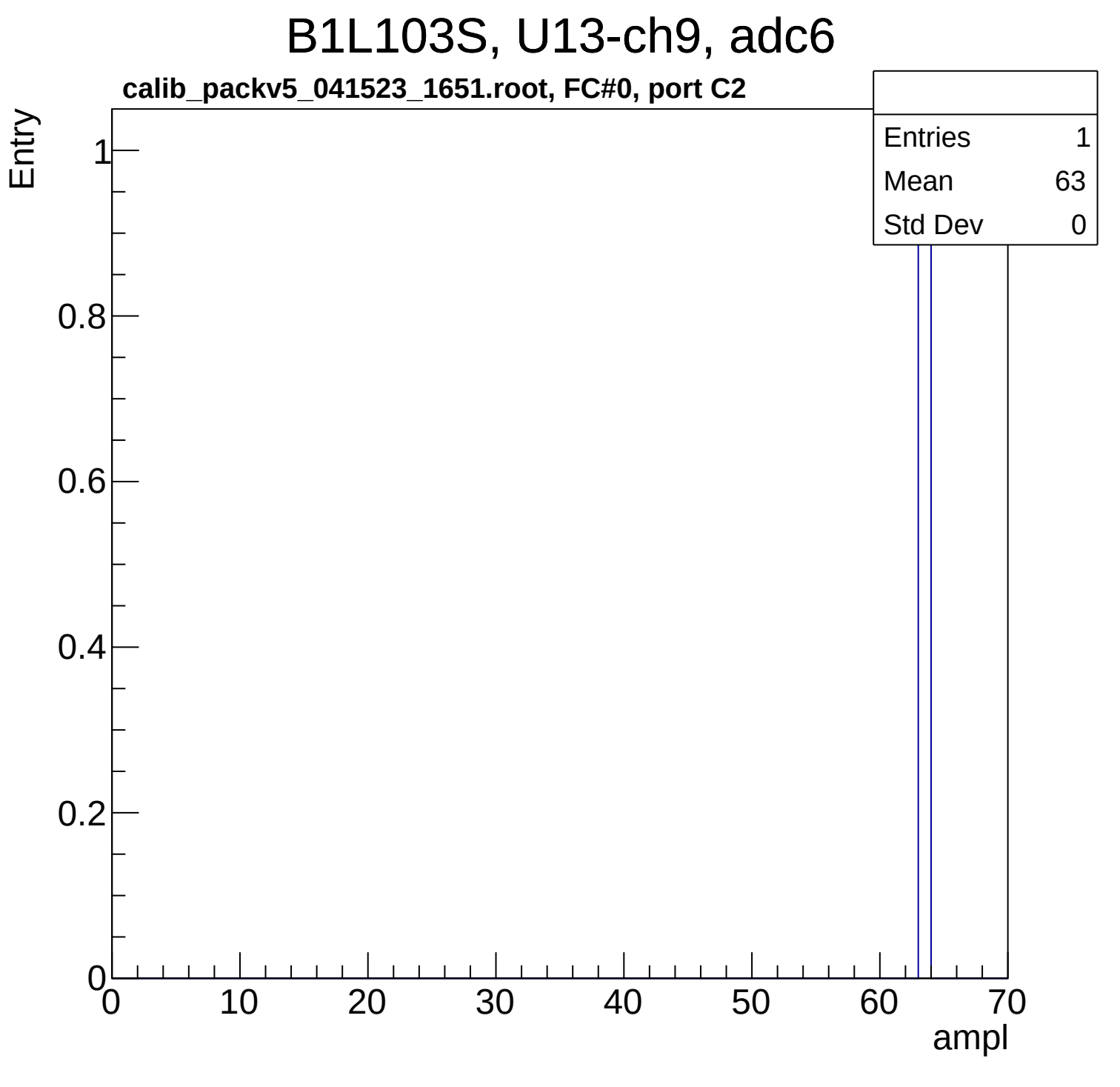
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch9, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 58.54
Std Dev 12.31
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U13-ch9, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 63
Std Dev 0
Entry
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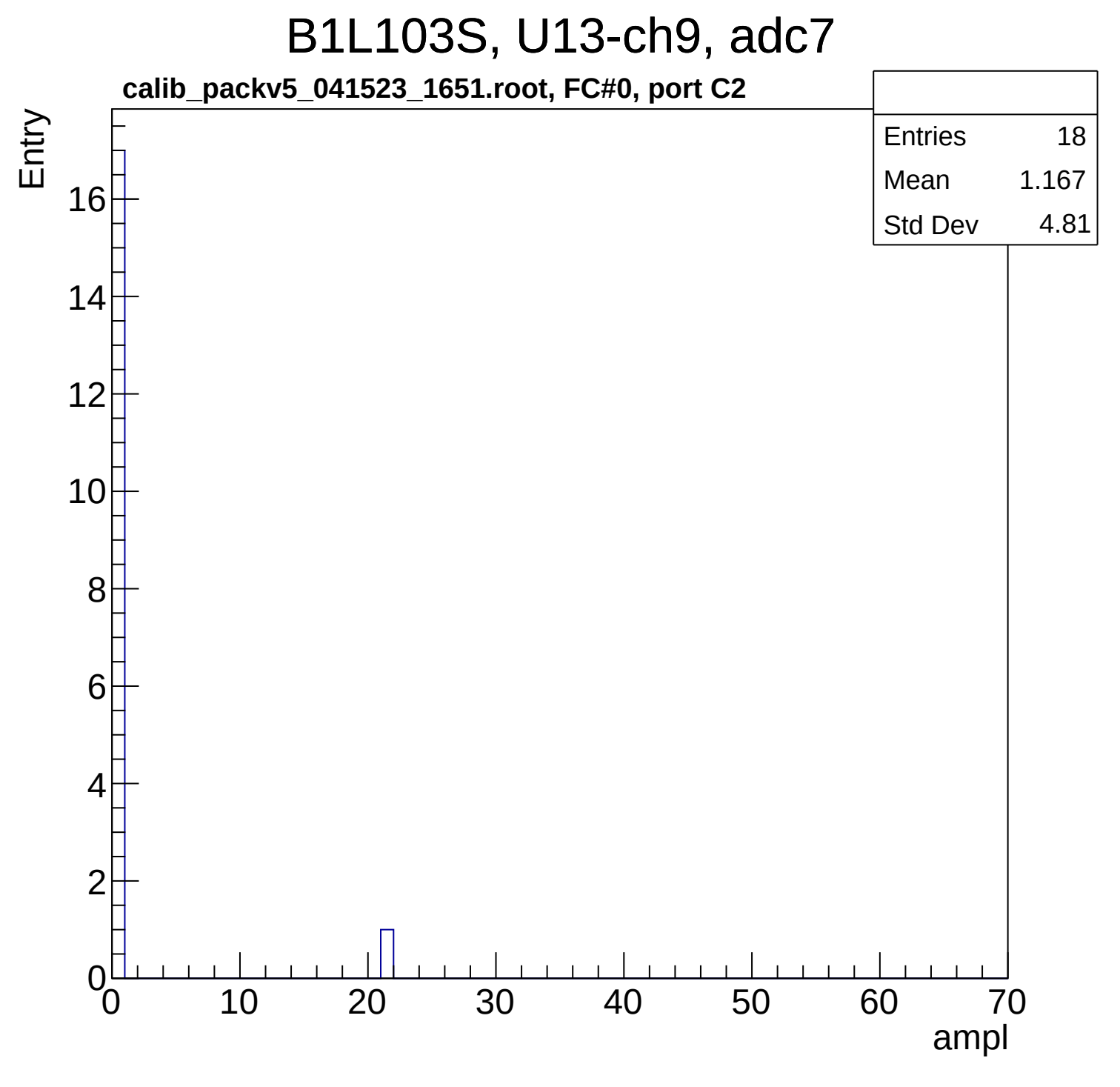
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch9, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.167
Std Dev 4.81
Entry
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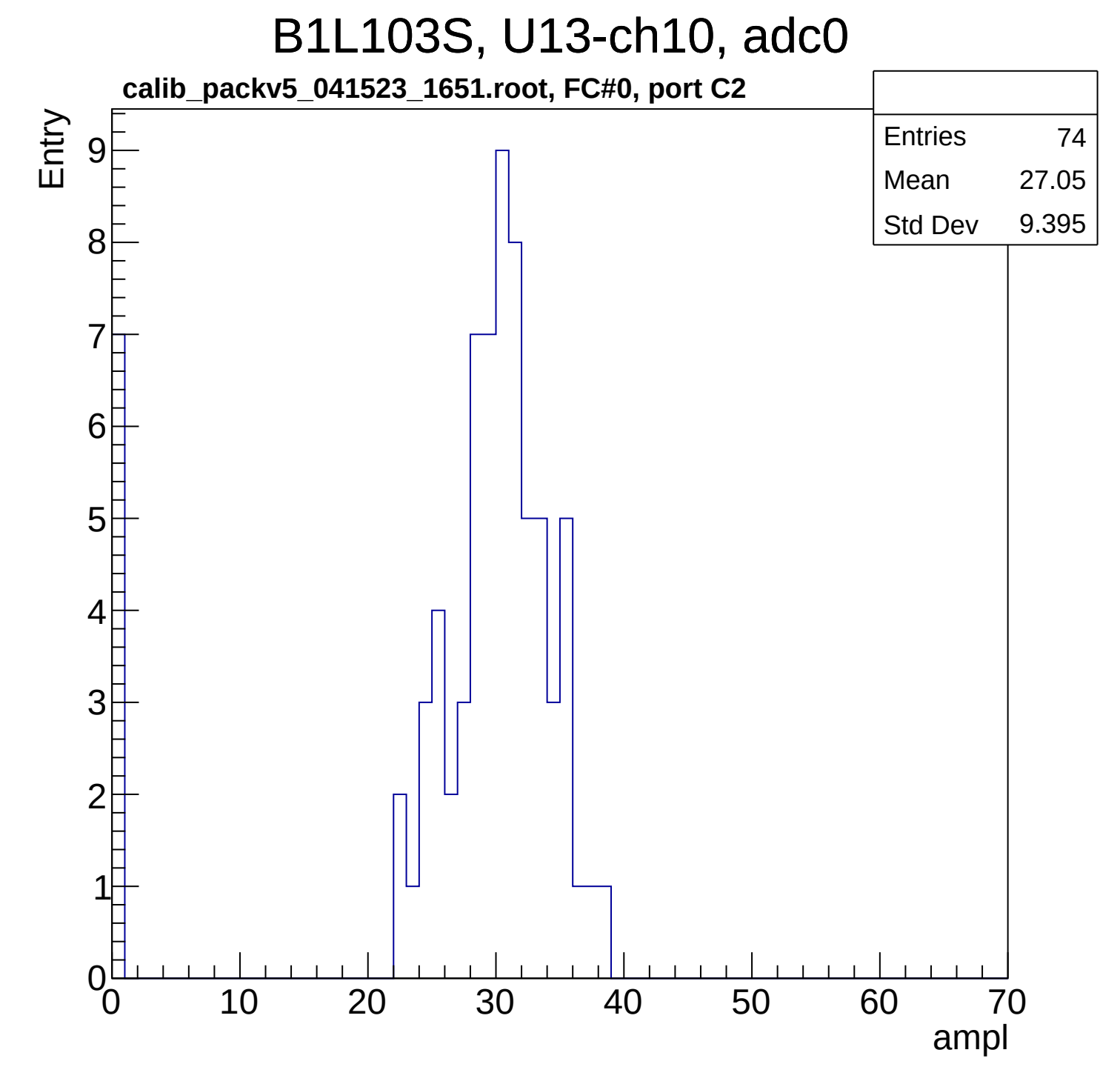
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch10, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 27.05
Std Dev 9.395
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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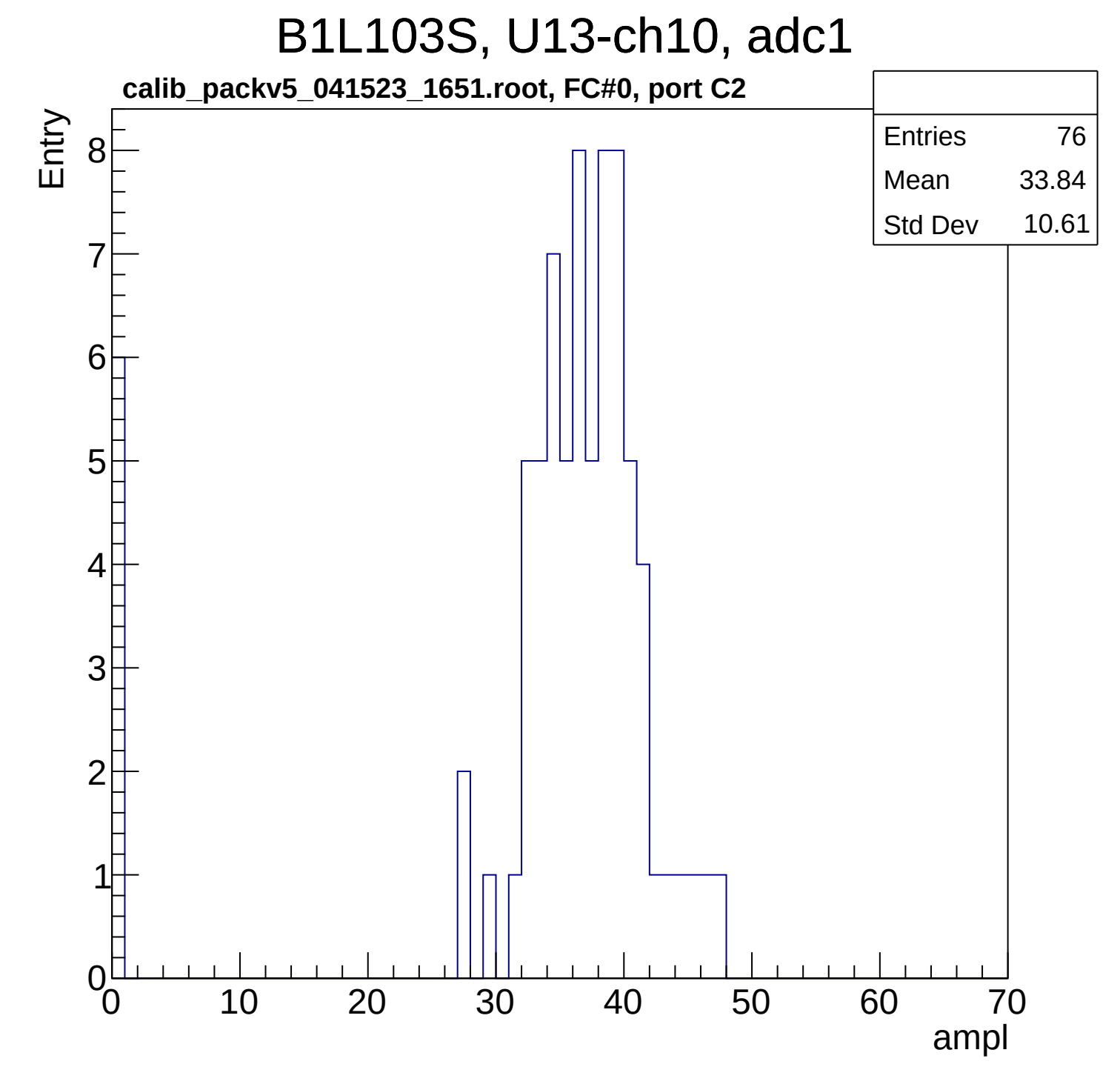
40
50
60
70


B1L103S, U13-ch10, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 33.84
Std Dev 10.61
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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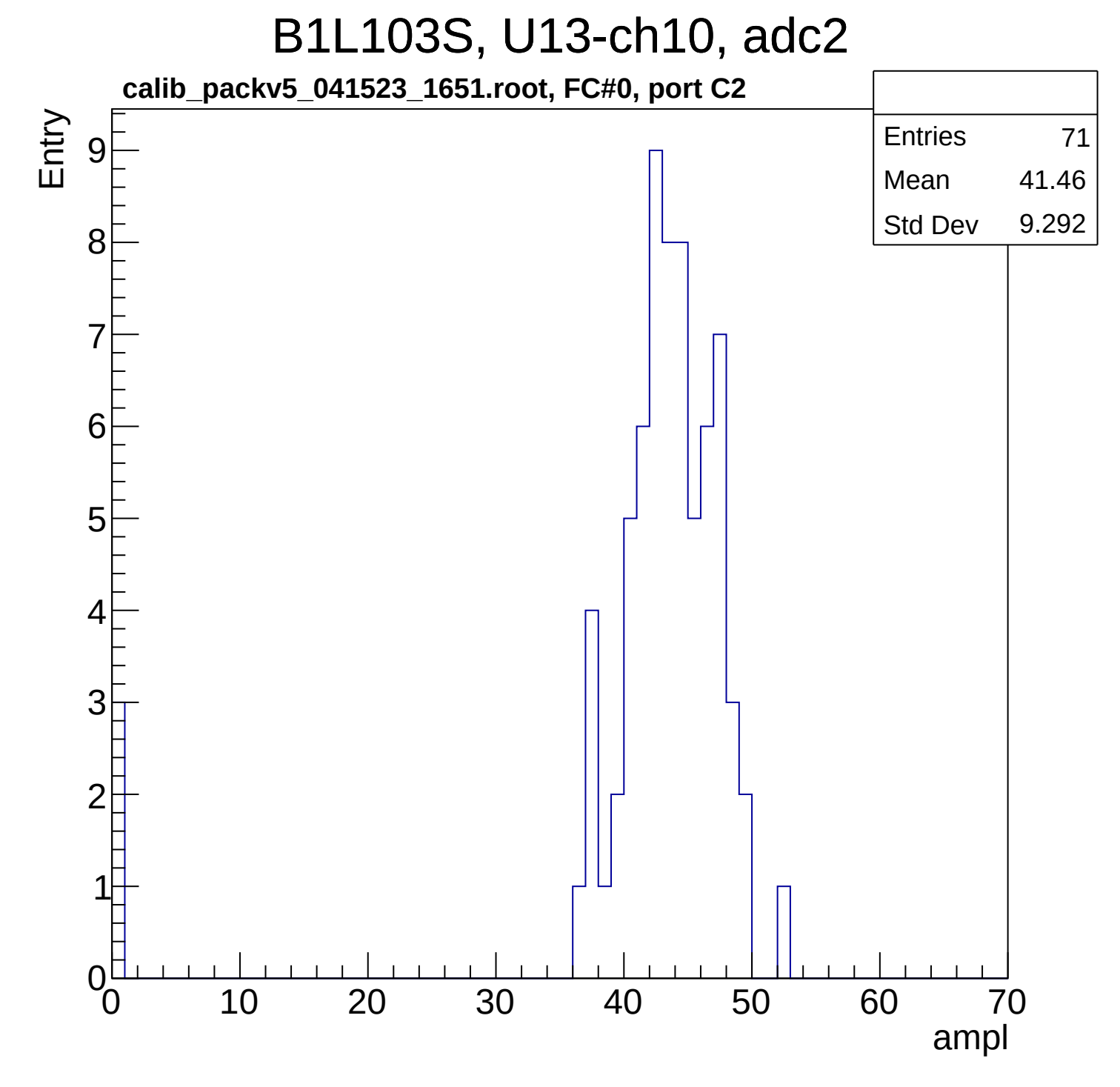
B1L103S, U13-ch10, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 41.46
Std Dev 9.292
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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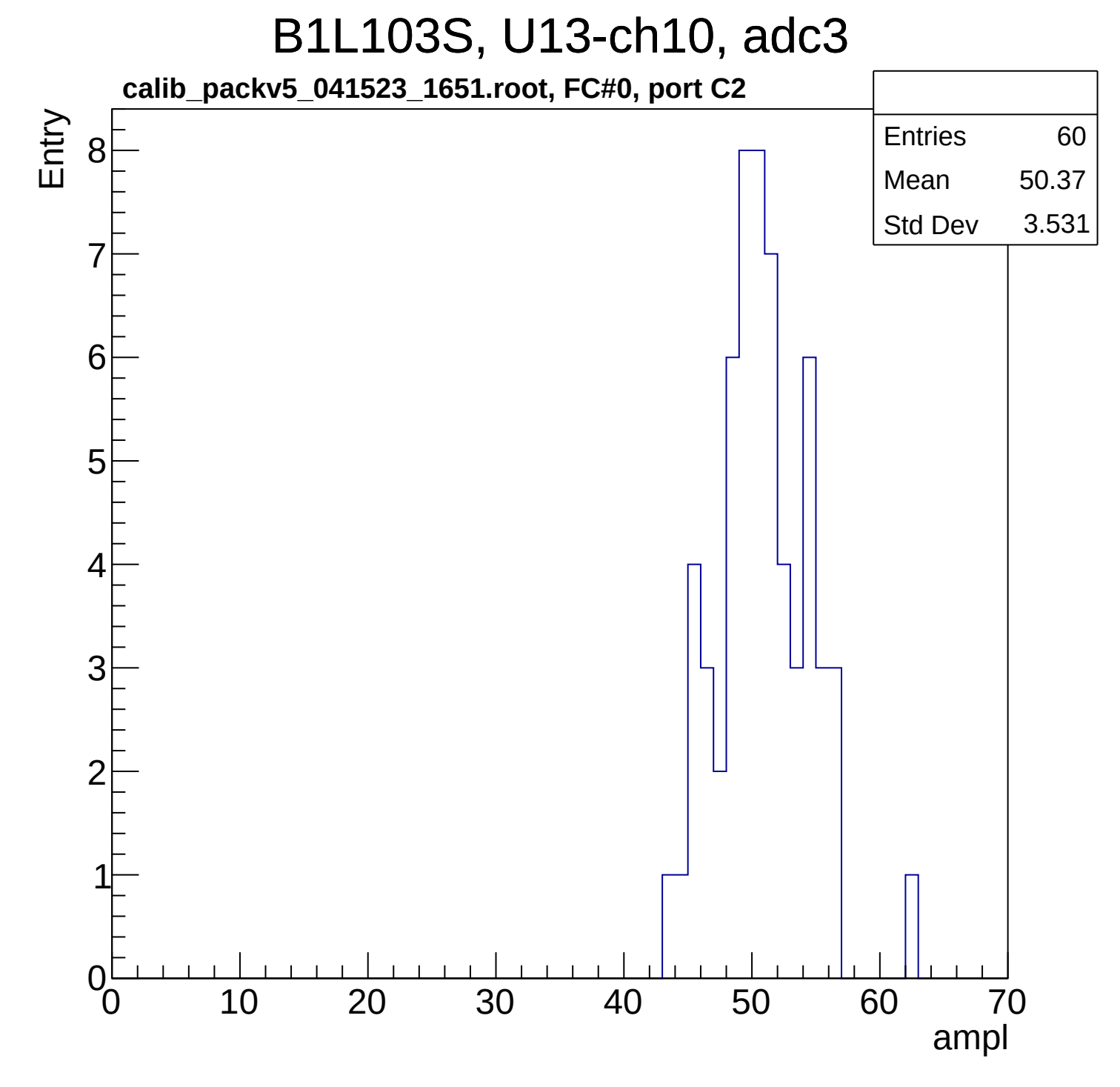
B1L103S, U13-ch10, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 50.37
Std Dev 3.531
Entry
ampl
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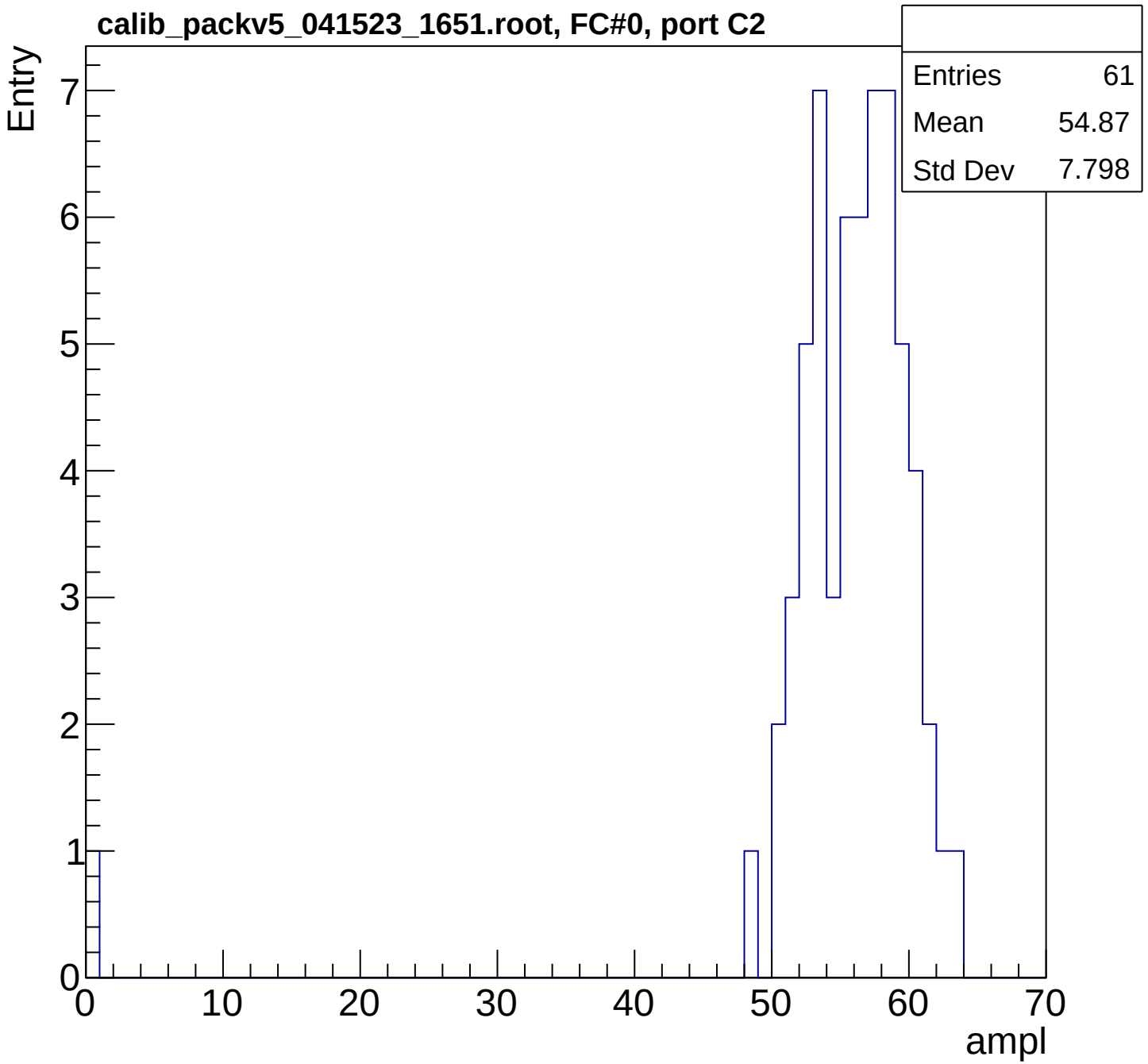
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch10, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 54.87
Std Dev 7.798
Entry
ampl
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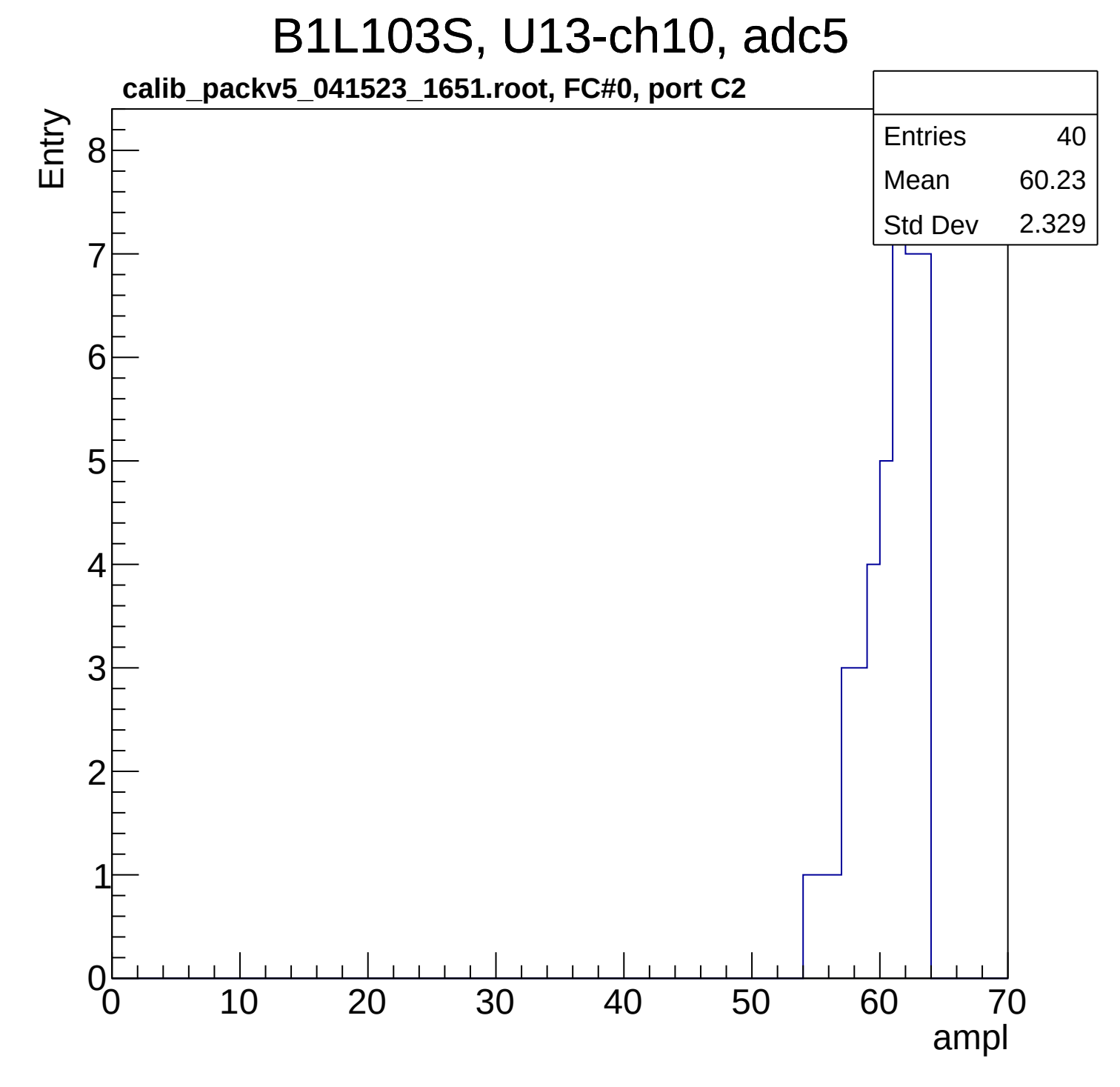
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch10, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 60.23
Std Dev 2.329
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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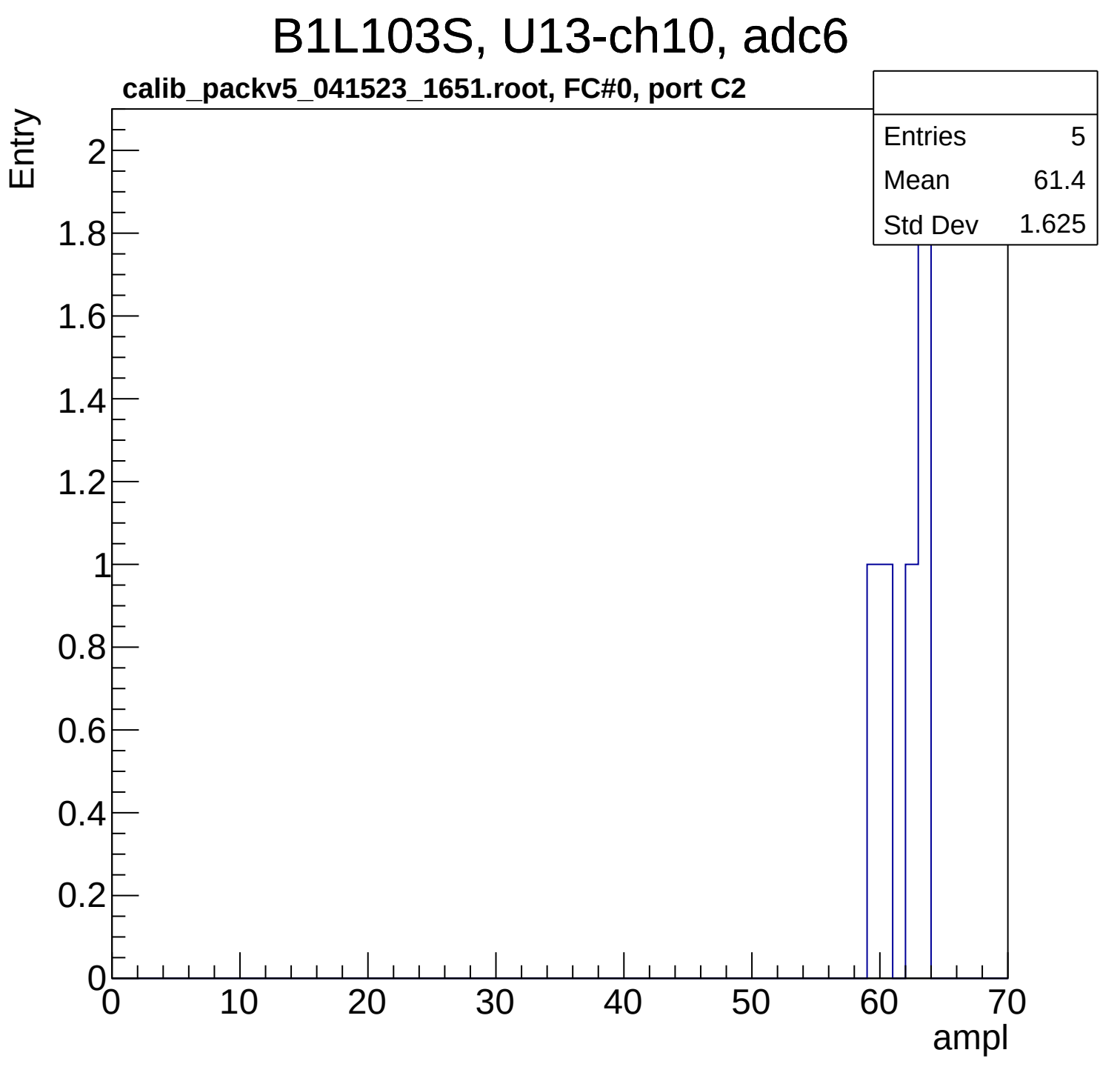
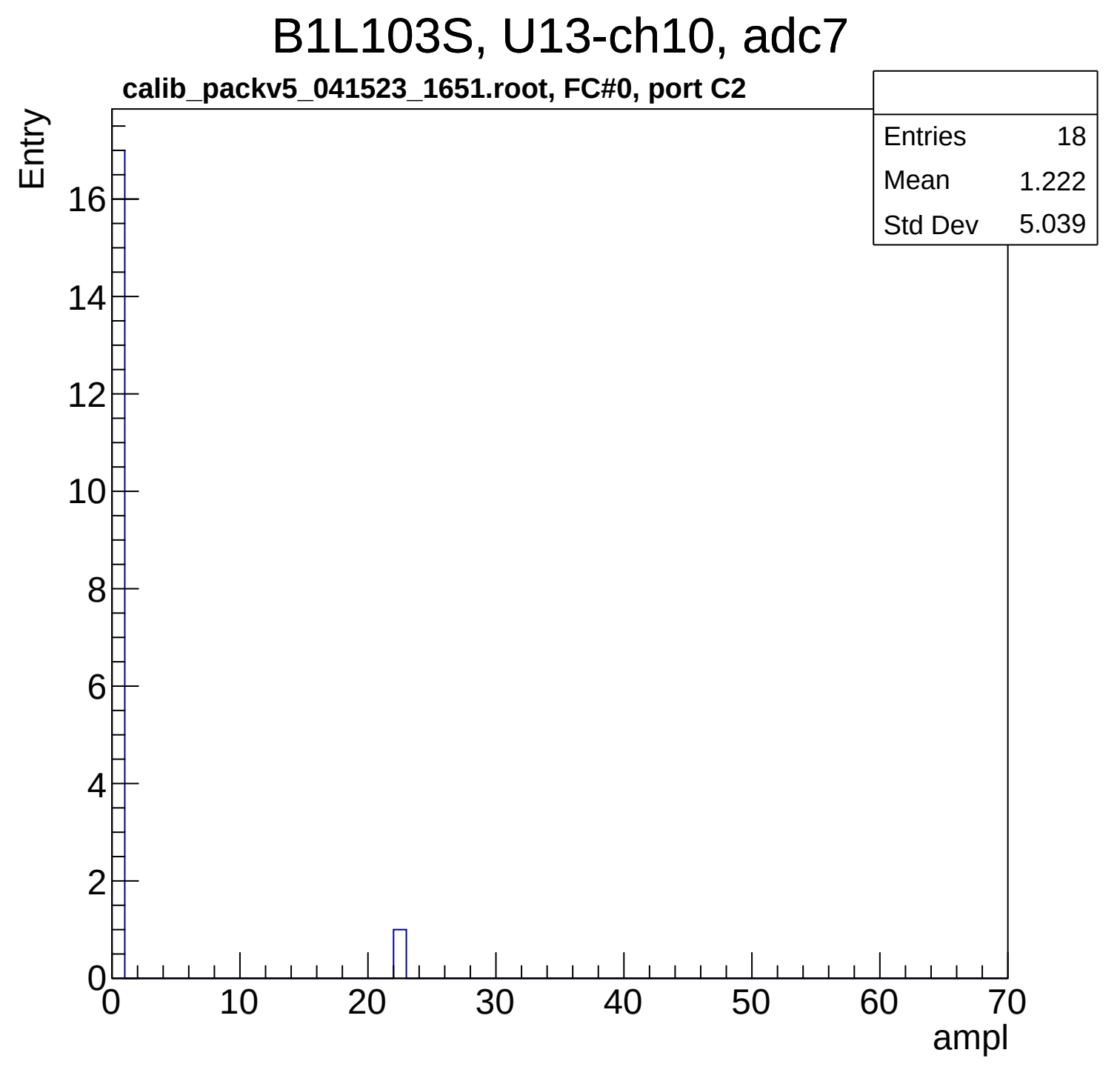
60
70


B1L103S, U13-ch10, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.4
Std Dev 1.625
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U13-ch10, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.222
Std Dev 5.039
Entry
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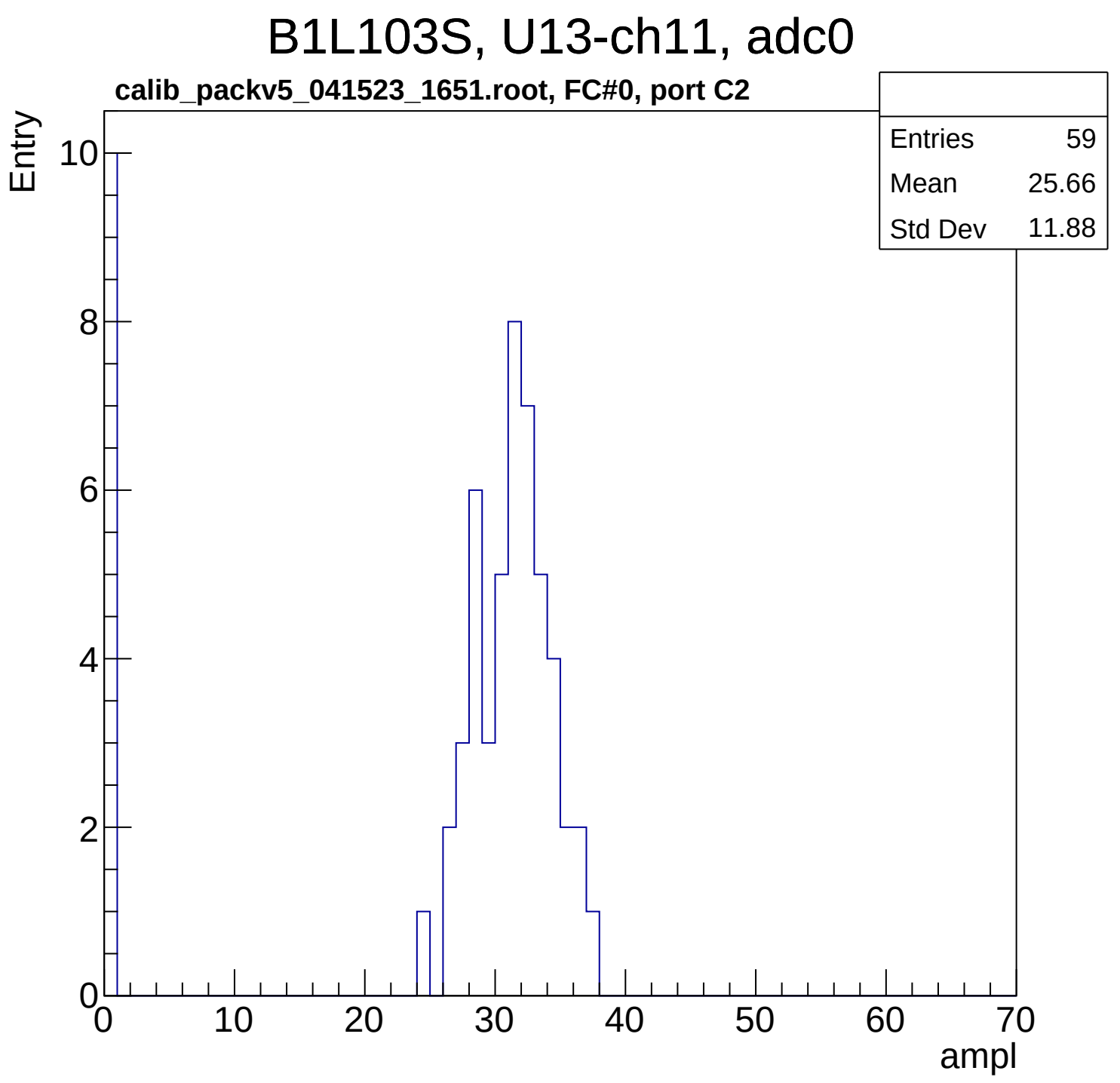
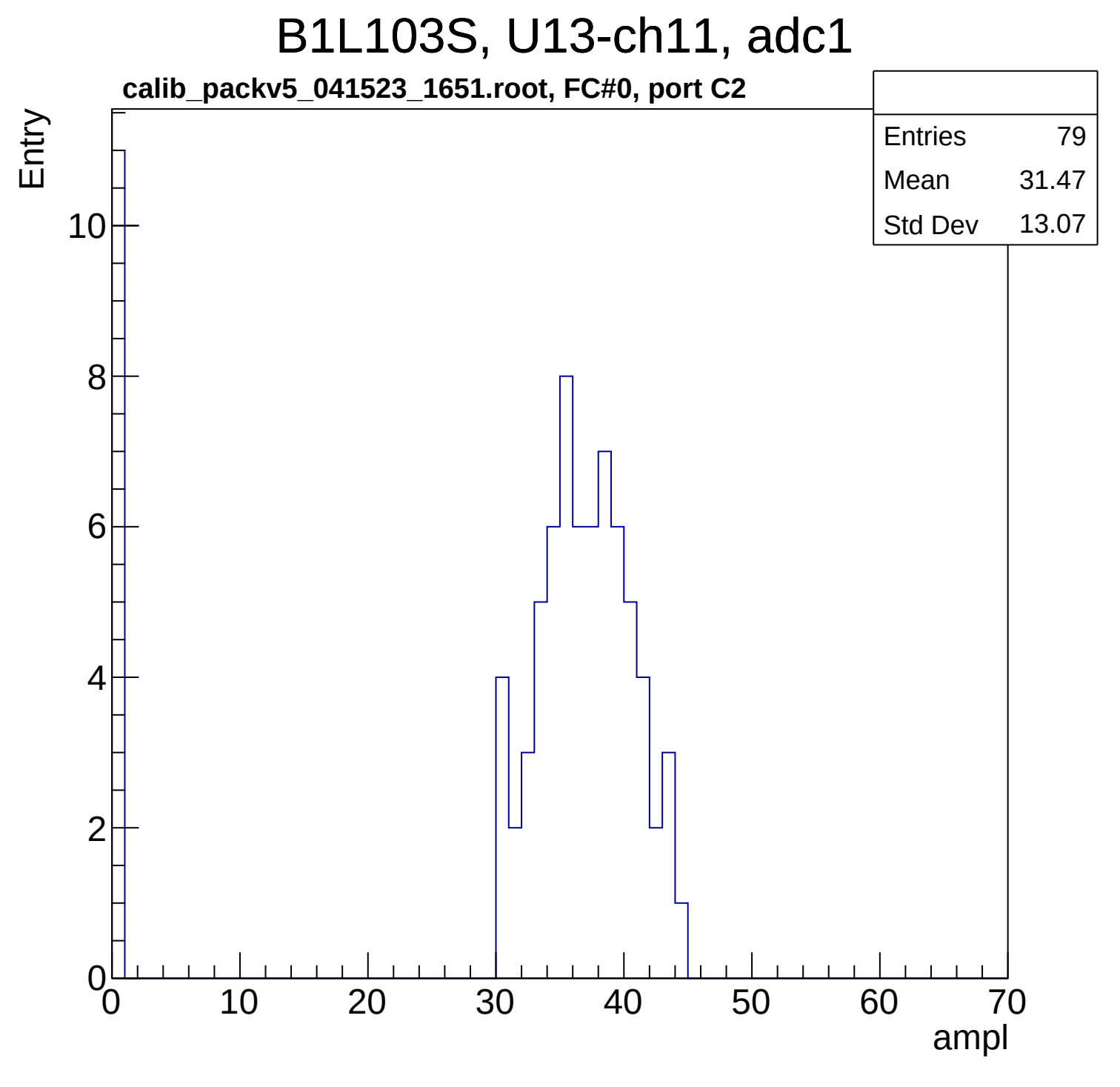
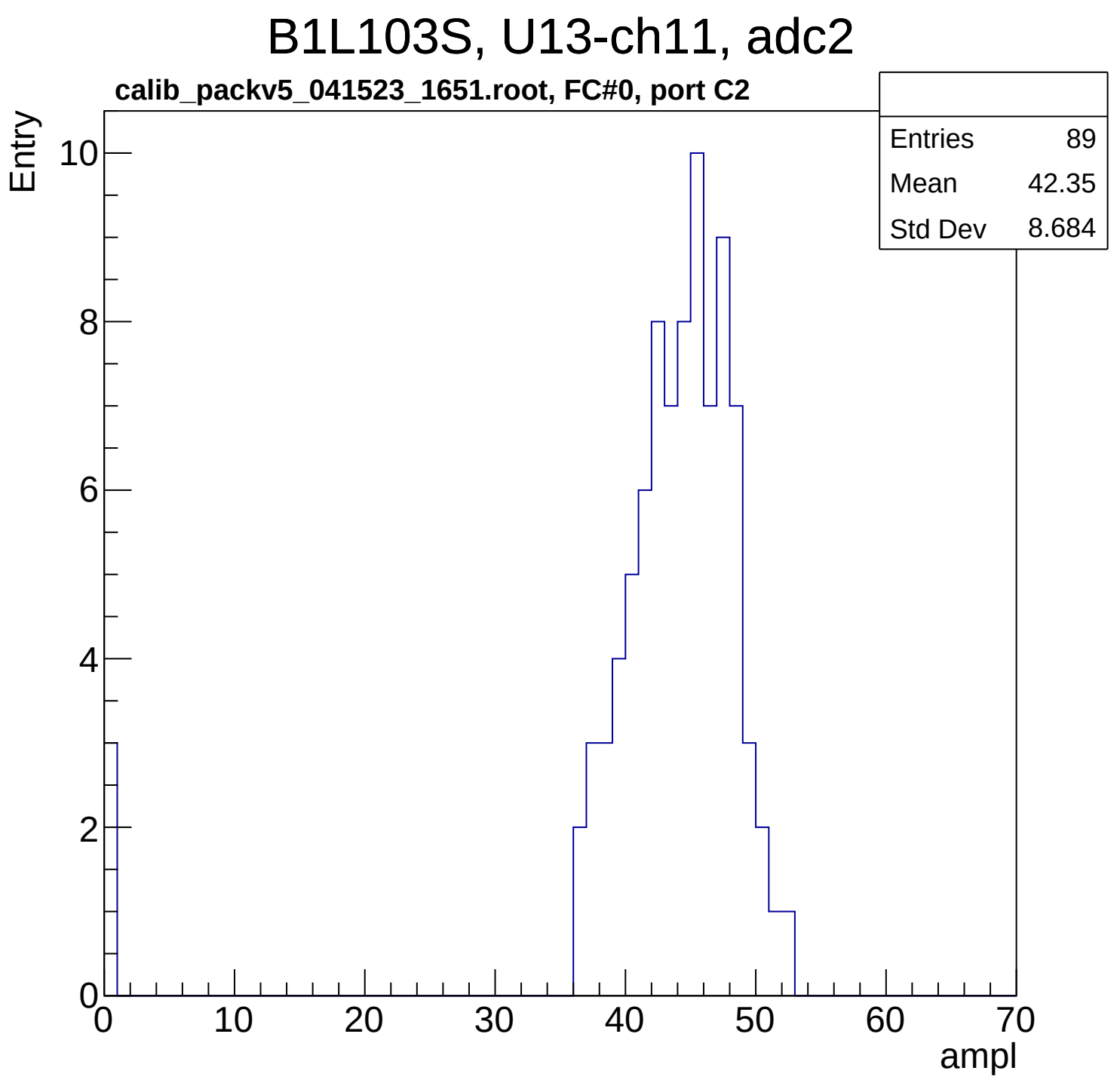
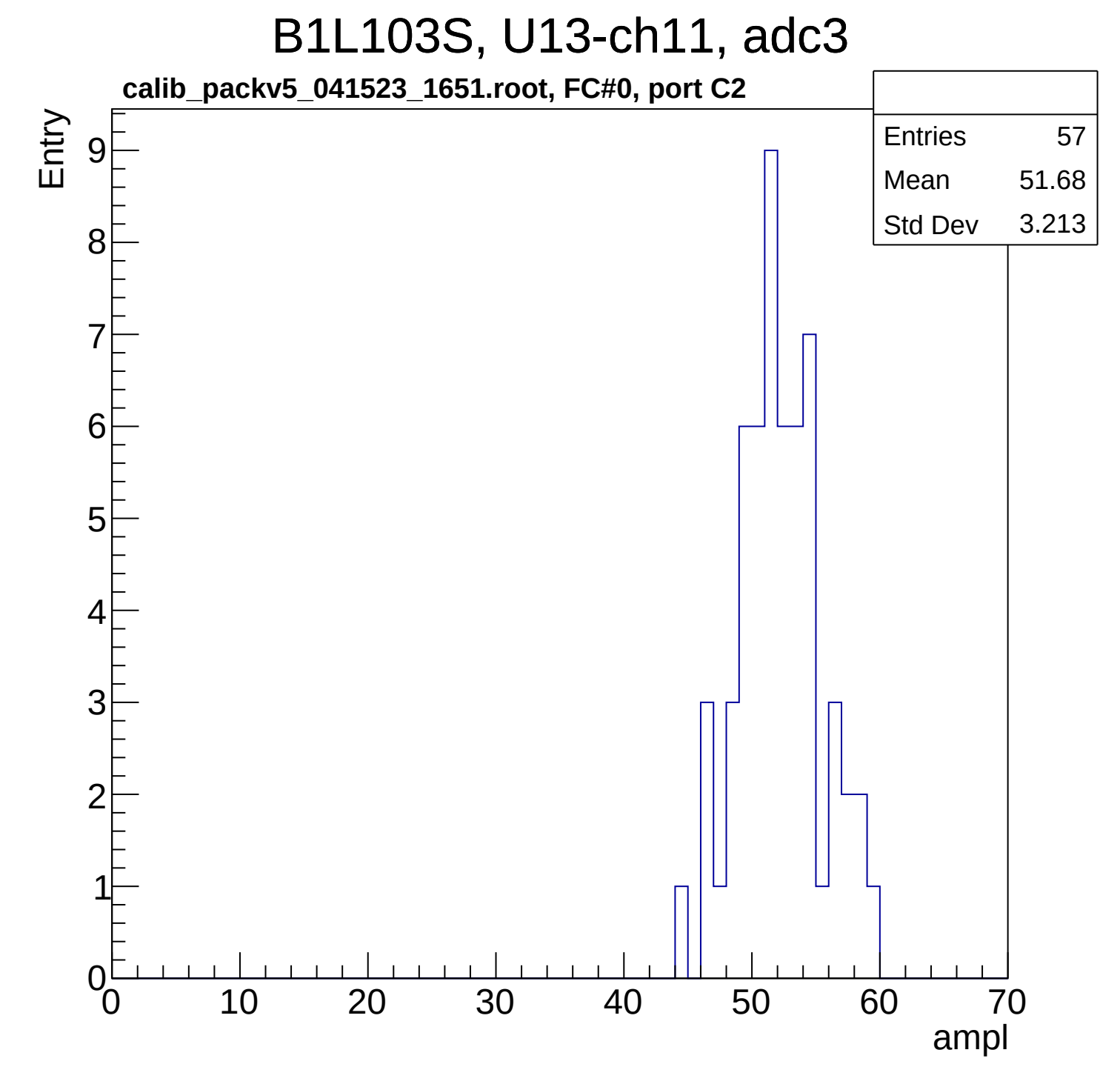
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch11, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 25.66
Std Dev 11.88
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch11, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 31.47
Std Dev 13.07
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch11, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 42.35
Std Dev 8.684
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch11, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 51.68
Std Dev 3.213
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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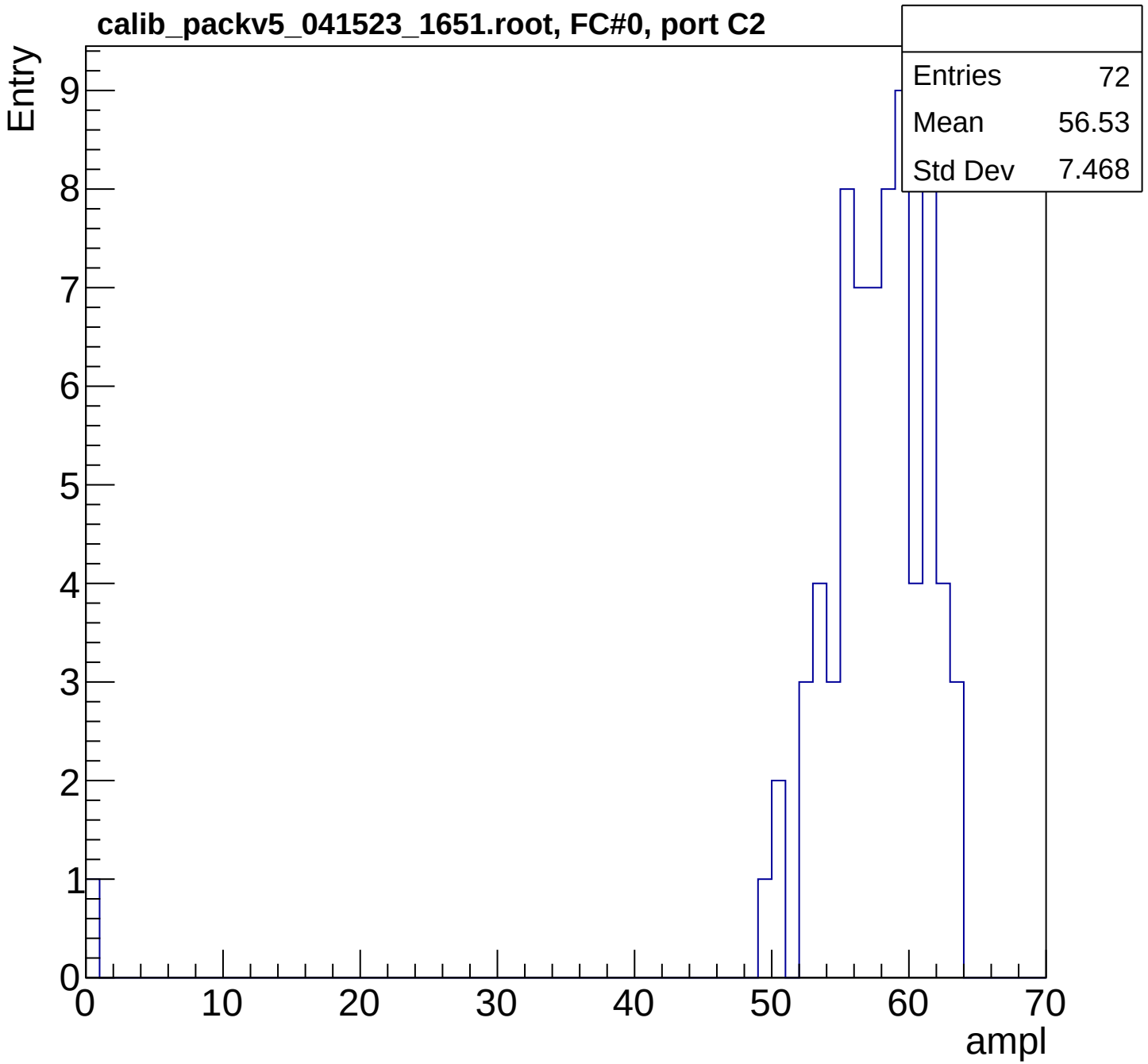
B1L103S, U13-ch11, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 56.53
Std Dev 7.468
Entry
ampl
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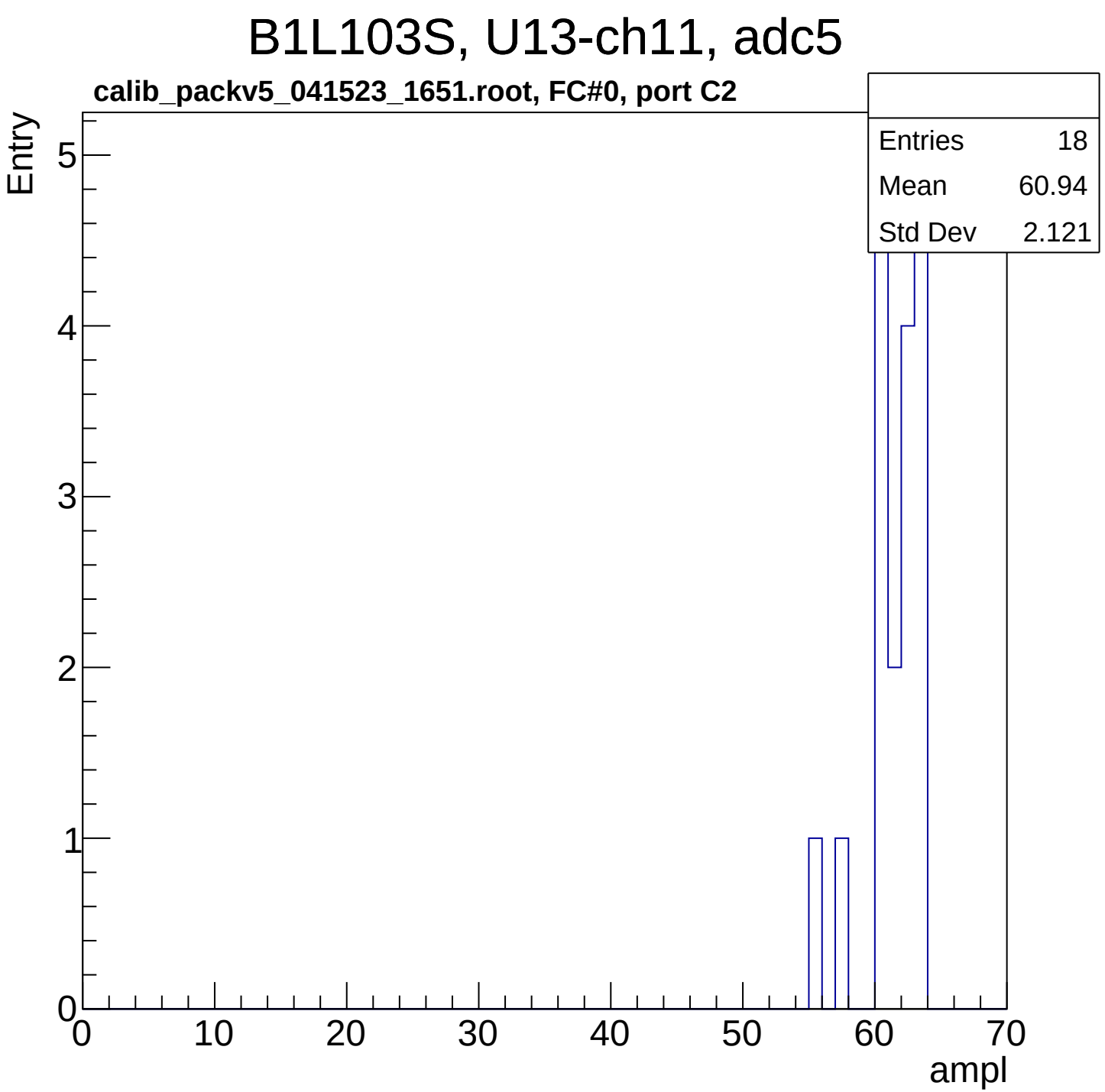
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch11, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 60.94
Std Dev 2.121
Entry
ampl
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2
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4
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0
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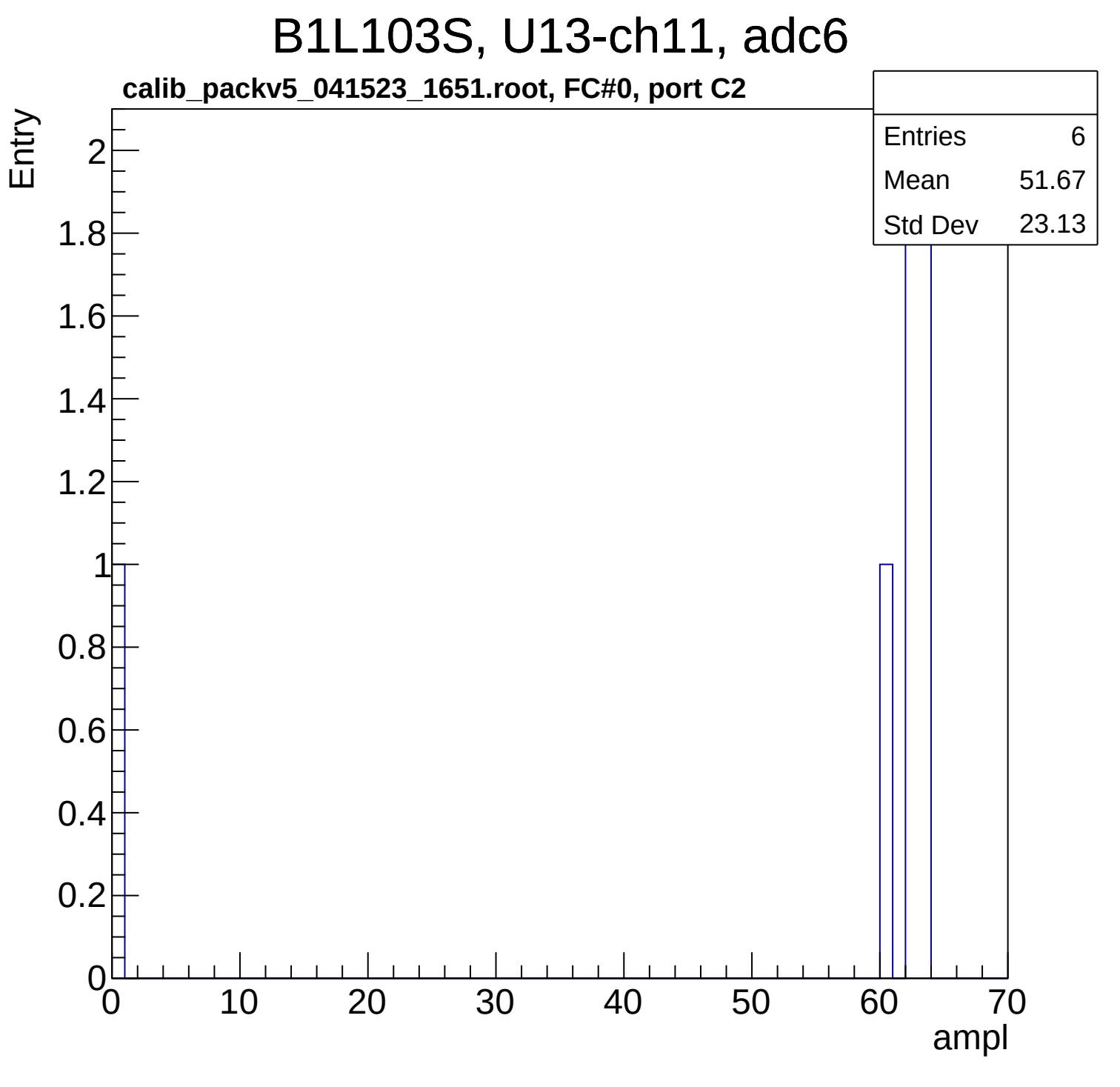
40
50
60
70


B1L103S, U13-ch11, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 51.67
Std Dev 23.13
Entry
ampl
0
0.2
0.4
0.6
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1.2
1.4
1.6
1.8
2
0
10
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60
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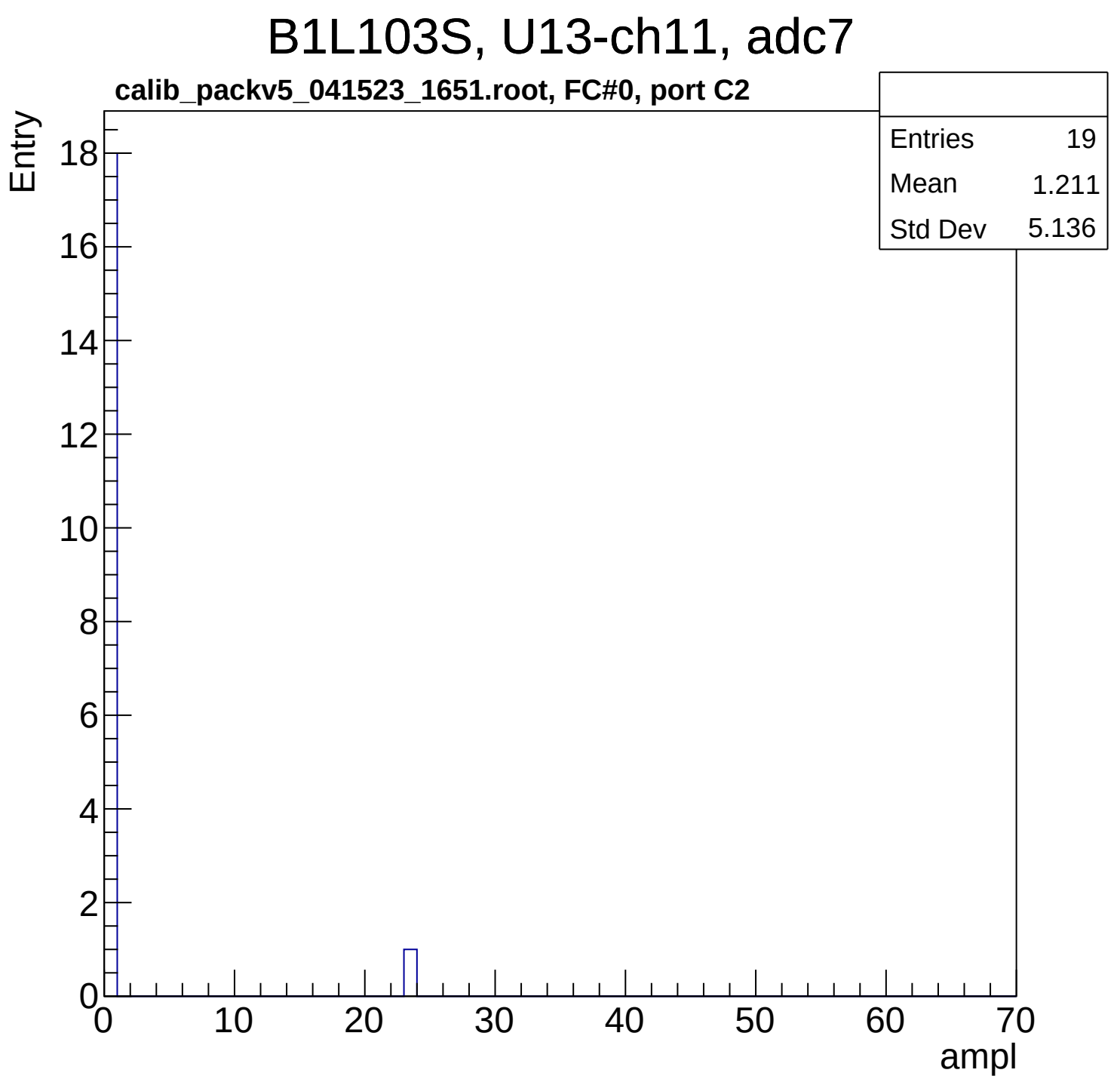
B1L103S, U13-ch11, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.211
Std Dev 5.136
Entry
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6
8
10
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14
16
18
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10
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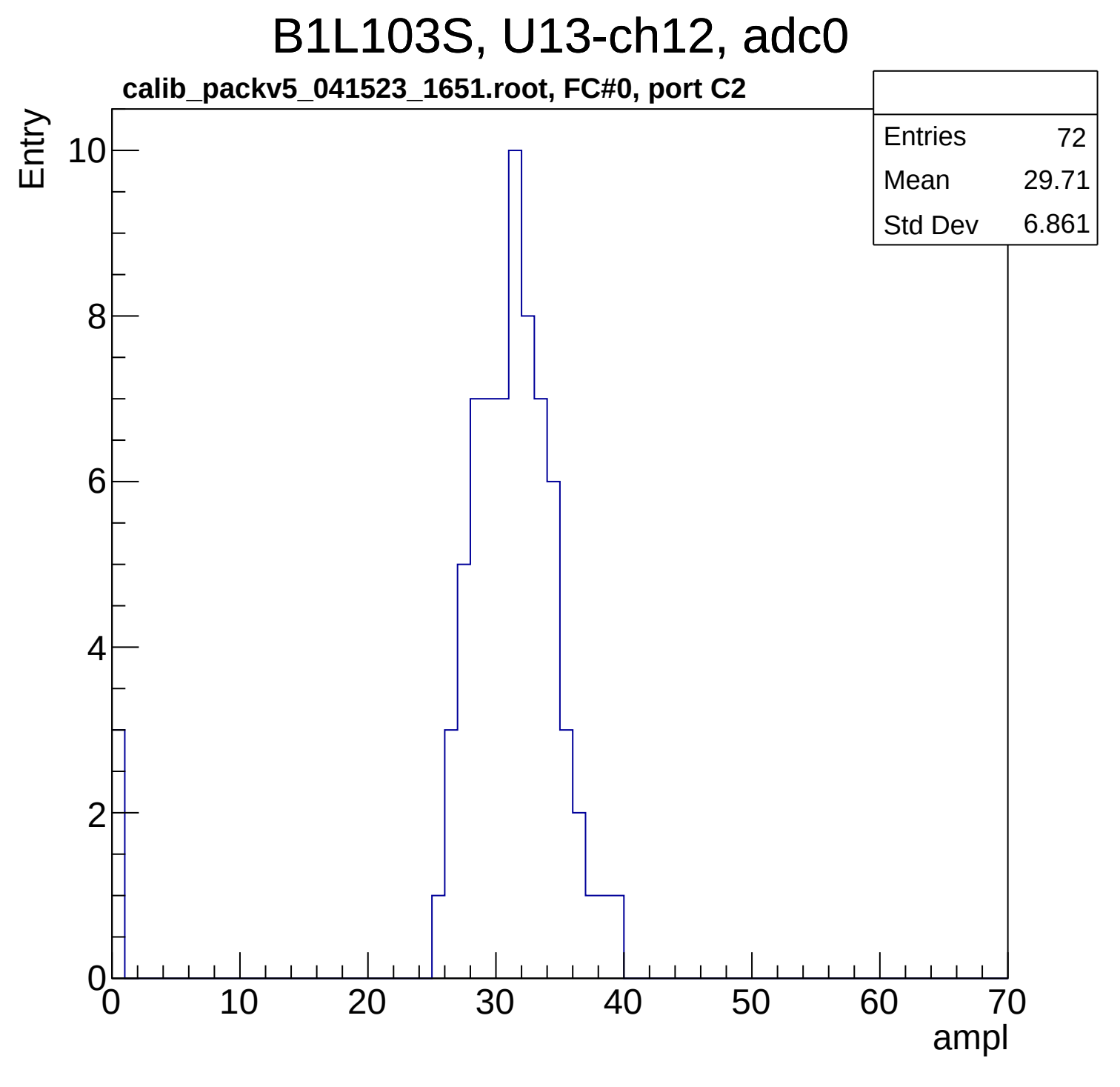
70
ampl


B1L103S, U13-ch12, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 29.71
Std Dev 6.861
Entry
ampl
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0
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40
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60
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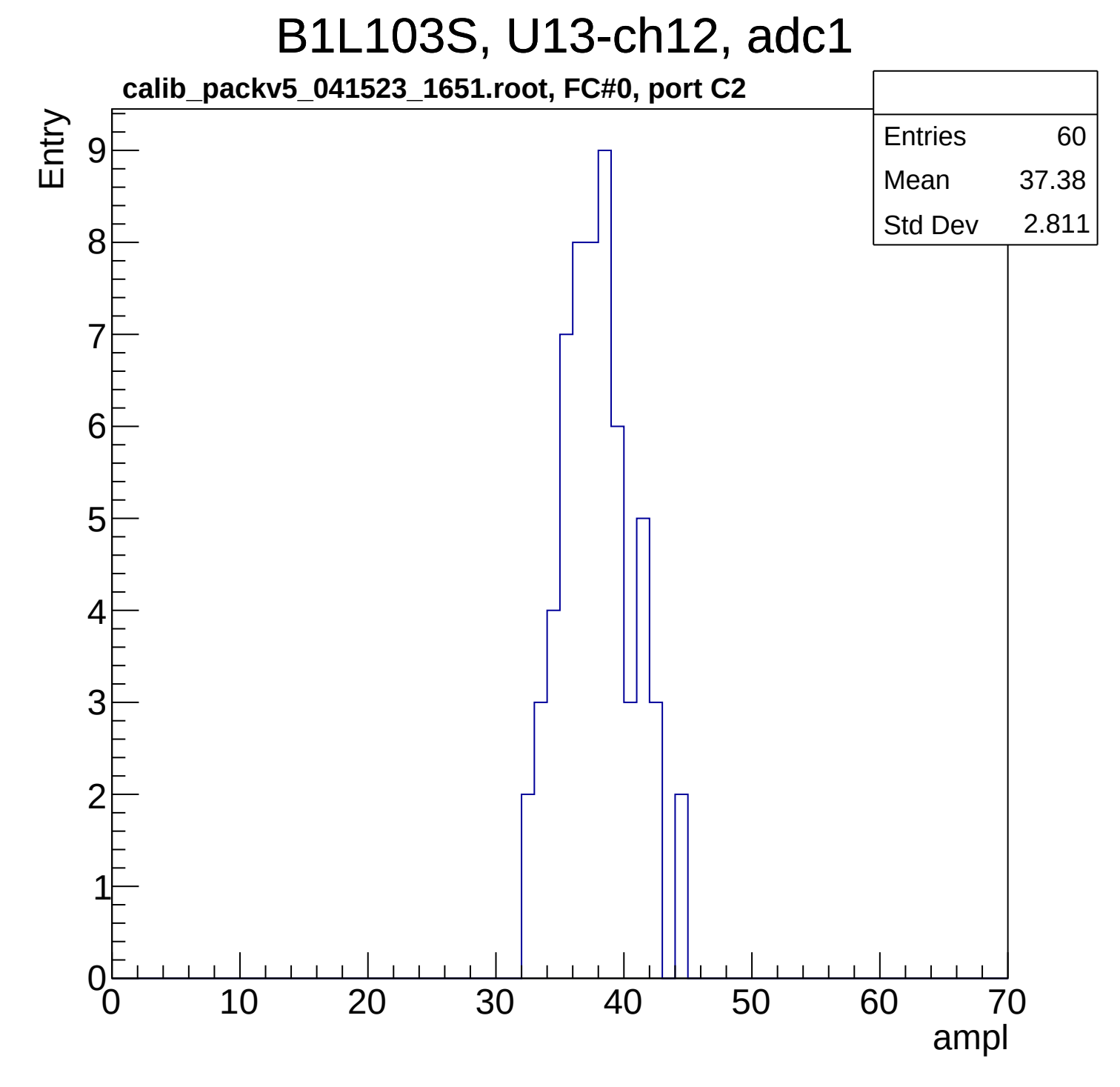
B1L103S, U13-ch12, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 37.38
Std Dev 2.811
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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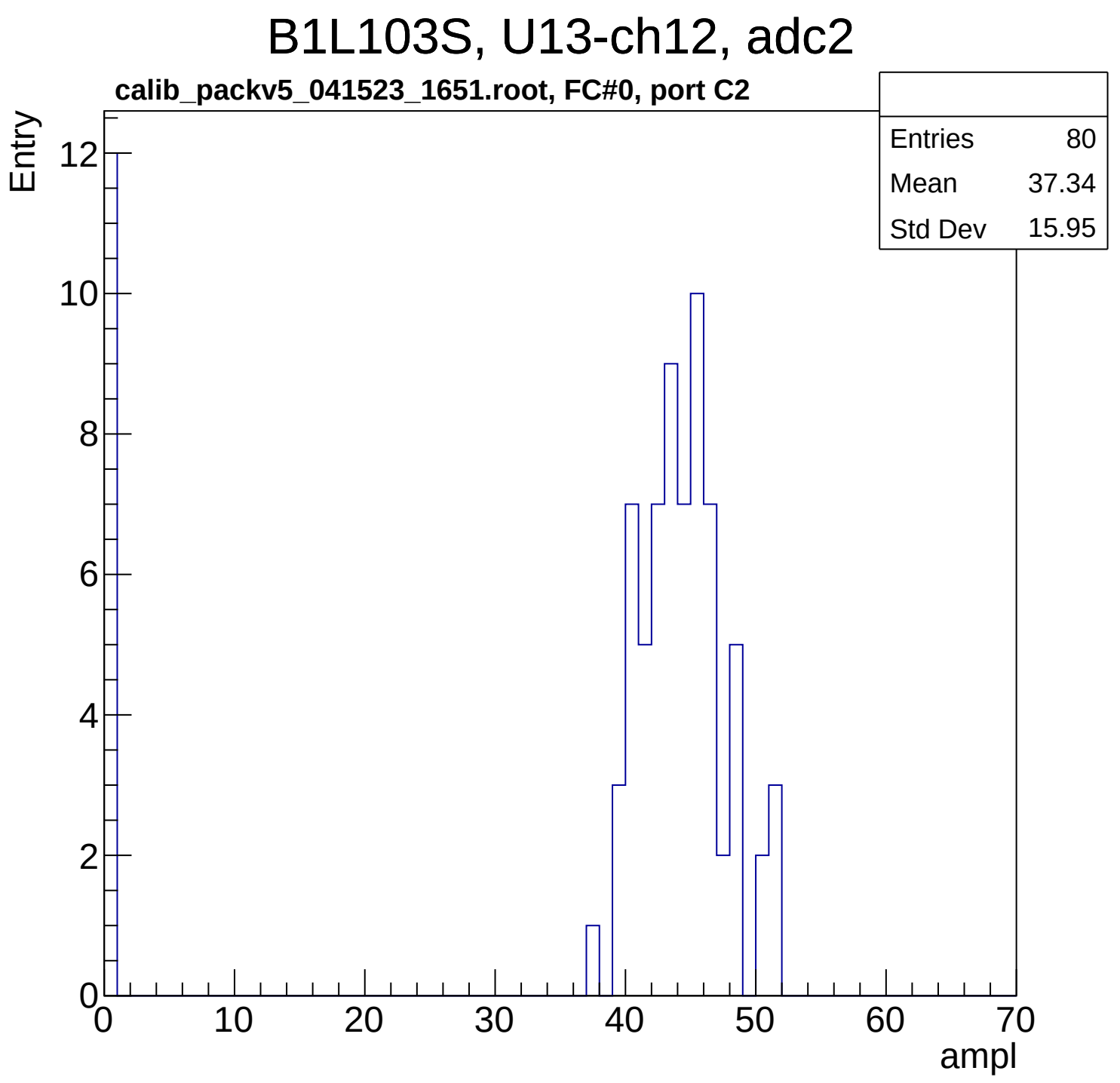
B1L103S, U13-ch12, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 37.34
Std Dev 15.95
Entry
ampl
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2
4
6
8
10
12
0
10
20
30
40
50
60
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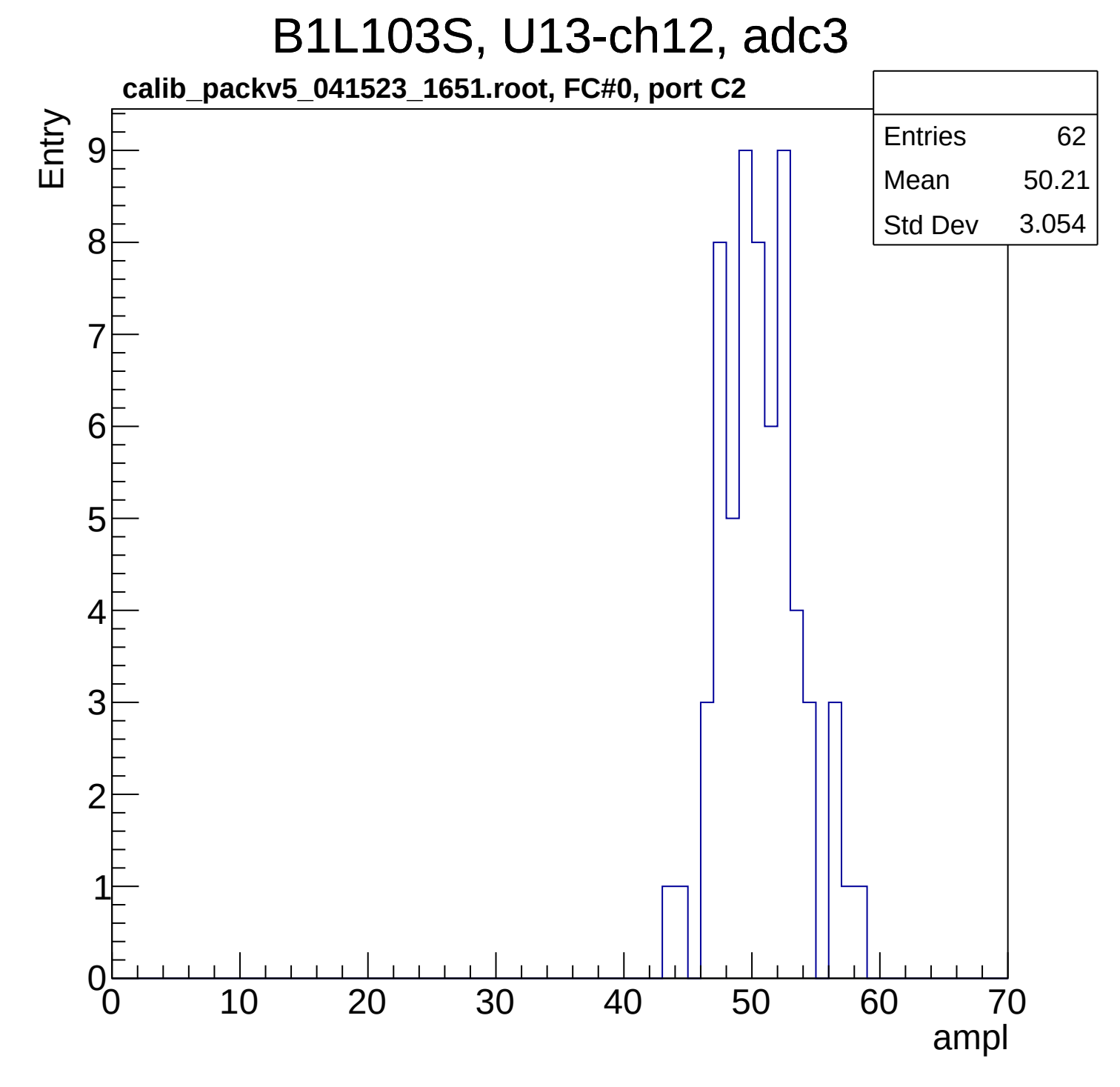
B1L103S, U13-ch12, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 50.21
Std Dev 3.054
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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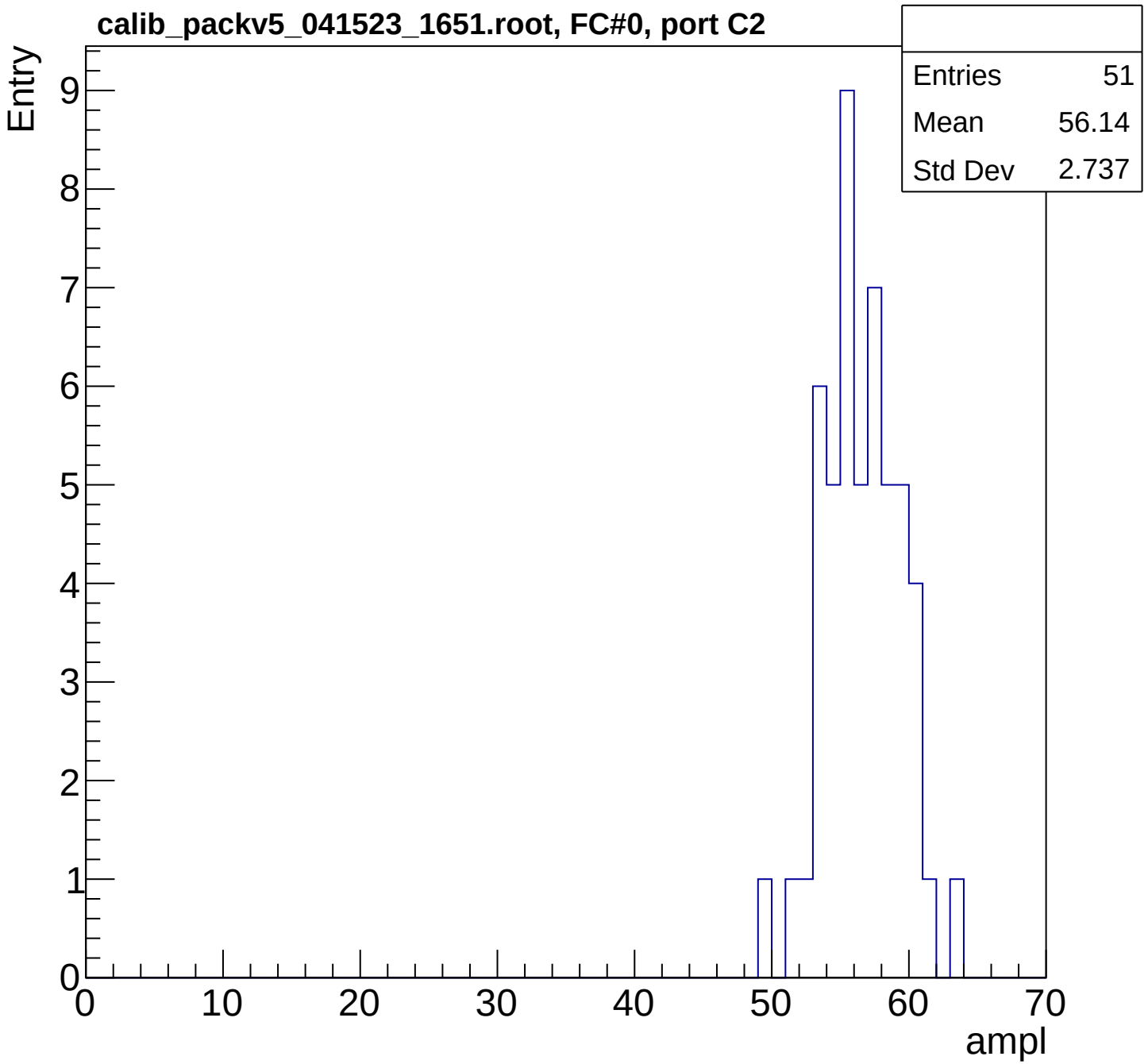
B1L103S, U13-ch12, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 56.14
Std Dev 2.737
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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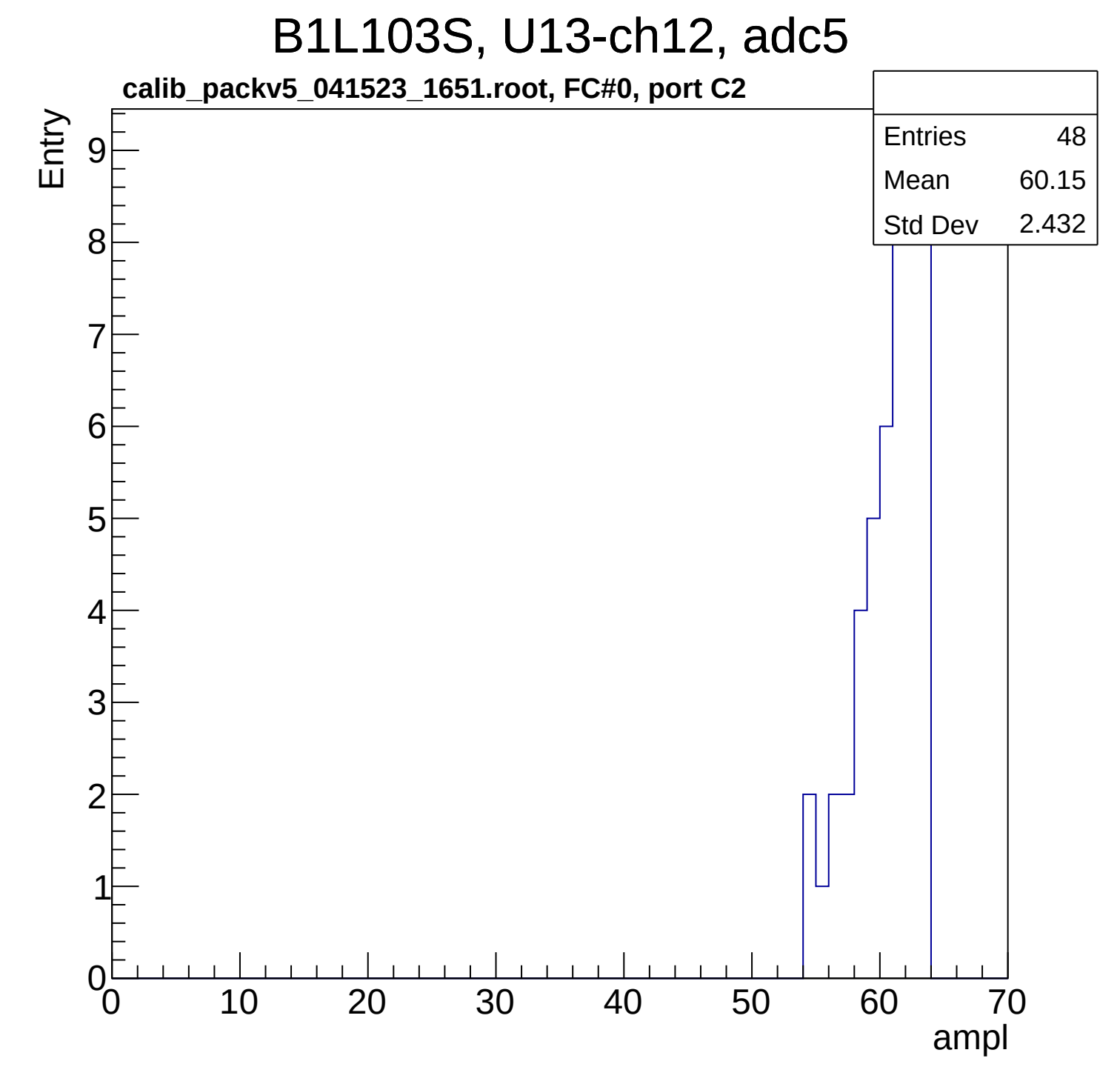
B1L103S, U13-ch12, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 60.15
Std Dev 2.432
Entry
ampl
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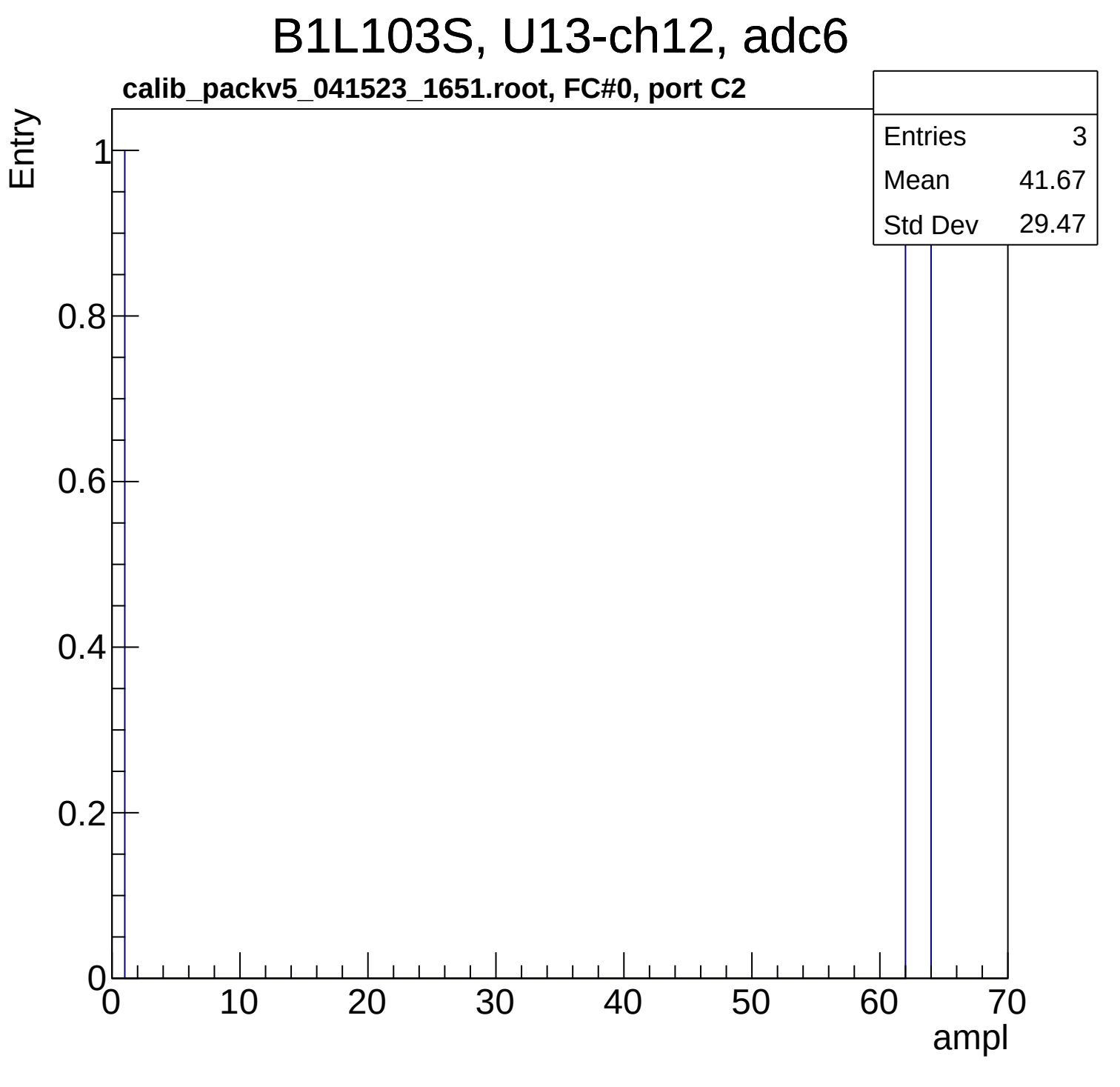
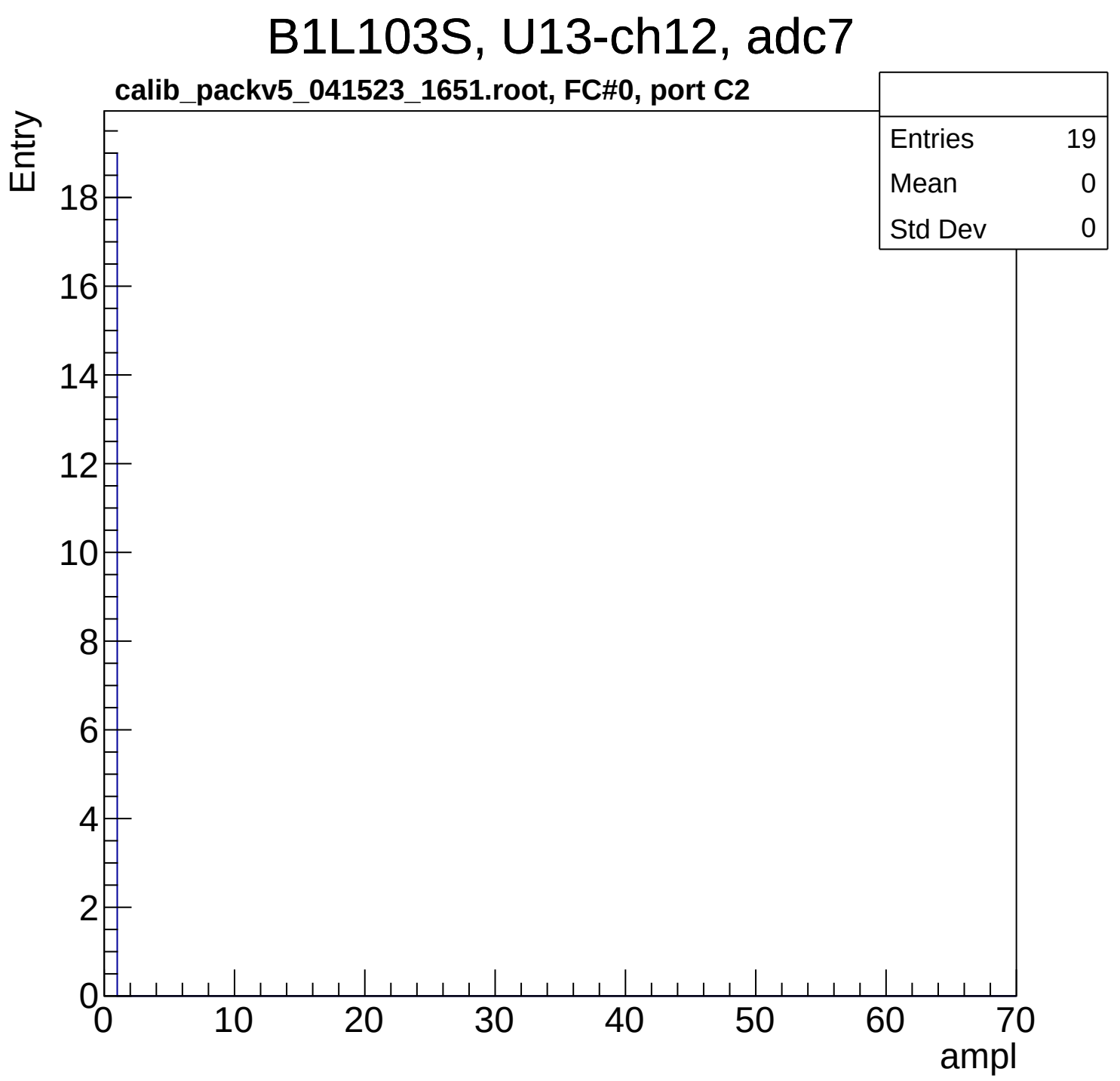
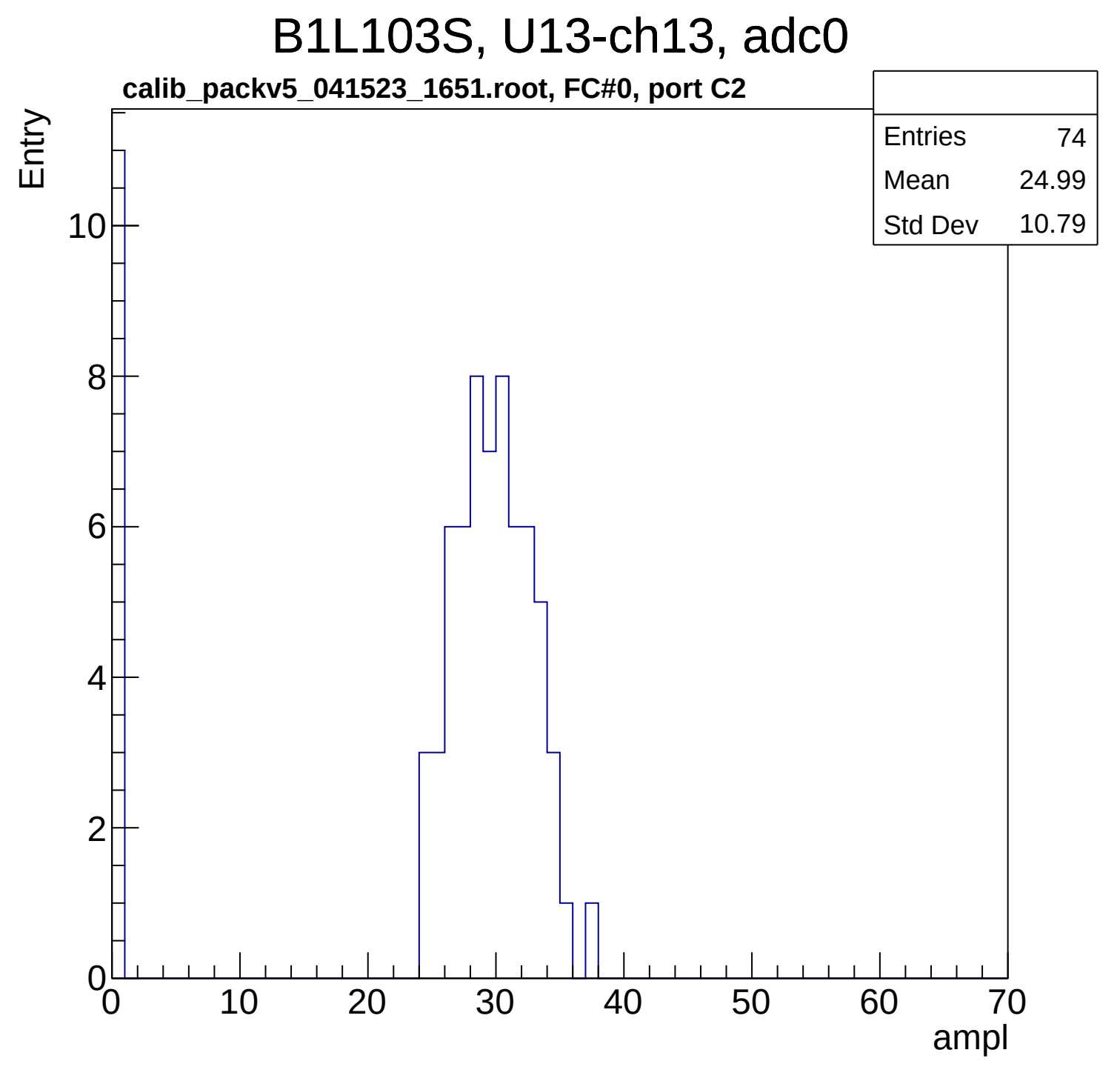
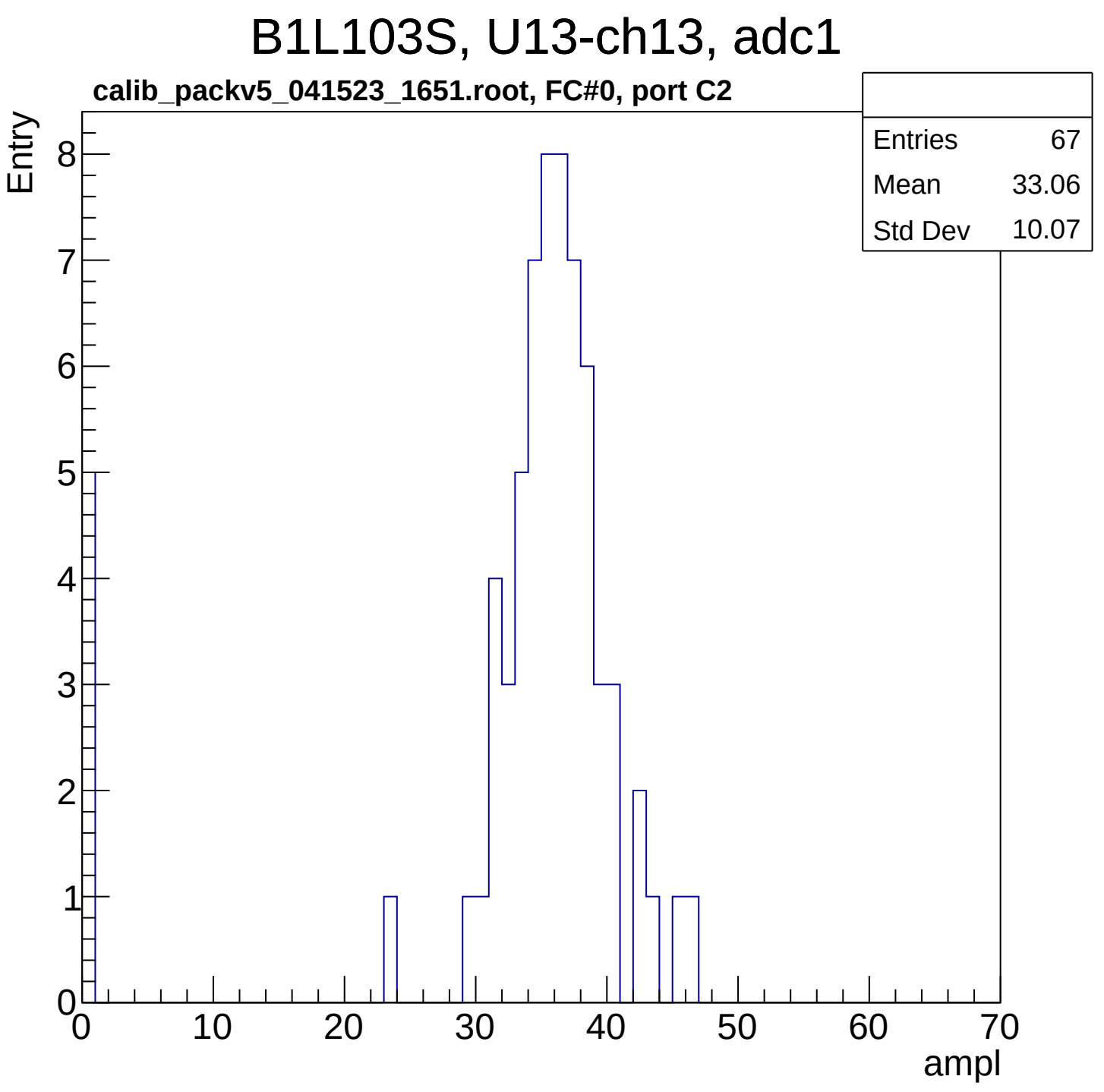
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch12, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 41.67
Std Dev 29.47
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch12, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch13, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 24.99
Std Dev 10.79
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch13, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 33.06
Std Dev 10.07
Entry
ampl
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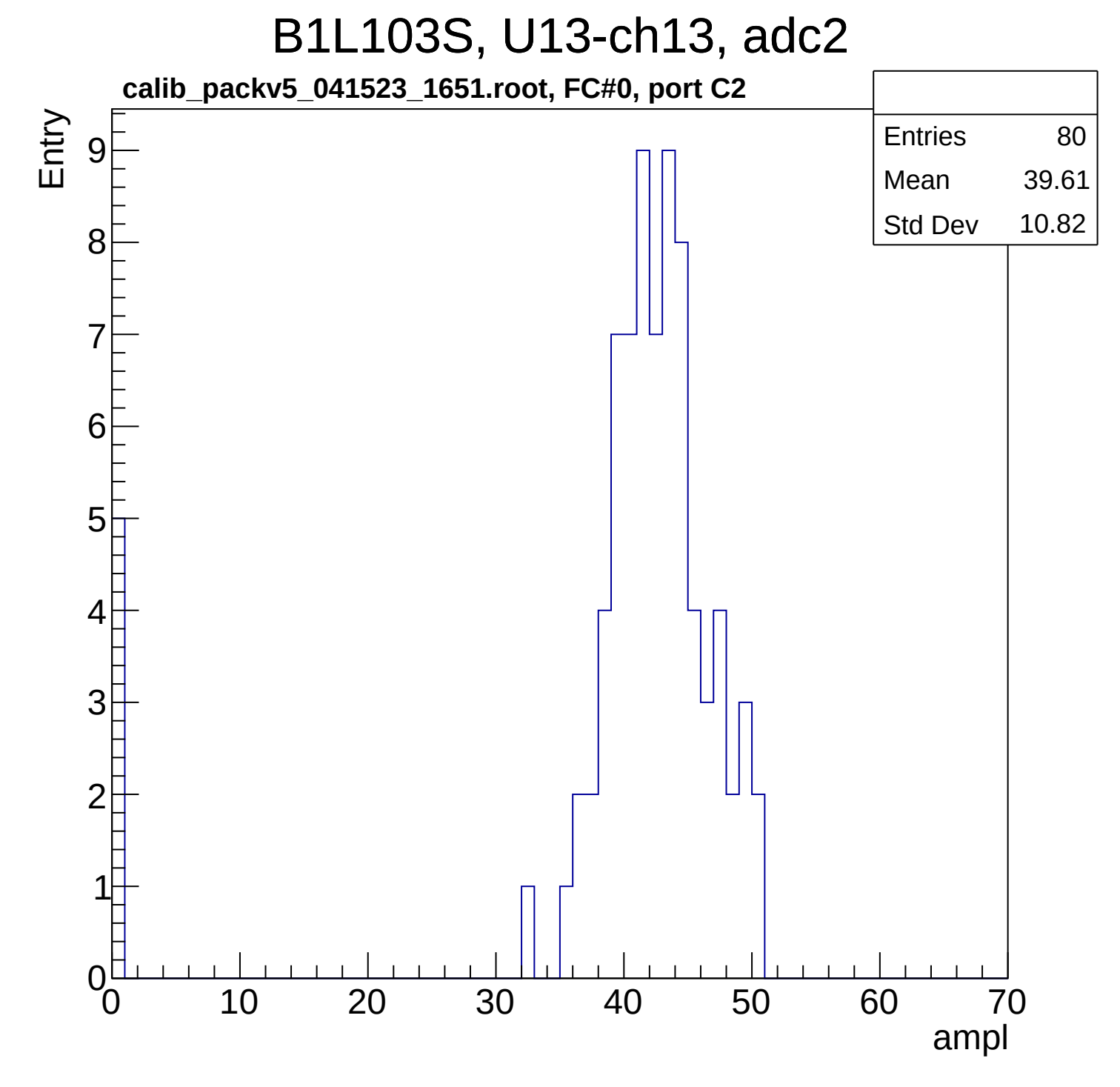
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch13, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 39.61
Std Dev 10.82
Entry
ampl
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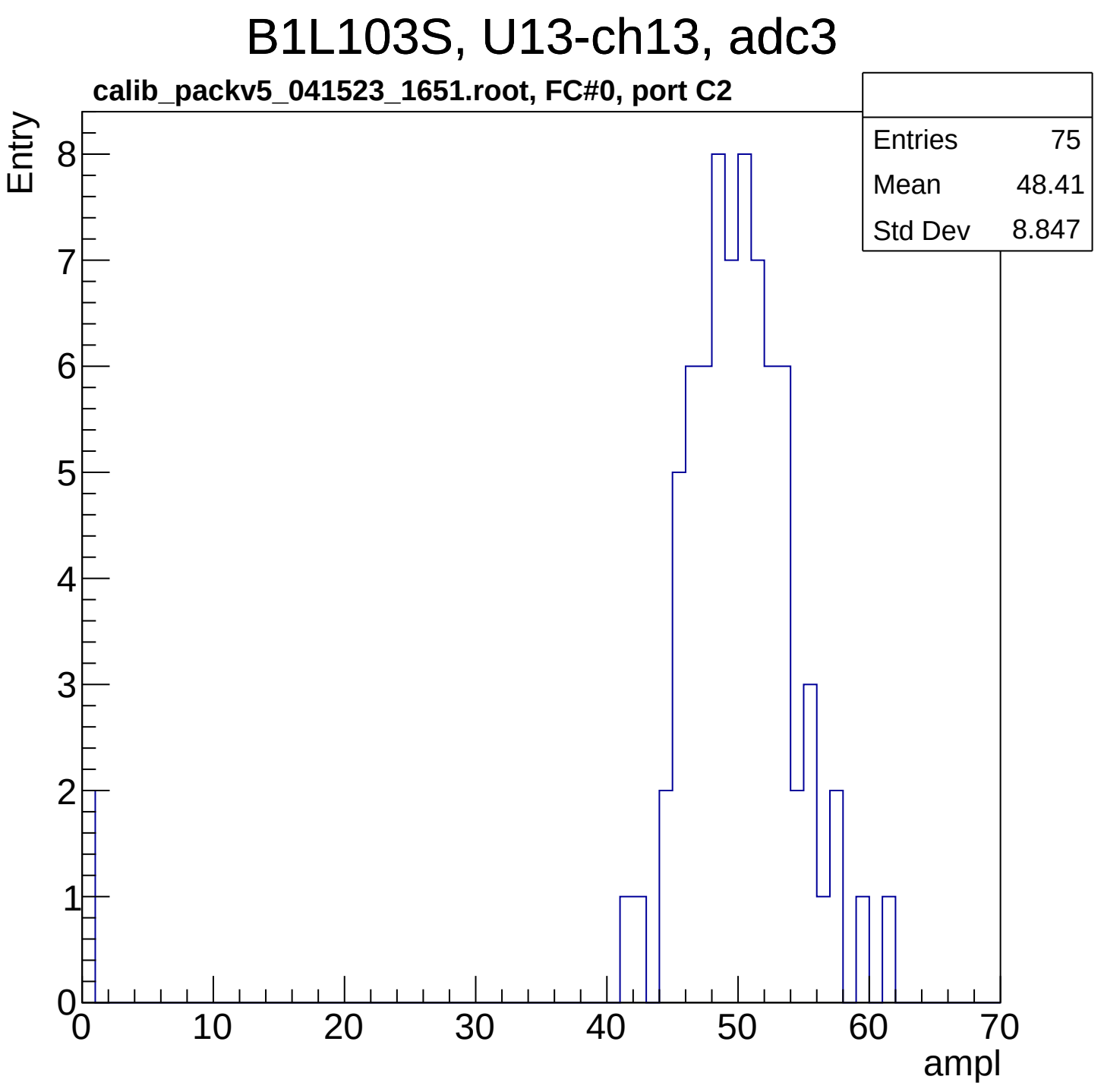
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch13, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 48.41
Std Dev 8.847
Entry
ampl
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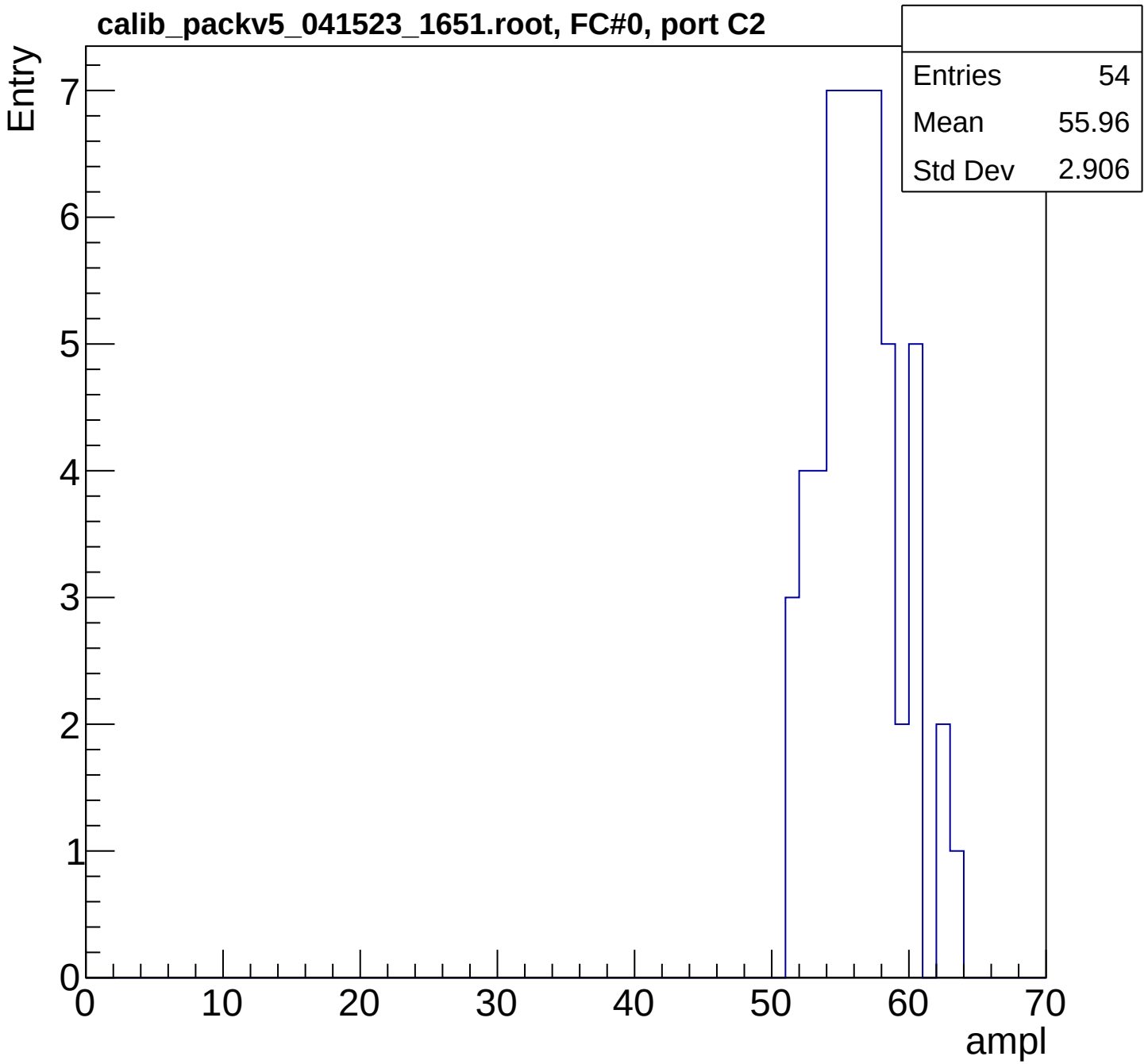
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch13, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 55.96
Std Dev 2.906
Entry
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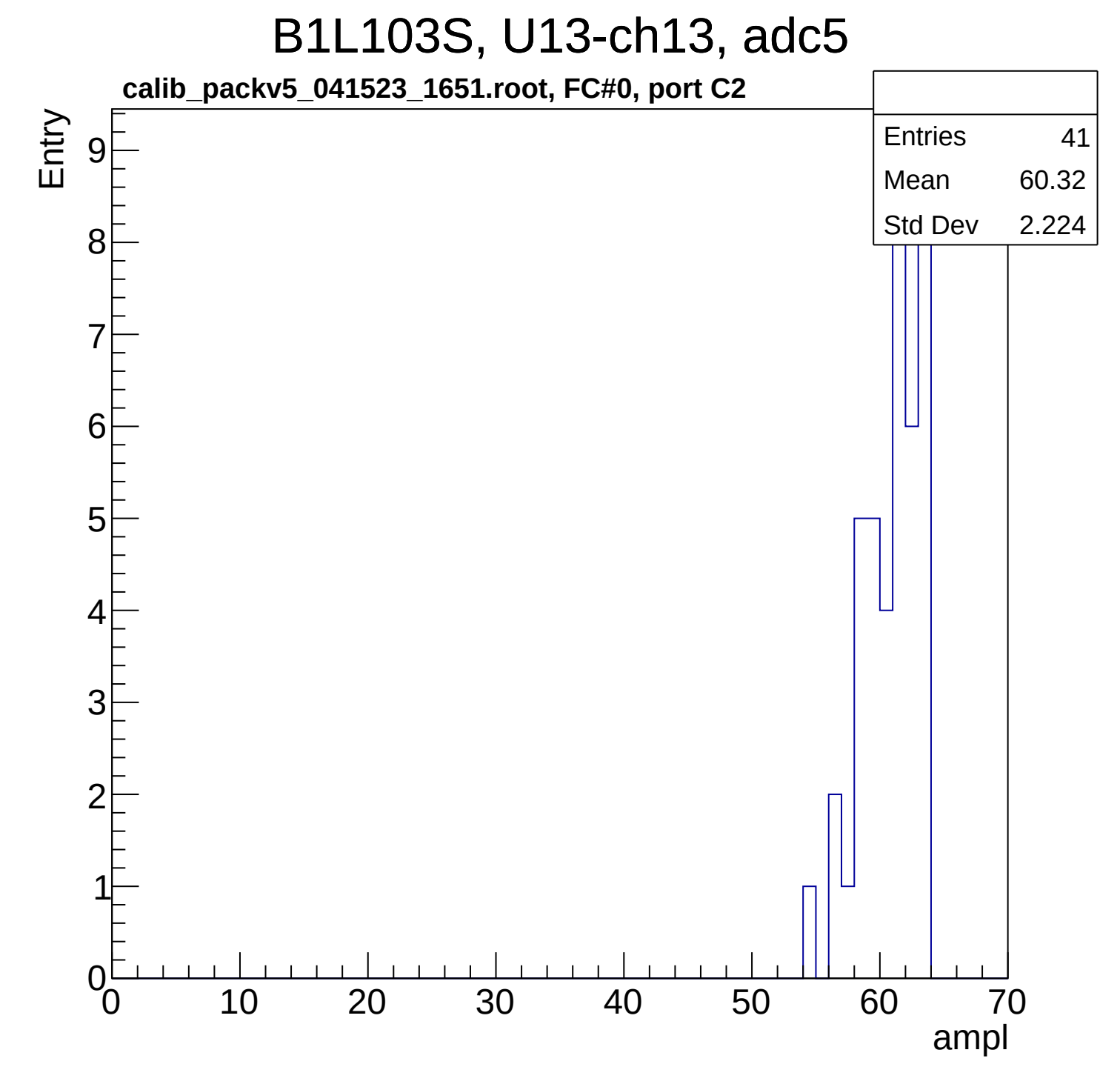
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch13, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 60.32
Std Dev 2.224
Entry
ampl
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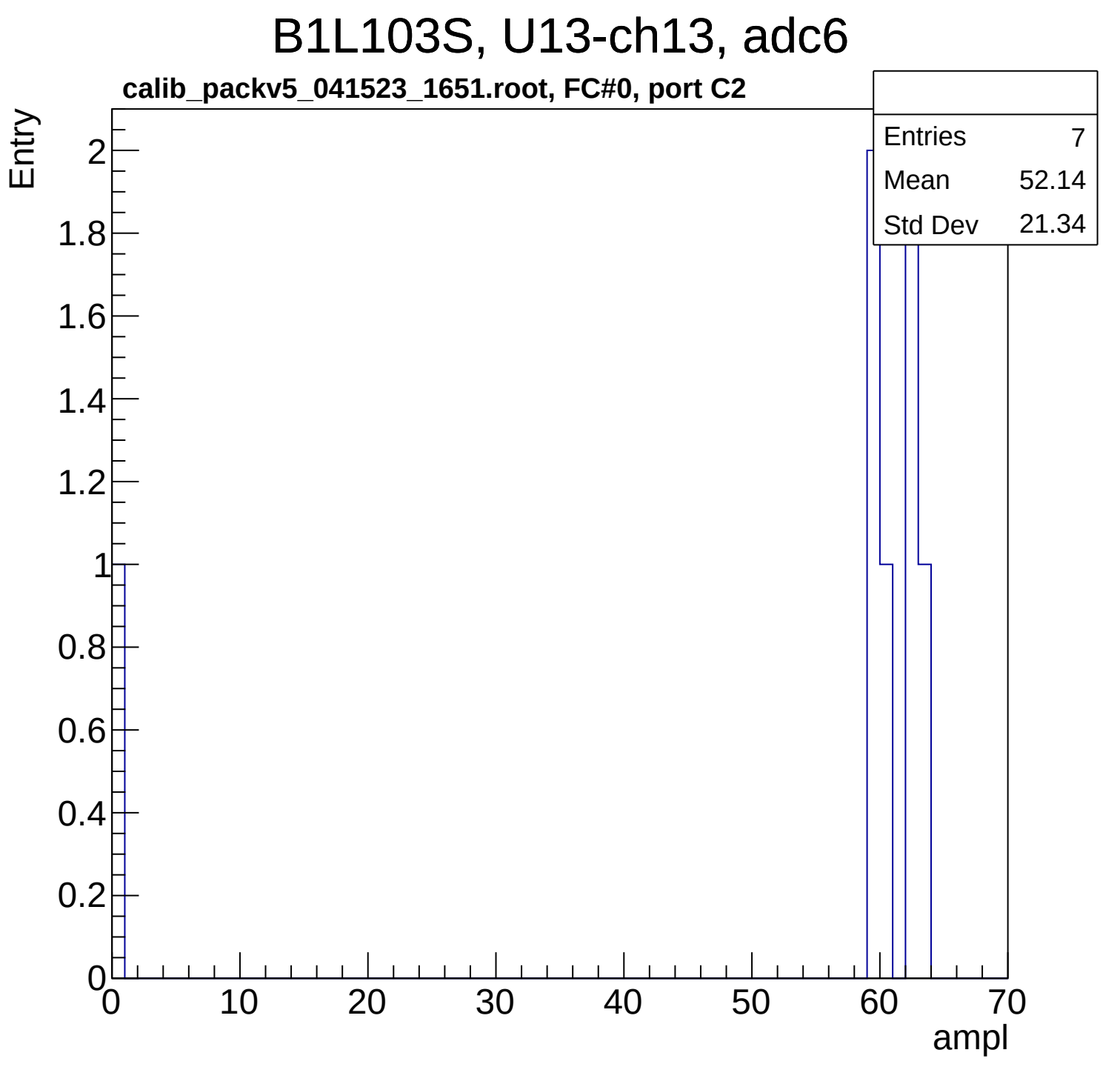
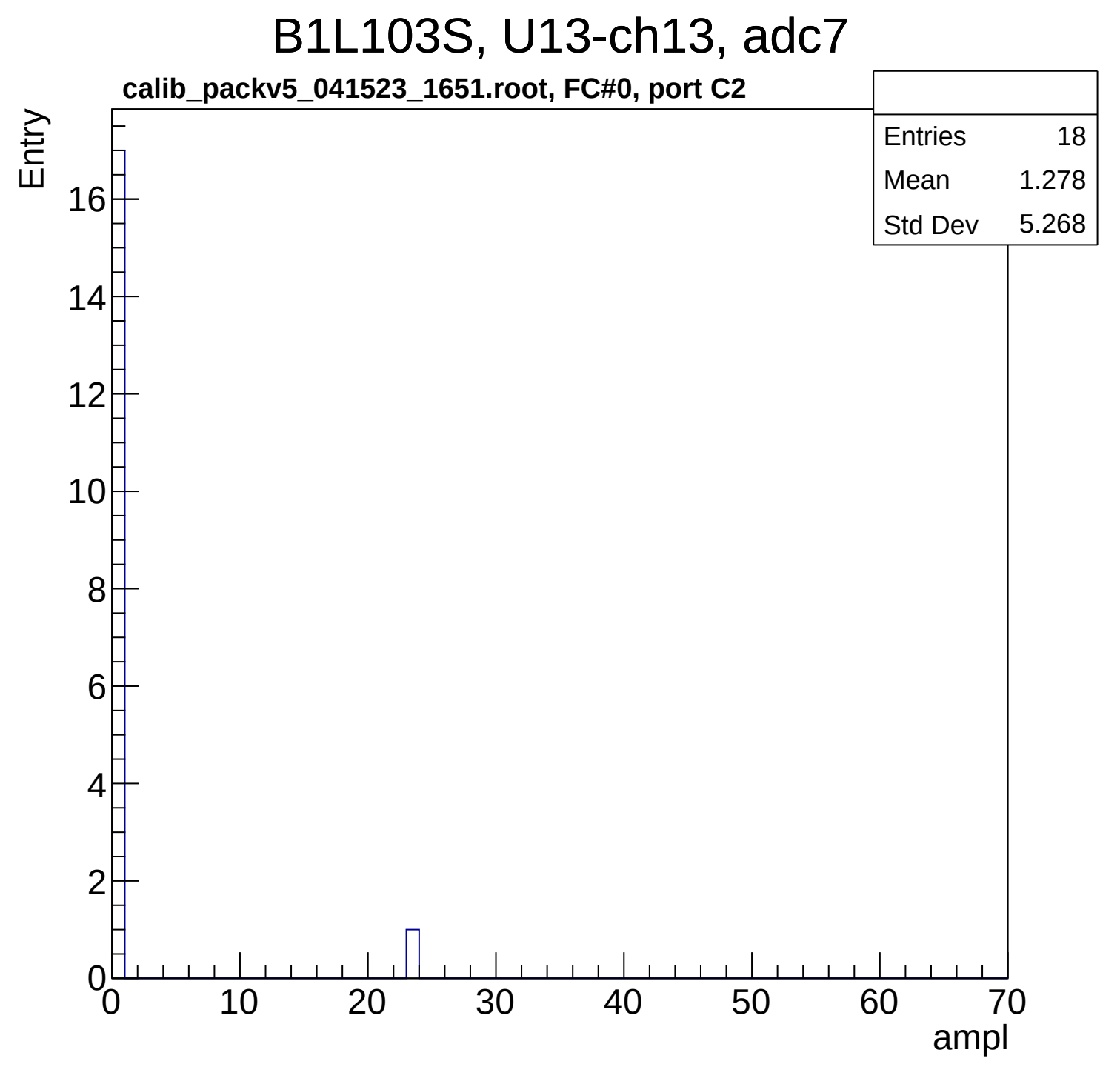
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch13, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 52.14
Std Dev 21.34
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U13-ch13, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.278
Std Dev 5.268
Entry
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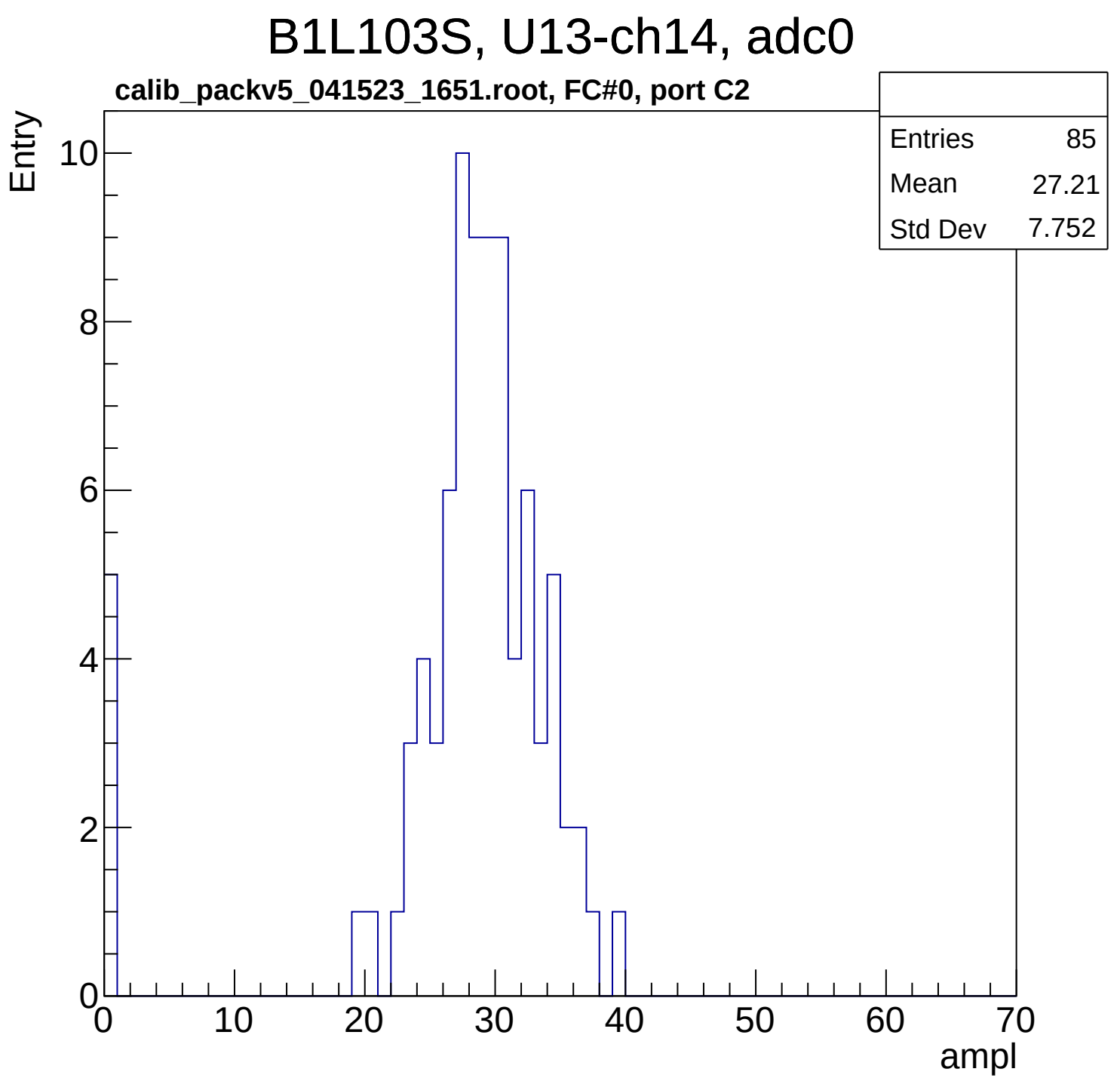
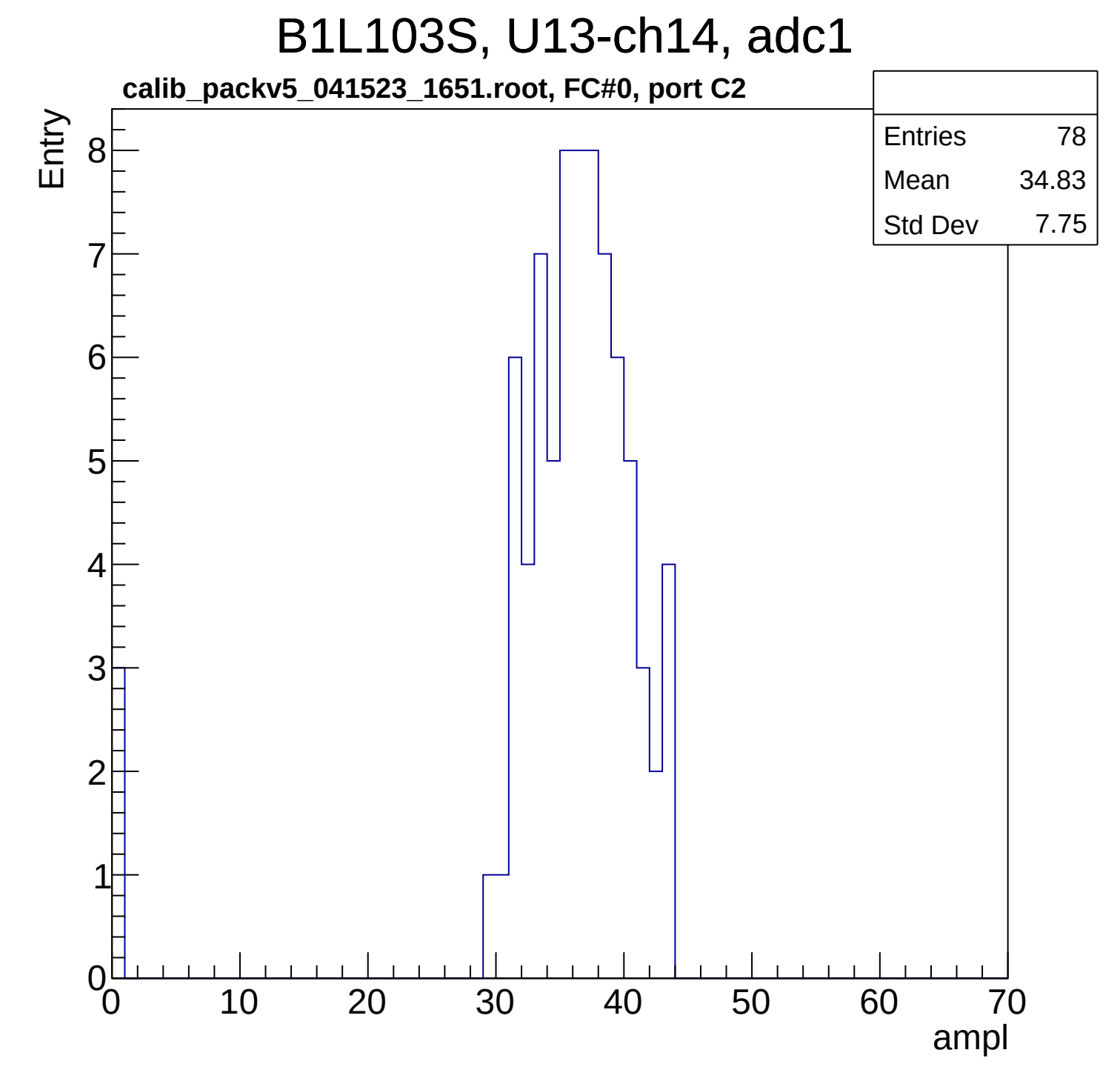
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch14, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 27.21
Std Dev 7.752
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch14, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 34.83
Std Dev 7.75
Entry
ampl
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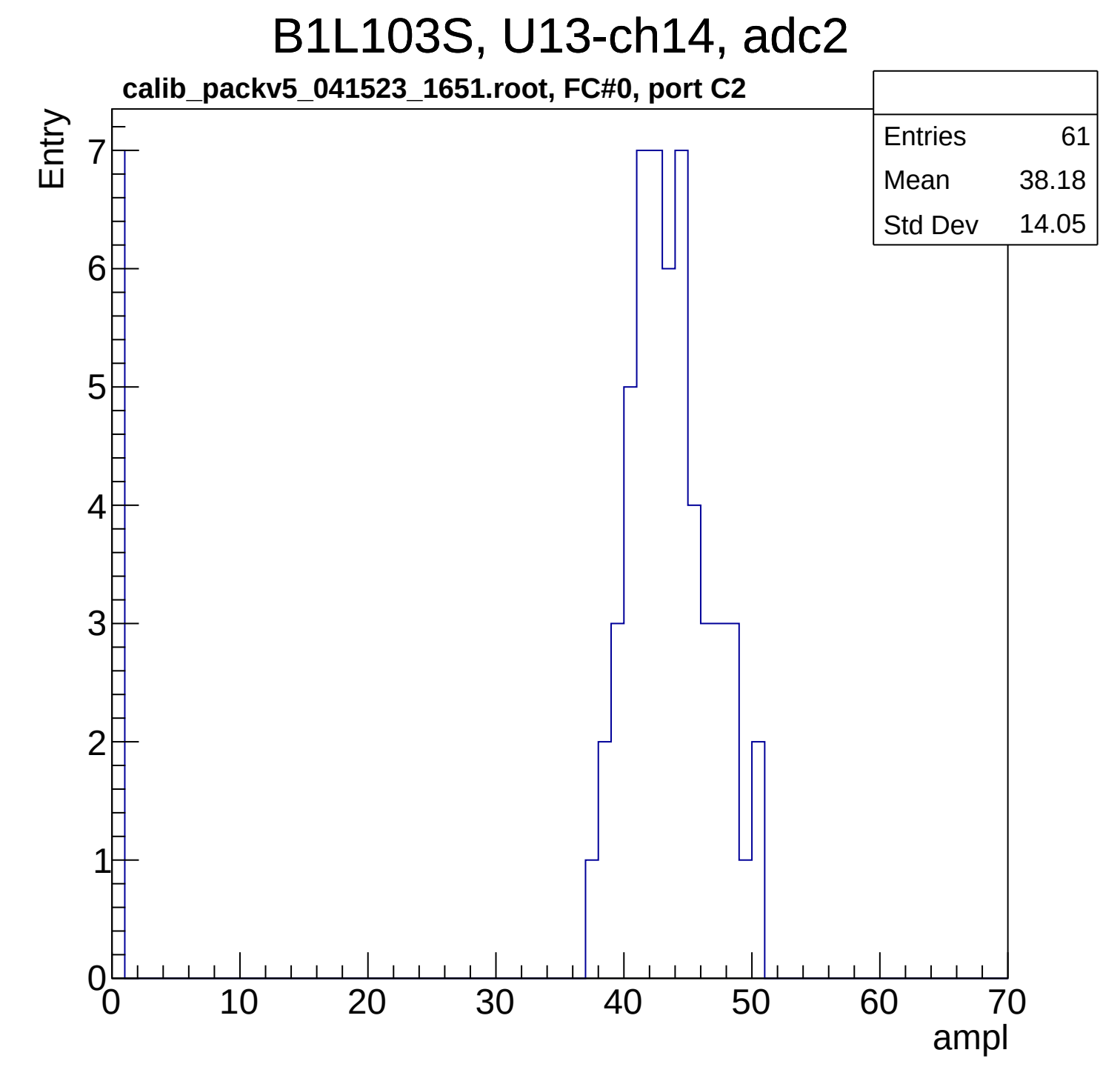
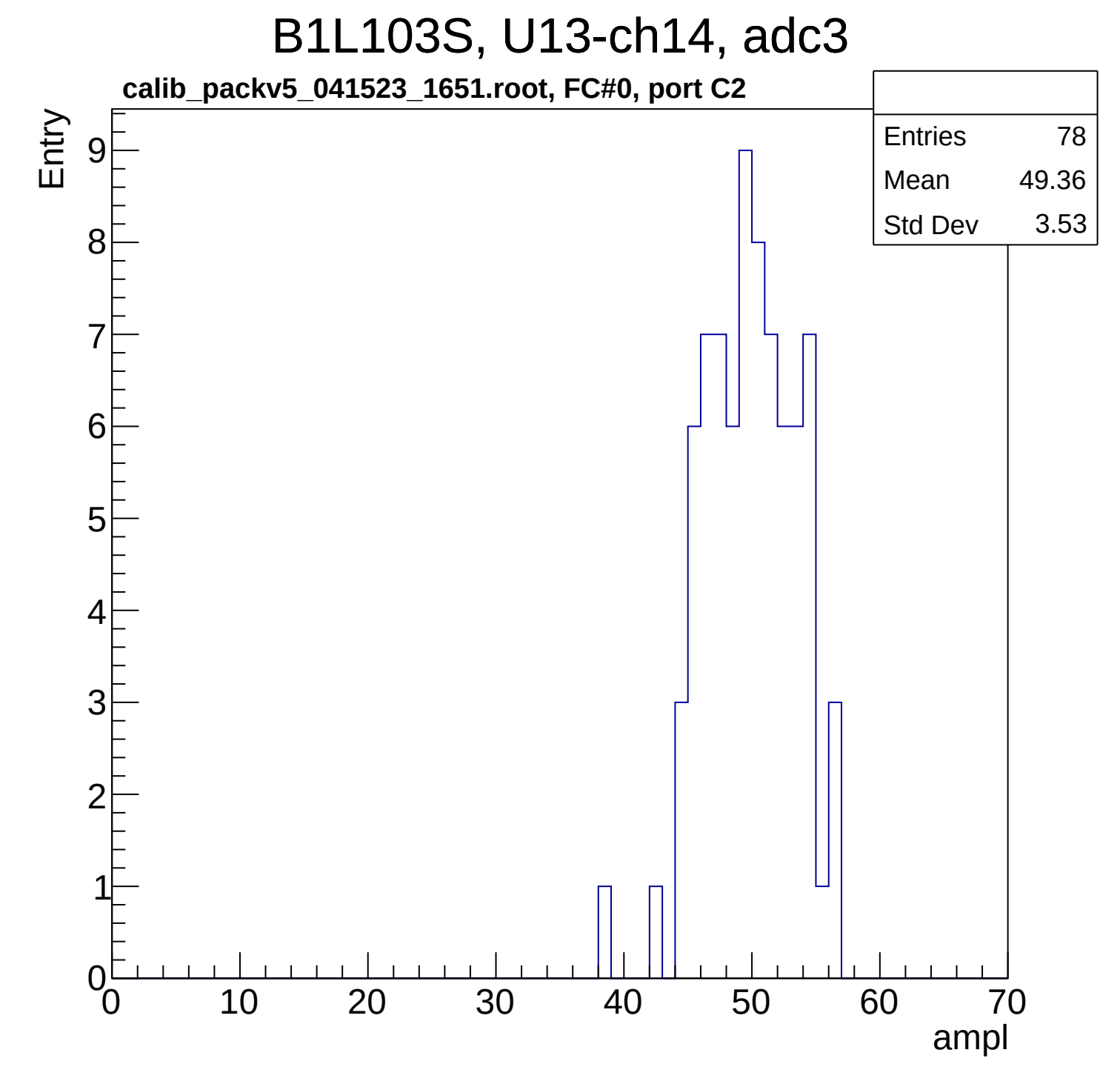
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch14, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 38.18
Std Dev 14.05
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch14, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 49.36
Std Dev 3.53
Entry
ampl
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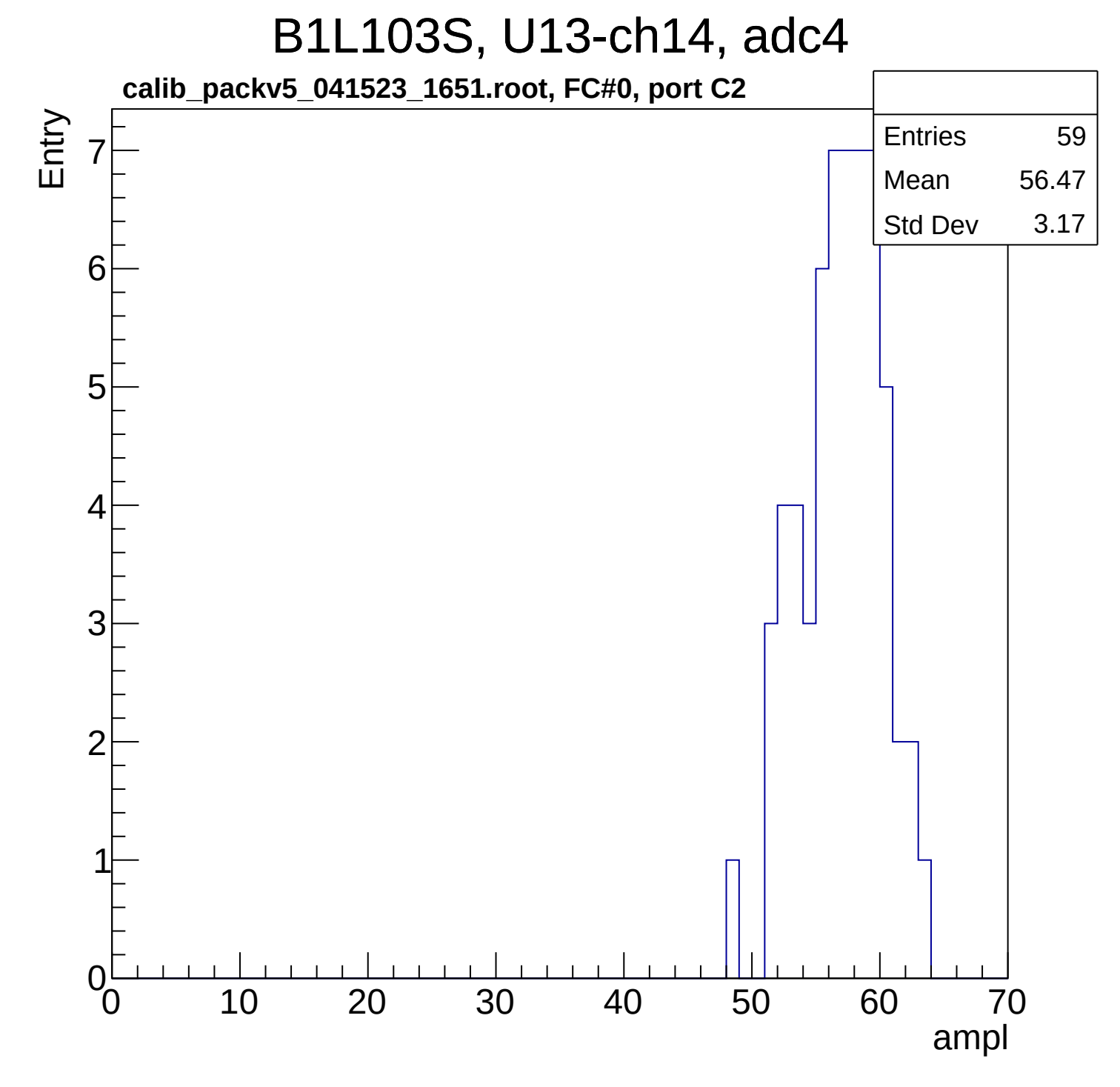
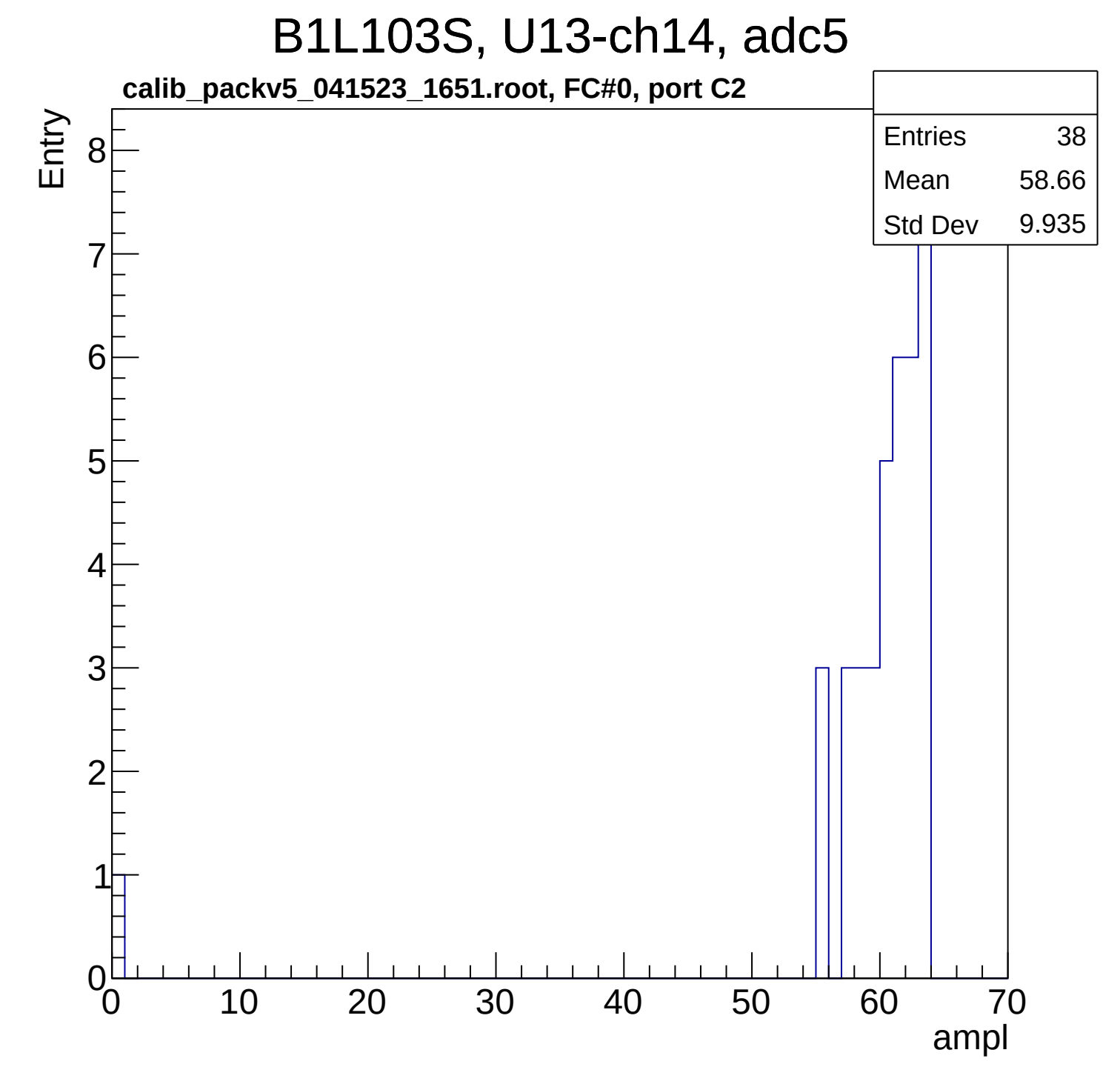
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch14, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 56.47
Std Dev 3.17
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch14, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 58.66
Std Dev 9.935
Entry
ampl
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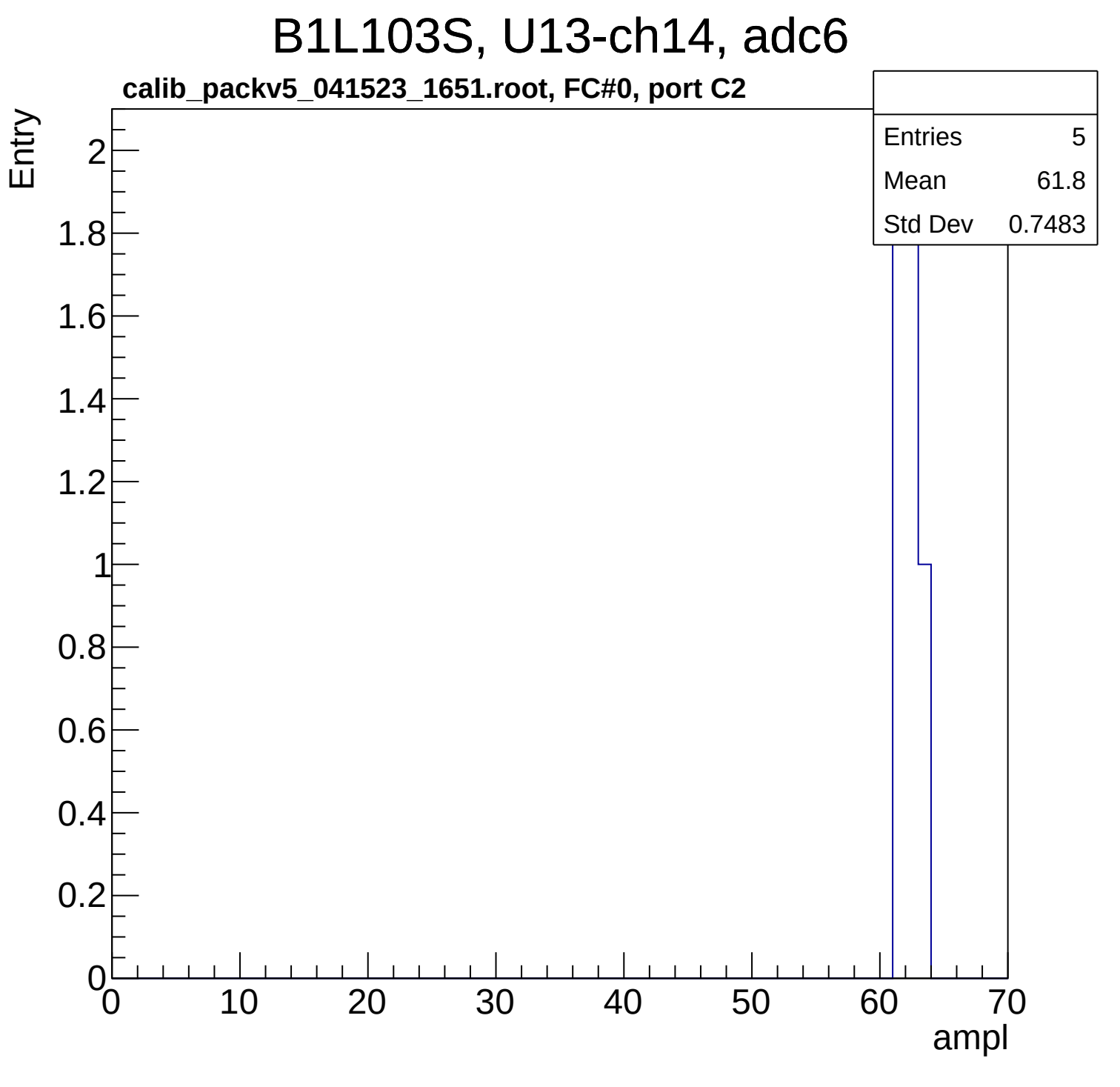
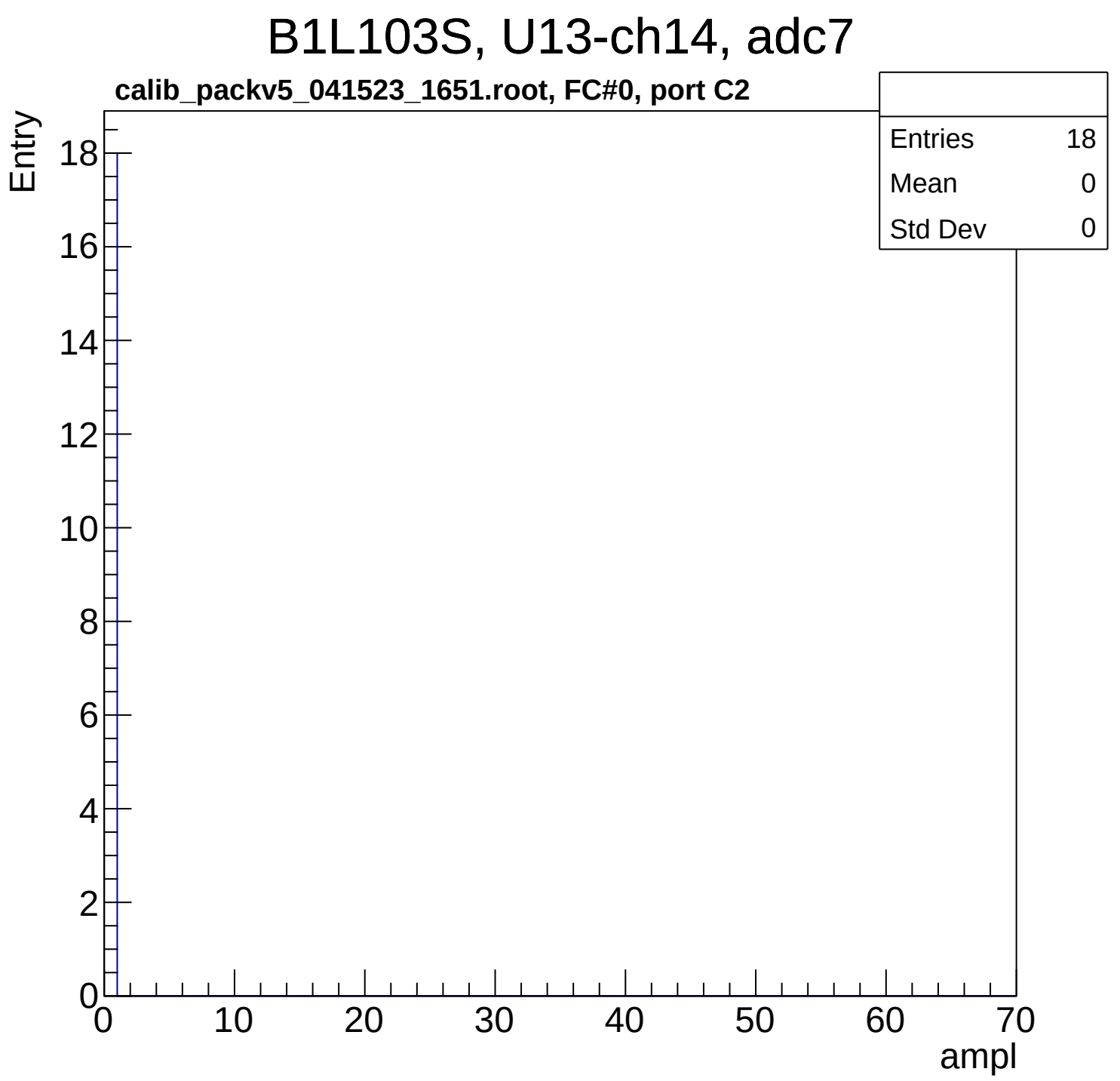
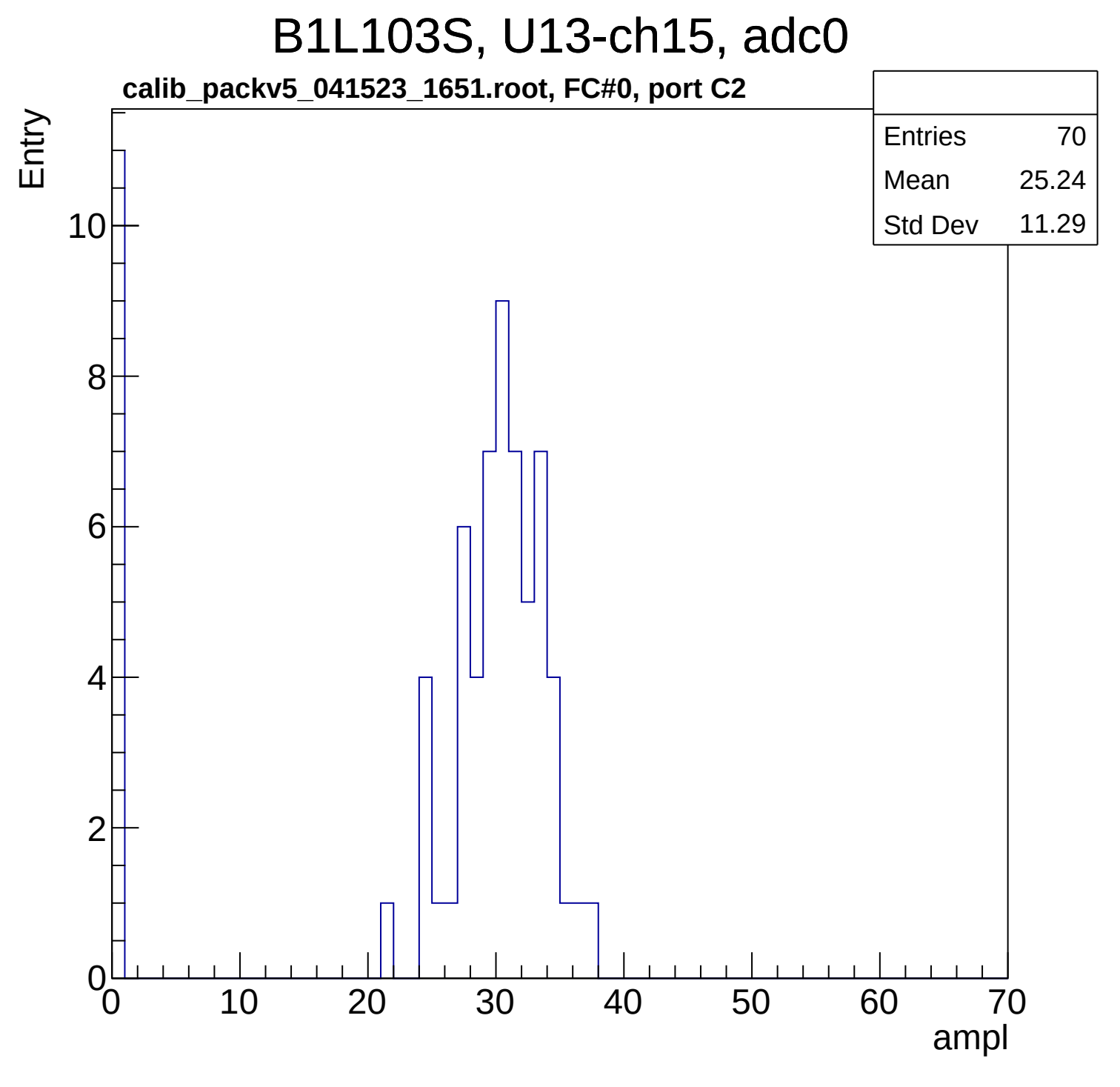
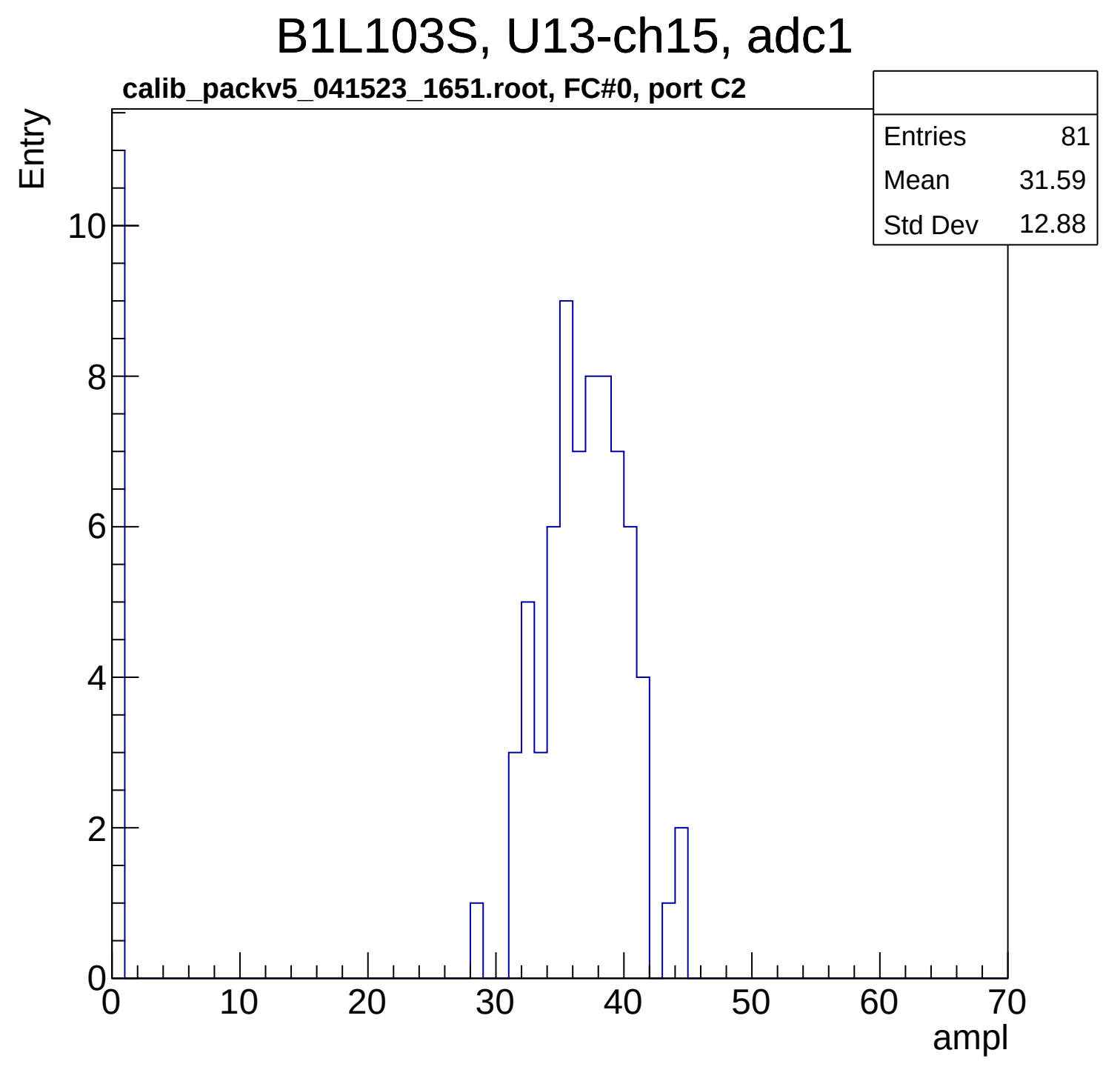
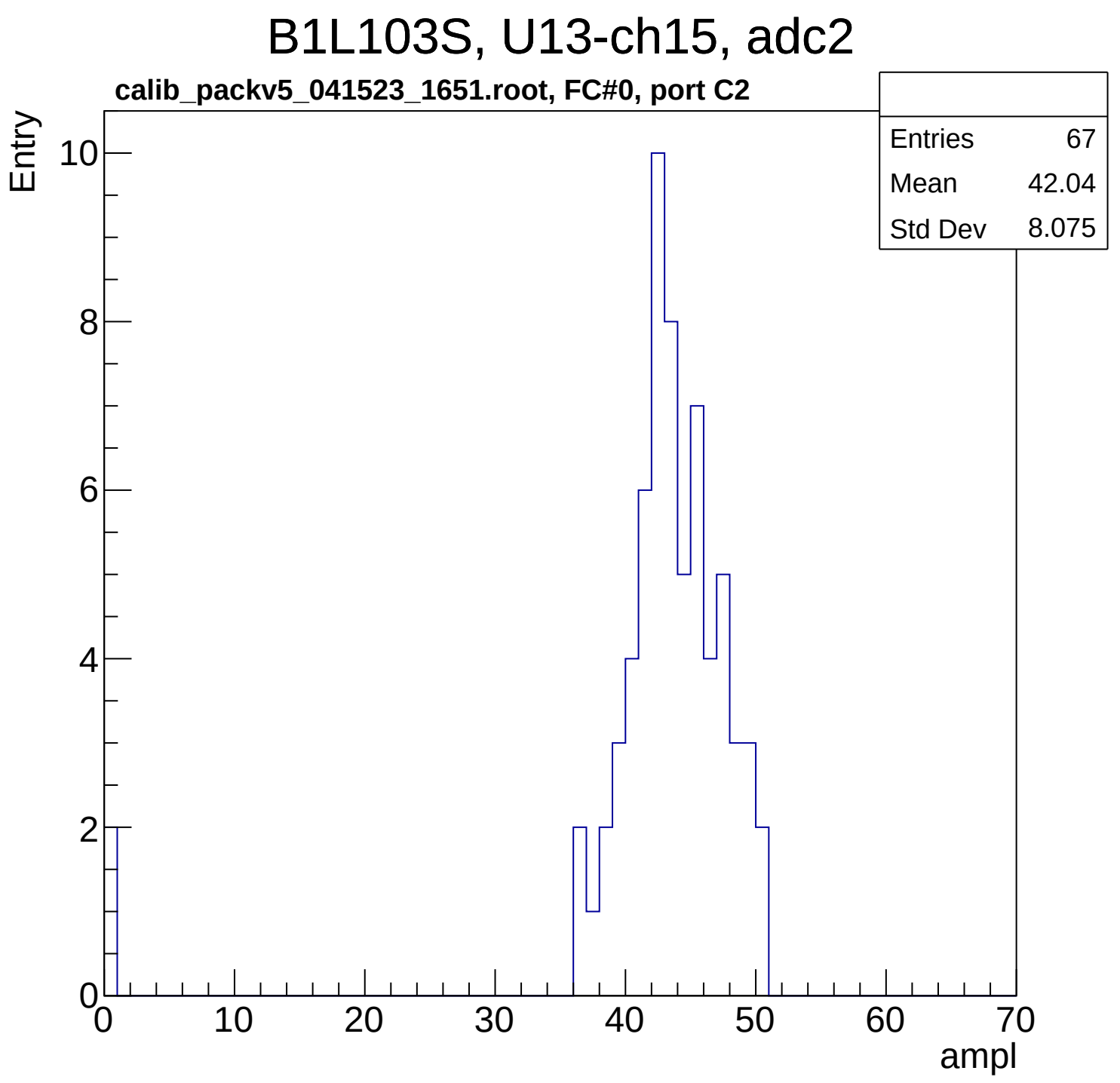
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

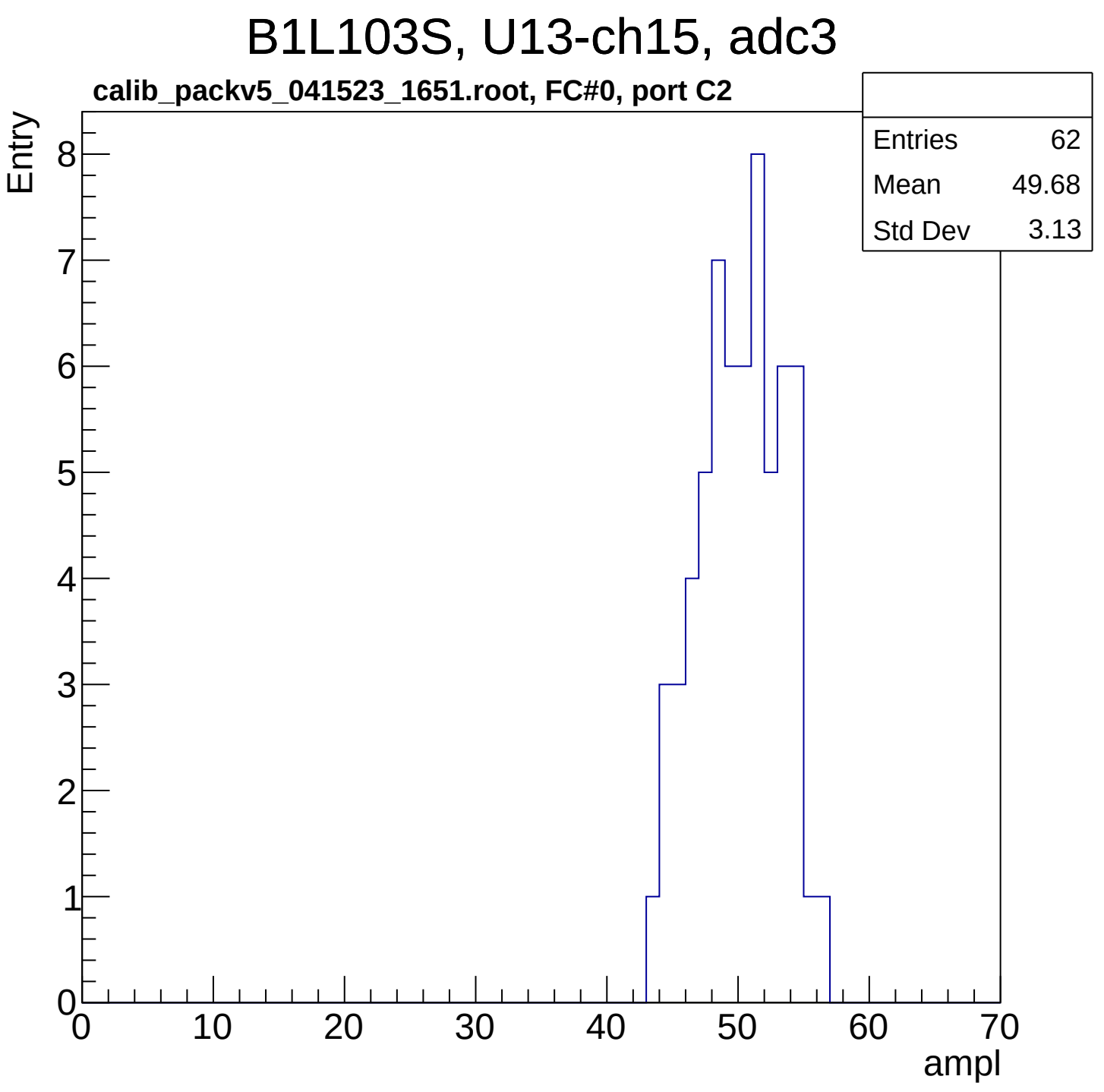

B1L103S, U13-ch14, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.8
Std Dev 0.7483
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

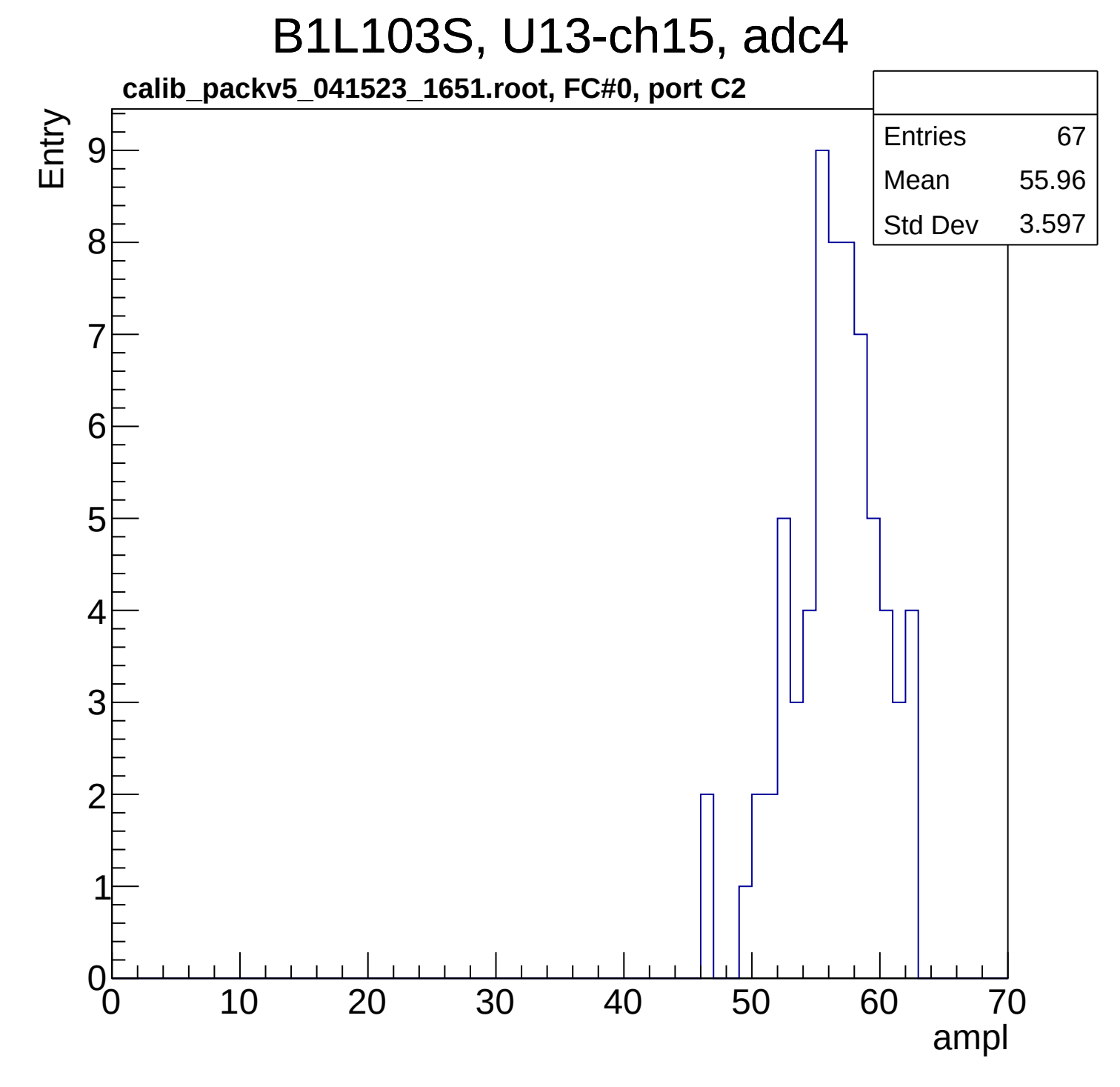

B1L103S, U13-ch14, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch15, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 25.24
Std Dev 11.29
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch15, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 31.59
Std Dev 12.88
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch15, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 42.04
Std Dev 8.075
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch15, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 49.68
Std Dev 3.13
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch15, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 55.96
Std Dev 3.597
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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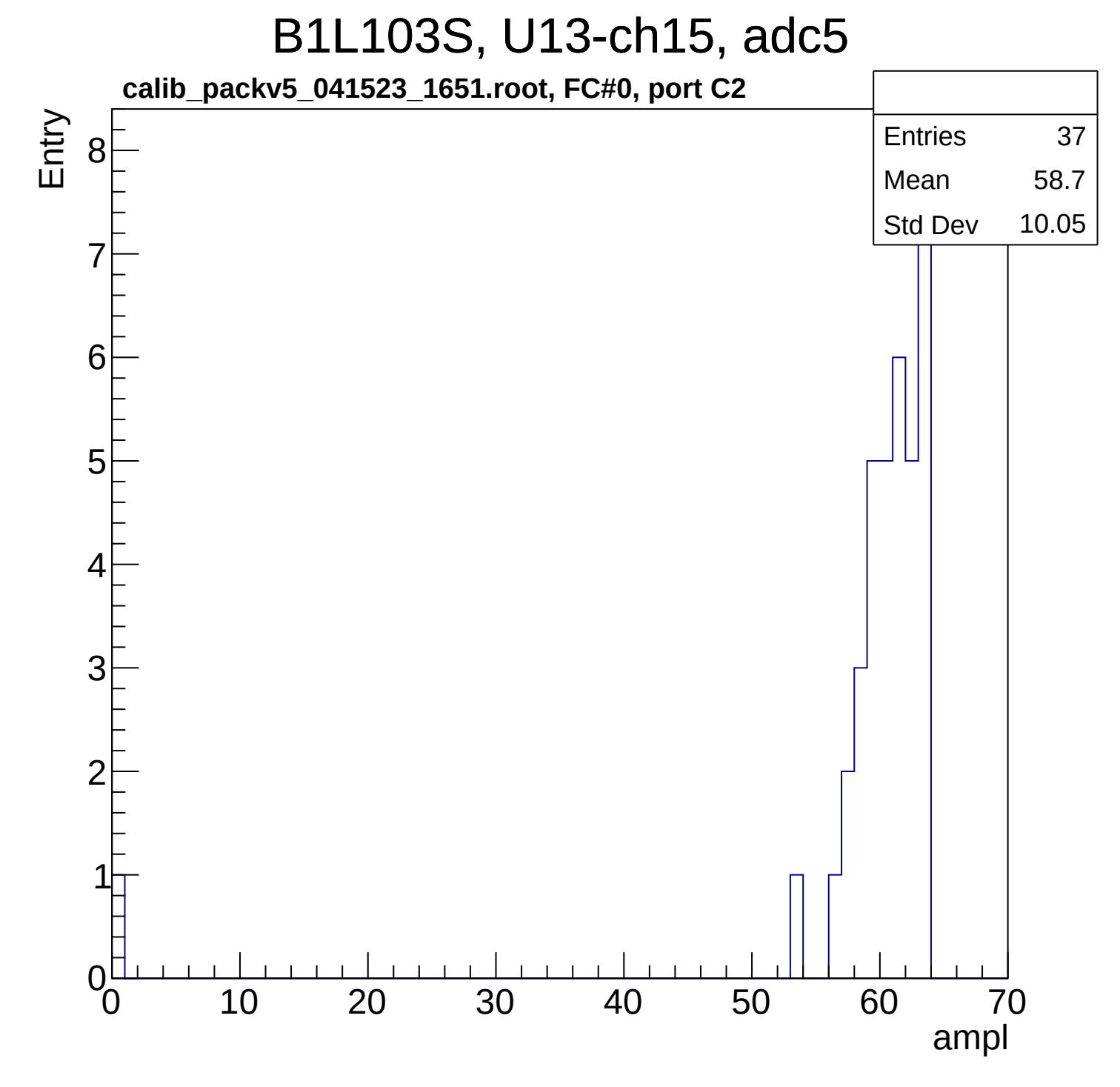
B1L103S, U13-ch15, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 58.7
Std Dev 10.05
Entry
ampl
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3
4
5
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7
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0
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60
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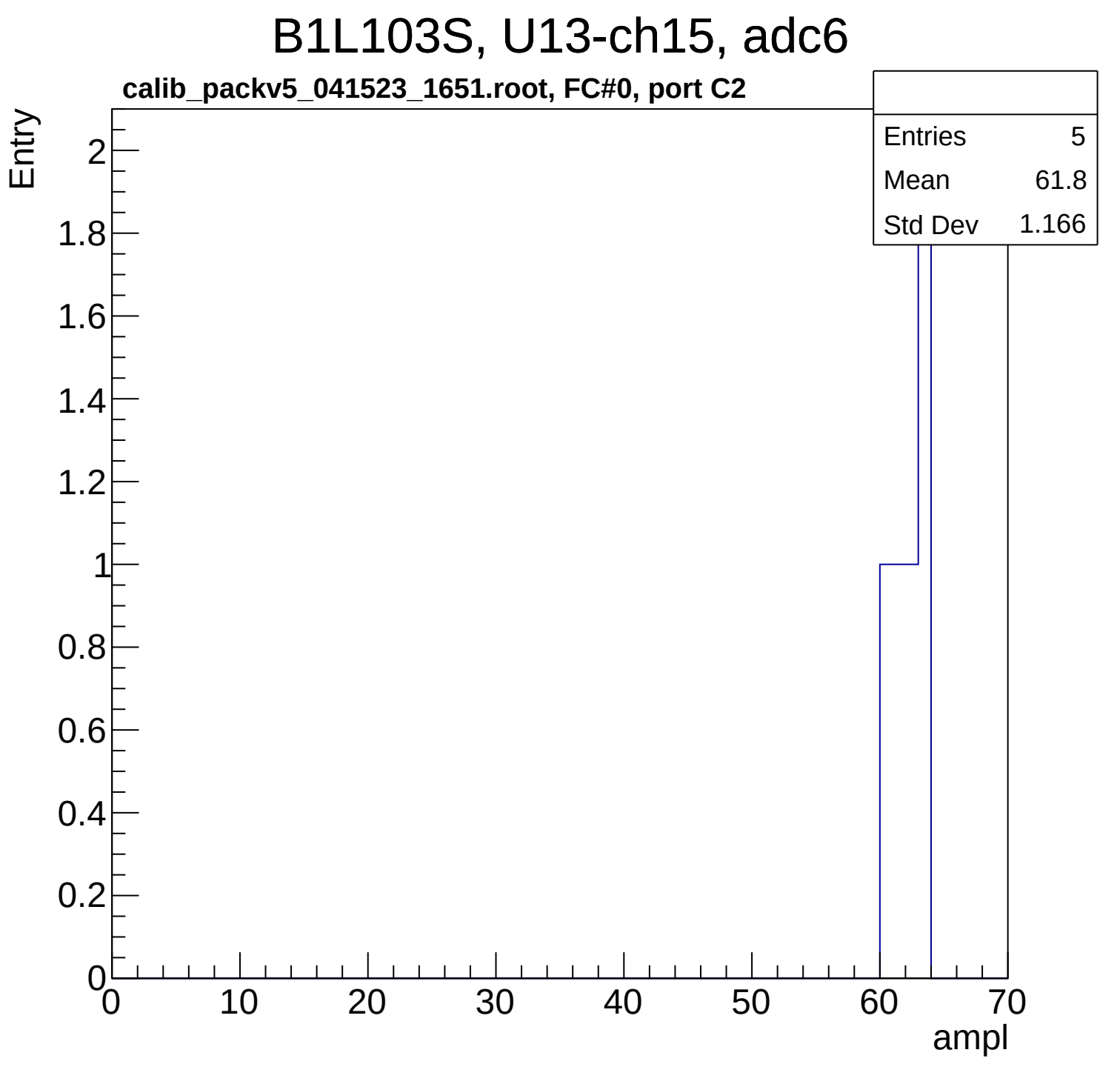
B1L103S, U13-ch15, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.8
Std Dev 1.166
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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40
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60
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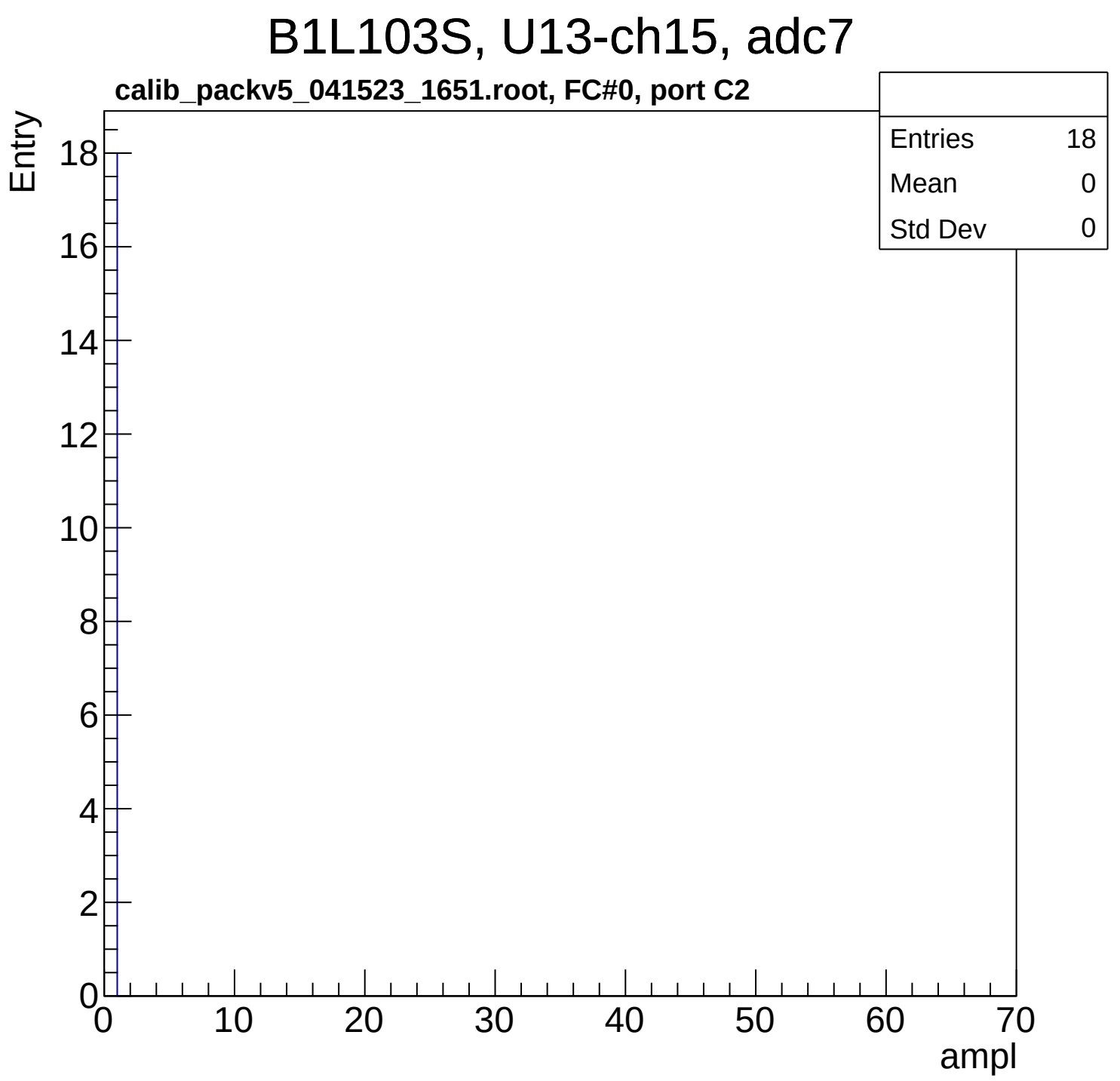
B1L103S, U13-ch15, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
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6
8
10
12
14
16
18
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50
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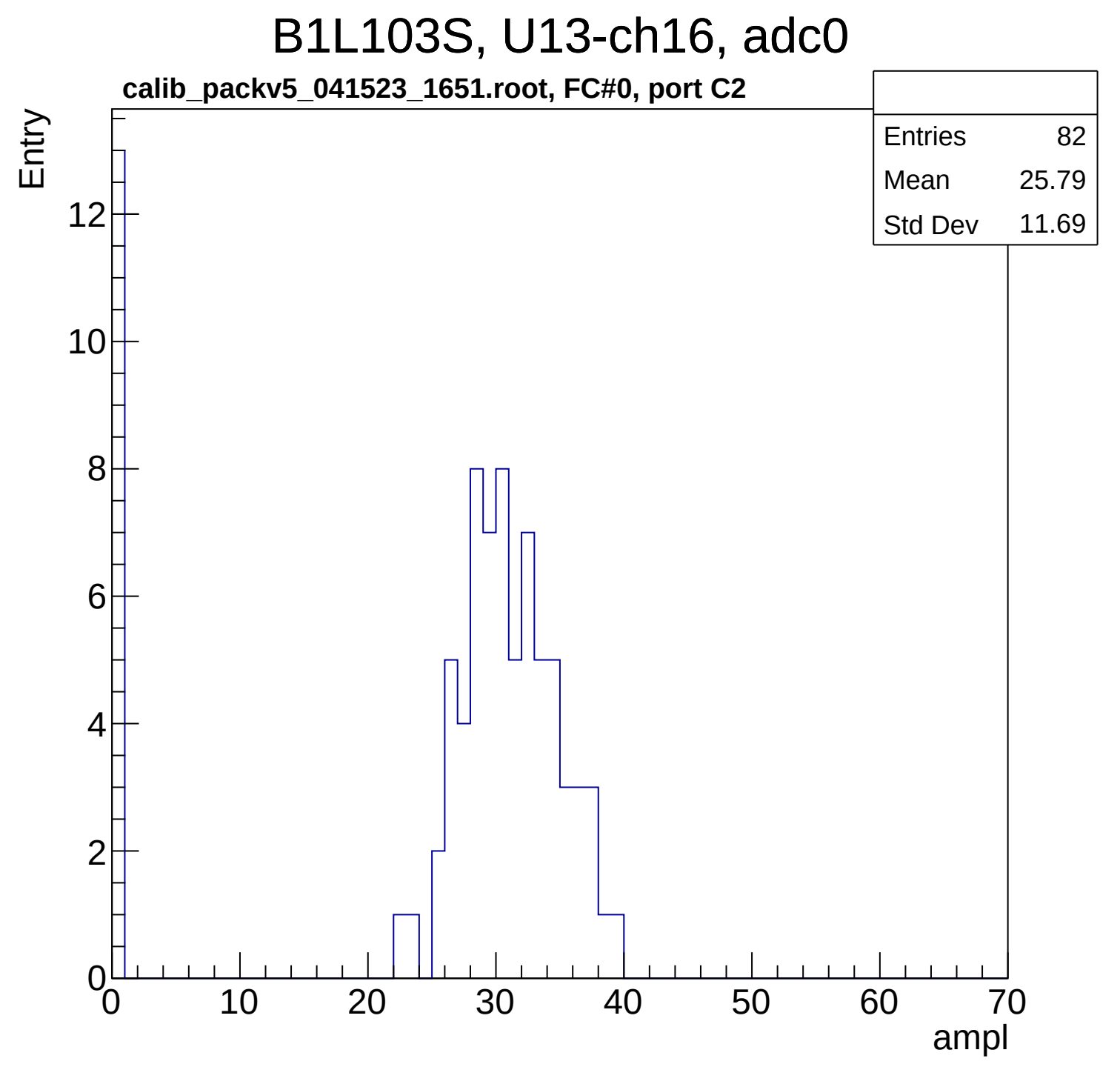
70
ampl


B1L103S, U13-ch16, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 25.79
Std Dev 11.69
Entry
0
2
4
6
8
10
12
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10
20
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50
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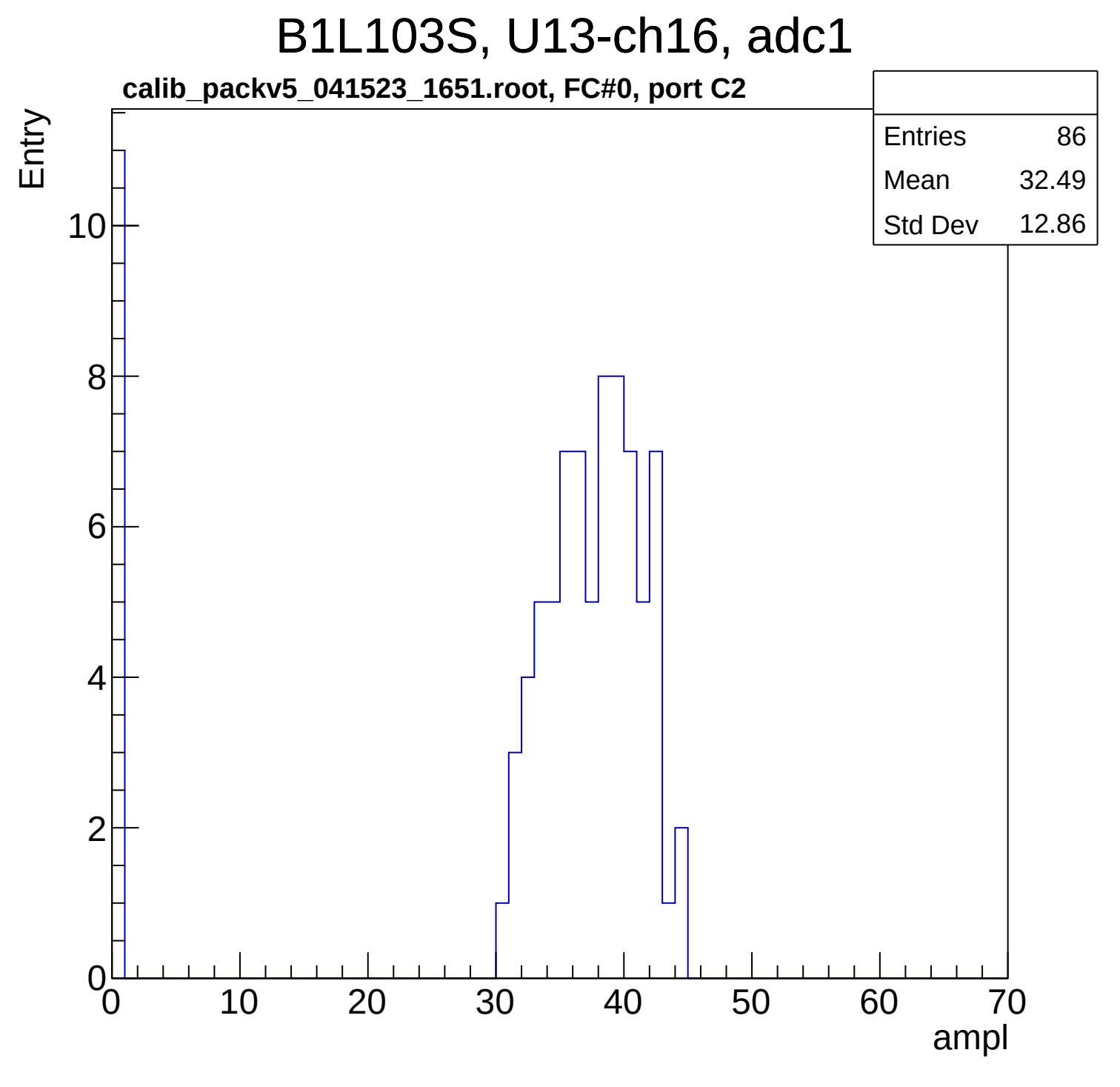
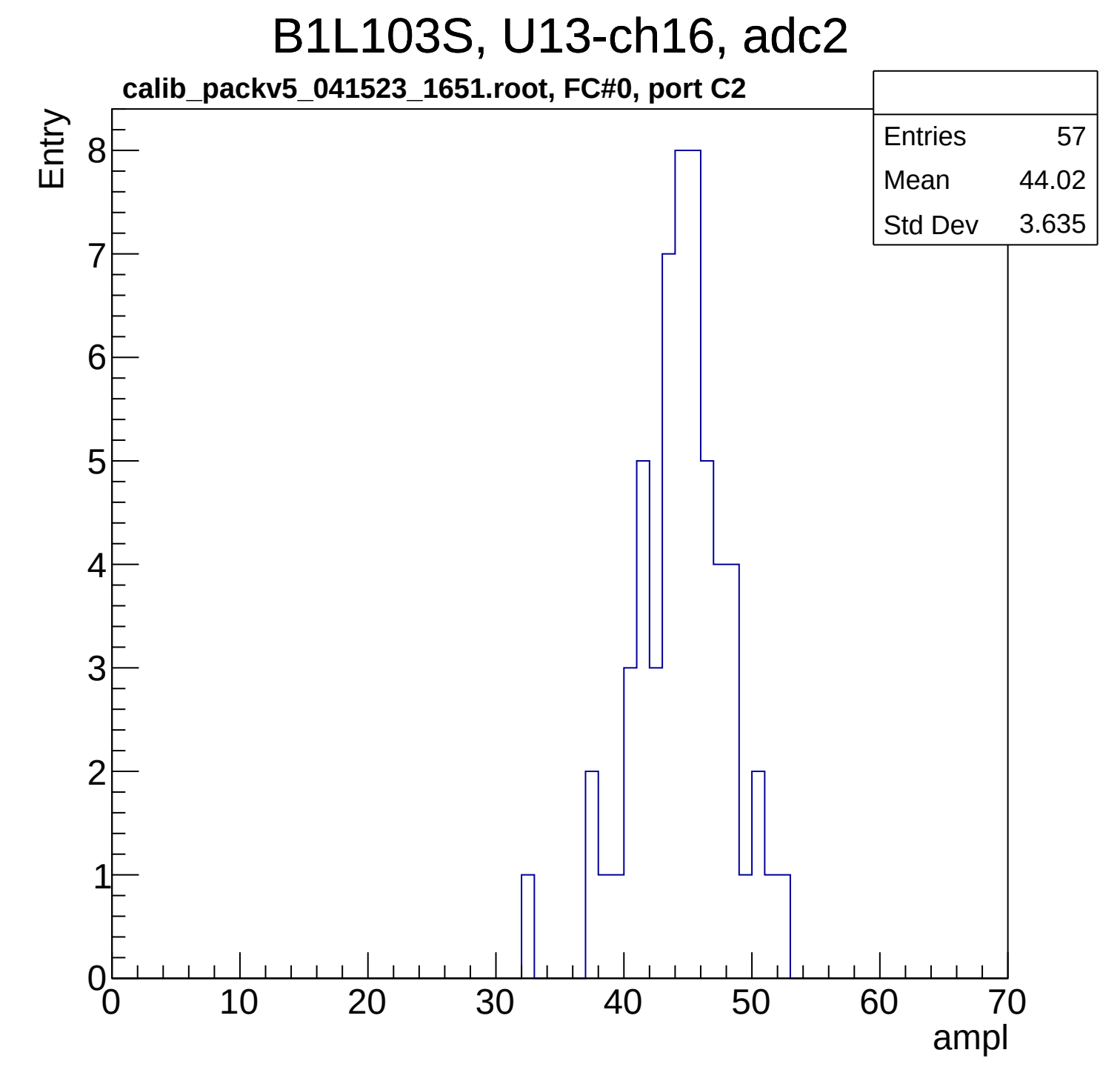
70
ampl


B1L103S, U13-ch16, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 32.49
Std Dev 12.86
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch16, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 44.02
Std Dev 3.635
Entry
ampl
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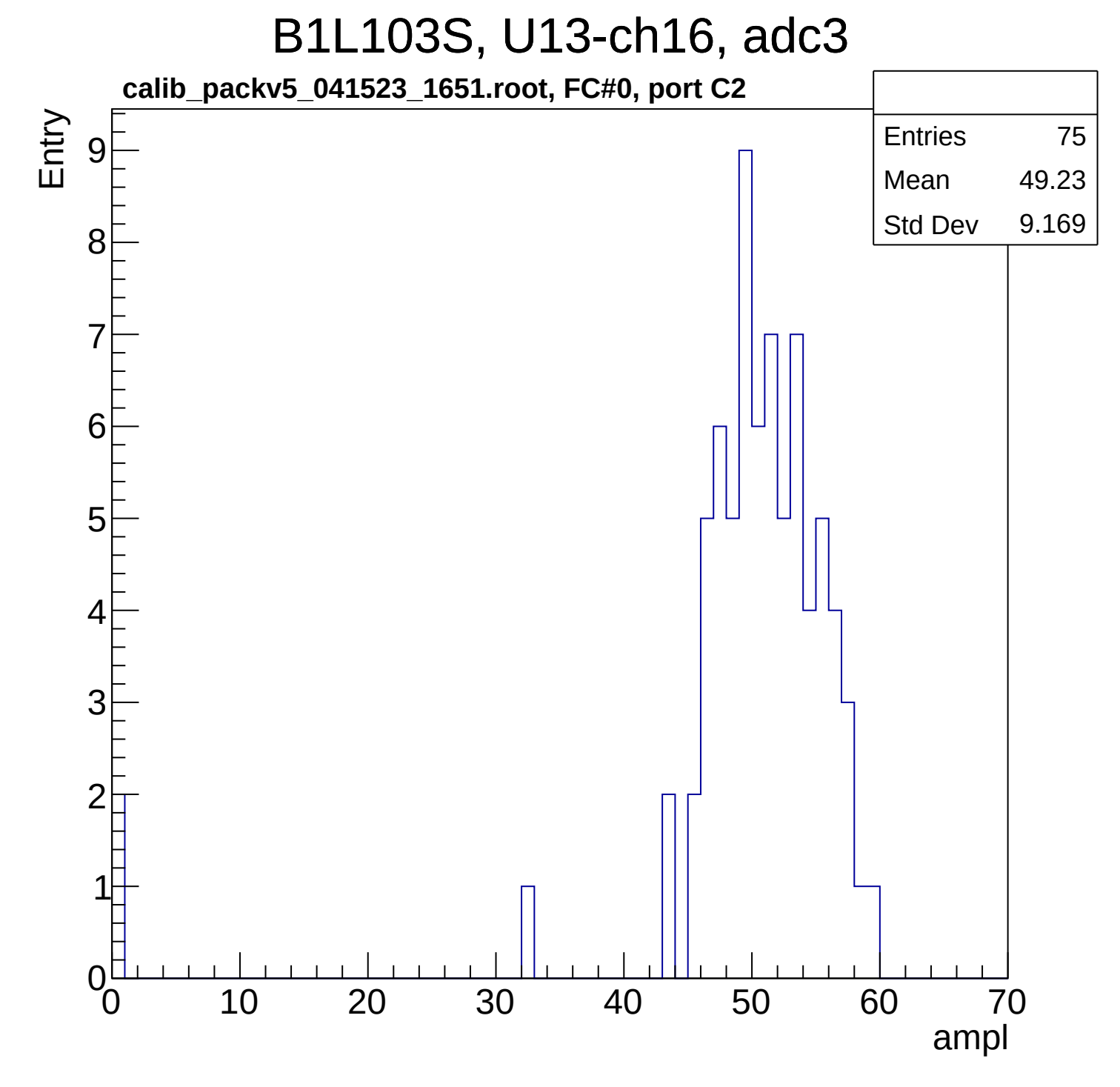
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch16, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 49.23
Std Dev 9.169
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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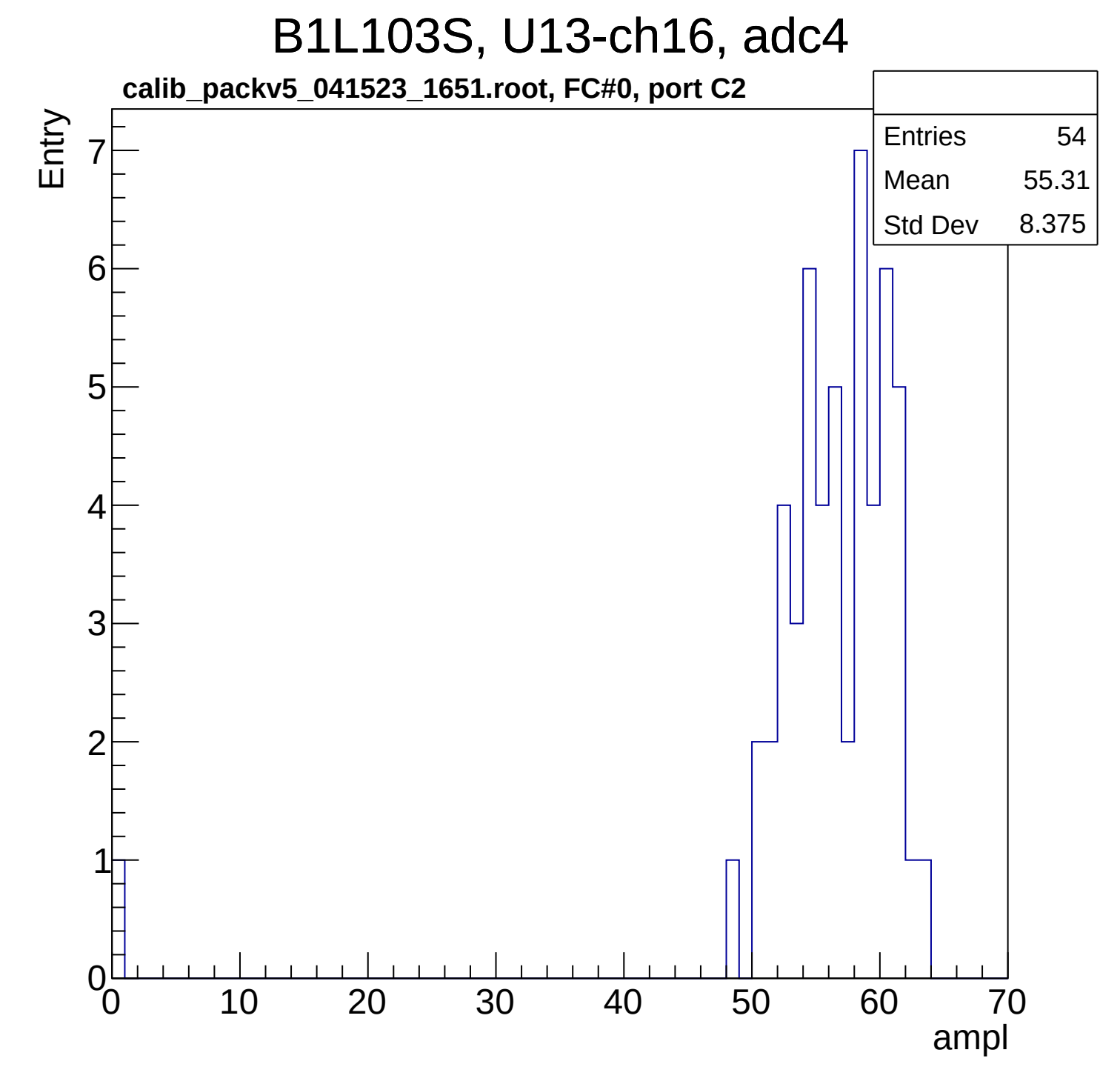
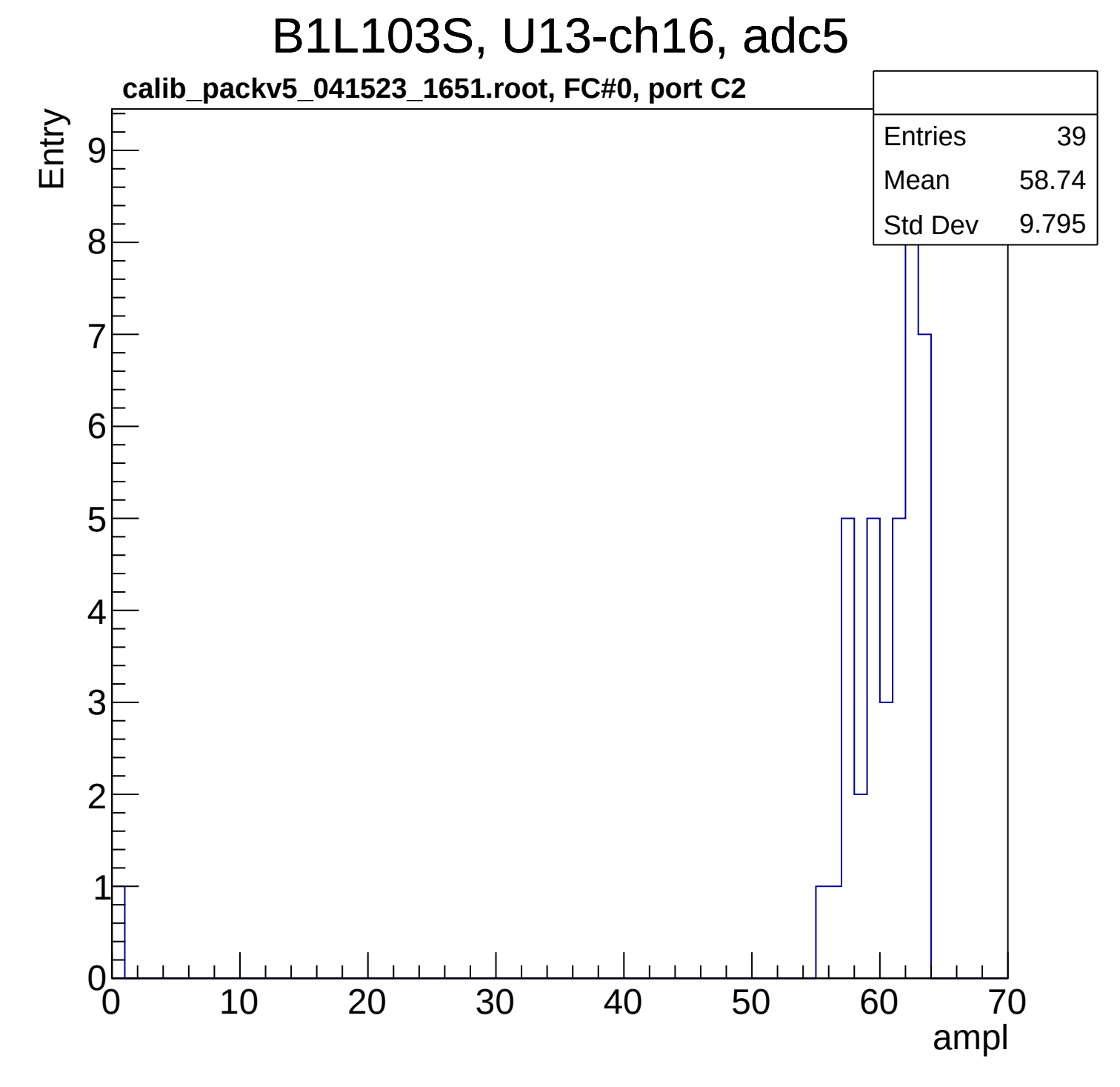
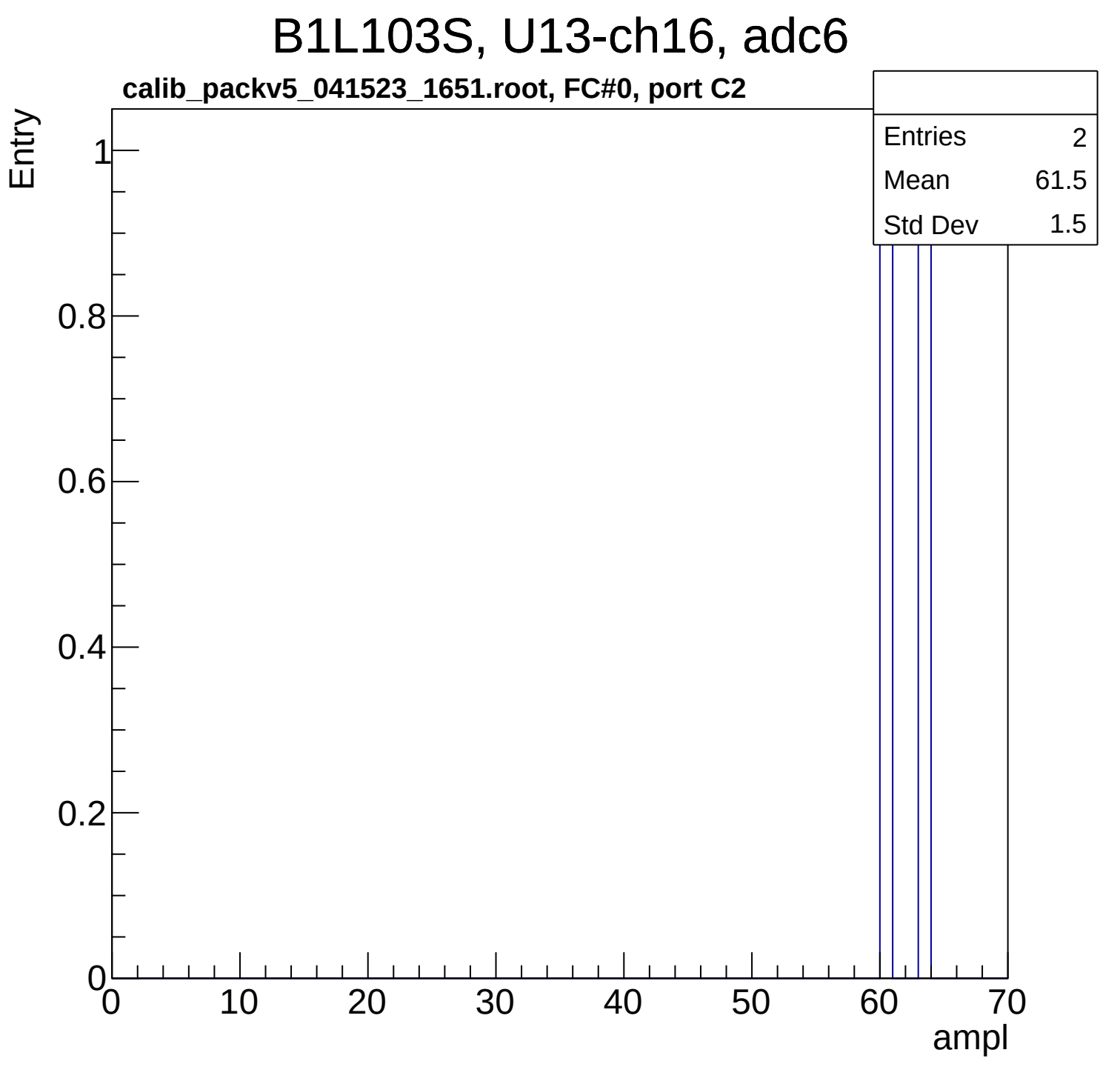
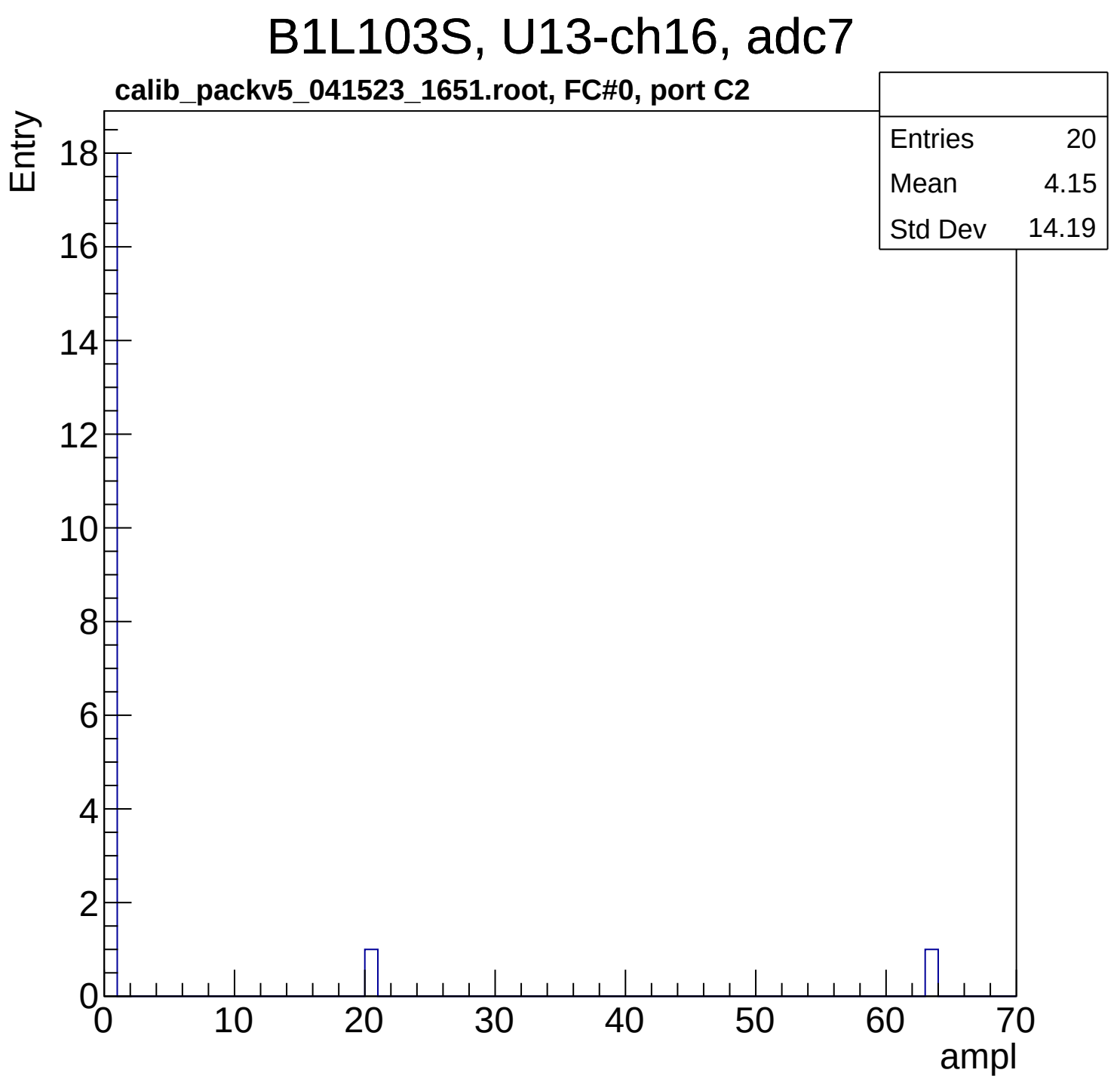
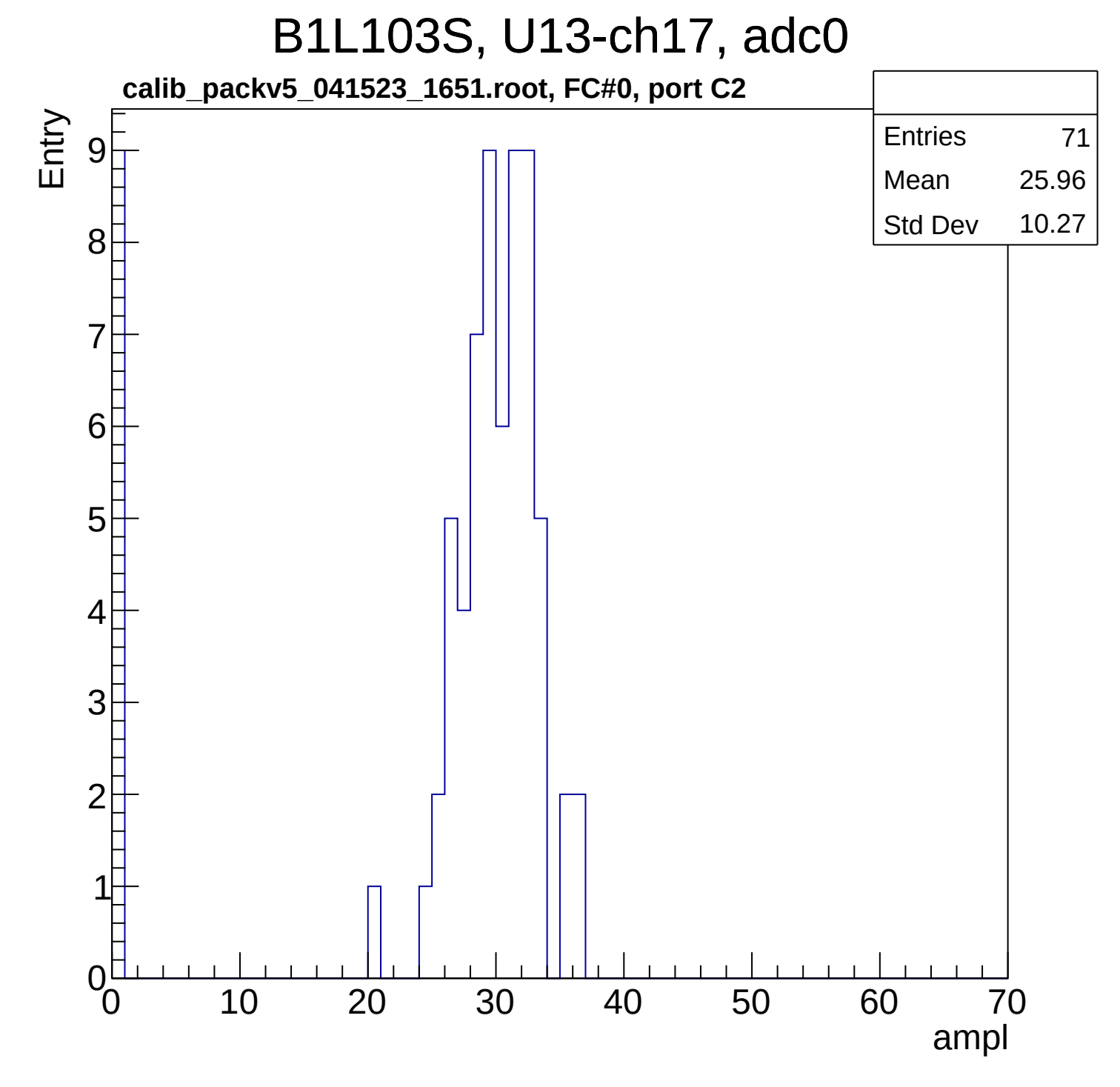

B1L103S, U13-ch16, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 55.31
Std Dev 8.375
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch16, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 58.74
Std Dev 9.795
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U13-ch16, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 61.5
Std Dev 1.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch16, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.15
Std Dev 14.19
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch17, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 25.96
Std Dev 10.27
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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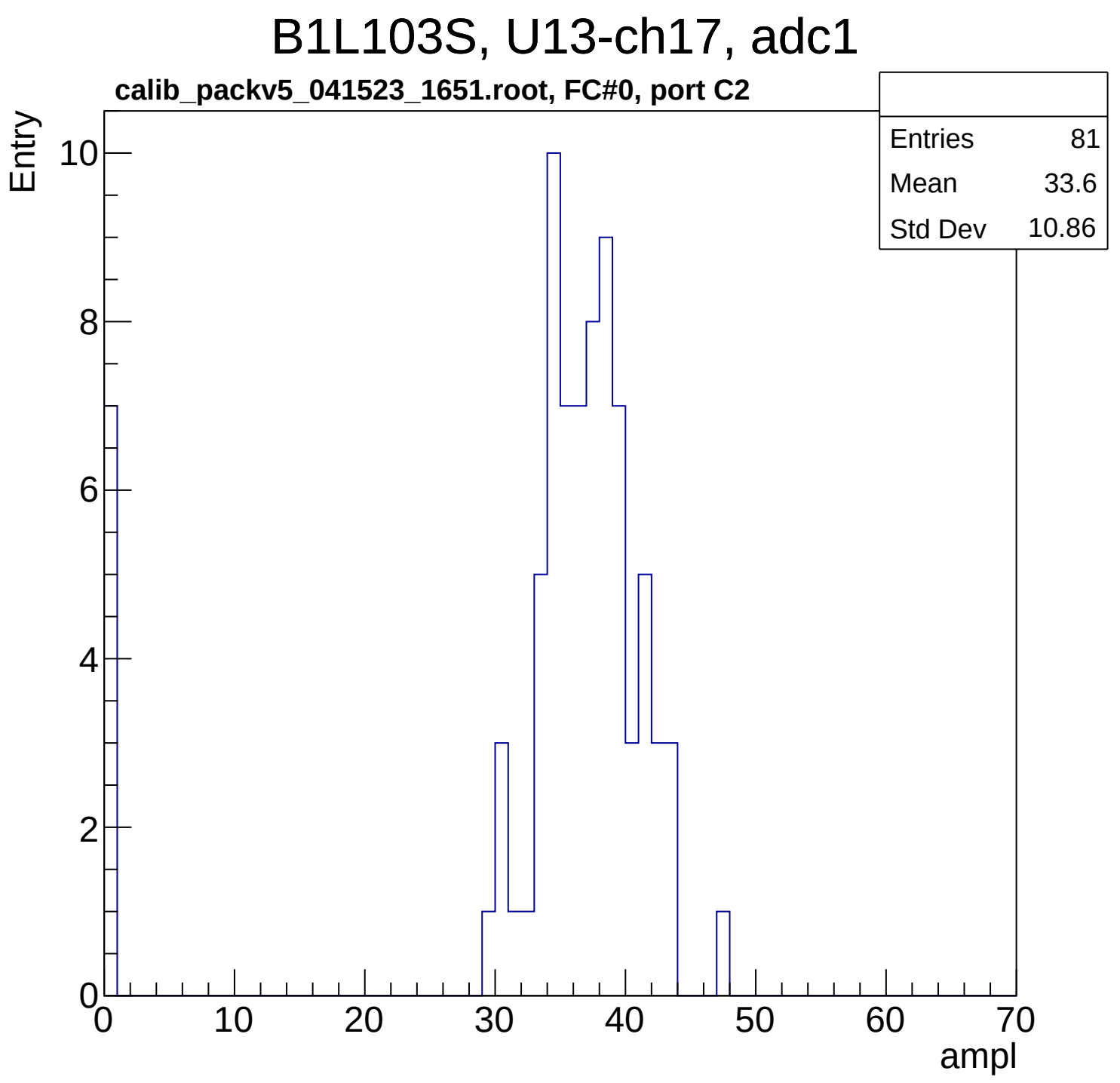
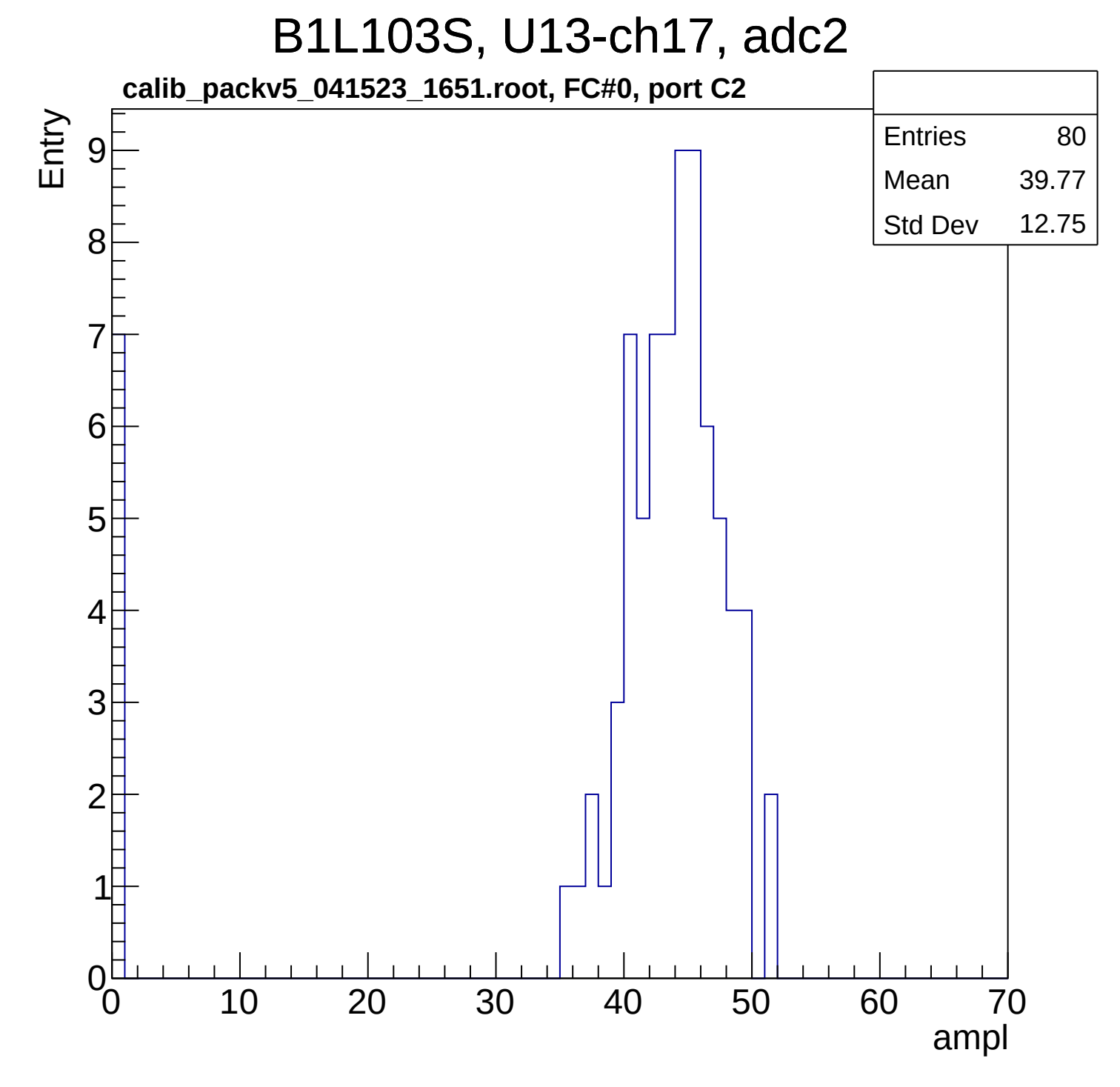
40
50
60
70


B1L103S, U13-ch17, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 33.6
Std Dev 10.86
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch17, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 39.77
Std Dev 12.75
Entry
ampl
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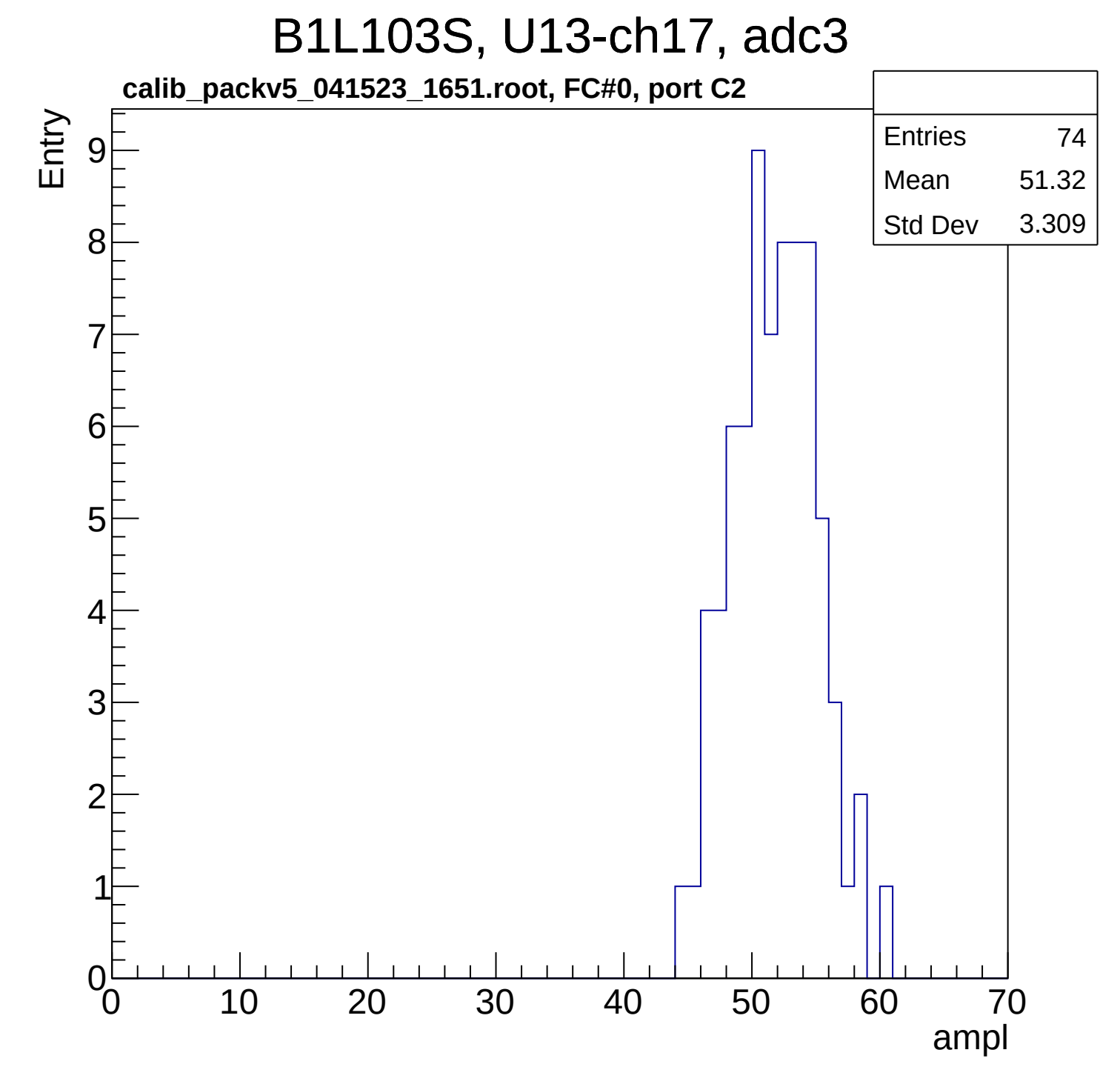
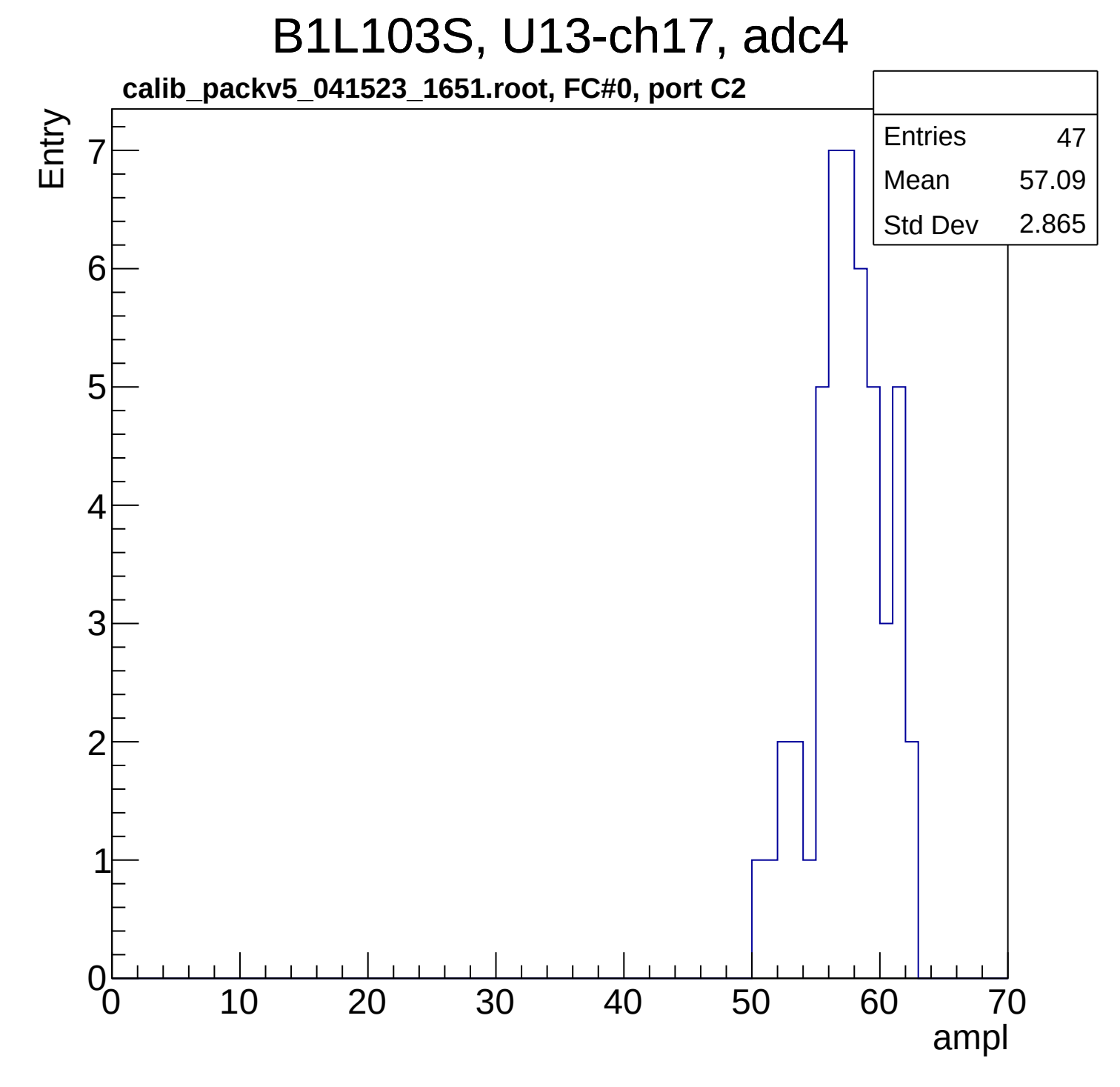
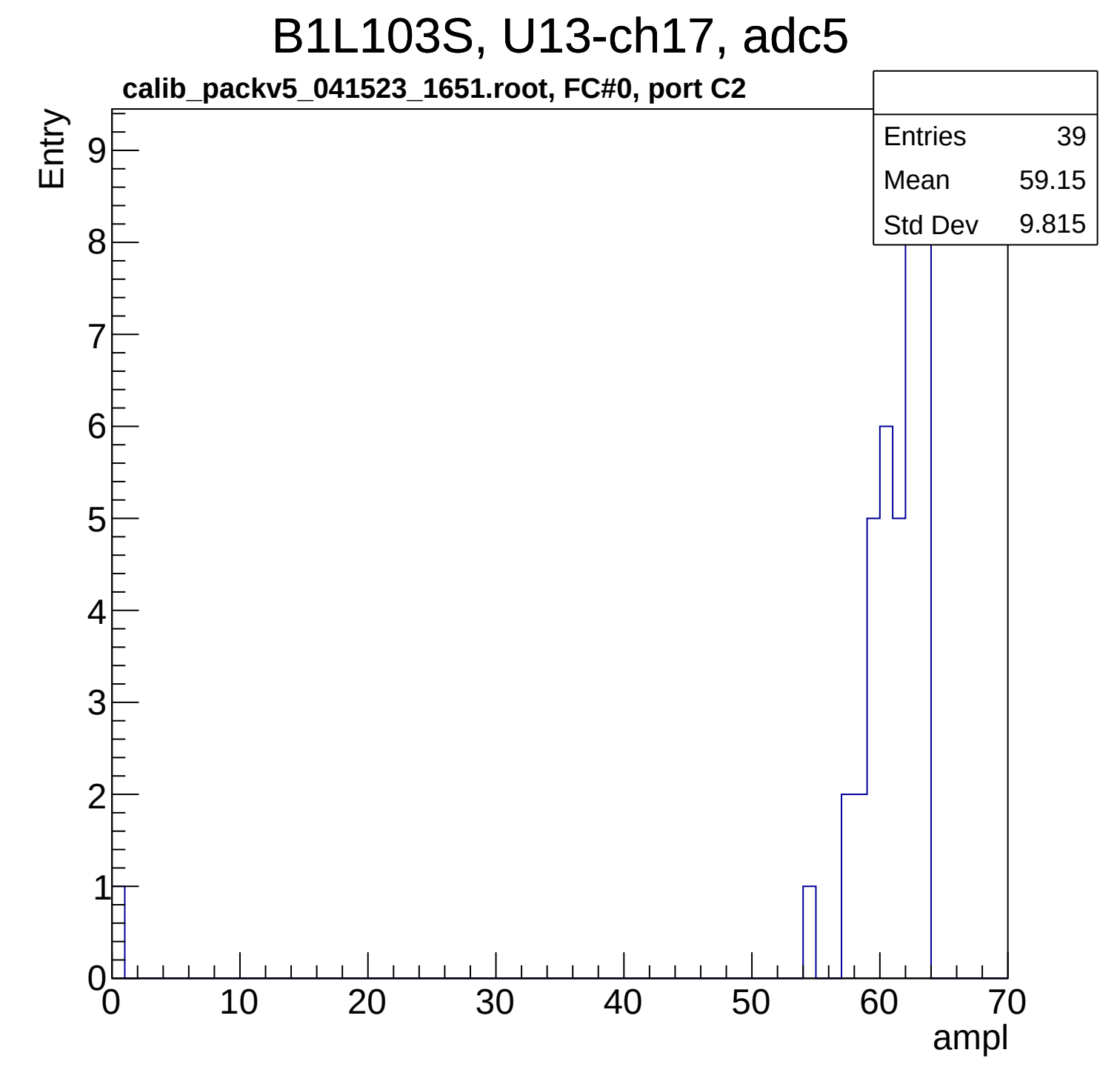
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch17, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 51.32
Std Dev 3.309
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch17, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 57.09
Std Dev 2.865
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch17, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 59.15
Std Dev 9.815
Entry
ampl
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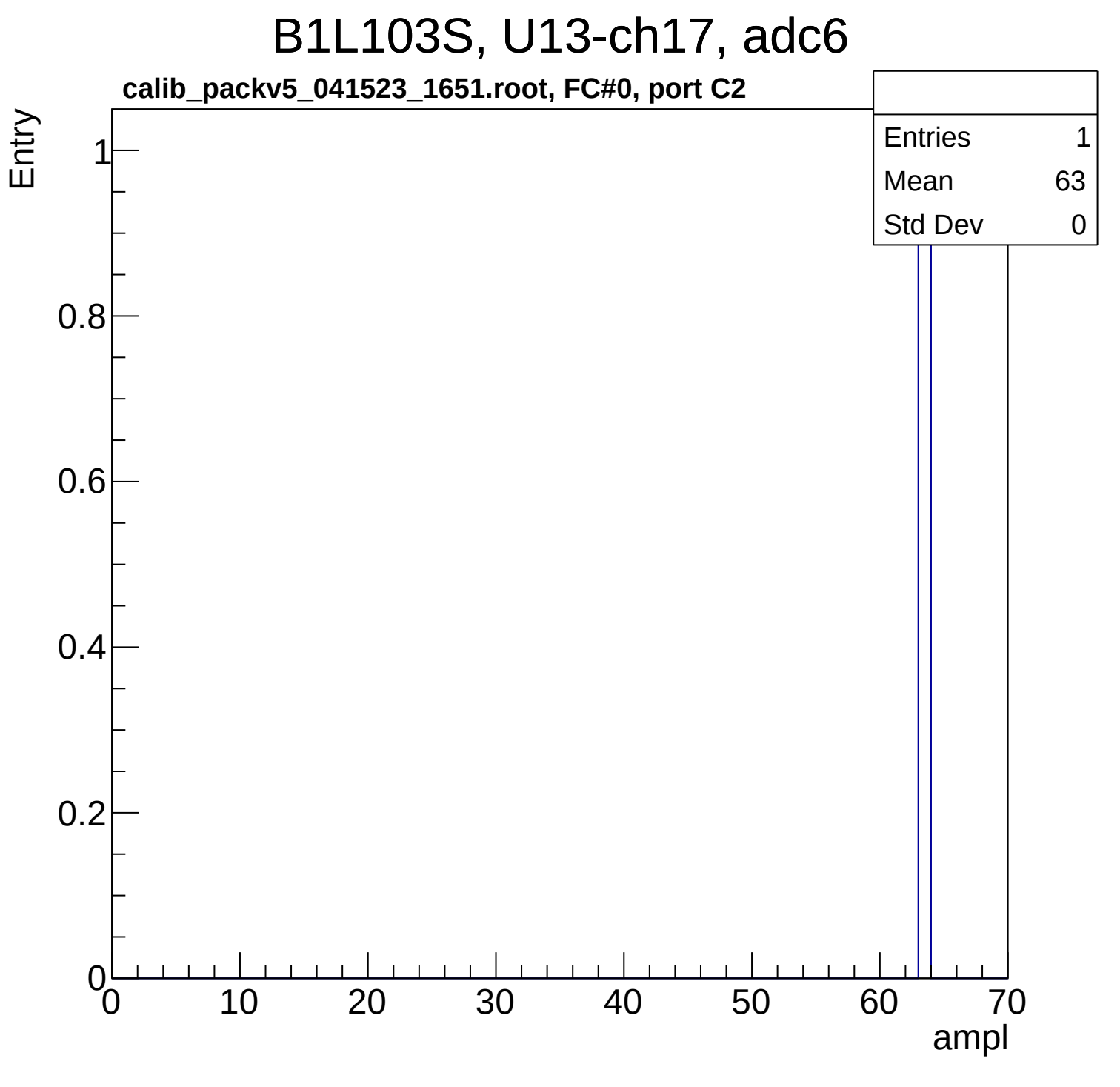
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch17, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 63
Std Dev 0
Entry
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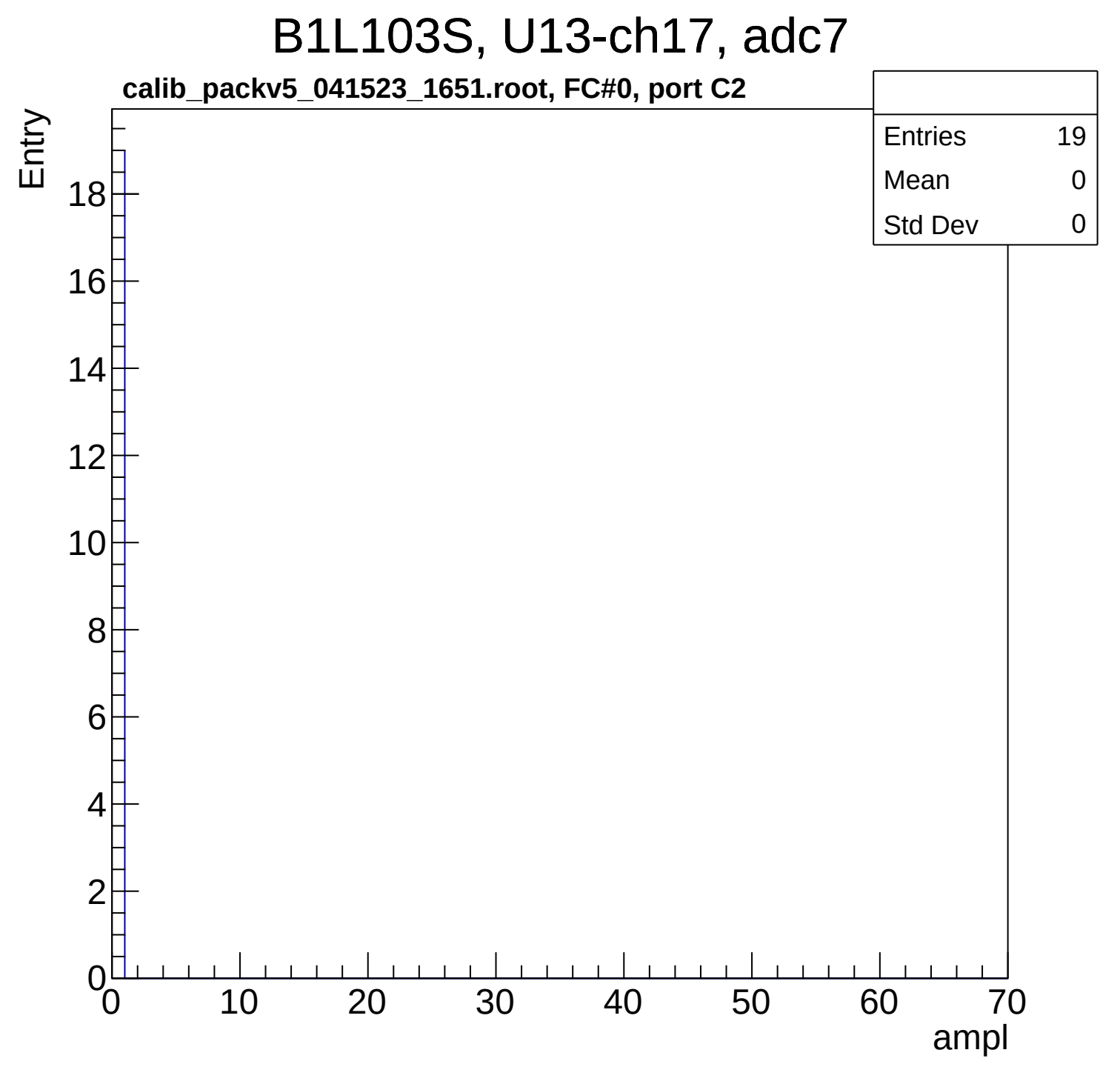
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch17, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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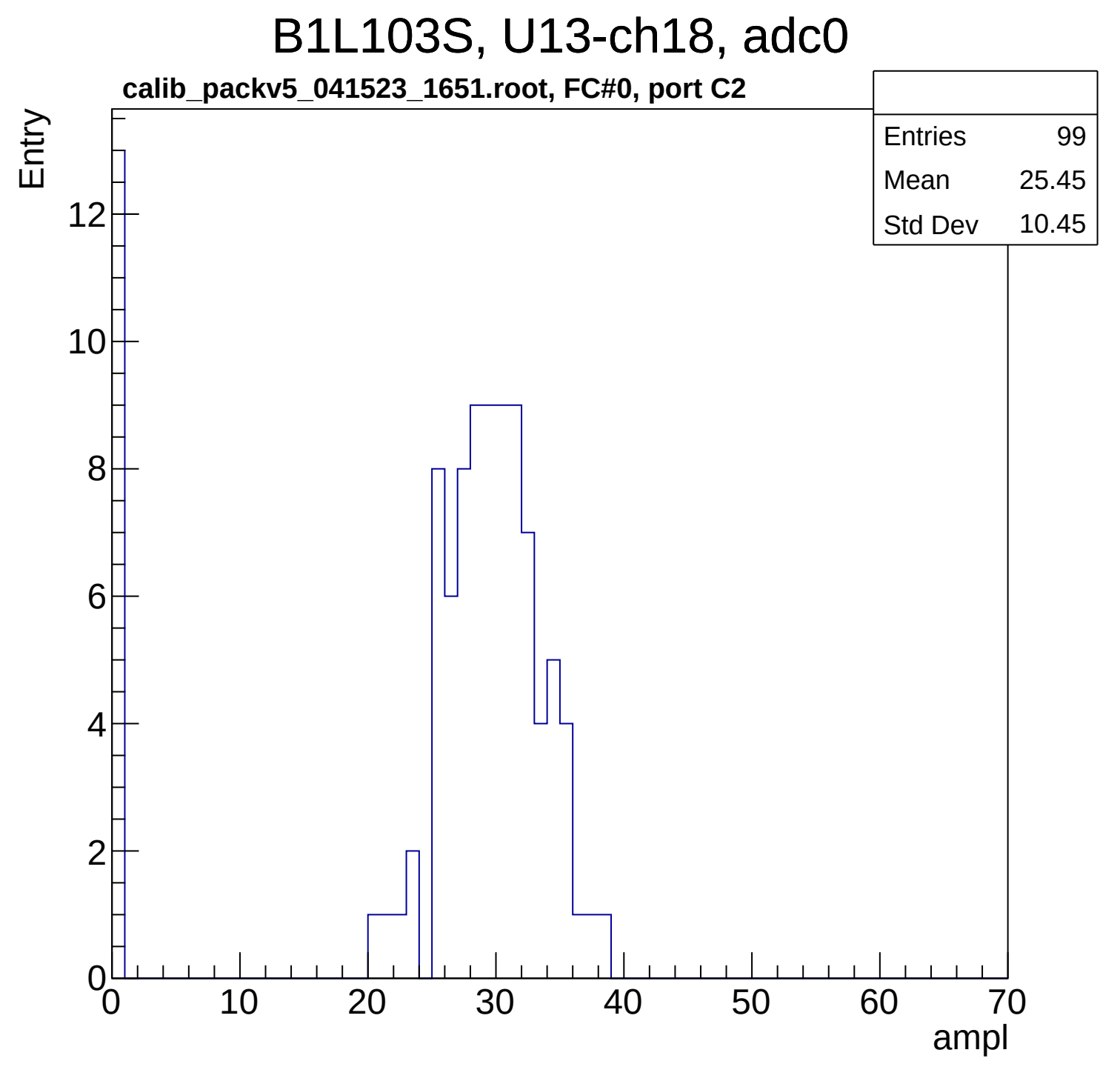
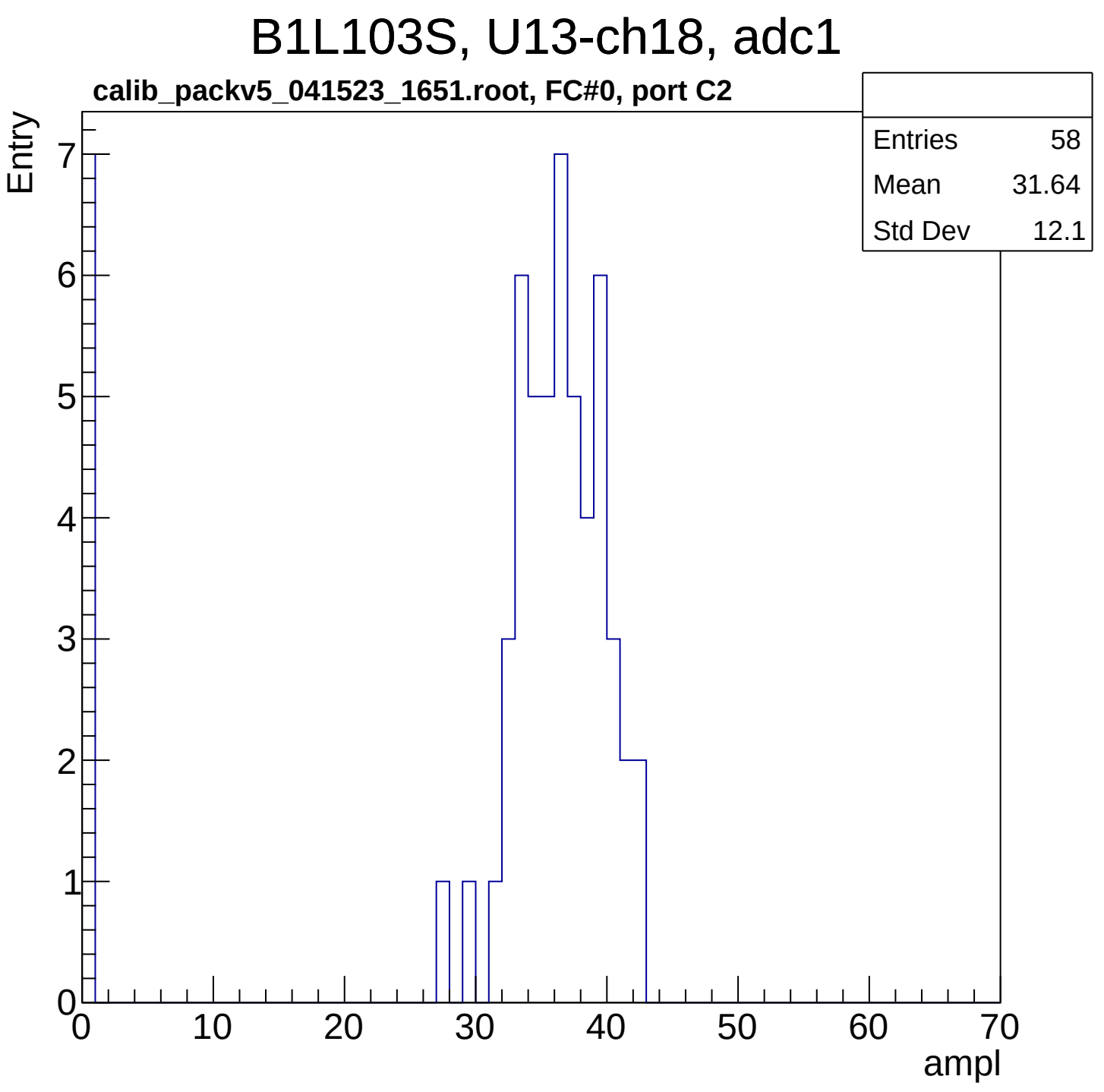
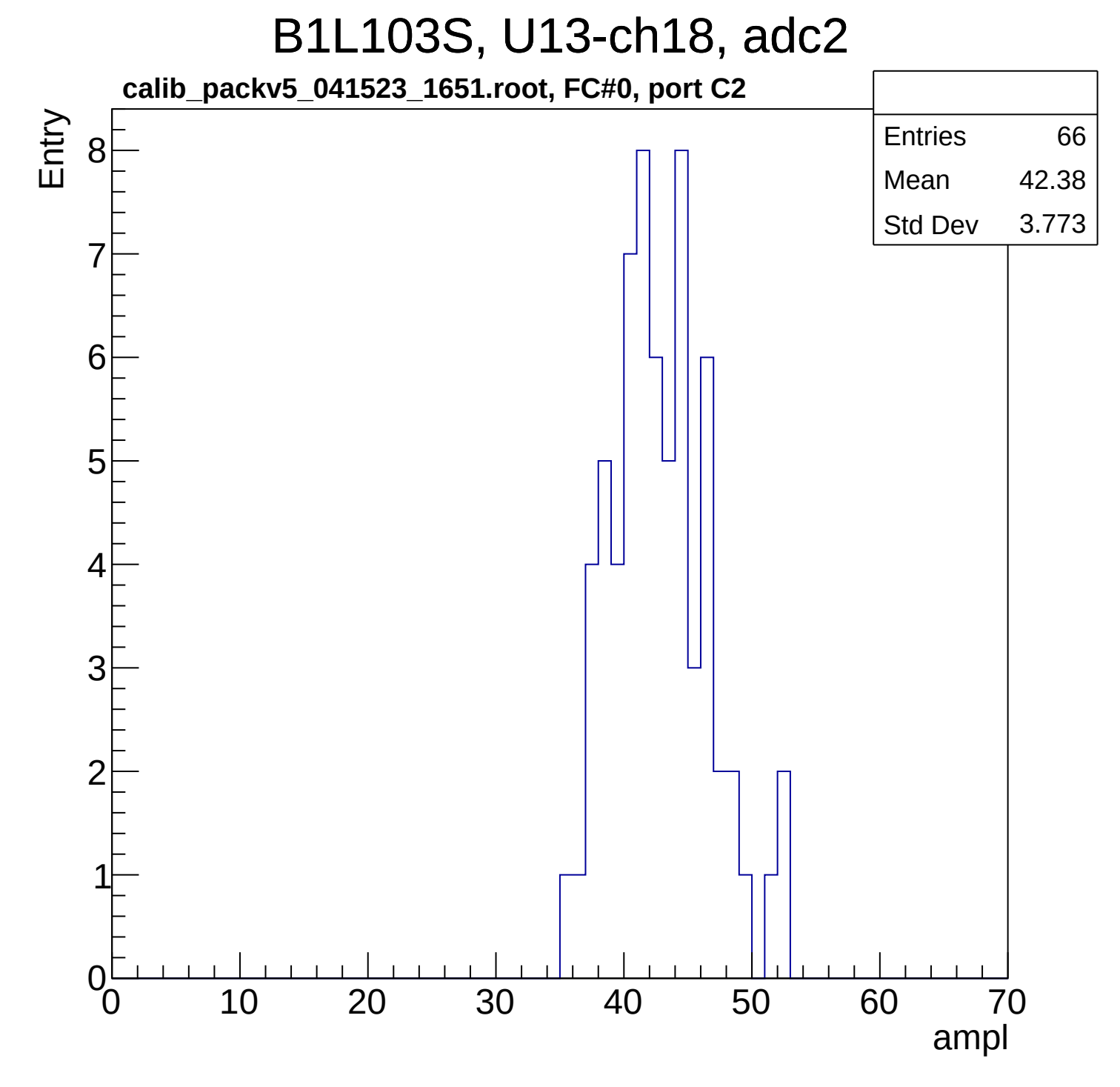
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch18, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 25.45
Std Dev 10.45
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch18, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 31.64
Std Dev 12.1
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch18, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 42.38
Std Dev 3.773
Entry
ampl
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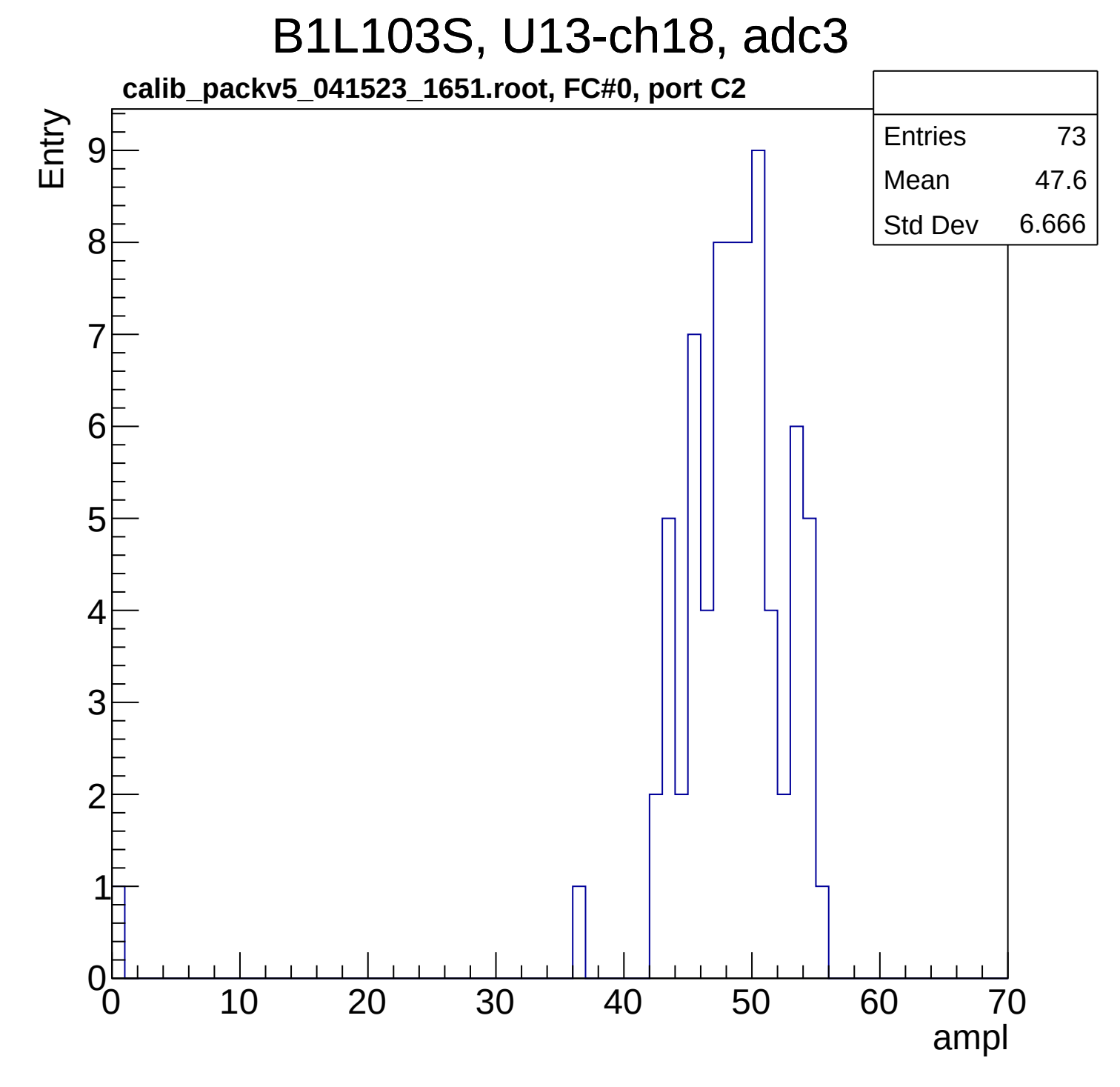
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch18, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 47.6
Std Dev 6.666
Entry
ampl
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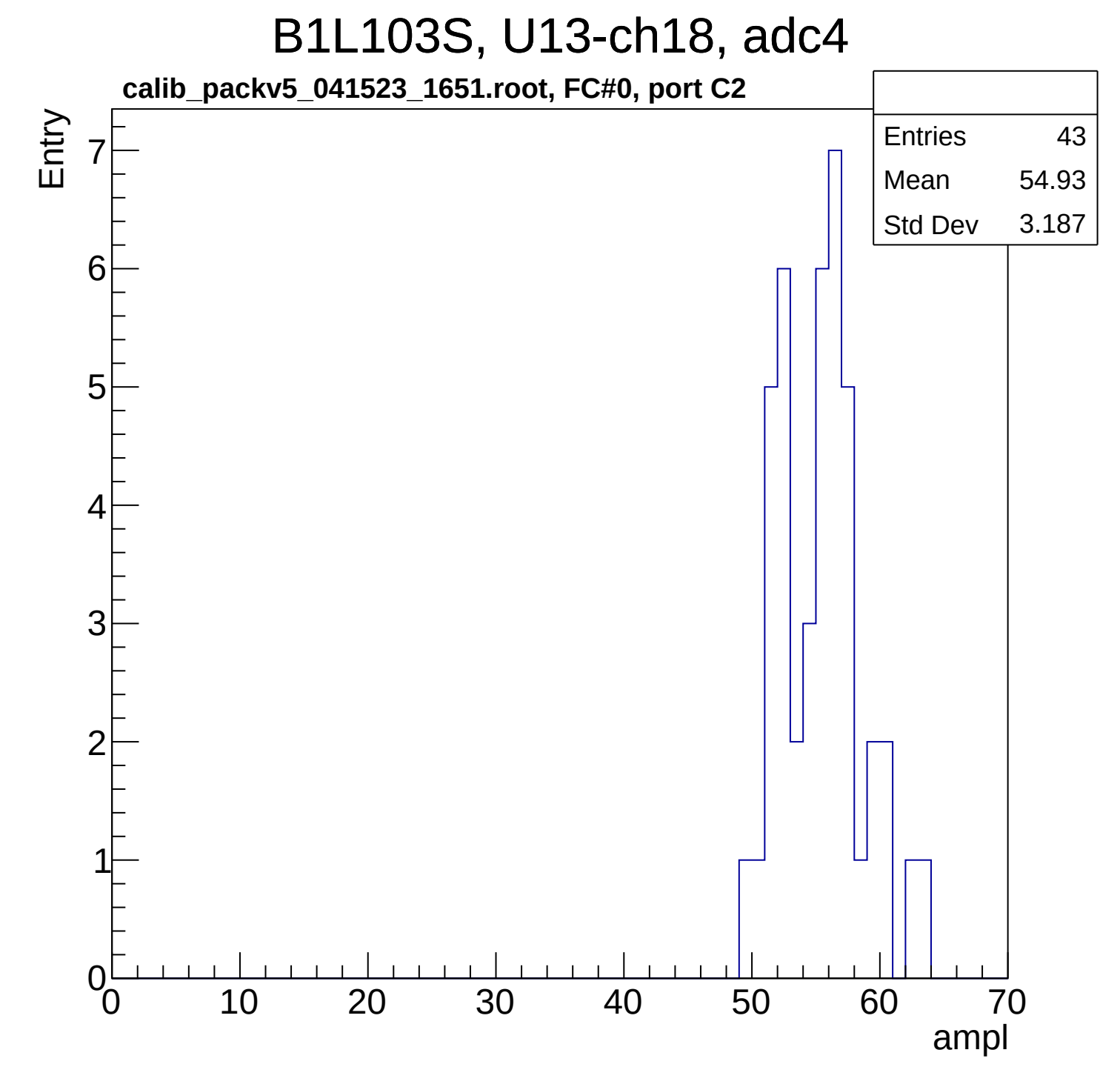
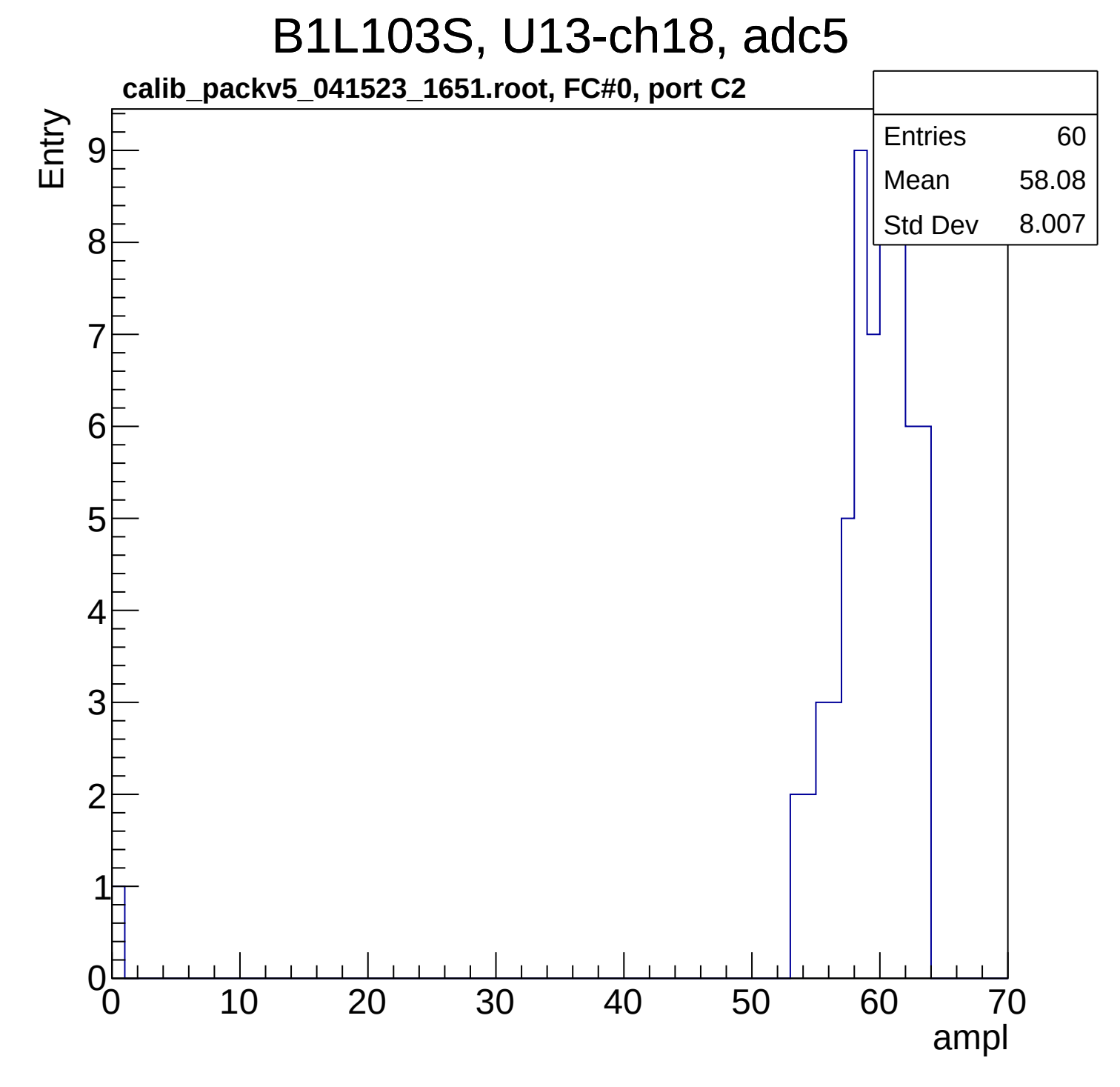
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch18, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 54.93
Std Dev 3.187
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch18, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 58.08
Std Dev 8.007
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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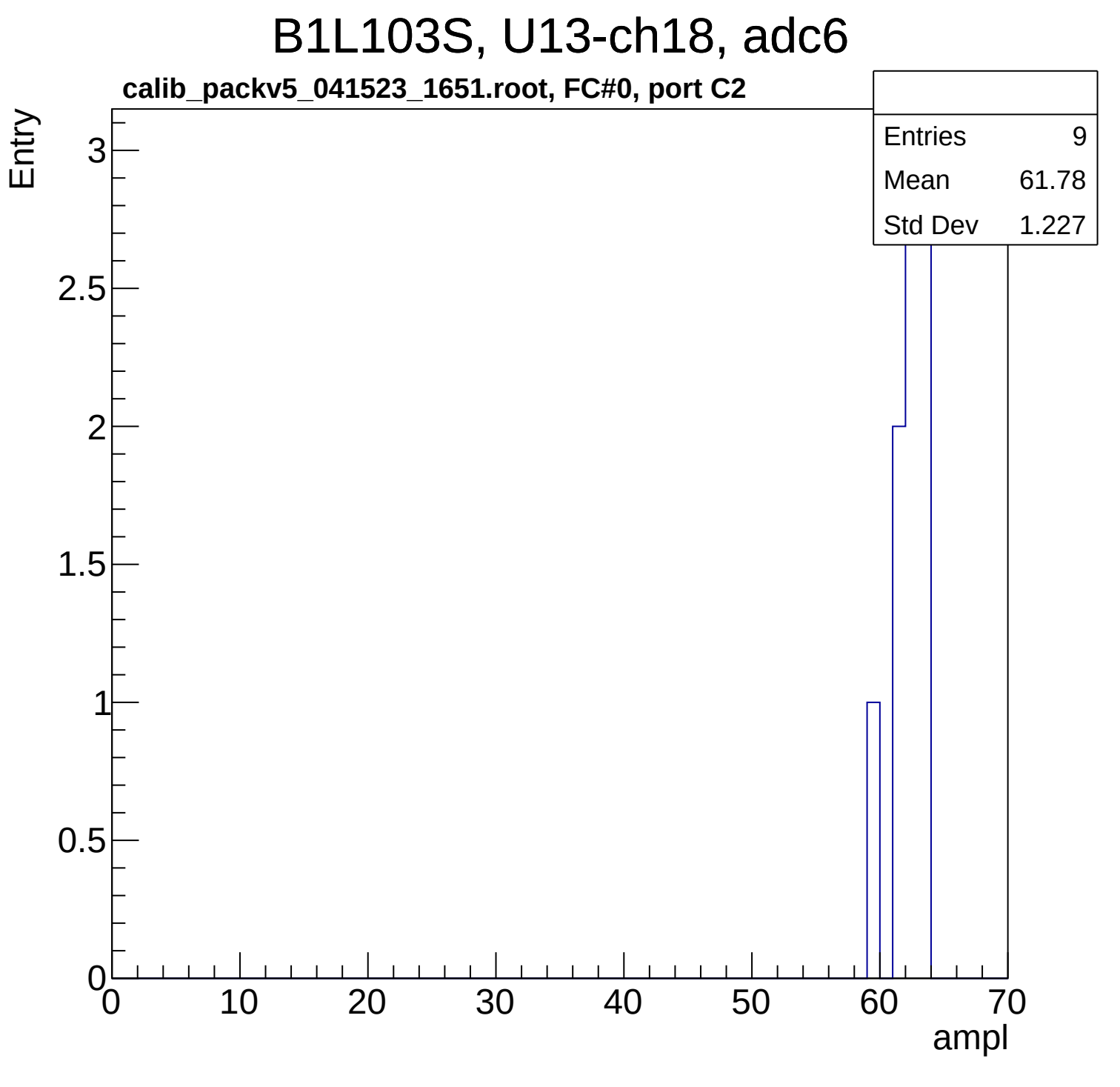
B1L103S, U13-ch18, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.78
Std Dev 1.227
Entry
ampl
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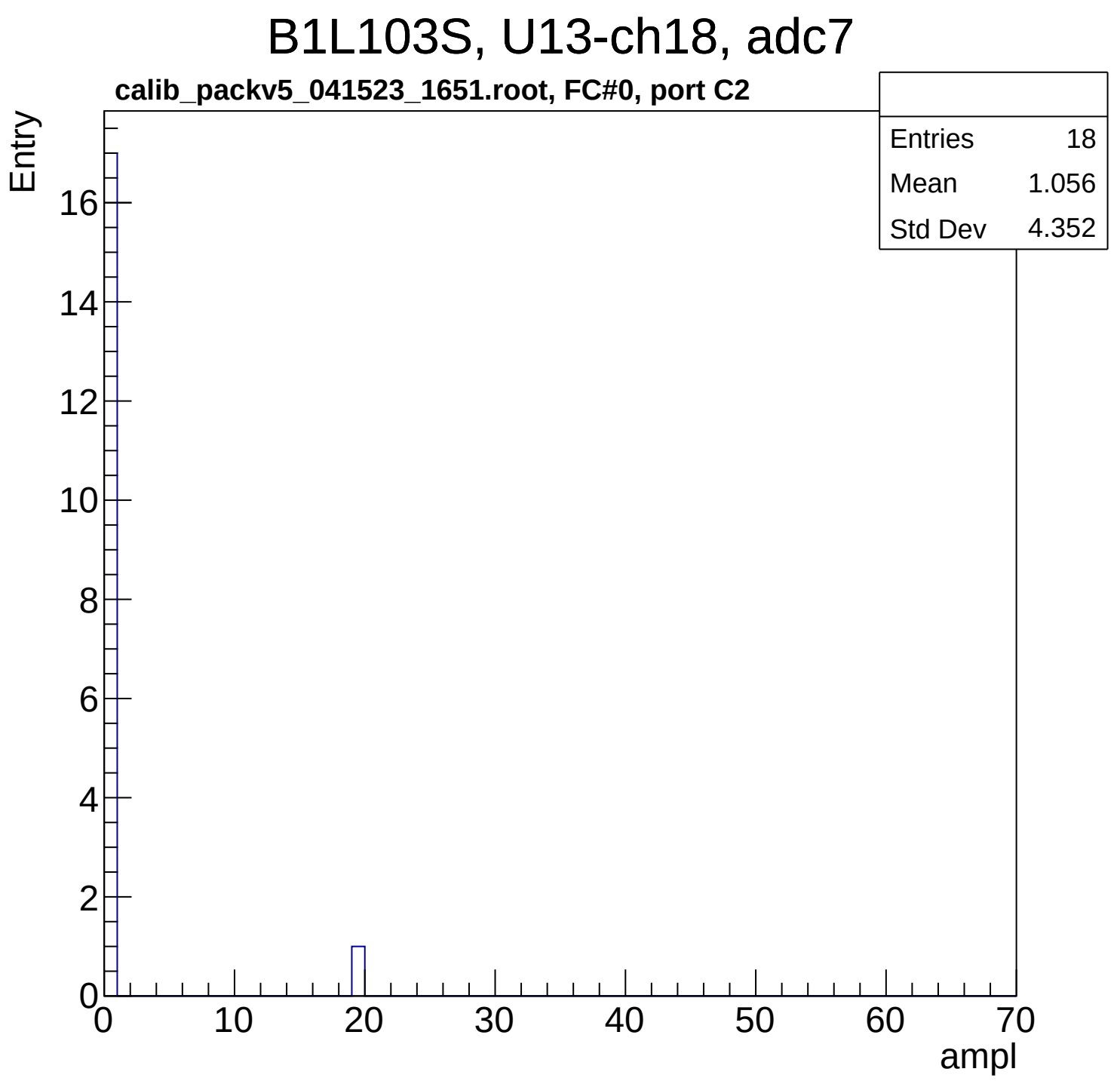
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U13-ch18, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.056
Std Dev 4.352
Entry
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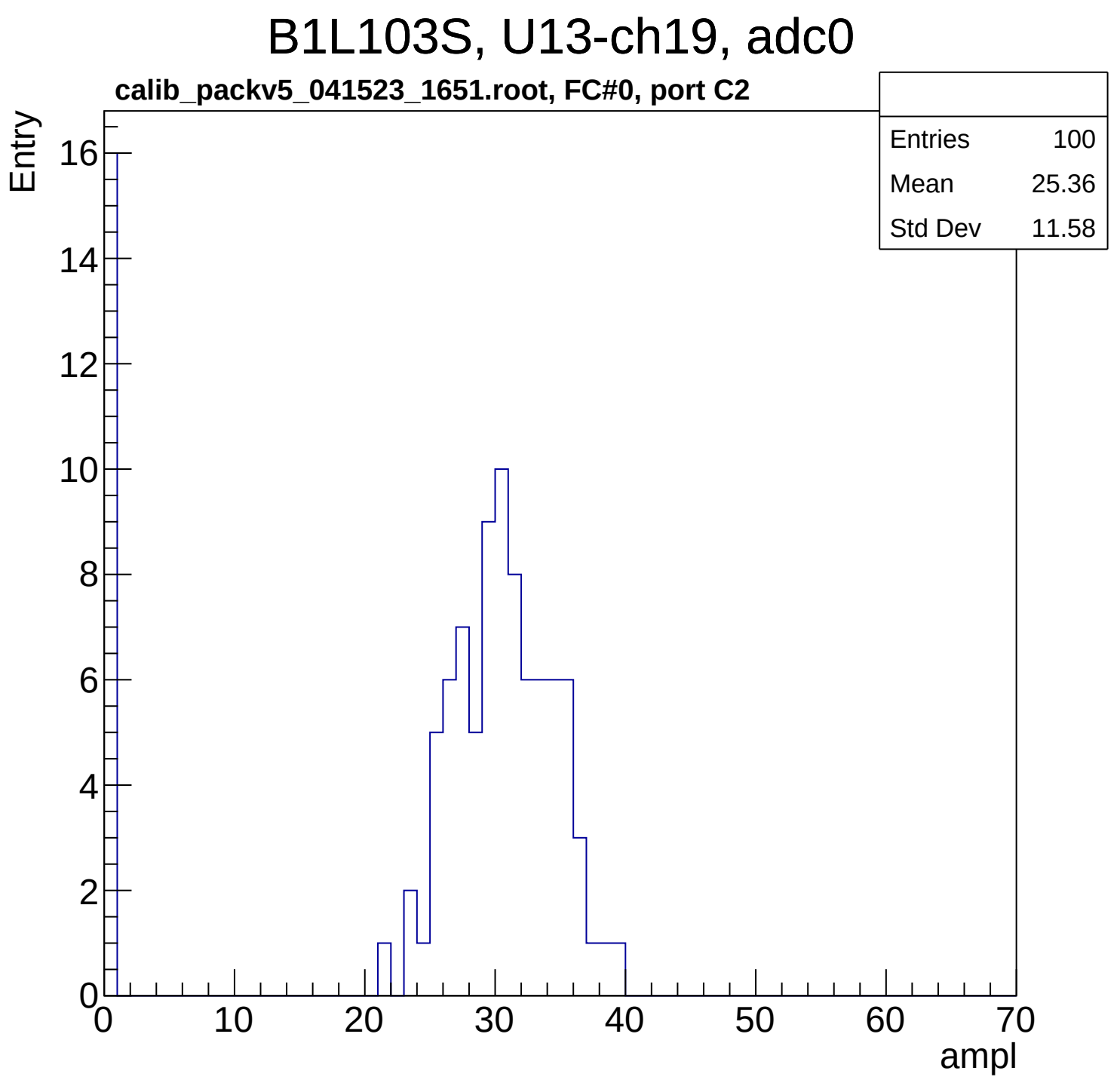
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch19, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 25.36
Std Dev 11.58
Entry
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4
6
8
10
12
14
16
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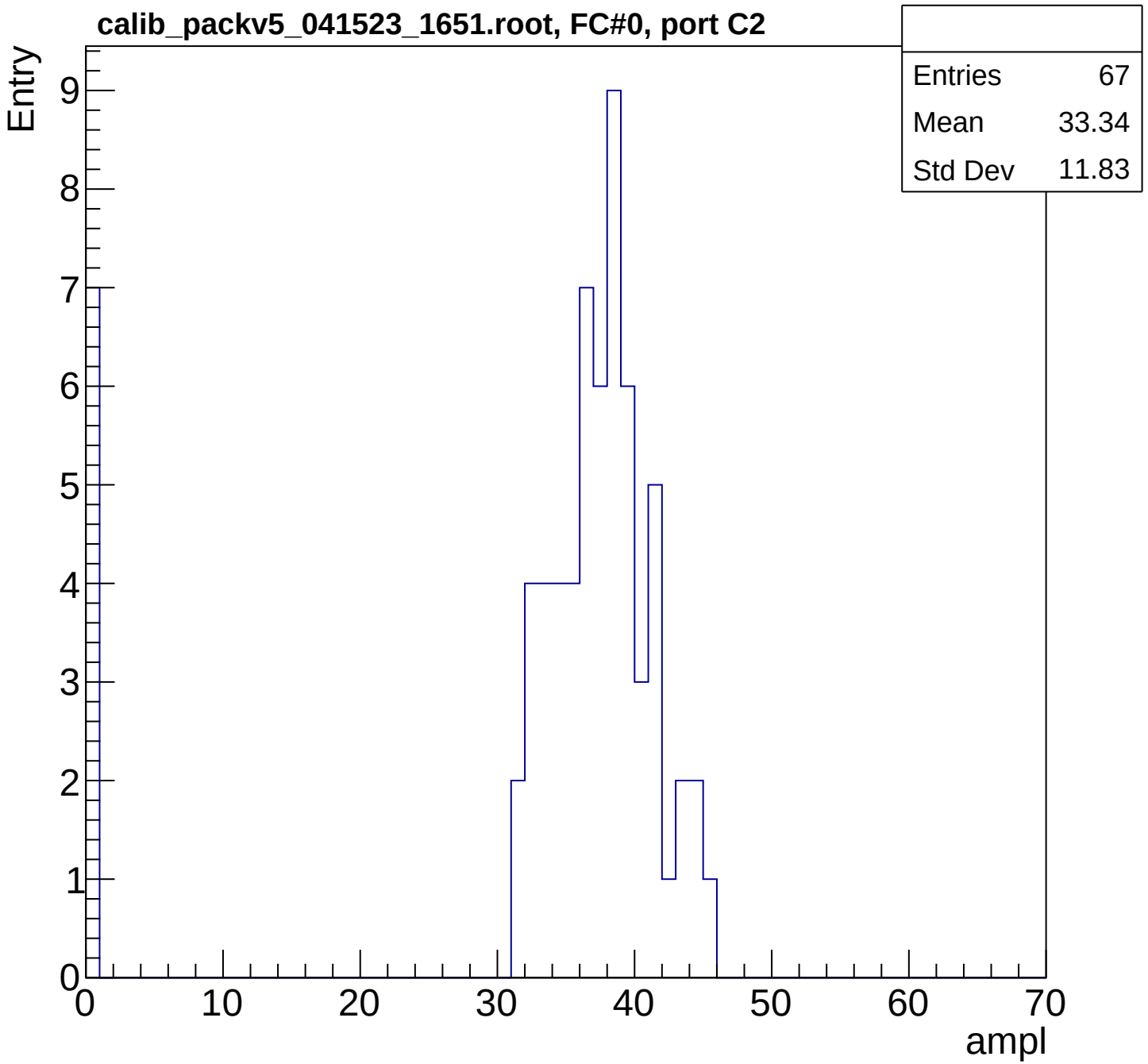
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch19, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 33.34
Std Dev 11.83
Entry
ampl
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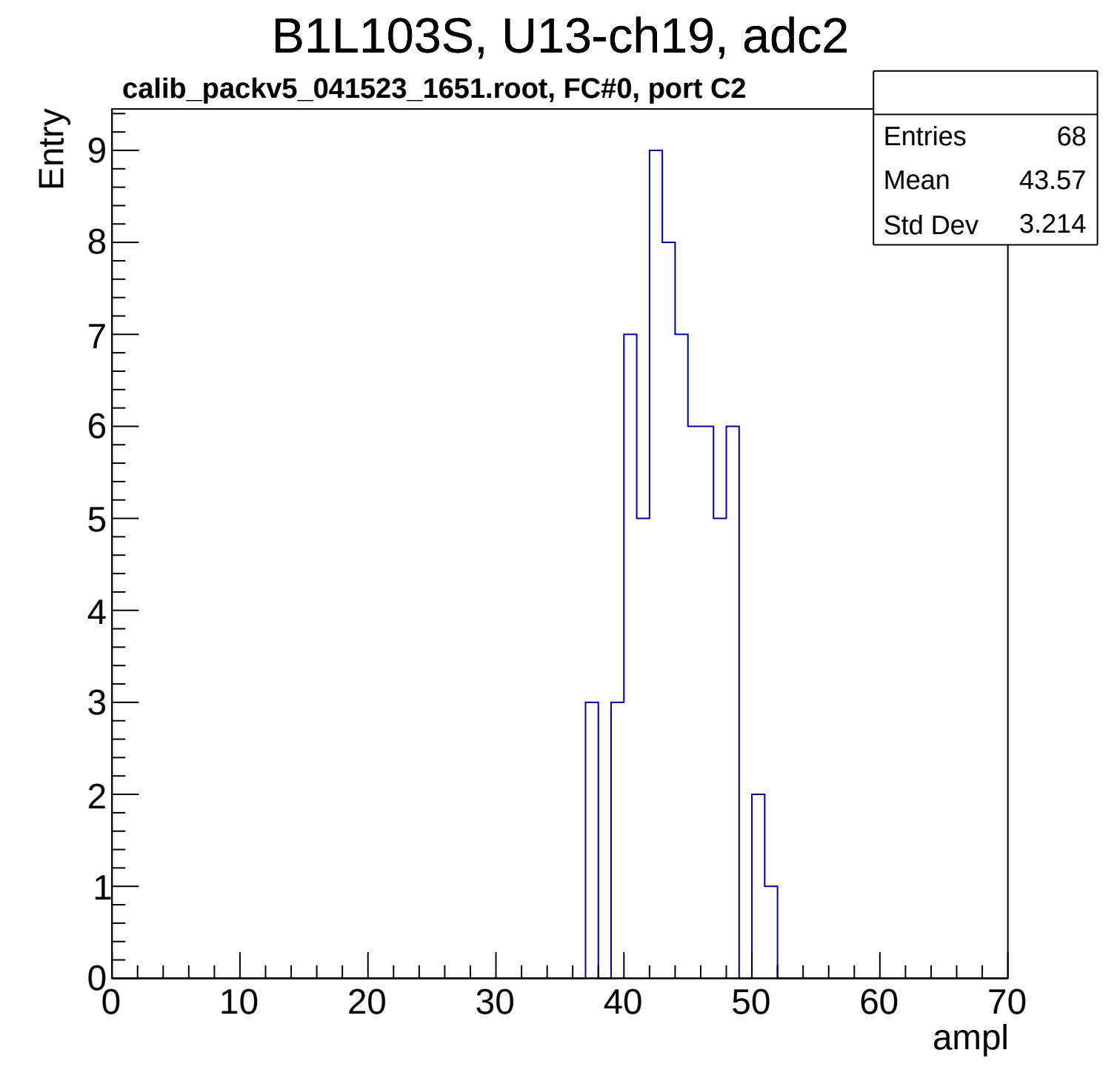
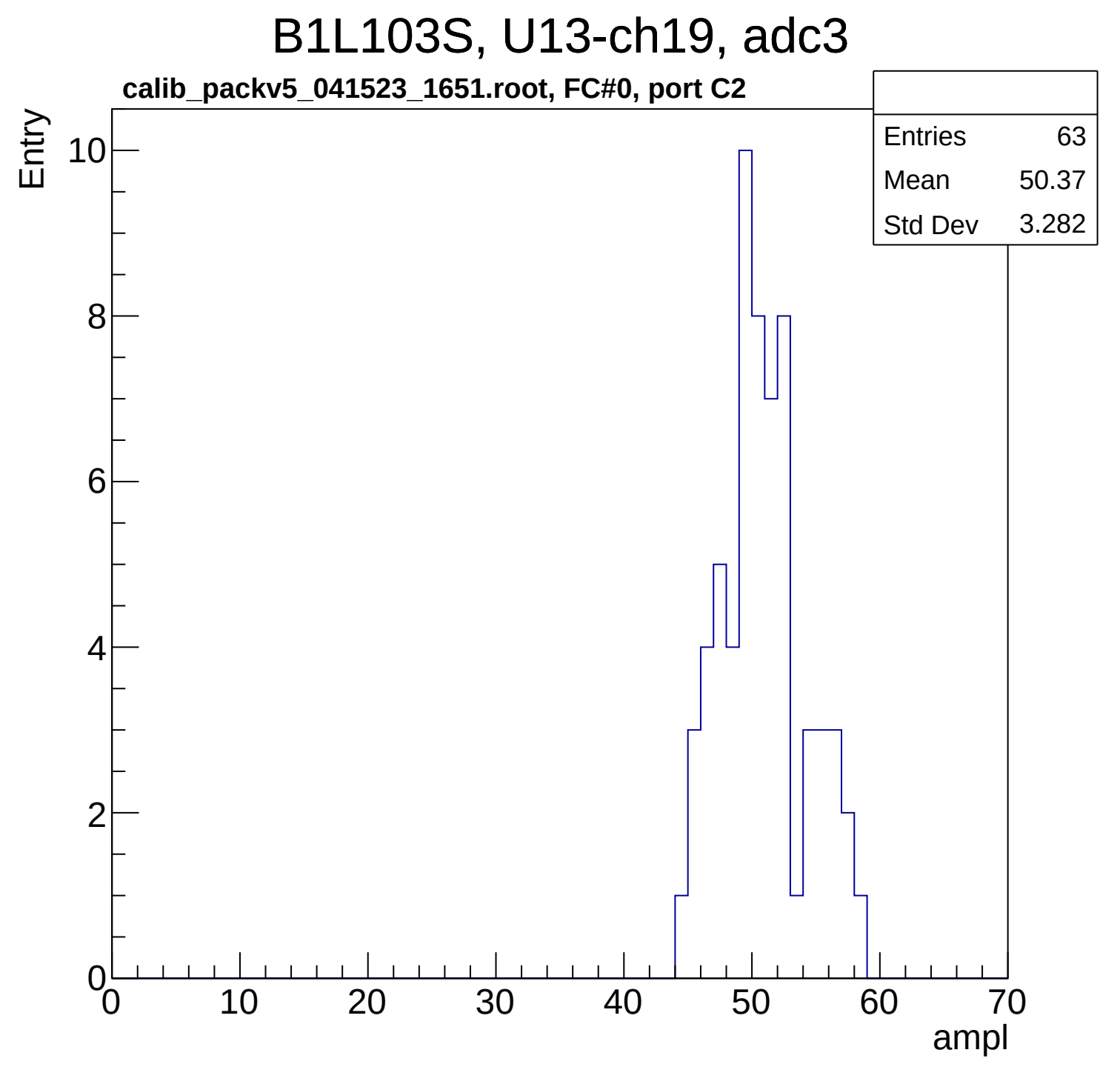
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch19, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 43.57
Std Dev 3.214
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch19, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 50.37
Std Dev 3.282
Entry
0
2
4
6
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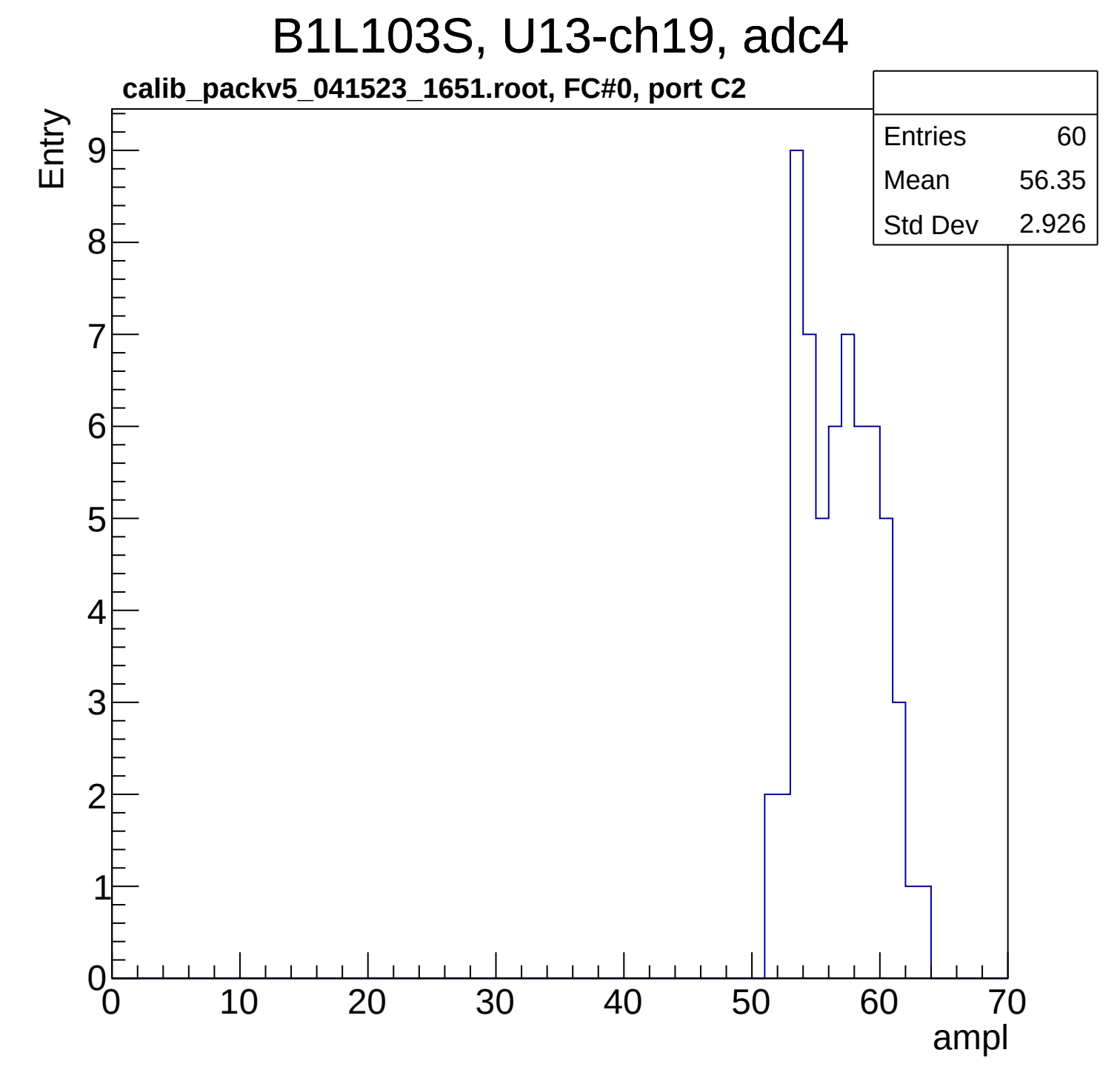
ampl


B1L103S, U13-ch19, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 56.35
Std Dev 2.926
Entry
ampl
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4
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8
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0
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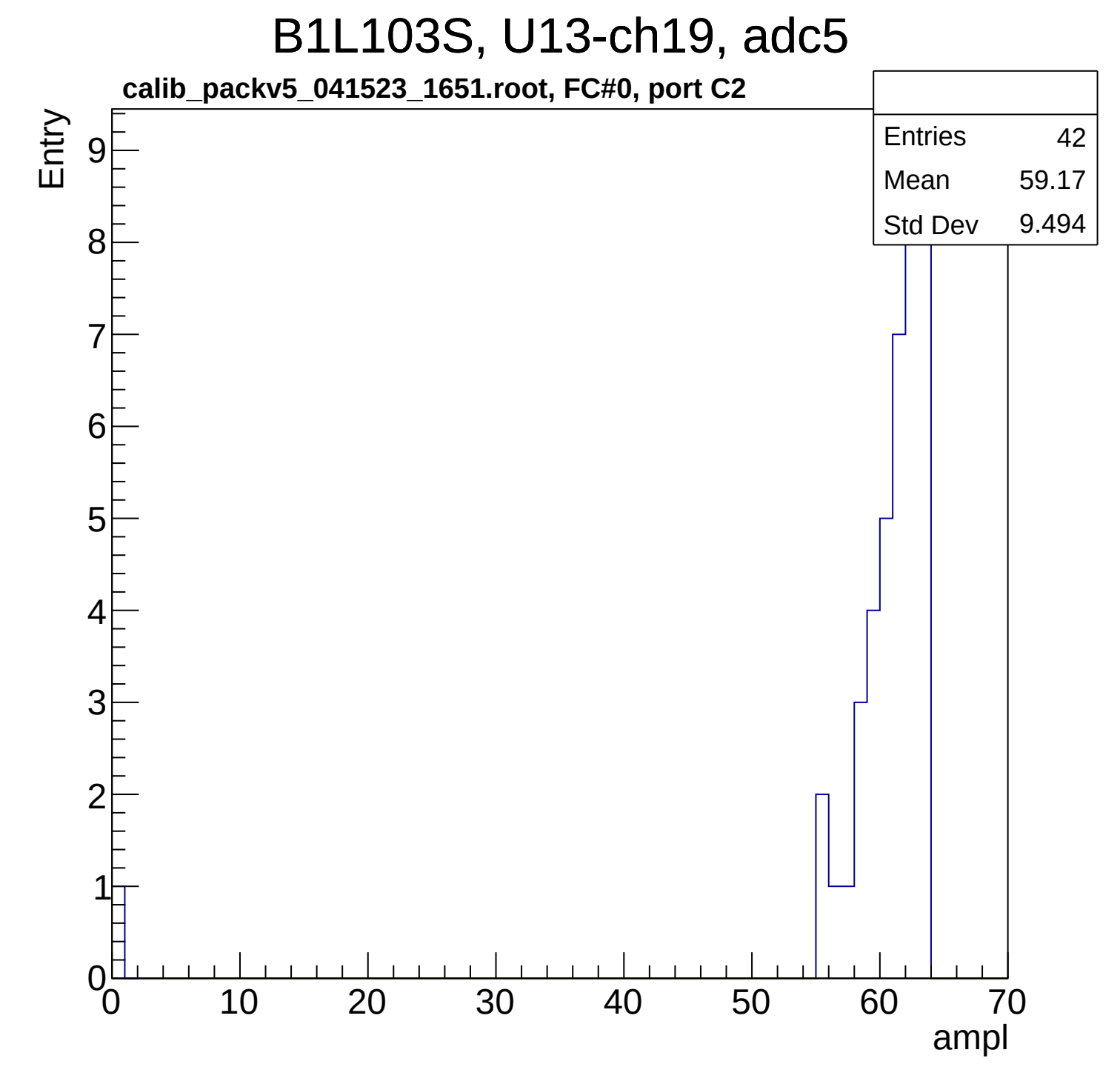
B1L103S, U13-ch19, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 59.17
Std Dev 9.494
Entry
ampl
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2
3
4
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6
7
8
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0
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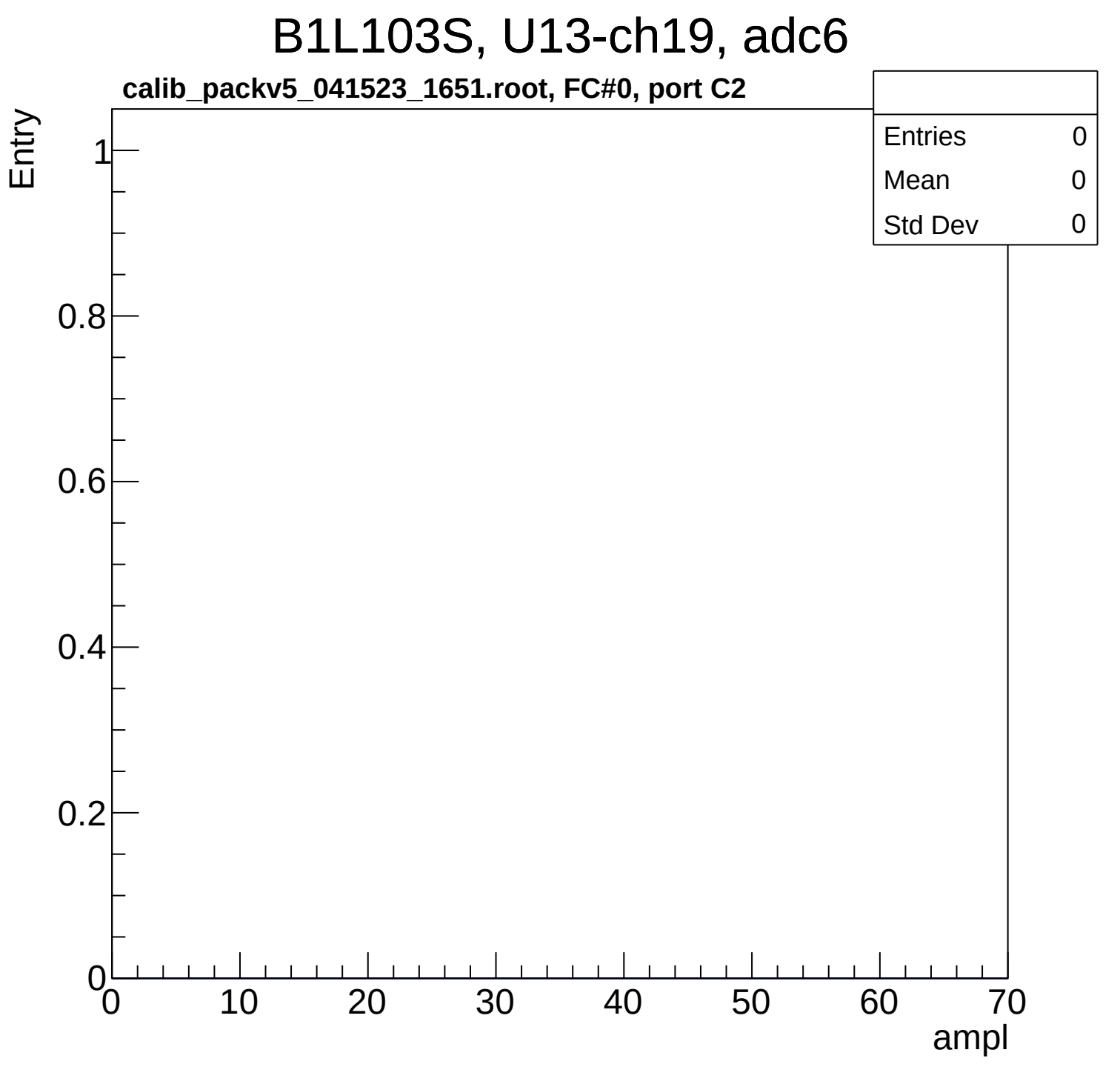
B1L103S, U13-ch19, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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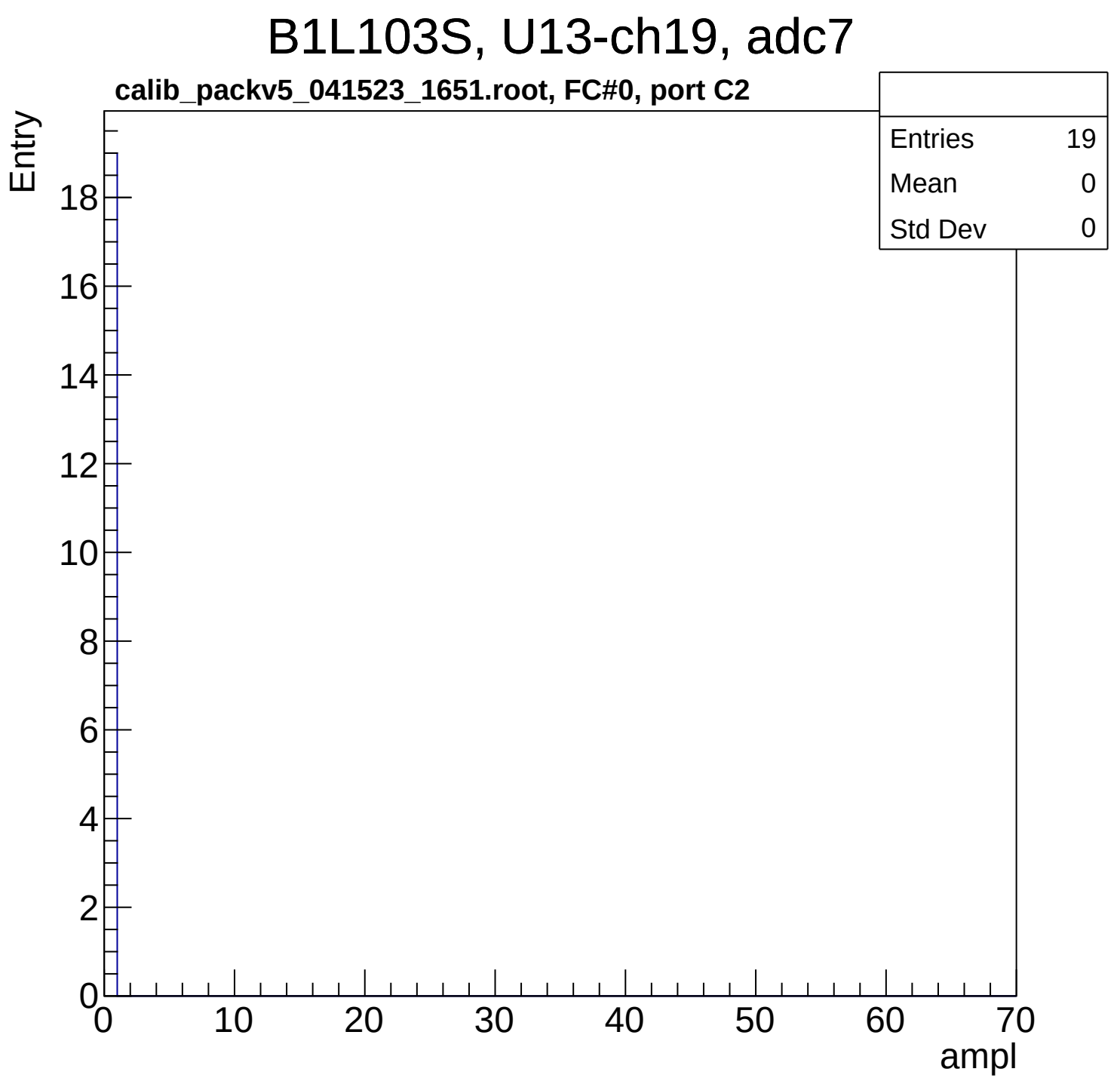
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch19, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
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50
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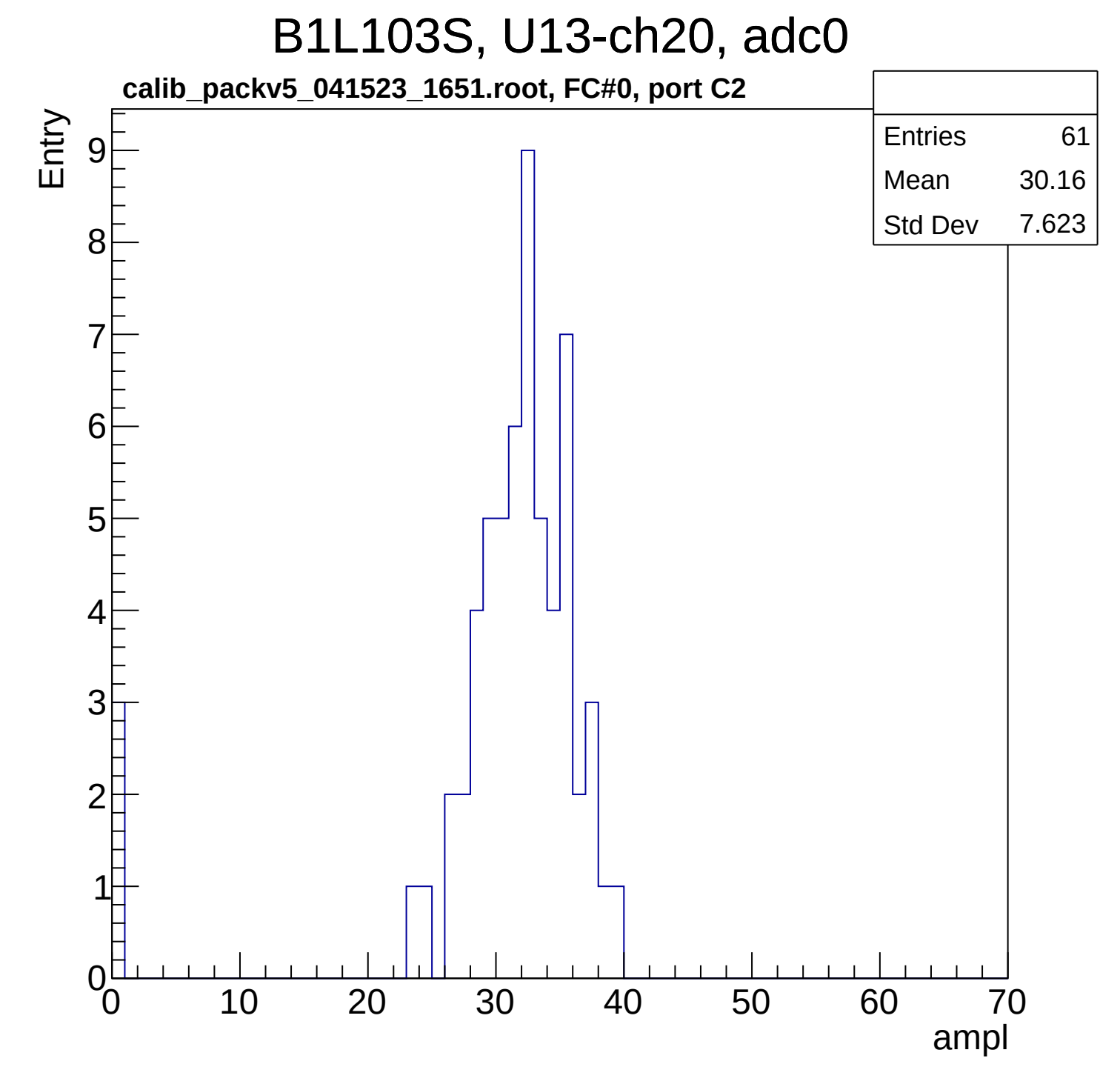
70
ampl


B1L103S, U13-ch20, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 30.16
Std Dev 7.623
Entry
ampl
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2
3
4
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6
7
8
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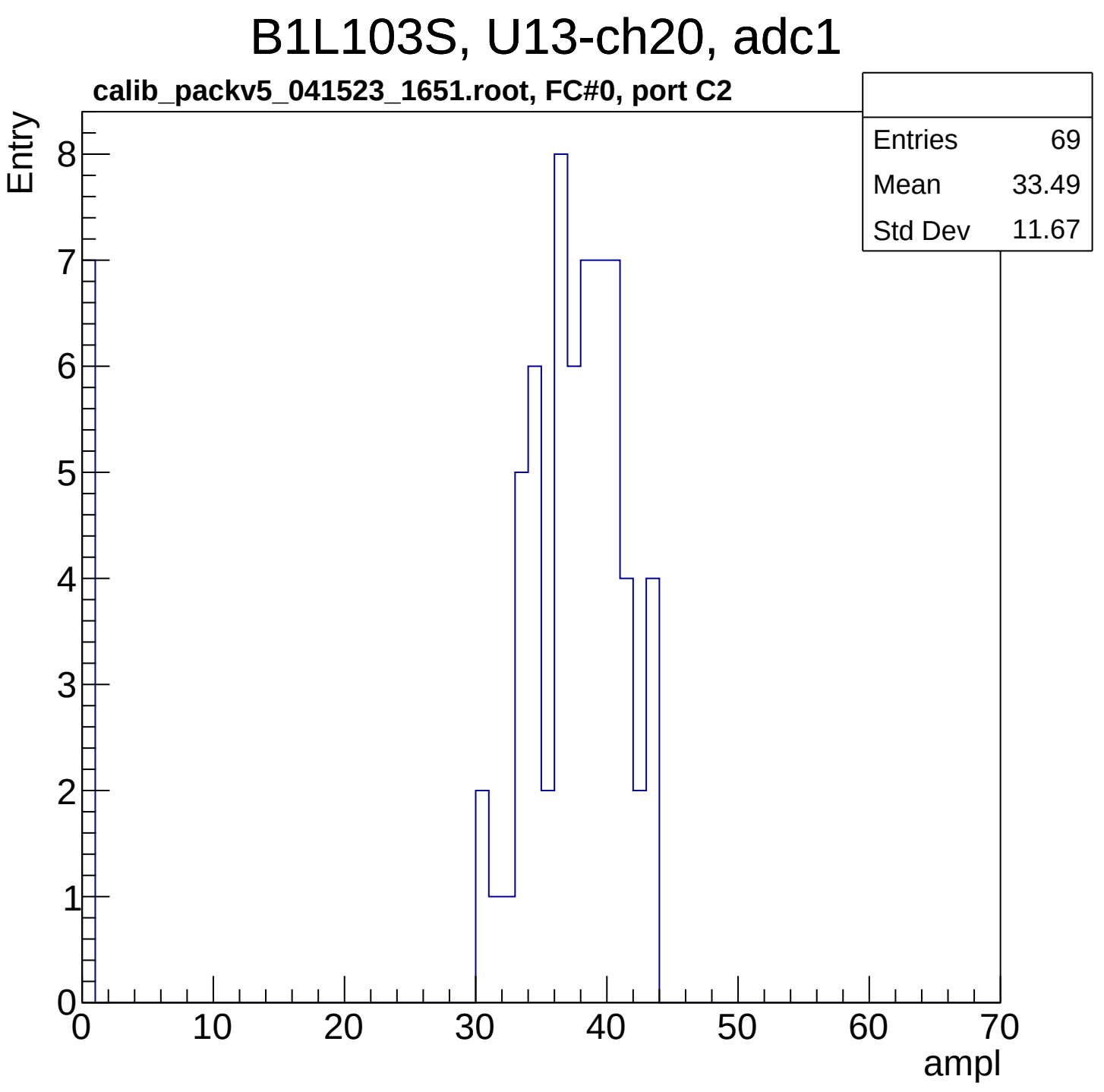
B1L103S, U13-ch20, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 33.49
Std Dev 11.67
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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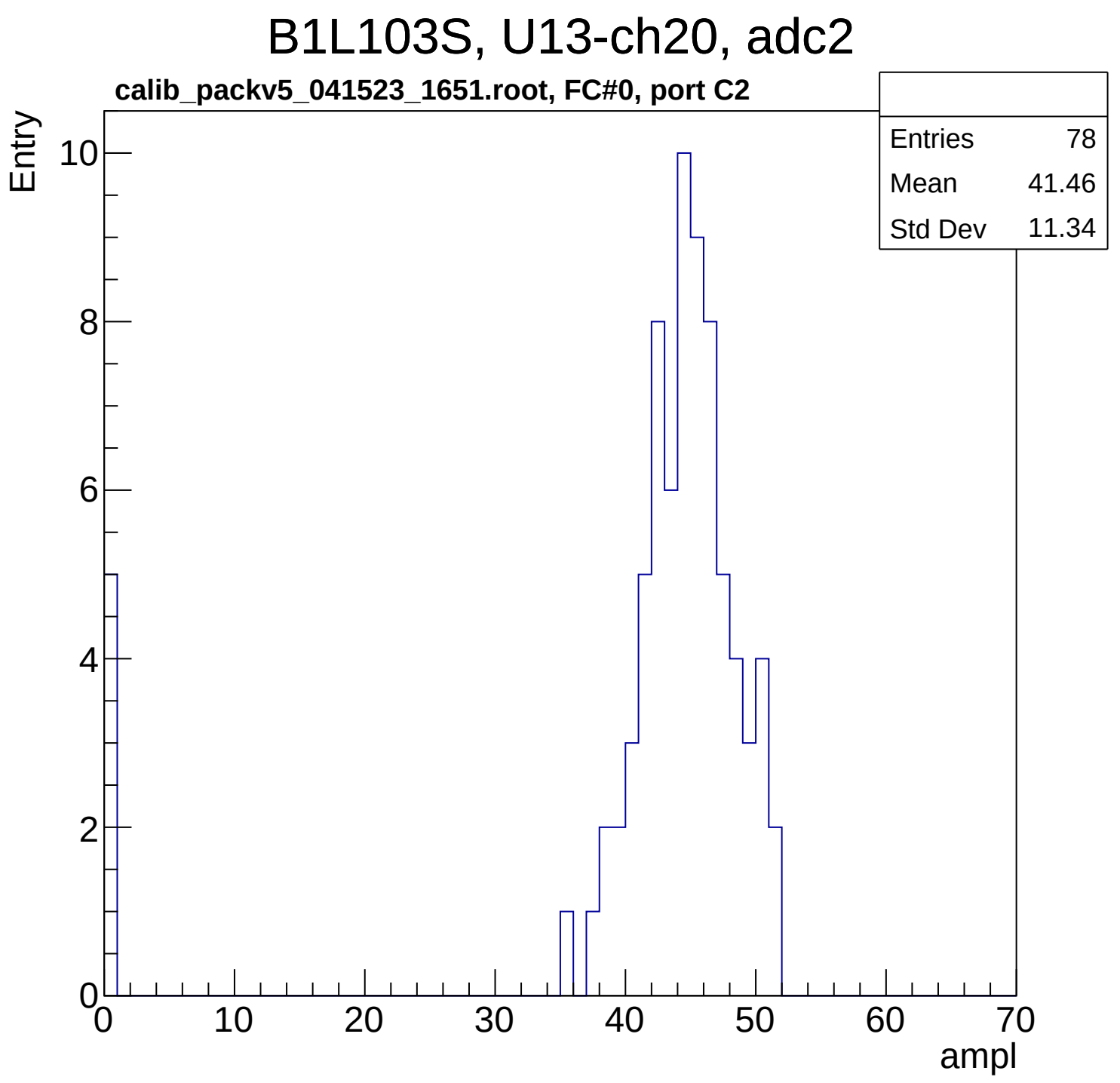
B1L103S, U13-ch20, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 41.46
Std Dev 11.34
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
50
60
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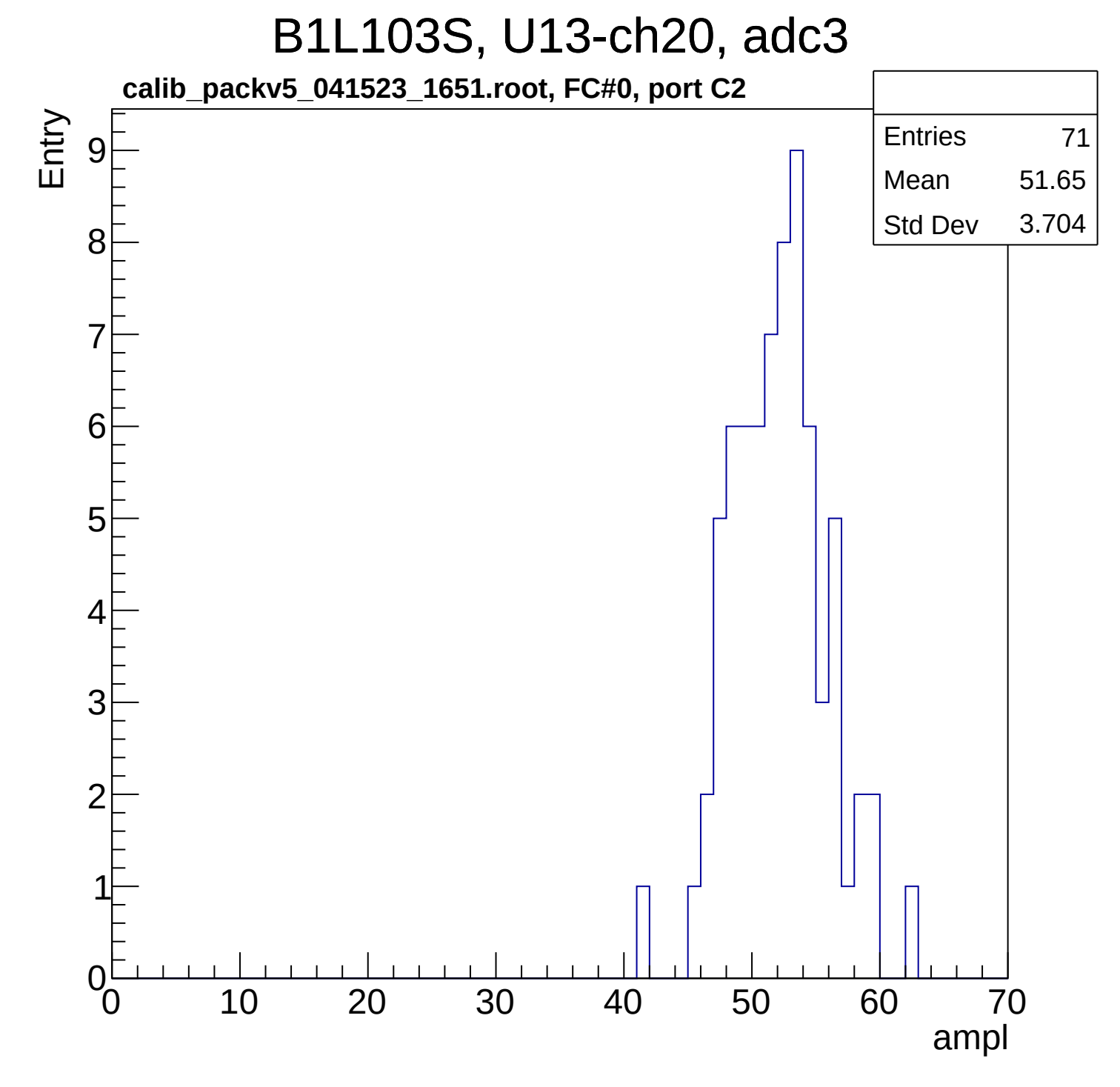
B1L103S, U13-ch20, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 51.65
Std Dev 3.704
Entry
ampl
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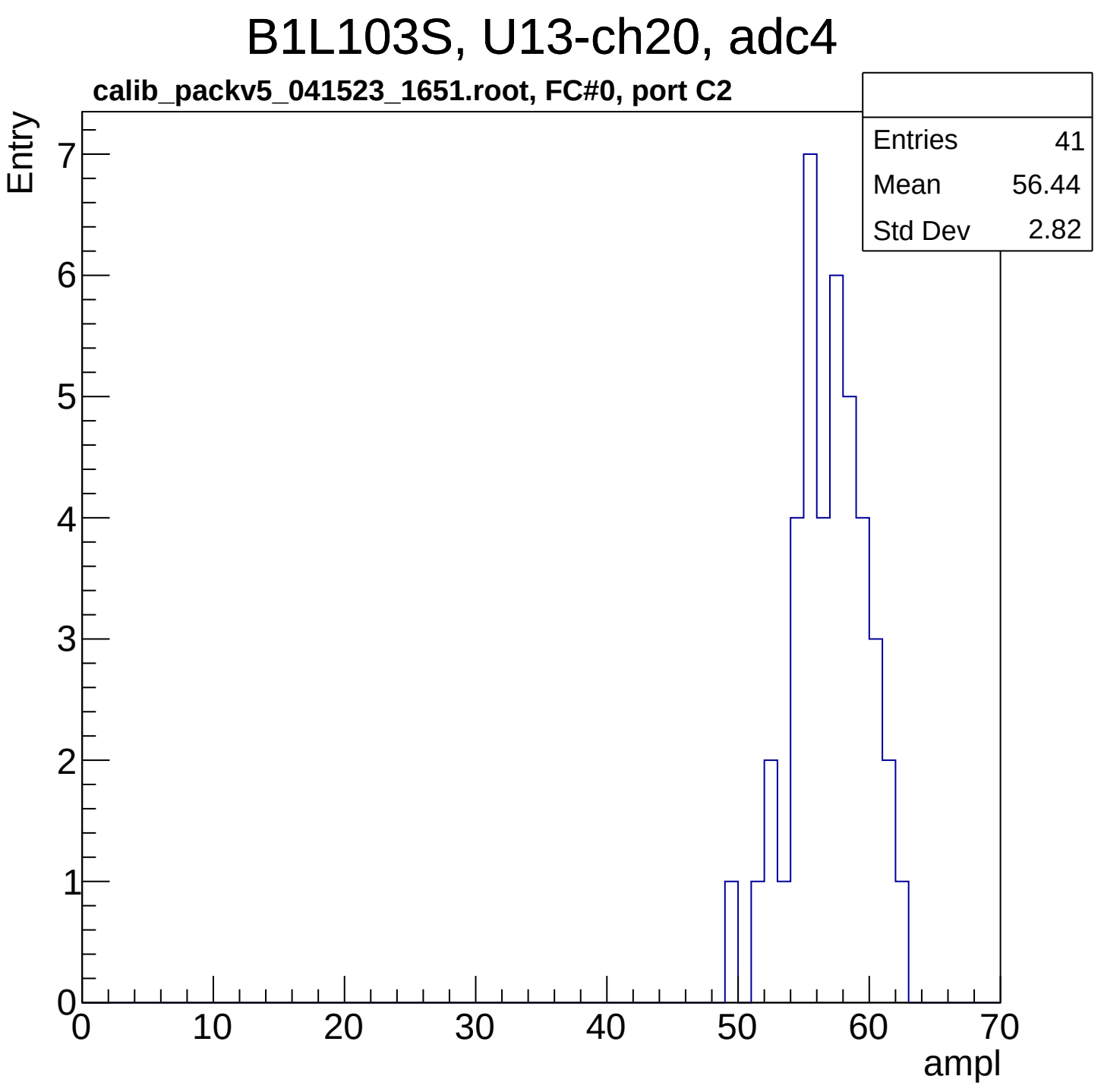
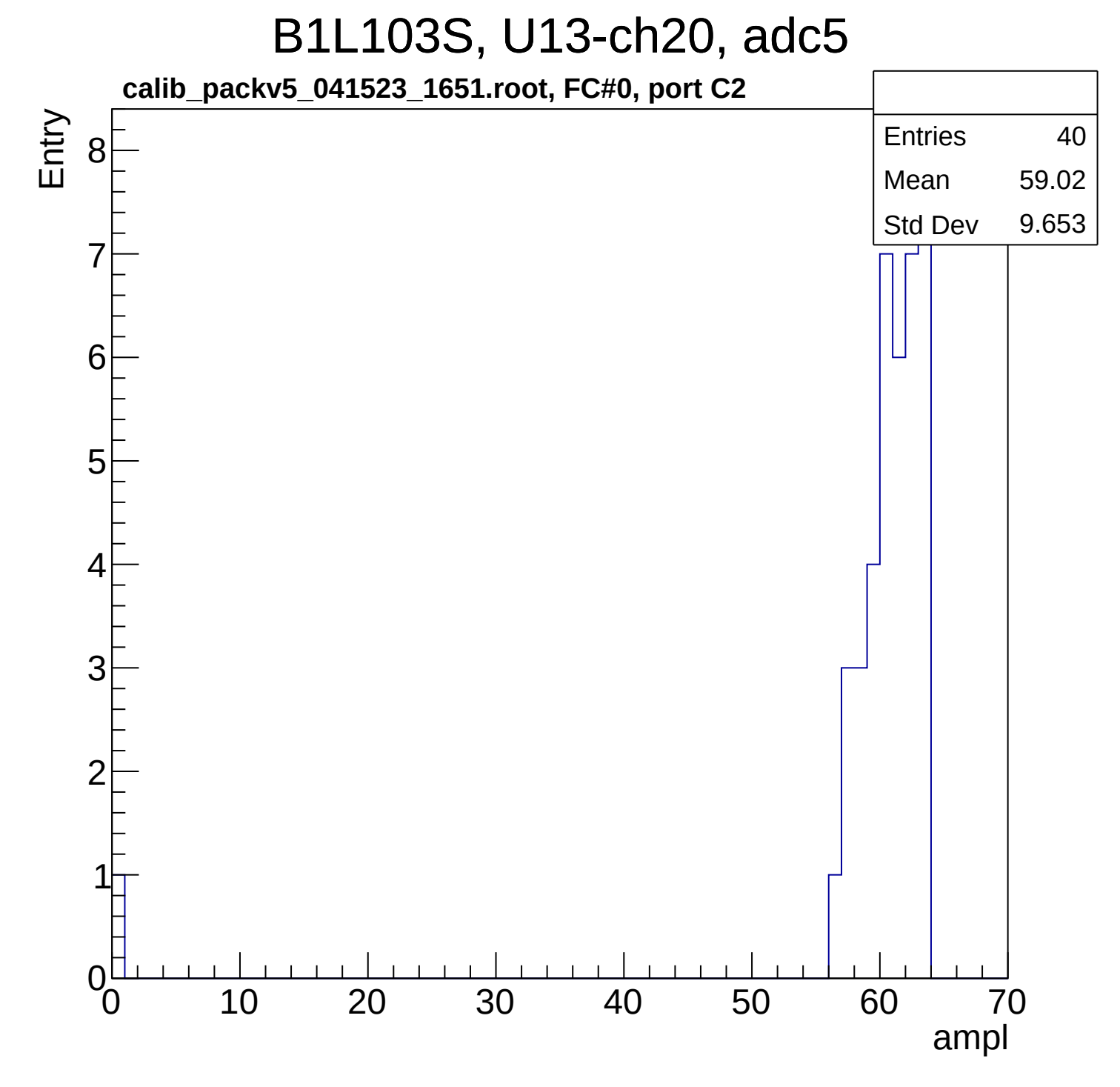
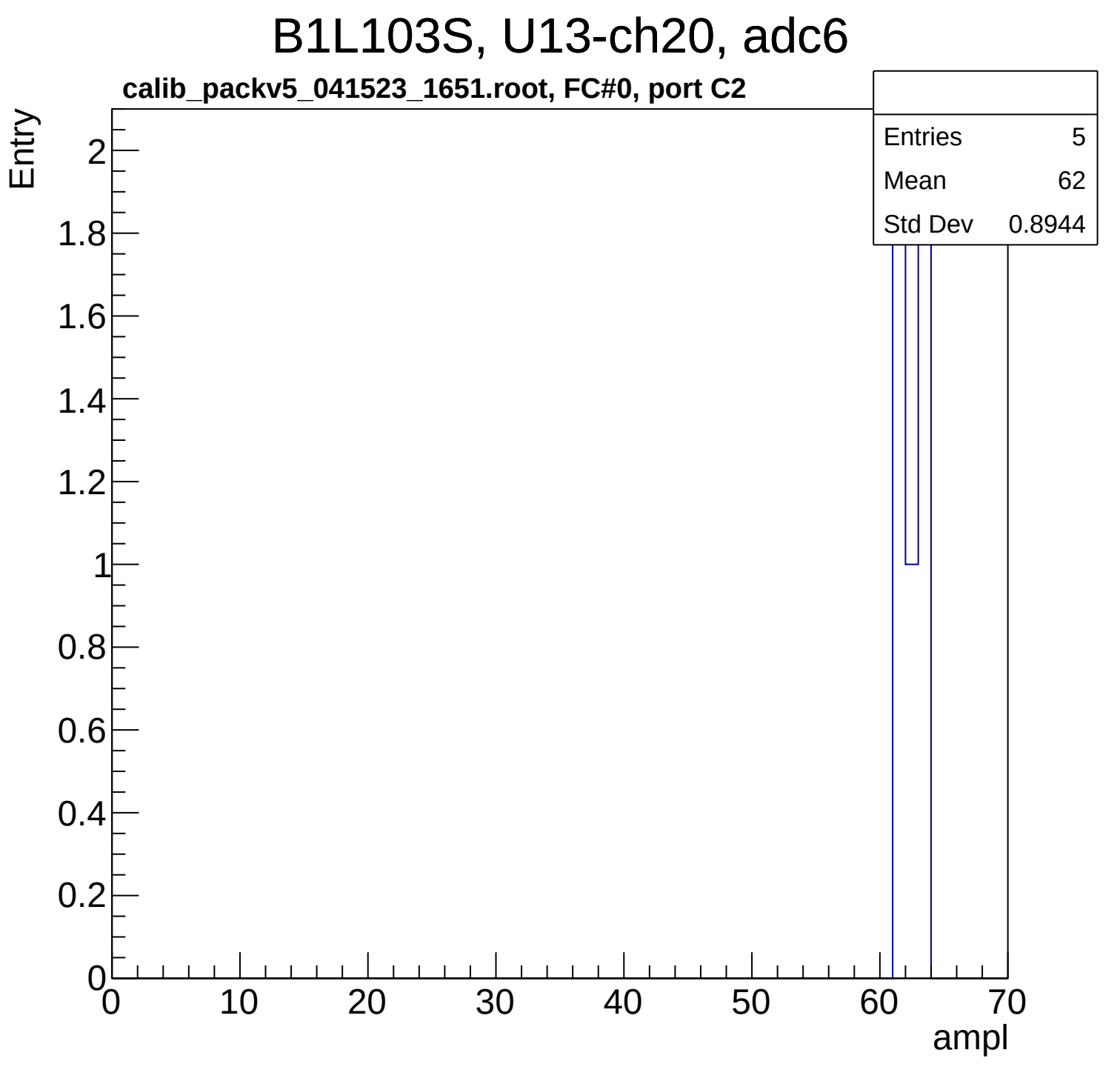
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch20, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 56.44
Std Dev 2.82
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch20, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 59.02
Std Dev 9.653
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch20, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62
Std Dev 0.8944
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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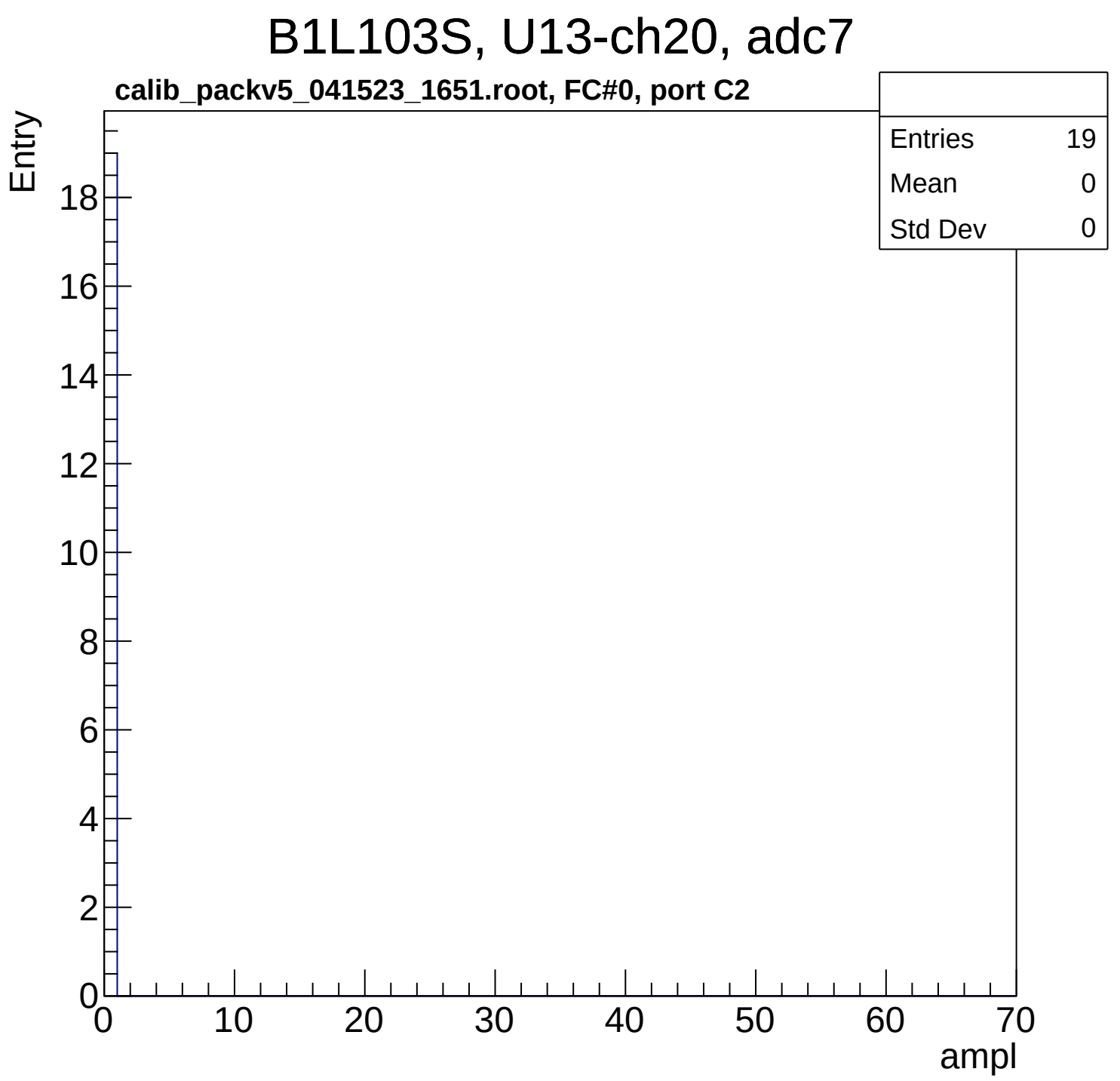
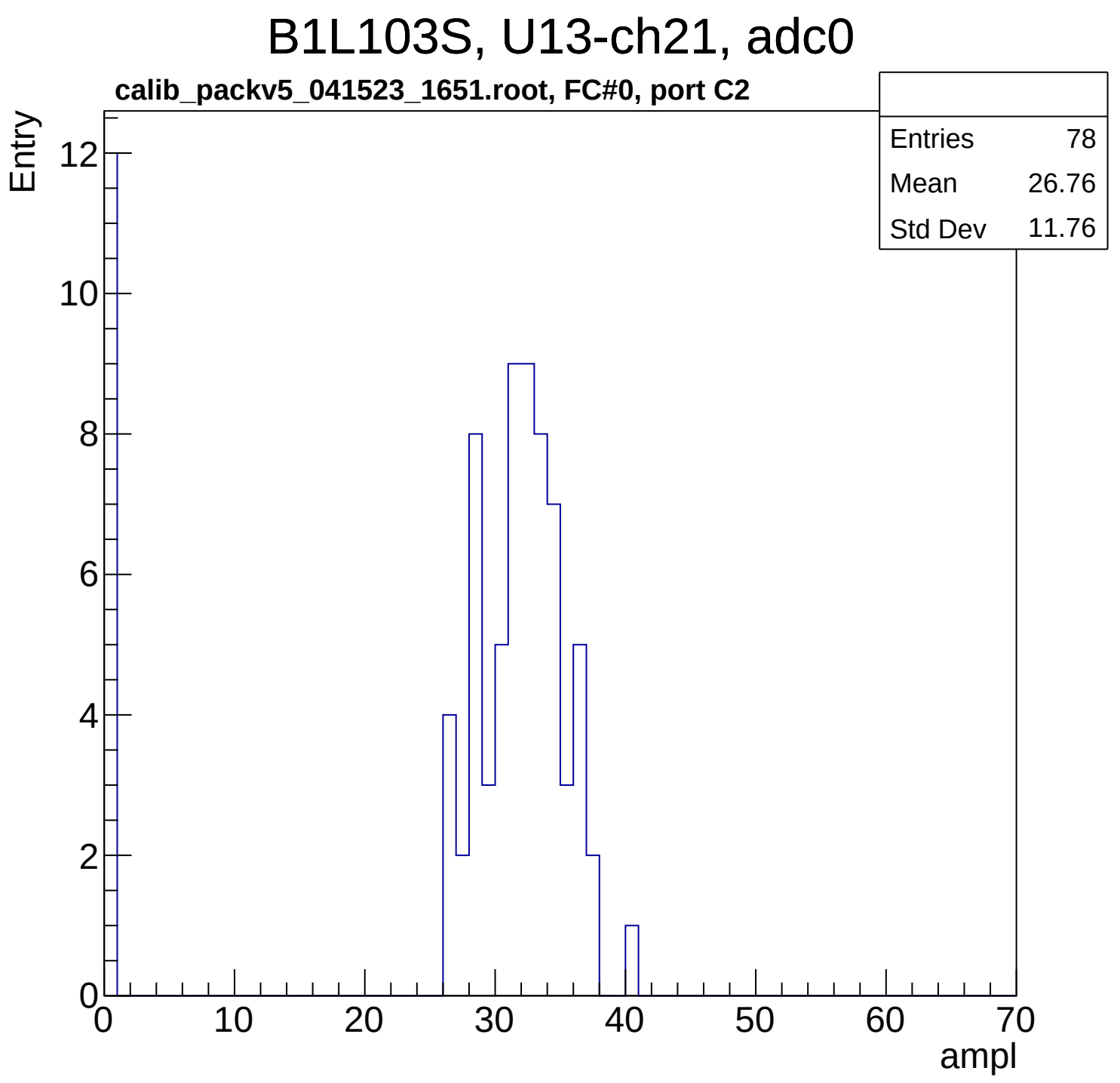

B1L103S, U13-ch20, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch21, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 26.76
Std Dev 11.76
Entry
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2
4
6
8
10
12
0
10
20
30
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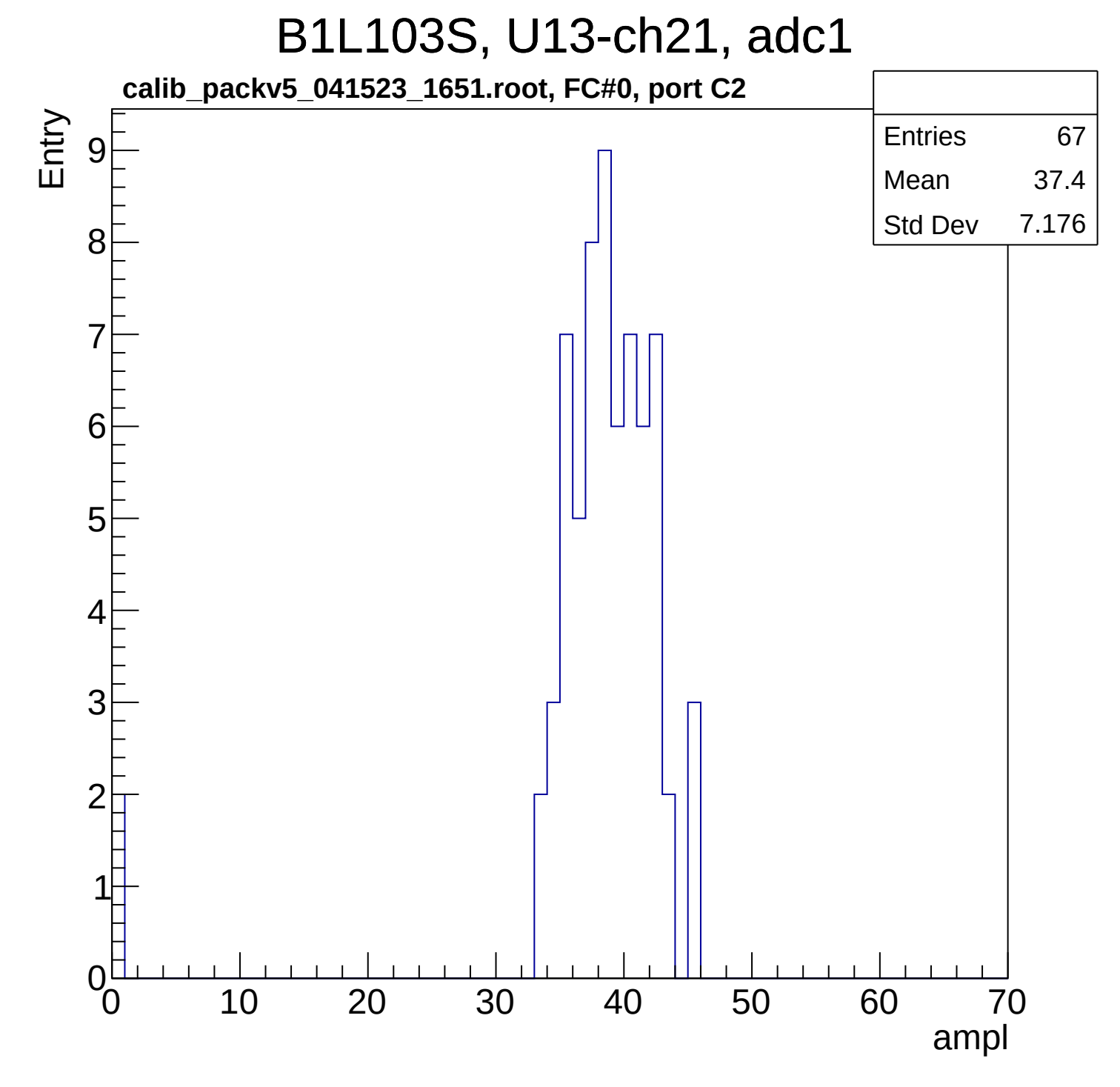
50
60
70
ampl


B1L103S, U13-ch21, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 37.4
Std Dev 7.176
Entry
ampl
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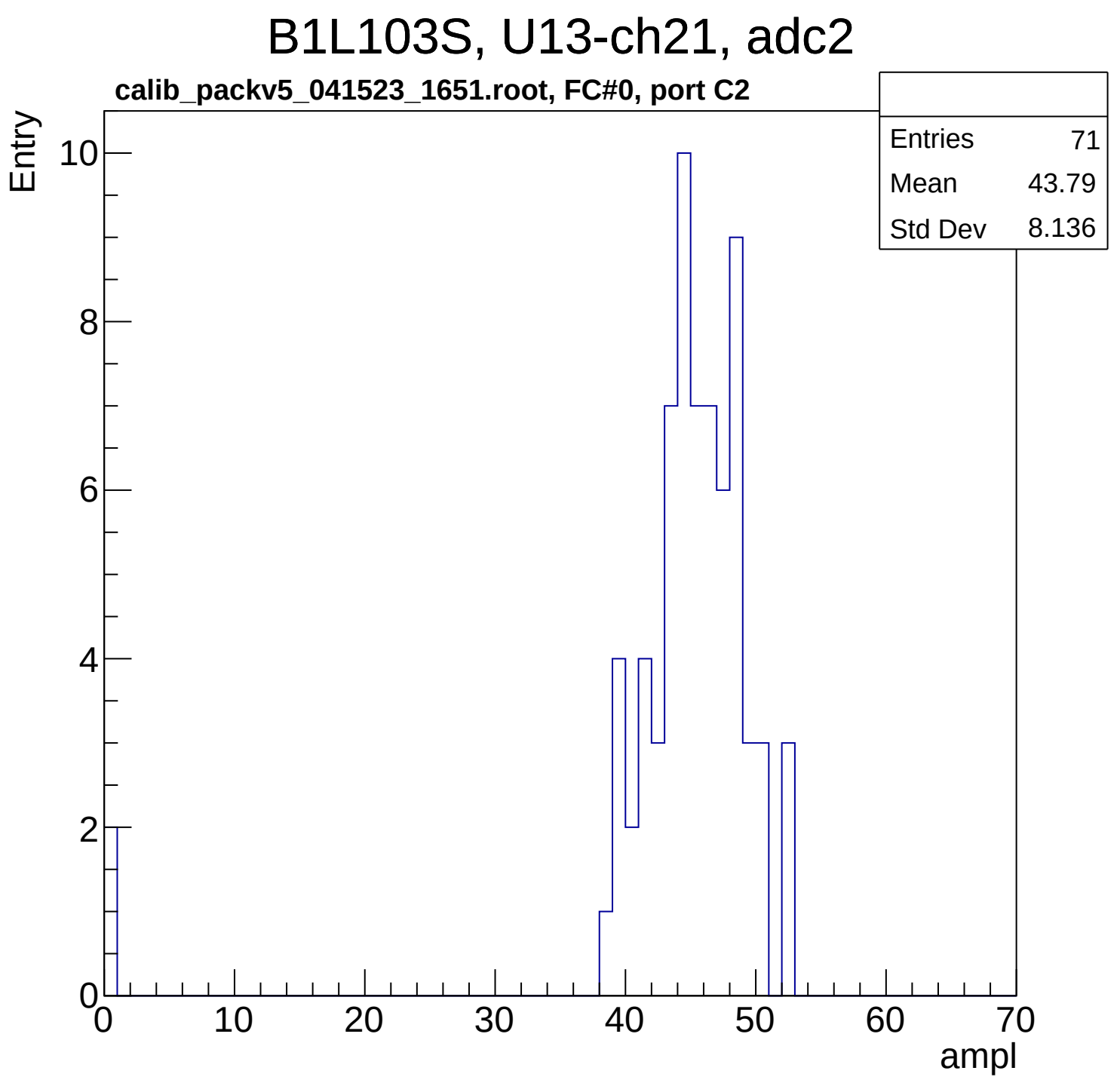
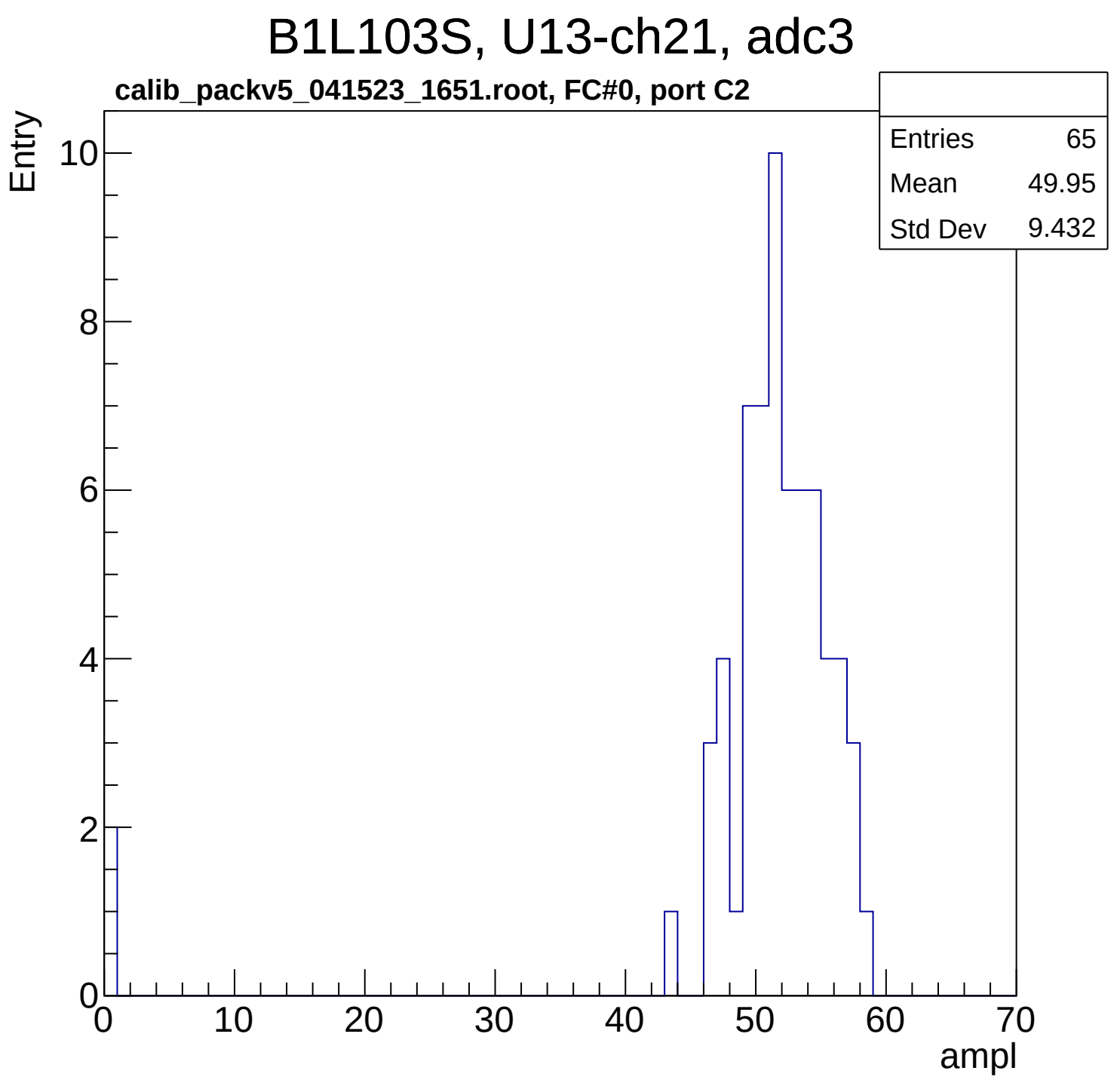
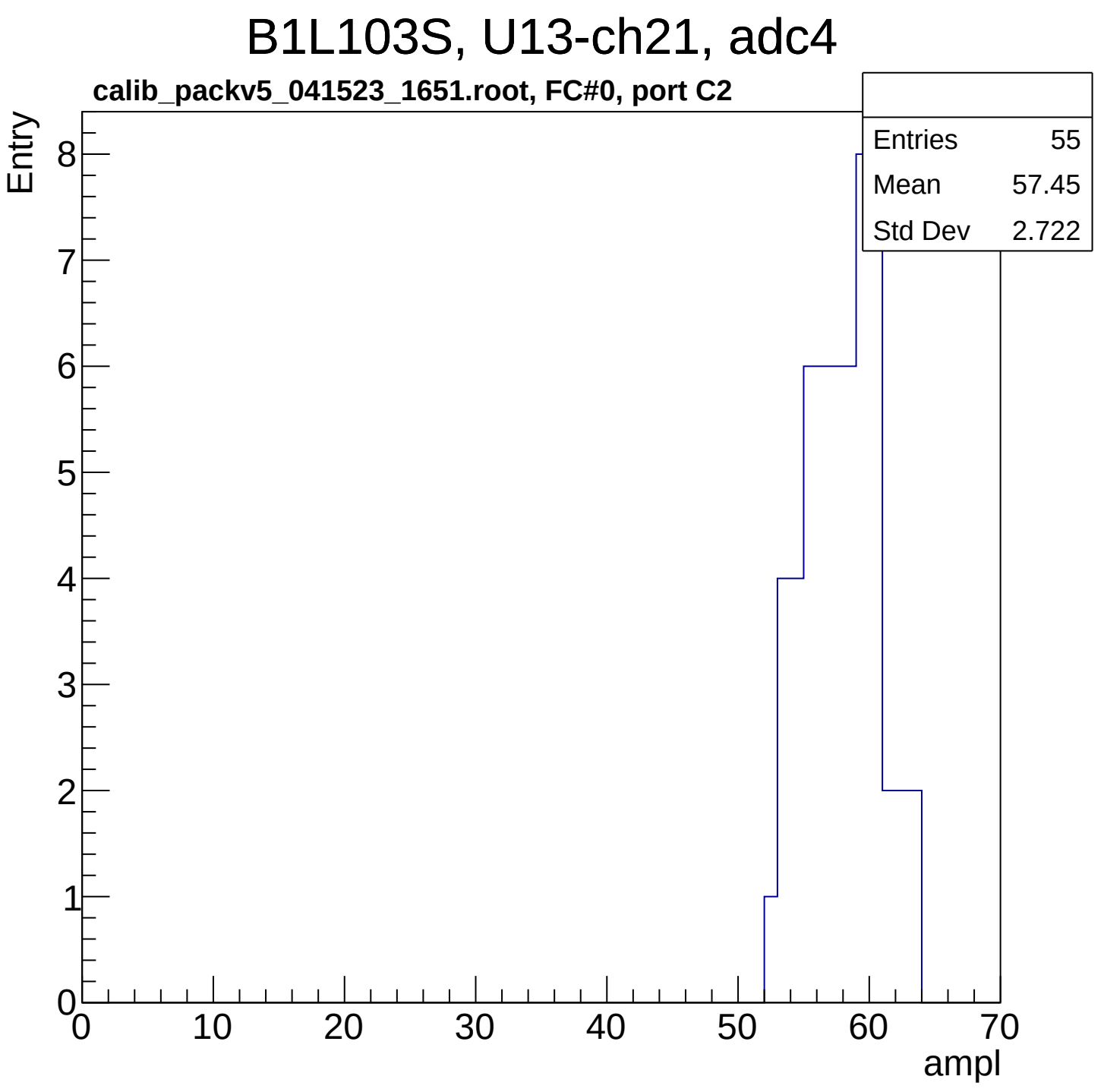
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch21, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 43.79
Std Dev 8.136
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch21, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 49.95
Std Dev 9.432
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch21, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.45
Std Dev 2.722
Entry
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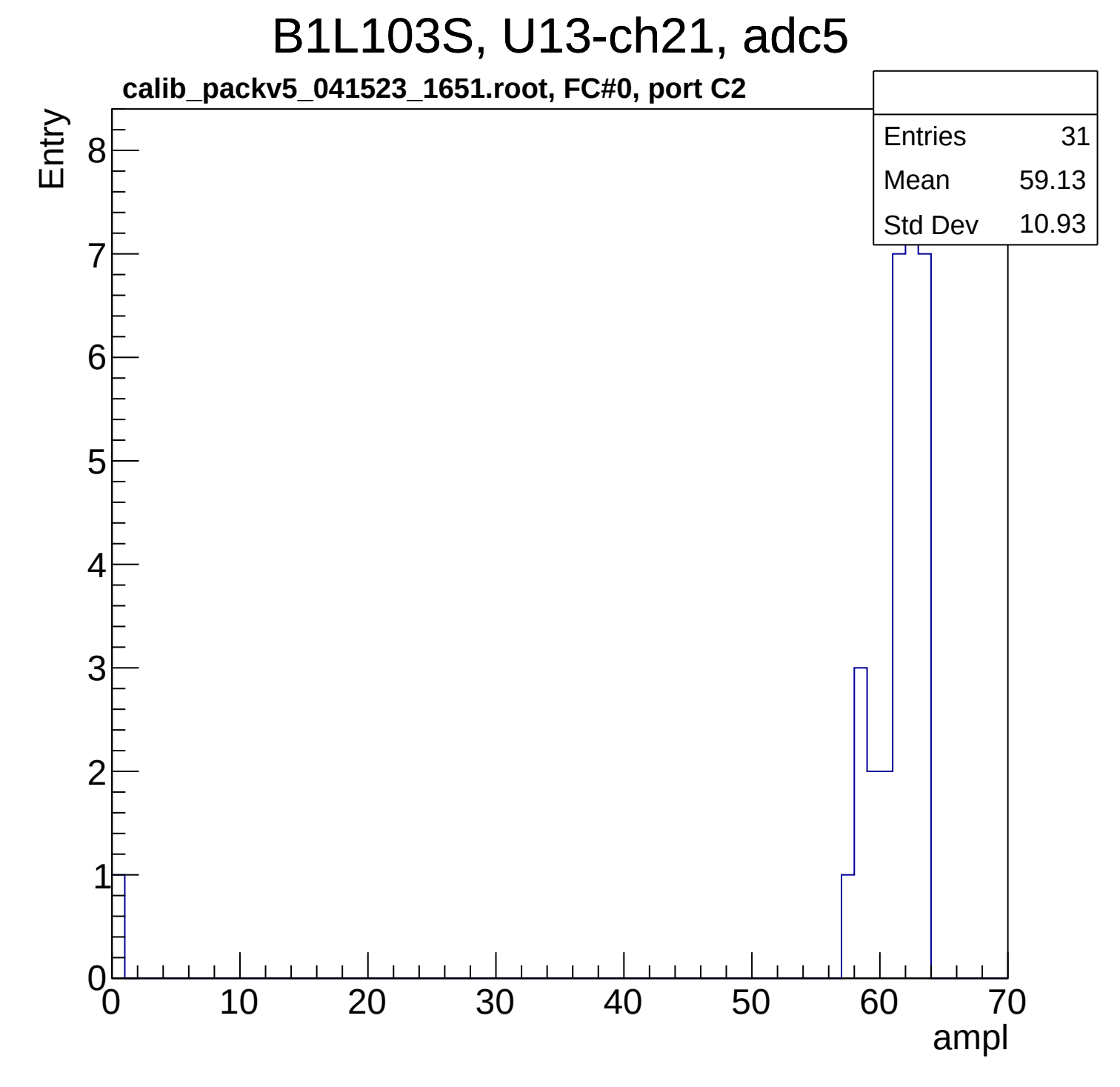
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch21, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 59.13
Std Dev 10.93
Entry
ampl
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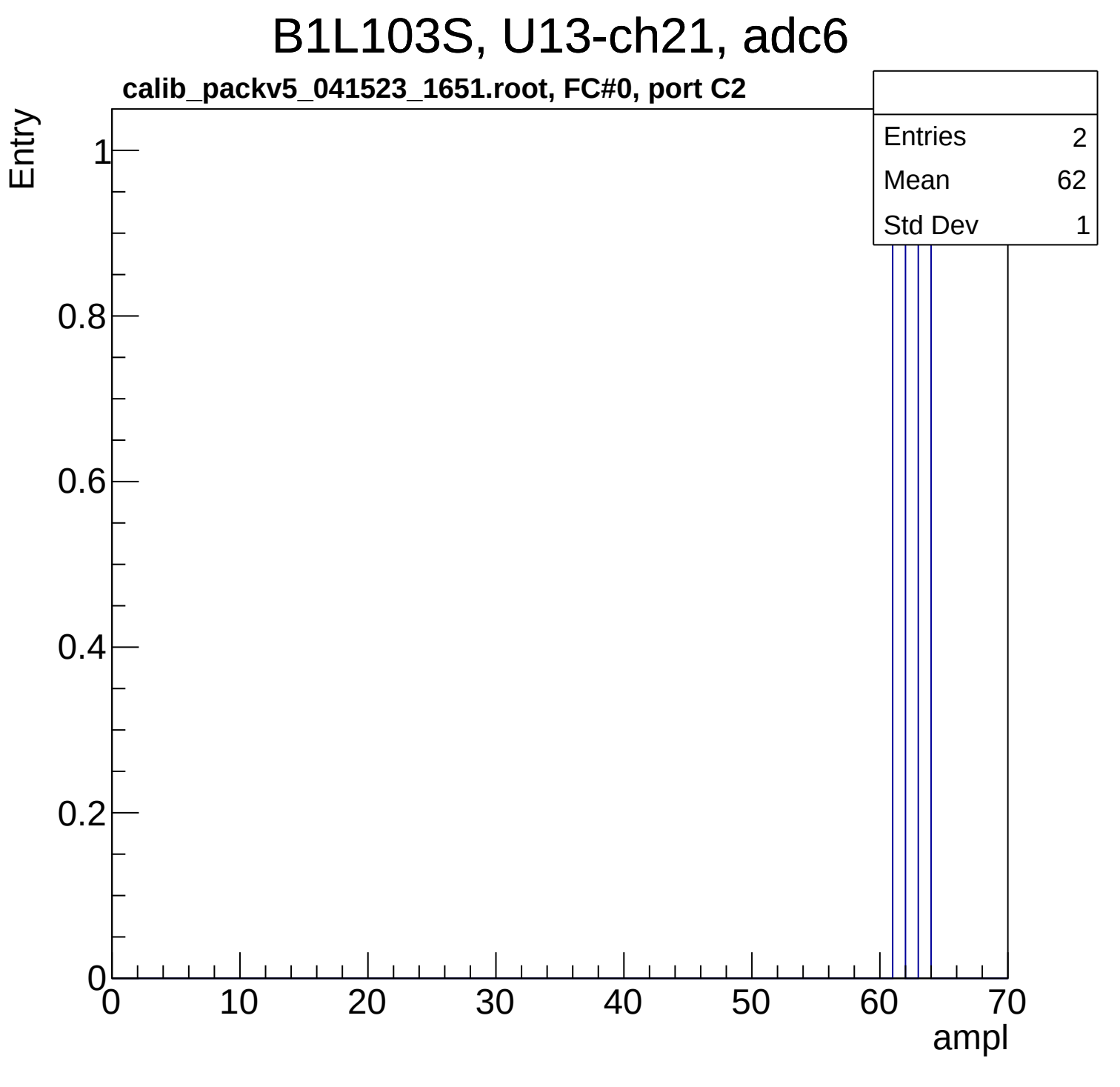
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch21, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62
Std Dev 1
Entry
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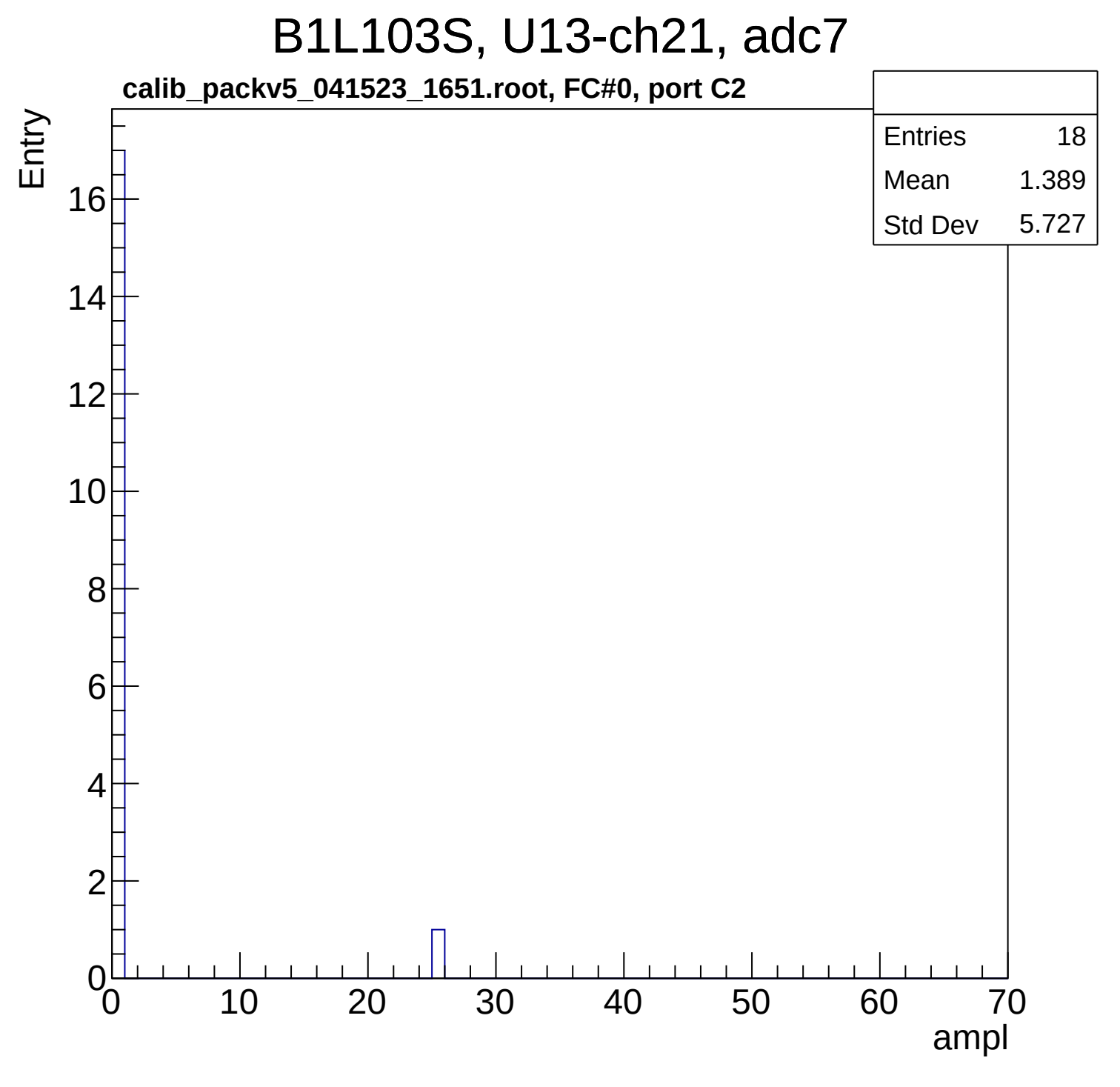
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch21, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.389
Std Dev 5.727
Entry
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4
6
8
10
12
14
16
0
10
20
30
40
50
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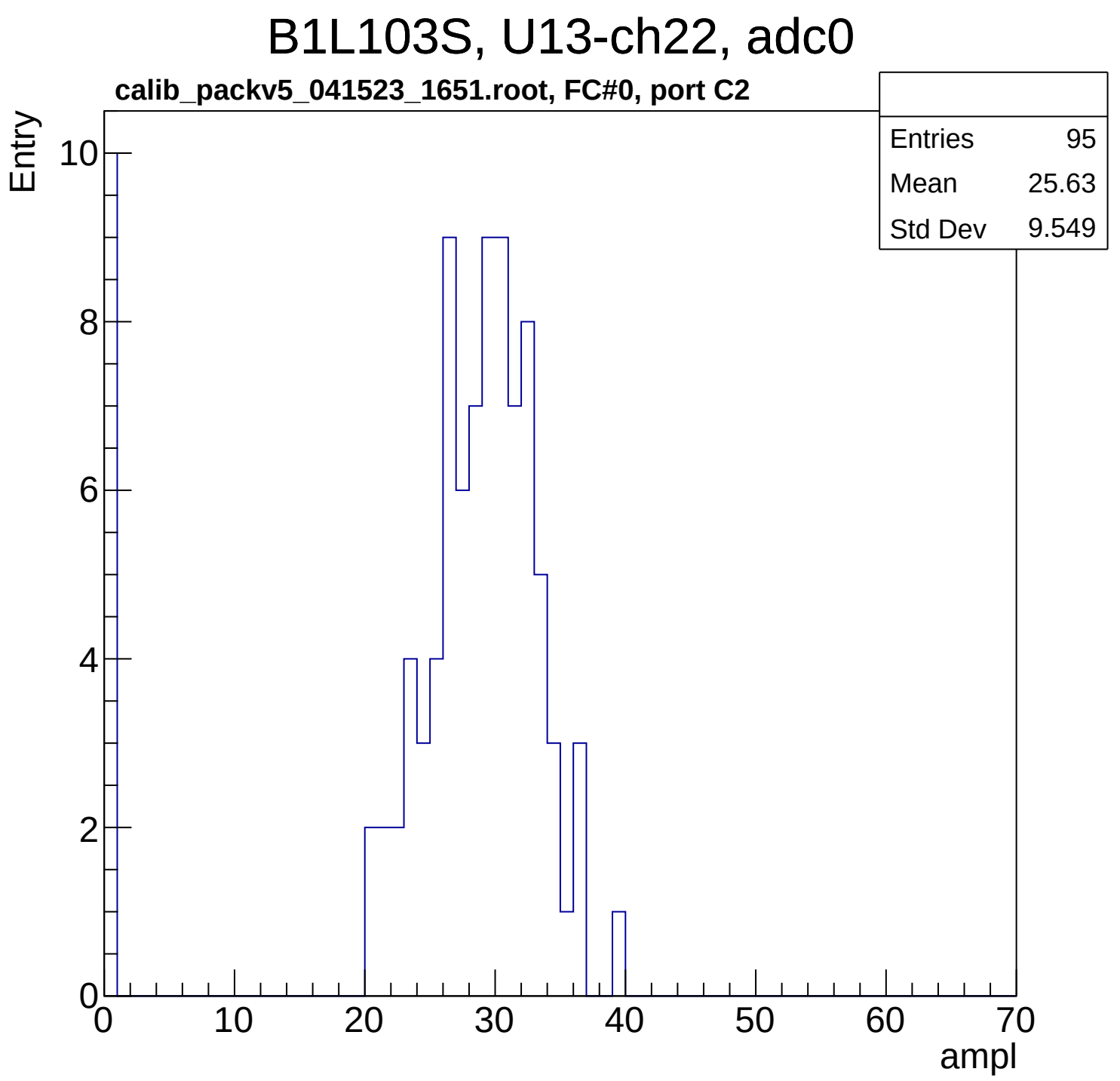
70
ampl


B1L103S, U13-ch22, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 25.63
Std Dev 9.549
Entry
ampl
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4
6
8
10
0
10
20
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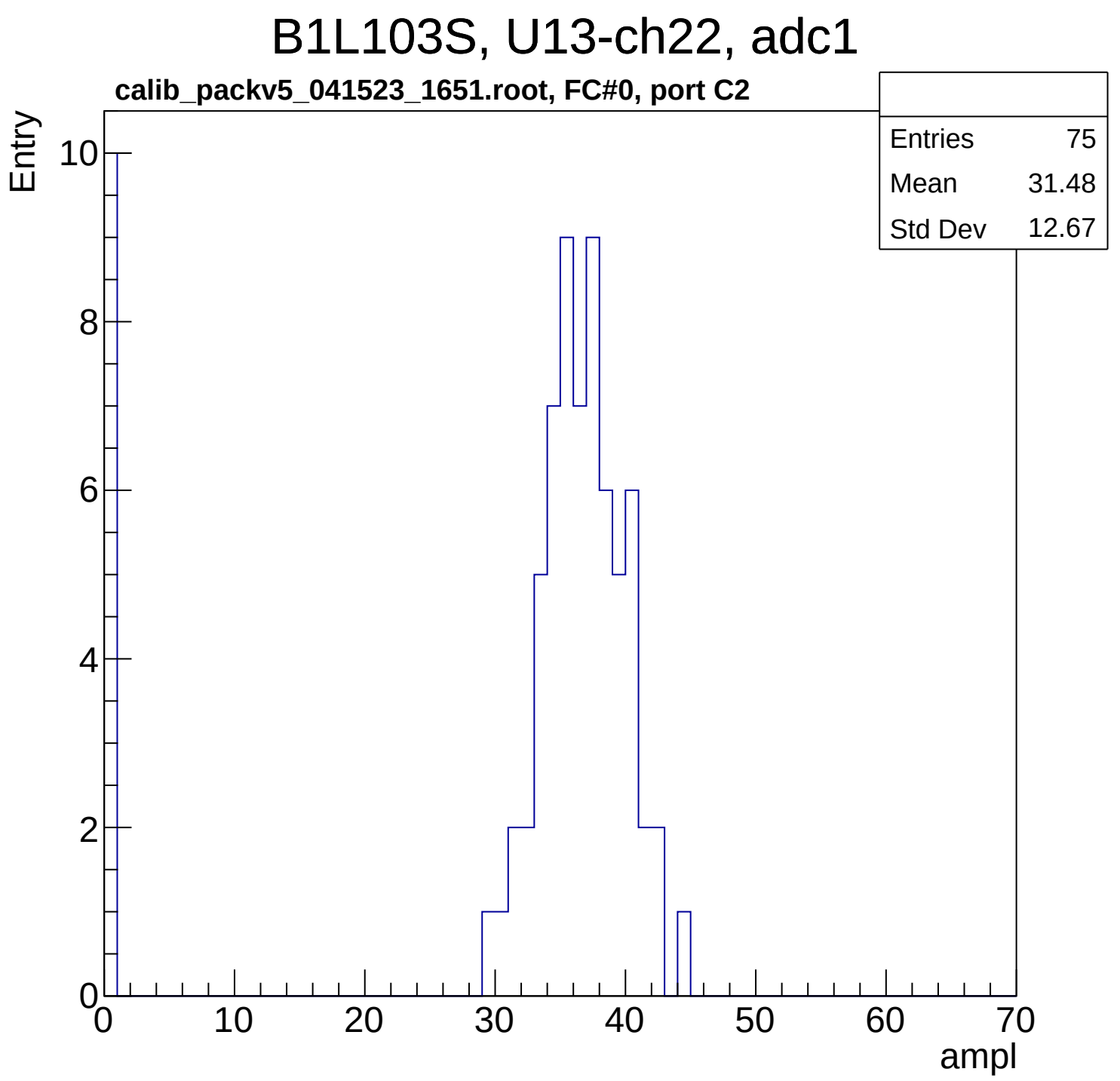
40
50
60
70


B1L103S, U13-ch22, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 31.48
Std Dev 12.67
Entry
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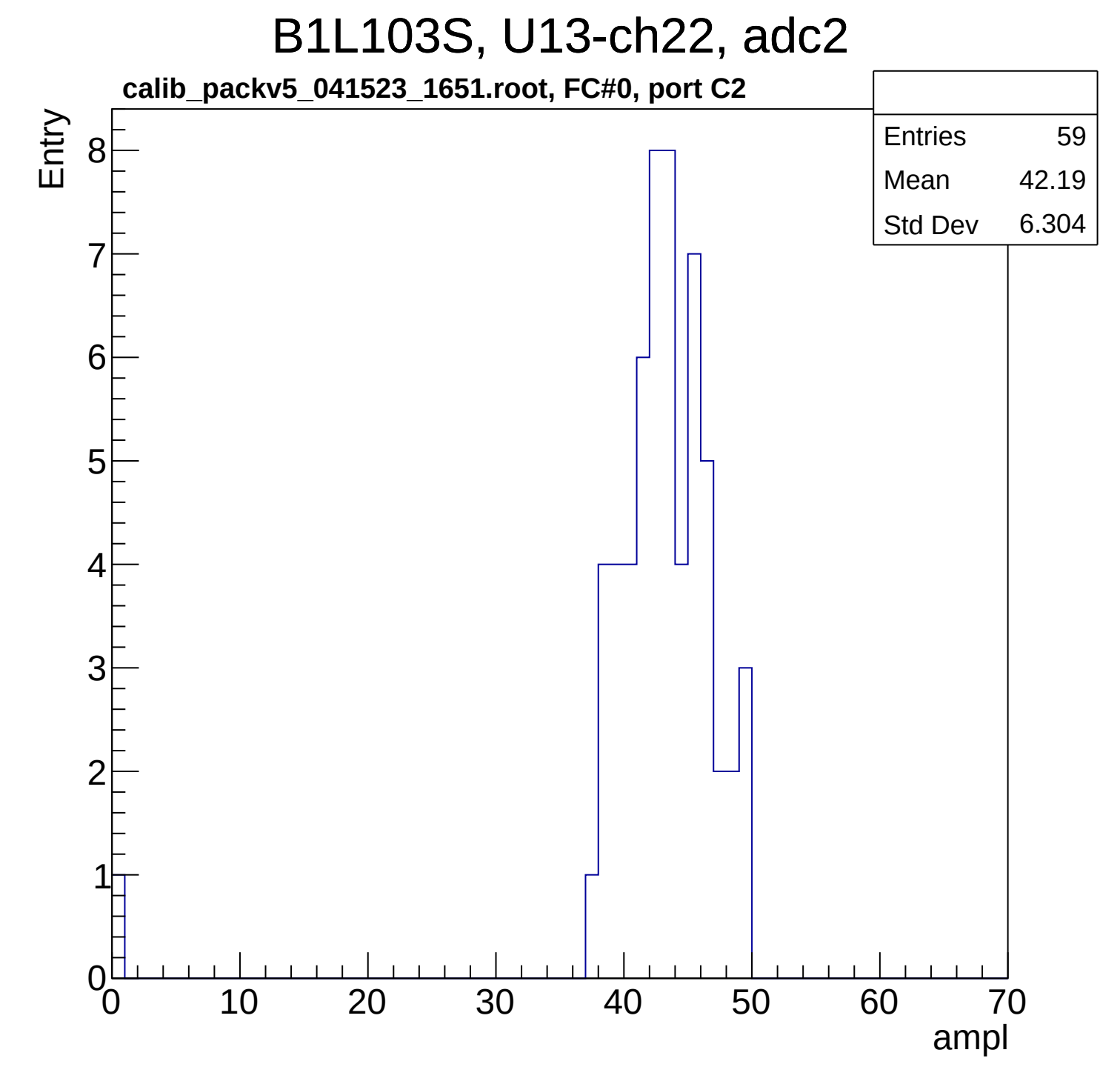
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch22, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 42.19
Std Dev 6.304
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
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60
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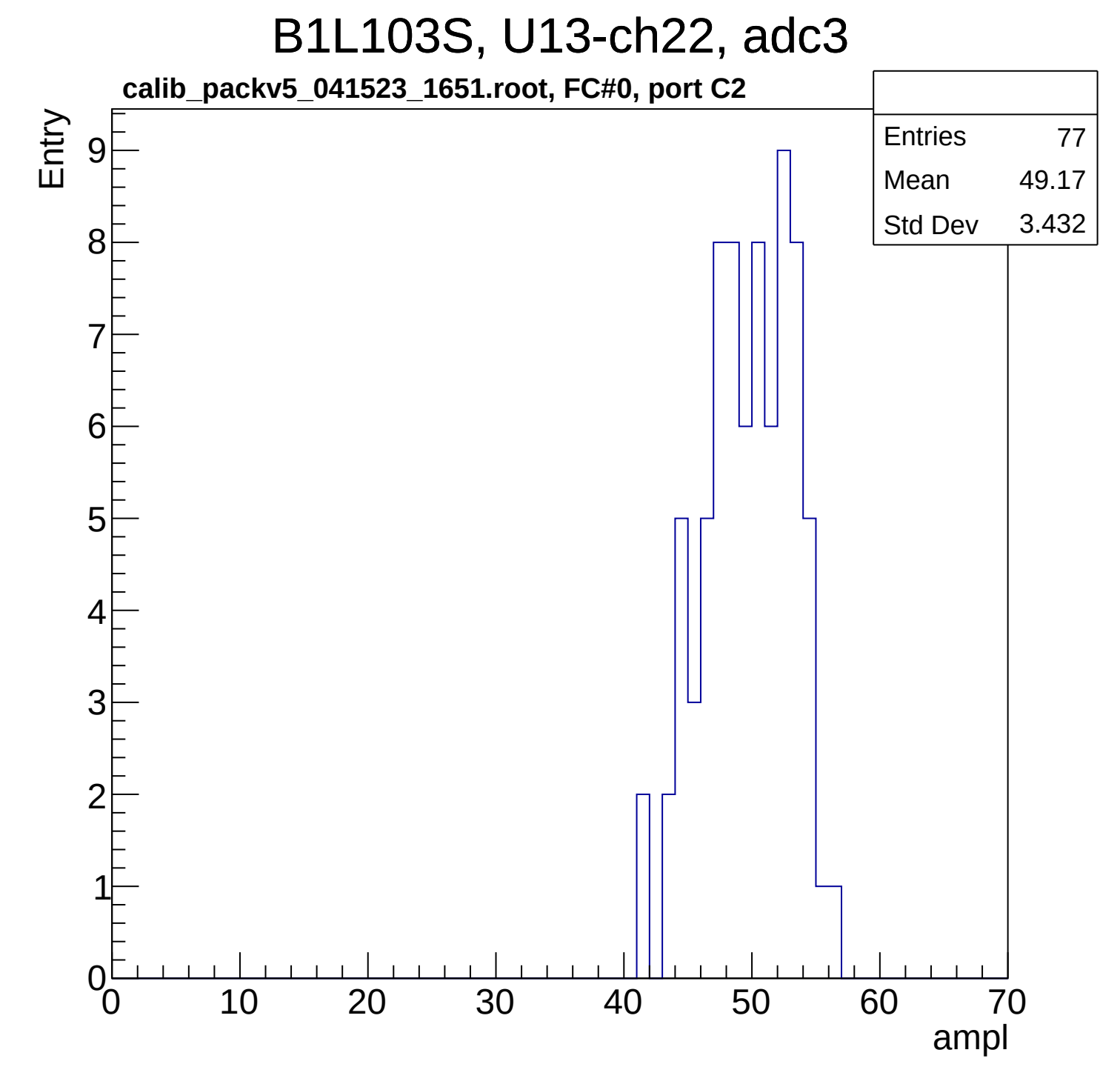
B1L103S, U13-ch22, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 49.17
Std Dev 3.432
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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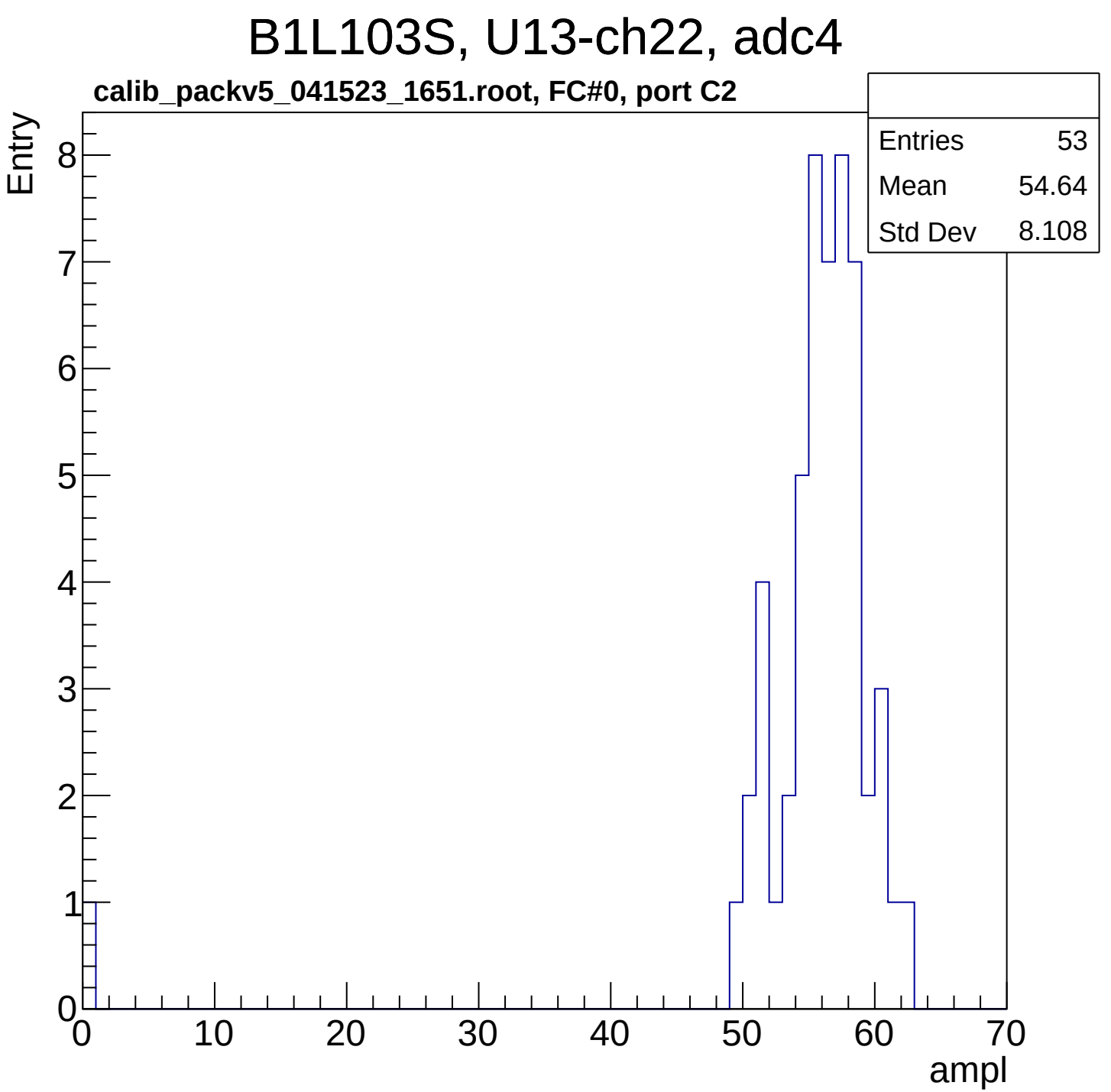
B1L103S, U13-ch22, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 54.64
Std Dev 8.108
Entry
ampl
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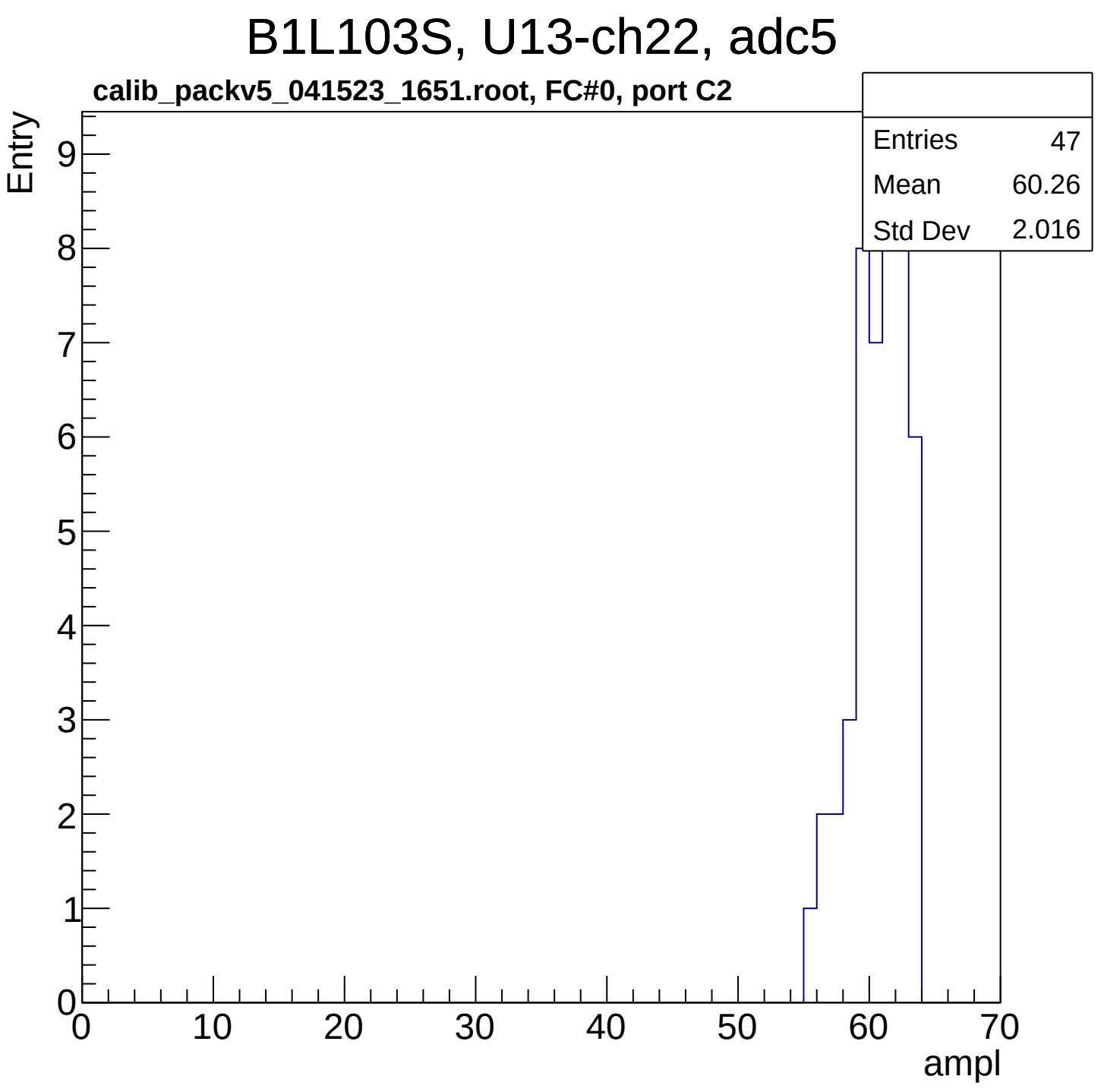
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch22, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 60.26
Std Dev 2.016
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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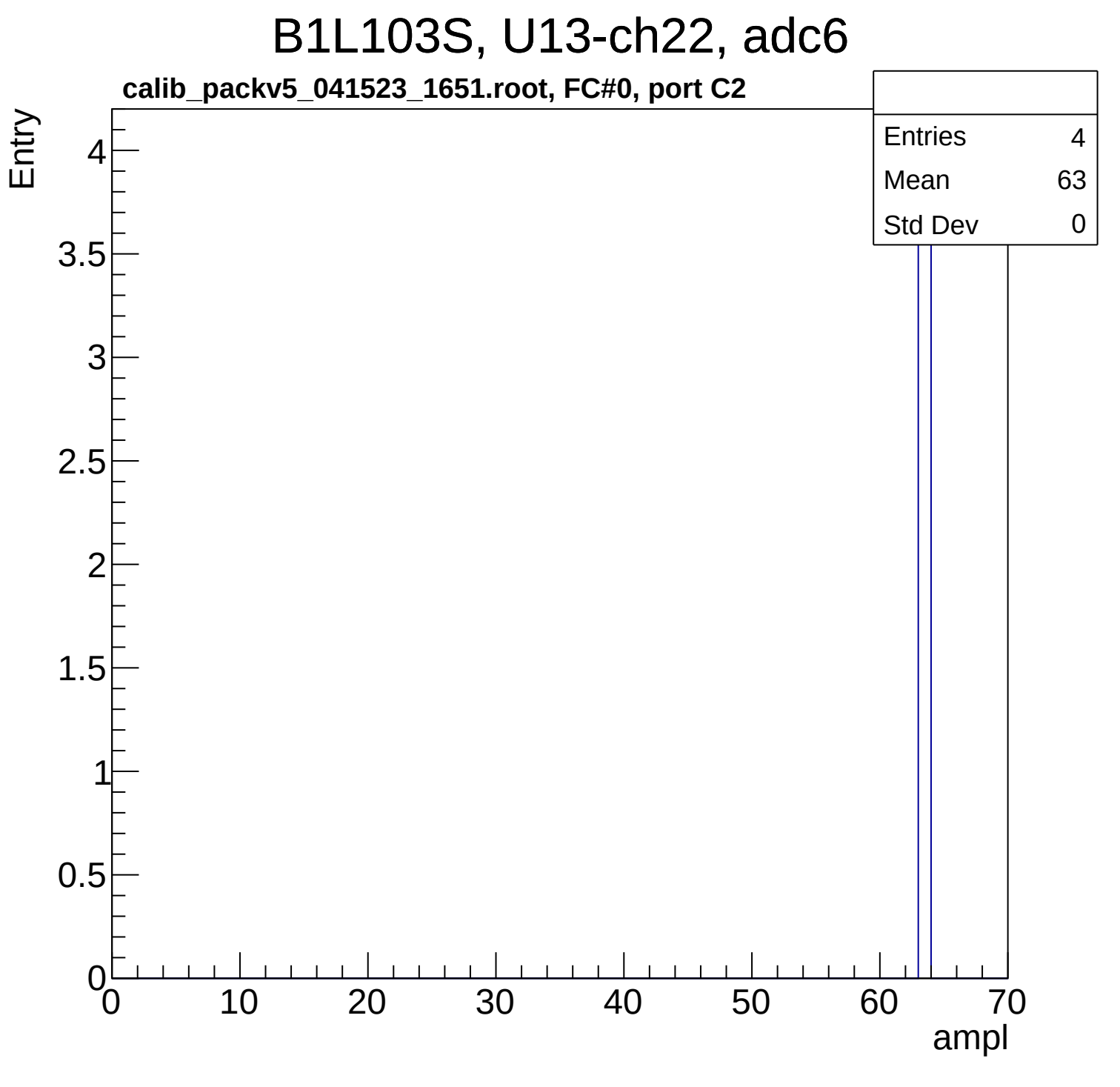
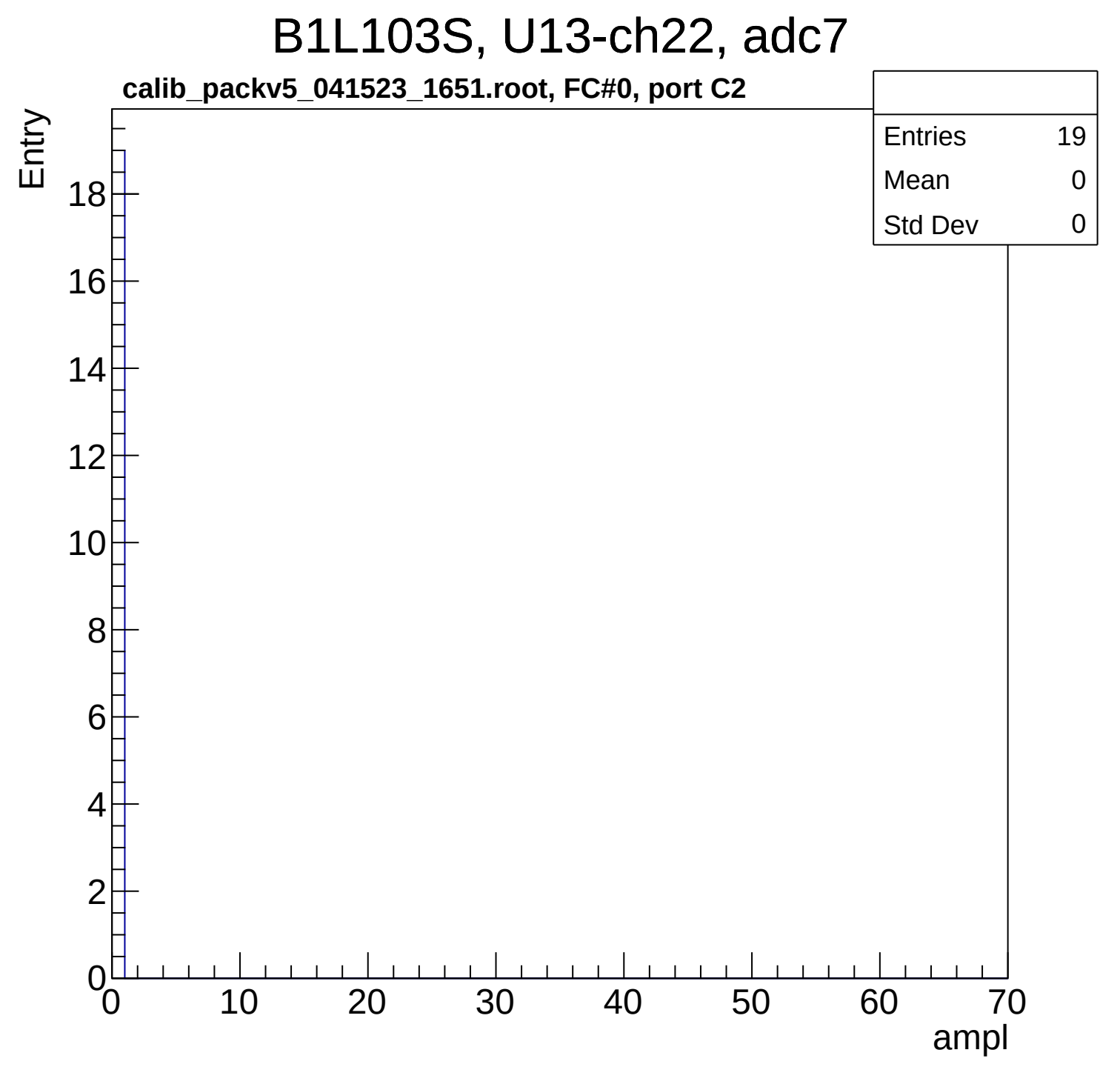
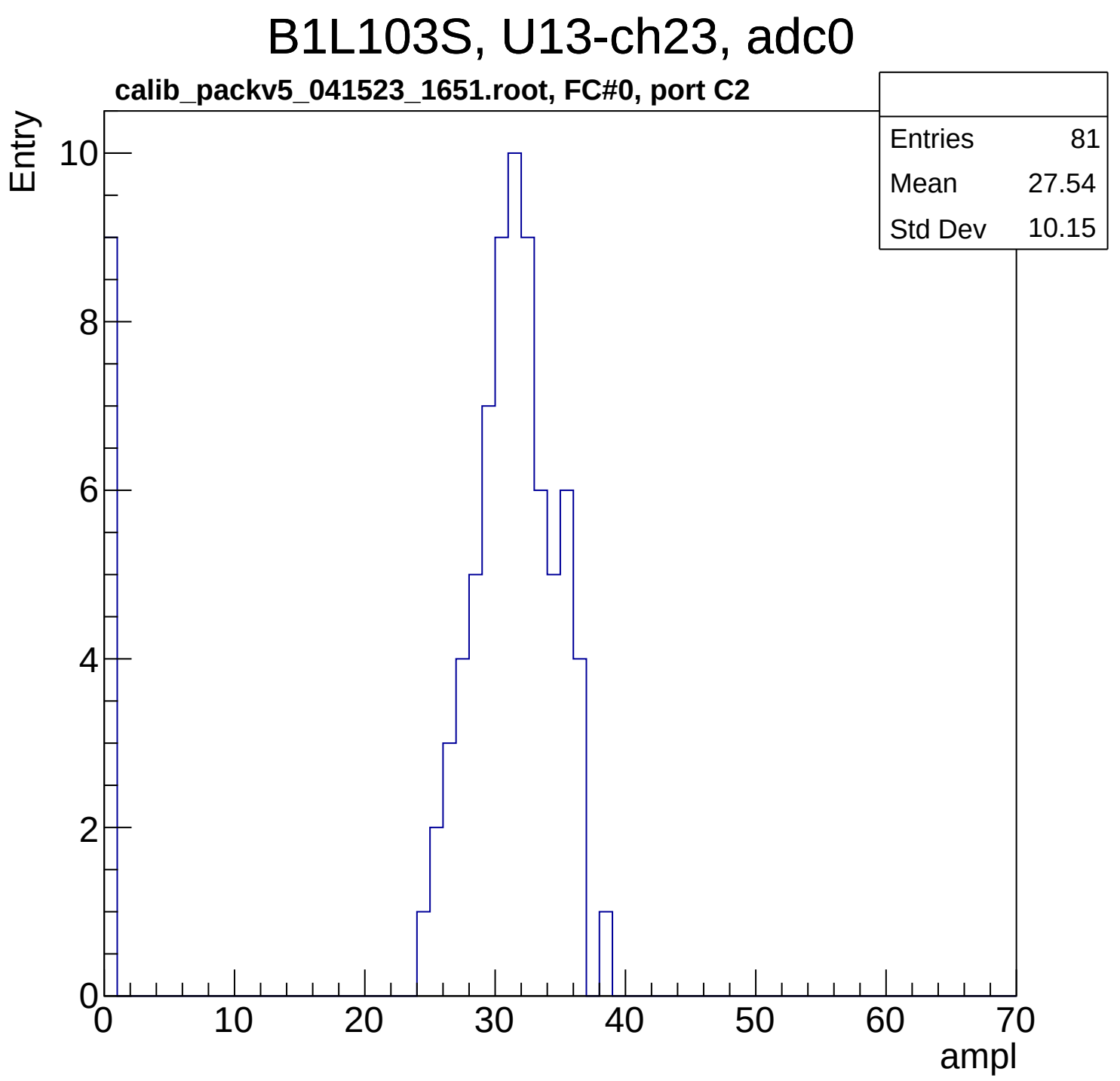
40
50
60
70


B1L103S, U13-ch22, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 63
Std Dev 0
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U13-ch22, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch23, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 27.54
Std Dev 10.15
Entry
ampl
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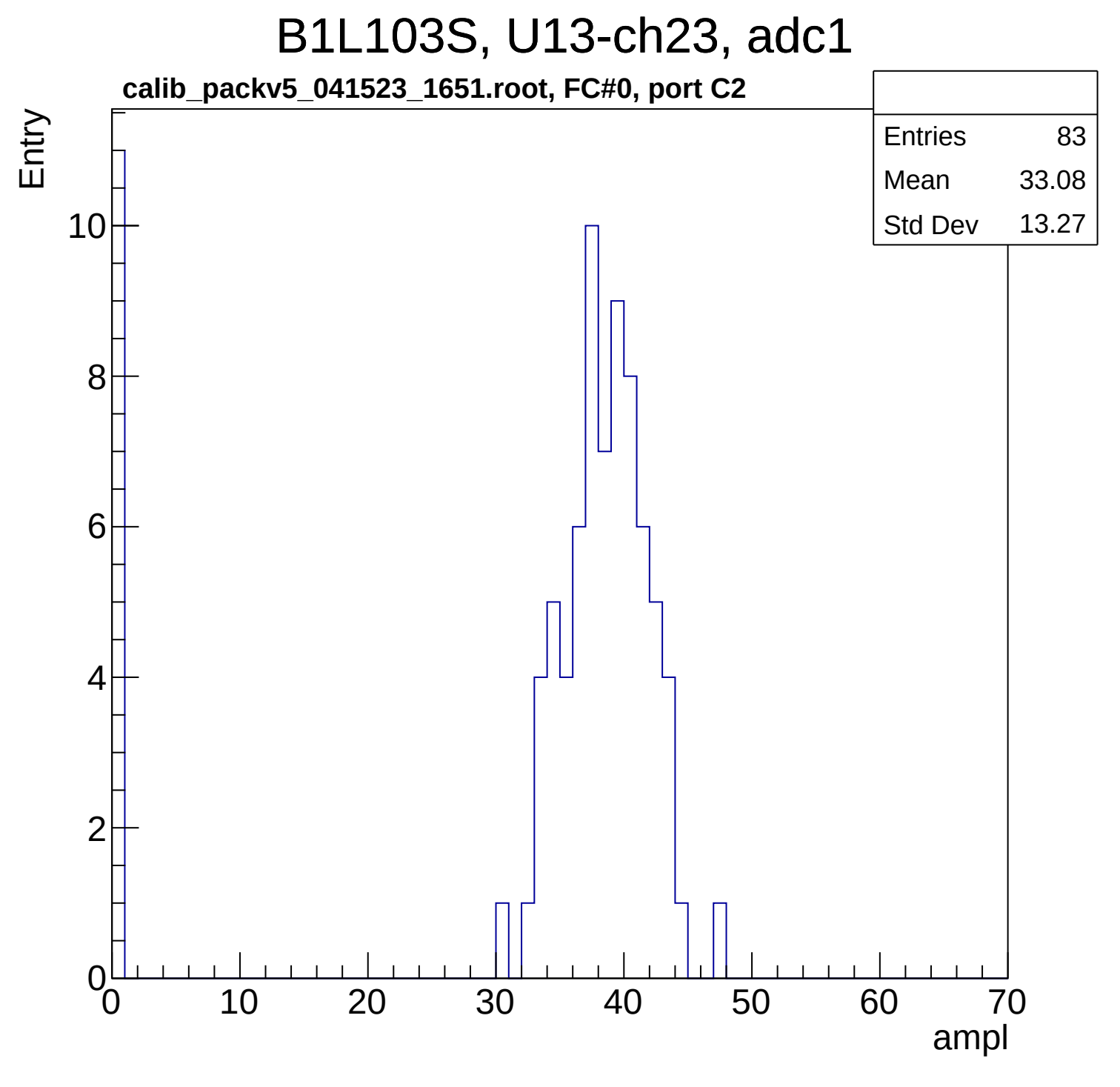
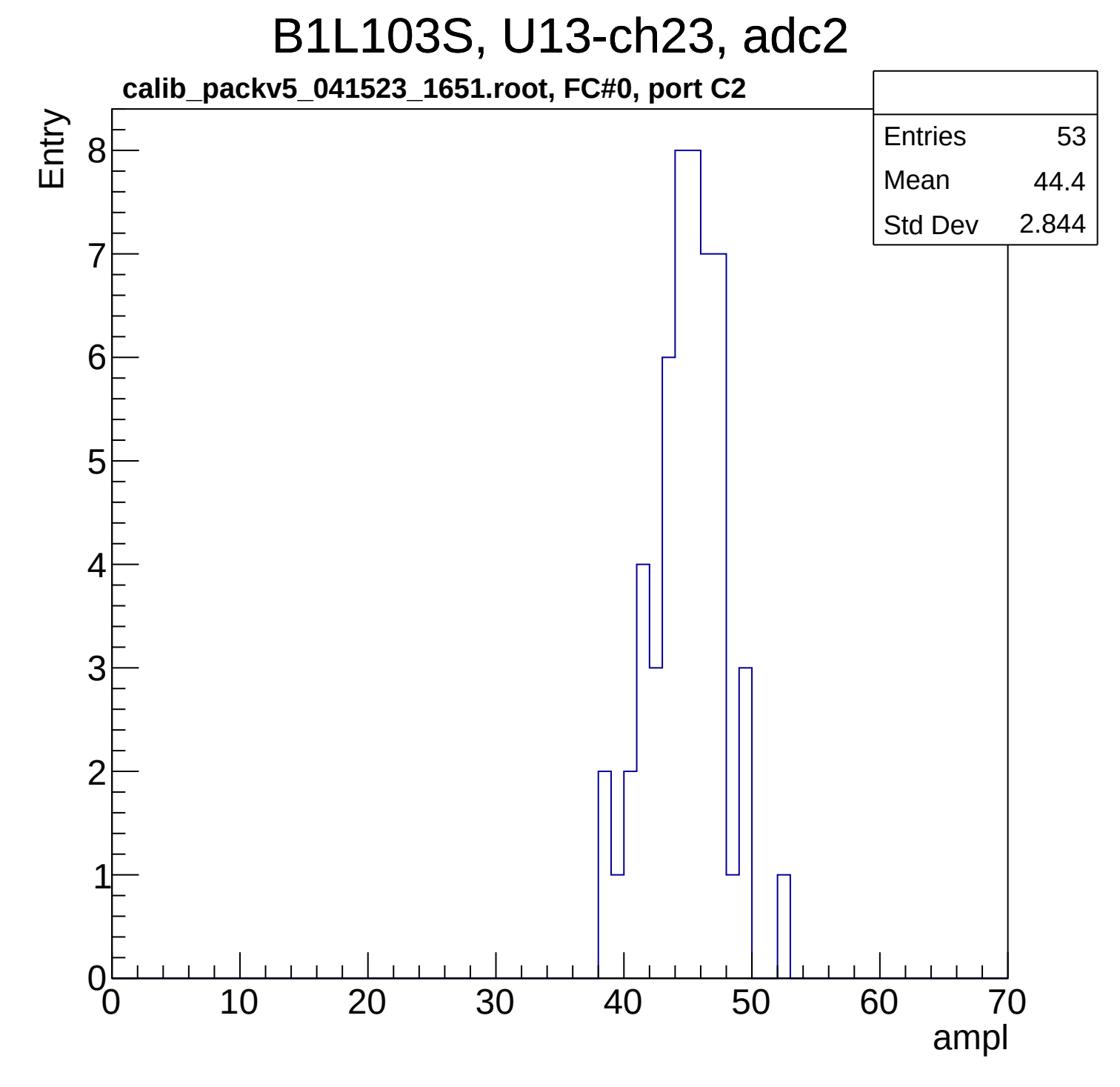
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch23, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 33.08
Std Dev 13.27
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch23, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 44.4
Std Dev 2.844
Entry
ampl
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2
3
4
5
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7
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0
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60
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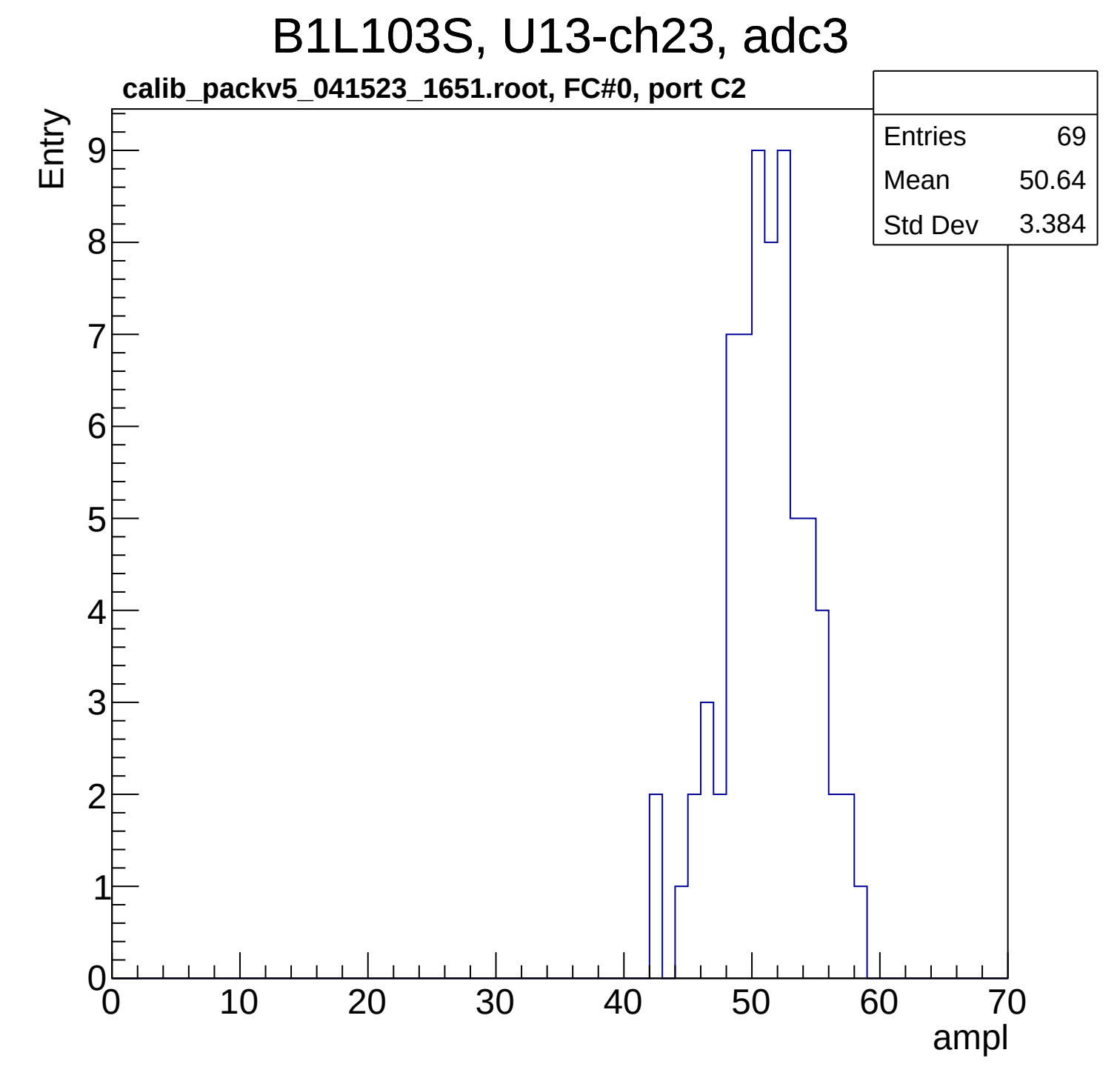
B1L103S, U13-ch23, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 50.64
Std Dev 3.384
Entry
ampl
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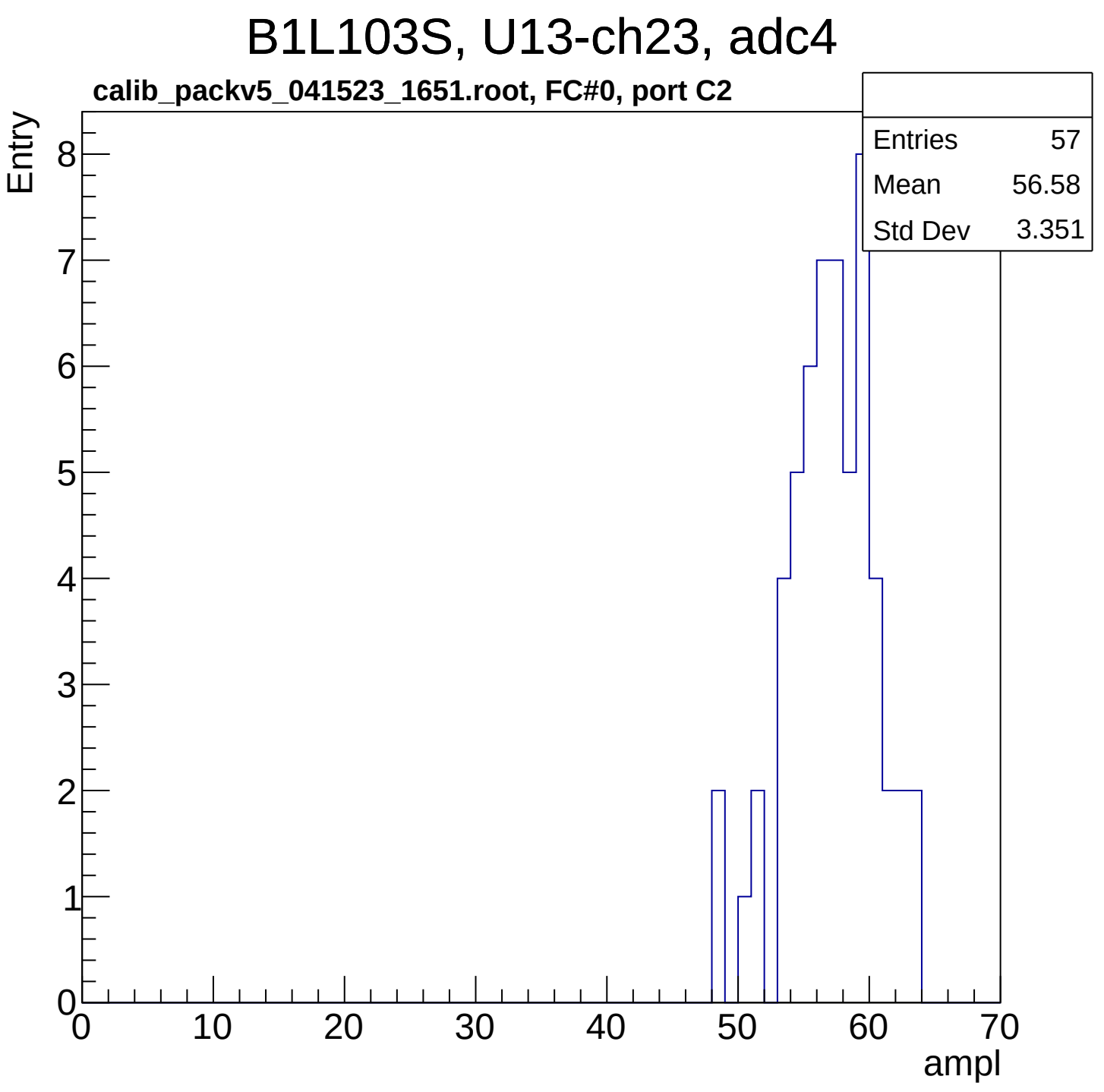
B1L103S, U13-ch23, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 56.58
Std Dev 3.351
Entry
ampl
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2
3
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5
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7
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0
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40
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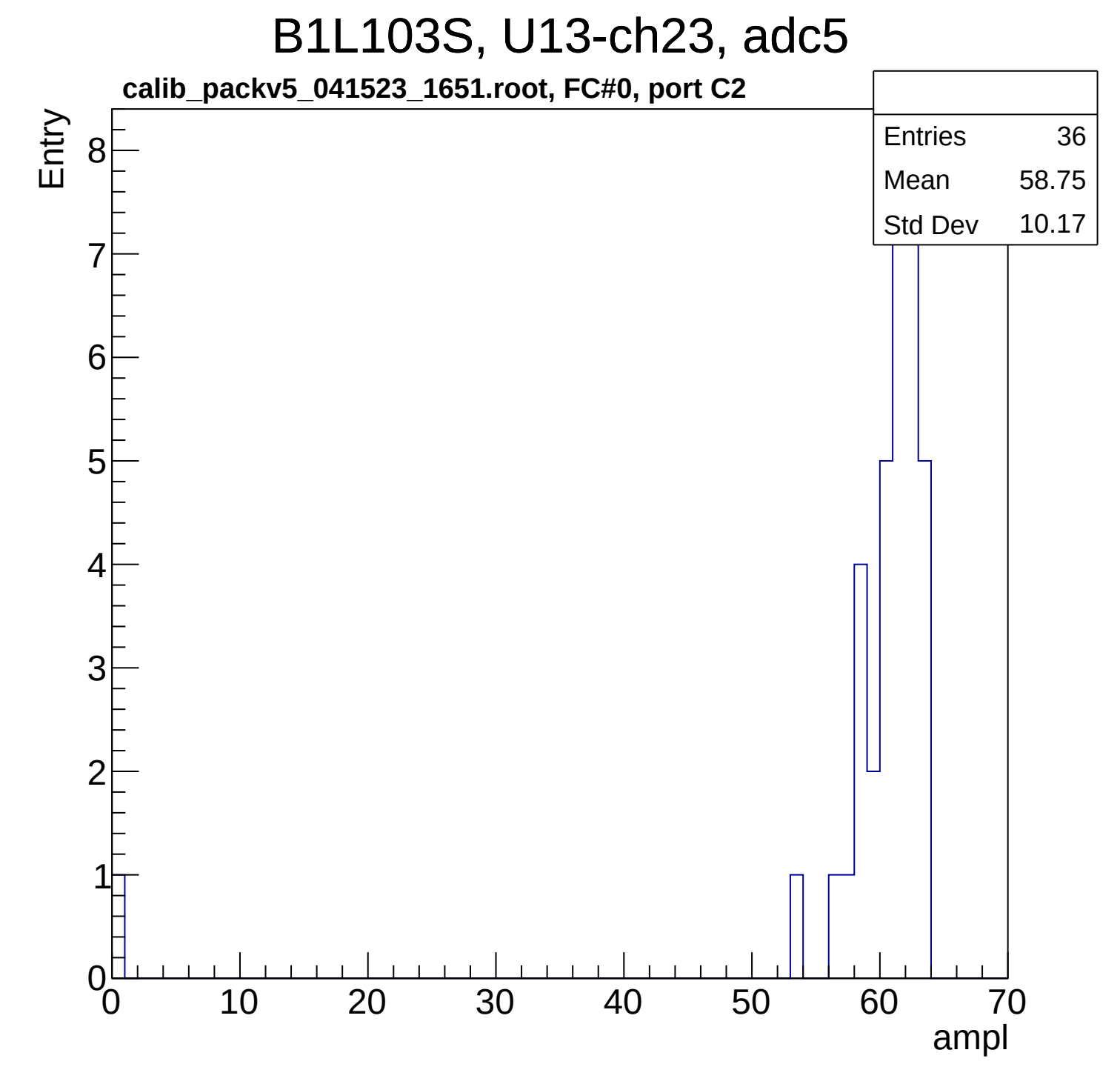
B1L103S, U13-ch23, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 58.75
Std Dev 10.17
Entry
ampl
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2
3
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7
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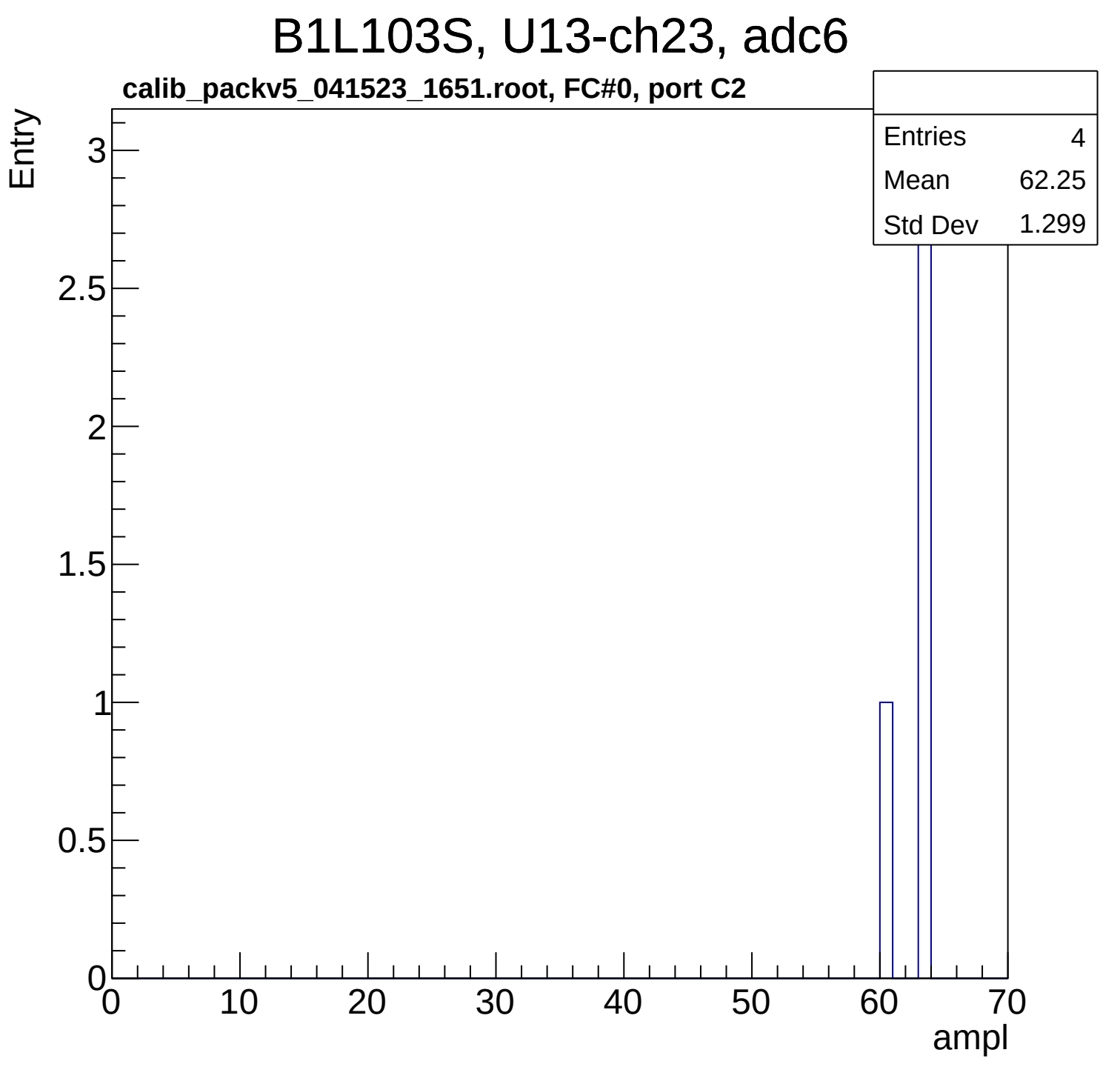
B1L103S, U13-ch23, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.25
Std Dev 1.299
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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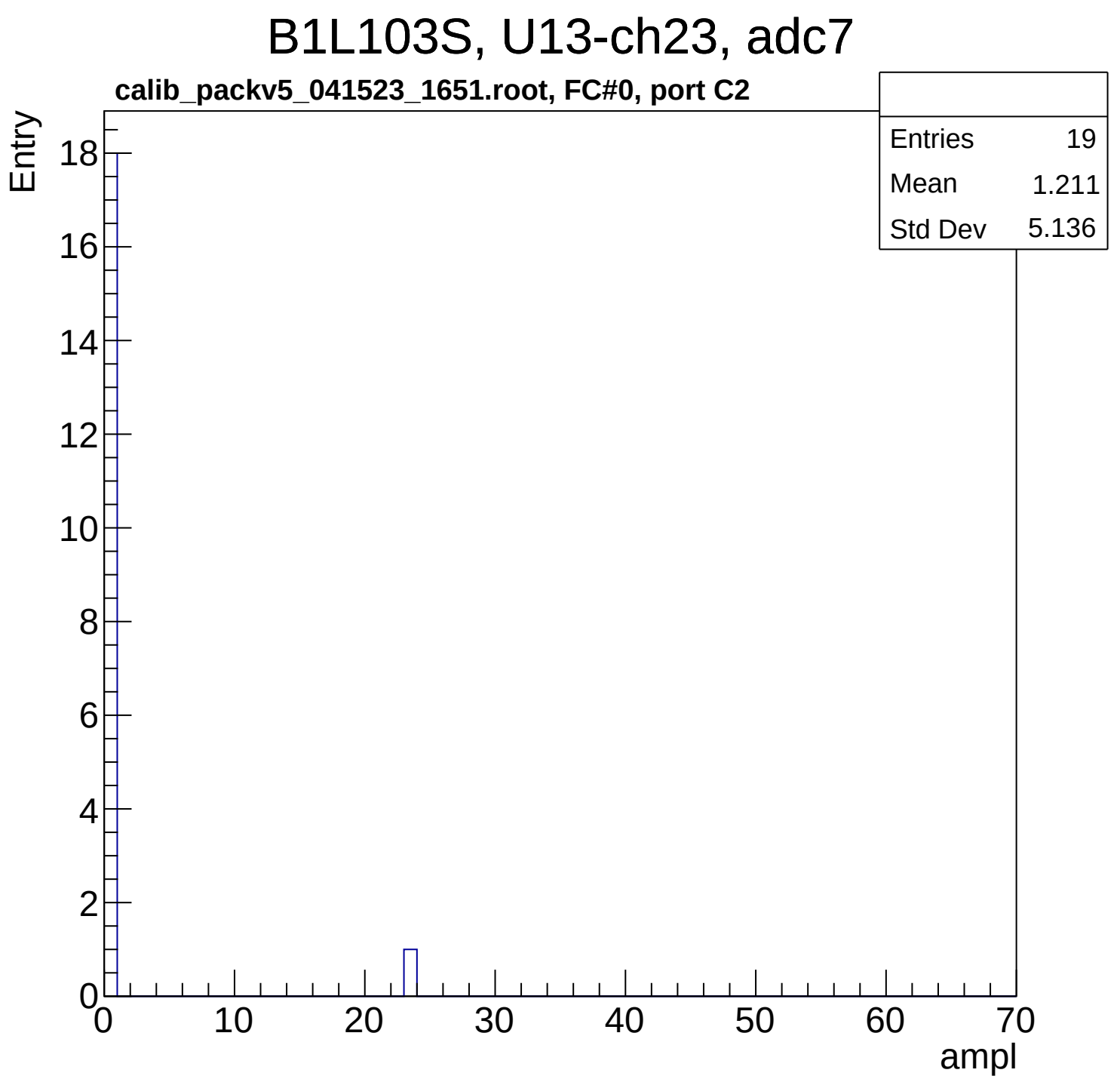
B1L103S, U13-ch23, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.211
Std Dev 5.136
Entry
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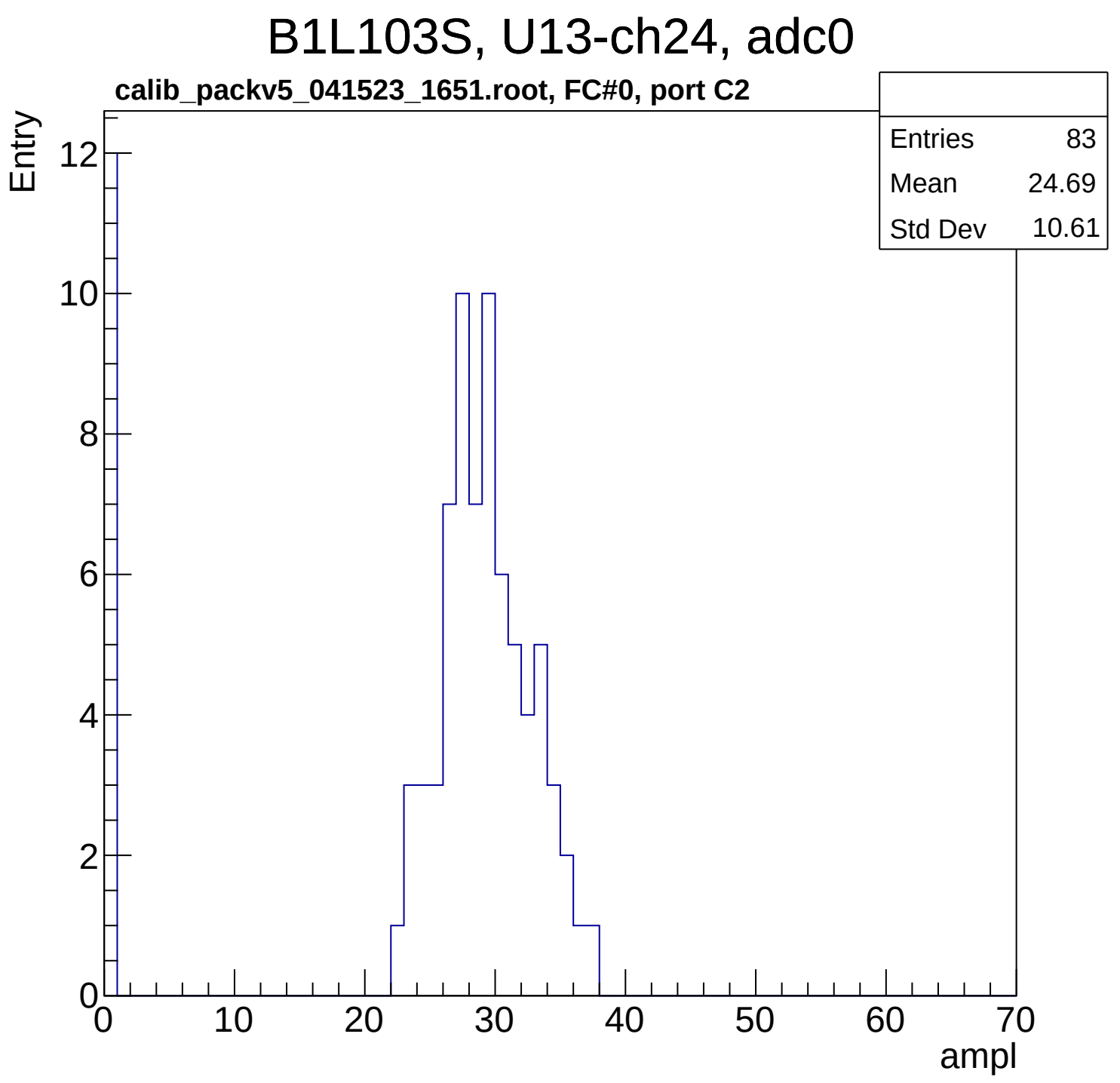
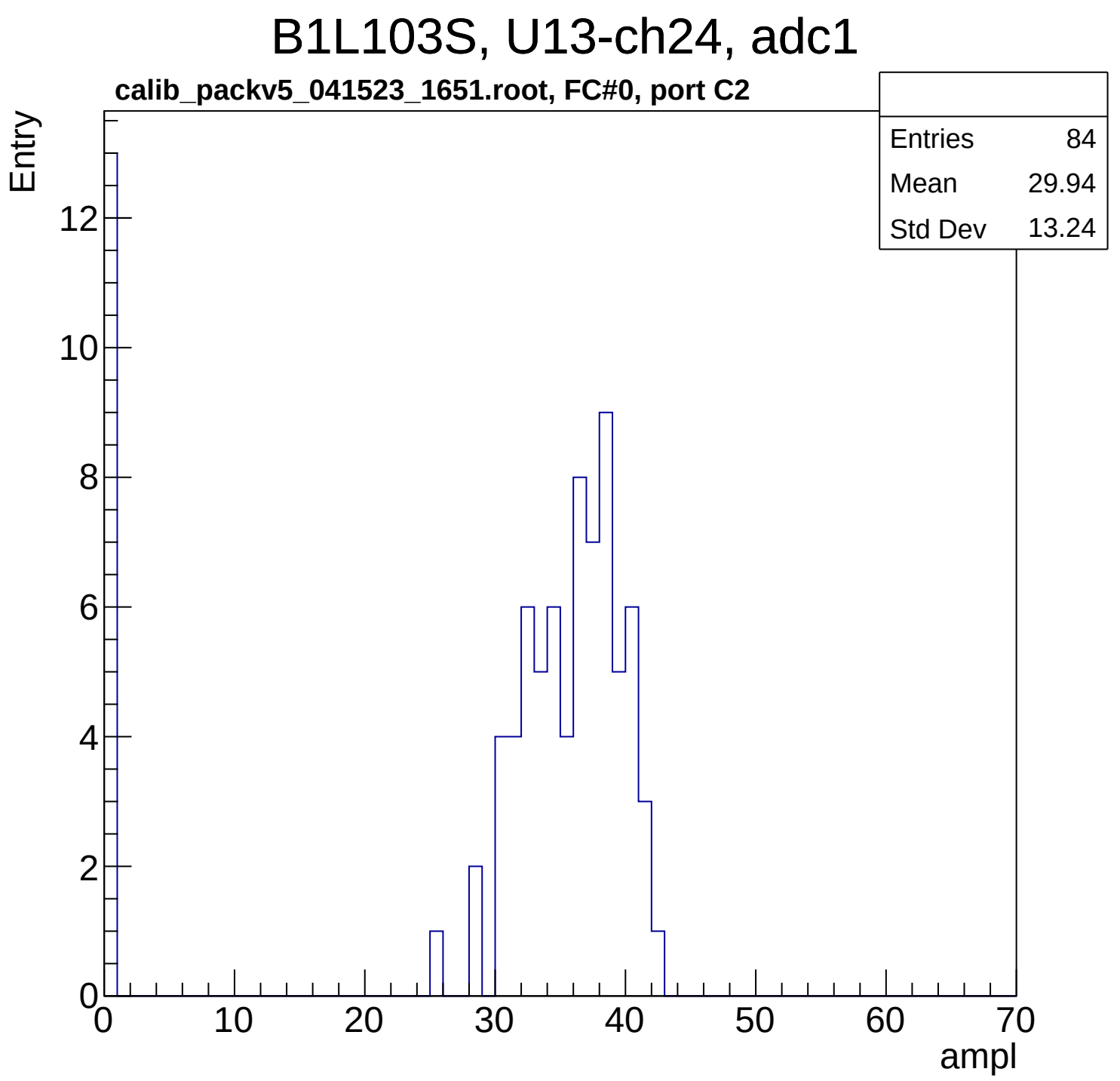
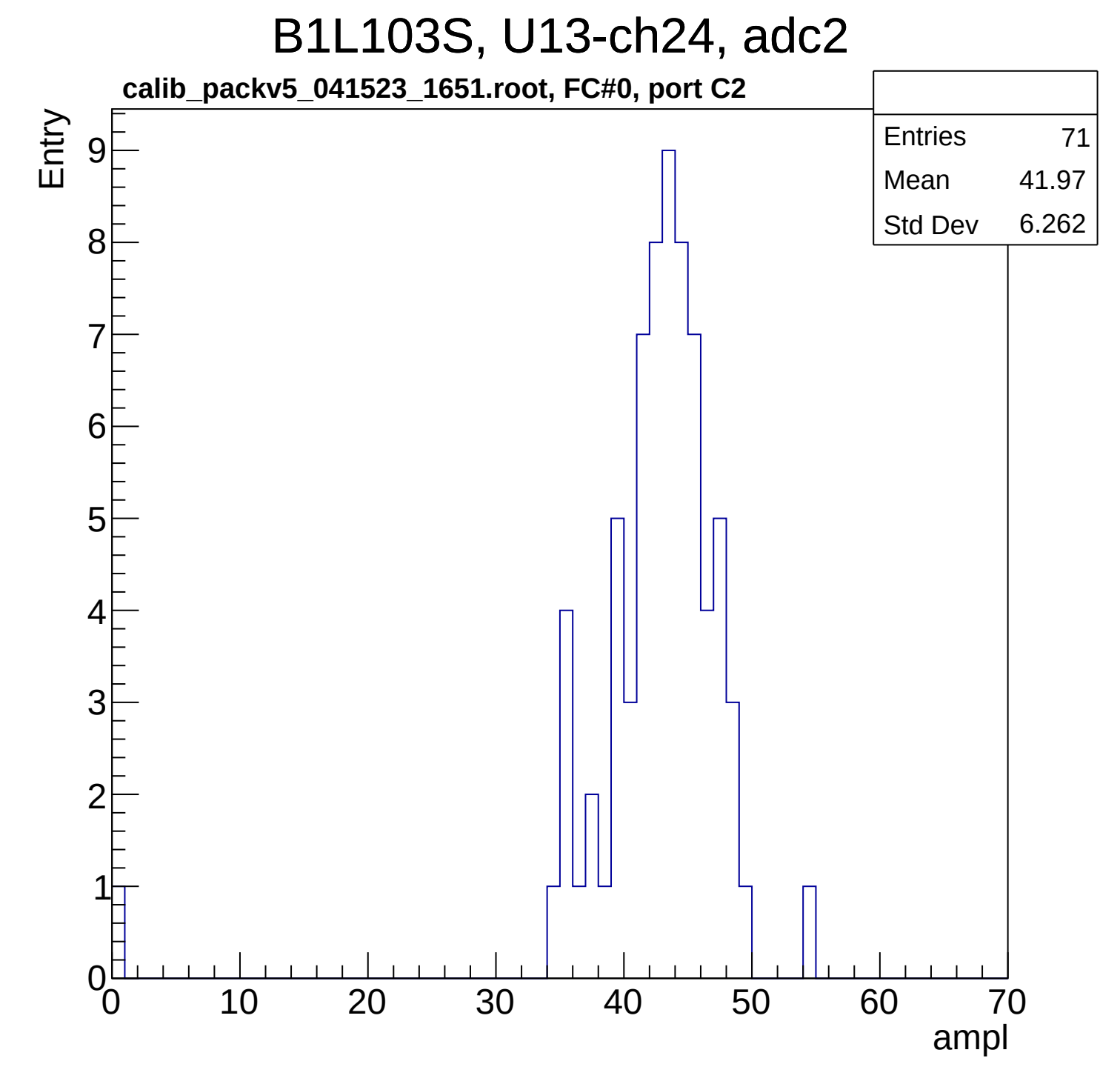
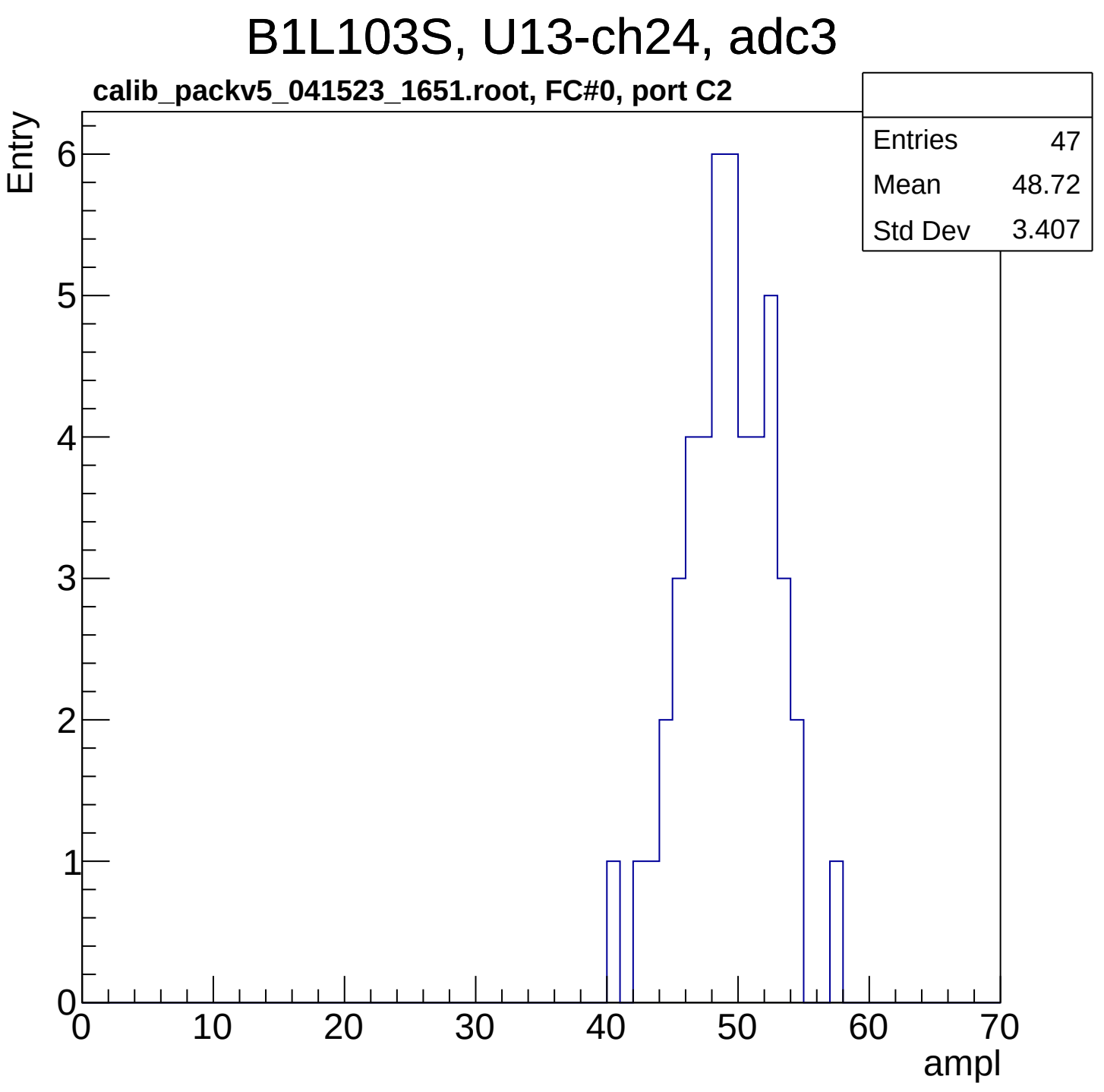
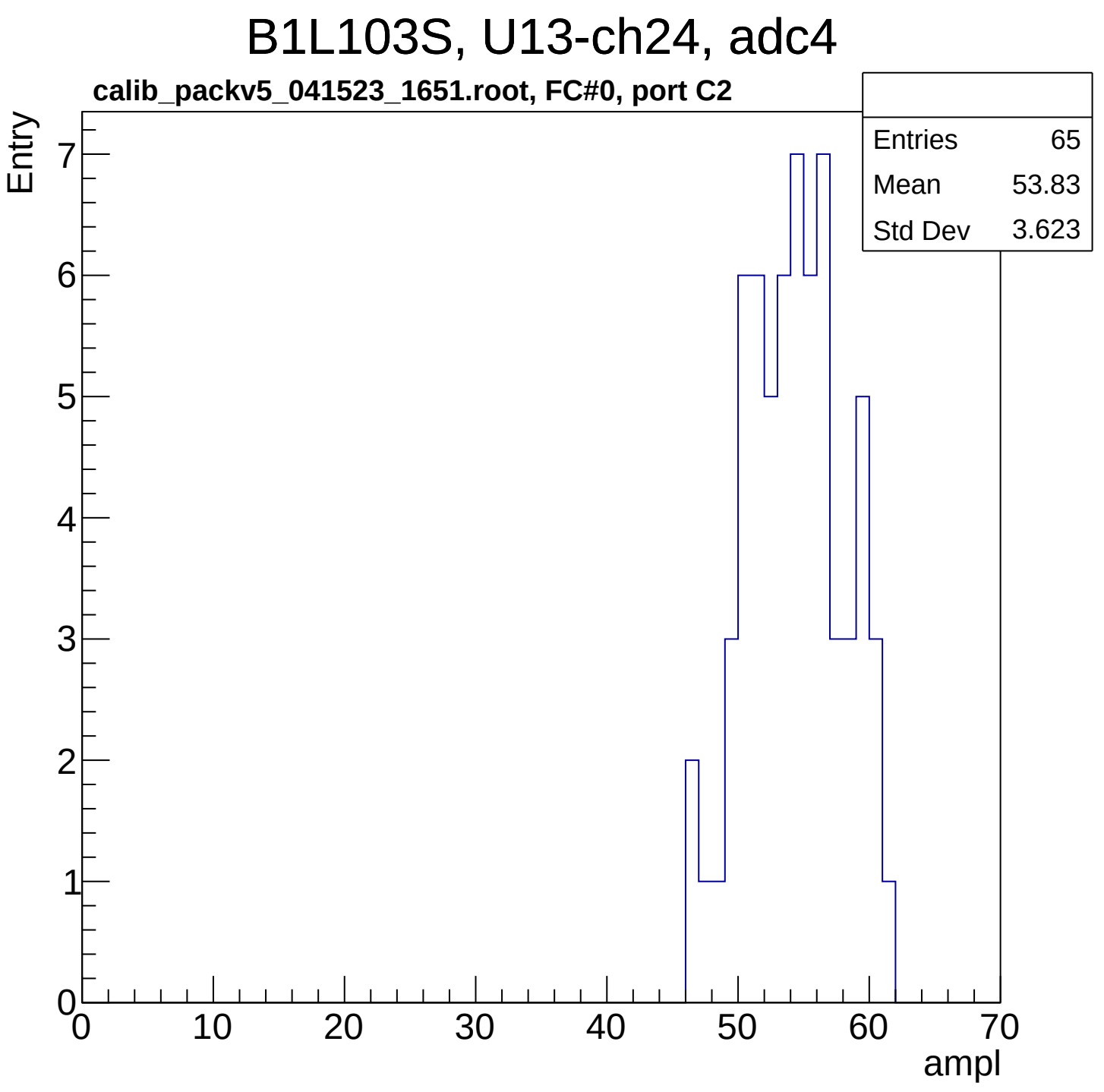
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch24, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 24.69
Std Dev 10.61
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch24, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 29.94
Std Dev 13.24
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch24, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 41.97
Std Dev 6.262
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch24, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 48.72
Std Dev 3.407
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U13-ch24, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 53.83
Std Dev 3.623
Entry
ampl
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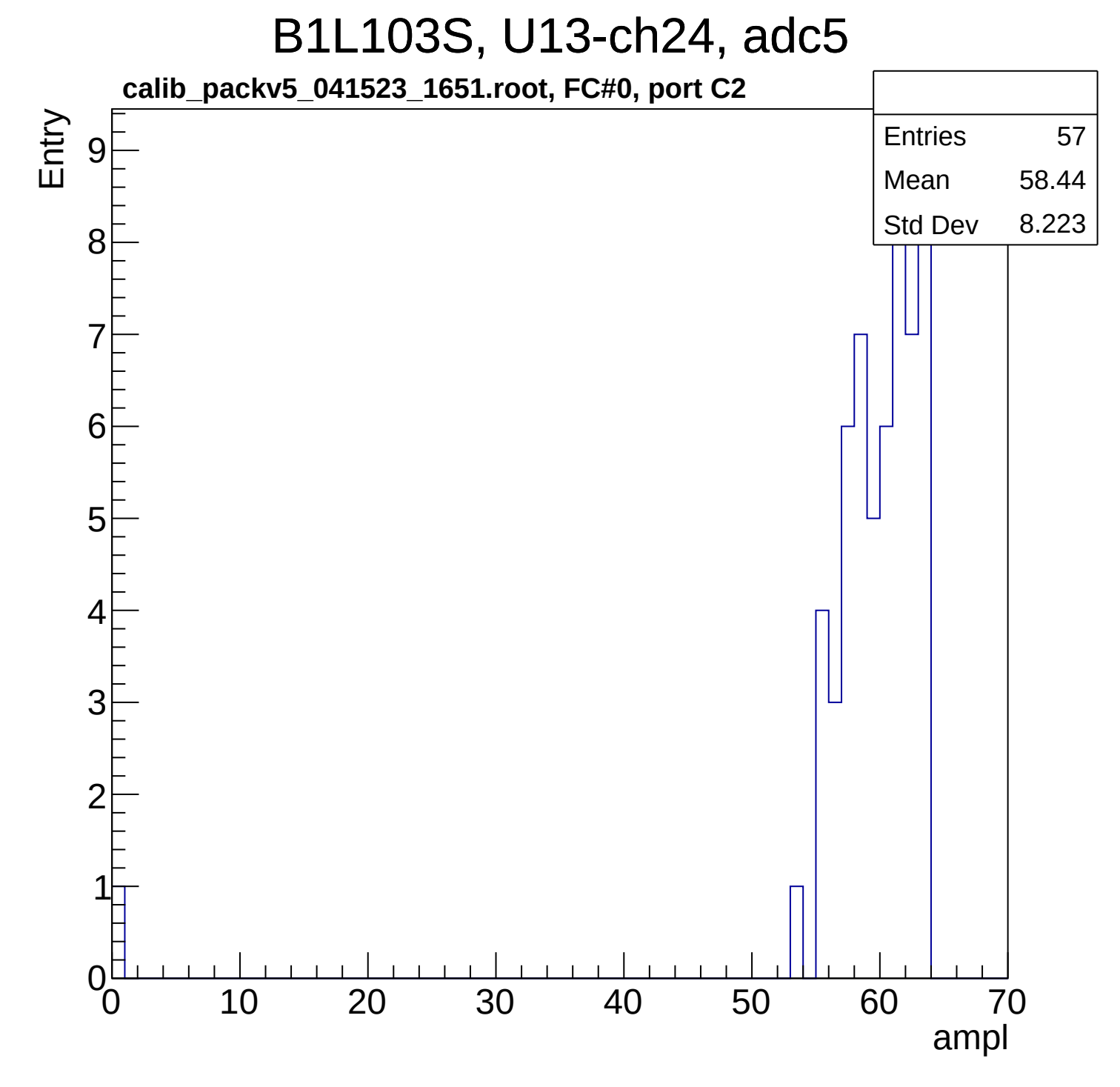
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch24, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.44
Std Dev 8.223
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
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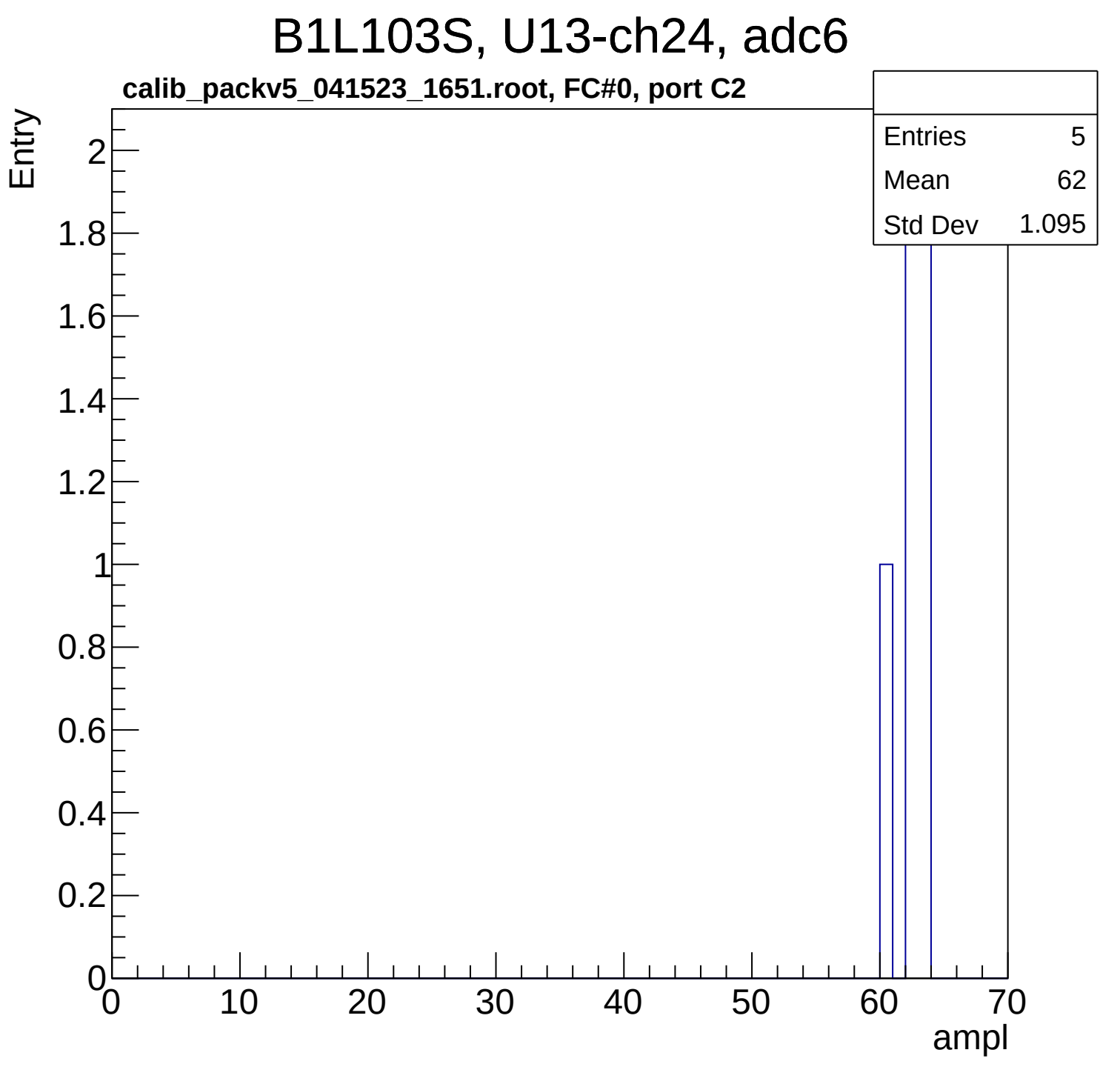
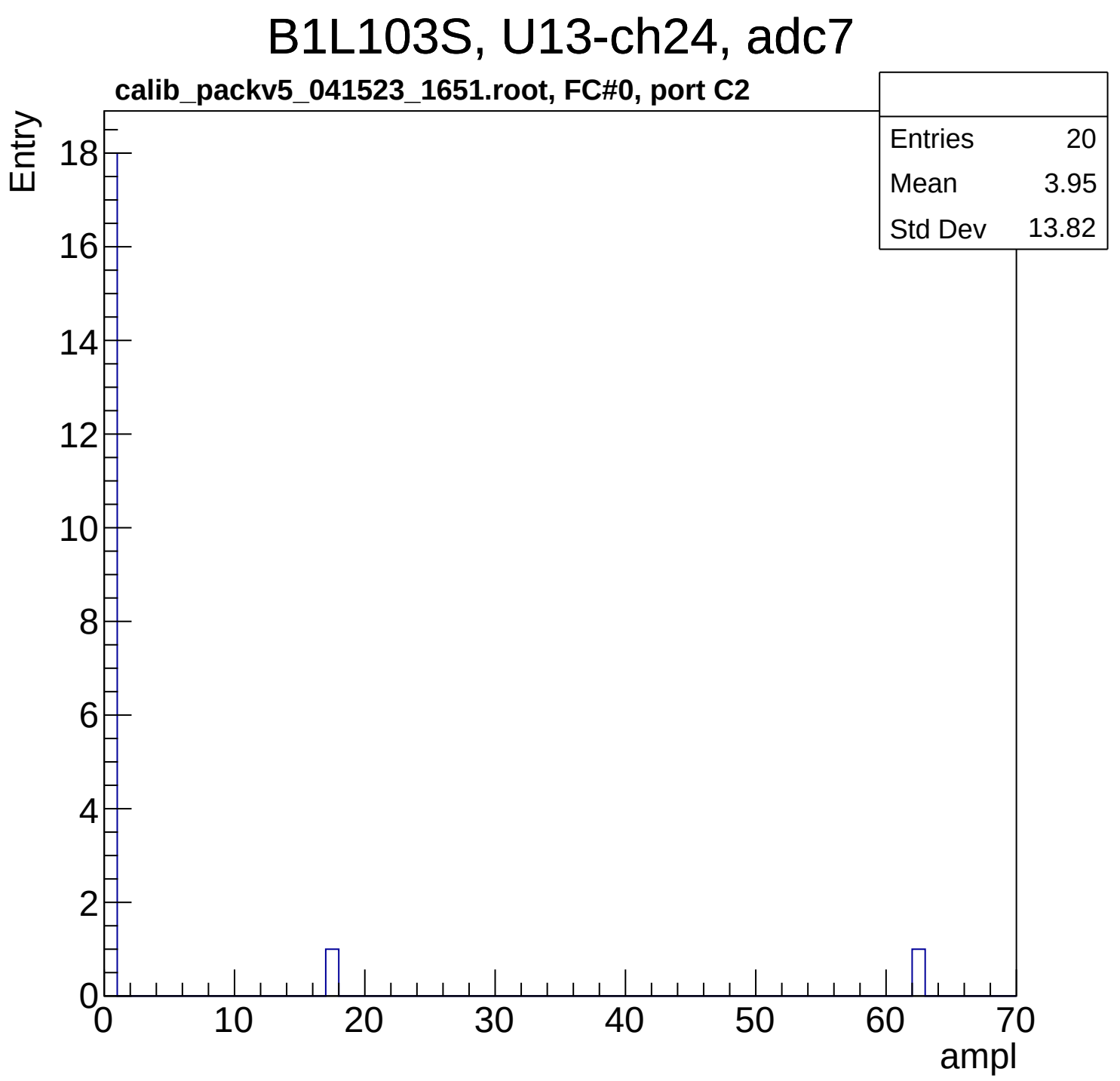
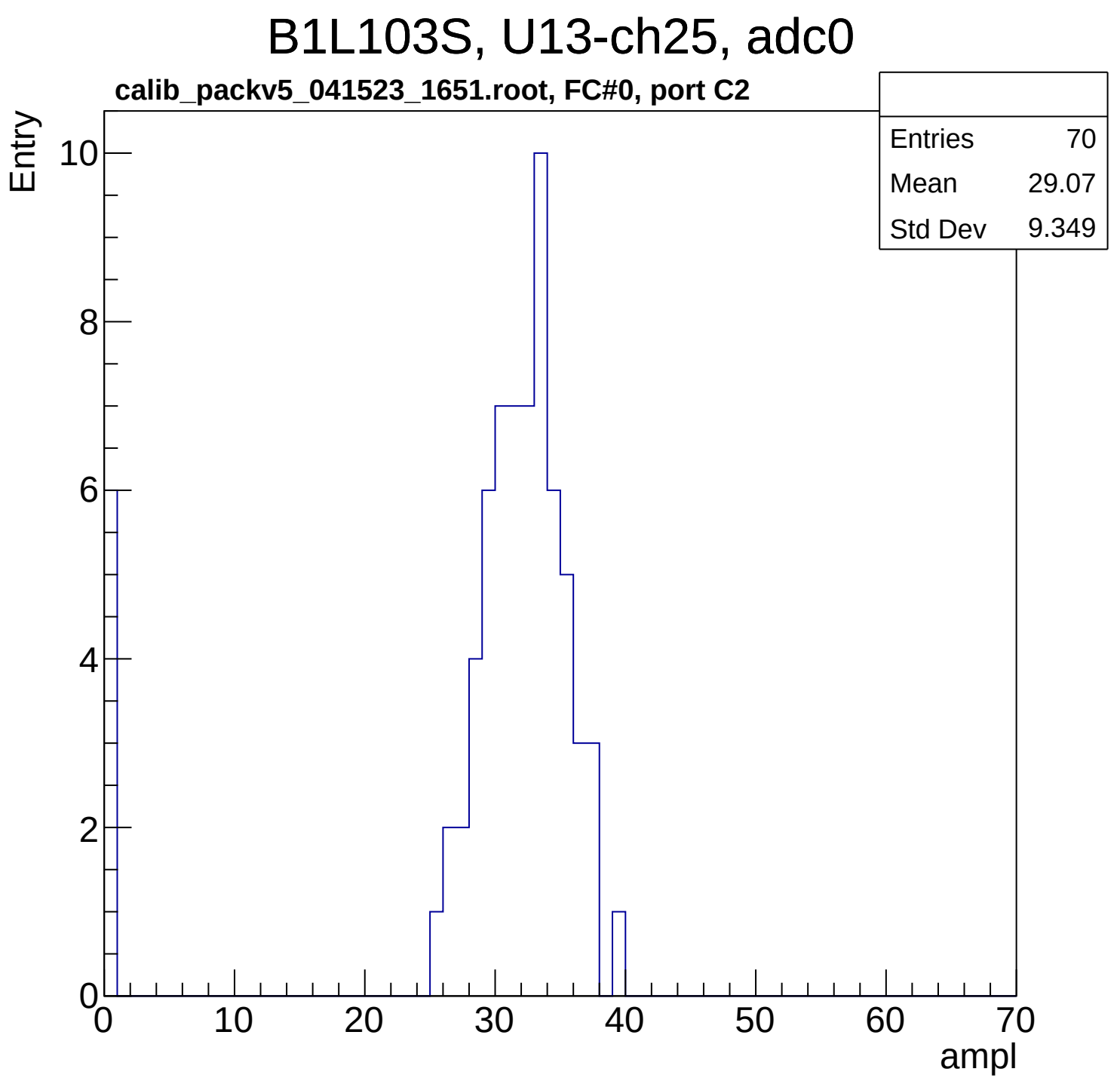
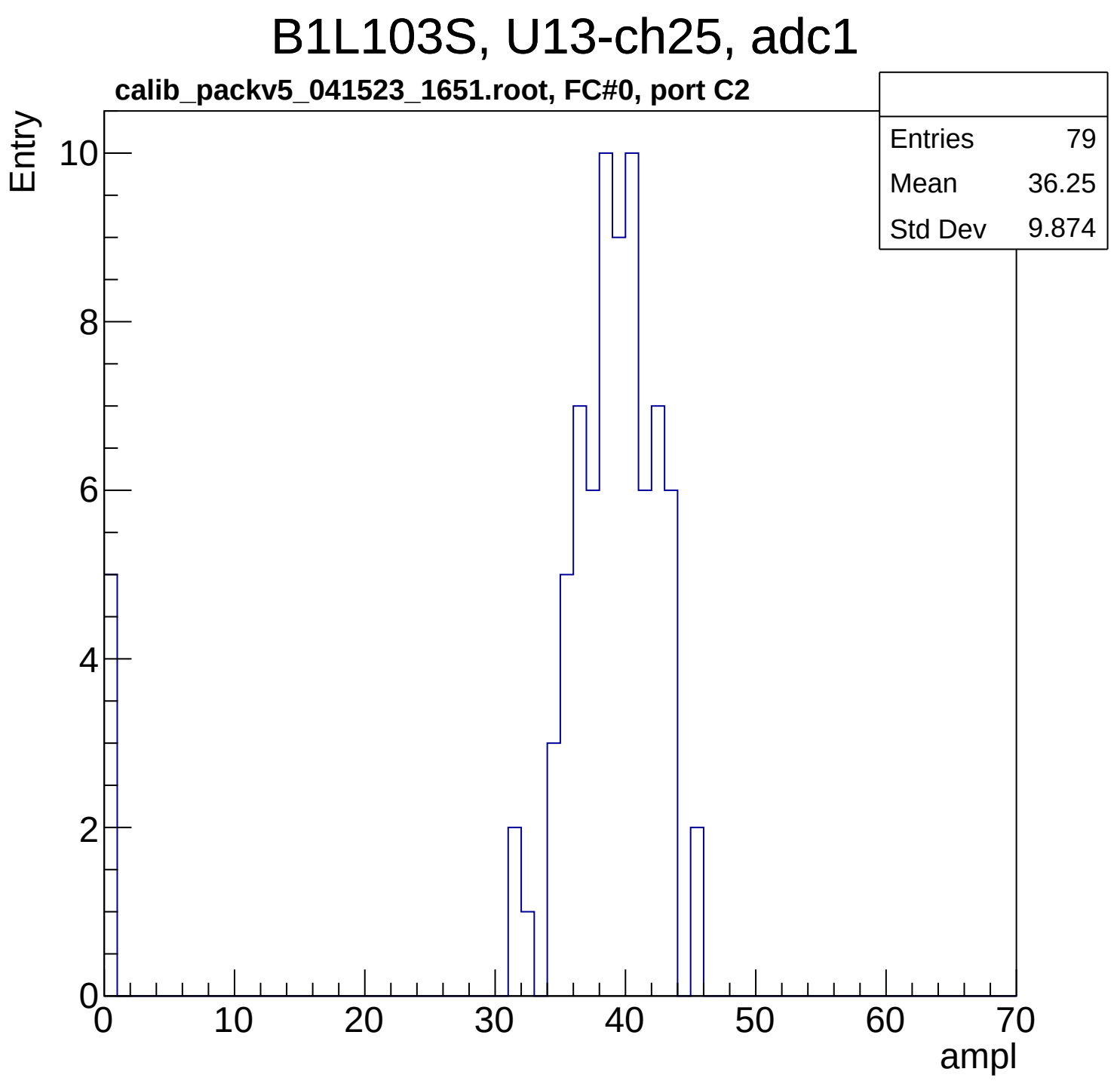
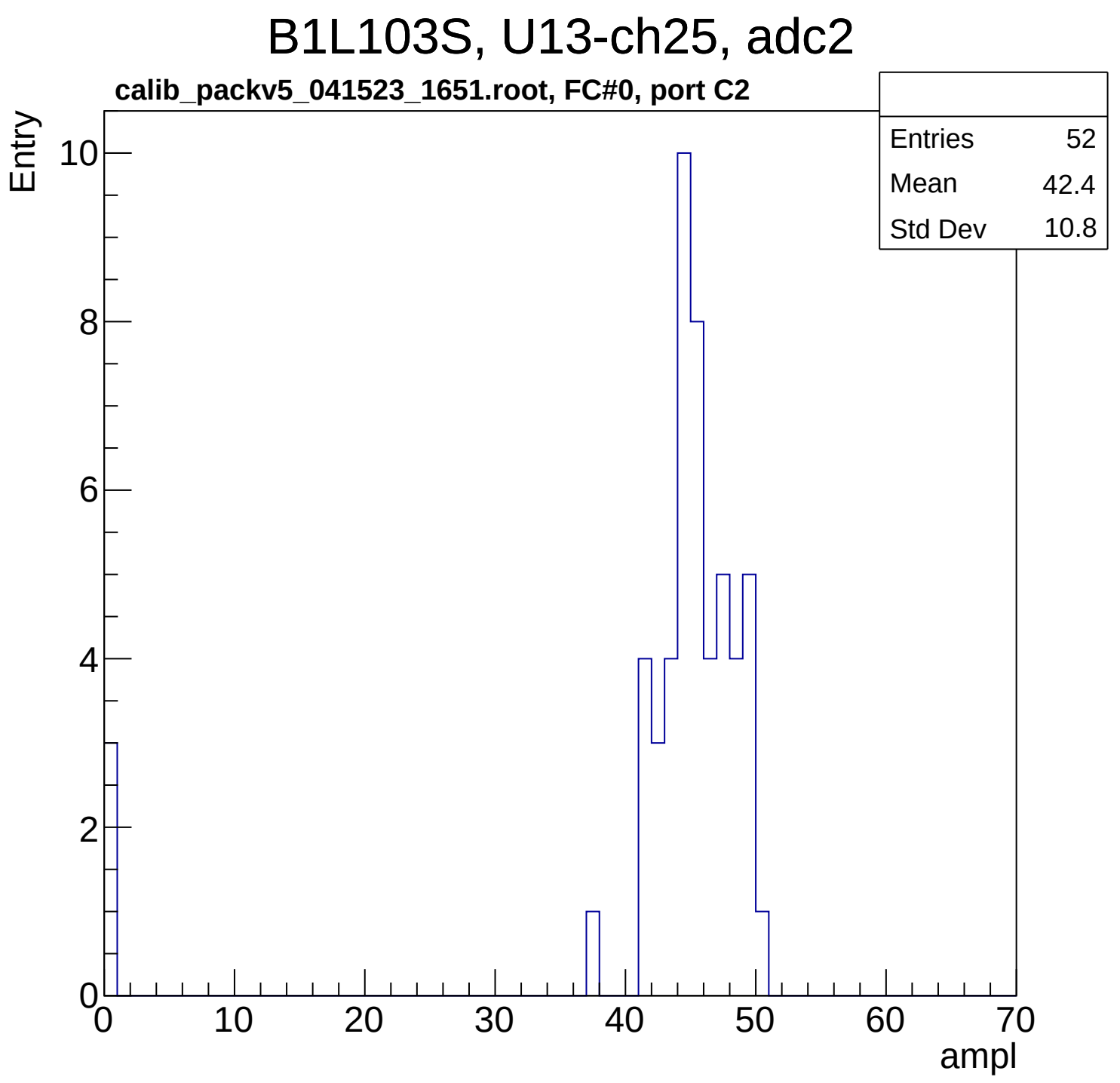
60
70

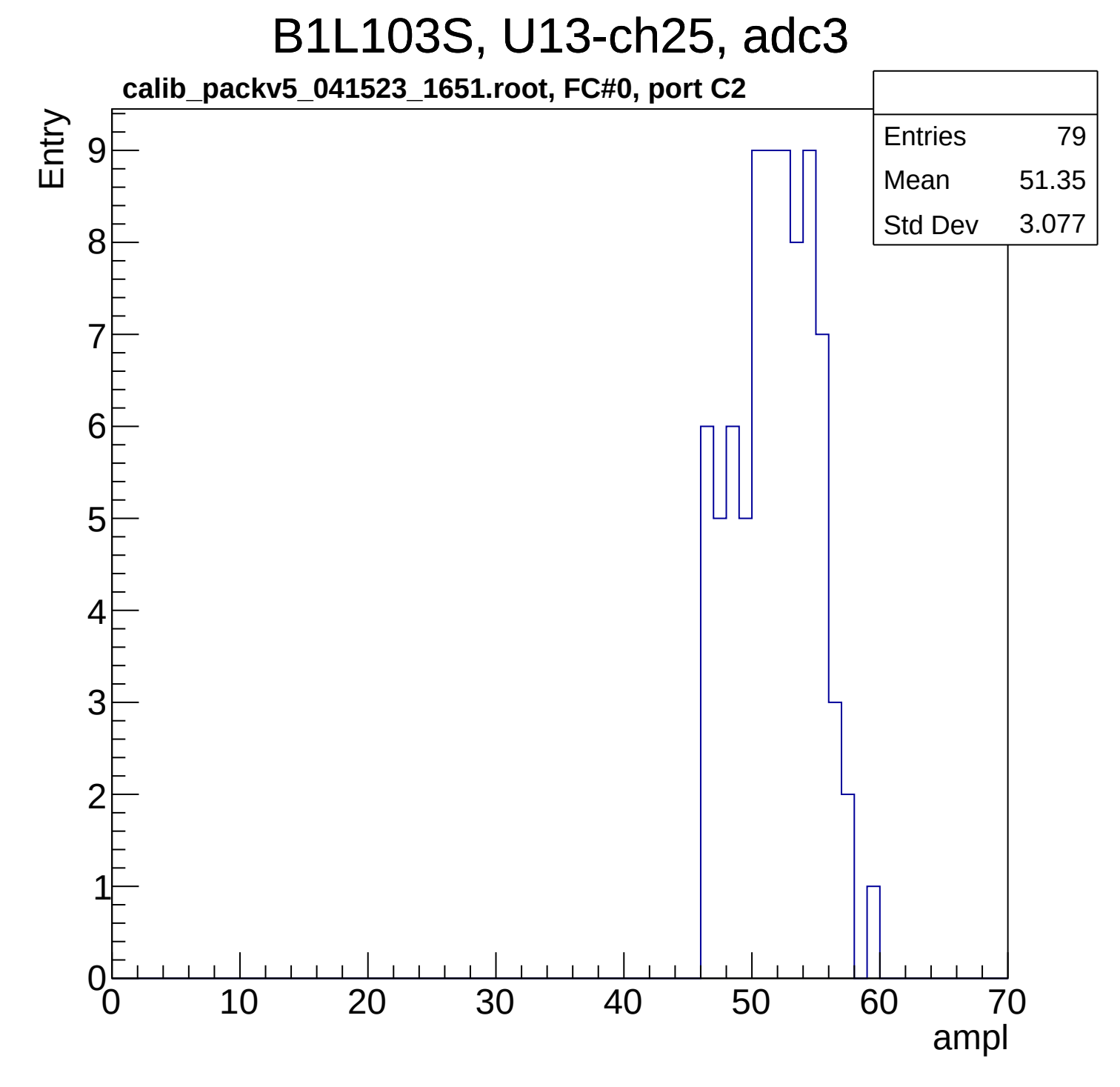

B1L103S, U13-ch24, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62
Std Dev 1.095
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U13-ch24, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.95
Std Dev 13.82
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch25, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 29.07
Std Dev 9.349
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch25, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 36.25
Std Dev 9.874
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch25, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 42.4
Std Dev 10.8
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch25, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 51.35
Std Dev 3.077
Entry
ampl
0
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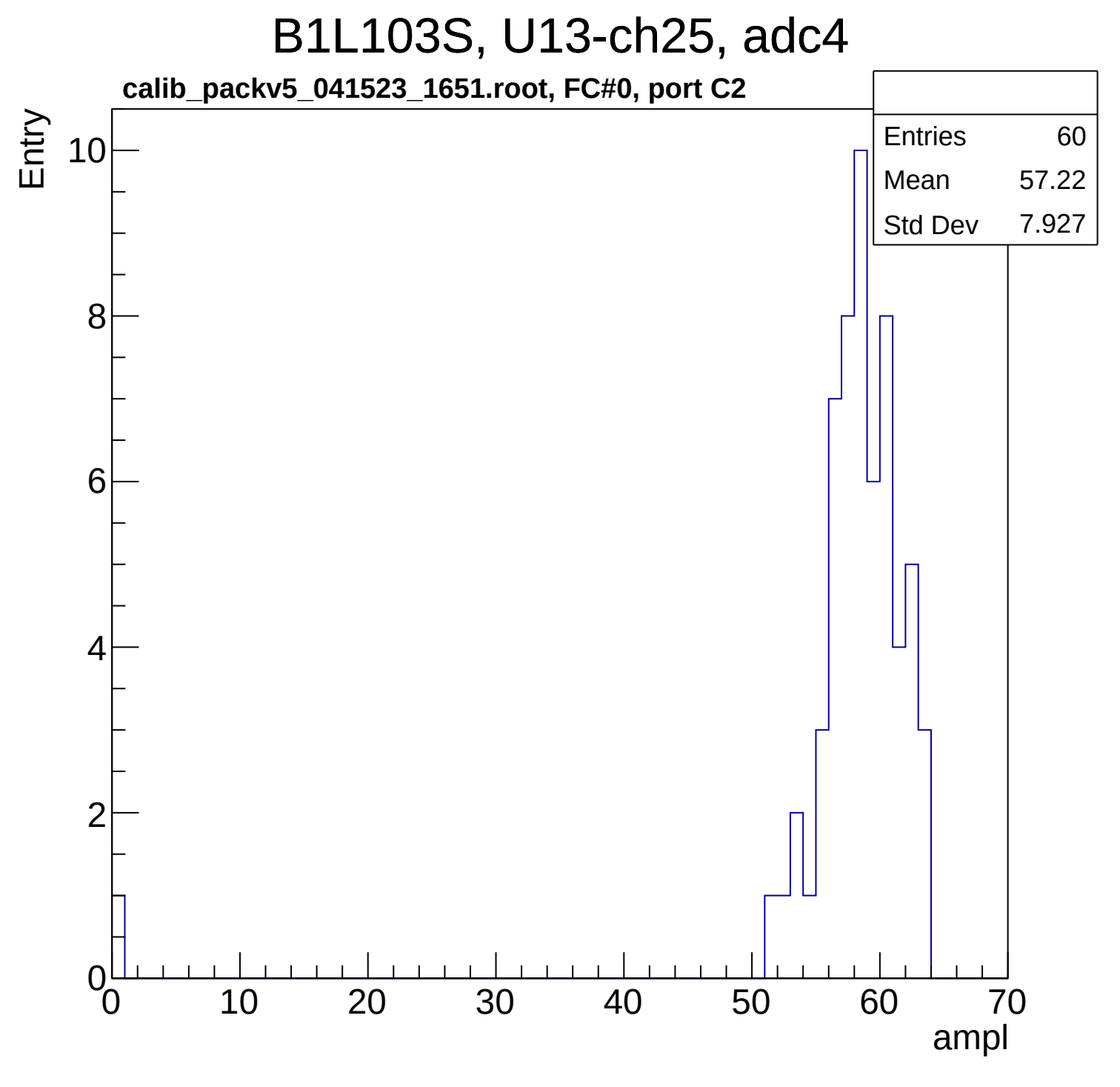
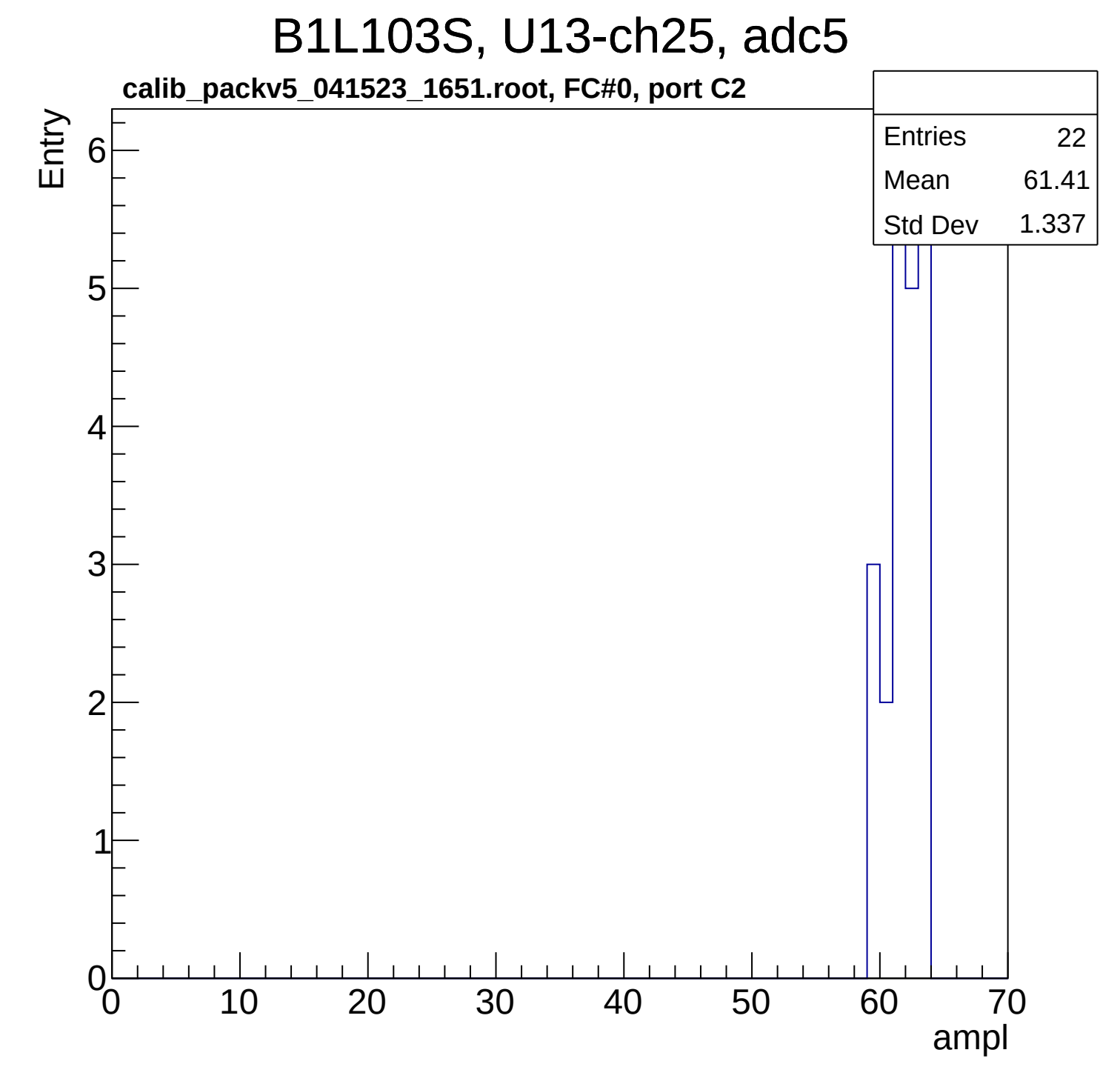
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch25, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 57.22
Std Dev 7.927
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch25, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 61.41
Std Dev 1.337
Entry
ampl
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3
4
5
6
0
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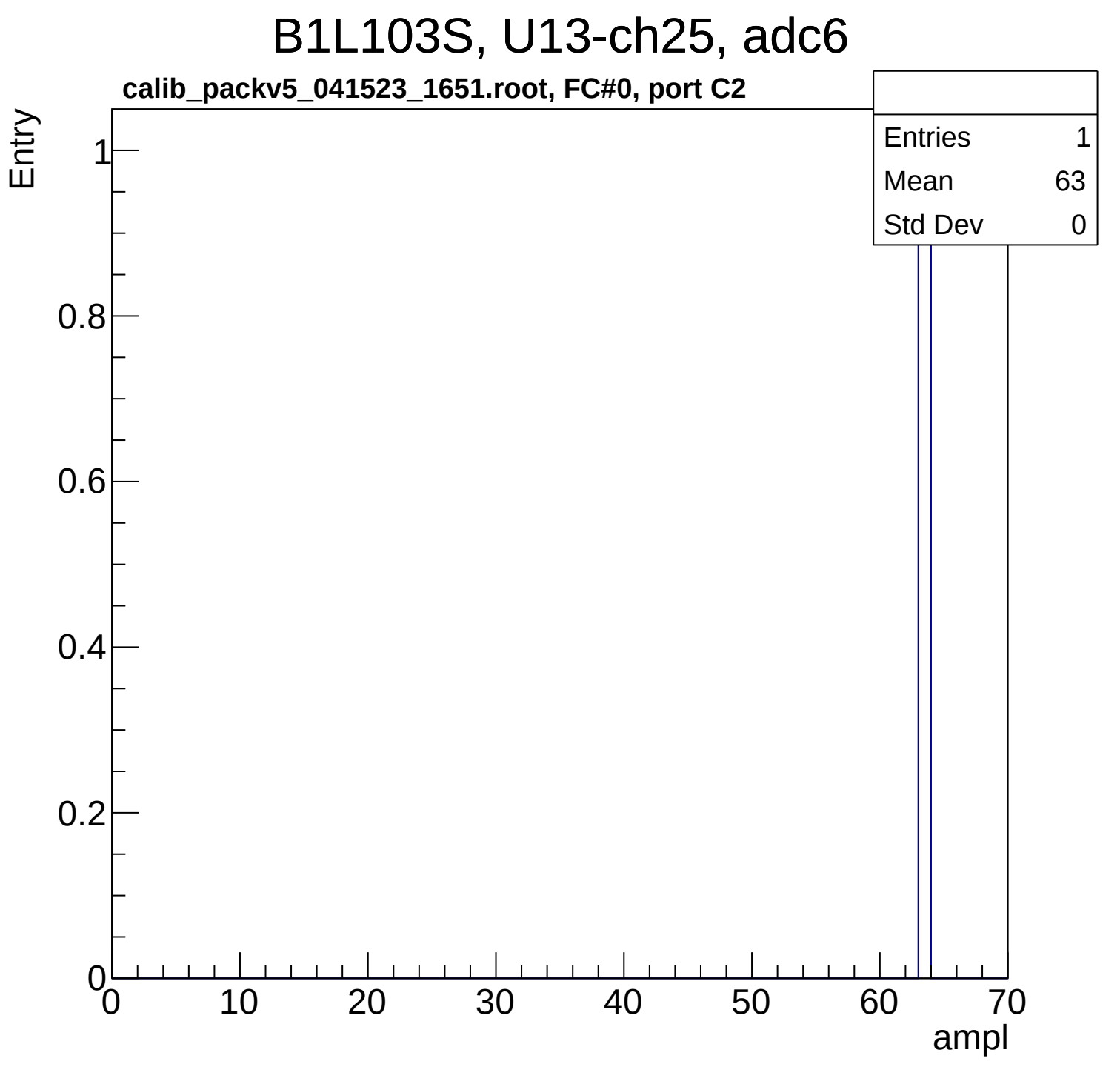
20
30
40
50
60
70


B1L103S, U13-ch25, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 63
Std Dev 0
Entry
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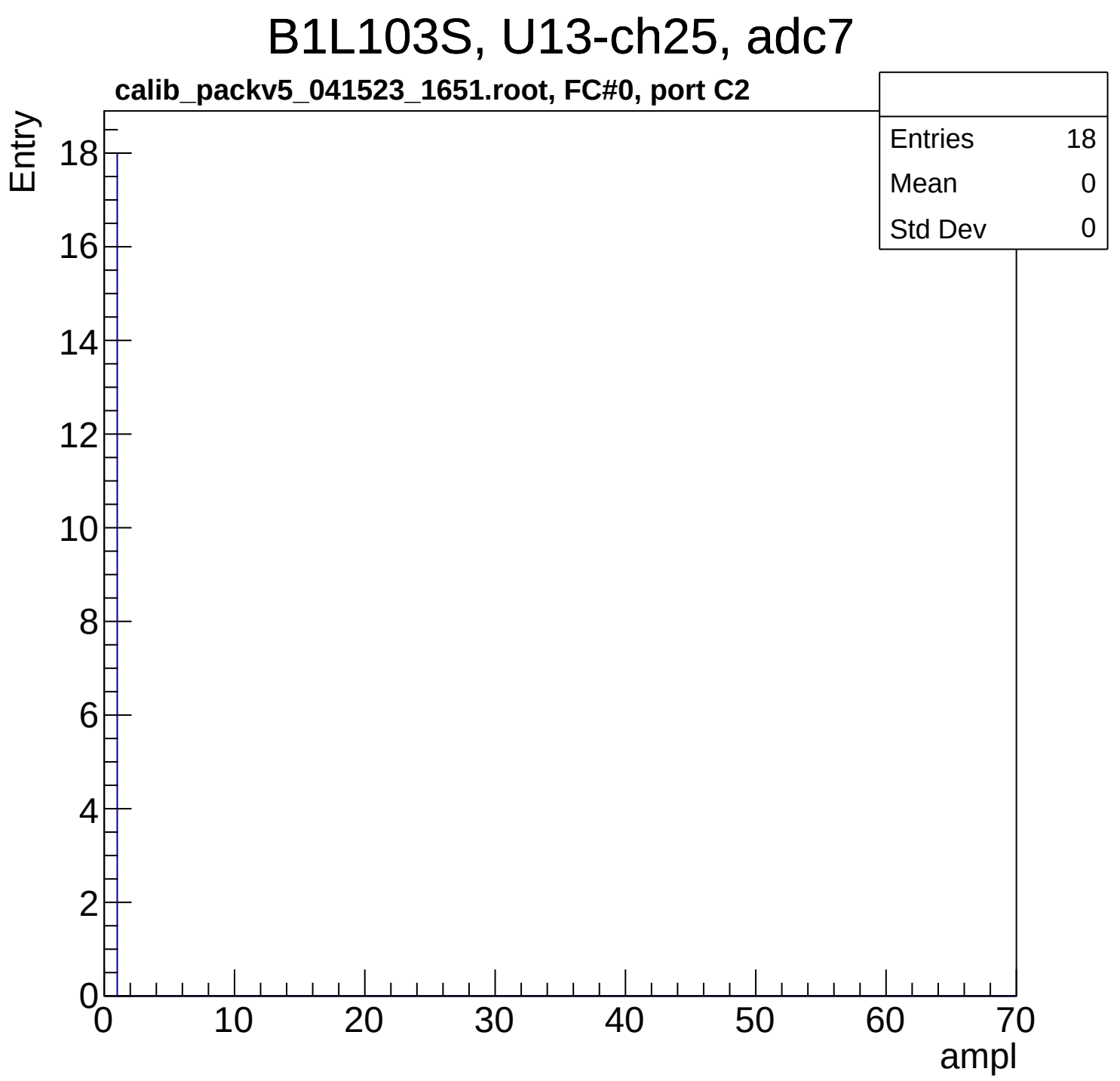
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch25, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
0
10
20
30
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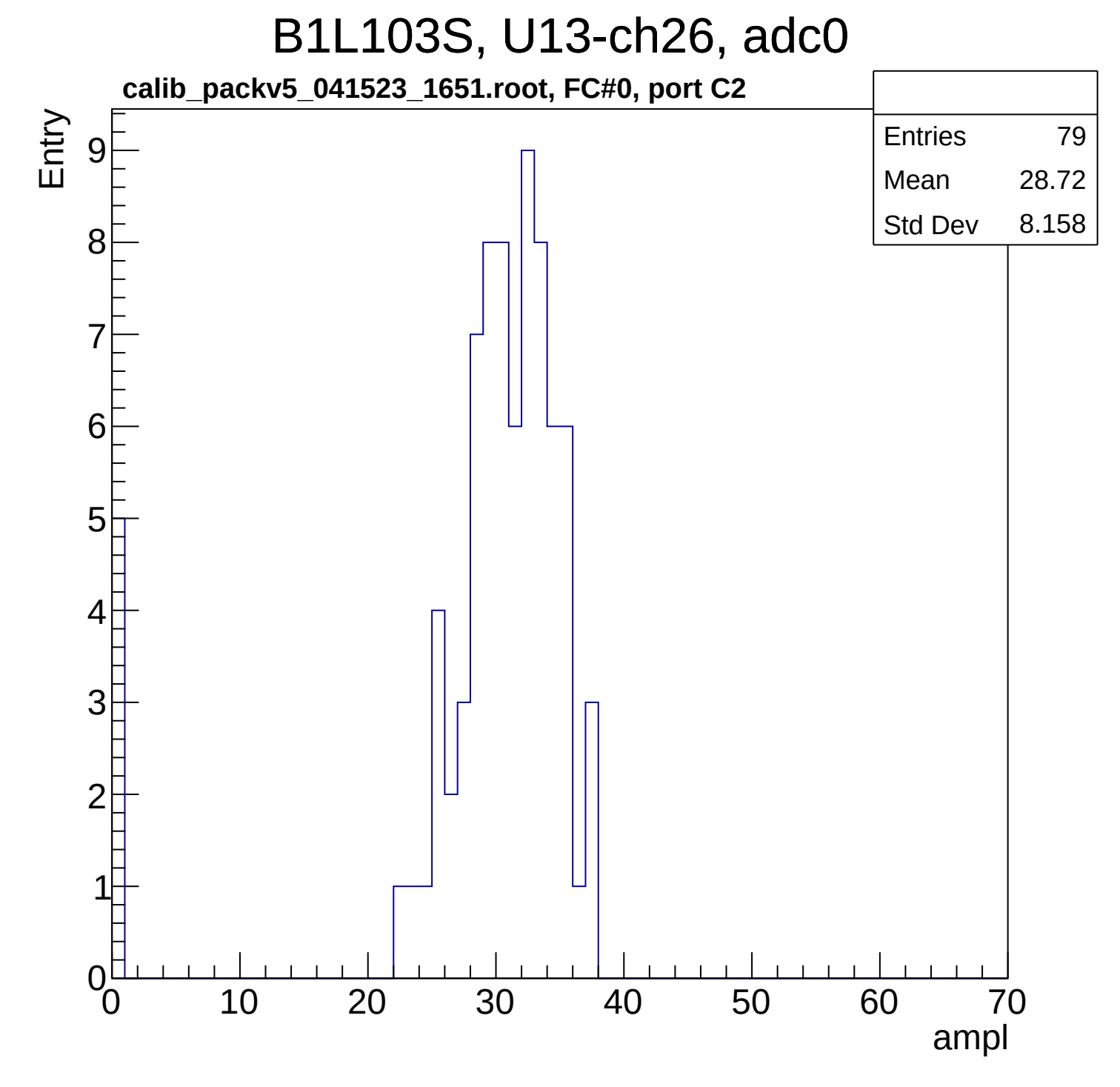
50
60
70
ampl


B1L103S, U13-ch26, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 28.72
Std Dev 8.158
Entry
ampl
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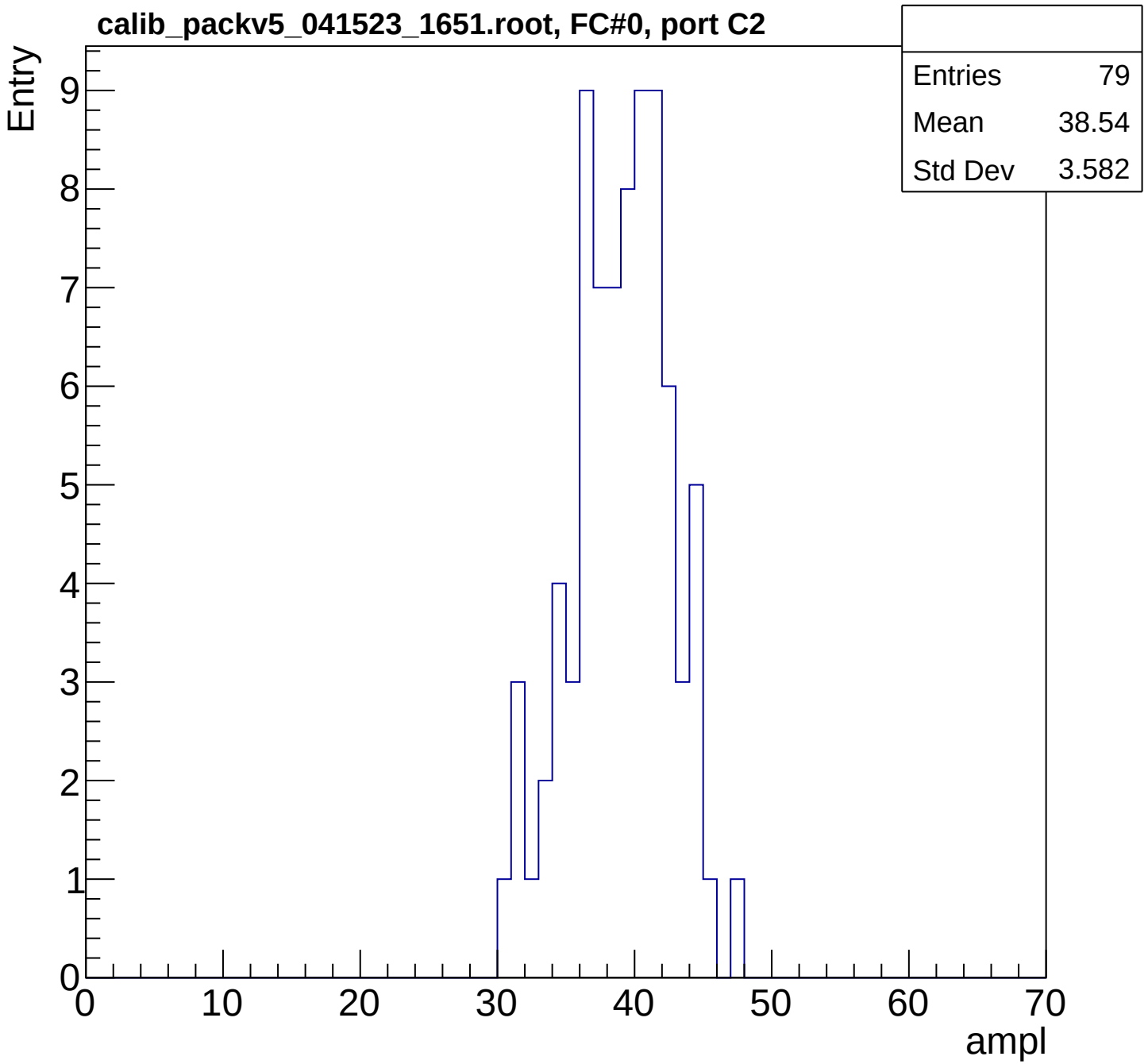
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch26, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 38.54
Std Dev 3.582
Entry
ampl
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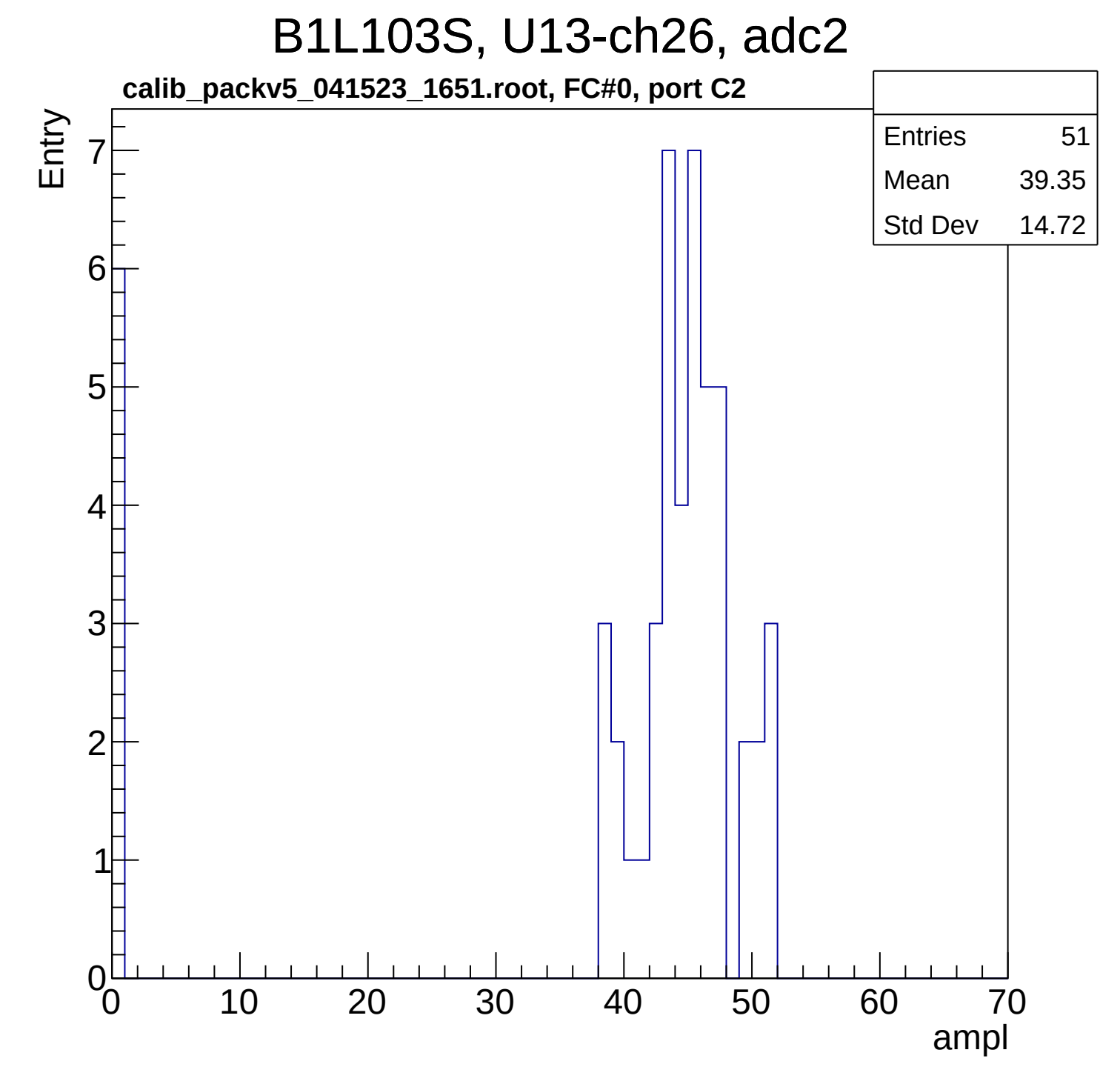
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch26, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 39.35
Std Dev 14.72
Entry
ampl
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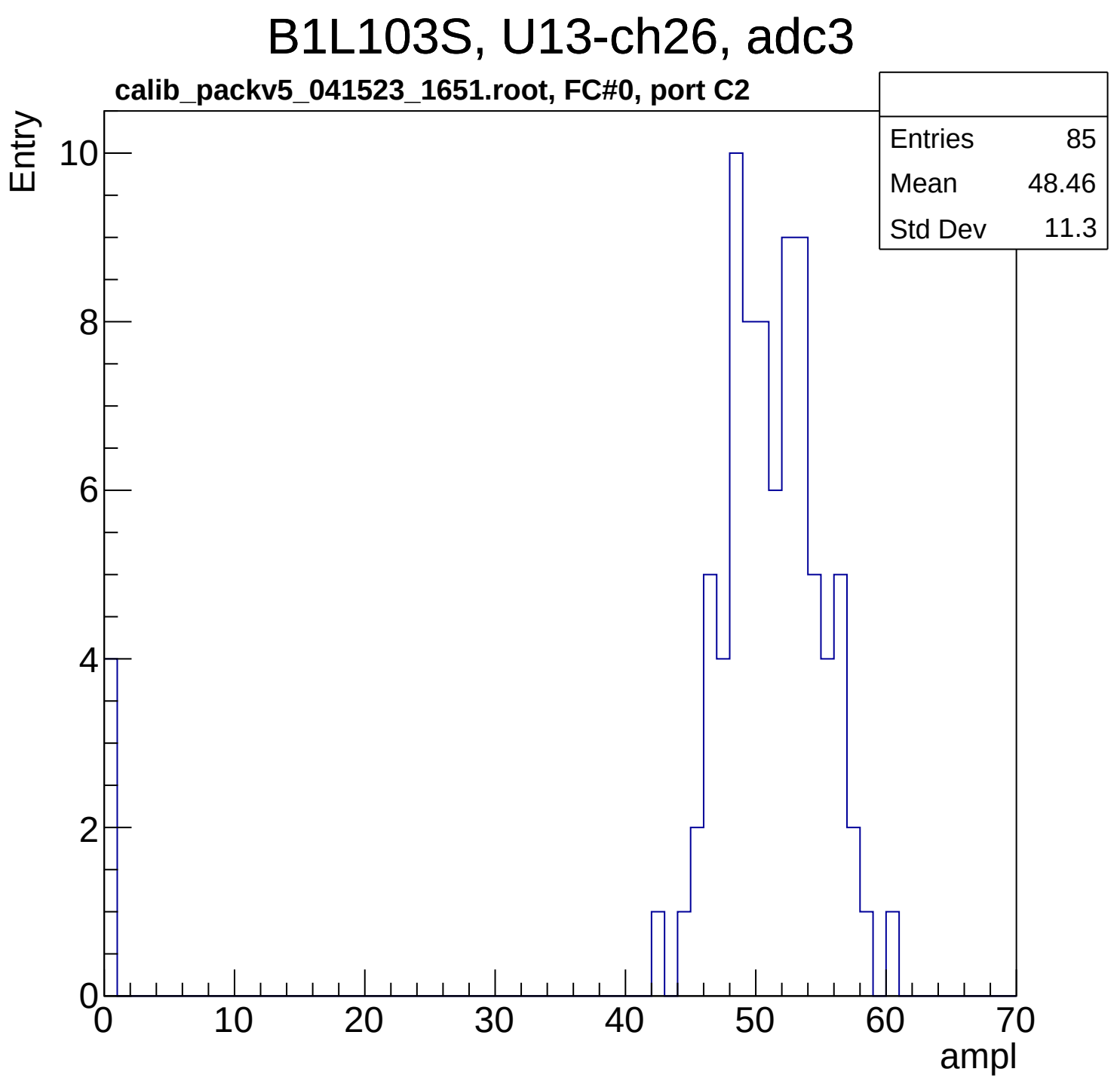
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch26, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 48.46
Std Dev 11.3
Entry
ampl
0
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8
10
0
10
20
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40
50
60
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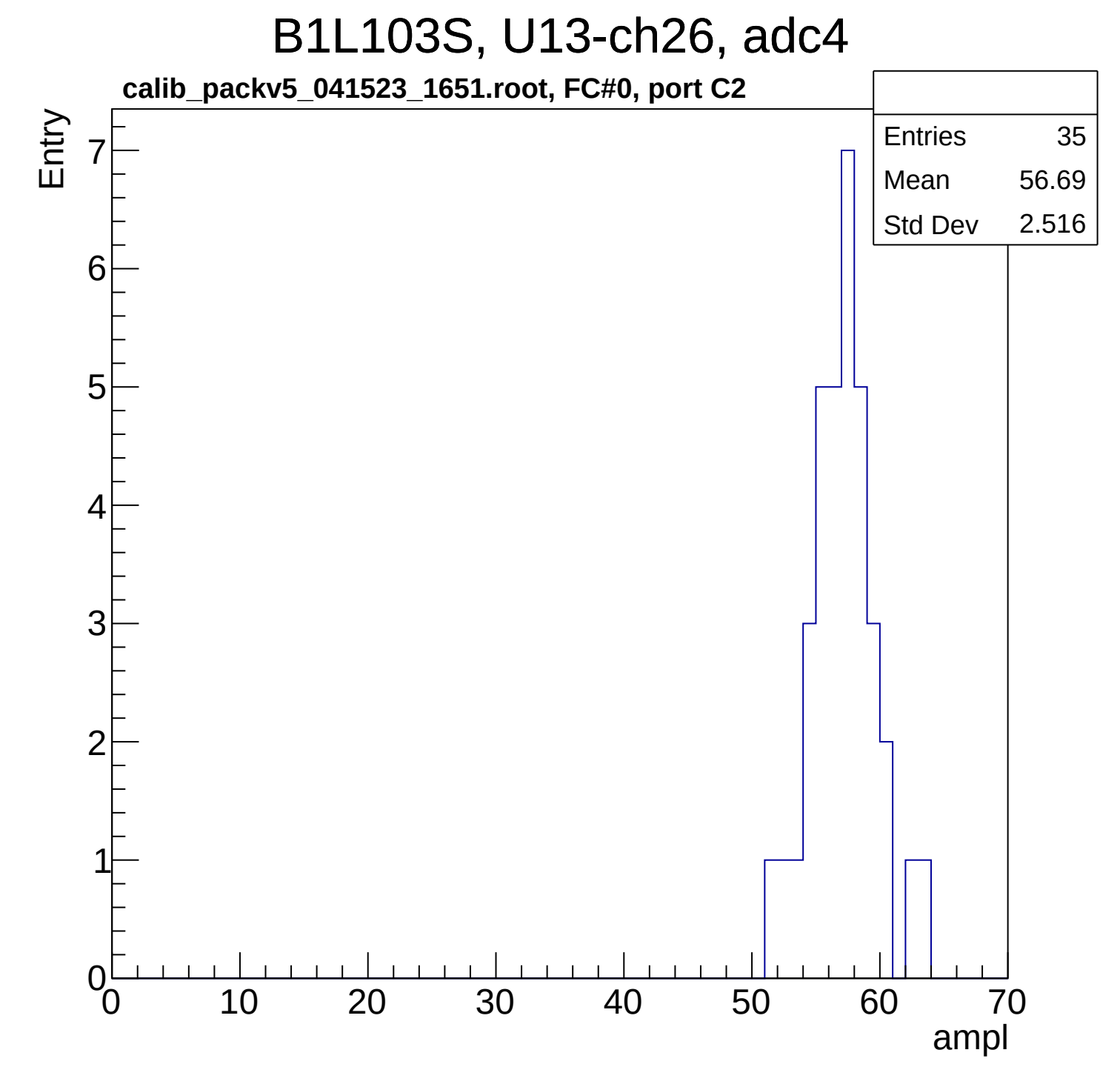
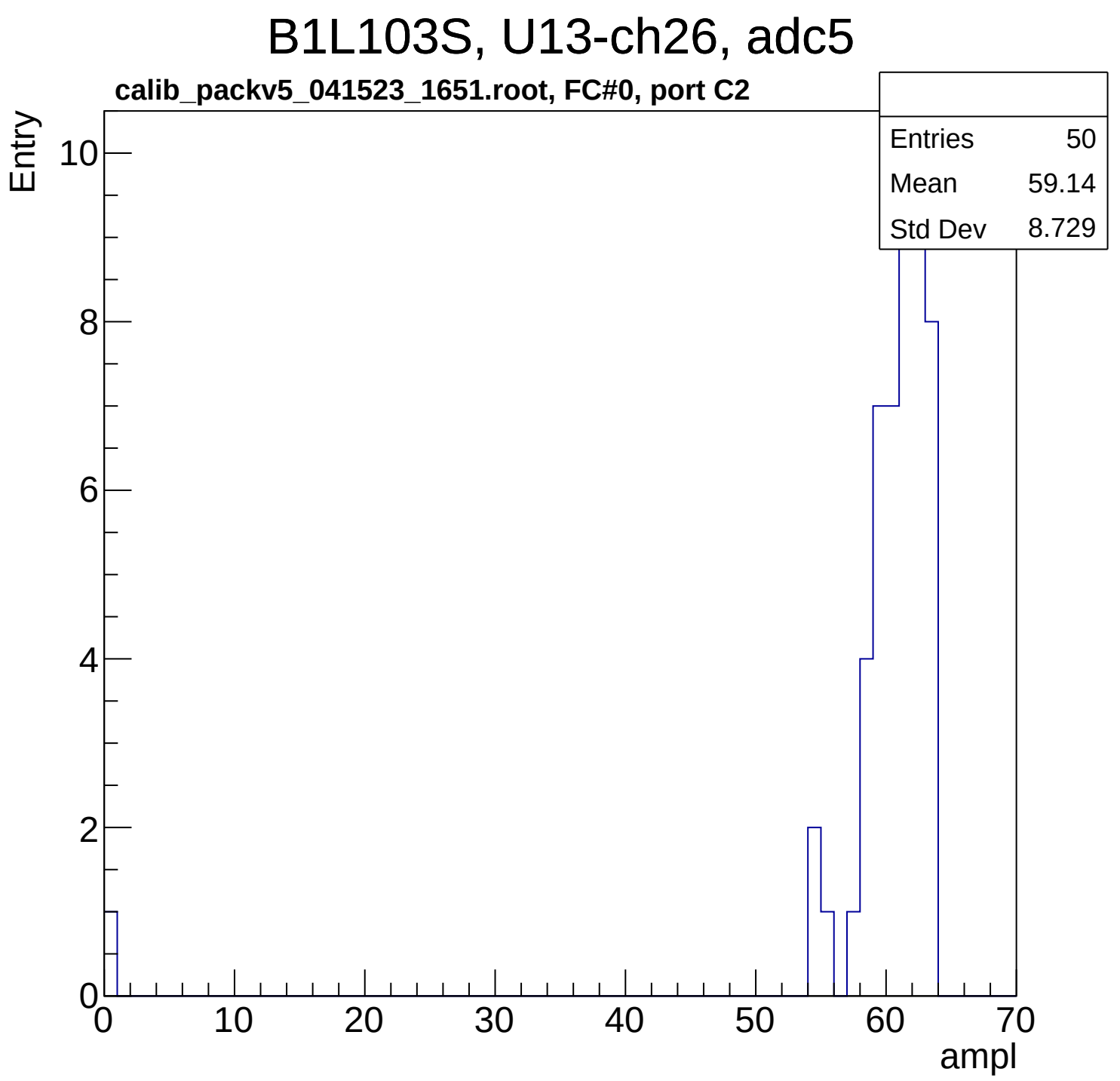
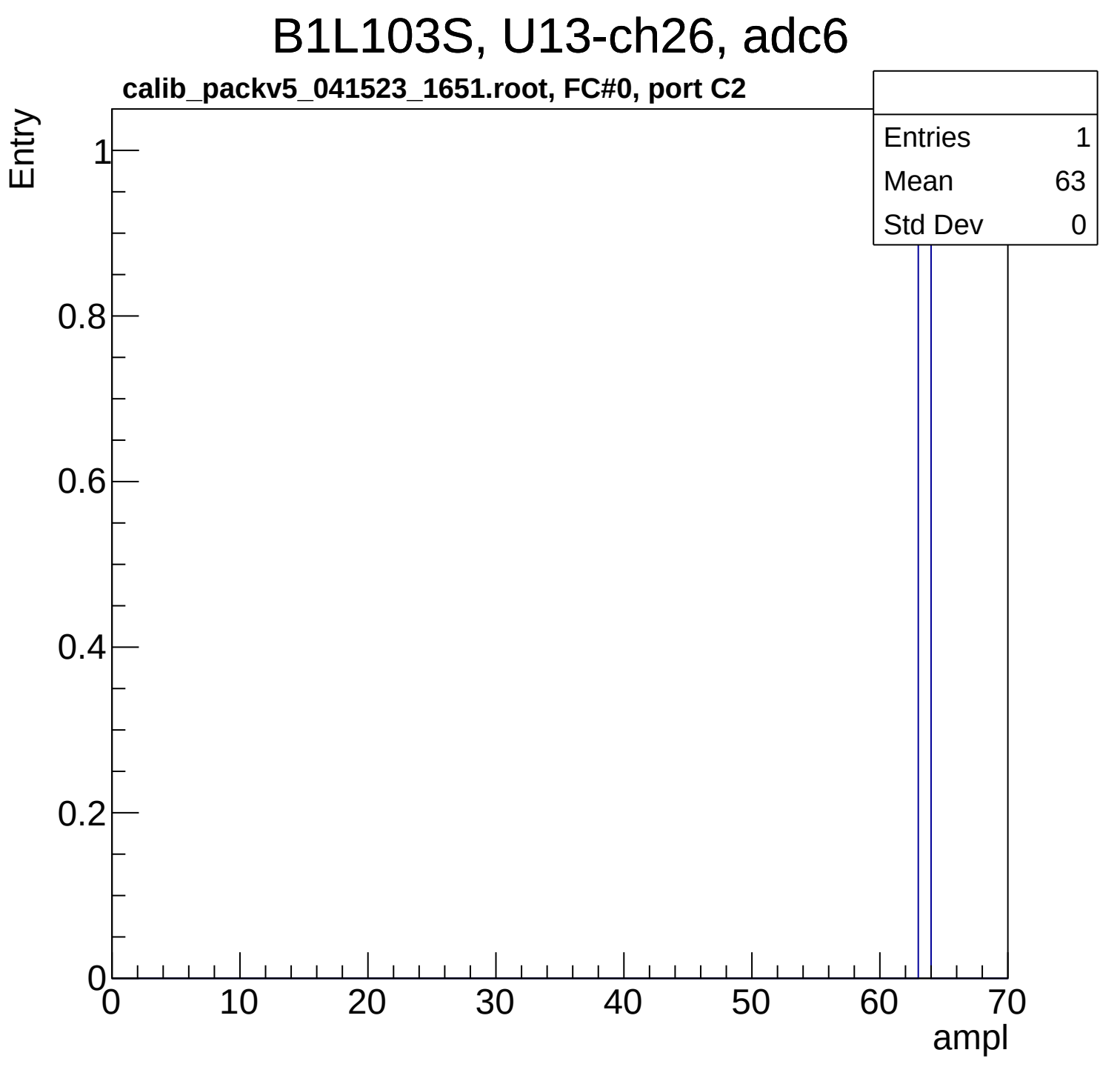

B1L103S, U13-ch26, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 56.69
Std Dev 2.516
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch26, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 59.14
Std Dev 8.729
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch26, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 63
Std Dev 0
Entry
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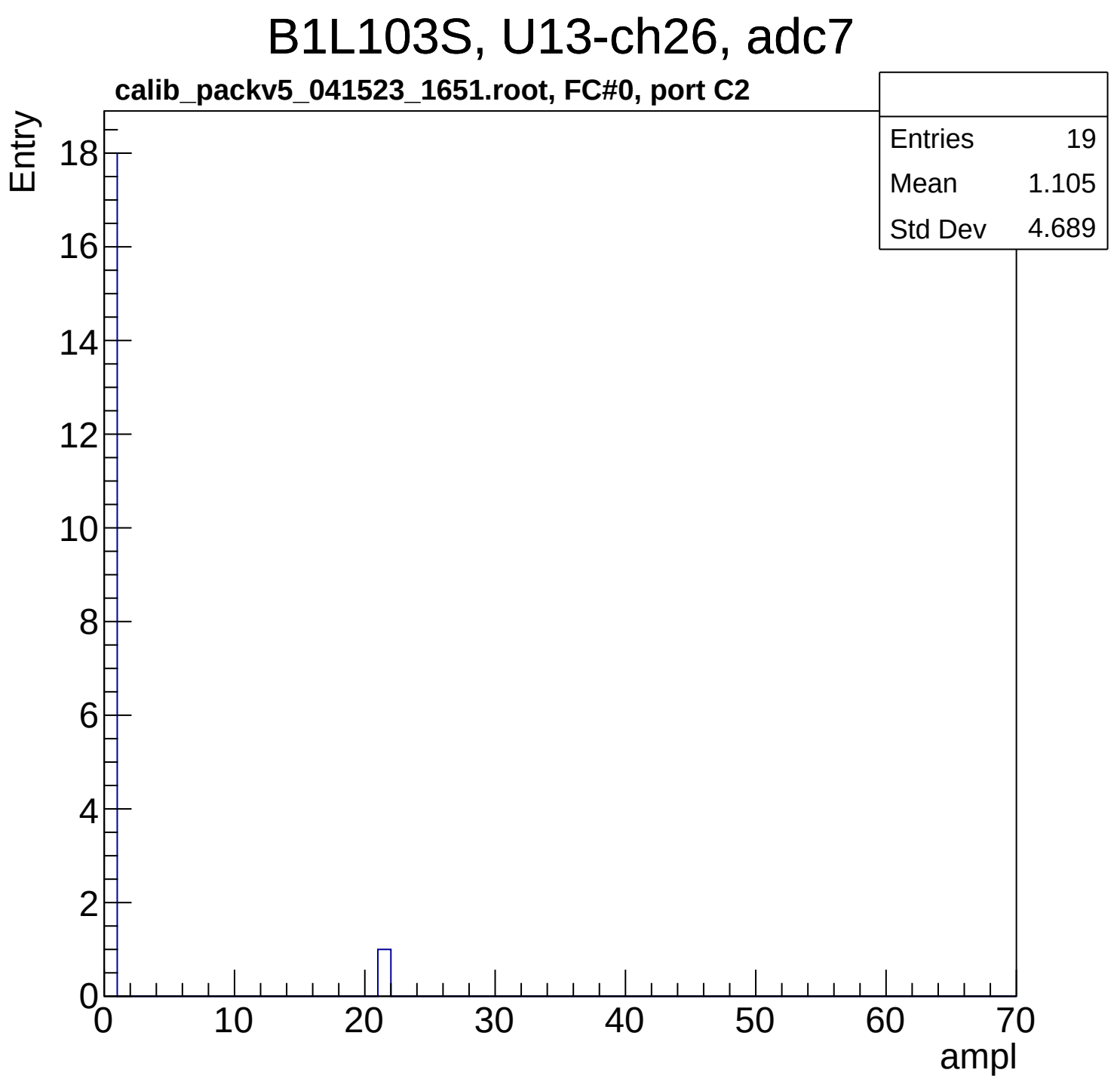
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch26, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
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6
8
10
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14
16
18
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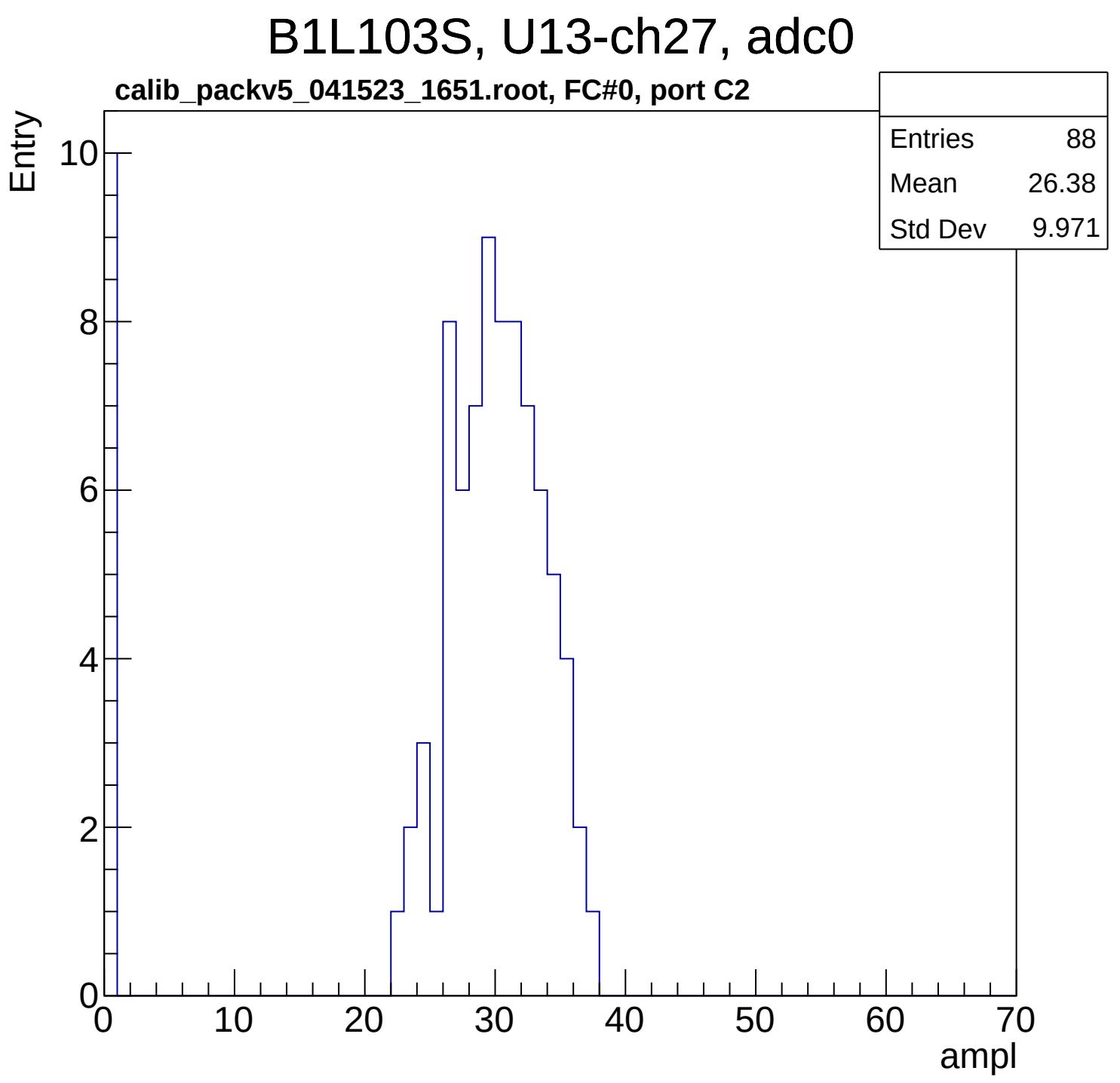
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch27, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 26.38
Std Dev 9.971
Entry
ampl
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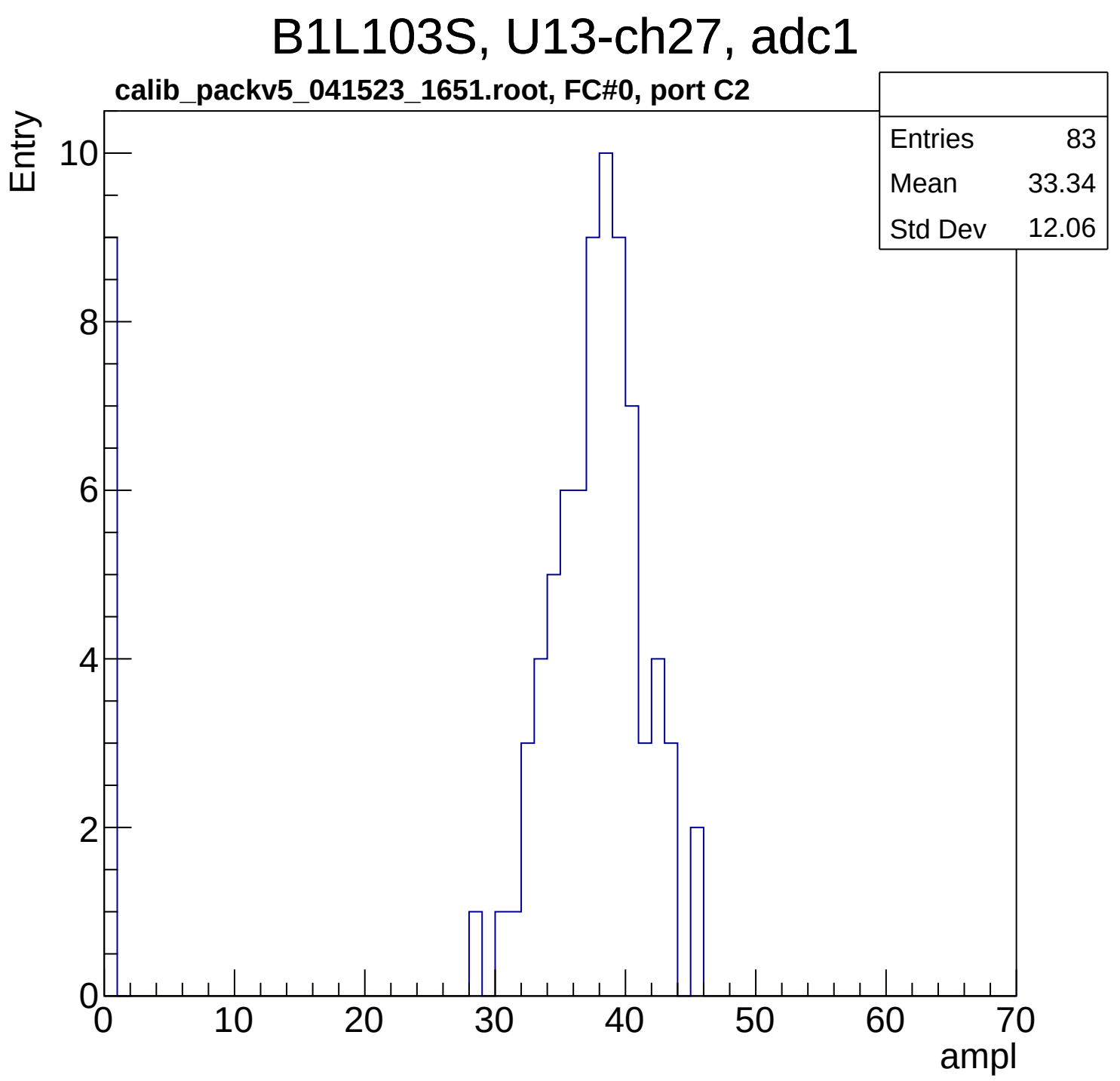
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch27, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 33.34
Std Dev 12.06
Entry
ampl
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4
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40
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60
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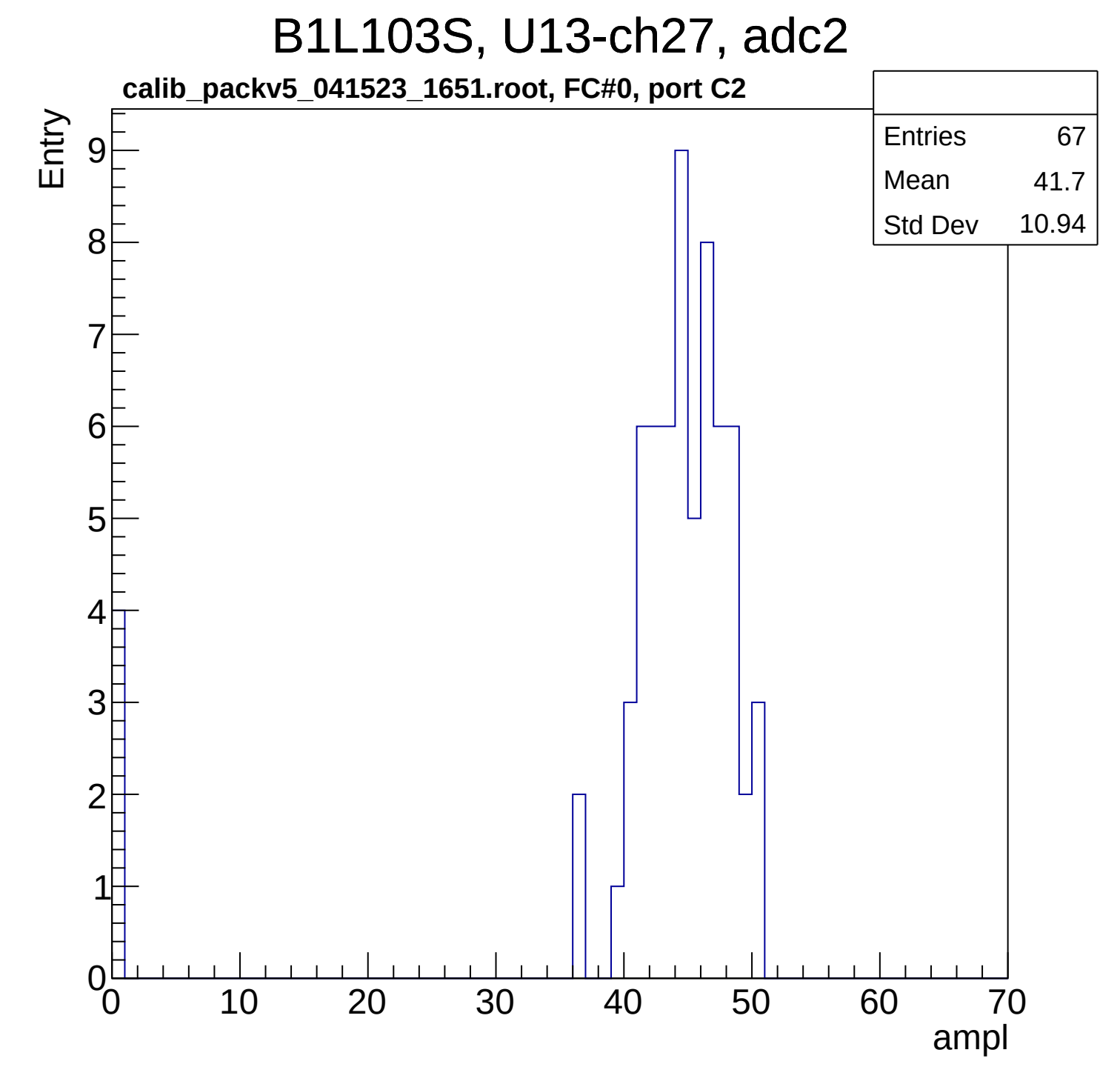
B1L103S, U13-ch27, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 41.7
Std Dev 10.94
Entry
ampl
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6
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10
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40
50
60
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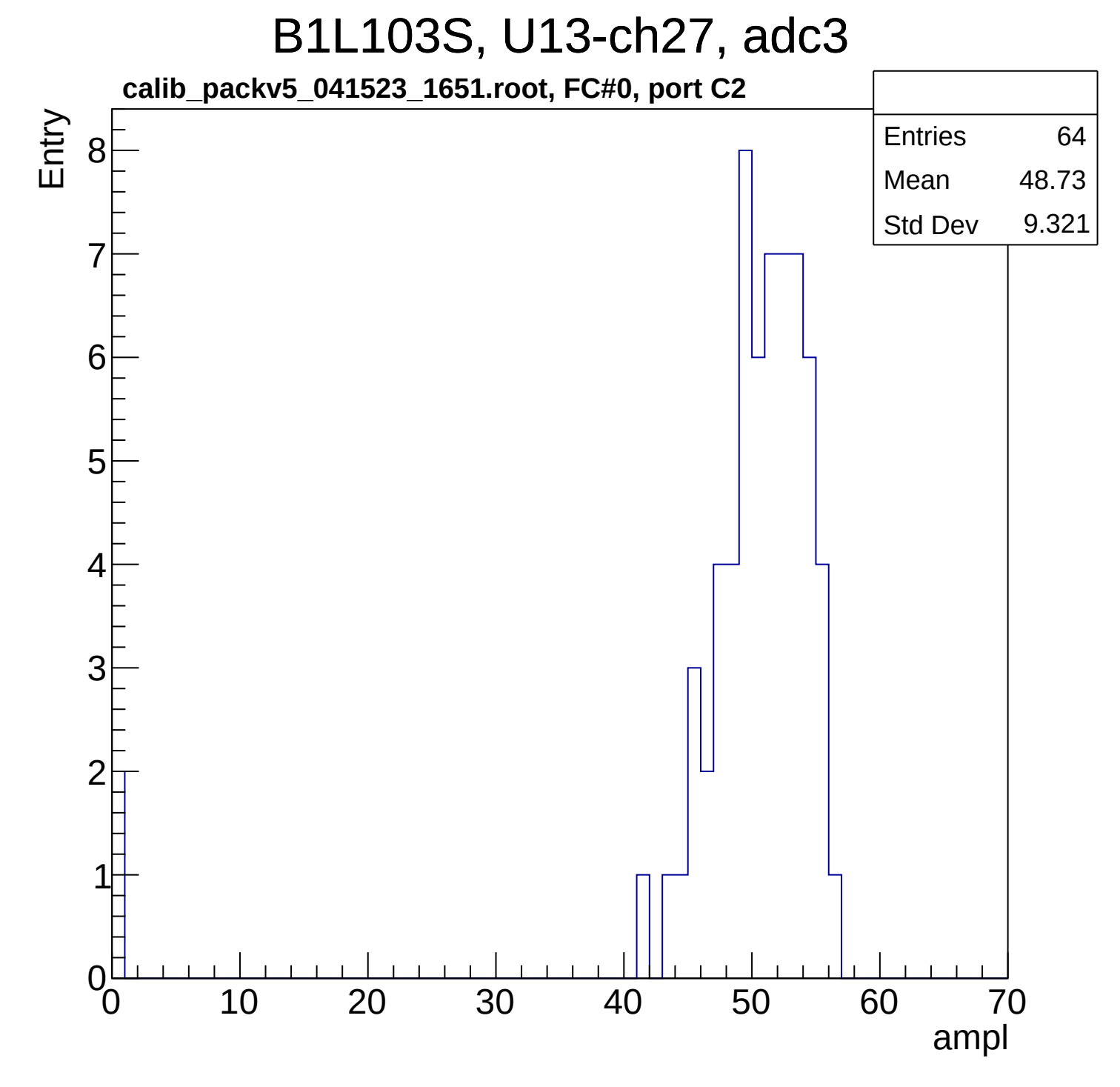
B1L103S, U13-ch27, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 48.73
Std Dev 9.321
Entry
ampl
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2
3
4
5
6
7
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0
10
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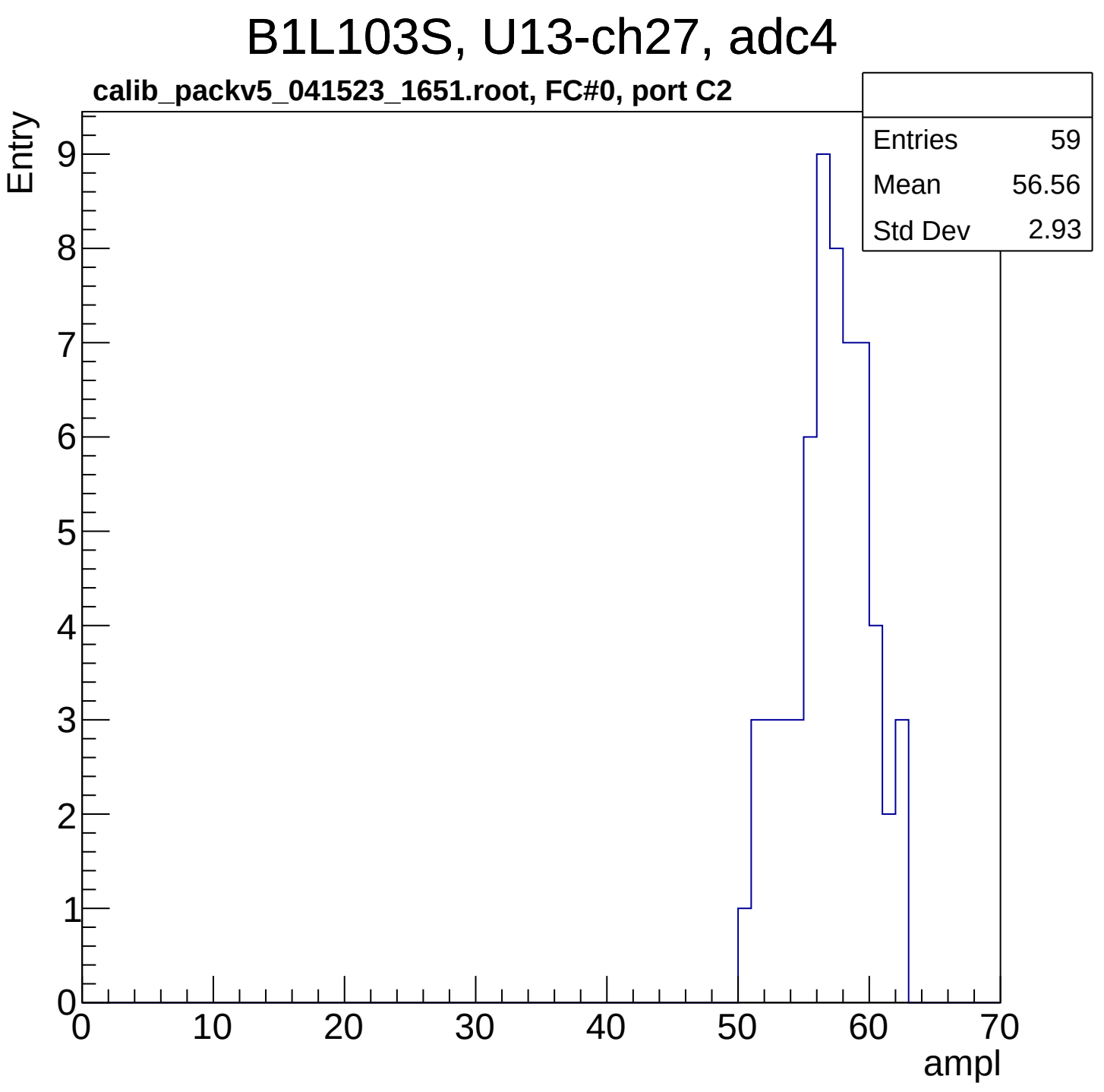
30
40
50
60
70


B1L103S, U13-ch27, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 56.56
Std Dev 2.93
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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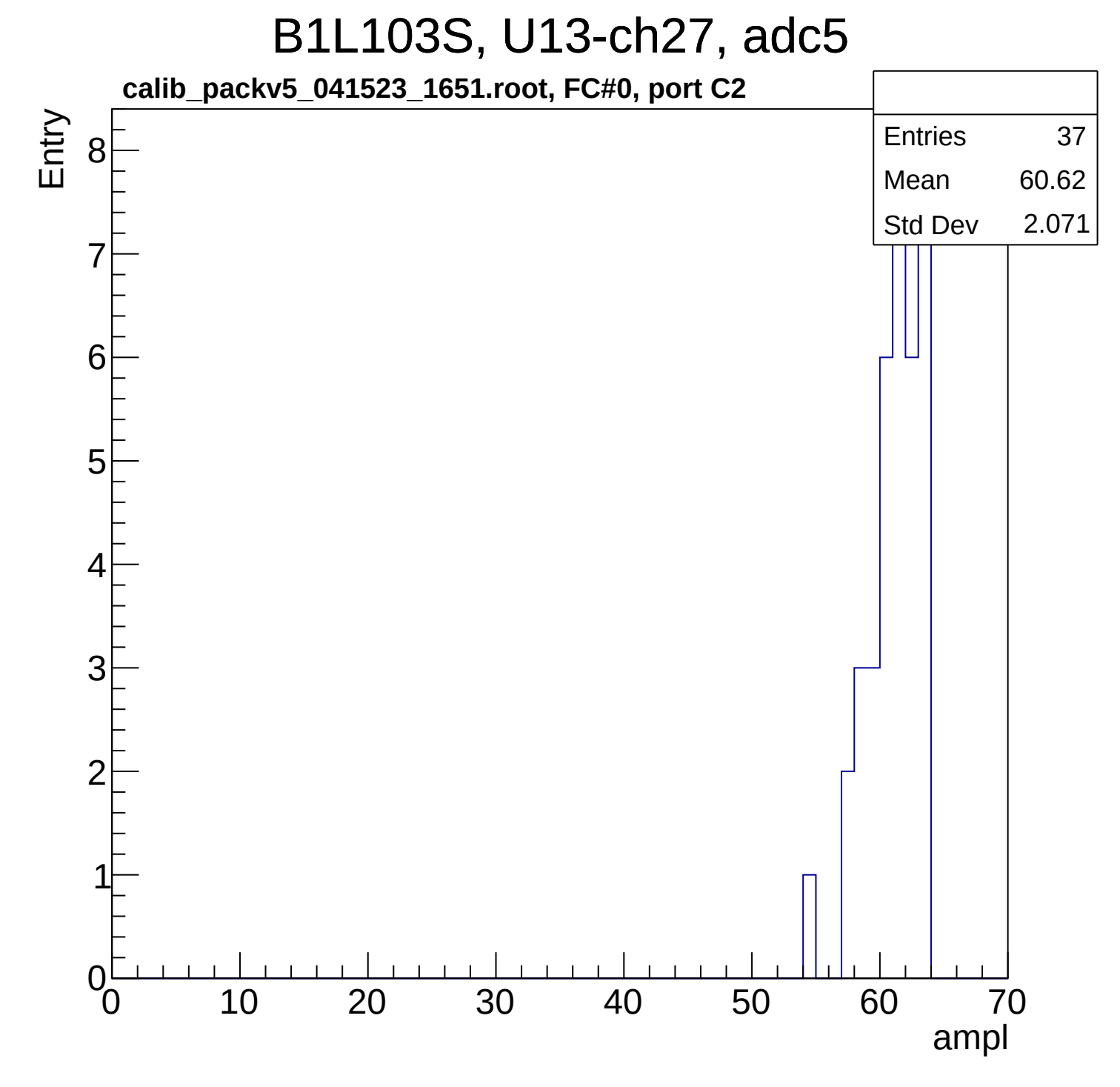
B1L103S, U13-ch27, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 60.62
Std Dev 2.071
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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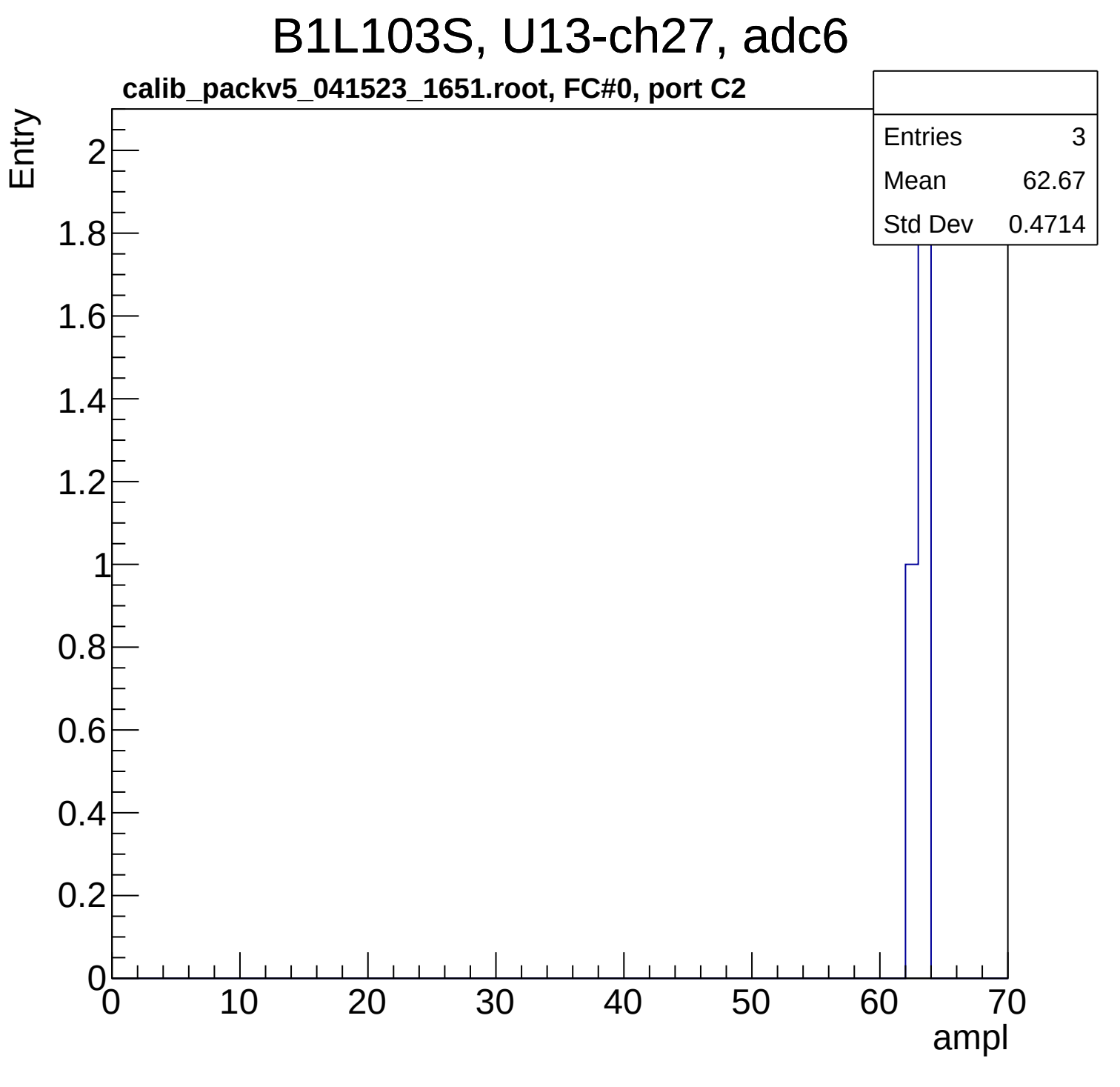
B1L103S, U13-ch27, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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40
50
60
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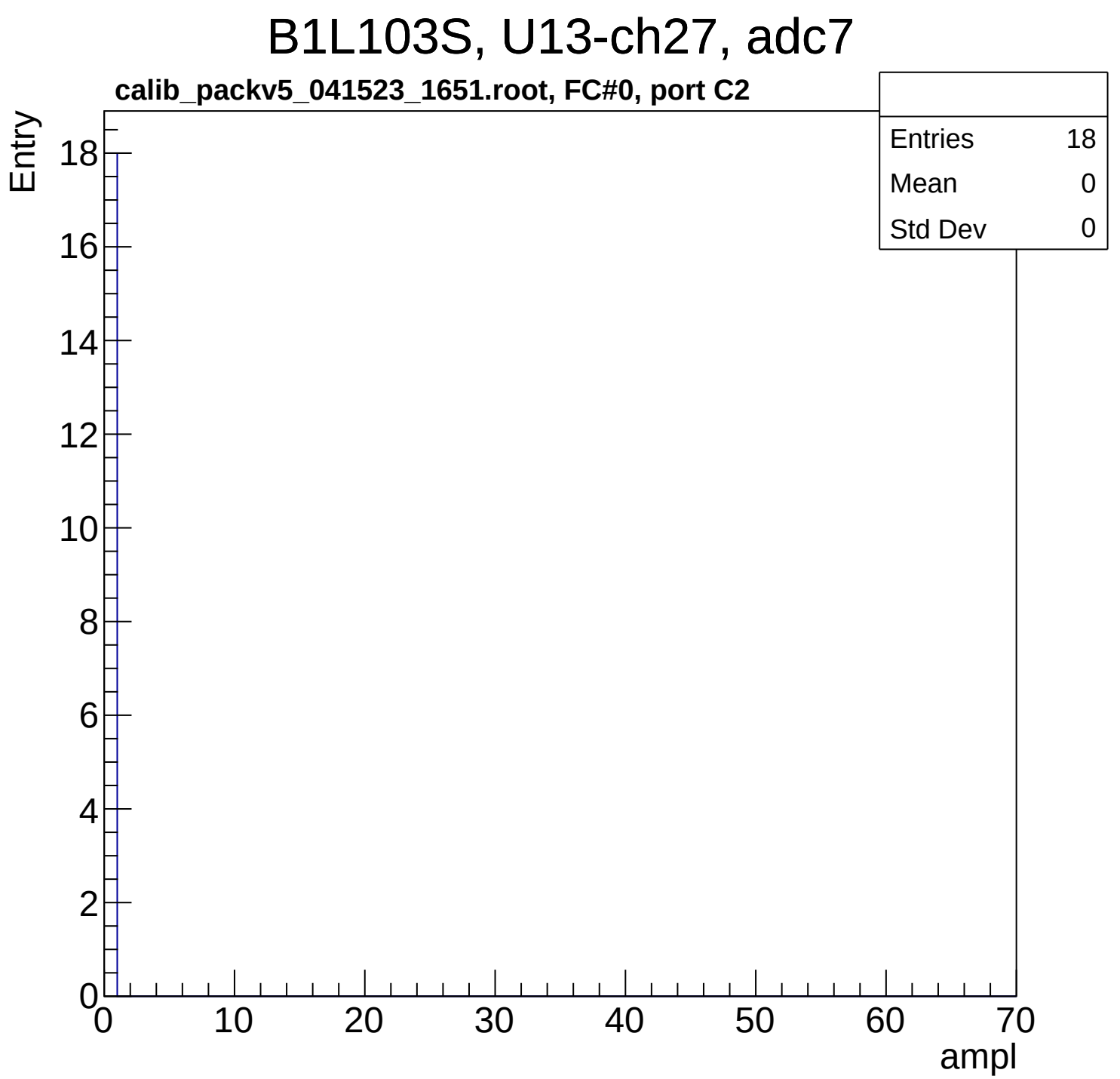
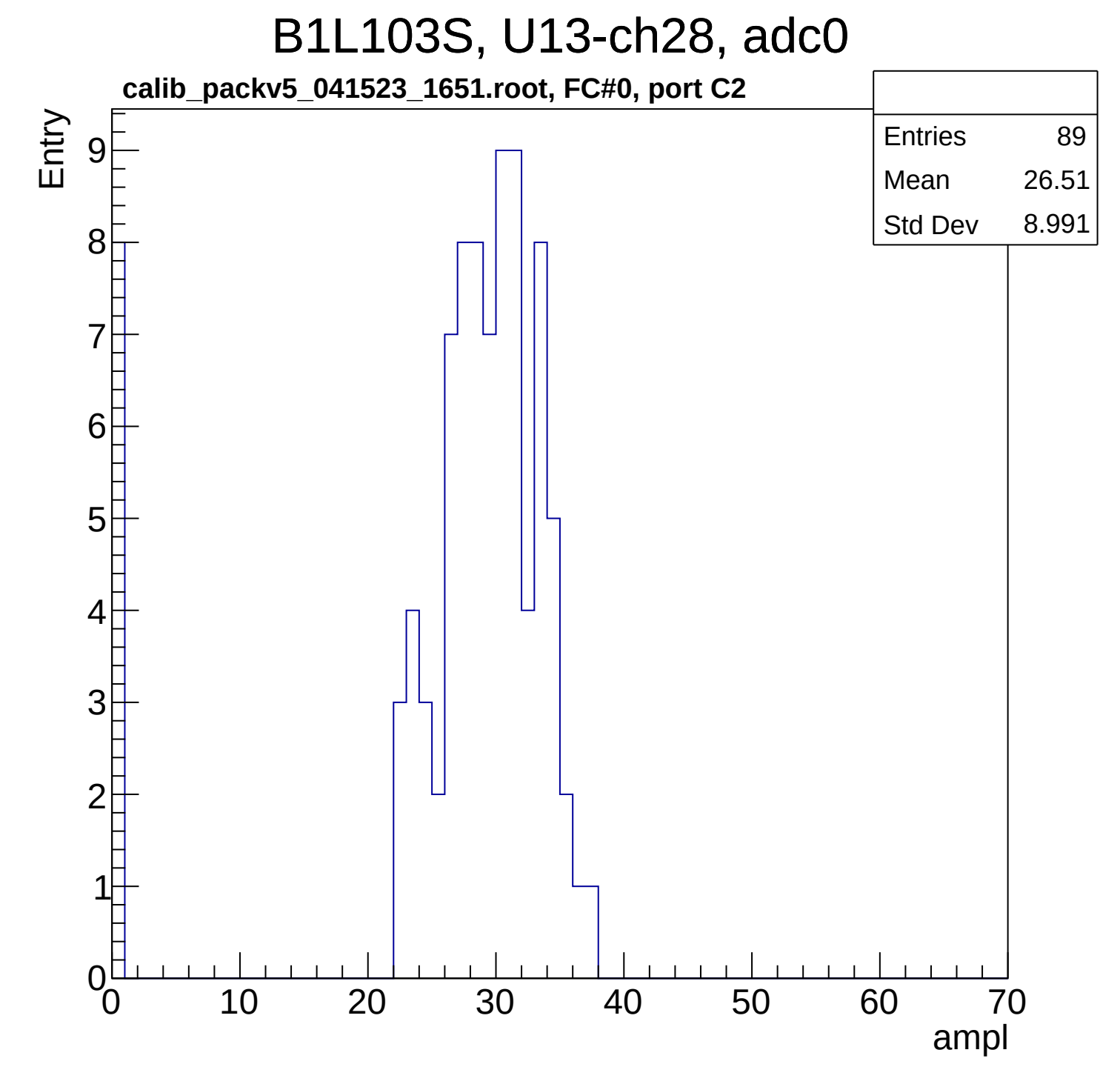

B1L103S, U13-ch27, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch28, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 26.51
Std Dev 8.991
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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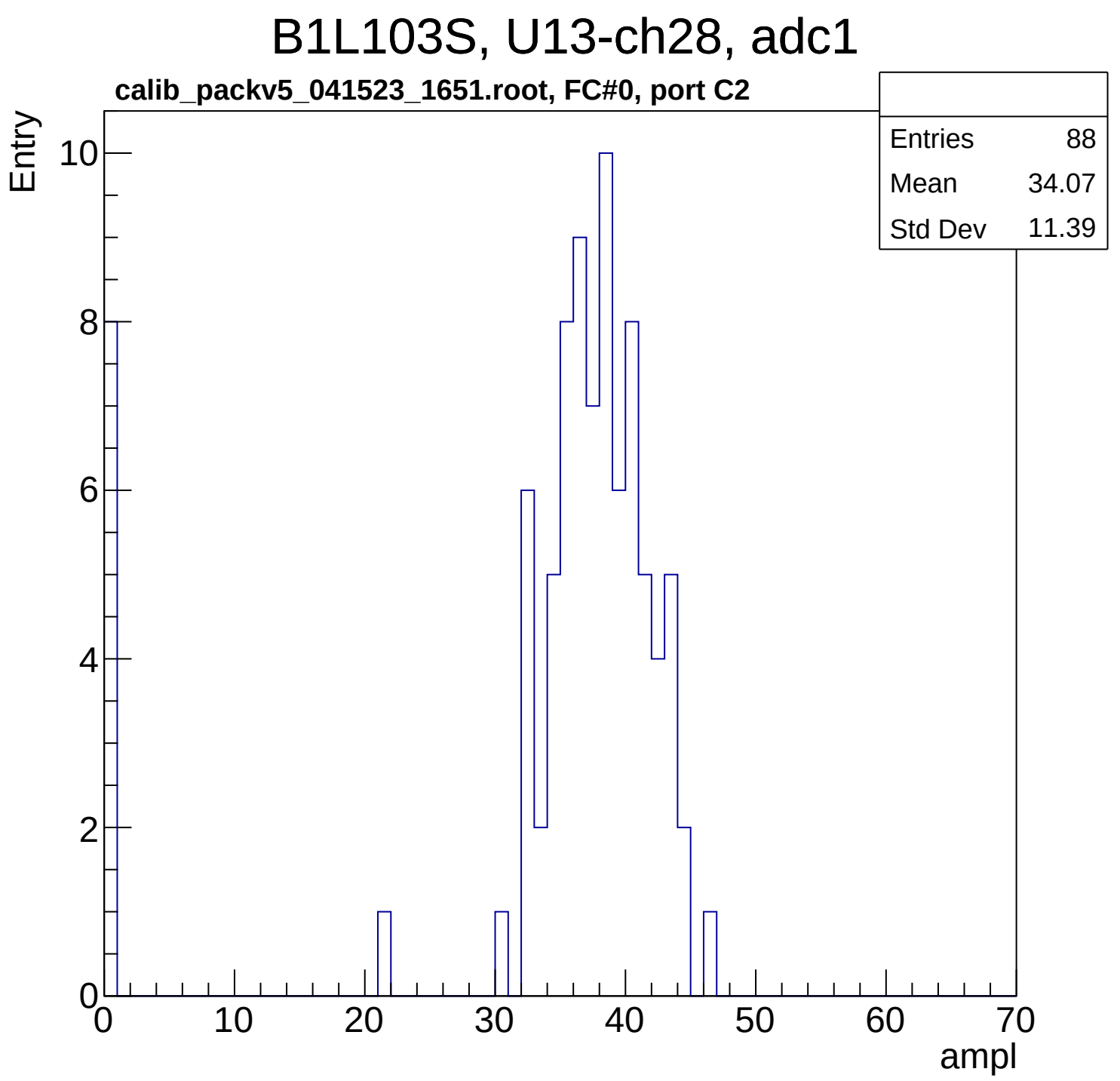
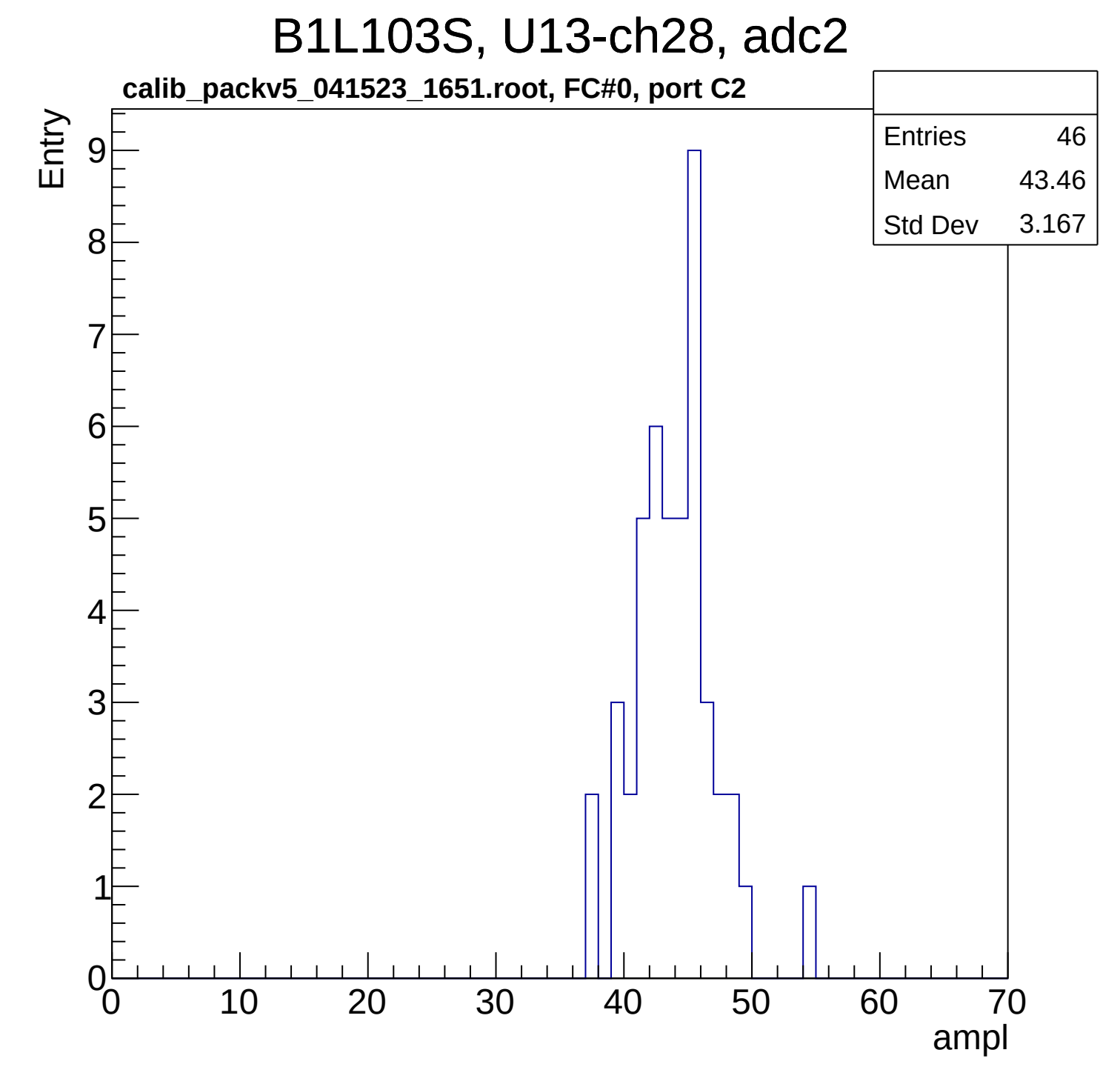

B1L103S, U13-ch28, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 34.07
Std Dev 11.39
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch28, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 43.46
Std Dev 3.167
Entry
ampl
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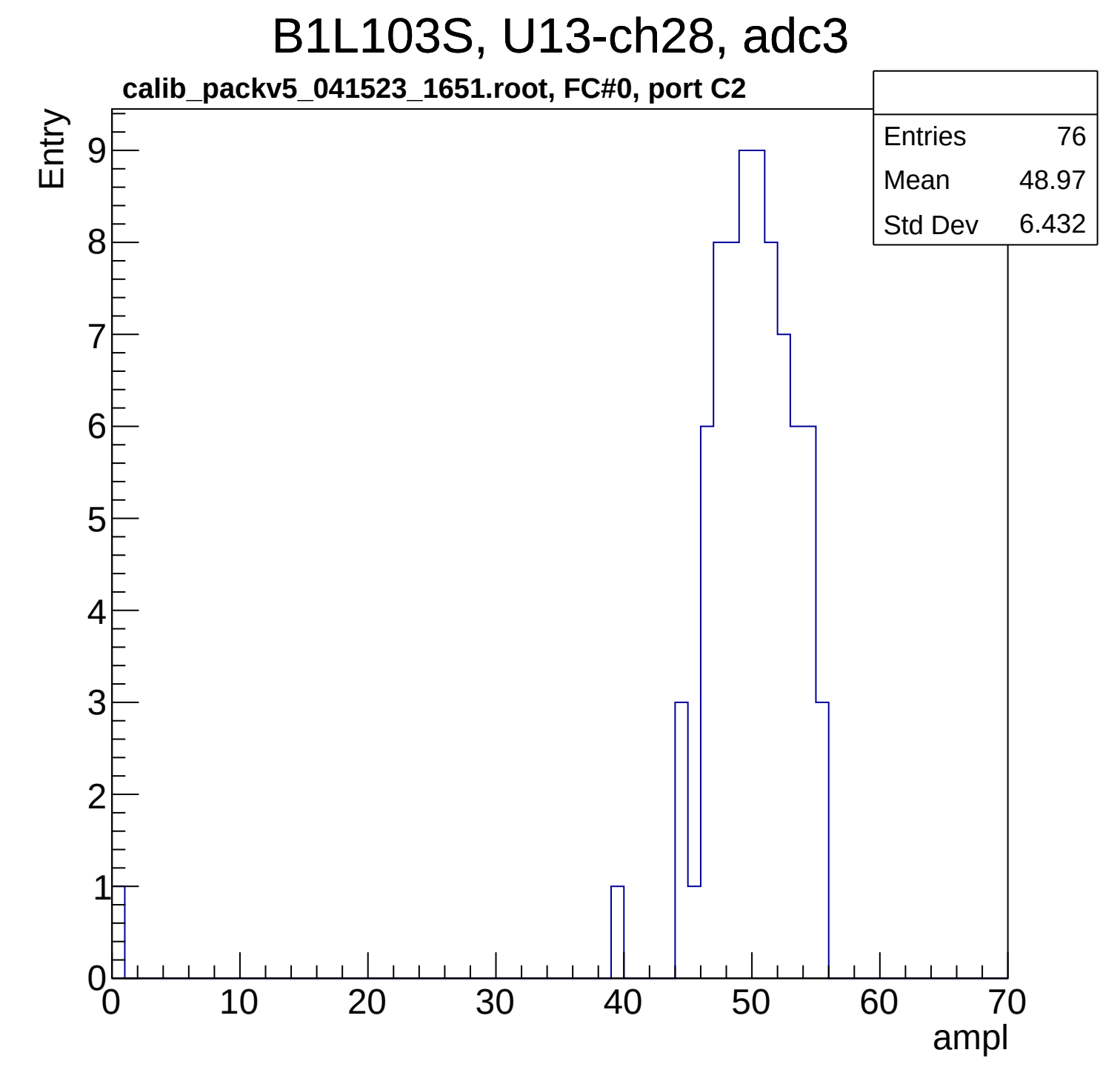
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch28, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 48.97
Std Dev 6.432
Entry
ampl
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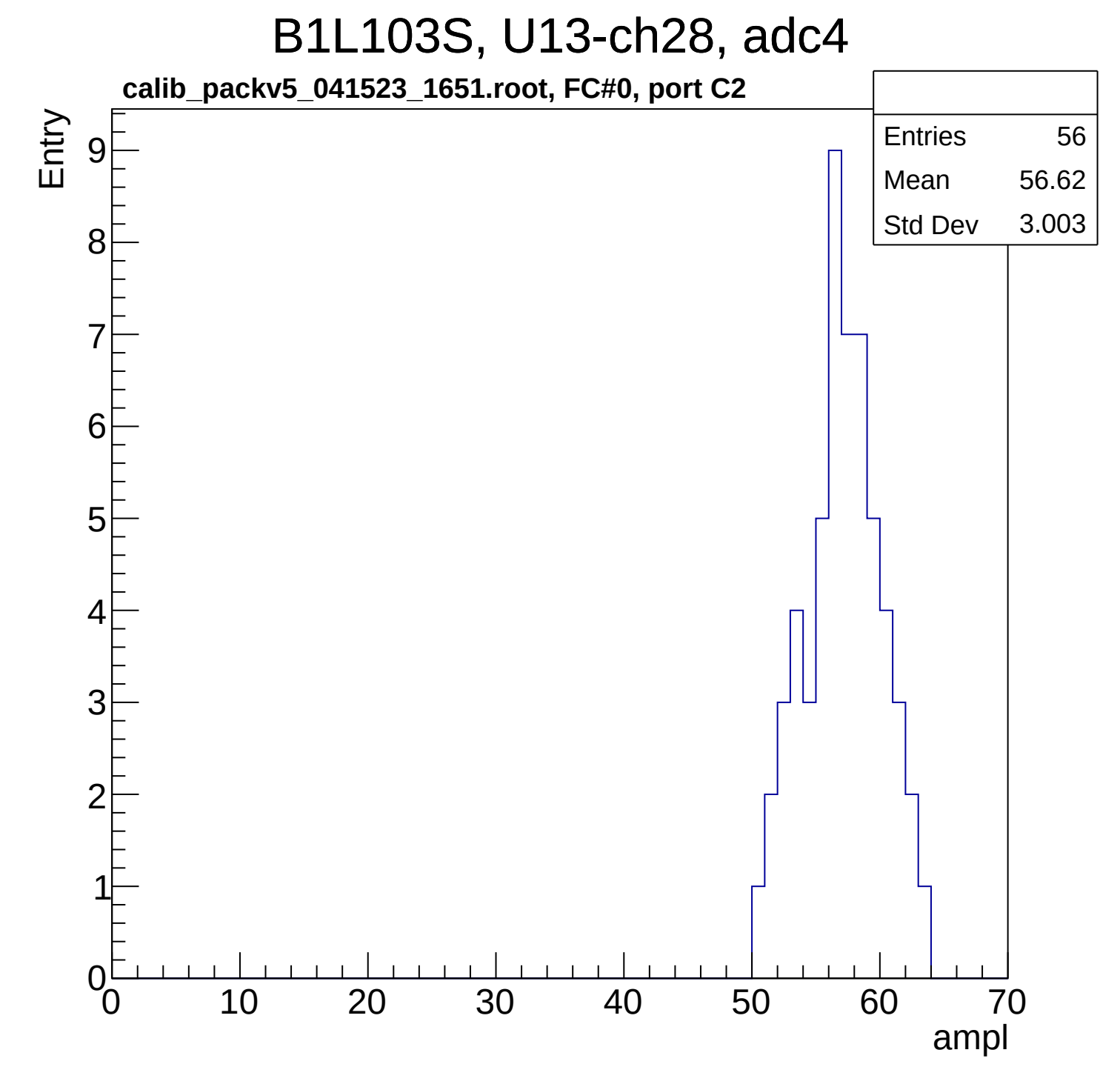
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch28, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 56.62
Std Dev 3.003
Entry
ampl
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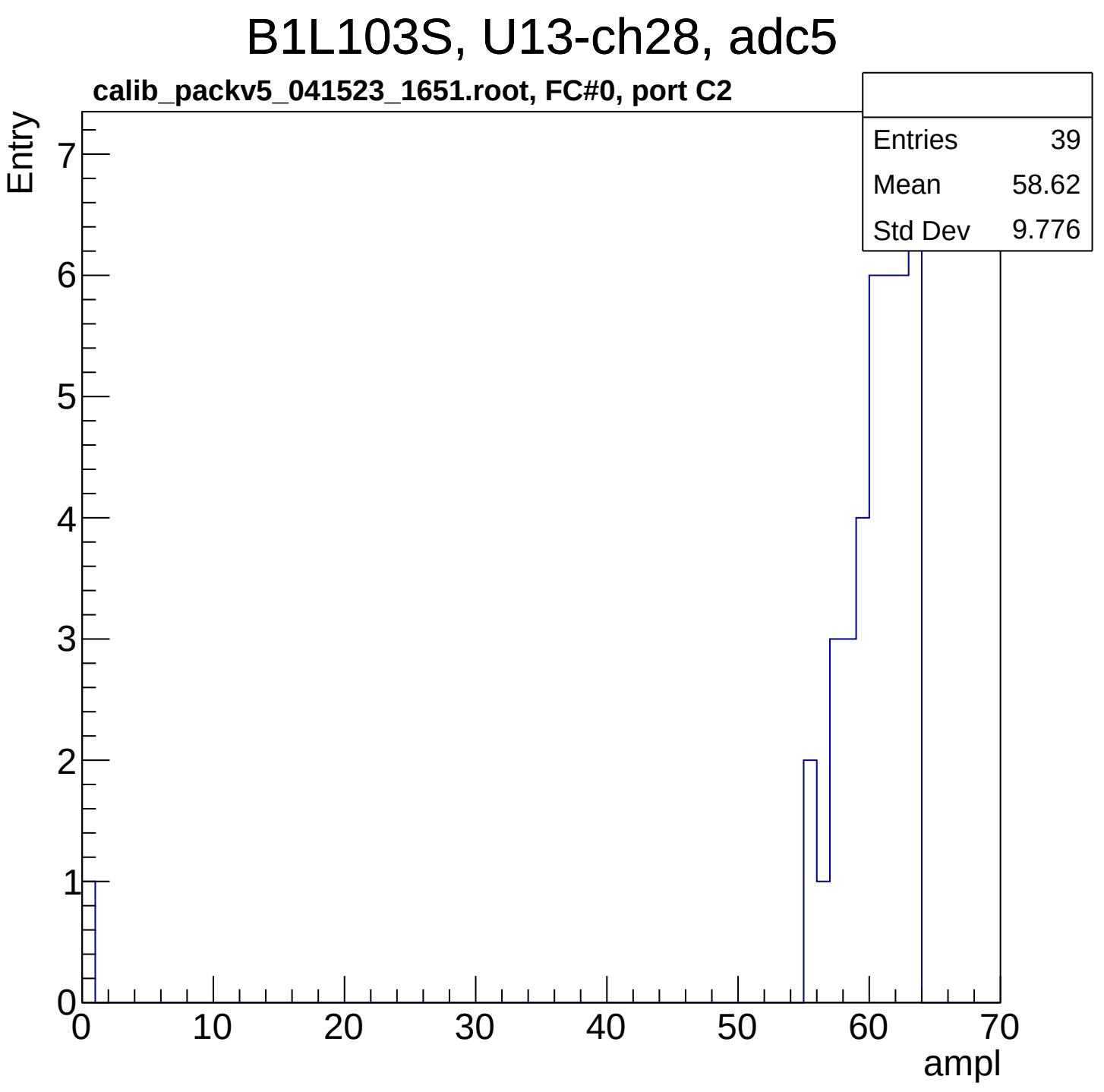
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch28, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 58.62
Std Dev 9.776
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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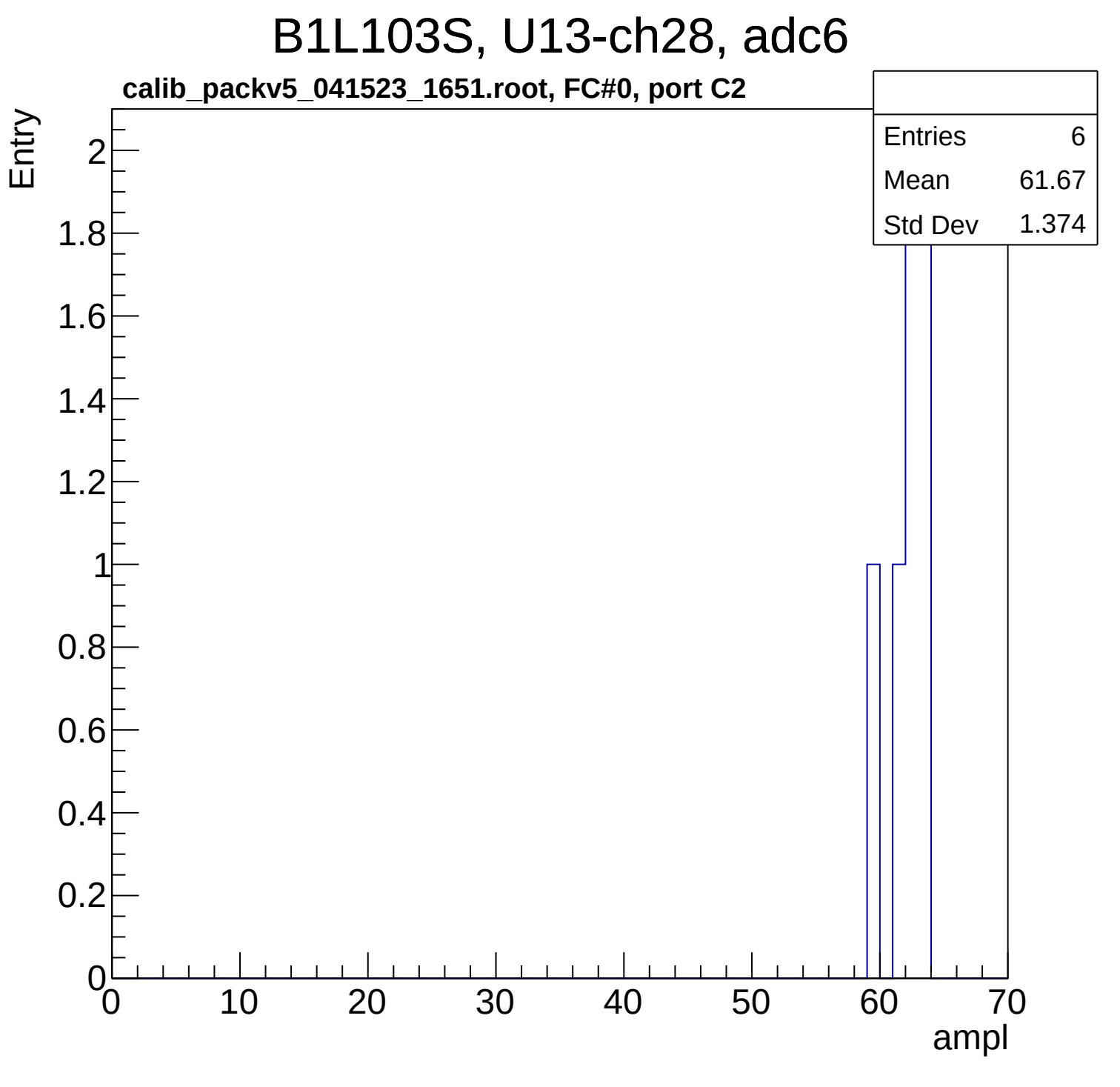
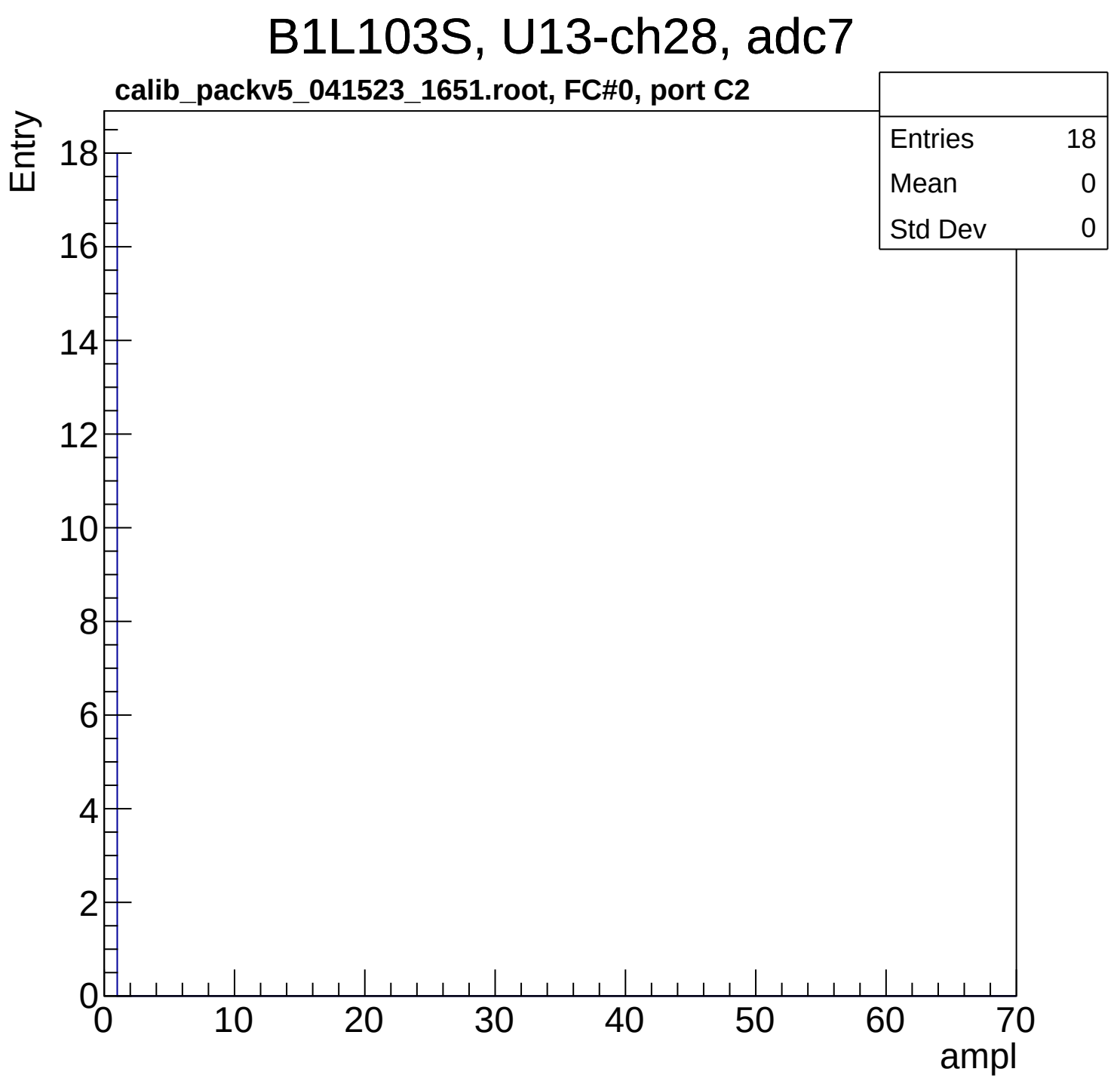
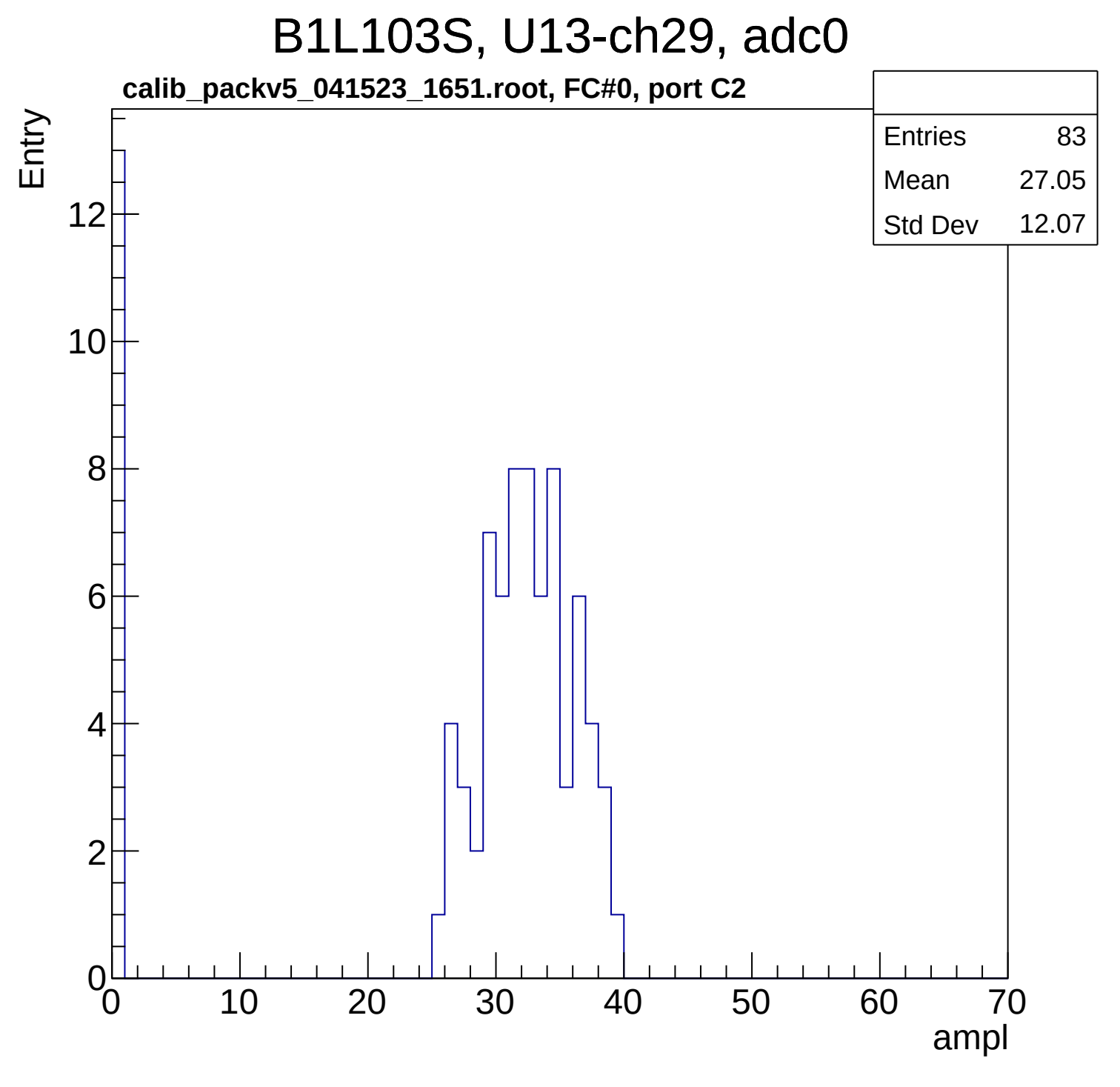
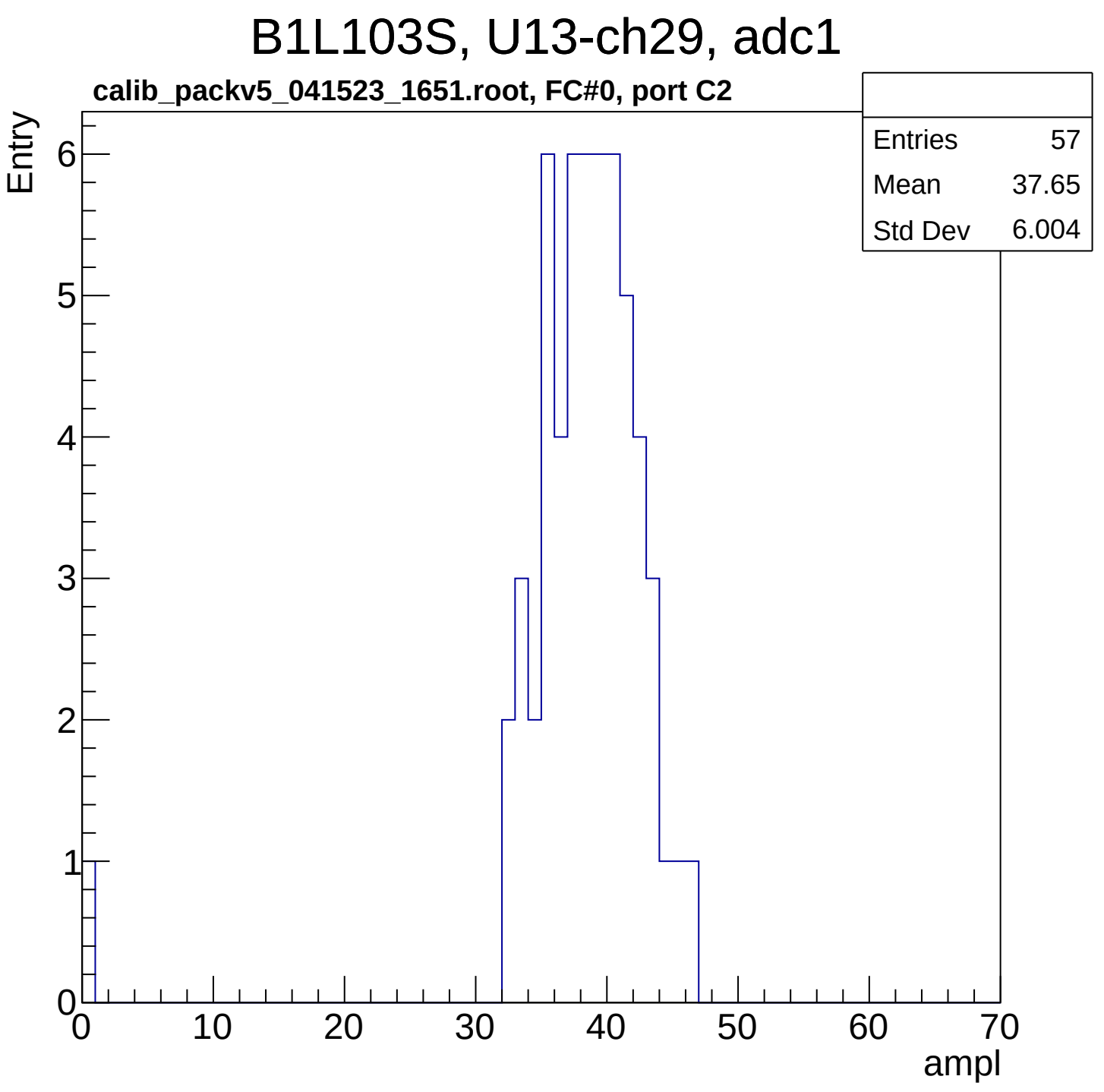
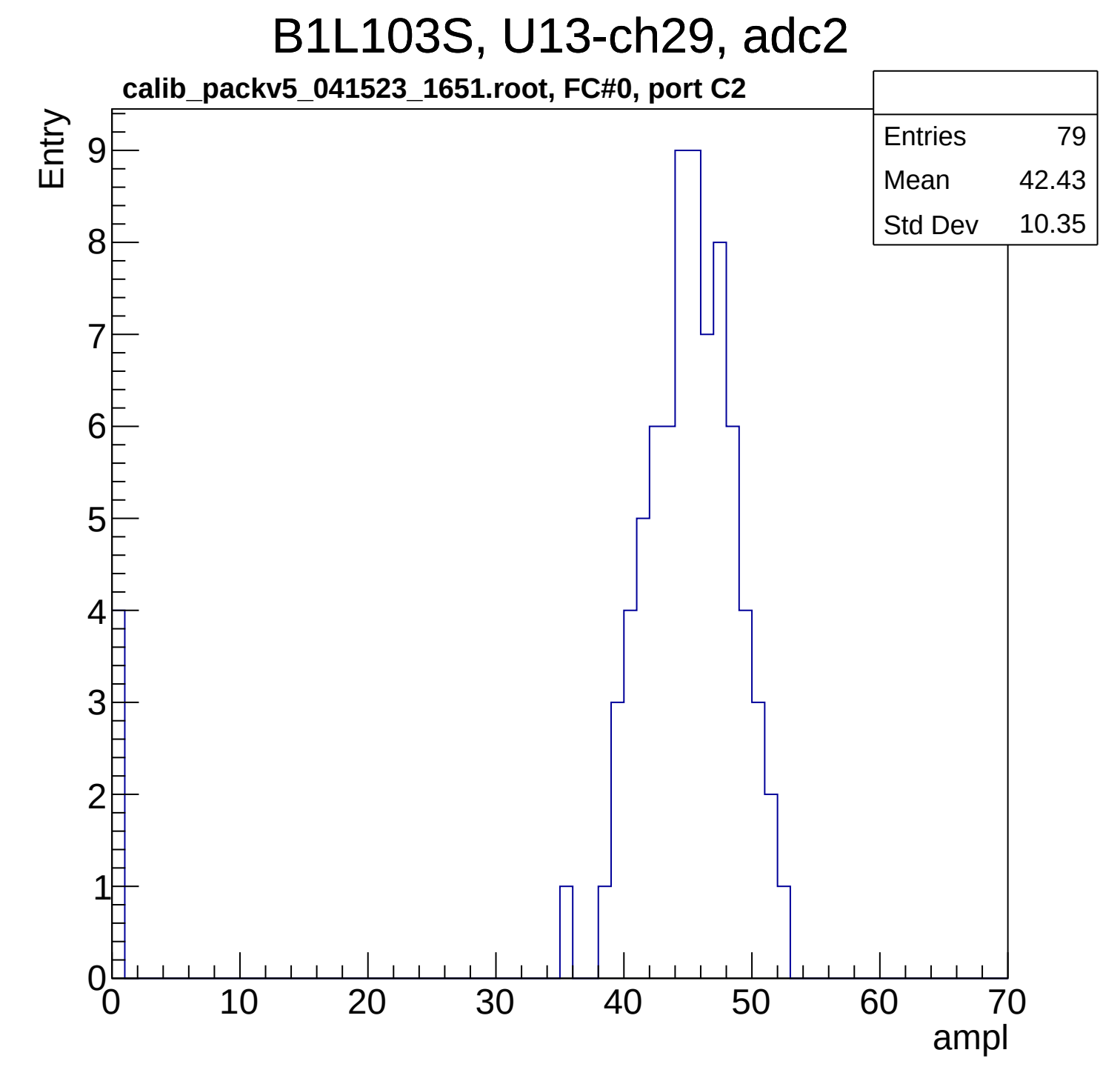
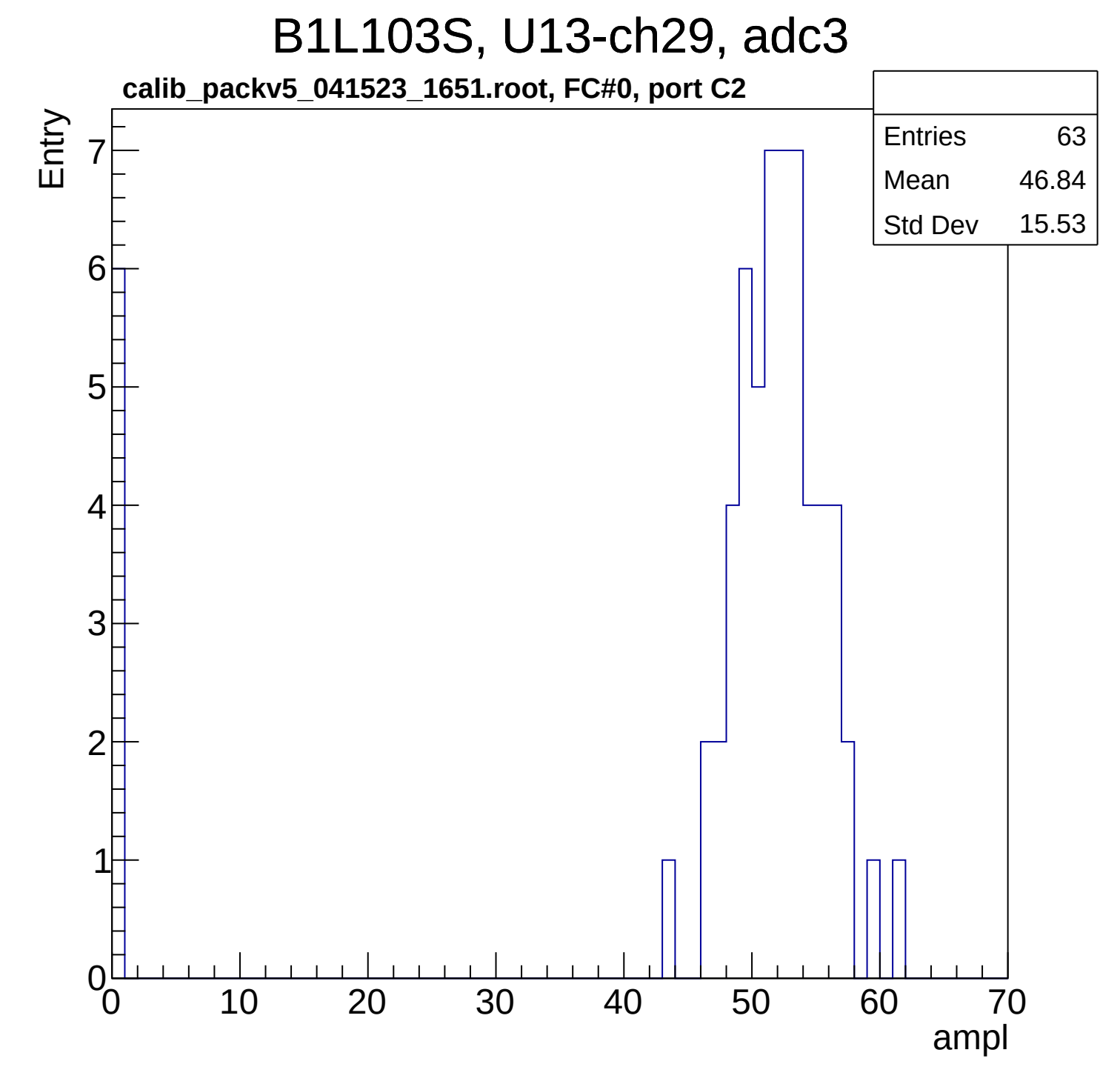

B1L103S, U13-ch28, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.67
Std Dev 1.374
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

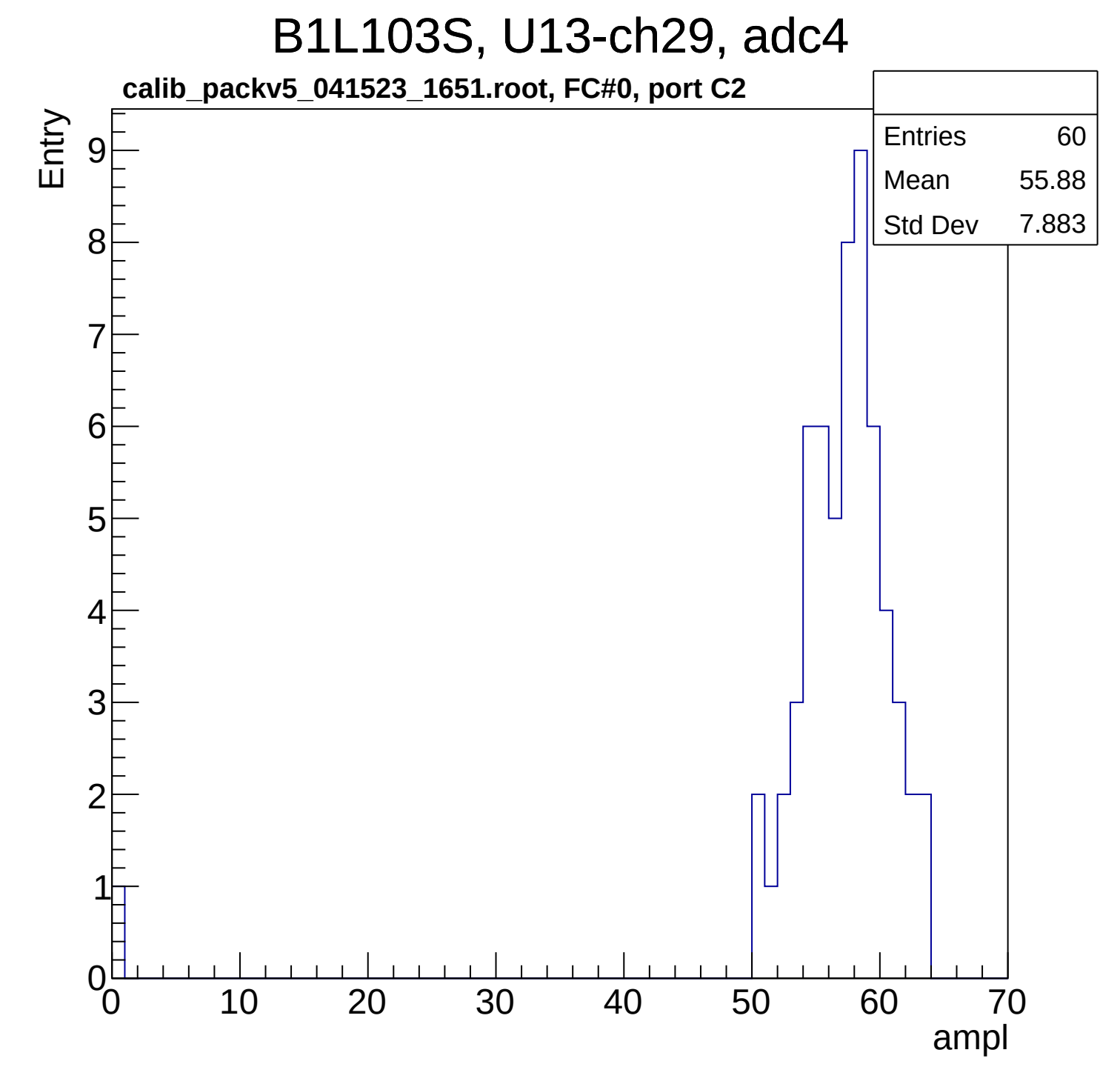

B1L103S, U13-ch28, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch29, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 27.05
Std Dev 12.07
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch29, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 37.65
Std Dev 6.004
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch29, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 42.43
Std Dev 10.35
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch29, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 46.84
Std Dev 15.53
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch29, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 55.88
Std Dev 7.883
Entry
ampl
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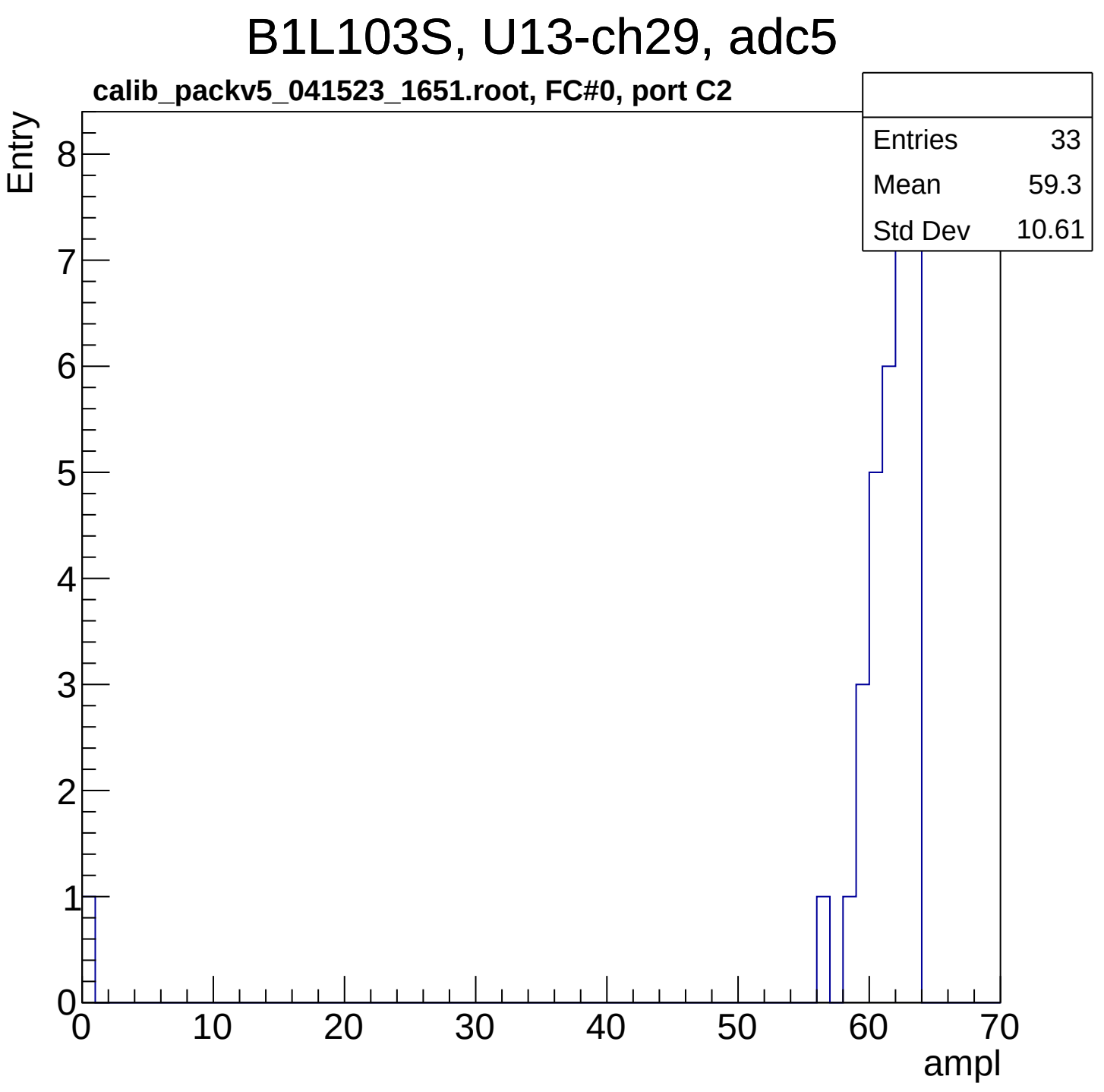
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch29, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 59.3
Std Dev 10.61
Entry
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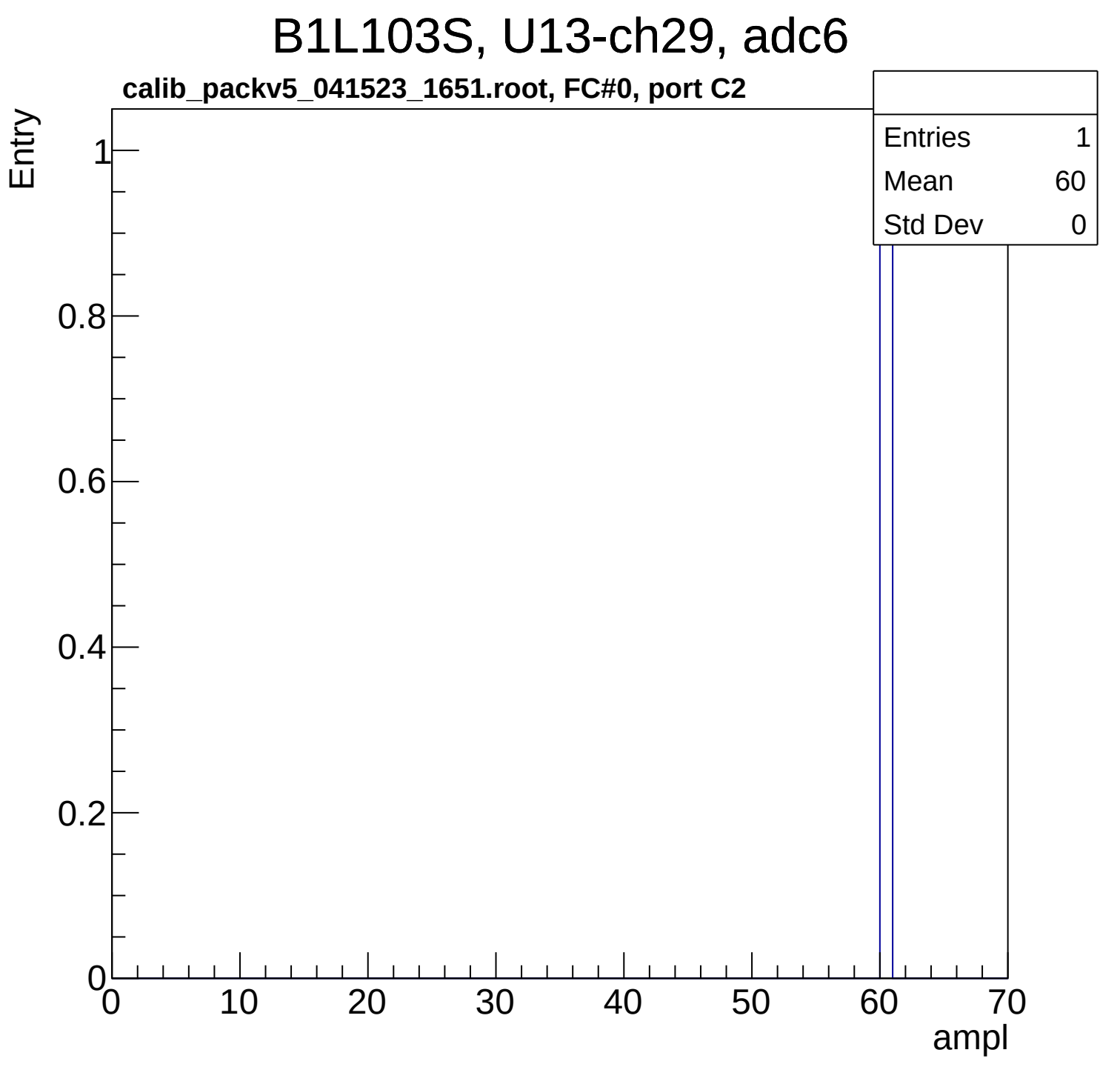
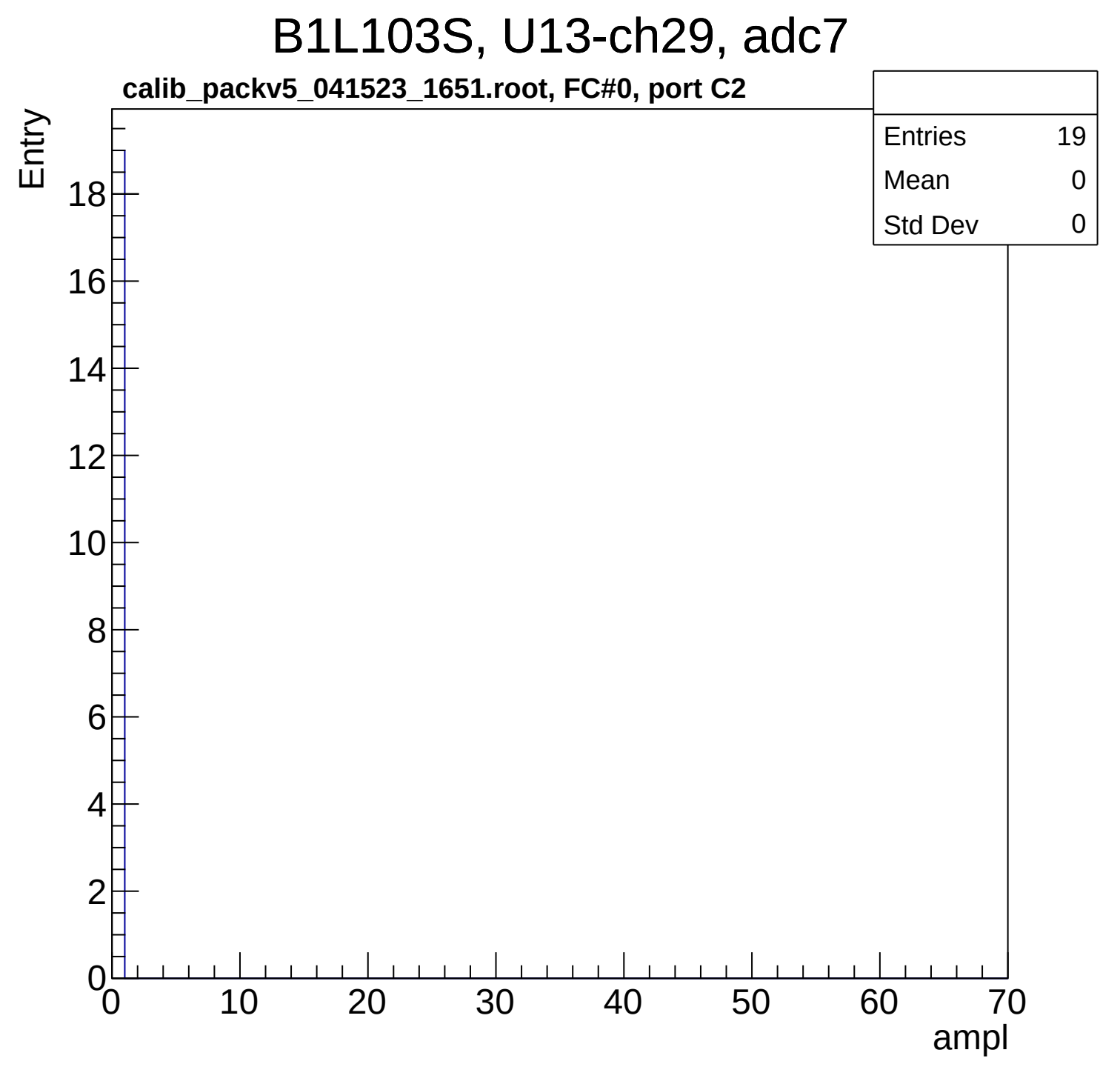
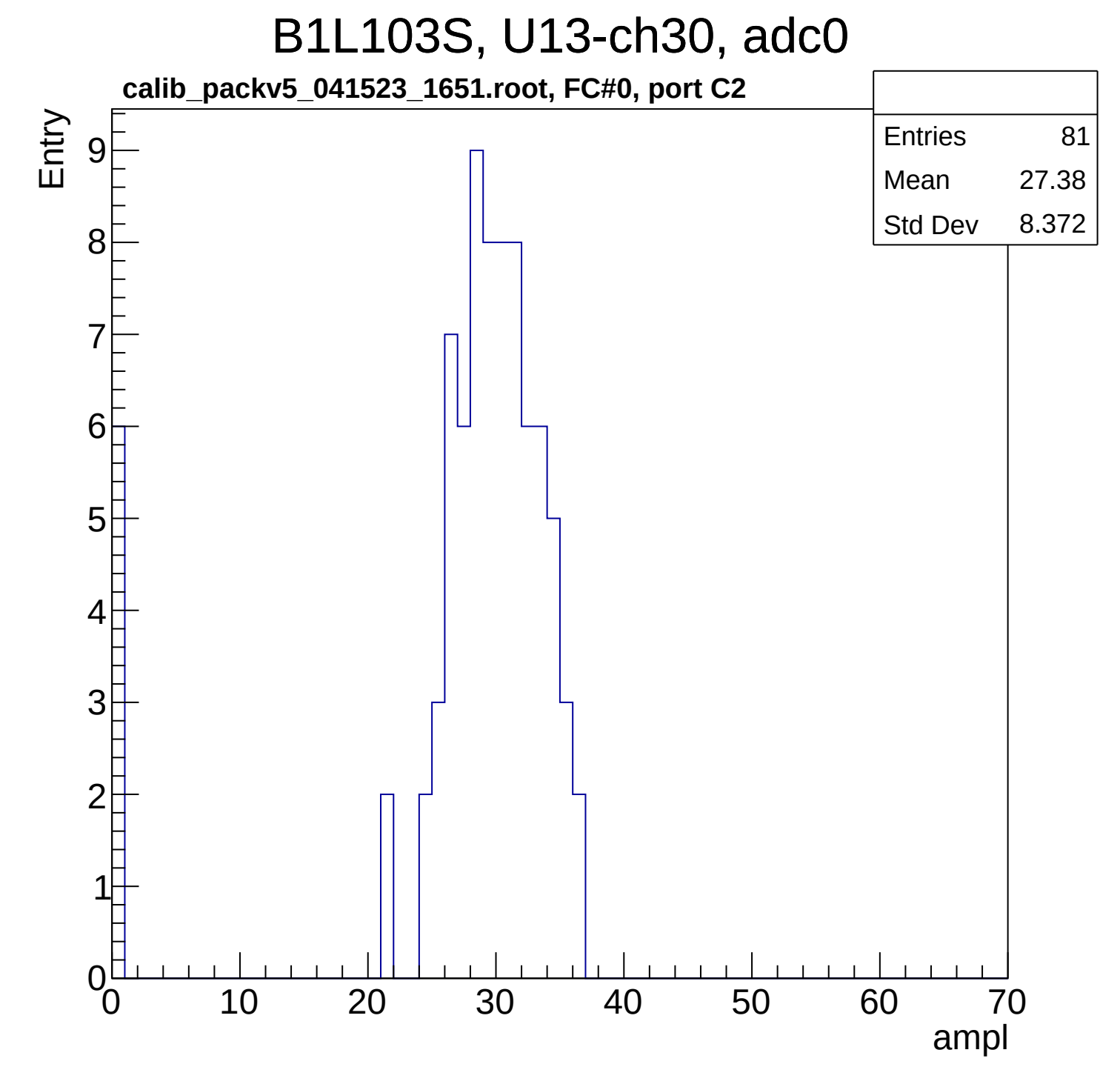
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch29, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 60
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch29, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch30, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 27.38
Std Dev 8.372
Entry
ampl
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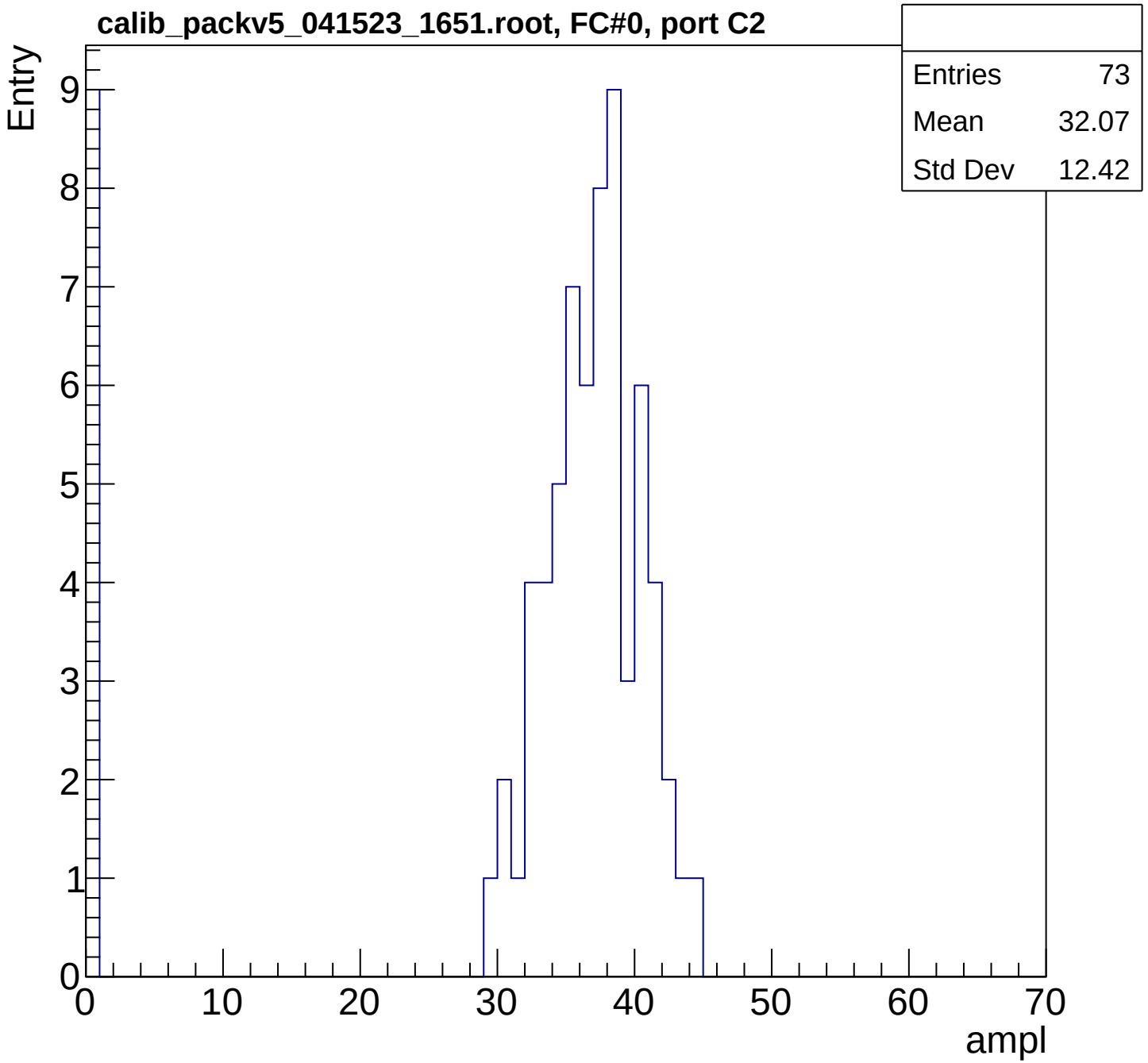
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch30, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 32.07
Std Dev 12.42
Entry
ampl
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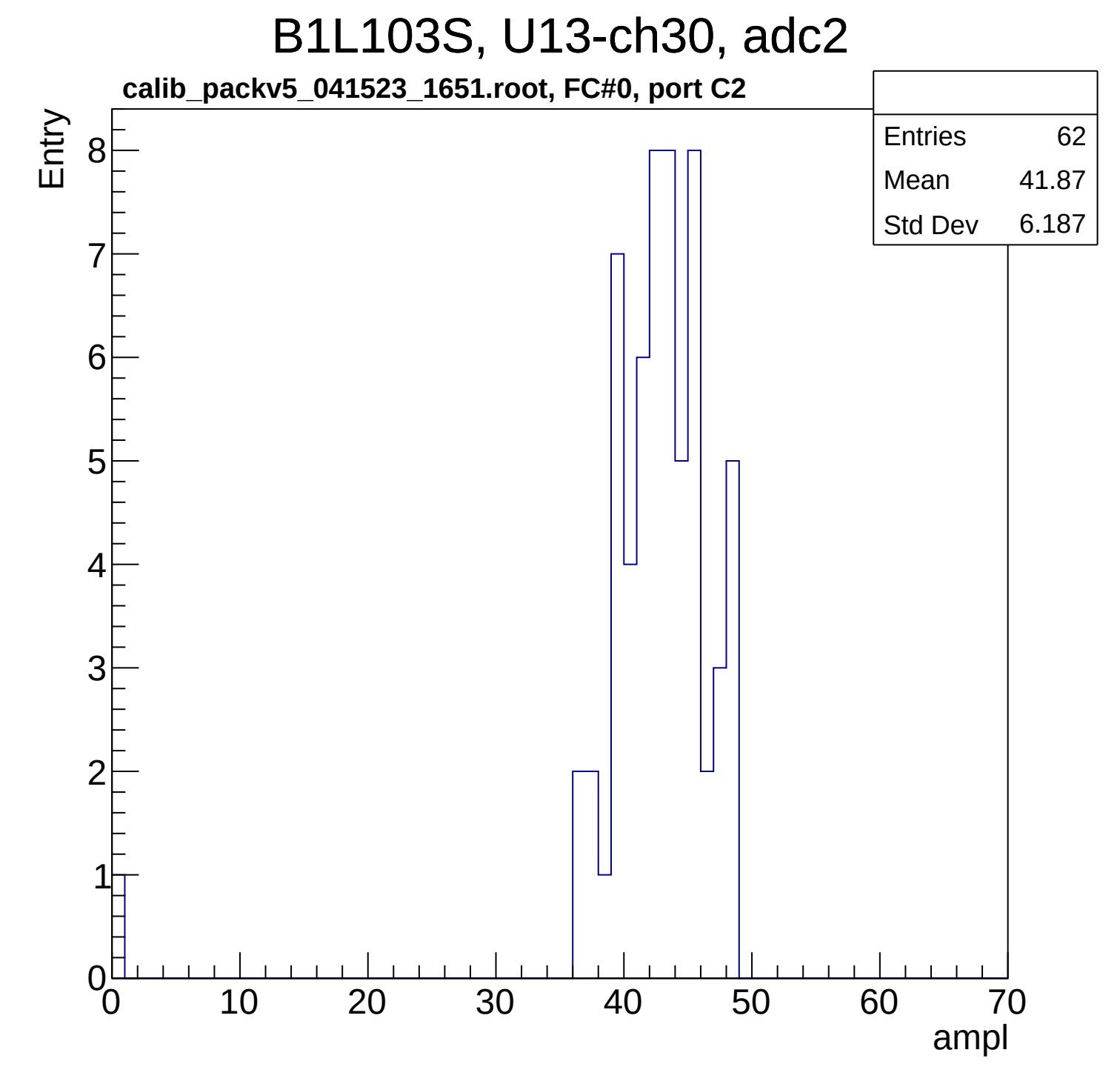
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch30, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 41.87
Std Dev 6.187
Entry
ampl
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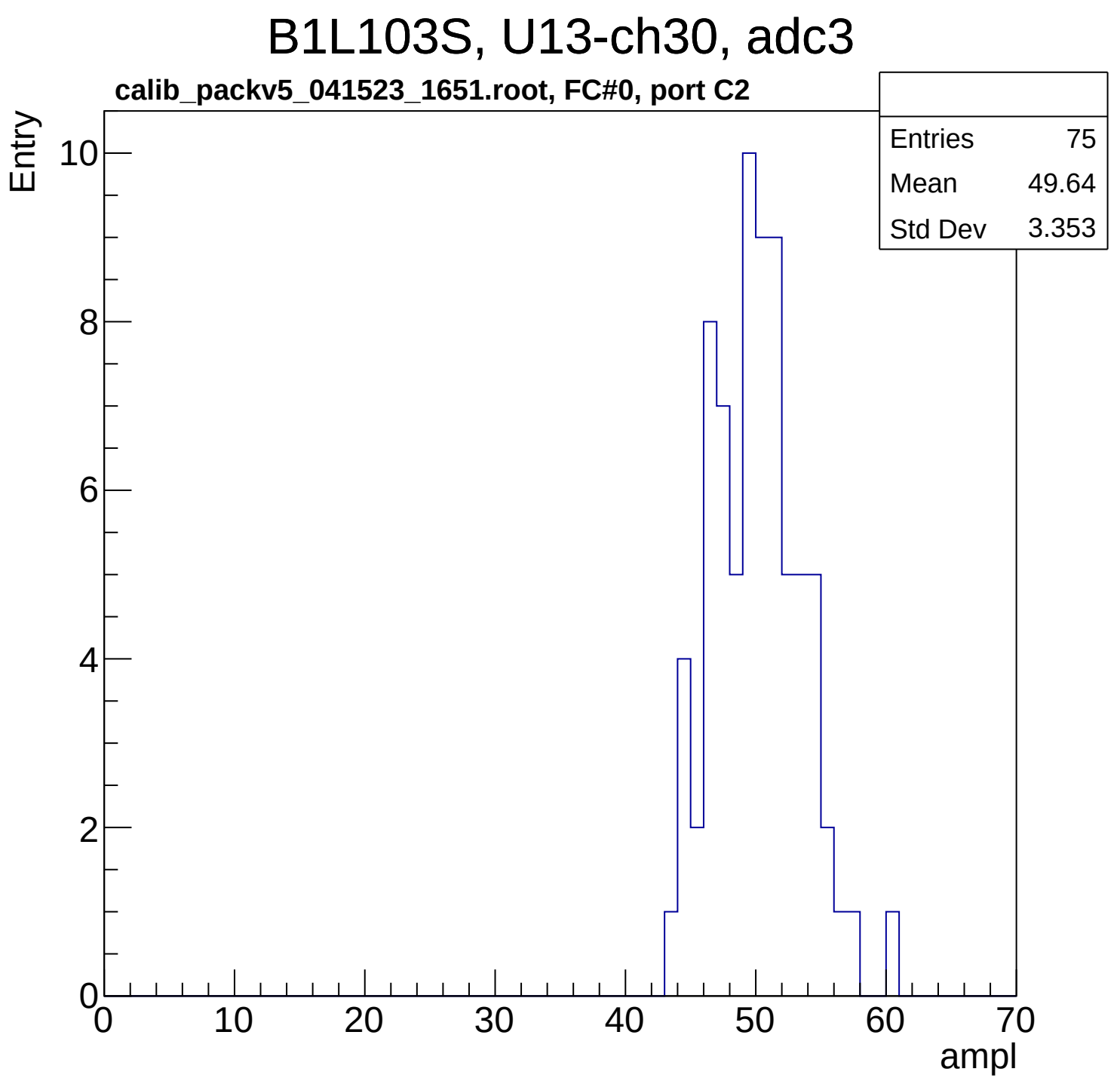
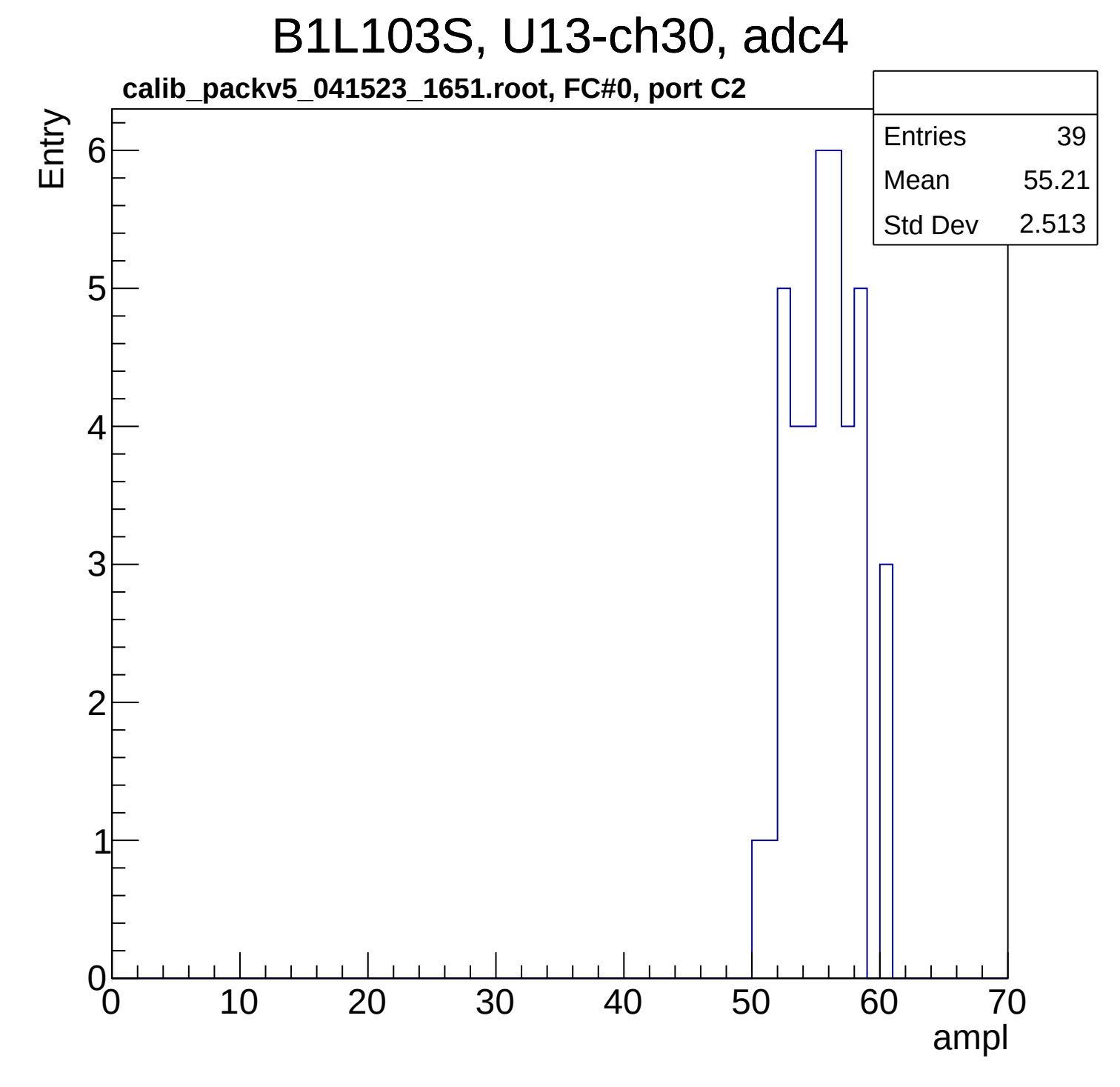
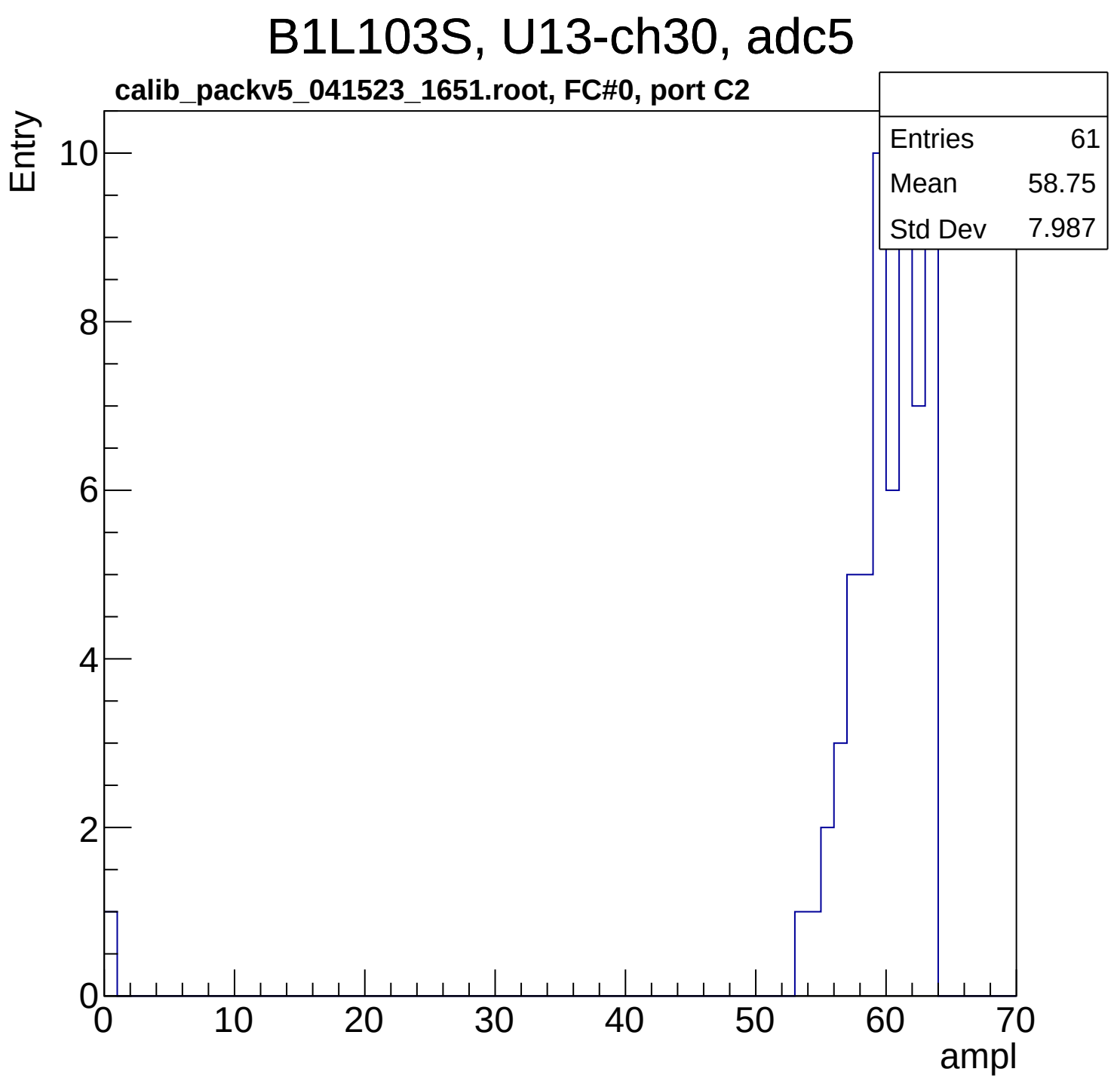
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch30, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 49.64
Std Dev 3.353
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch30, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 55.21
Std Dev 2.513
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U13-ch30, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 58.75
Std Dev 7.987
Entry
ampl
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2
4
6
8
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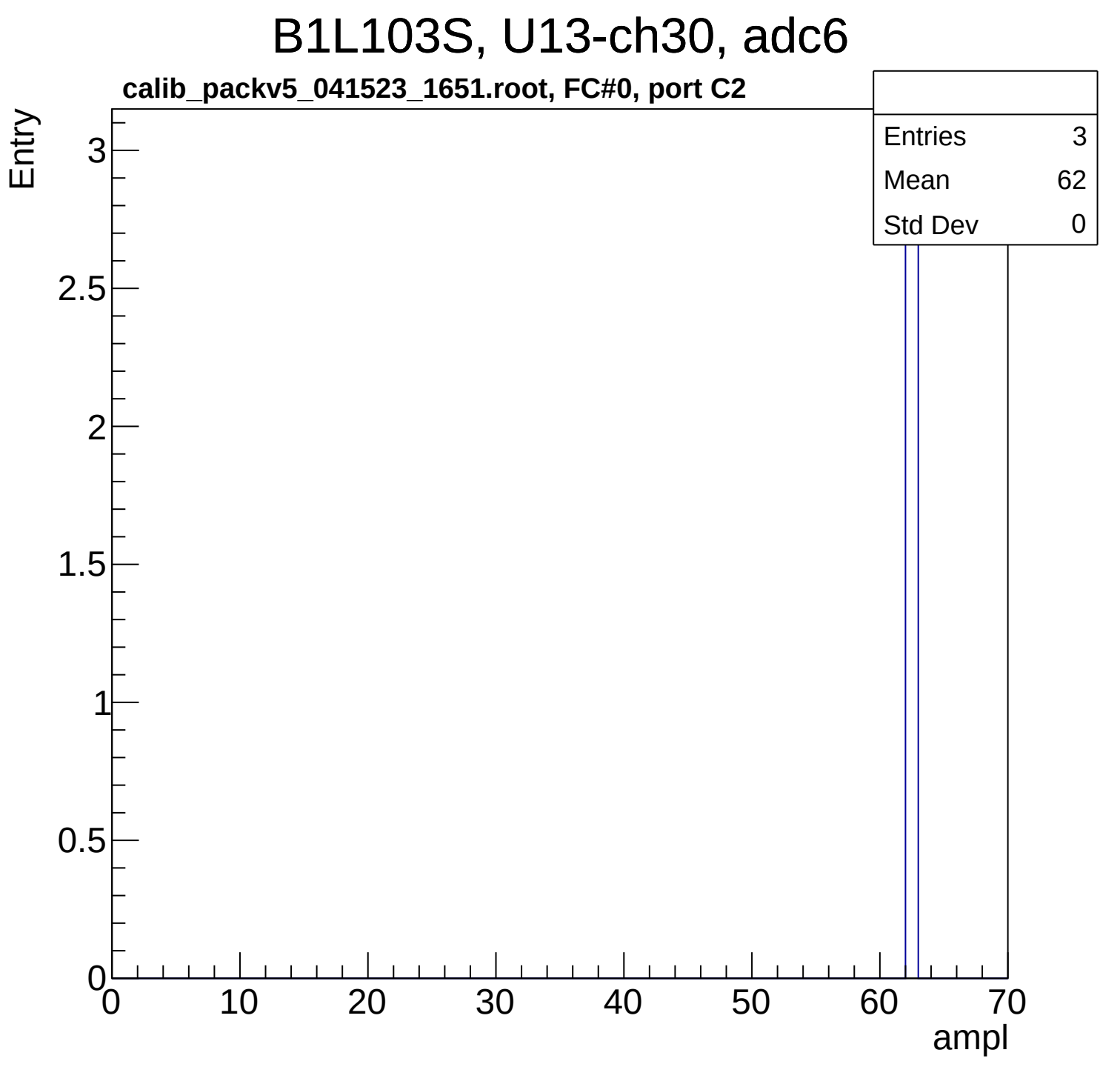
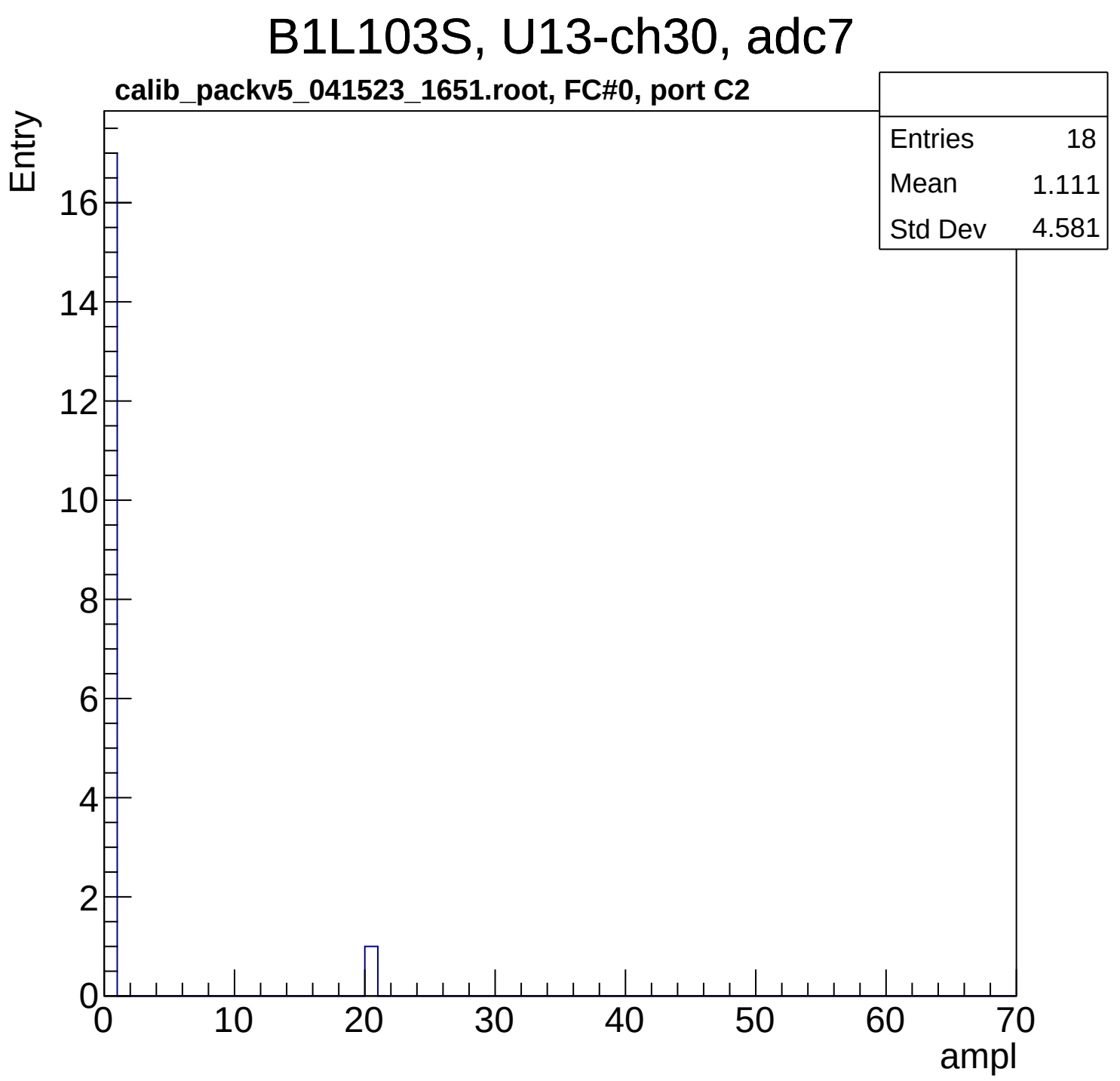
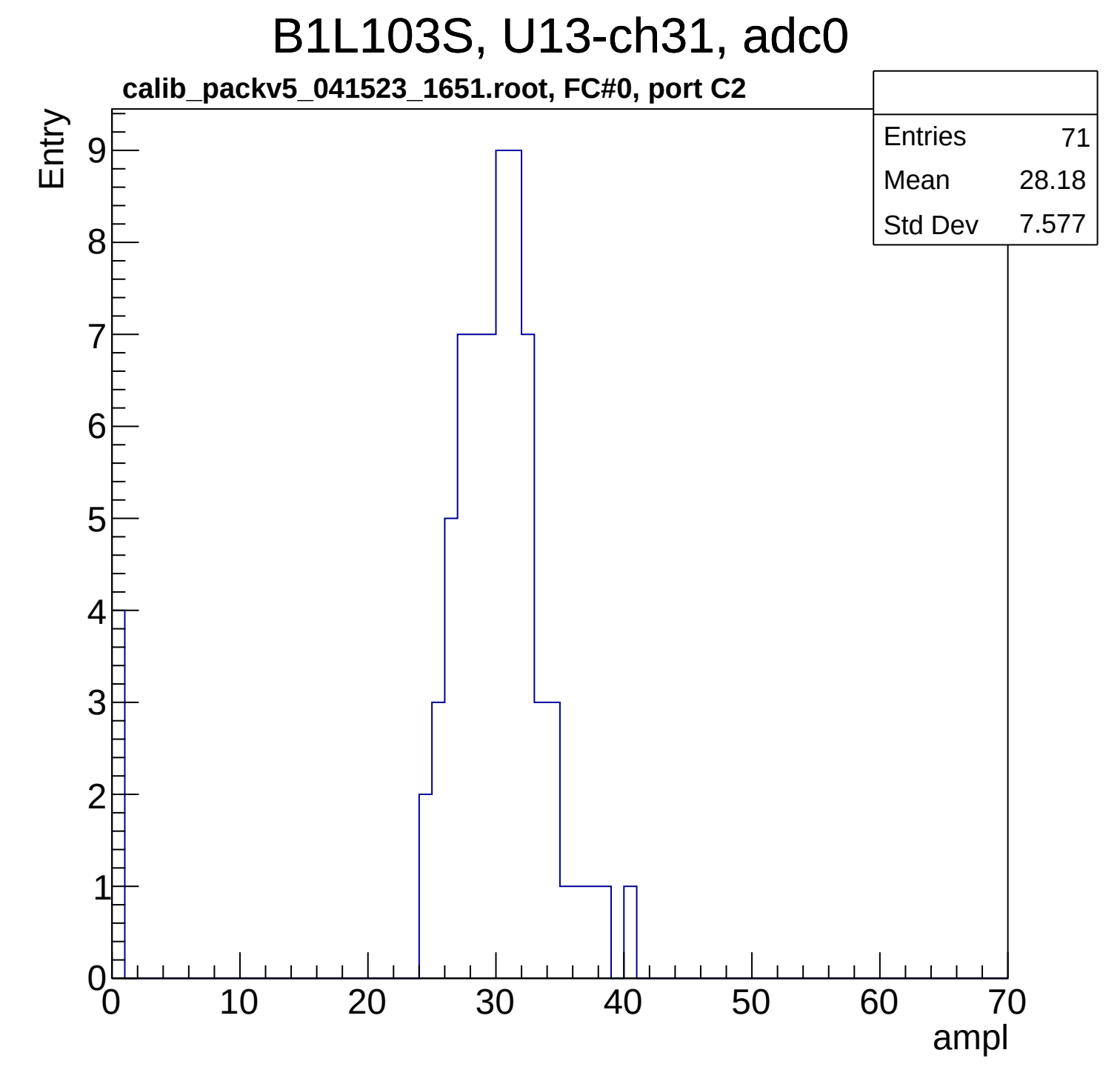
0
10
20
30
40
50
60
70


B1L103S, U13-ch30, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62
Std Dev 0
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U13-ch30, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.111
Std Dev 4.581
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch31, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 28.18
Std Dev 7.577
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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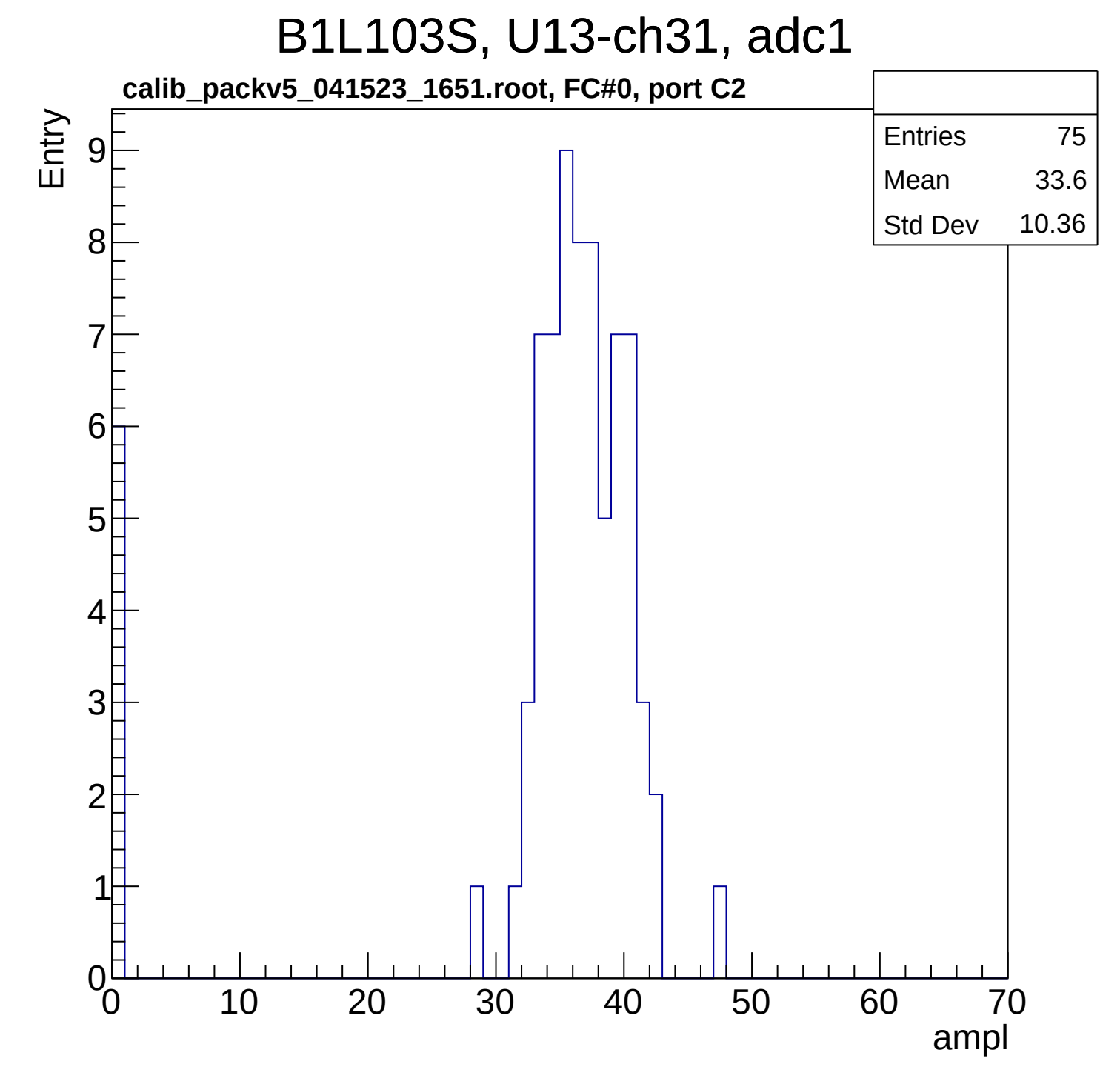
B1L103S, U13-ch31, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 33.6
Std Dev 10.36
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
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60
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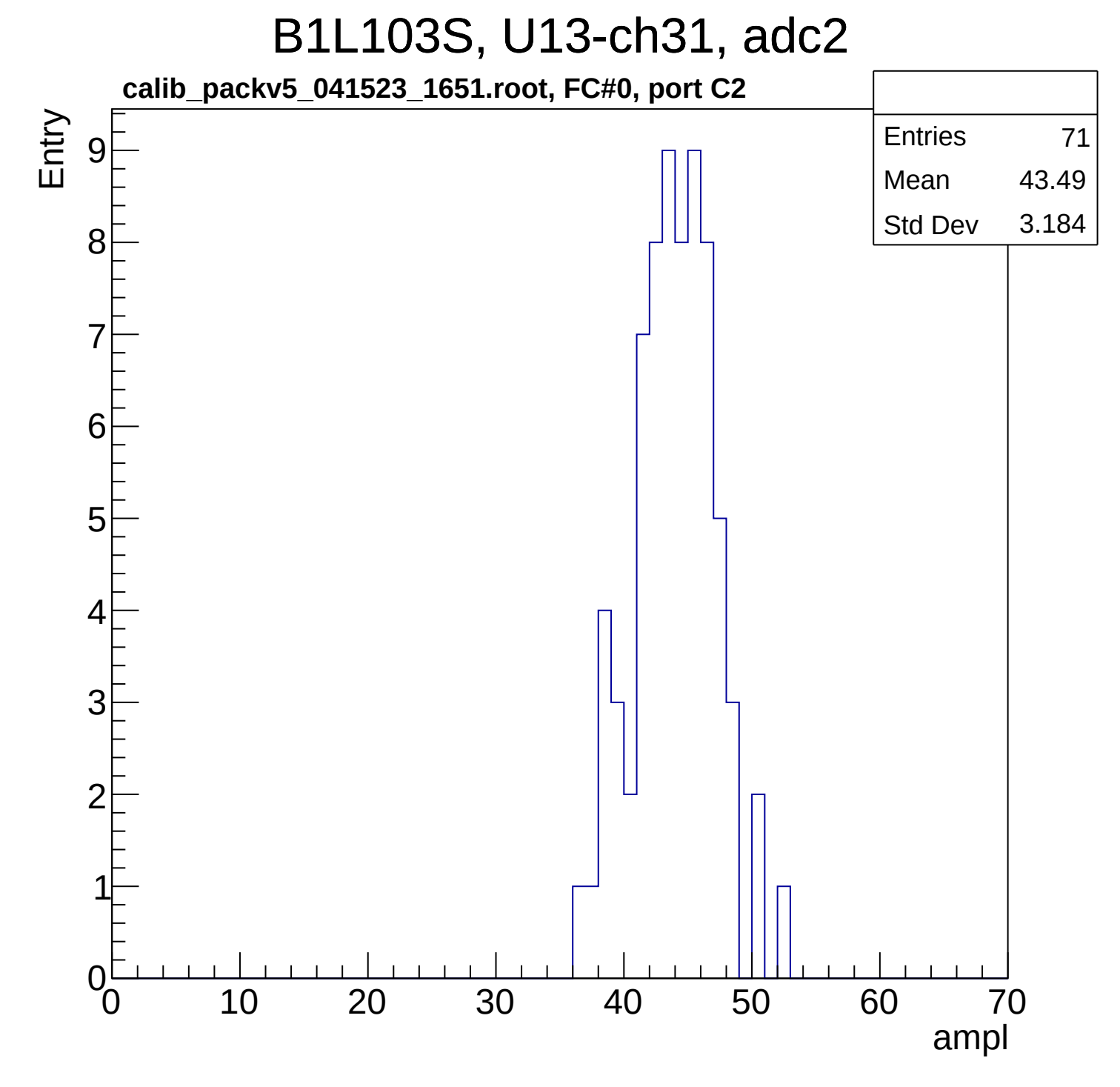
B1L103S, U13-ch31, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 43.49
Std Dev 3.184
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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30
40
50
60
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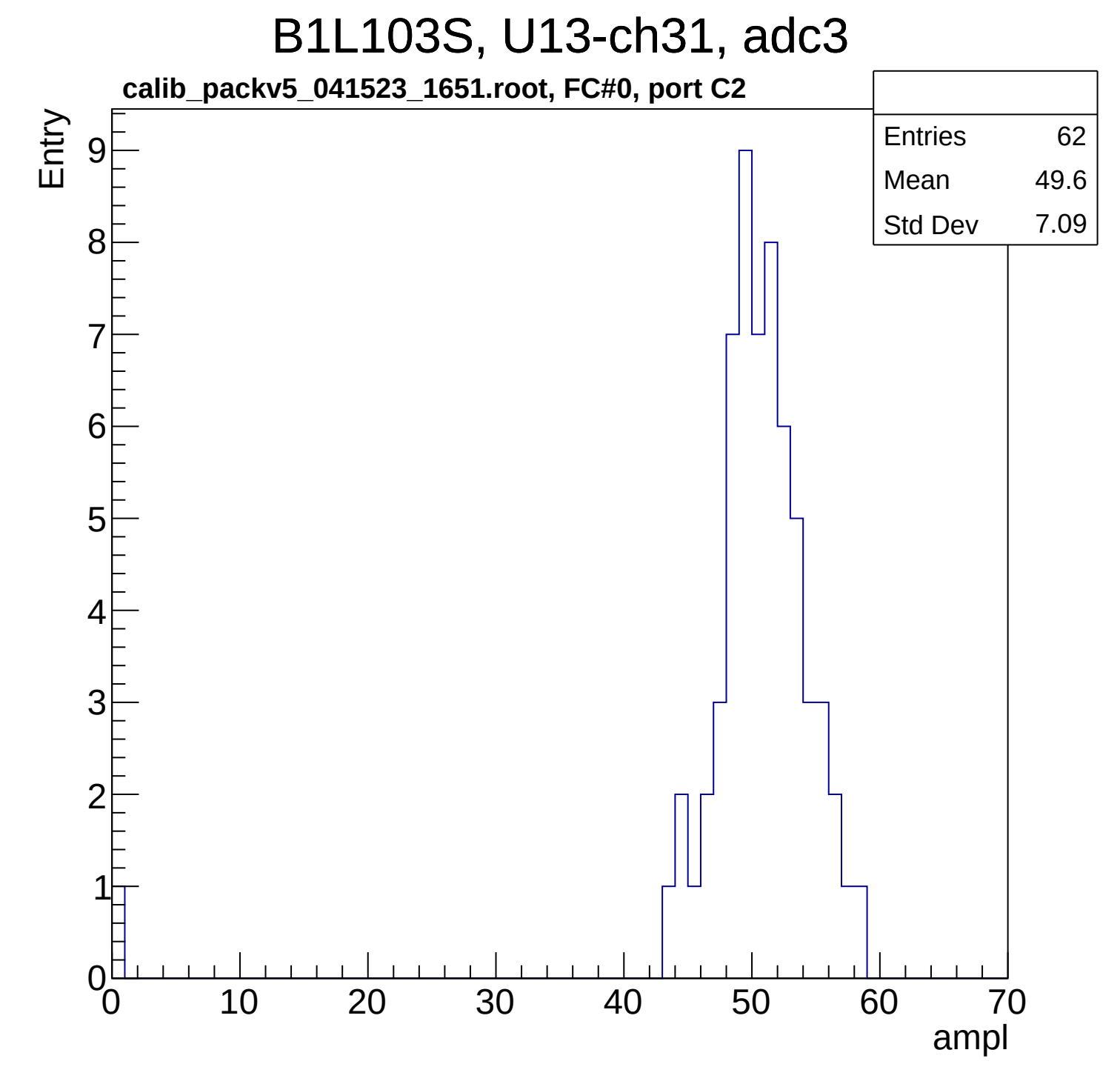
B1L103S, U13-ch31, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 49.6
Std Dev 7.09
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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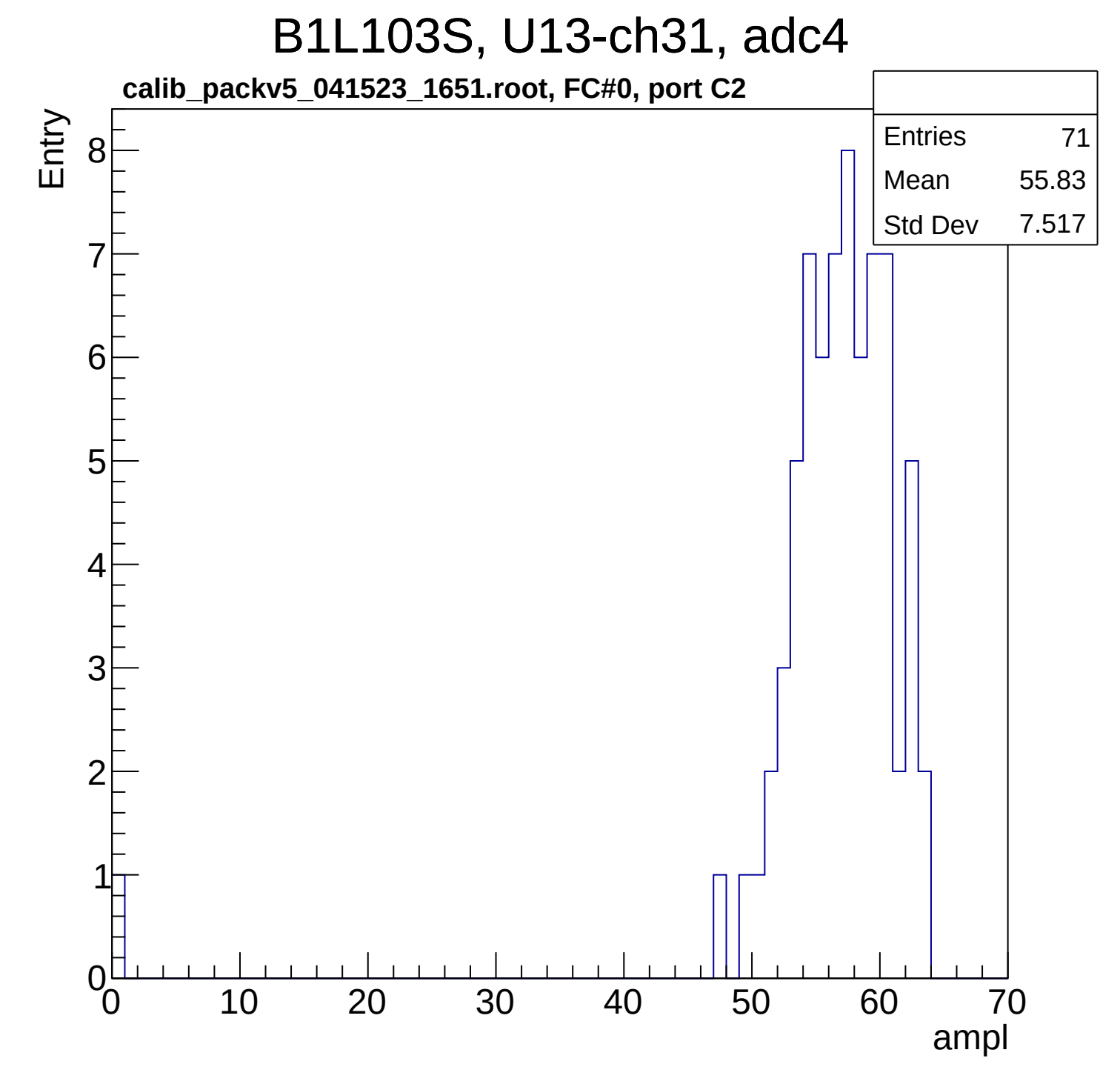
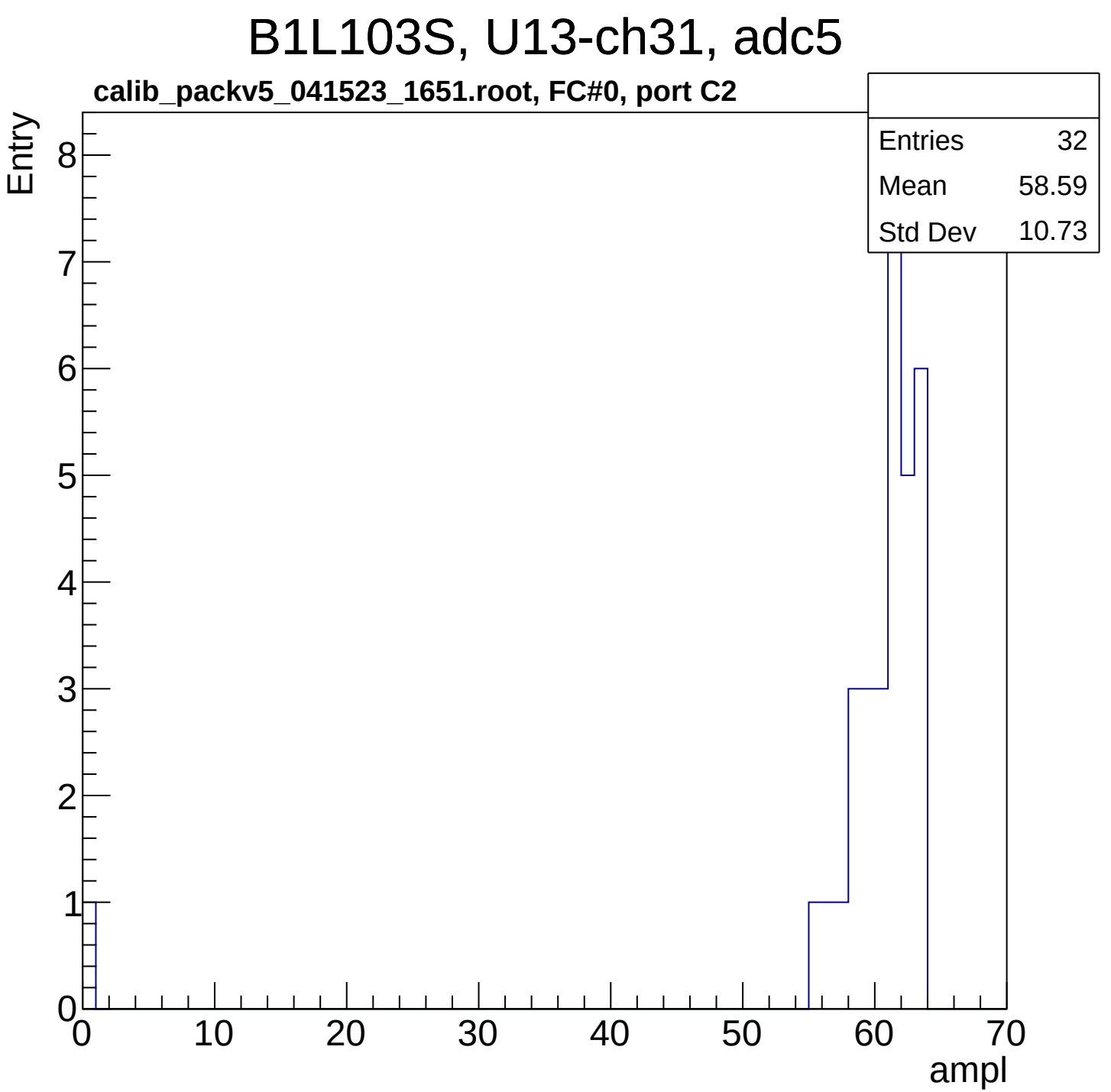

B1L103S, U13-ch31, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 55.83
Std Dev 7.517
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch31, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 58.59
Std Dev 10.73
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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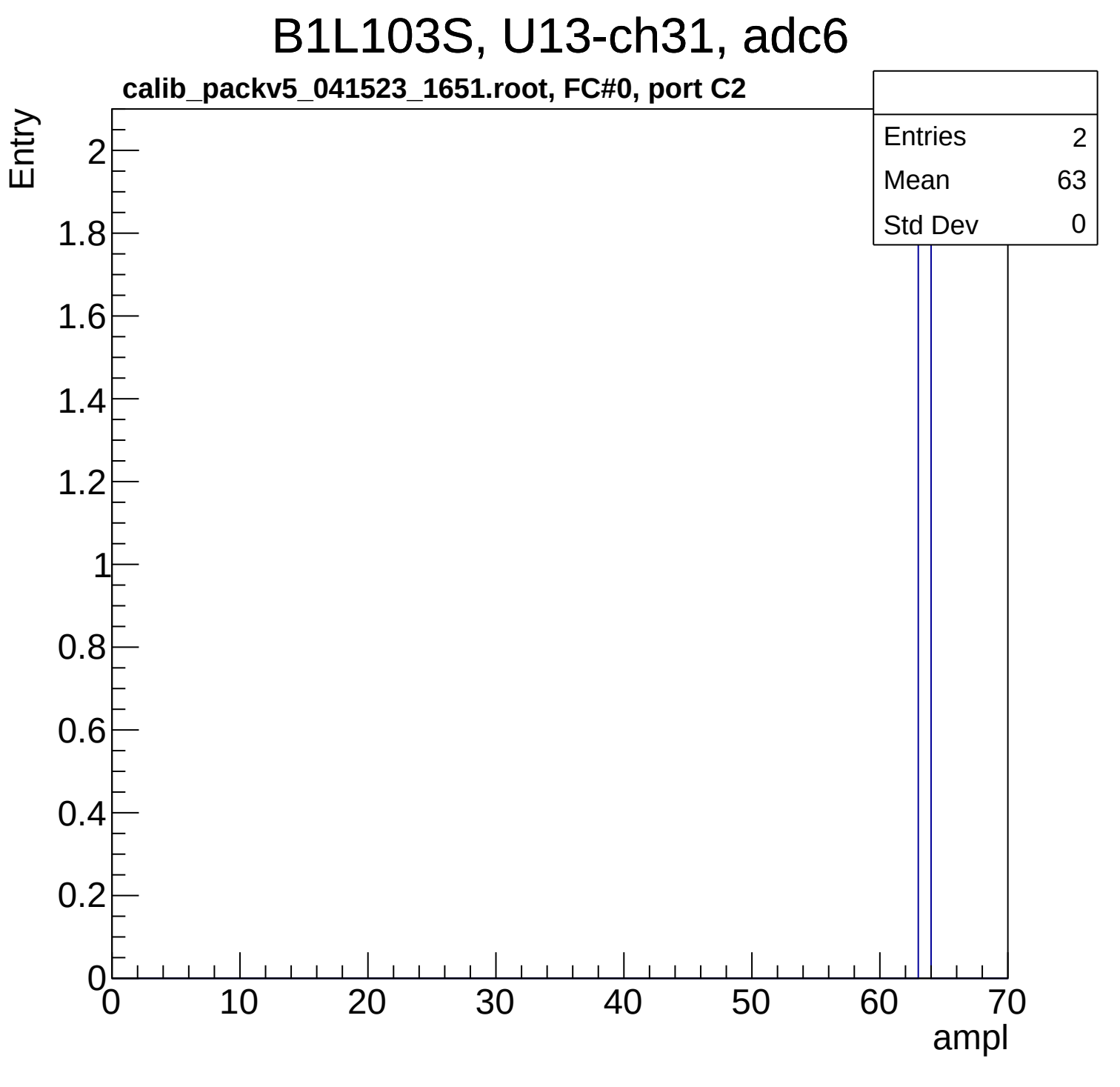
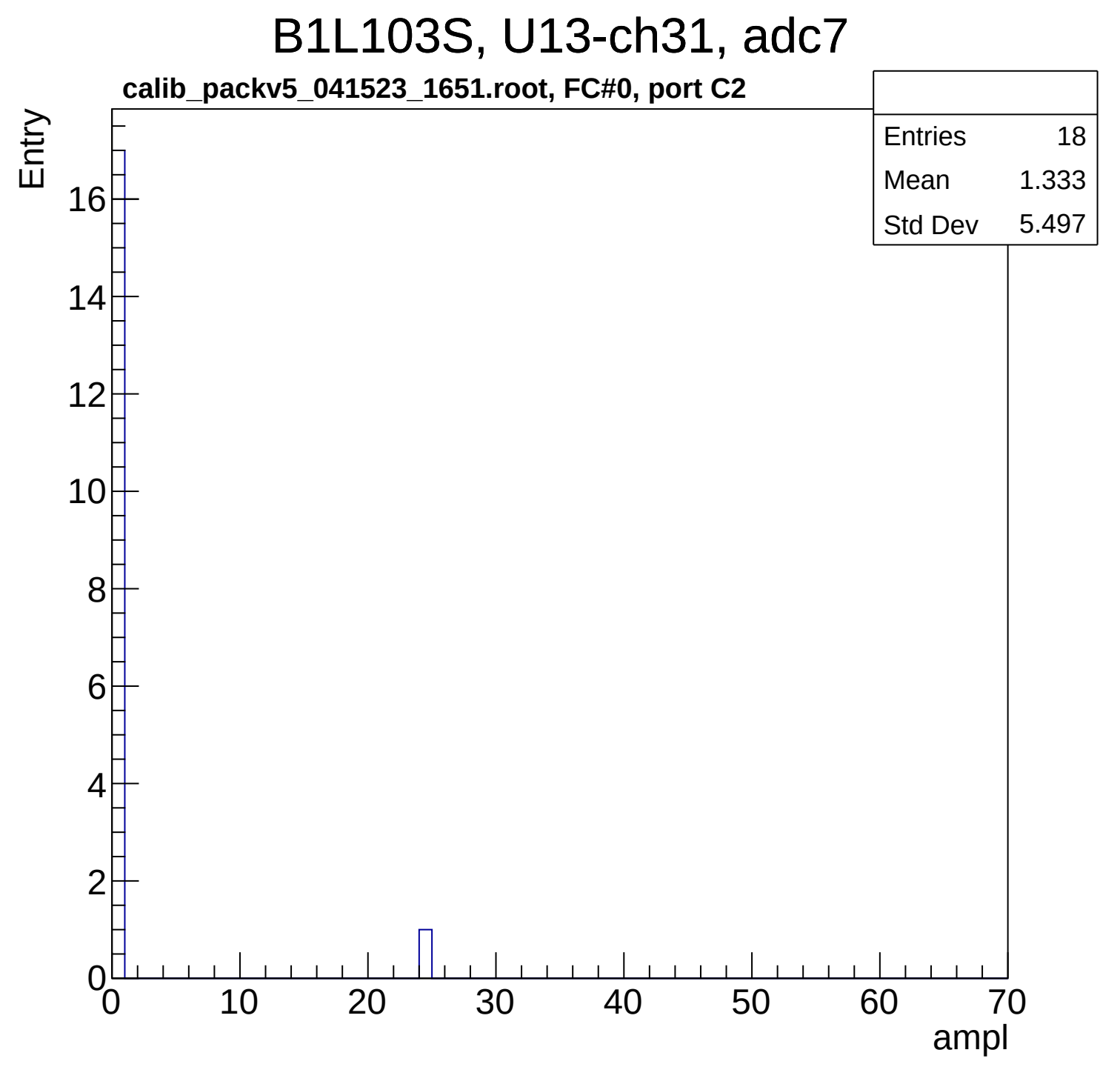
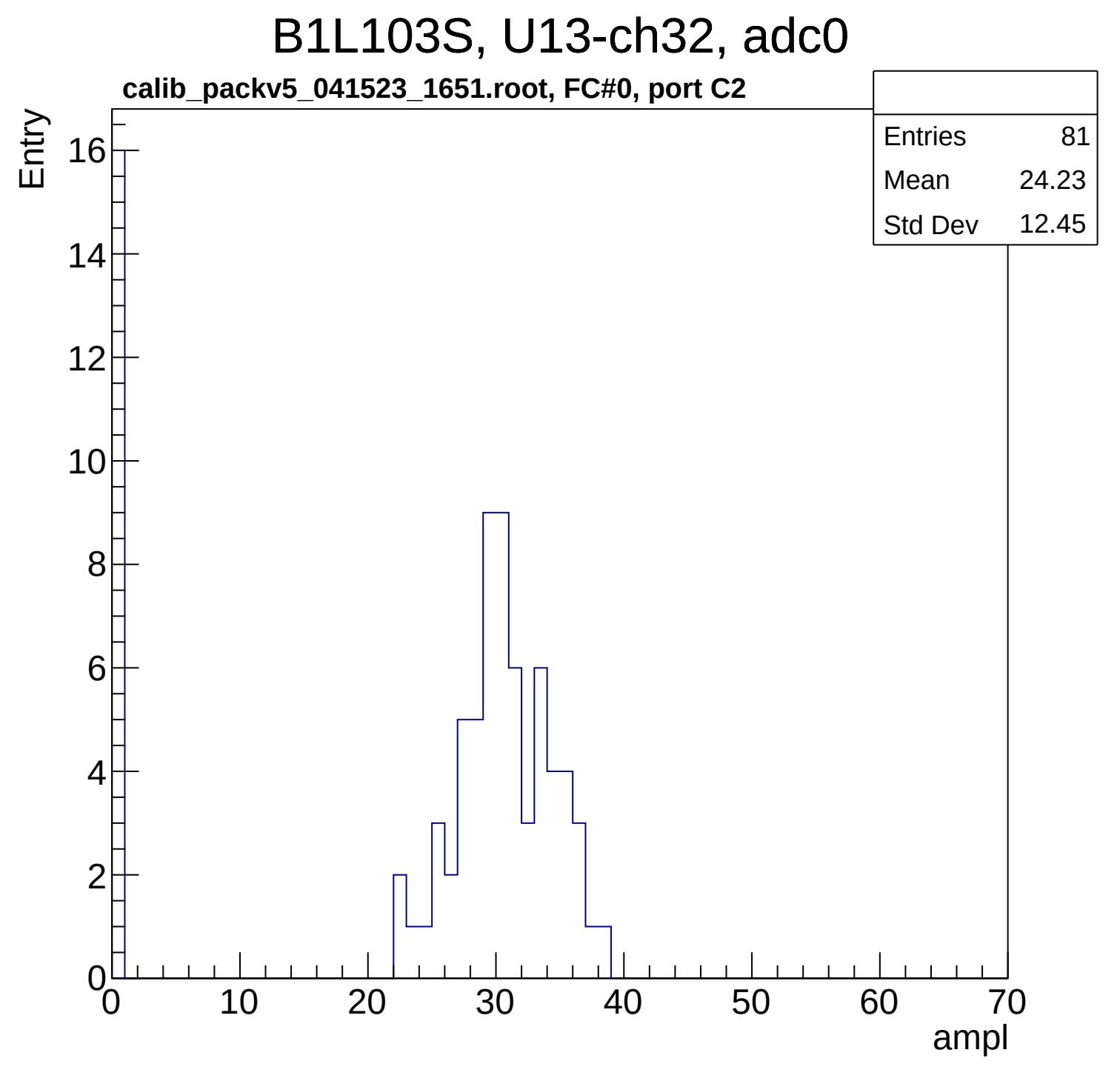
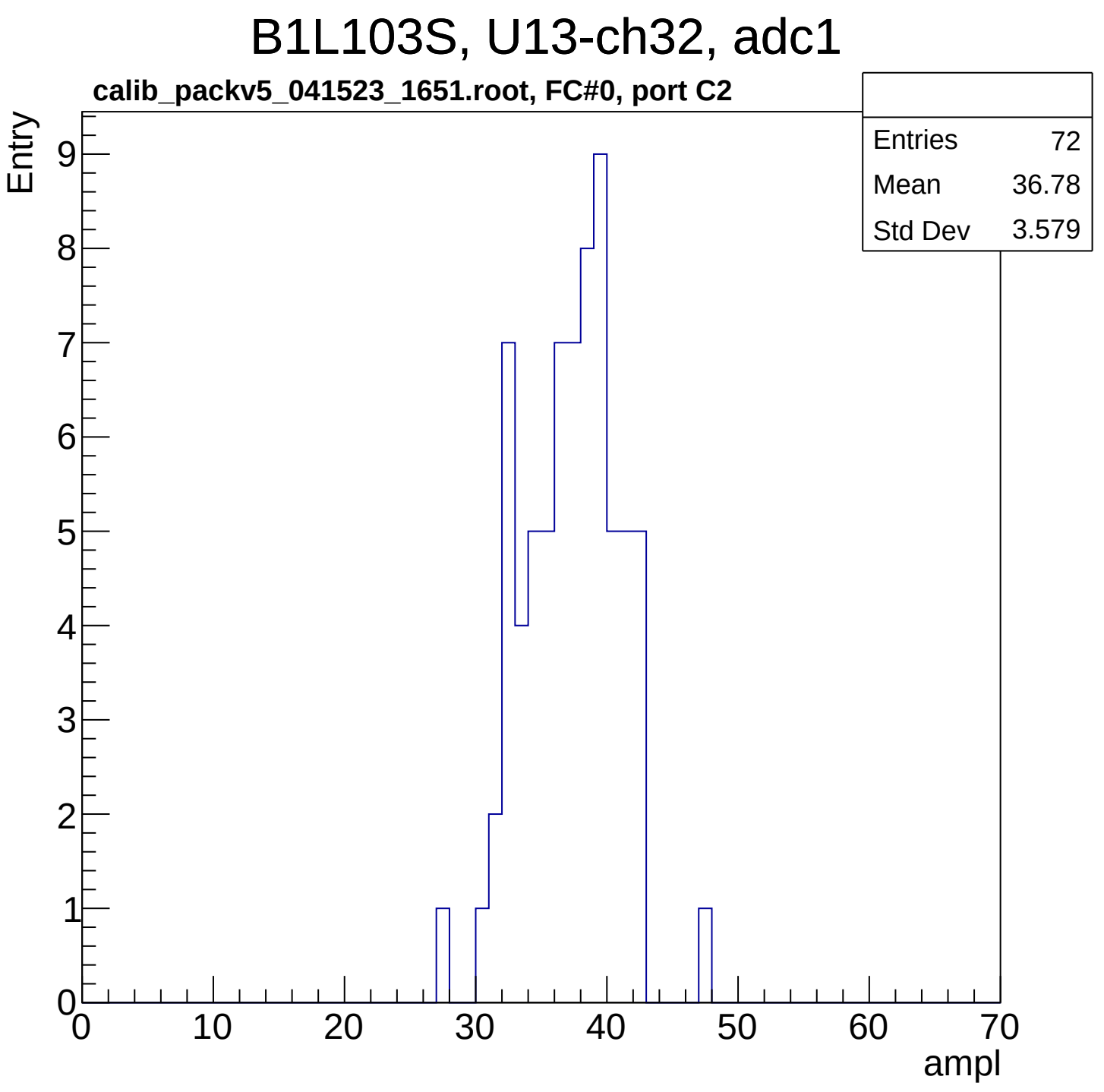
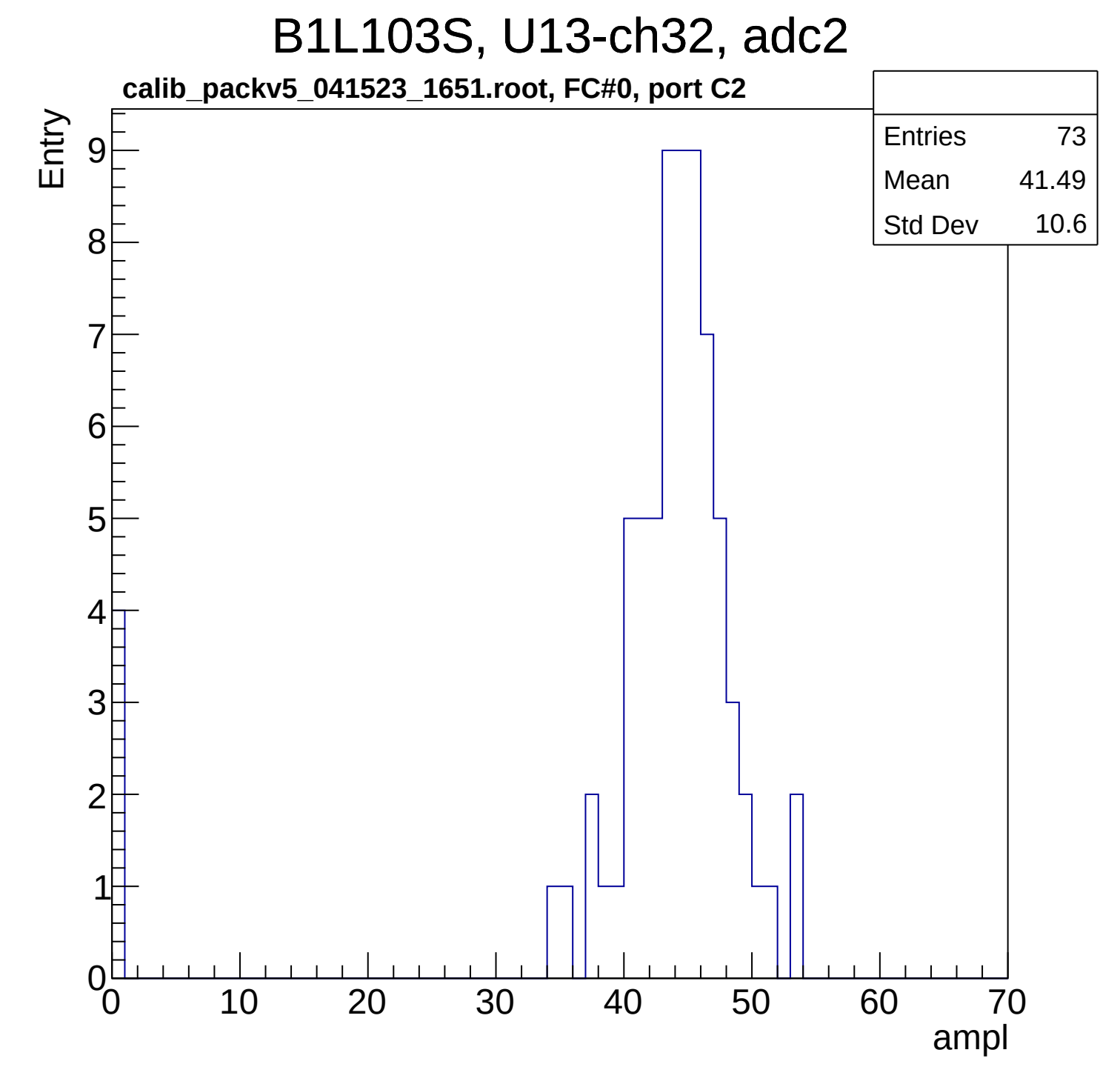
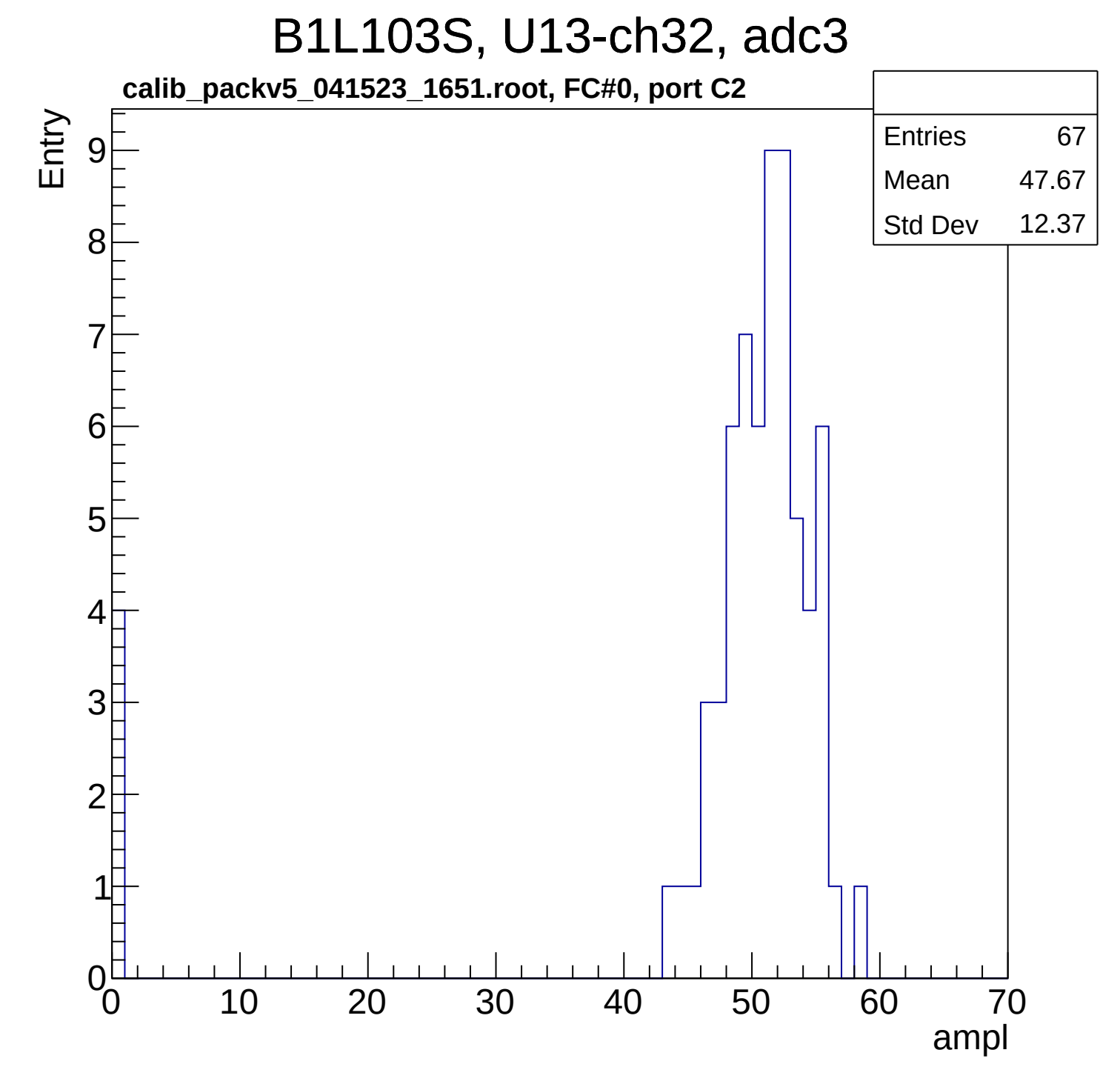

B1L103S, U13-ch31, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U13-ch31, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.333
Std Dev 5.497
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch32, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 24.23
Std Dev 12.45
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U13-ch32, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 36.78
Std Dev 3.579
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch32, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 41.49
Std Dev 10.6
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch32, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 47.67
Std Dev 12.37
Entry
ampl
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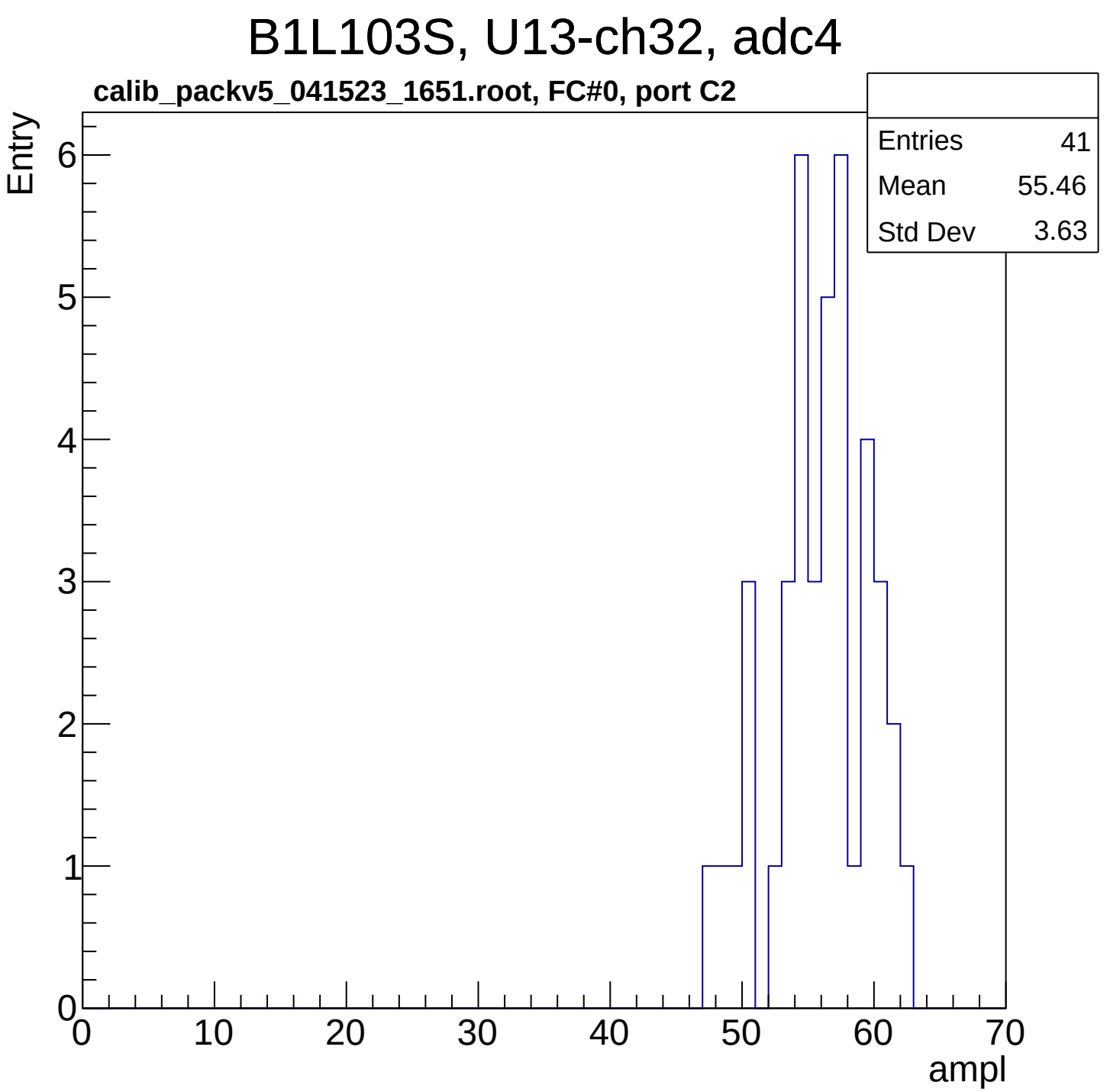
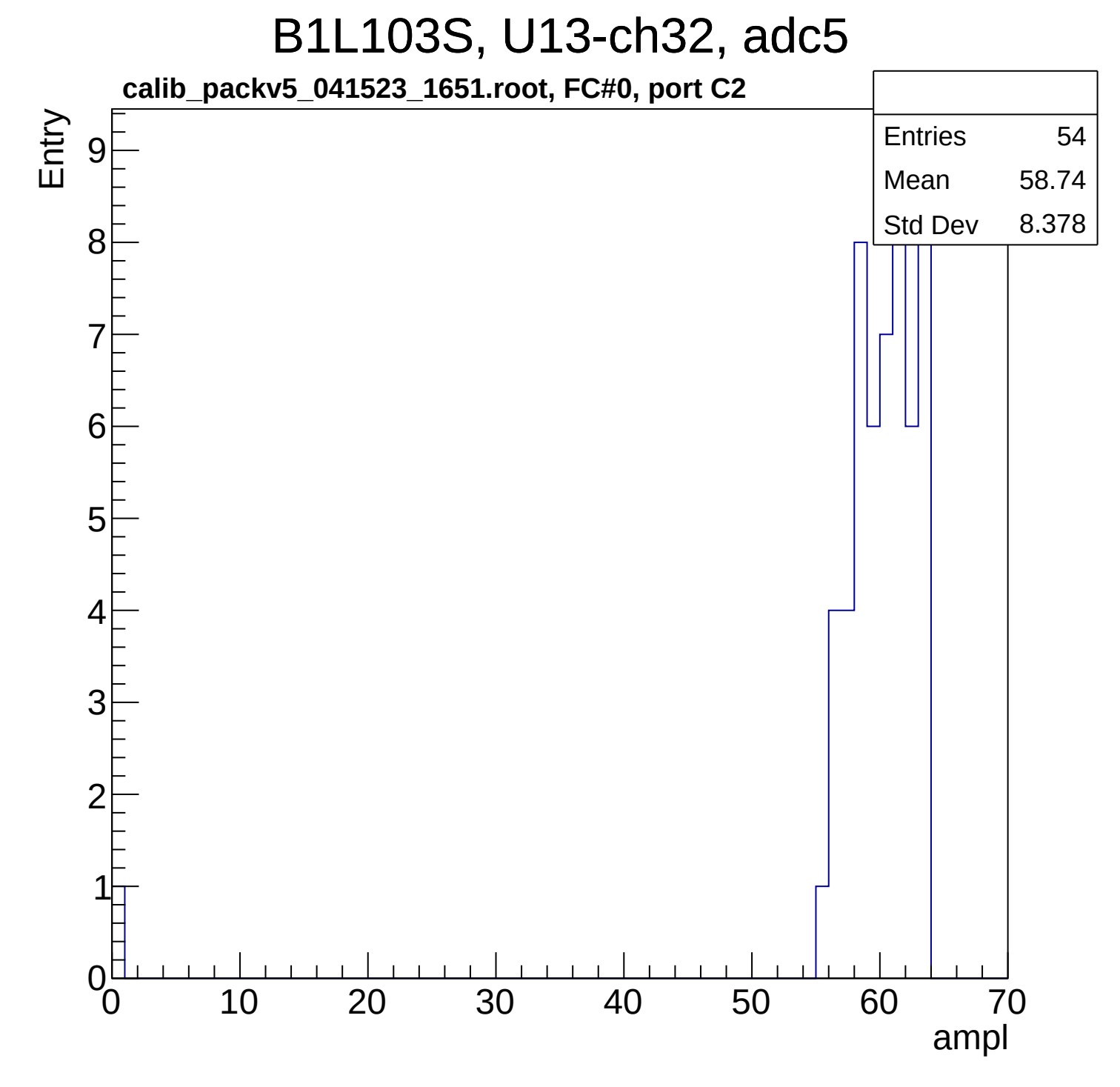
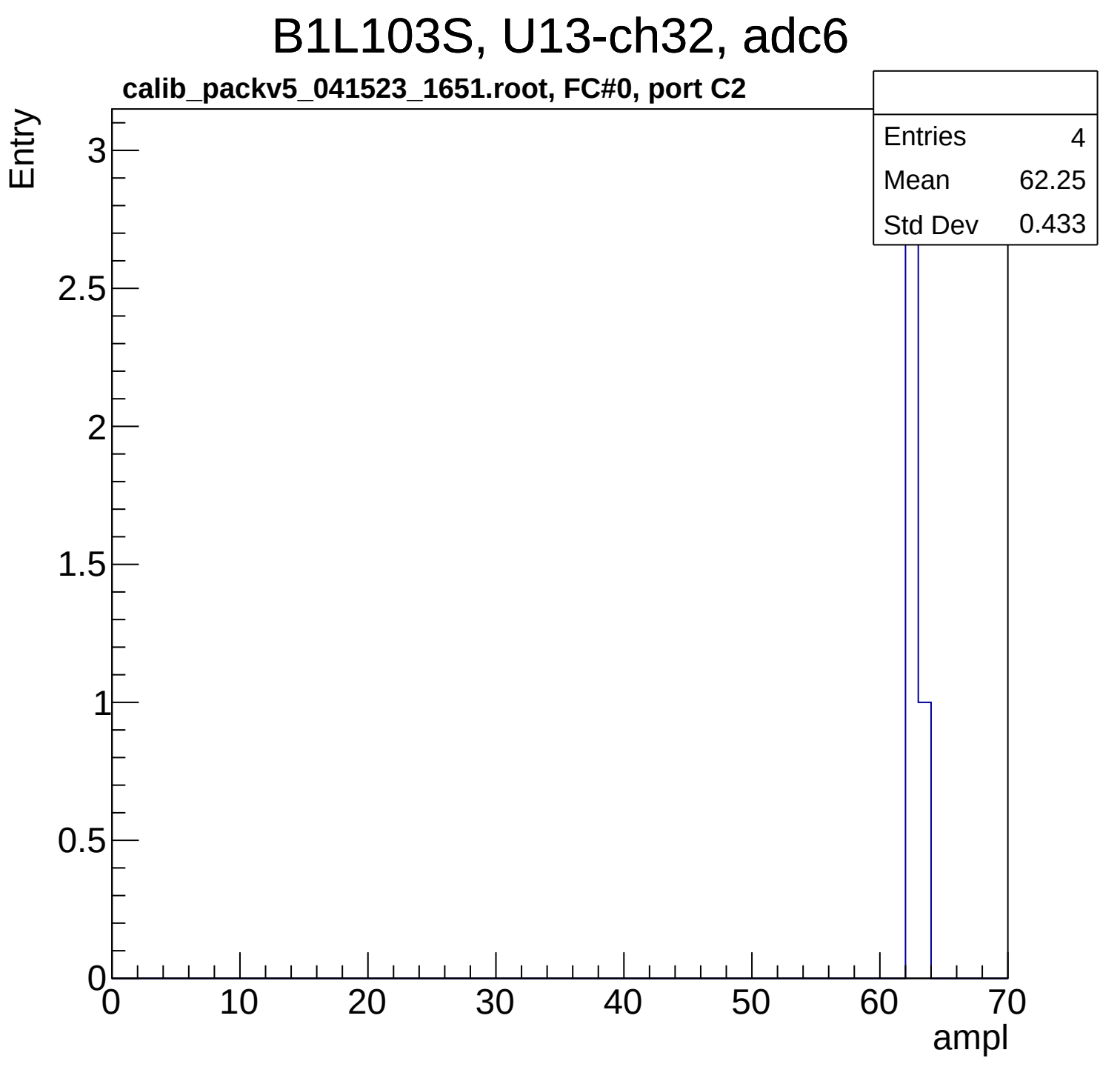
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch32, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 55.46
Std Dev 3.63
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch32, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.74
Std Dev 8.378
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch32, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.25
Std Dev 0.433
Entry
ampl
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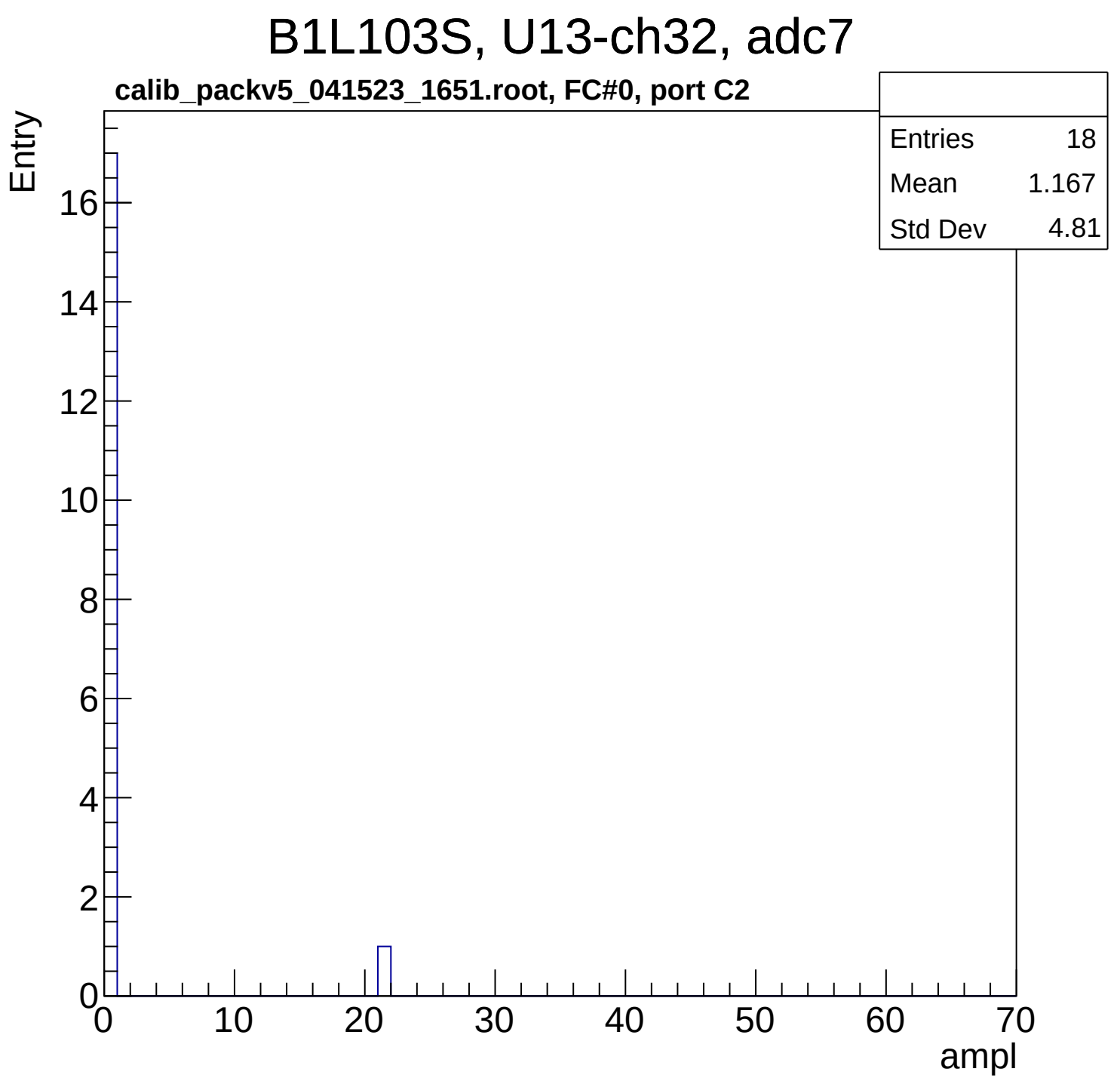
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U13-ch32, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.167
Std Dev 4.81
Entry
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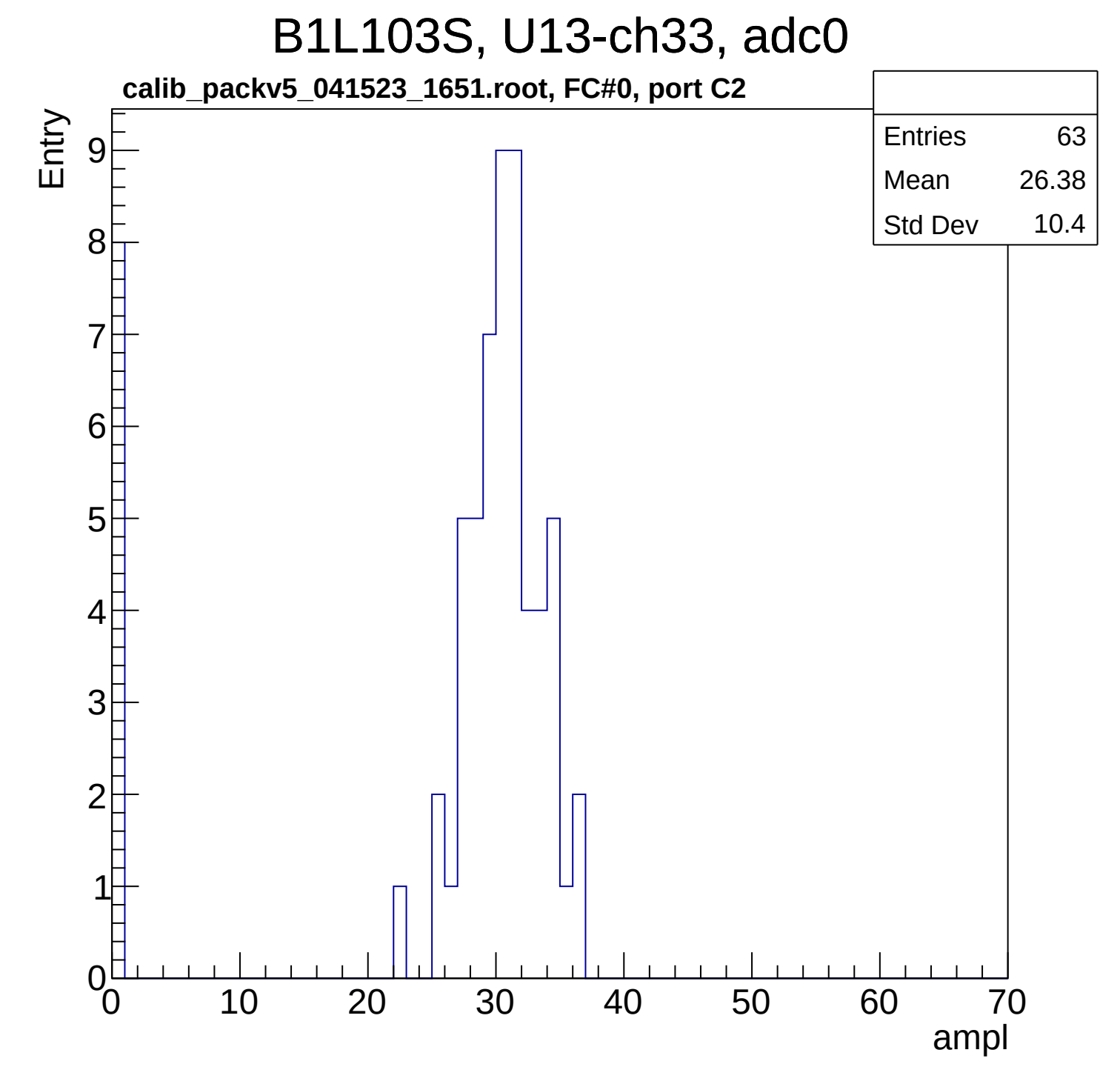
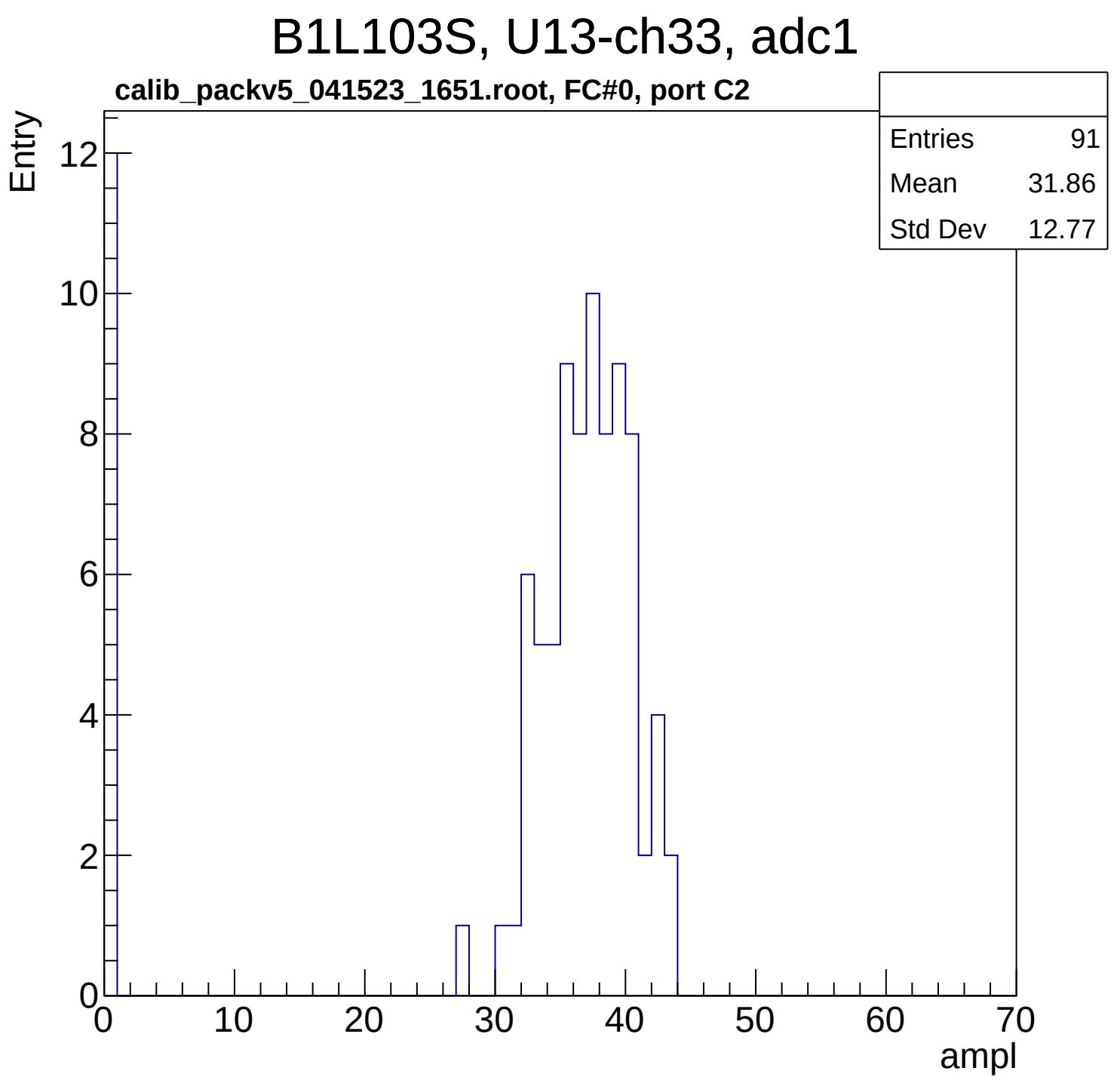
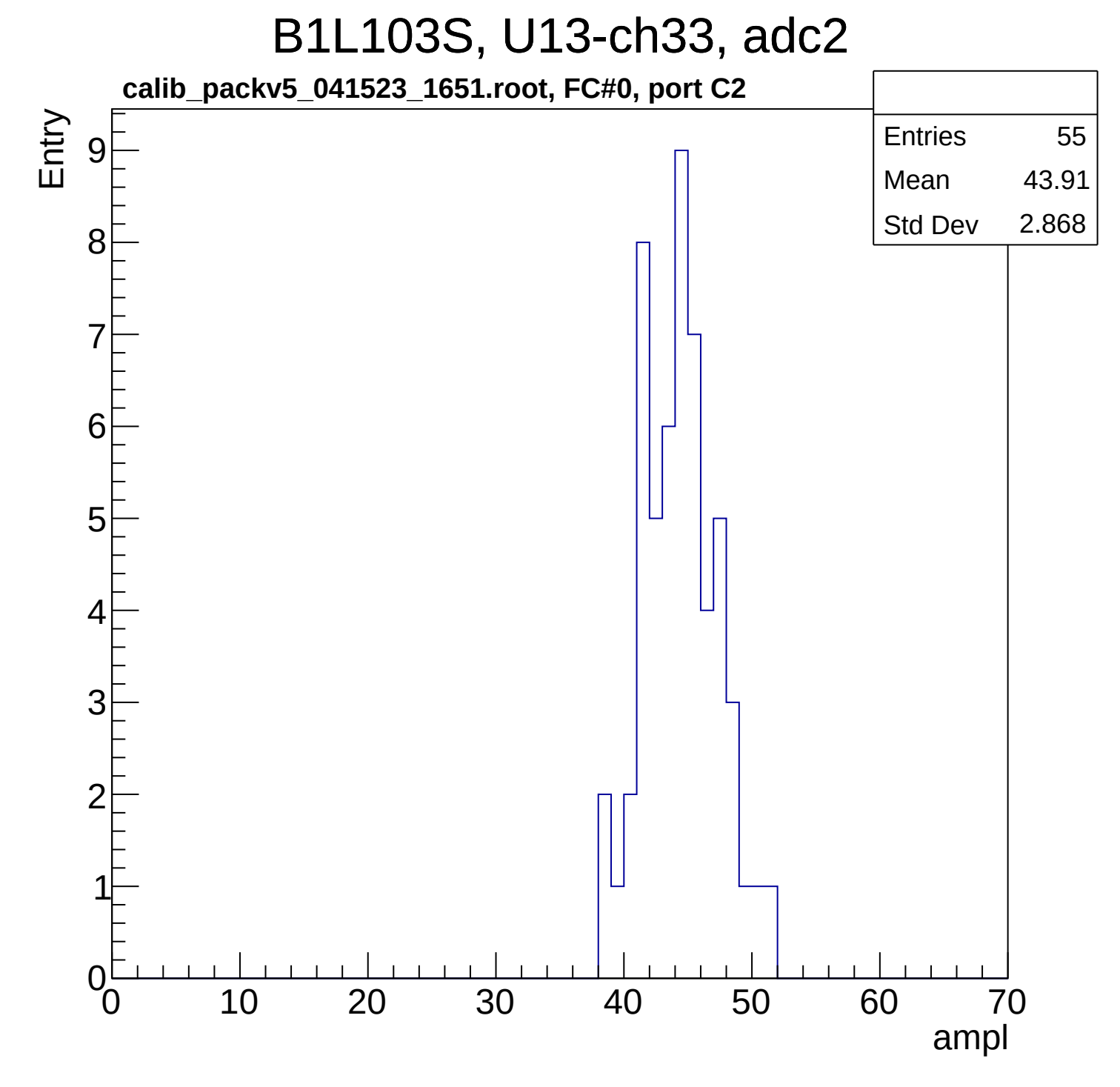
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch33, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 26.38
Std Dev 10.4
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch33, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 31.86
Std Dev 12.77
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch33, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 43.91
Std Dev 2.868
Entry
ampl
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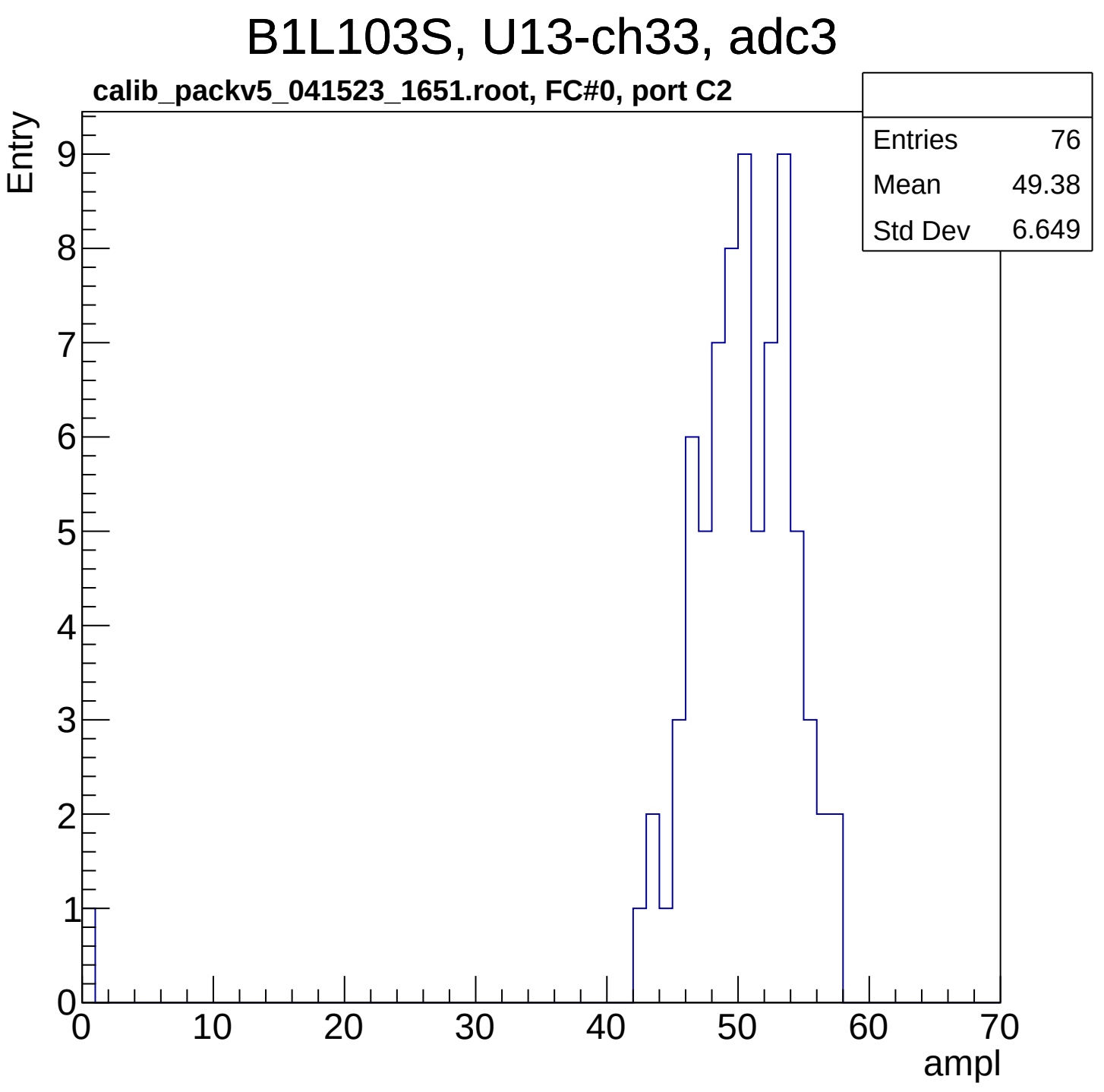
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch33, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 49.38
Std Dev 6.649
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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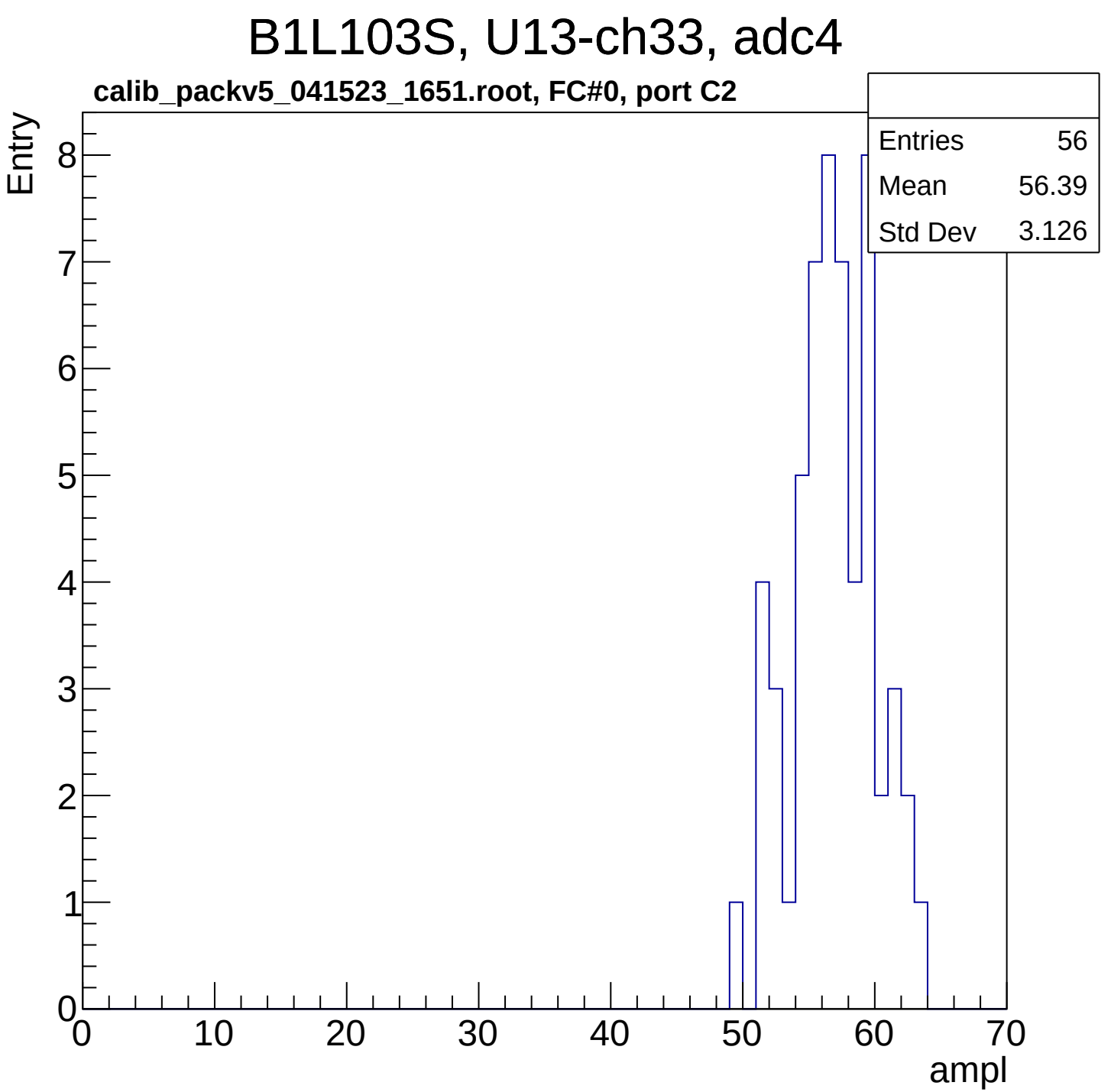
40
50
60
70


B1L103S, U13-ch33, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 56.39
Std Dev 3.126
Entry
ampl
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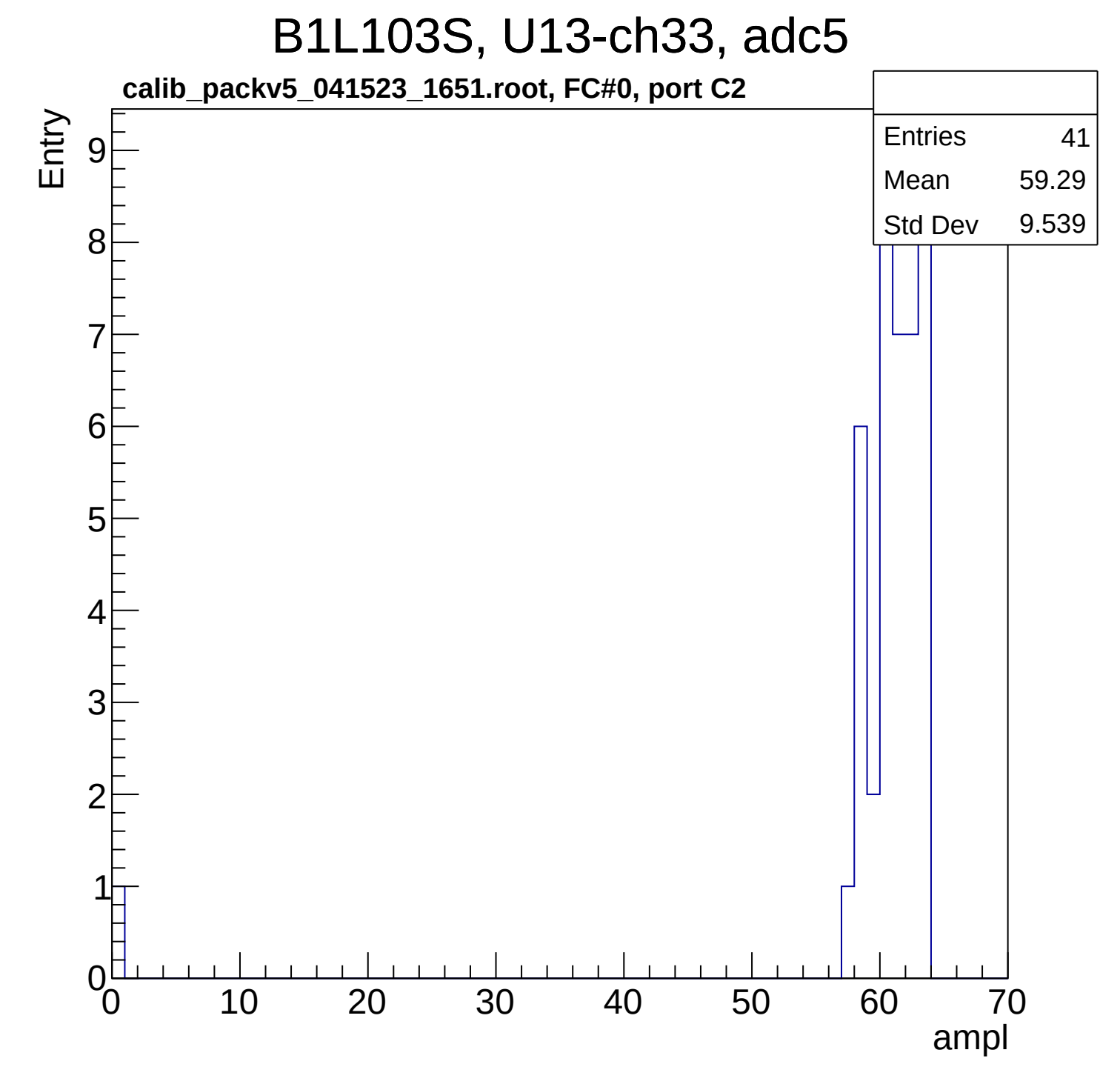
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch33, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 59.29
Std Dev 9.539
Entry
ampl
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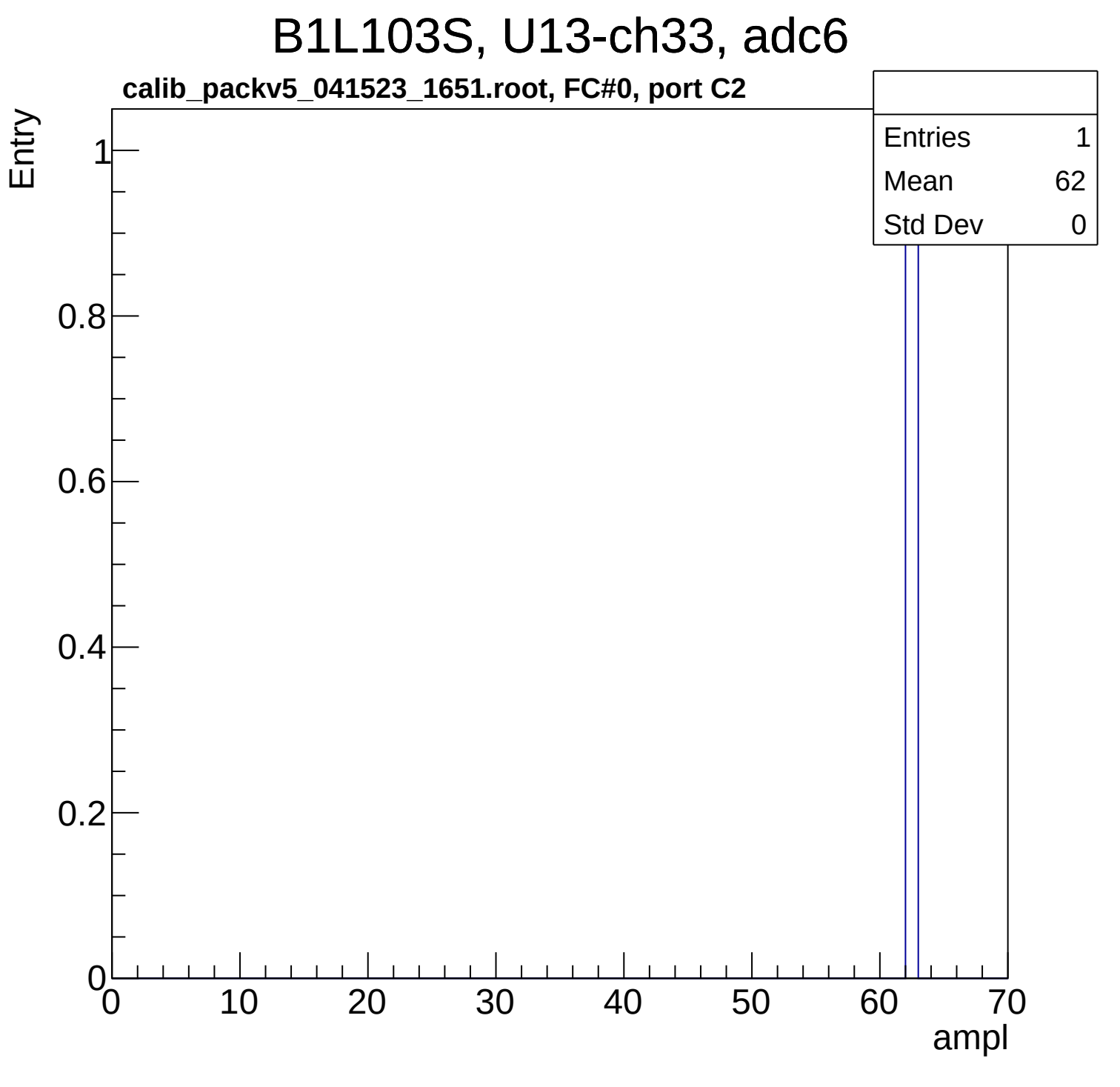
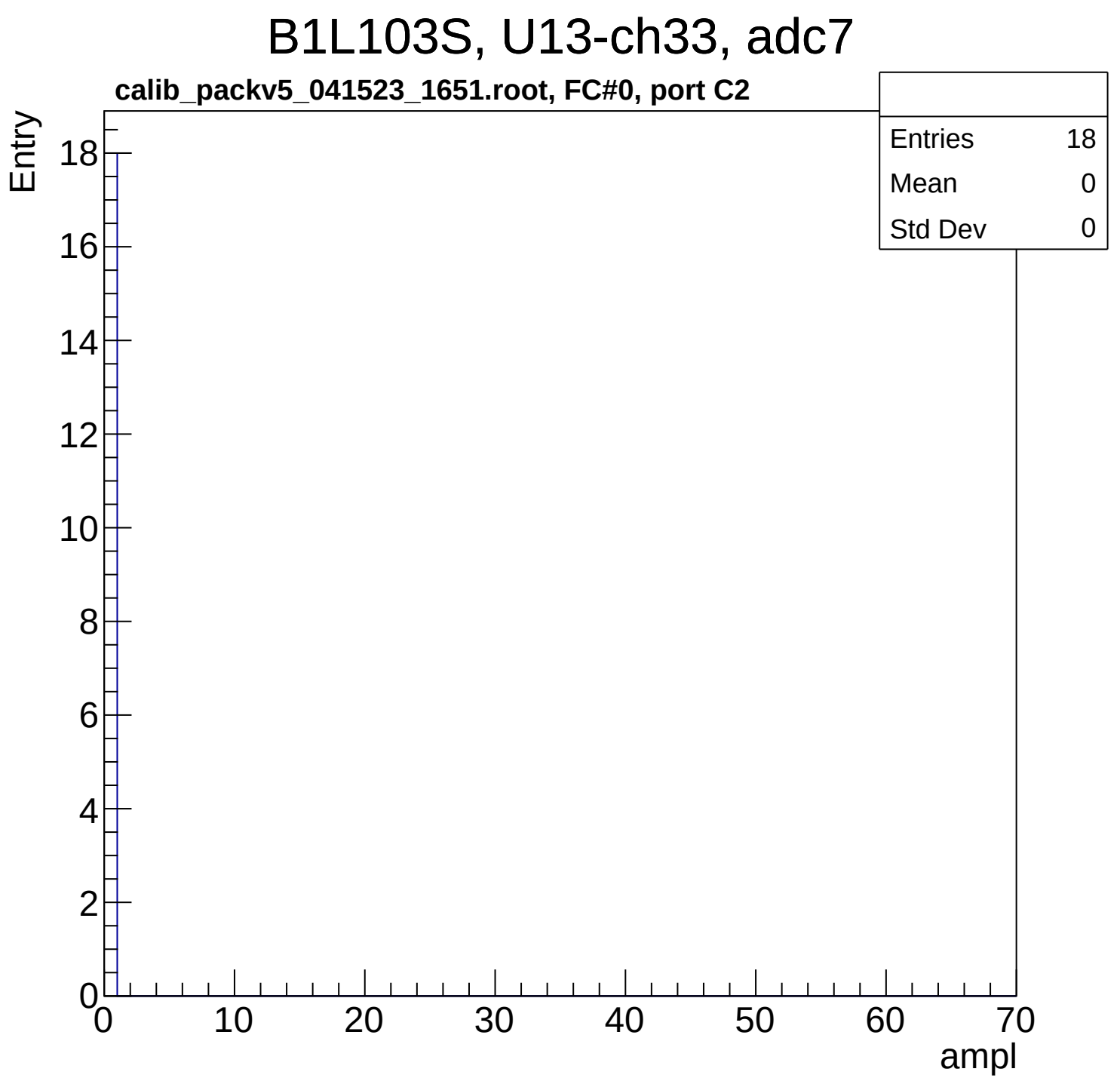
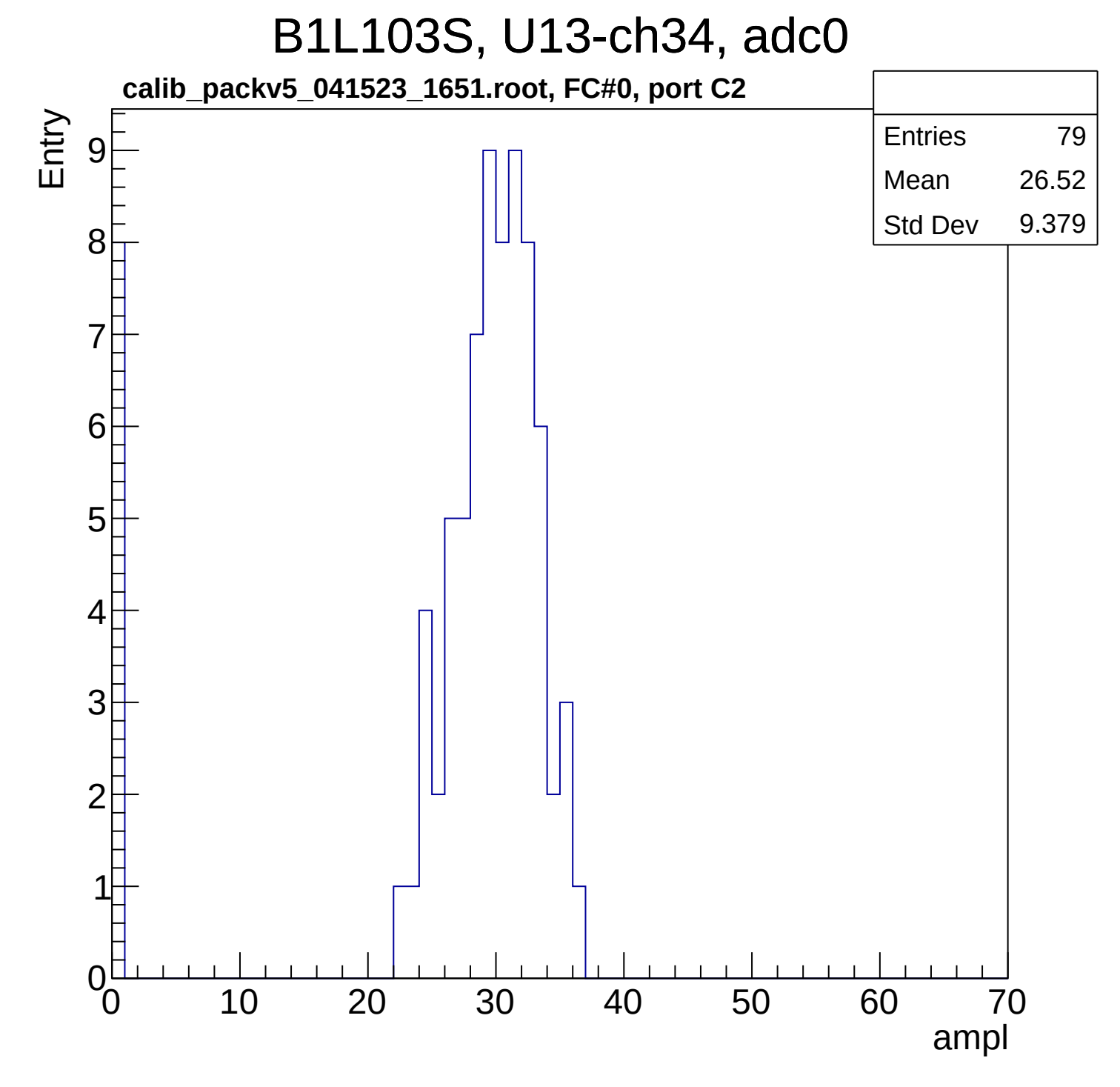
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch33, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch33, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch34, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 26.52
Std Dev 9.379
Entry
ampl
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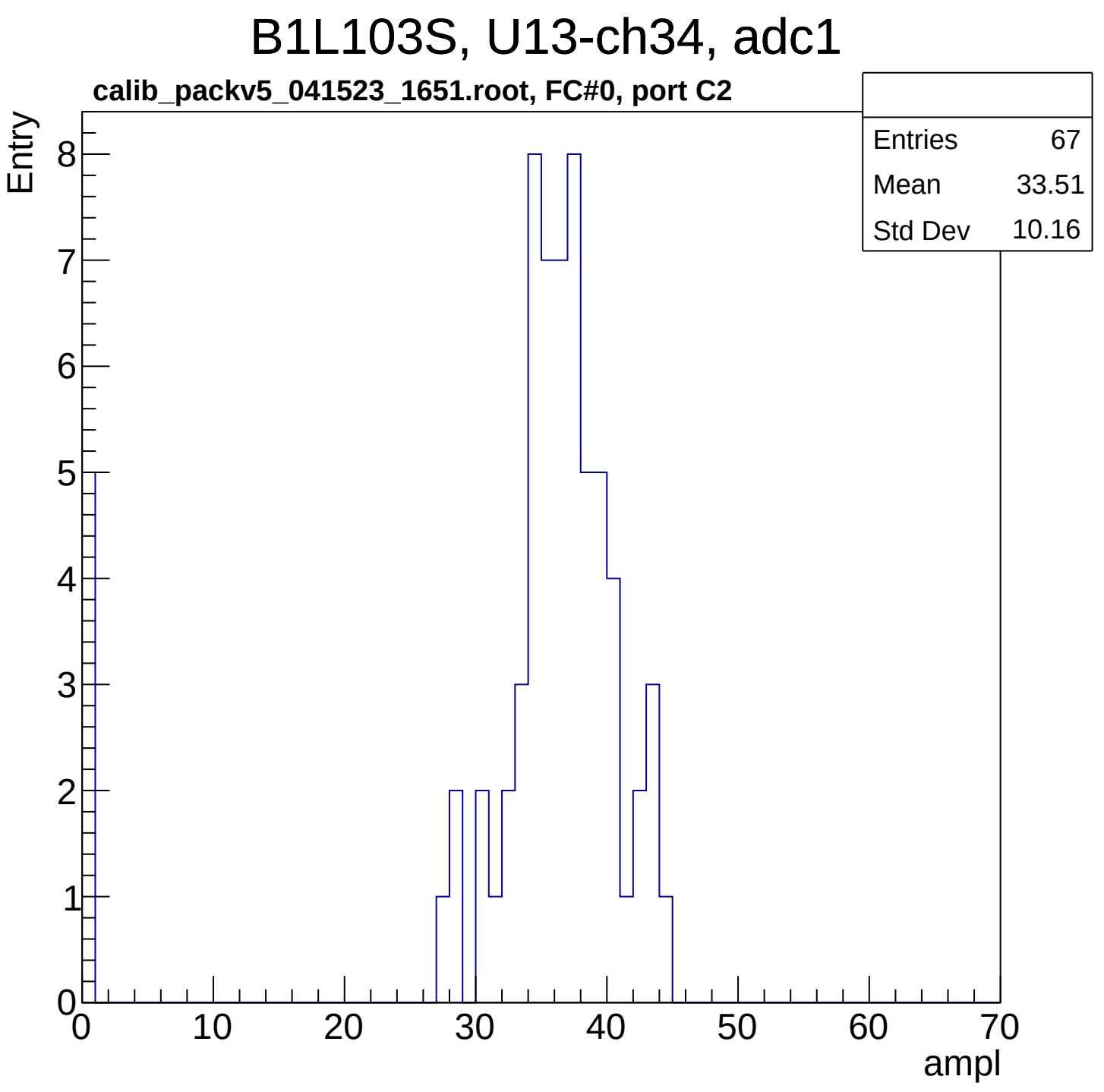
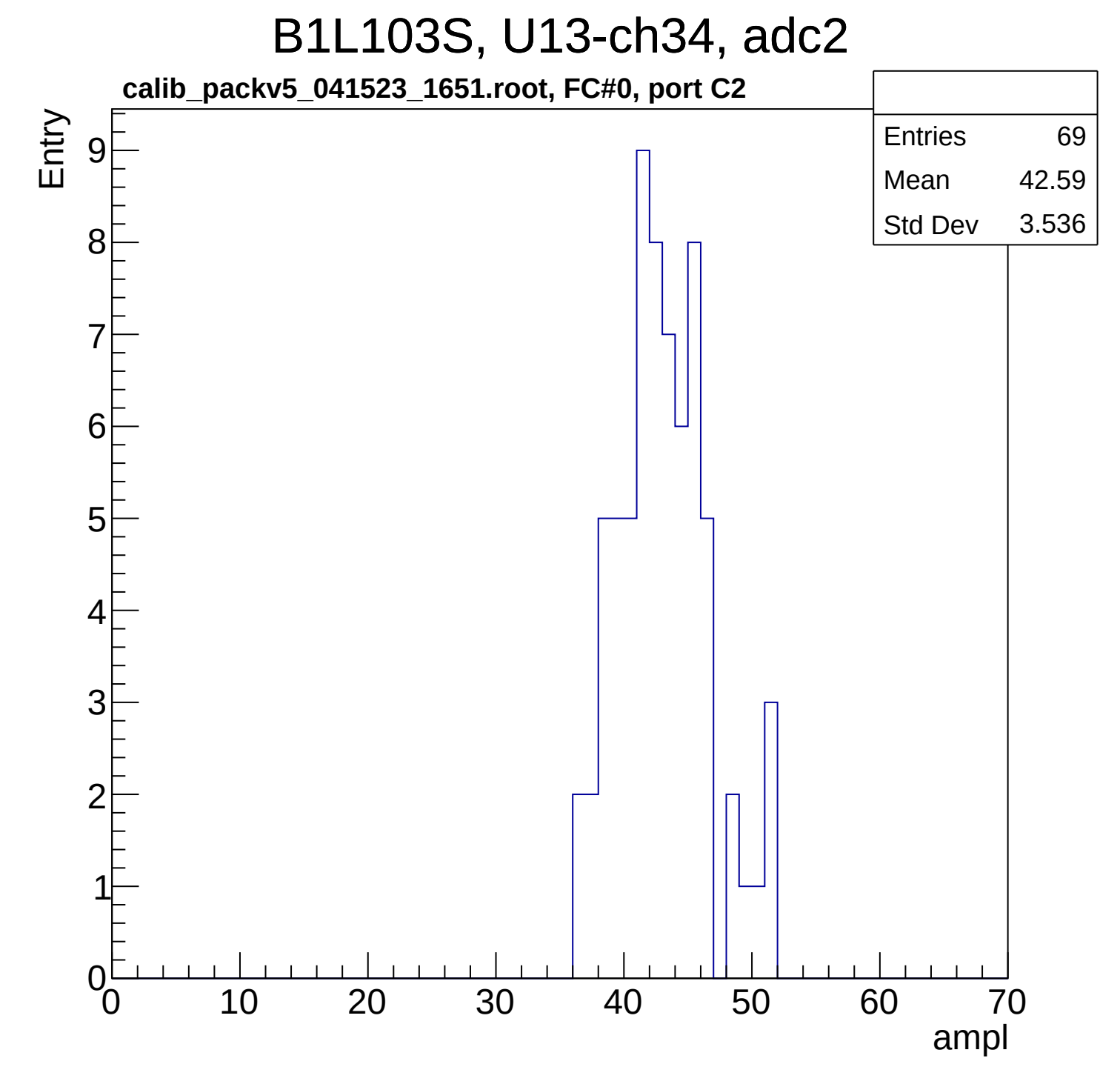
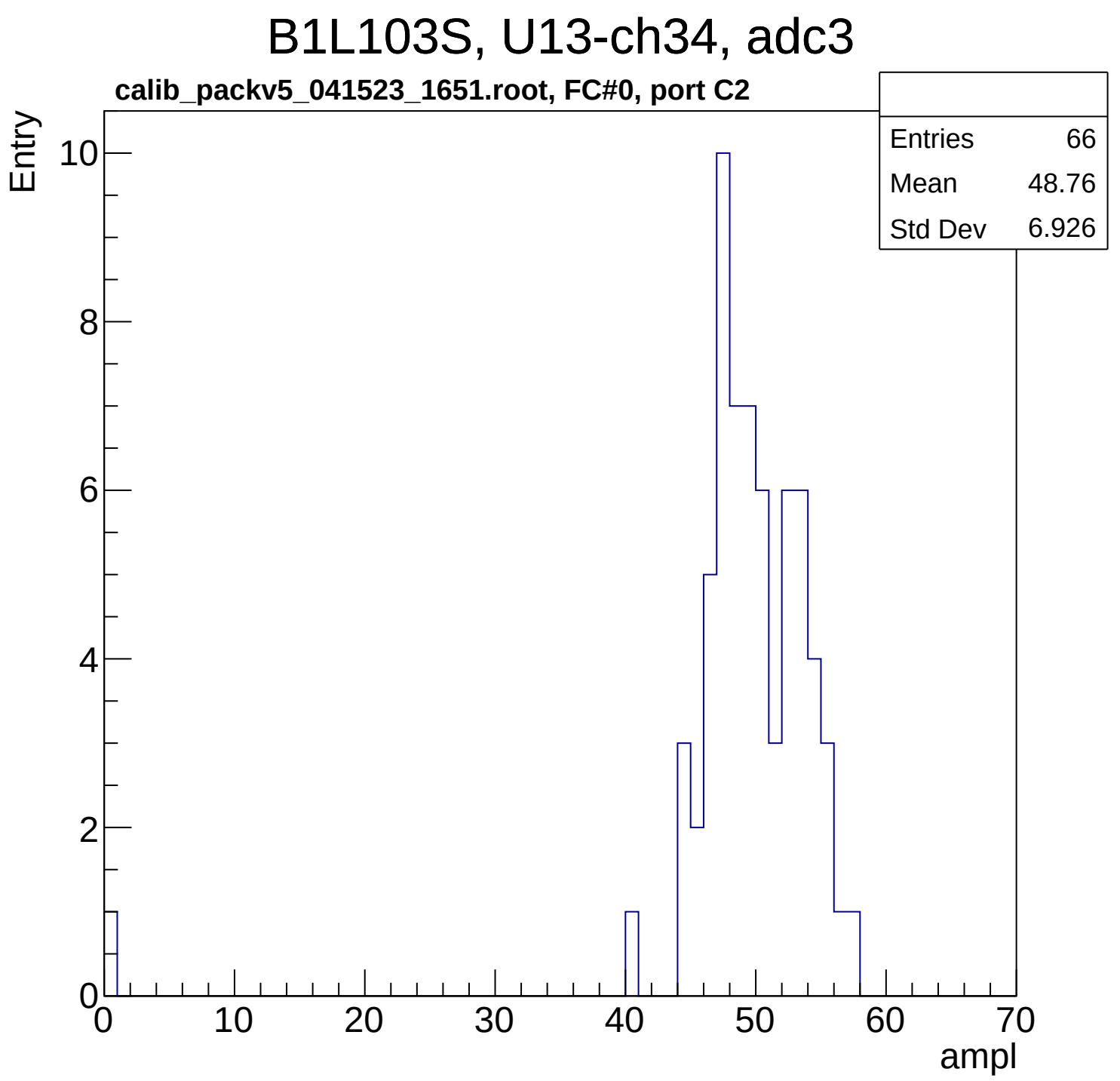
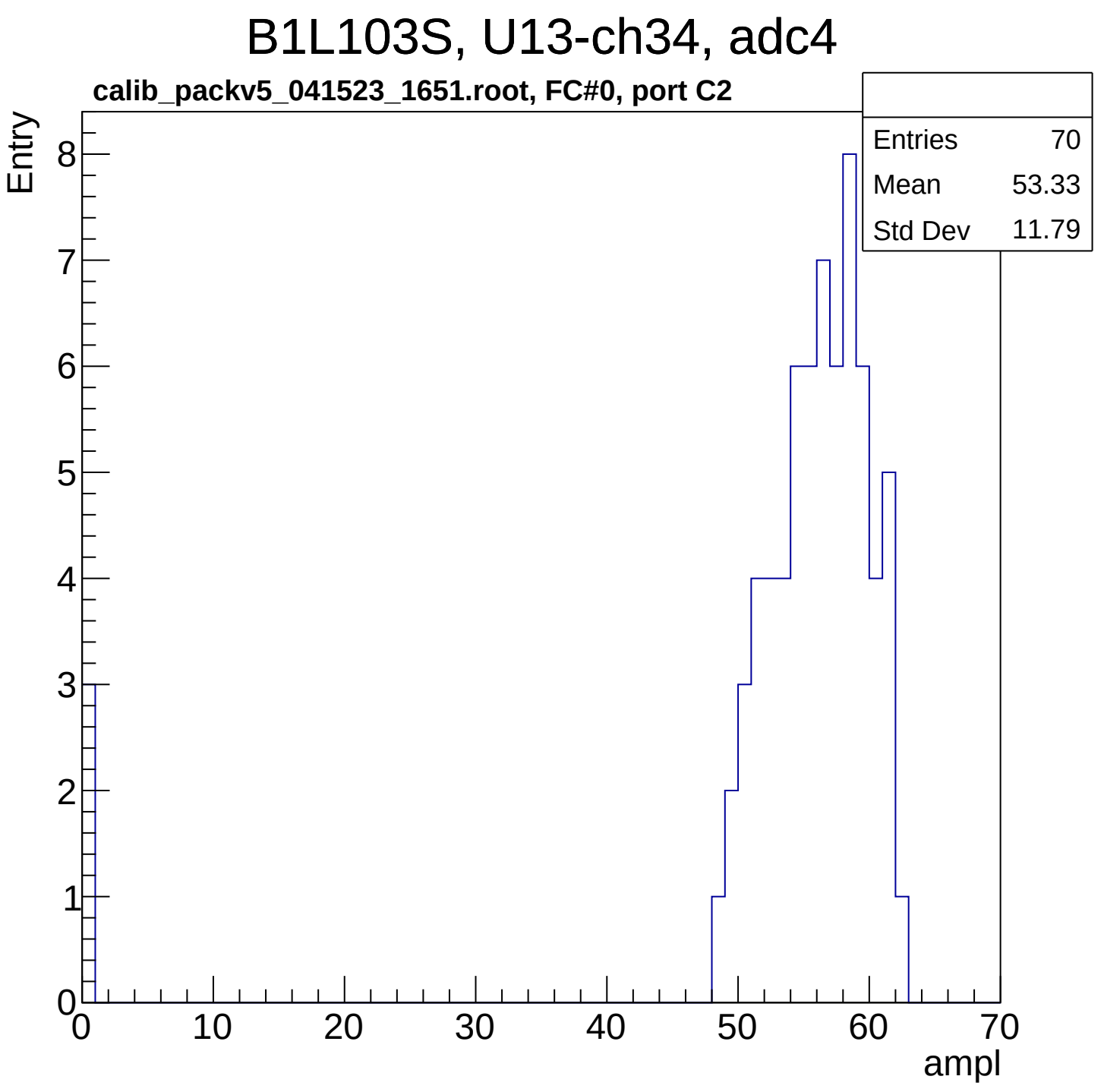
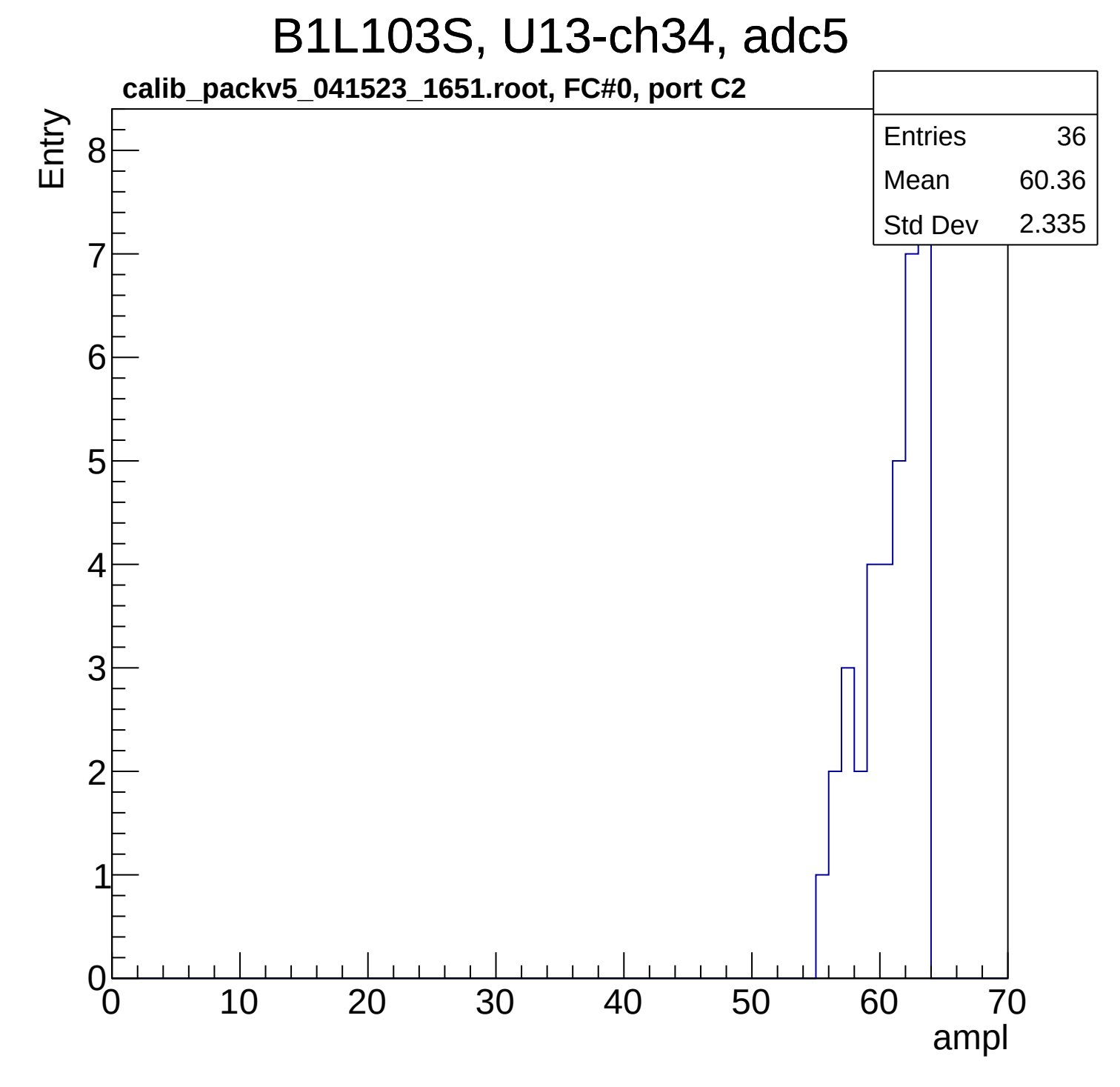
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch34, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 33.51
Std Dev 10.16
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch34, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 42.59
Std Dev 3.536
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch34, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 48.76
Std Dev 6.926
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch34, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 53.33
Std Dev 11.79
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch34, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 60.36
Std Dev 2.335
Entry
ampl
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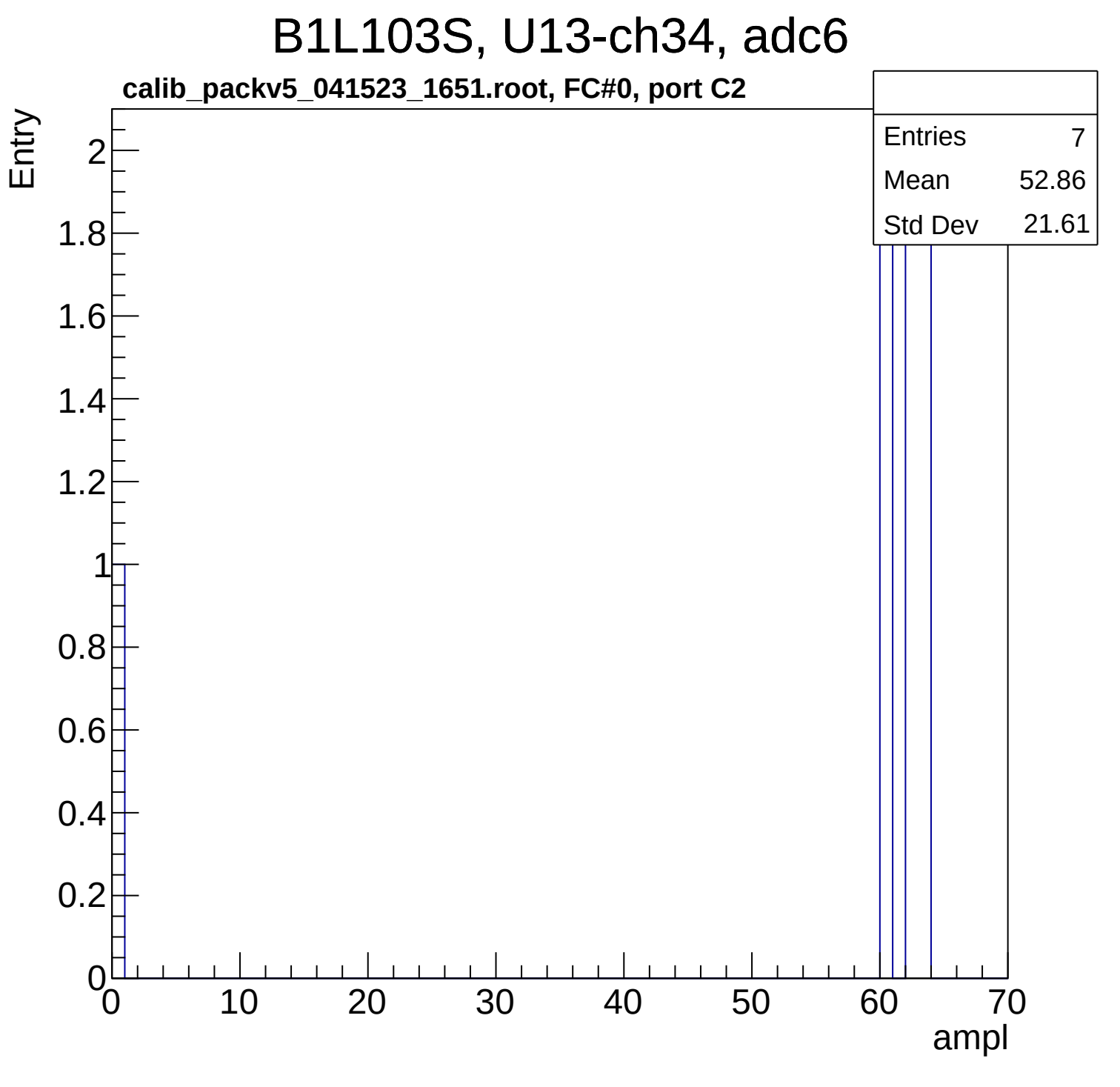
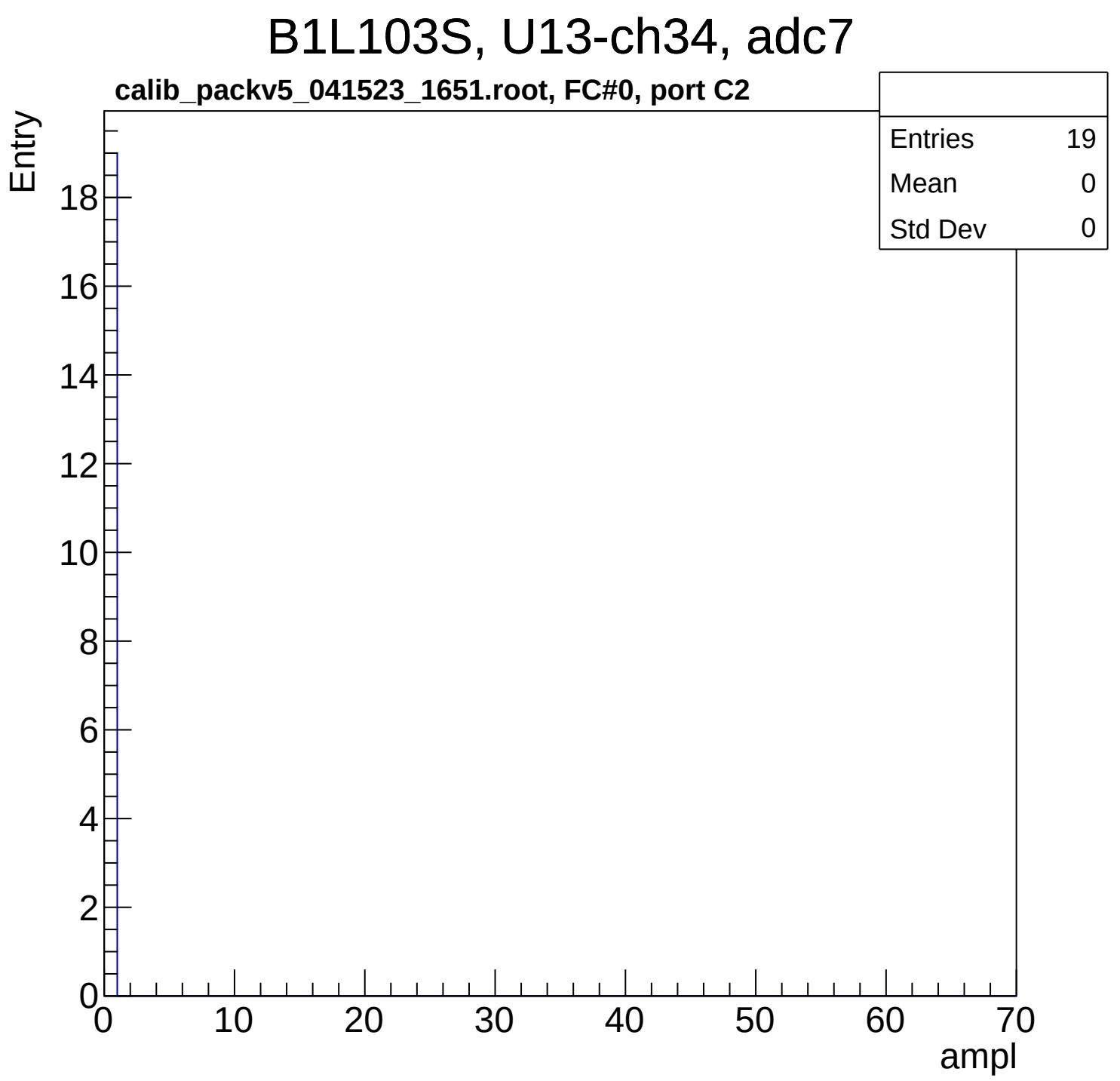
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch34, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 52.86
Std Dev 21.61
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U13-ch34, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
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6
8
10
12
14
16
18
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10
20
30
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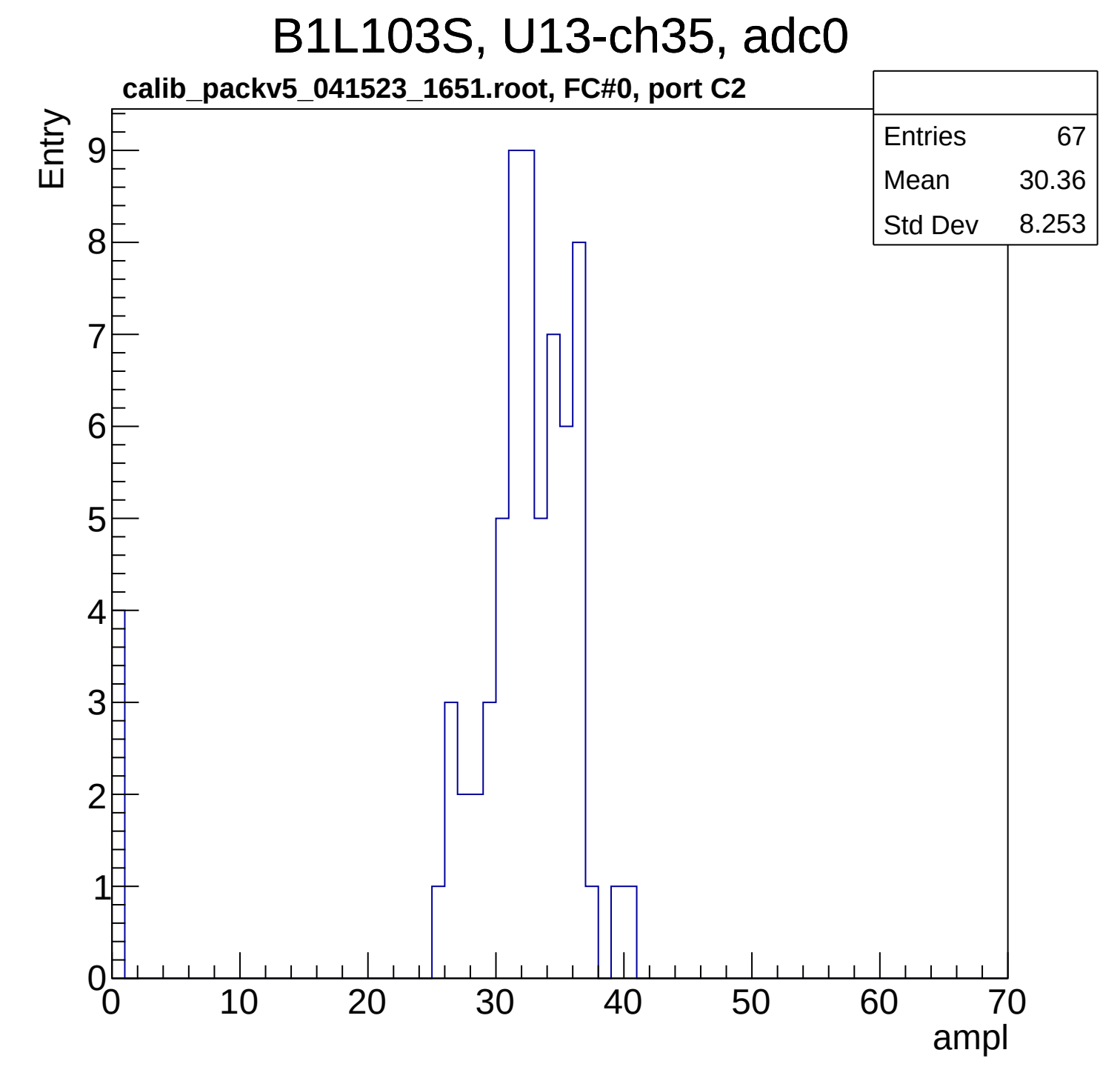
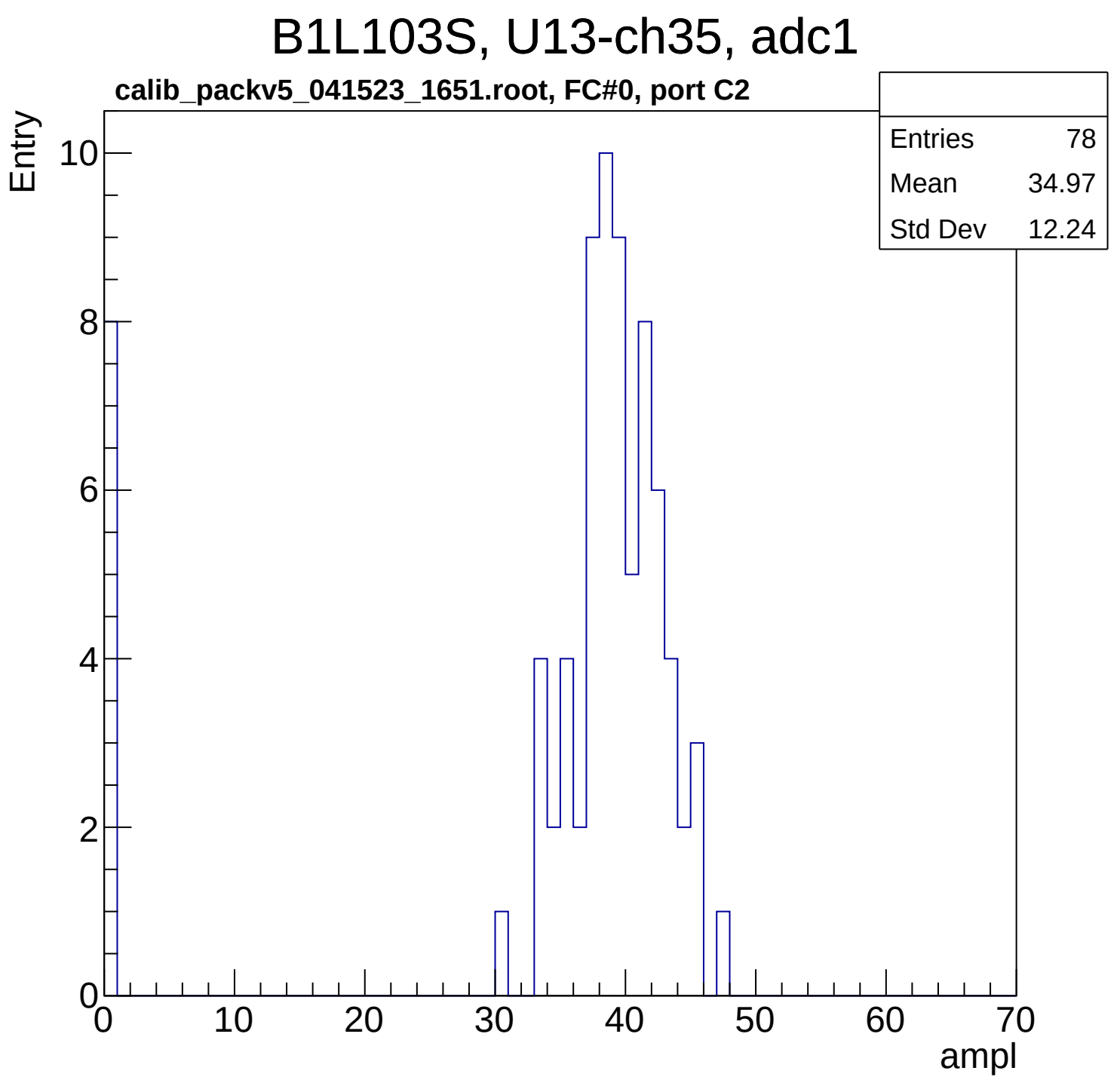
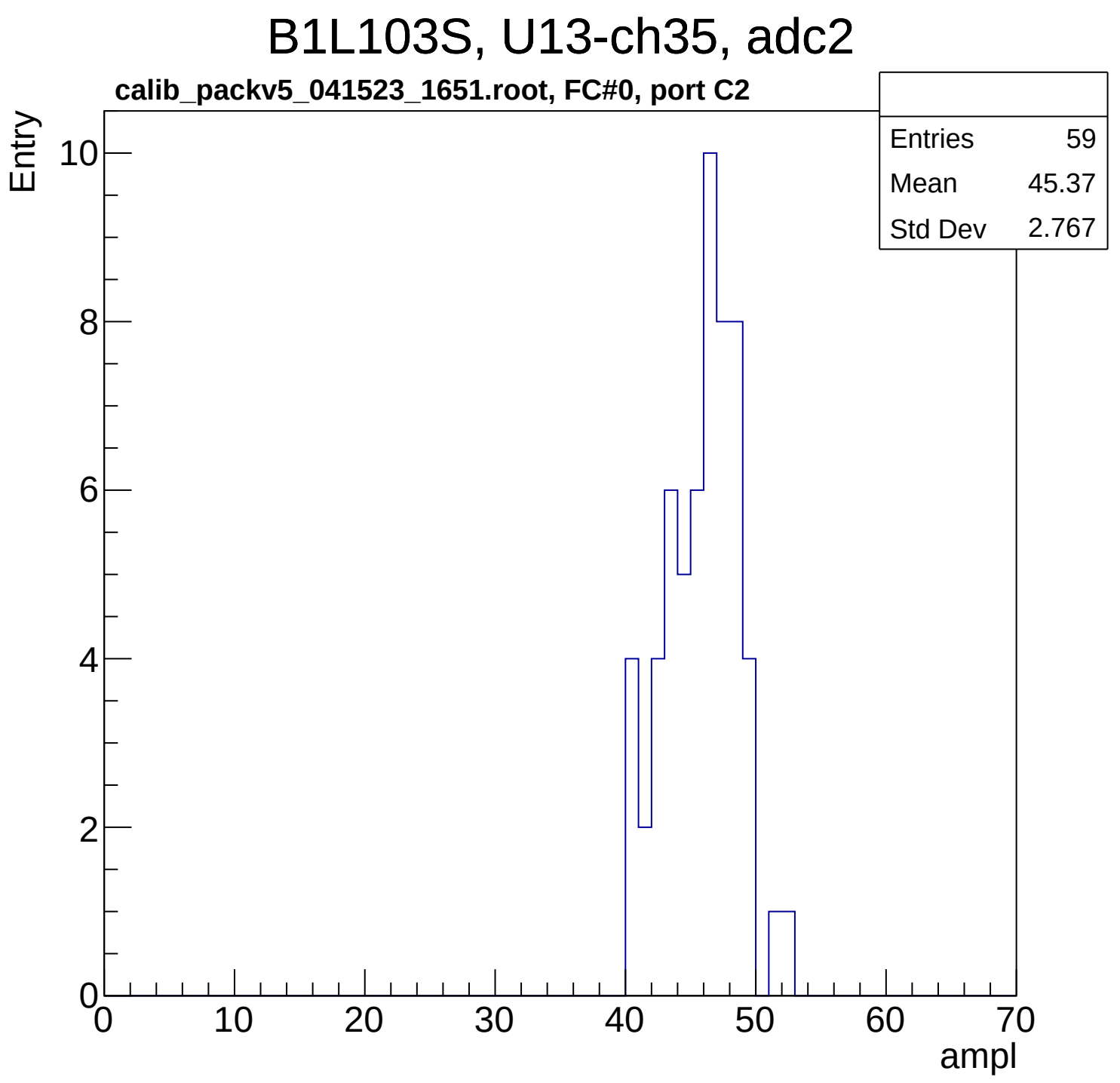
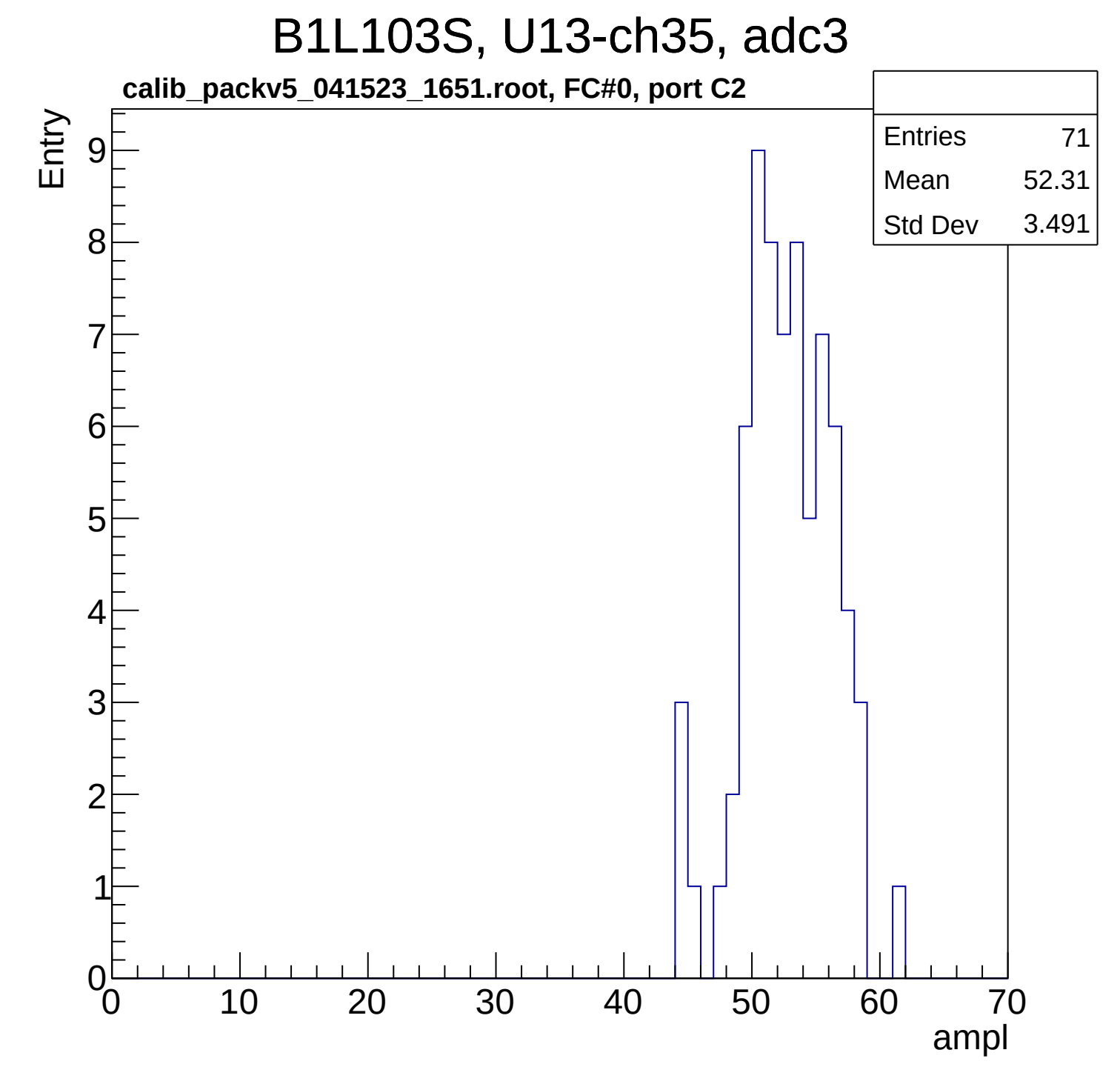
50
60
70
ampl


B1L103S, U13-ch35, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 30.36
Std Dev 8.253
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch35, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 34.97
Std Dev 12.24
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch35, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 45.37
Std Dev 2.767
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch35, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 52.31
Std Dev 3.491
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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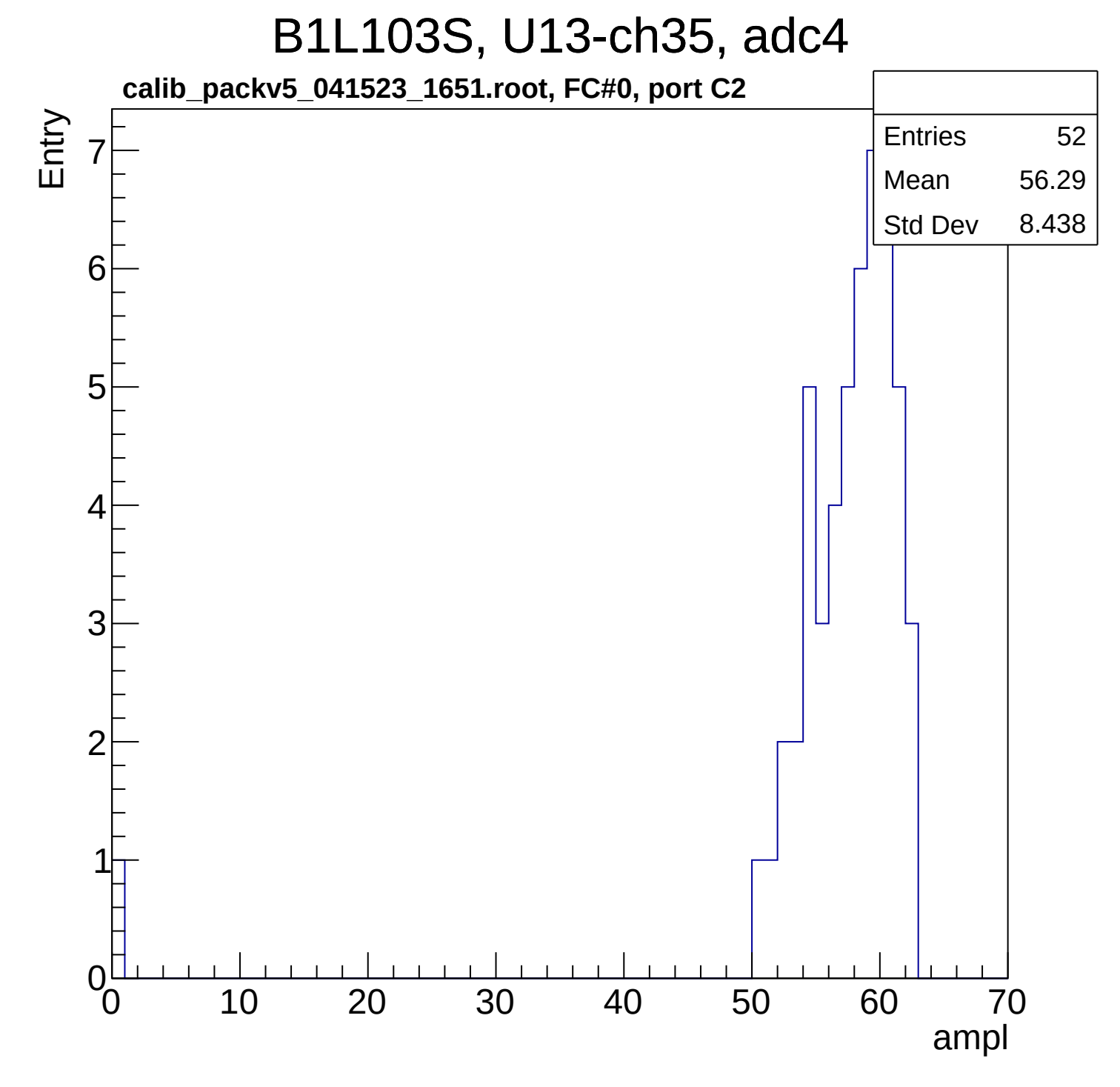
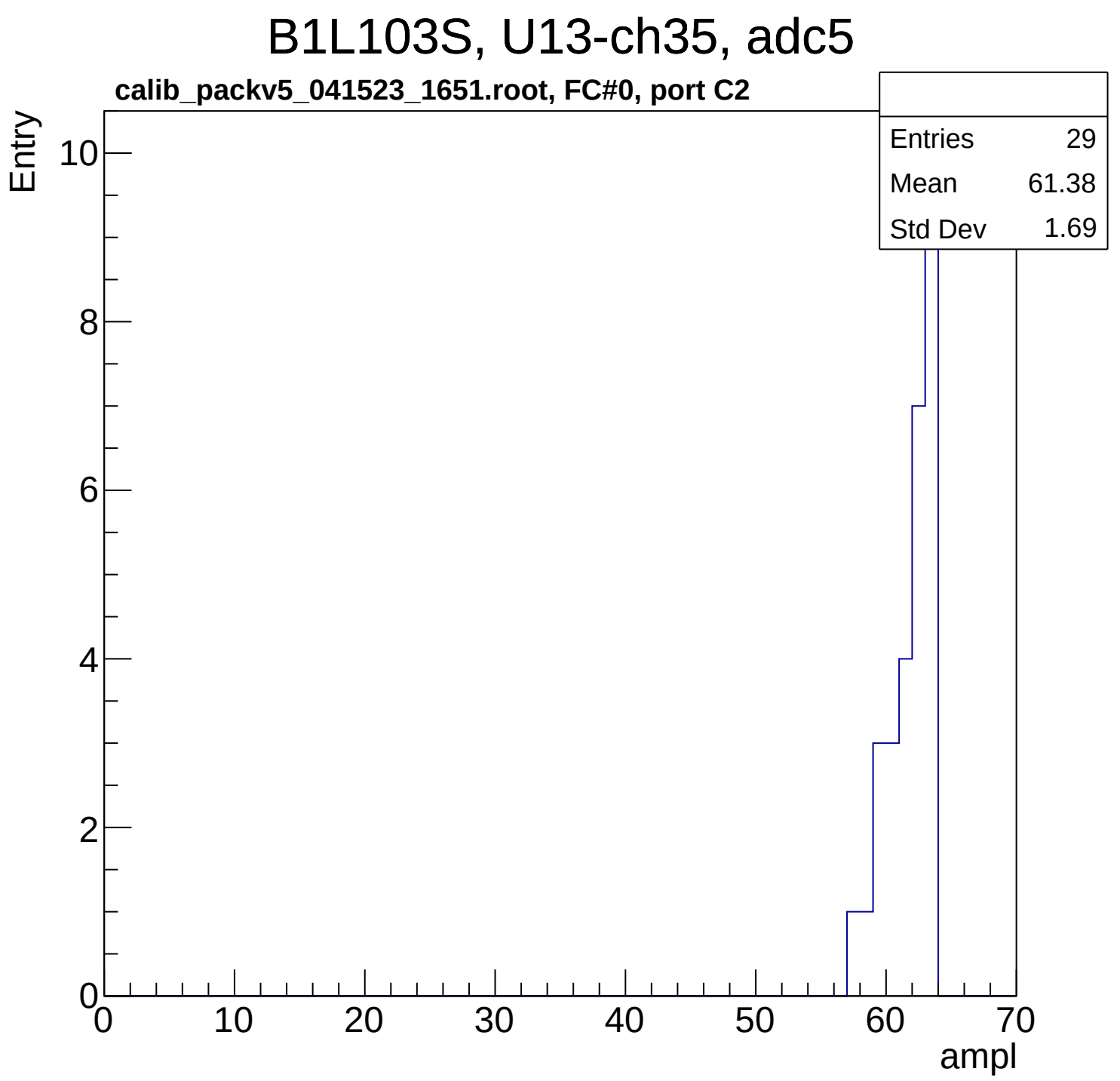
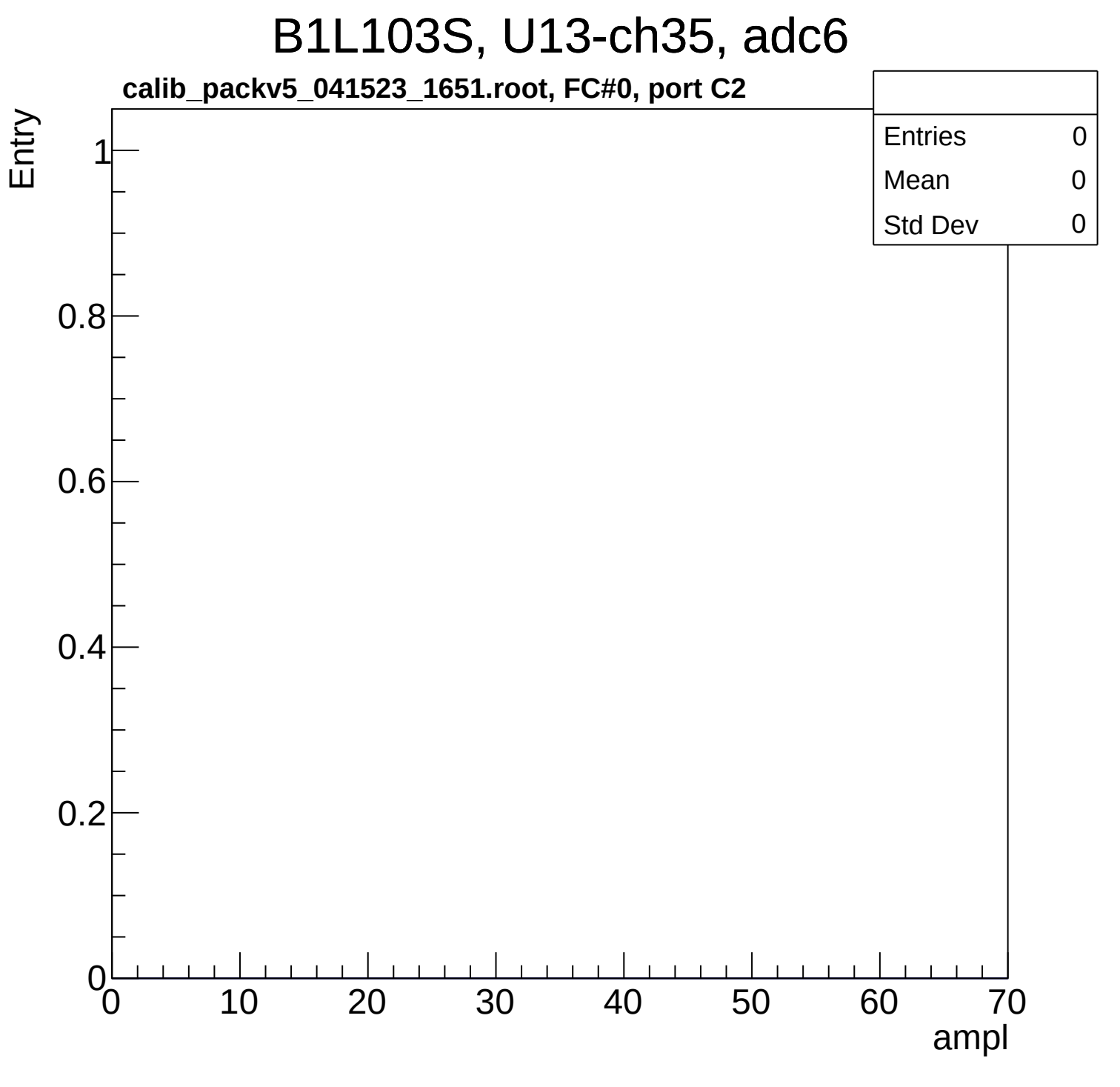
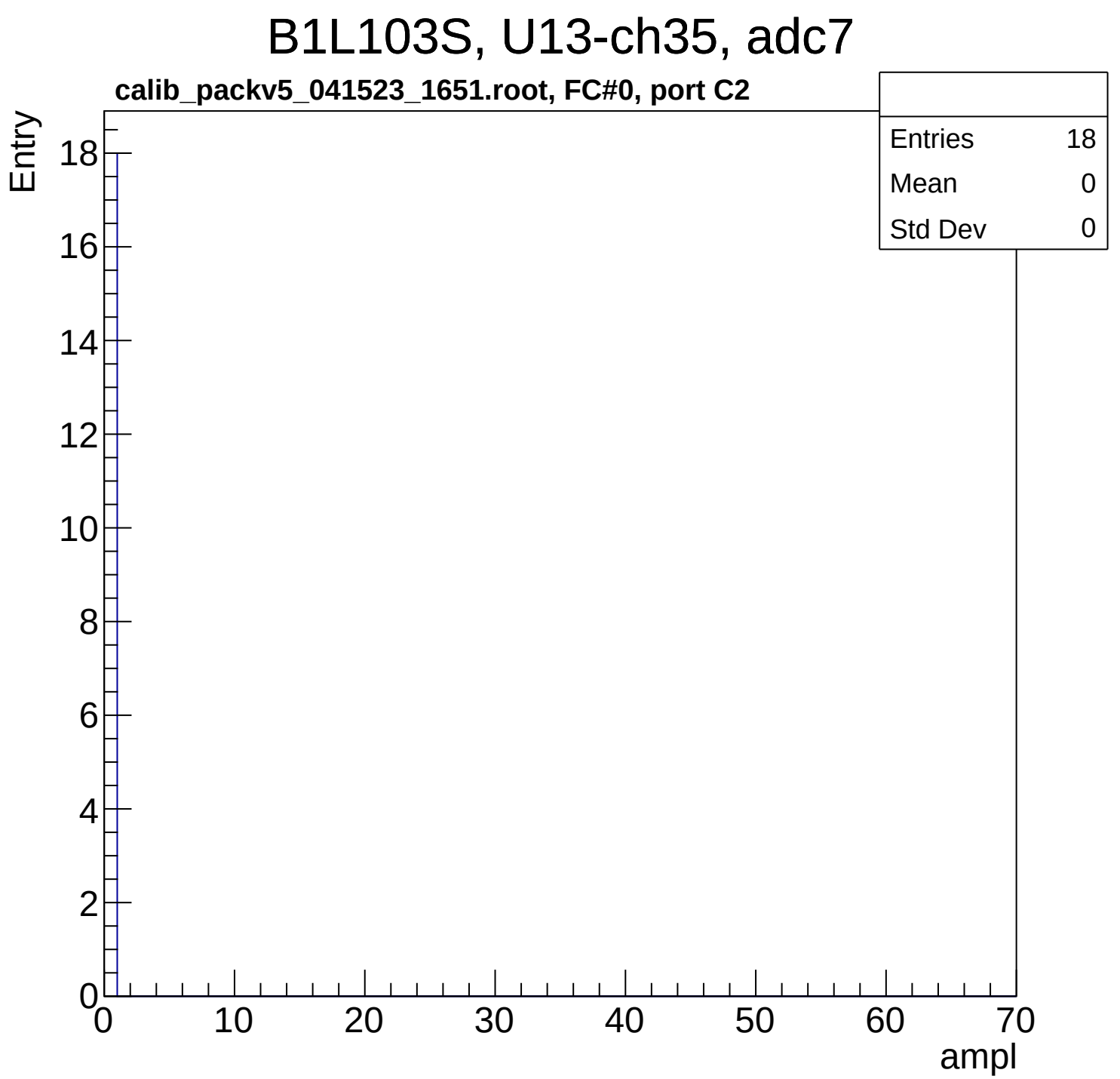
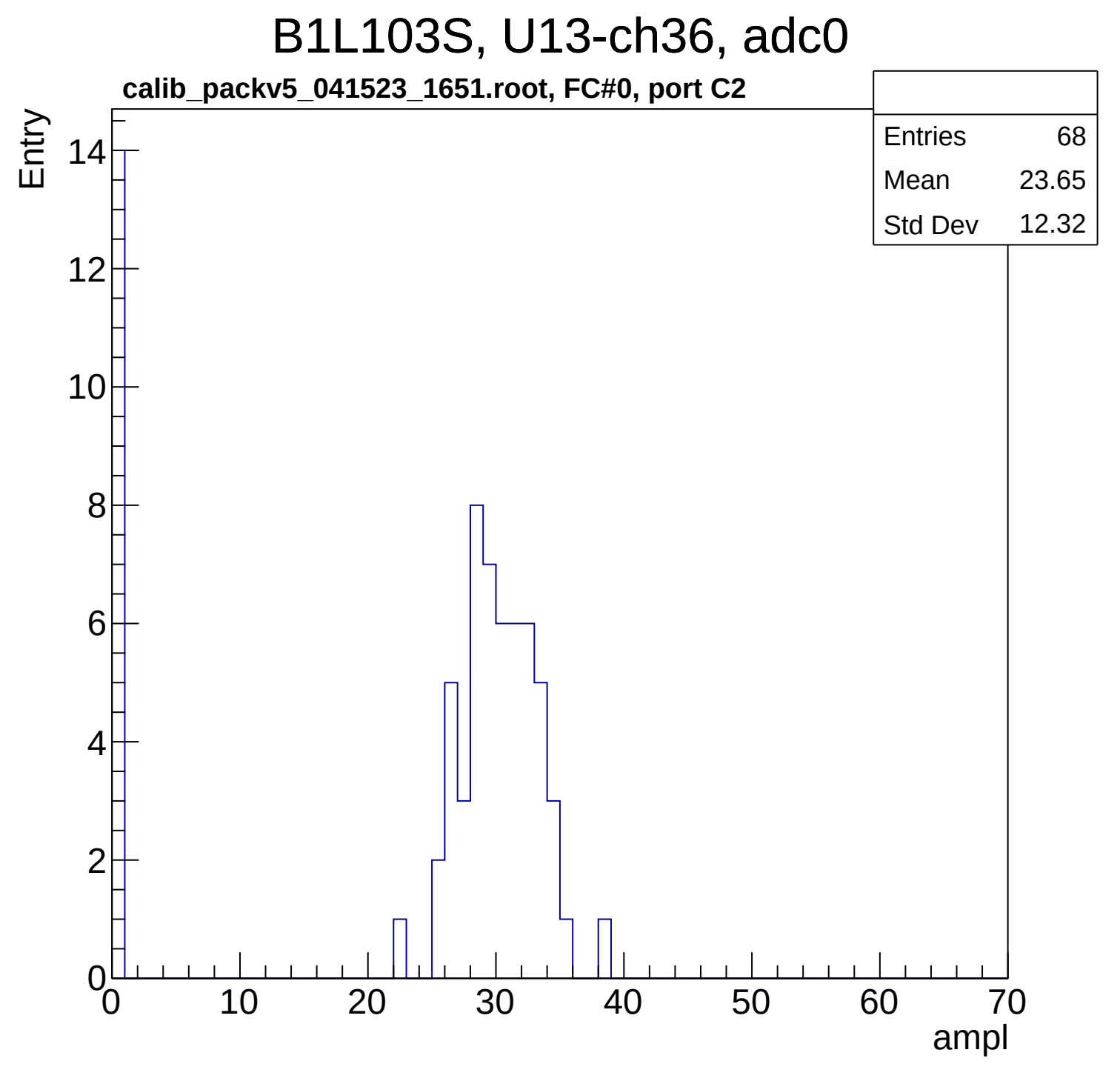
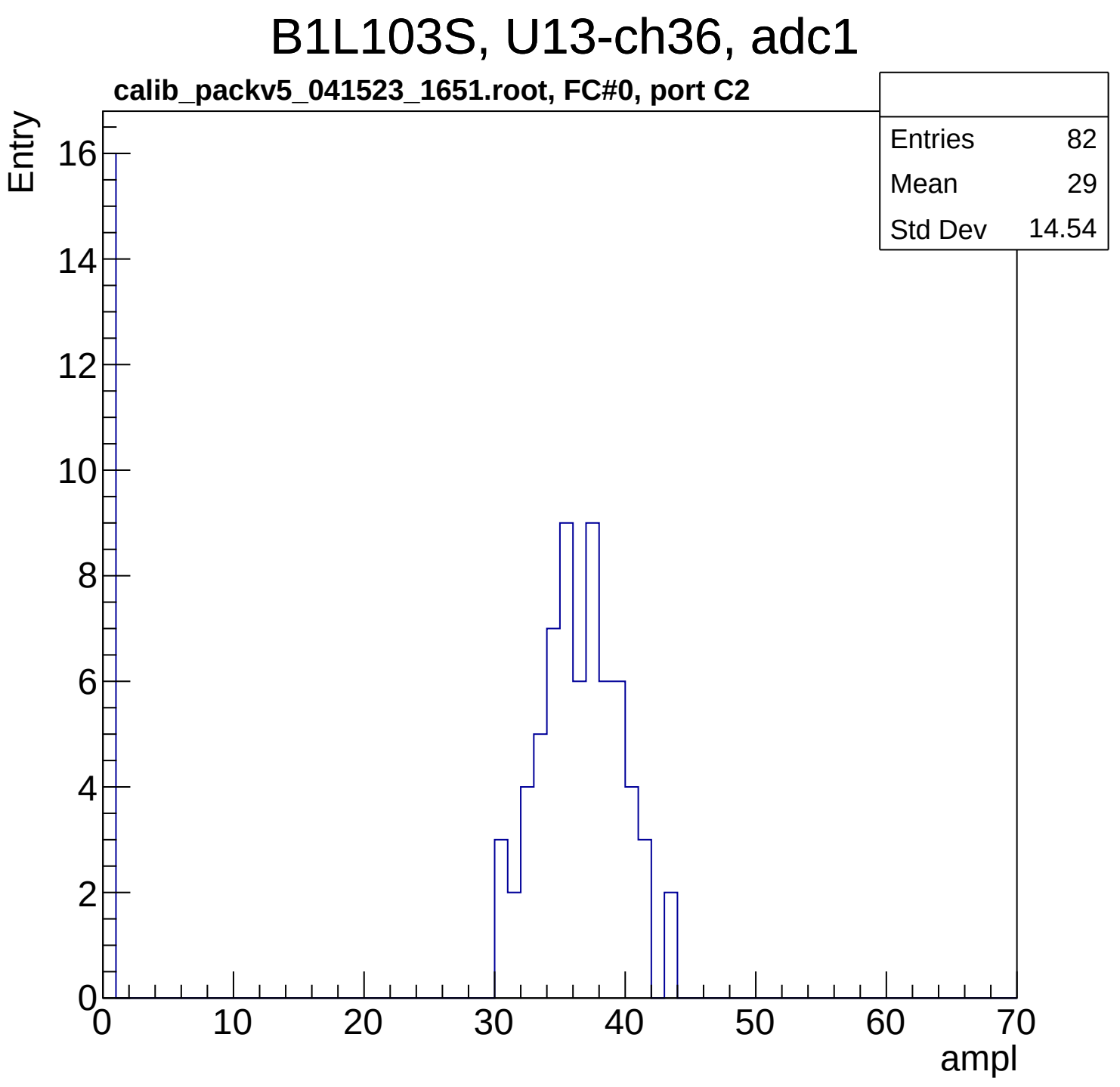

B1L103S, U13-ch35, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 56.29
Std Dev 8.438
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

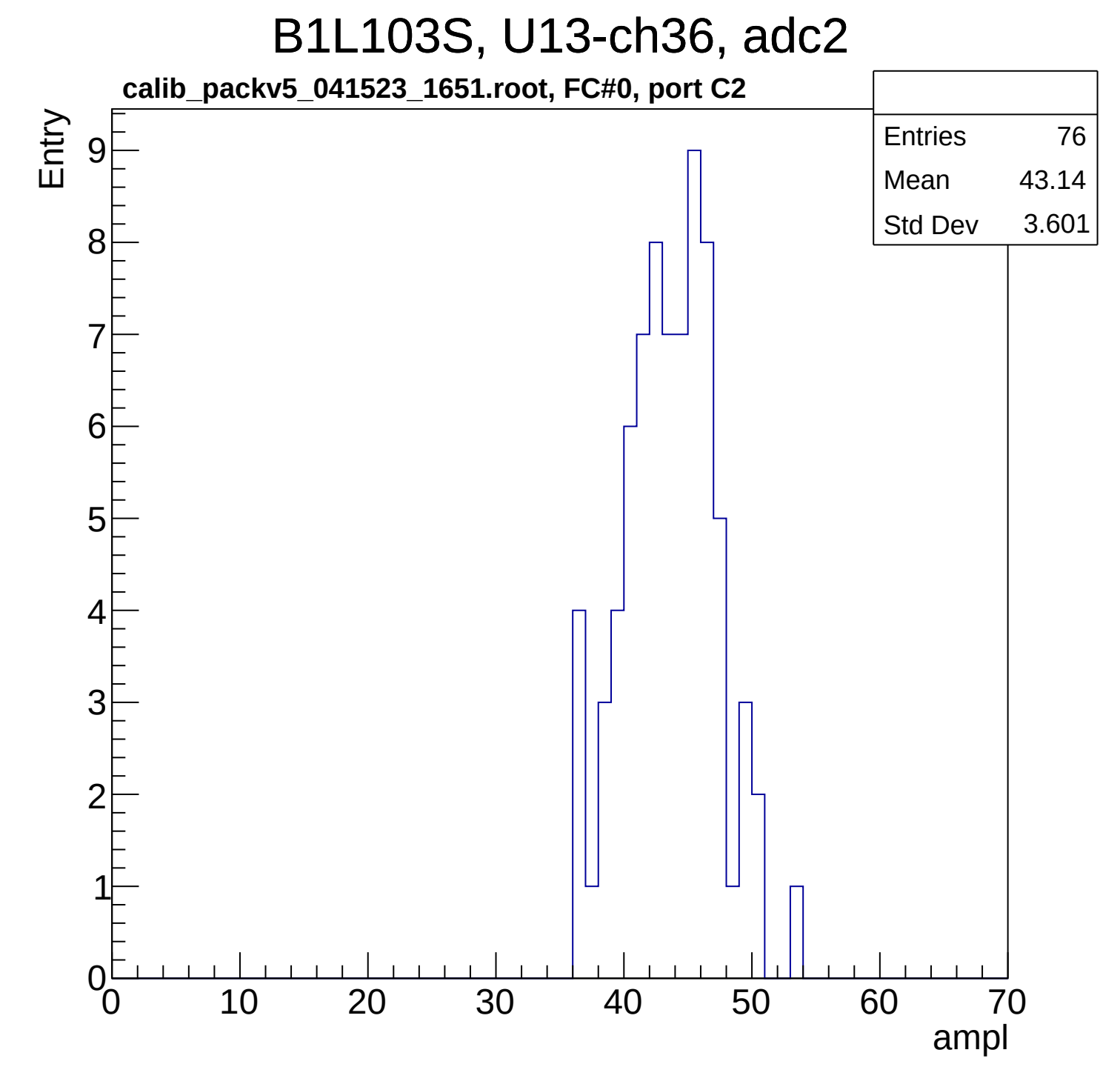

B1L103S, U13-ch35, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 61.38
Std Dev 1.69
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

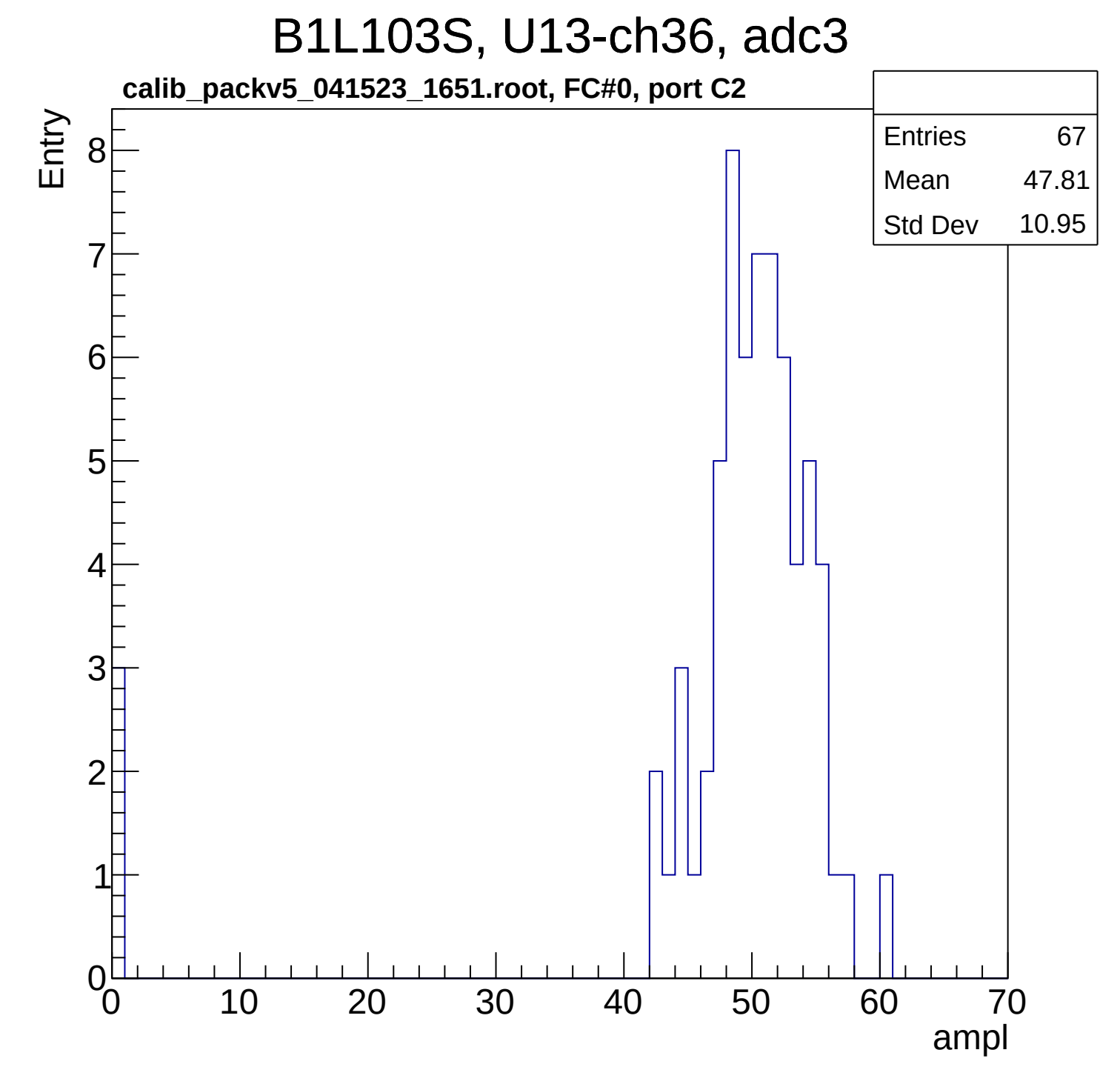

B1L103S, U13-ch35, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

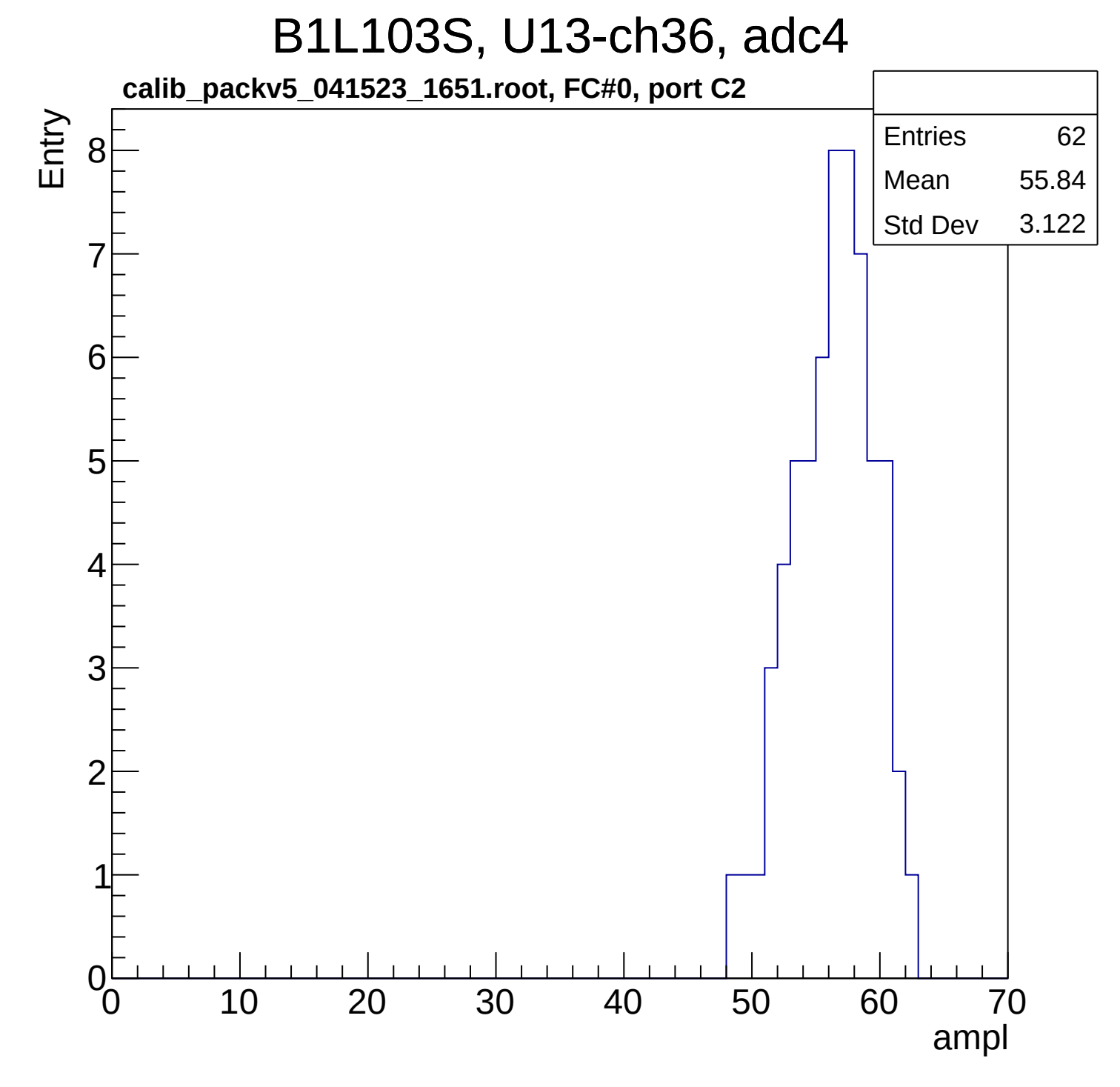

B1L103S, U13-ch35, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

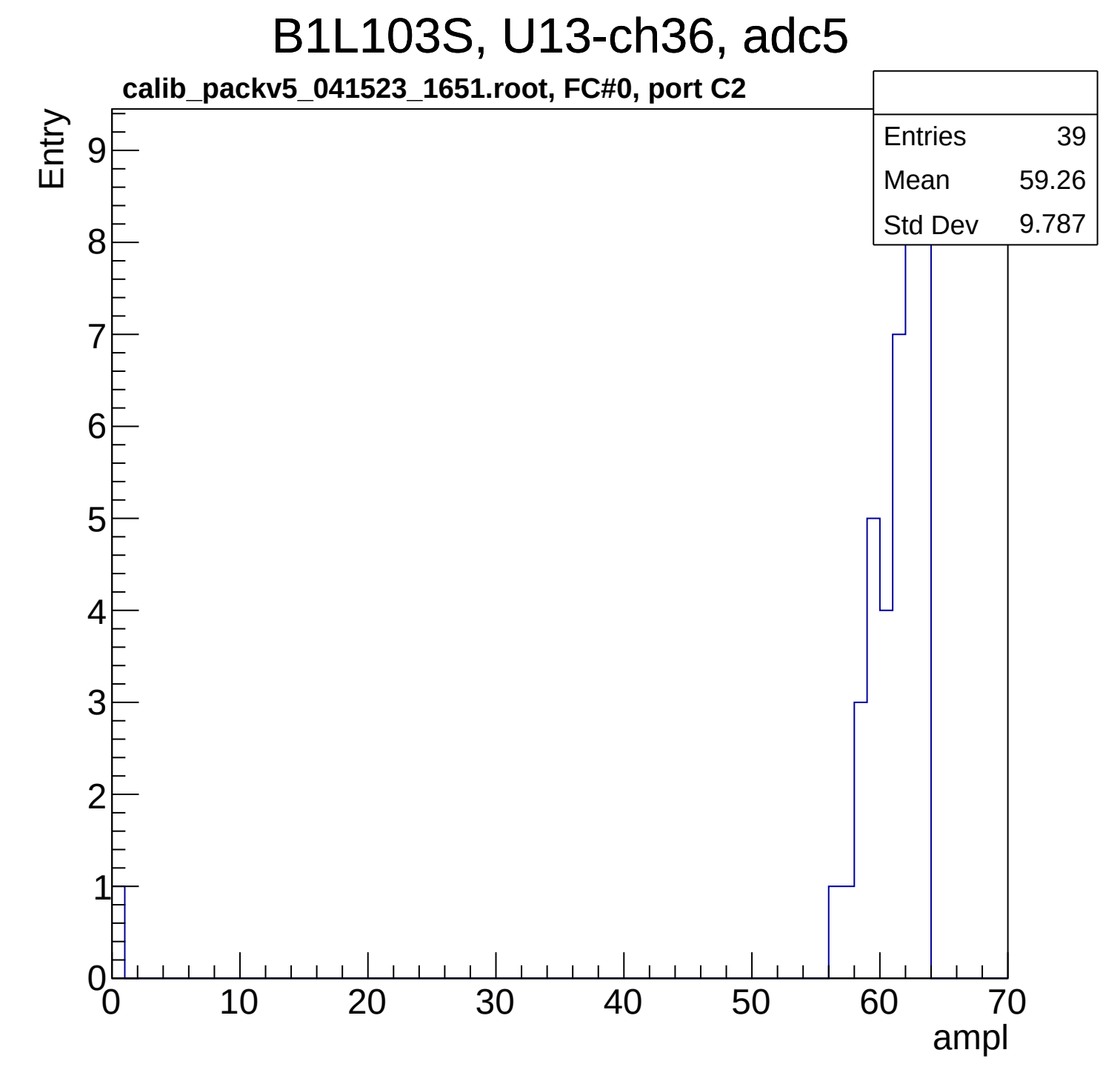

B1L103S, U13-ch36, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 23.65
Std Dev 12.32
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

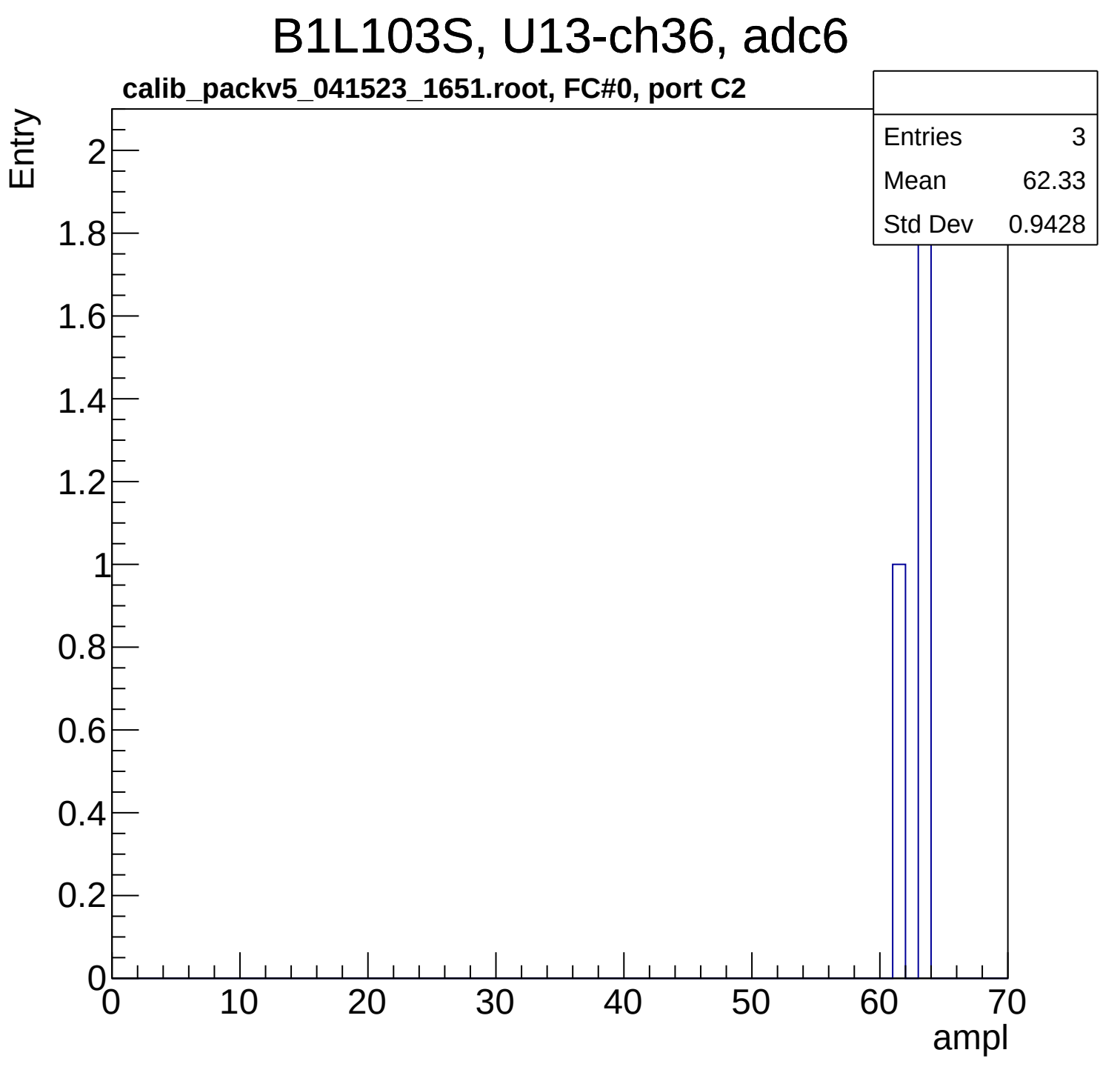

B1L103S, U13-ch36, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 29
Std Dev 14.54
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

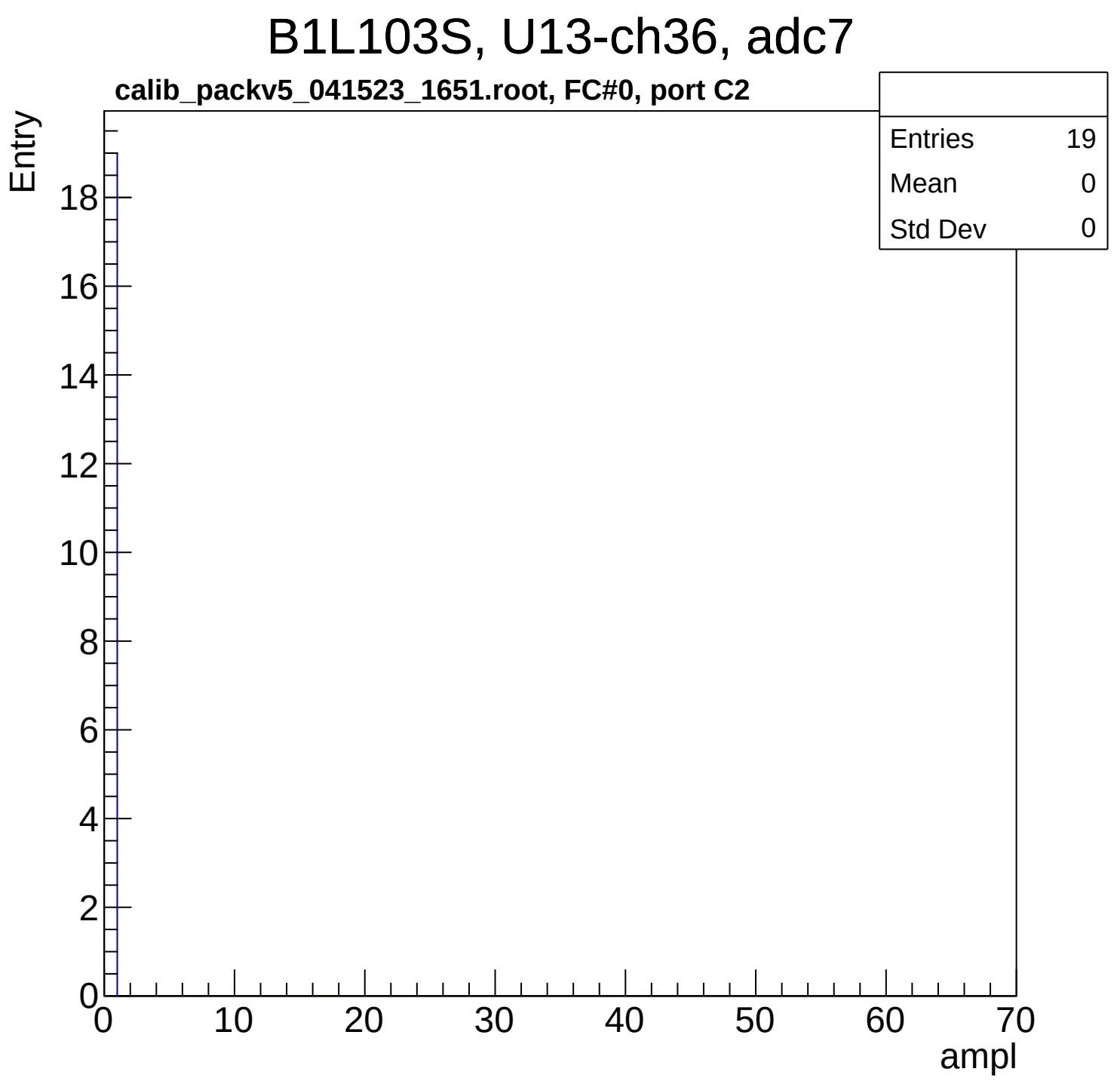

B1L103S, U13-ch36, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 43.14
Std Dev 3.601
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

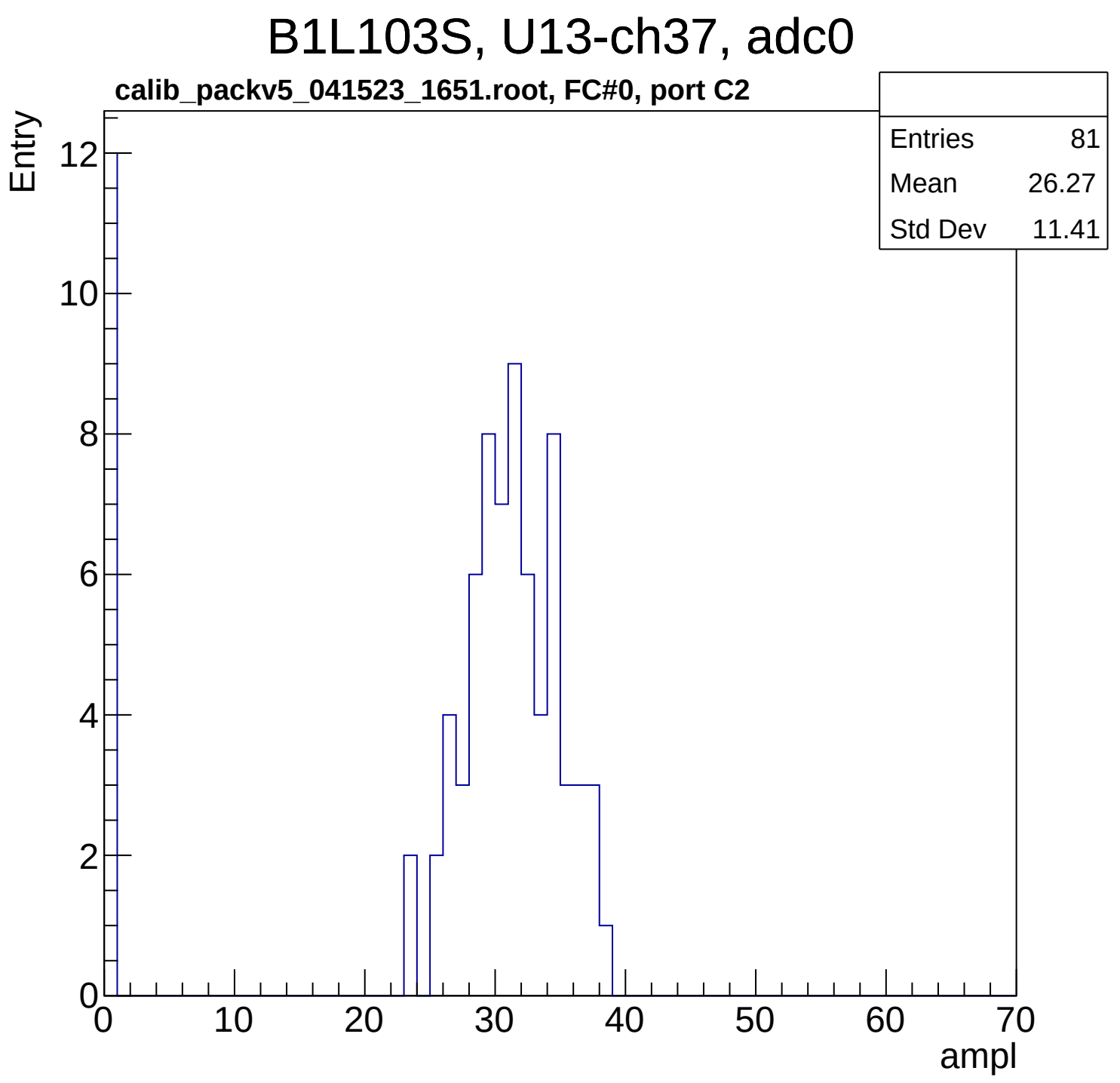

B1L103S, U13-ch36, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 47.81
Std Dev 10.95
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

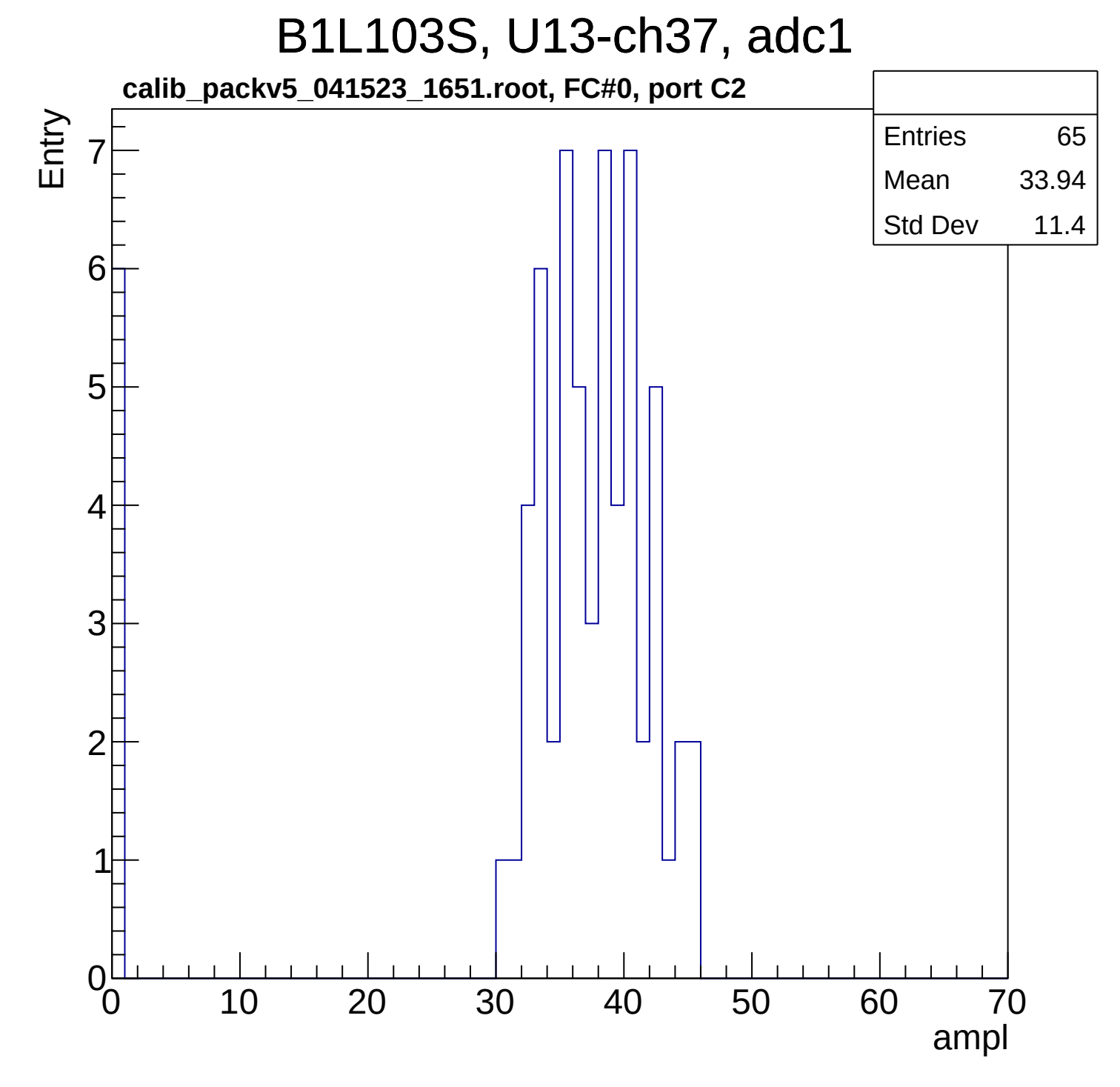

B1L103S, U13-ch36, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 55.84
Std Dev 3.122
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

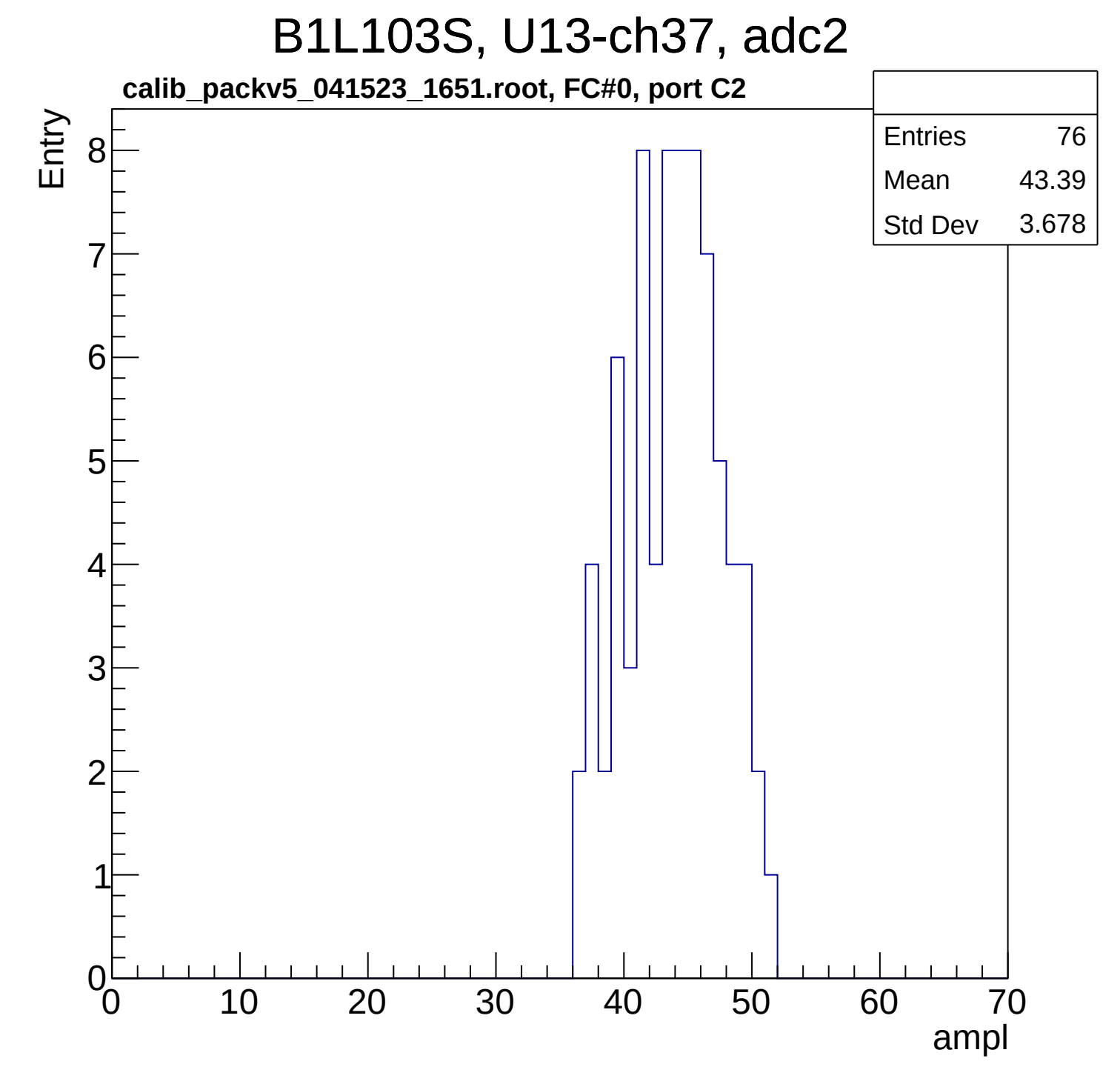

B1L103S, U13-ch36, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 59.26
Std Dev 9.787
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

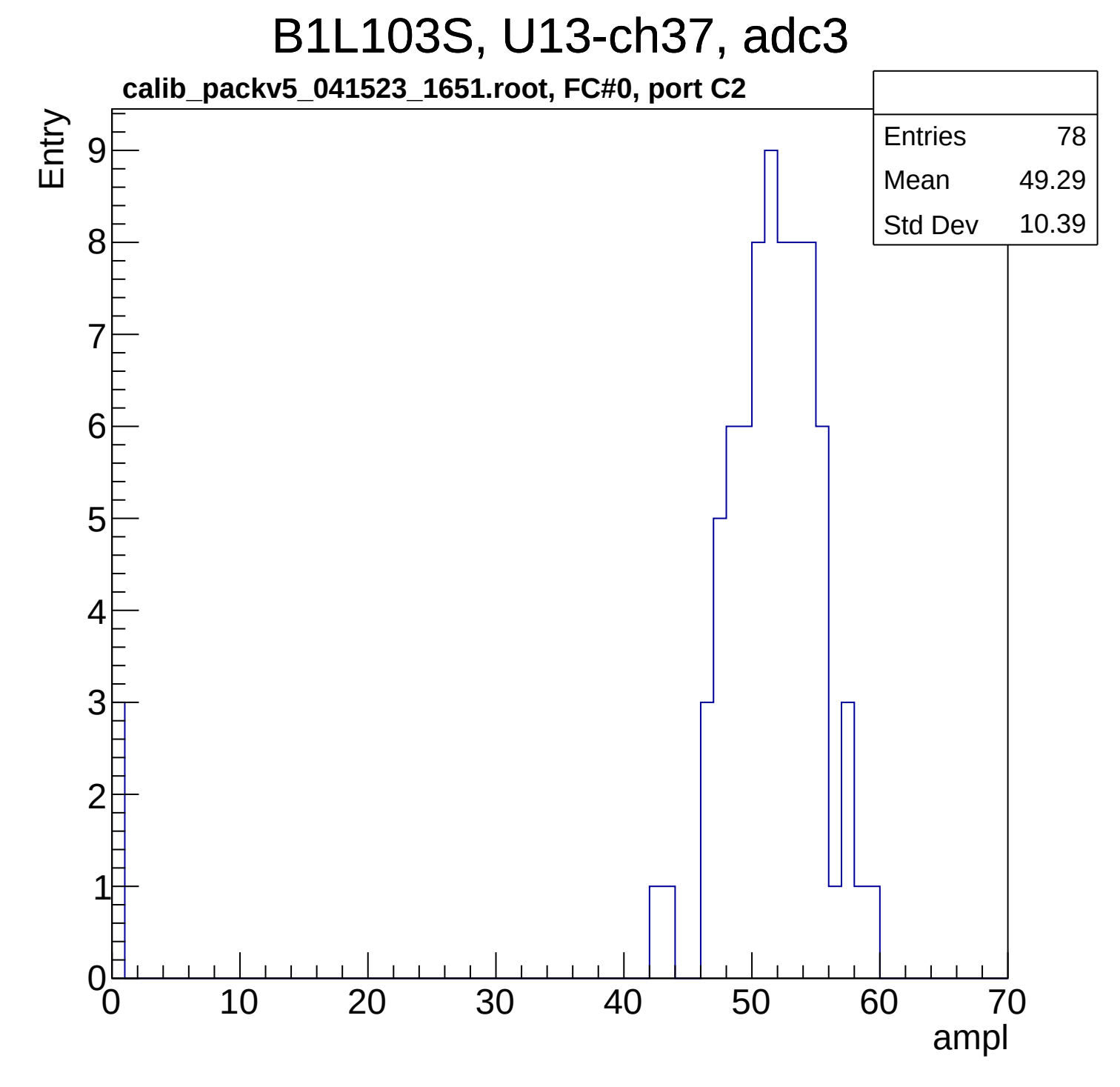

B1L103S, U13-ch36, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.33
Std Dev 0.9428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

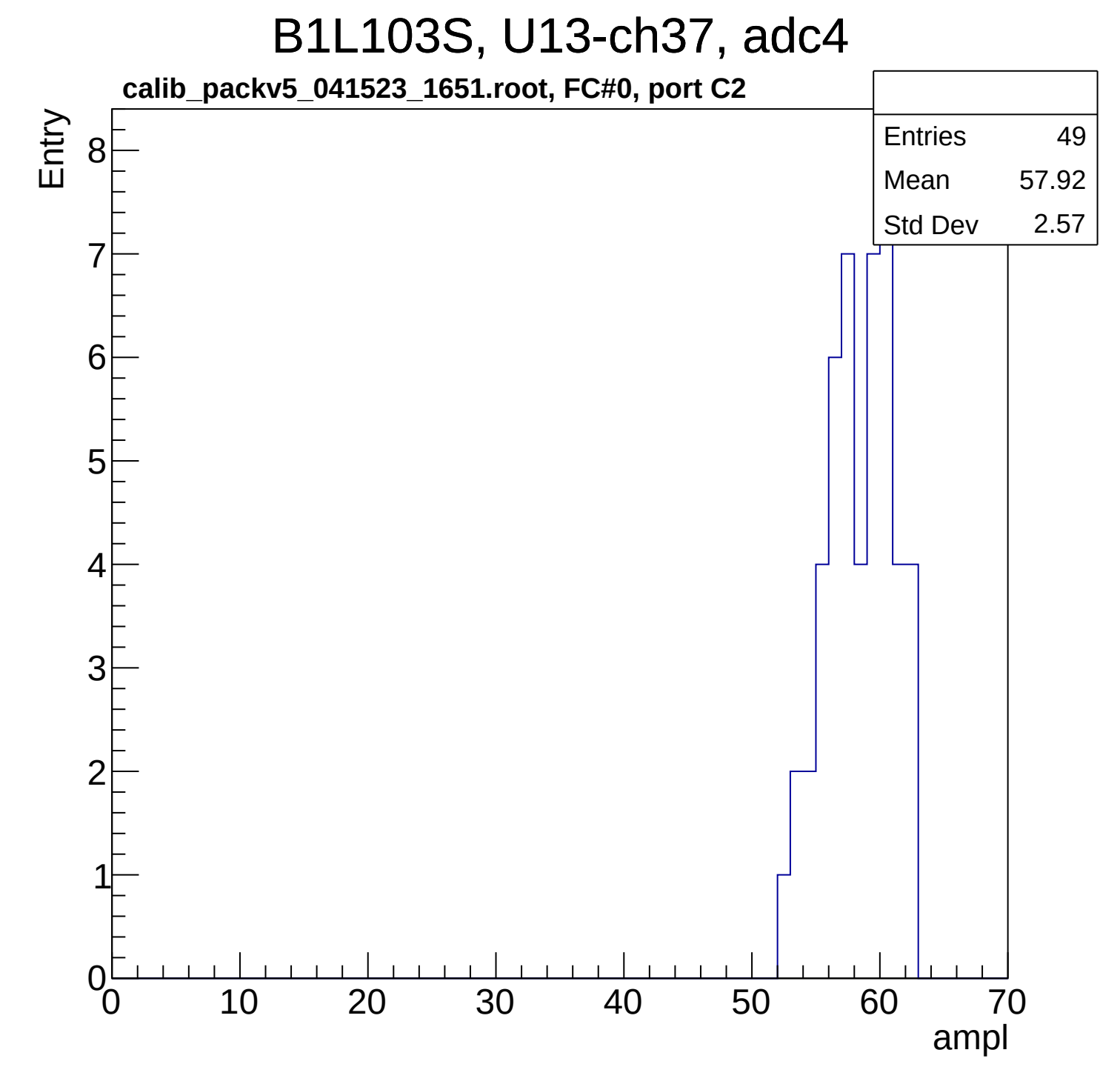

B1L103S, U13-ch36, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch37, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 26.27
Std Dev 11.41
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch37, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 33.94
Std Dev 11.4
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch37, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 43.39
Std Dev 3.678
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch37, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 49.29
Std Dev 10.39
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch37, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 57.92
Std Dev 2.57
Entry
ampl
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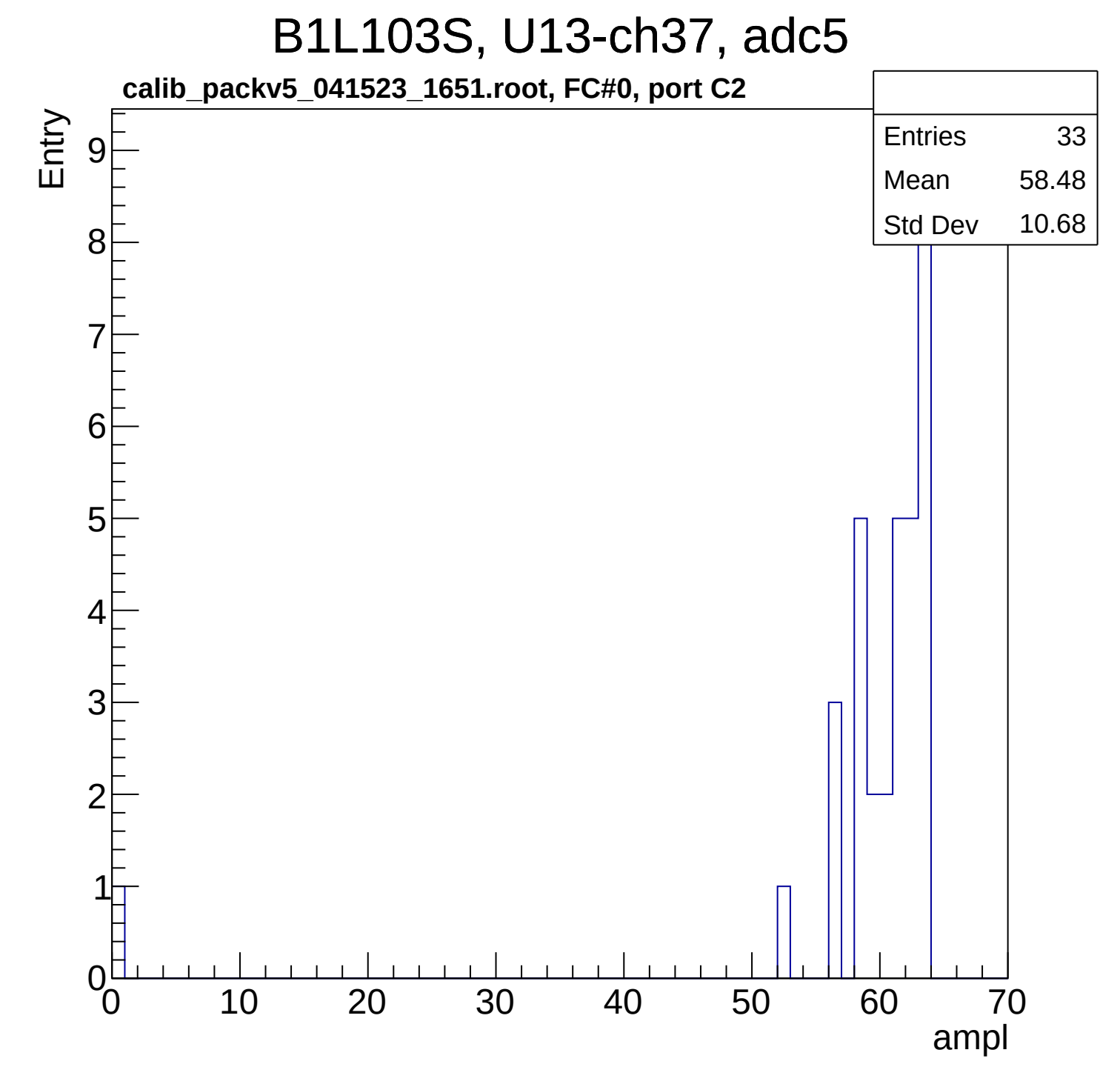
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch37, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 58.48
Std Dev 10.68
Entry
ampl
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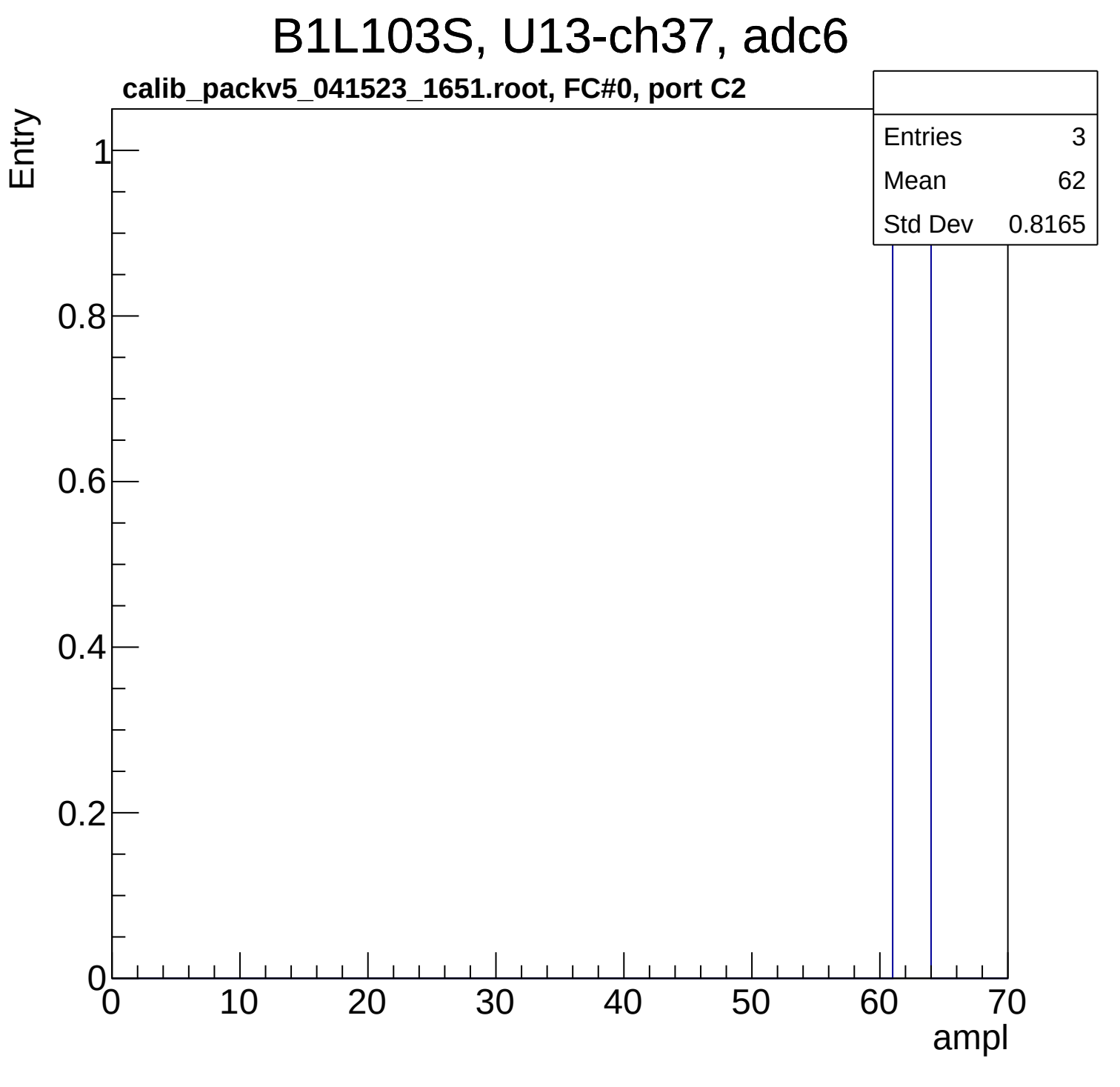
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch37, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62
Std Dev 0.8165
Entry
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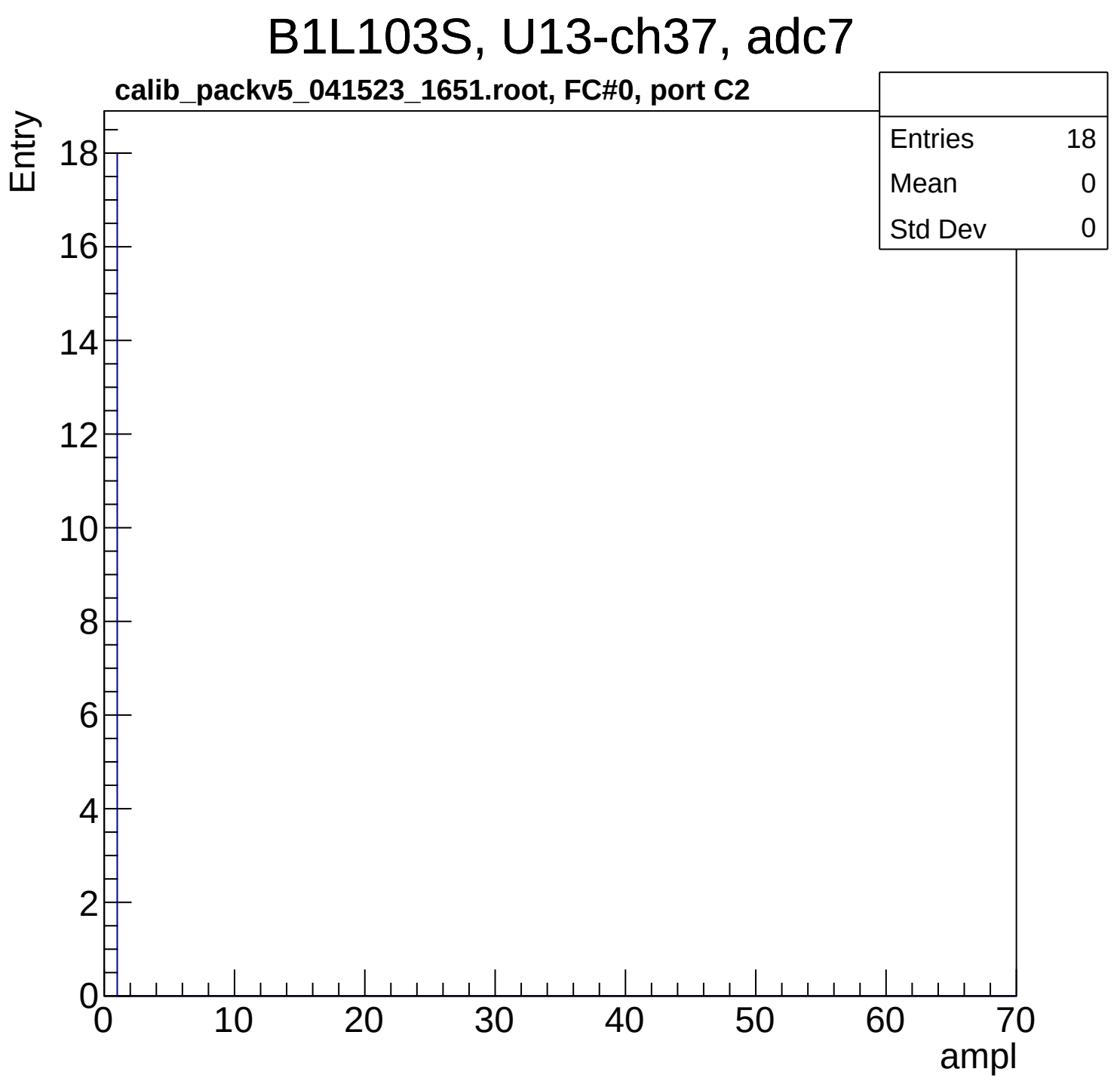
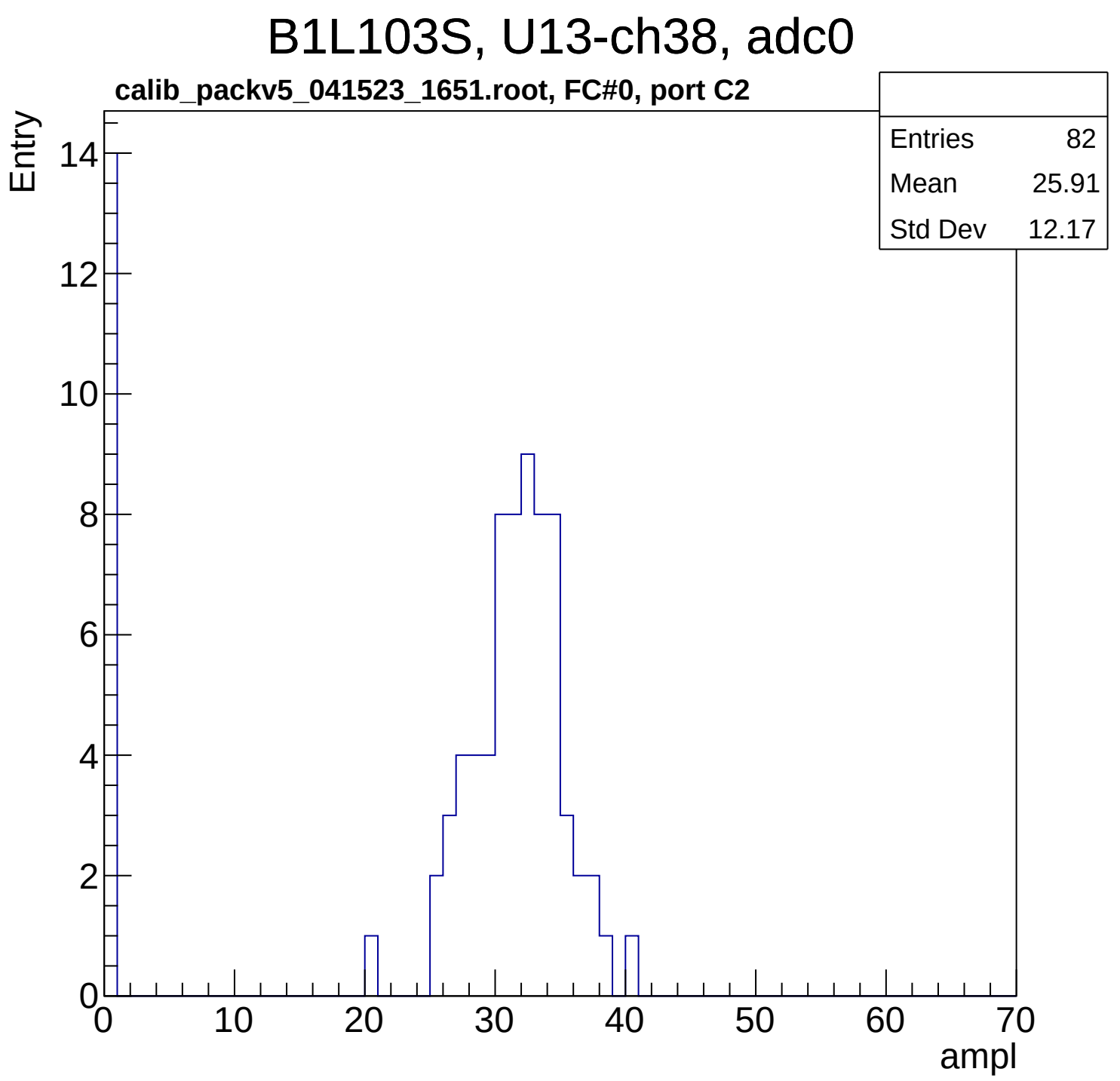
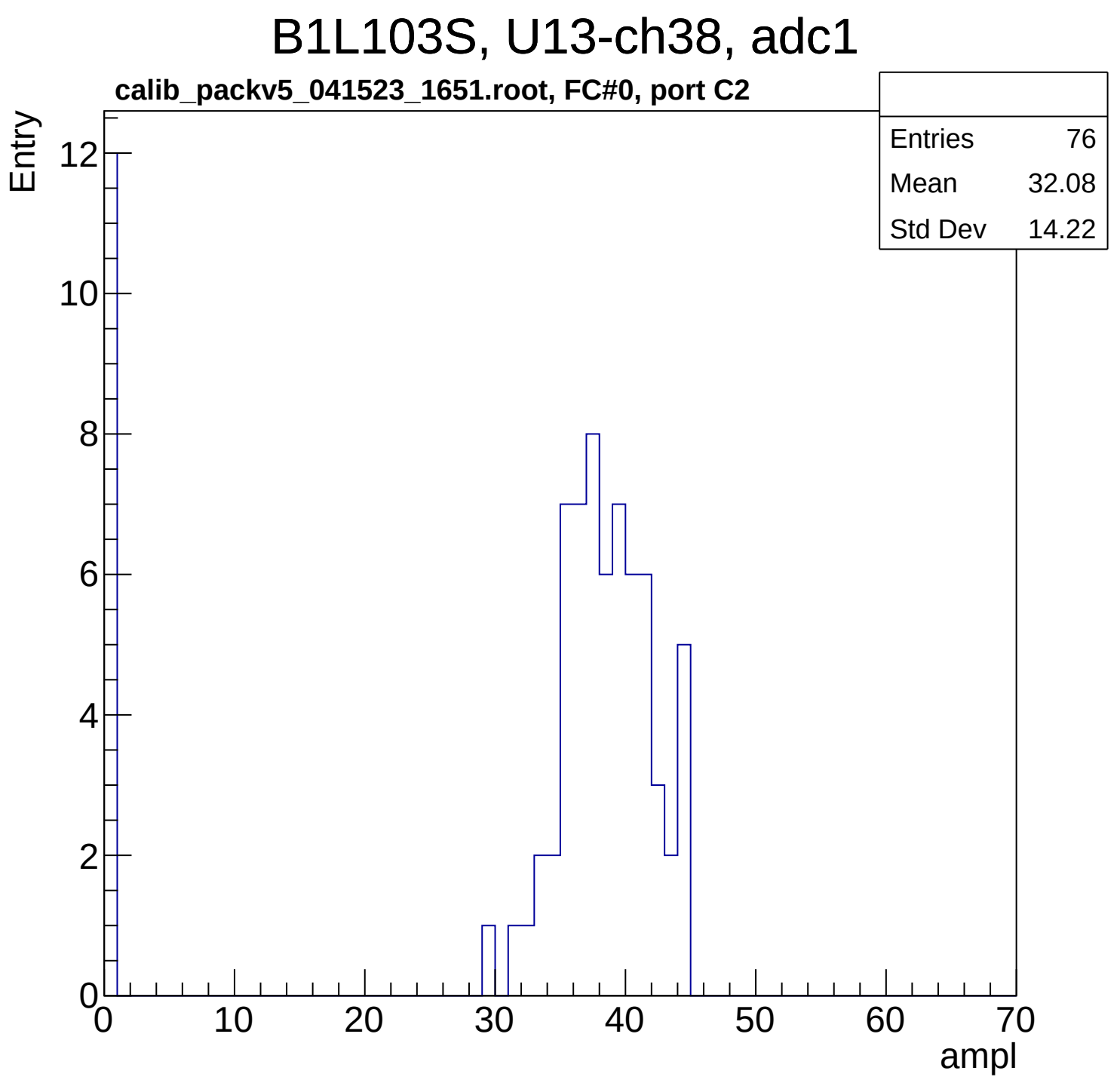
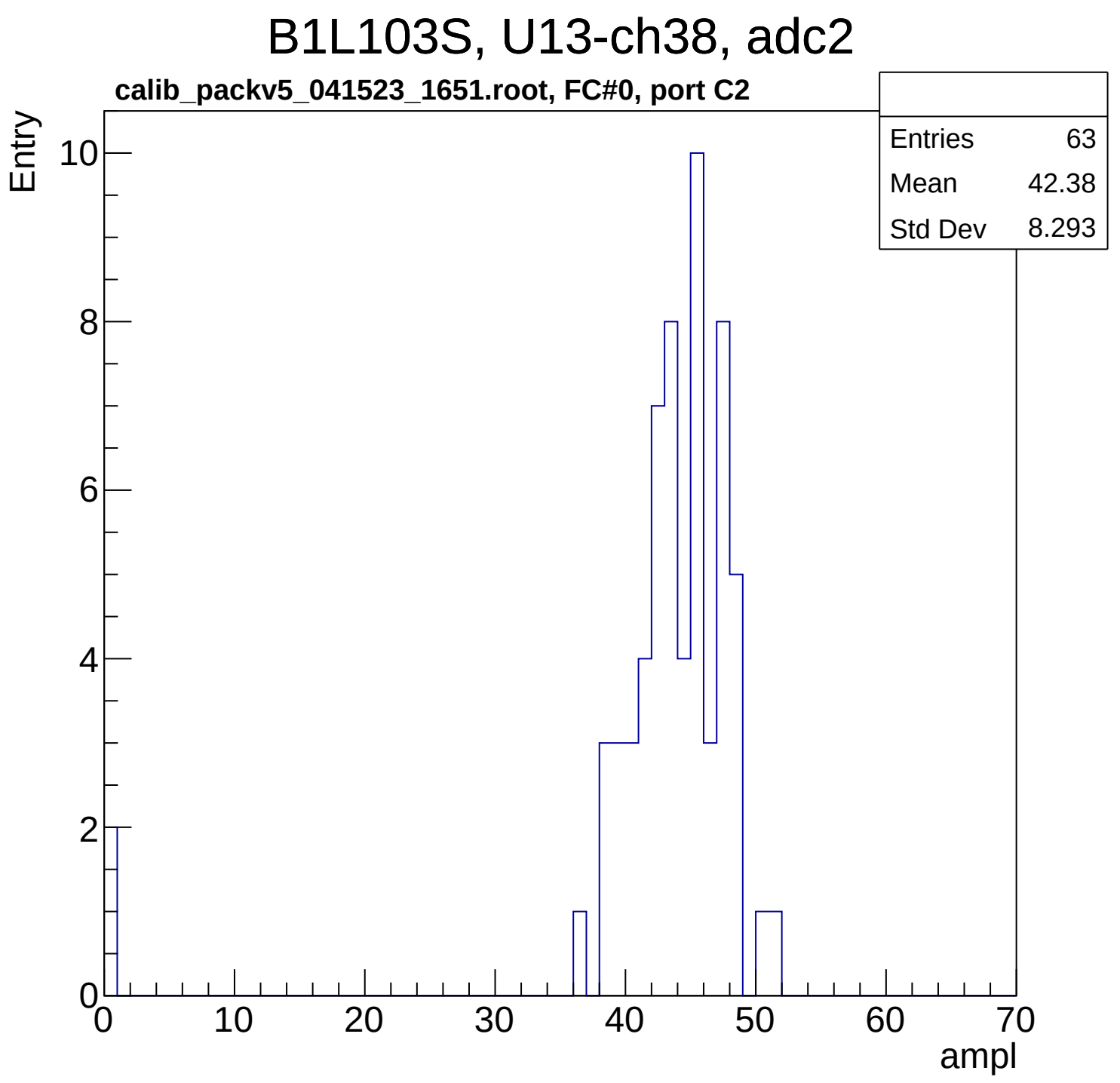
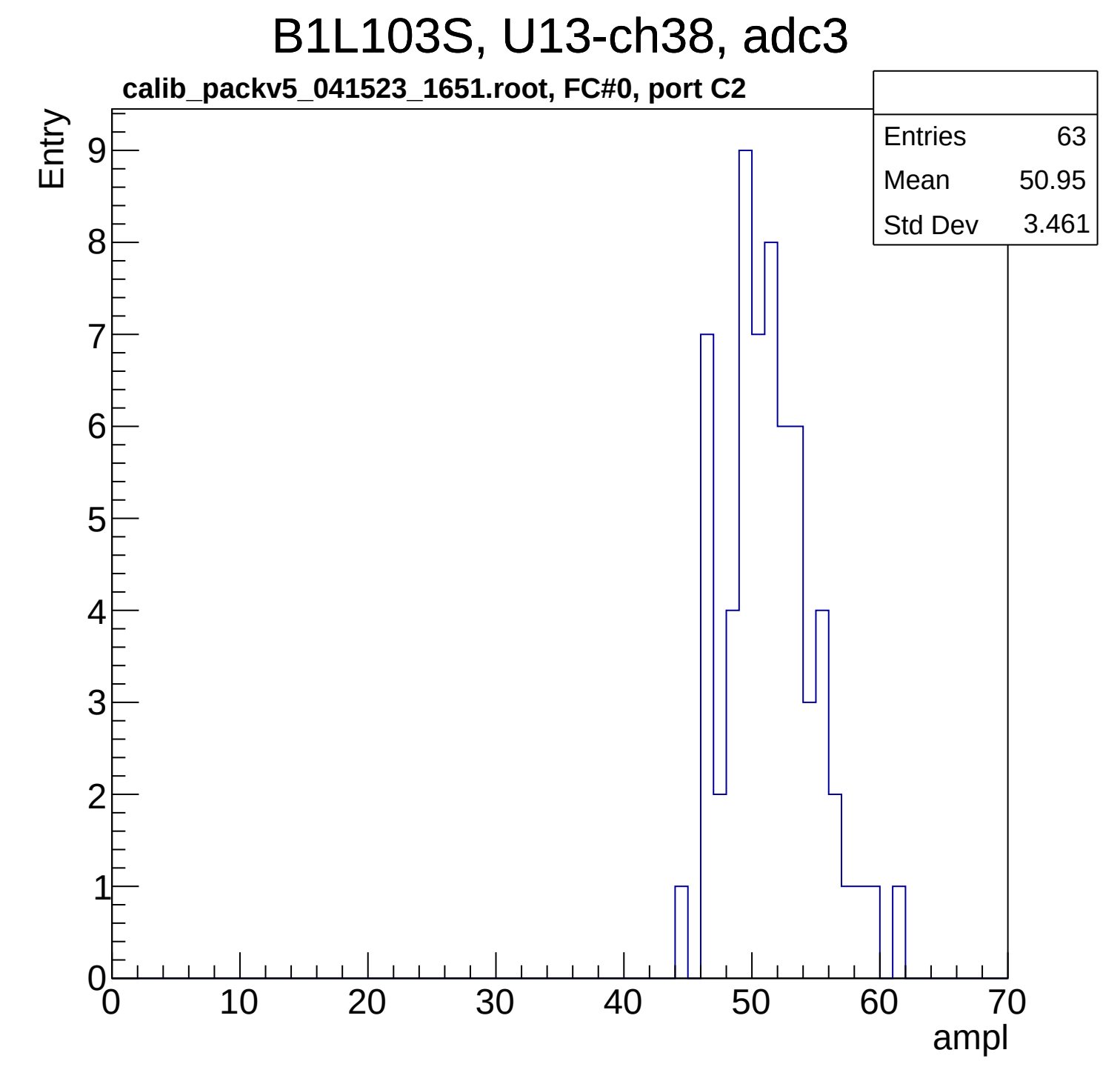
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch37, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch38, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 25.91
Std Dev 12.17
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch38, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 32.08
Std Dev 14.22
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch38, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 42.38
Std Dev 8.293
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch38, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 50.95
Std Dev 3.461
Entry
ampl
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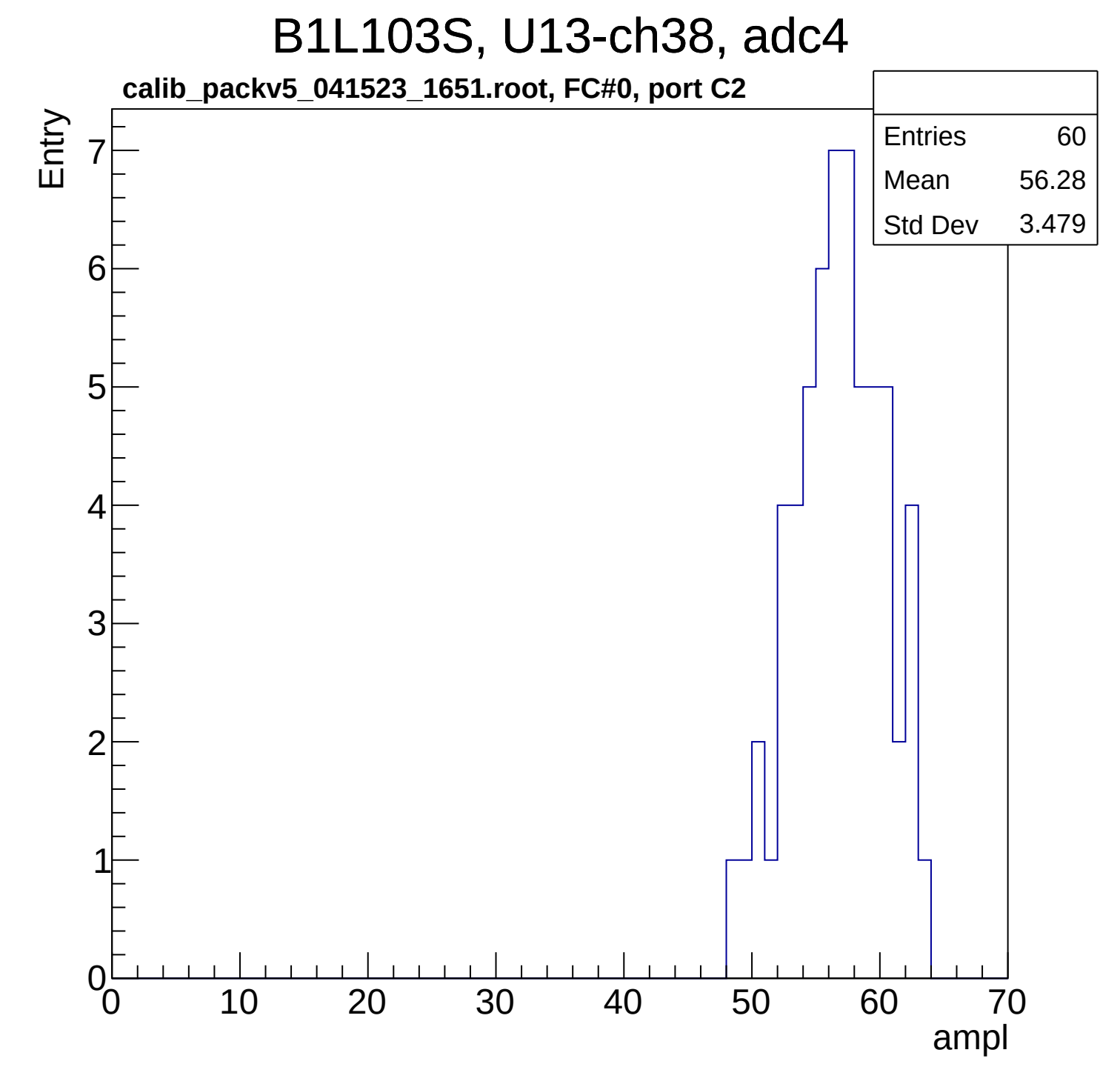
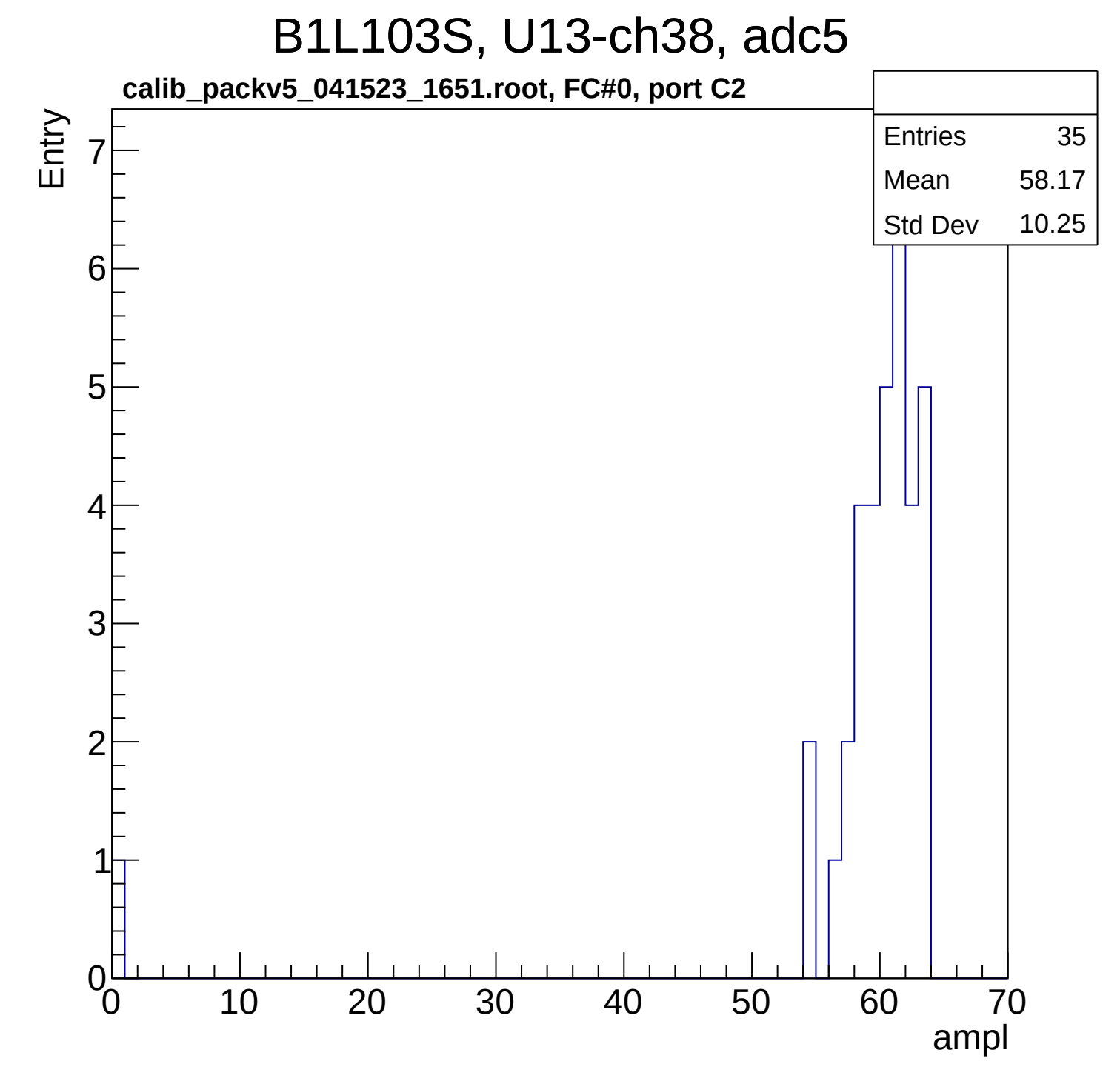
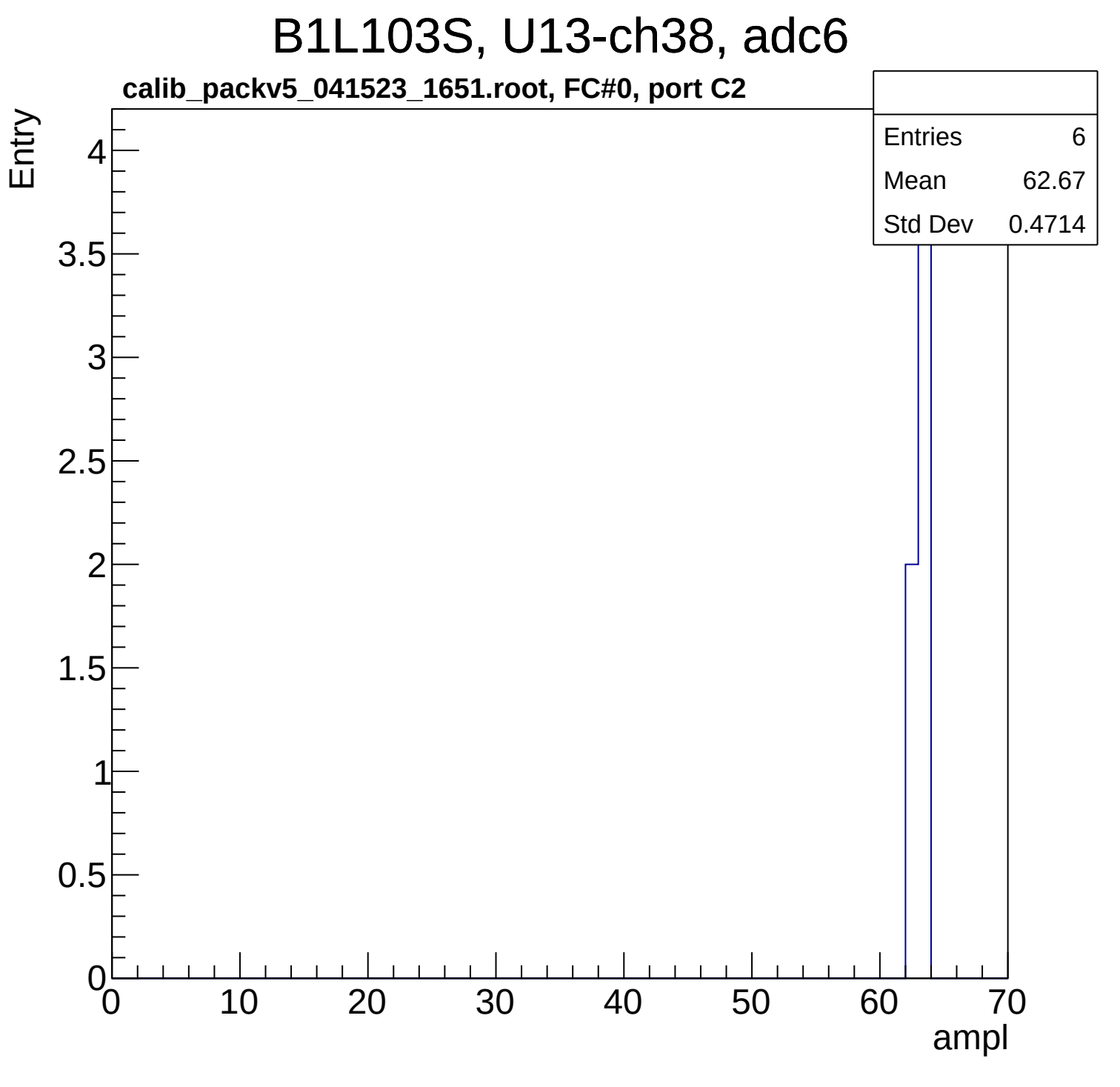
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch38, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 56.28
Std Dev 3.479
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch38, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 58.17
Std Dev 10.25
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch38, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
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20
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40
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60
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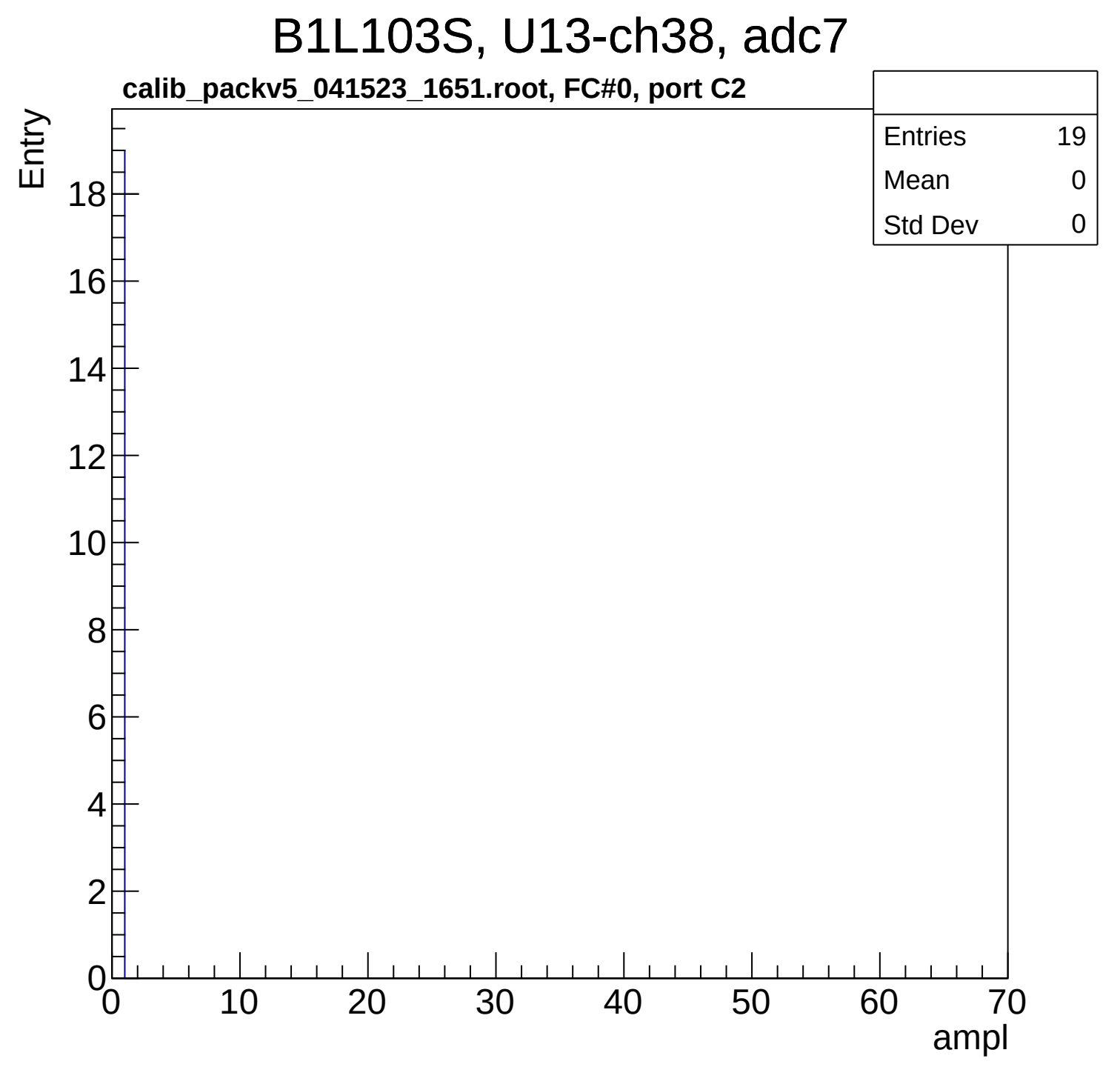
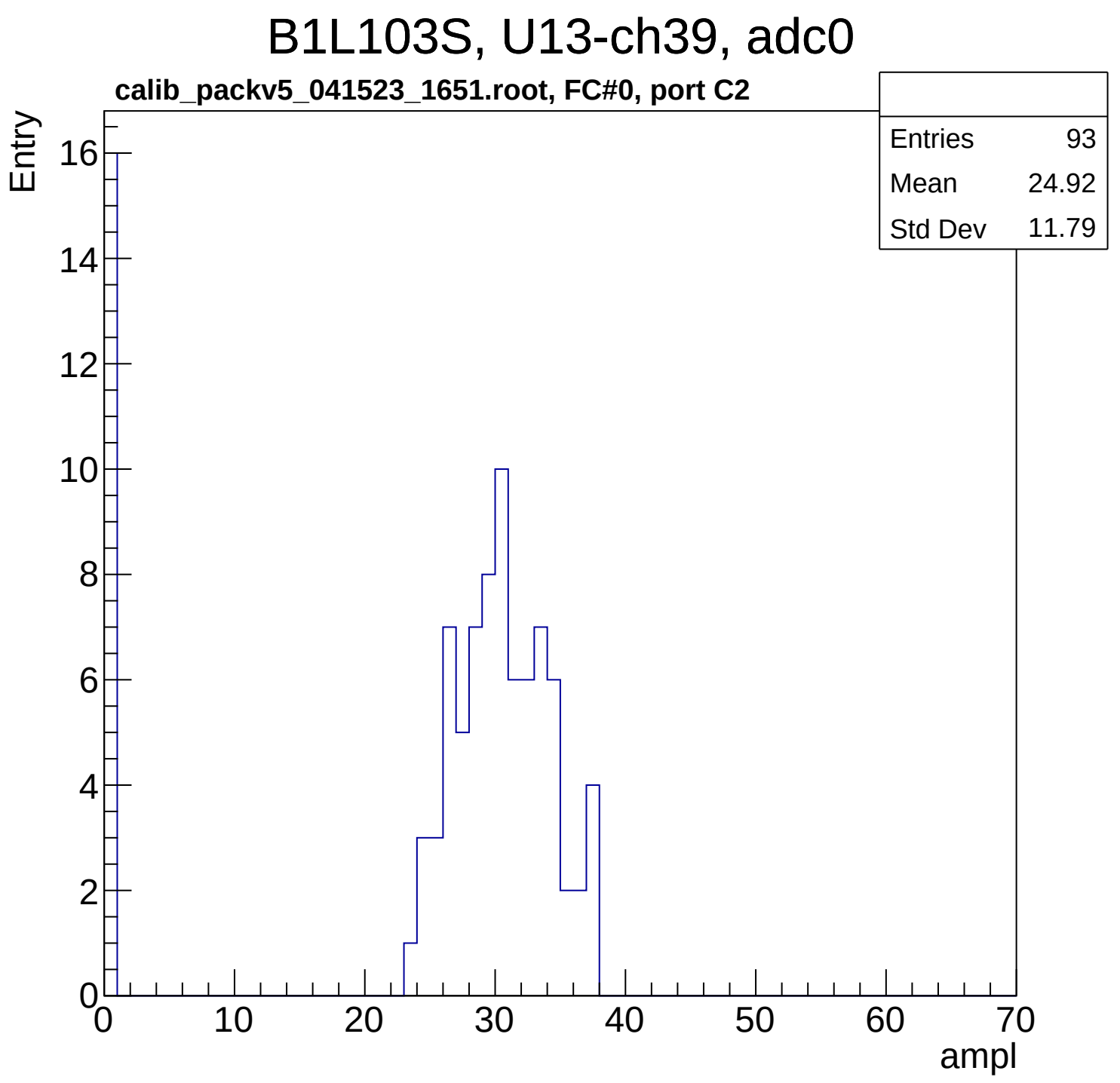
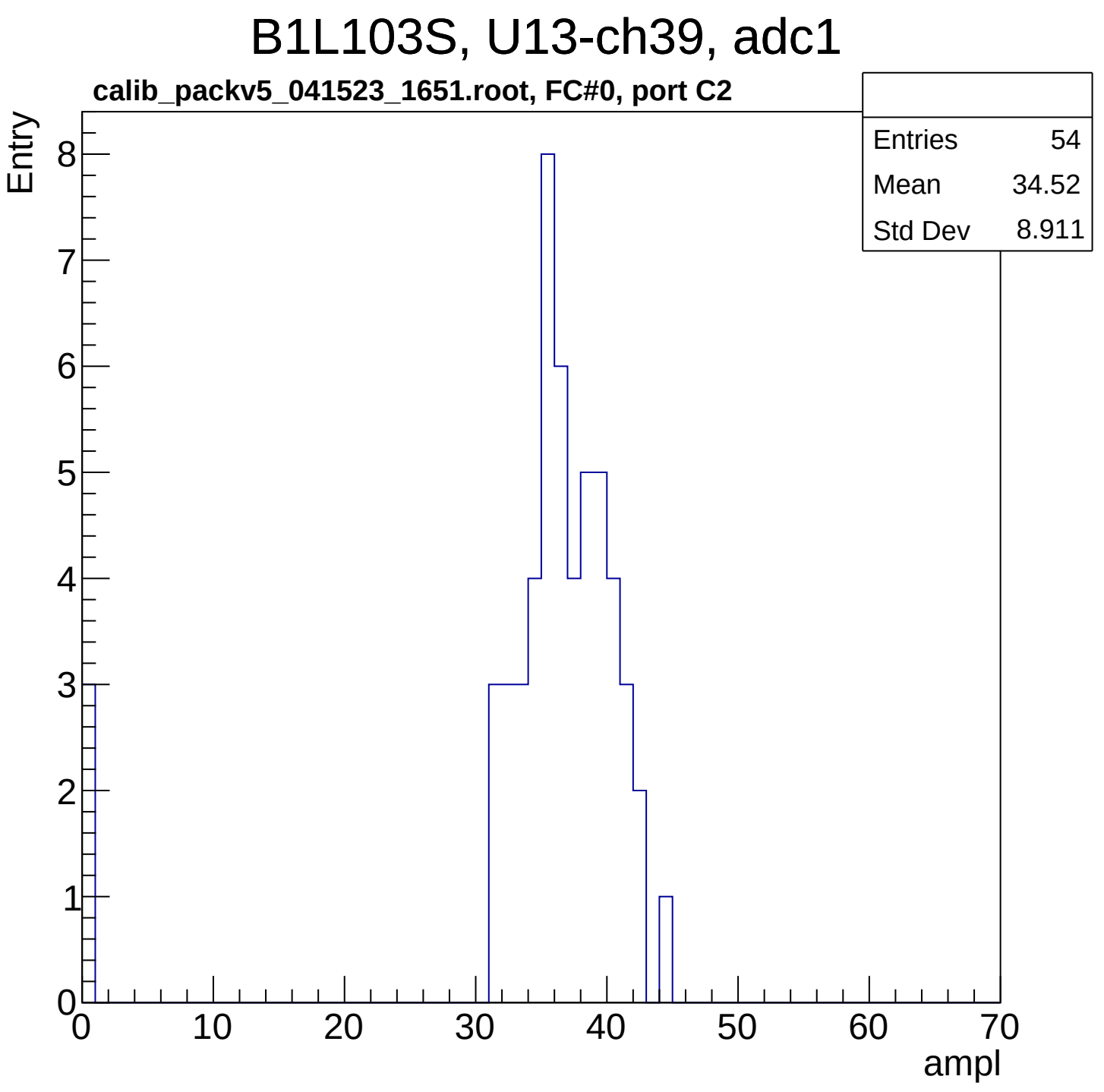

B1L103S, U13-ch38, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch39, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 24.92
Std Dev 11.79
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch39, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 34.52
Std Dev 8.911
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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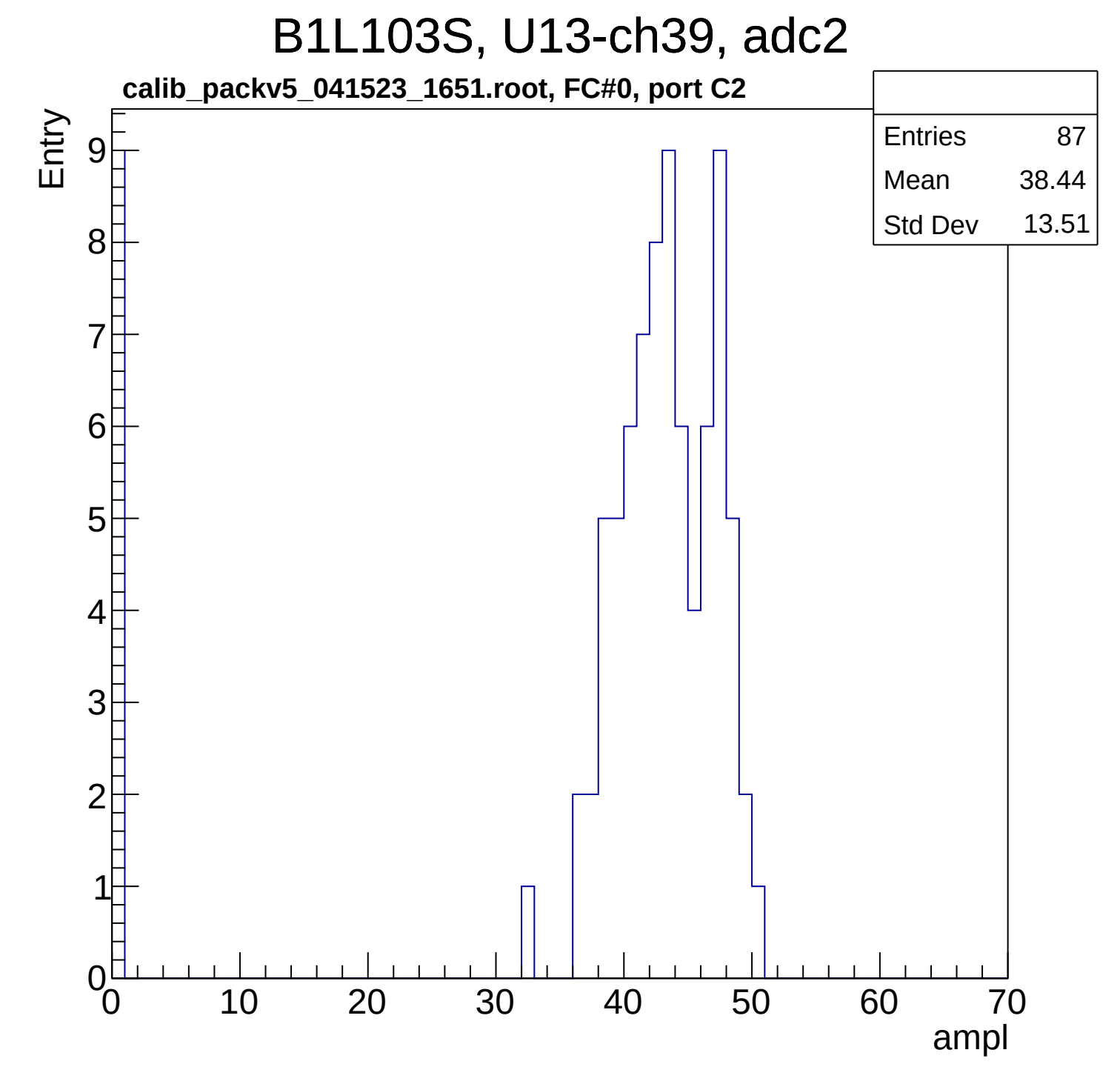
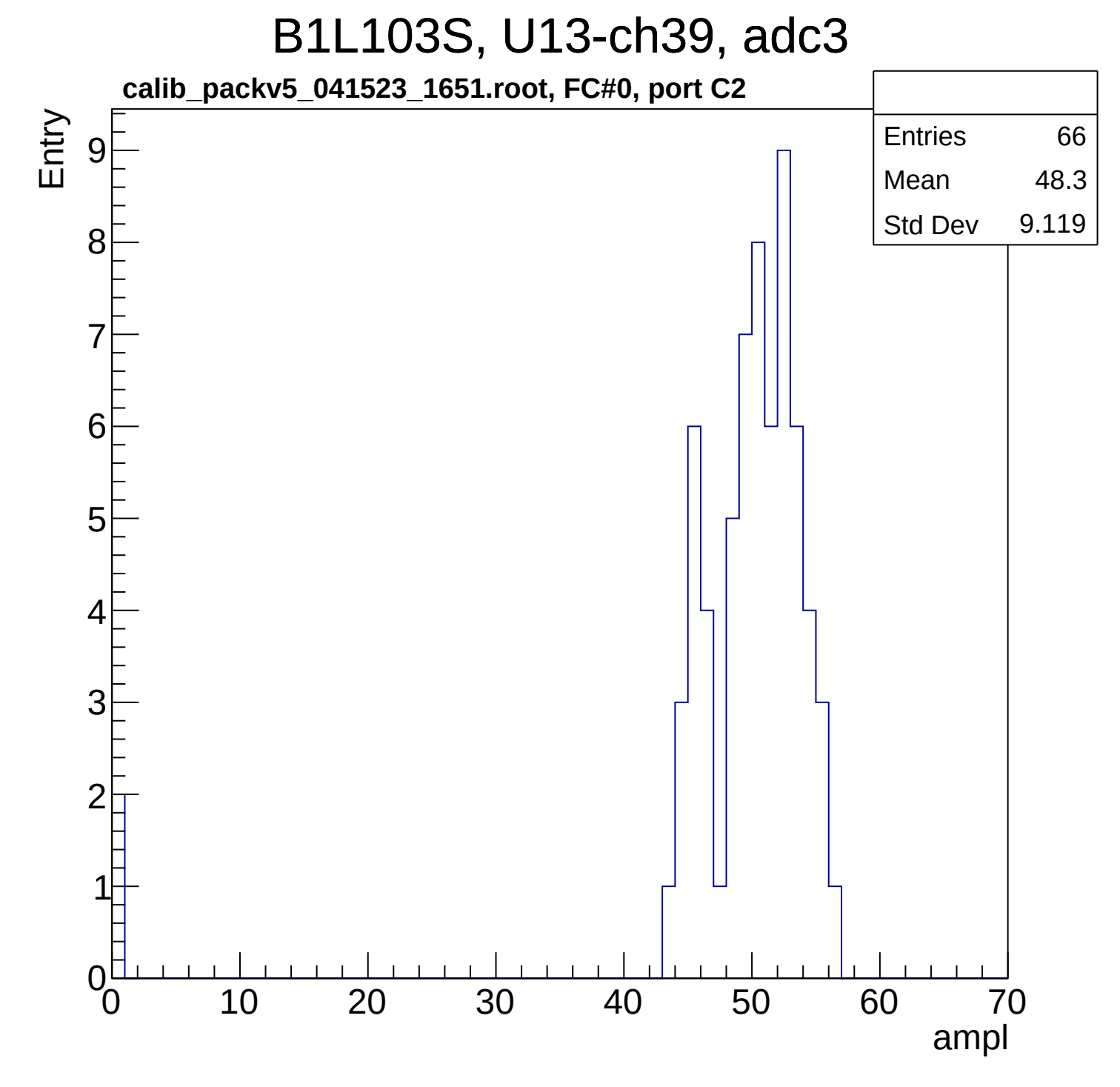
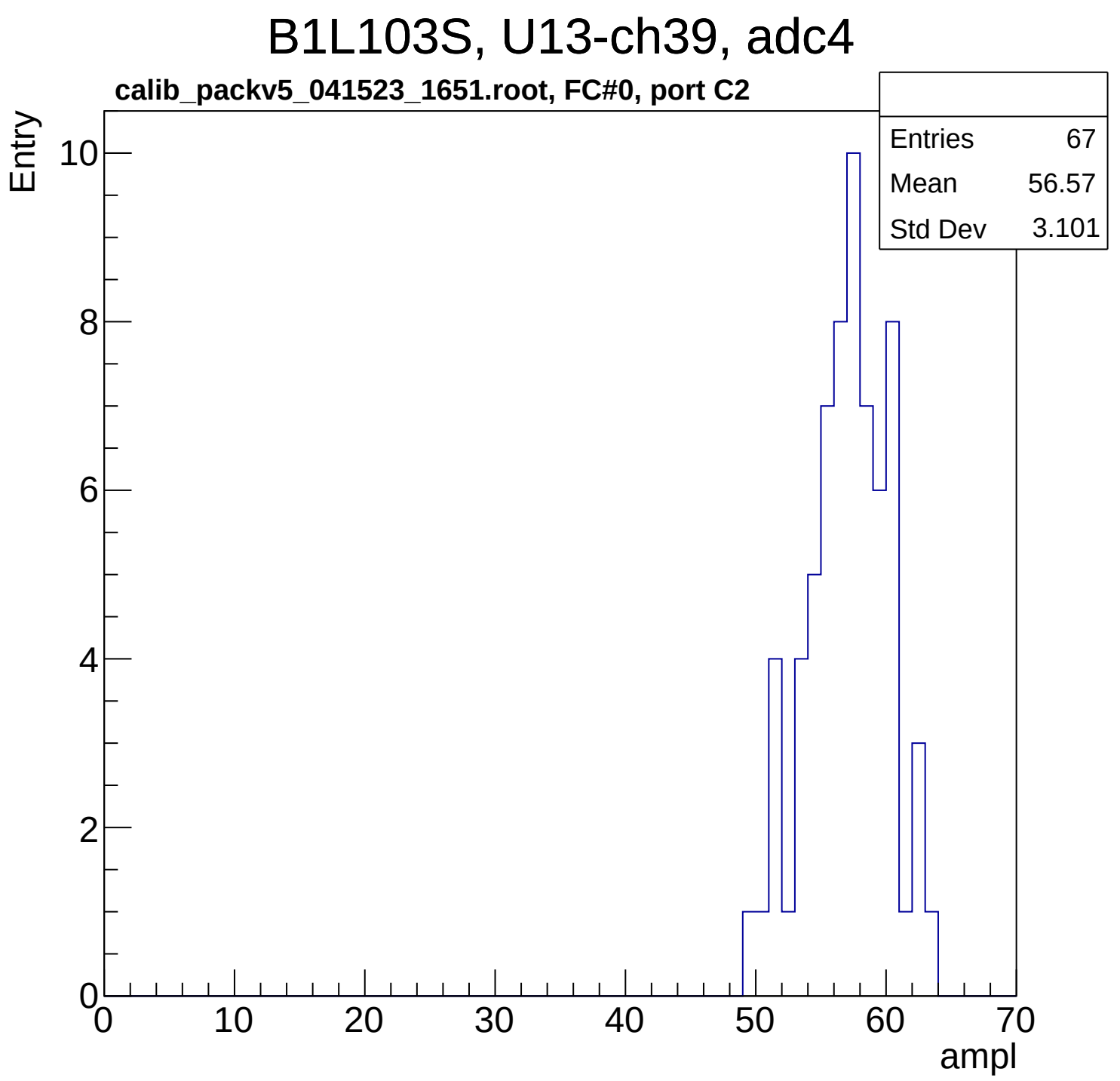
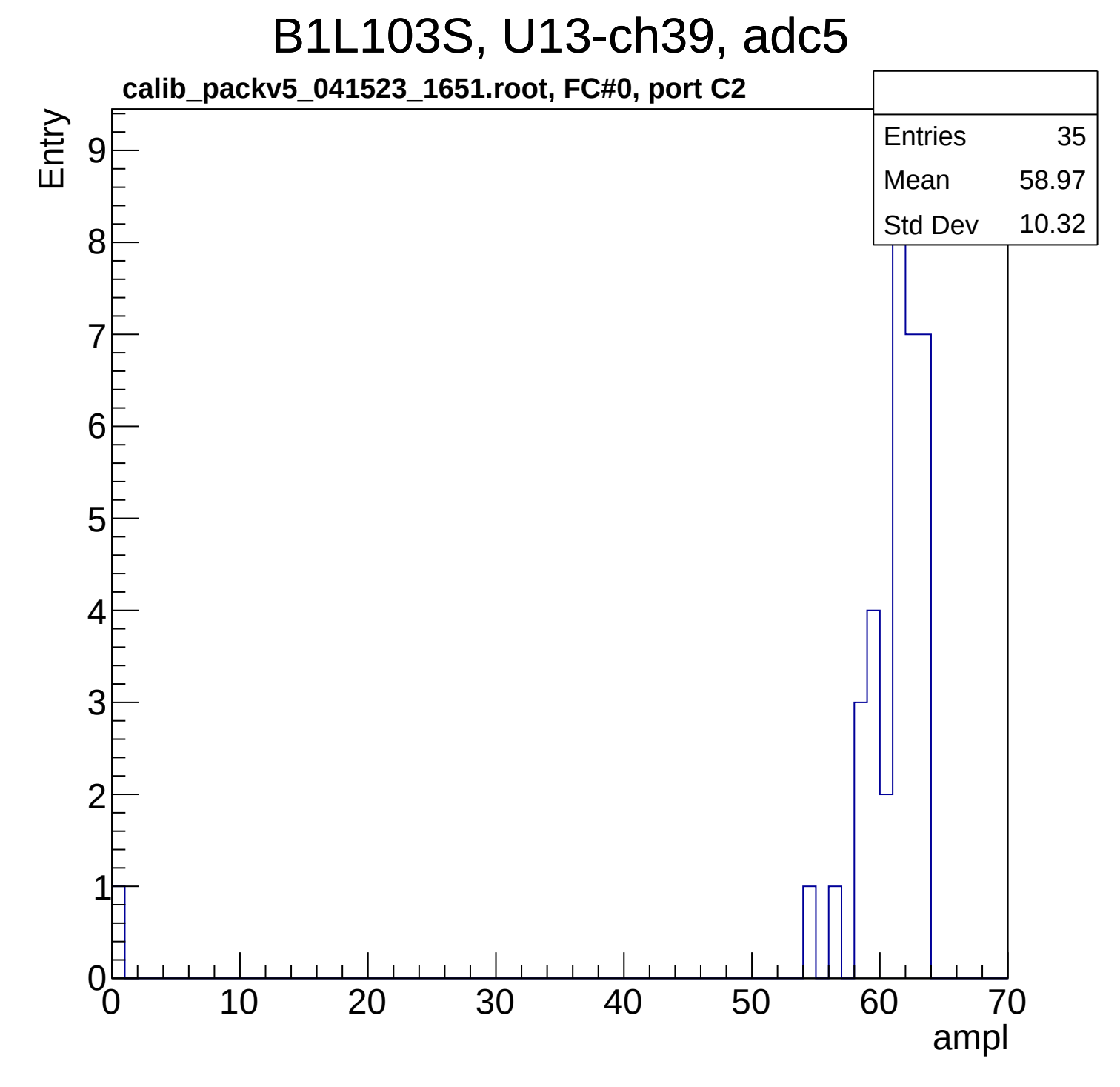
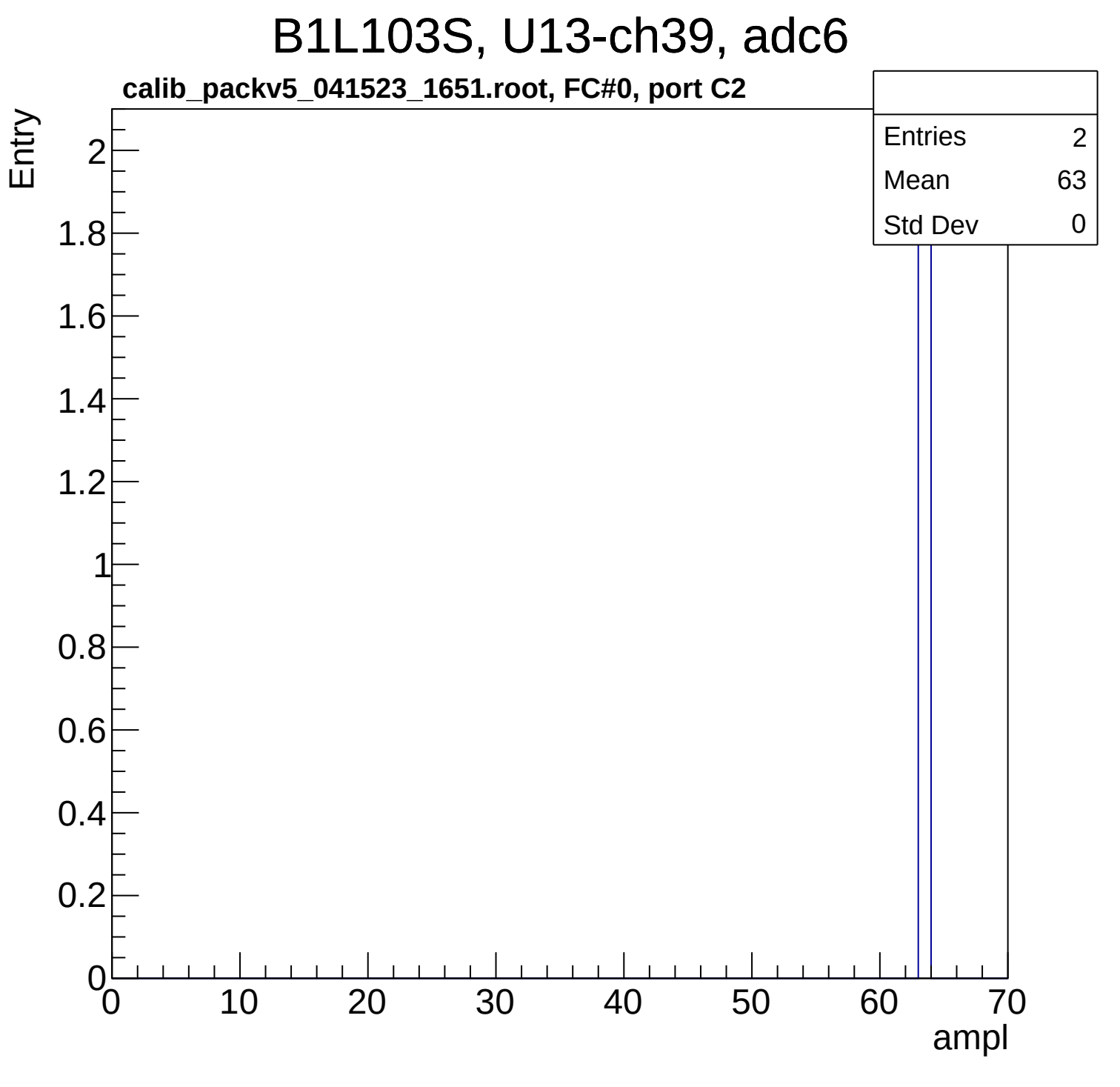
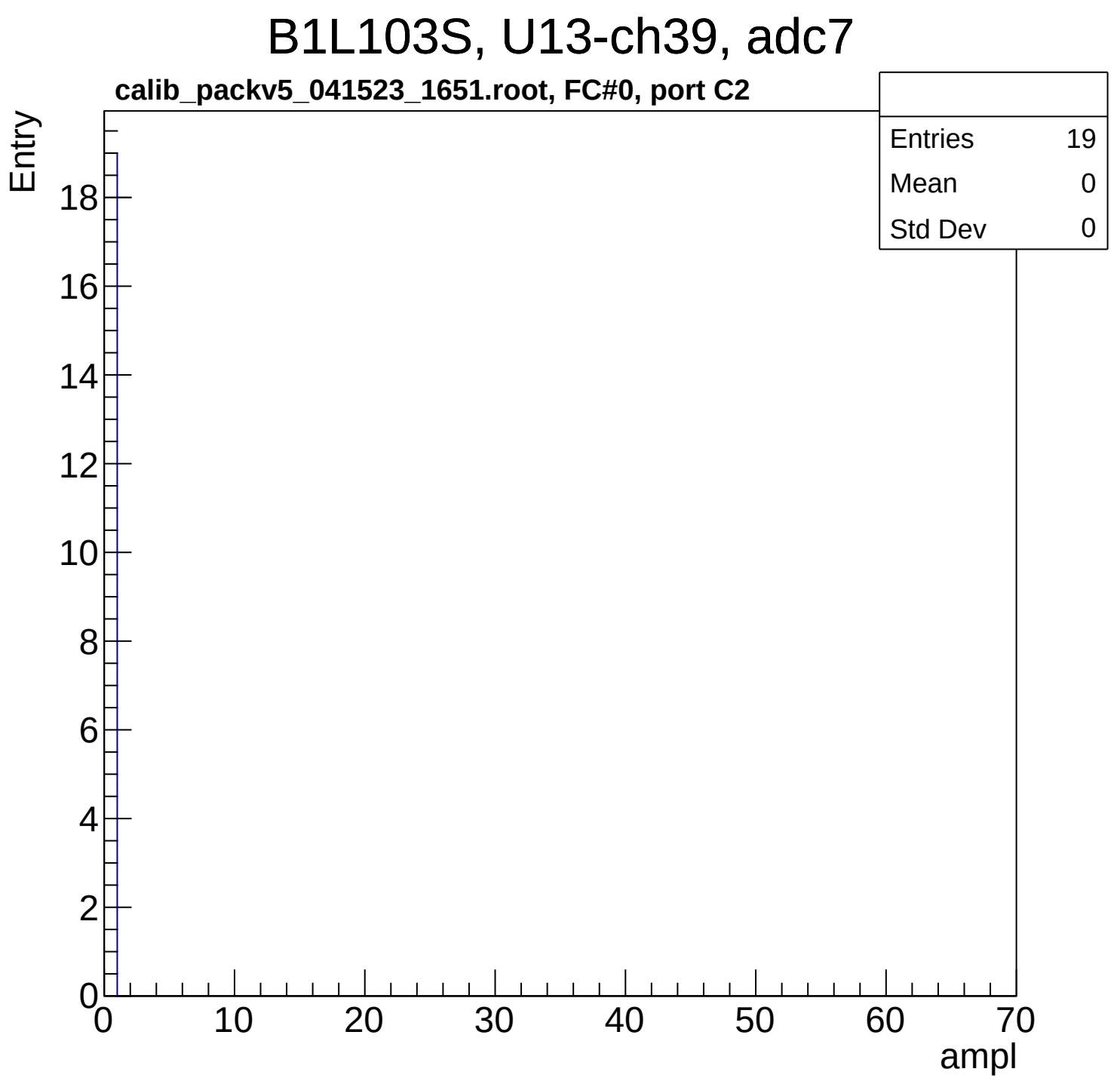

B1L103S, U13-ch39, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 38.44
Std Dev 13.51
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

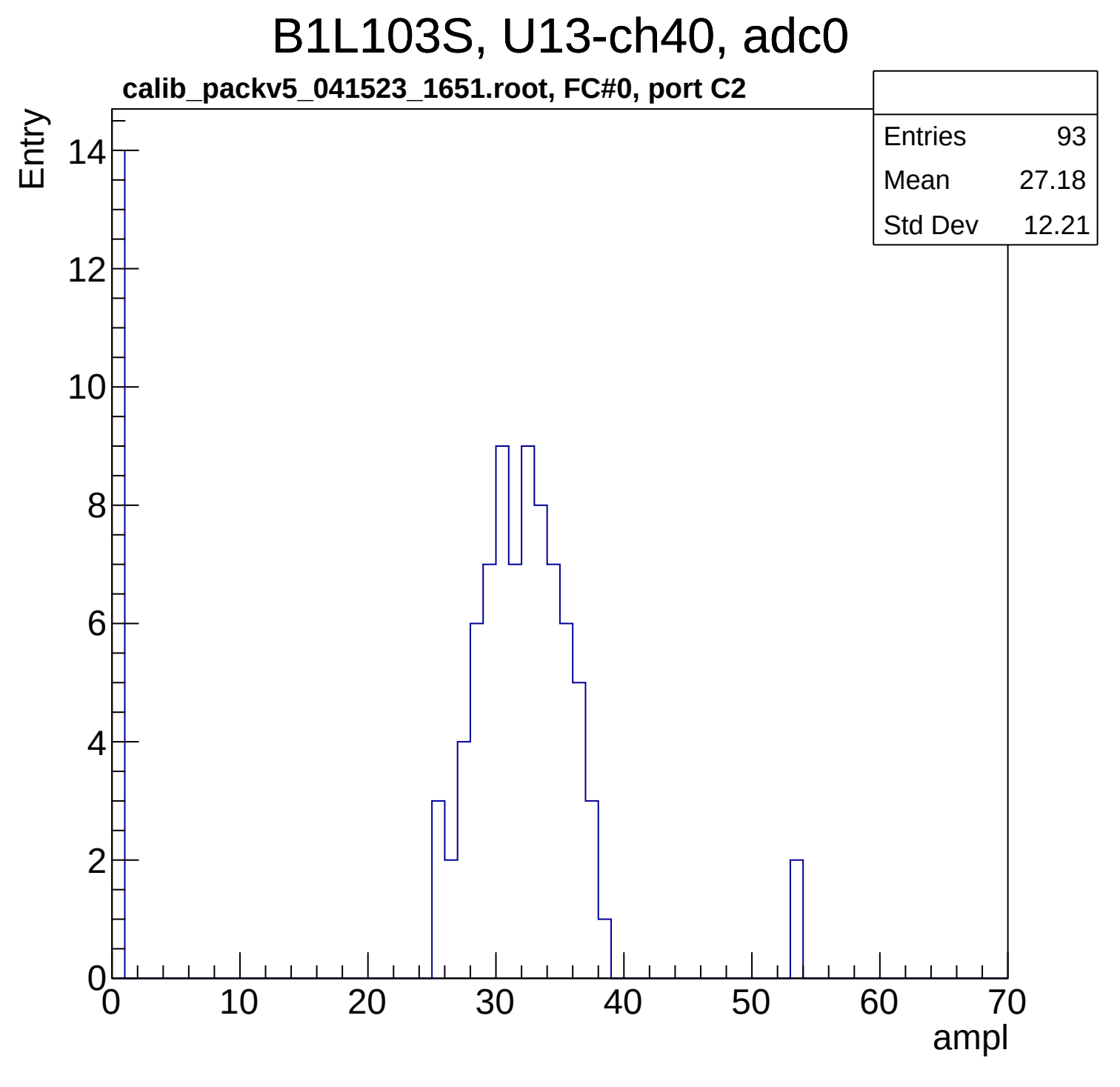

B1L103S, U13-ch39, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 48.3
Std Dev 9.119
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

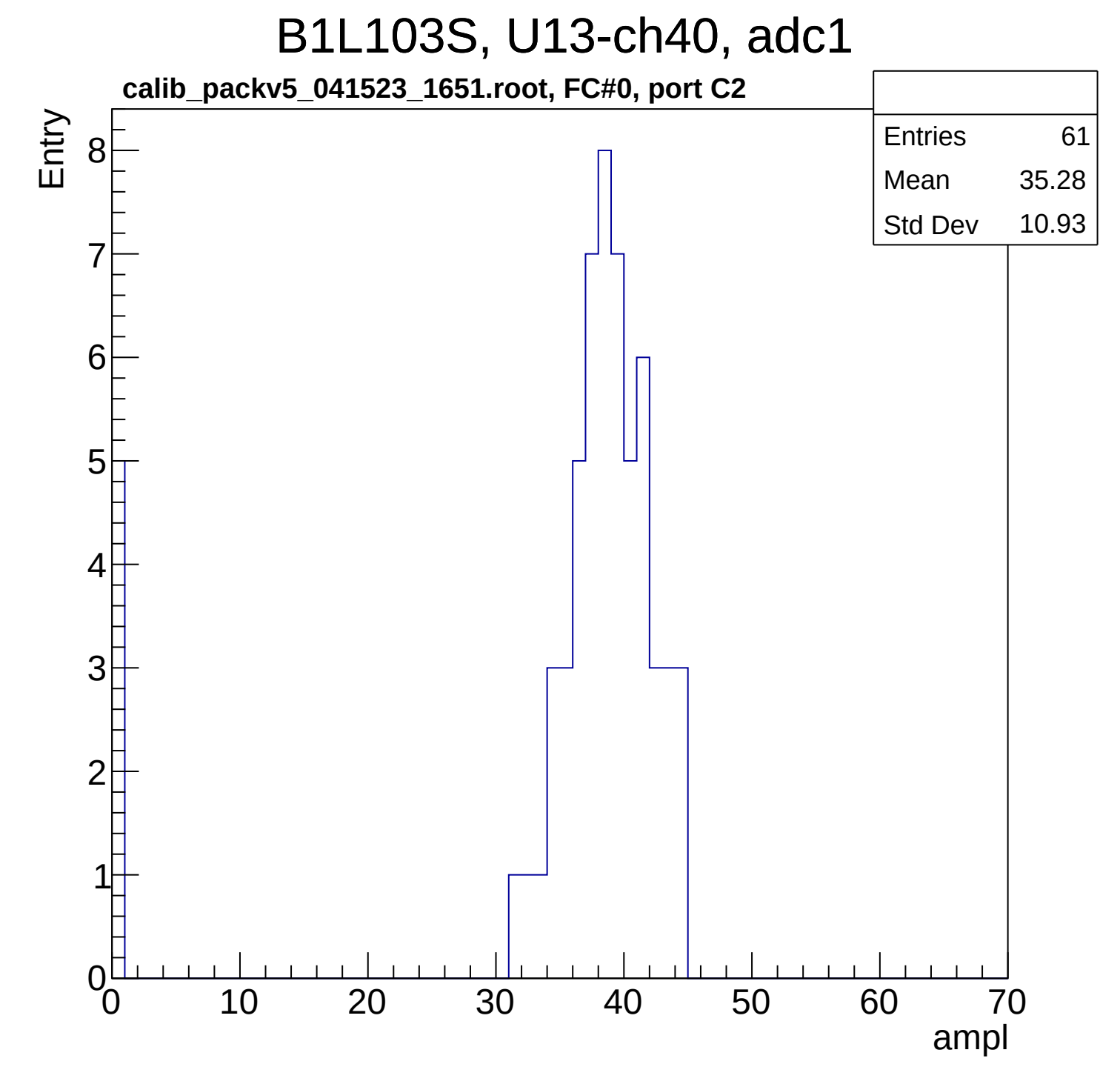

B1L103S, U13-ch39, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 56.57
Std Dev 3.101
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

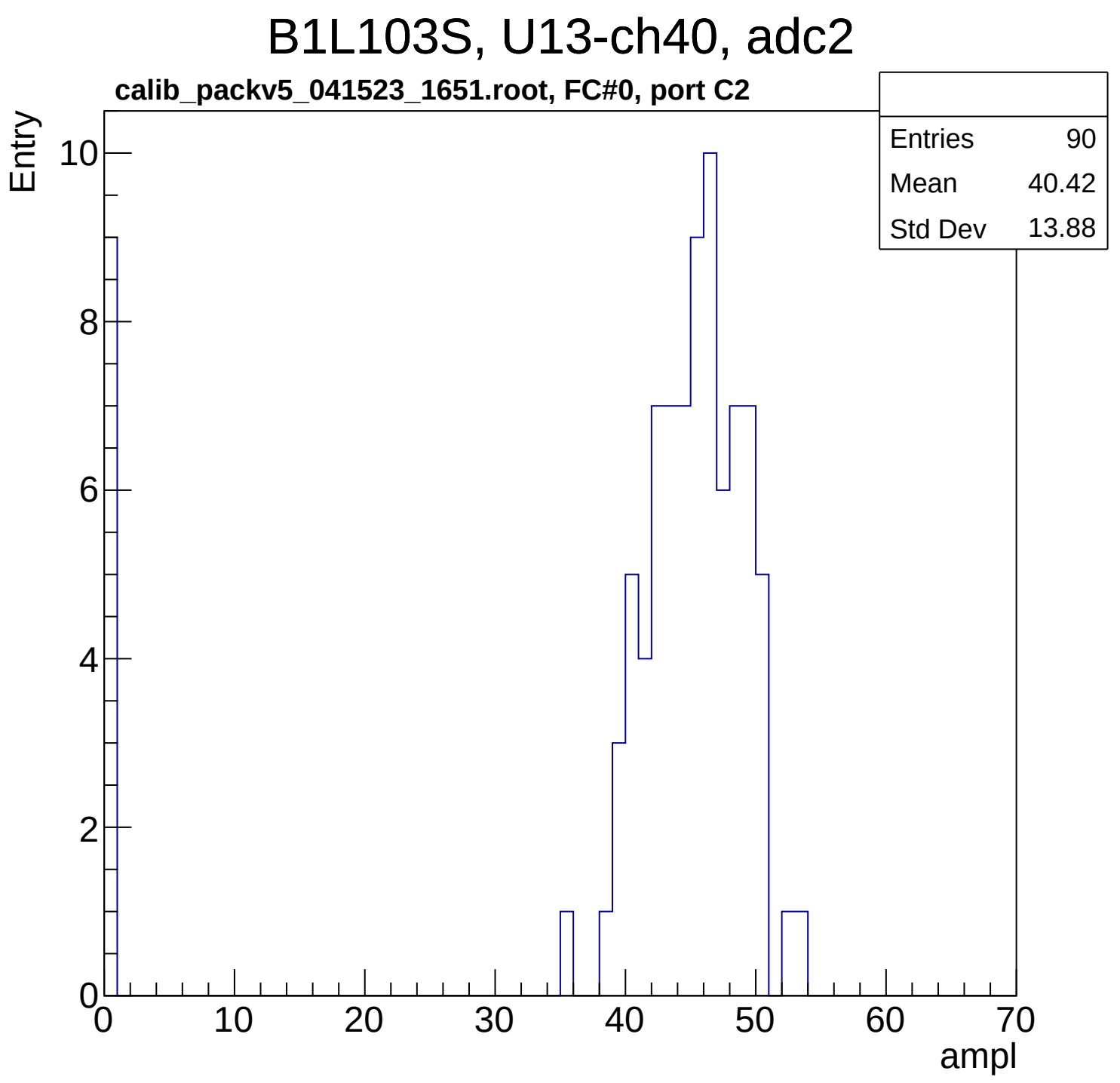

B1L103S, U13-ch39, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 58.97
Std Dev 10.32
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

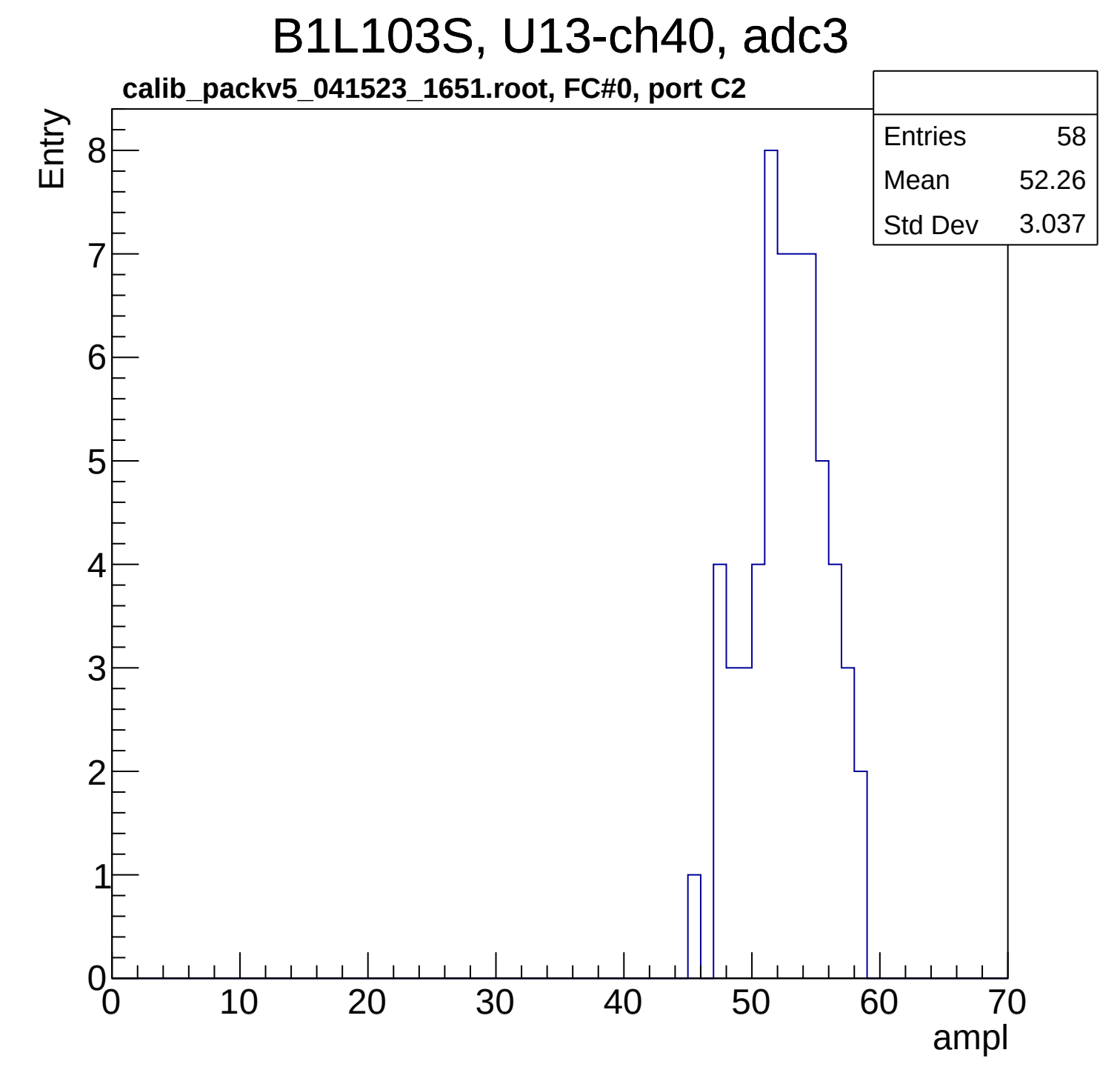

B1L103S, U13-ch39, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

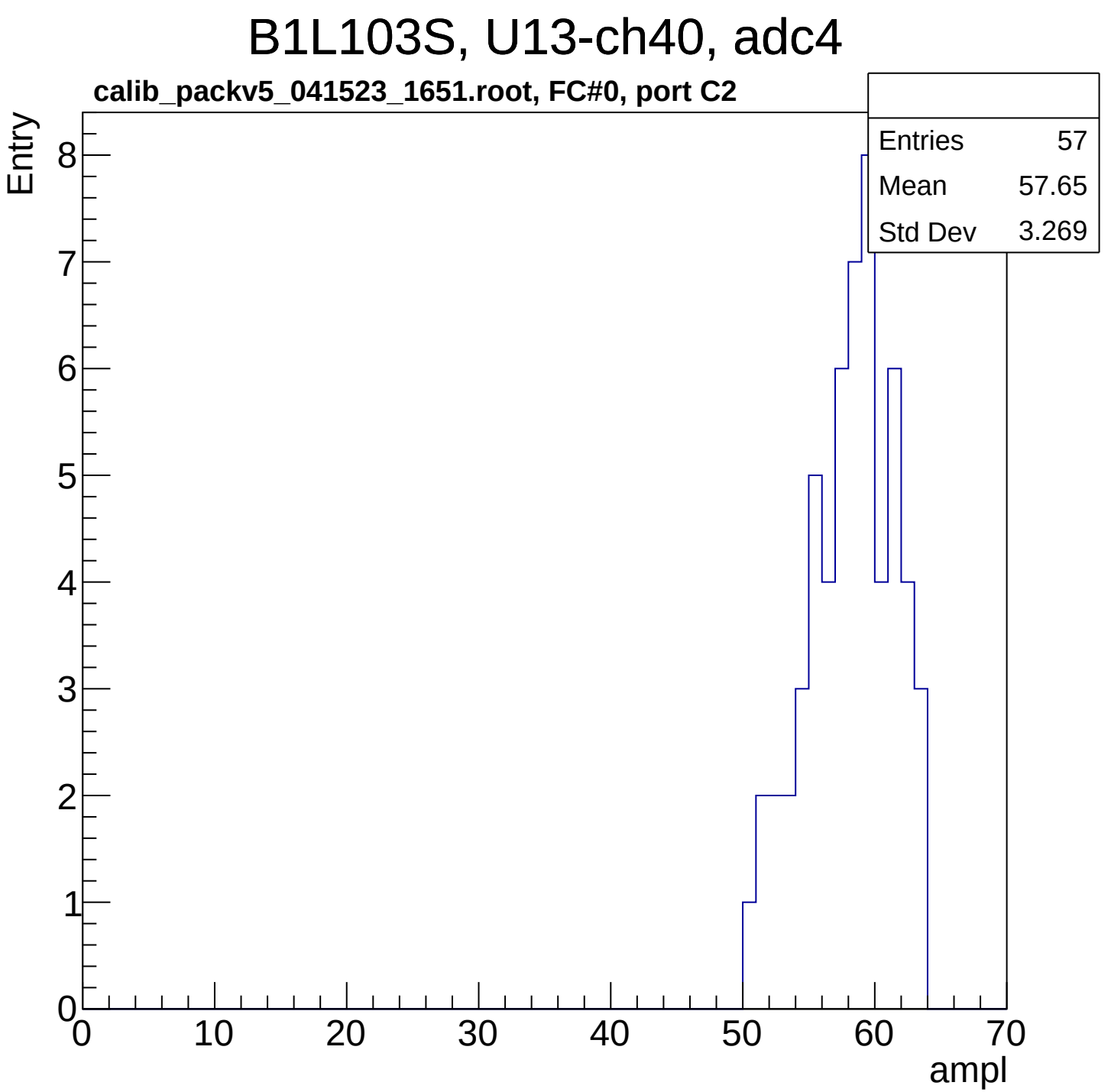

B1L103S, U13-ch39, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

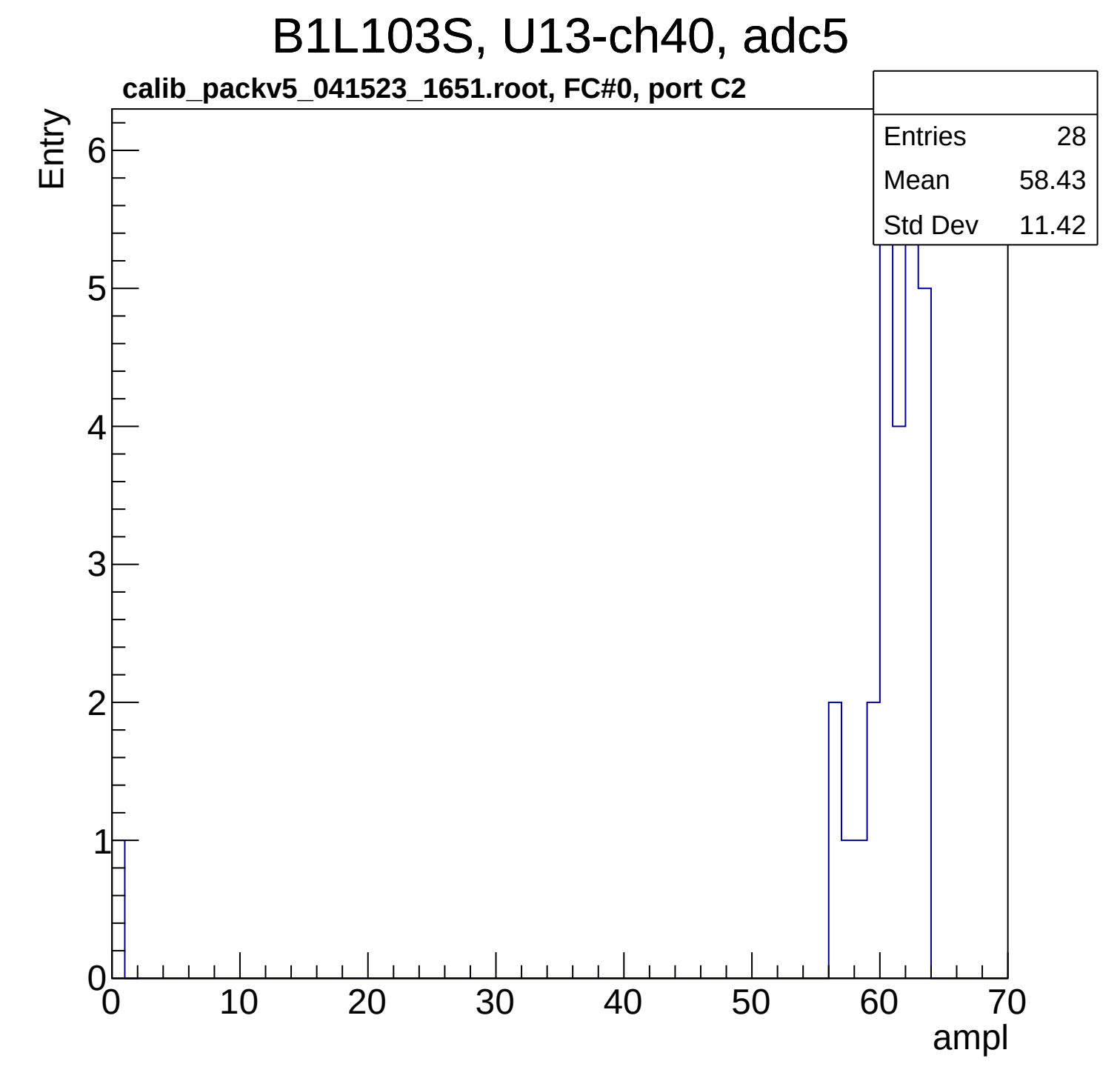

B1L103S, U13-ch40, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 27.18
Std Dev 12.21
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

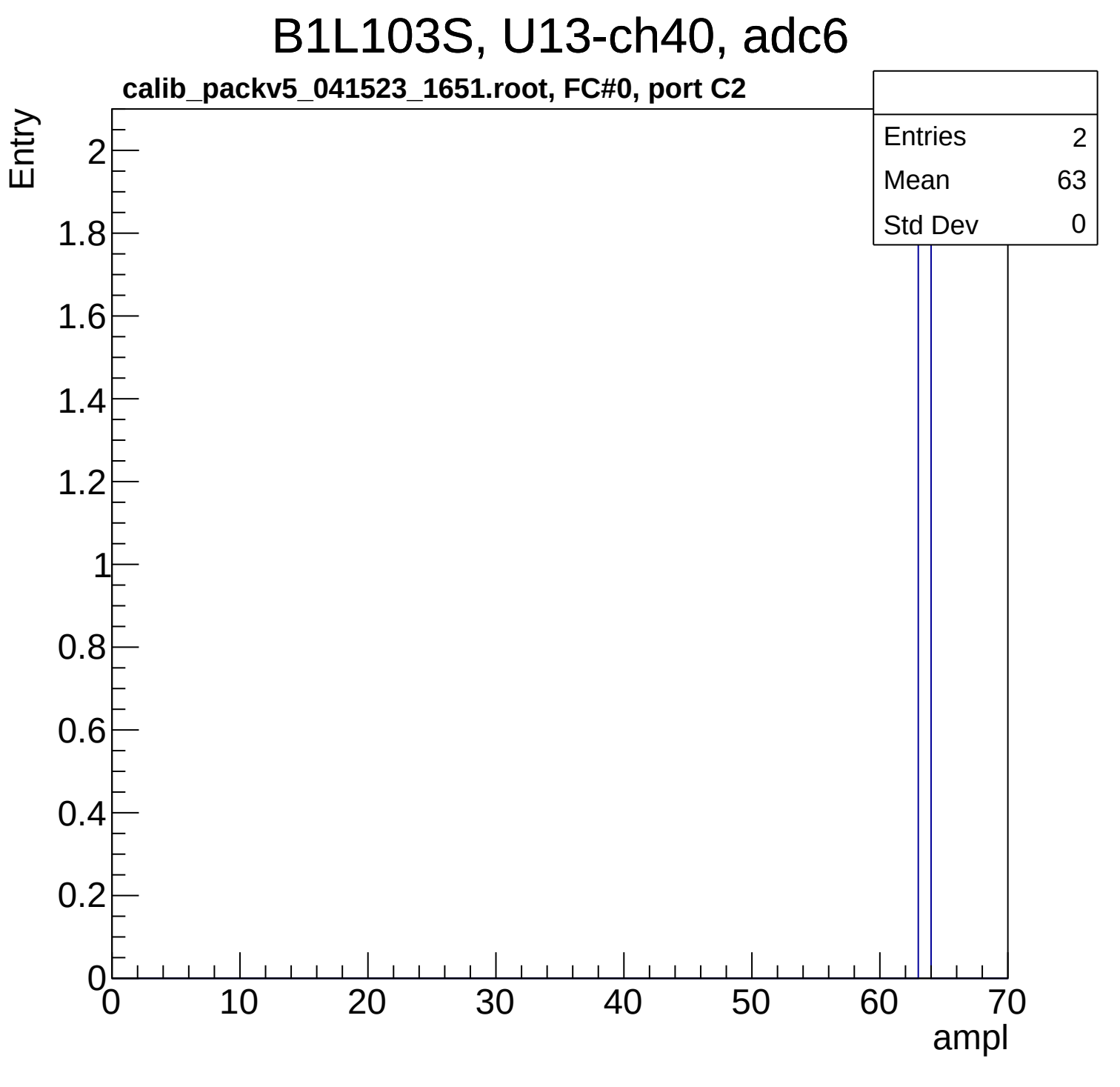

B1L103S, U13-ch40, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 35.28
Std Dev 10.93
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

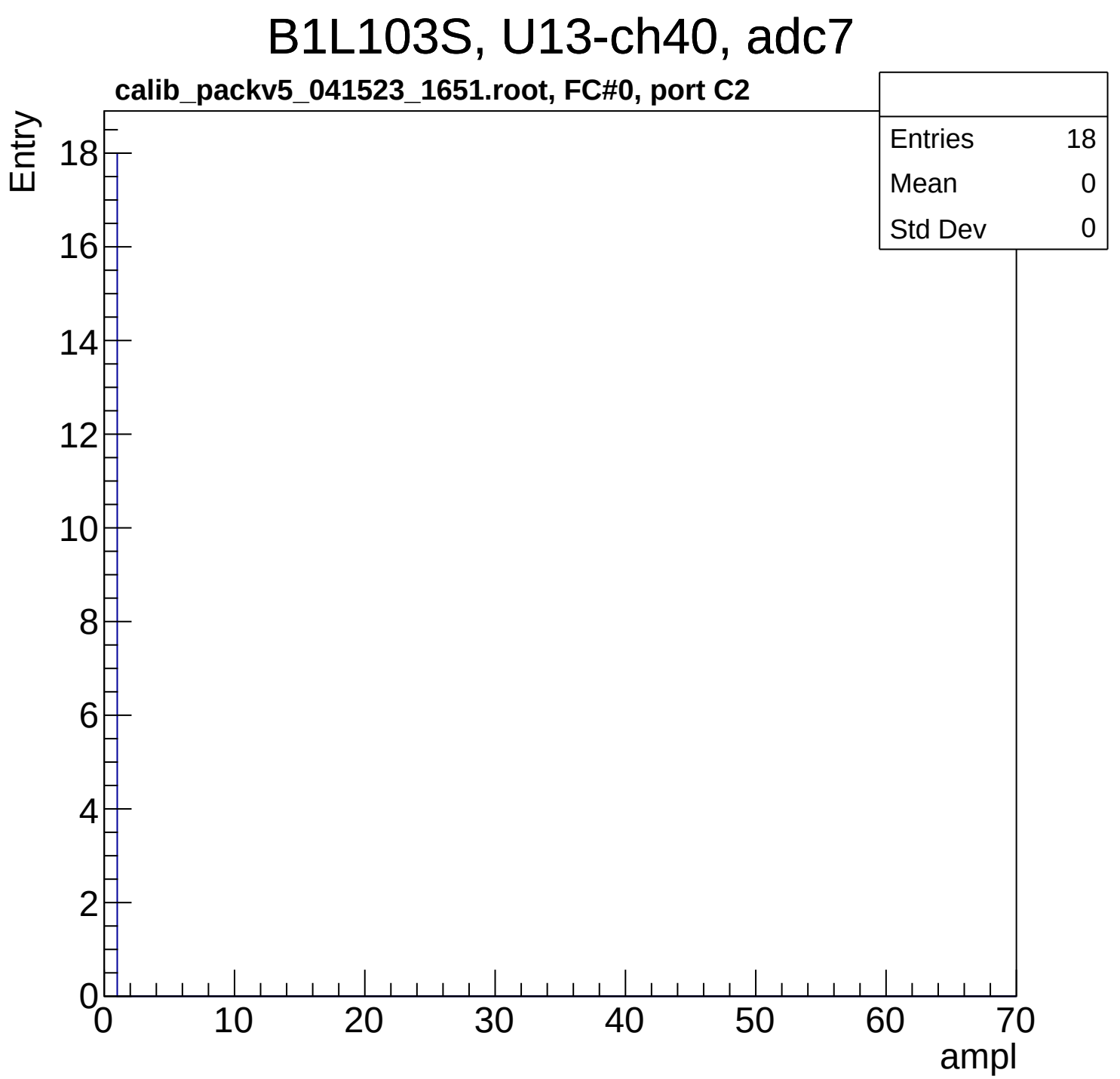

B1L103S, U13-ch40, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 40.42
Std Dev 13.88
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

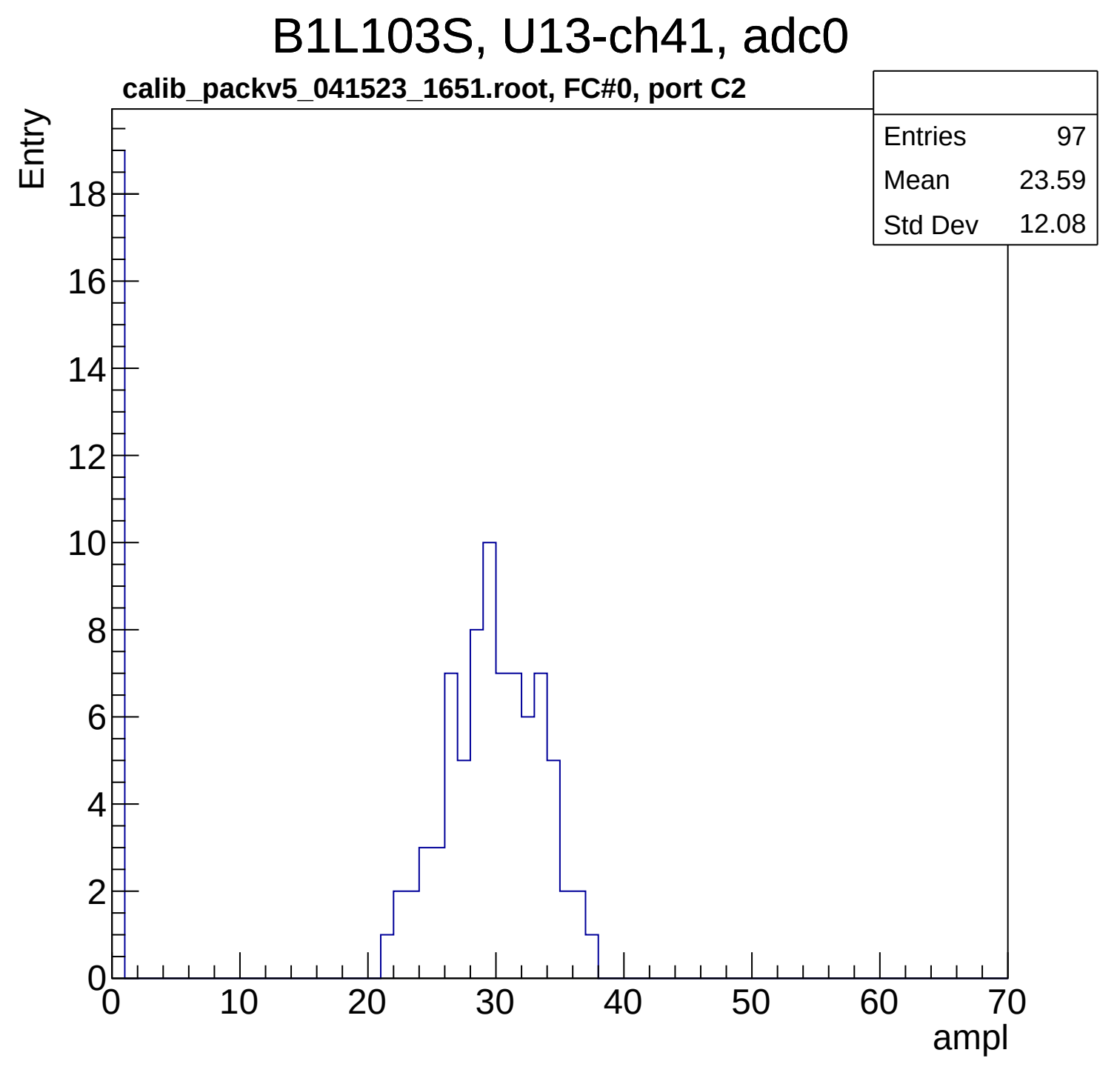

B1L103S, U13-ch40, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 52.26
Std Dev 3.037
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

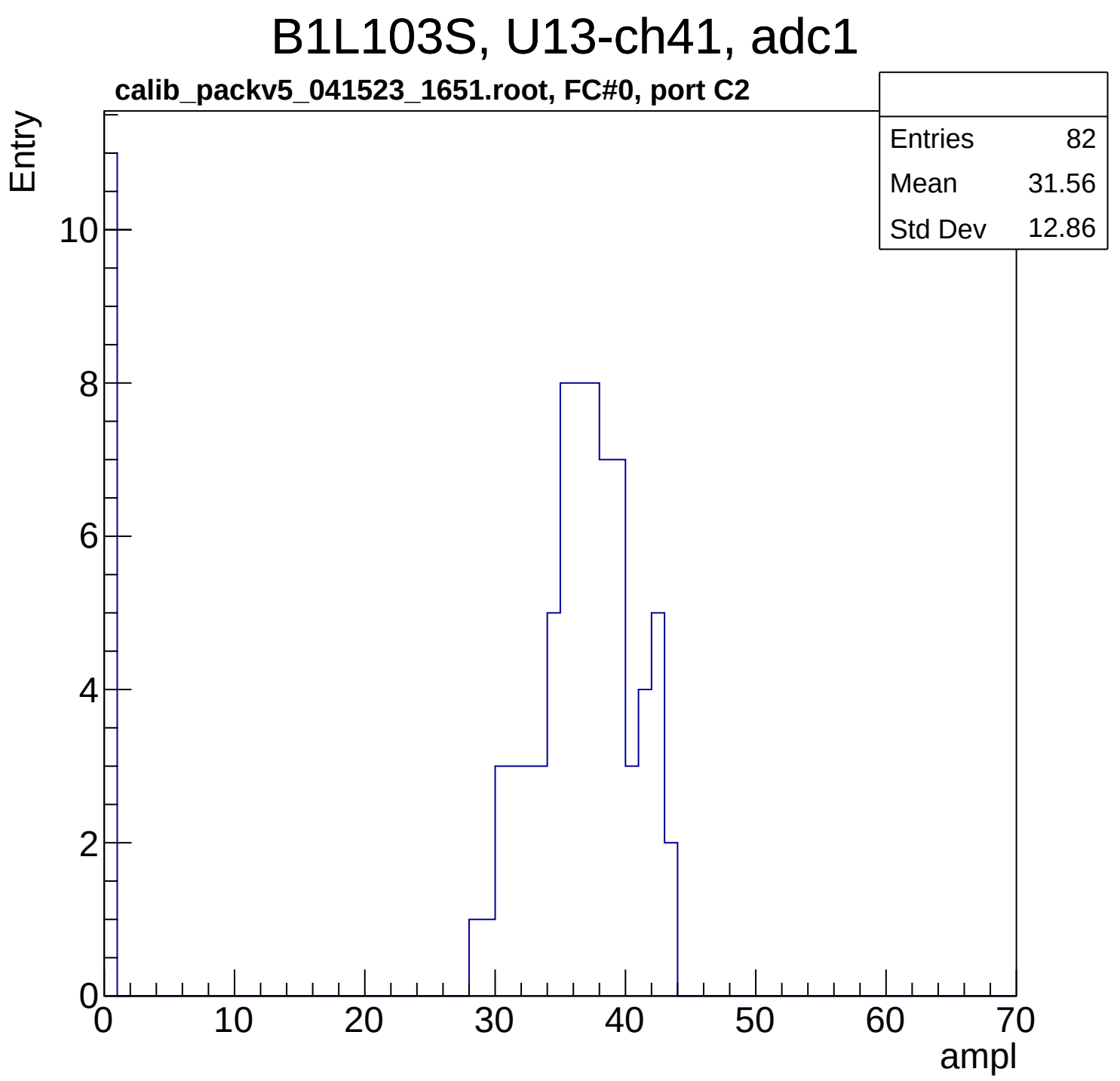

B1L103S, U13-ch40, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 57.65
Std Dev 3.269
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

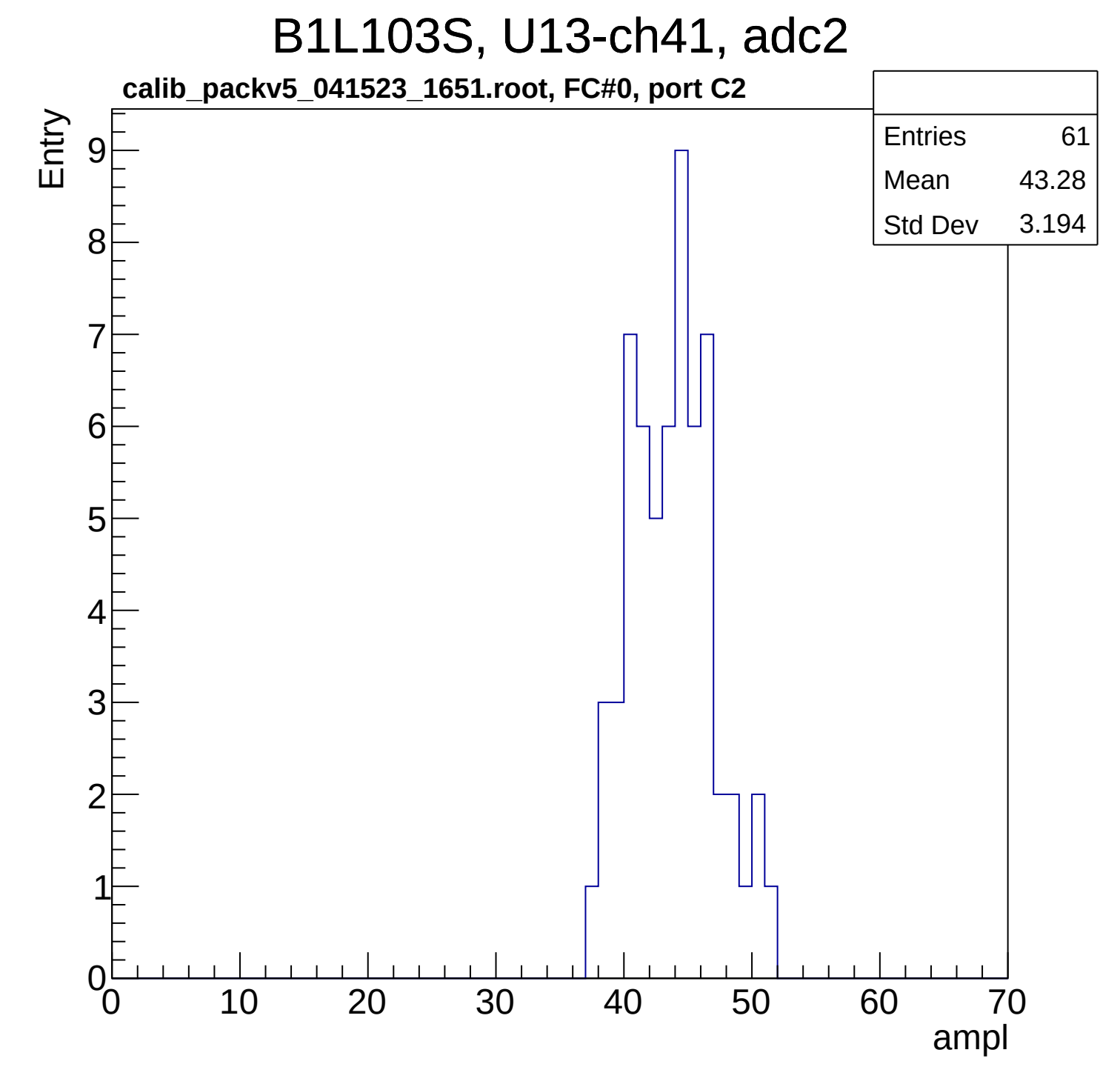

B1L103S, U13-ch40, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 58.43
Std Dev 11.42
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

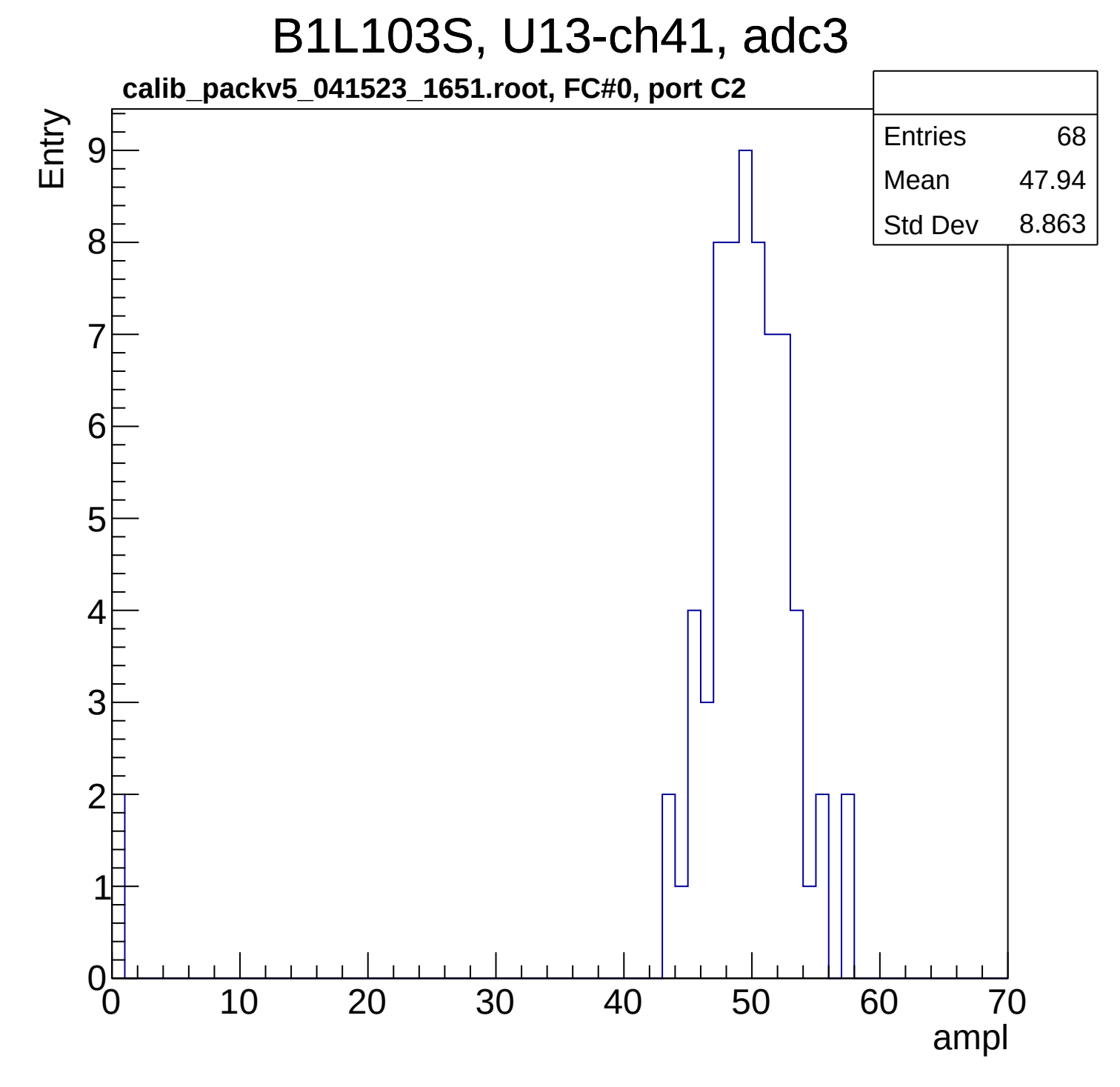

B1L103S, U13-ch40, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U13-ch40, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch41, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 23.59
Std Dev 12.08
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch41, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 31.56
Std Dev 12.86
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch41, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 43.28
Std Dev 3.194
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch41, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 47.94
Std Dev 8.863
Entry
ampl
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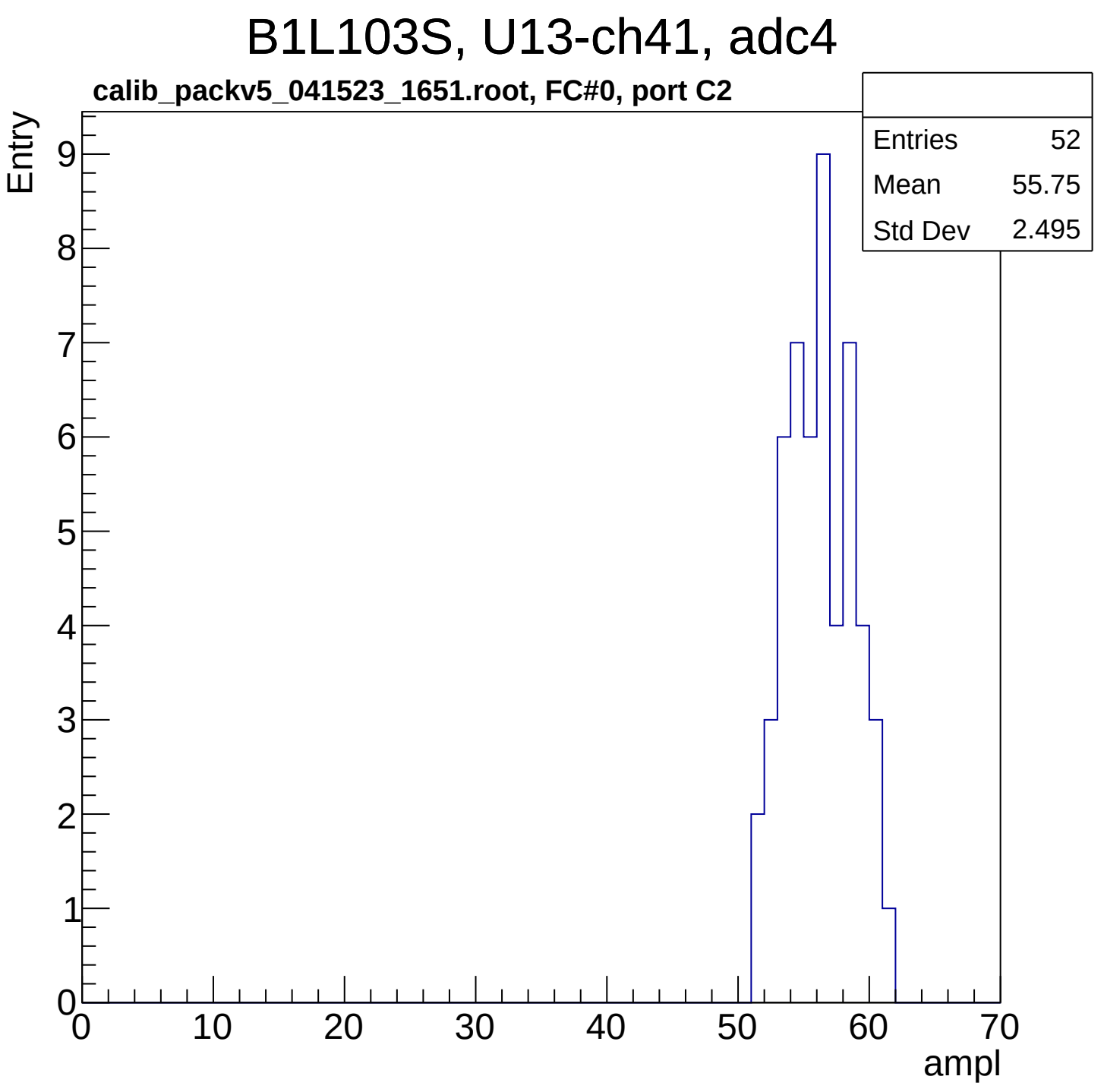
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch41, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 55.75
Std Dev 2.495
Entry
ampl
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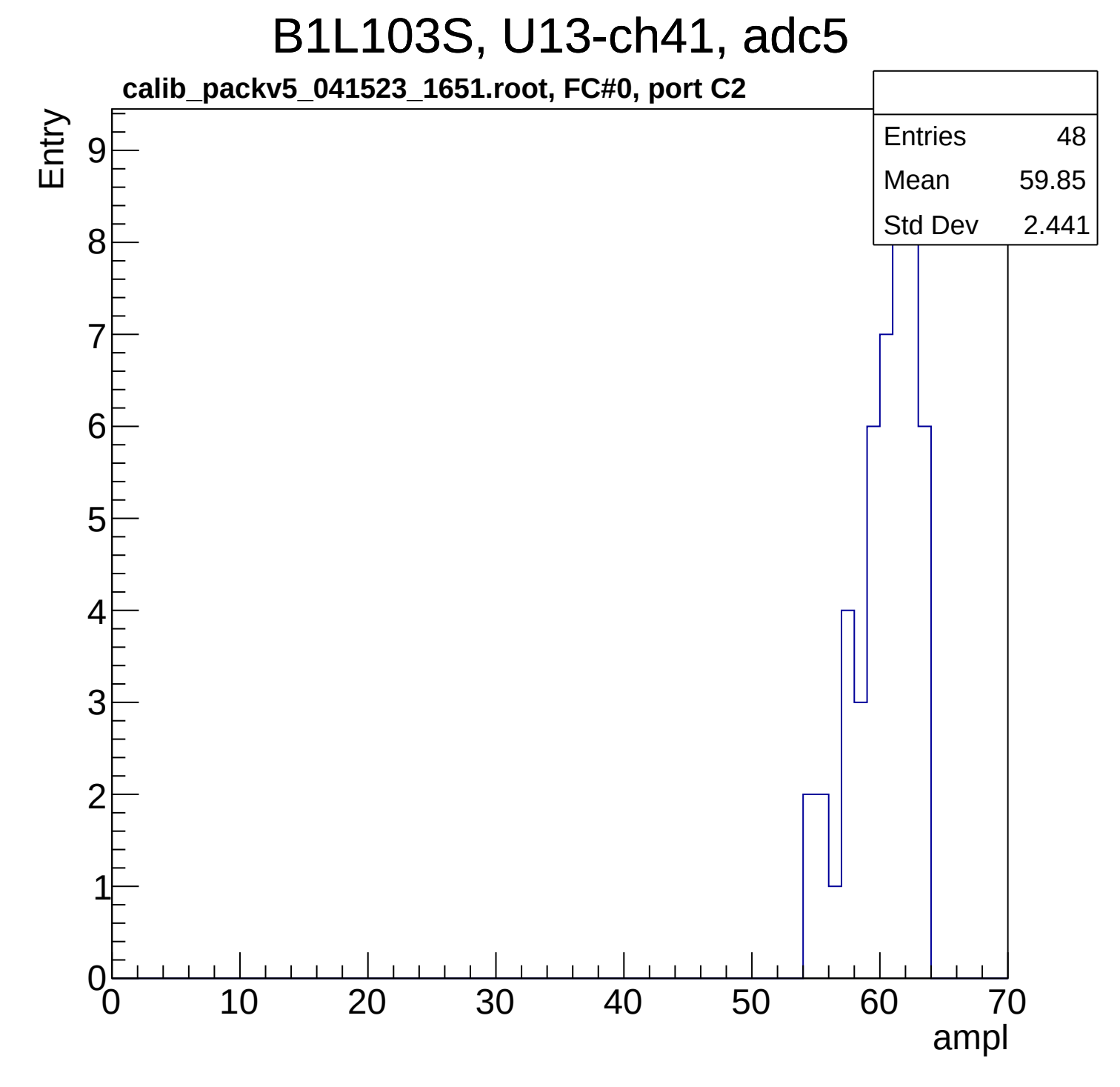
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch41, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 59.85
Std Dev 2.441
Entry
ampl
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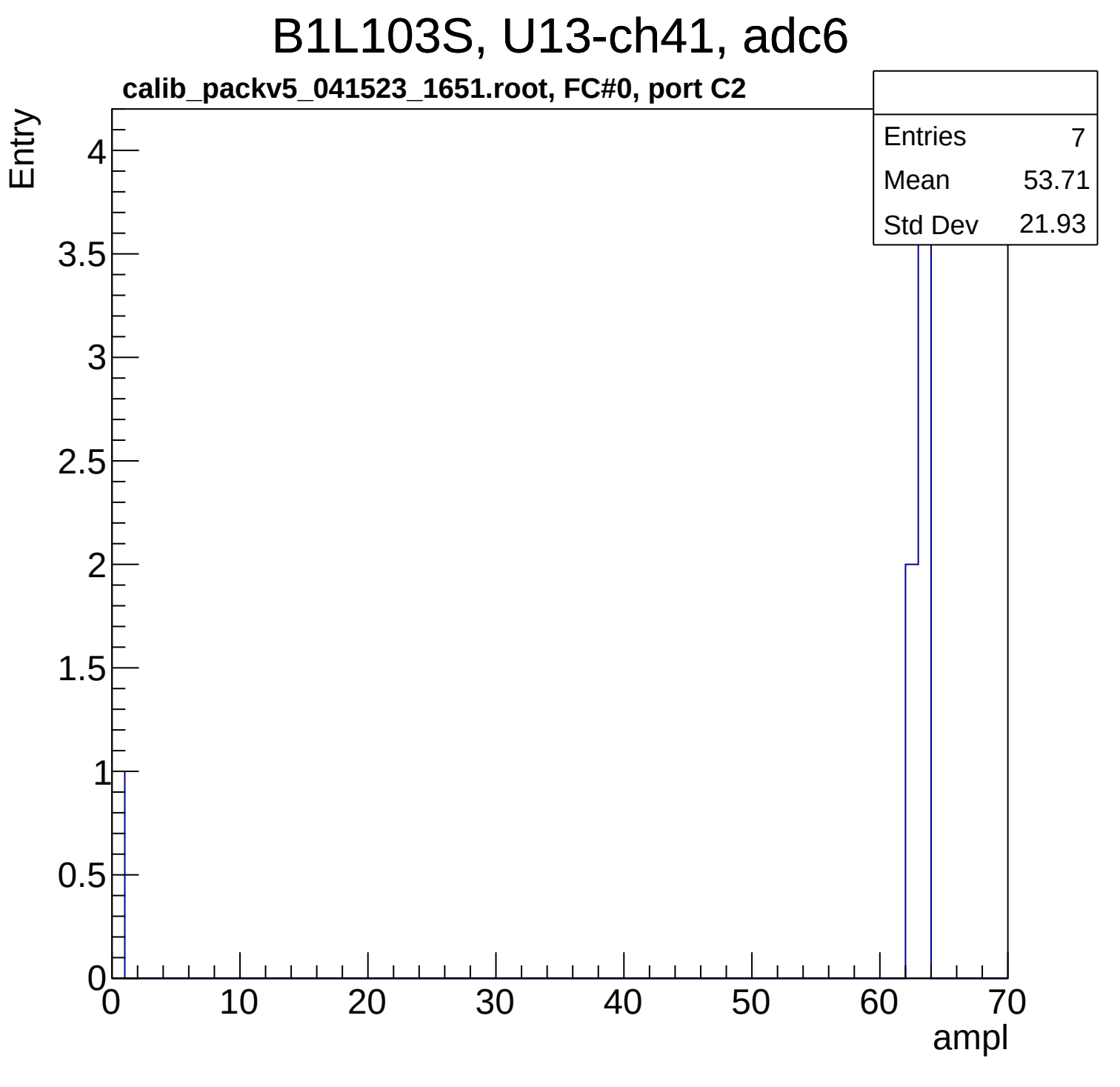
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch41, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 53.71
Std Dev 21.93
Entry
ampl
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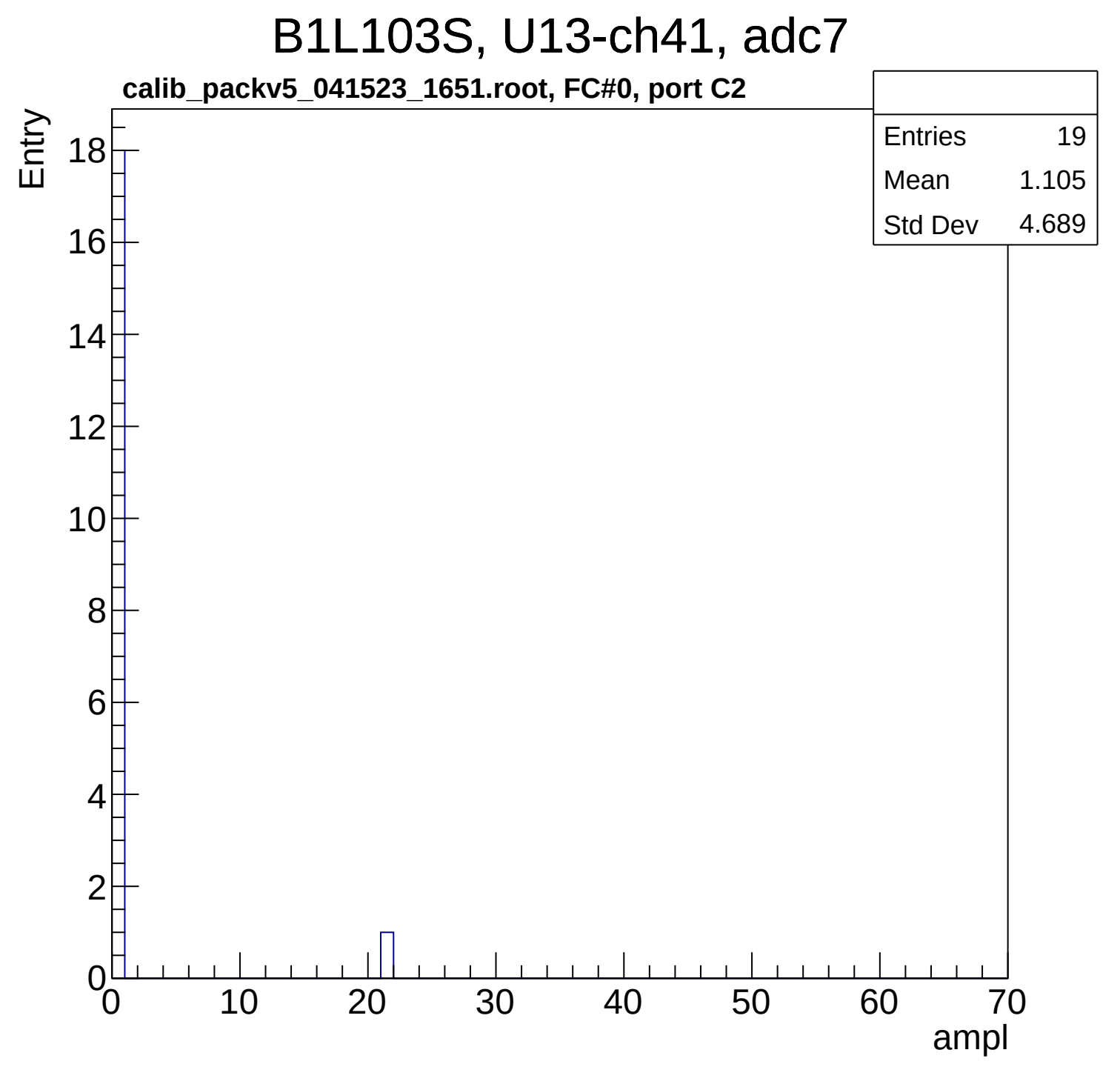
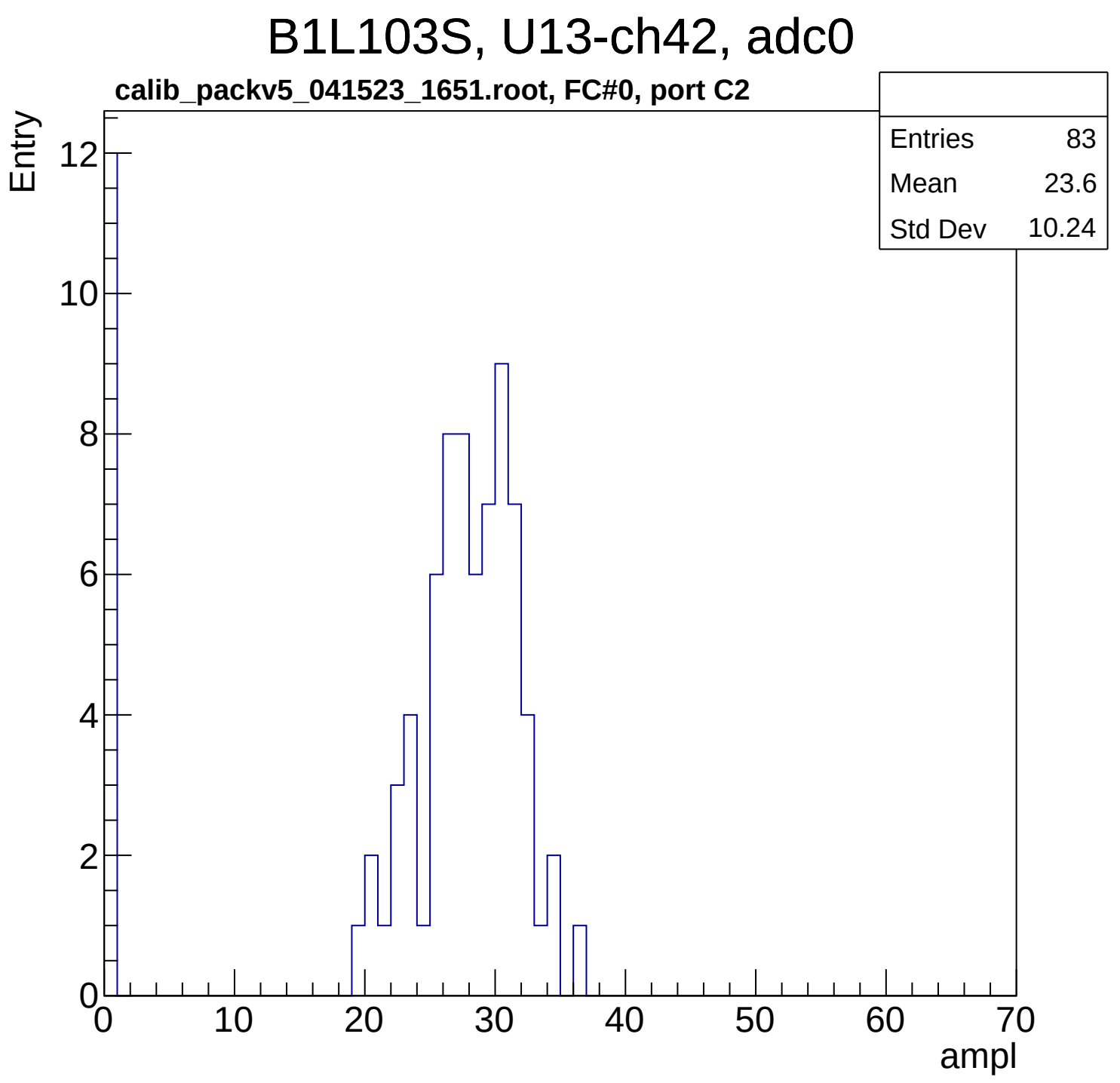
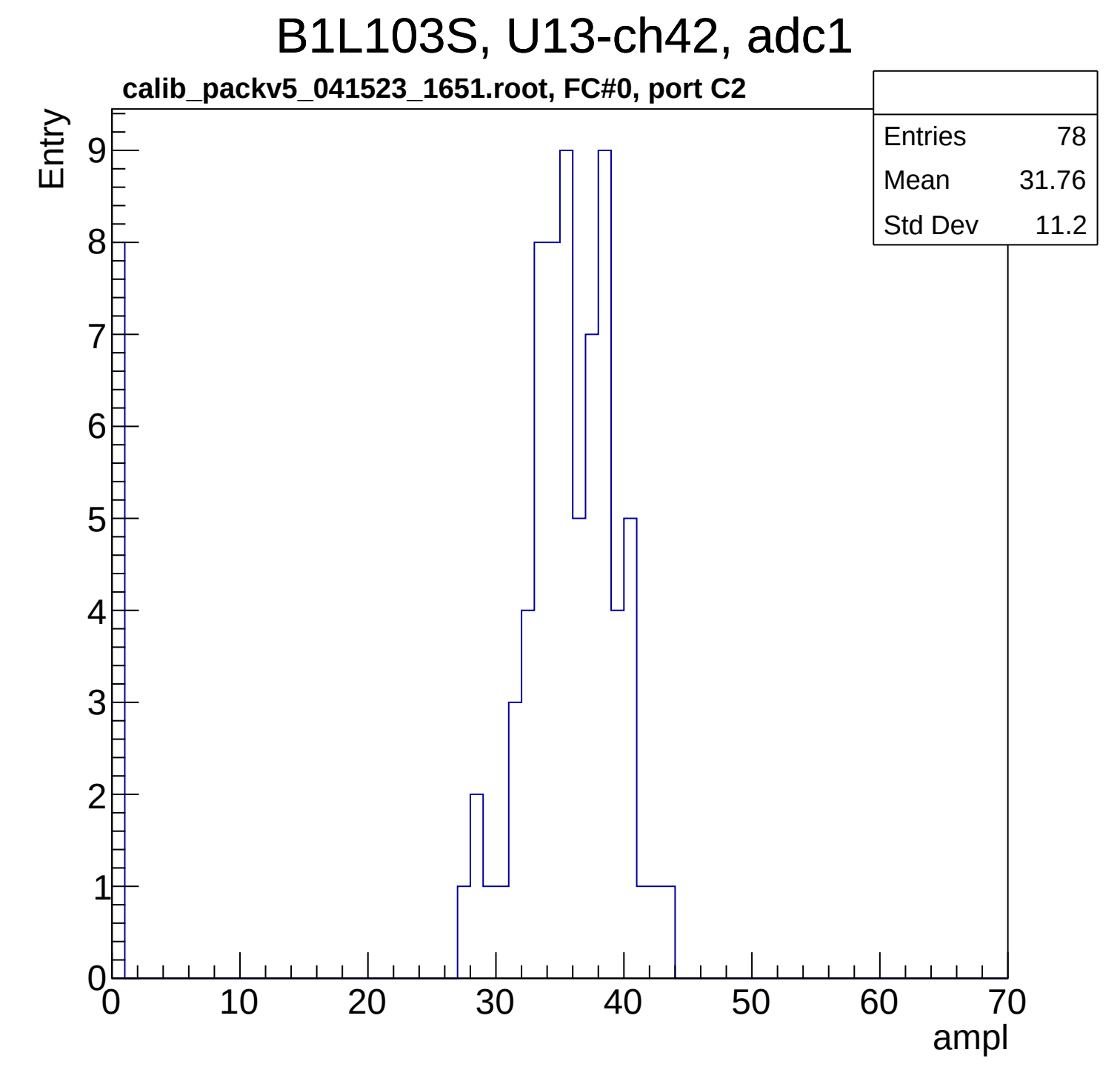
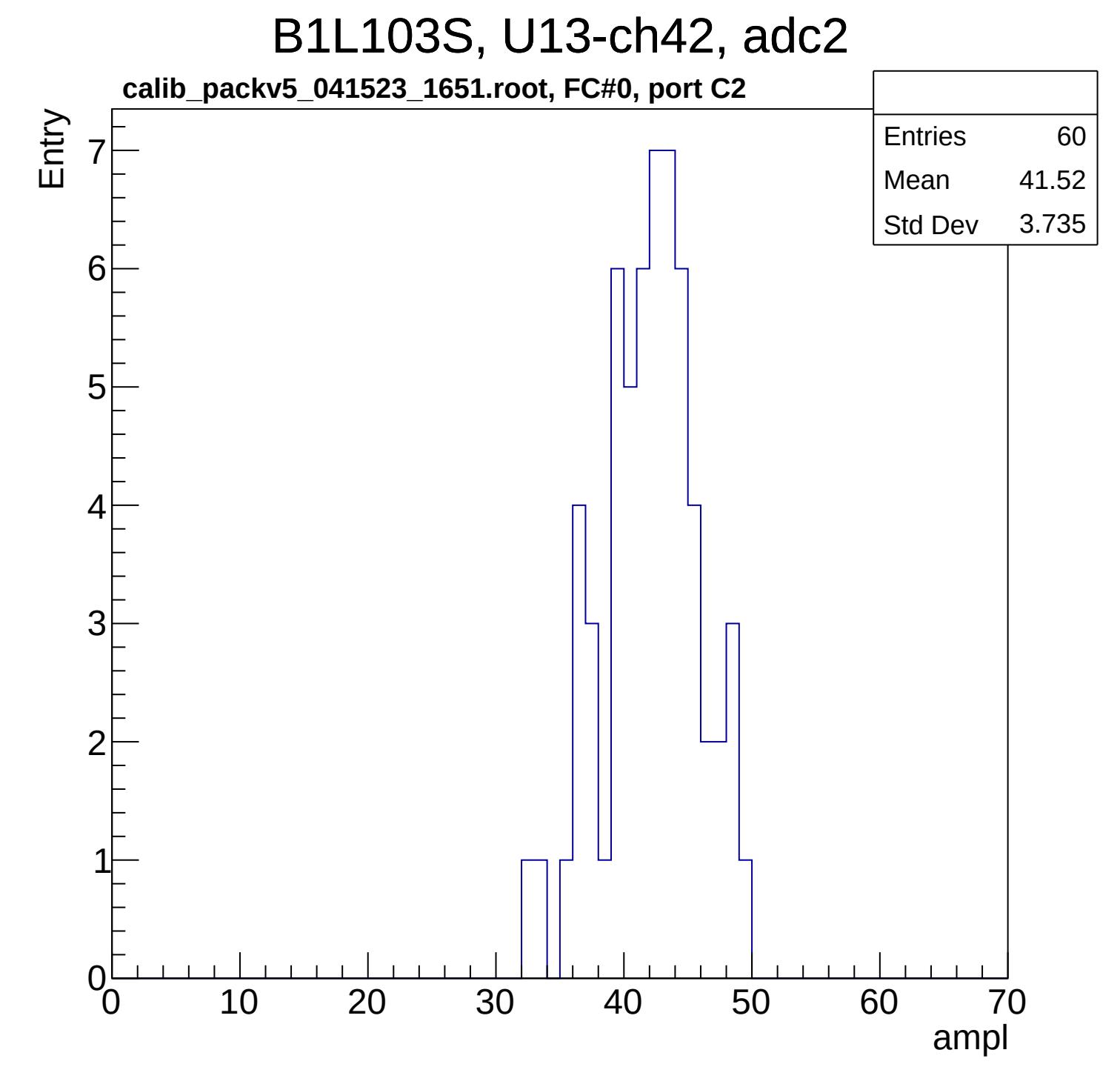
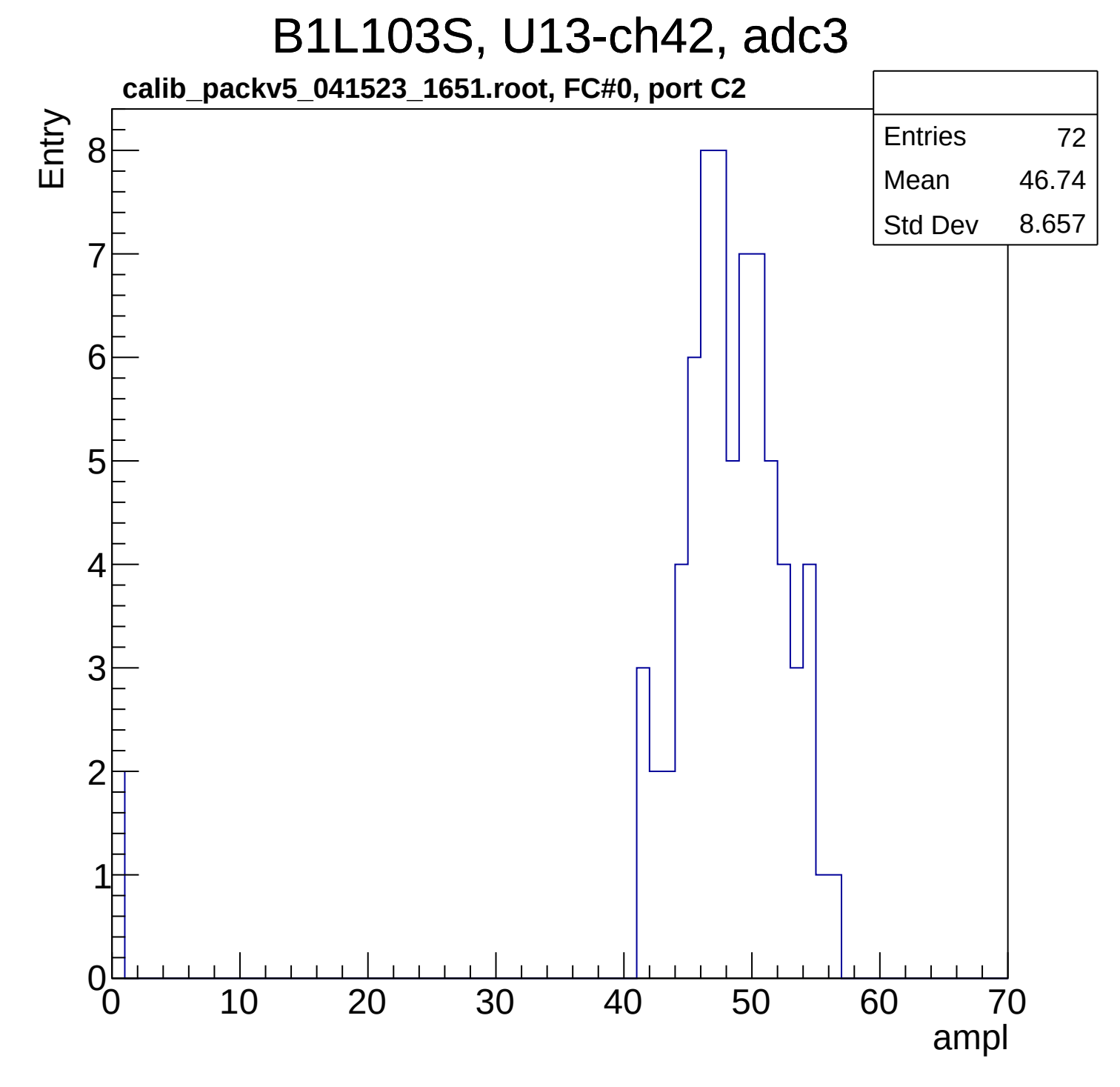
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U13-ch41, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch42, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 23.6
Std Dev 10.24
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch42, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 31.76
Std Dev 11.2
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch42, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 41.52
Std Dev 3.735
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch42, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 46.74
Std Dev 8.657
Entry
ampl
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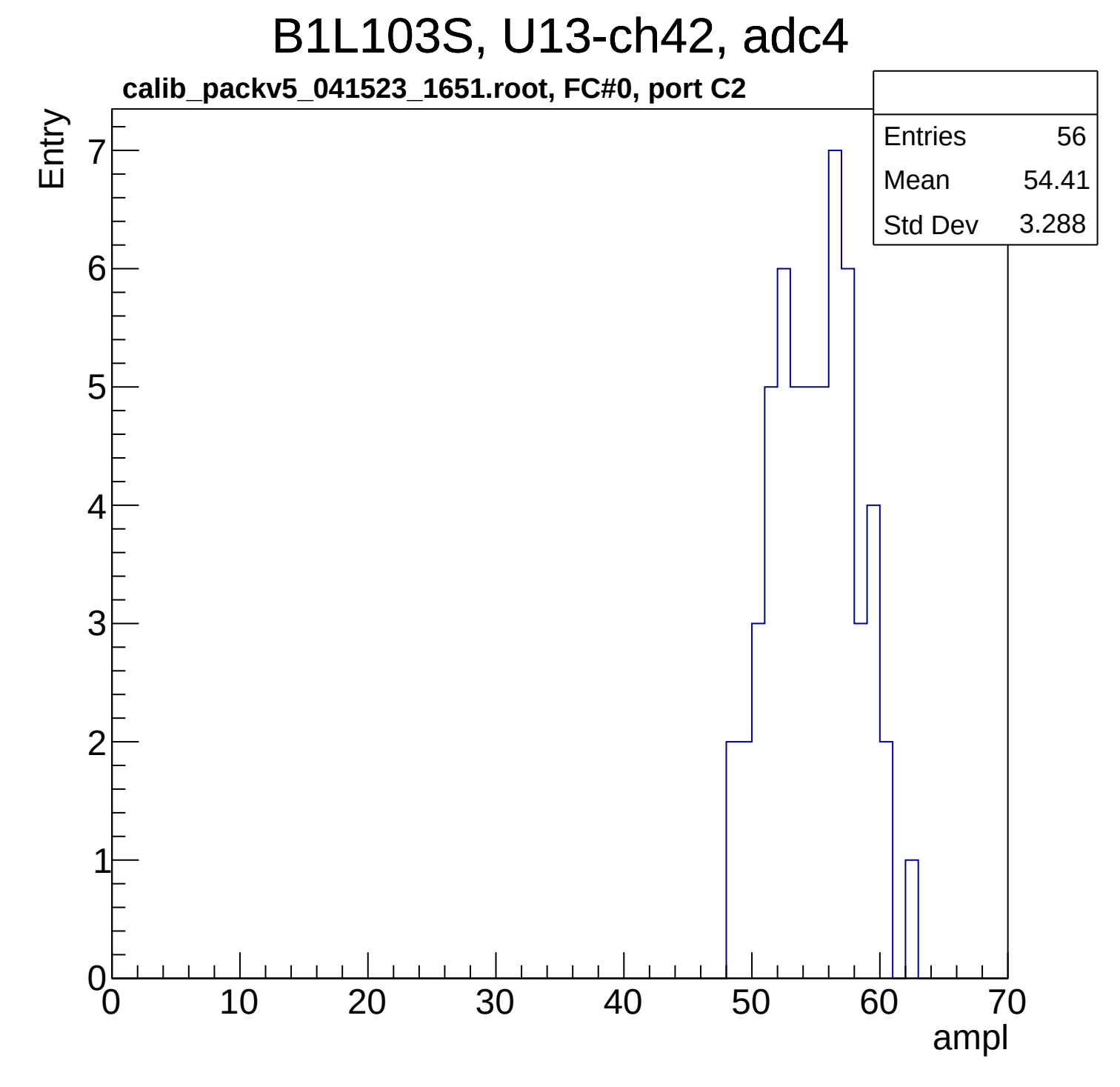
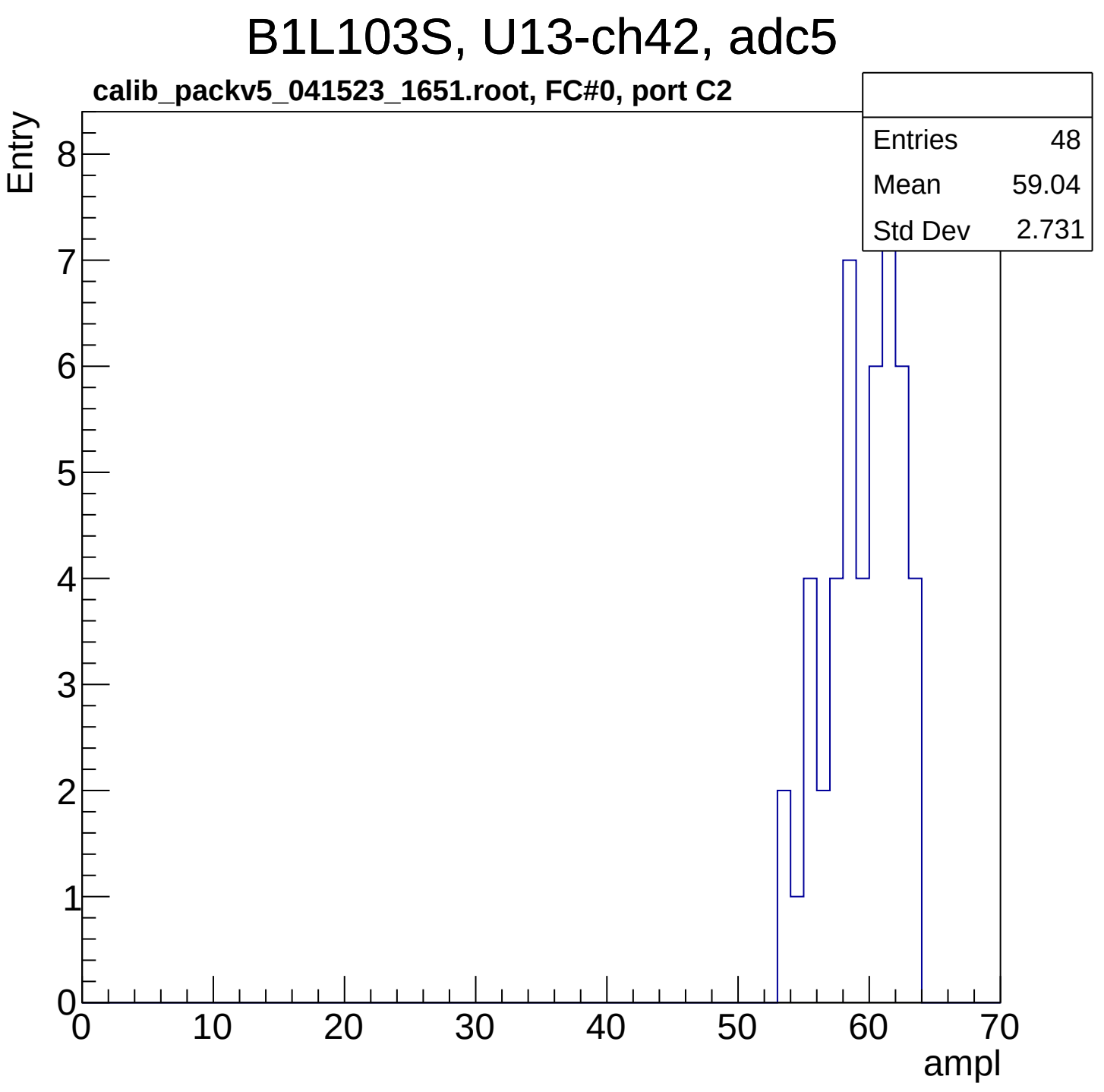
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch42, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 54.41
Std Dev 3.288
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch42, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 59.04
Std Dev 2.731
Entry
ampl
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1
2
3
4
5
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7
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0
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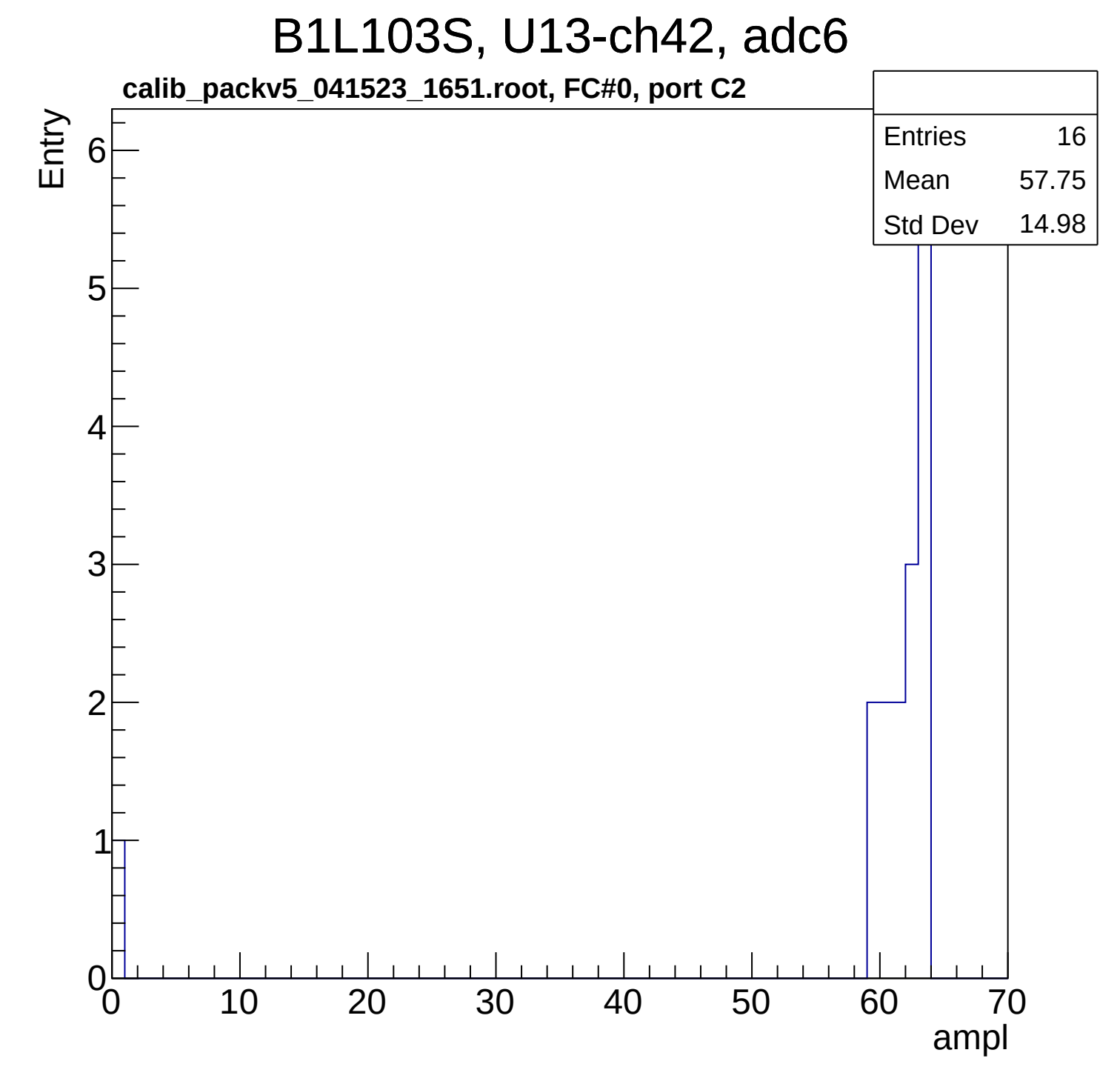
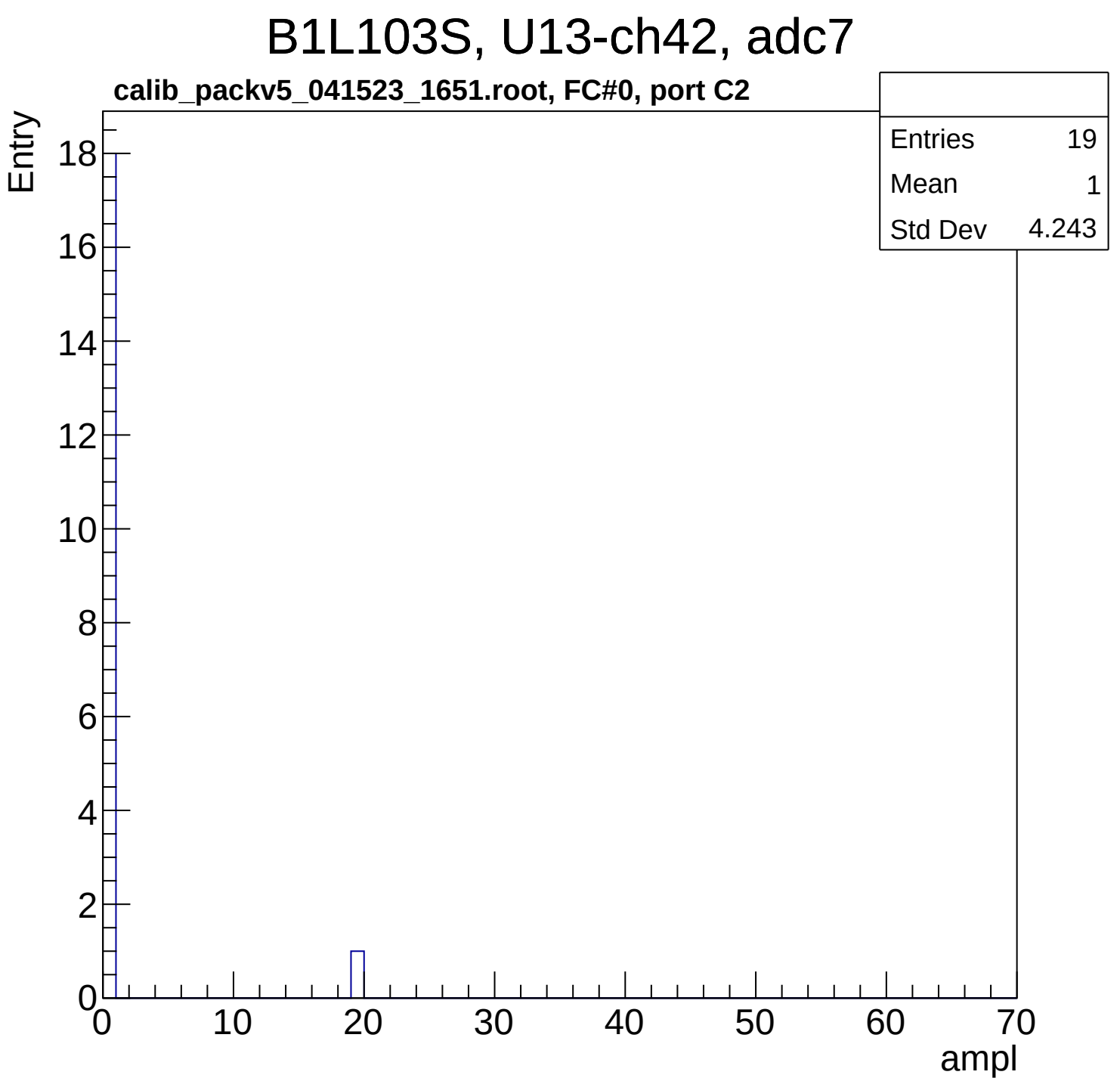

B1L103S, U13-ch42, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.75
Std Dev 14.98
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch42, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1
Std Dev 4.243
Entry
0
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6
8
10
12
14
16
18
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10
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50
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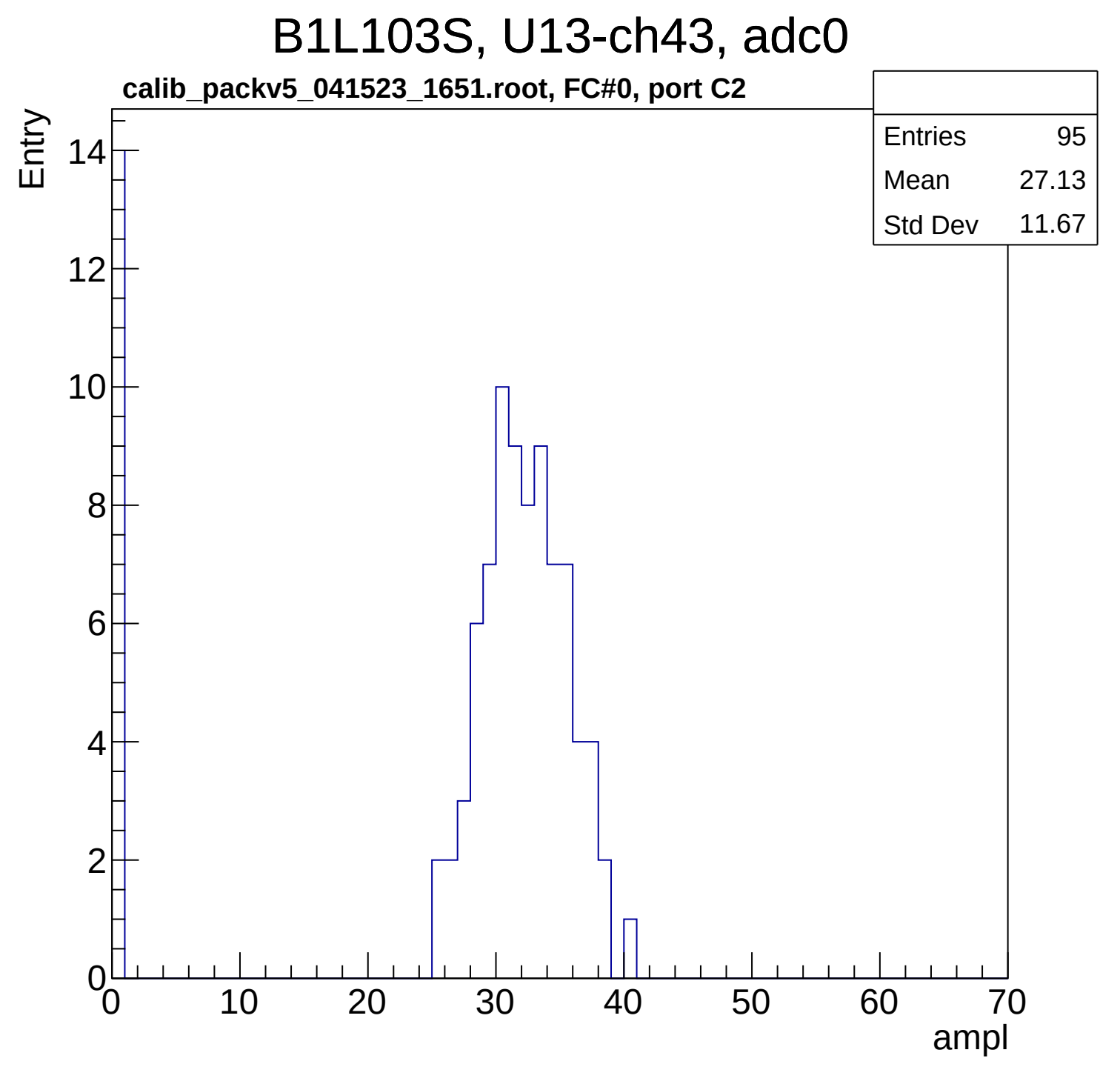
70
ampl


B1L103S, U13-ch43, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 27.13
Std Dev 11.67
Entry
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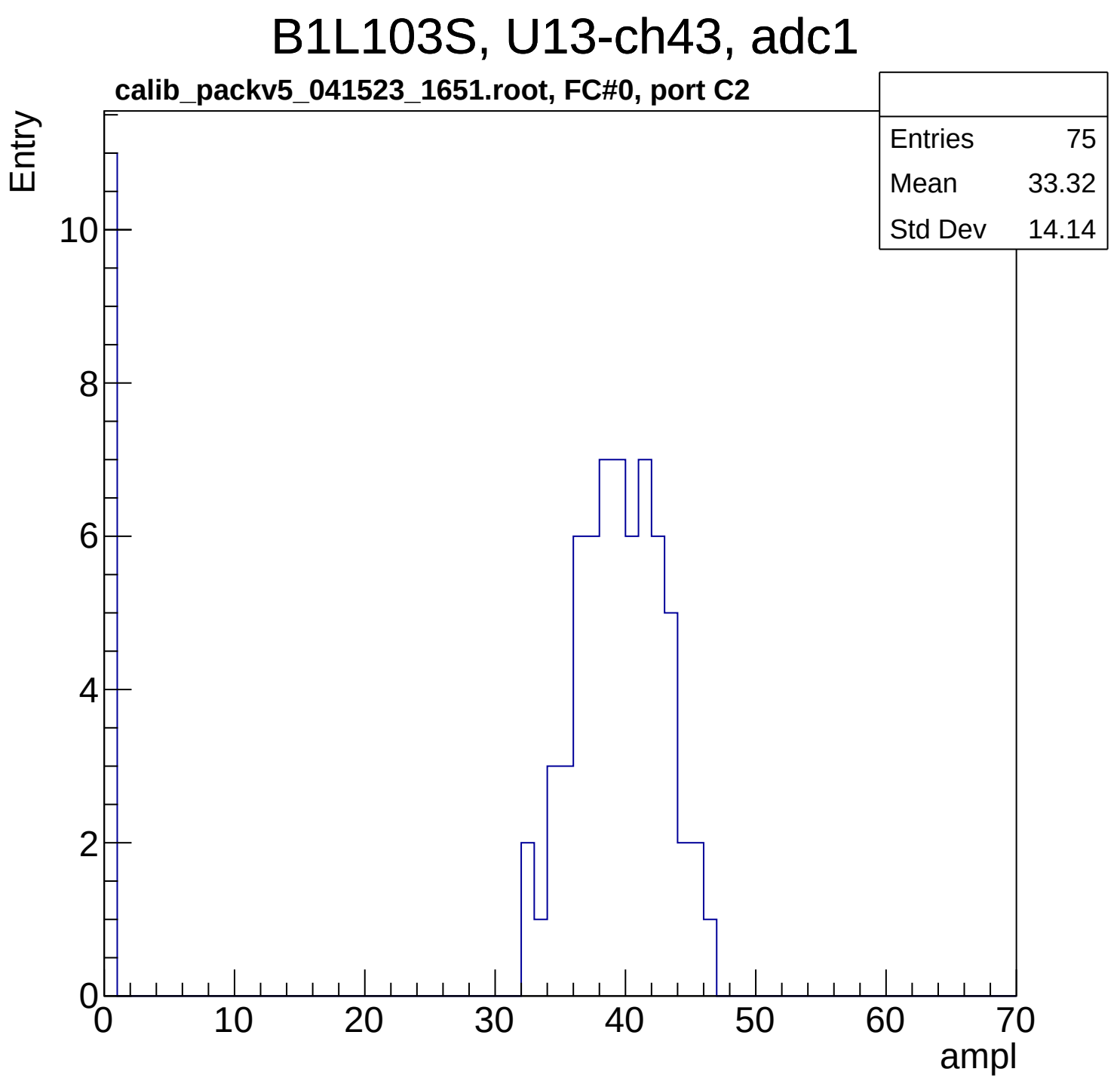
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch43, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 33.32
Std Dev 14.14
Entry
0
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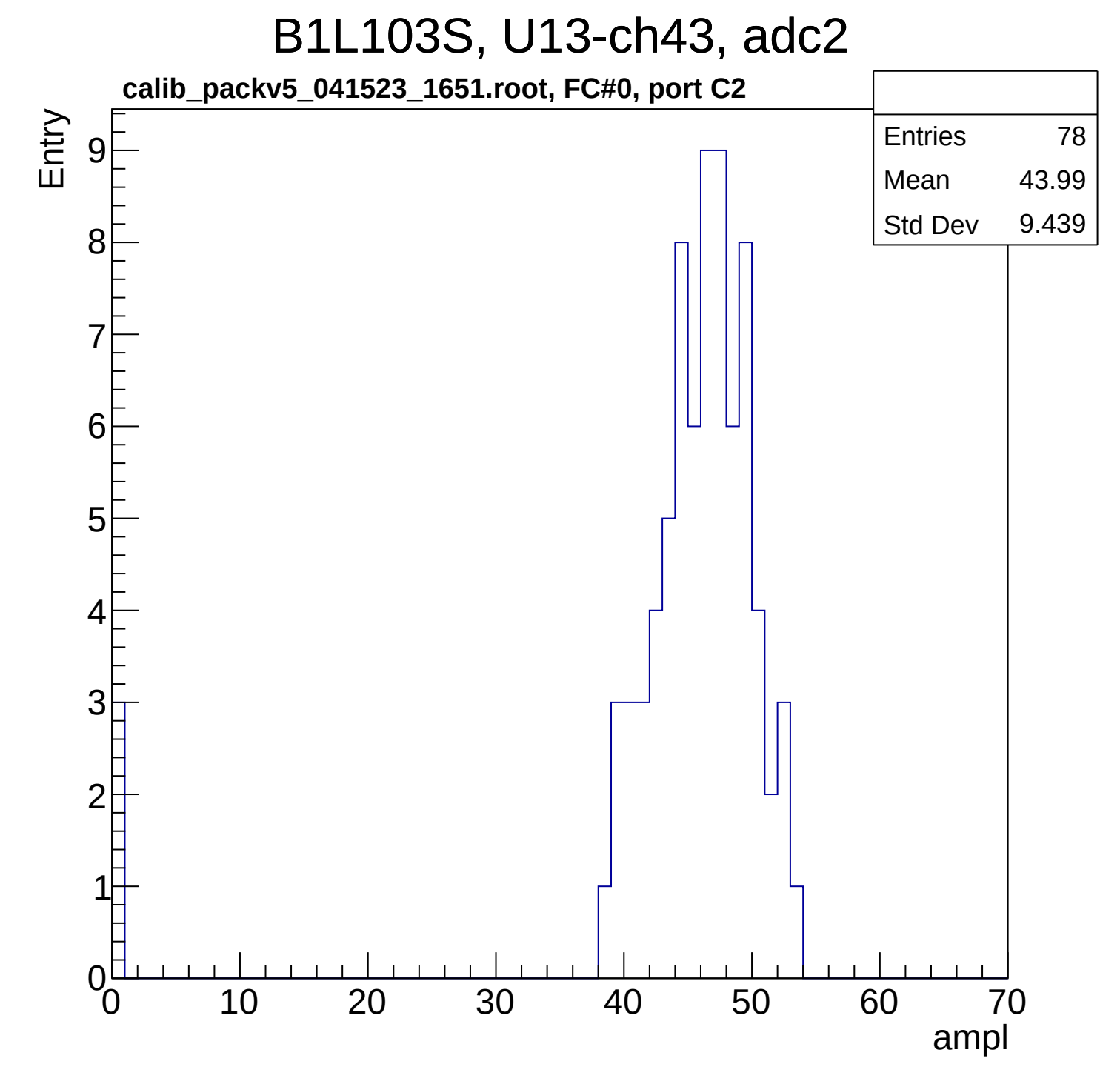
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch43, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 43.99
Std Dev 9.439
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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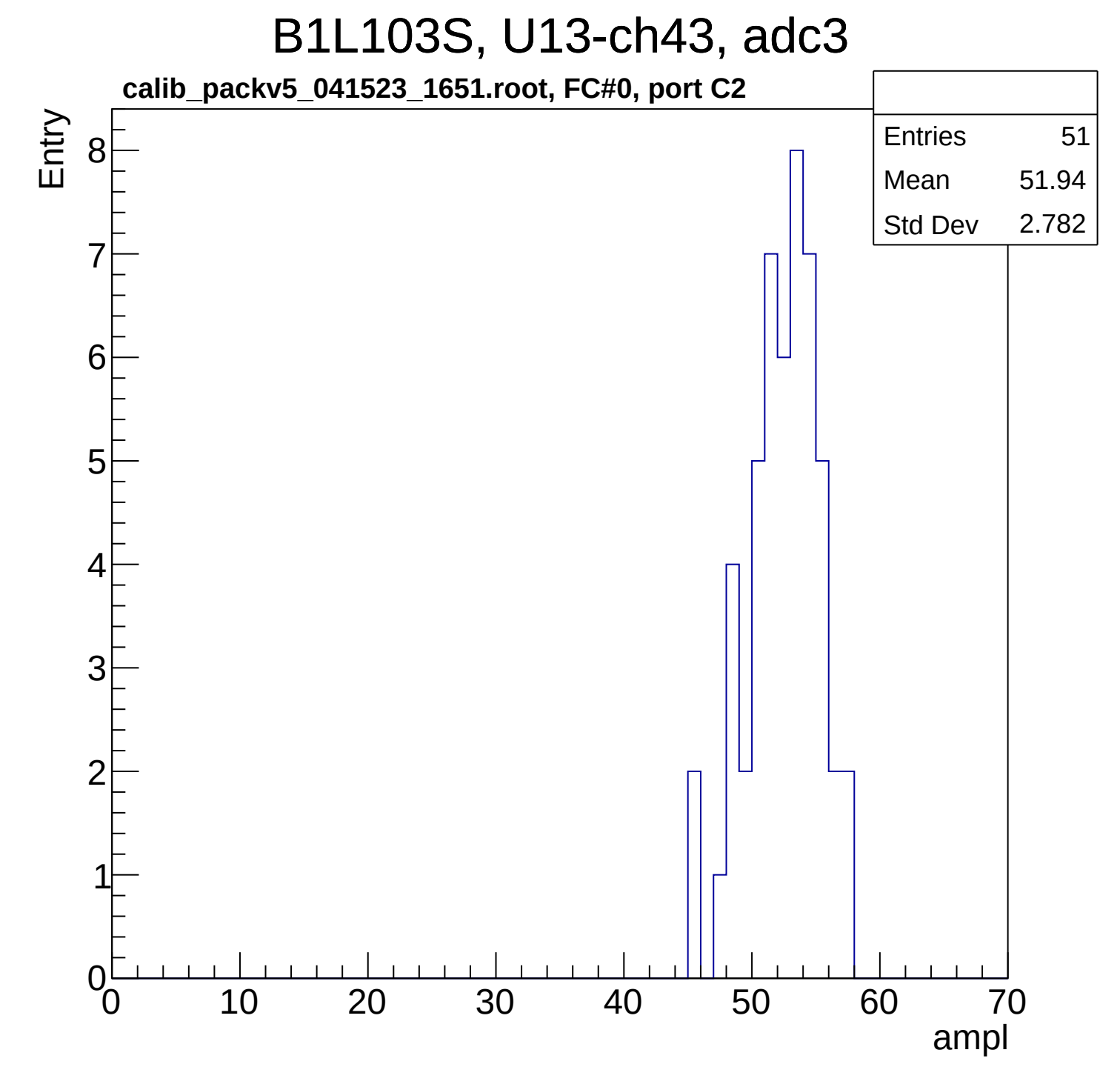
B1L103S, U13-ch43, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 51.94
Std Dev 2.782
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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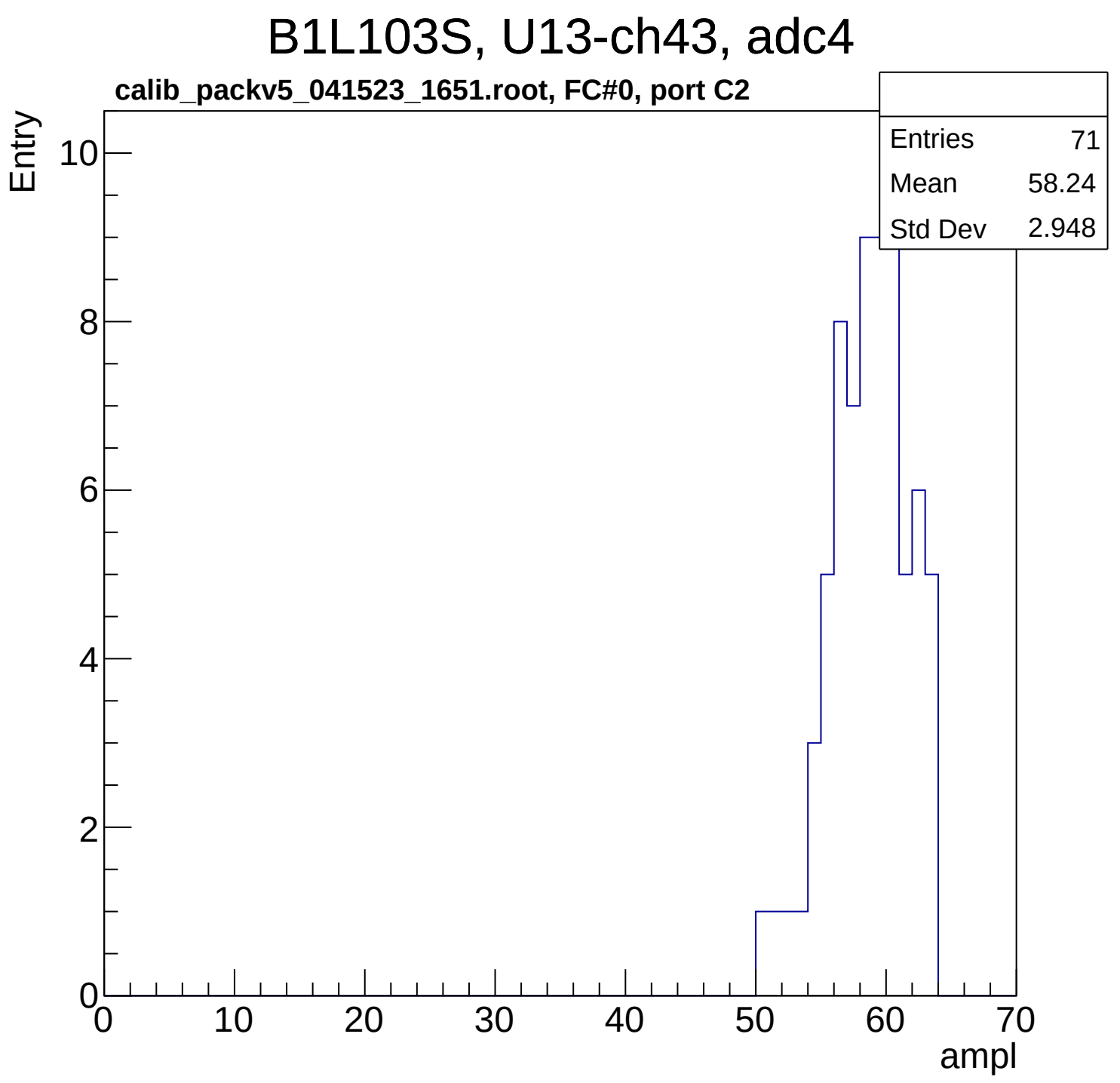
B1L103S, U13-ch43, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 58.24
Std Dev 2.948
Entry
ampl
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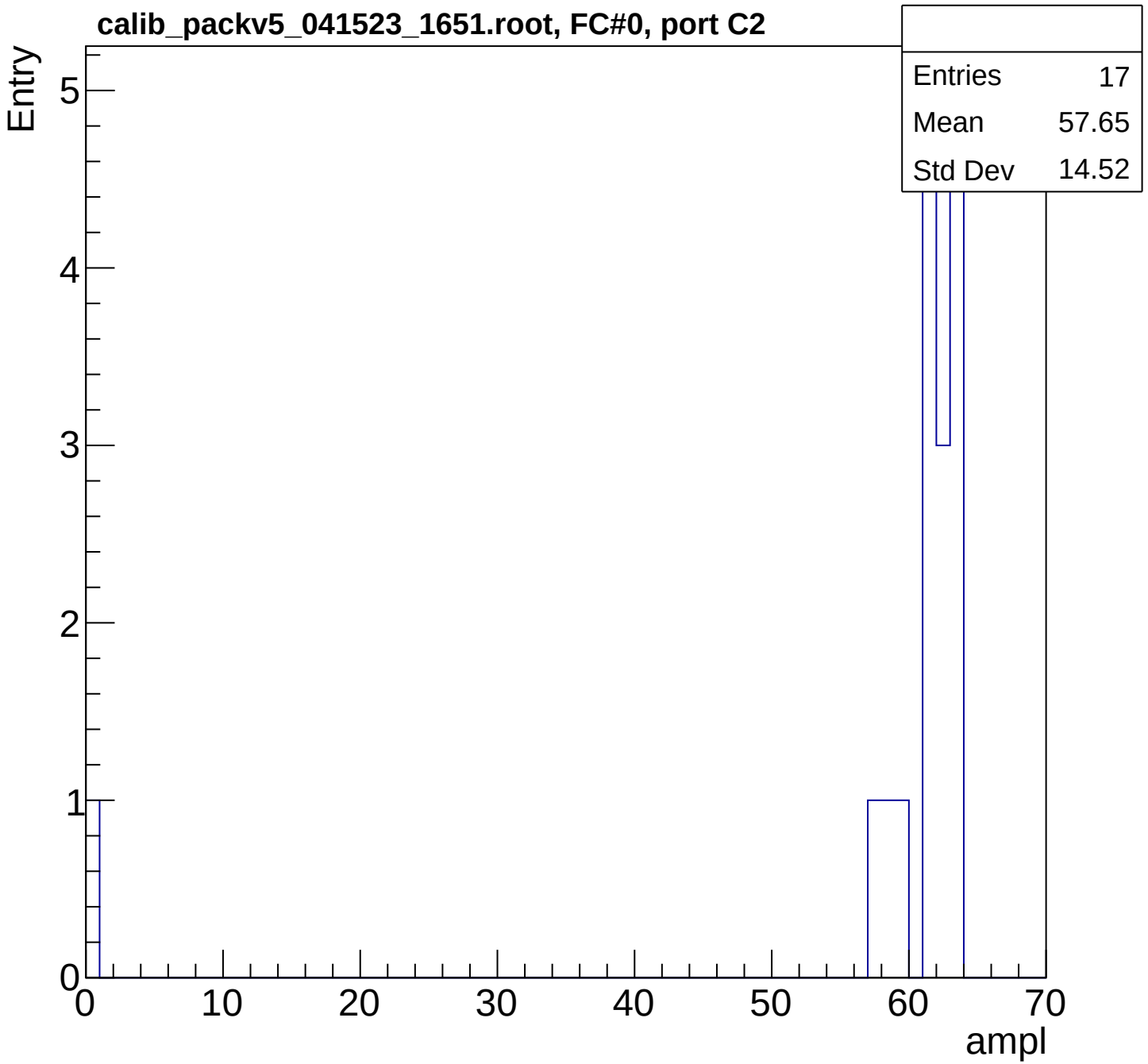
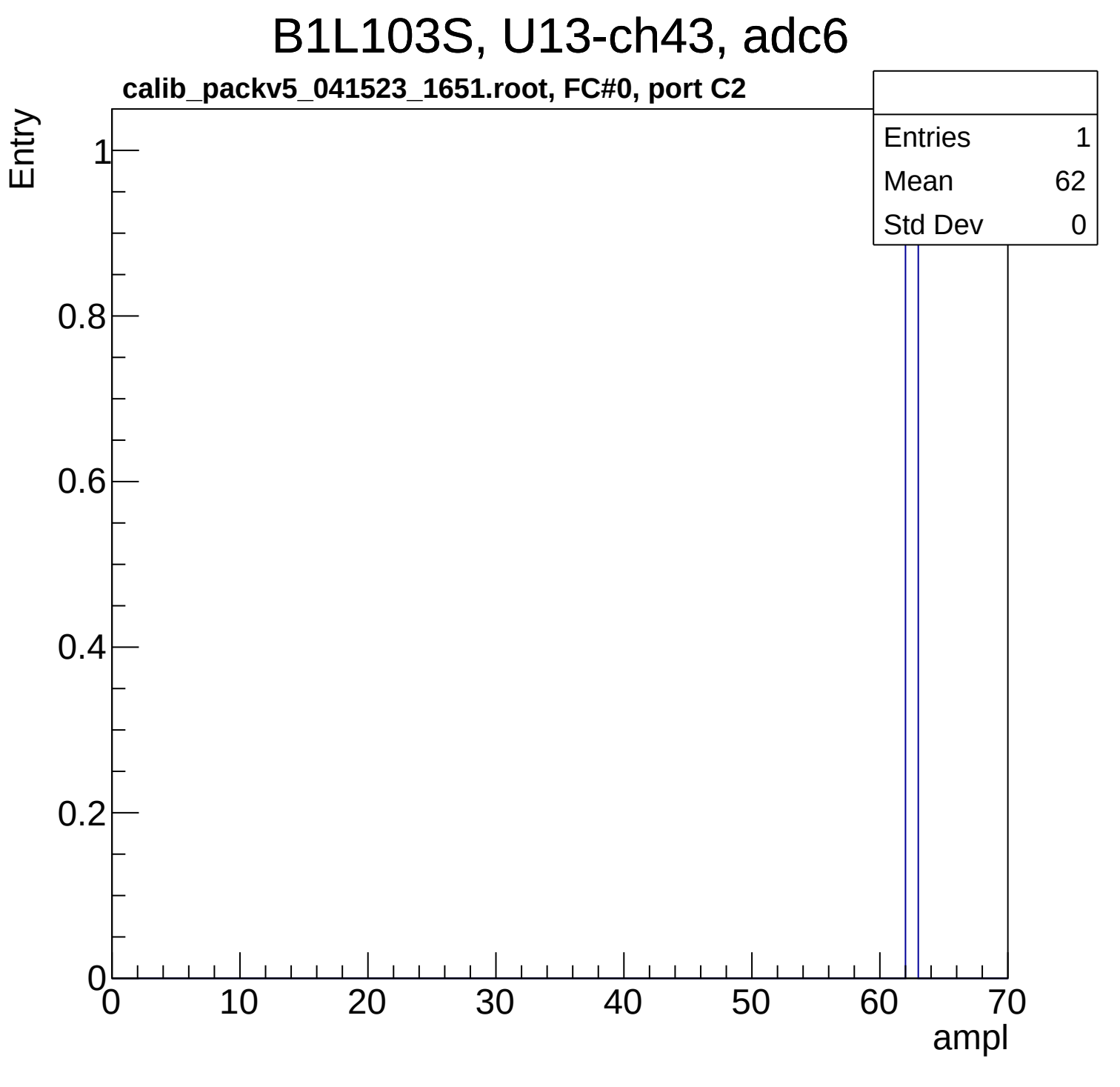
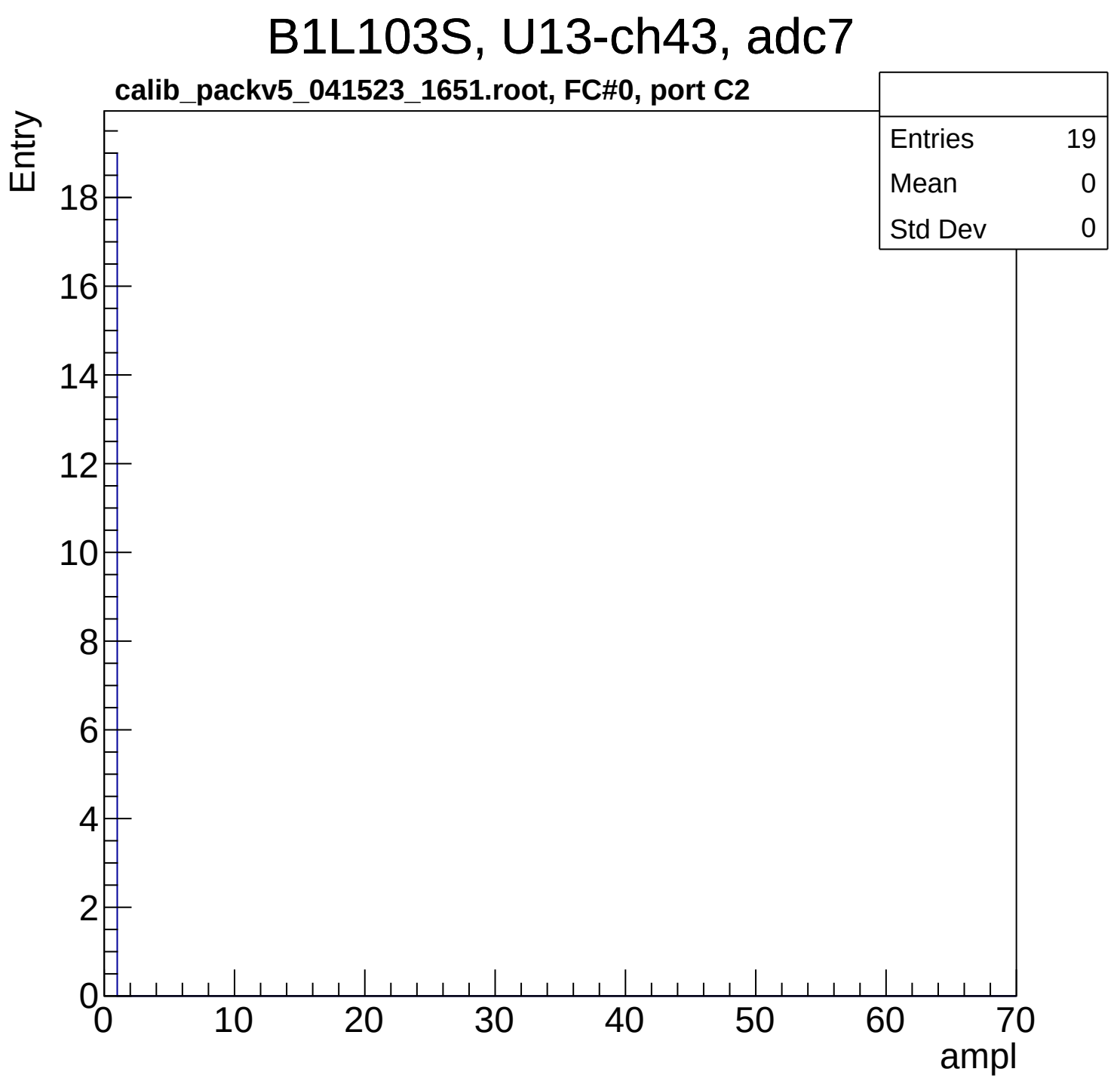
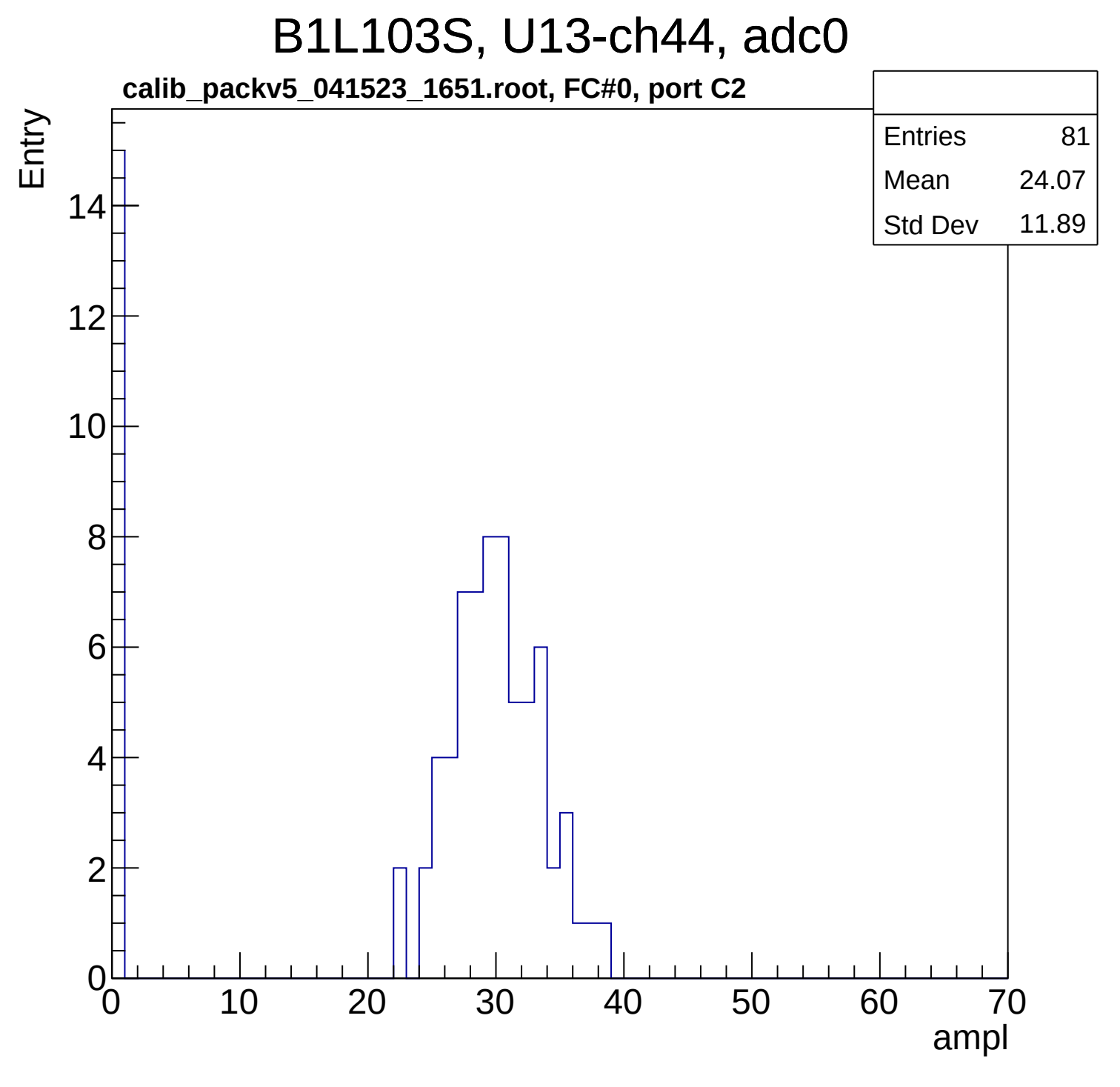
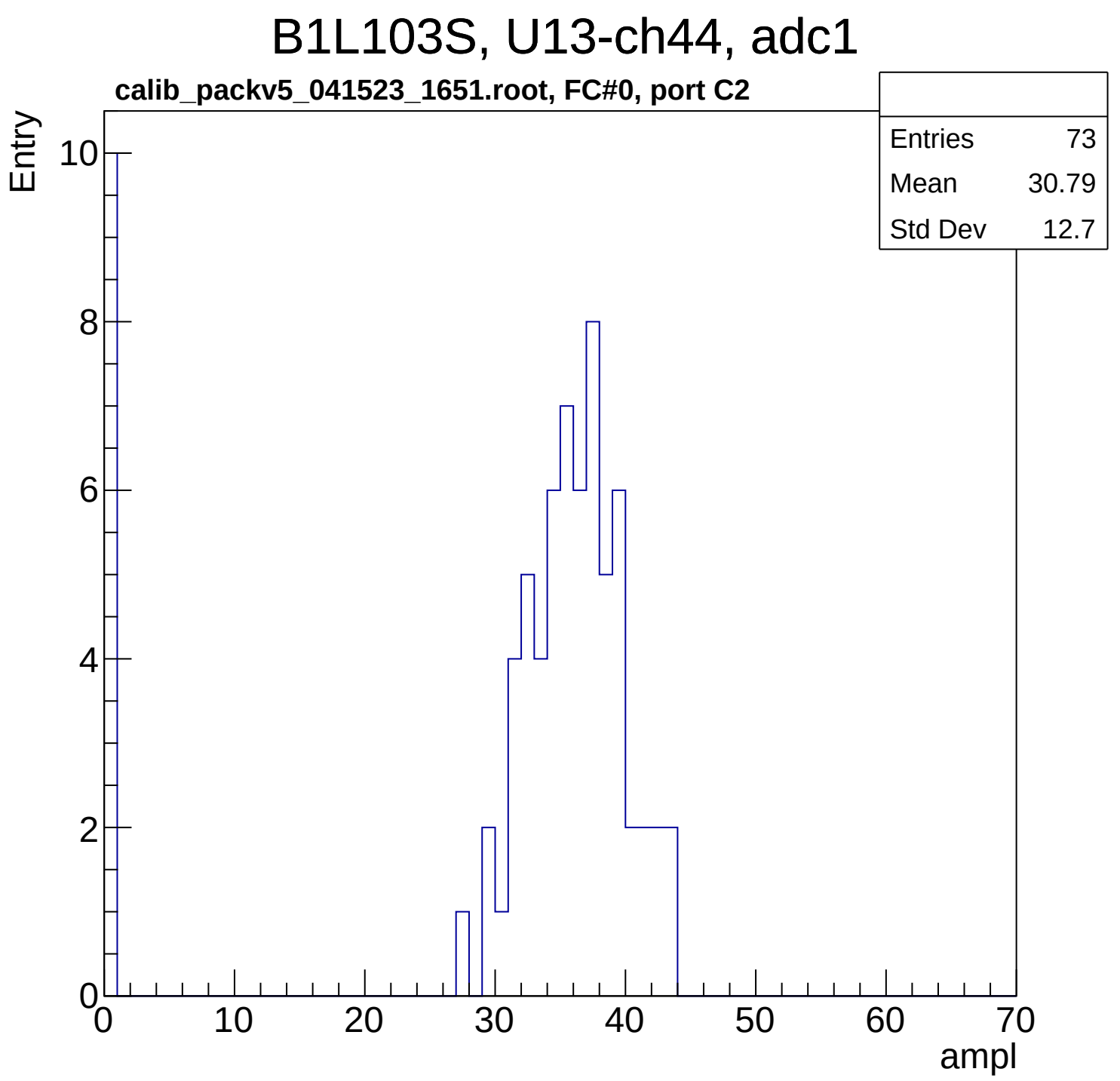
2
4
6
8
10
0
10
20
30
40
50
60
70

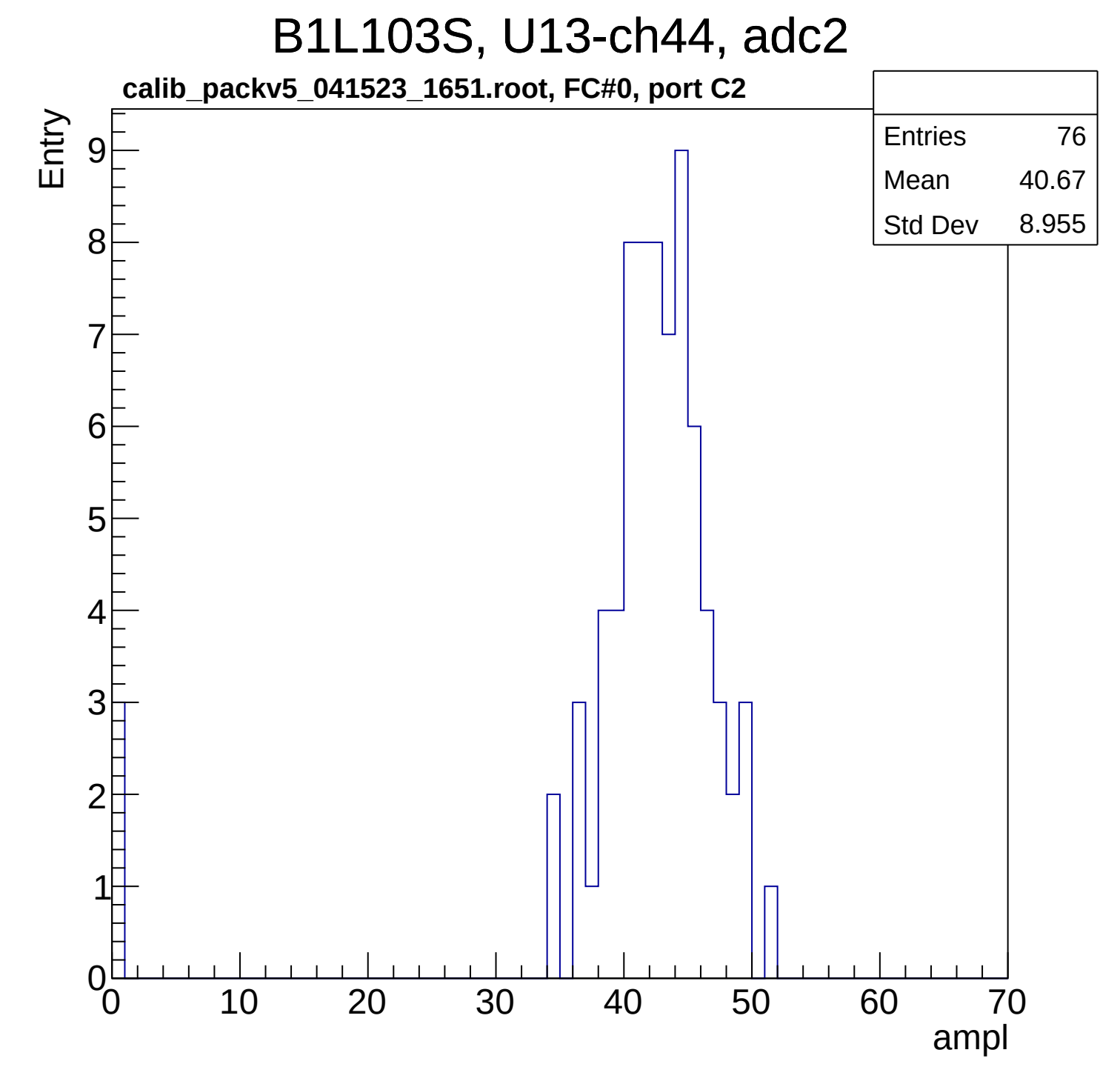

B1L103S, U13-ch43, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 57.65
Std Dev 14.52
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch43, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch43, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch44, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 24.07
Std Dev 11.89
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch44, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 30.79
Std Dev 12.7
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch44, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 40.67
Std Dev 8.955
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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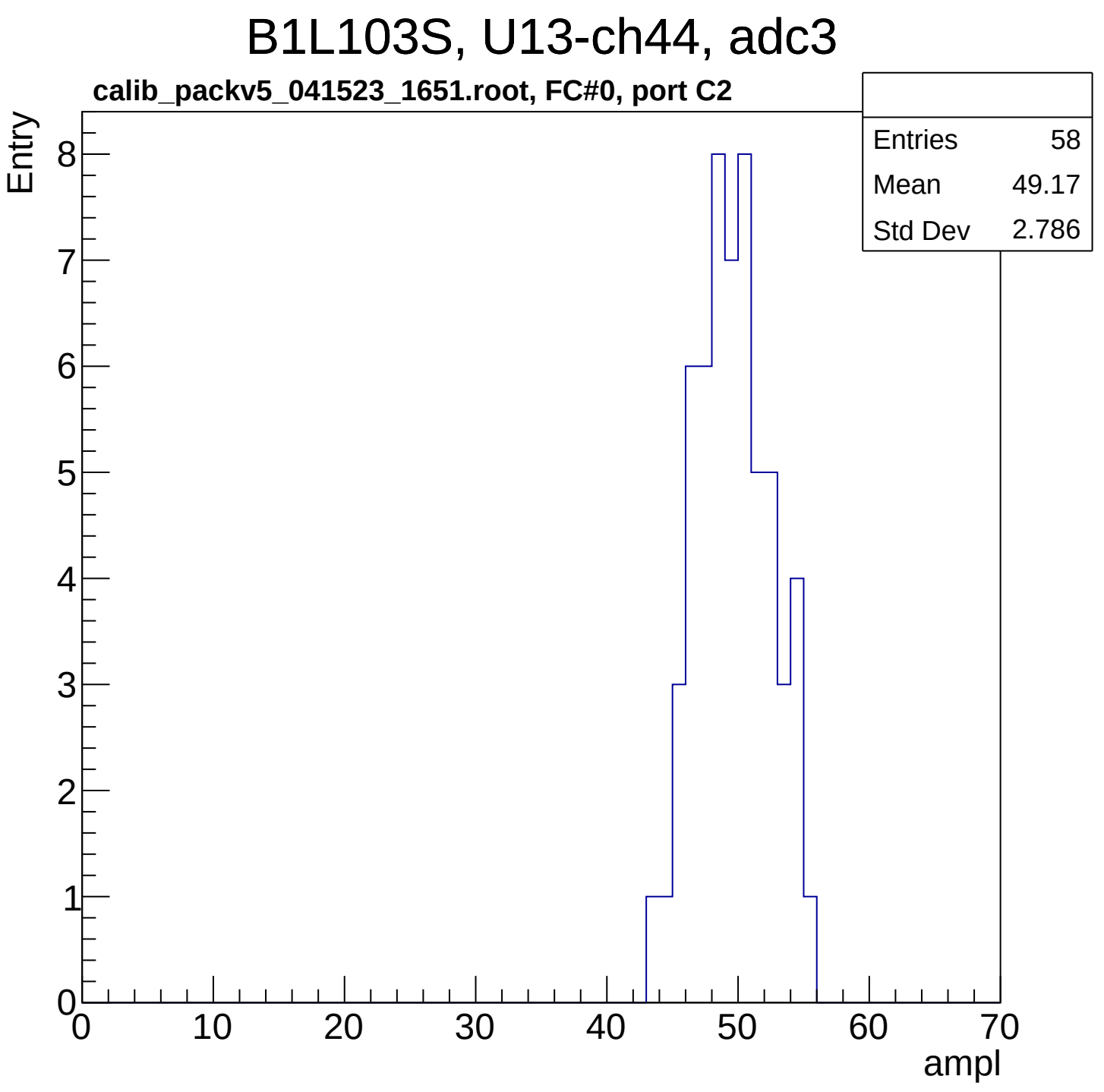
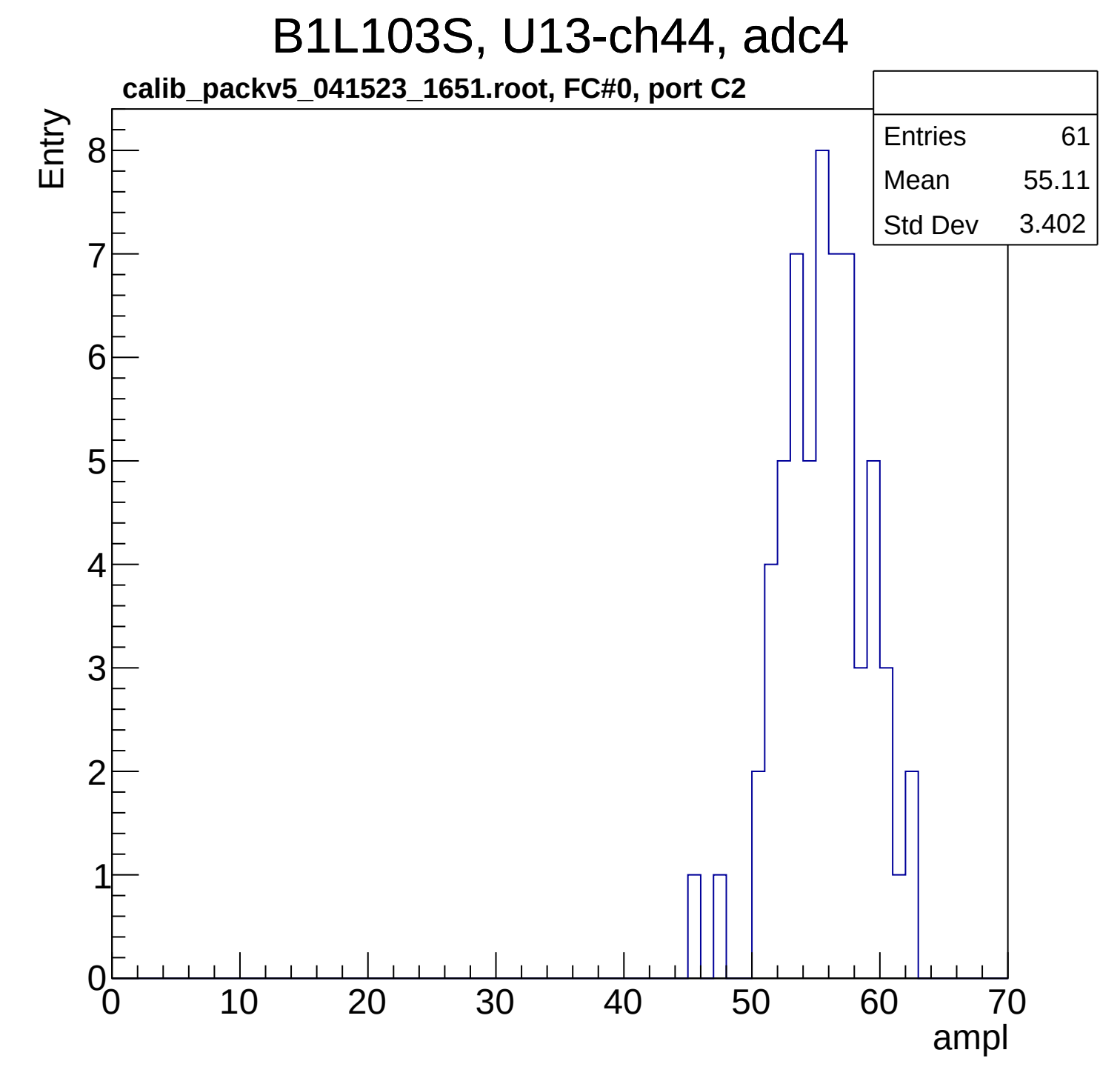

B1L103S, U13-ch44, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 49.17
Std Dev 2.786
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch44, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 55.11
Std Dev 3.402
Entry
ampl
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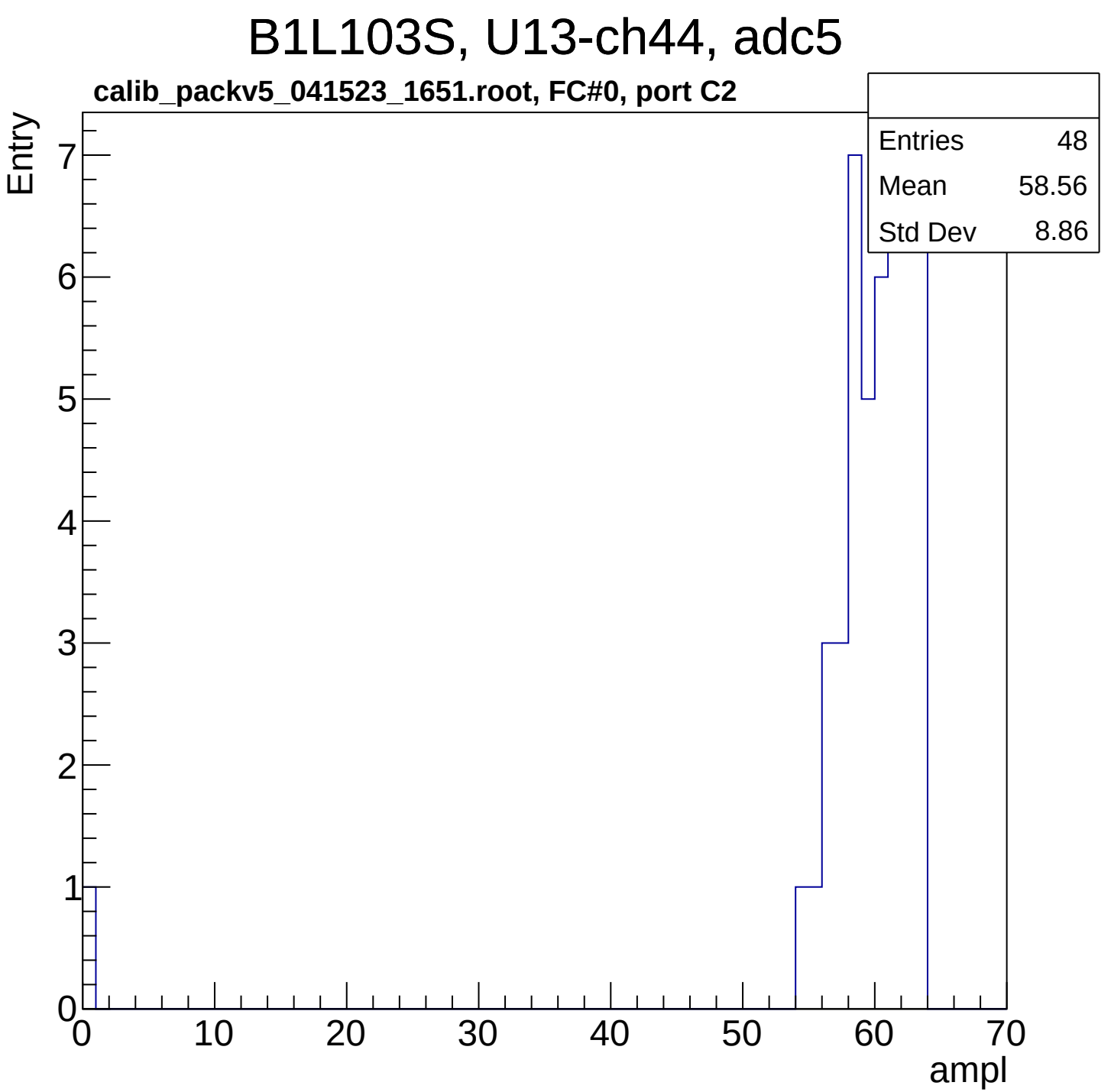
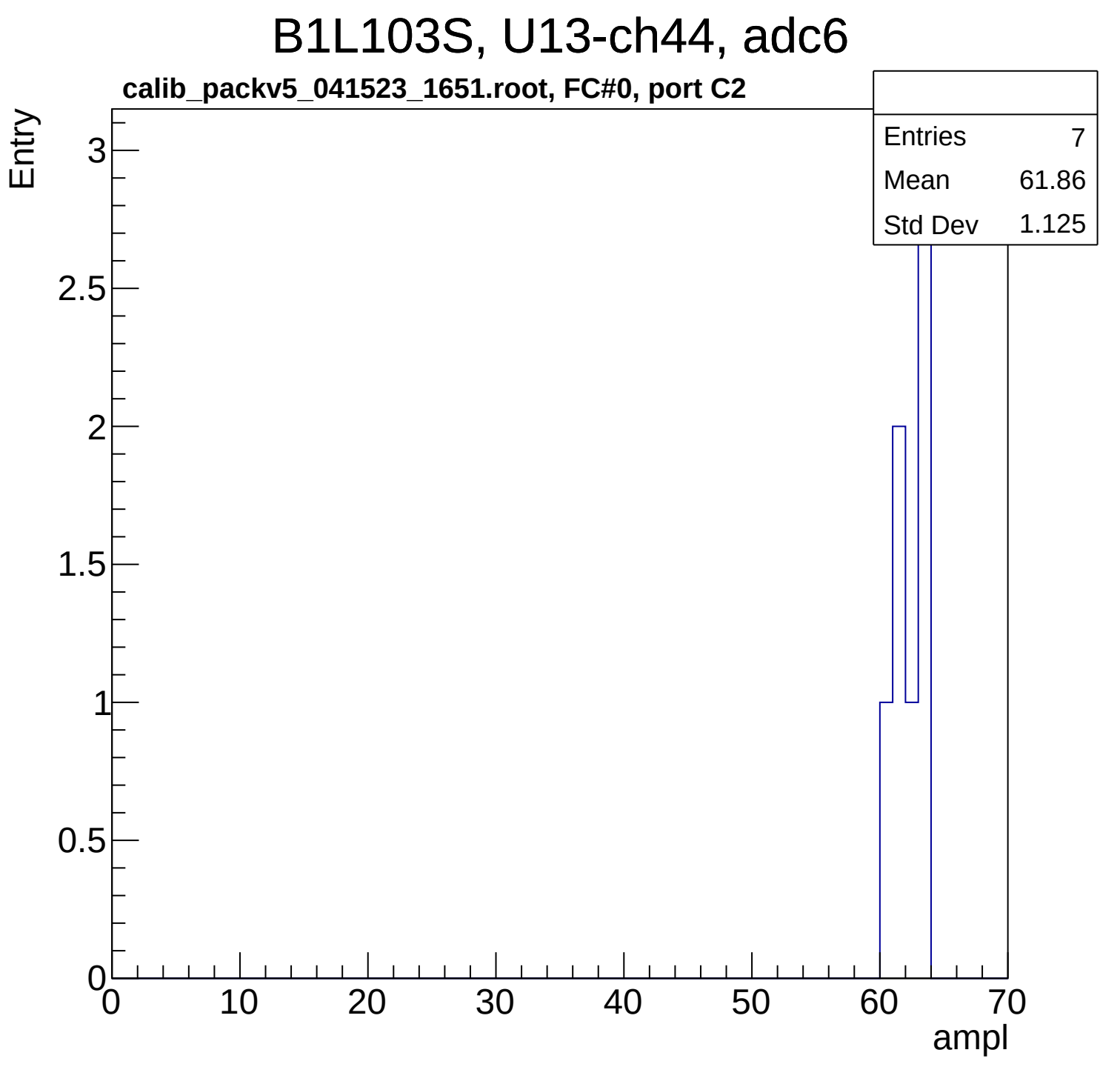
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch44, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.56
Std Dev 8.86
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch44, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.86
Std Dev 1.125
Entry
ampl
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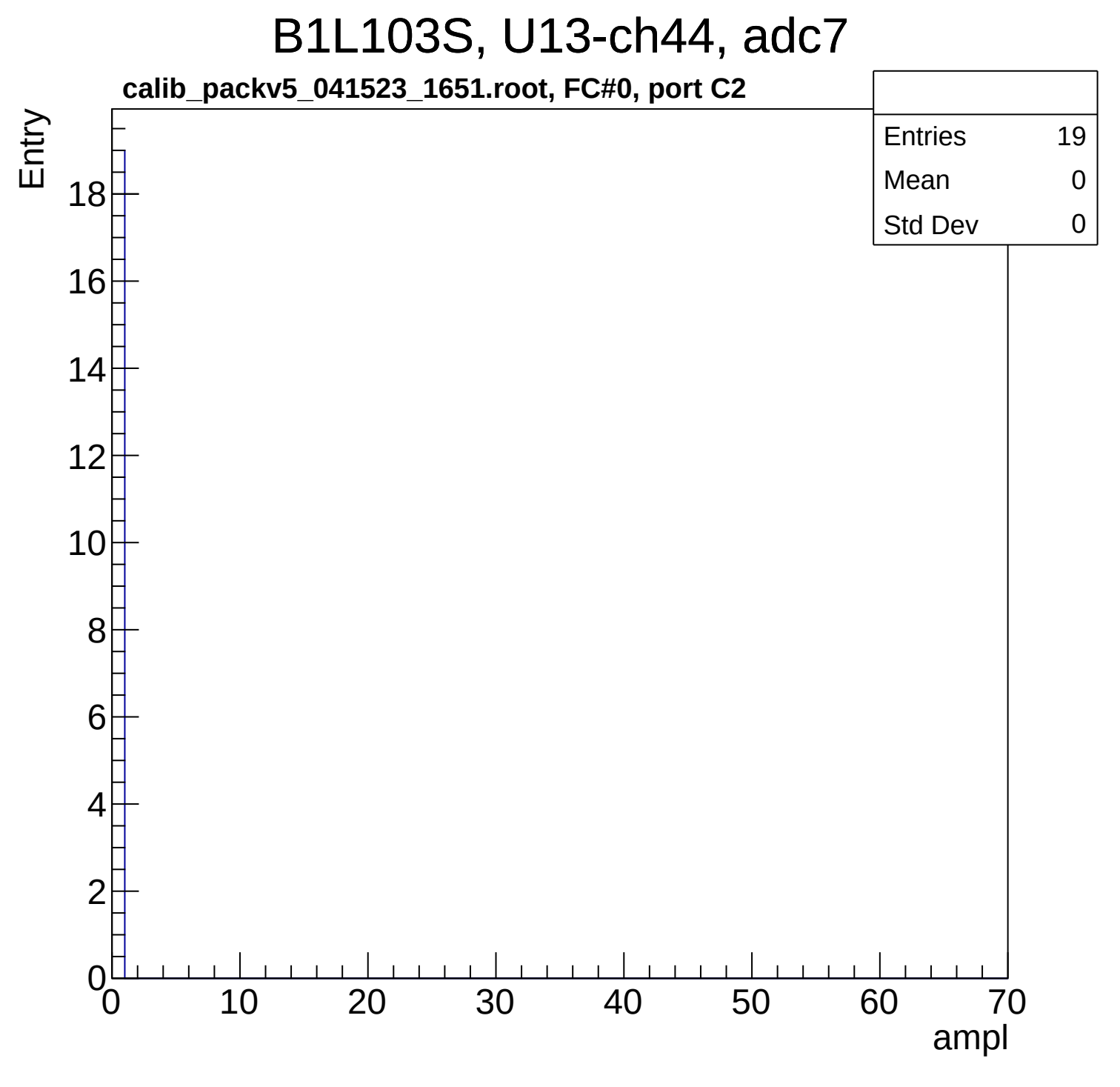
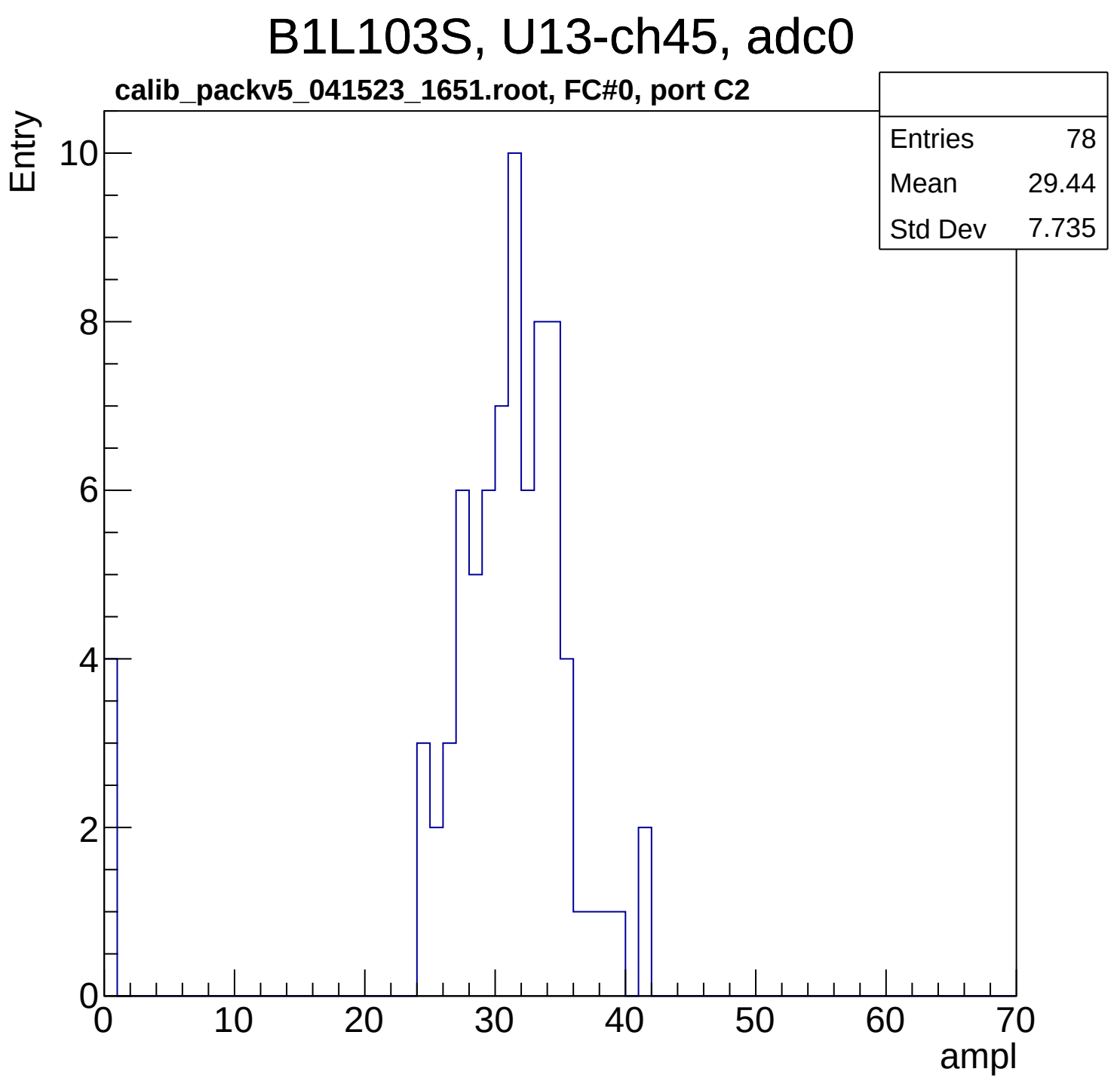
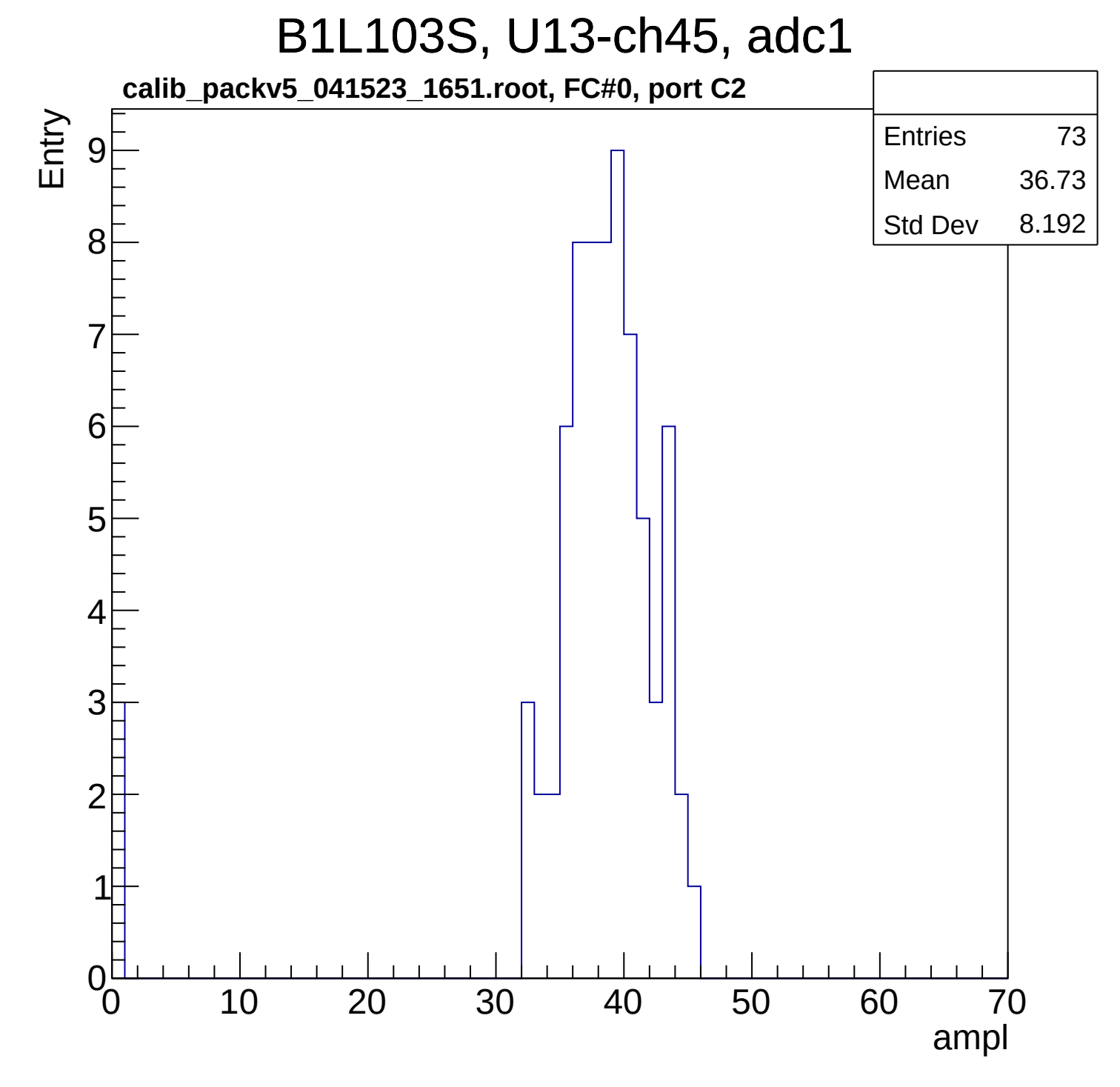
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U13-ch44, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch45, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 29.44
Std Dev 7.735
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch45, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 36.73
Std Dev 8.192
Entry
ampl
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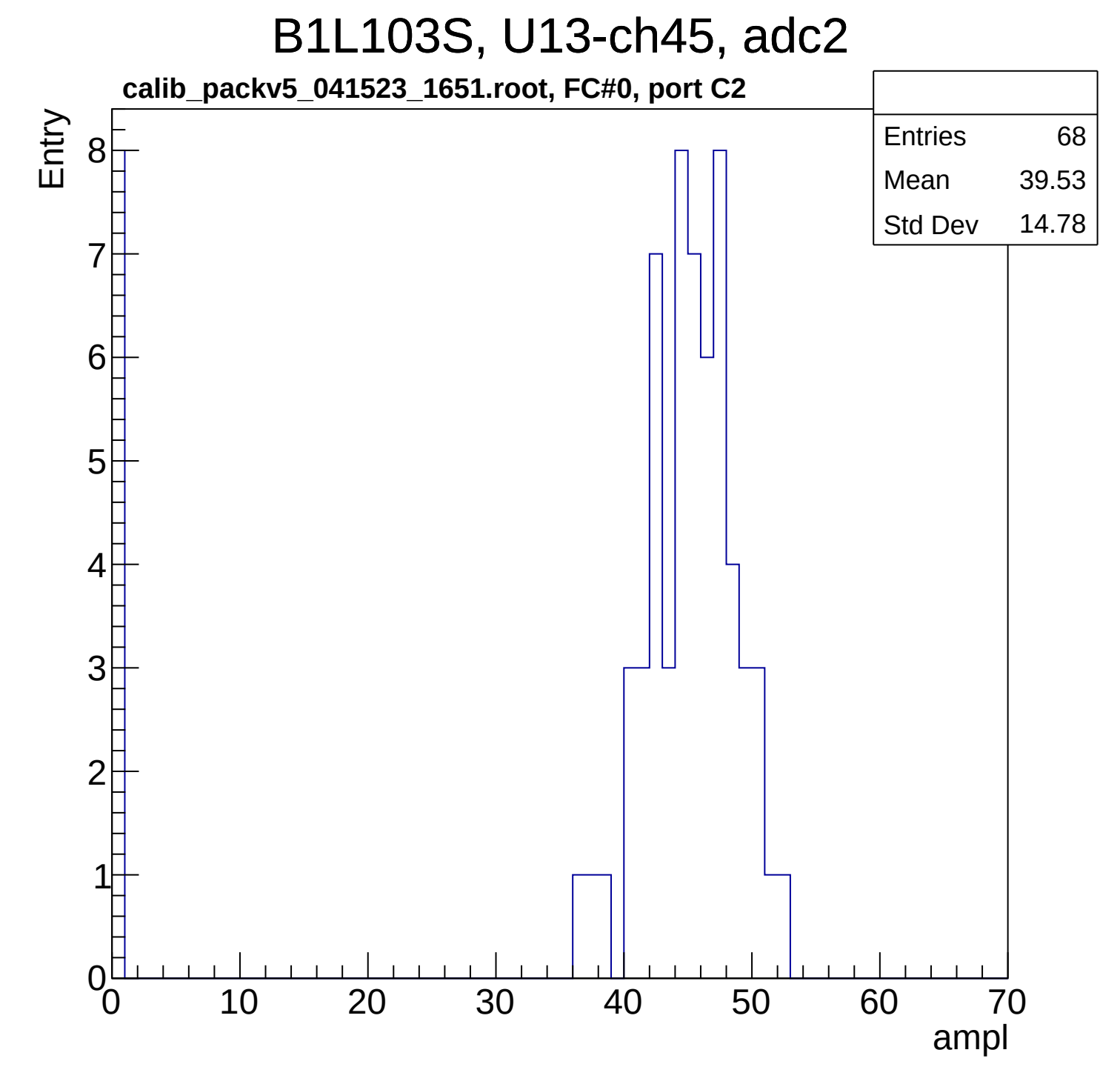
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch45, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 39.53
Std Dev 14.78
Entry
ampl
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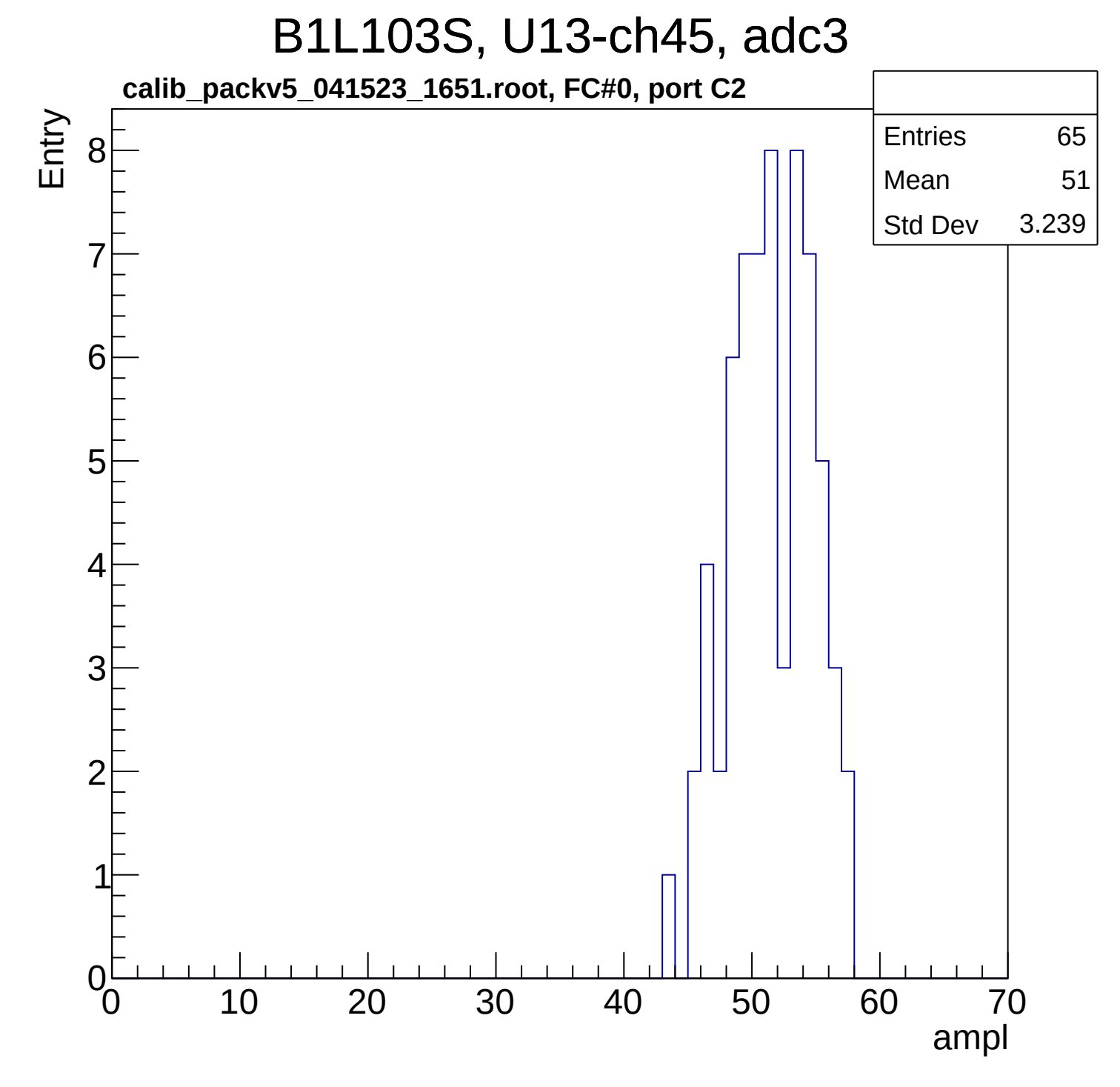
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch45, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 51
Std Dev 3.239
Entry
ampl
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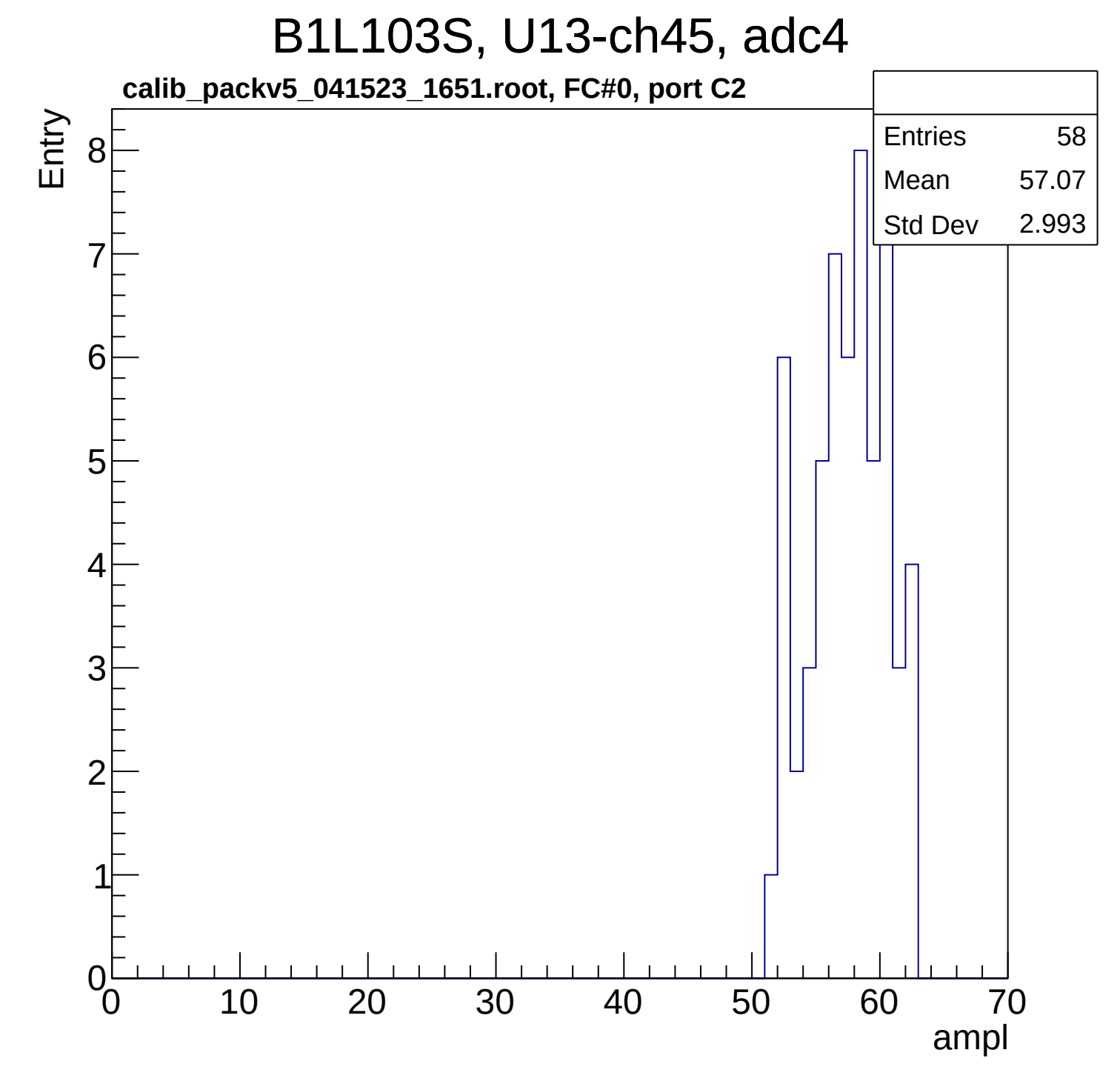
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch45, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 57.07
Std Dev 2.993
Entry
ampl
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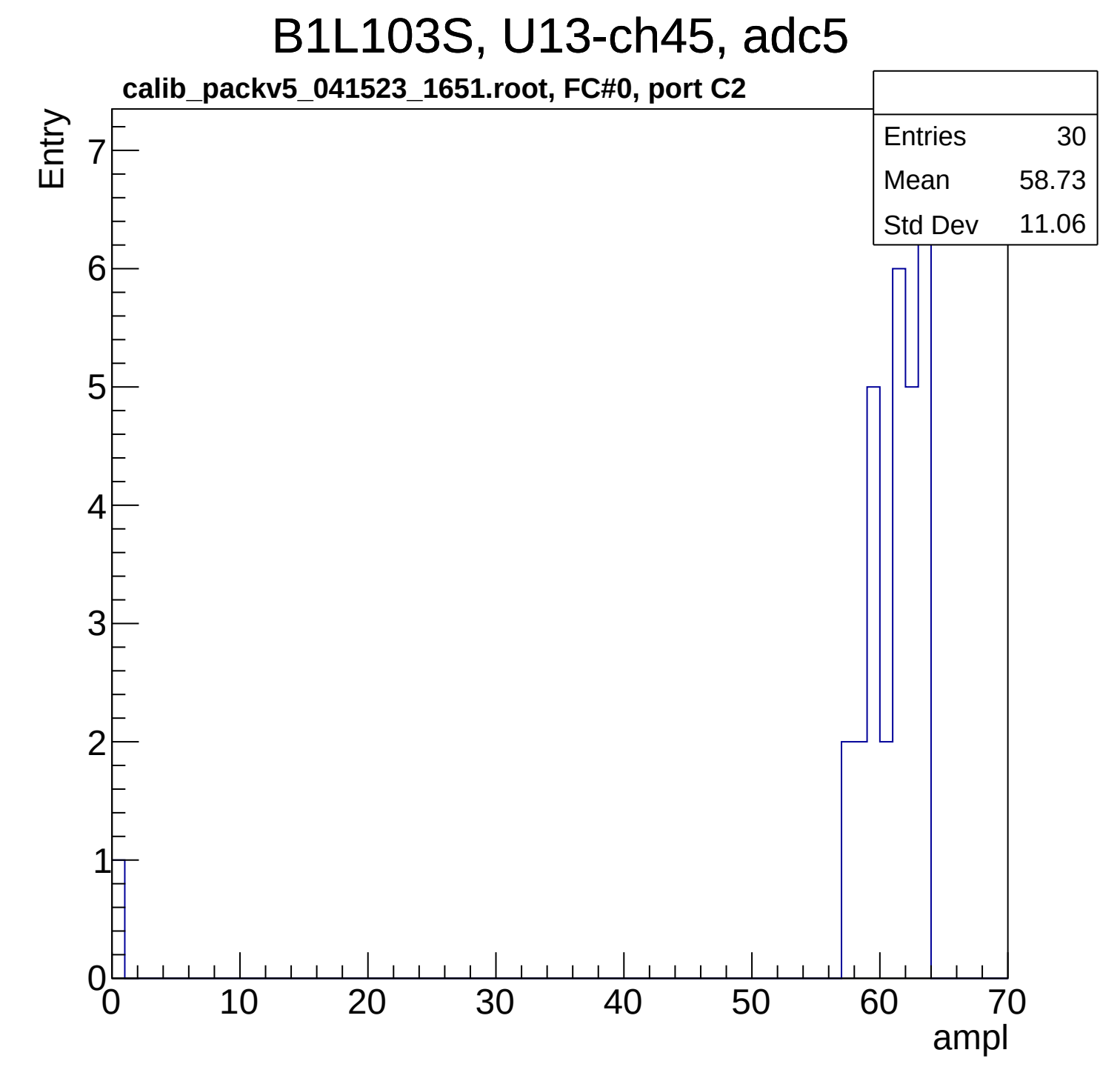
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch45, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 58.73
Std Dev 11.06
Entry
ampl
0
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2
3
4
5
6
7
0
10
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30
40
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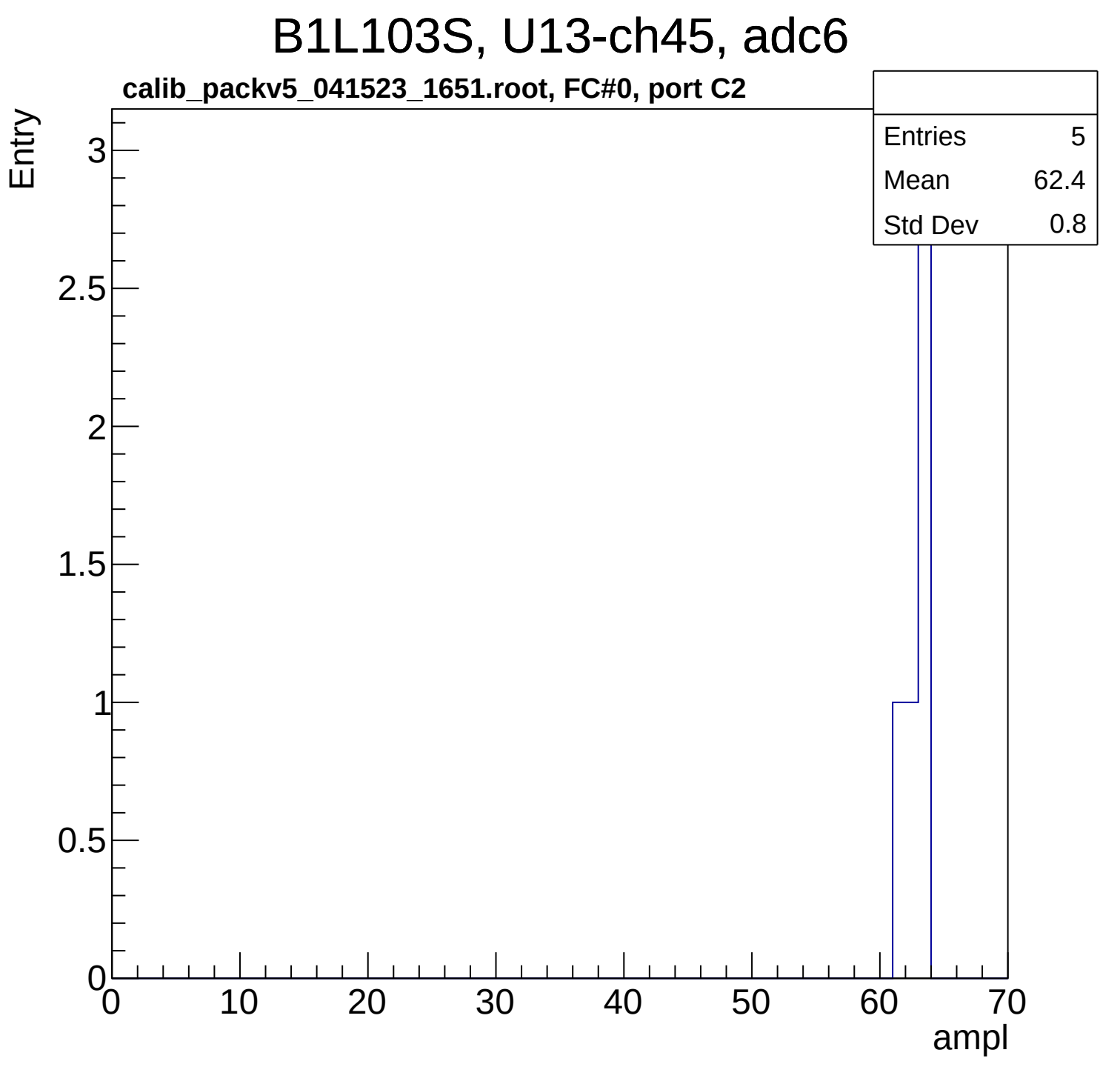
60
70


B1L103S, U13-ch45, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.4
Std Dev 0.8
Entry
ampl
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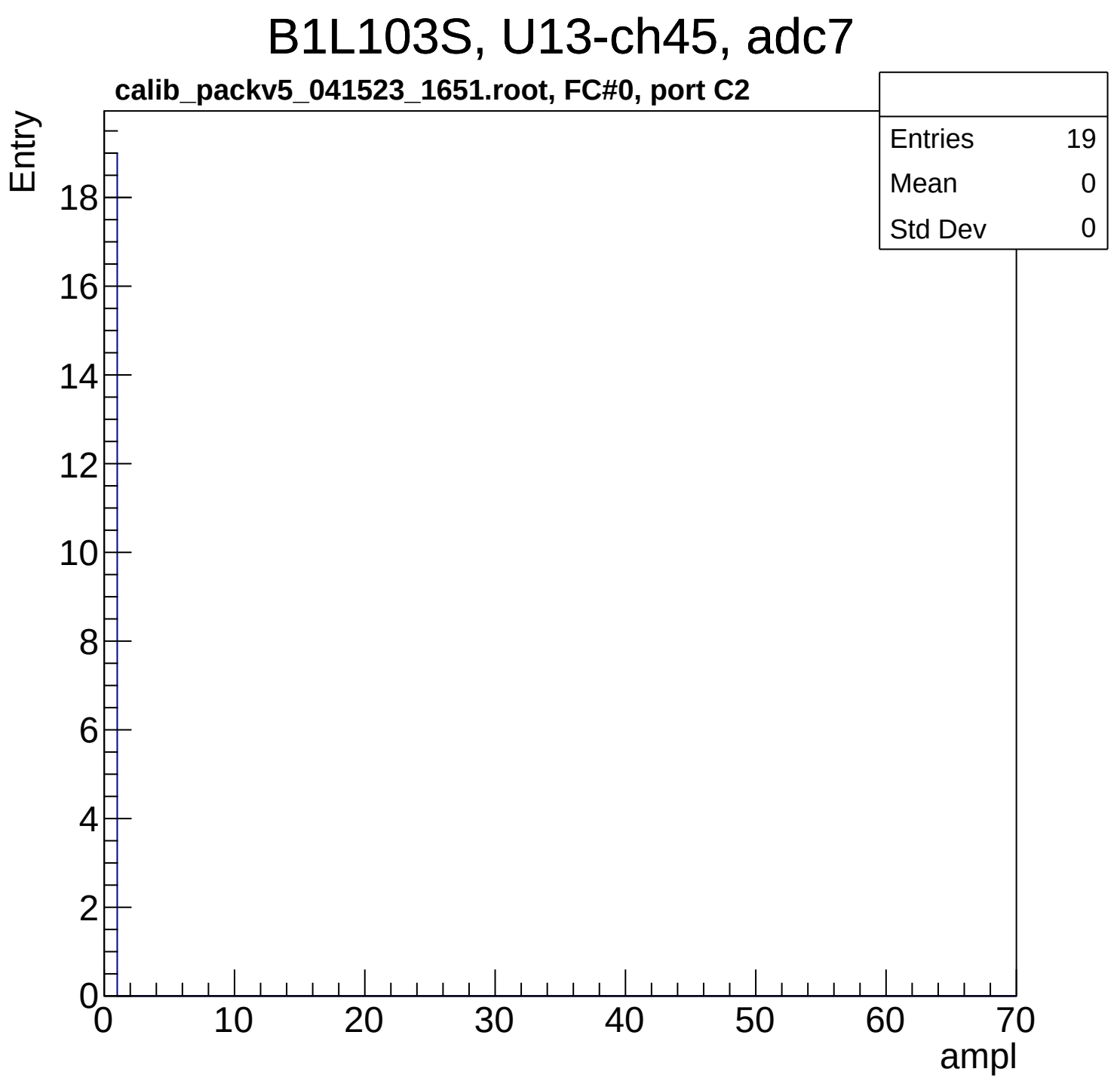
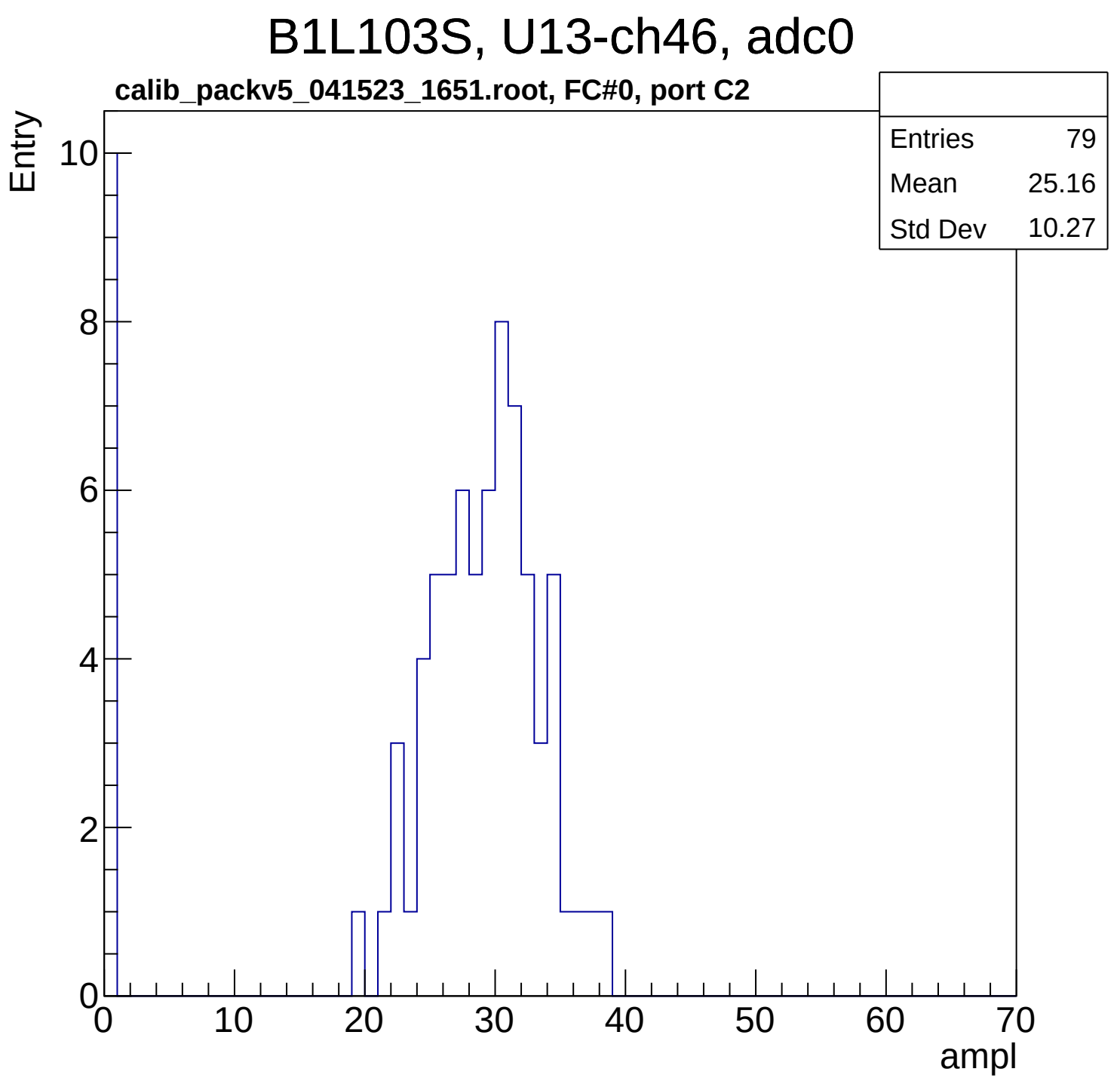
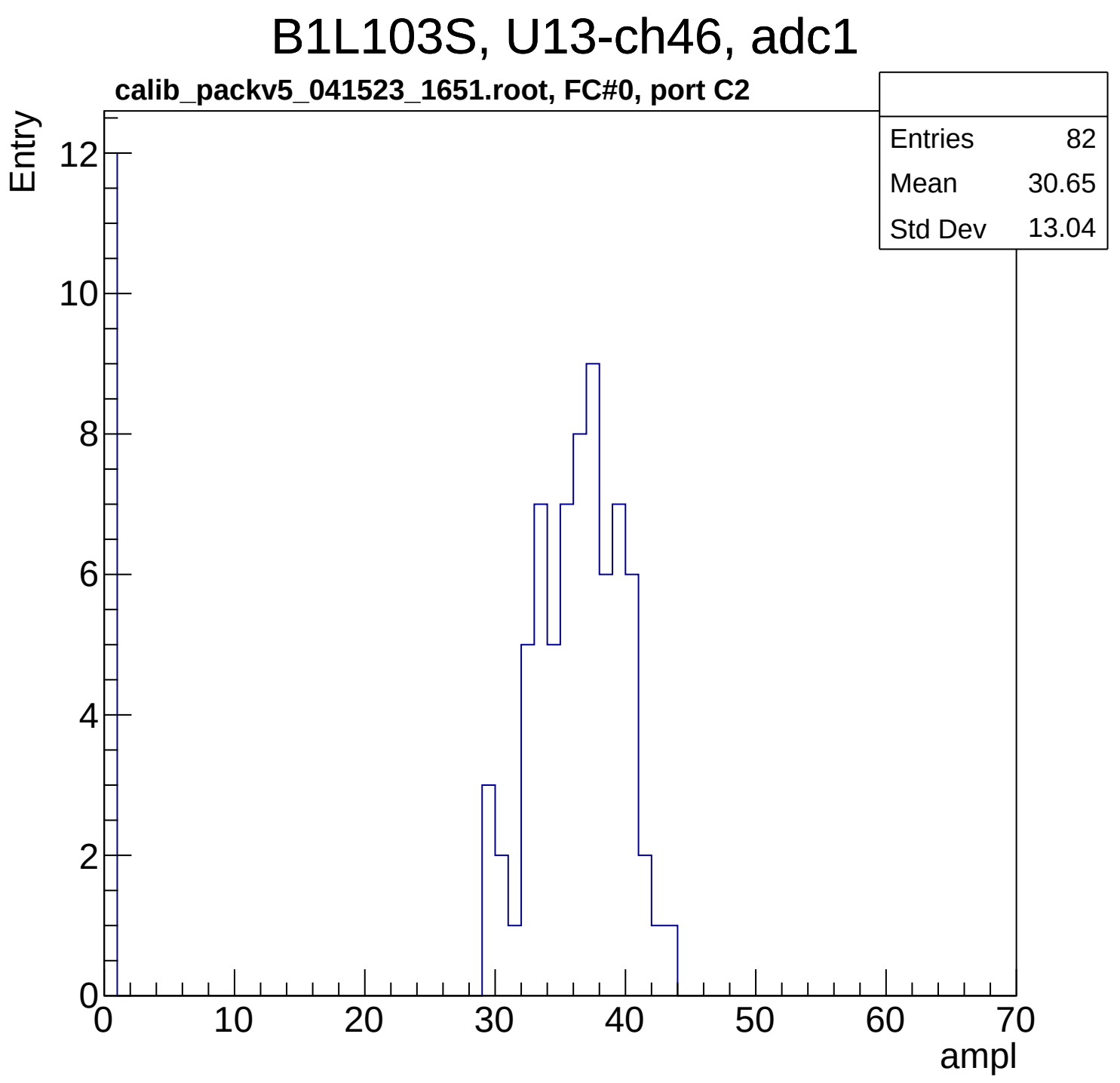
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U13-ch45, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch46, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 25.16
Std Dev 10.27
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch46, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 30.65
Std Dev 13.04
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
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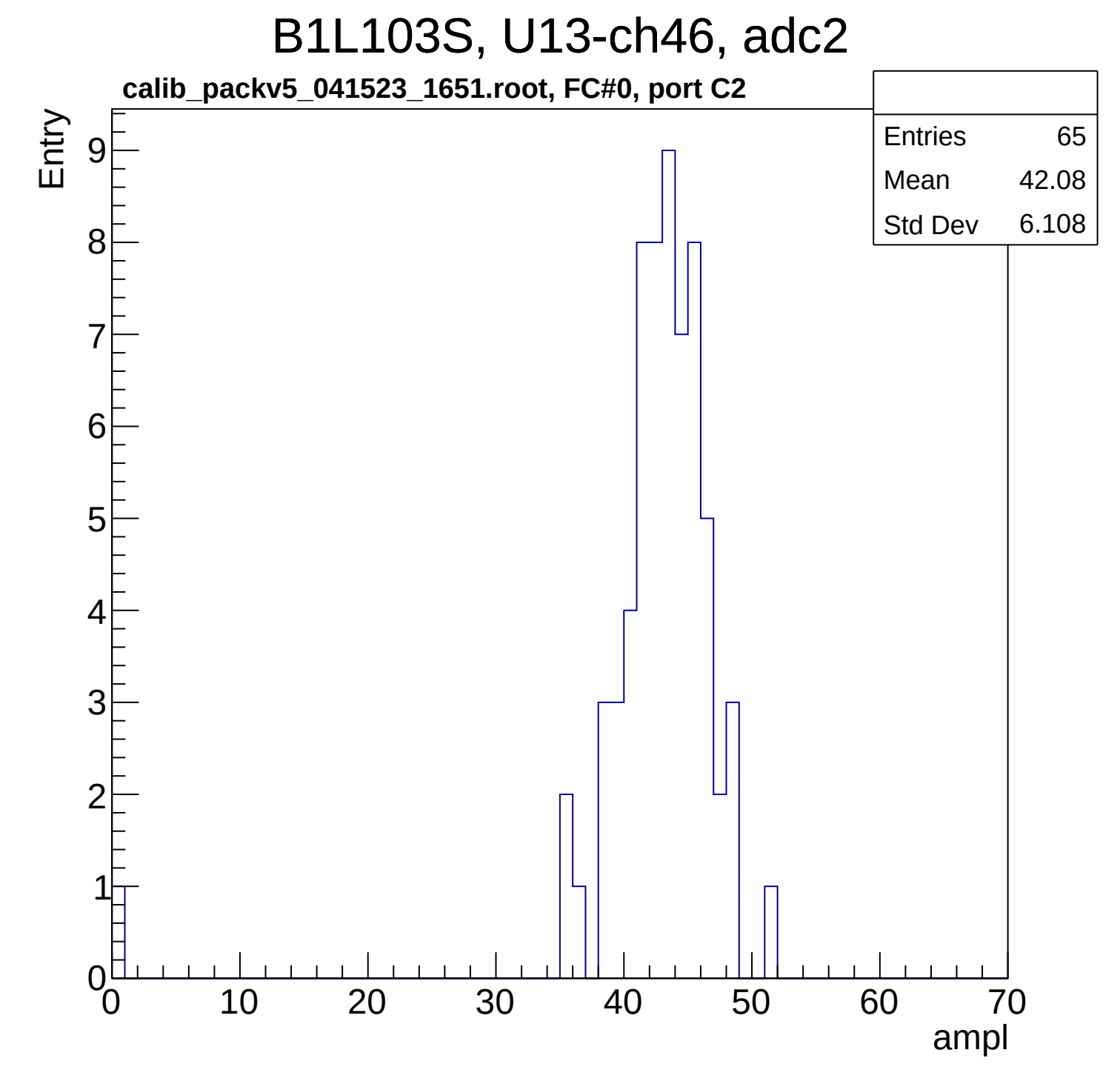
70
ampl


B1L103S, U13-ch46, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 42.08
Std Dev 6.108
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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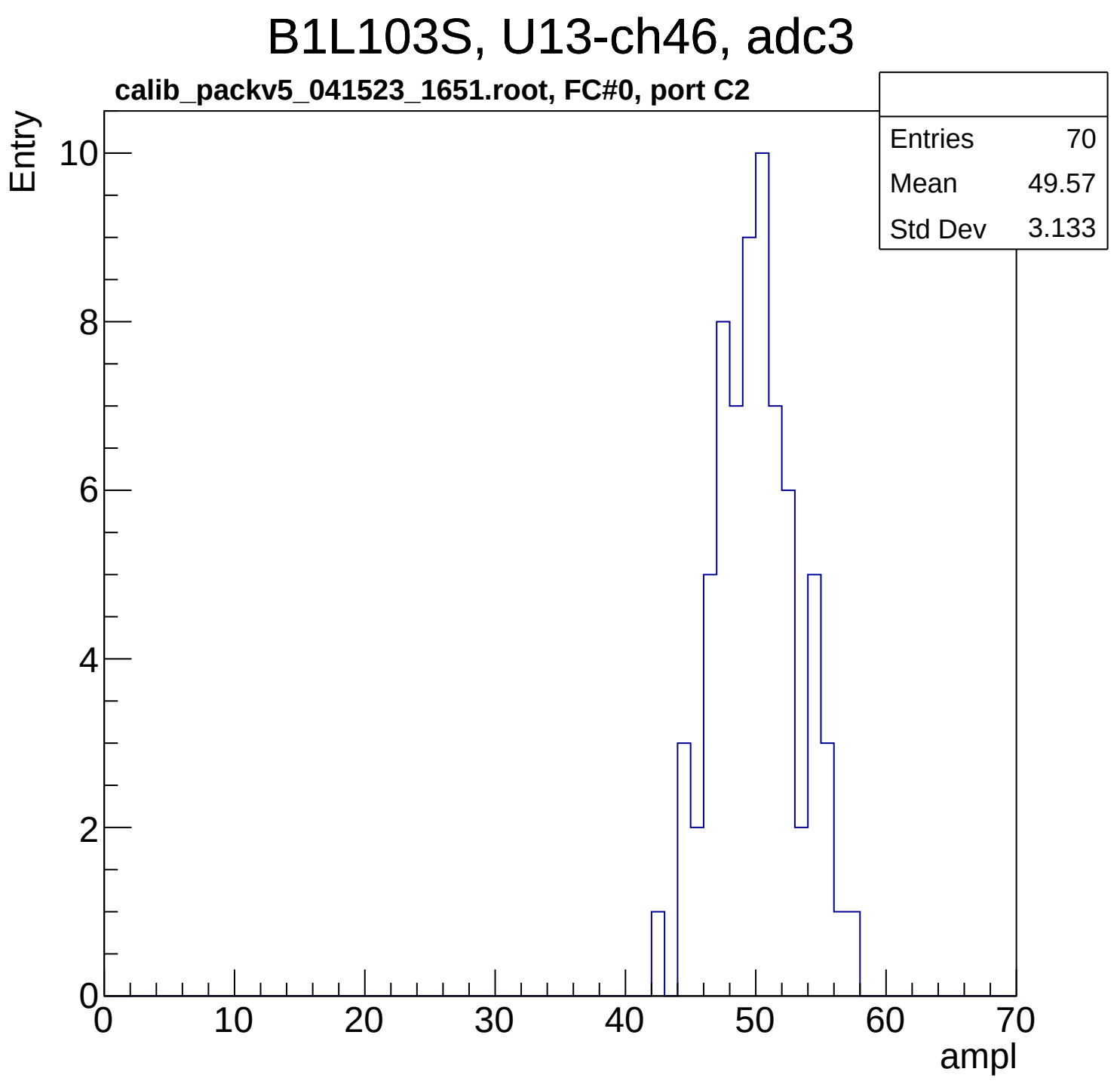
60
70


B1L103S, U13-ch46, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 49.57
Std Dev 3.133
Entry
ampl
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2
4
6
8
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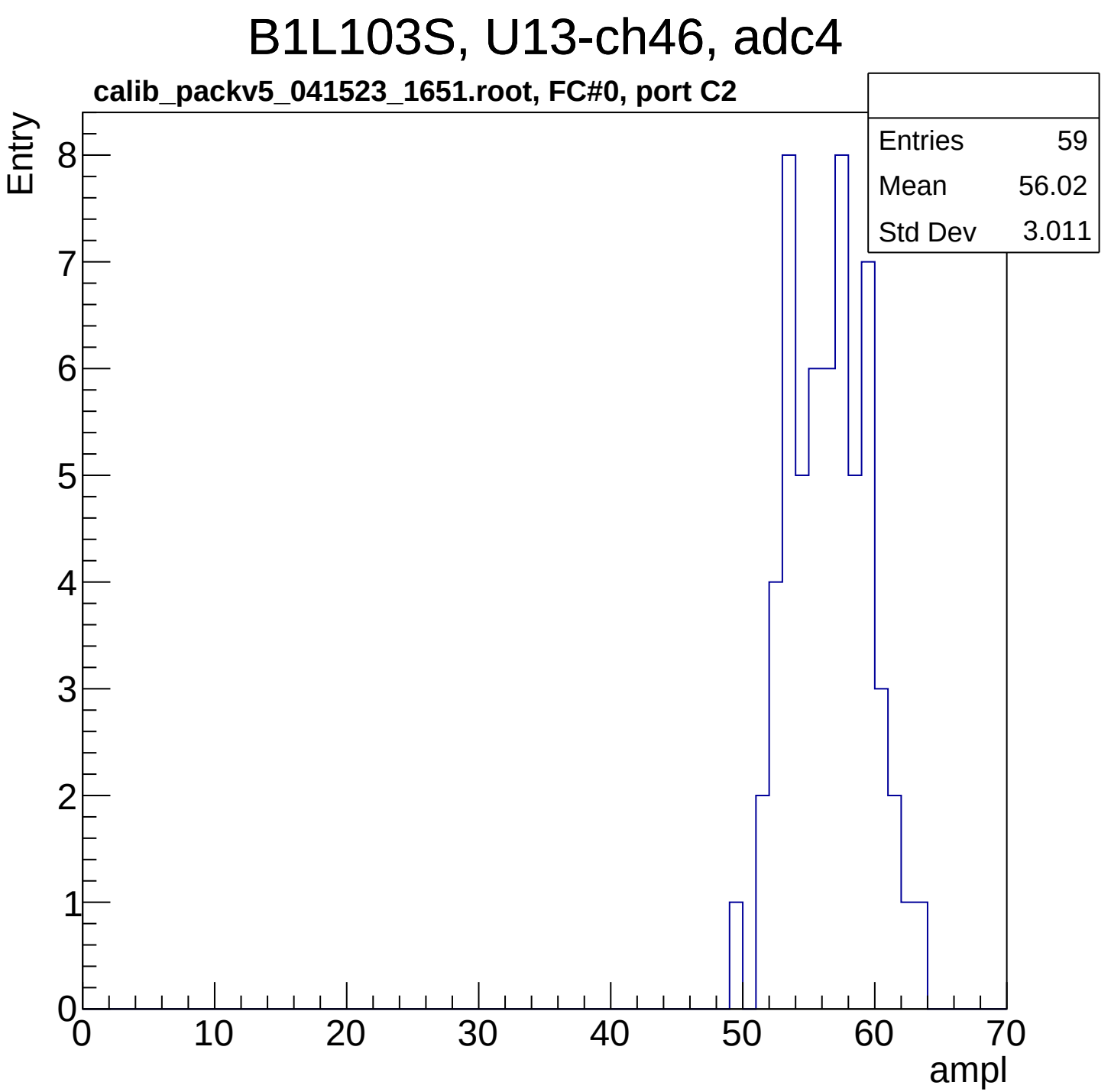
0
10
20
30
40
50
60
70


B1L103S, U13-ch46, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 56.02
Std Dev 3.011
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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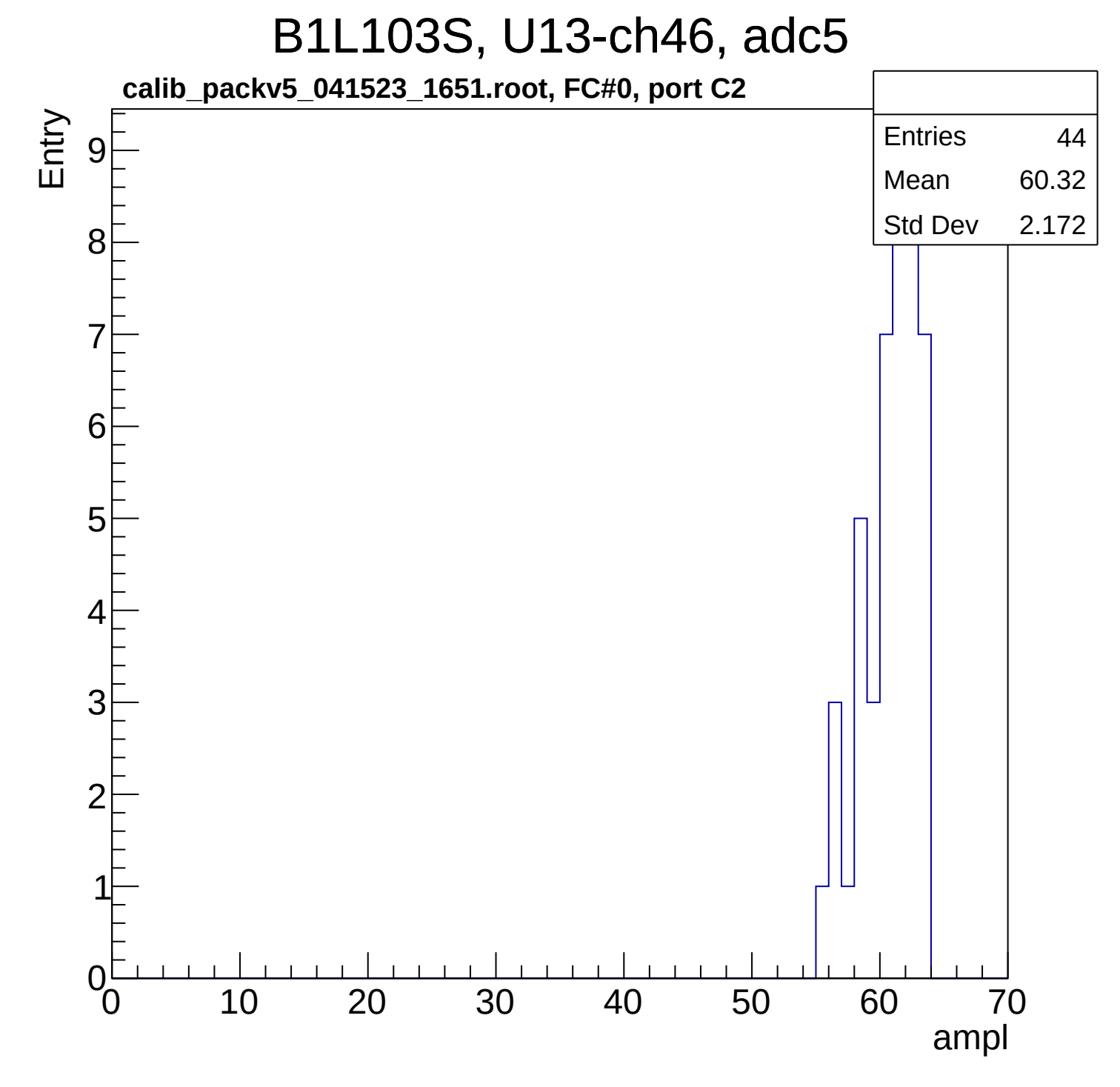
40
50
60
70


B1L103S, U13-ch46, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 60.32
Std Dev 2.172
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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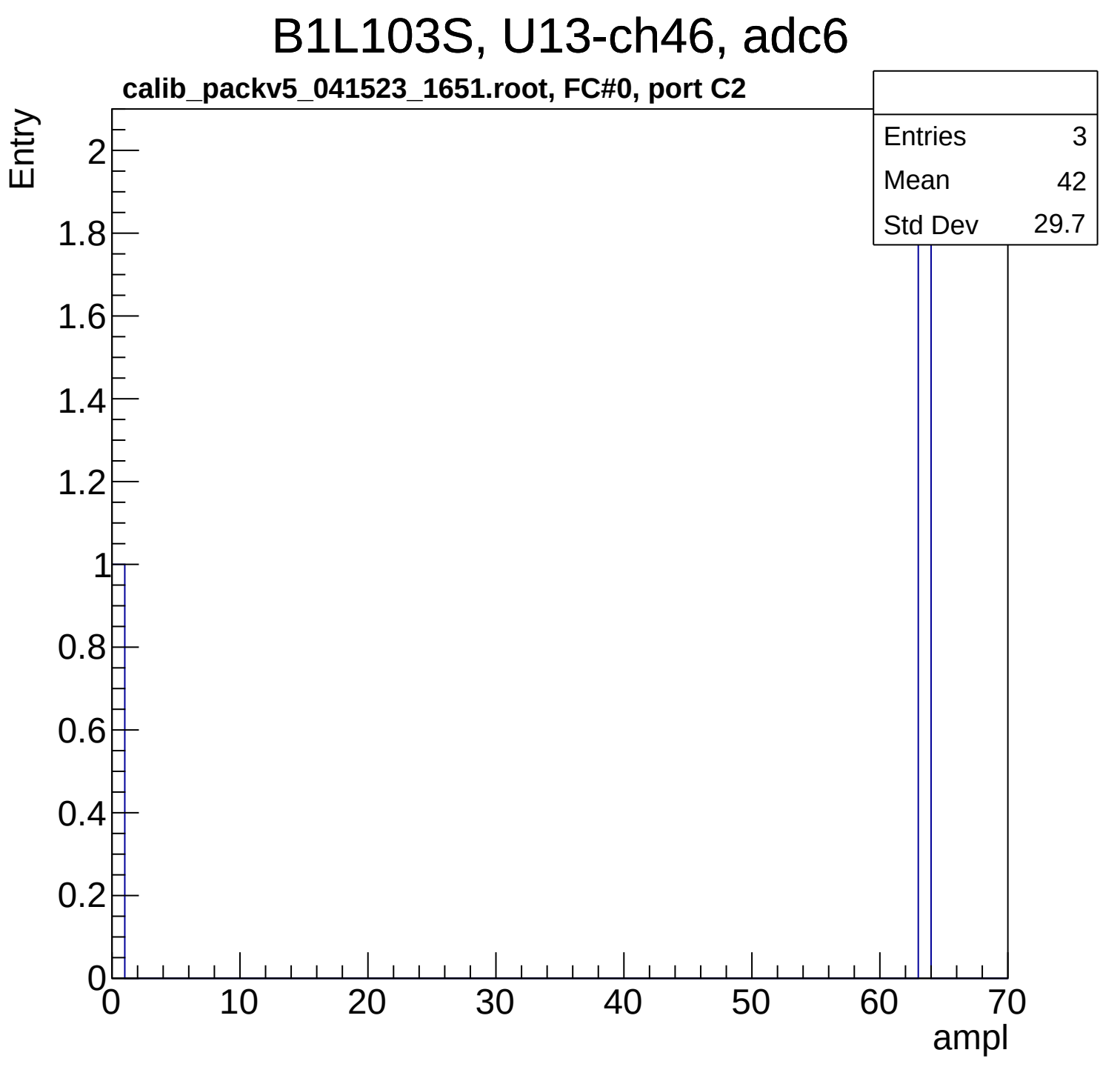
B1L103S, U13-ch46, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 42
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
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30
40
50
60
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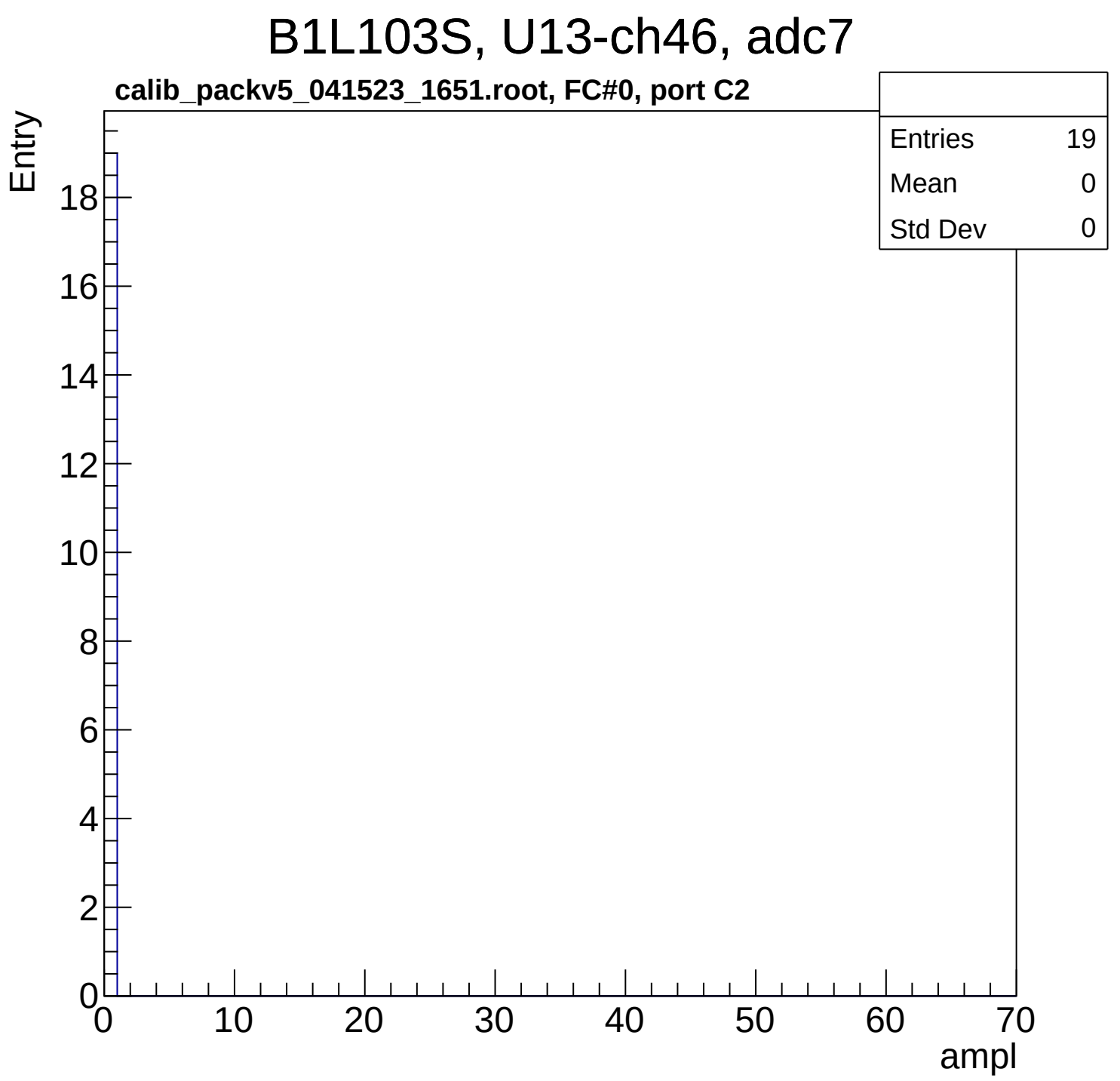
B1L103S, U13-ch46, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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10
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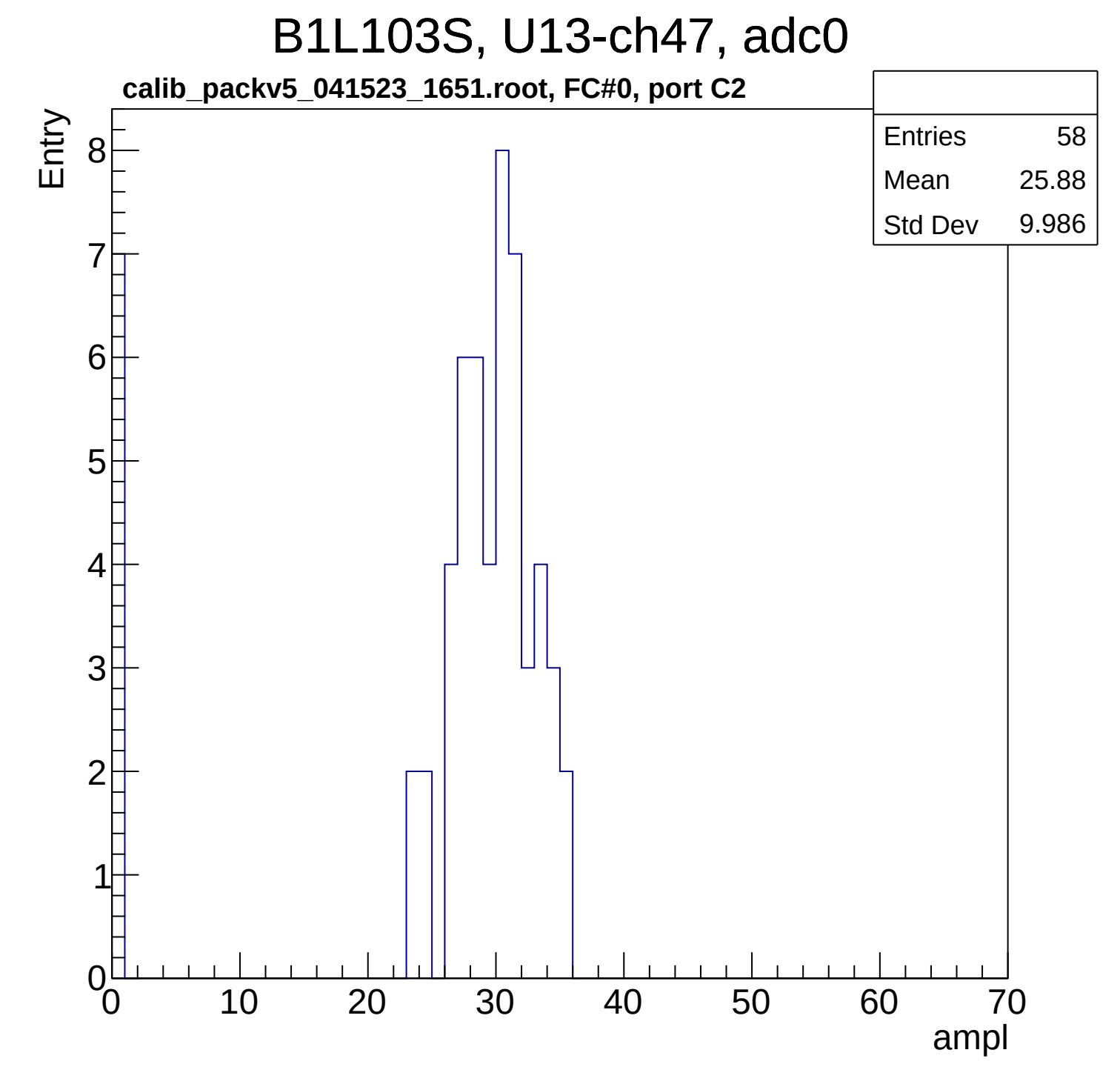
50
60
70
ampl


B1L103S, U13-ch47, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 25.88
Std Dev 9.986
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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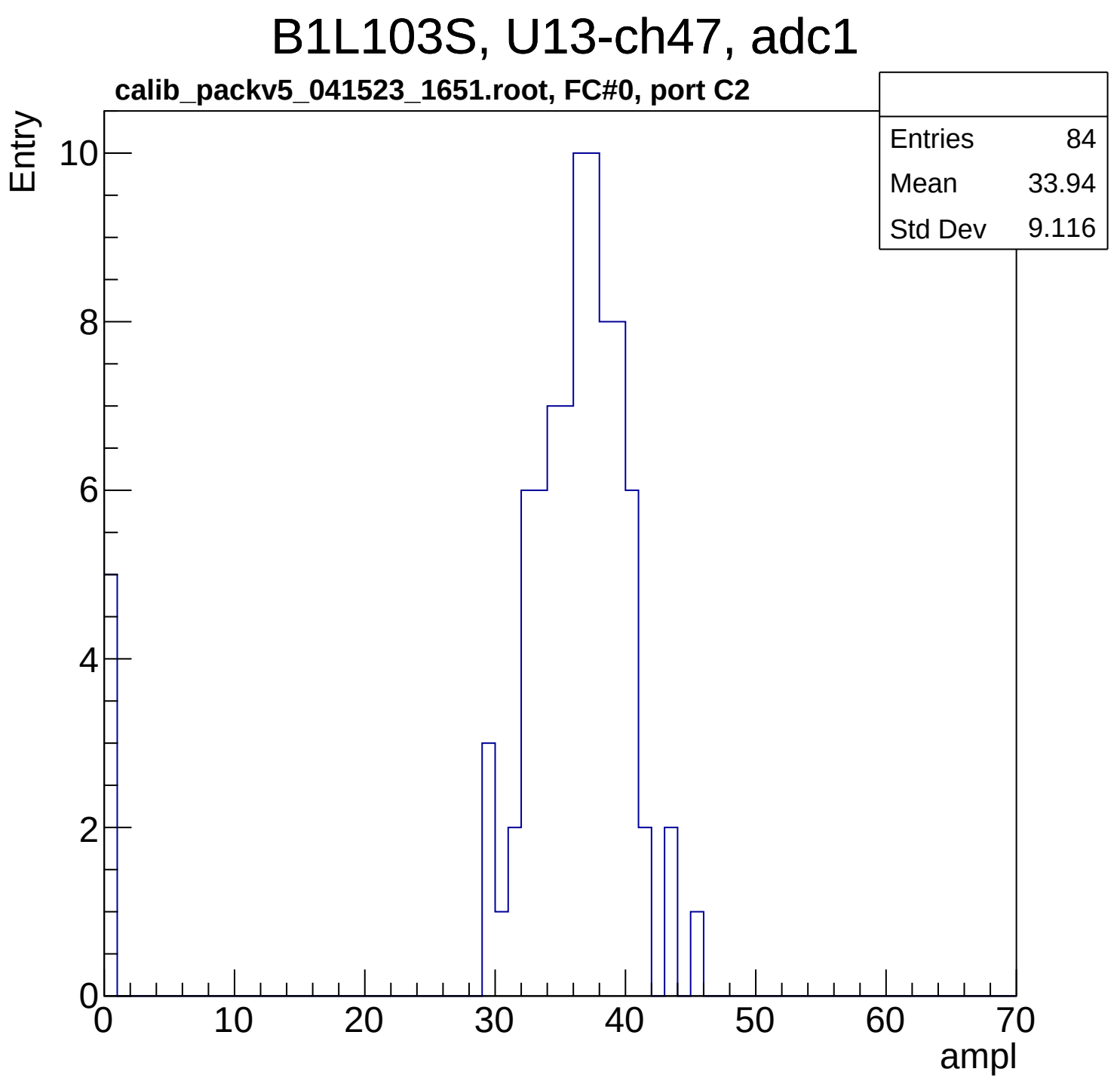
B1L103S, U13-ch47, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 33.94
Std Dev 9.116
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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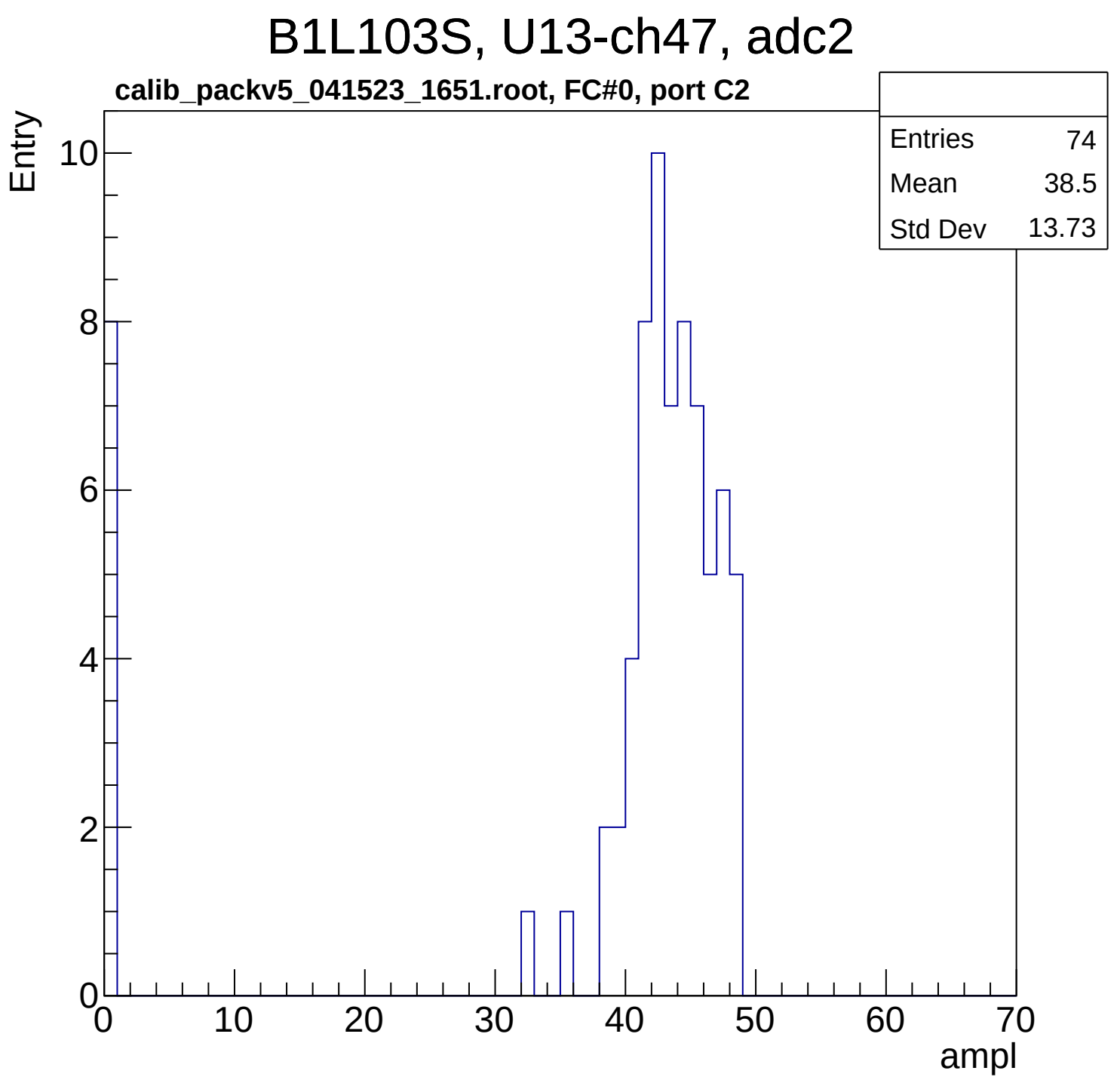
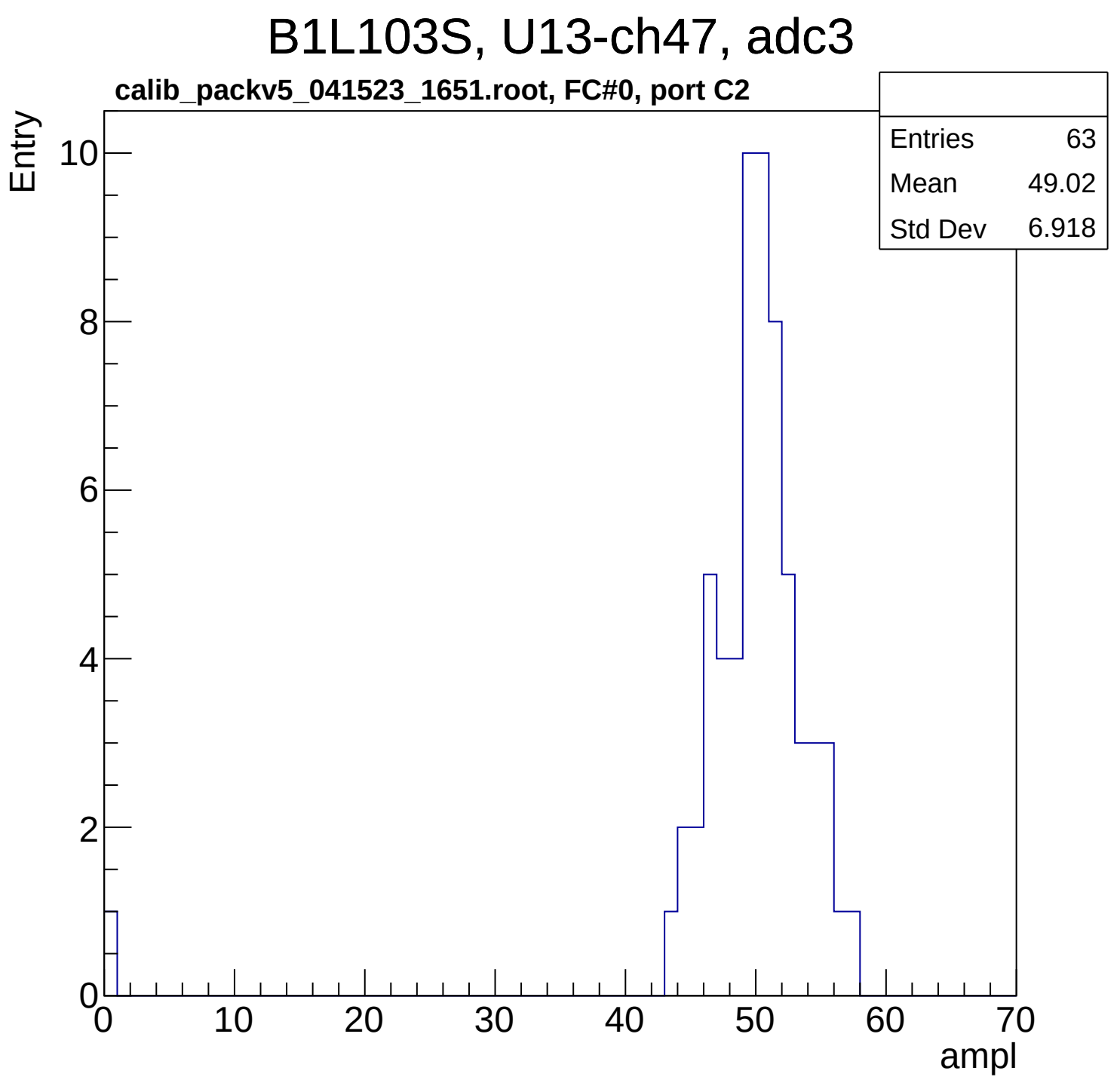
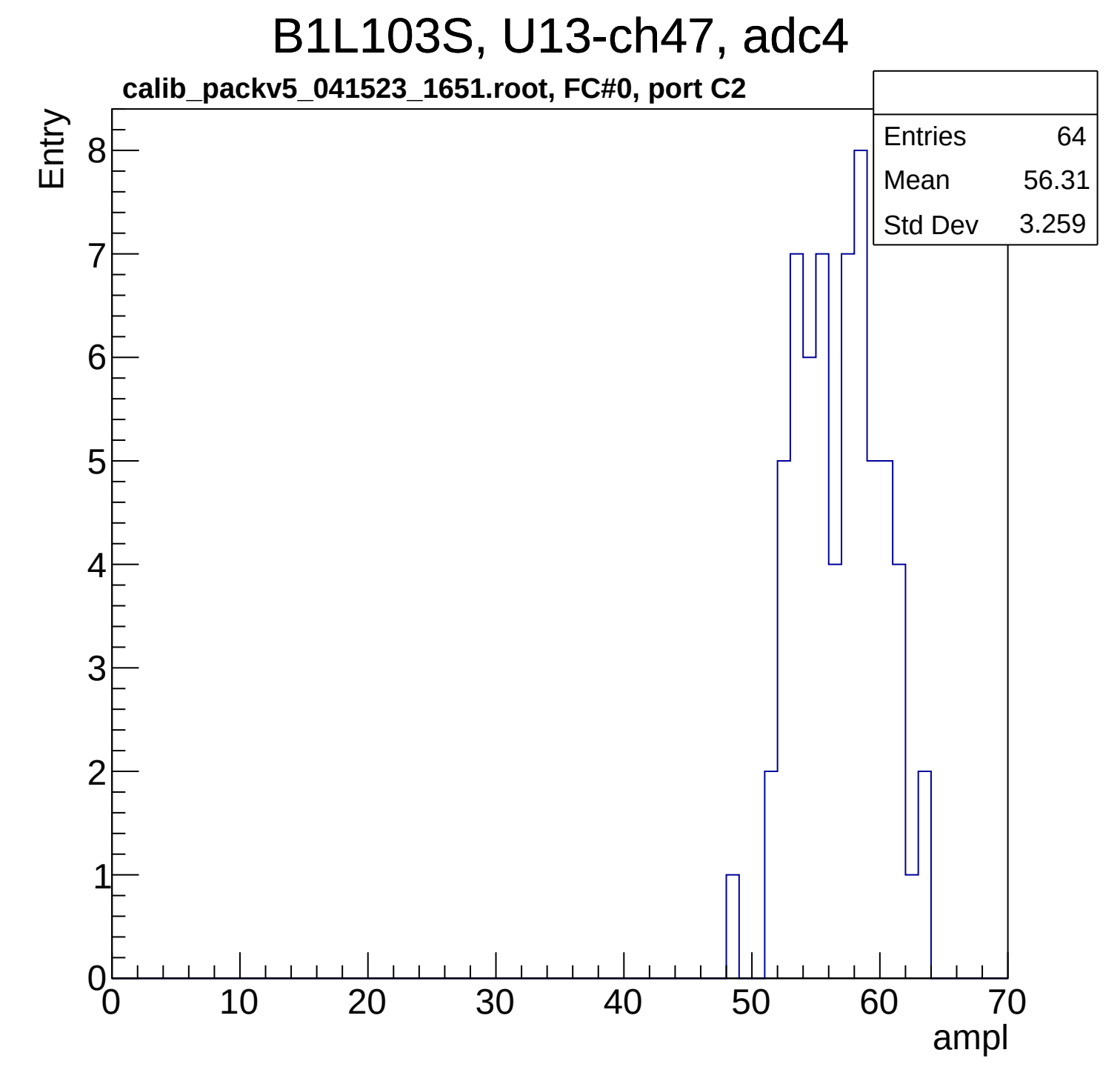
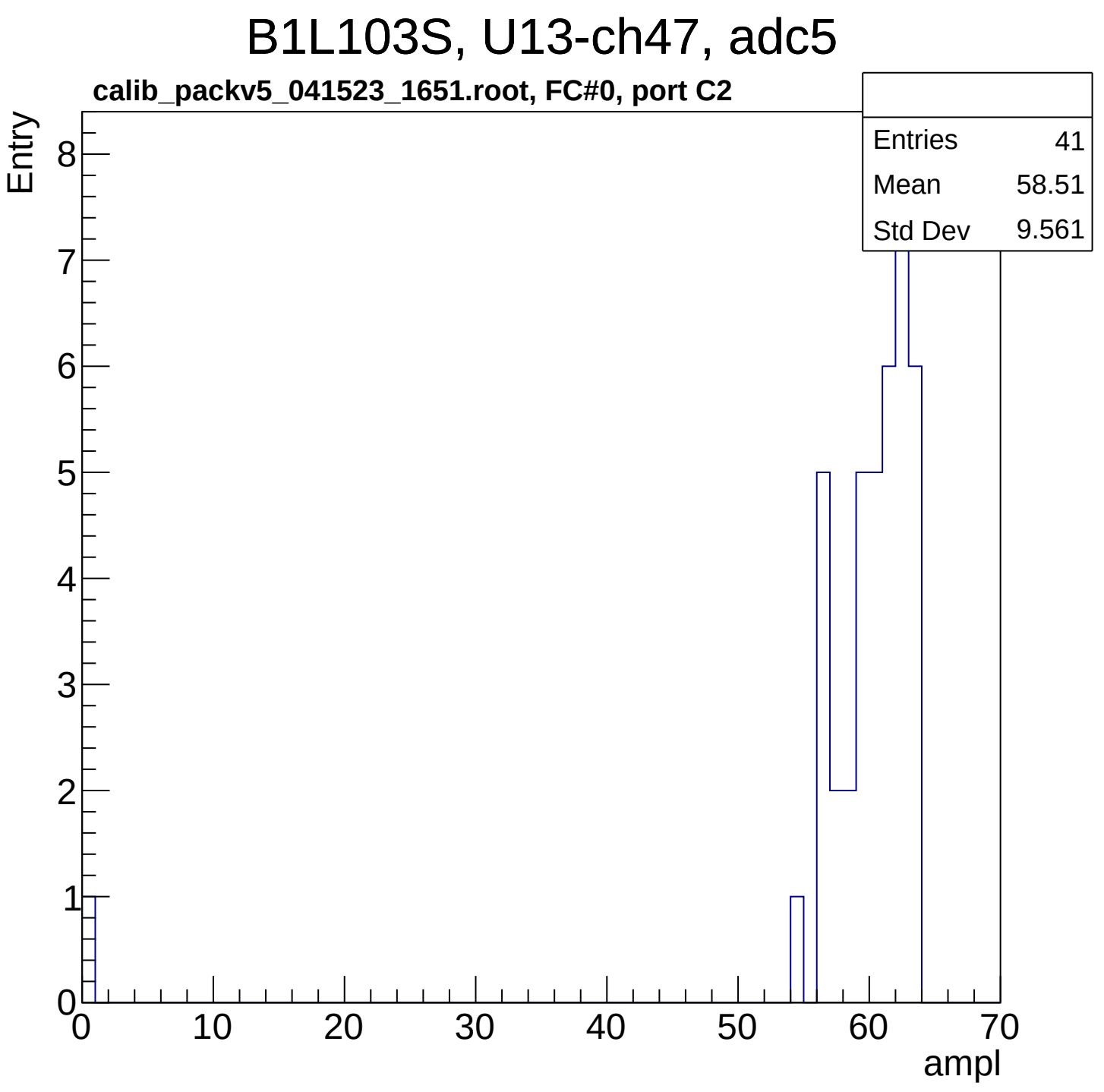
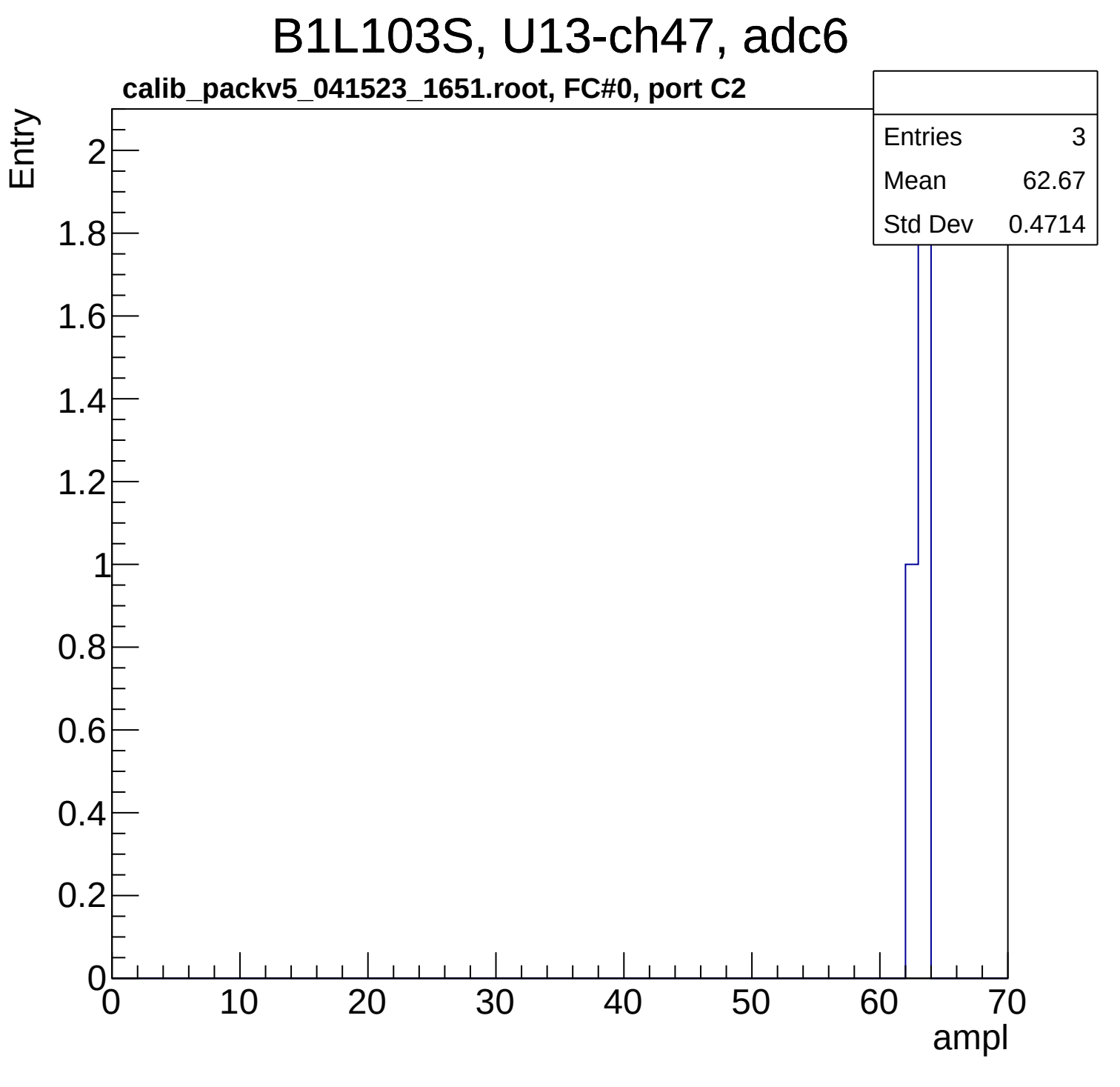
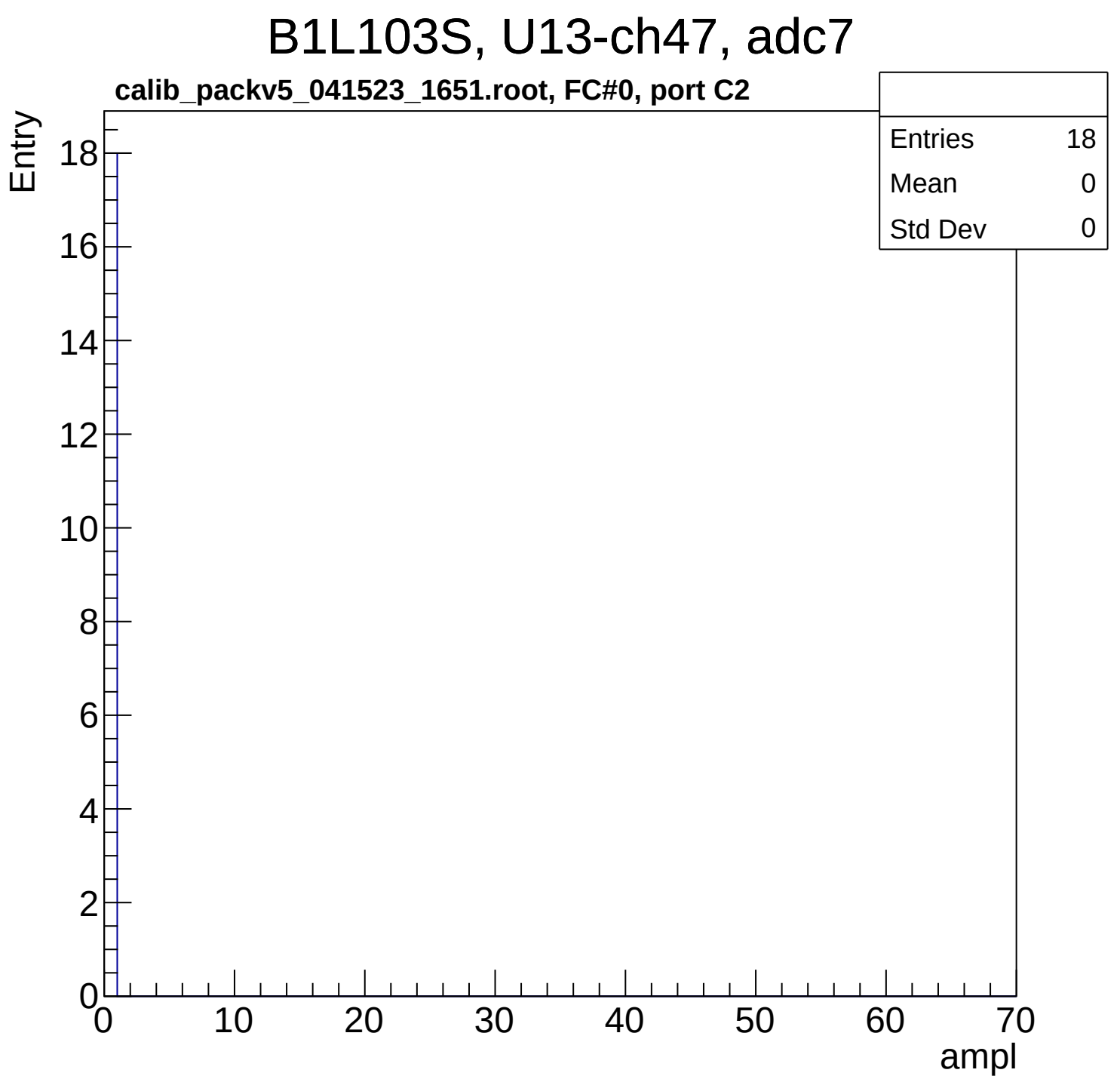

B1L103S, U13-ch47, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 38.5
Std Dev 13.73
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

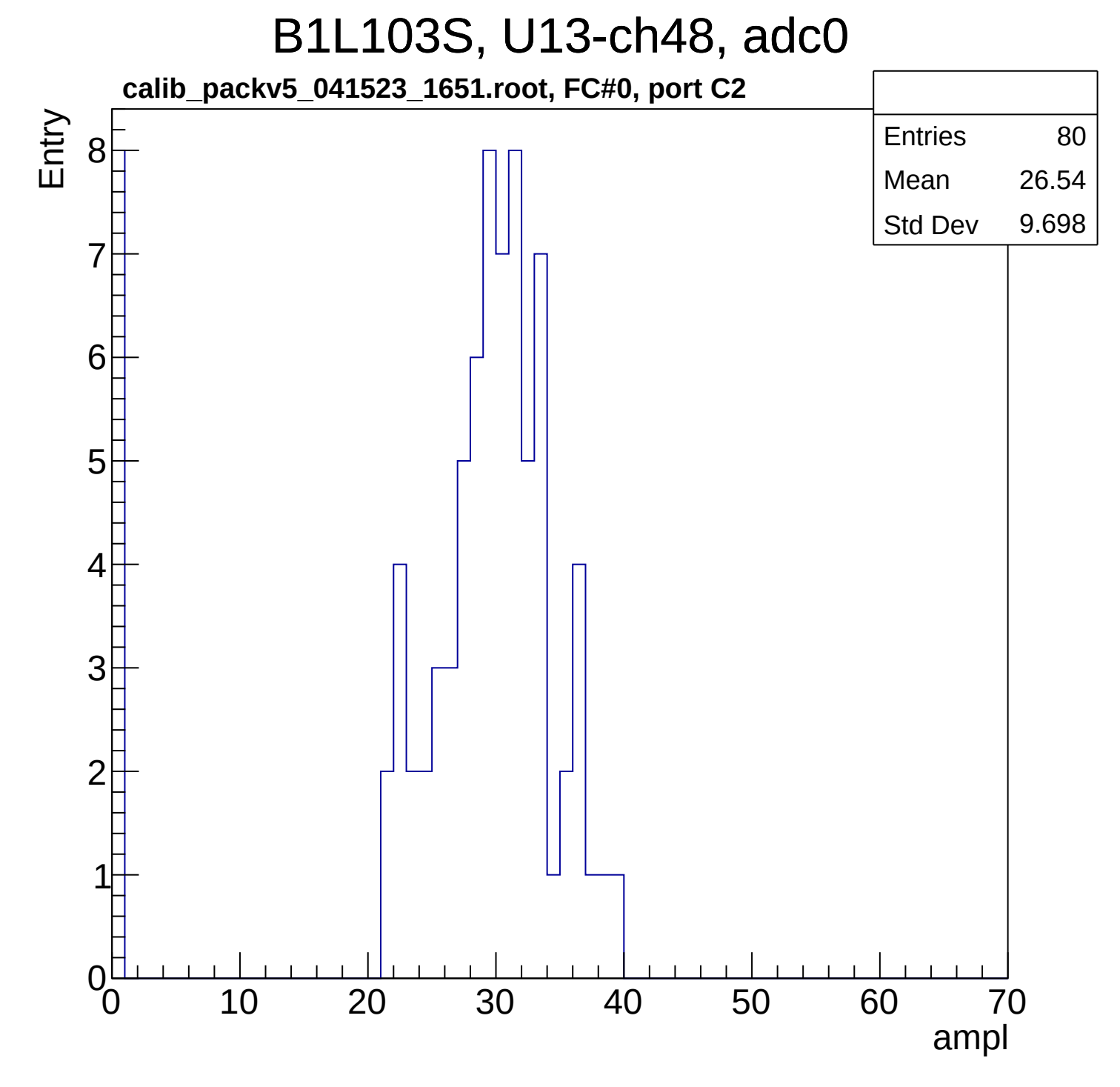

B1L103S, U13-ch47, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 49.02
Std Dev 6.918
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

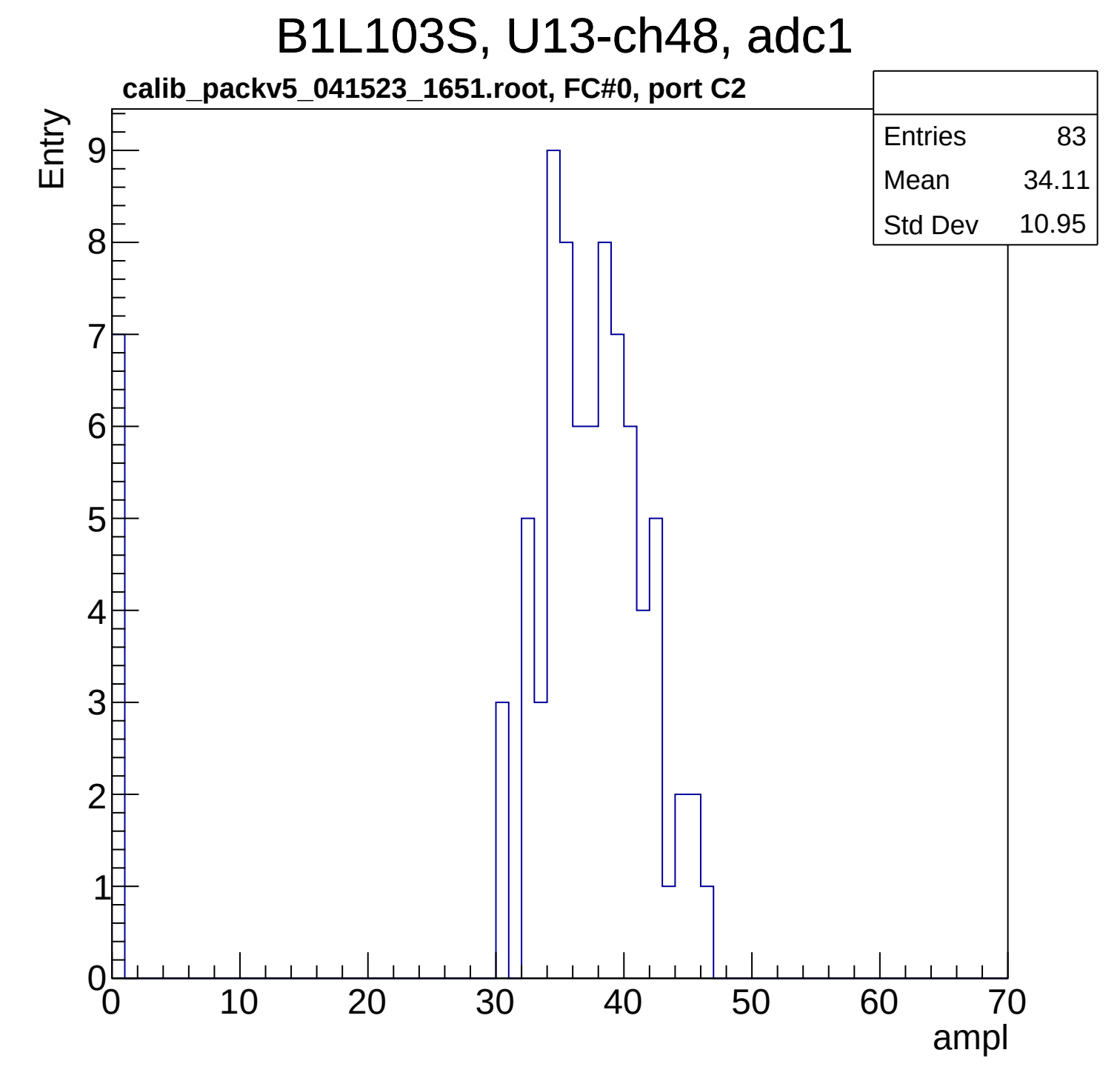

B1L103S, U13-ch47, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 56.31
Std Dev 3.259
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

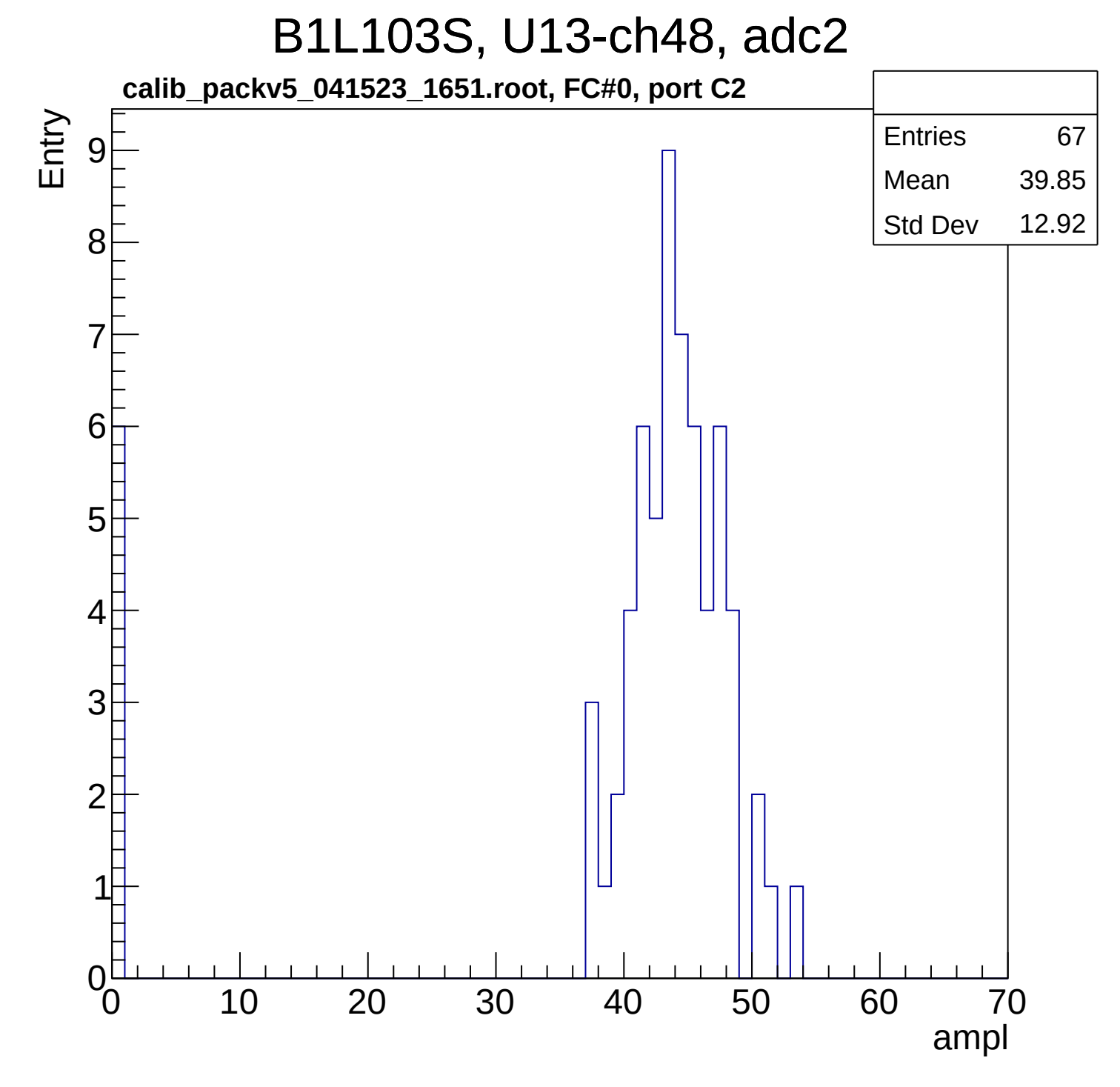

B1L103S, U13-ch47, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 58.51
Std Dev 9.561
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

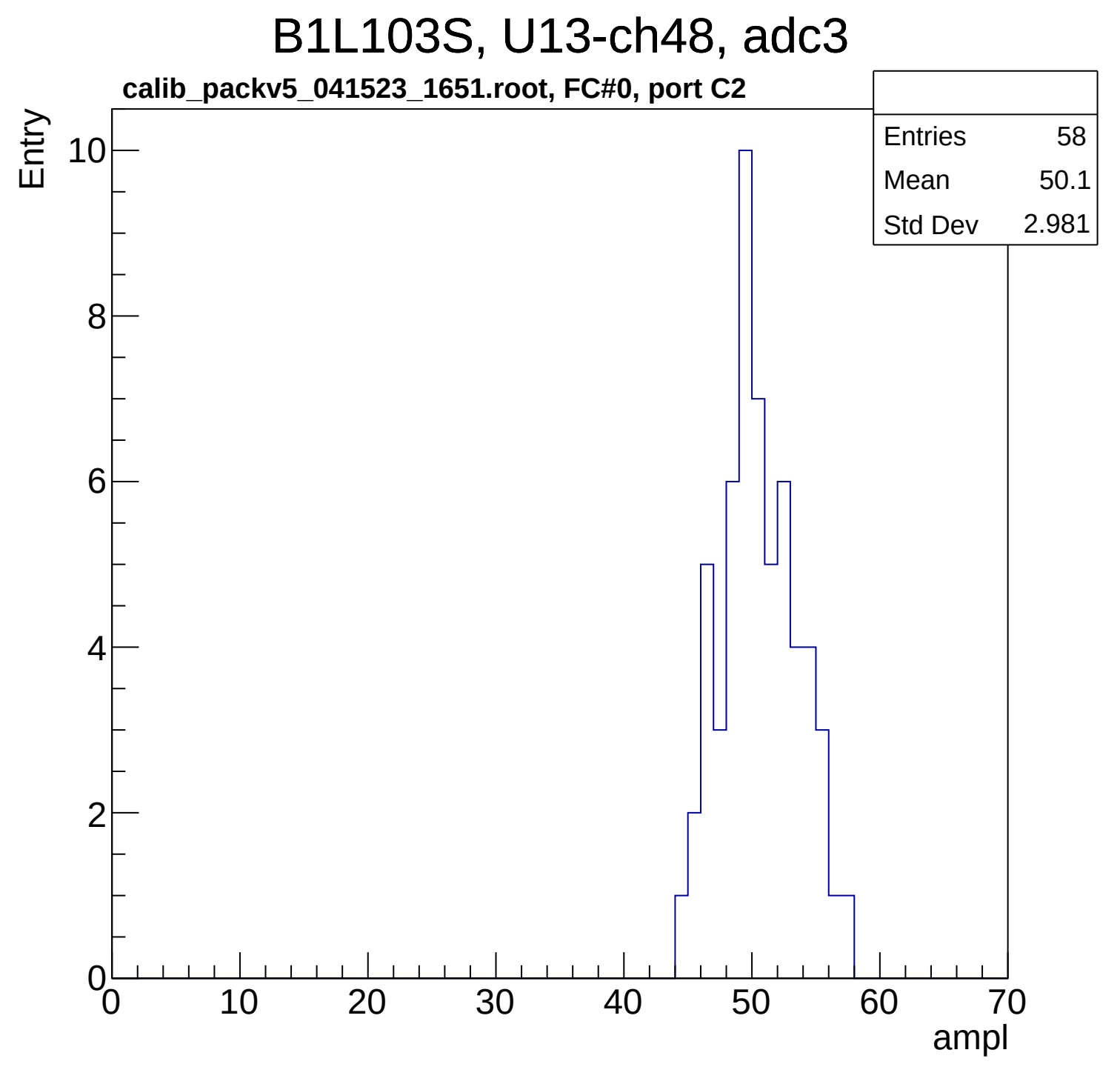

B1L103S, U13-ch47, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

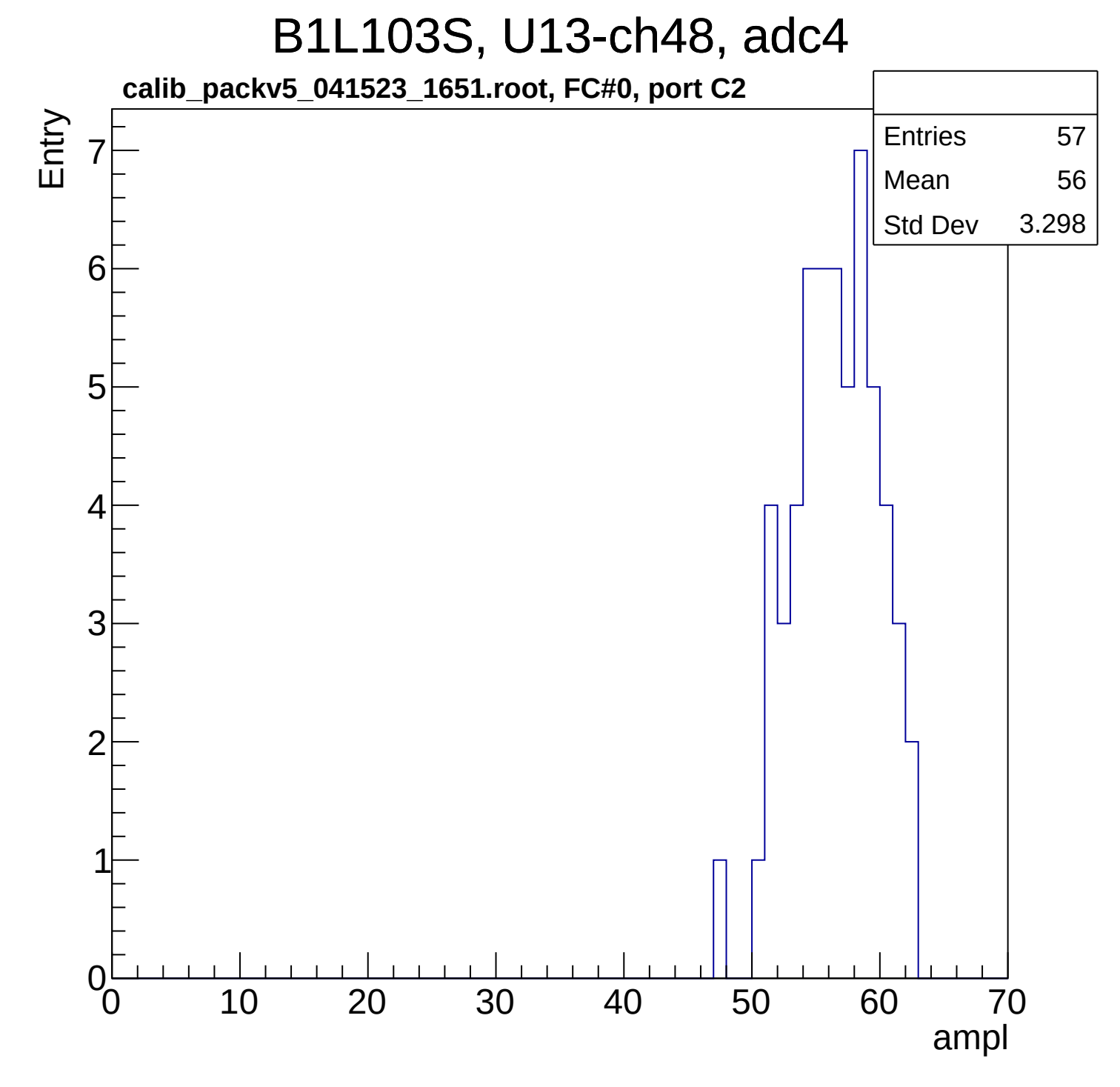

B1L103S, U13-ch47, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

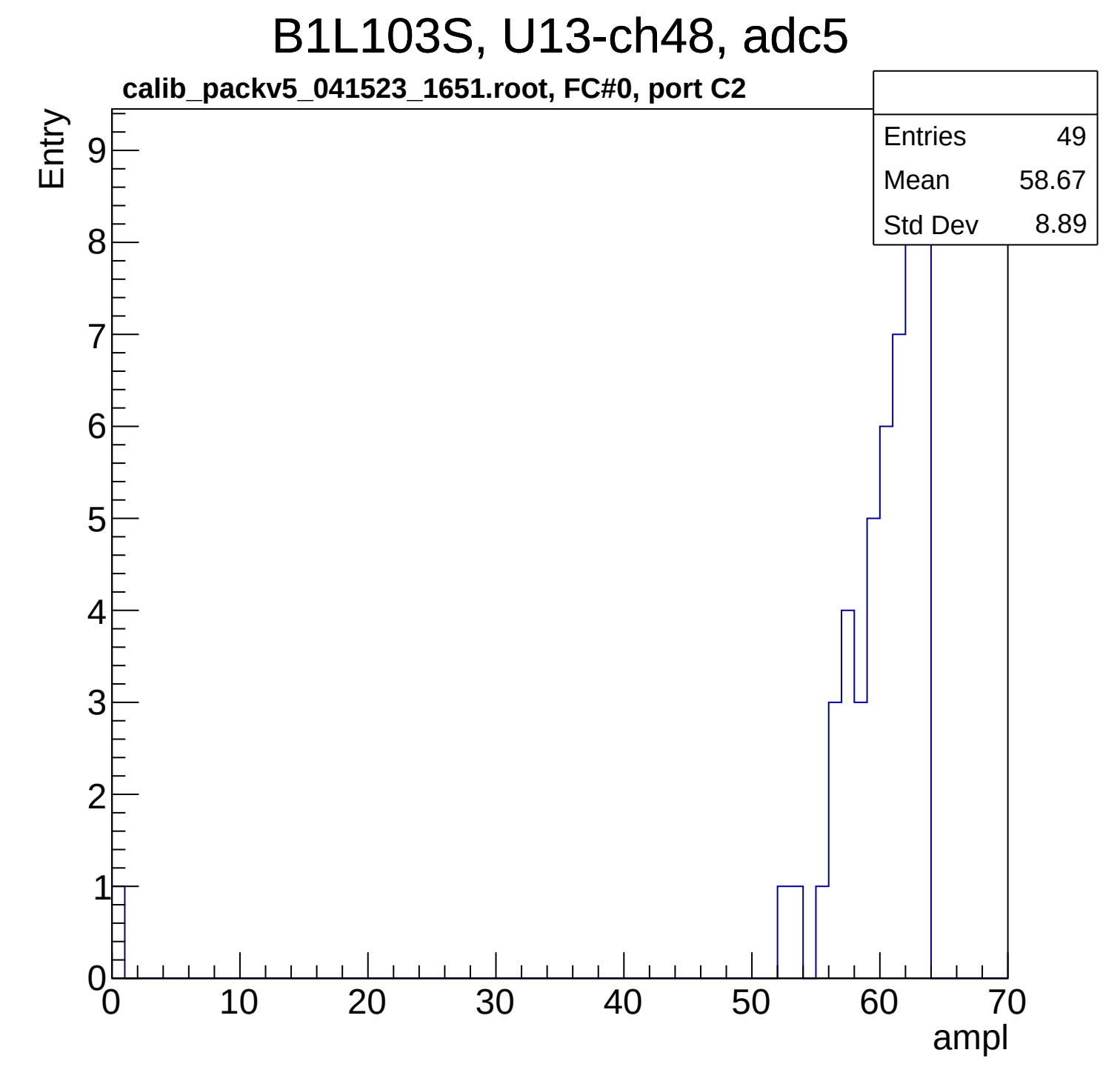

B1L103S, U13-ch48, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 26.54
Std Dev 9.698
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch48, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 34.11
Std Dev 10.95
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch48, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 39.85
Std Dev 12.92
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch48, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 50.1
Std Dev 2.981
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch48, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 56
Std Dev 3.298
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch48, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.67
Std Dev 8.89
Entry
ampl
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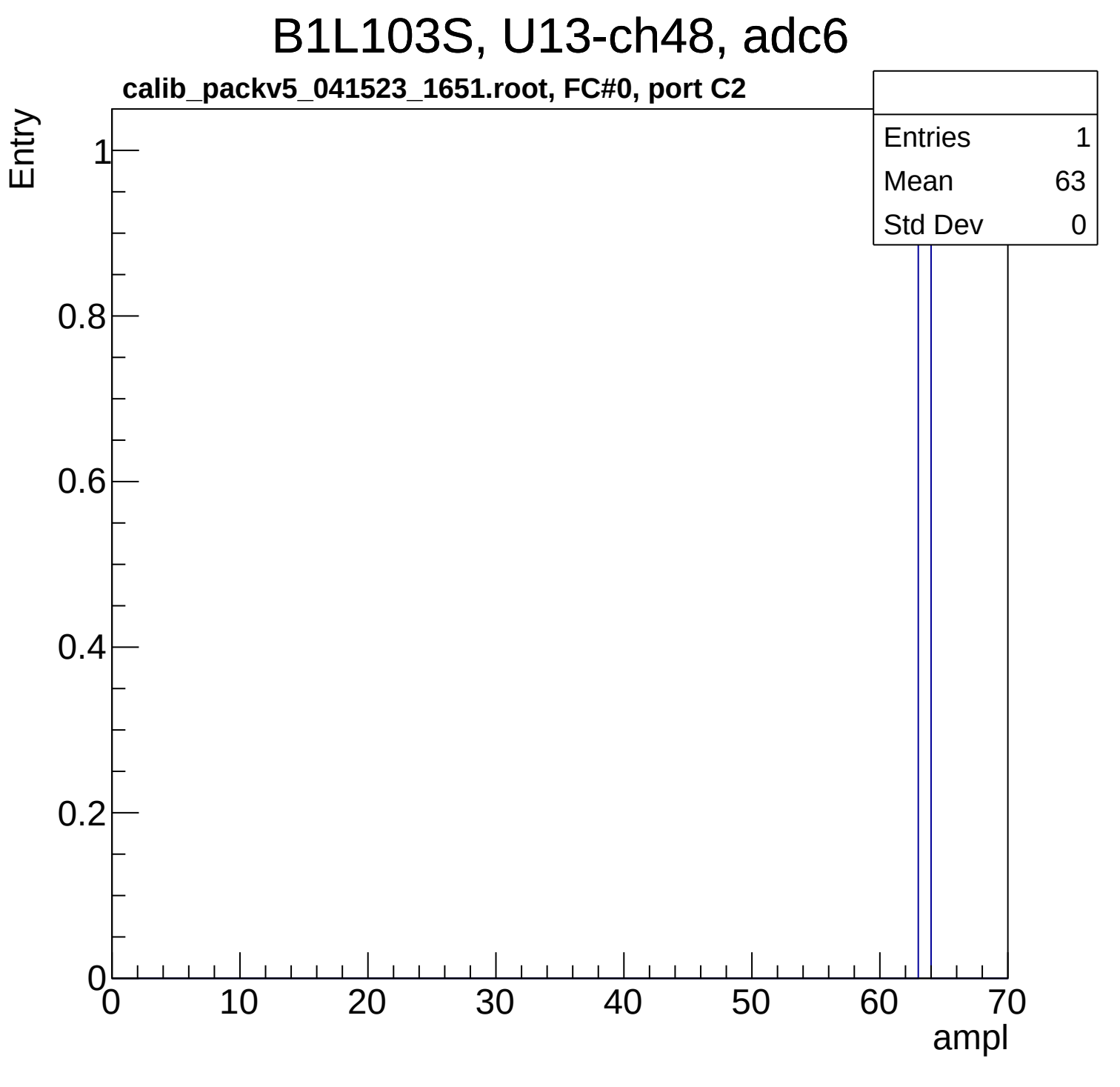
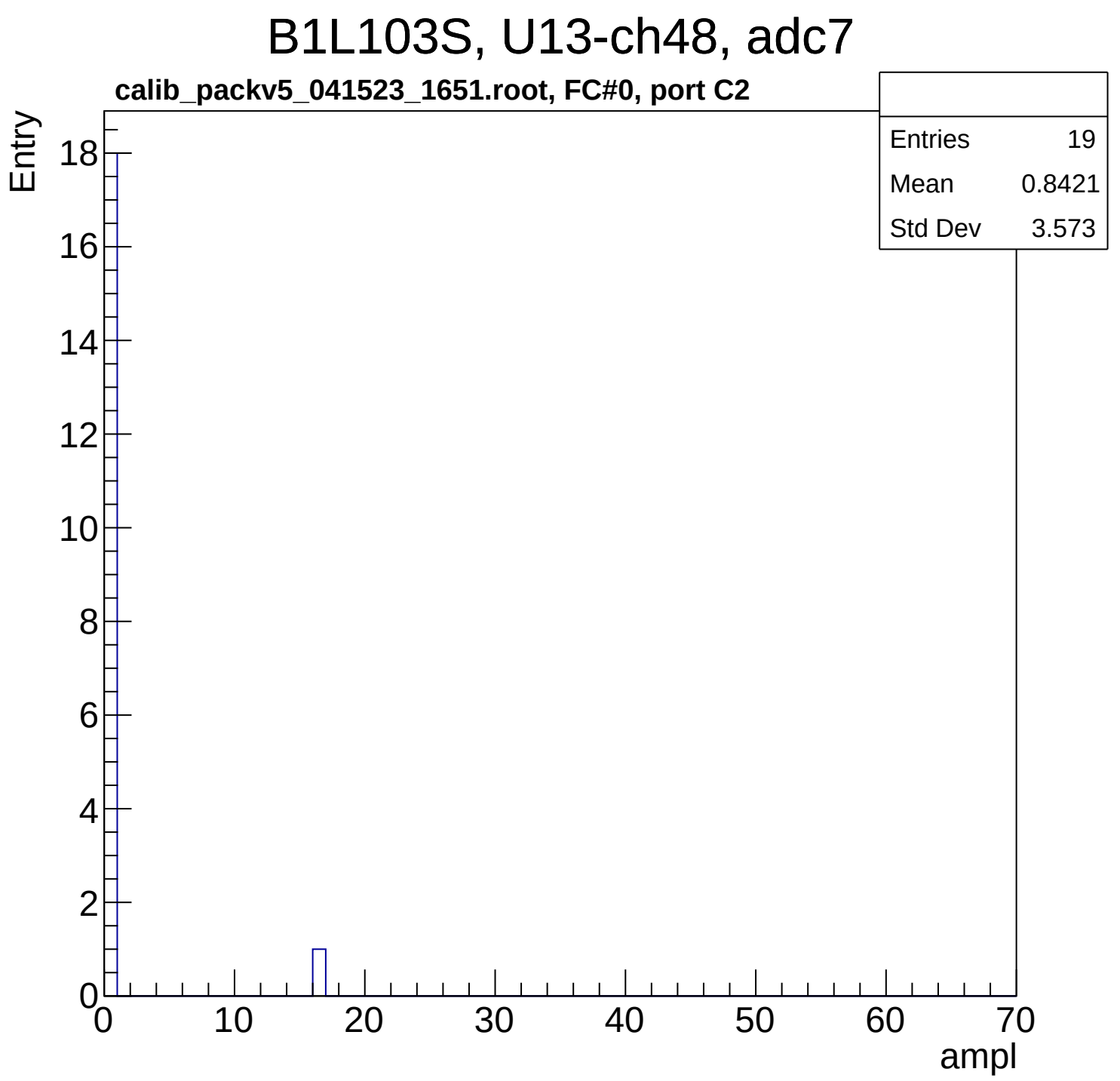
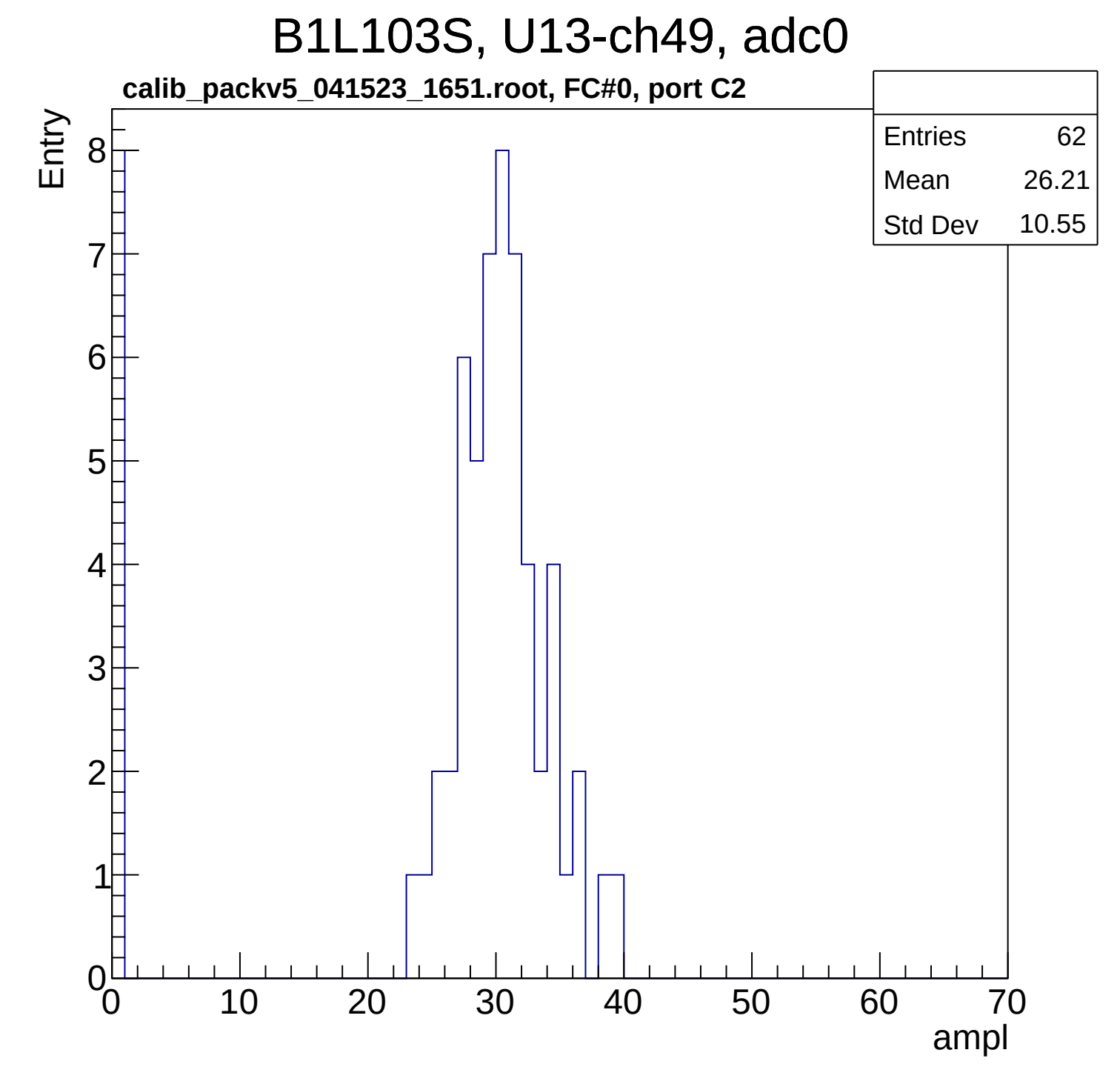
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch48, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch48, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0.8421
Std Dev 3.573
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch49, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 26.21
Std Dev 10.55
Entry
ampl
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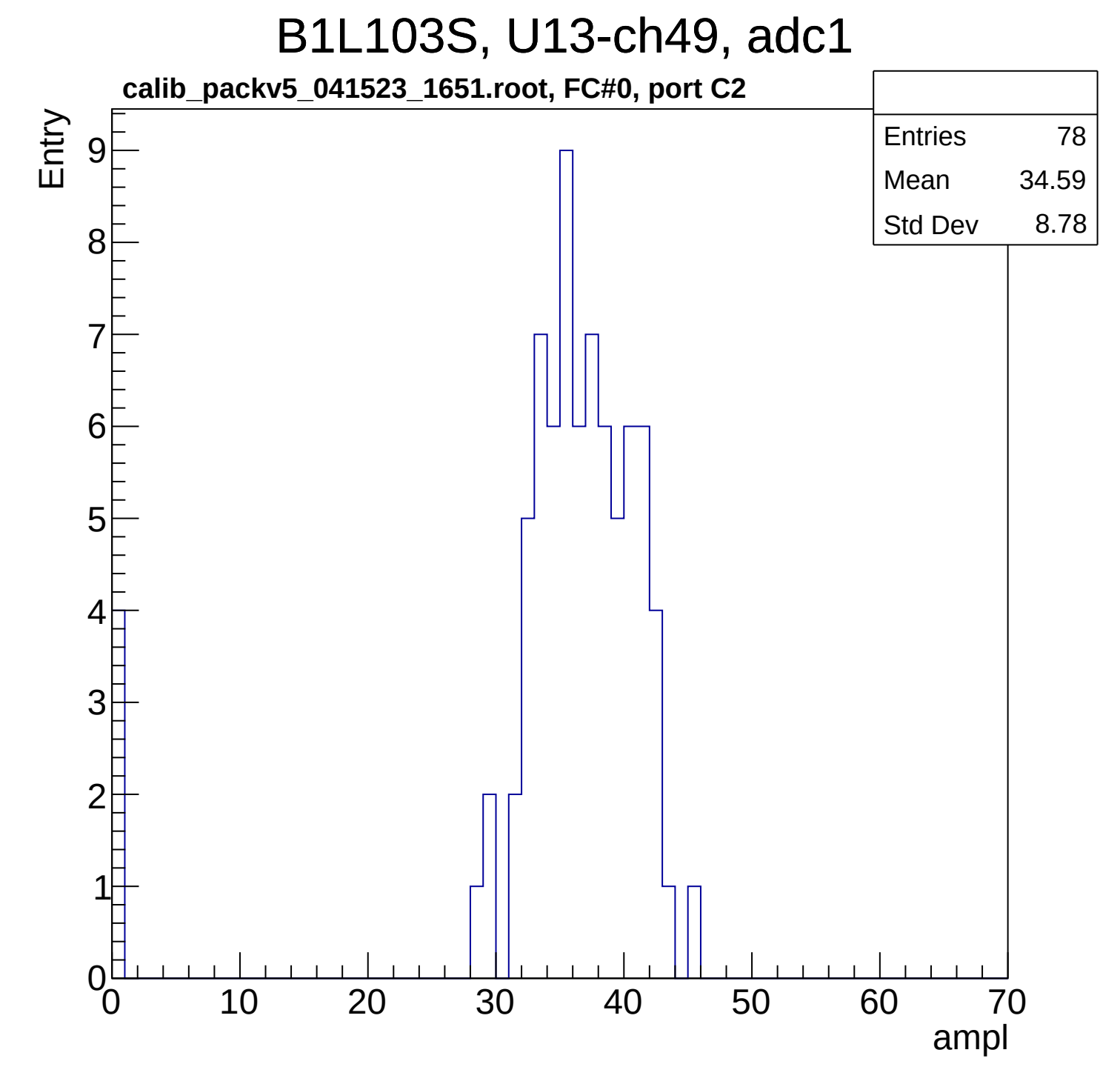
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch49, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 34.59
Std Dev 8.78
Entry
ampl
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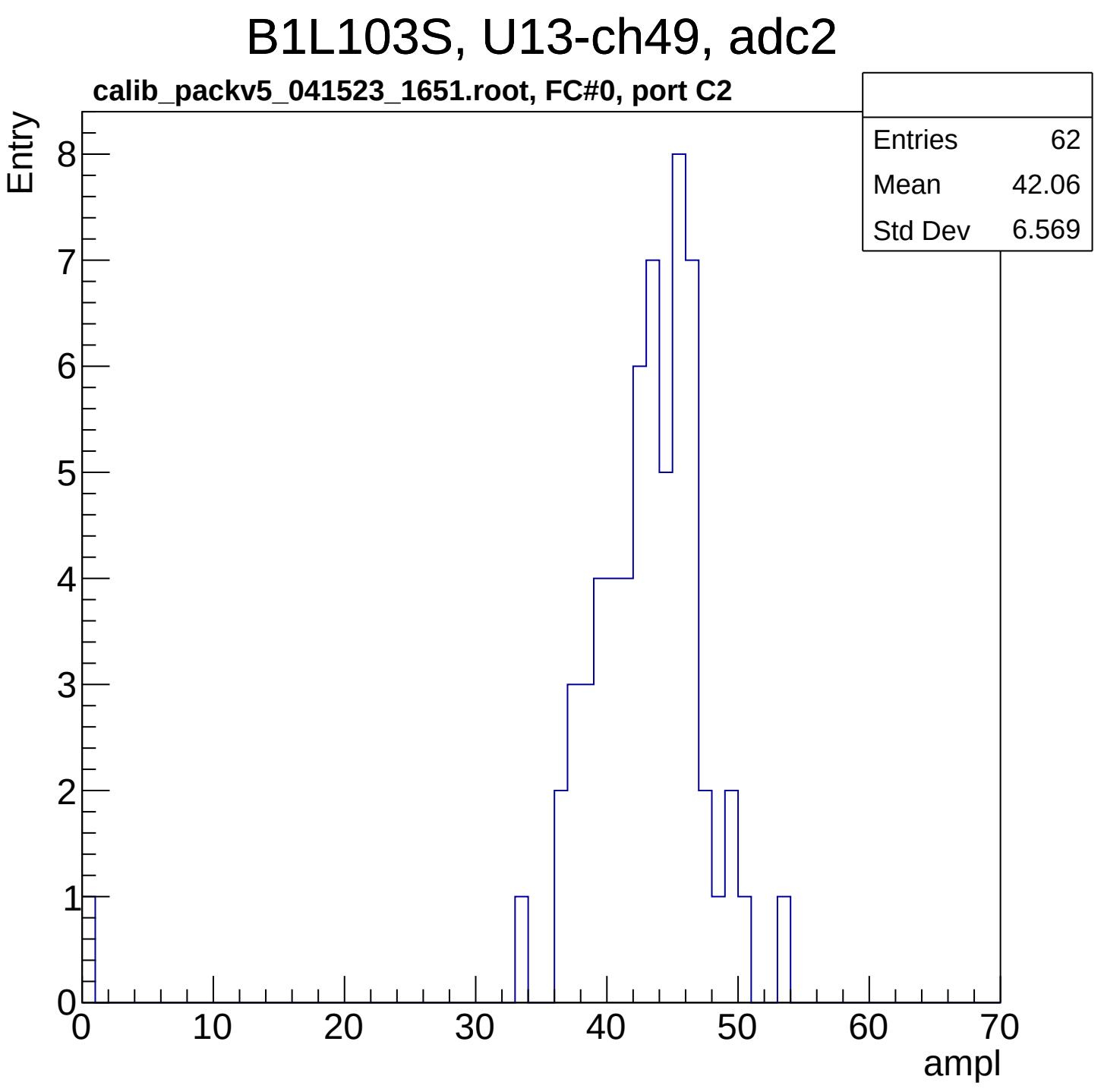
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch49, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 42.06
Std Dev 6.569
Entry
ampl
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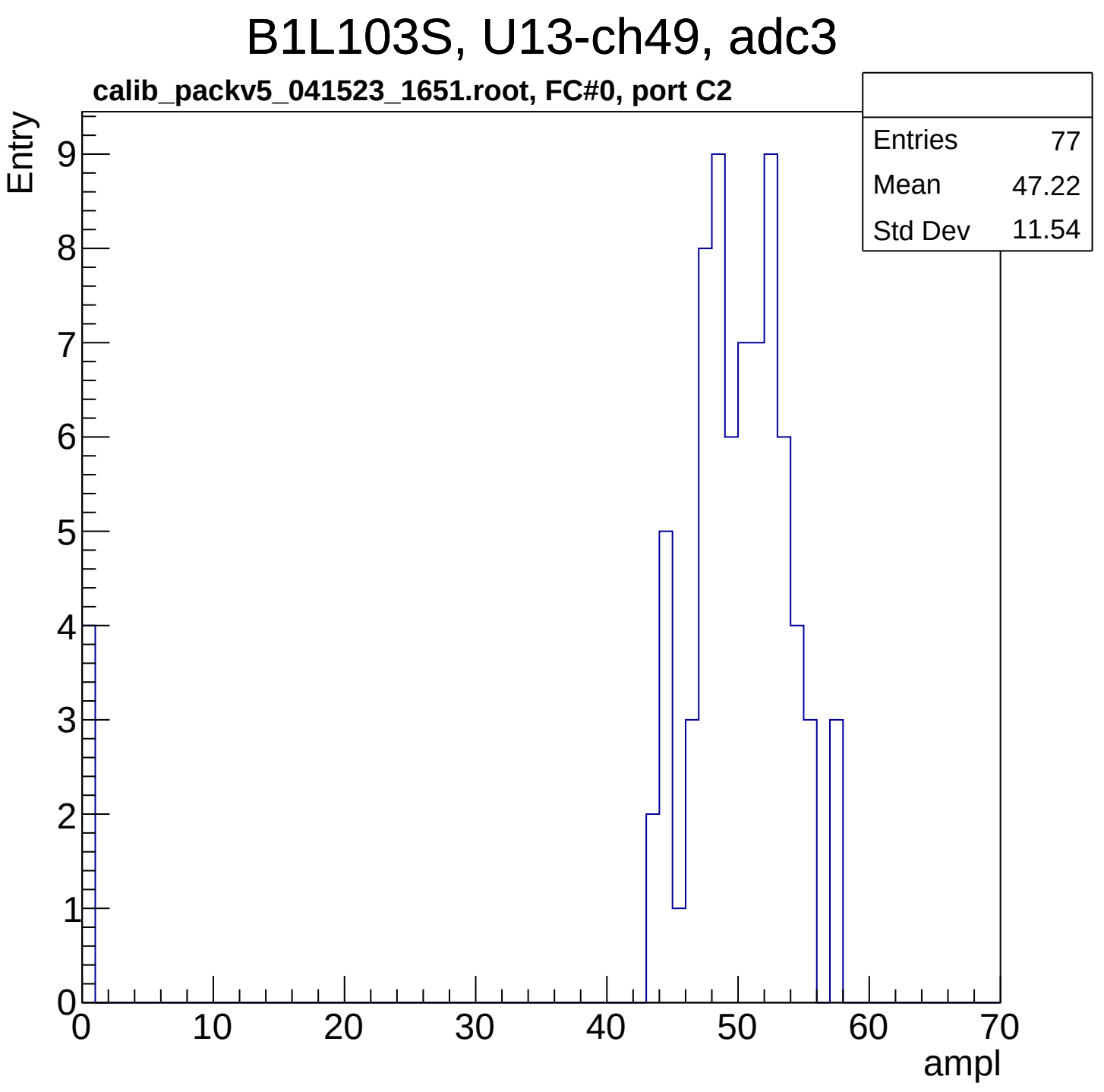
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch49, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 47.22
Std Dev 11.54
Entry
ampl
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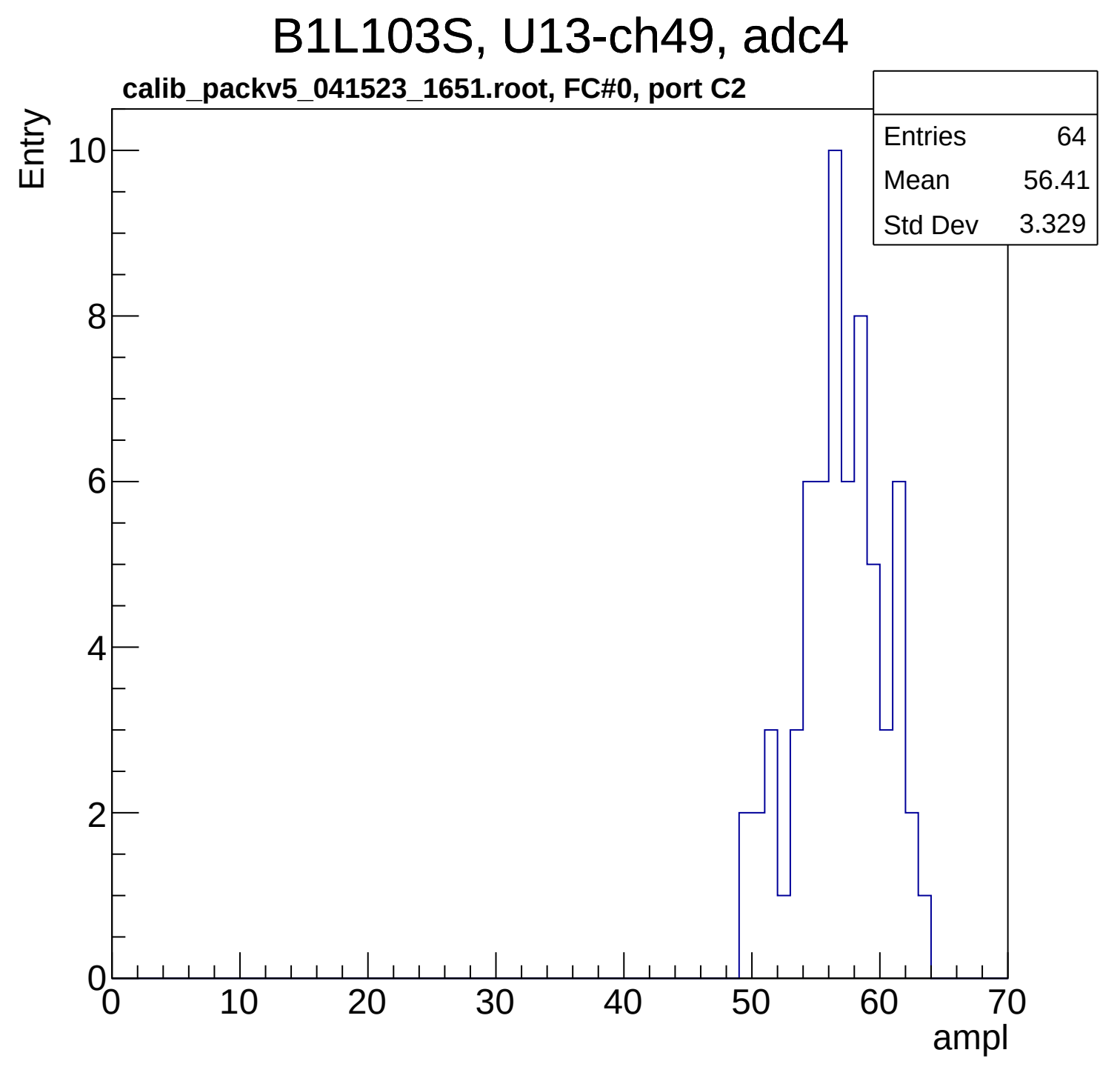
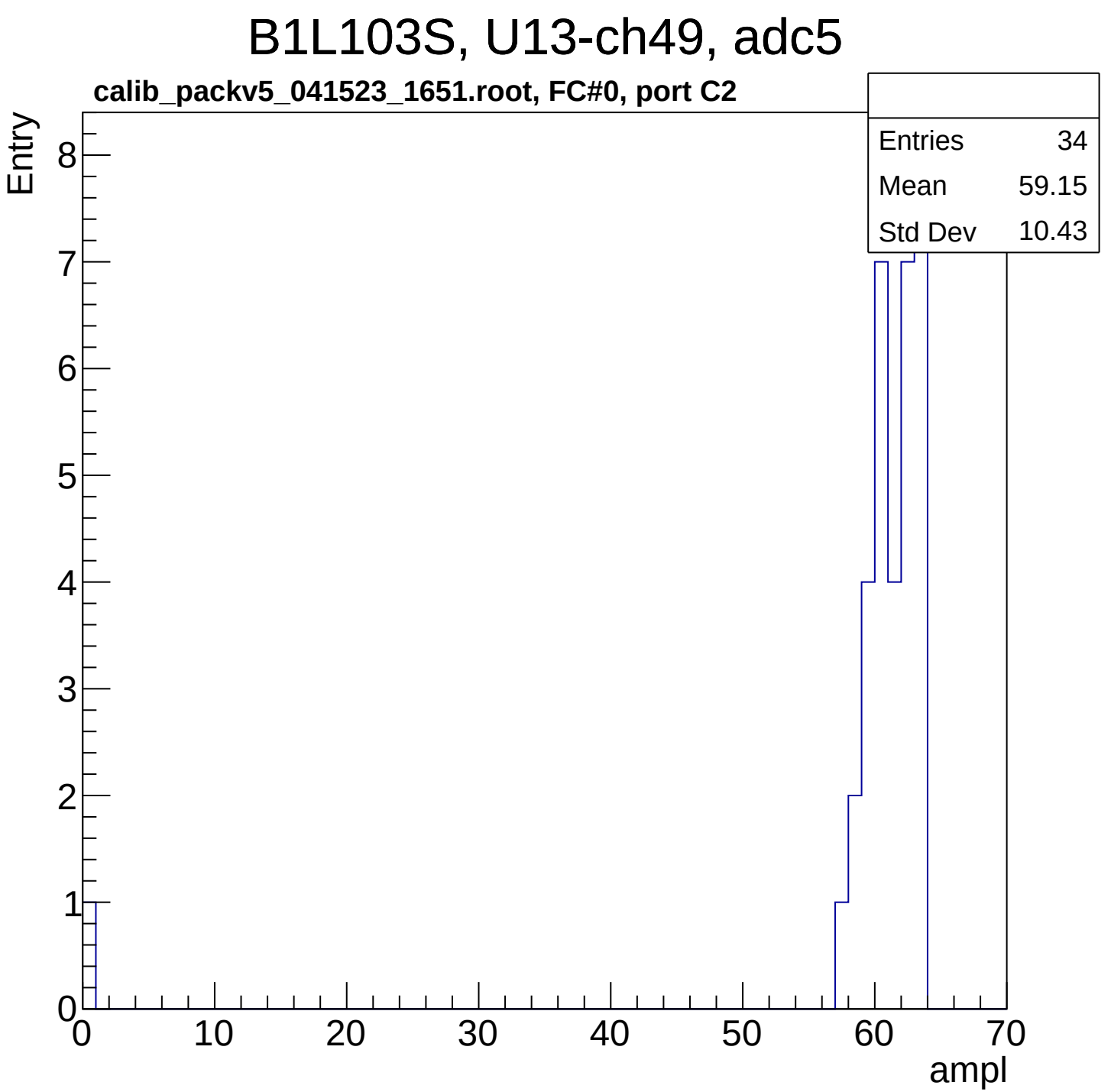
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch49, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 56.41
Std Dev 3.329
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch49, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 59.15
Std Dev 10.43
Entry
ampl
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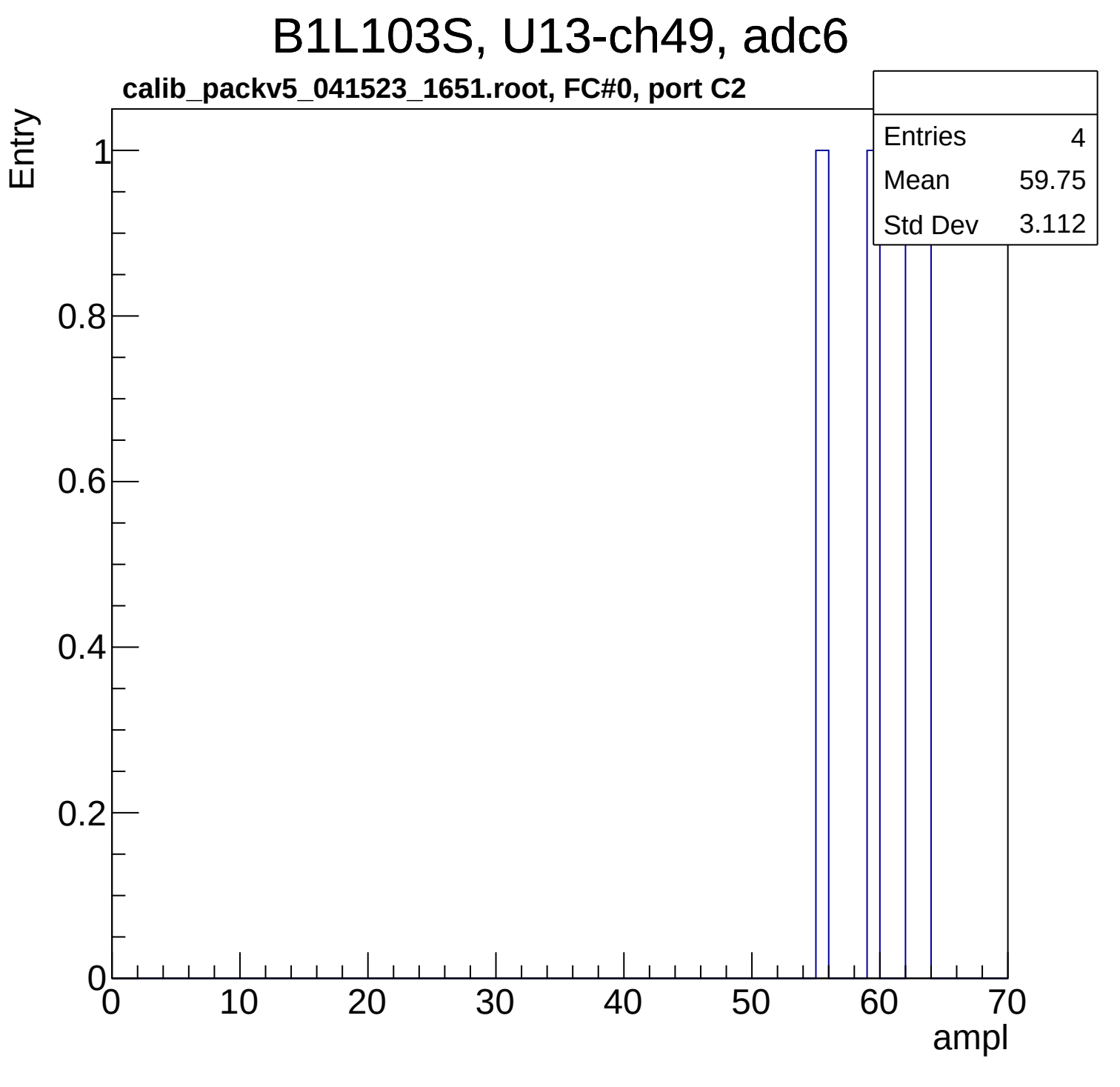
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch49, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 59.75
Std Dev 3.112
Entry
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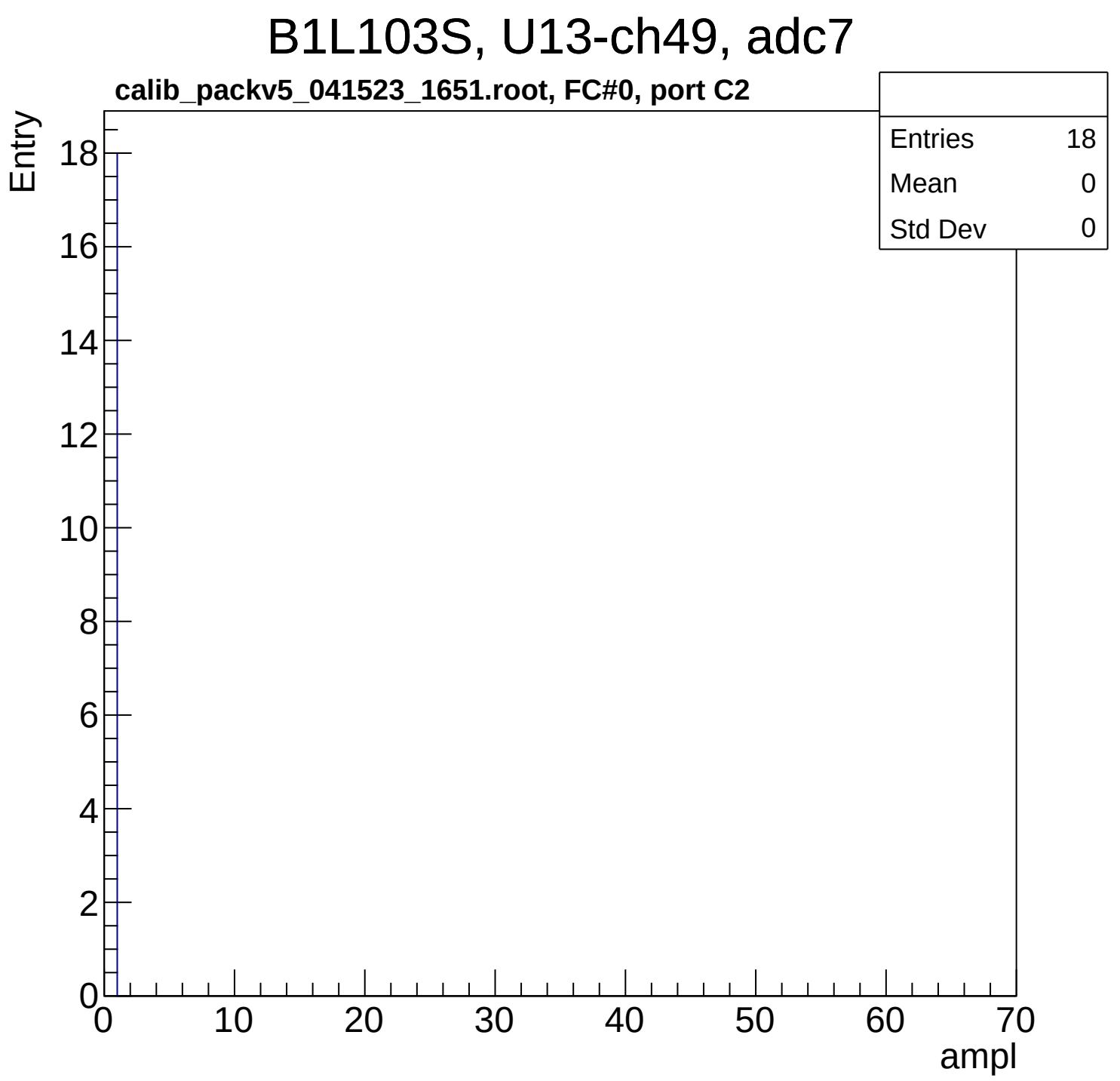
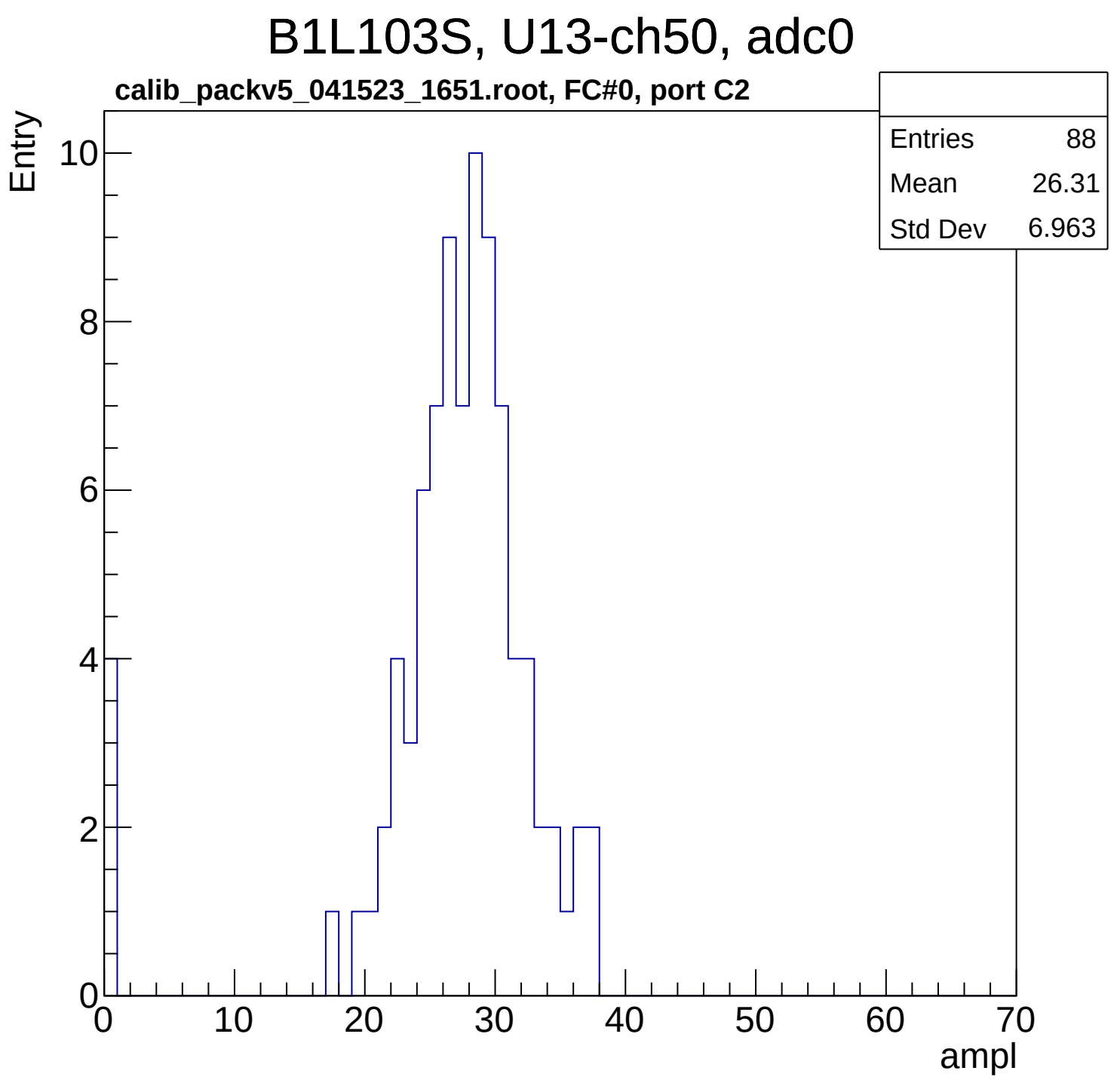
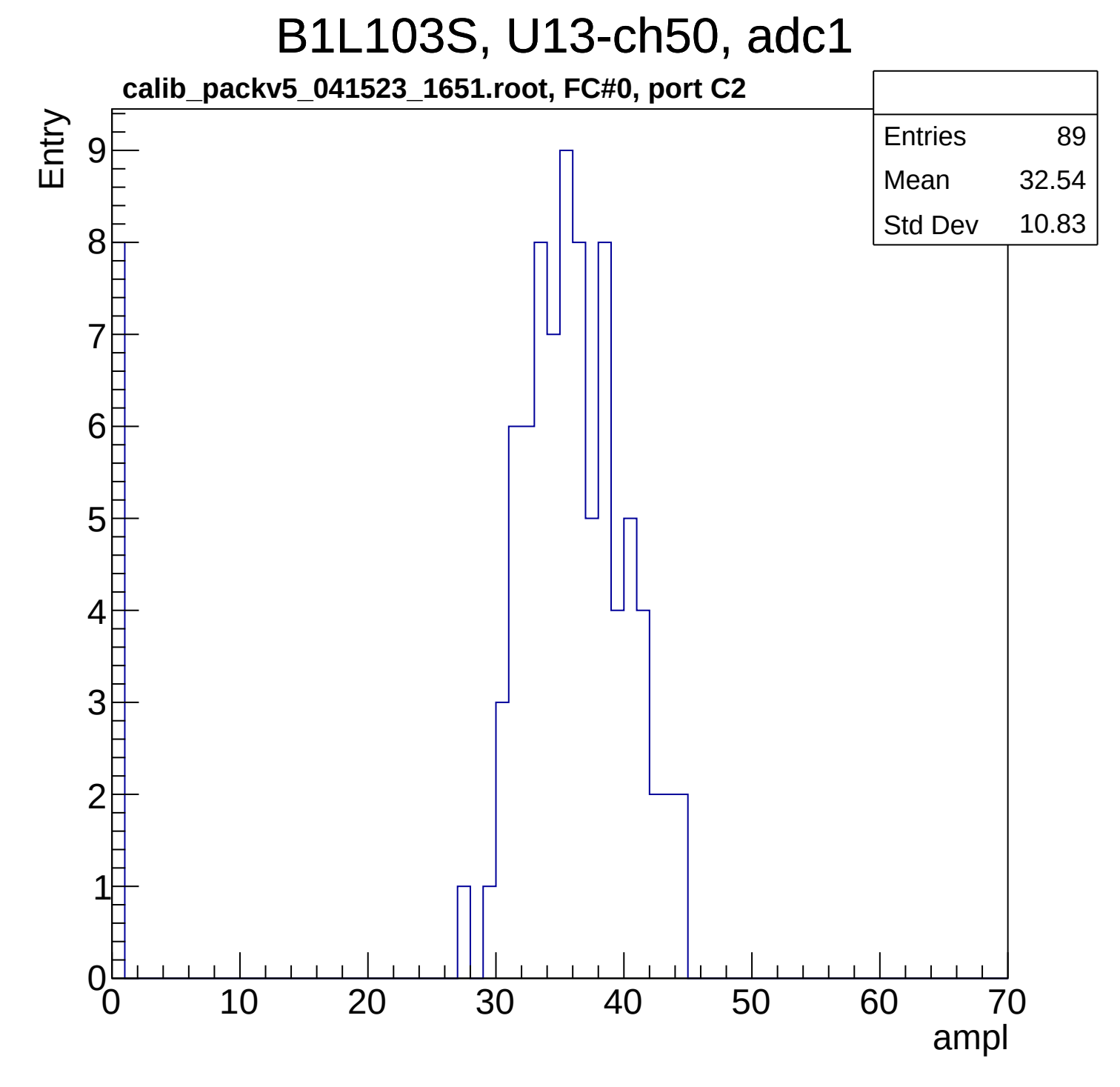
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch49, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch50, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 26.31
Std Dev 6.963
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch50, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 32.54
Std Dev 10.83
Entry
ampl
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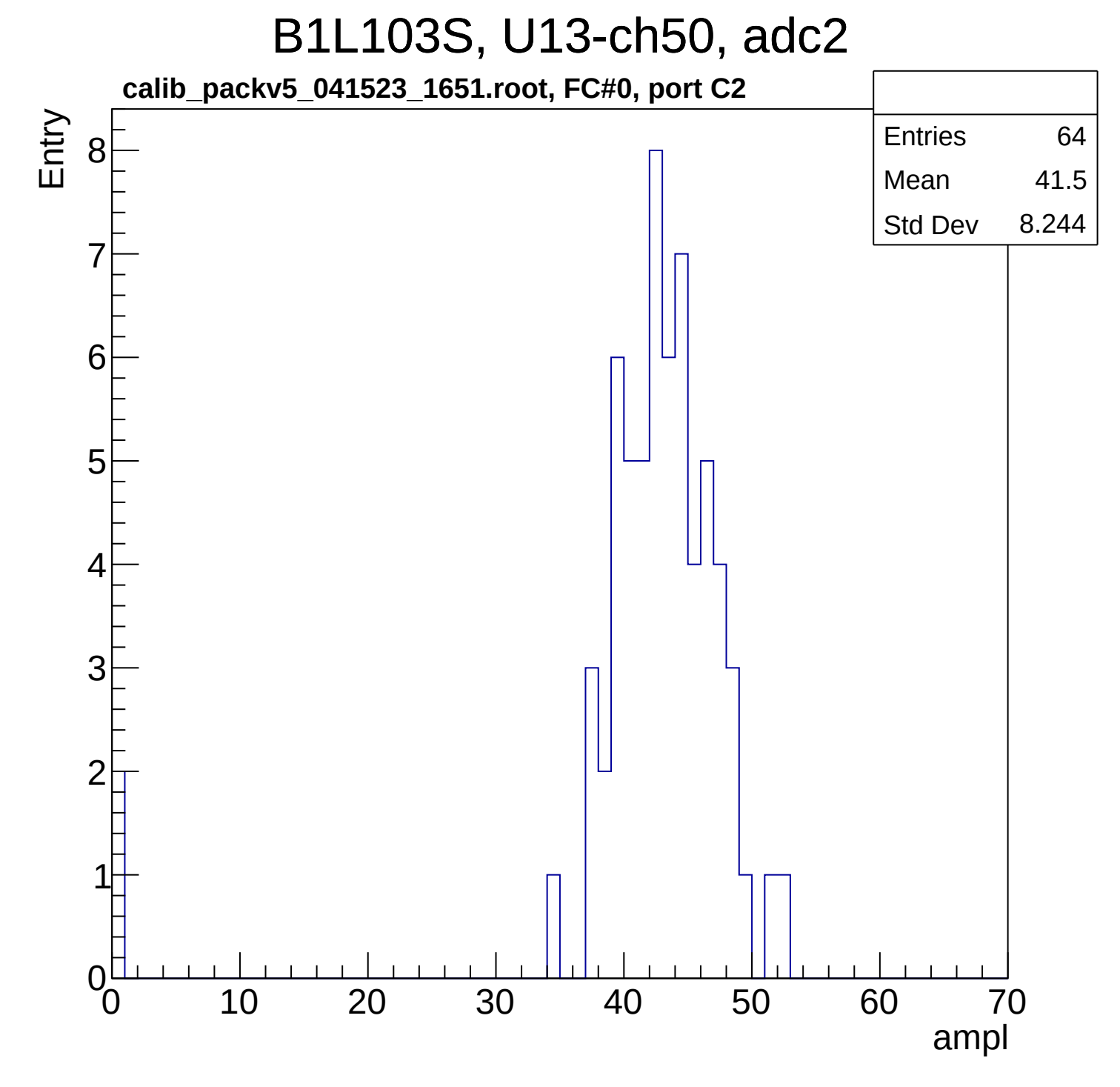
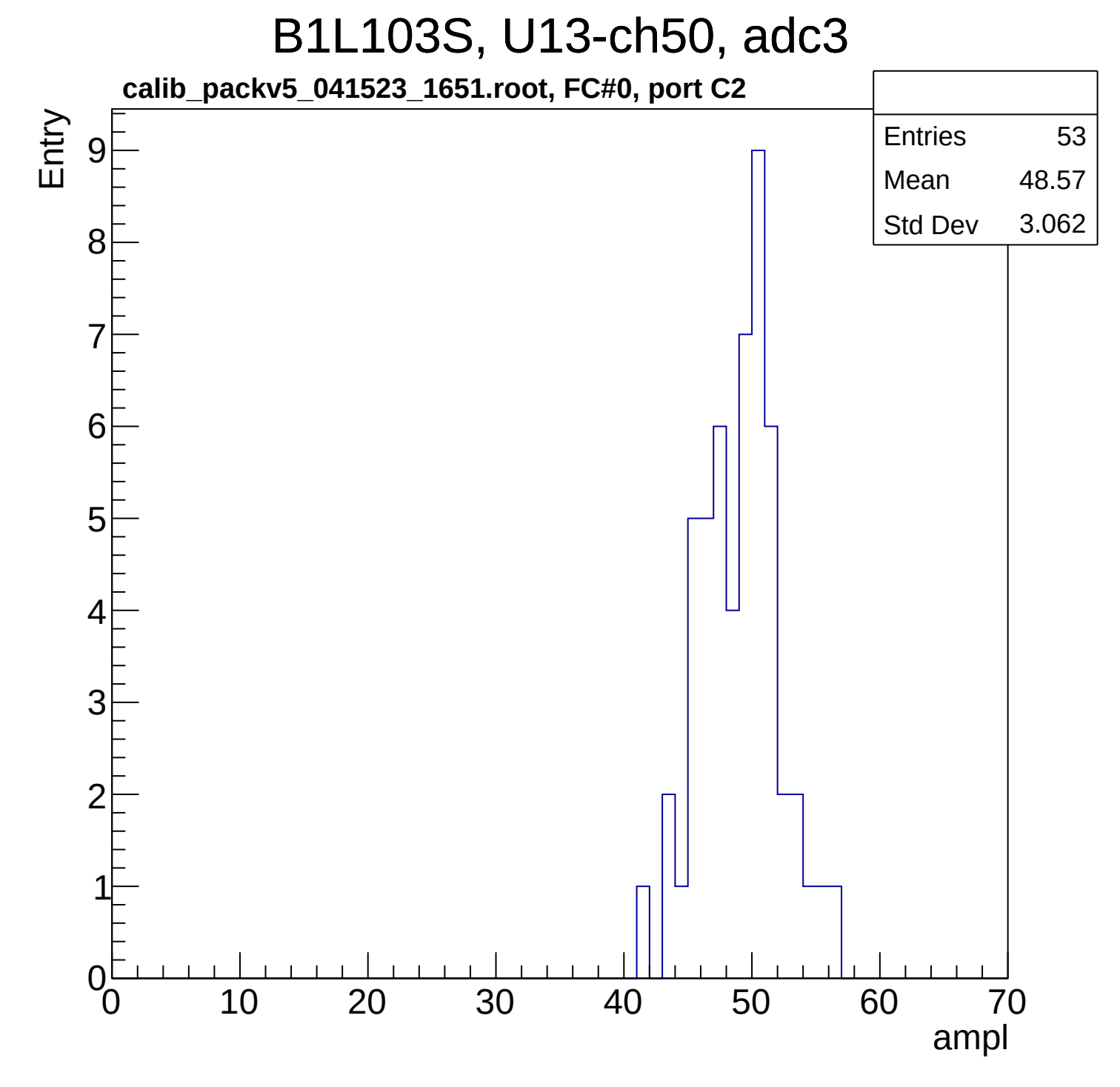
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch50, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 41.5
Std Dev 8.244
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch50, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 48.57
Std Dev 3.062
Entry
ampl
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2
3
4
5
6
7
8
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0
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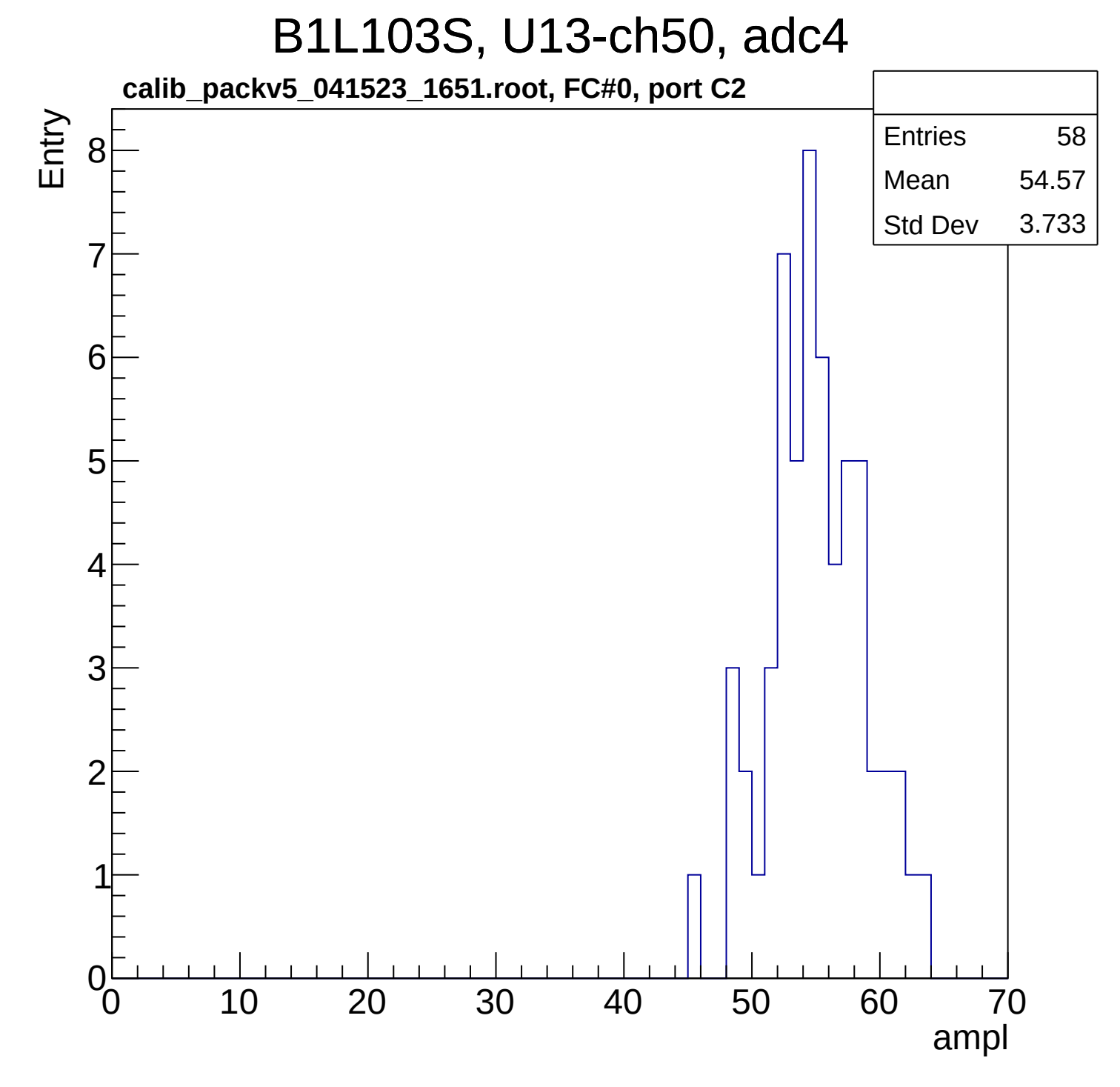
B1L103S, U13-ch50, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 54.57
Std Dev 3.733
Entry
ampl
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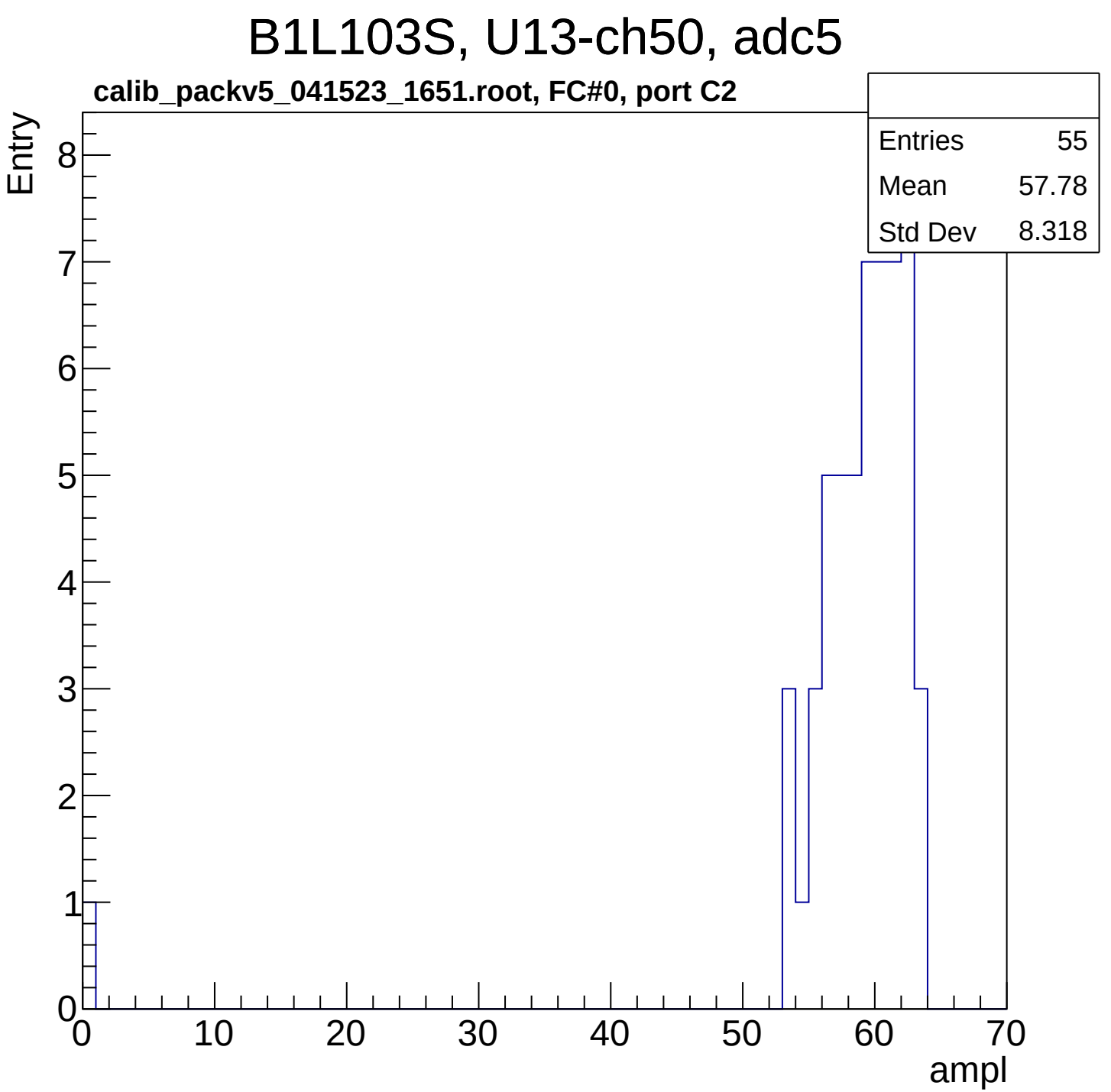
B1L103S, U13-ch50, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.78
Std Dev 8.318
Entry
ampl
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0
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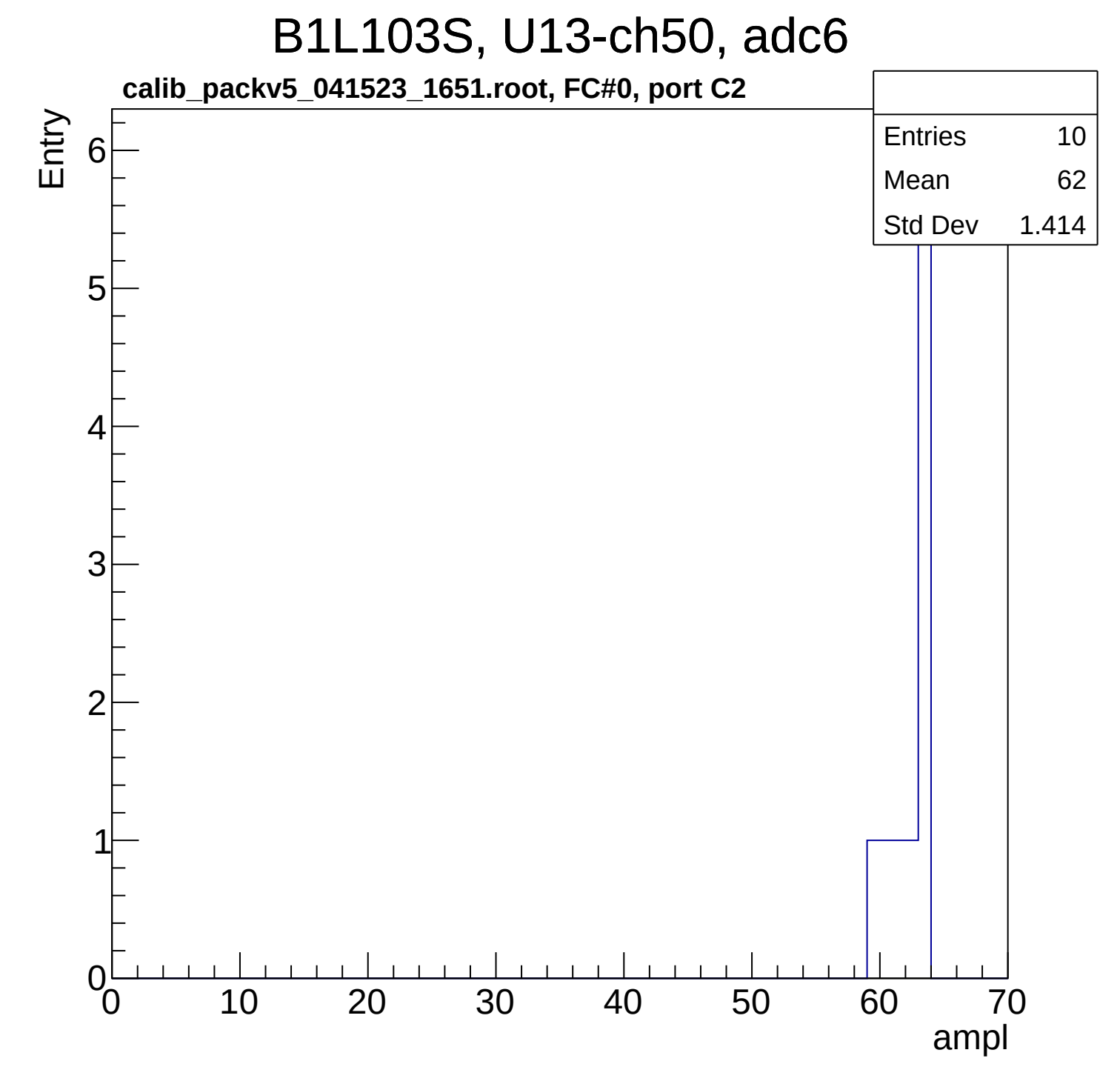
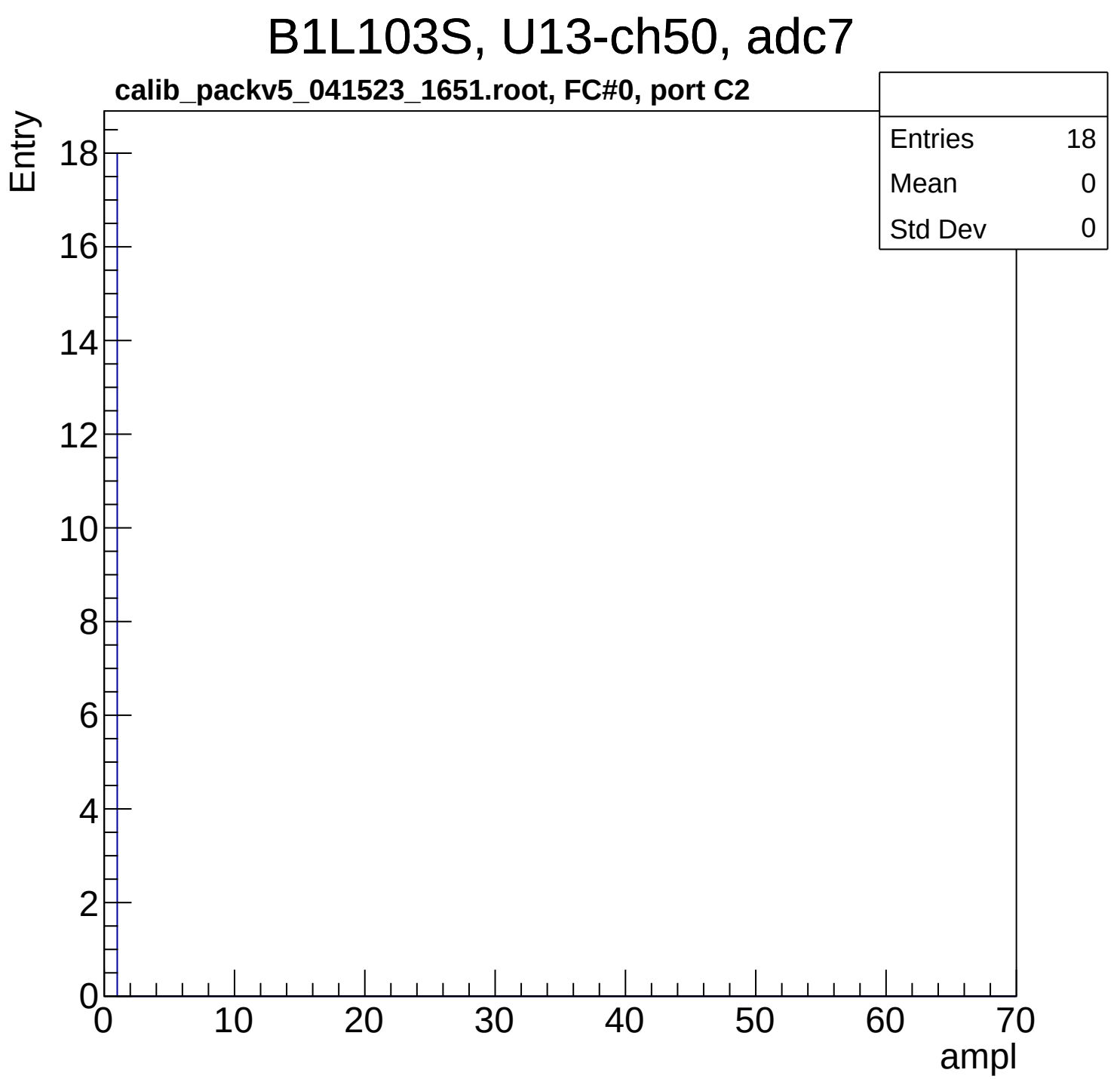

B1L103S, U13-ch50, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 62
Std Dev 1.414
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch50, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
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50
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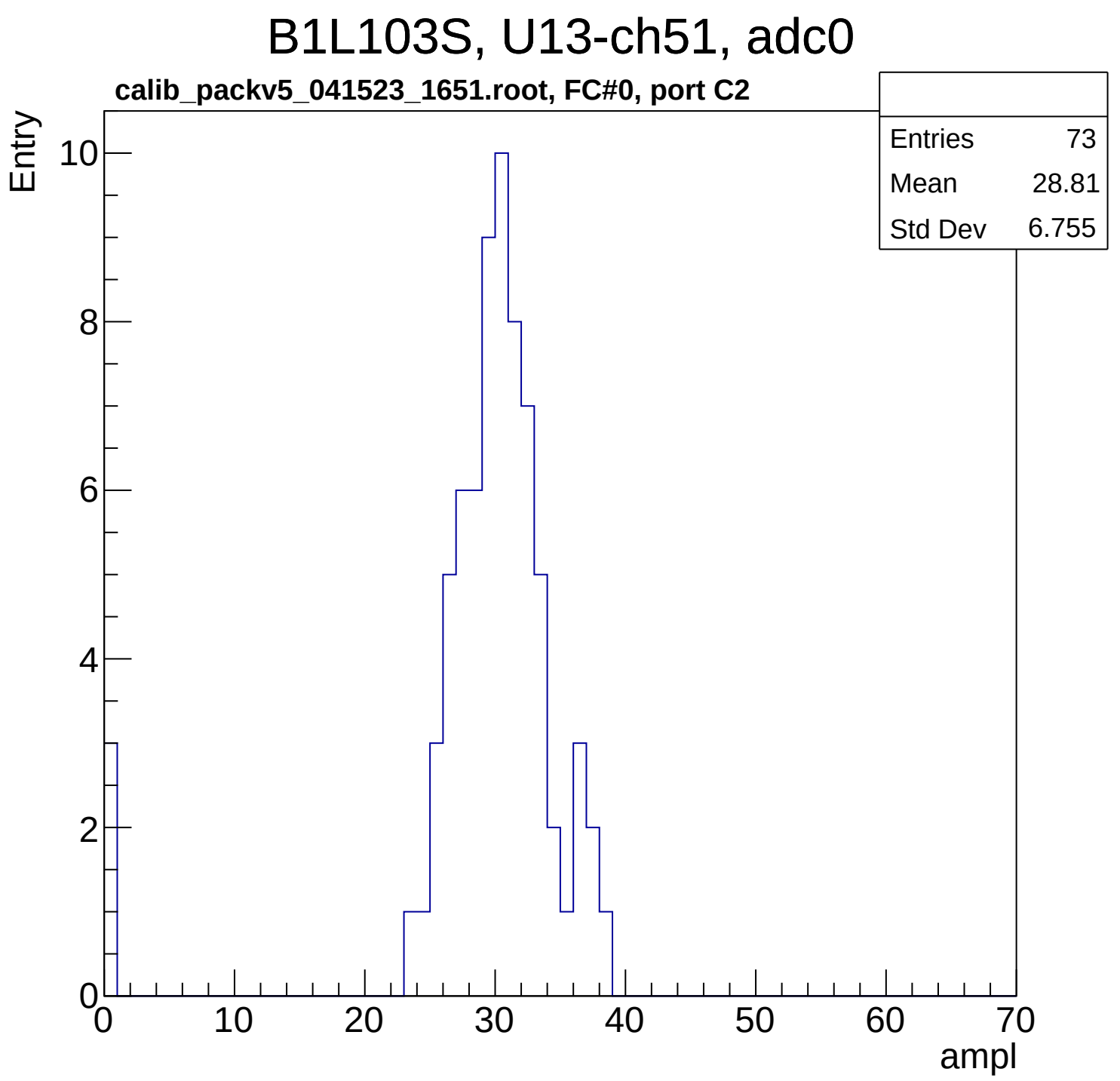
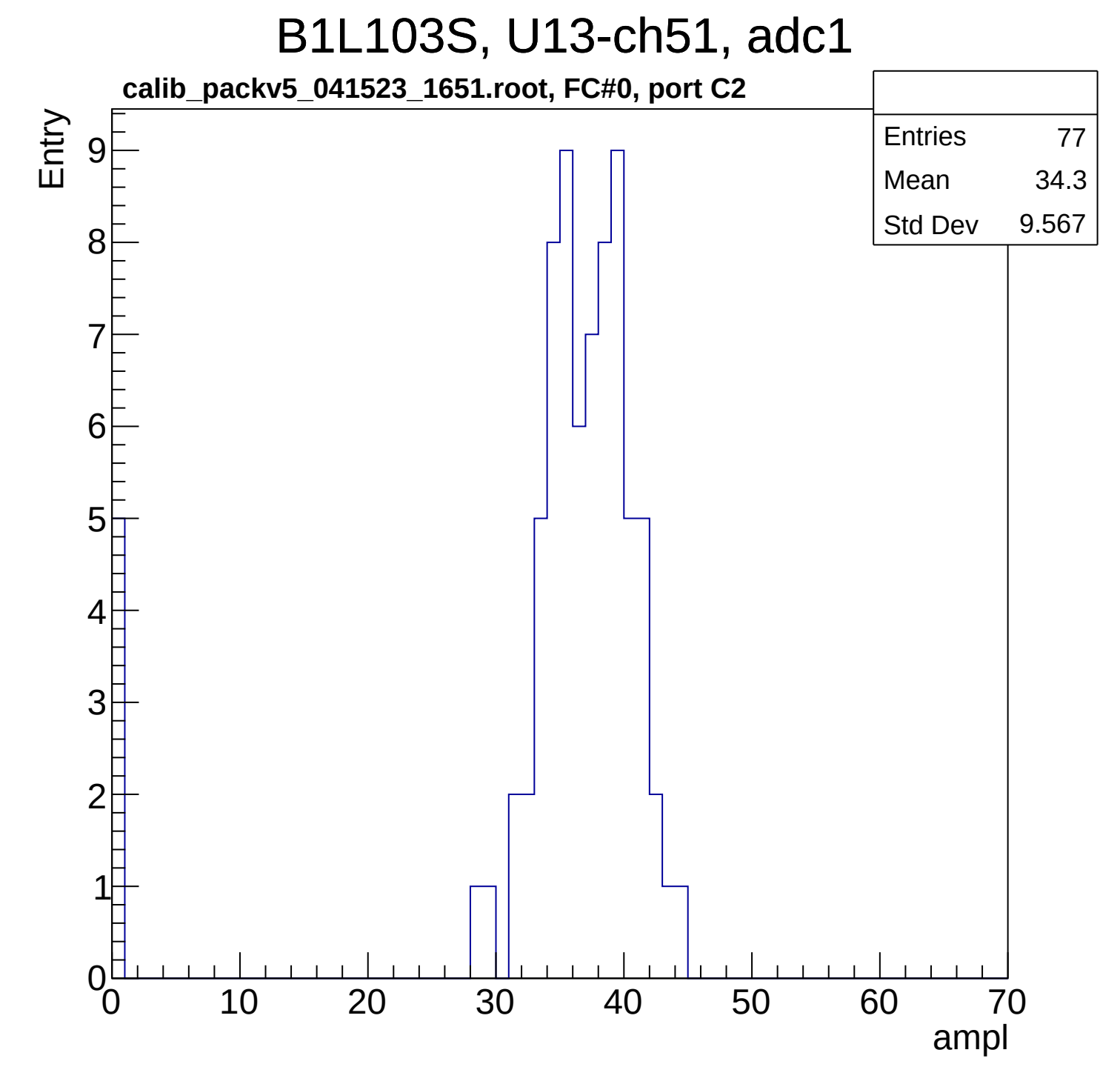
70
ampl


B1L103S, U13-ch51, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 28.81
Std Dev 6.755
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch51, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 34.3
Std Dev 9.567
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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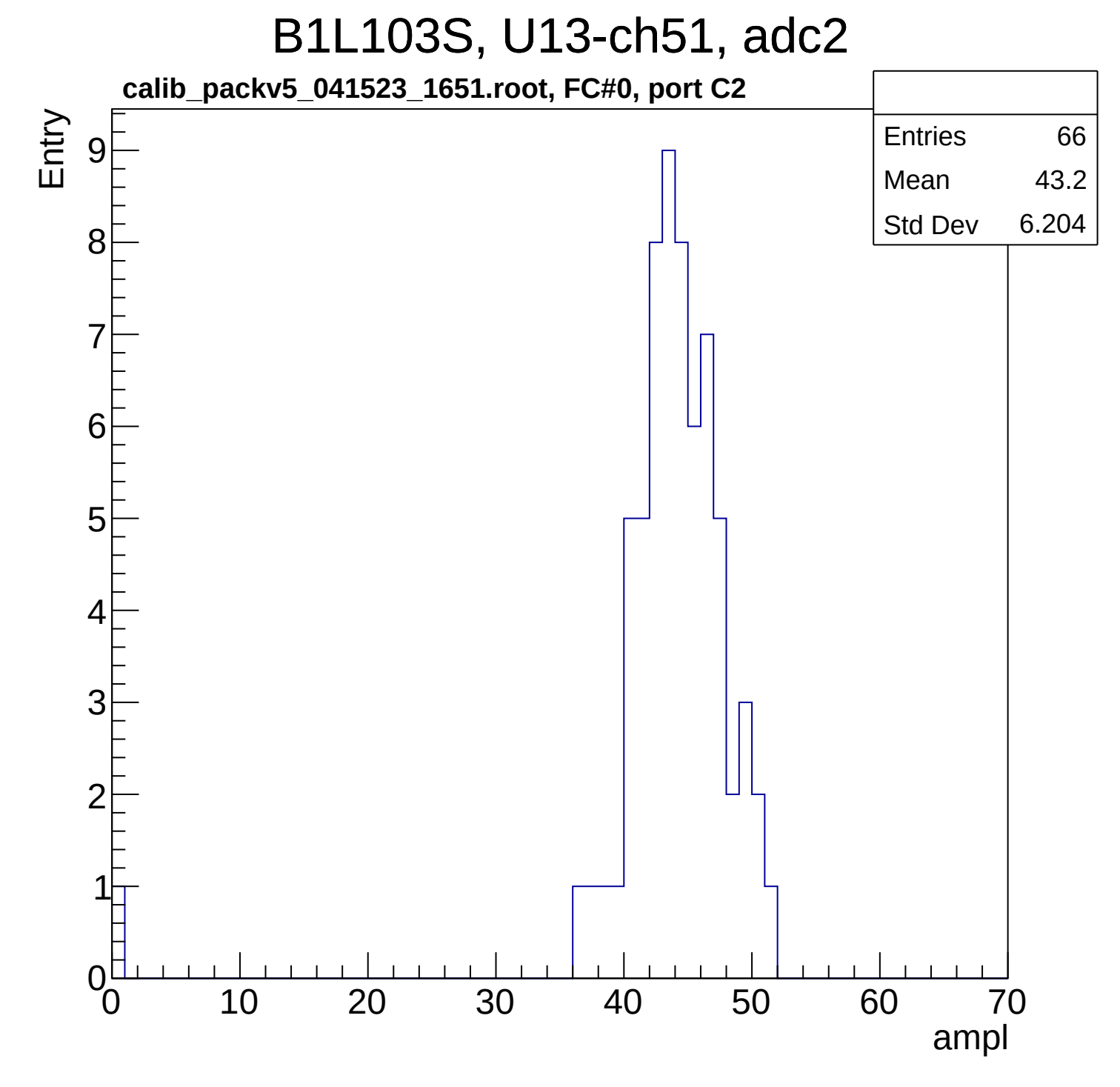
B1L103S, U13-ch51, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 43.2
Std Dev 6.204
Entry
ampl
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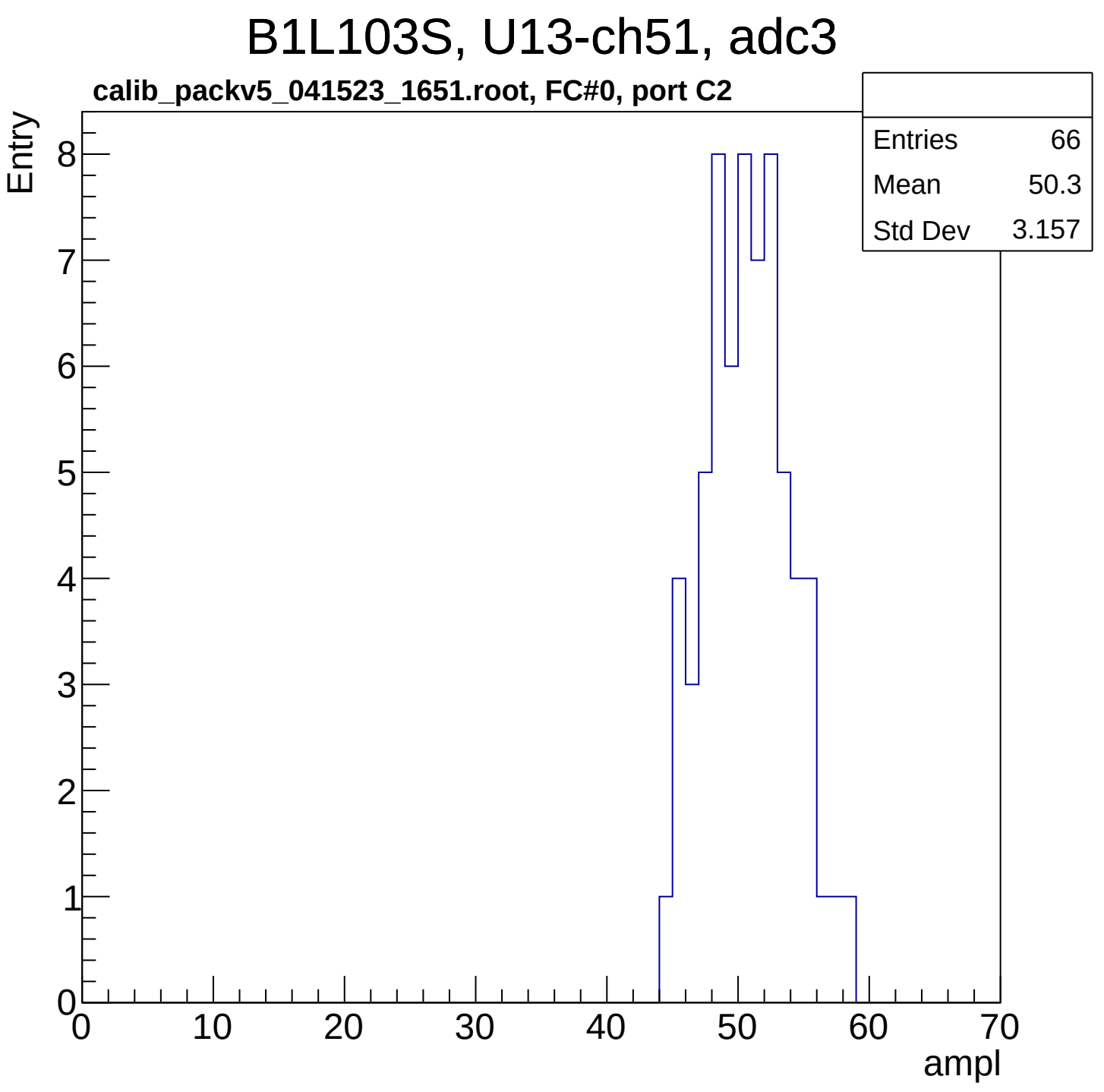
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch51, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 50.3
Std Dev 3.157
Entry
ampl
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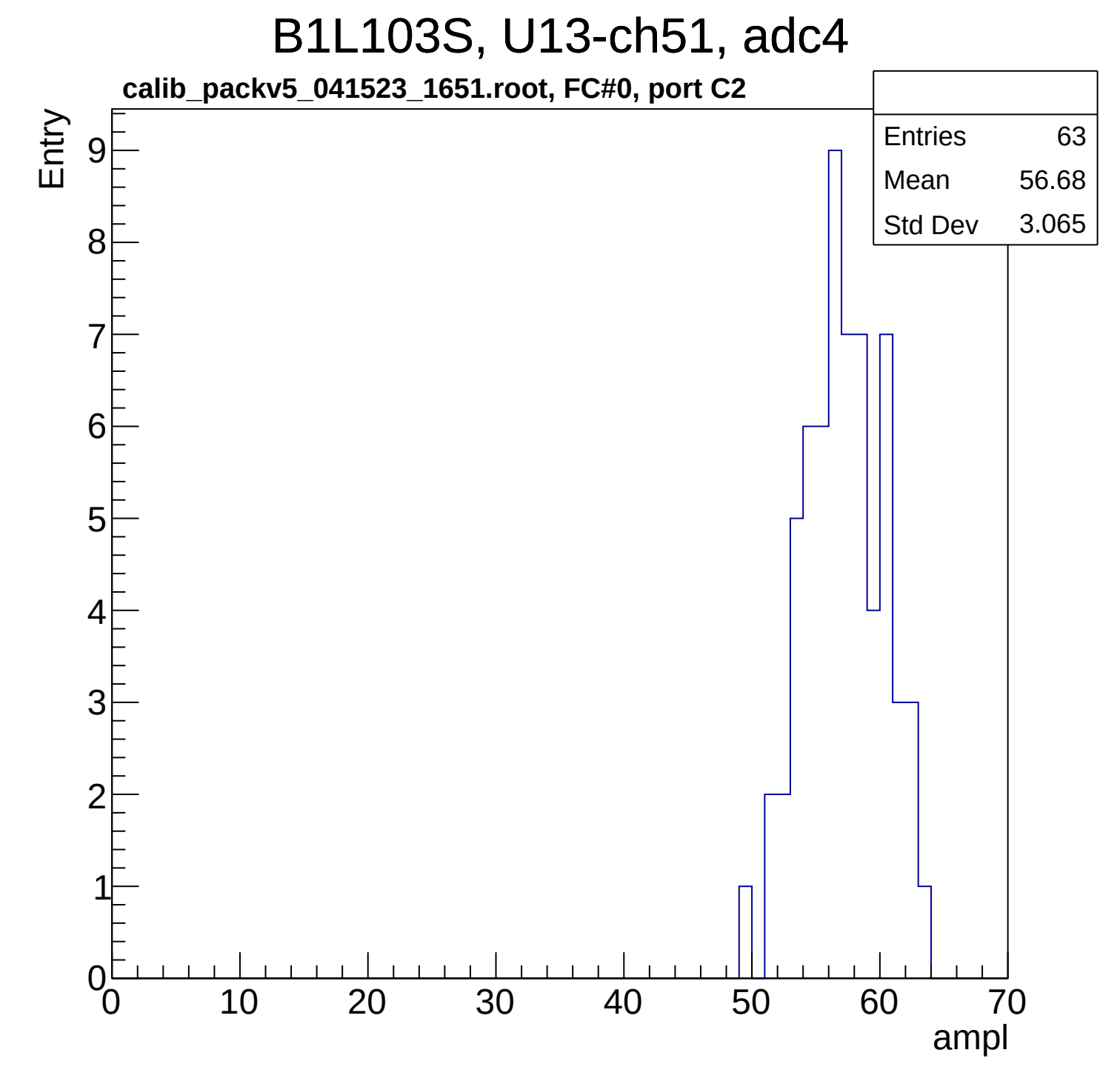
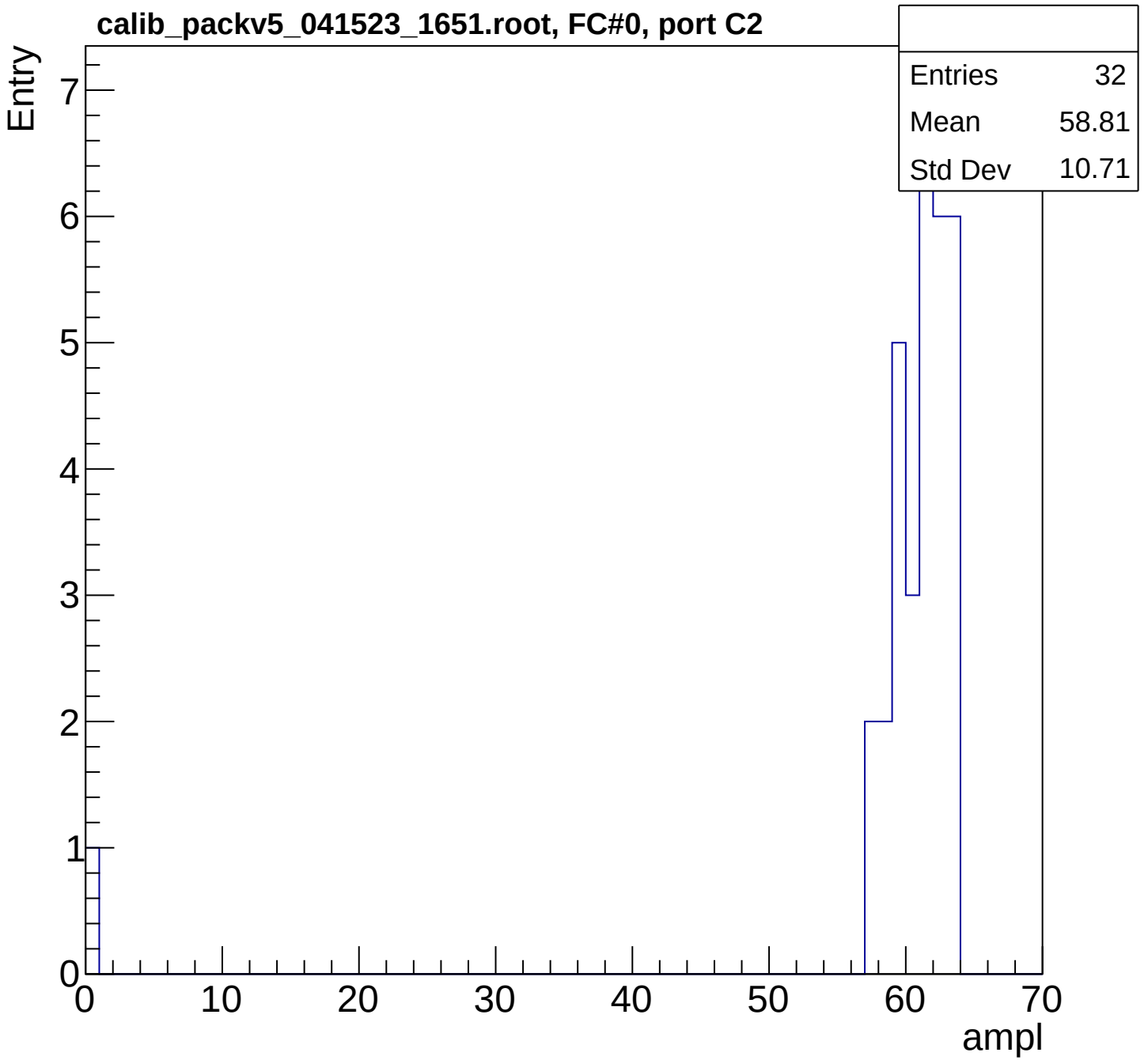
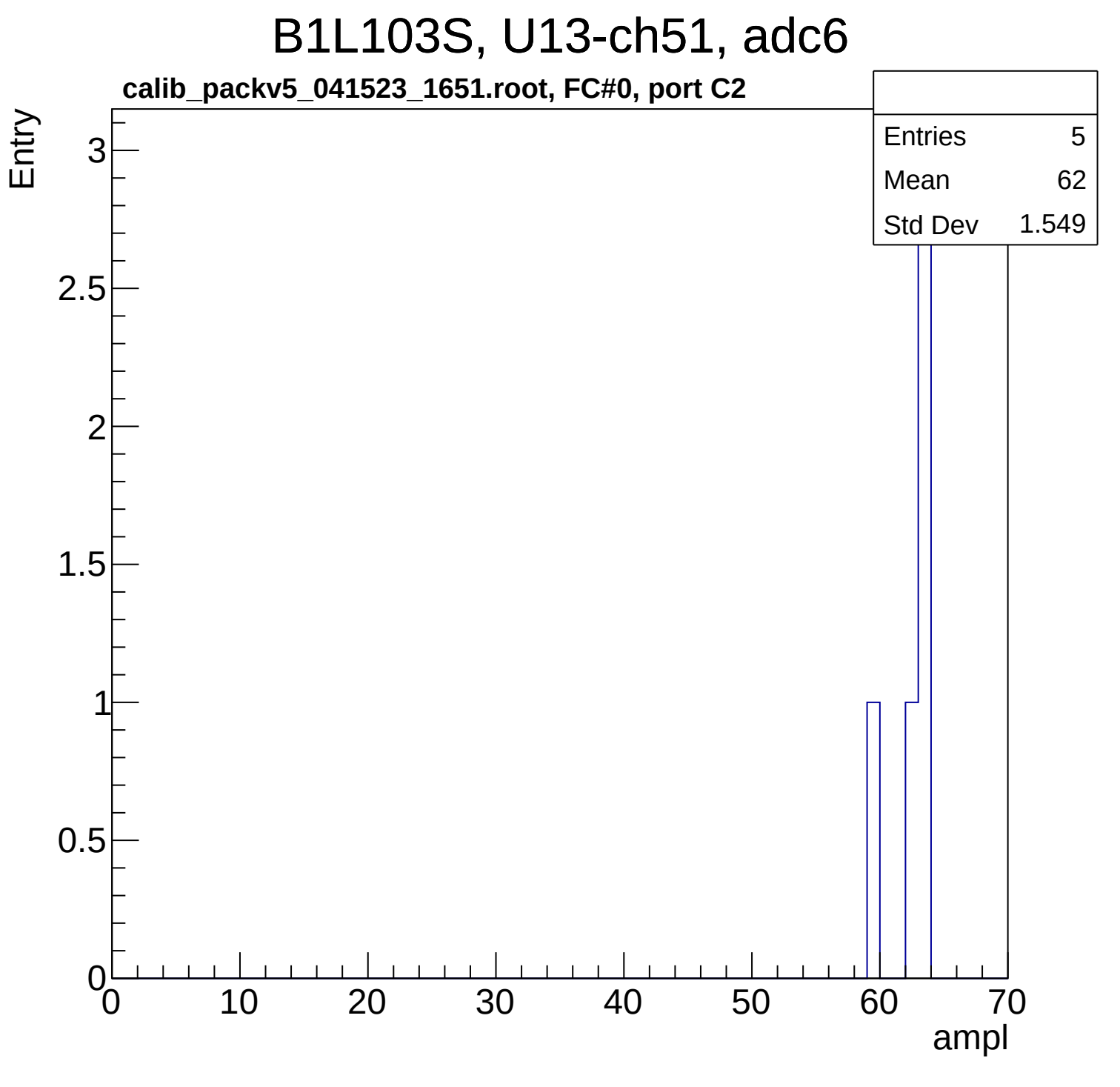
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch51, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 56.68
Std Dev 3.065
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch51, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 58.81
Std Dev 10.71
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch51, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62
Std Dev 1.549
Entry
ampl
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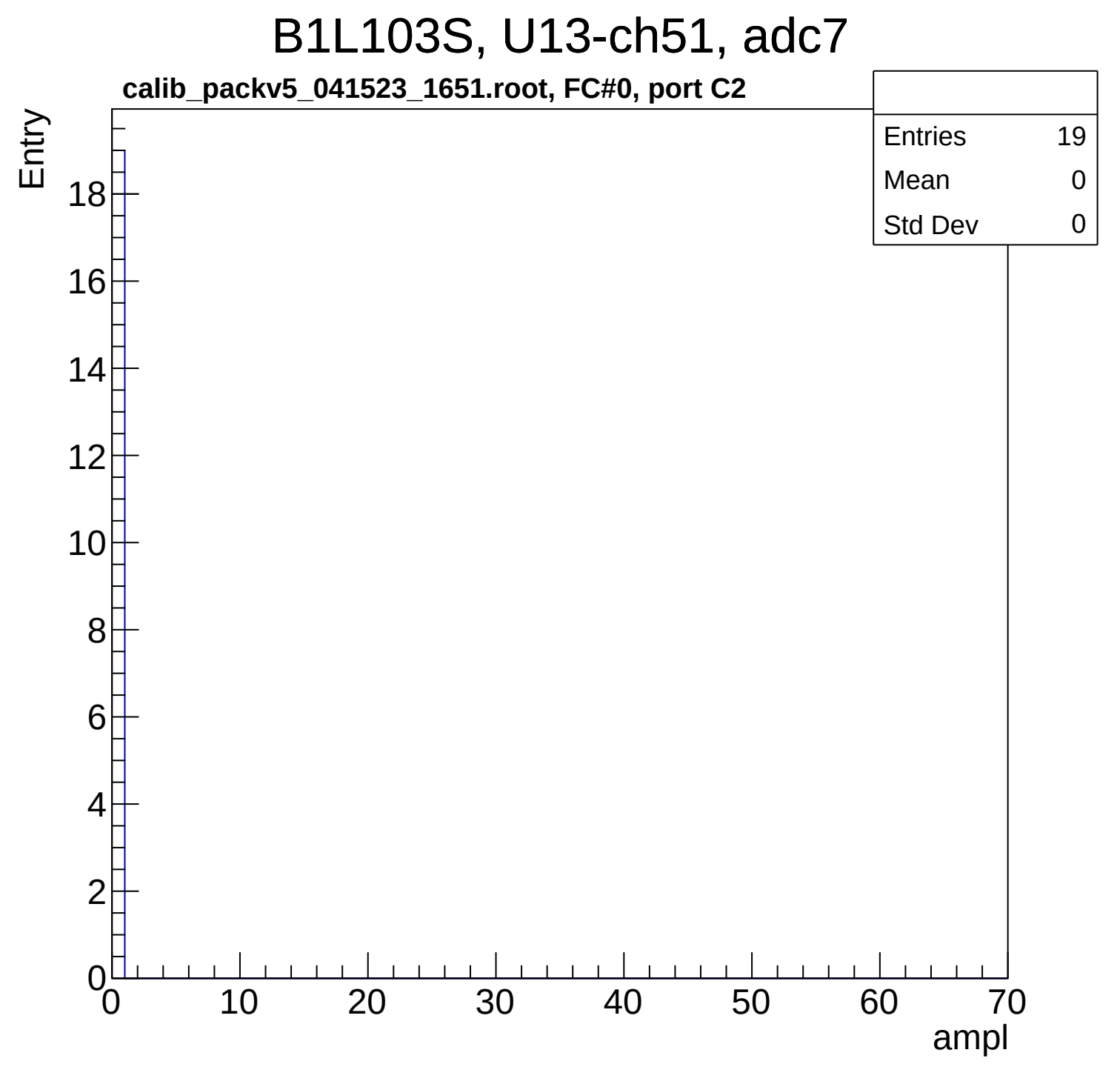
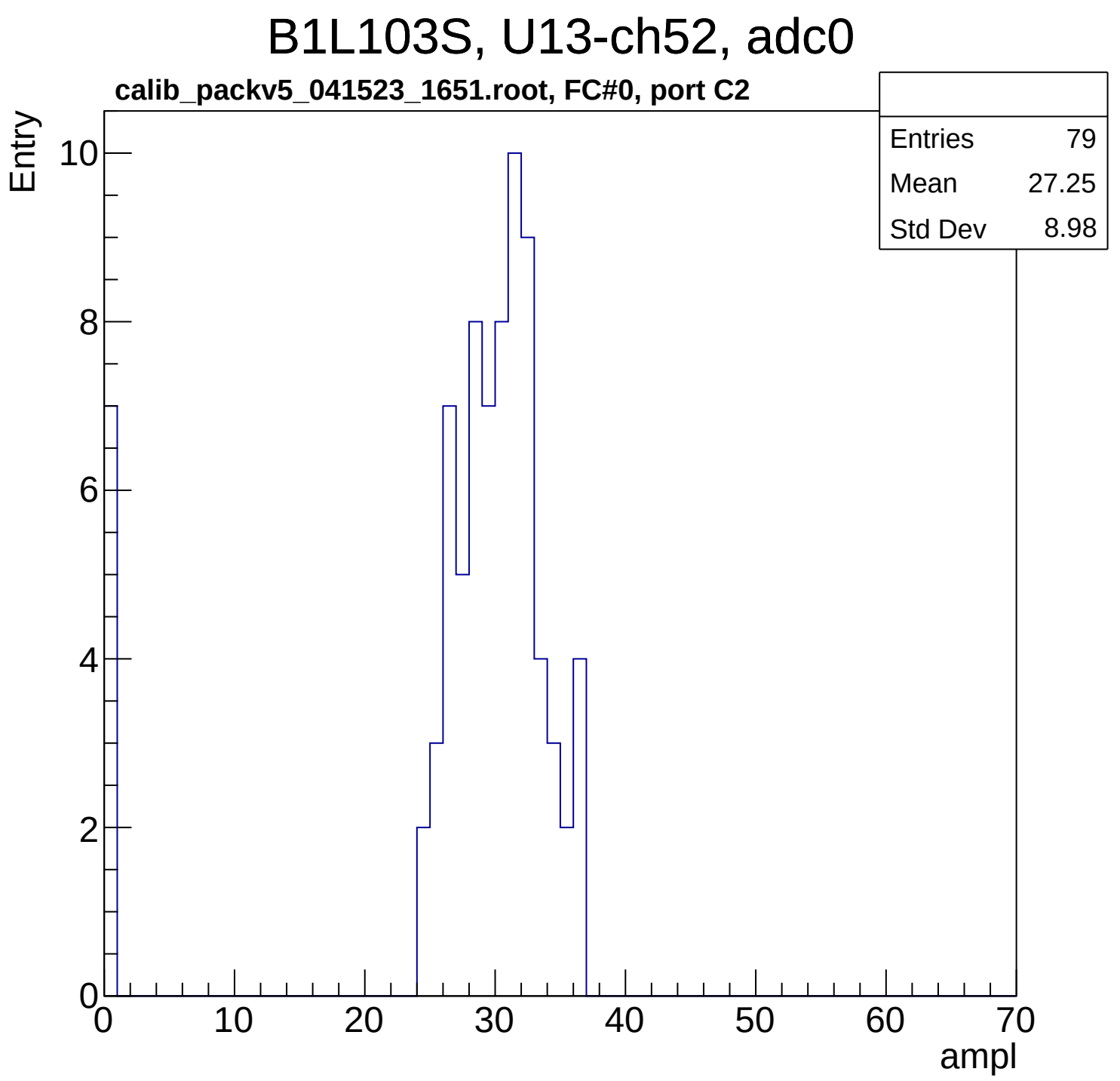
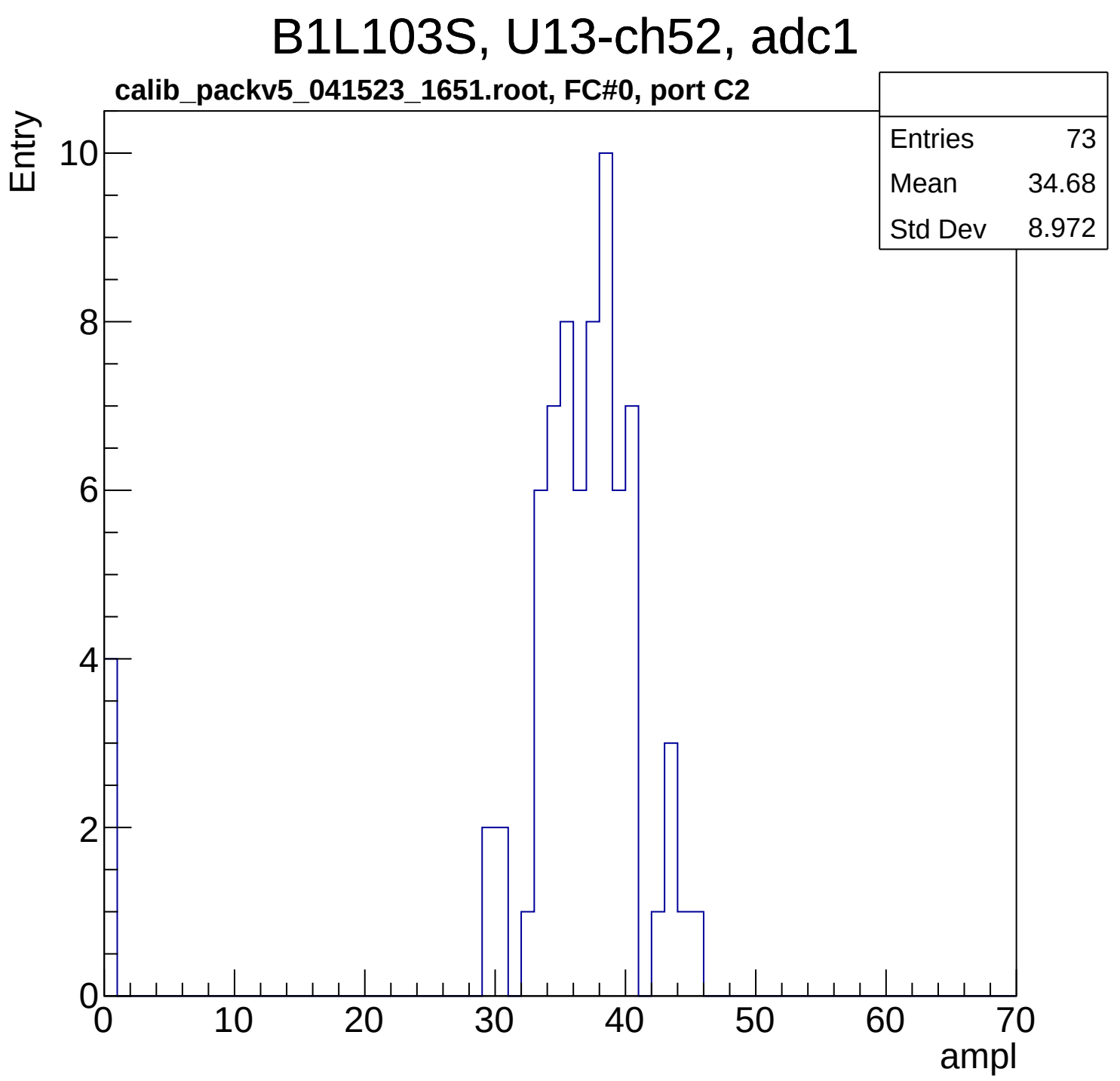
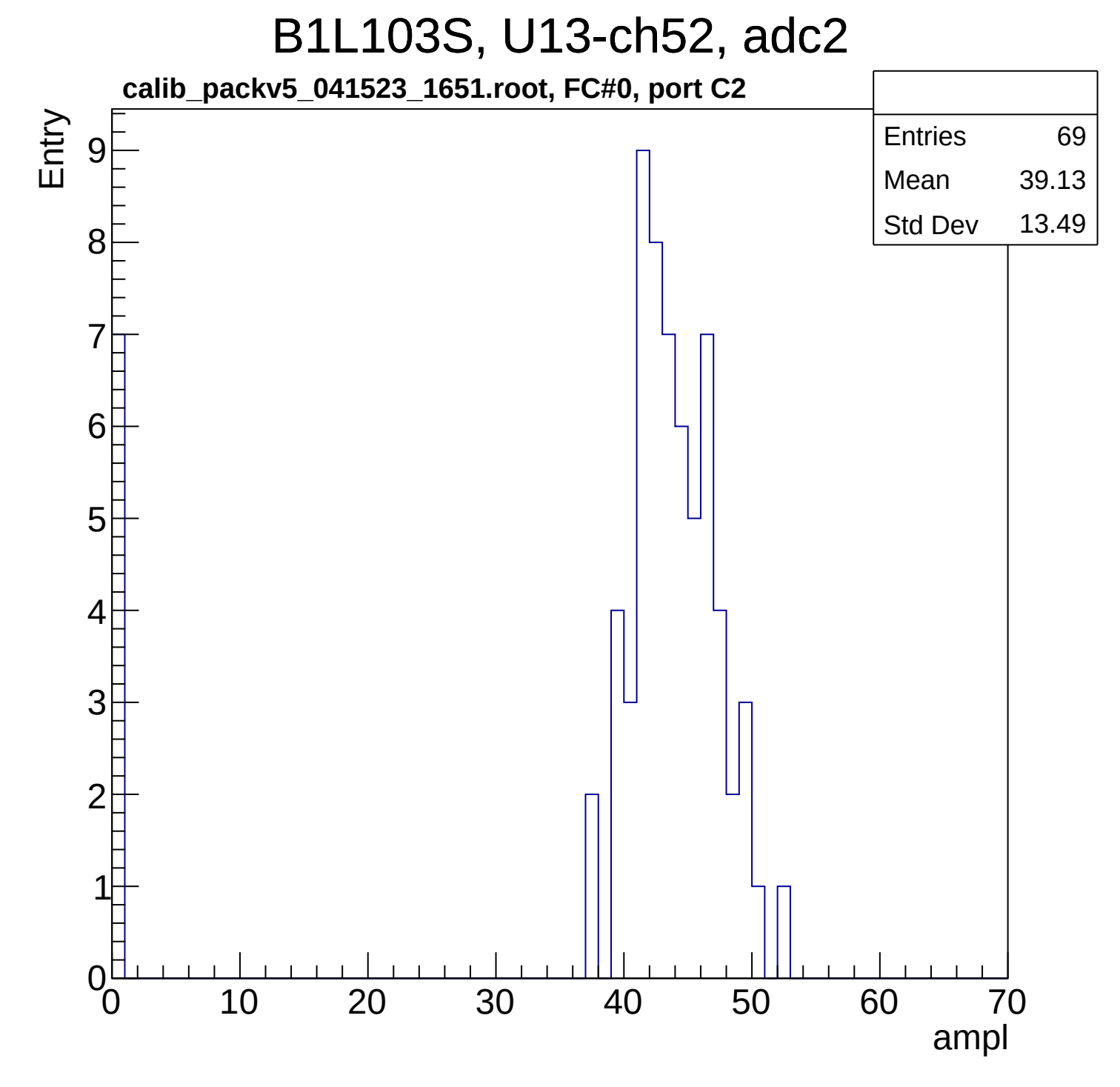
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U13-ch51, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch52, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 27.25
Std Dev 8.98
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch52, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 34.68
Std Dev 8.972
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch52, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 39.13
Std Dev 13.49
Entry
ampl
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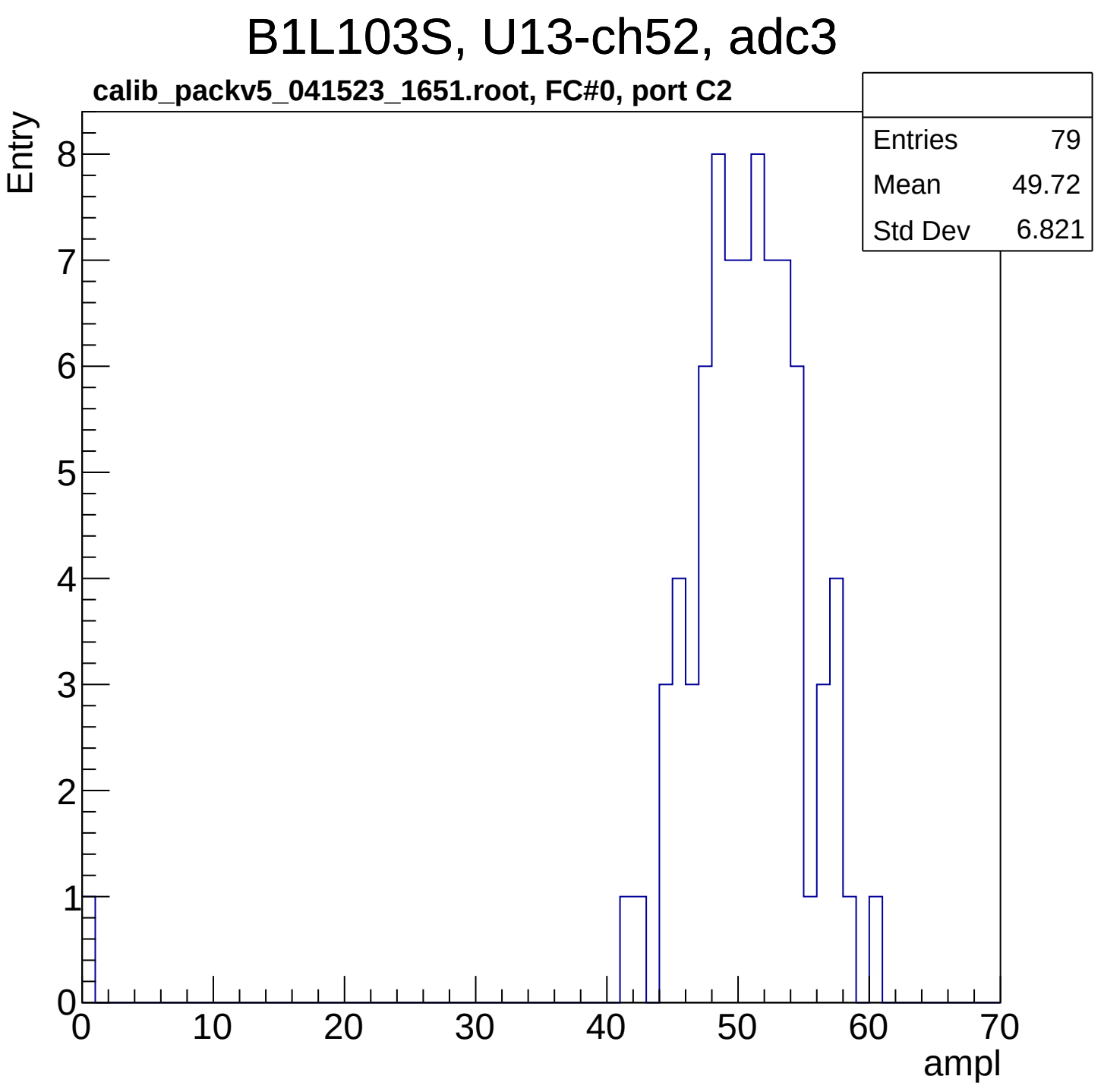
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch52, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 49.72
Std Dev 6.821
Entry
ampl
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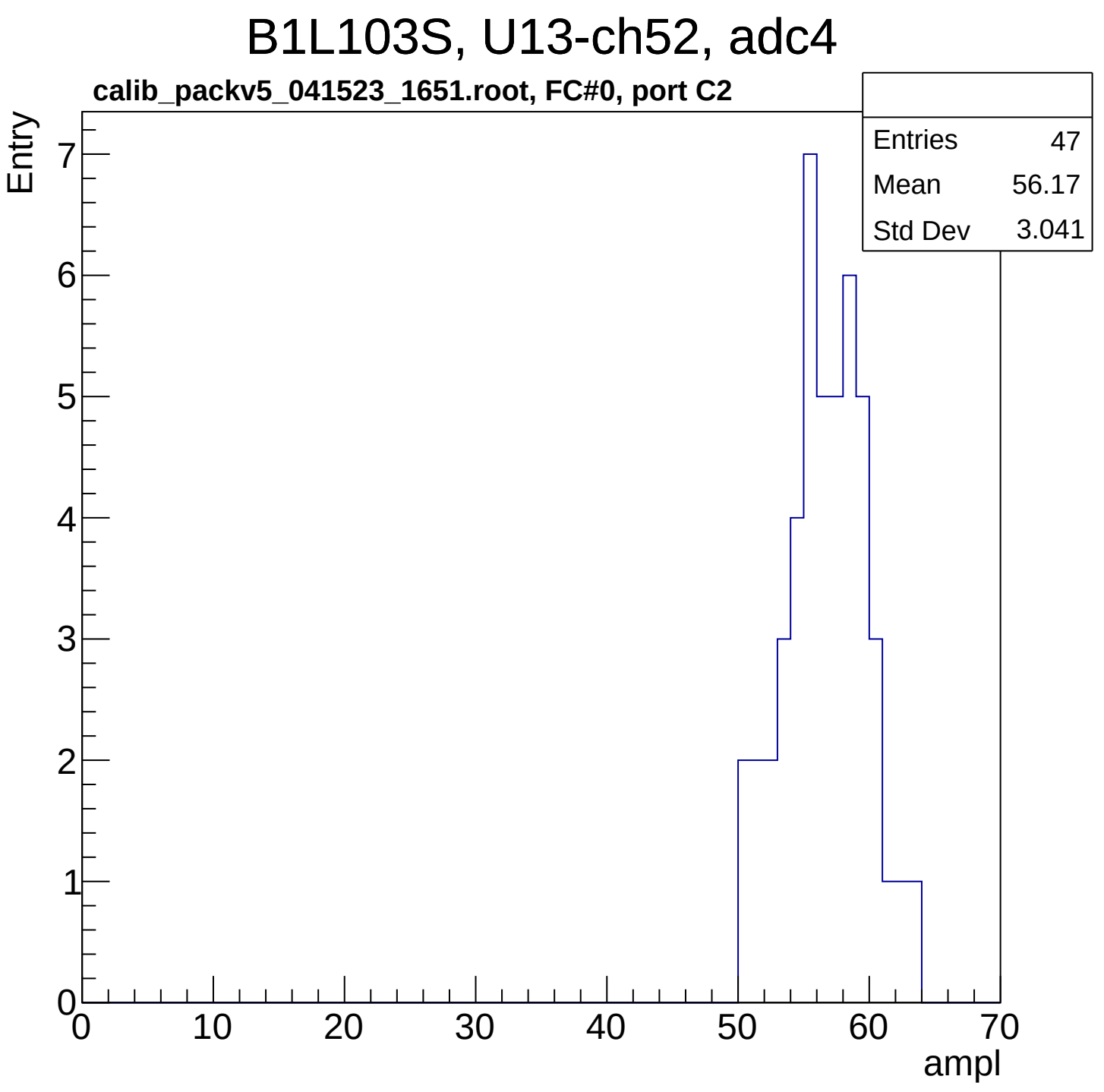
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch52, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 56.17
Std Dev 3.041
Entry
ampl
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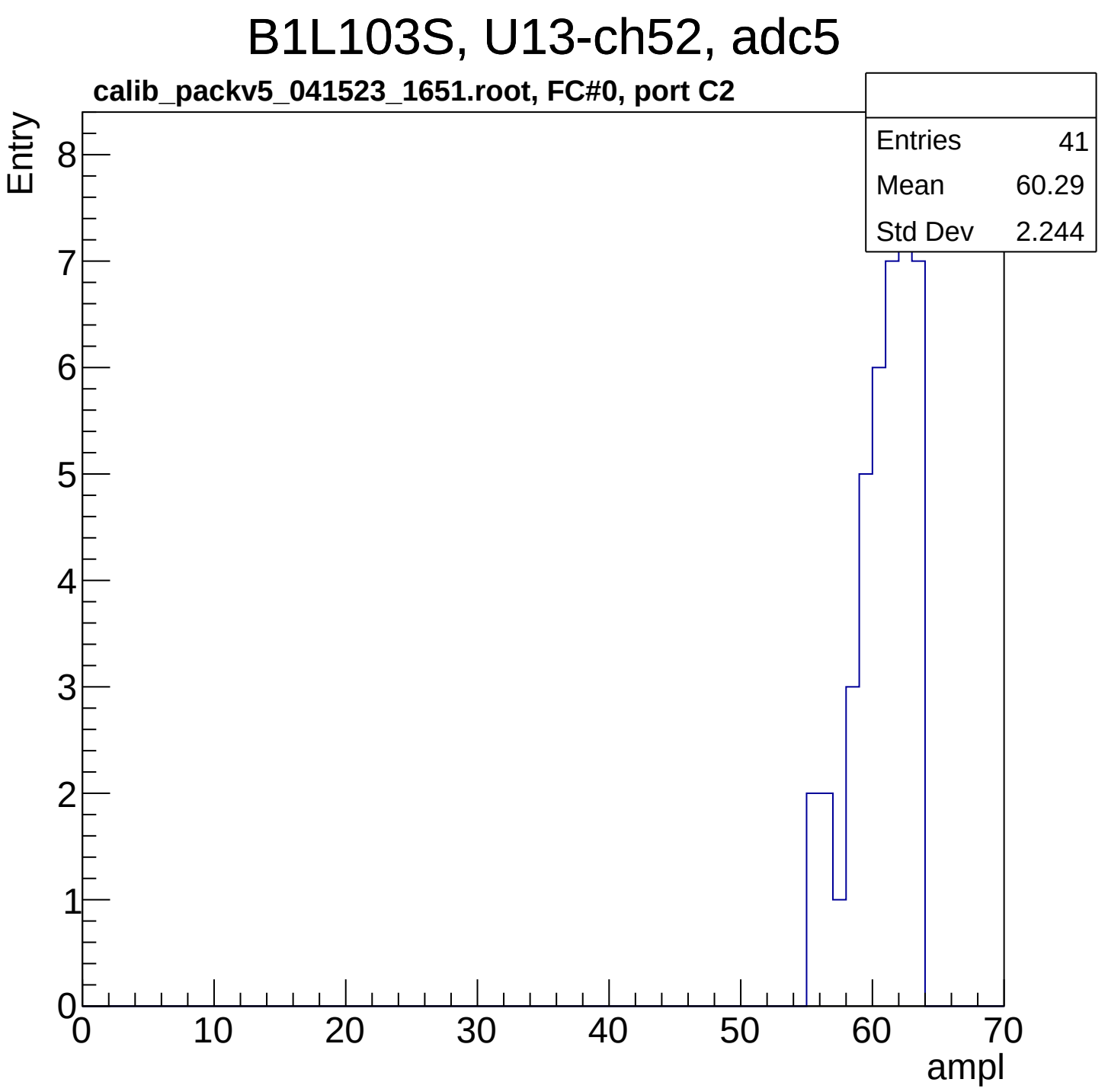
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch52, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 60.29
Std Dev 2.244
Entry
ampl
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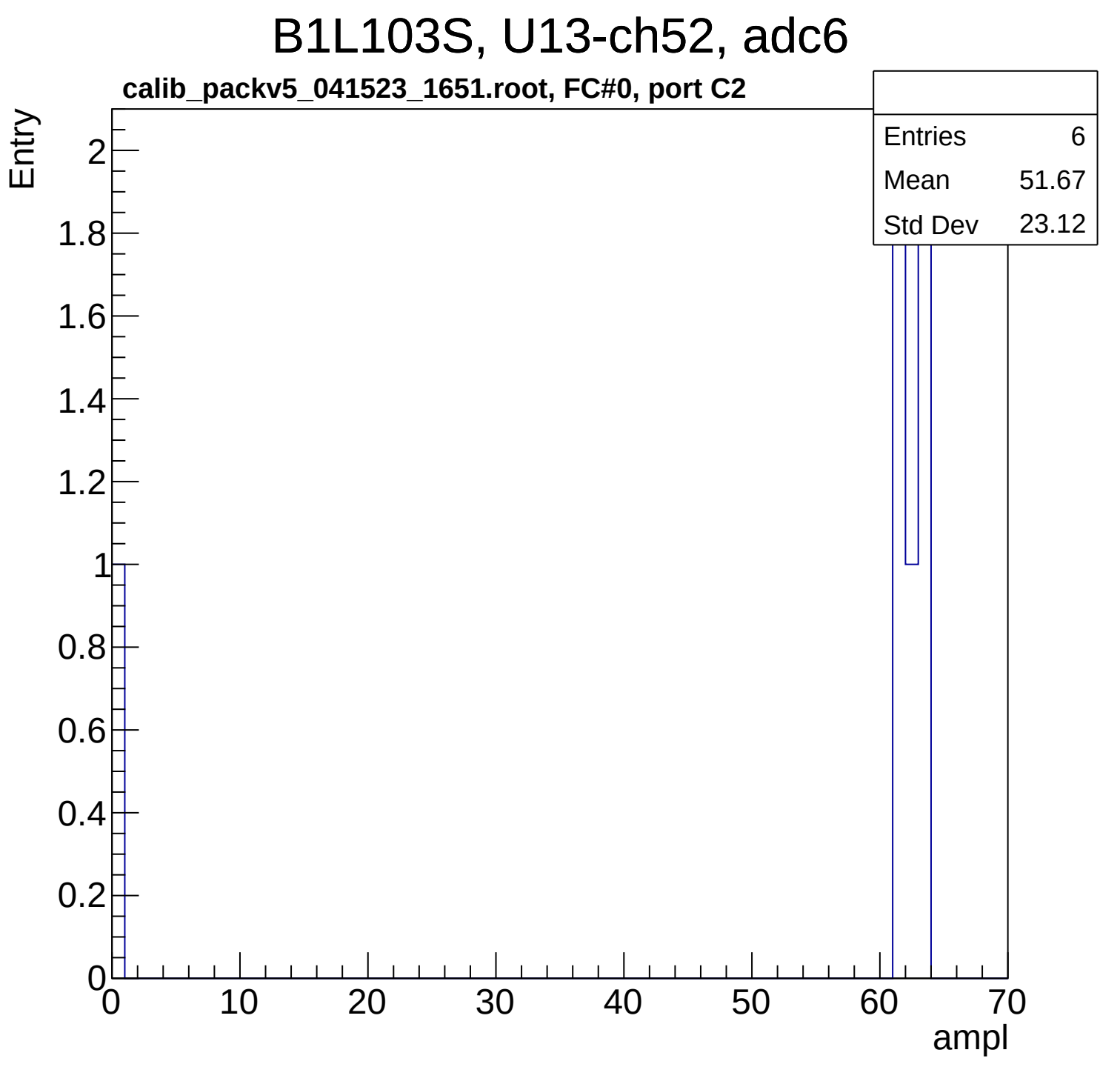
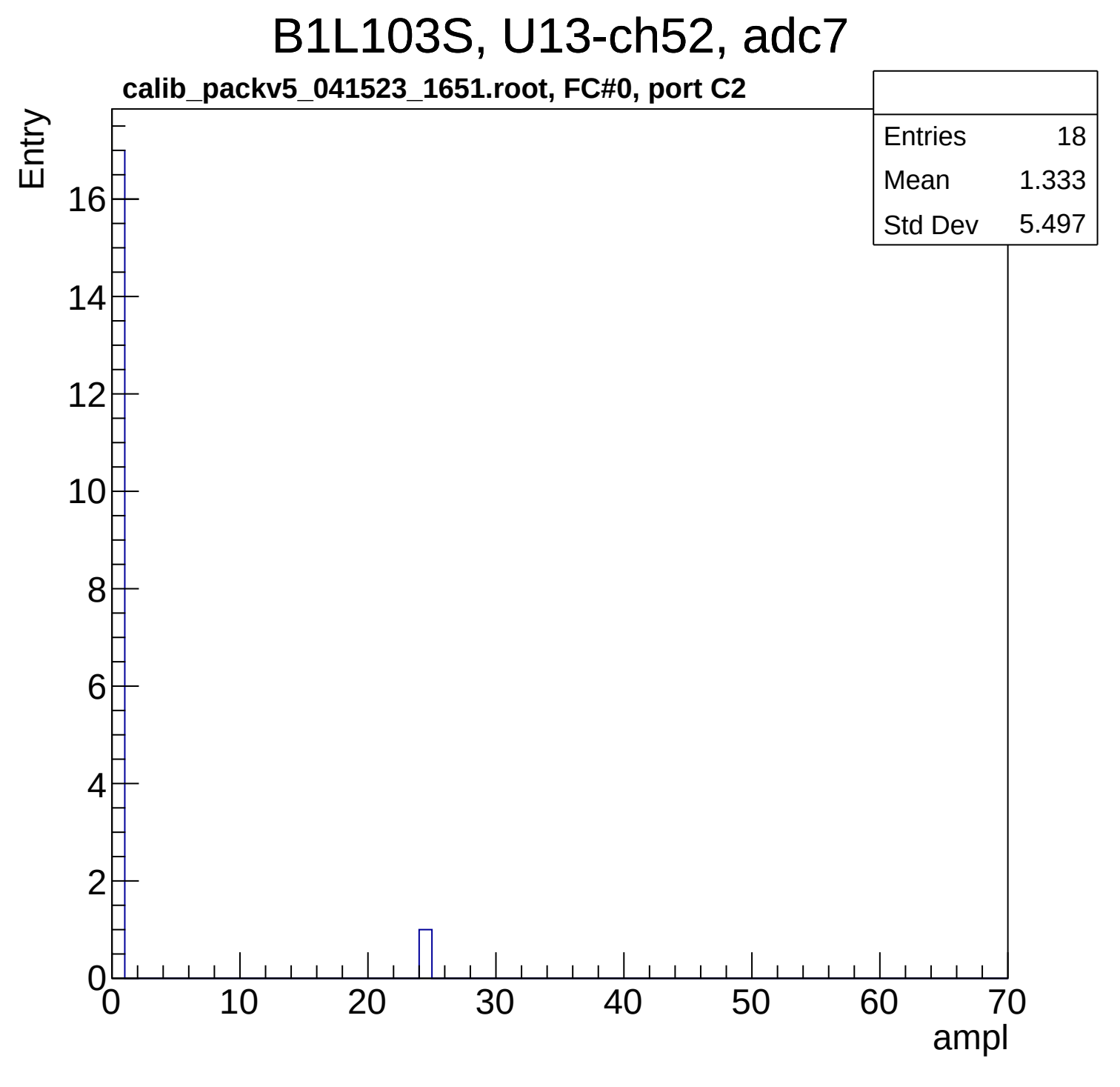
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch52, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 51.67
Std Dev 23.12
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U13-ch52, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.333
Std Dev 5.497
Entry
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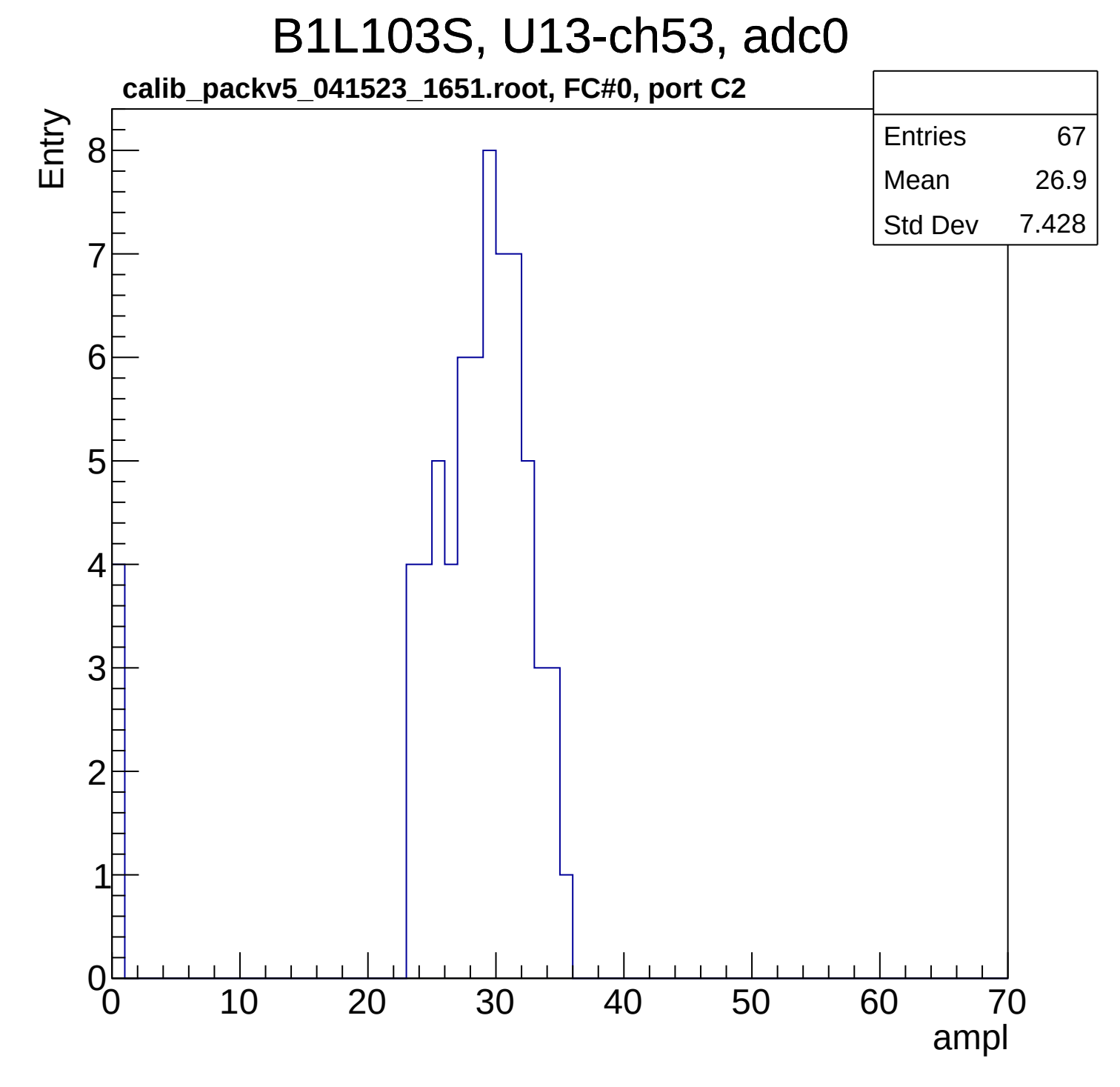
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch53, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 26.9
Std Dev 7.428
Entry
ampl
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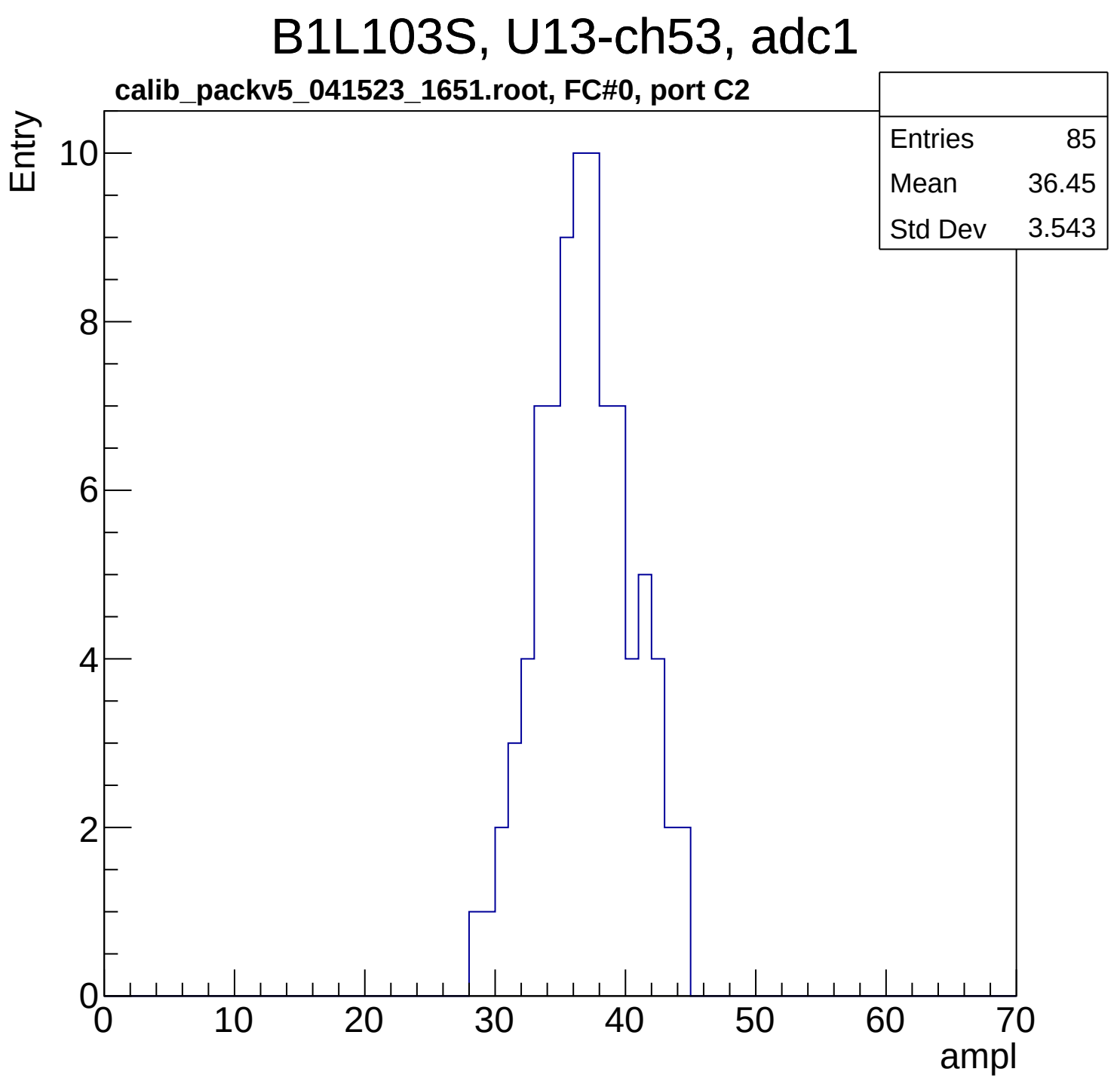
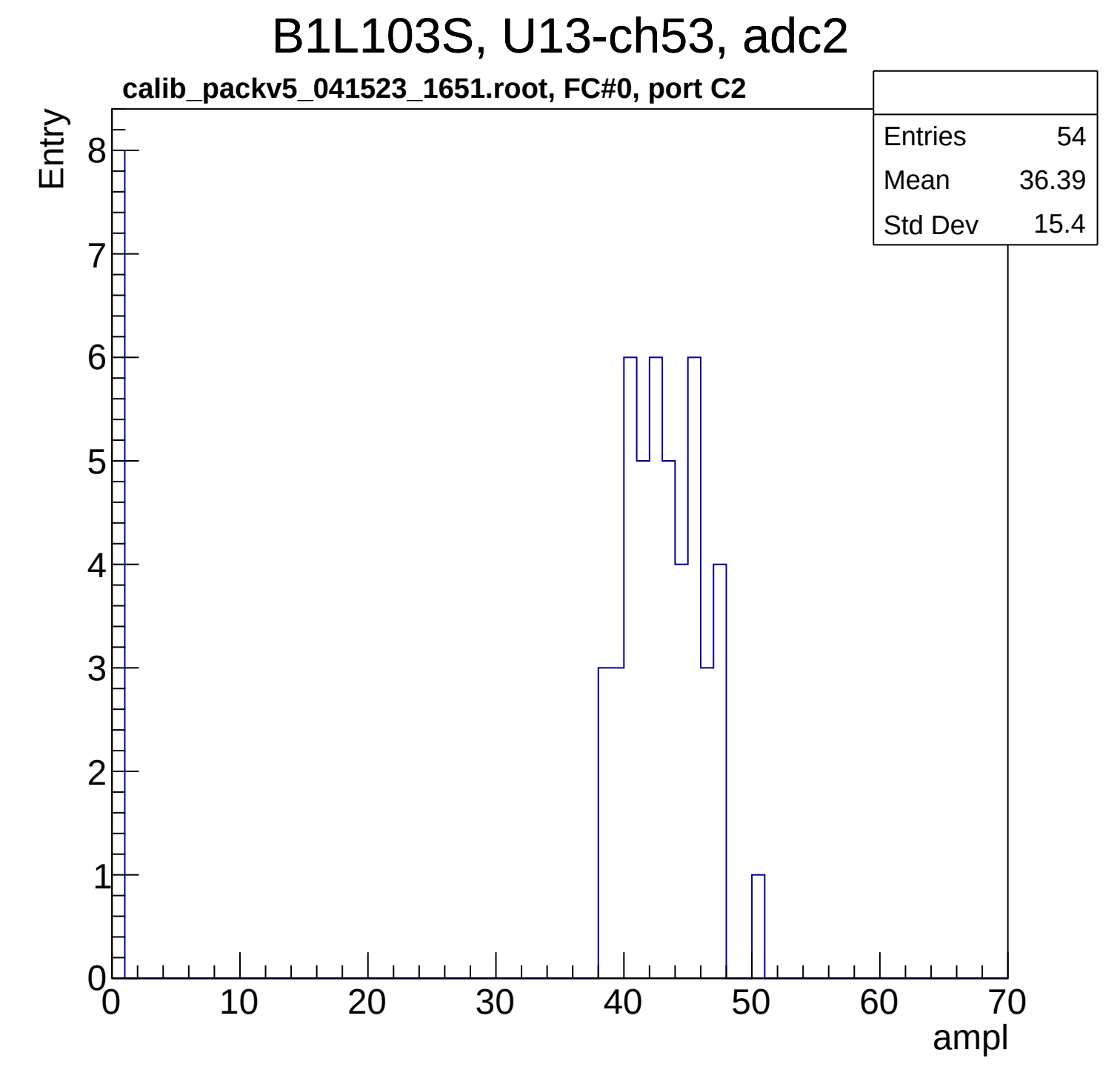
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch53, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 36.45
Std Dev 3.543
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch53, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 36.39
Std Dev 15.4
Entry
ampl
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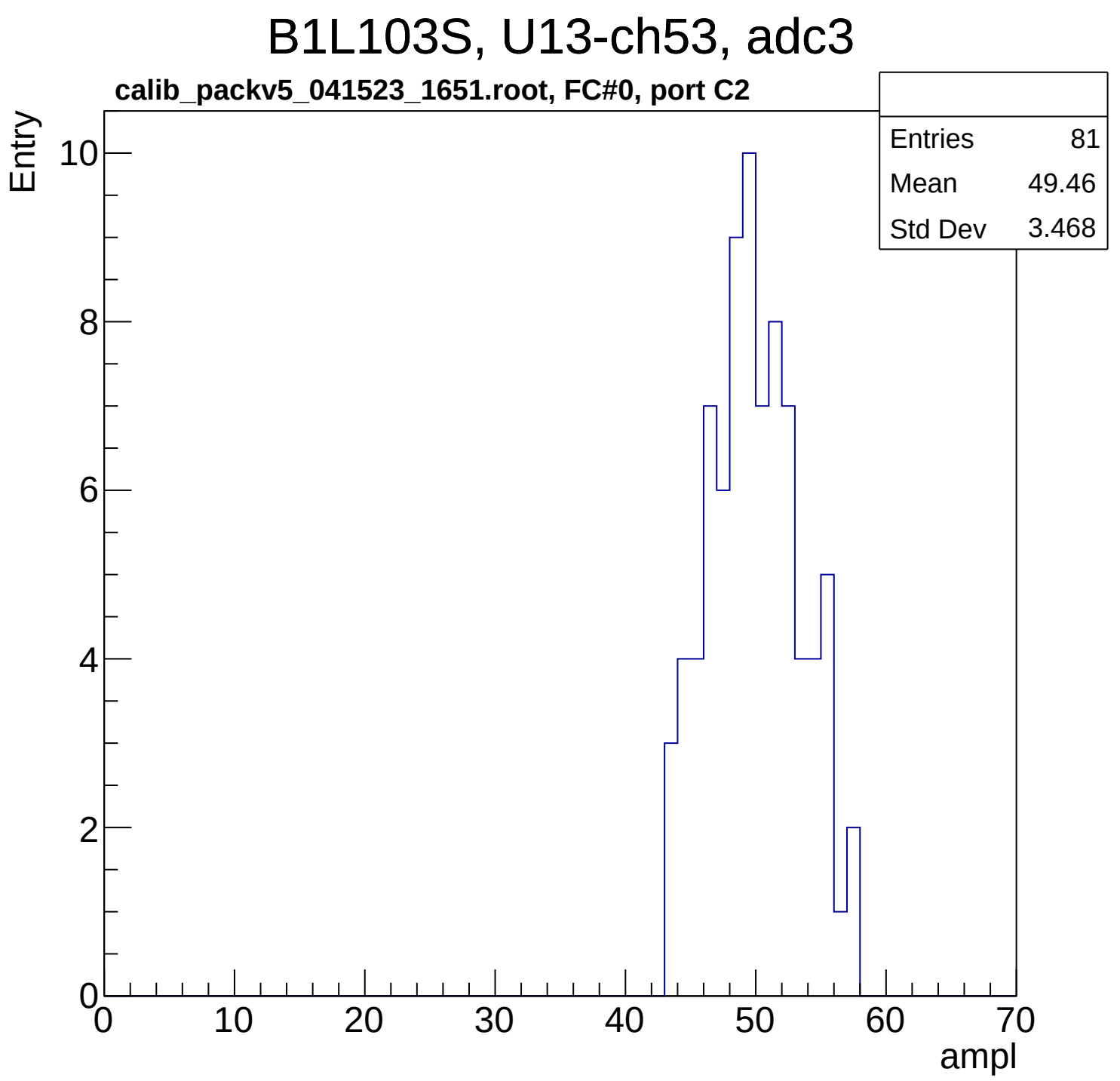
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch53, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 49.46
Std Dev 3.468
Entry
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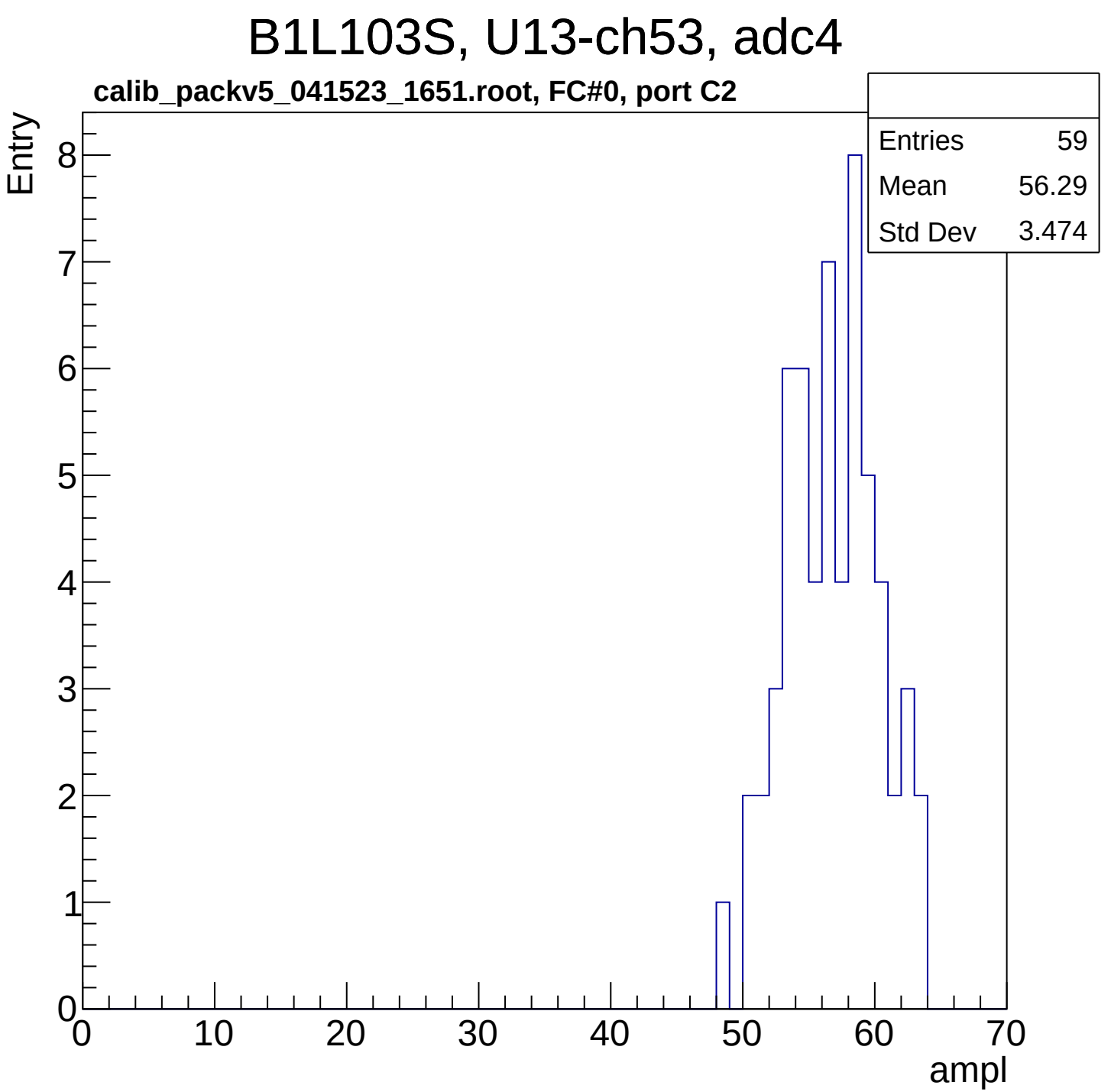
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch53, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 56.29
Std Dev 3.474
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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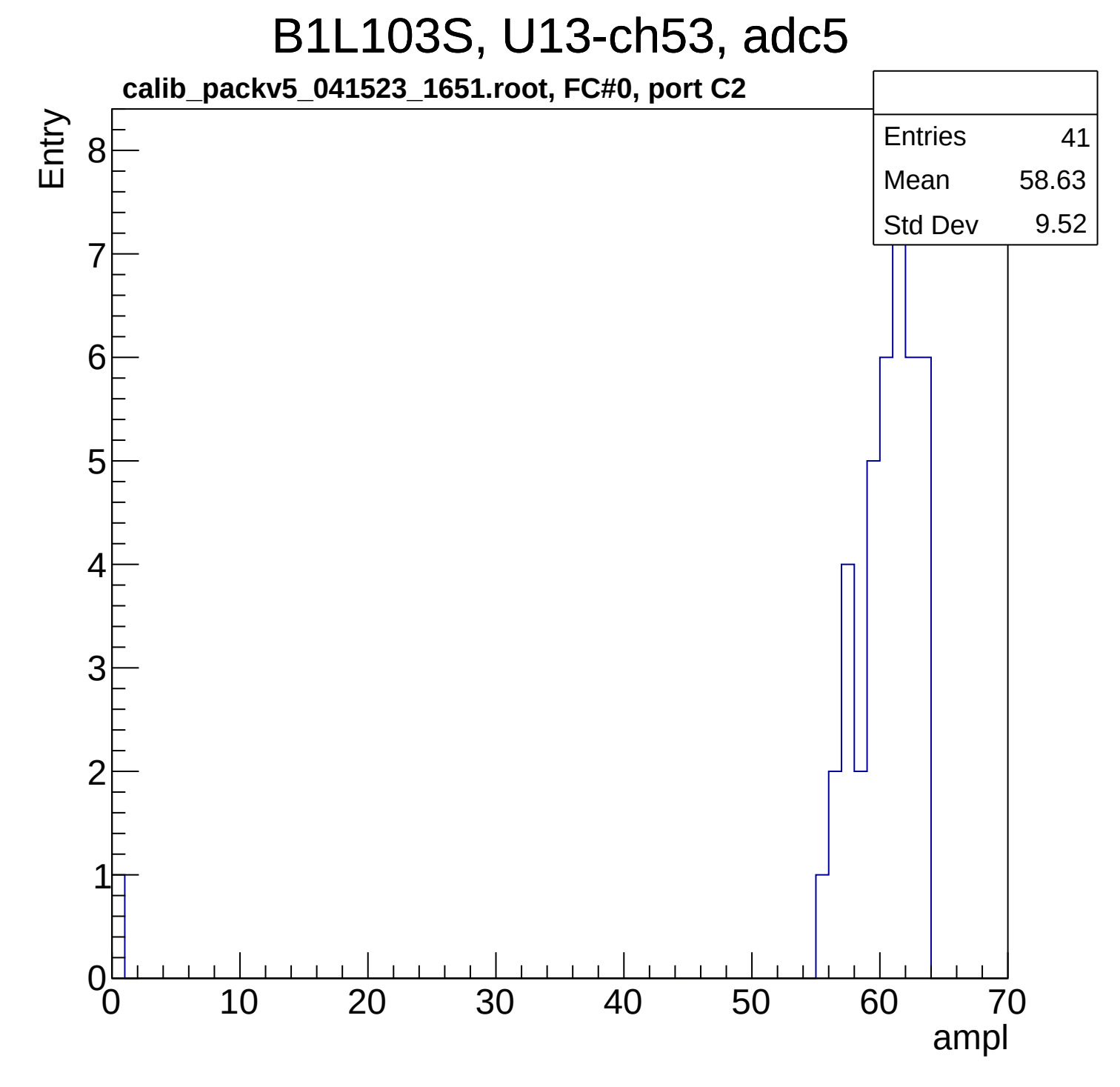
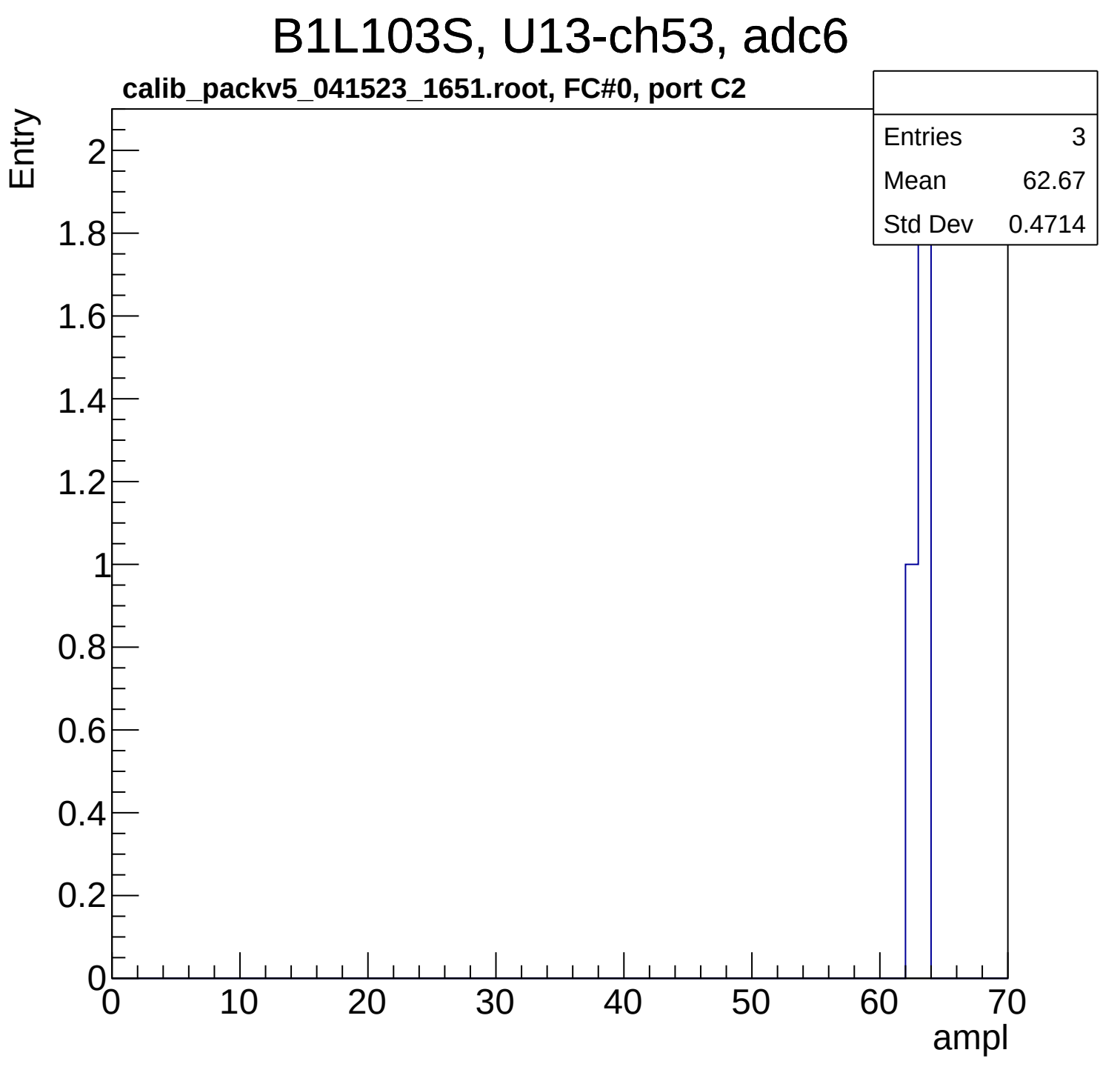
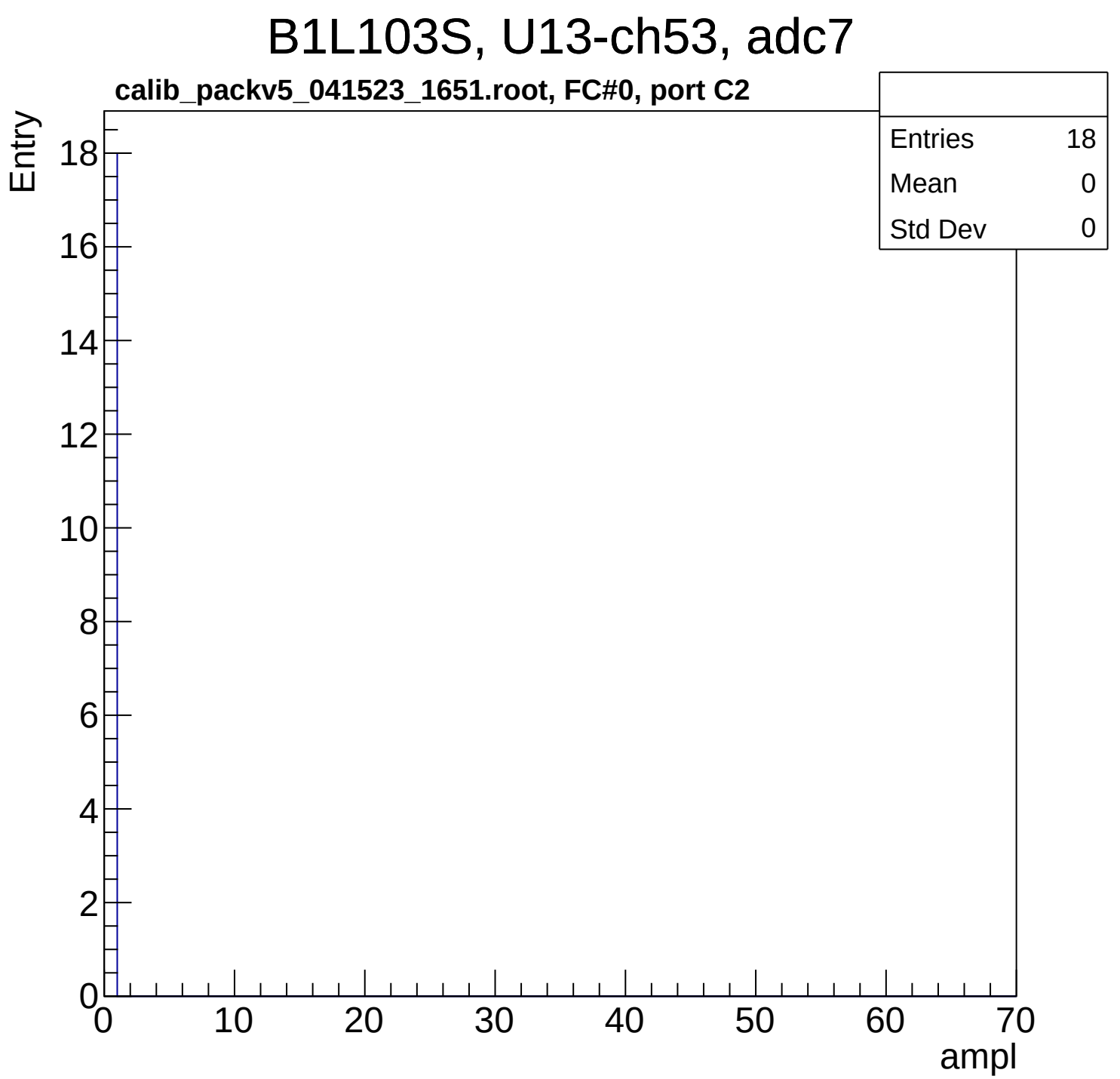
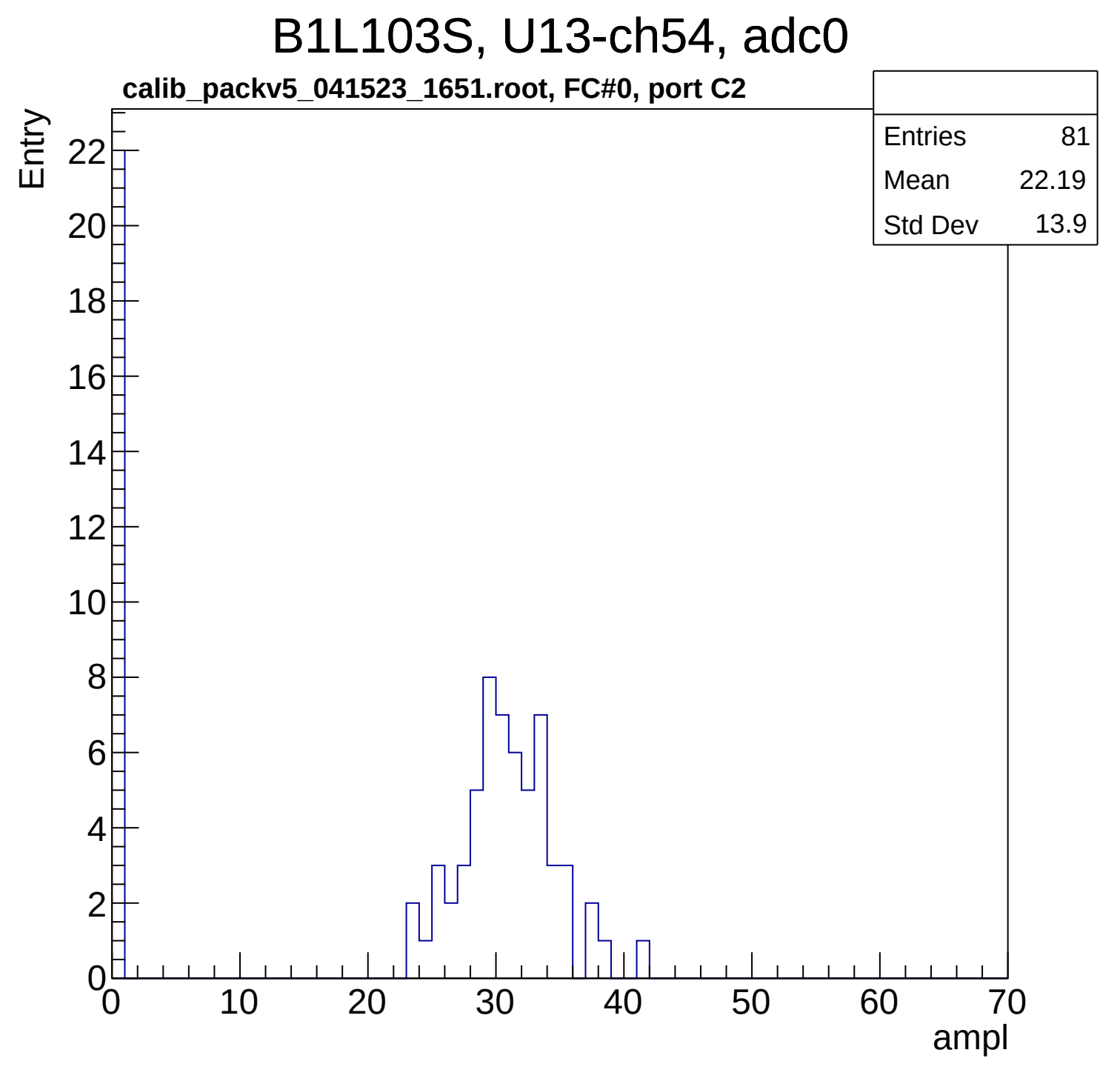
60
70


B1L103S, U13-ch53, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 58.63
Std Dev 9.52
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch53, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U13-ch53, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch54, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 22.19
Std Dev 13.9
Entry
ampl
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2
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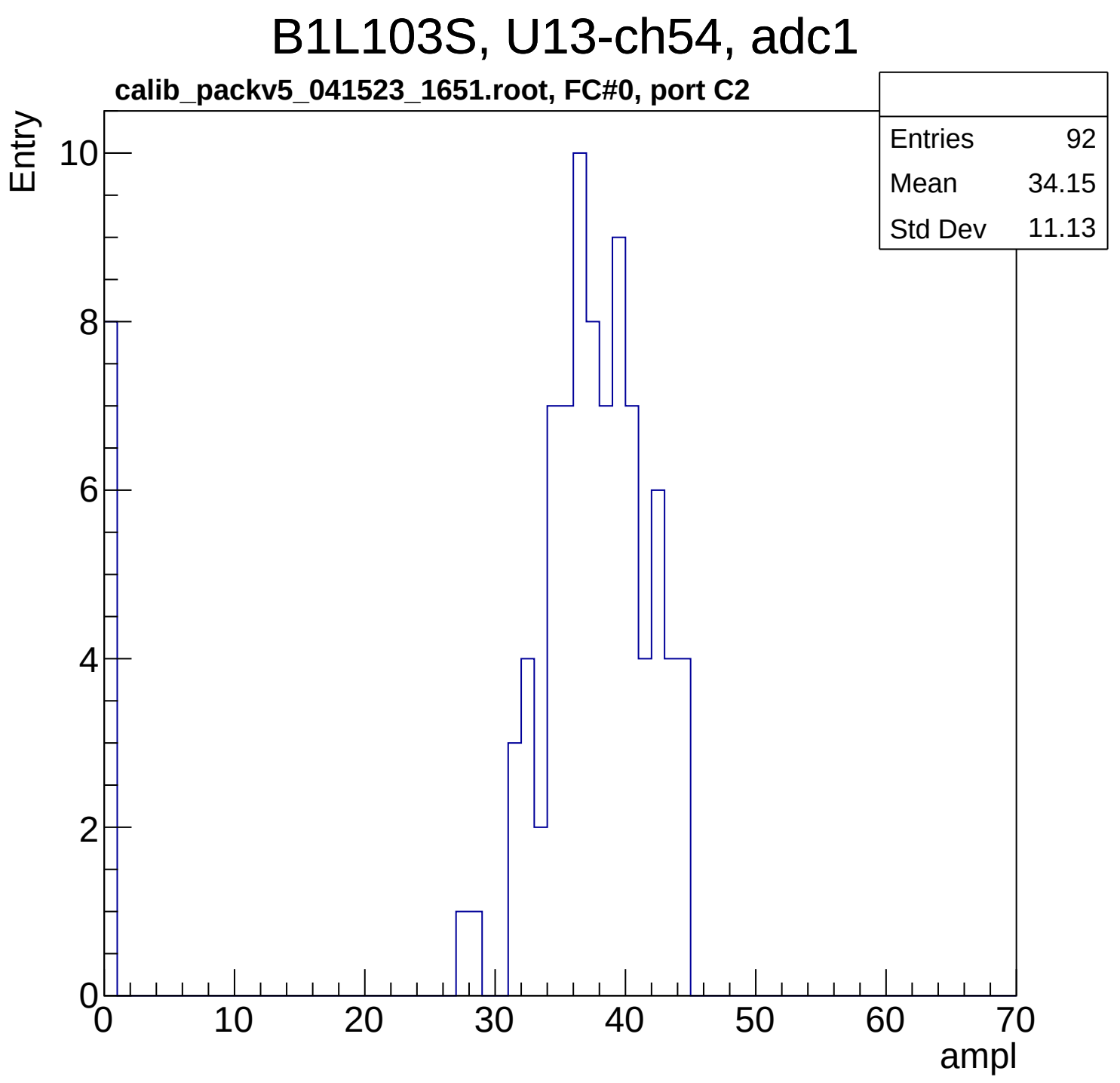
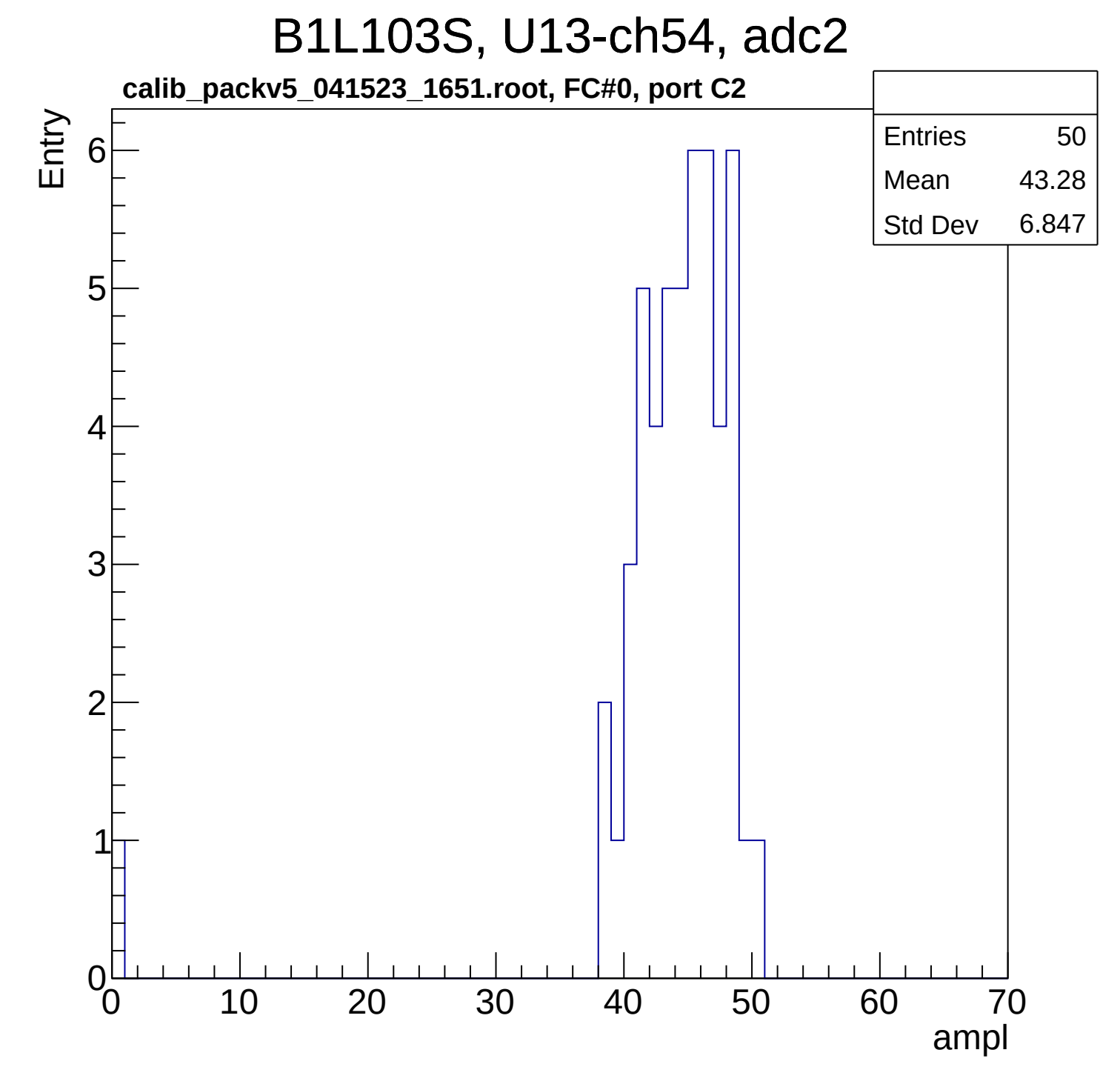
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U13-ch54, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 34.15
Std Dev 11.13
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch54, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 43.28
Std Dev 6.847
Entry
0
1
2
3
4
5
6
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10
20
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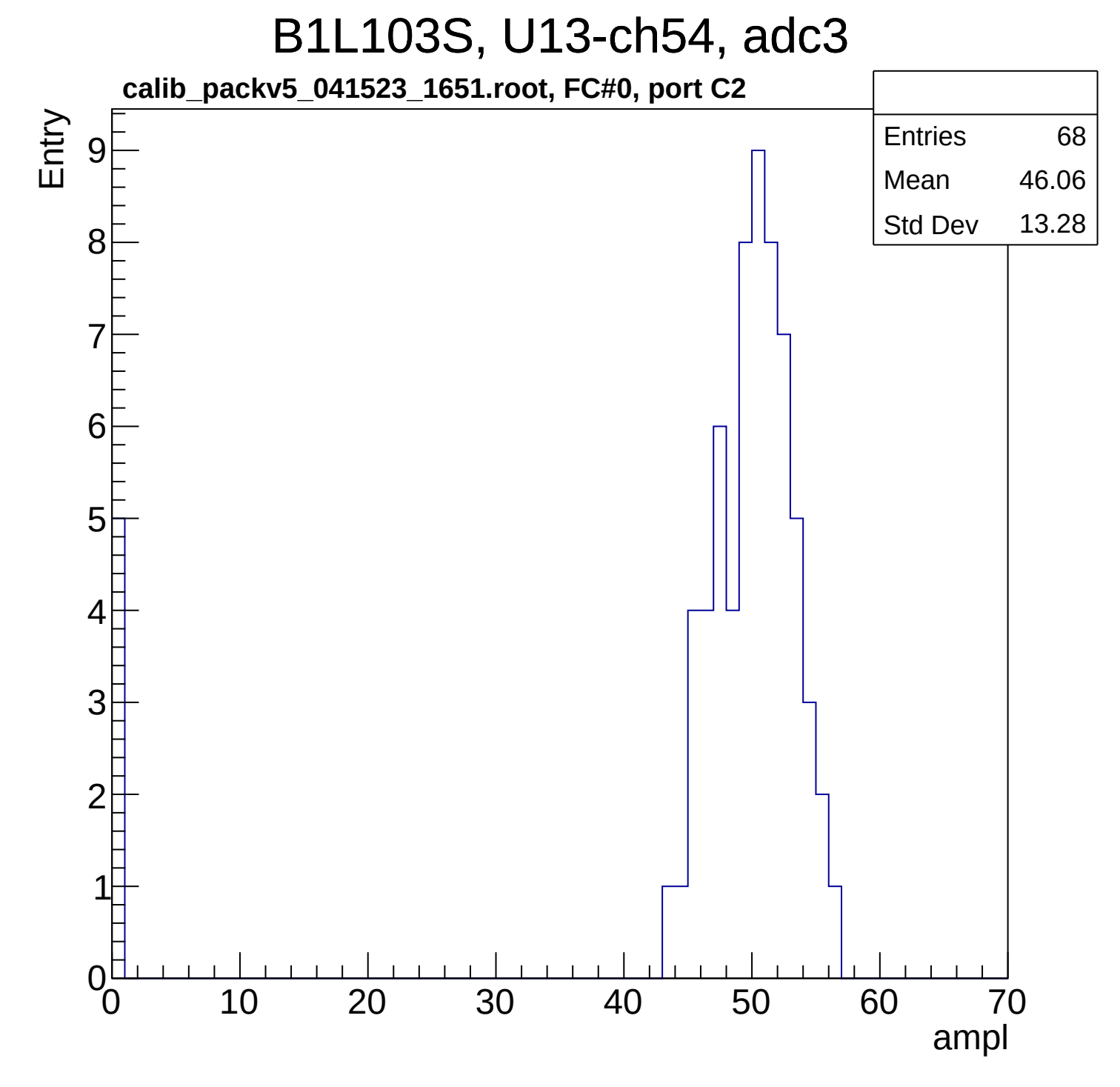
50
60
70
ampl


B1L103S, U13-ch54, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 46.06
Std Dev 13.28
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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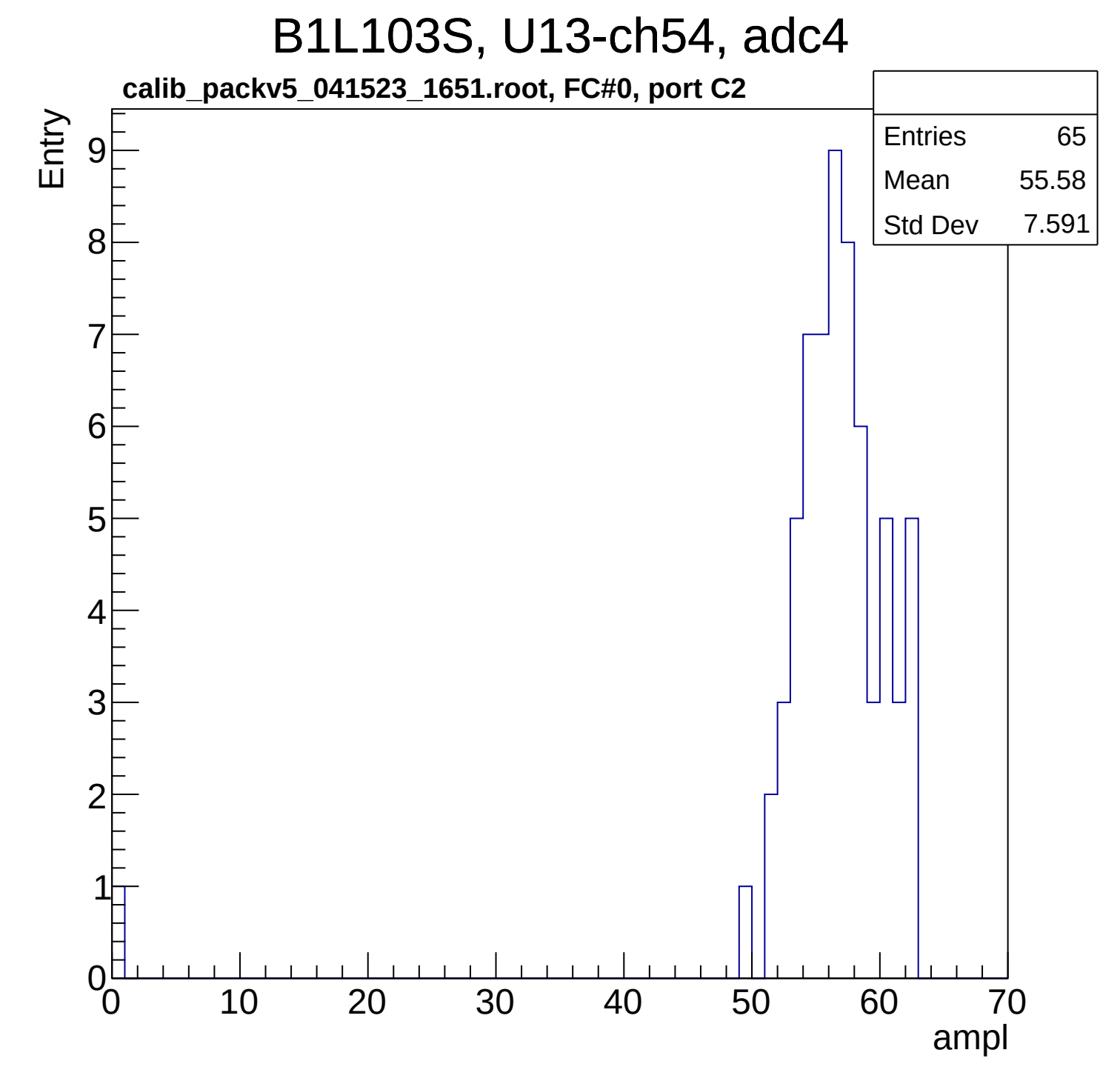
B1L103S, U13-ch54, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 55.58
Std Dev 7.591
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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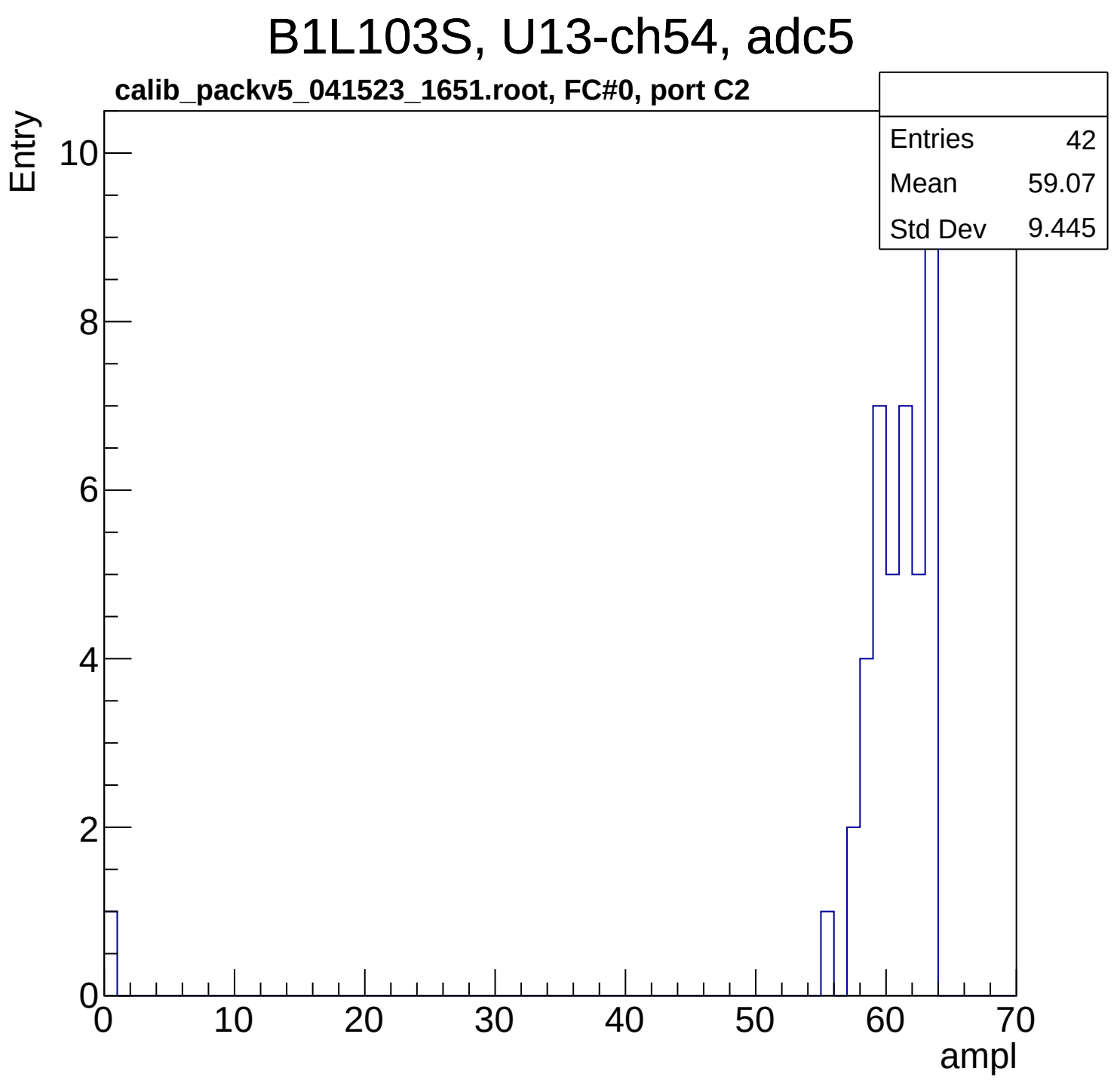
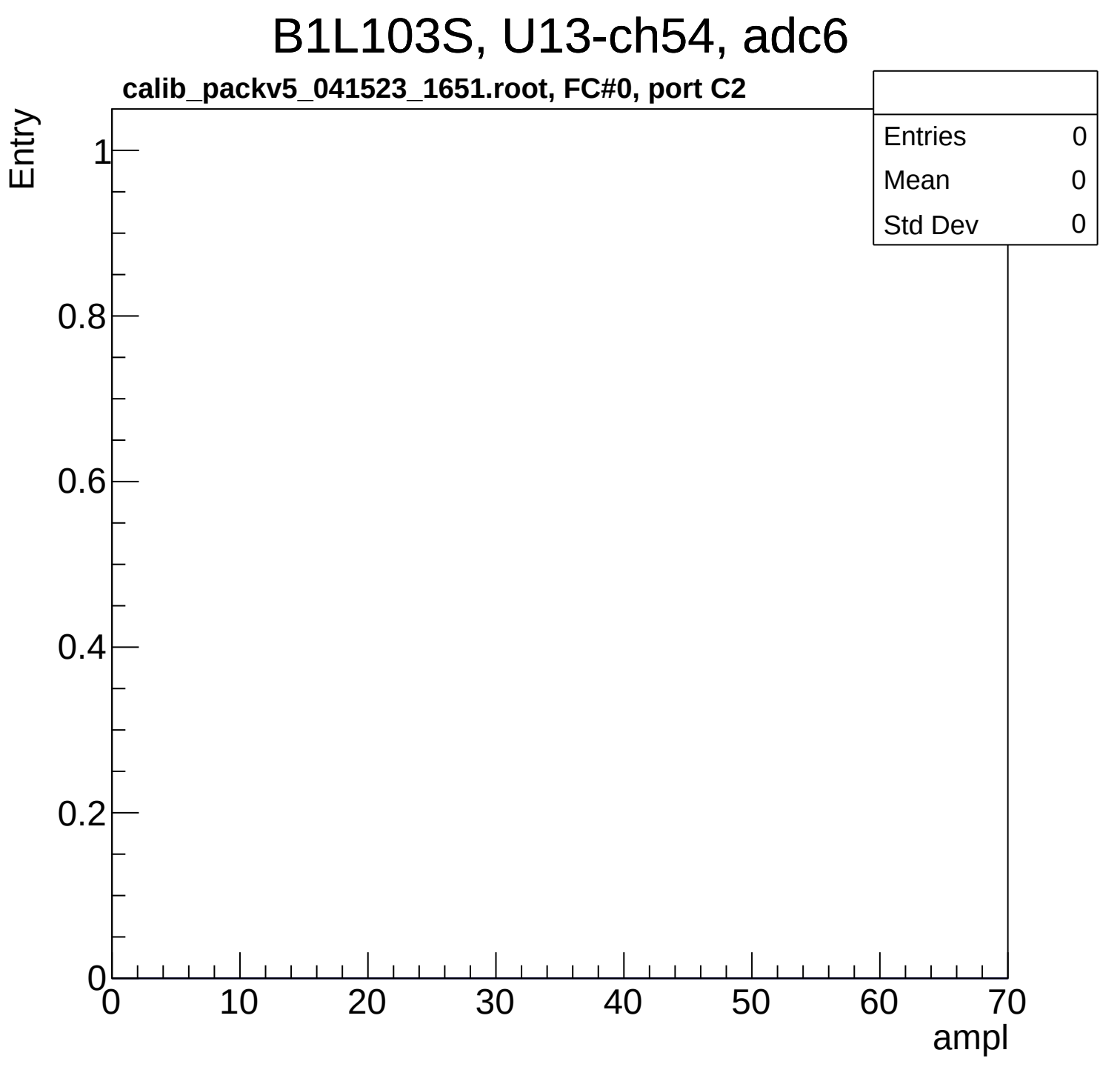
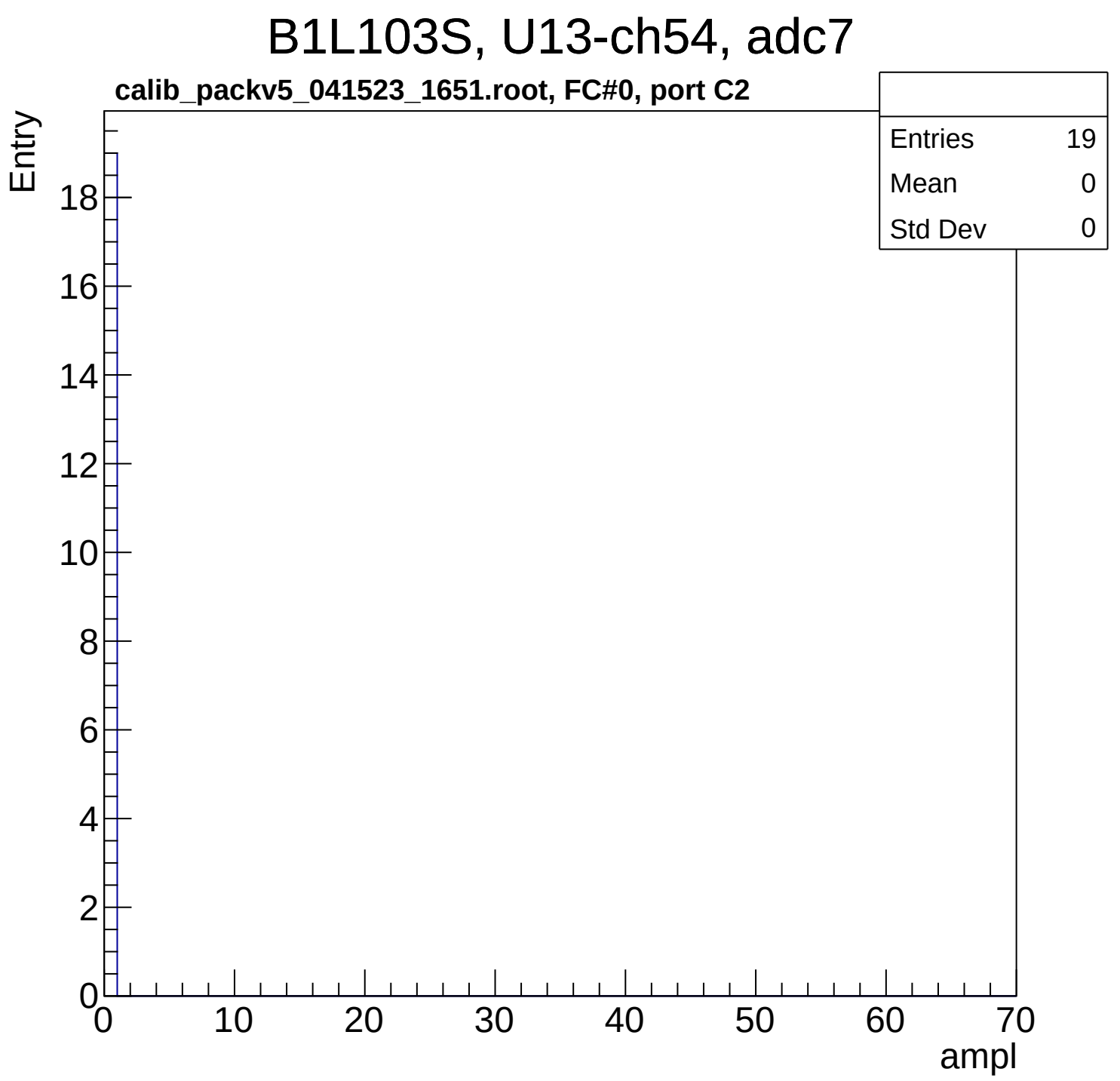
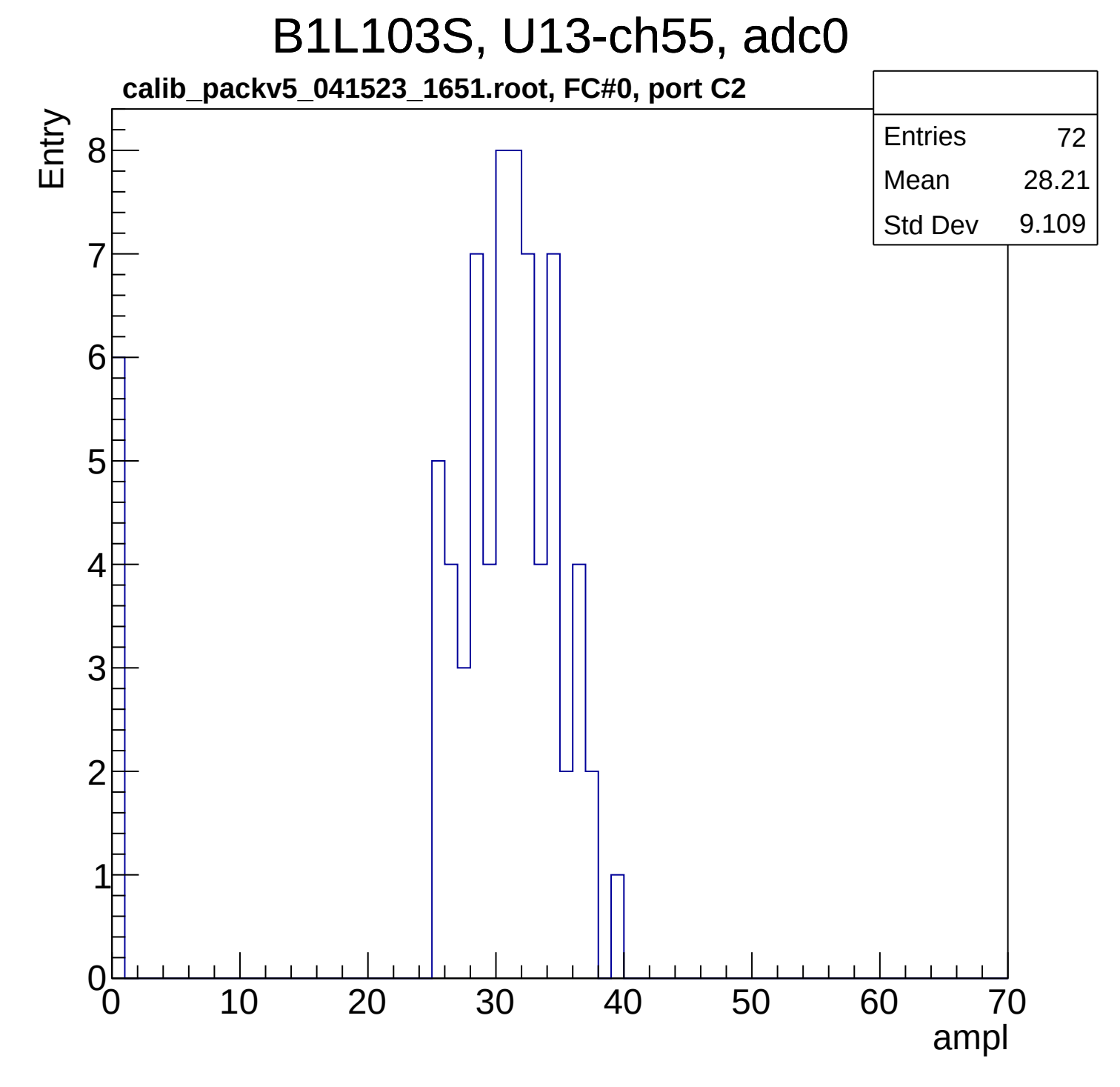
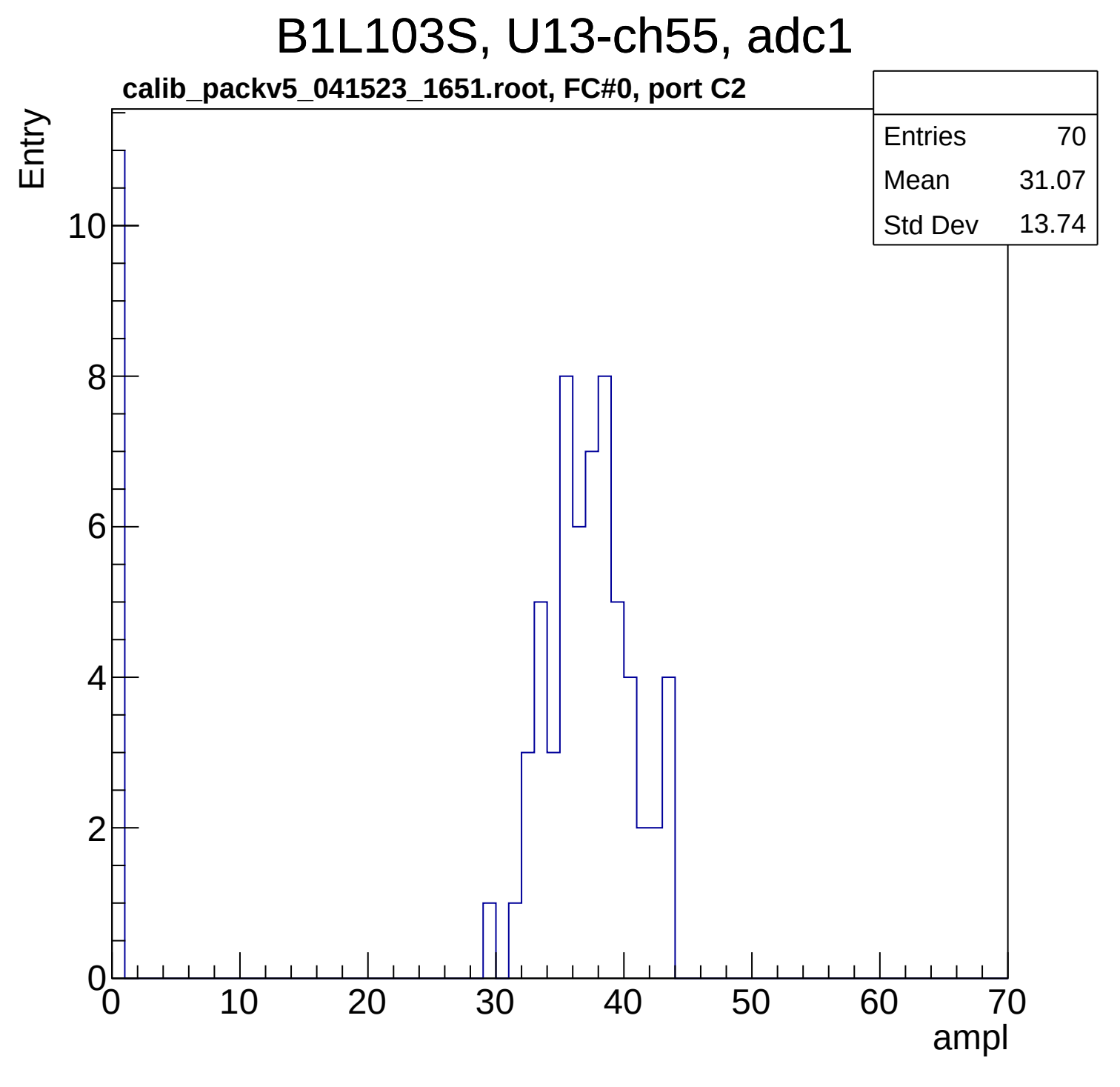
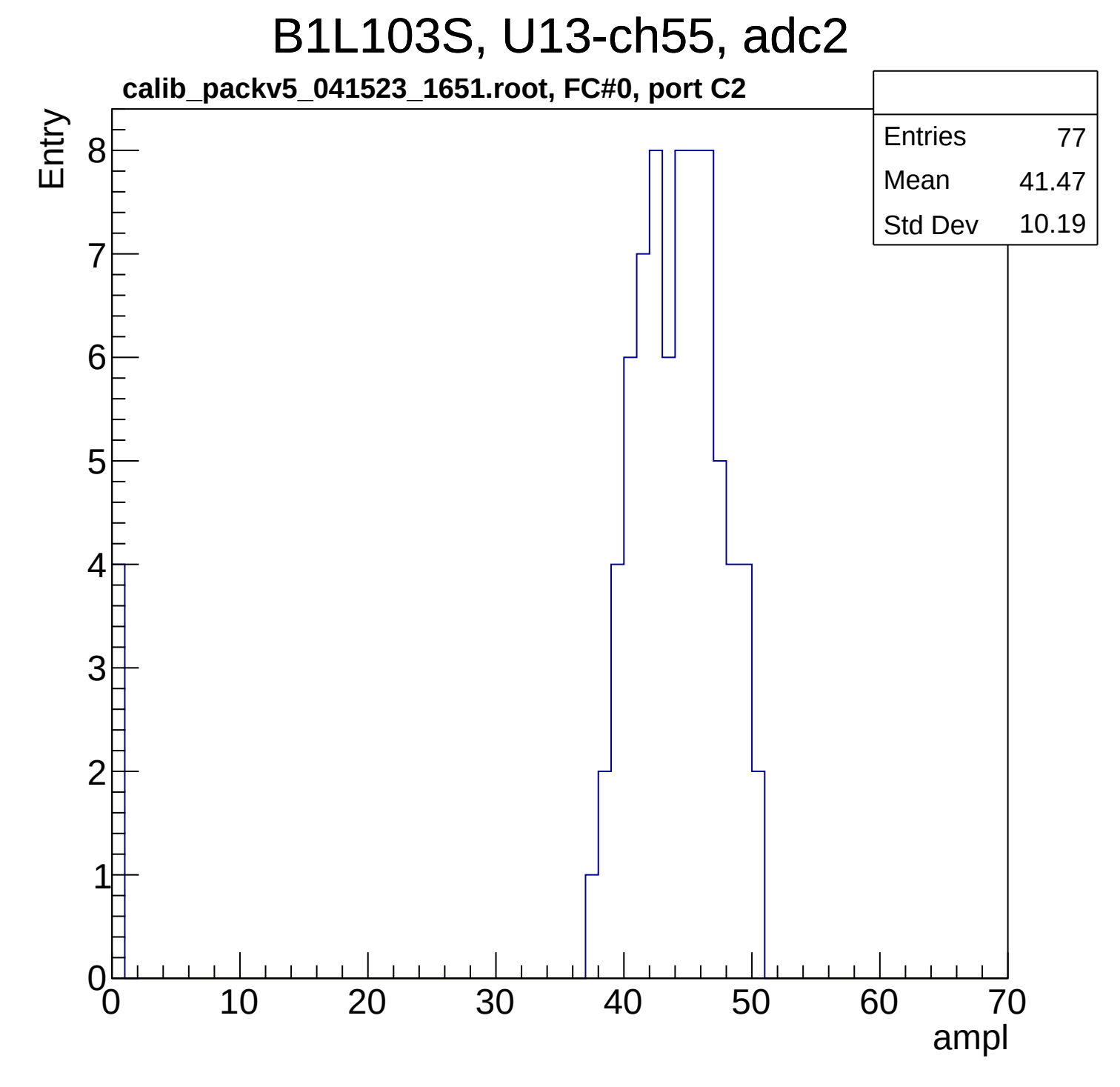

B1L103S, U13-ch54, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 59.07
Std Dev 9.445
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

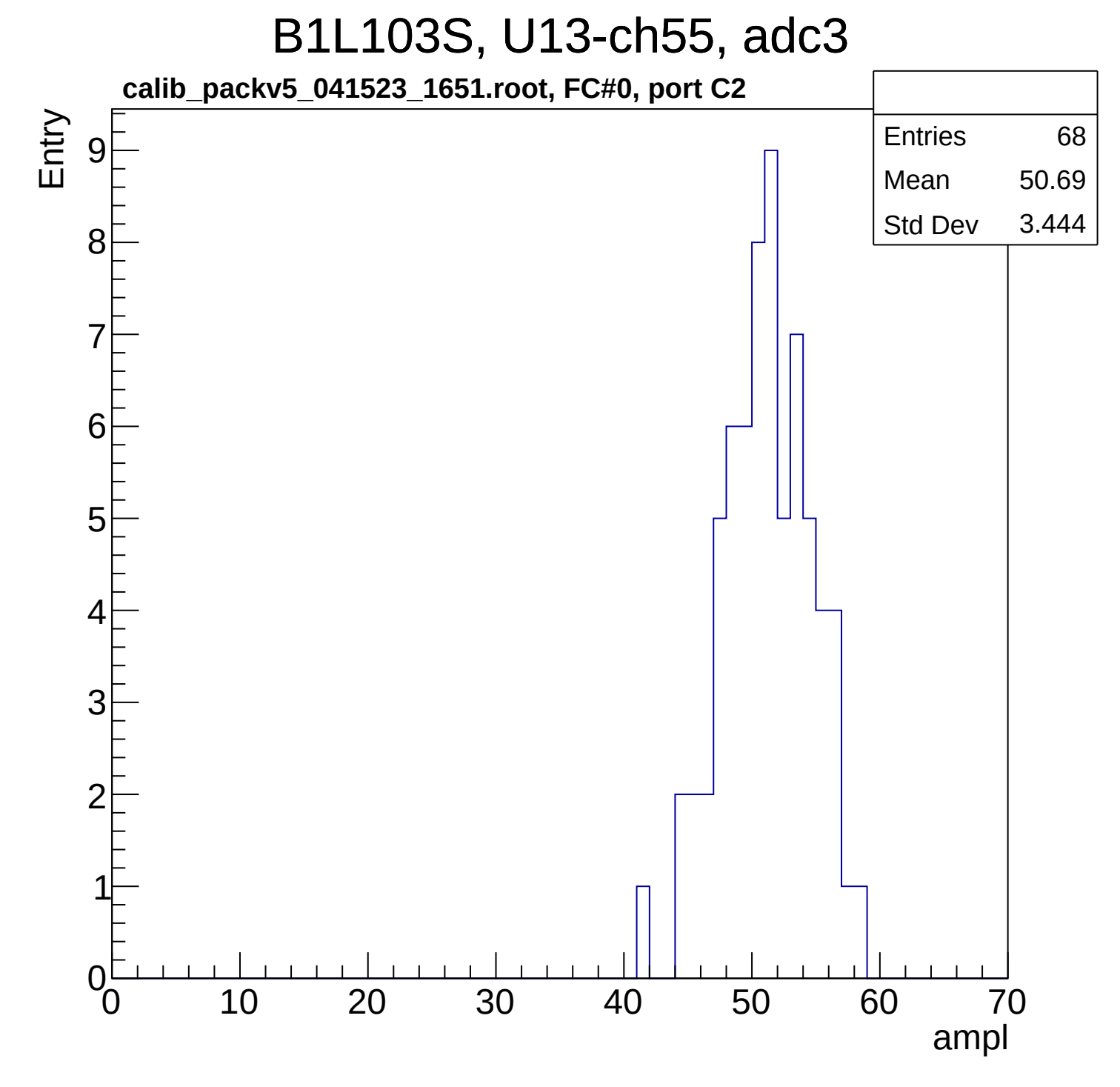

B1L103S, U13-ch54, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

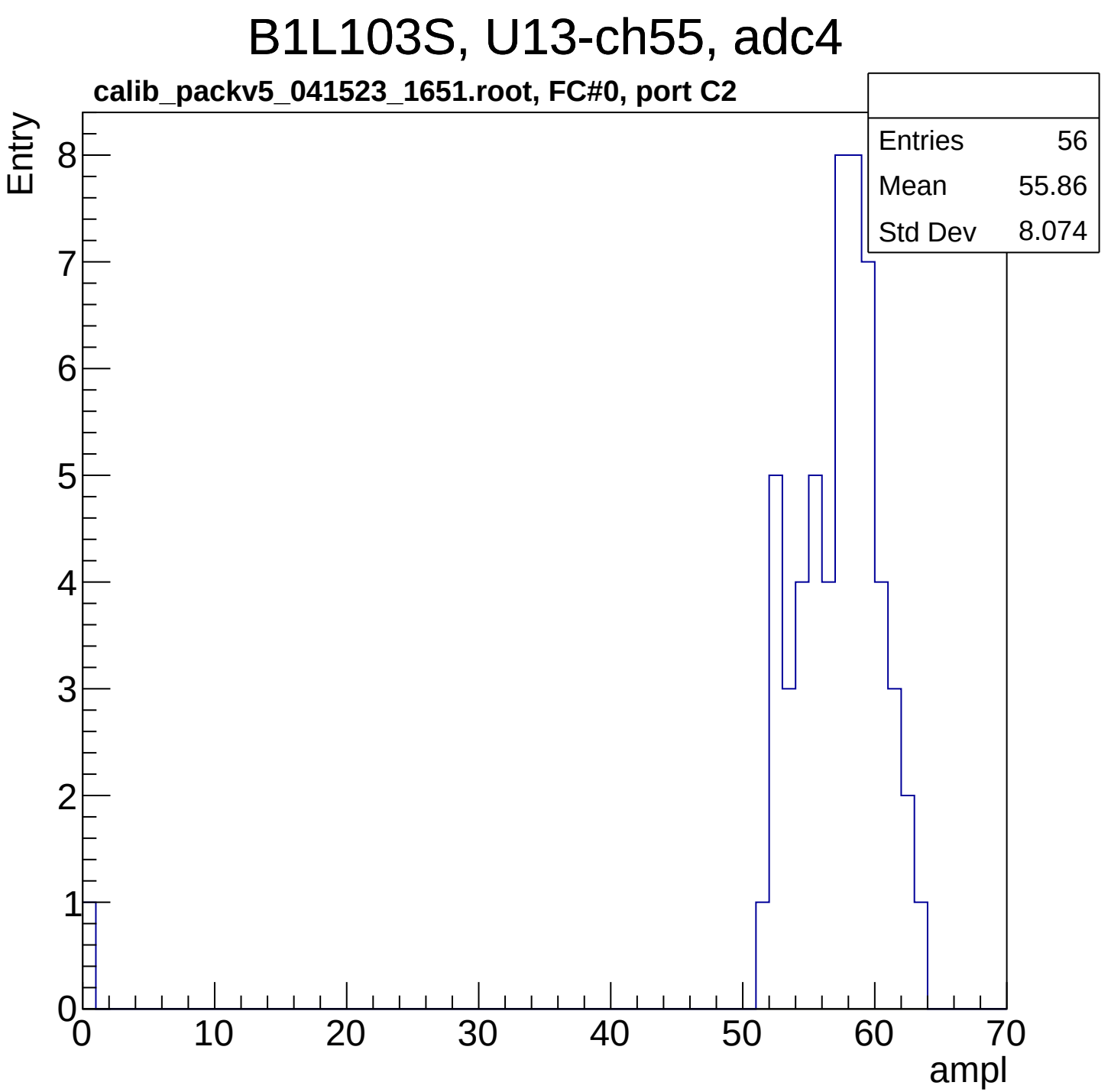

B1L103S, U13-ch54, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

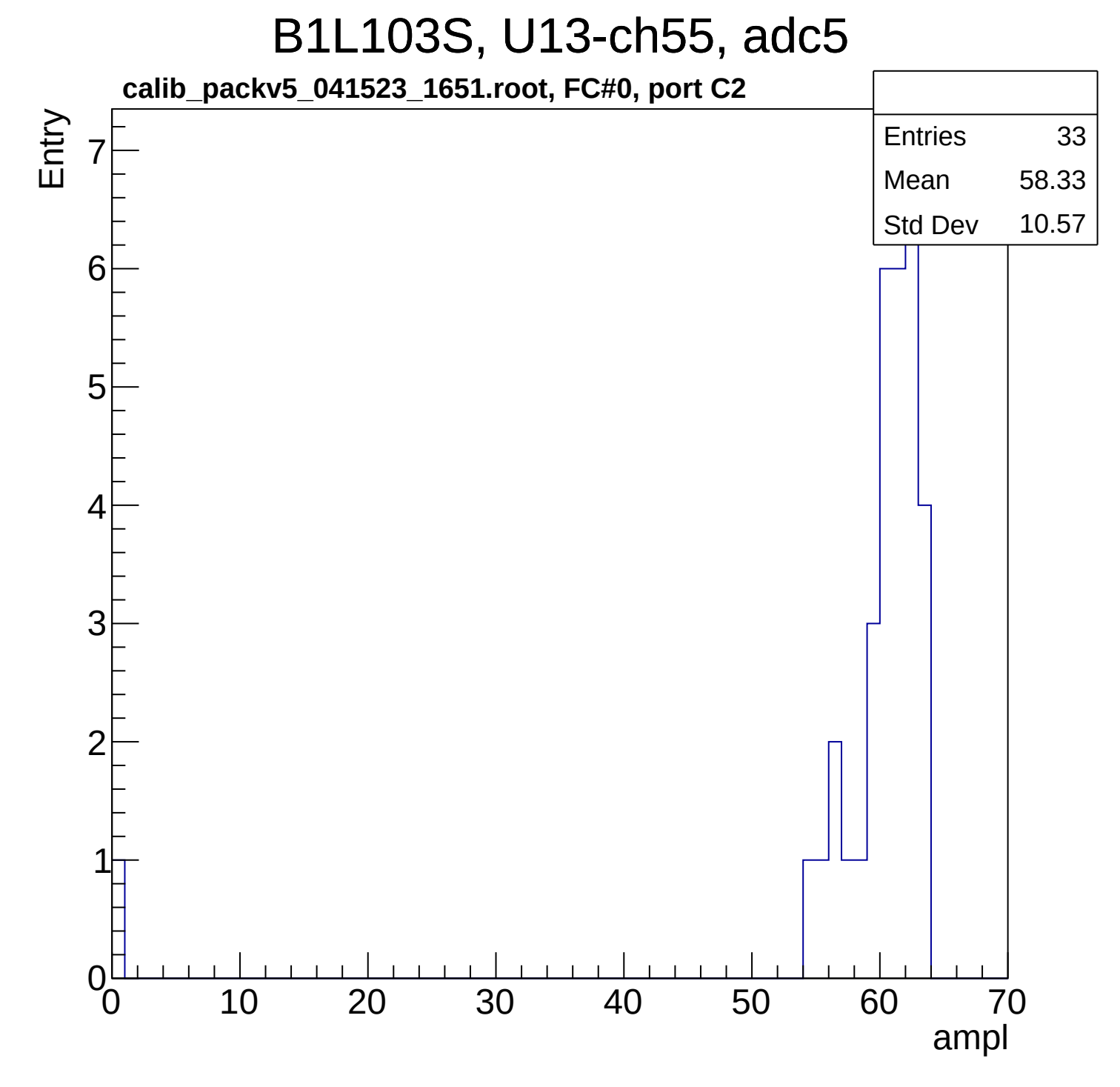

B1L103S, U13-ch55, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 28.21
Std Dev 9.109
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

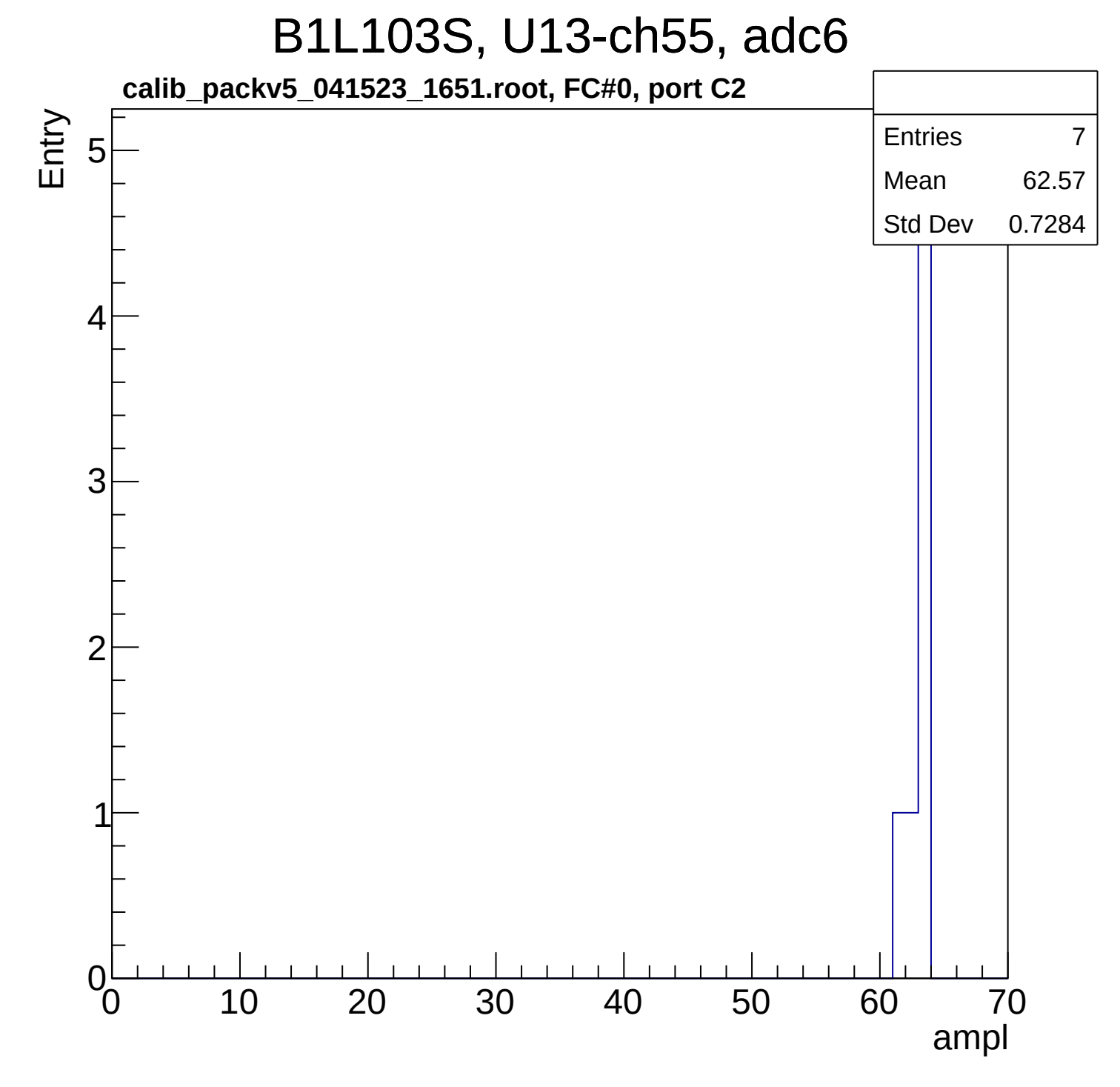

B1L103S, U13-ch55, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 31.07
Std Dev 13.74
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

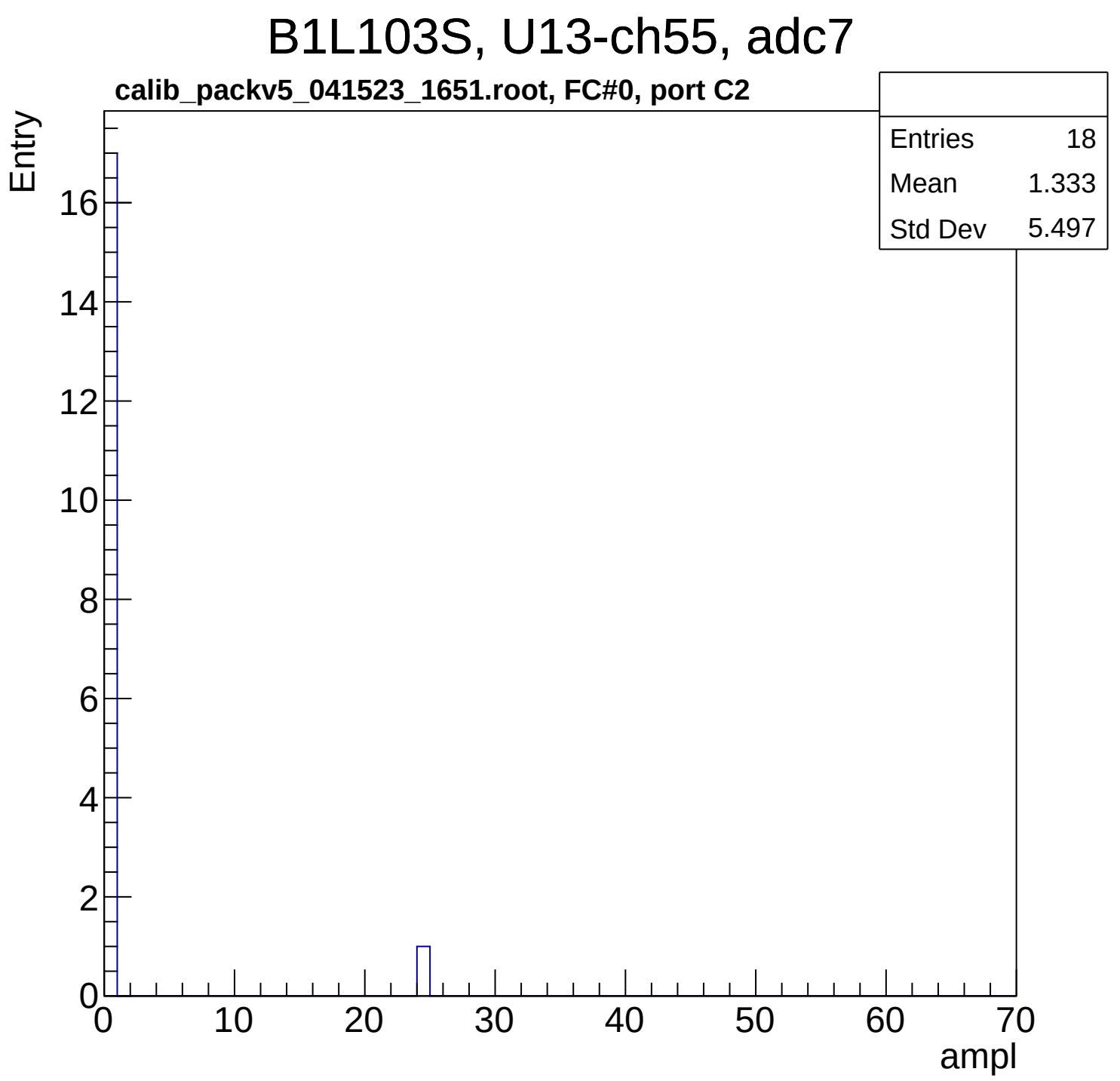

B1L103S, U13-ch55, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 41.47
Std Dev 10.19
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch55, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 50.69
Std Dev 3.444
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch55, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 55.86
Std Dev 8.074
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch55, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 58.33
Std Dev 10.57
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch55, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62.57
Std Dev 0.7284
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U13-ch55, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.333
Std Dev 5.497
Entry
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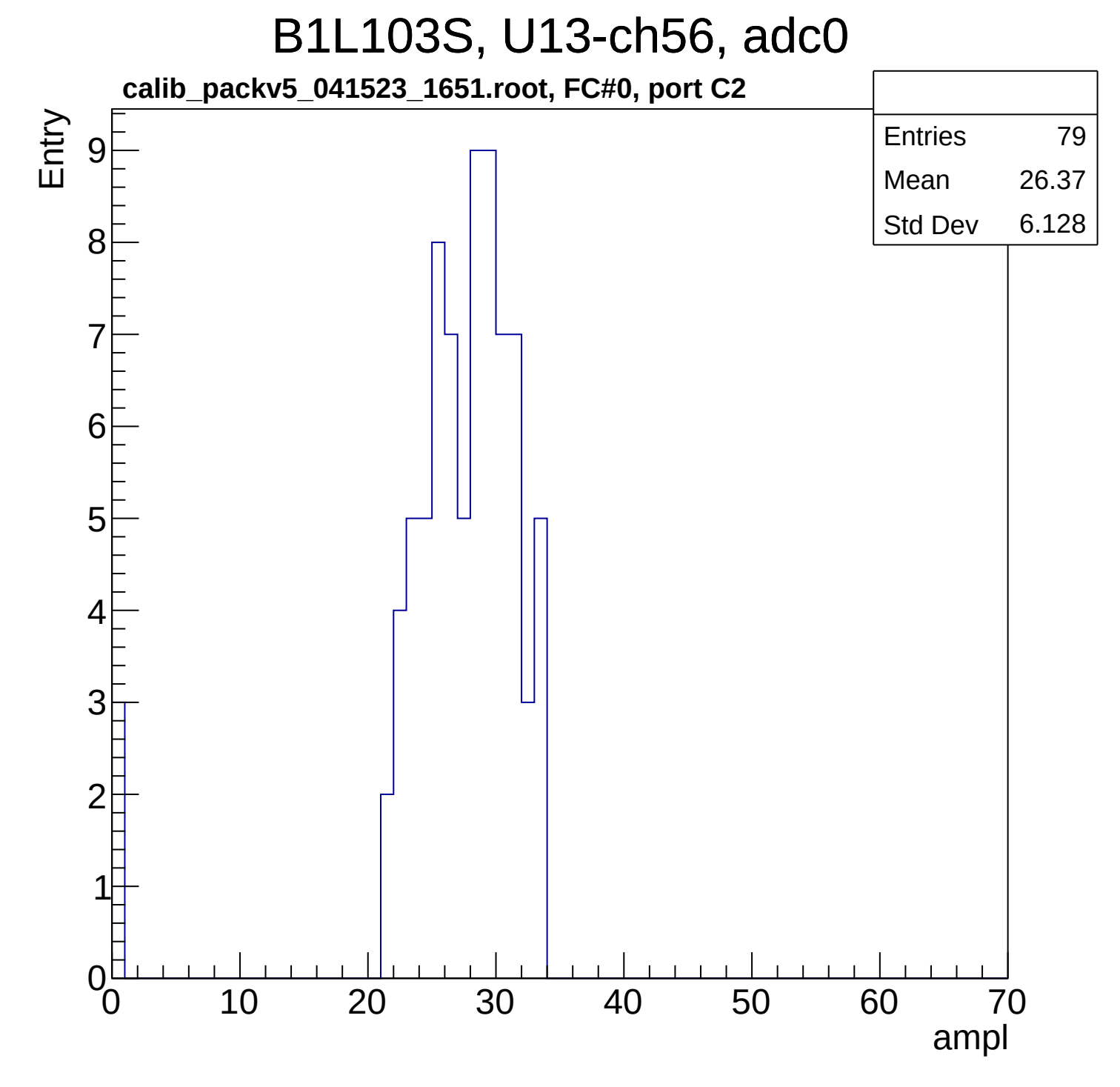
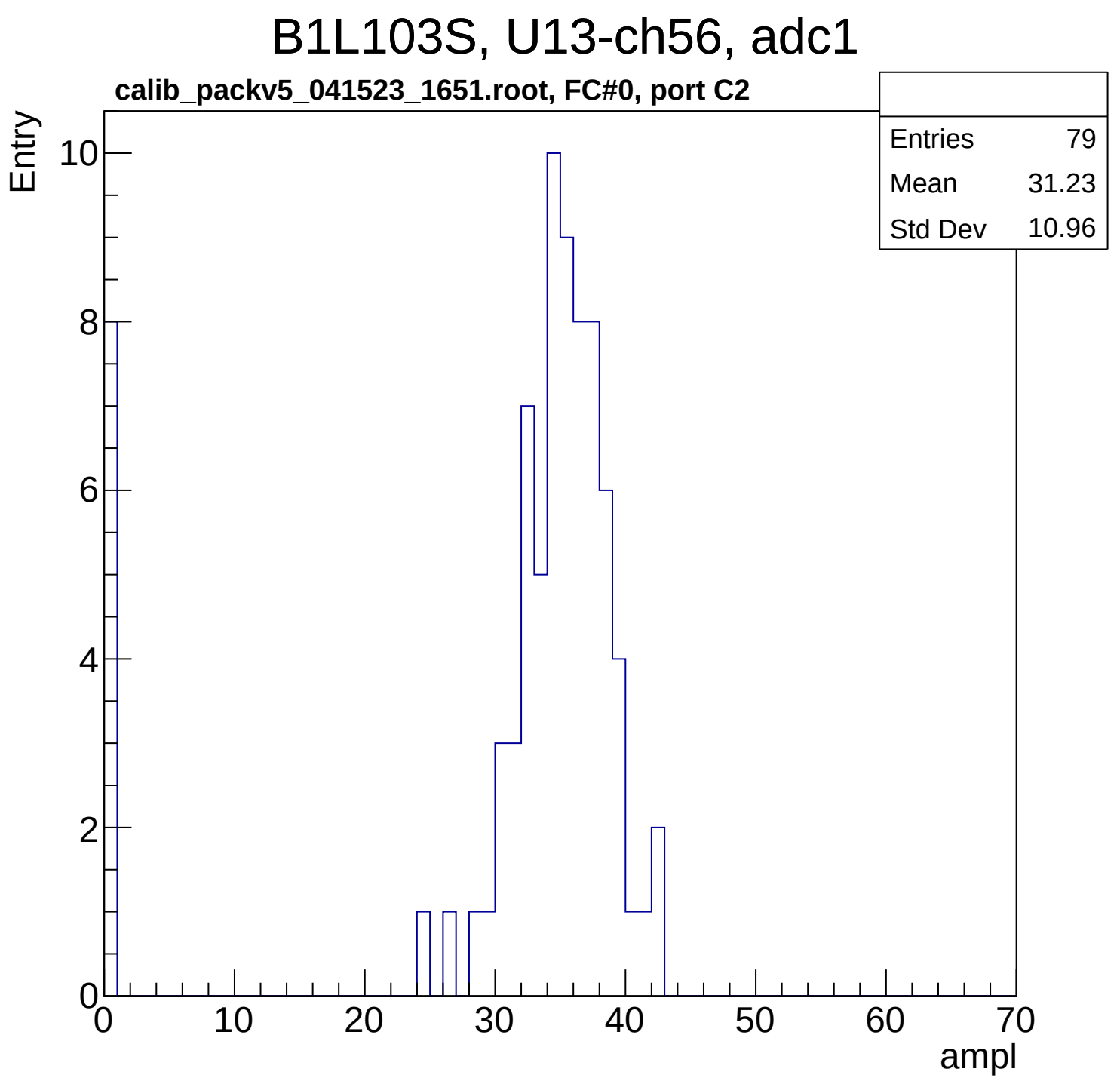
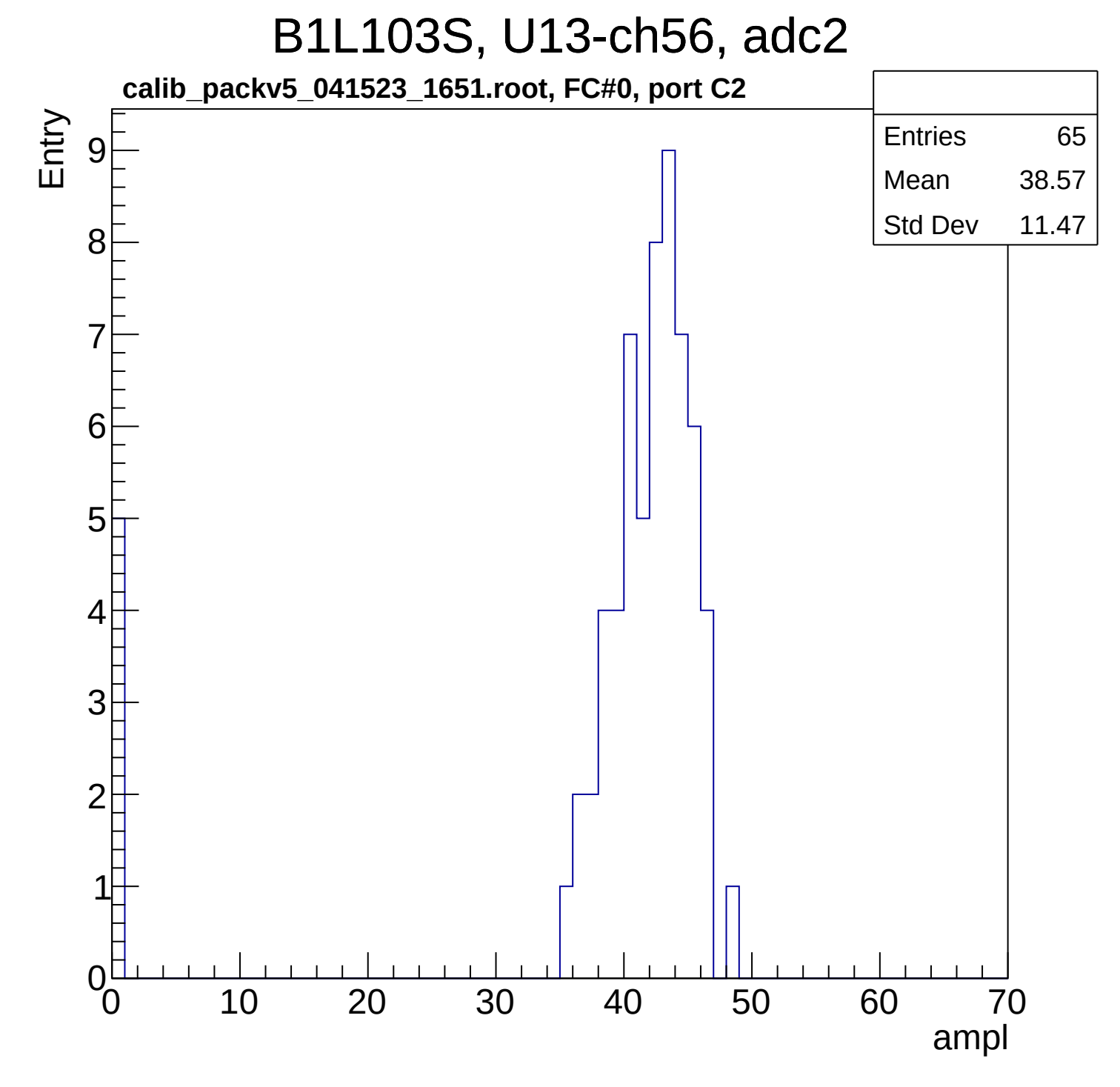
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch56, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 26.37
Std Dev 6.128
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch56, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 31.23
Std Dev 10.96
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch56, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 38.57
Std Dev 11.47
Entry
ampl
0
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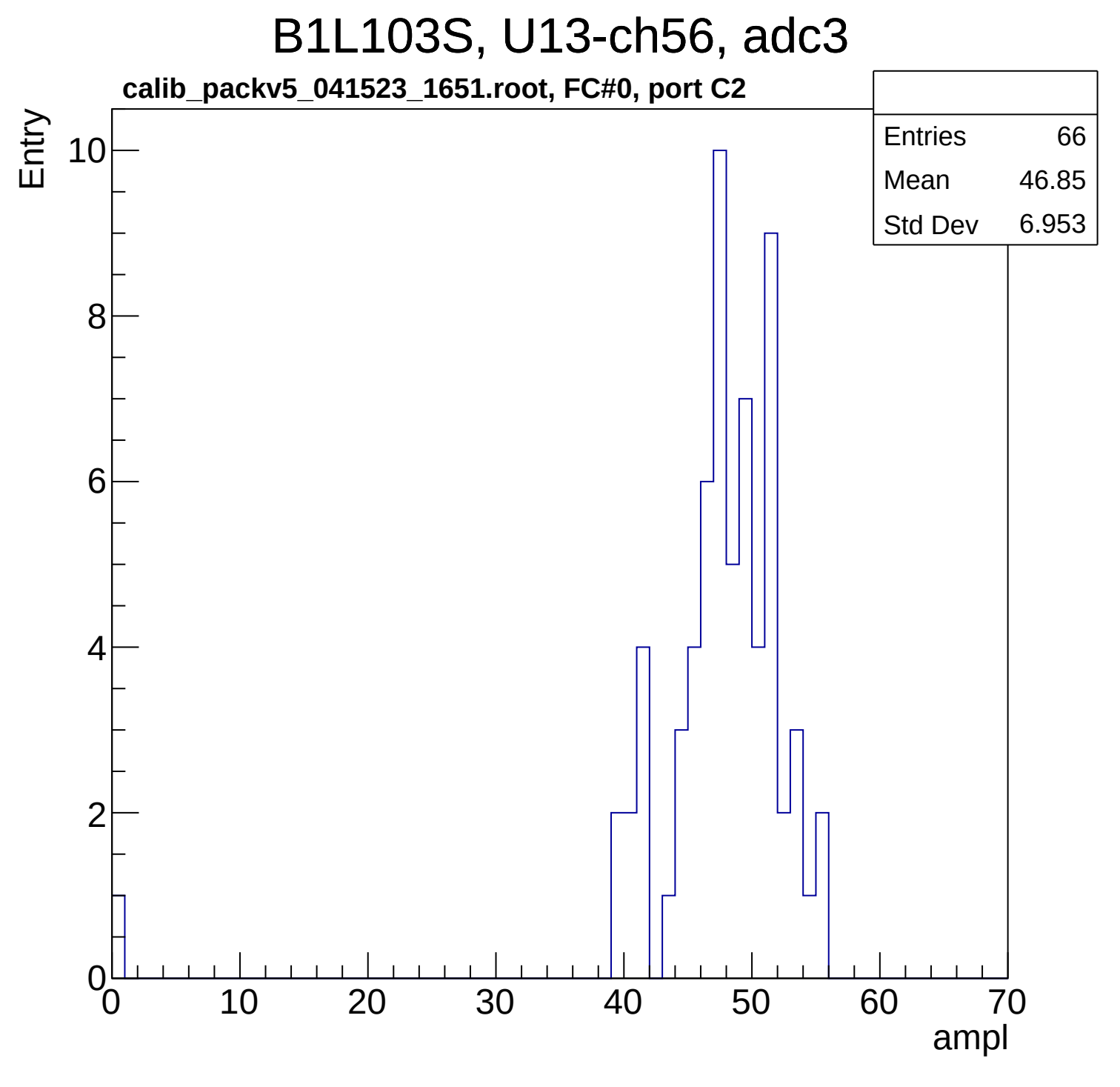
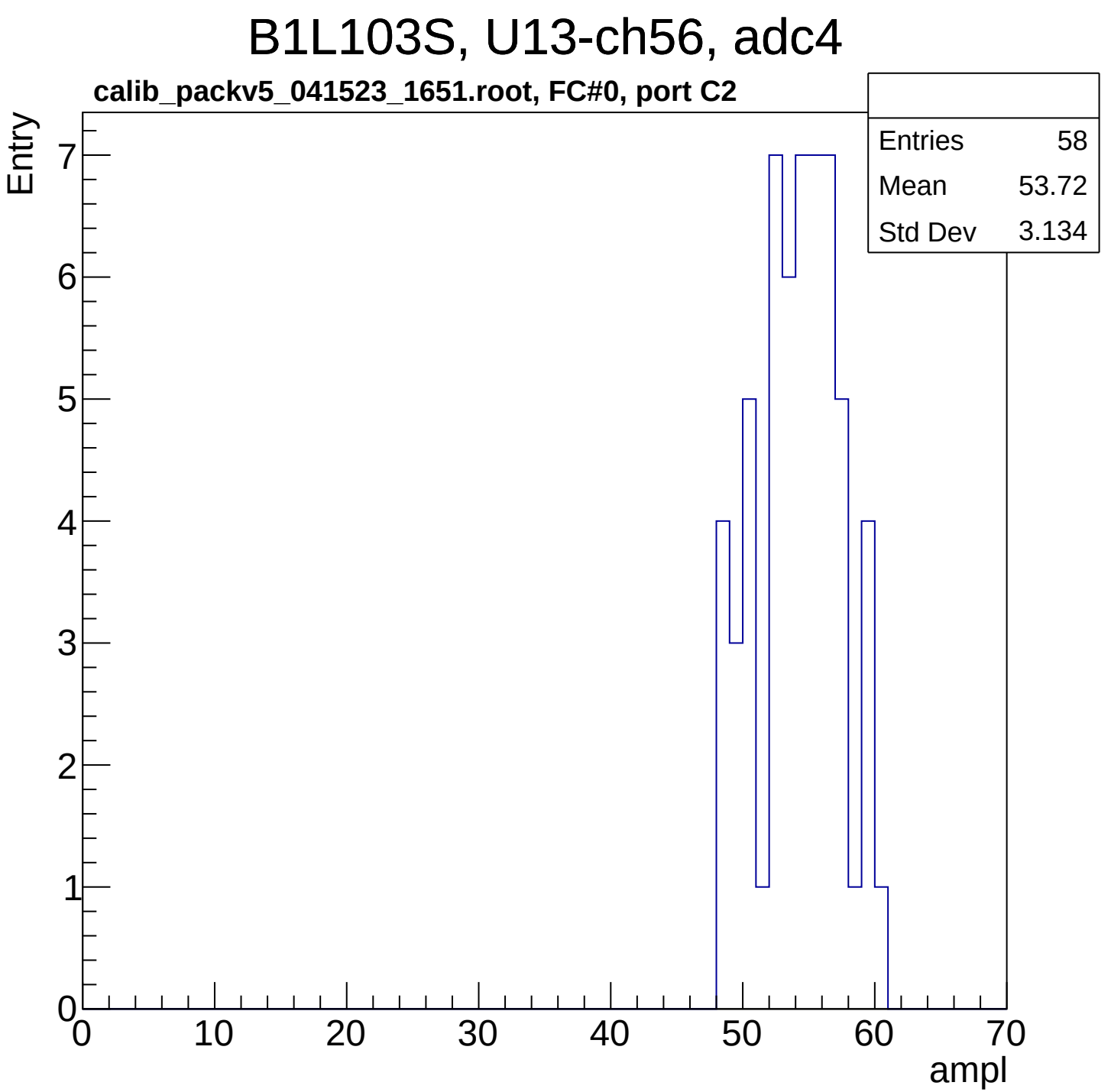
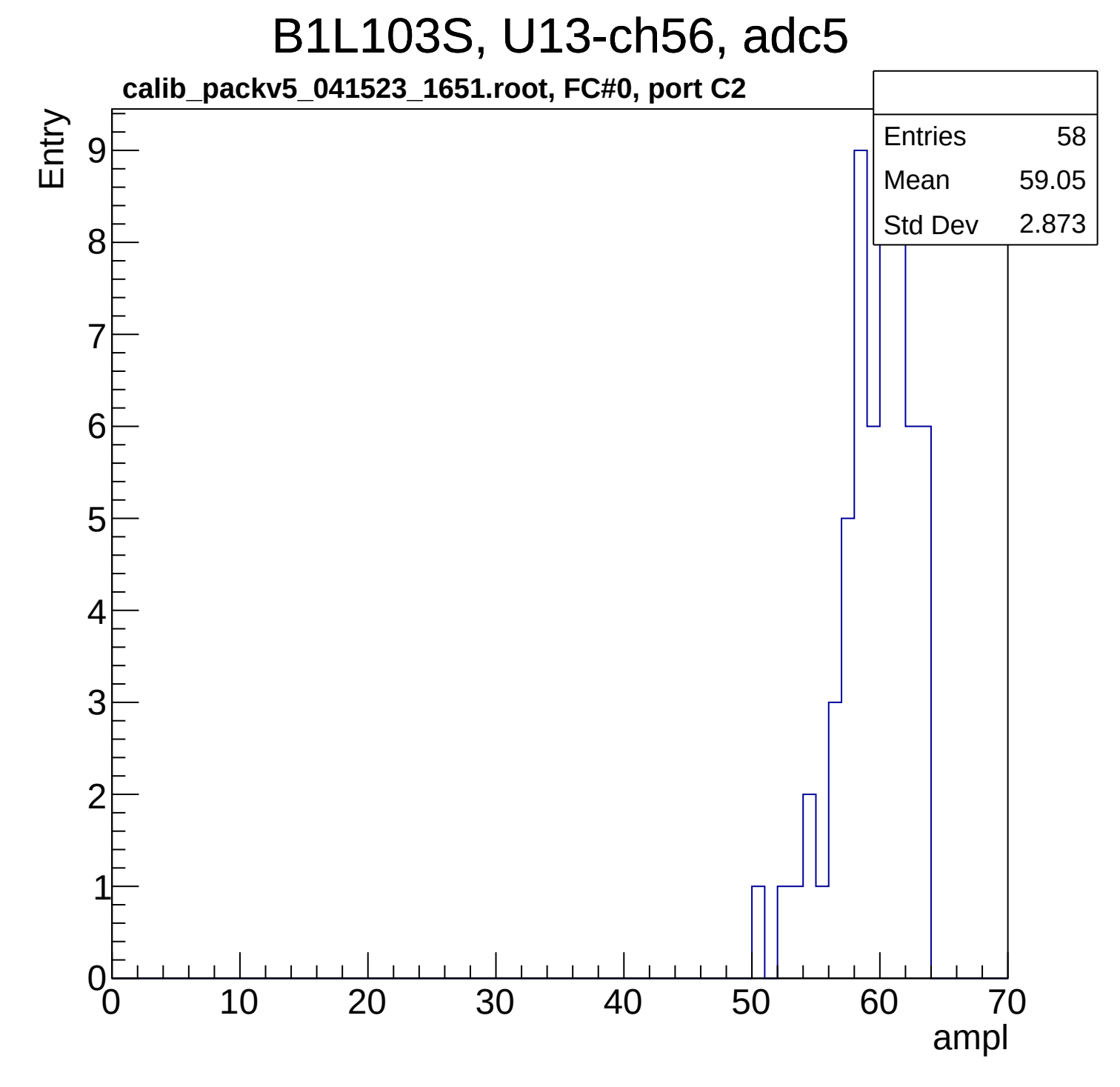
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch56, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 46.85
Std Dev 6.953
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch56, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 53.72
Std Dev 3.134
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch56, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 59.05
Std Dev 2.873
Entry
ampl
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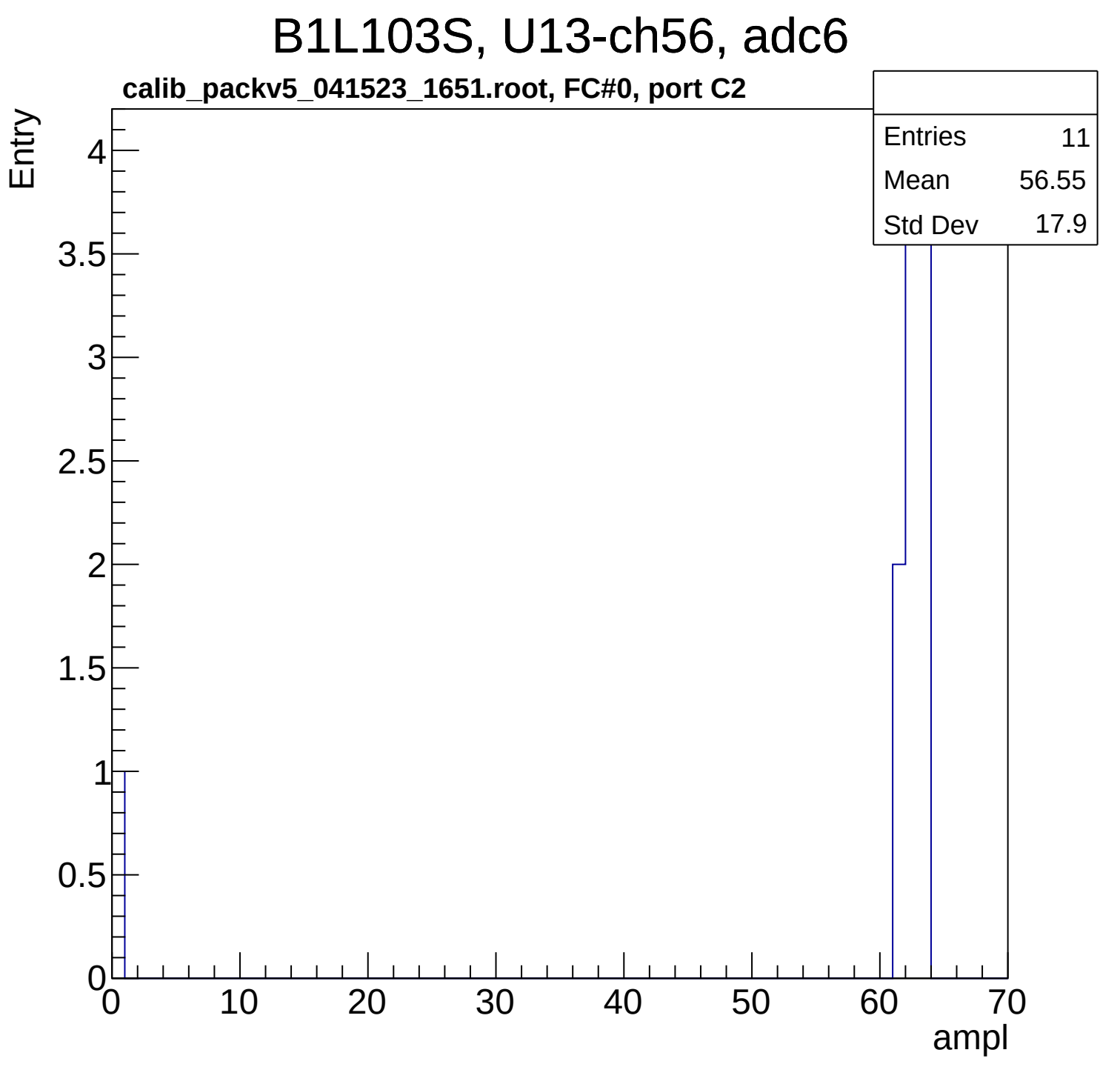
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U13-ch56, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 56.55
Std Dev 17.9
Entry
ampl
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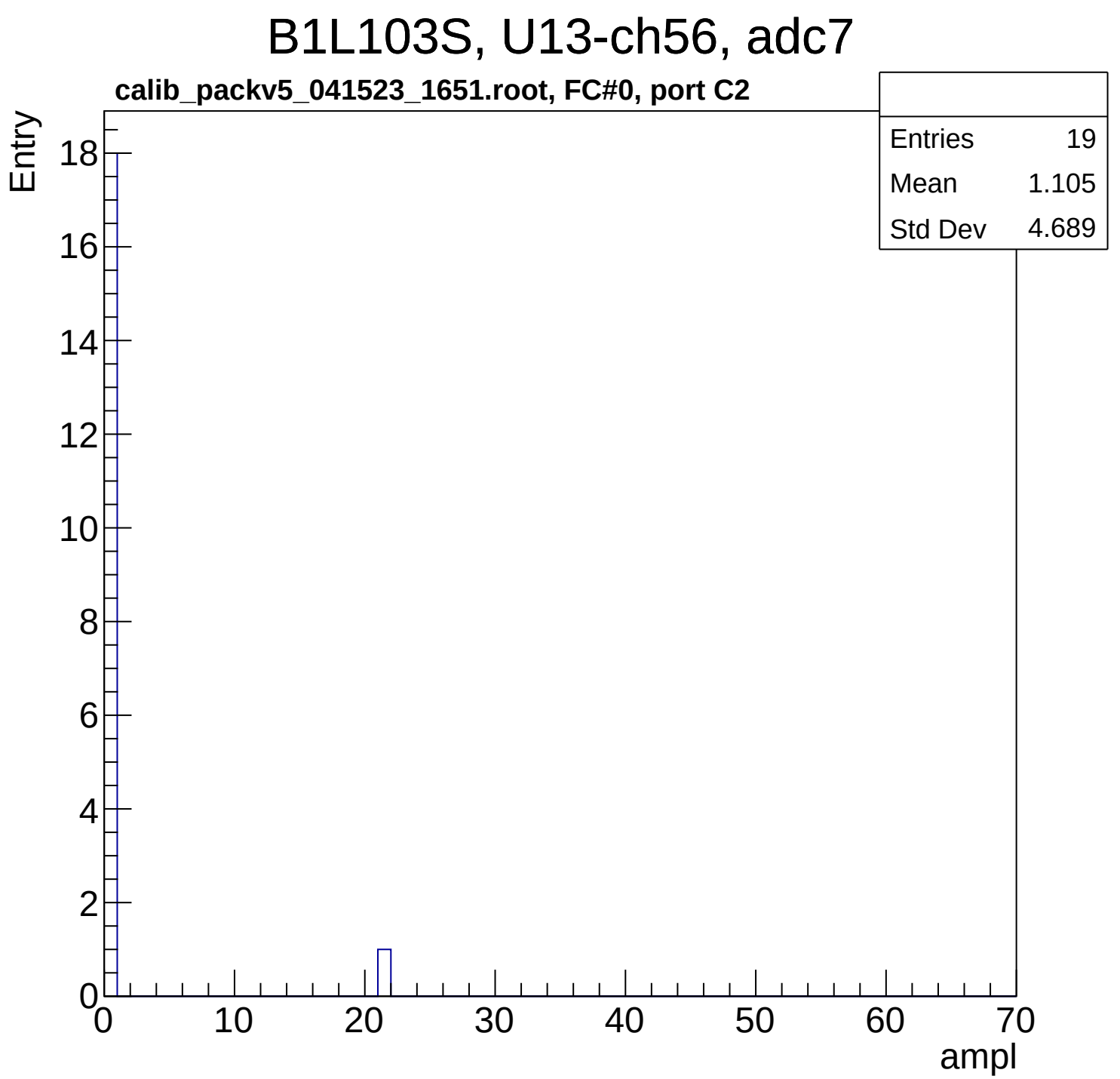
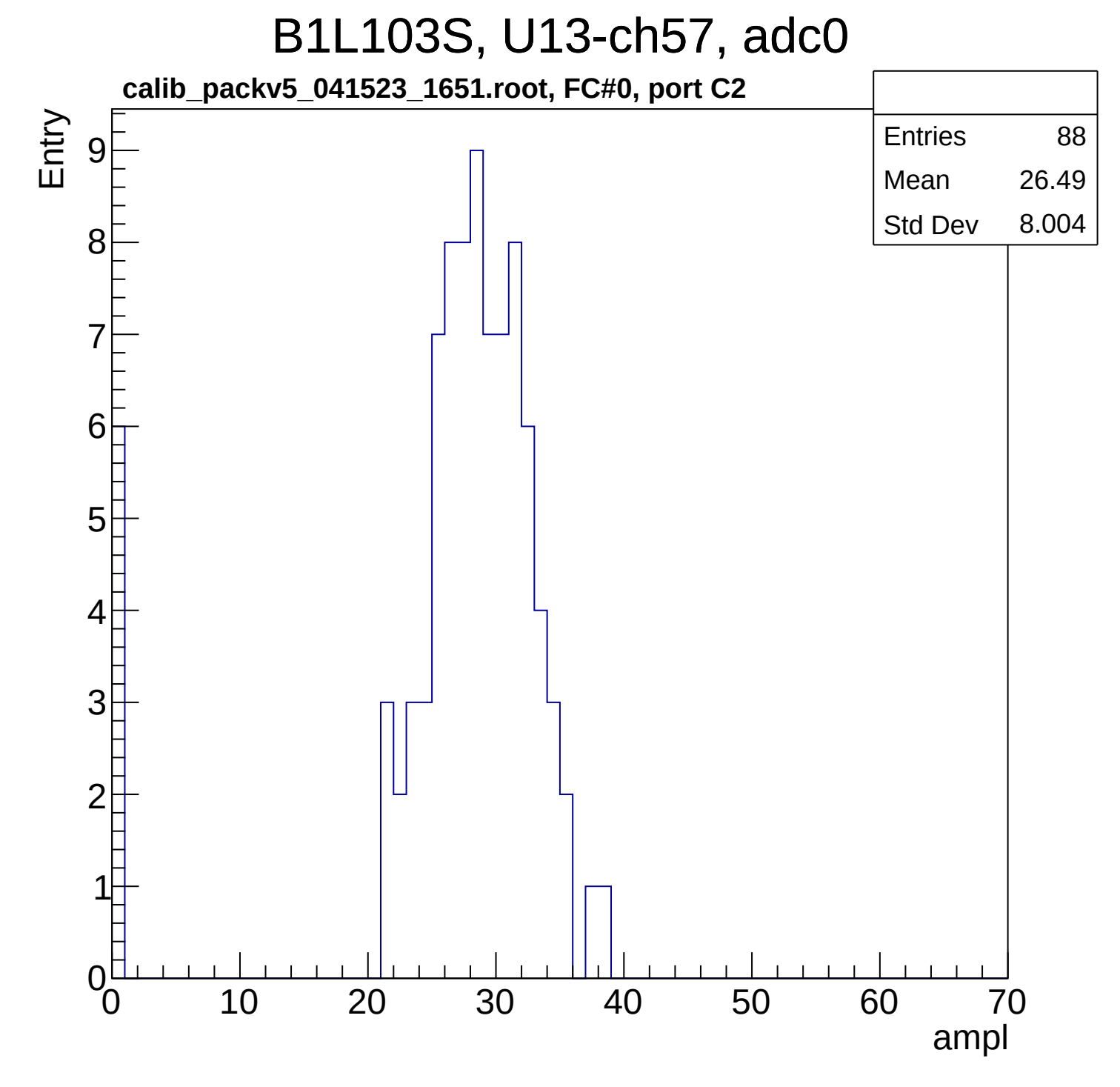
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U13-ch56, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch57, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 26.49
Std Dev 8.004
Entry
ampl
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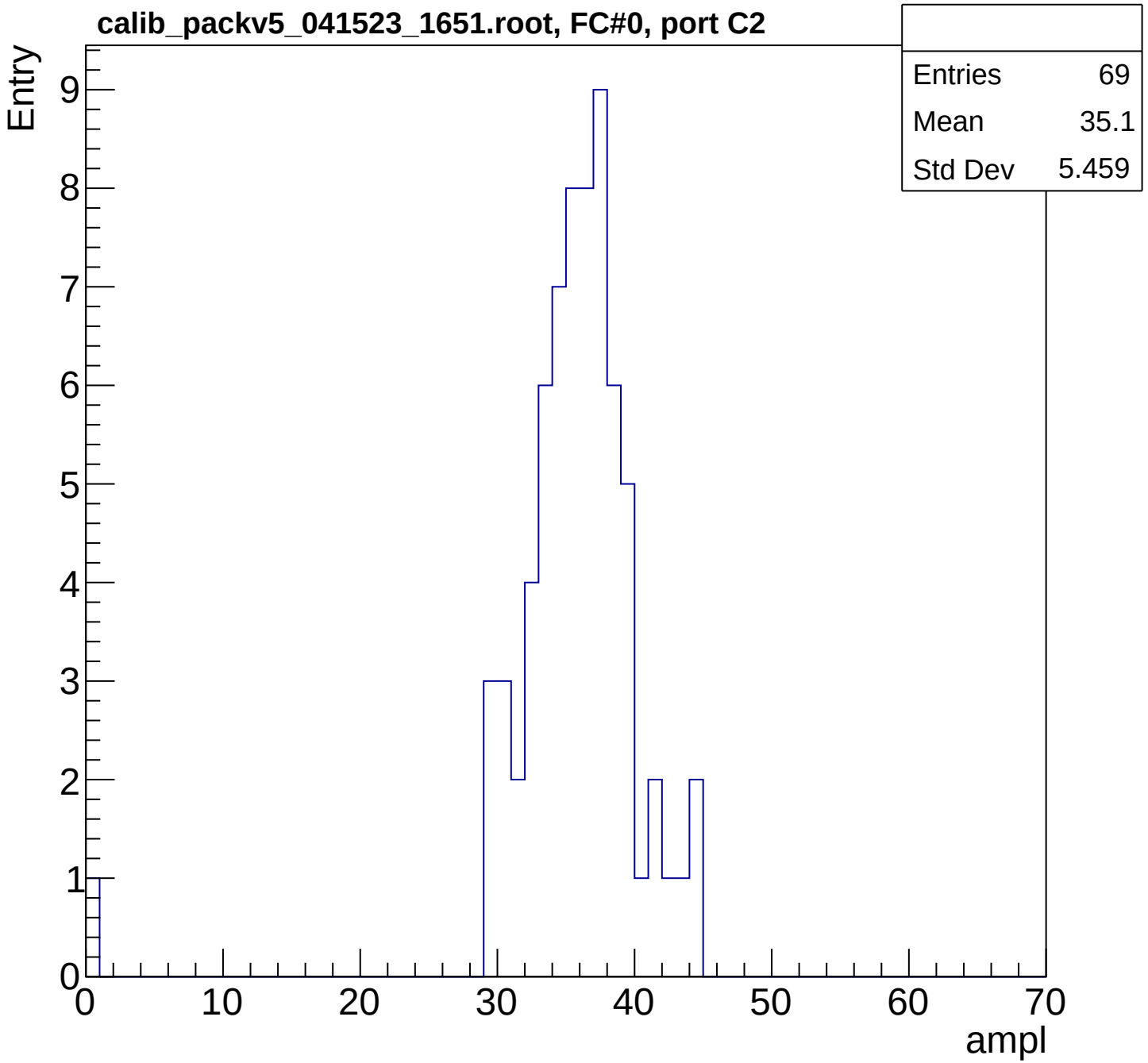
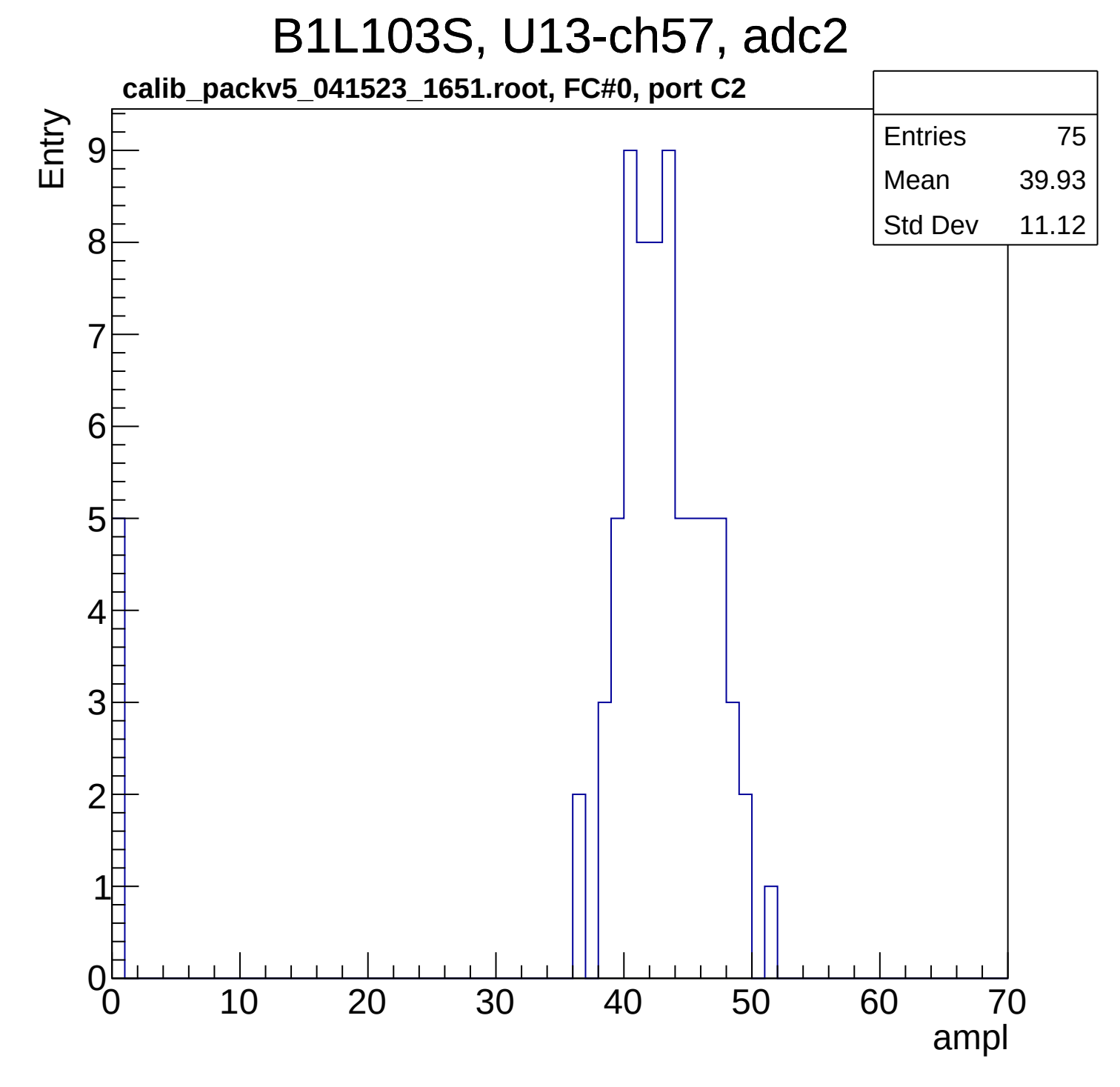
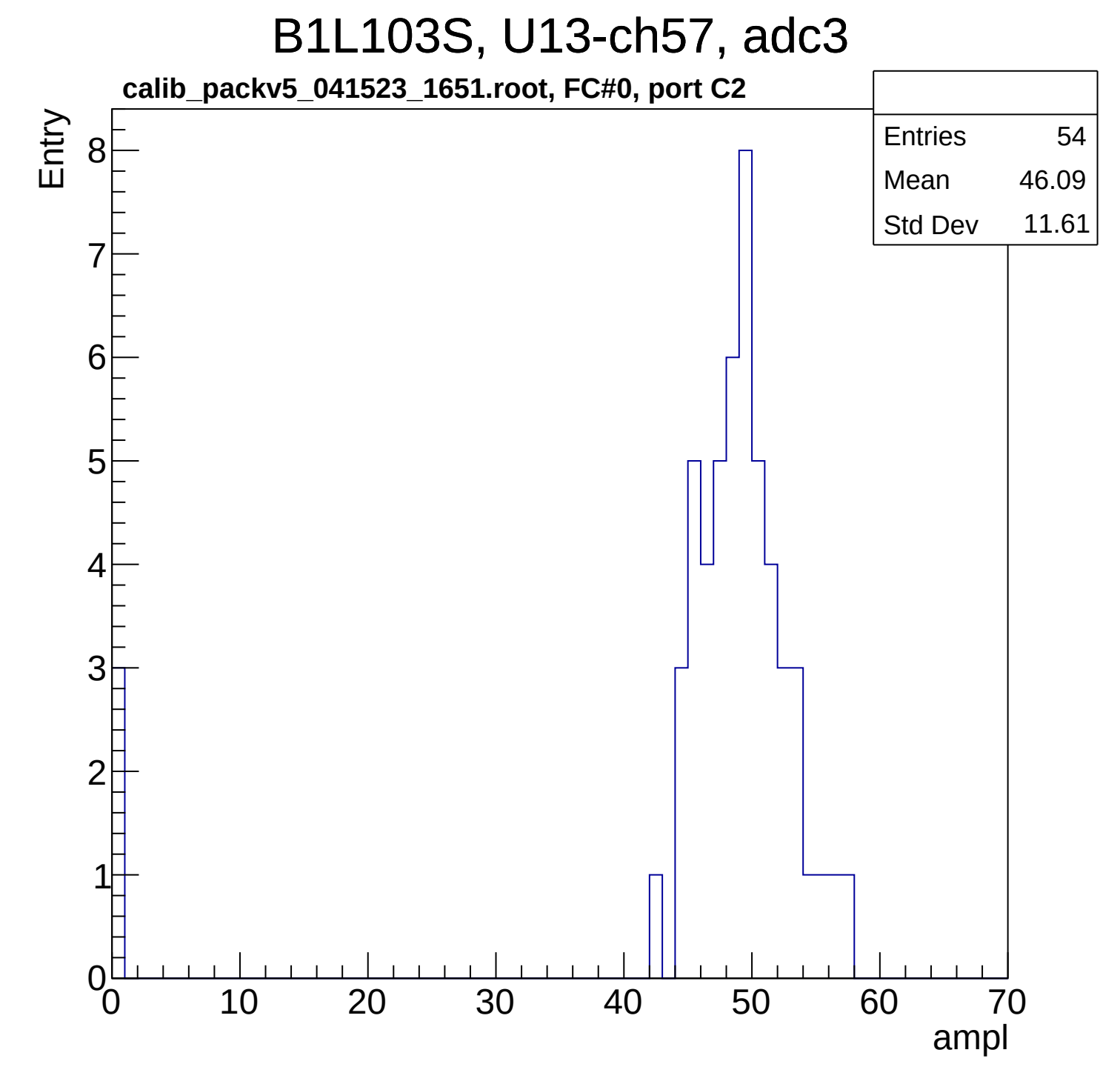
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch57, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 35.1
Std Dev 5.459
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch57, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 39.93
Std Dev 11.12
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch57, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 46.09
Std Dev 11.61
Entry
ampl
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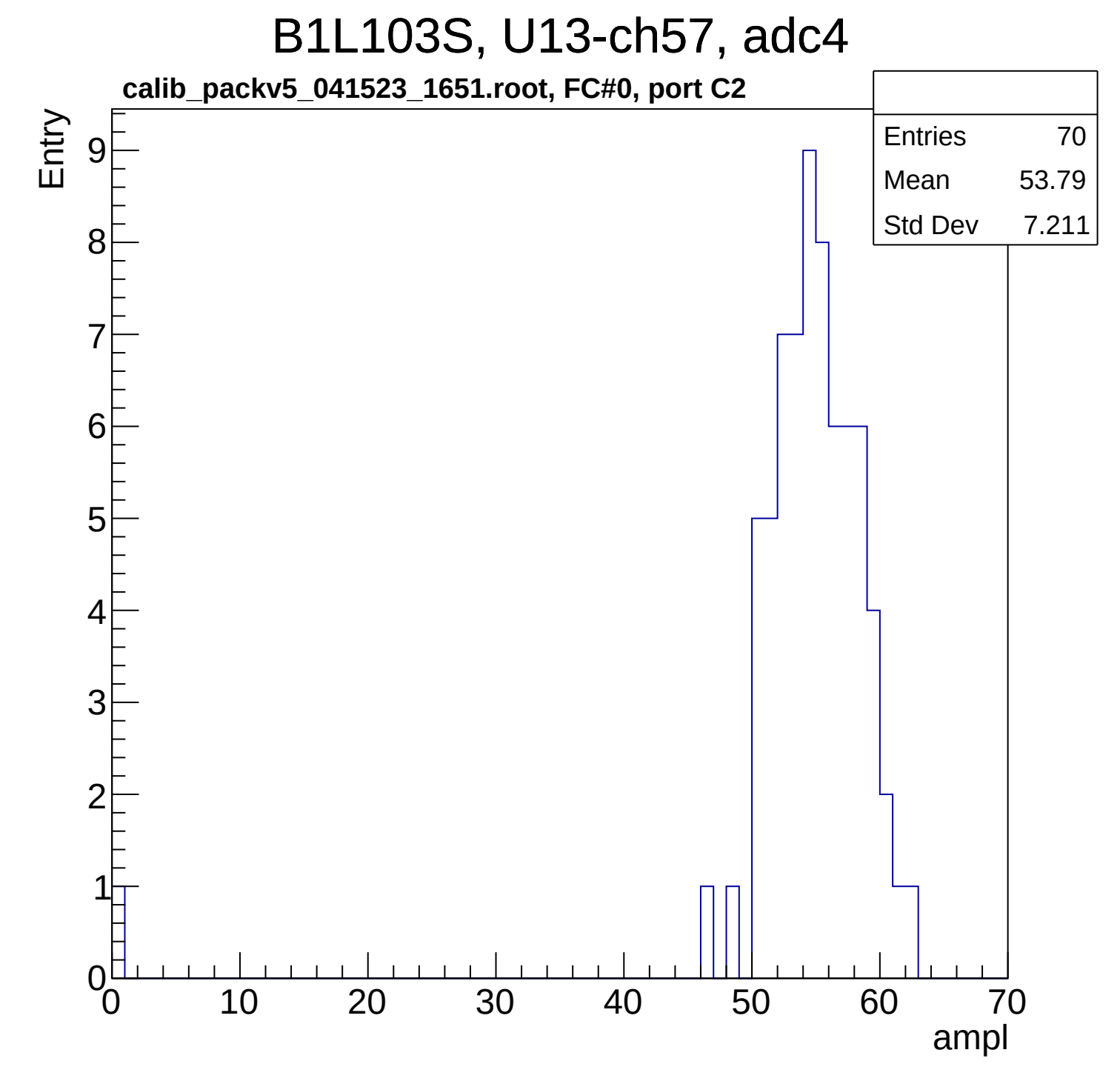
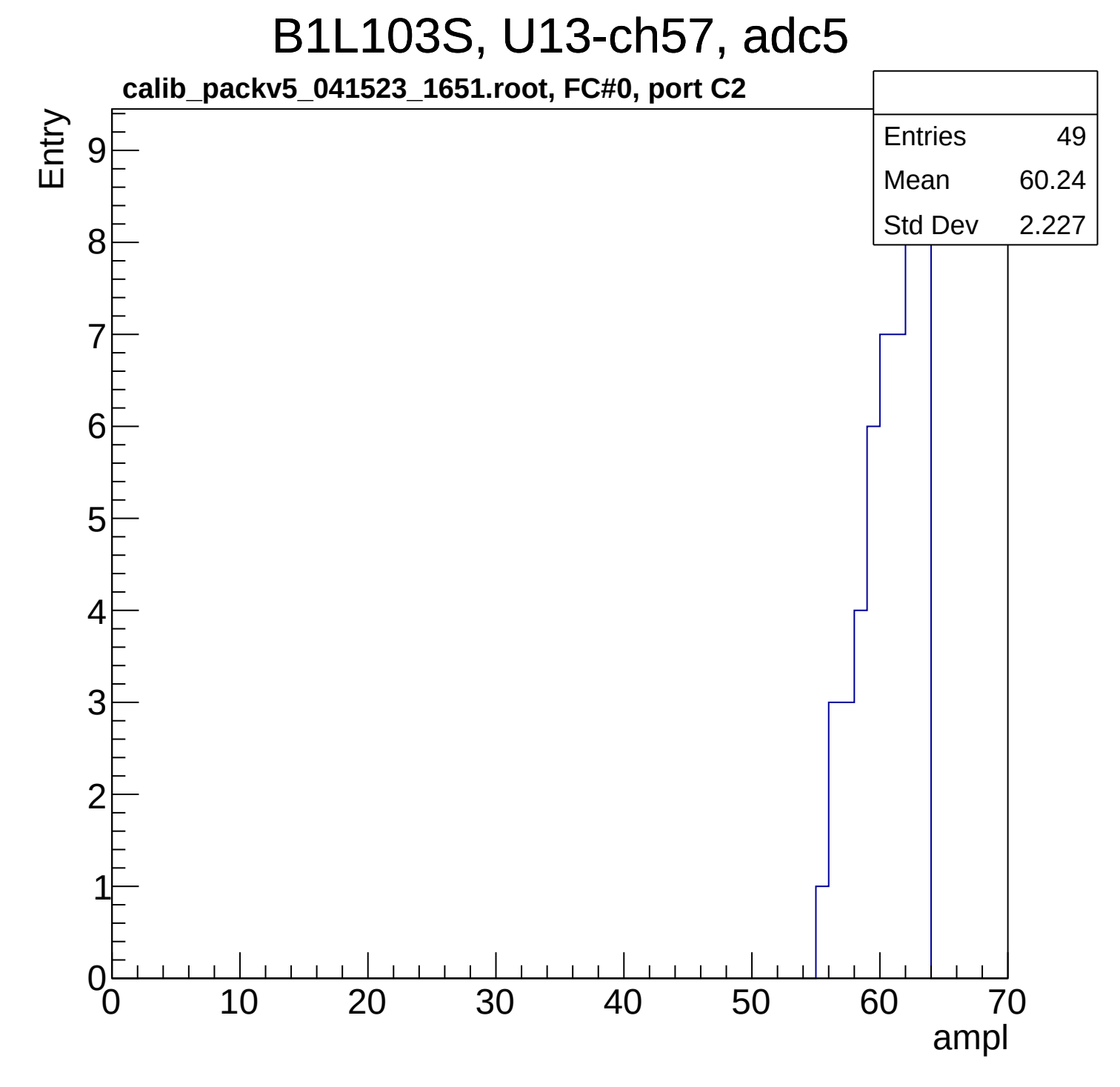
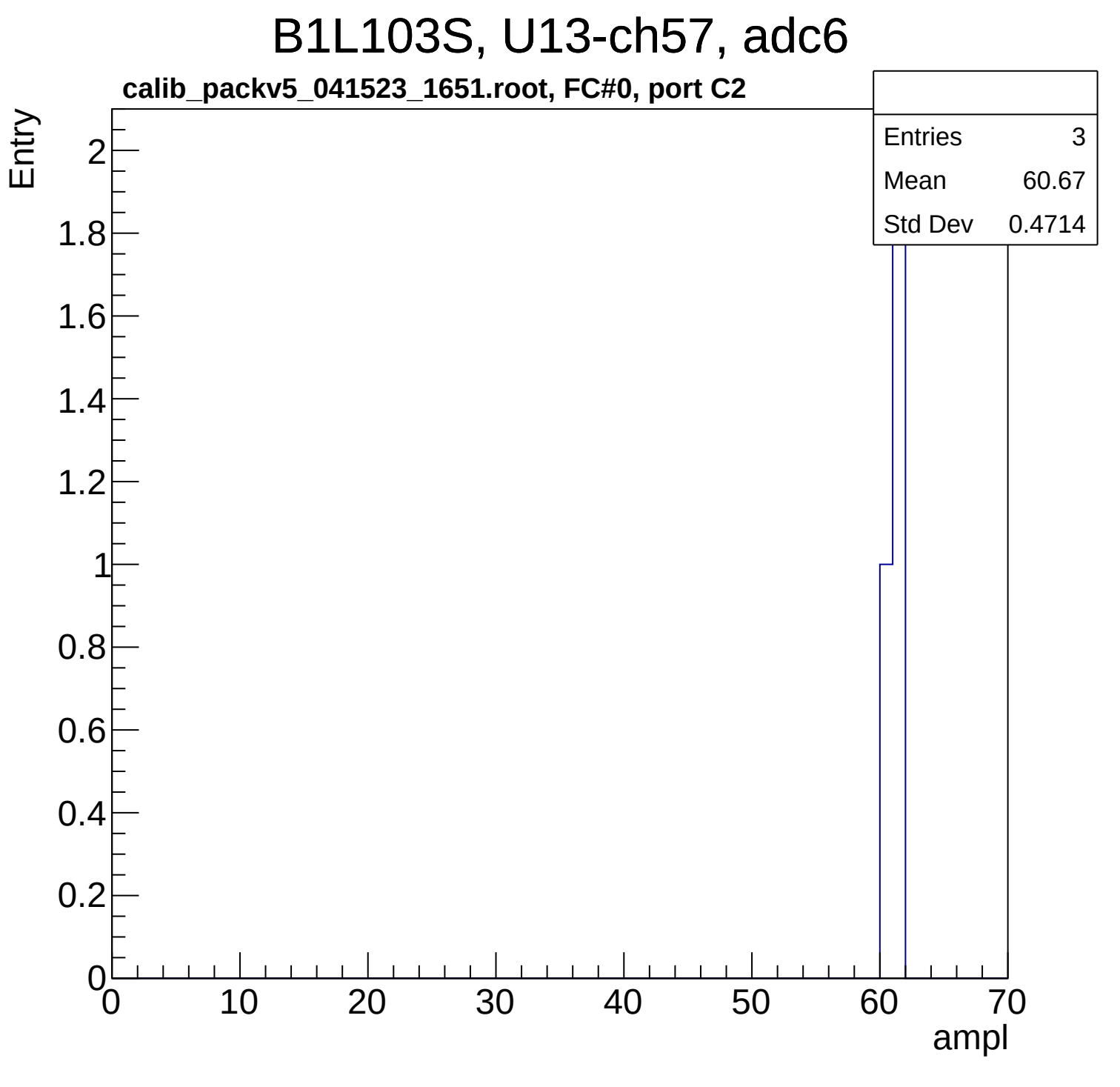
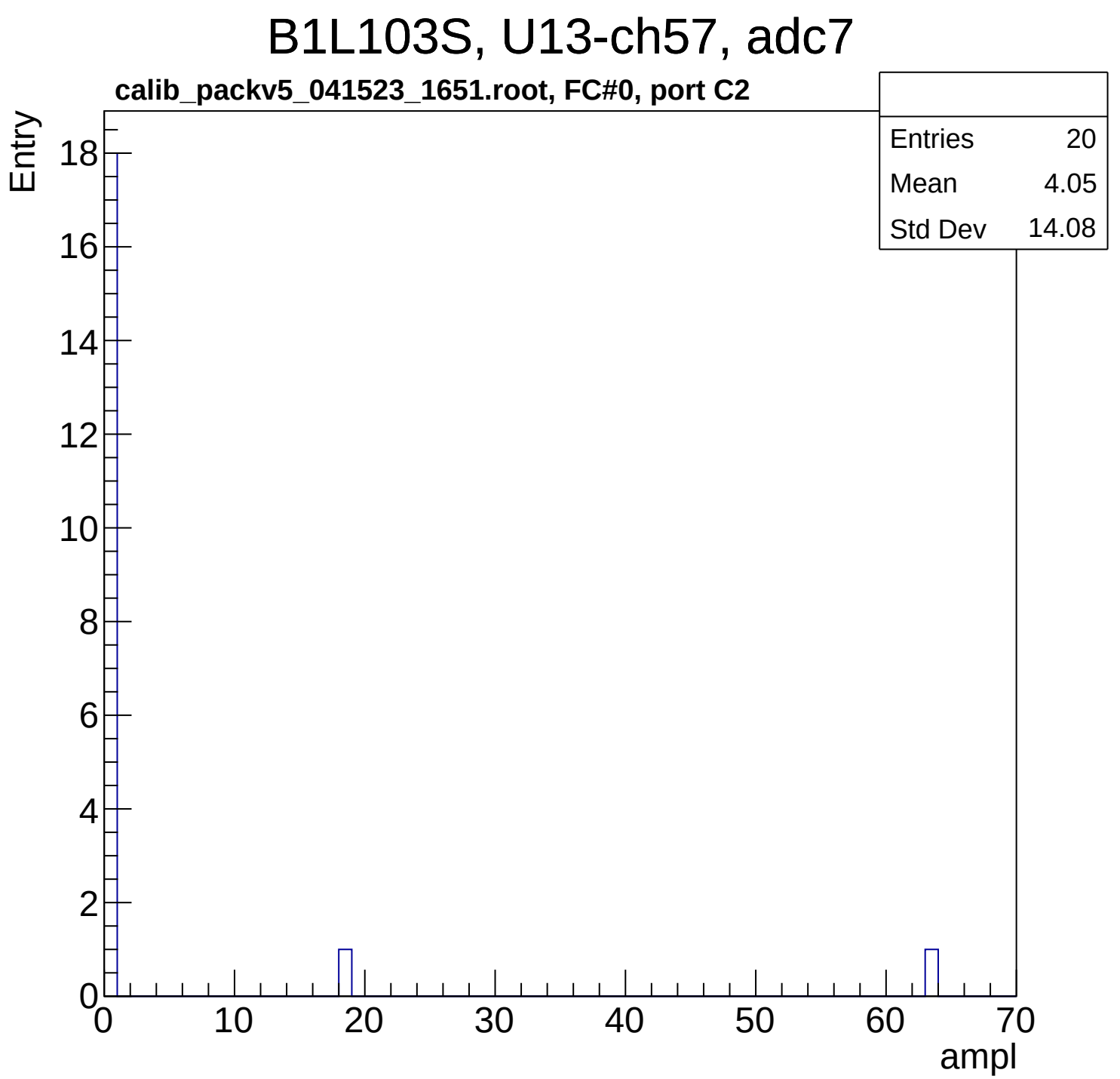
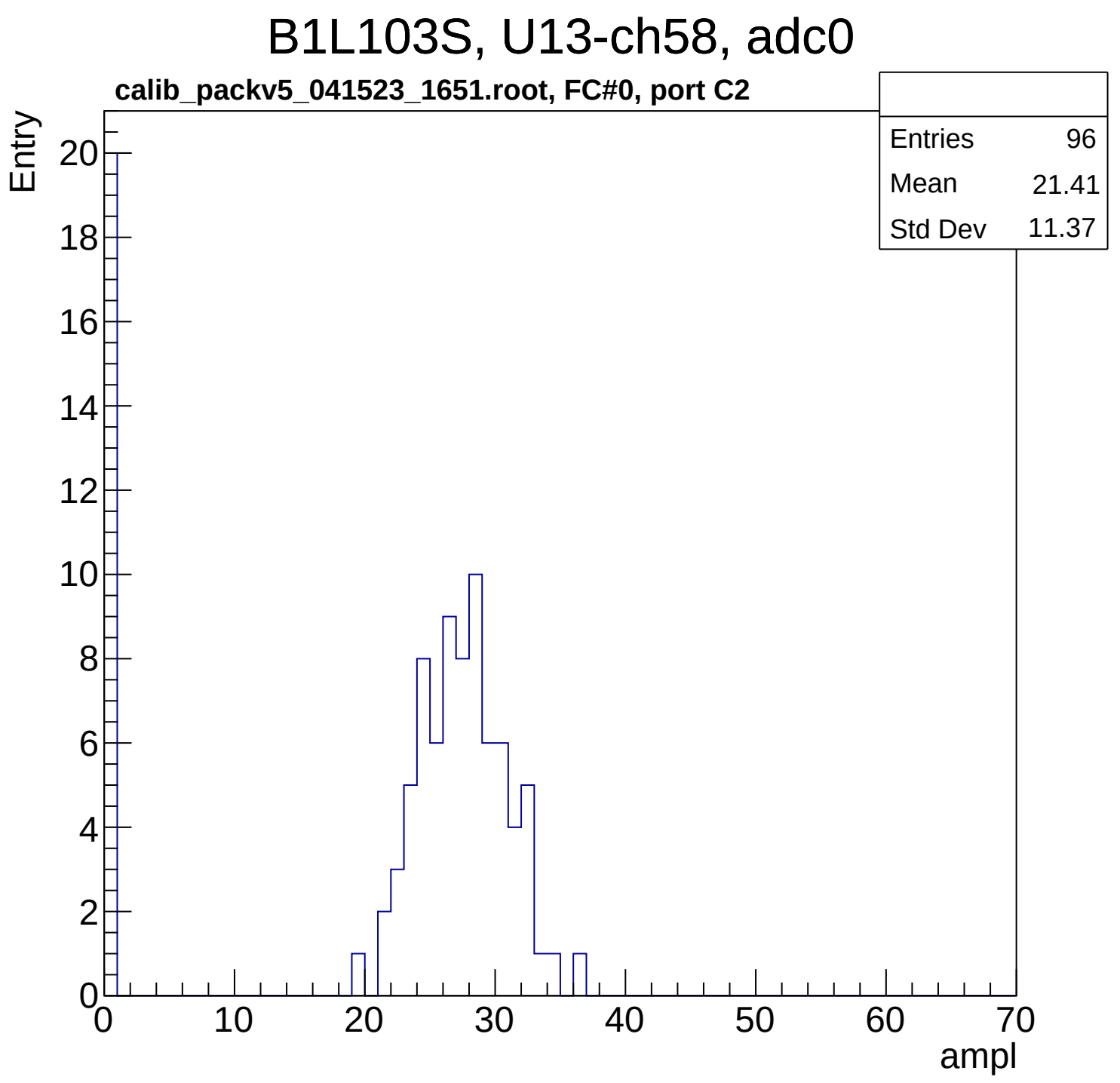
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

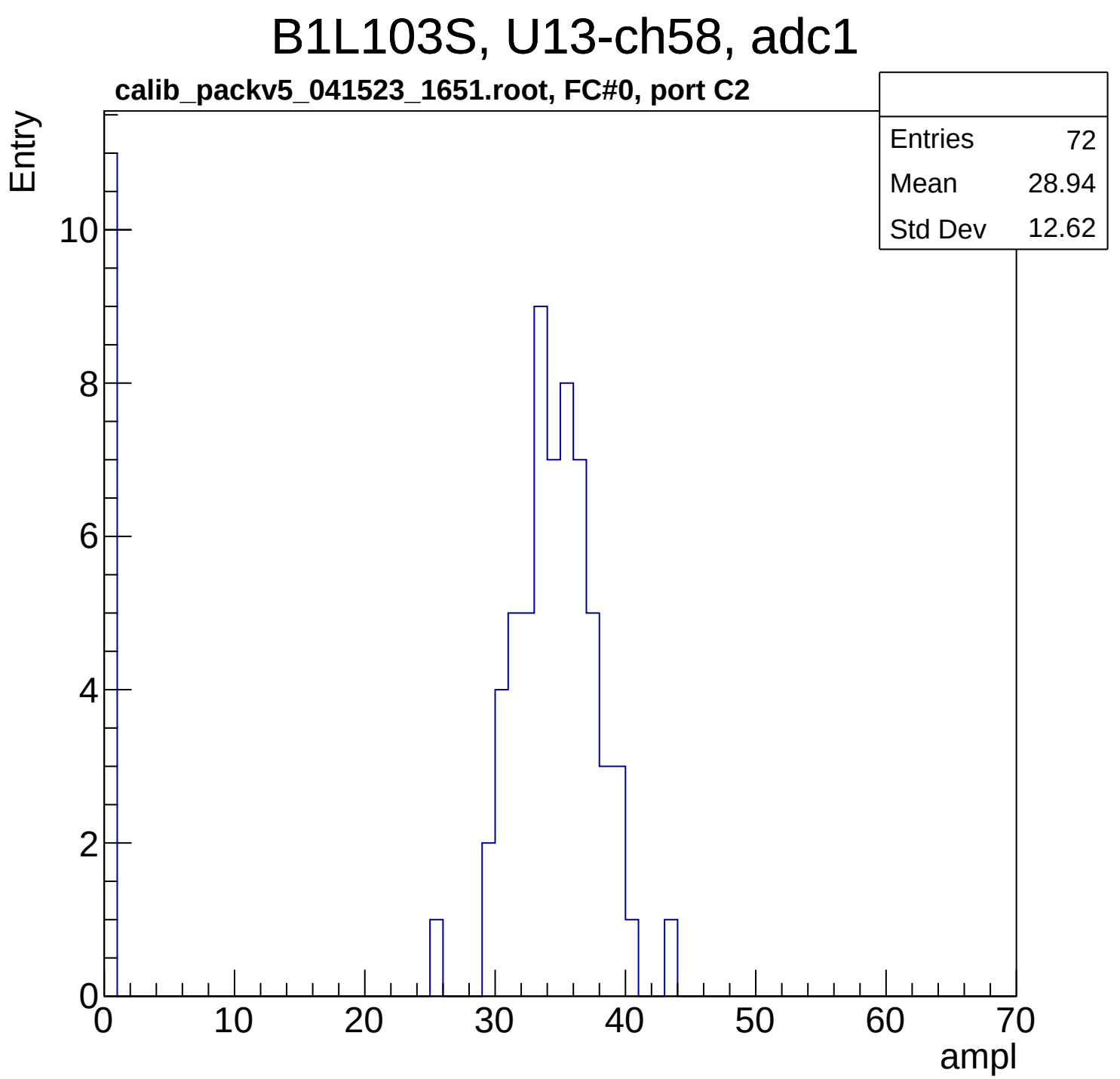

B1L103S, U13-ch57, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 53.79
Std Dev 7.211
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch57, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 60.24
Std Dev 2.227
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch57, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 60.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U13-ch57, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.05
Std Dev 14.08
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch58, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 21.41
Std Dev 11.37
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch58, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 28.94
Std Dev 12.62
Entry
0
2
4
6
8
10
0
10
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50
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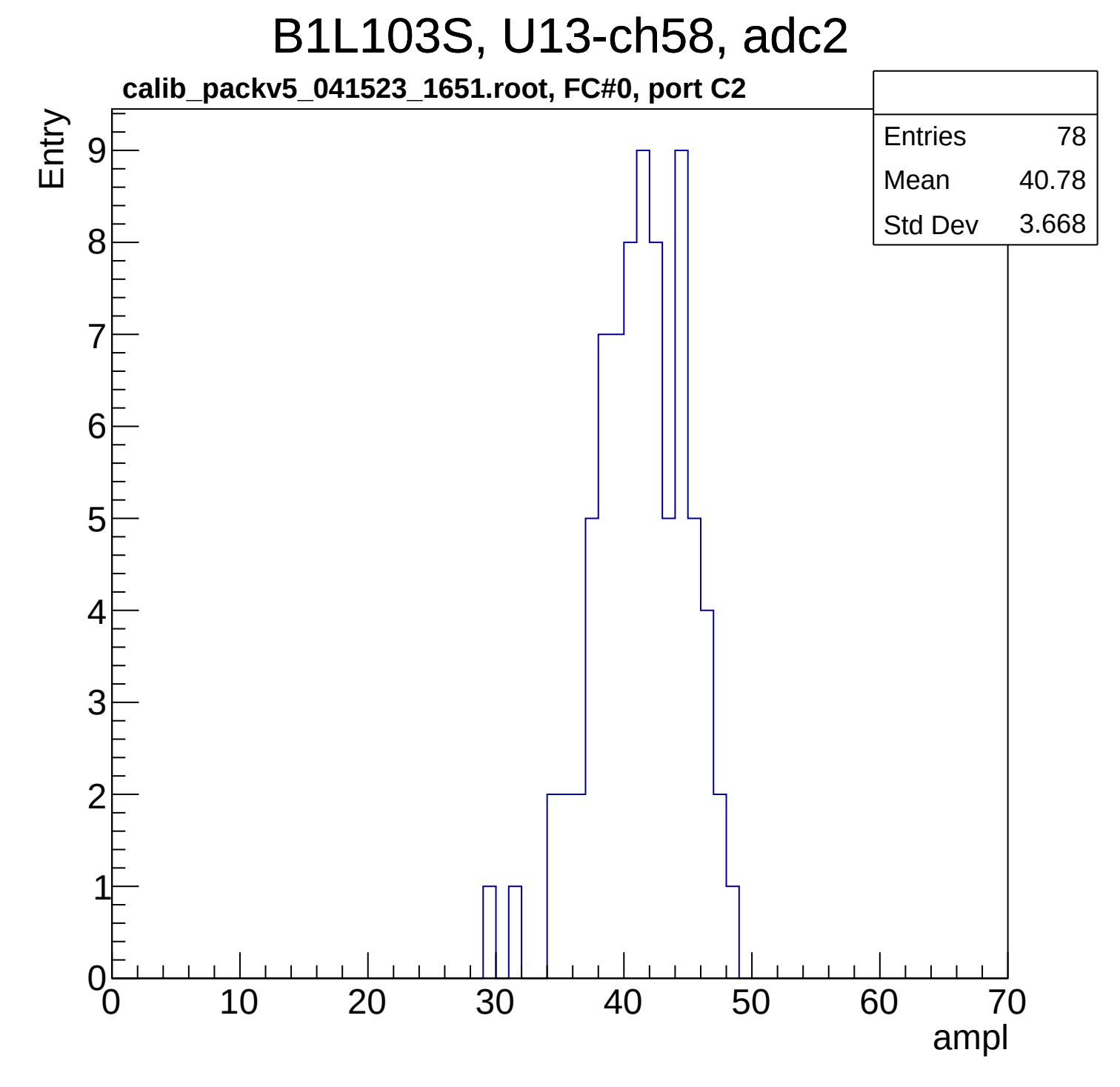
70
ampl


B1L103S, U13-ch58, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 40.78
Std Dev 3.668
Entry
ampl
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2
3
4
5
6
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8
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0
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40
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60
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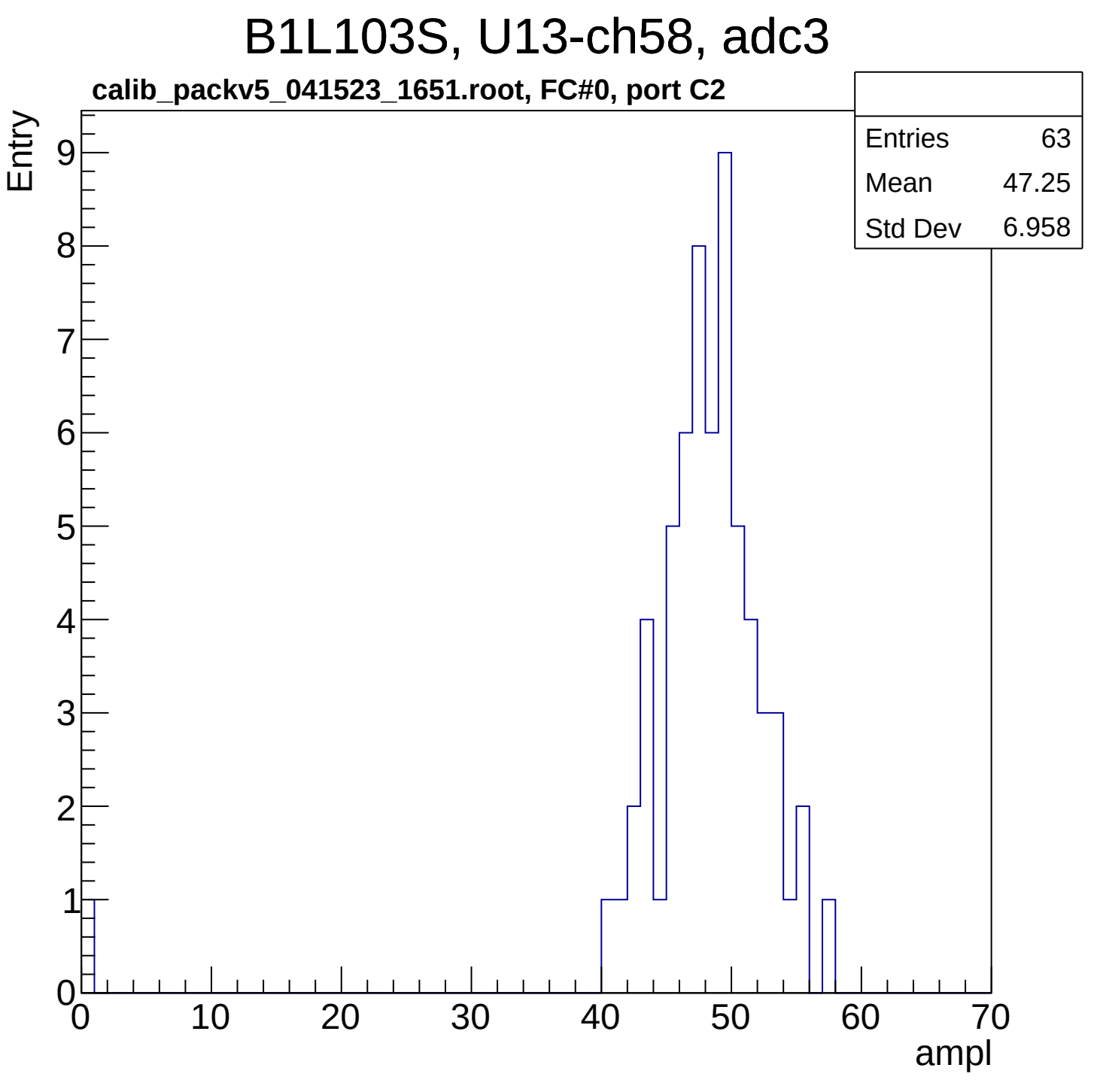
B1L103S, U13-ch58, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 47.25
Std Dev 6.958
Entry
ampl
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2
3
4
5
6
7
8
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0
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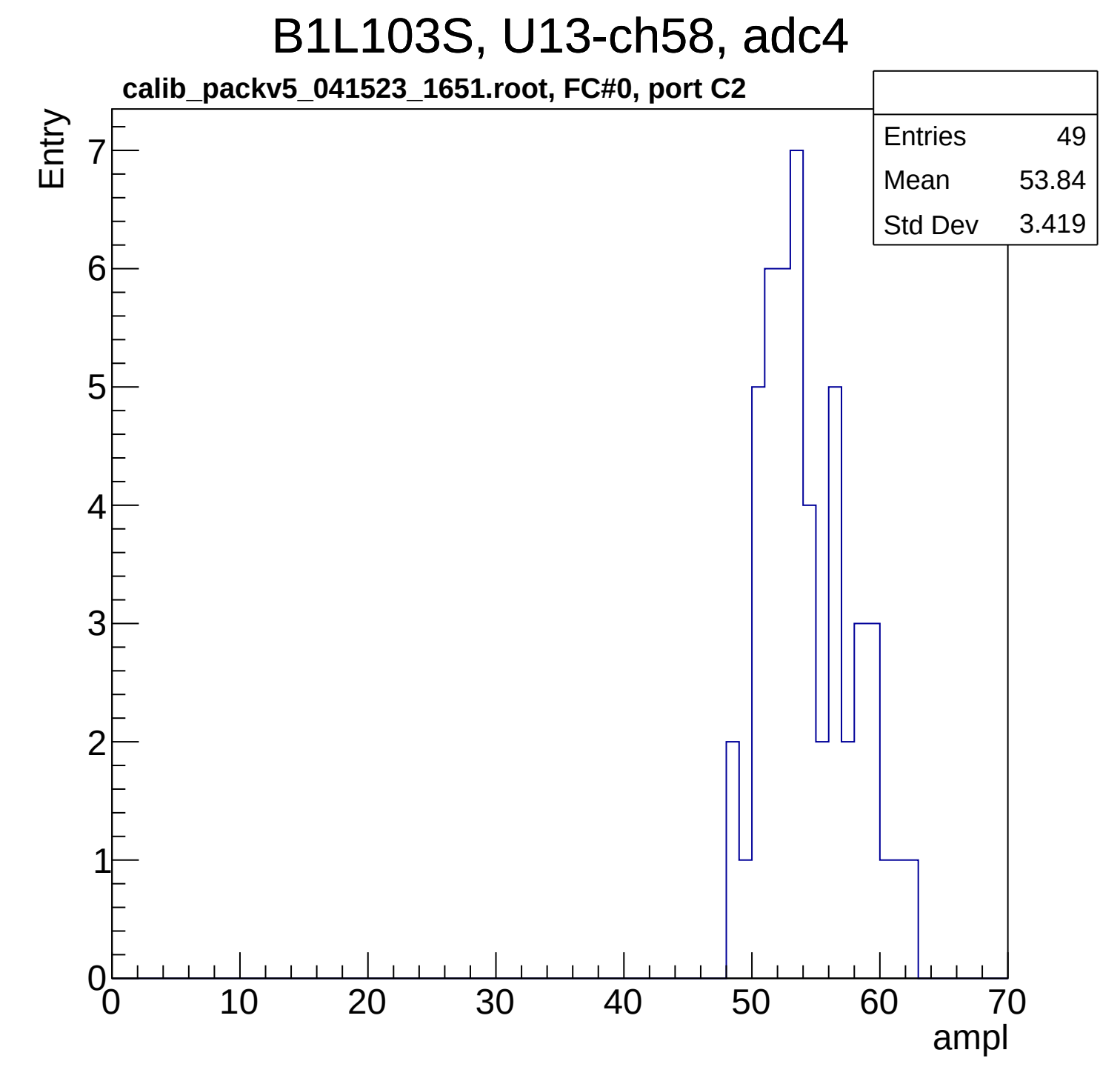
B1L103S, U13-ch58, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 53.84
Std Dev 3.419
Entry
ampl
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4
5
6
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0
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40
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60
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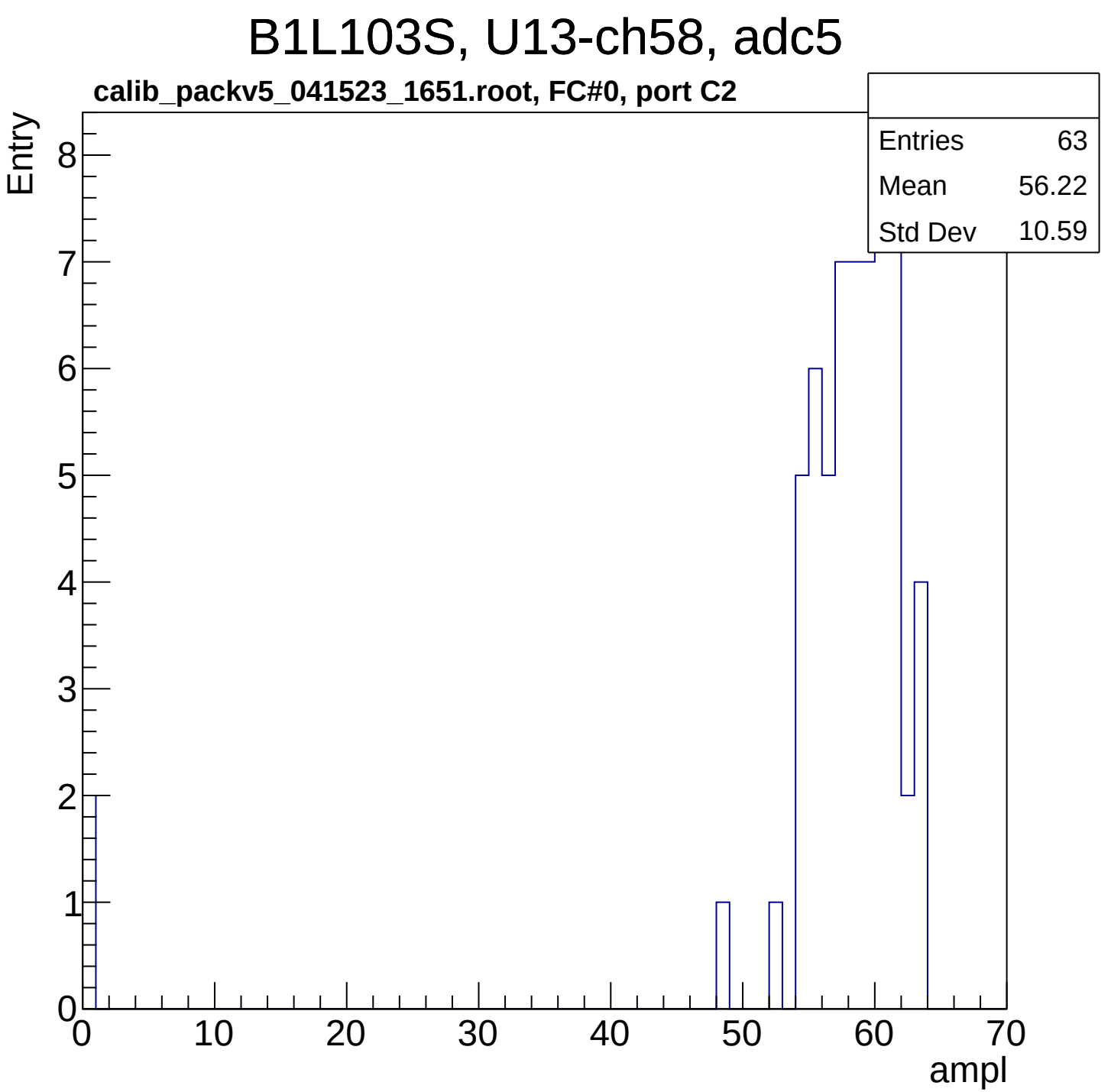
B1L103S, U13-ch58, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 56.22
Std Dev 10.59
Entry
ampl
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1
2
3
4
5
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7
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0
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40
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60
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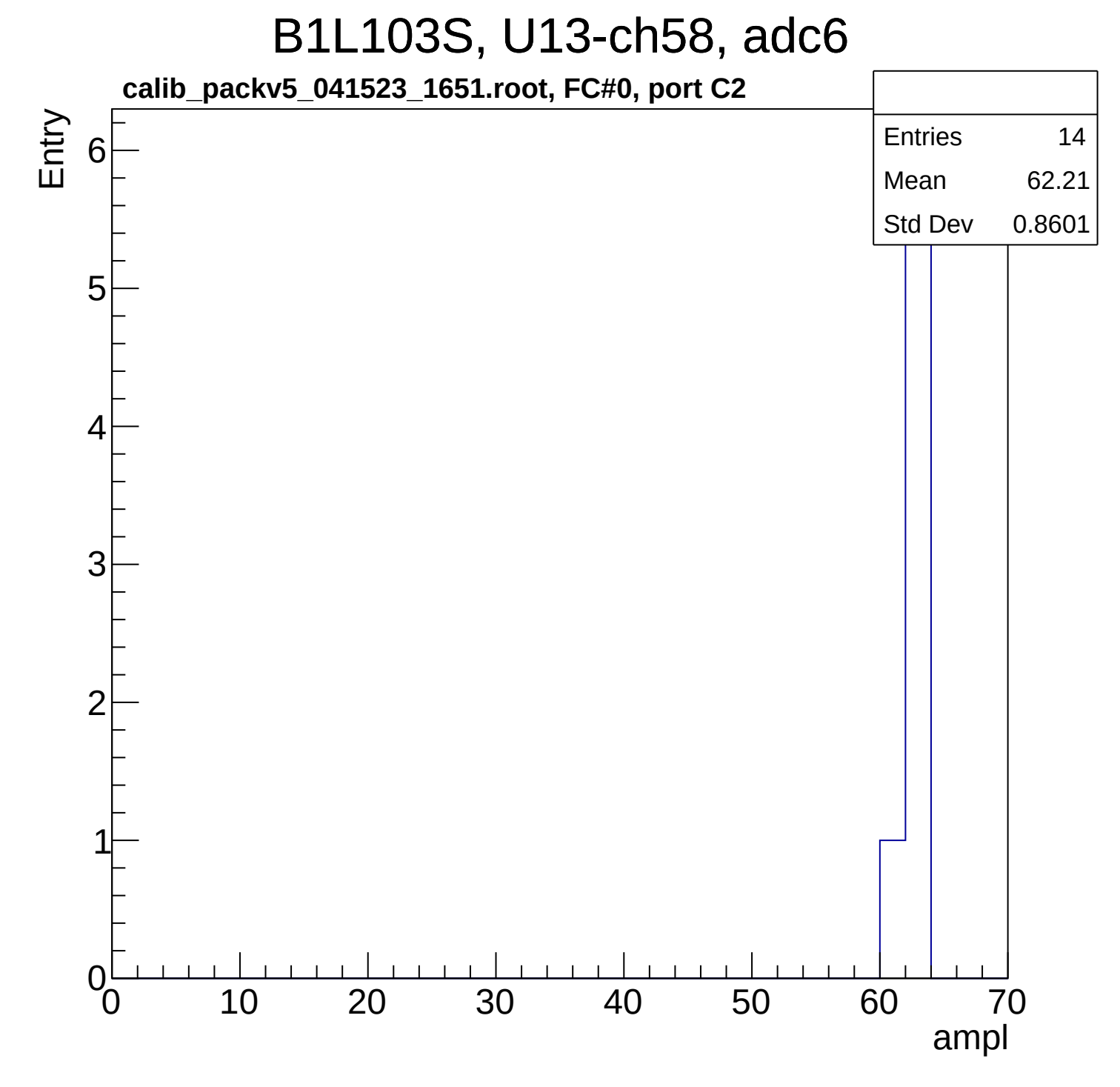
B1L103S, U13-ch58, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 62.21
Std Dev 0.8601
Entry
0
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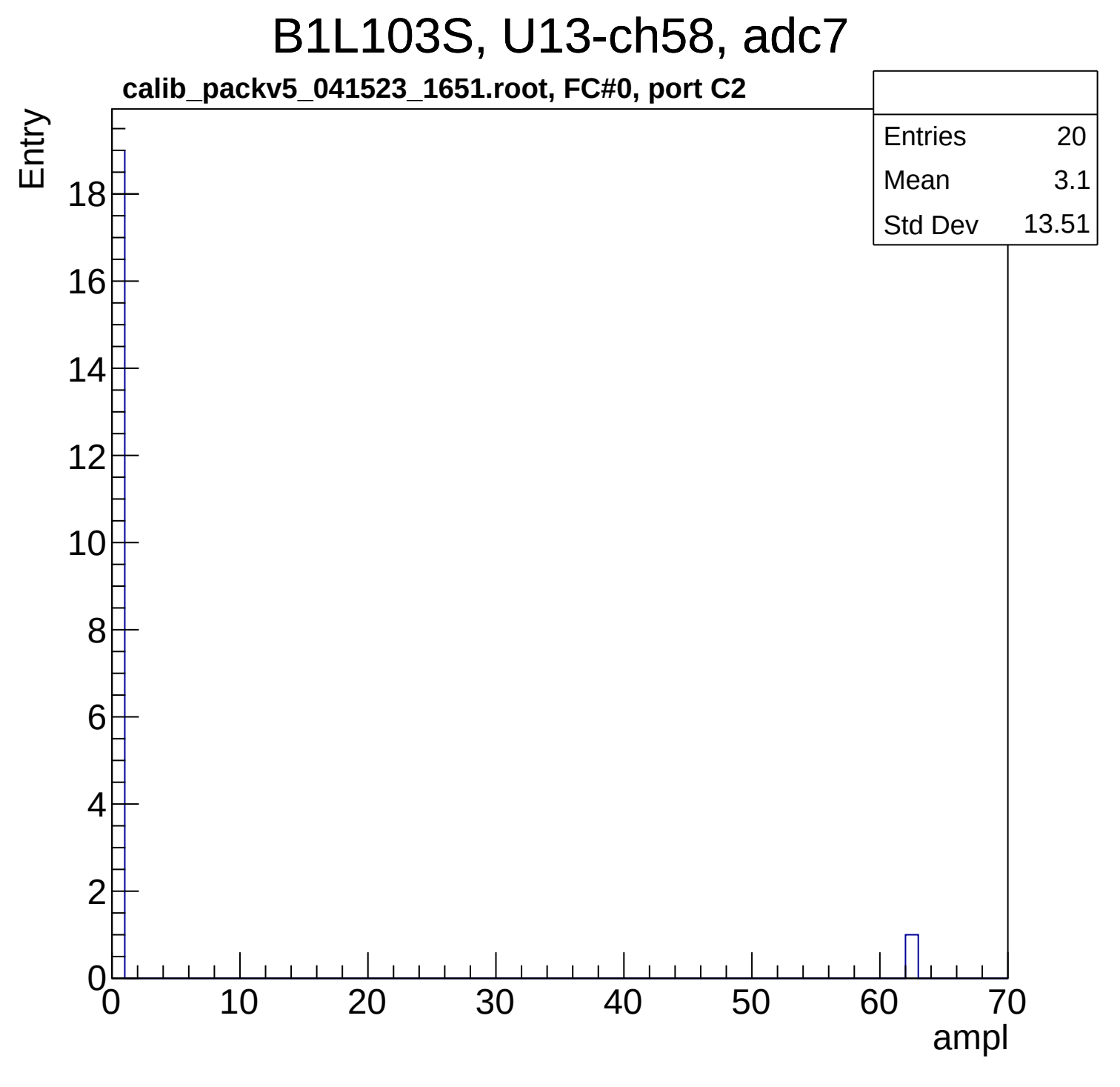
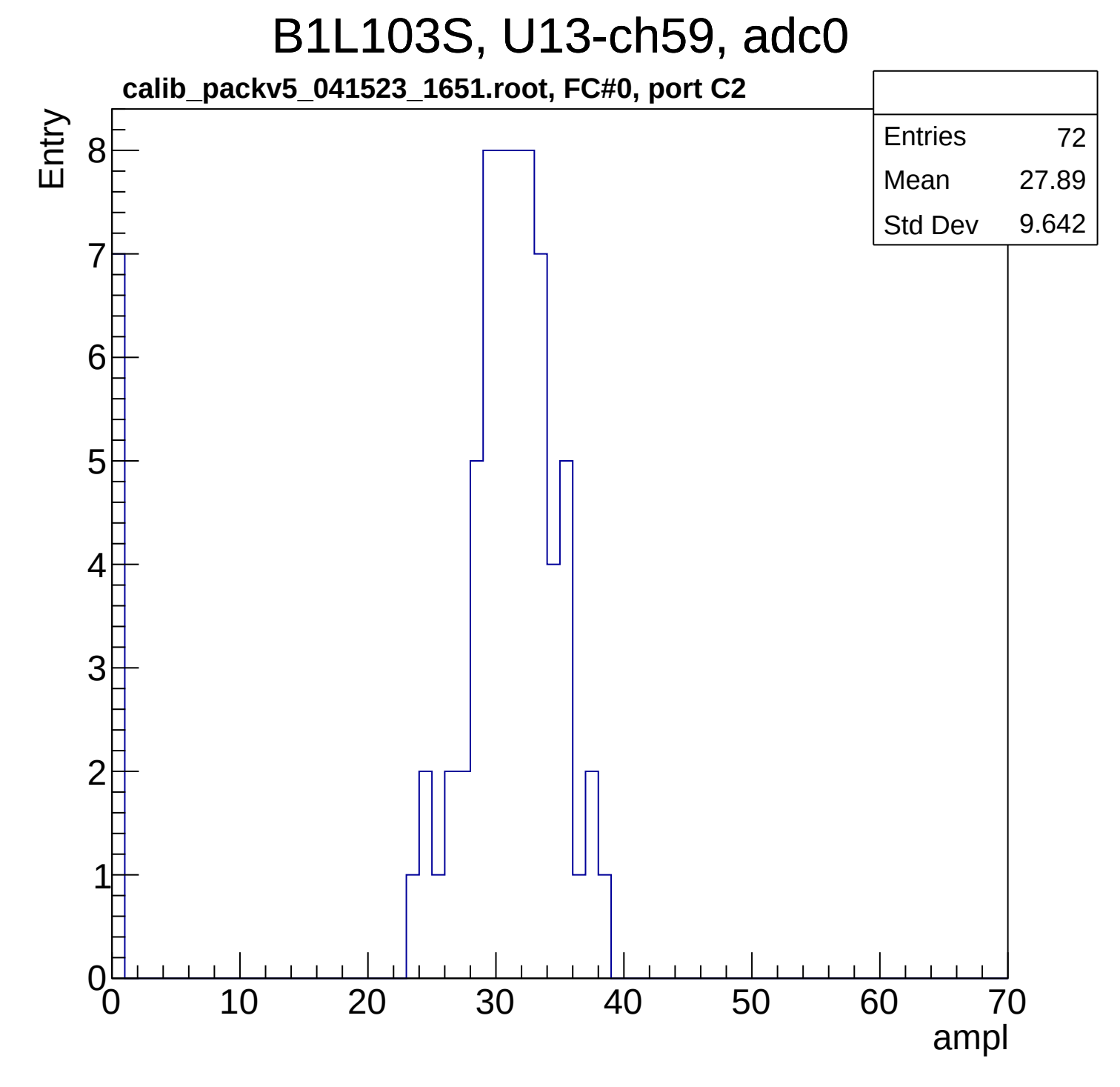
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch58, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch59, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 27.89
Std Dev 9.642
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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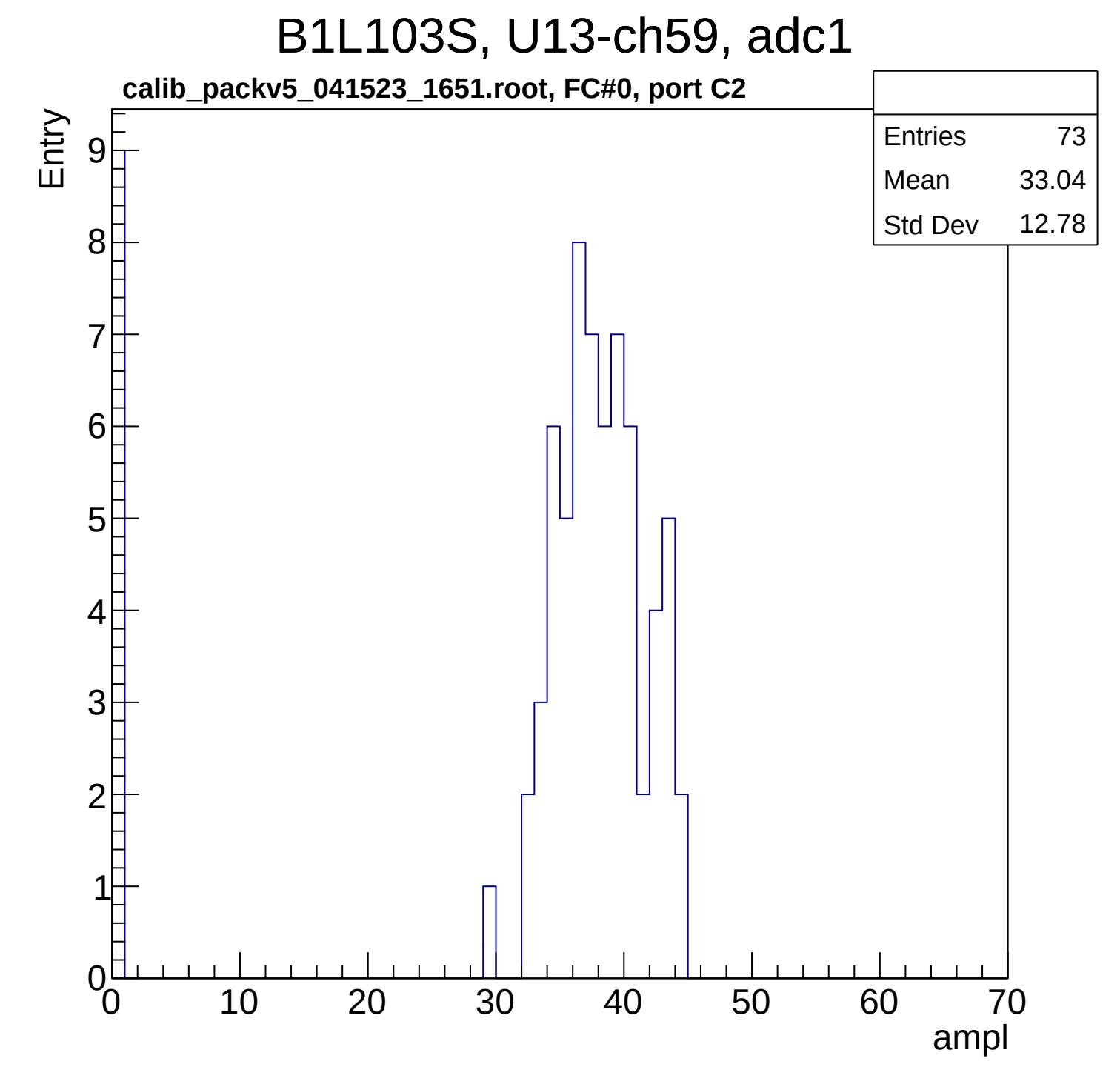
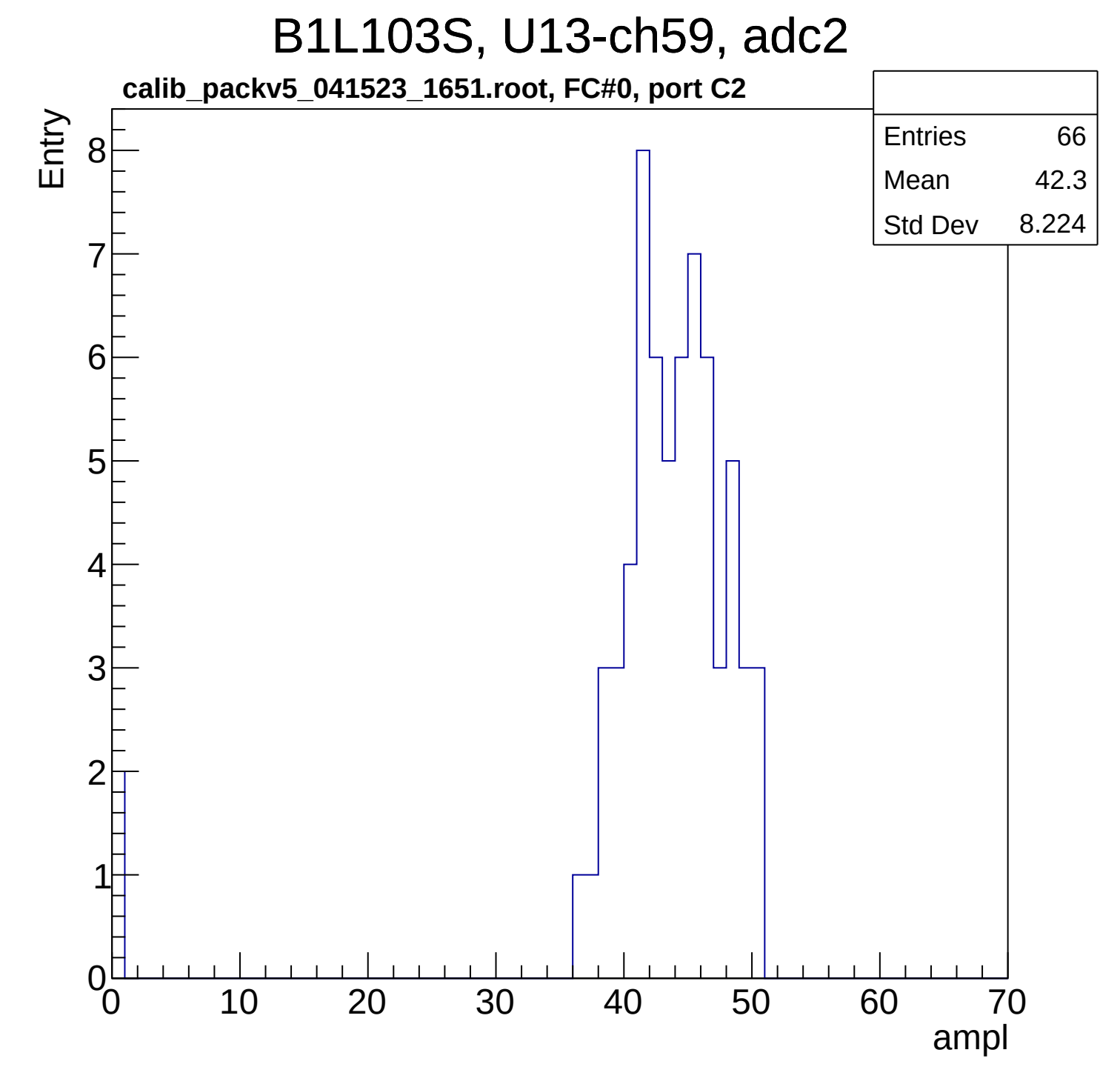
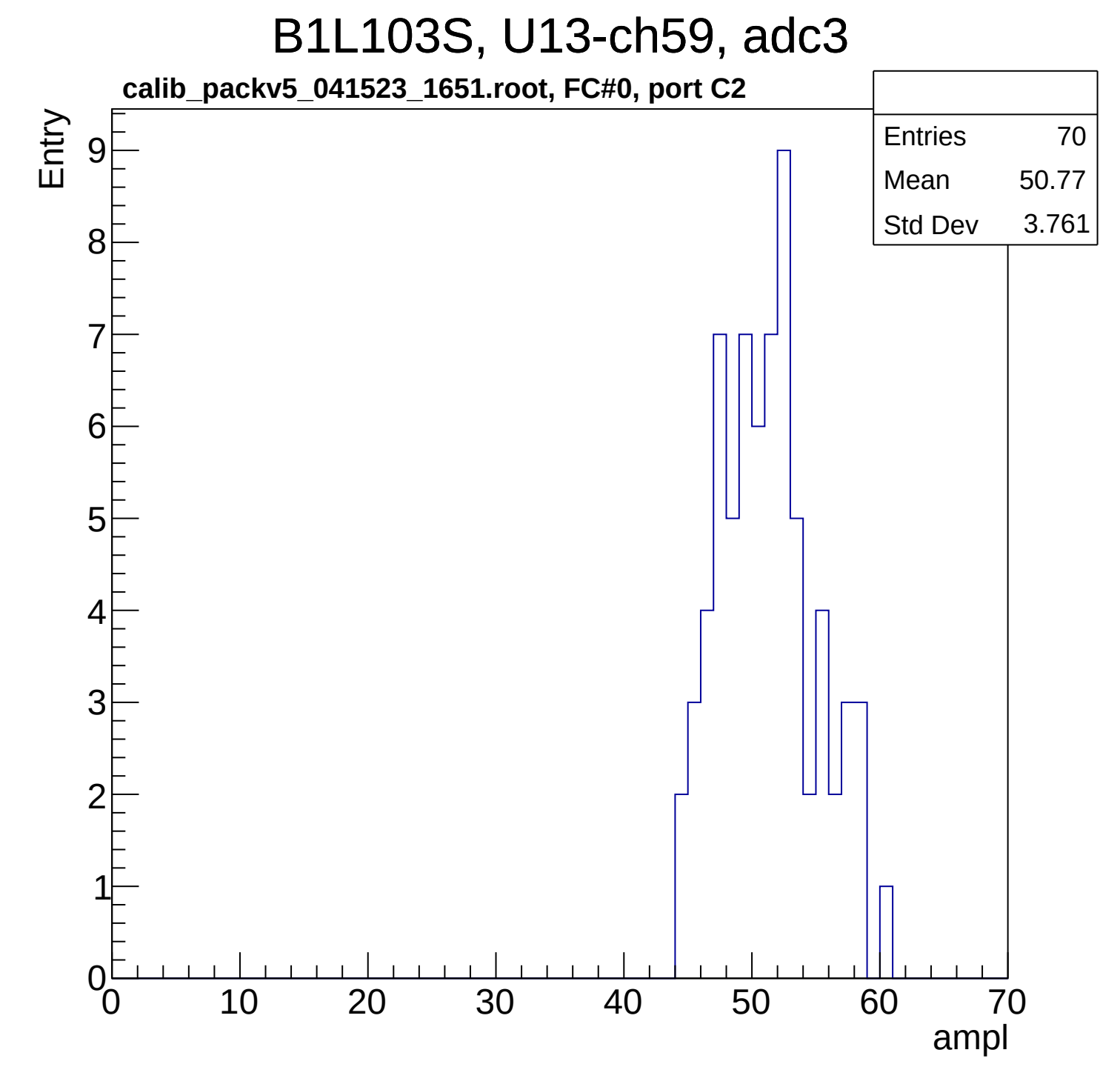

B1L103S, U13-ch59, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 33.04
Std Dev 12.78
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch59, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 42.3
Std Dev 8.224
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch59, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 50.77
Std Dev 3.761
Entry
ampl
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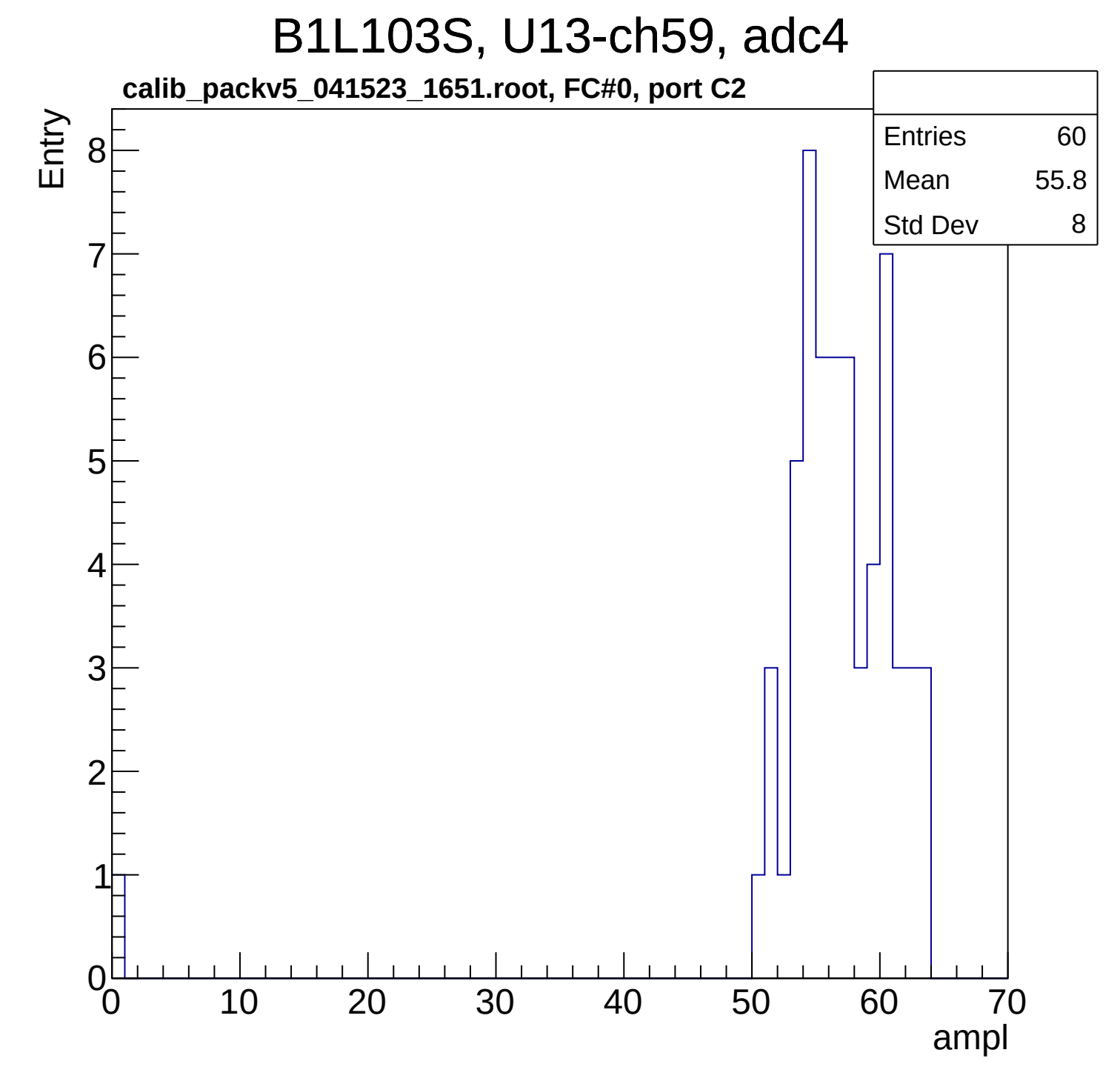
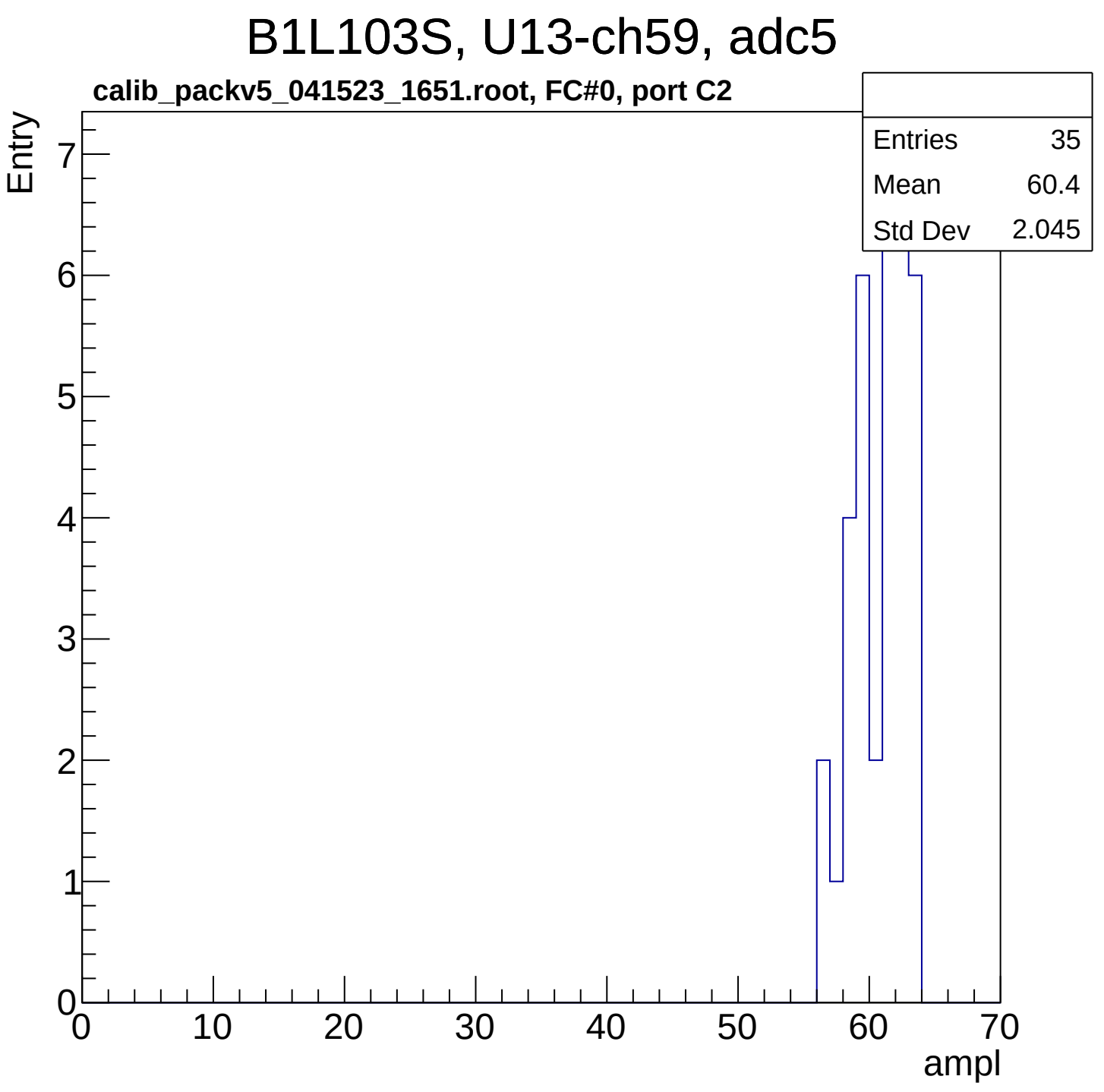
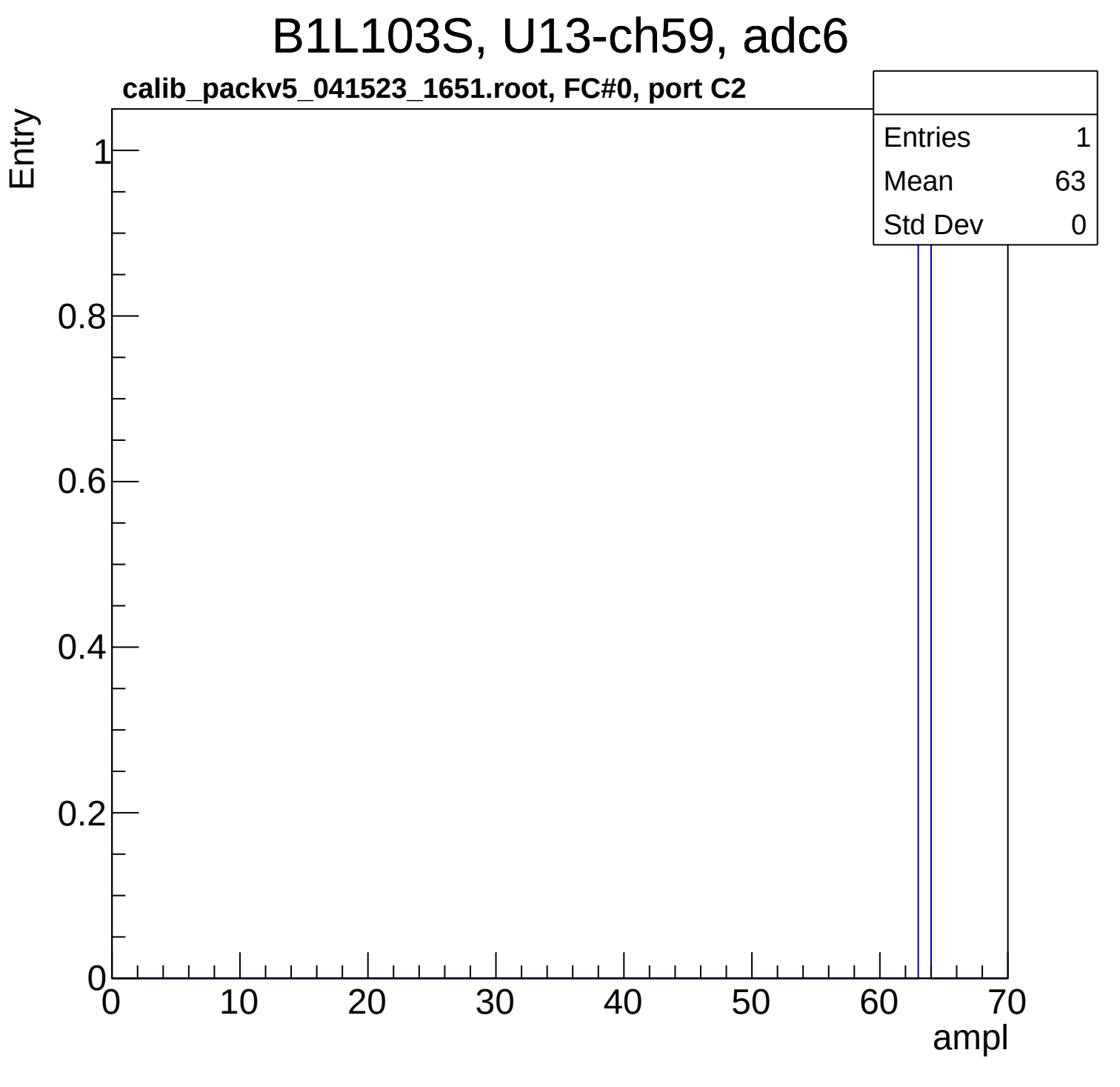
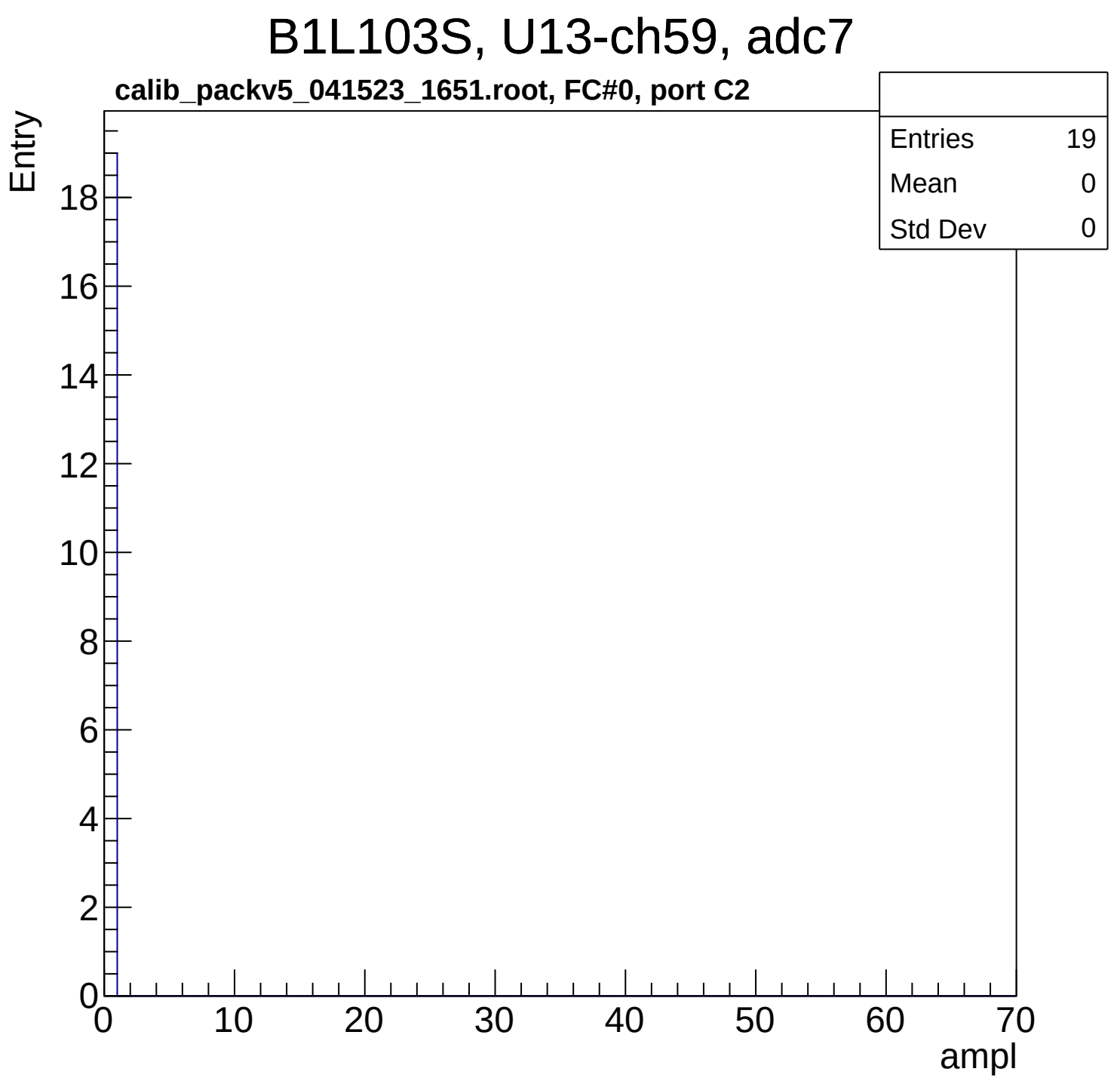
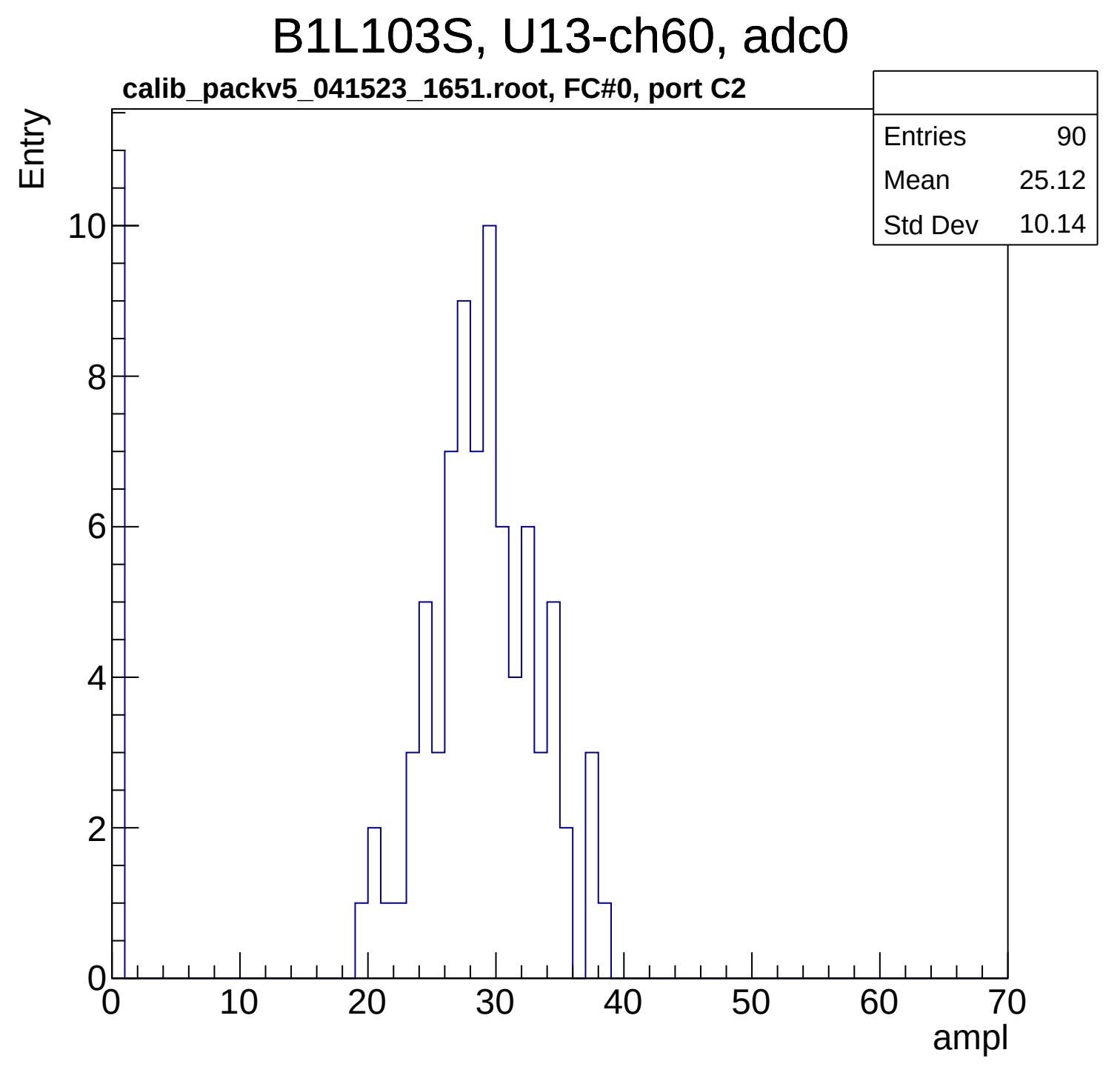
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

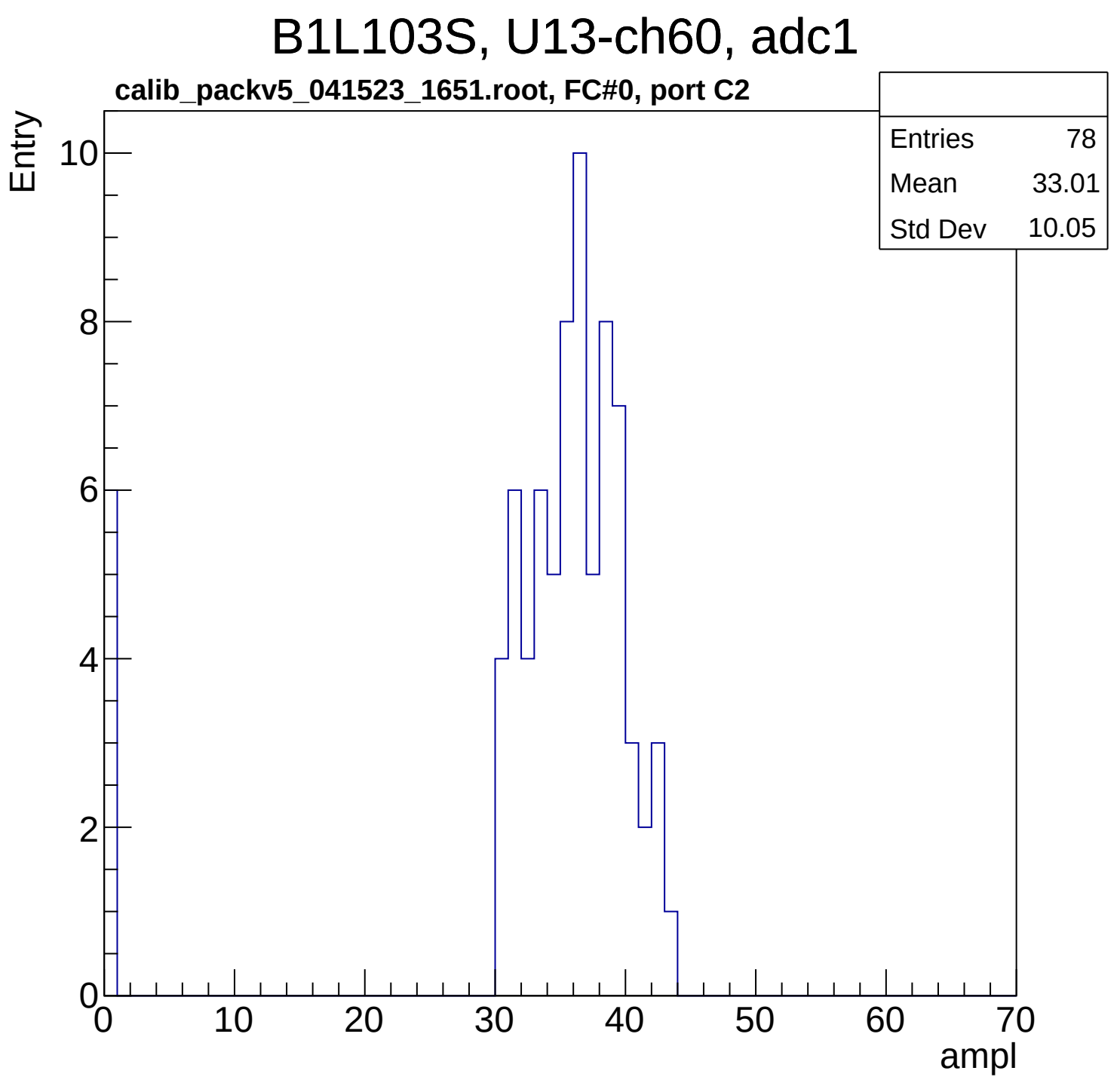

B1L103S, U13-ch59, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 55.8
Std Dev 8
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

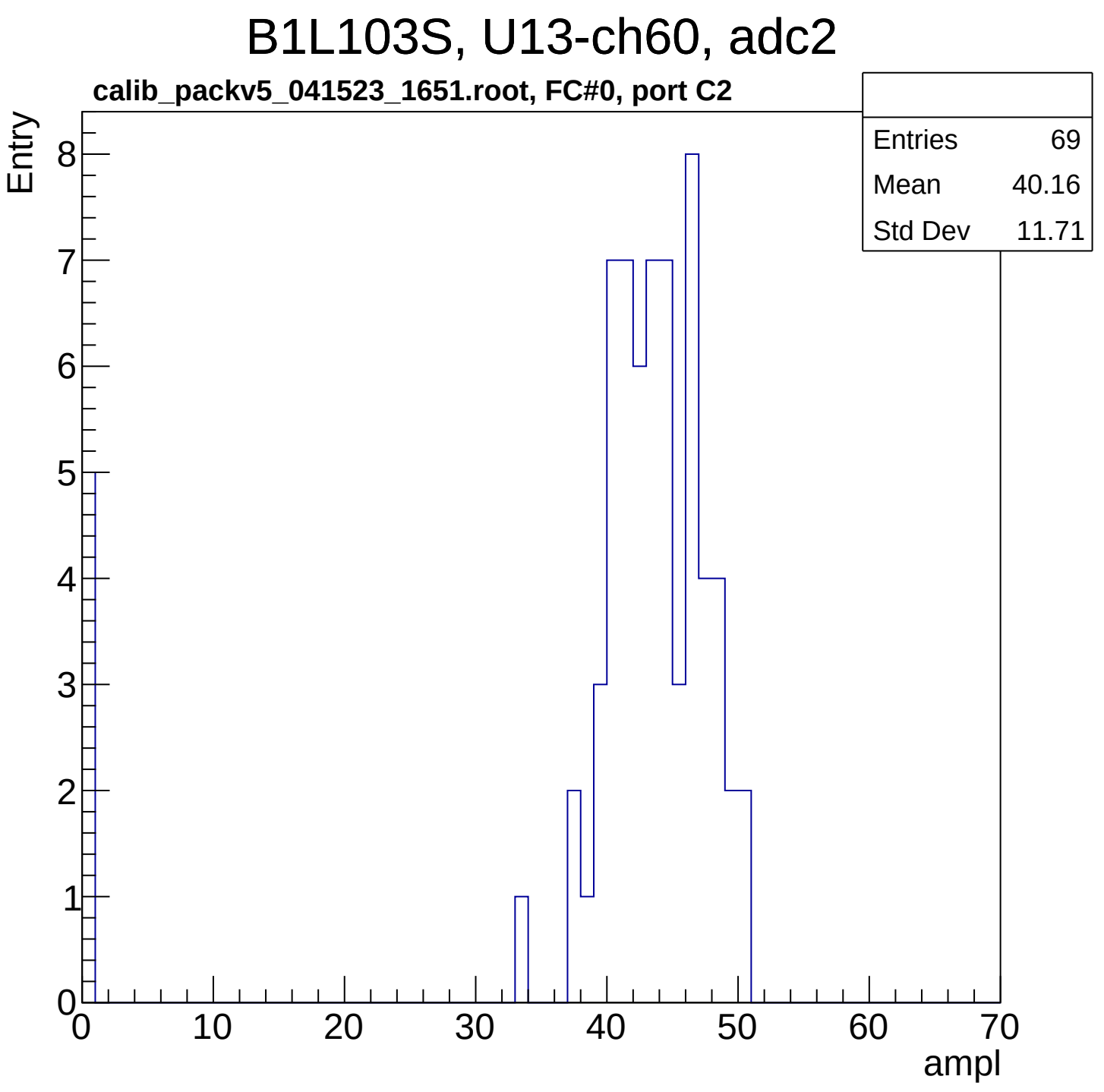

B1L103S, U13-ch59, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 60.4
Std Dev 2.045
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch59, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch59, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch60, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 25.12
Std Dev 10.14
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch60, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 33.01
Std Dev 10.05
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch60, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 40.16
Std Dev 11.71
Entry
ampl
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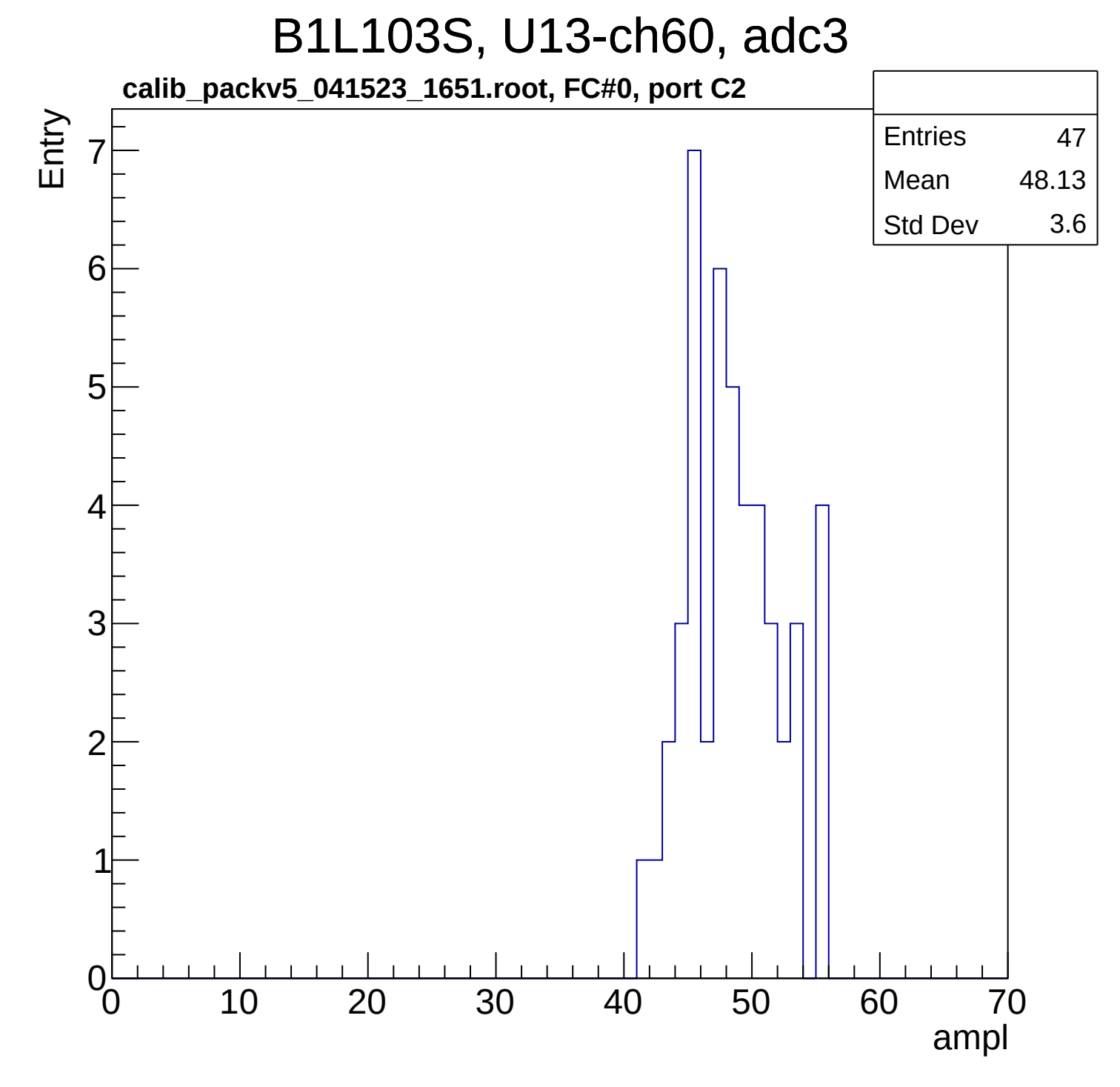
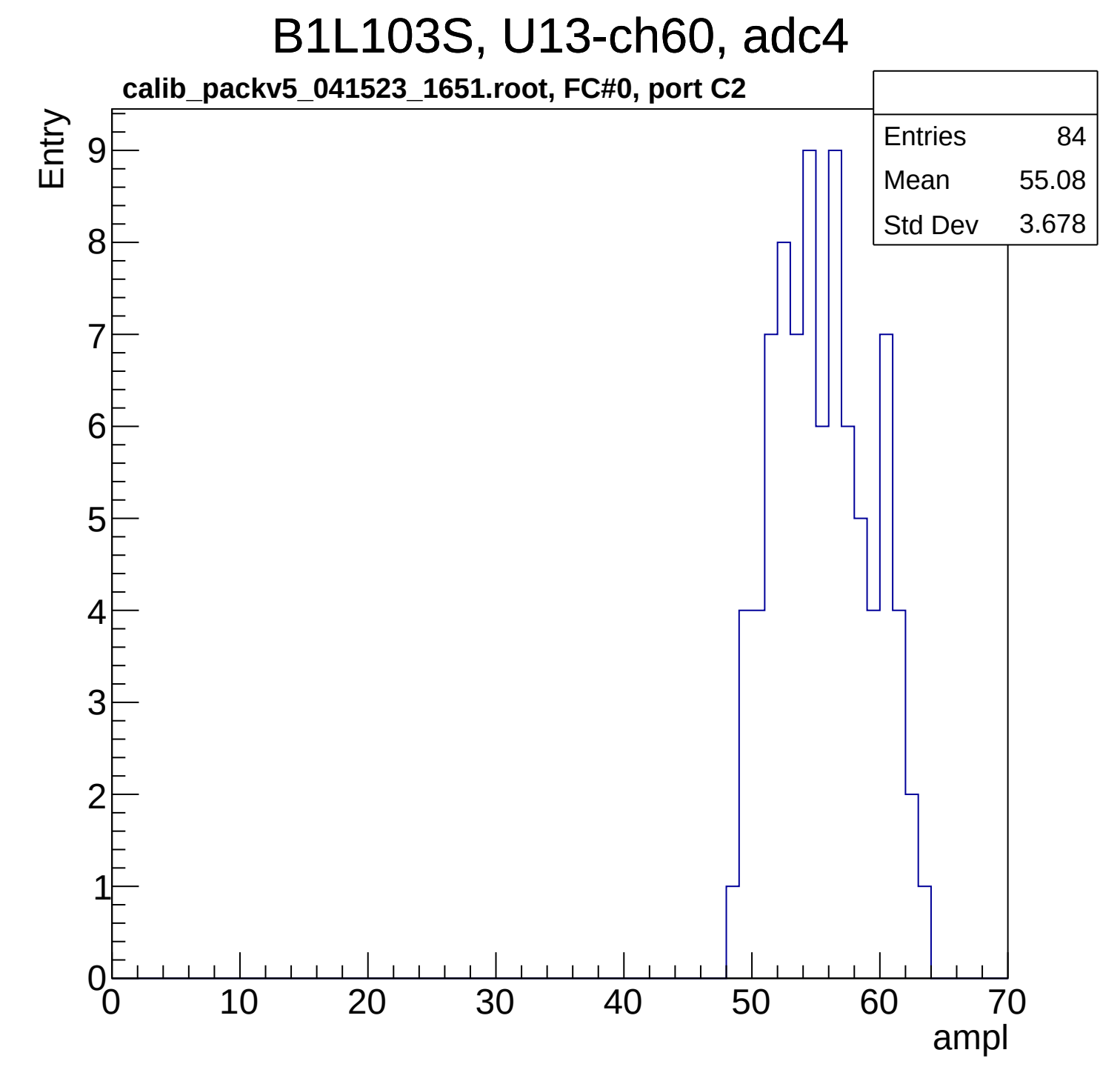
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch60, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 48.13
Std Dev 3.6
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch60, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 55.08
Std Dev 3.678
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
50
60
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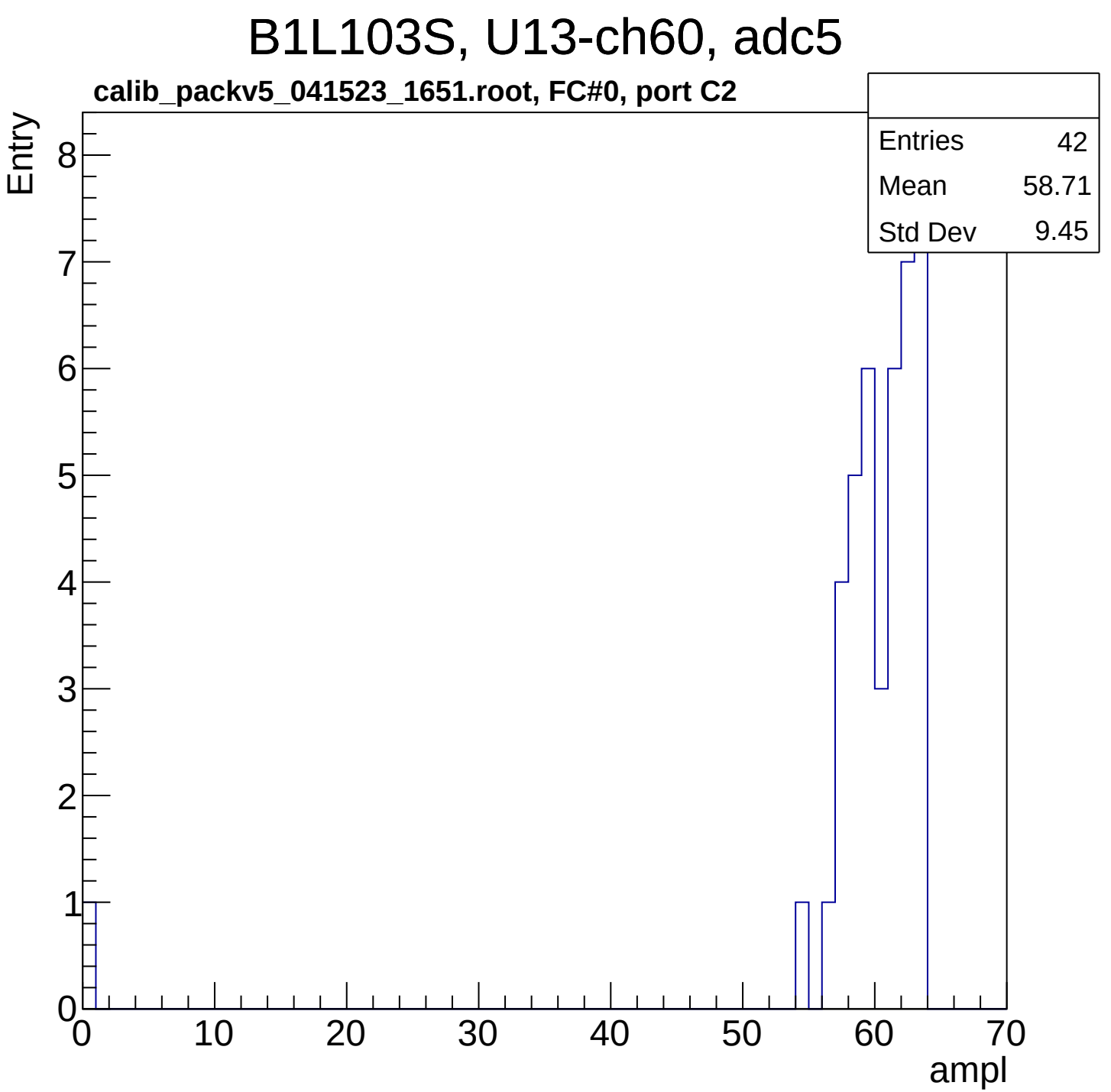
B1L103S, U13-ch60, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 58.71
Std Dev 9.45
Entry
ampl
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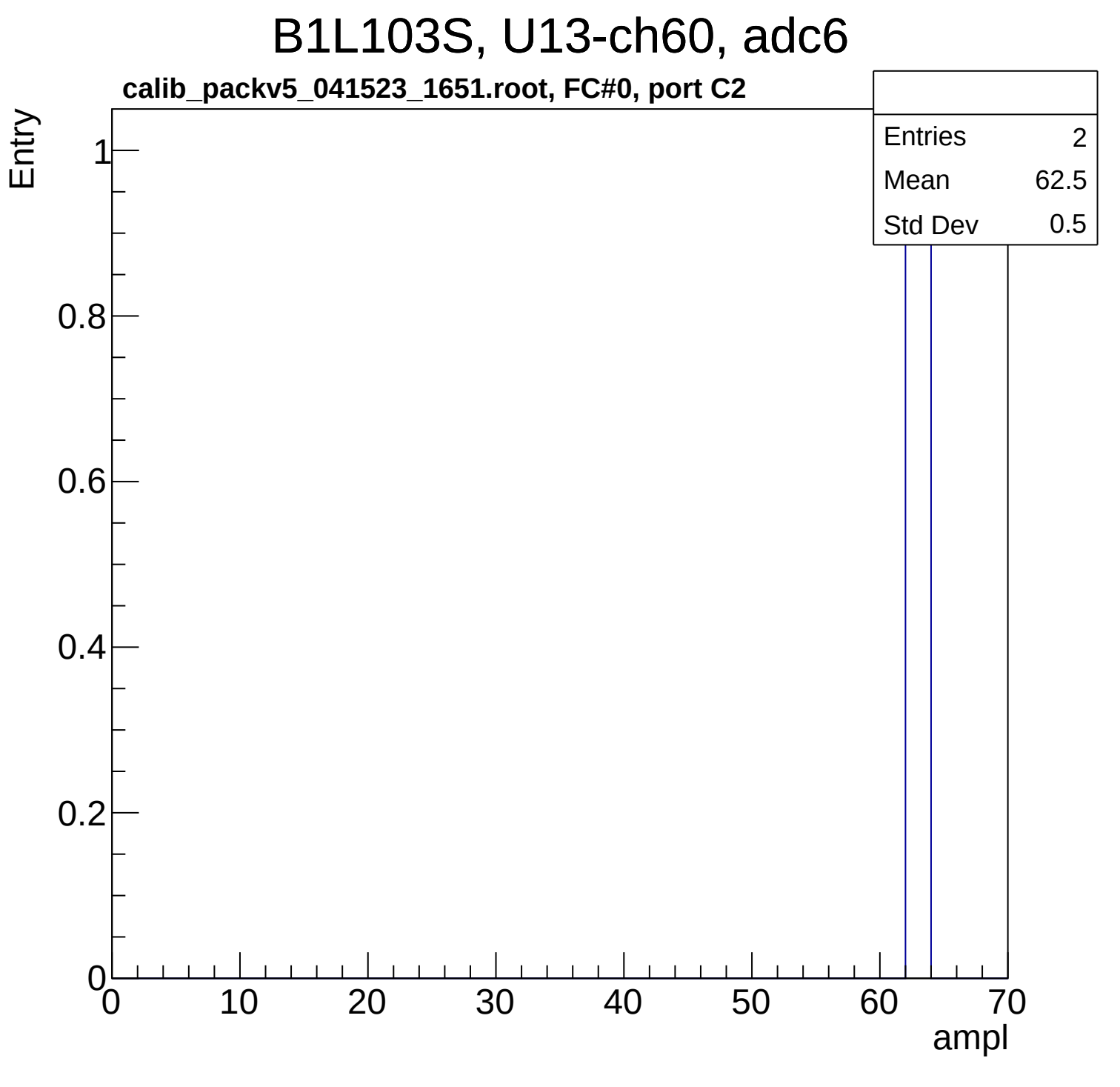
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch60, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
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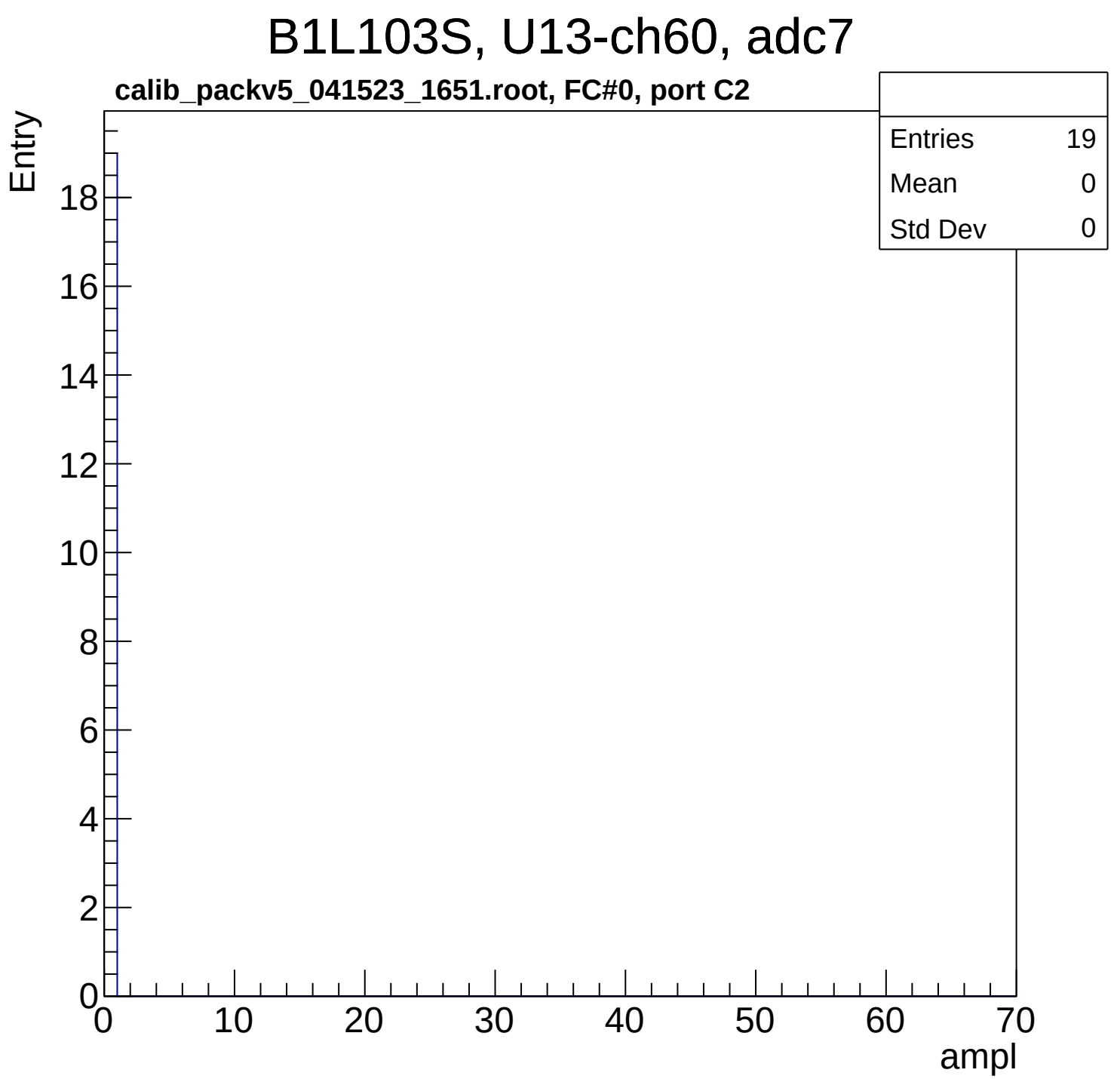
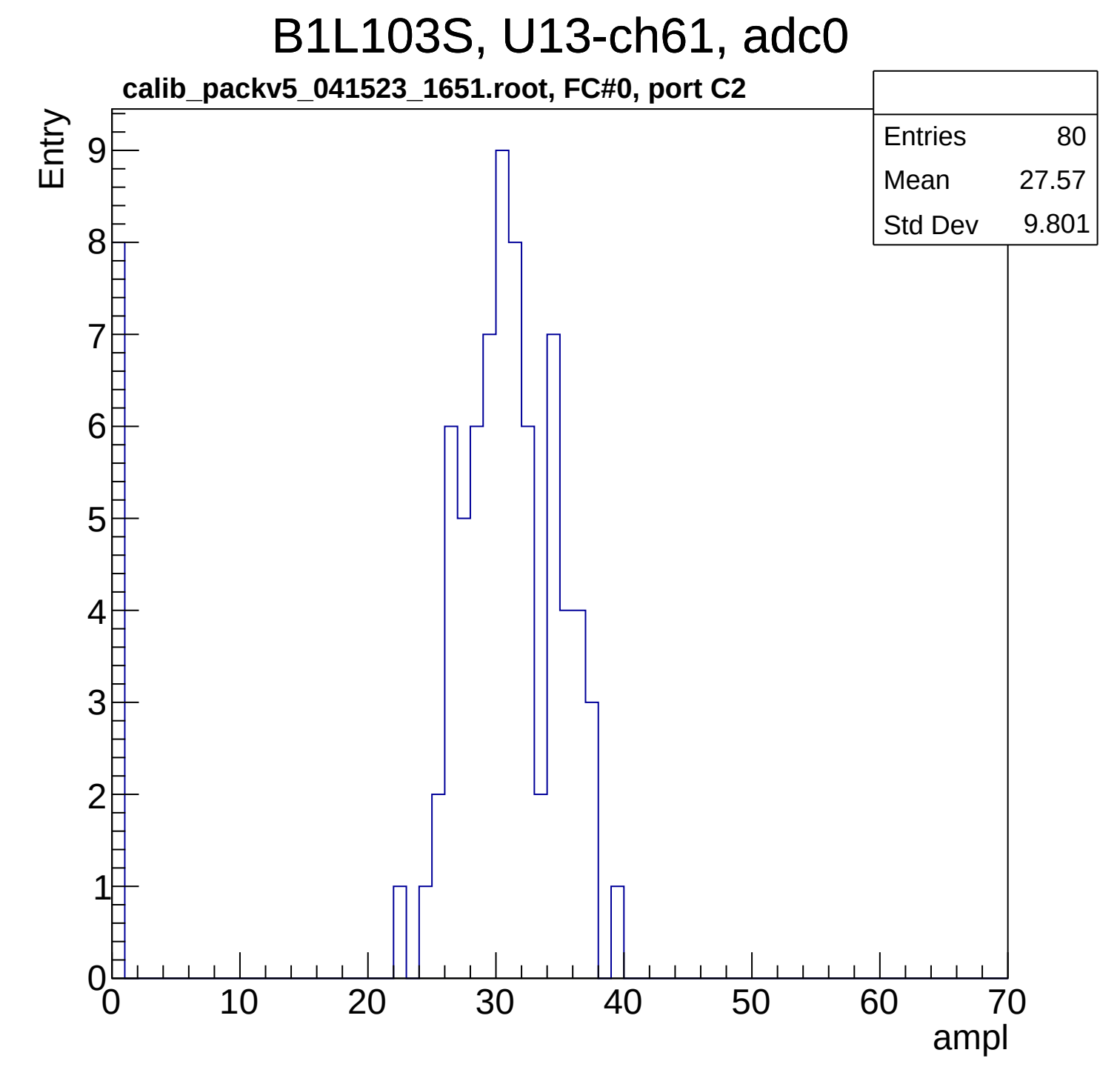
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch60, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch61, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 27.57
Std Dev 9.801
Entry
ampl
0
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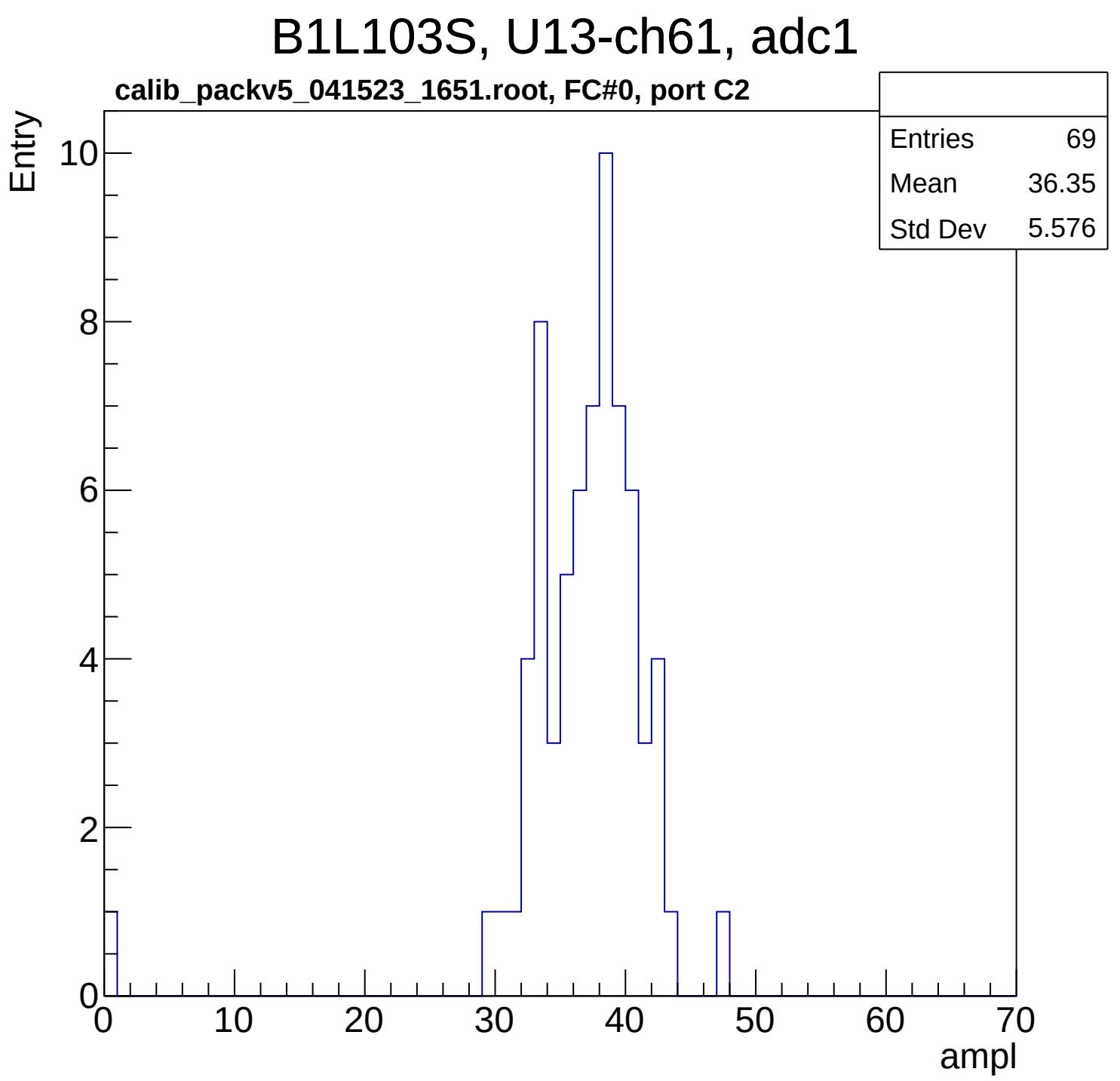
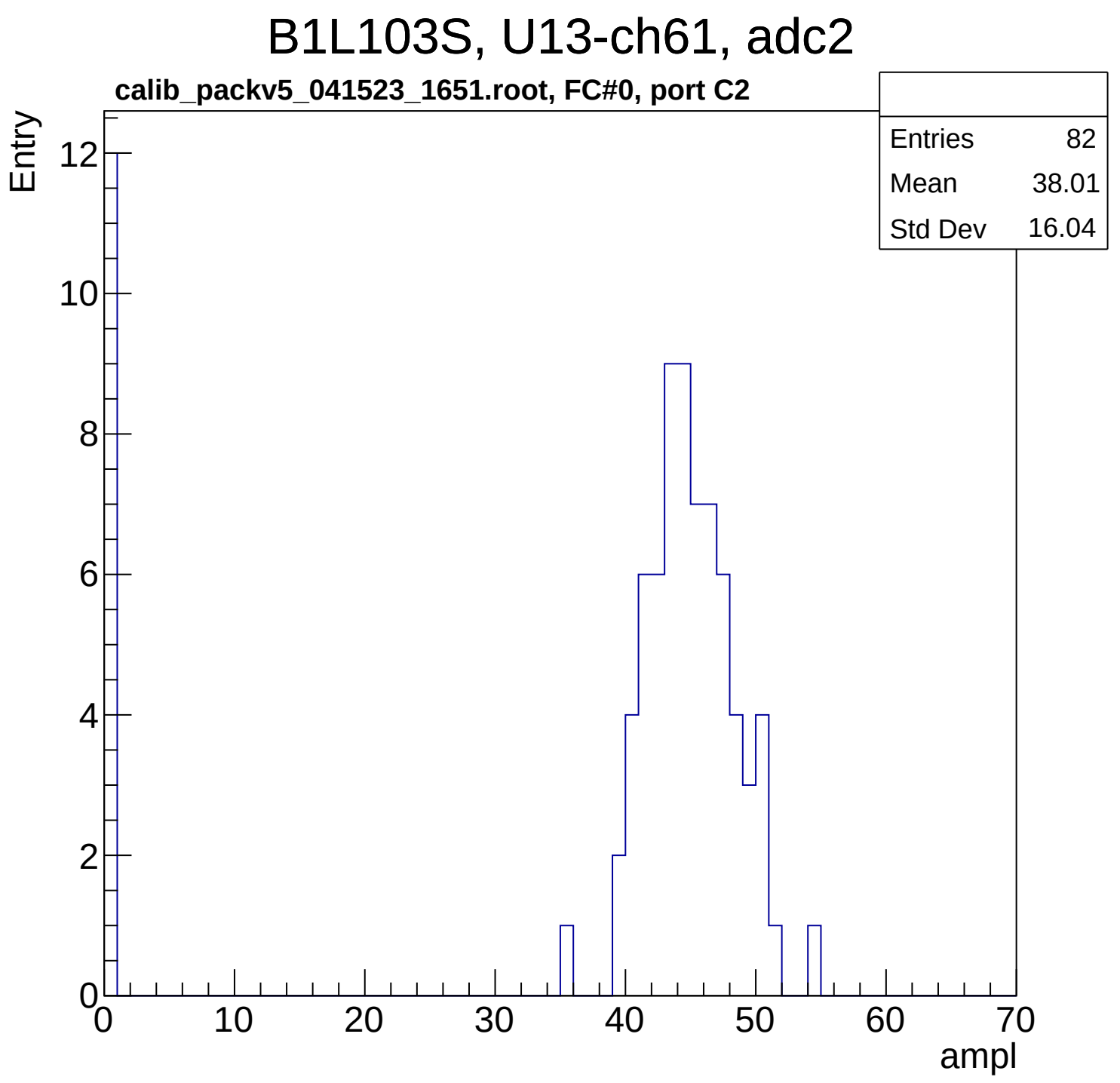
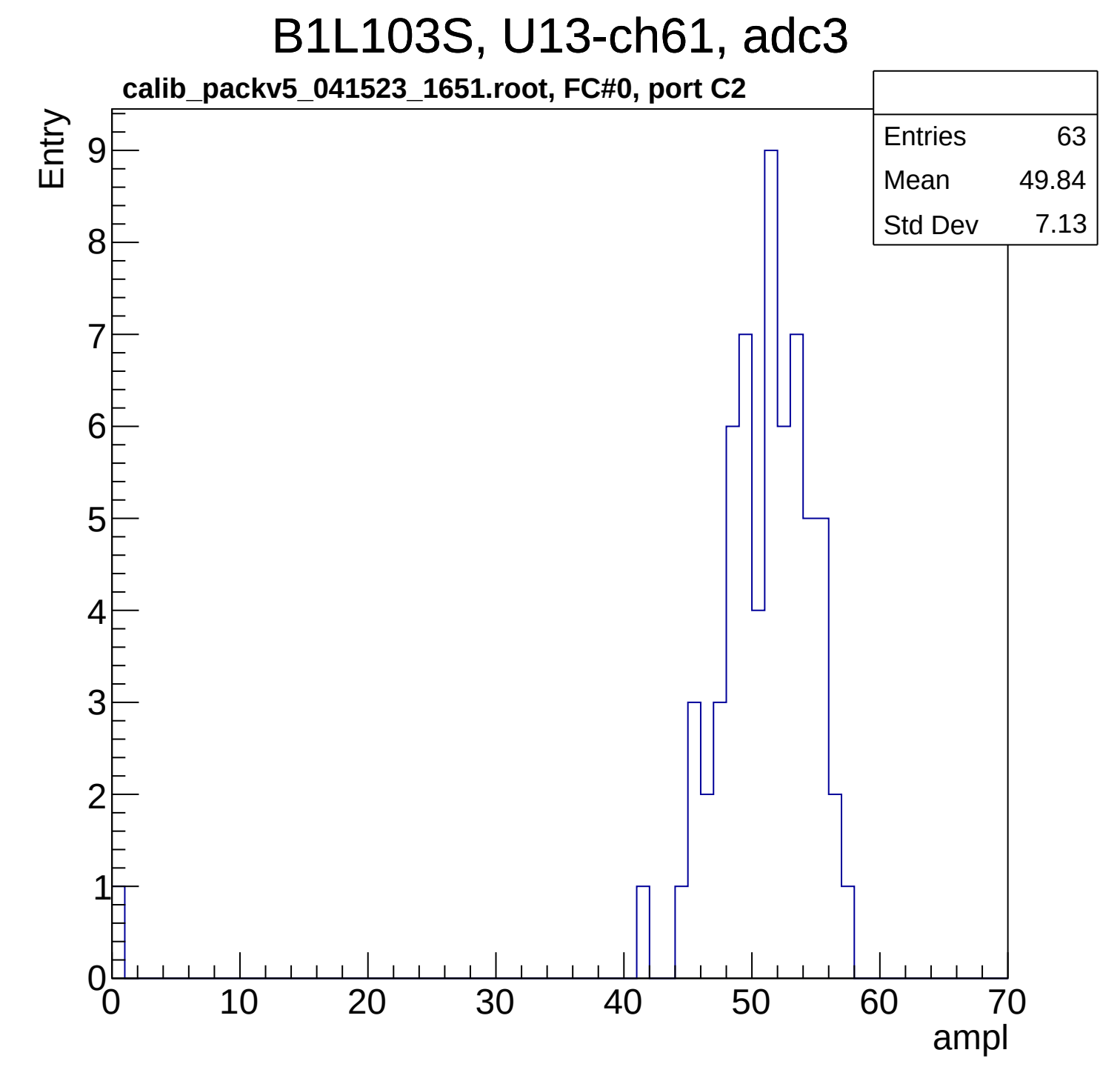
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch61, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 36.35
Std Dev 5.576
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch61, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 38.01
Std Dev 16.04
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch61, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 49.84
Std Dev 7.13
Entry
ampl
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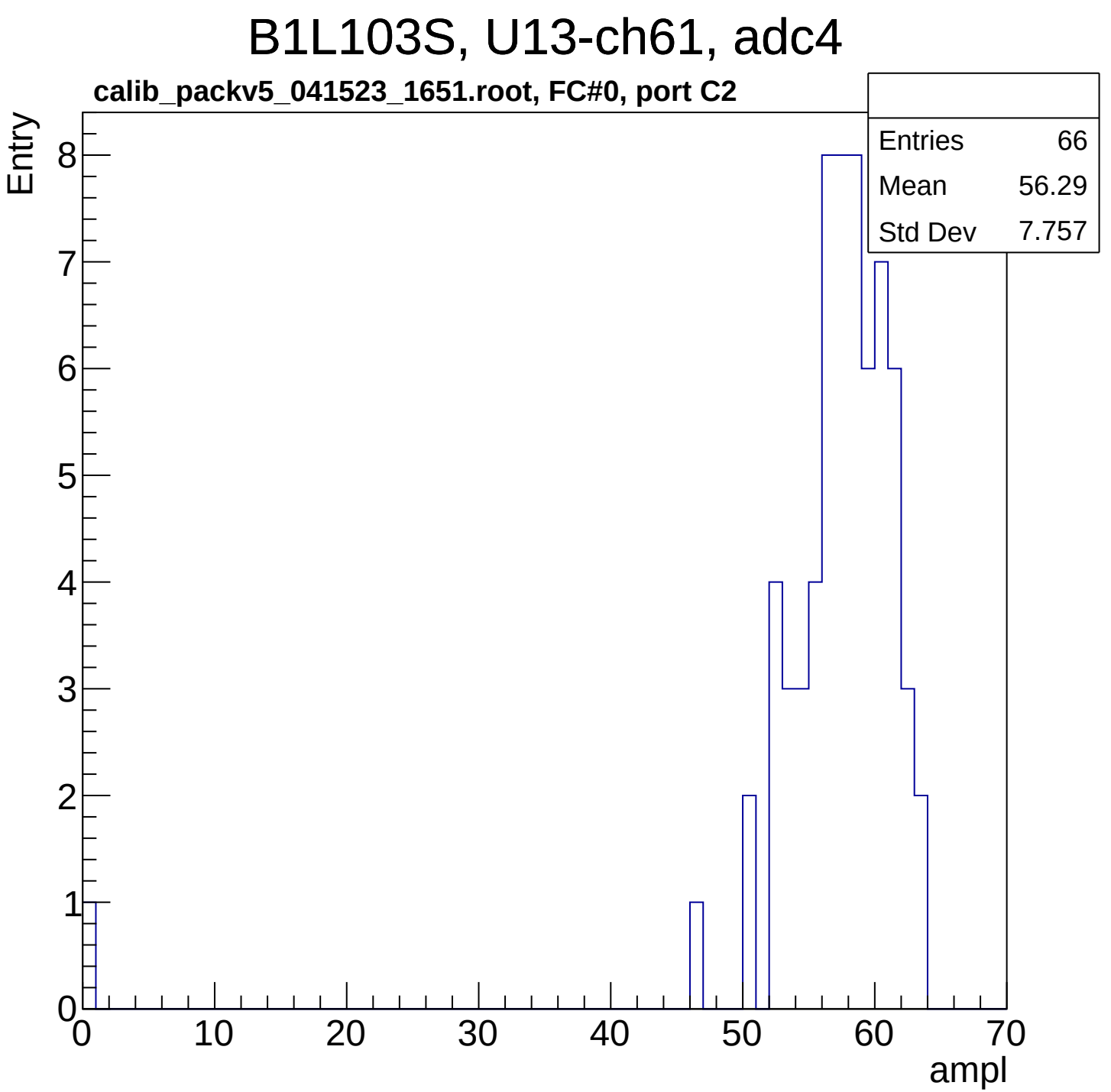
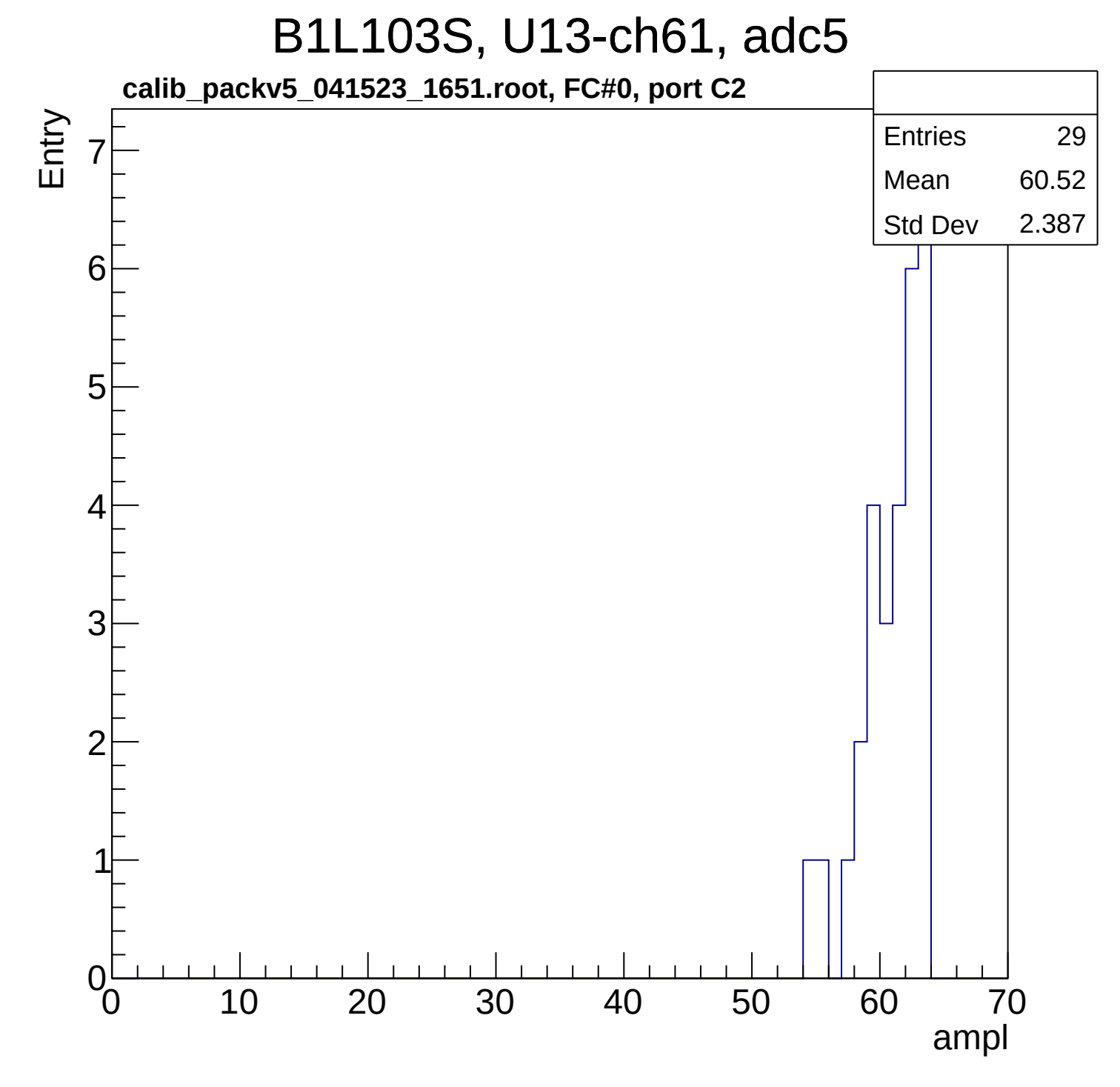
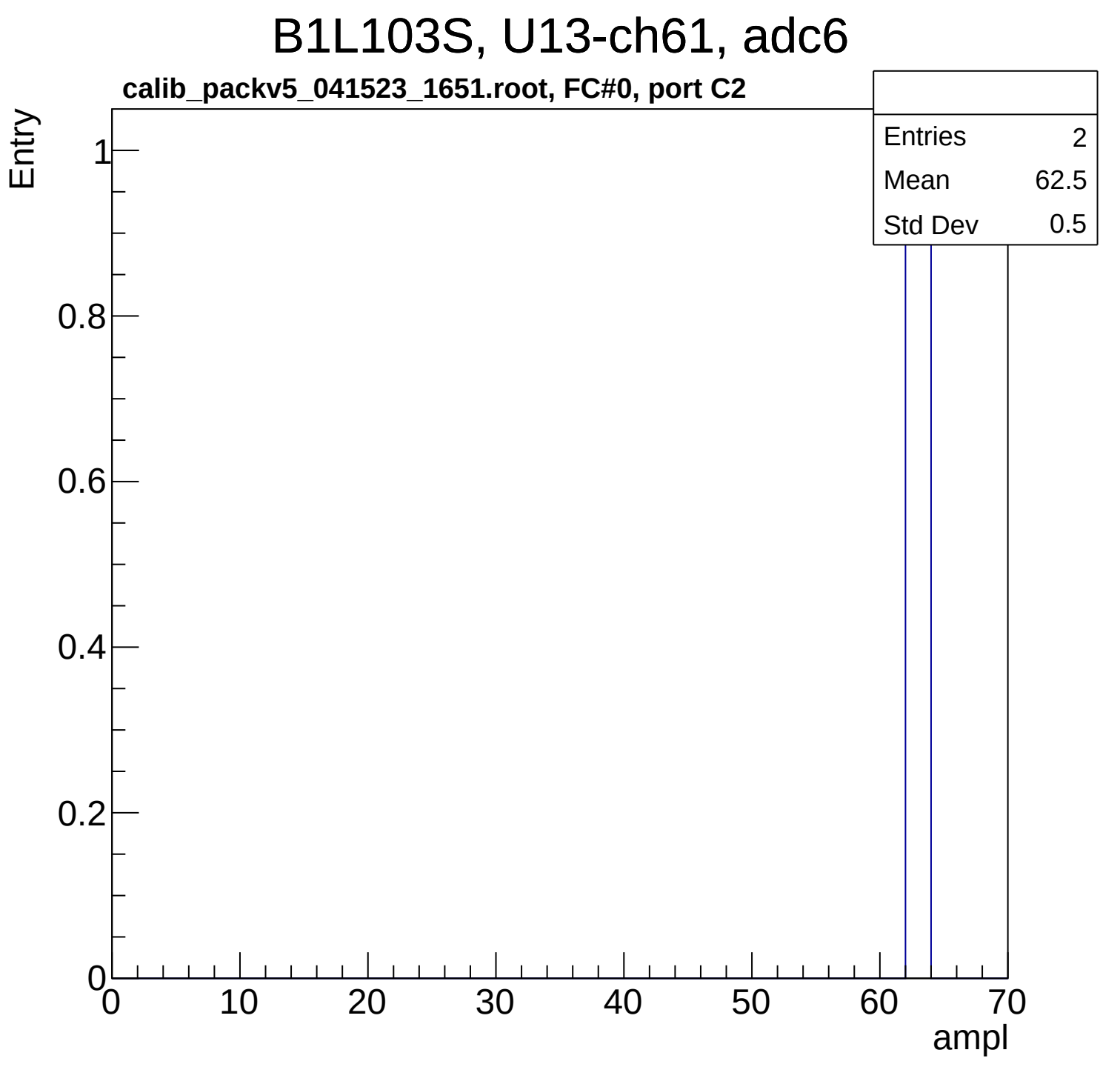
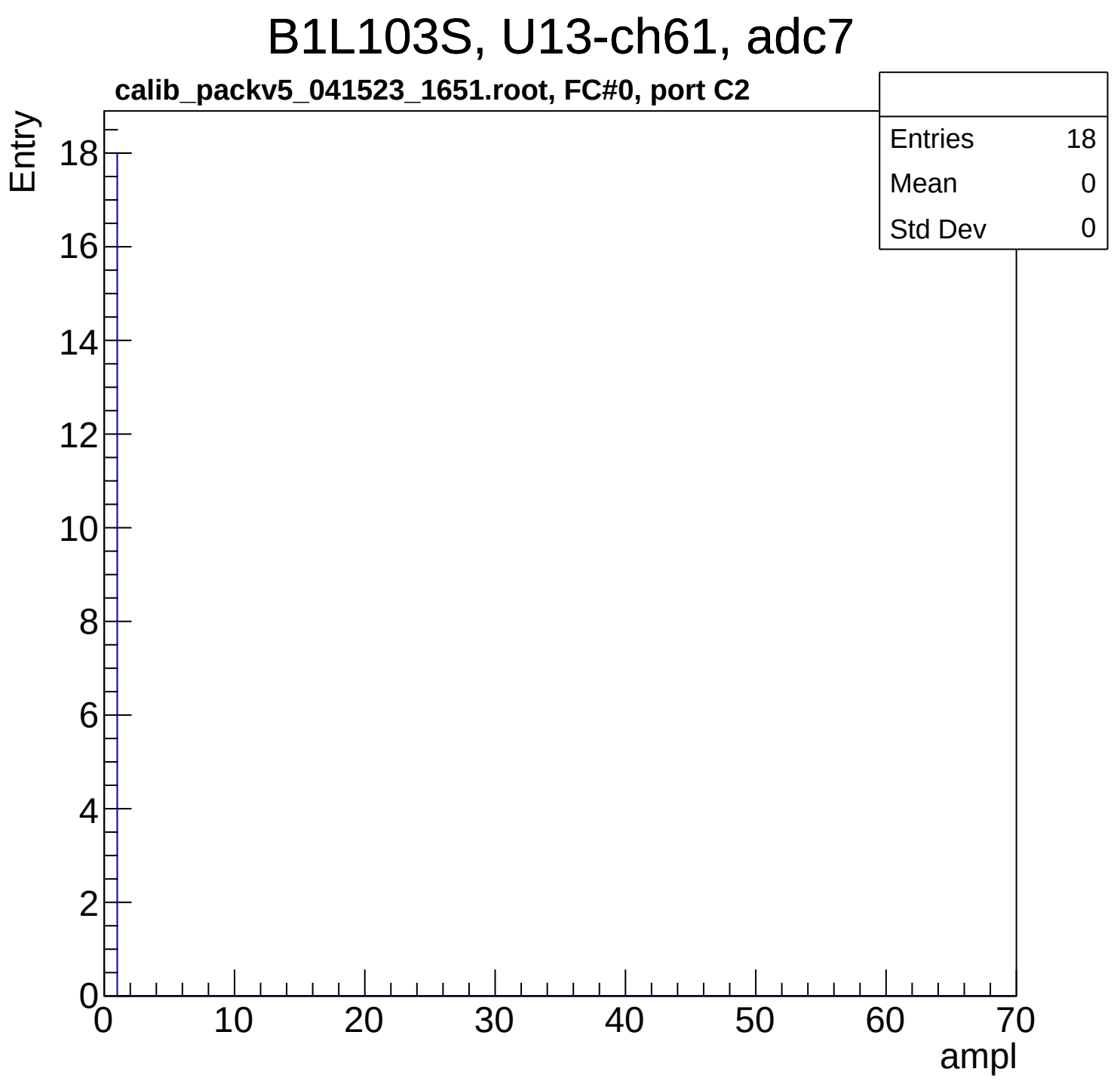
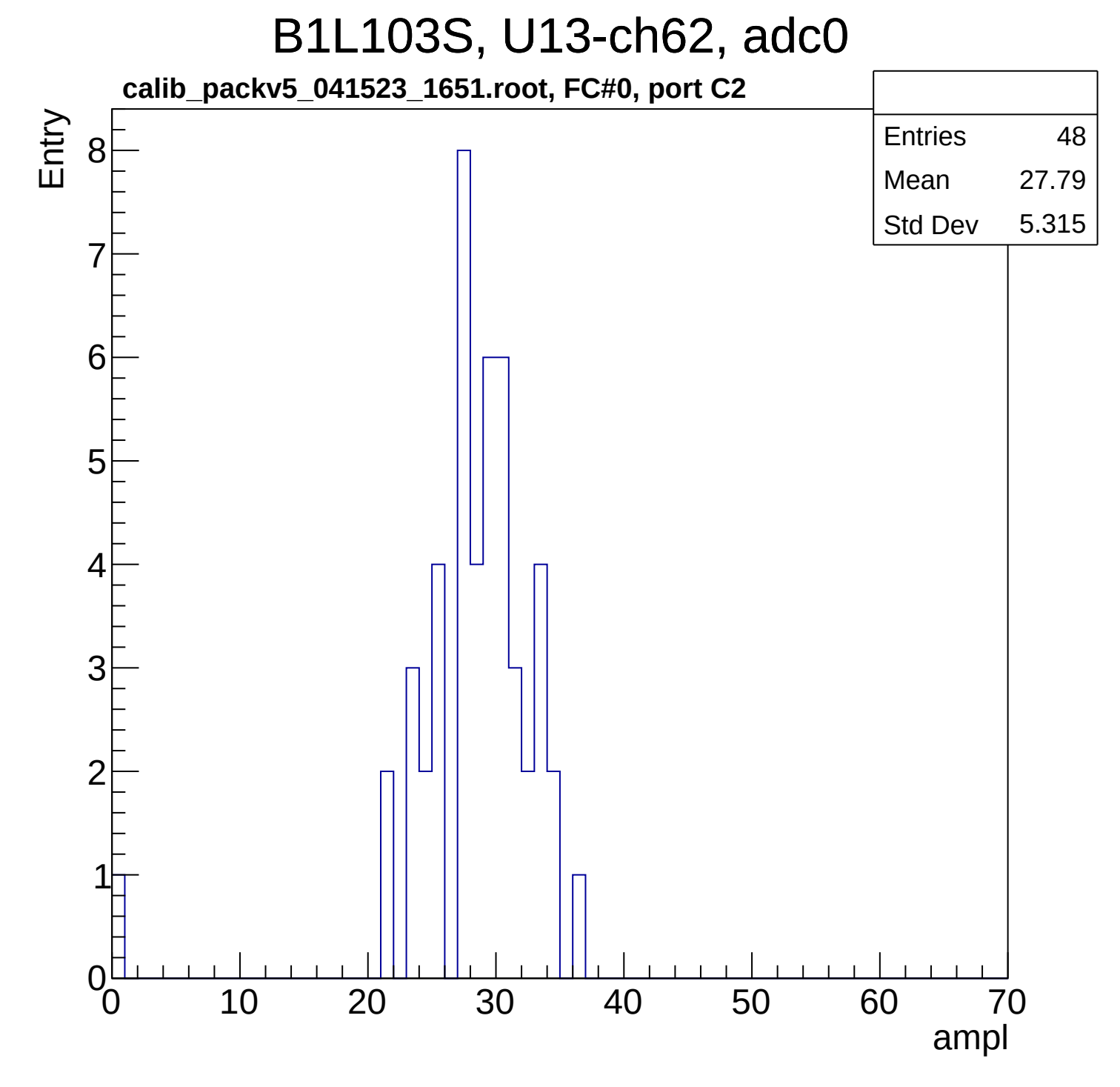
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch61, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 56.29
Std Dev 7.757
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch61, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 60.52
Std Dev 2.387
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch61, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch61, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch62, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 27.79
Std Dev 5.315
Entry
ampl
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1
2
3
4
5
6
7
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0
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40
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60
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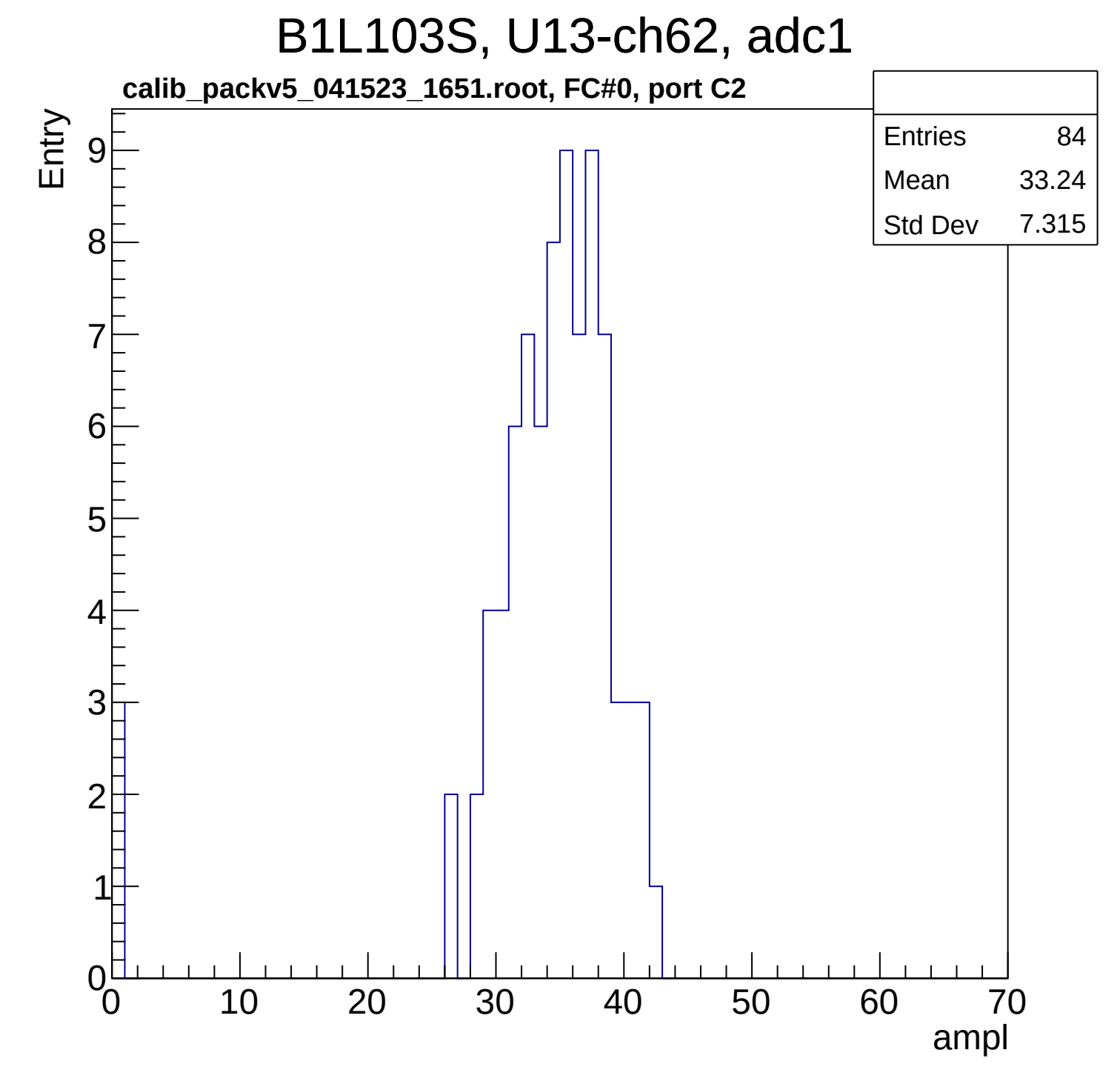
B1L103S, U13-ch62, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 33.24
Std Dev 7.315
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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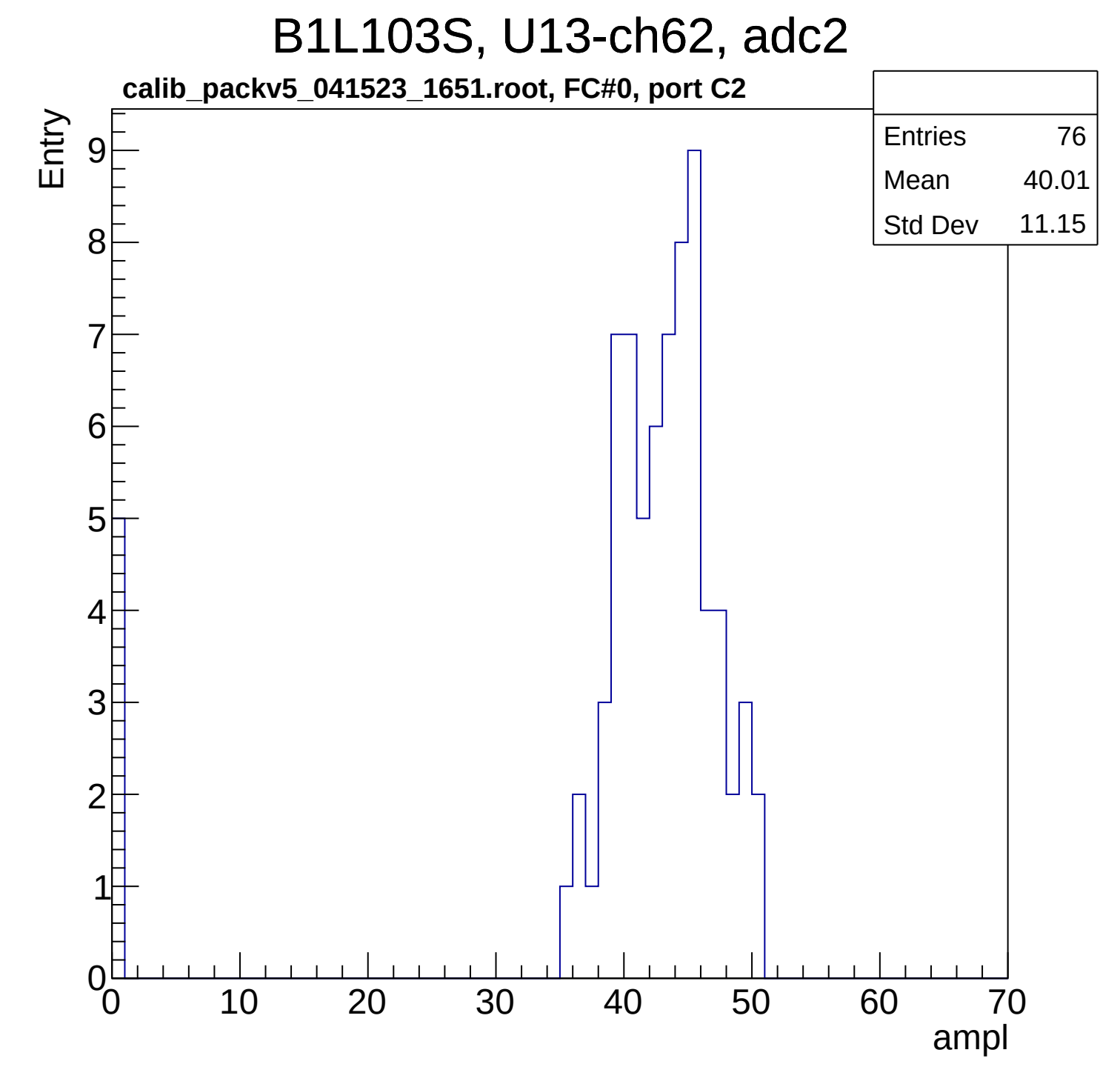
B1L103S, U13-ch62, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 40.01
Std Dev 11.15
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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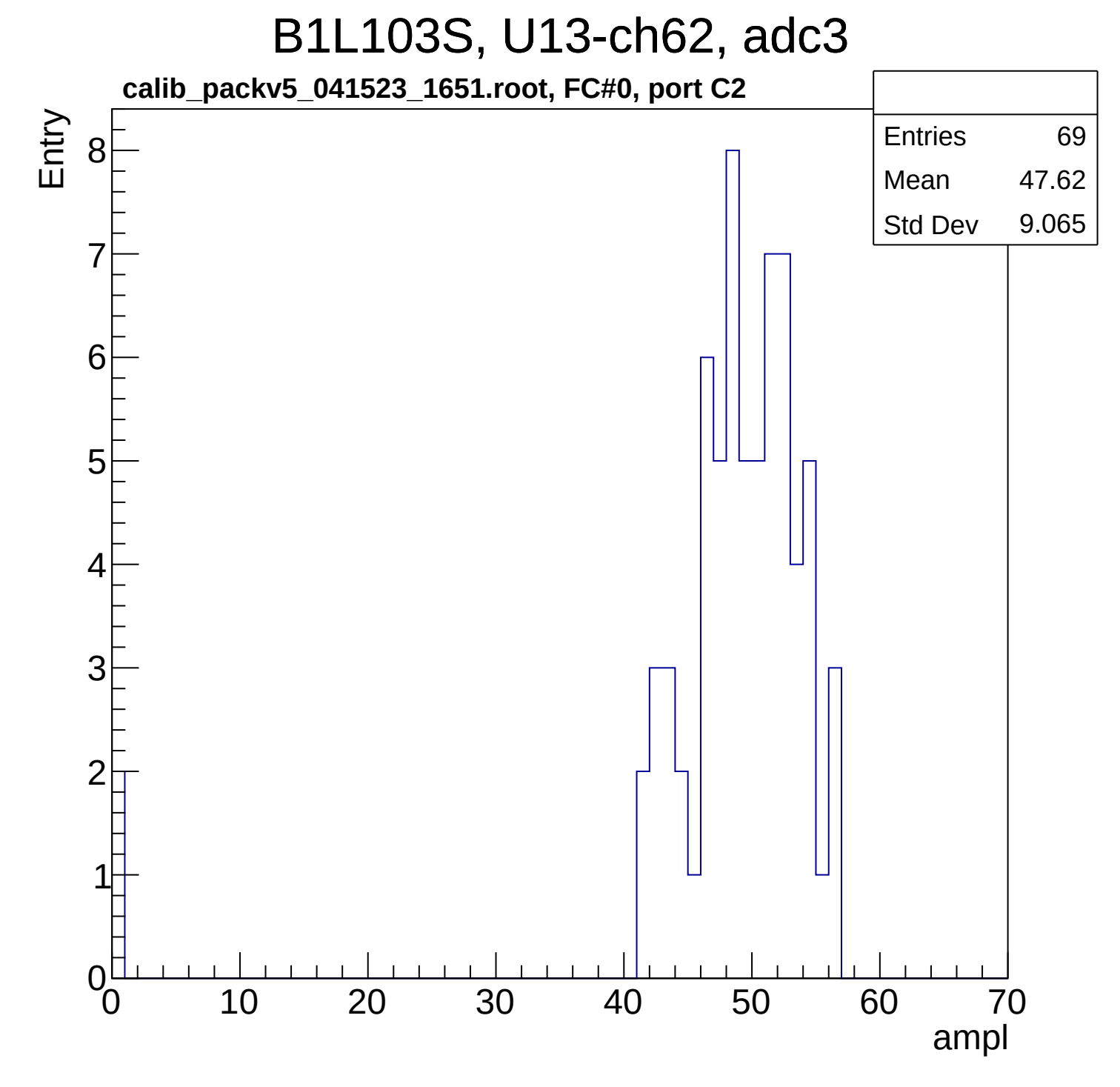
40
50
60
70


B1L103S, U13-ch62, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 47.62
Std Dev 9.065
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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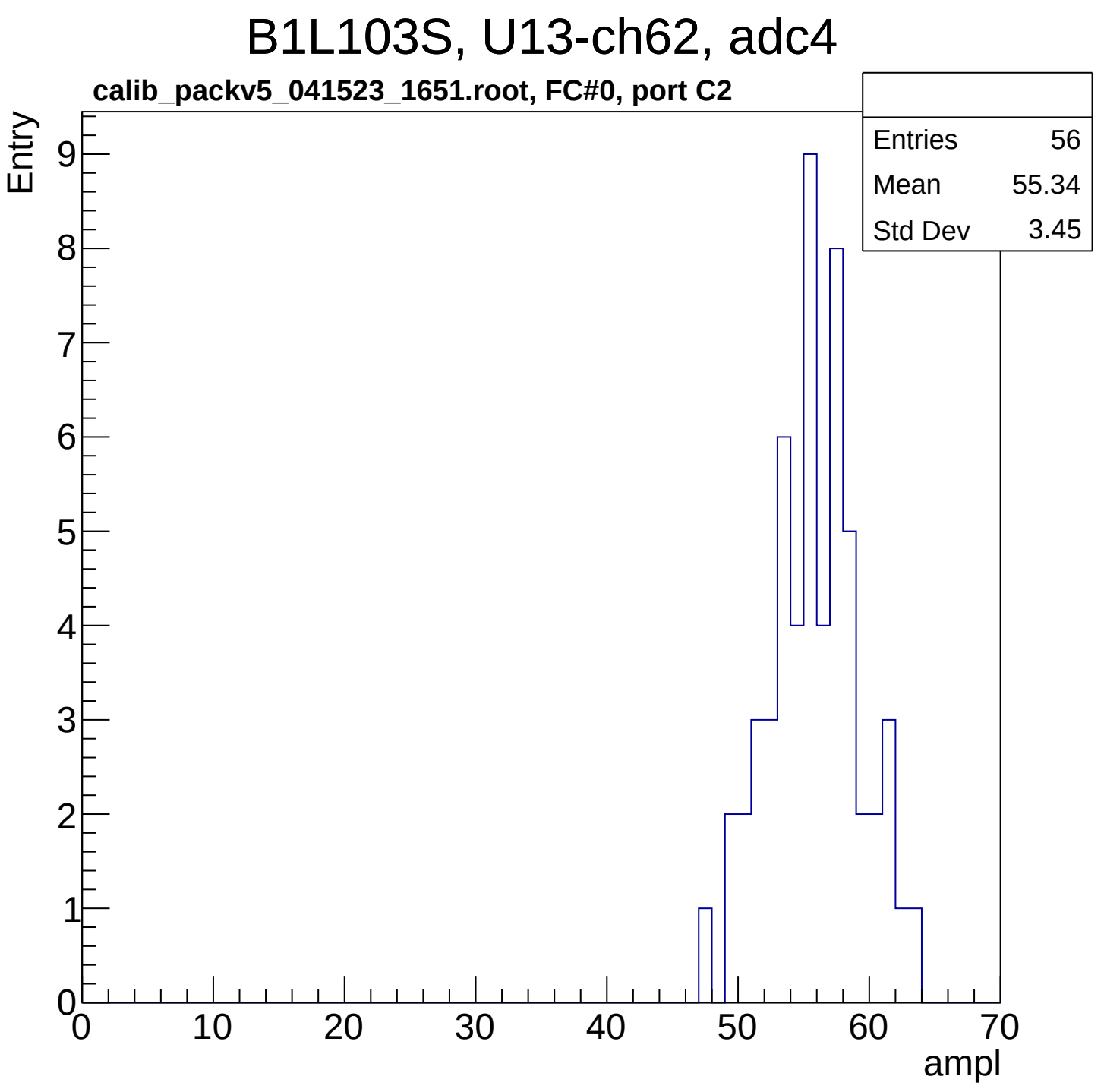
B1L103S, U13-ch62, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 55.34
Std Dev 3.45
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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40
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60
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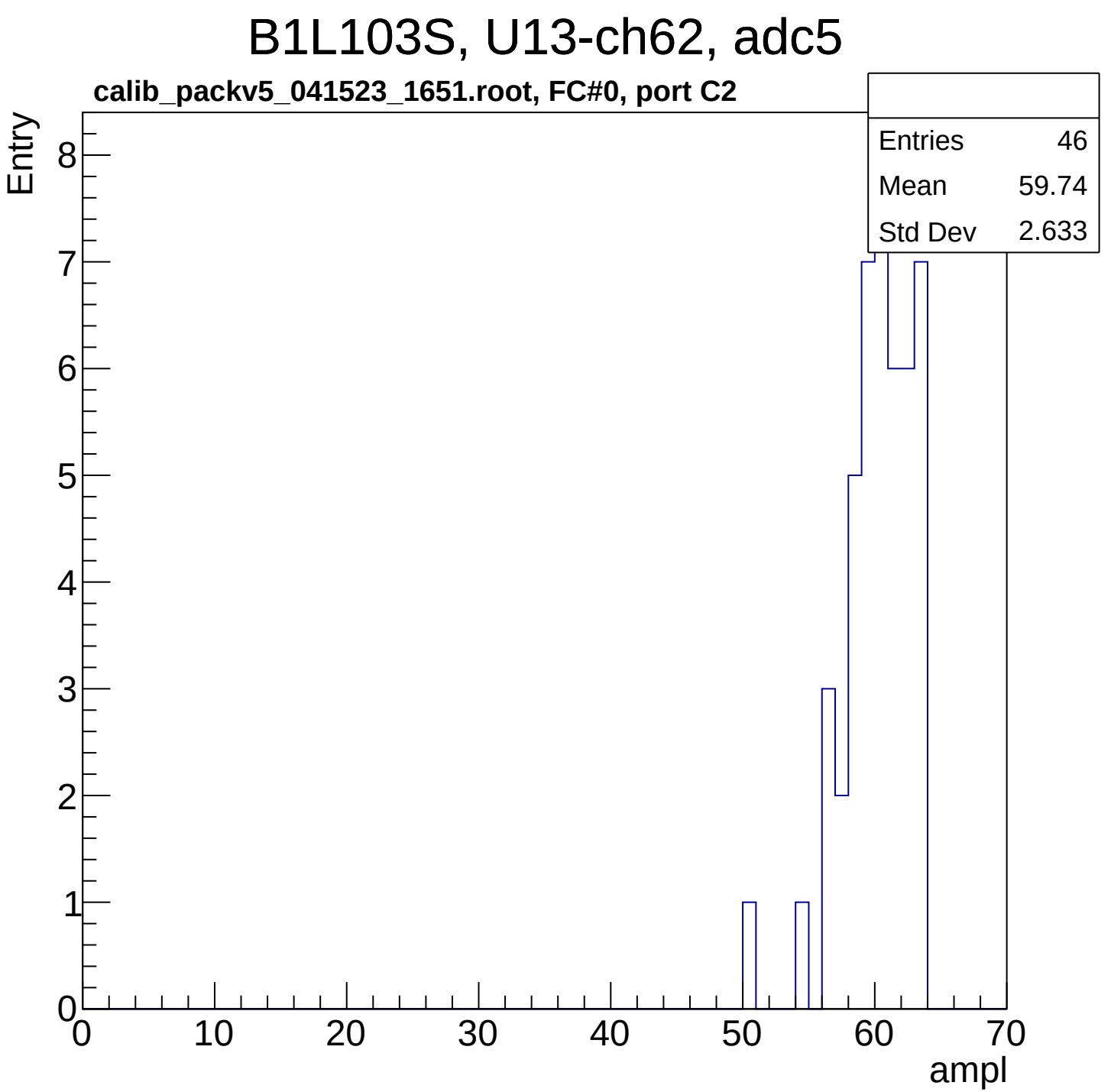
B1L103S, U13-ch62, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 59.74
Std Dev 2.633
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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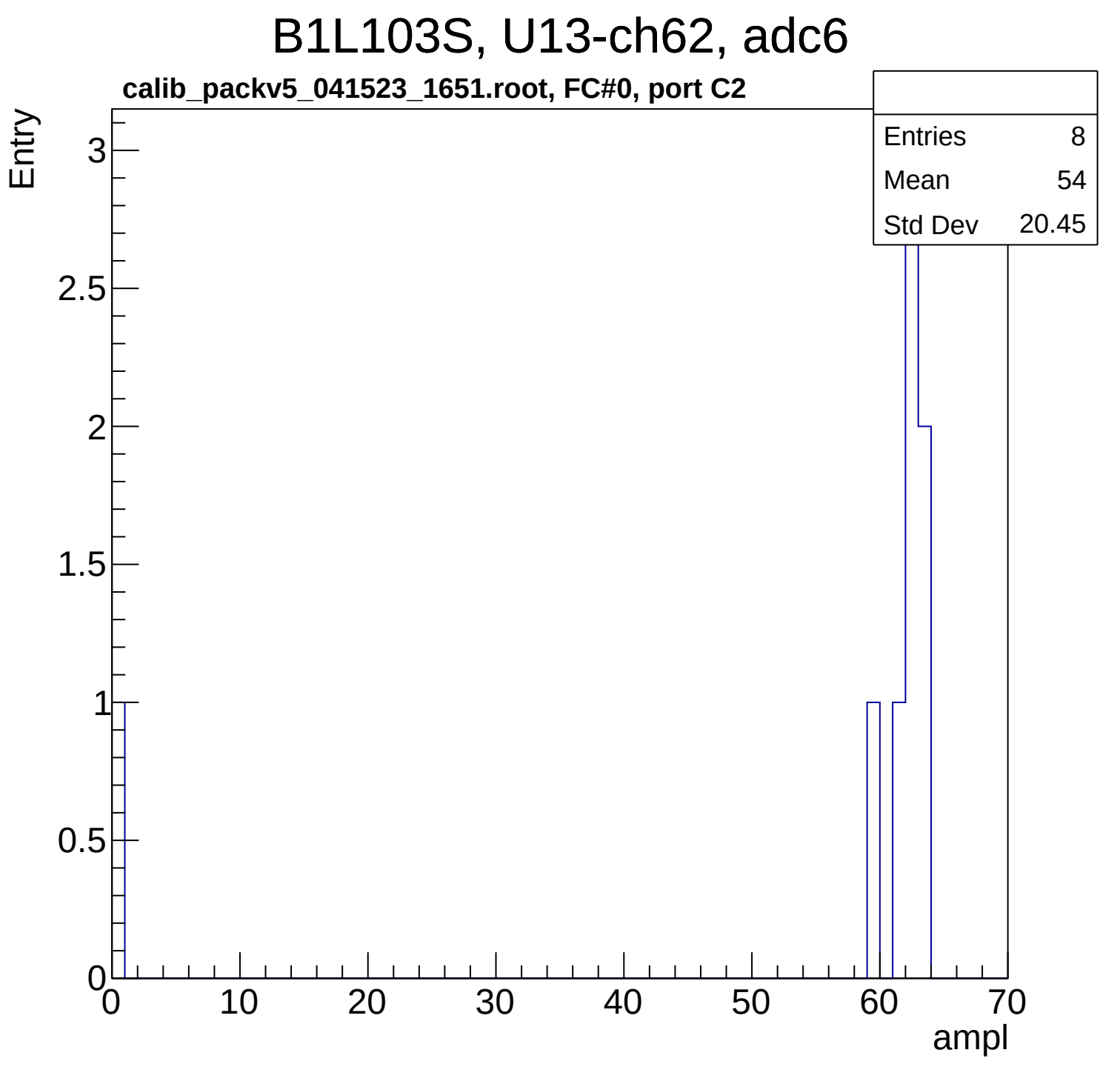
B1L103S, U13-ch62, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 54
Std Dev 20.45
Entry
ampl
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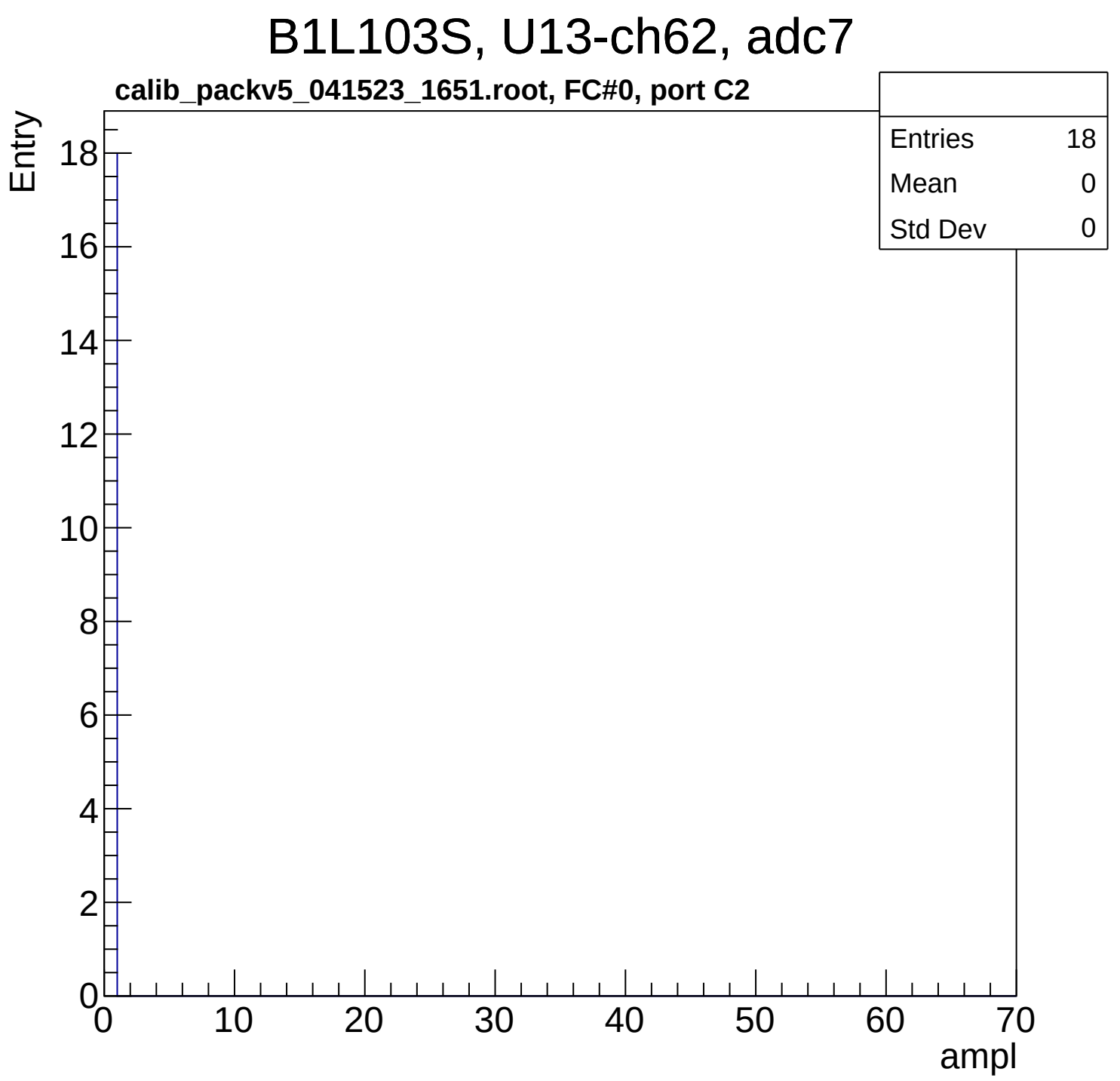
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U13-ch62, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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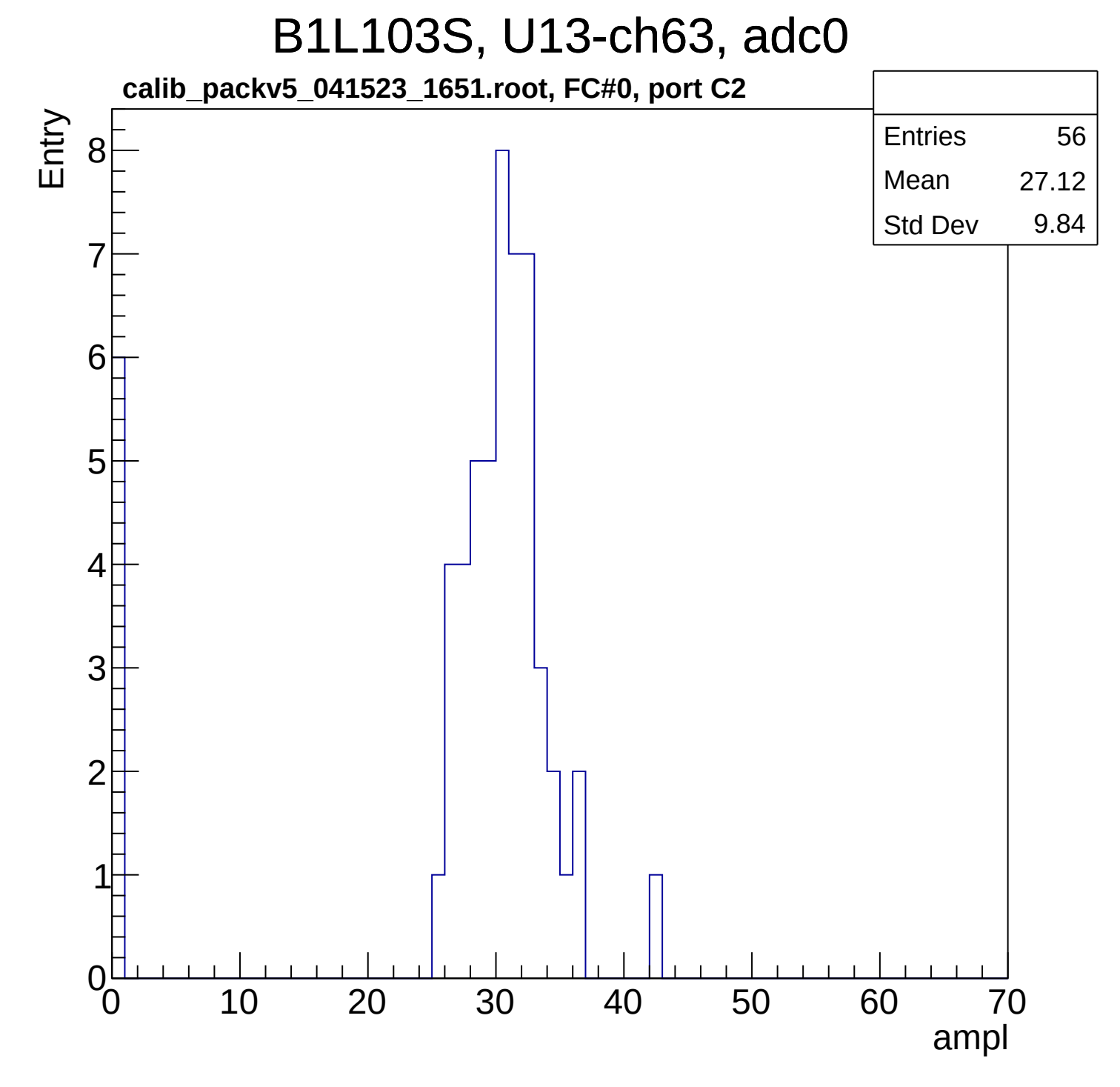
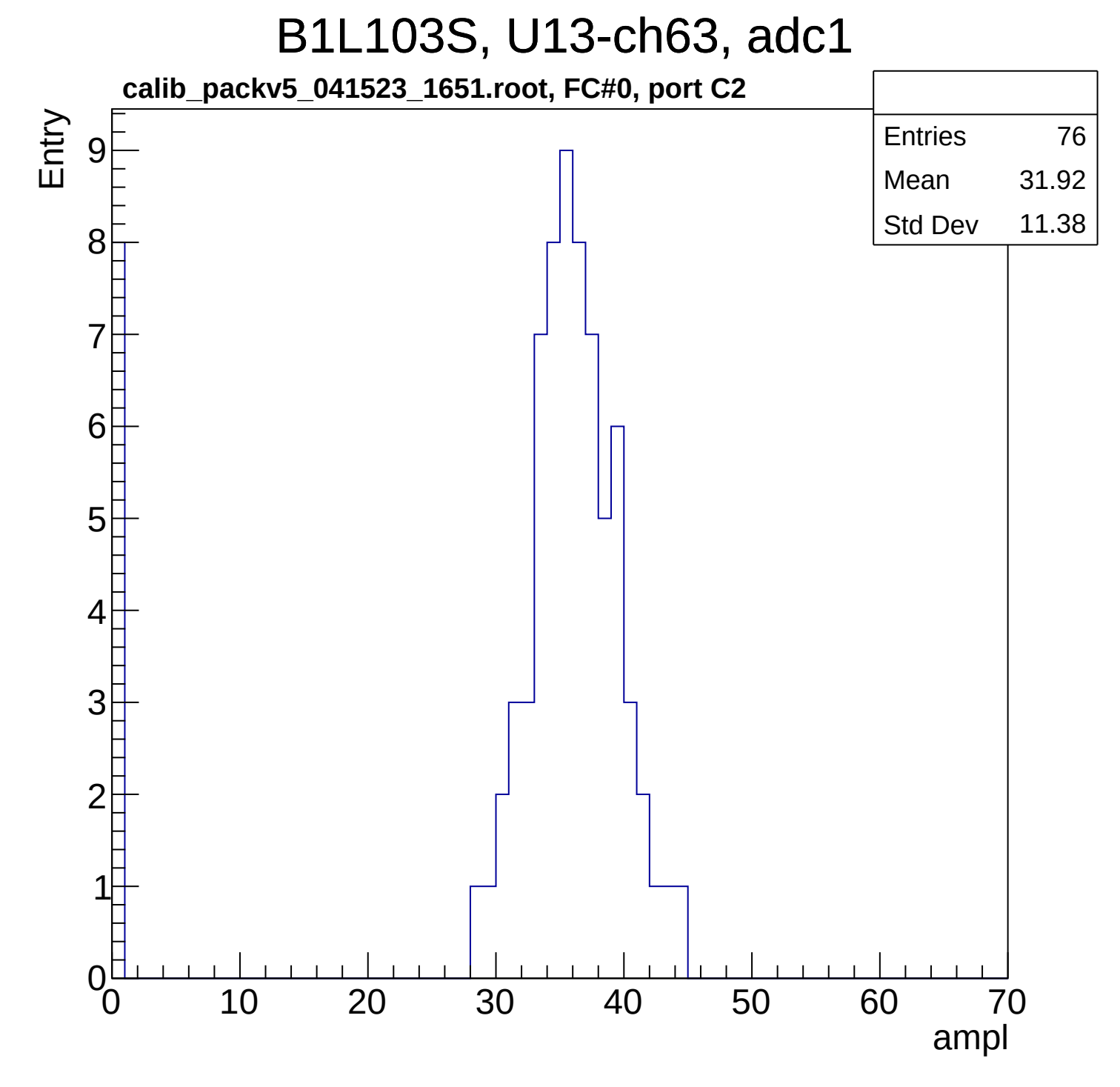
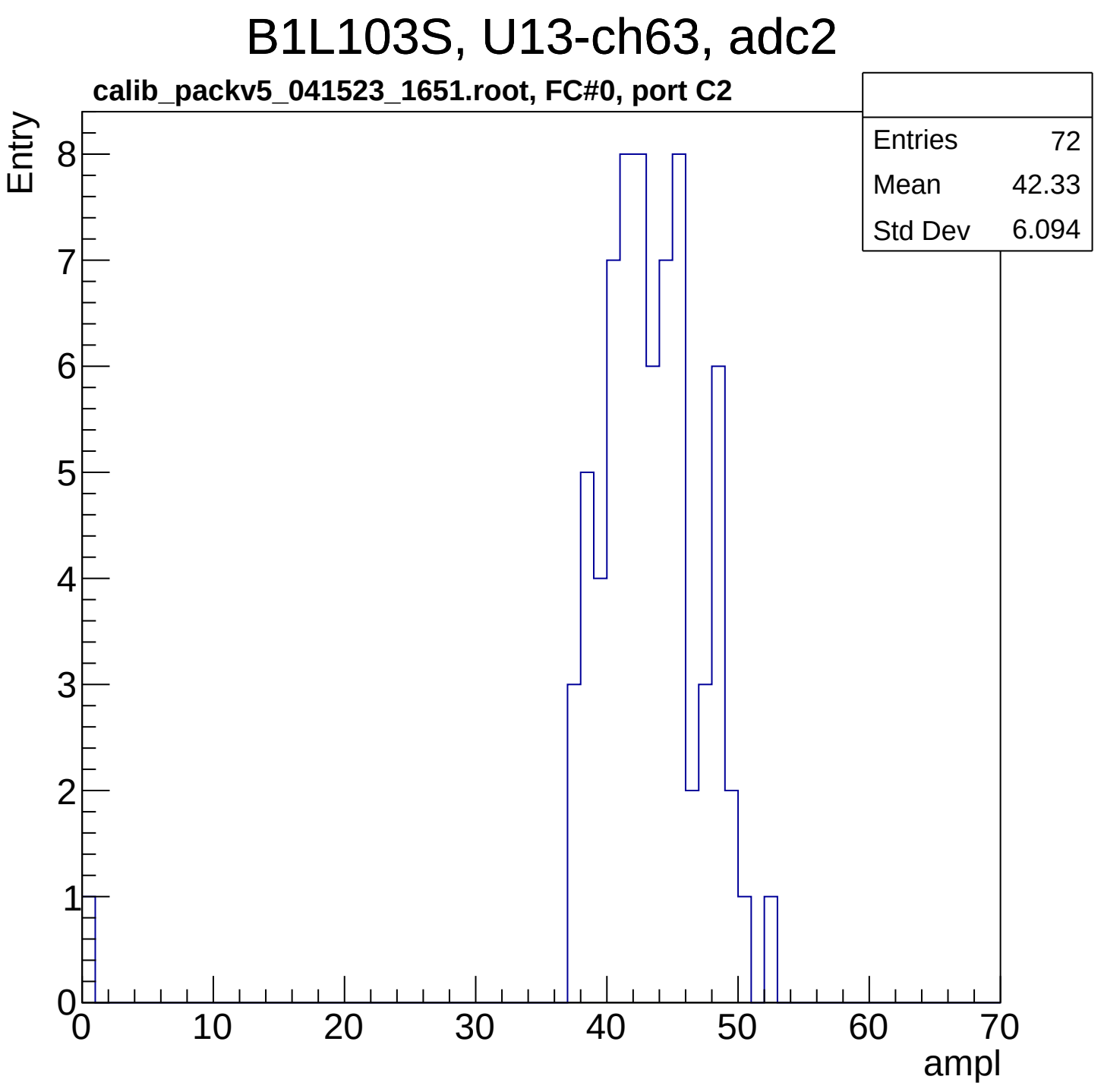
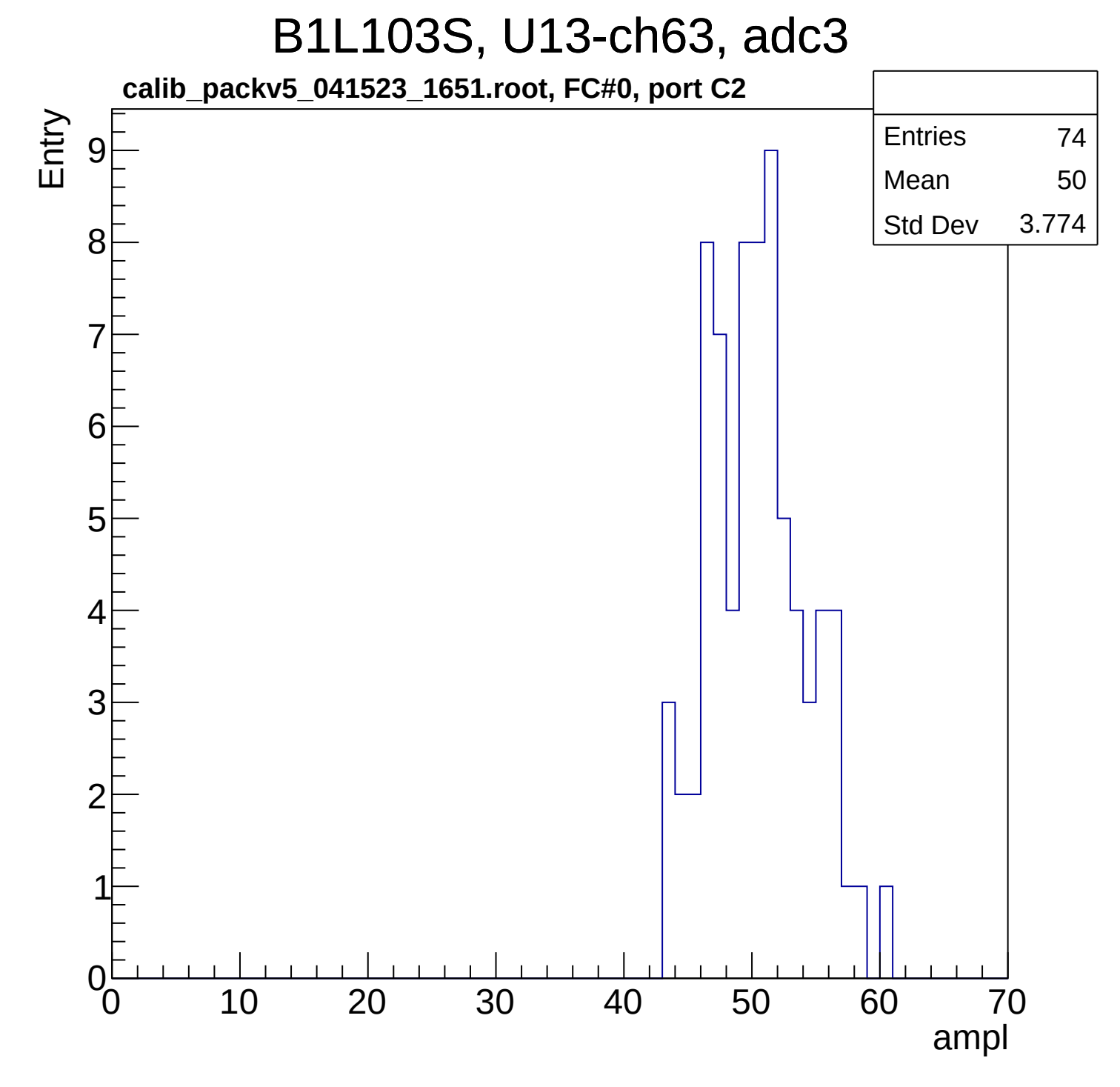
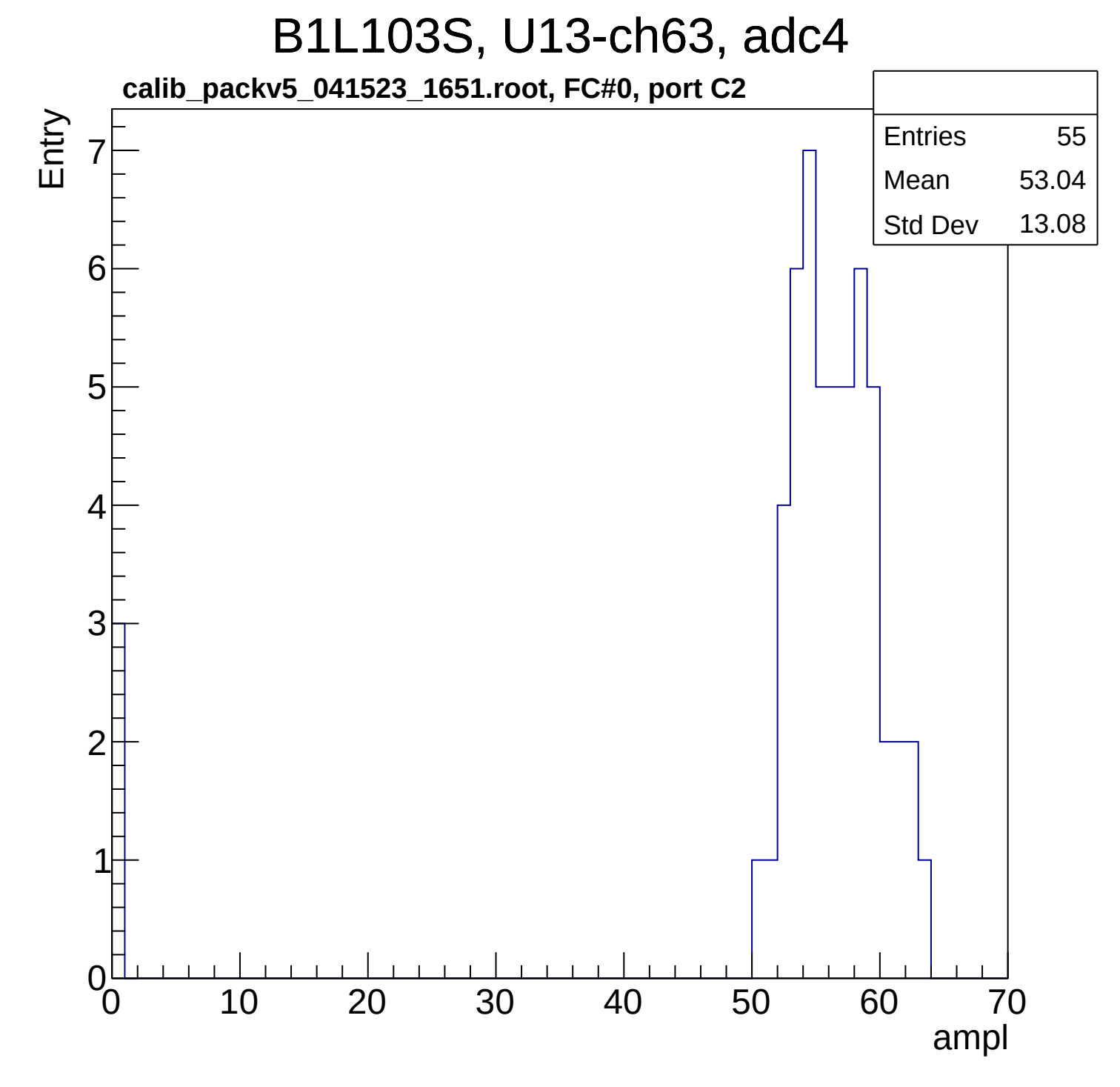
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

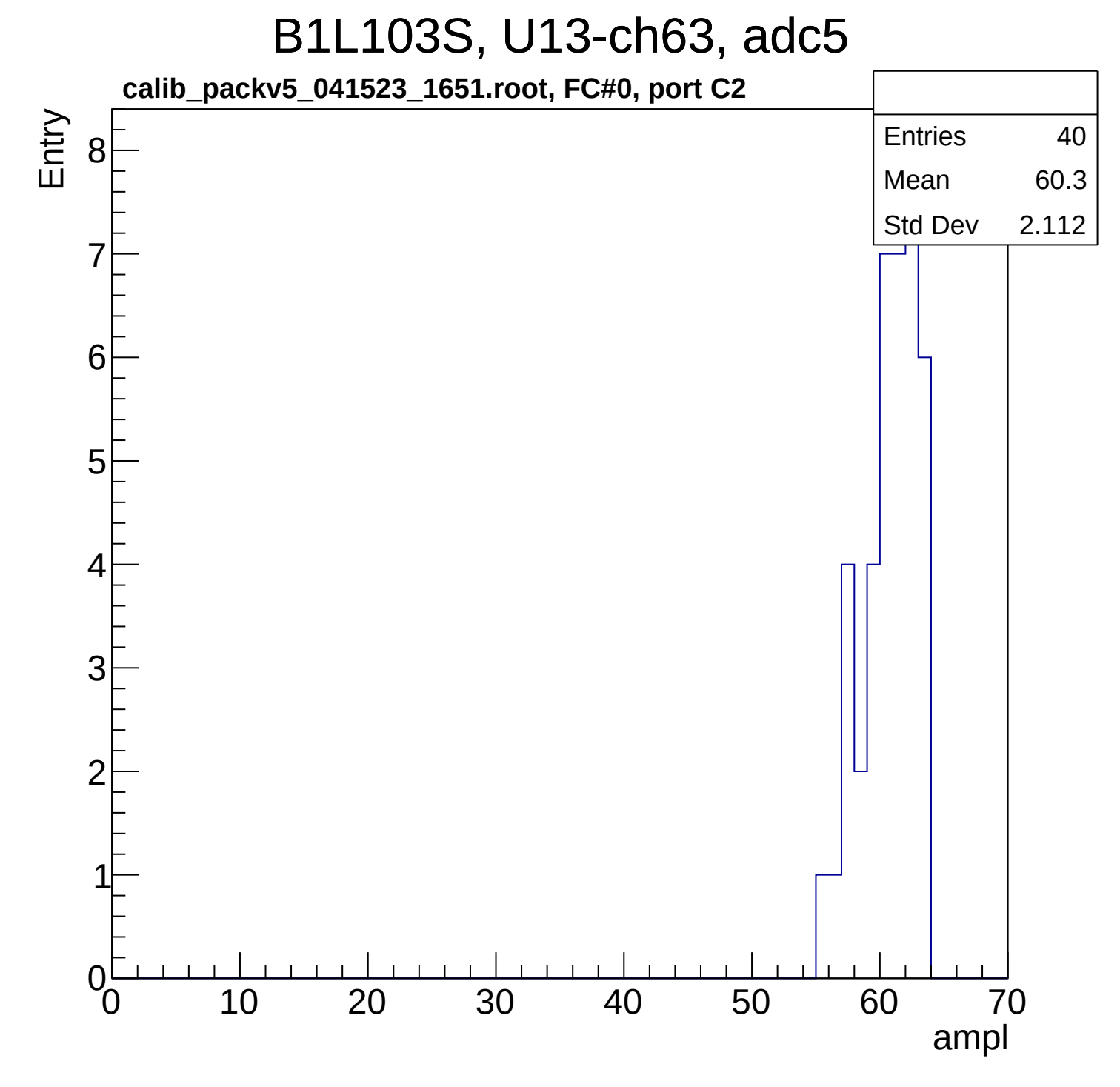

B1L103S, U13-ch63, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 27.12
Std Dev 9.84
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

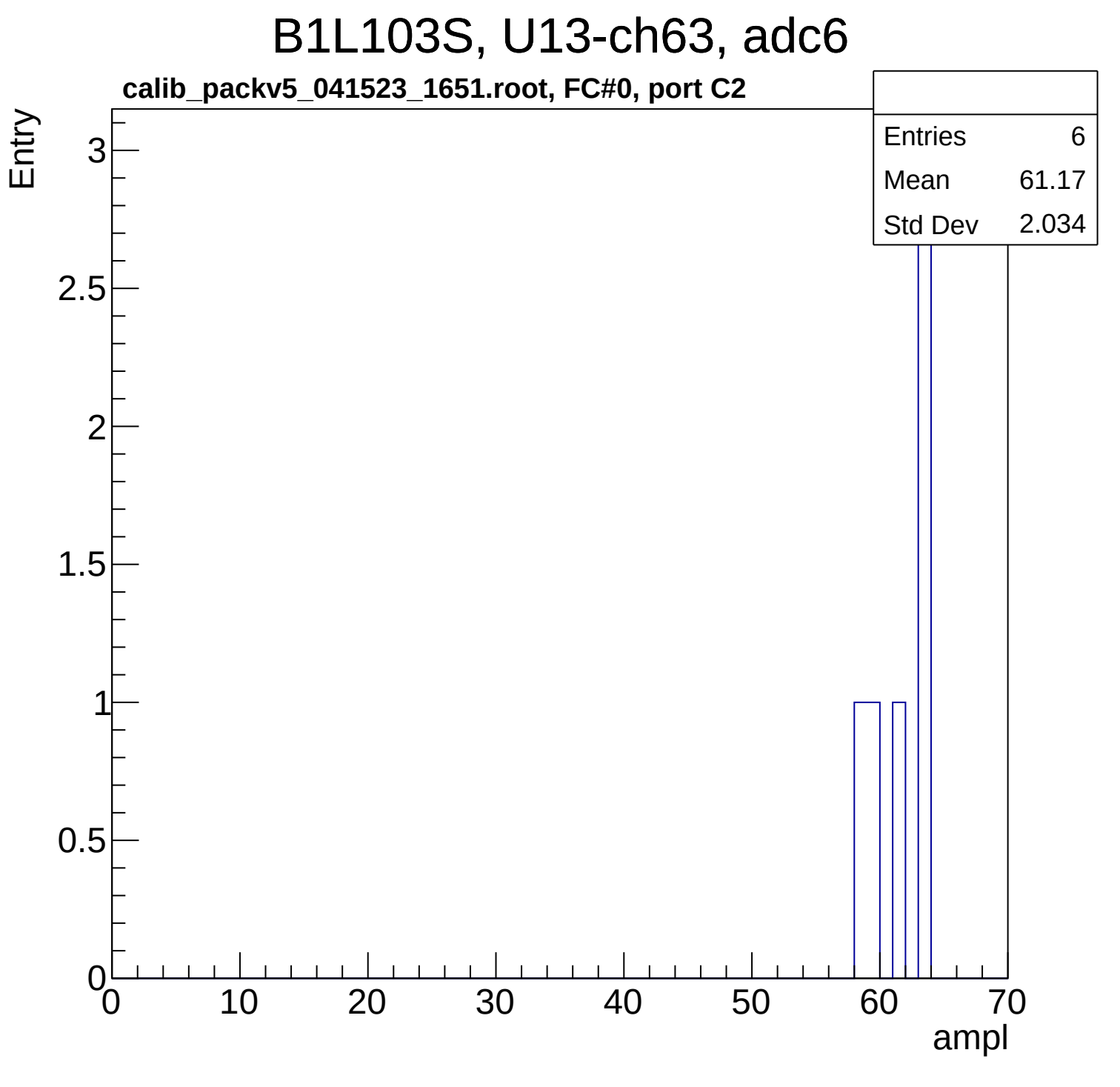

B1L103S, U13-ch63, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 31.92
Std Dev 11.38
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

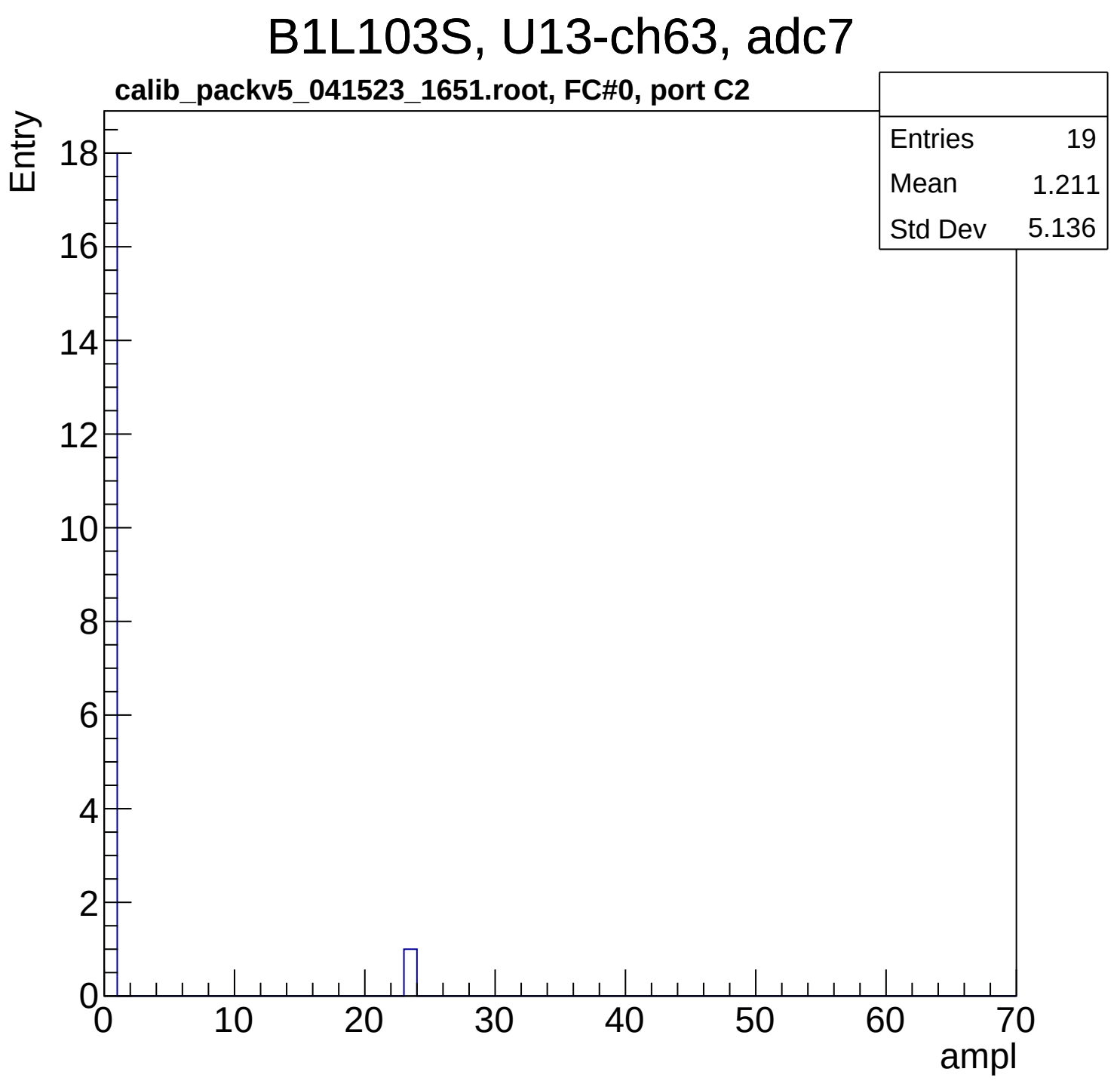

B1L103S, U13-ch63, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 42.33
Std Dev 6.094
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

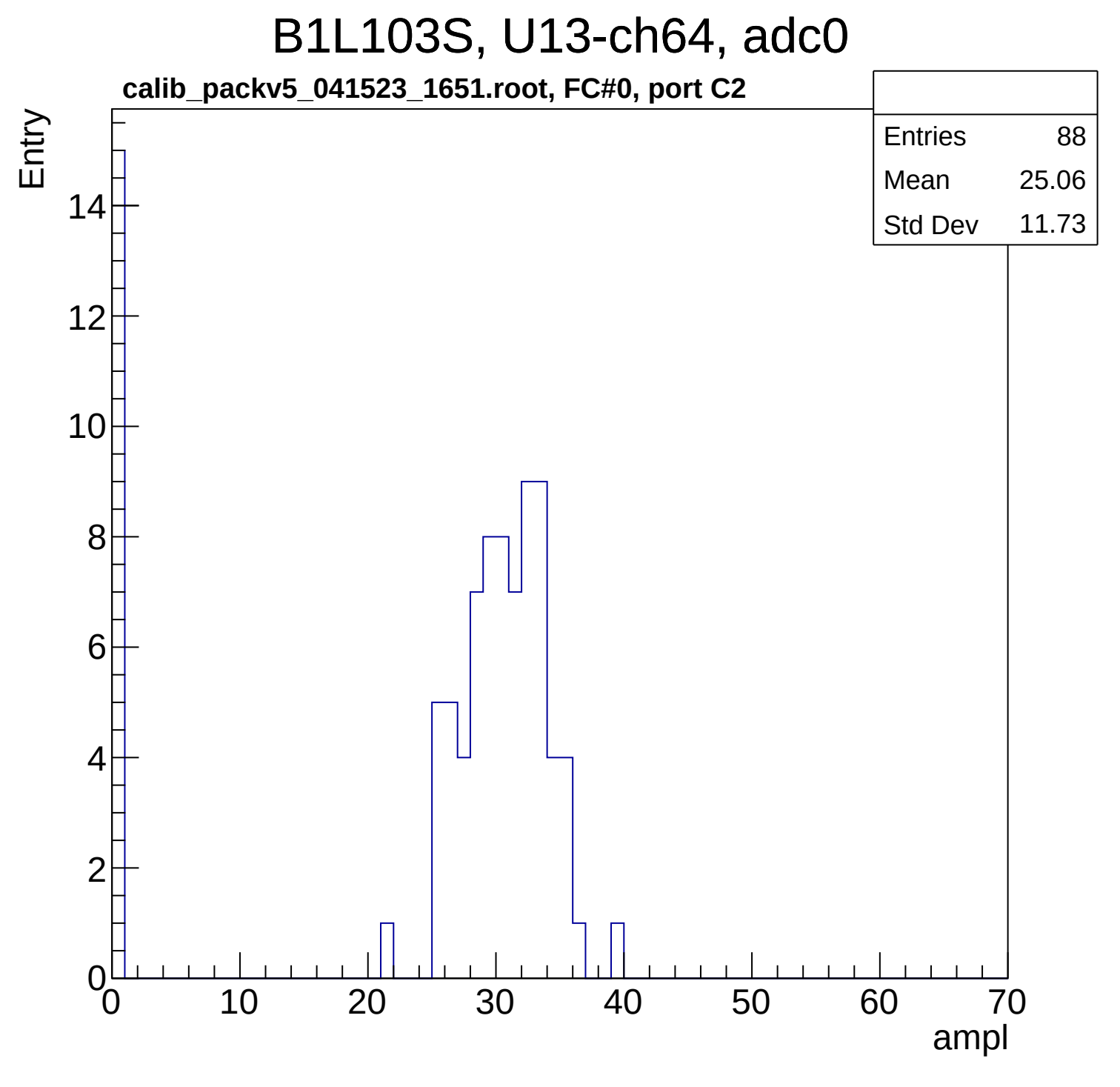

B1L103S, U13-ch63, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 50
Std Dev 3.774
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

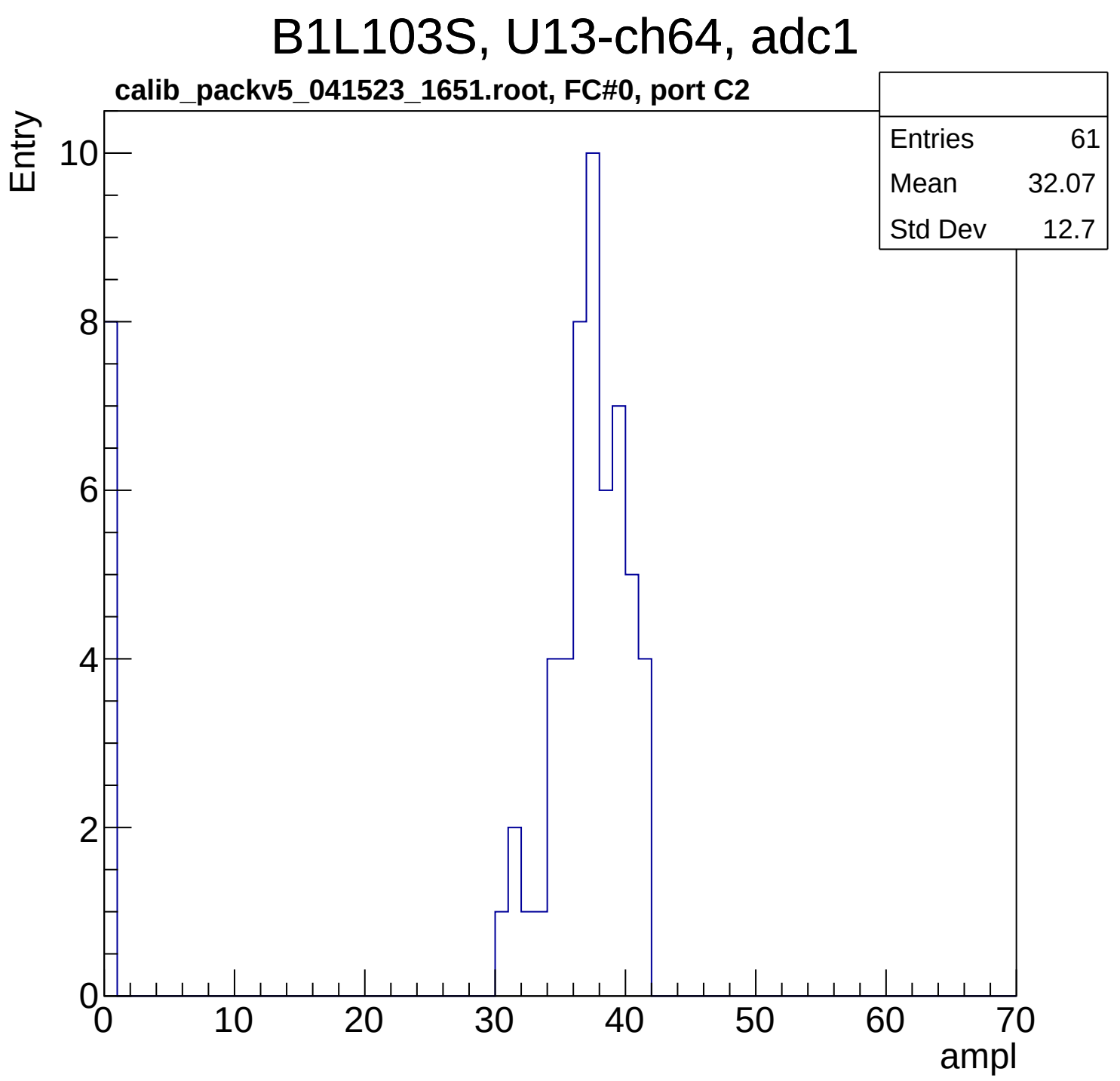

B1L103S, U13-ch63, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 53.04
Std Dev 13.08
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

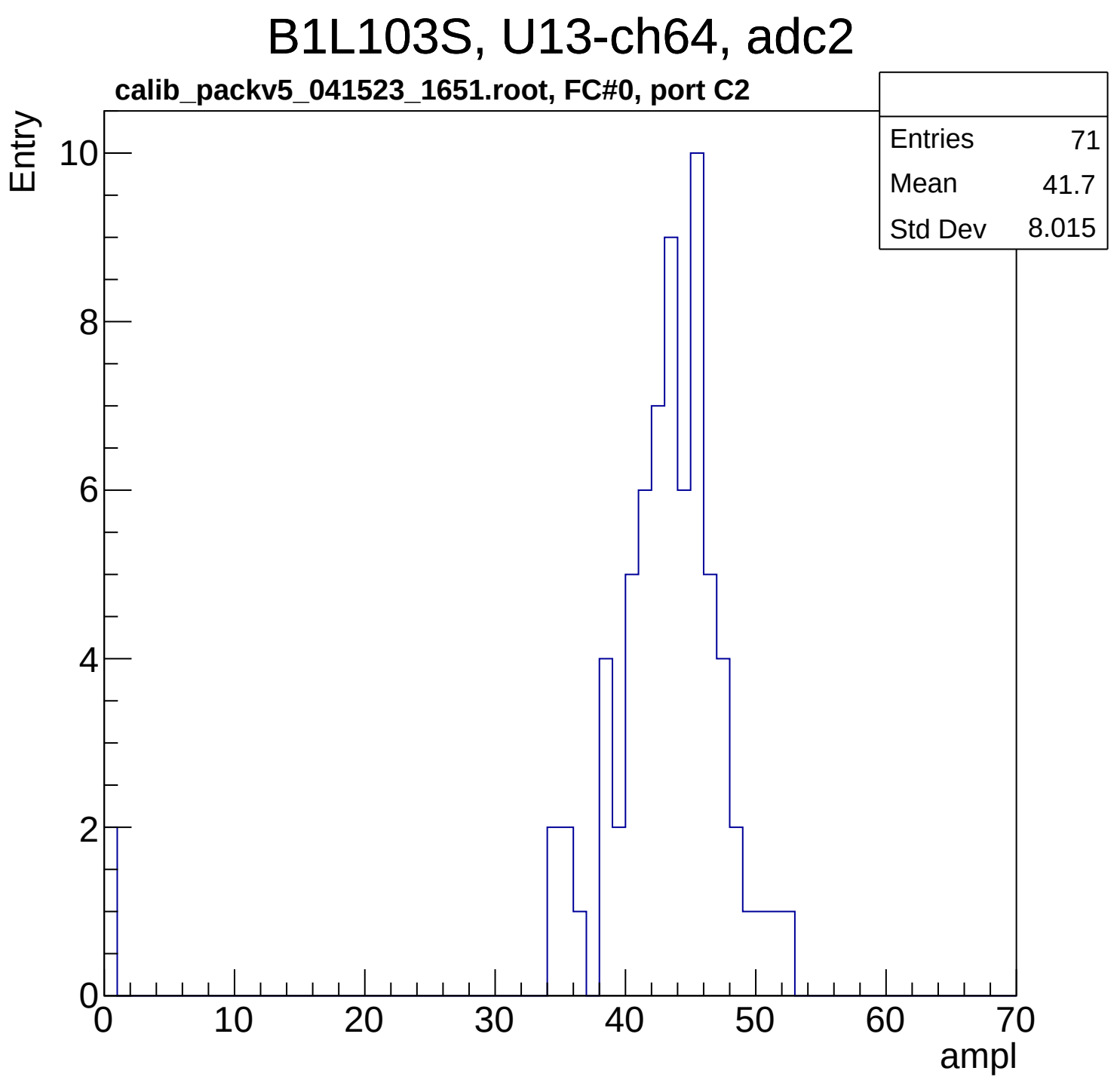

B1L103S, U13-ch63, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 60.3
Std Dev 2.112
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

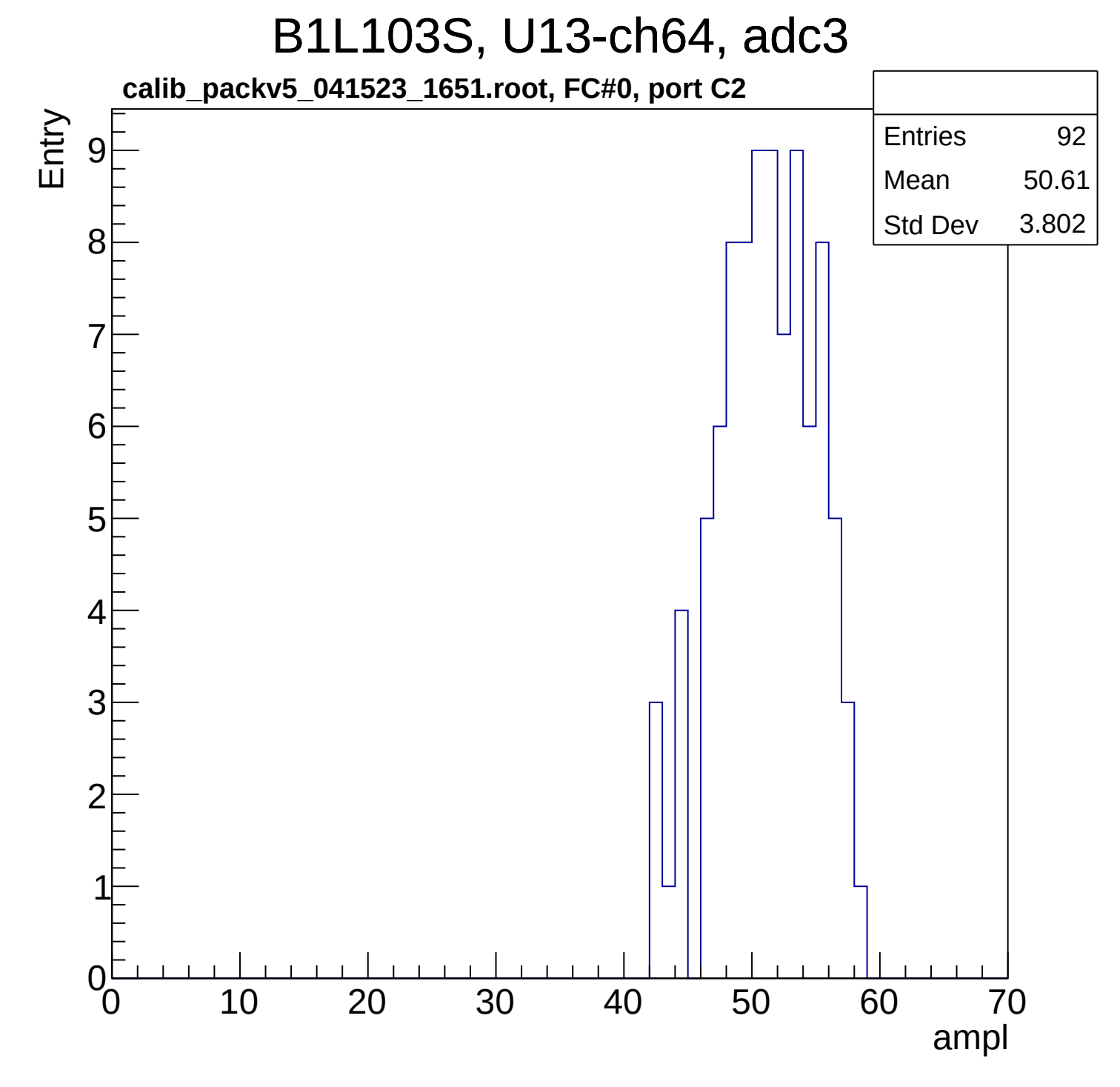

B1L103S, U13-ch63, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.17
Std Dev 2.034
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U13-ch63, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.211
Std Dev 5.136
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch64, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 25.06
Std Dev 11.73
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch64, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 32.07
Std Dev 12.7
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch64, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 41.7
Std Dev 8.015
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch64, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 50.61
Std Dev 3.802
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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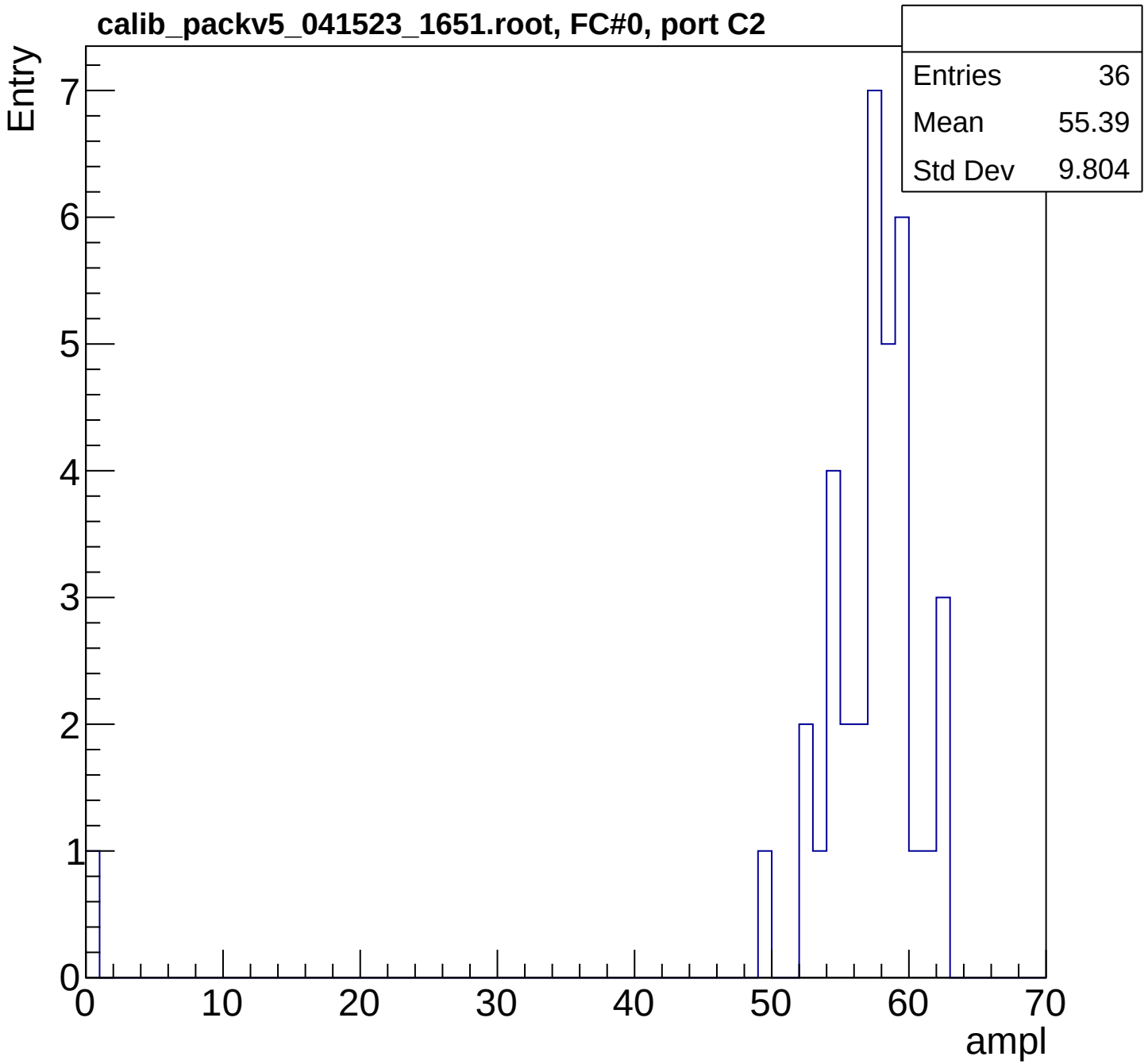
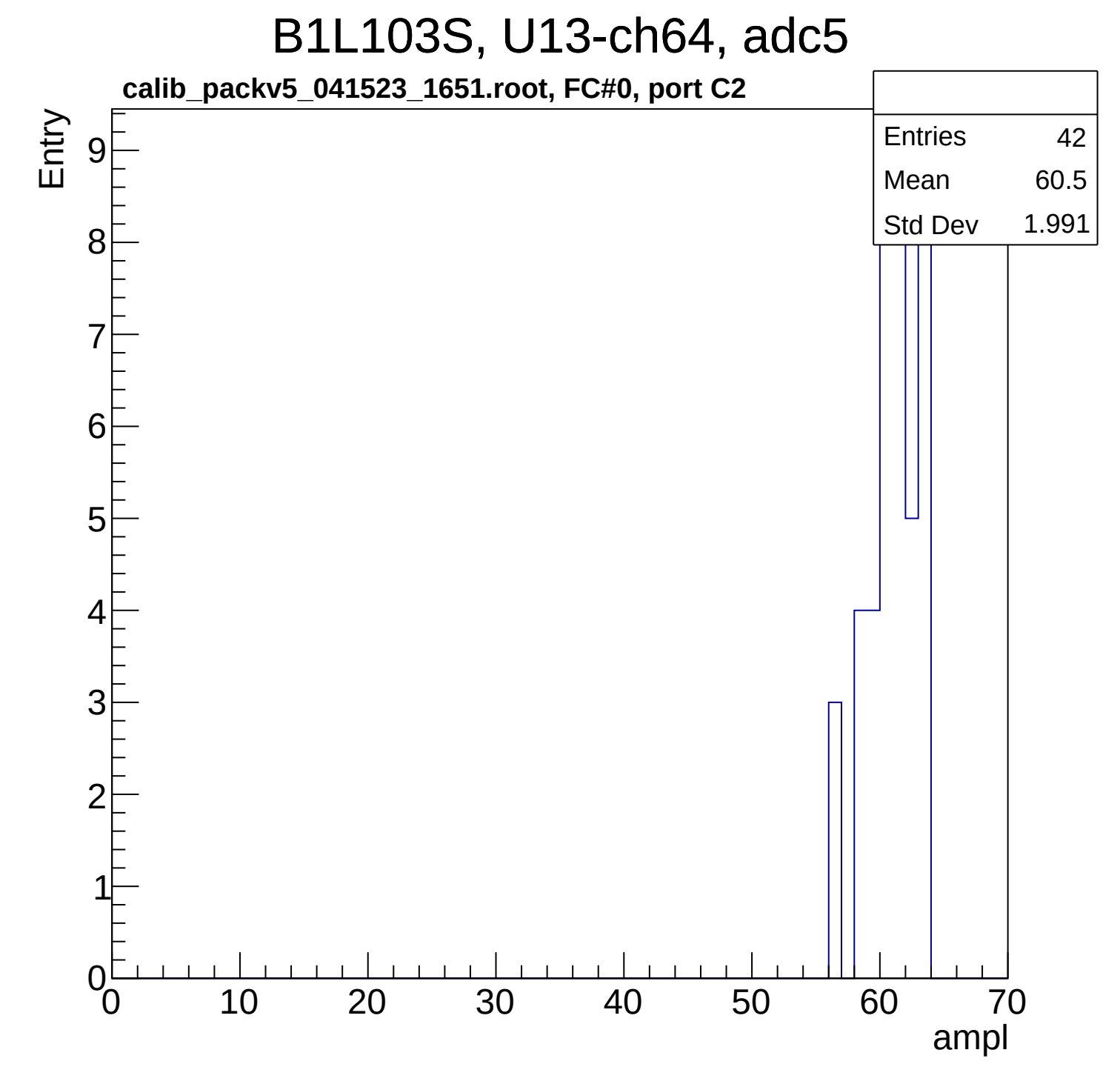
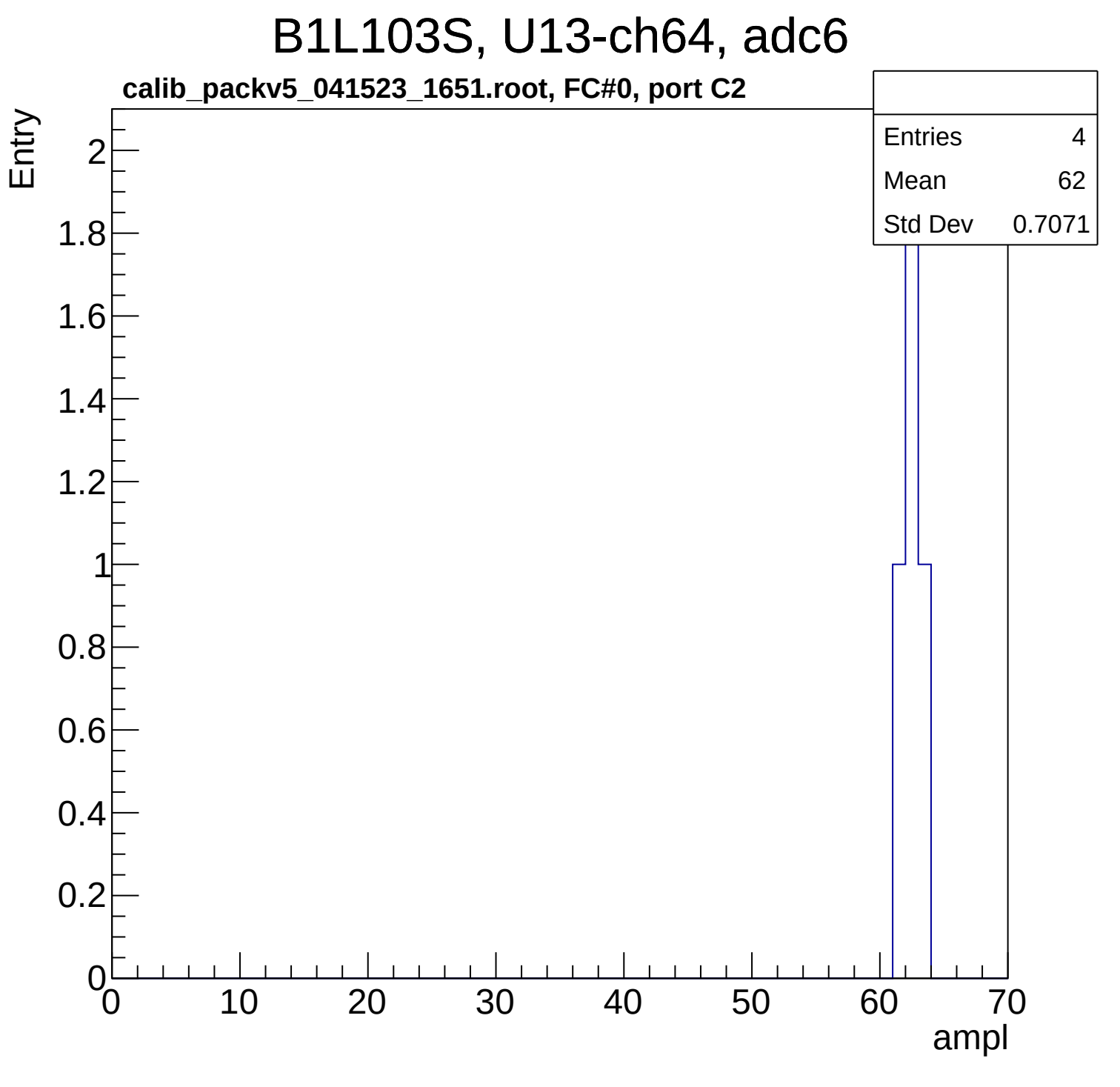
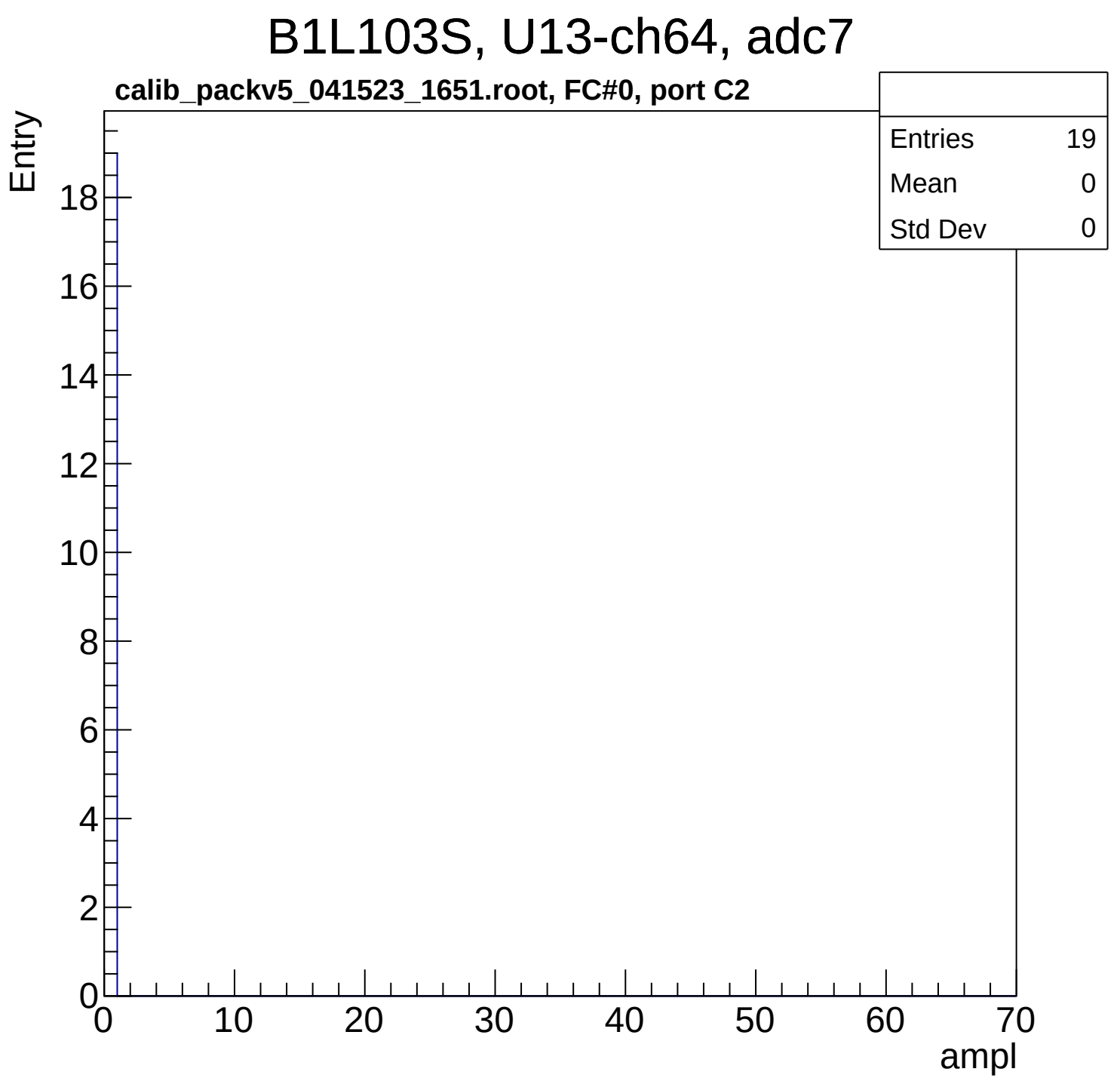
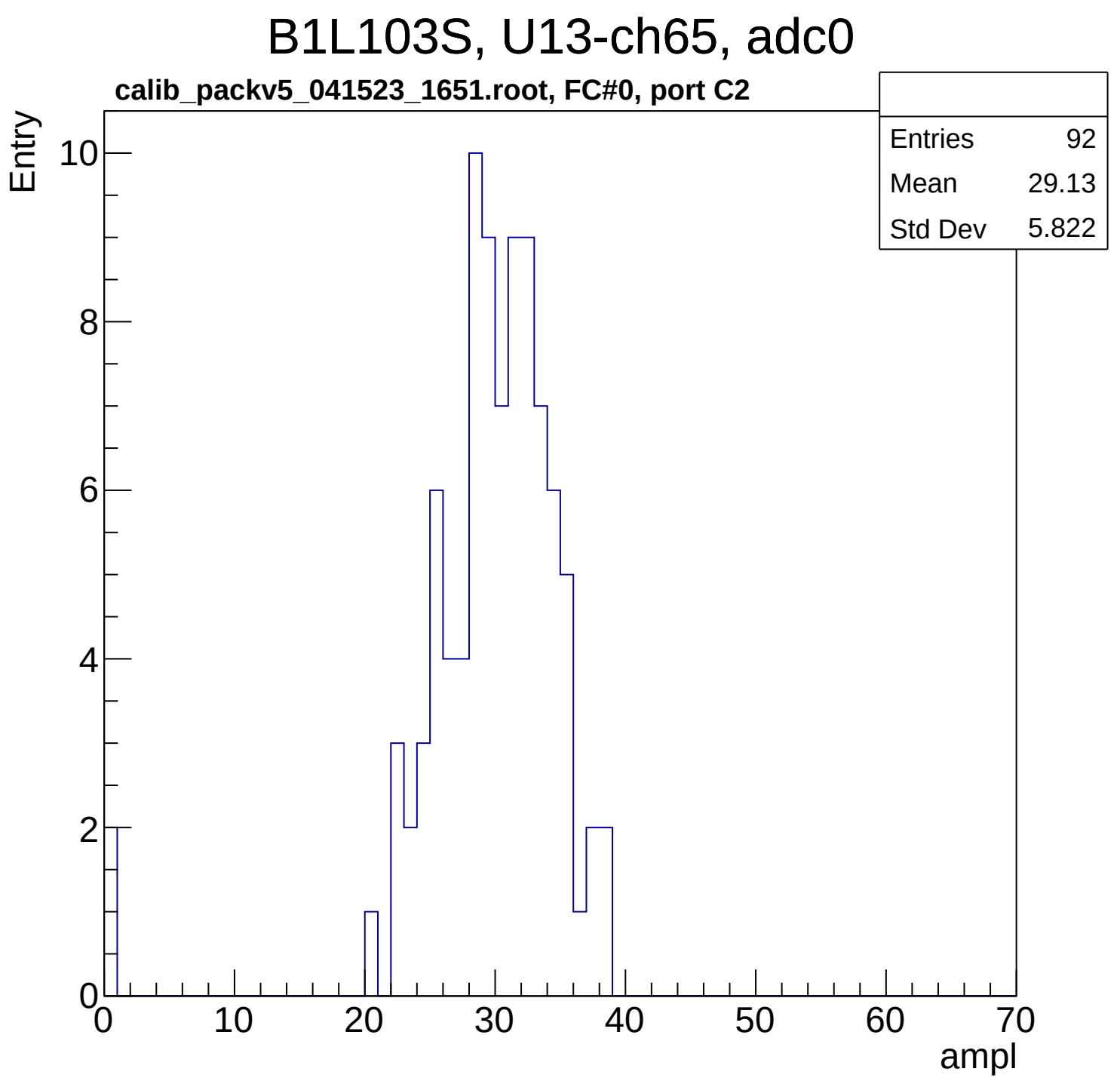
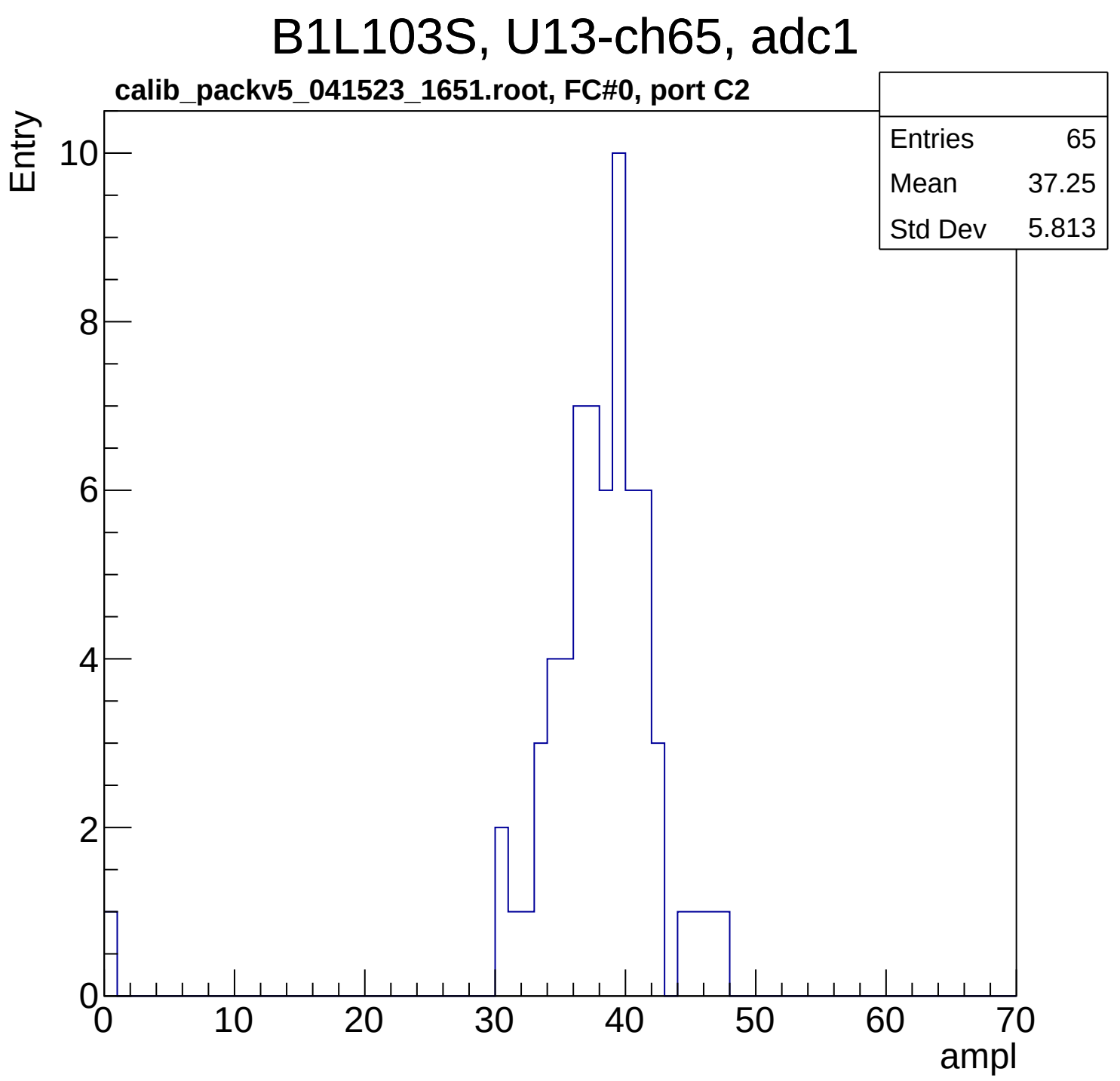

B1L103S, U13-ch64, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 55.39
Std Dev 9.804
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

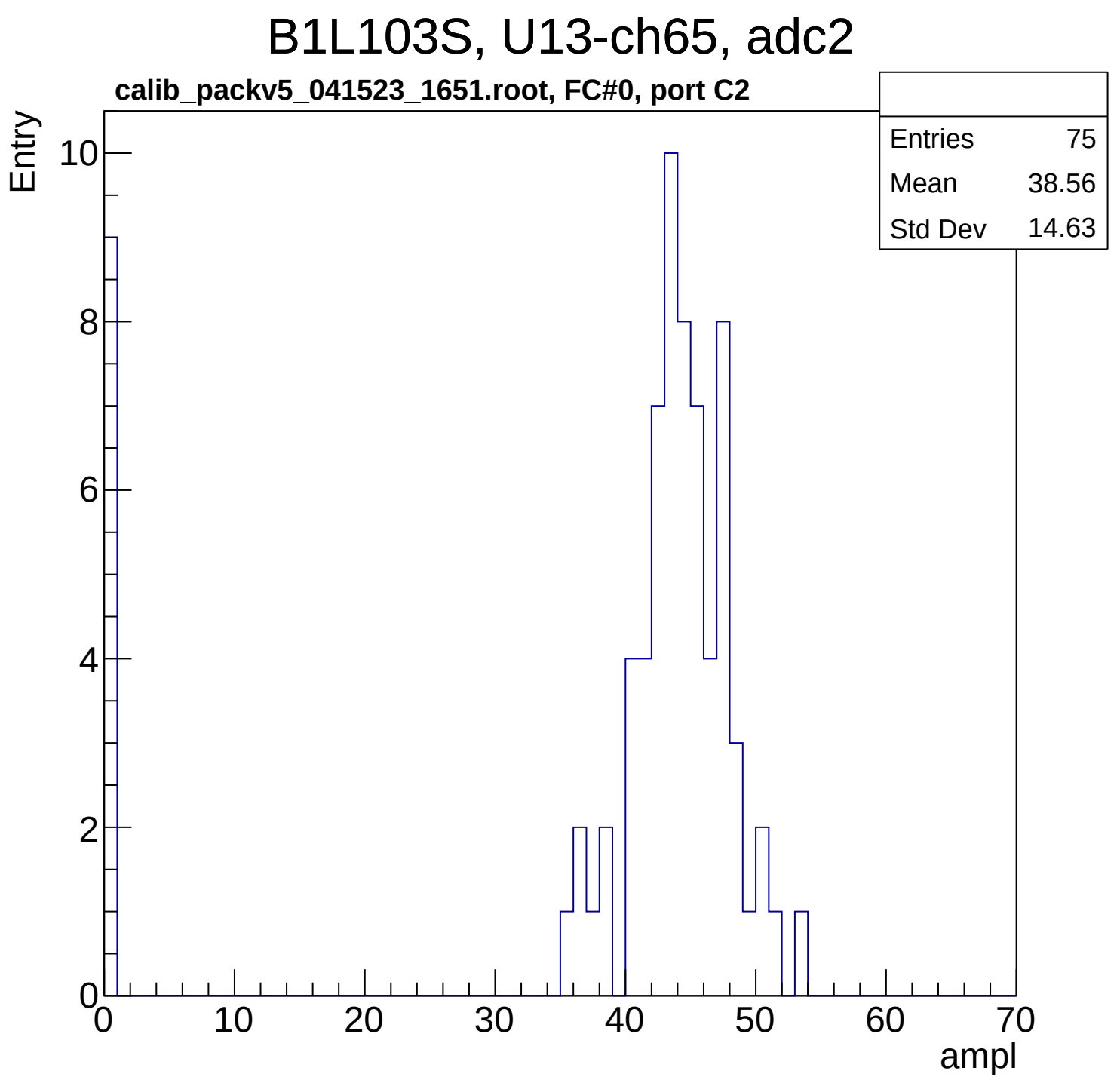

B1L103S, U13-ch64, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 60.5
Std Dev 1.991
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

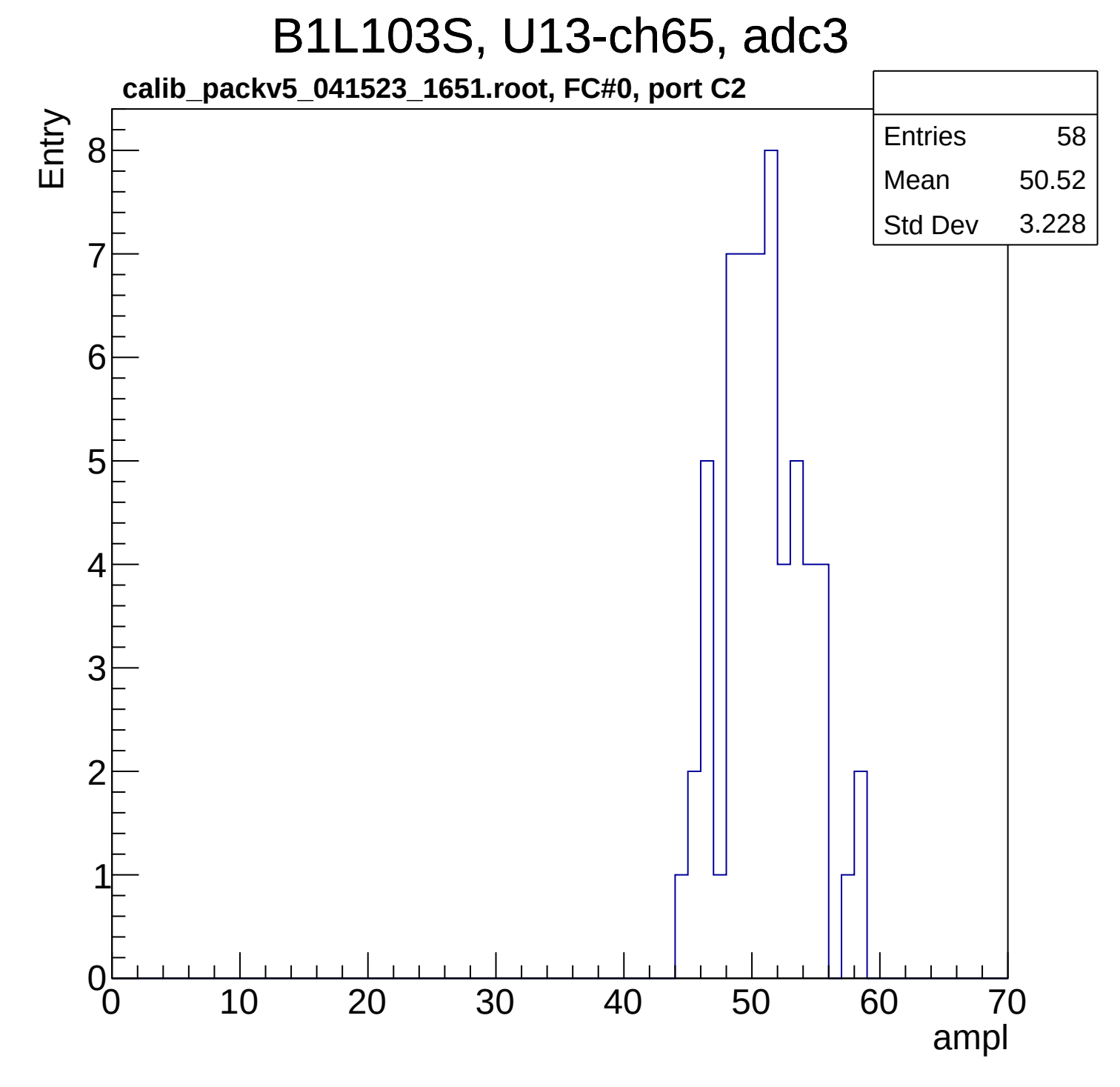

B1L103S, U13-ch64, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62
Std Dev 0.7071
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

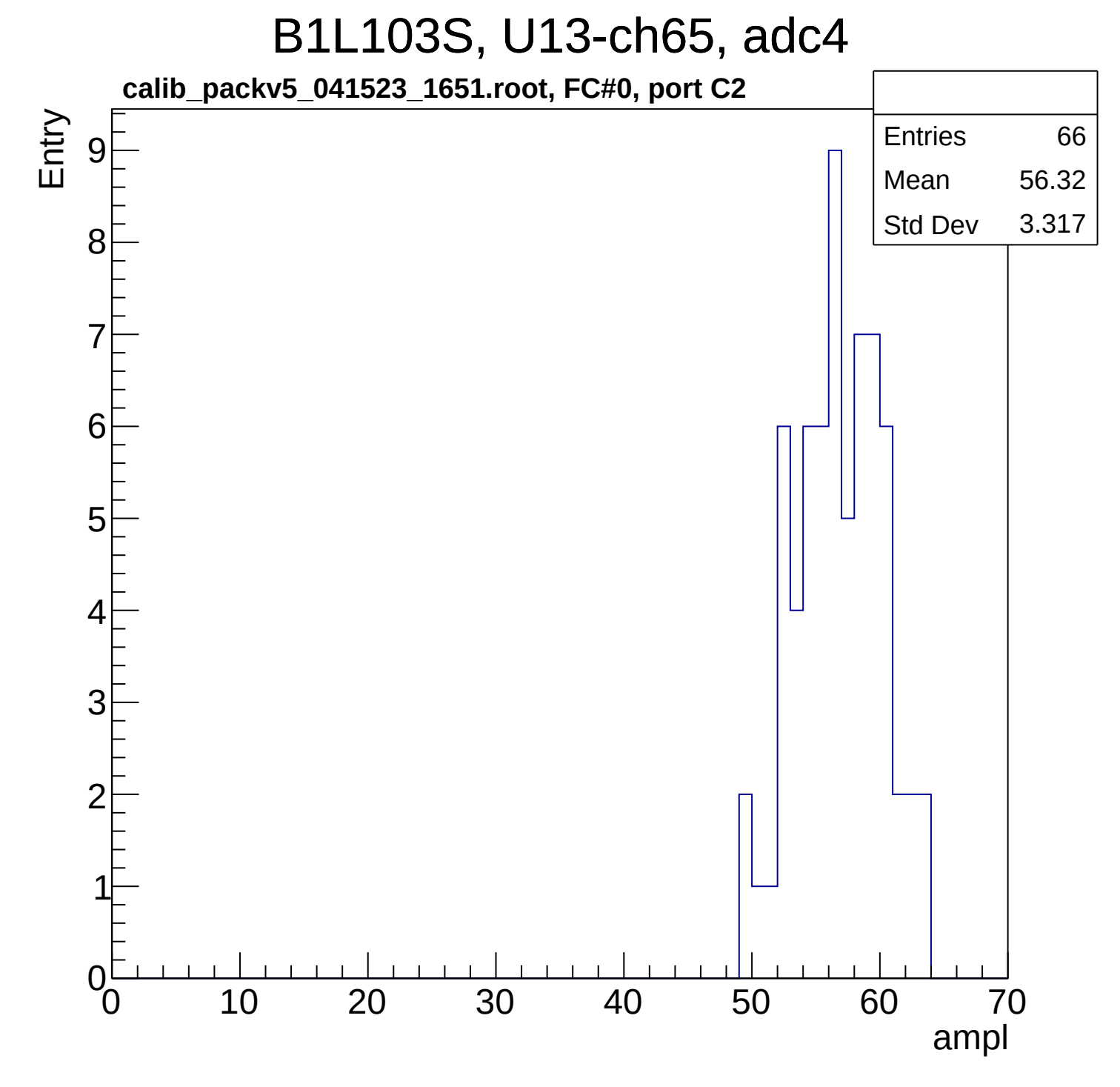

B1L103S, U13-ch64, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch65, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 29.13
Std Dev 5.822
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch65, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 37.25
Std Dev 5.813
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch65, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 38.56
Std Dev 14.63
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch65, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 50.52
Std Dev 3.228
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch65, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 56.32
Std Dev 3.317
Entry
ampl
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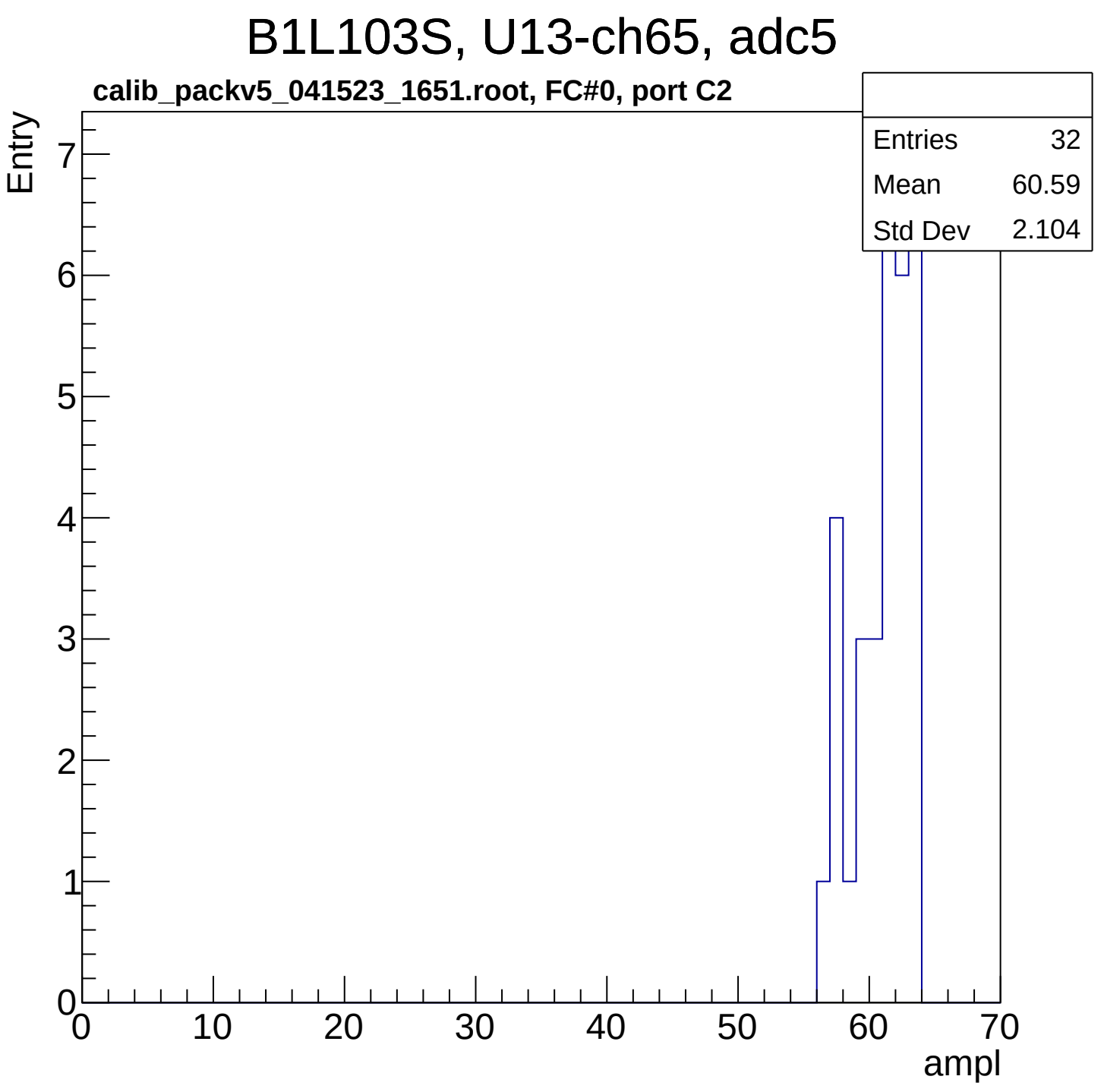
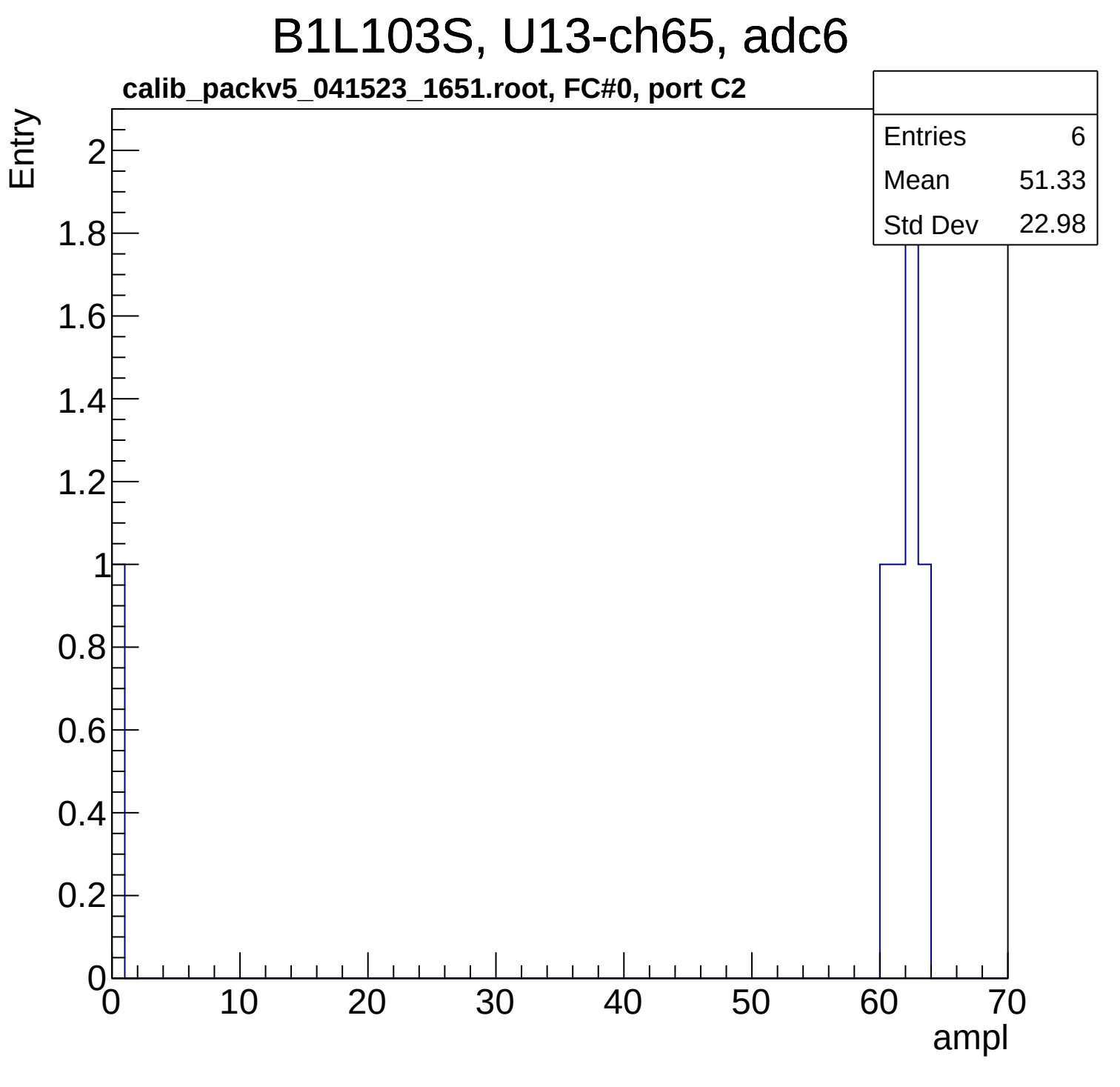
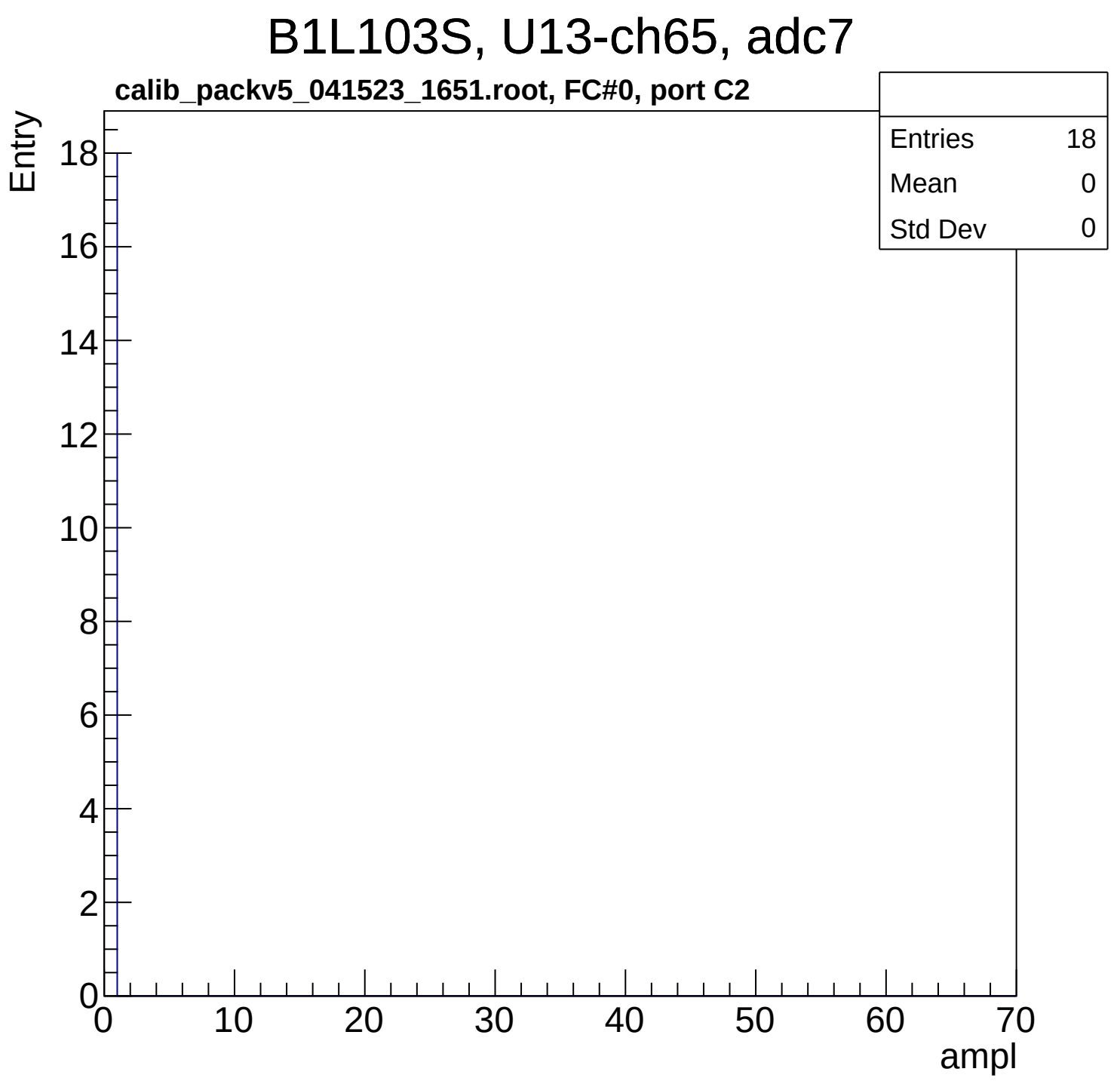
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch65, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 60.59
Std Dev 2.104
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch65, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 51.33
Std Dev 22.98
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U13-ch65, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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10
20
30
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50
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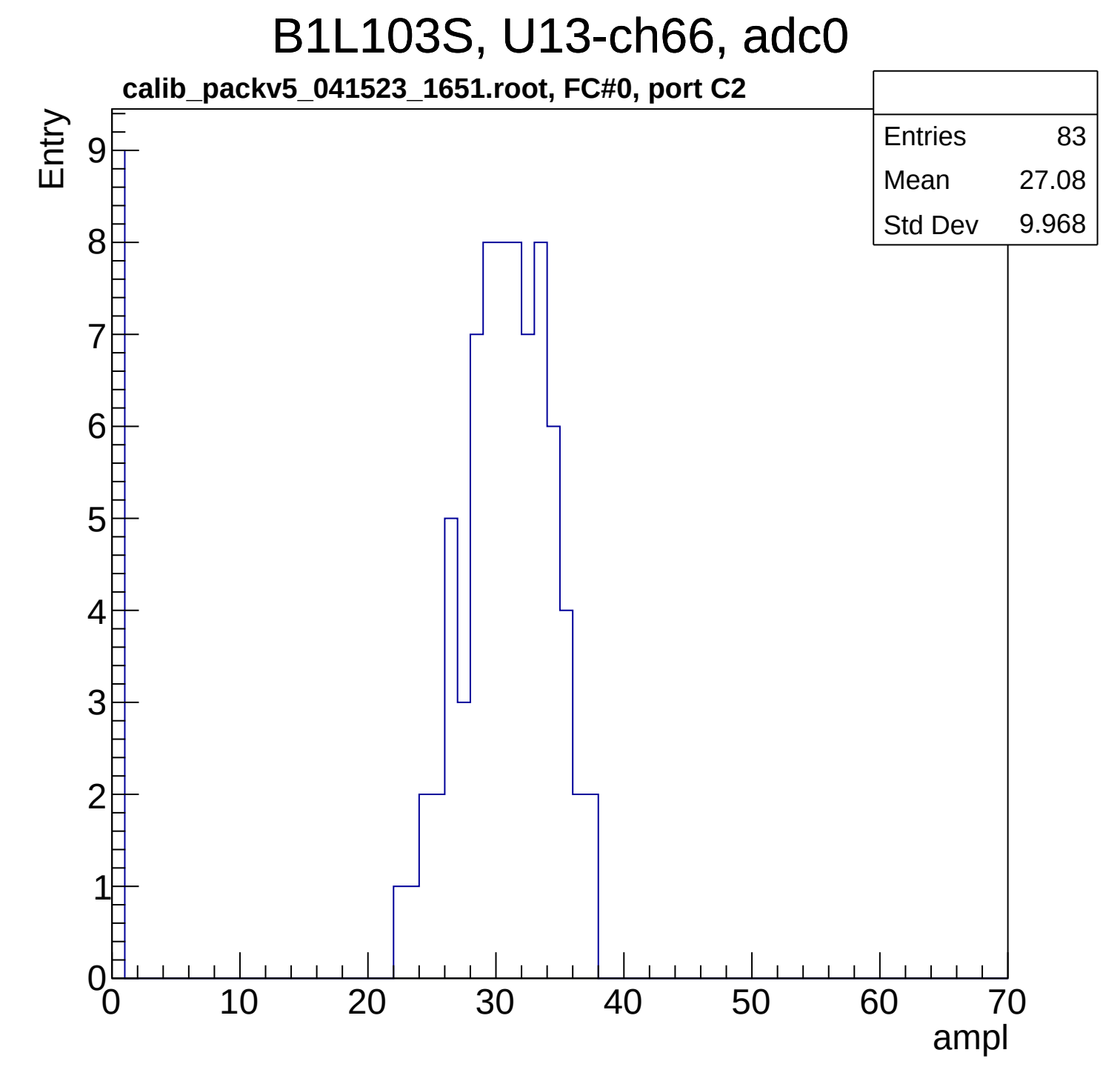
70
ampl


B1L103S, U13-ch66, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 27.08
Std Dev 9.968
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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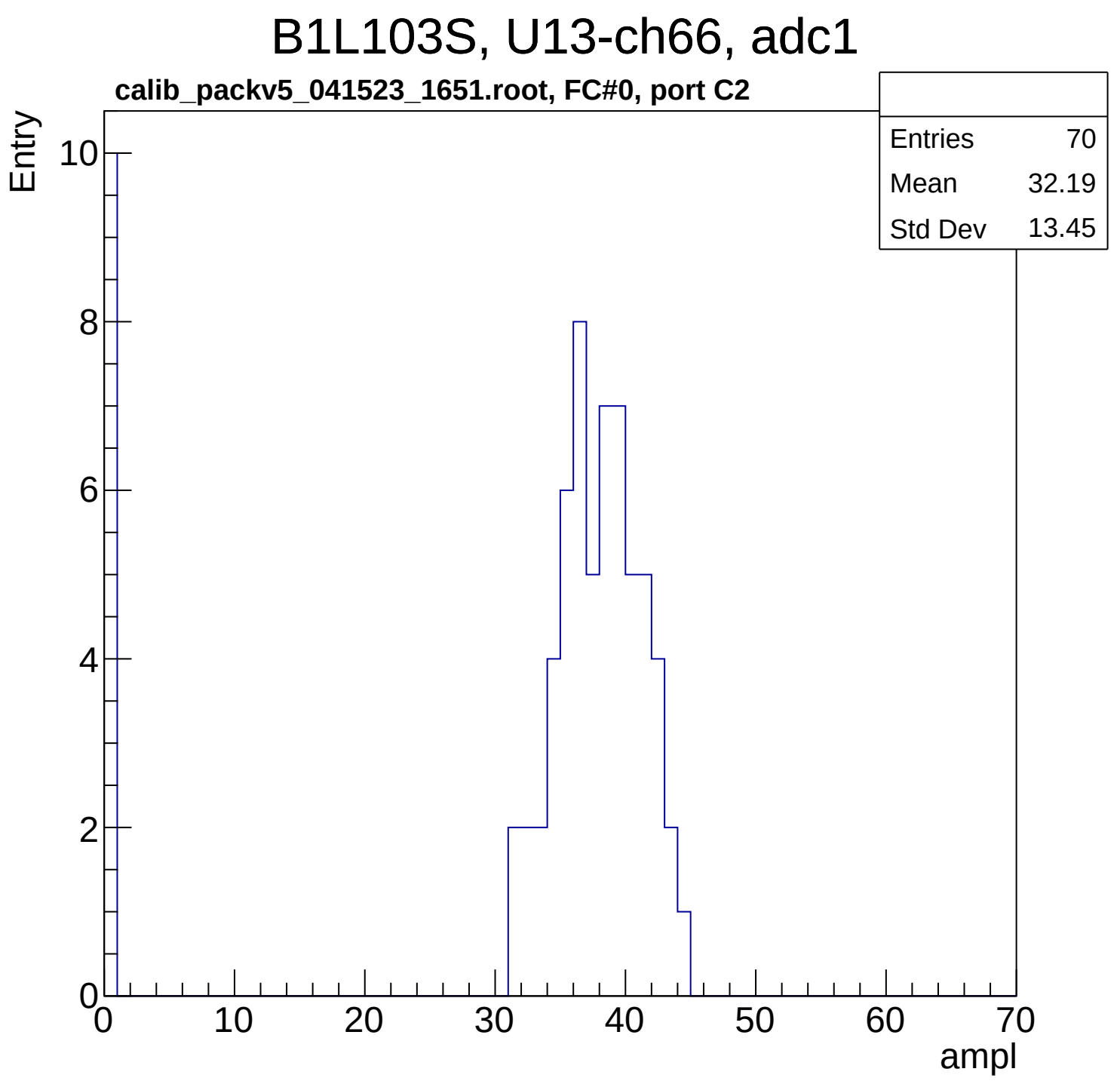
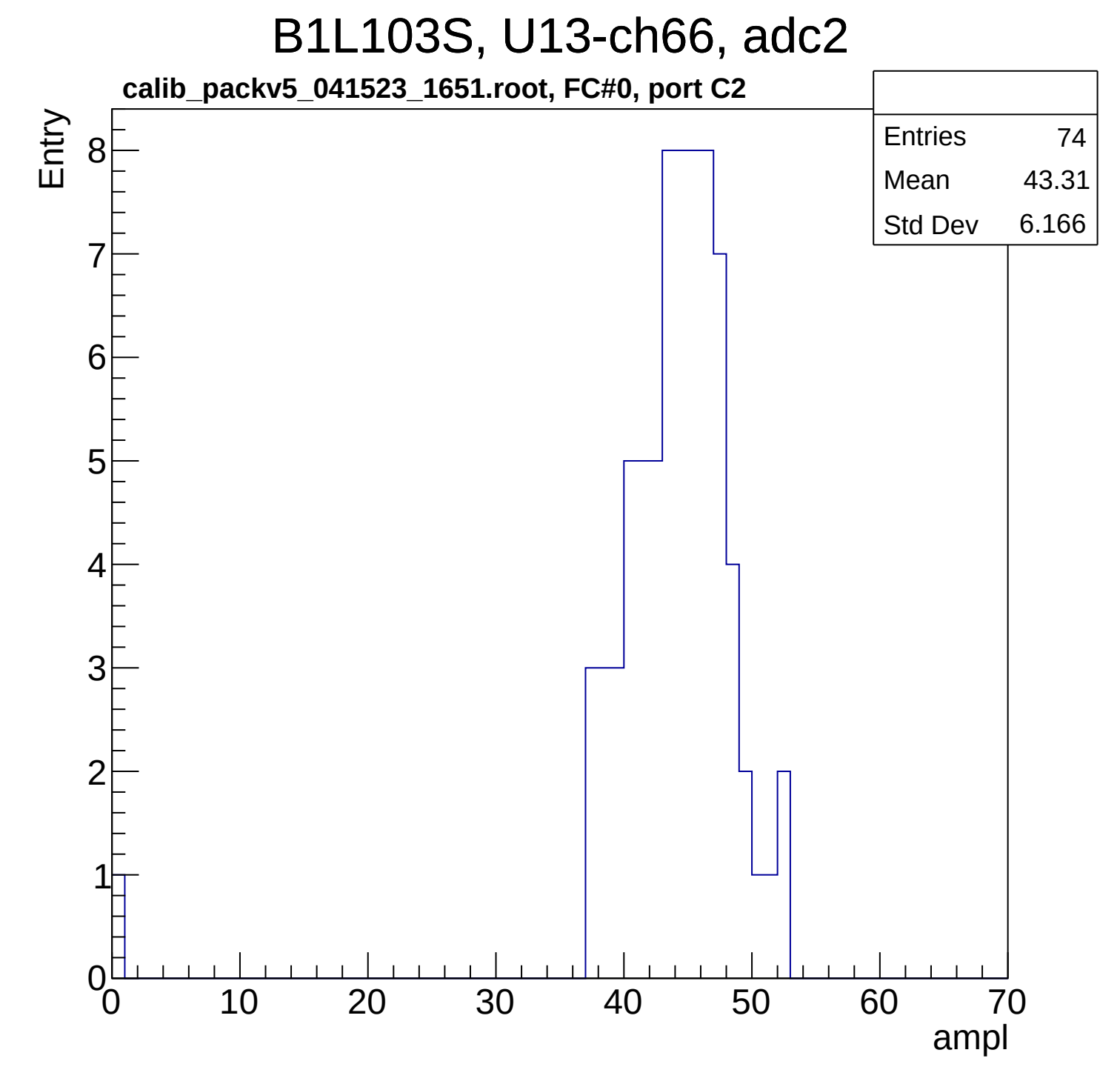

B1L103S, U13-ch66, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 32.19
Std Dev 13.45
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch66, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 43.31
Std Dev 6.166
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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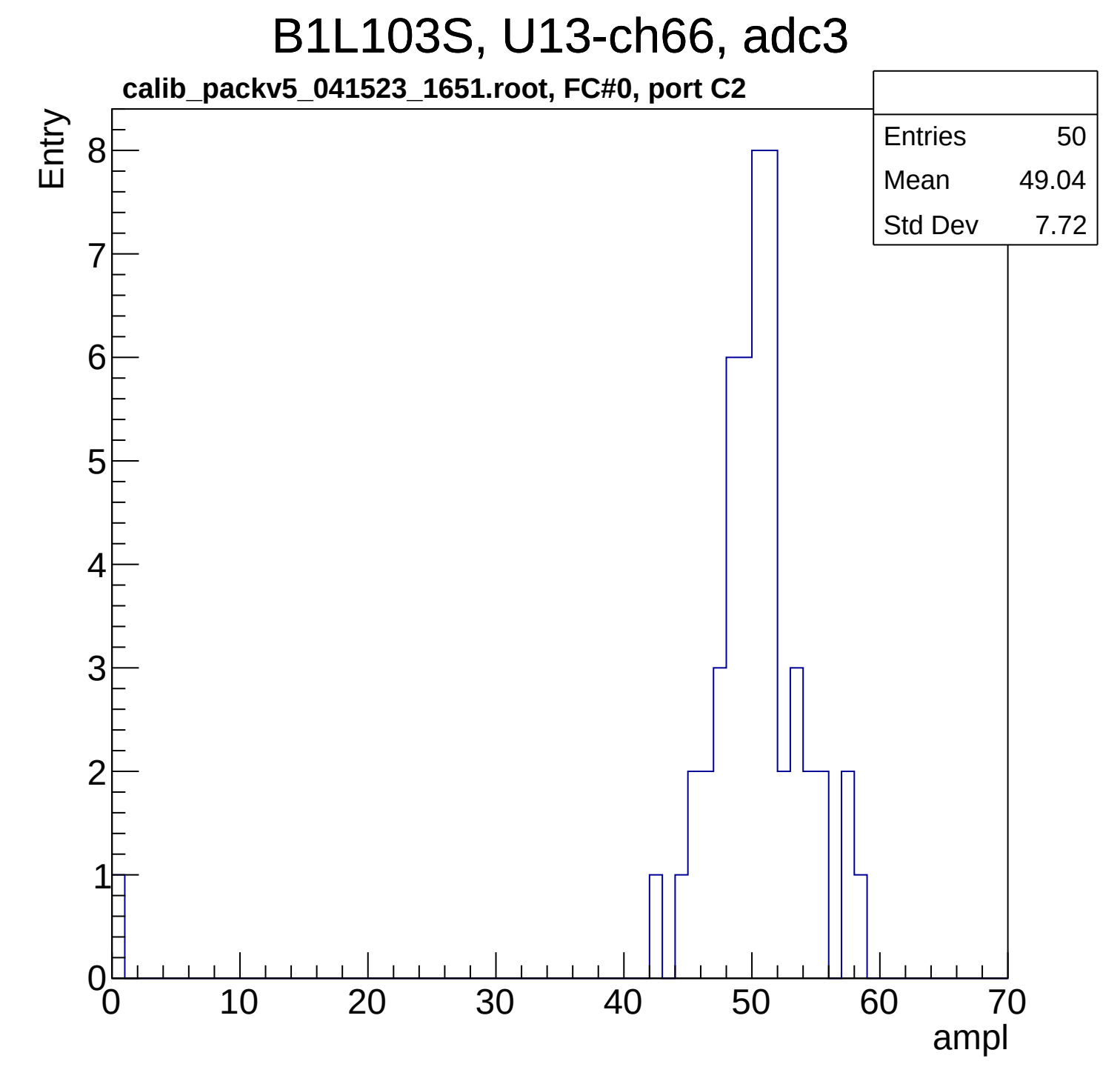
B1L103S, U13-ch66, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 49.04
Std Dev 7.72
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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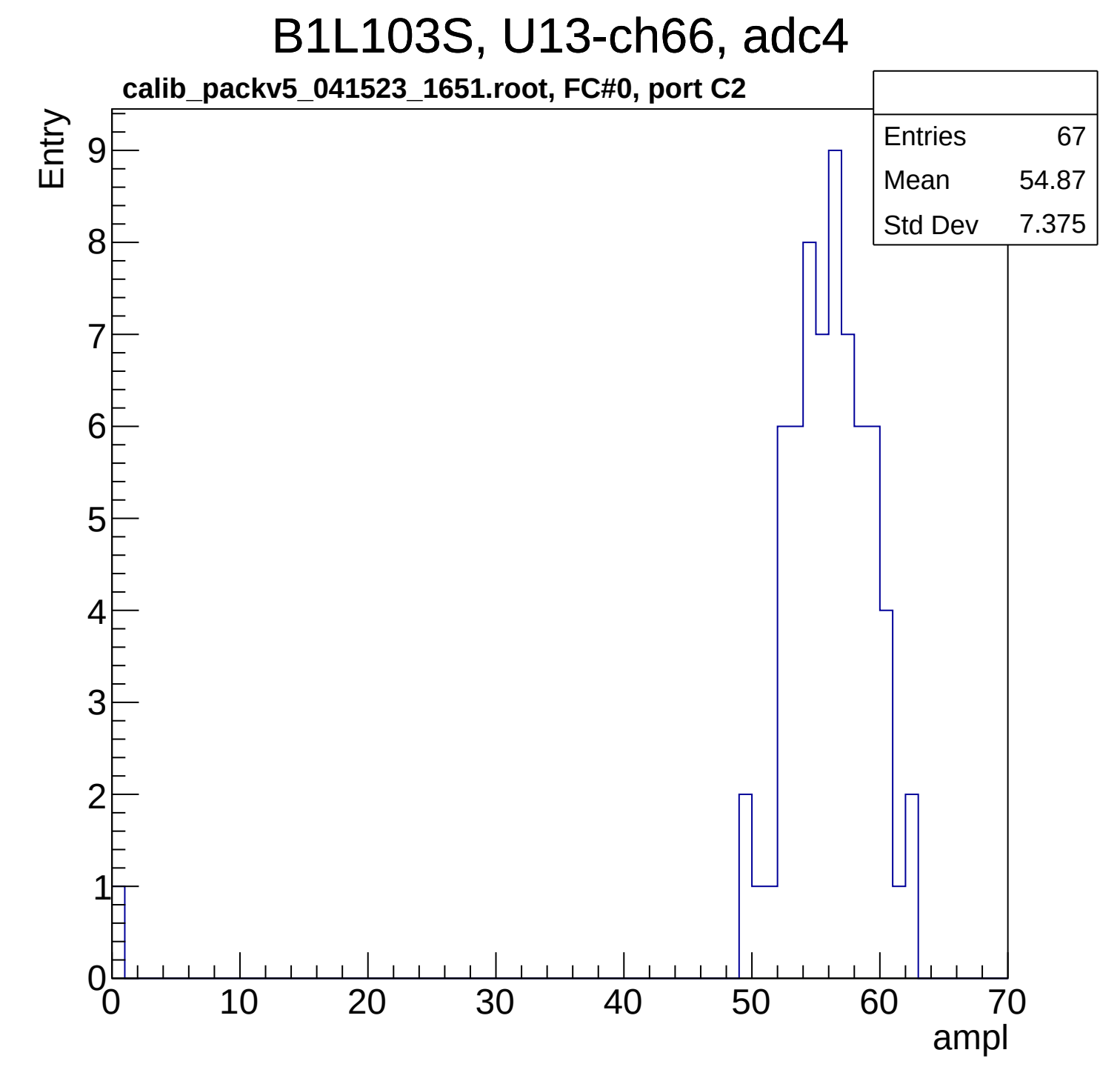
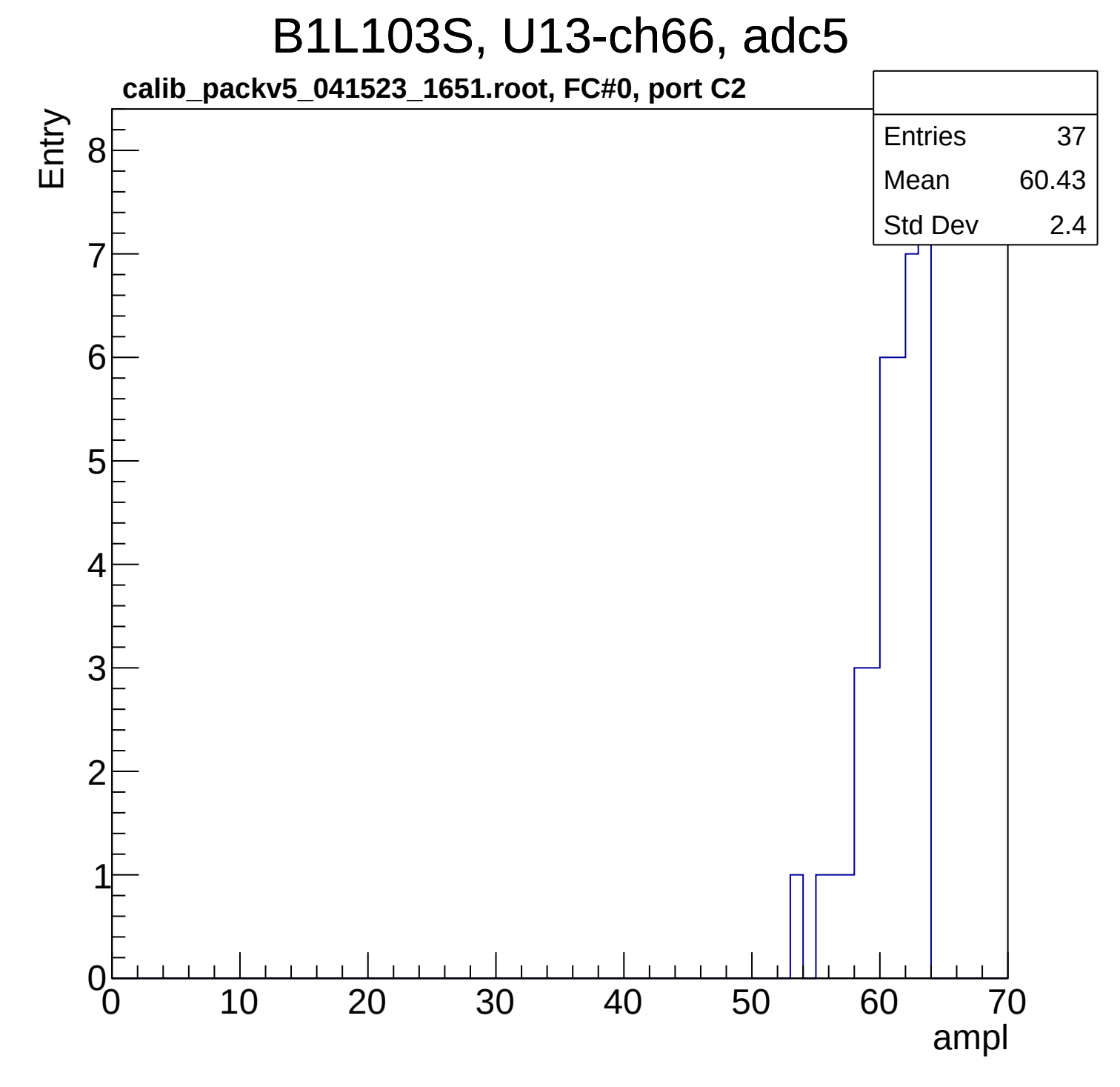
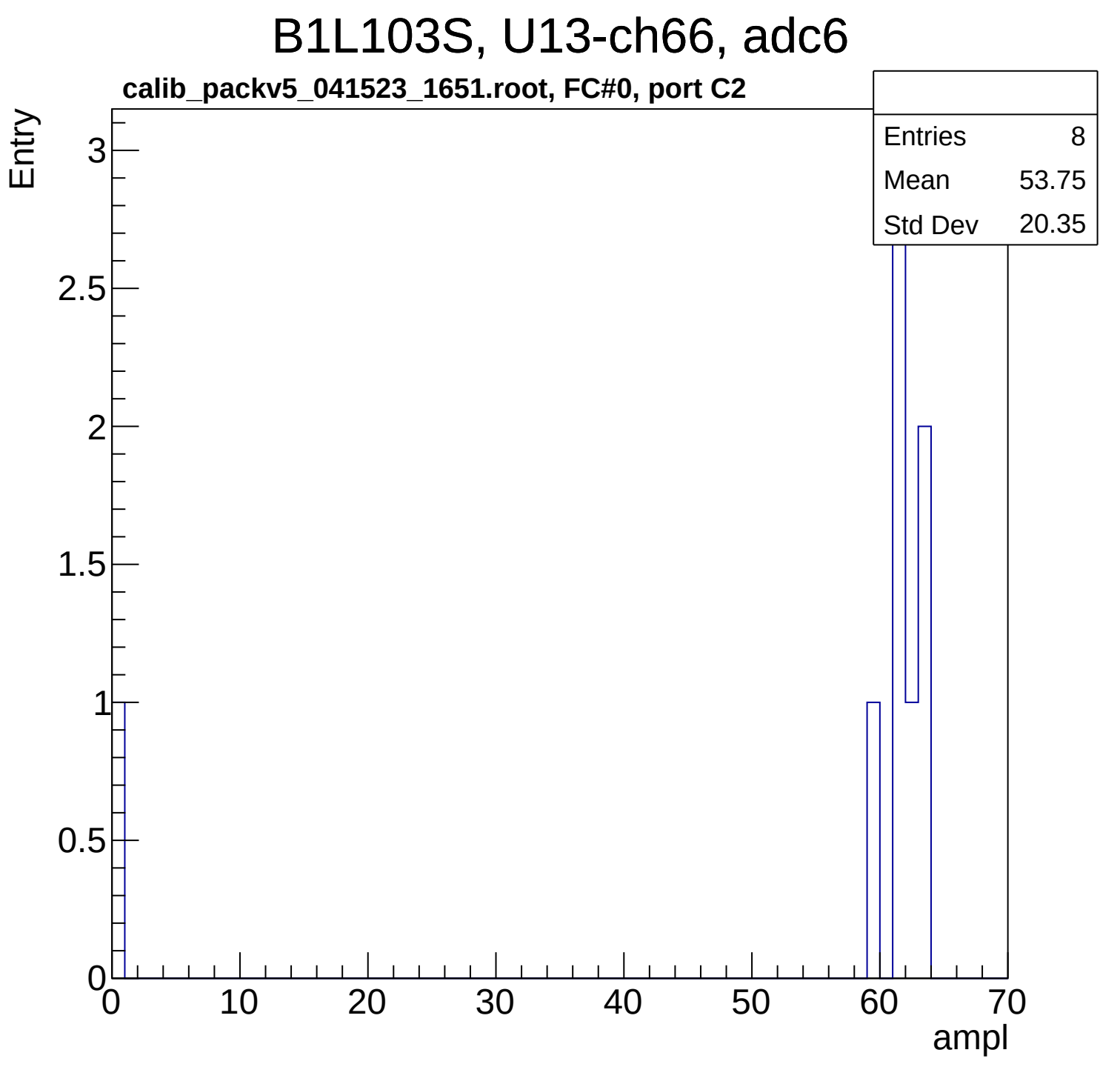

B1L103S, U13-ch66, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 54.87
Std Dev 7.375
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch66, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 60.43
Std Dev 2.4
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch66, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 53.75
Std Dev 20.35
Entry
ampl
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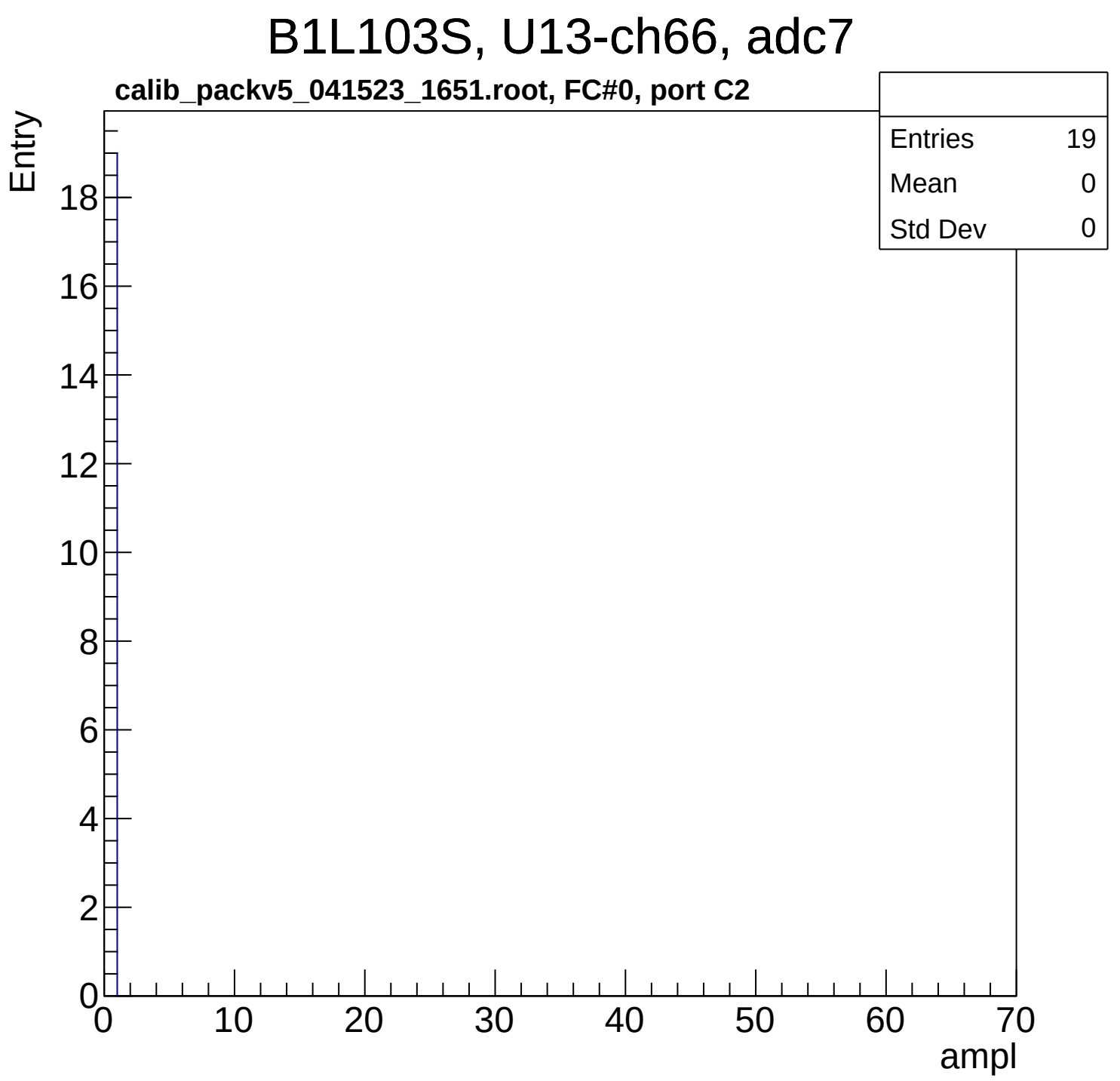
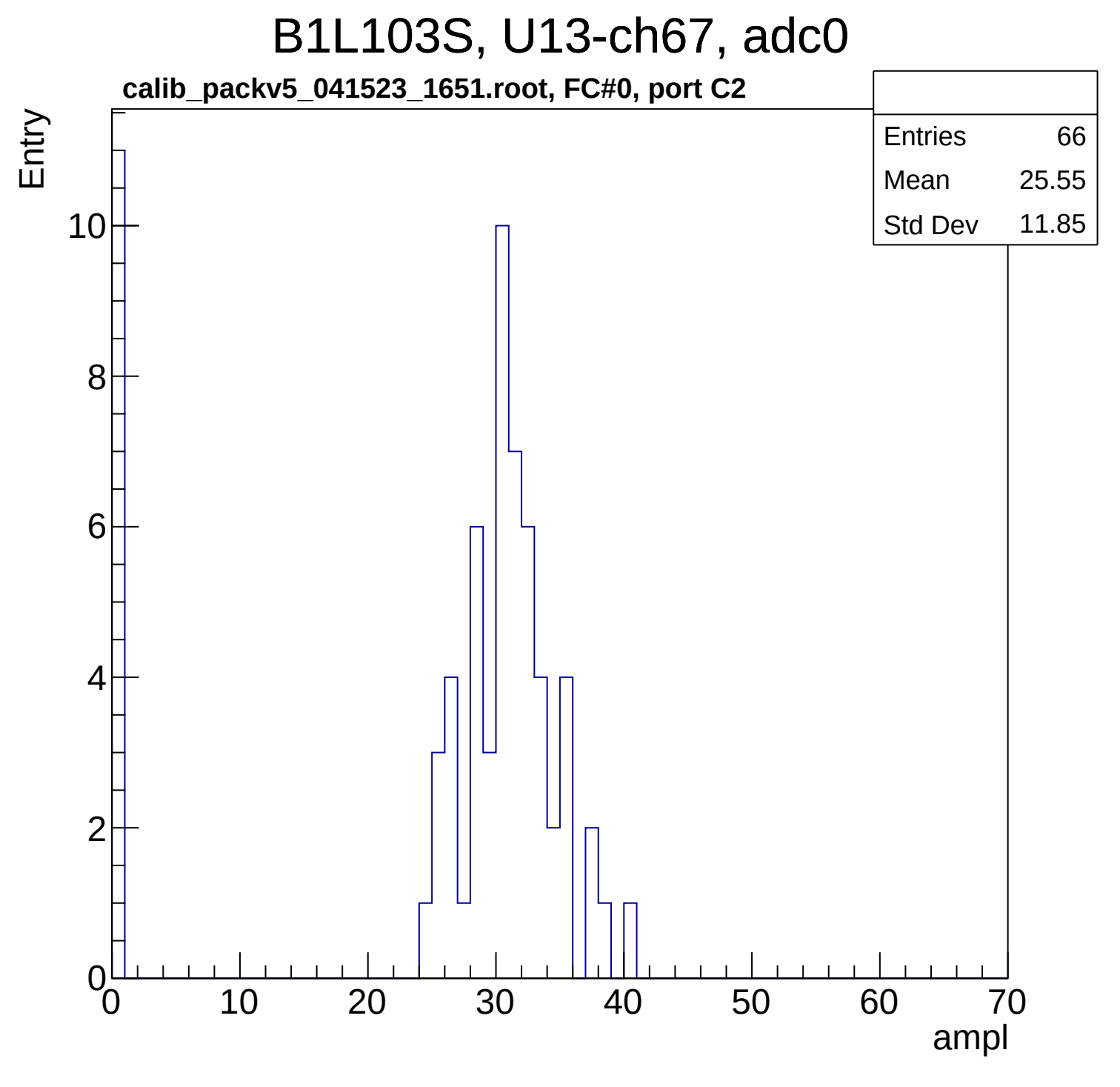
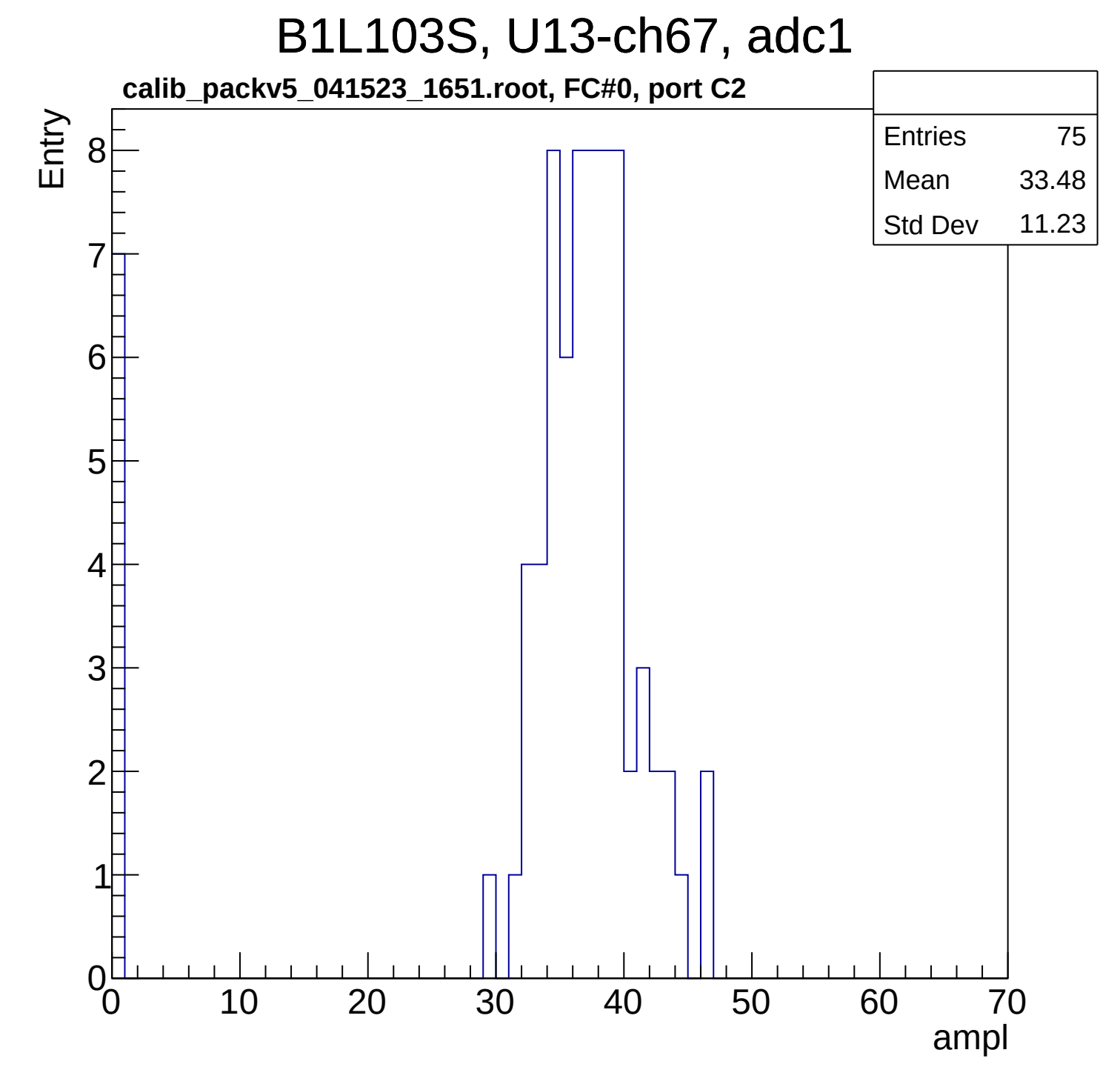
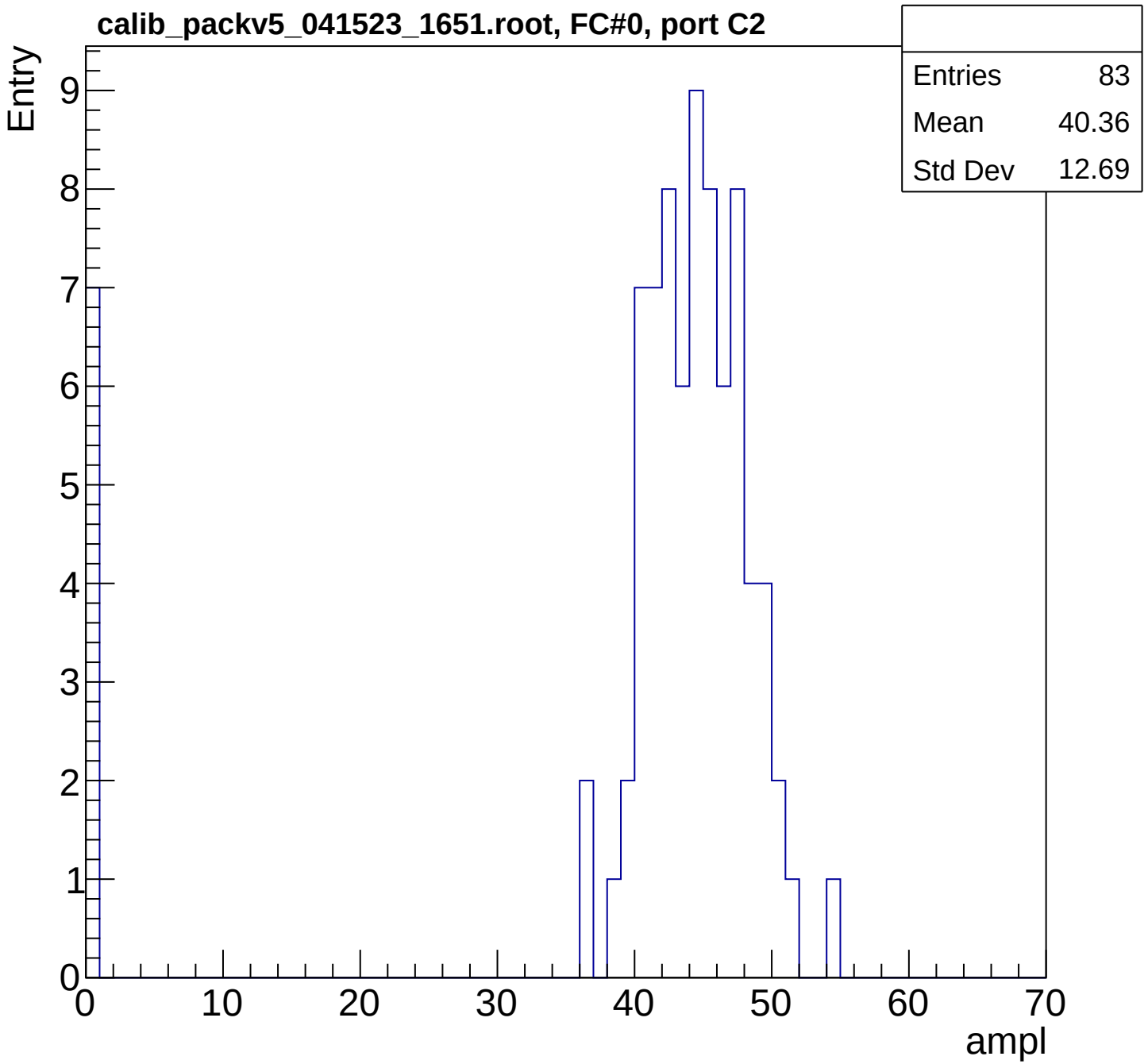
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U13-ch66, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch67, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 25.55
Std Dev 11.85
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch67, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 33.48
Std Dev 11.23
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch67, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 40.36
Std Dev 12.69
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
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40
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60
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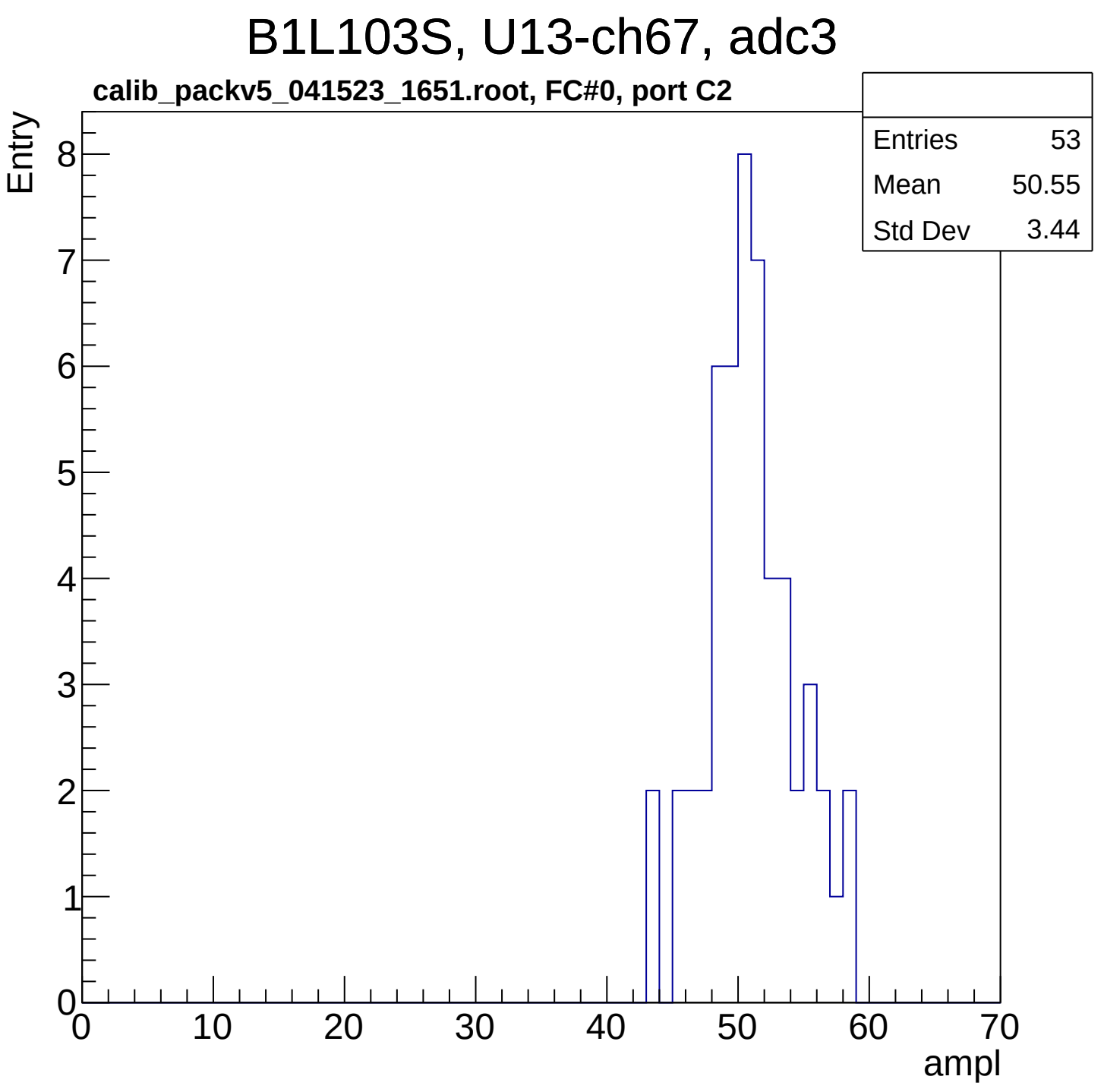
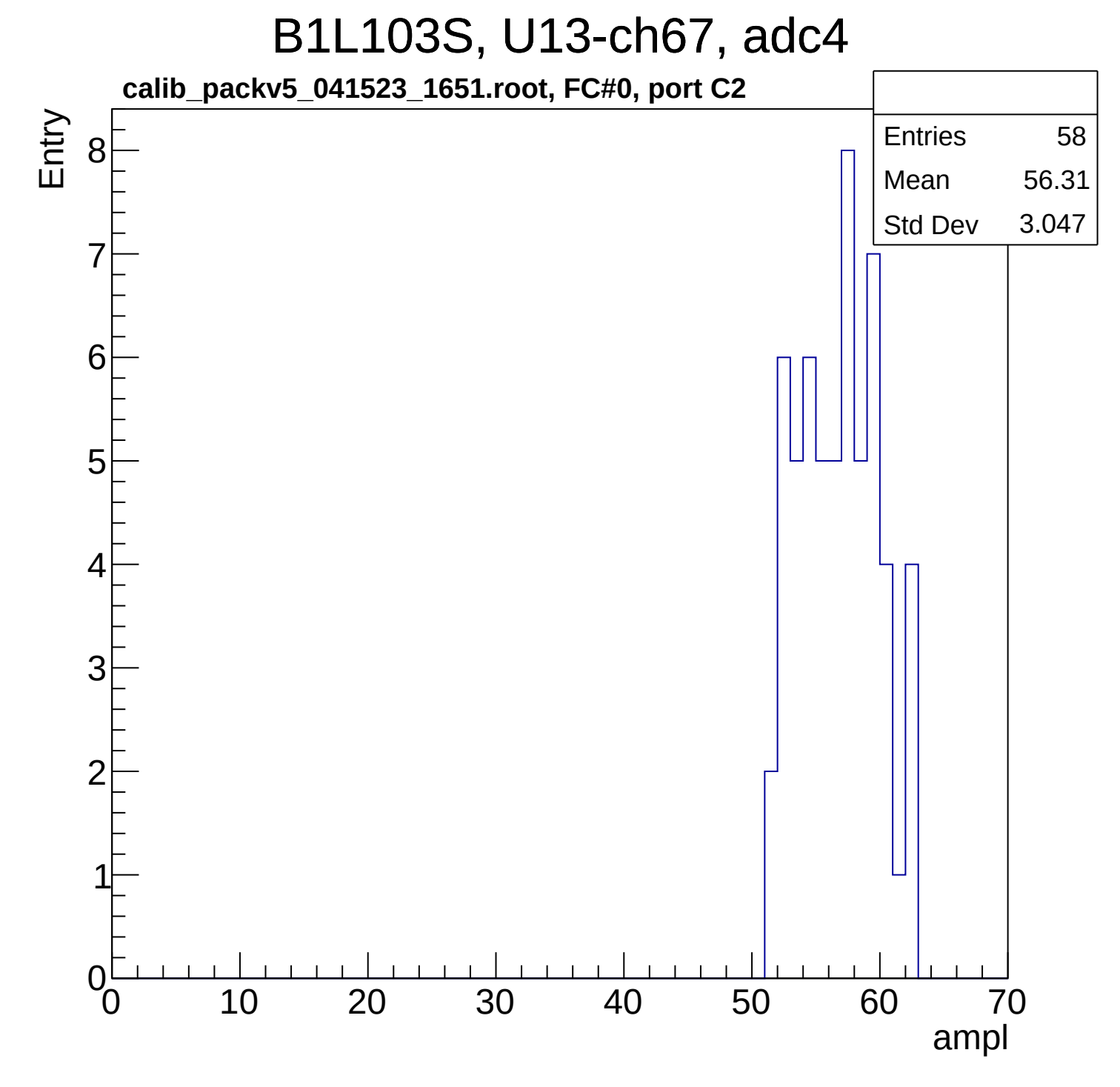
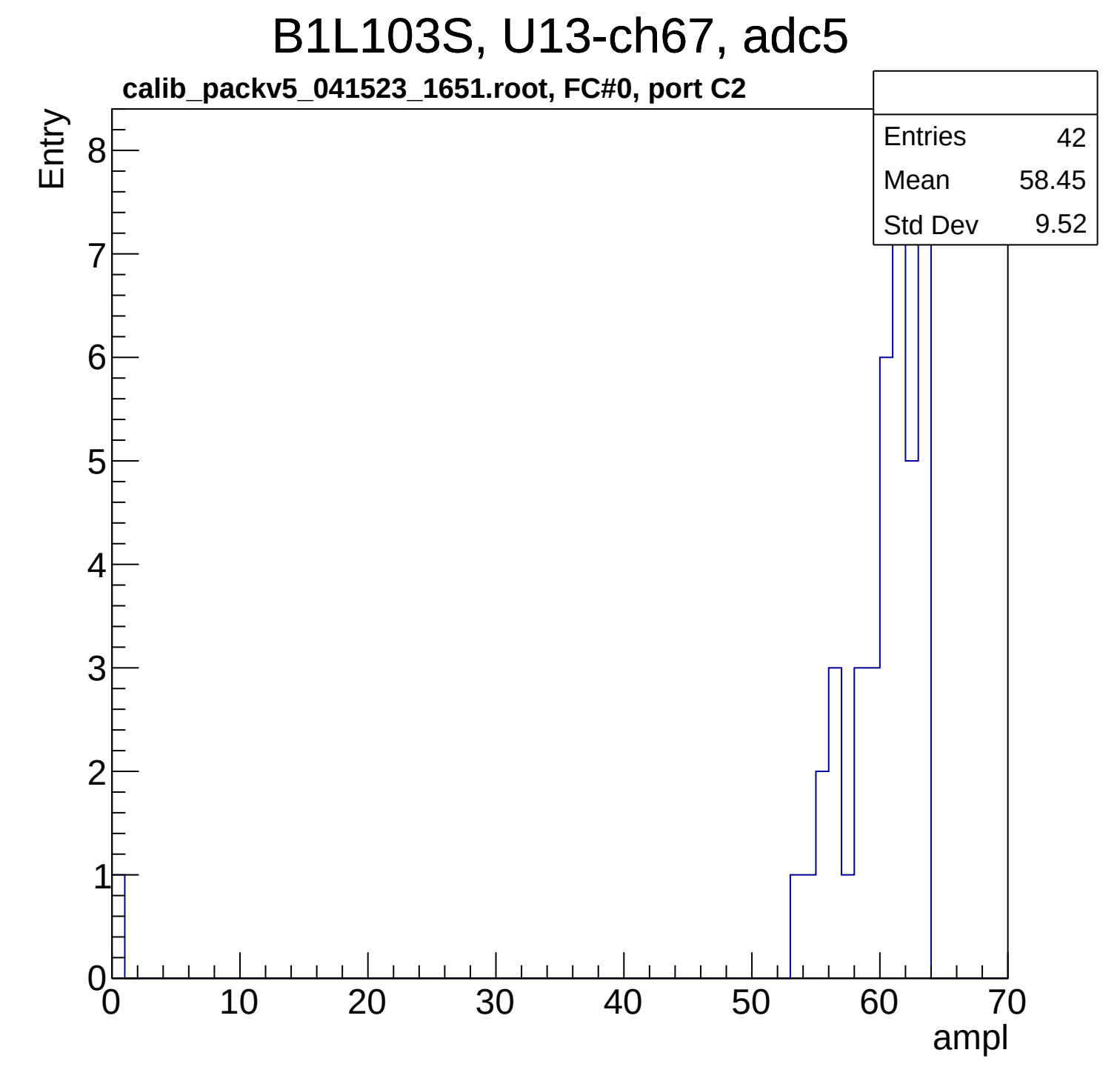

B1L103S, U13-ch67, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 50.55
Std Dev 3.44
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch67, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 56.31
Std Dev 3.047
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch67, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 58.45
Std Dev 9.52
Entry
ampl
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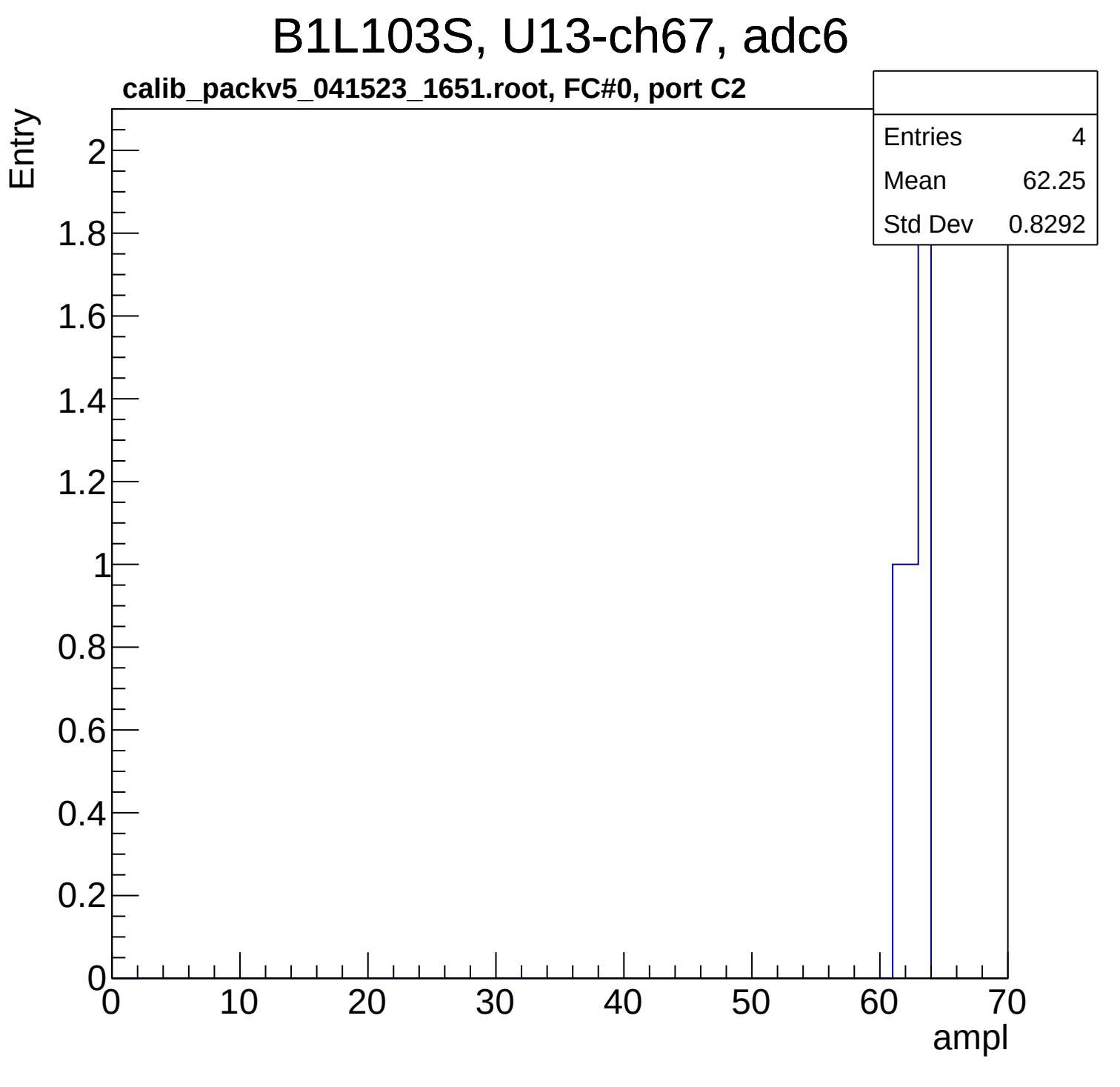
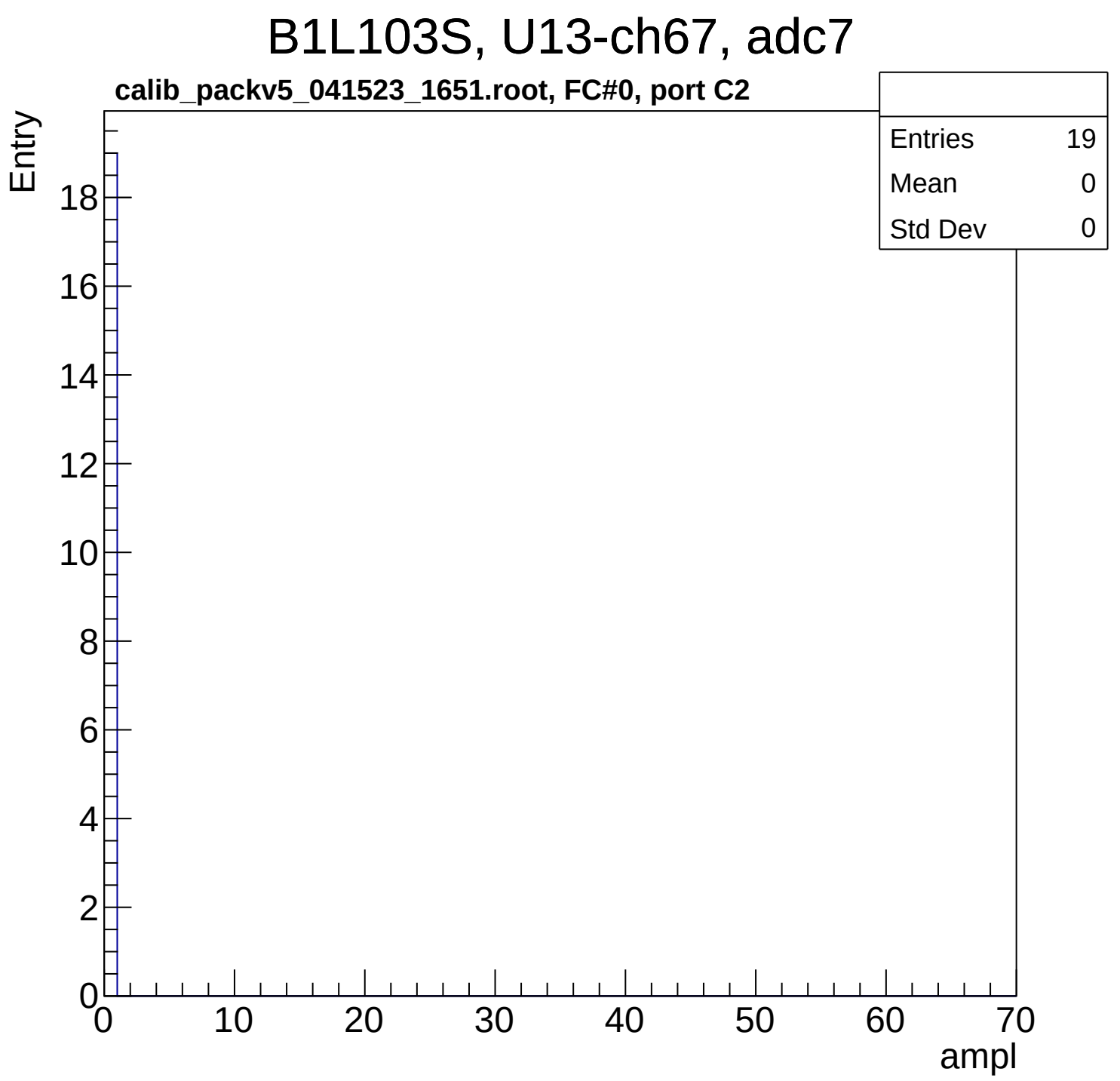
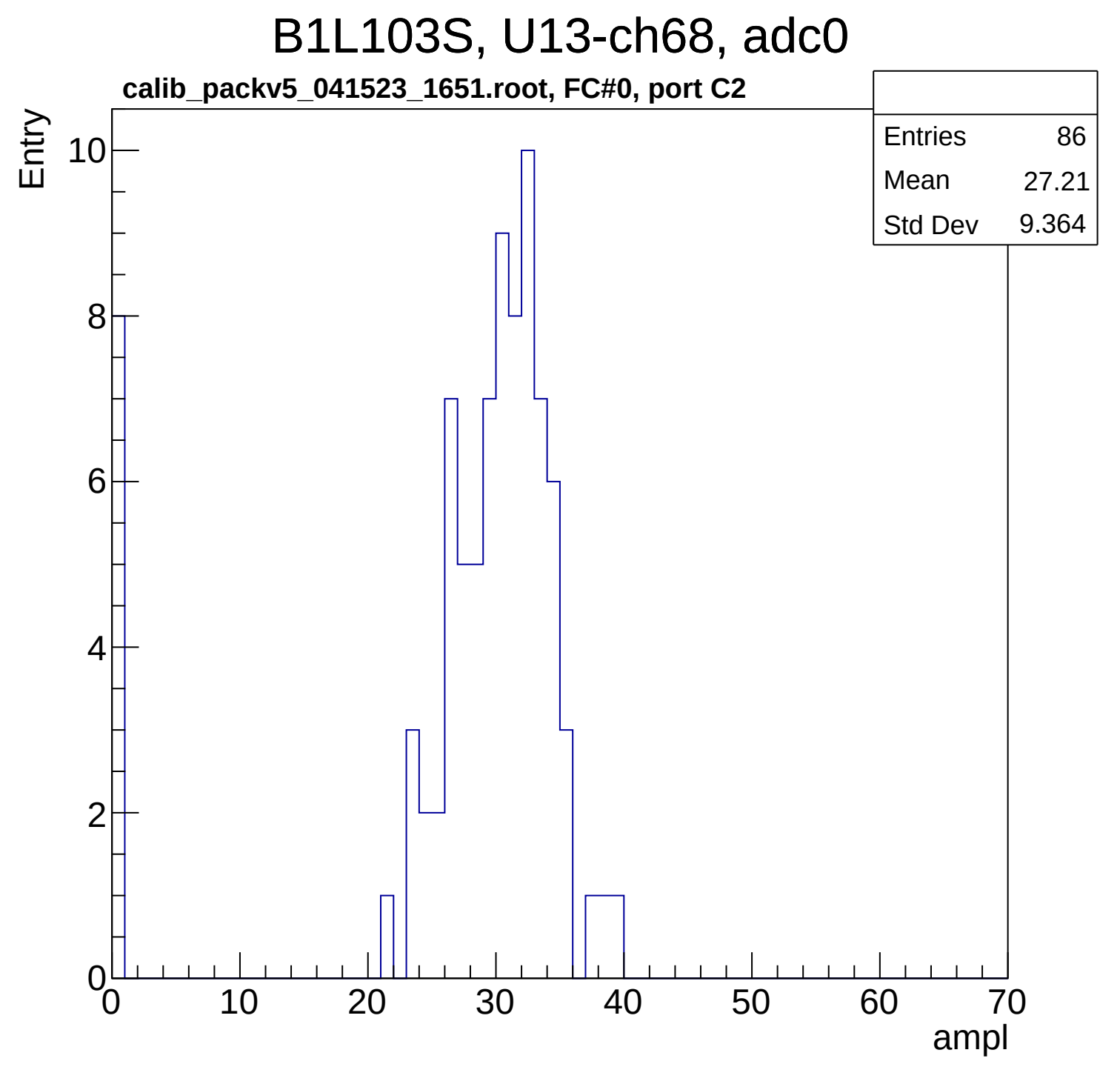
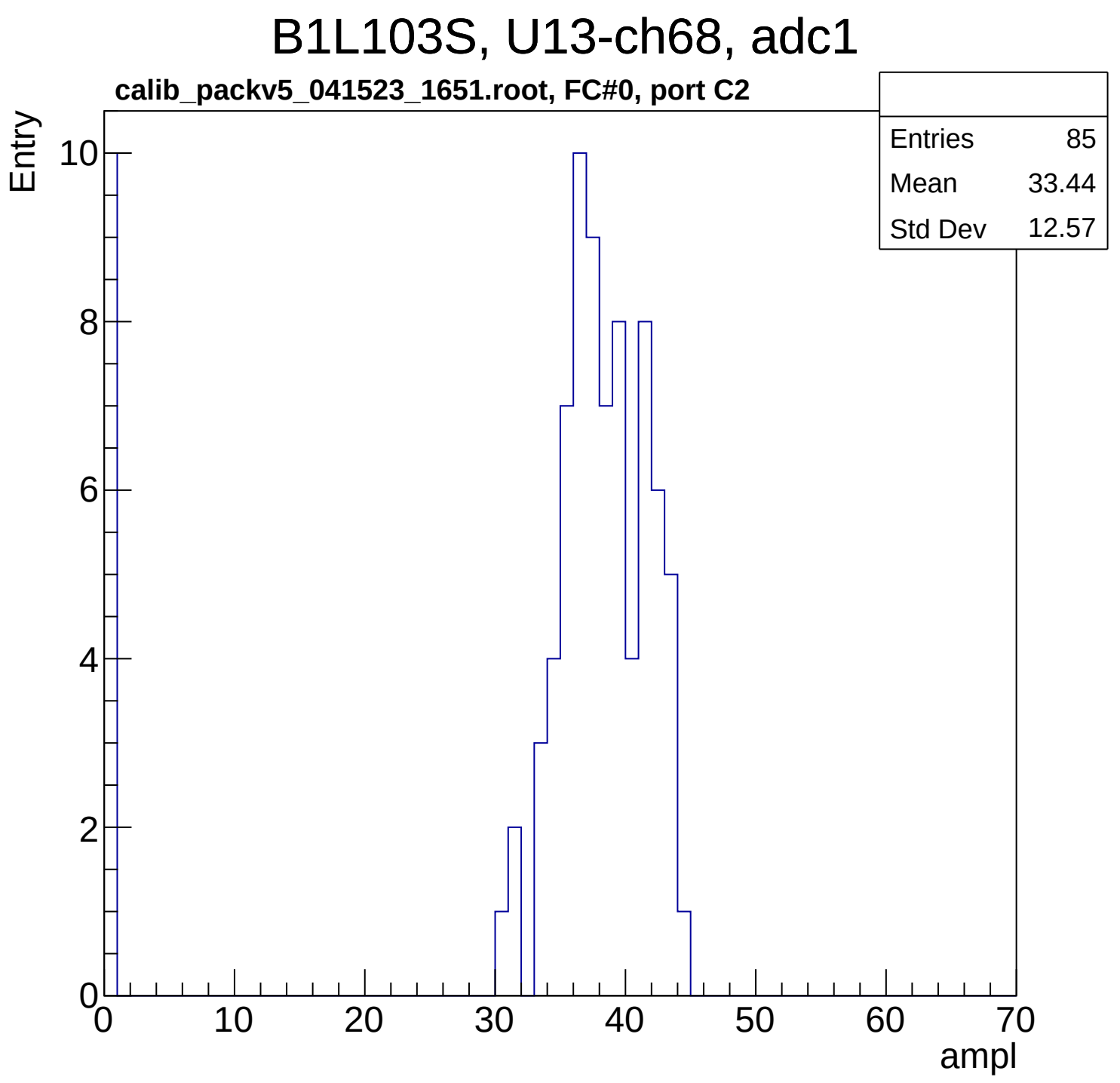
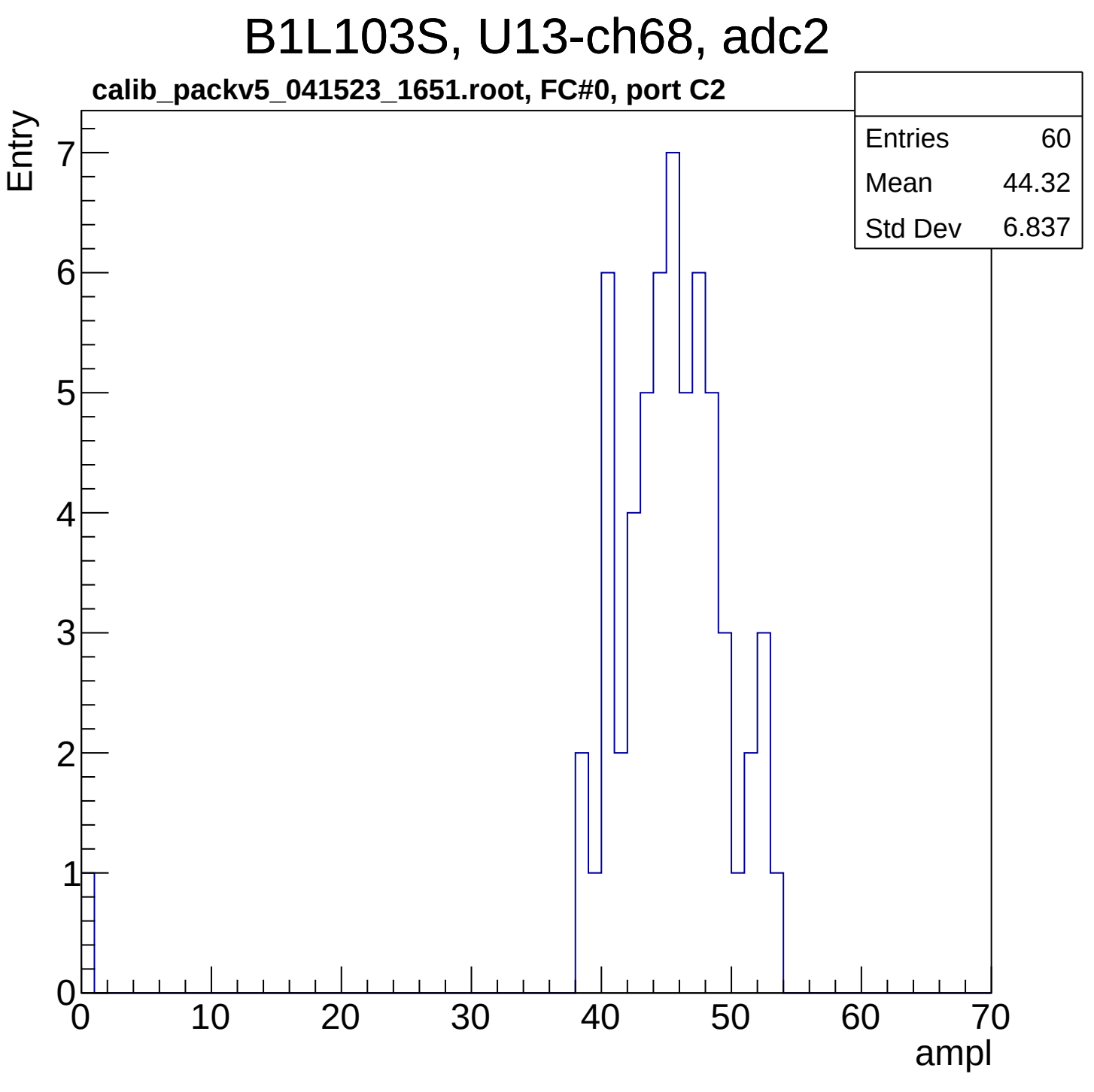
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

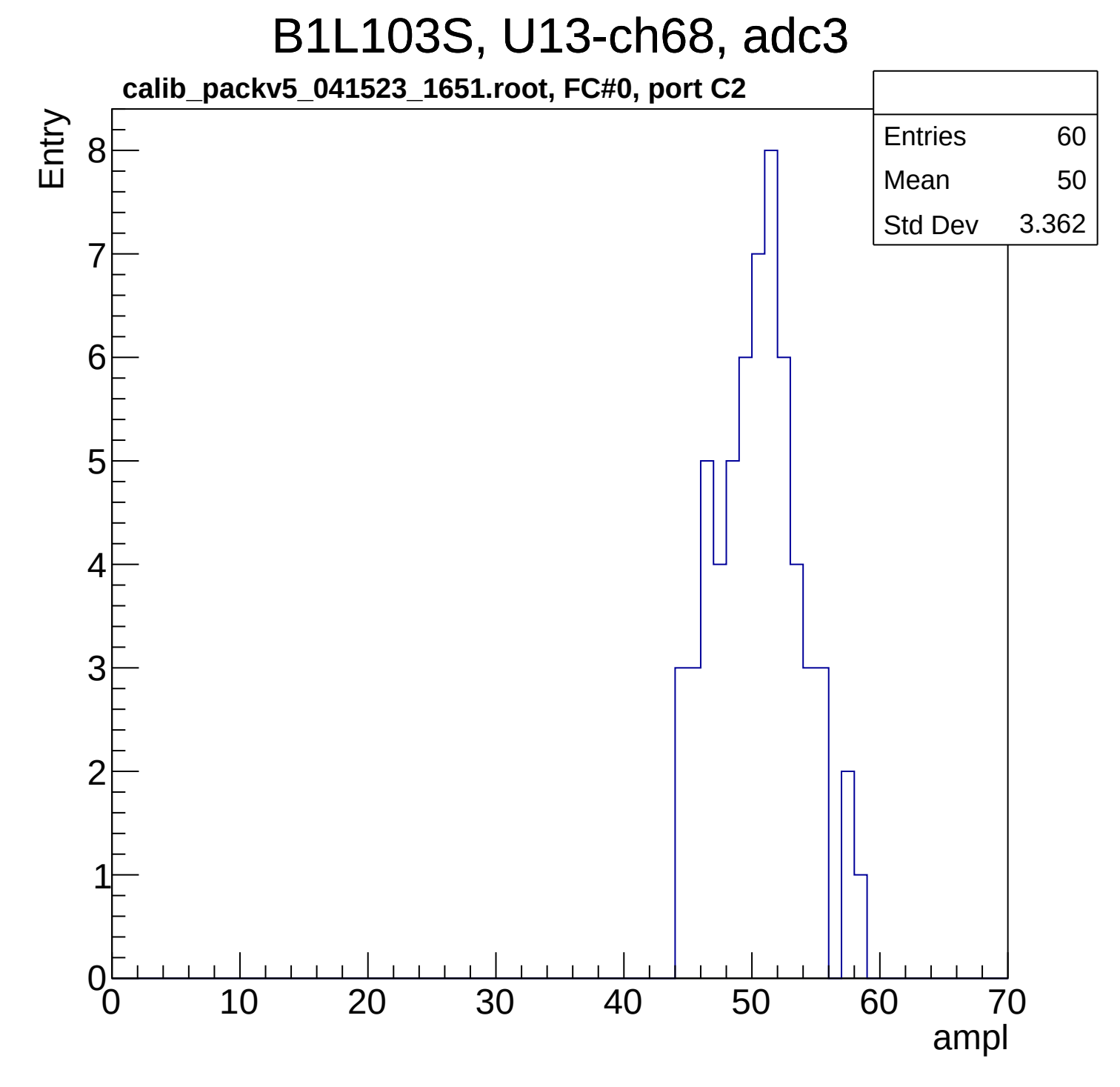

B1L103S, U13-ch67, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U13-ch67, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch68, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 27.21
Std Dev 9.364
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch68, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 33.44
Std Dev 12.57
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch68, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 44.32
Std Dev 6.837
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch68, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 50
Std Dev 3.362
Entry
ampl
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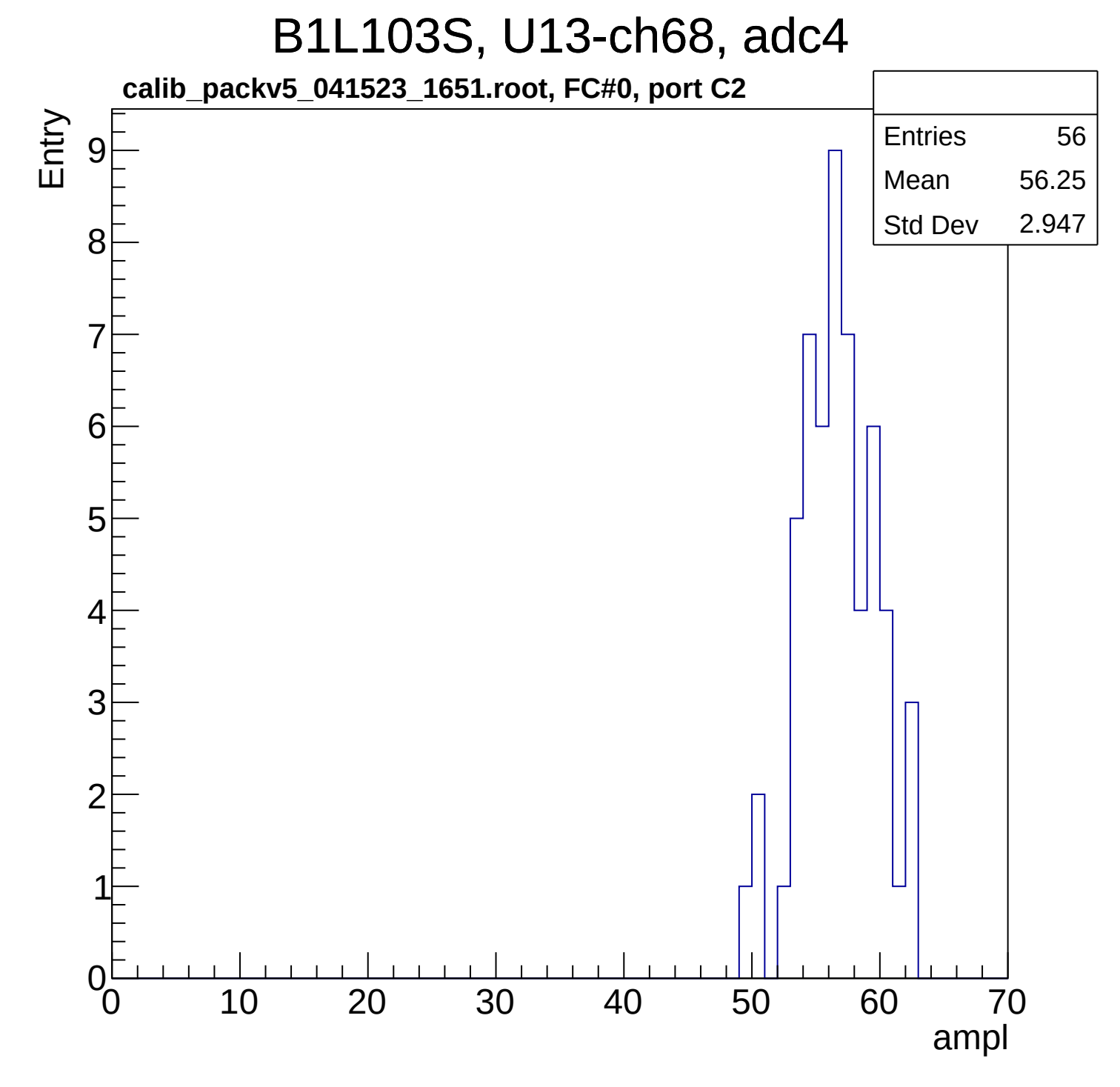
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch68, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 56.25
Std Dev 2.947
Entry
ampl
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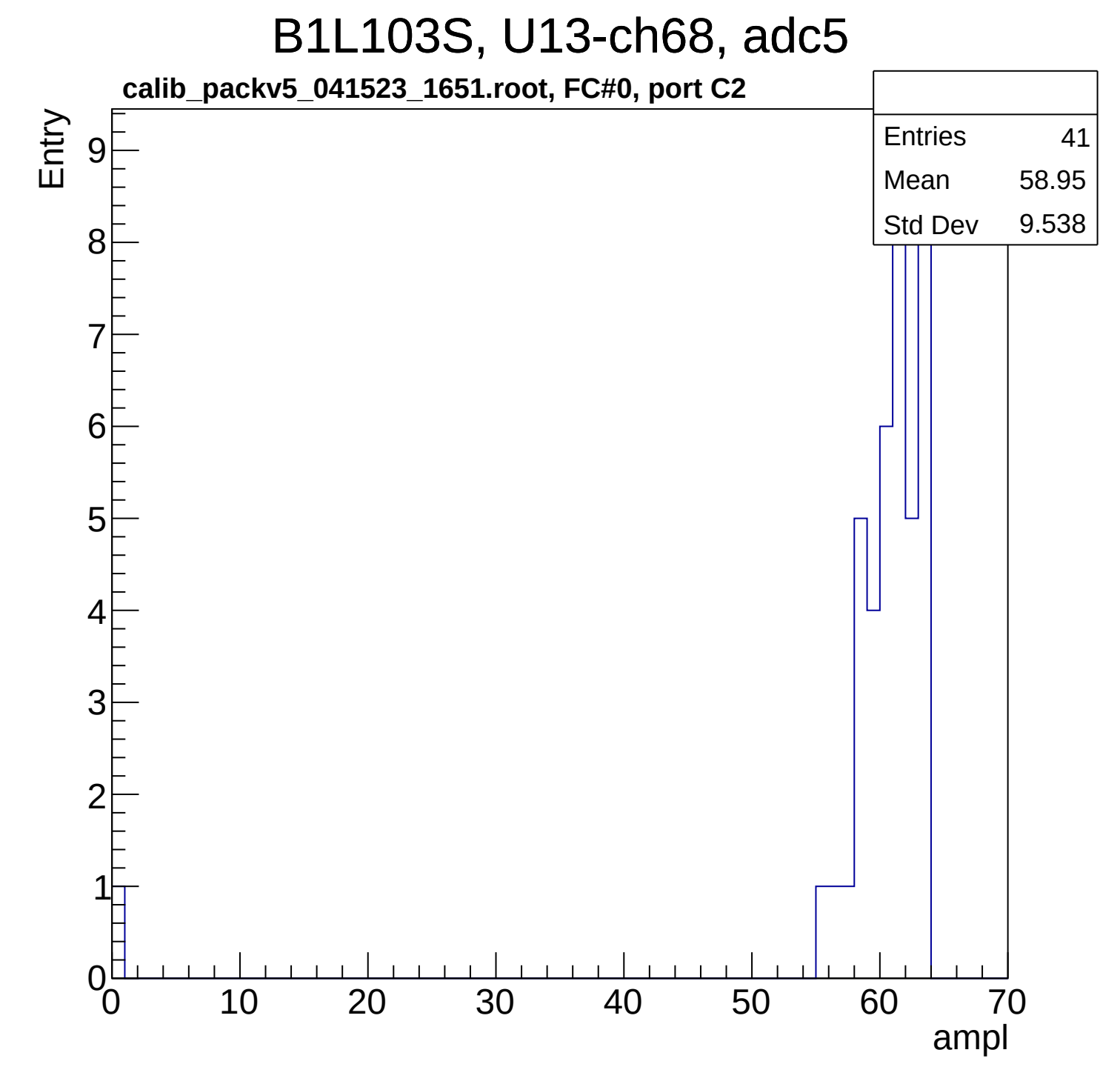
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch68, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 58.95
Std Dev 9.538
Entry
ampl
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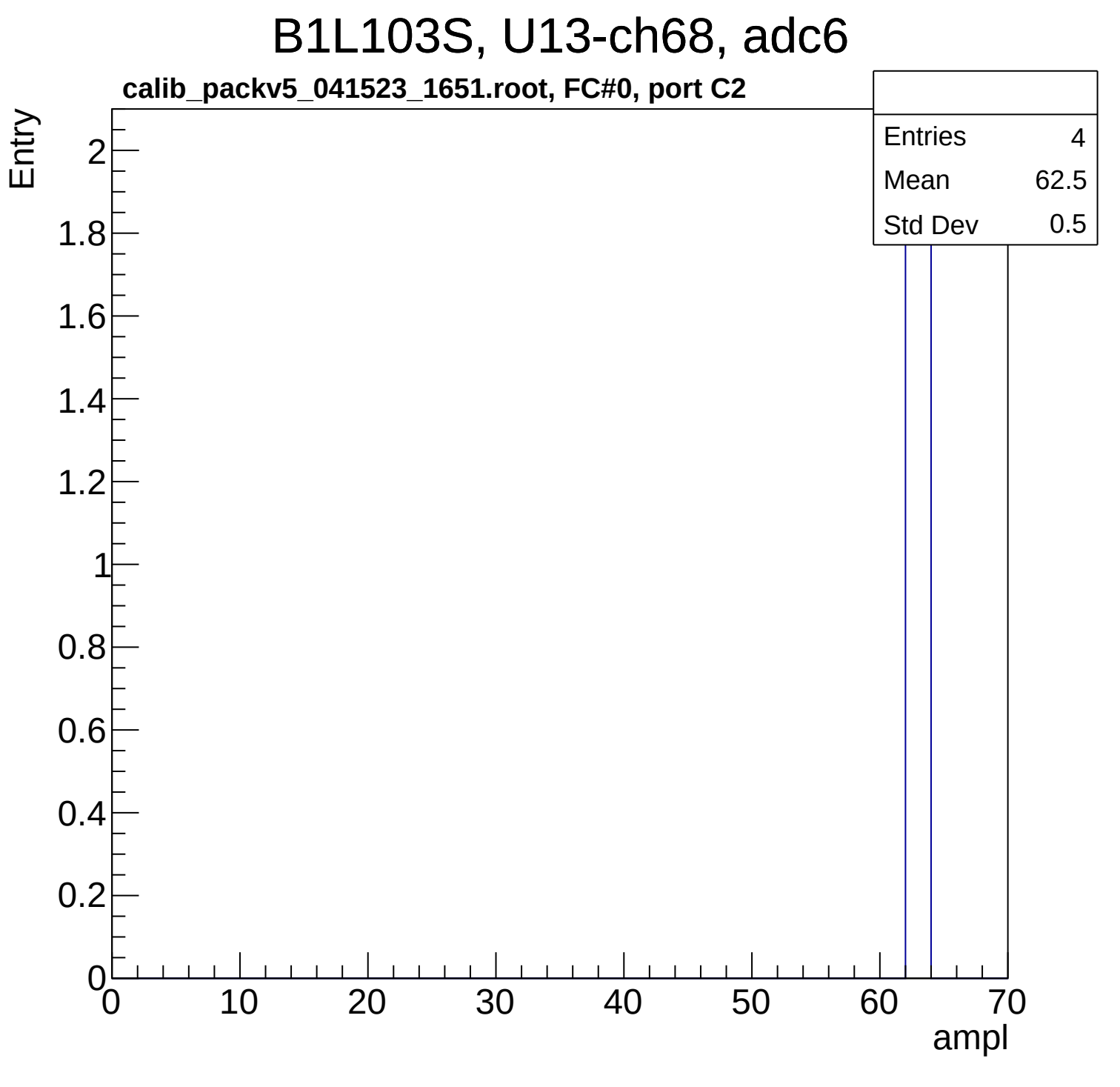
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch68, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.5
Std Dev 0.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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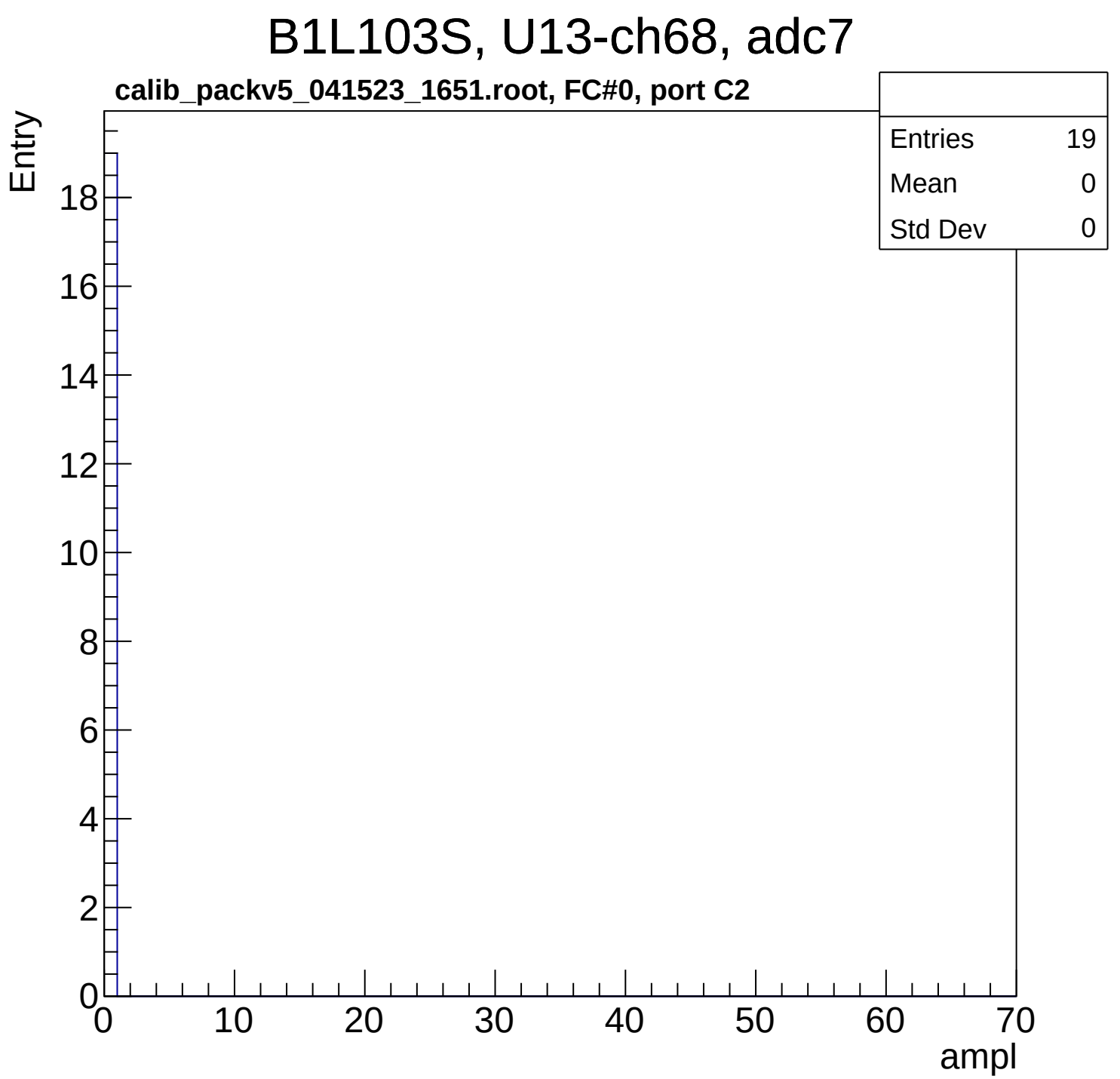
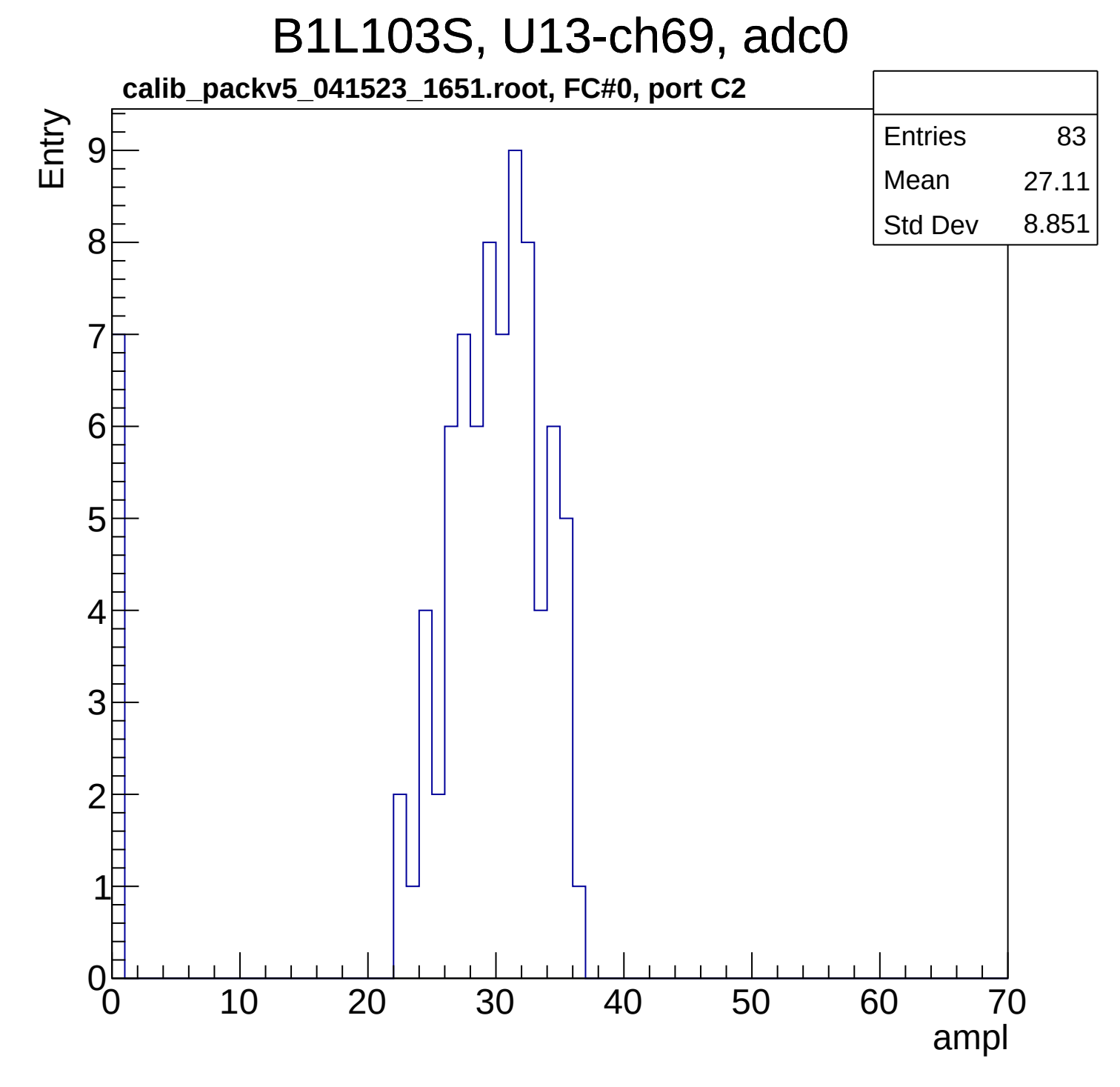
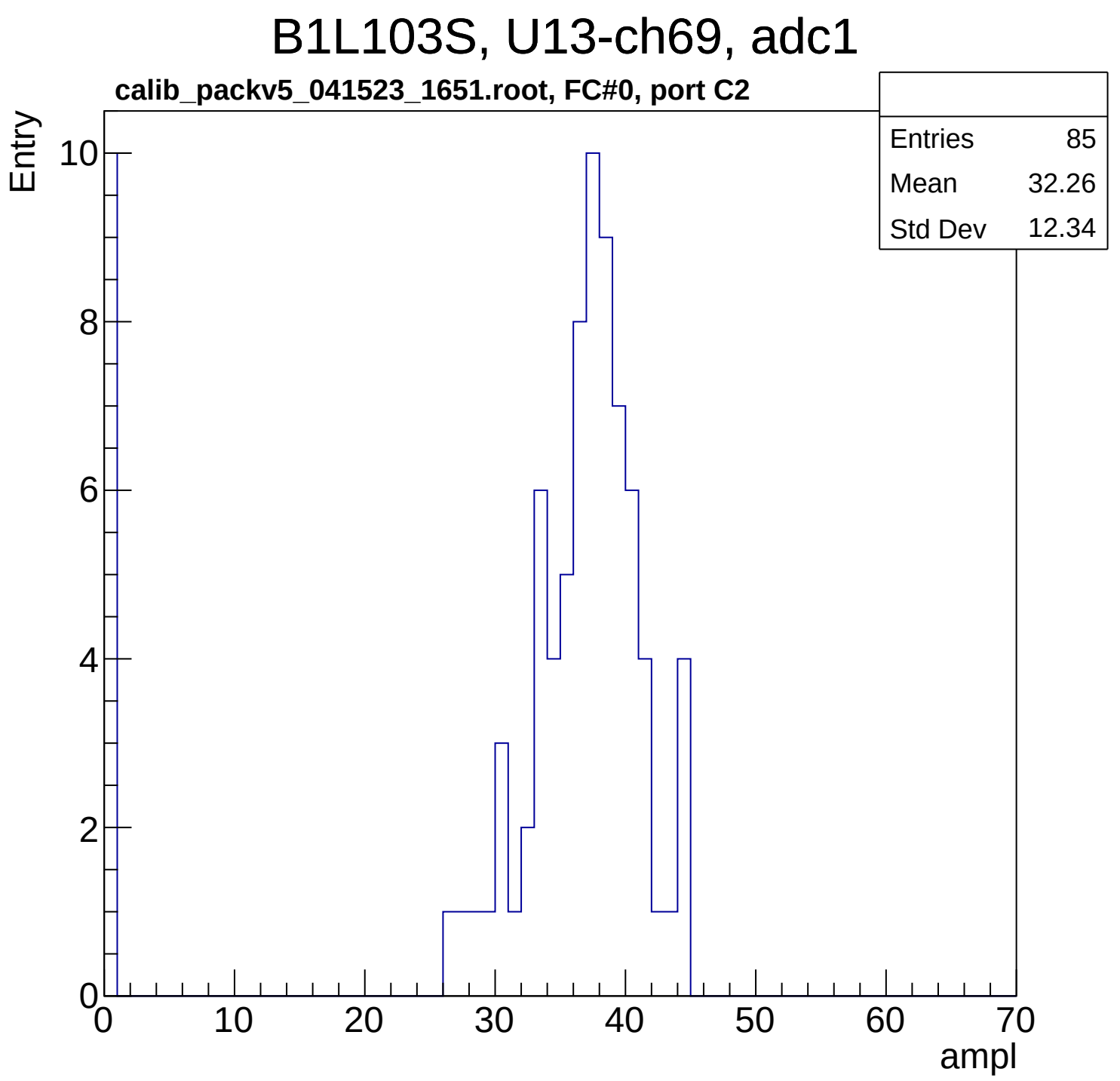
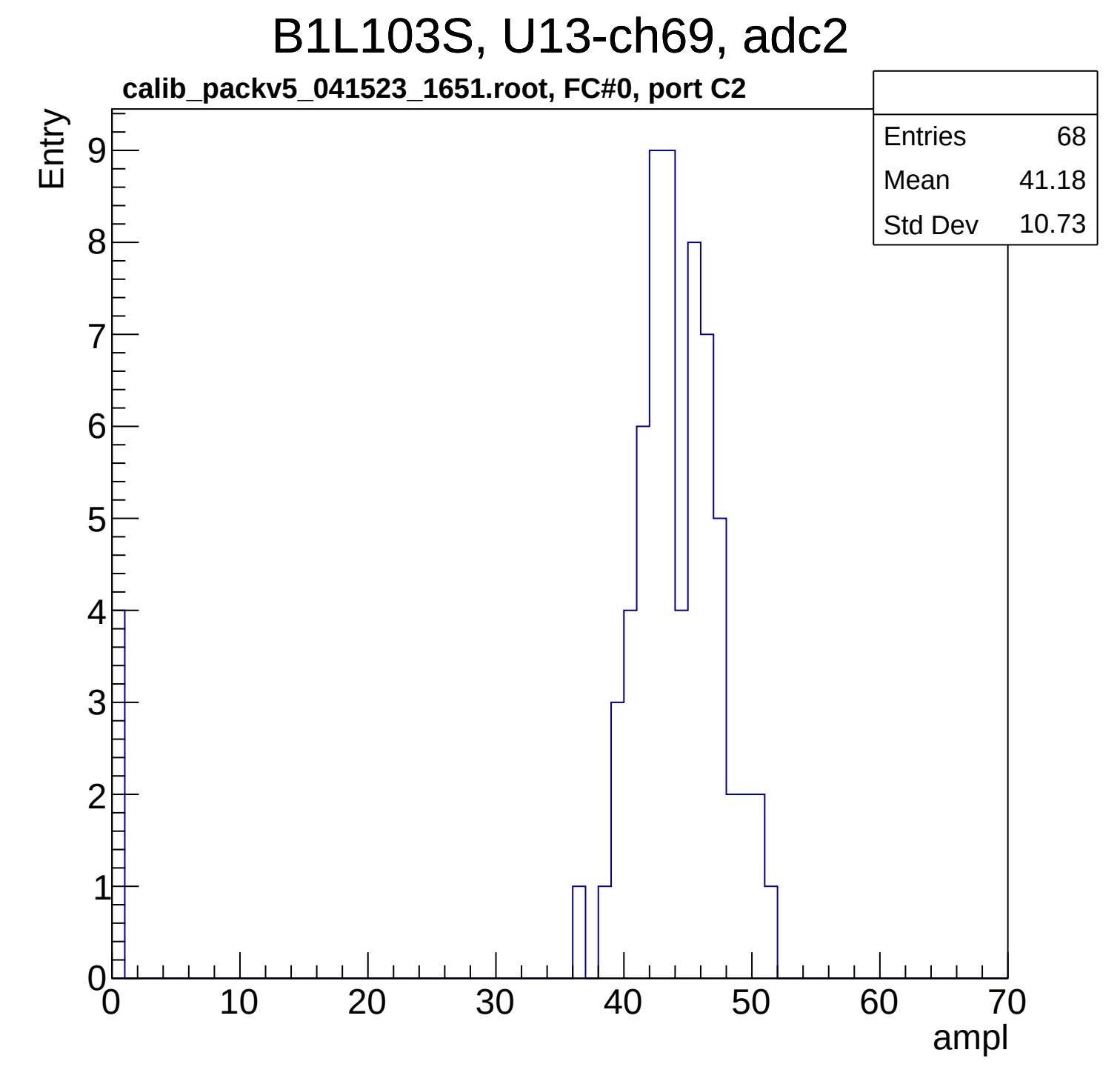
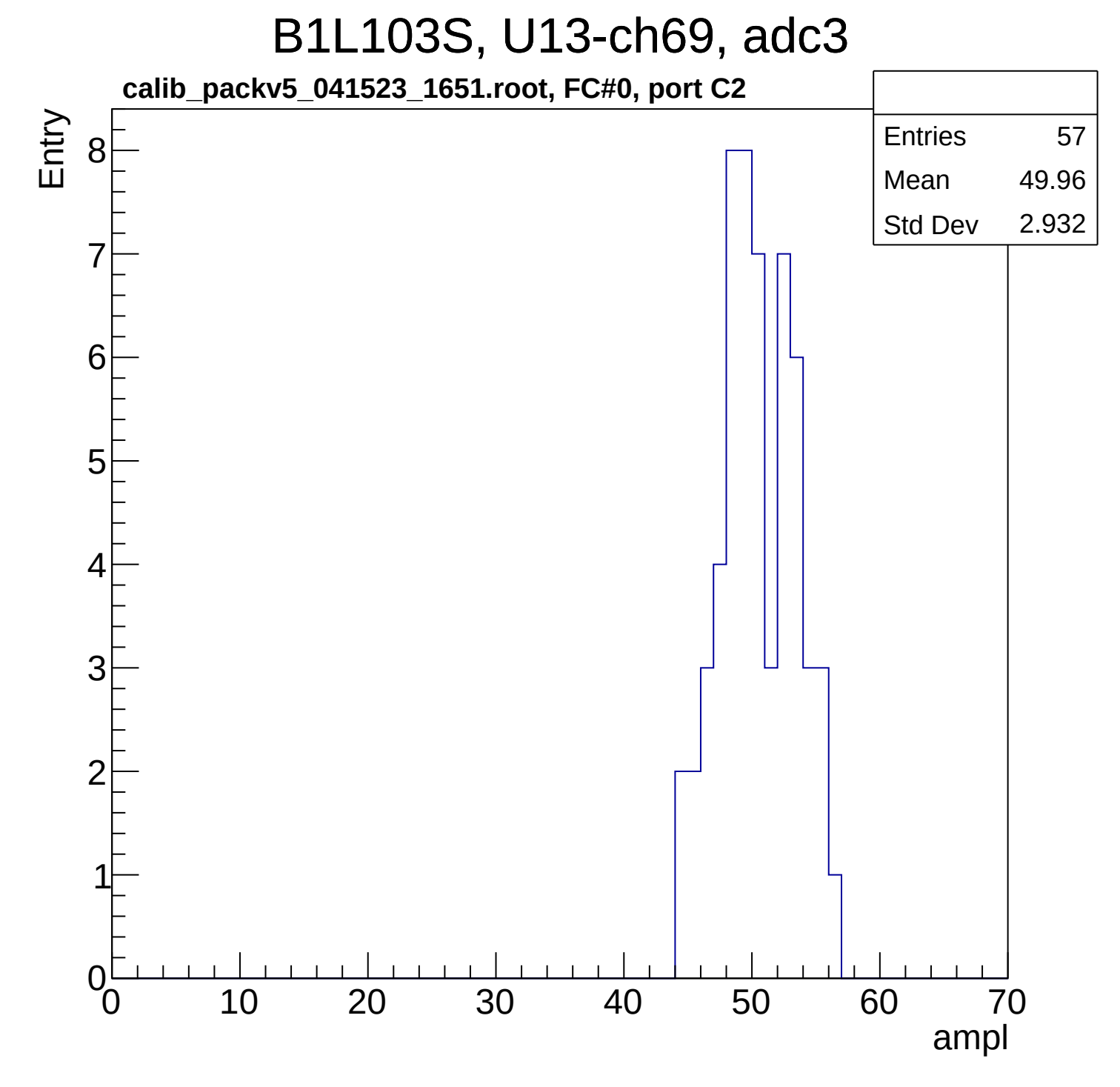

B1L103S, U13-ch68, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch69, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 27.11
Std Dev 8.851
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch69, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 32.26
Std Dev 12.34
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch69, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 41.18
Std Dev 10.73
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch69, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 49.96
Std Dev 2.932
Entry
ampl
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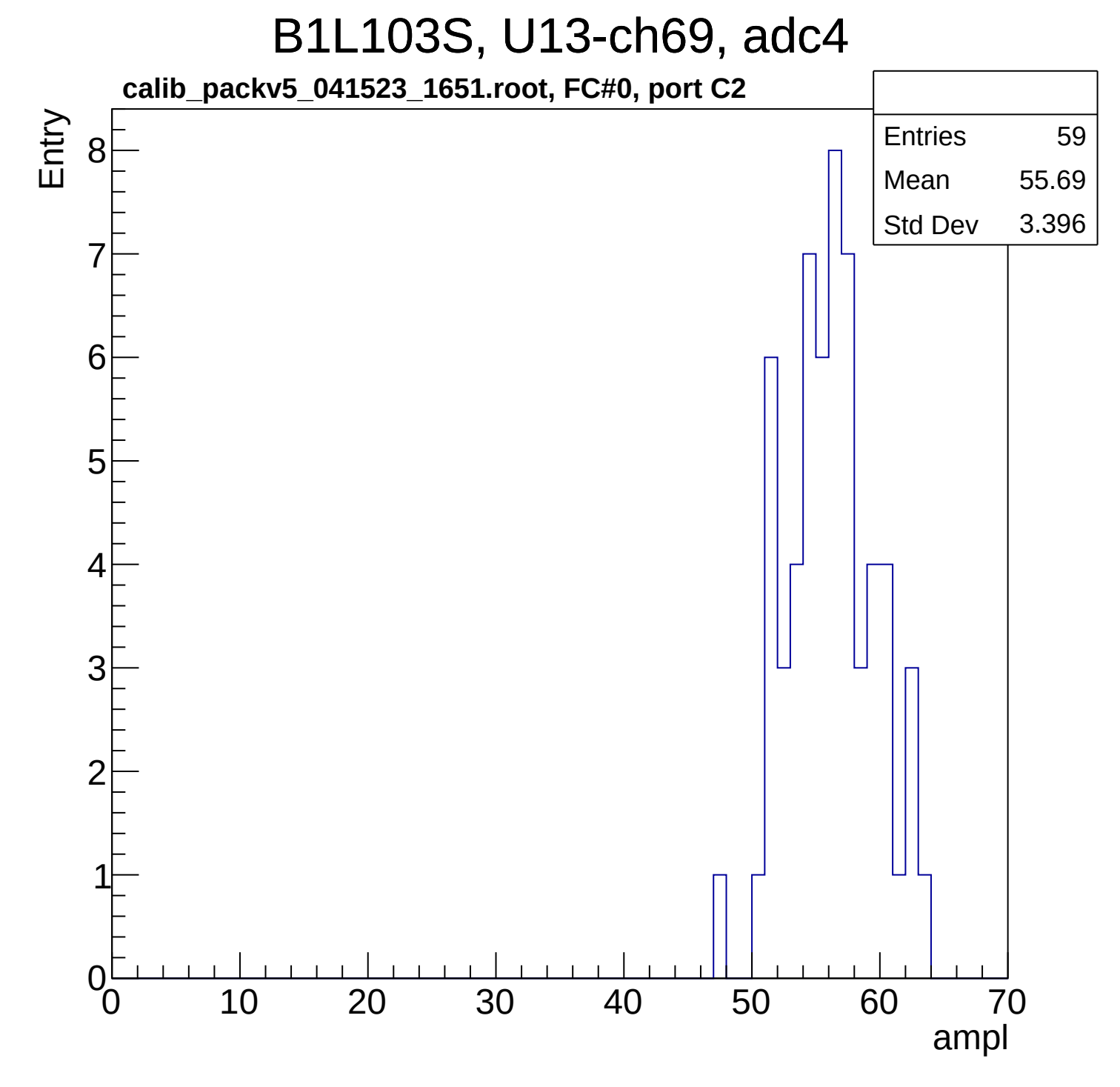
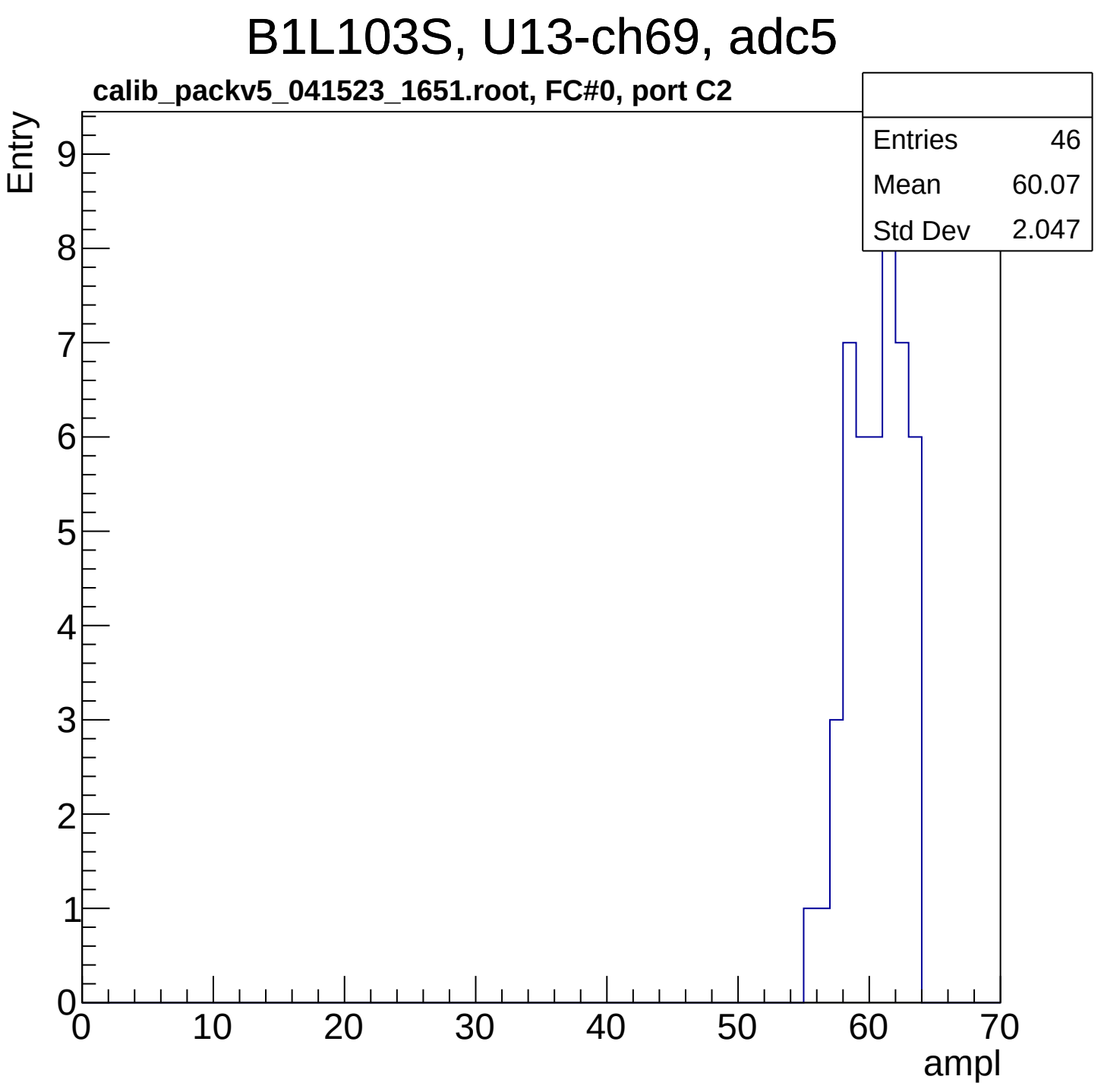
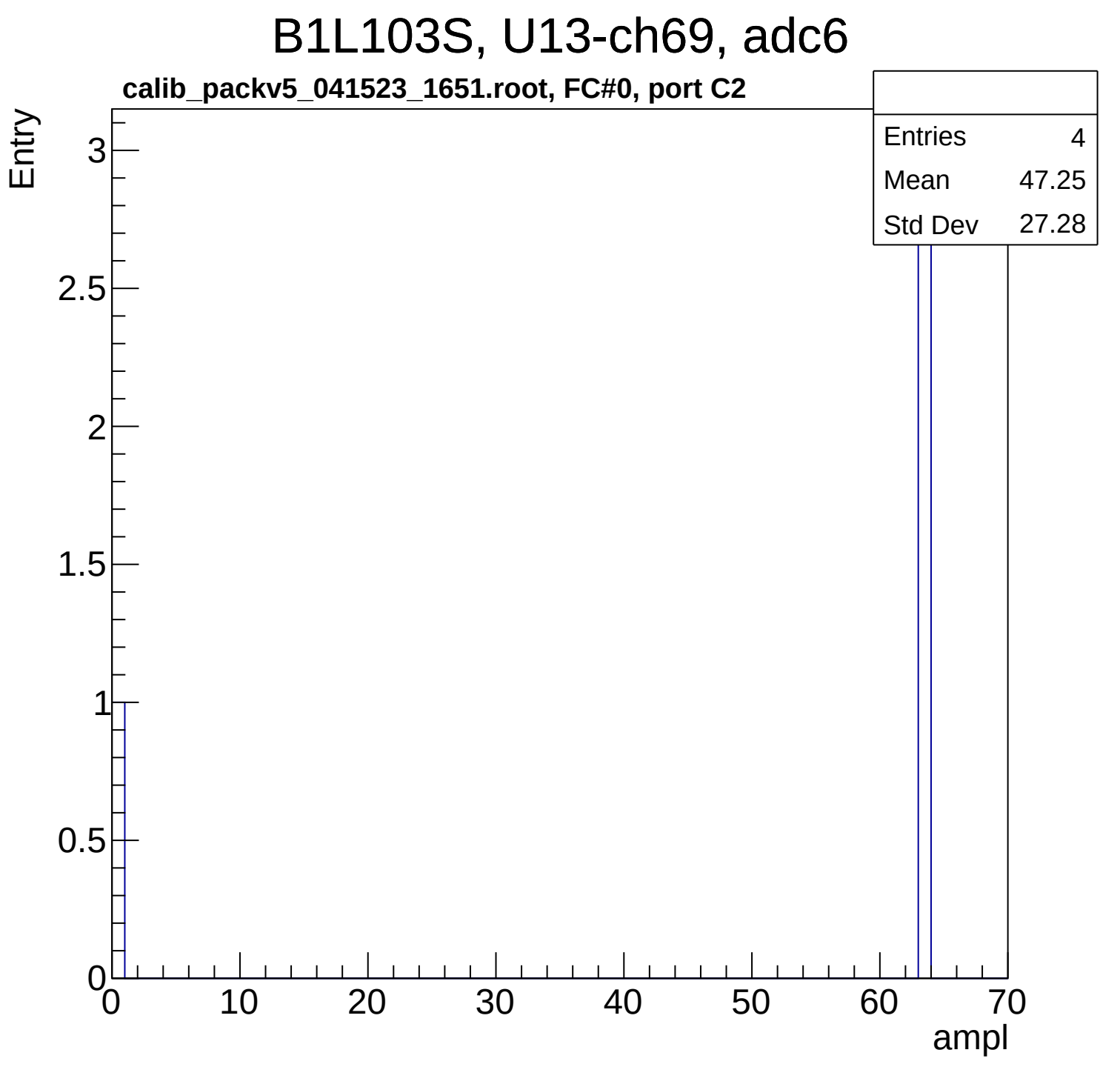
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch69, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 55.69
Std Dev 3.396
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch69, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 60.07
Std Dev 2.047
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch69, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 47.25
Std Dev 27.28
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
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40
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60
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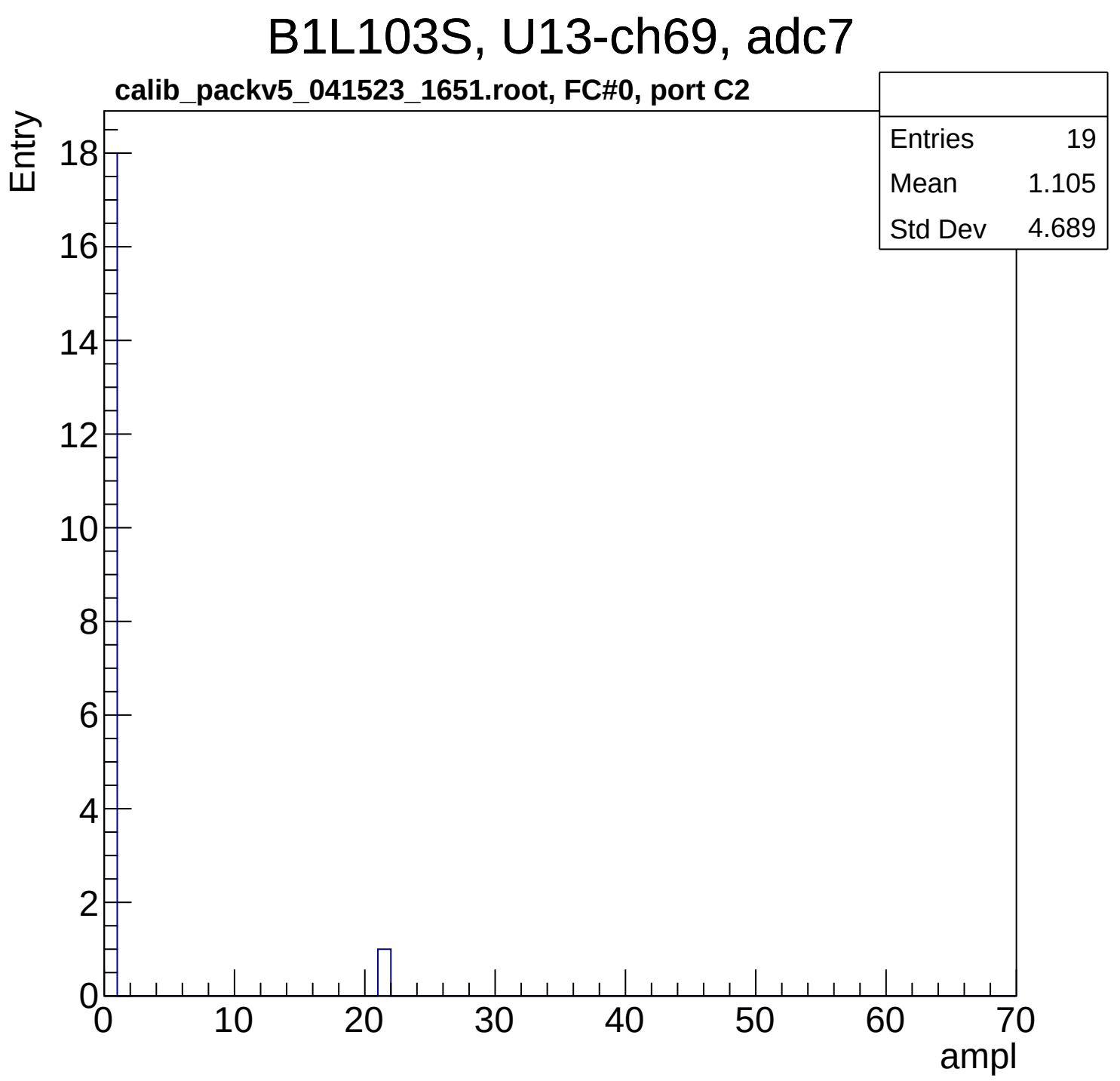
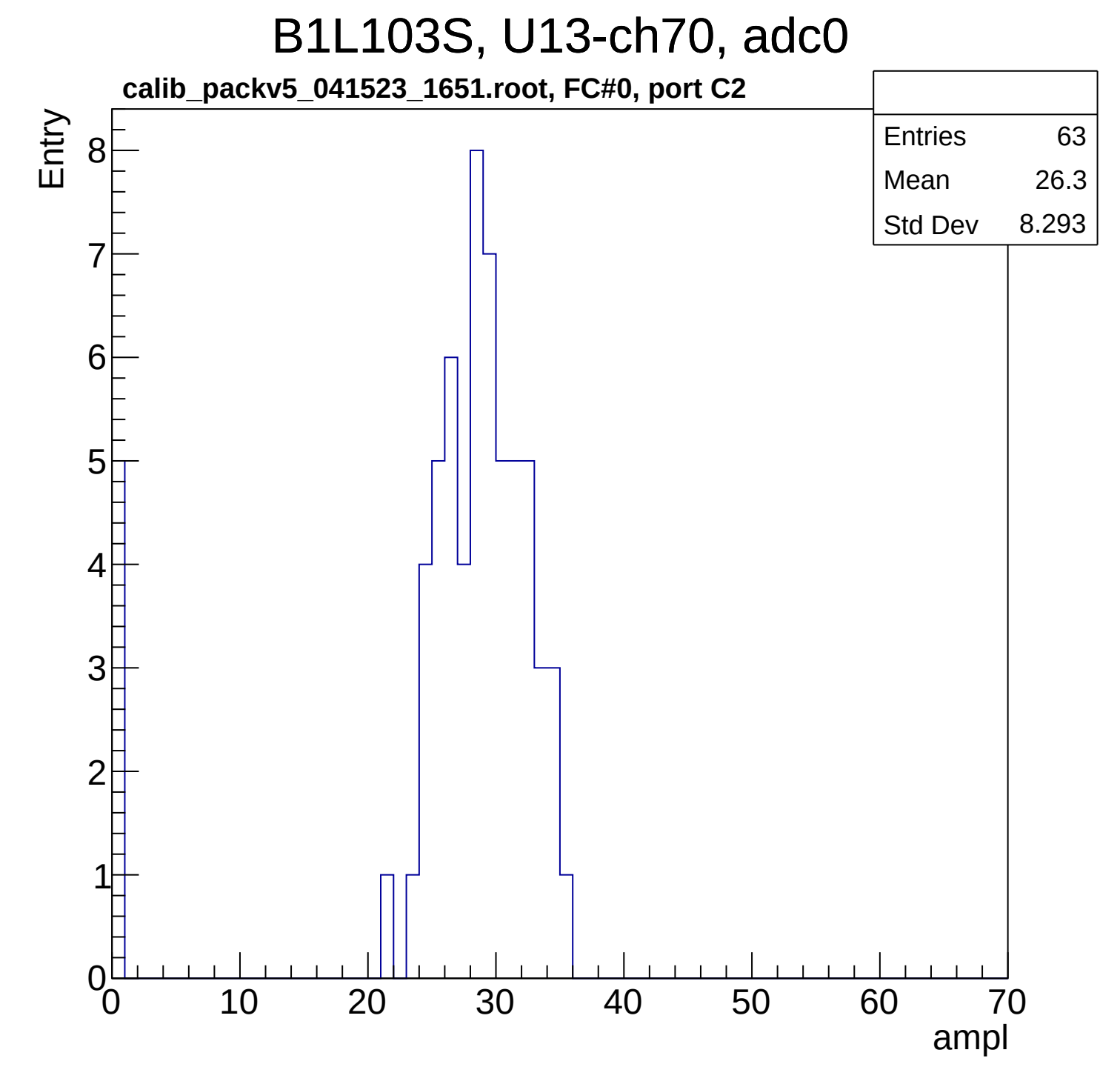

B1L103S, U13-ch69, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch70, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 26.3
Std Dev 8.293
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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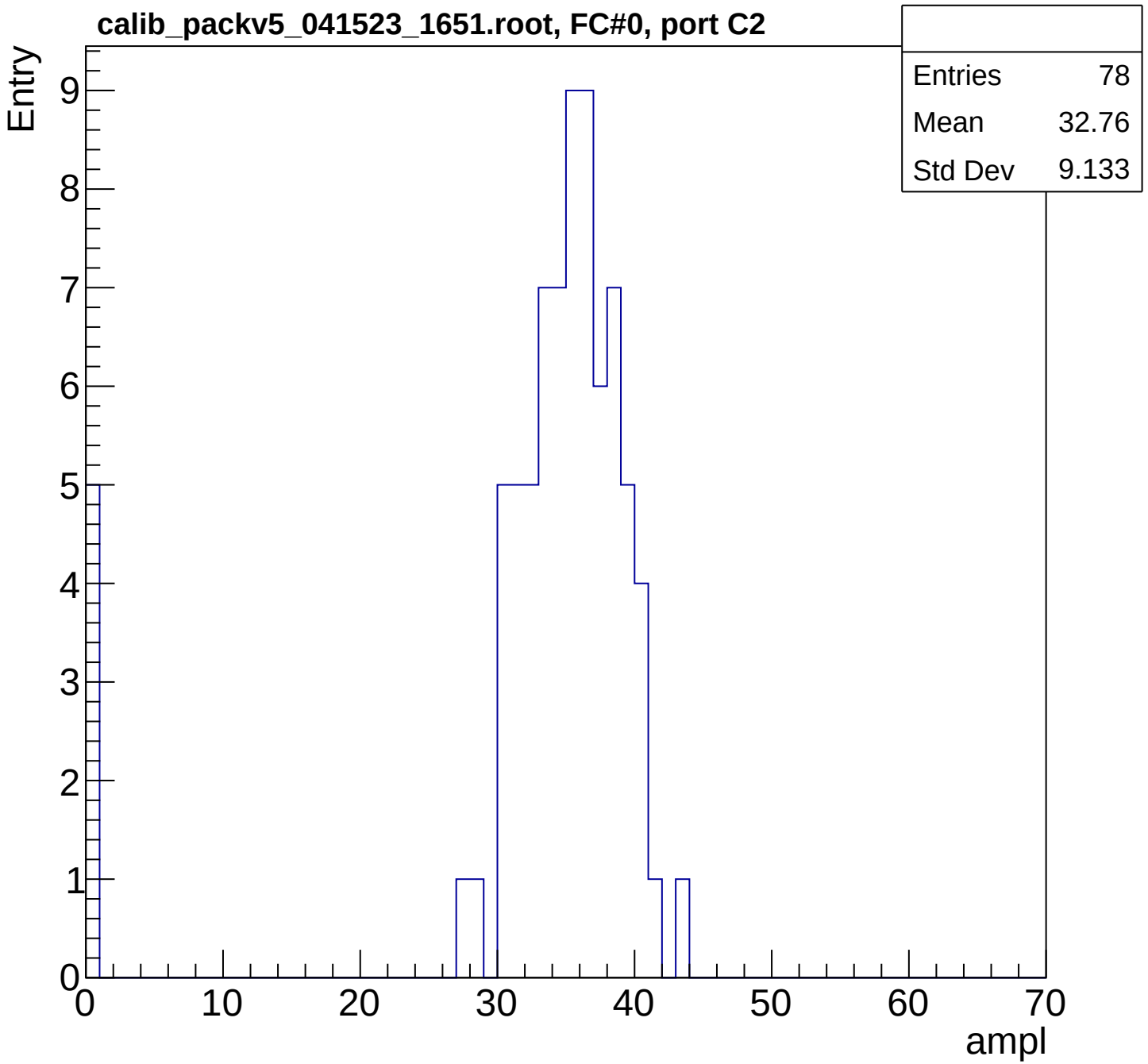
B1L103S, U13-ch70, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 32.76
Std Dev 9.133
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
30
40
50
60
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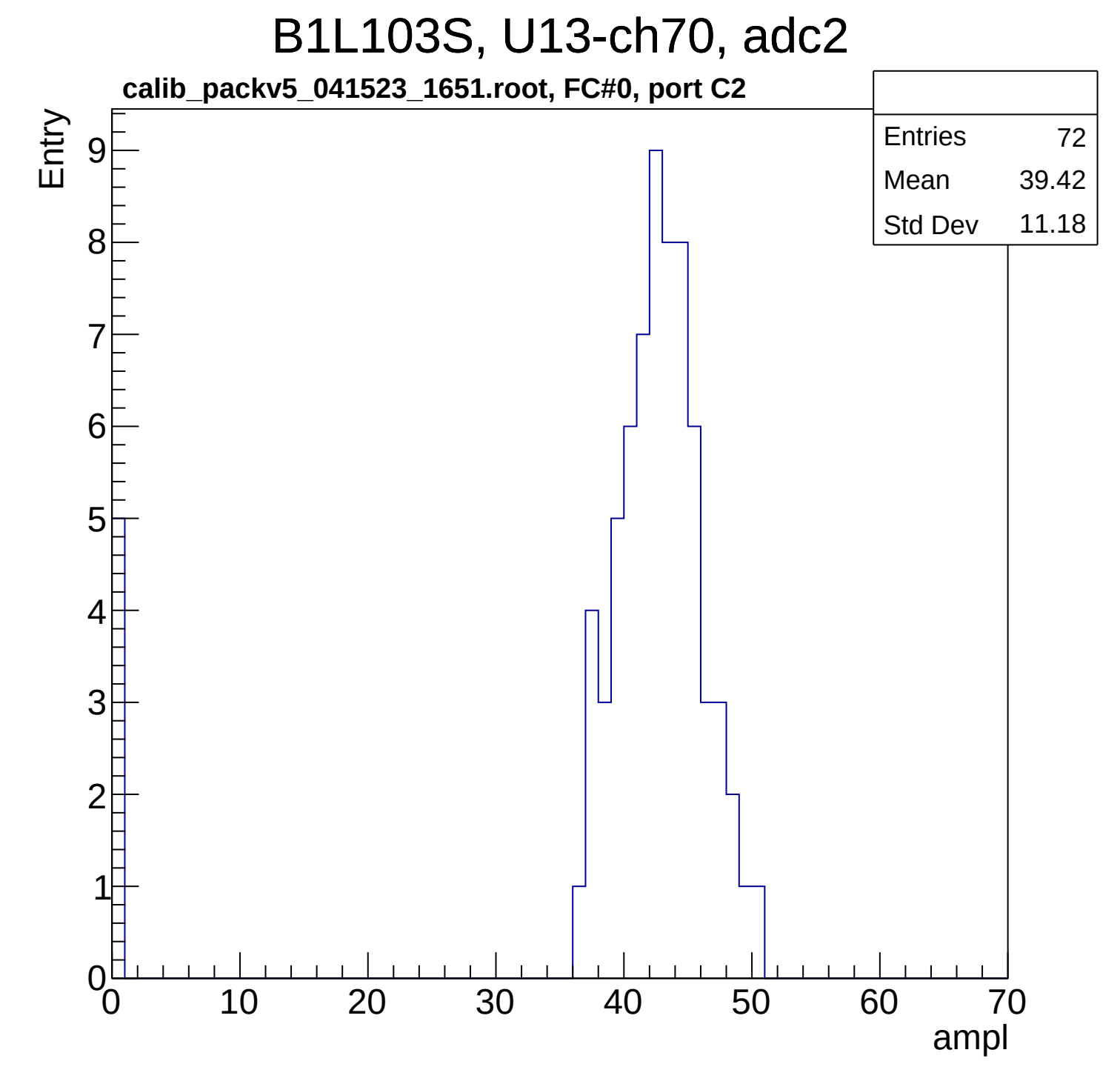
B1L103S, U13-ch70, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 39.42
Std Dev 11.18
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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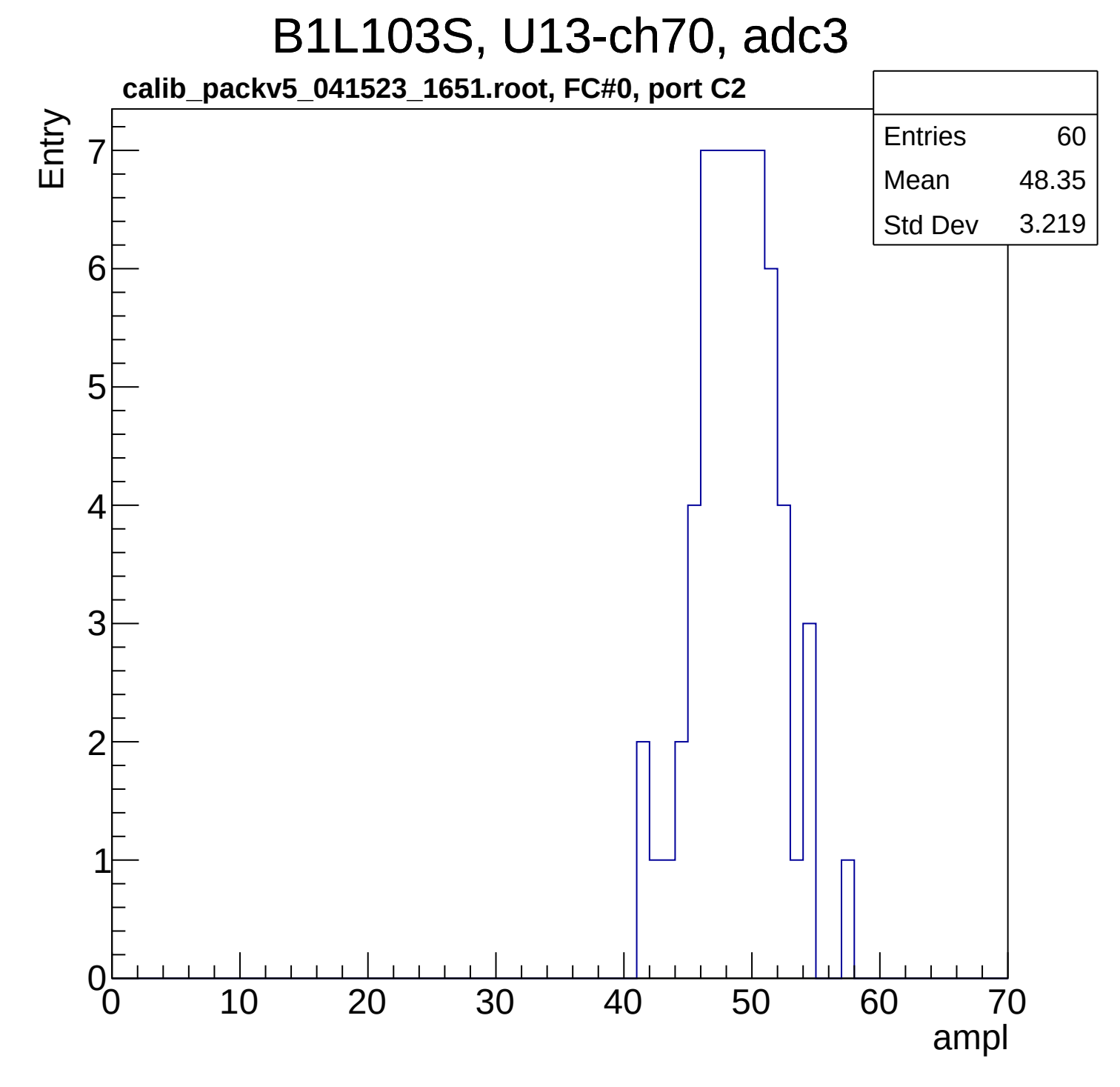
B1L103S, U13-ch70, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 48.35
Std Dev 3.219
Entry
ampl
0
1
2
3
4
5
6
7
0
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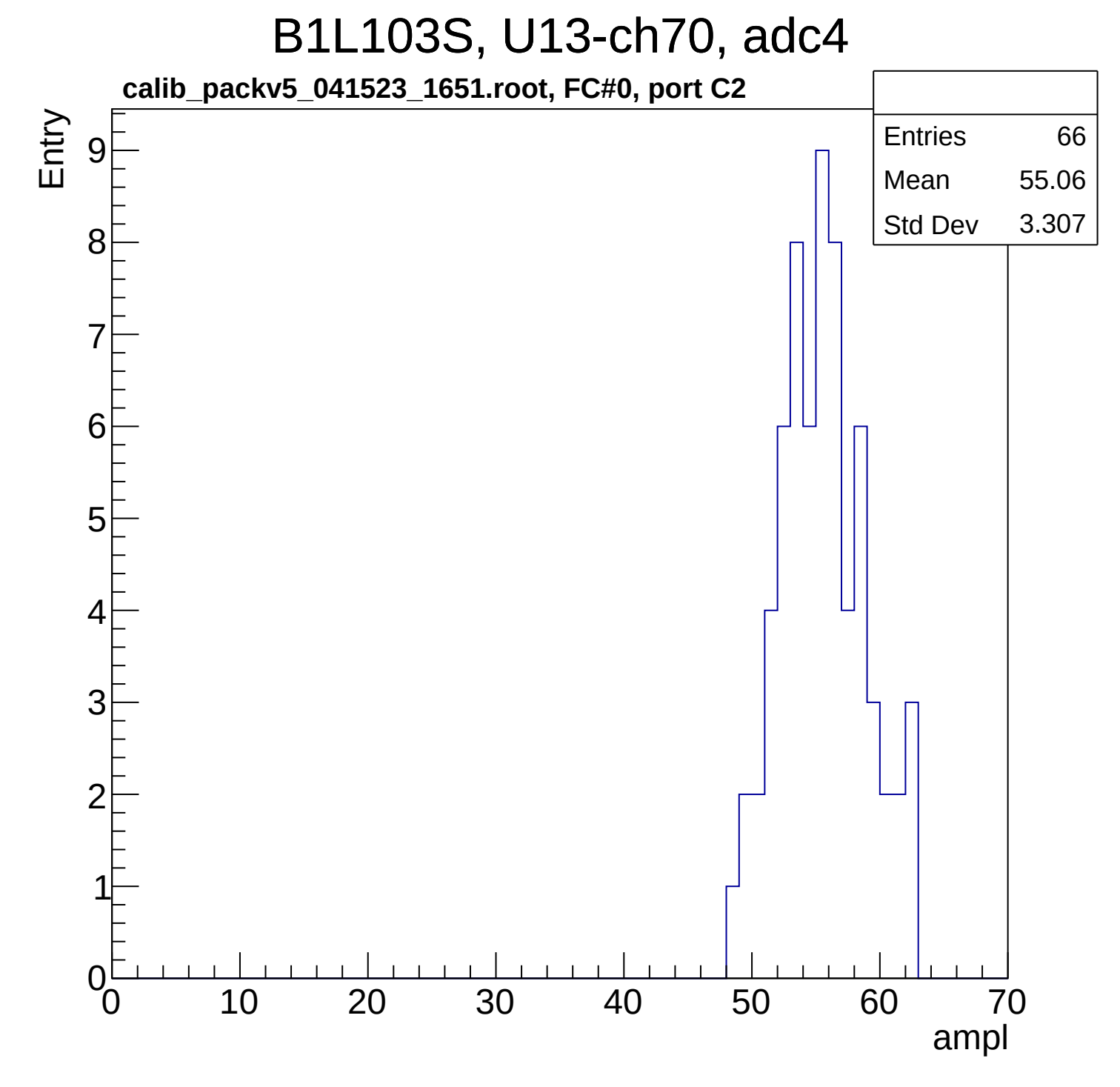
20
30
40
50
60
70


B1L103S, U13-ch70, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 55.06
Std Dev 3.307
Entry
ampl
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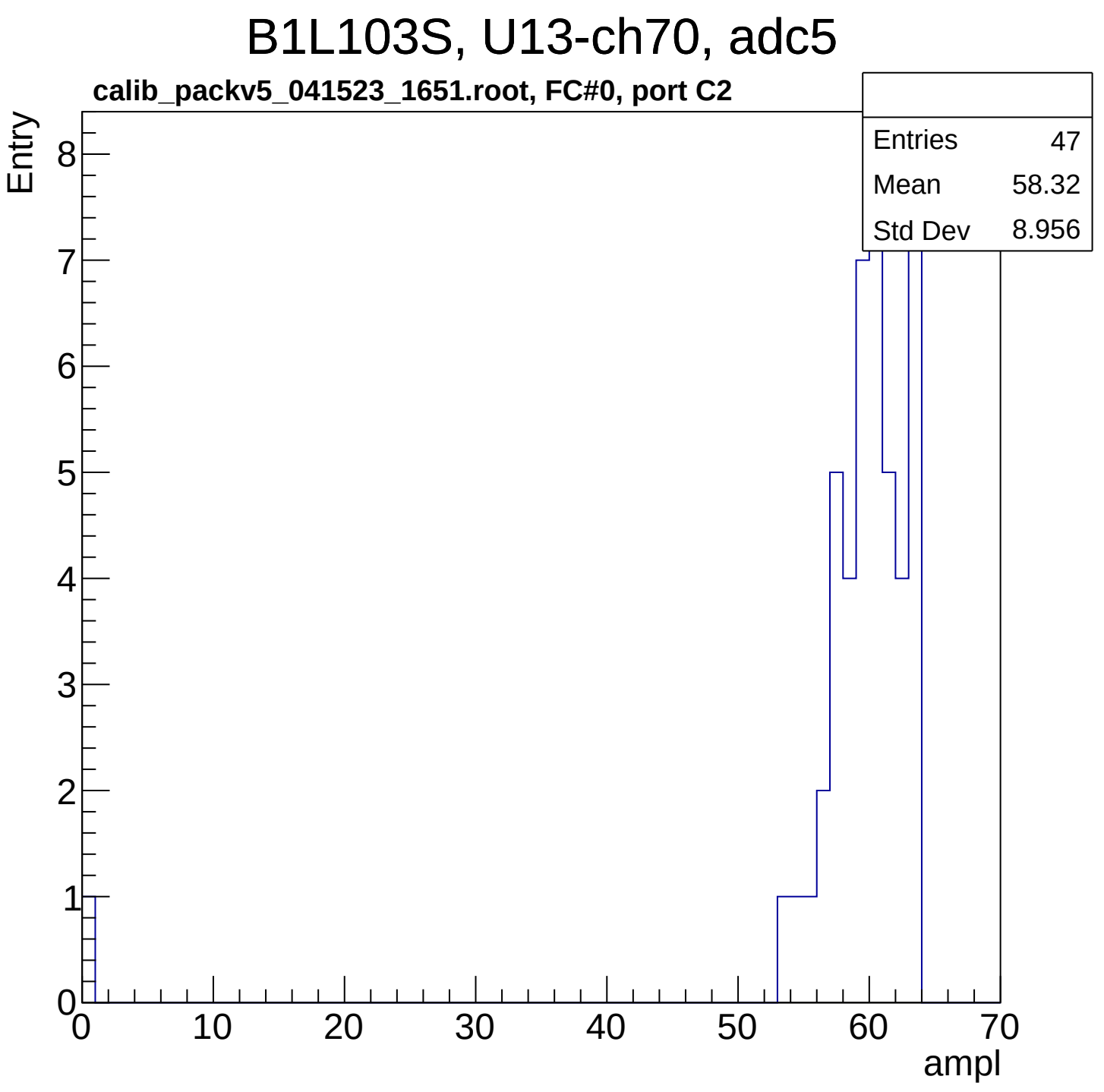
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch70, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.32
Std Dev 8.956
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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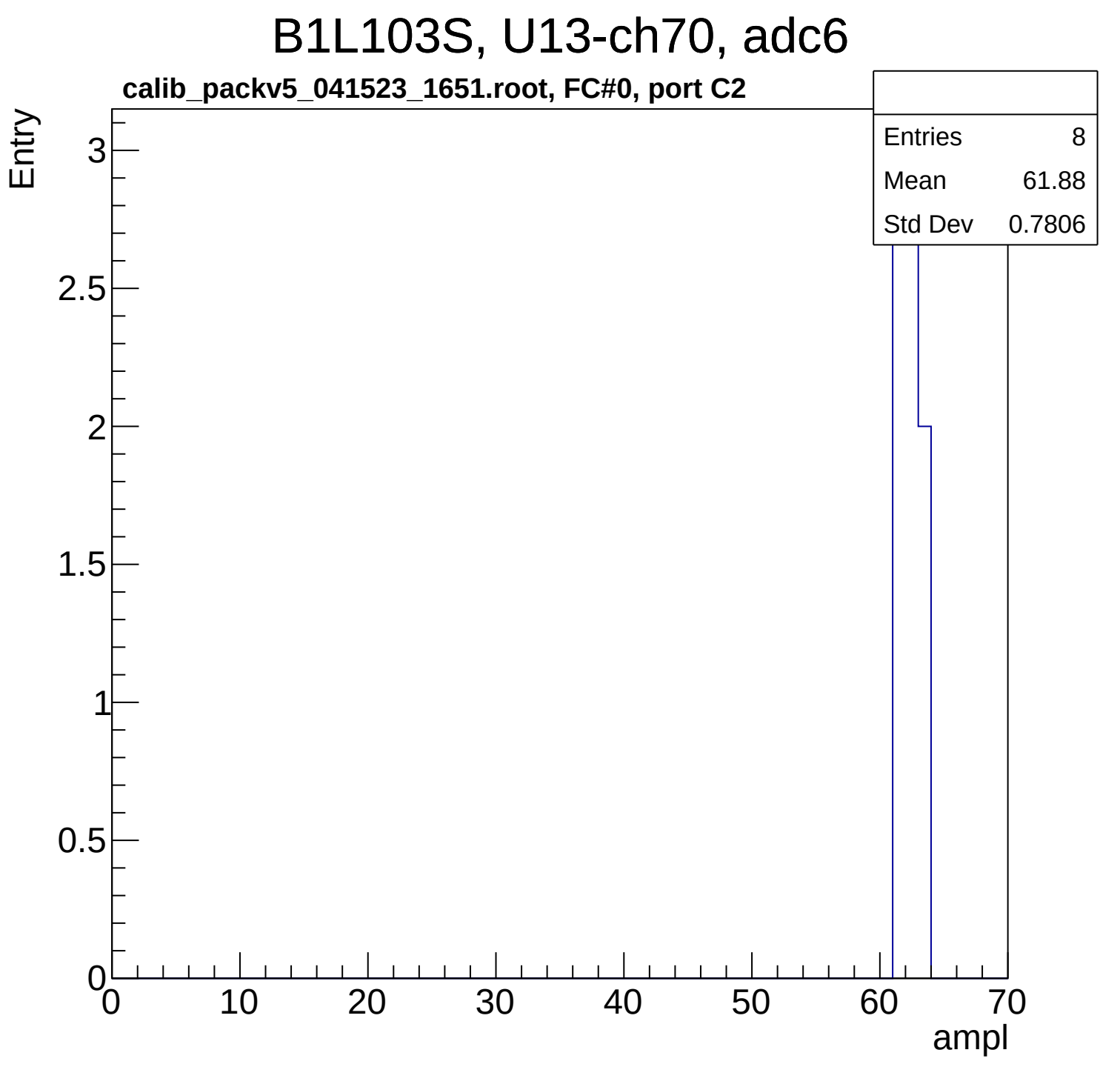
B1L103S, U13-ch70, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.88
Std Dev 0.7806
Entry
ampl
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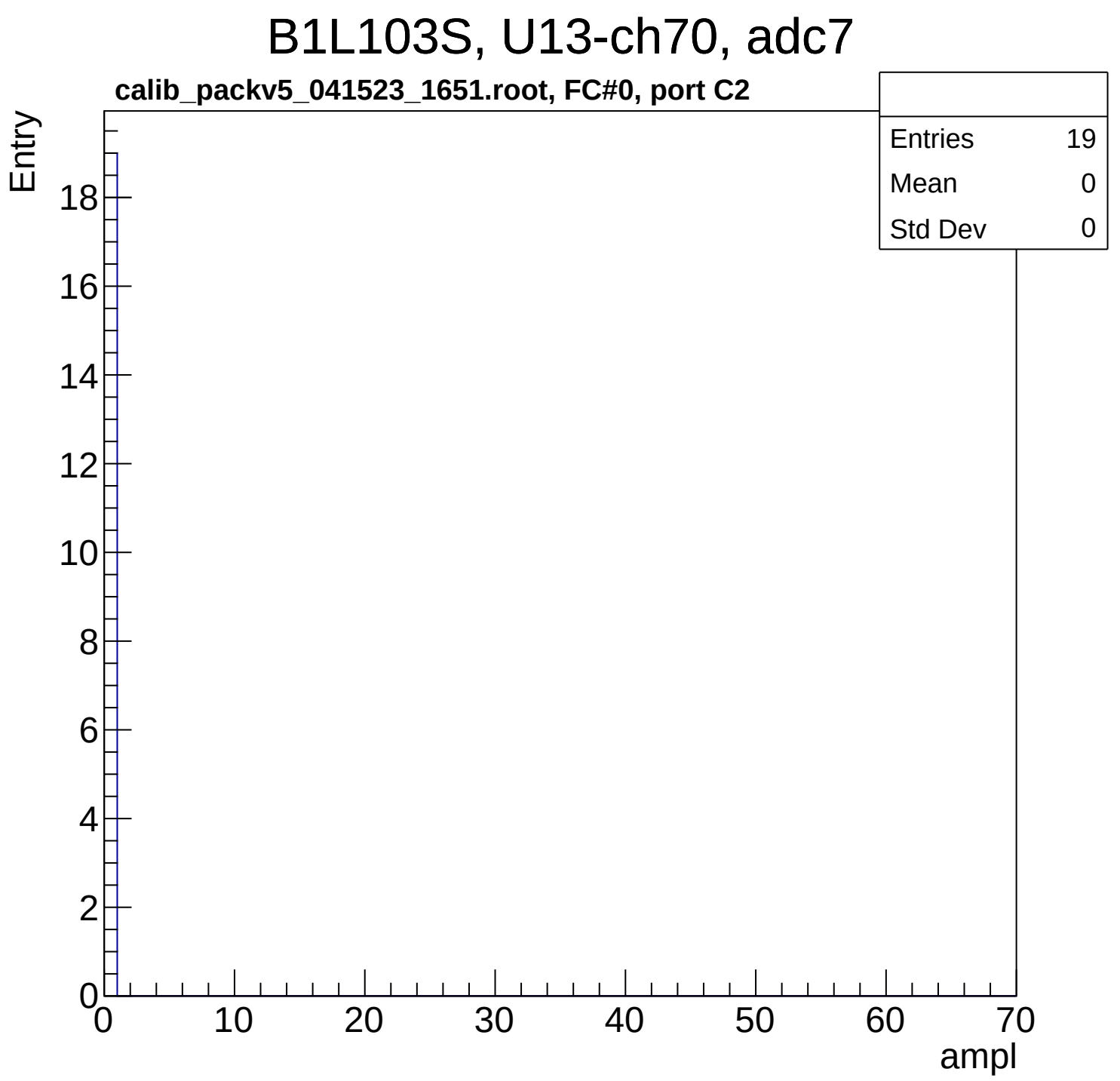
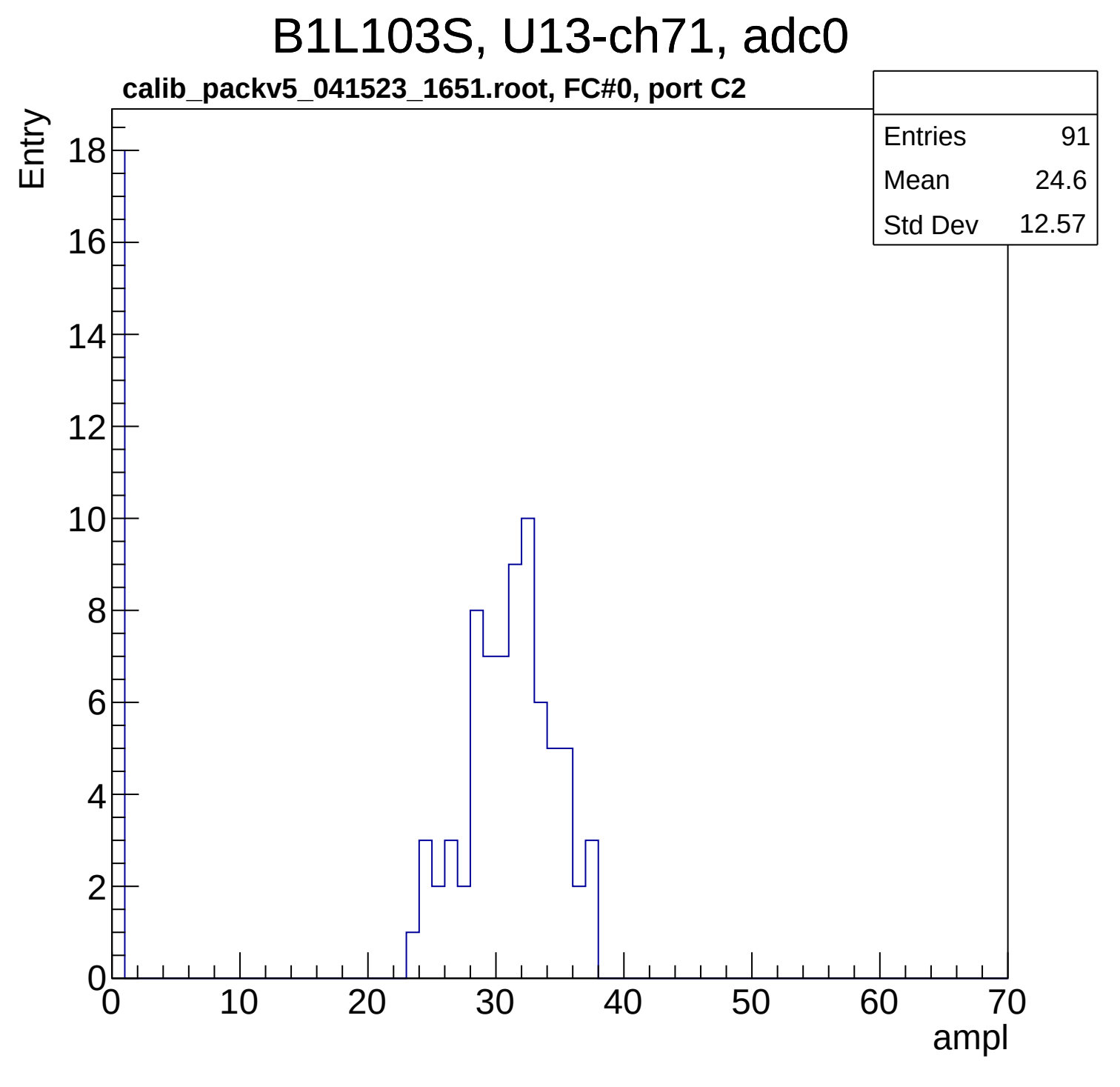
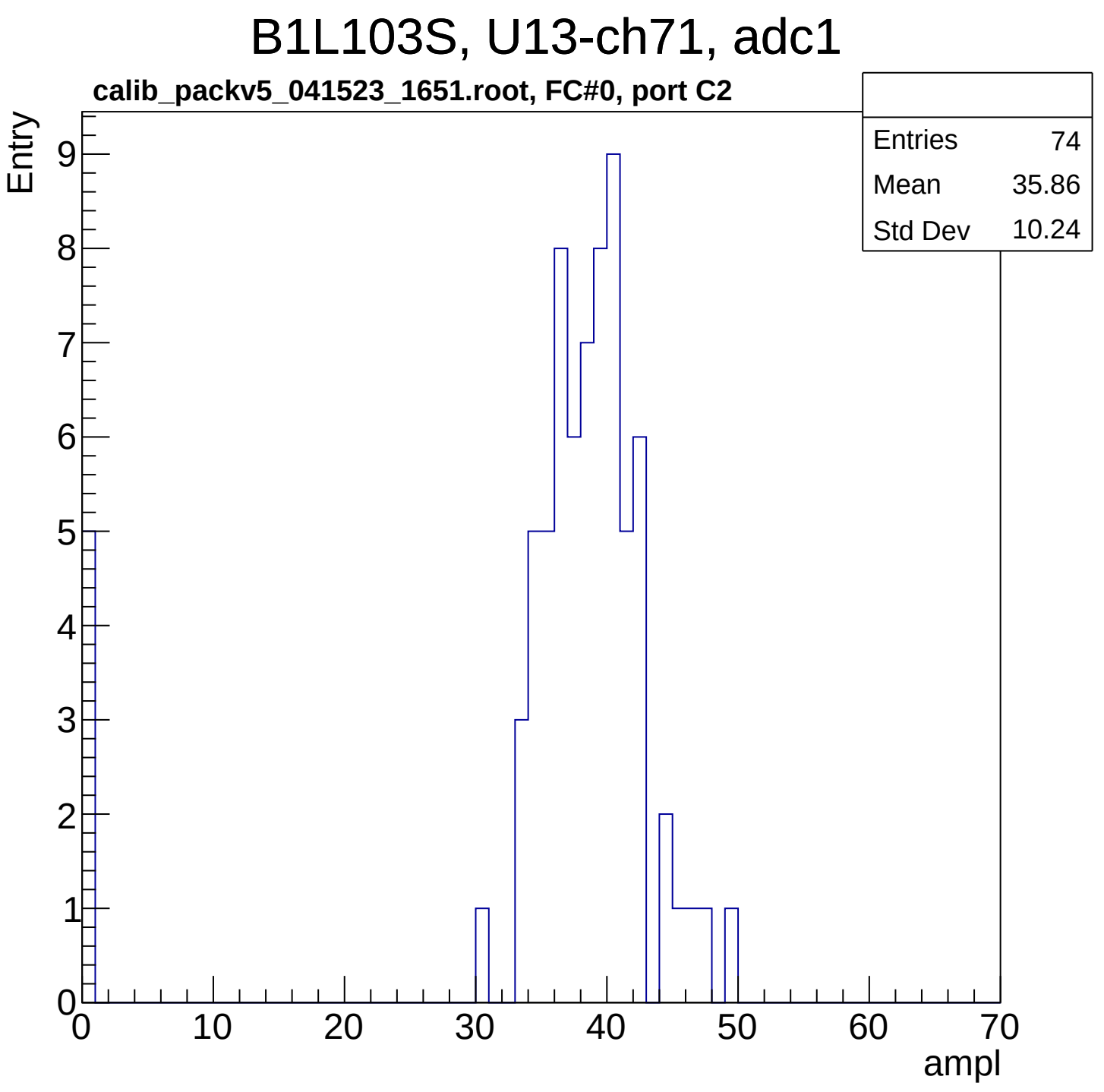
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U13-ch70, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch71, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 24.6
Std Dev 12.57
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch71, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 35.86
Std Dev 10.24
Entry
ampl
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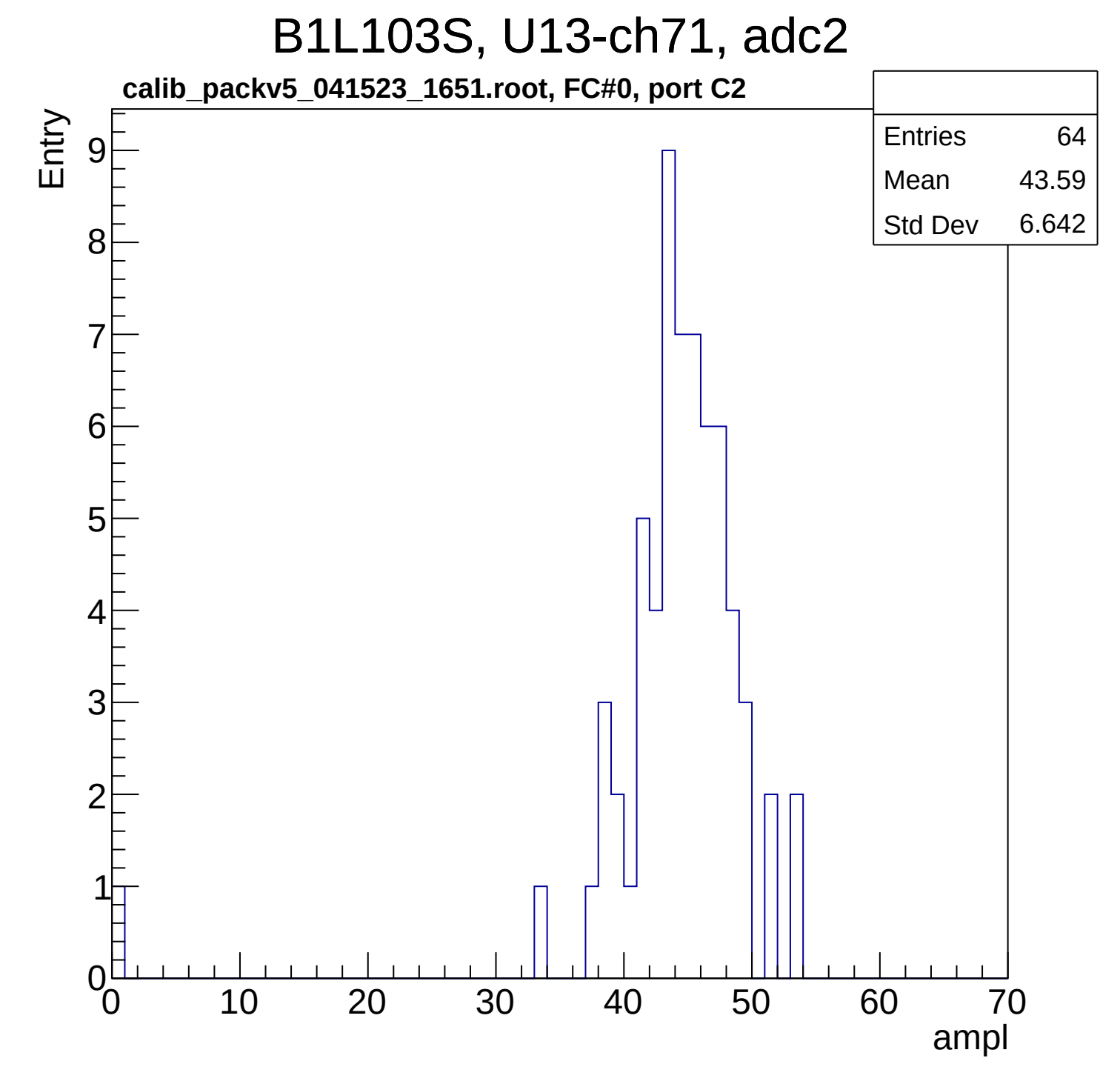
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch71, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 43.59
Std Dev 6.642
Entry
ampl
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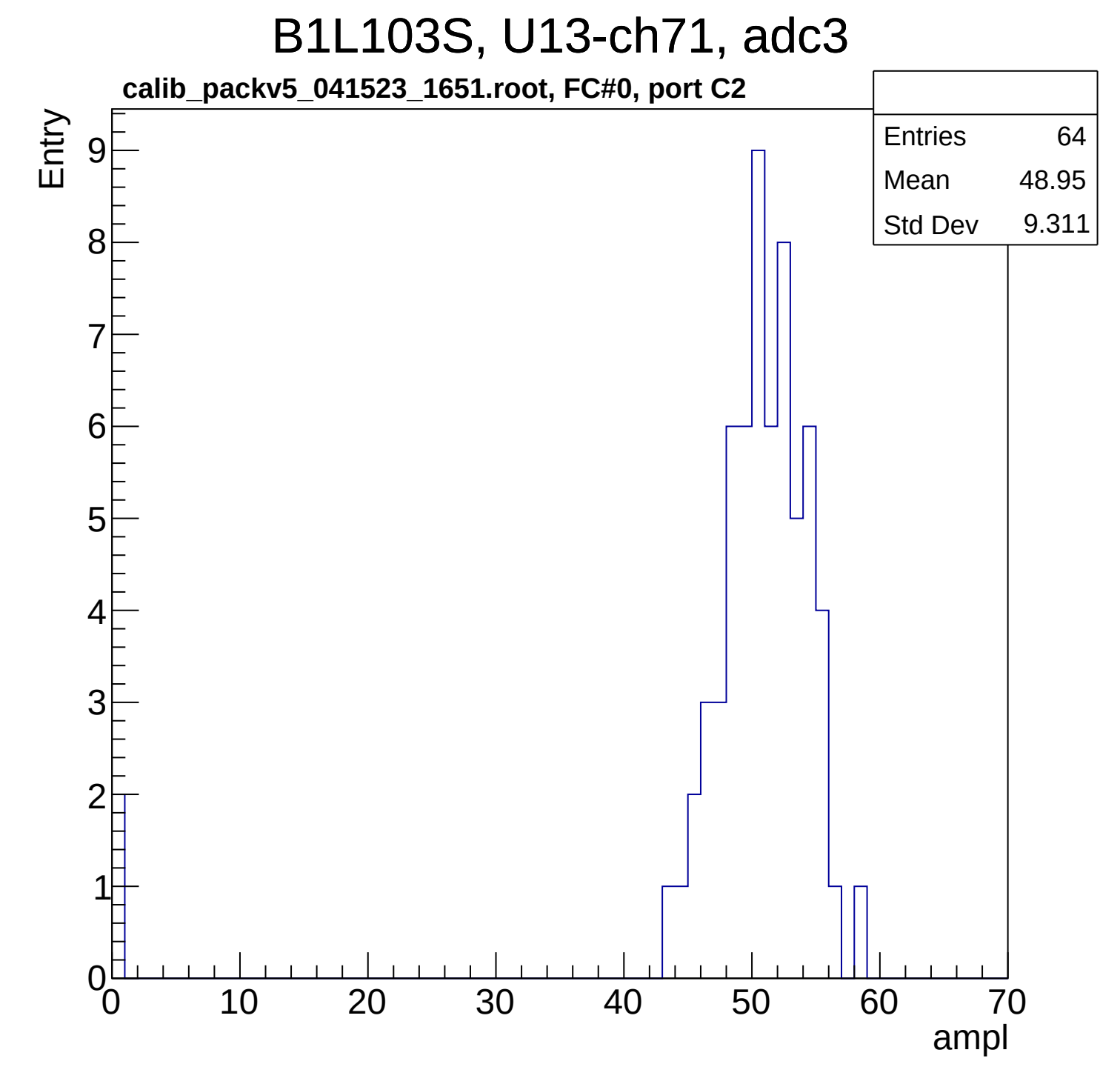
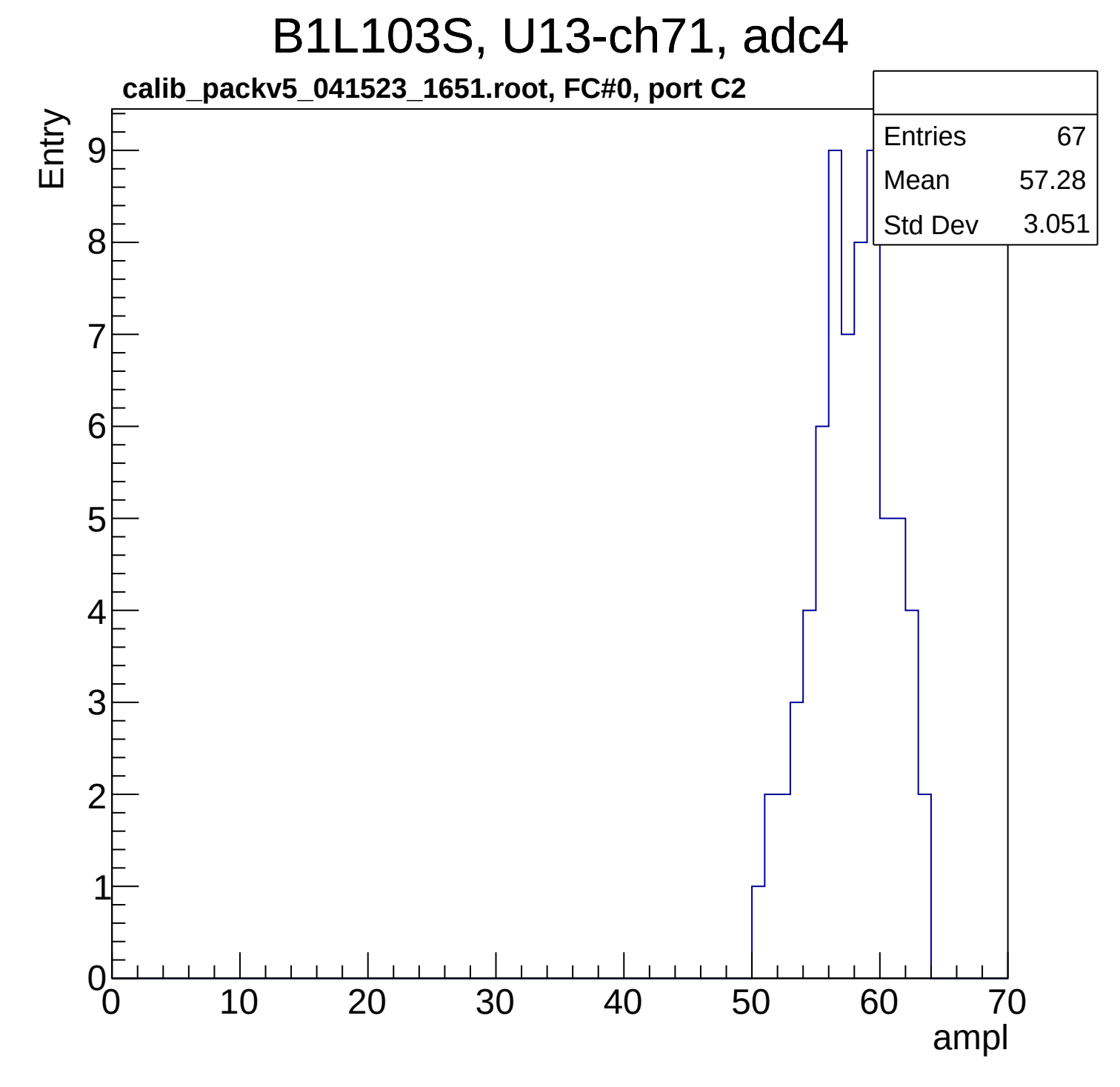
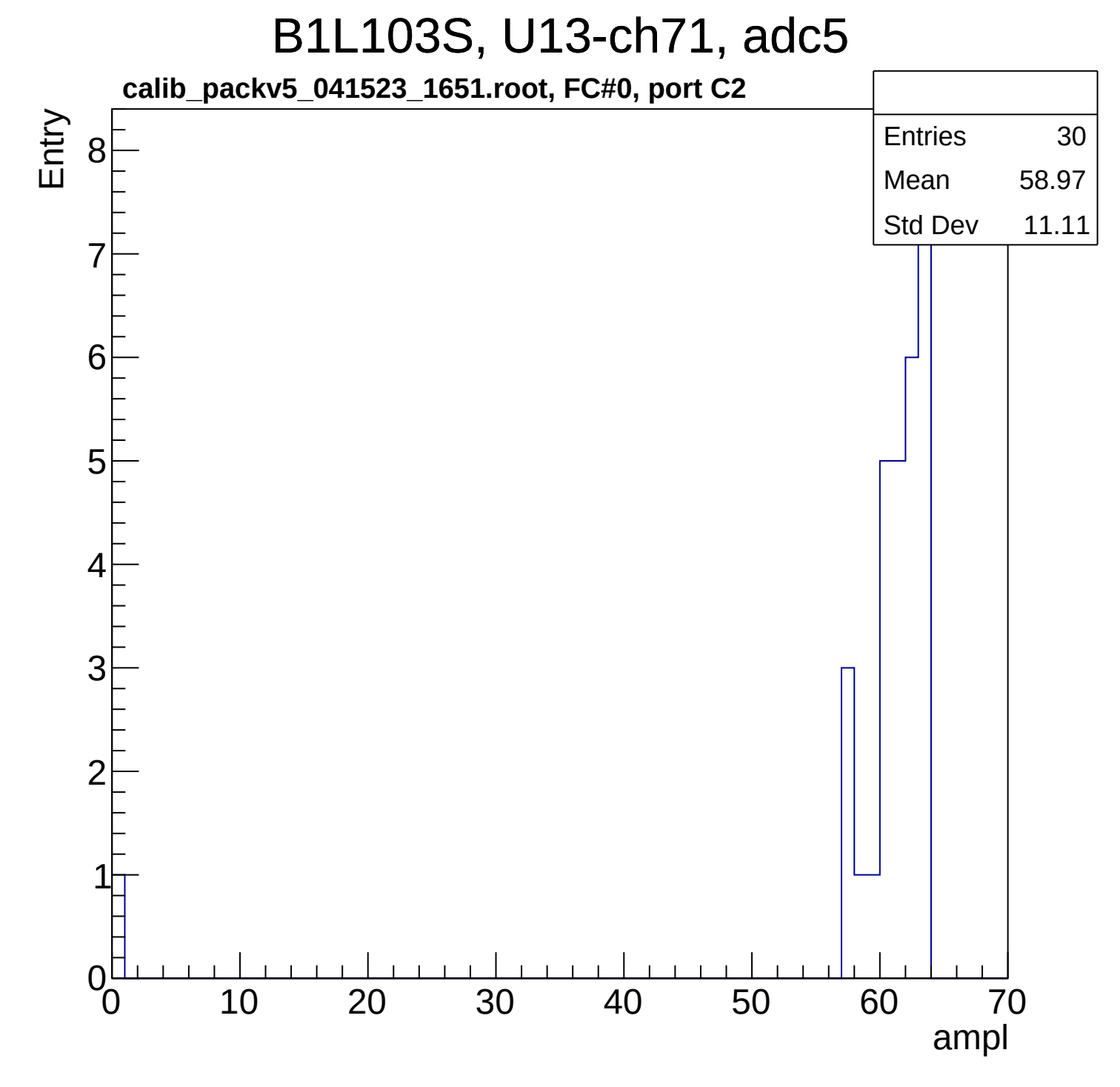
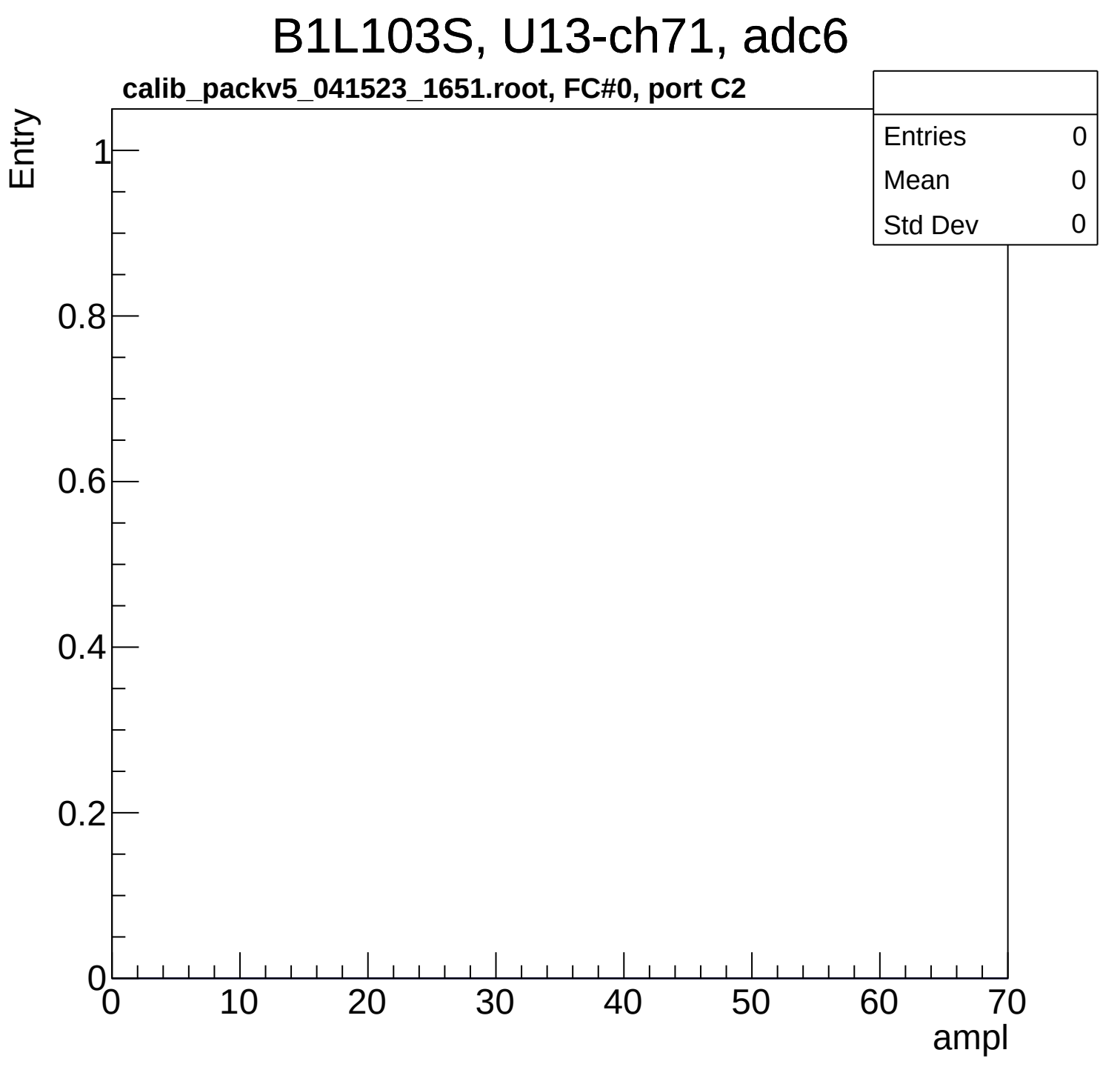
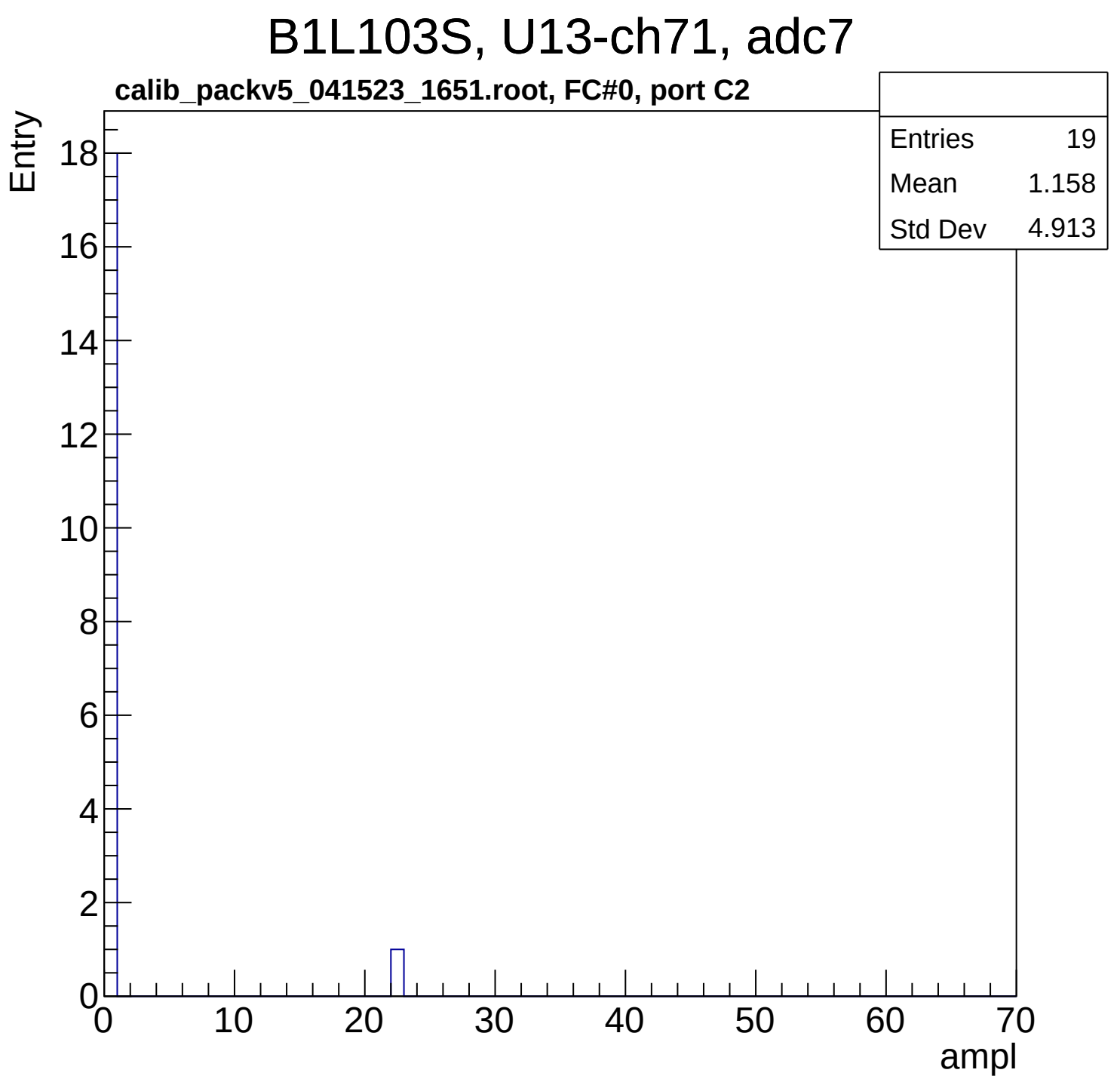
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

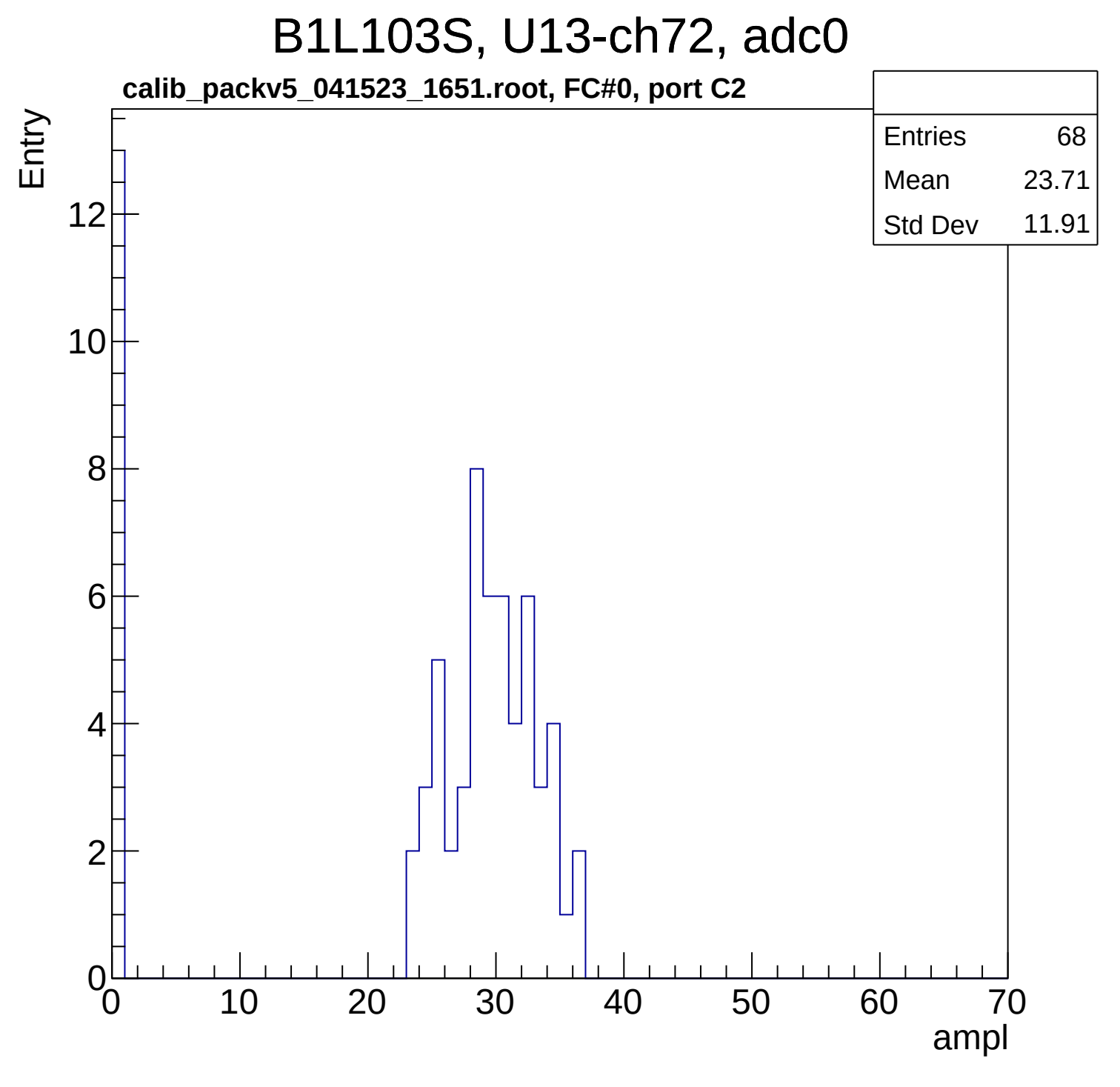

B1L103S, U13-ch71, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 48.95
Std Dev 9.311
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

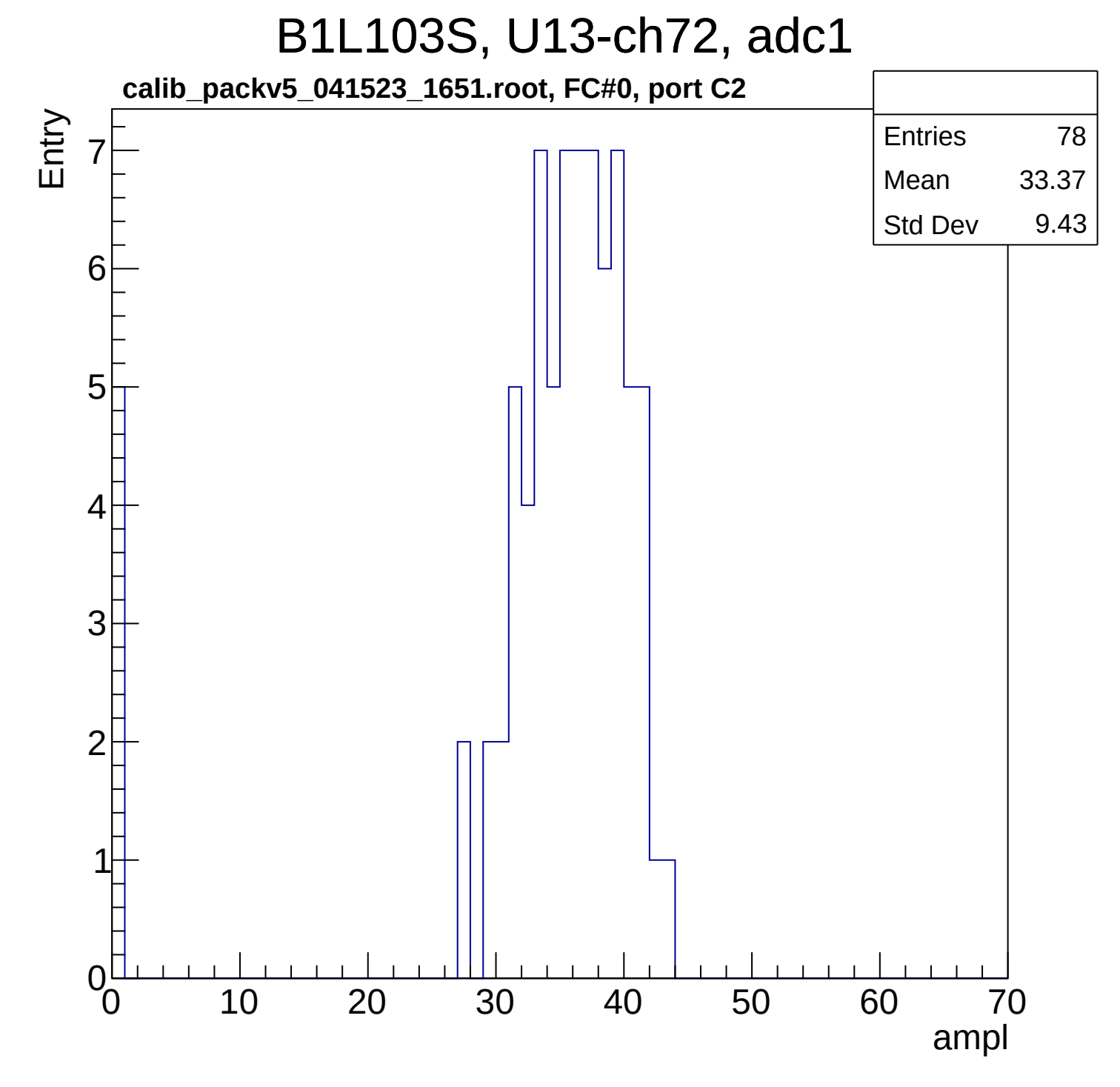

B1L103S, U13-ch71, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 57.28
Std Dev 3.051
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

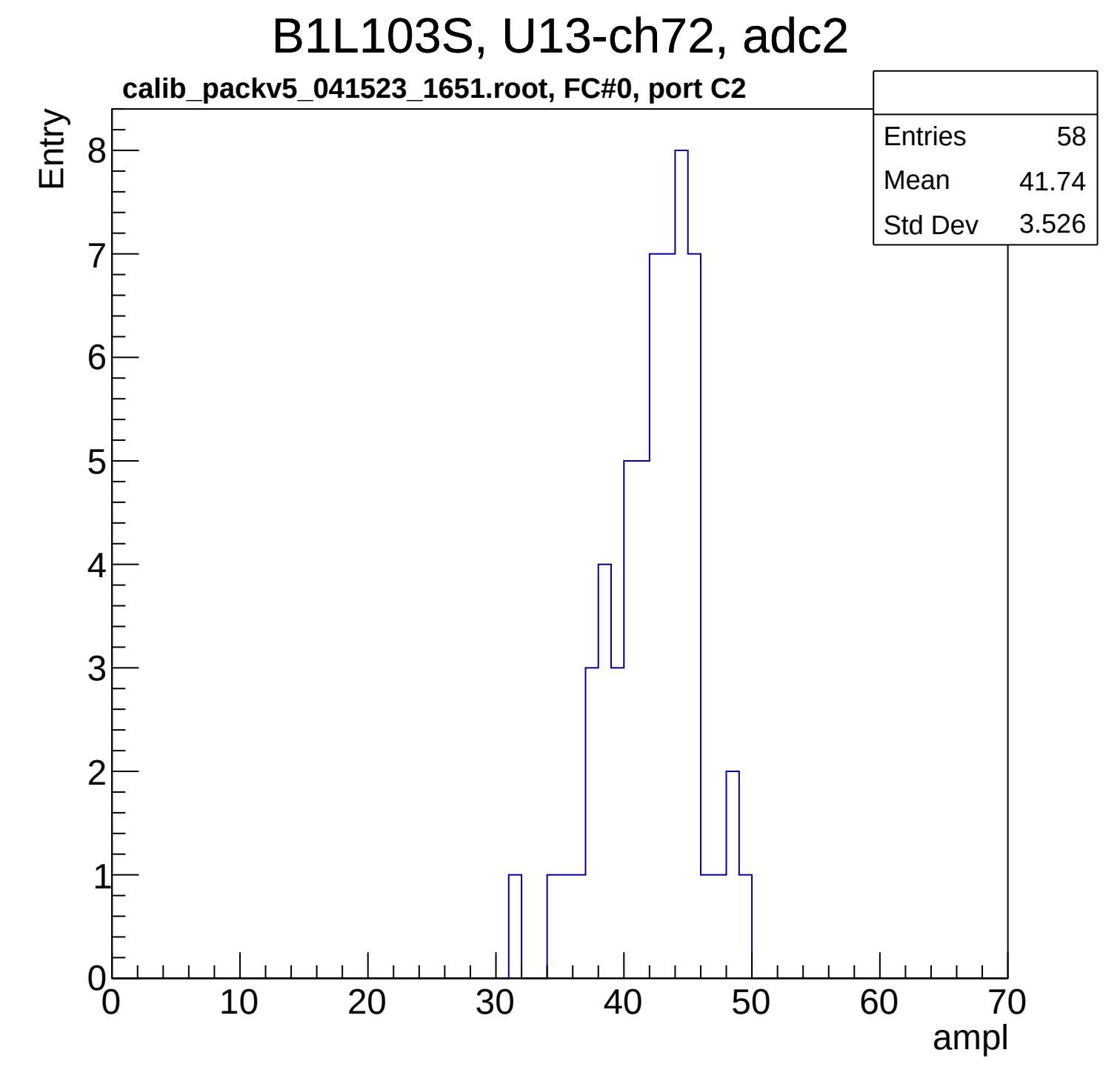

B1L103S, U13-ch71, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 58.97
Std Dev 11.11
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch71, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch71, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch72, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 23.71
Std Dev 11.91
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch72, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 33.37
Std Dev 9.43
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch72, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 41.74
Std Dev 3.526
Entry
ampl
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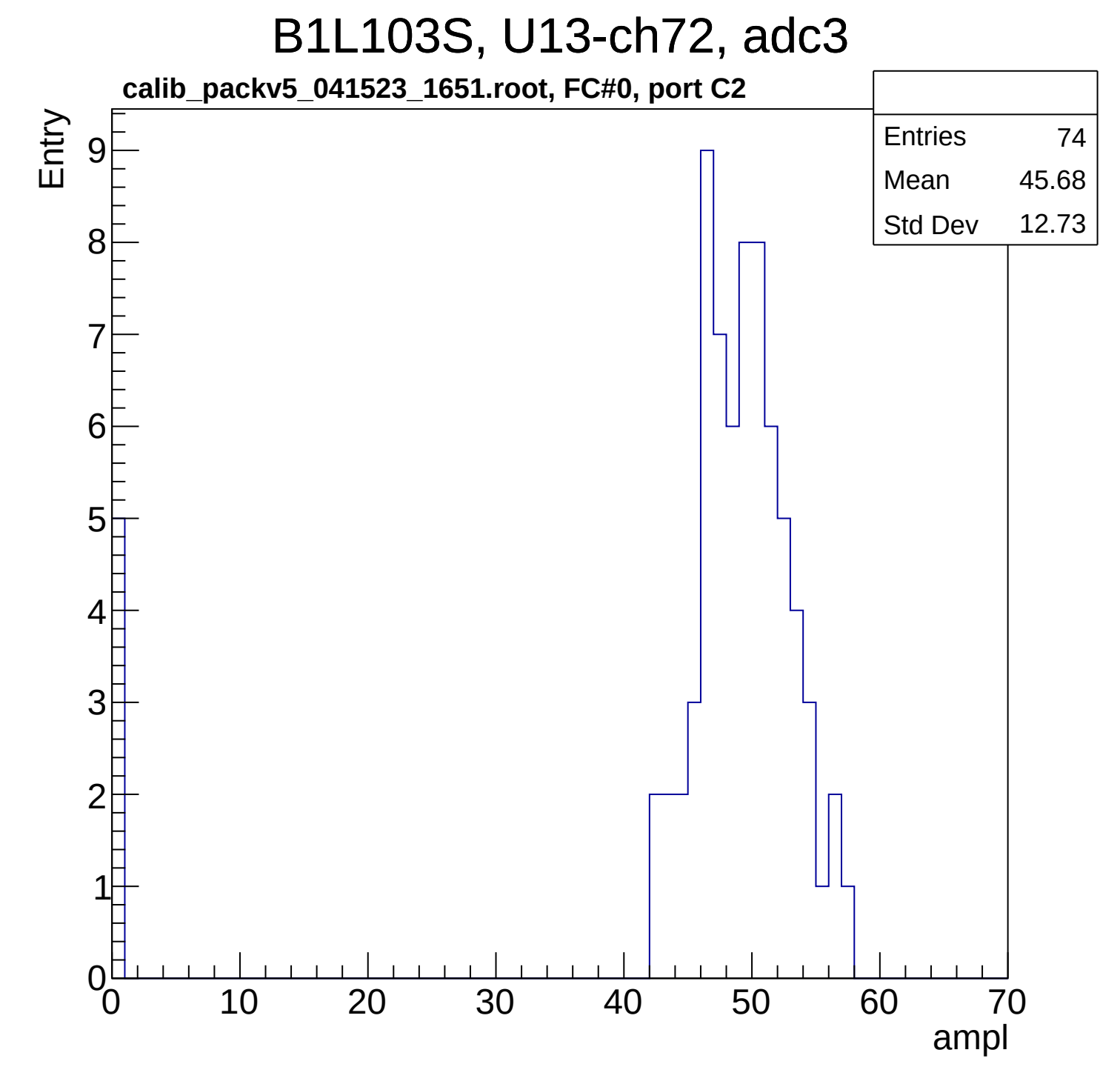
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch72, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 45.68
Std Dev 12.73
Entry
ampl
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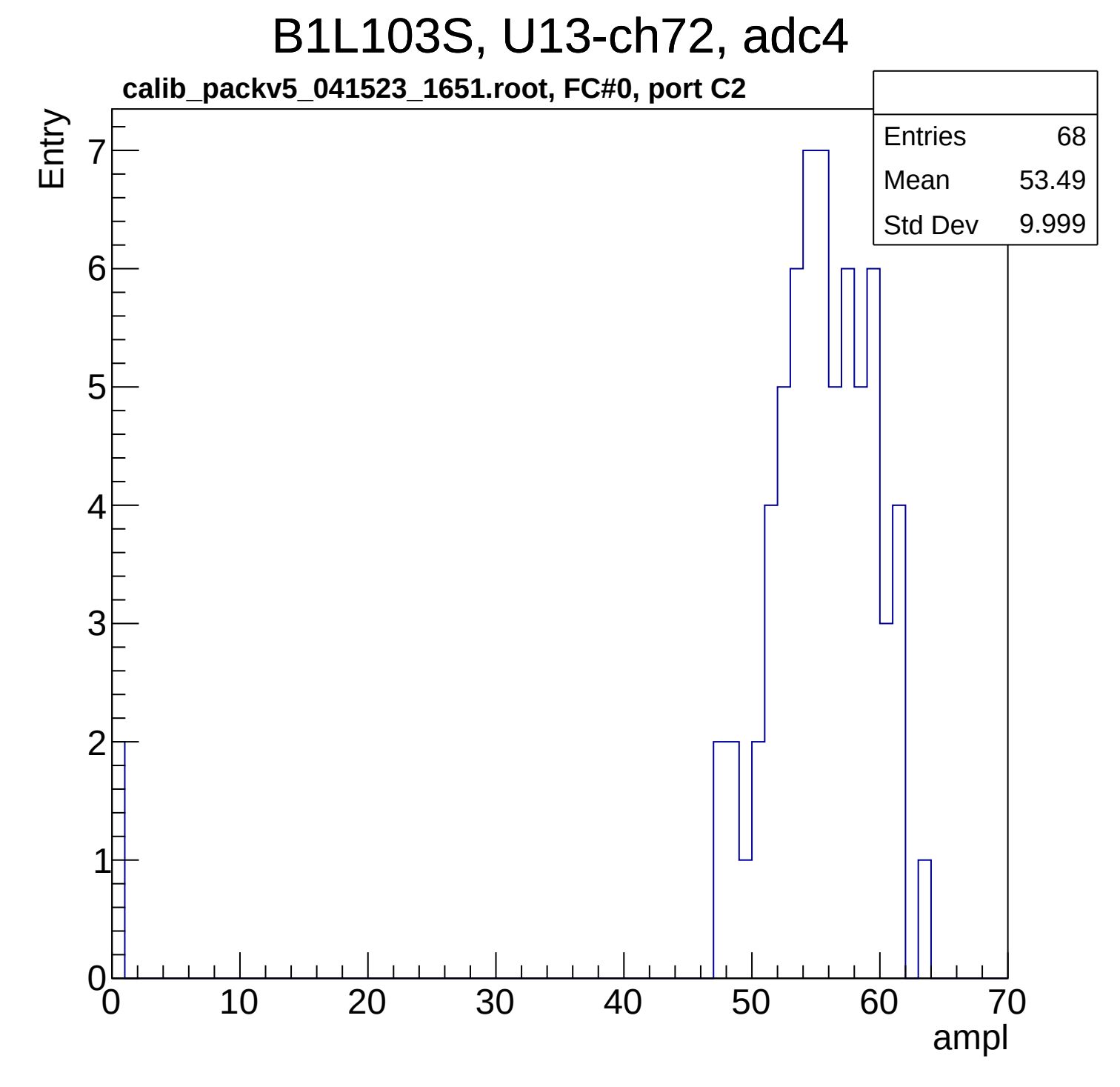
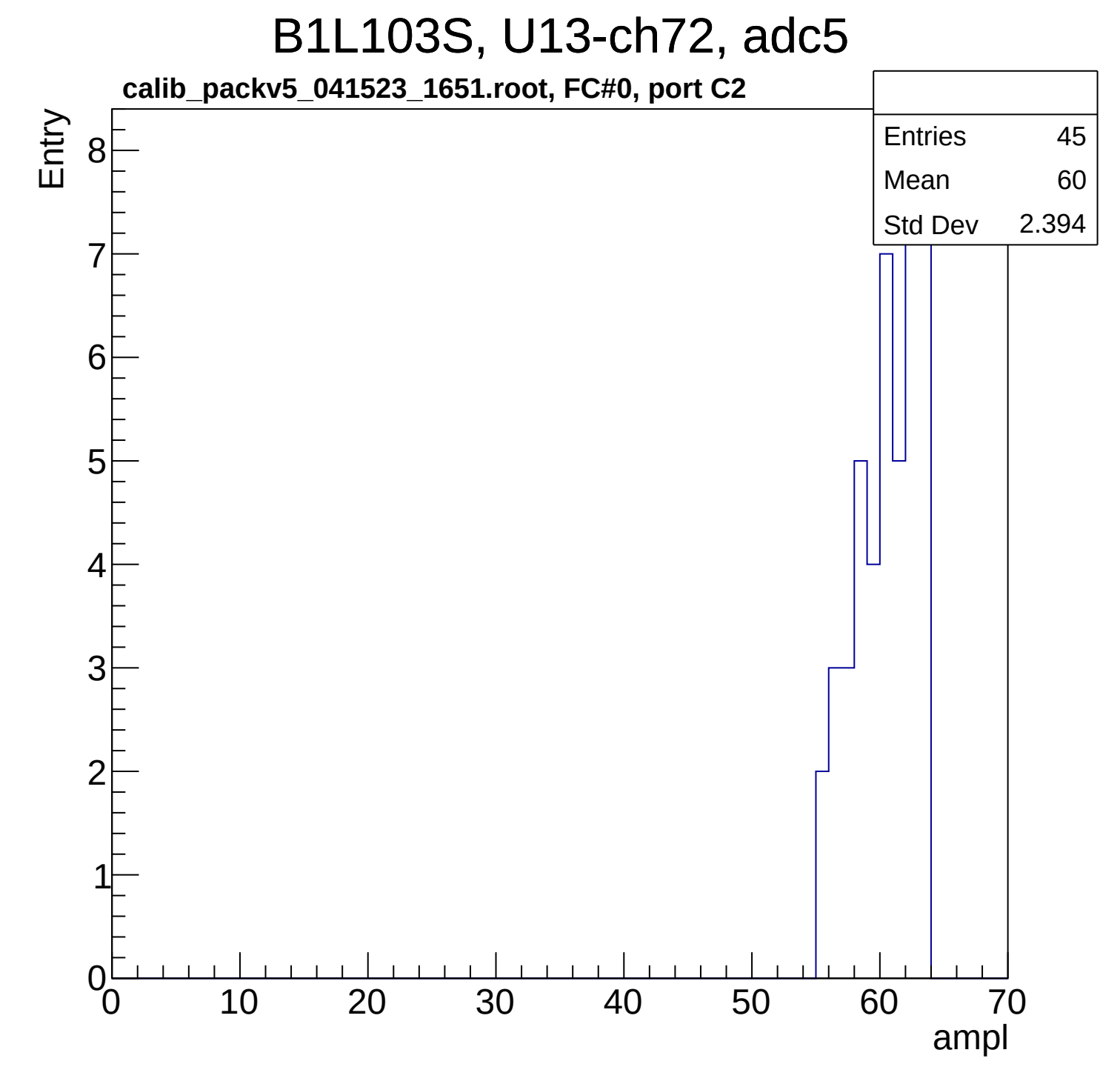
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch72, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 53.49
Std Dev 9.999
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch72, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 60
Std Dev 2.394
Entry
ampl
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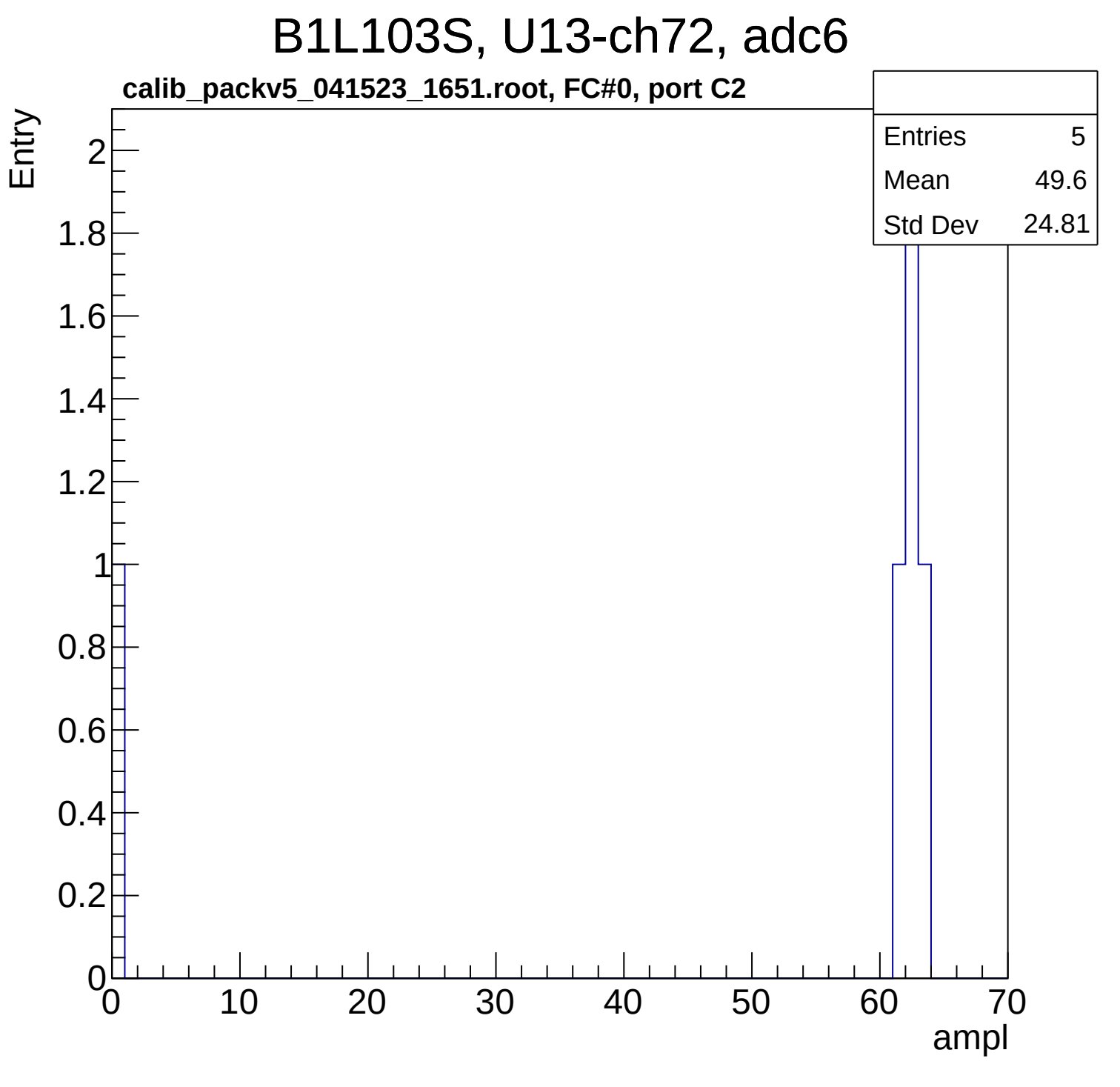
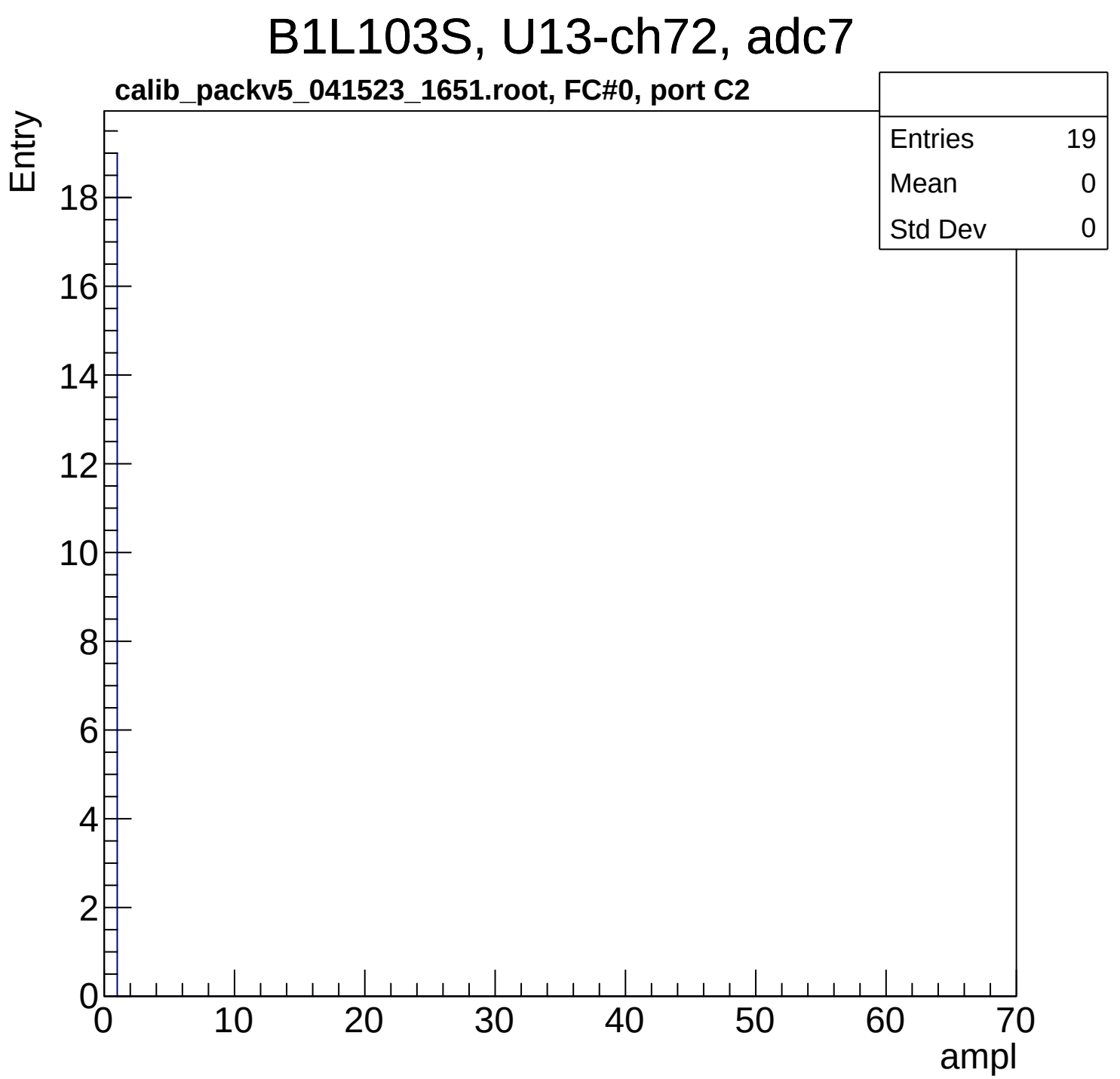
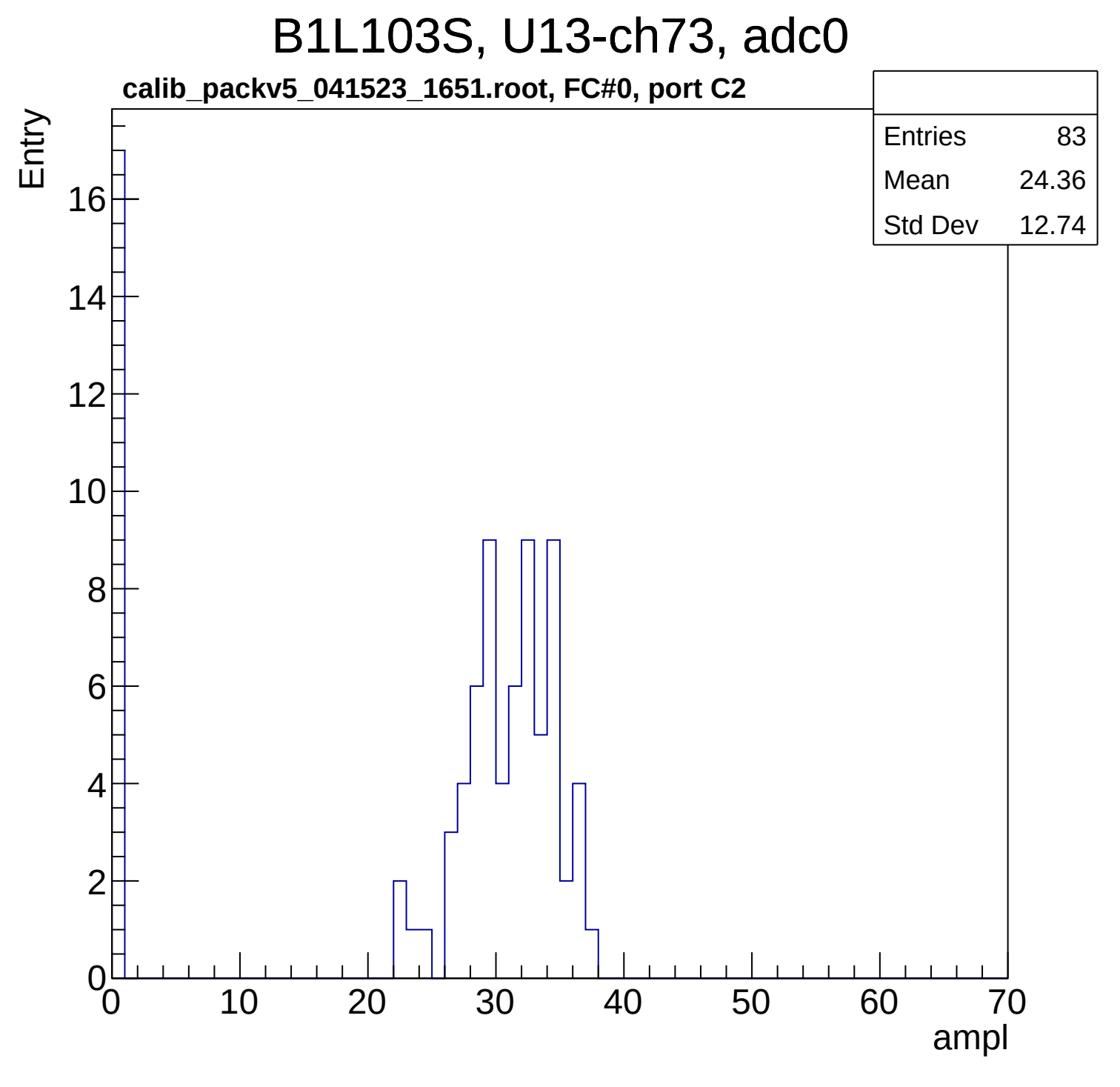
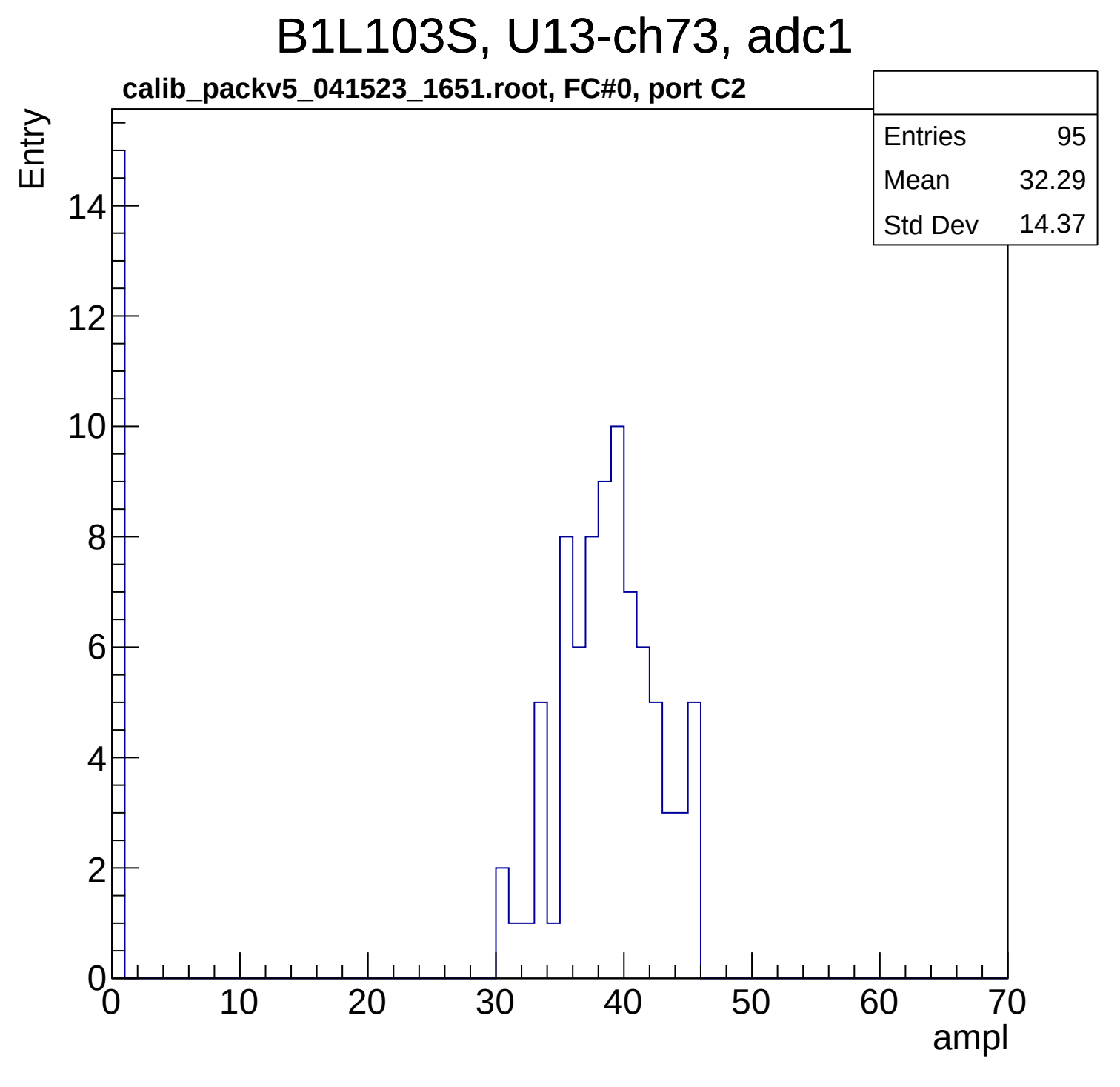
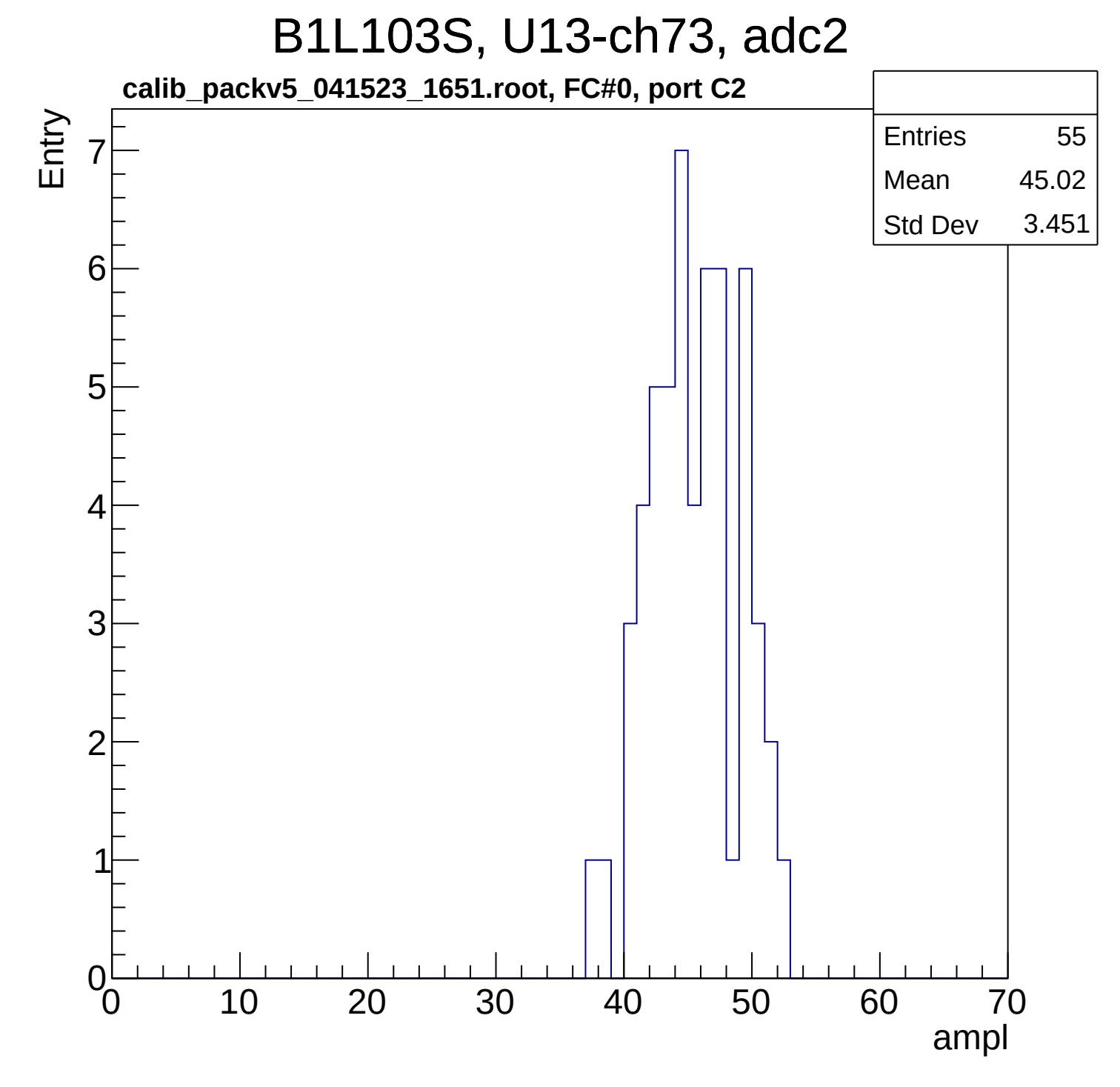
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch72, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 49.6
Std Dev 24.81
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U13-ch72, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch73, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 24.36
Std Dev 12.74
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch73, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 32.29
Std Dev 14.37
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch73, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 45.02
Std Dev 3.451
Entry
ampl
0
1
2
3
4
5
6
7
0
10
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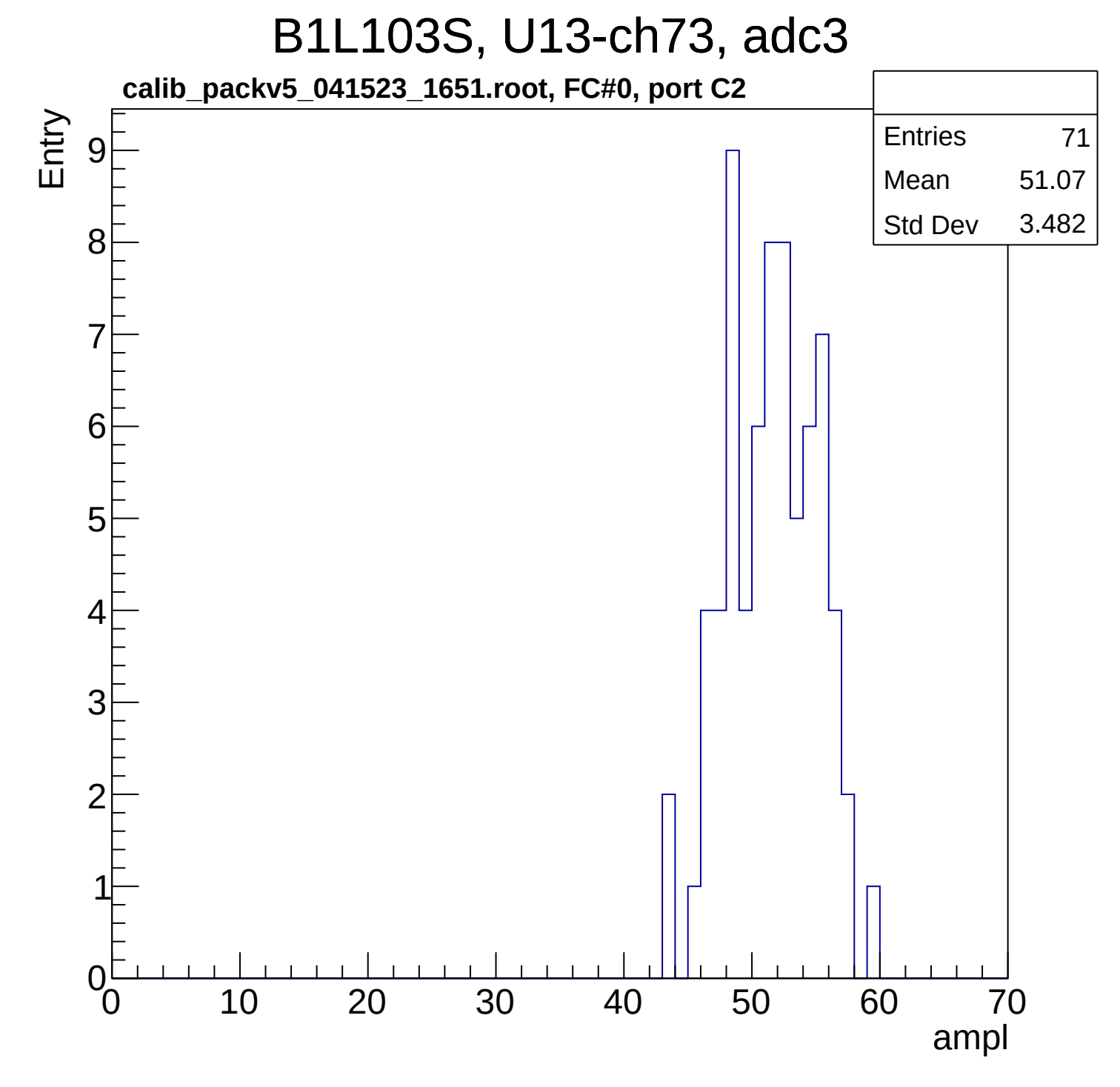
30
40
50
60
70


B1L103S, U13-ch73, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 51.07
Std Dev 3.482
Entry
ampl
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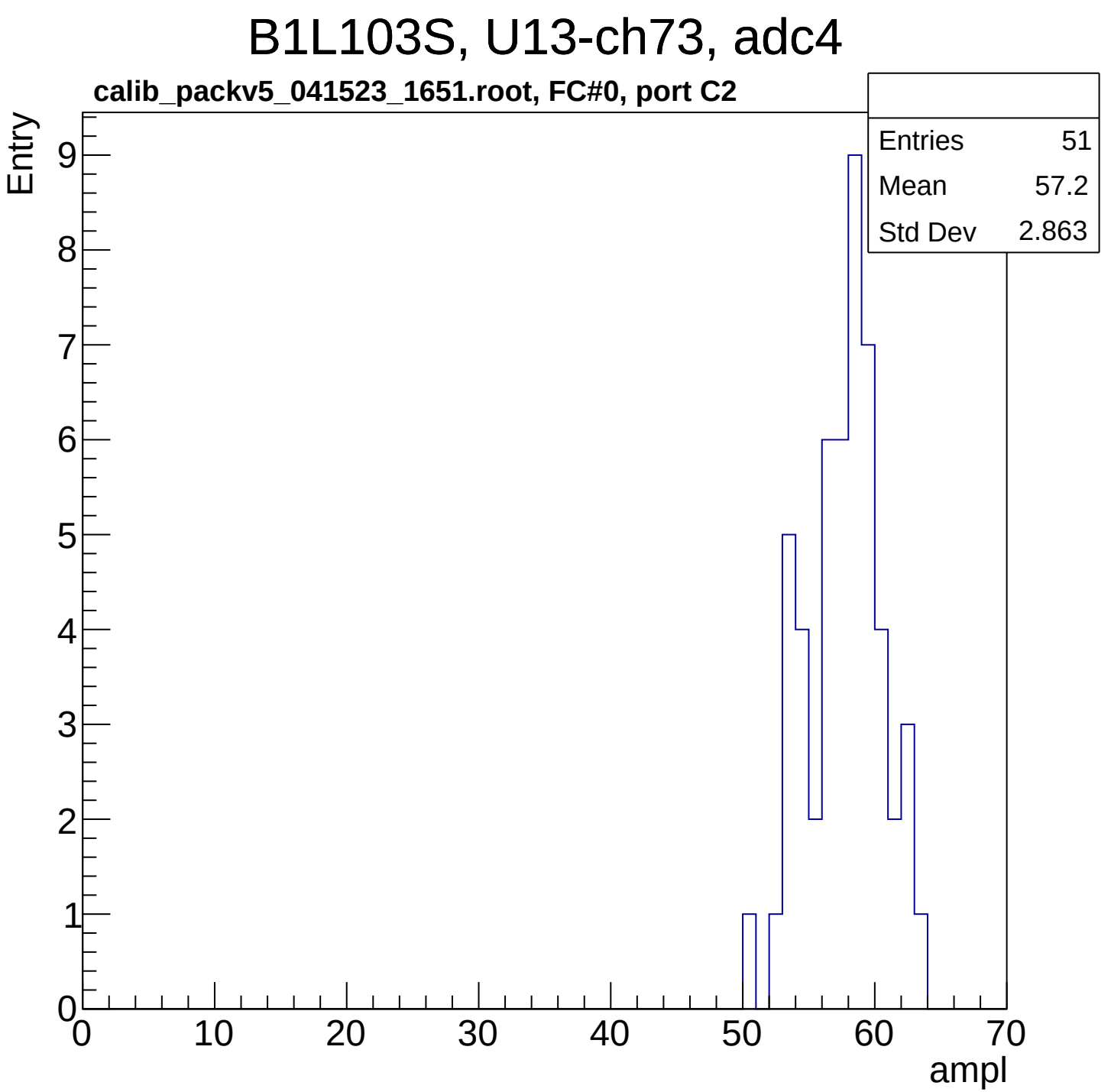
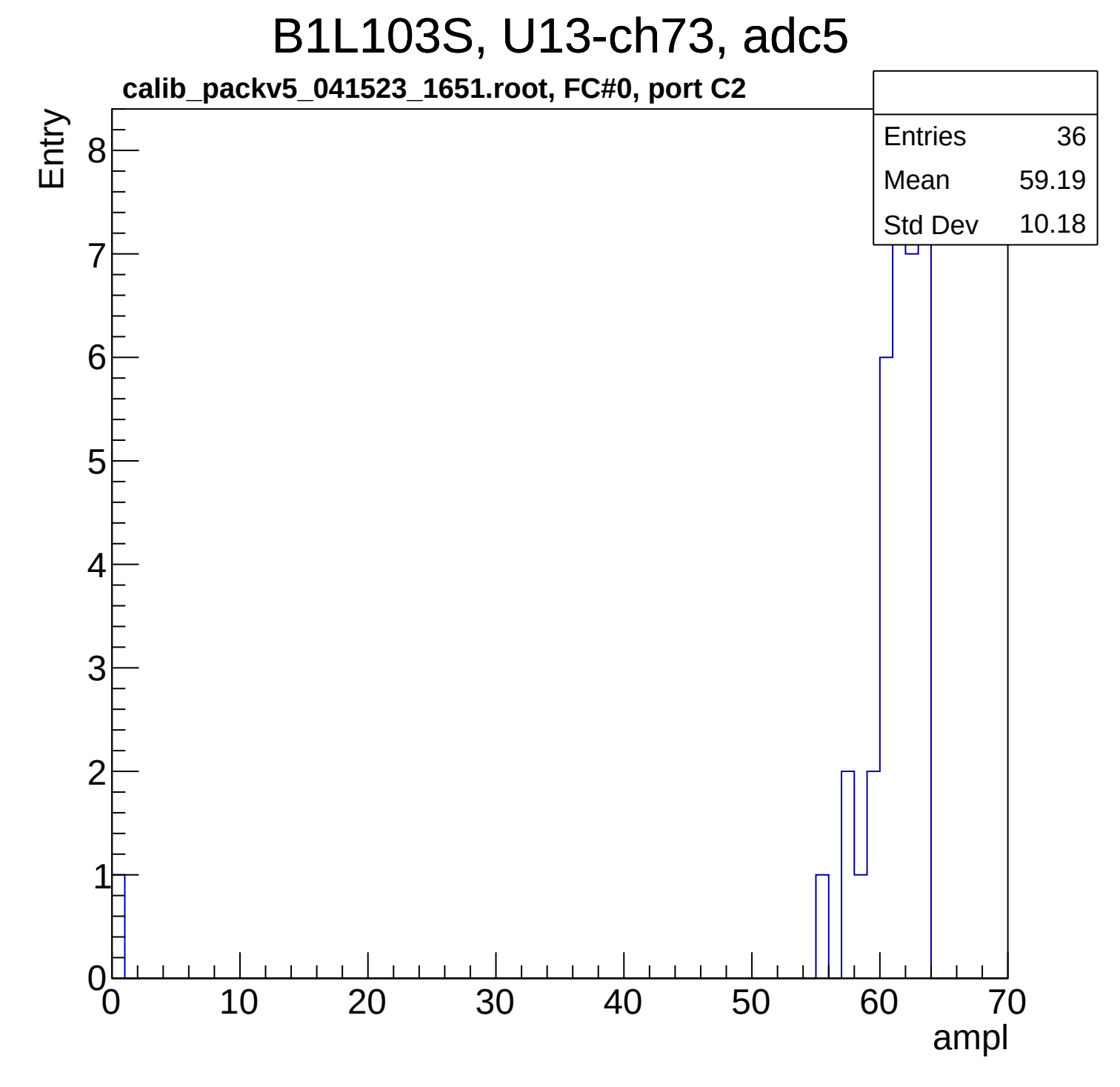
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch73, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 57.2
Std Dev 2.863
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch73, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 59.19
Std Dev 10.18
Entry
ampl
0
1
2
3
4
5
6
7
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0
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40
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60
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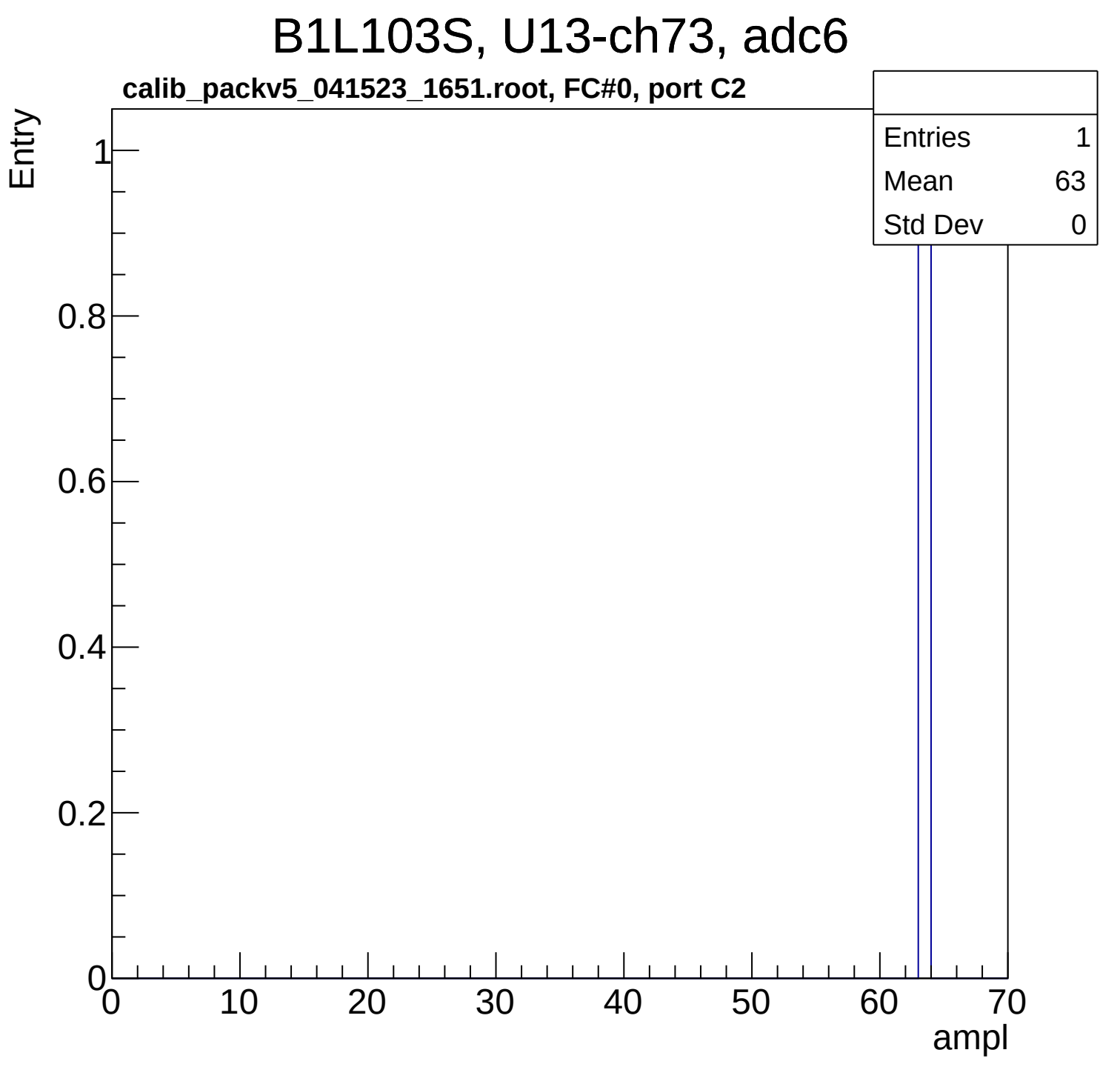
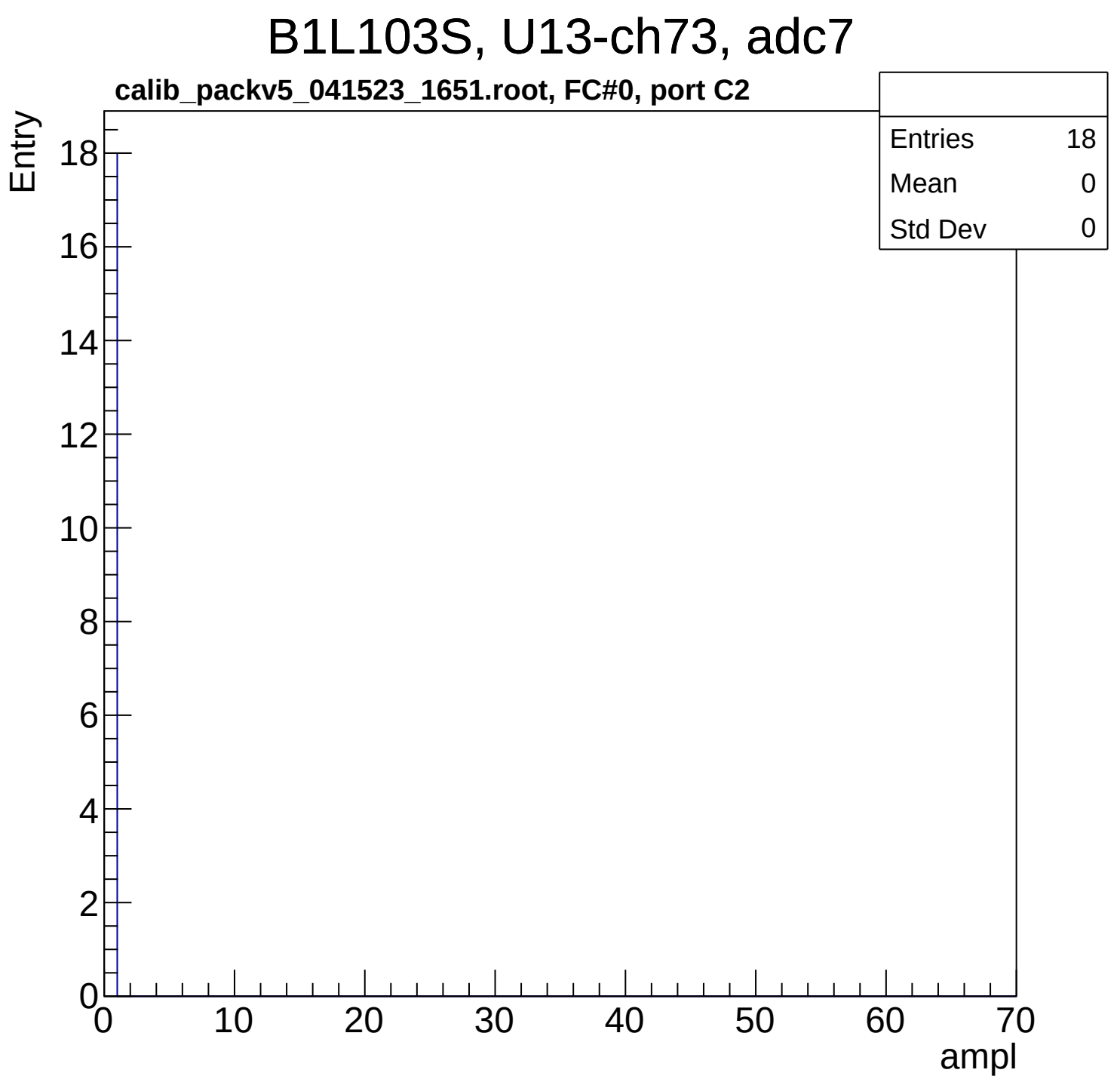
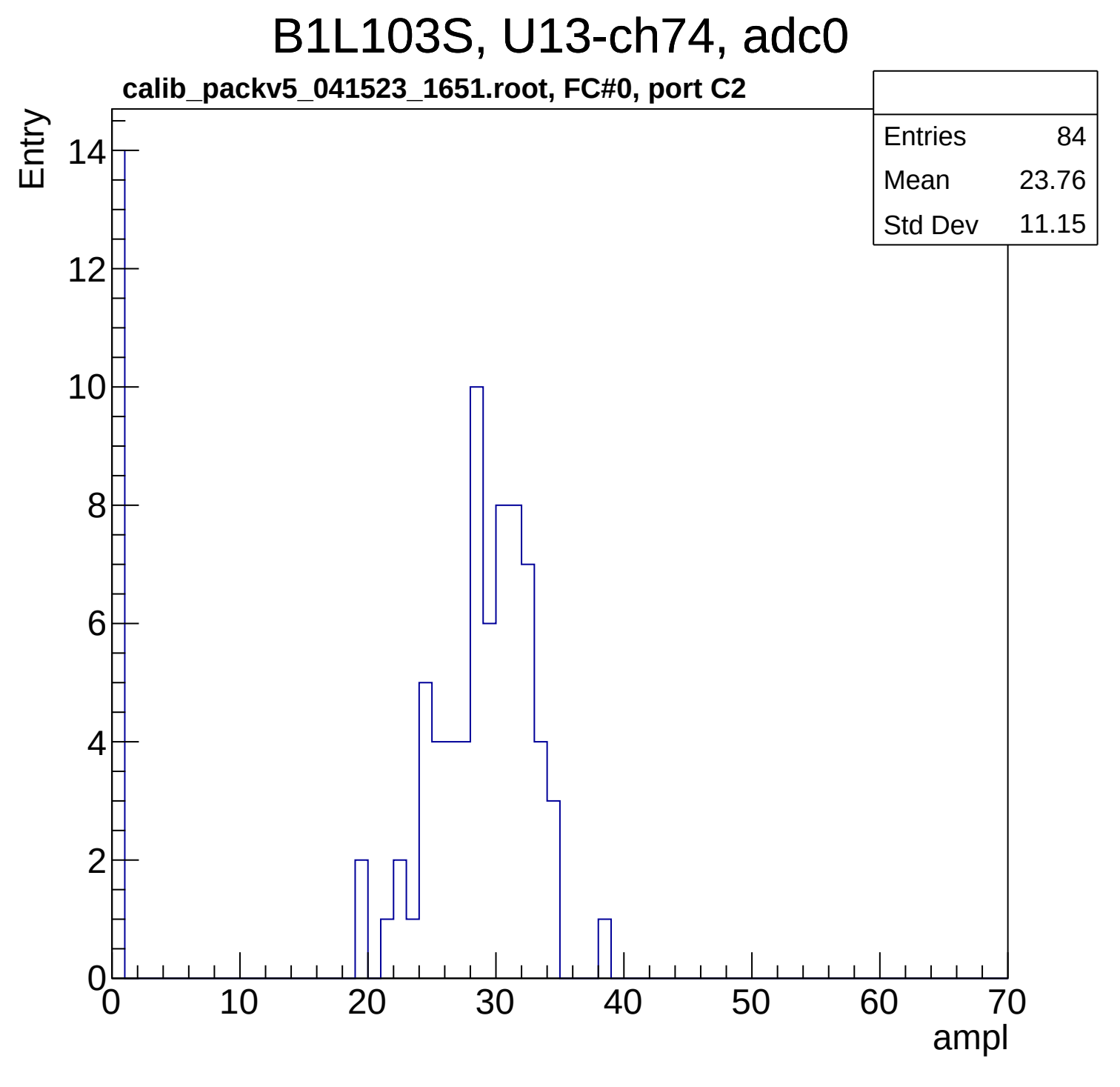
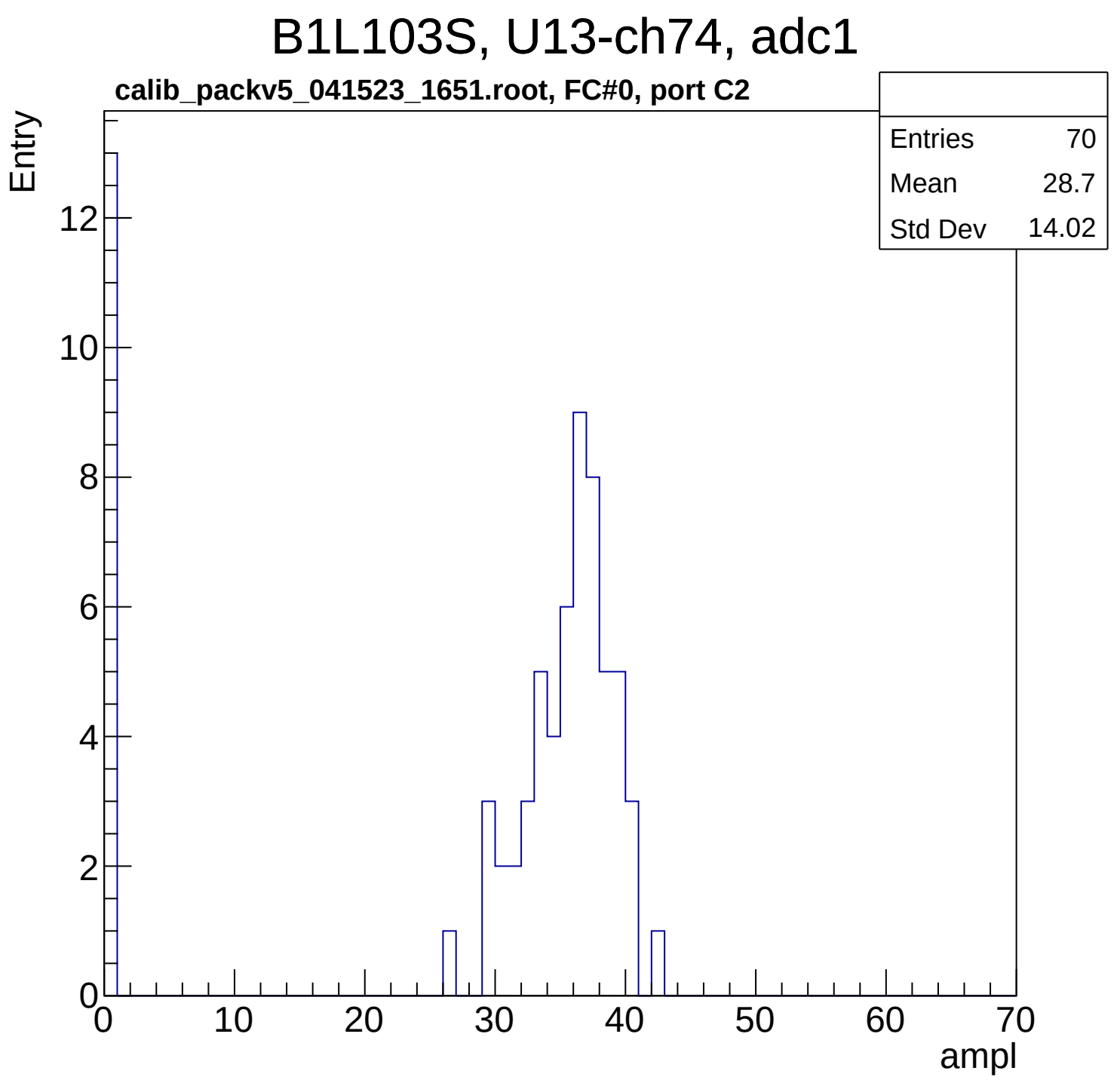
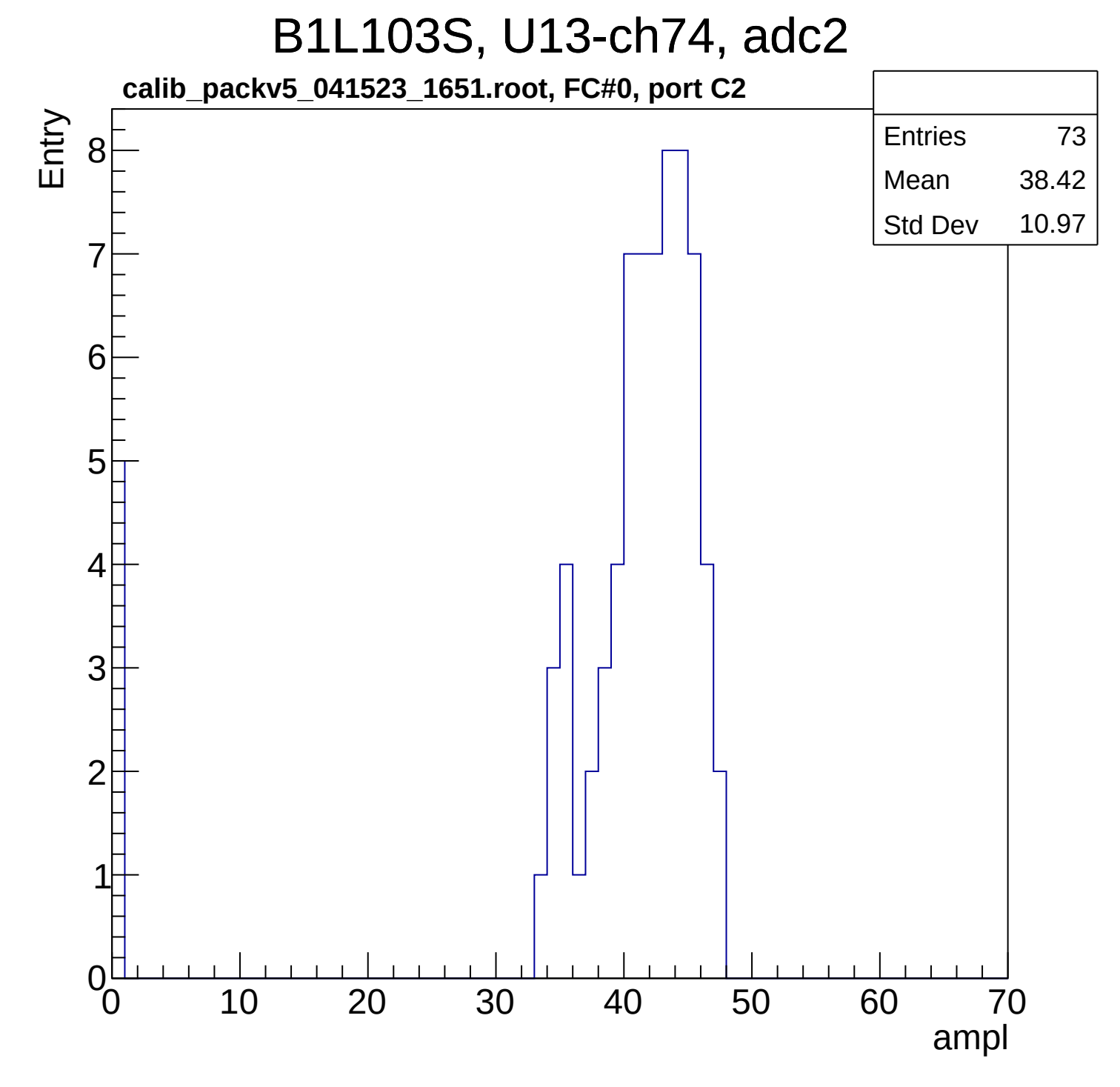
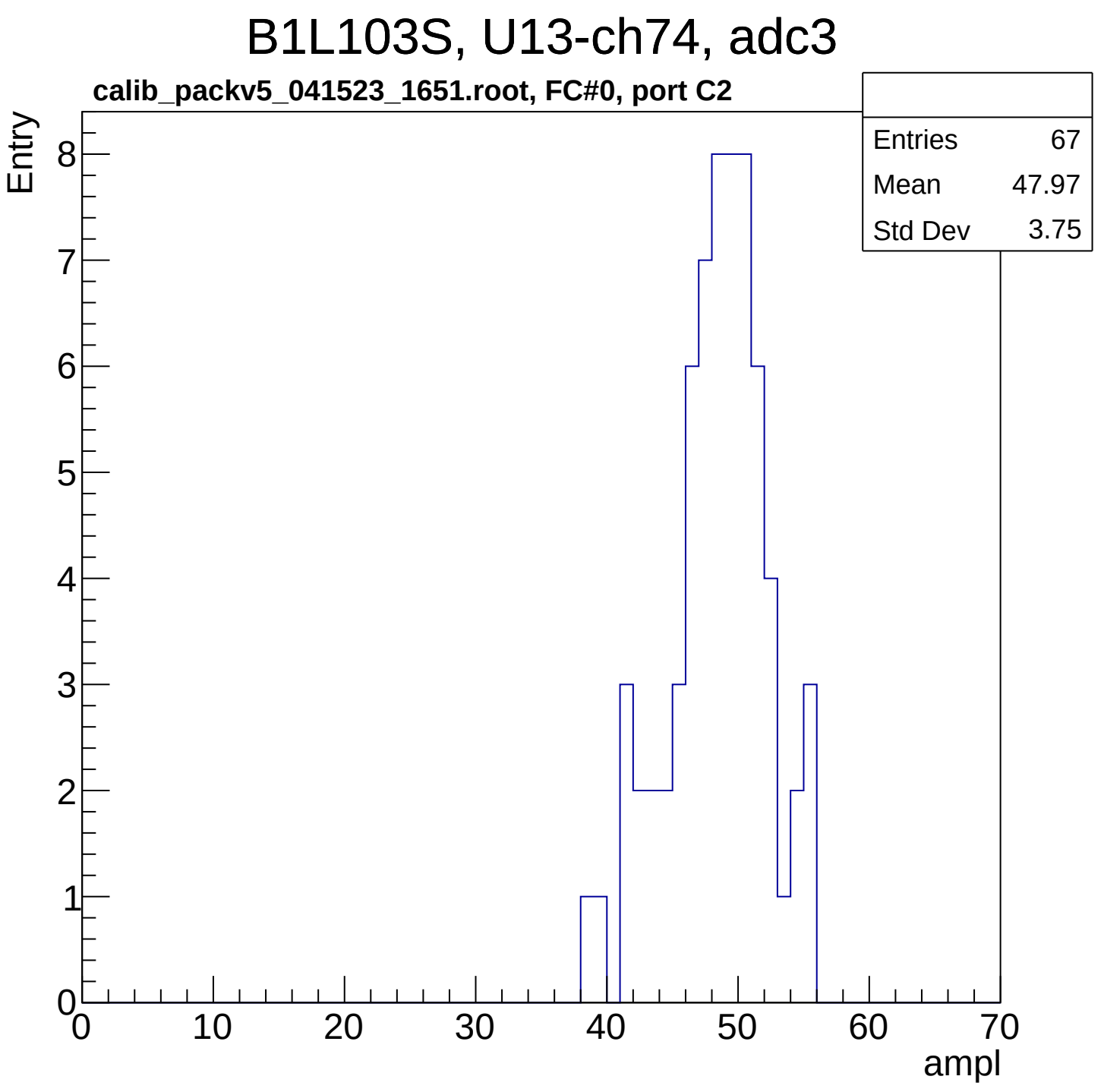

B1L103S, U13-ch73, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

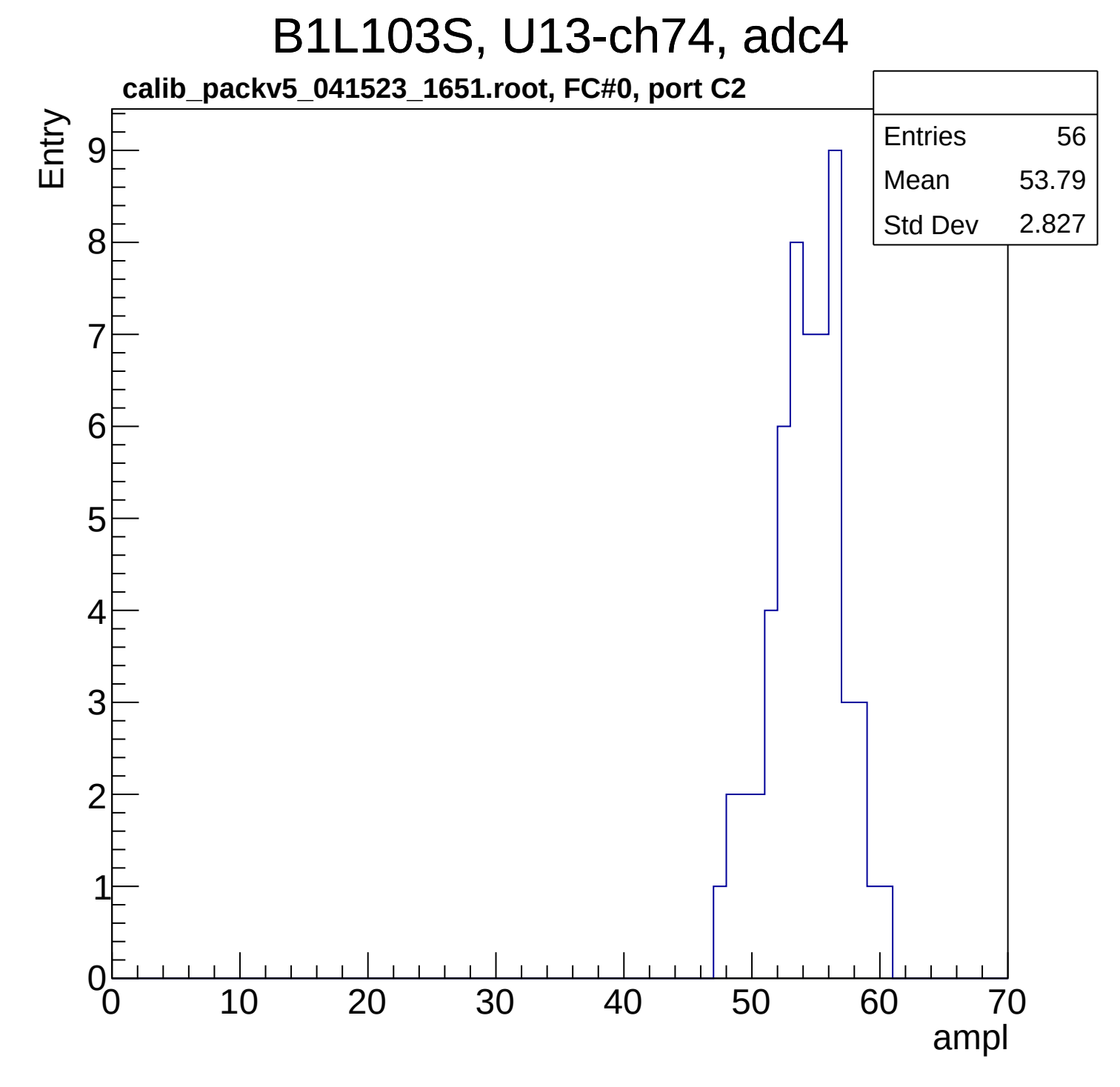

B1L103S, U13-ch73, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

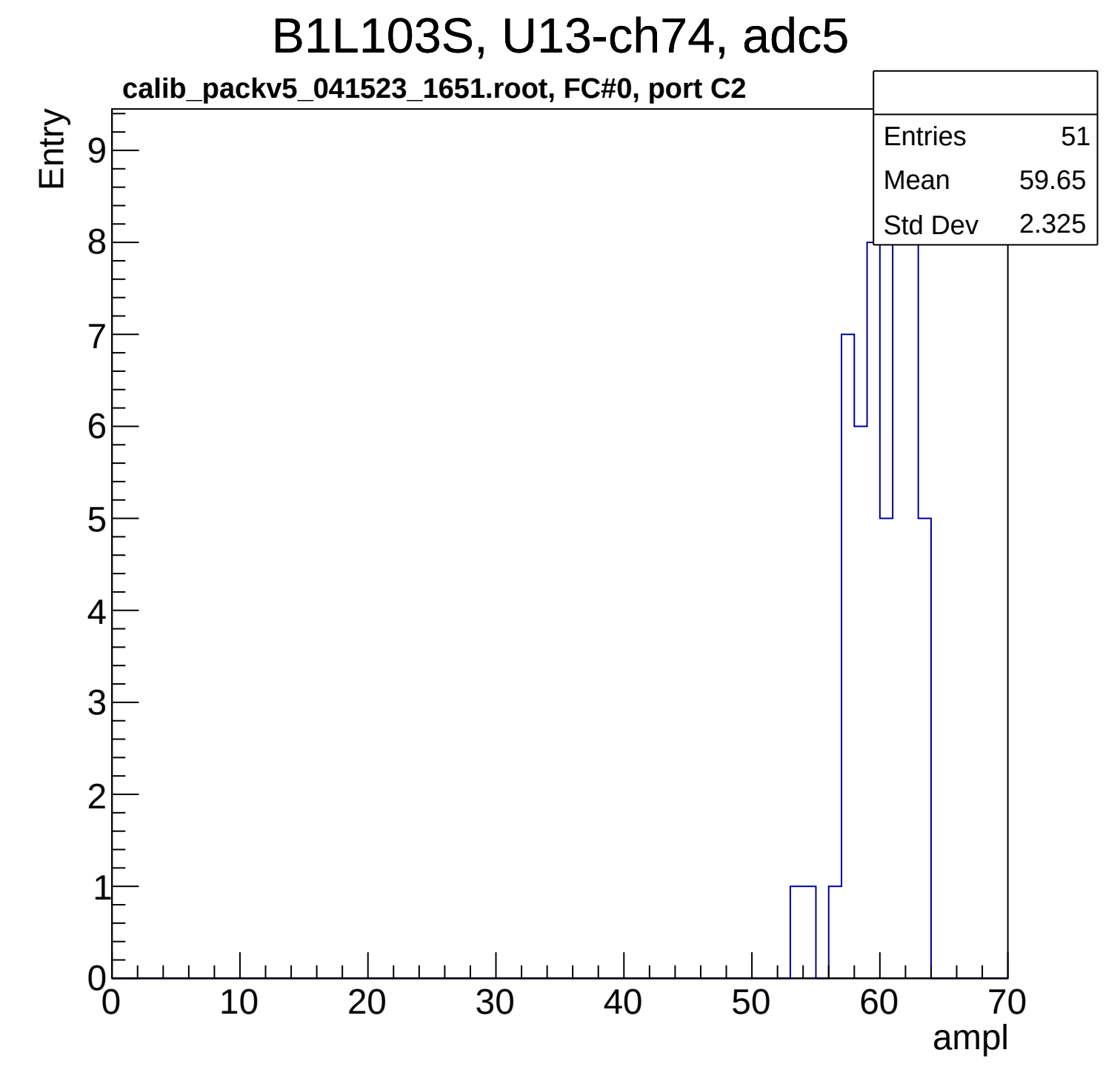

B1L103S, U13-ch74, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 23.76
Std Dev 11.15
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

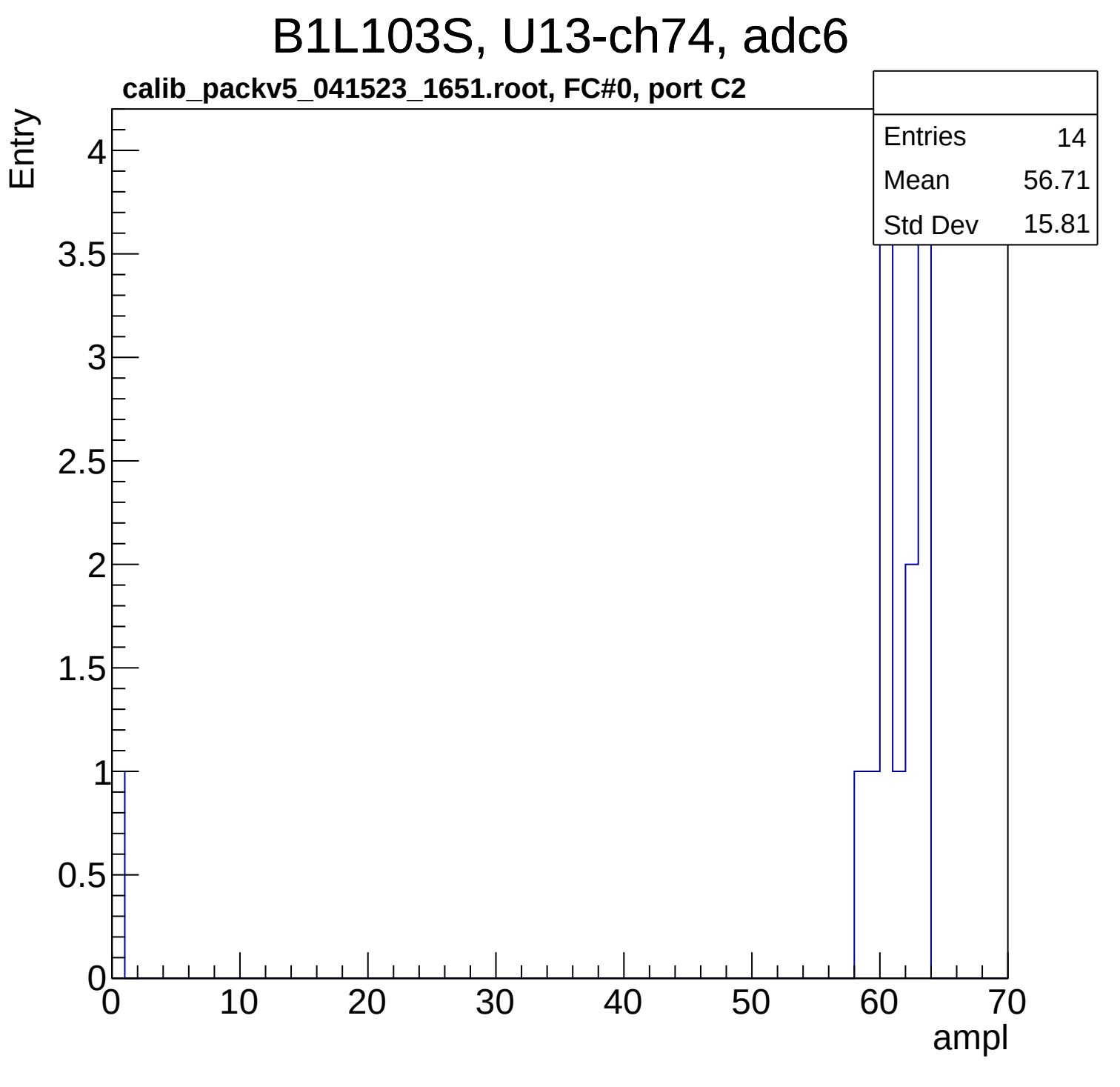

B1L103S, U13-ch74, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 28.7
Std Dev 14.02
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

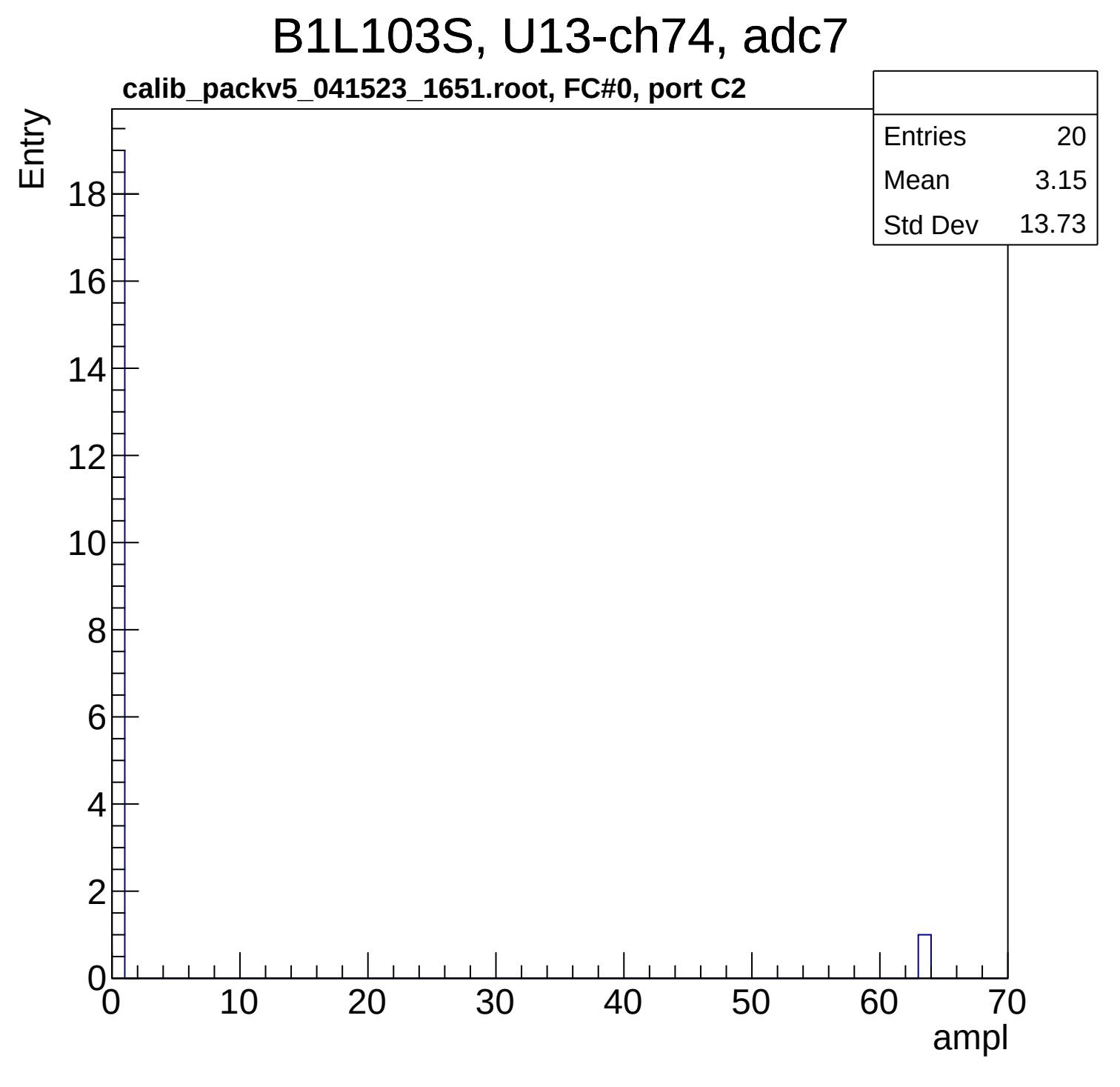

B1L103S, U13-ch74, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 38.42
Std Dev 10.97
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

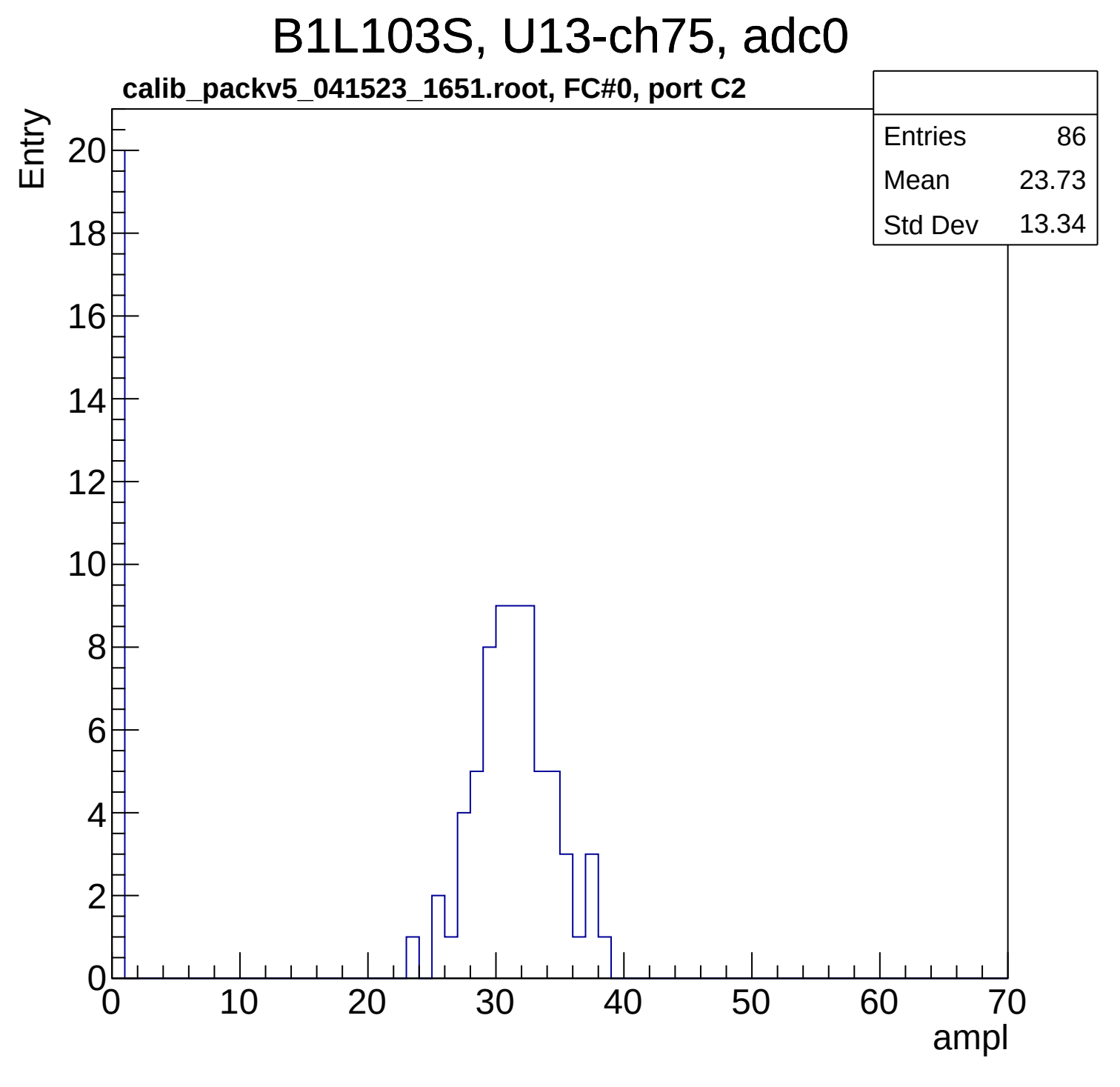

B1L103S, U13-ch74, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 47.97
Std Dev 3.75
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

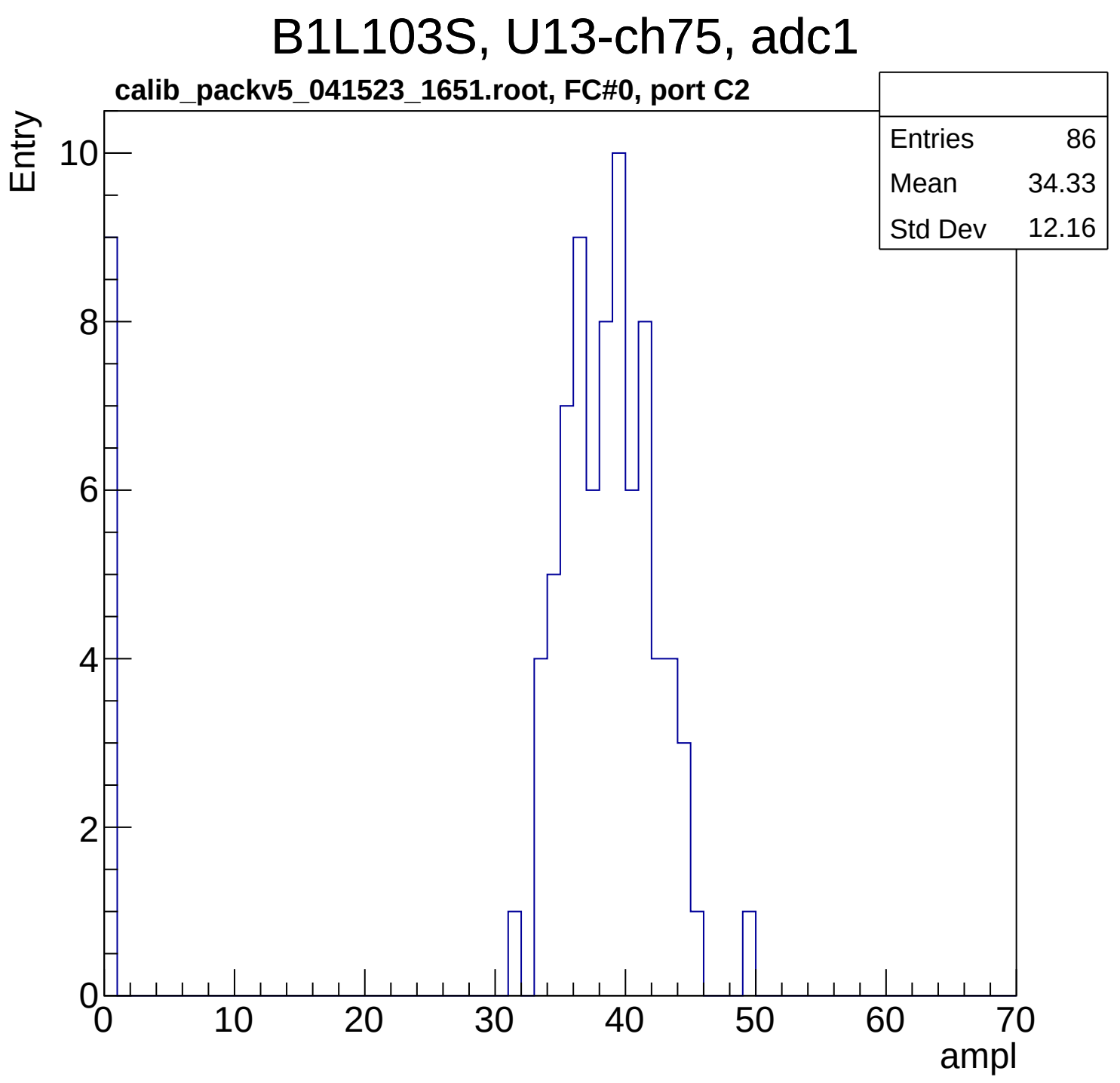

B1L103S, U13-ch74, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 53.79
Std Dev 2.827
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

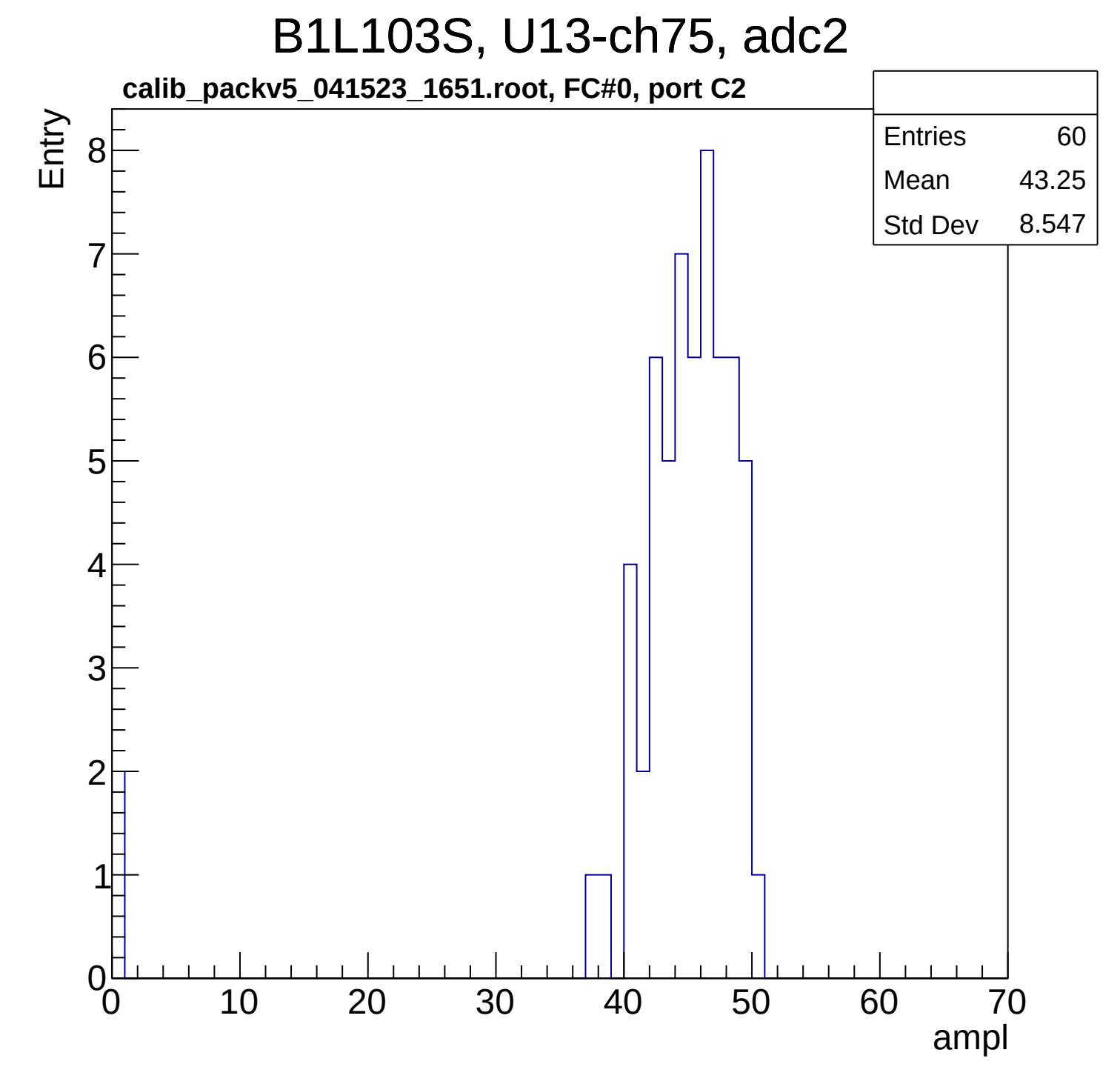

B1L103S, U13-ch74, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 59.65
Std Dev 2.325
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

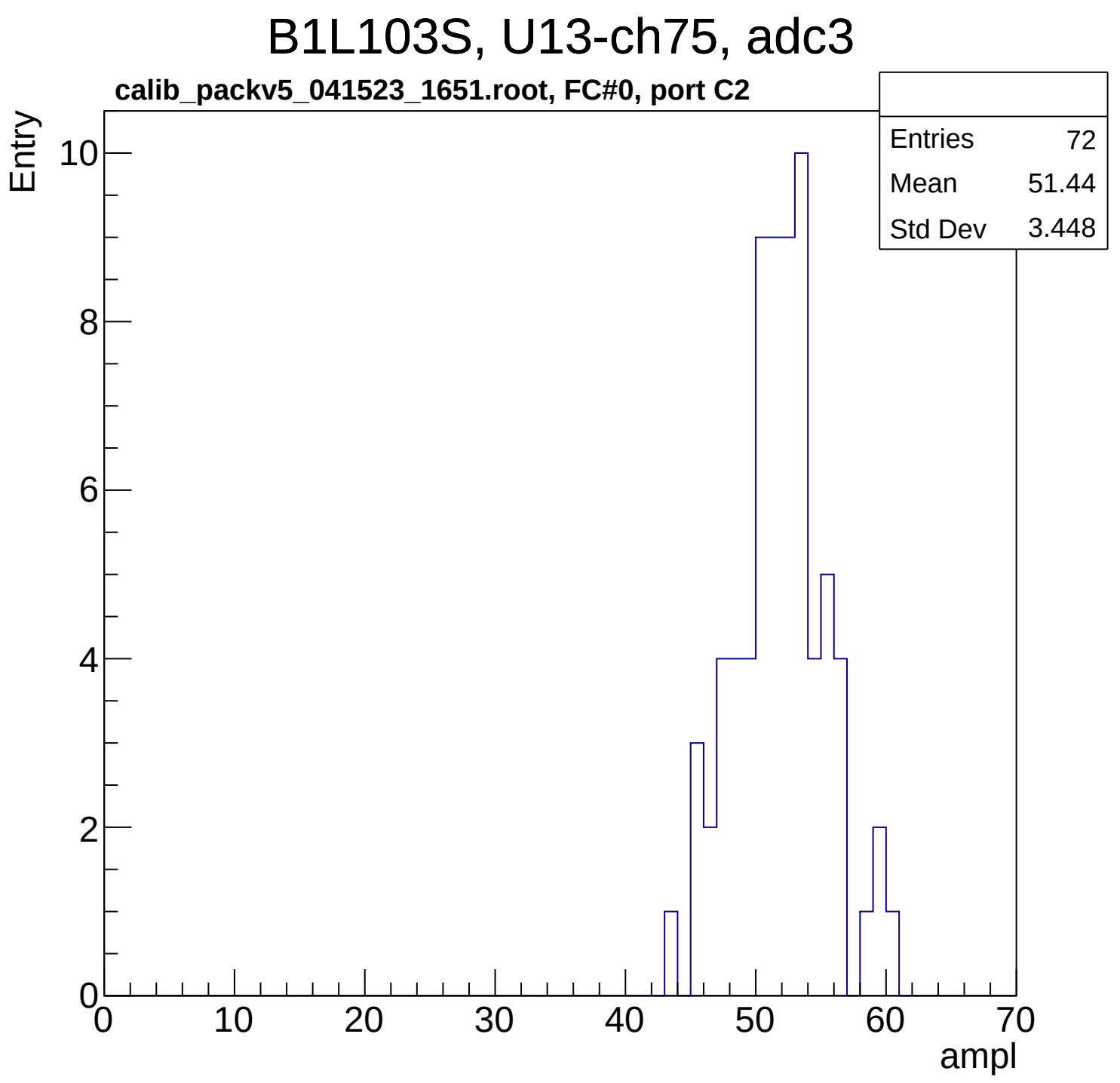

B1L103S, U13-ch74, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 56.71
Std Dev 15.81
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

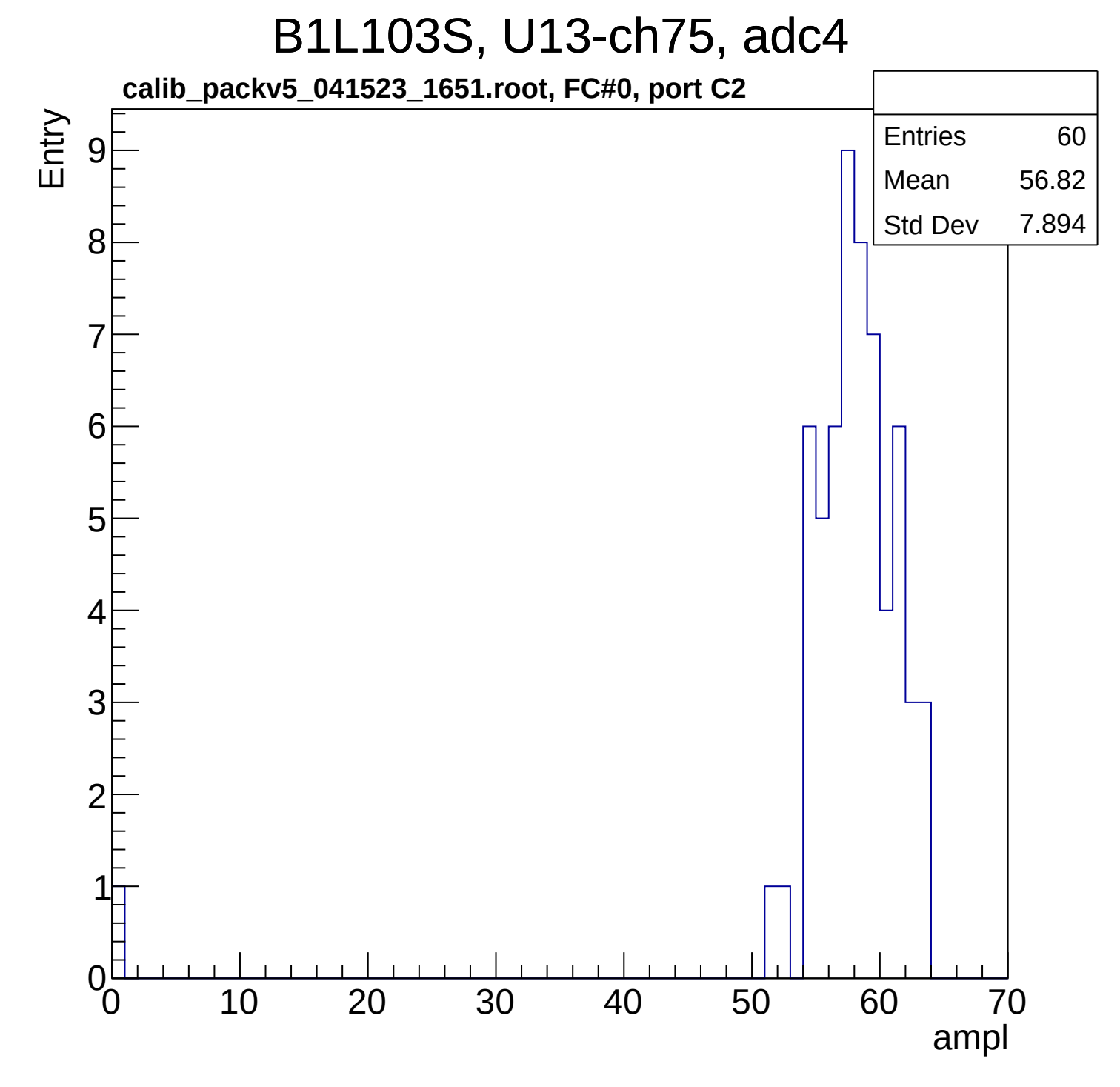

B1L103S, U13-ch74, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

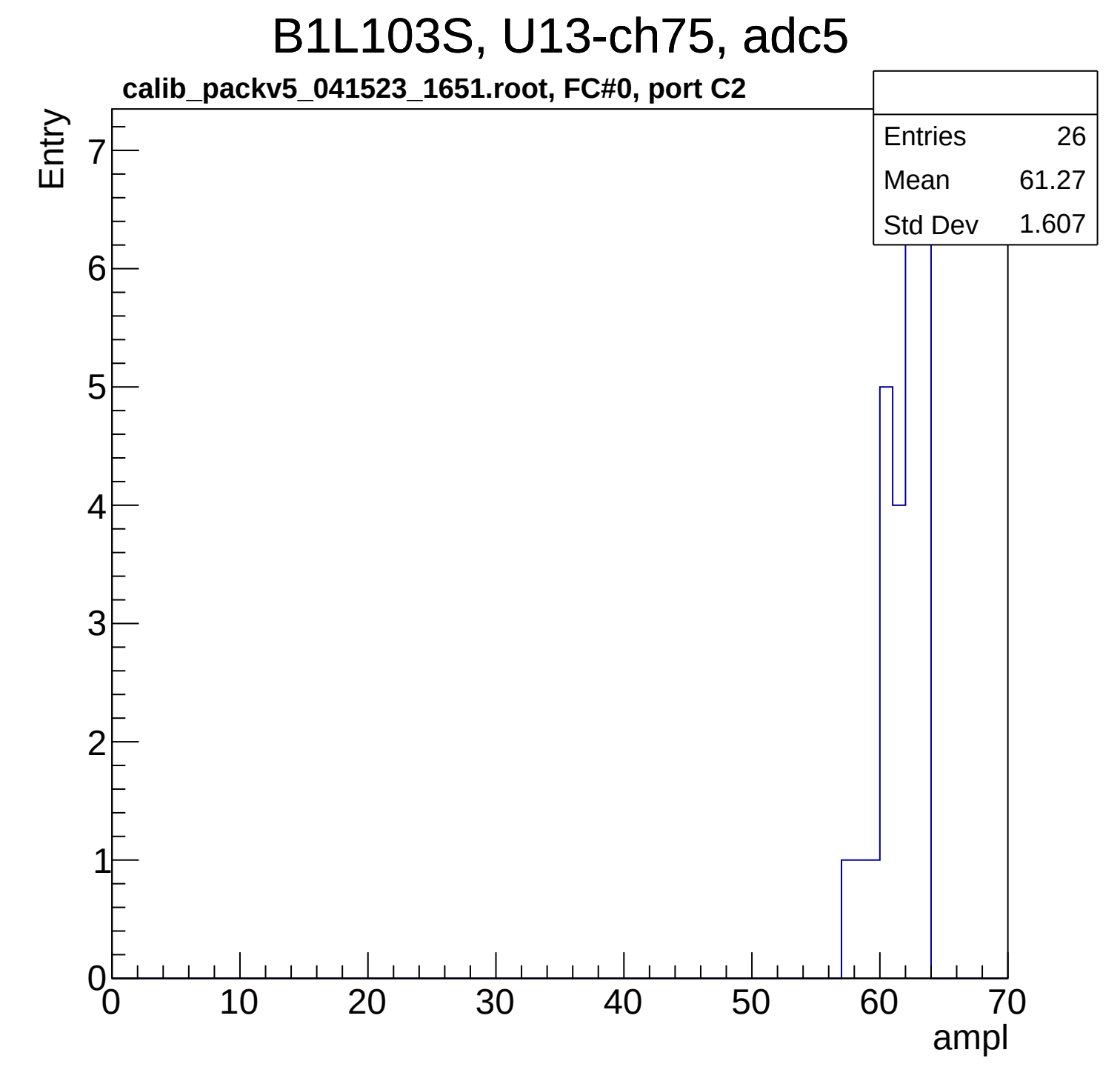

B1L103S, U13-ch75, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 23.73
Std Dev 13.34
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

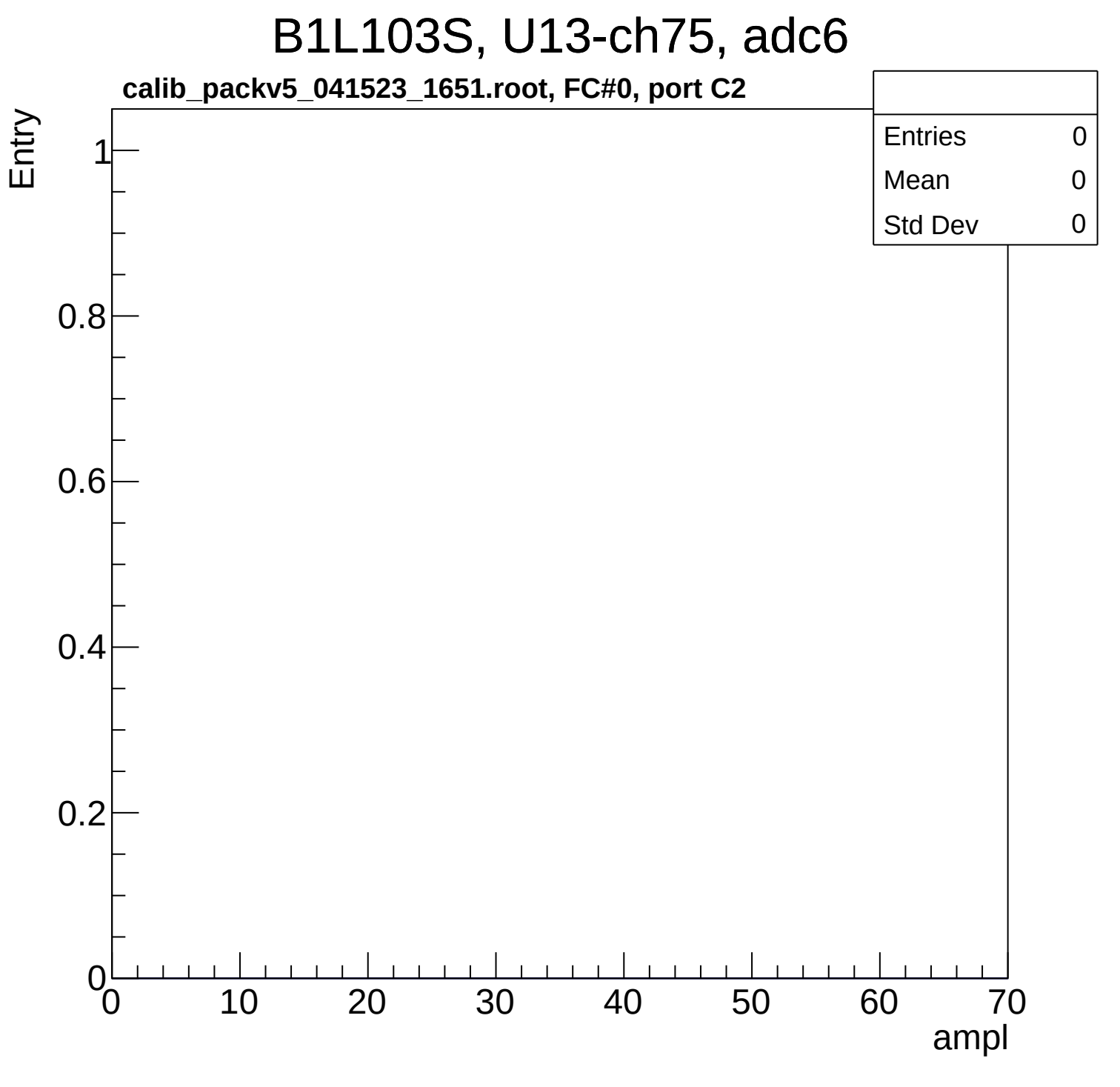

B1L103S, U13-ch75, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 34.33
Std Dev 12.16
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

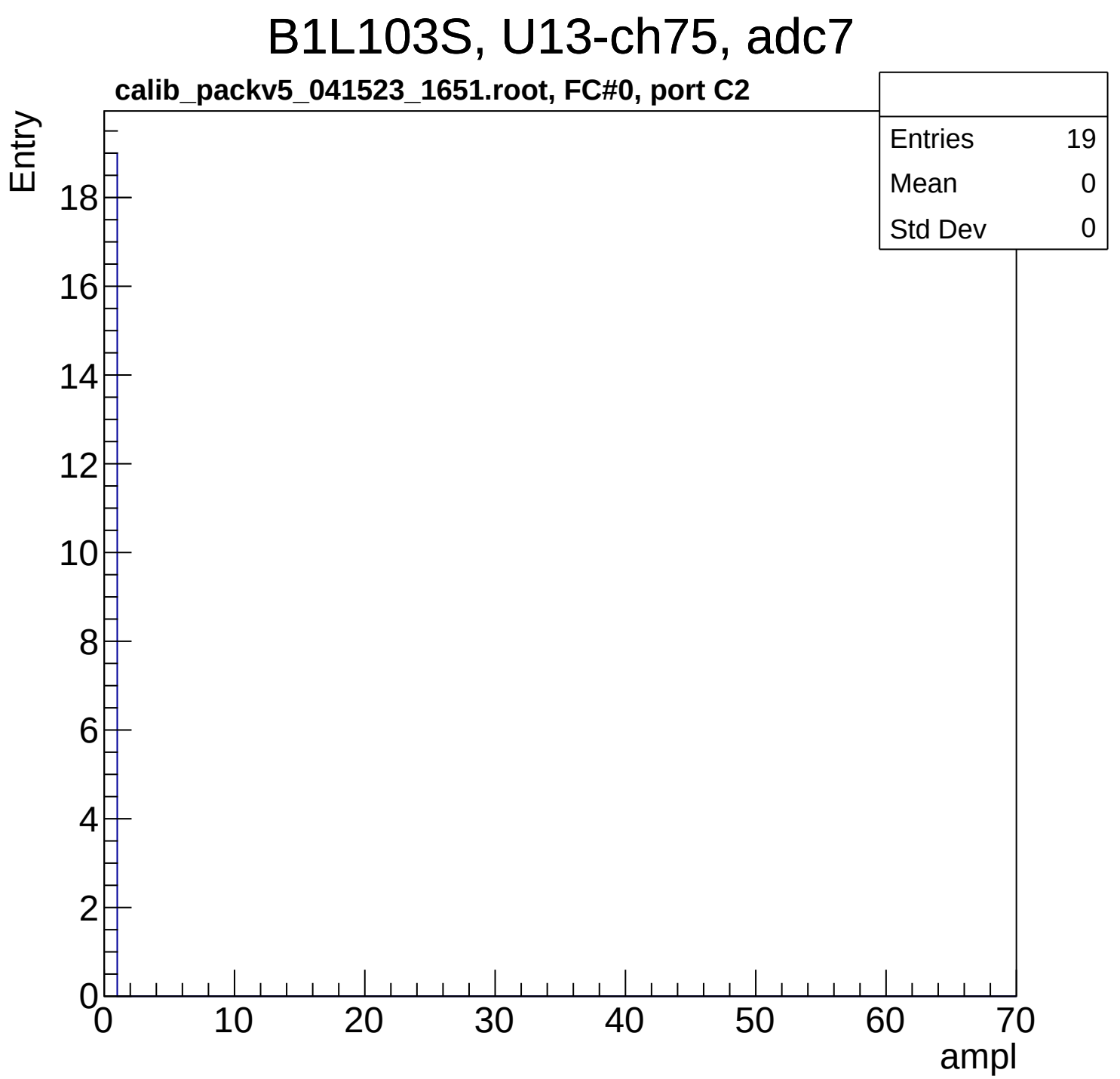

B1L103S, U13-ch75, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 43.25
Std Dev 8.547
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

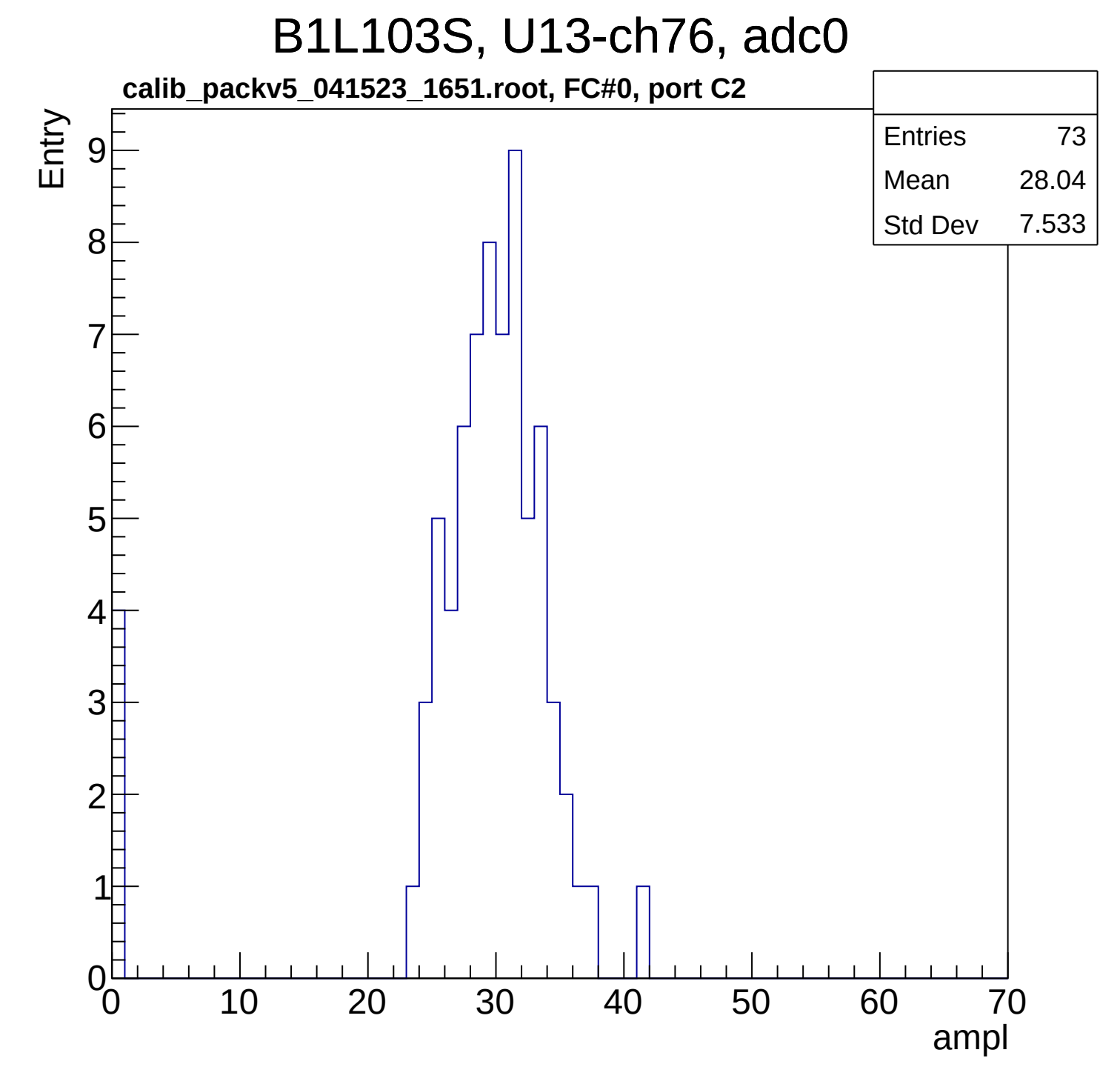

B1L103S, U13-ch75, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 51.44
Std Dev 3.448
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

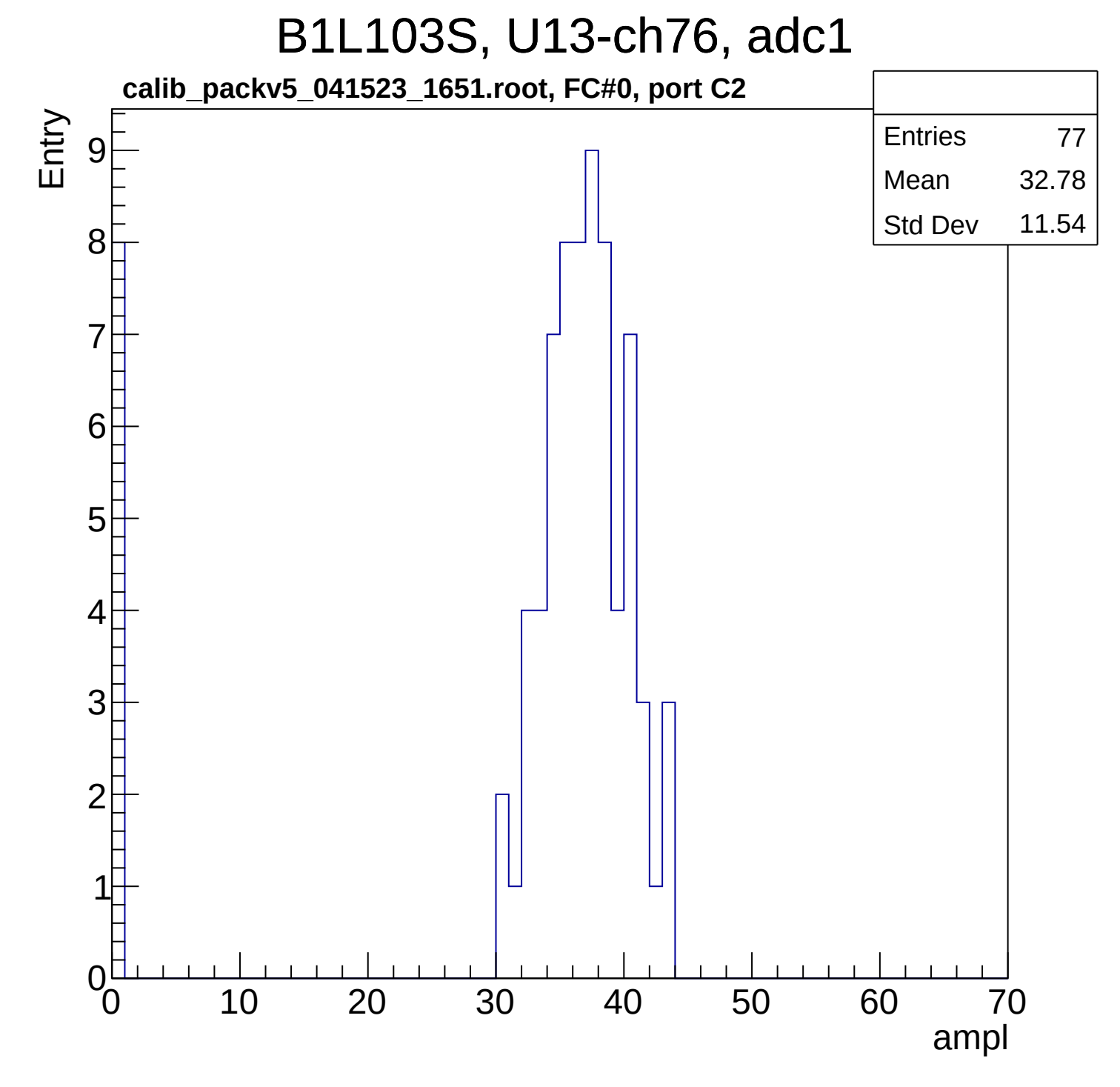

B1L103S, U13-ch75, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 56.82
Std Dev 7.894
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch75, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 61.27
Std Dev 1.607
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch75, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch75, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch76, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 28.04
Std Dev 7.533
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch76, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 32.78
Std Dev 11.54
Entry
ampl
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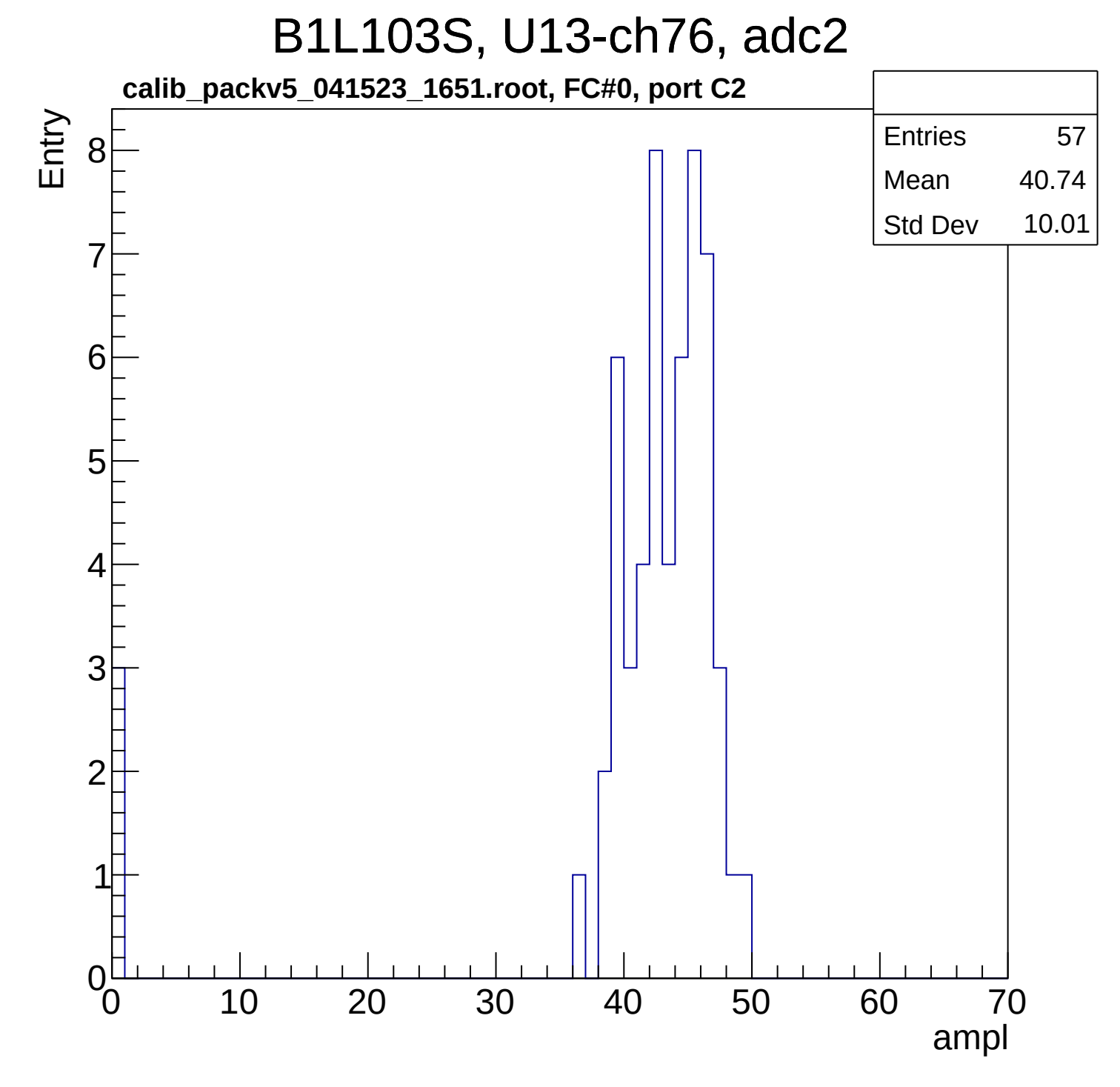
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch76, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 40.74
Std Dev 10.01
Entry
ampl
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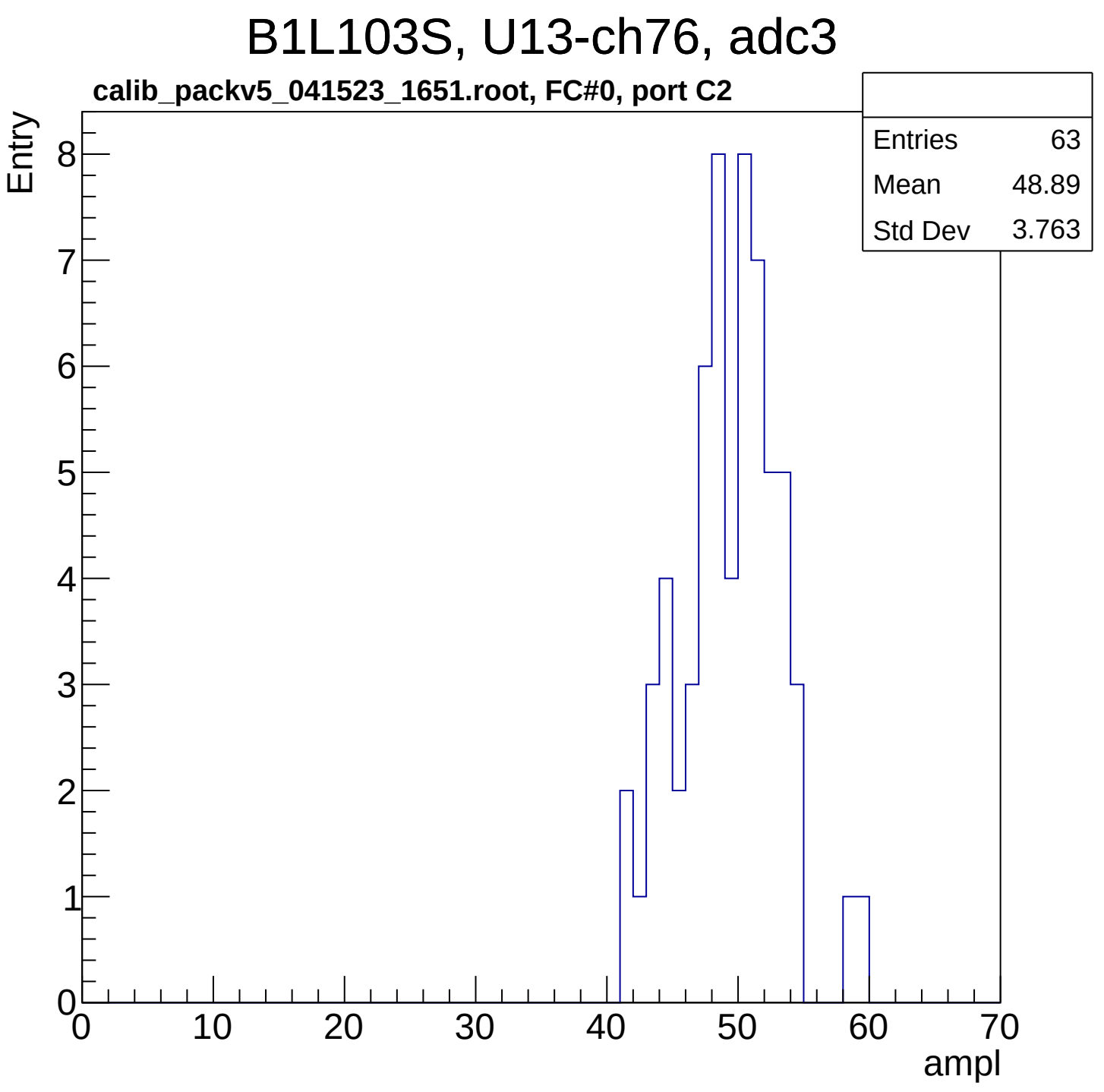
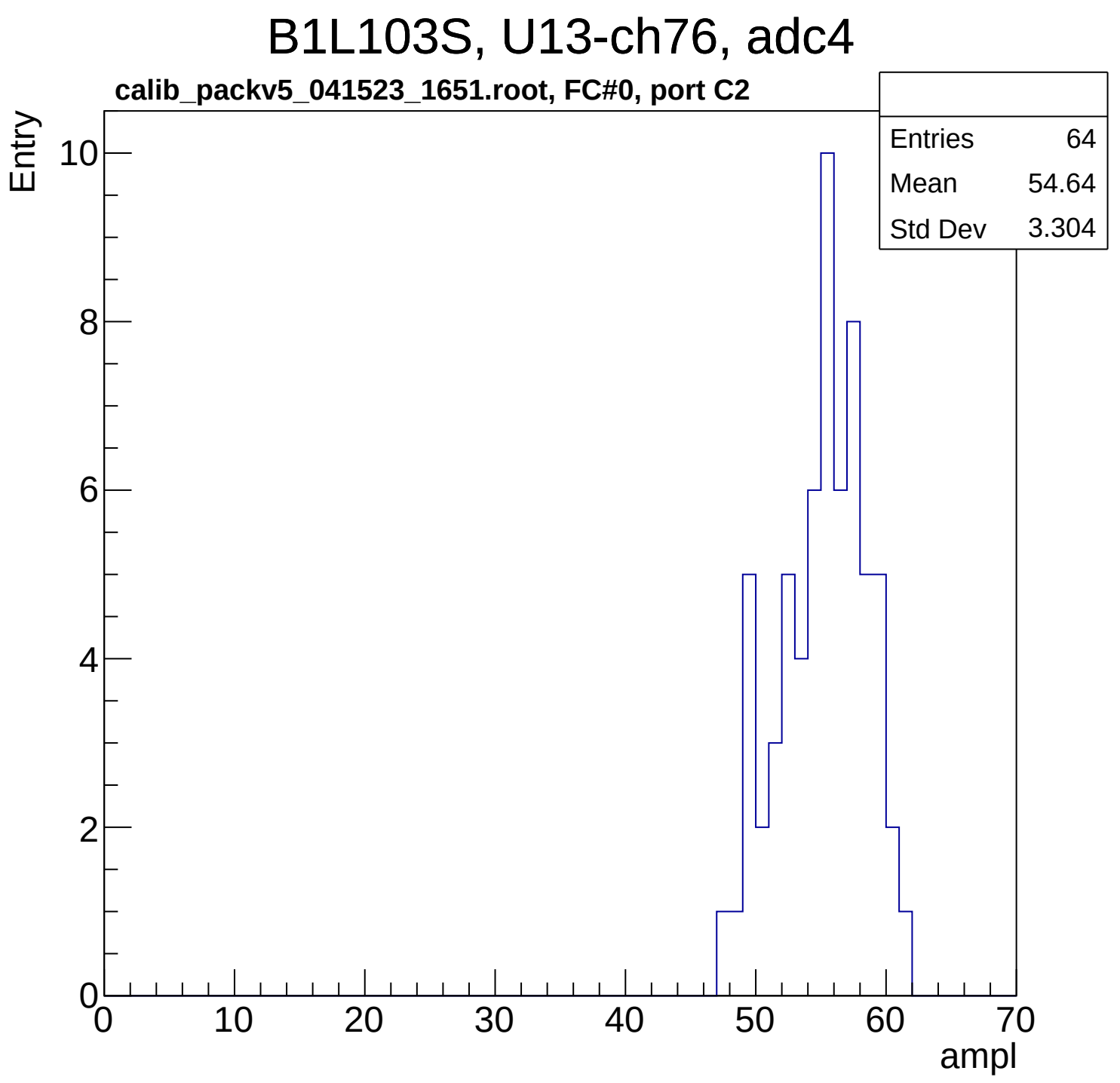
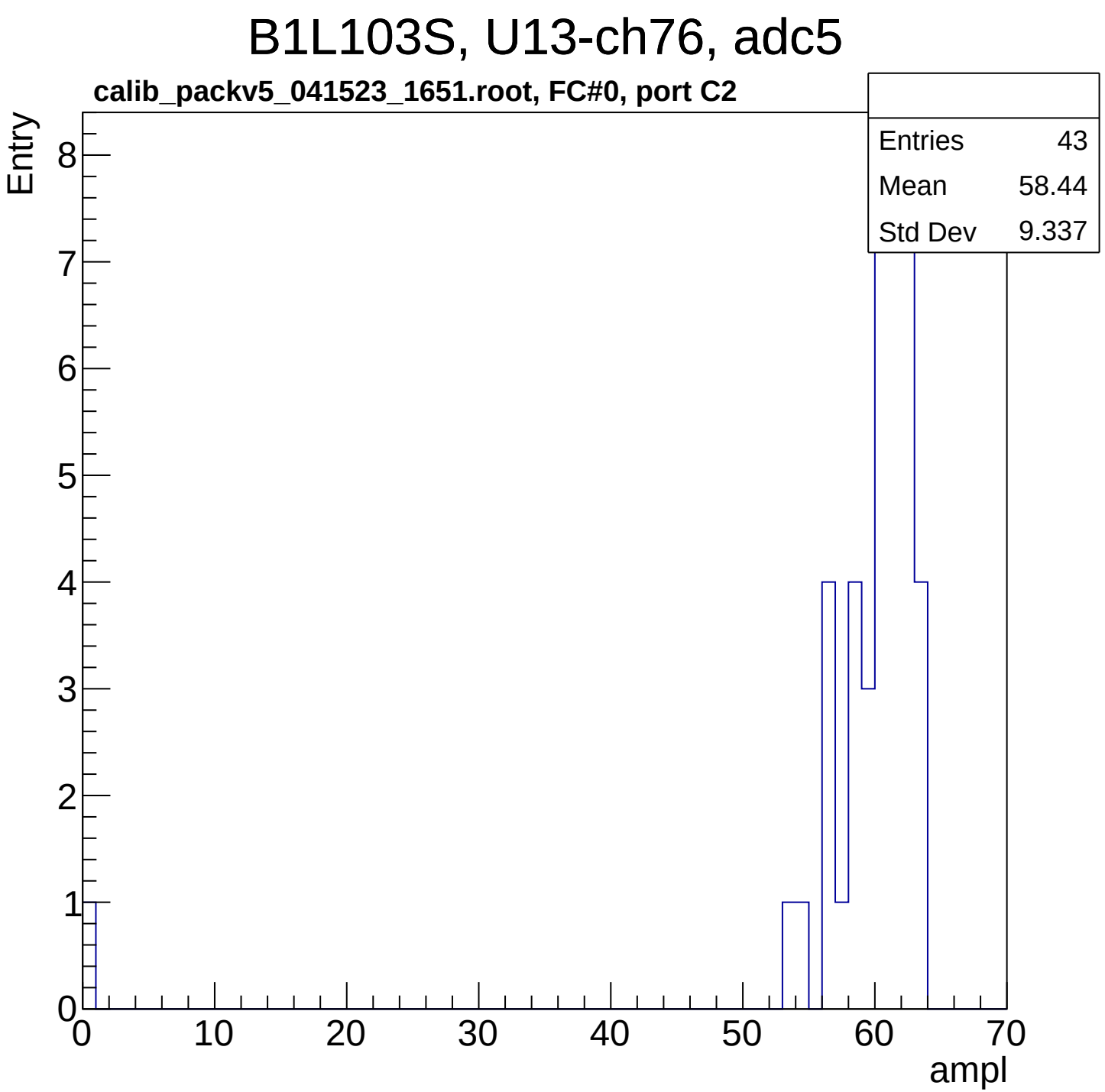
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch76, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 48.89
Std Dev 3.763
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch76, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 54.64
Std Dev 3.304
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch76, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 58.44
Std Dev 9.337
Entry
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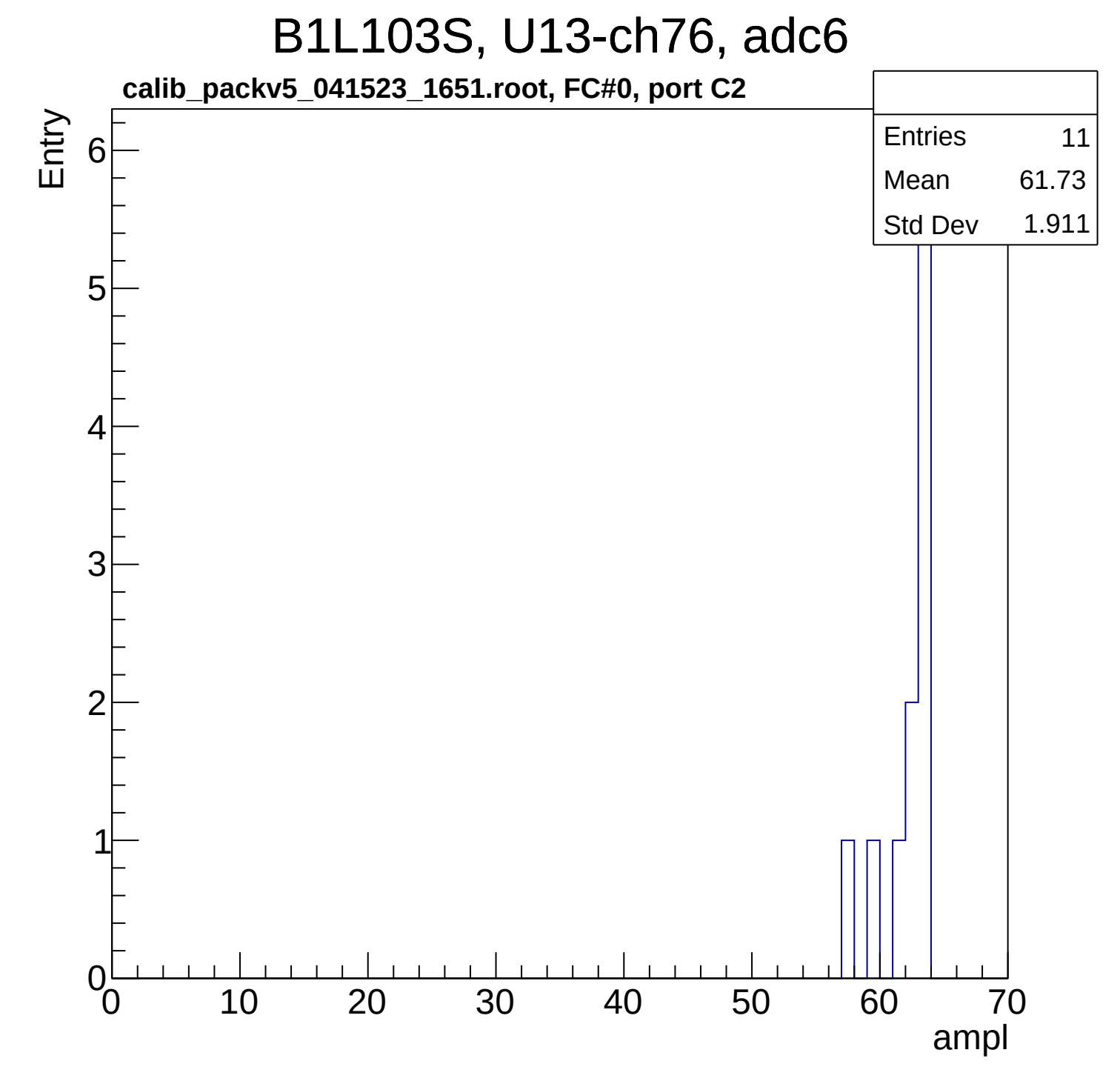
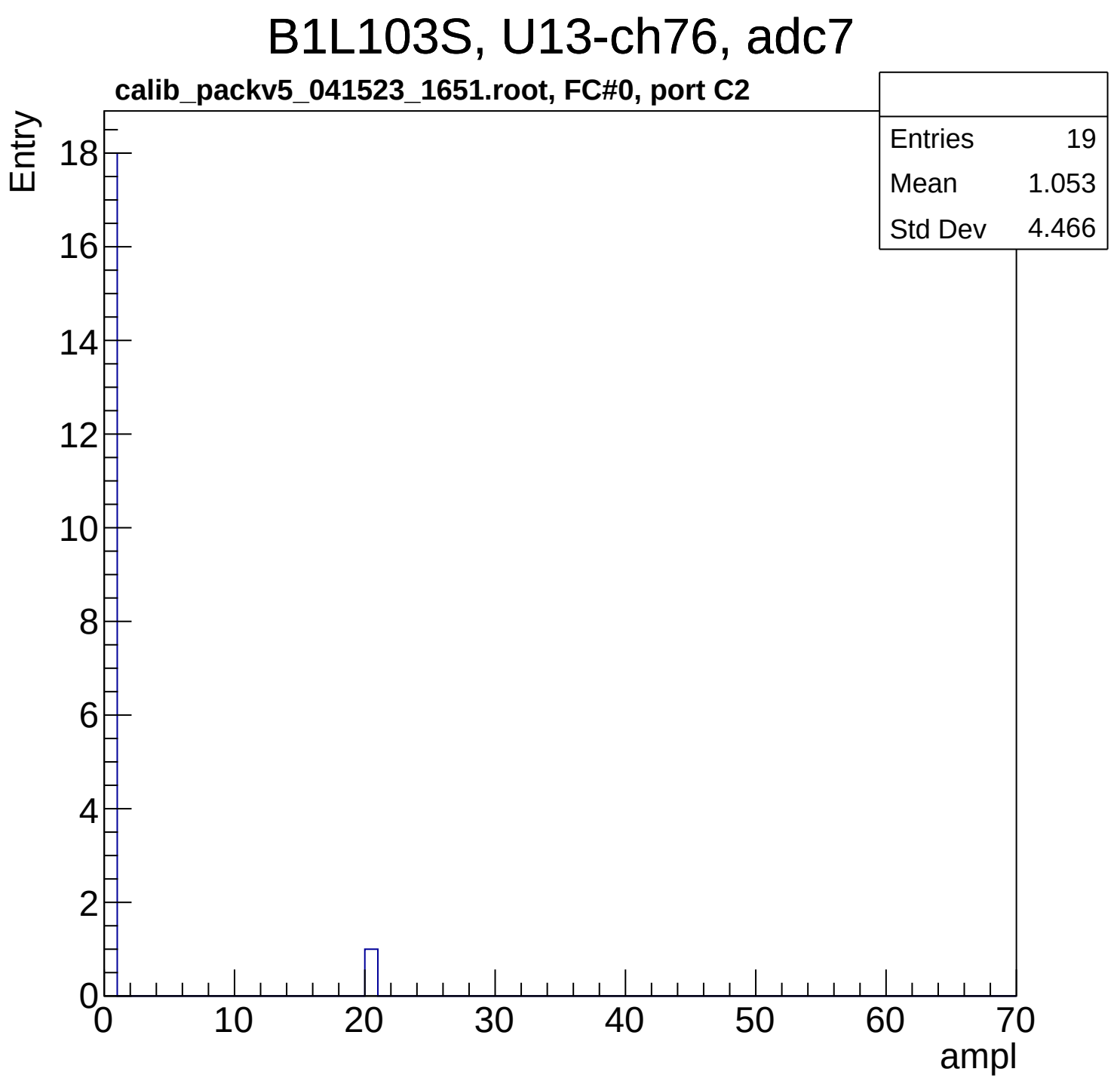
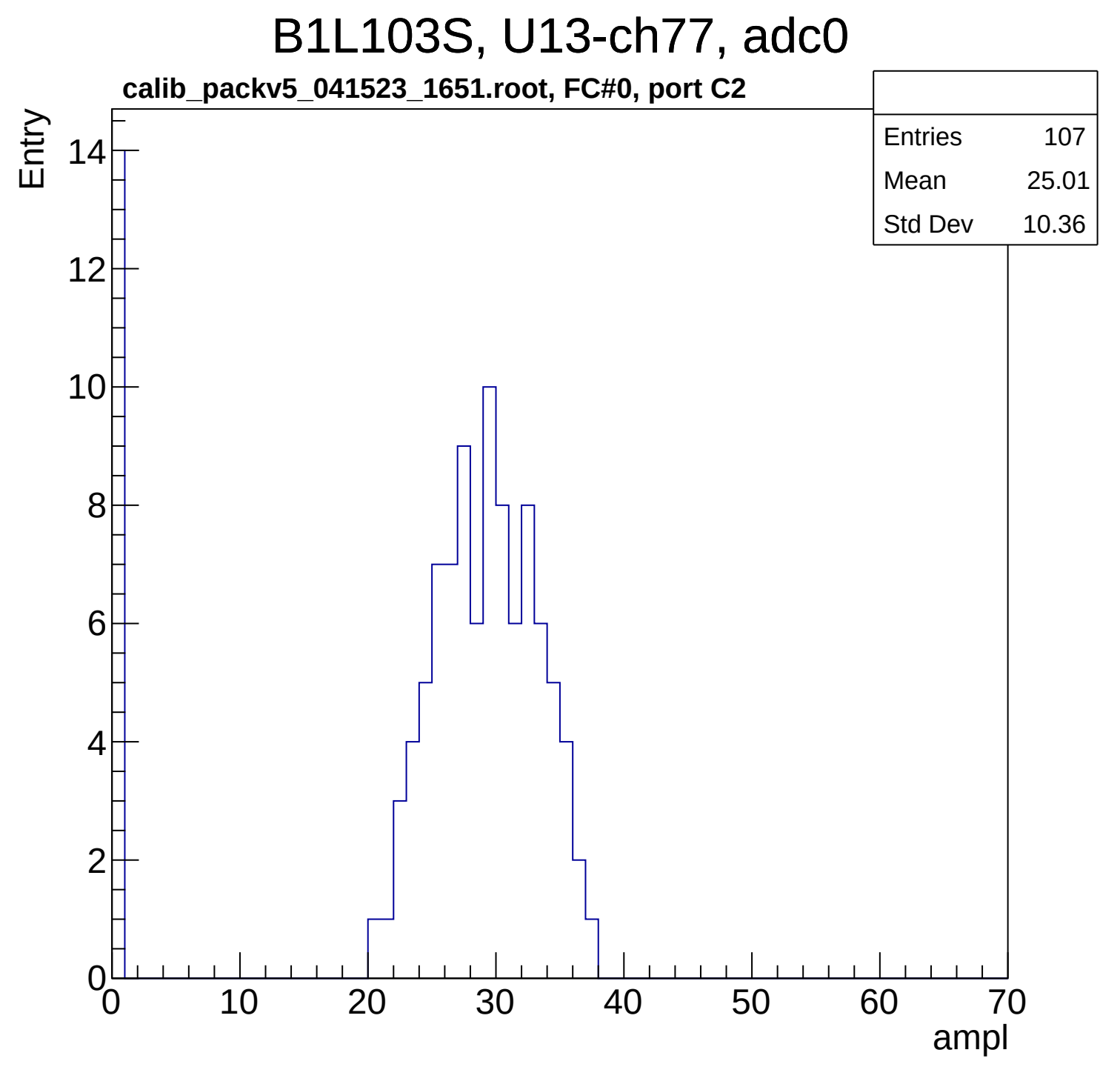
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch76, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.73
Std Dev 1.911
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U13-ch76, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.053
Std Dev 4.466
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch77, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 107
Mean 25.01
Std Dev 10.36
Entry
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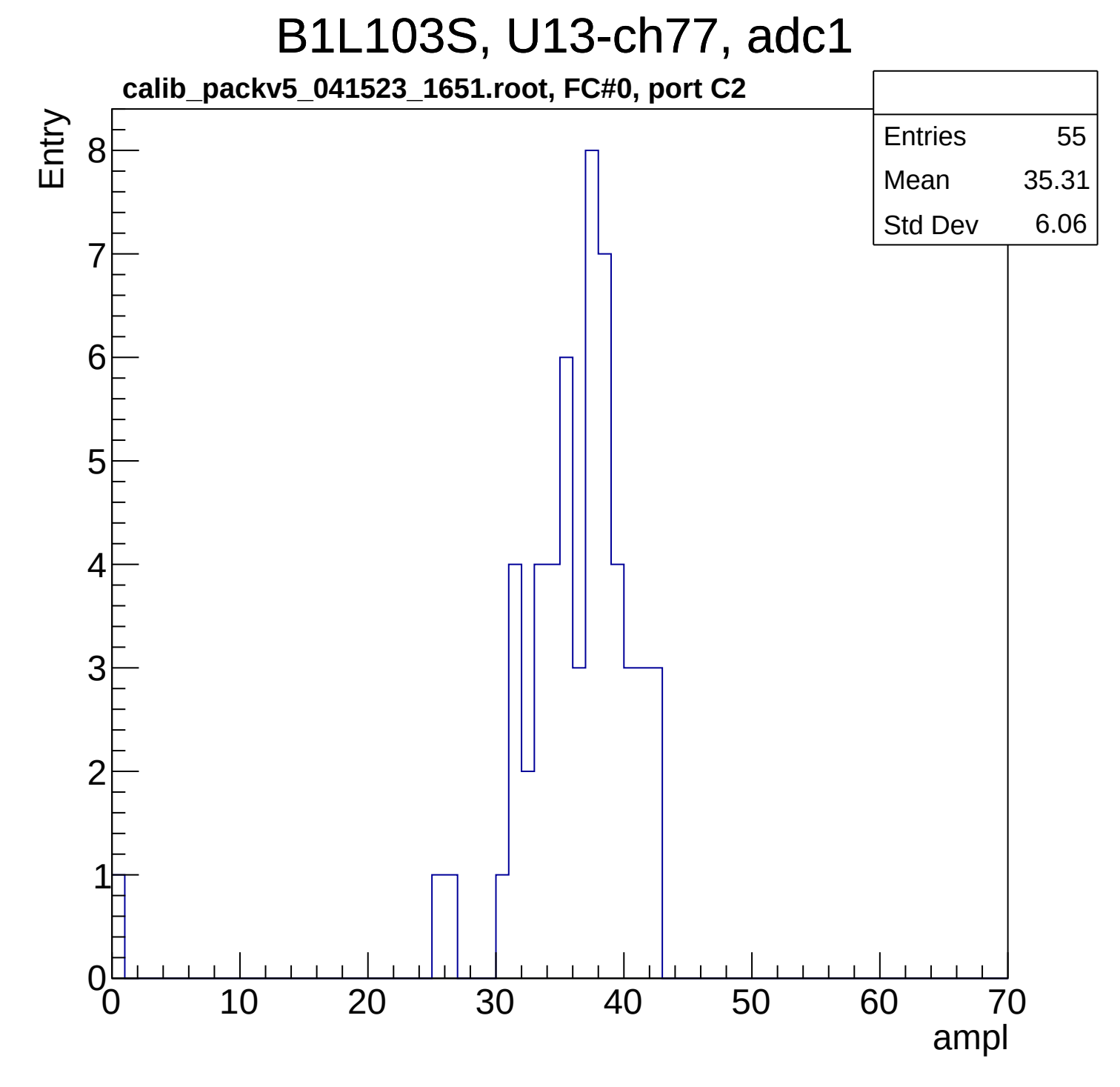
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch77, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 35.31
Std Dev 6.06
Entry
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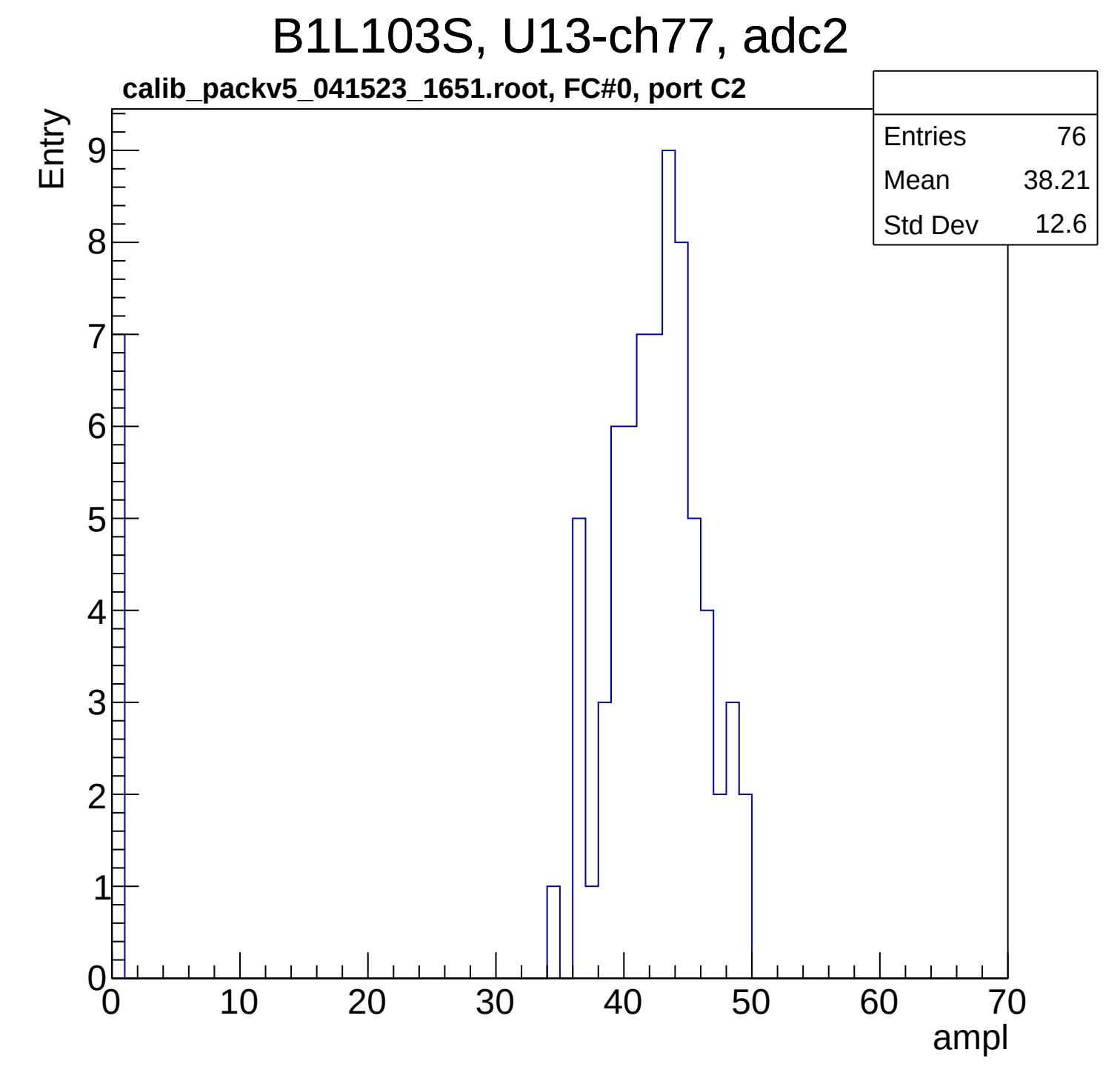
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch77, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 38.21
Std Dev 12.6
Entry
ampl
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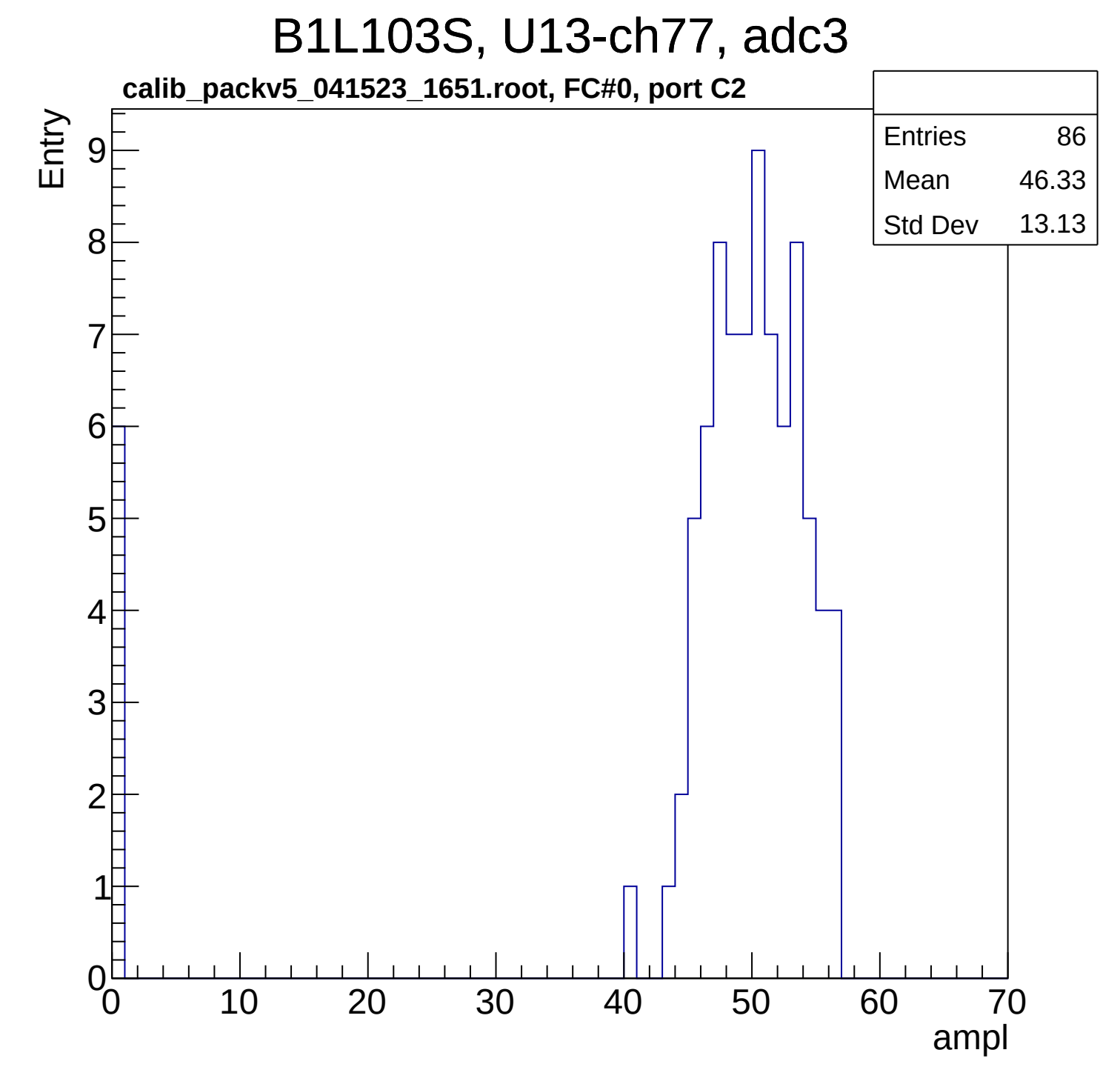
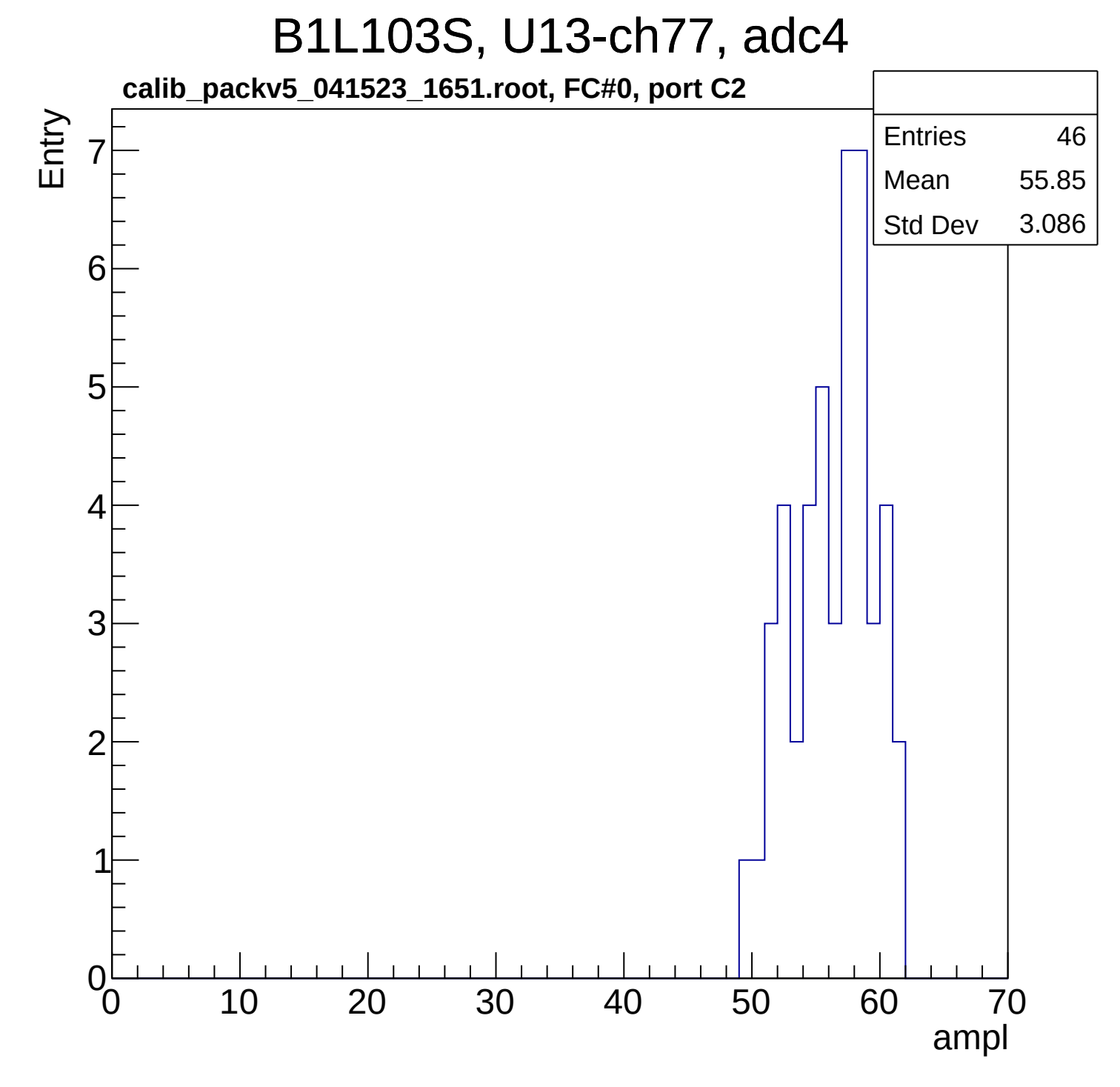
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch77, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 46.33
Std Dev 13.13
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch77, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 55.85
Std Dev 3.086
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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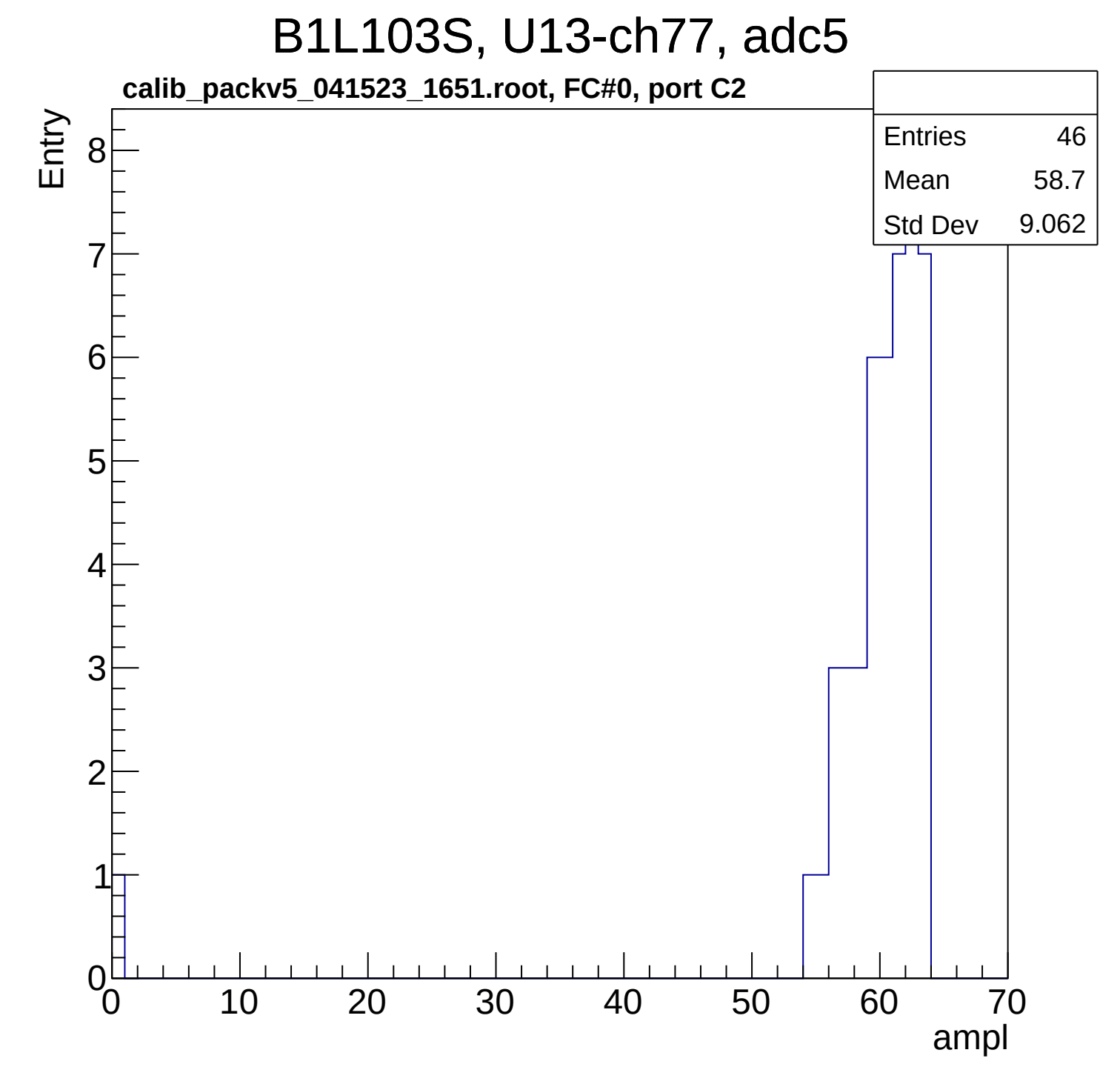
B1L103S, U13-ch77, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.7
Std Dev 9.062
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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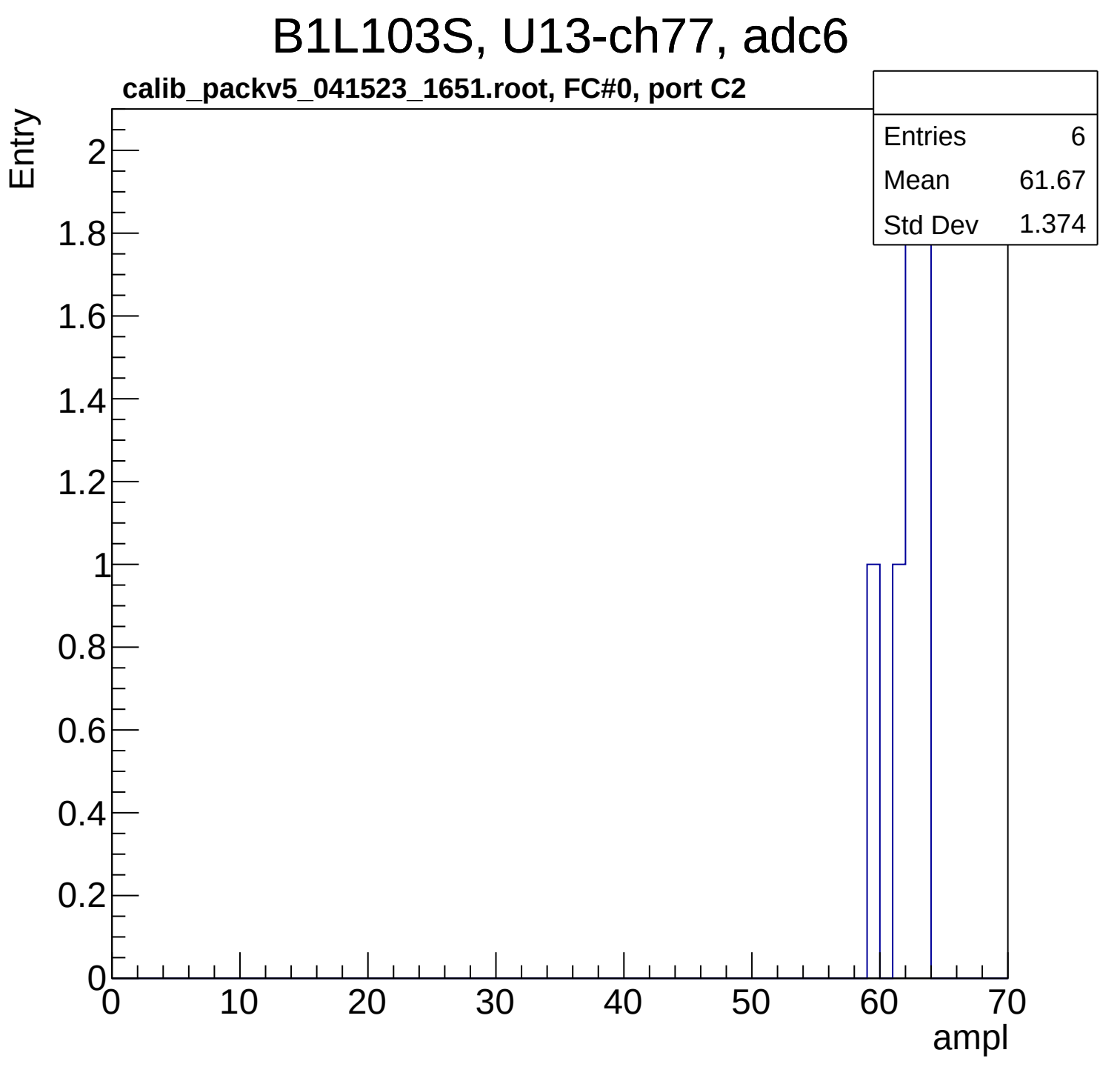
B1L103S, U13-ch77, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.67
Std Dev 1.374
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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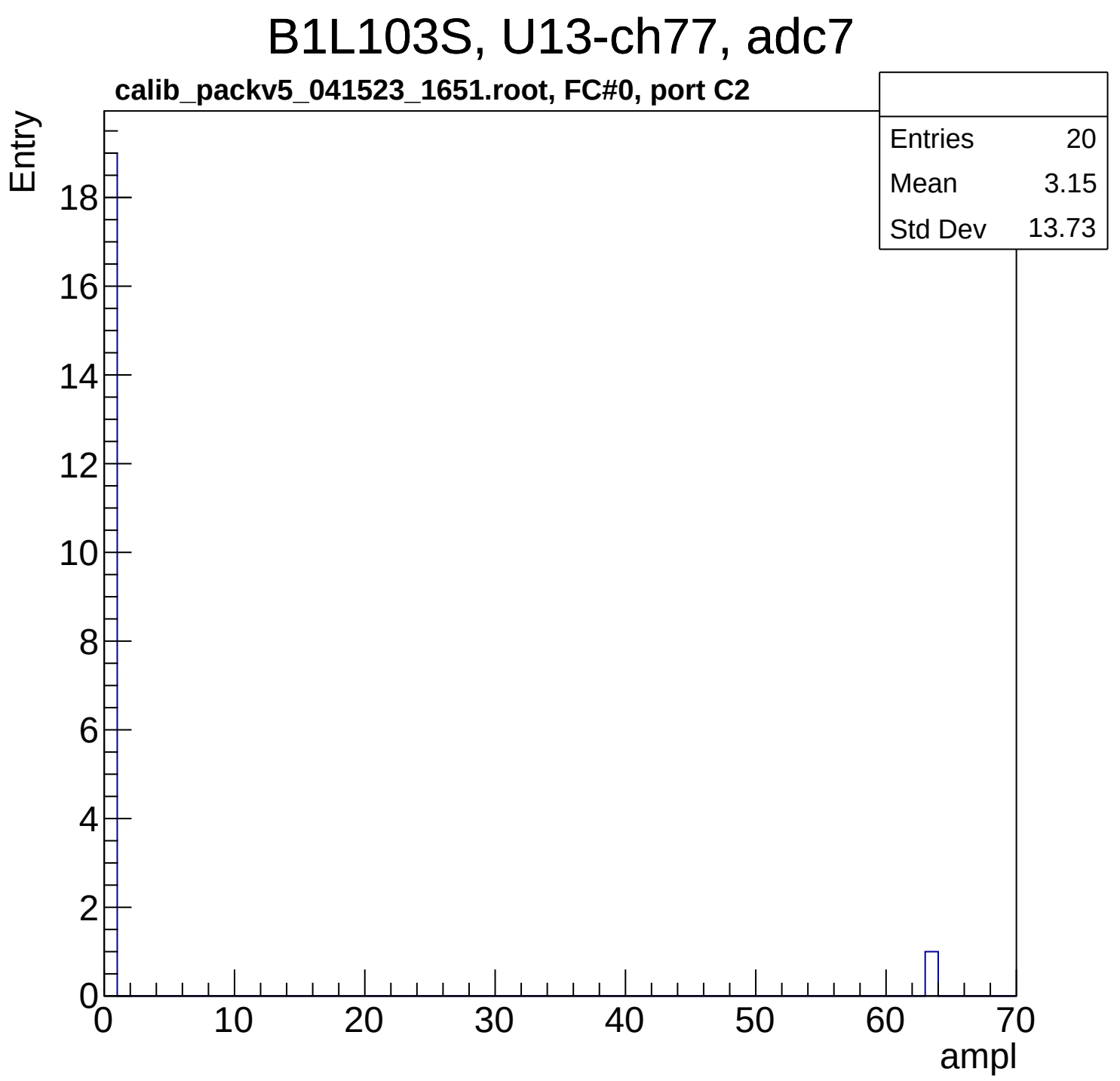
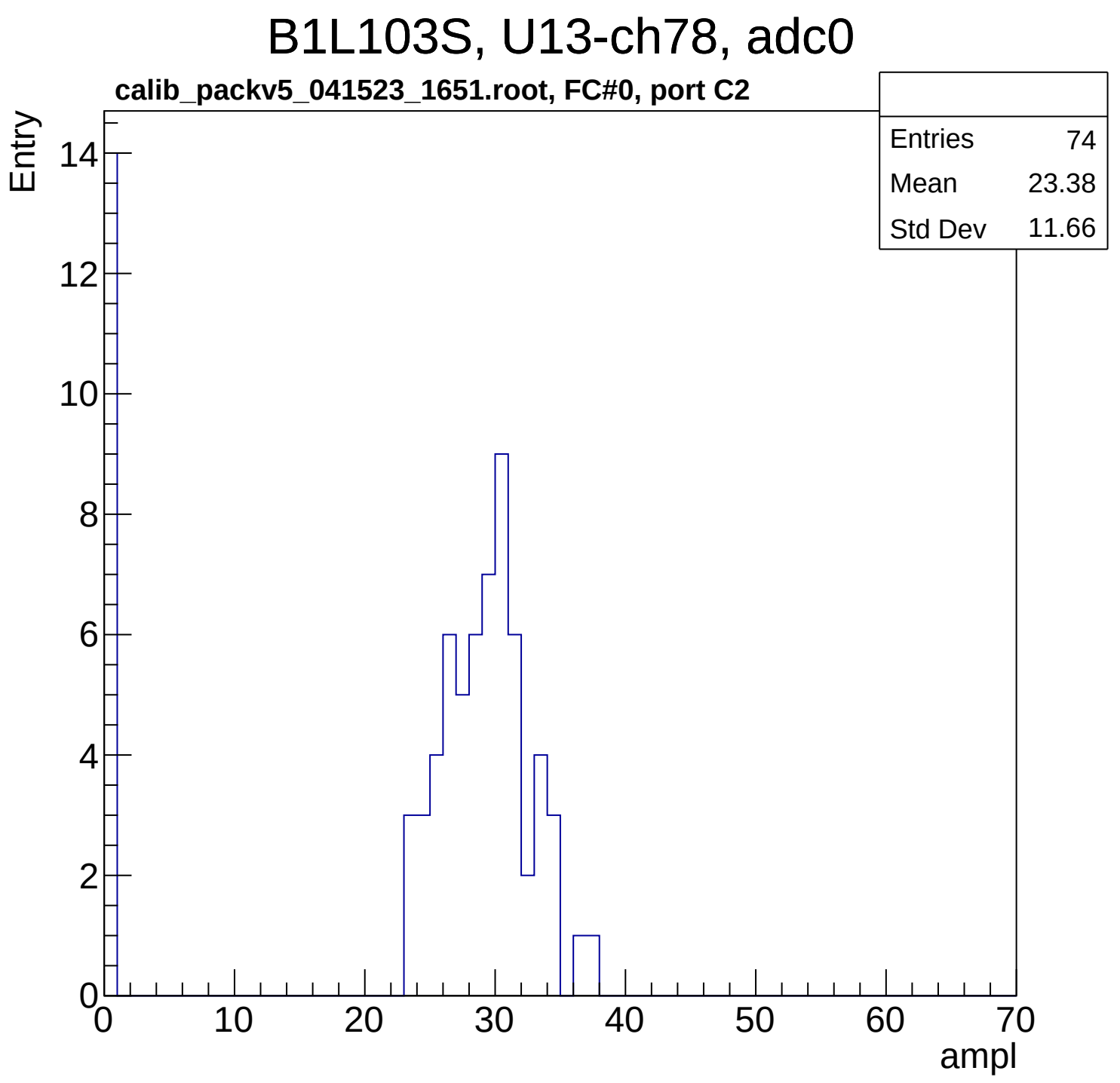
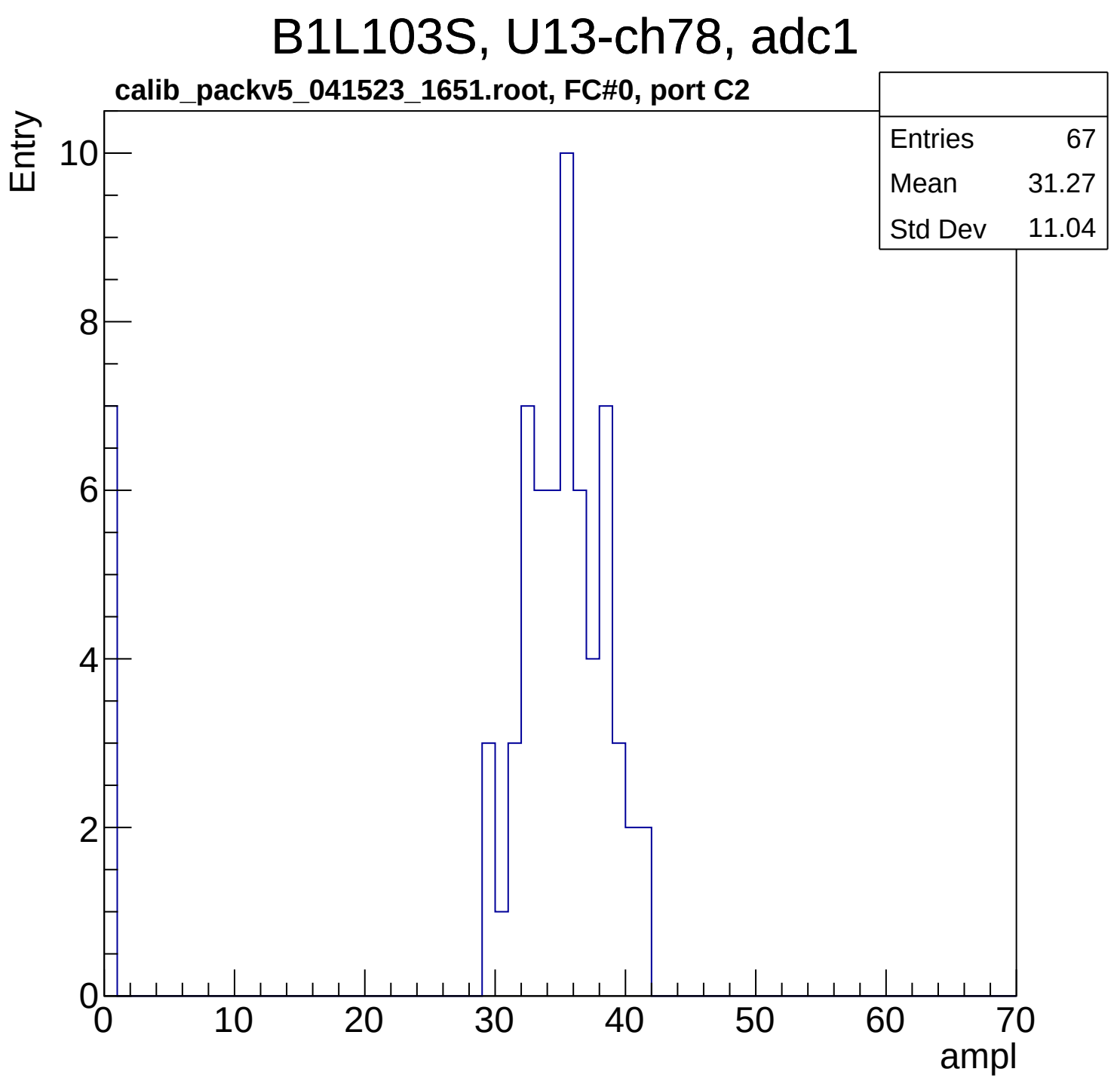
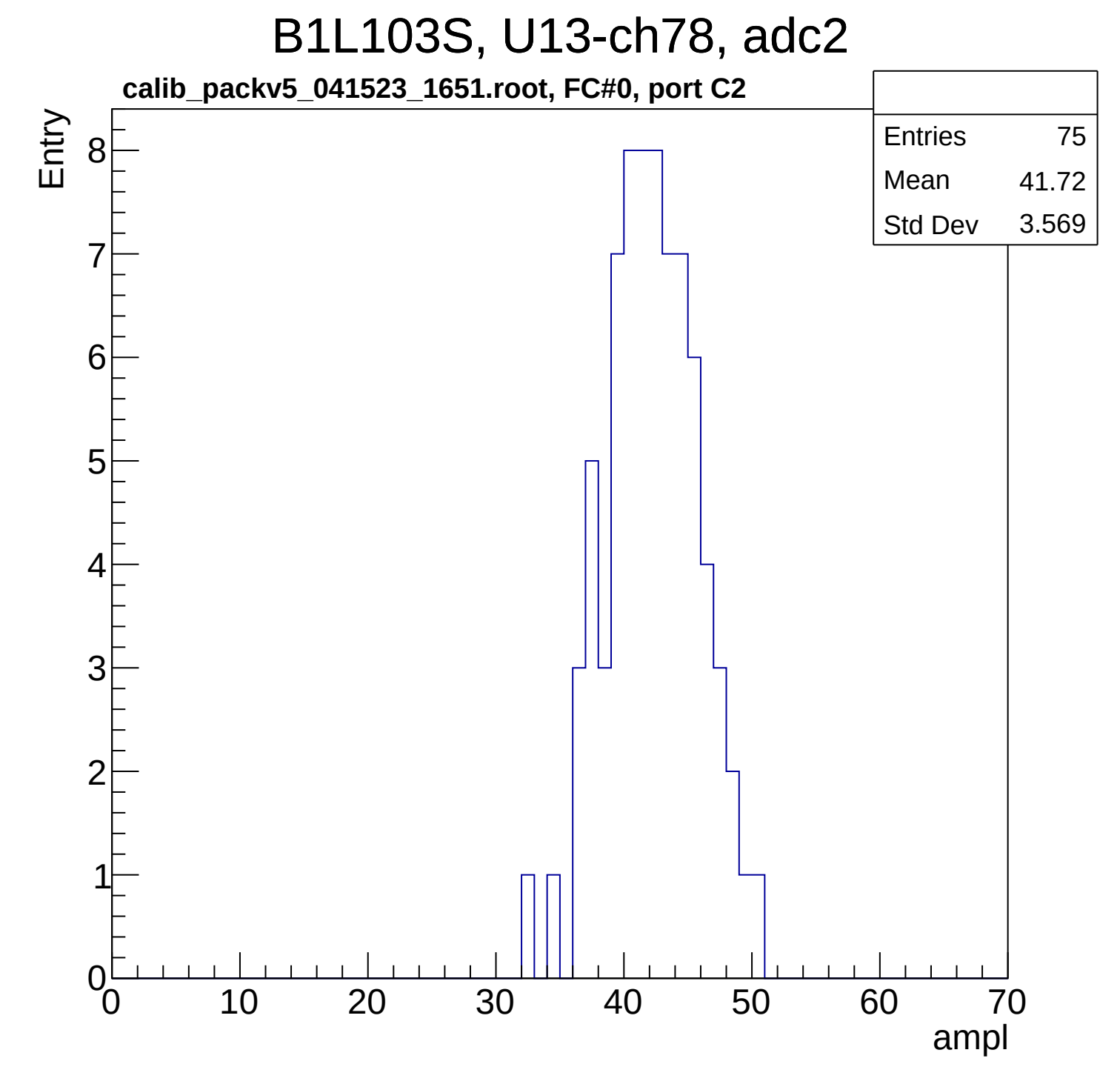
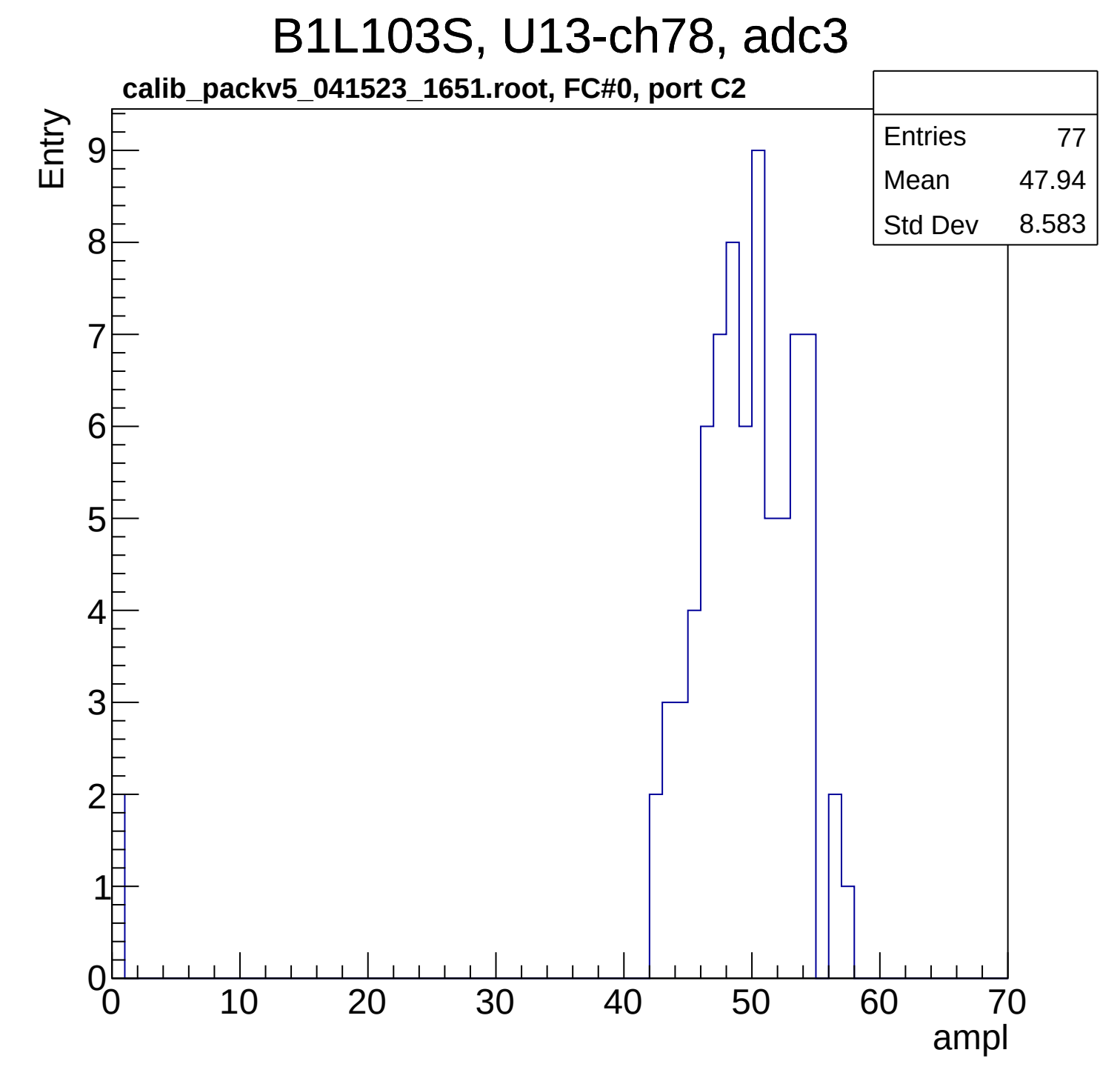
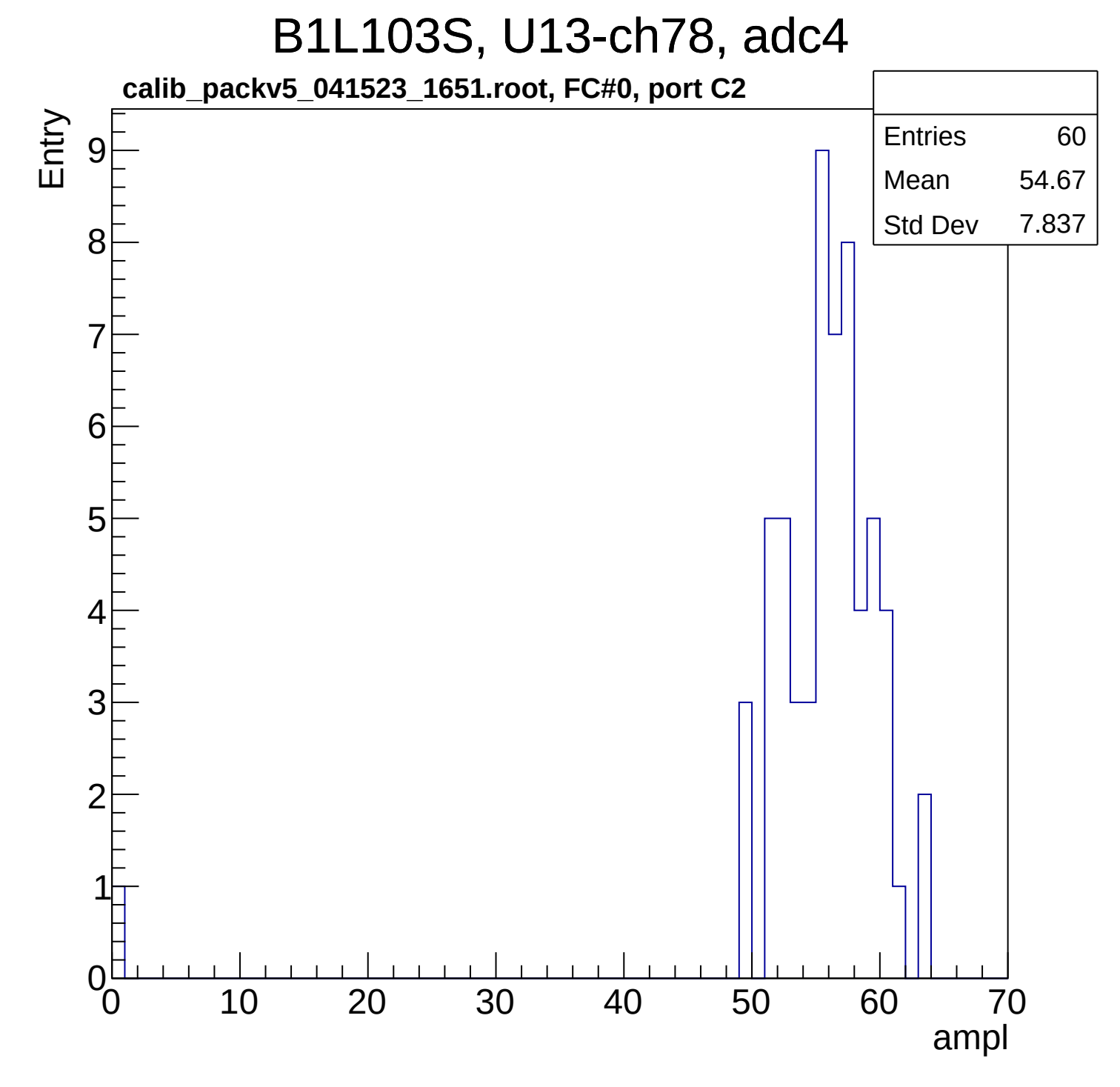

B1L103S, U13-ch77, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

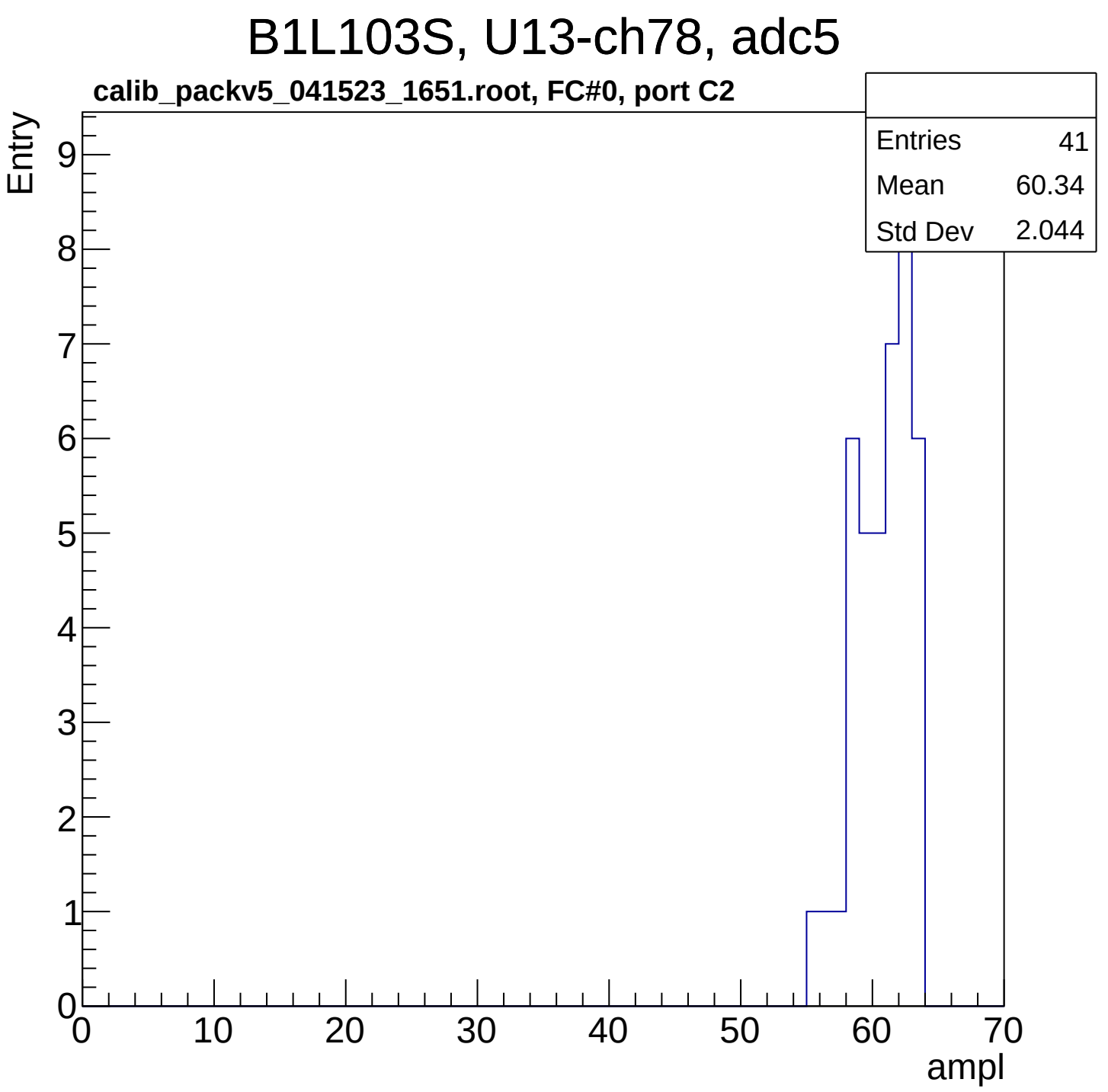

B1L103S, U13-ch78, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 23.38
Std Dev 11.66
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

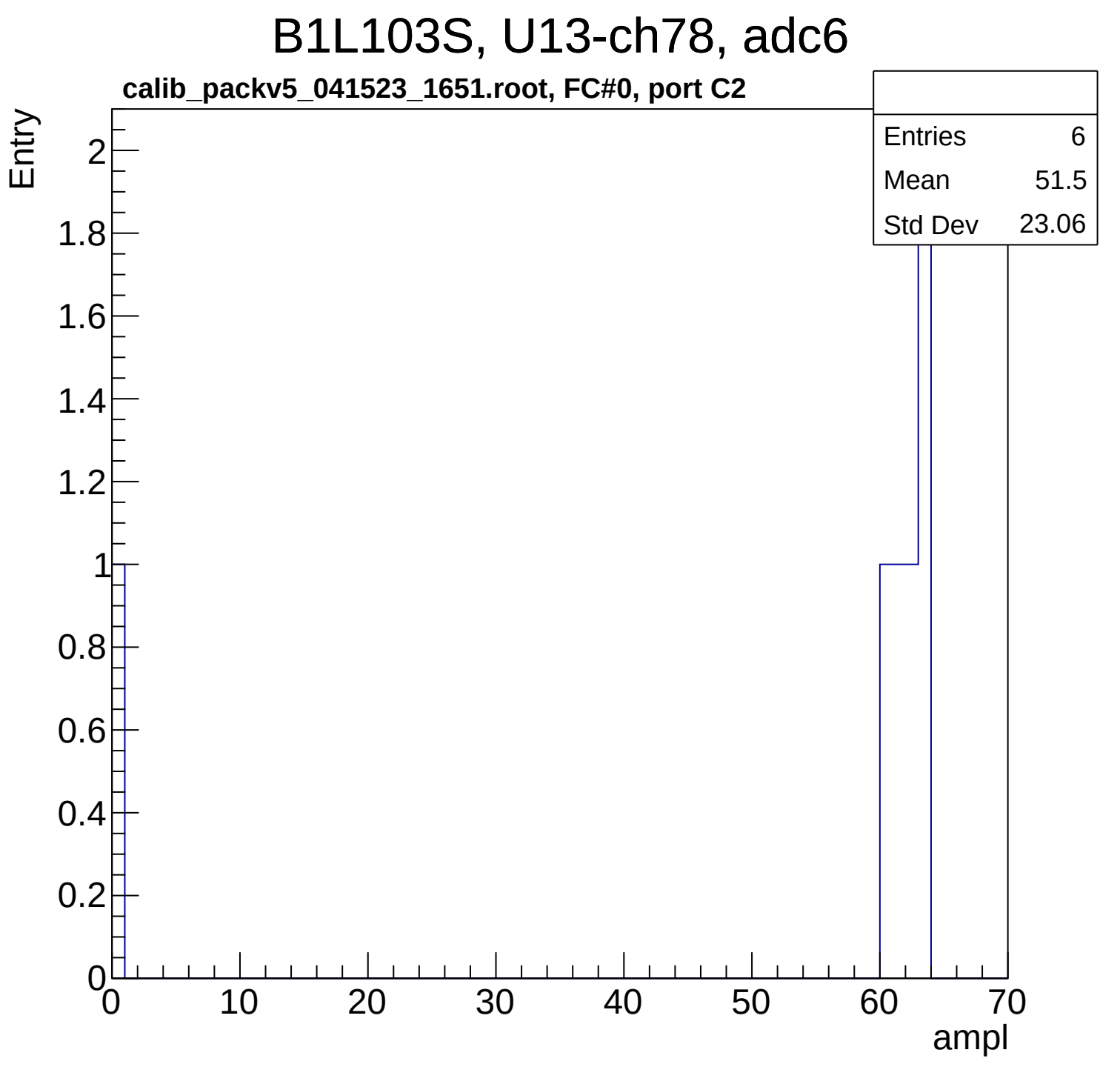

B1L103S, U13-ch78, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 31.27
Std Dev 11.04
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

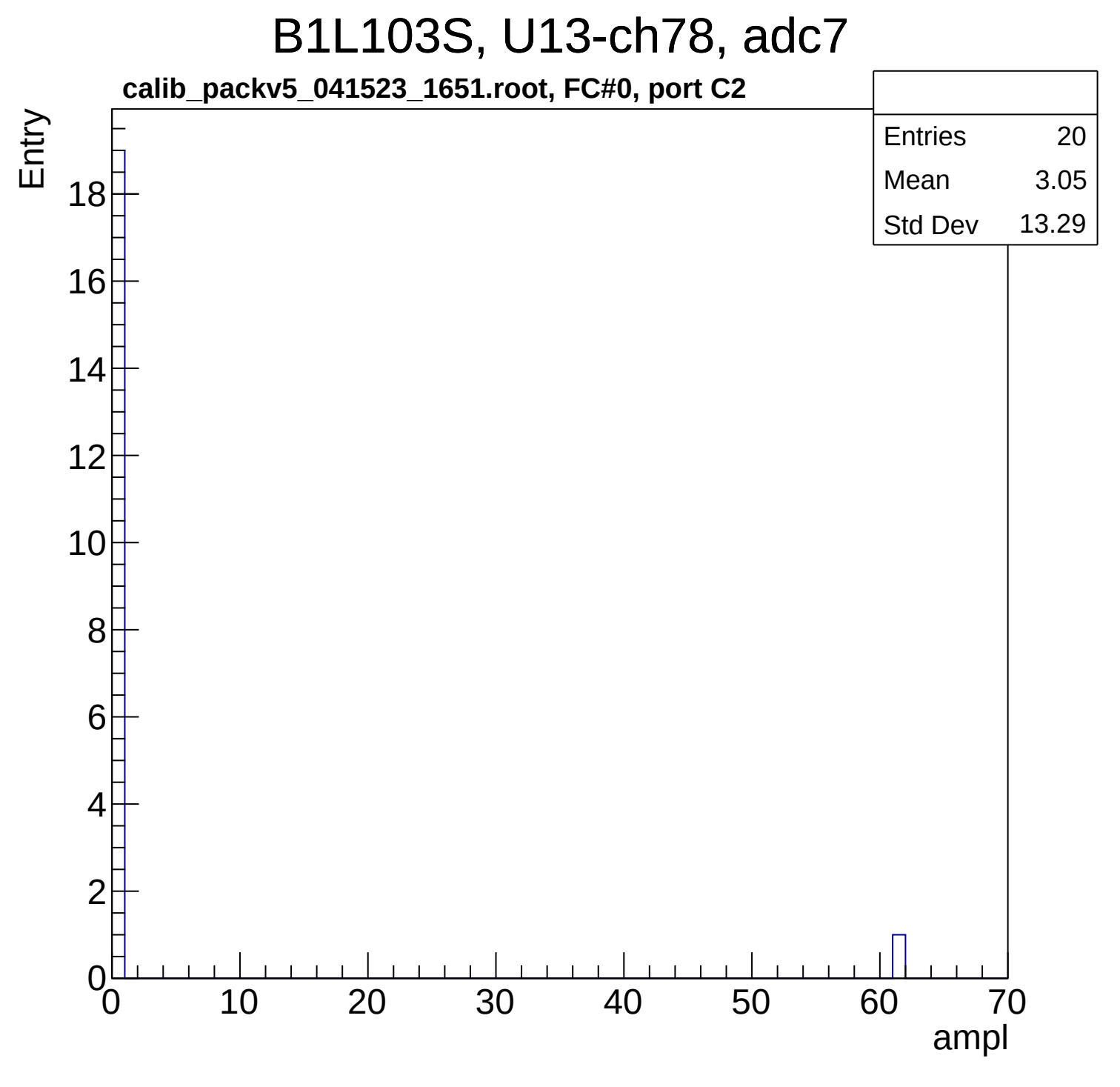

B1L103S, U13-ch78, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 41.72
Std Dev 3.569
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

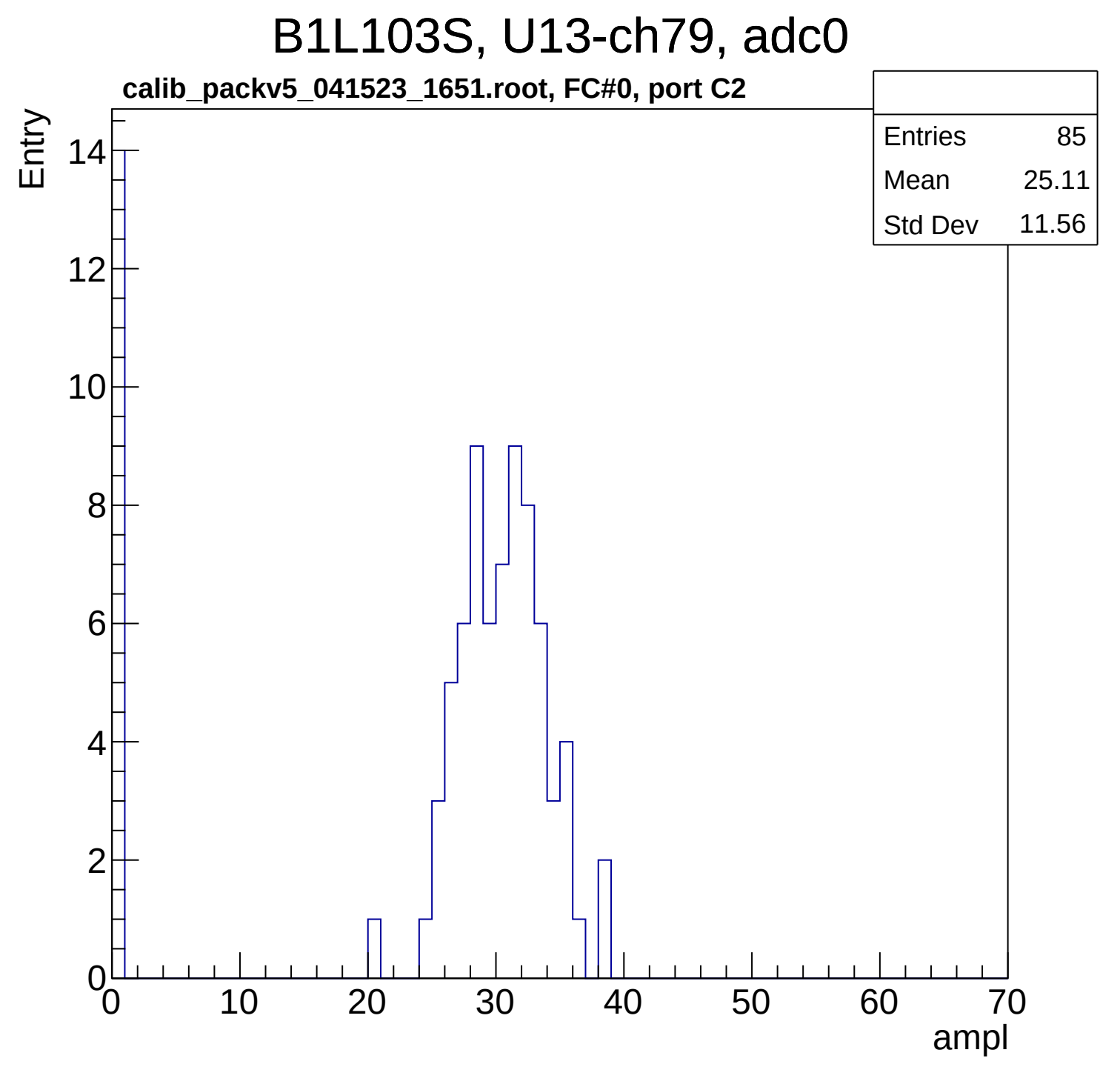

B1L103S, U13-ch78, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 47.94
Std Dev 8.583
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

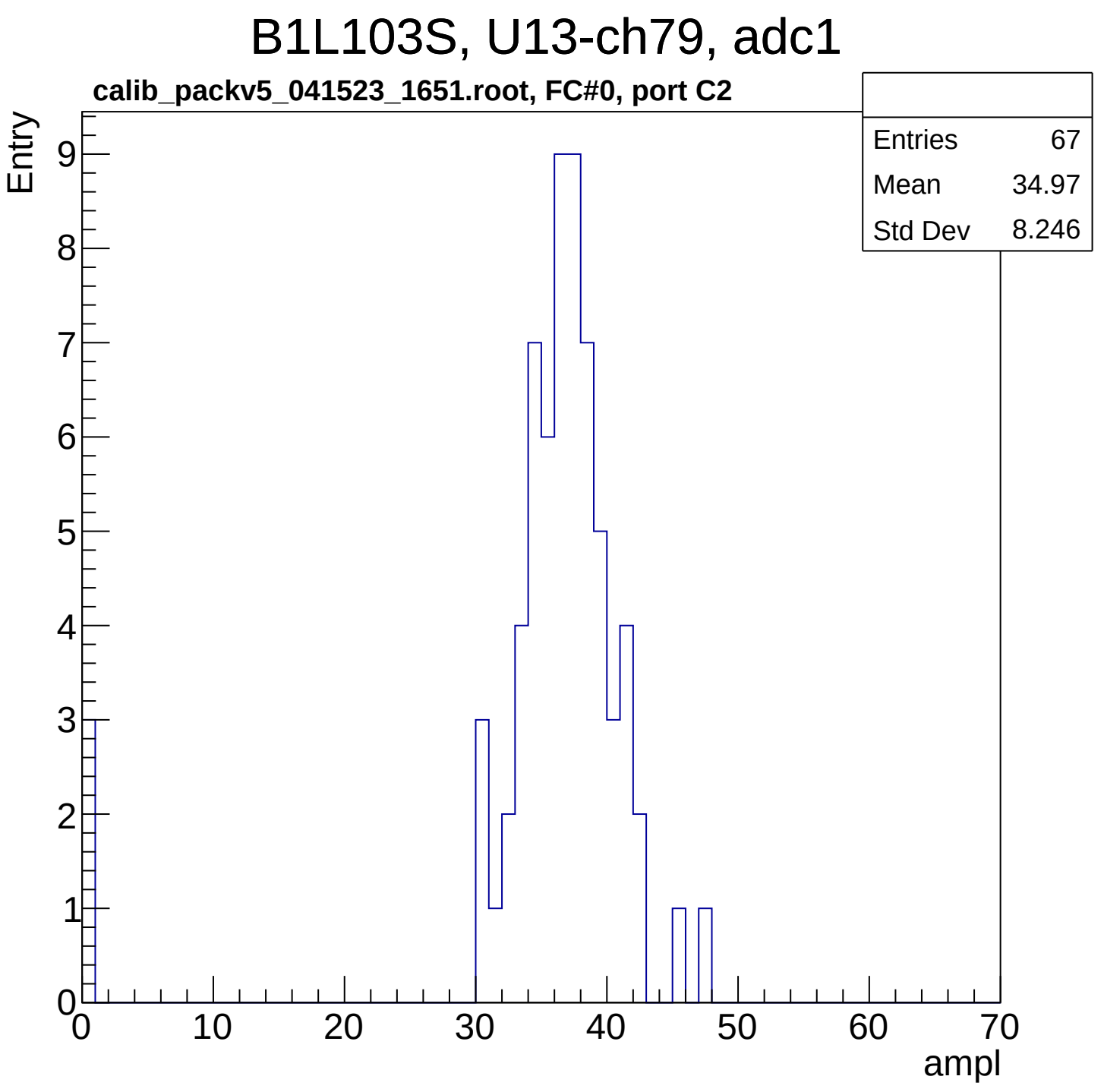

B1L103S, U13-ch78, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 54.67
Std Dev 7.837
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

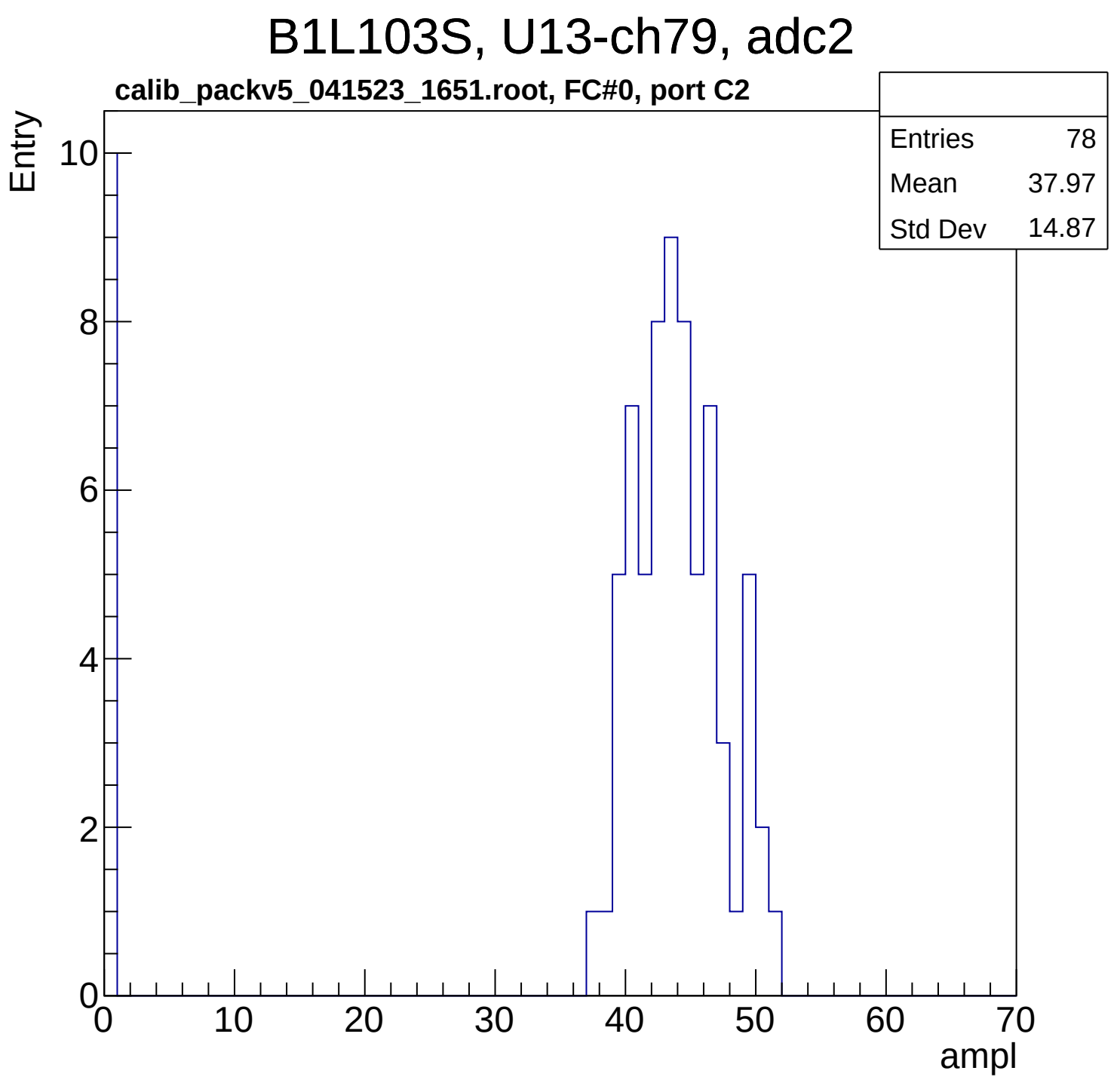

B1L103S, U13-ch78, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 60.34
Std Dev 2.044
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

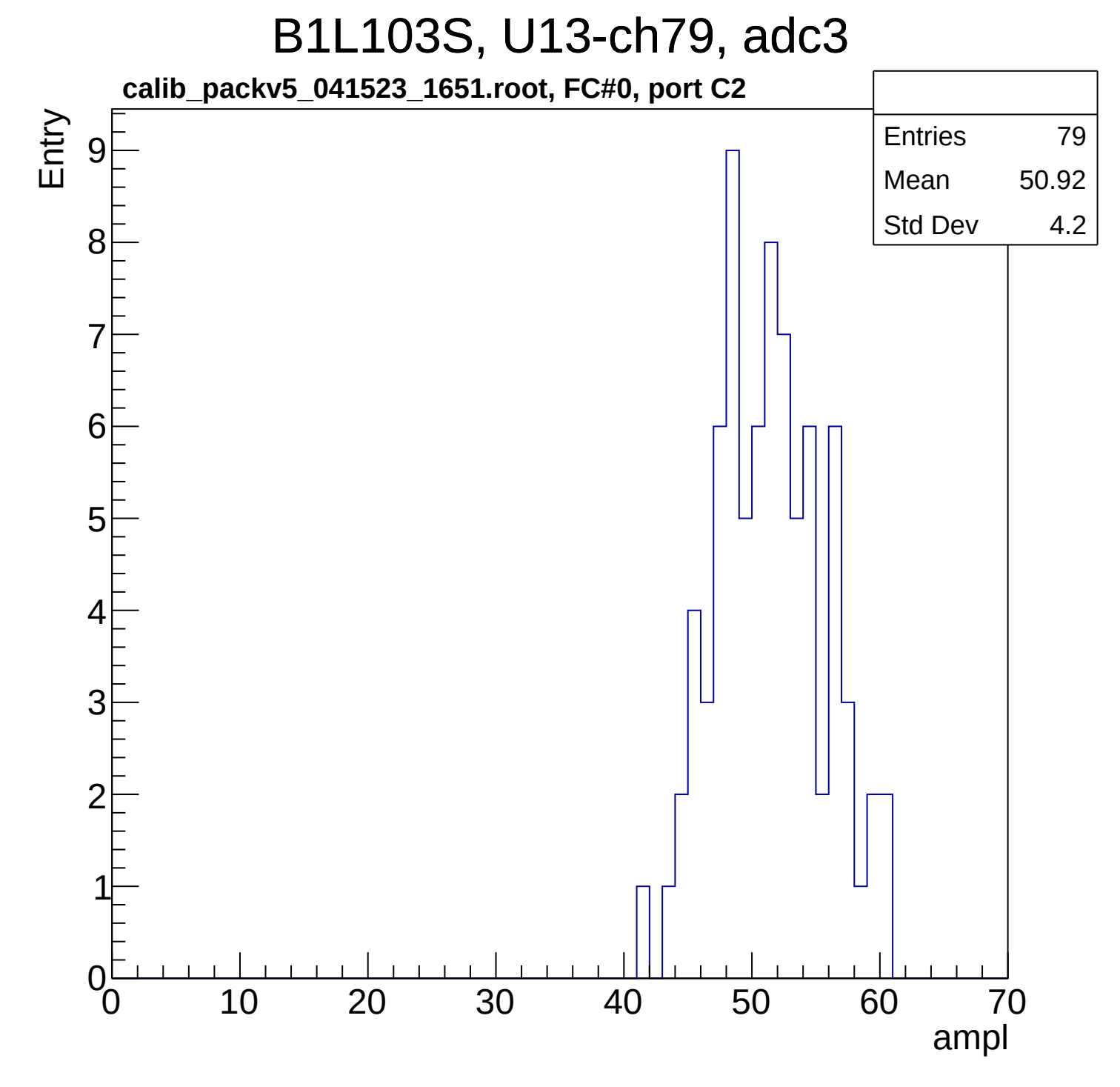

B1L103S, U13-ch78, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 51.5
Std Dev 23.06
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

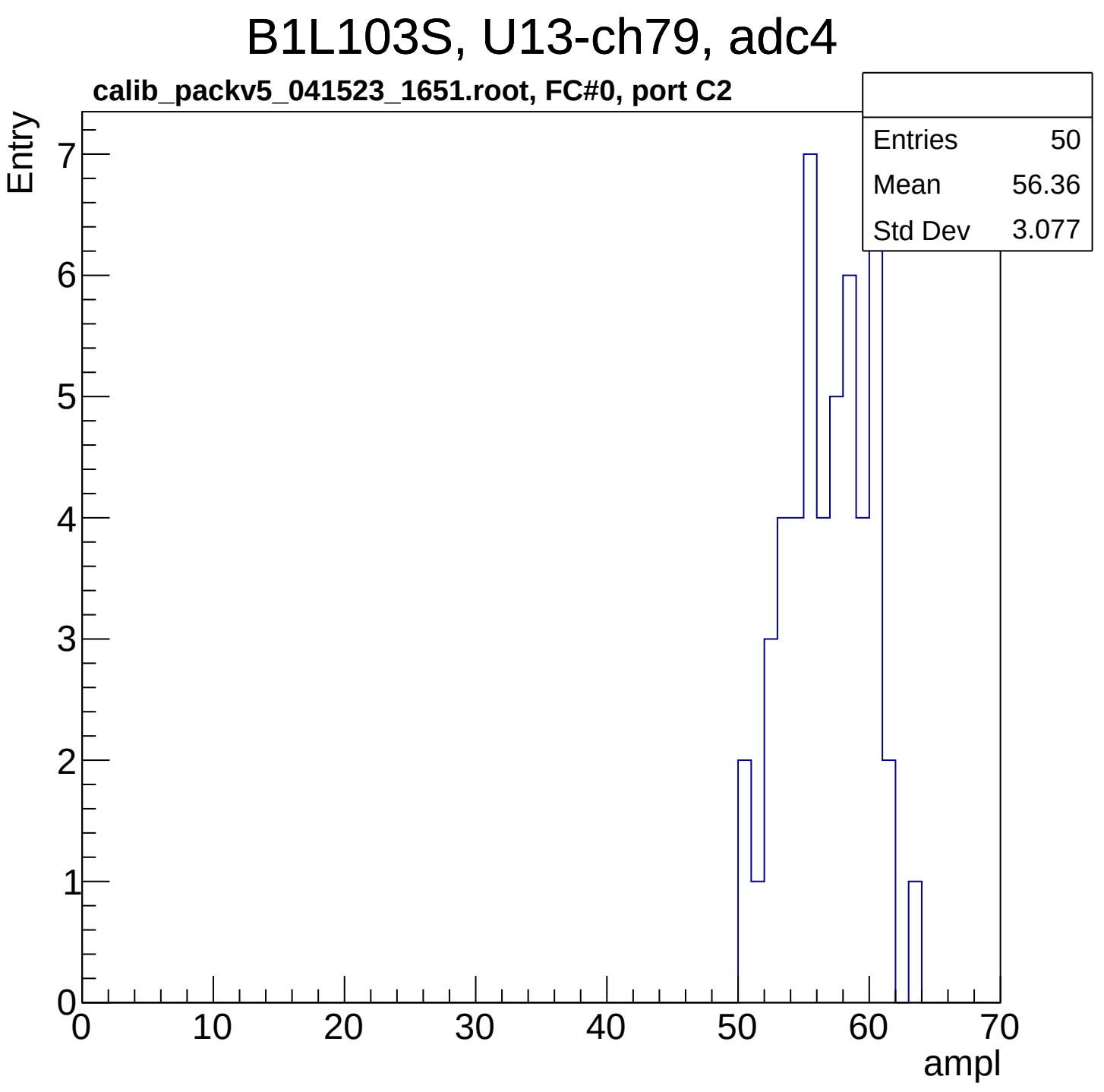

B1L103S, U13-ch78, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

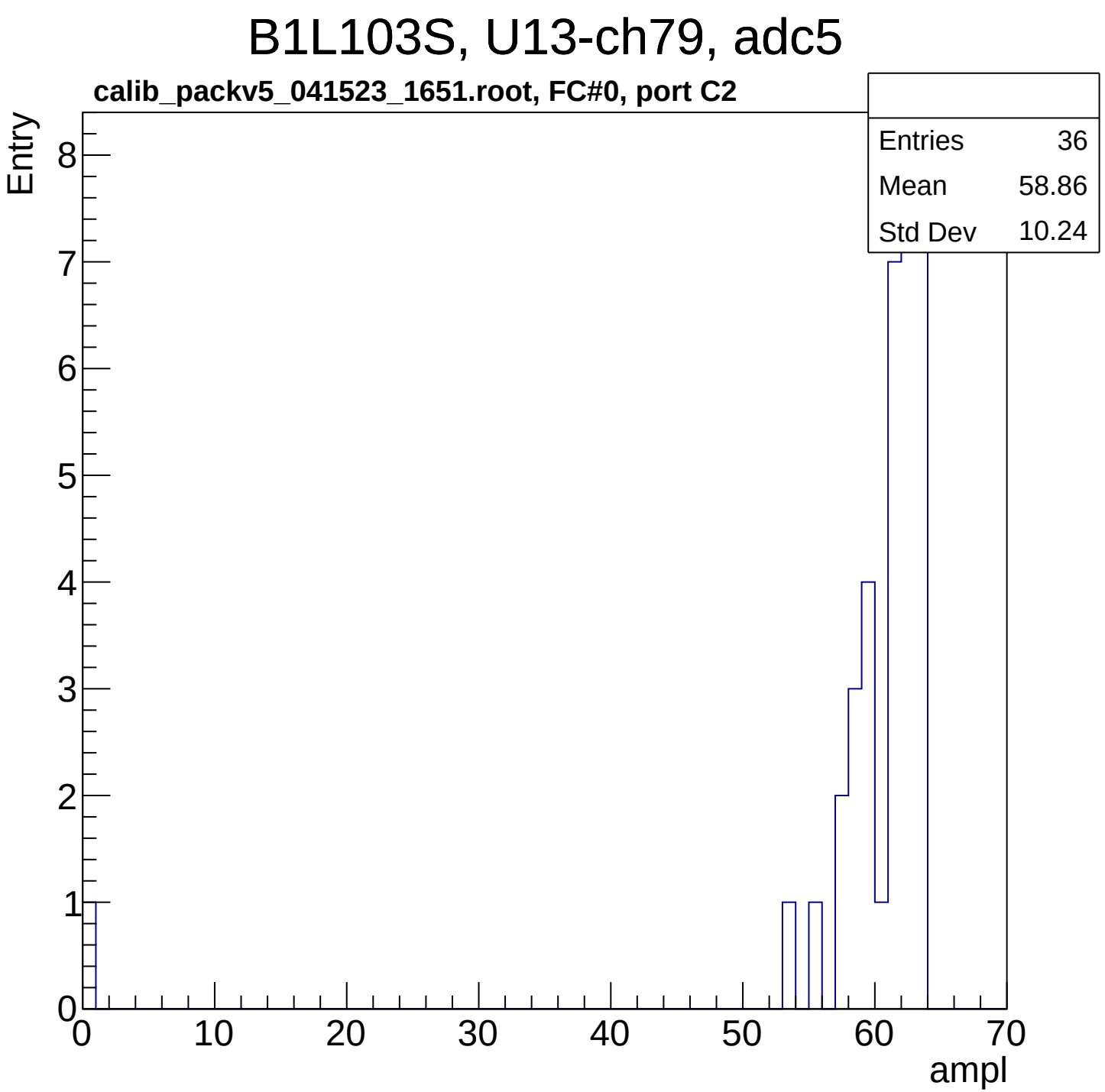

B1L103S, U13-ch79, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 25.11
Std Dev 11.56
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch79, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 34.97
Std Dev 8.246
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch79, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 37.97
Std Dev 14.87
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch79, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 50.92
Std Dev 4.2
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U13-ch79, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 56.36
Std Dev 3.077
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch79, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 58.86
Std Dev 10.24
Entry
ampl
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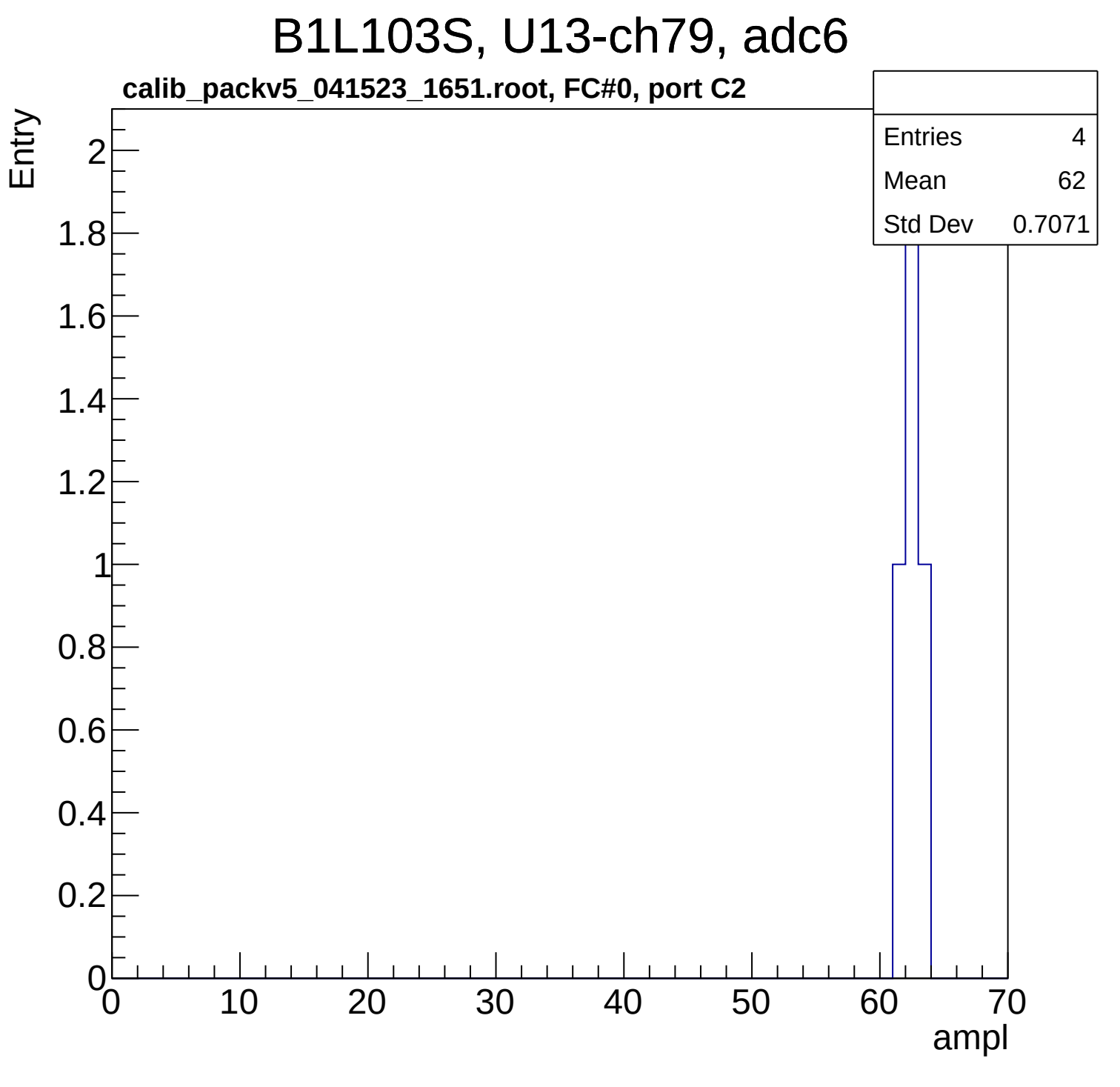
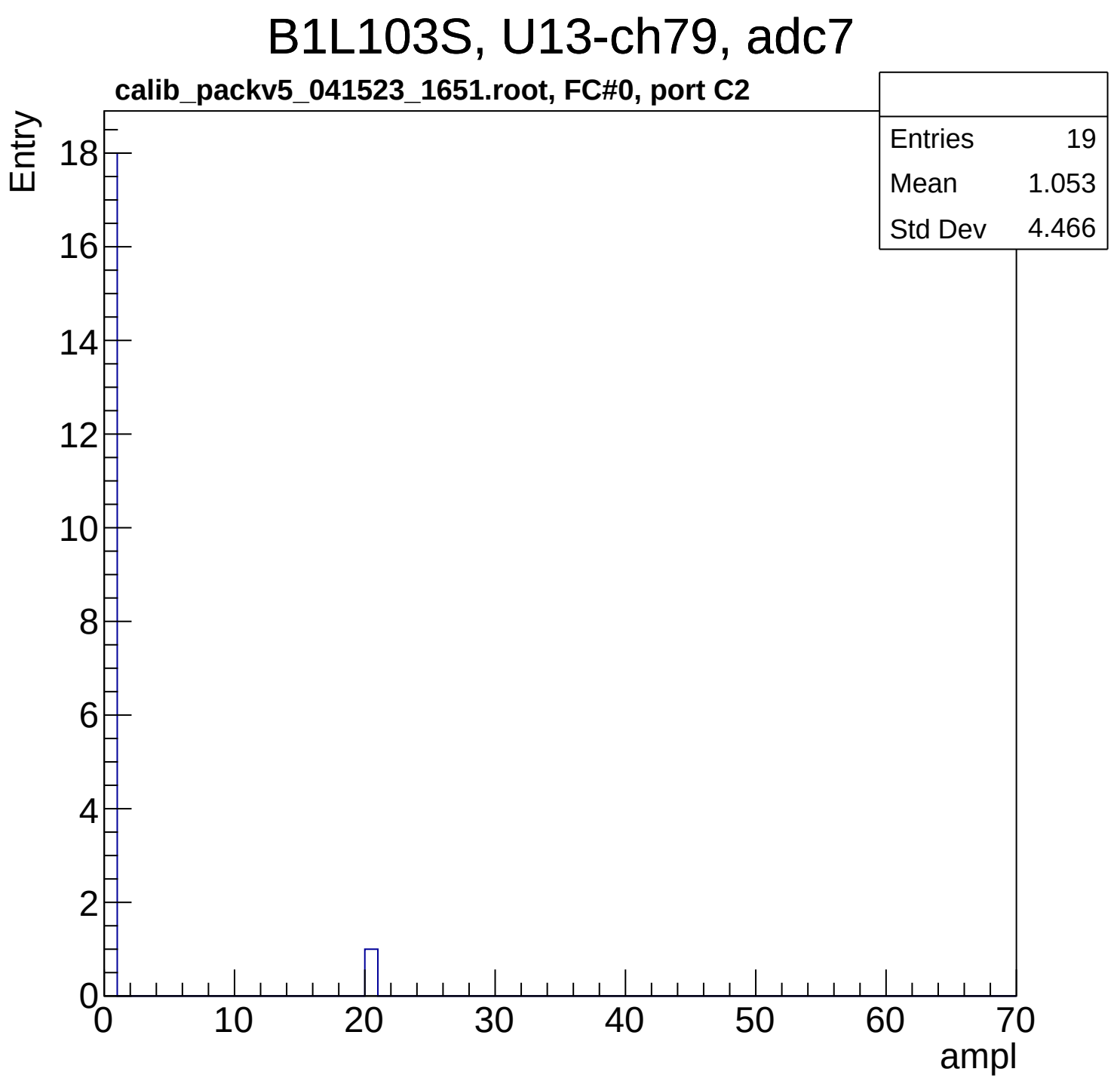
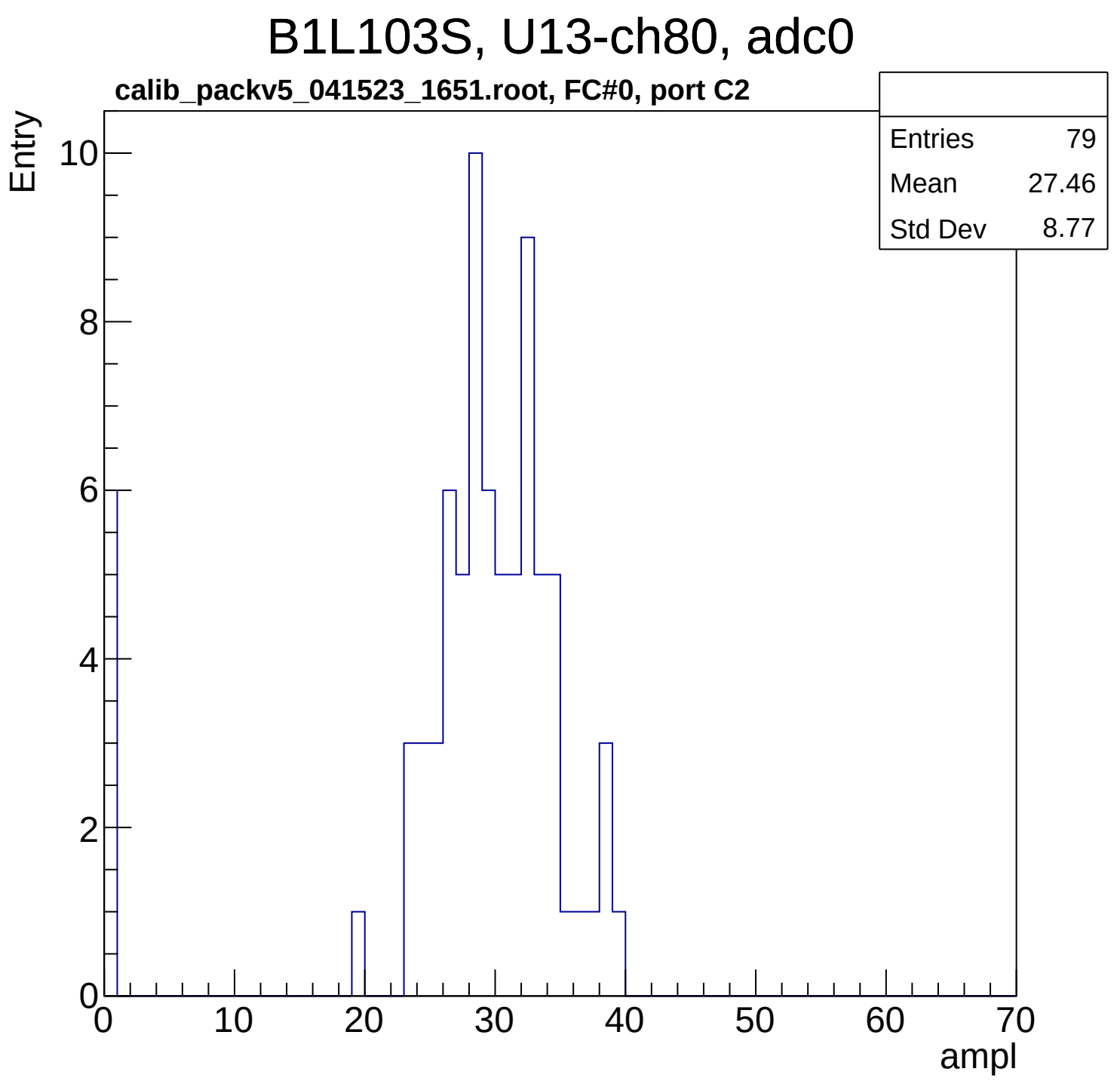
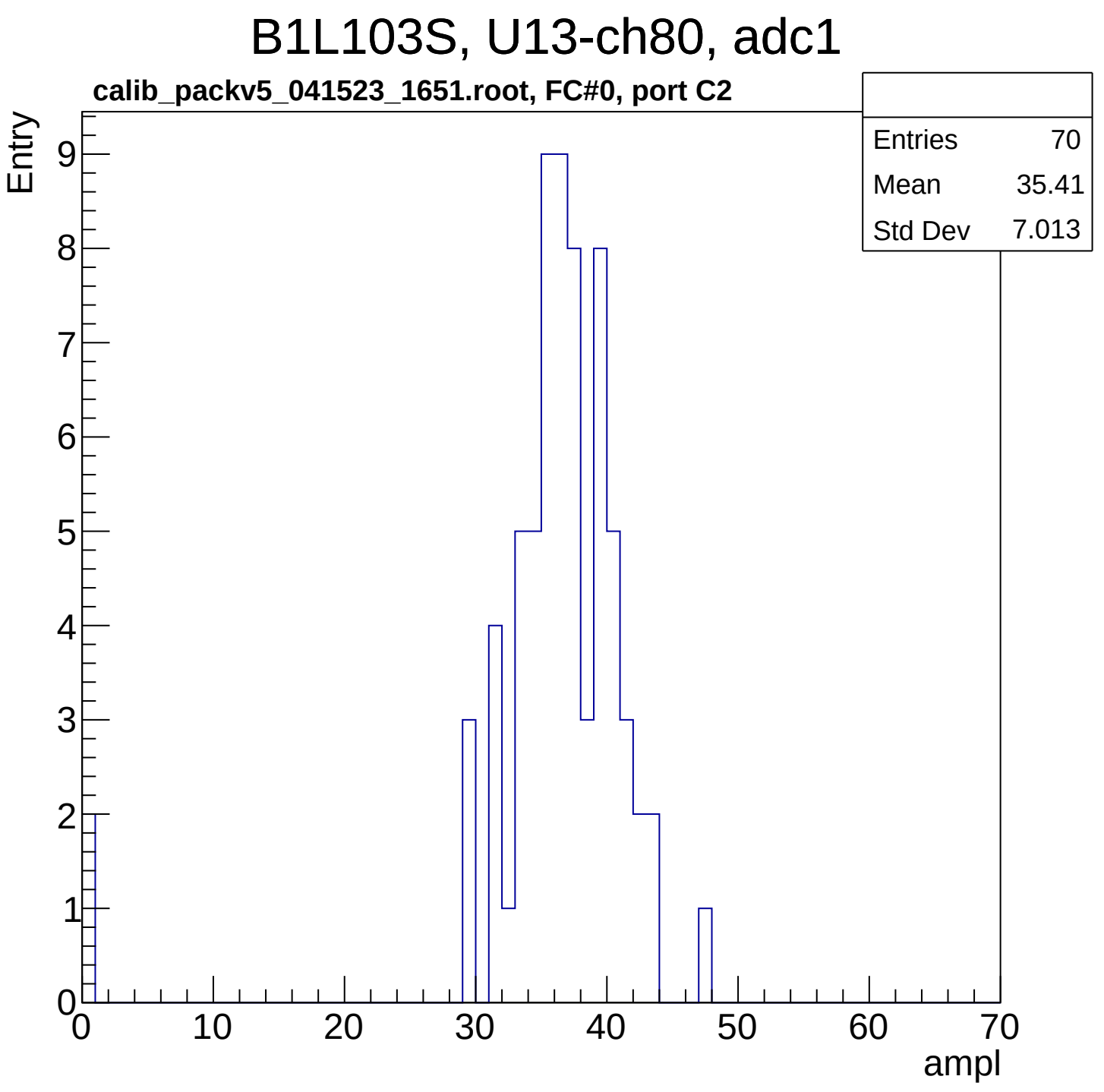
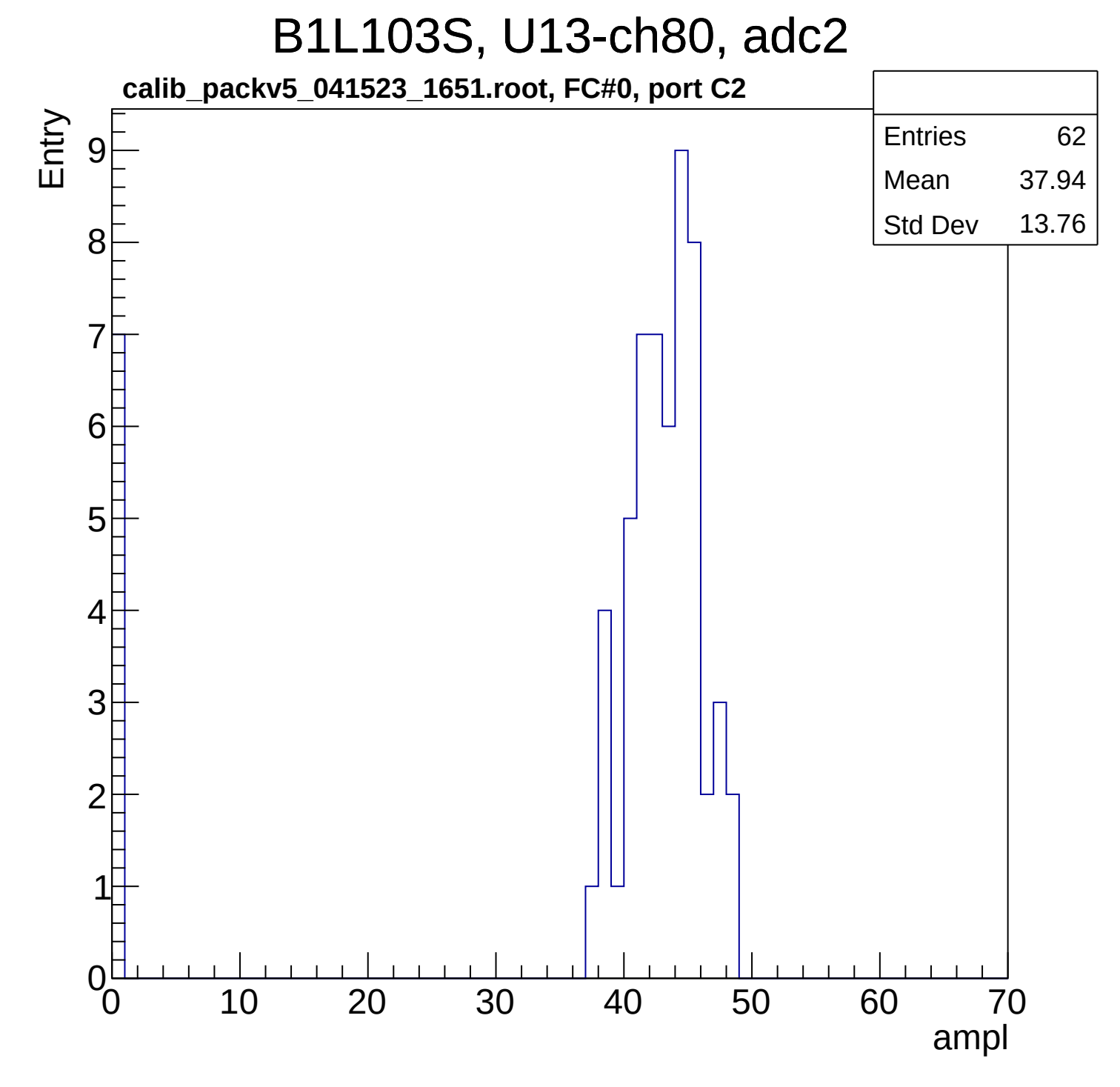
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

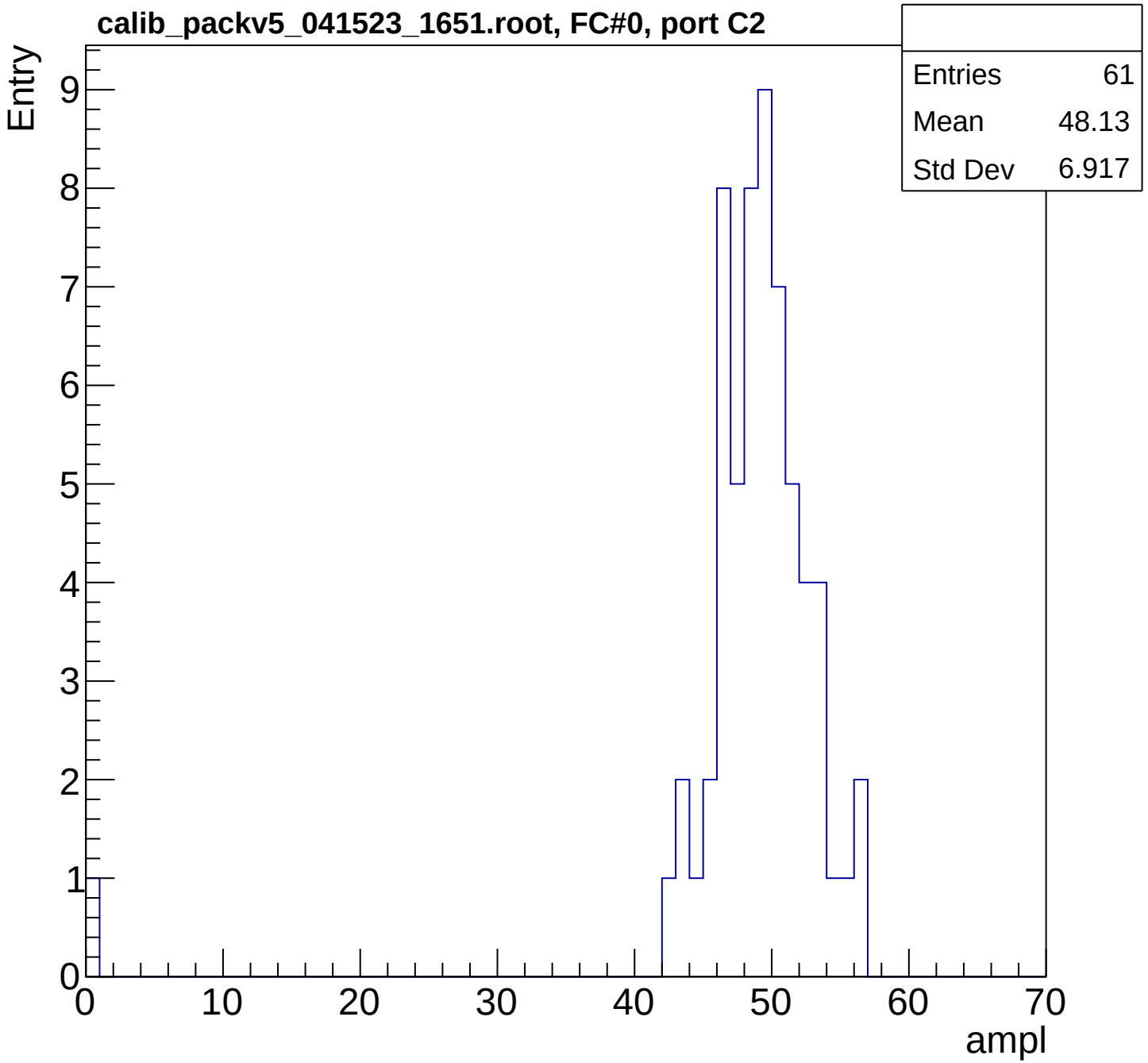

B1L103S, U13-ch79, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62
Std Dev 0.7071
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

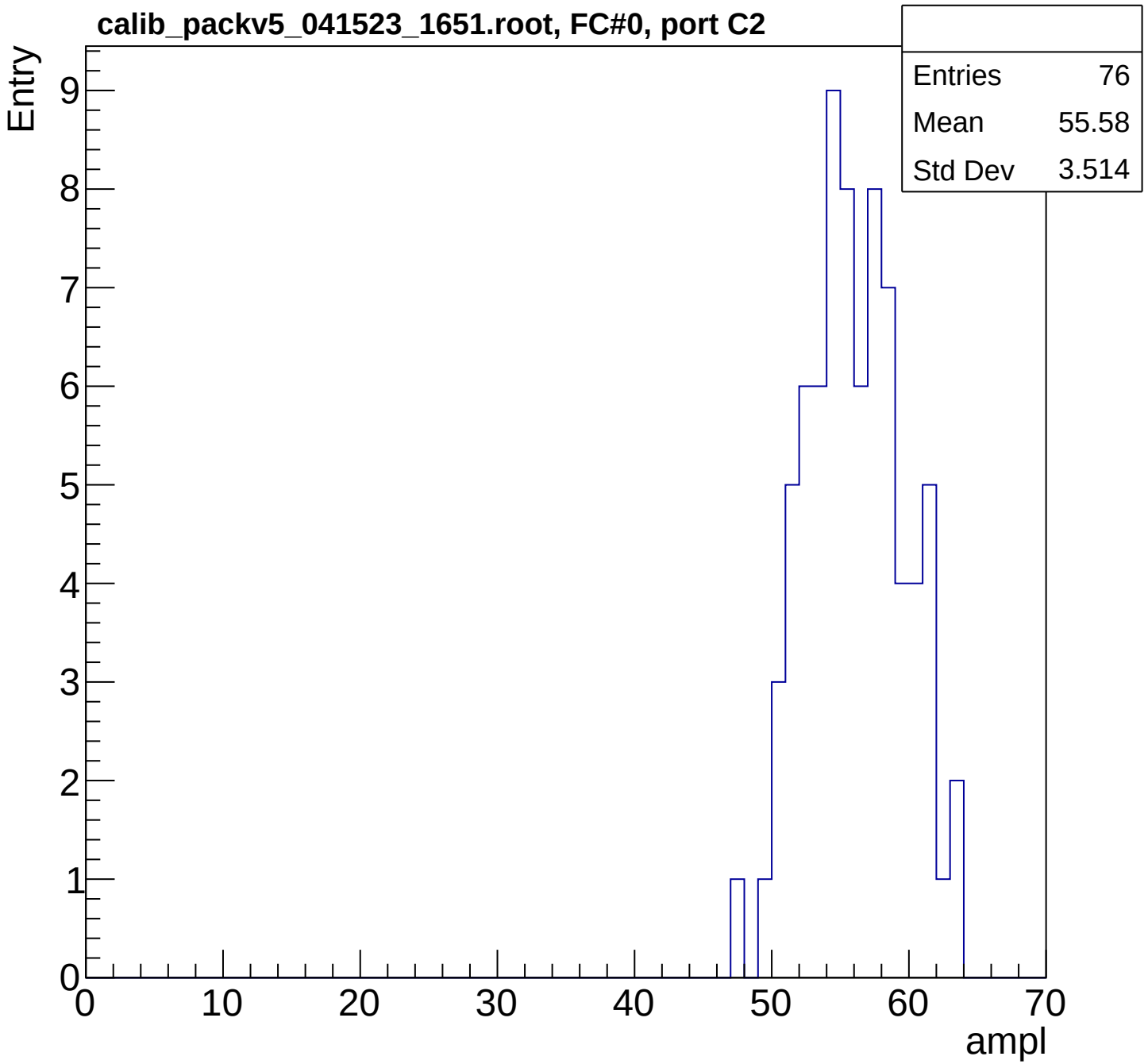

B1L103S, U13-ch79, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.053
Std Dev 4.466
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

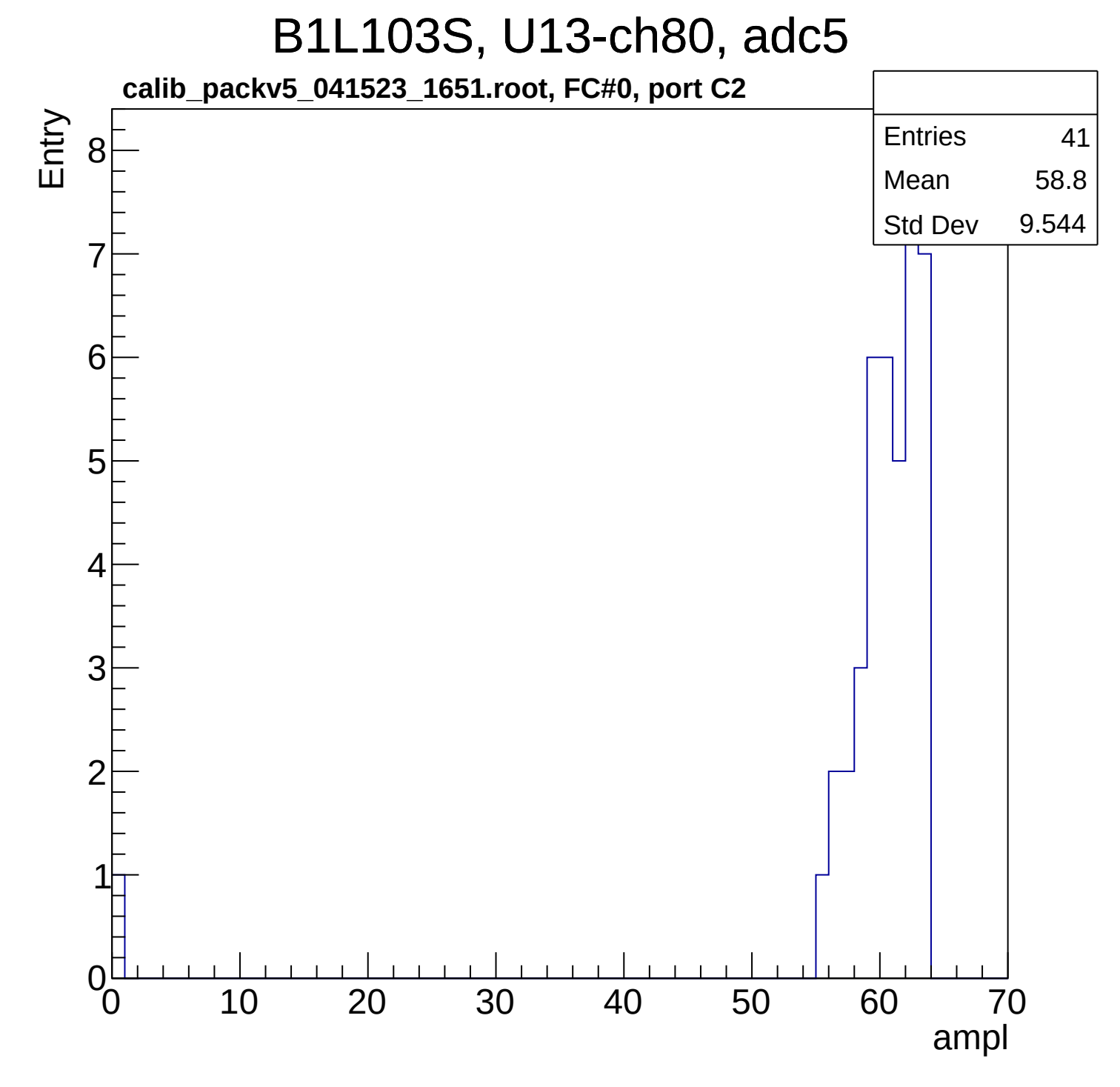

B1L103S, U13-ch80, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 27.46
Std Dev 8.77
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

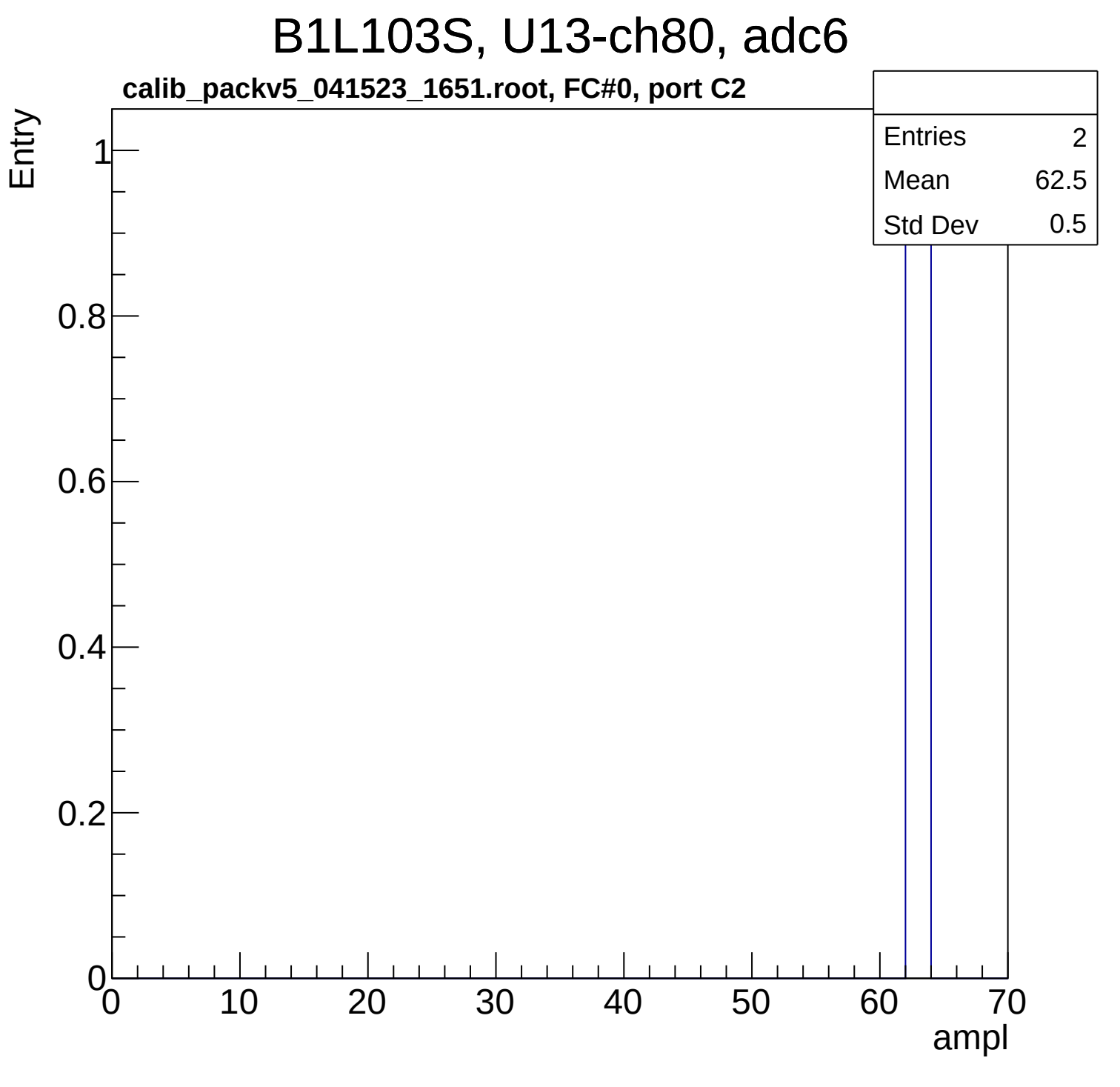

B1L103S, U13-ch80, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 35.41
Std Dev 7.013
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

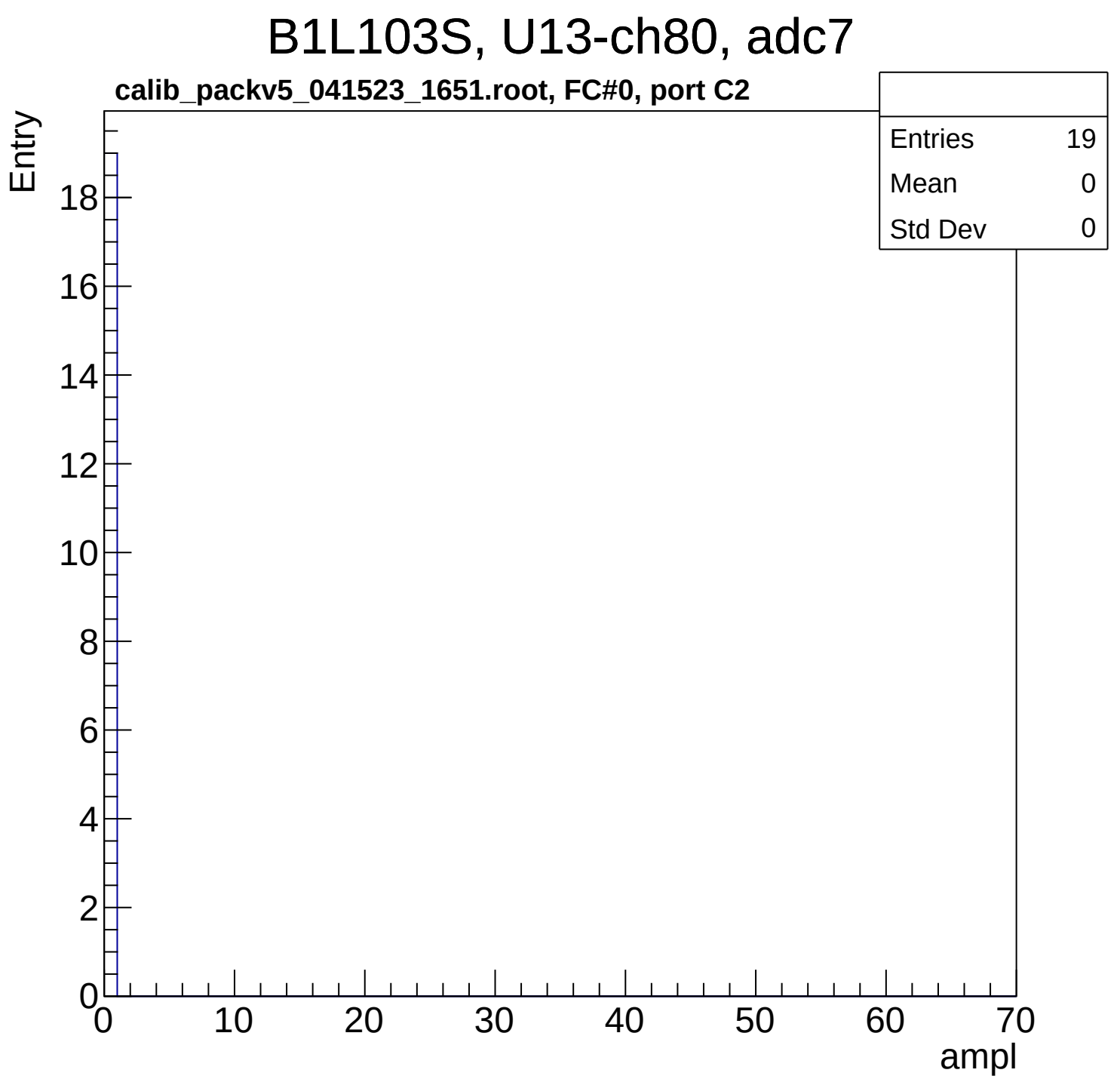

B1L103S, U13-ch80, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 37.94
Std Dev 13.76
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

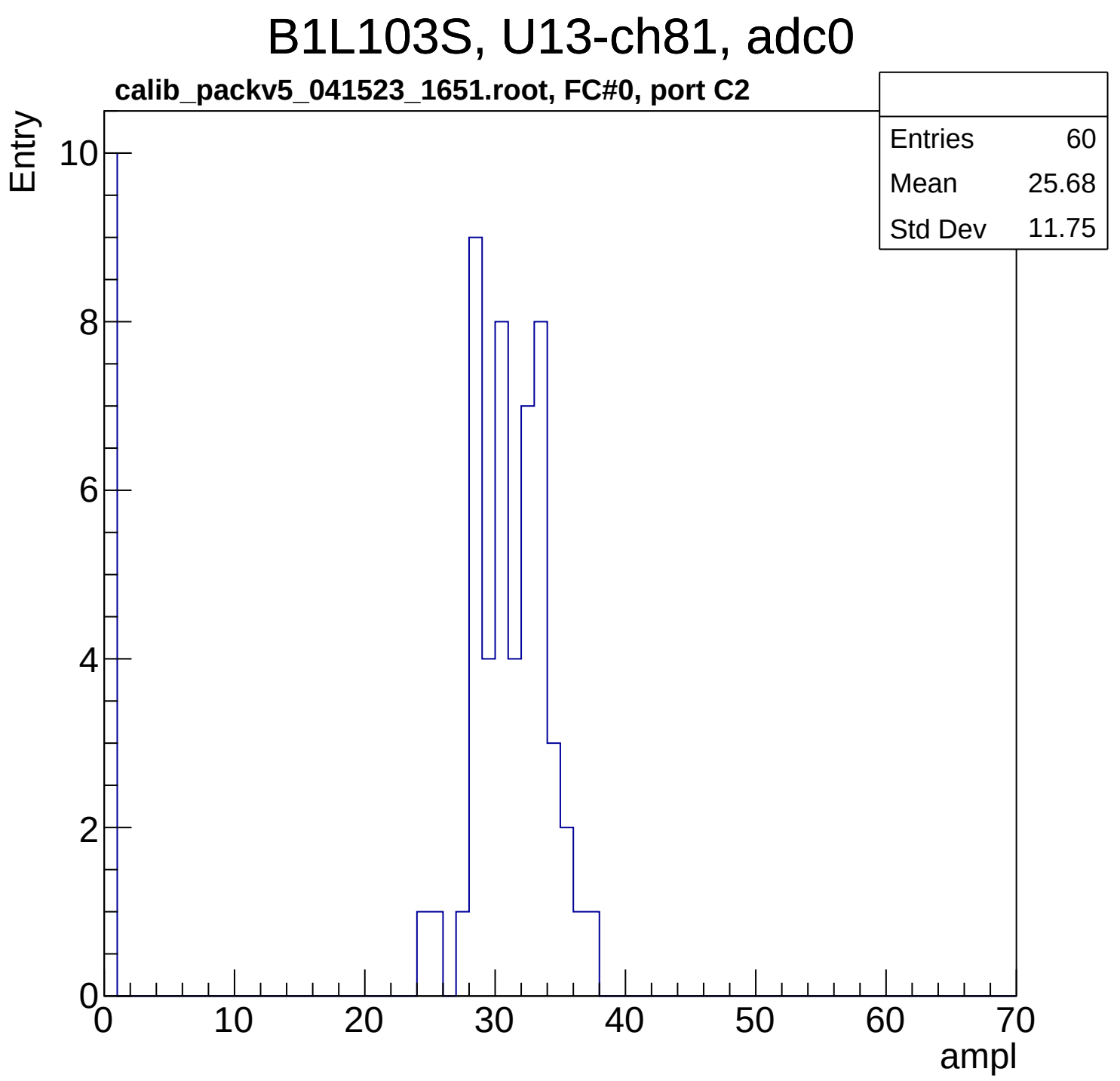

B1L103S, U13-ch80, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 48.13
Std Dev 6.917
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

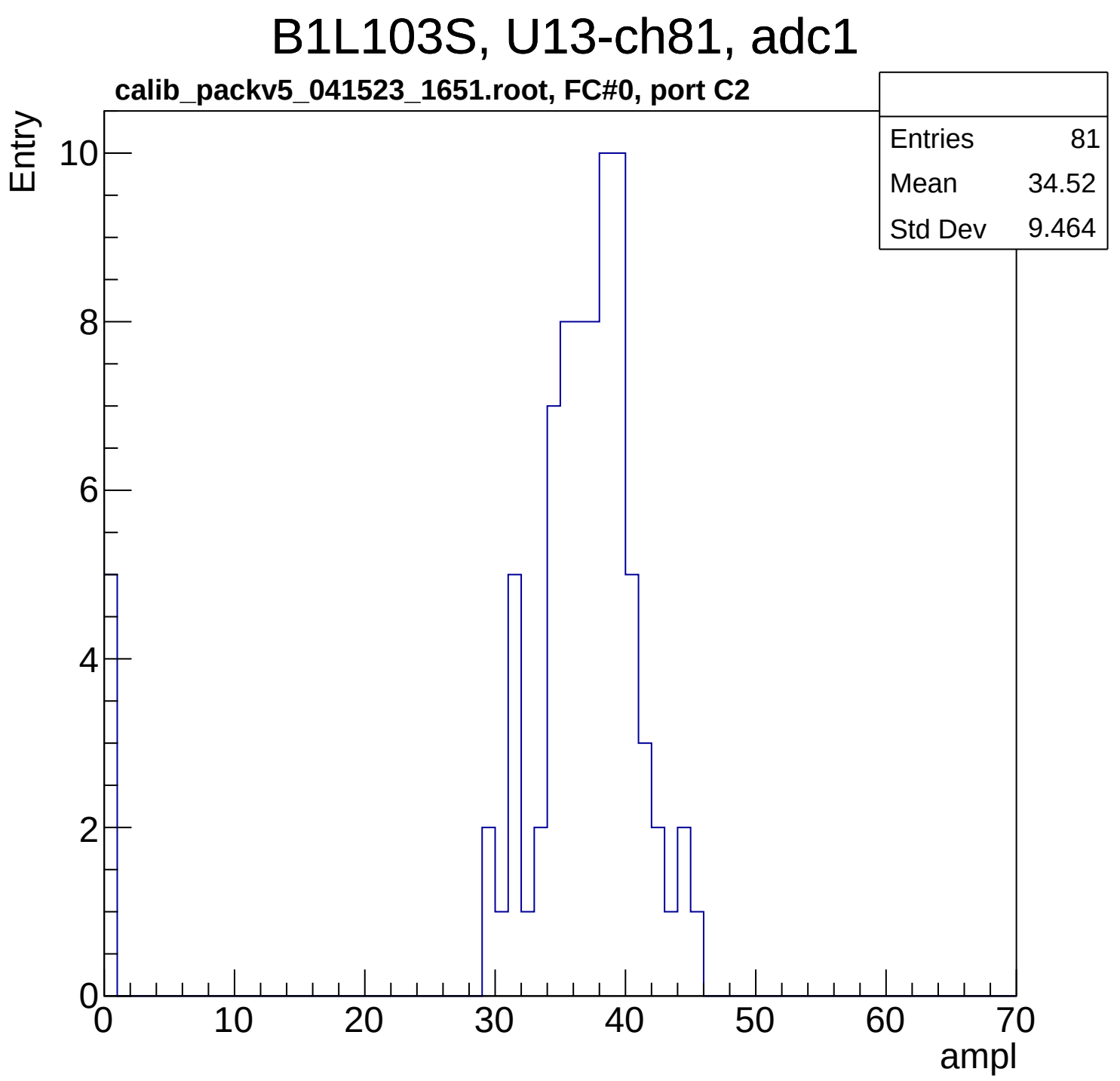

B1L103S, U13-ch80, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 55.58
Std Dev 3.514
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

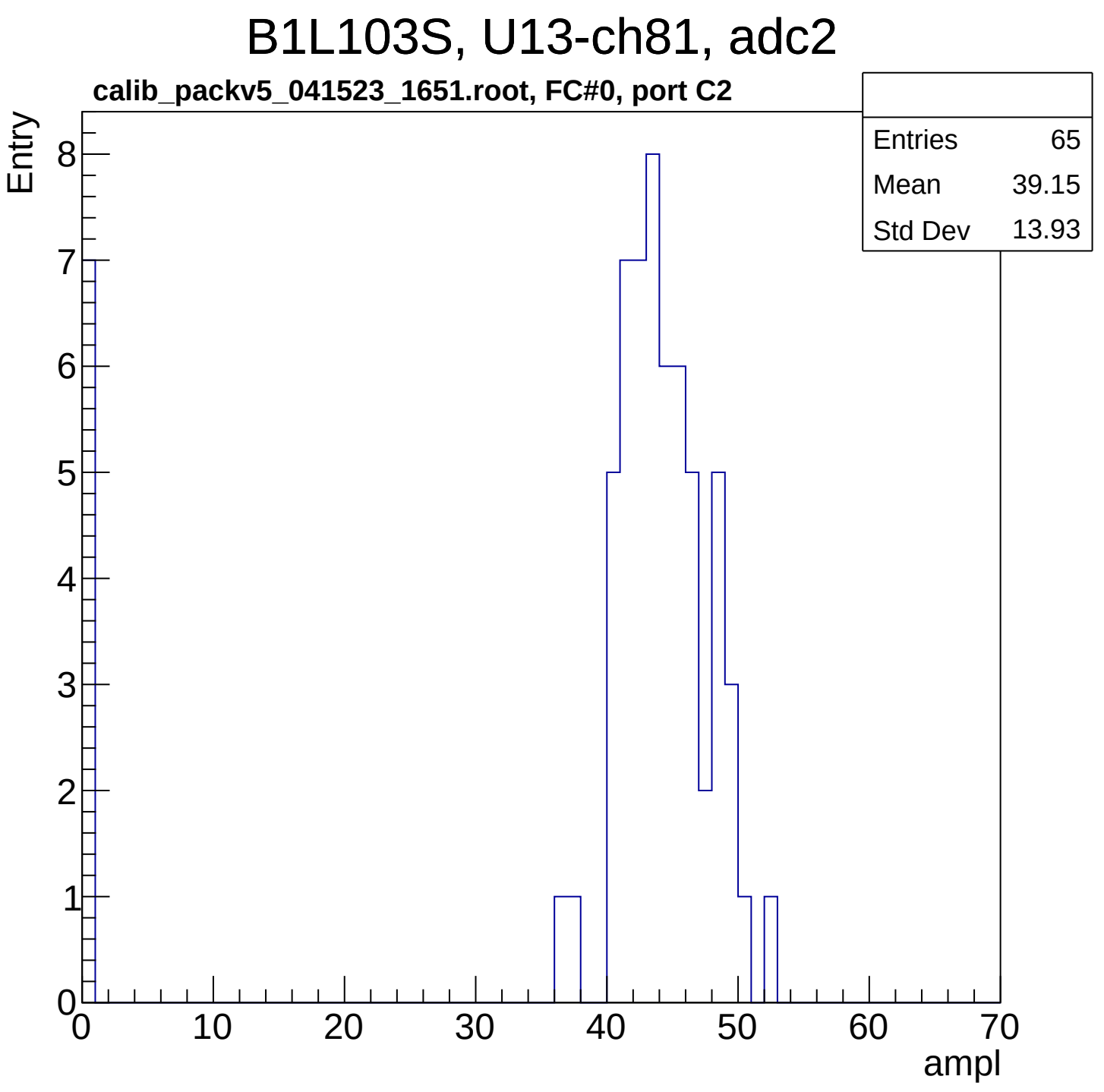

B1L103S, U13-ch80, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 58.8
Std Dev 9.544
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

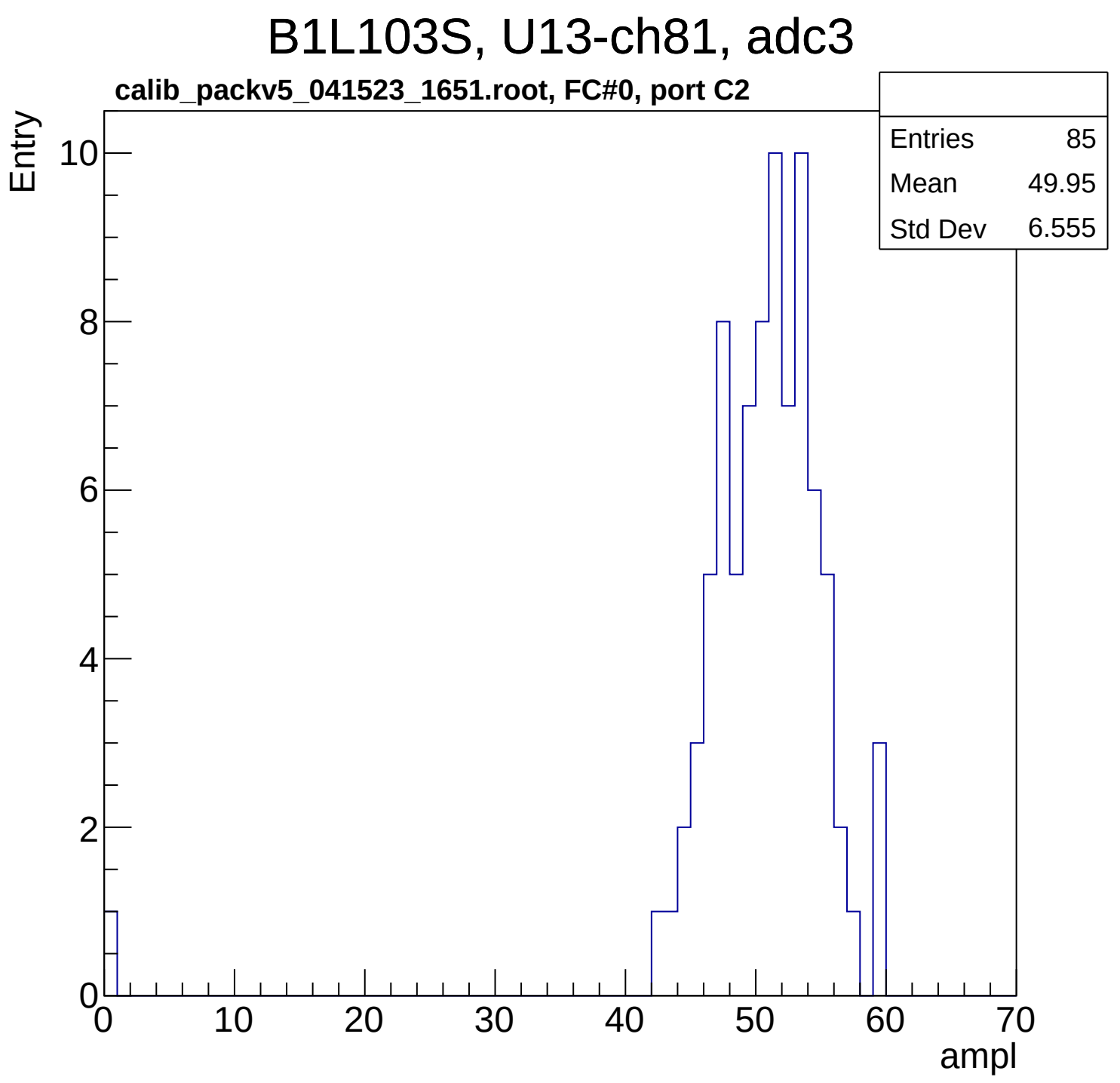

B1L103S, U13-ch80, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch80, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch81, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 25.68
Std Dev 11.75
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch81, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 34.52
Std Dev 9.464
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch81, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 39.15
Std Dev 13.93
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch81, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 49.95
Std Dev 6.555
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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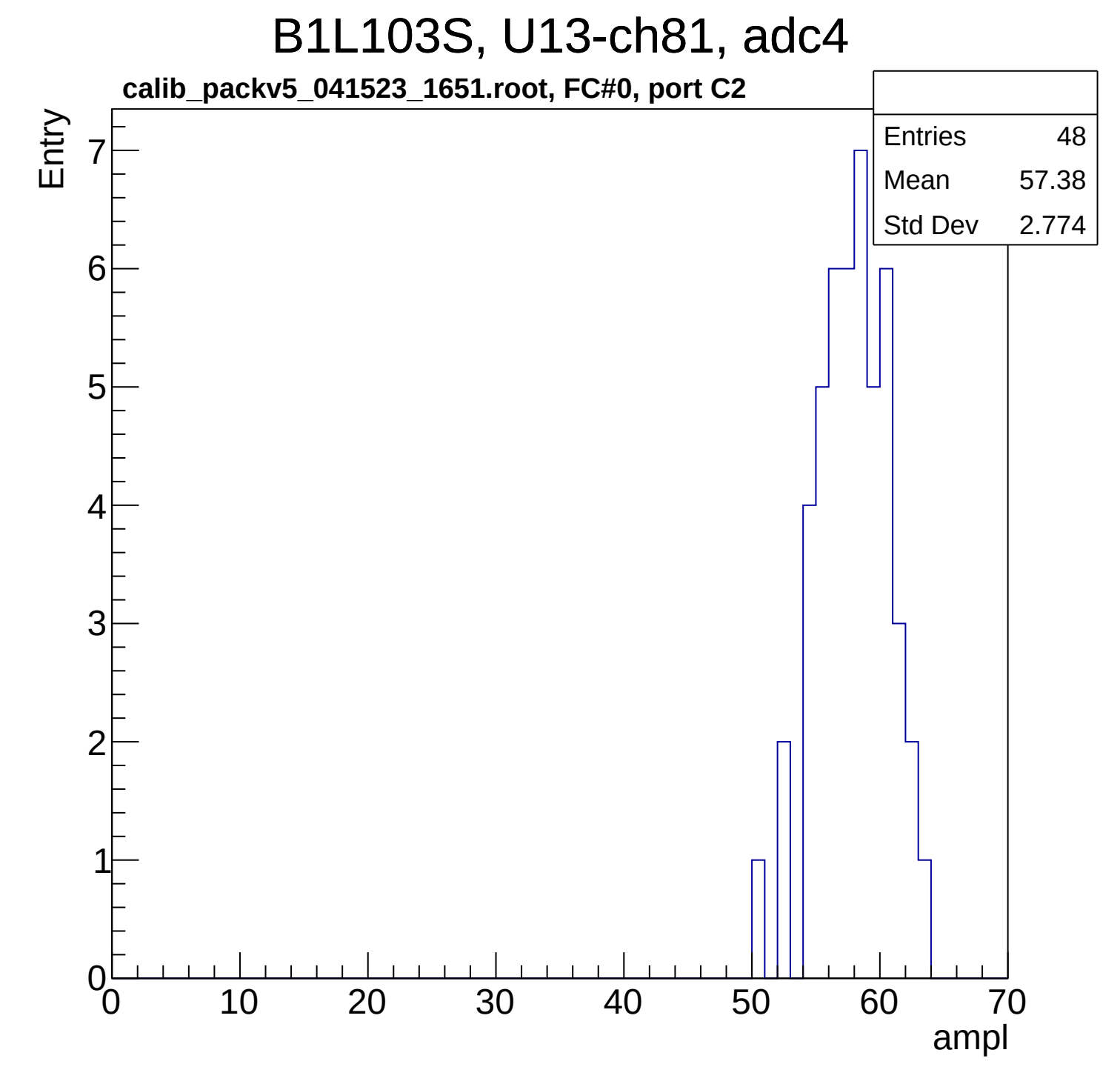
B1L103S, U13-ch81, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 57.38
Std Dev 2.774
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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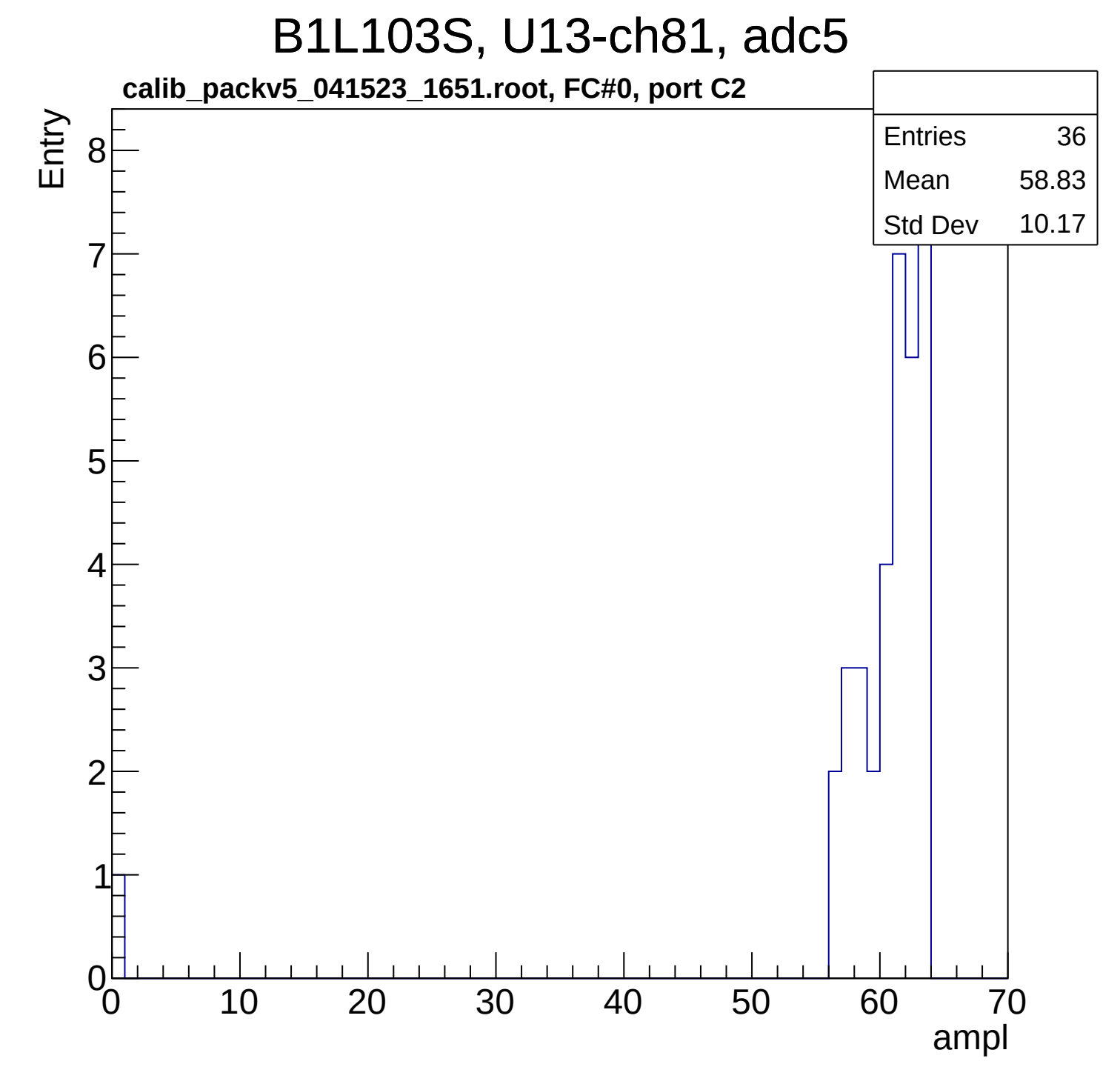
B1L103S, U13-ch81, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 58.83
Std Dev 10.17
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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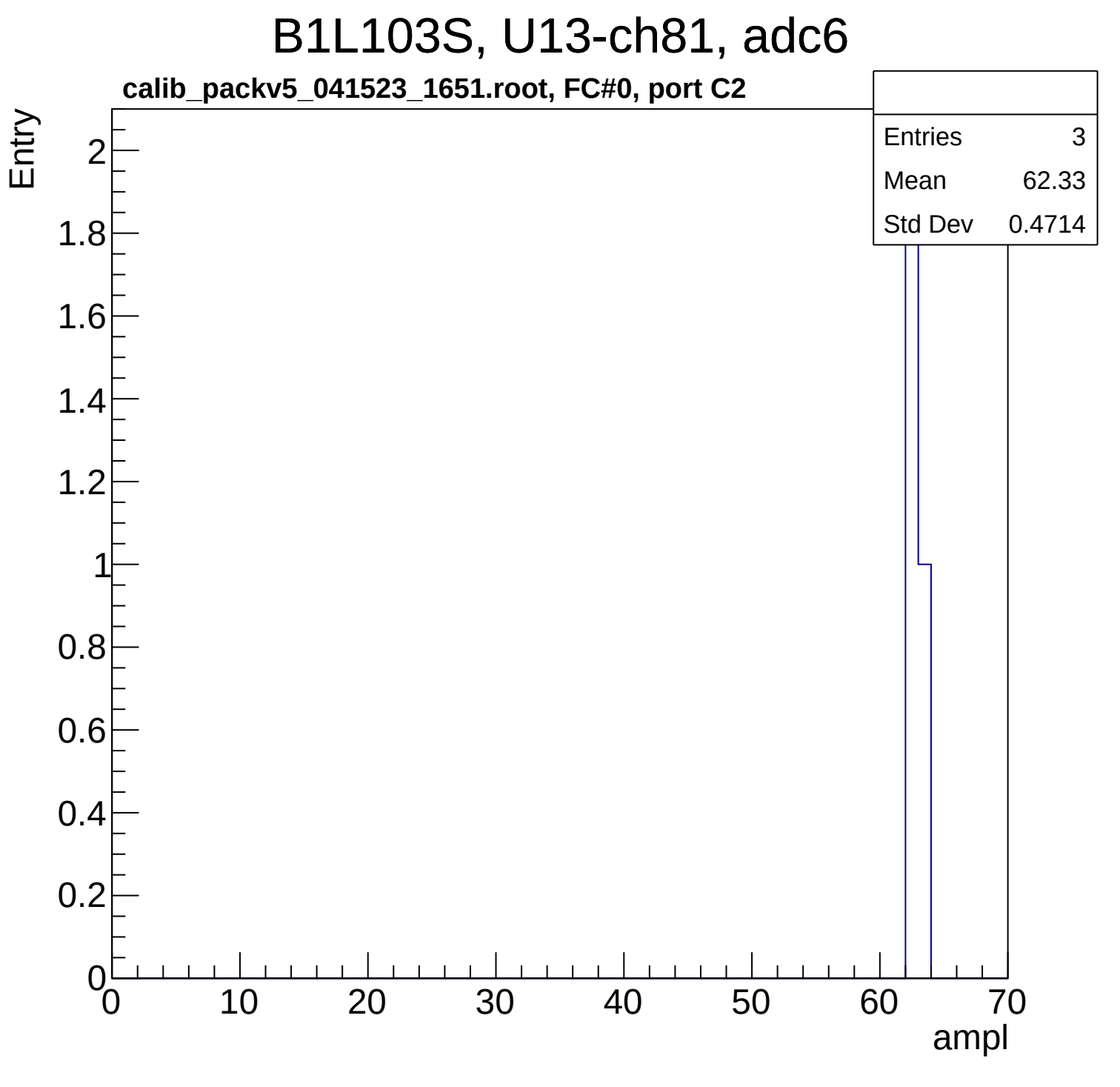
B1L103S, U13-ch81, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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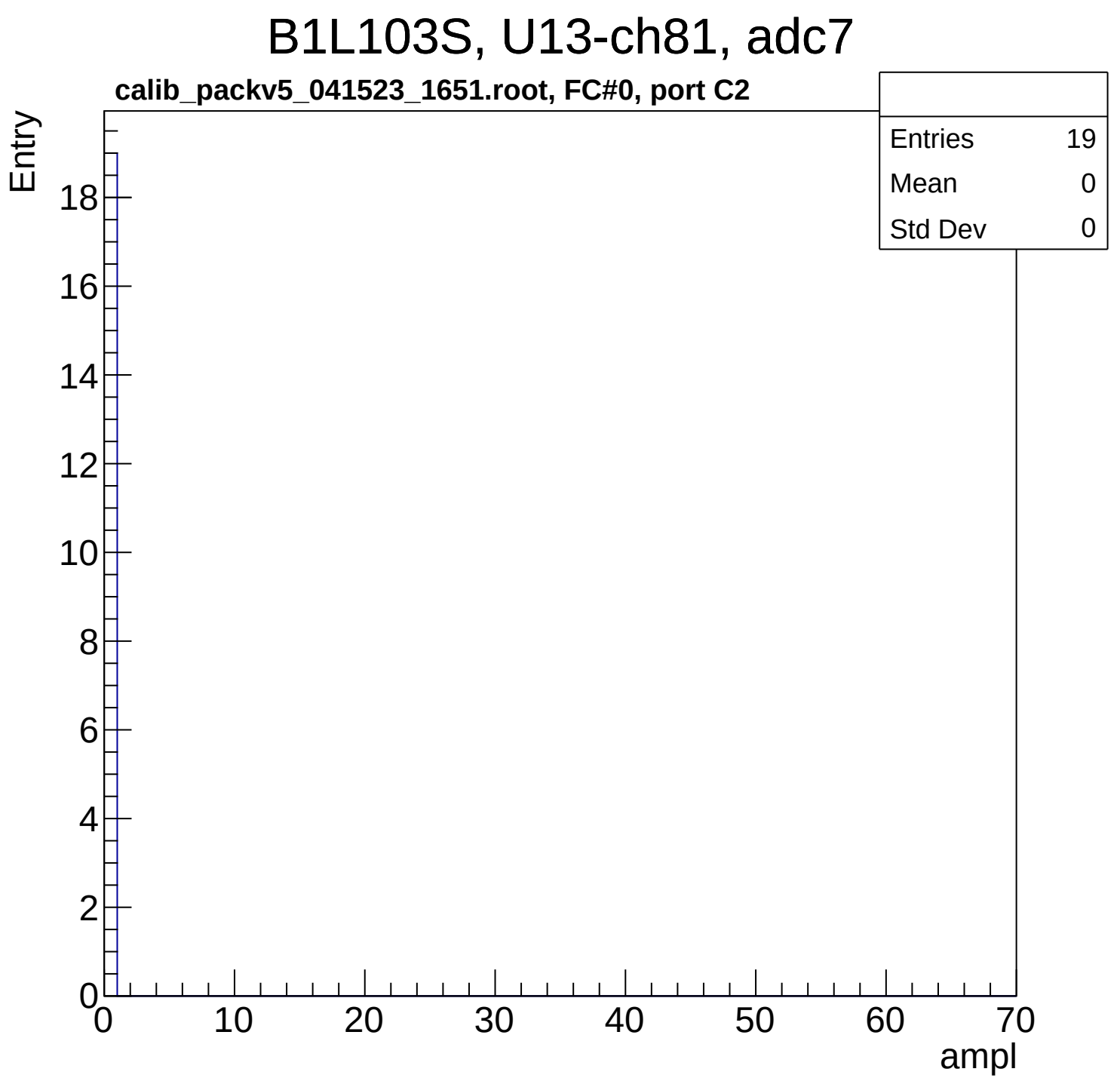
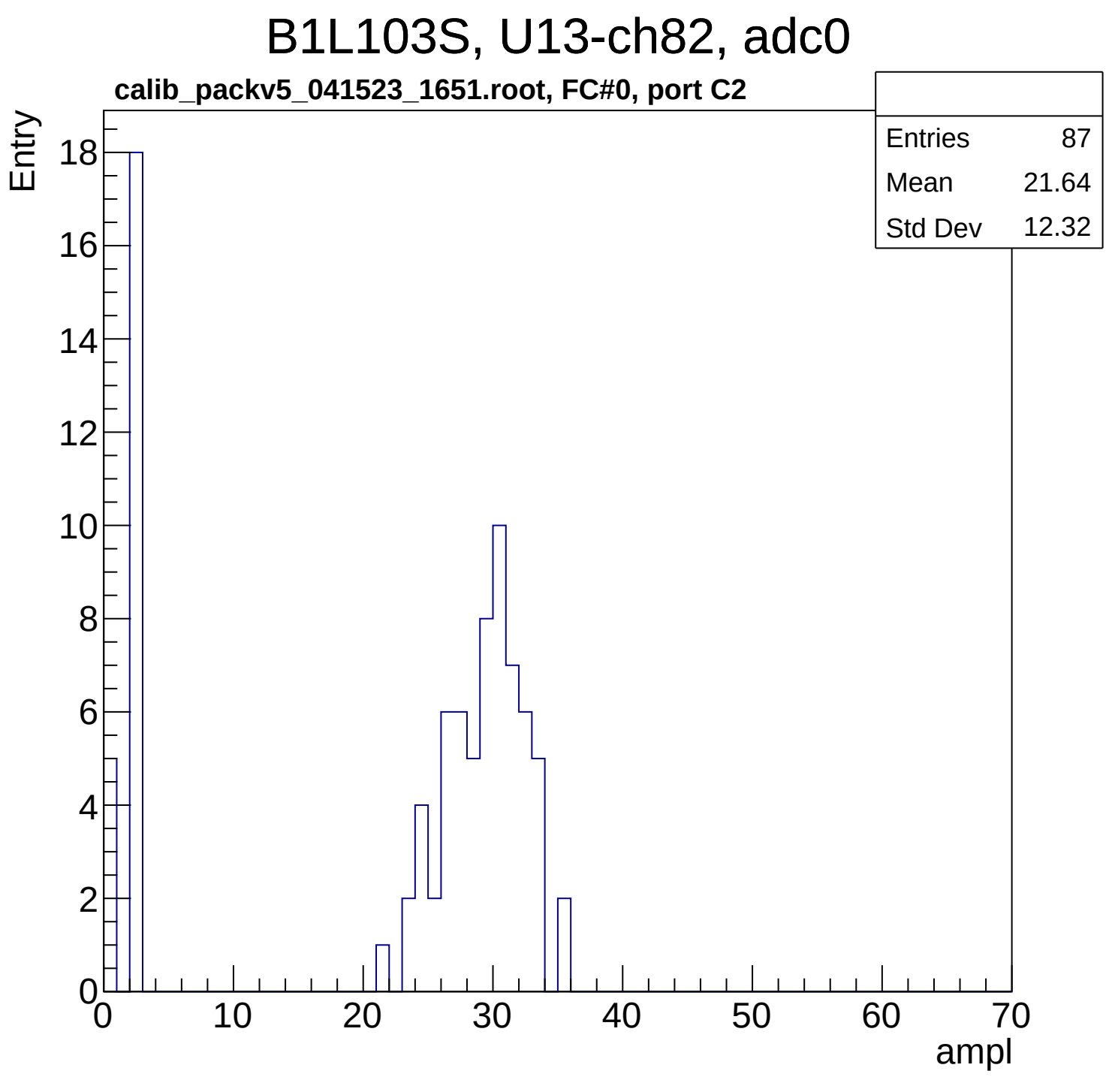

B1L103S, U13-ch81, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch82, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 21.64
Std Dev 12.32
Entry
ampl
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2
4
6
8
10
12
14
16
18
0
10
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40
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60
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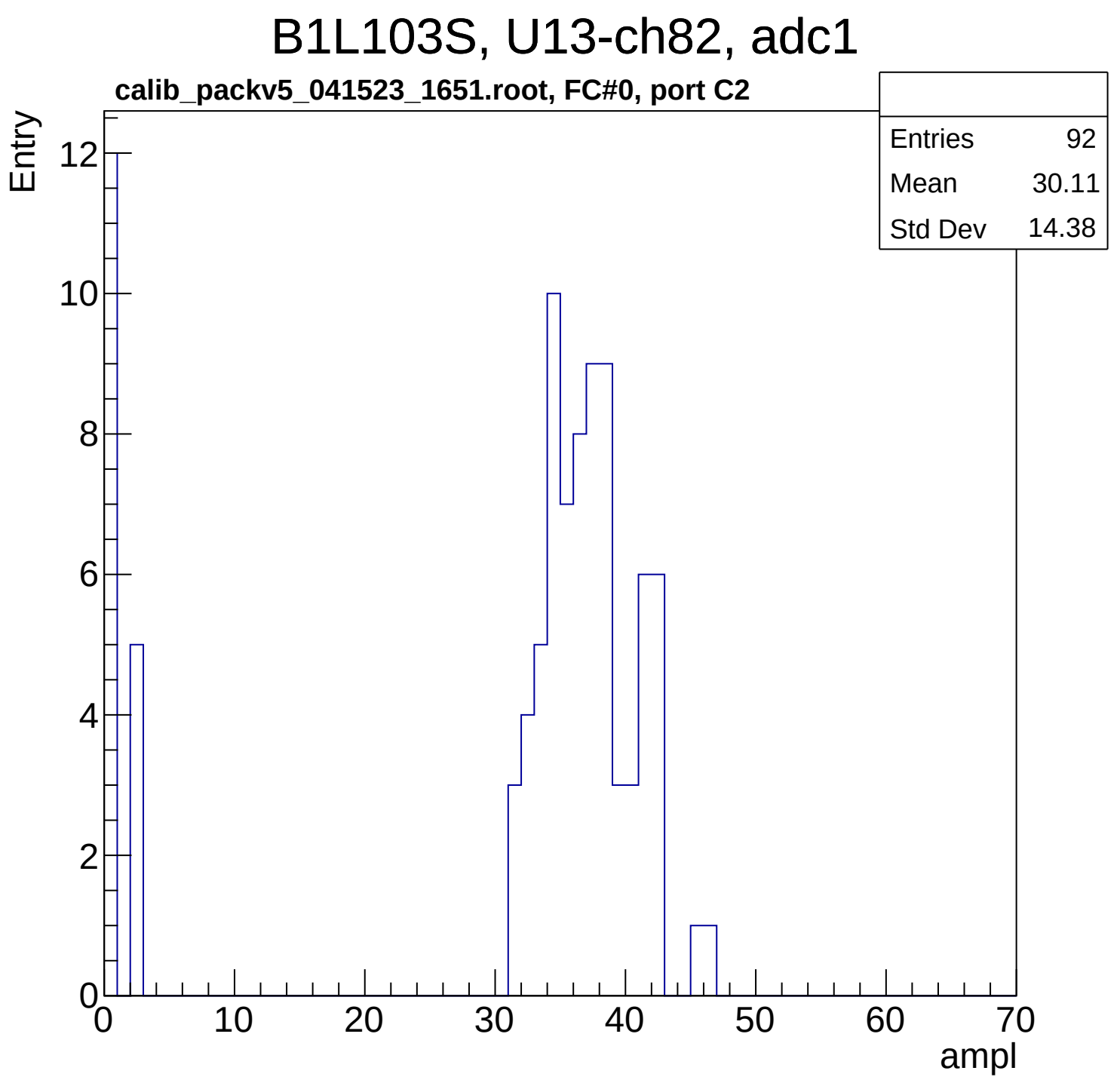
B1L103S, U13-ch82, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 30.11
Std Dev 14.38
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
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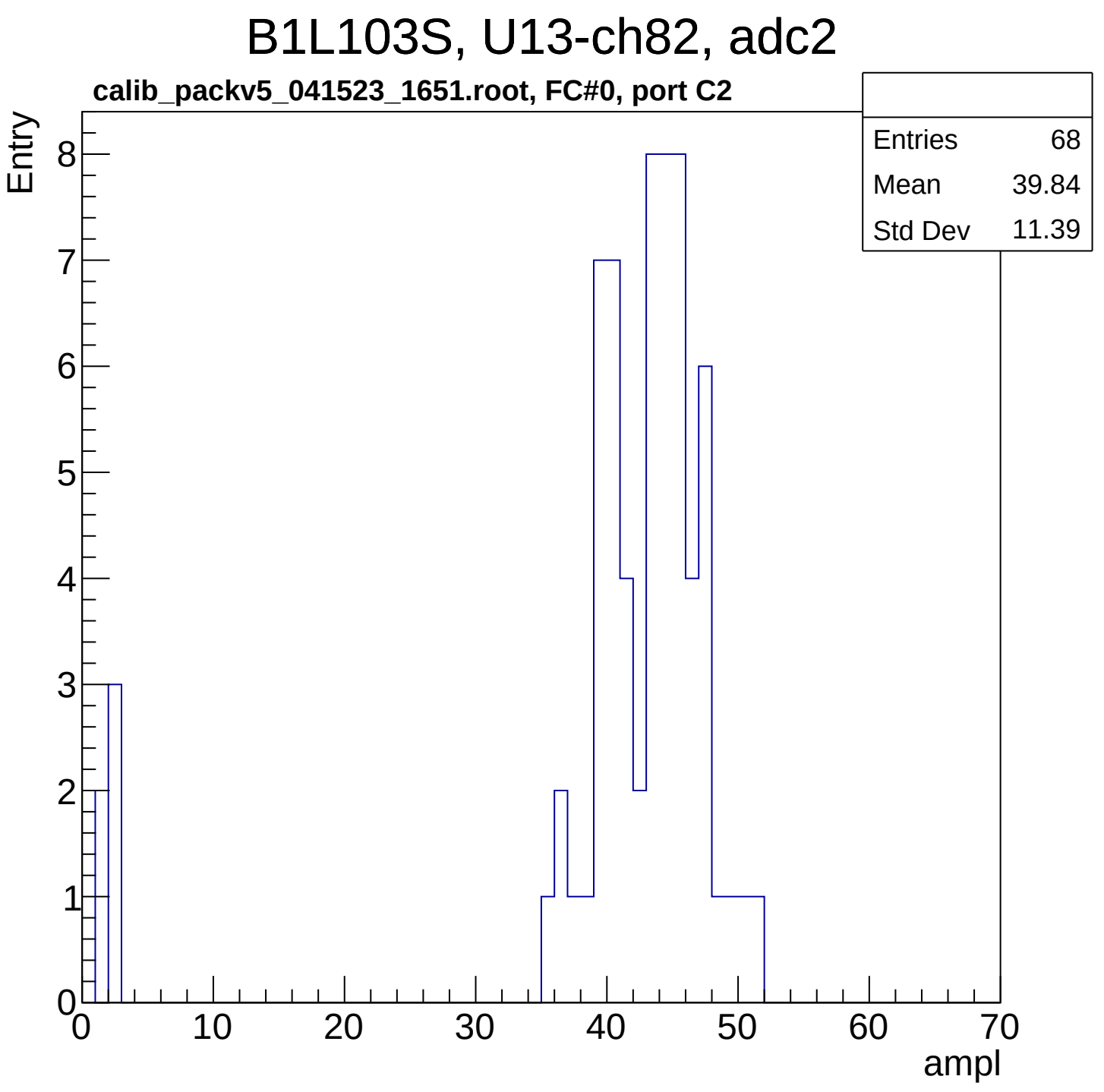
B1L103S, U13-ch82, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 39.84
Std Dev 11.39
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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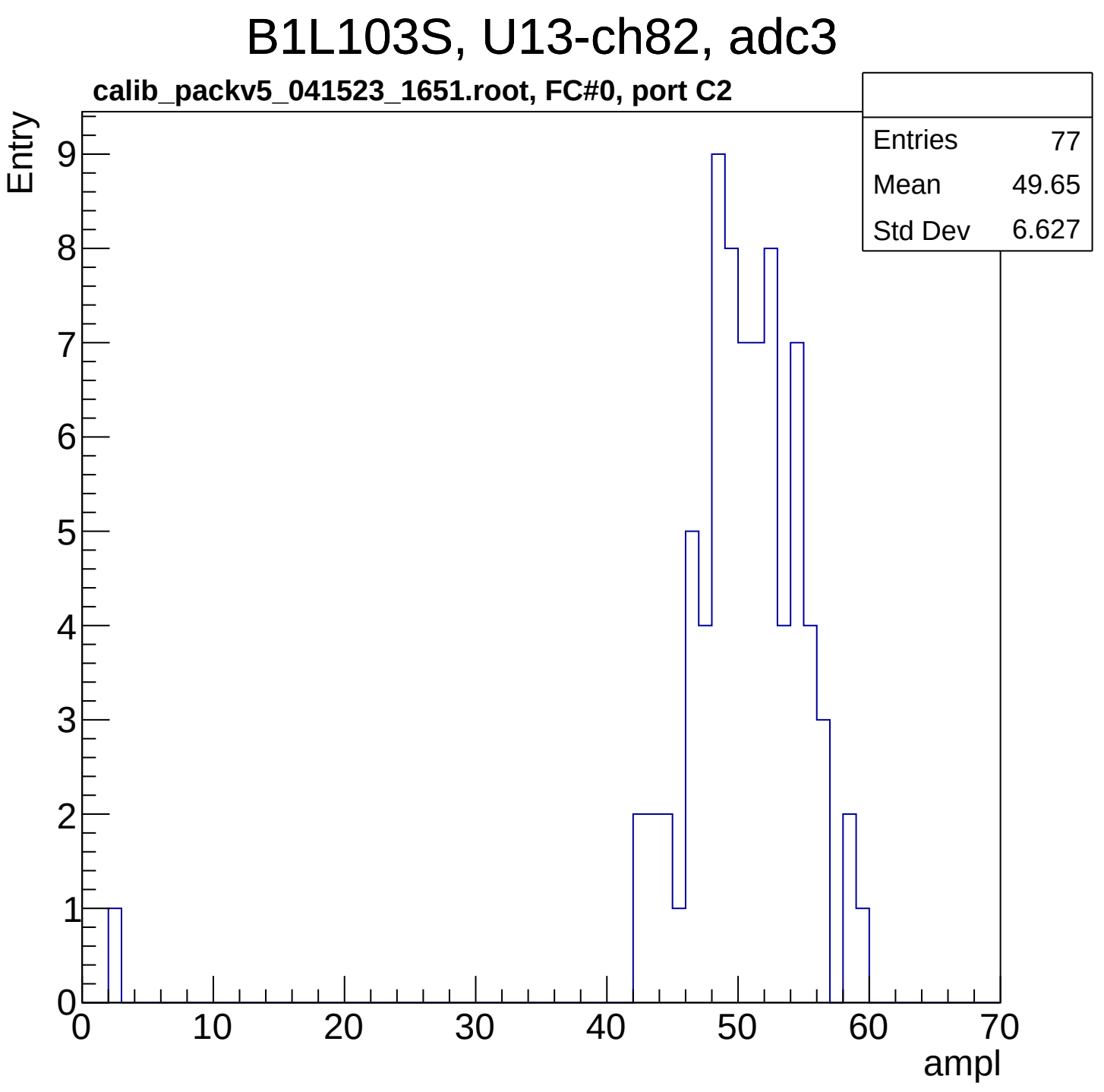
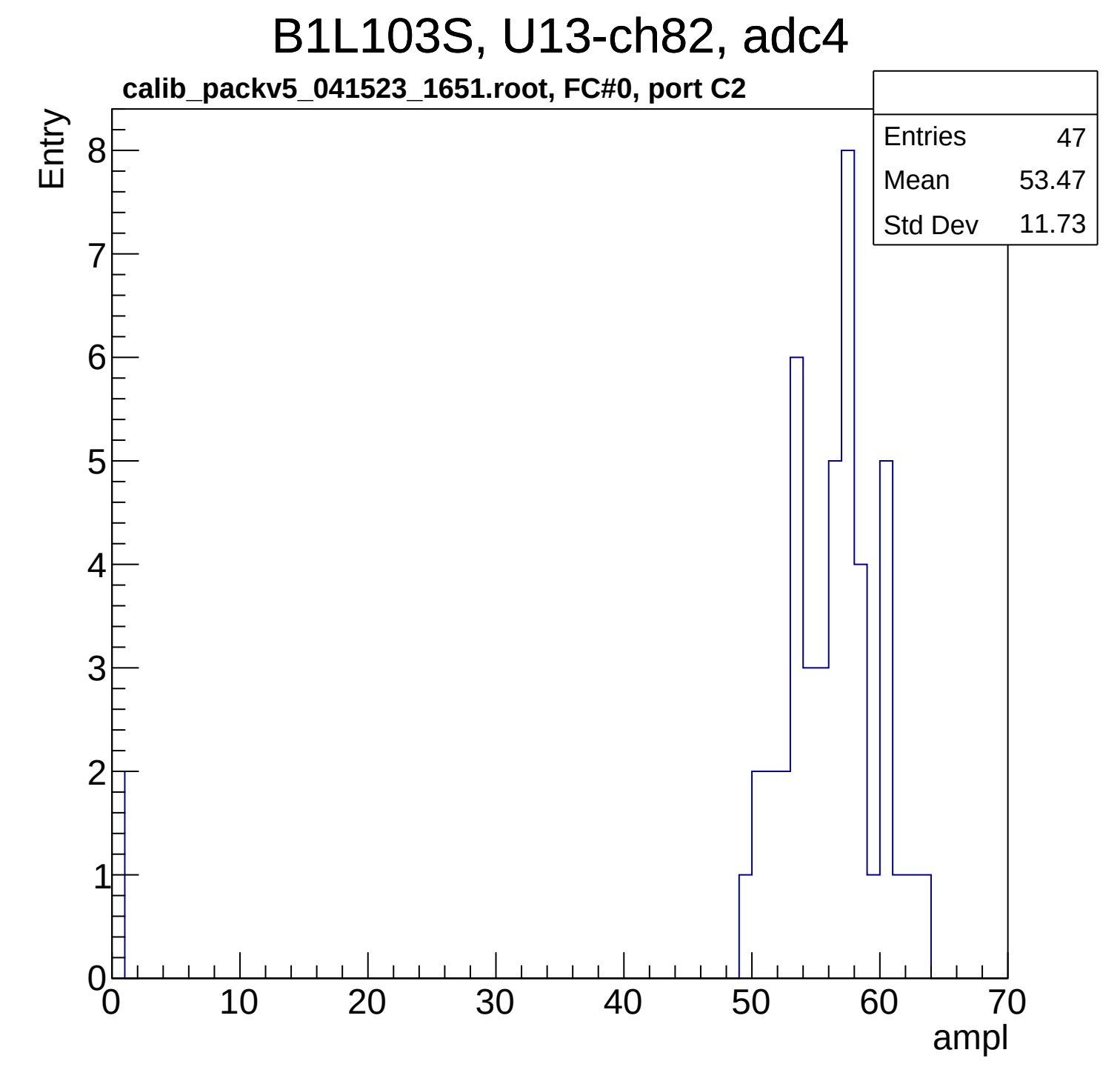
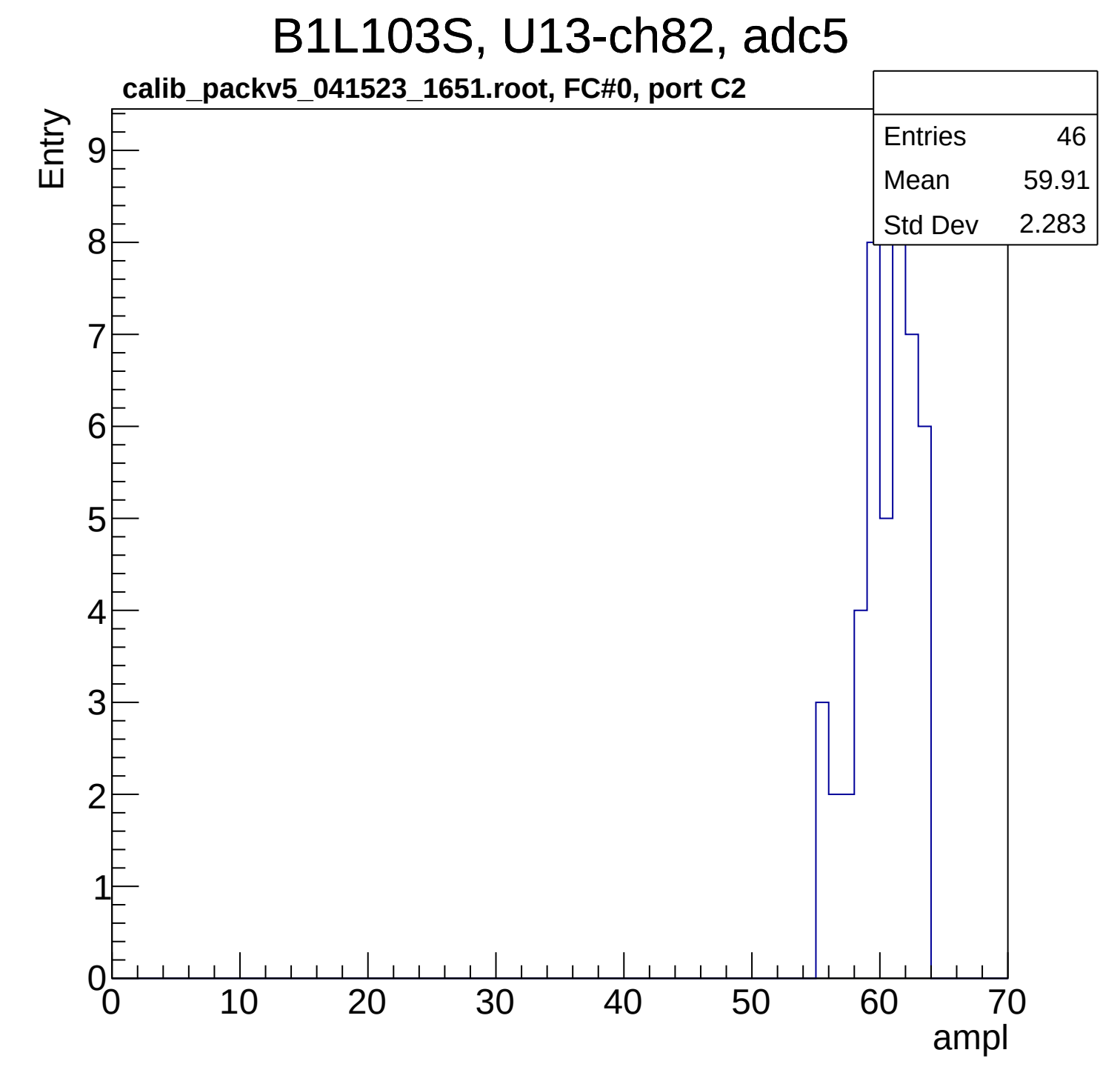
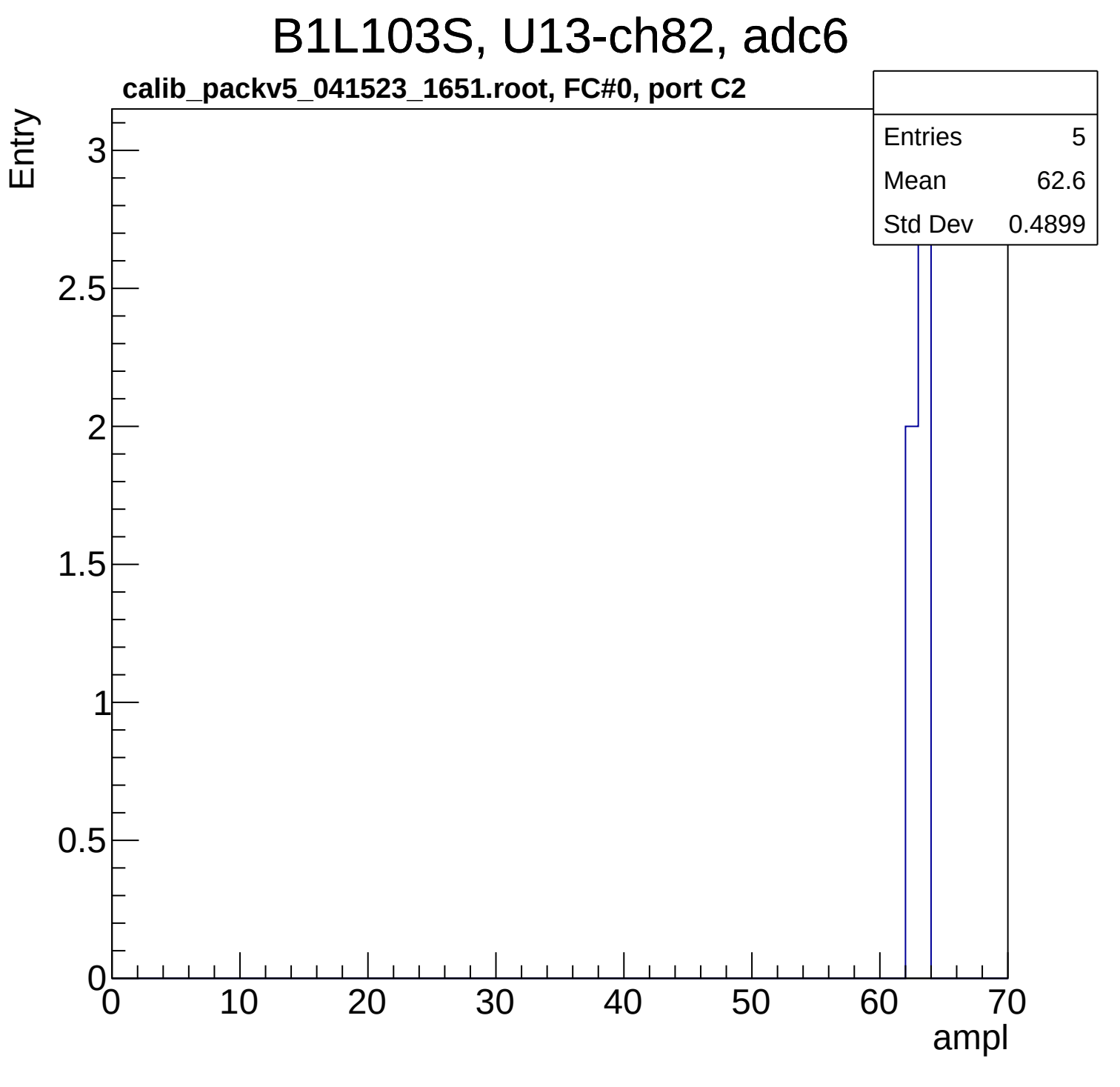

B1L103S, U13-ch82, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 49.65
Std Dev 6.627
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch82, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 53.47
Std Dev 11.73
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch82, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 59.91
Std Dev 2.283
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch82, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.6
Std Dev 0.4899
Entry
ampl
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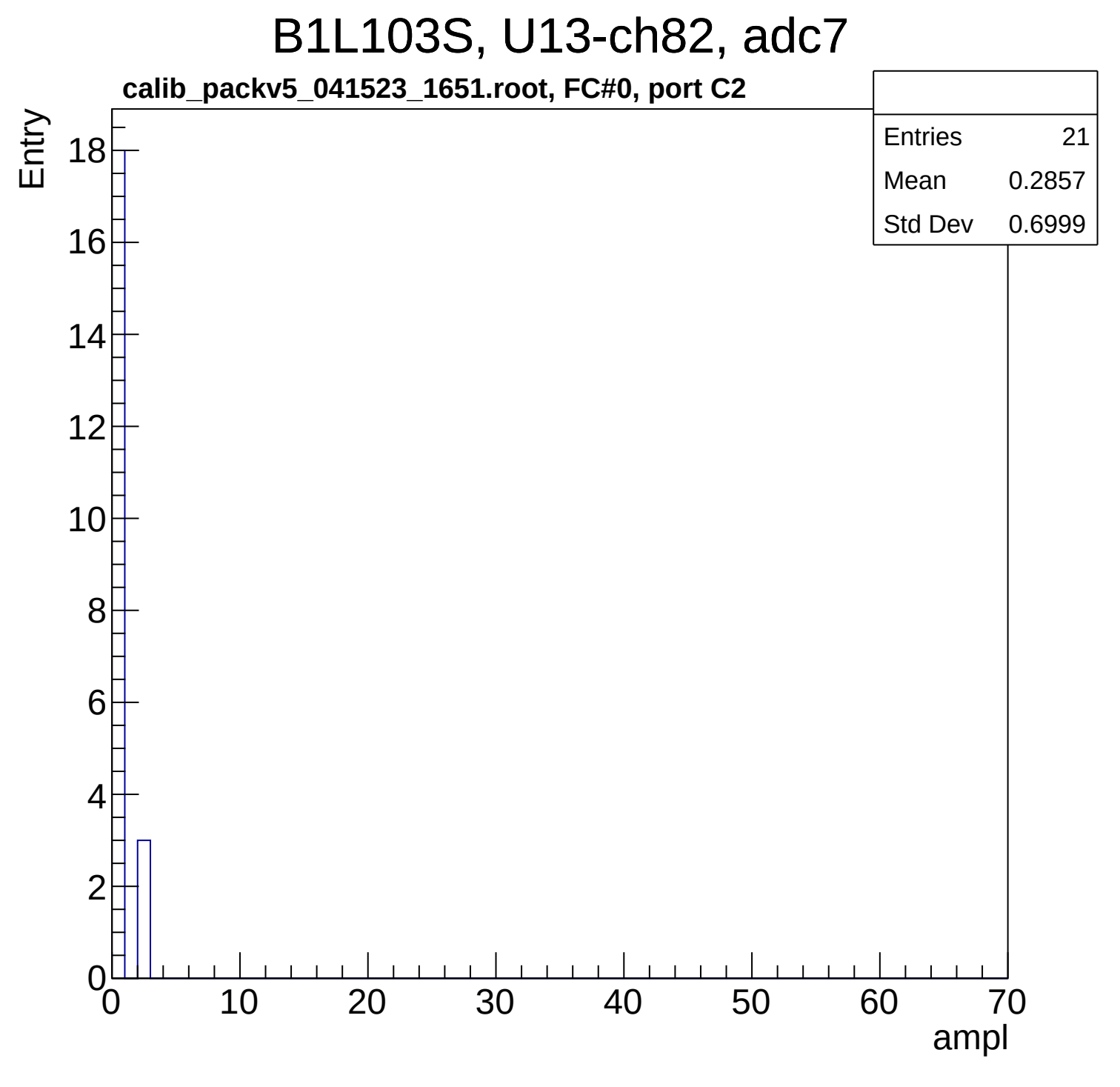
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U13-ch82, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 0.2857
Std Dev 0.6999
Entry
ampl
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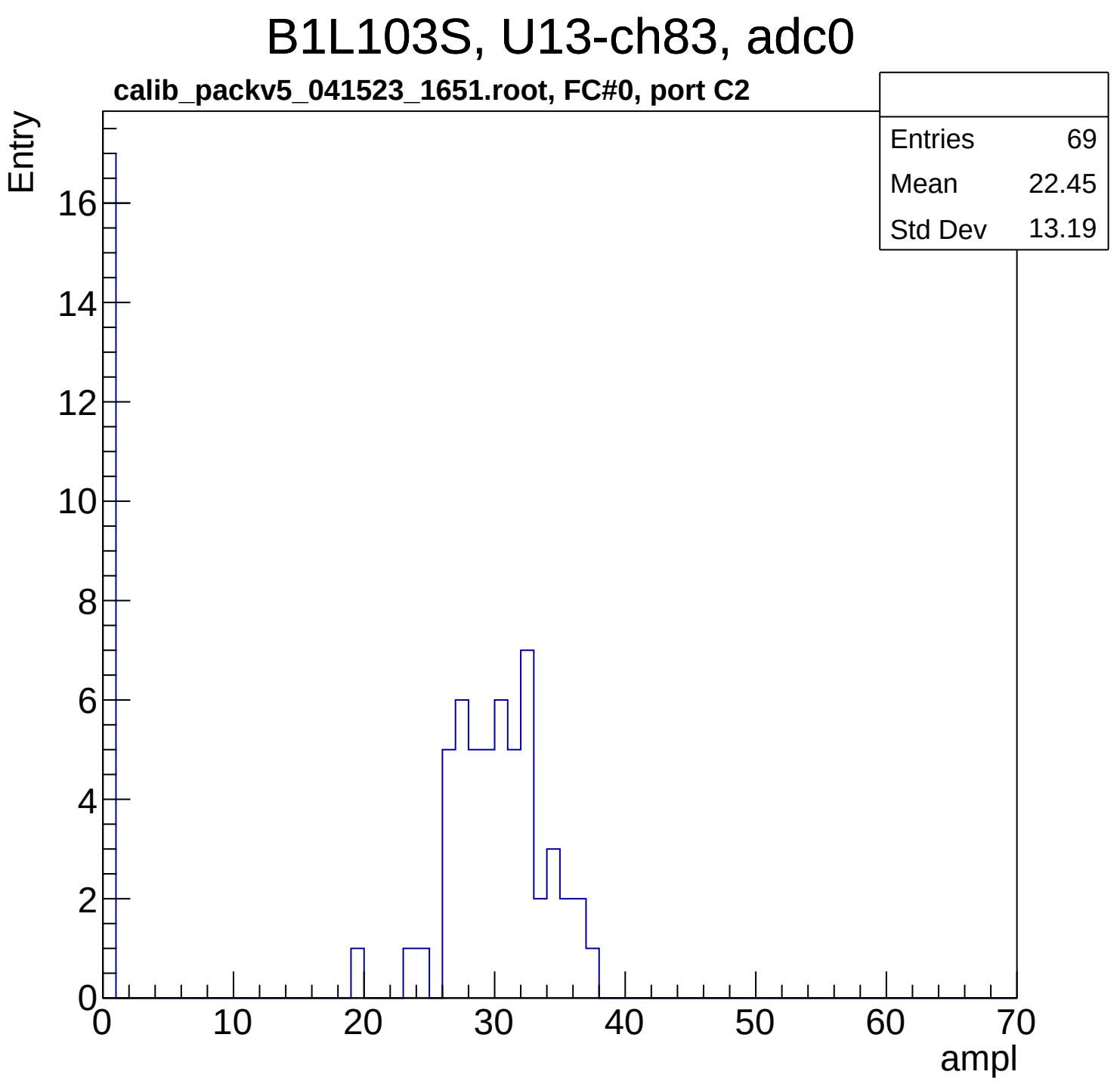
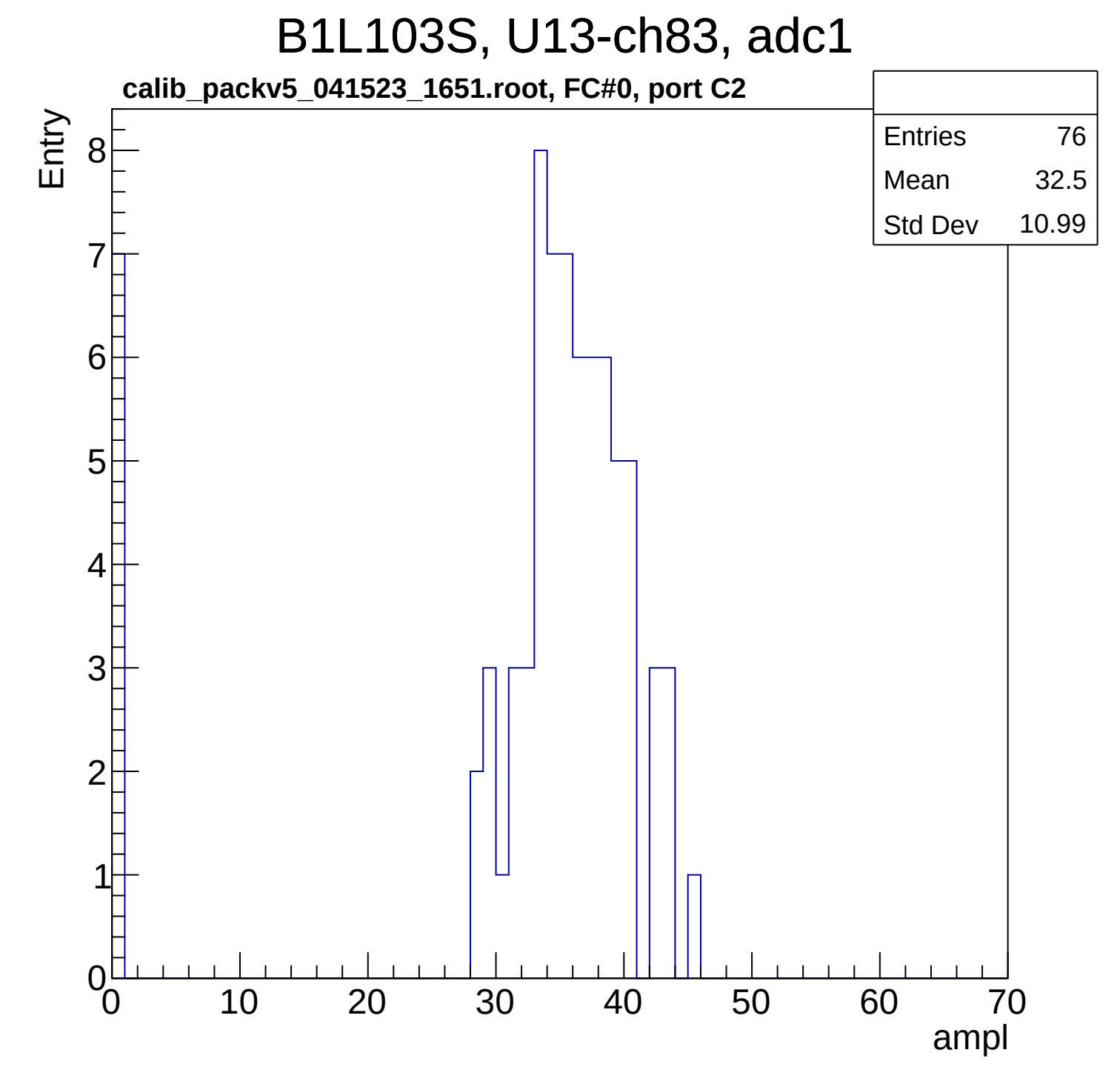
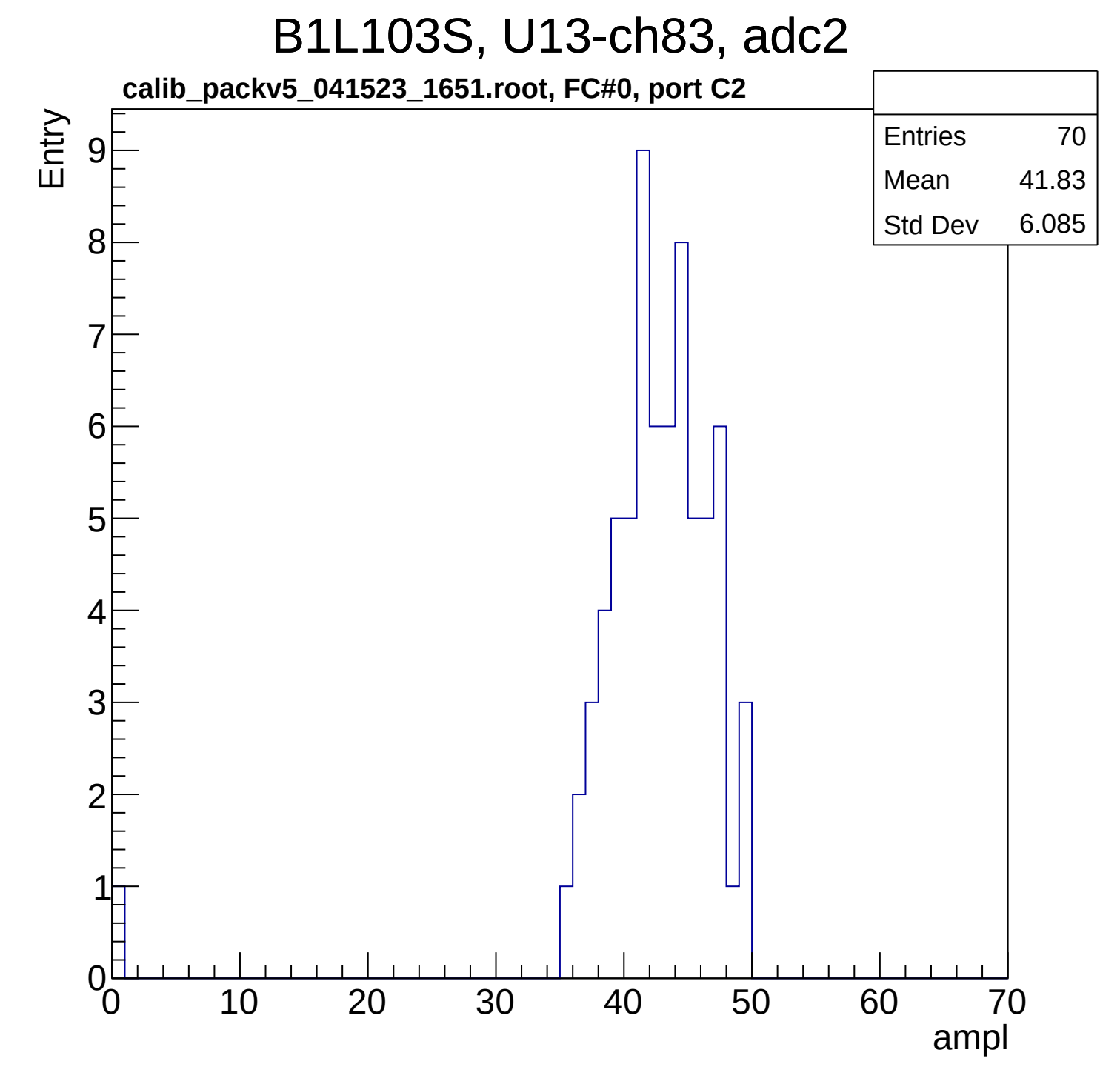
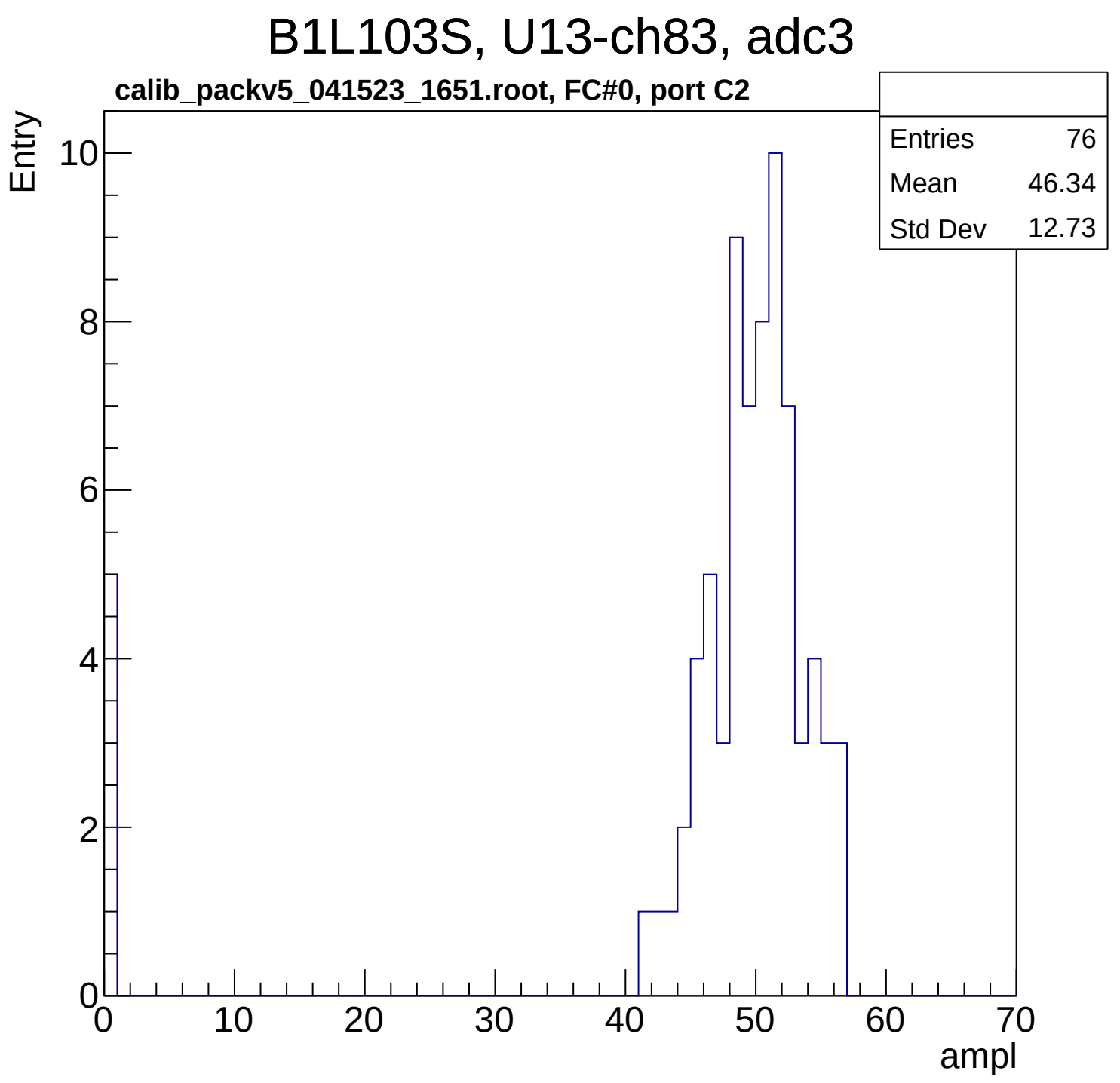
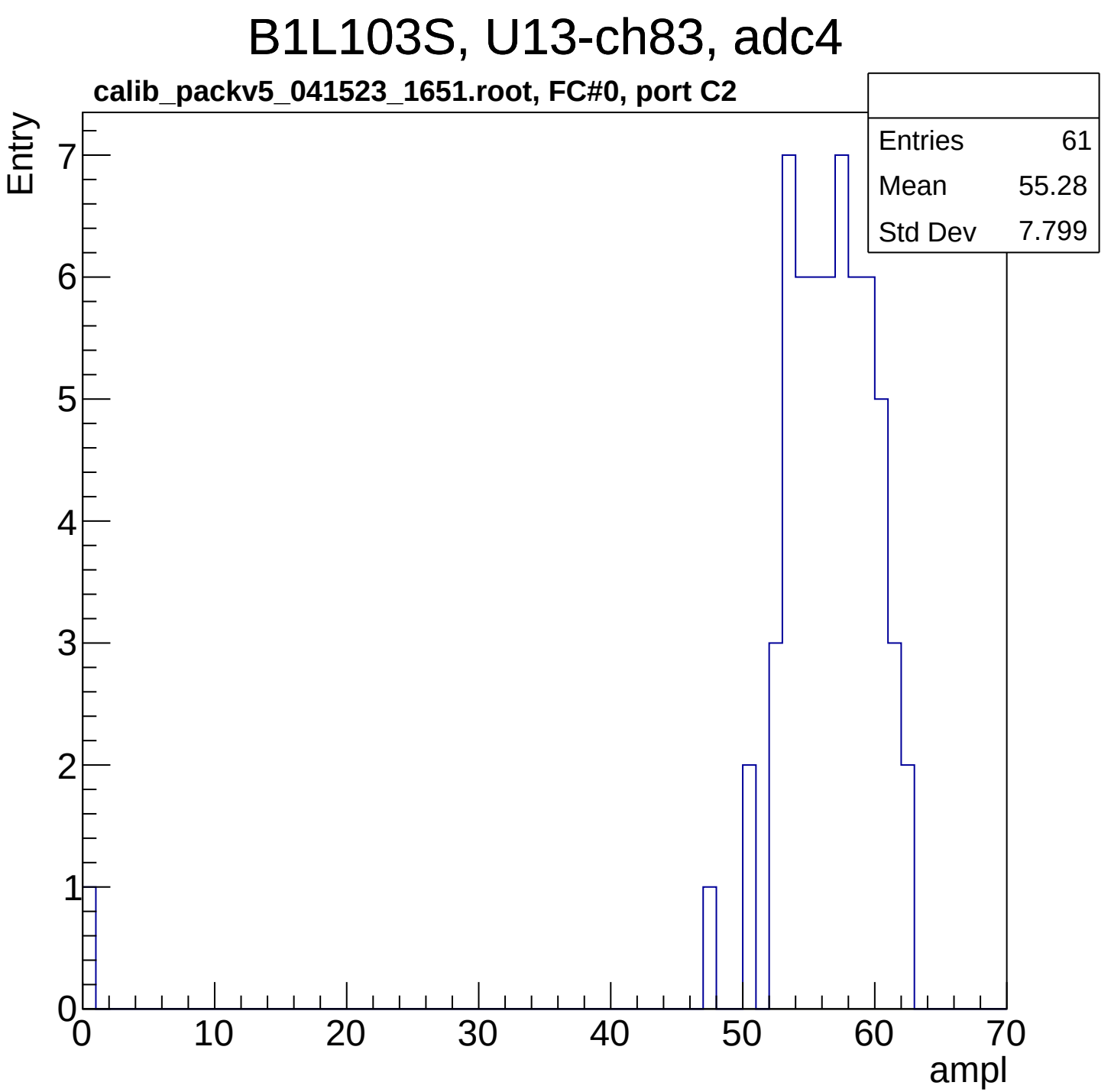
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

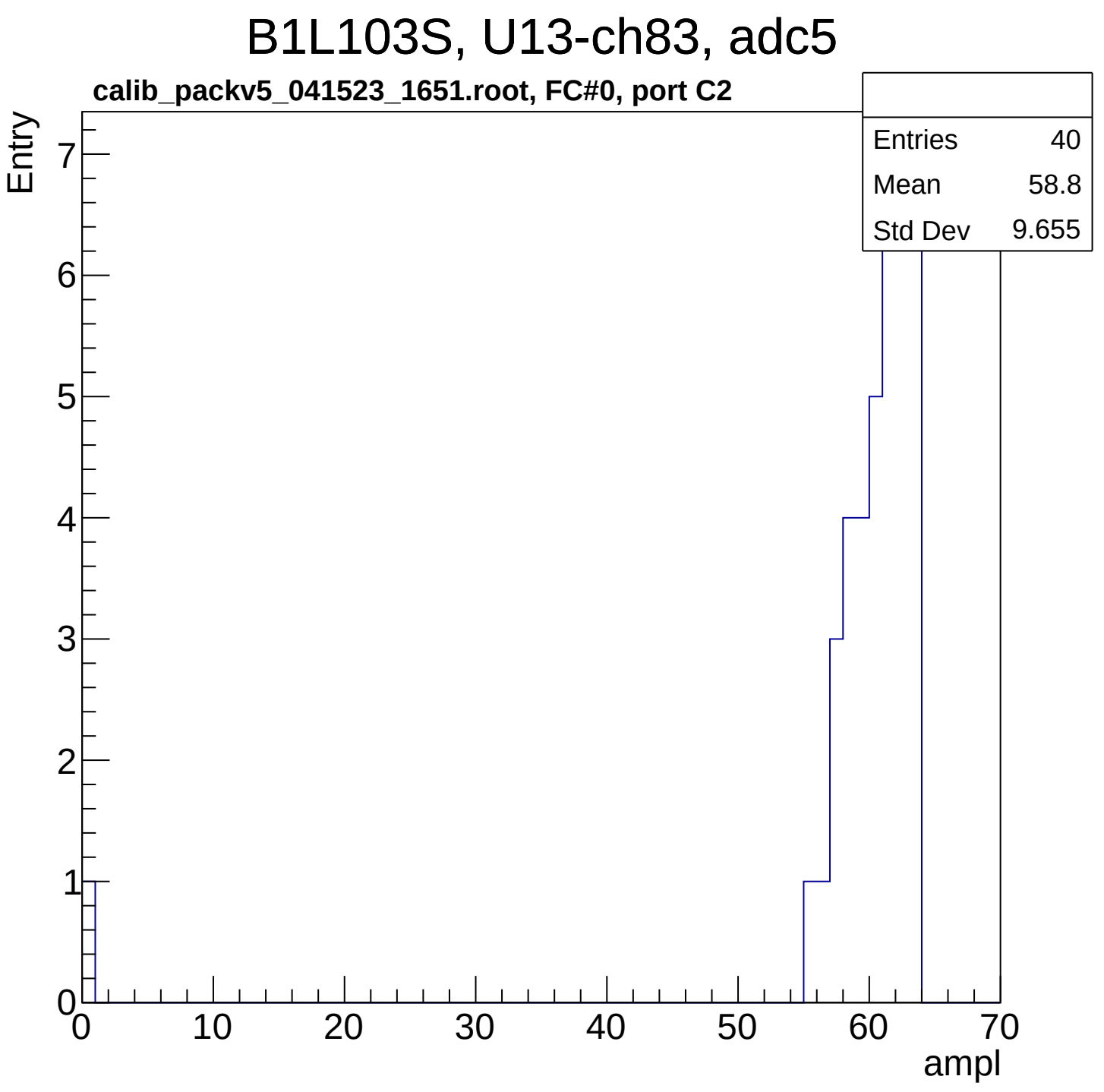

B1L103S, U13-ch83, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 22.45
Std Dev 13.19
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

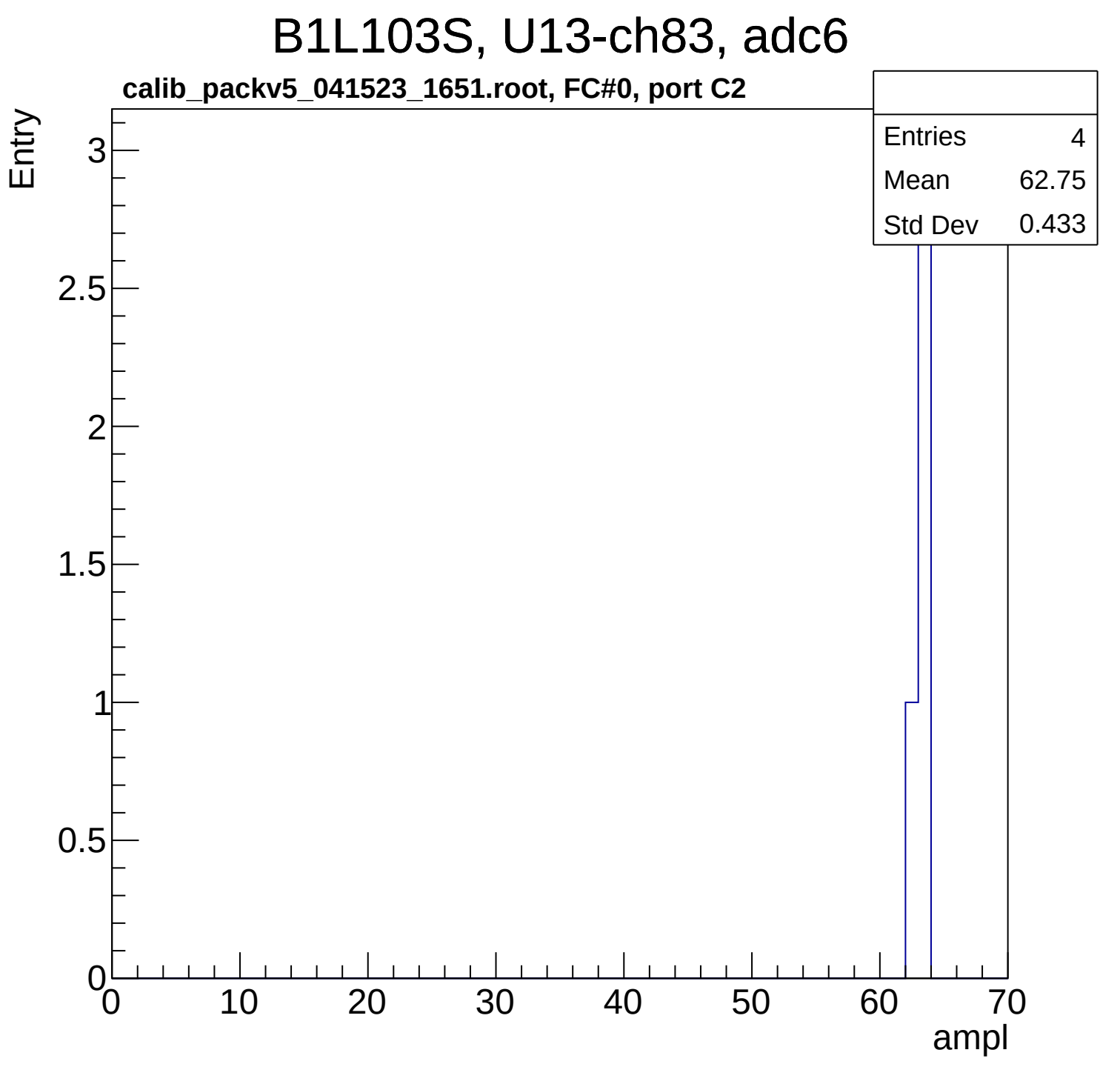

B1L103S, U13-ch83, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 32.5
Std Dev 10.99
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch83, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 41.83
Std Dev 6.085
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch83, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 46.34
Std Dev 12.73
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch83, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 55.28
Std Dev 7.799
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch83, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 58.8
Std Dev 9.655
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch83, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.75
Std Dev 0.433
Entry
ampl
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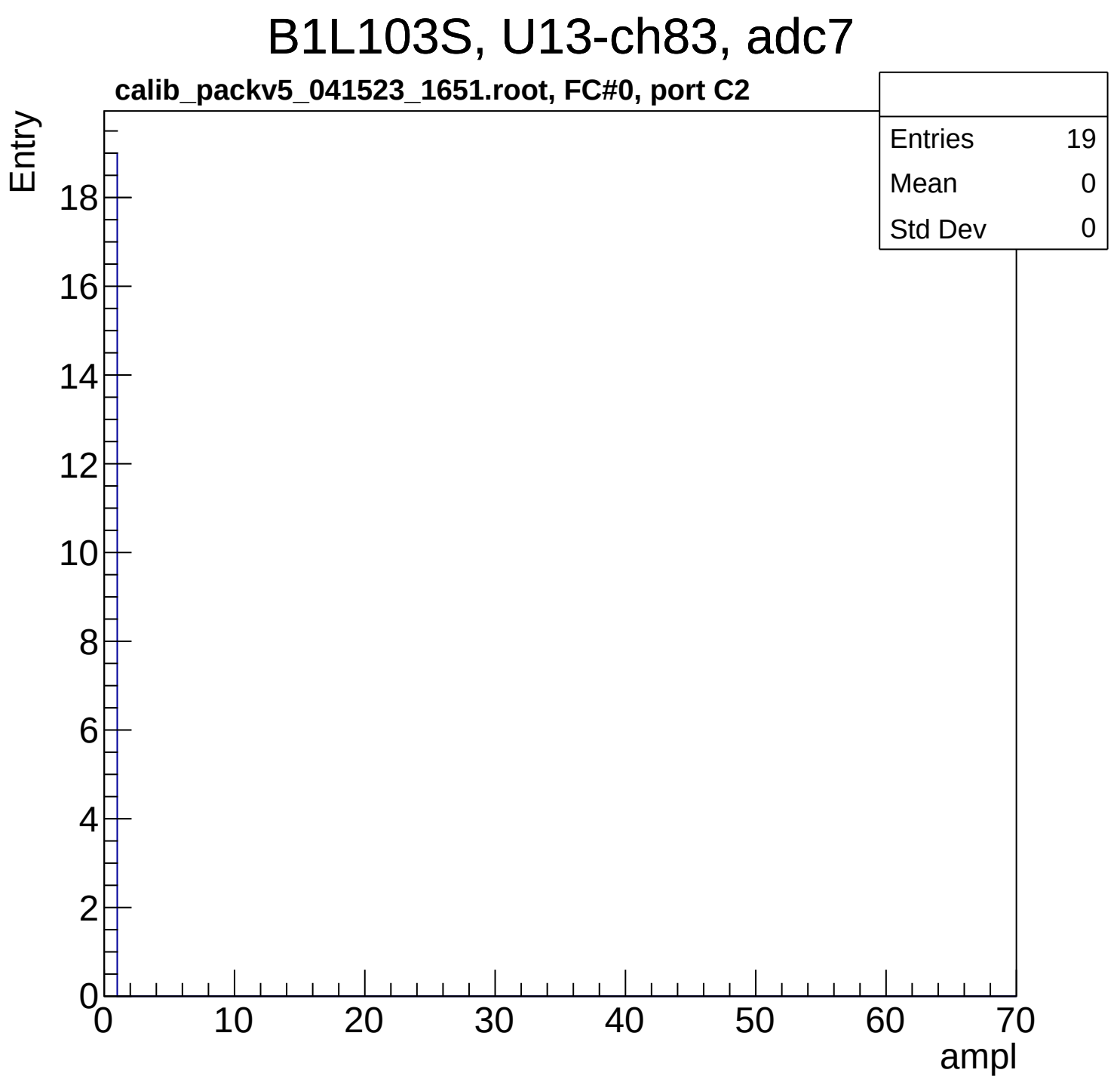
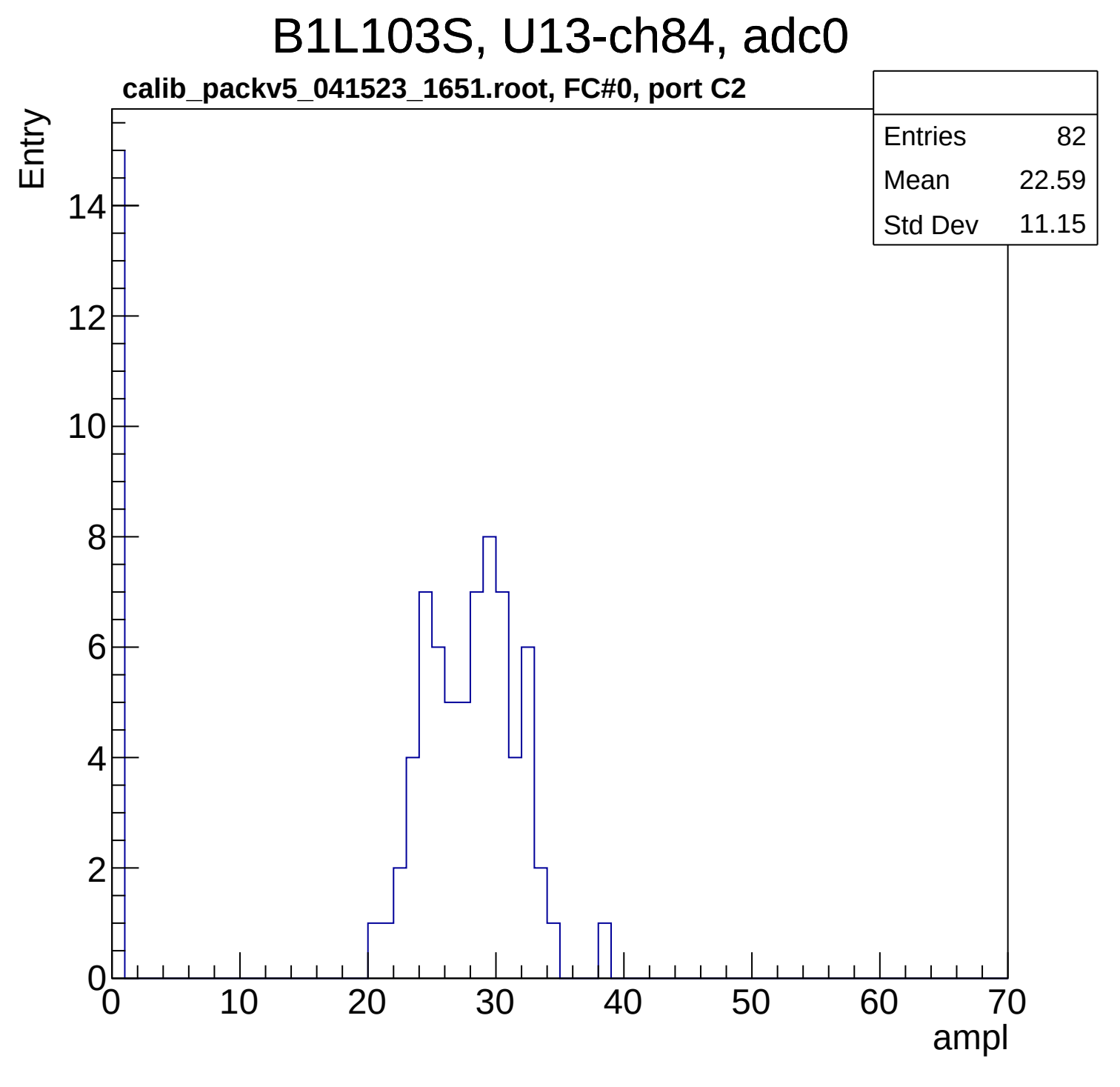
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U13-ch83, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch84, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 22.59
Std Dev 11.15
Entry
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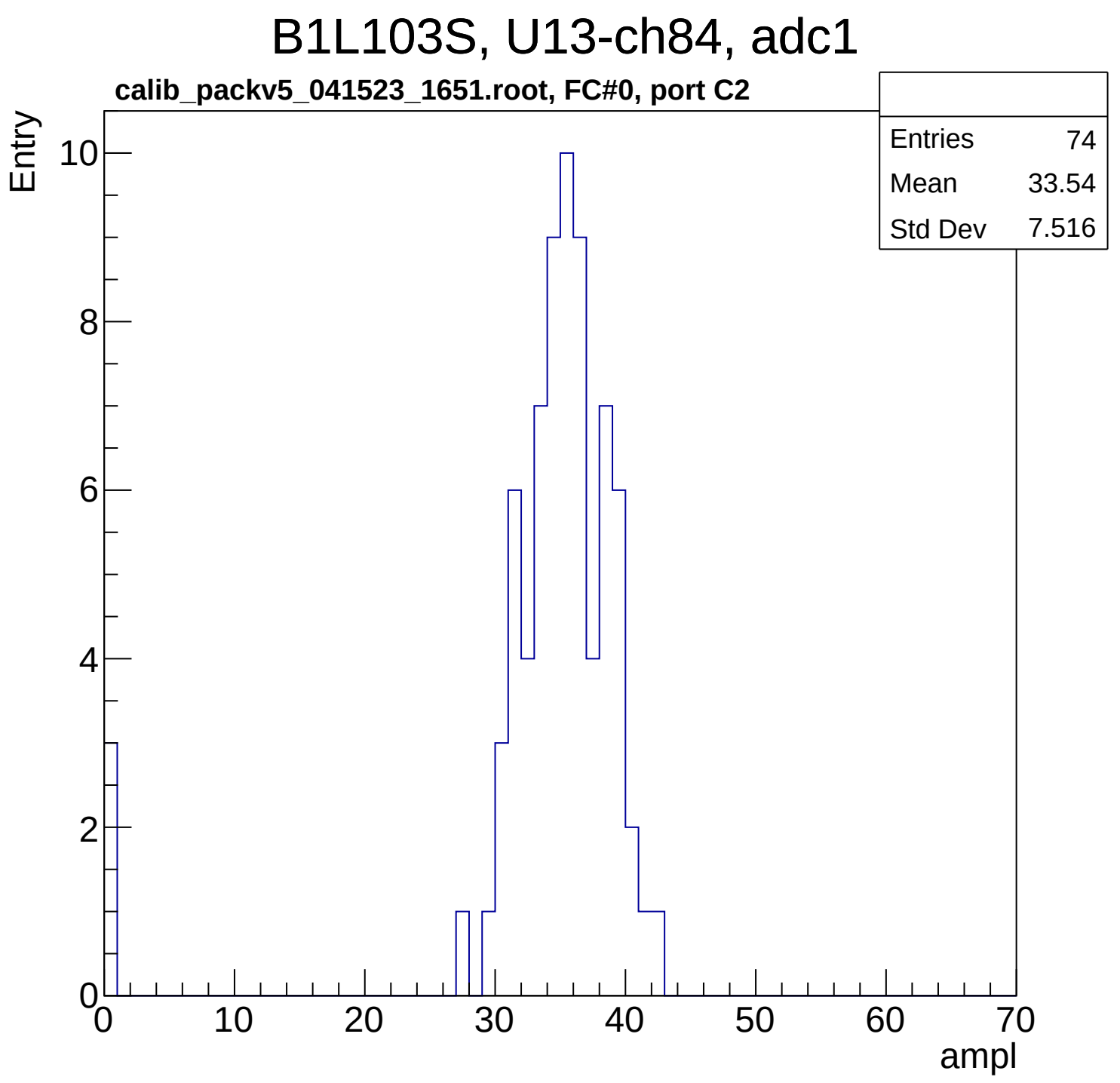
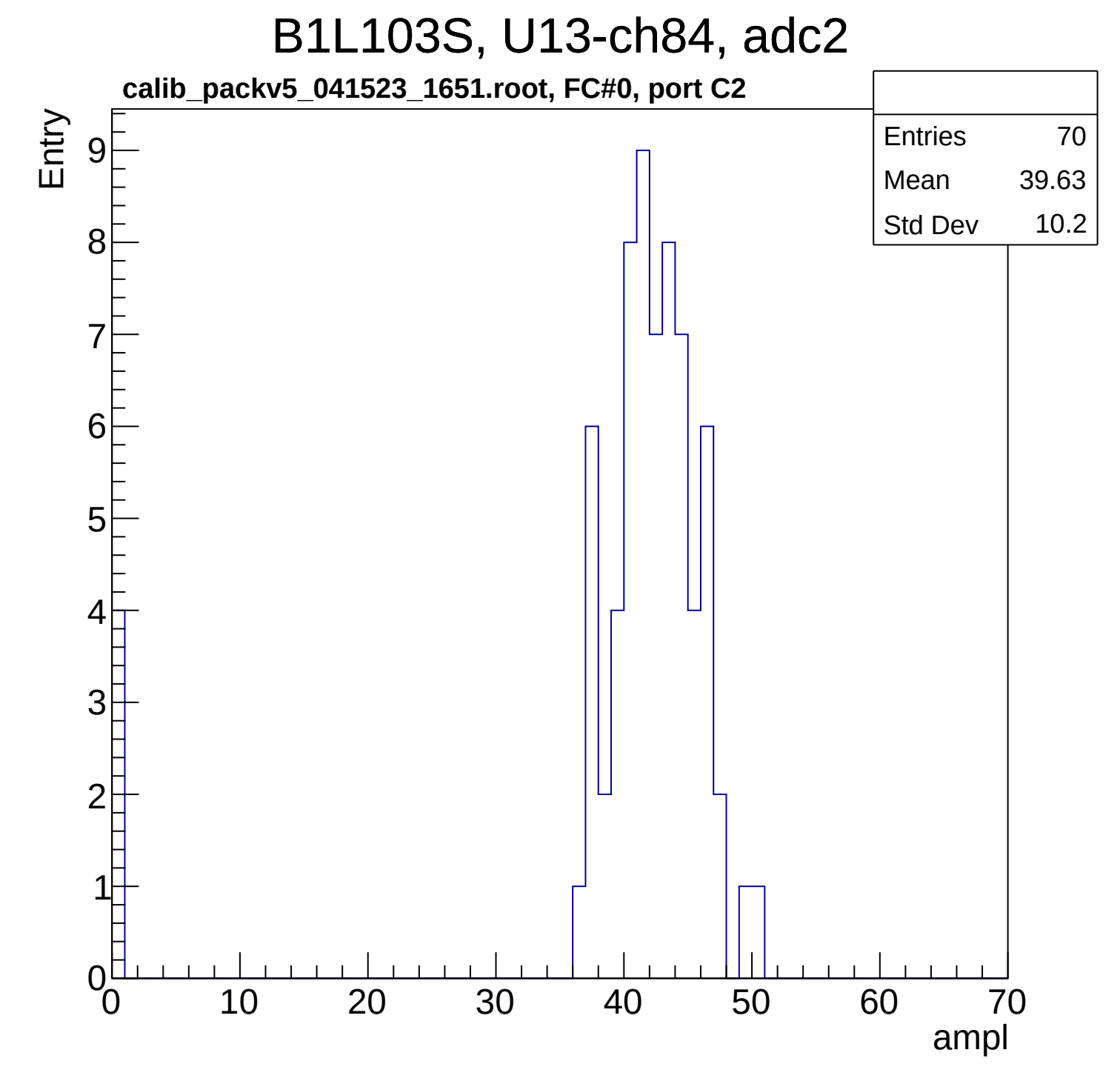
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch84, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 33.54
Std Dev 7.516
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch84, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 39.63
Std Dev 10.2
Entry
ampl
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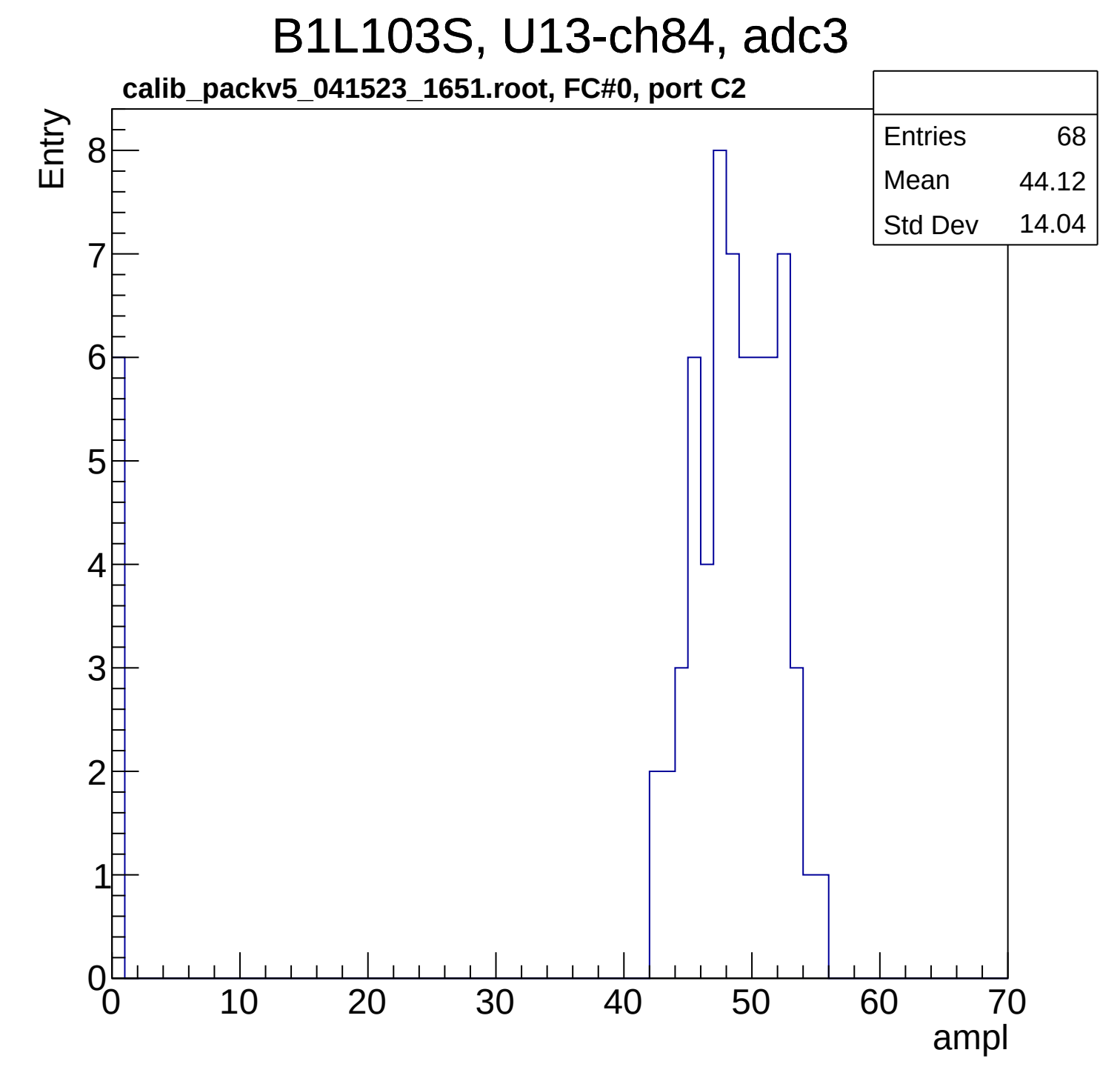
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch84, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 44.12
Std Dev 14.04
Entry
ampl
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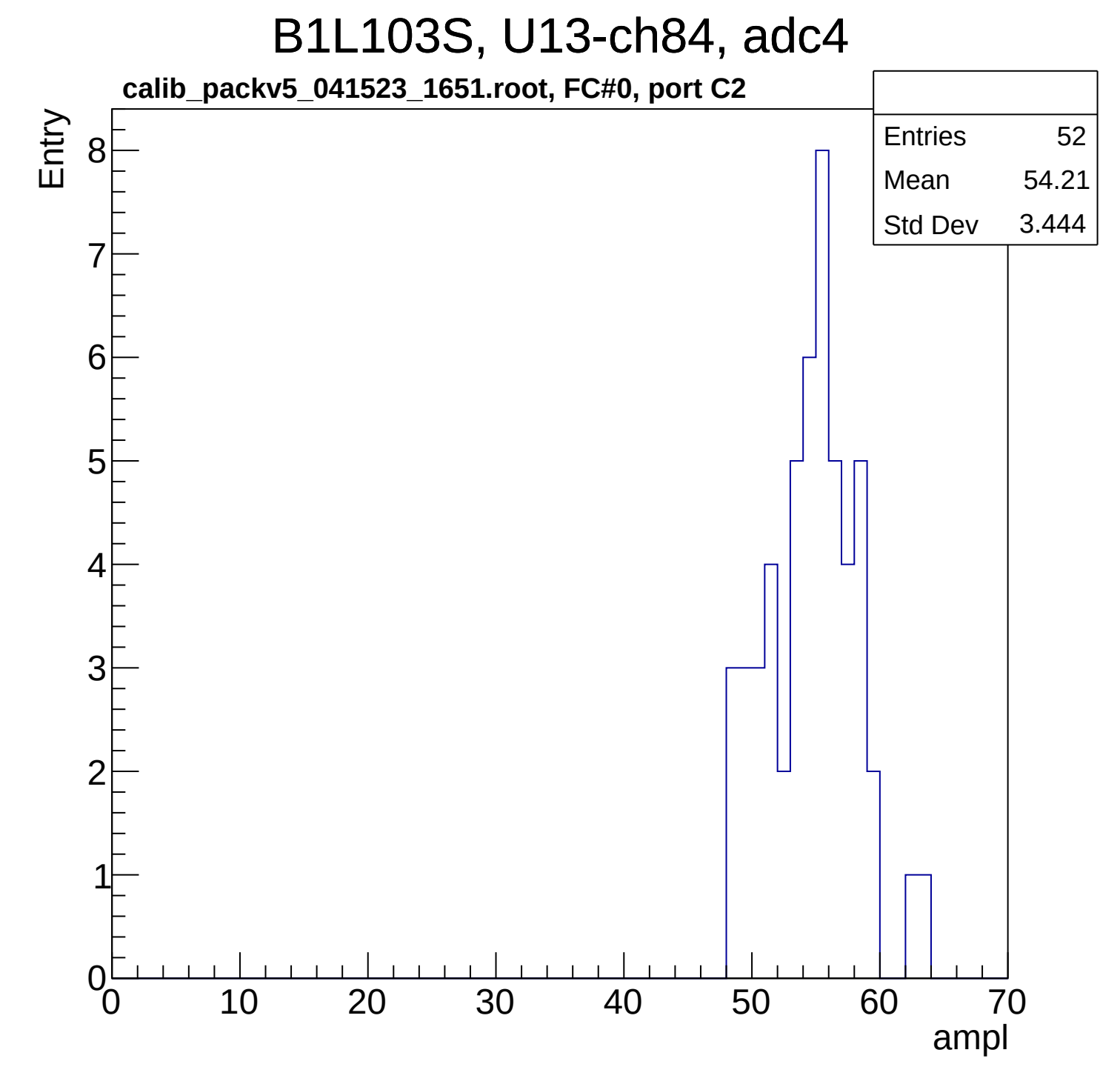
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch84, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 54.21
Std Dev 3.444
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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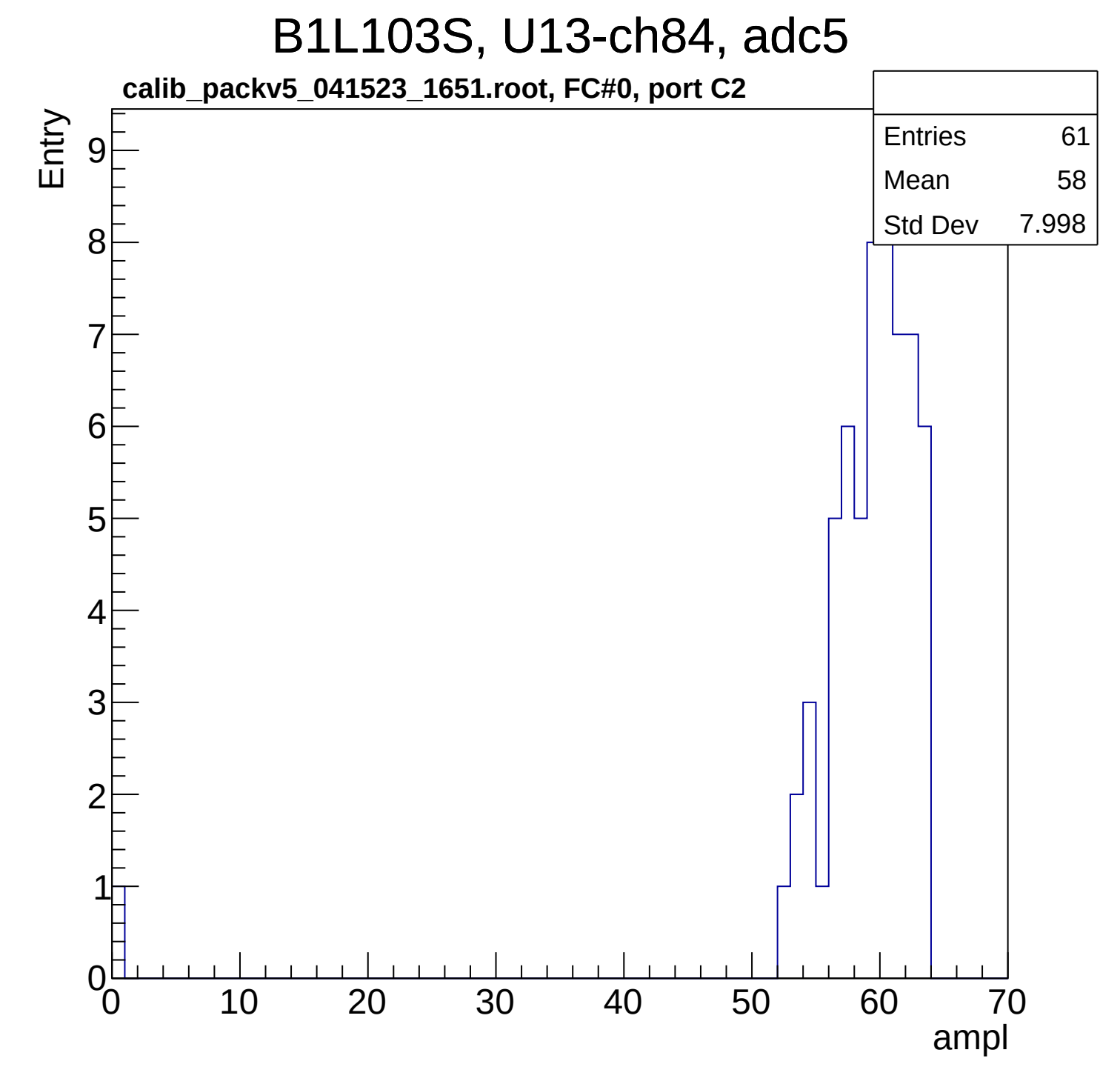
B1L103S, U13-ch84, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 58
Std Dev 7.998
Entry
ampl
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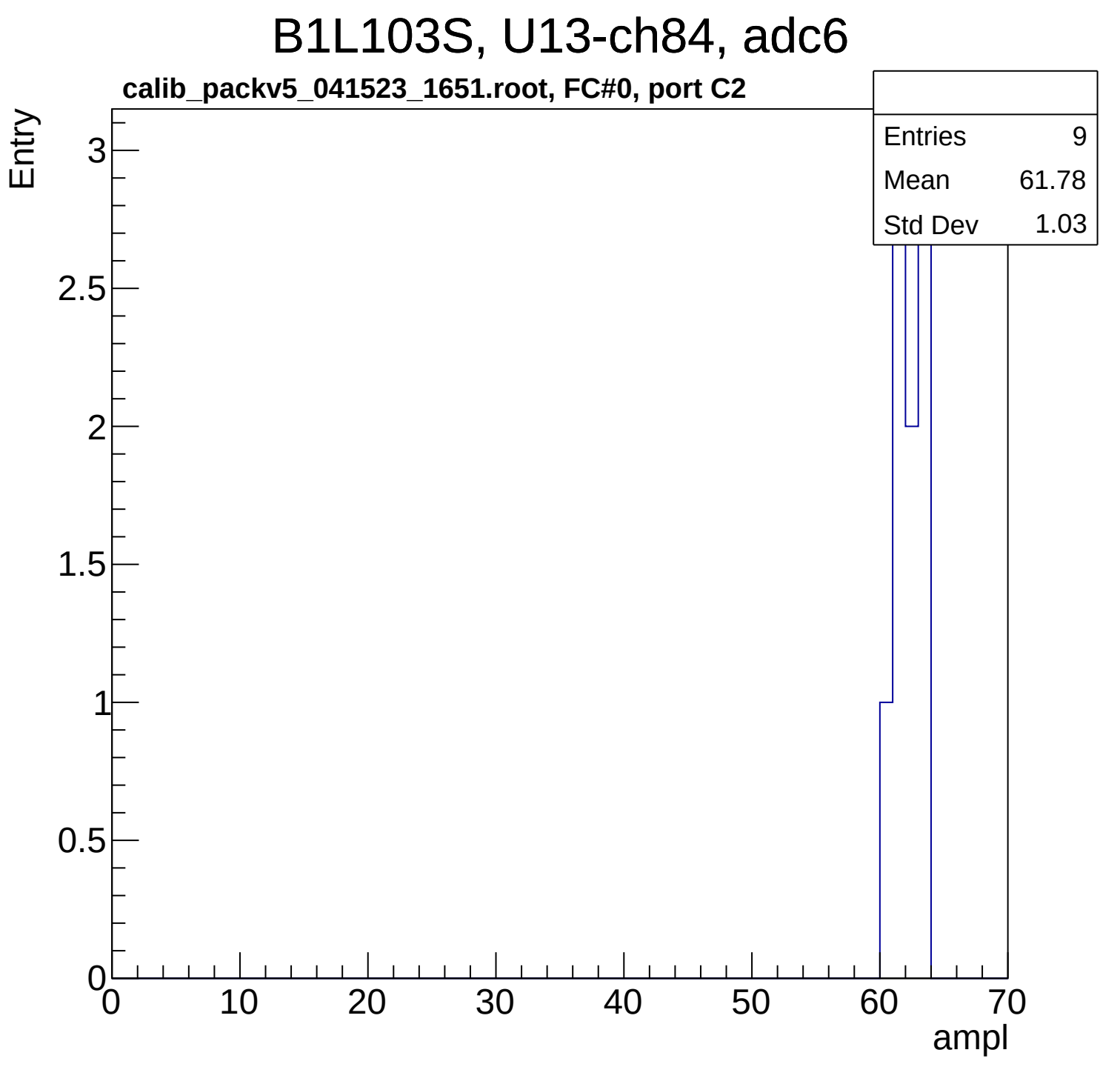
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U13-ch84, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.78
Std Dev 1.03
Entry
ampl
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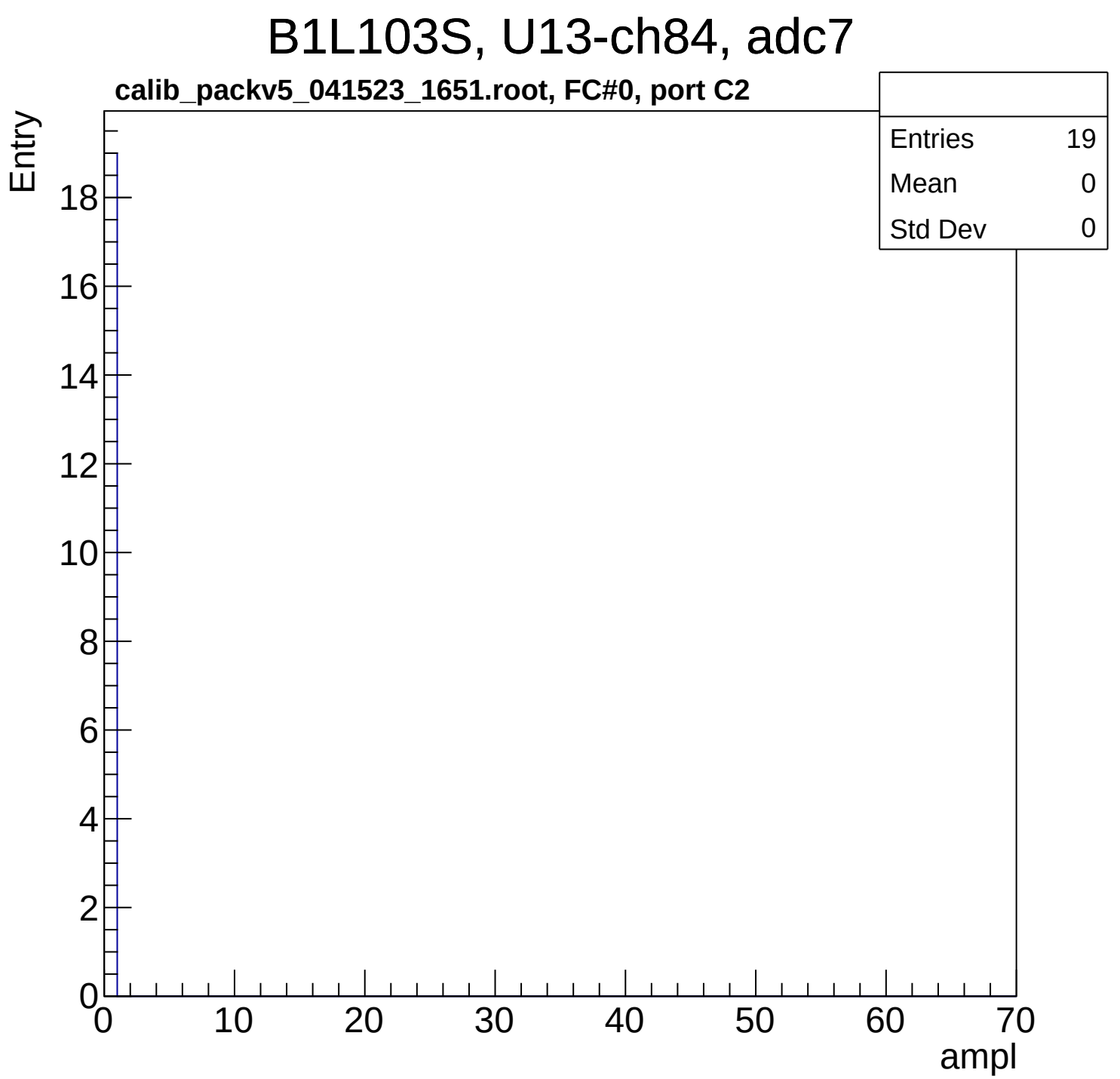
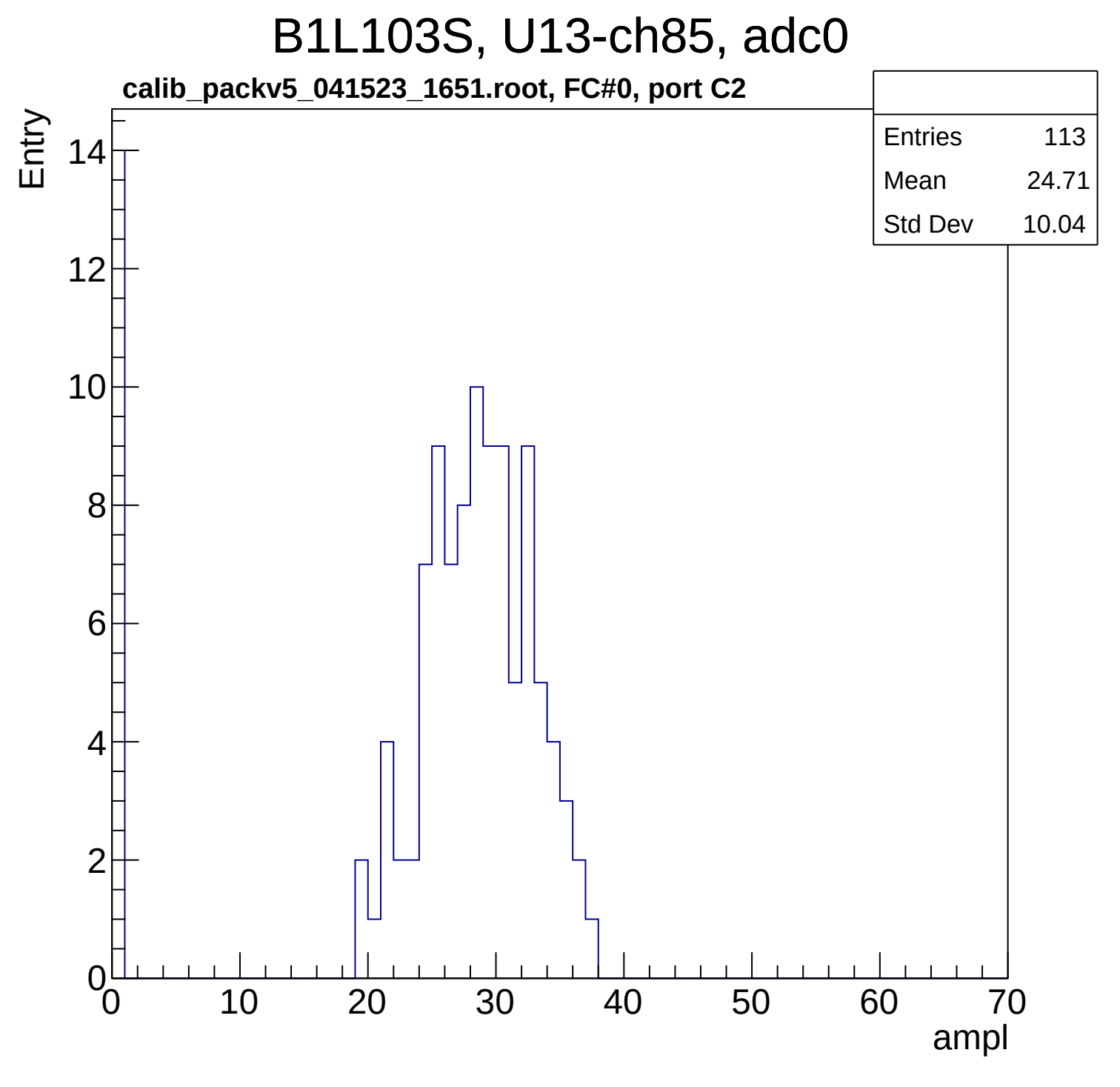
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U13-ch84, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch85, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 113
Mean 24.71
Std Dev 10.04
Entry
ampl
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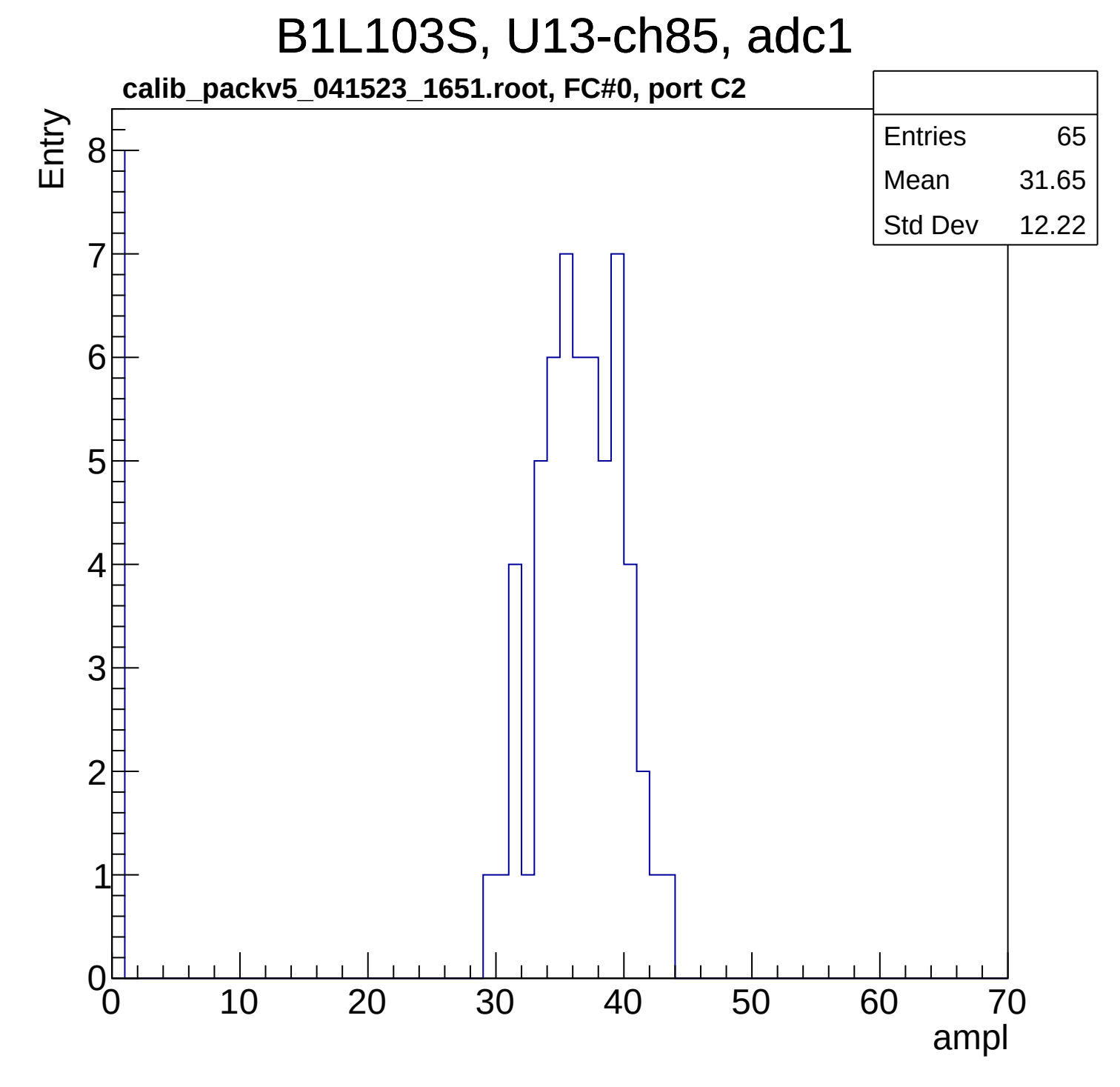
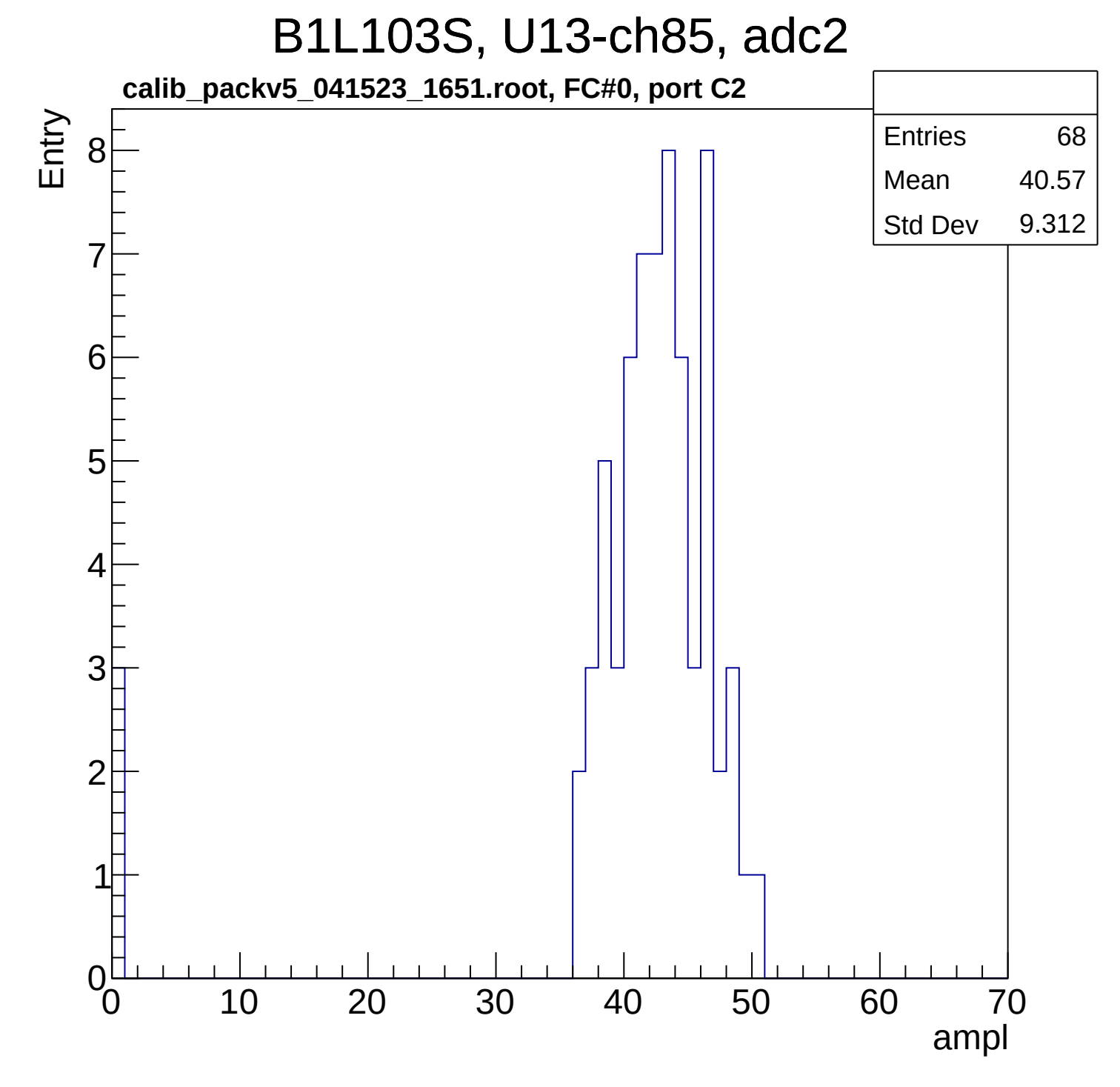
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U13-ch85, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 31.65
Std Dev 12.22
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch85, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 40.57
Std Dev 9.312
Entry
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2
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4
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6
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8
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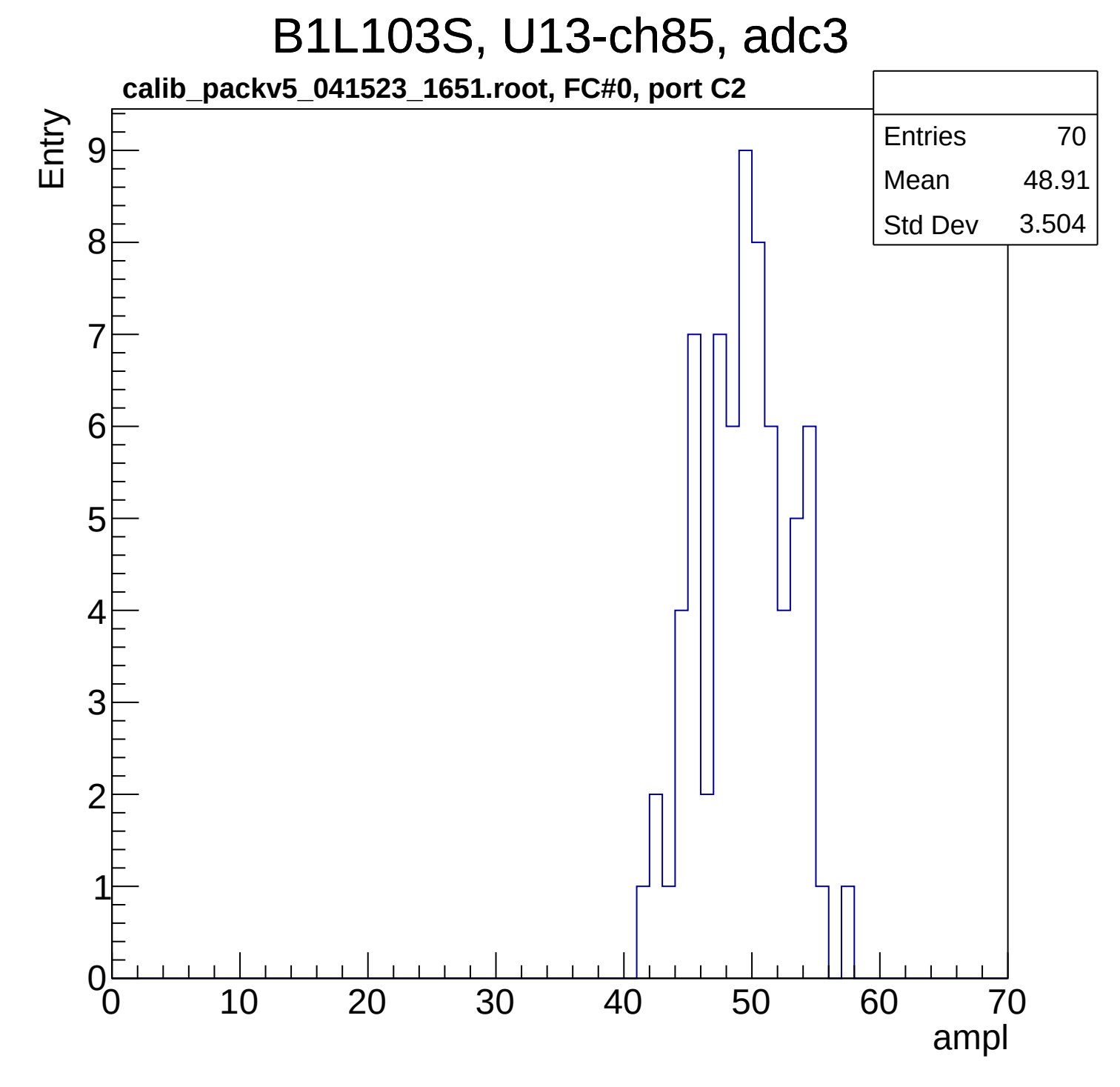
ampl


B1L103S, U13-ch85, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 48.91
Std Dev 3.504
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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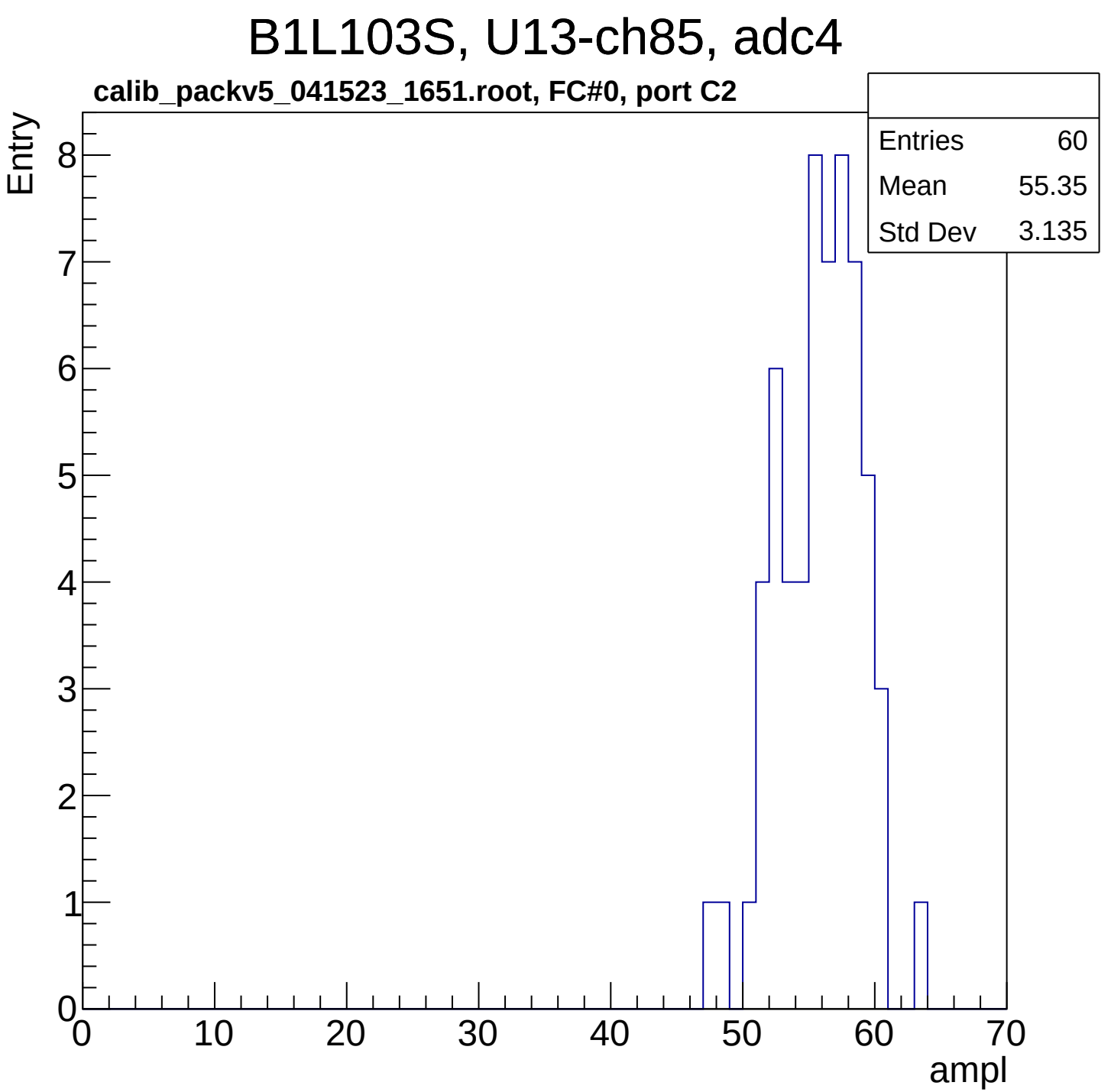
B1L103S, U13-ch85, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 55.35
Std Dev 3.135
Entry
ampl
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2
3
4
5
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0
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40
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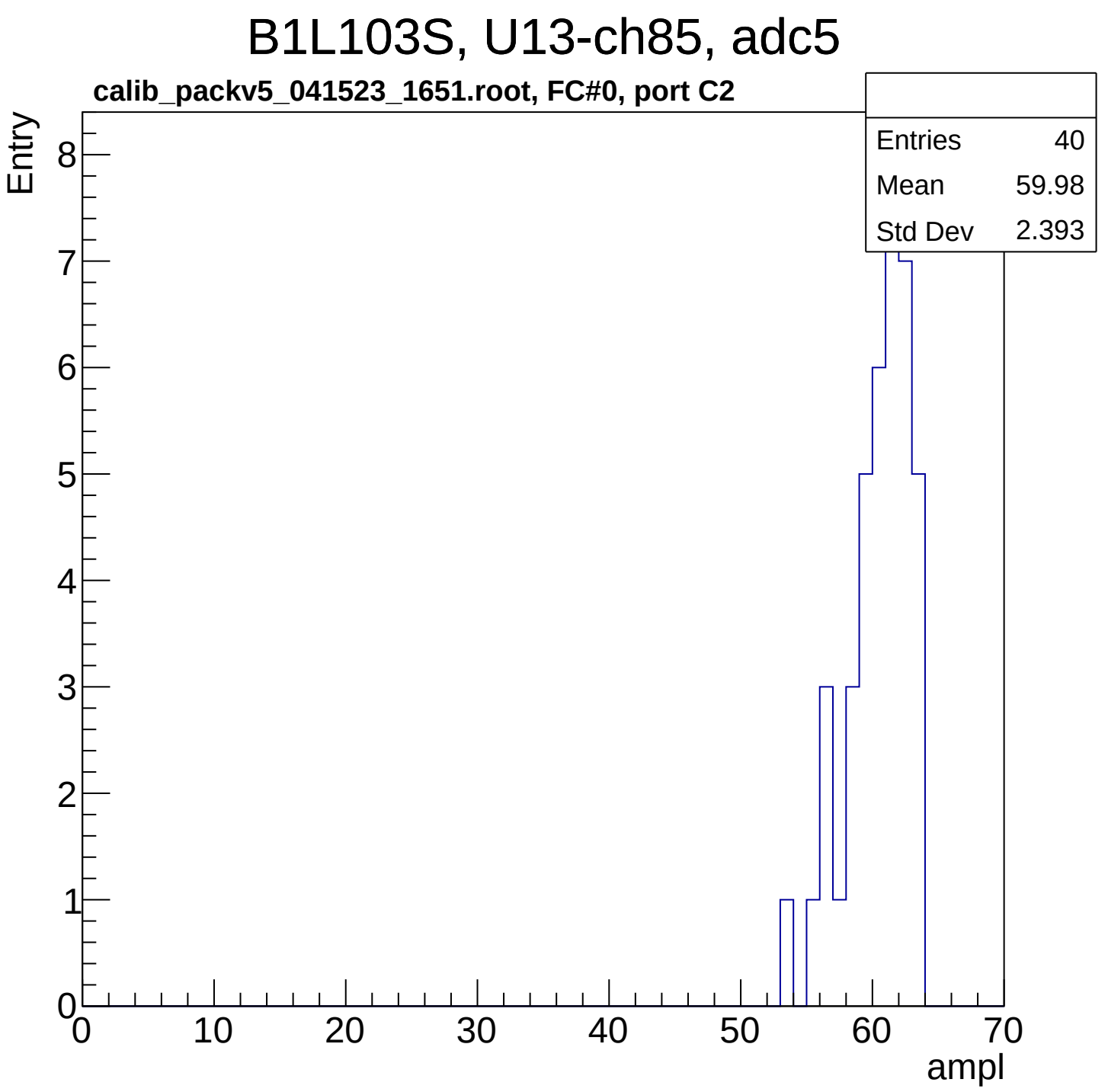
B1L103S, U13-ch85, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 59.98
Std Dev 2.393
Entry
ampl
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2
3
4
5
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7
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0
10
20
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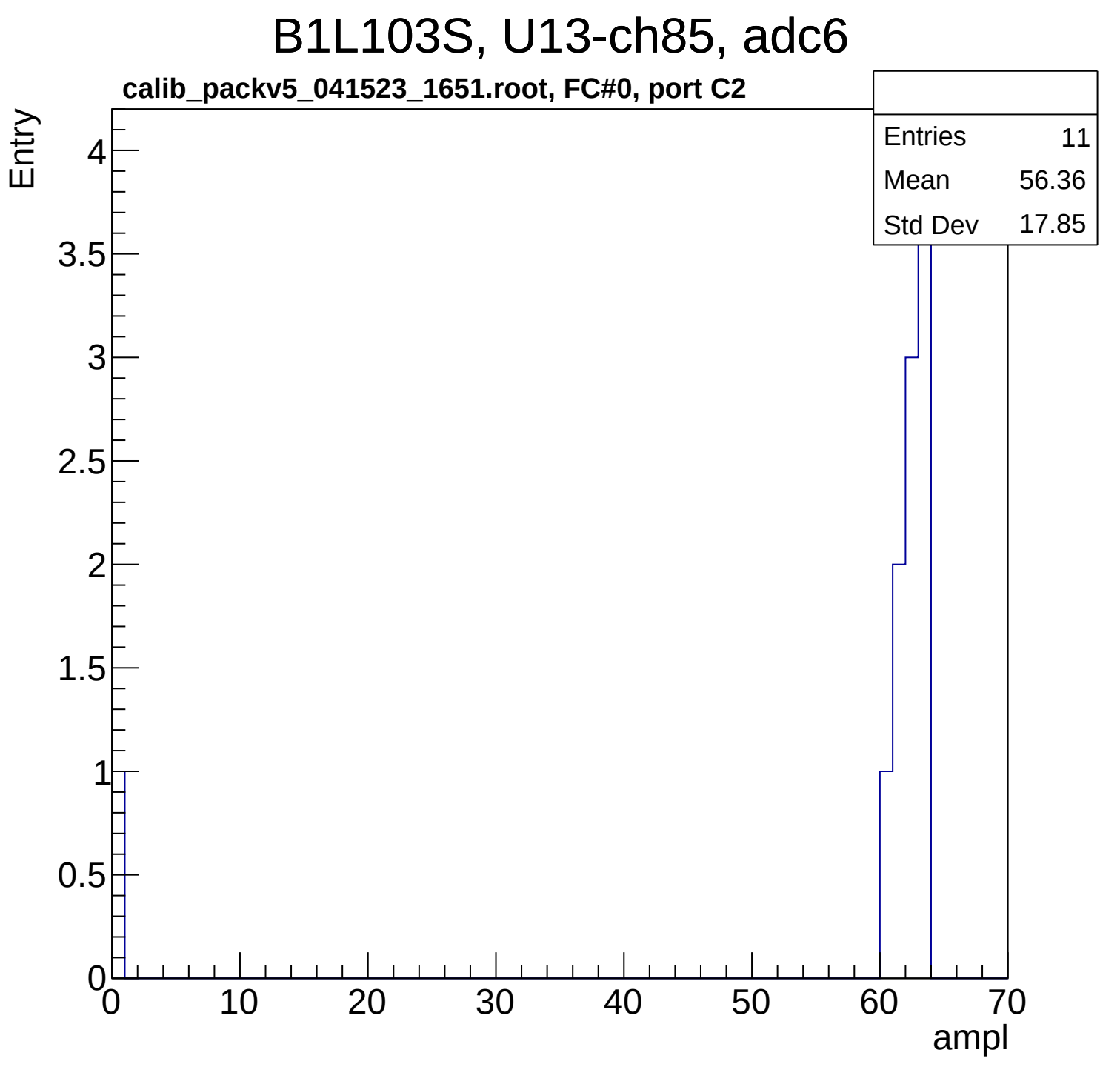
40
50
60
70


B1L103S, U13-ch85, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 56.36
Std Dev 17.85
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
50
60
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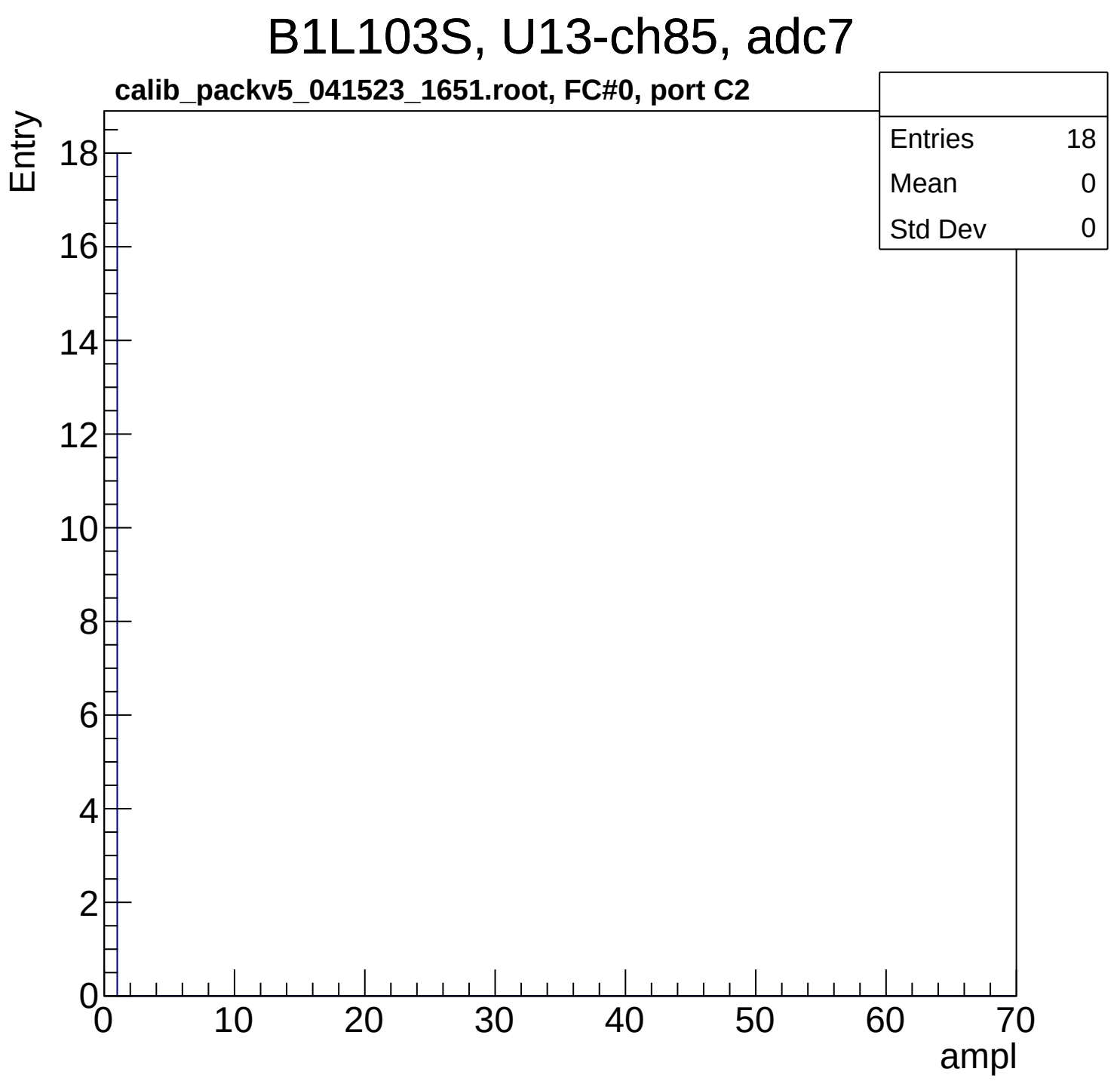
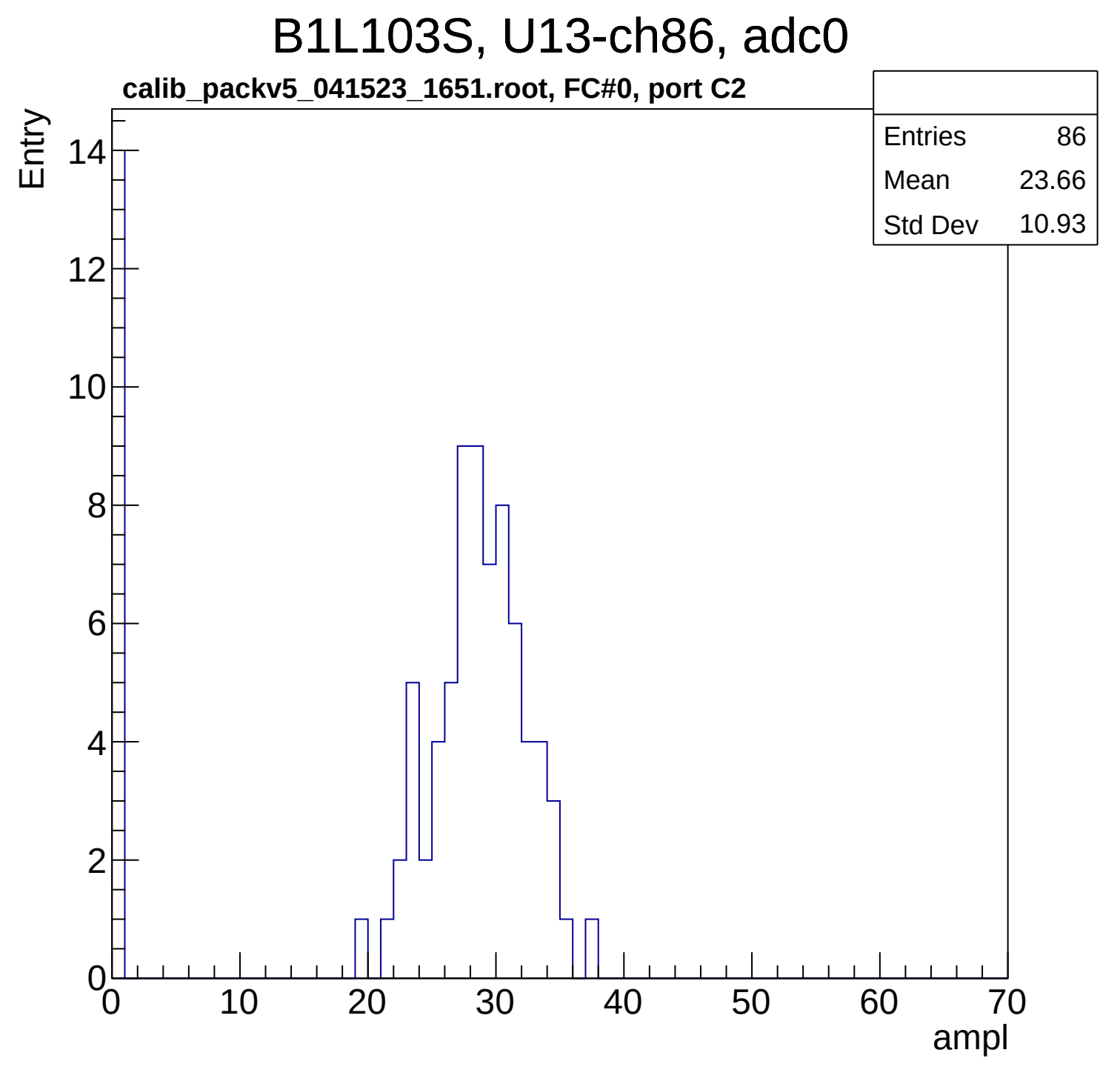
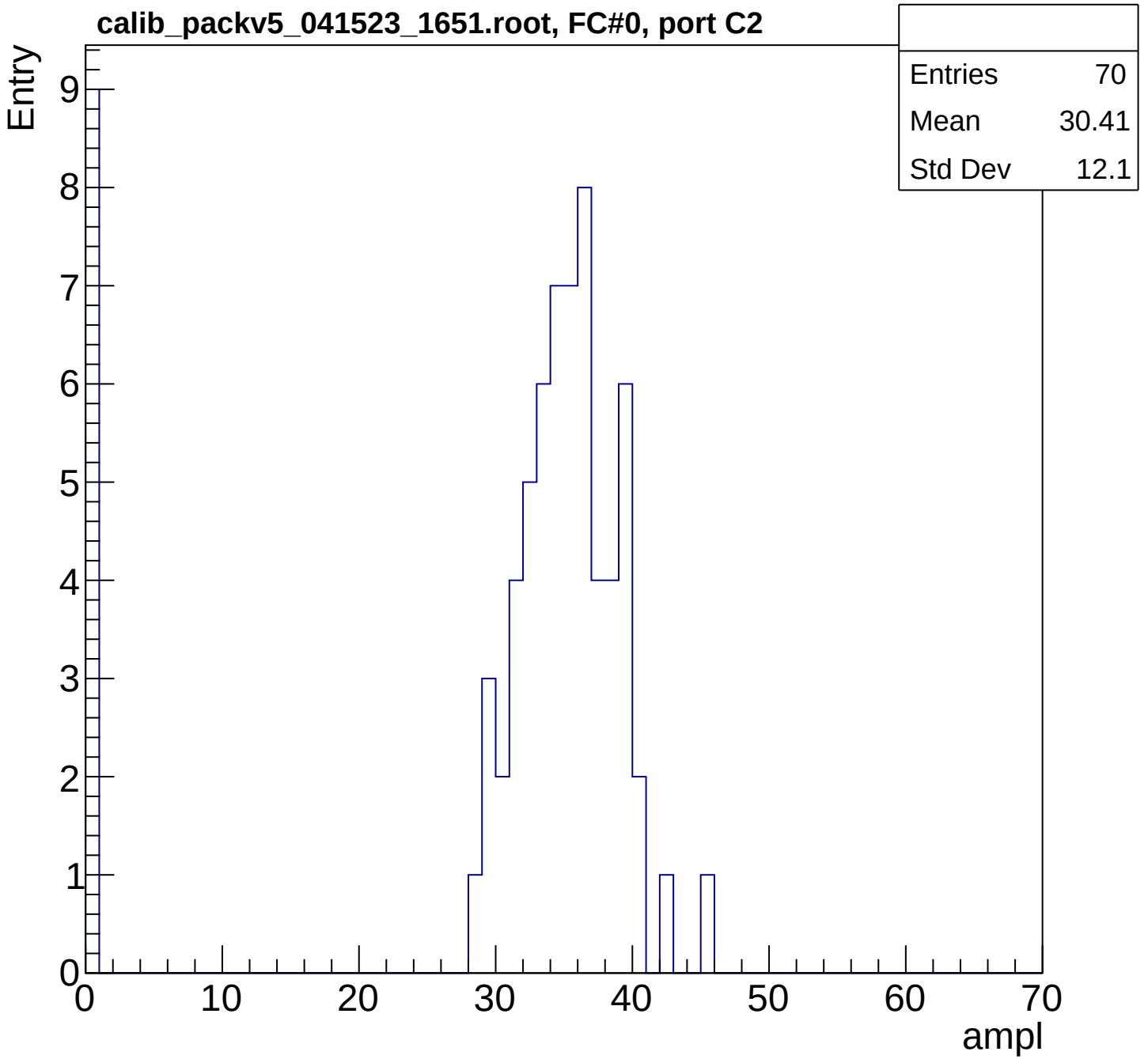

B1L103S, U13-ch85, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch86, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 23.66
Std Dev 10.93
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch86, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 30.41
Std Dev 12.1
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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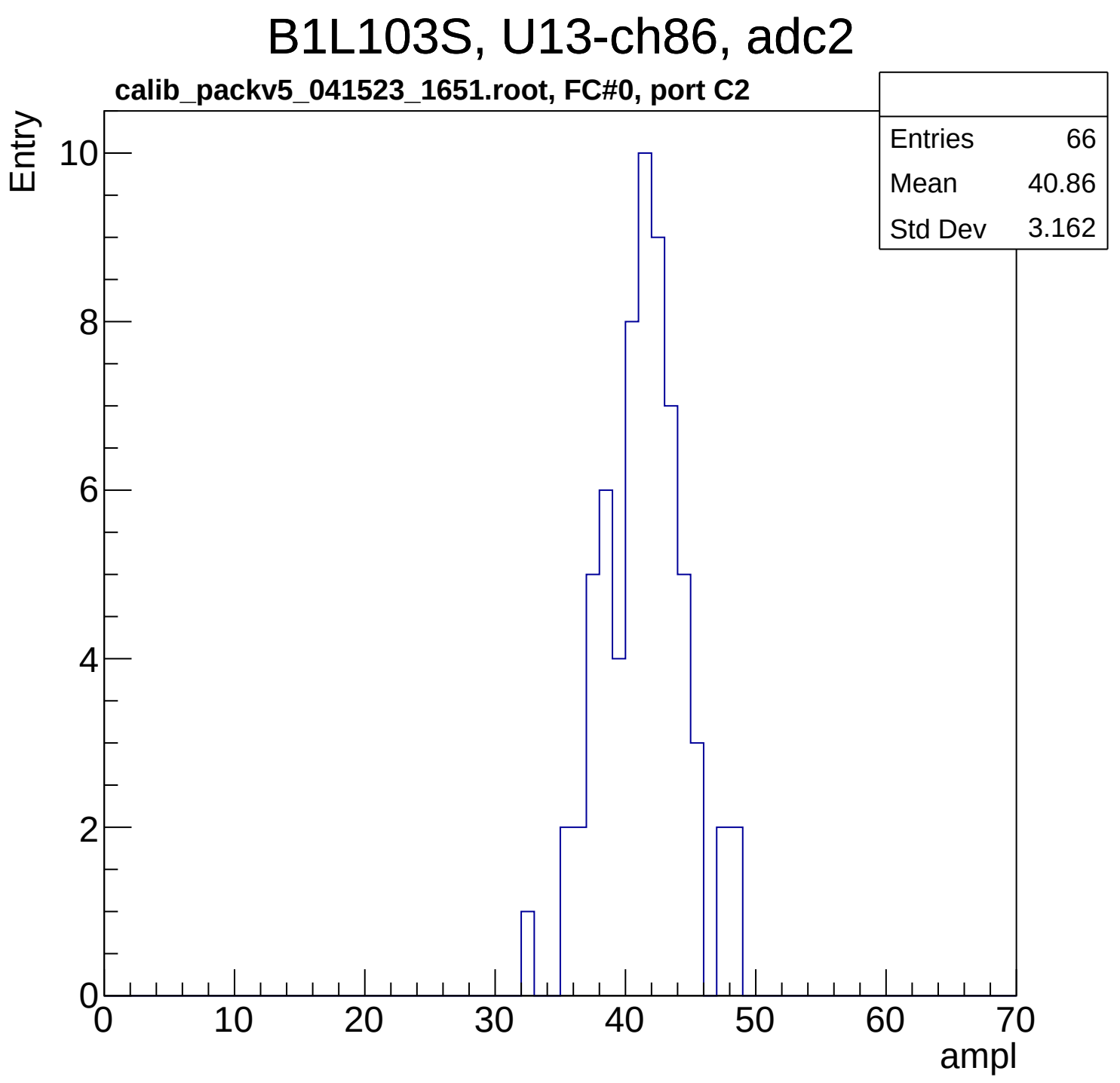
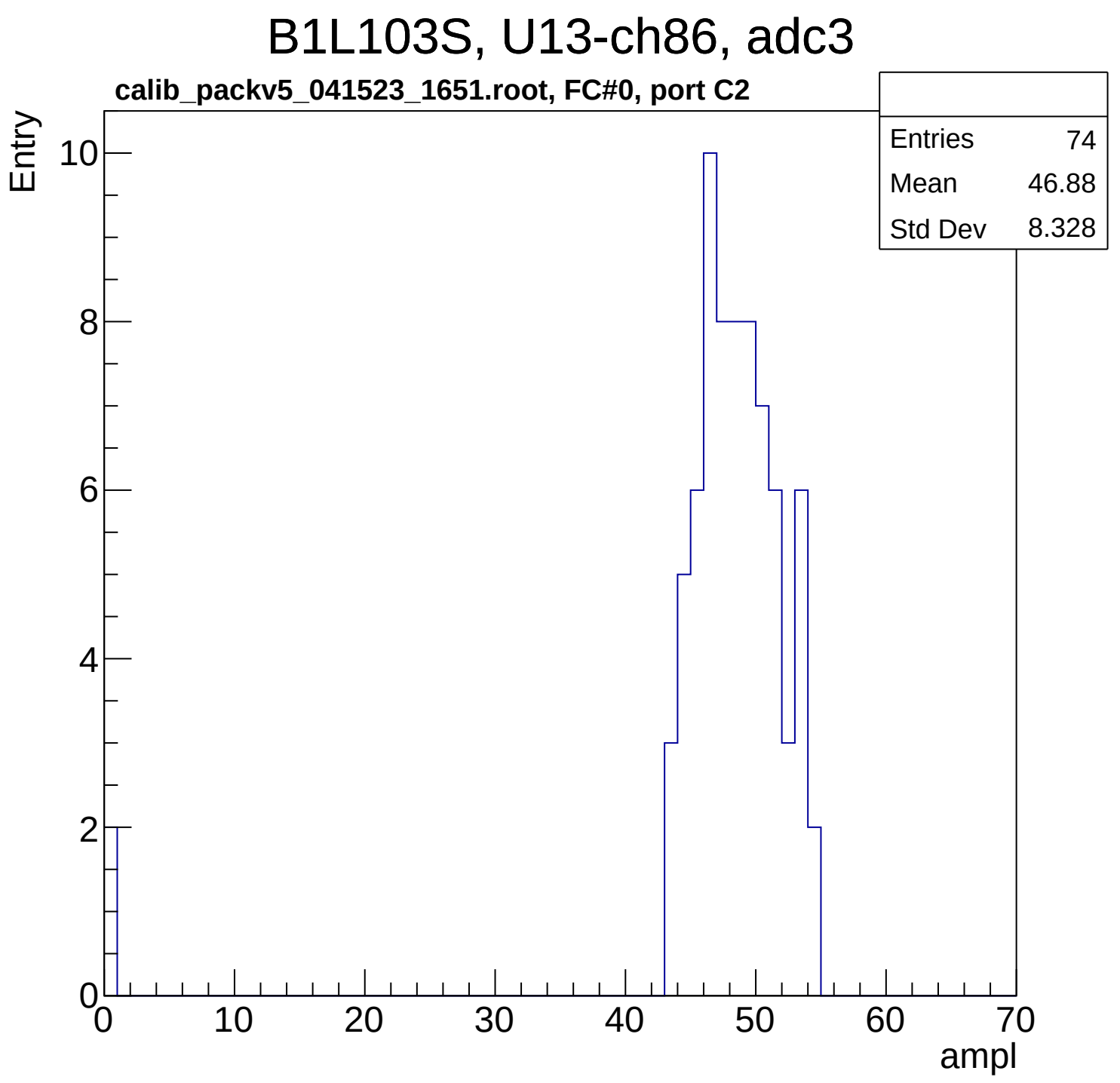
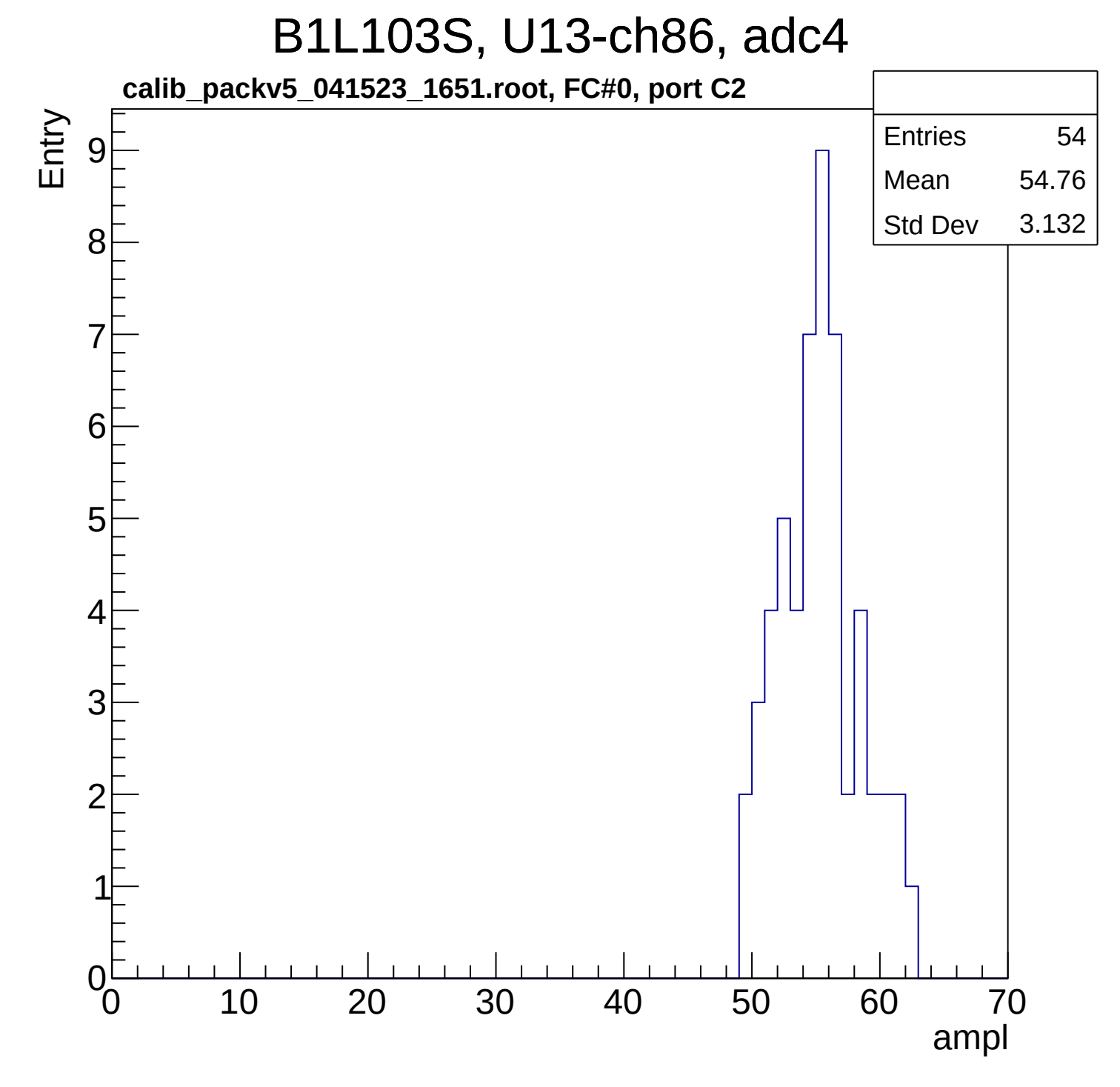
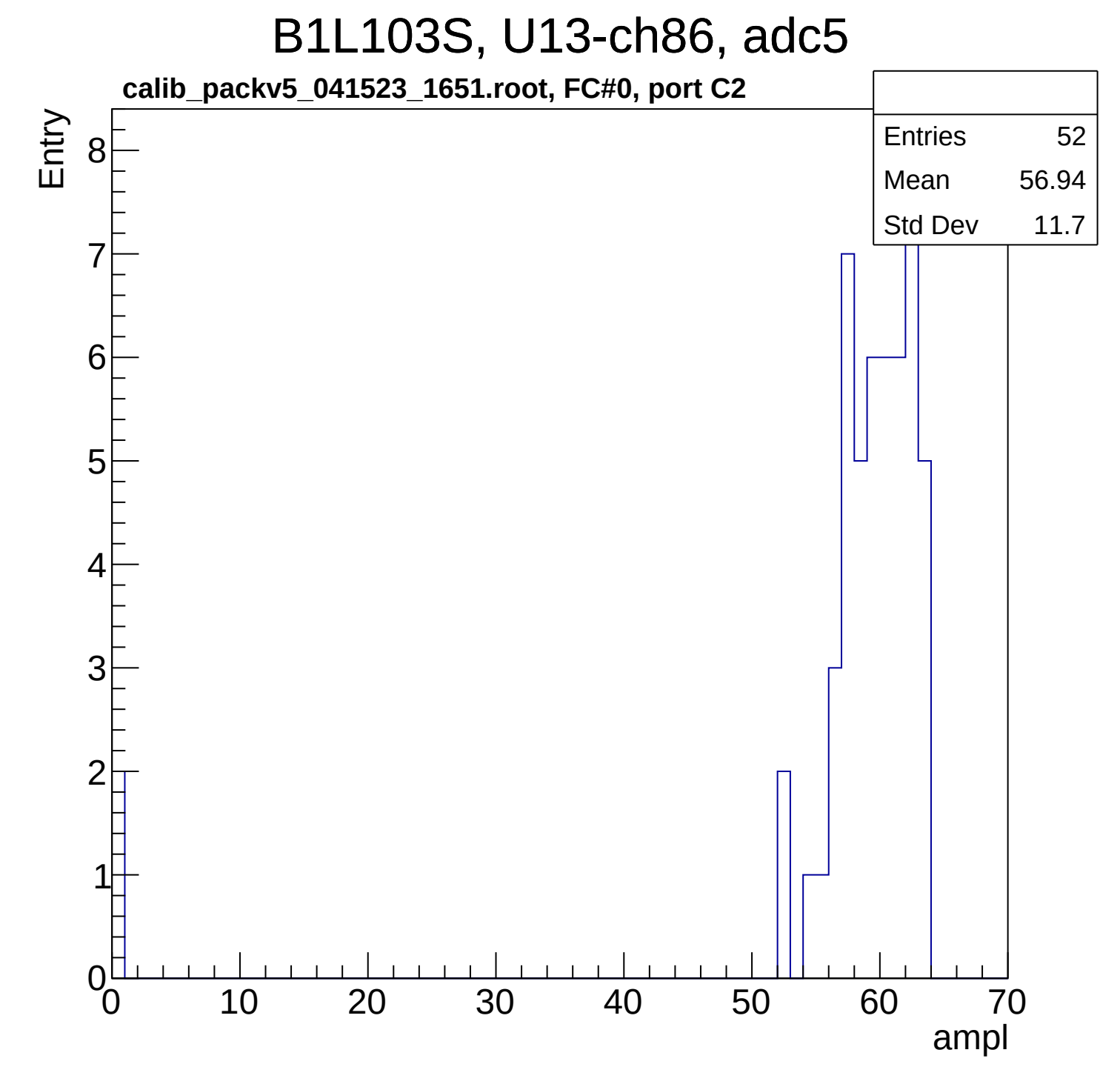

B1L103S, U13-ch86, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 40.86
Std Dev 3.162
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch86, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 46.88
Std Dev 8.328
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch86, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 54.76
Std Dev 3.132
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch86, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 56.94
Std Dev 11.7
Entry
ampl
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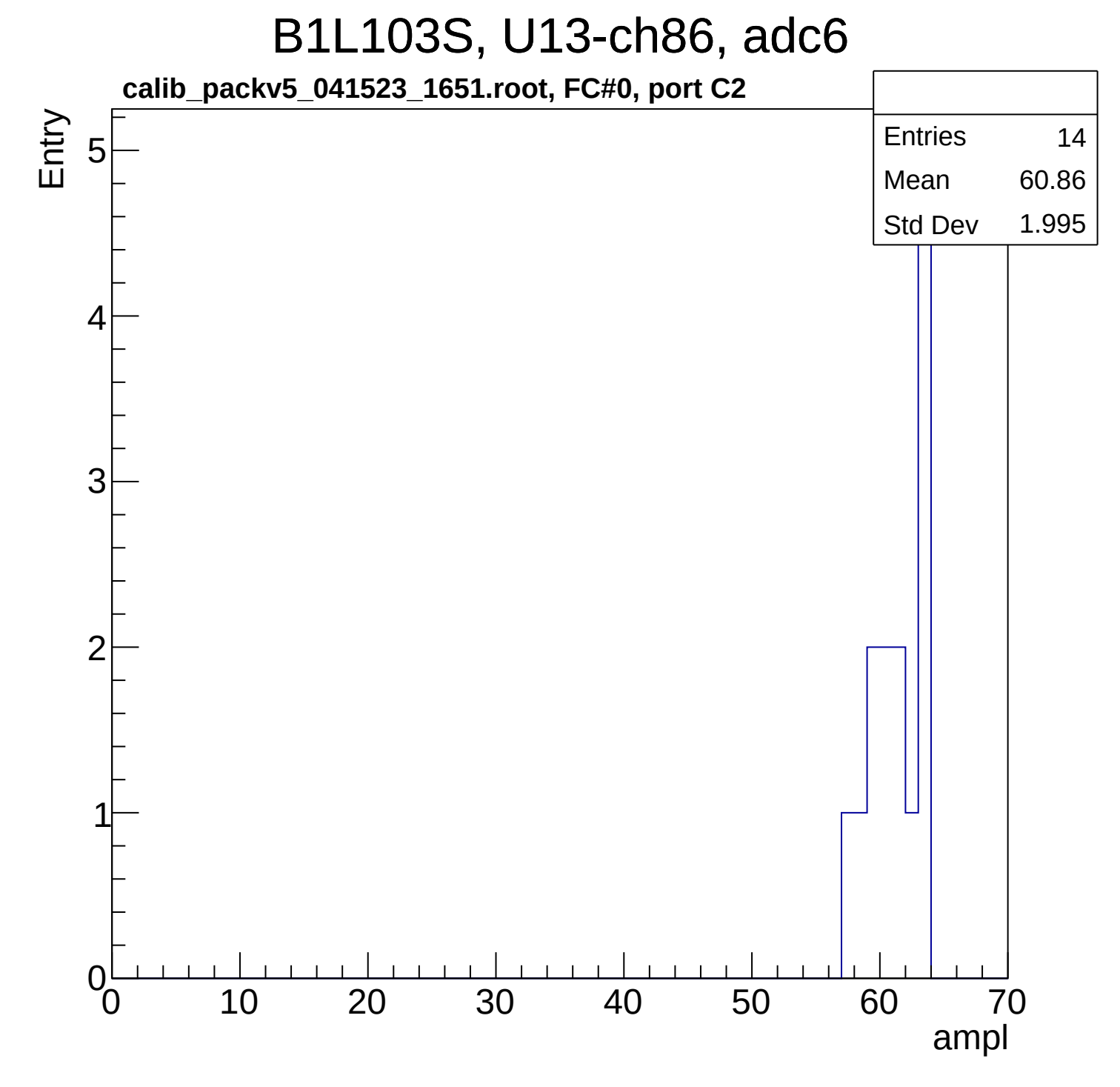
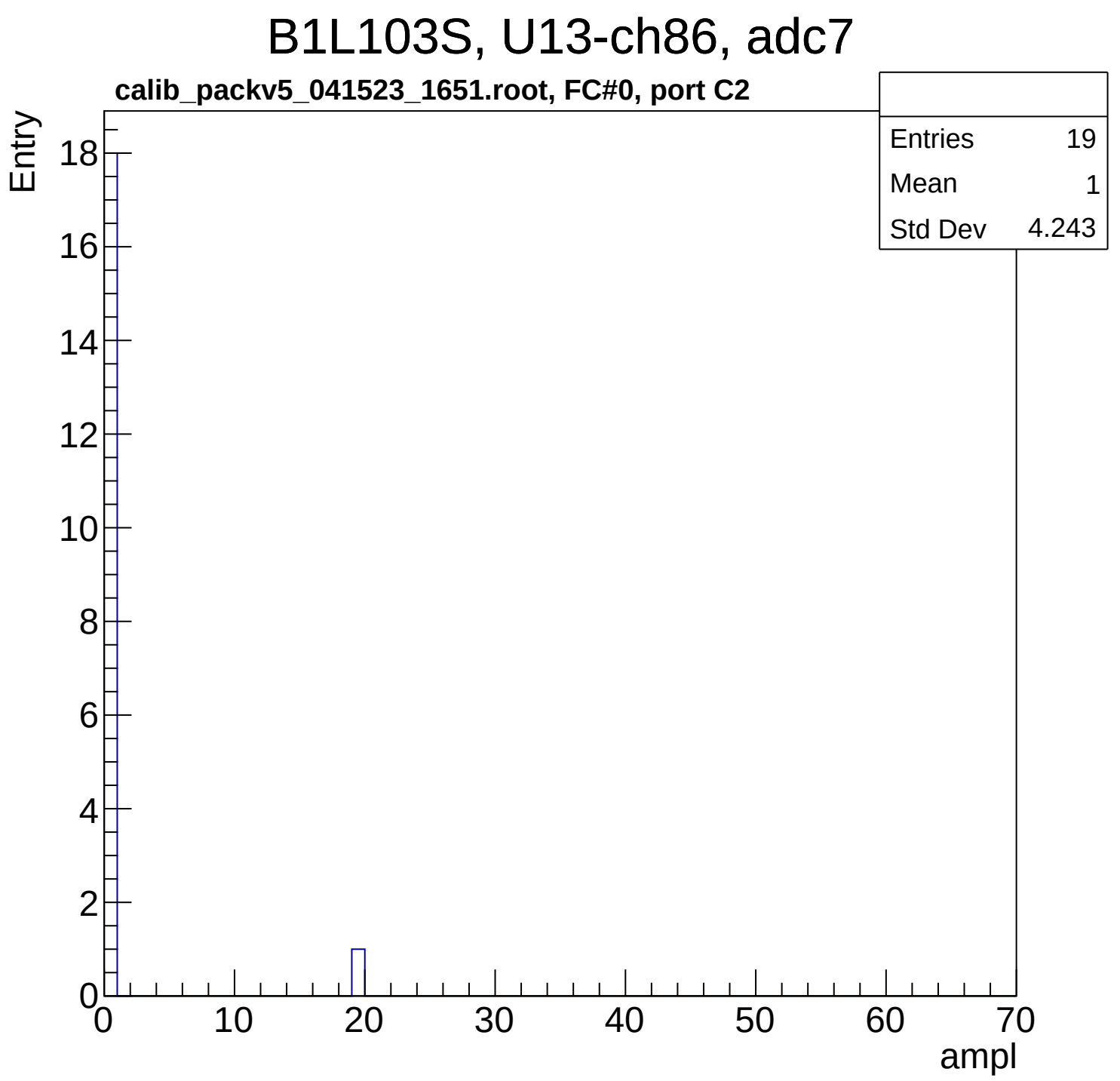
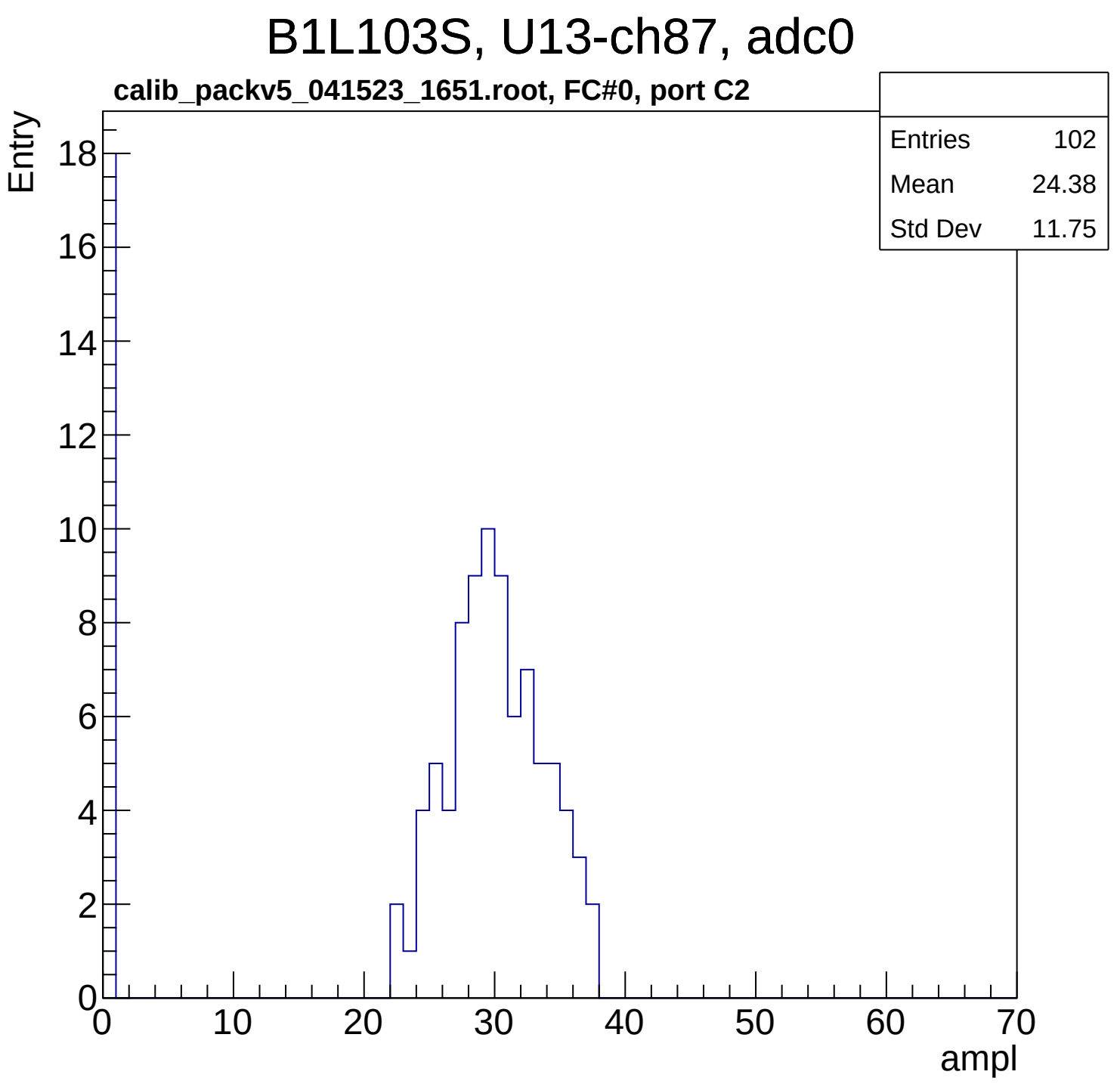
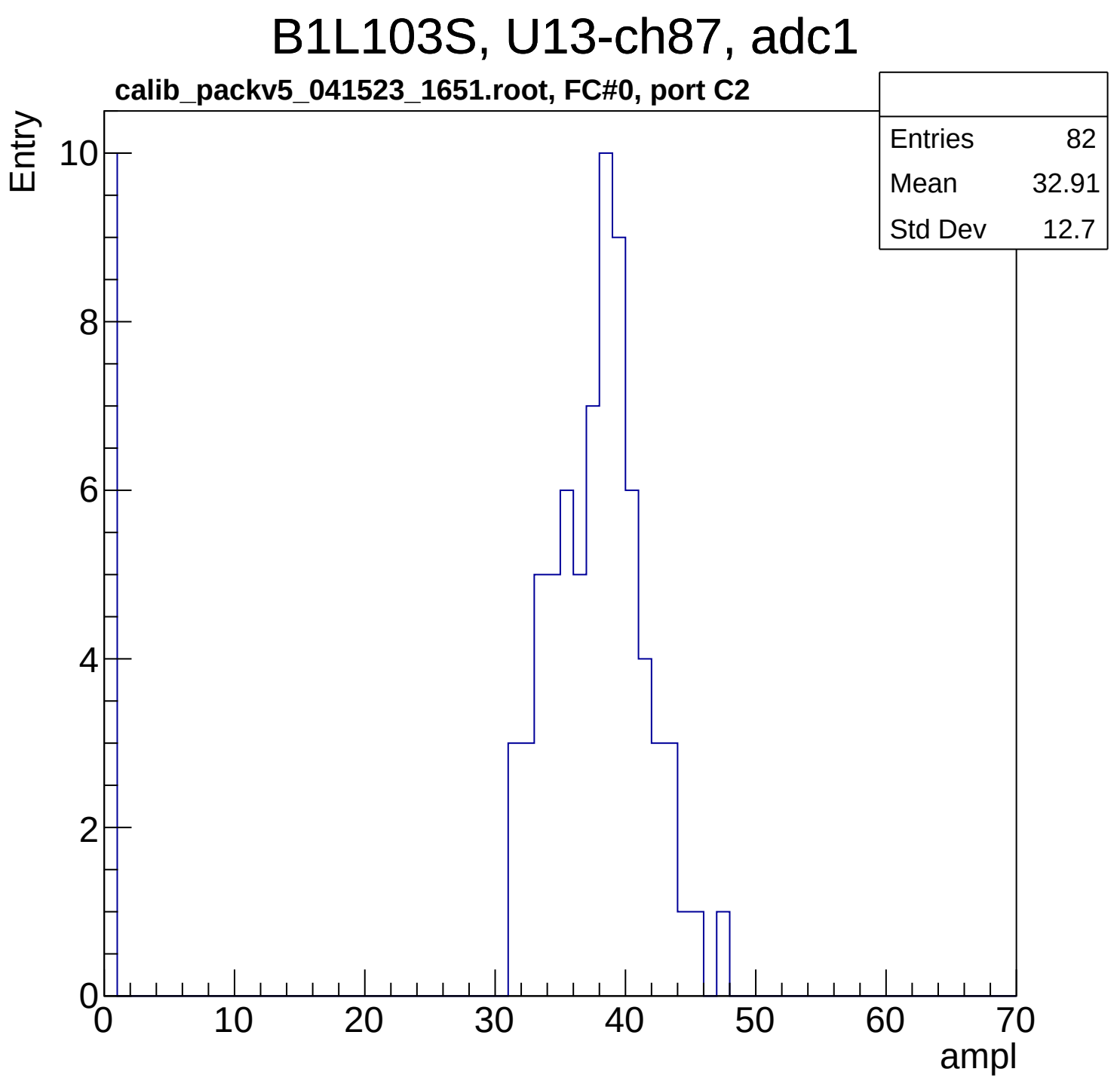
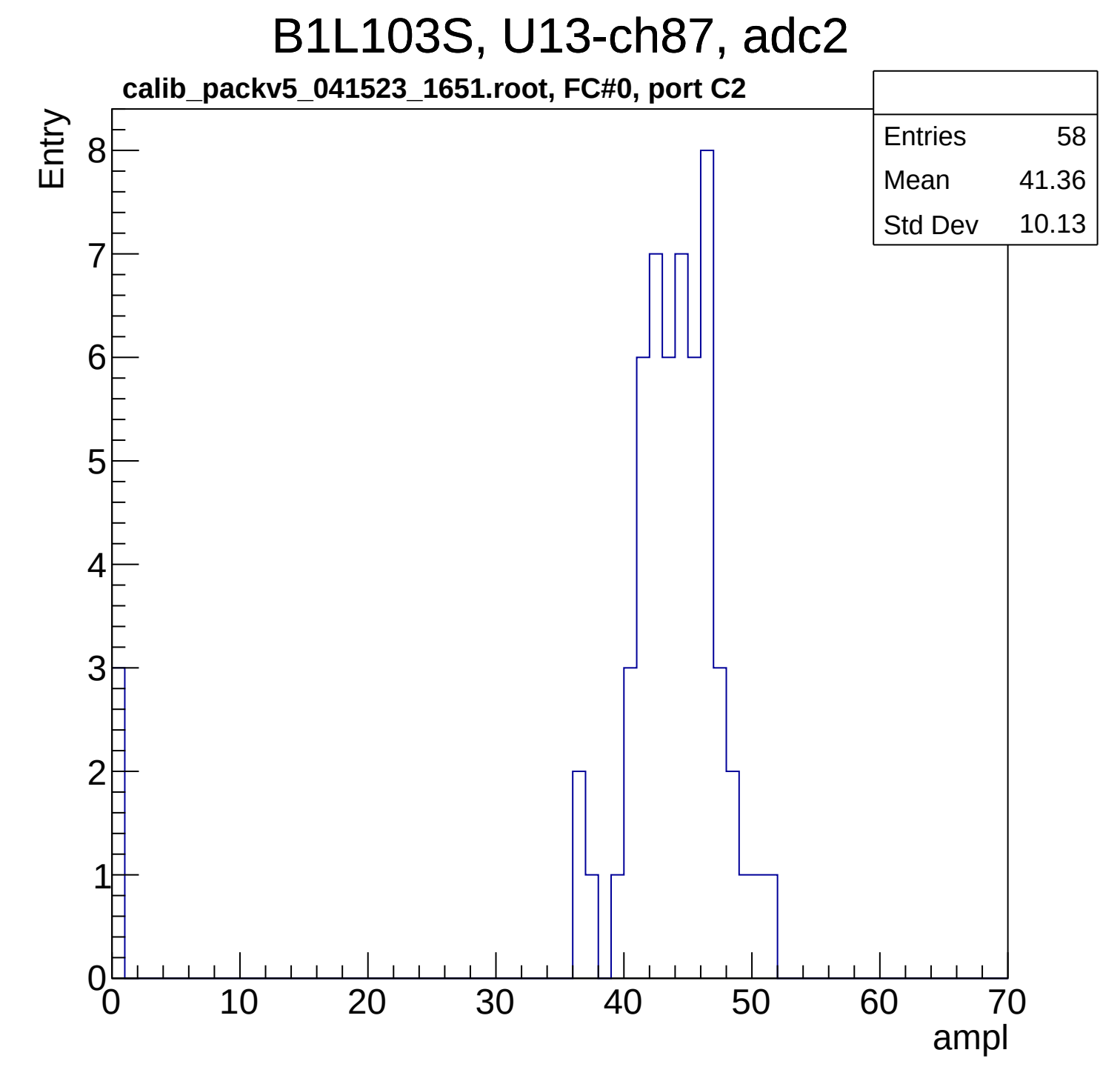
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch86, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 60.86
Std Dev 1.995
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch86, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1
Std Dev 4.243
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch87, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 24.38
Std Dev 11.75
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch87, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 32.91
Std Dev 12.7
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch87, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 41.36
Std Dev 10.13
Entry
ampl
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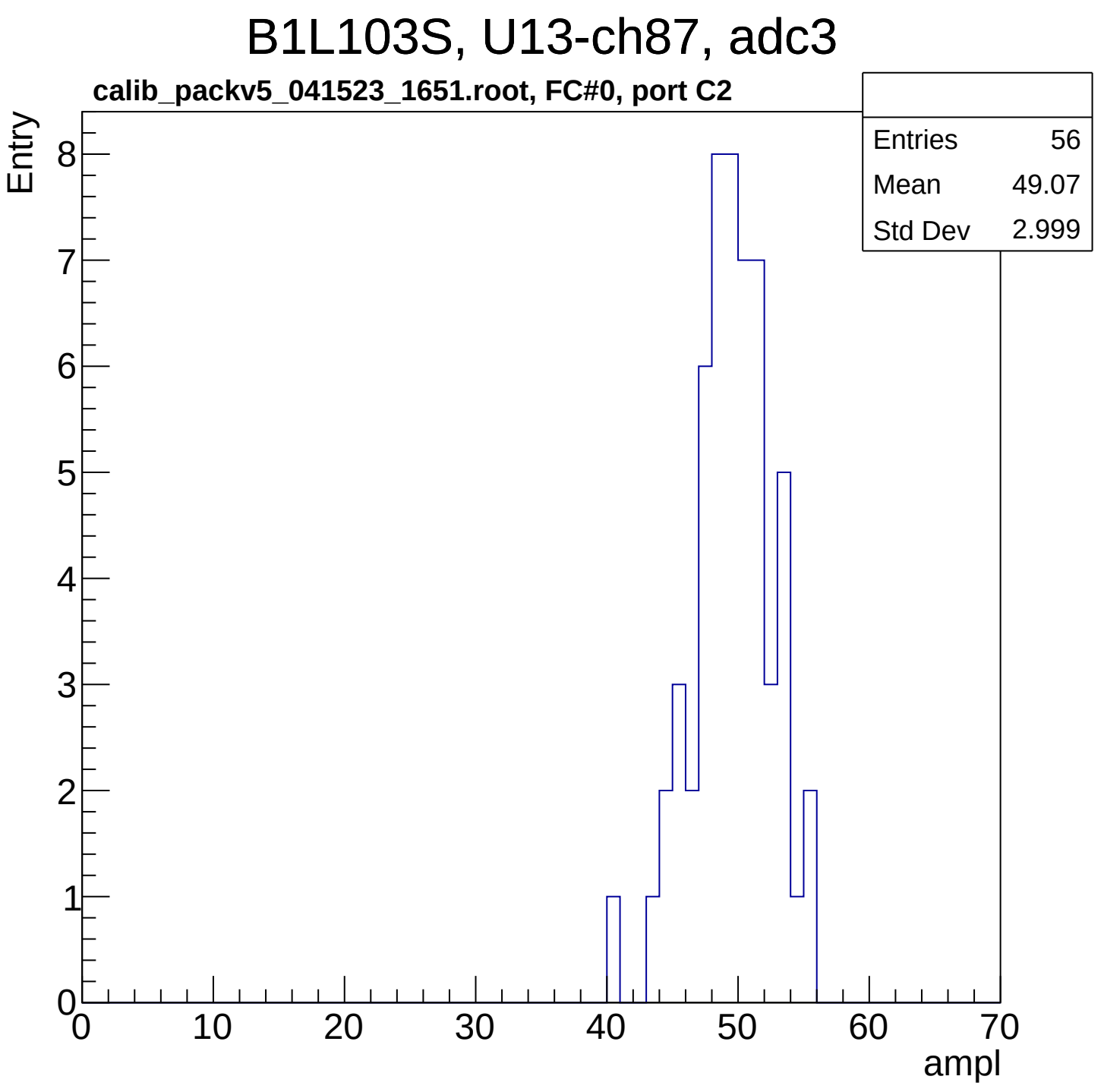
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch87, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 49.07
Std Dev 2.999
Entry
ampl
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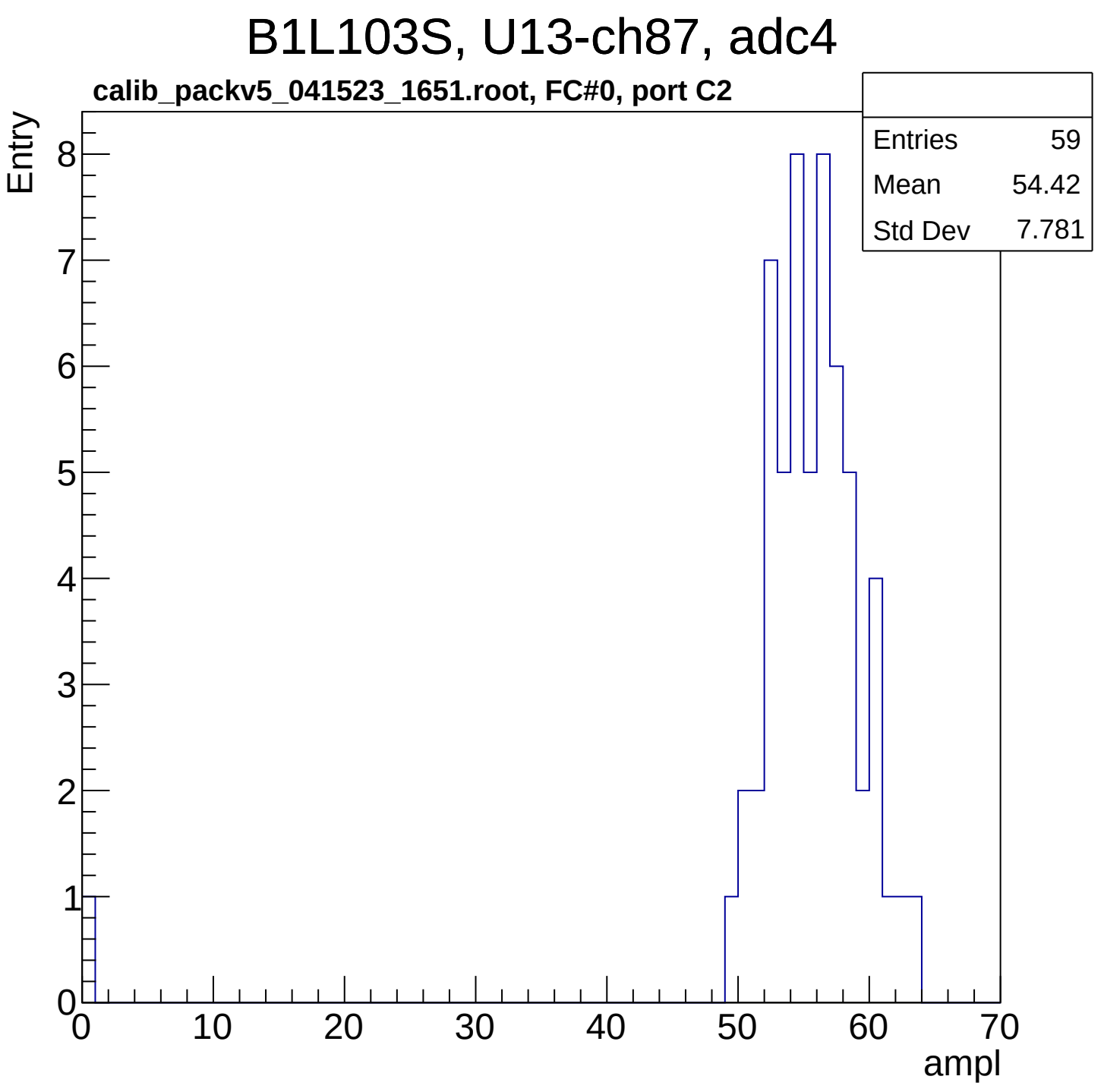
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch87, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.42
Std Dev 7.781
Entry
ampl
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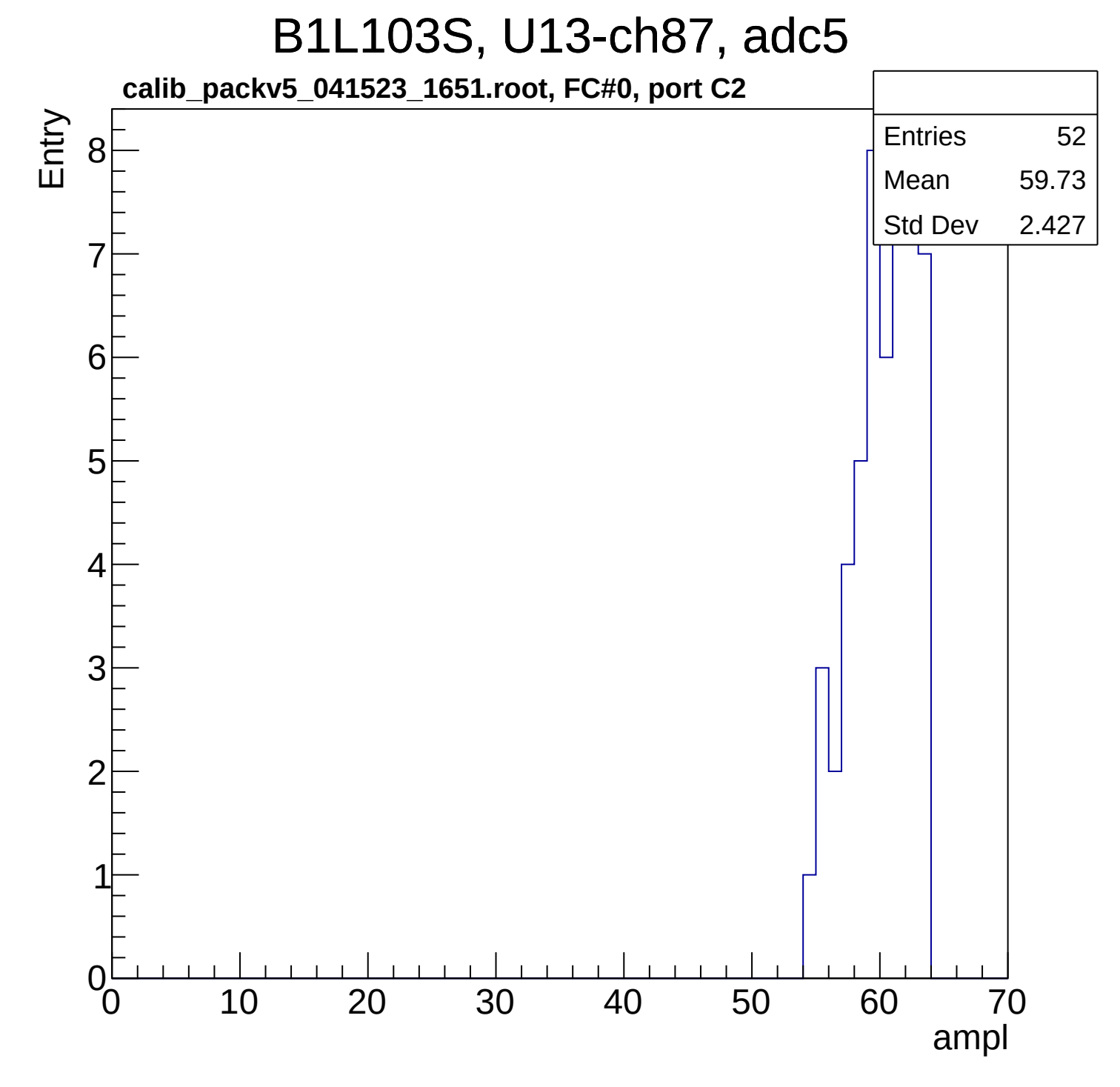
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch87, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 59.73
Std Dev 2.427
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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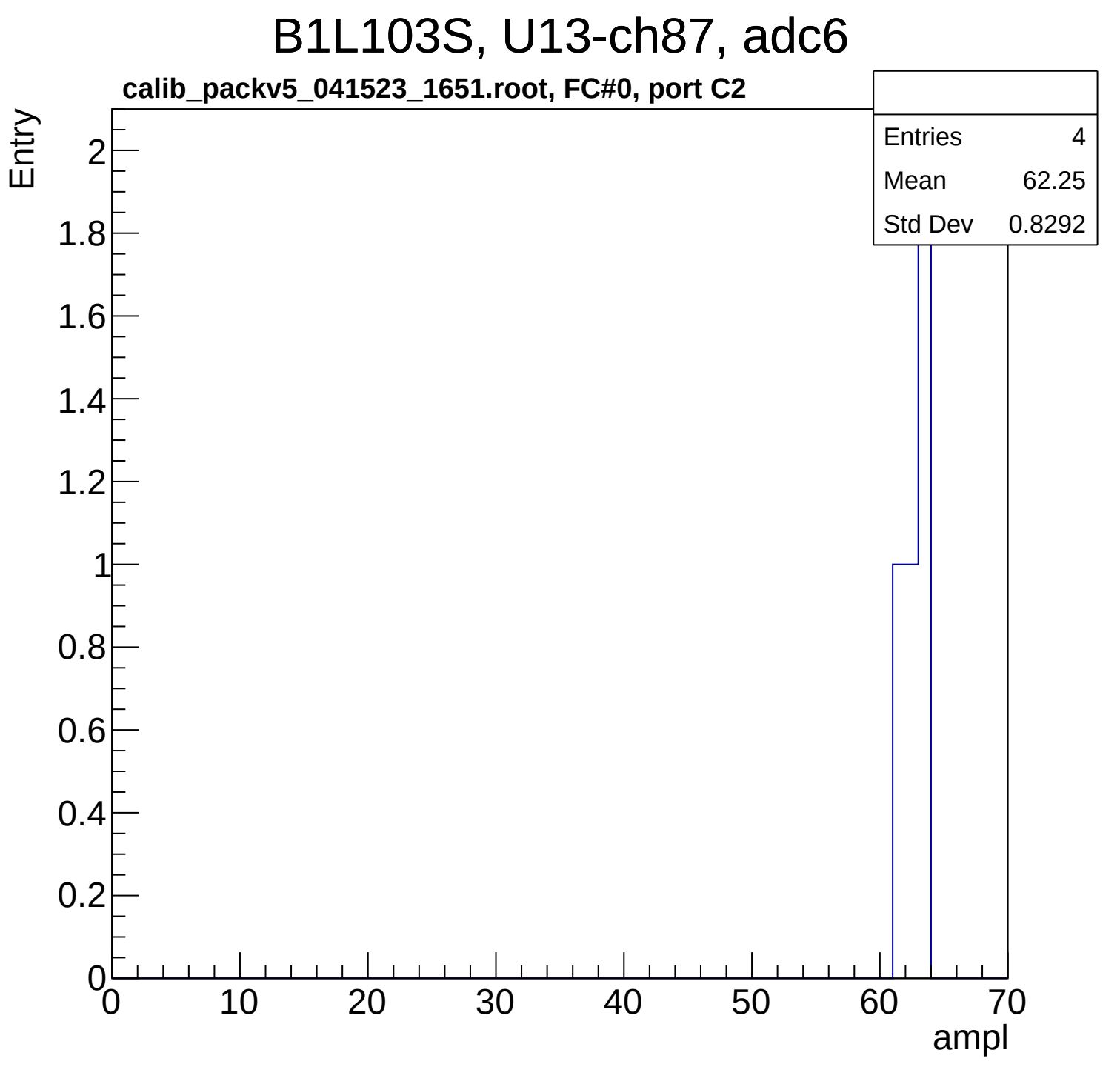
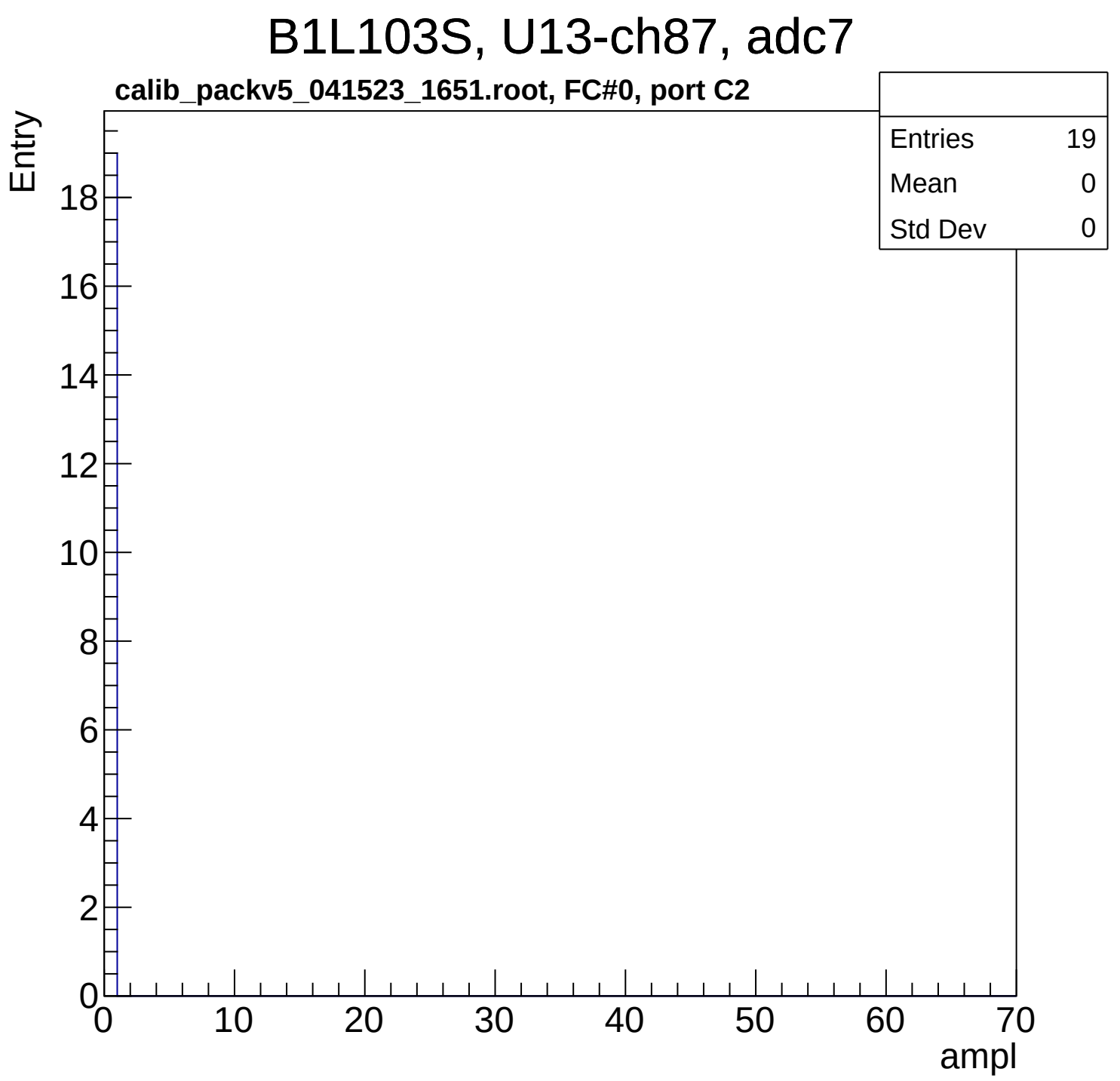
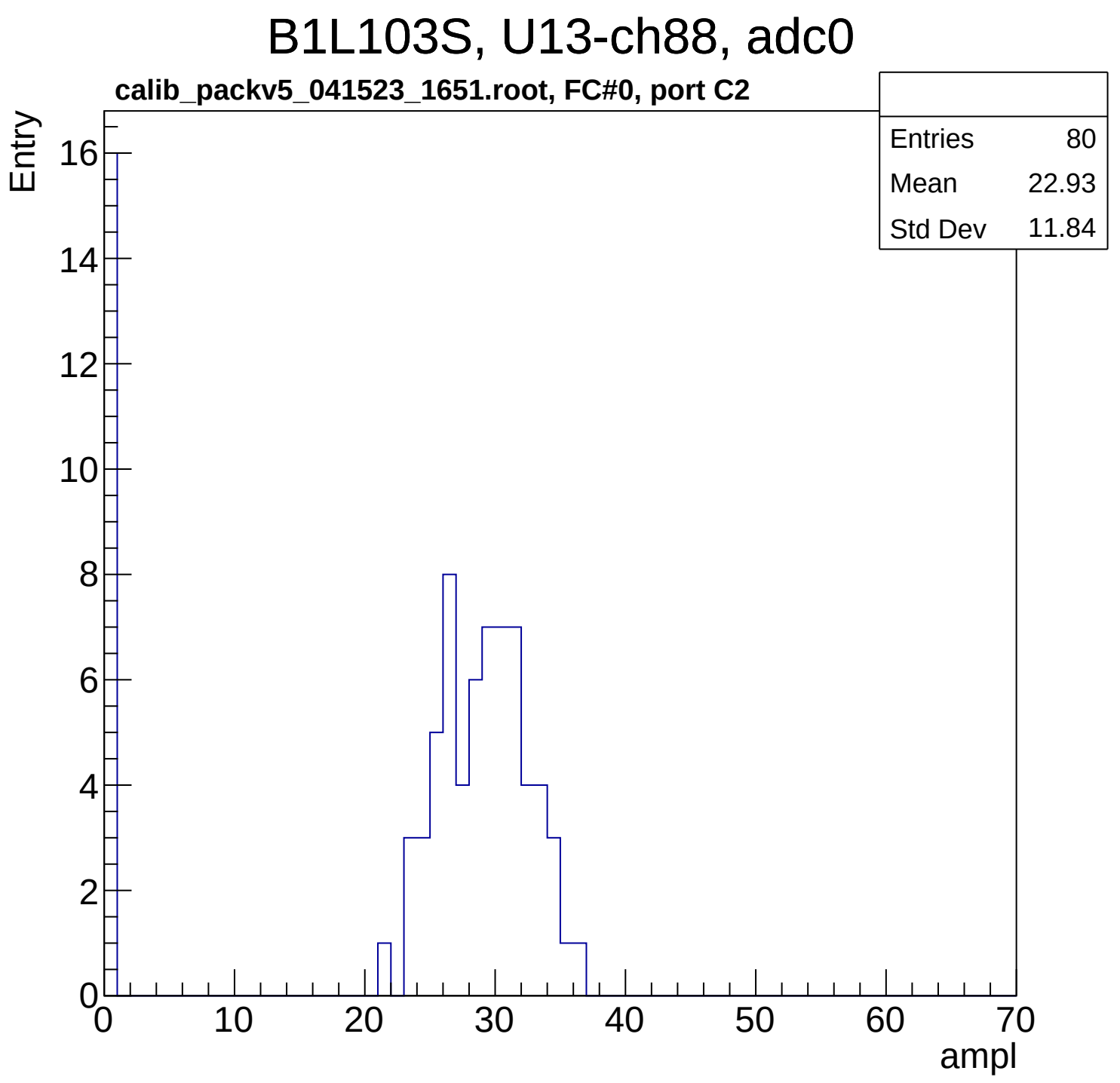
40
50
60
70


B1L103S, U13-ch87, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U13-ch87, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch88, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 22.93
Std Dev 11.84
Entry
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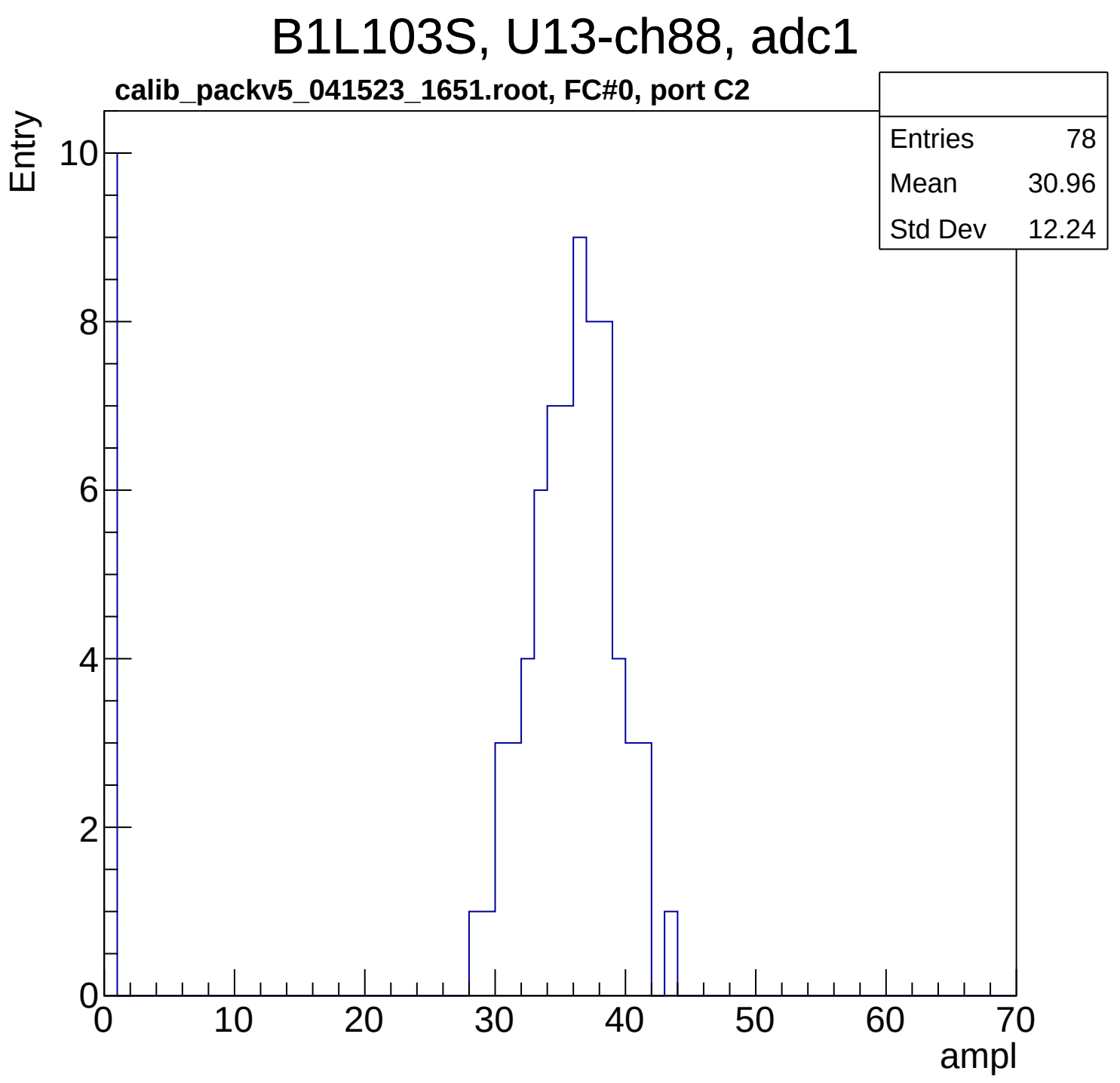
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch88, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 30.96
Std Dev 12.24
Entry
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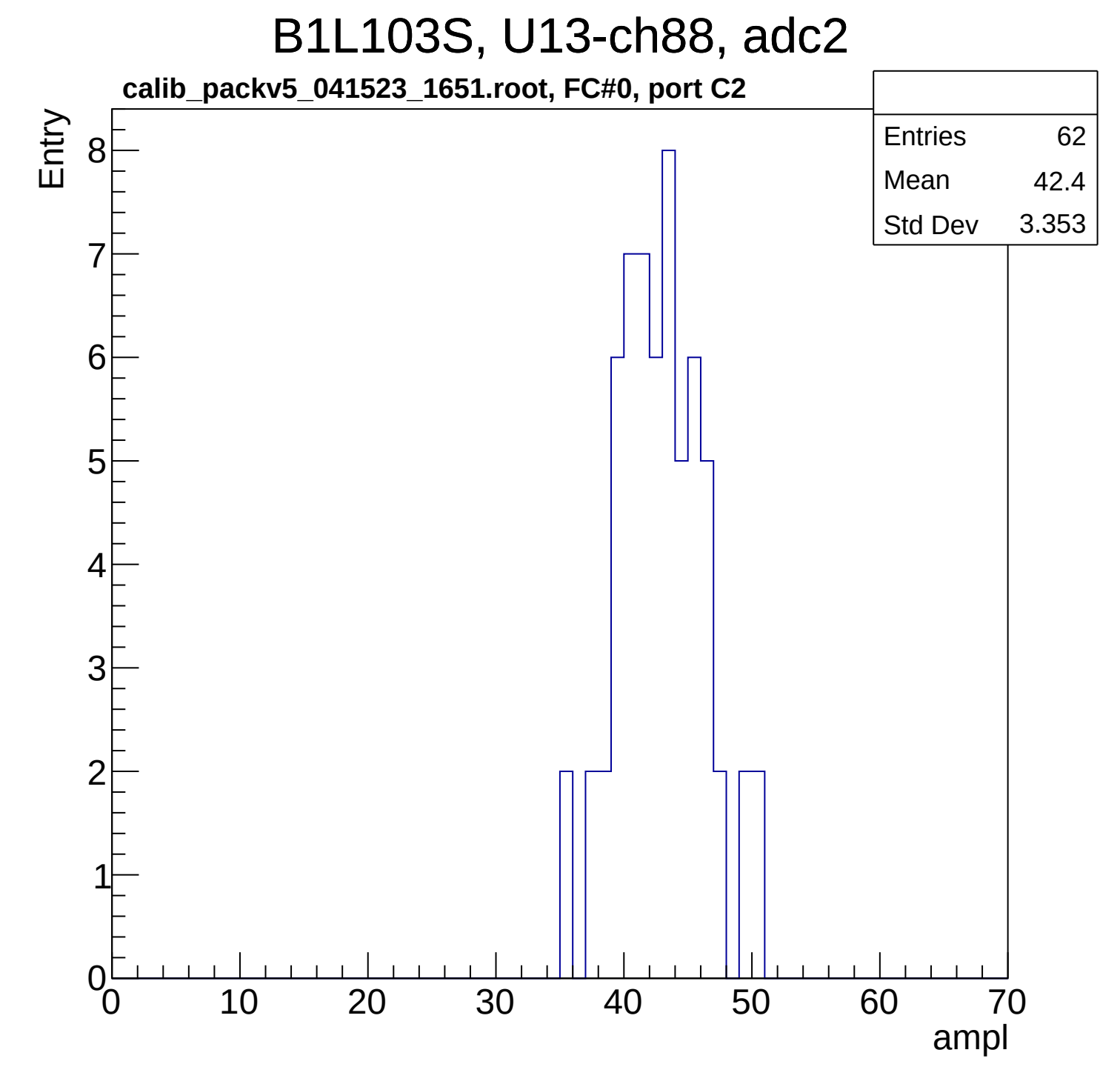
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch88, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 42.4
Std Dev 3.353
Entry
ampl
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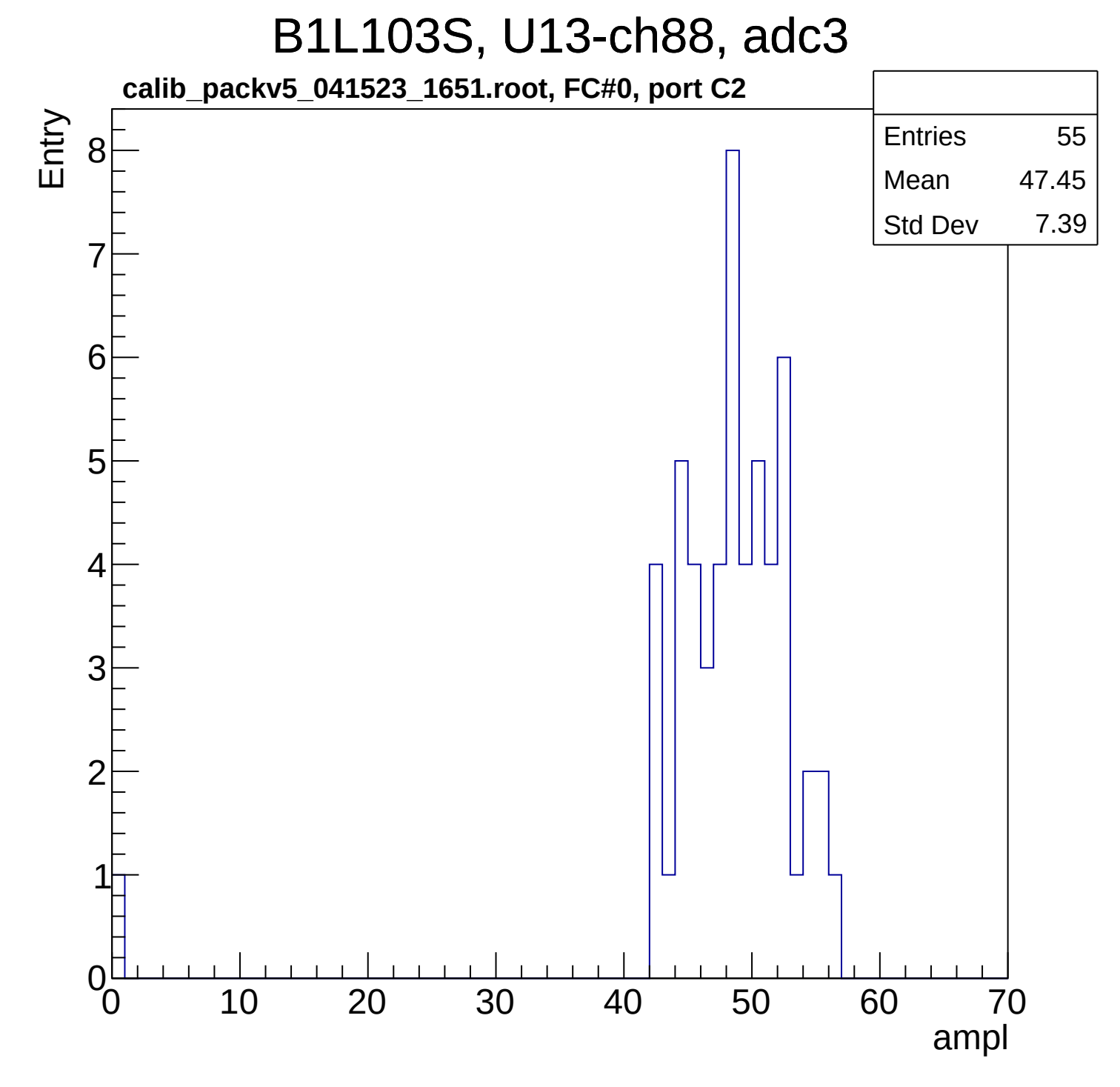
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch88, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 47.45
Std Dev 7.39
Entry
ampl
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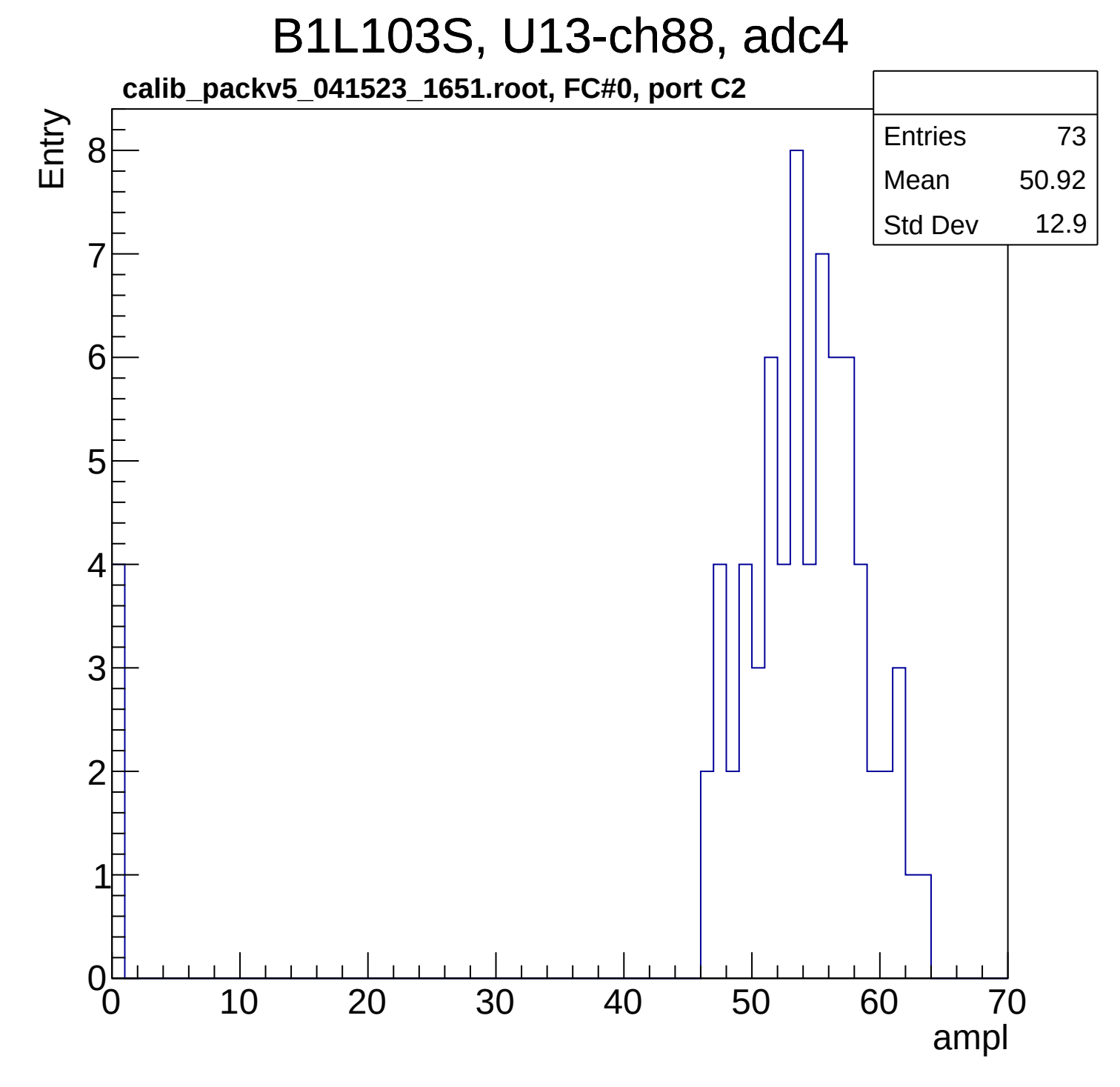
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch88, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 50.92
Std Dev 12.9
Entry
ampl
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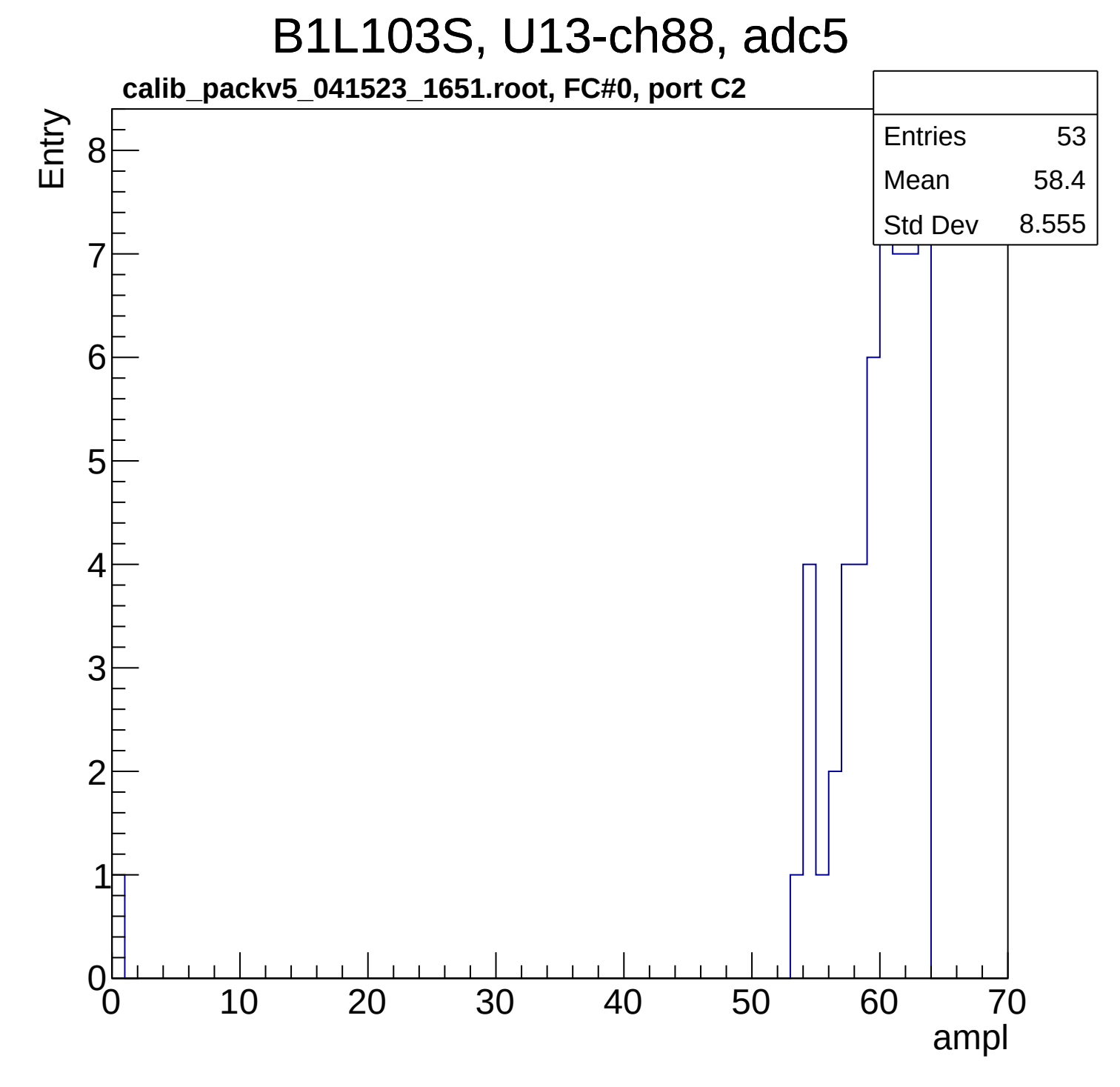
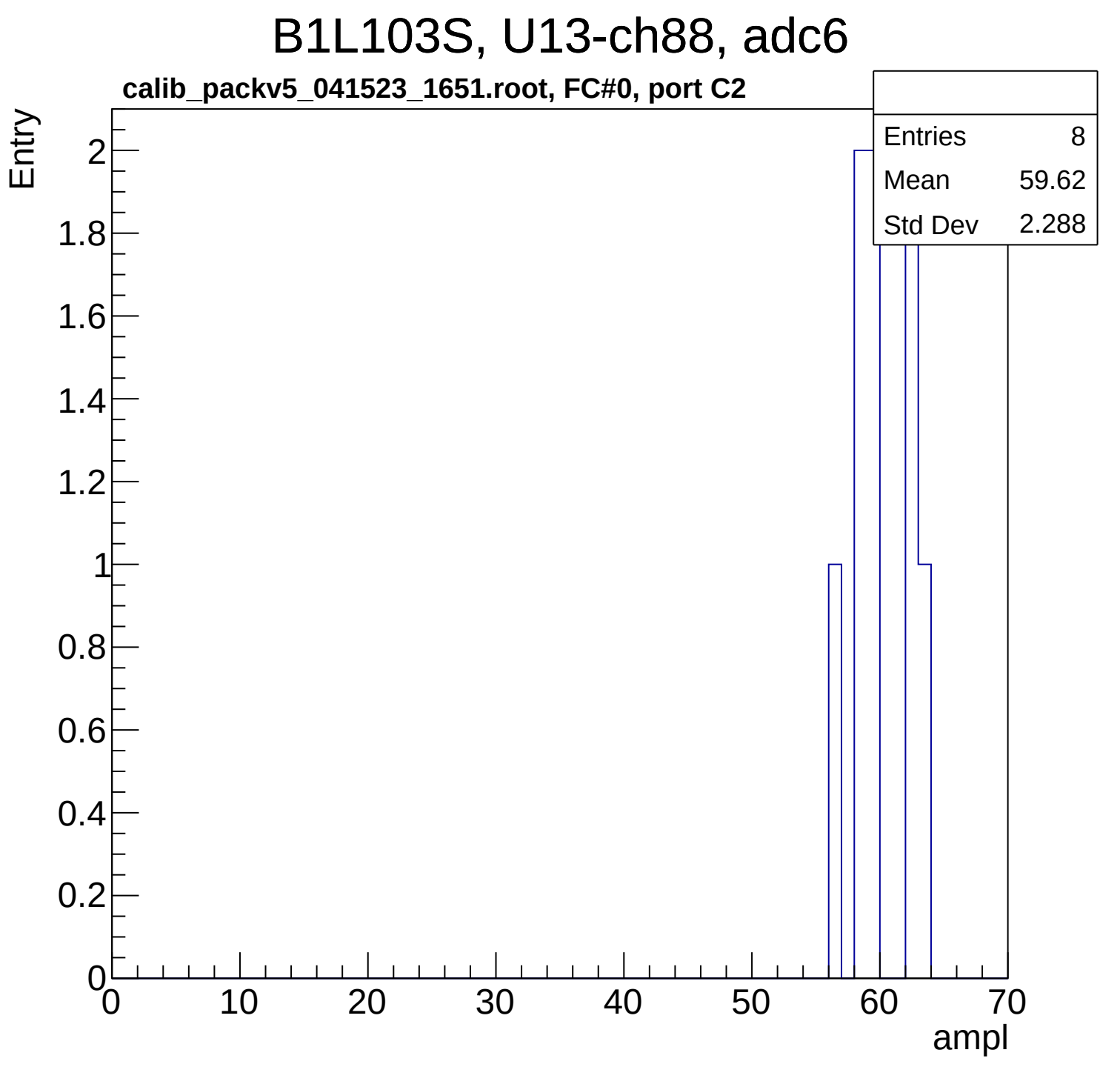
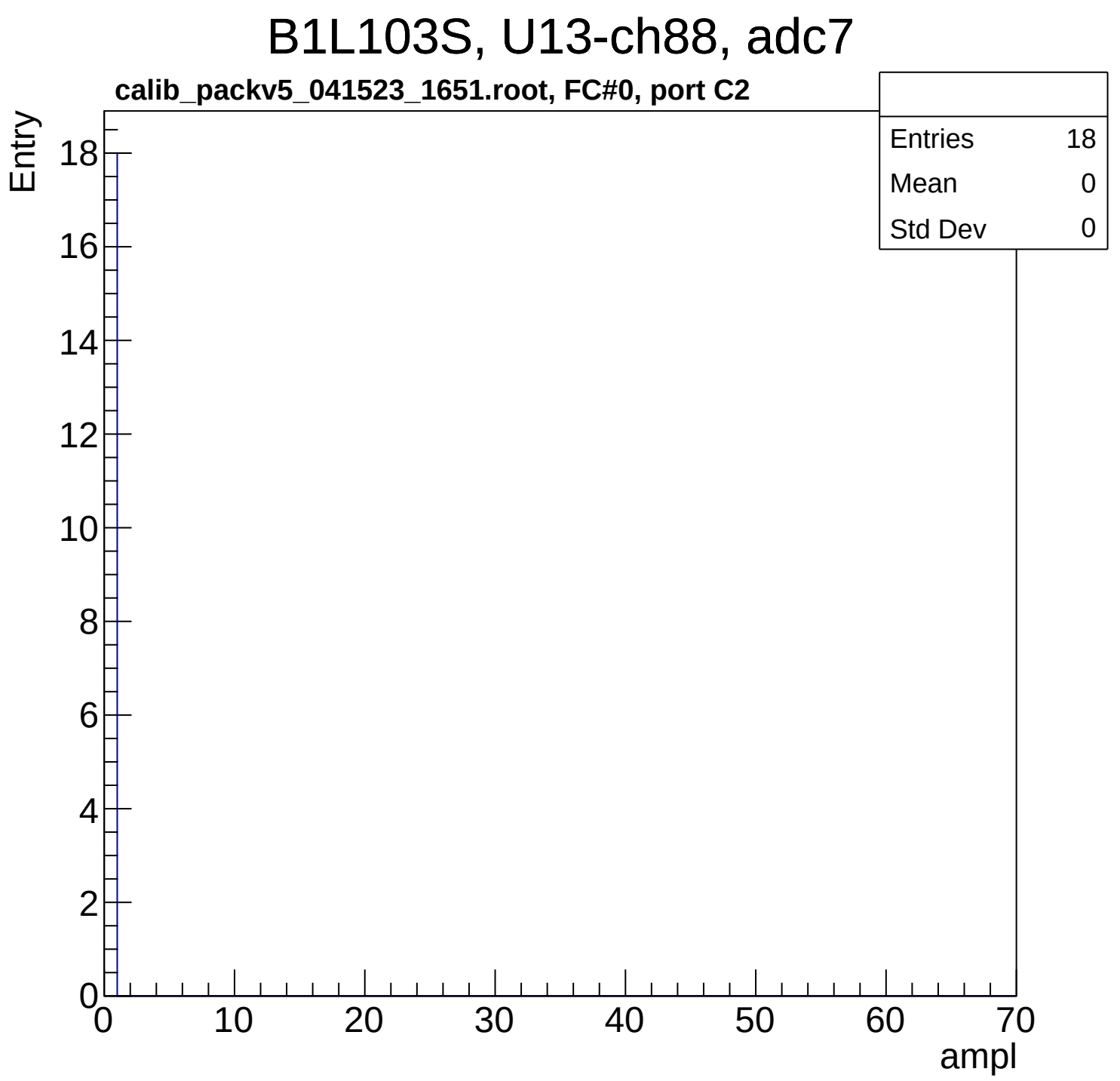
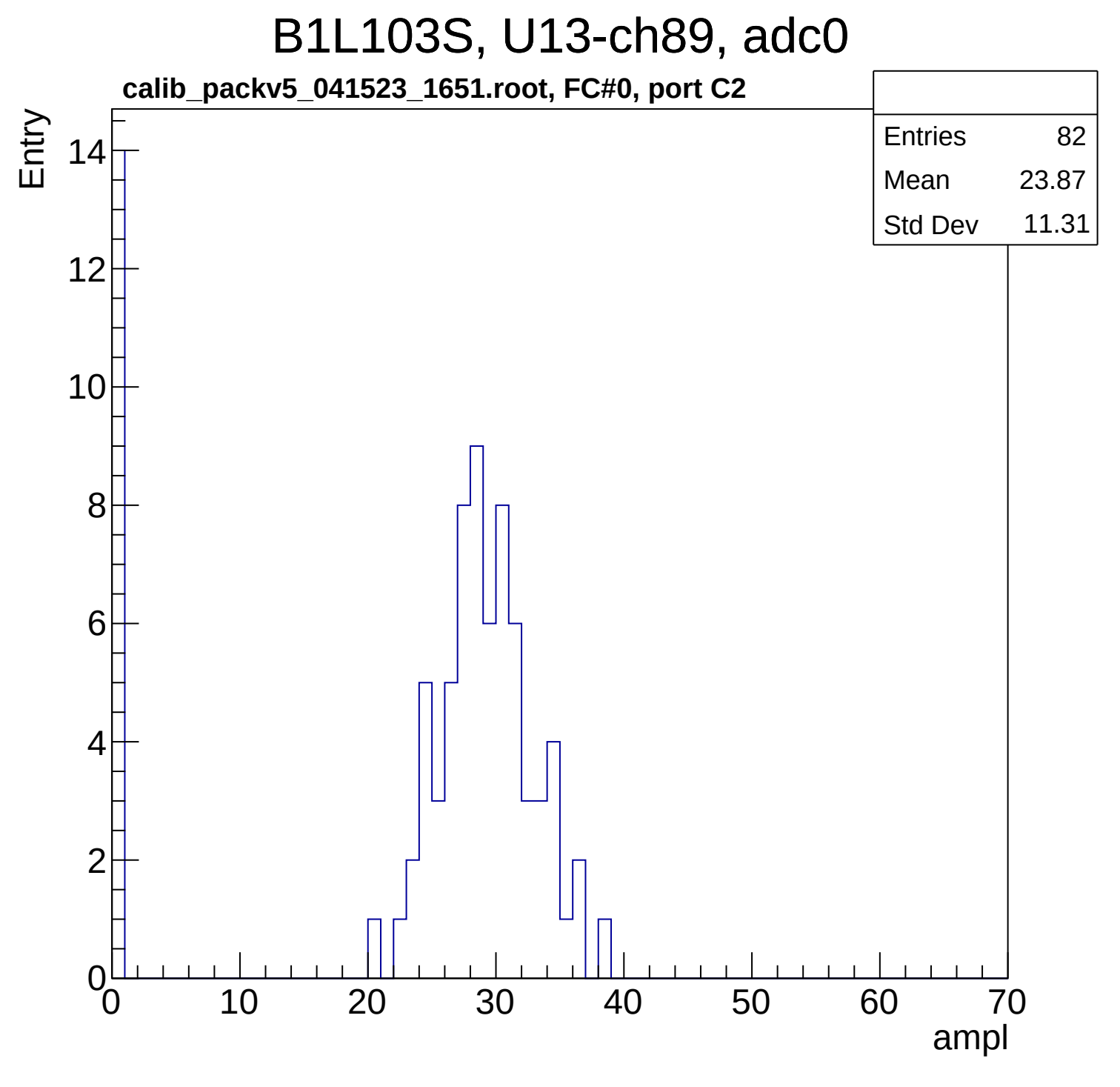
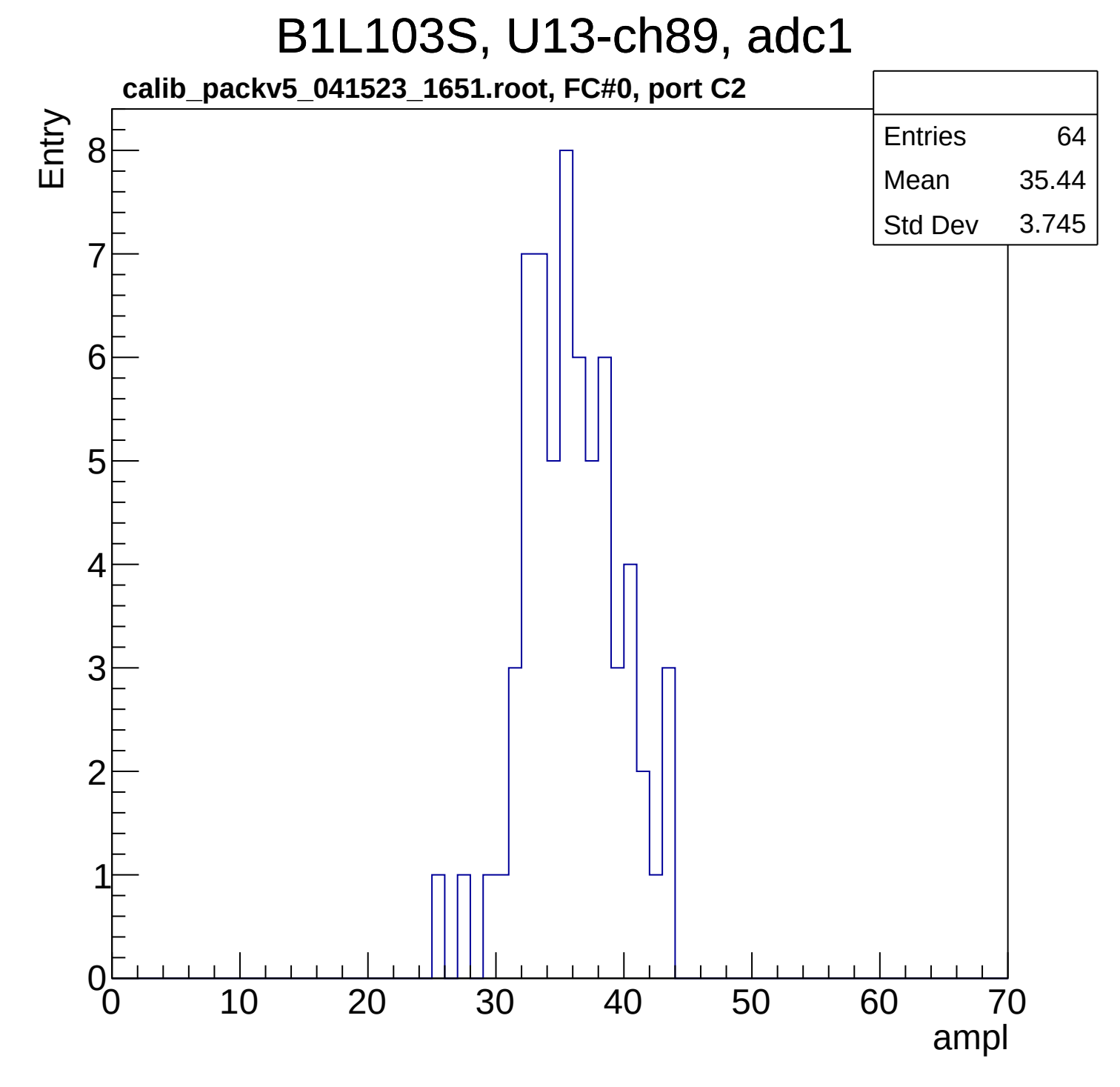
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch88, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.4
Std Dev 8.555
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch88, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 59.62
Std Dev 2.288
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U13-ch88, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch89, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 23.87
Std Dev 11.31
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U13-ch89, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 35.44
Std Dev 3.745
Entry
ampl
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2
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4
5
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7
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0
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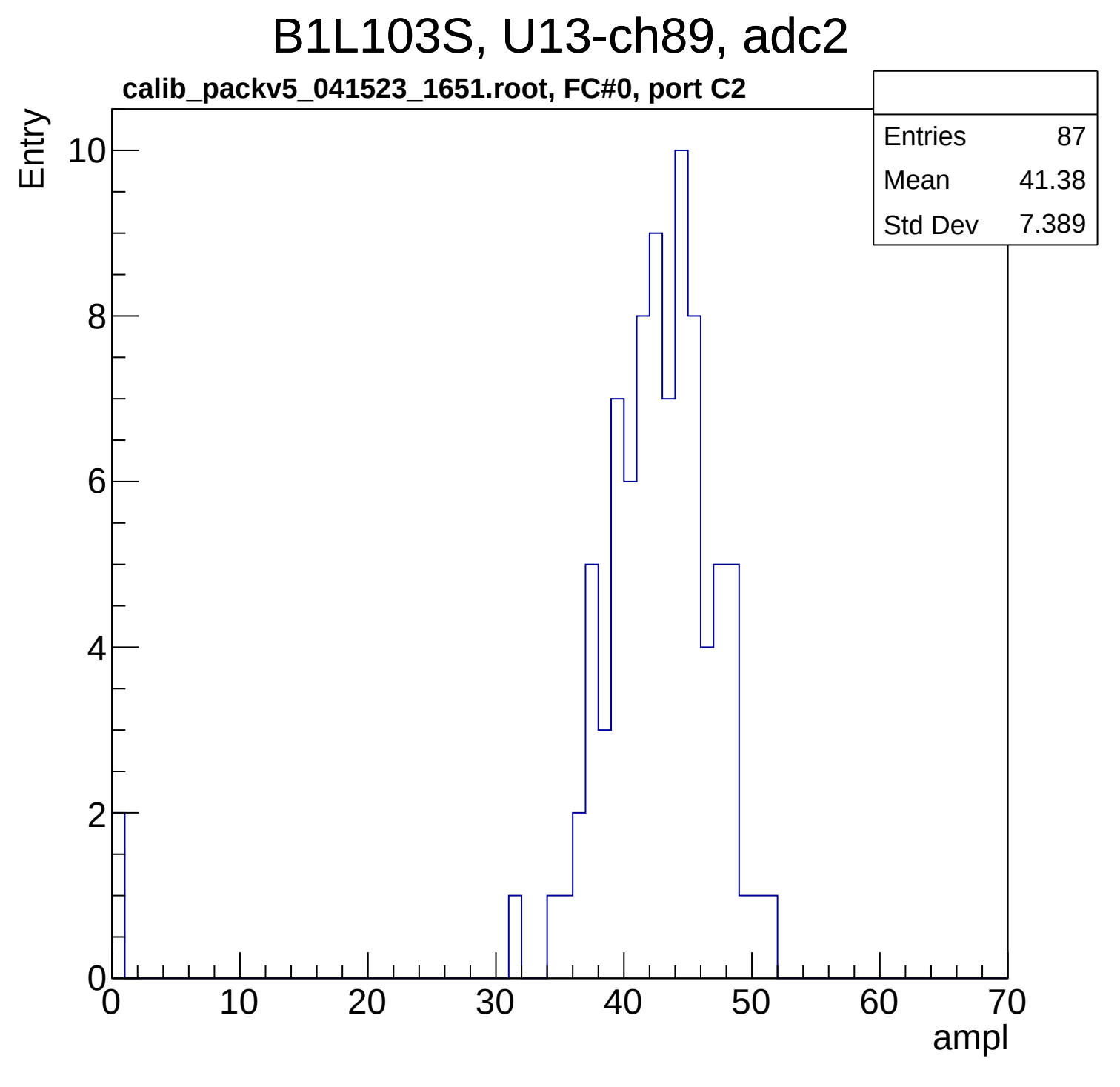
B1L103S, U13-ch89, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 41.38
Std Dev 7.389
Entry
ampl
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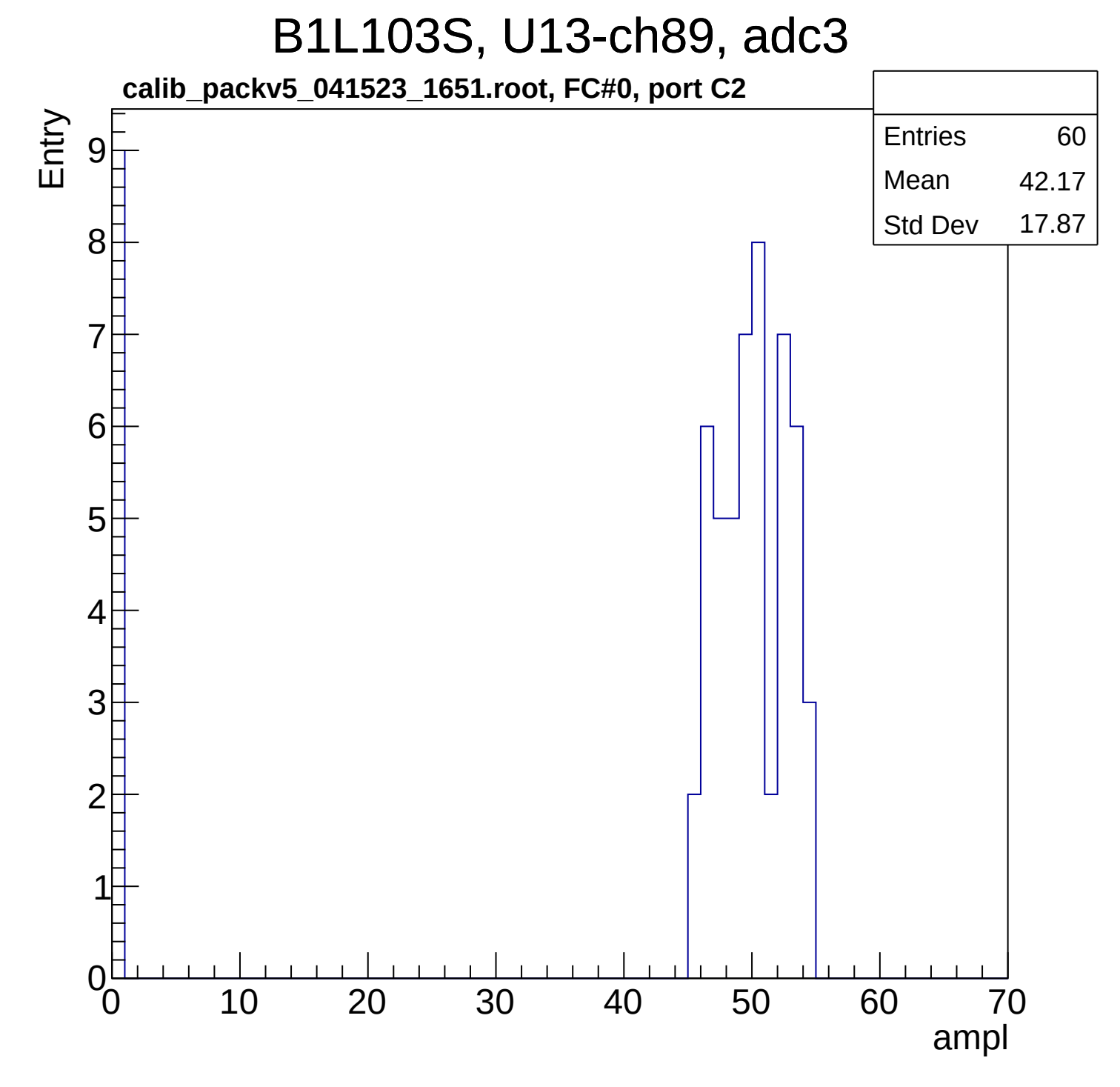
B1L103S, U13-ch89, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 42.17
Std Dev 17.87
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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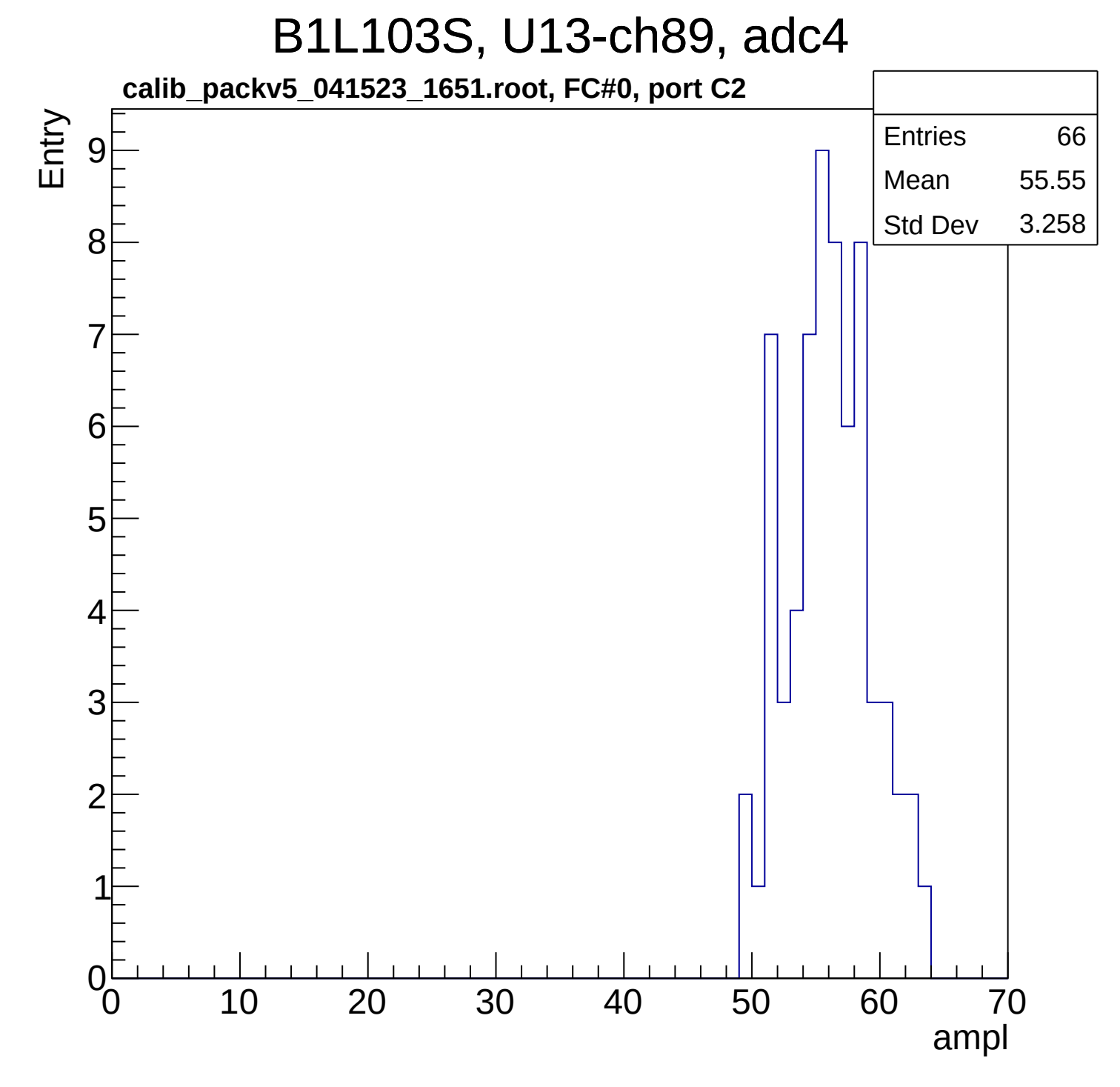
B1L103S, U13-ch89, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 55.55
Std Dev 3.258
Entry
ampl
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3
4
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0
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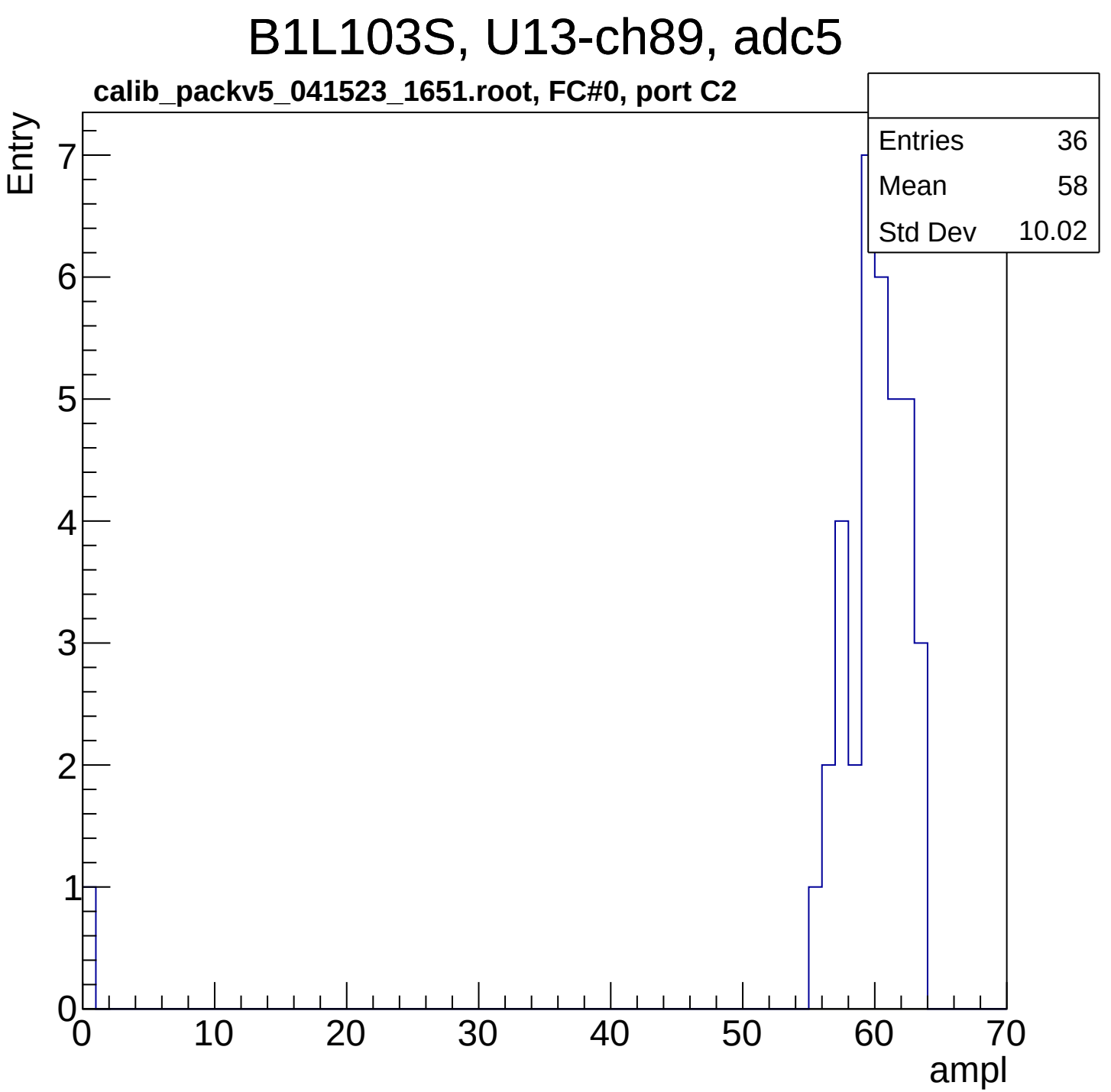
B1L103S, U13-ch89, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 58
Std Dev 10.02
Entry
ampl
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1
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0
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60
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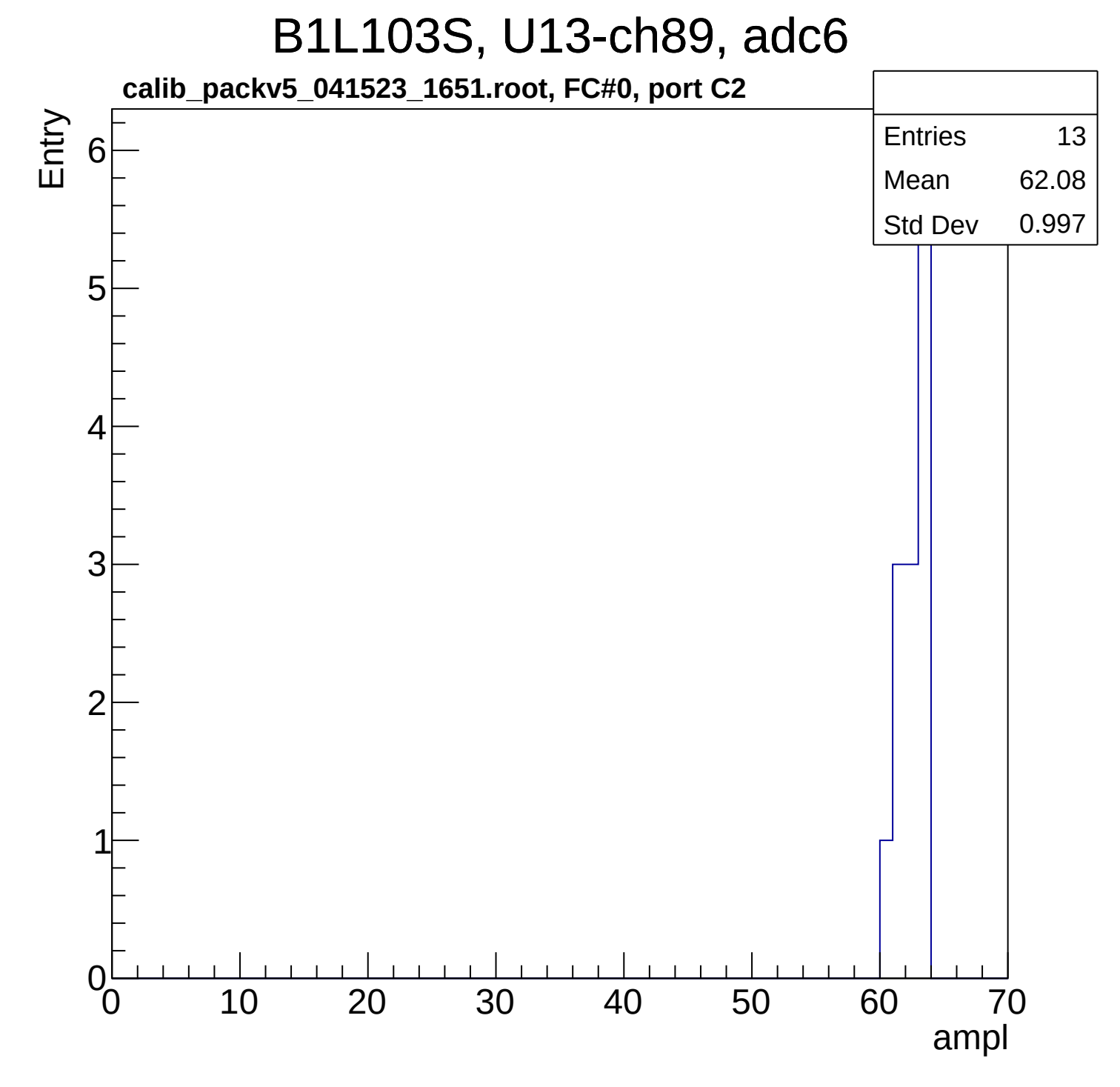
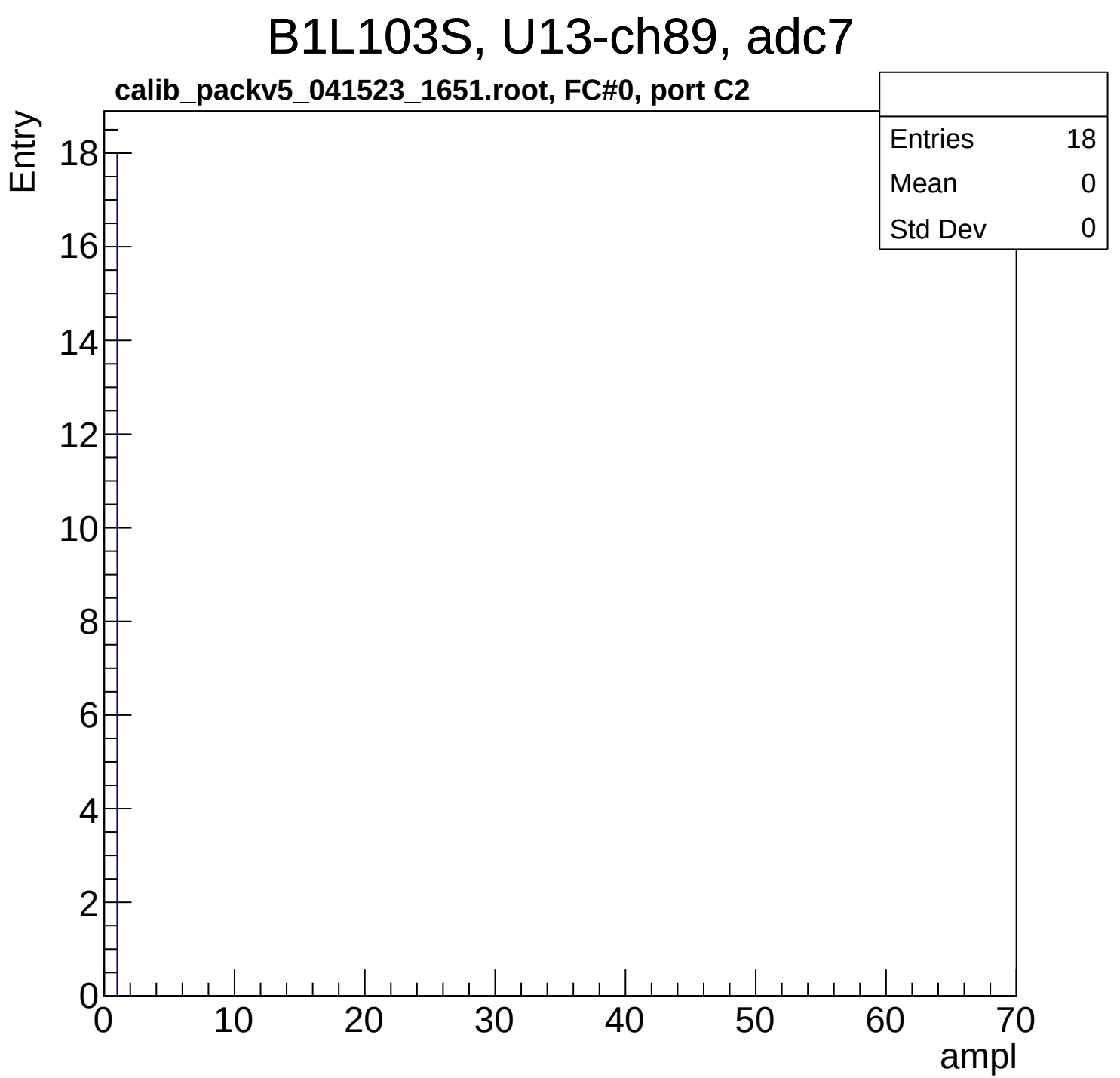
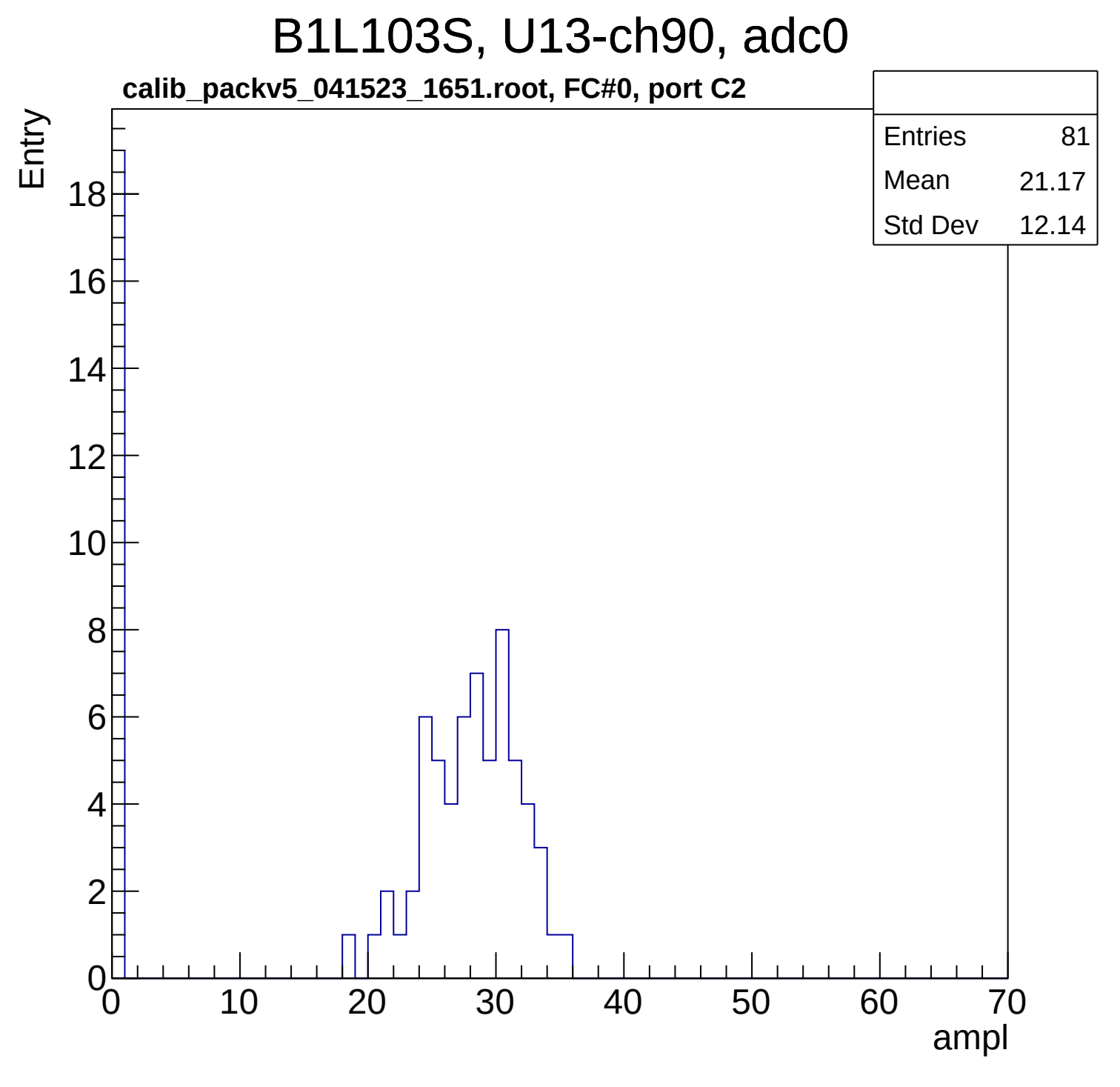

B1L103S, U13-ch89, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 62.08
Std Dev 0.997
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch89, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch90, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 21.17
Std Dev 12.14
Entry
0
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6
8
10
12
14
16
18
0
10
20
30
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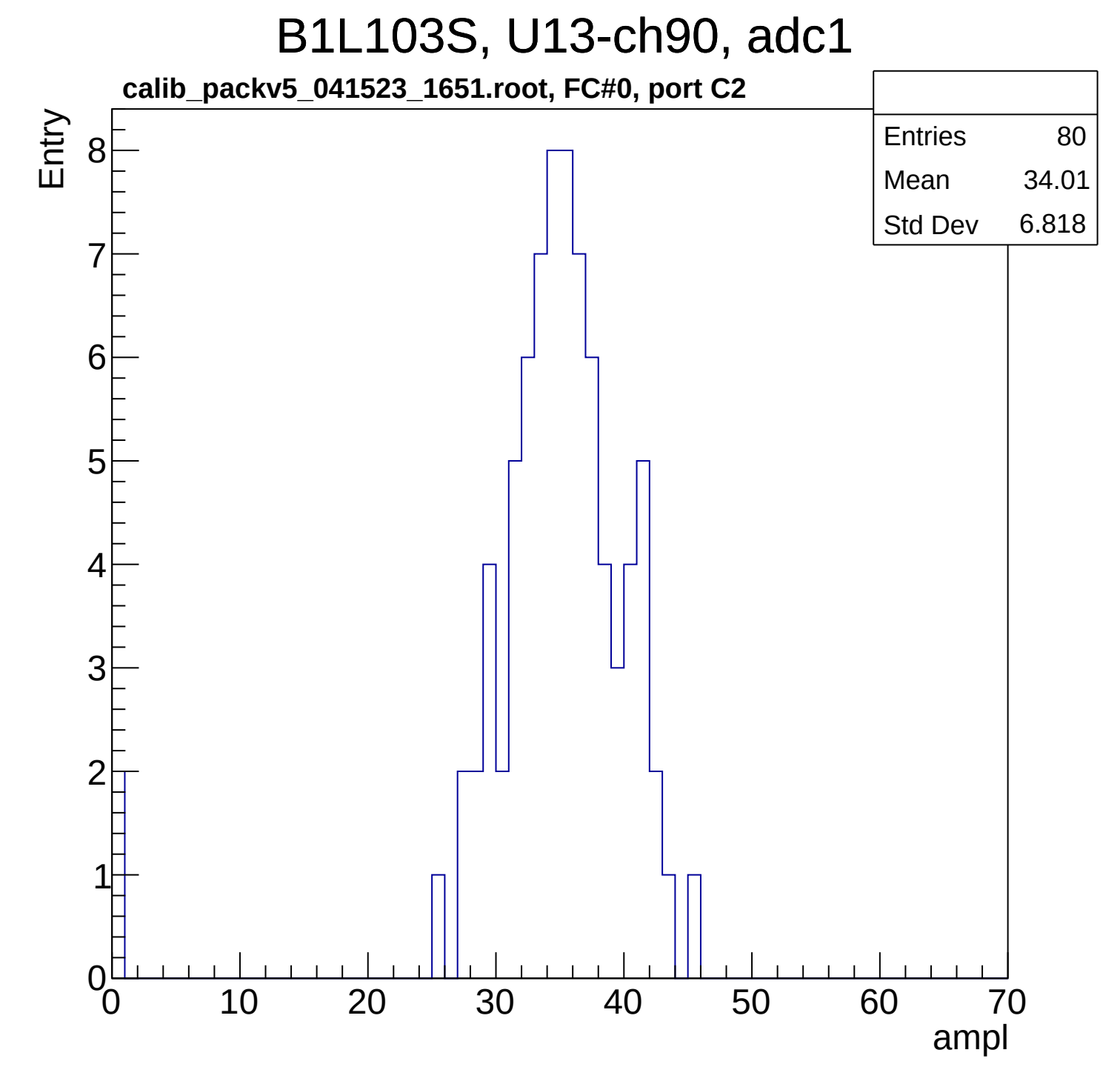
50
60
70
ampl


B1L103S, U13-ch90, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 34.01
Std Dev 6.818
Entry
ampl
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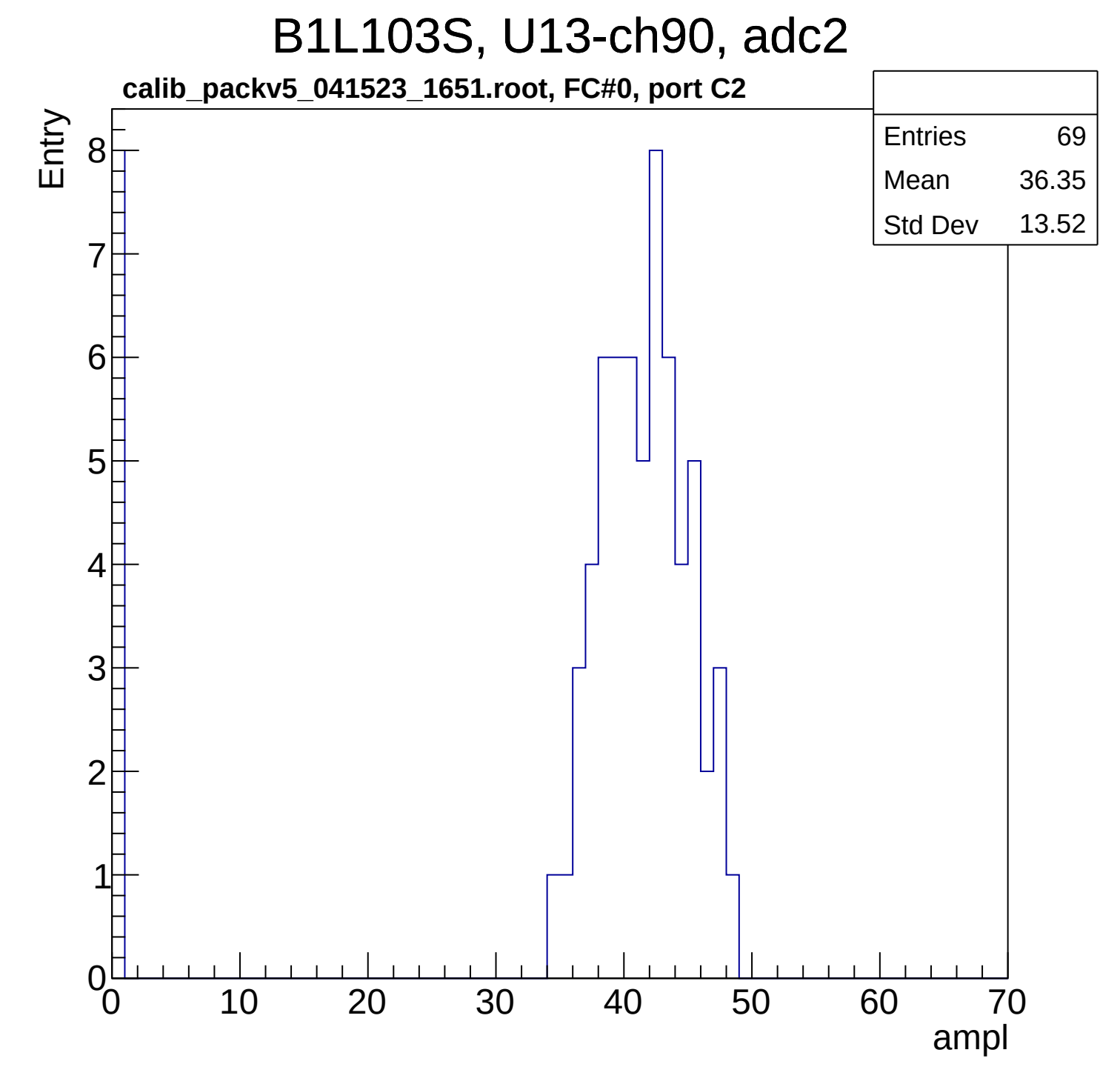
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch90, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 36.35
Std Dev 13.52
Entry
ampl
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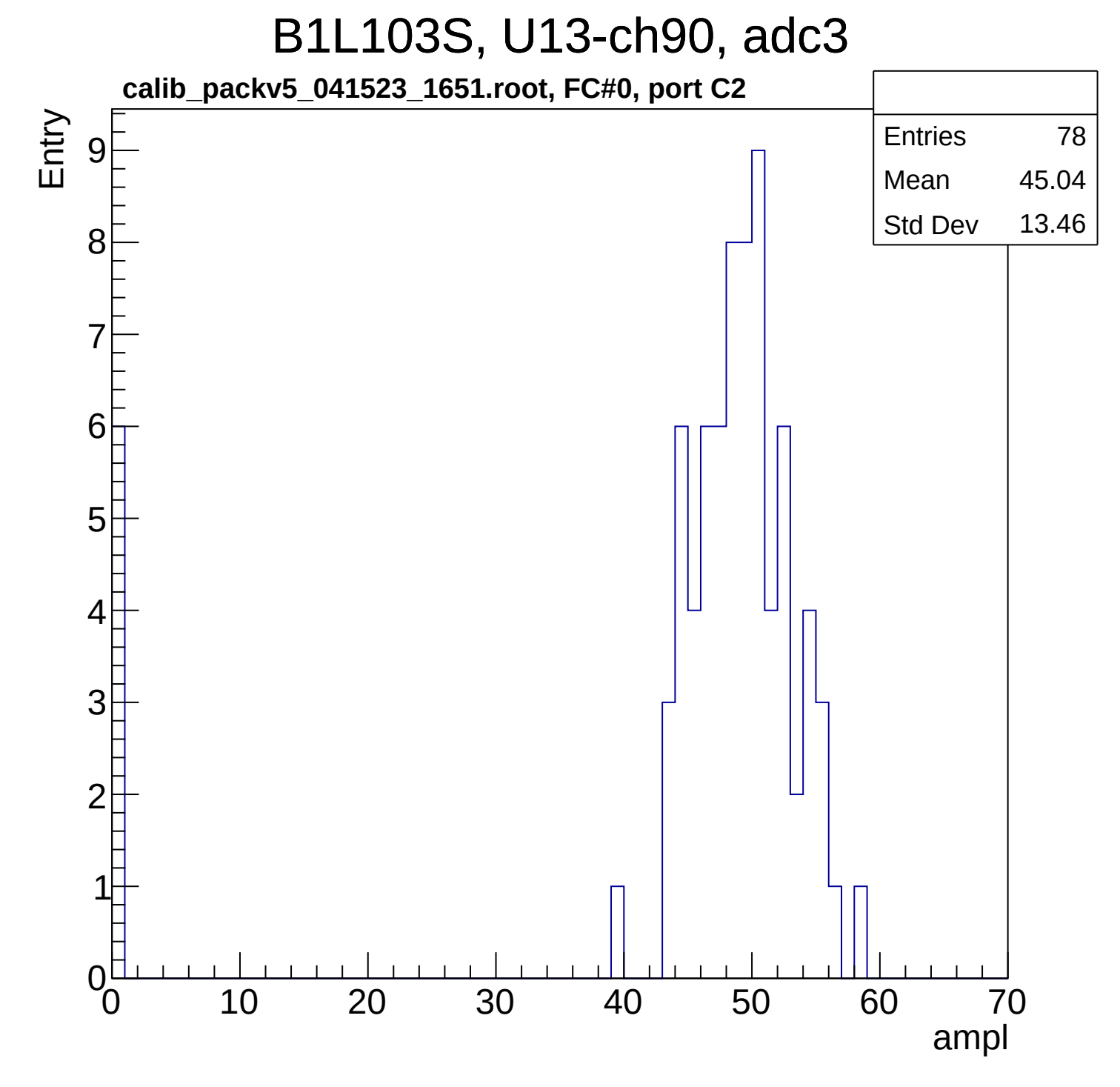
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch90, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 45.04
Std Dev 13.46
Entry
ampl
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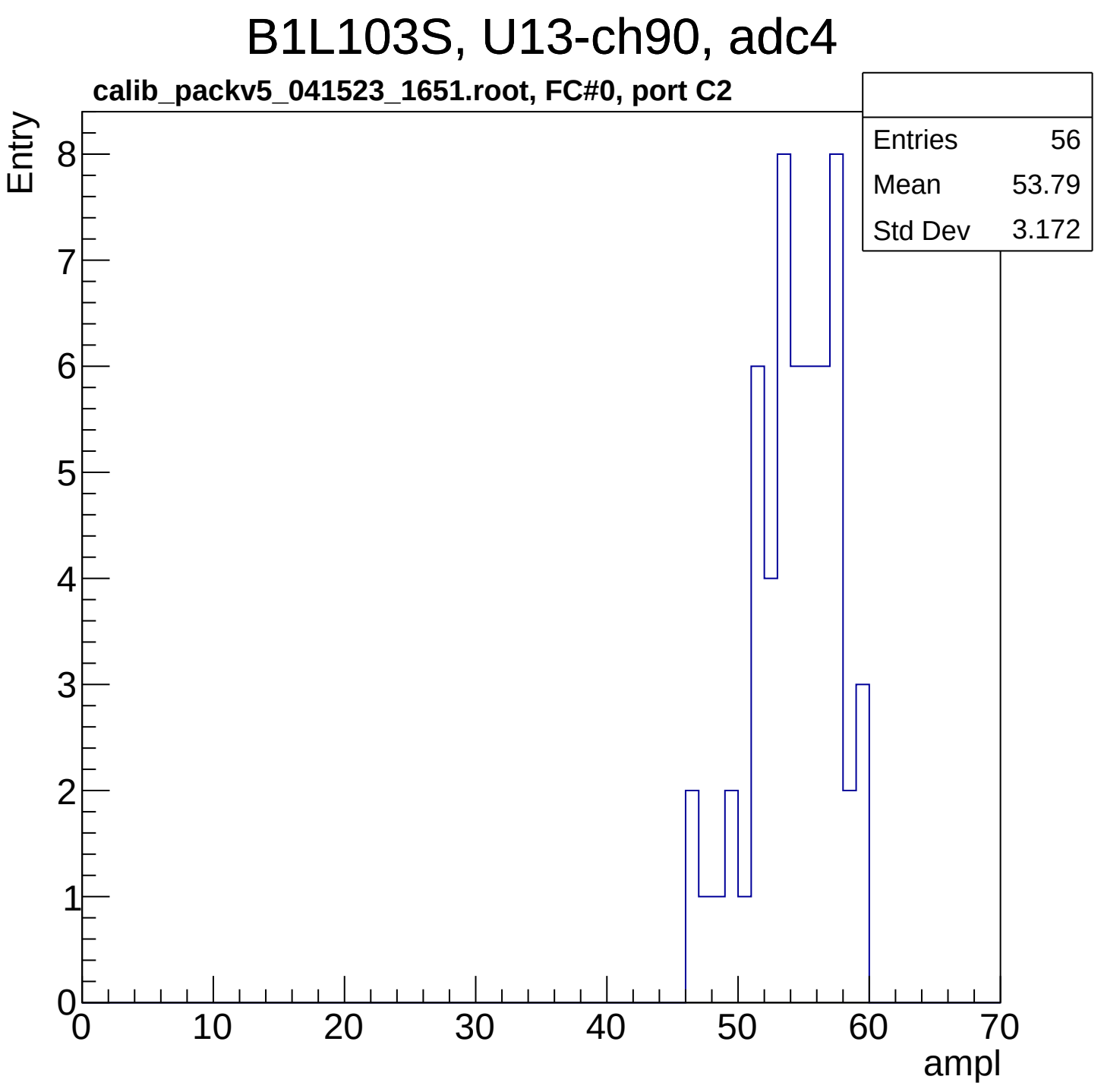
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch90, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 53.79
Std Dev 3.172
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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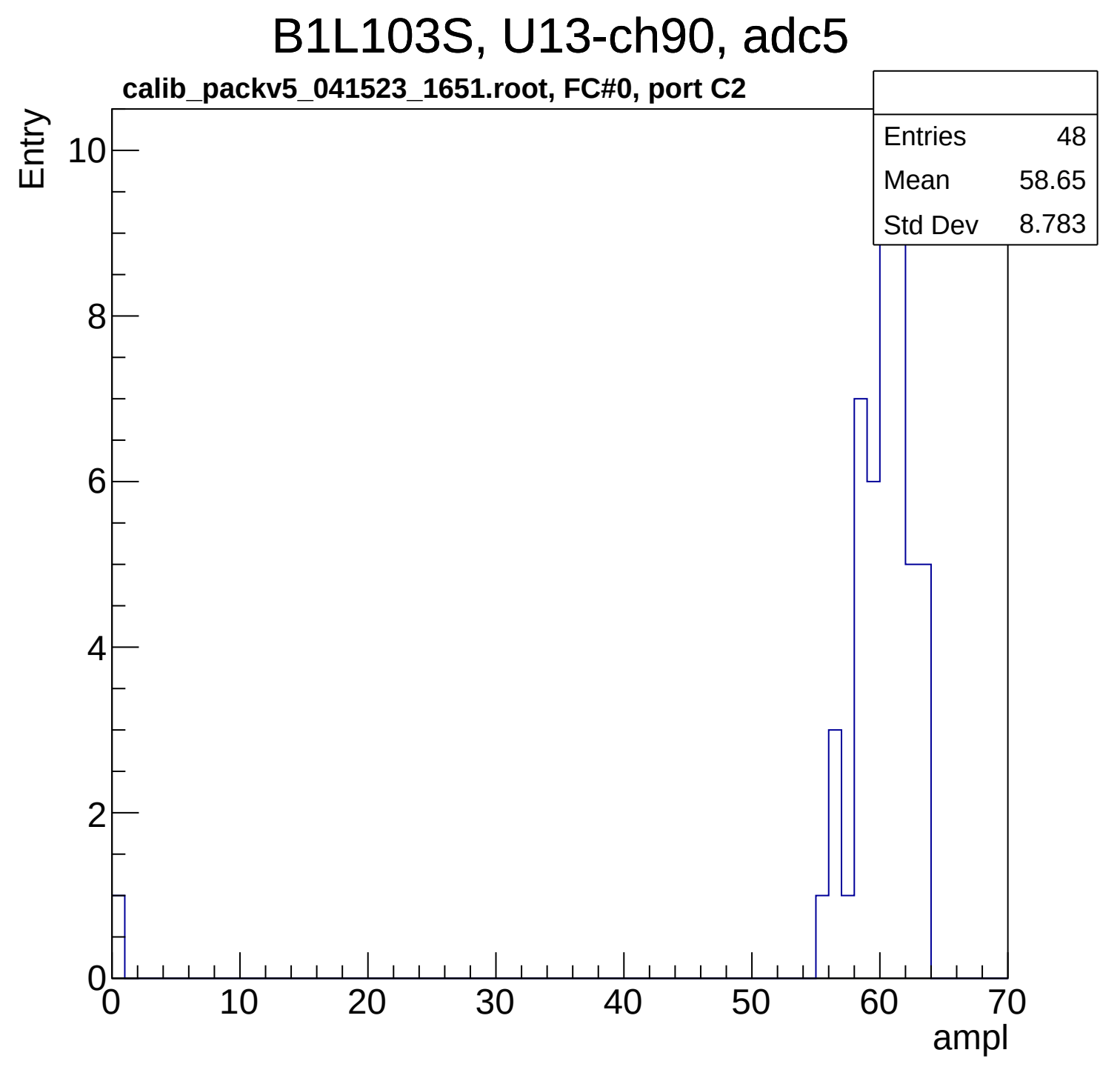
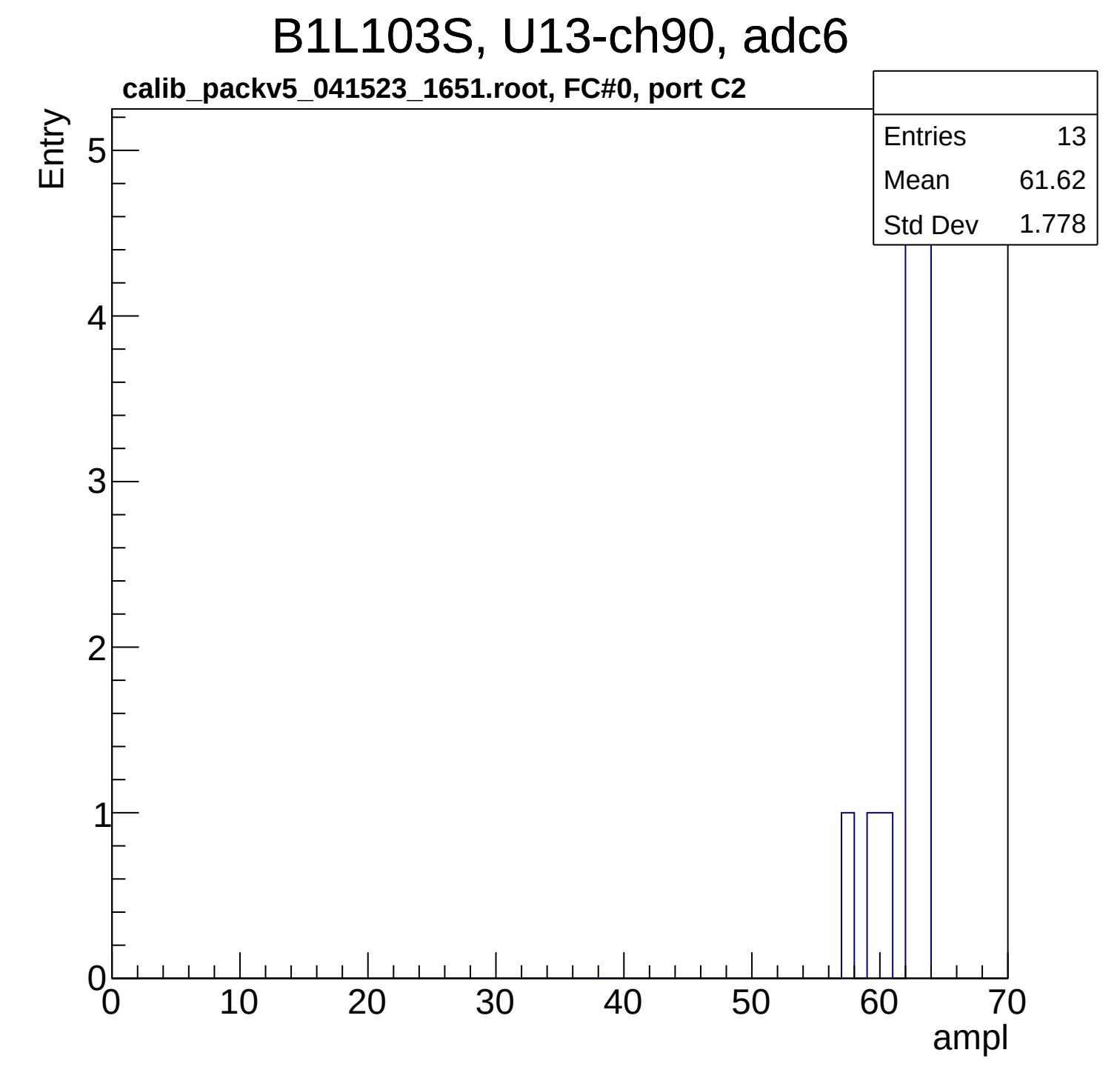
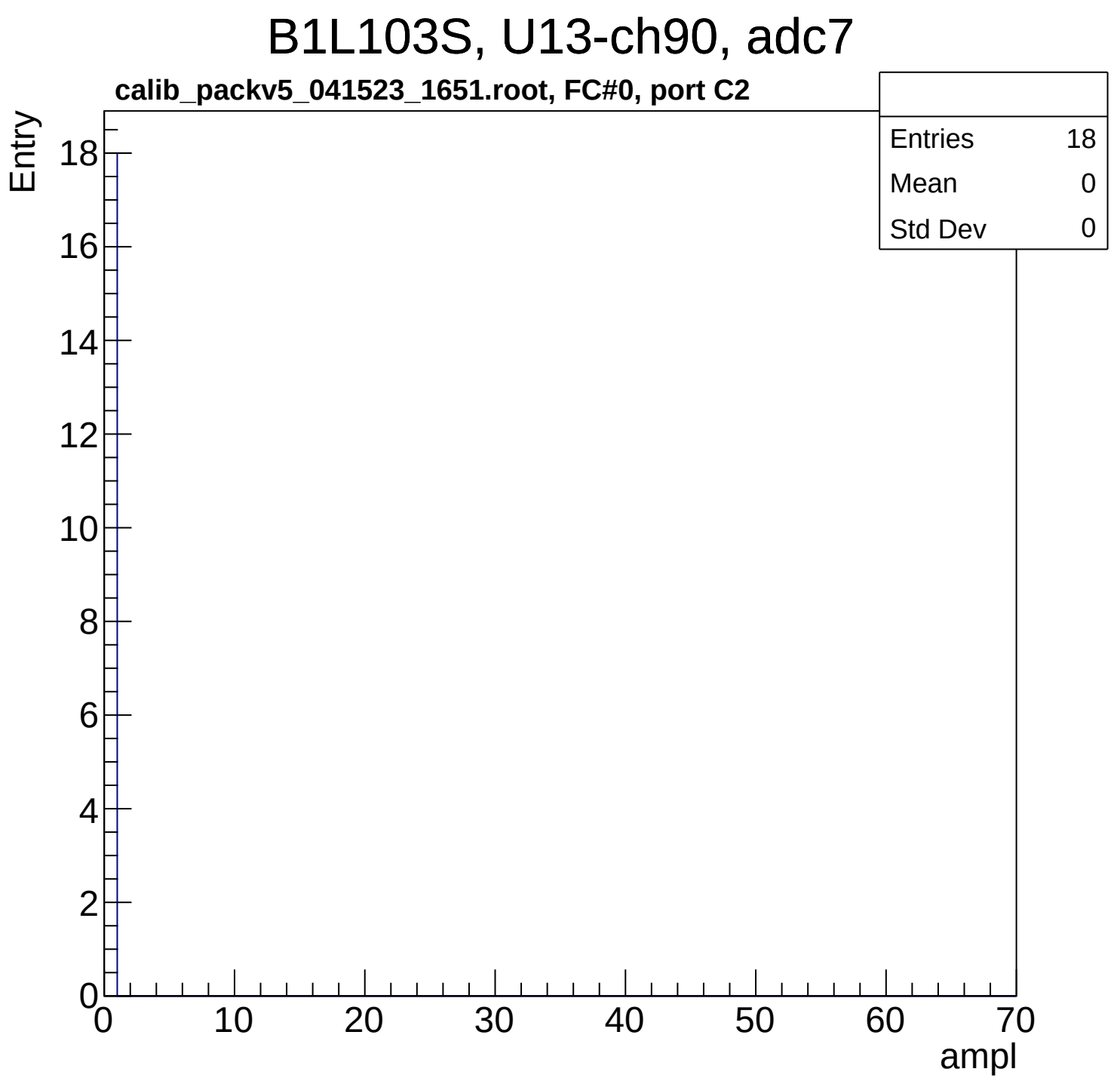
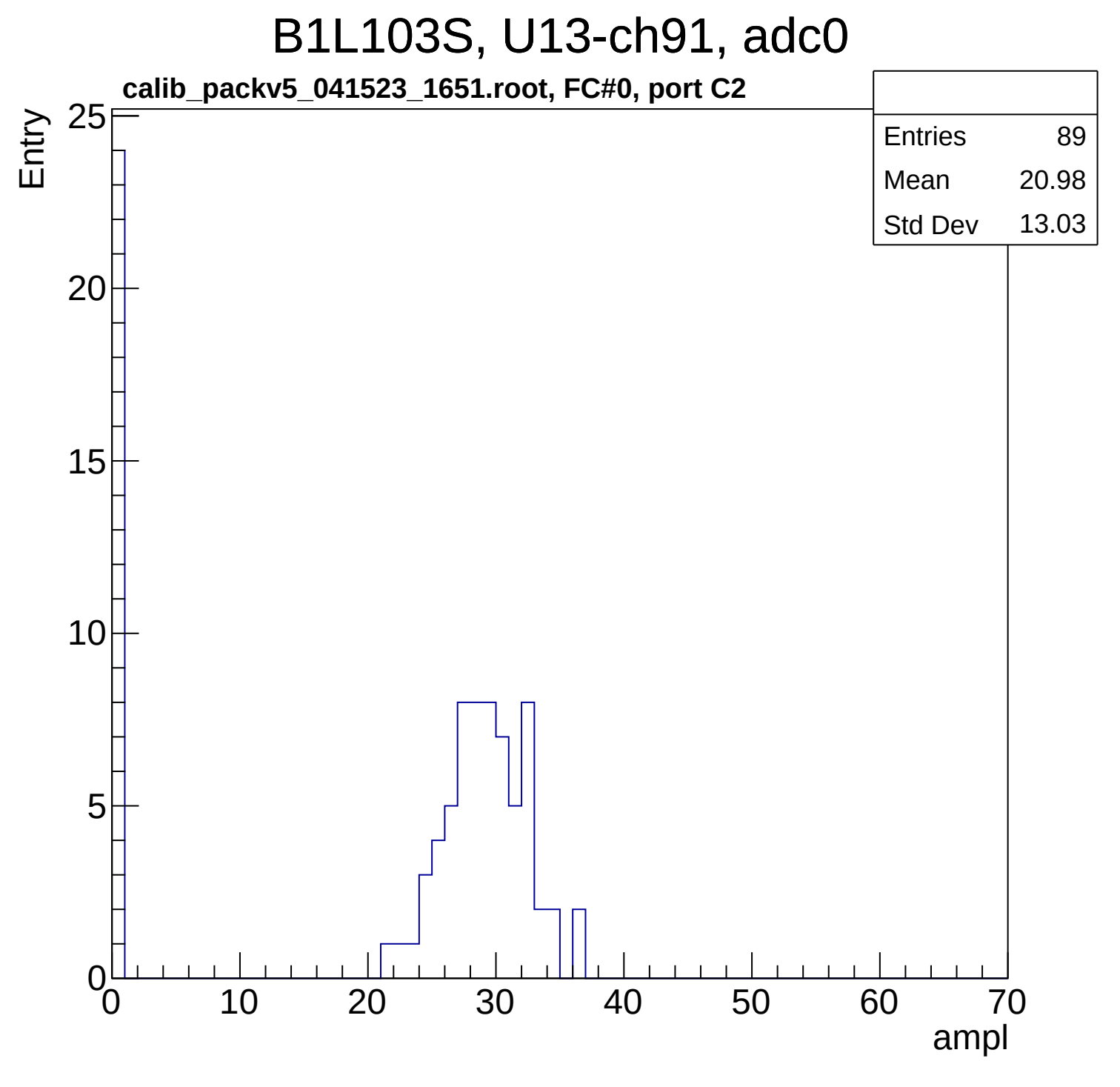
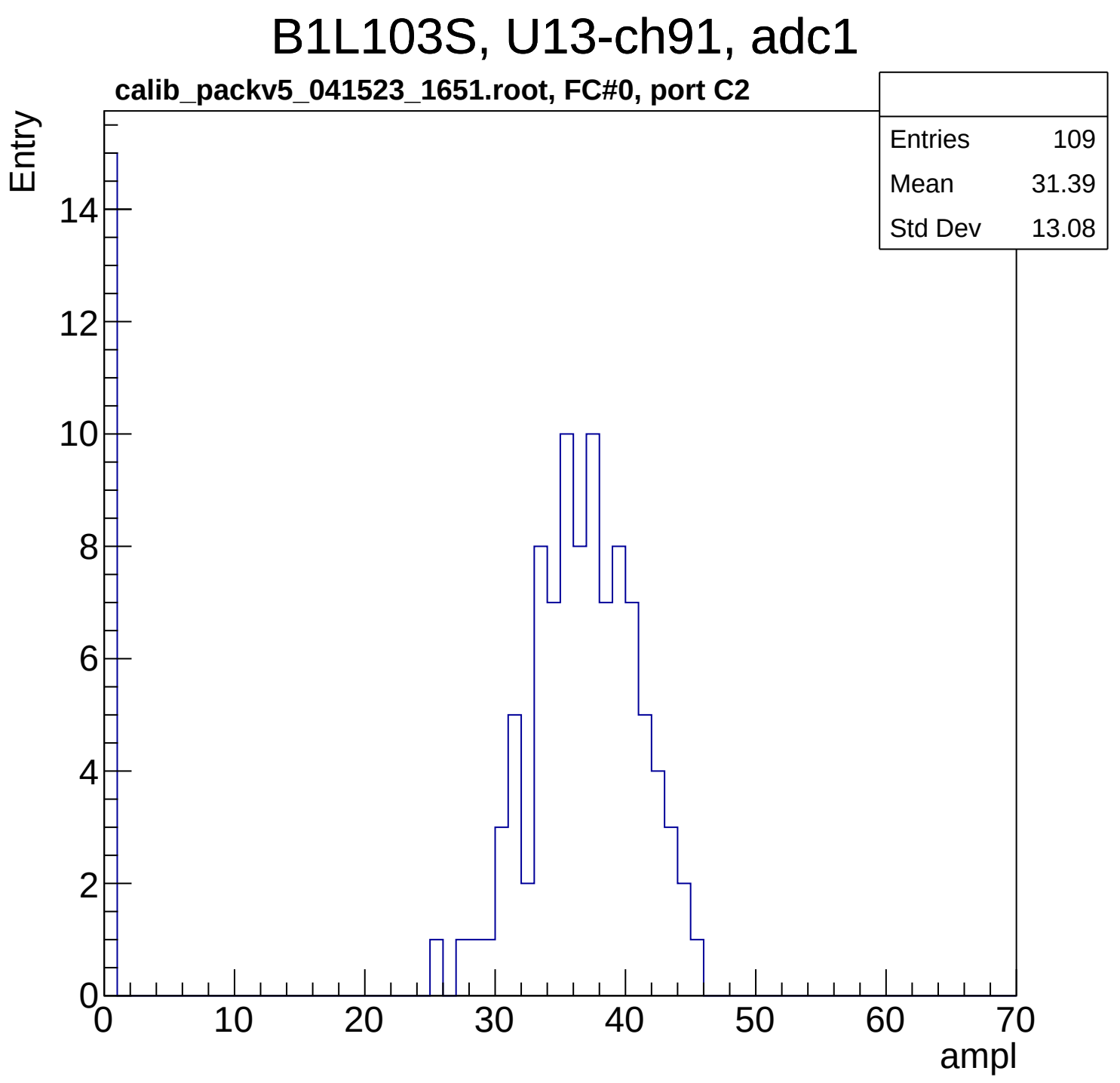

B1L103S, U13-ch90, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.65
Std Dev 8.783
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch90, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.62
Std Dev 1.778
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U13-ch90, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch91, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 20.98
Std Dev 13.03
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U13-ch91, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 109
Mean 31.39
Std Dev 13.08
Entry
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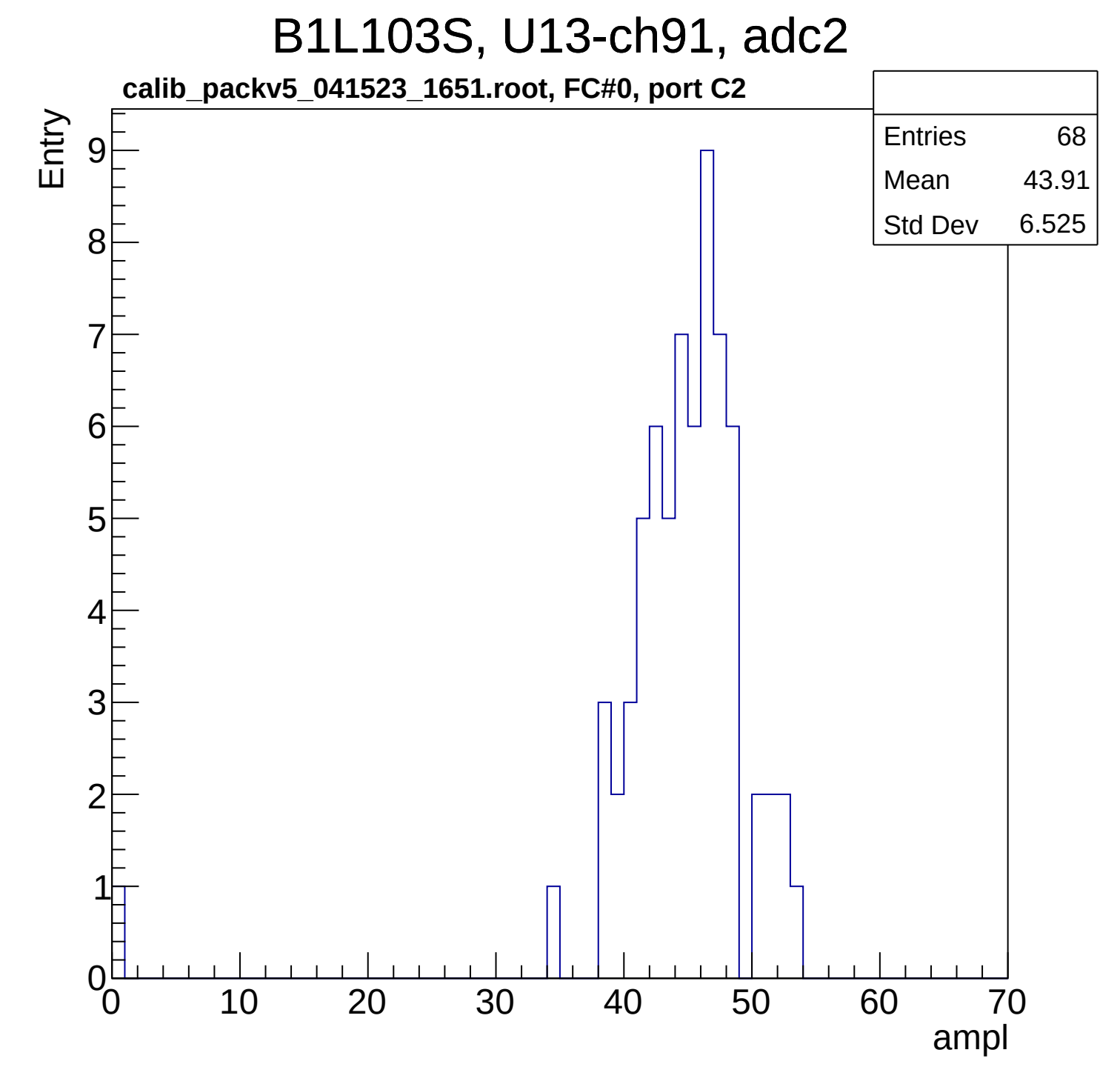
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch91, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 43.91
Std Dev 6.525
Entry
ampl
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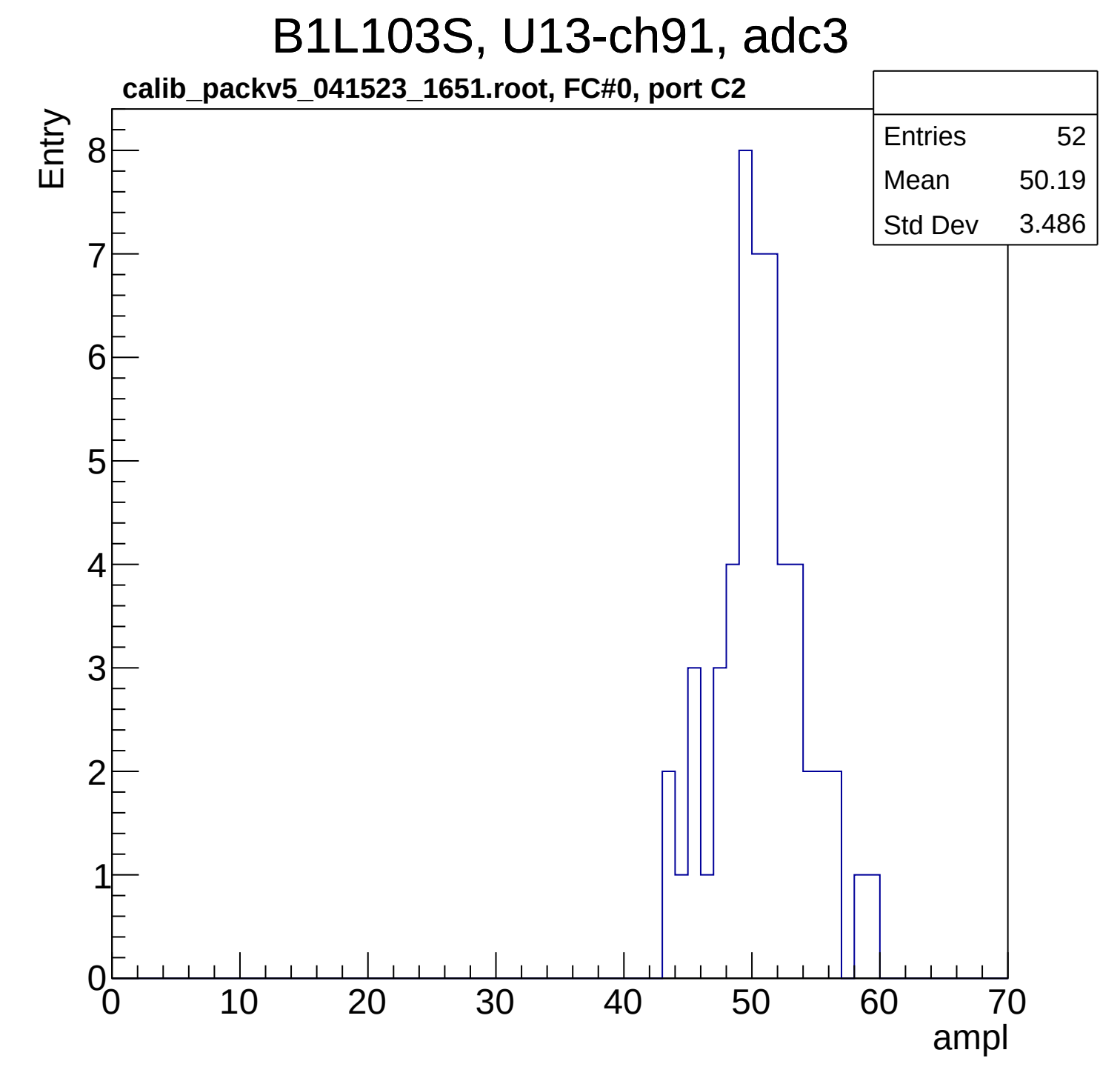
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch91, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 50.19
Std Dev 3.486
Entry
ampl
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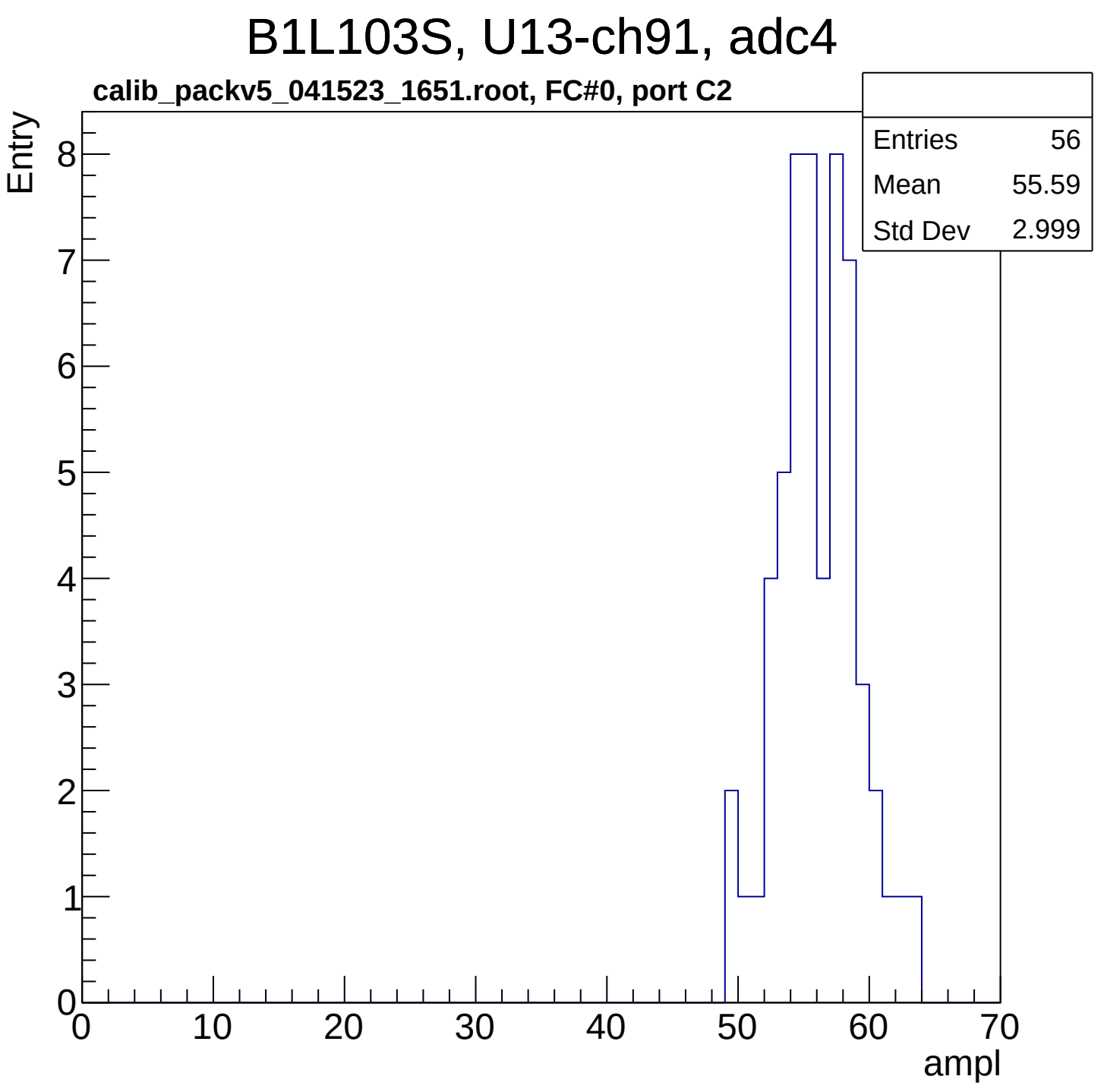
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch91, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 55.59
Std Dev 2.999
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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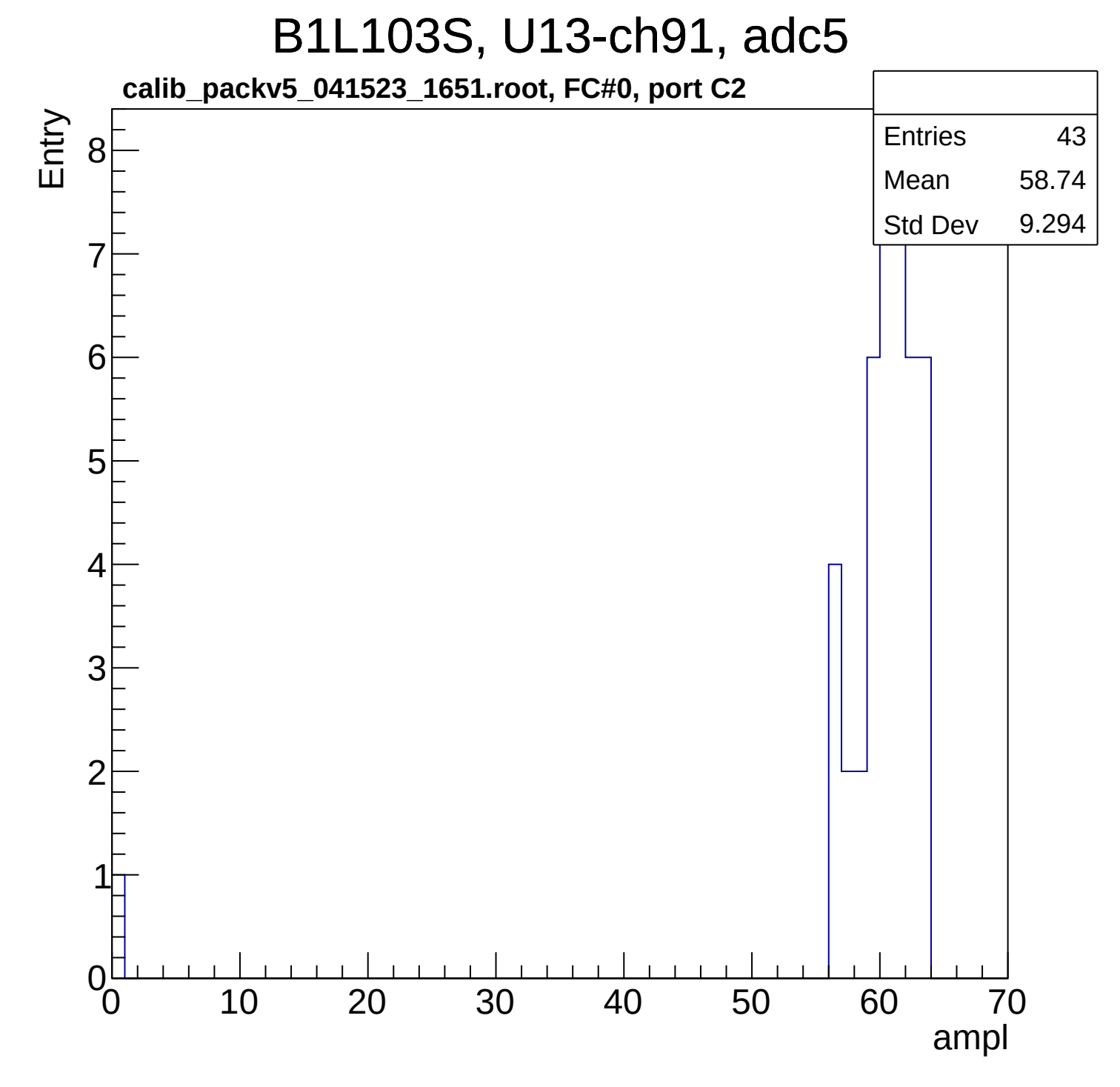
B1L103S, U13-ch91, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 58.74
Std Dev 9.294
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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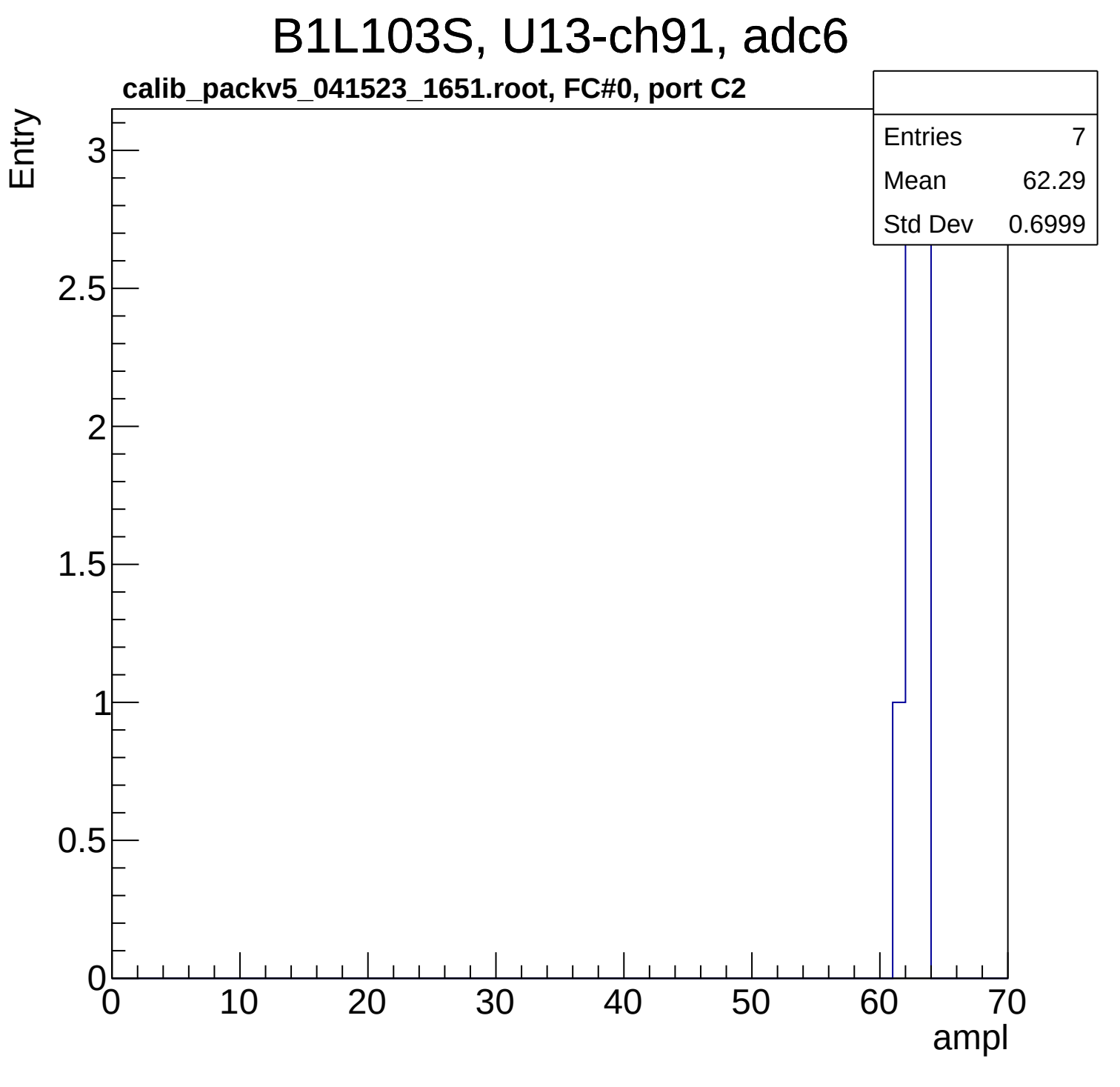
B1L103S, U13-ch91, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62.29
Std Dev 0.6999
Entry
ampl
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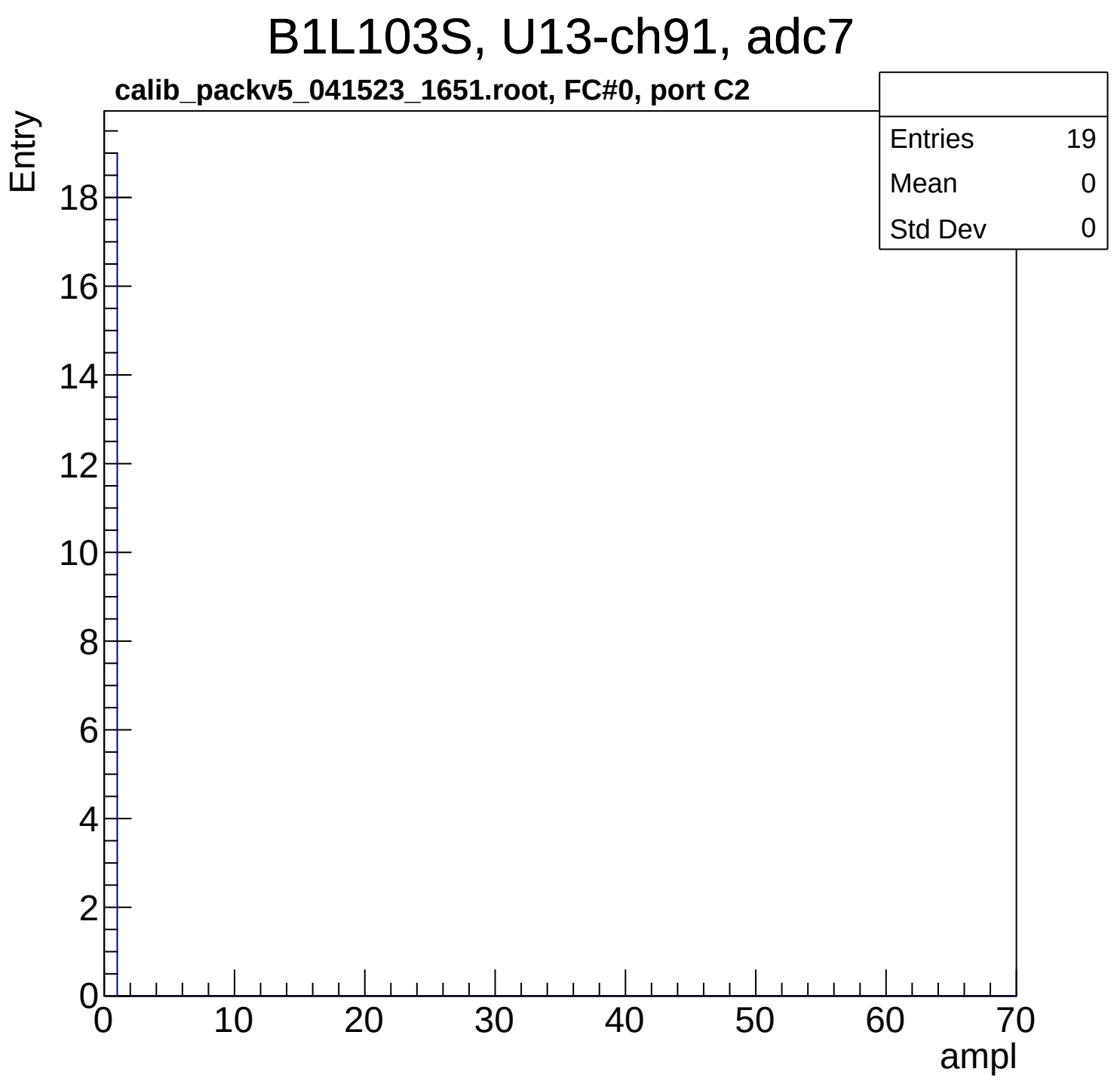
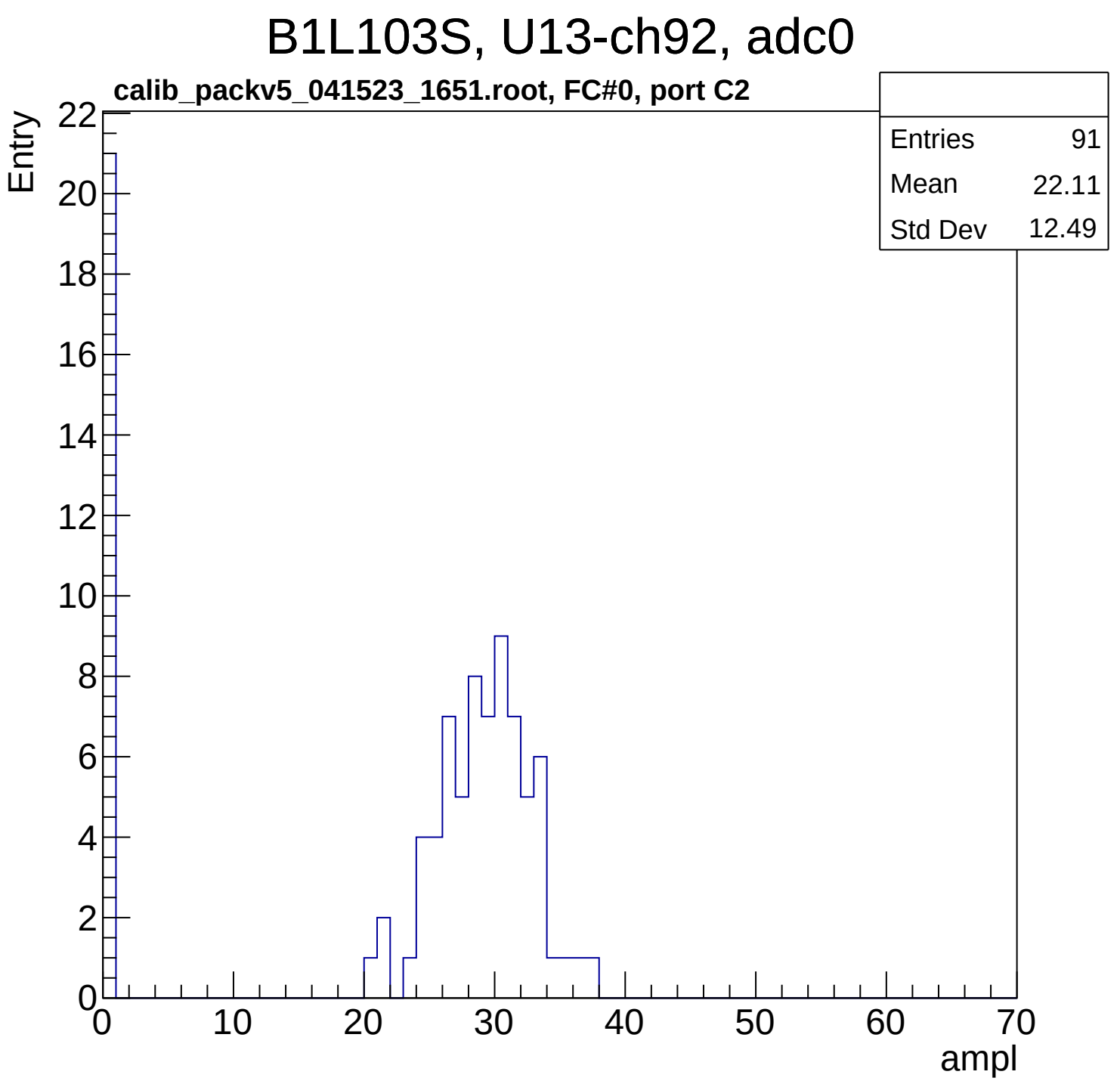
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U13-ch91, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch92, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 22.11
Std Dev 12.49
Entry
ampl
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8
10
12
14
16
18
20
22
0
10
20
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60
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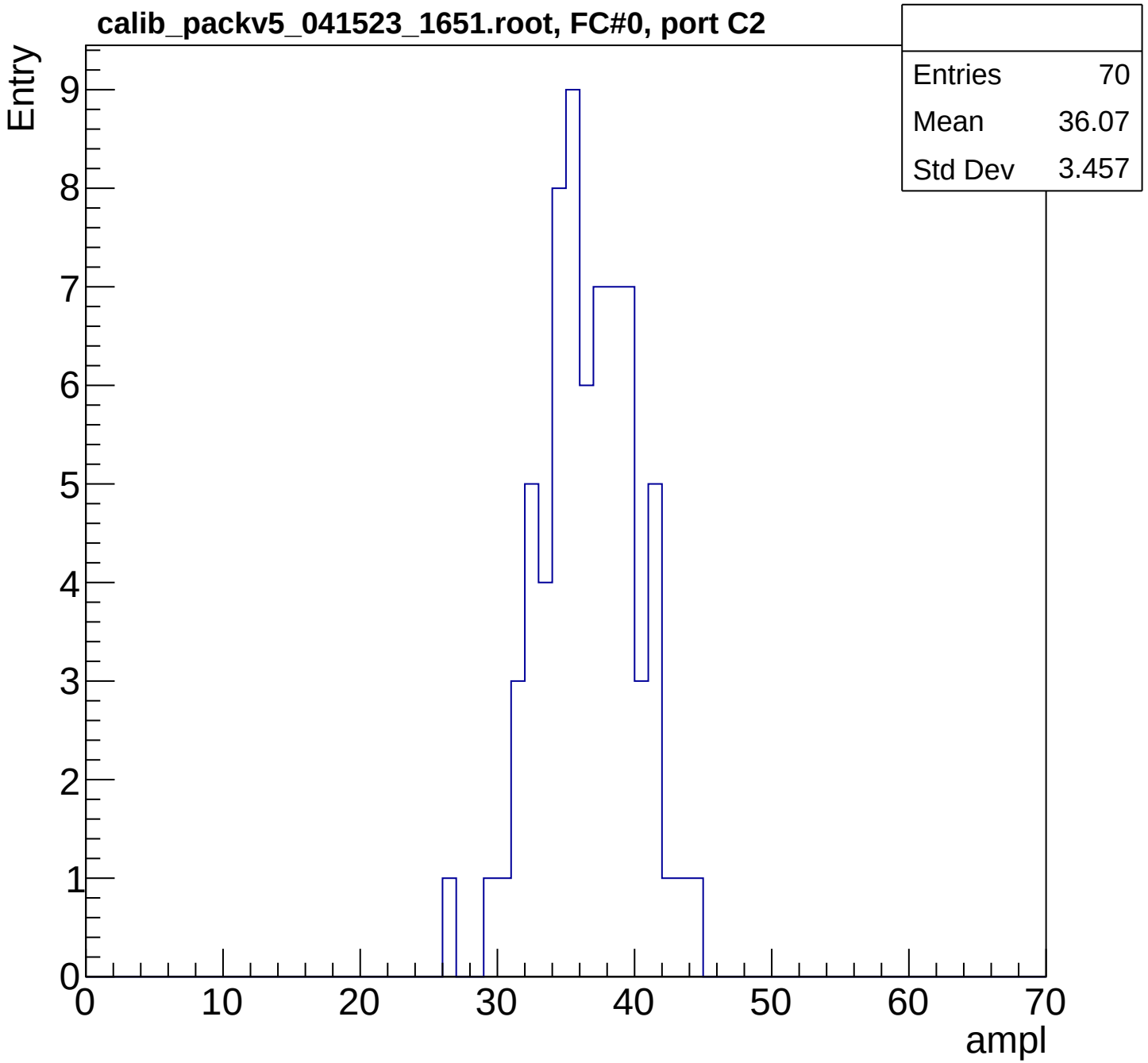
B1L103S, U13-ch92, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 36.07
Std Dev 3.457
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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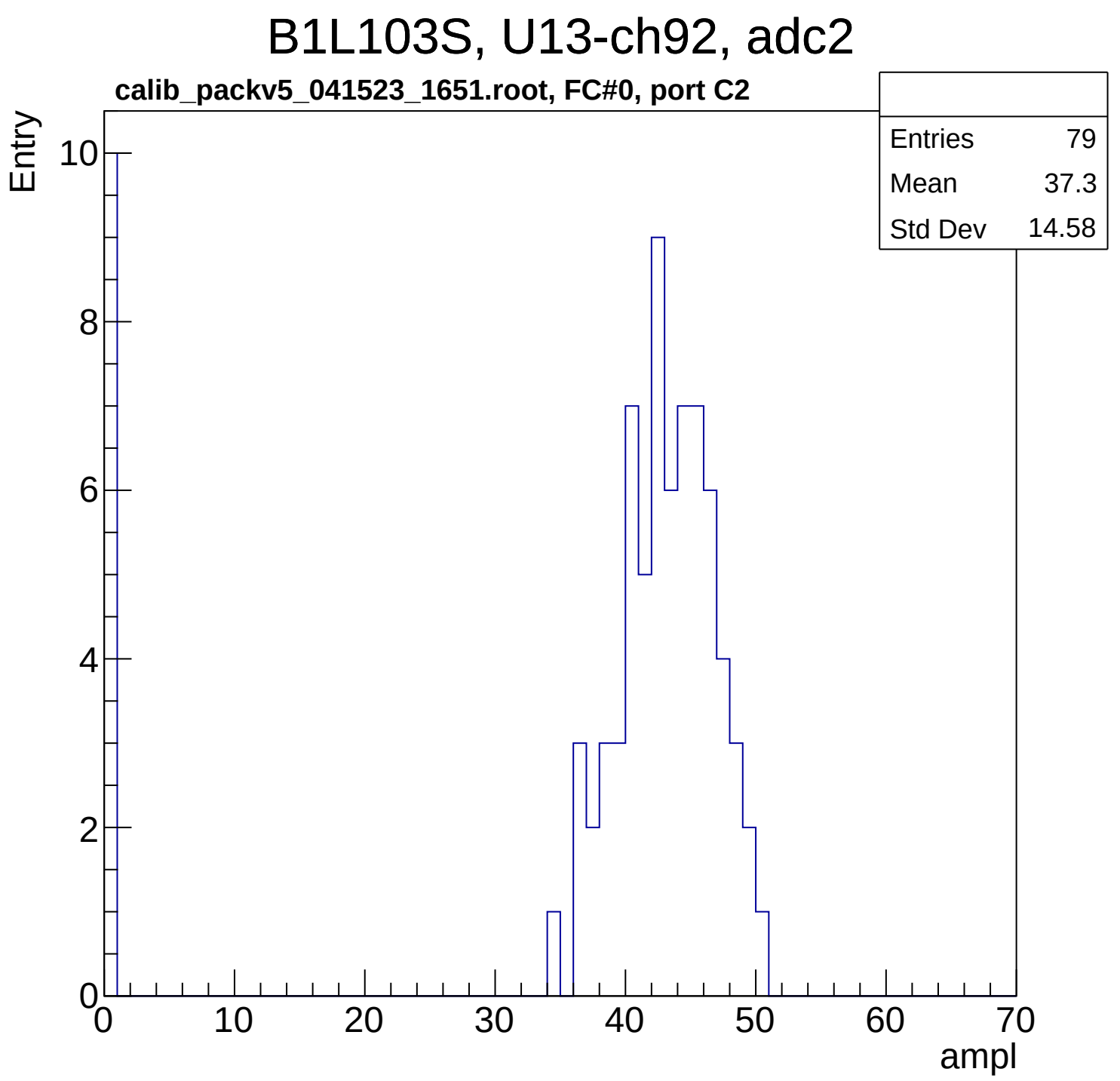
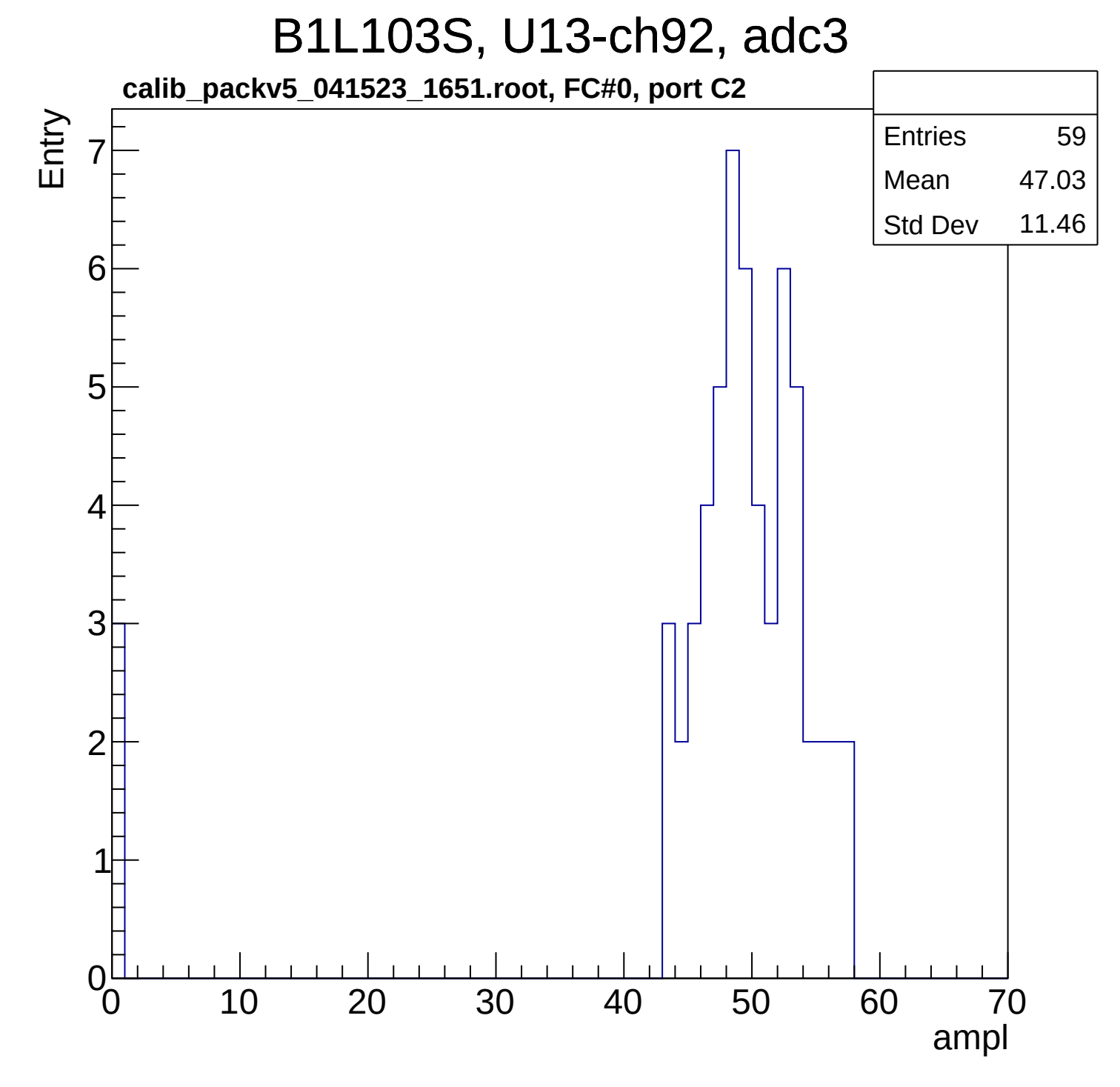
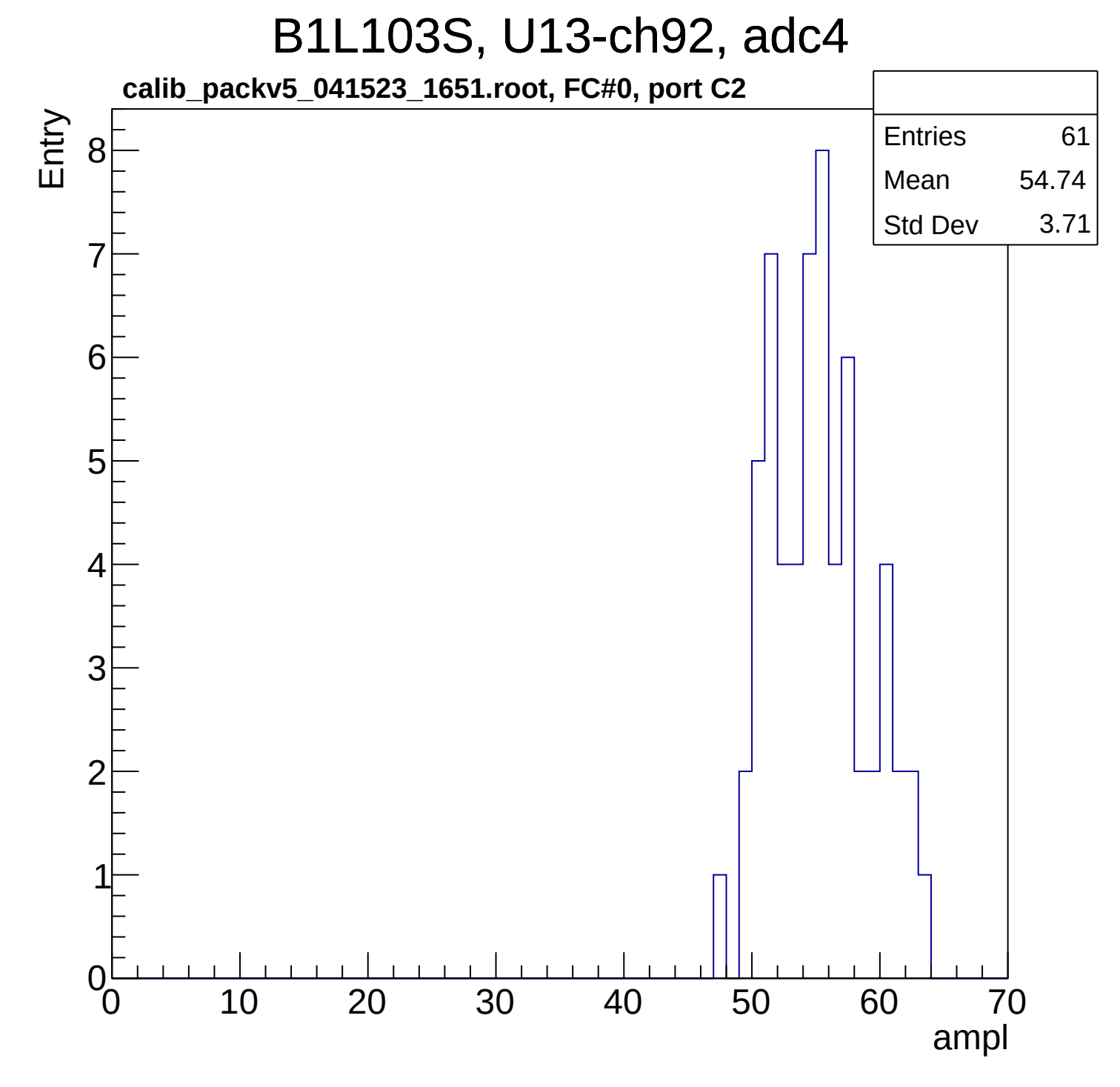

B1L103S, U13-ch92, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 37.3
Std Dev 14.58
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch92, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 47.03
Std Dev 11.46
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch92, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 54.74
Std Dev 3.71
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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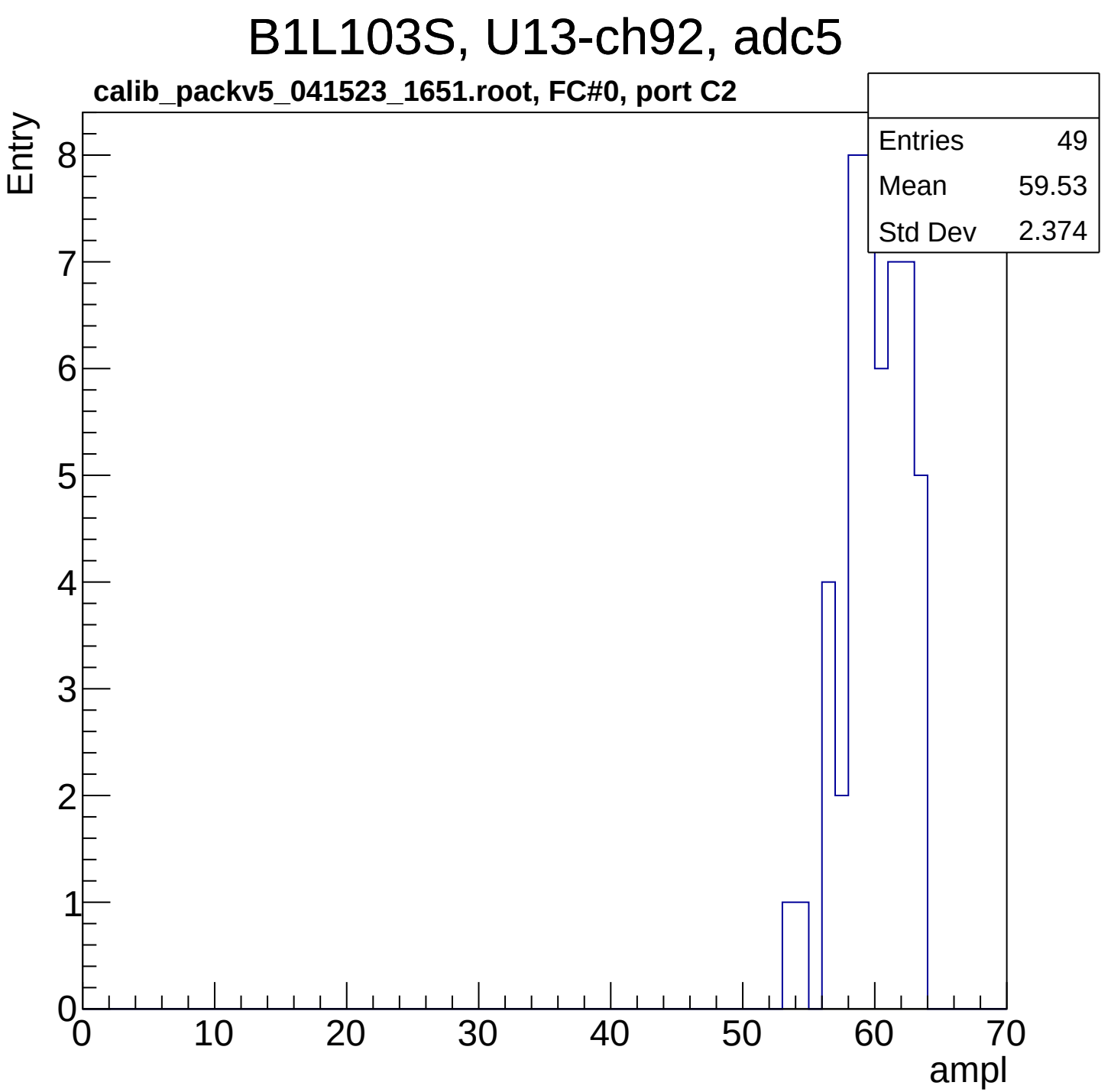
40
50
60
70


B1L103S, U13-ch92, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 59.53
Std Dev 2.374
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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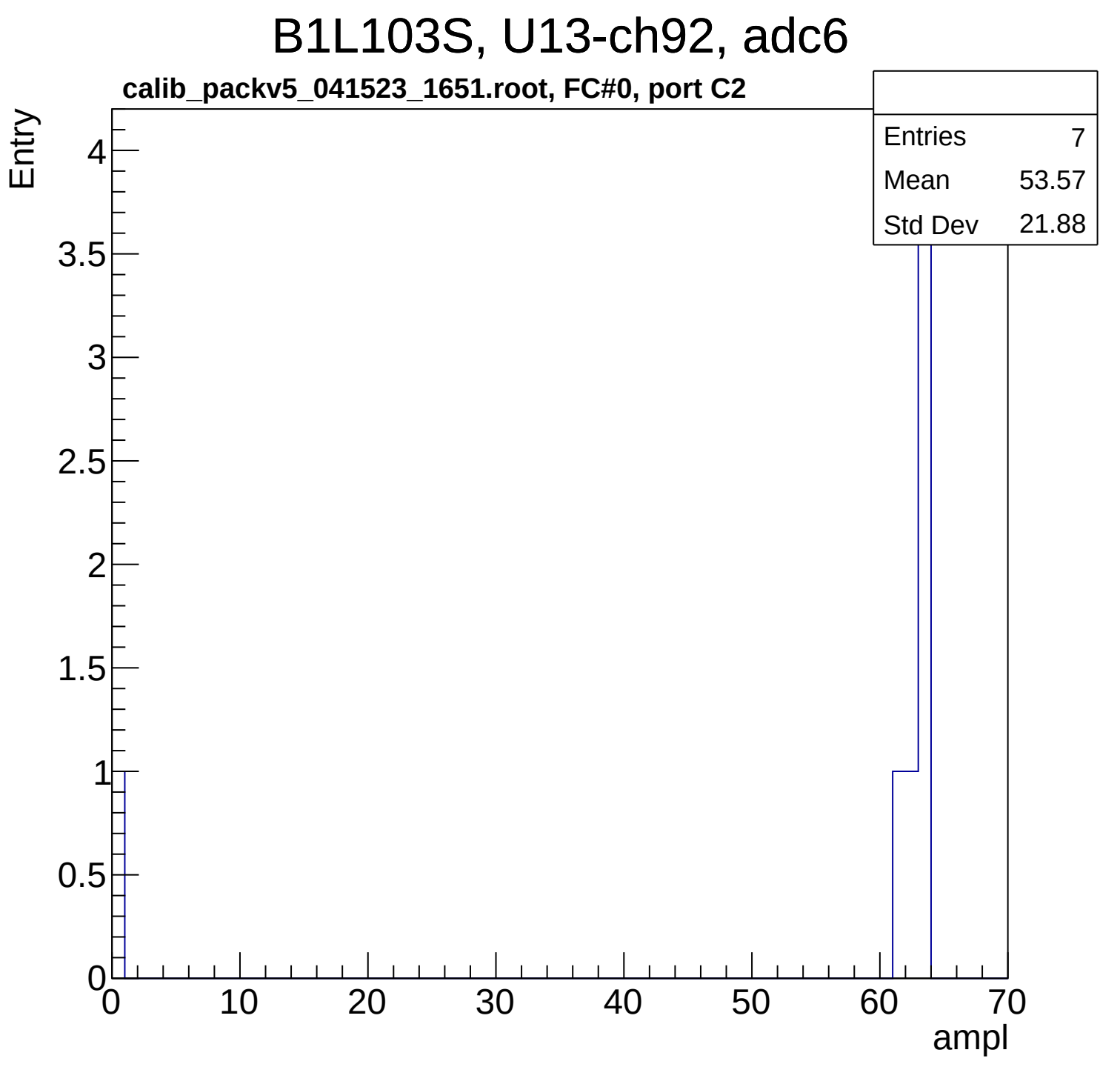
B1L103S, U13-ch92, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 53.57
Std Dev 21.88
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
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60
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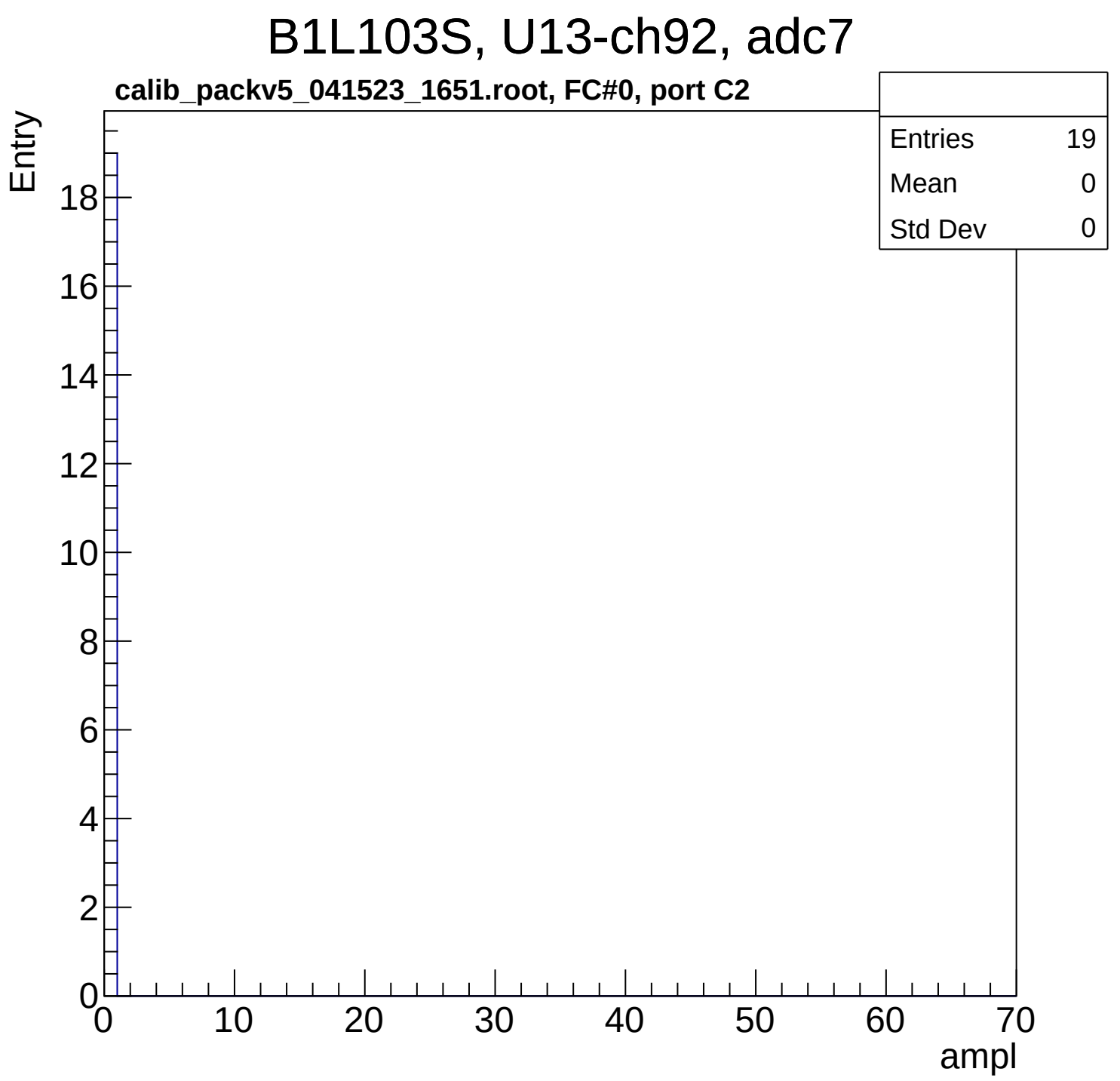
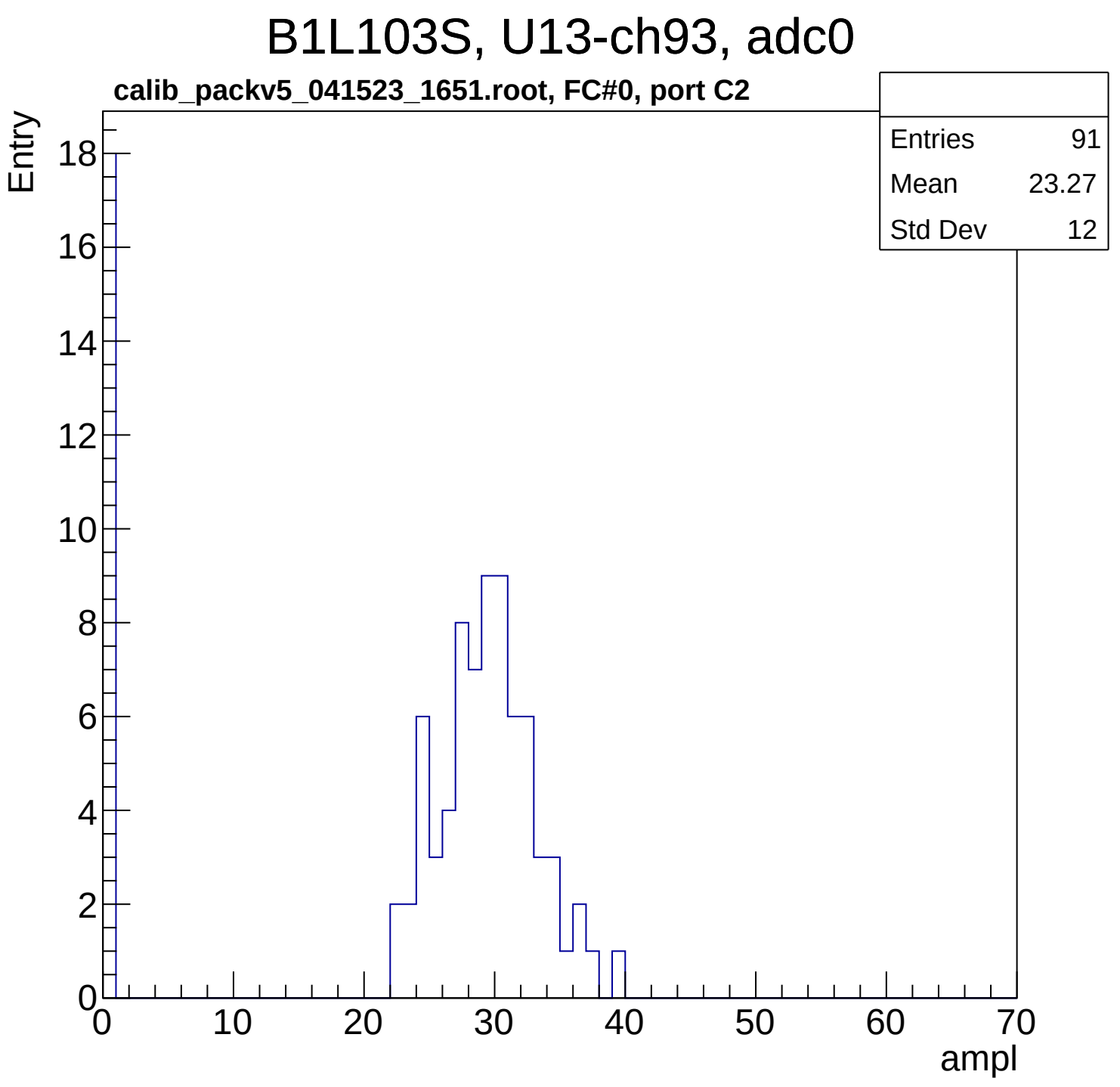
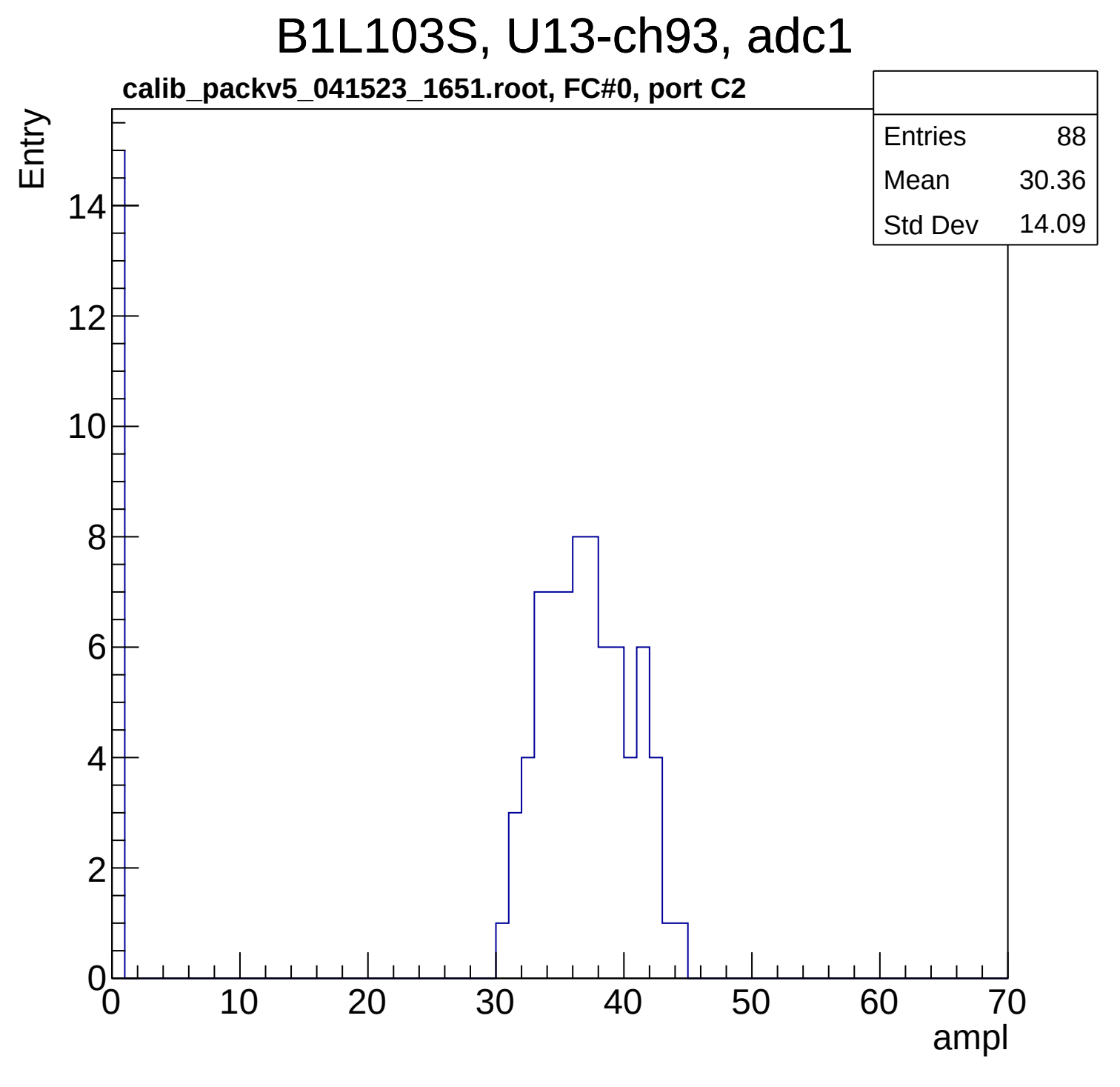
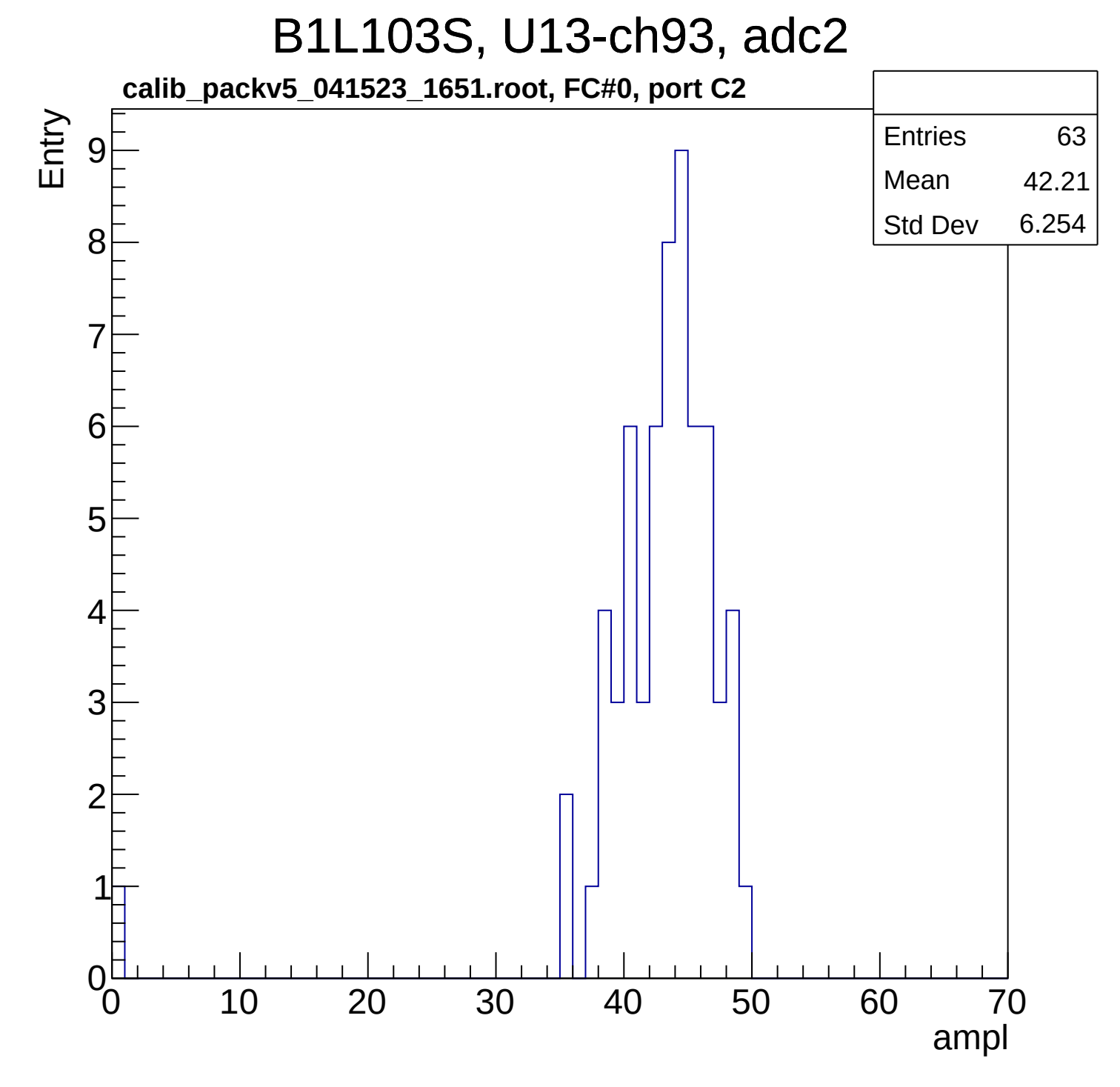

B1L103S, U13-ch92, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch93, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 23.27
Std Dev 12
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch93, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 30.36
Std Dev 14.09
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch93, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 42.21
Std Dev 6.254
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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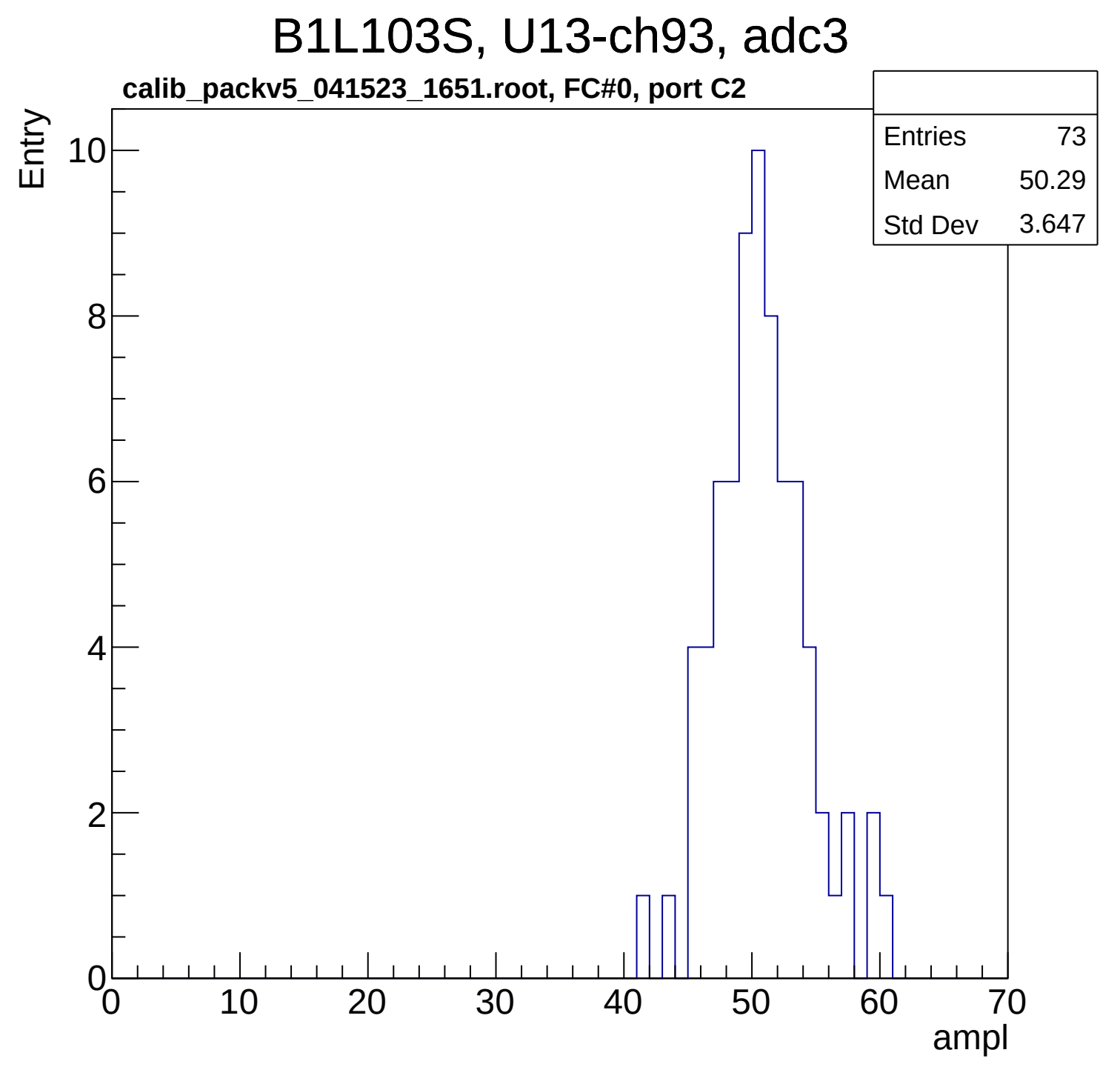
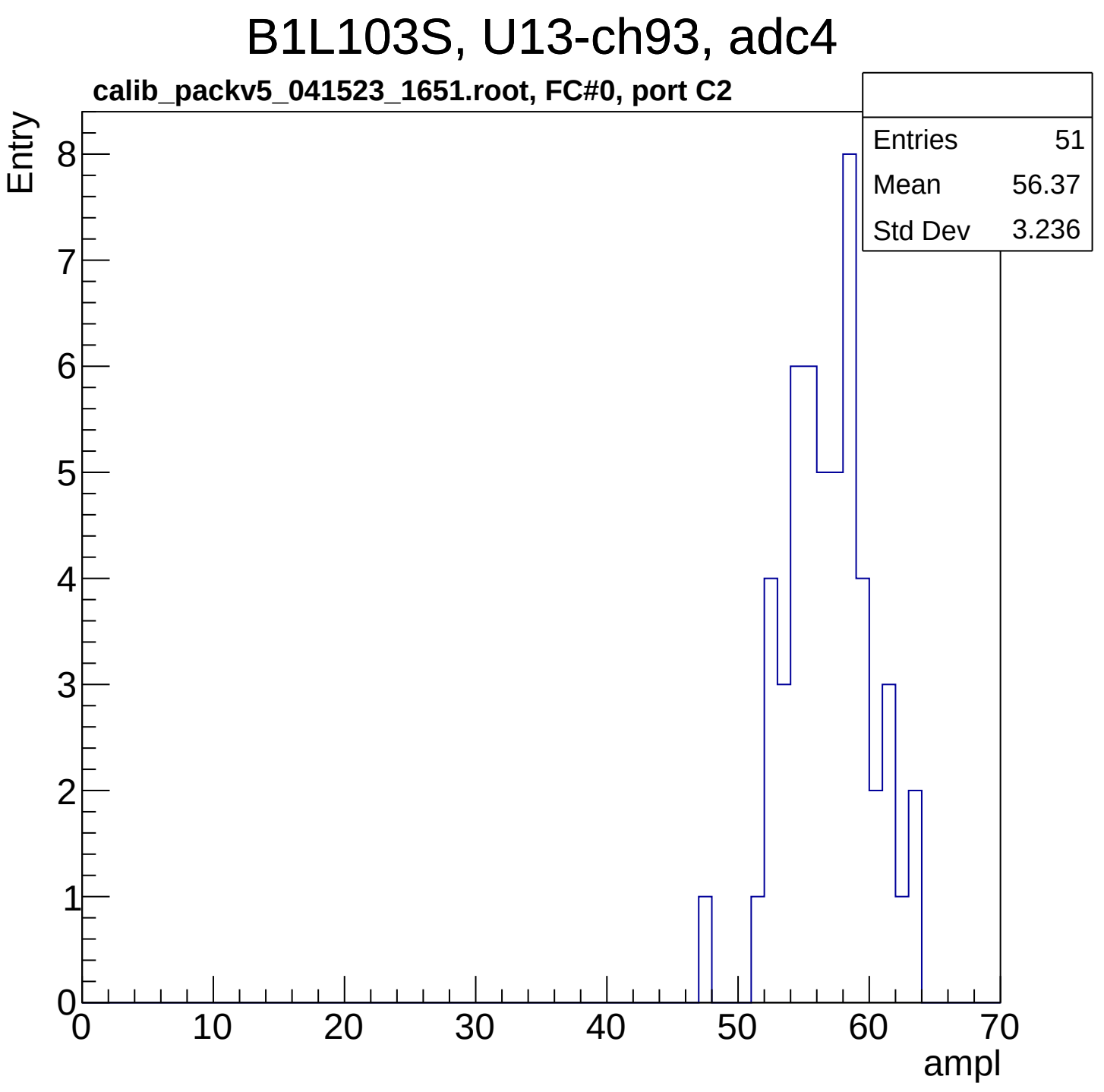
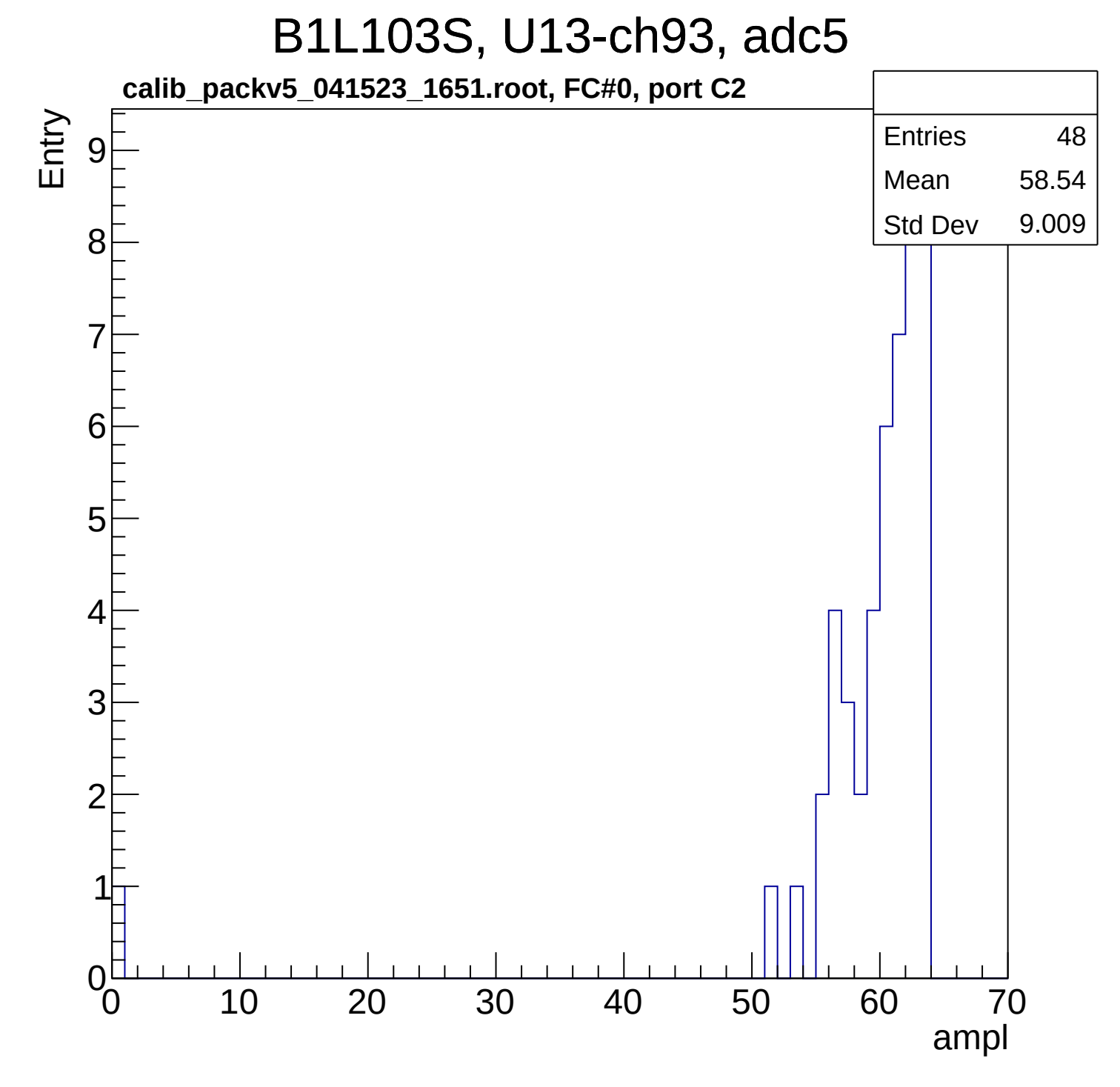
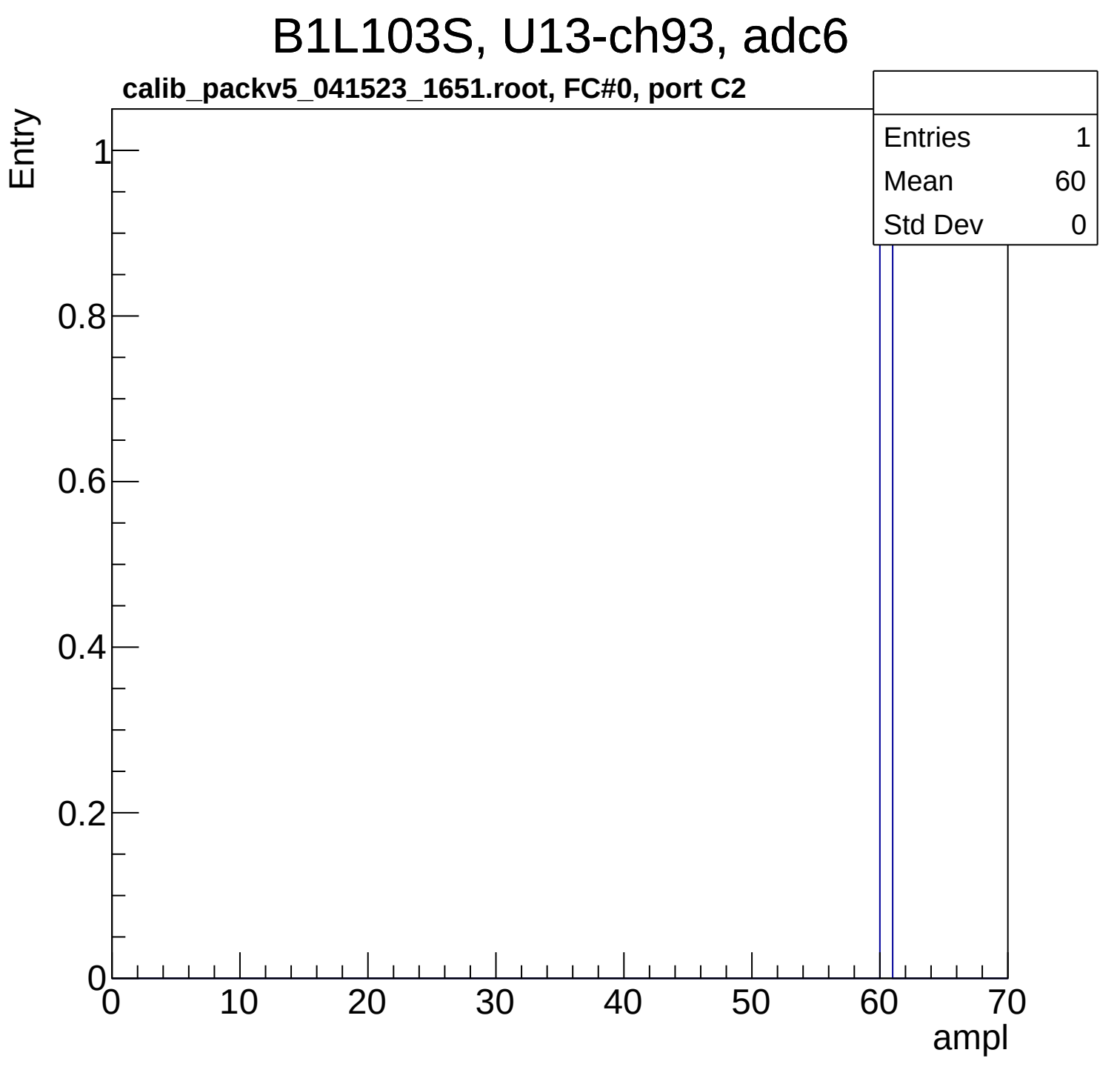
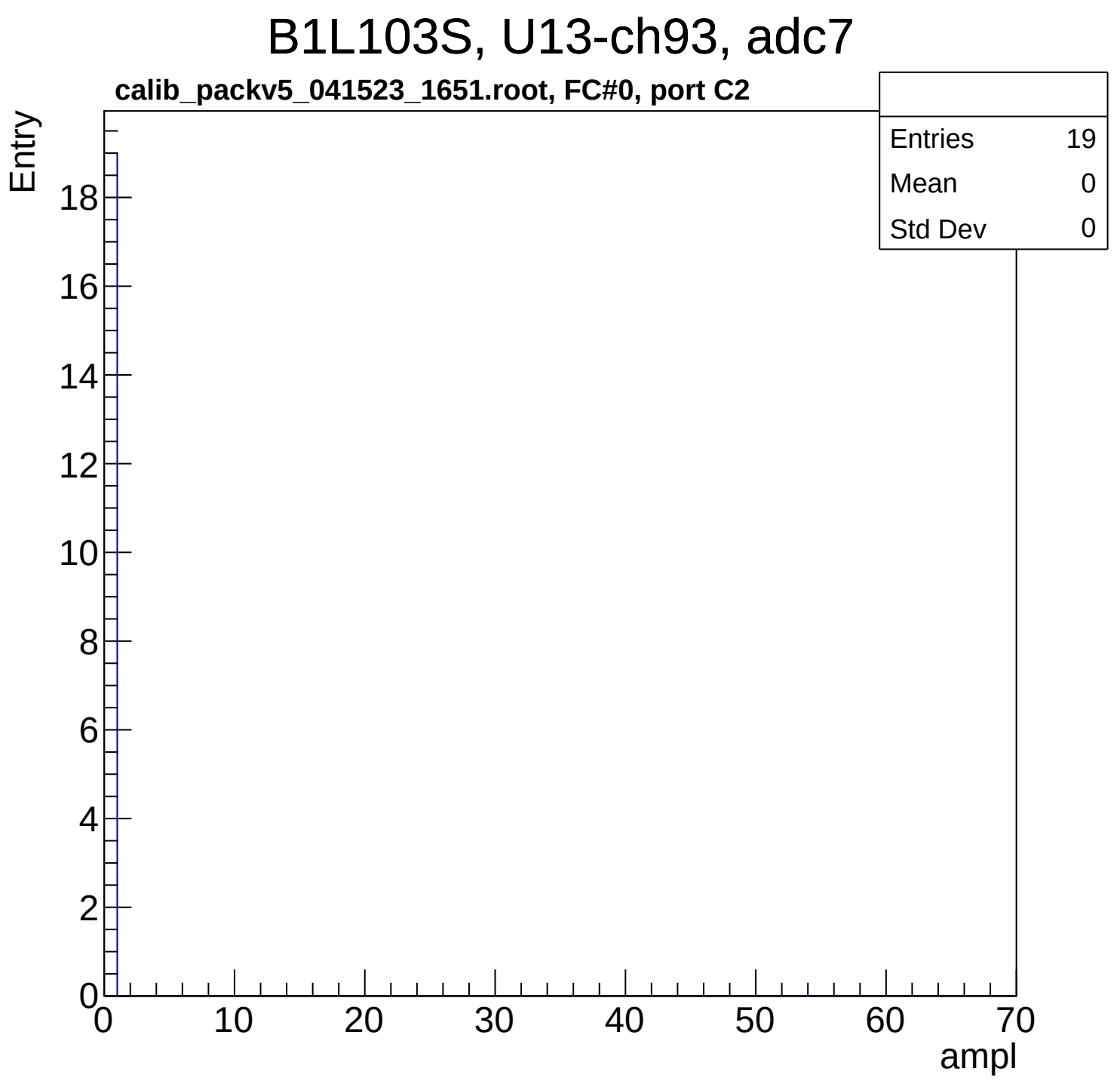
40
50
60
70

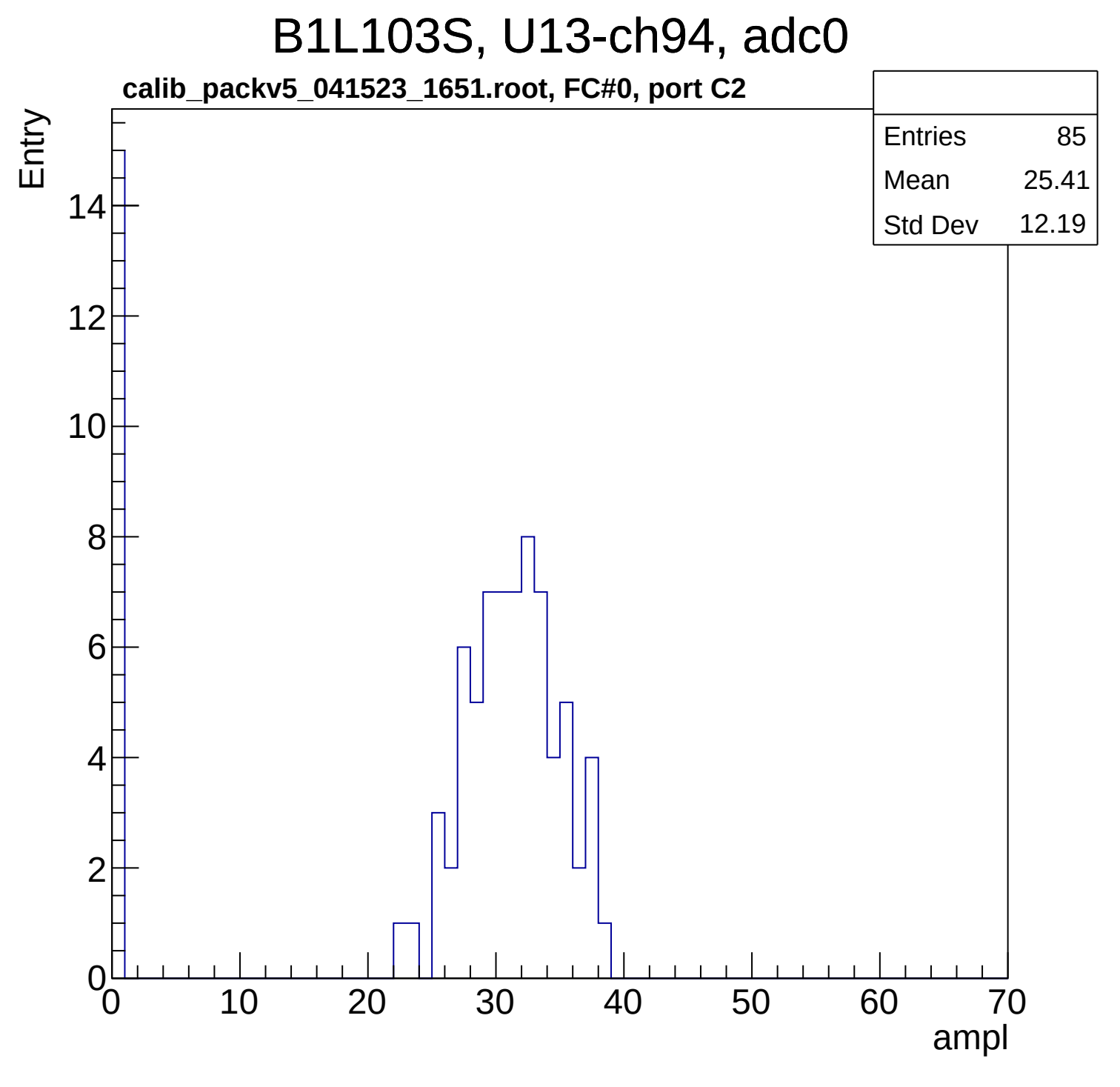

B1L103S, U13-ch93, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 50.29
Std Dev 3.647
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

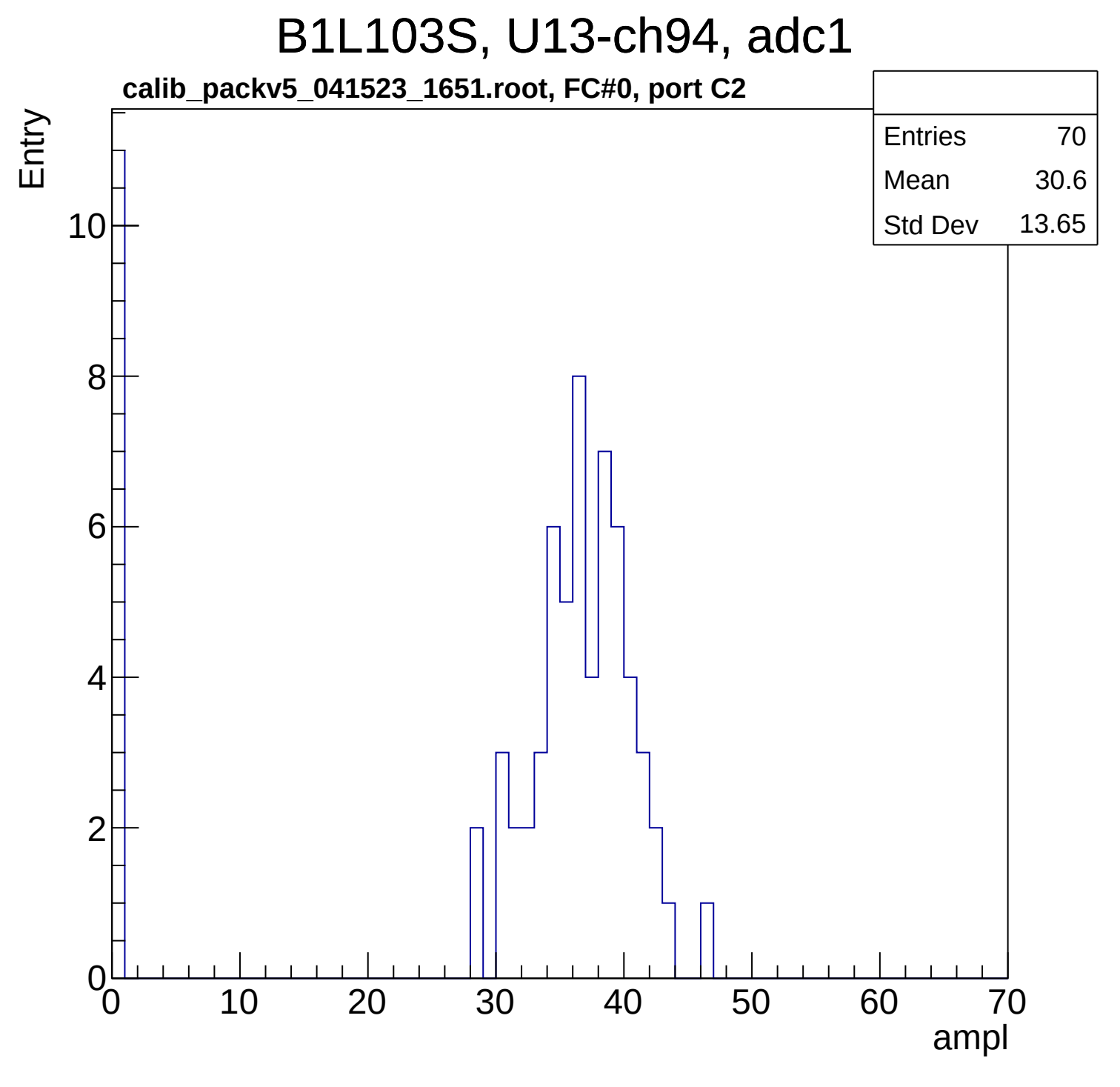

B1L103S, U13-ch93, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 56.37
Std Dev 3.236
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

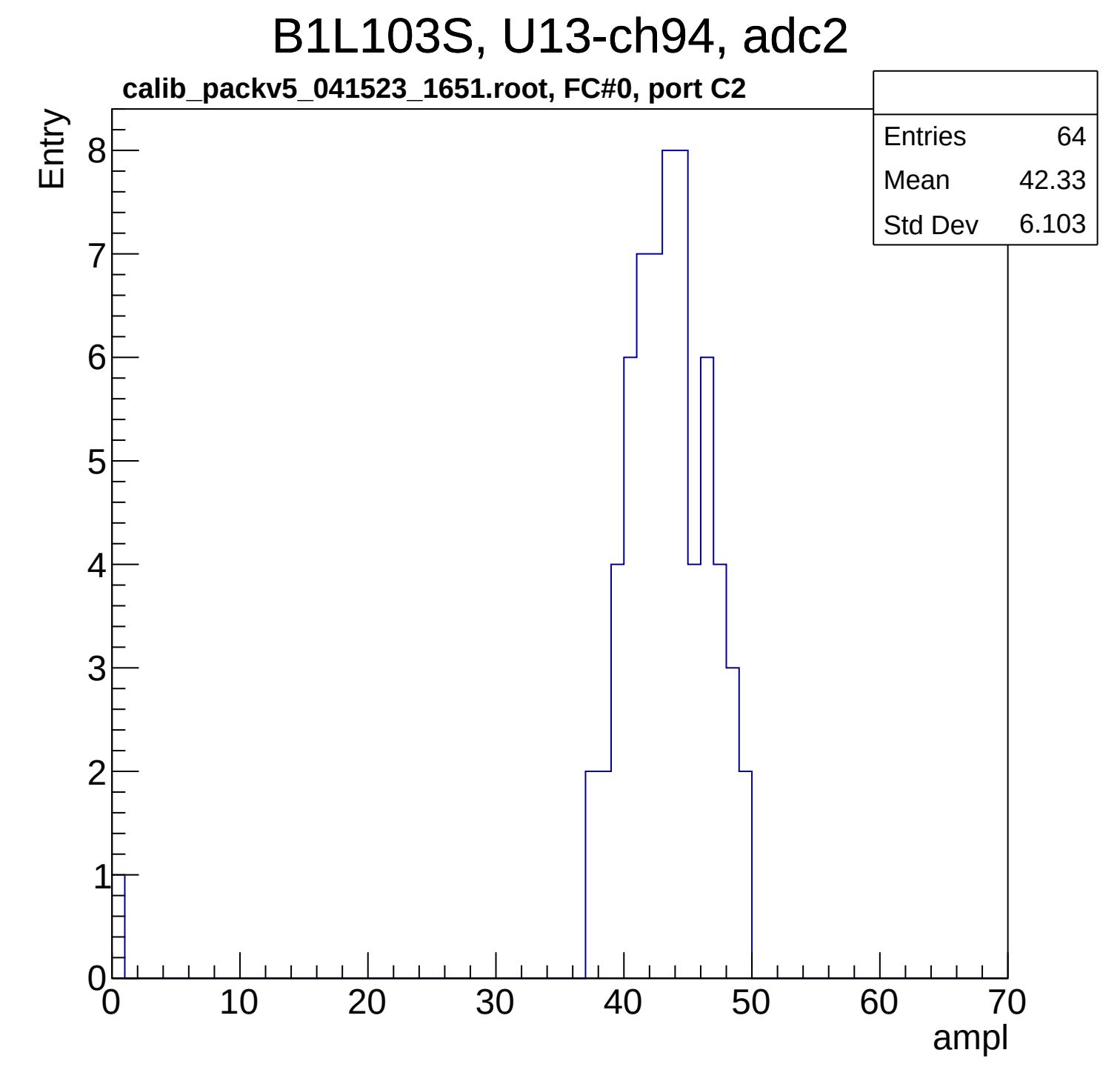

B1L103S, U13-ch93, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.54
Std Dev 9.009
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

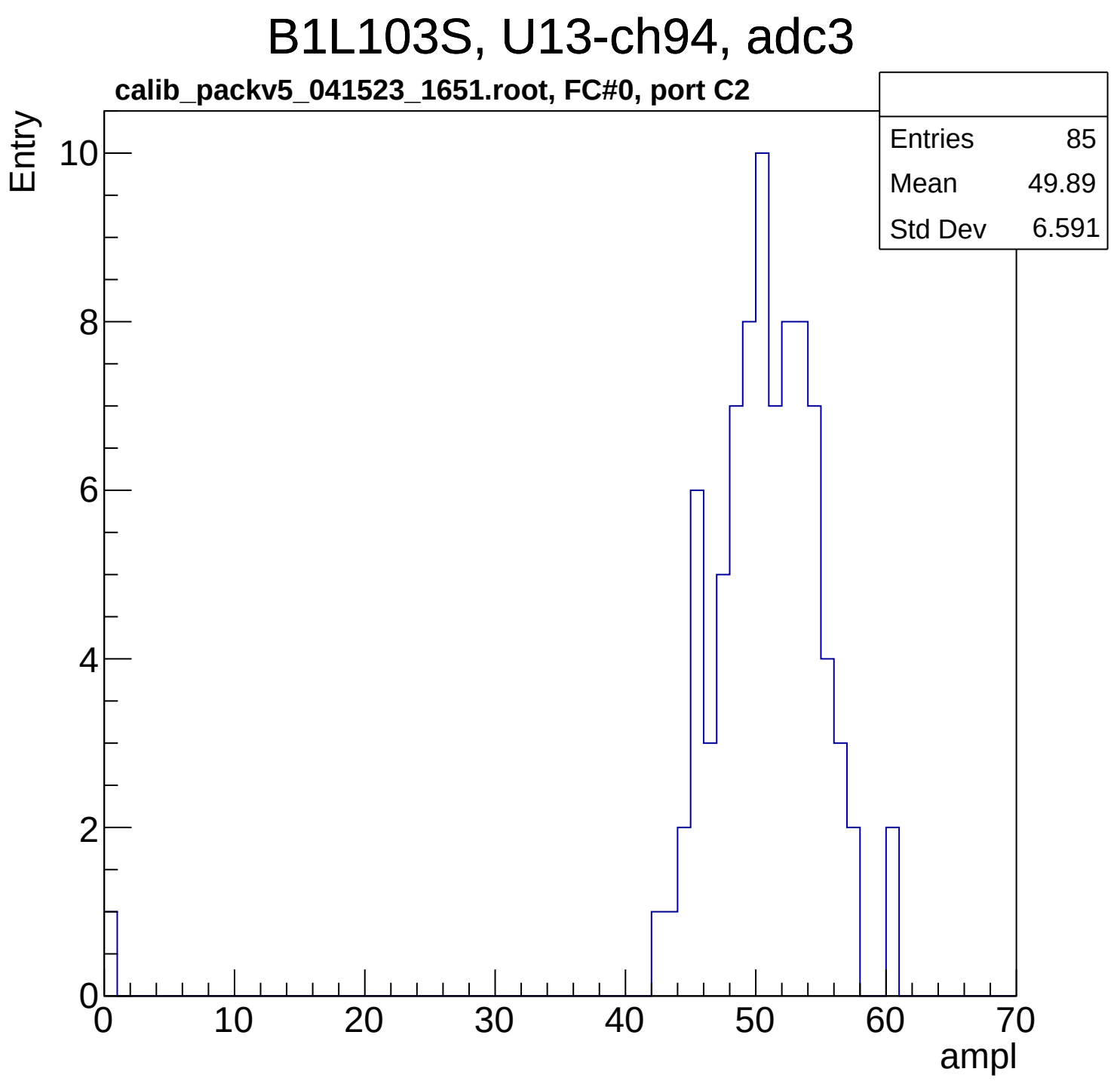

B1L103S, U13-ch93, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 60
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

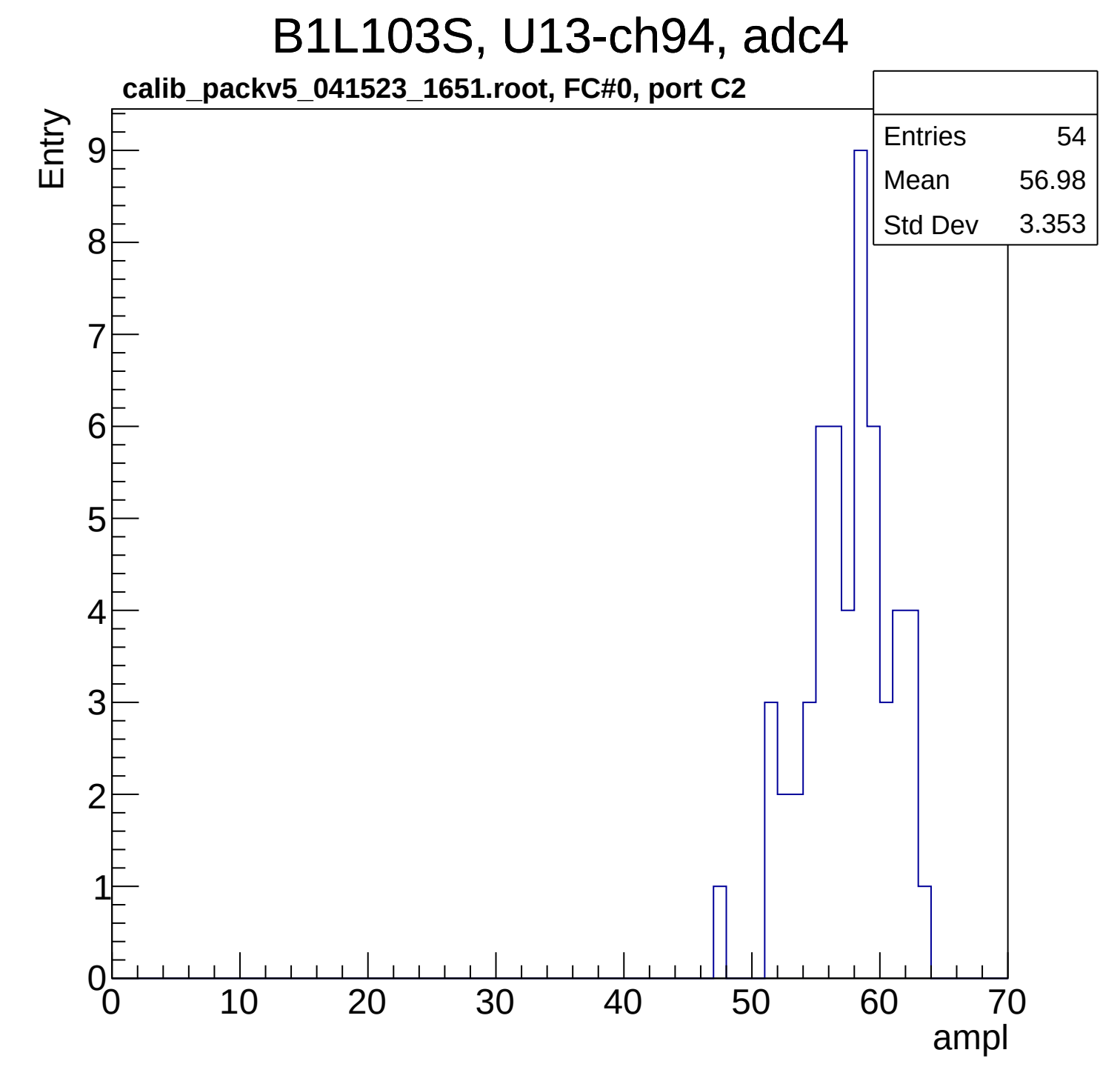

B1L103S, U13-ch93, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

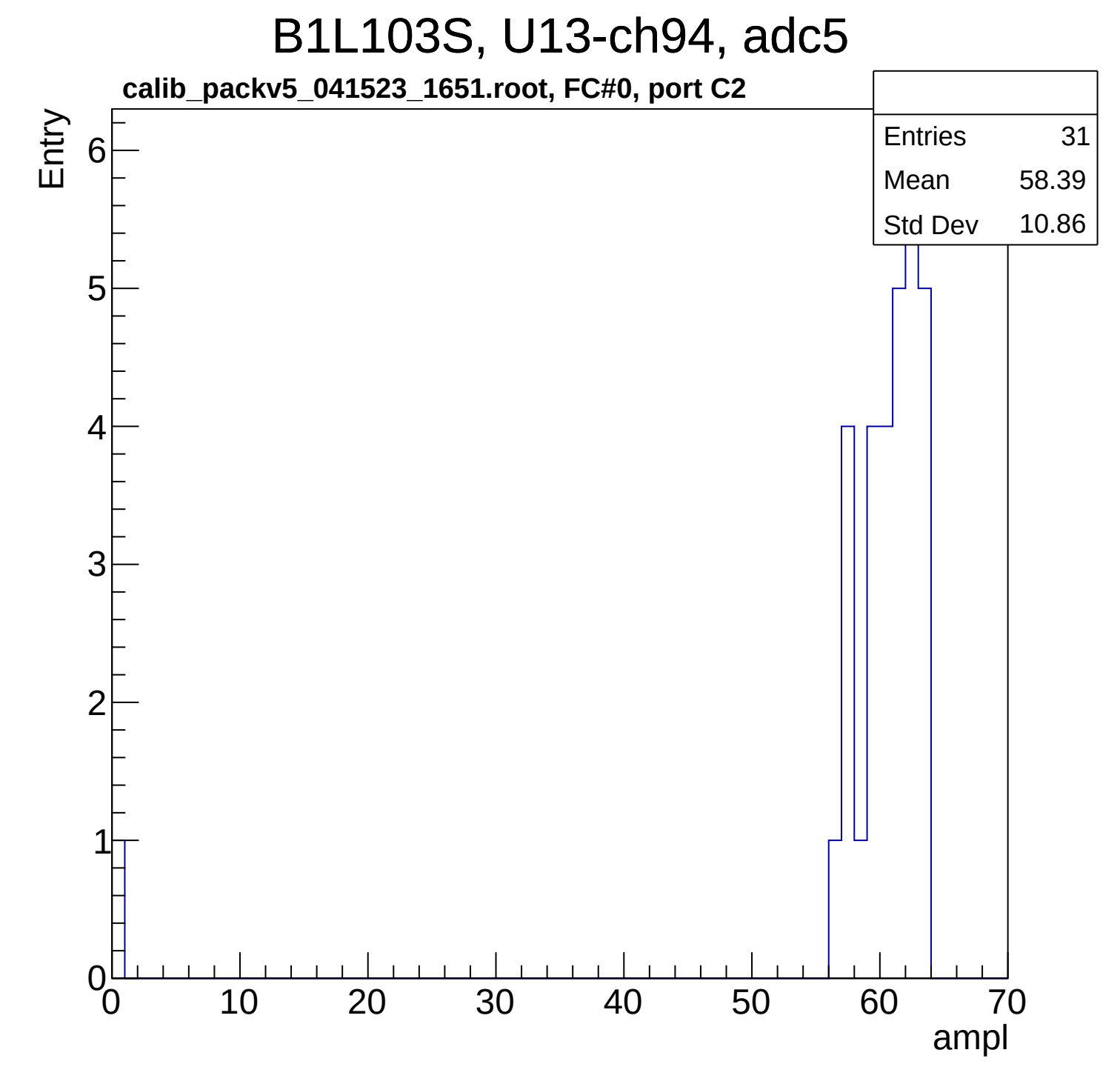

B1L103S, U13-ch94, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 25.41
Std Dev 12.19
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

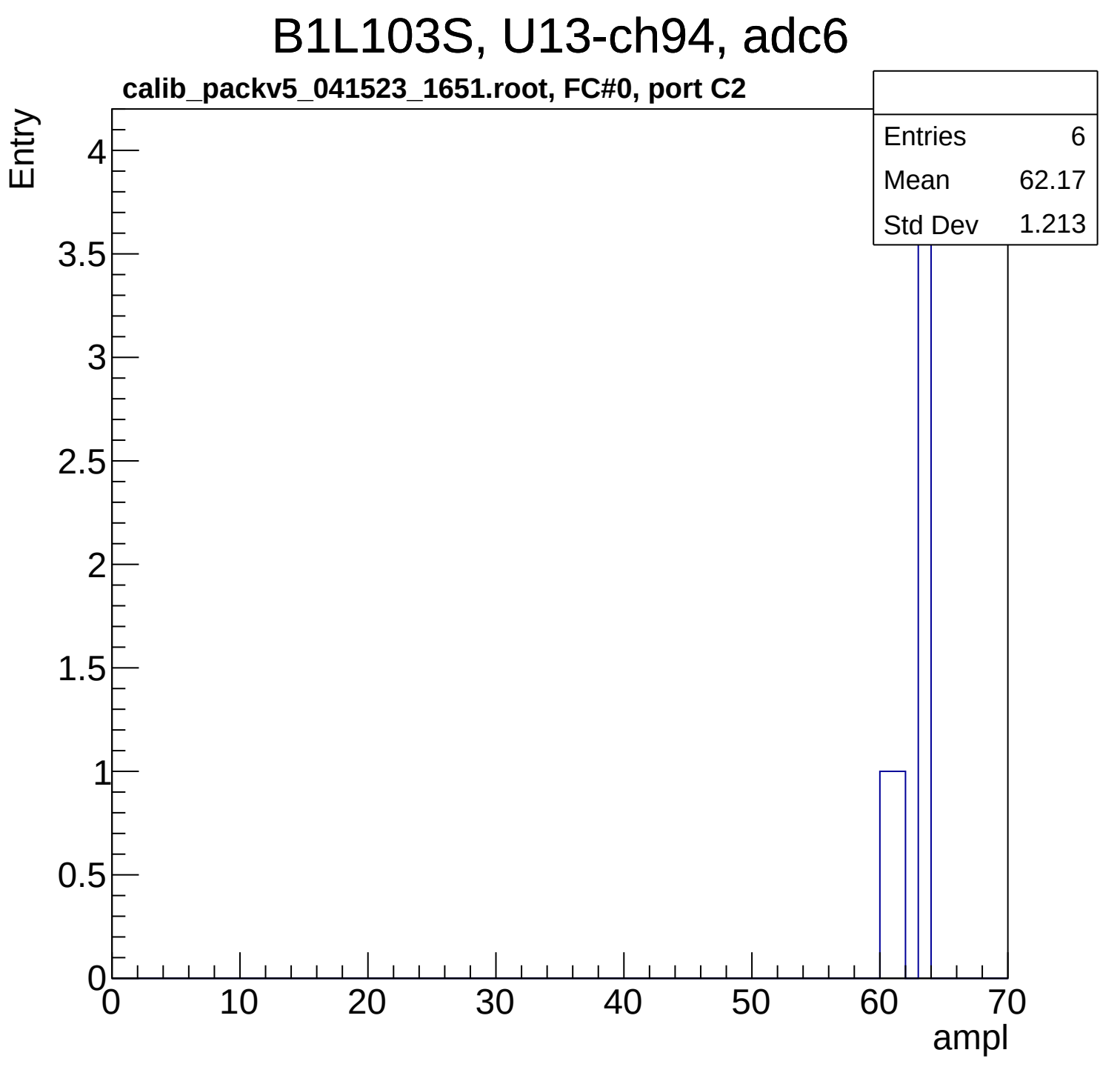

B1L103S, U13-ch94, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 30.6
Std Dev 13.65
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

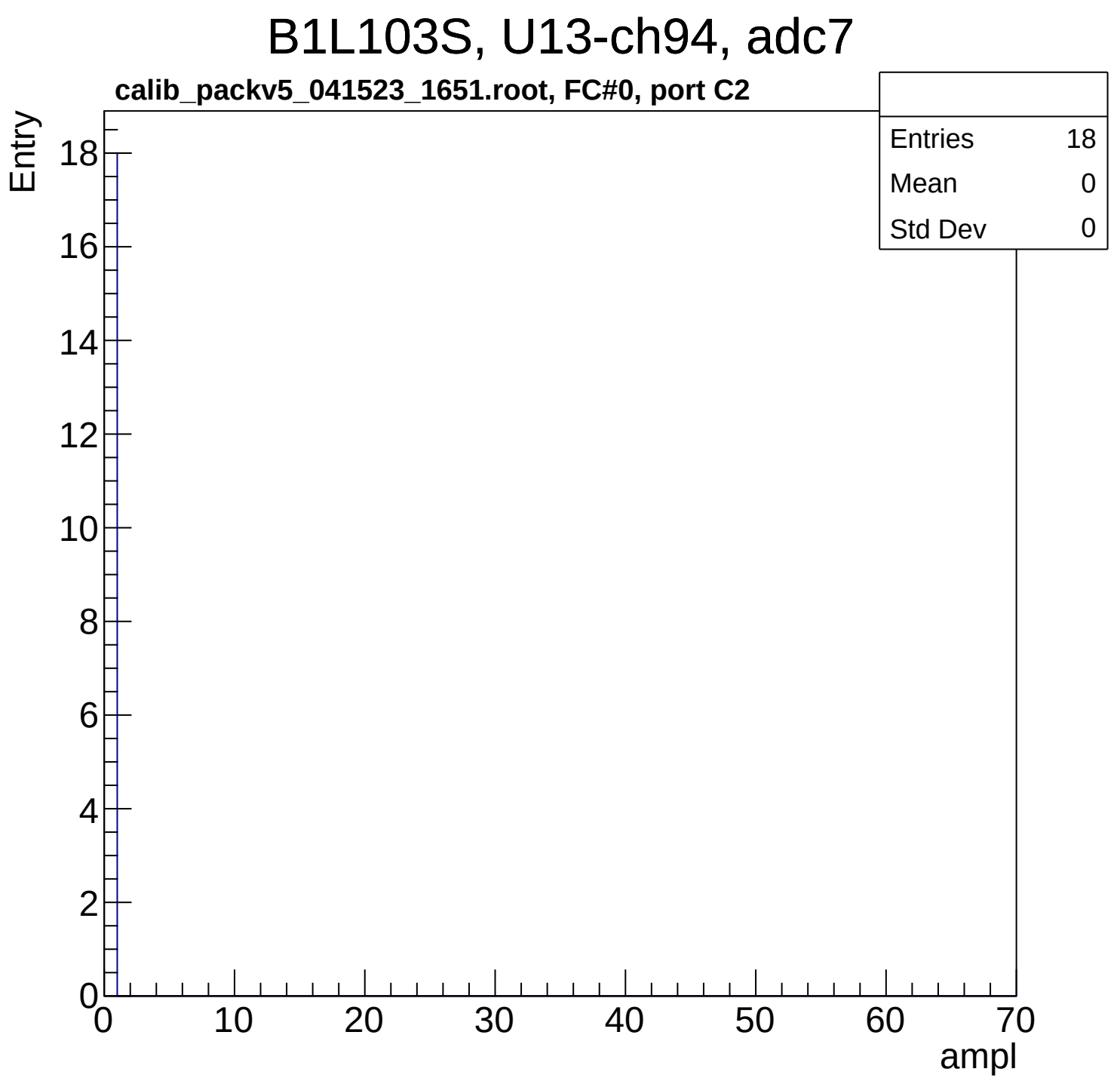

B1L103S, U13-ch94, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 42.33
Std Dev 6.103
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

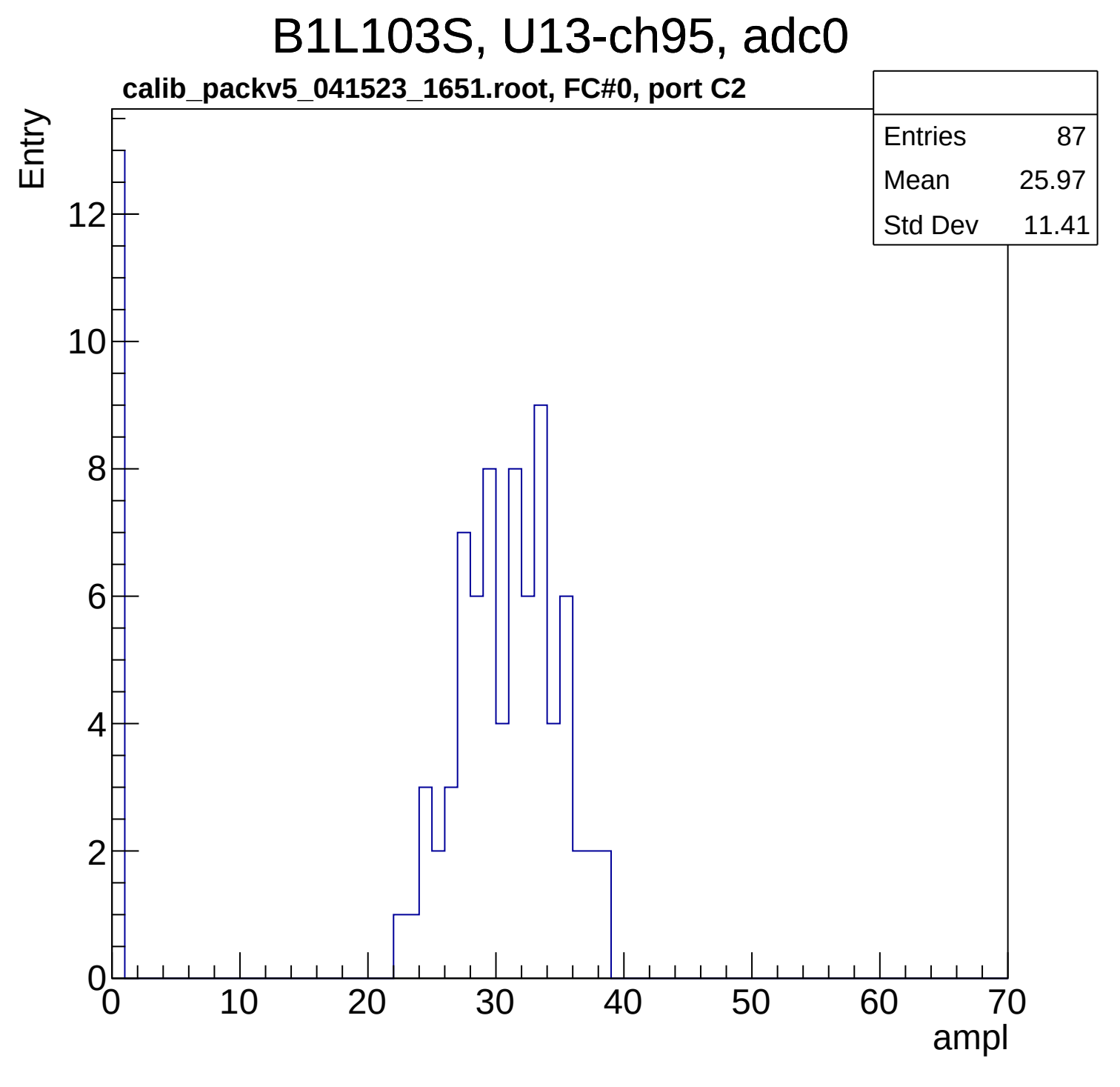

B1L103S, U13-ch94, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 49.89
Std Dev 6.591
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

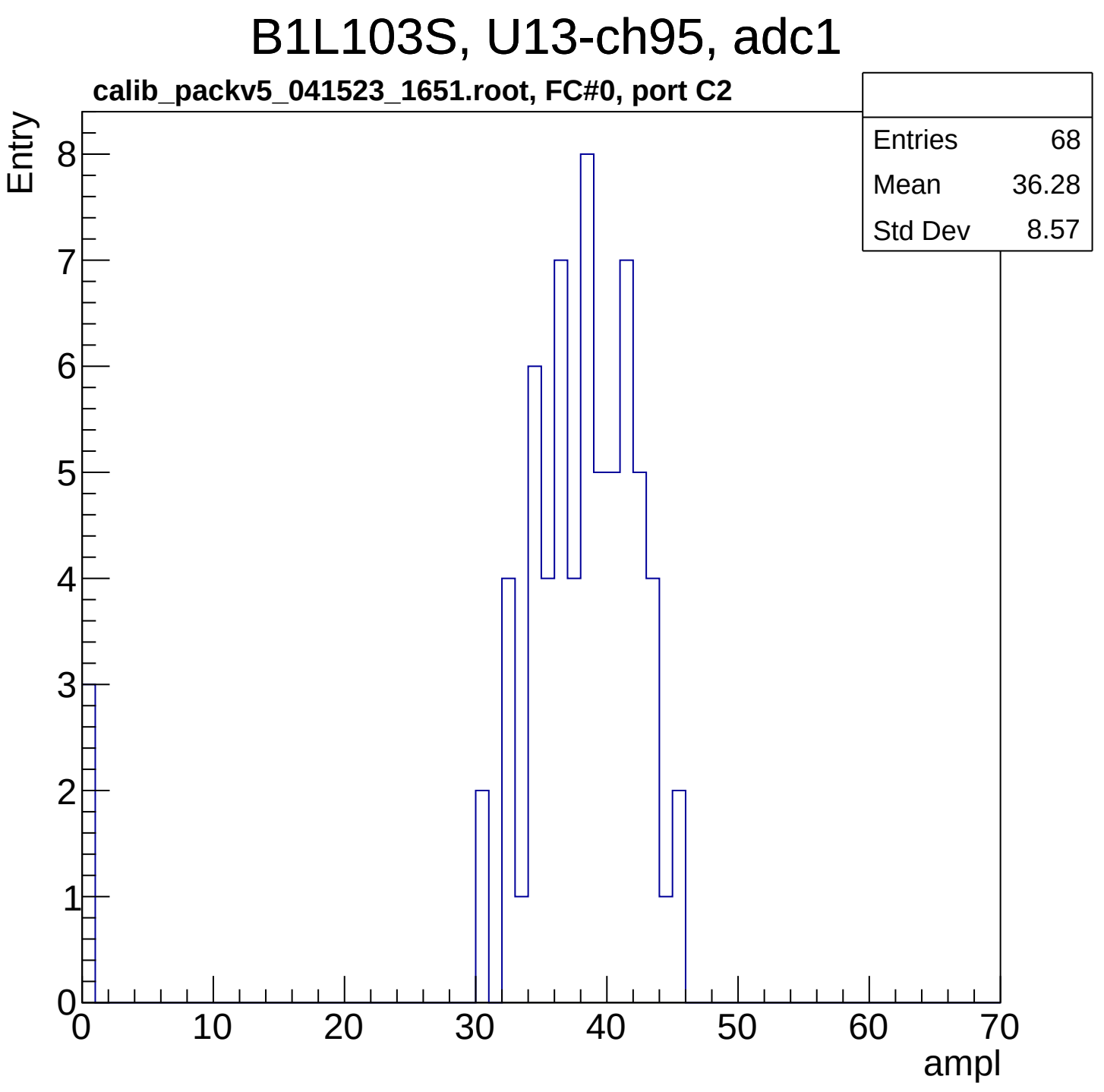

B1L103S, U13-ch94, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 56.98
Std Dev 3.353
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

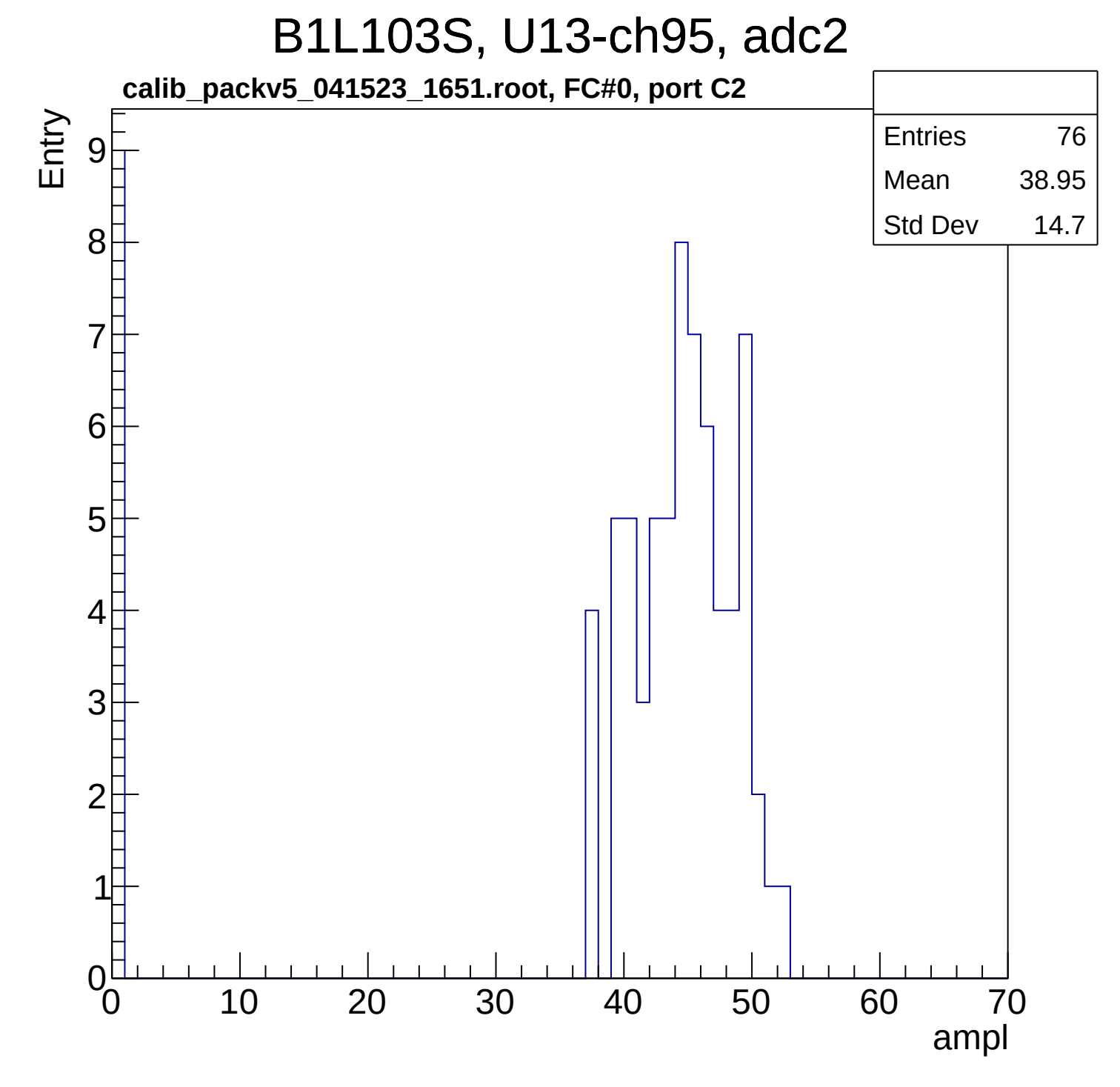

B1L103S, U13-ch94, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 58.39
Std Dev 10.86
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

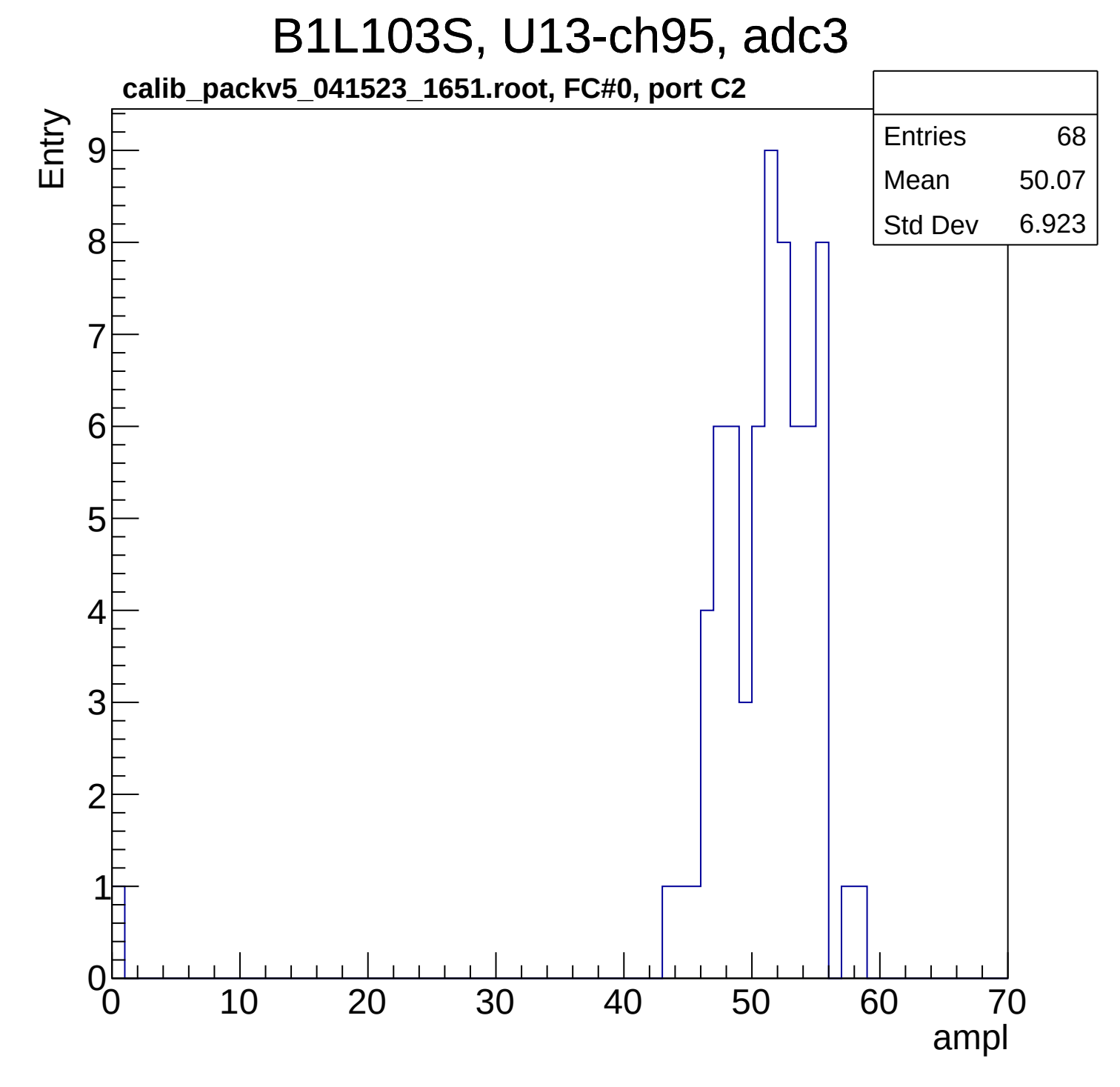

B1L103S, U13-ch94, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.17
Std Dev 1.213
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

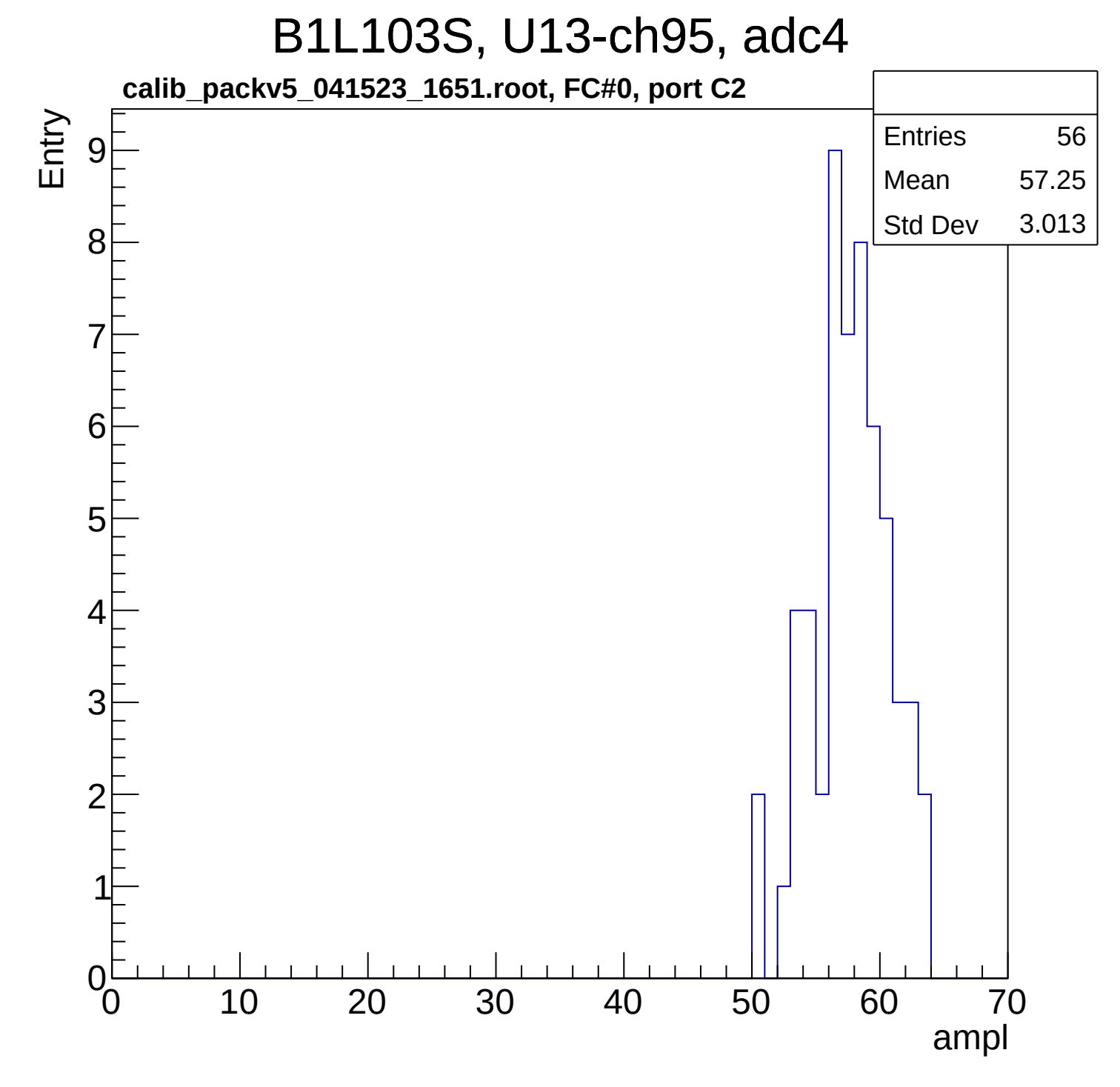

B1L103S, U13-ch94, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

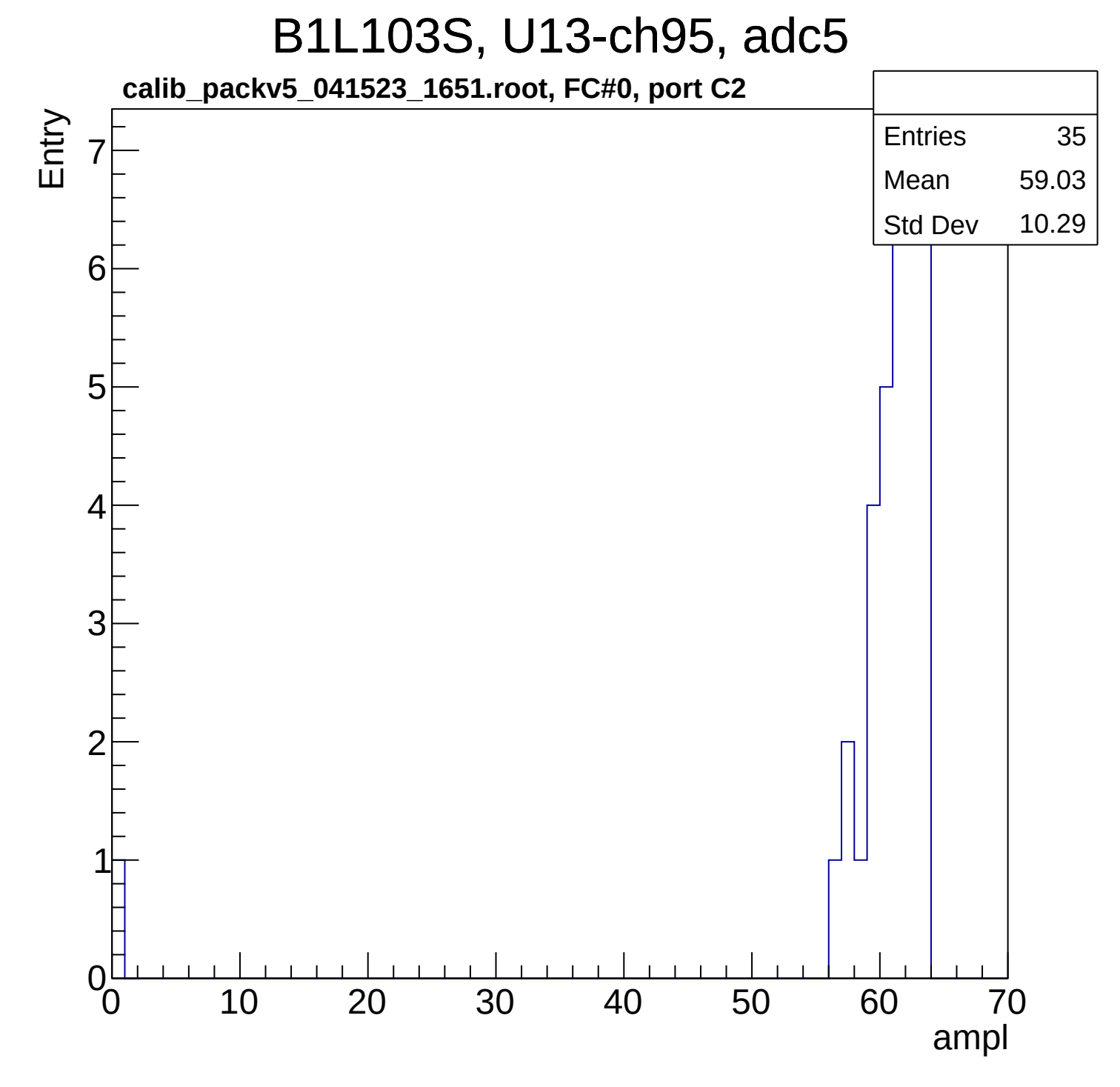

B1L103S, U13-ch95, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 25.97
Std Dev 11.41
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

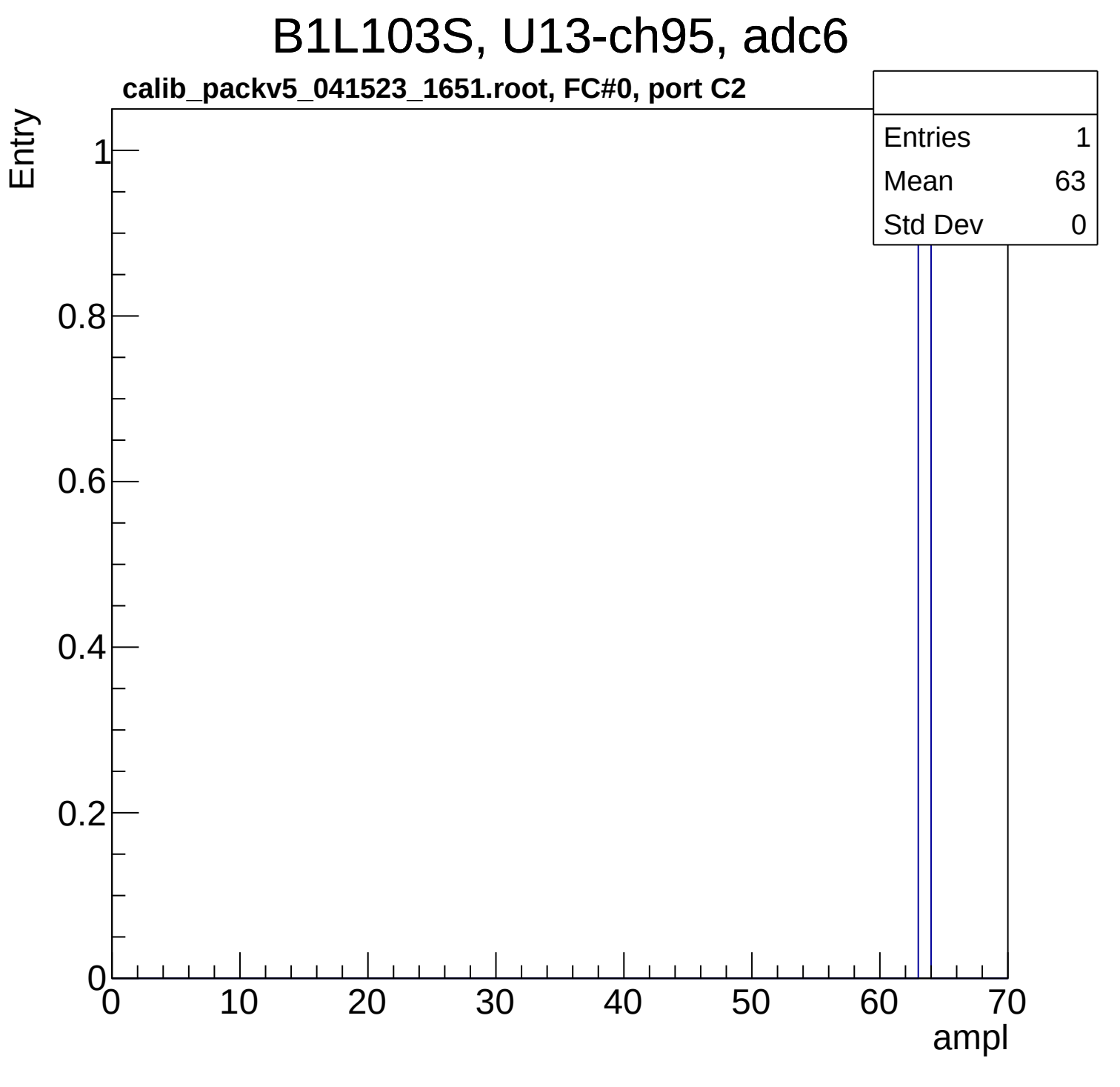

B1L103S, U13-ch95, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 36.28
Std Dev 8.57
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

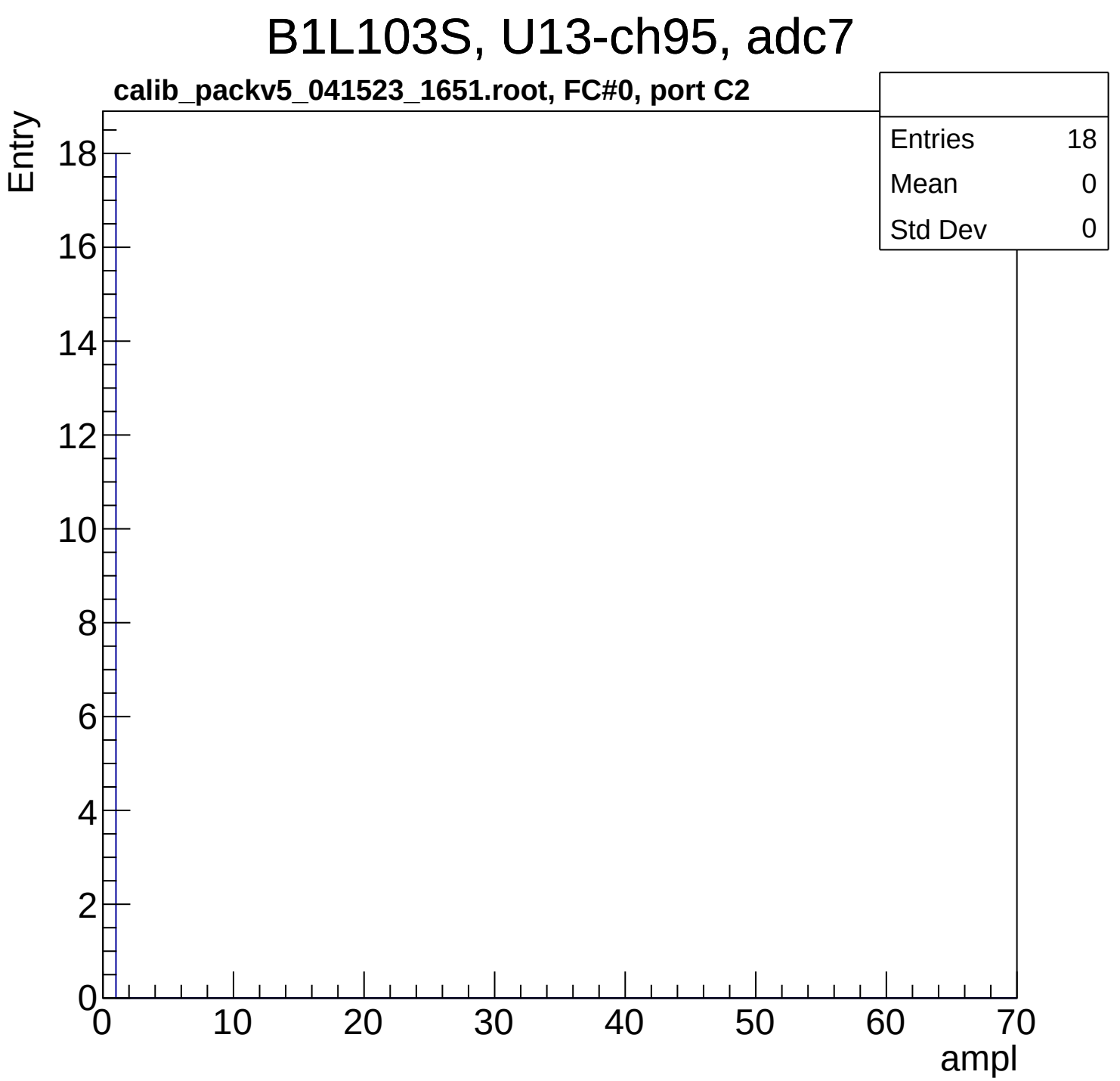

B1L103S, U13-ch95, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 38.95
Std Dev 14.7
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

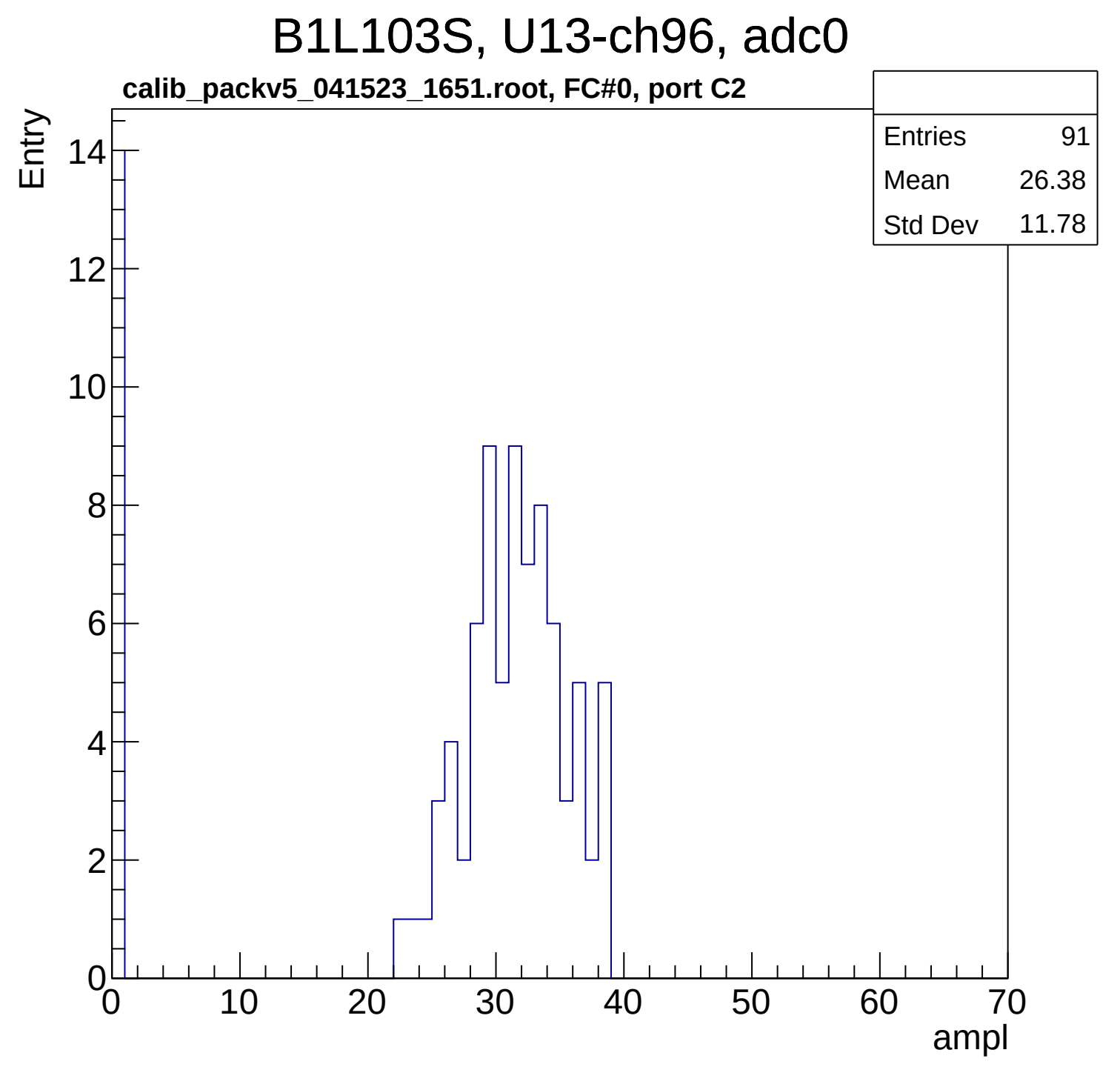

B1L103S, U13-ch95, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 50.07
Std Dev 6.923
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

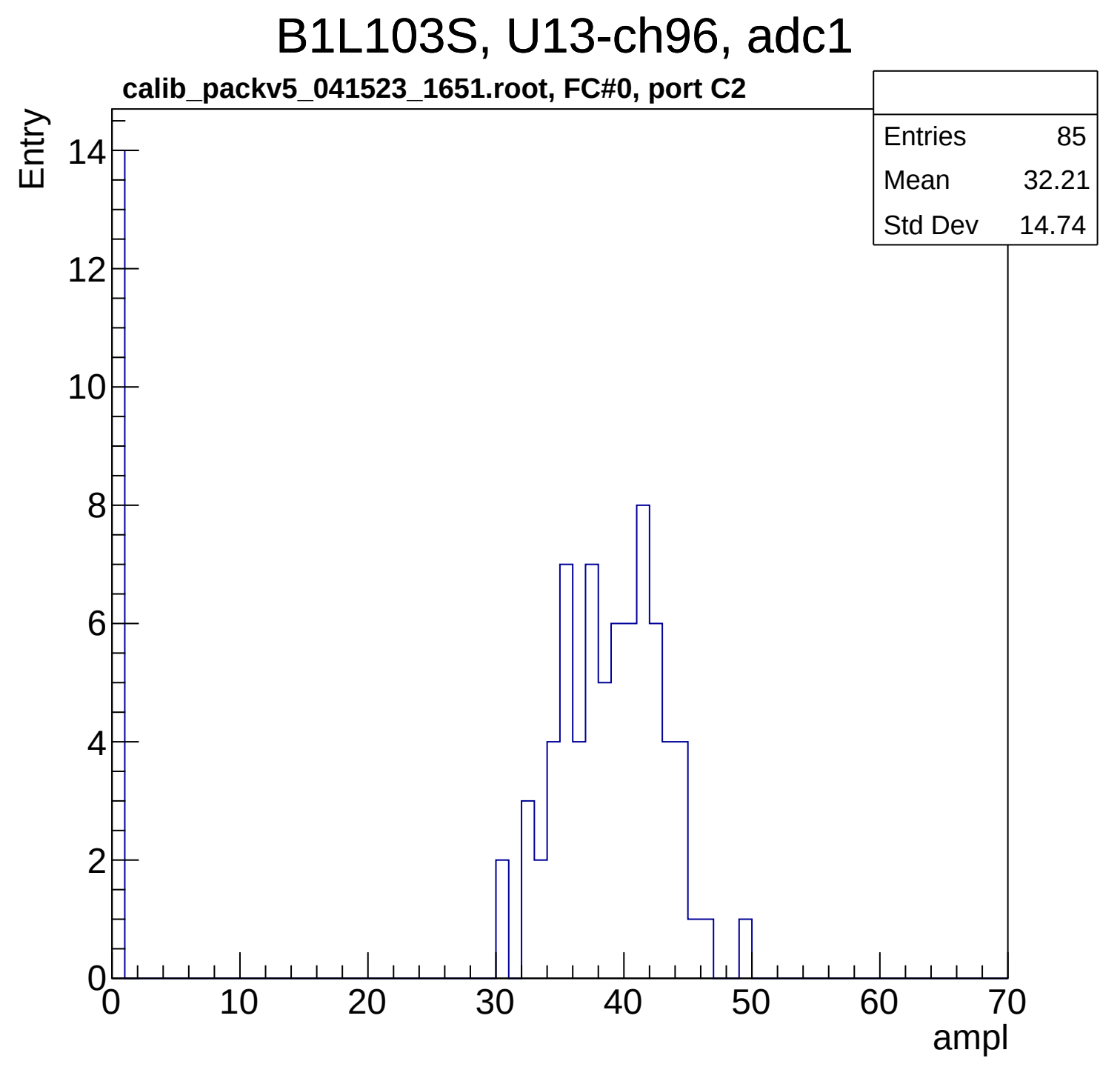

B1L103S, U13-ch95, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 57.25
Std Dev 3.013
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

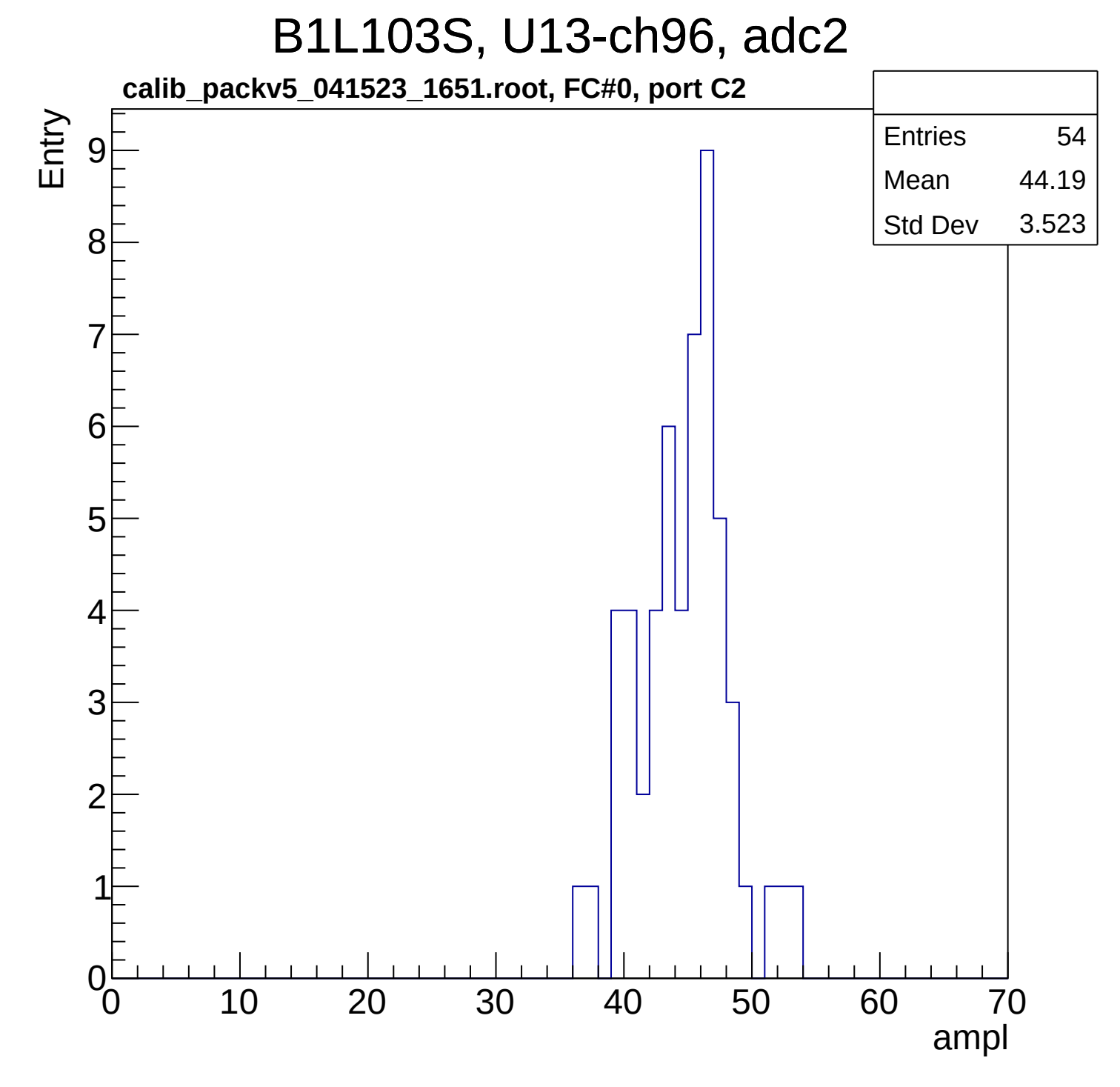

B1L103S, U13-ch95, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 59.03
Std Dev 10.29
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

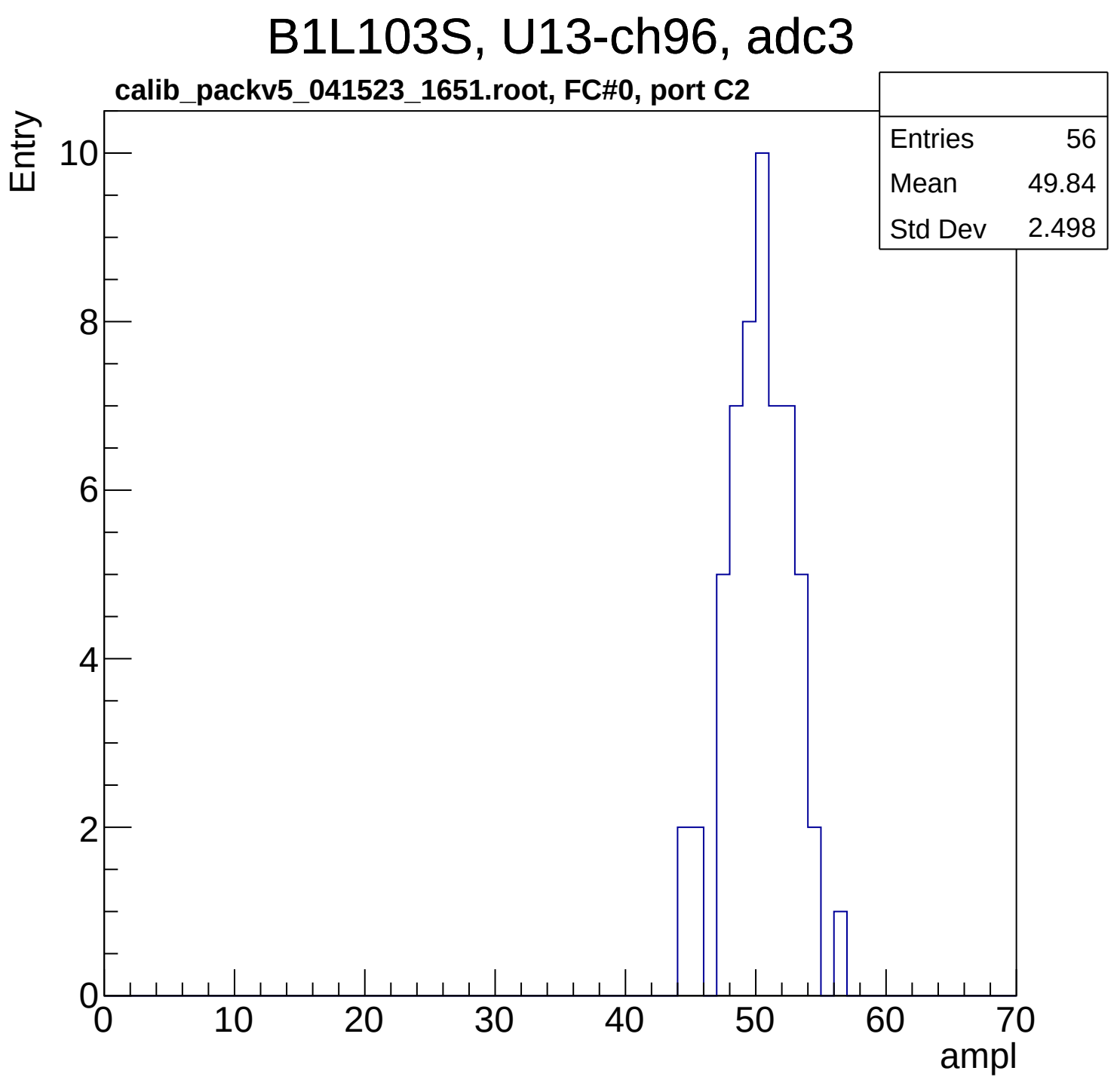

B1L103S, U13-ch95, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

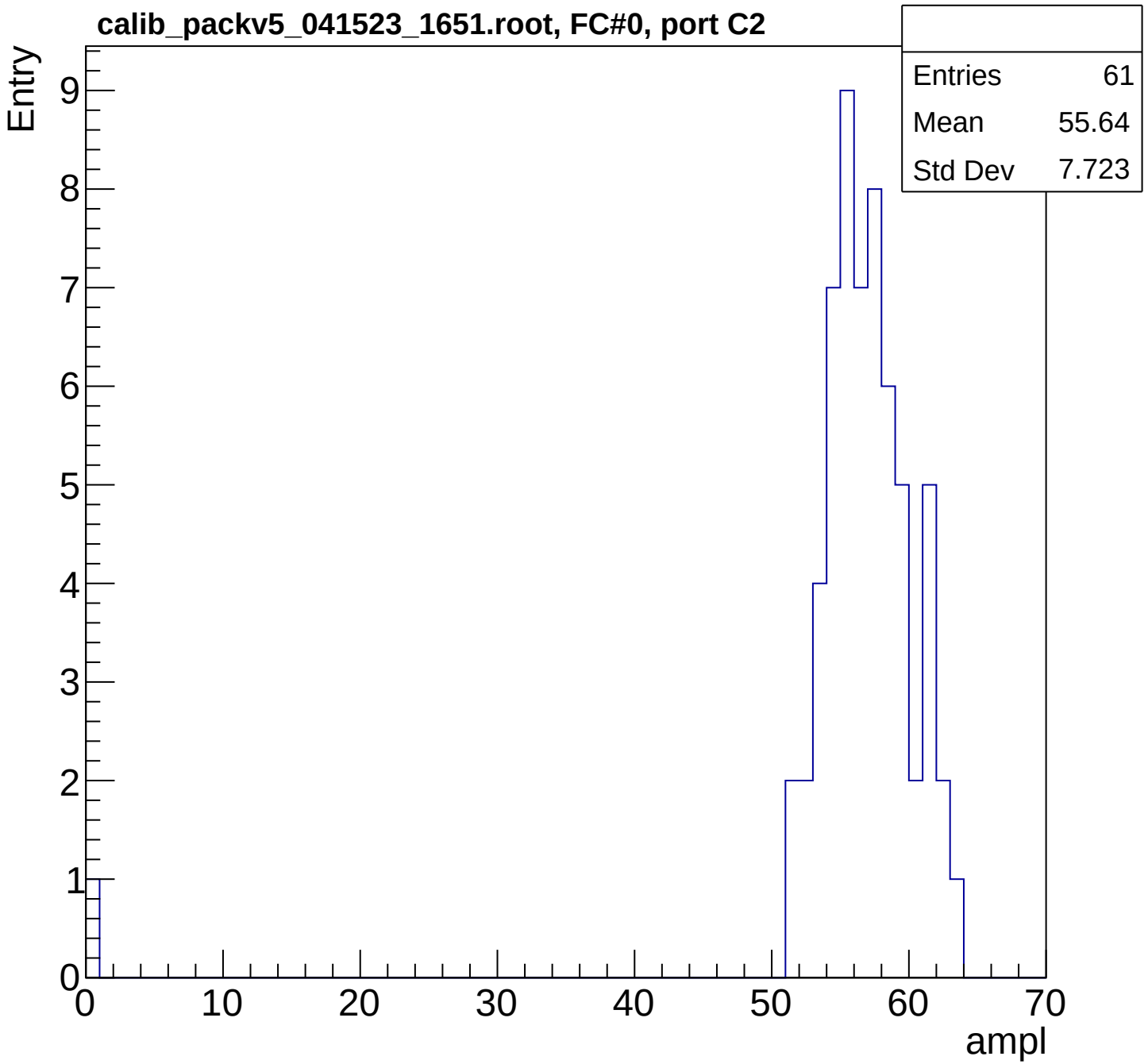

B1L103S, U13-ch95, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

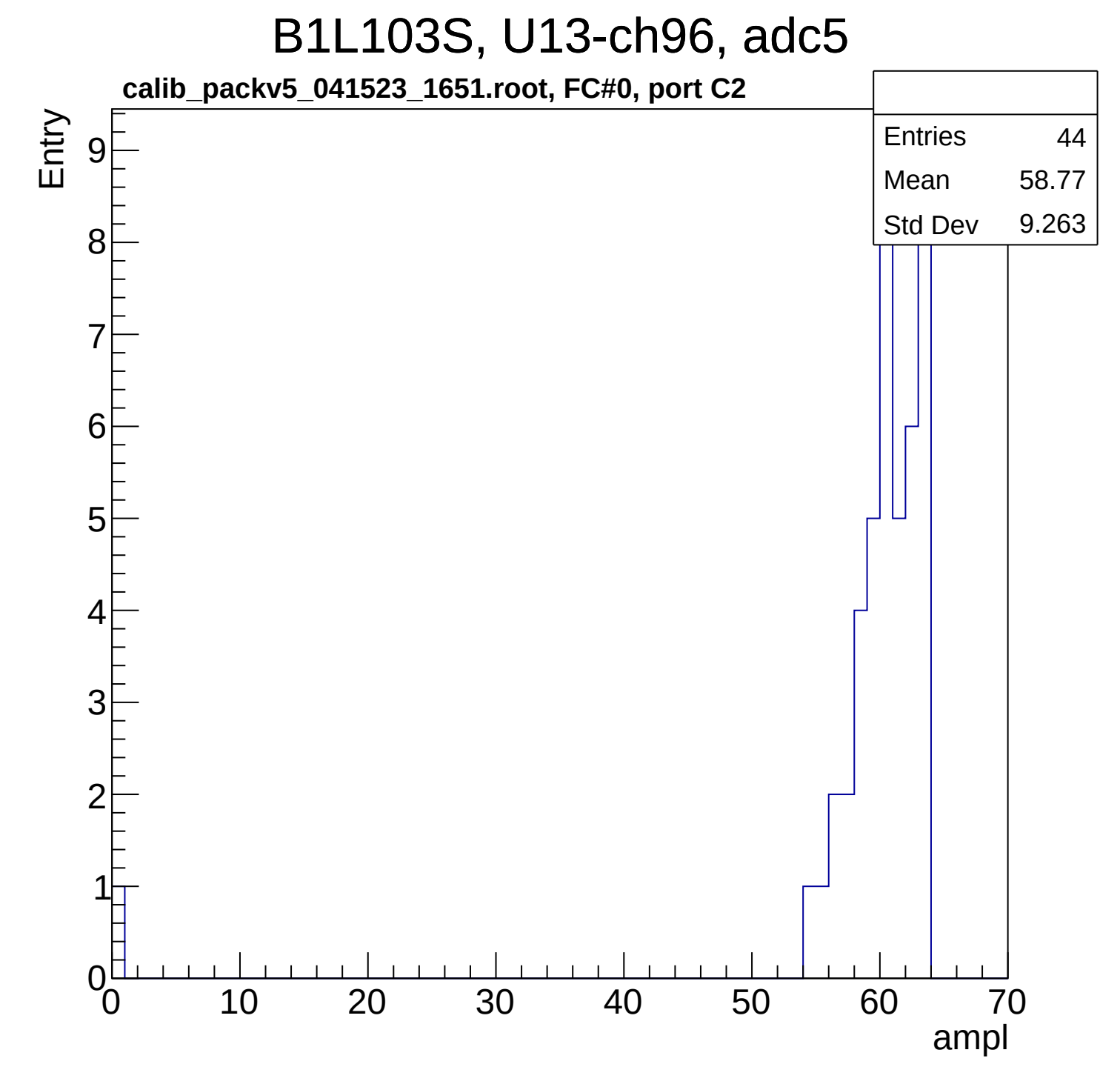

B1L103S, U13-ch96, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 26.38
Std Dev 11.78
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U13-ch96, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 32.21
Std Dev 14.74
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch96, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 44.19
Std Dev 3.523
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch96, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 49.84
Std Dev 2.498
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch96, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 55.64
Std Dev 7.723
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch96, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 58.77
Std Dev 9.263
Entry
ampl
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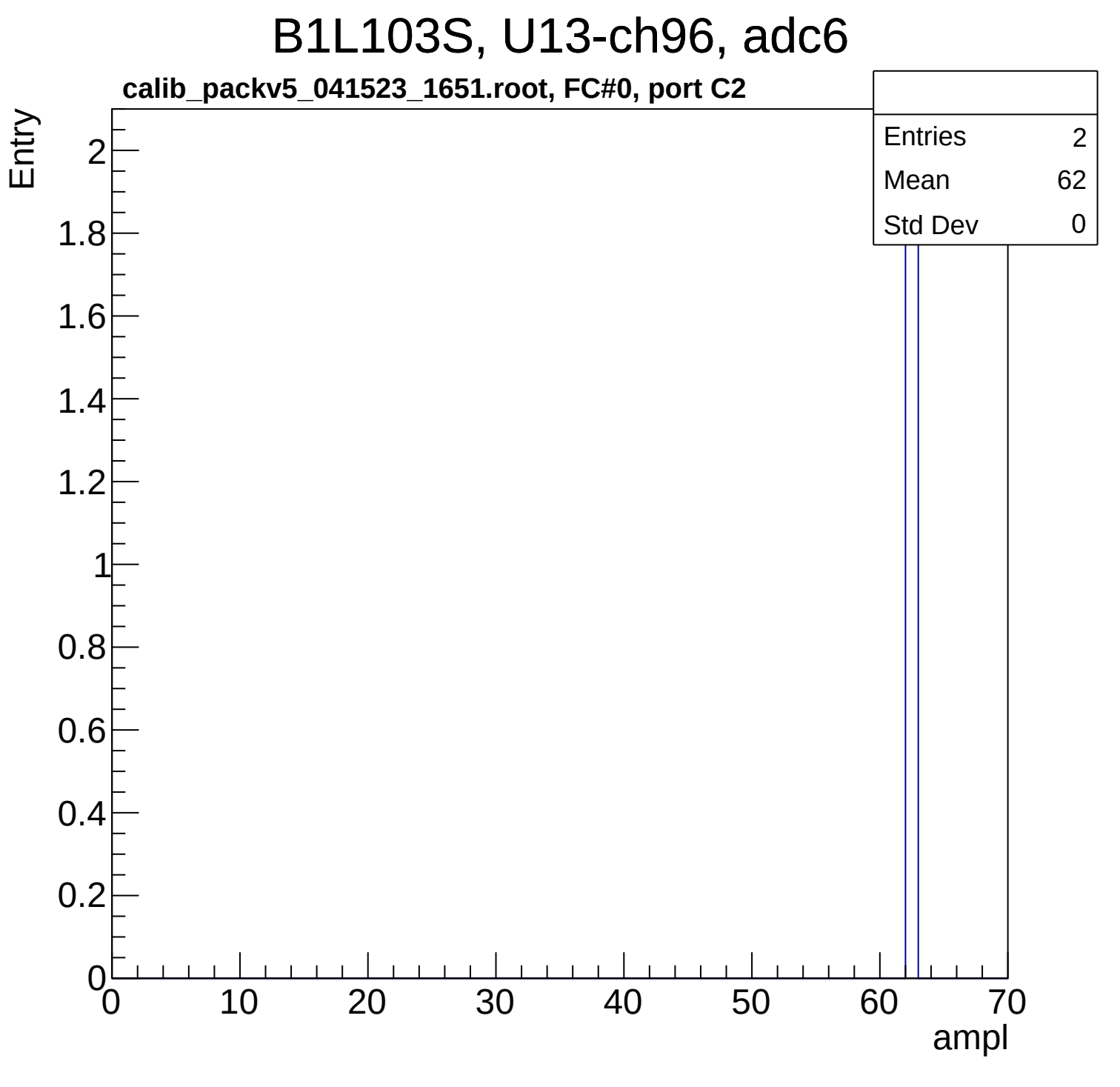
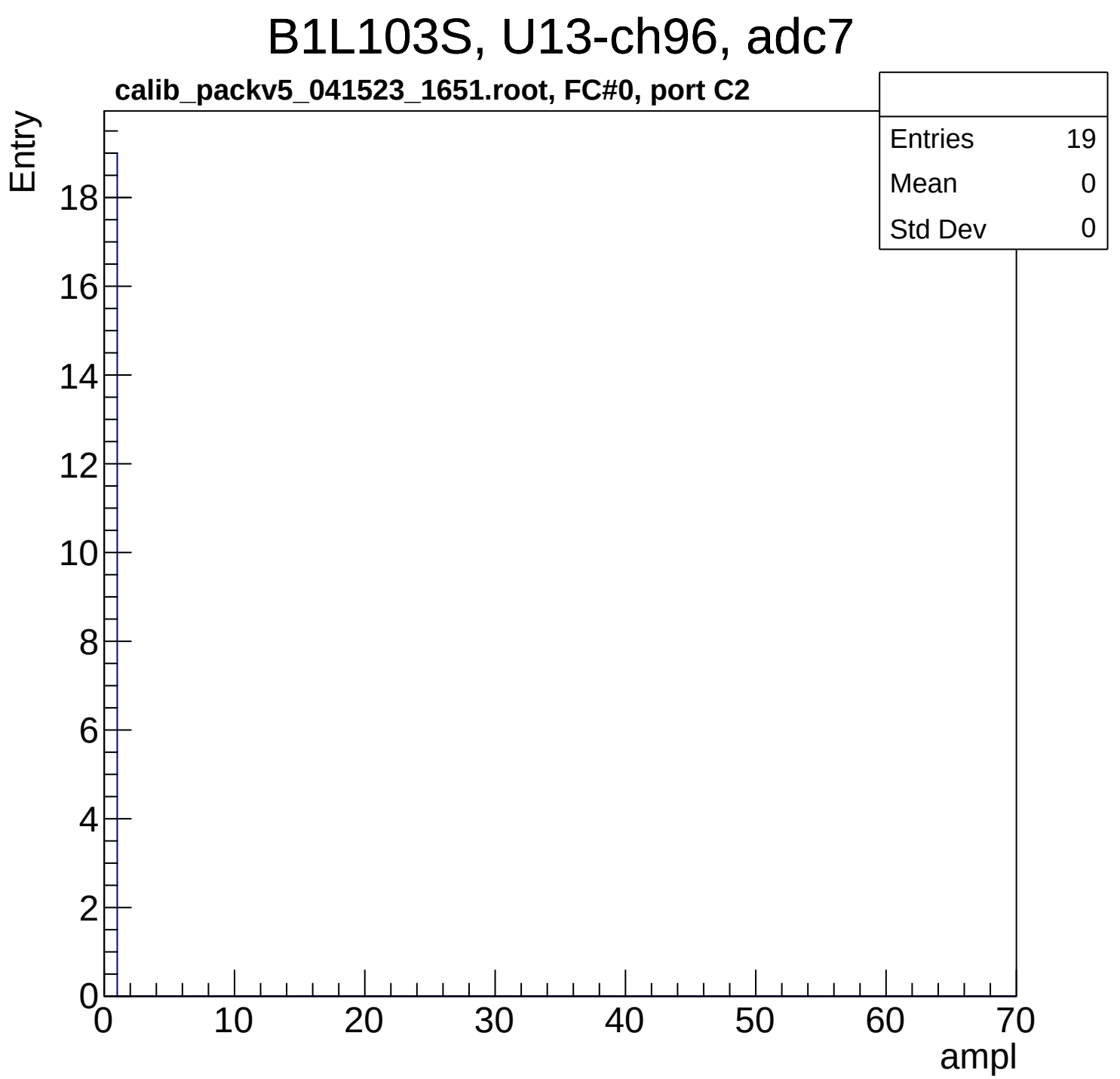
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch96, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U13-ch96, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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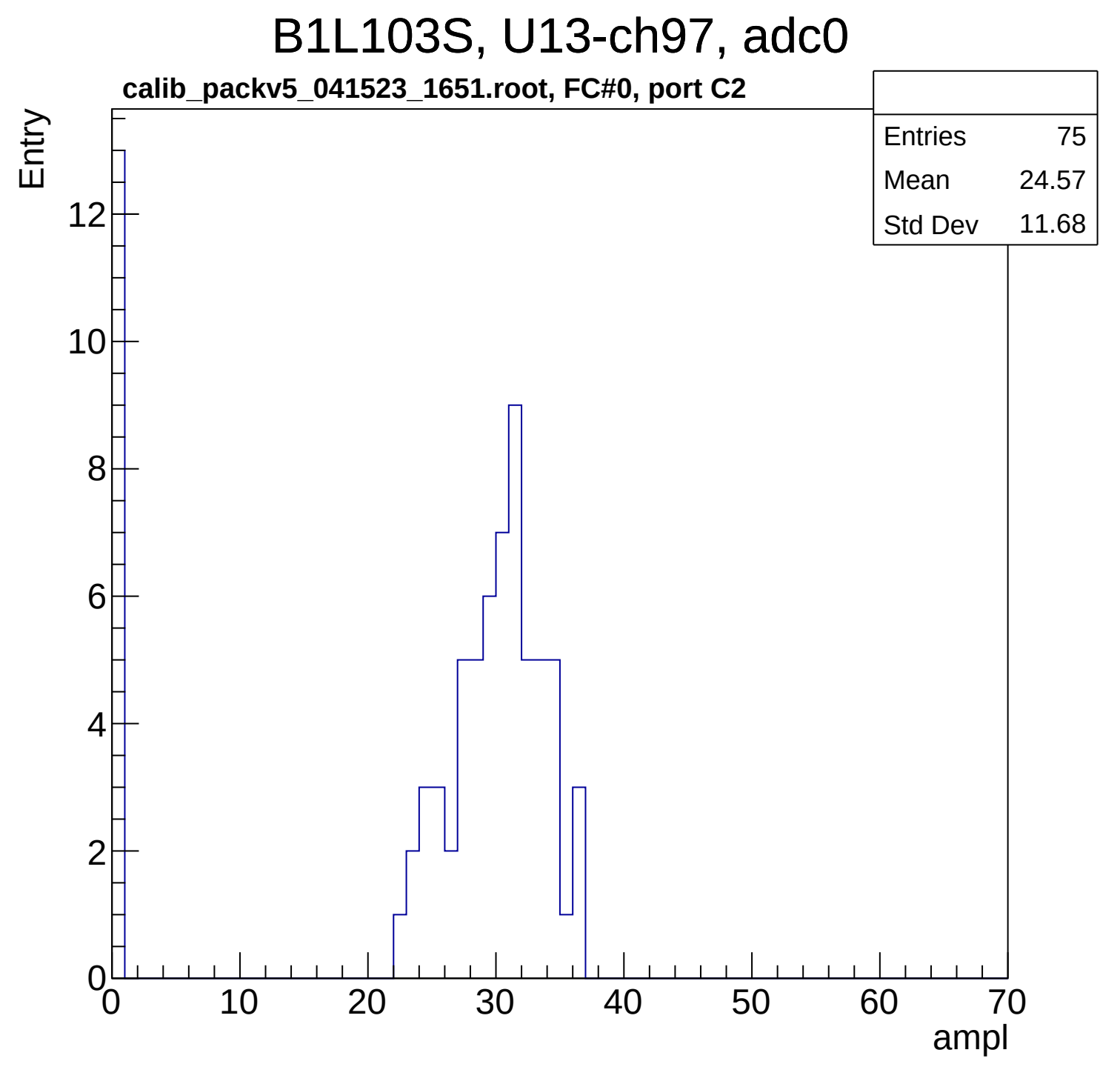
50
60
70
ampl


B1L103S, U13-ch97, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 24.57
Std Dev 11.68
Entry
0
2
4
6
8
10
12
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10
20
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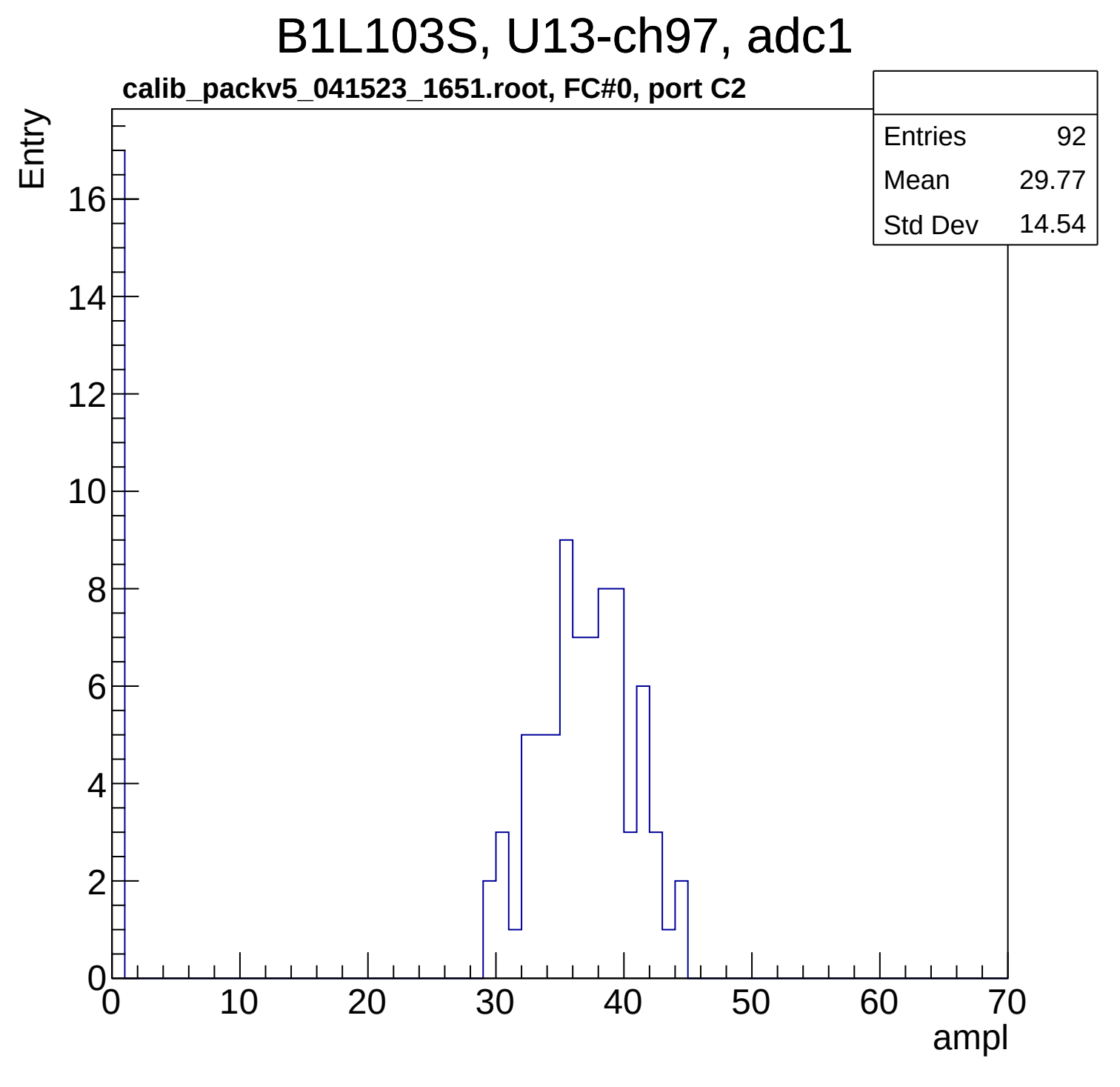
50
60
70
ampl


B1L103S, U13-ch97, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 29.77
Std Dev 14.54
Entry
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2
4
6
8
10
12
14
16
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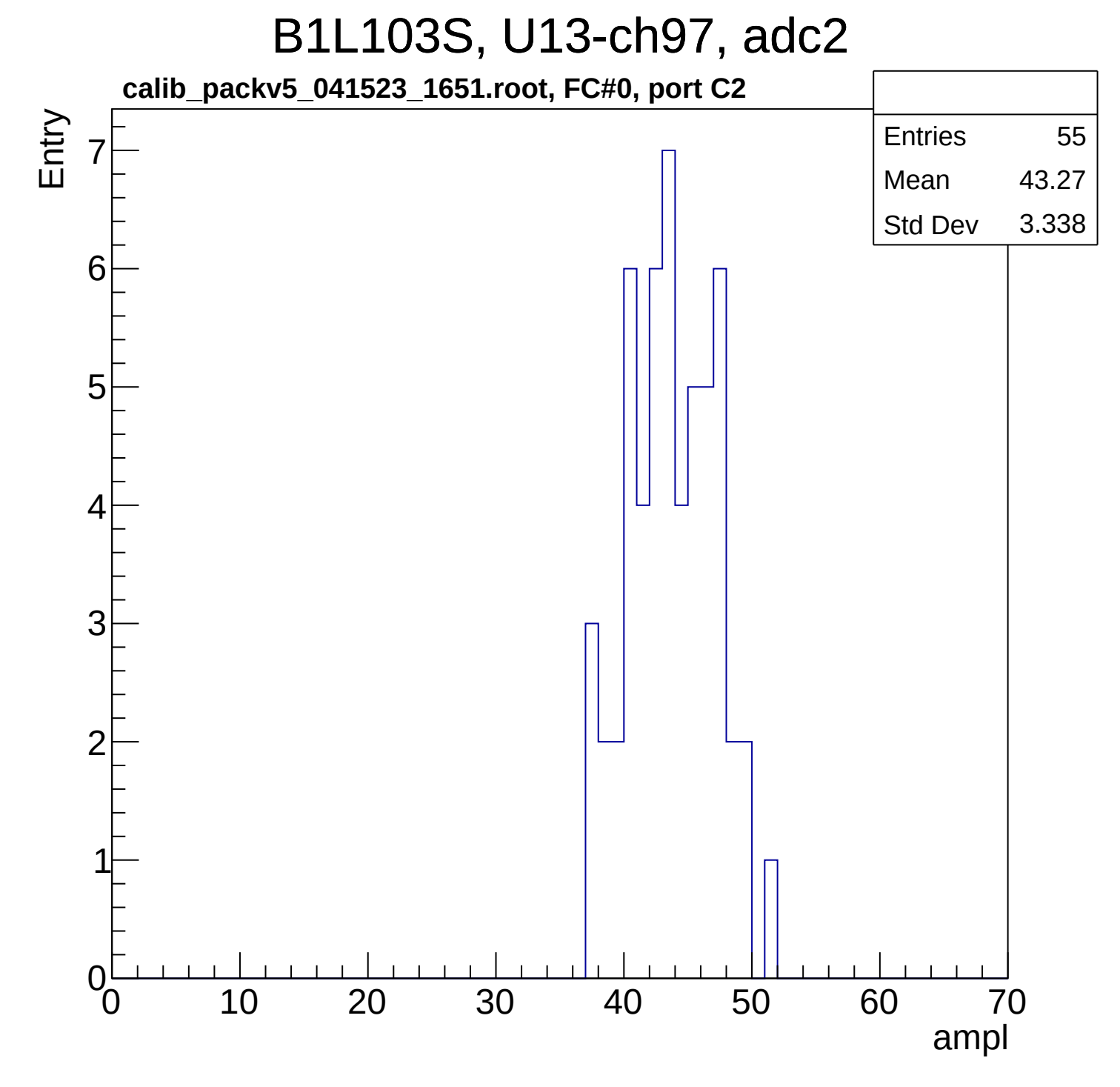
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch97, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 43.27
Std Dev 3.338
Entry
ampl
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1
2
3
4
5
6
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0
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40
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60
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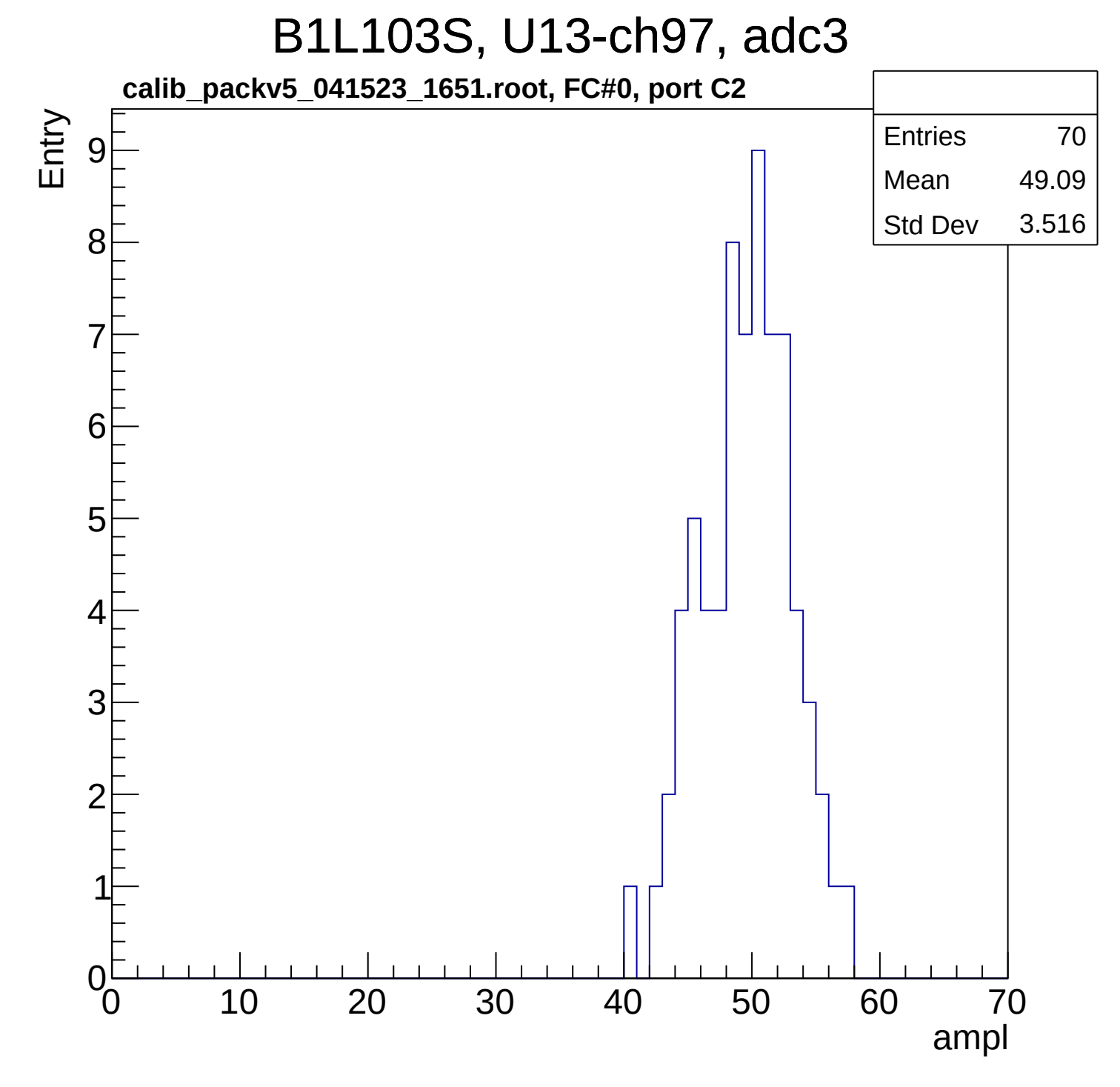
B1L103S, U13-ch97, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 49.09
Std Dev 3.516
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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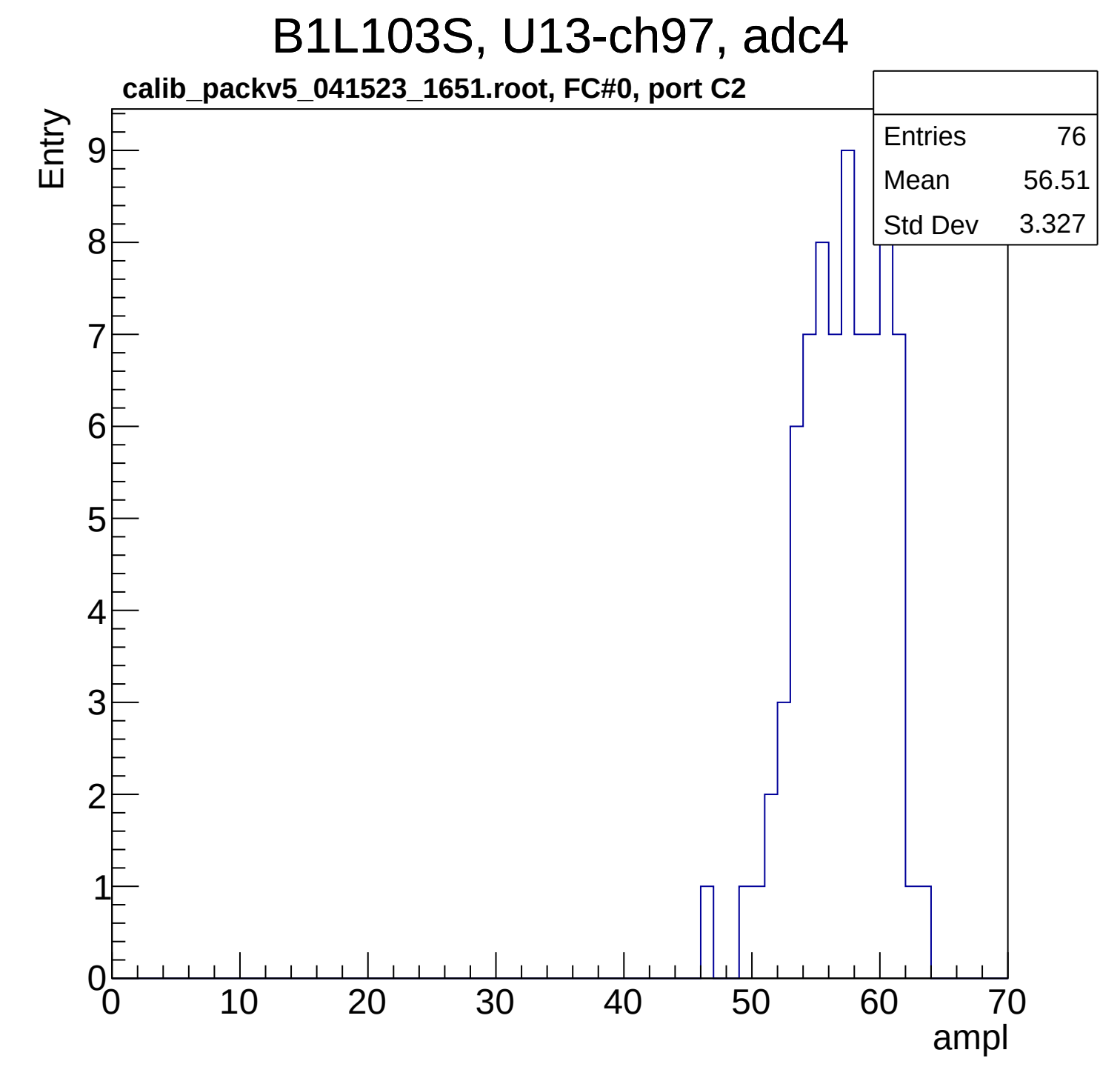
B1L103S, U13-ch97, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 56.51
Std Dev 3.327
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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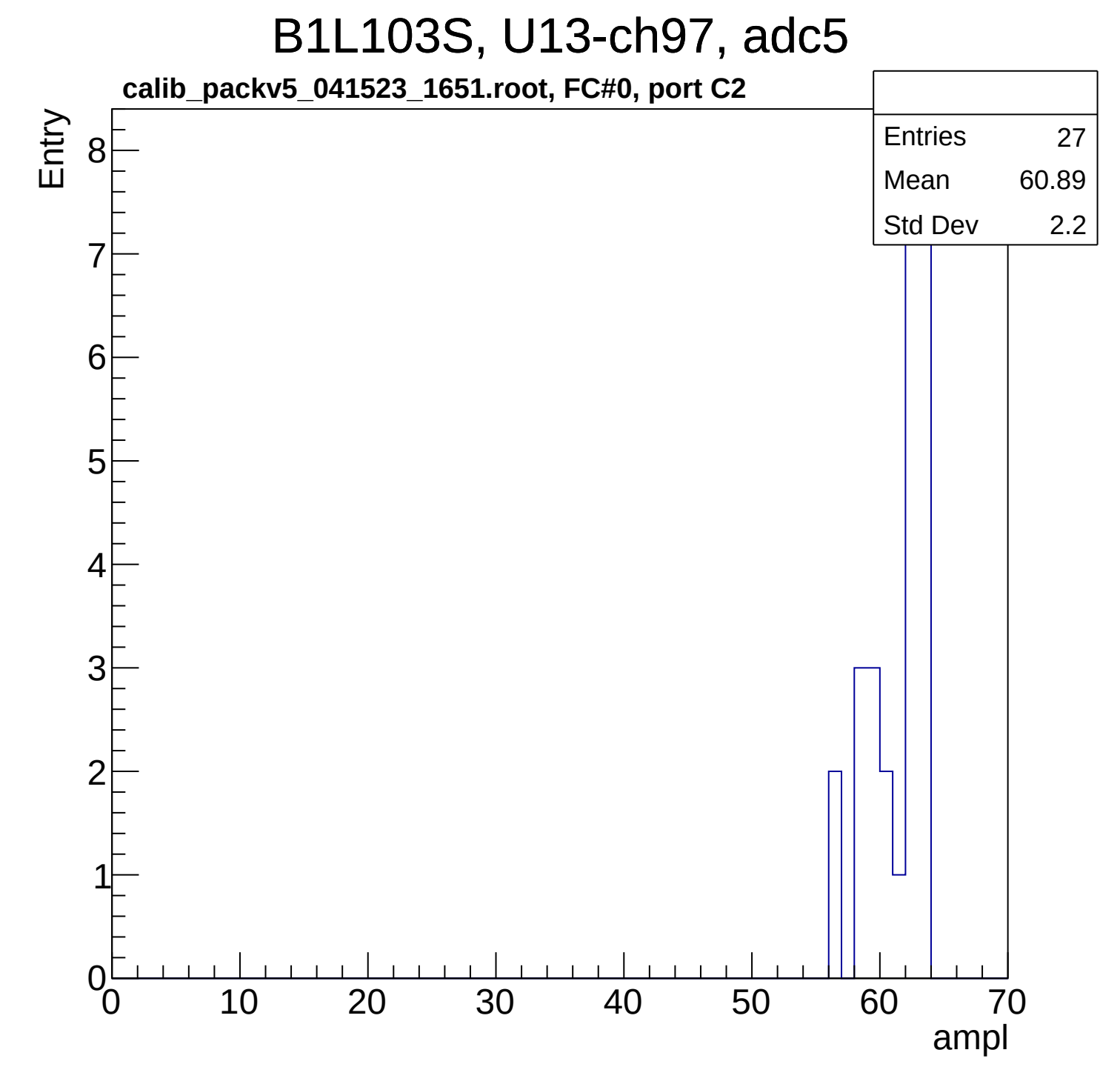
B1L103S, U13-ch97, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 60.89
Std Dev 2.2
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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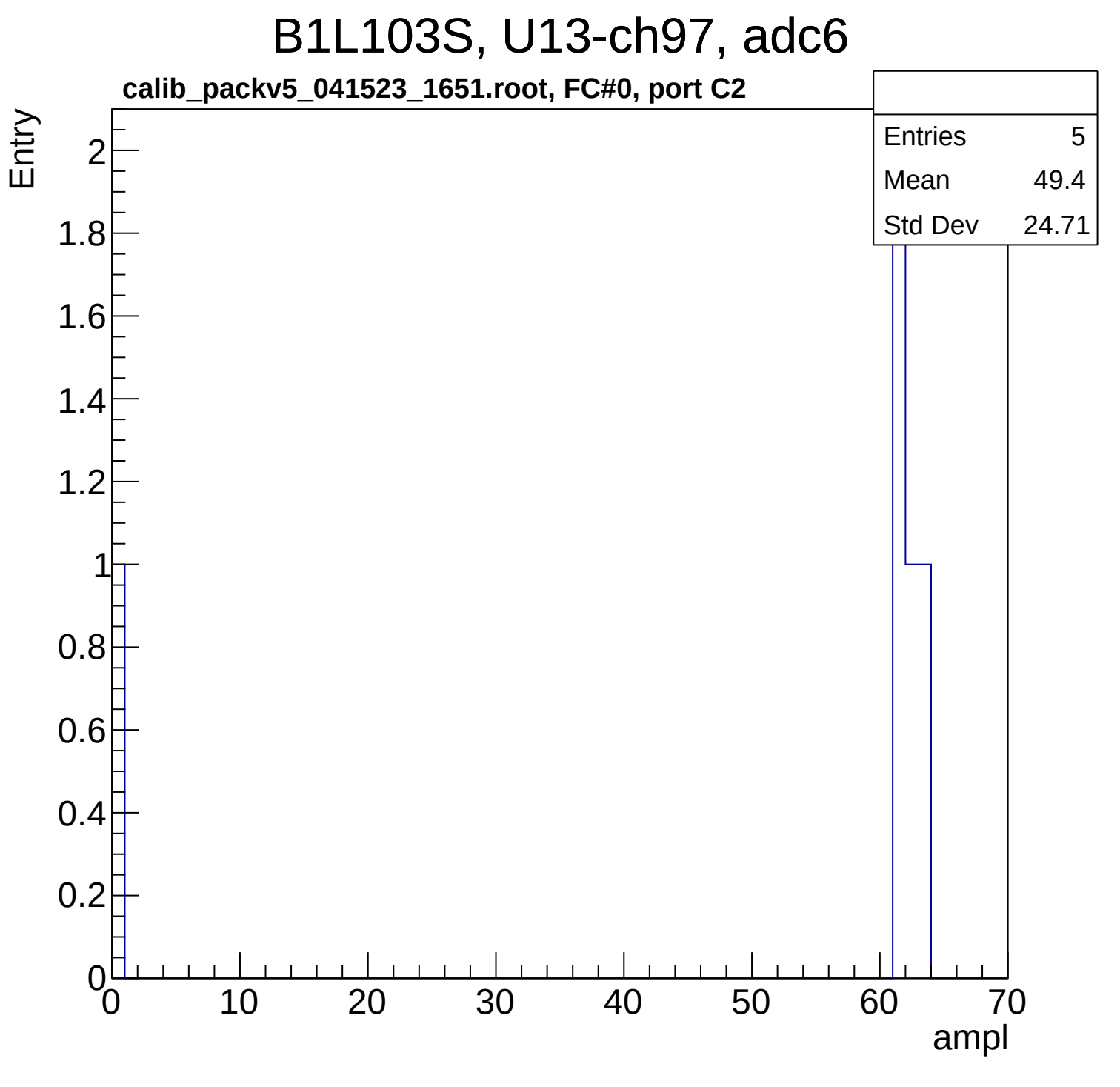
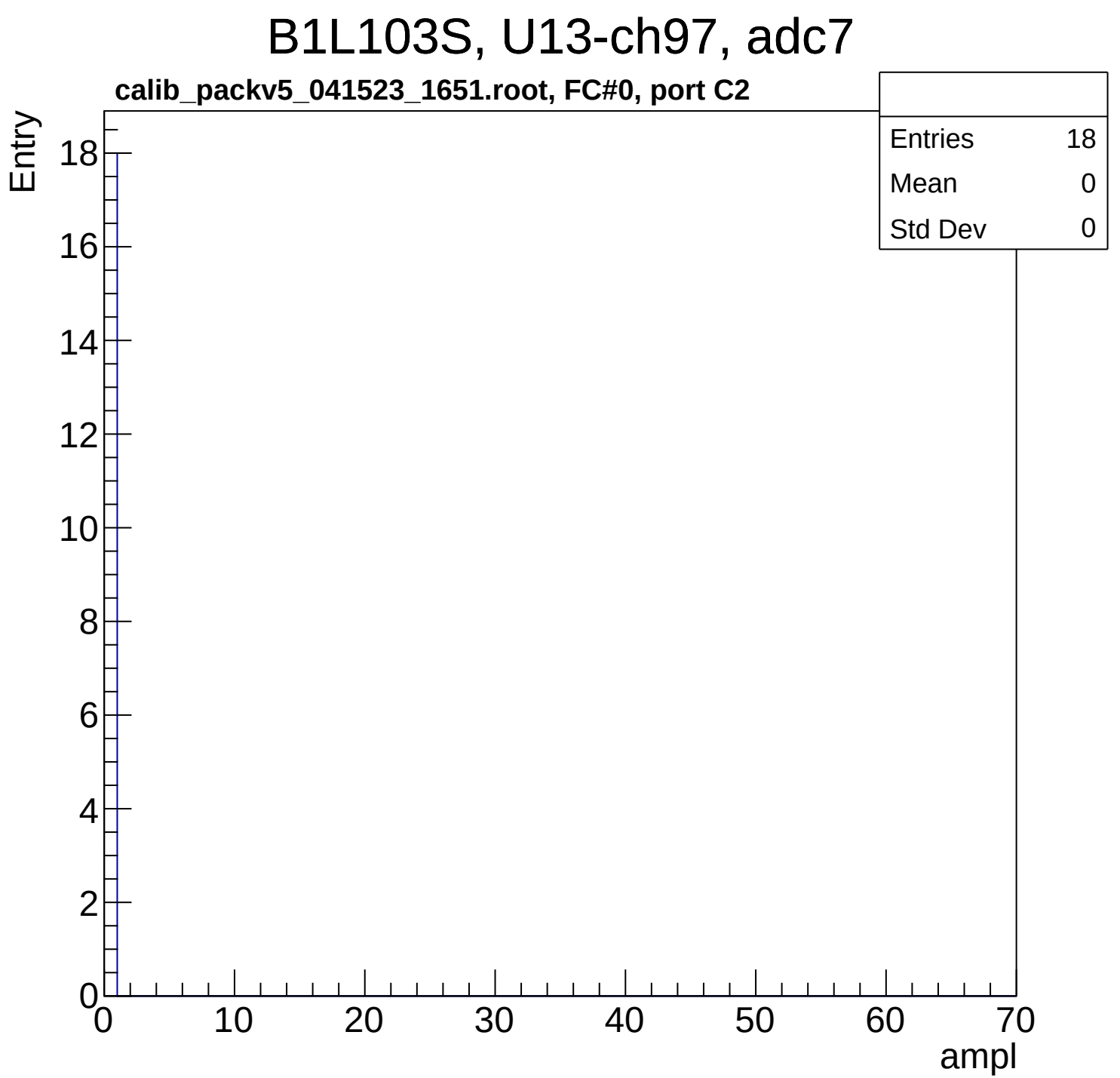
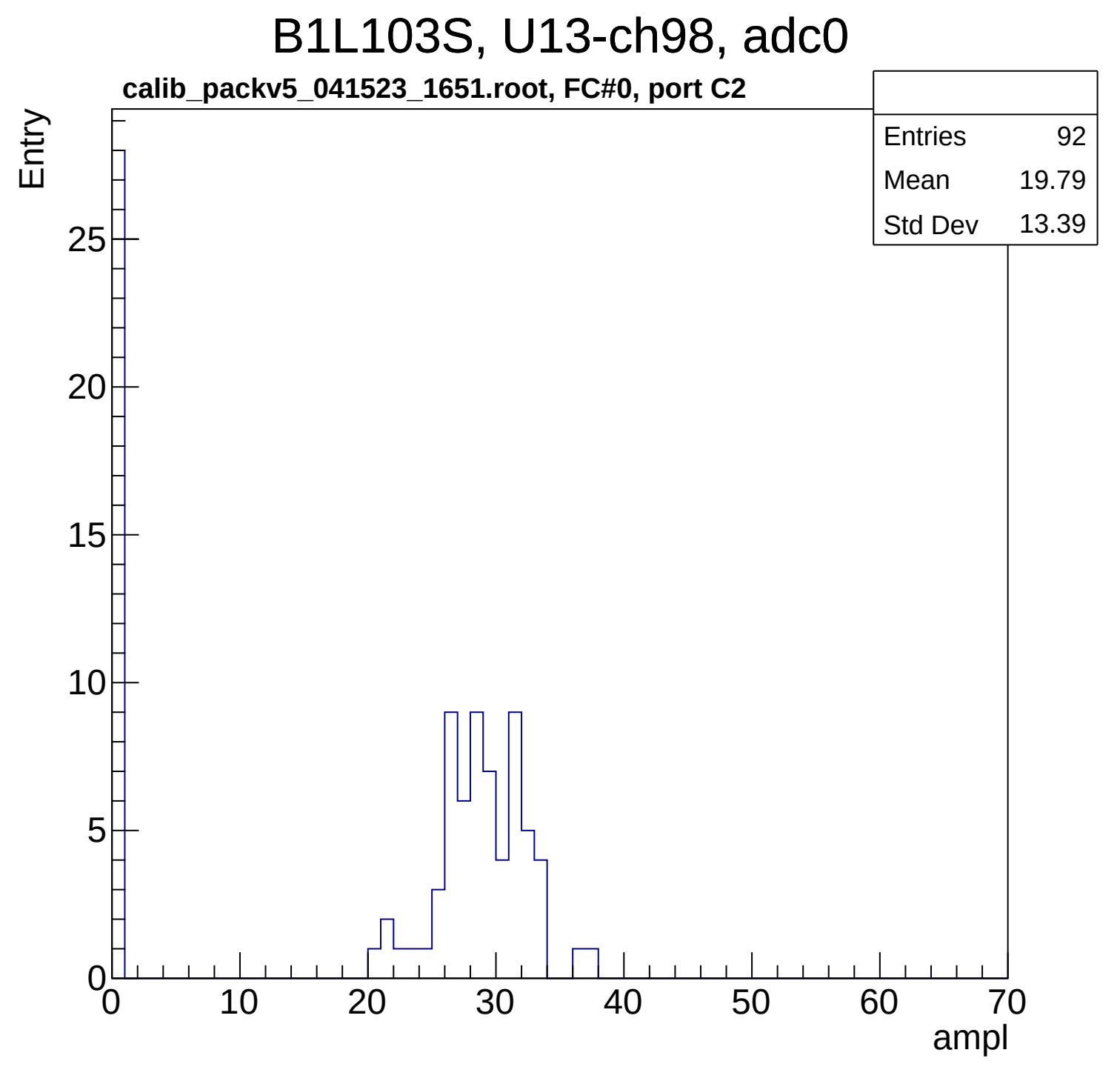
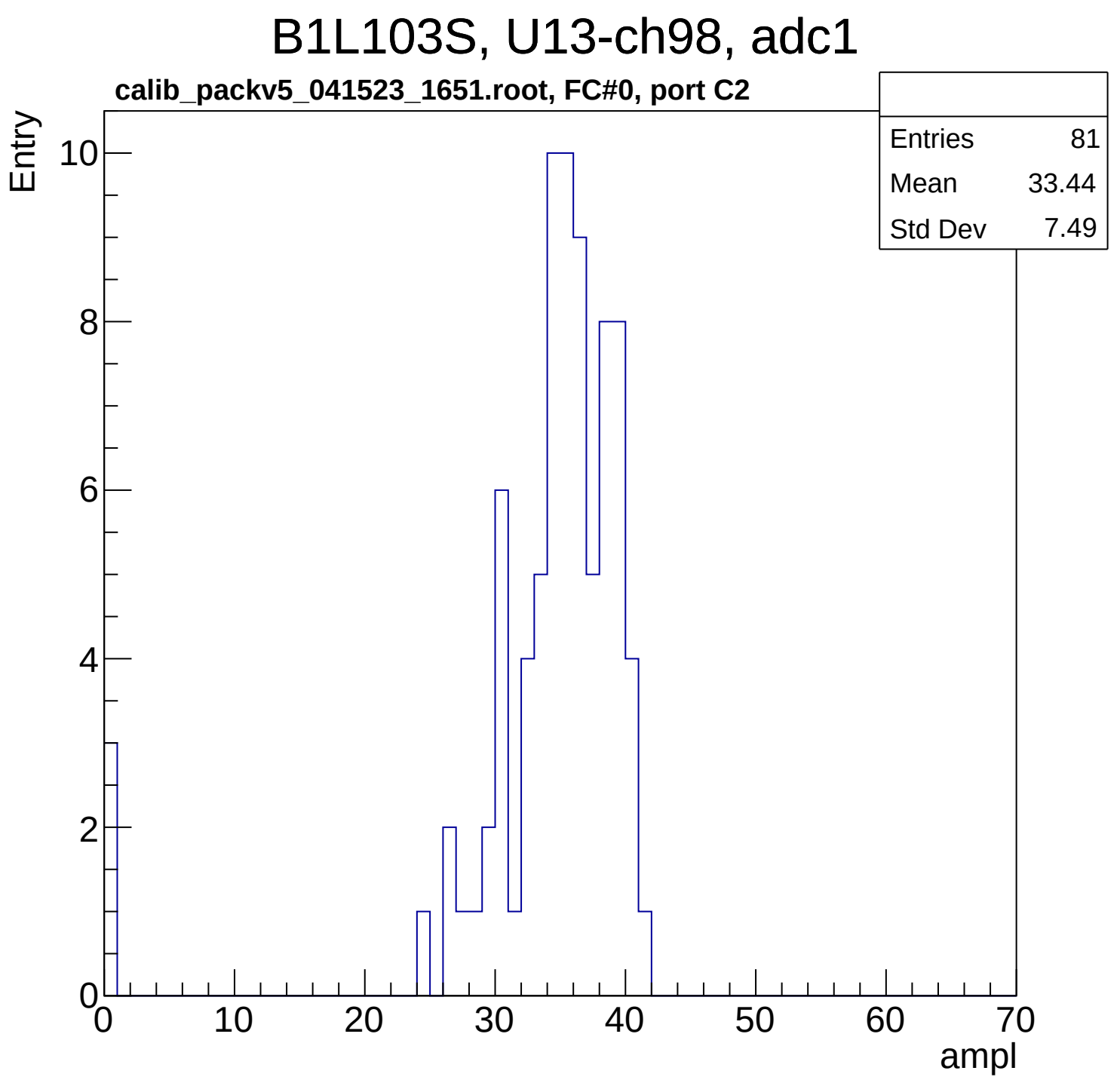
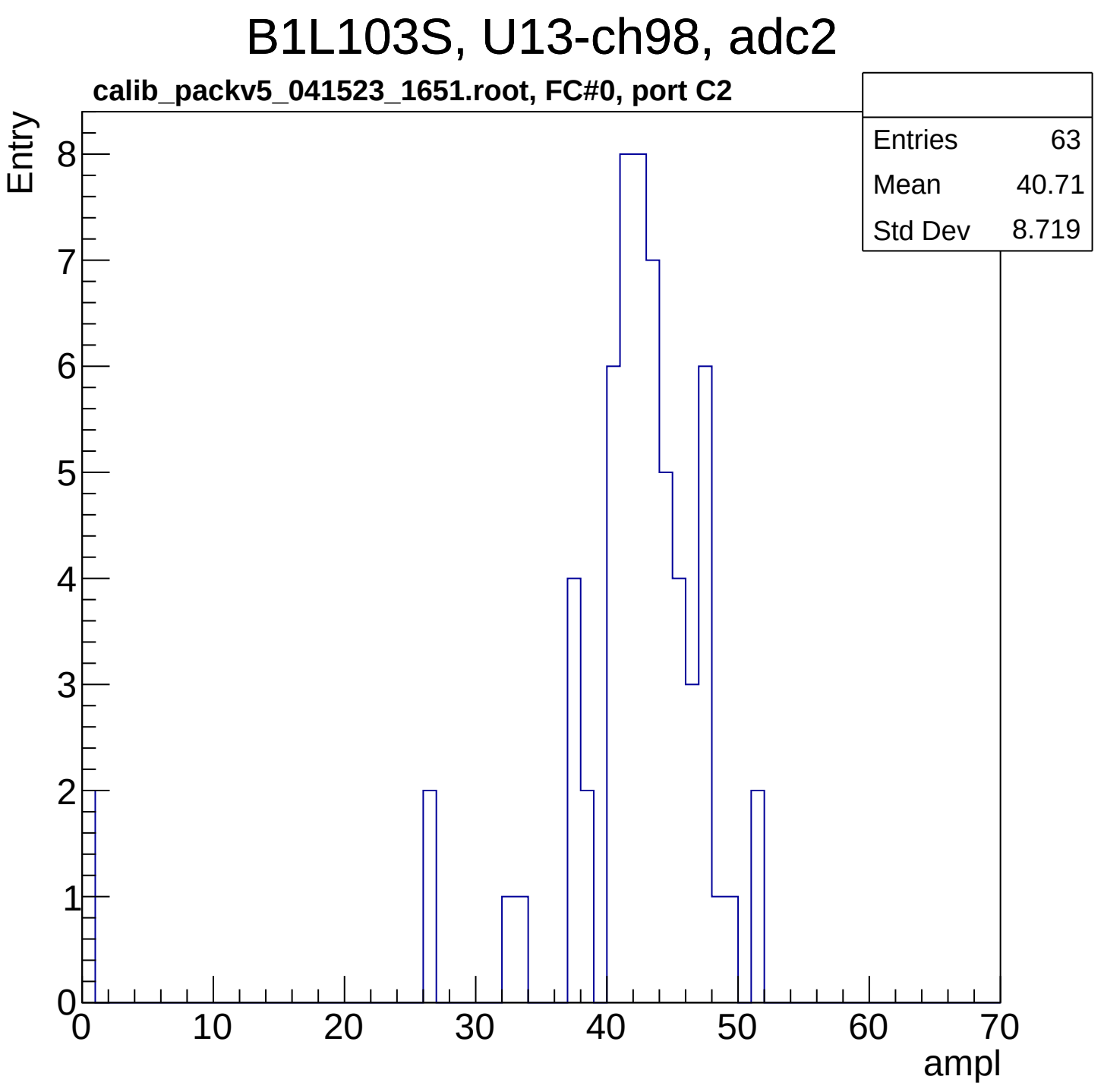

B1L103S, U13-ch97, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 49.4
Std Dev 24.71
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U13-ch97, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch98, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 19.79
Std Dev 13.39
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch98, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 33.44
Std Dev 7.49
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch98, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 40.71
Std Dev 8.719
Entry
ampl
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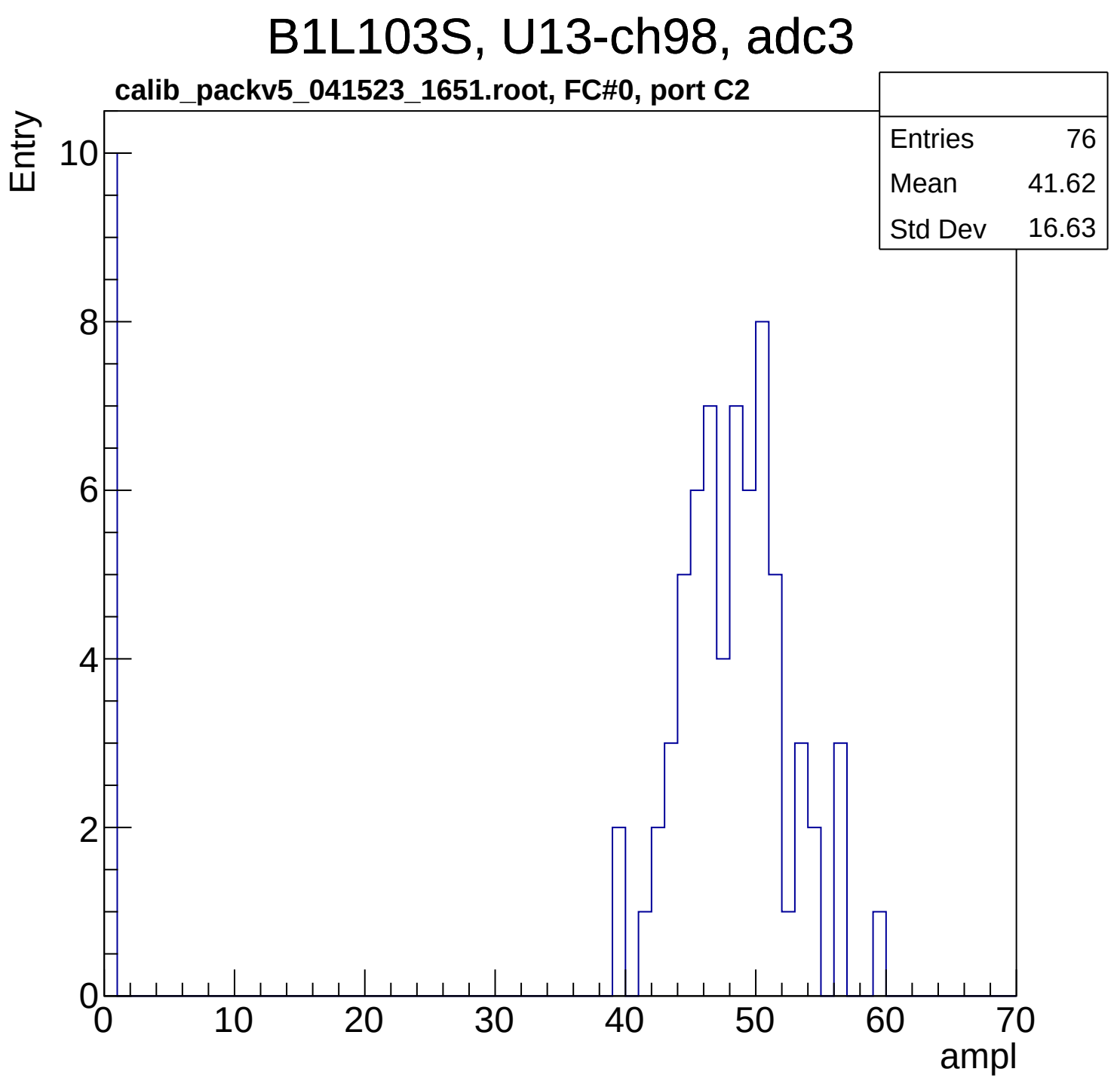
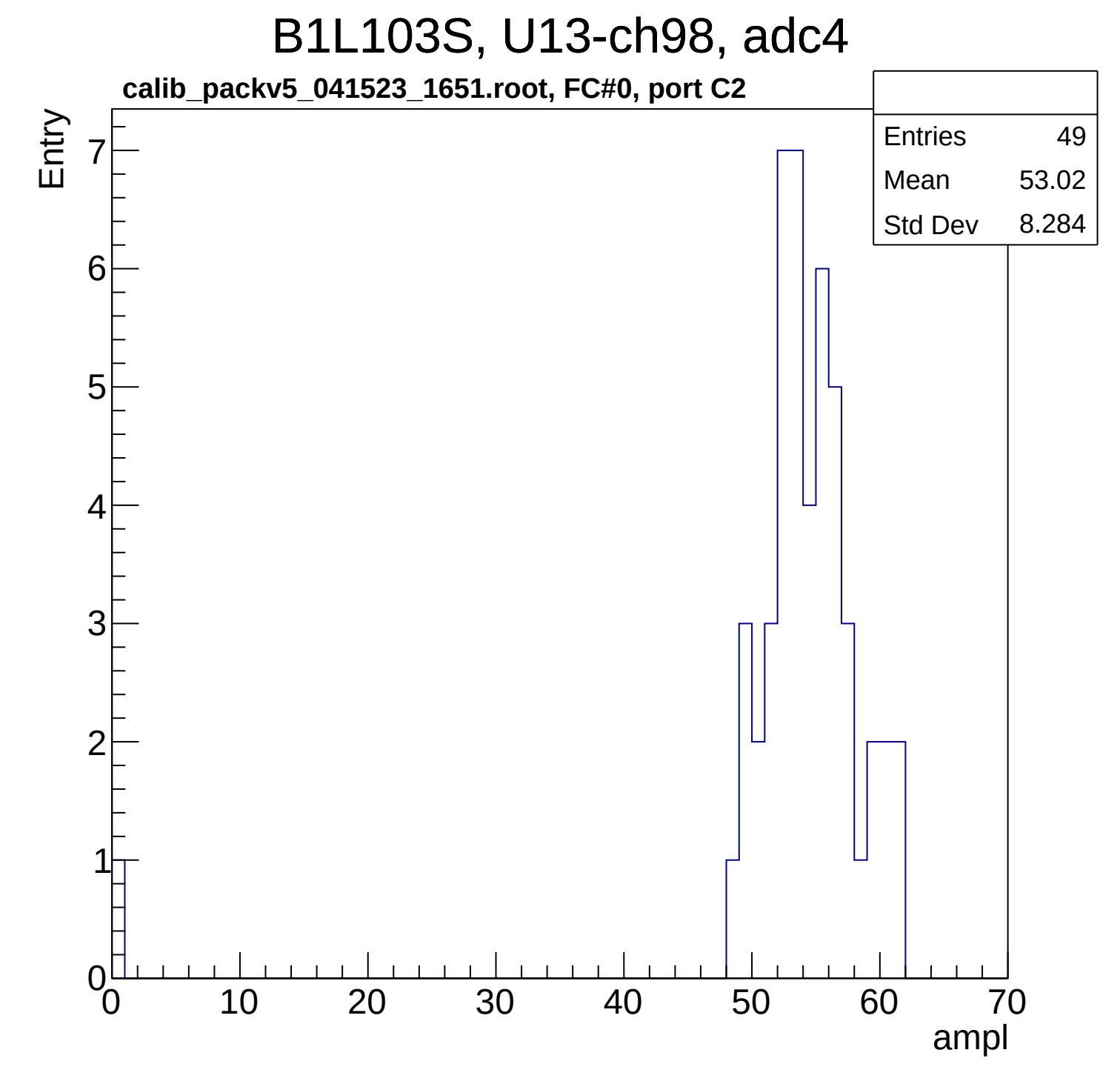
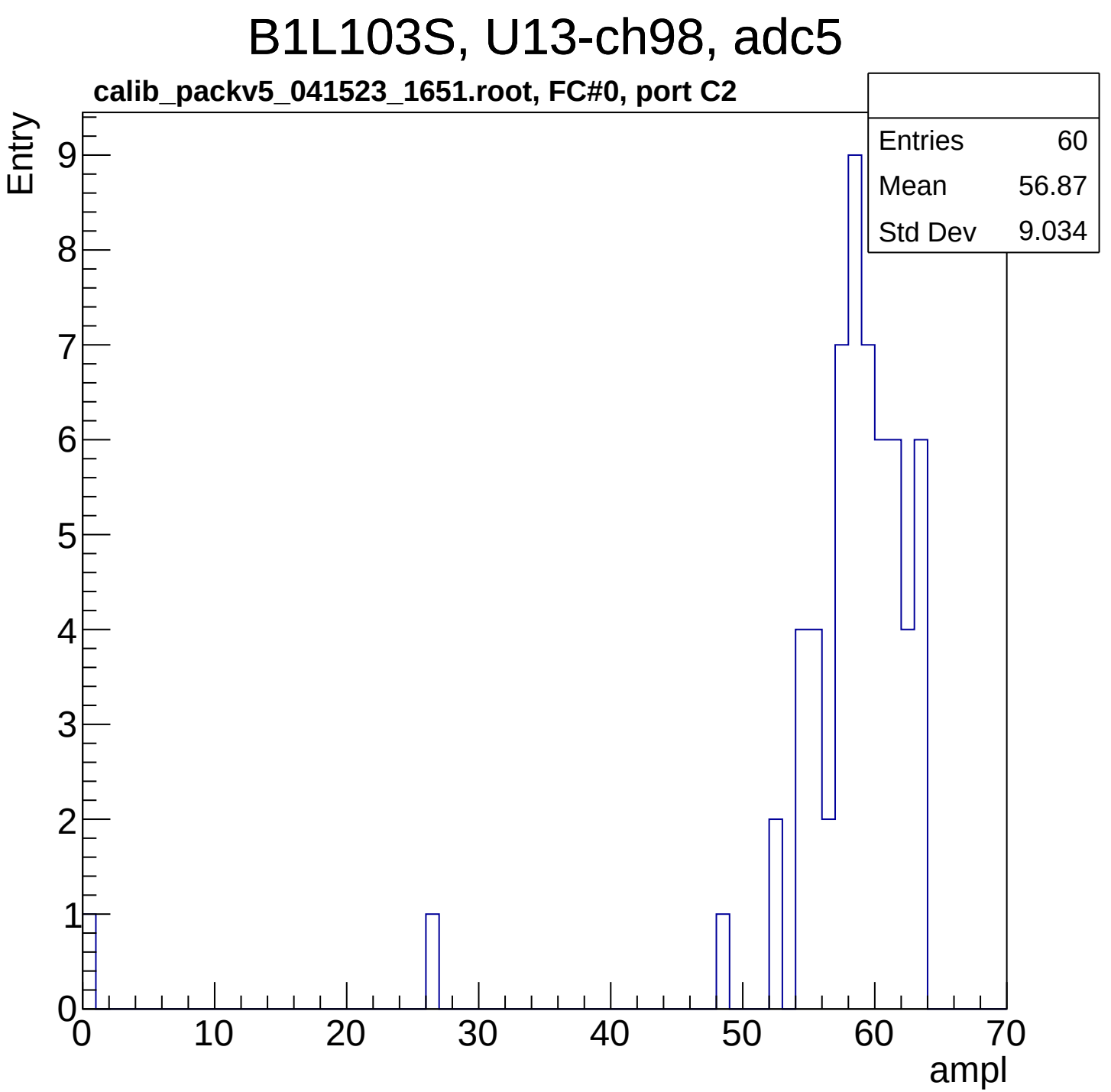
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch98, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 41.62
Std Dev 16.63
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch98, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 53.02
Std Dev 8.284
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch98, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 56.87
Std Dev 9.034
Entry
ampl
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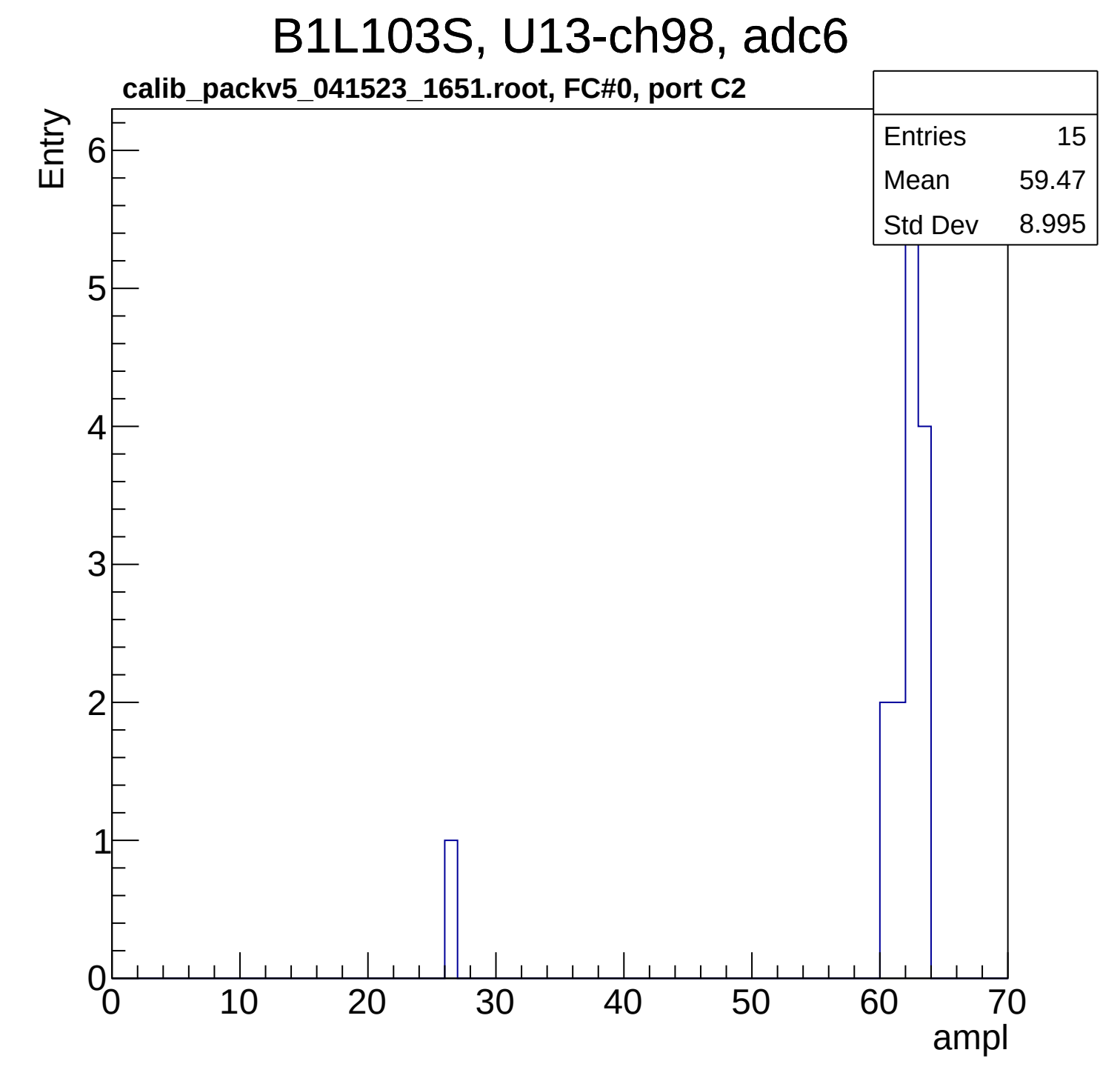
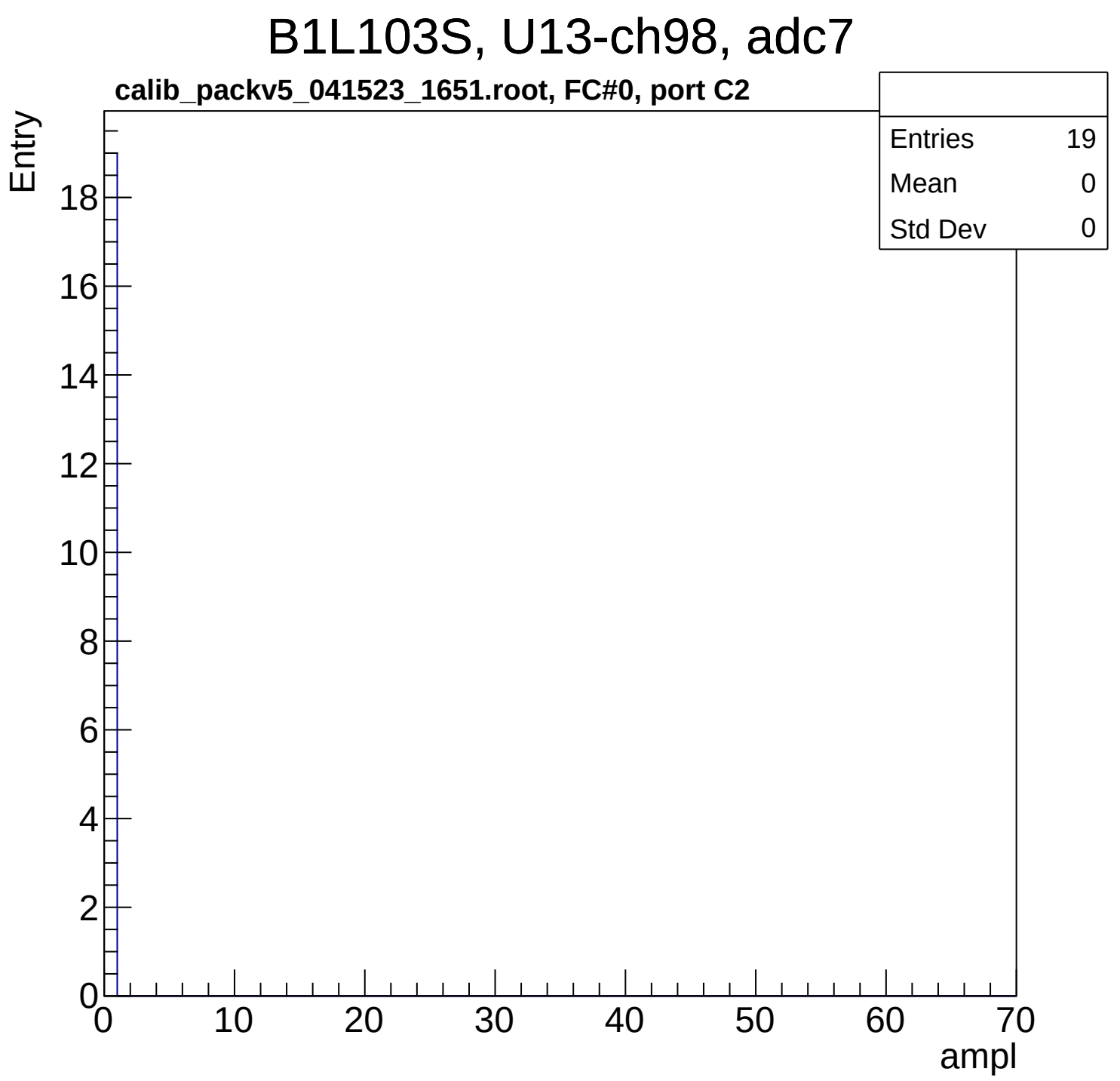
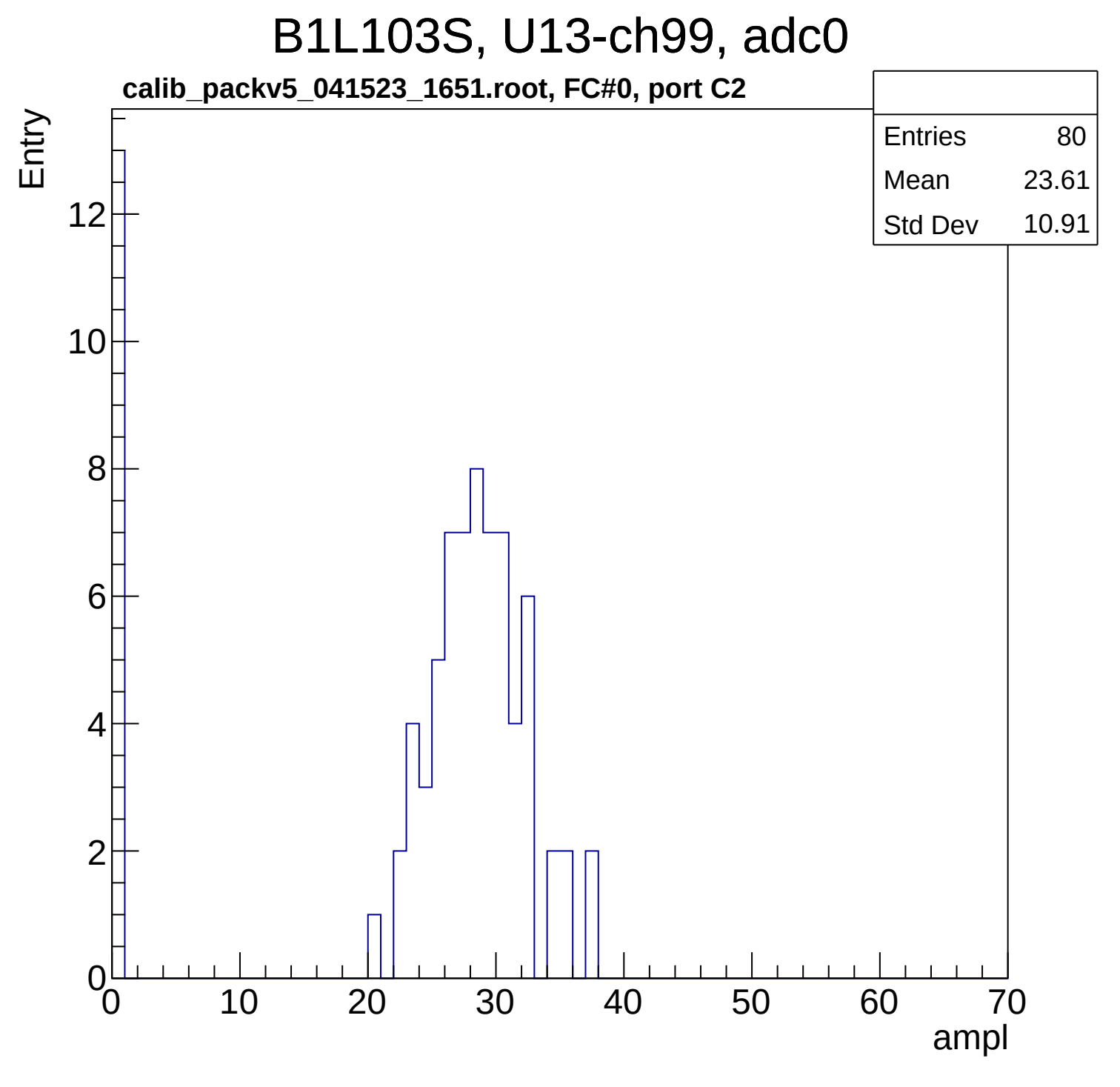
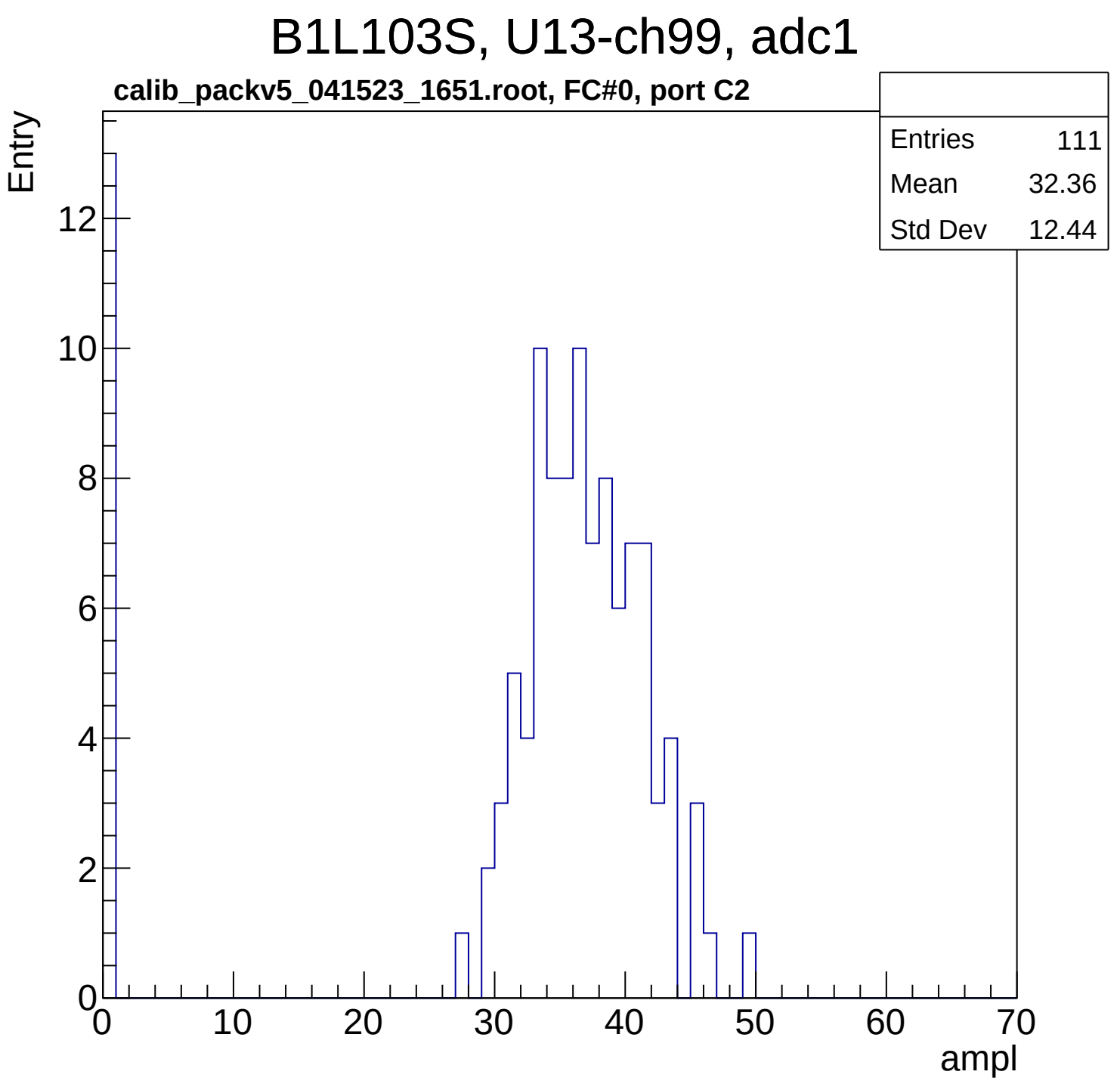
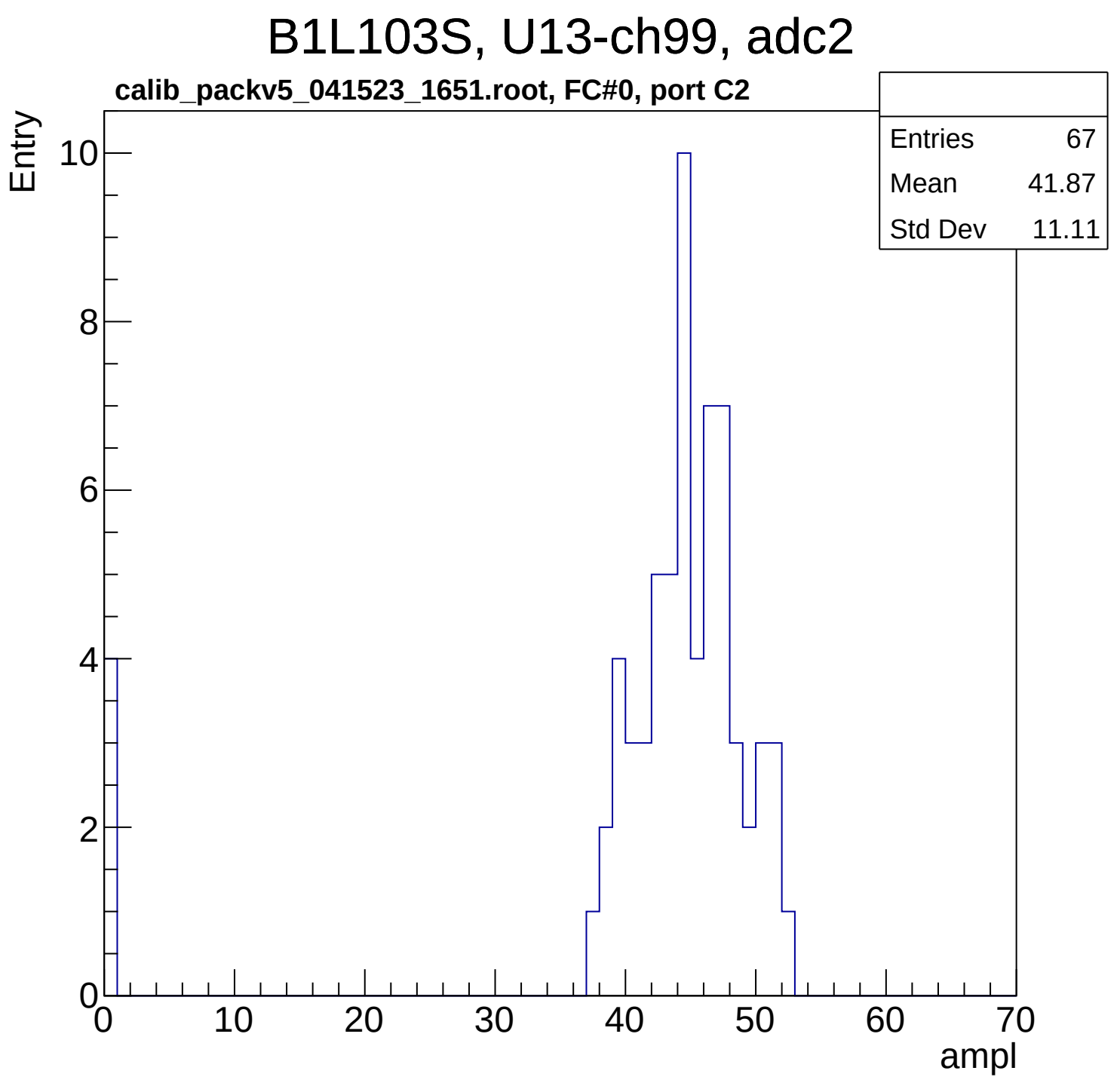
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

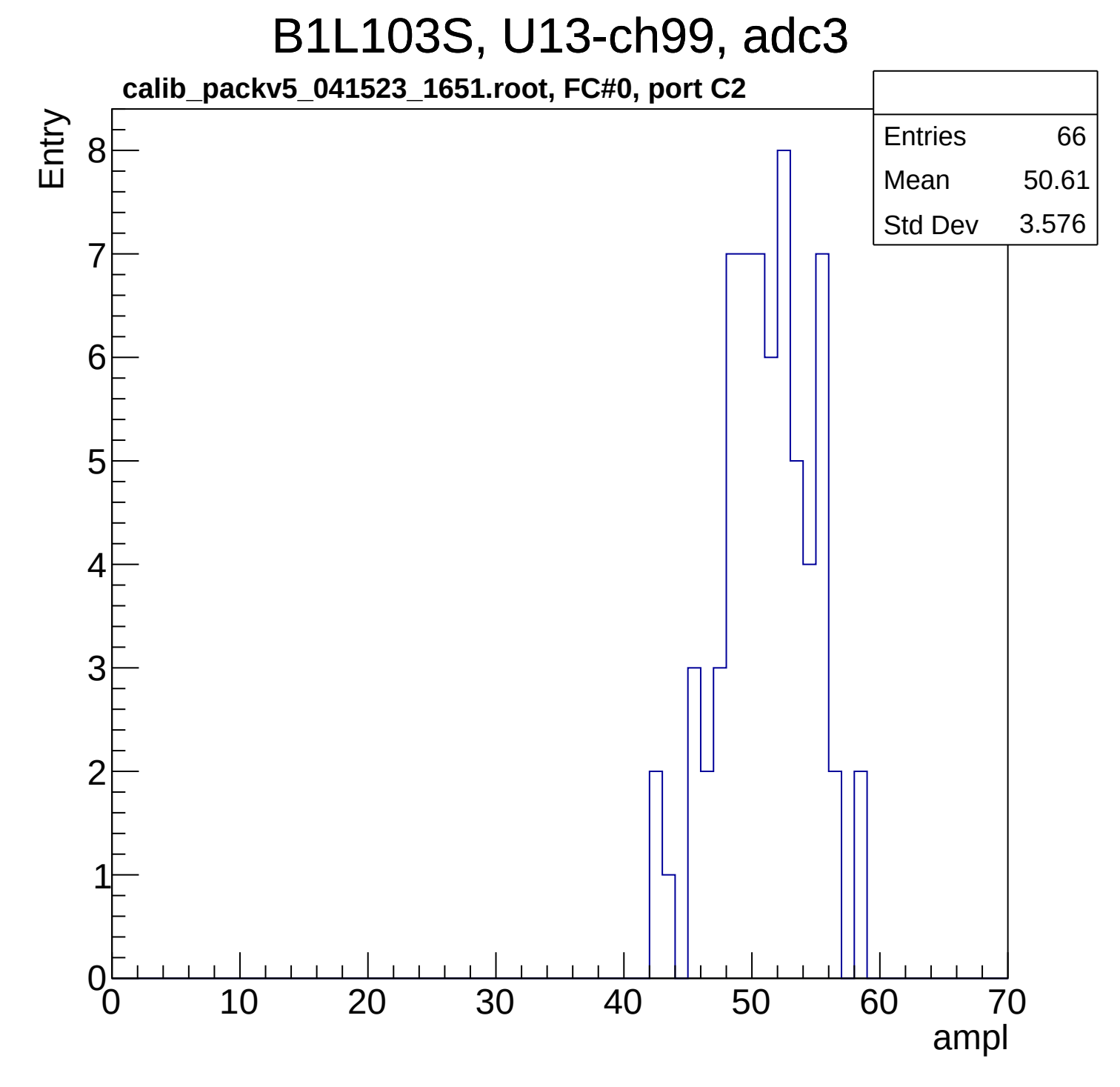

B1L103S, U13-ch98, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 59.47
Std Dev 8.995
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch98, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch99, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 23.61
Std Dev 10.91
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch99, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 111
Mean 32.36
Std Dev 12.44
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch99, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 41.87
Std Dev 11.11
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch99, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 50.61
Std Dev 3.576
Entry
ampl
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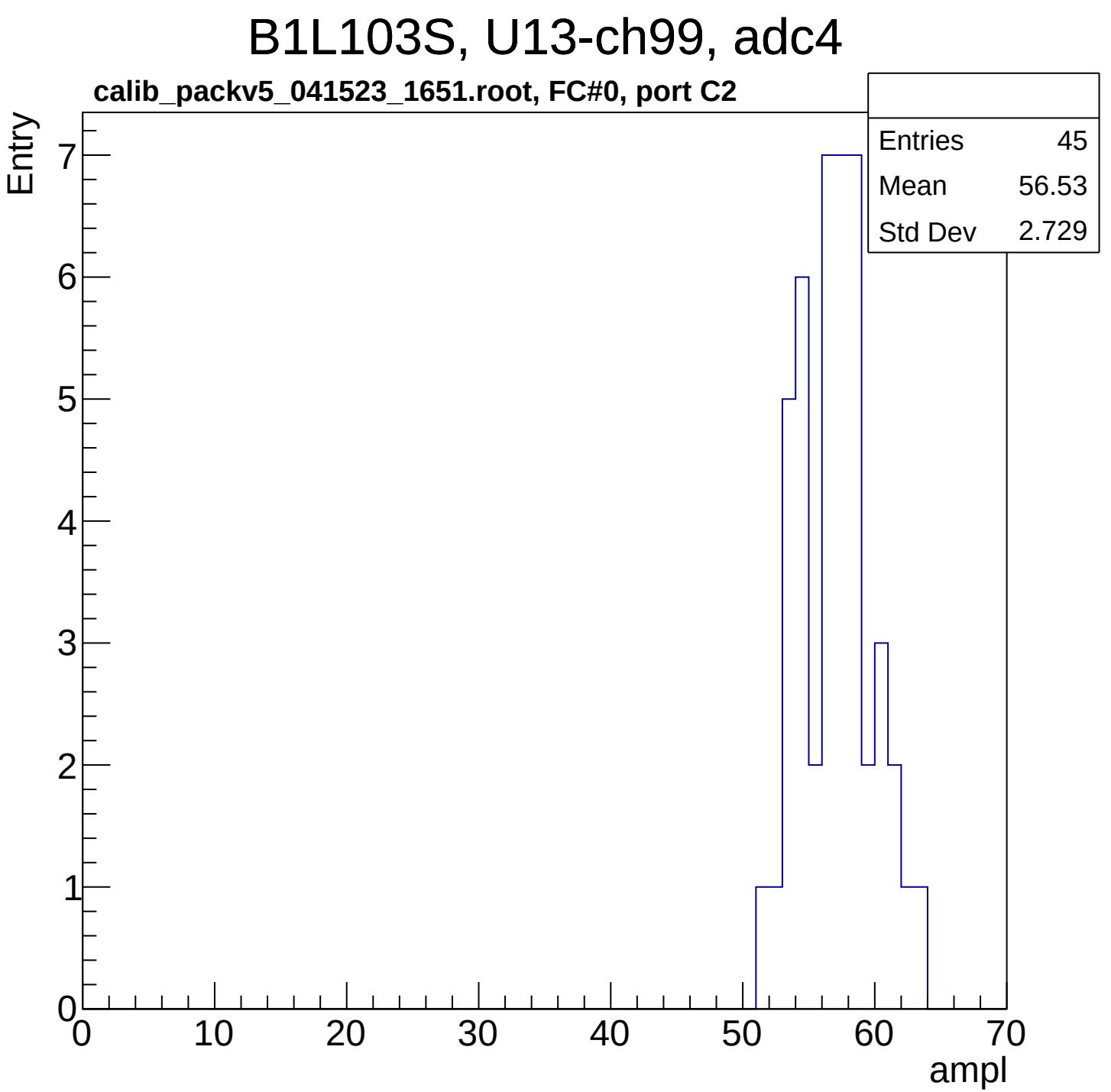
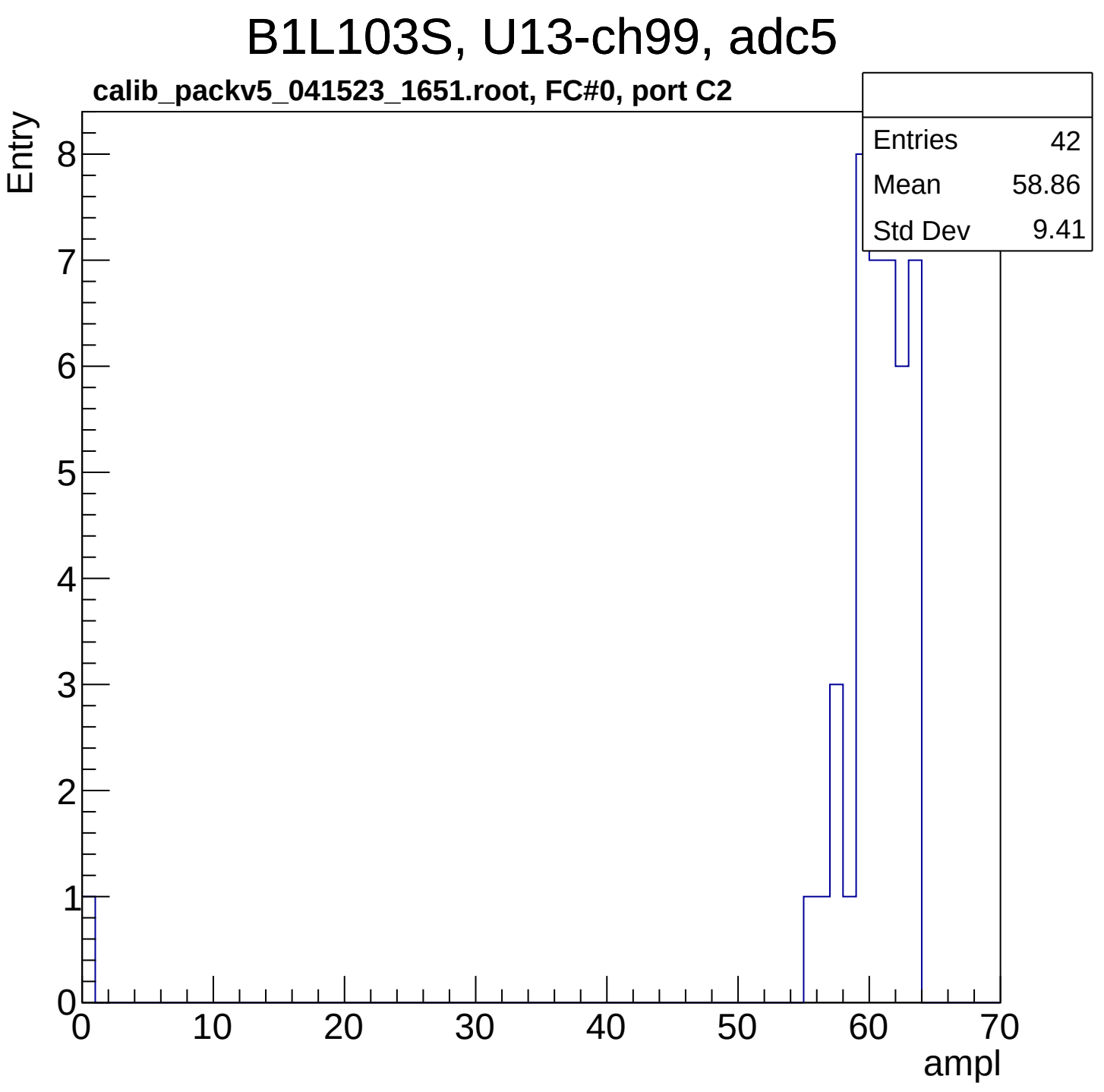
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch99, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 56.53
Std Dev 2.729
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch99, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 58.86
Std Dev 9.41
Entry
ampl
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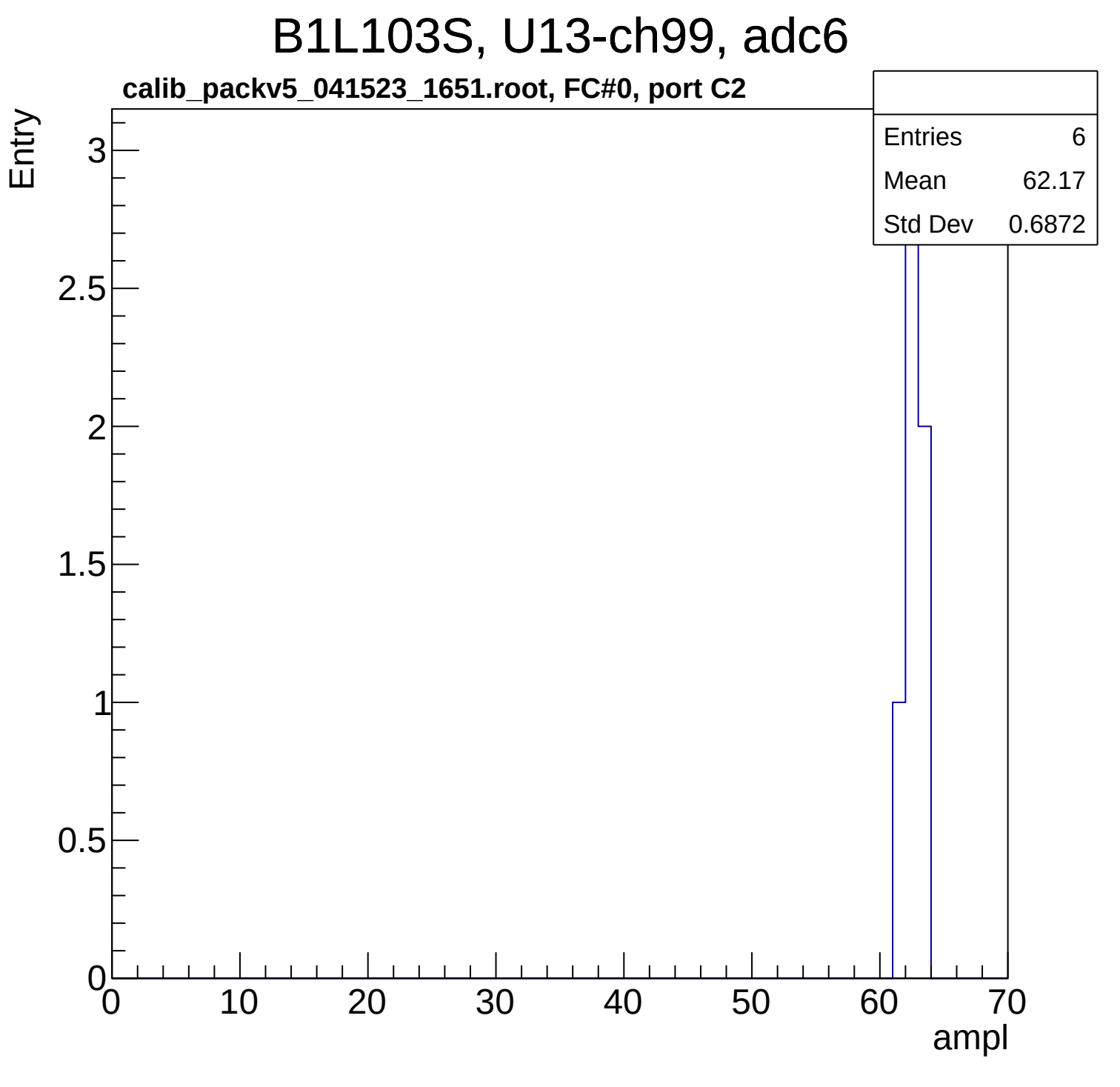
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch99, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.17
Std Dev 0.6872
Entry
ampl
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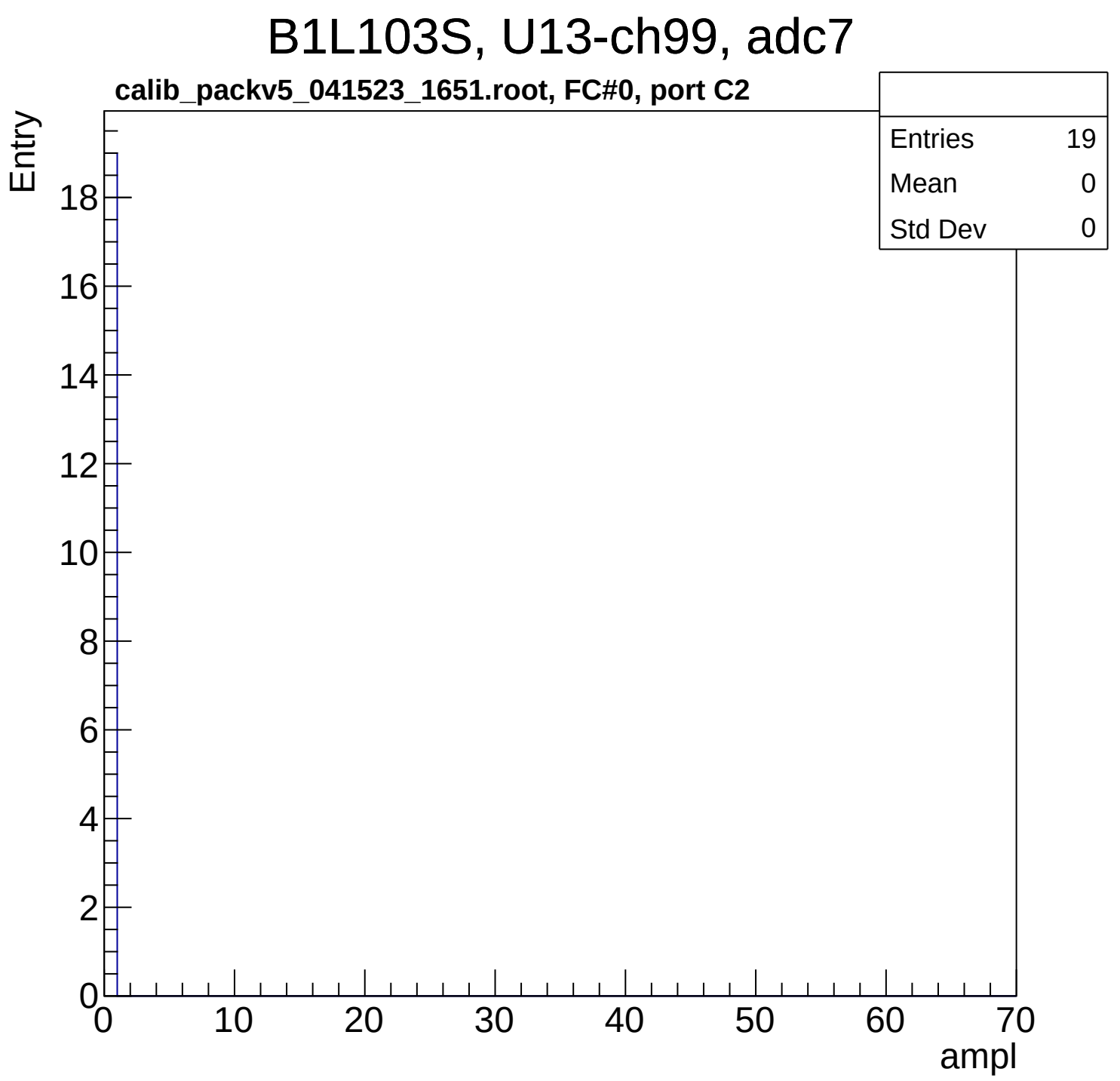
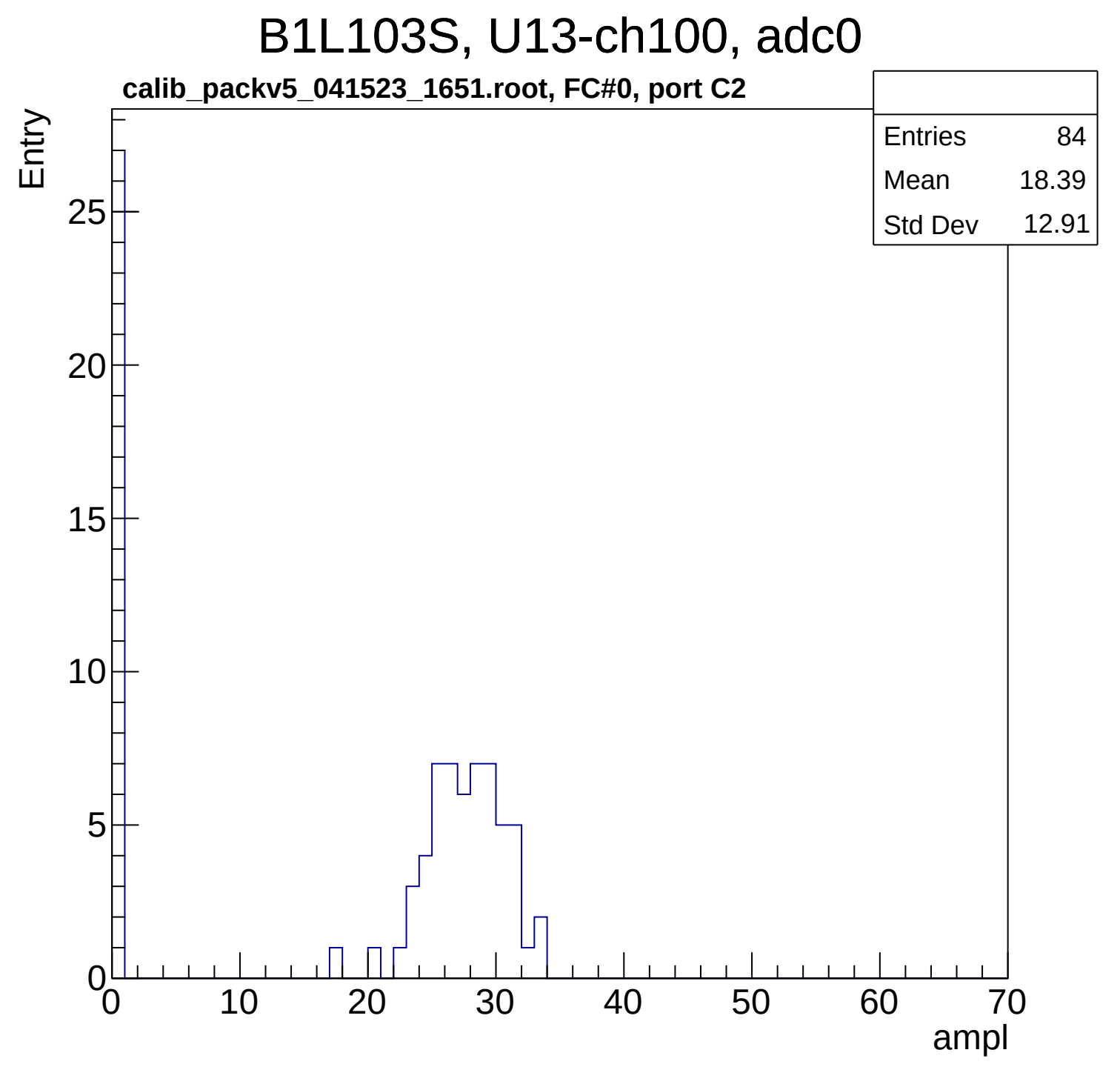
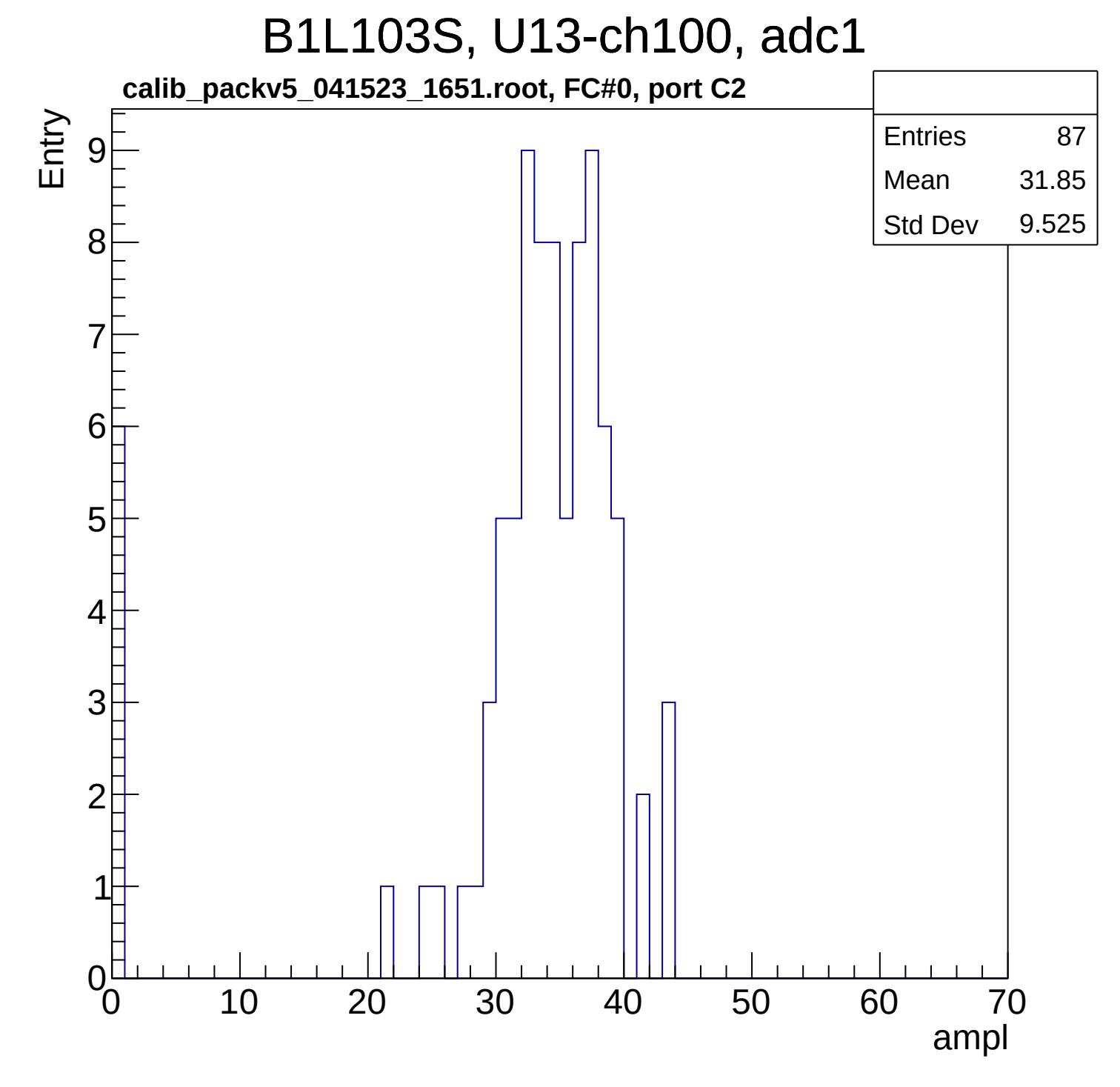
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U13-ch99, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch100, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 18.39
Std Dev 12.91
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch100, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 31.85
Std Dev 9.525
Entry
ampl
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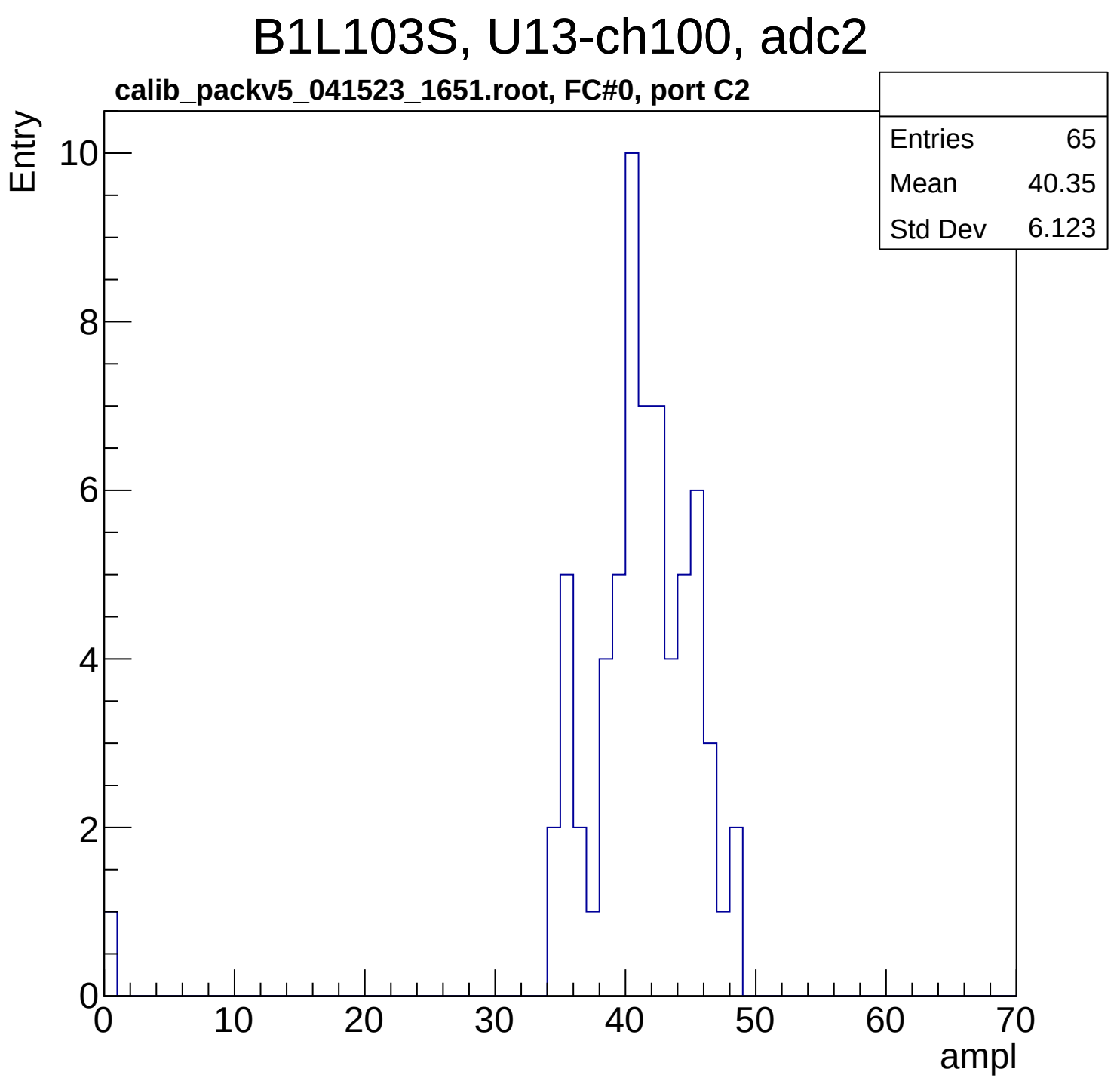
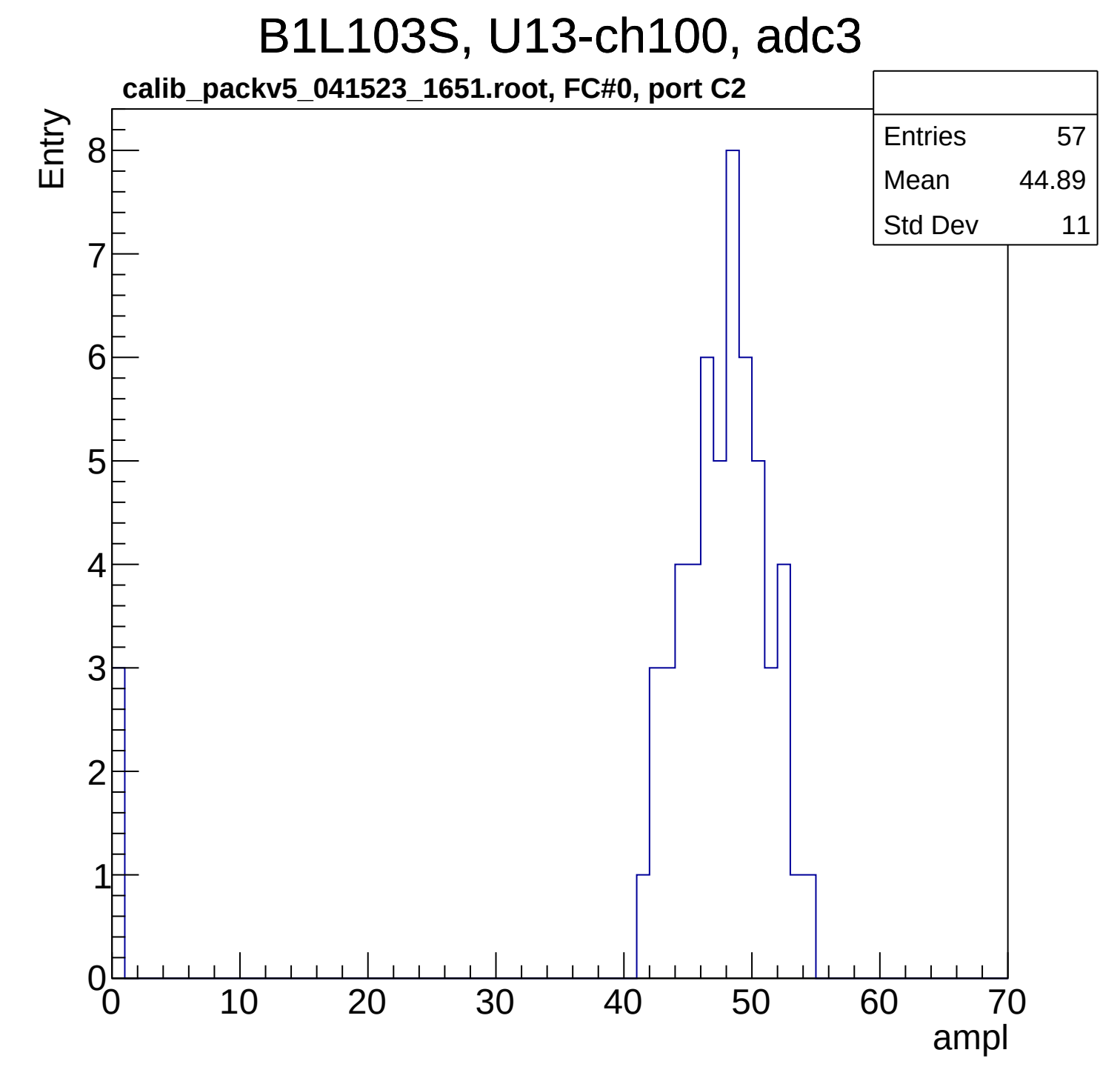
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch100, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 40.35
Std Dev 6.123
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch100, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 44.89
Std Dev 11
Entry
ampl
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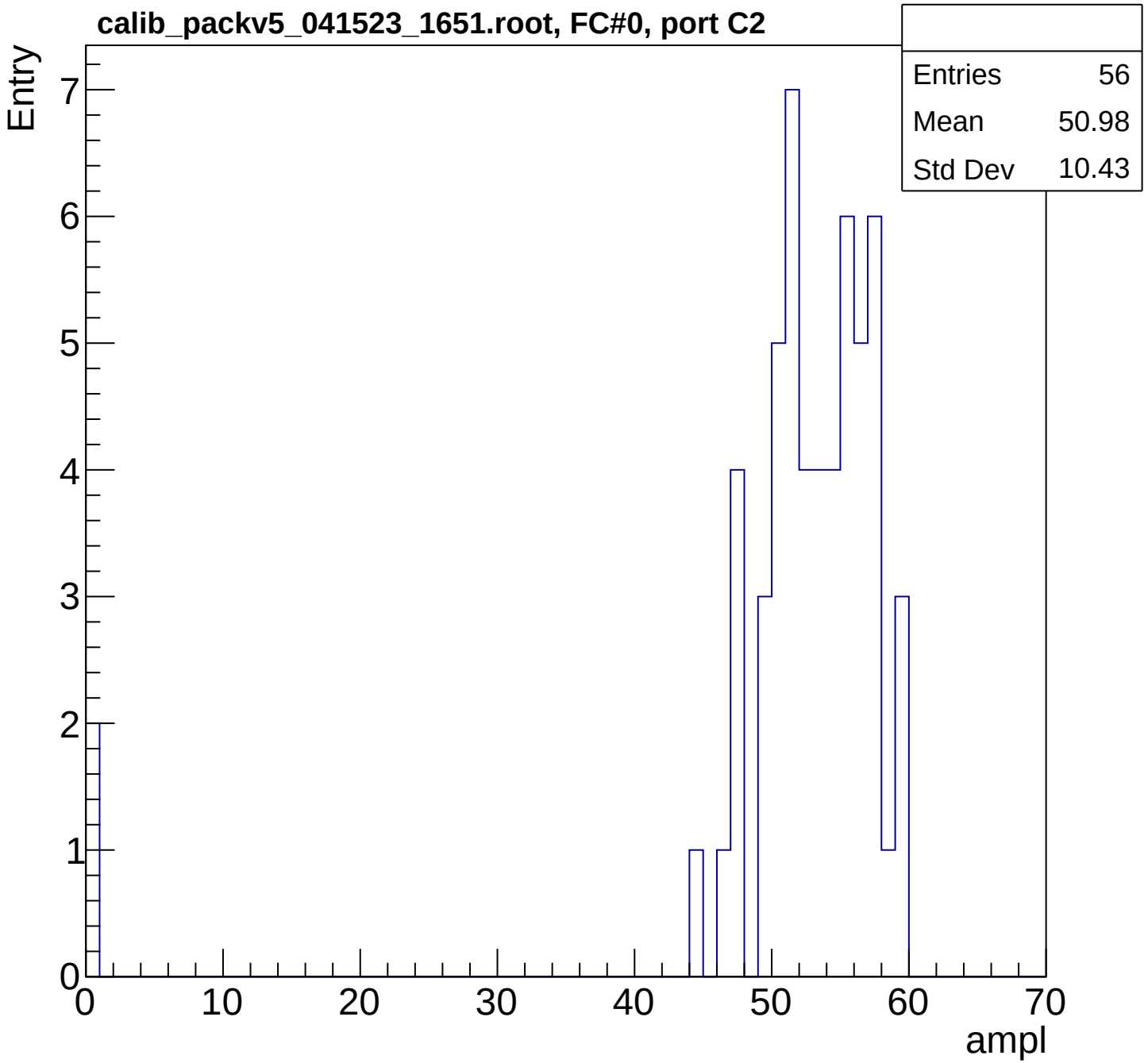
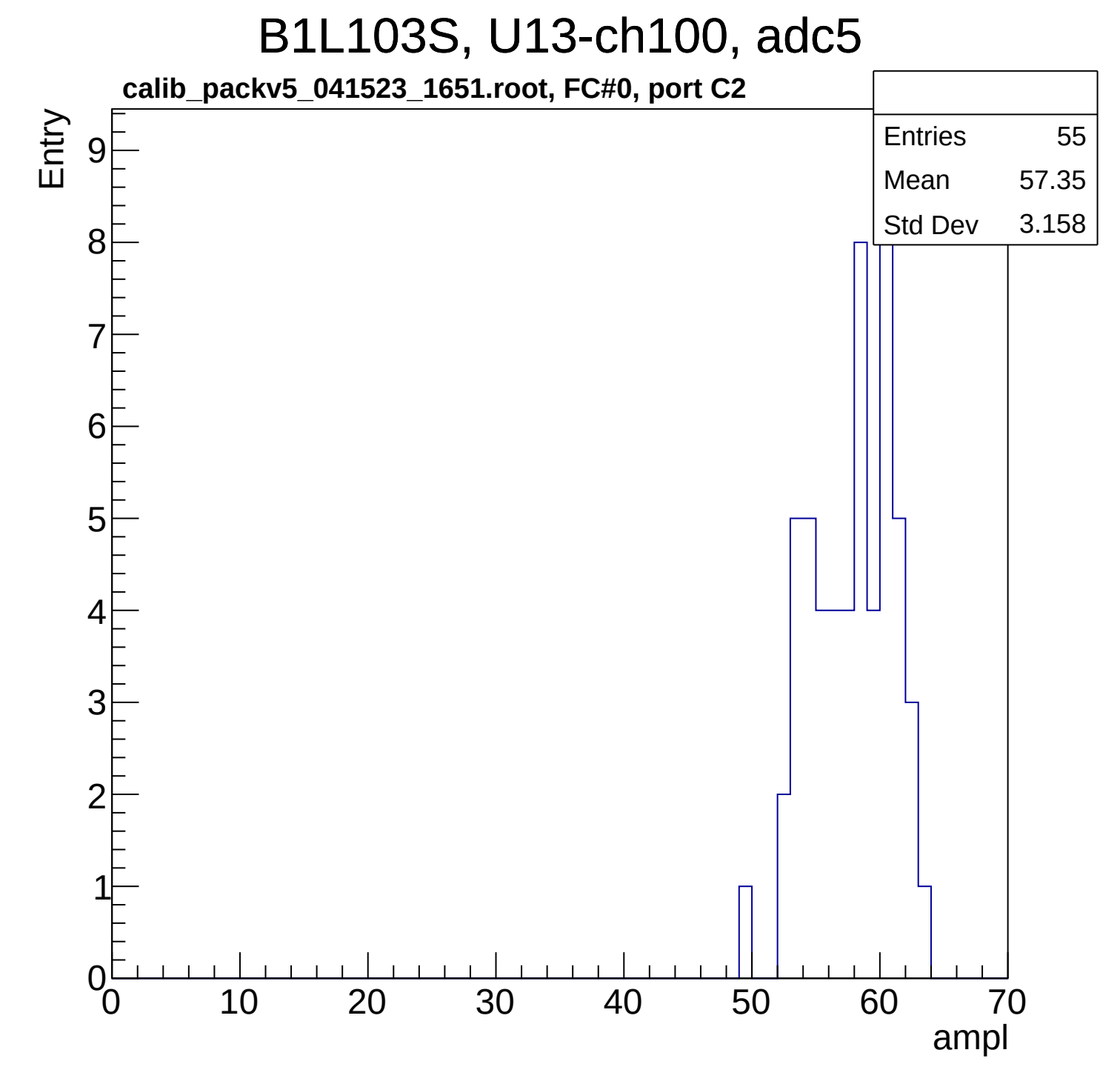
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch100, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 50.98
Std Dev 10.43
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch100, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.35
Std Dev 3.158
Entry
ampl
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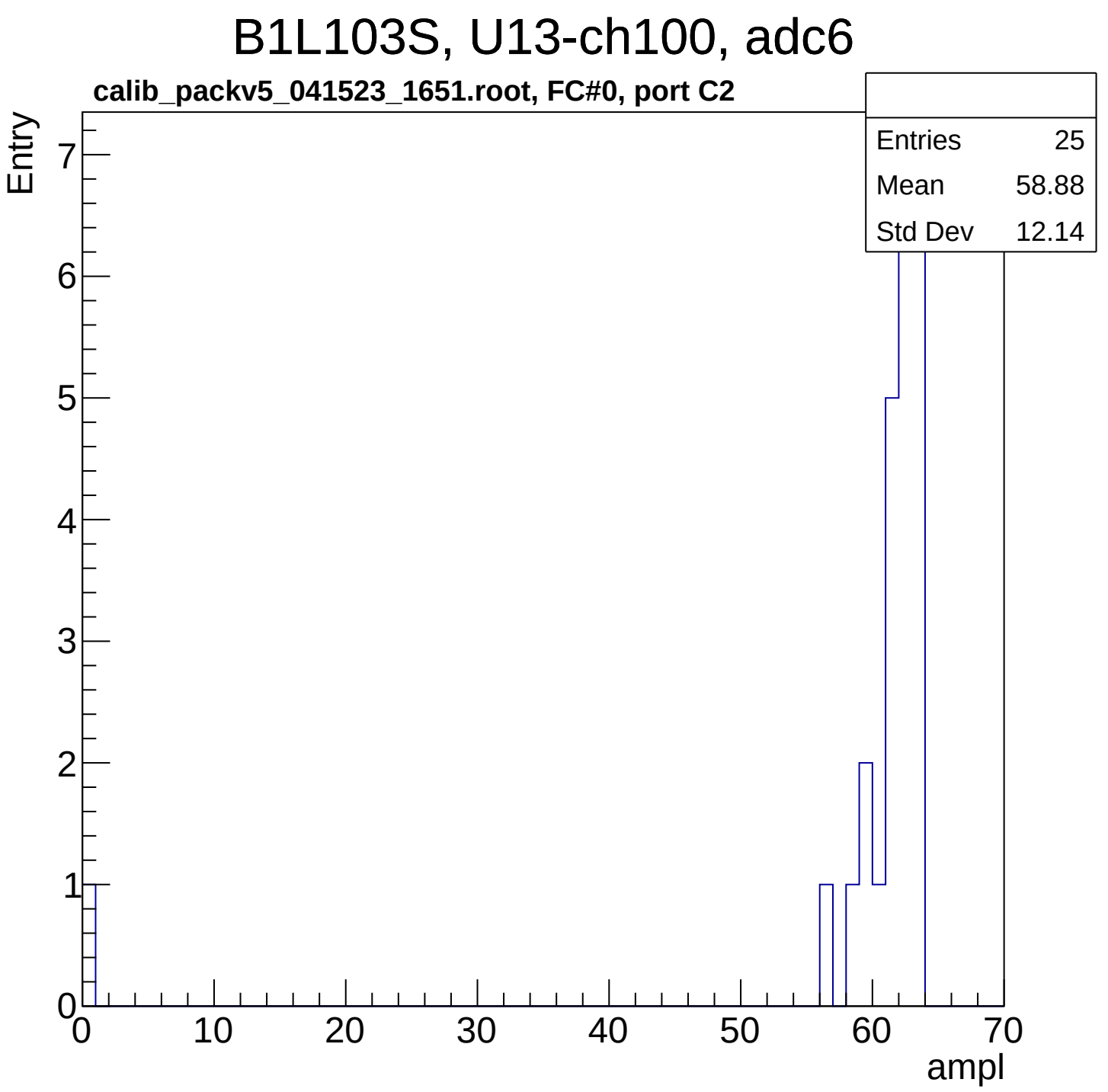
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch100, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 58.88
Std Dev 12.14
Entry
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1
2
3
4
5
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7
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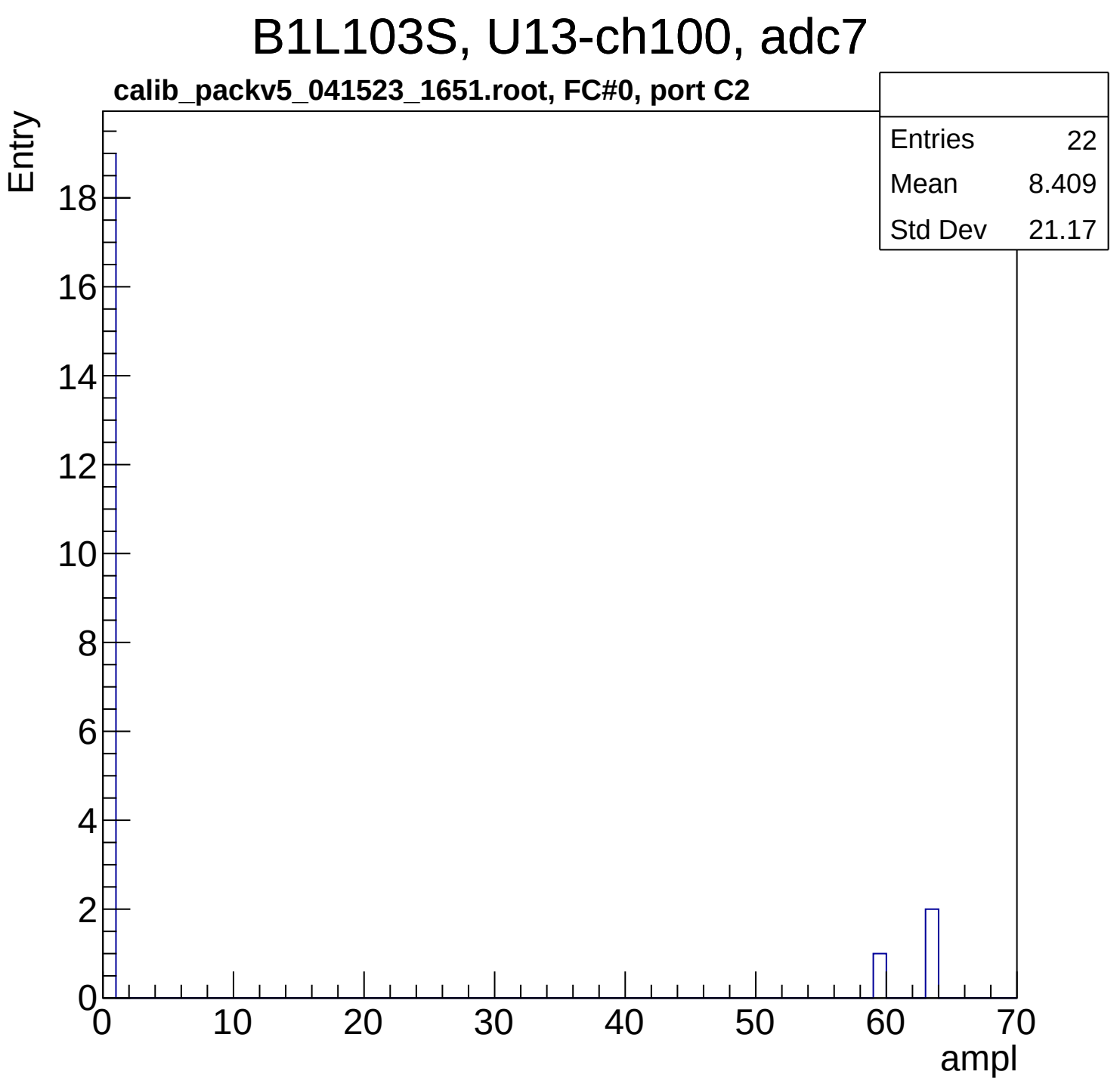
70
ampl


B1L103S, U13-ch100, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.409
Std Dev 21.17
Entry
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6
8
10
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14
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18
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10
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50
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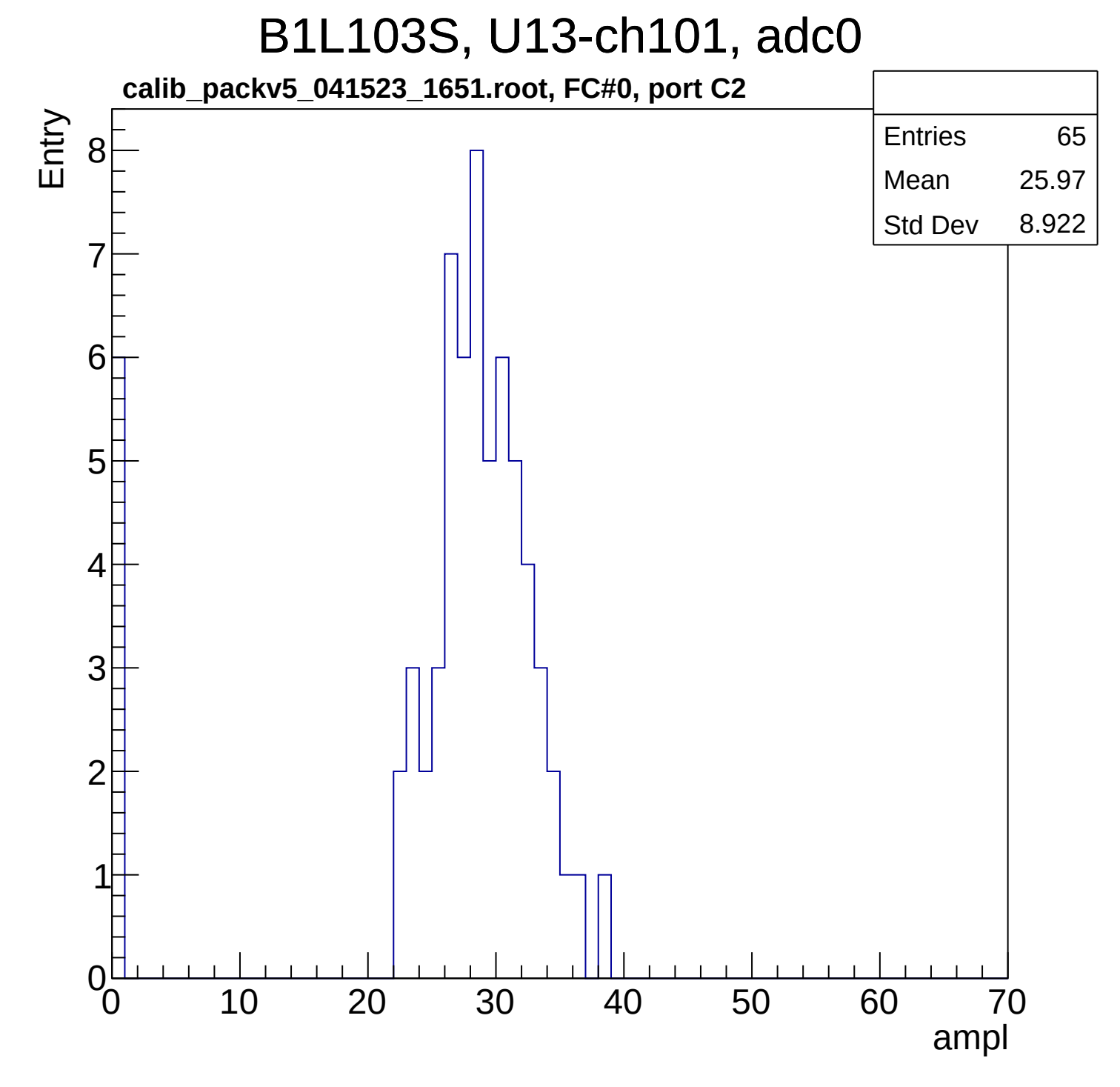
70
ampl


B1L103S, U13-ch101, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 25.97
Std Dev 8.922
Entry
ampl
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0
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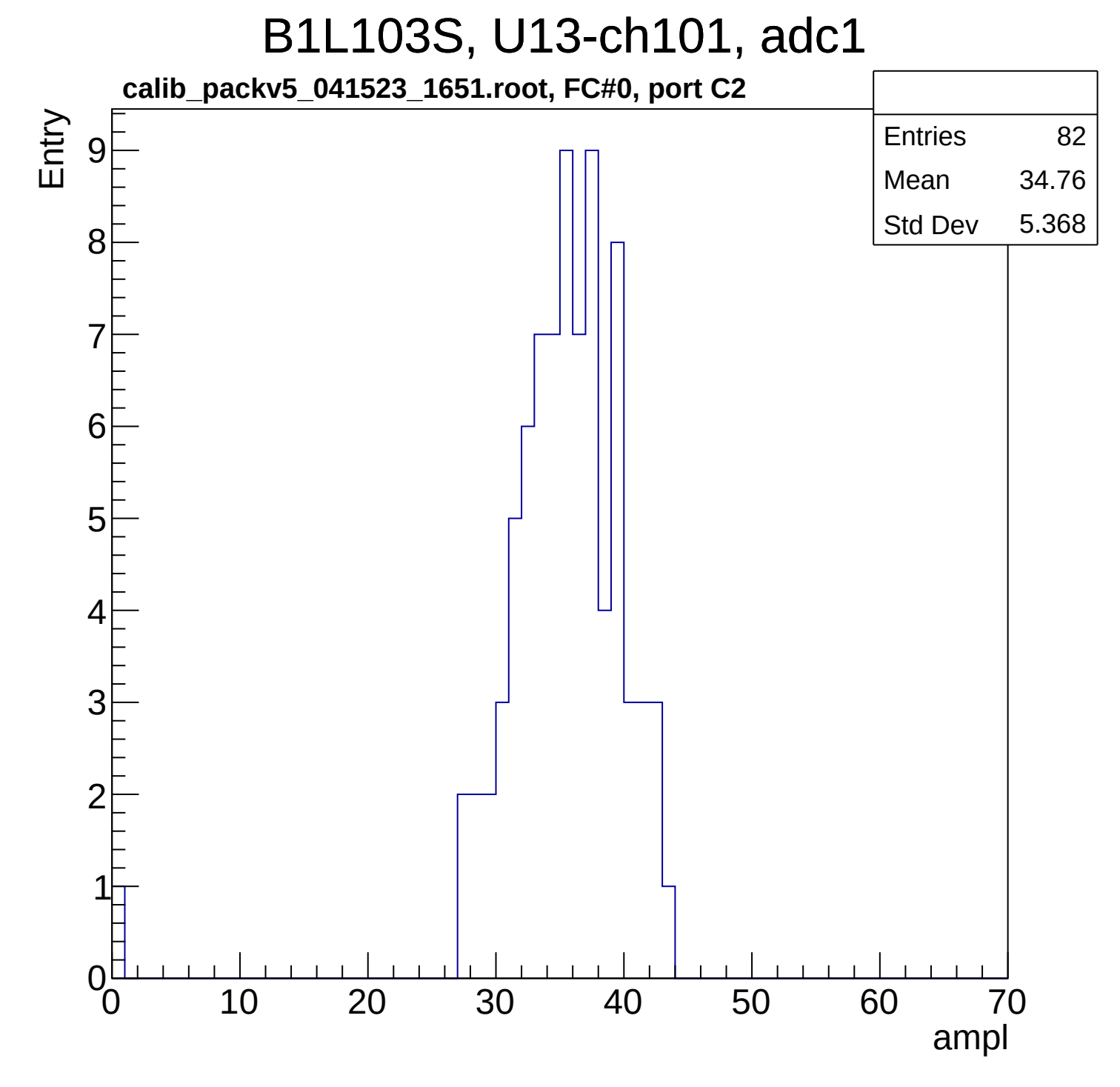
B1L103S, U13-ch101, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 34.76
Std Dev 5.368
Entry
ampl
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0
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60
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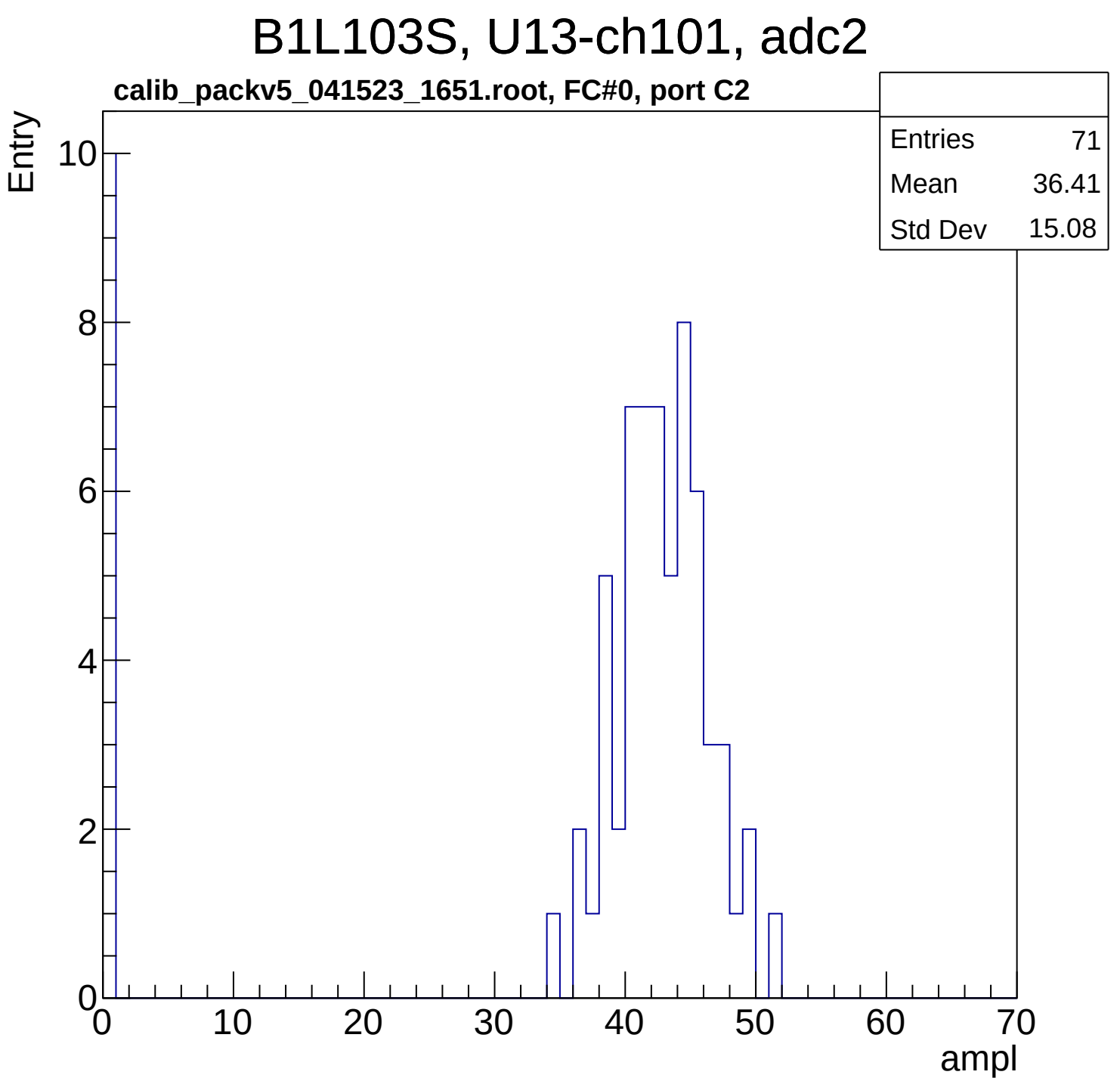
B1L103S, U13-ch101, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 36.41
Std Dev 15.08
Entry
0
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10
0
10
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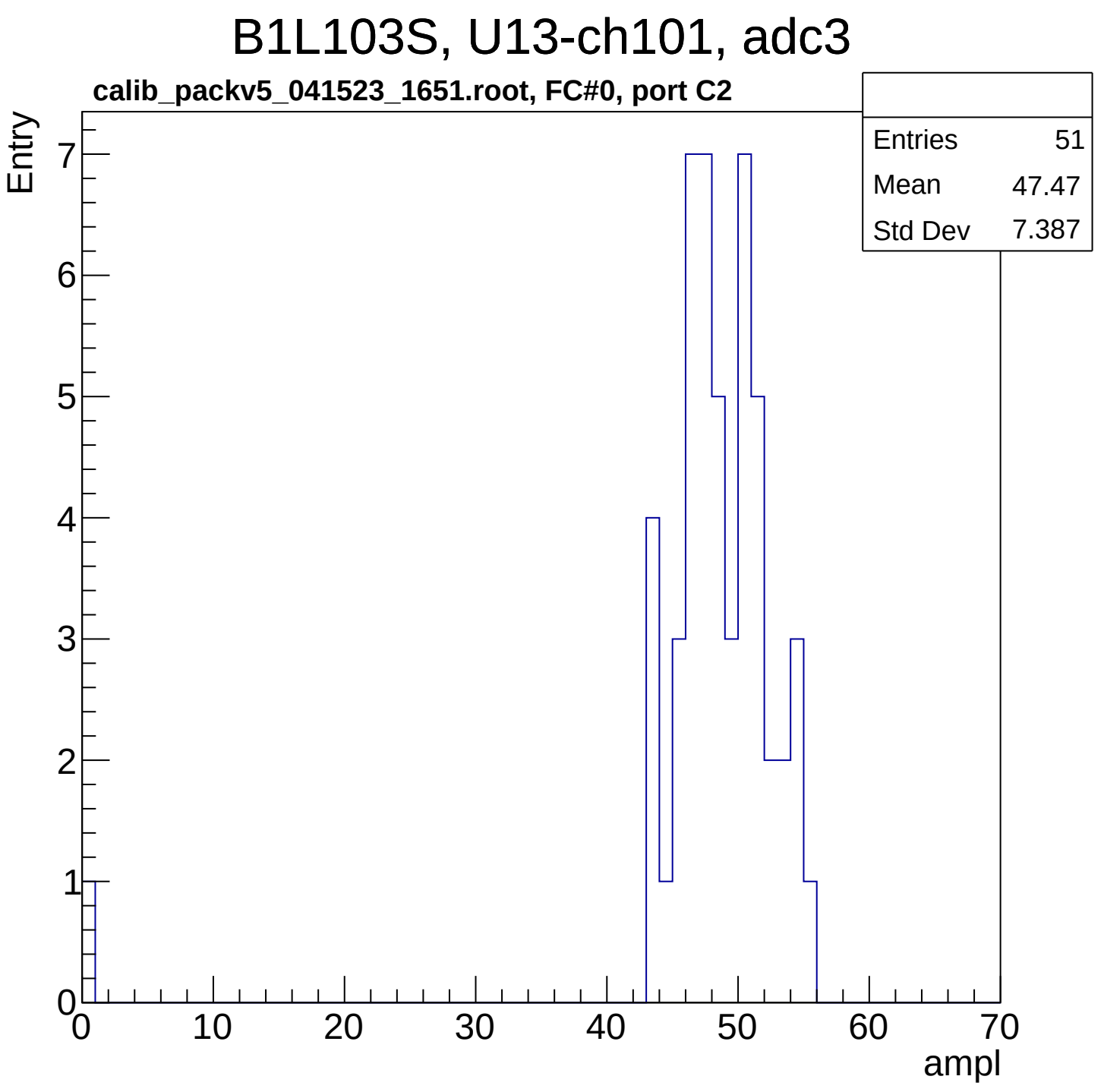
50
60
70
ampl


B1L103S, U13-ch101, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 47.47
Std Dev 7.387
Entry
ampl
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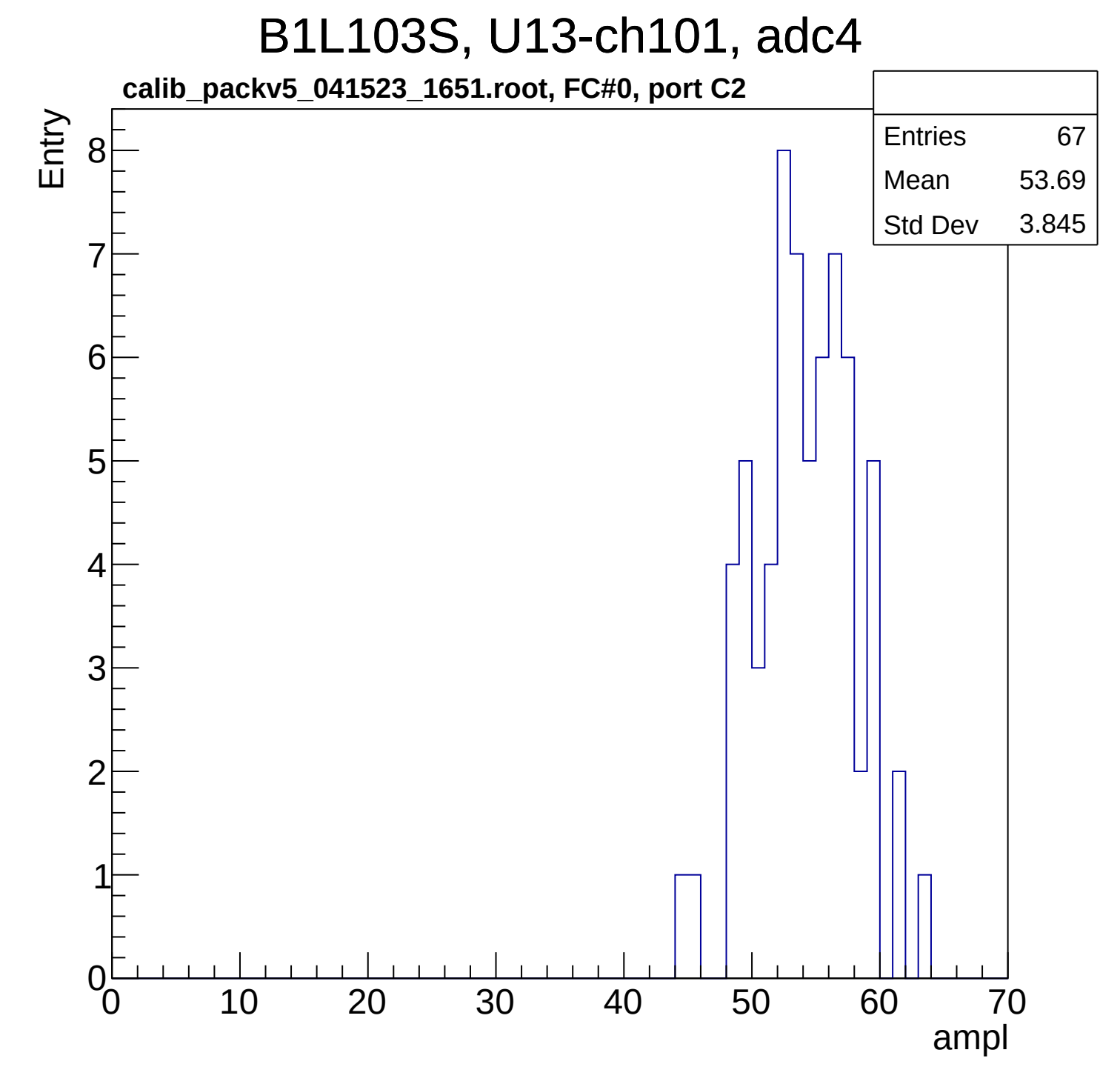
B1L103S, U13-ch101, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 53.69
Std Dev 3.845
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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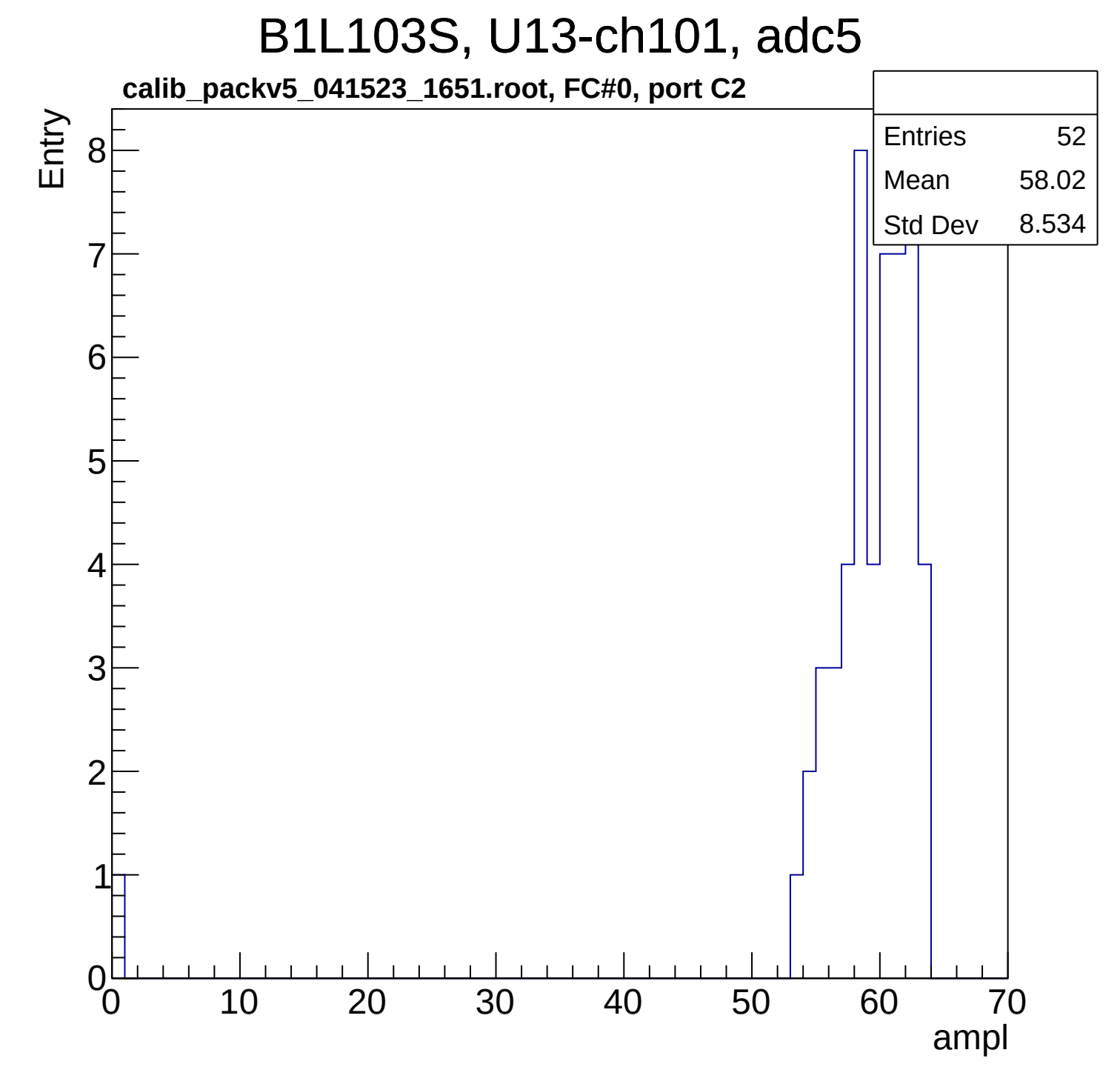
B1L103S, U13-ch101, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.02
Std Dev 8.534
Entry
ampl
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2
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8
0
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60
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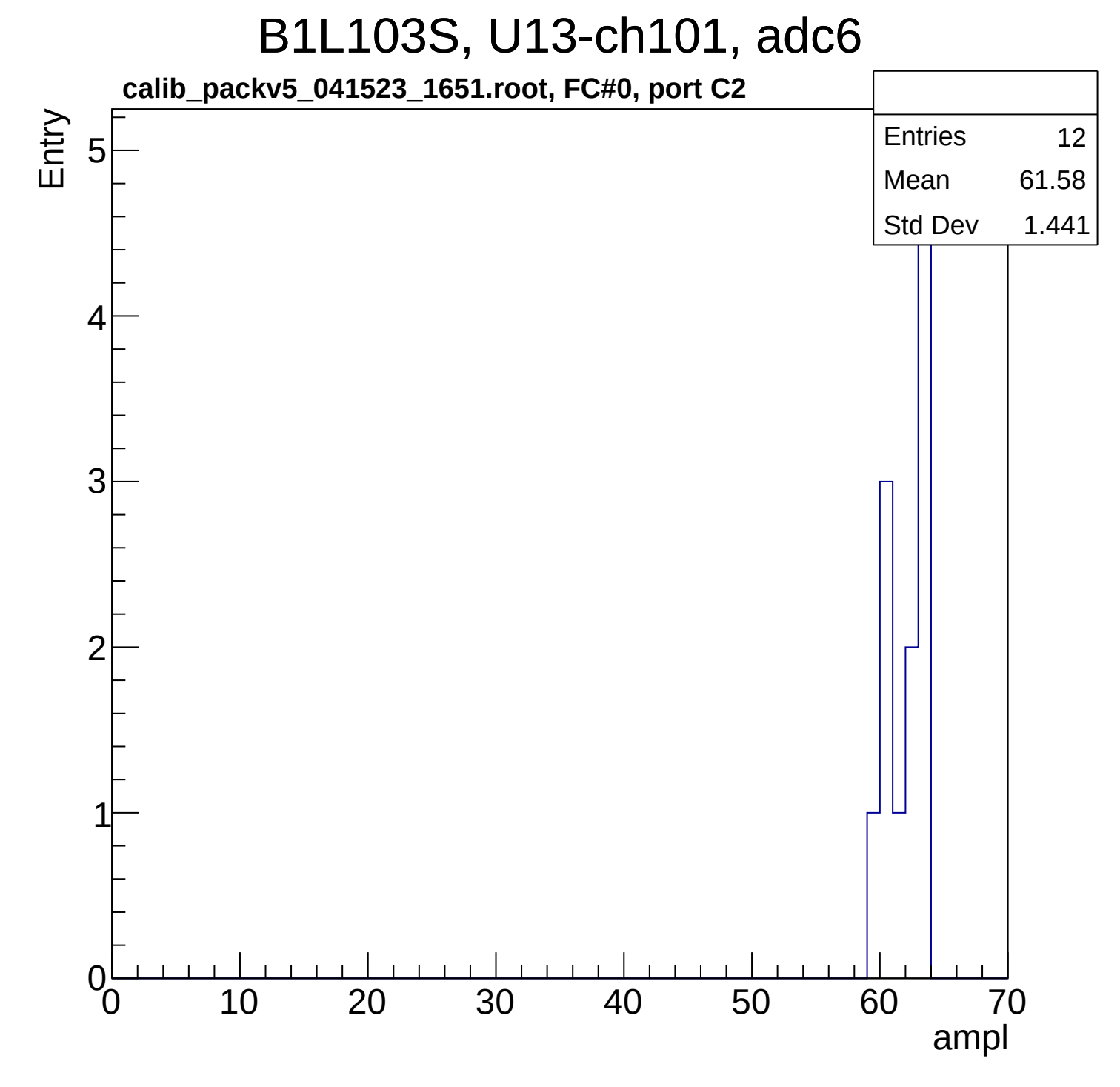
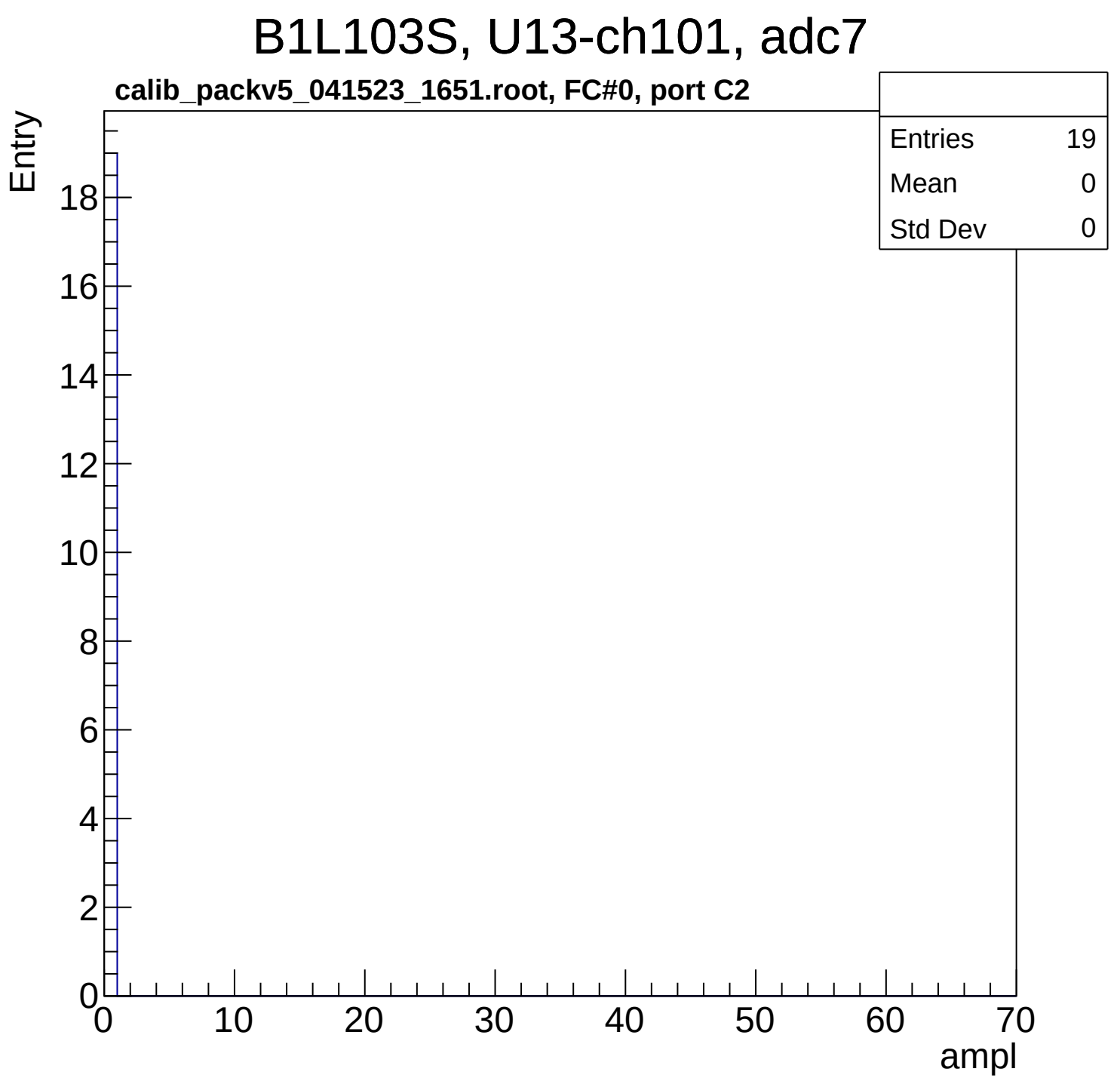
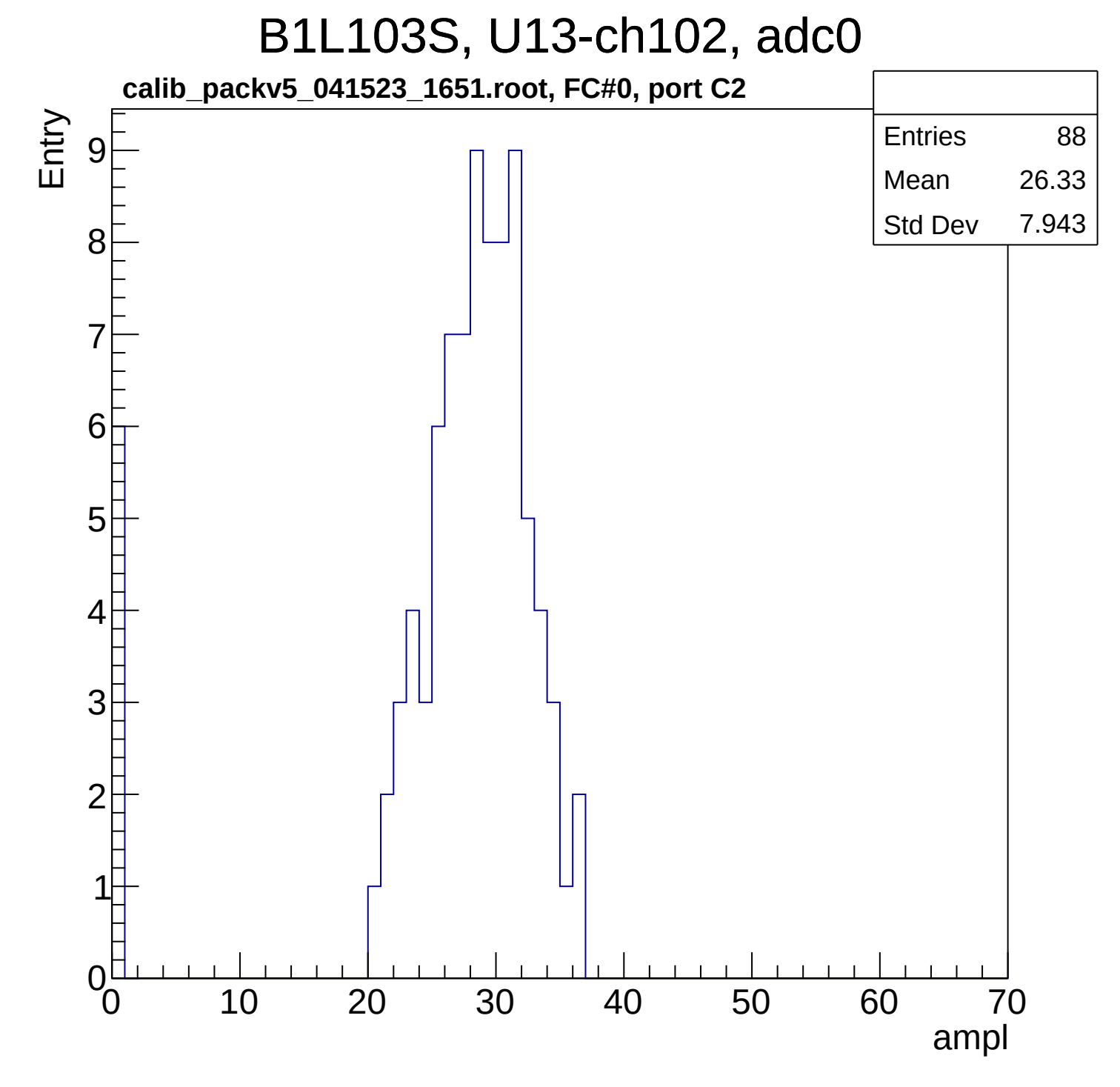
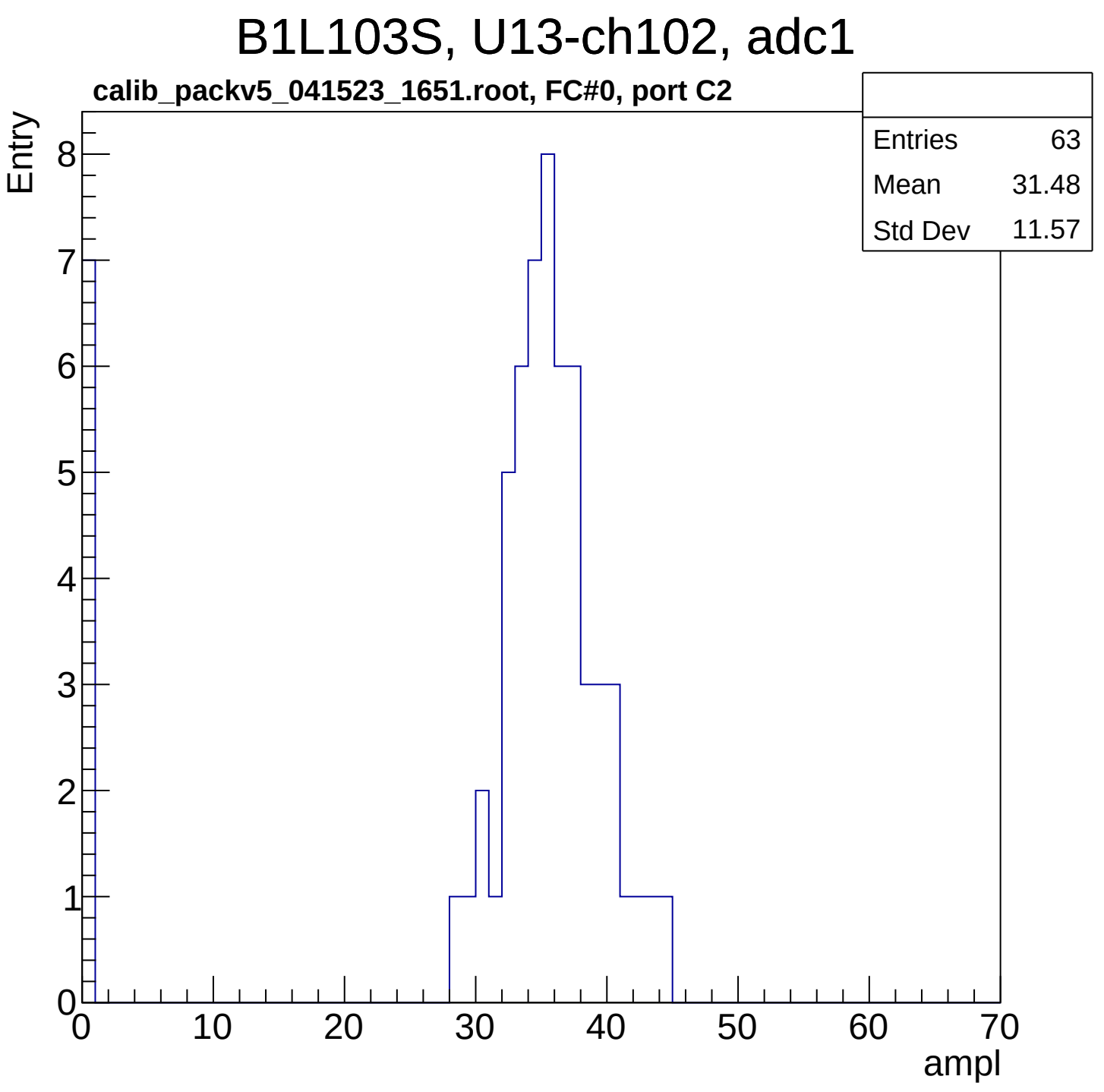

B1L103S, U13-ch101, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.58
Std Dev 1.441
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U13-ch101, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch102, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 26.33
Std Dev 7.943
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch102, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 31.48
Std Dev 11.57
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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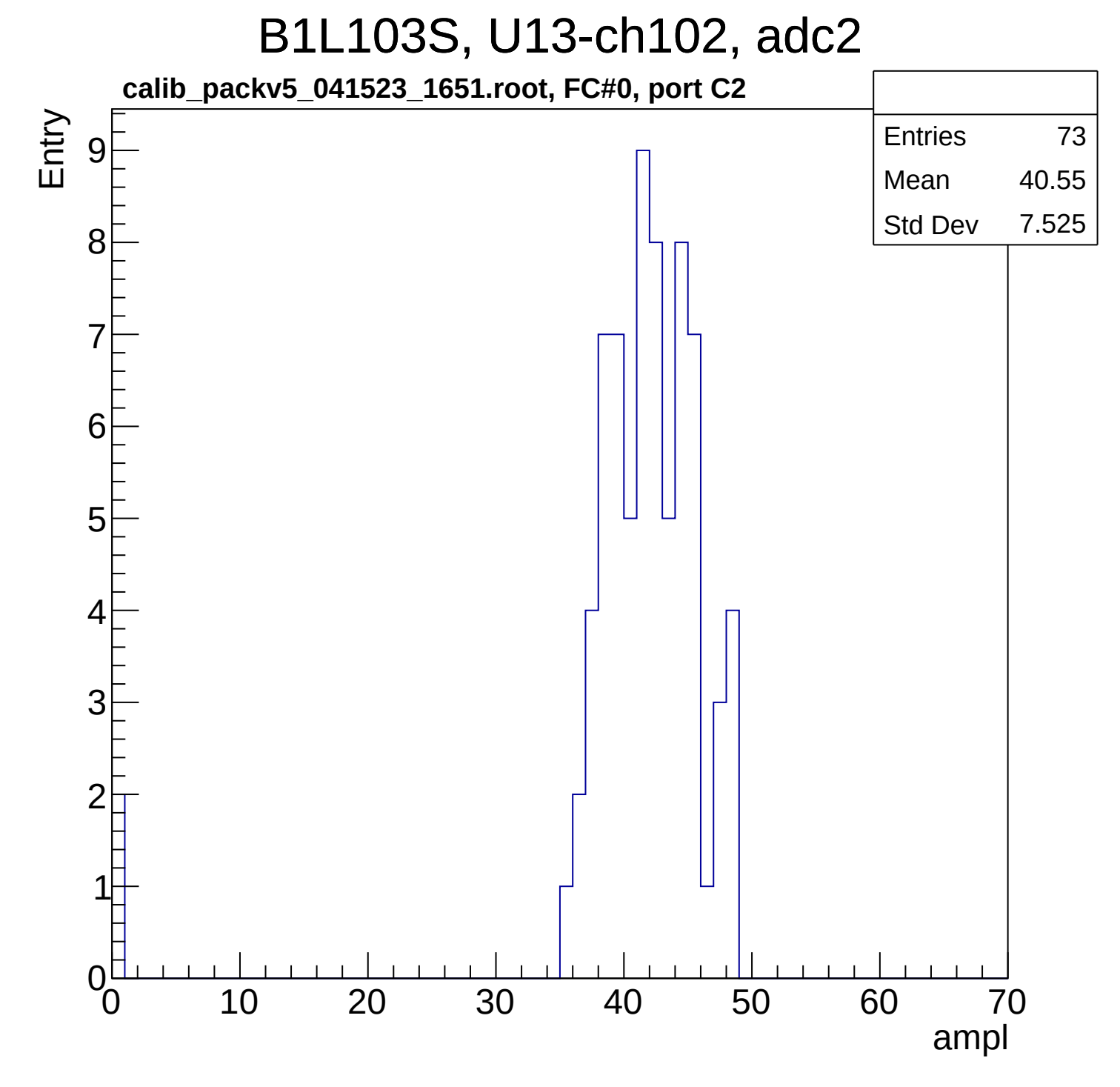
B1L103S, U13-ch102, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 40.55
Std Dev 7.525
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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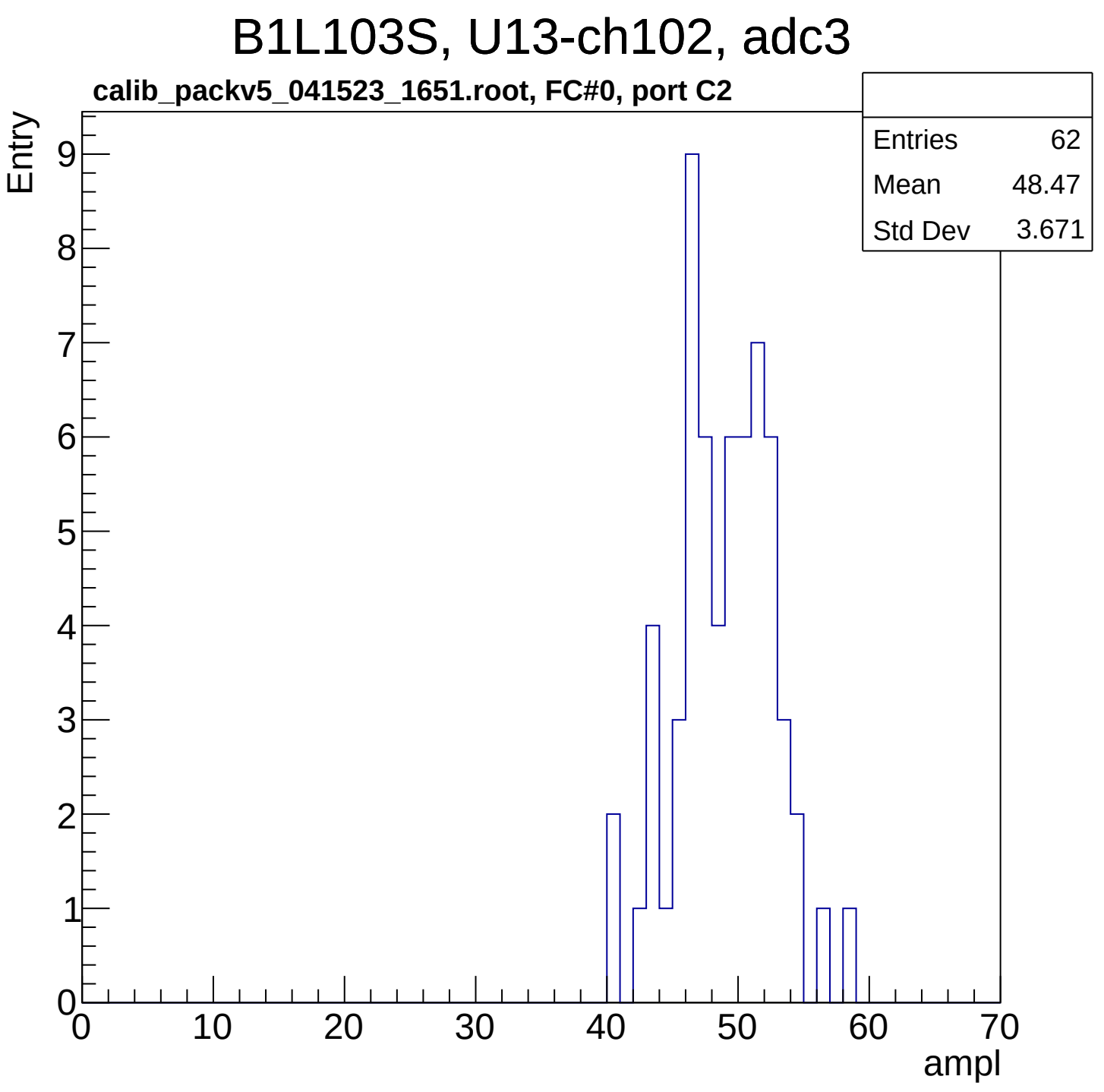
40
50
60
70


B1L103S, U13-ch102, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 48.47
Std Dev 3.671
Entry
ampl
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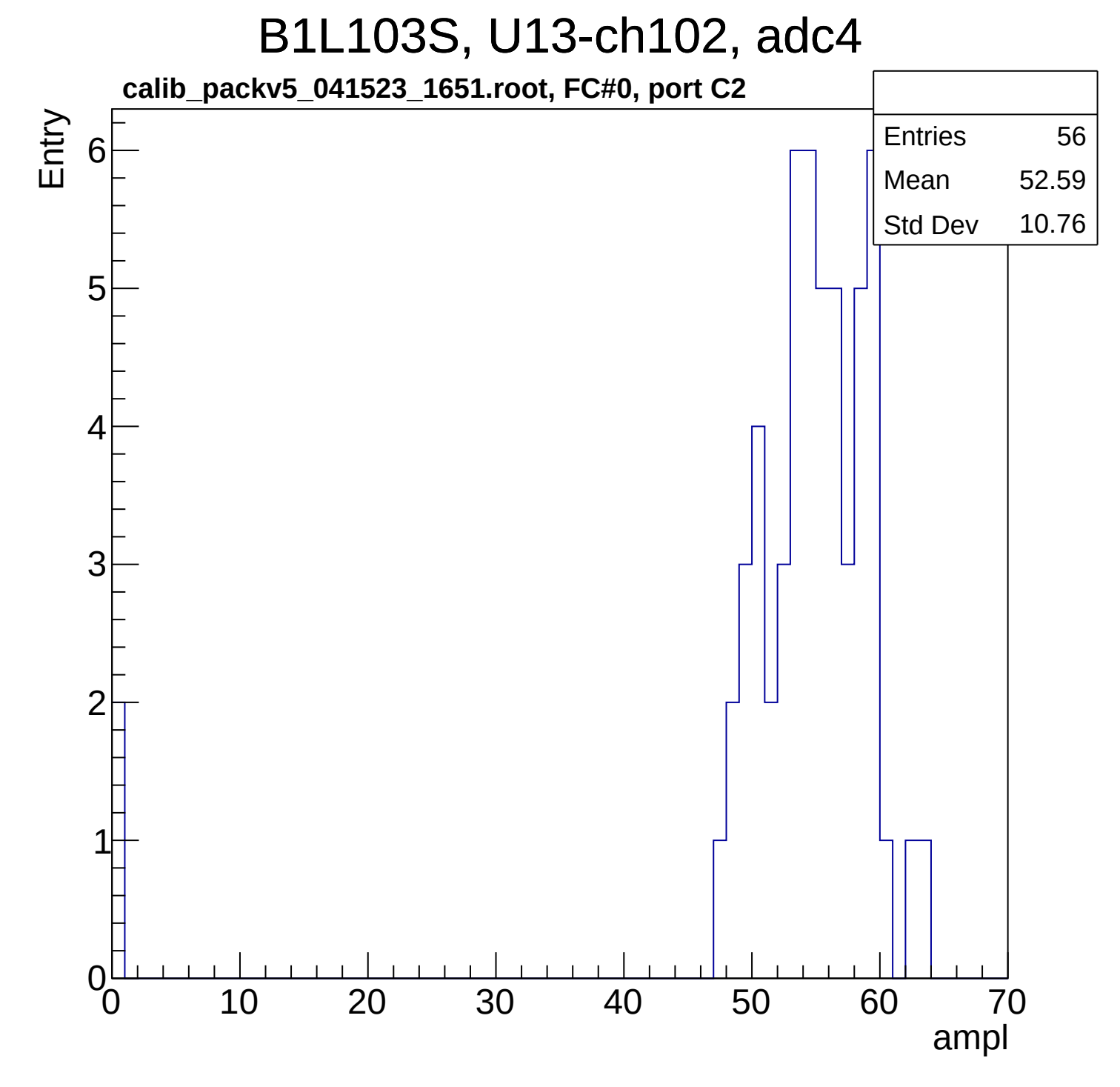
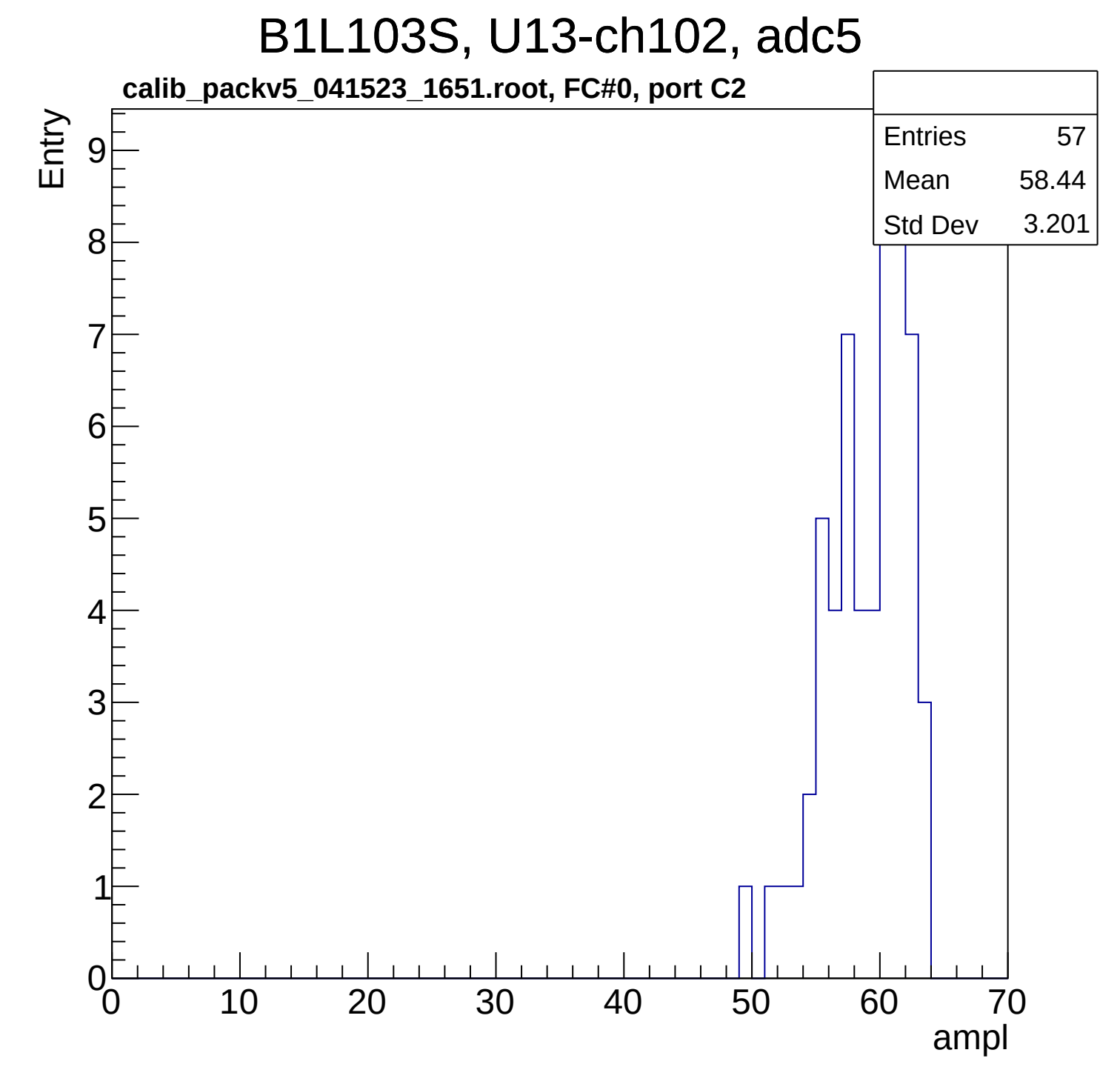
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch102, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 52.59
Std Dev 10.76
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch102, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.44
Std Dev 3.201
Entry
ampl
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2
3
4
5
6
7
8
9
0
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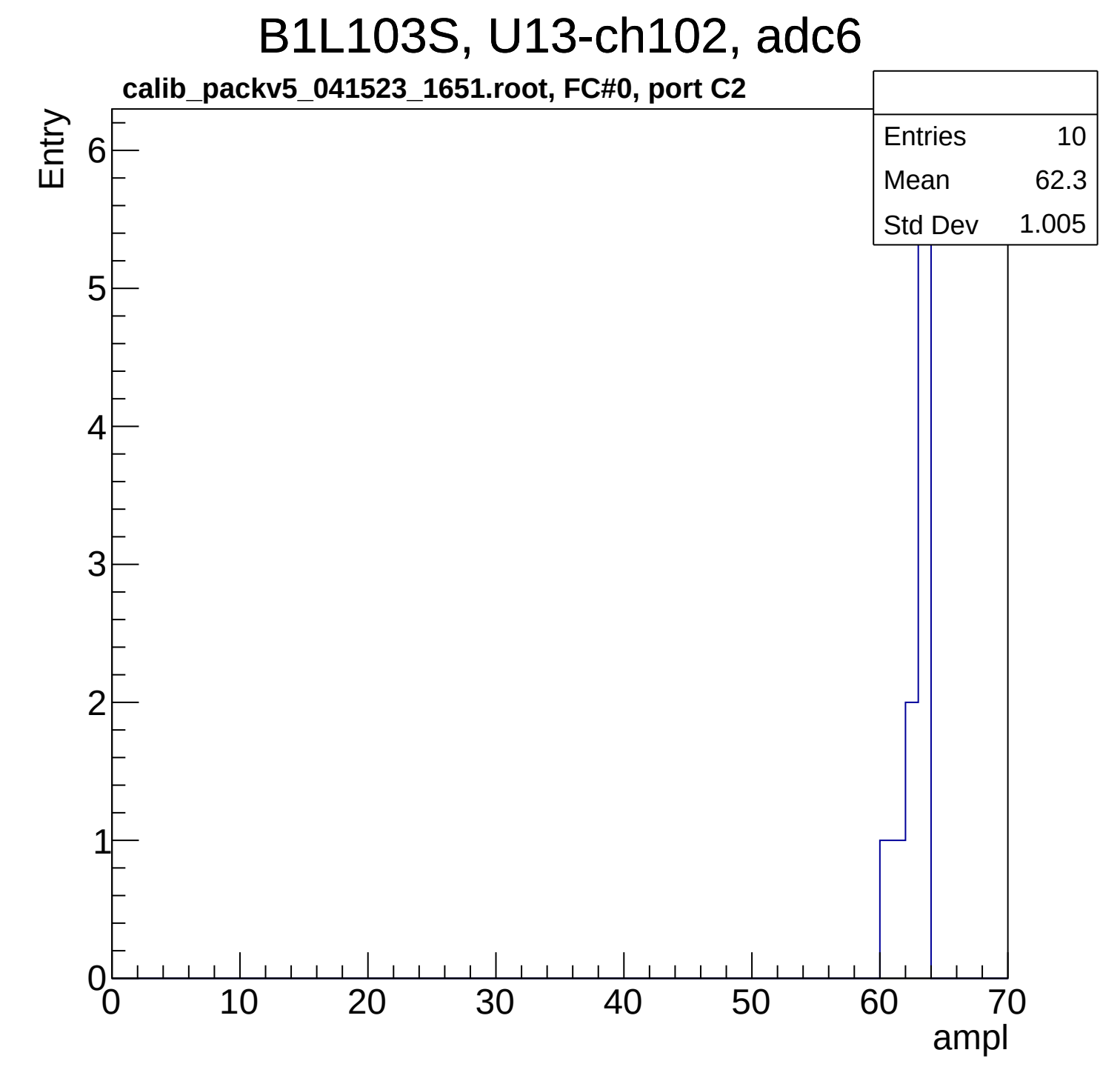
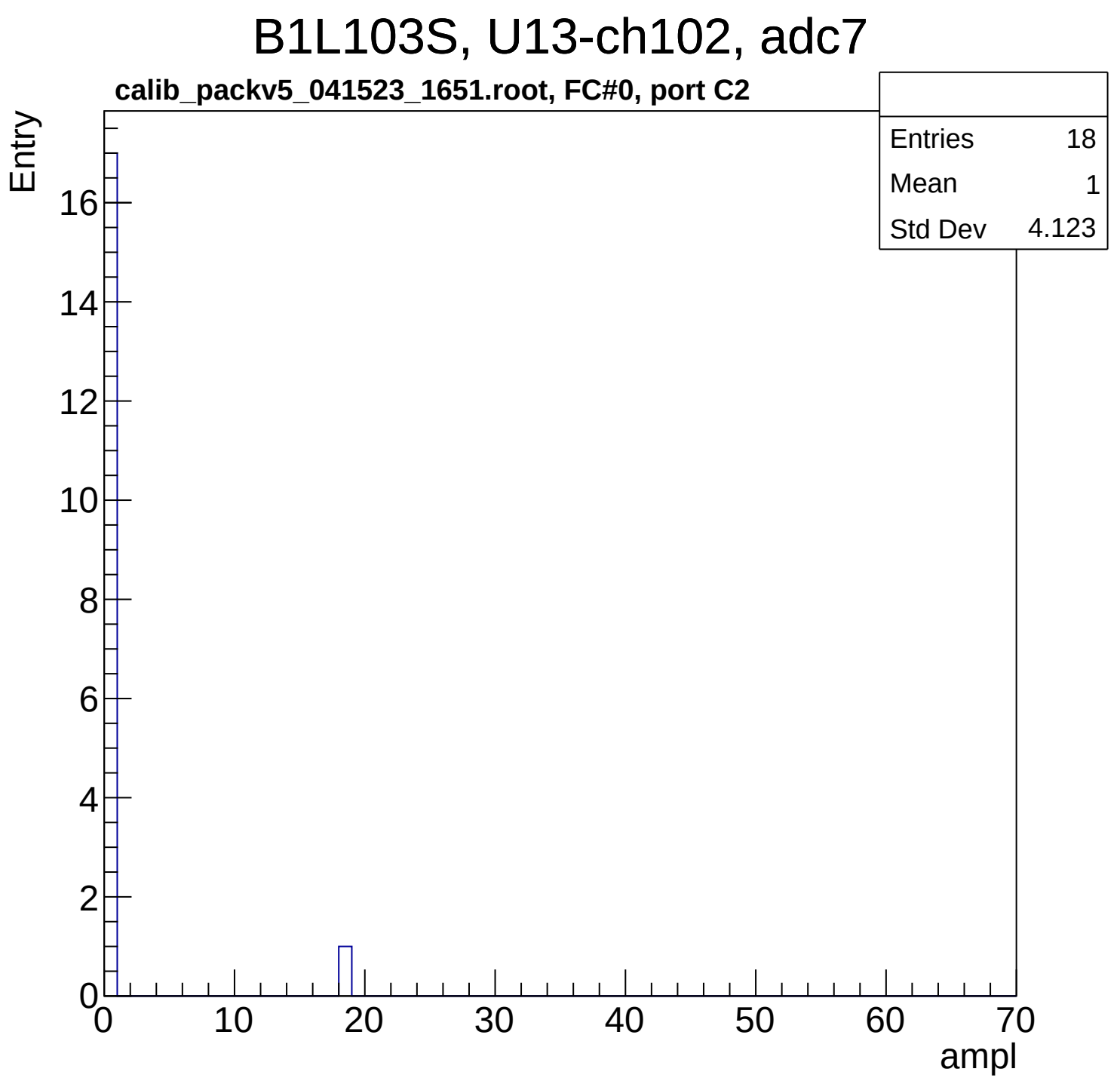
20
30
40
50
60
70


B1L103S, U13-ch102, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 62.3
Std Dev 1.005
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch102, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1
Std Dev 4.123
Entry
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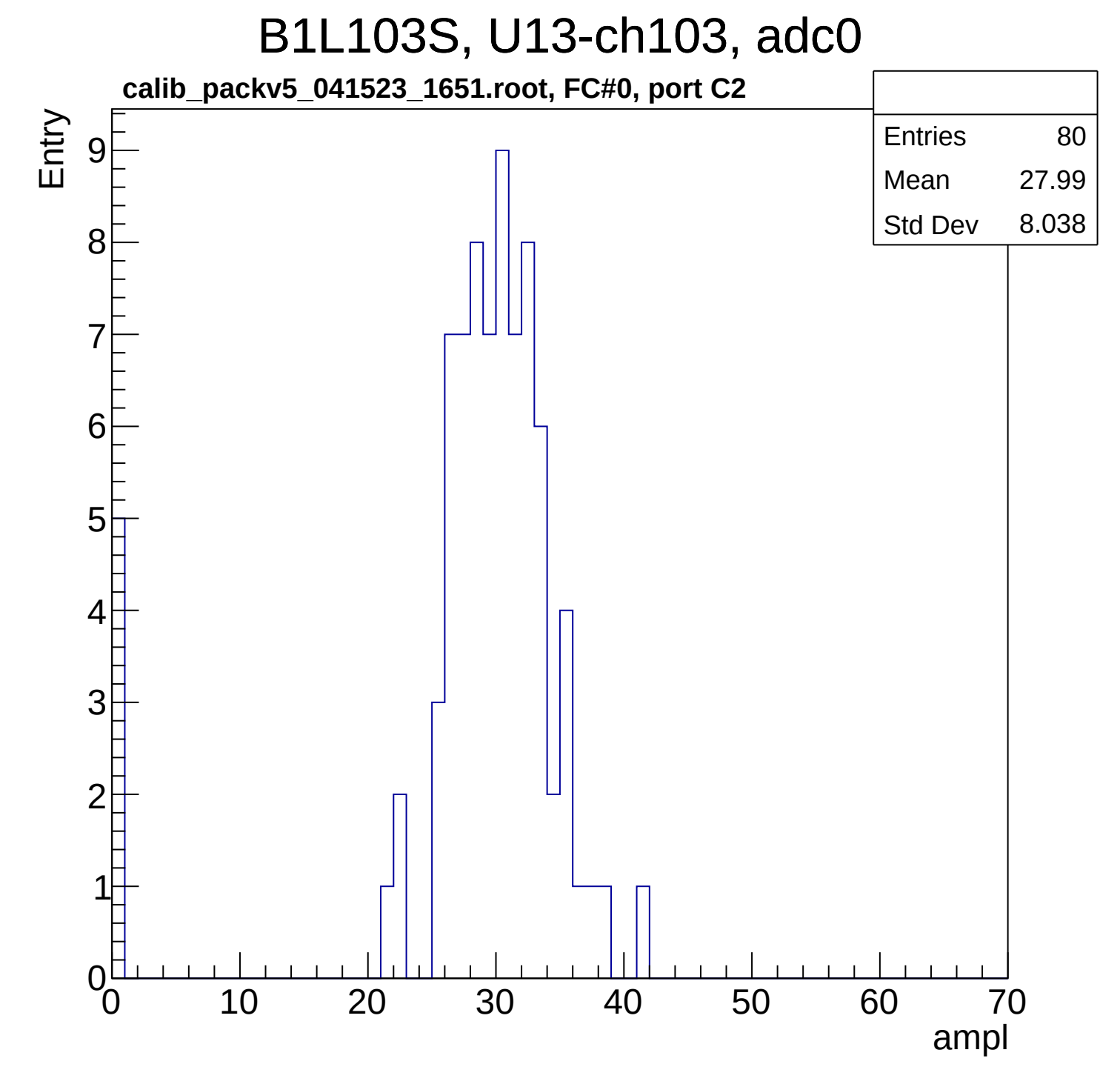
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch103, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 27.99
Std Dev 8.038
Entry
ampl
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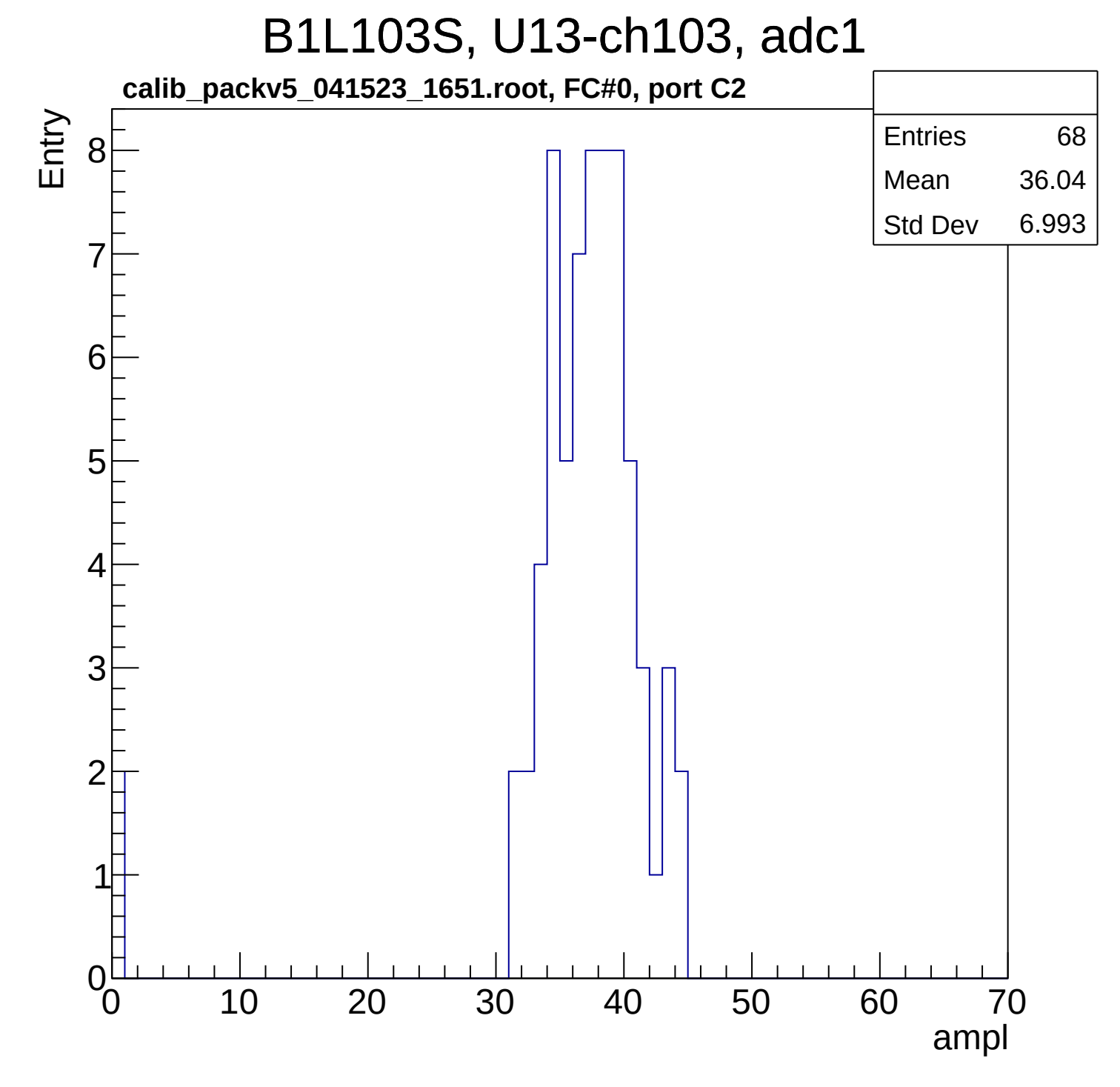
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch103, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 36.04
Std Dev 6.993
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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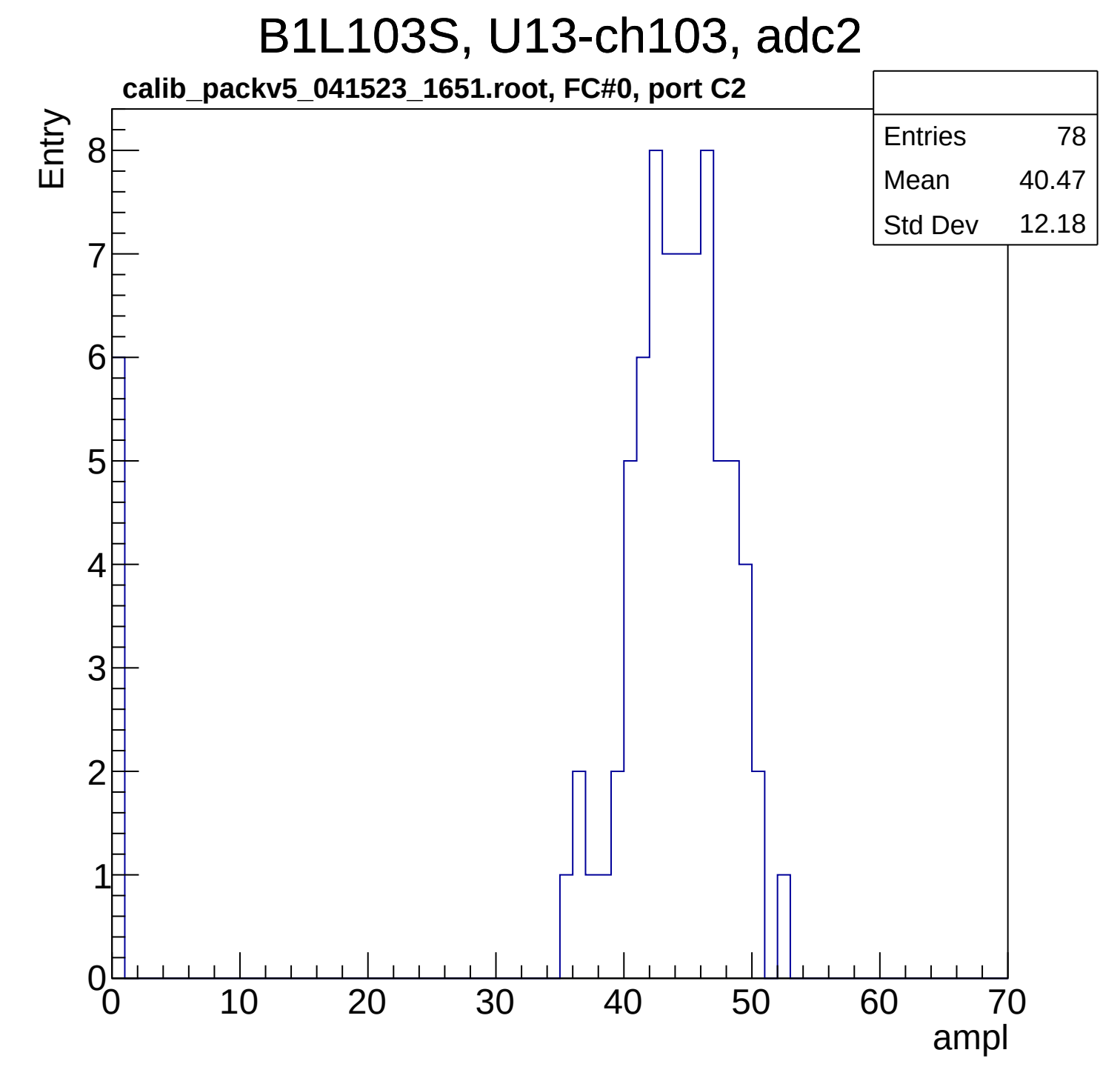
B1L103S, U13-ch103, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 40.47
Std Dev 12.18
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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60
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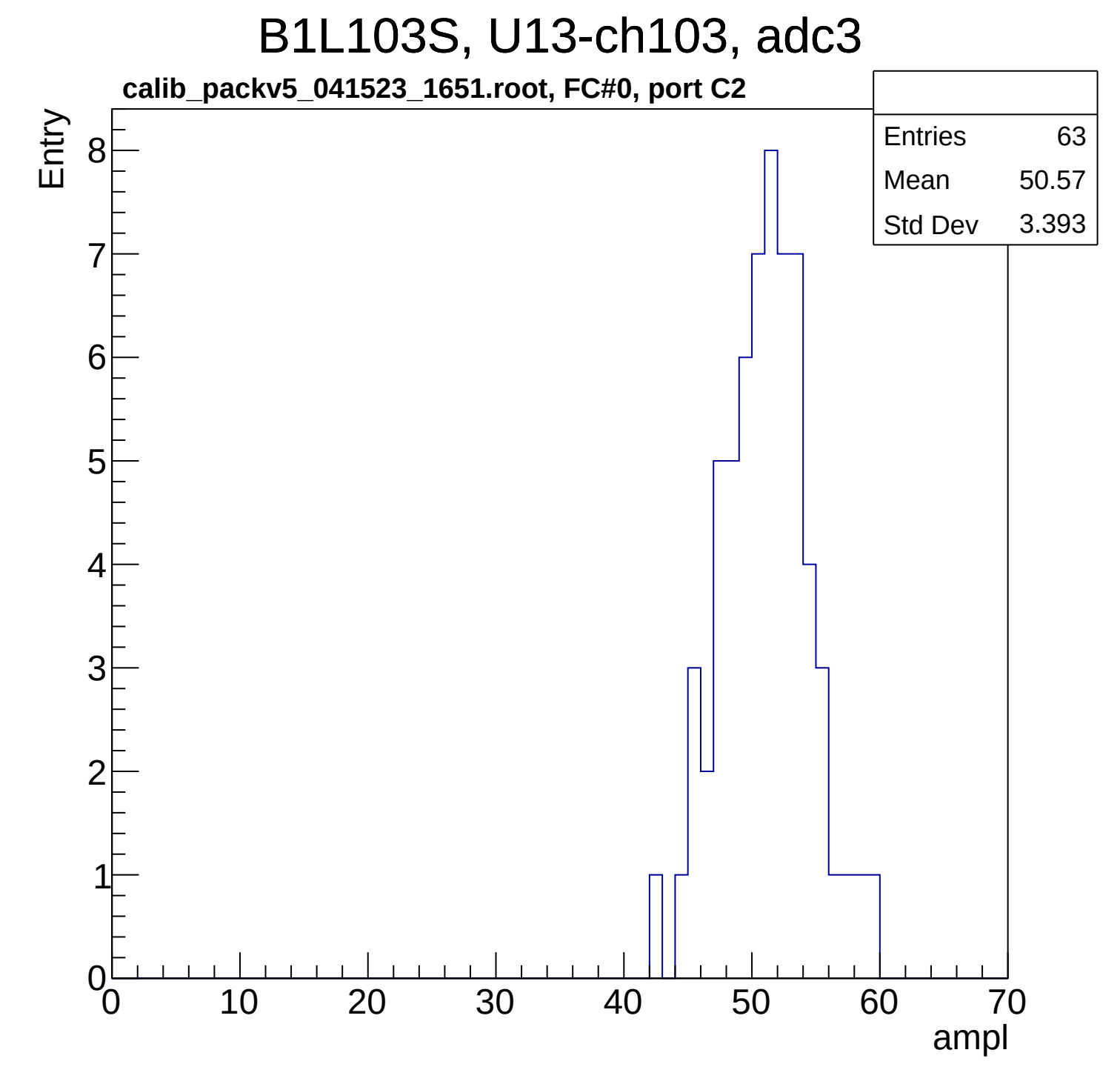
B1L103S, U13-ch103, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 50.57
Std Dev 3.393
Entry
ampl
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1
2
3
4
5
6
7
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0
10
20
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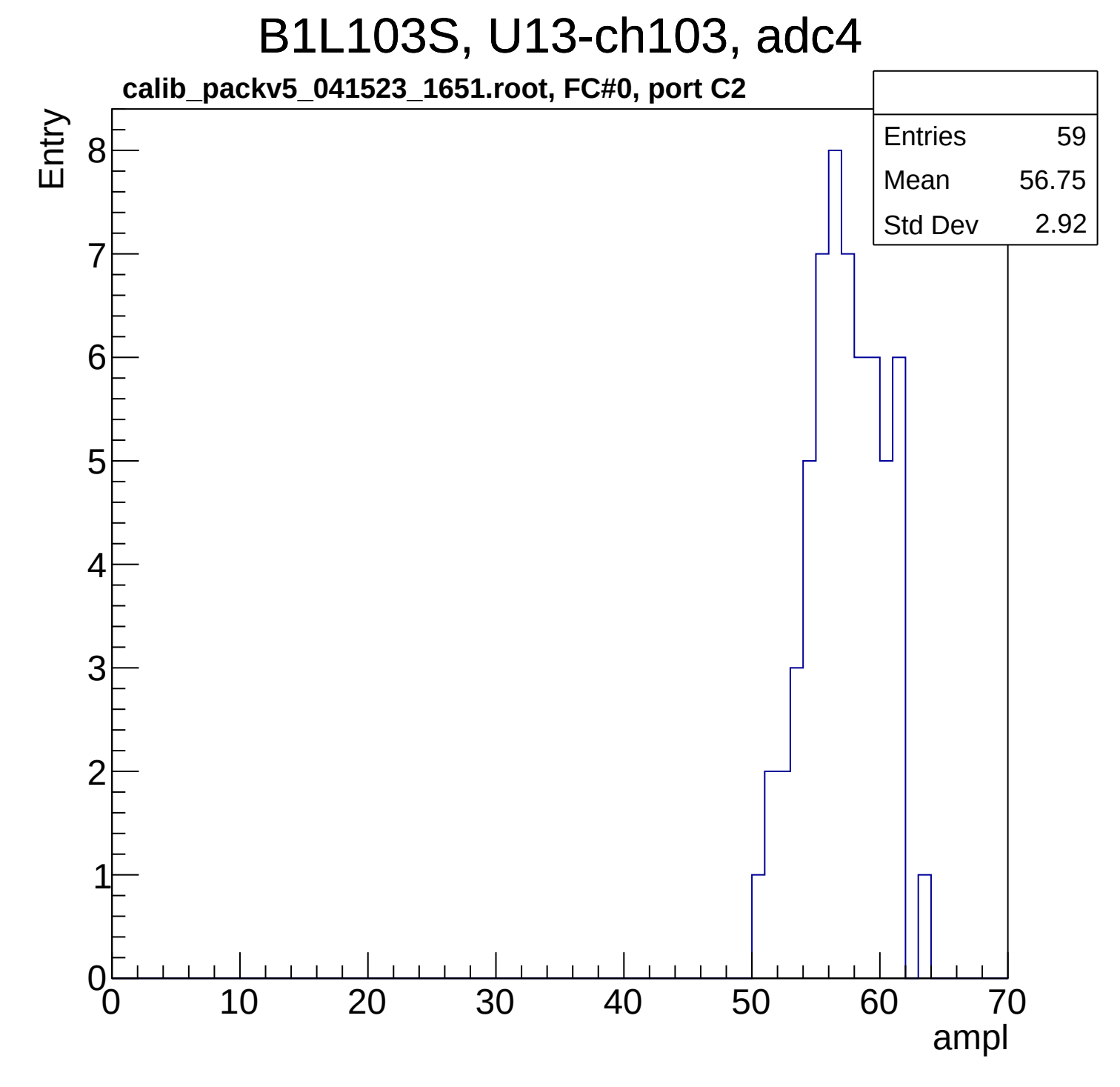
40
50
60
70


B1L103S, U13-ch103, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 56.75
Std Dev 2.92
Entry
ampl
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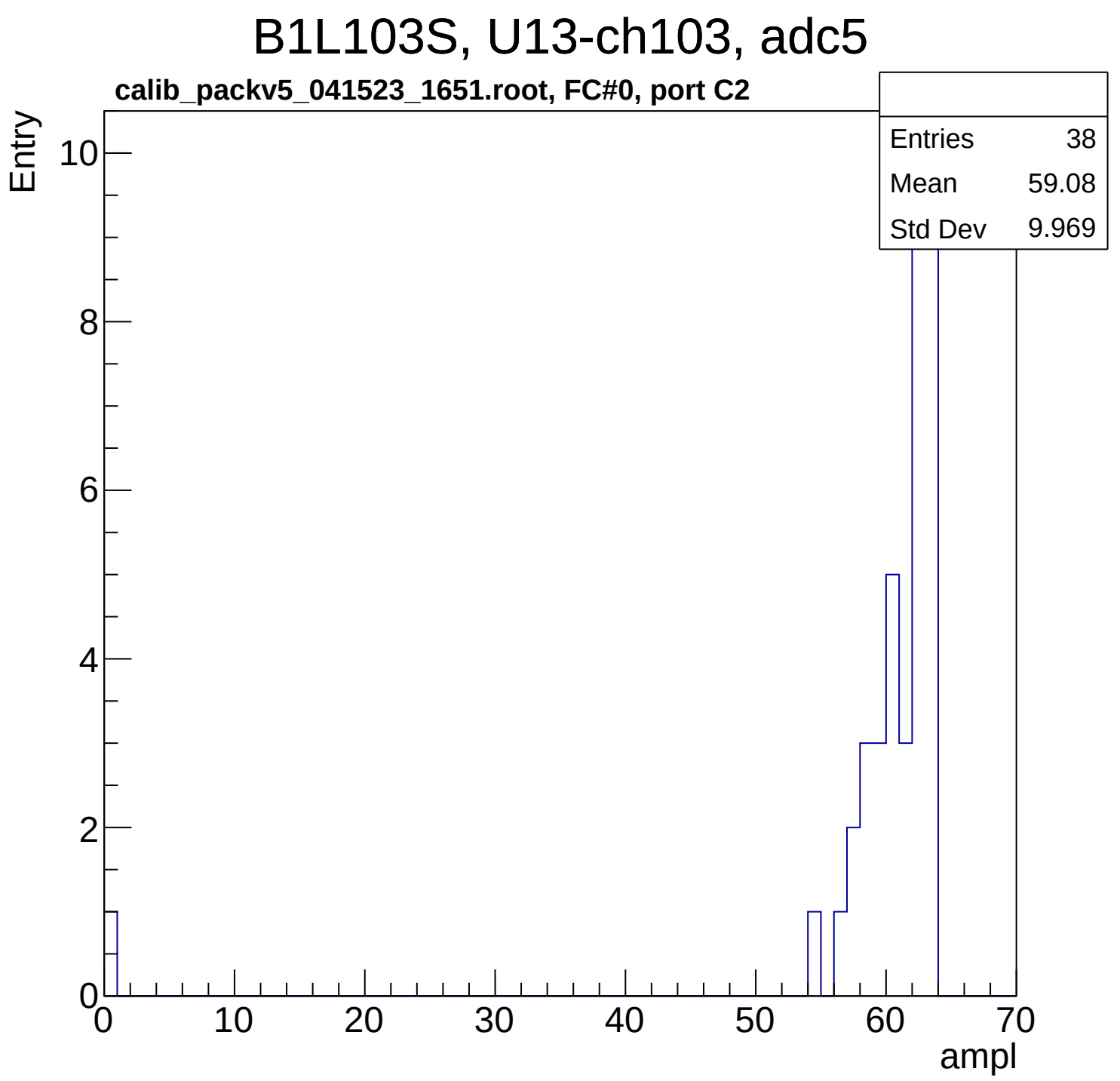
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch103, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 59.08
Std Dev 9.969
Entry
ampl
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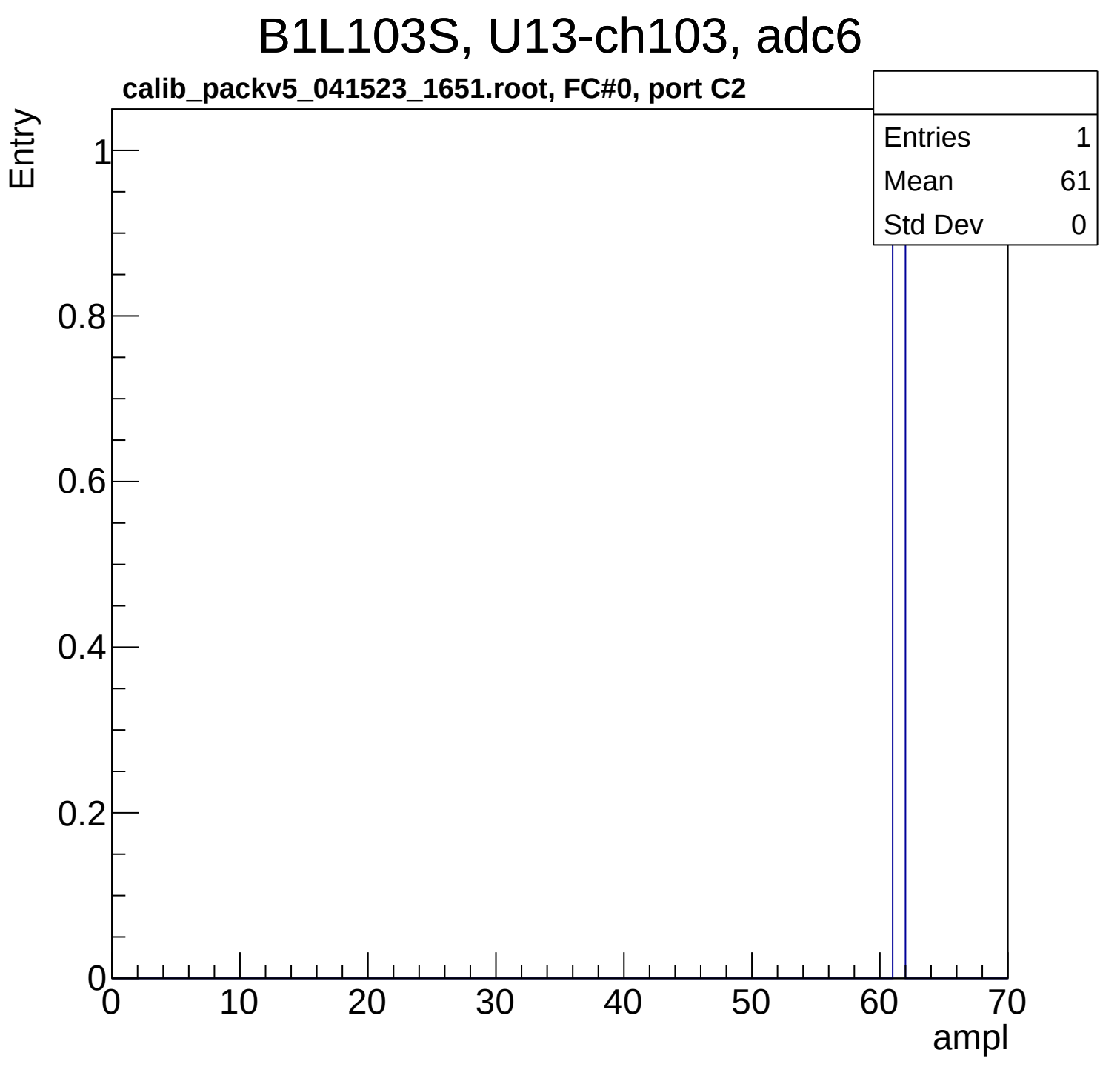
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch103, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 61
Std Dev 0
Entry
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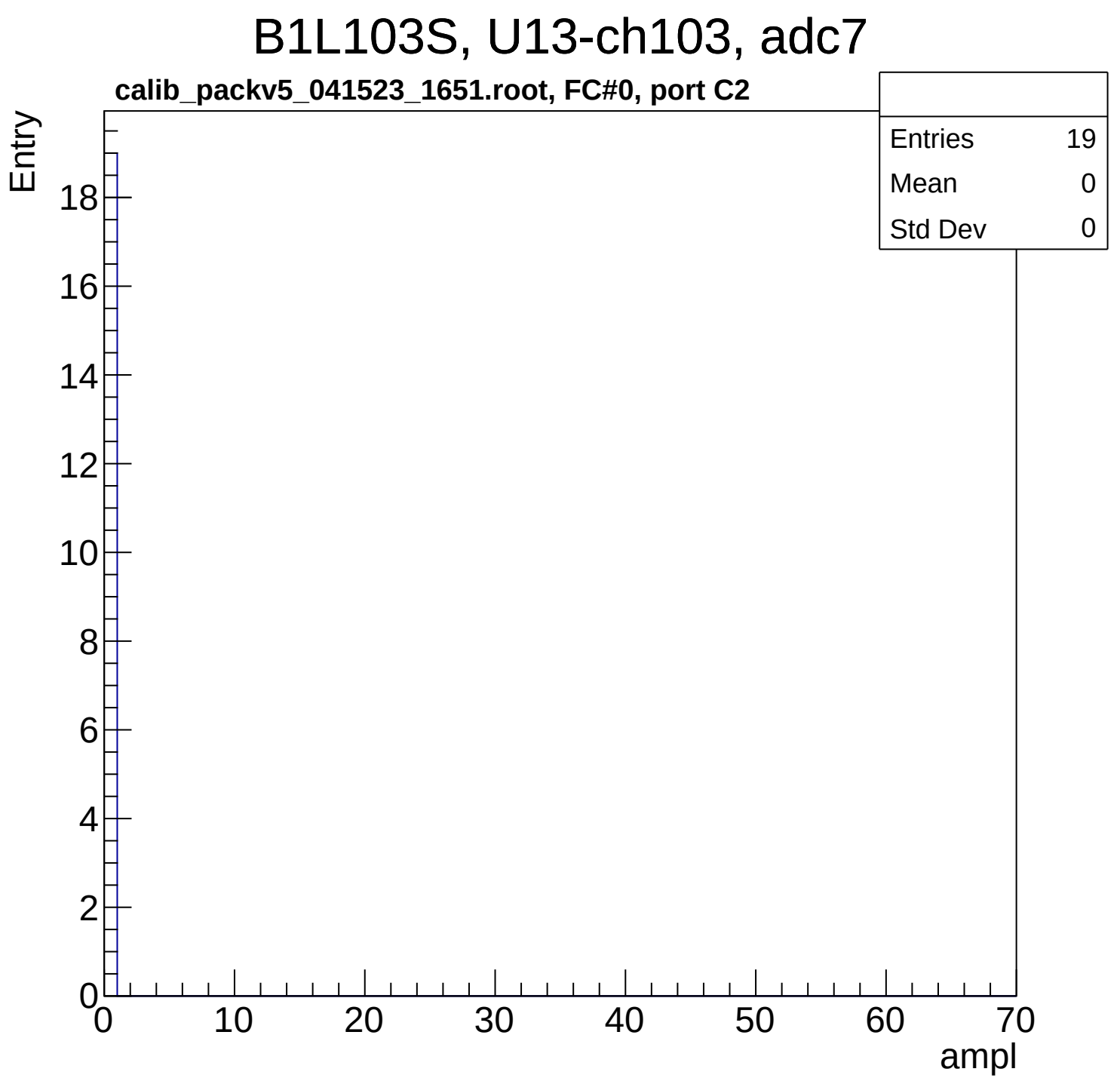
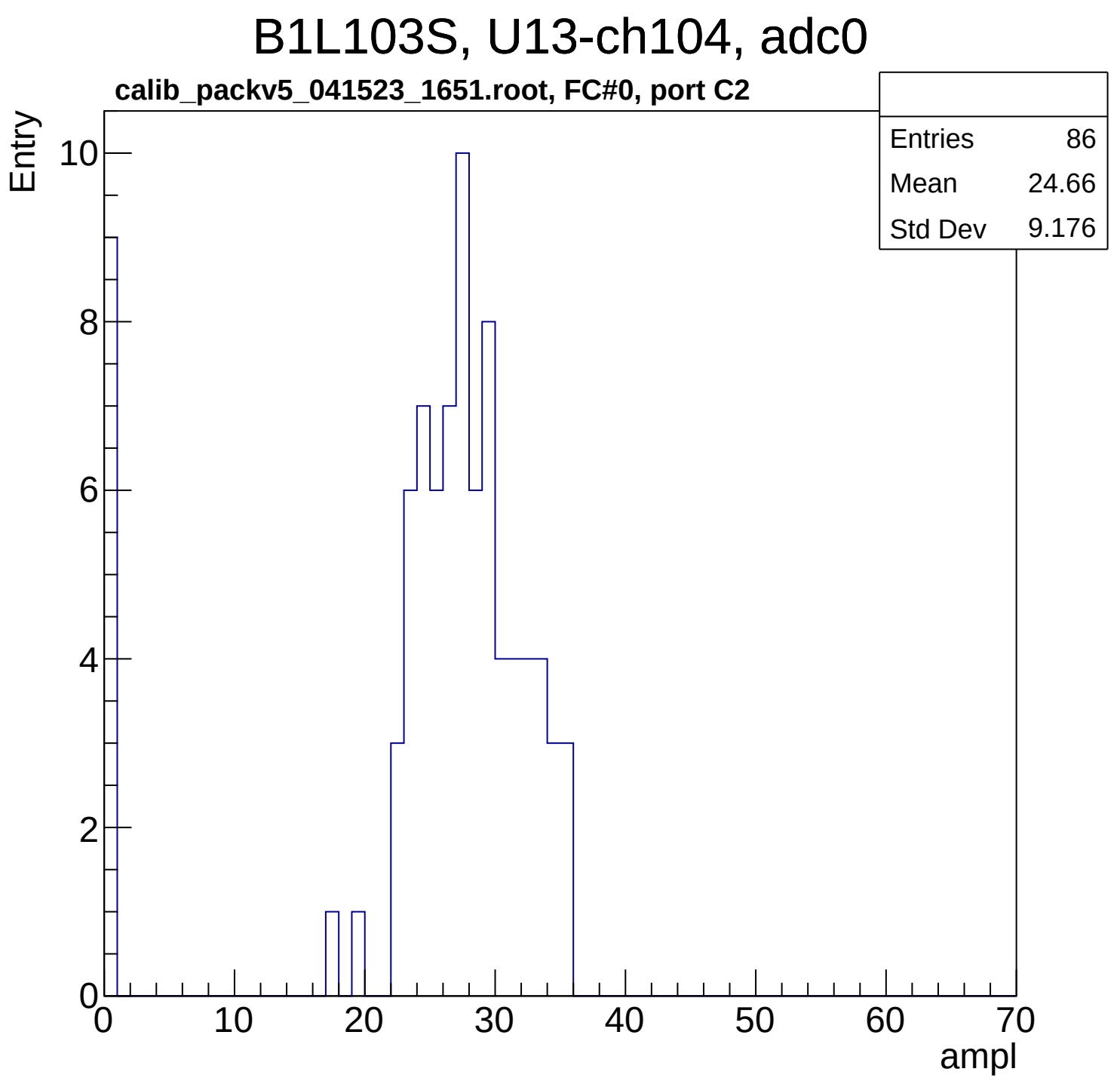
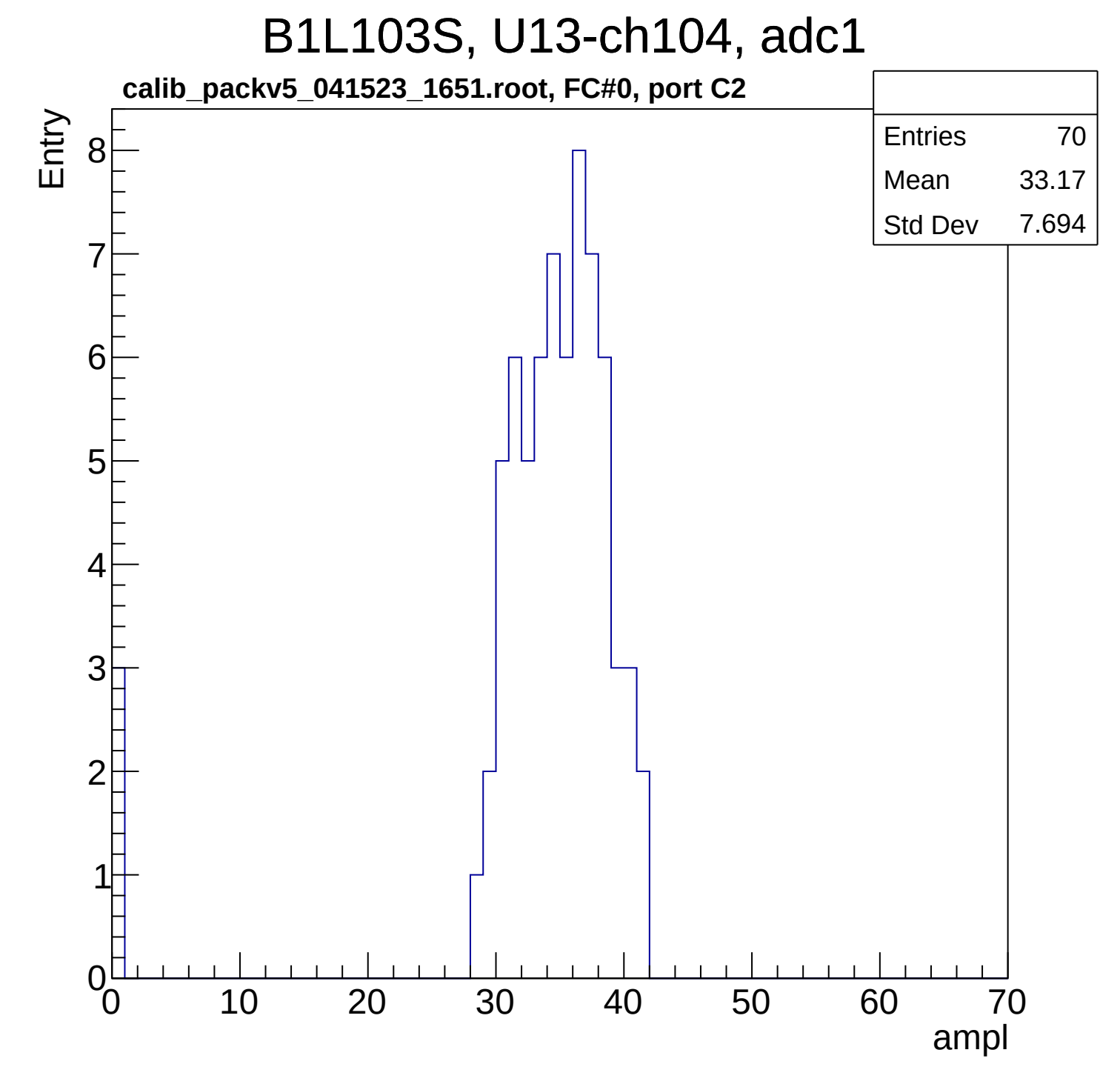
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch103, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch104, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 24.66
Std Dev 9.176
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch104, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 33.17
Std Dev 7.694
Entry
ampl
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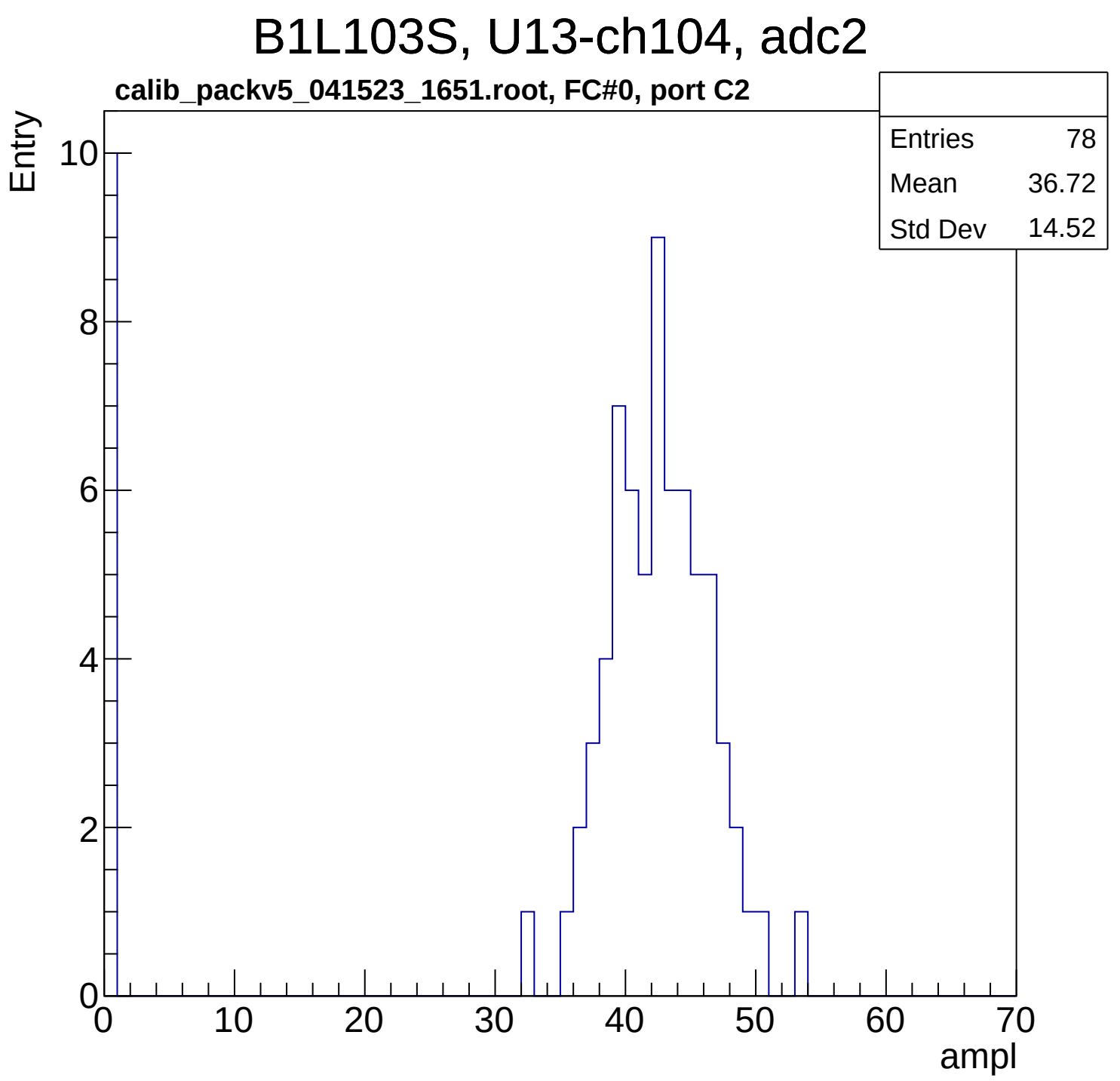
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch104, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 36.72
Std Dev 14.52
Entry
ampl
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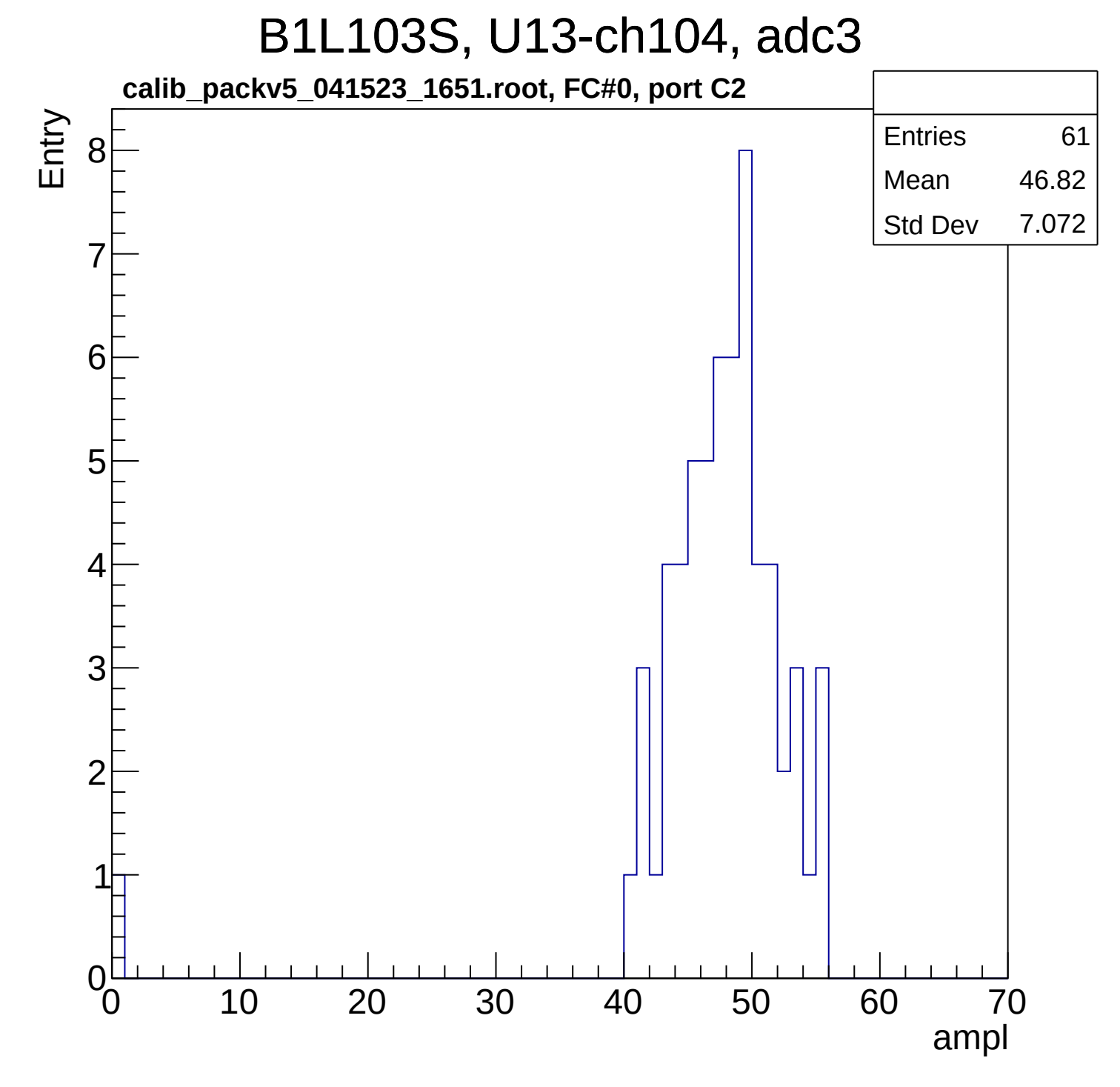
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch104, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 46.82
Std Dev 7.072
Entry
ampl
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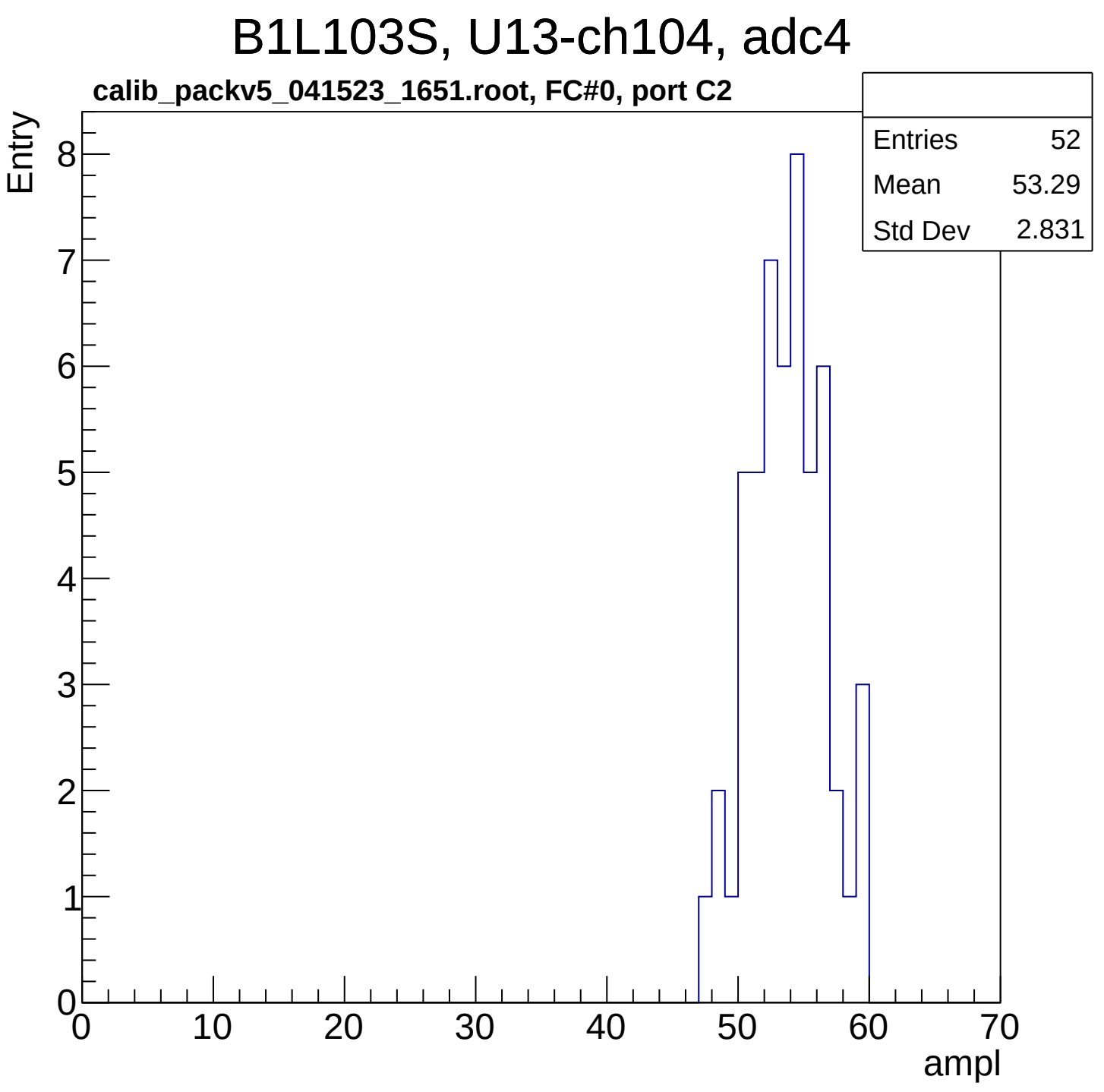
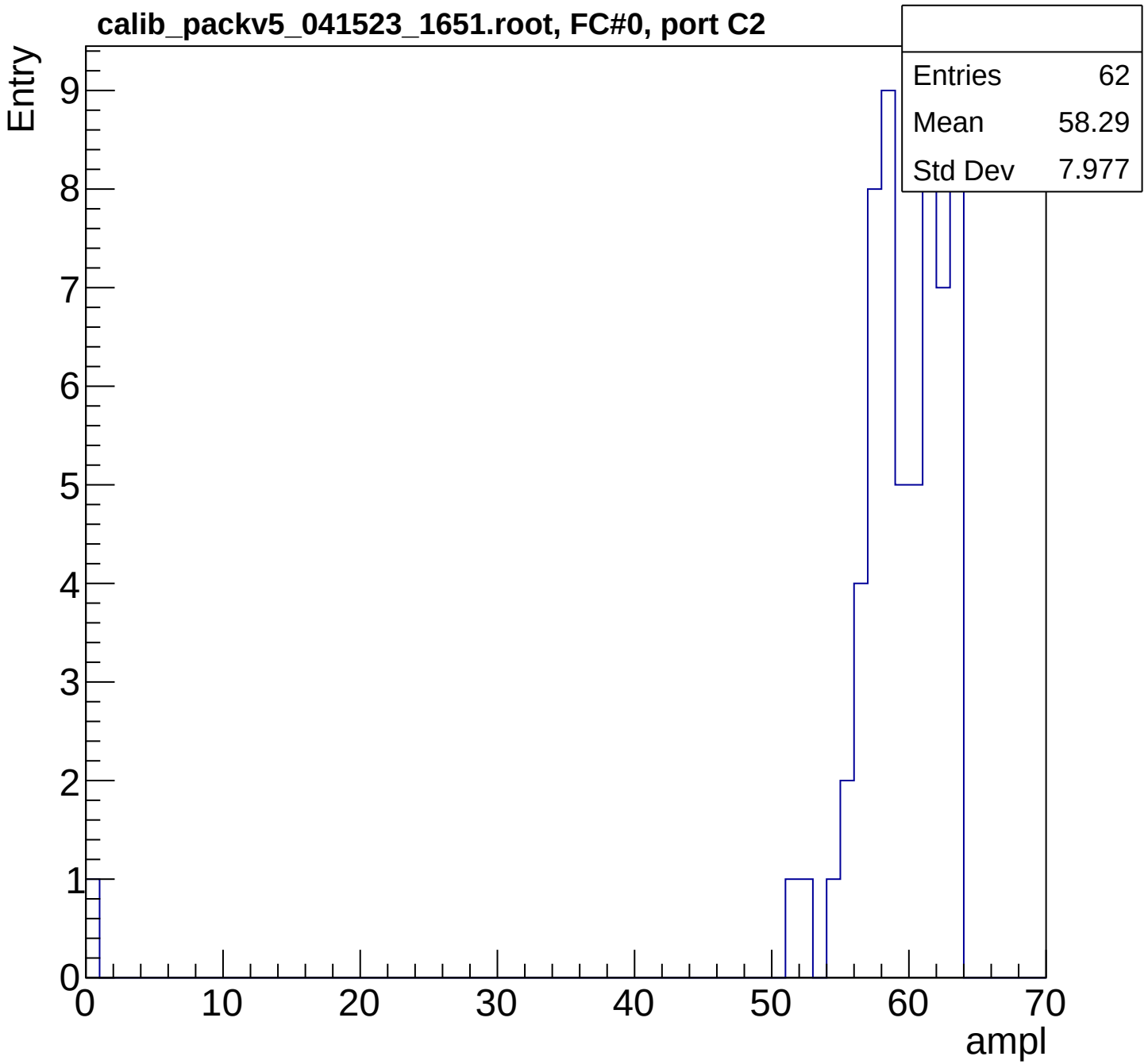
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch104, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 53.29
Std Dev 2.831
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch104, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 58.29
Std Dev 7.977
Entry
ampl
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20
30
40
50
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2
3
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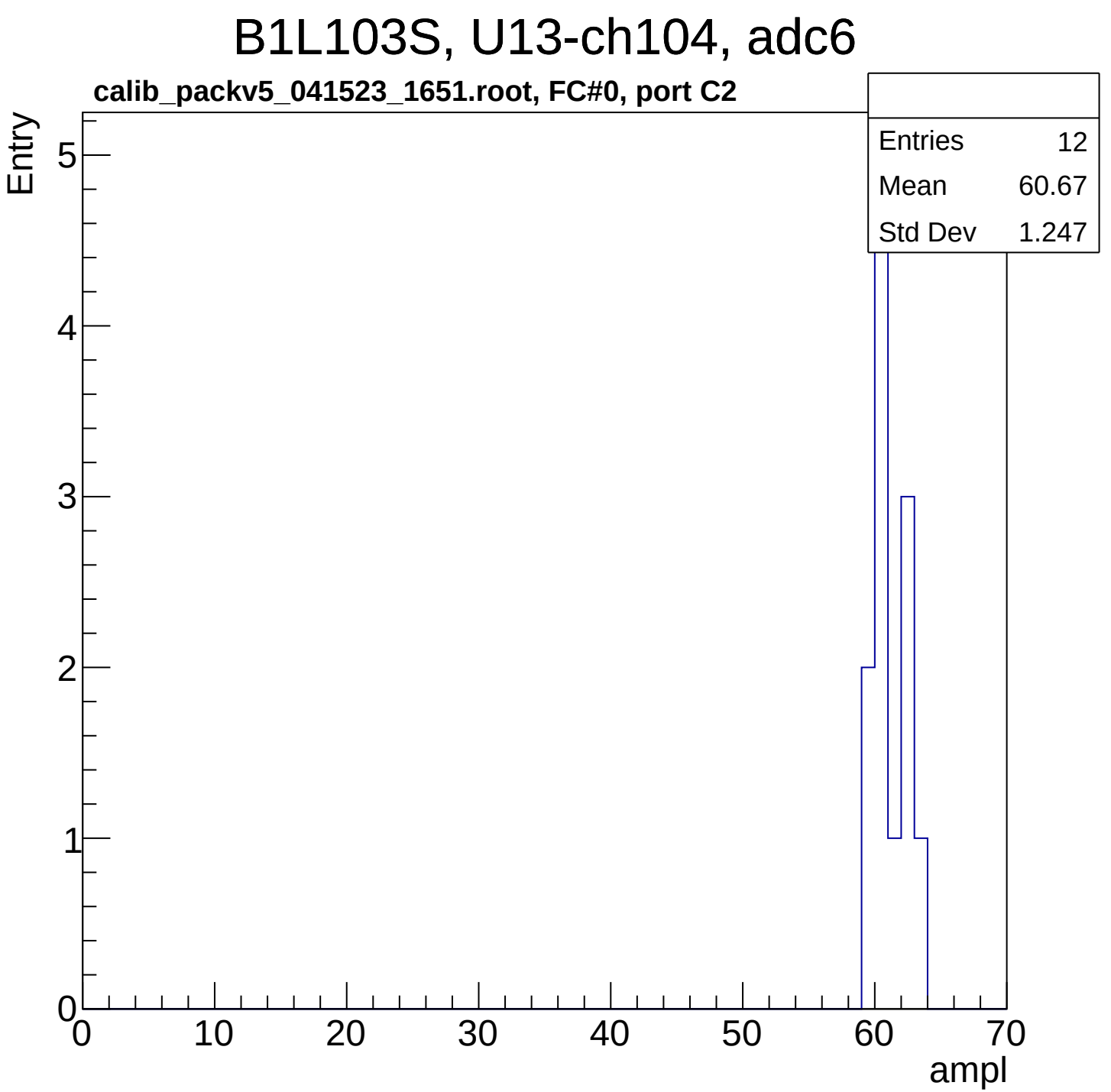
8
9


B1L103S, U13-ch104, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 60.67
Std Dev 1.247
Entry
ampl
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0
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40
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60
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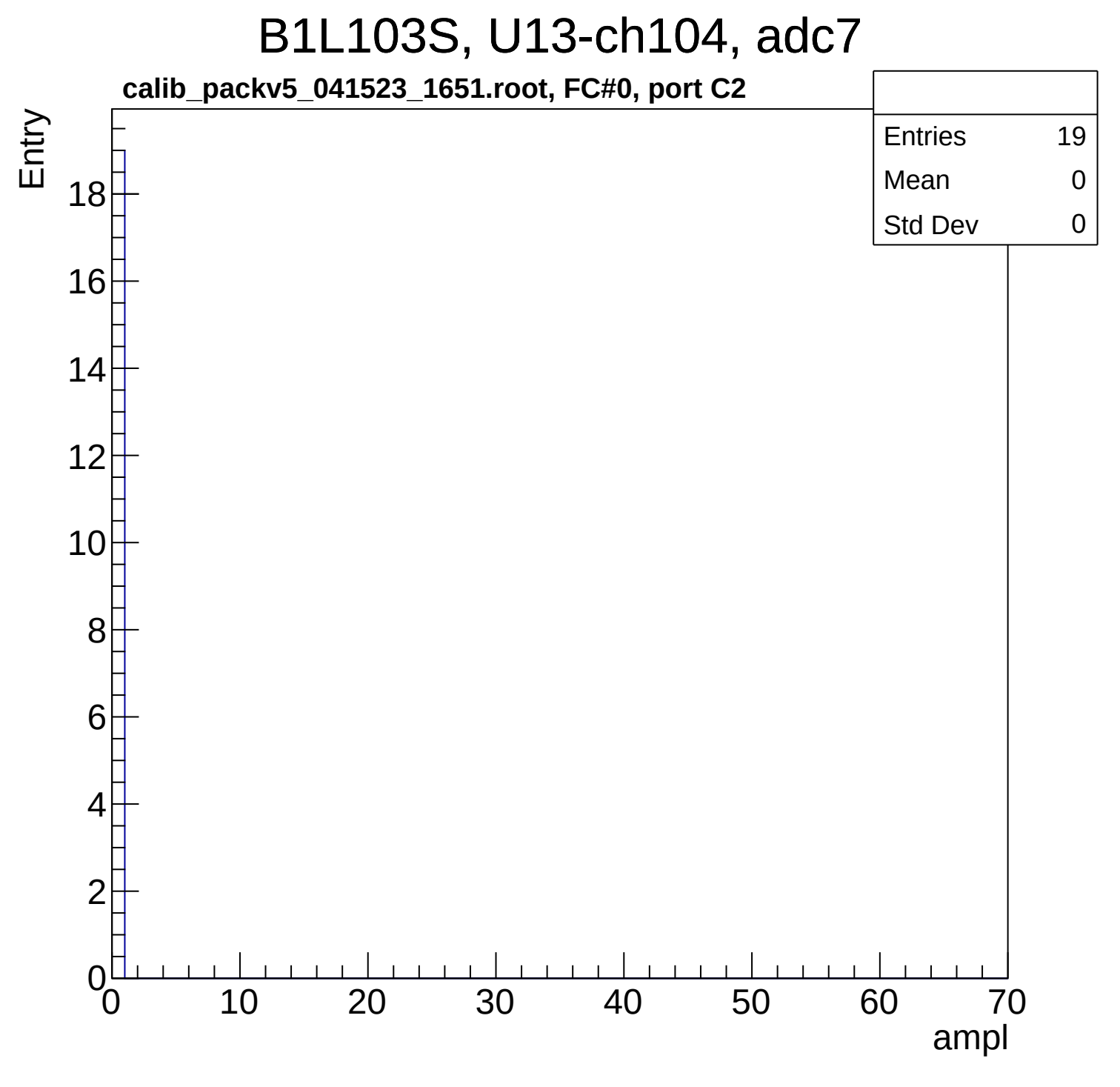
B1L103S, U13-ch104, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
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6
8
10
12
14
16
18
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10
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30
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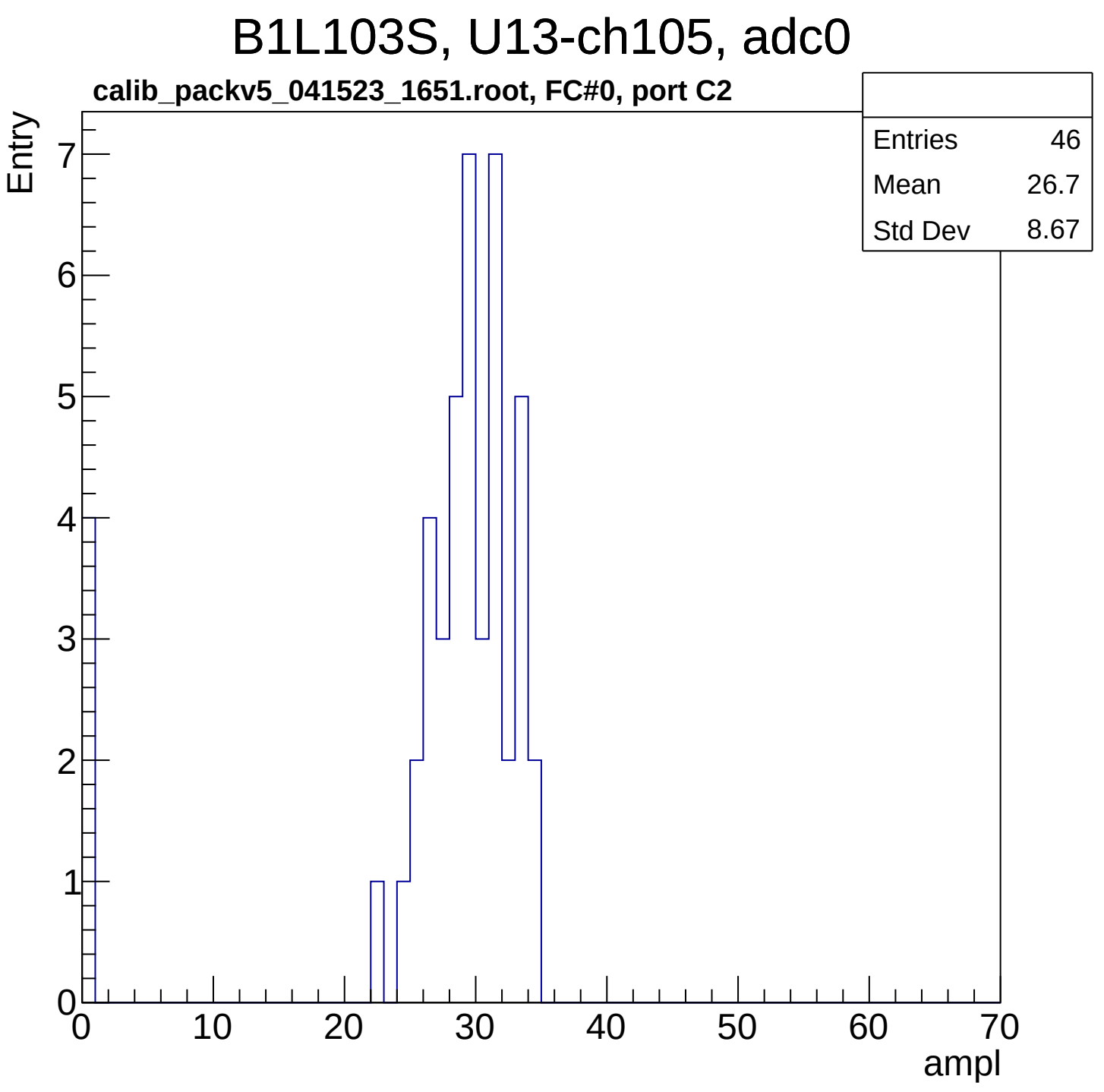
50
60
70
ampl


B1L103S, U13-ch105, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 26.7
Std Dev 8.67
Entry
ampl
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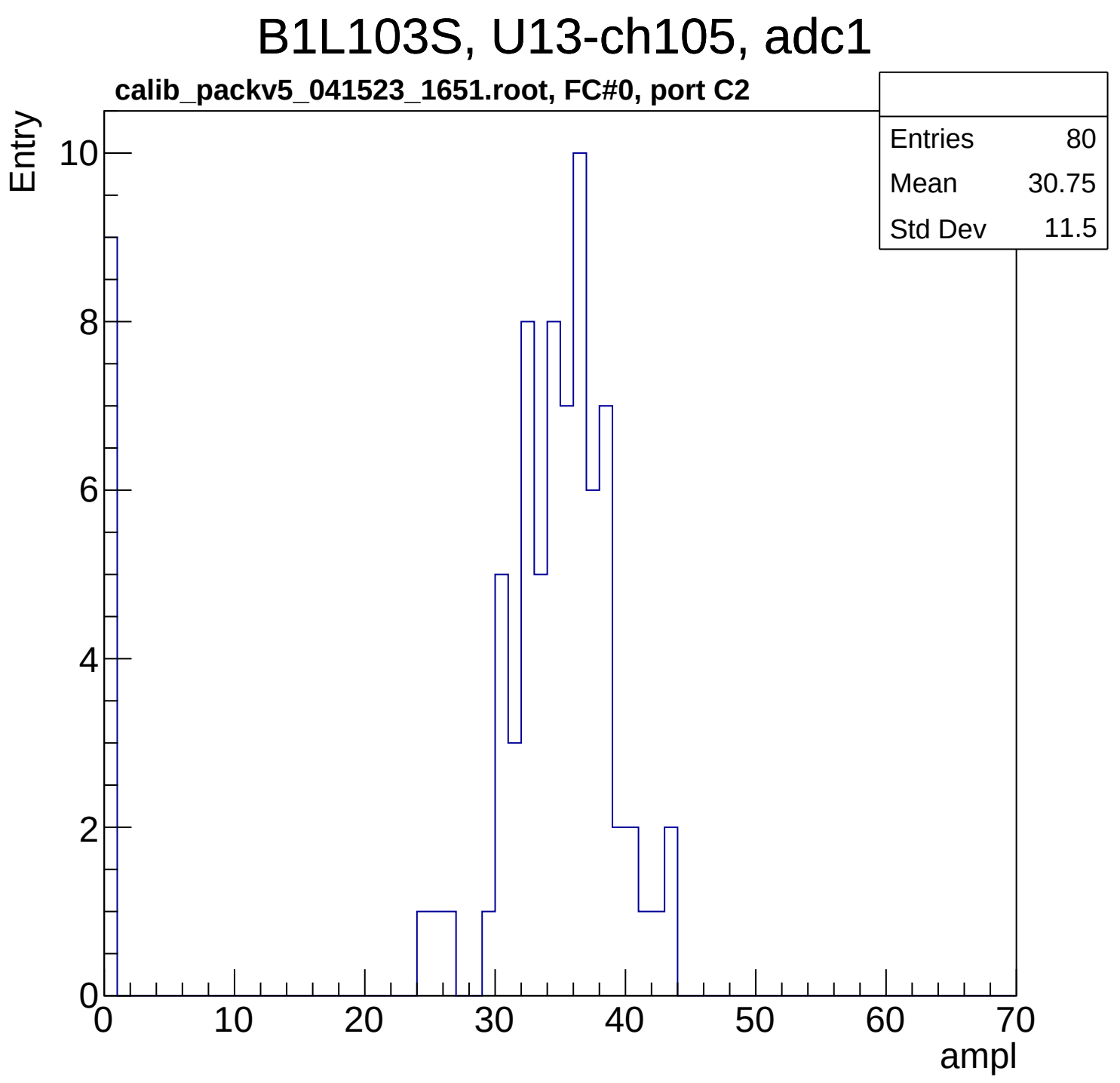
B1L103S, U13-ch105, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 30.75
Std Dev 11.5
Entry
ampl
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4
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0
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40
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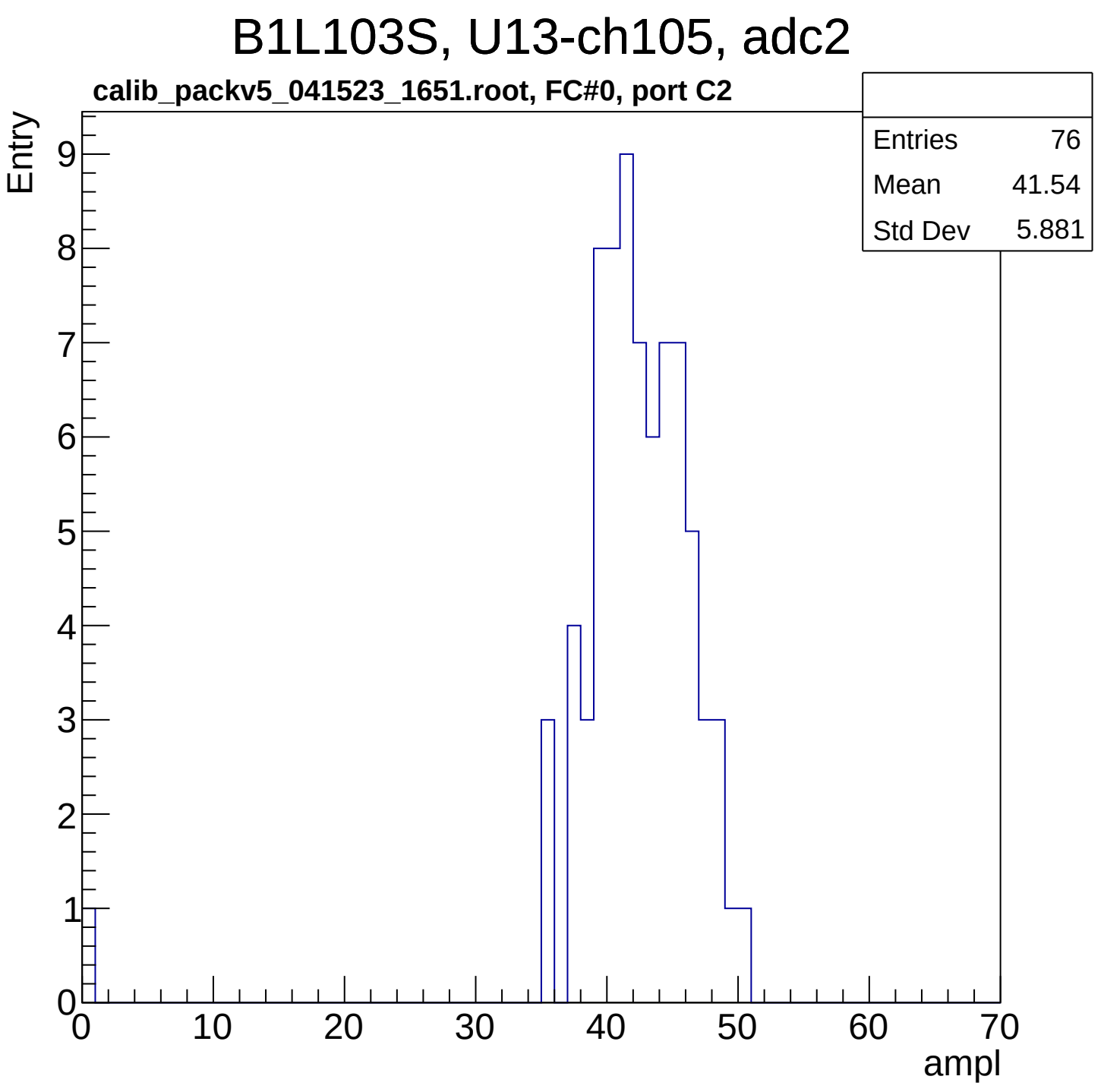
B1L103S, U13-ch105, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 41.54
Std Dev 5.881
Entry
ampl
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3
4
5
6
7
8
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0
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40
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60
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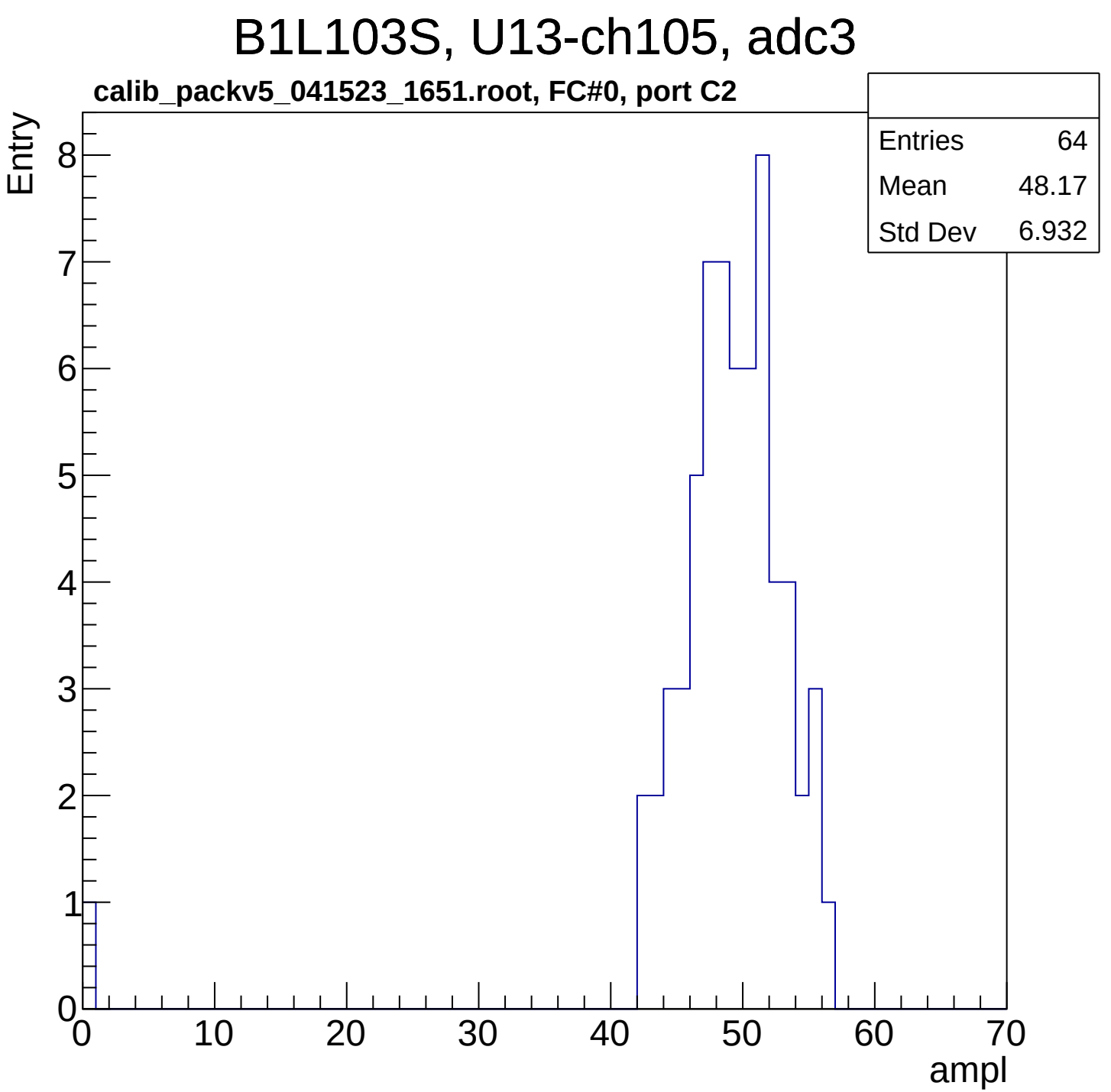
B1L103S, U13-ch105, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 48.17
Std Dev 6.932
Entry
ampl
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2
3
4
5
6
7
8
0
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40
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60
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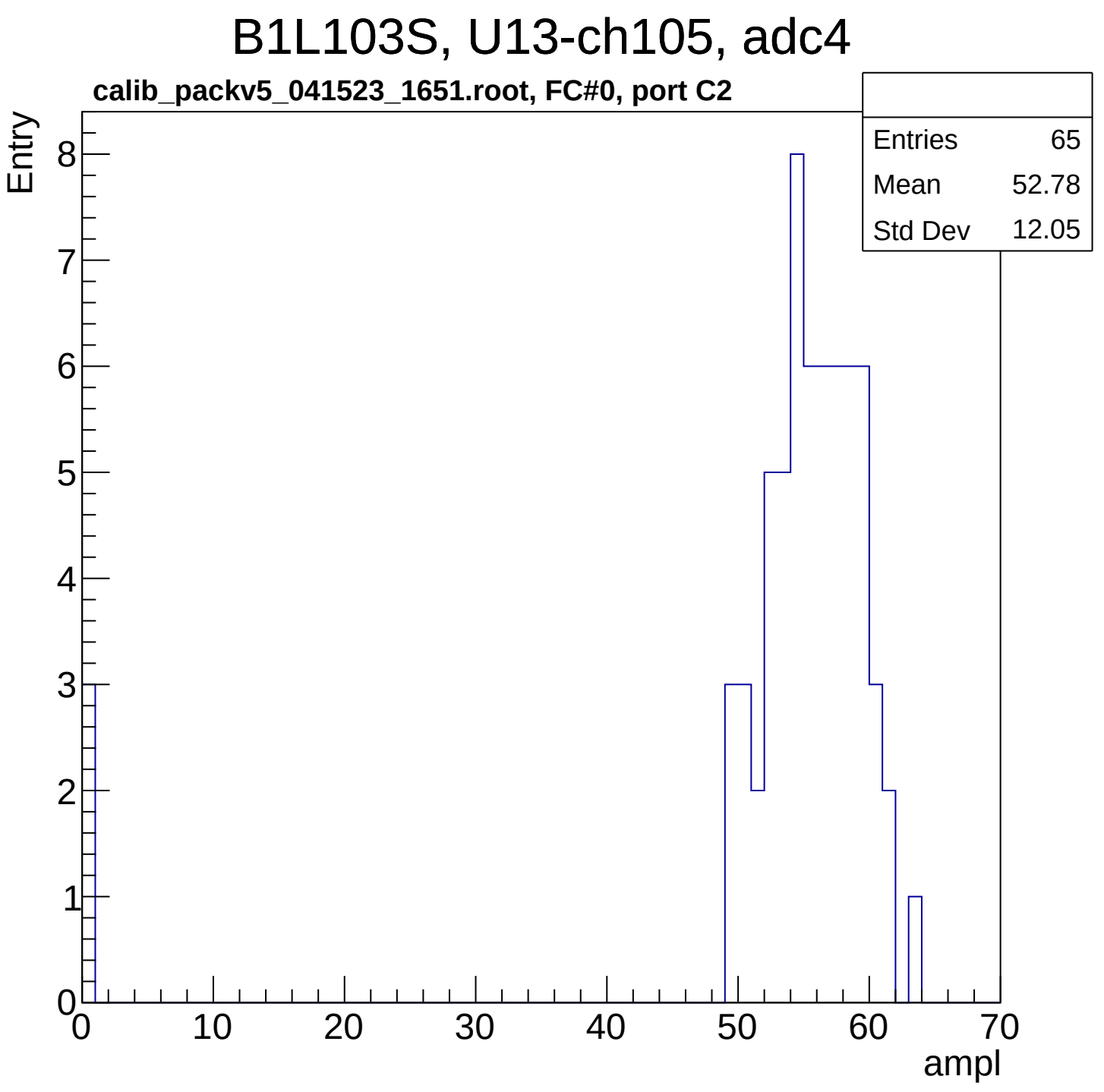
B1L103S, U13-ch105, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 52.78
Std Dev 12.05
Entry
ampl
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2
3
4
5
6
7
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0
10
20
30
40
50
60
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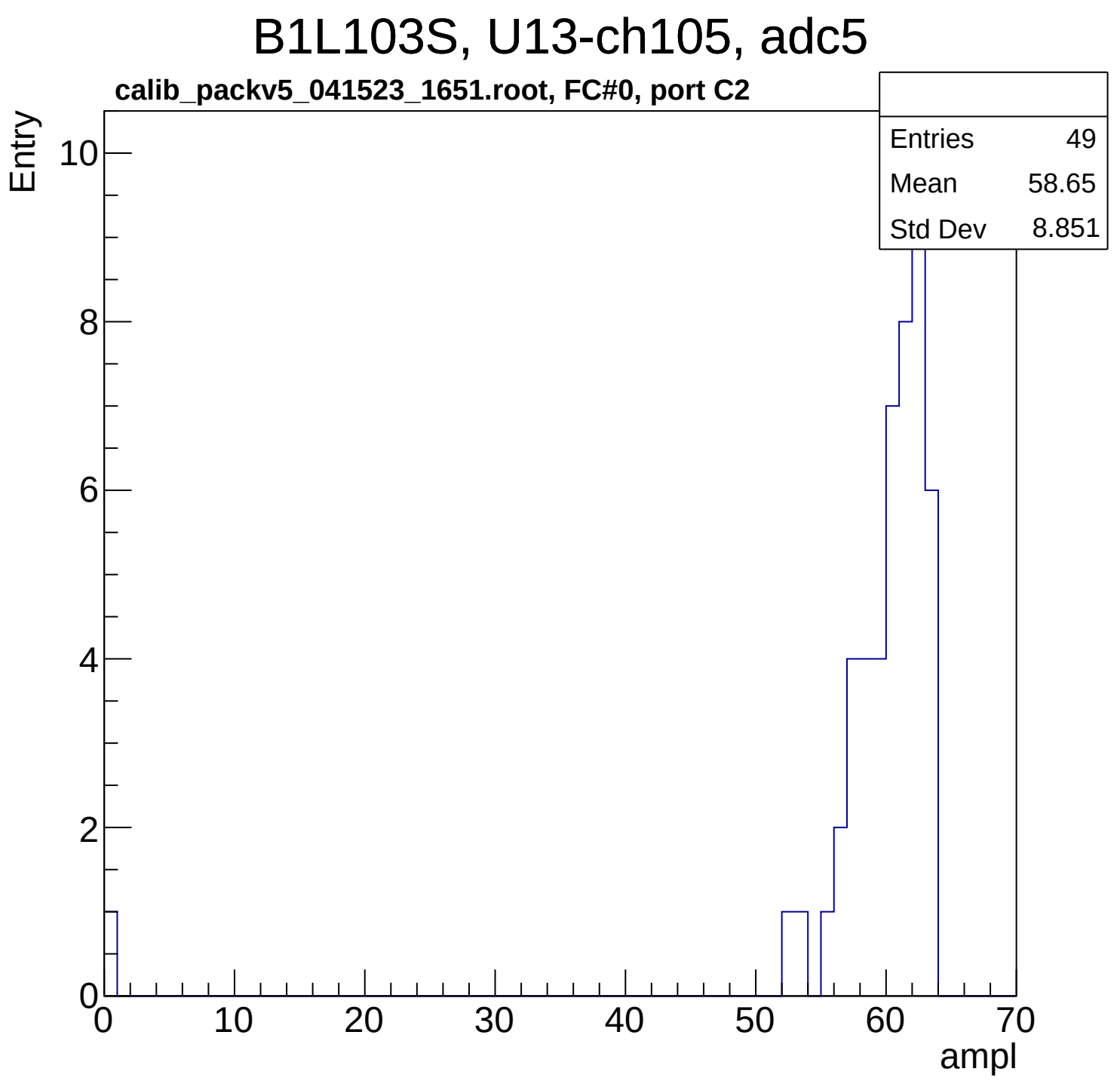
B1L103S, U13-ch105, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.65
Std Dev 8.851
Entry
ampl
0
2
4
6
8
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0
10
20
30
40
50
60
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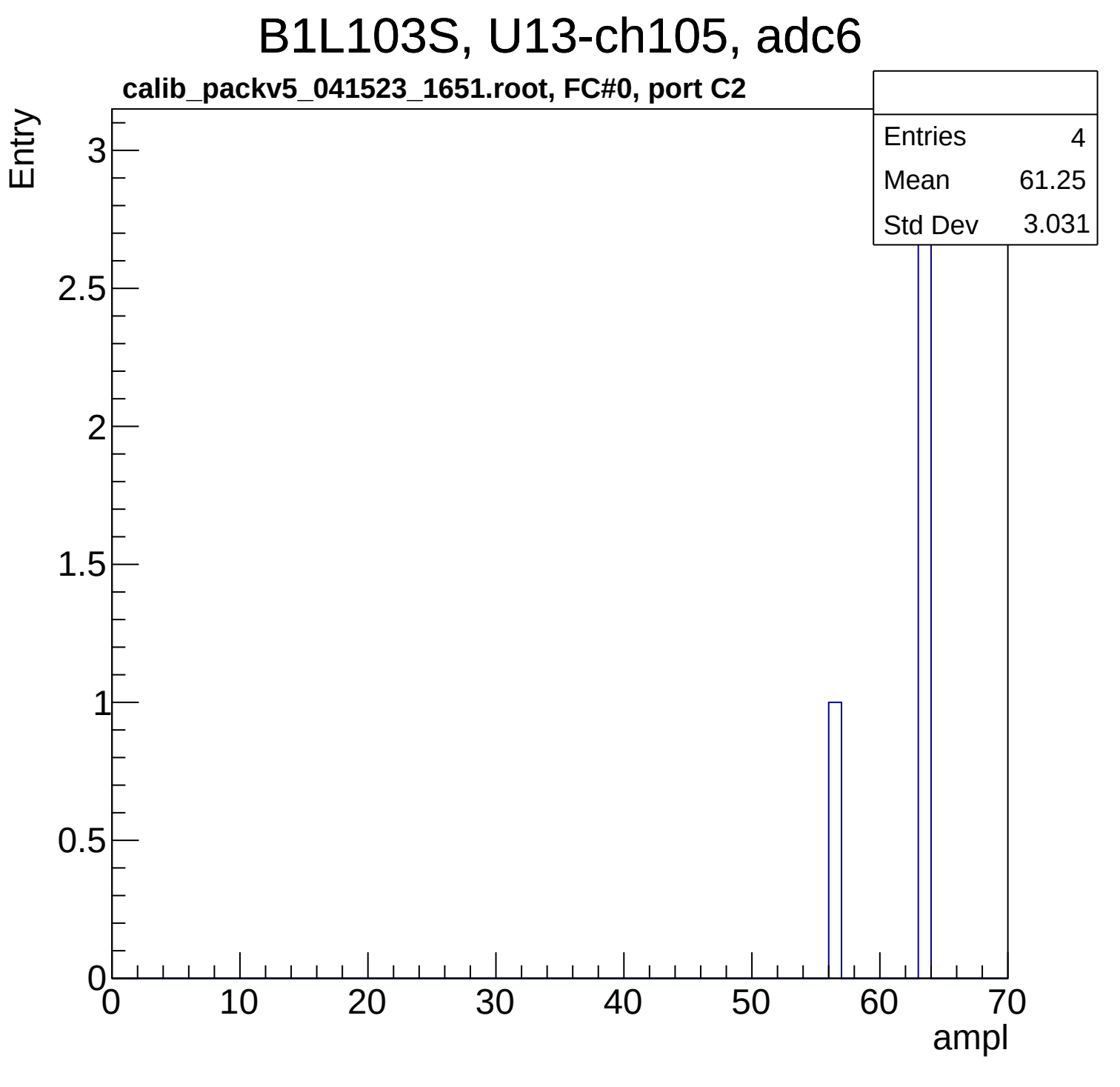
B1L103S, U13-ch105, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61.25
Std Dev 3.031
Entry
ampl
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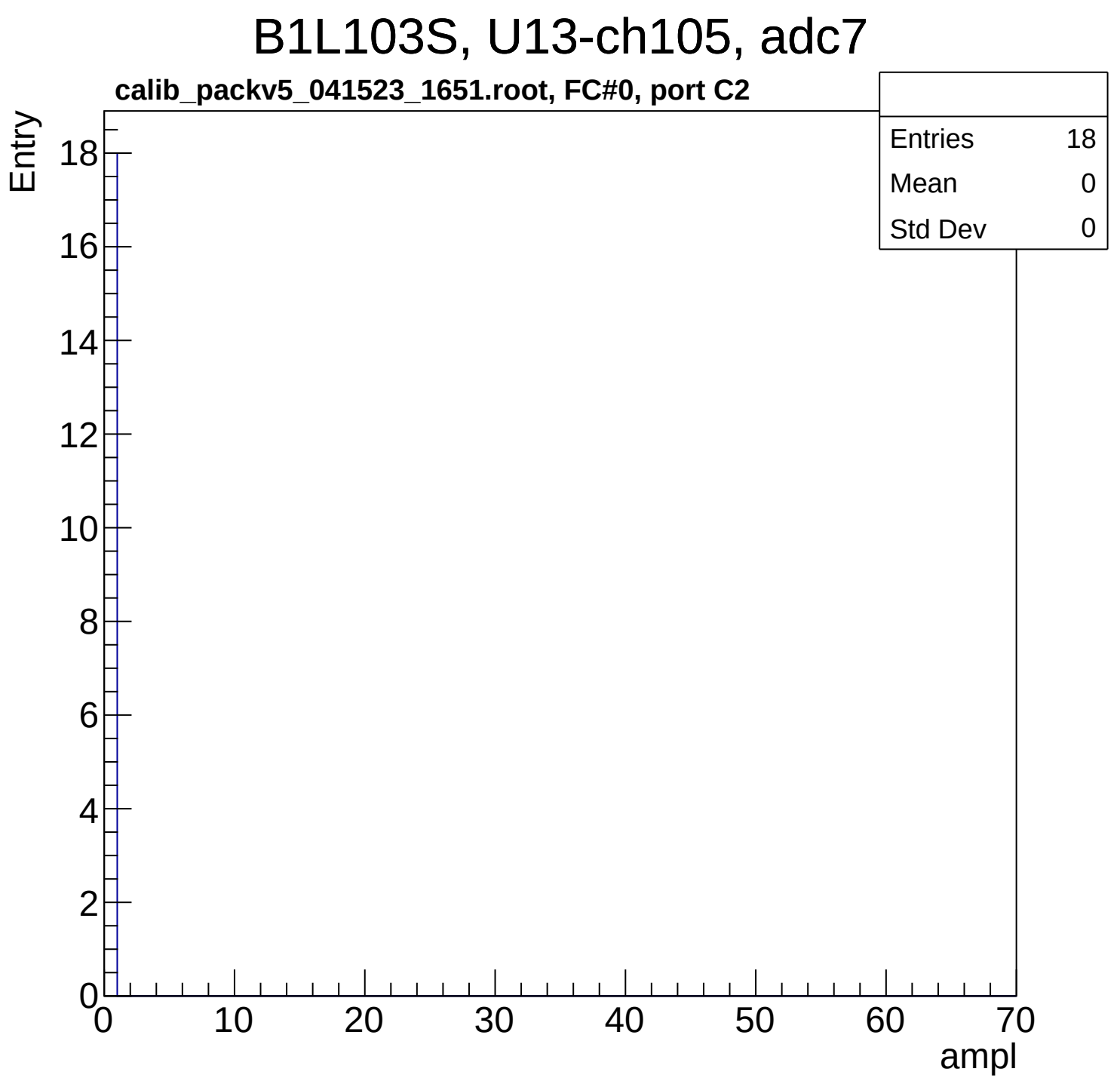
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U13-ch105, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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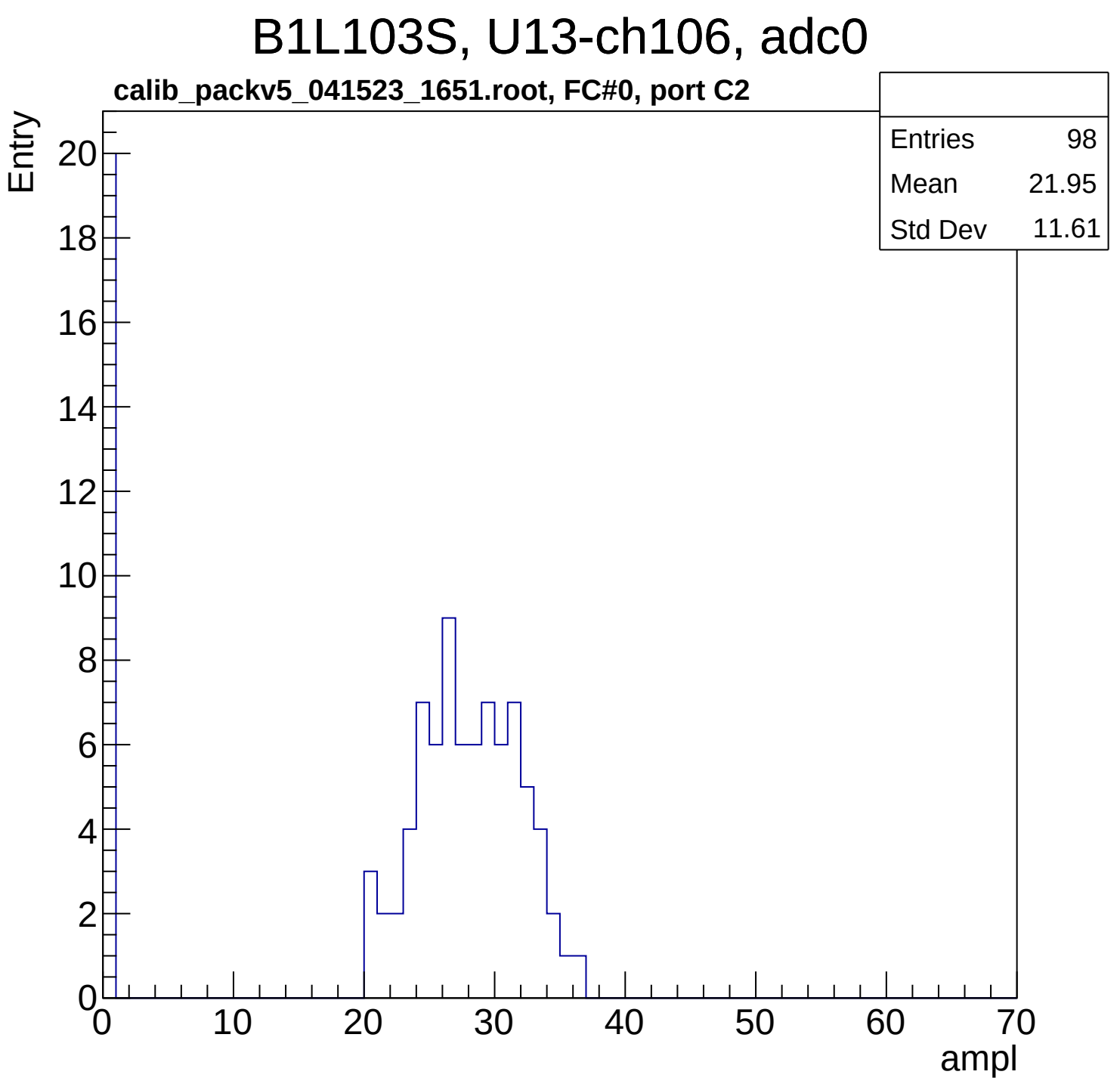
50
60
70
ampl


B1L103S, U13-ch106, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 21.95
Std Dev 11.61
Entry
ampl
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6
8
10
12
14
16
18
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0
10
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30
40
50
60
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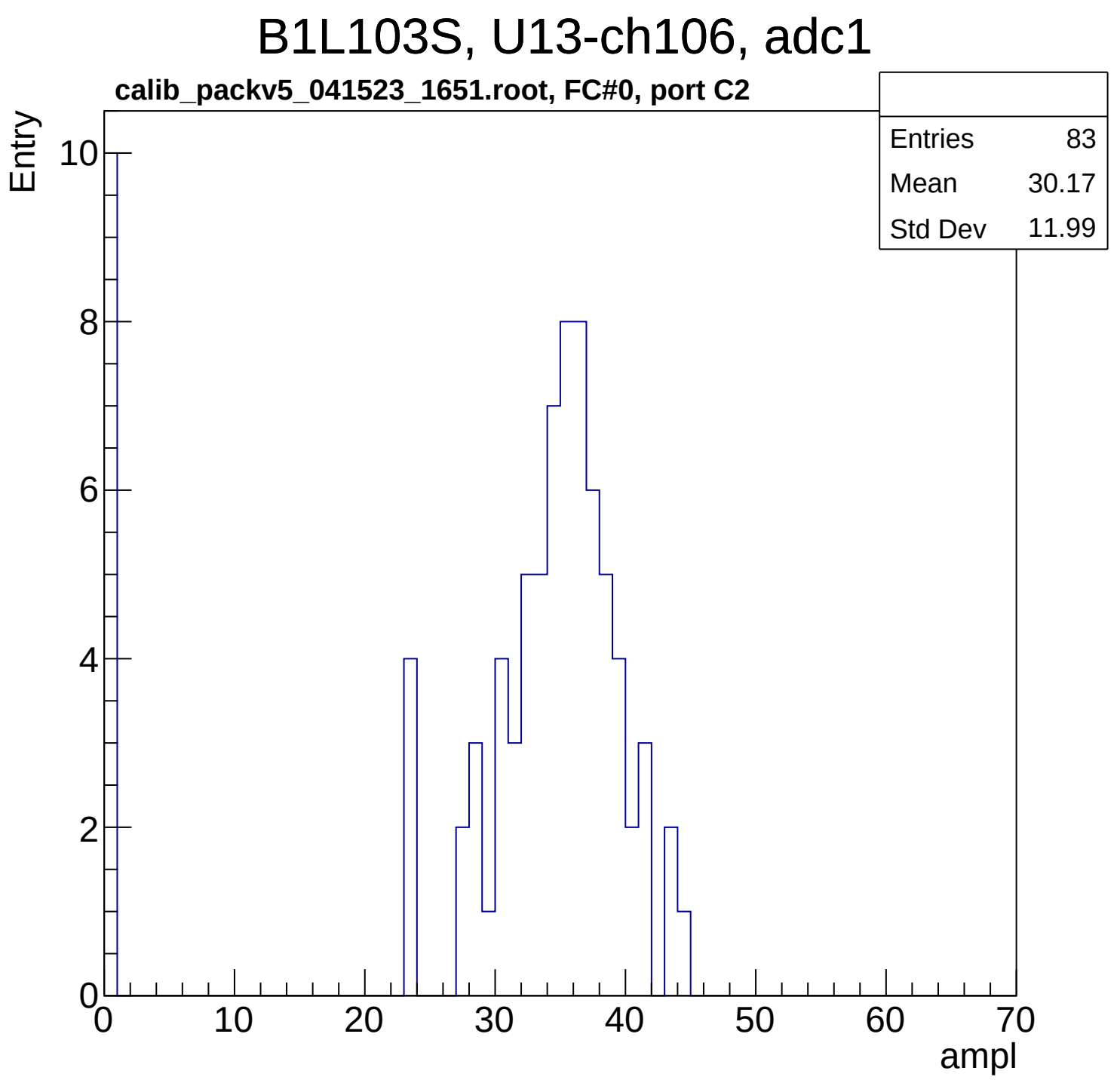
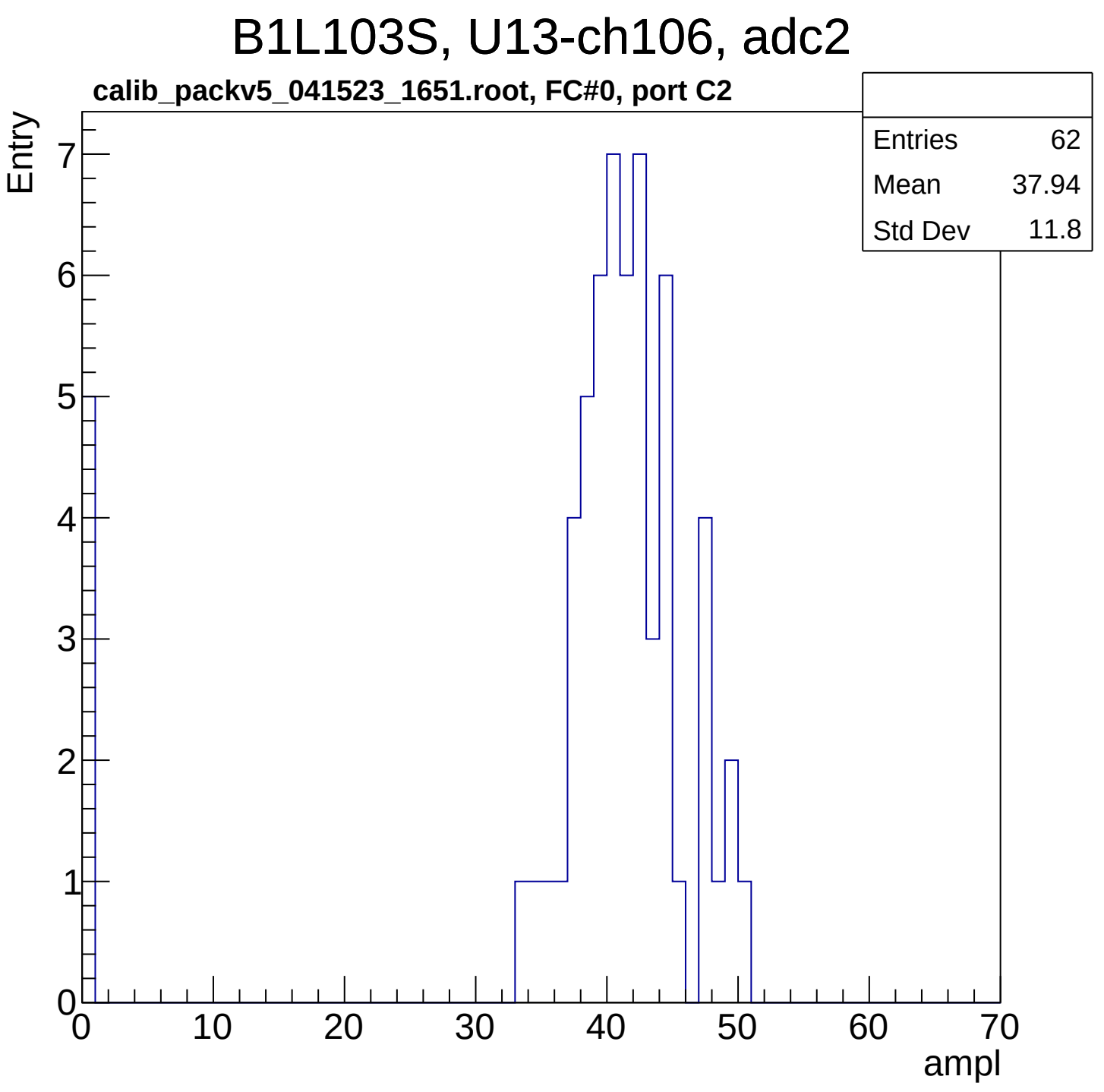
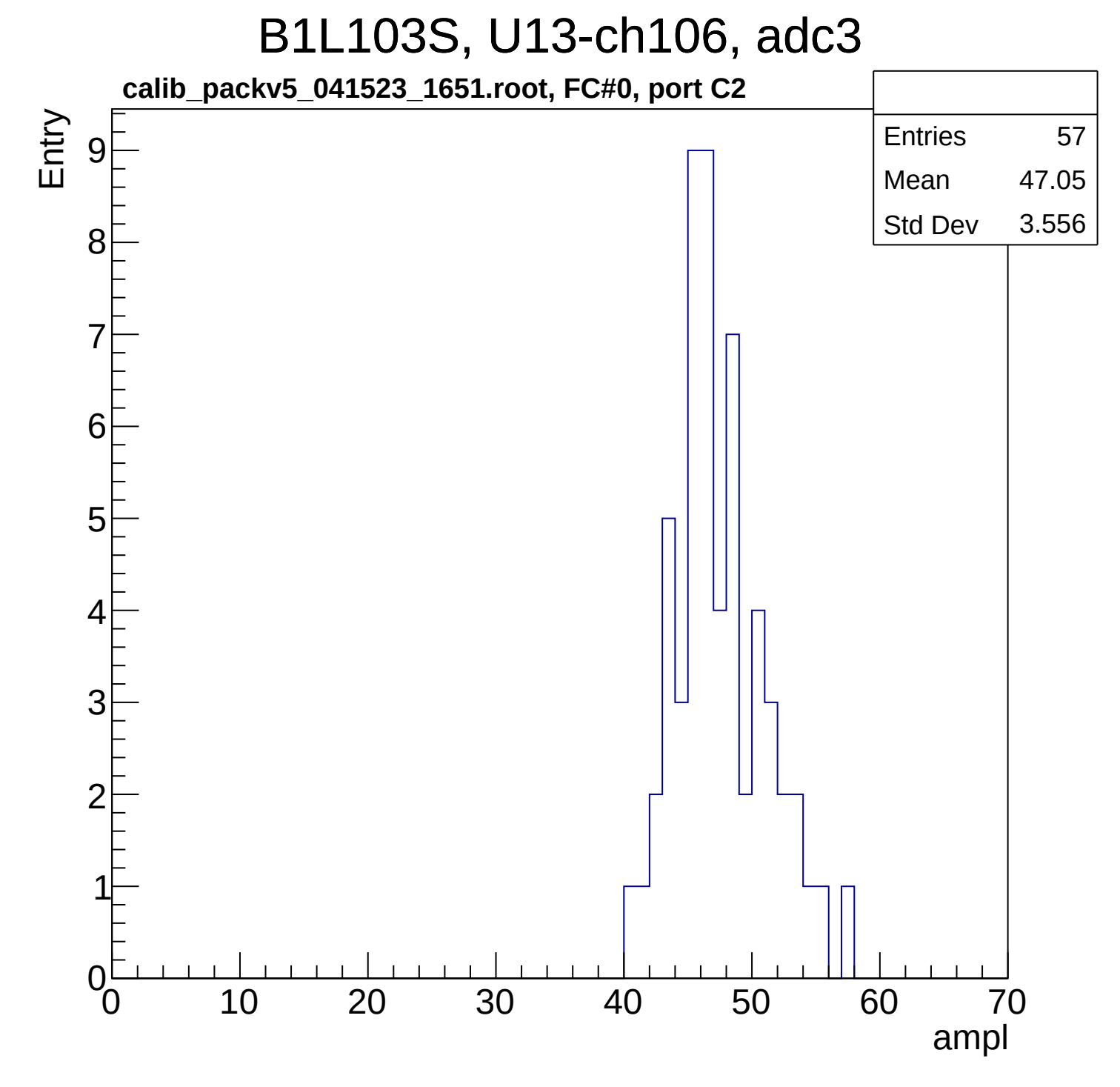

B1L103S, U13-ch106, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 30.17
Std Dev 11.99
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch106, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 37.94
Std Dev 11.8
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch106, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 47.05
Std Dev 3.556
Entry
ampl
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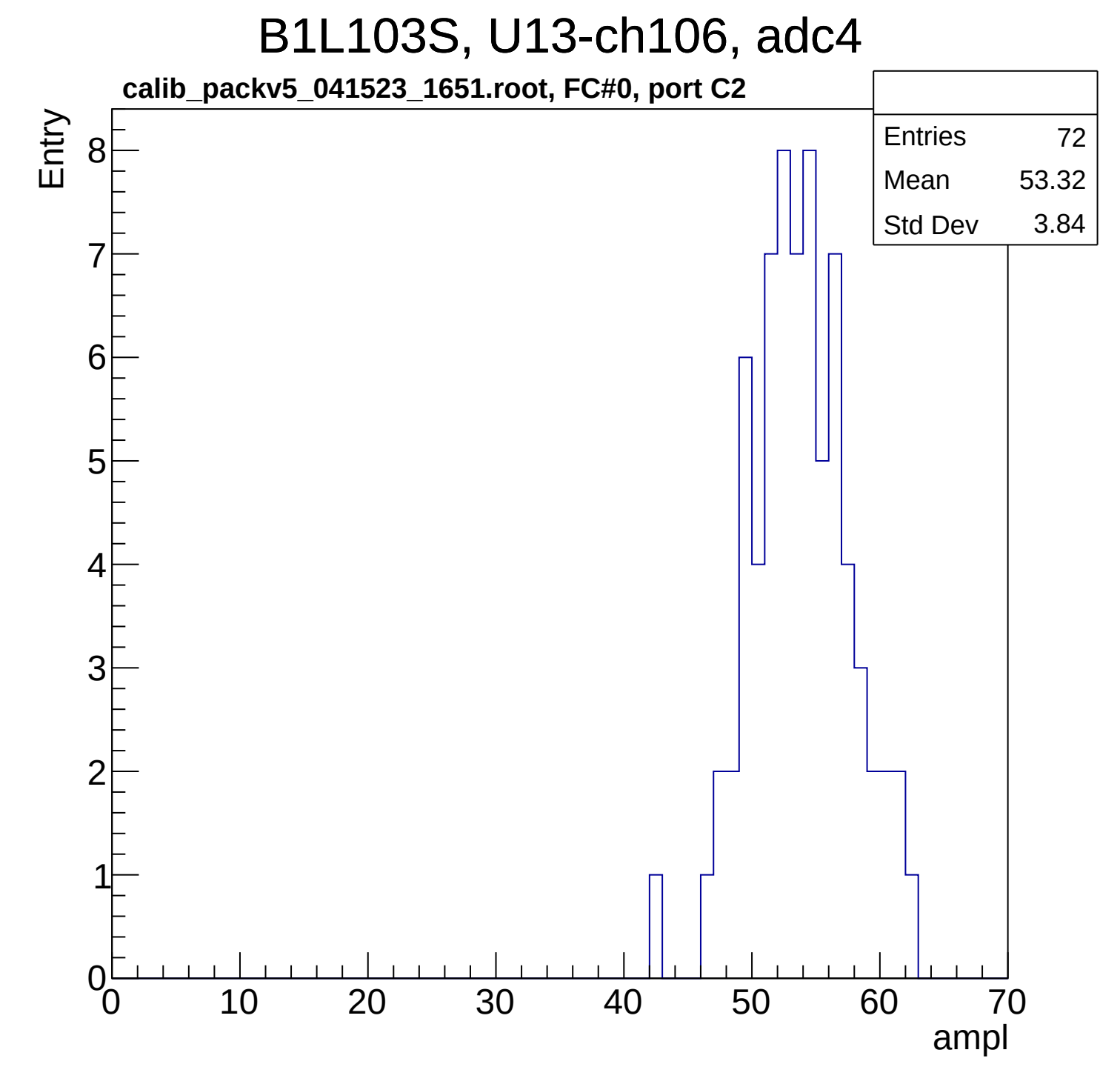
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch106, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 53.32
Std Dev 3.84
Entry
ampl
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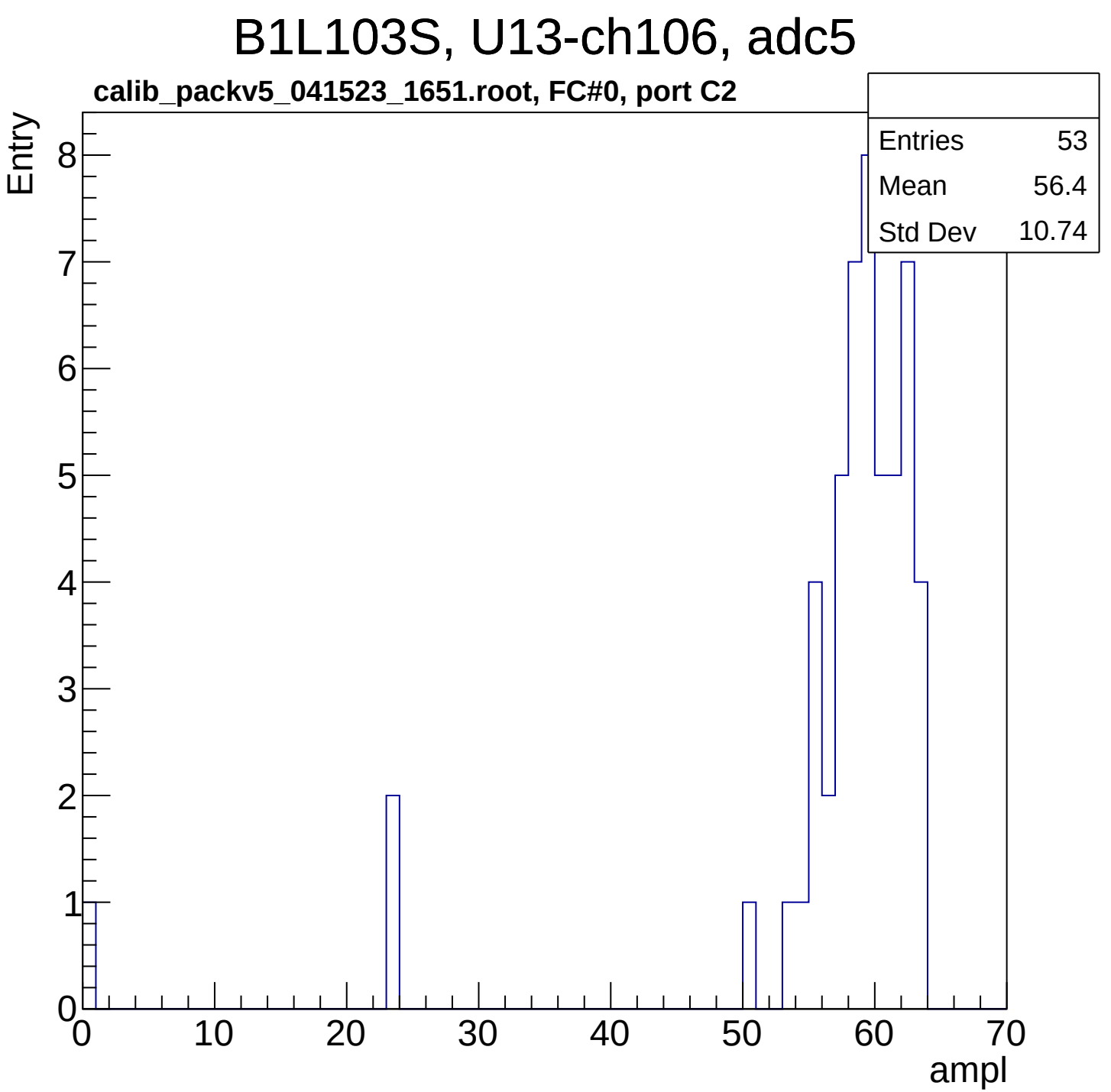
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch106, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 56.4
Std Dev 10.74
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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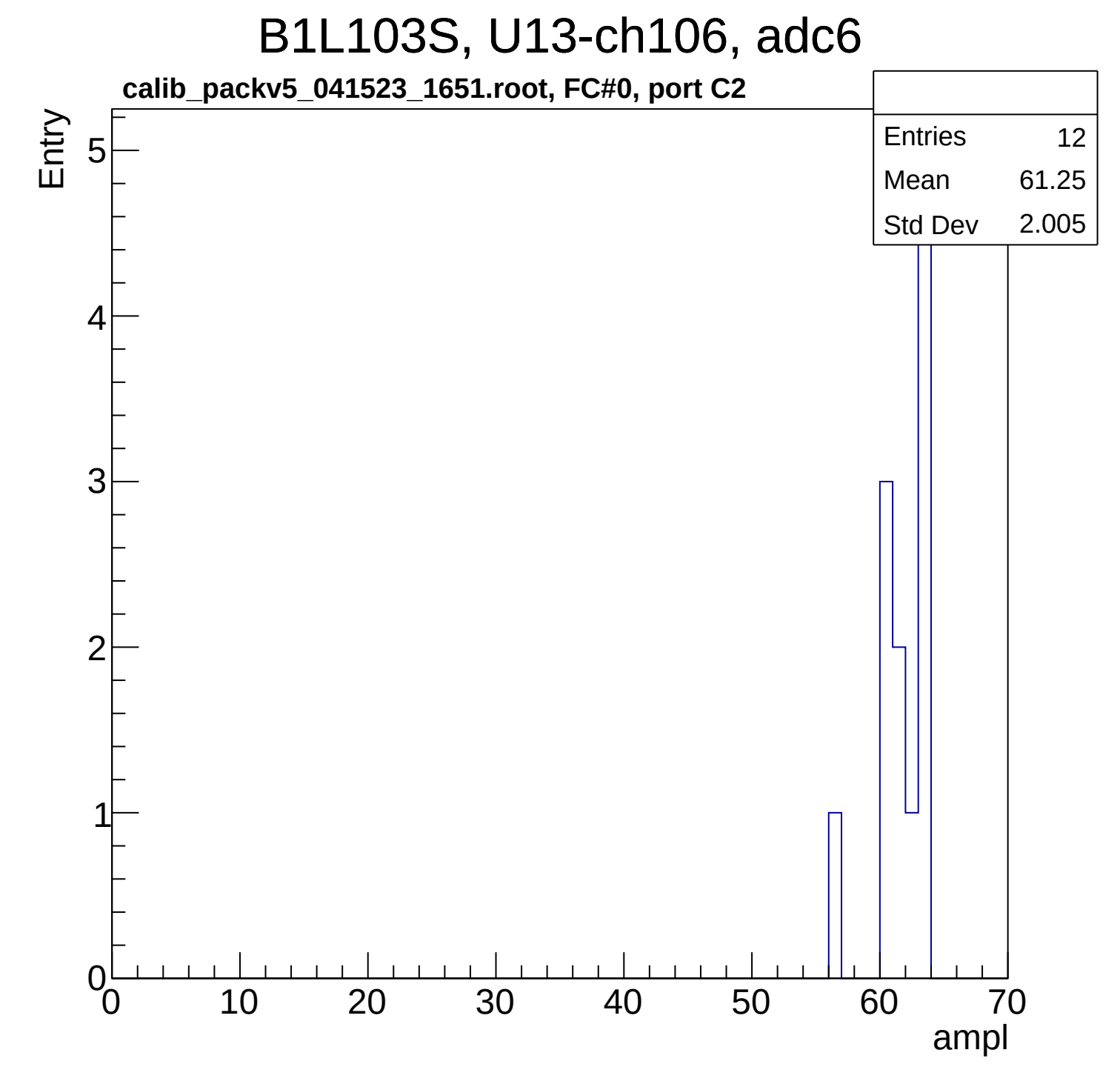
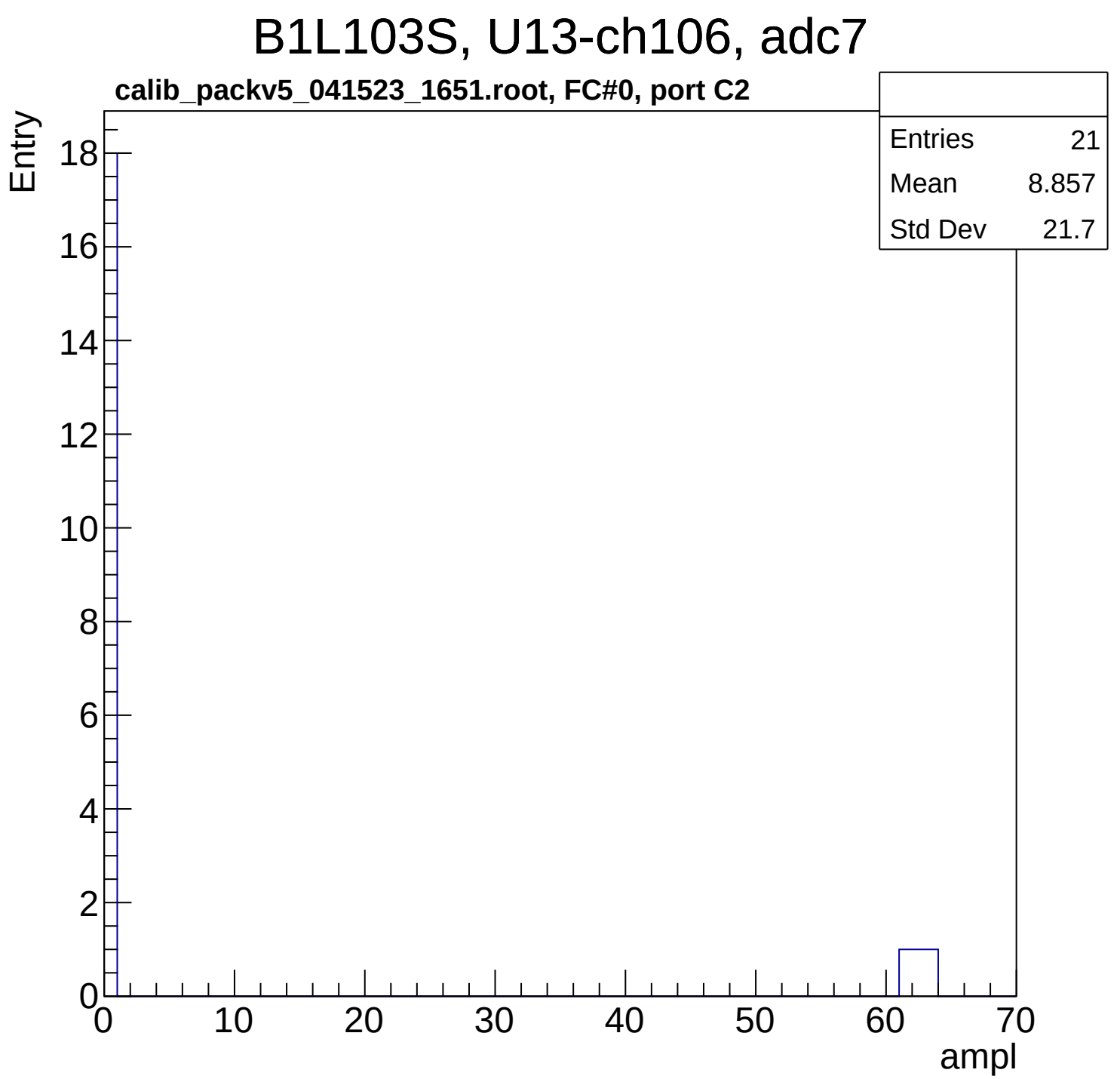

B1L103S, U13-ch106, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.25
Std Dev 2.005
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U13-ch106, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 8.857
Std Dev 21.7
Entry
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6
8
10
12
14
16
18
0
10
20
30
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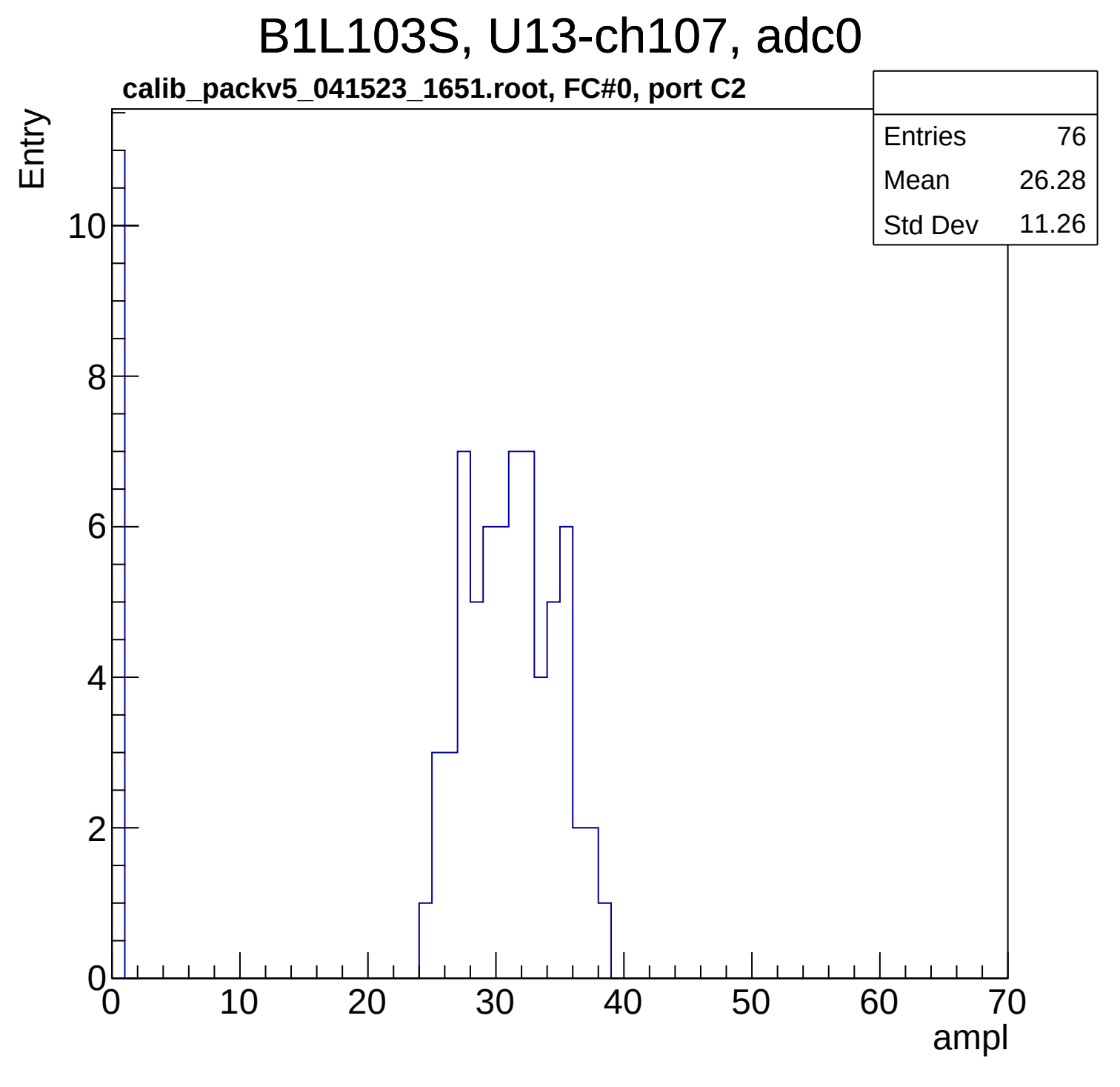
50
60
70
ampl


B1L103S, U13-ch107, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 26.28
Std Dev 11.26
Entry
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2
4
6
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10
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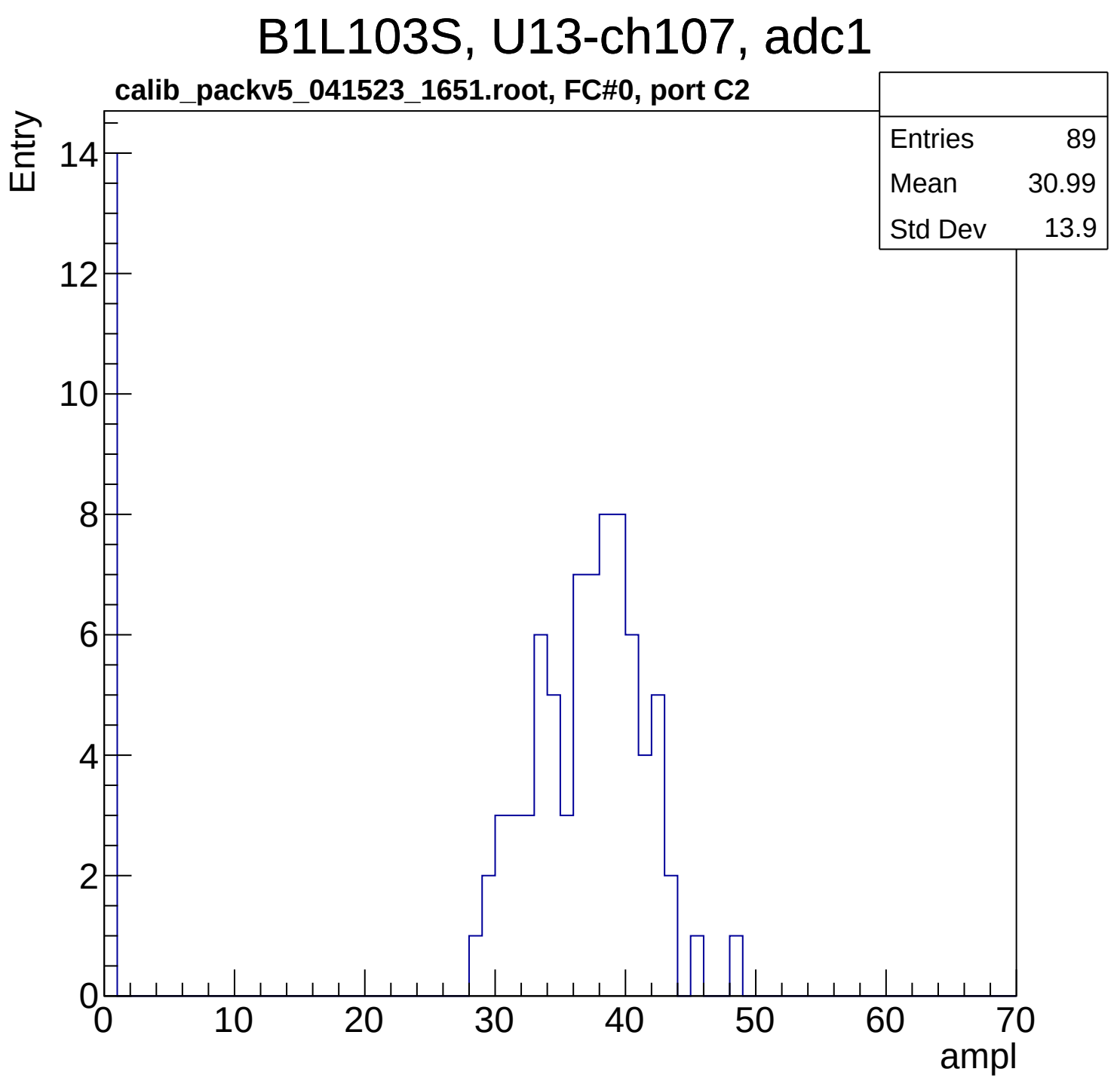
50
60
70
ampl


B1L103S, U13-ch107, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 30.99
Std Dev 13.9
Entry
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14
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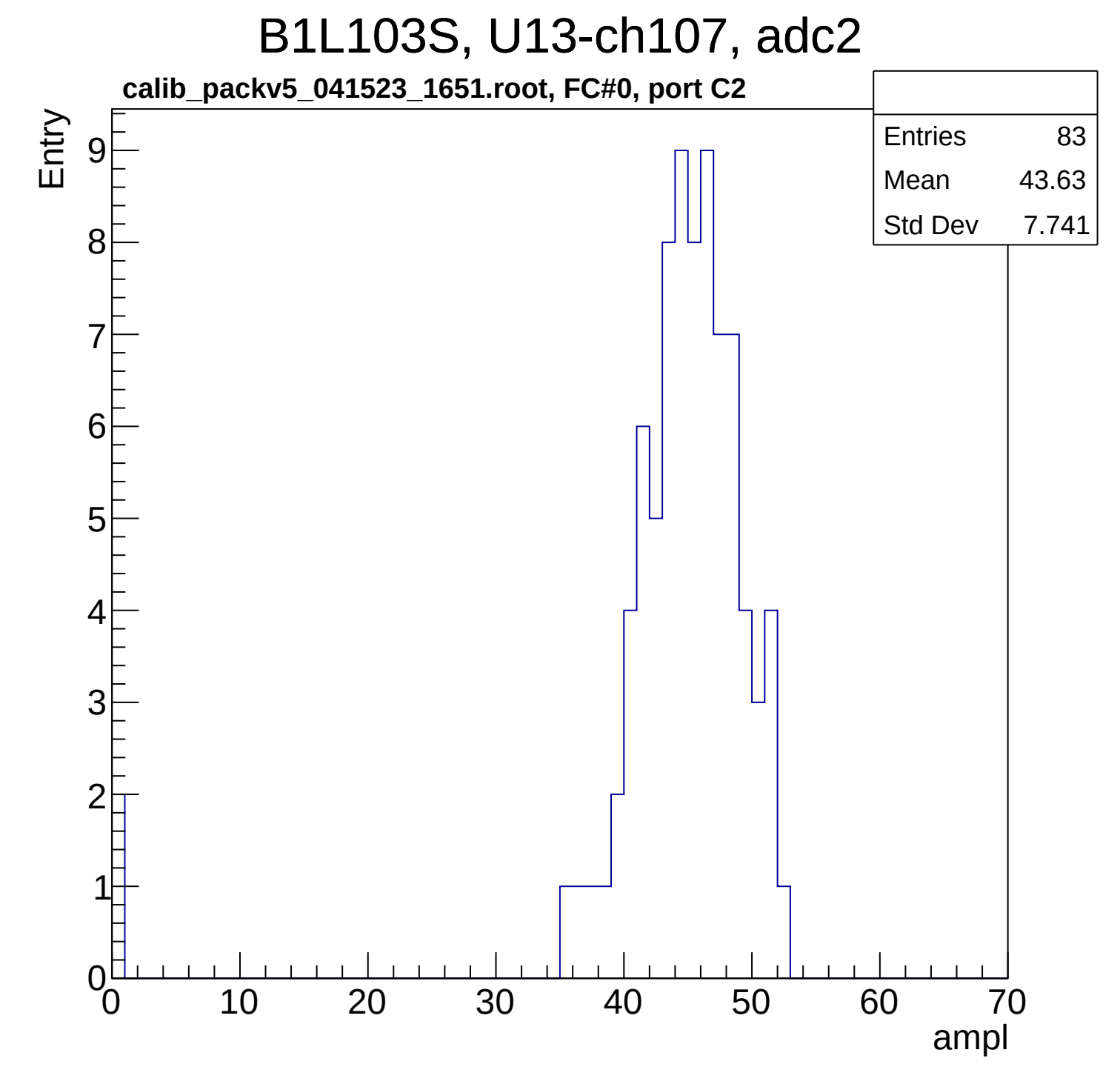
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch107, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 43.63
Std Dev 7.741
Entry
ampl
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3
4
5
6
7
8
9
0
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40
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60
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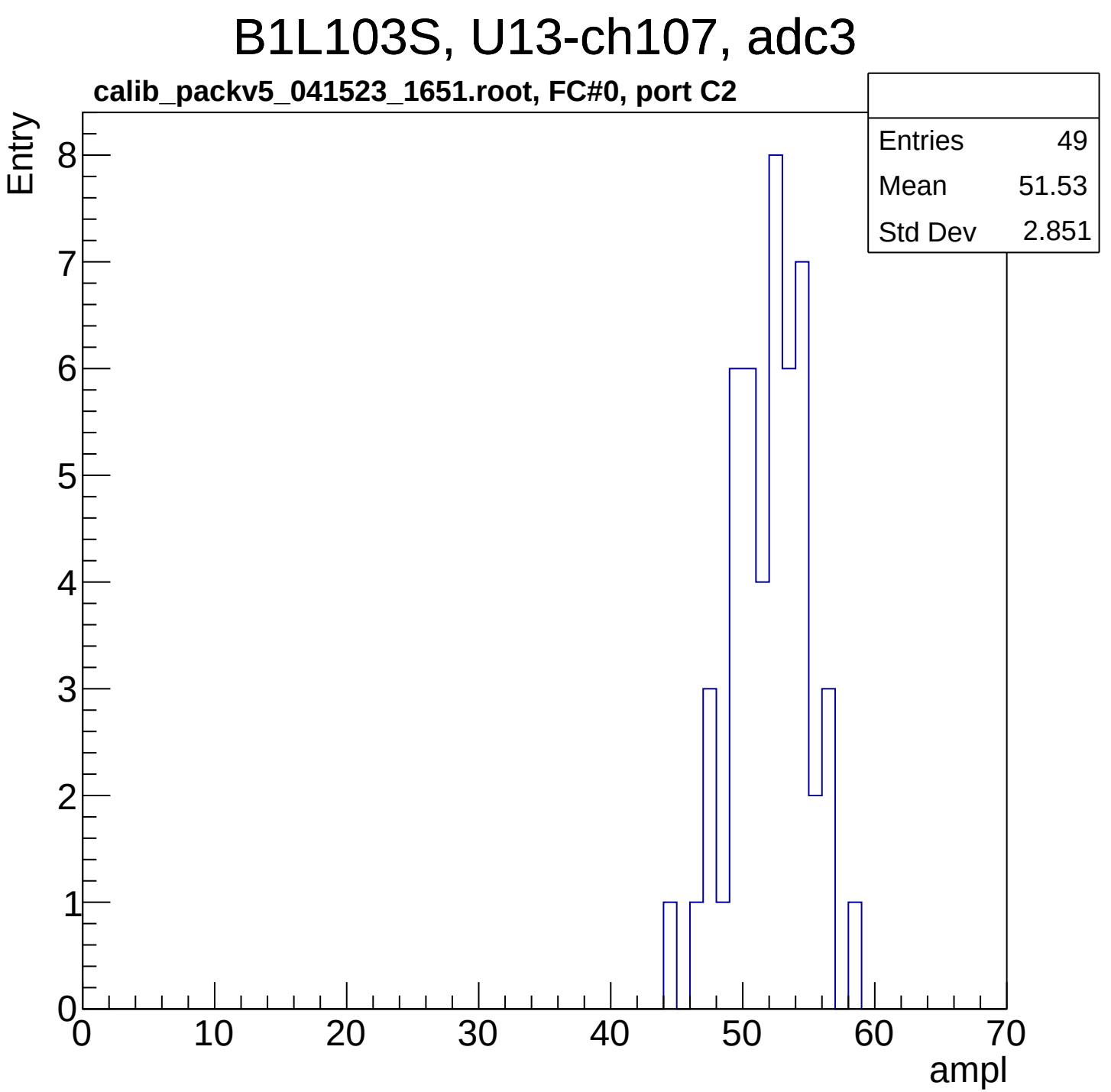
B1L103S, U13-ch107, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 51.53
Std Dev 2.851
Entry
ampl
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2
3
4
5
6
7
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0
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20
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60
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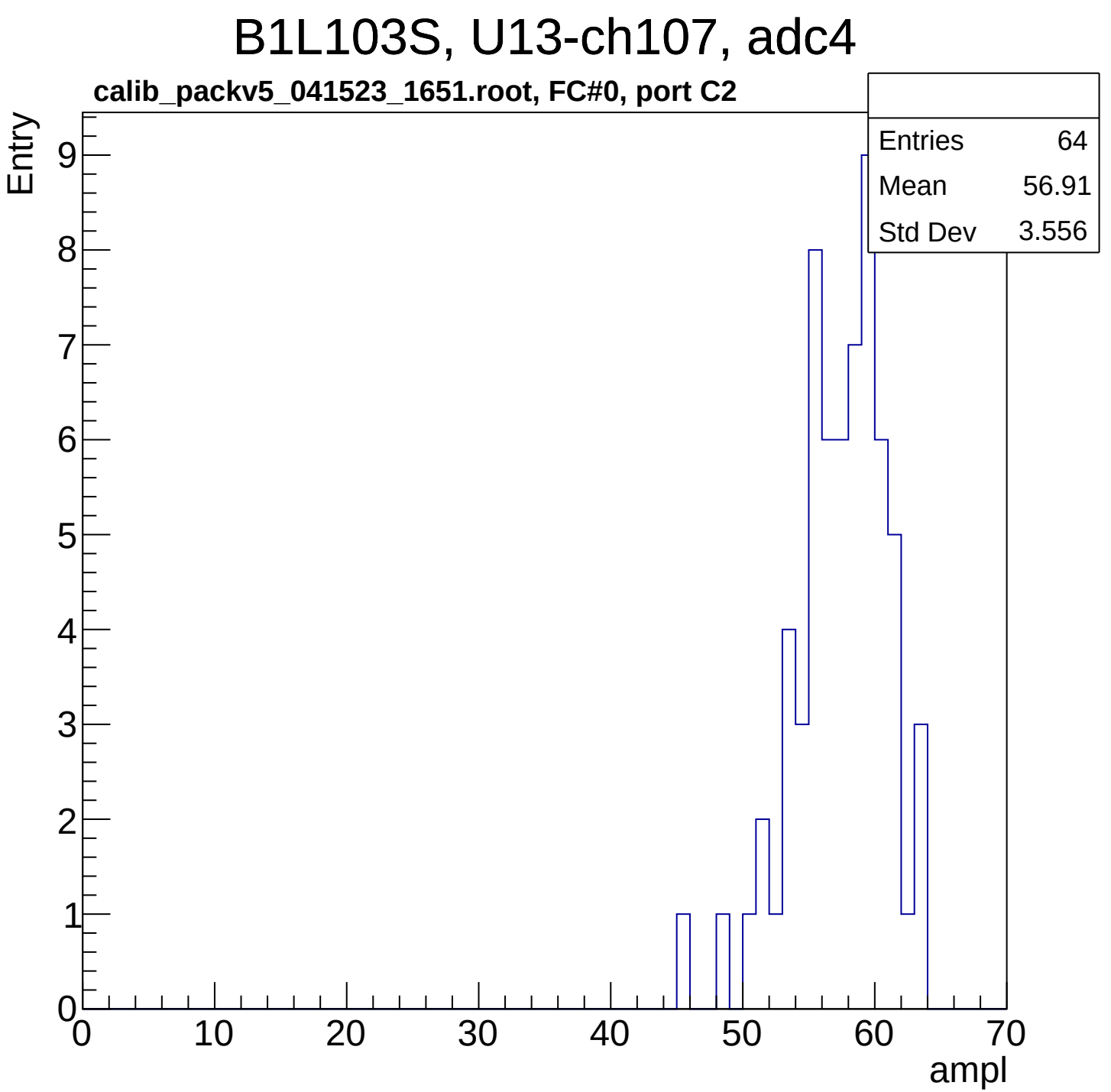
B1L103S, U13-ch107, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 56.91
Std Dev 3.556
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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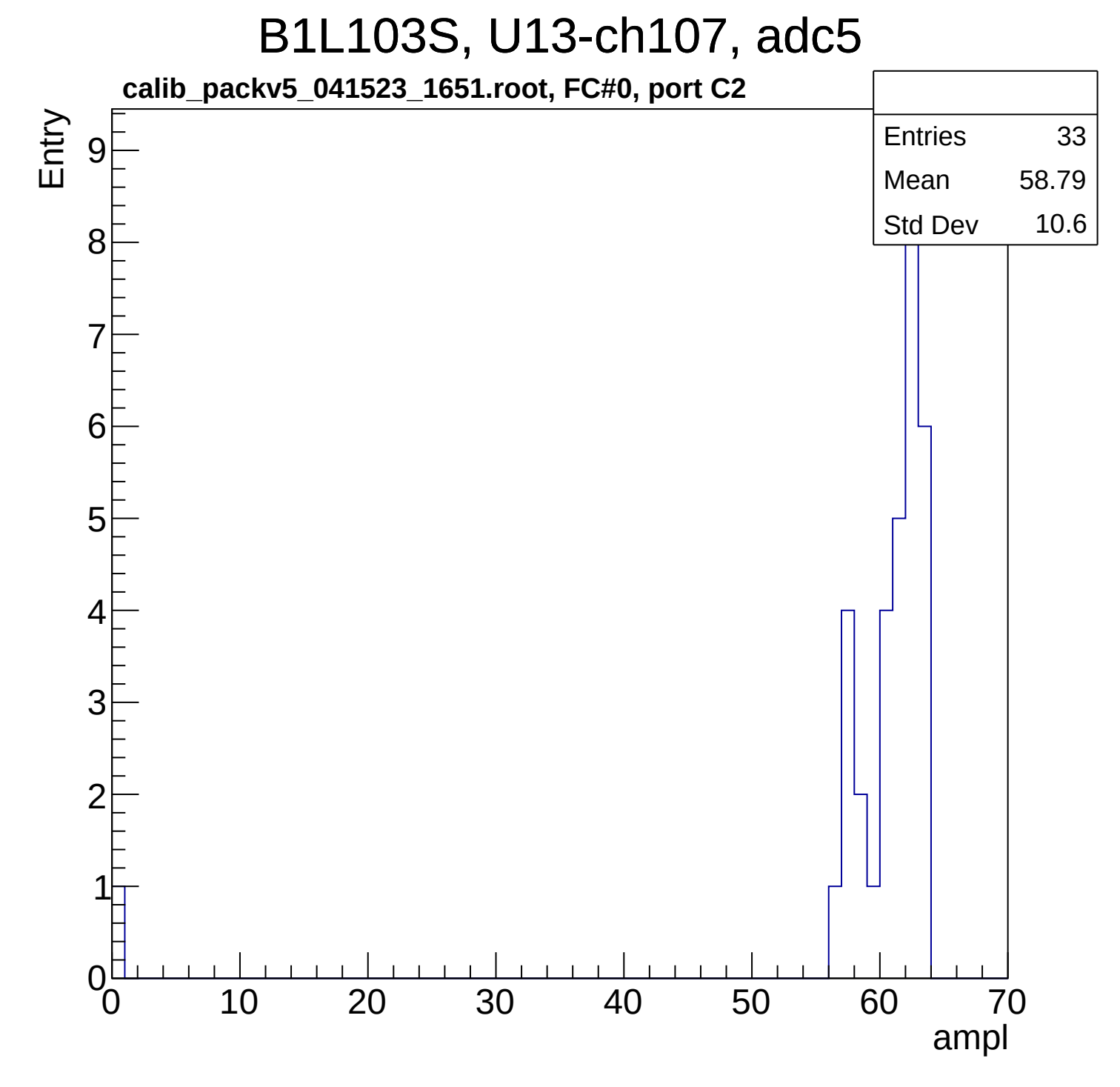
B1L103S, U13-ch107, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 58.79
Std Dev 10.6
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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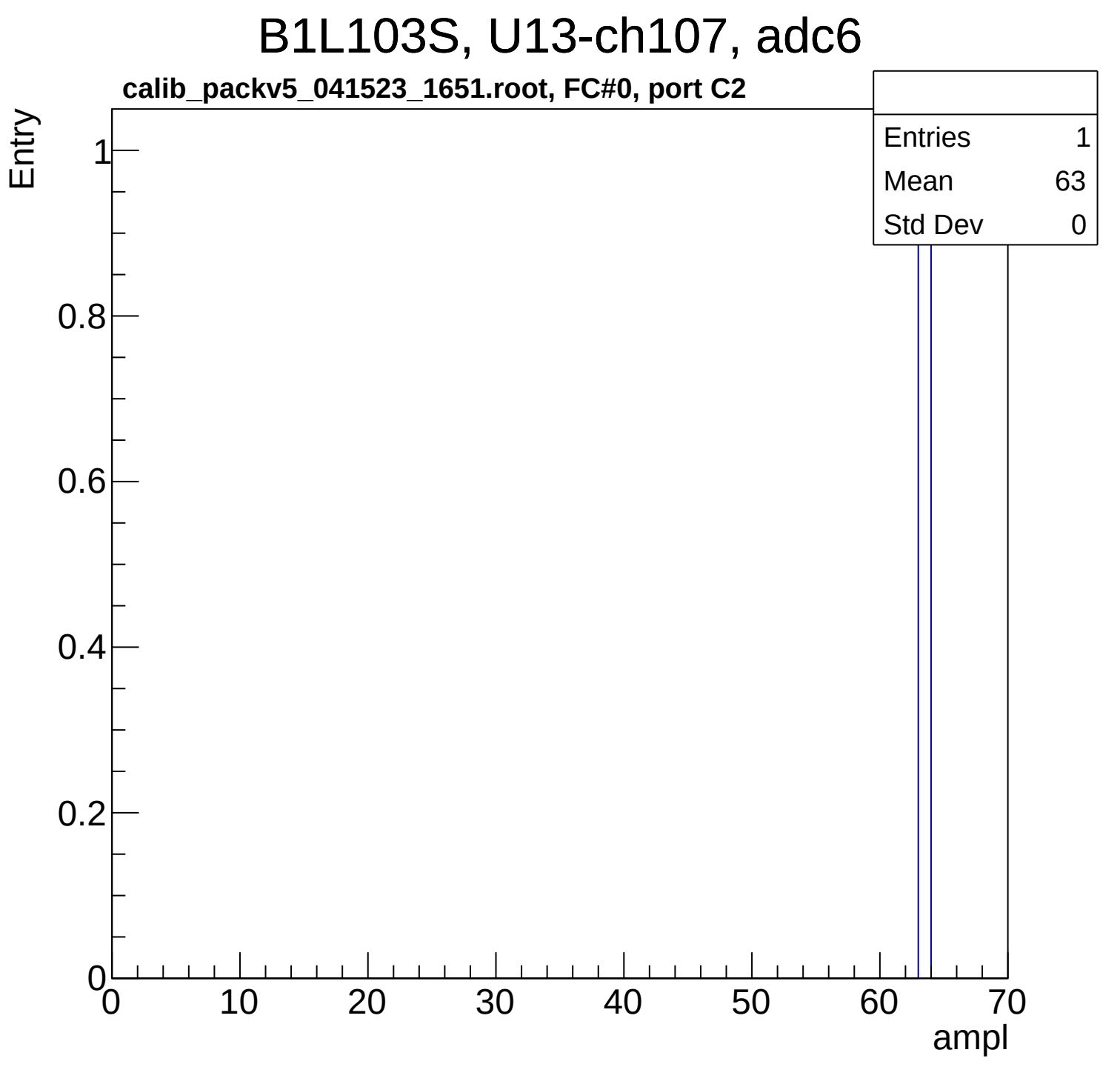
B1L103S, U13-ch107, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 63
Std Dev 0
Entry
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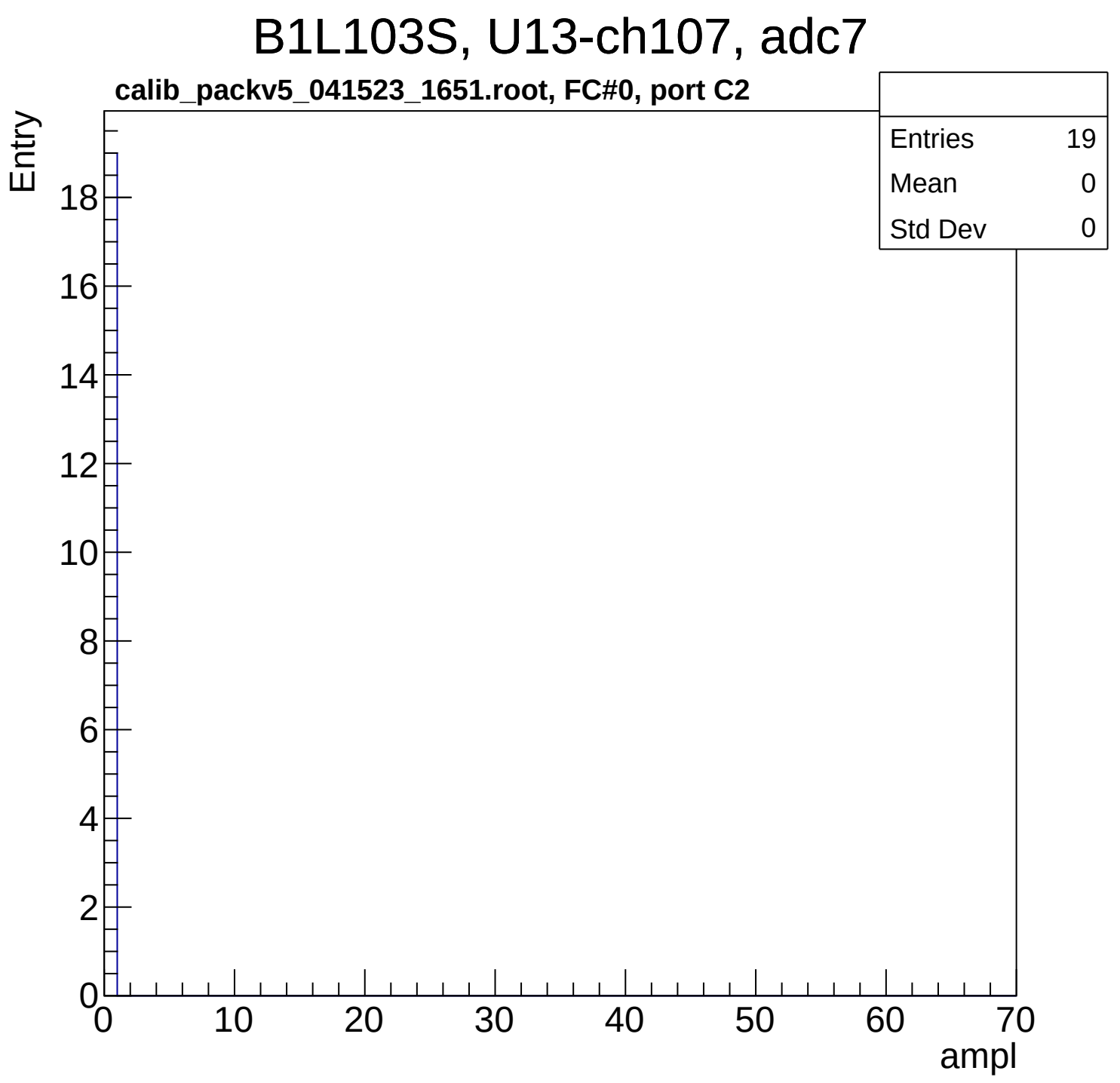
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch107, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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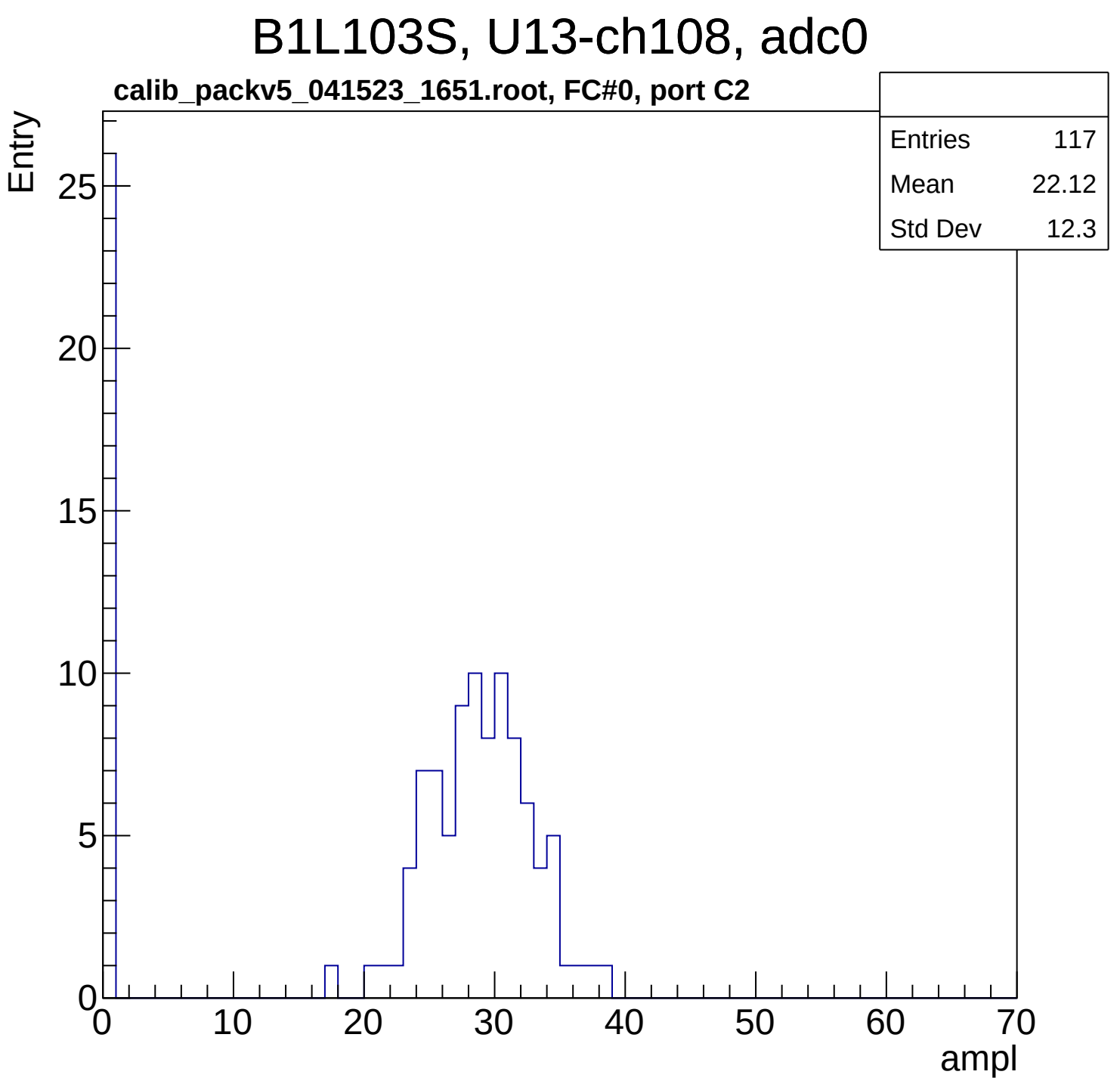
50
60
70
ampl


B1L103S, U13-ch108, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 117
Mean 22.12
Std Dev 12.3
Entry
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5
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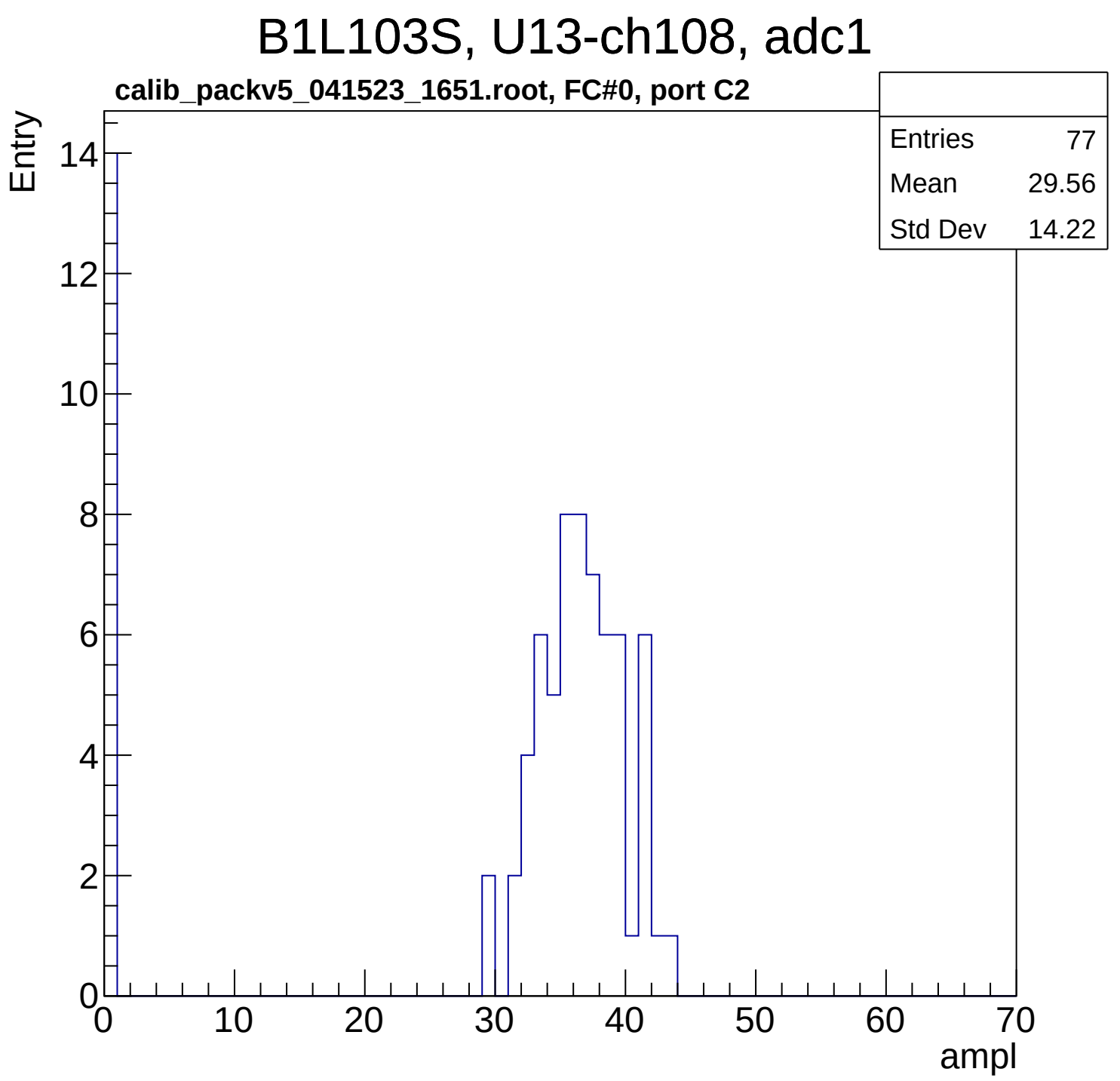
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch108, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 29.56
Std Dev 14.22
Entry
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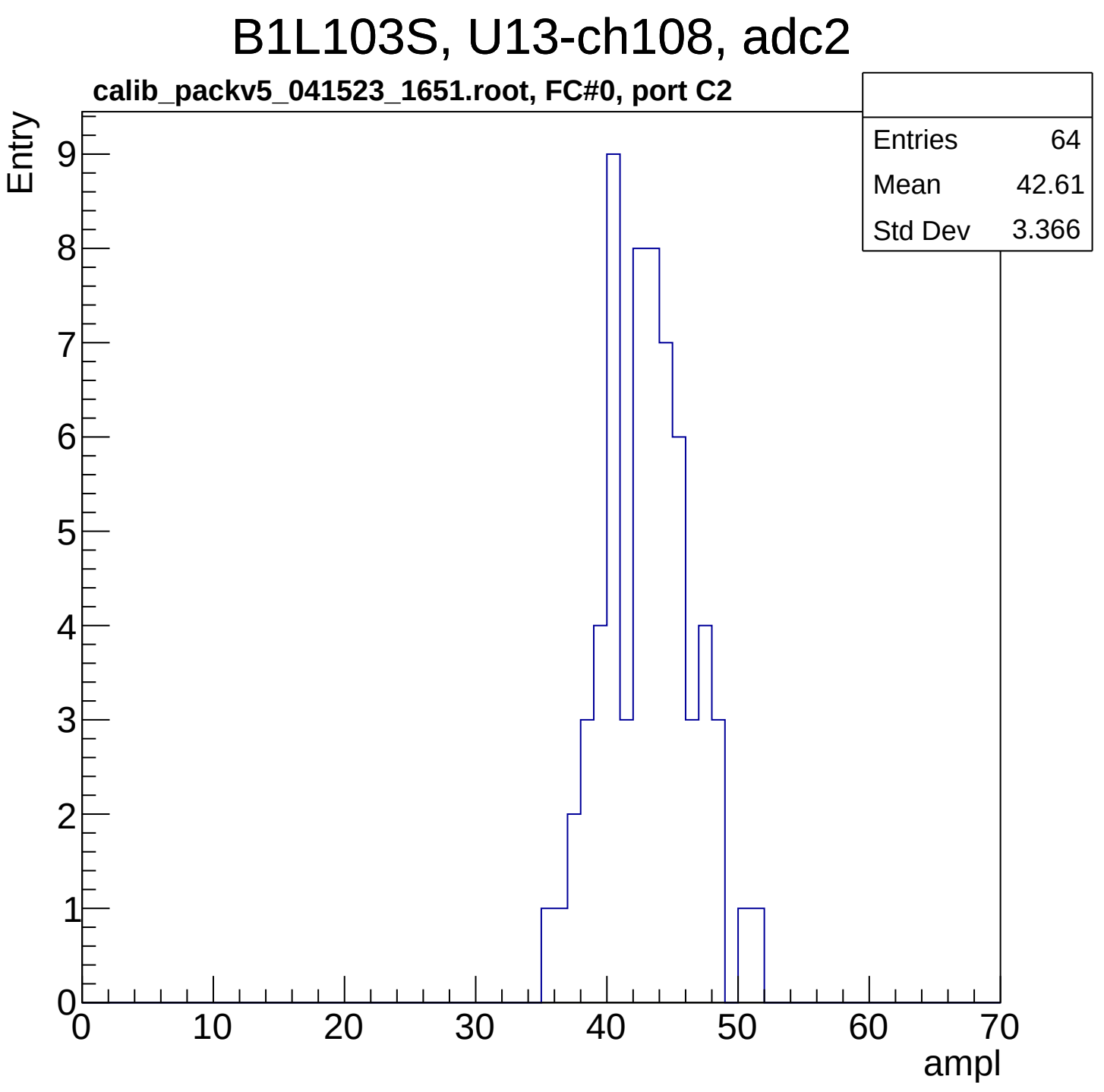
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch108, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 42.61
Std Dev 3.366
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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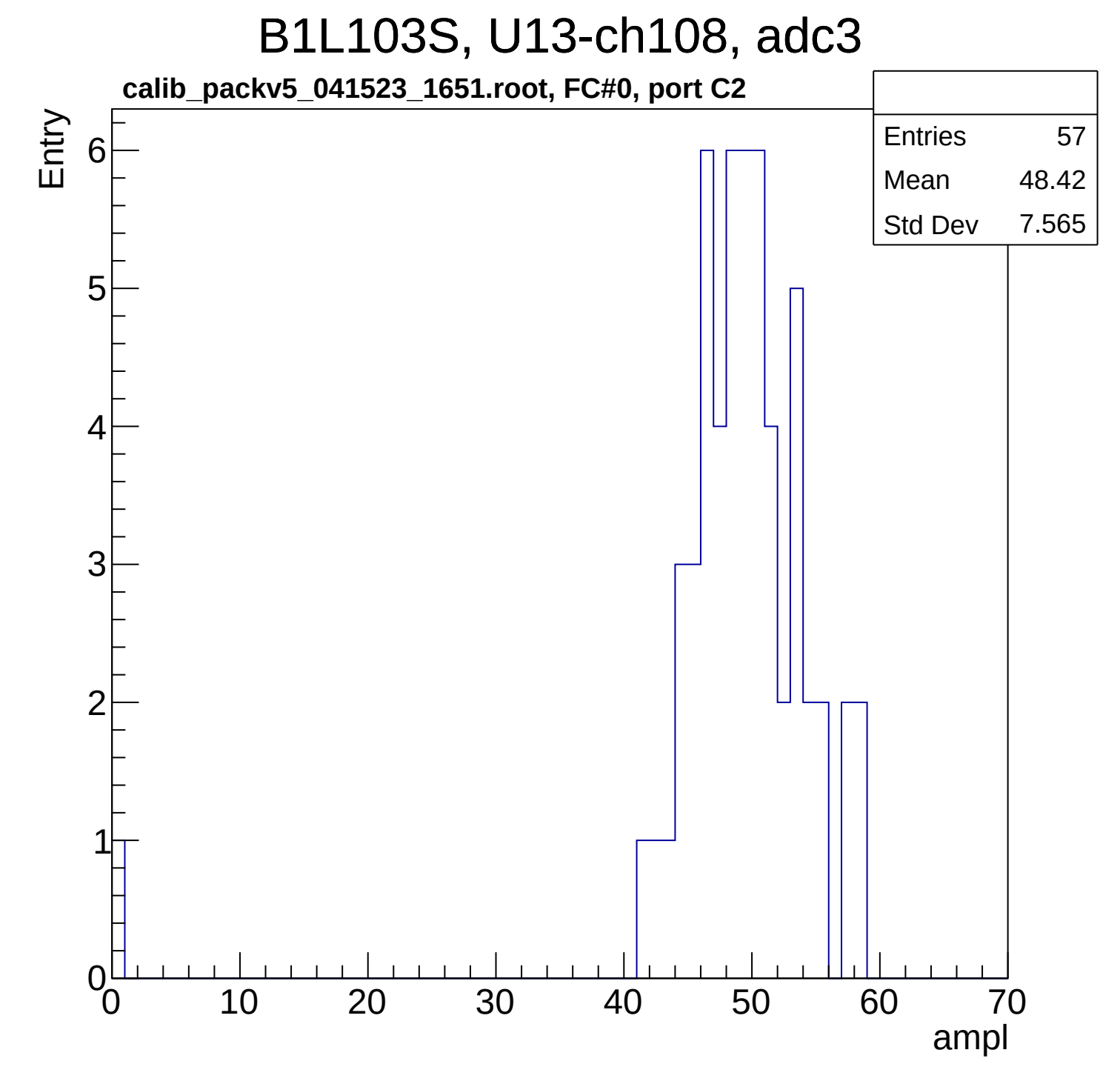
B1L103S, U13-ch108, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 48.42
Std Dev 7.565
Entry
ampl
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2
3
4
5
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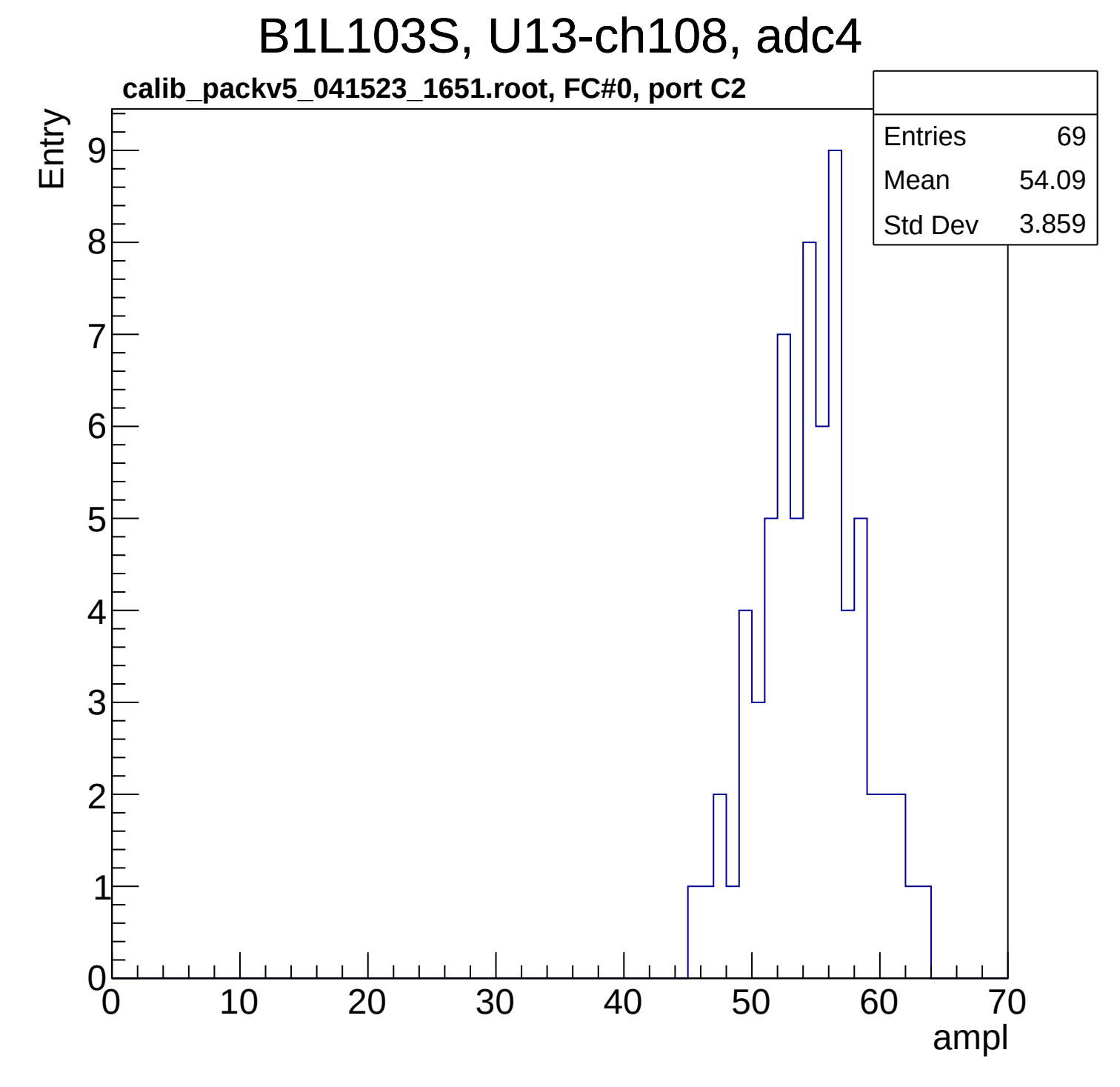
0
10
20
30
40
50
60
70


B1L103S, U13-ch108, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 54.09
Std Dev 3.859
Entry
ampl
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3
4
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6
7
8
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0
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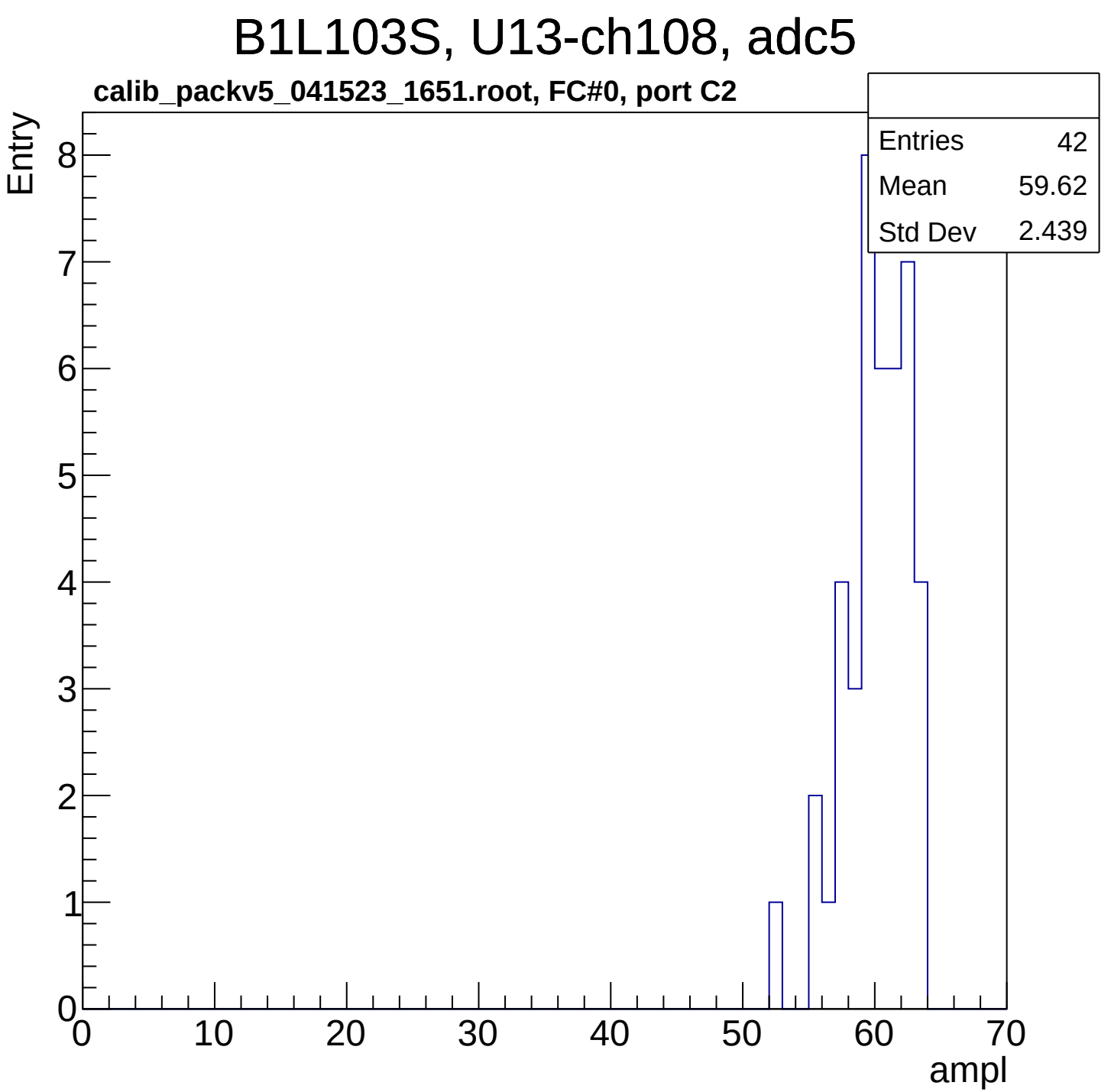
B1L103S, U13-ch108, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 59.62
Std Dev 2.439
Entry
ampl
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60
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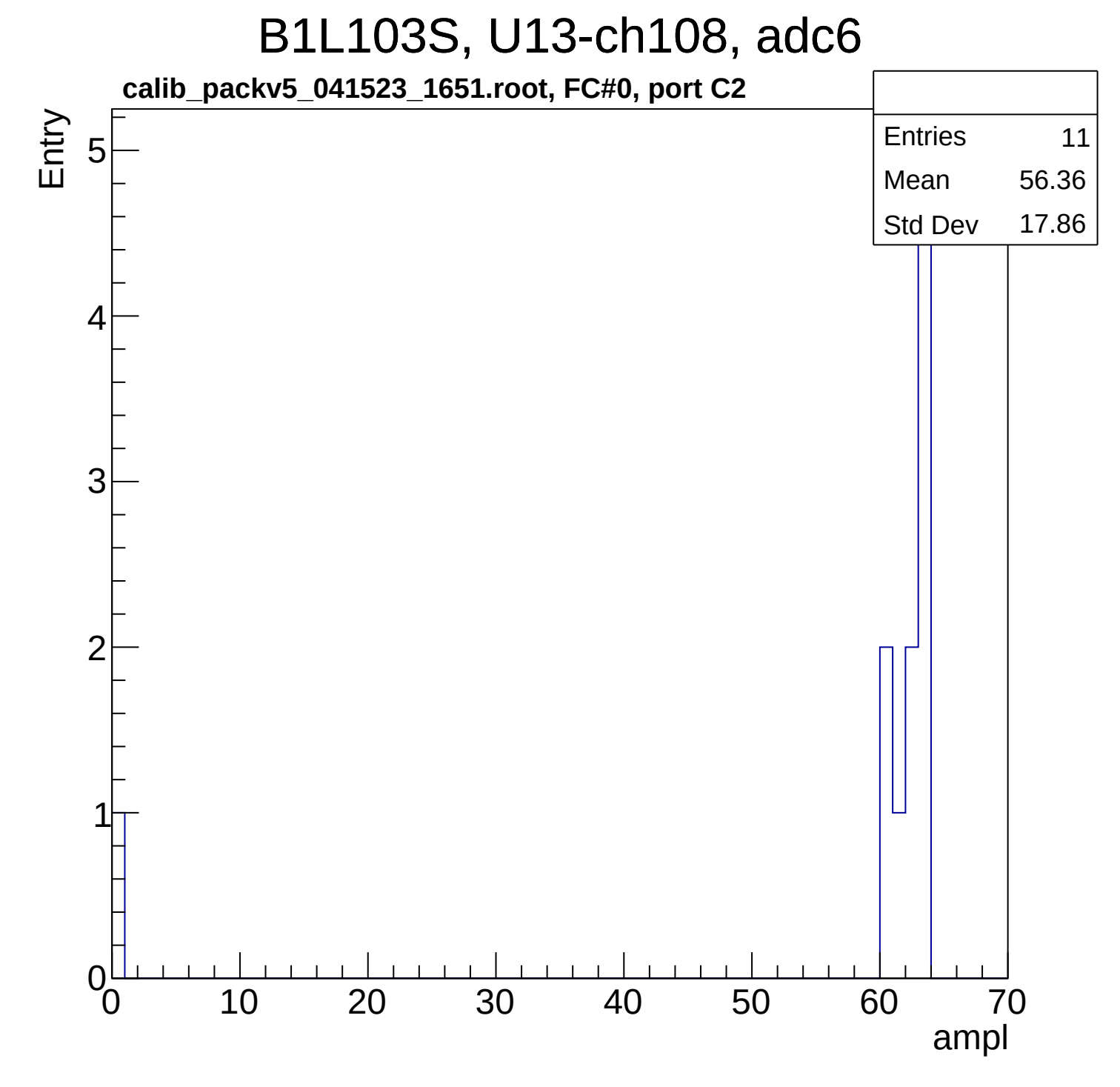
B1L103S, U13-ch108, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 56.36
Std Dev 17.86
Entry
ampl
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40
50
60
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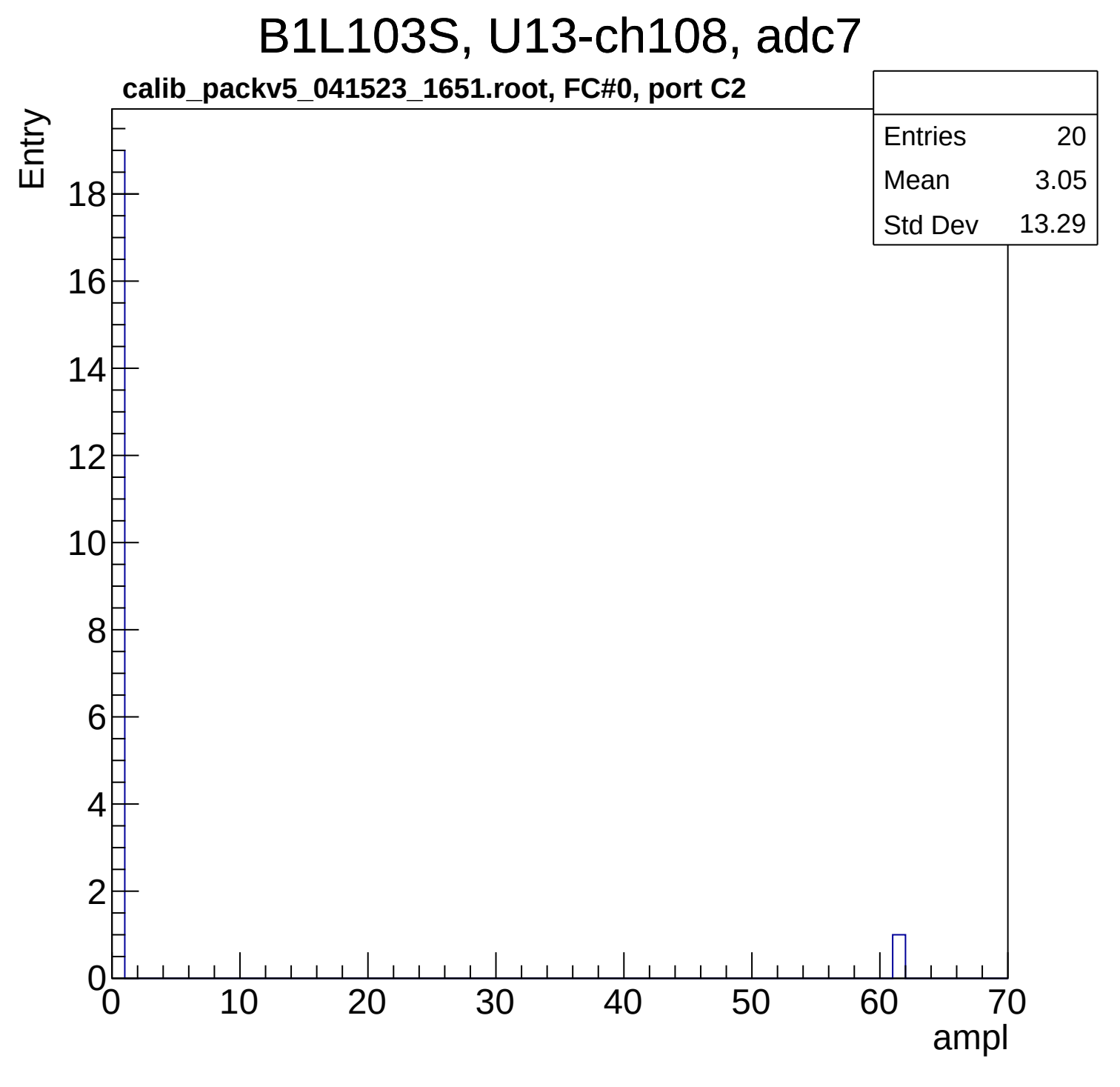
B1L103S, U13-ch108, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
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6
8
10
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14
16
18
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10
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50
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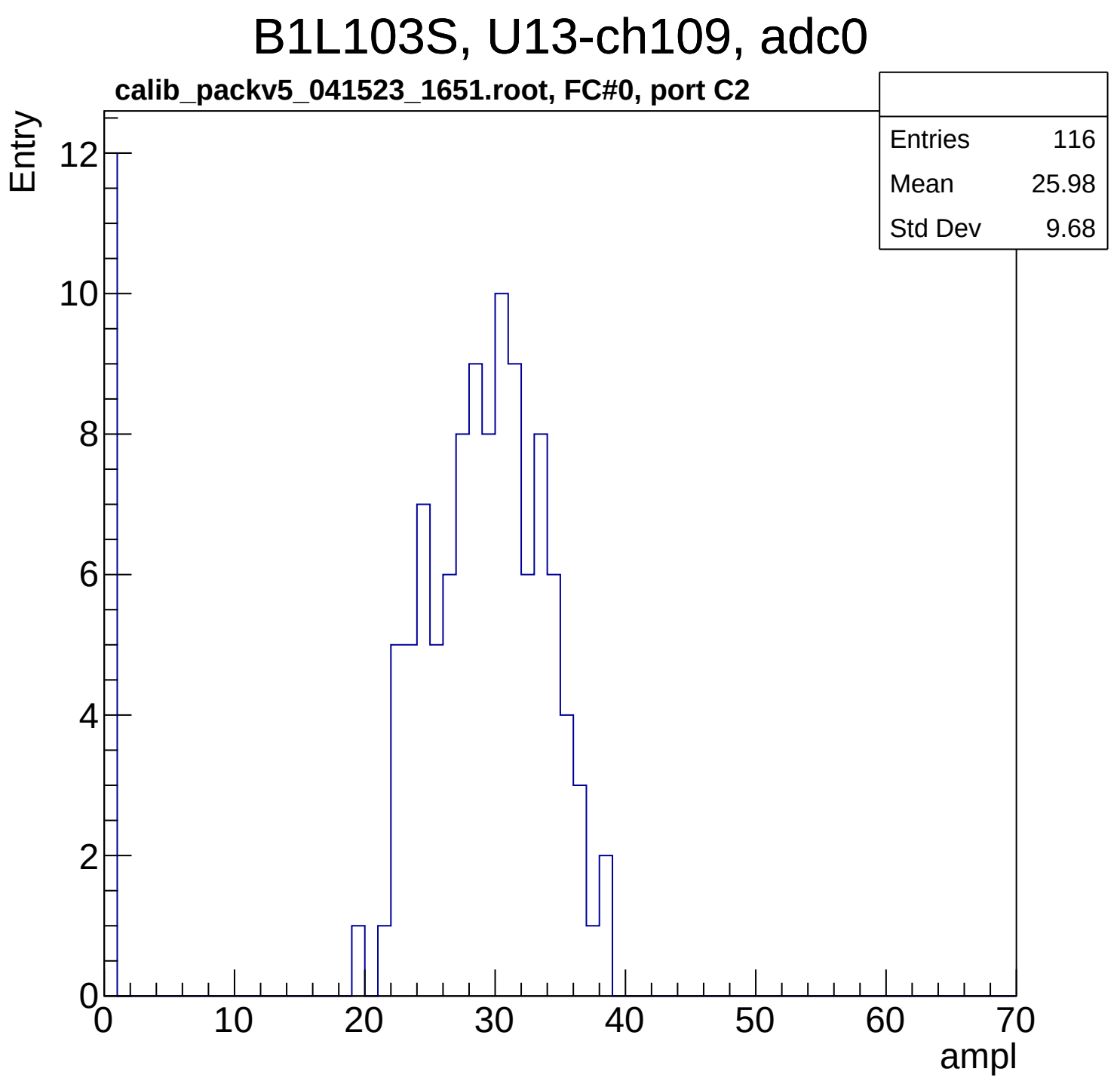
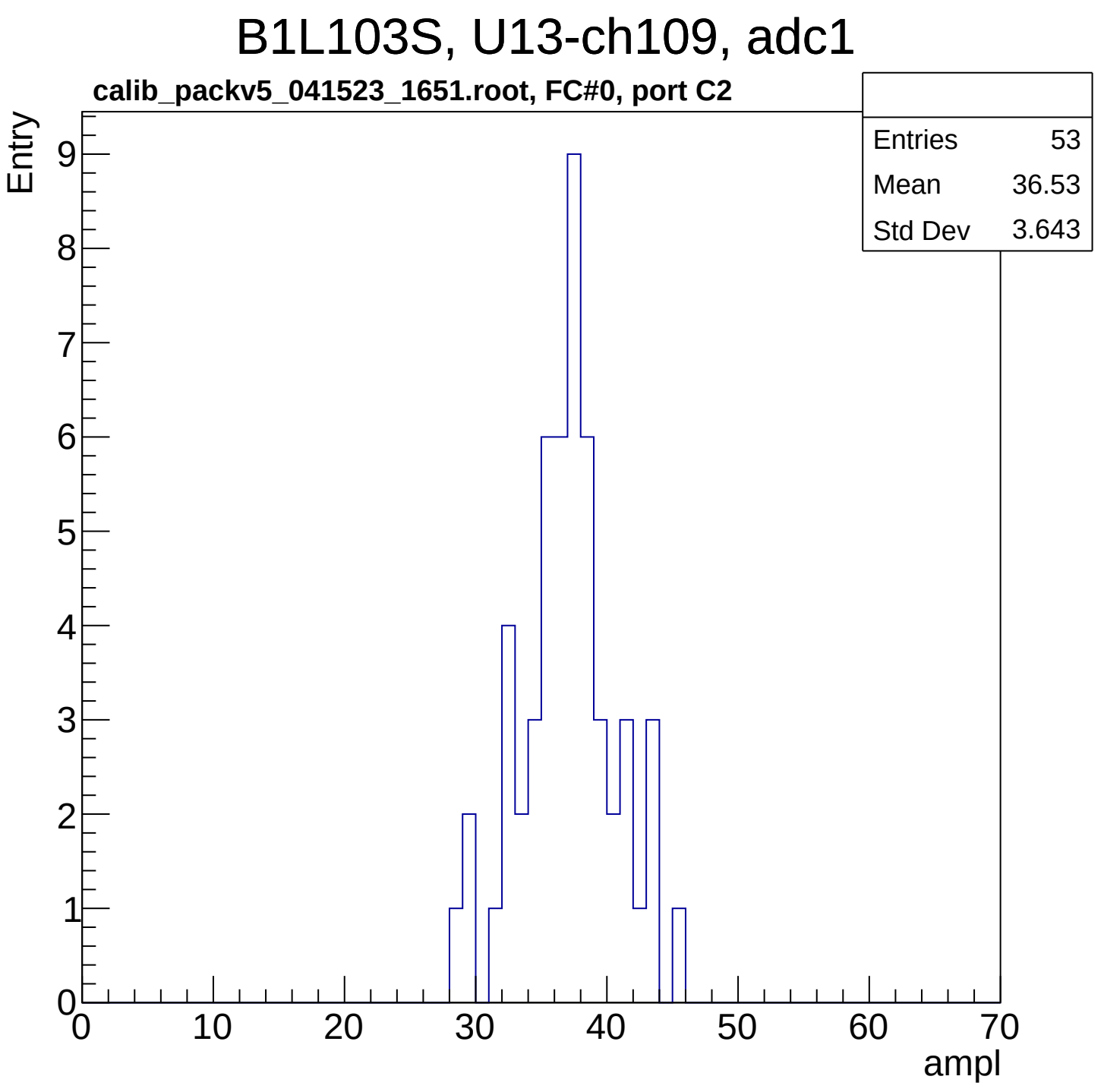
70
ampl


B1L103S, U13-ch109, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 116
Mean 25.98
Std Dev 9.68
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch109, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 36.53
Std Dev 3.643
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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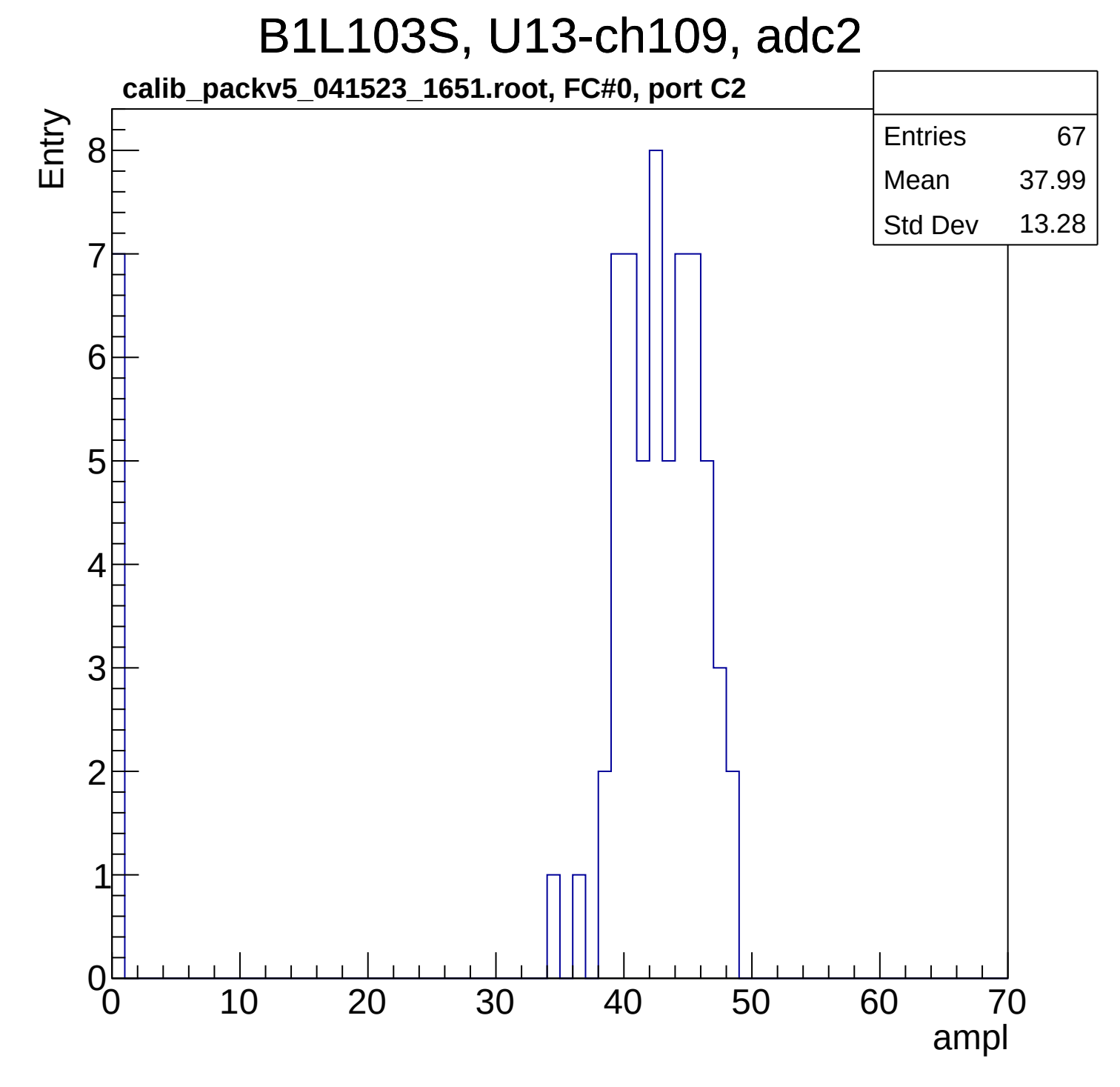
B1L103S, U13-ch109, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 37.99
Std Dev 13.28
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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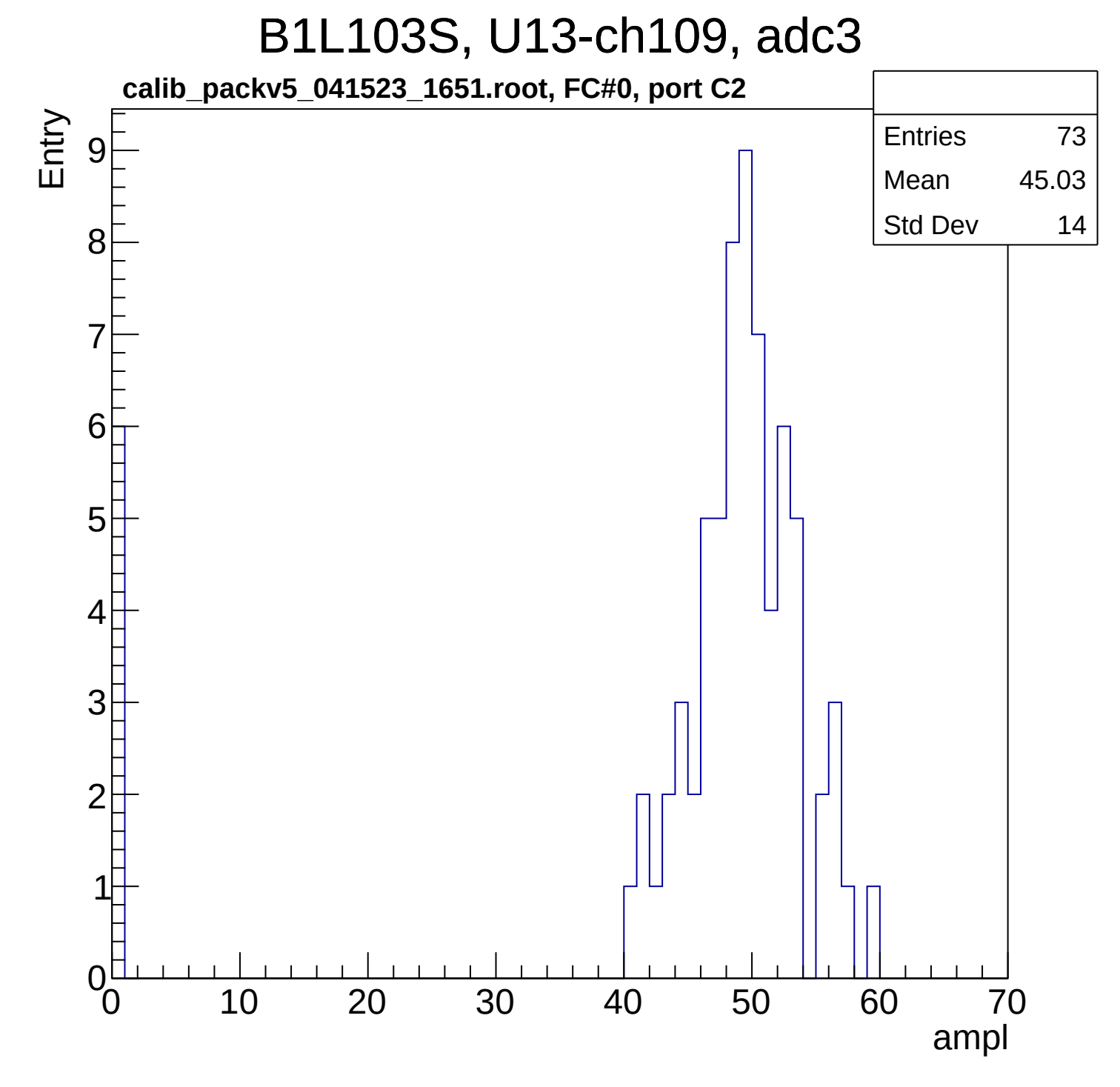
B1L103S, U13-ch109, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 45.03
Std Dev 14
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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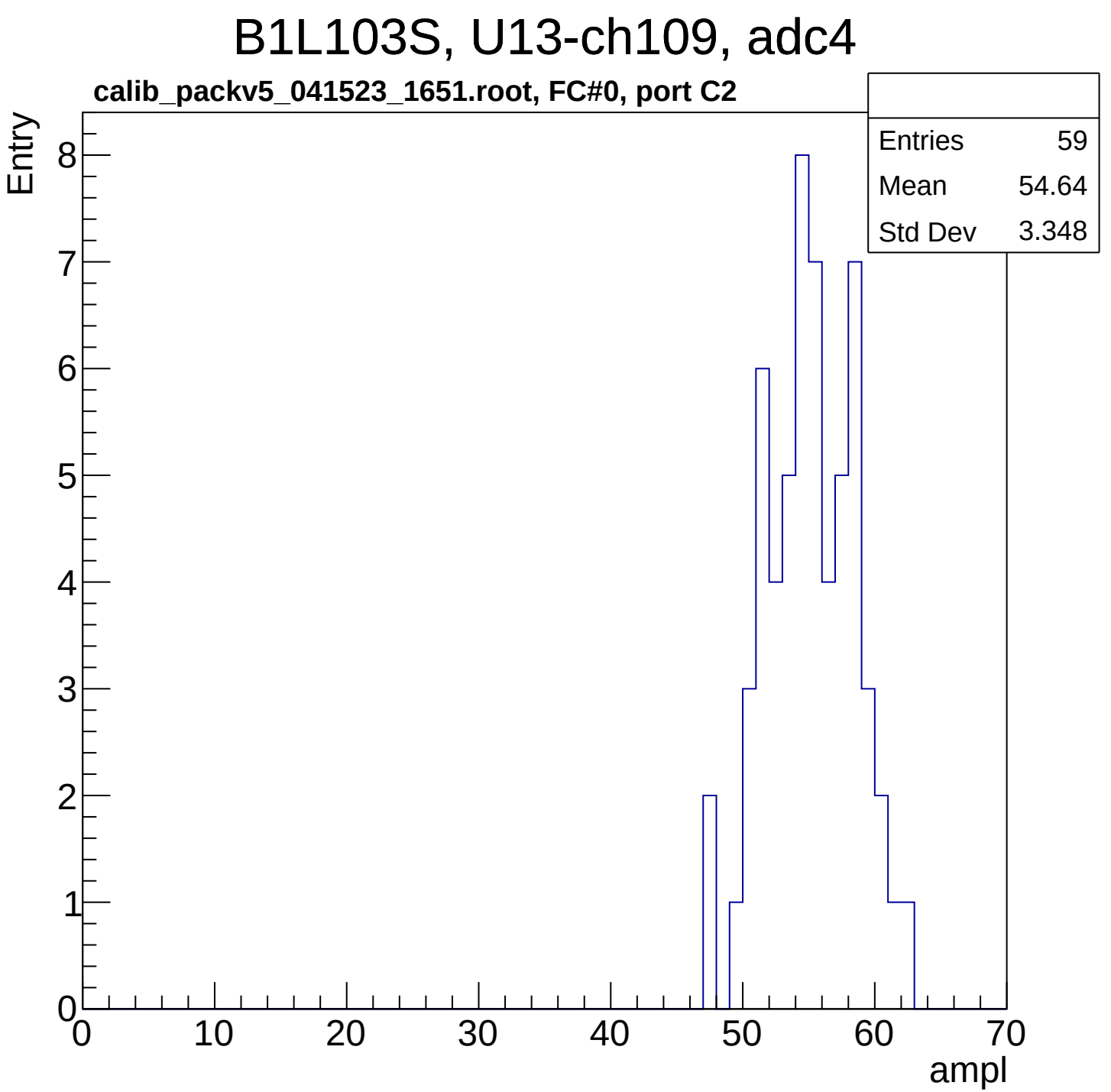
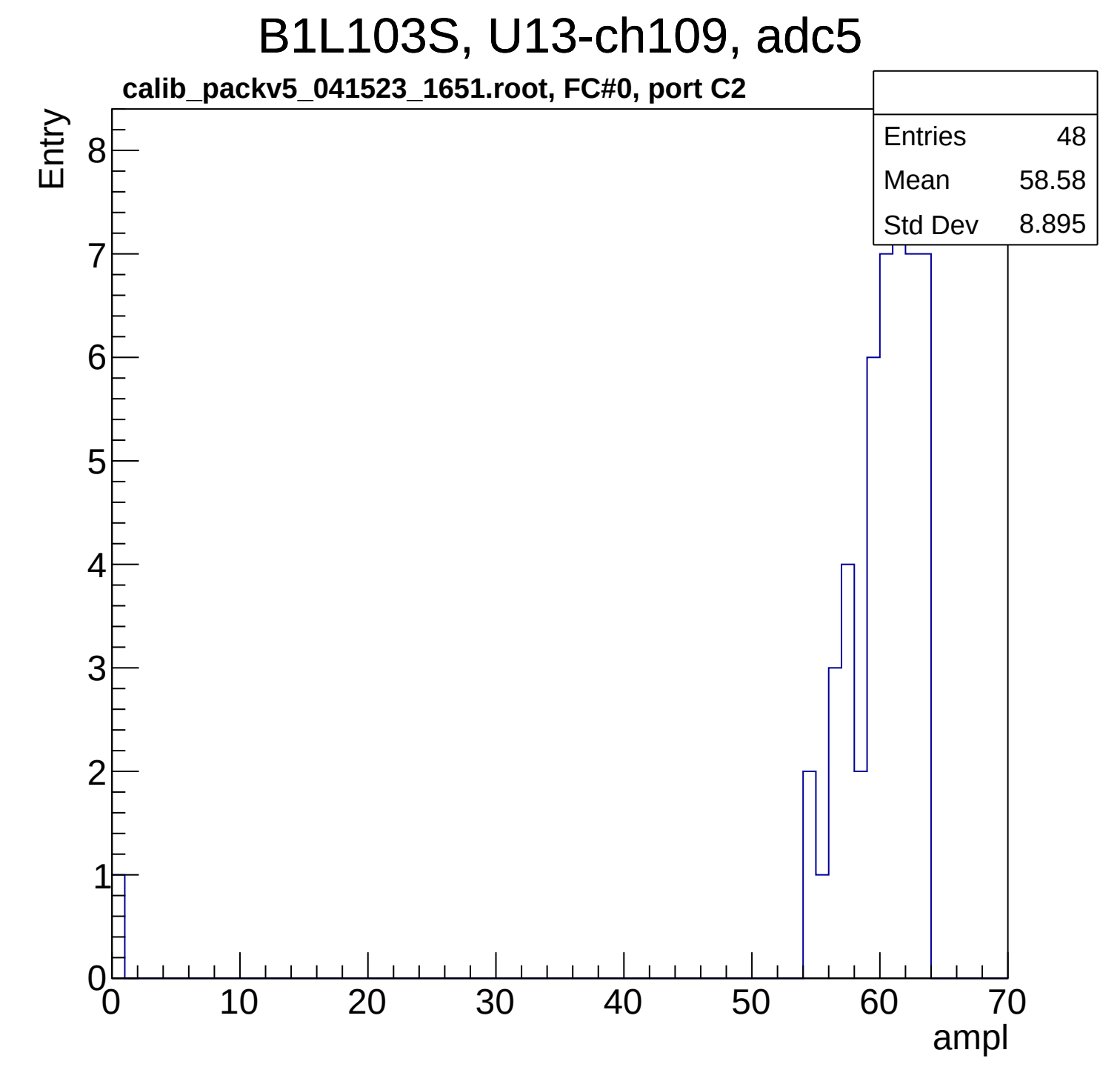
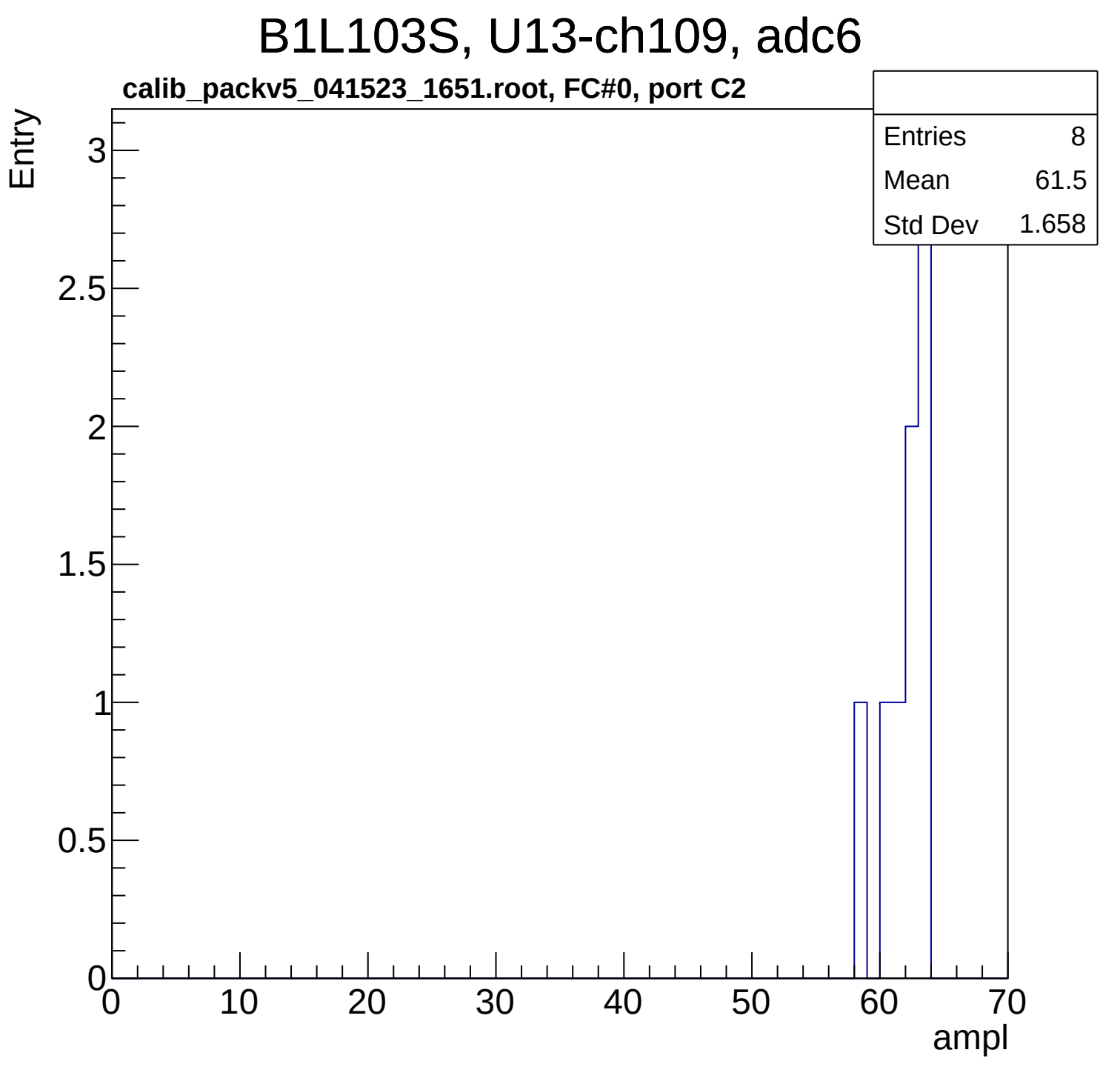
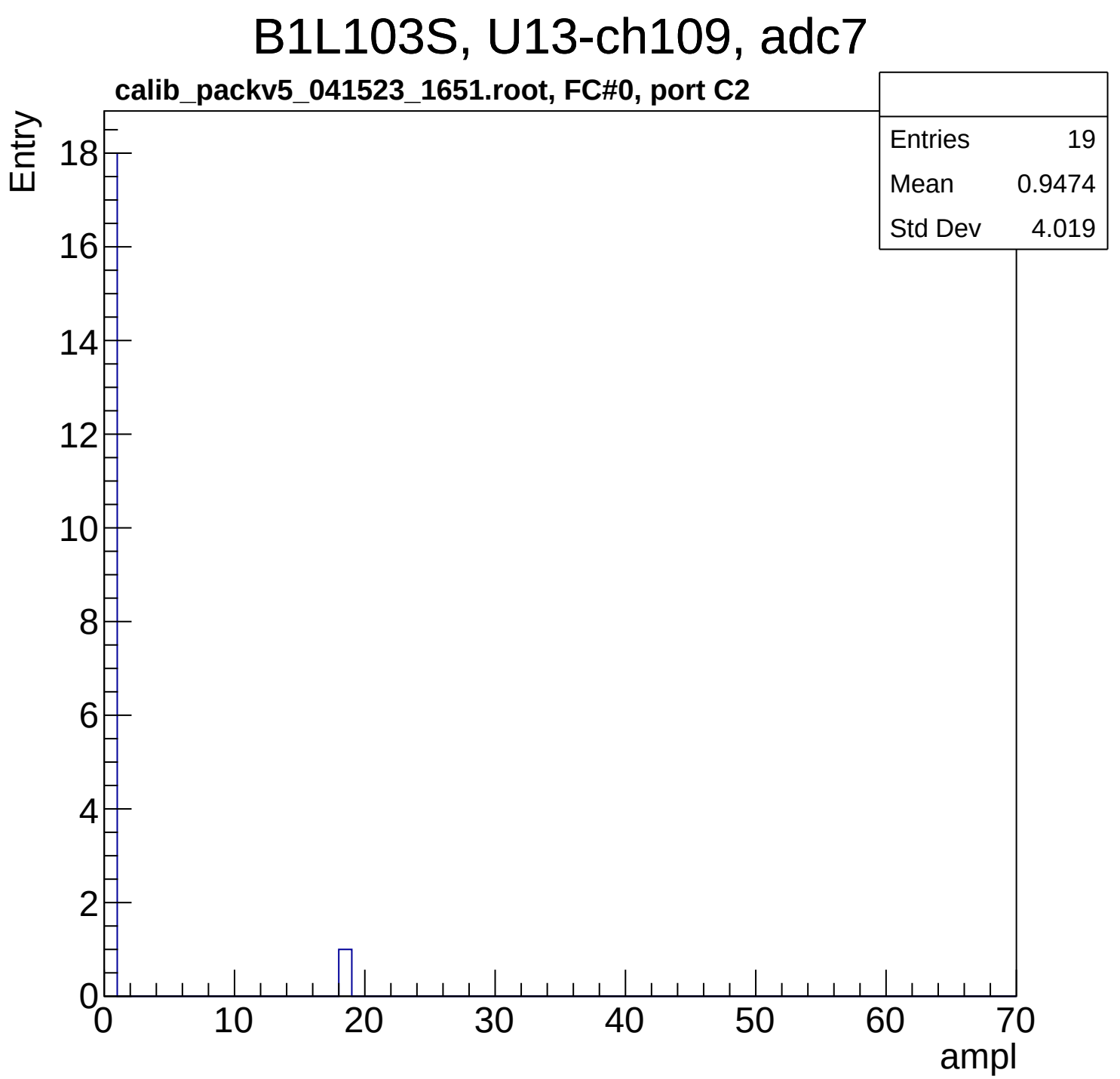
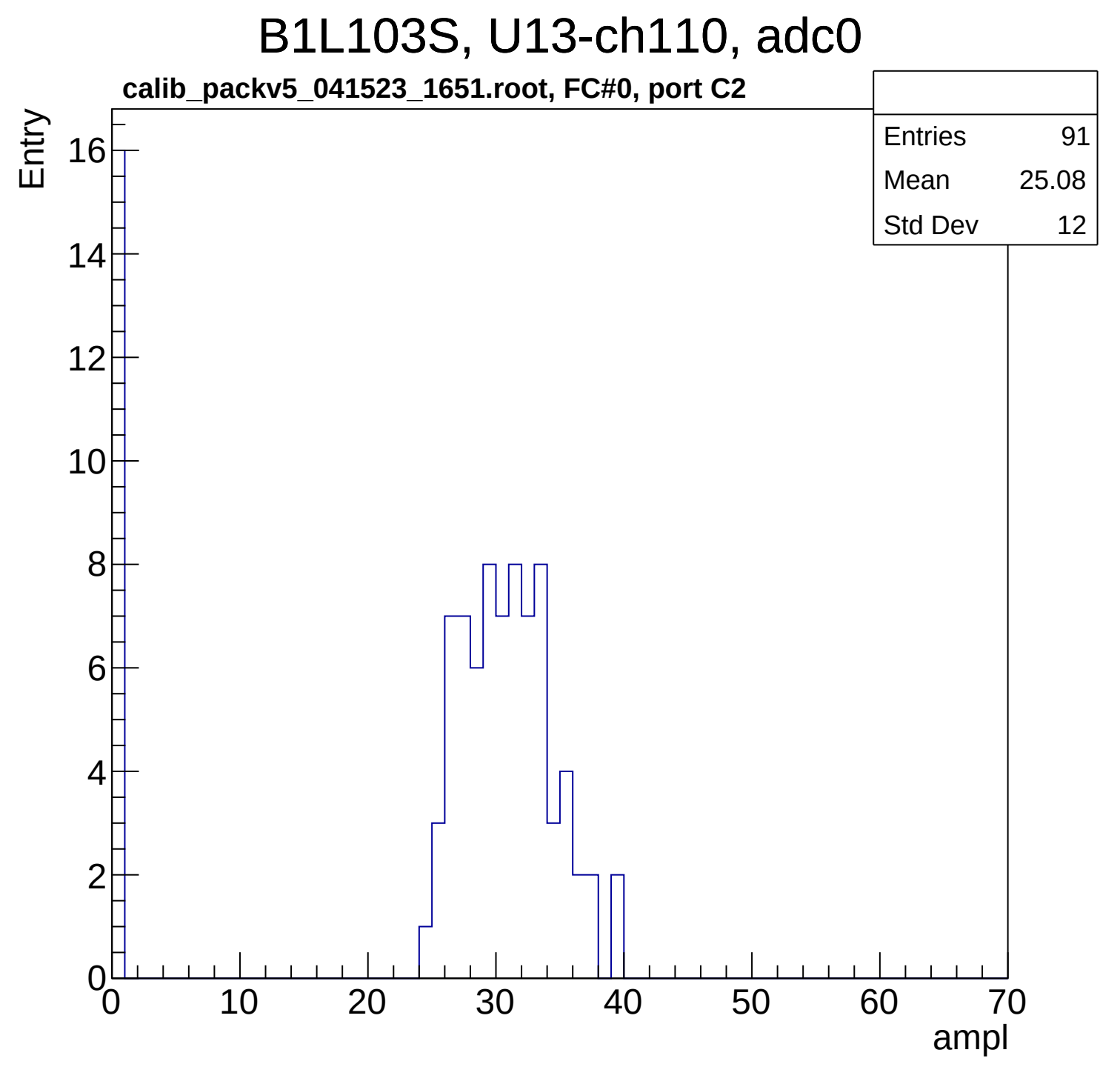

B1L103S, U13-ch109, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.64
Std Dev 3.348
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch109, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.58
Std Dev 8.895
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch109, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.5
Std Dev 1.658
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U13-ch109, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0.9474
Std Dev 4.019
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch110, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 25.08
Std Dev 12
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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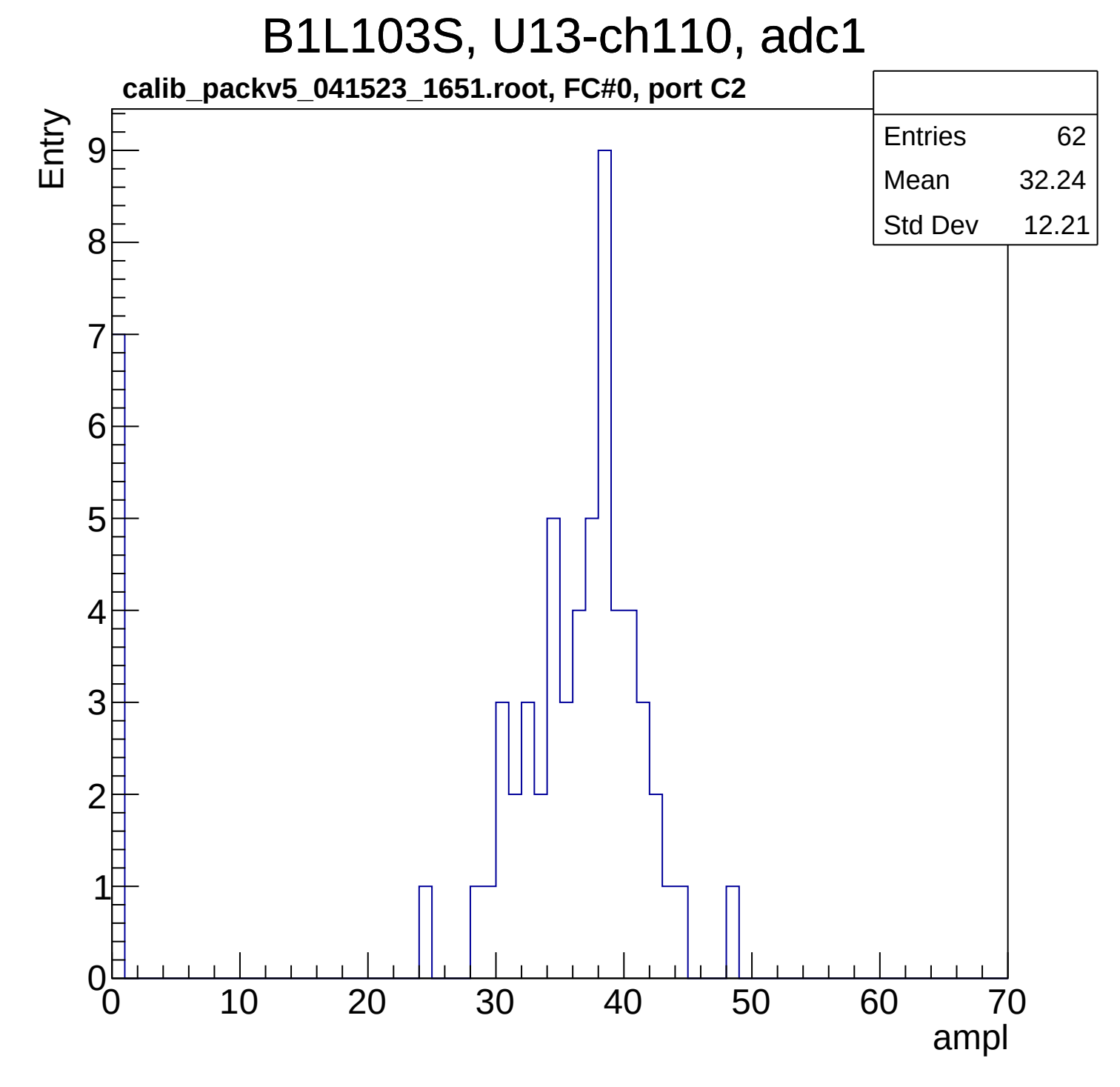
B1L103S, U13-ch110, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 32.24
Std Dev 12.21
Entry
ampl
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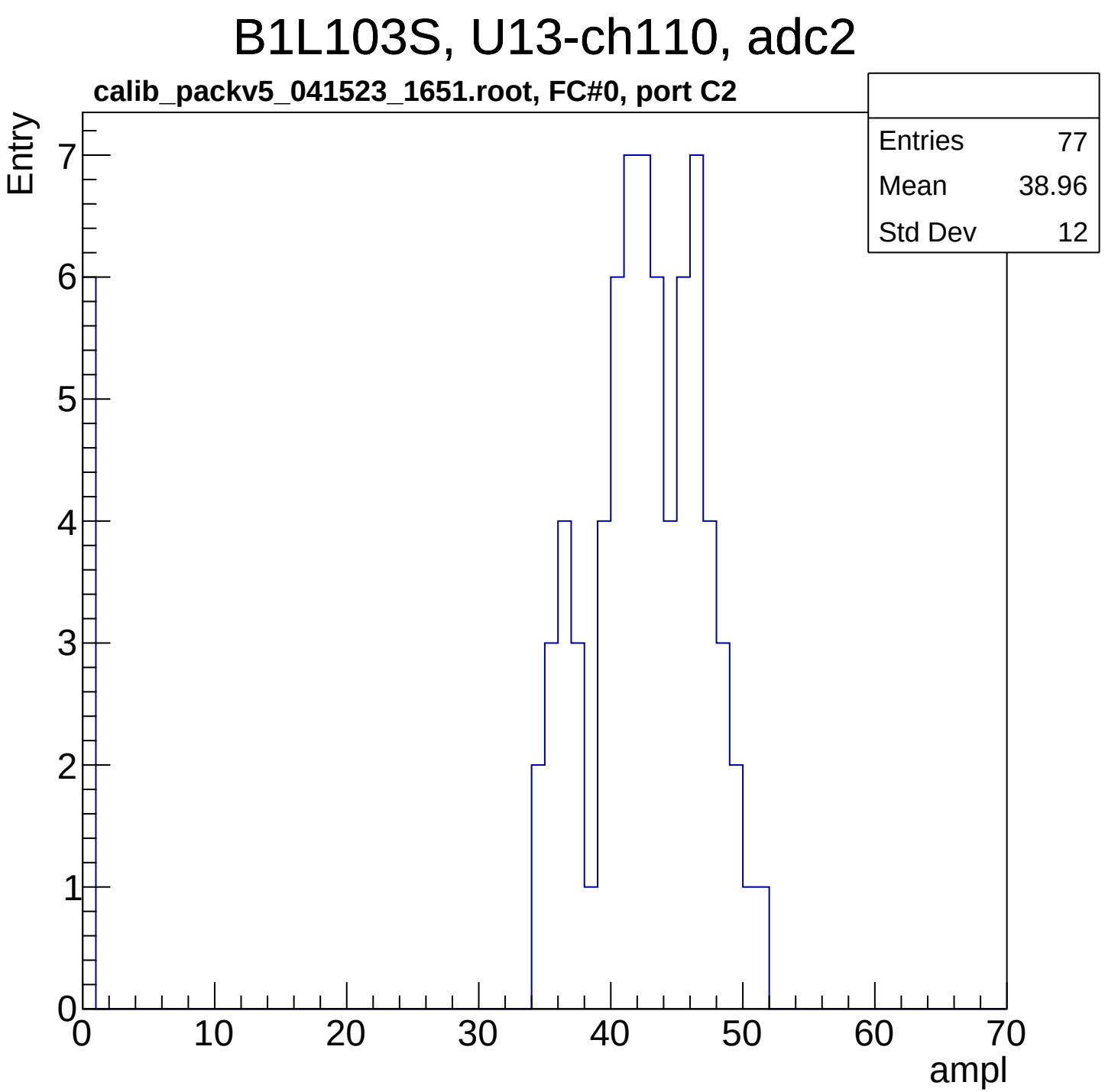
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch110, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 38.96
Std Dev 12
Entry
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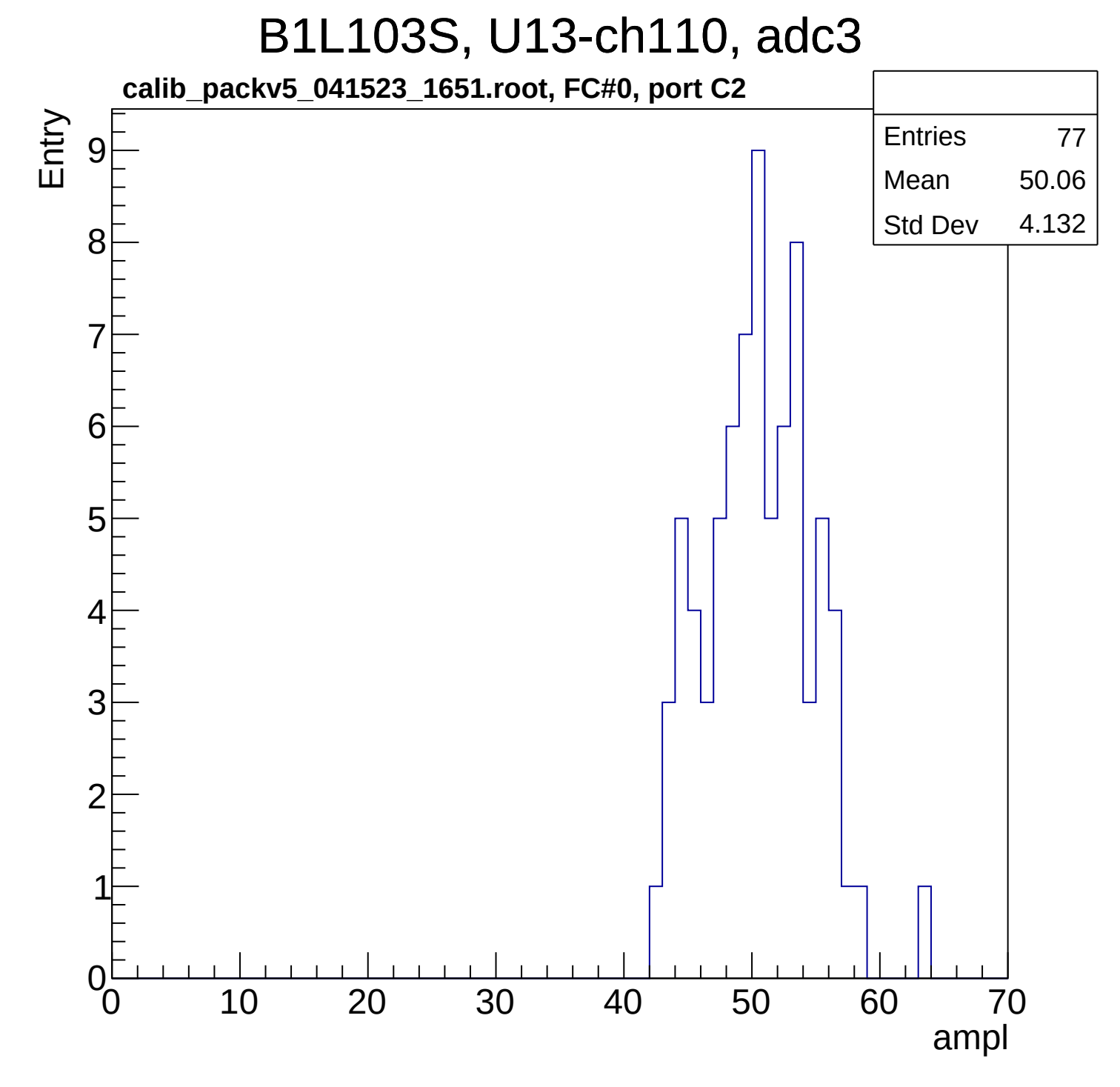
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch110, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 50.06
Std Dev 4.132
Entry
ampl
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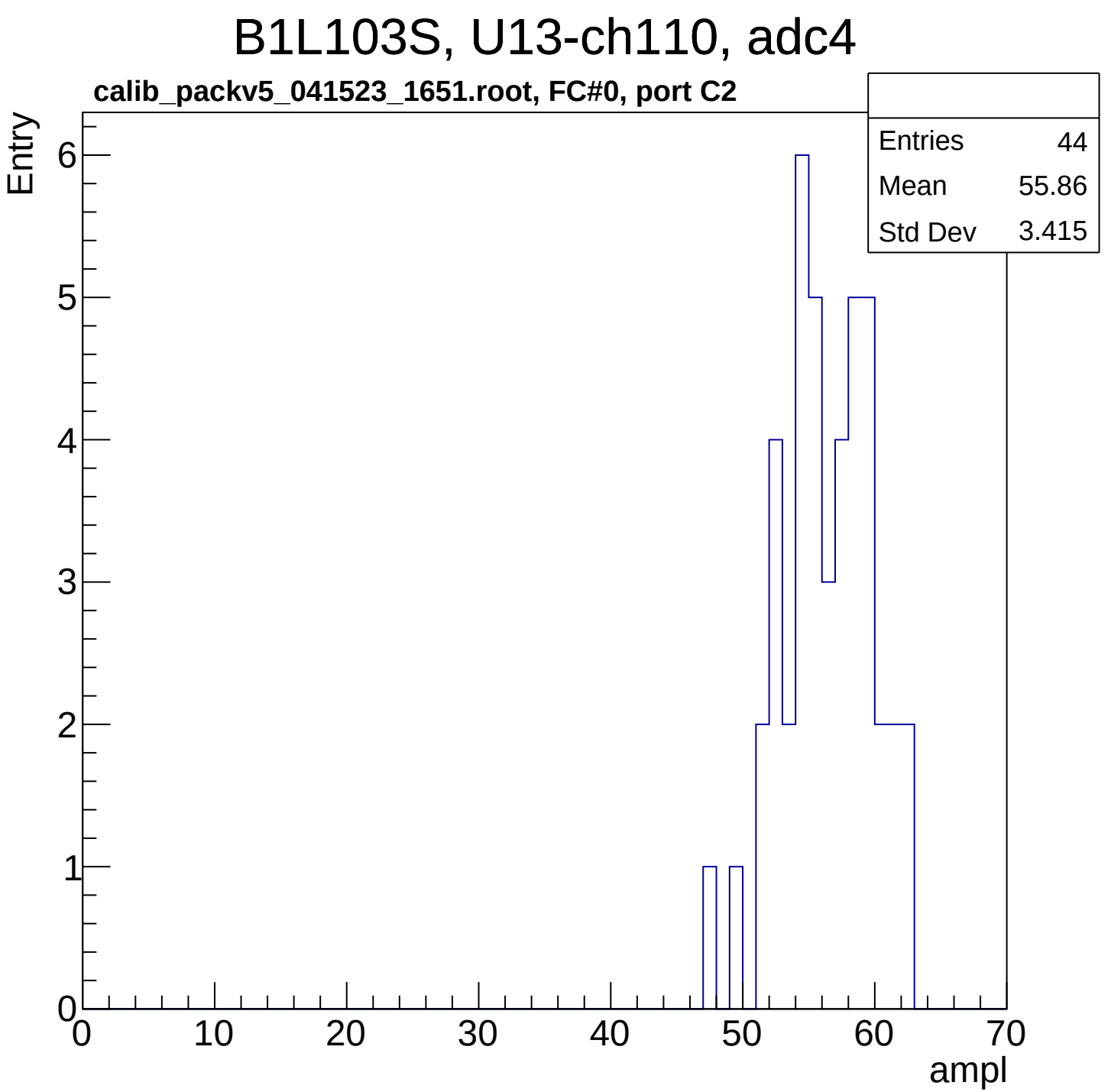
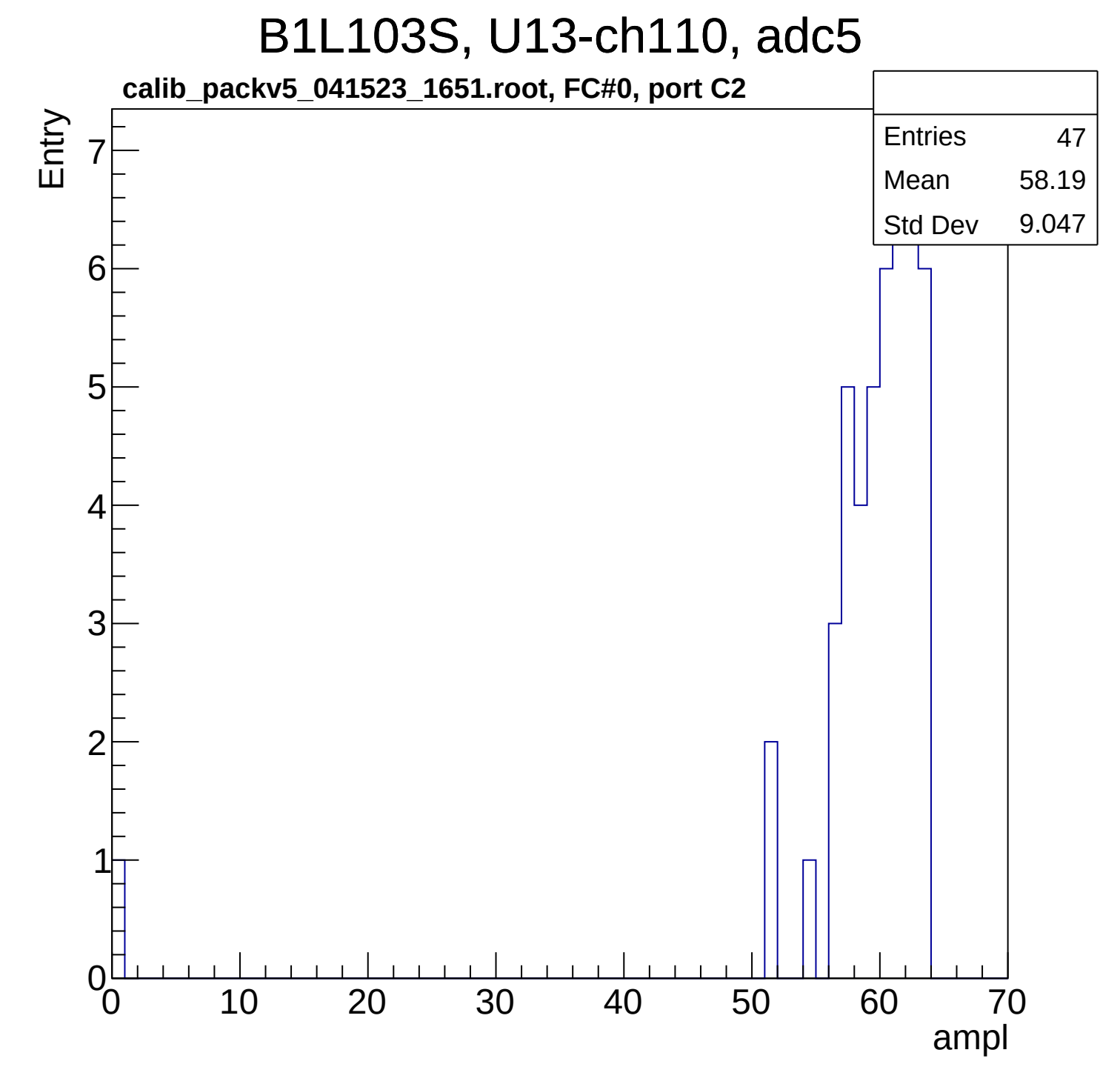
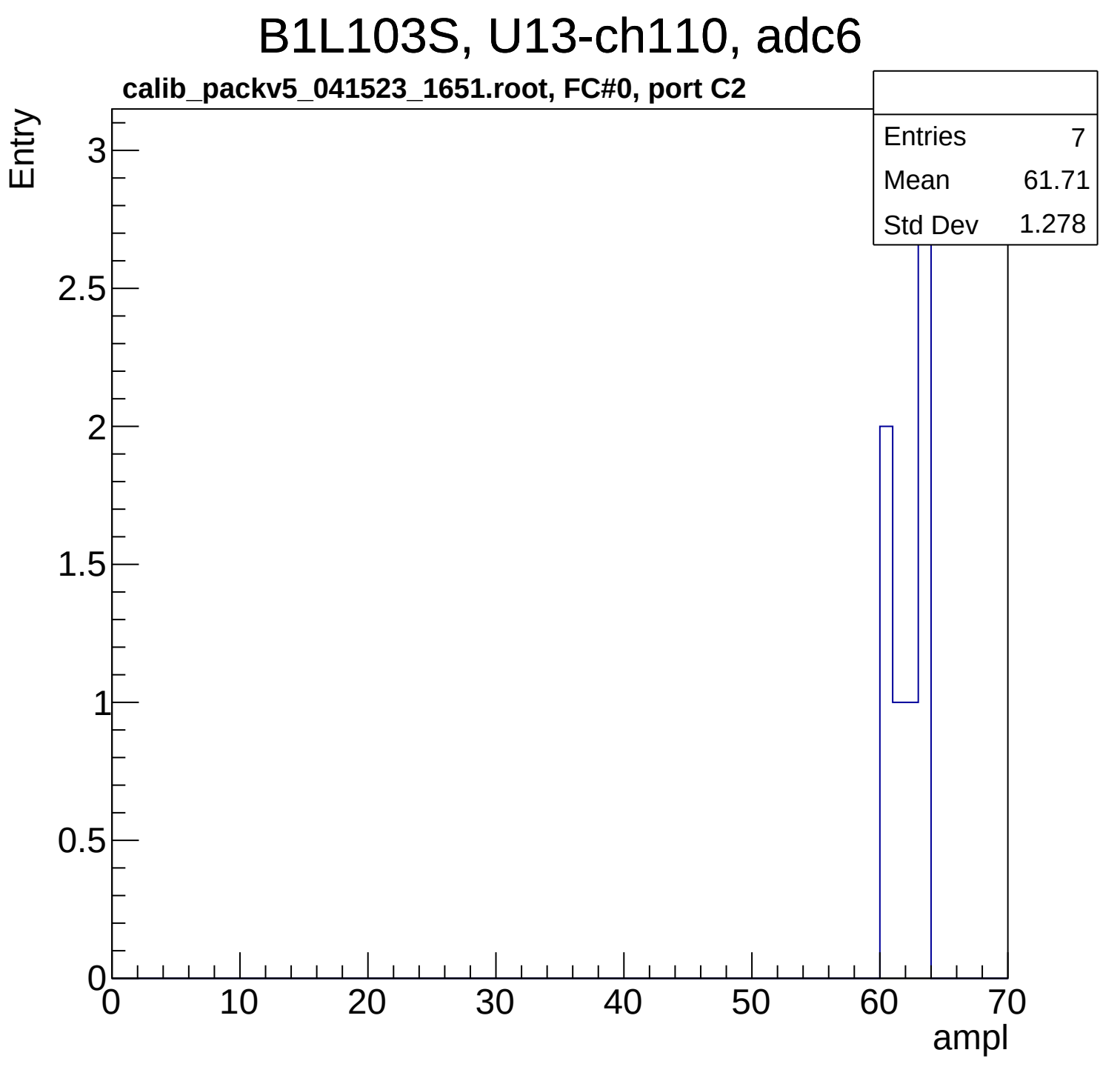
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch110, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 55.86
Std Dev 3.415
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch110, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.19
Std Dev 9.047
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch110, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.71
Std Dev 1.278
Entry
ampl
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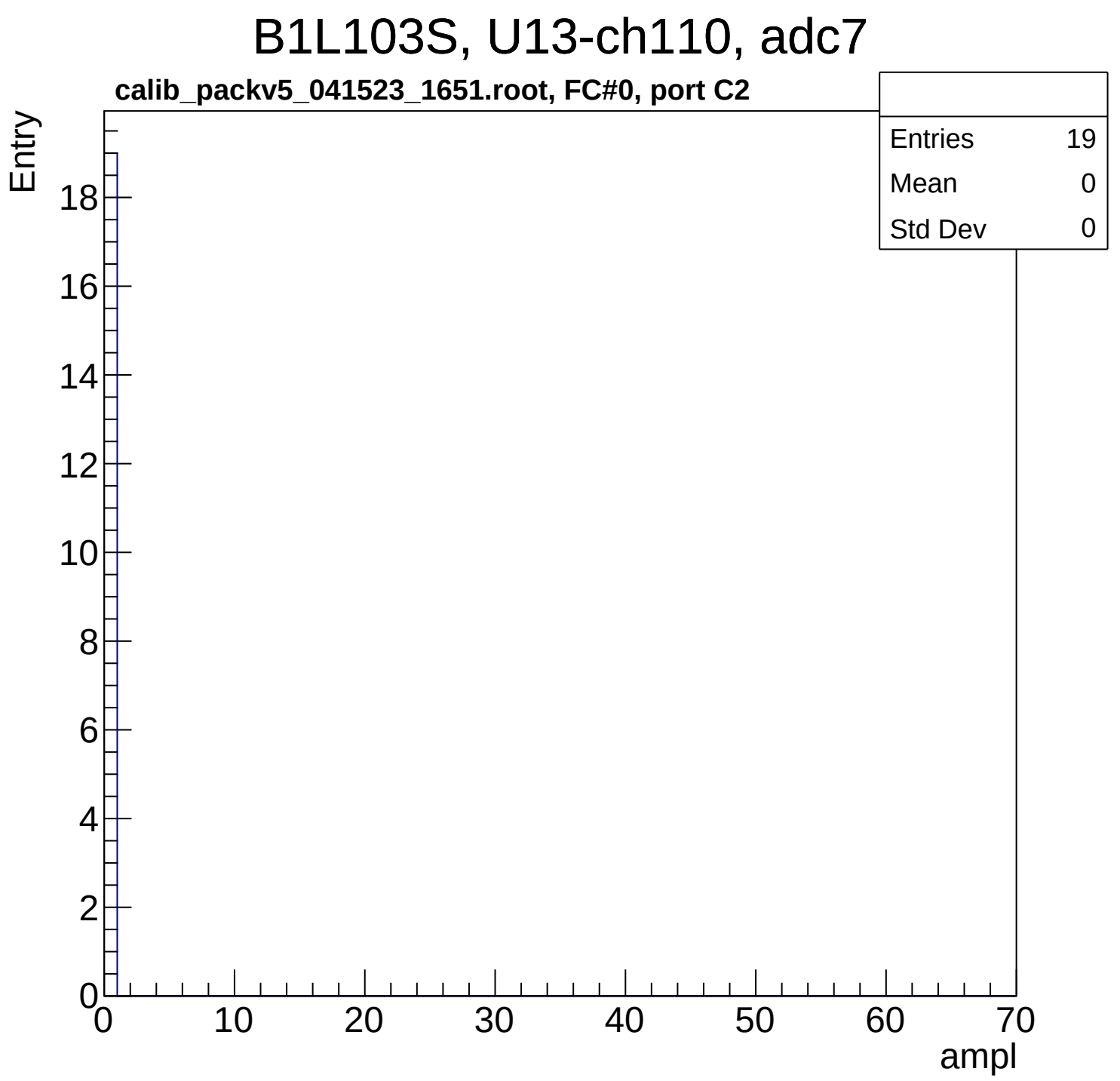
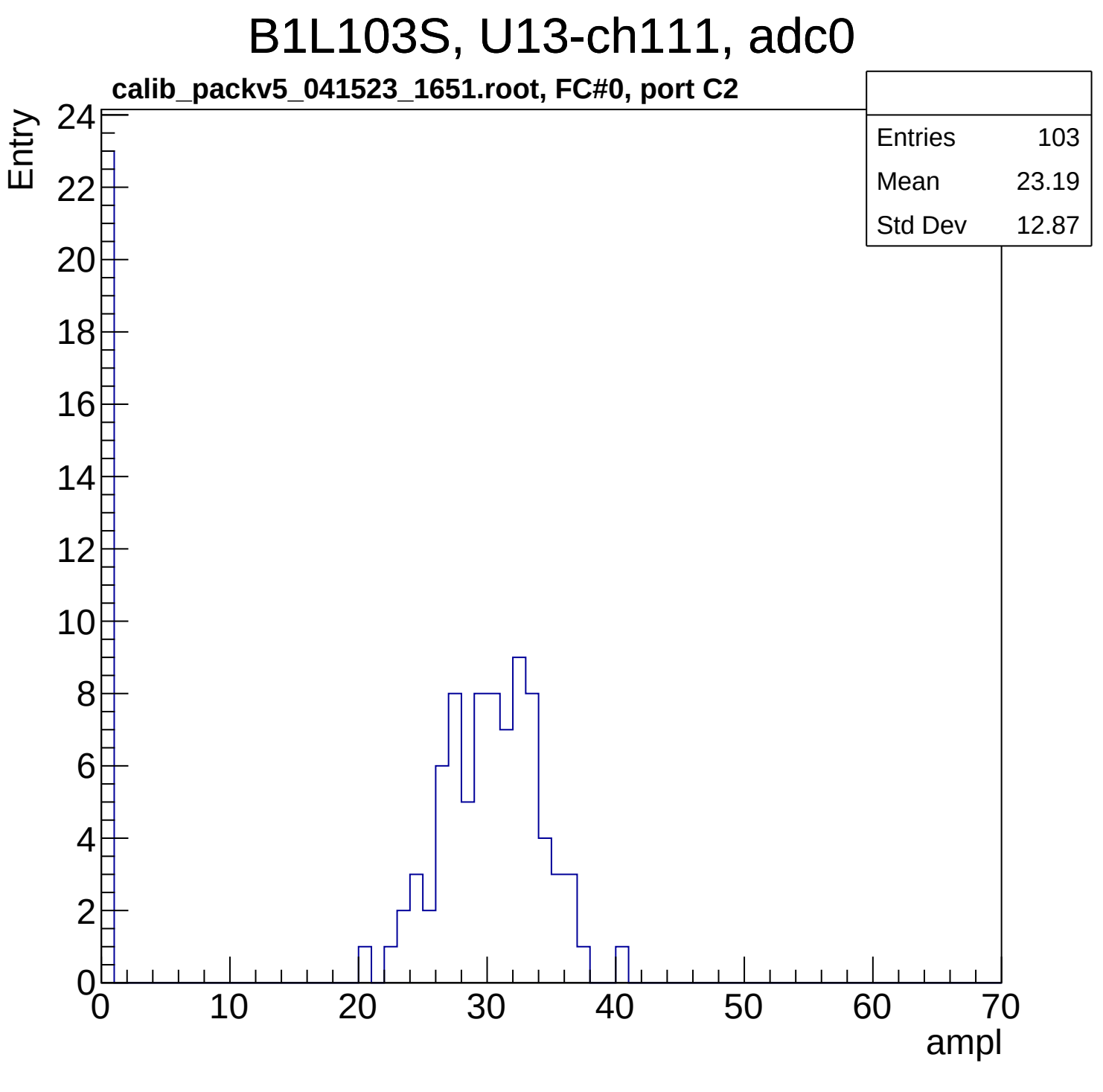
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U13-ch110, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch111, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 23.19
Std Dev 12.87
Entry
ampl
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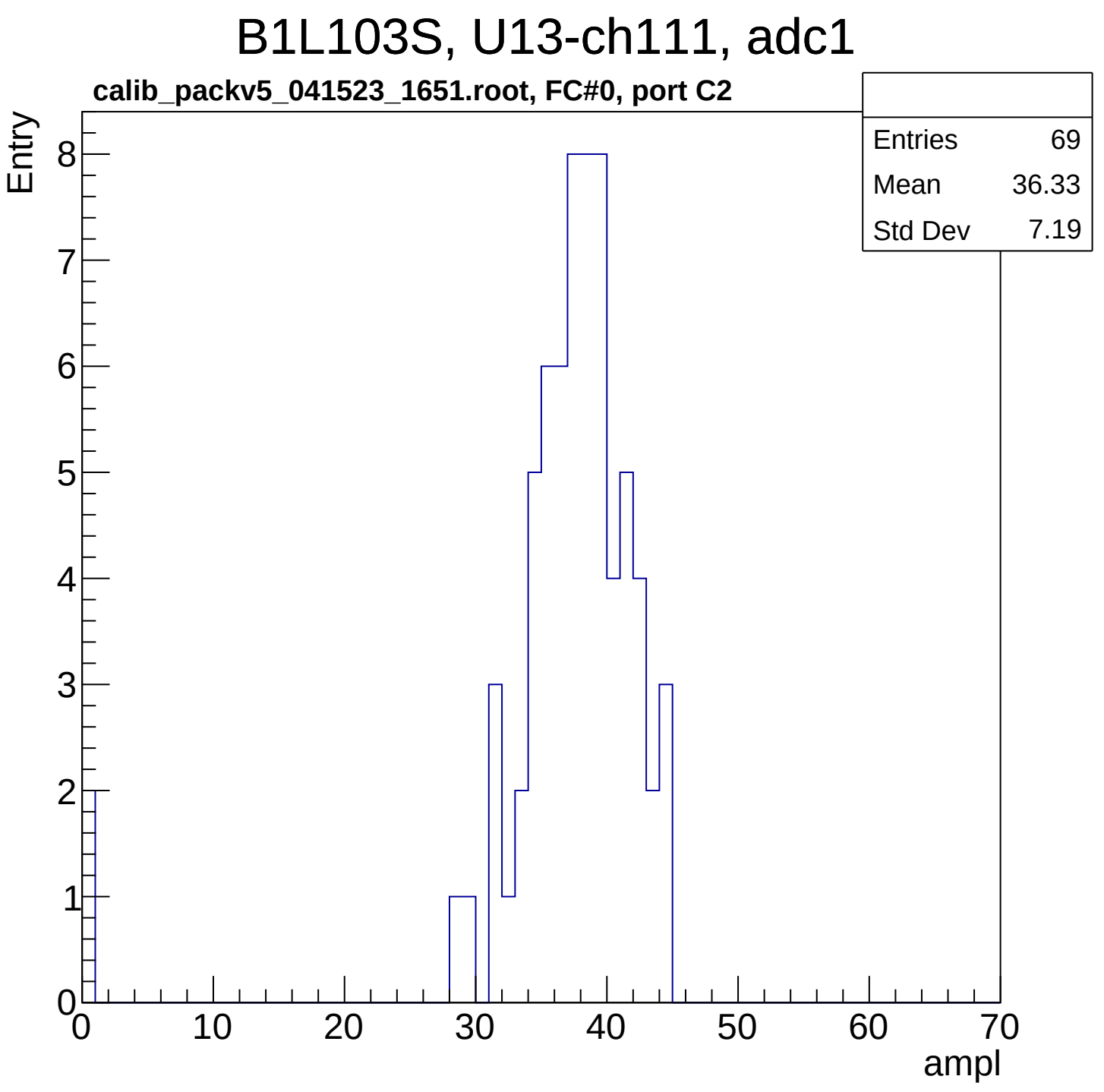
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70


B1L103S, U13-ch111, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 36.33
Std Dev 7.19
Entry
ampl
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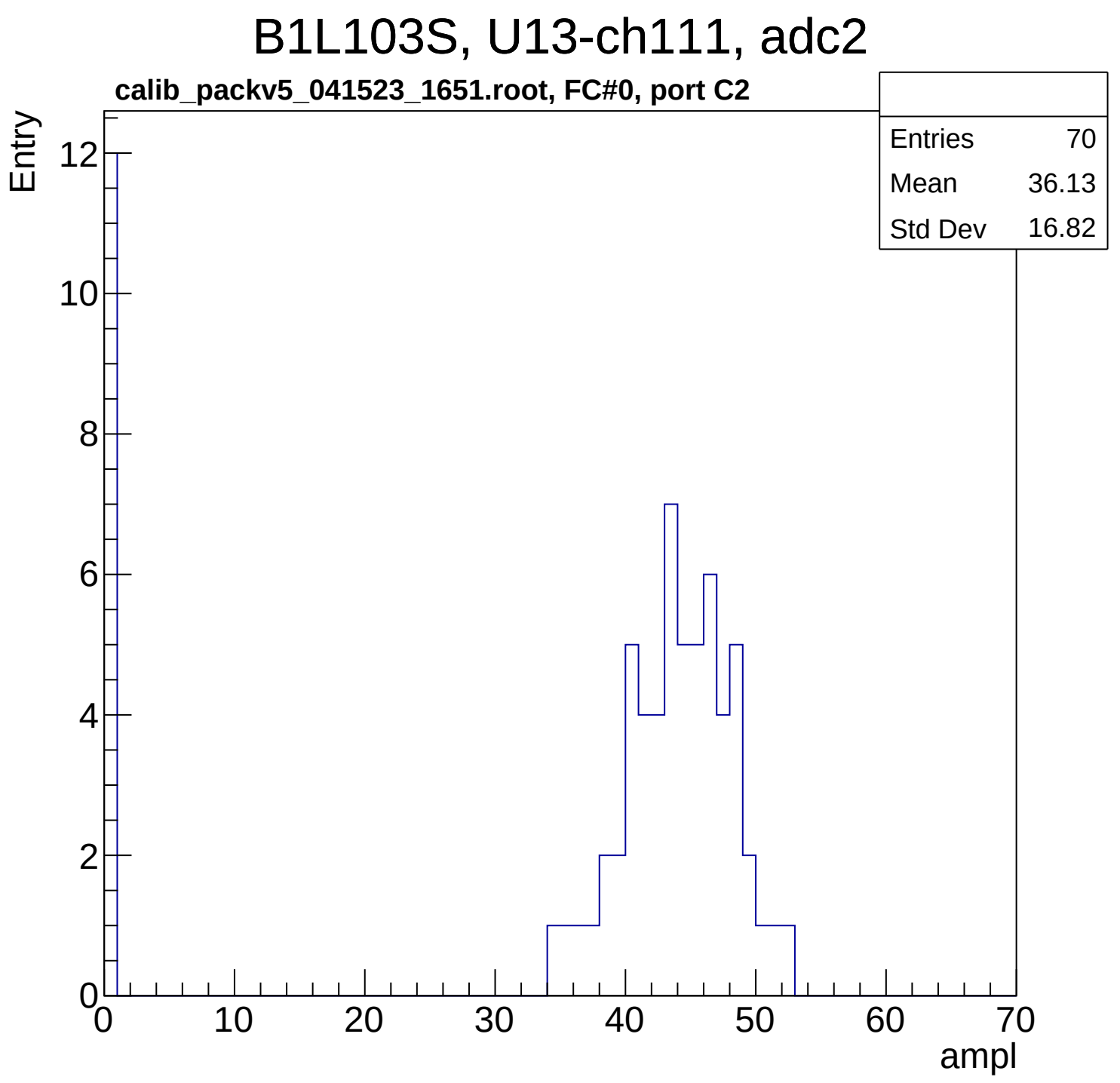
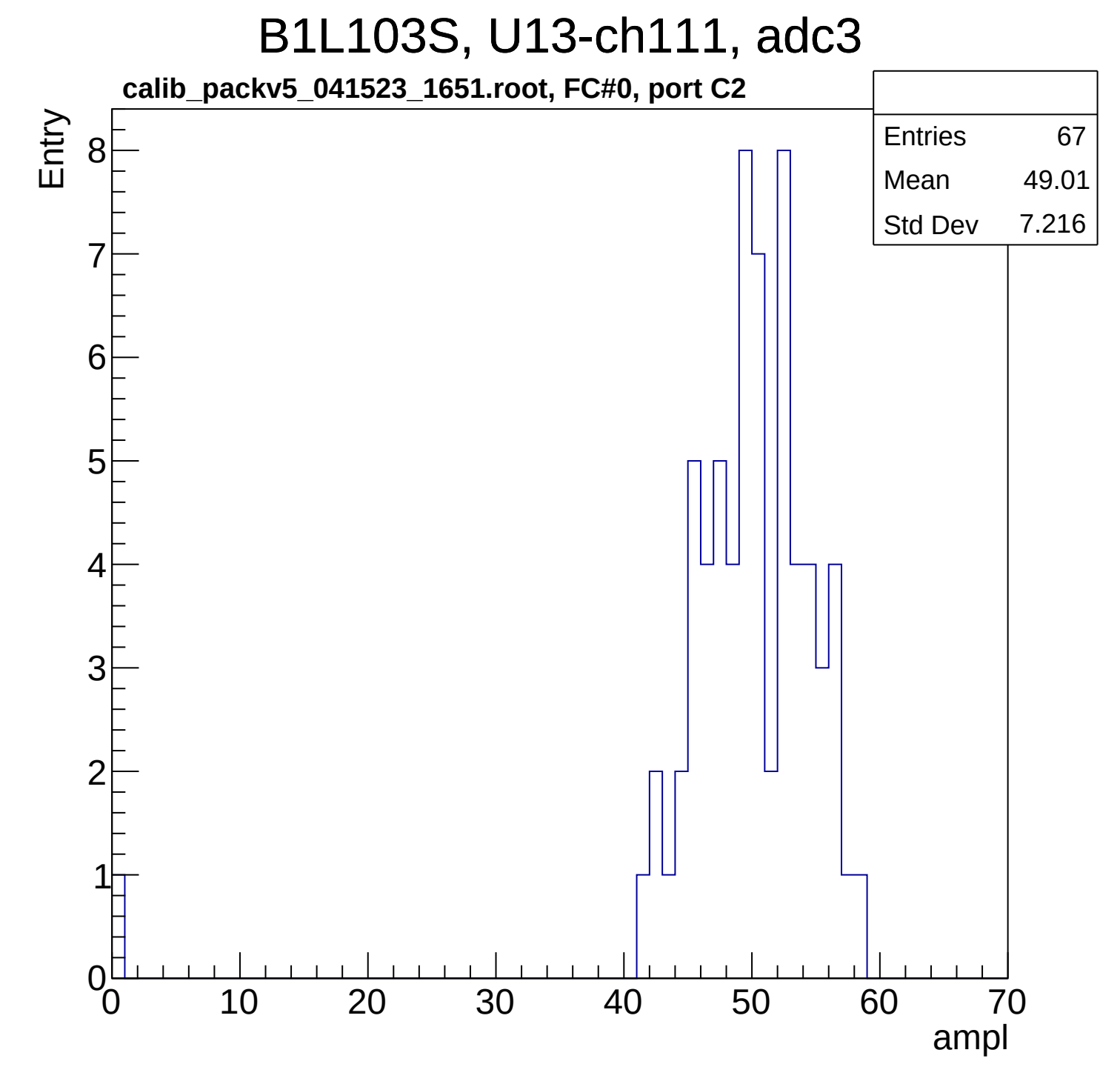
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch111, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 36.13
Std Dev 16.82
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch111, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 49.01
Std Dev 7.216
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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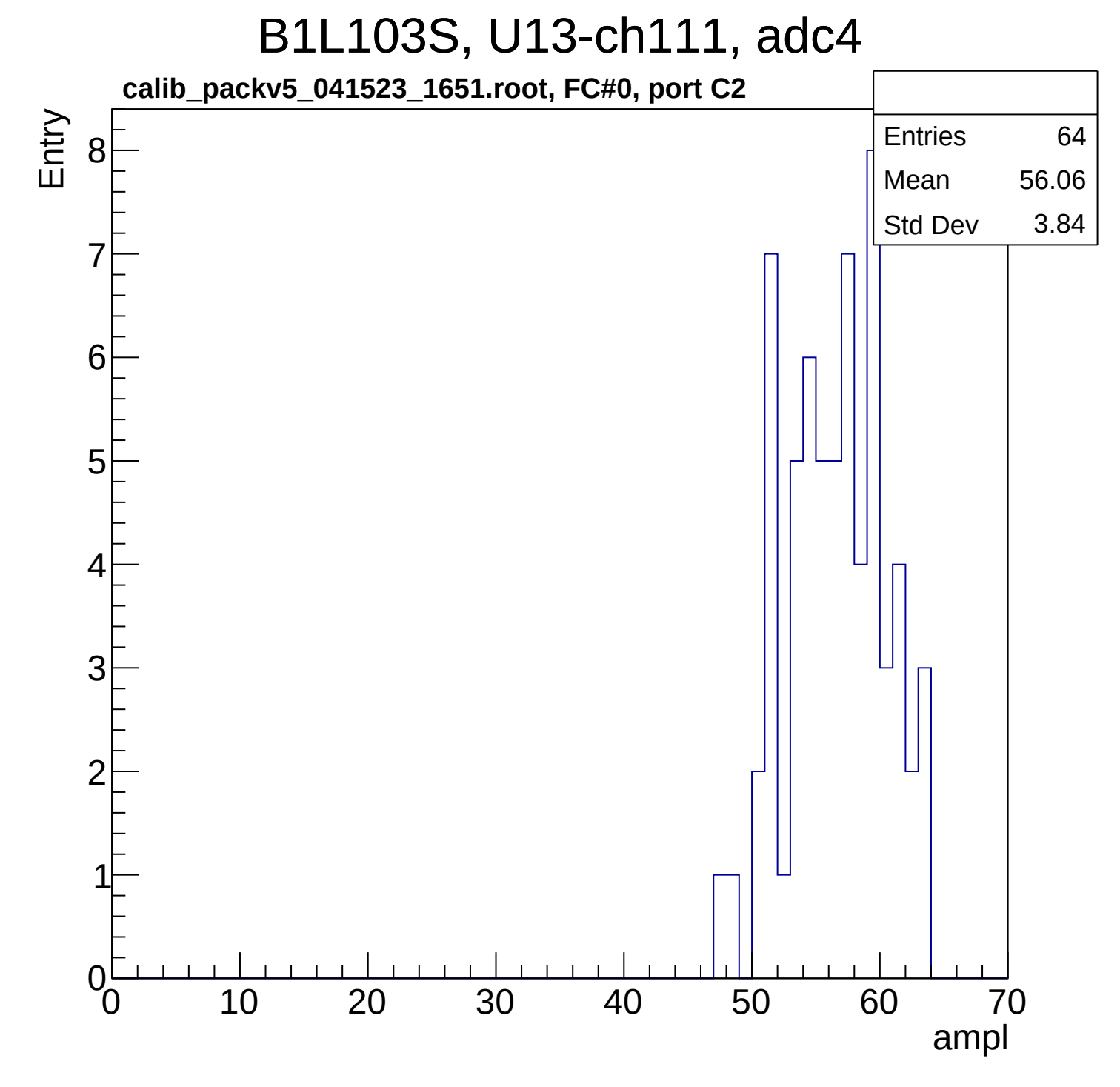
40
50
60
70


B1L103S, U13-ch111, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 56.06
Std Dev 3.84
Entry
ampl
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2
3
4
5
6
7
8
0
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60
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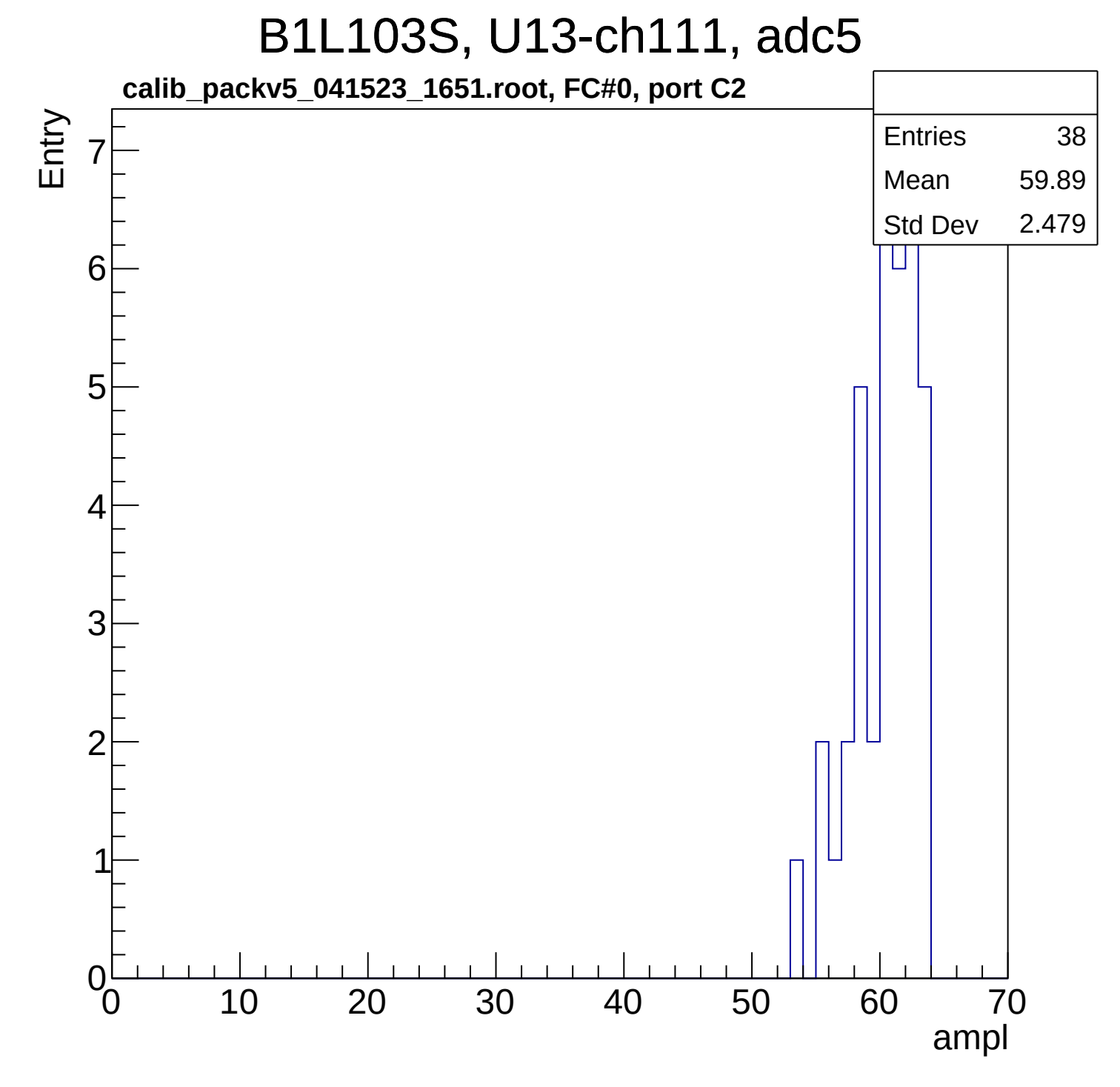
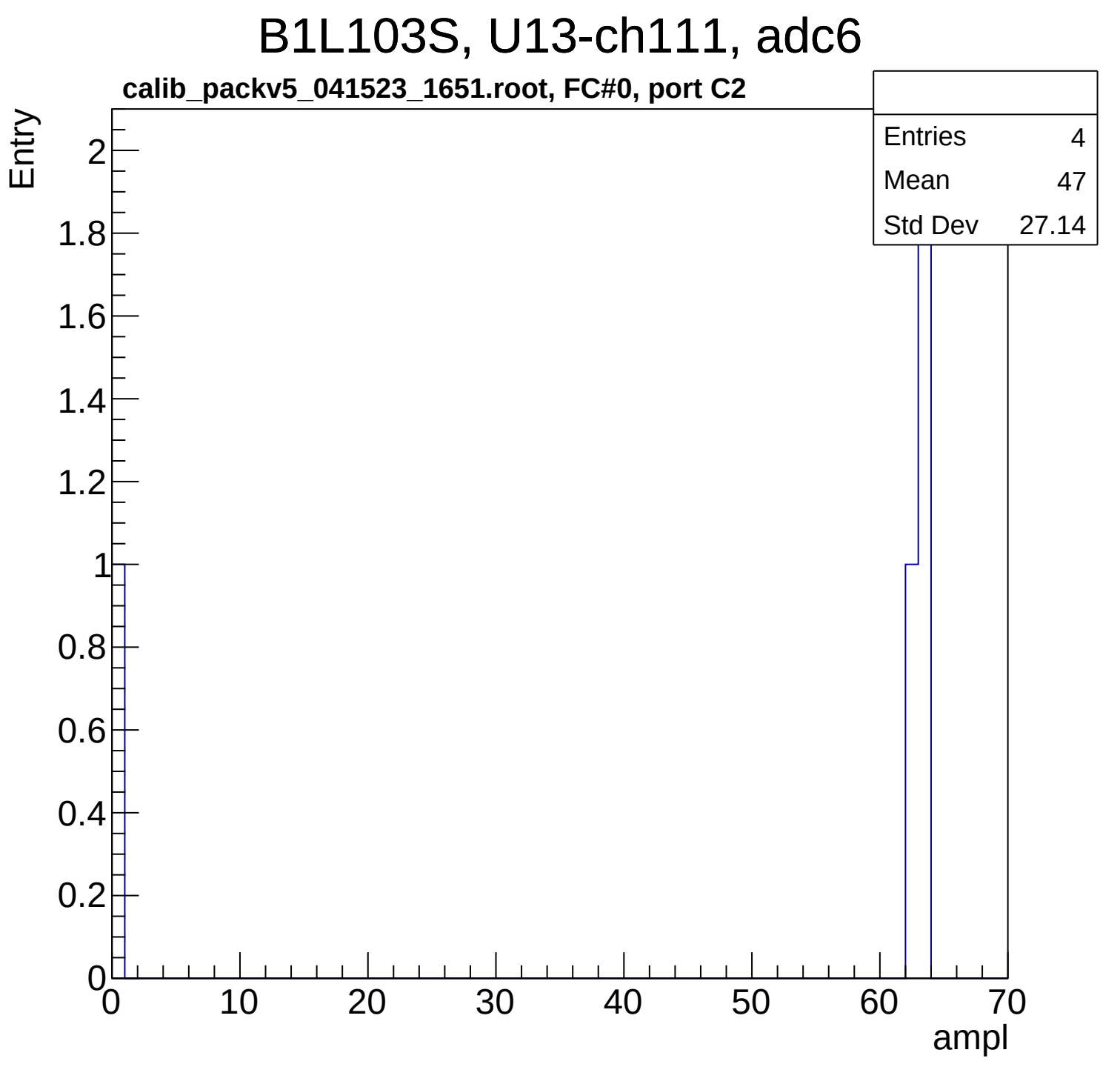
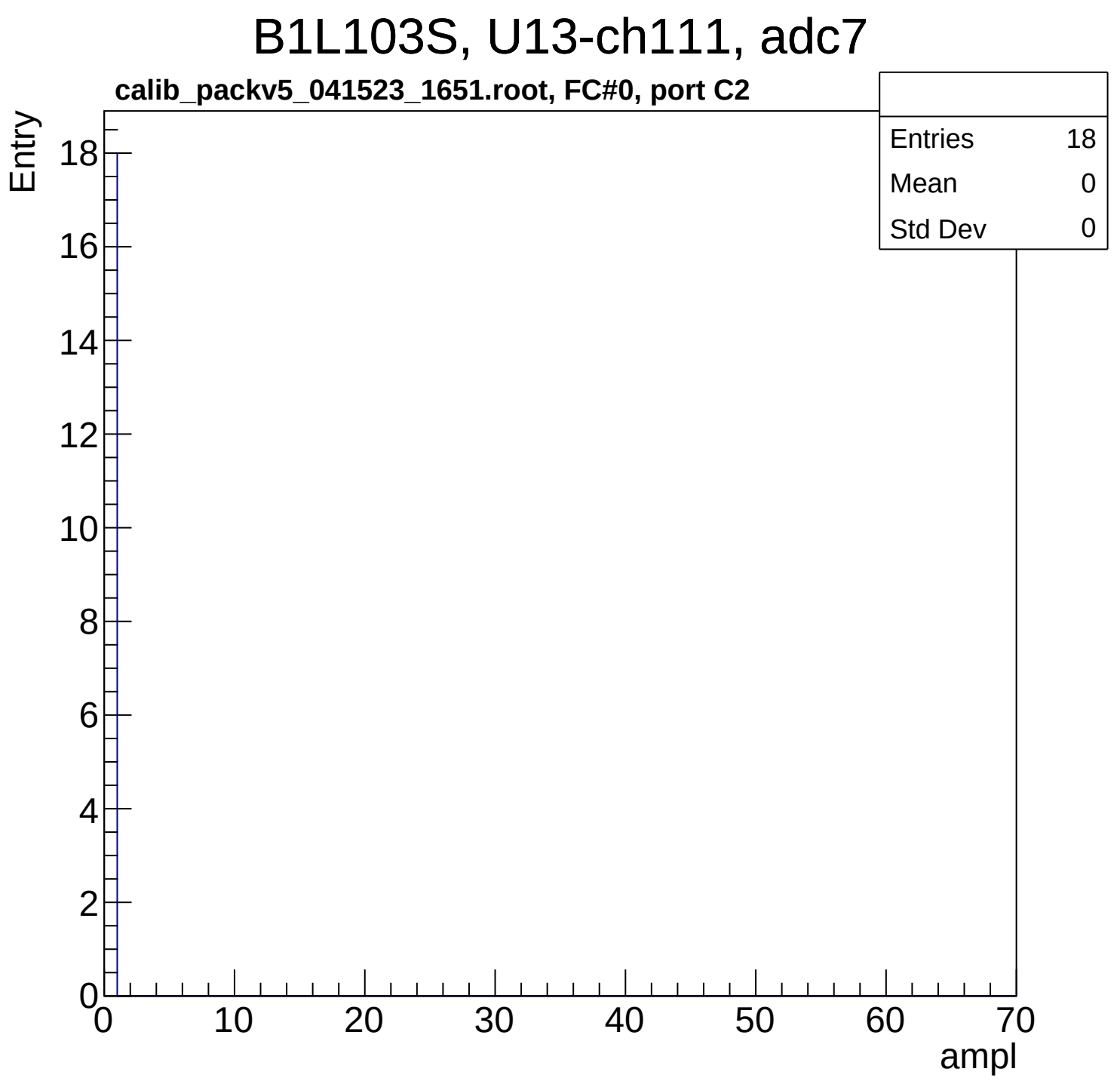
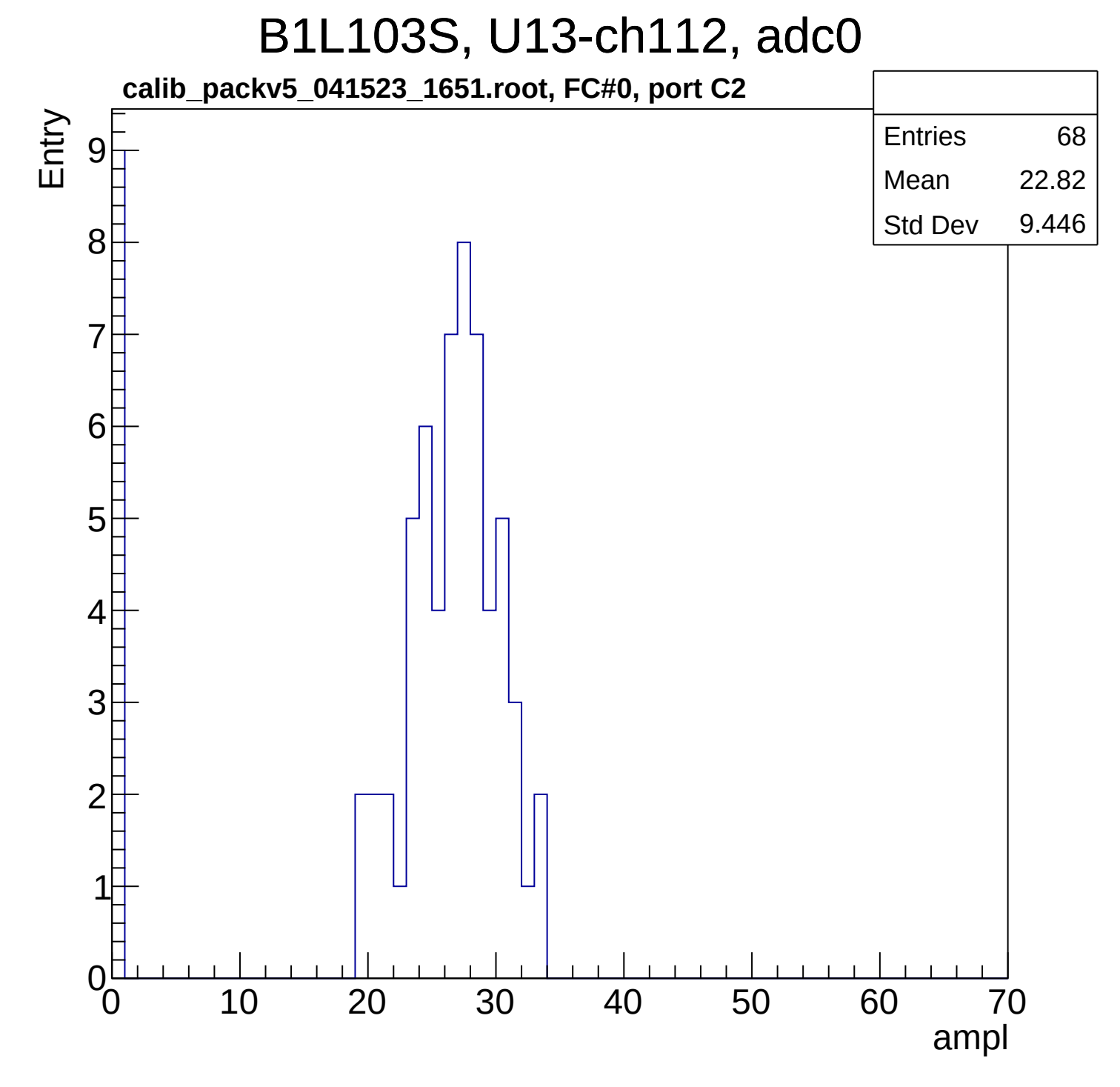

B1L103S, U13-ch111, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 59.89
Std Dev 2.479
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch111, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 47
Std Dev 27.14
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U13-ch111, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch112, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 22.82
Std Dev 9.446
Entry
ampl
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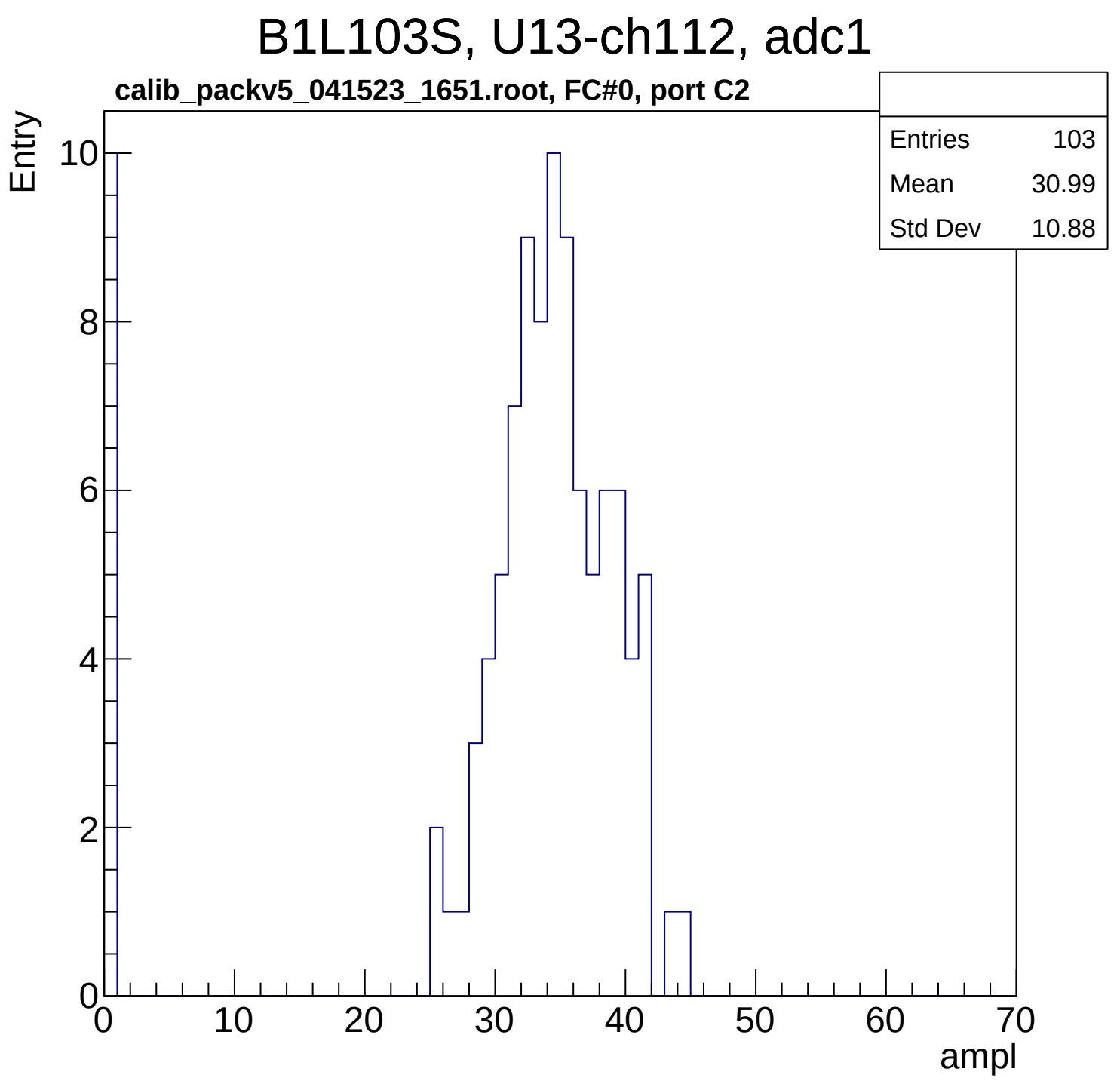
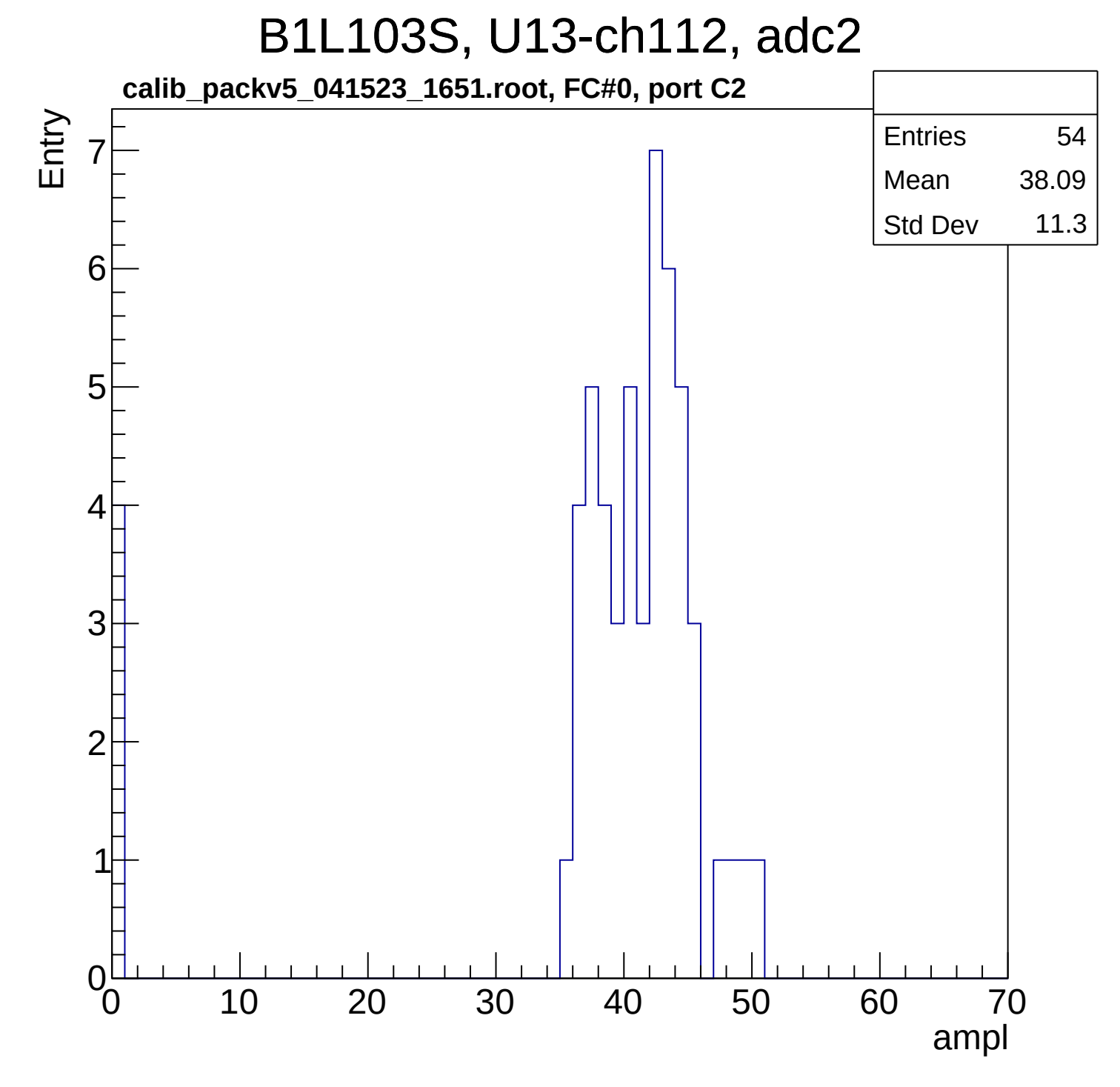
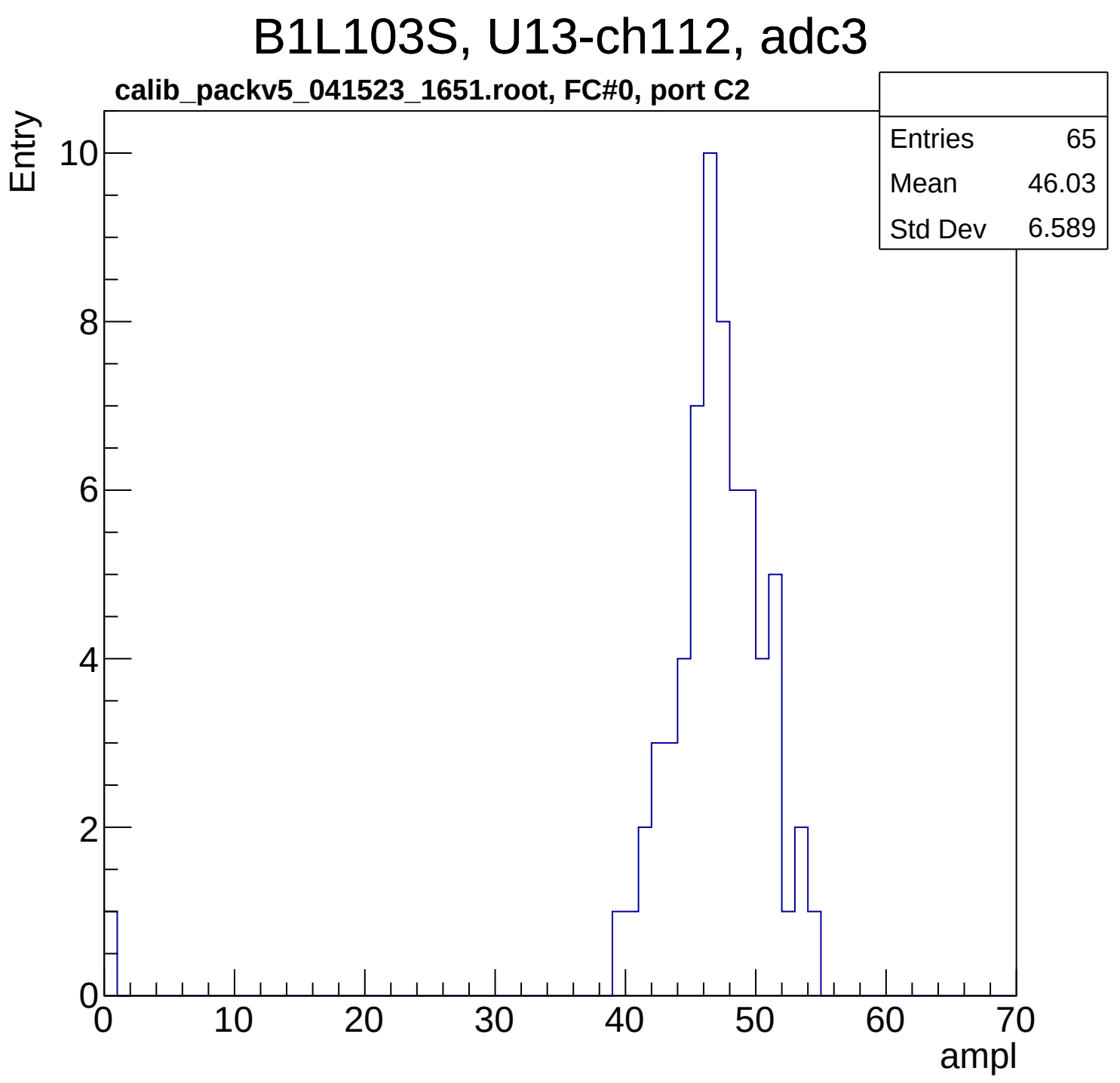
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch112, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 30.99
Std Dev 10.88
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch112, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 38.09
Std Dev 11.3
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch112, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 46.03
Std Dev 6.589
Entry
ampl
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4
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8
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0
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40
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60
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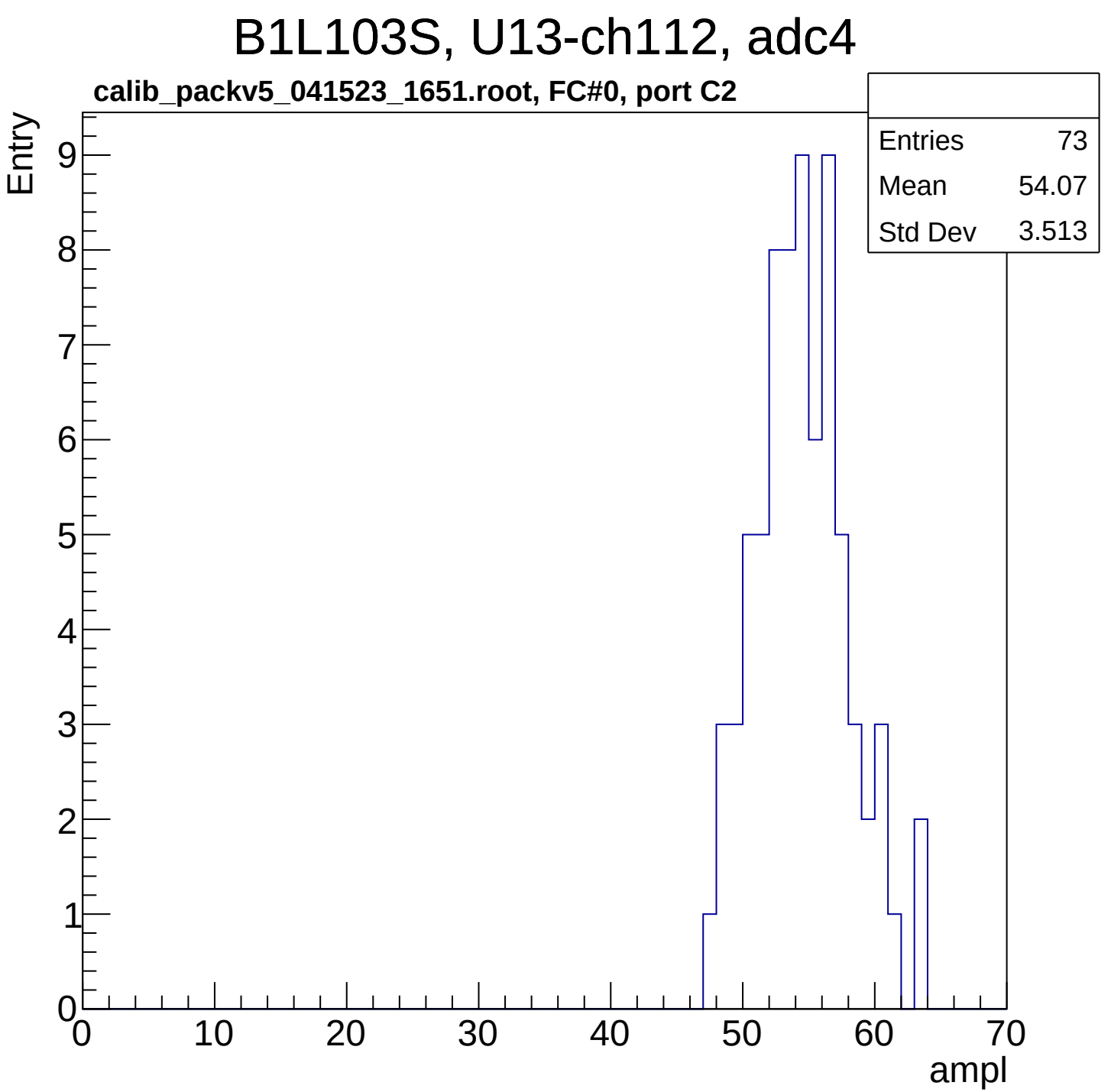
B1L103S, U13-ch112, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 54.07
Std Dev 3.513
Entry
ampl
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4
5
6
7
8
9
0
10
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40
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60
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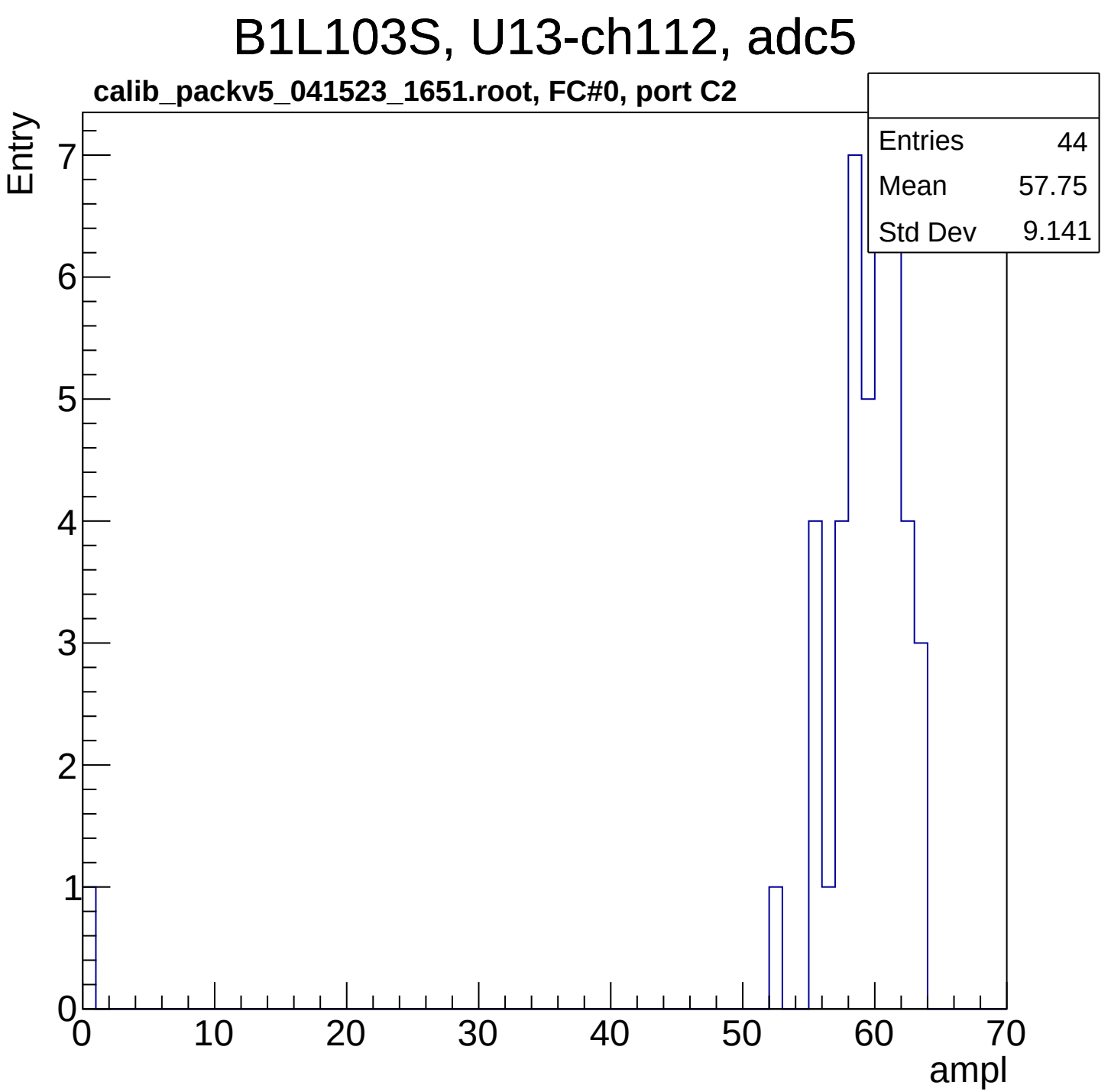
B1L103S, U13-ch112, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 57.75
Std Dev 9.141
Entry
ampl
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1
2
3
4
5
6
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0
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40
50
60
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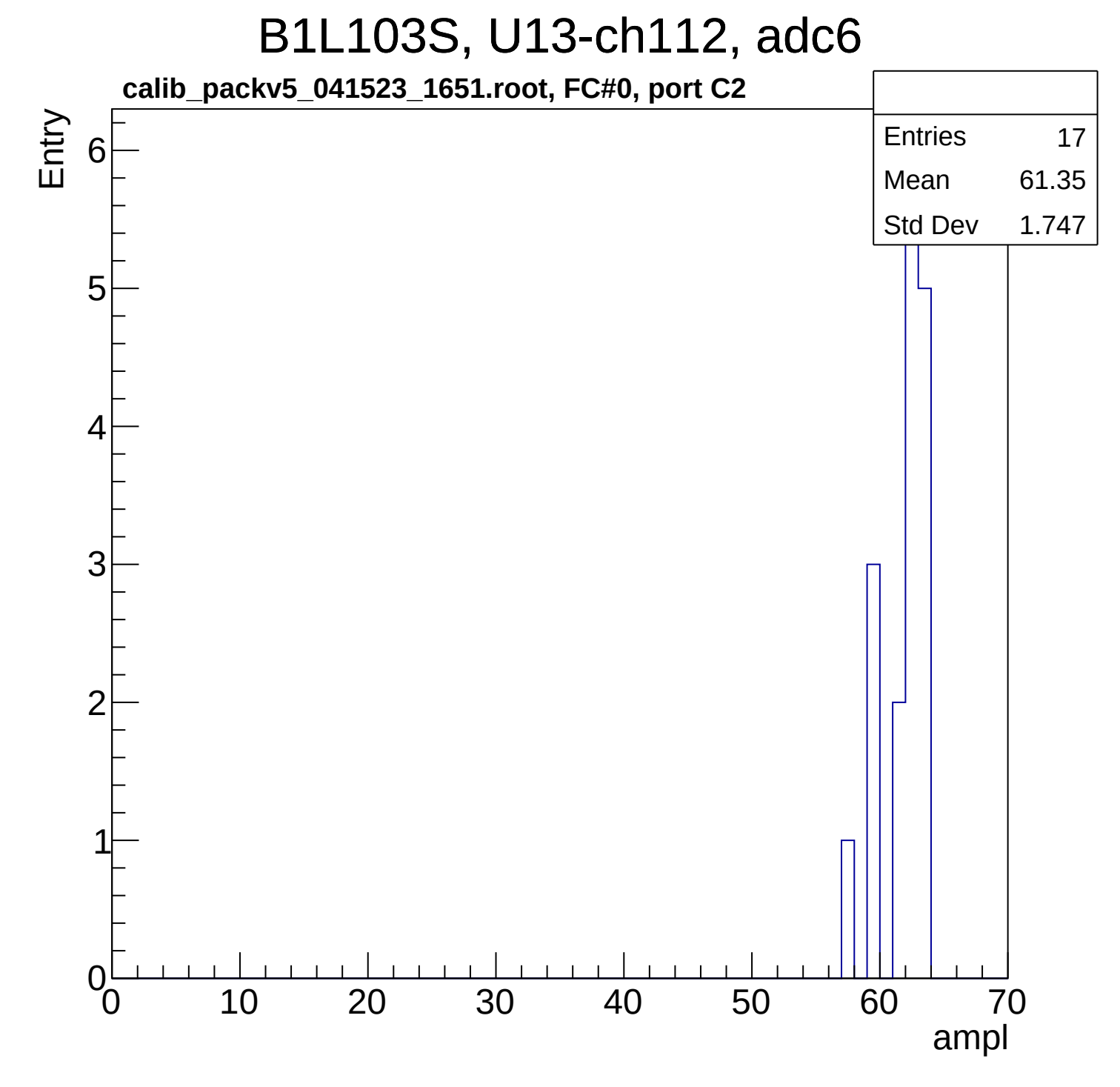
B1L103S, U13-ch112, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.35
Std Dev 1.747
Entry
ampl
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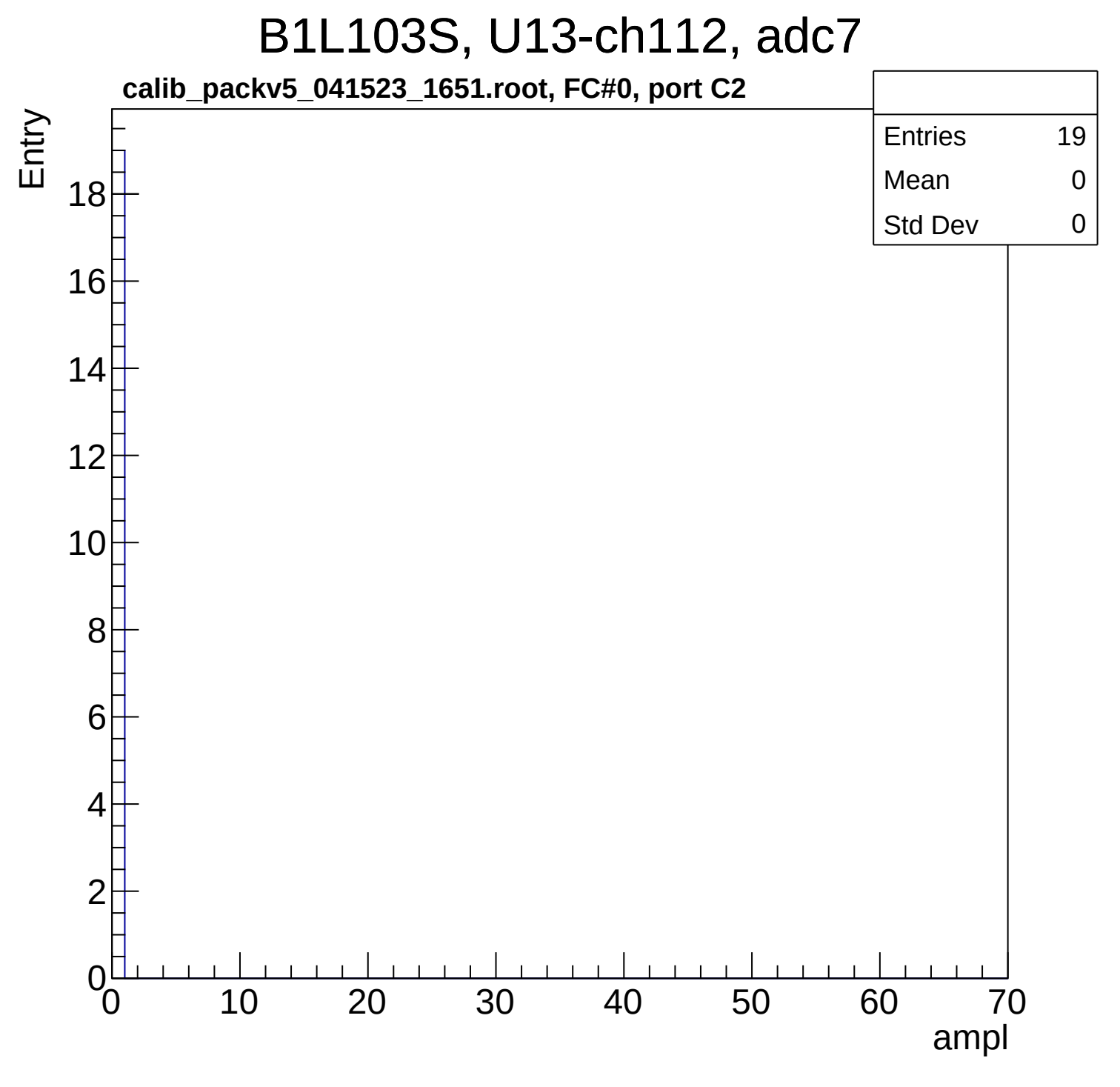
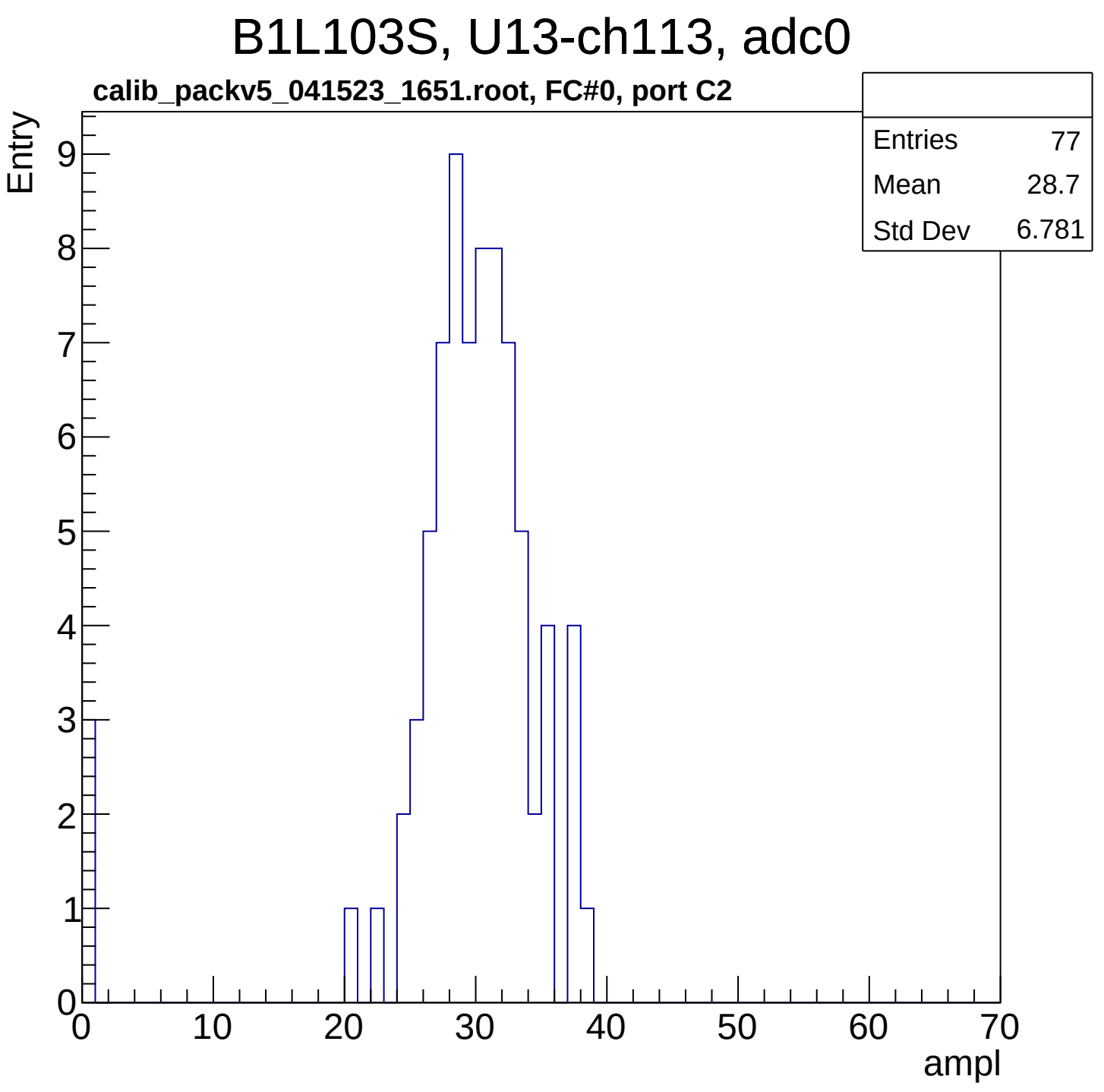
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U13-ch112, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch113, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 28.7
Std Dev 6.781
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
50
60
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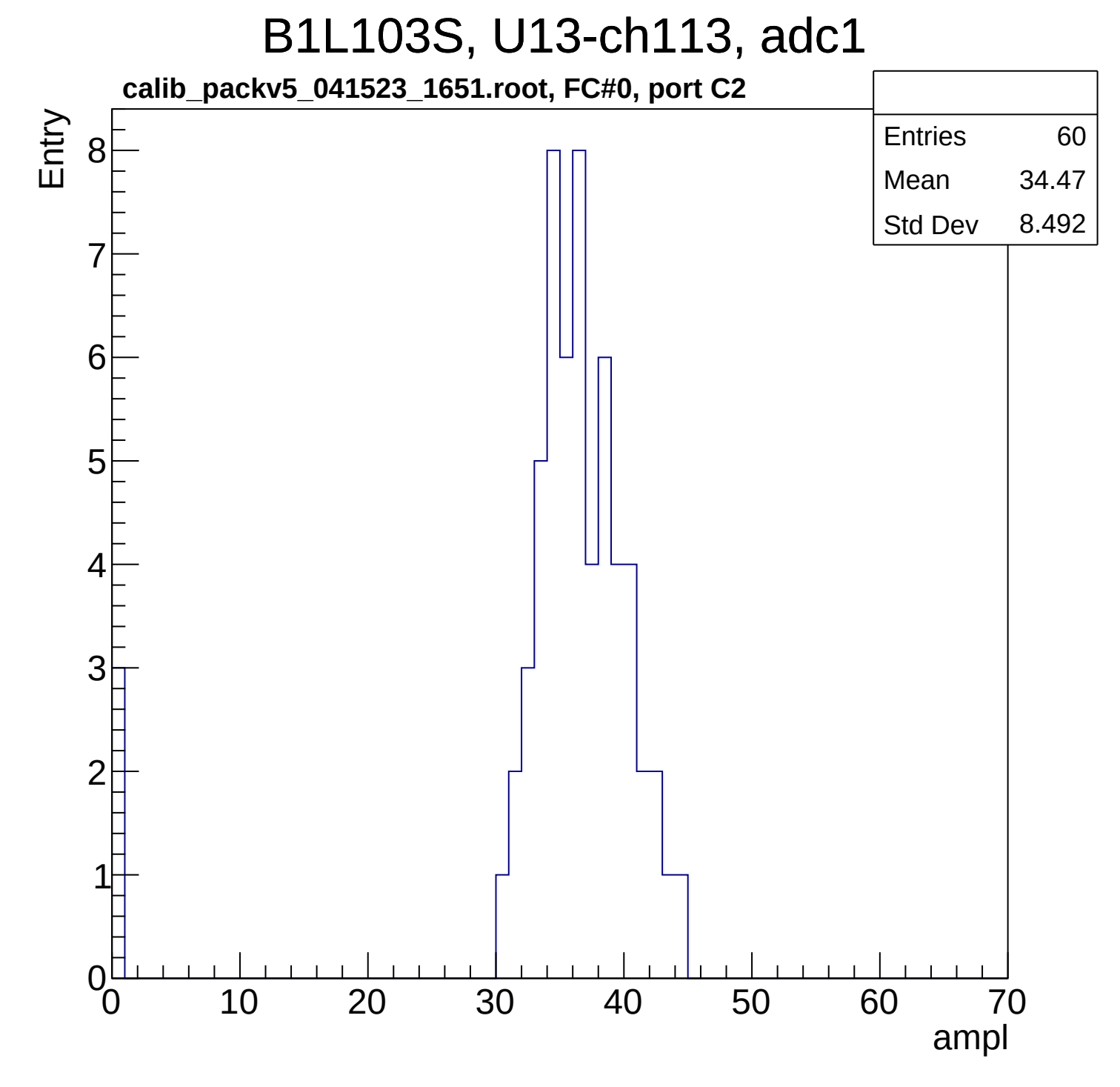
B1L103S, U13-ch113, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 34.47
Std Dev 8.492
Entry
ampl
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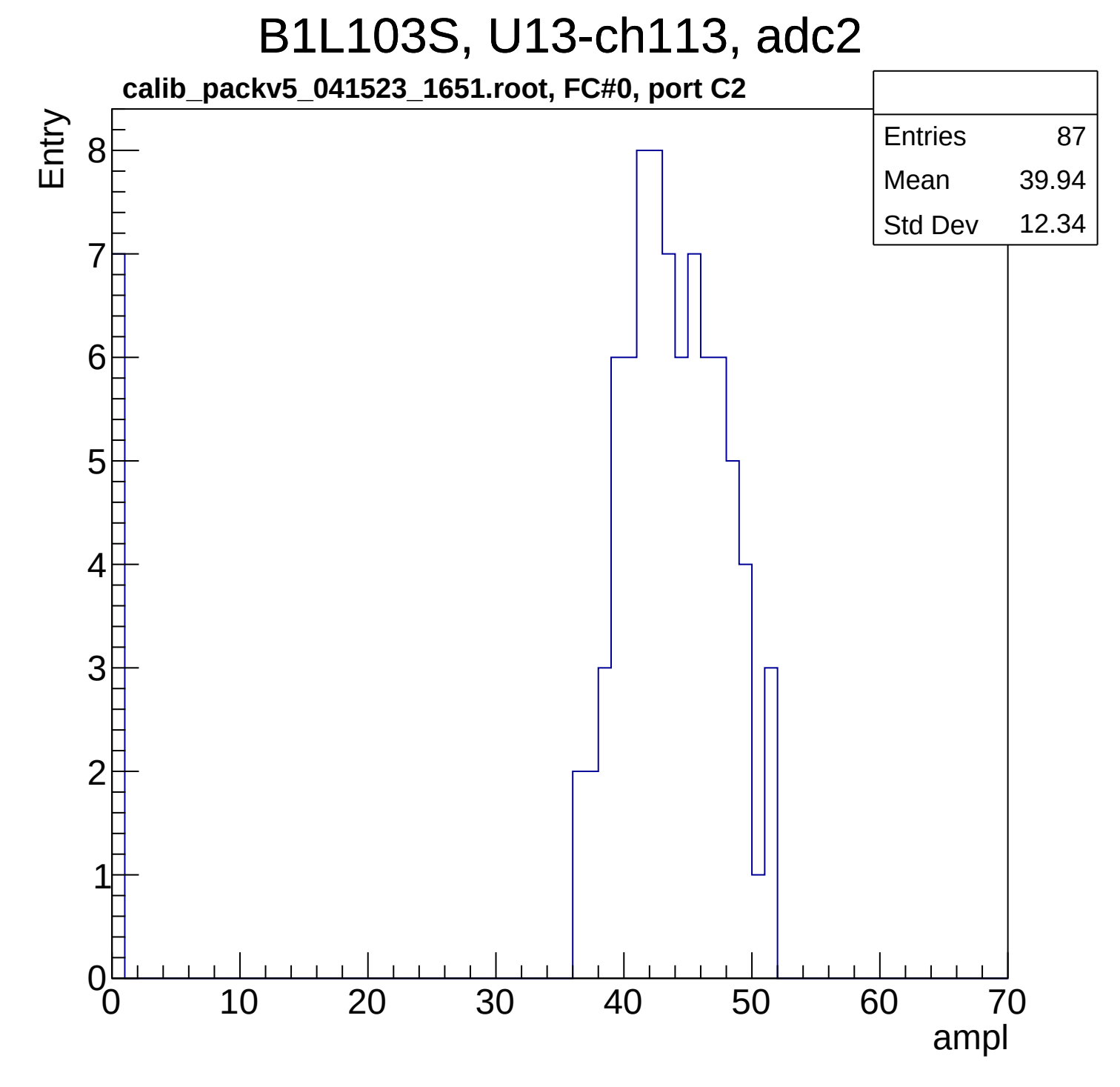
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch113, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 39.94
Std Dev 12.34
Entry
ampl
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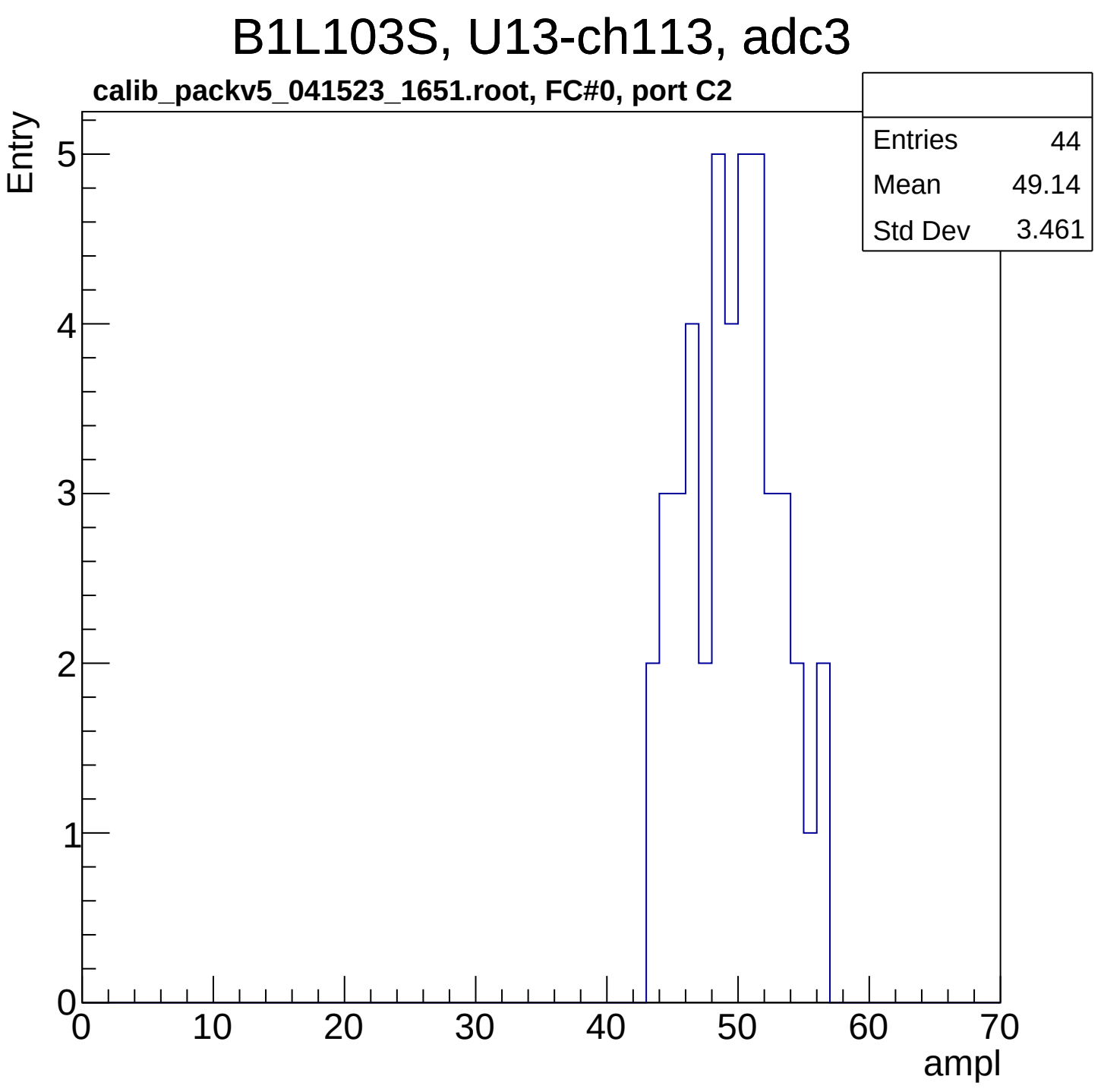
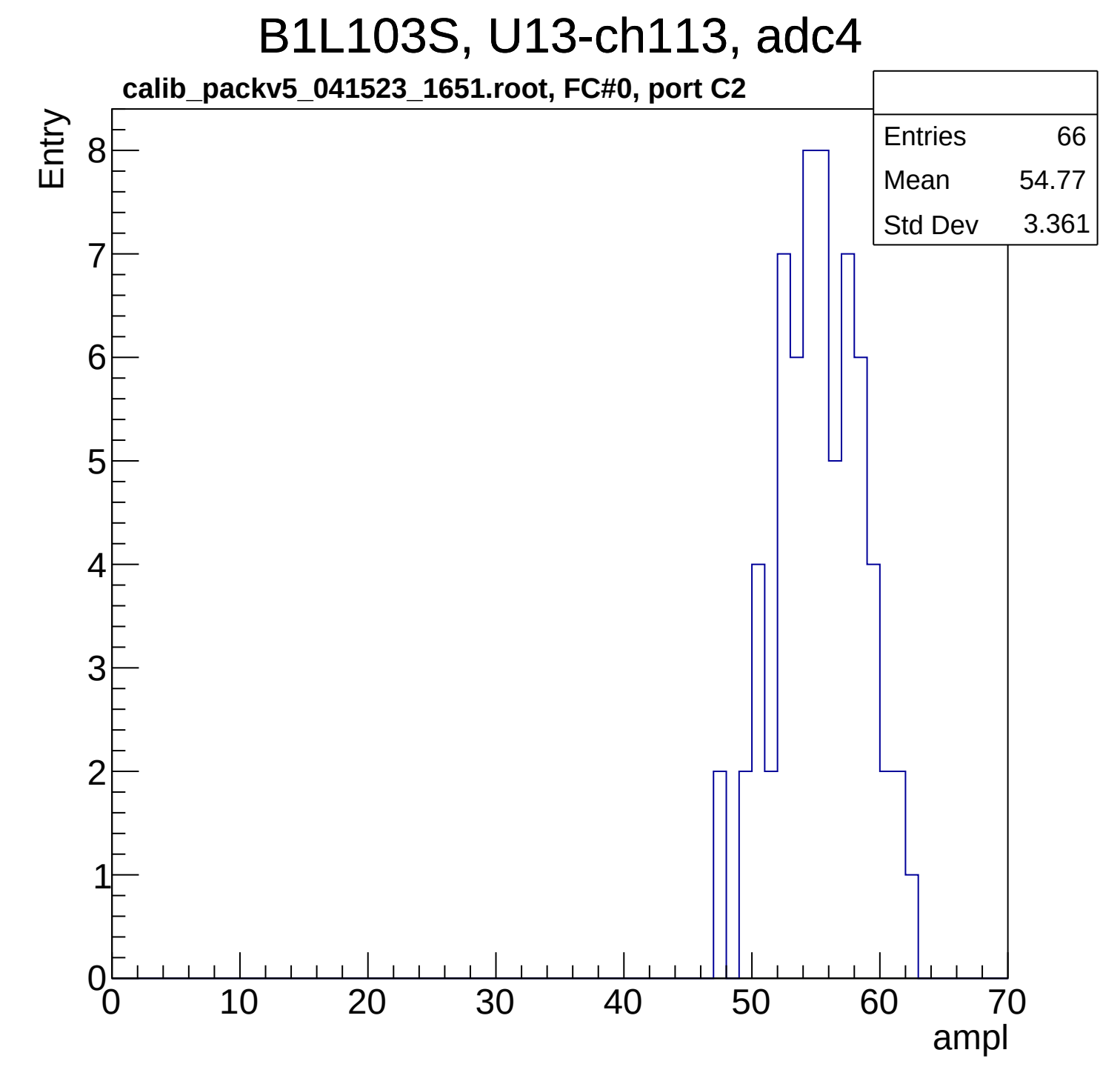
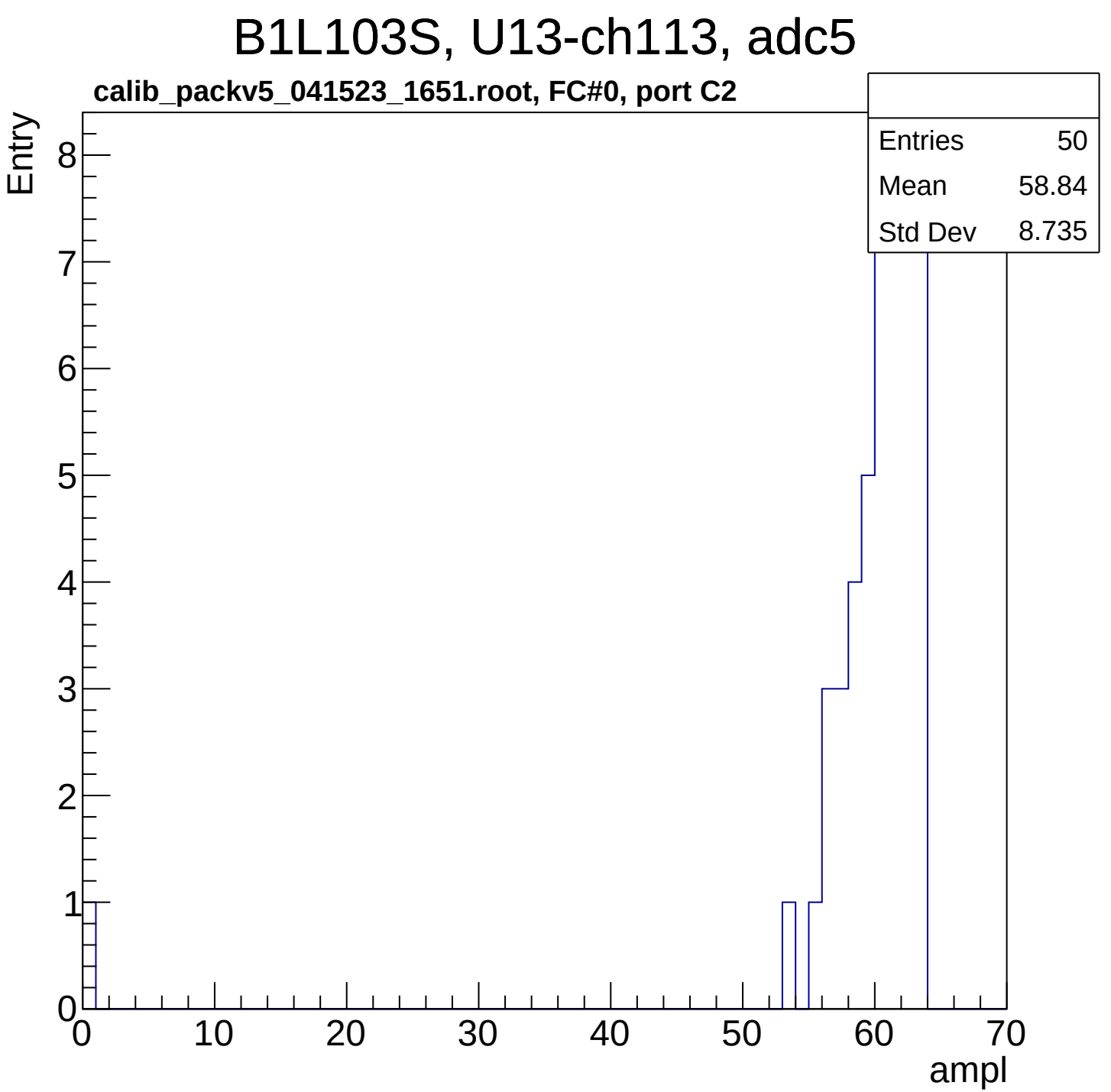
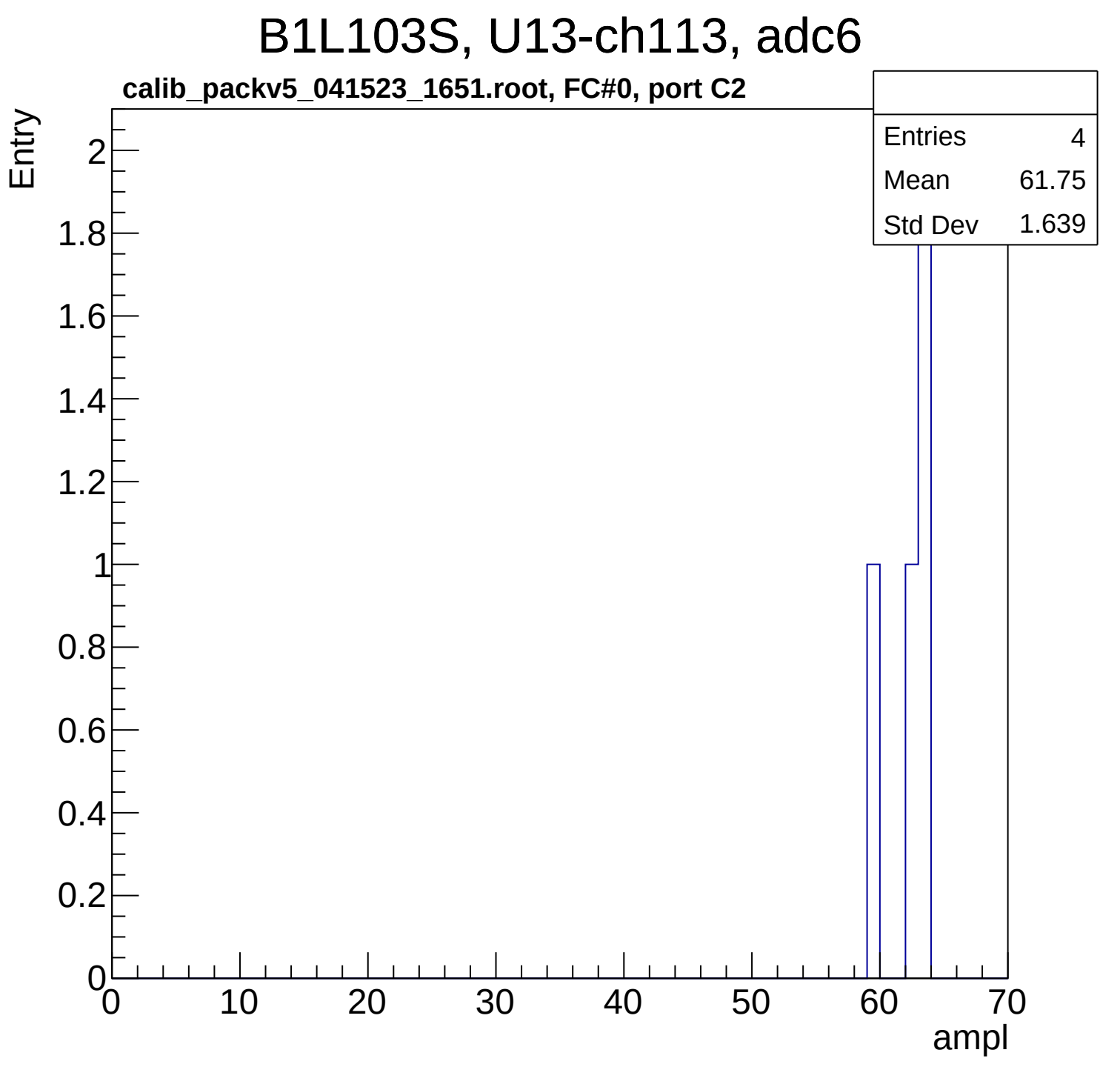
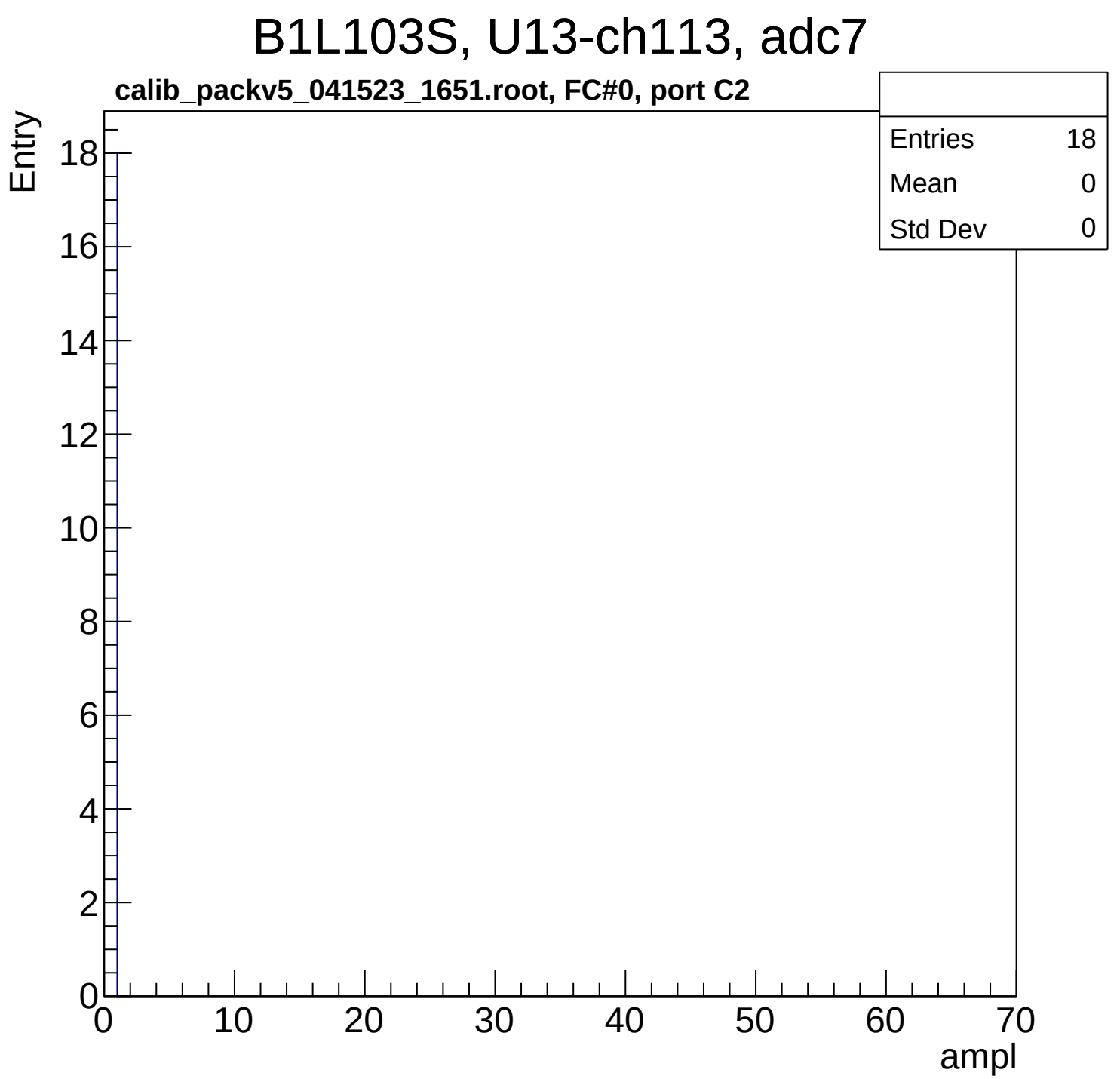
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

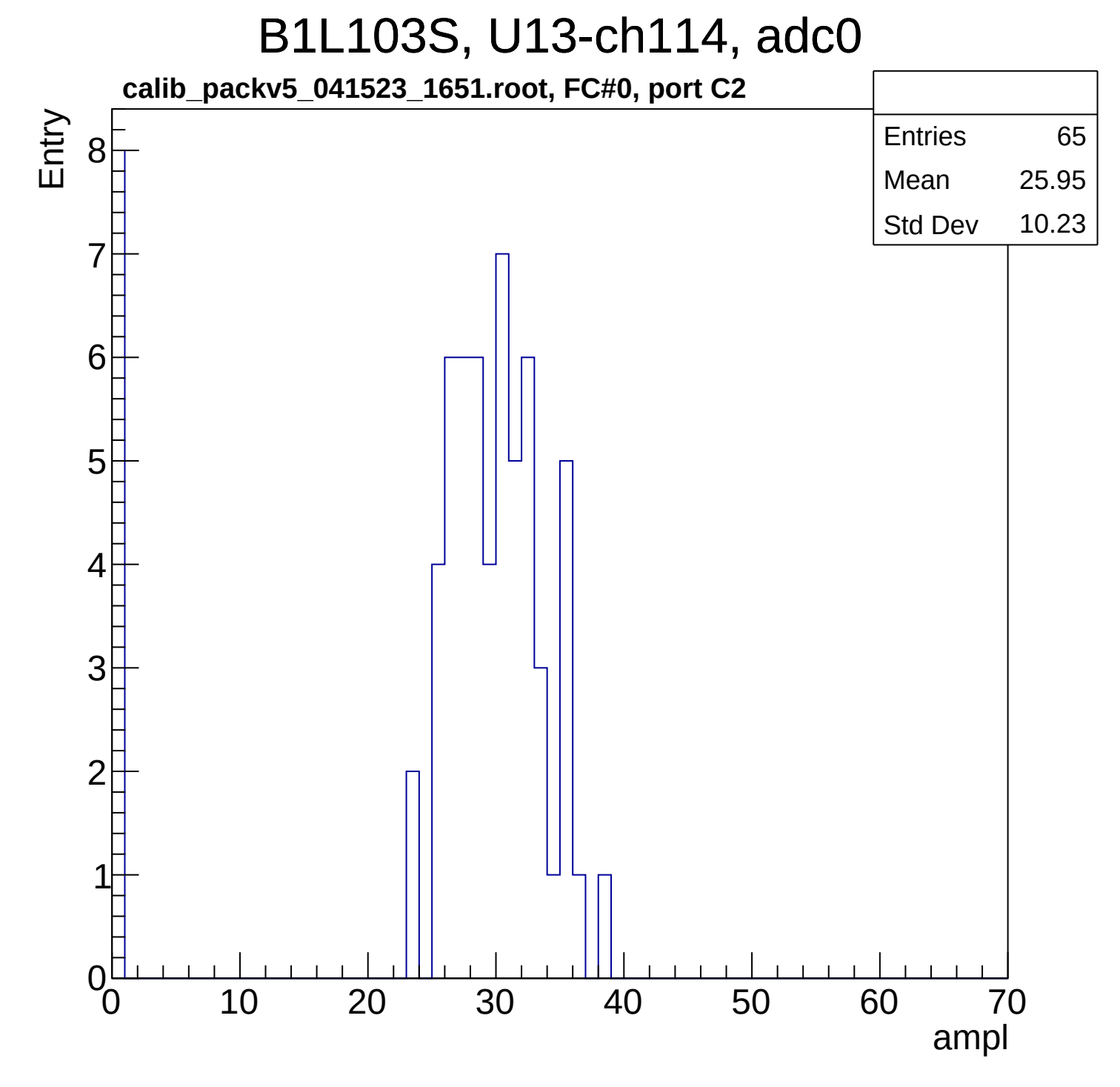

B1L103S, U13-ch113, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 49.14
Std Dev 3.461
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch113, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 54.77
Std Dev 3.361
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch113, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.84
Std Dev 8.735
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch113, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61.75
Std Dev 1.639
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U13-ch113, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch114, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 25.95
Std Dev 10.23
Entry
0
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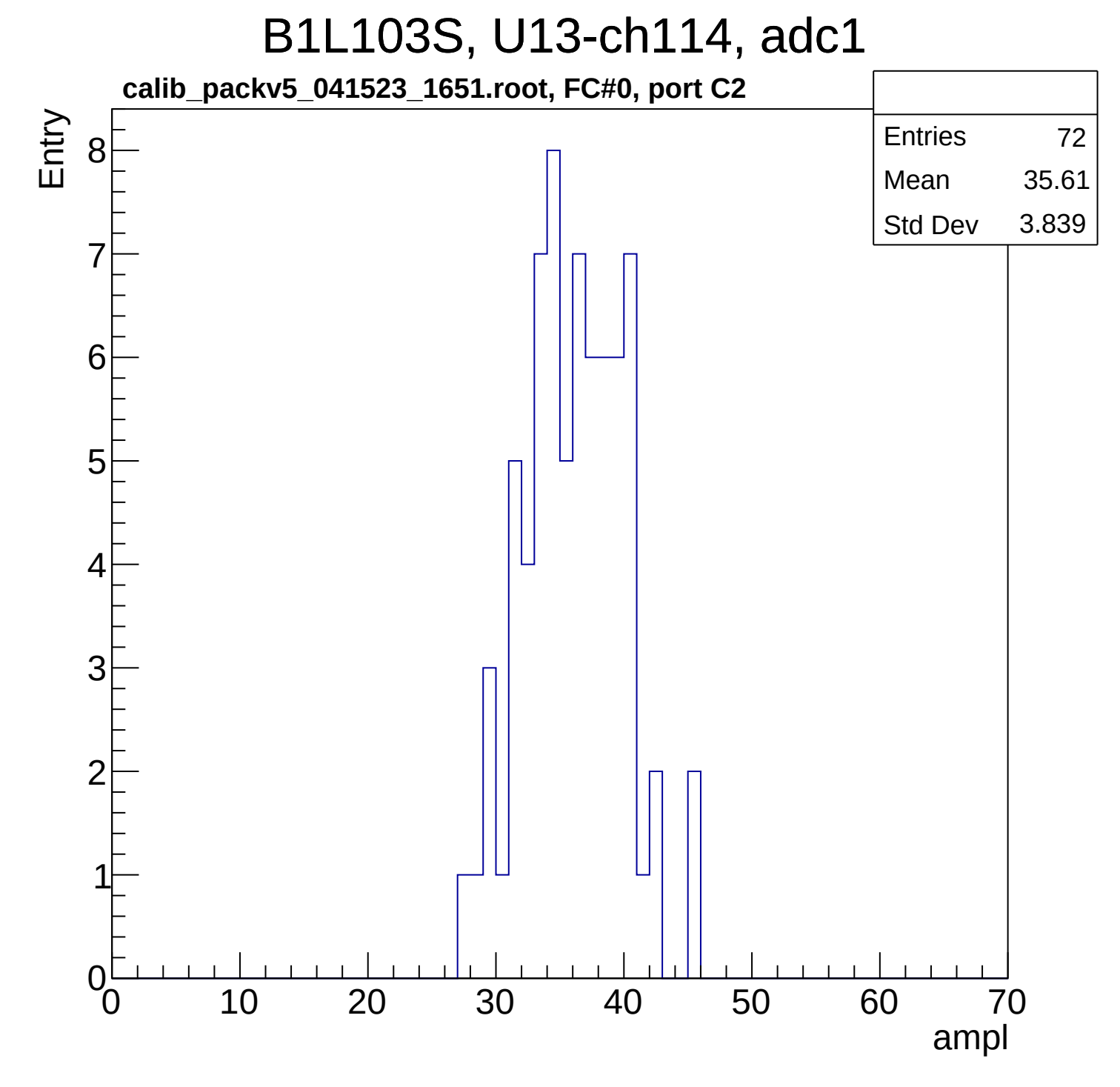
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch114, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 35.61
Std Dev 3.839
Entry
ampl
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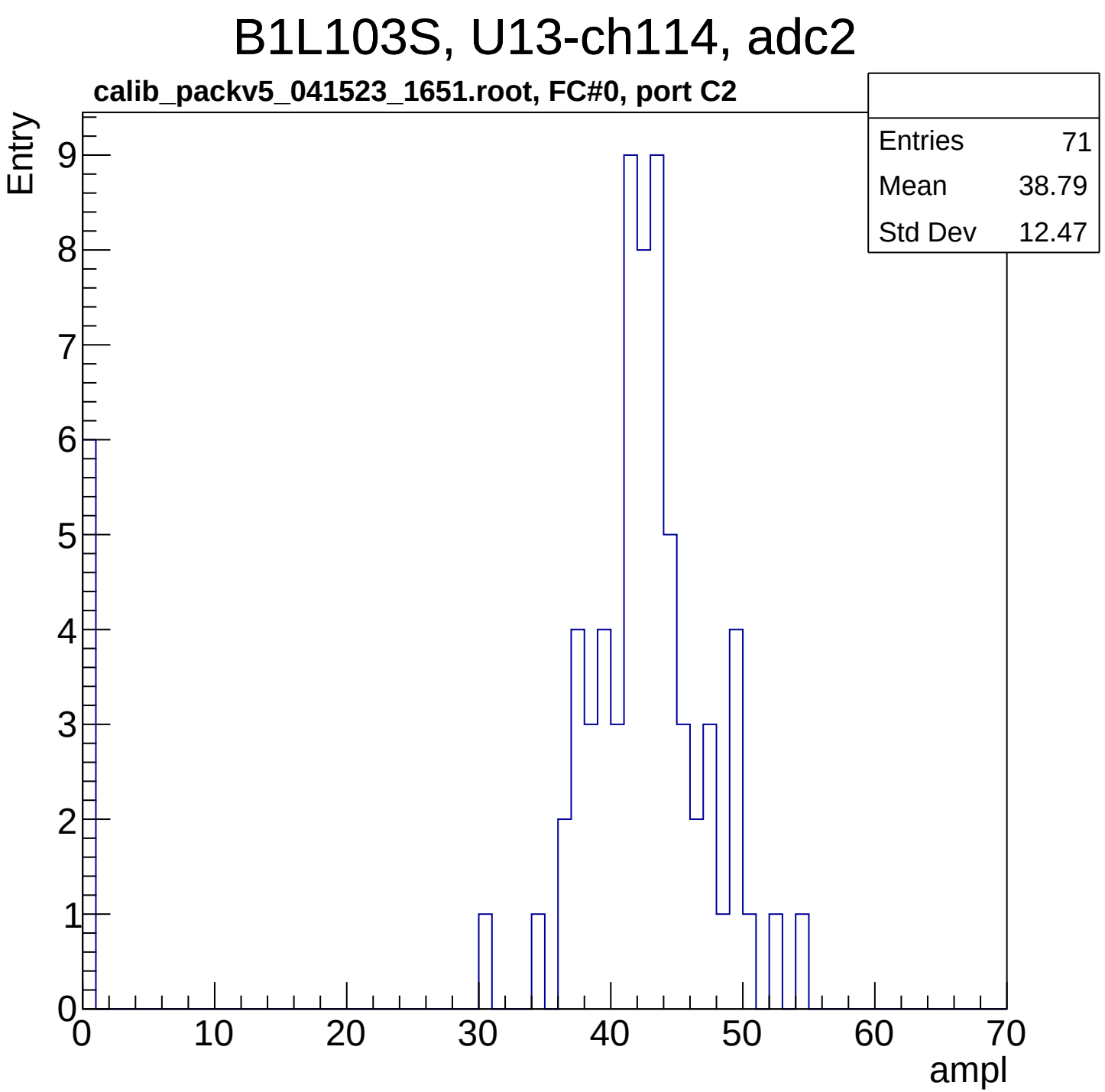
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch114, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 38.79
Std Dev 12.47
Entry
ampl
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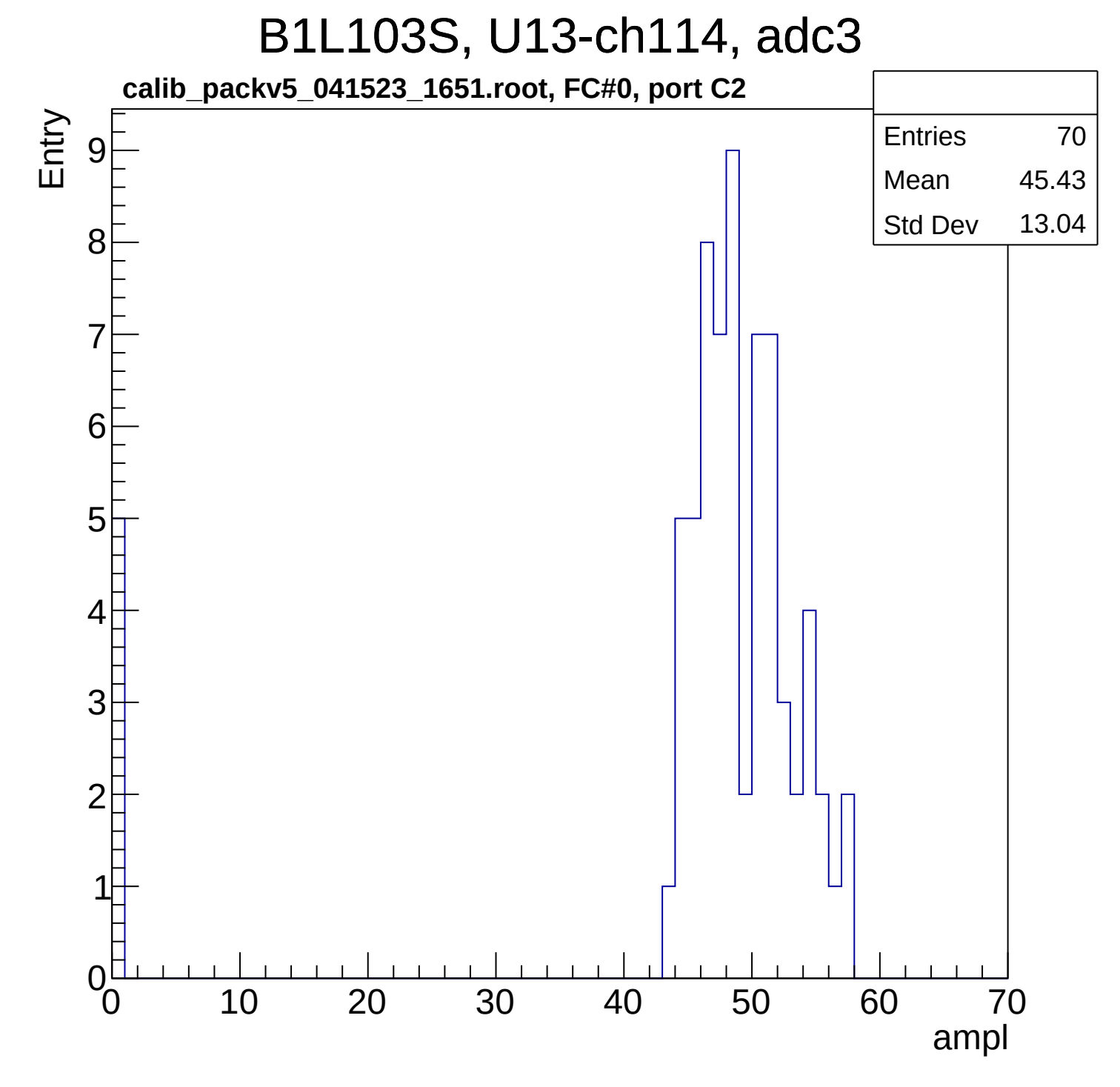
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch114, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 45.43
Std Dev 13.04
Entry
ampl
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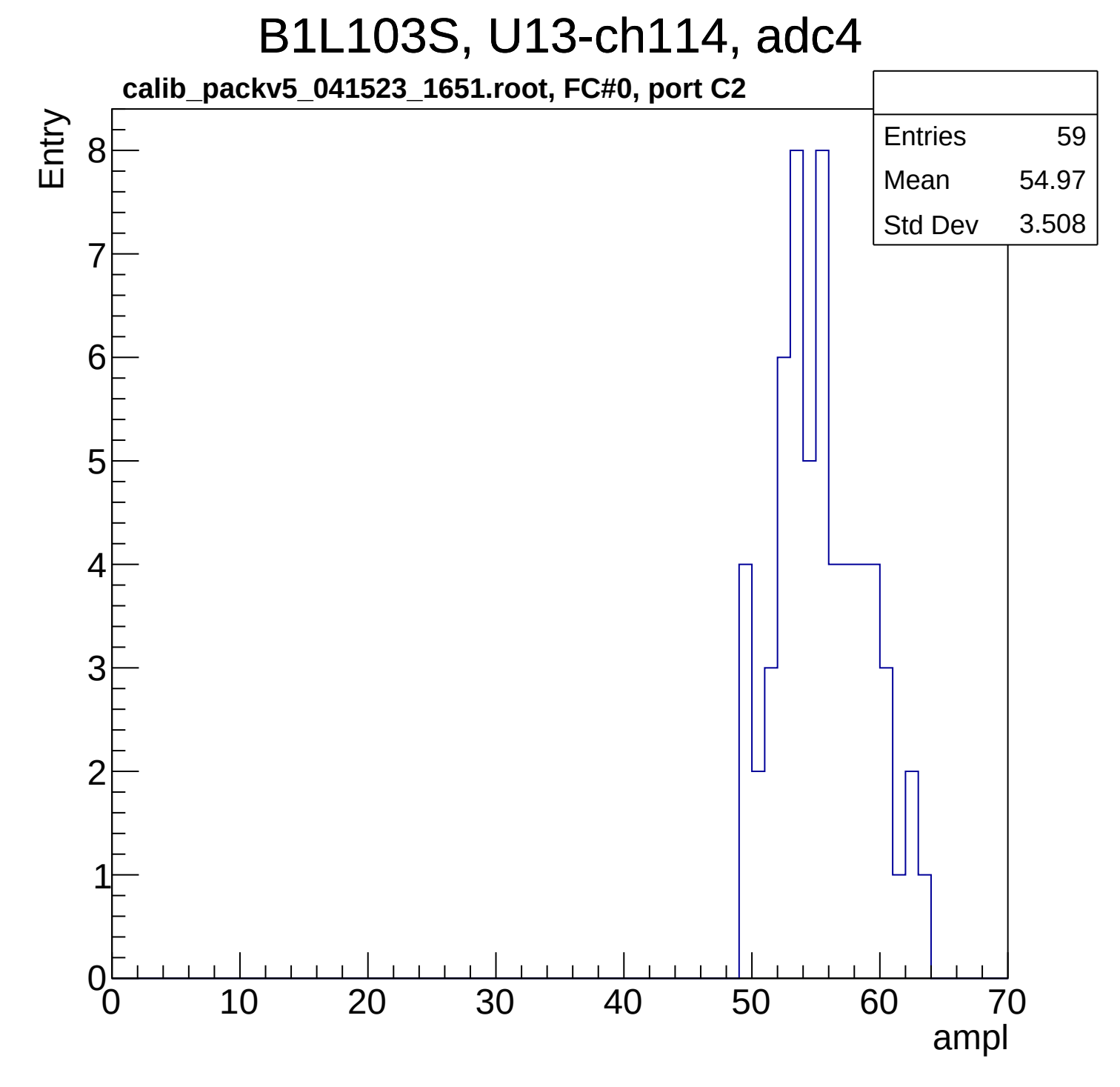
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch114, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.97
Std Dev 3.508
Entry
ampl
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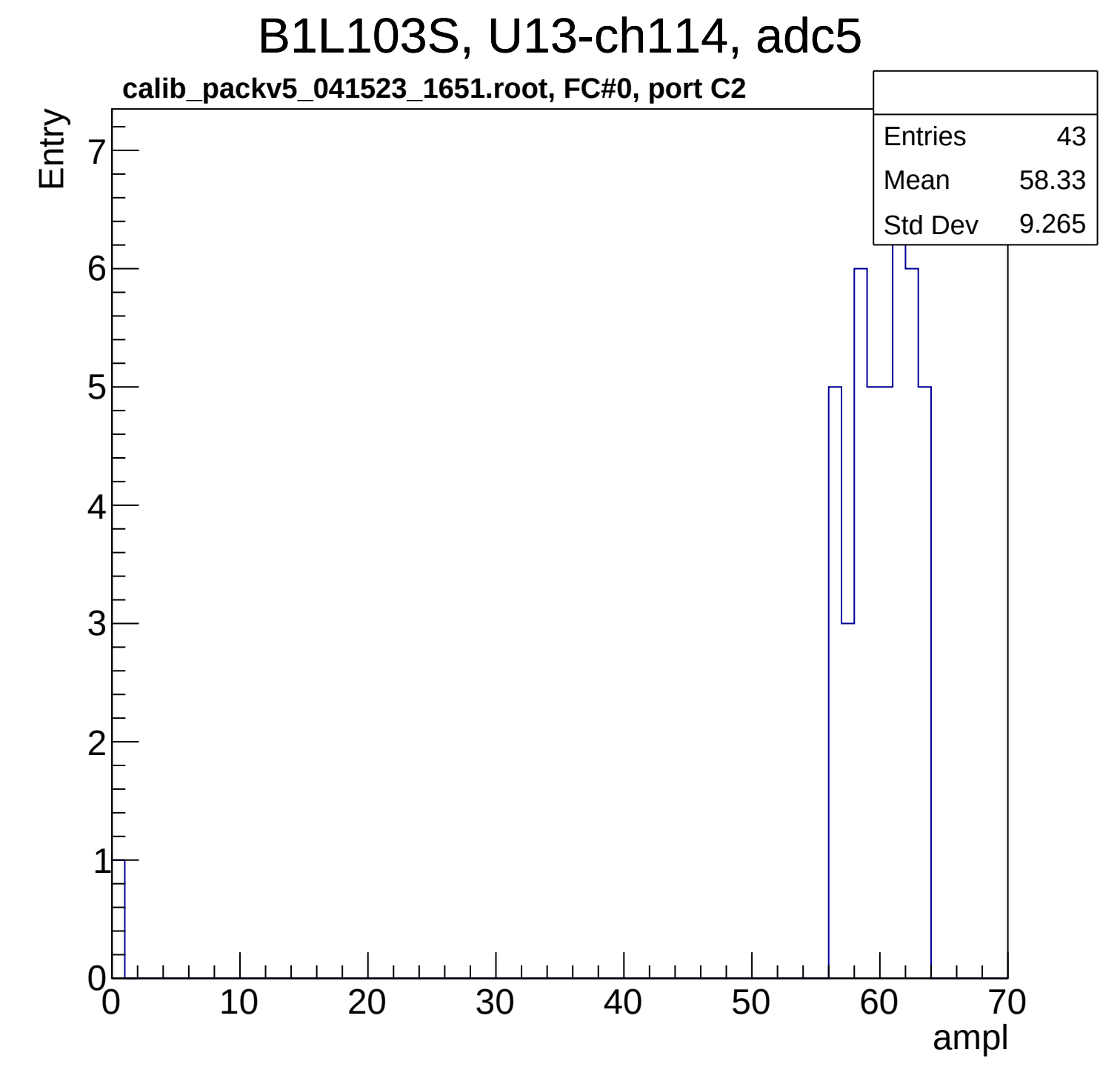
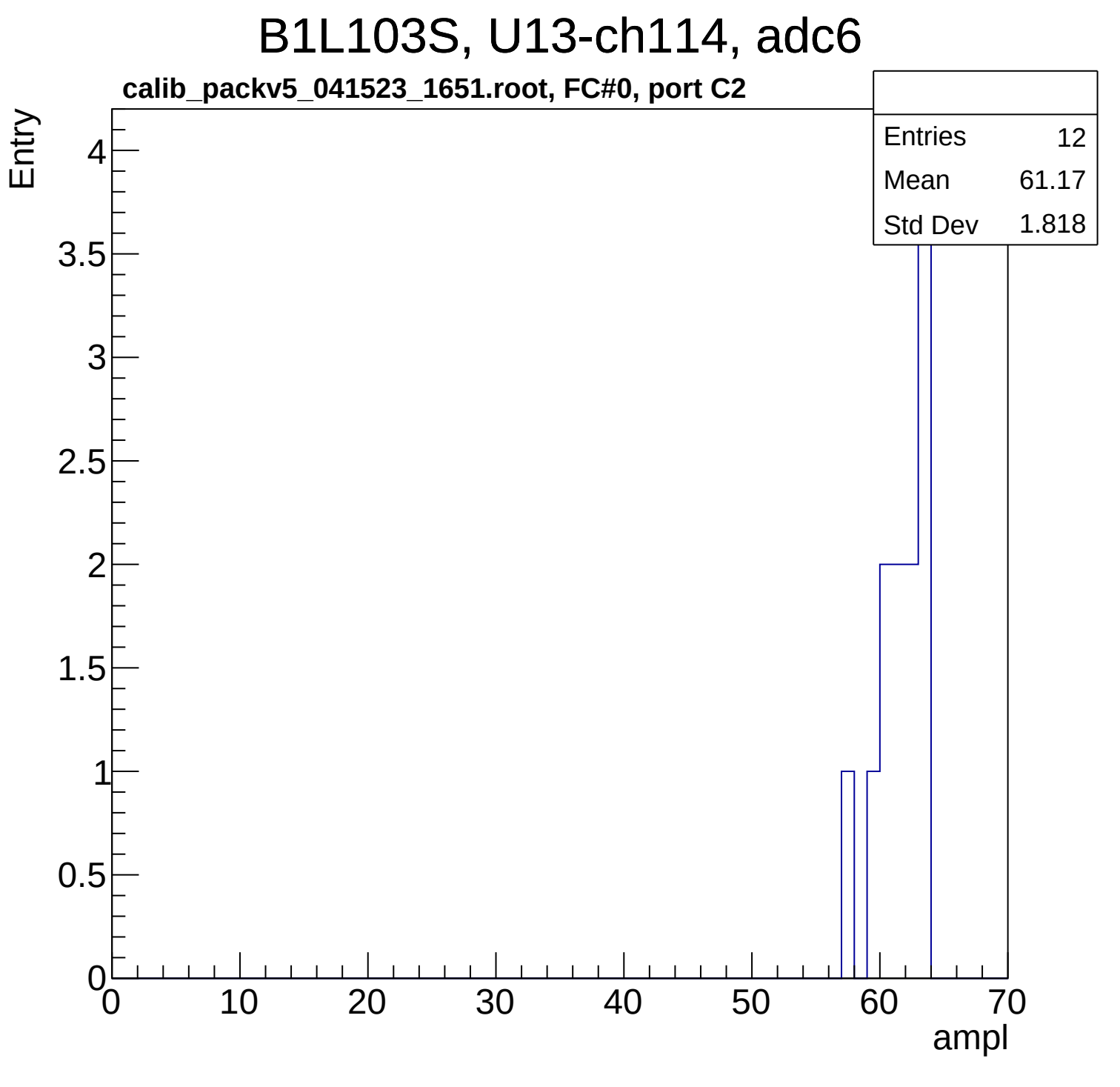
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch114, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 58.33
Std Dev 9.265
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch114, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.17
Std Dev 1.818
Entry
ampl
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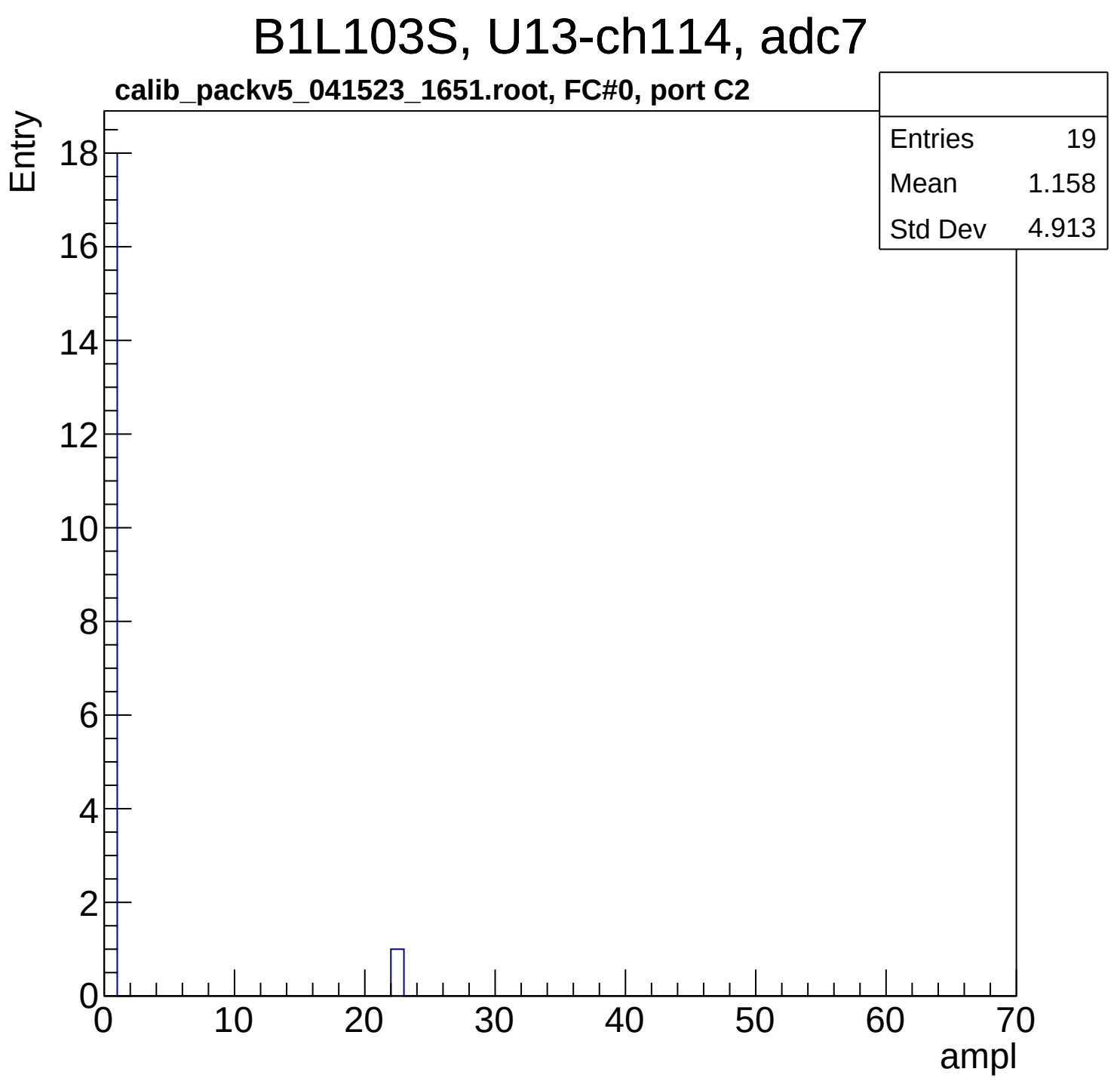
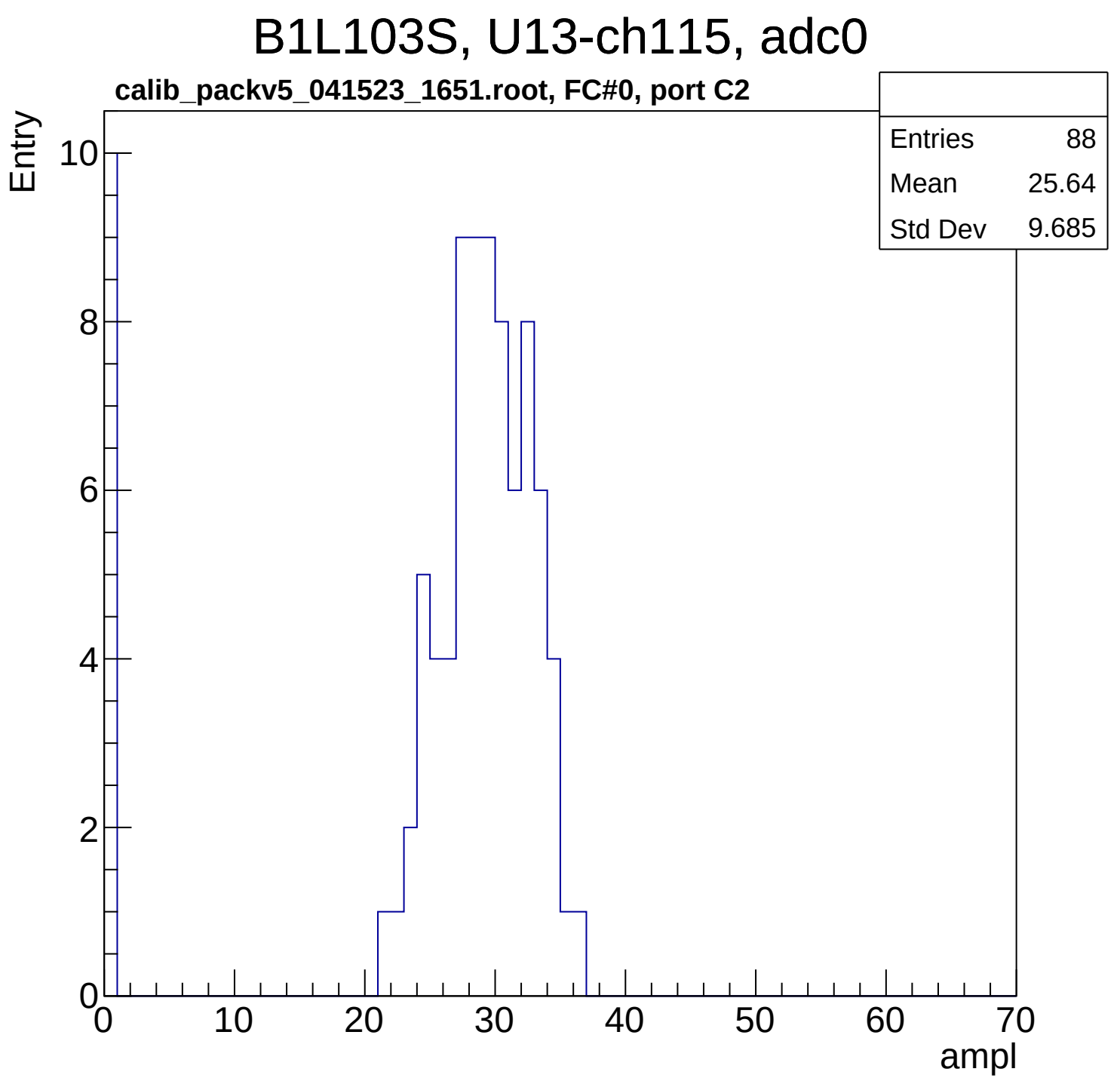
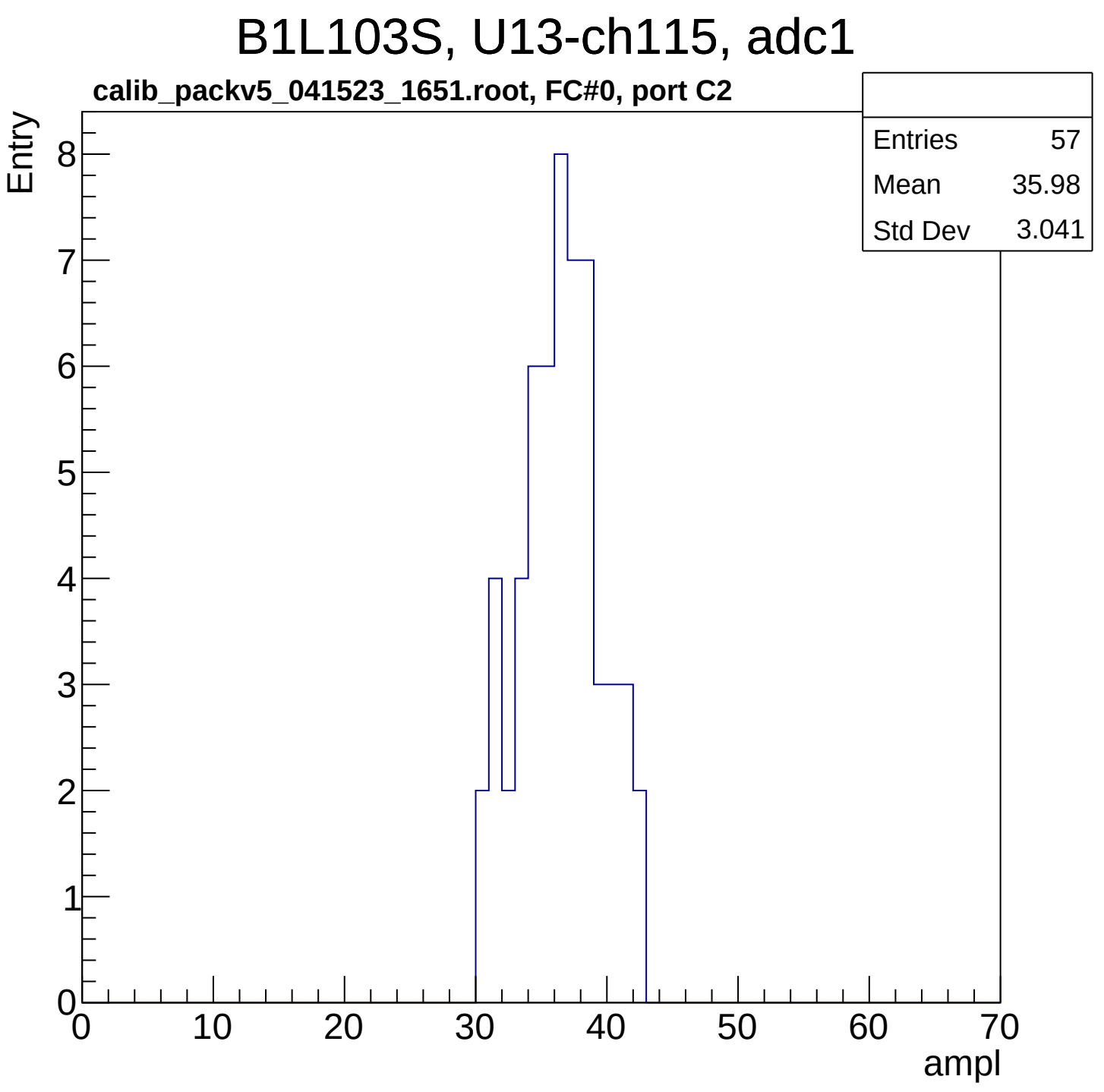
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U13-ch114, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch115, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 25.64
Std Dev 9.685
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch115, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 35.98
Std Dev 3.041
Entry
ampl
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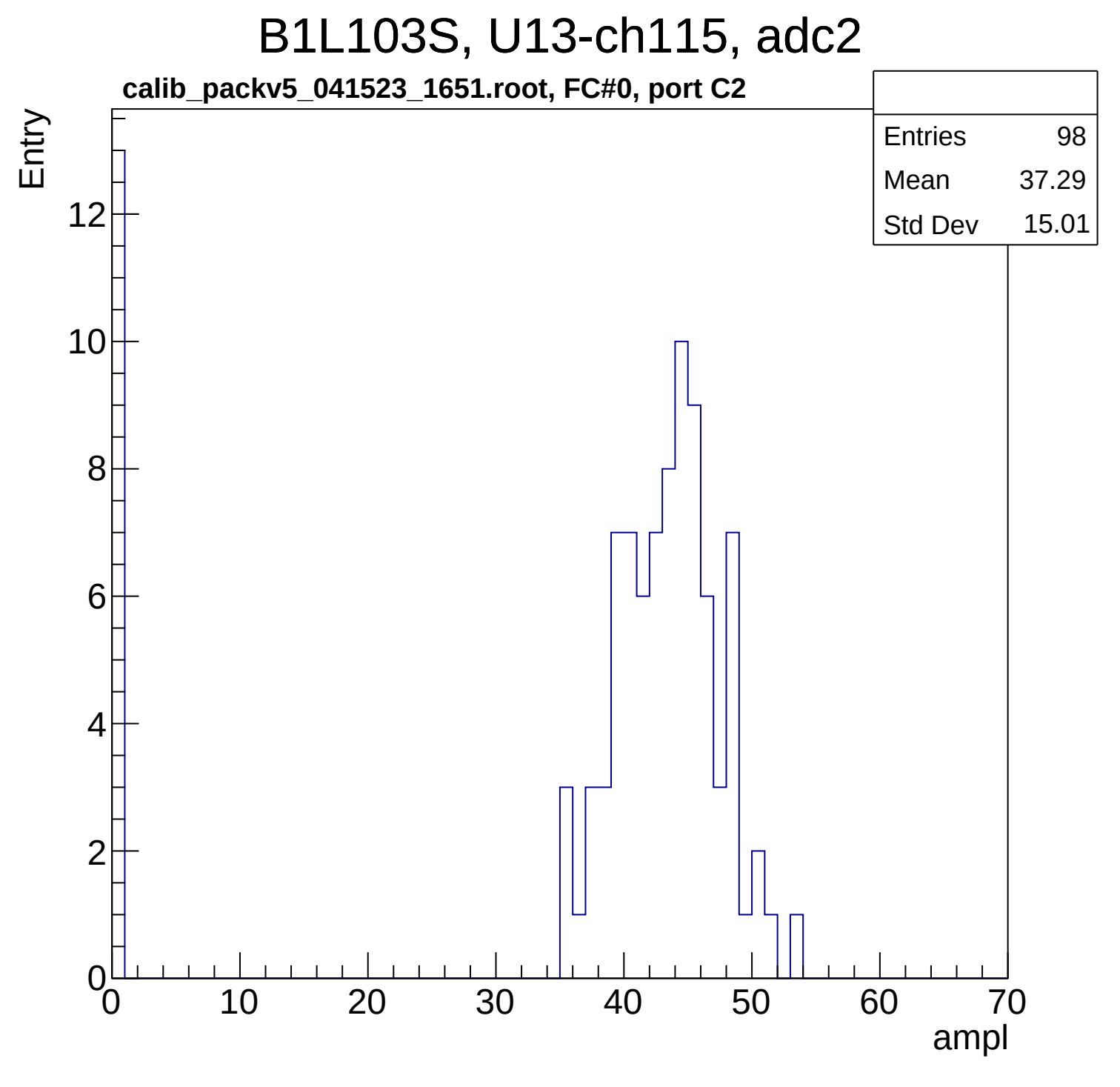
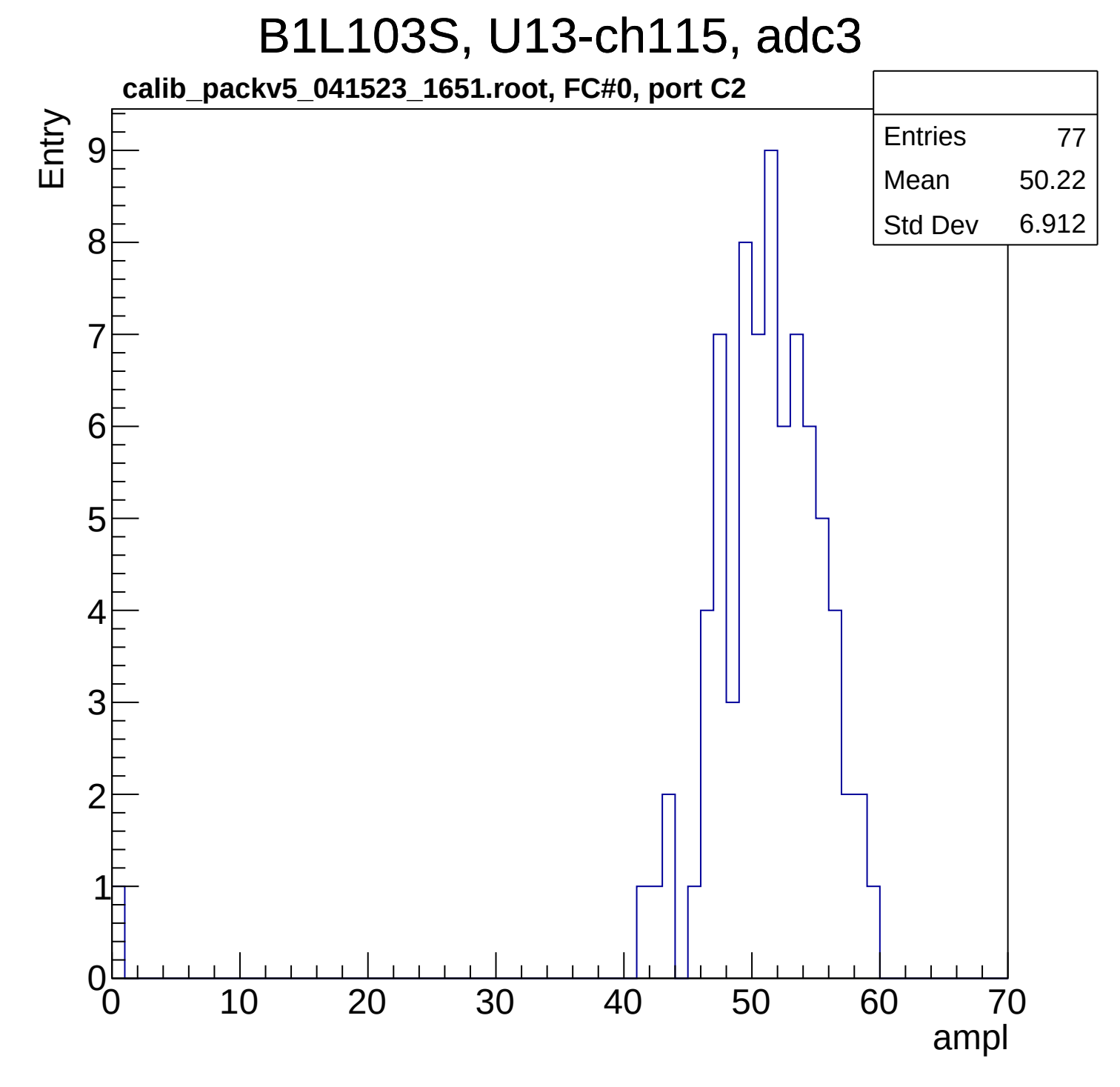
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch115, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 37.29
Std Dev 15.01
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch115, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 50.22
Std Dev 6.912
Entry
ampl
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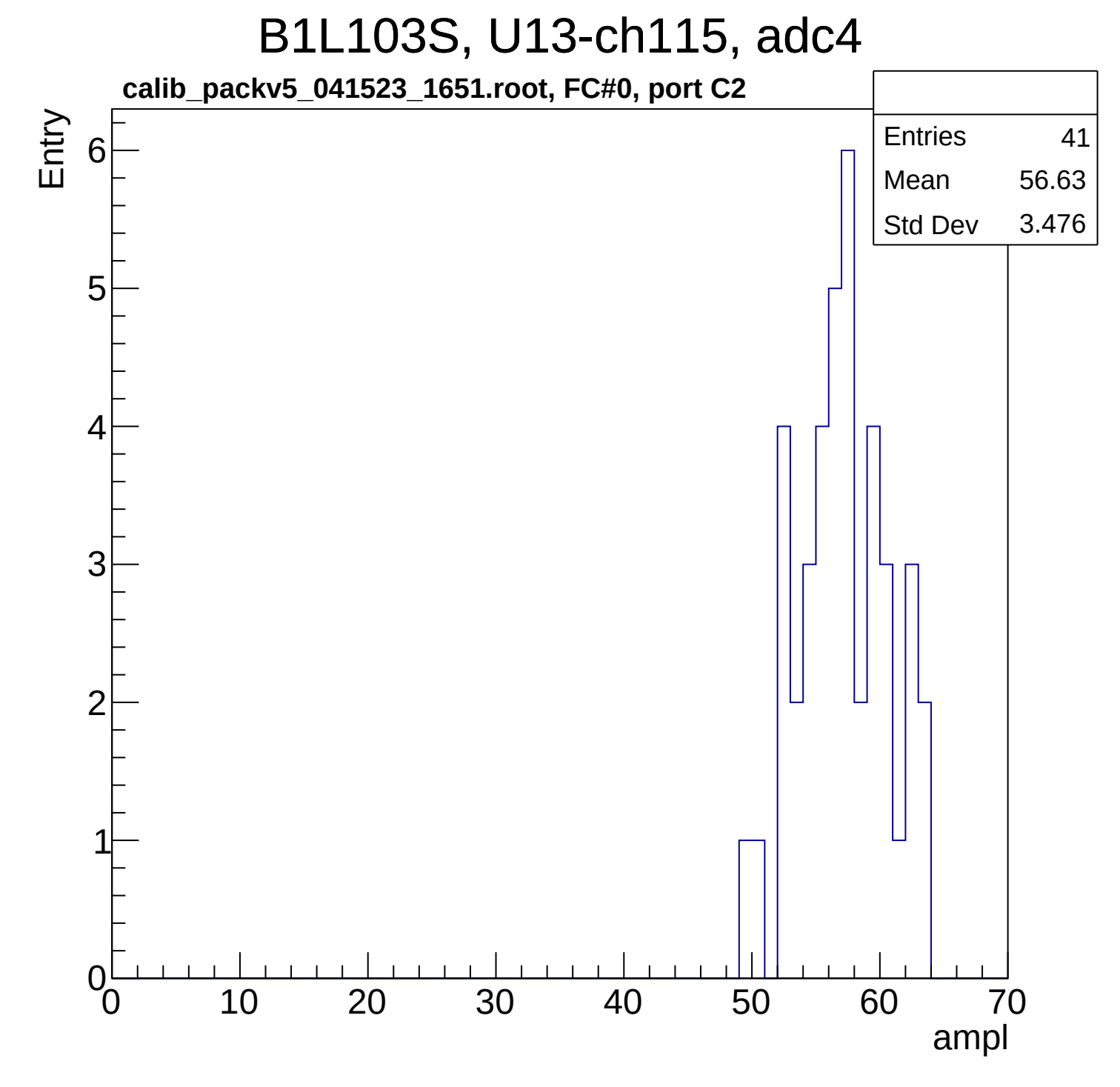
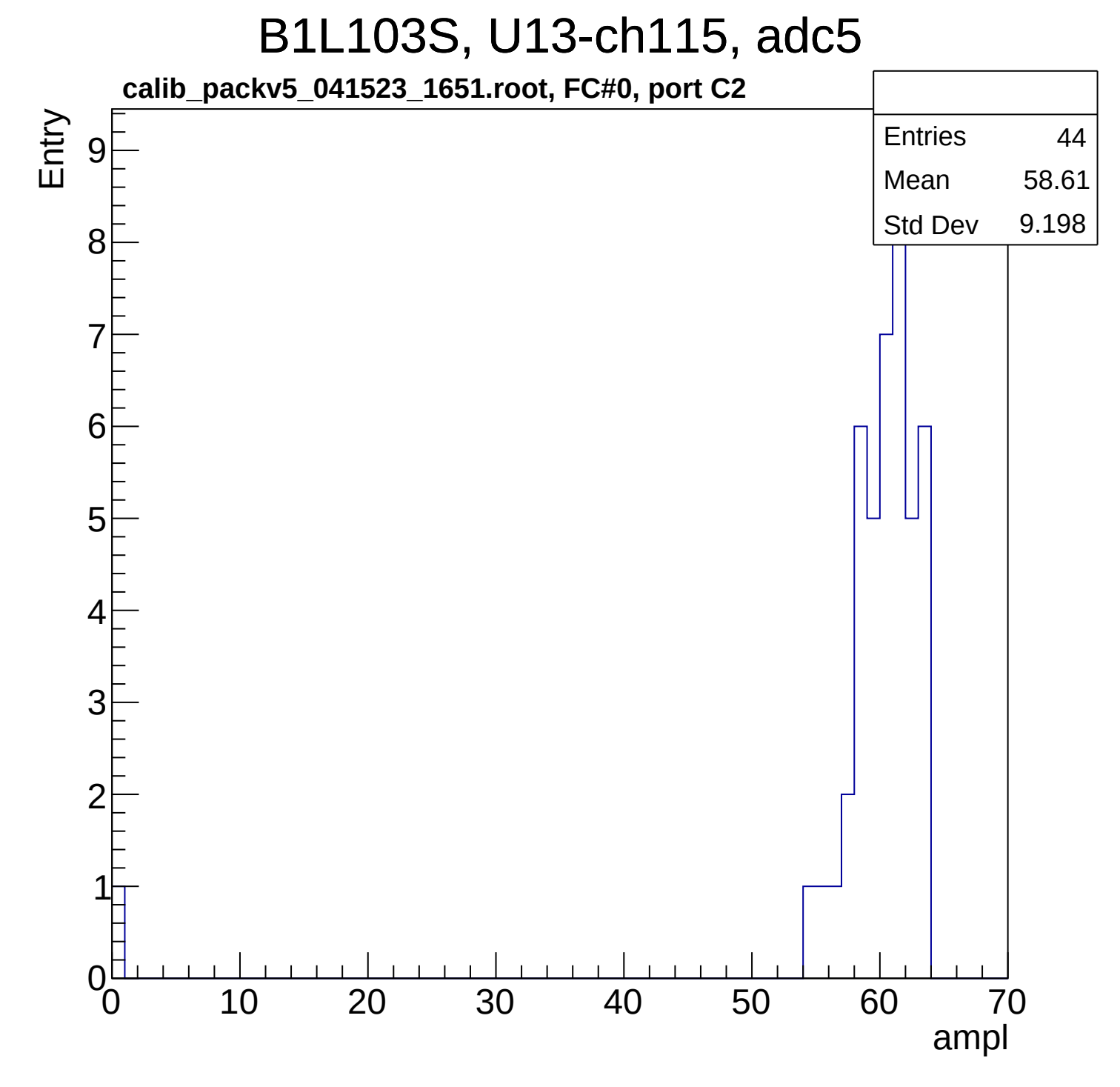
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U13-ch115, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 56.63
Std Dev 3.476
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U13-ch115, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 58.61
Std Dev 9.198
Entry
ampl
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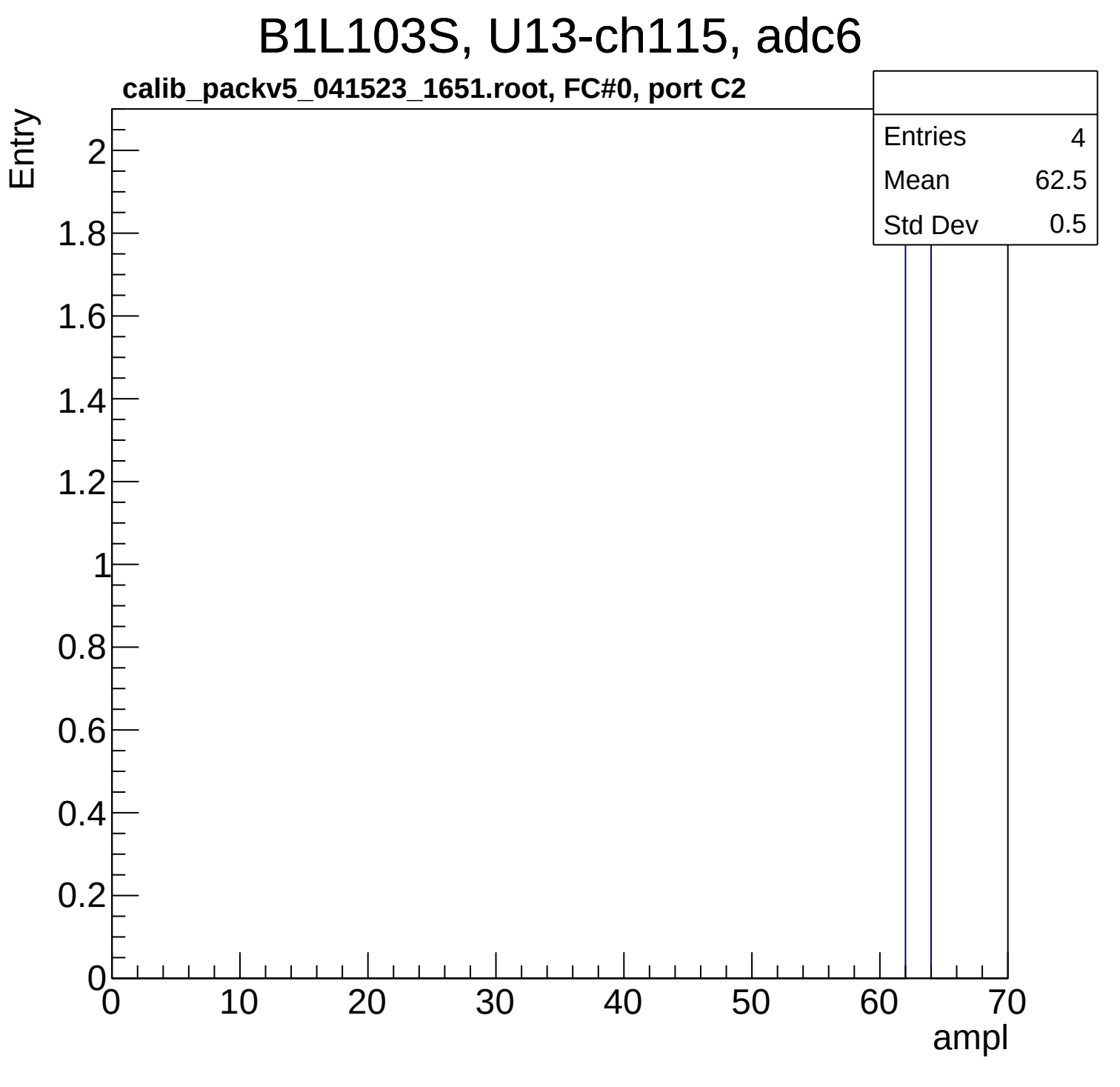
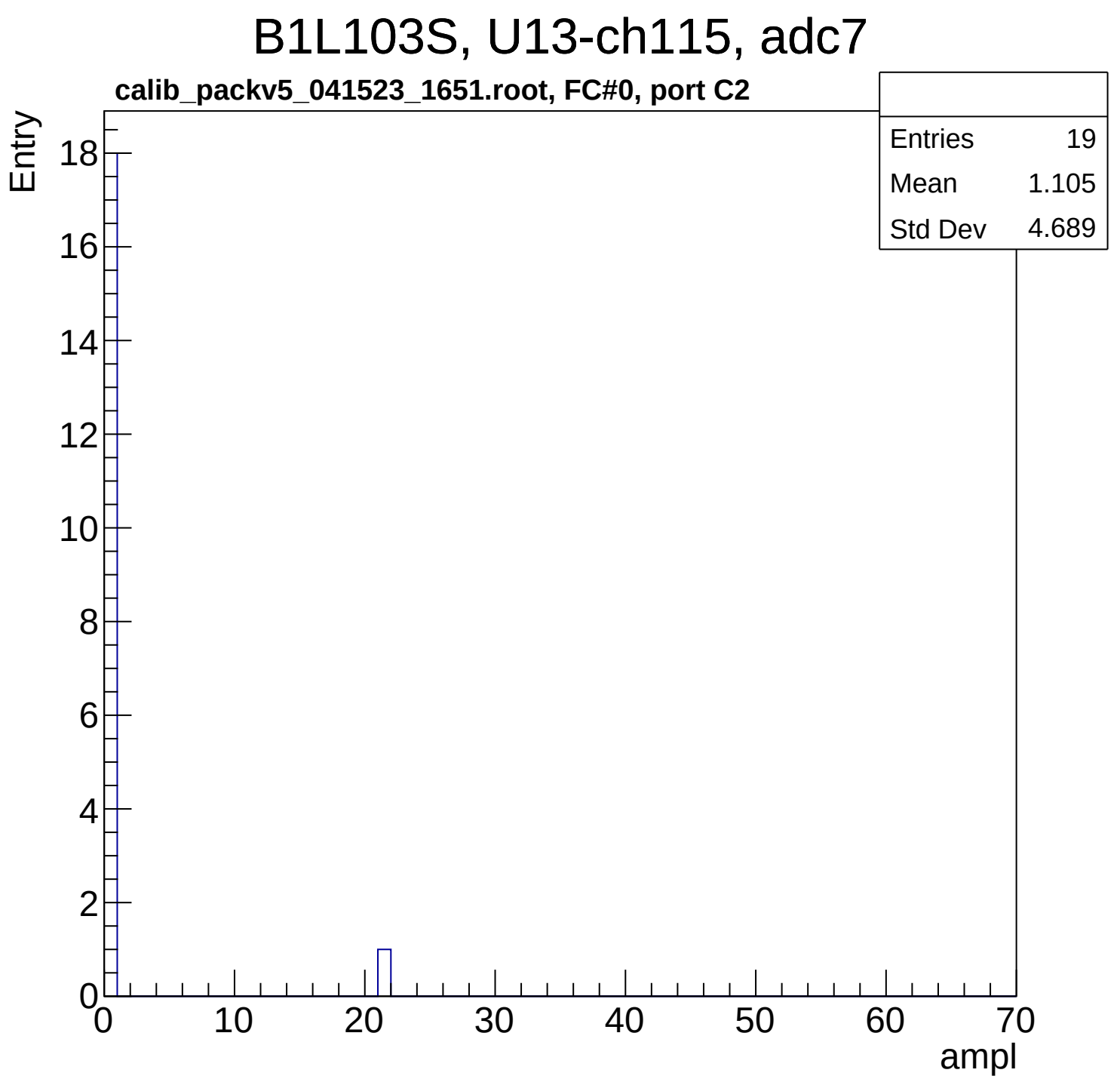
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch115, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.5
Std Dev 0.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U13-ch115, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
ampl
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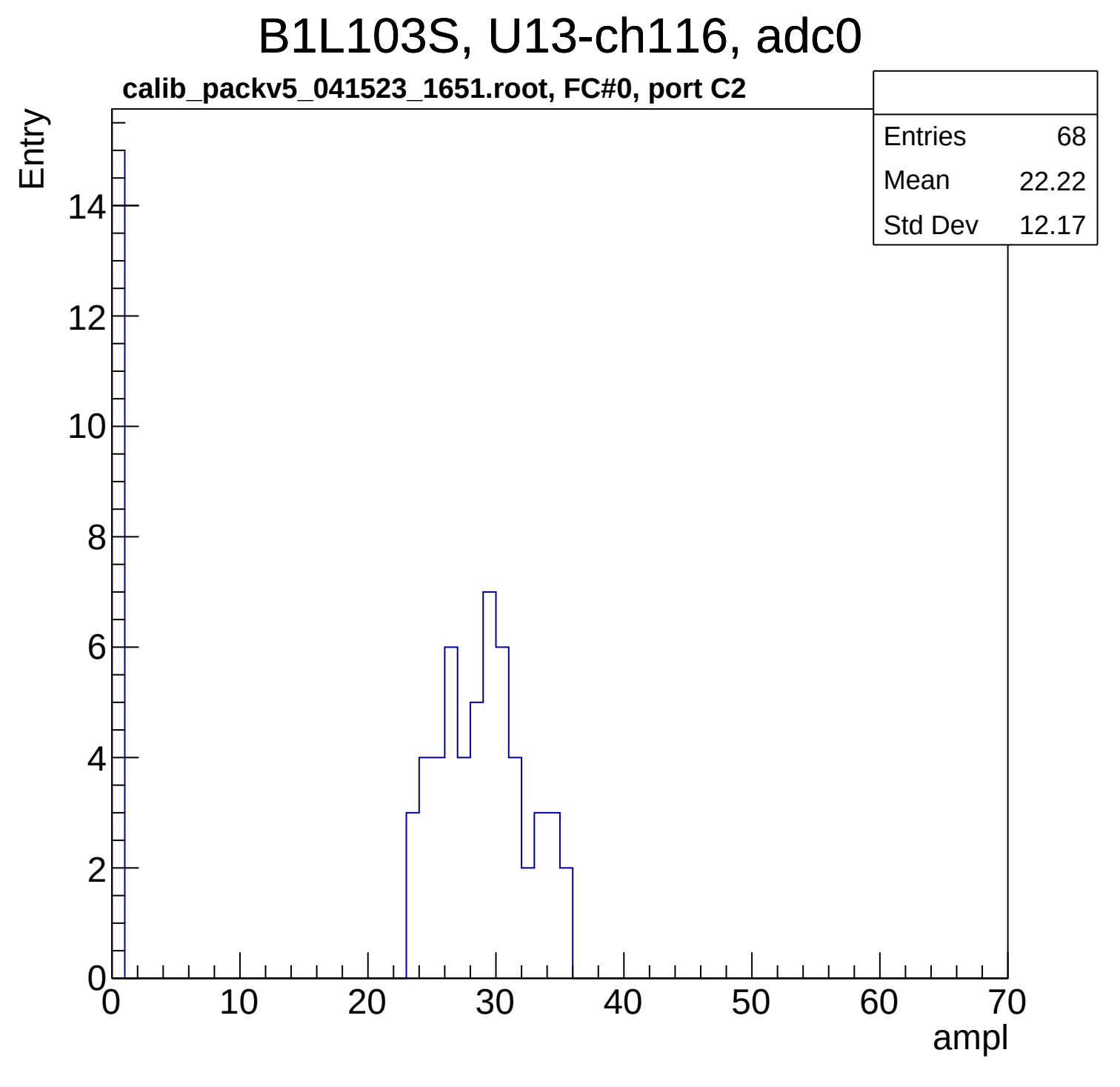
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L103S, U13-ch116, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 22.22
Std Dev 12.17
Entry
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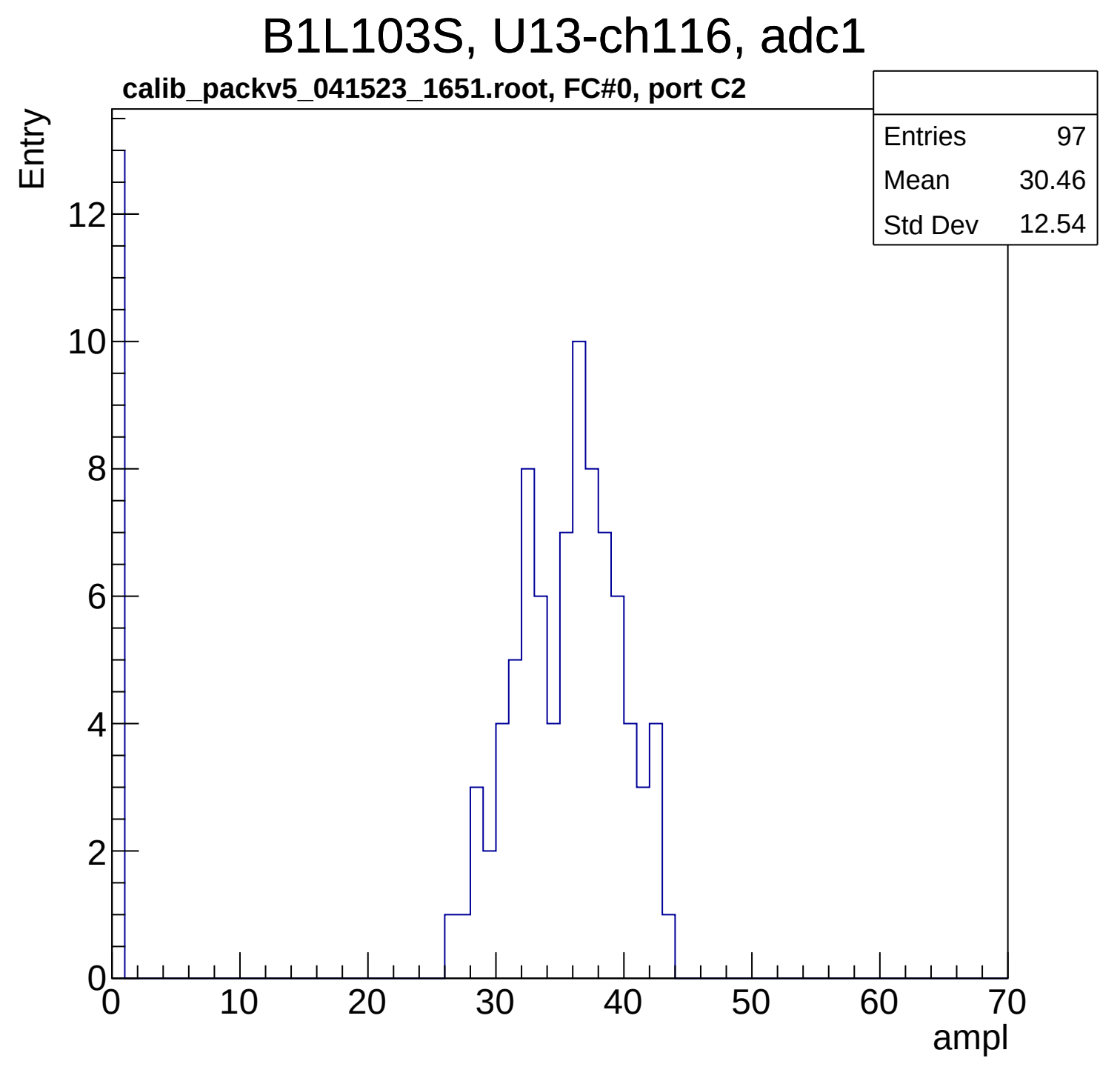
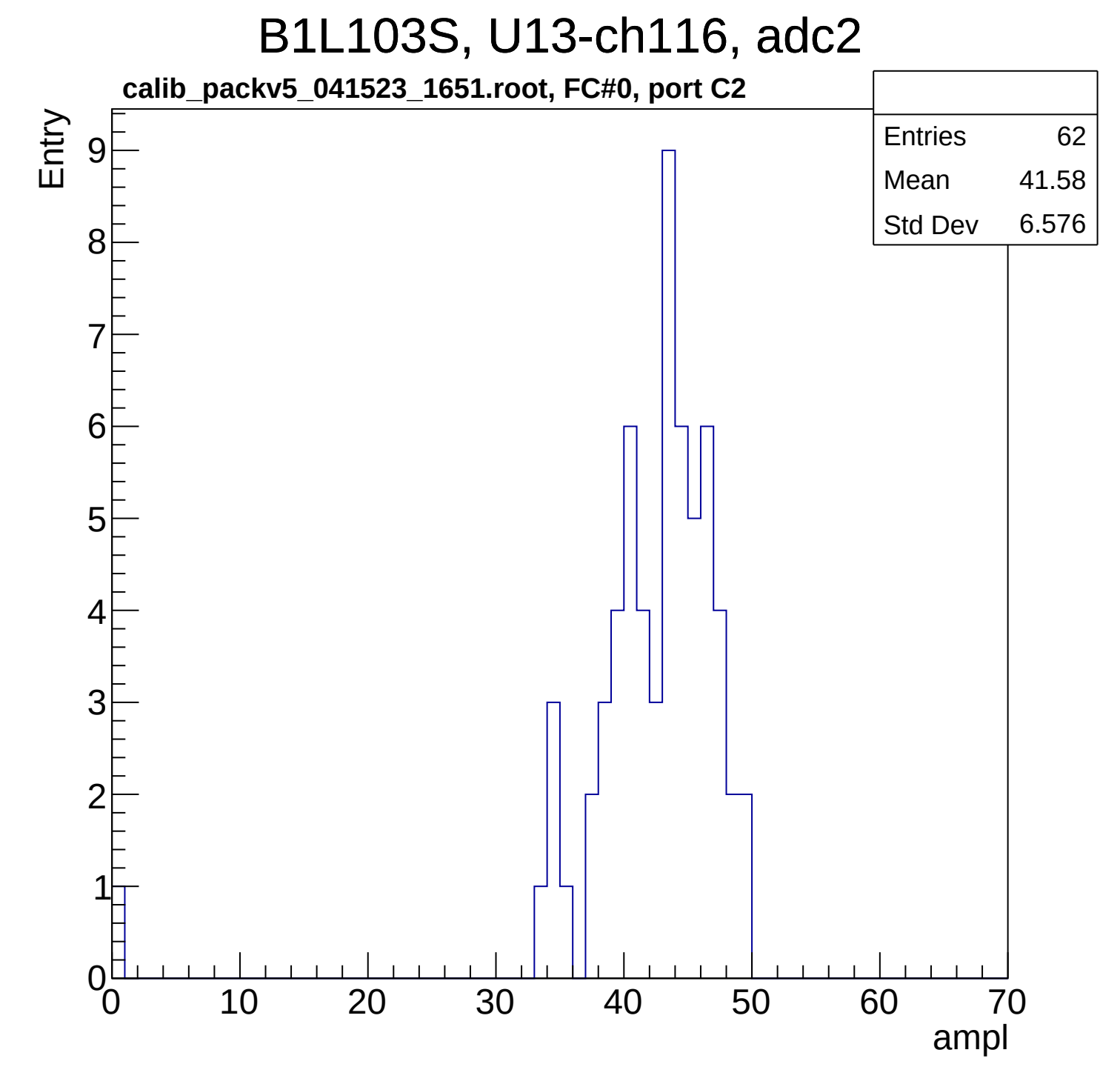
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch116, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 30.46
Std Dev 12.54
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch116, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 41.58
Std Dev 6.576
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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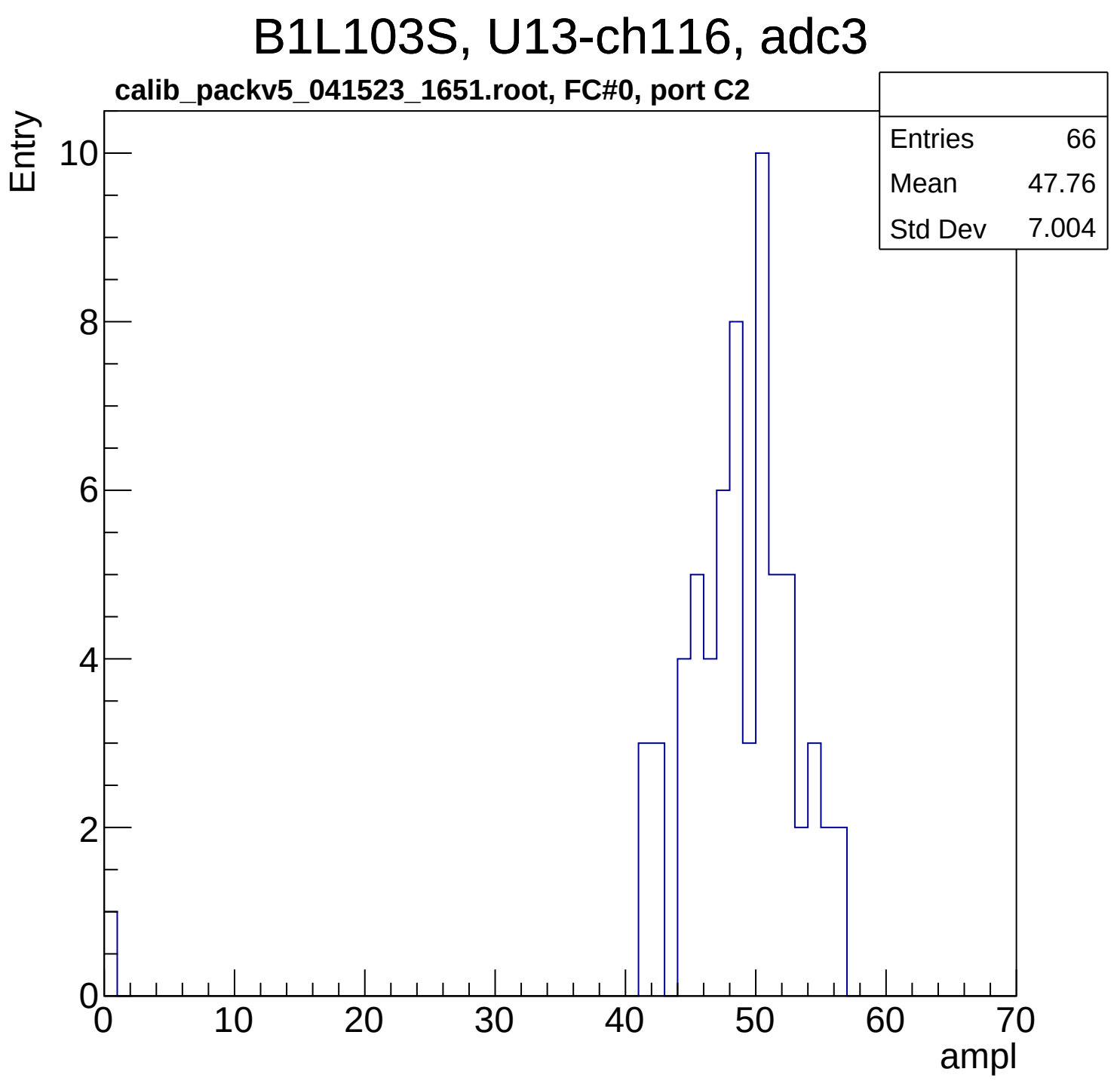
B1L103S, U13-ch116, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 47.76
Std Dev 7.004
Entry
ampl
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2
4
6
8
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0
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40
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60
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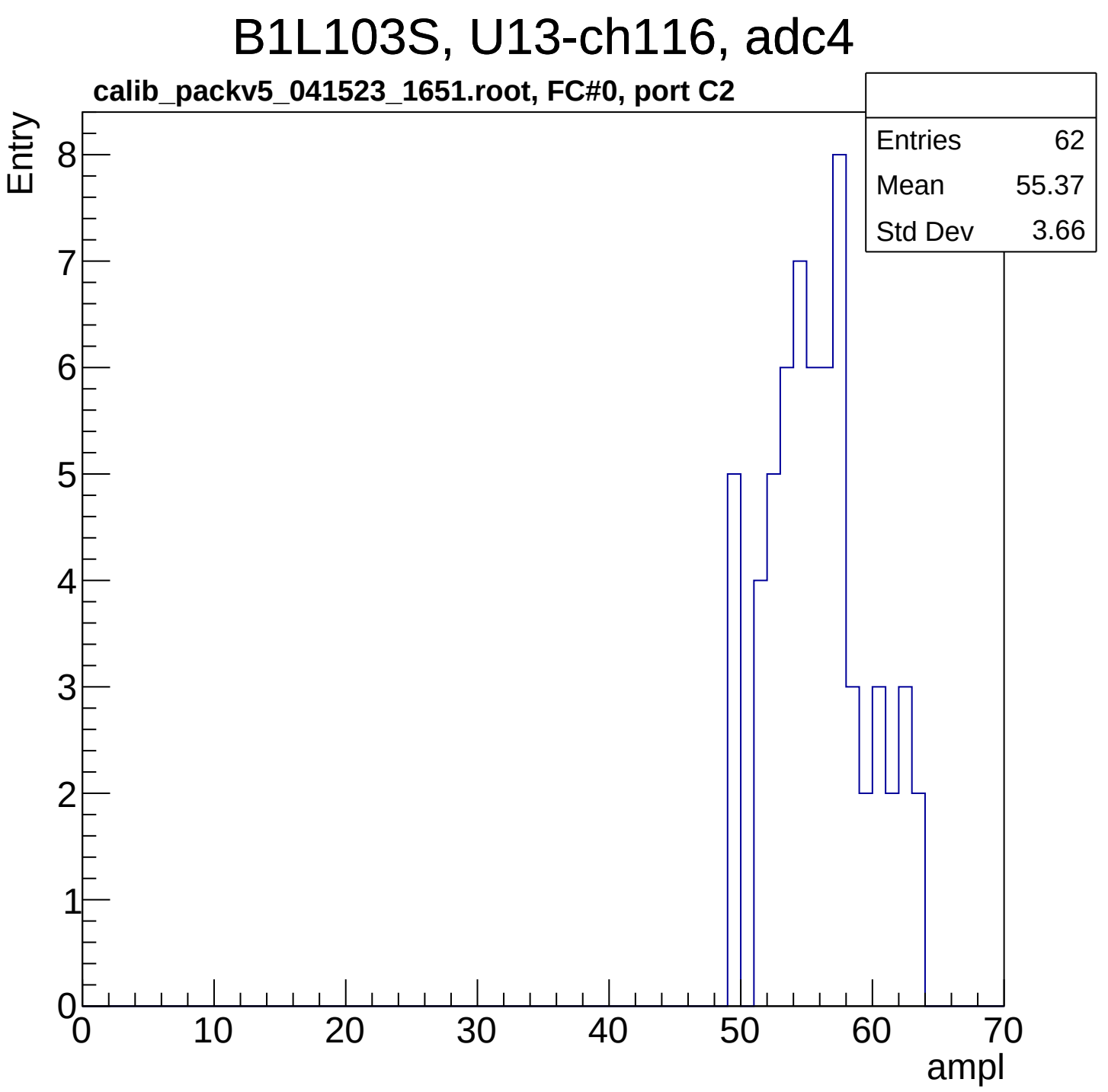
B1L103S, U13-ch116, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 55.37
Std Dev 3.66
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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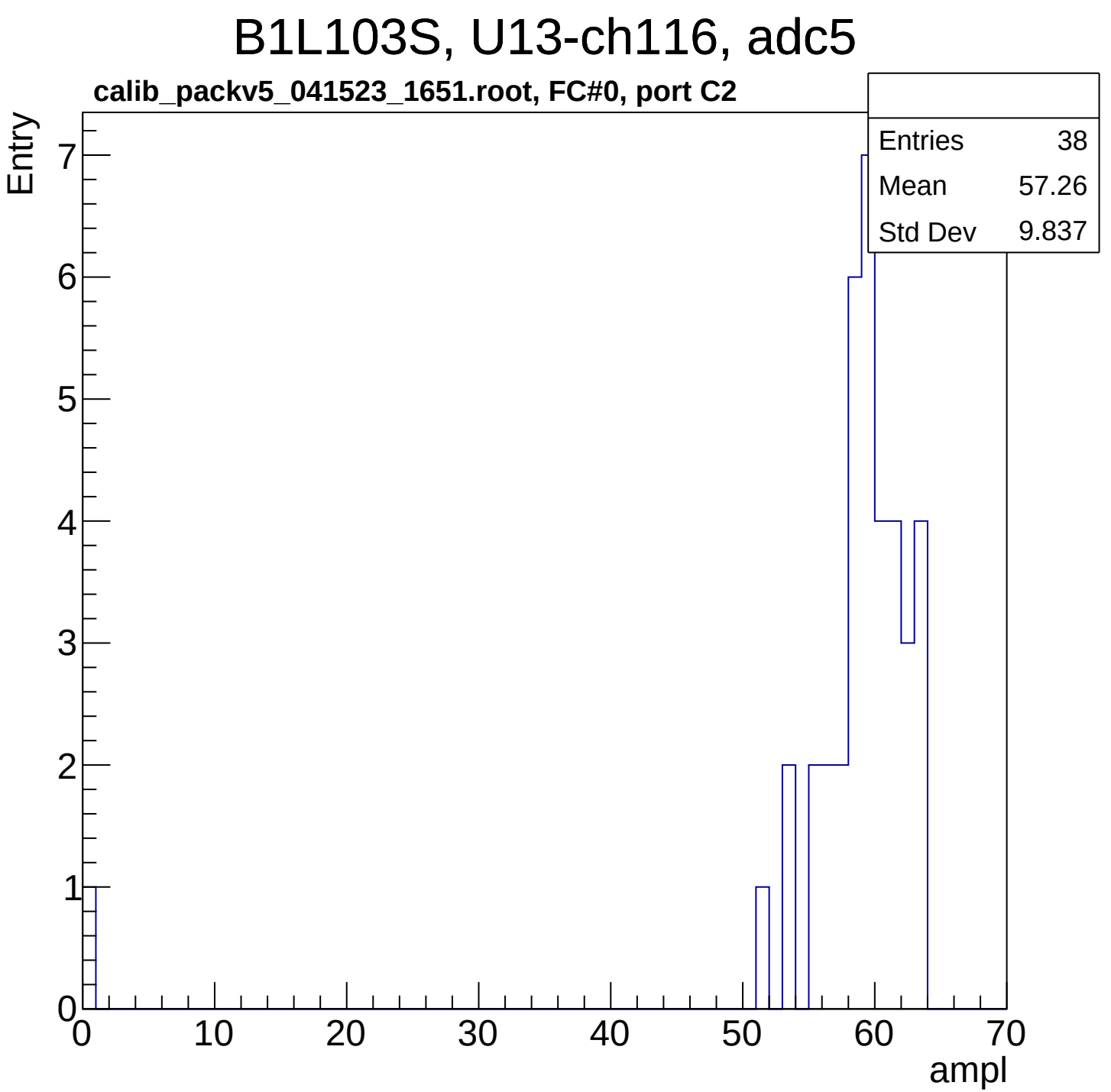
B1L103S, U13-ch116, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 57.26
Std Dev 9.837
Entry
ampl
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2
3
4
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6
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0
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40
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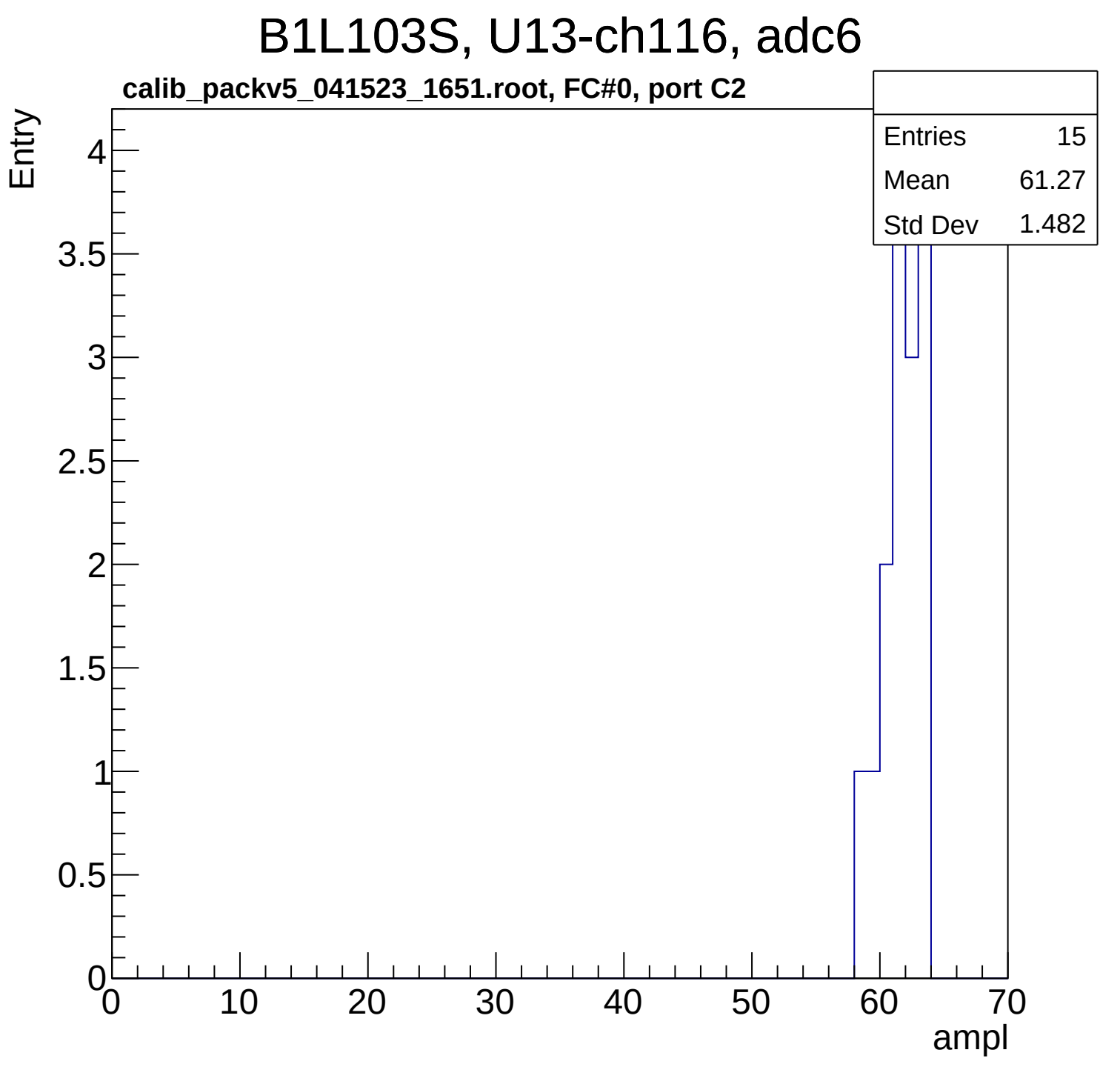
B1L103S, U13-ch116, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.27
Std Dev 1.482
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
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60
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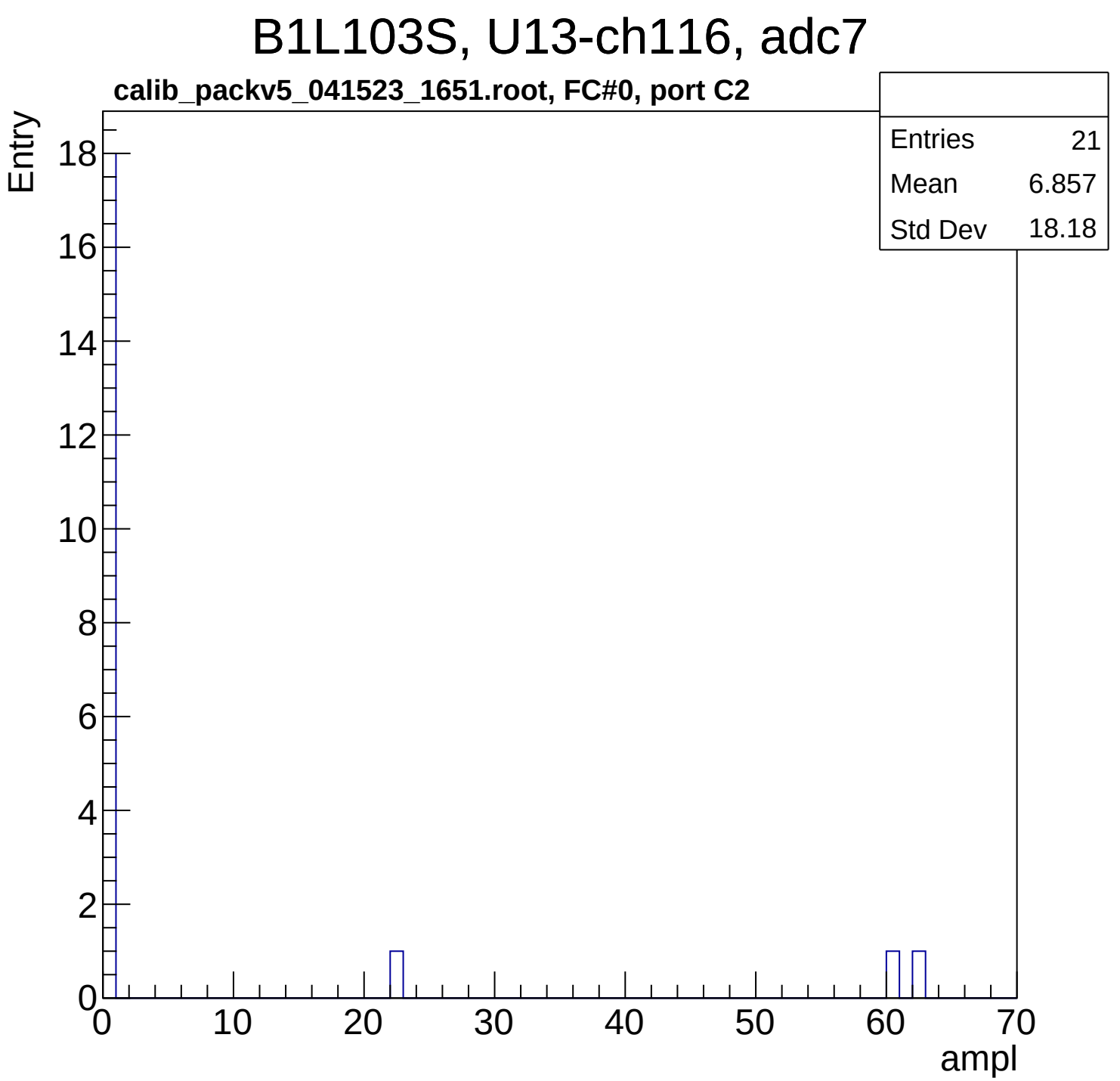
B1L103S, U13-ch116, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6.857
Std Dev 18.18
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
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40
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60
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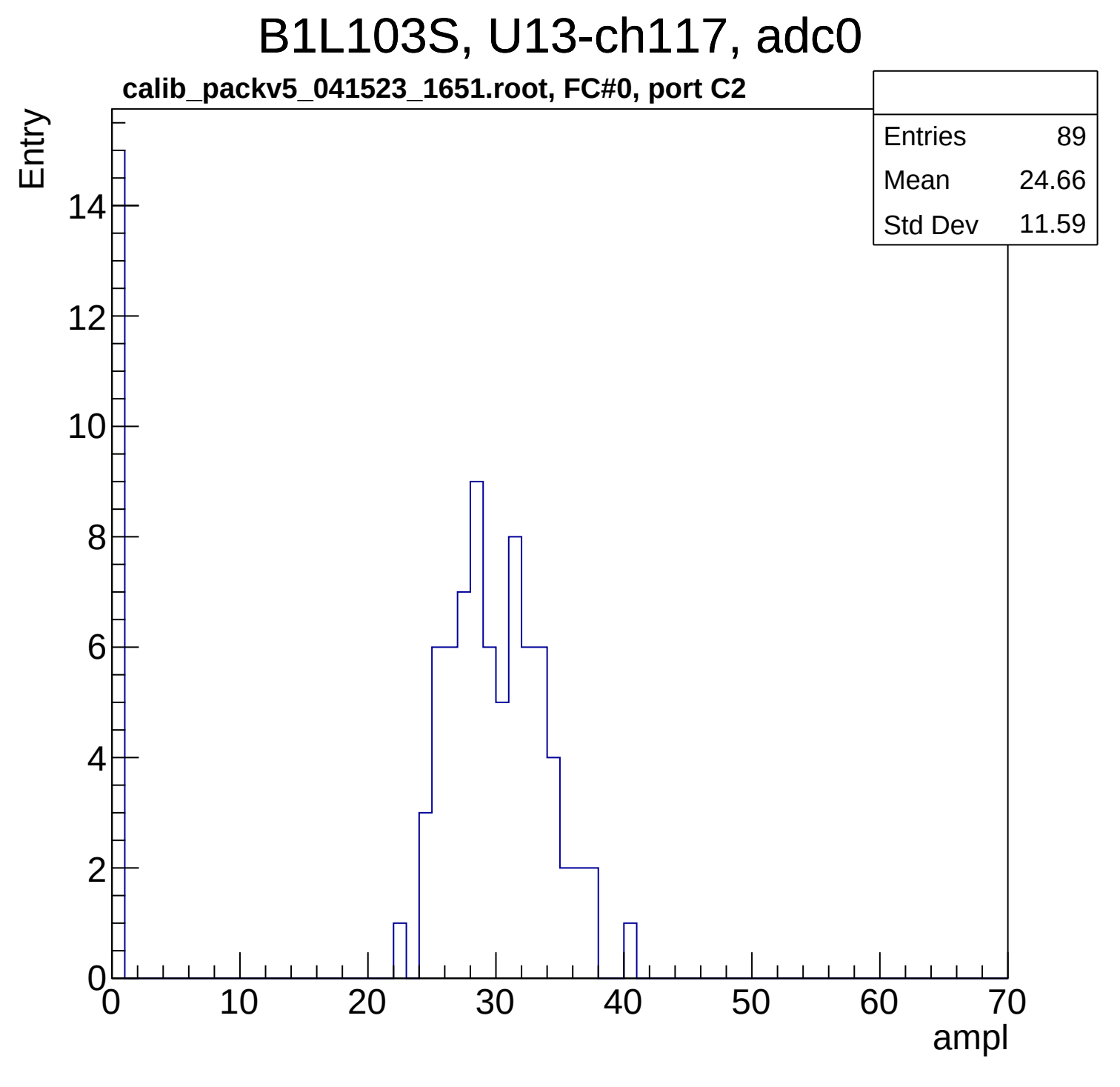
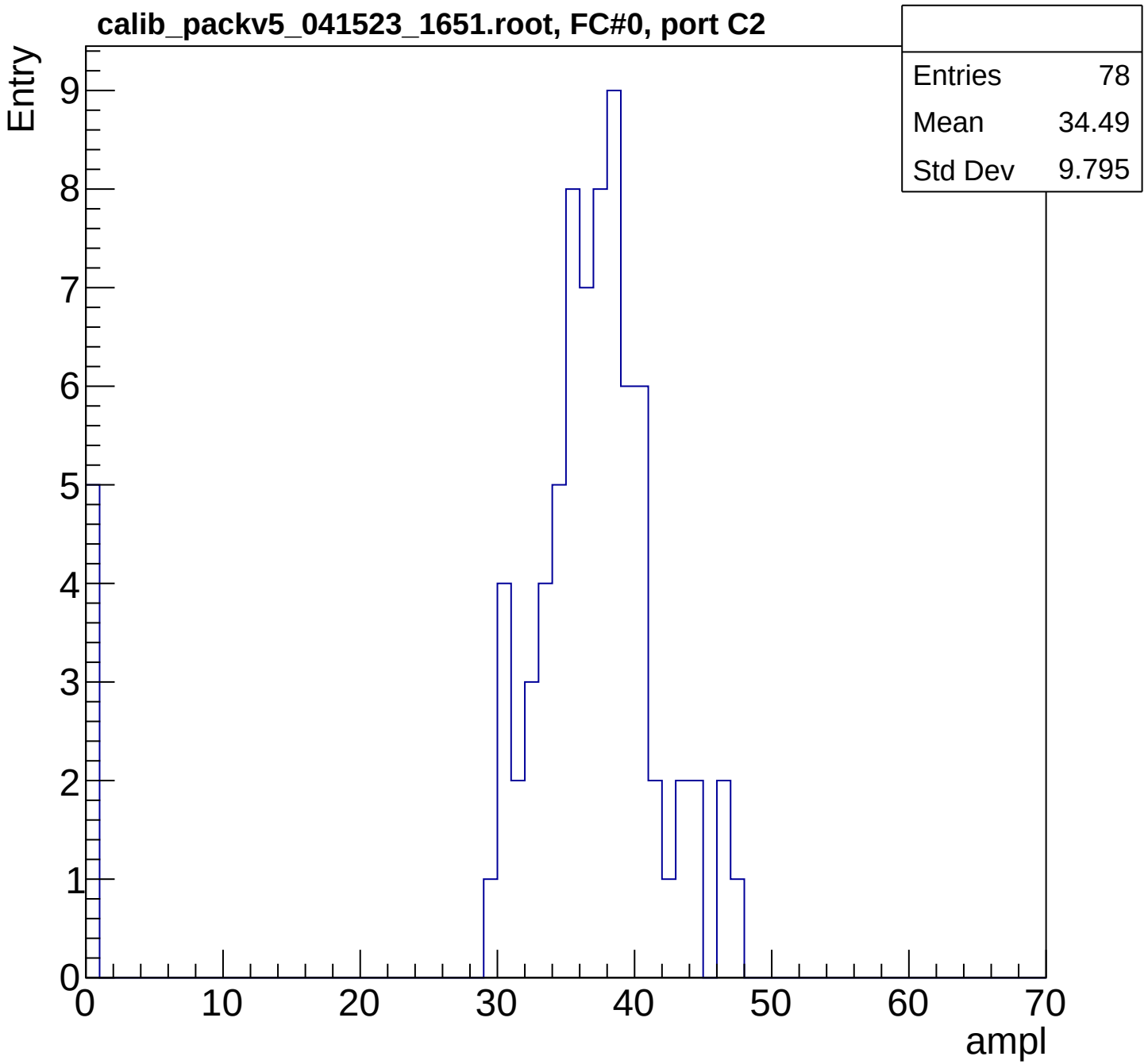

B1L103S, U13-ch117, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 24.66
Std Dev 11.59
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch117, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 34.49
Std Dev 9.795
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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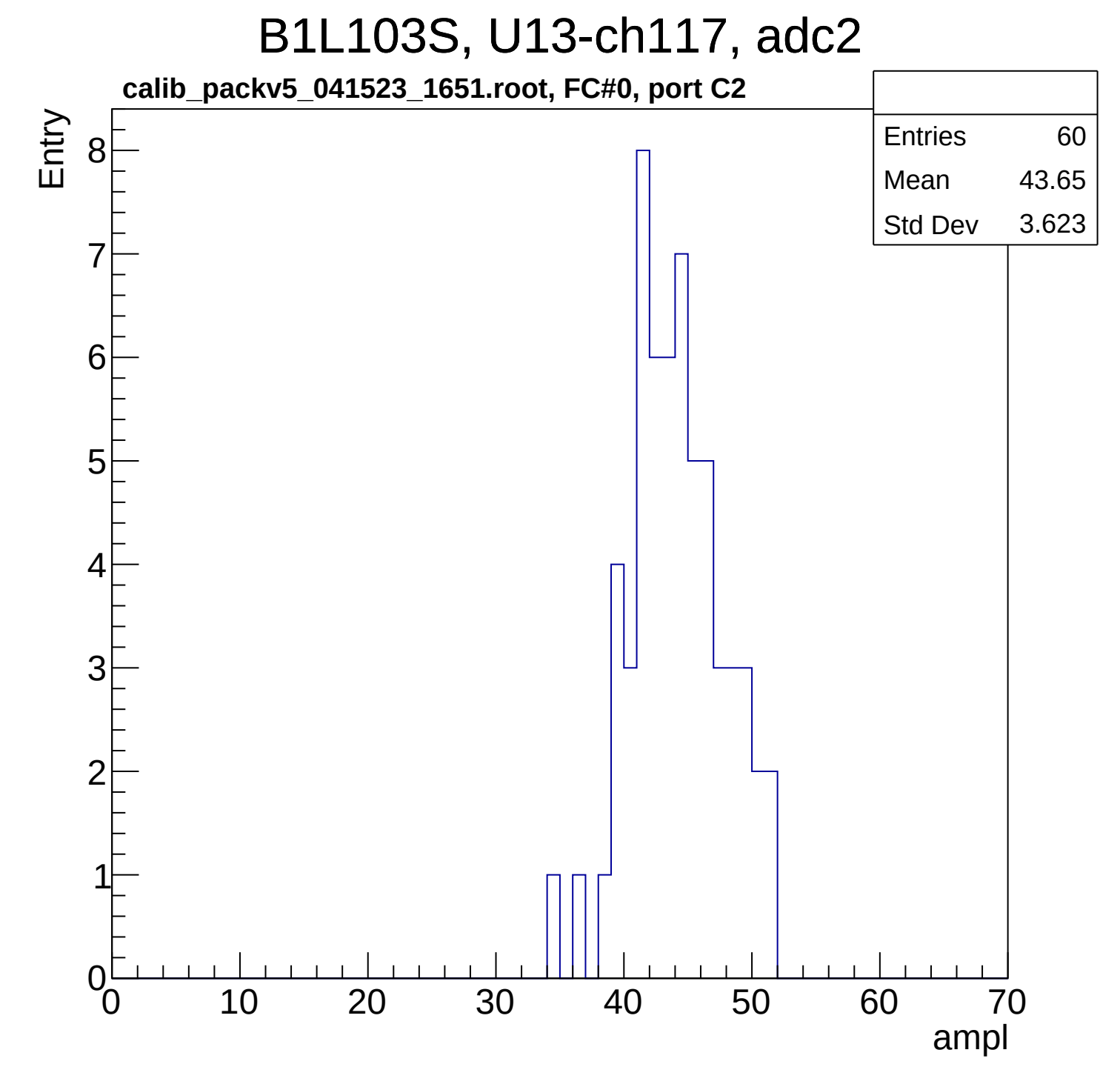
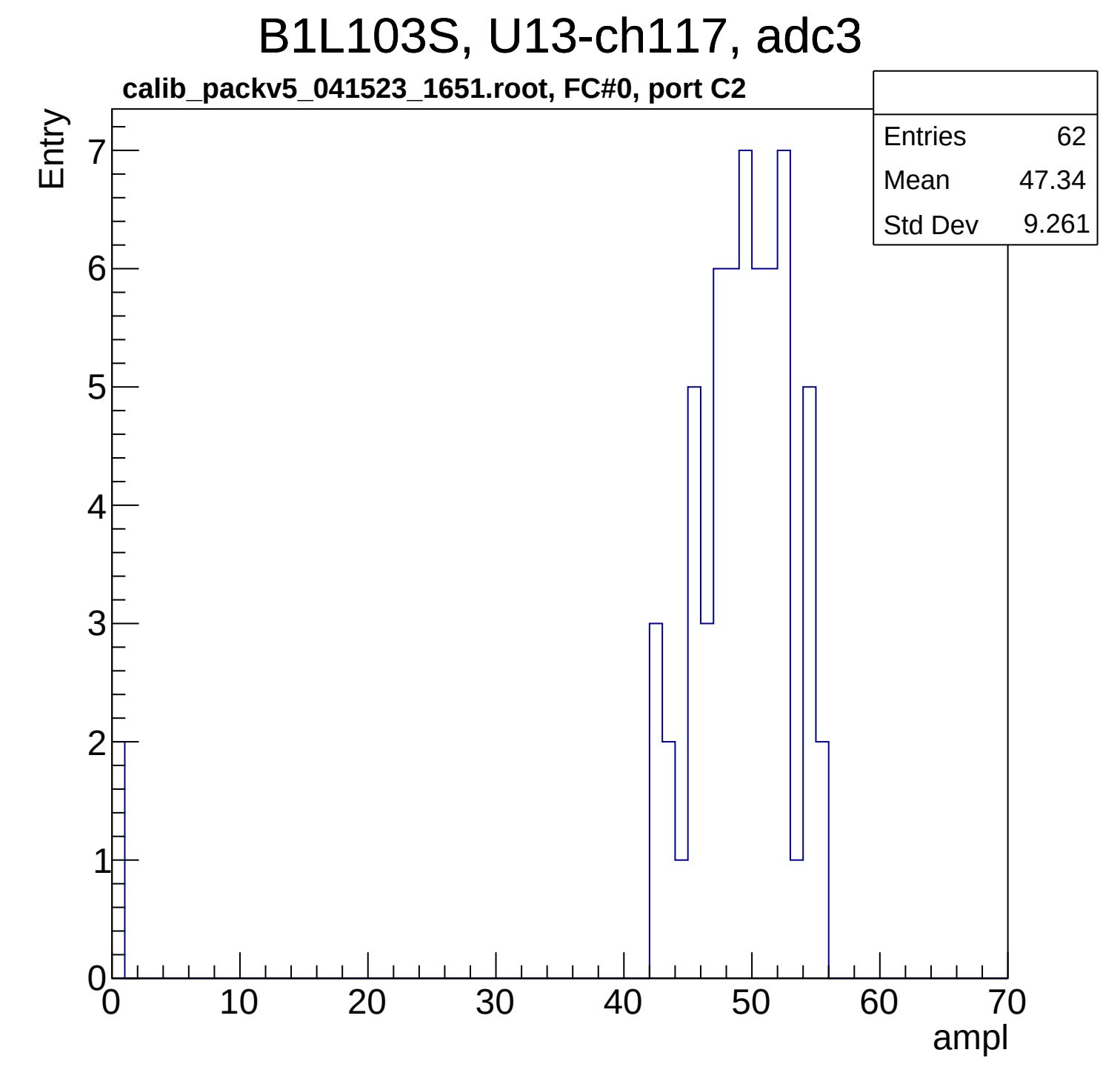
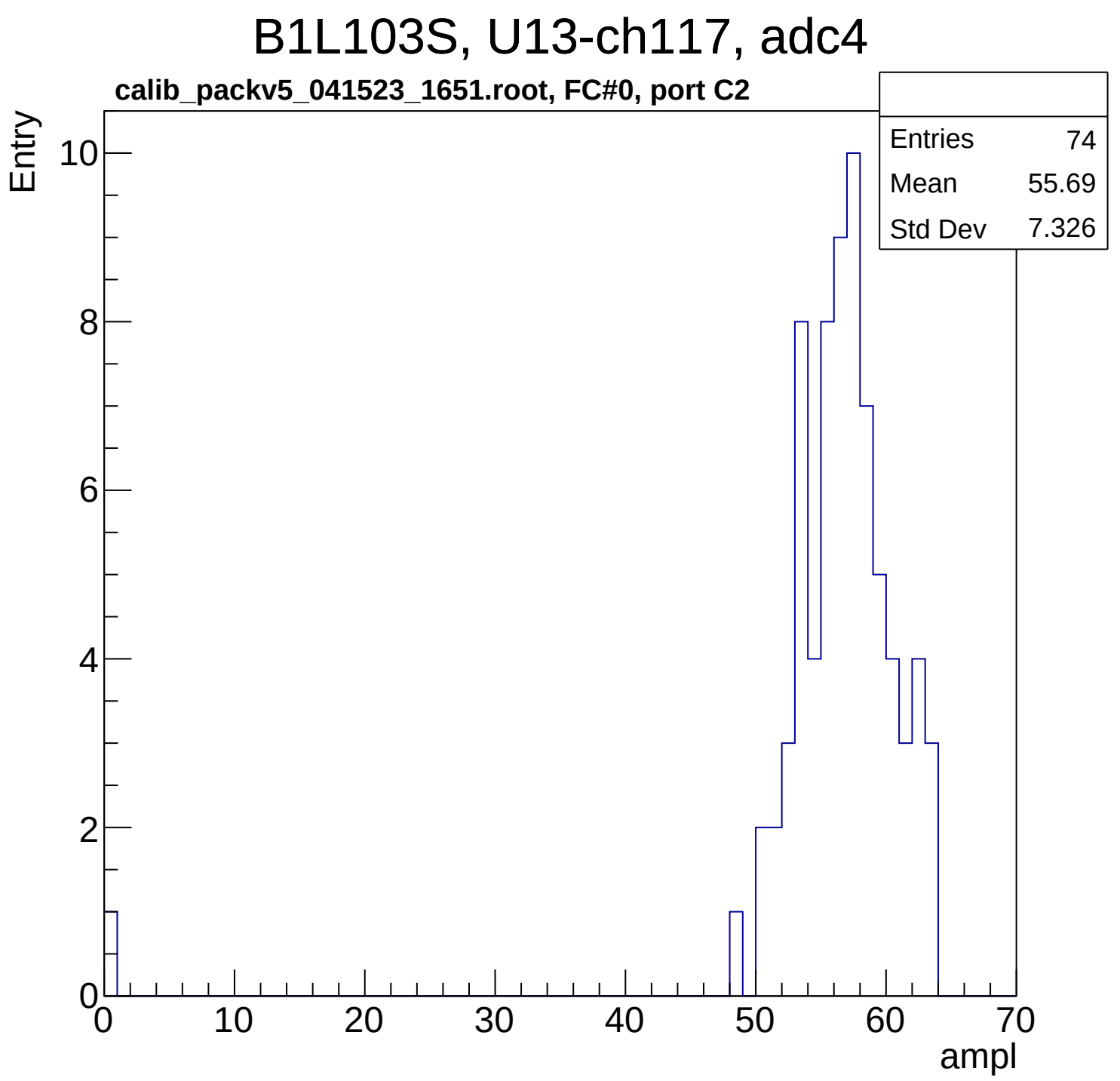
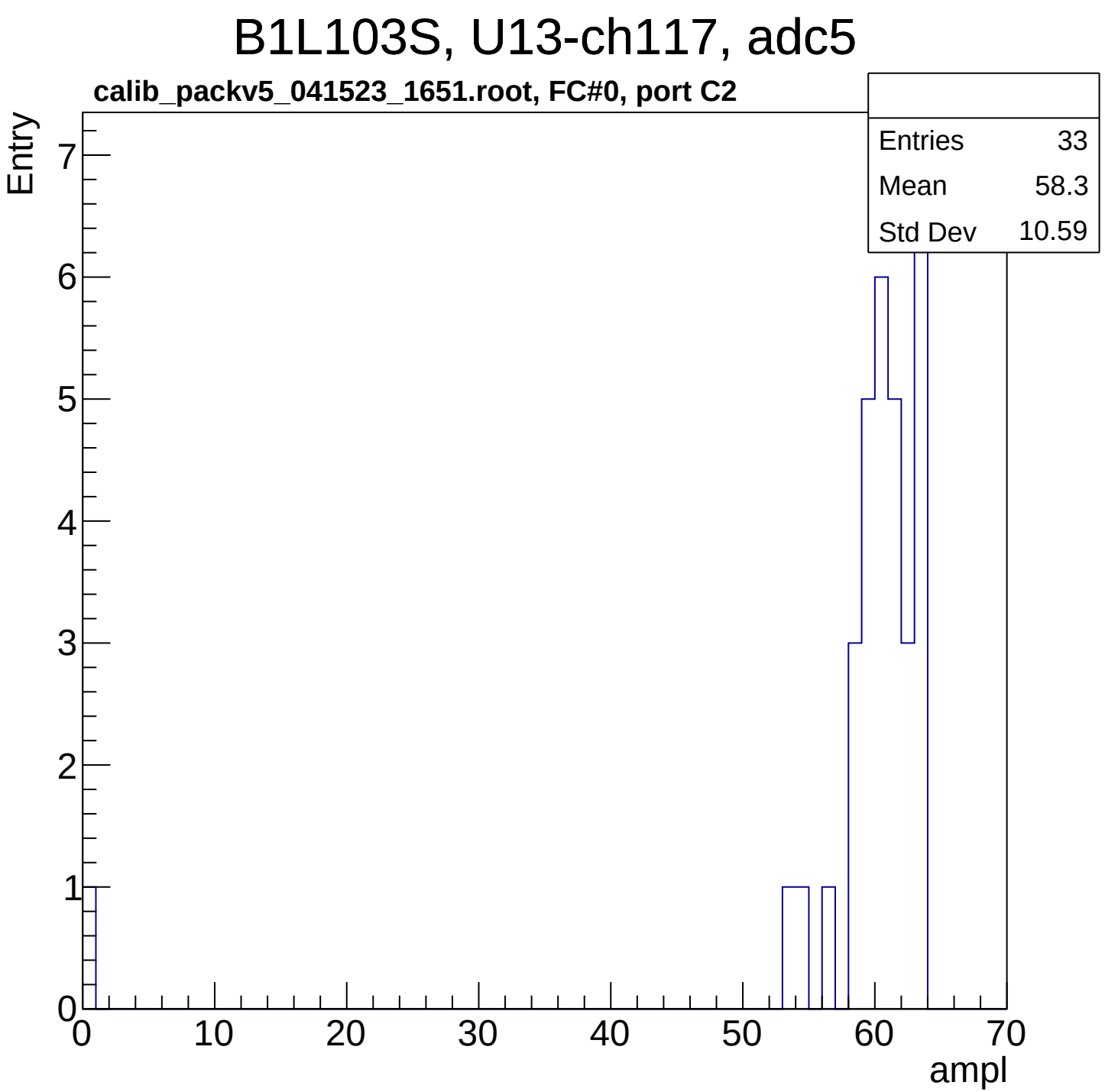

B1L103S, U13-ch117, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 43.65
Std Dev 3.623
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch117, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 47.34
Std Dev 9.261
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch117, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 55.69
Std Dev 7.326
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch117, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 58.3
Std Dev 10.59
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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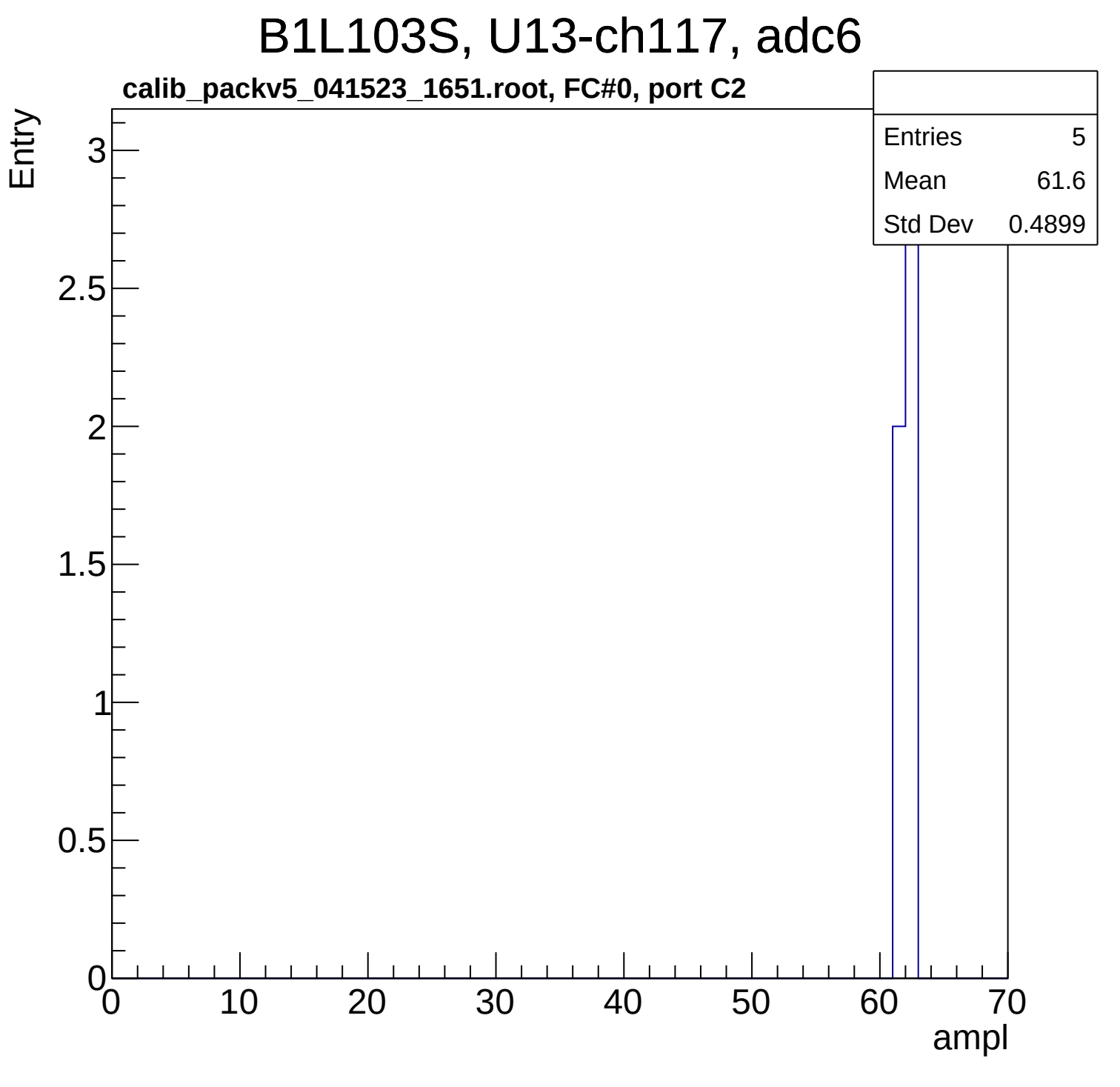
B1L103S, U13-ch117, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.6
Std Dev 0.4899
Entry
ampl
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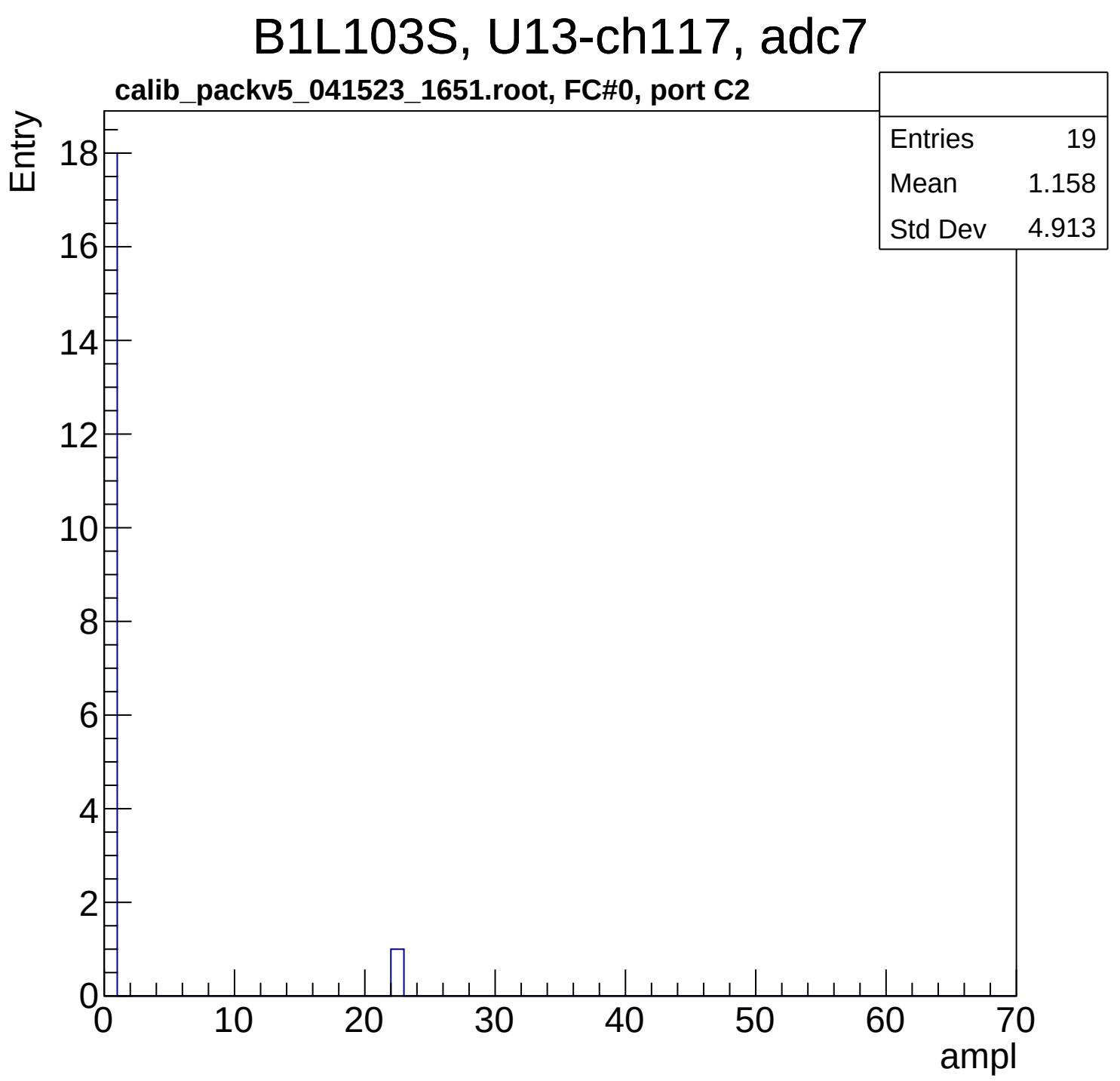
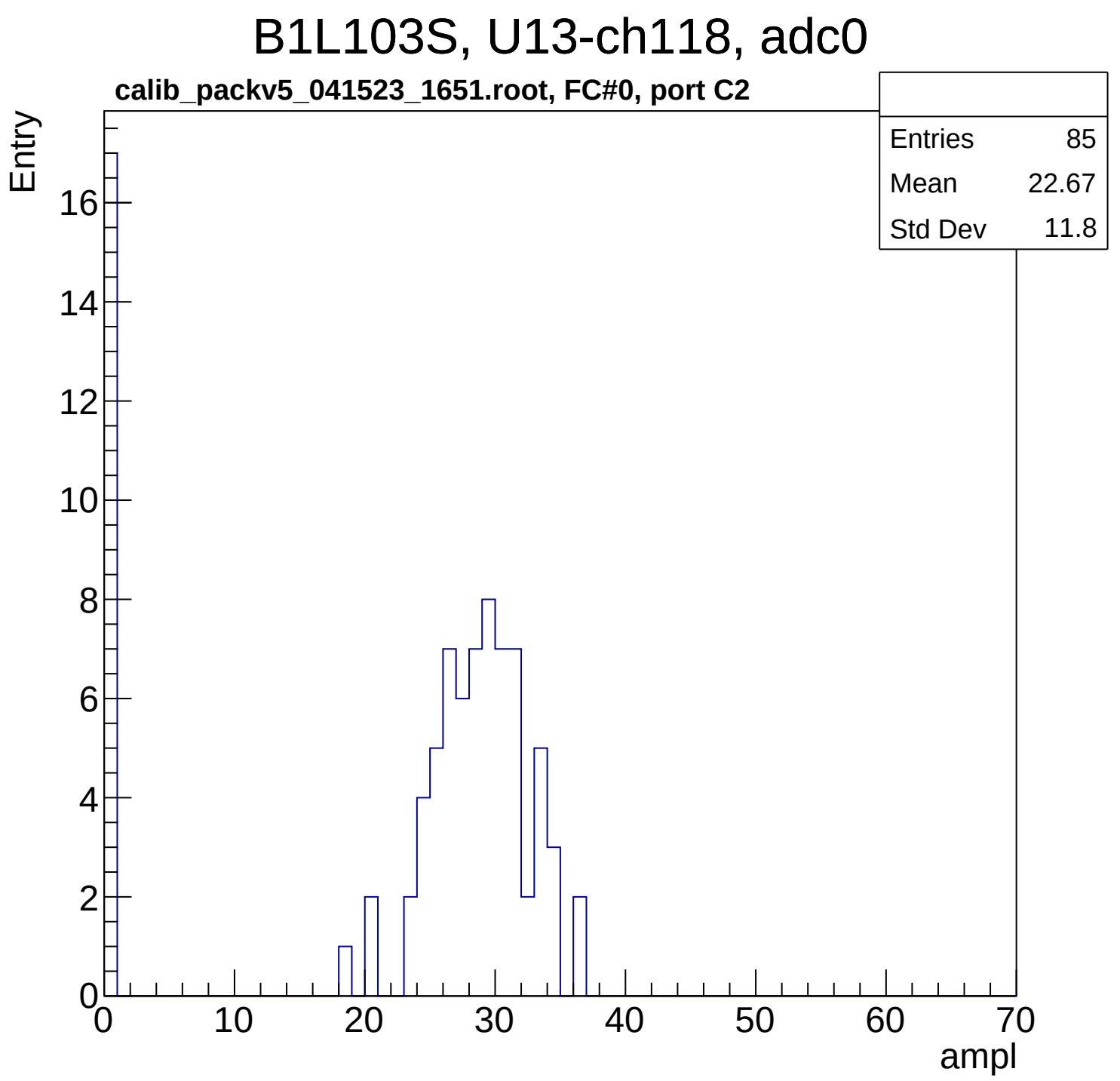
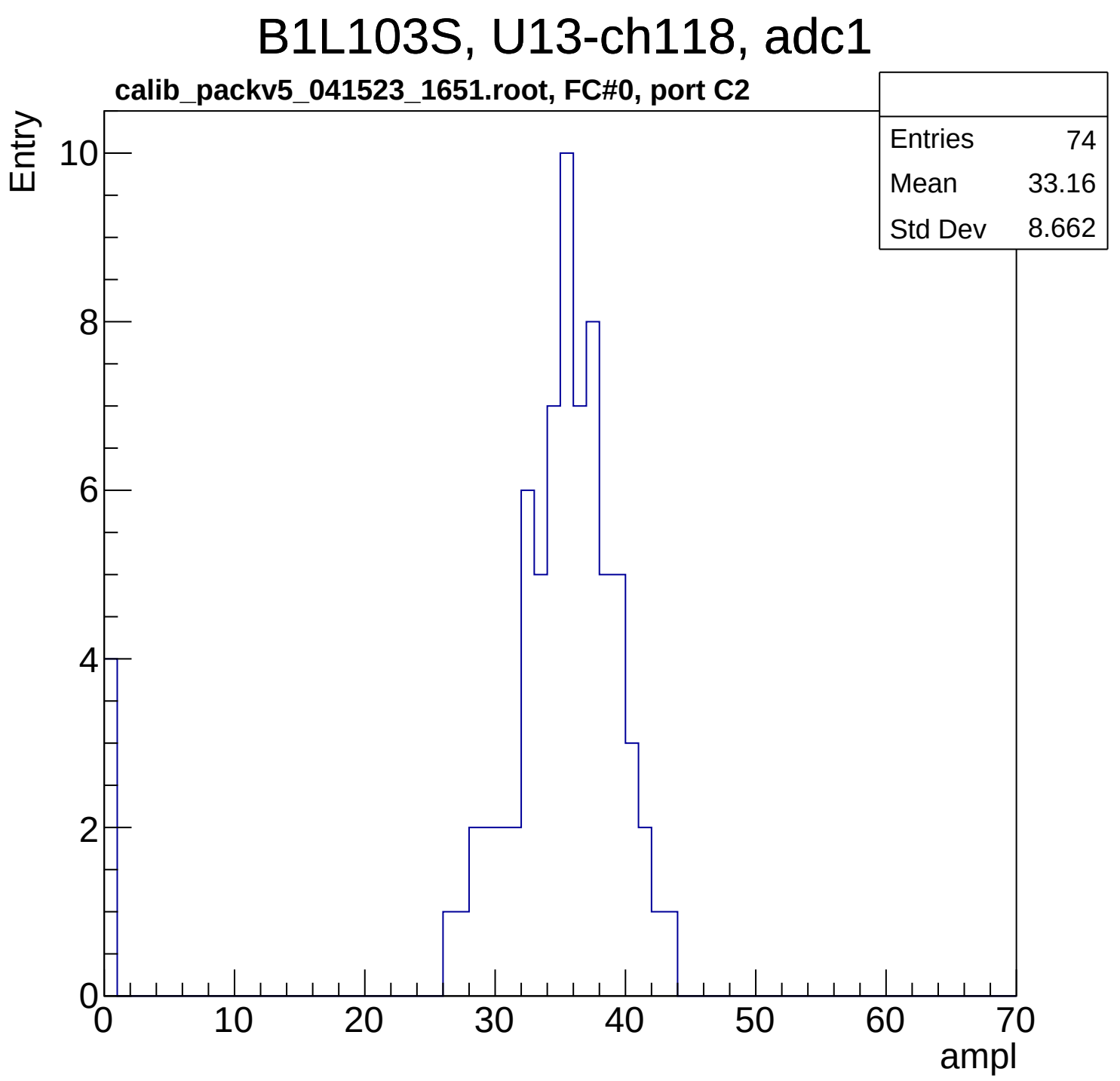
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U13-ch117, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch118, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 22.67
Std Dev 11.8
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch118, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 33.16
Std Dev 8.662
Entry
ampl
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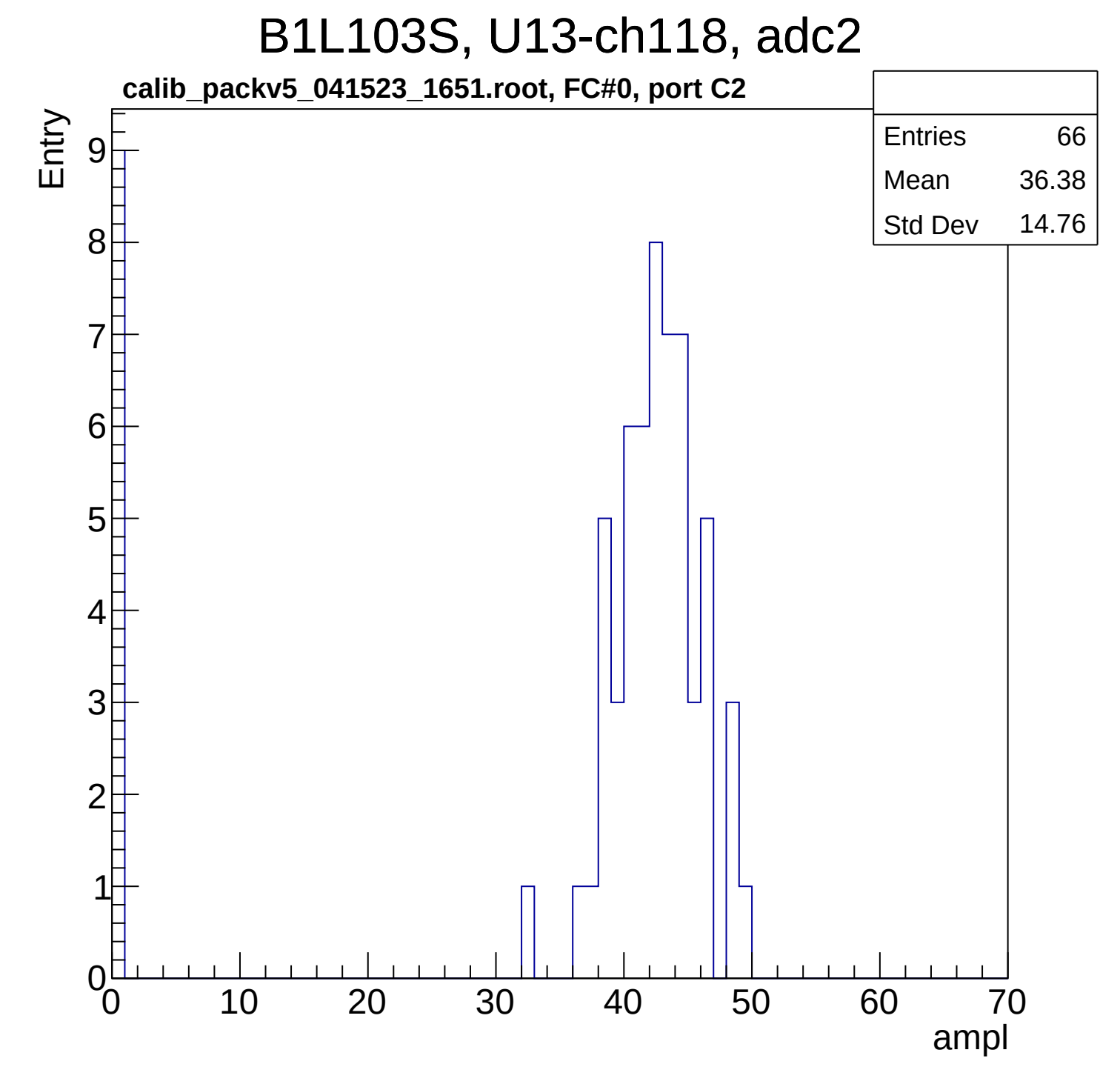
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U13-ch118, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 36.38
Std Dev 14.76
Entry
ampl
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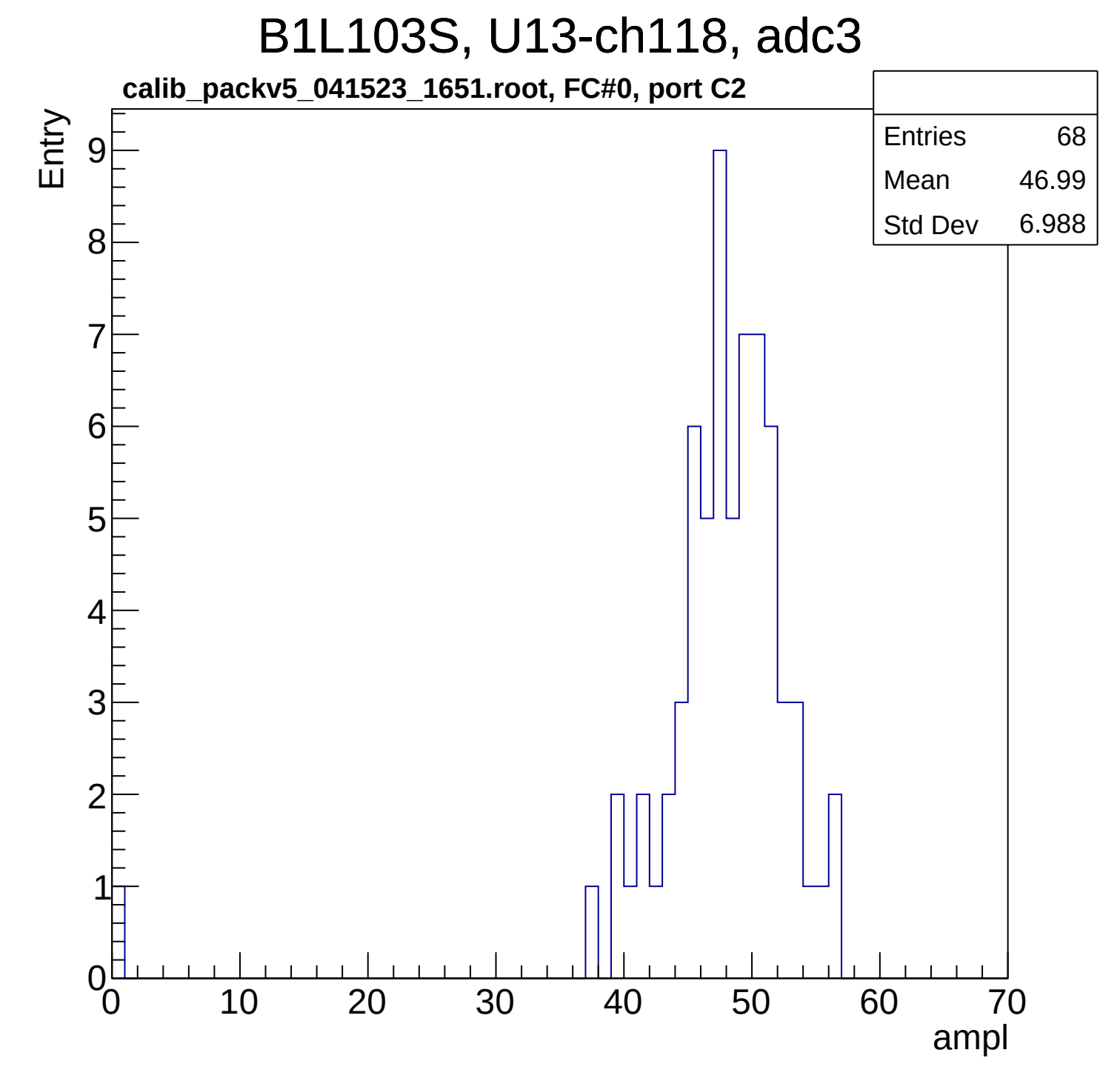
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch118, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 46.99
Std Dev 6.988
Entry
ampl
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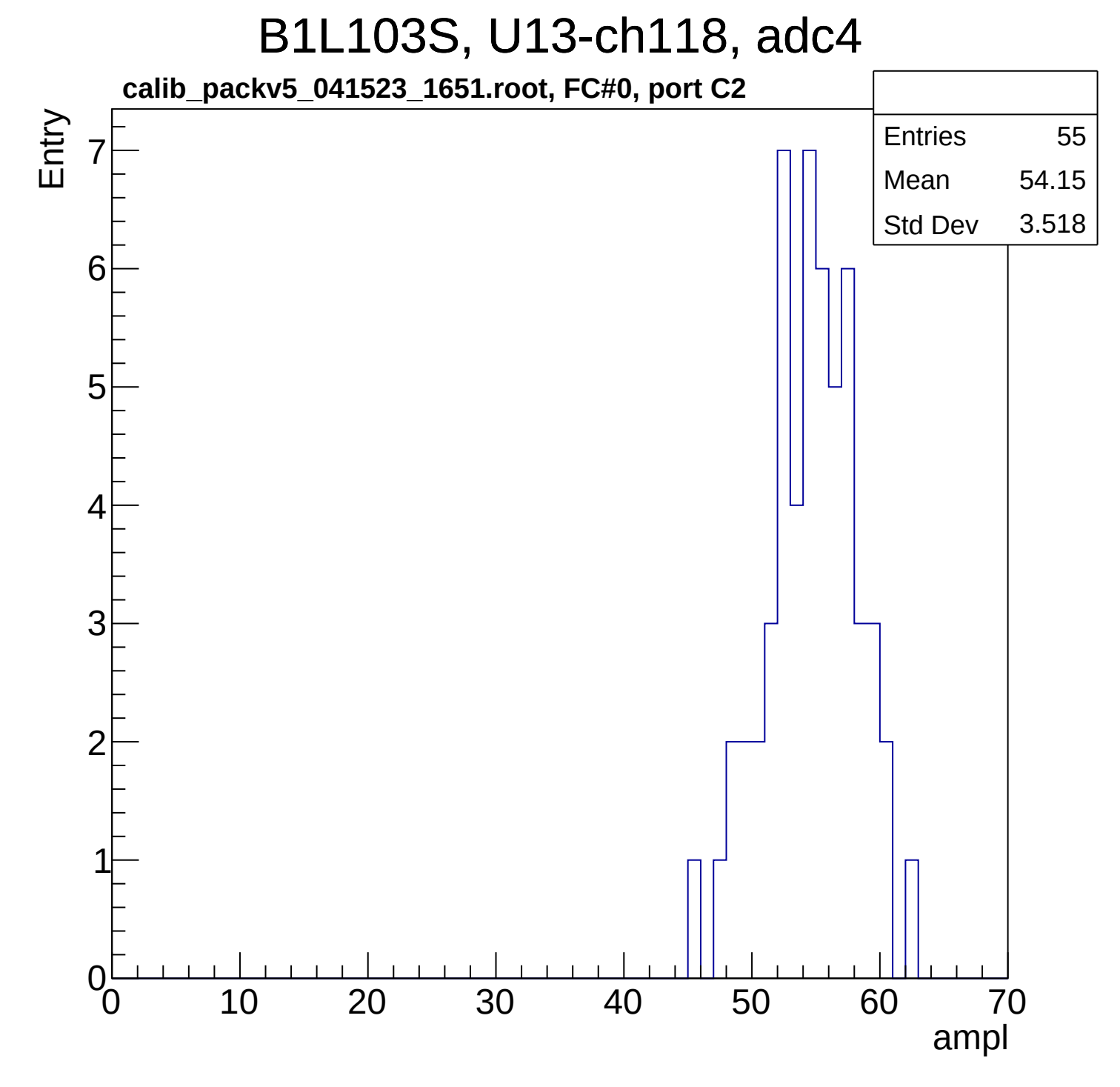
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch118, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 54.15
Std Dev 3.518
Entry
ampl
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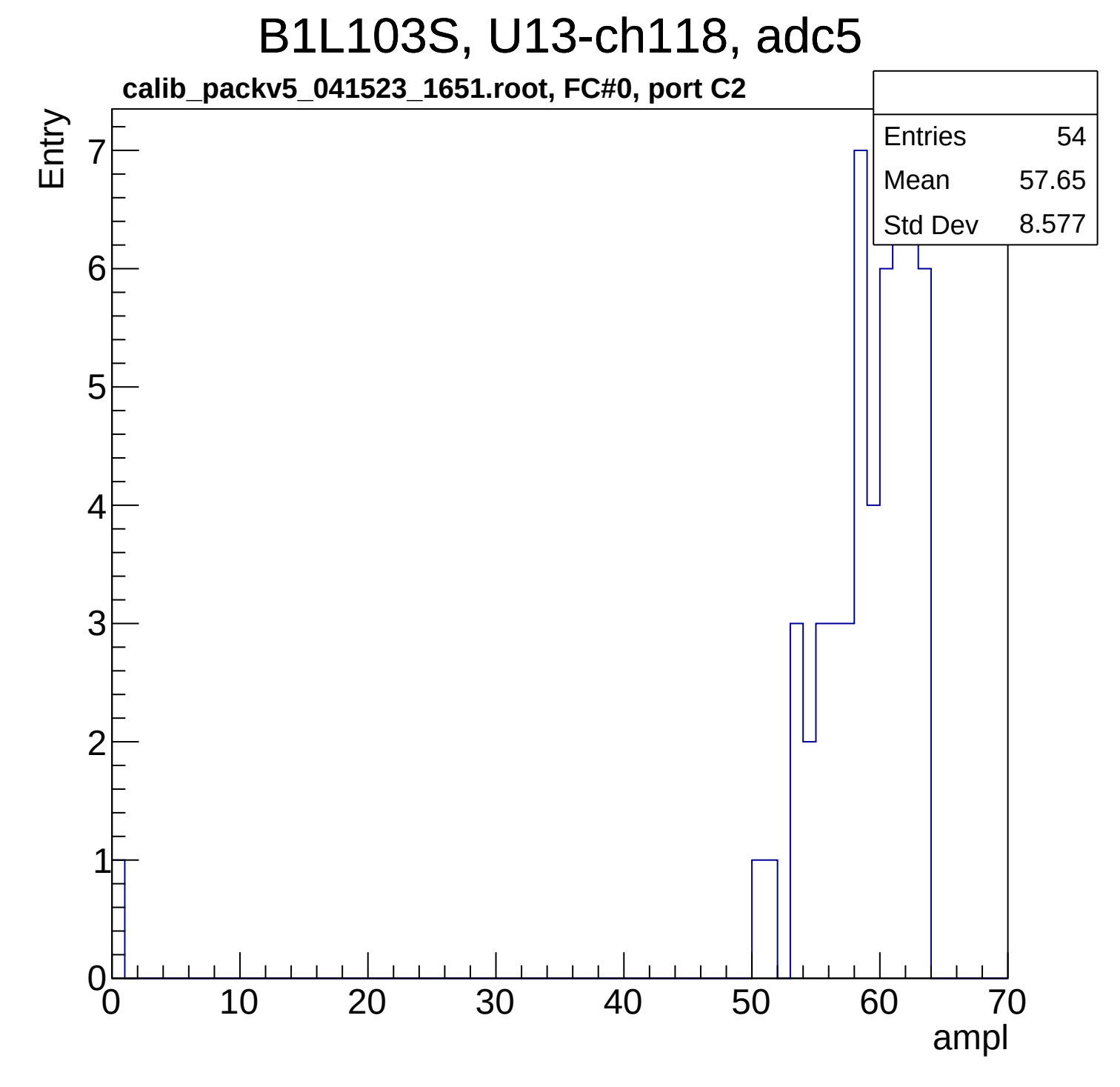
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch118, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.65
Std Dev 8.577
Entry
ampl
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1
2
3
4
5
6
7
0
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40
50
60
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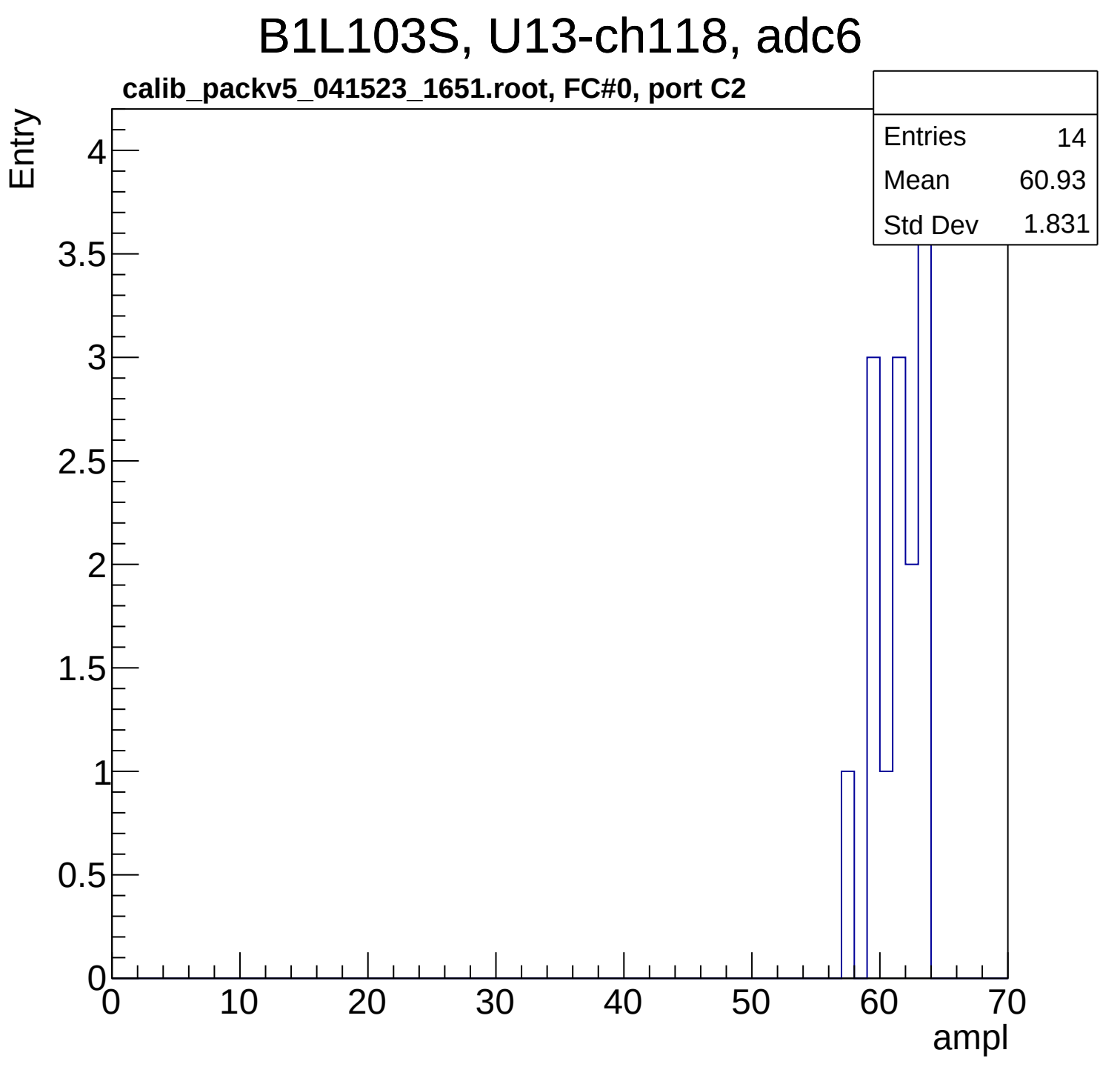
B1L103S, U13-ch118, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 60.93
Std Dev 1.831
Entry
ampl
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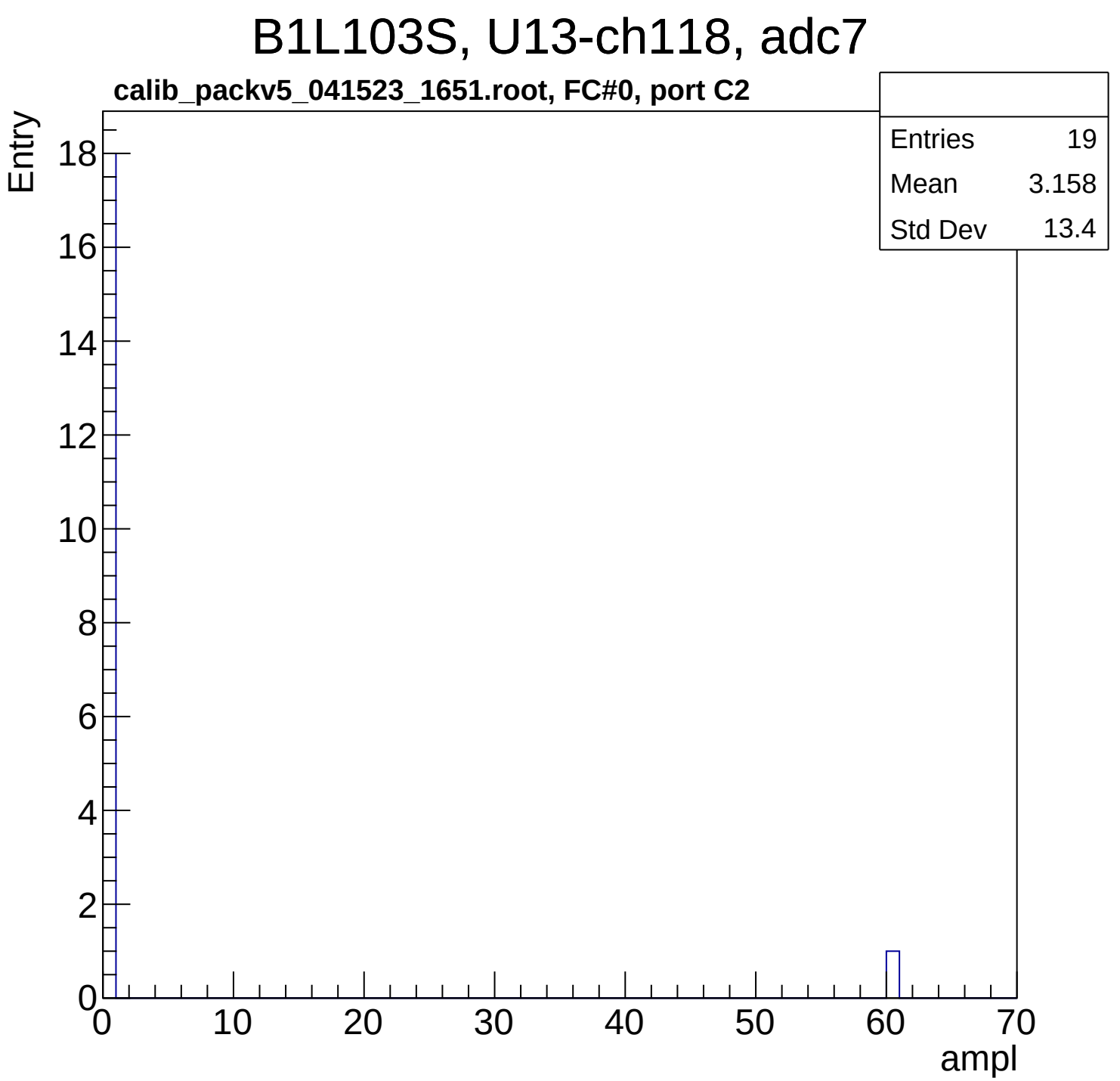
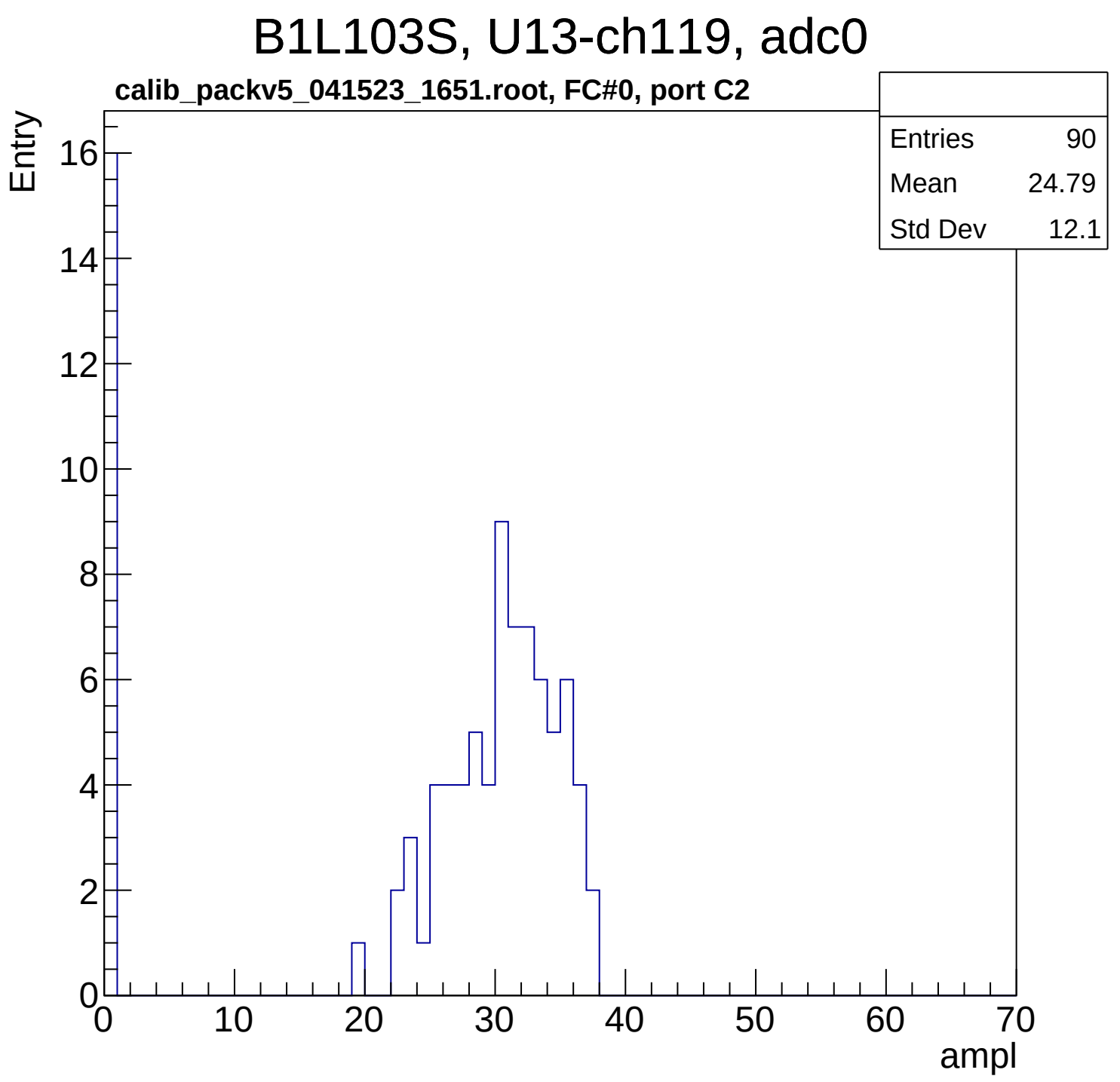
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U13-ch118, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.158
Std Dev 13.4
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch119, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 24.79
Std Dev 12.1
Entry
ampl
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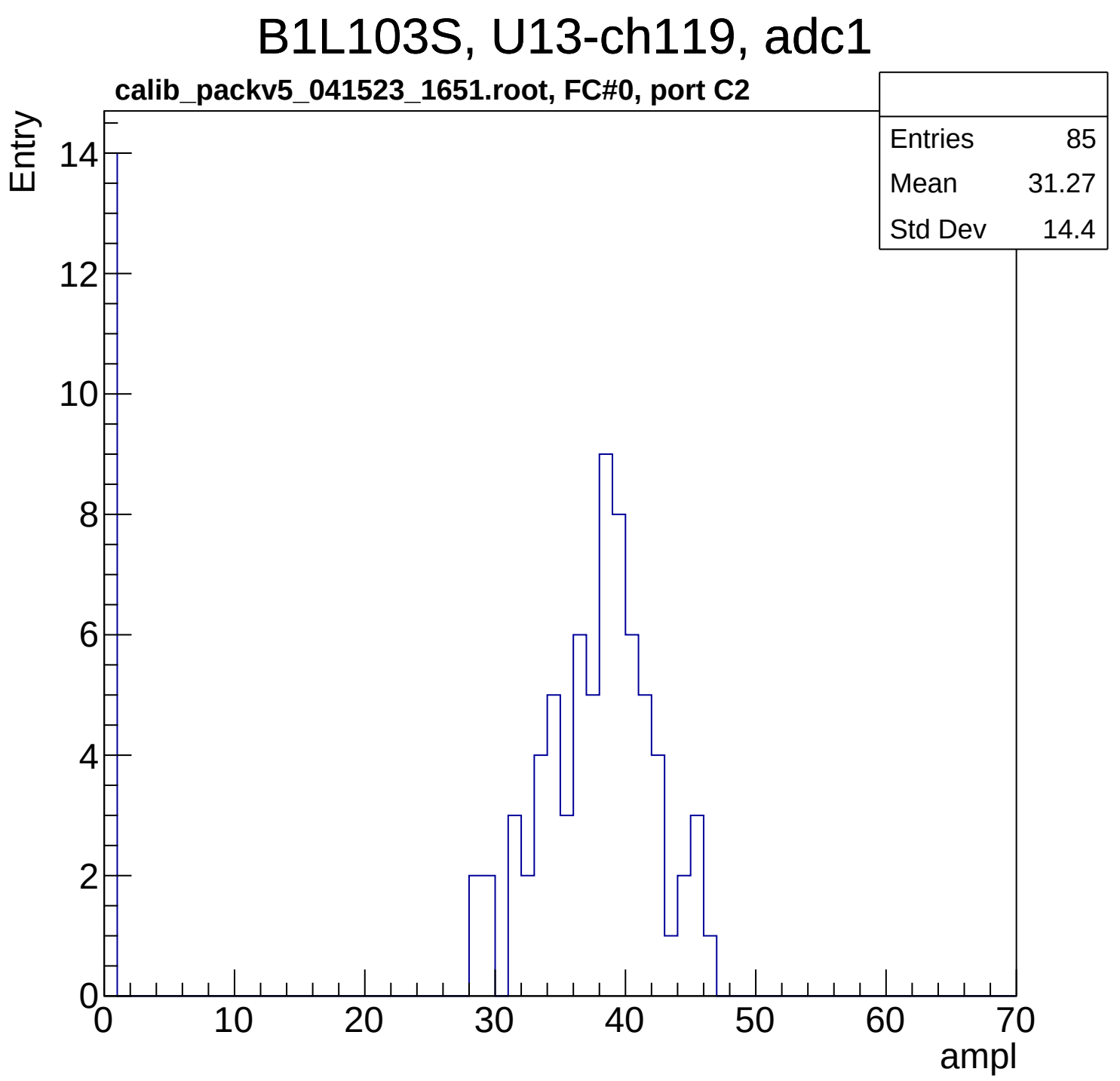
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U13-ch119, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 31.27
Std Dev 14.4
Entry
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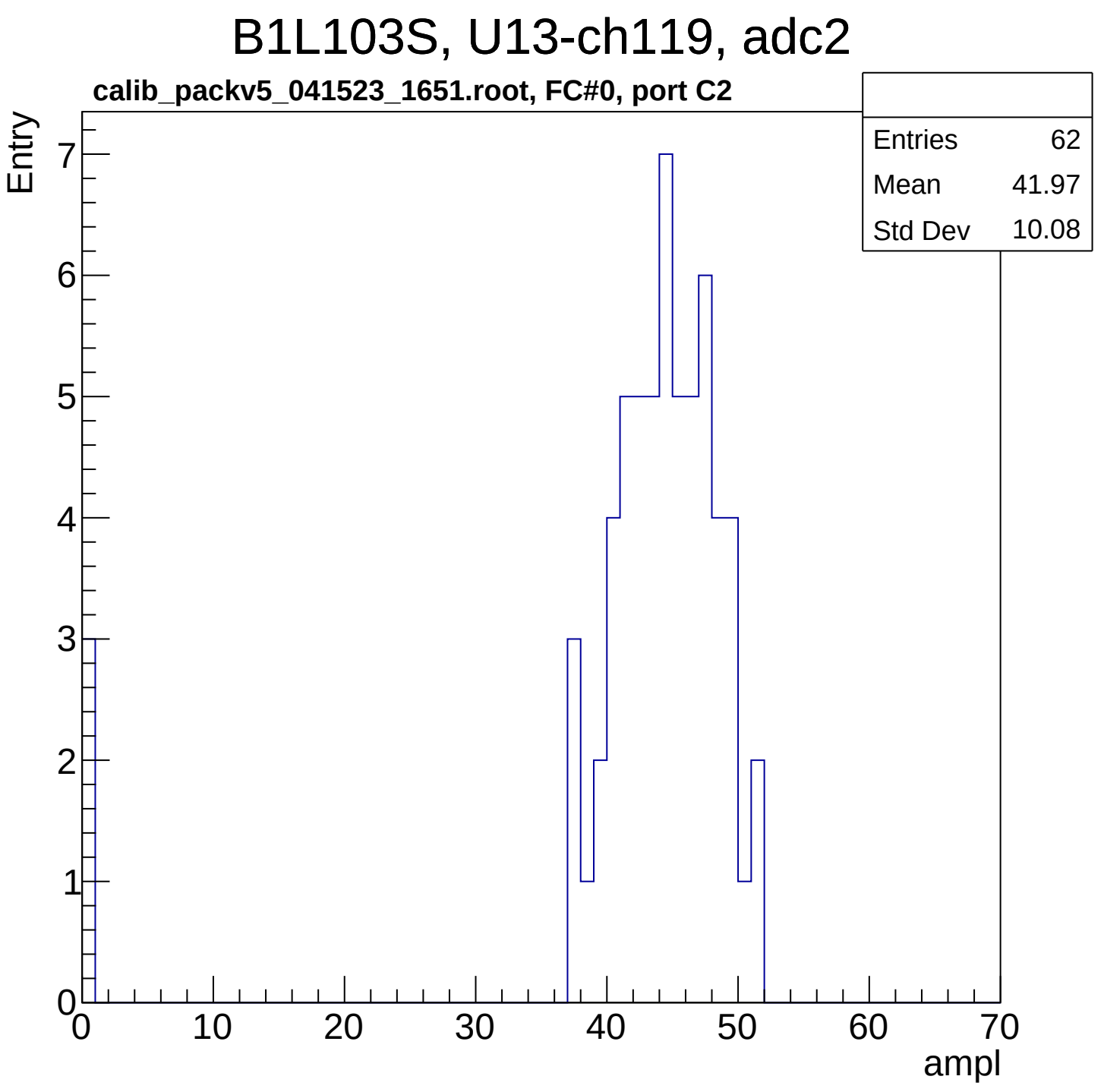
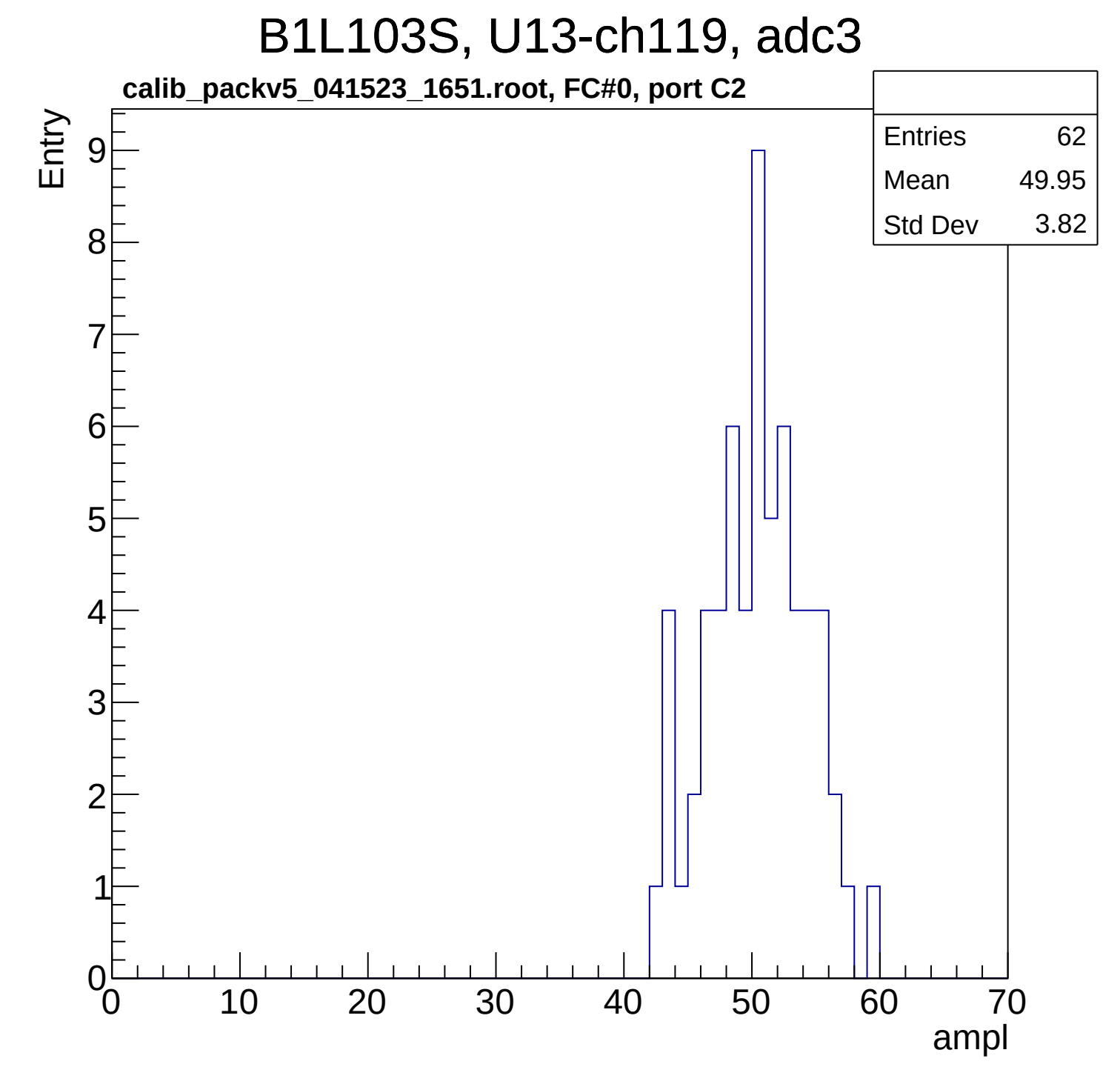
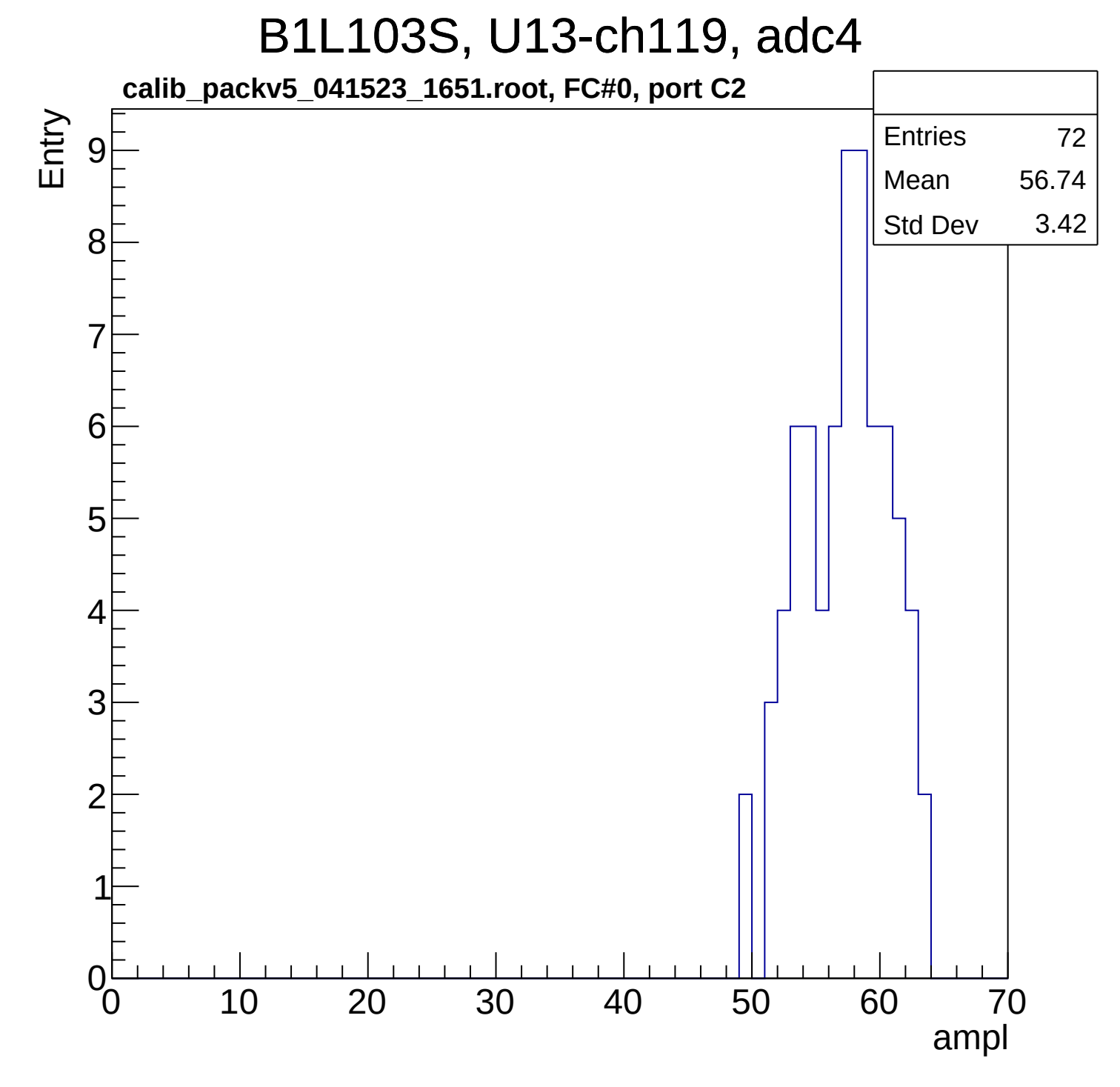
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch119, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 41.97
Std Dev 10.08
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch119, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 49.95
Std Dev 3.82
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch119, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 56.74
Std Dev 3.42
Entry
ampl
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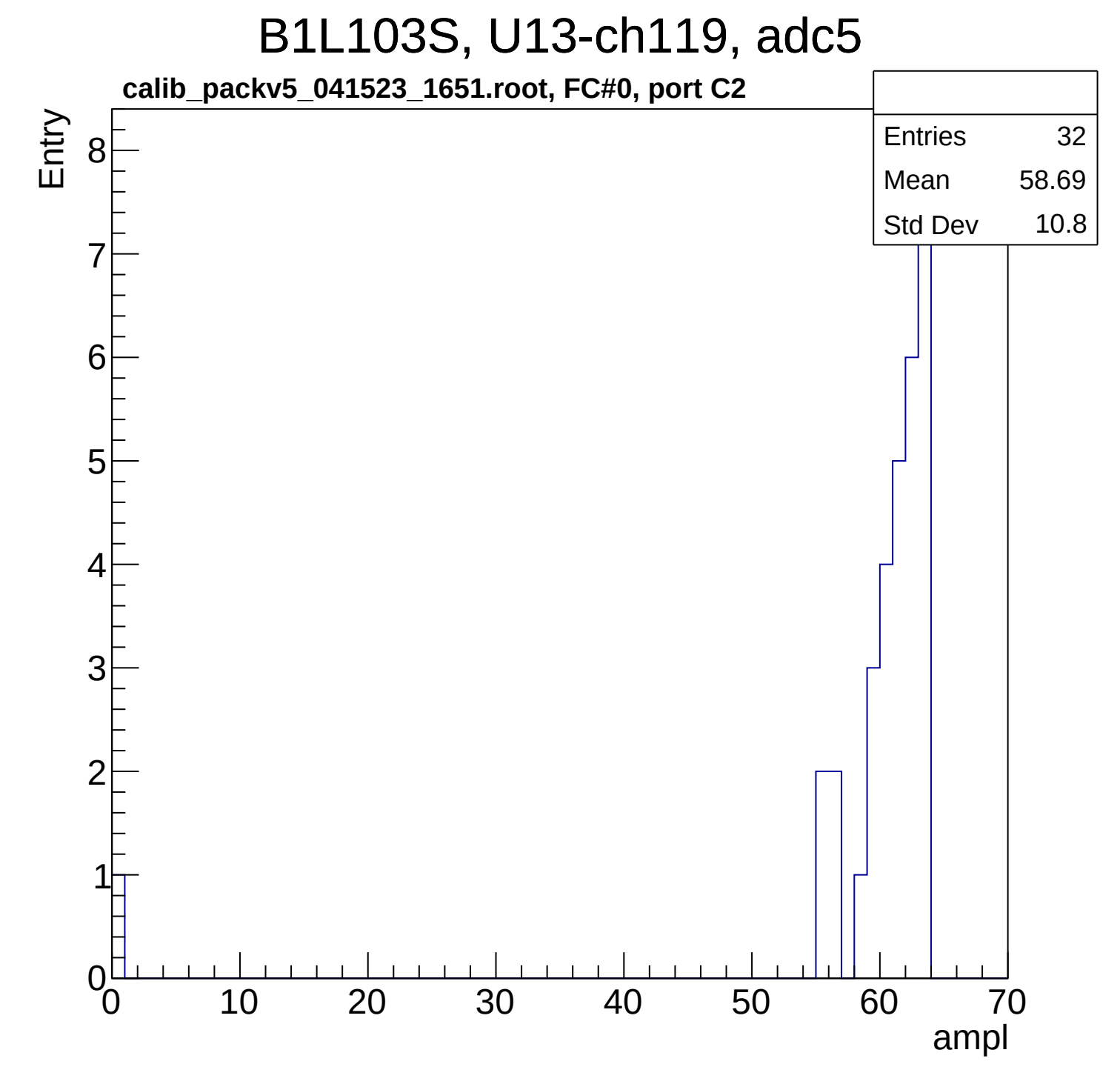
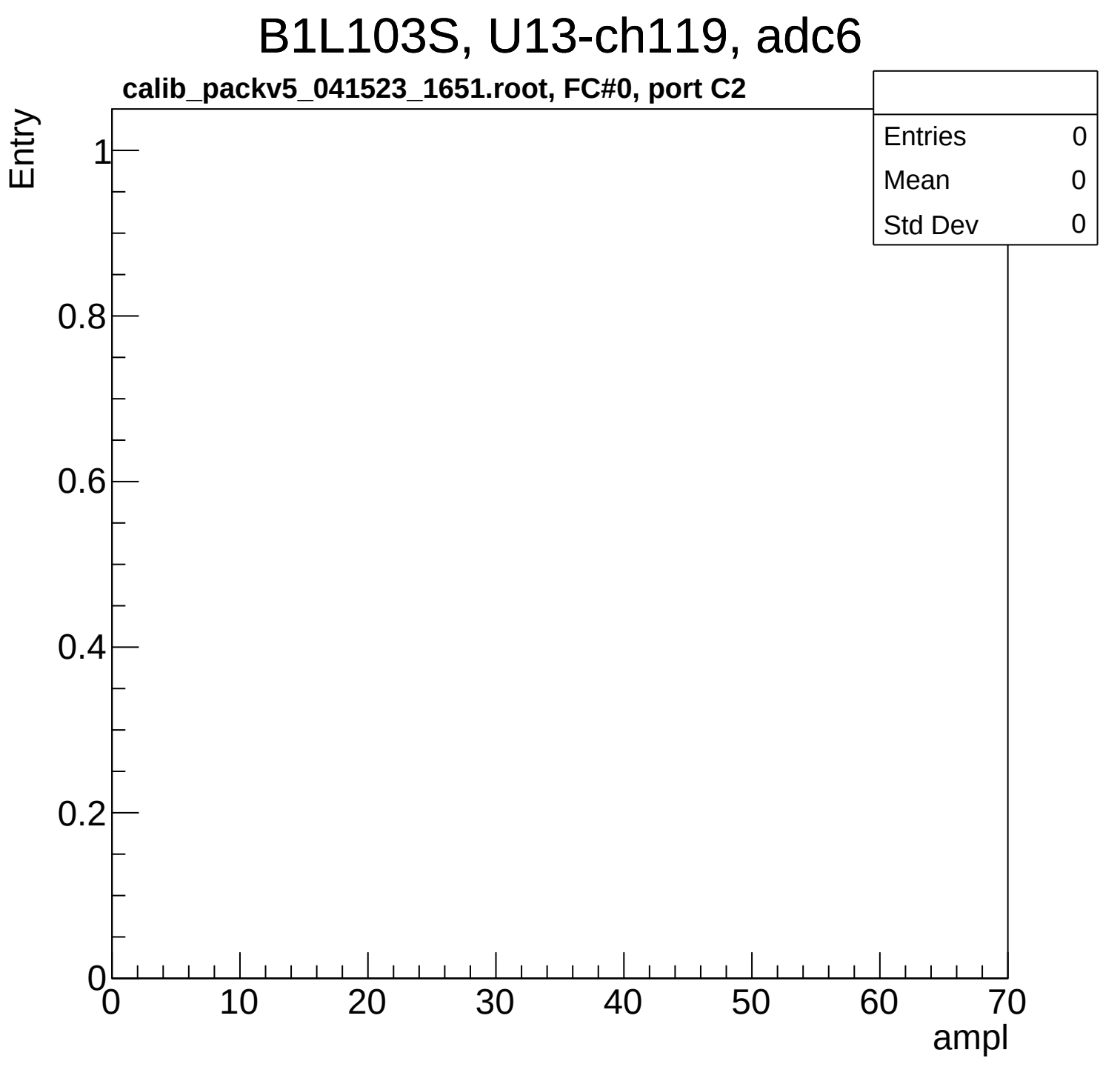
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch119, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 58.69
Std Dev 10.8
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch119, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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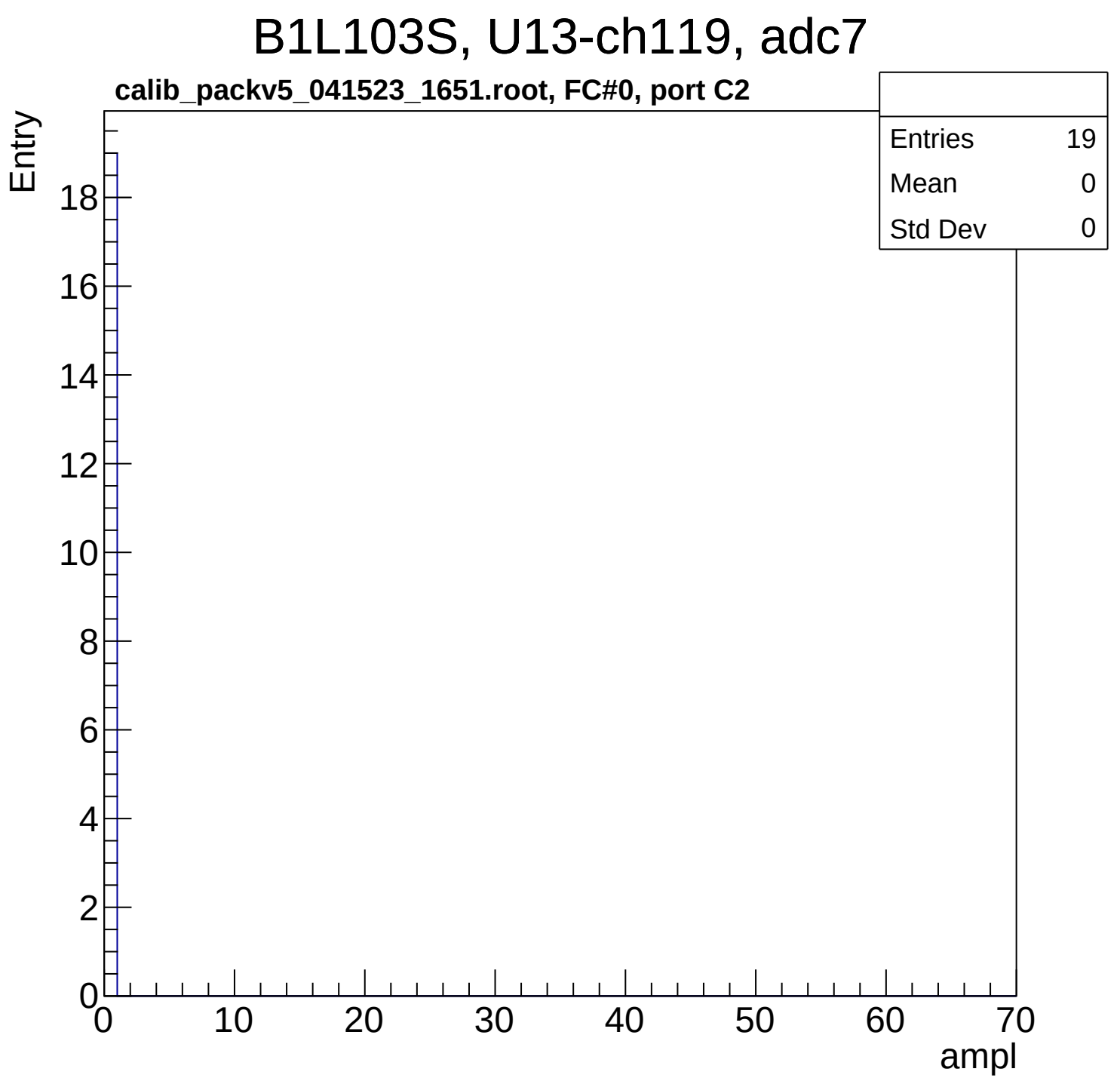
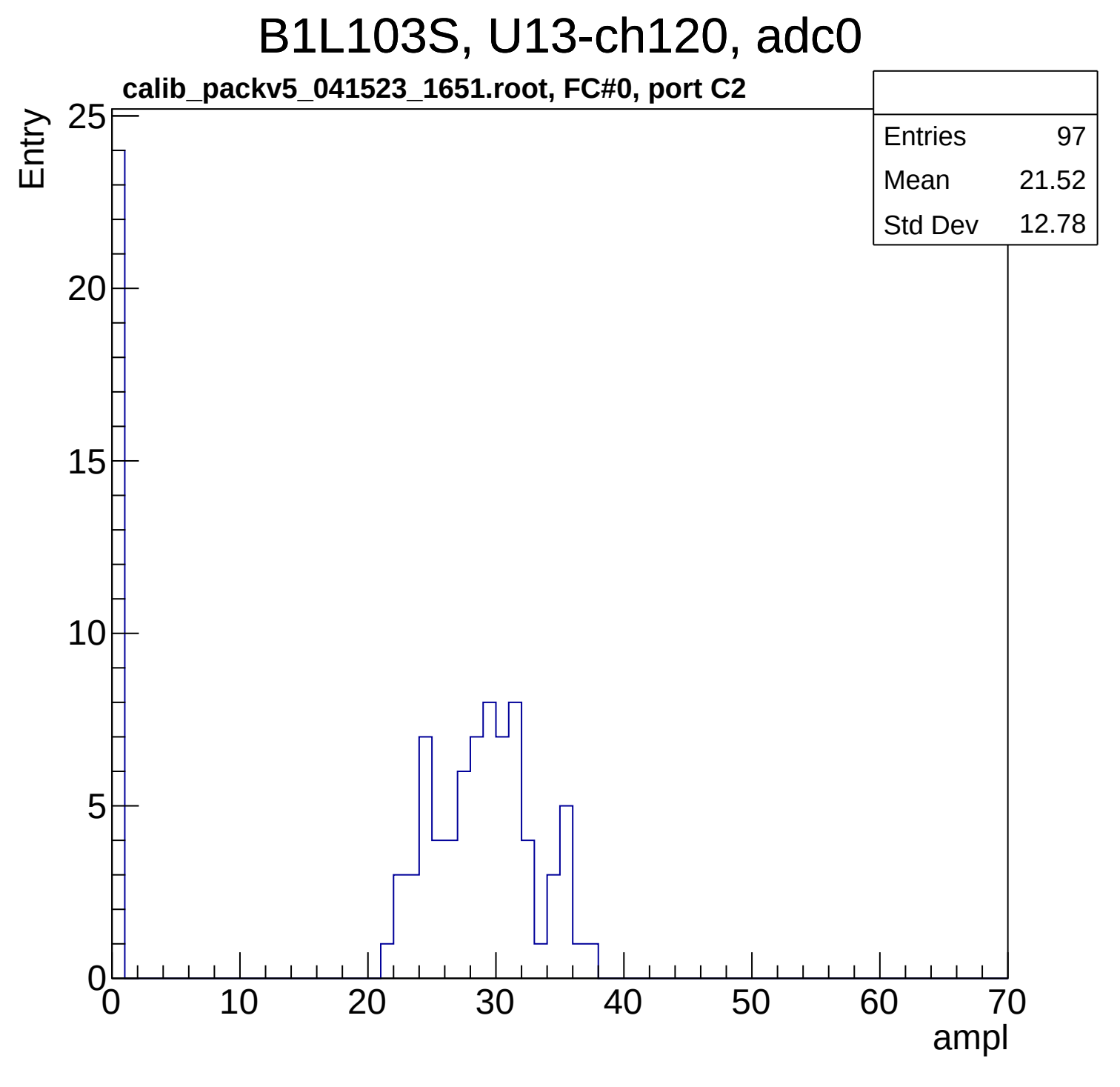
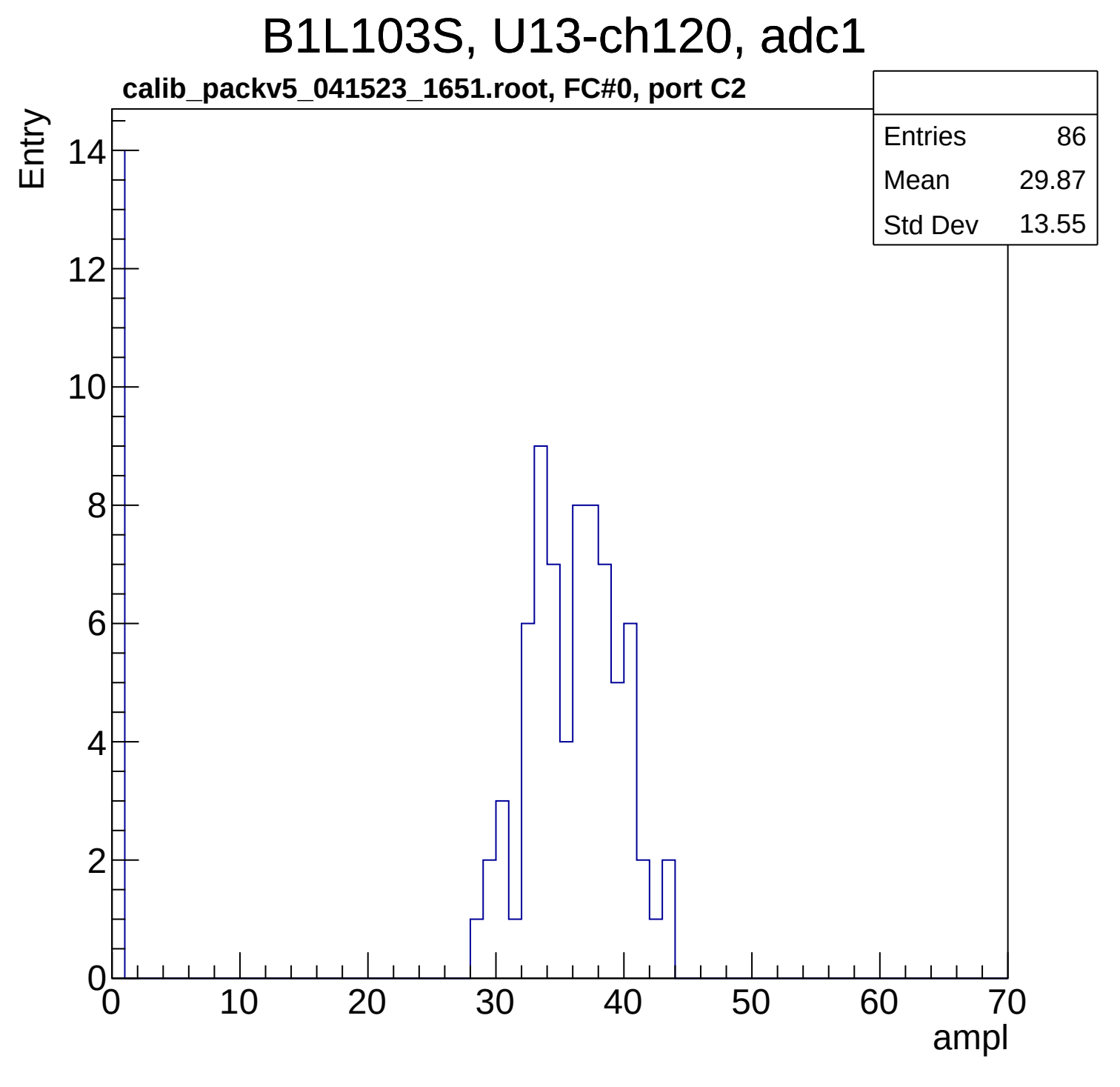
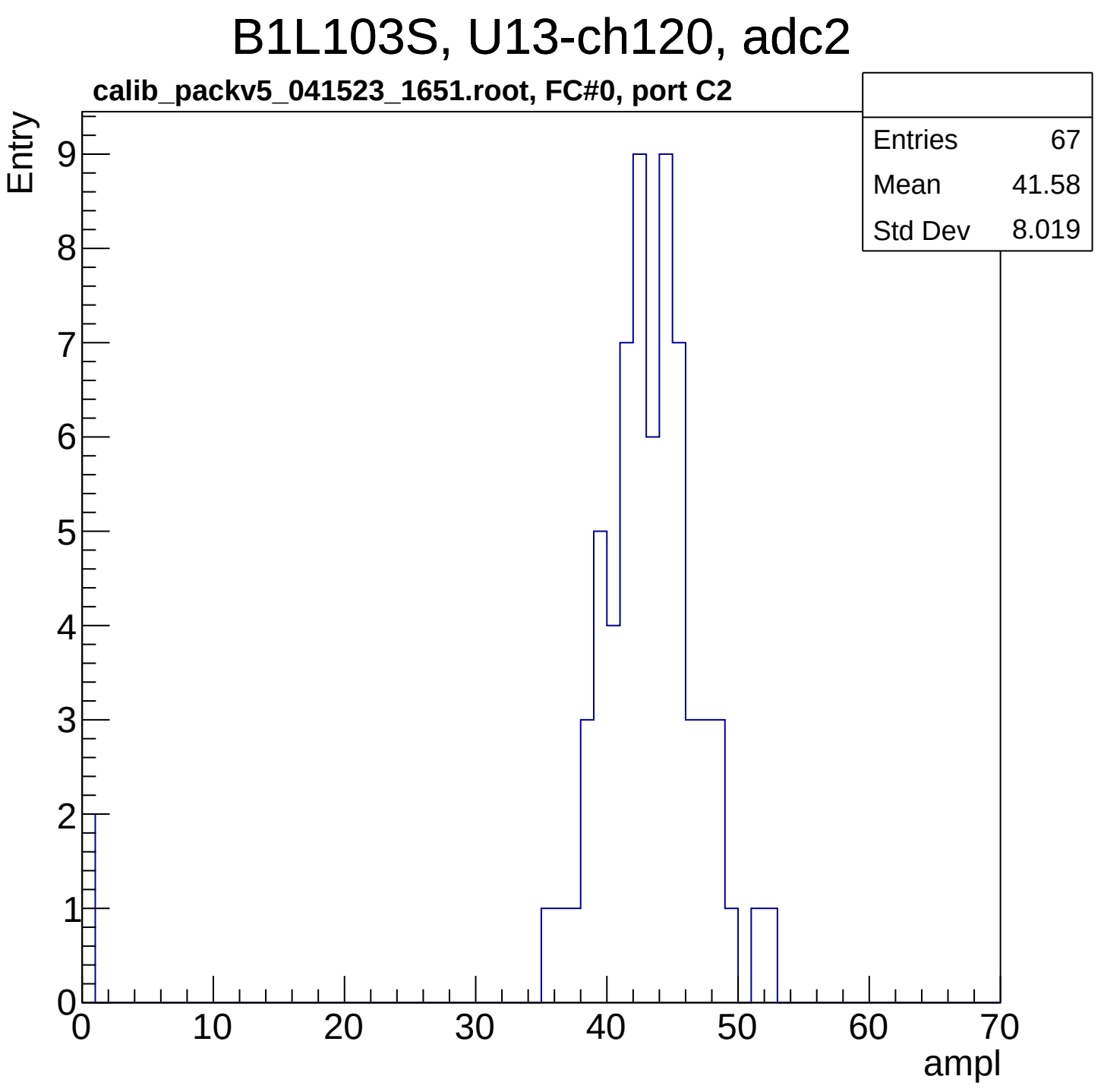
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch119, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch120, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 21.52
Std Dev 12.78
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U13-ch120, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 29.87
Std Dev 13.55
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U13-ch120, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 41.58
Std Dev 8.019
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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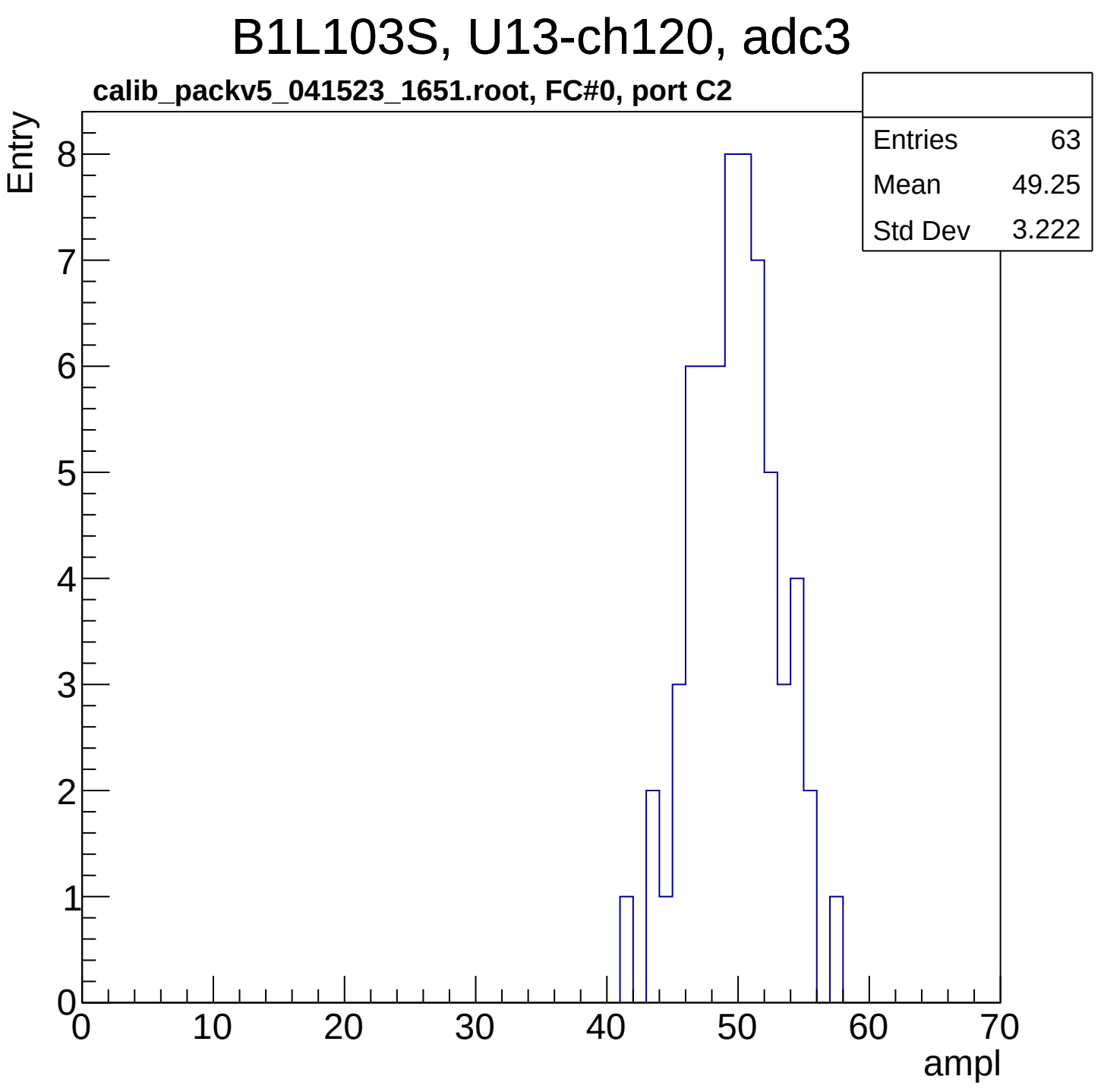
B1L103S, U13-ch120, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 49.25
Std Dev 3.222
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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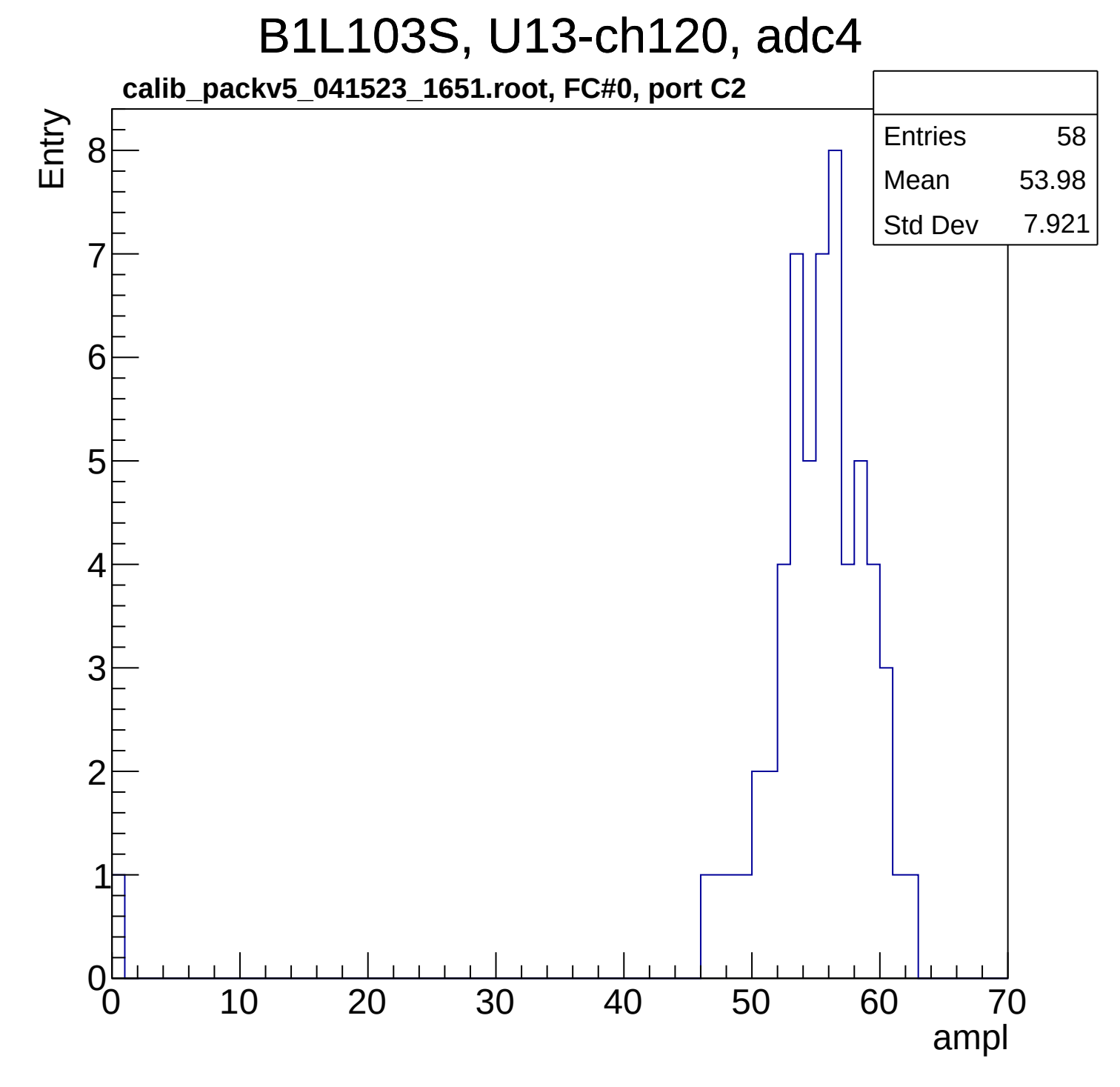
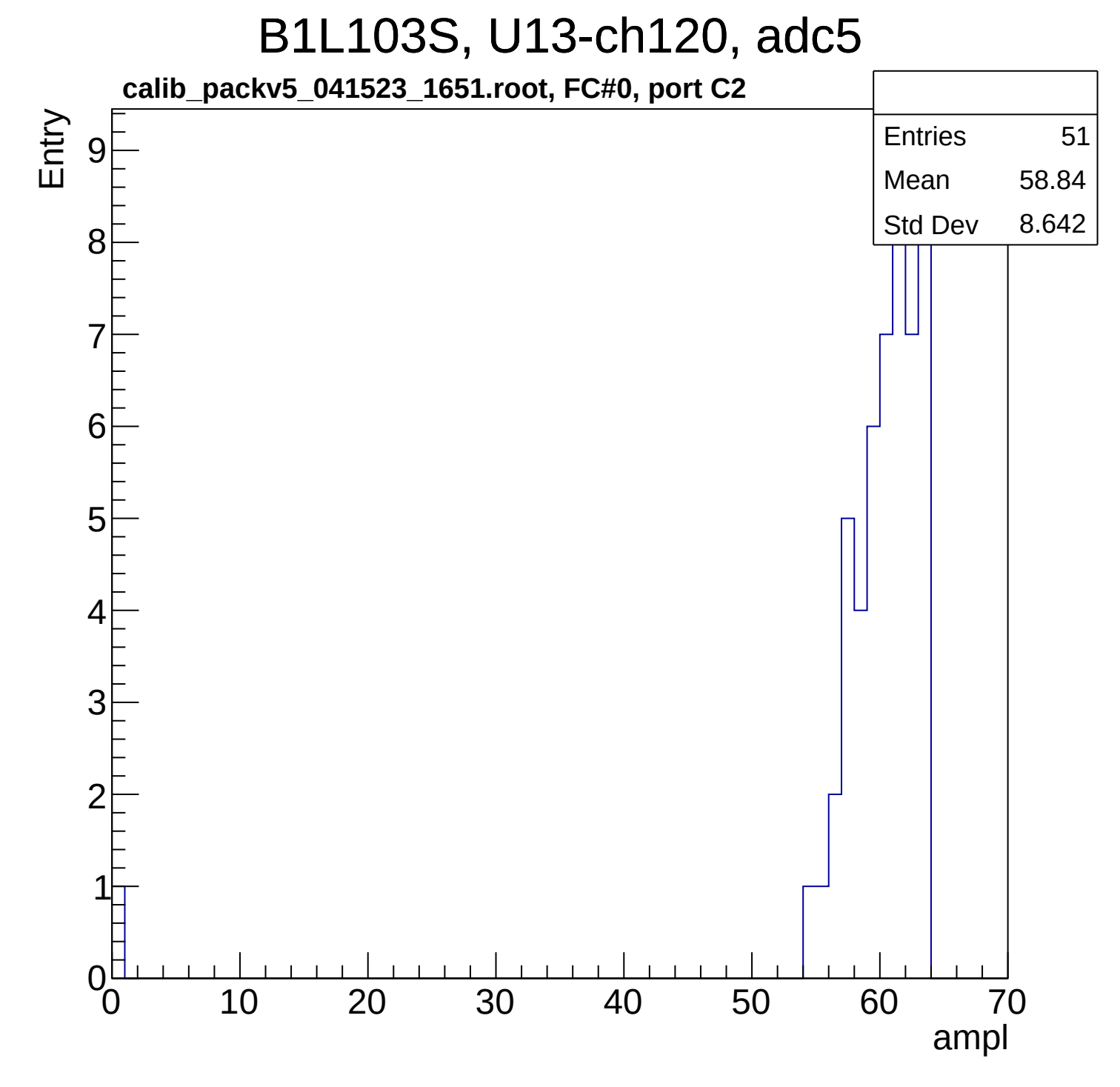

B1L103S, U13-ch120, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 53.98
Std Dev 7.921
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch120, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.84
Std Dev 8.642
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
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40
50
60
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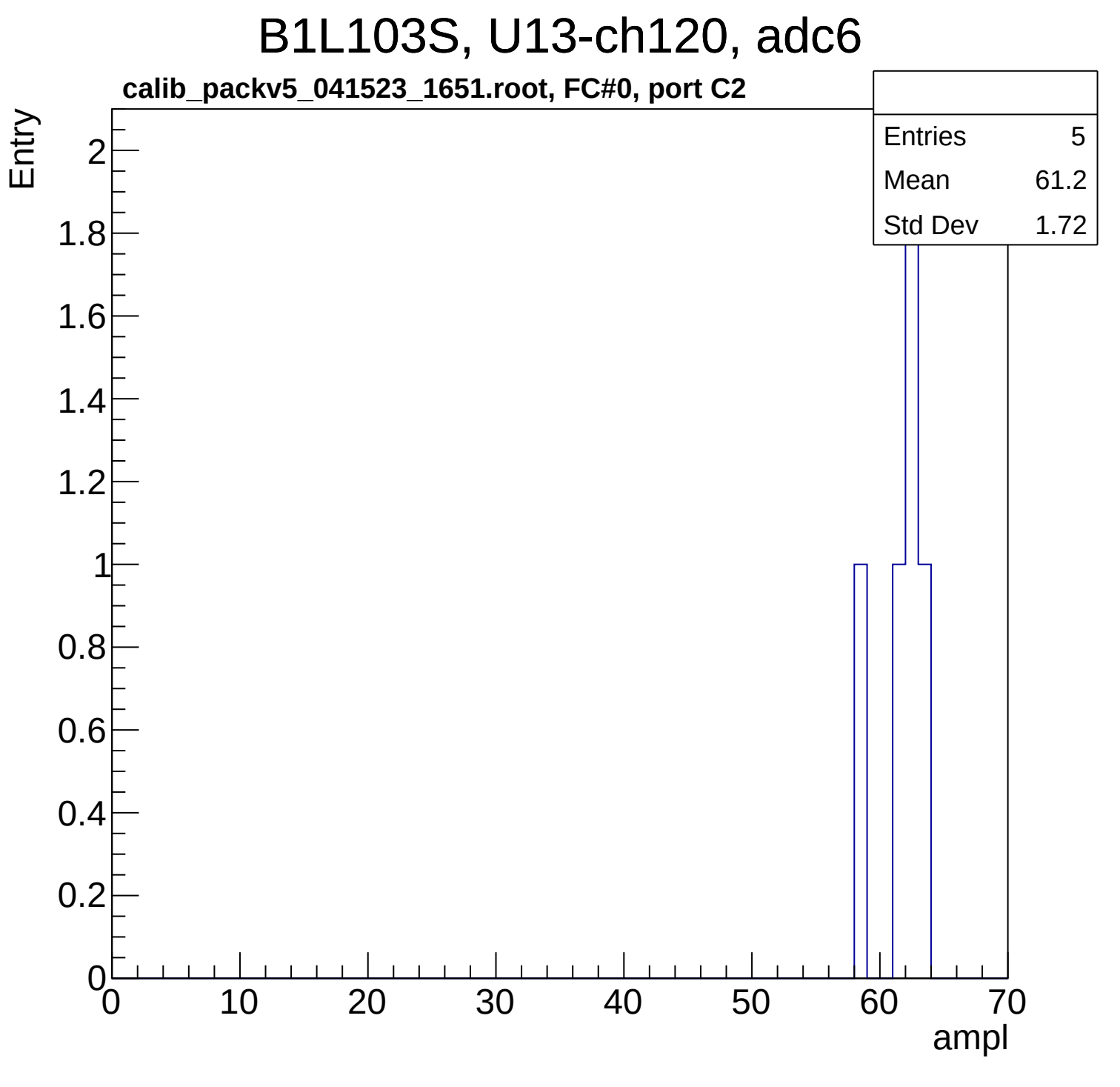
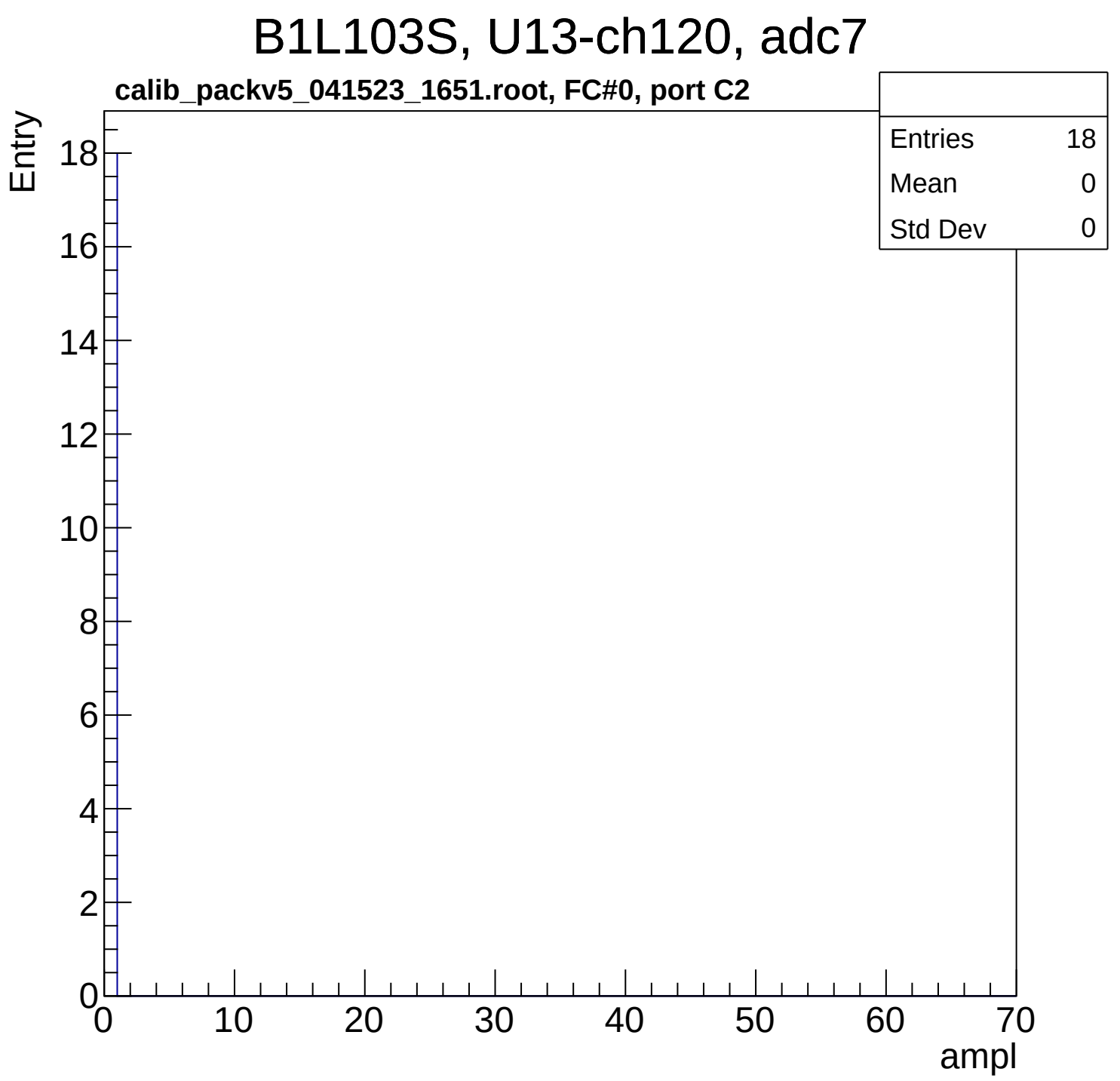
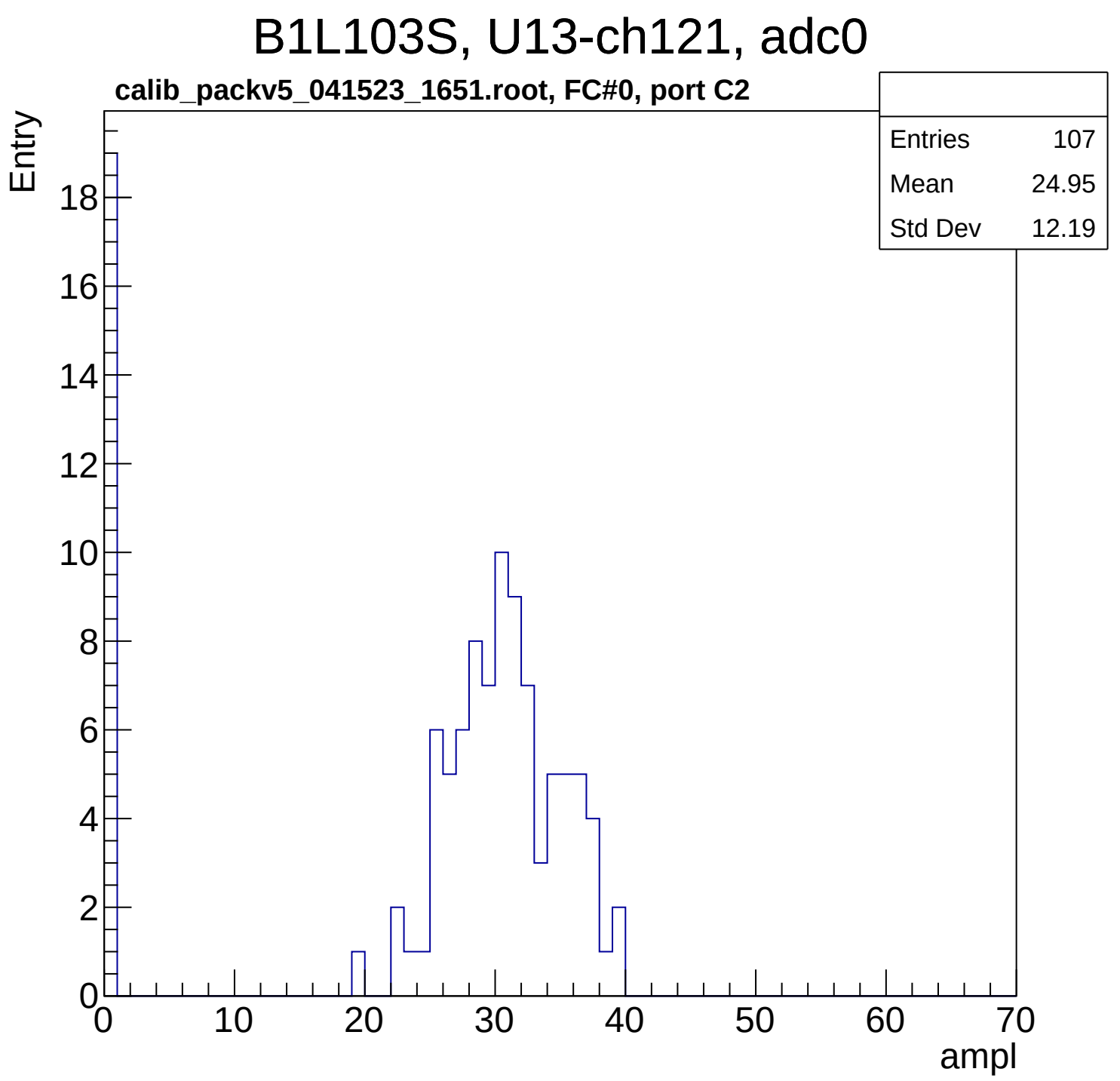
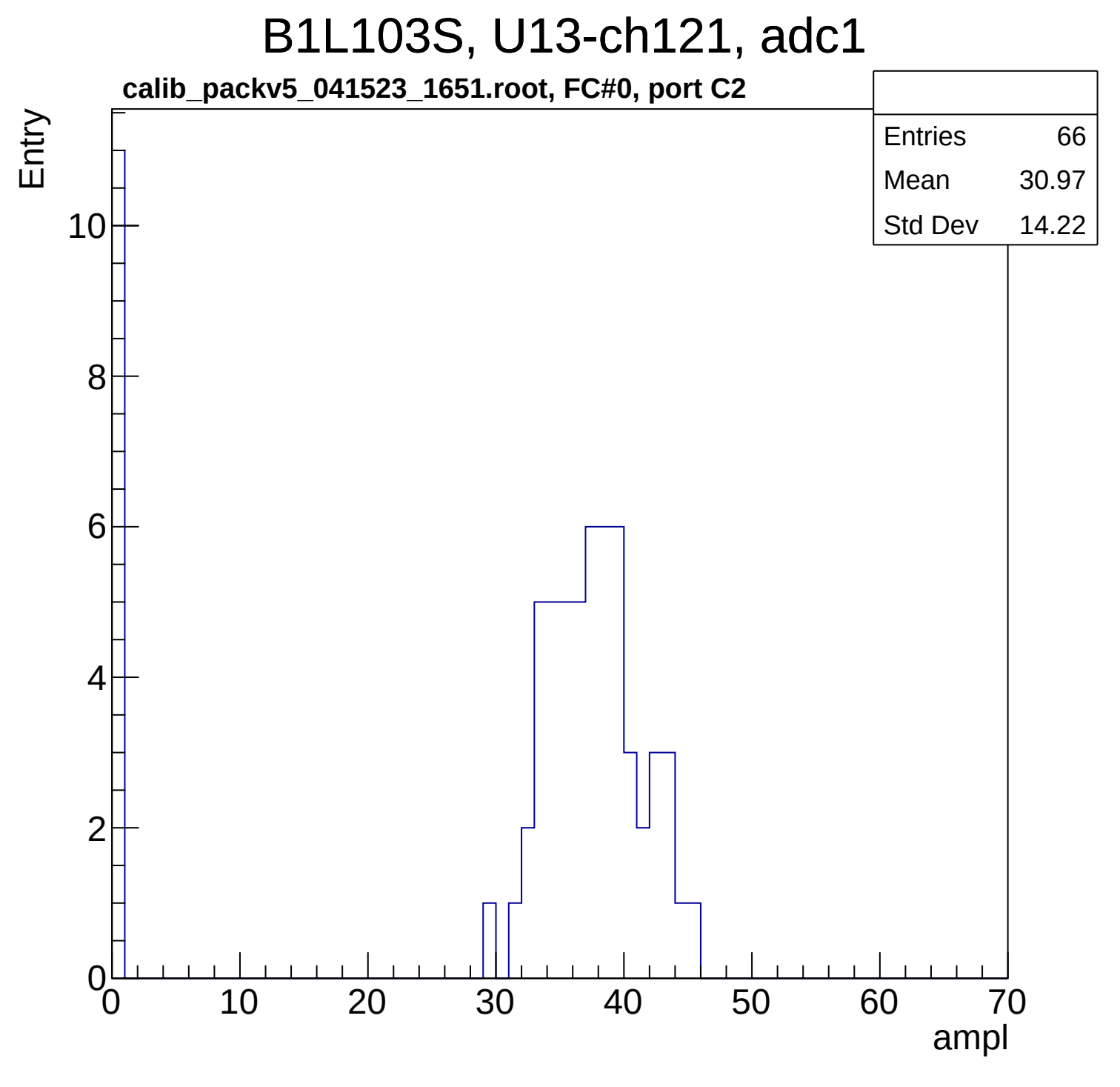
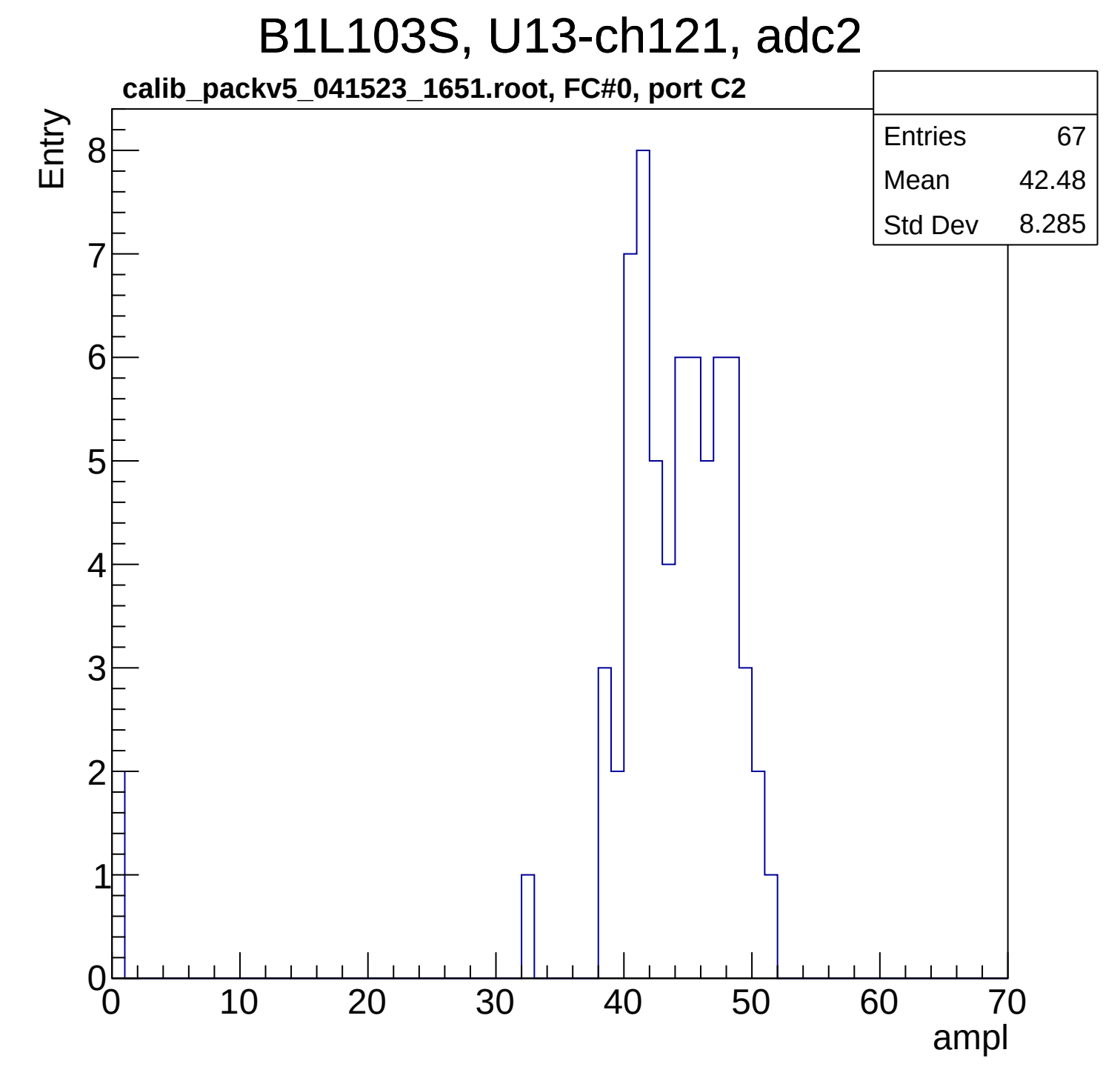
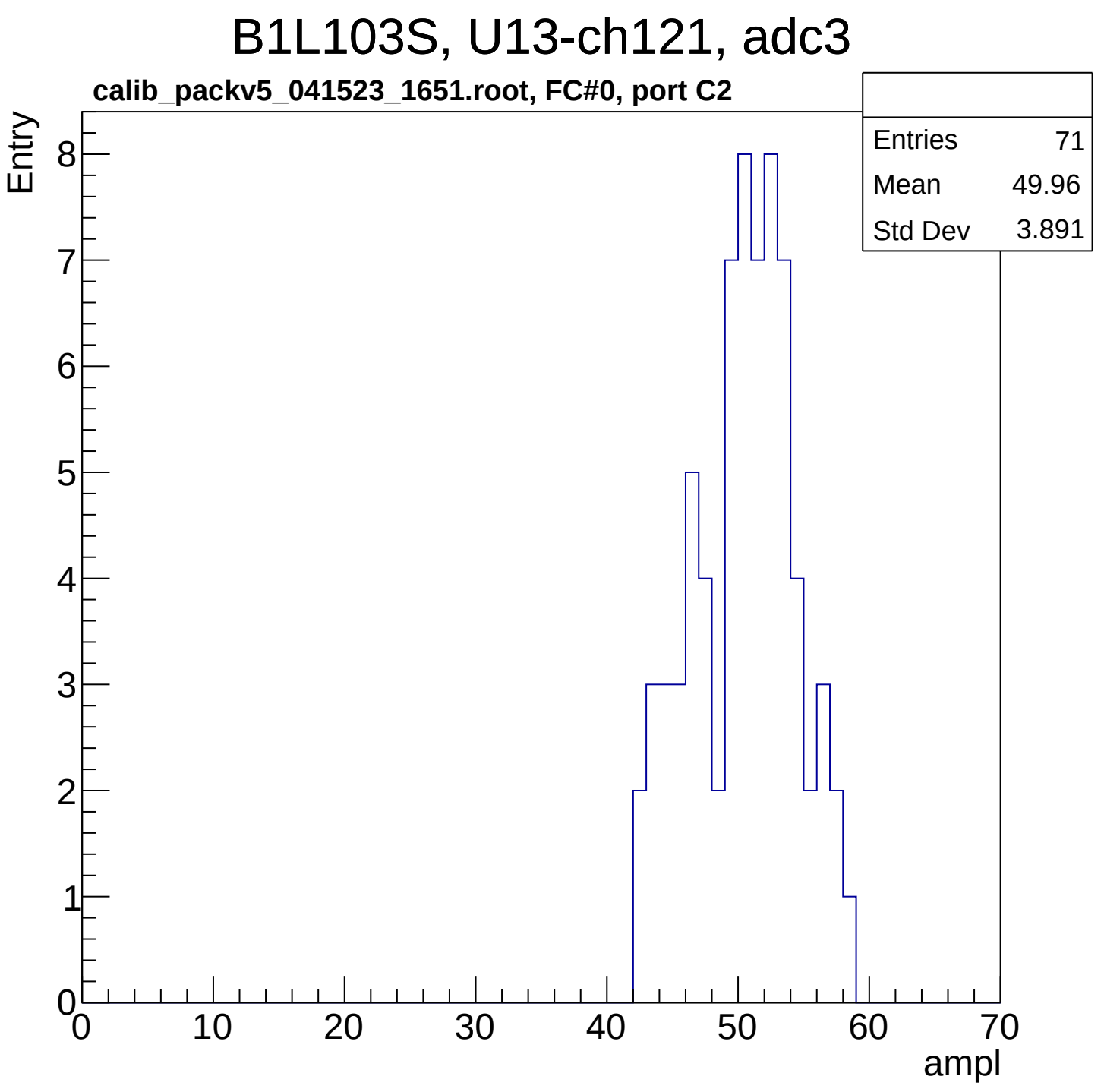

B1L103S, U13-ch120, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.2
Std Dev 1.72
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

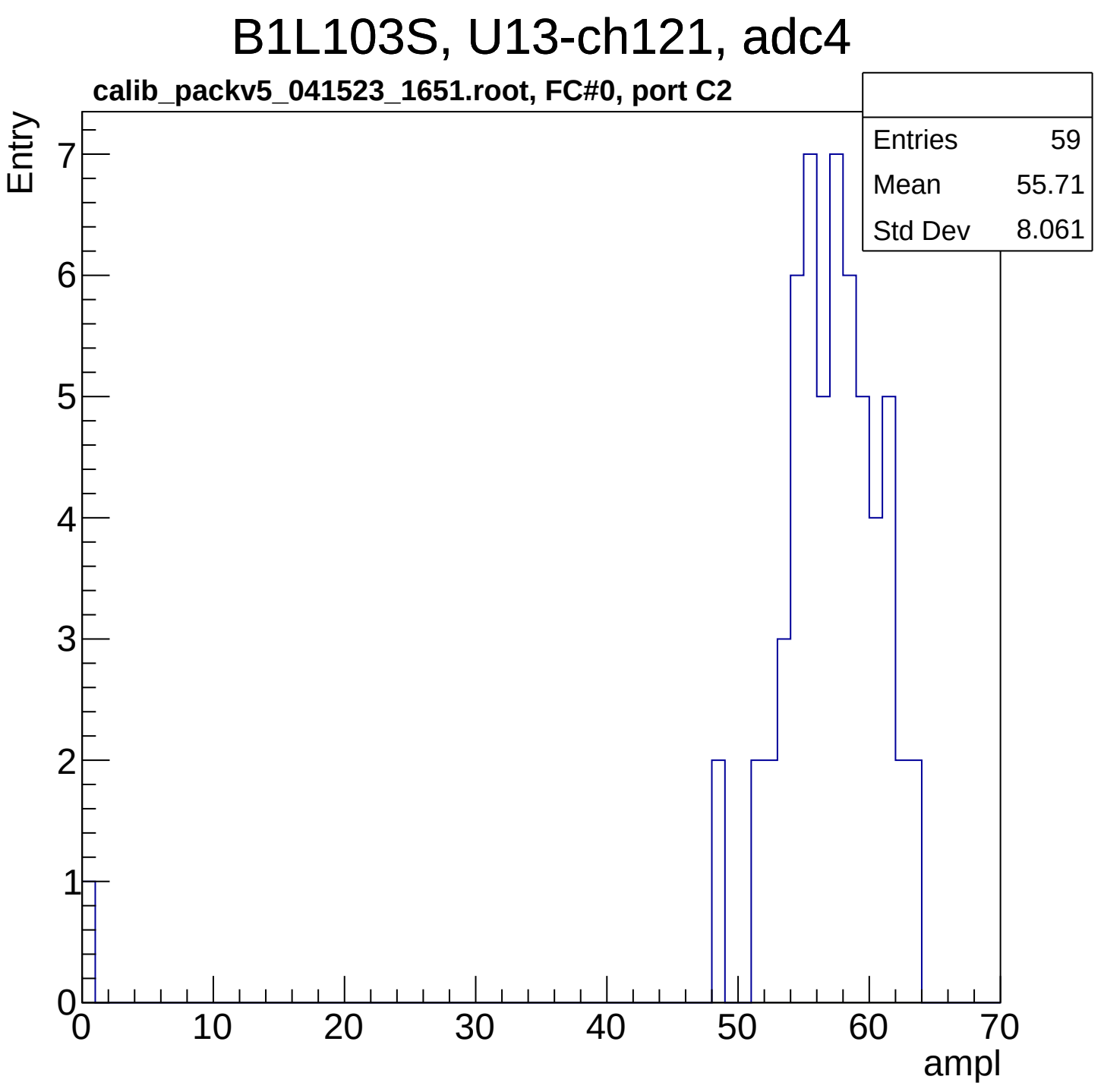

B1L103S, U13-ch120, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

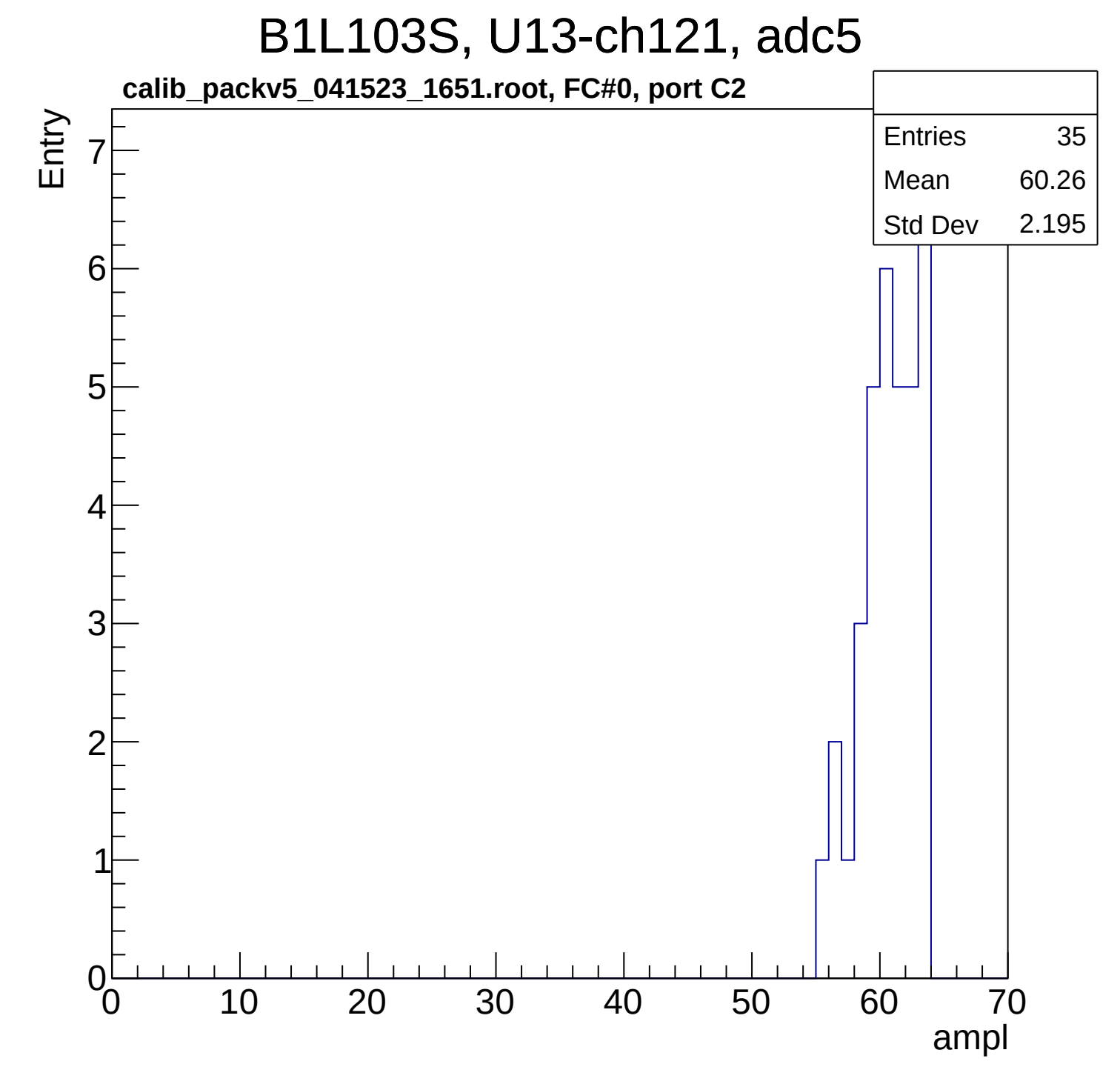

B1L103S, U13-ch121, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 107
Mean 24.95
Std Dev 12.19
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

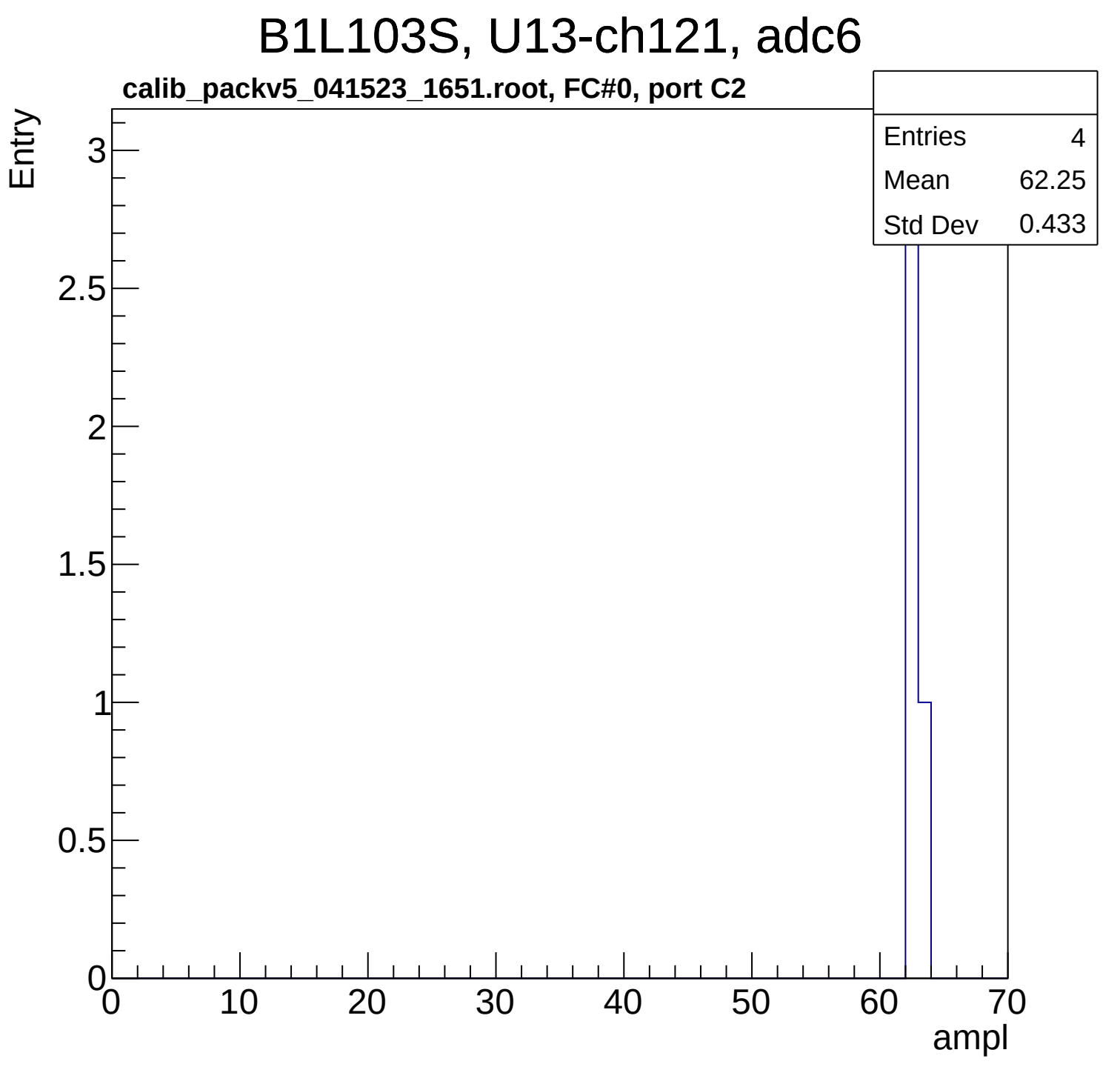

B1L103S, U13-ch121, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 30.97
Std Dev 14.22
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

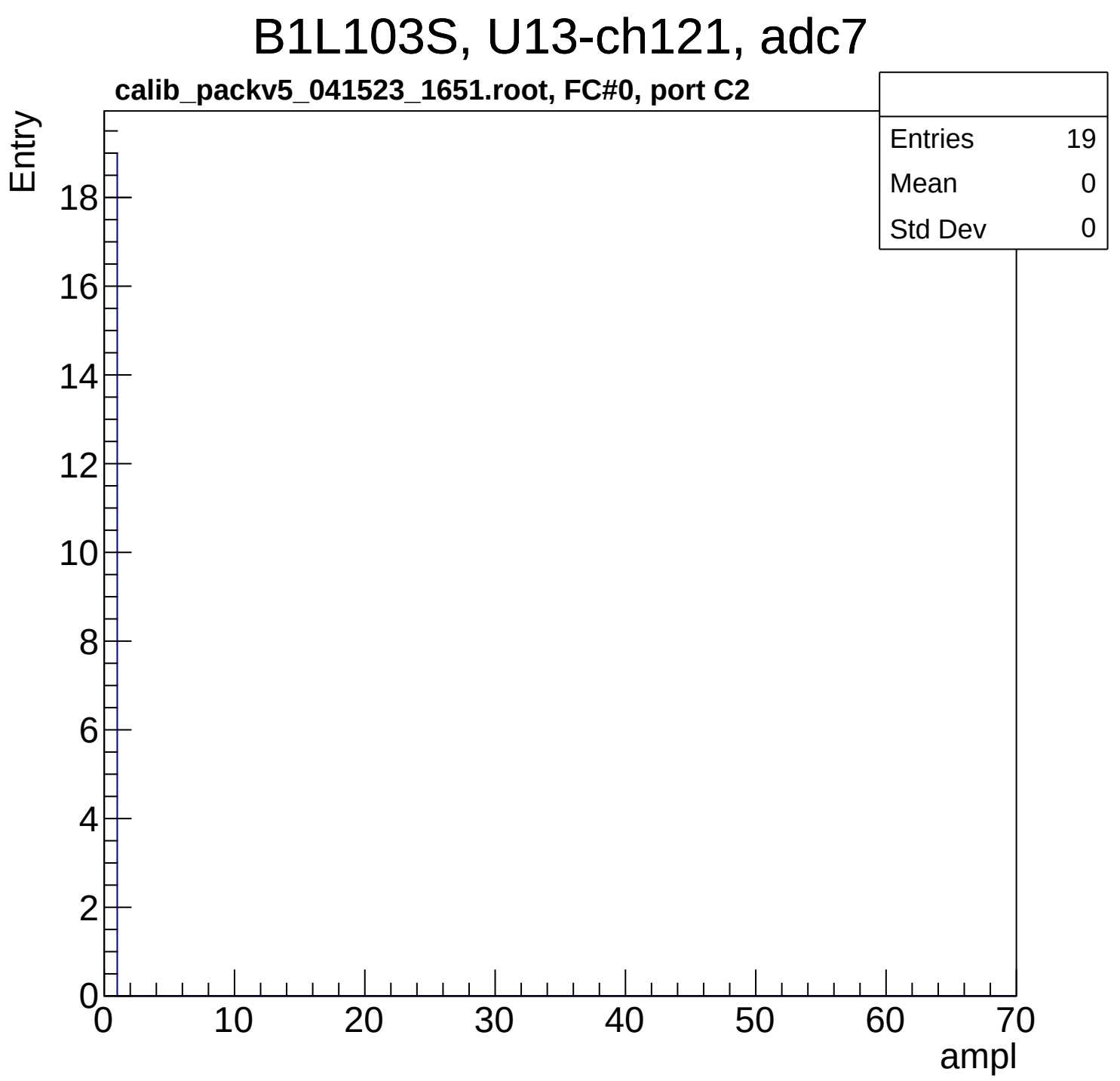

B1L103S, U13-ch121, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 42.48
Std Dev 8.285
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

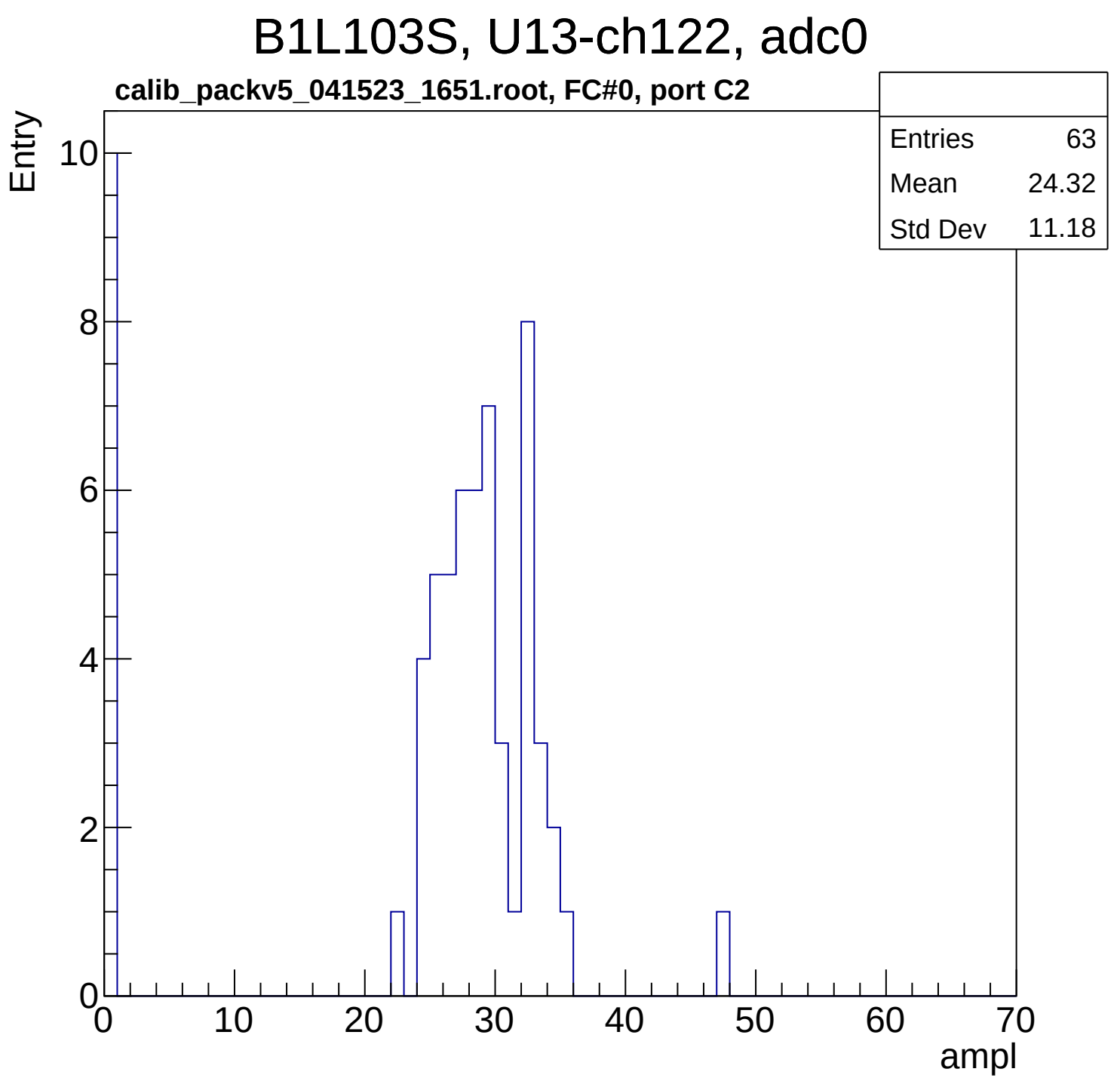

B1L103S, U13-ch121, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 49.96
Std Dev 3.891
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

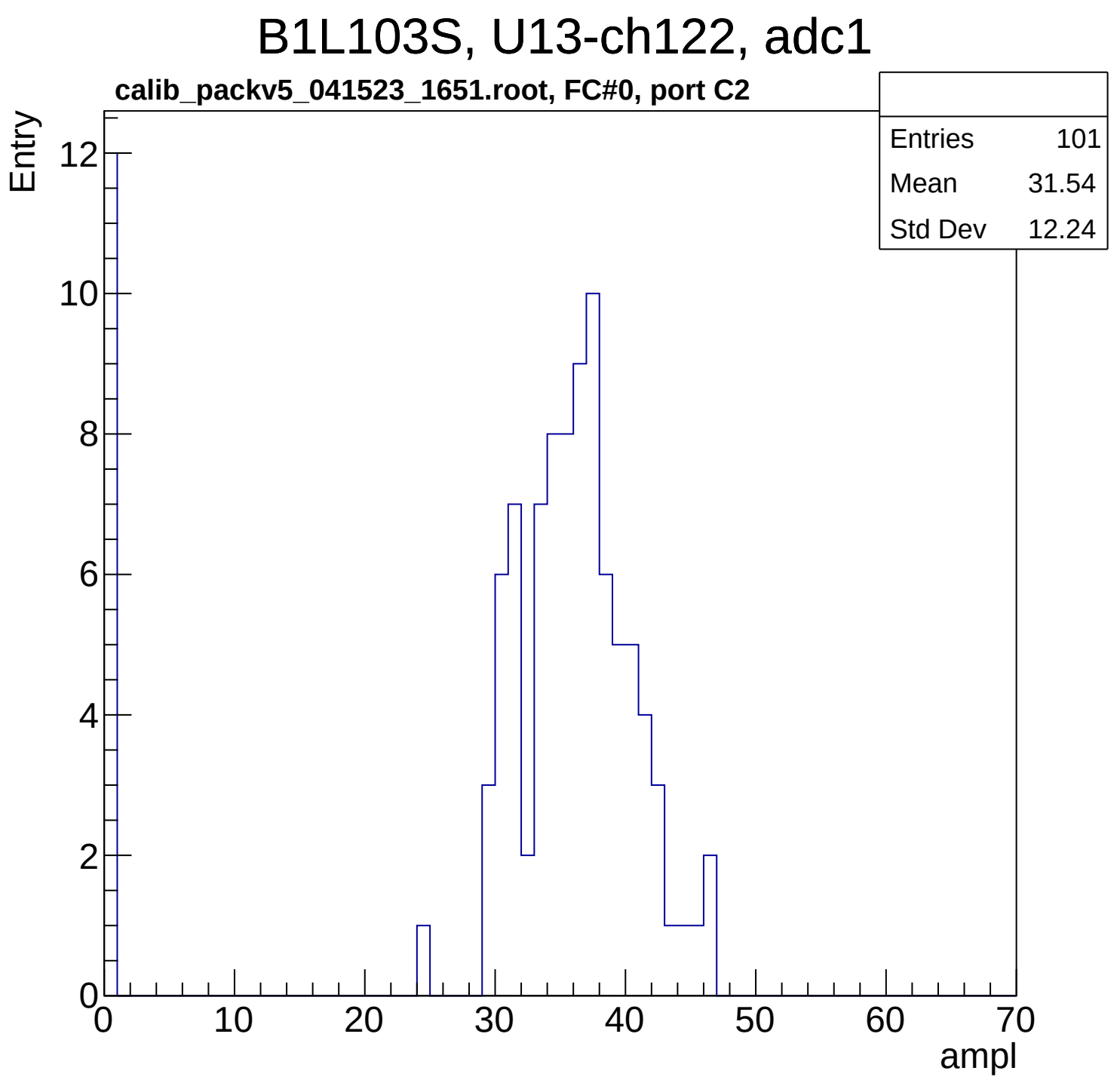

B1L103S, U13-ch121, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 55.71
Std Dev 8.061
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

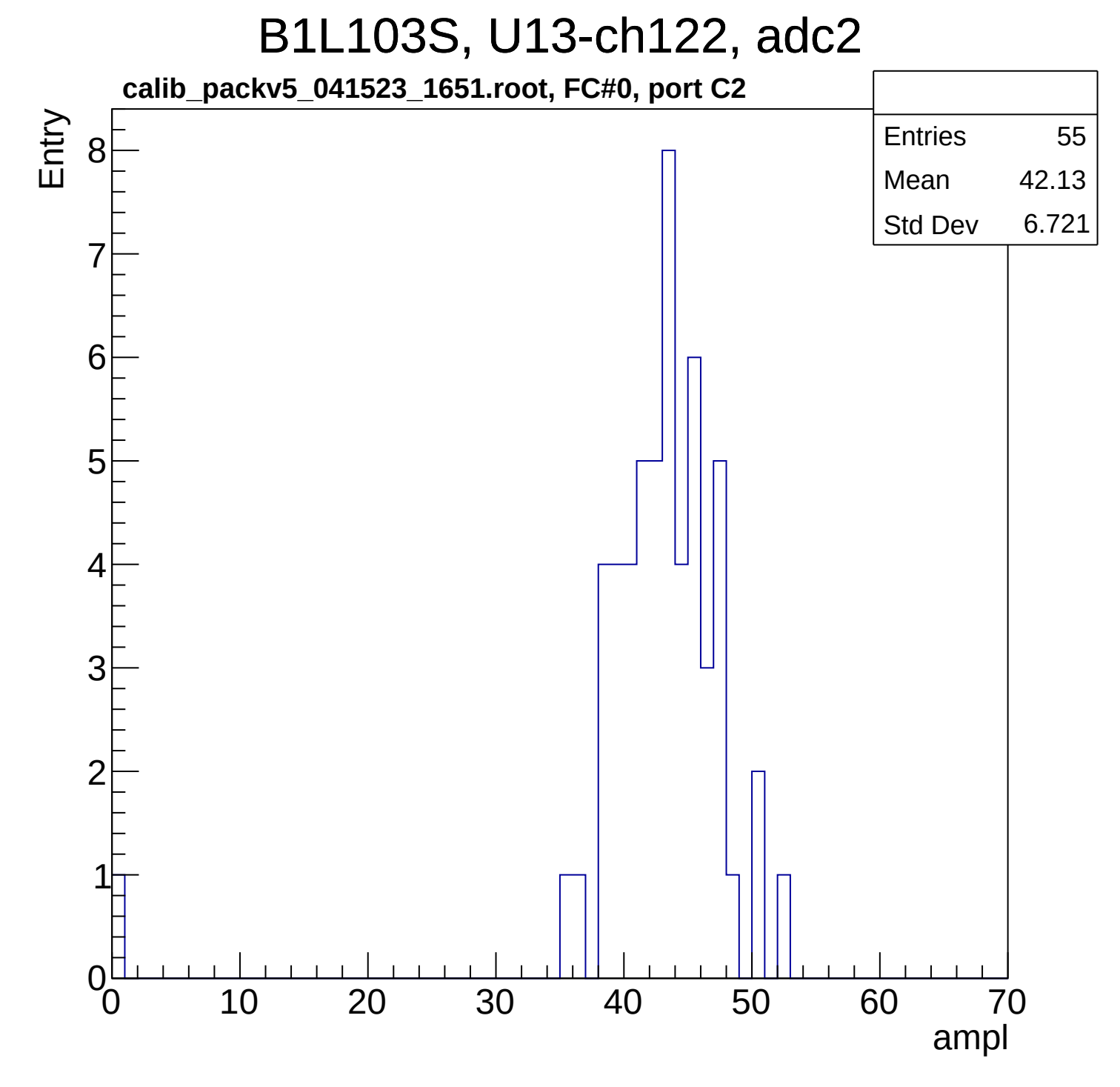

B1L103S, U13-ch121, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 60.26
Std Dev 2.195
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

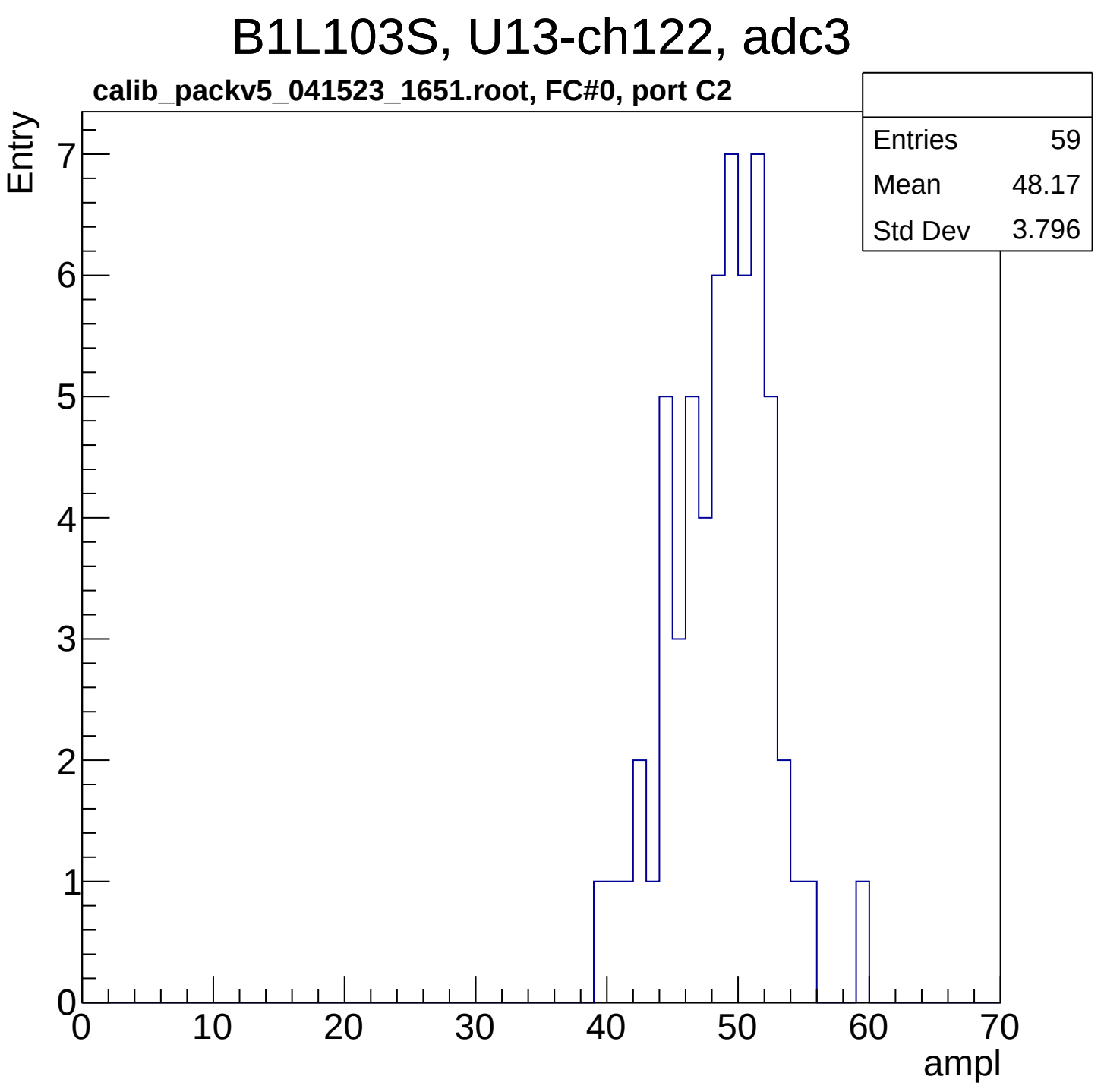

B1L103S, U13-ch121, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.25
Std Dev 0.433
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

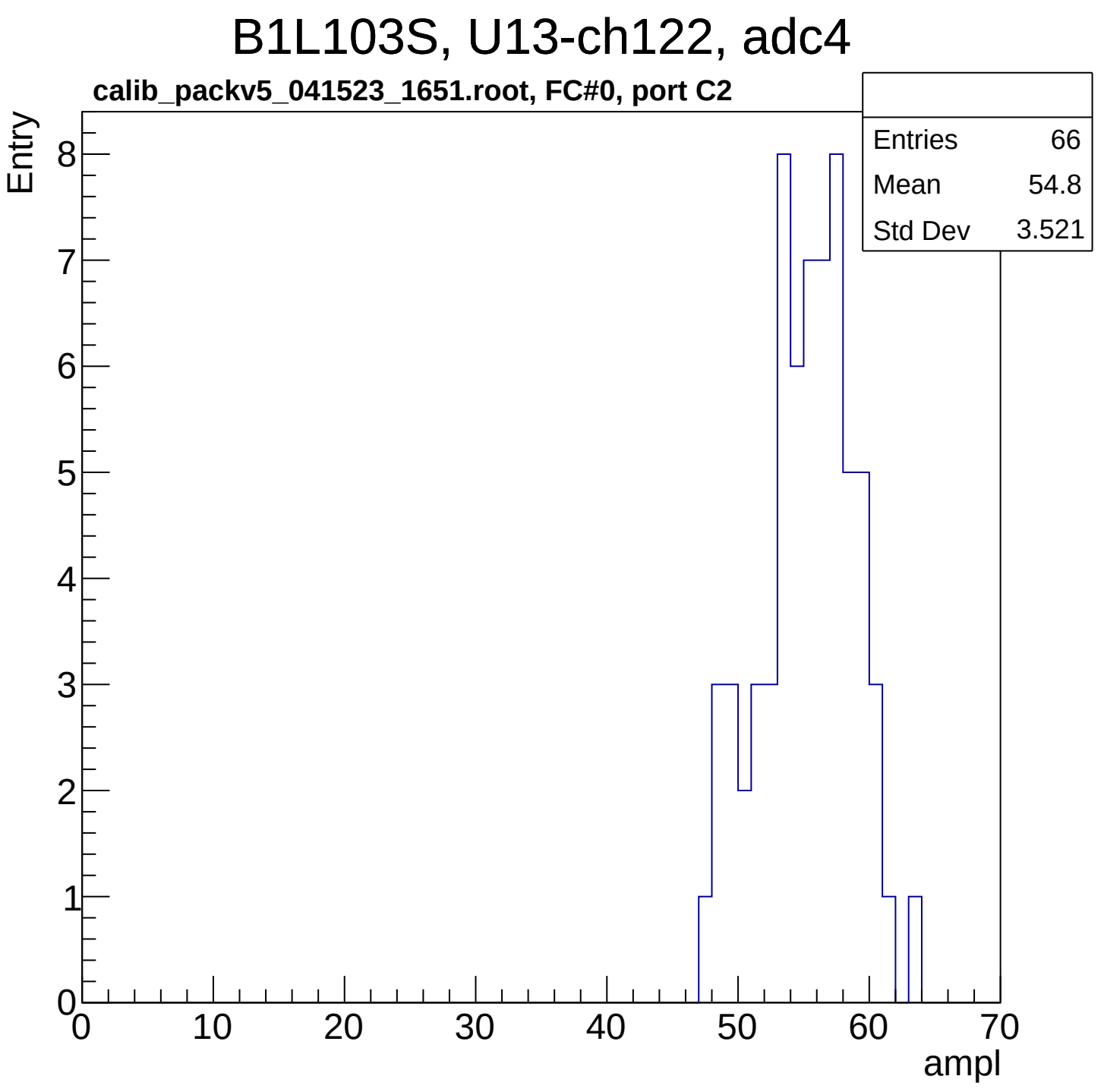

B1L103S, U13-ch121, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

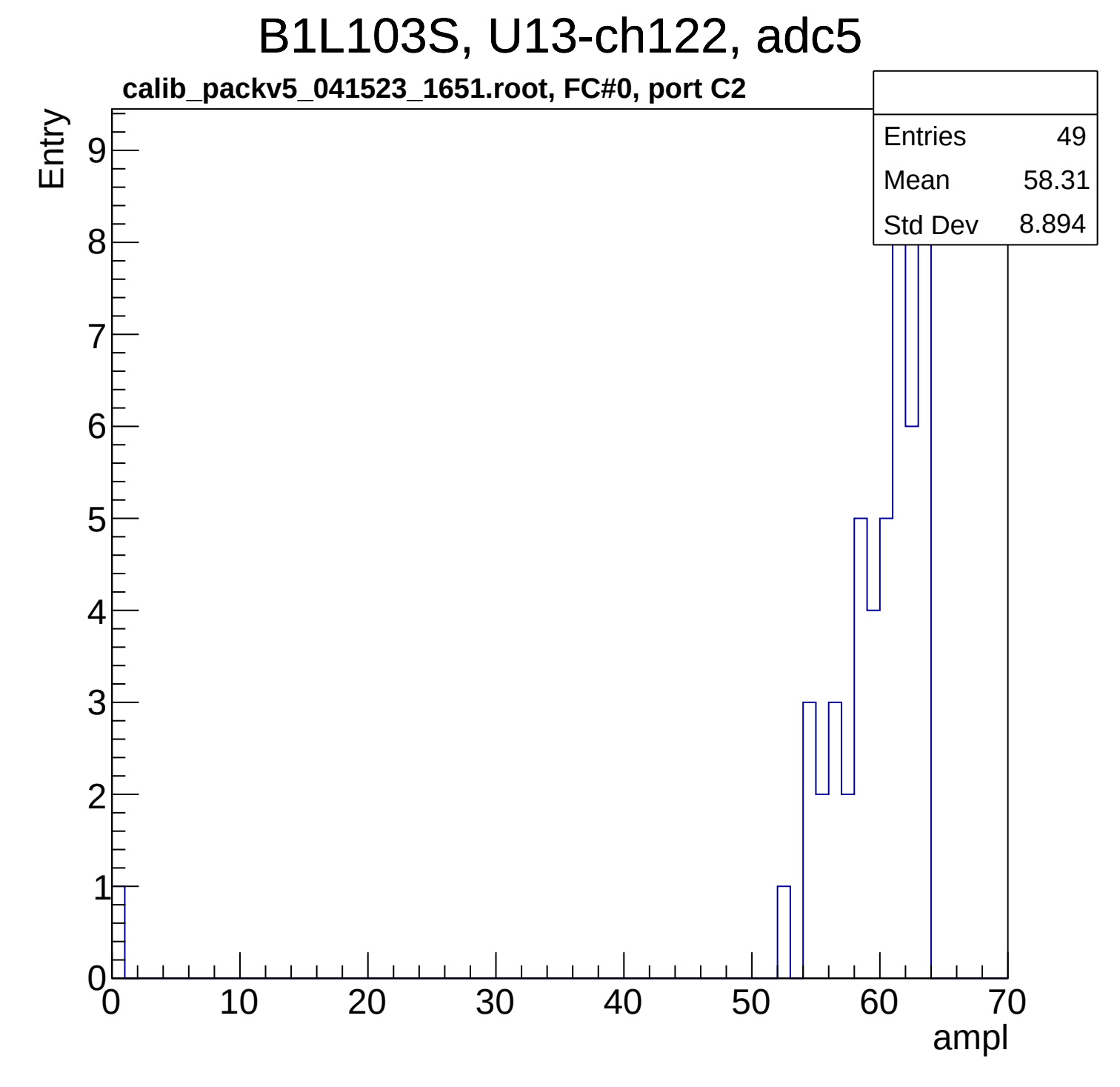

B1L103S, U13-ch122, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 24.32
Std Dev 11.18
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

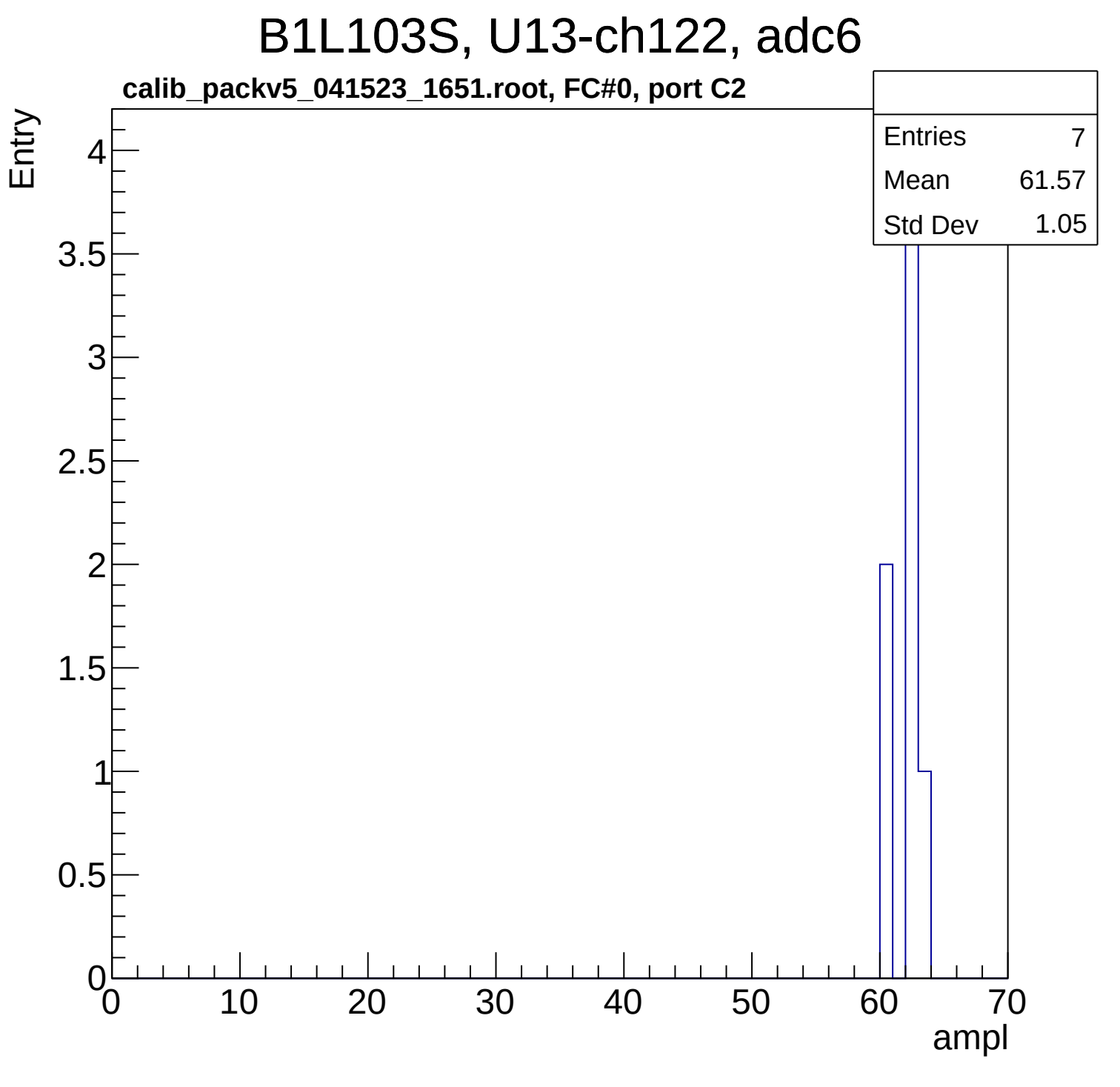

B1L103S, U13-ch122, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 31.54
Std Dev 12.24
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

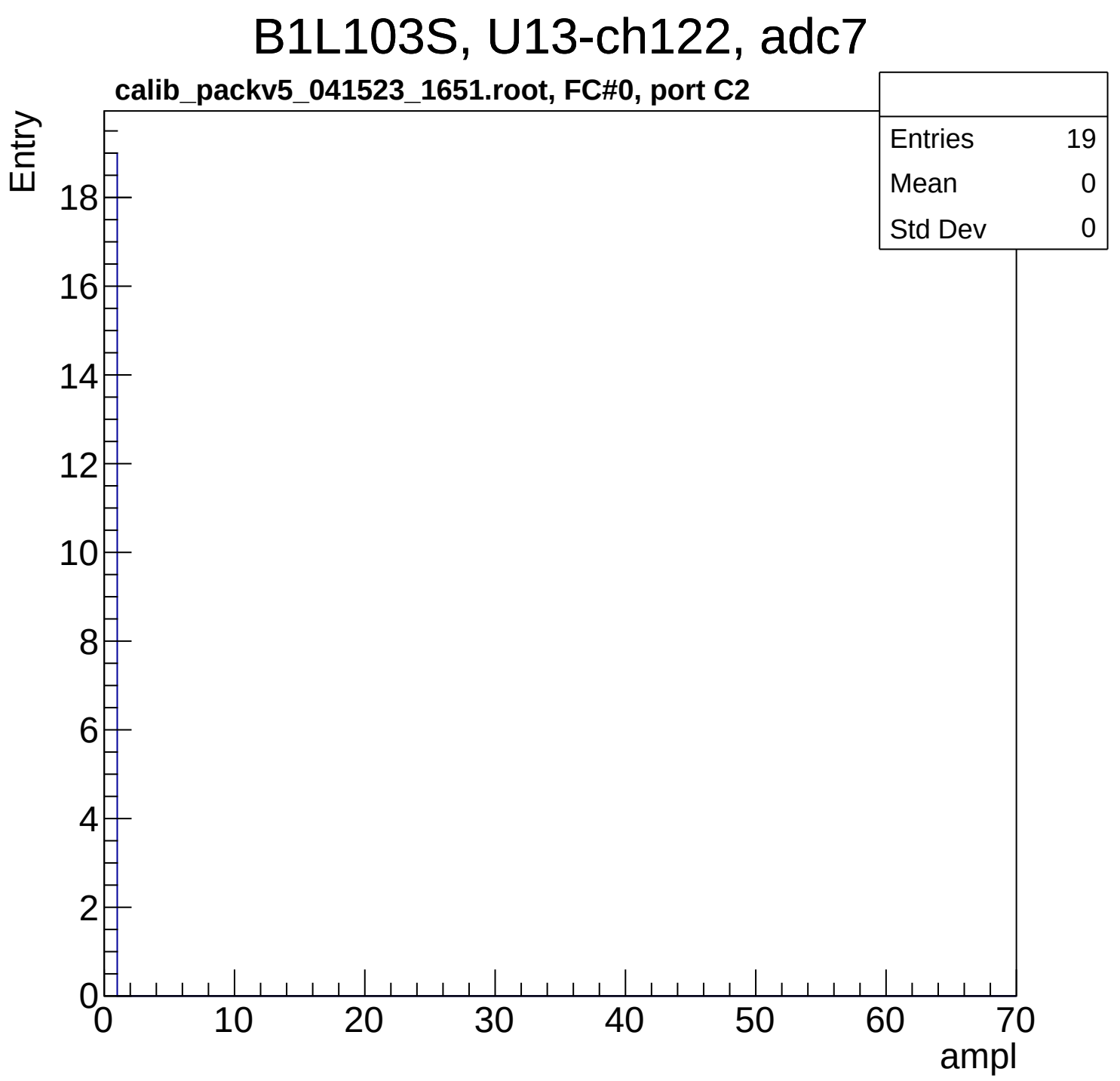

B1L103S, U13-ch122, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 42.13
Std Dev 6.721
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

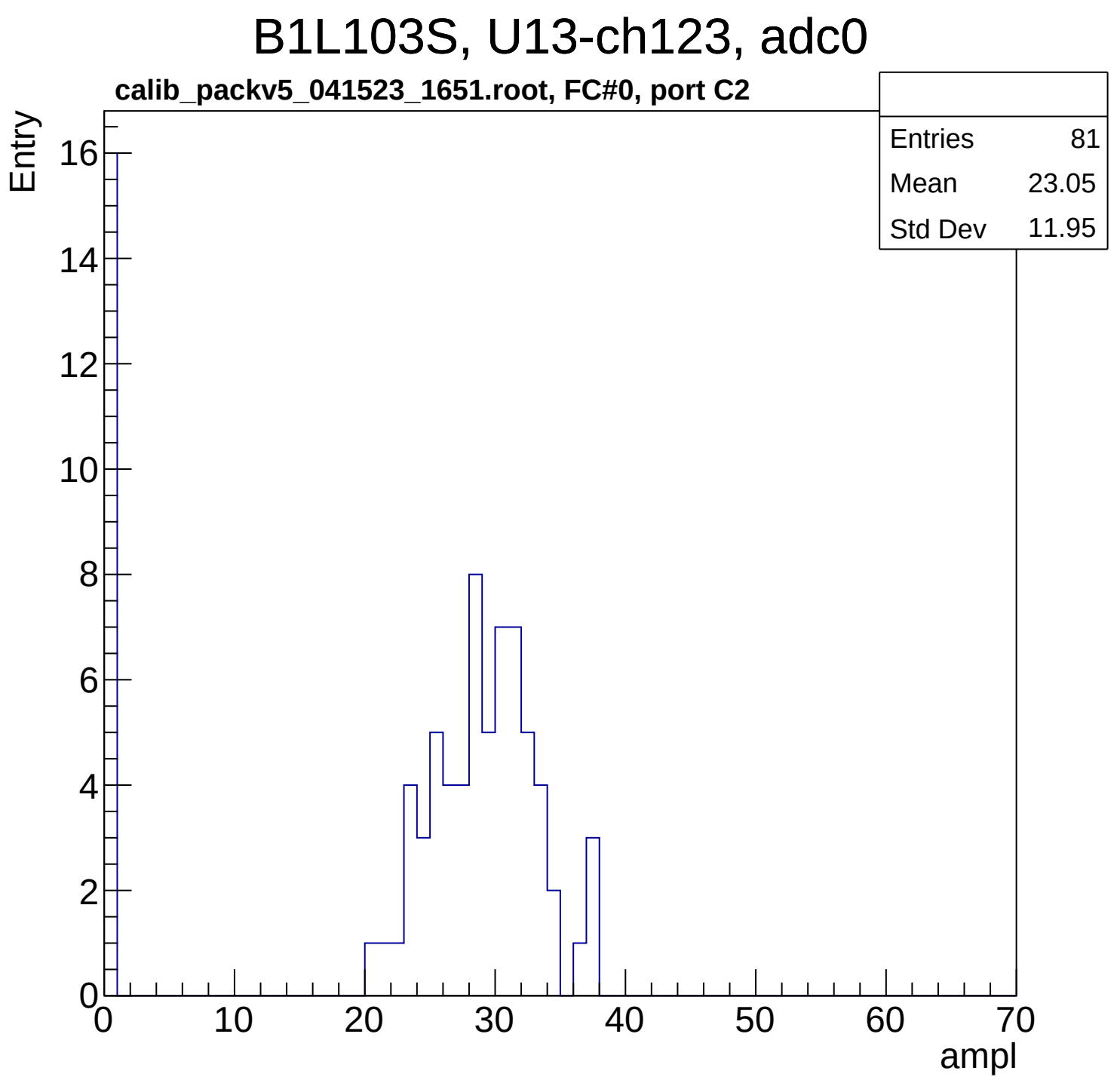

B1L103S, U13-ch122, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 48.17
Std Dev 3.796
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch122, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 54.8
Std Dev 3.521
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch122, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.31
Std Dev 8.894
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch122, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.57
Std Dev 1.05
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U13-ch122, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch123, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 23.05
Std Dev 11.95
Entry
ampl
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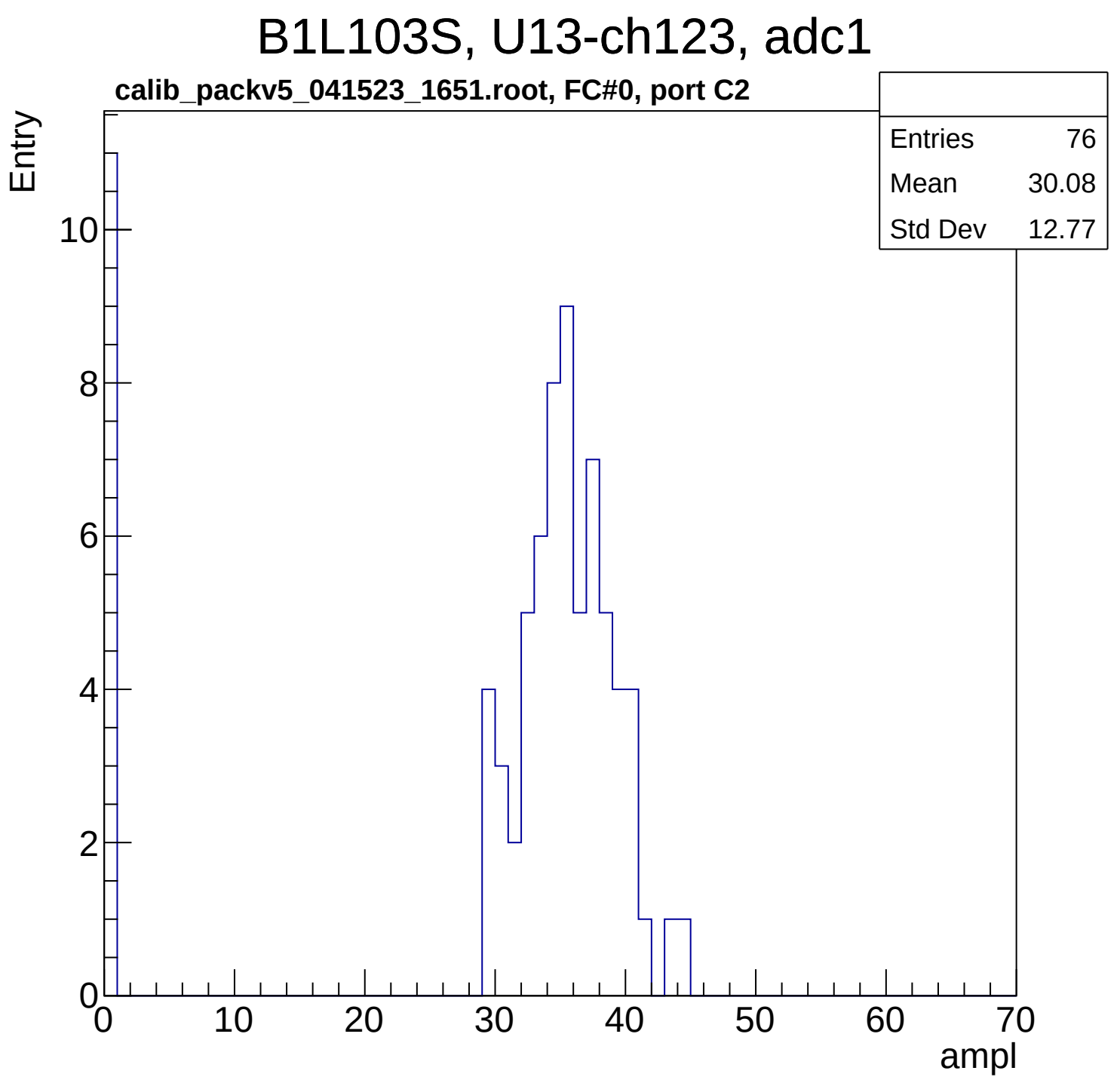
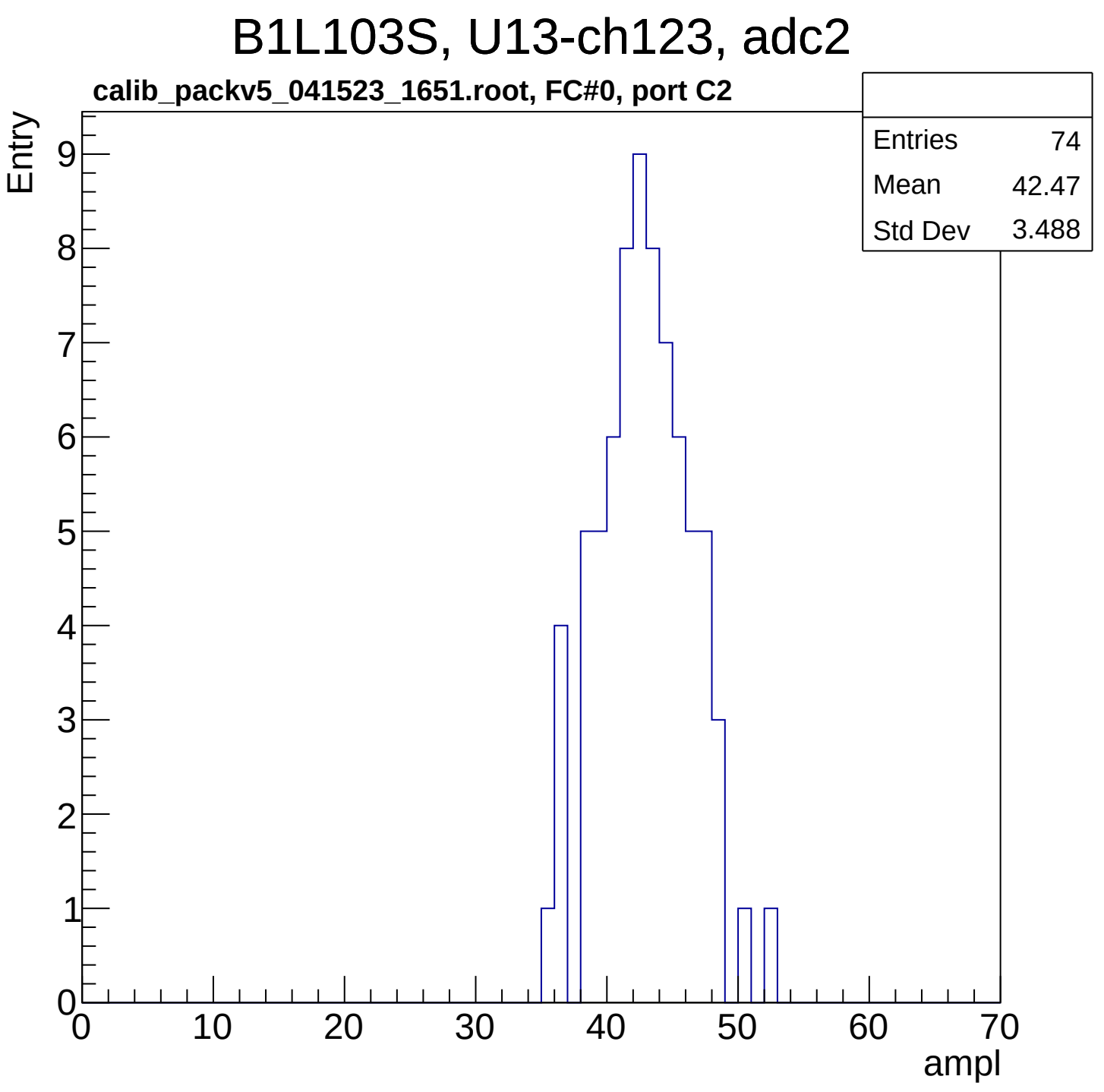
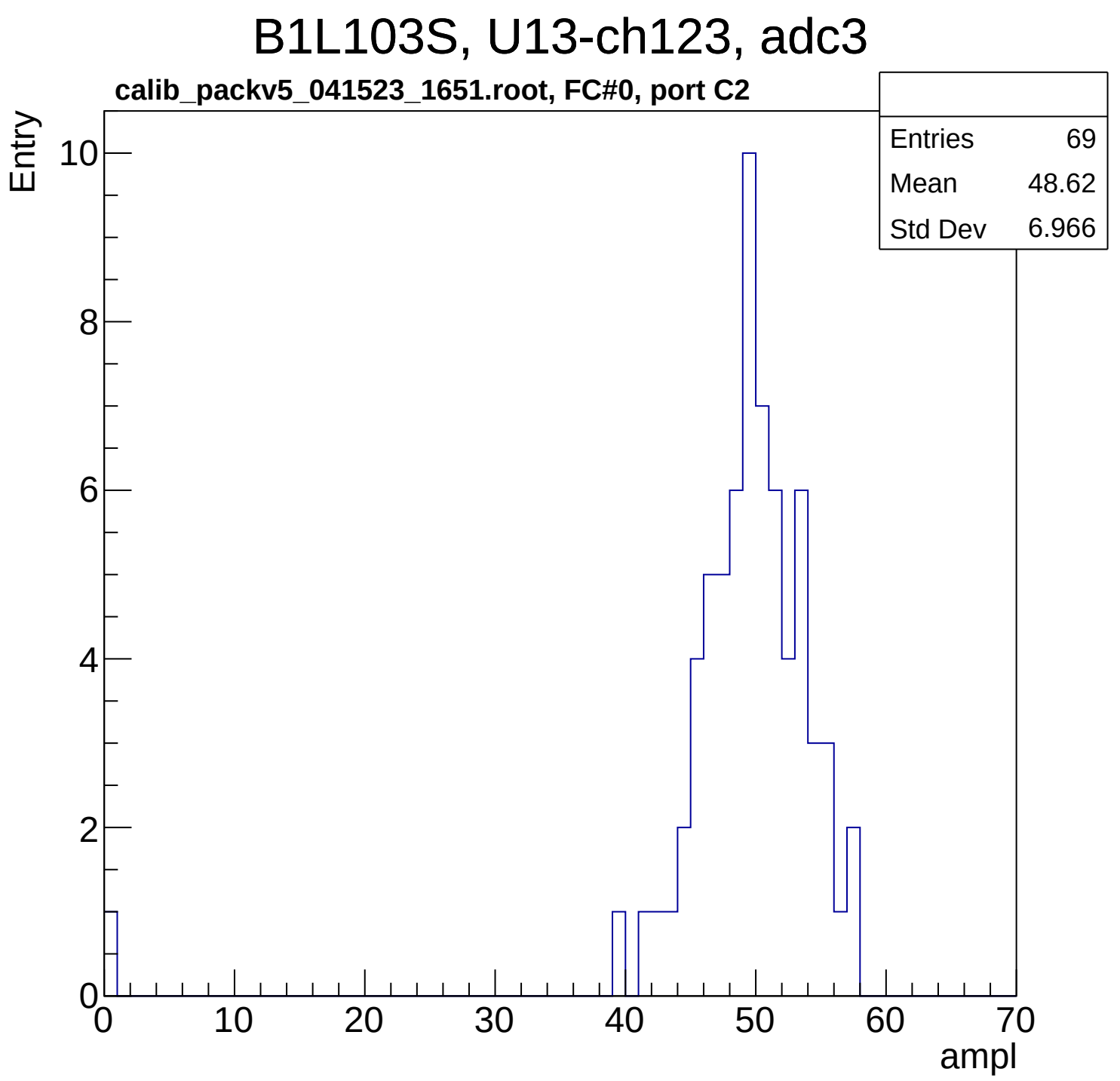
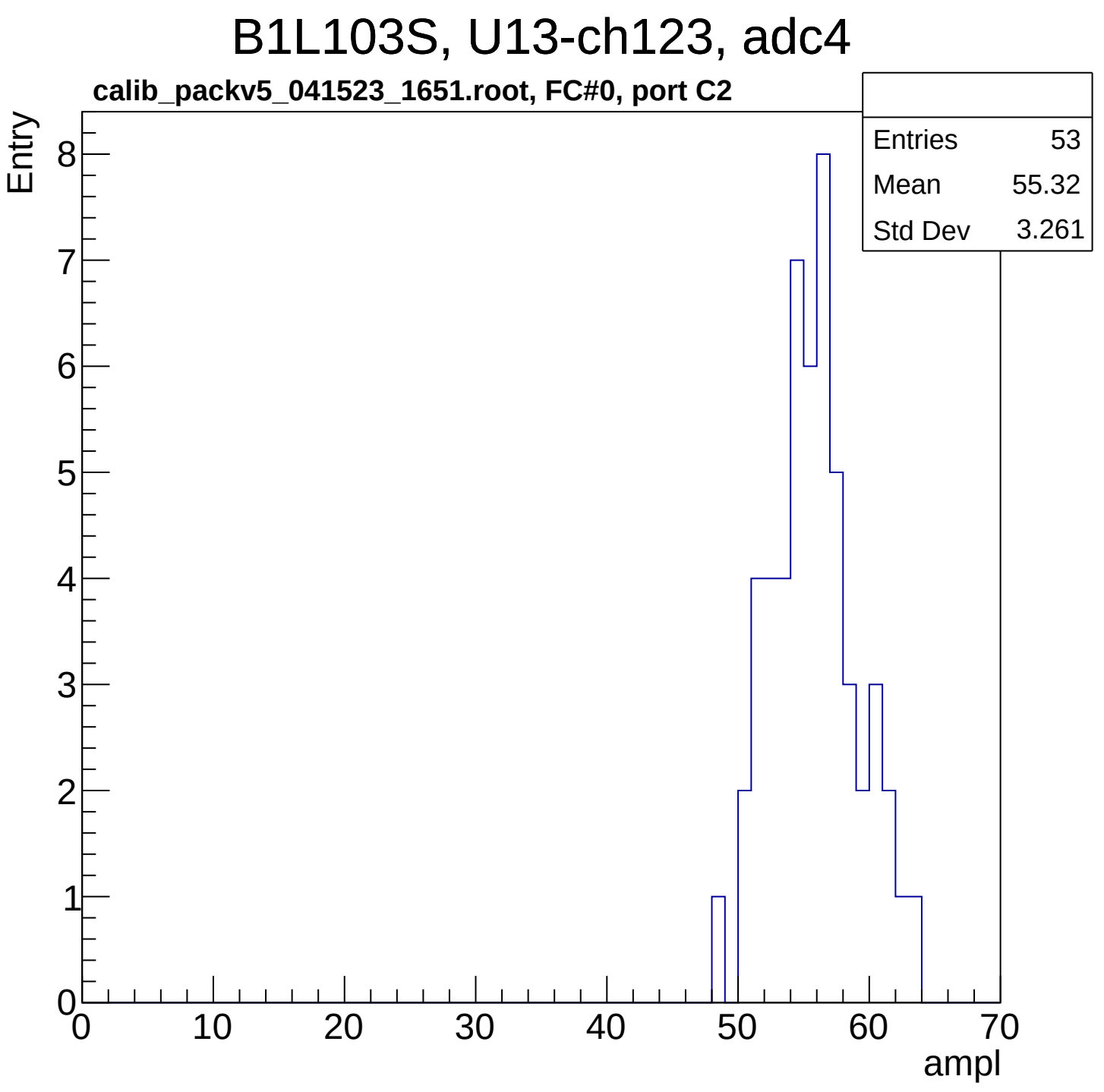
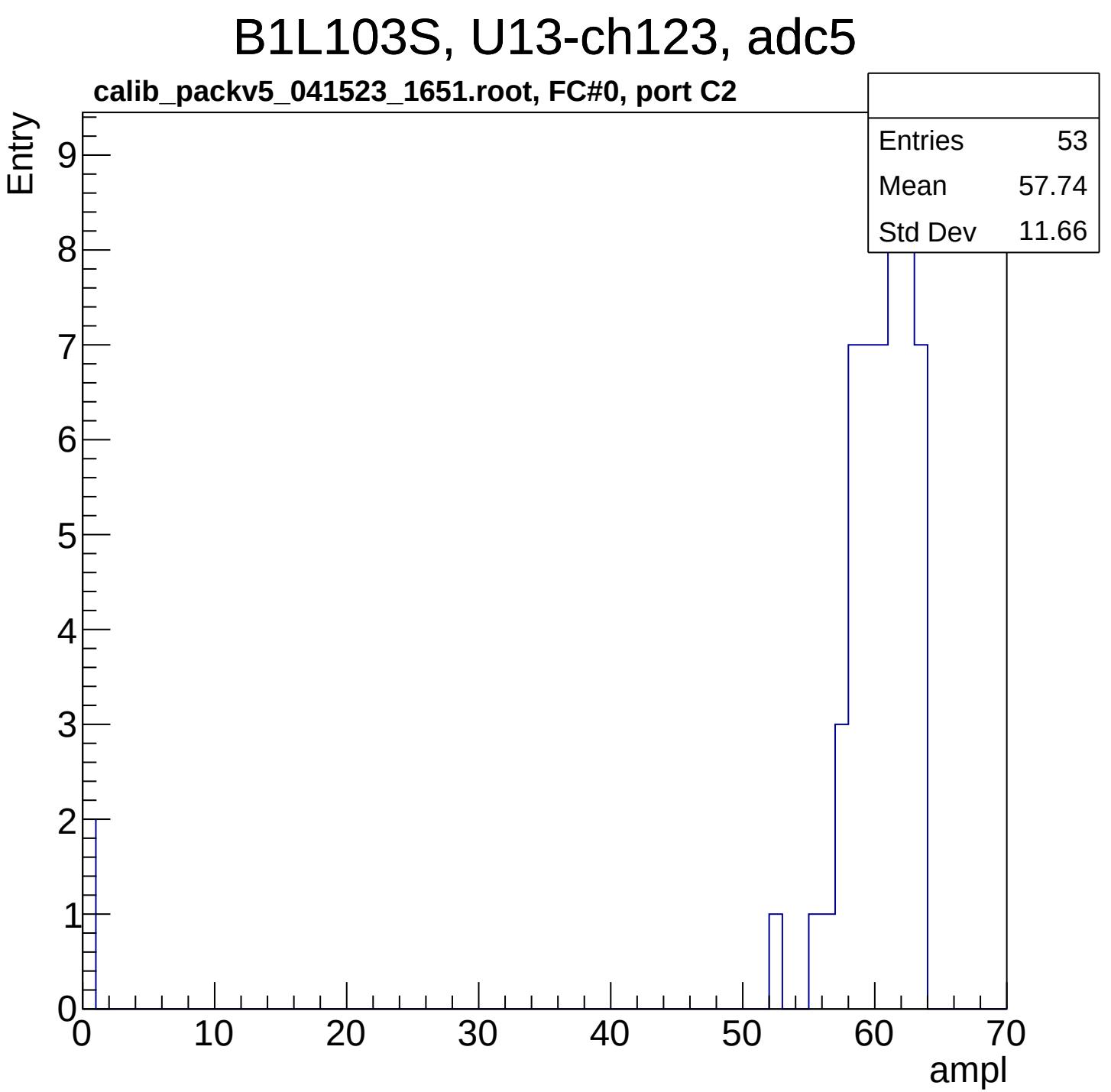
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

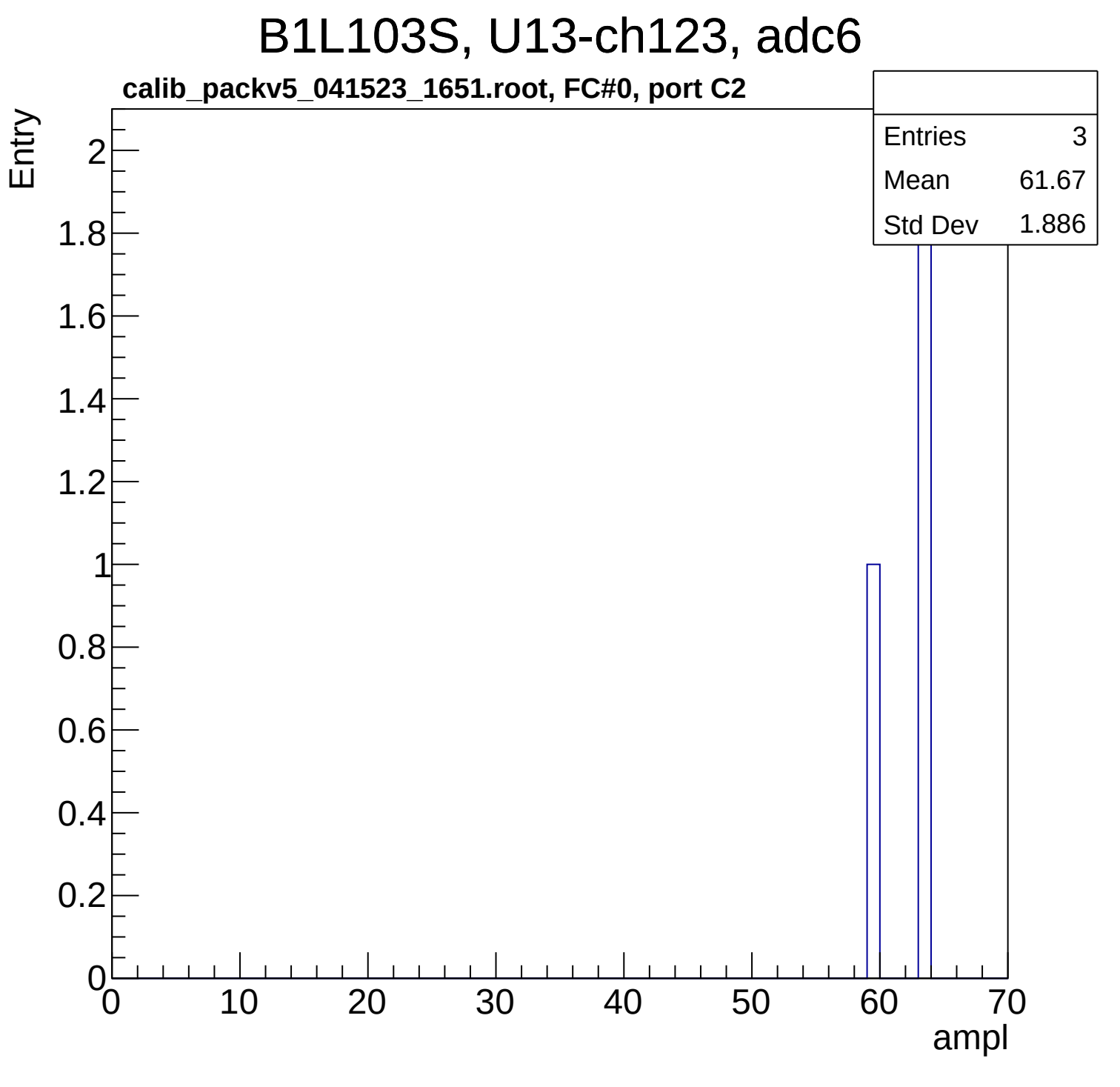

B1L103S, U13-ch123, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 30.08
Std Dev 12.77
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

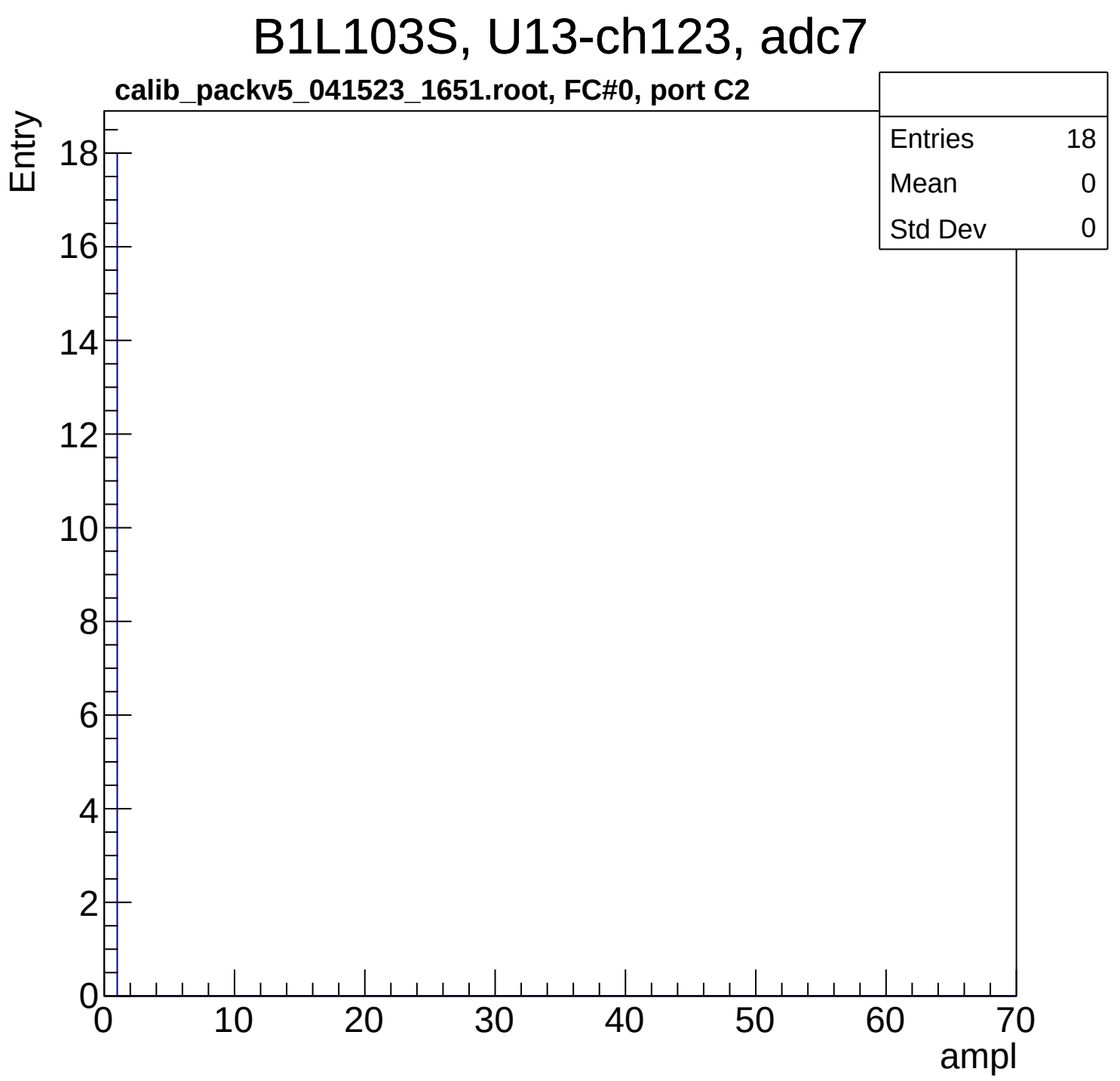

B1L103S, U13-ch123, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 42.47
Std Dev 3.488
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

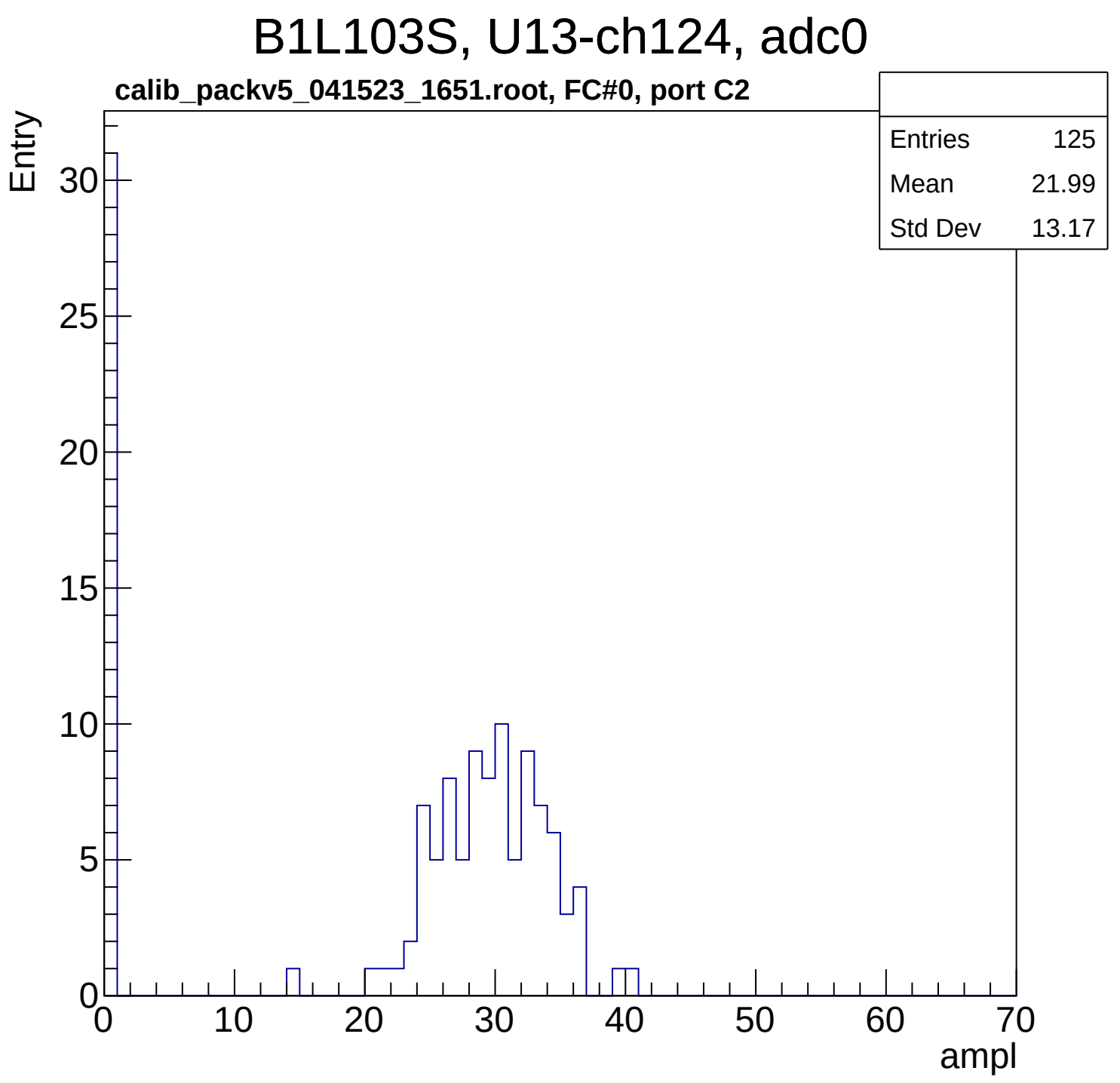

B1L103S, U13-ch123, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 48.62
Std Dev 6.966
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch123, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 55.32
Std Dev 3.261
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch123, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 57.74
Std Dev 11.66
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch123, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 61.67
Std Dev 1.886
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U13-ch123, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch124, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 125
Mean 21.99
Std Dev 13.17
Entry
0
5
10
15
20
25
30
0
10
20
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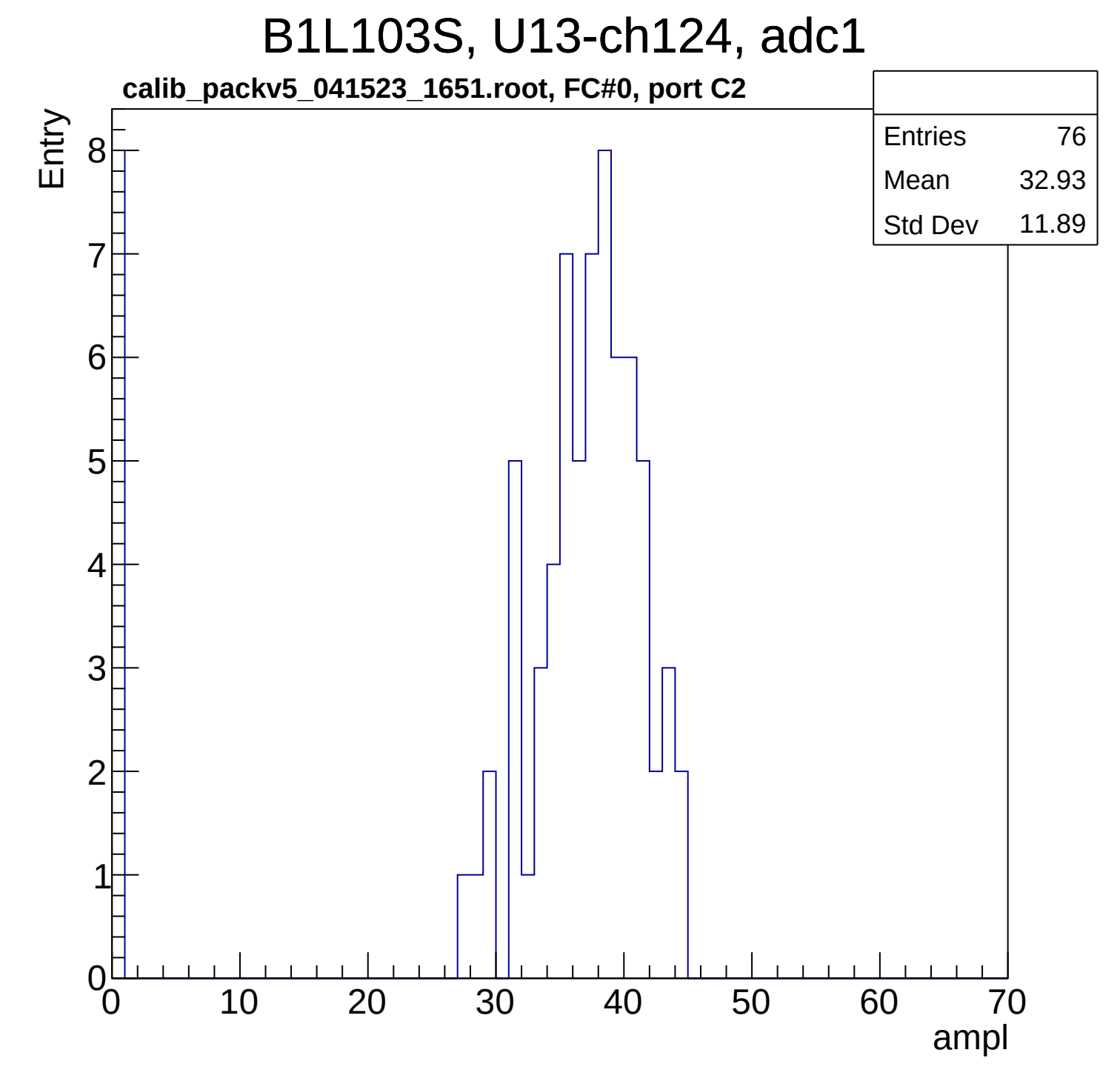
50
60
70
ampl


B1L103S, U13-ch124, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 32.93
Std Dev 11.89
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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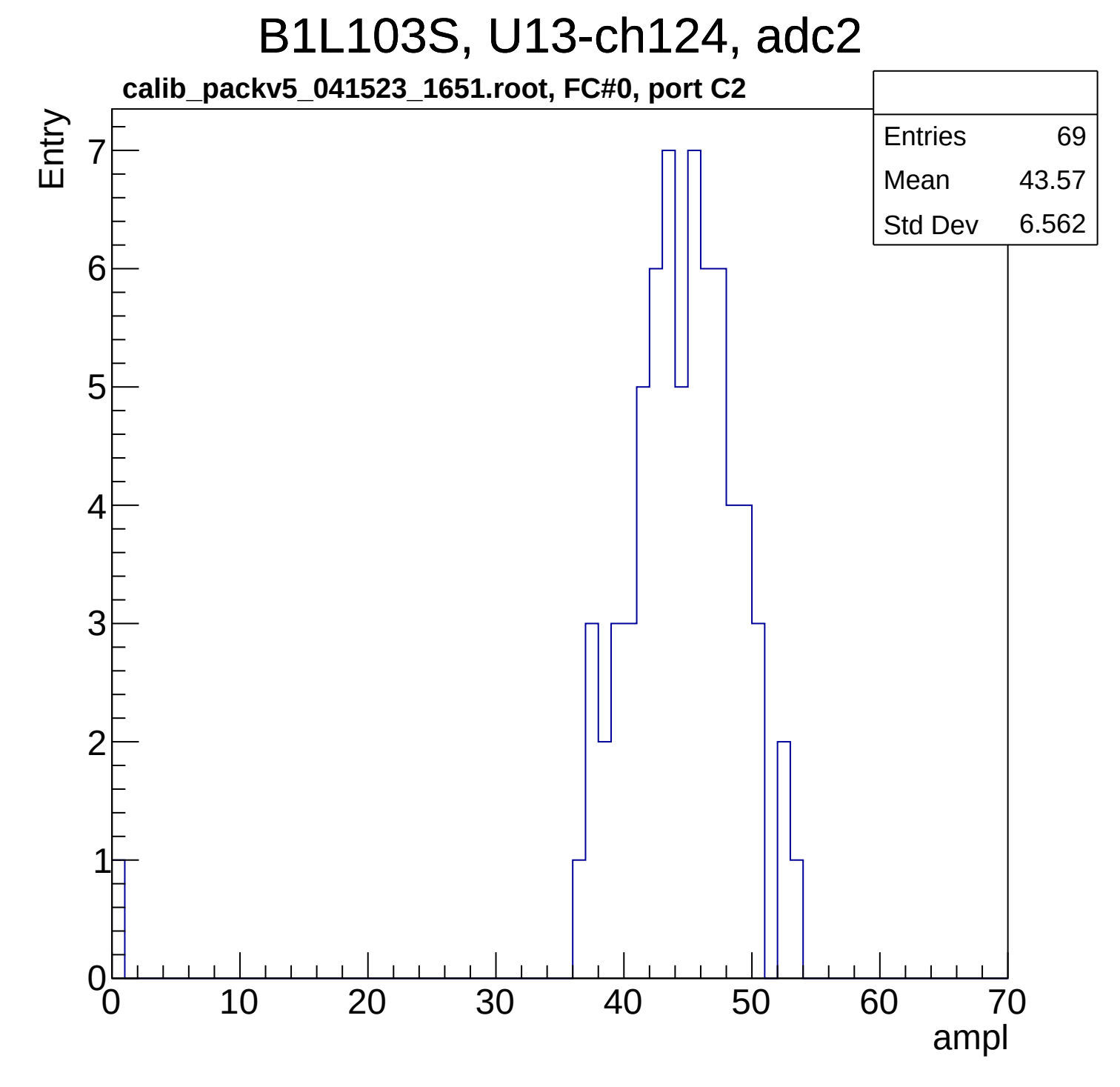
B1L103S, U13-ch124, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 43.57
Std Dev 6.562
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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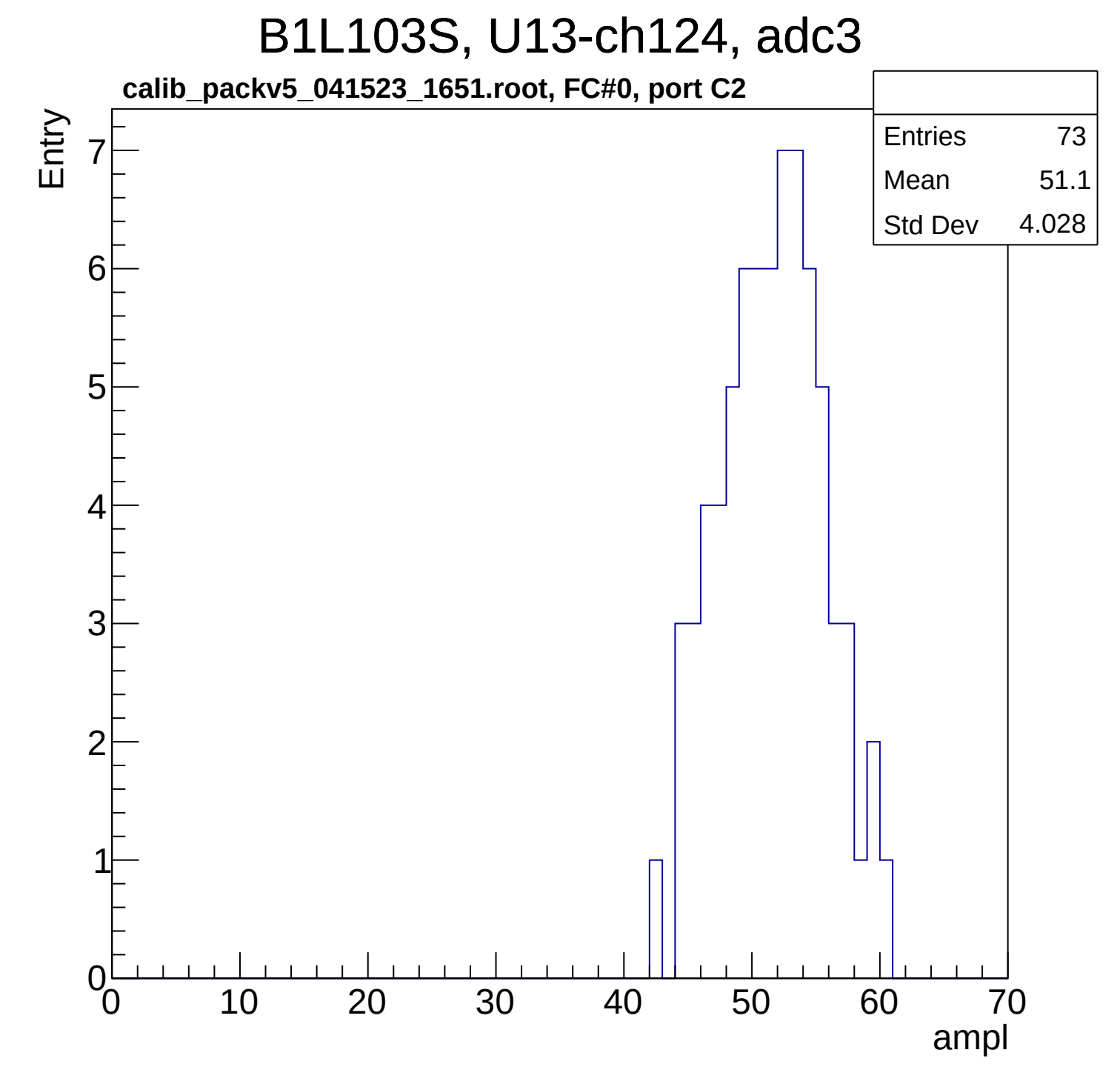
40
50
60
70


B1L103S, U13-ch124, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 51.1
Std Dev 4.028
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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40
50
60
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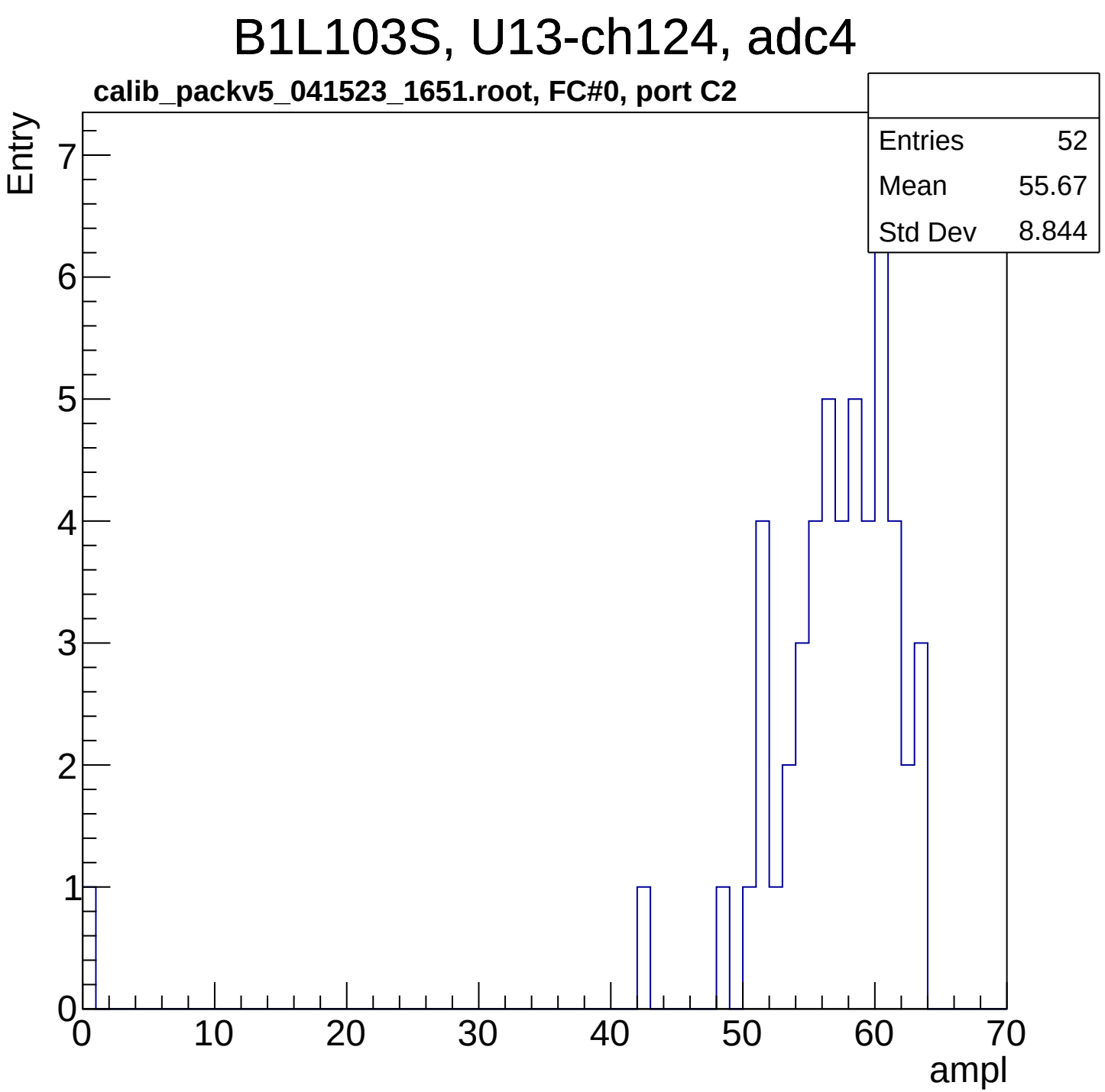
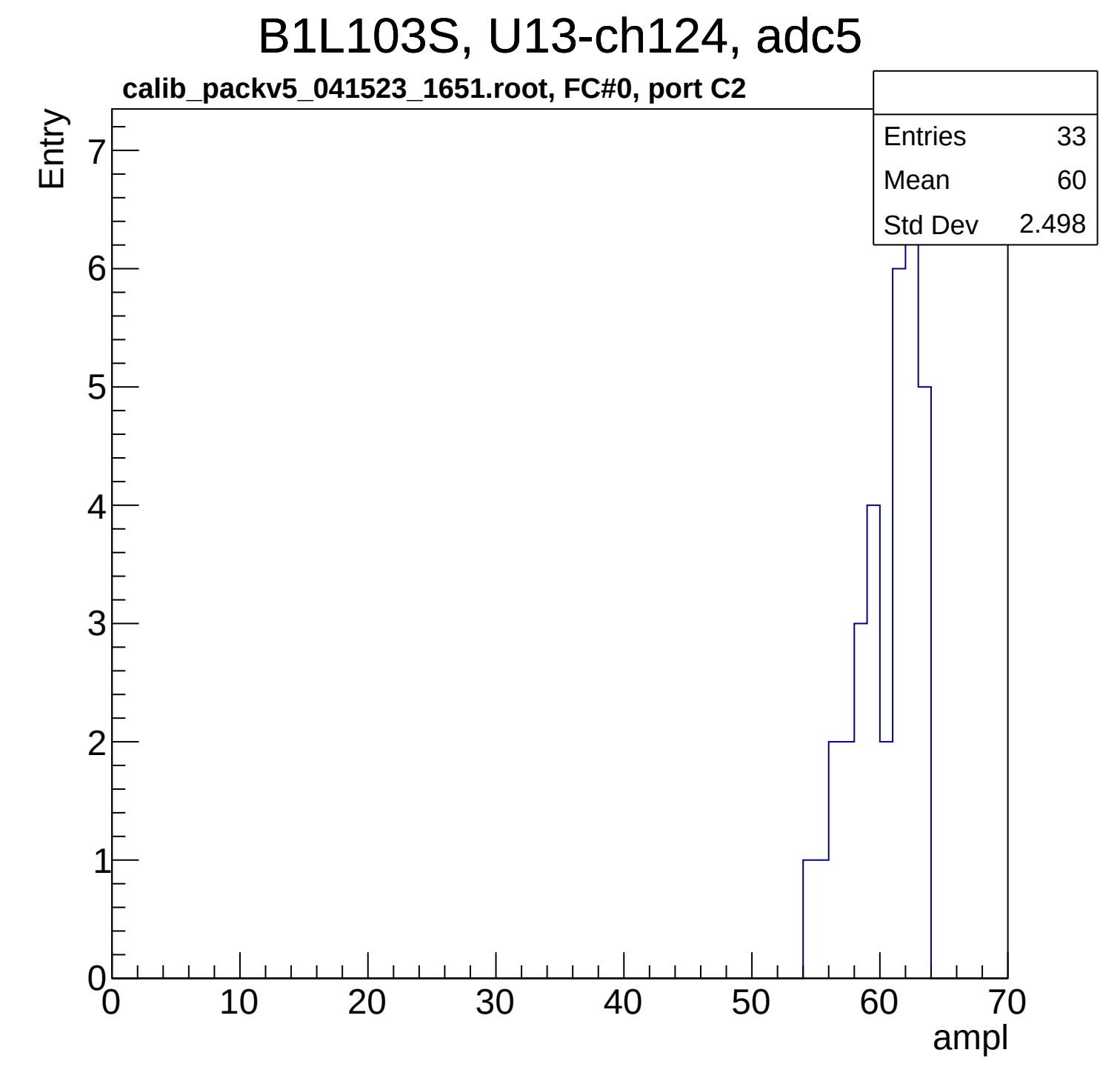

B1L103S, U13-ch124, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 55.67
Std Dev 8.844
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U13-ch124, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 60
Std Dev 2.498
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
50
60
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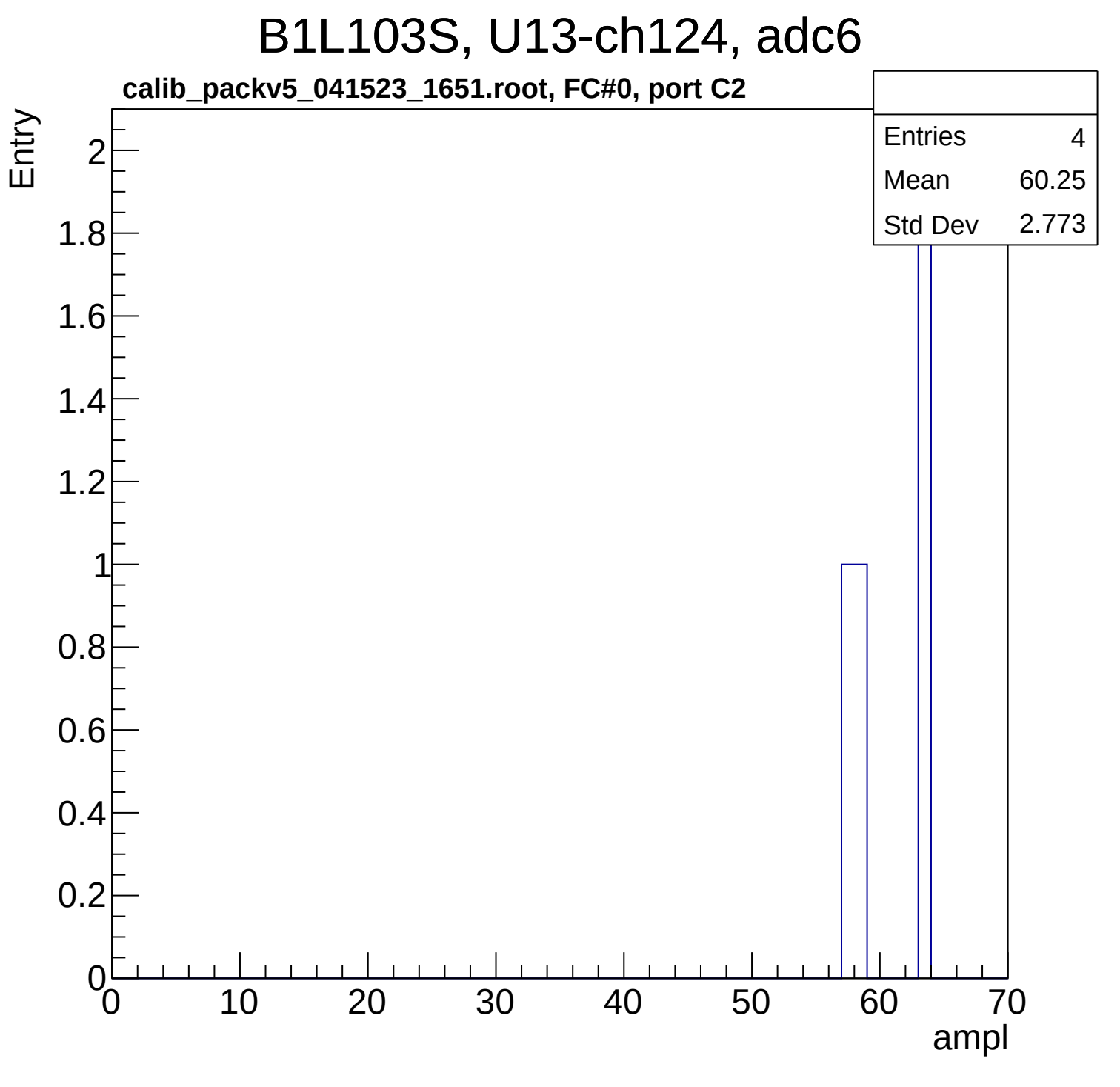
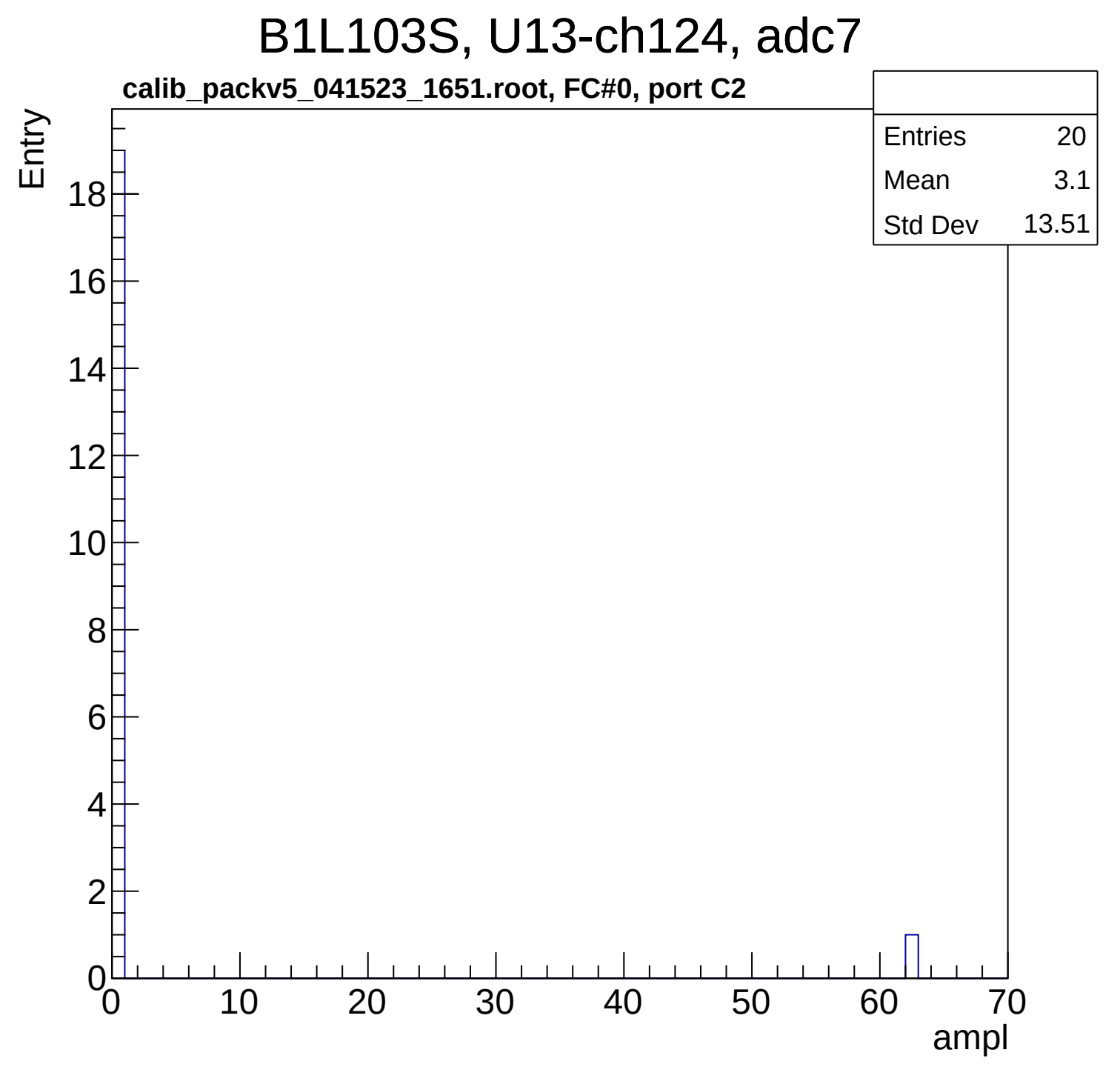
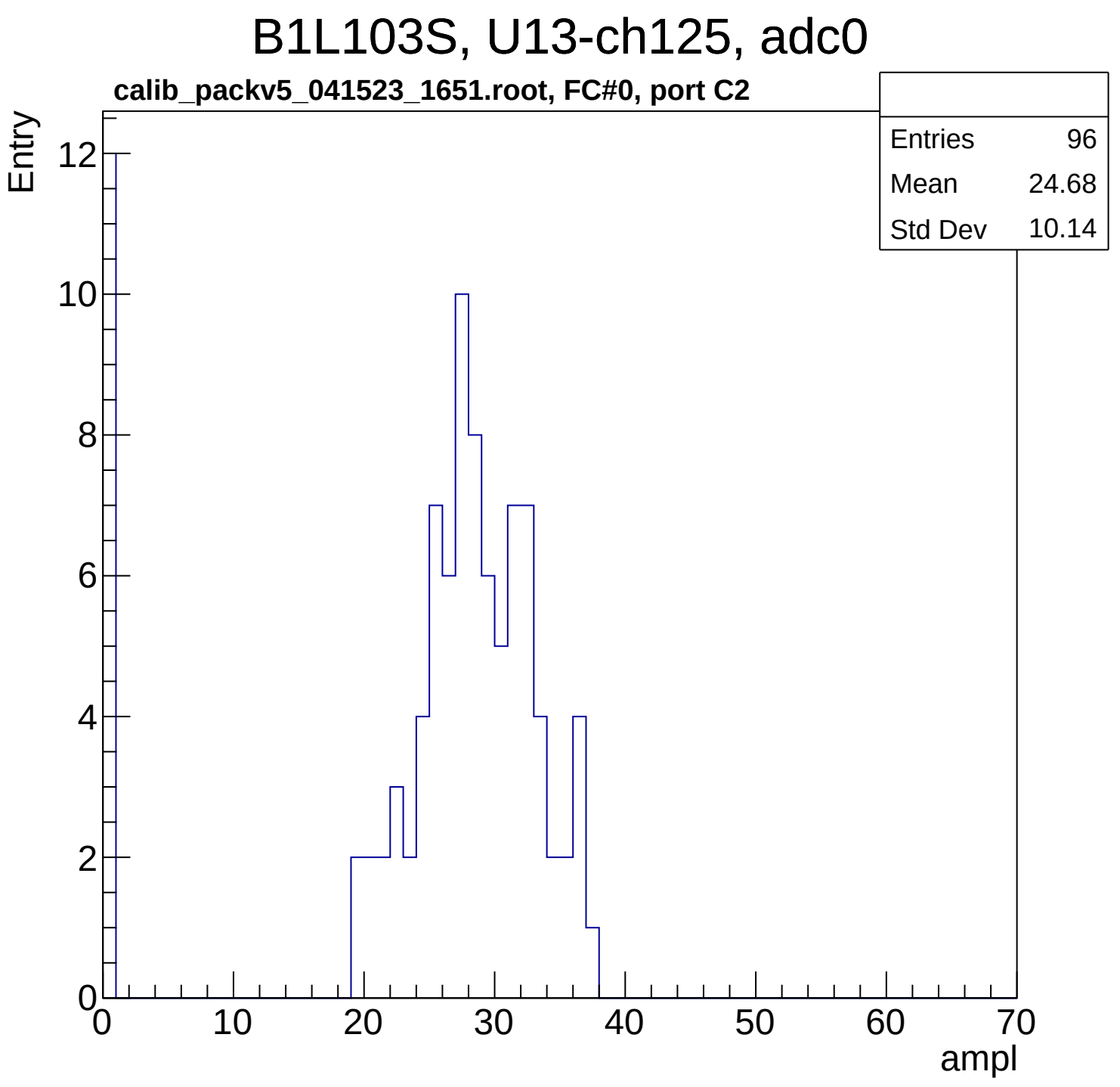
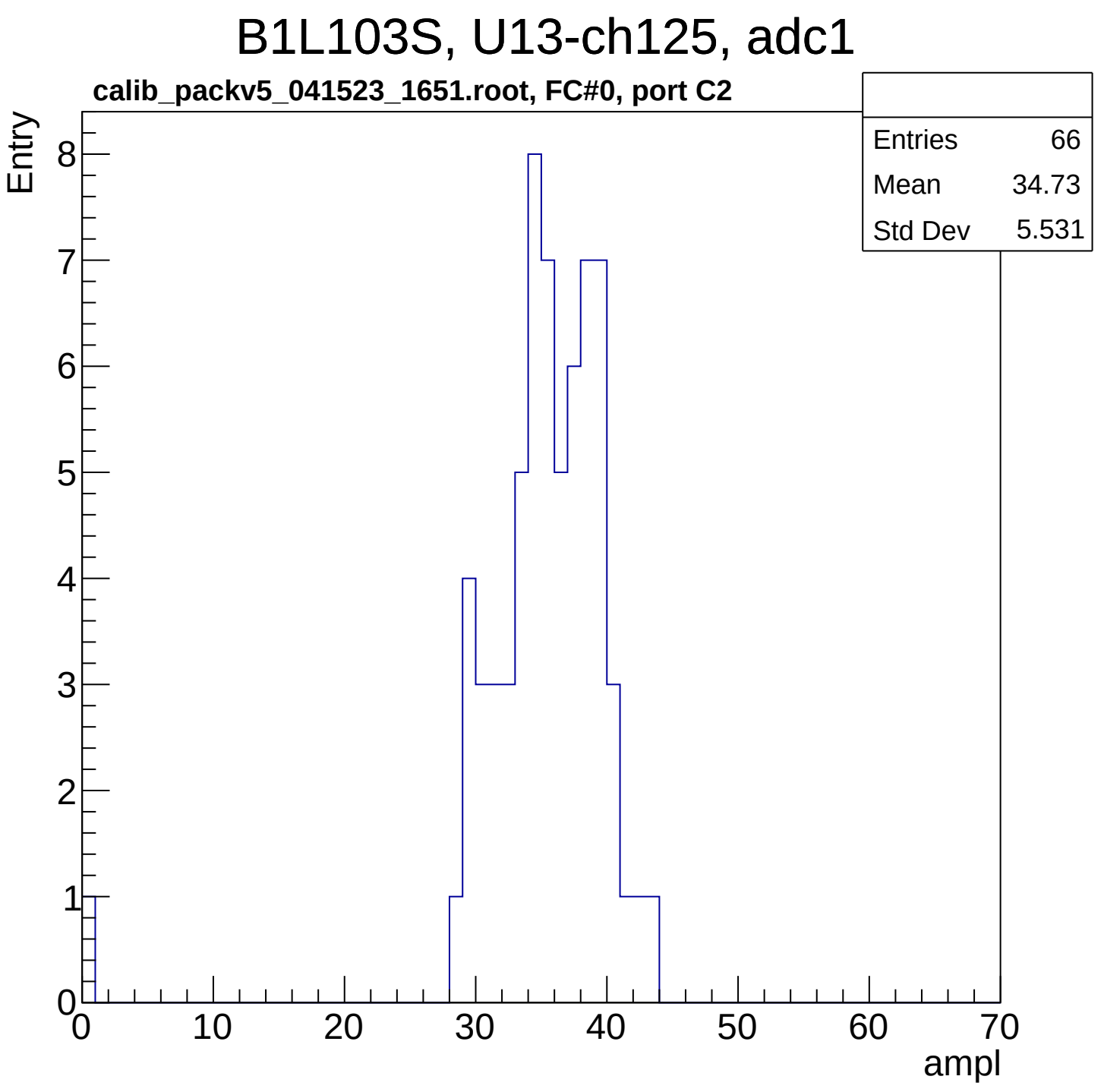
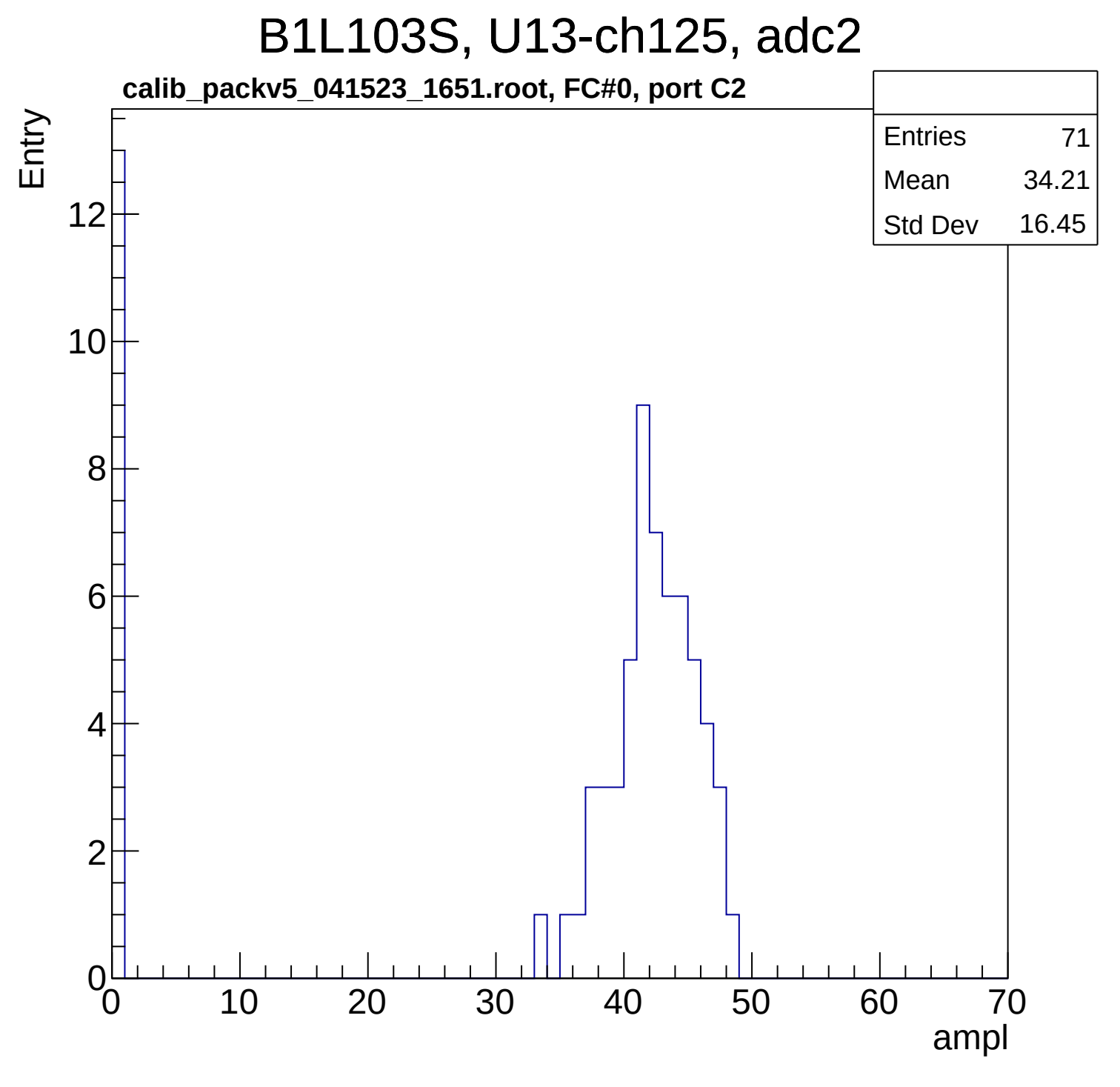
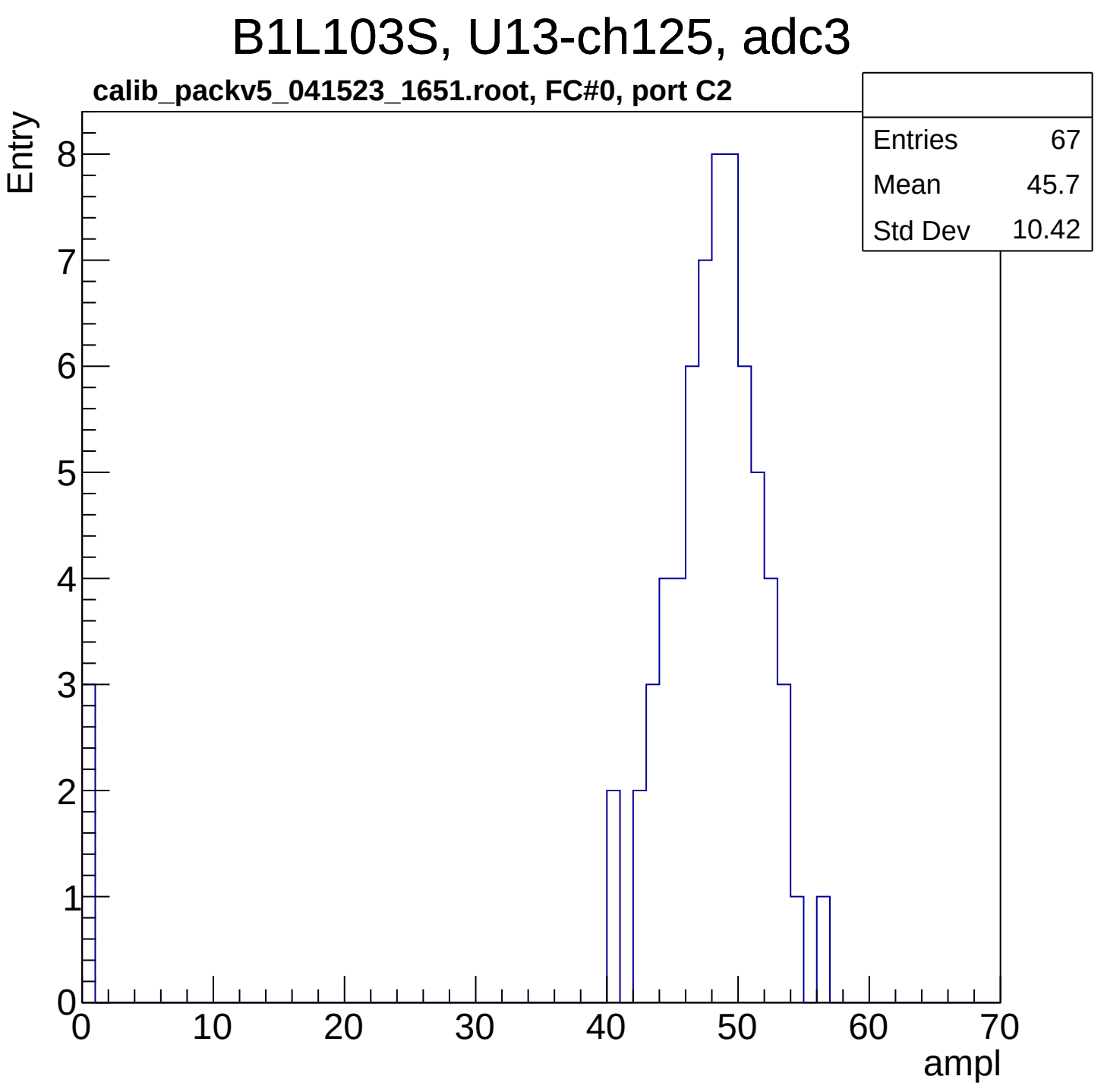

B1L103S, U13-ch124, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 60.25
Std Dev 2.773
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U13-ch124, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch125, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 24.68
Std Dev 10.14
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch125, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 34.73
Std Dev 5.531
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch125, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 34.21
Std Dev 16.45
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch125, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 45.7
Std Dev 10.42
Entry
ampl
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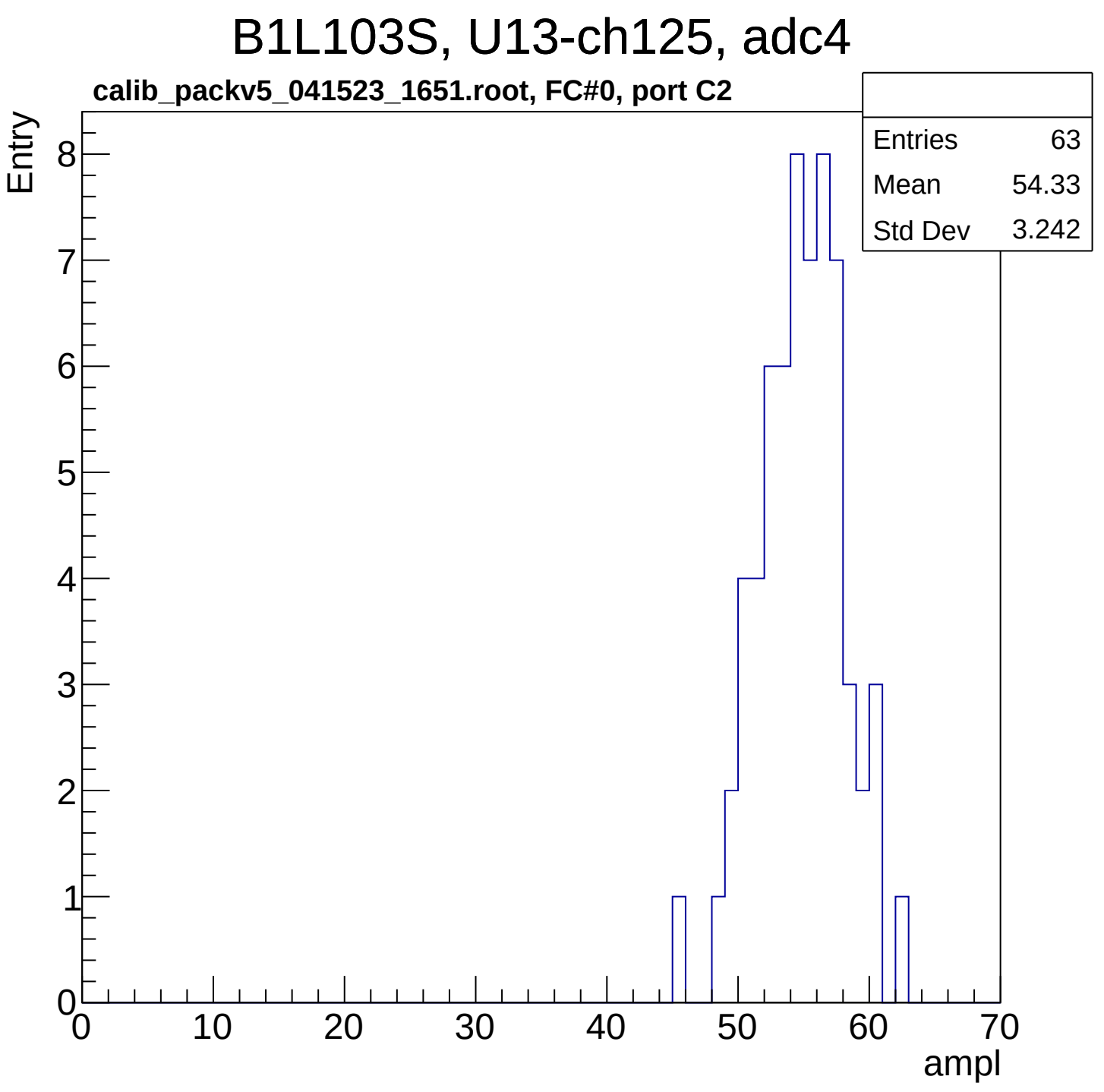
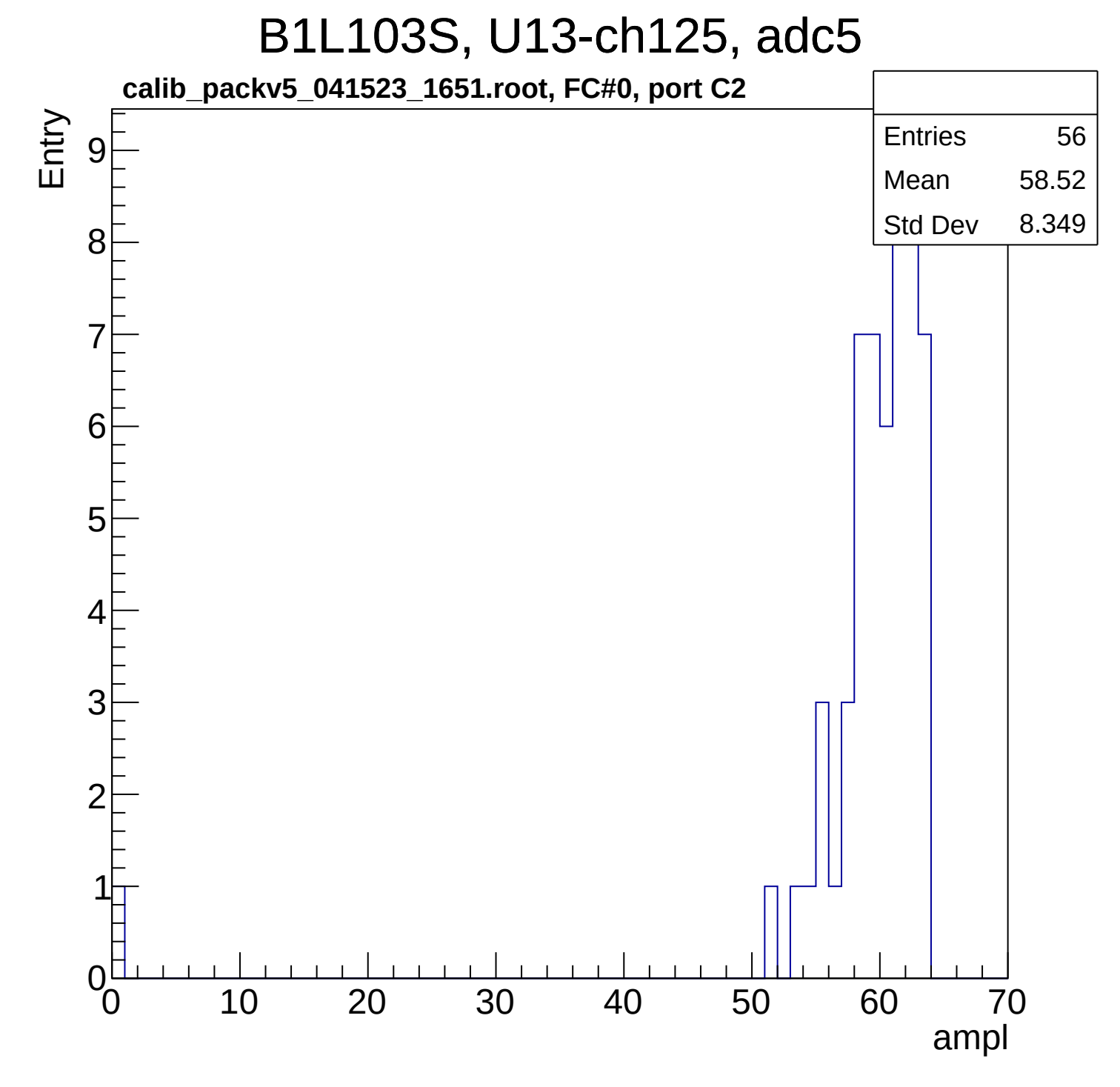
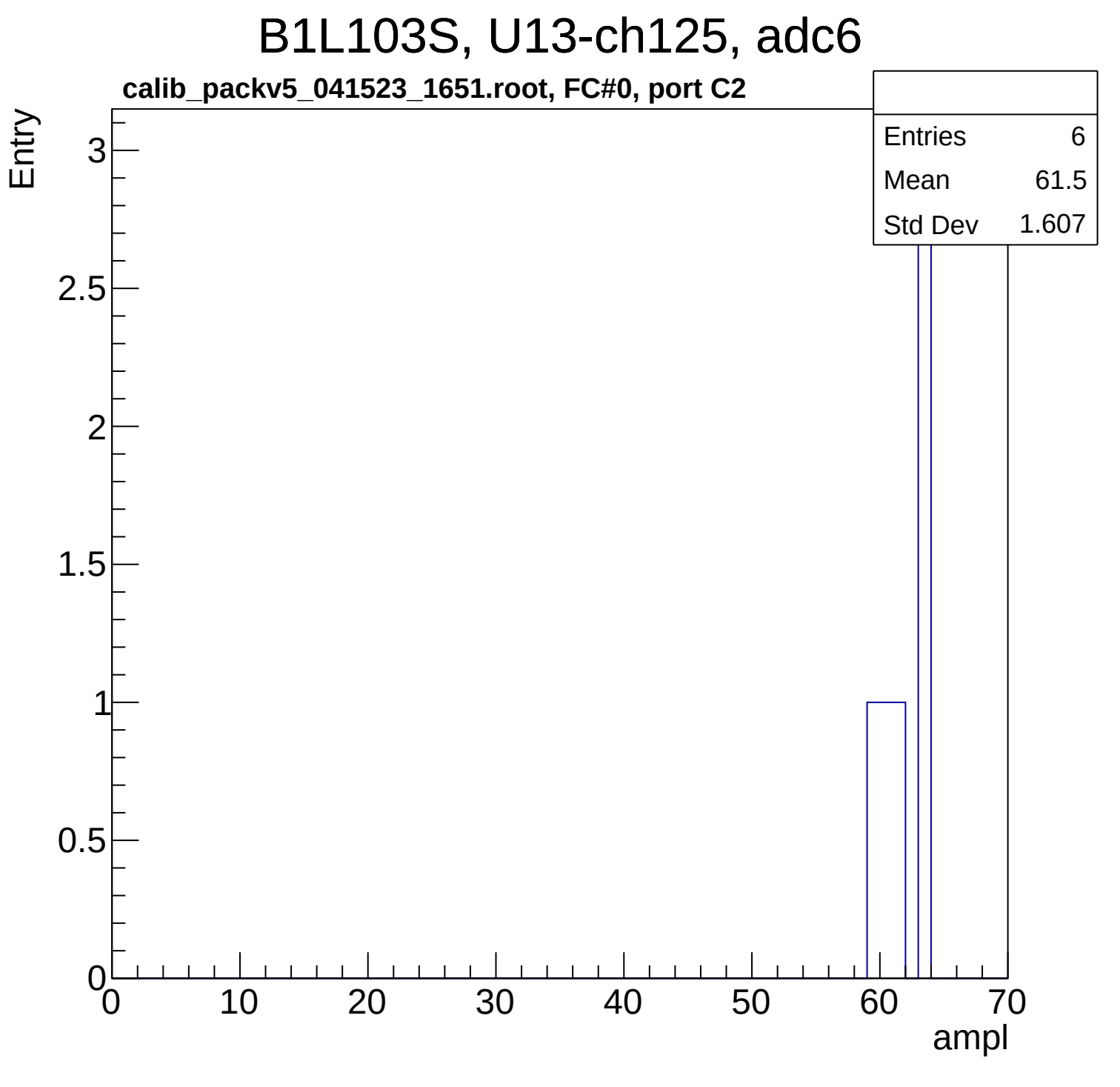
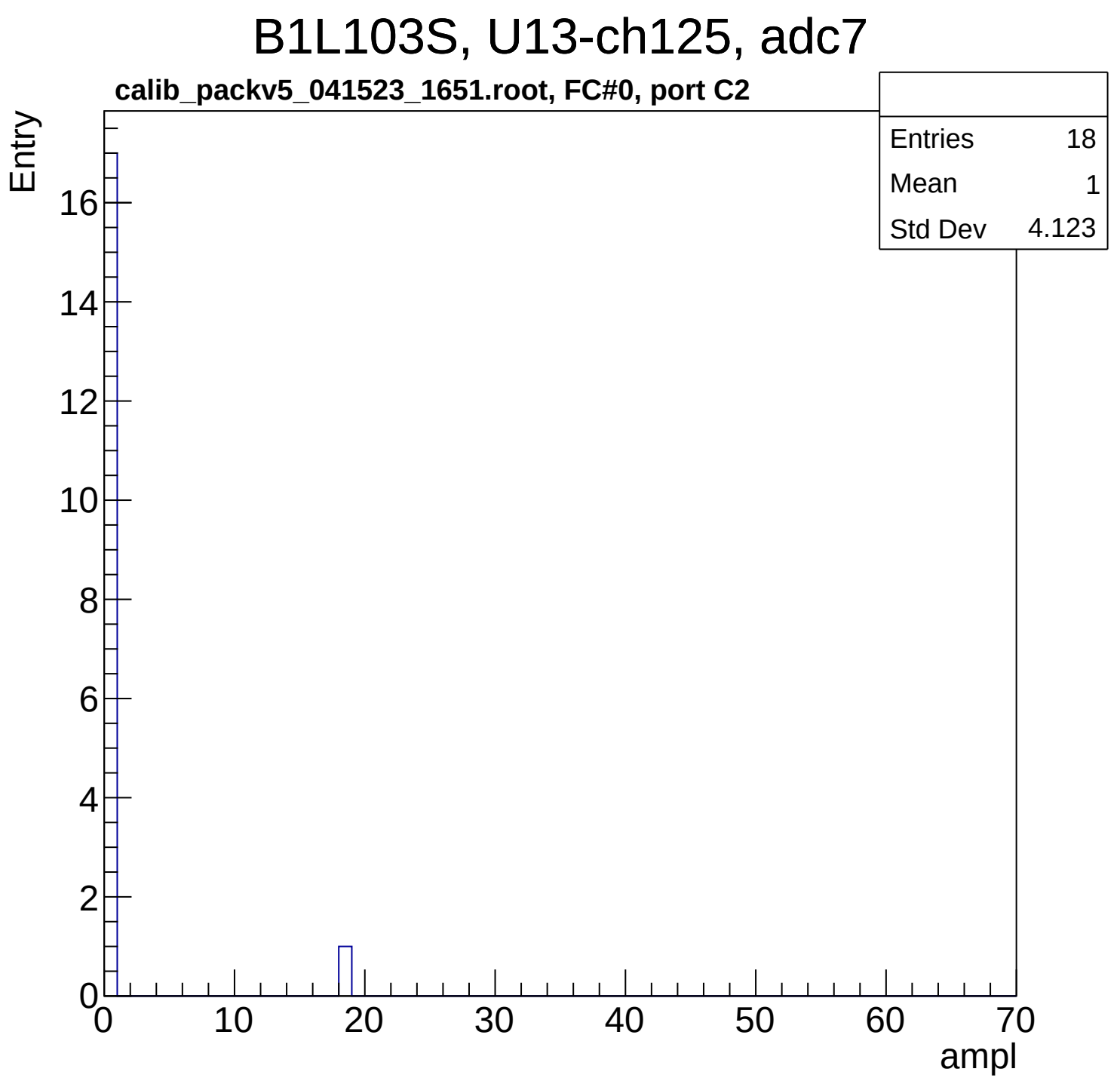
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch125, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 54.33
Std Dev 3.242
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch125, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.52
Std Dev 8.349
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch125, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.5
Std Dev 1.607
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U13-ch125, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1
Std Dev 4.123
Entry
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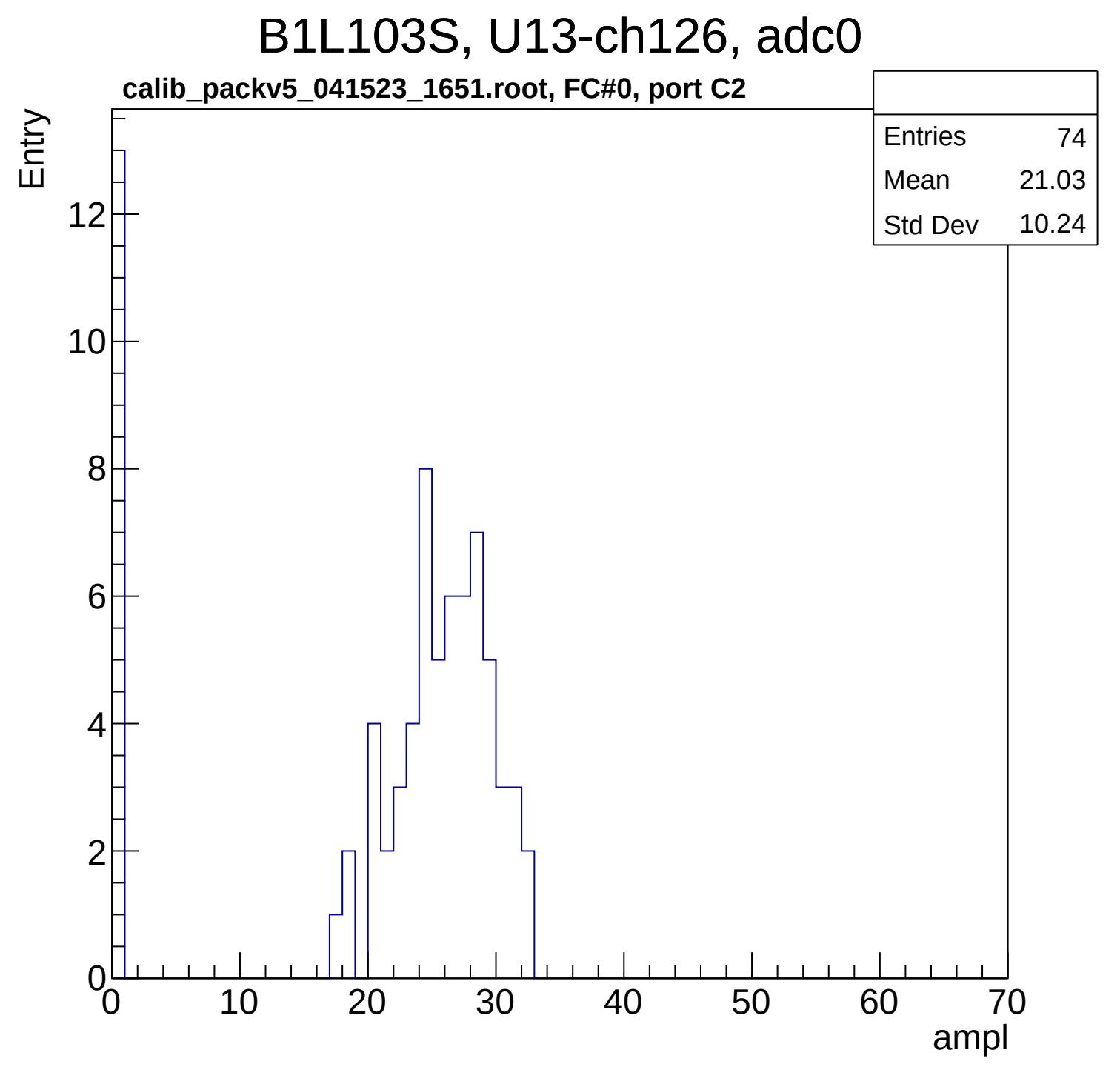
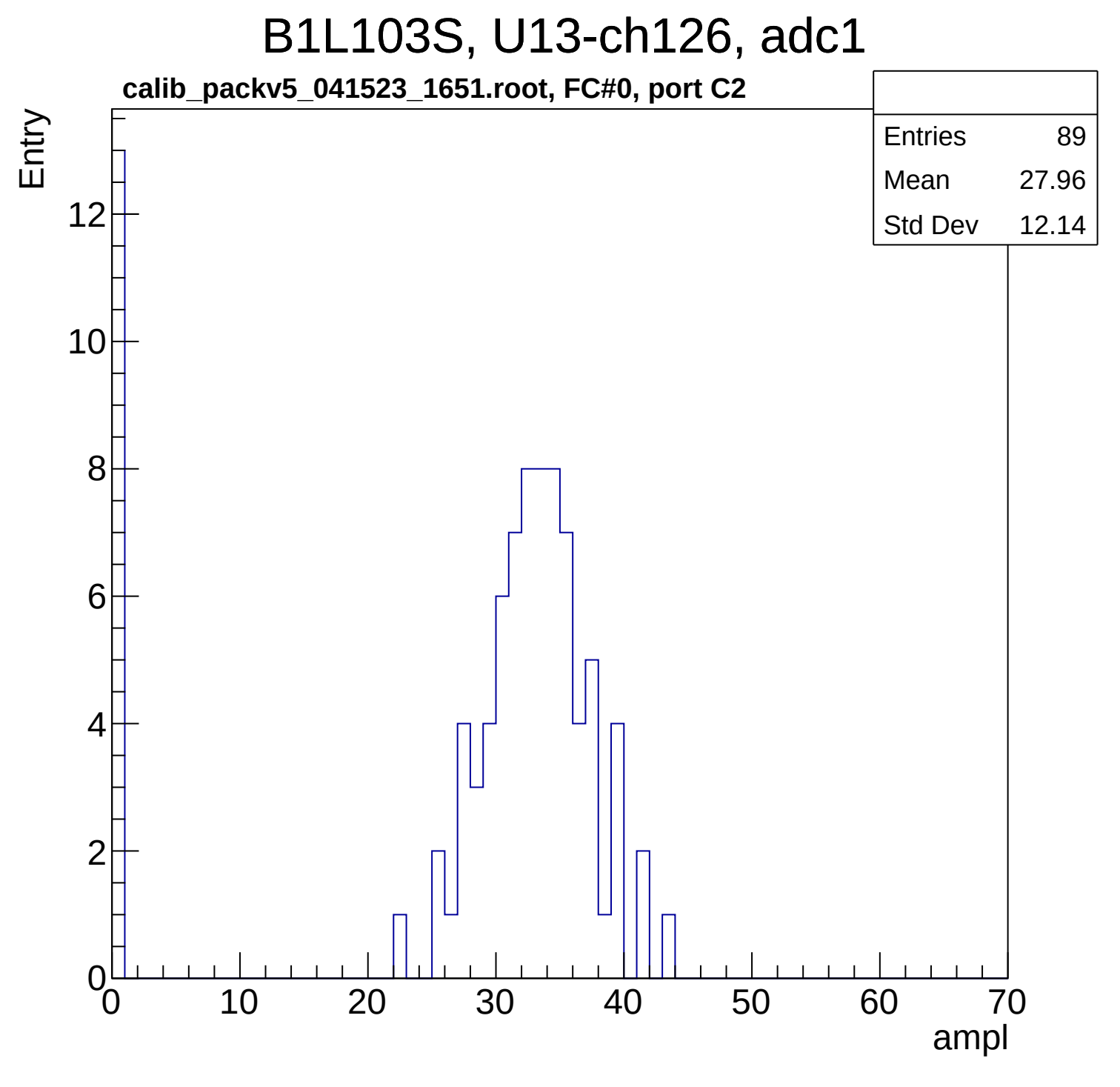
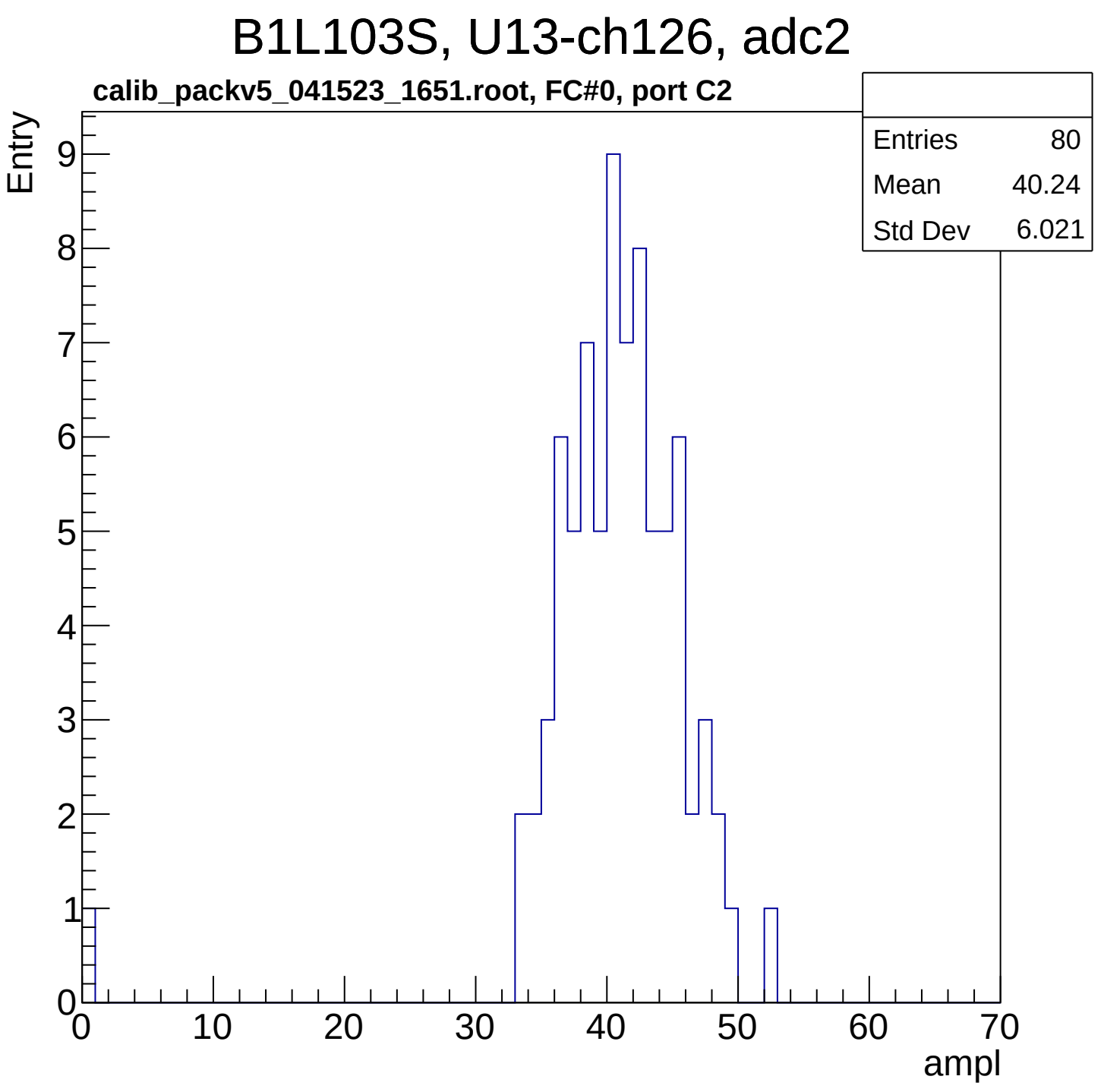
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch126, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 21.03
Std Dev 10.24
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch126, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 27.96
Std Dev 12.14
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch126, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 40.24
Std Dev 6.021
Entry
ampl
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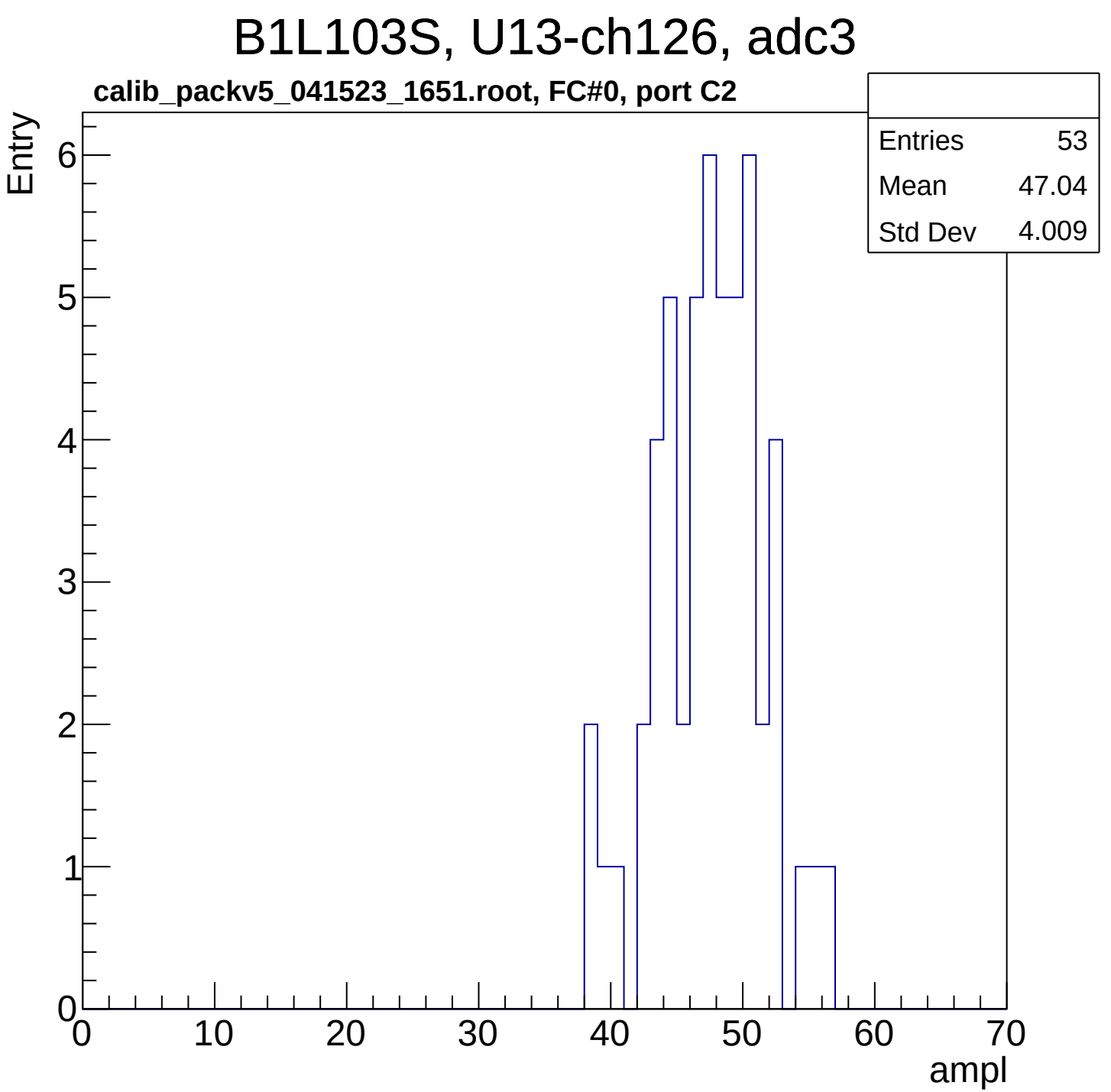
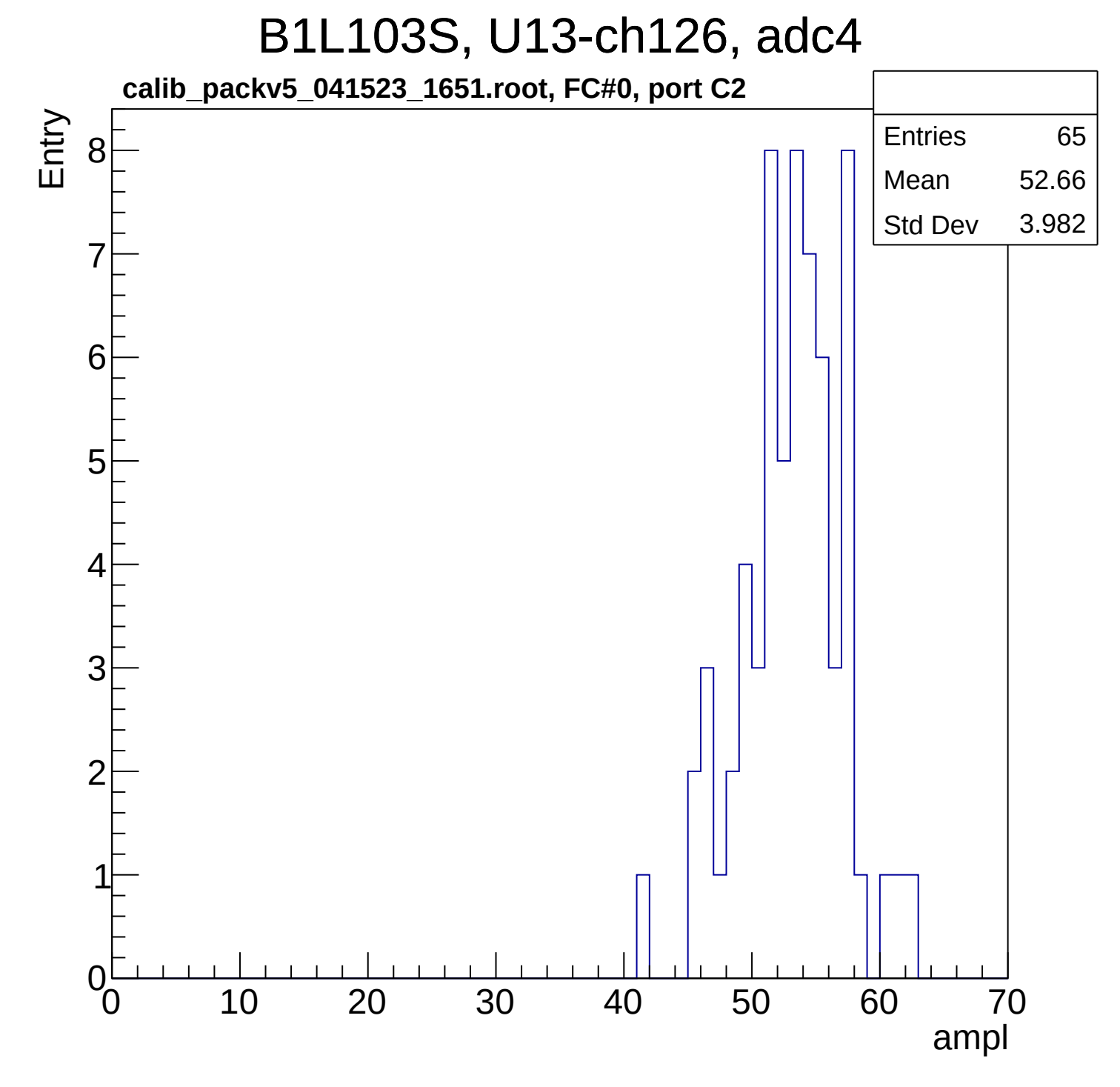
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch126, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 47.04
Std Dev 4.009
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch126, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 52.66
Std Dev 3.982
Entry
ampl
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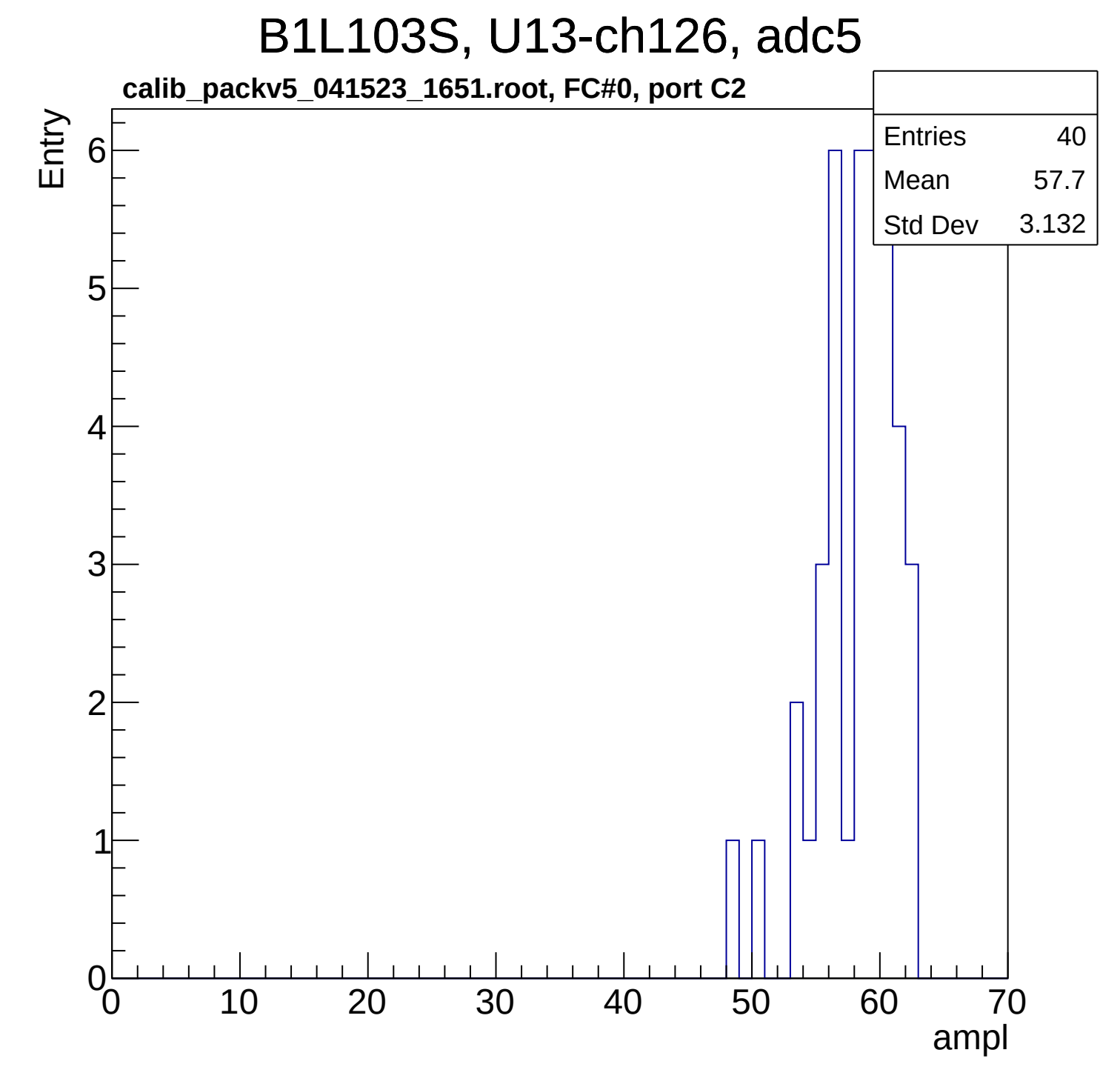
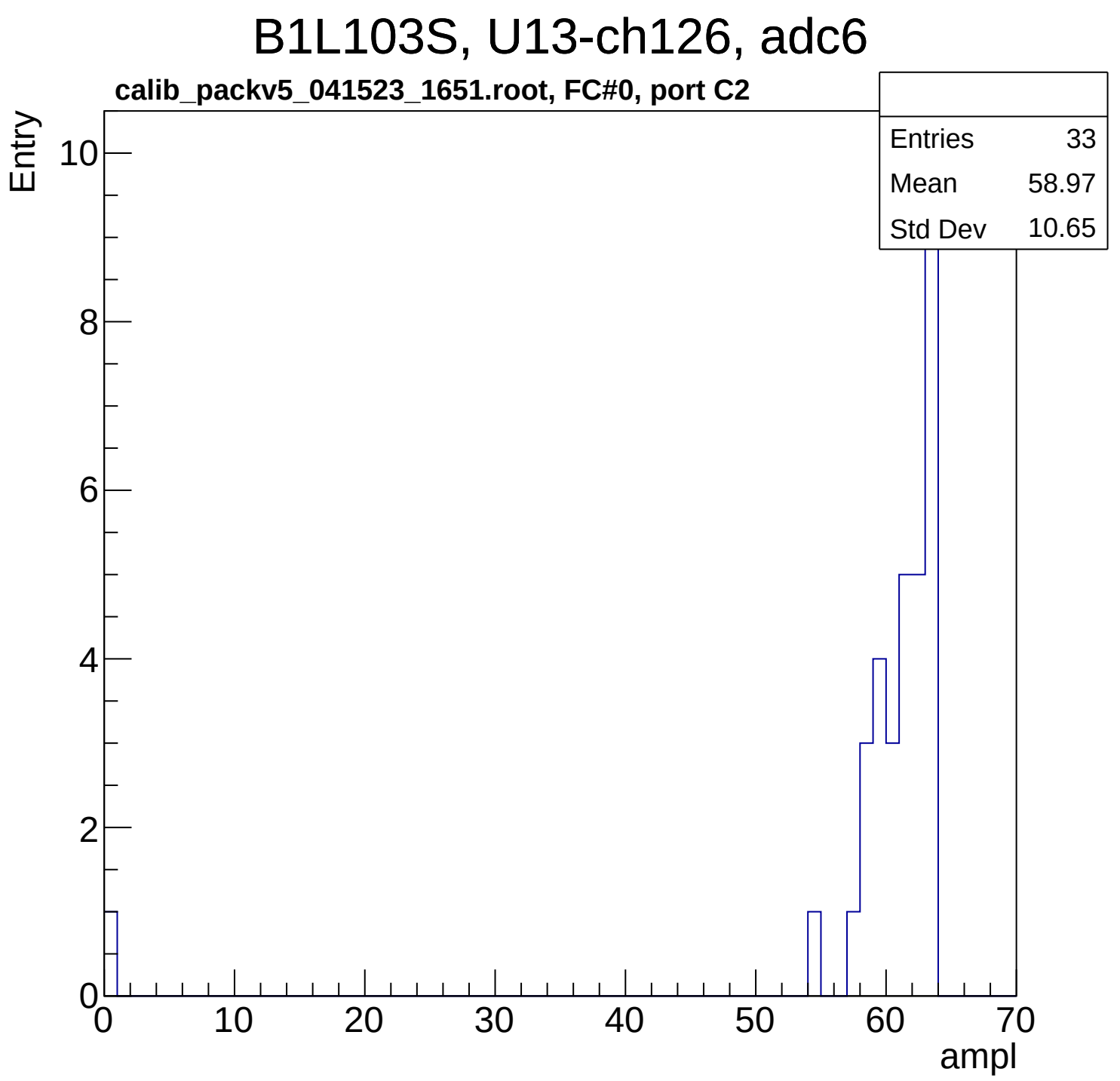
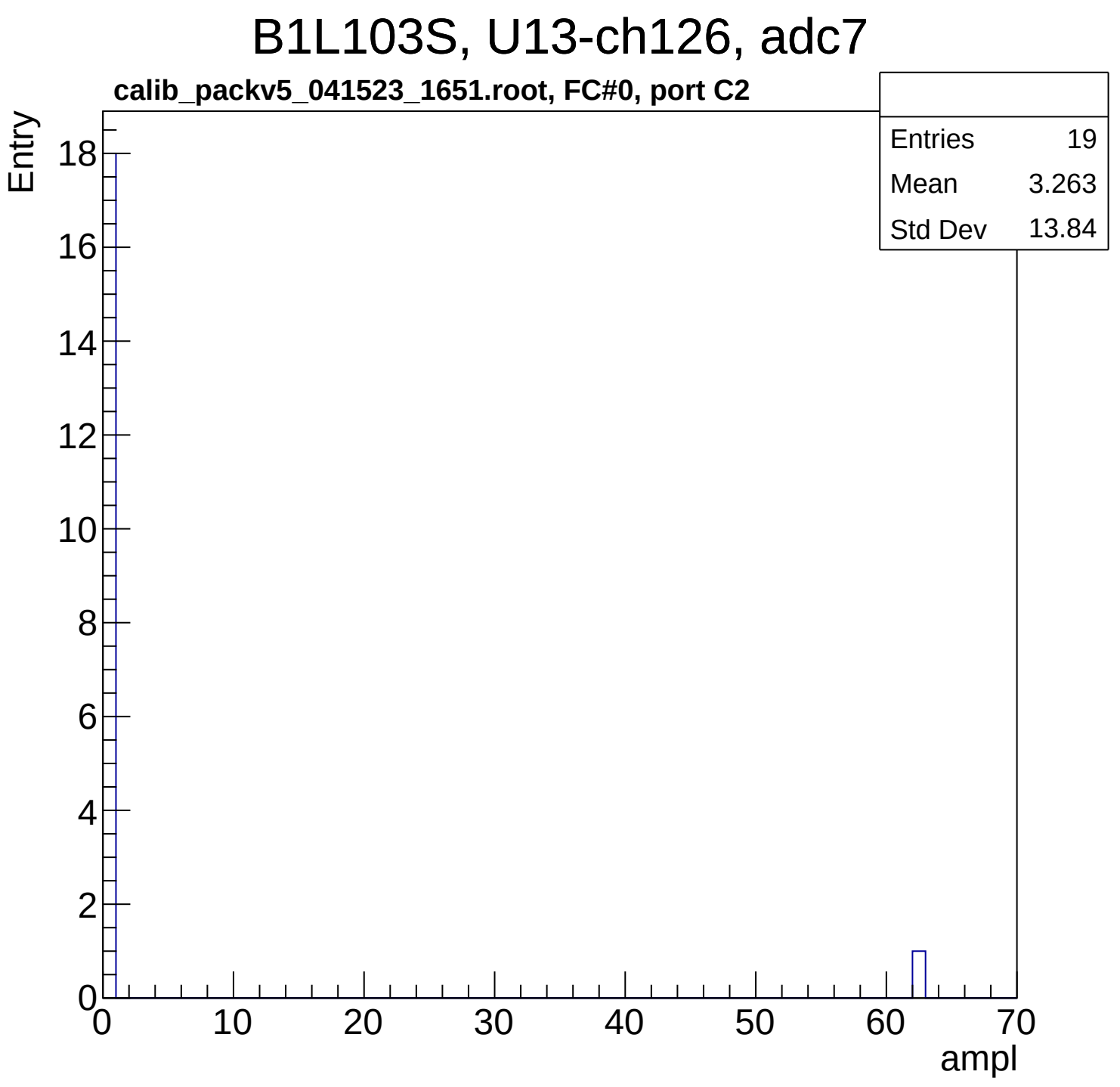
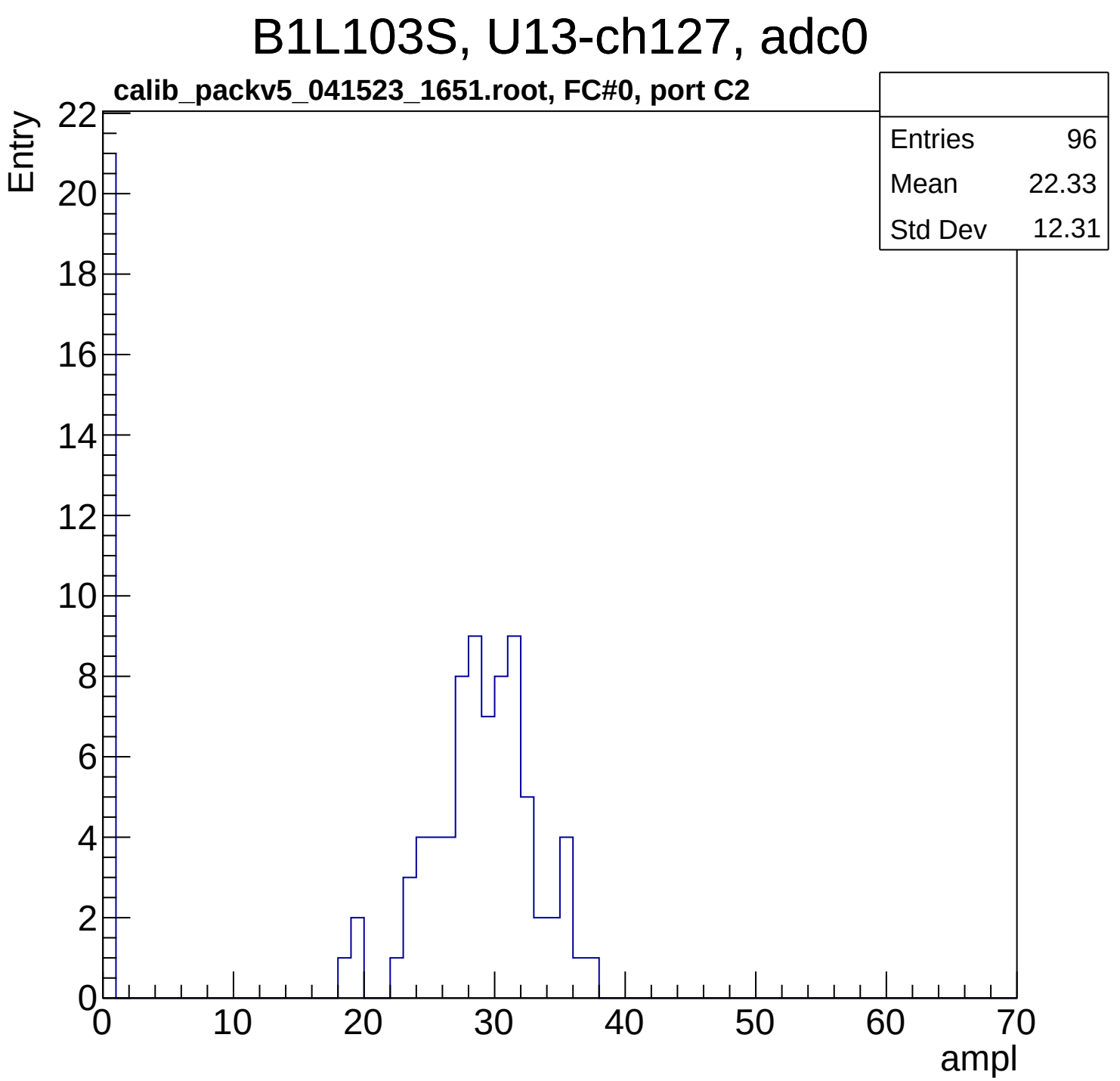
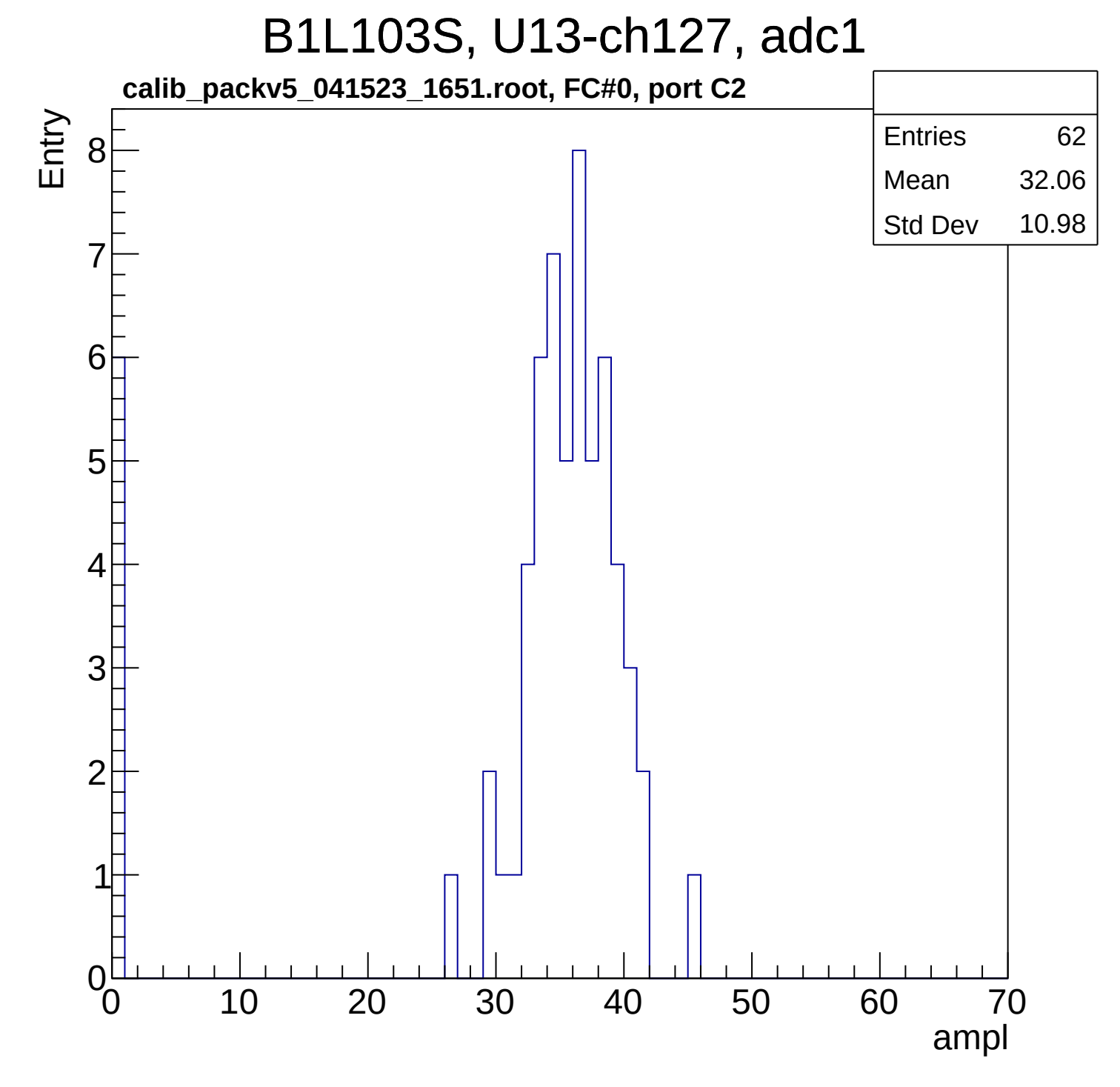
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch126, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 57.7
Std Dev 3.132
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U13-ch126, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 58.97
Std Dev 10.65
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch126, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.263
Std Dev 13.84
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch127, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 22.33
Std Dev 12.31
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U13-ch127, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 32.06
Std Dev 10.98
Entry
ampl
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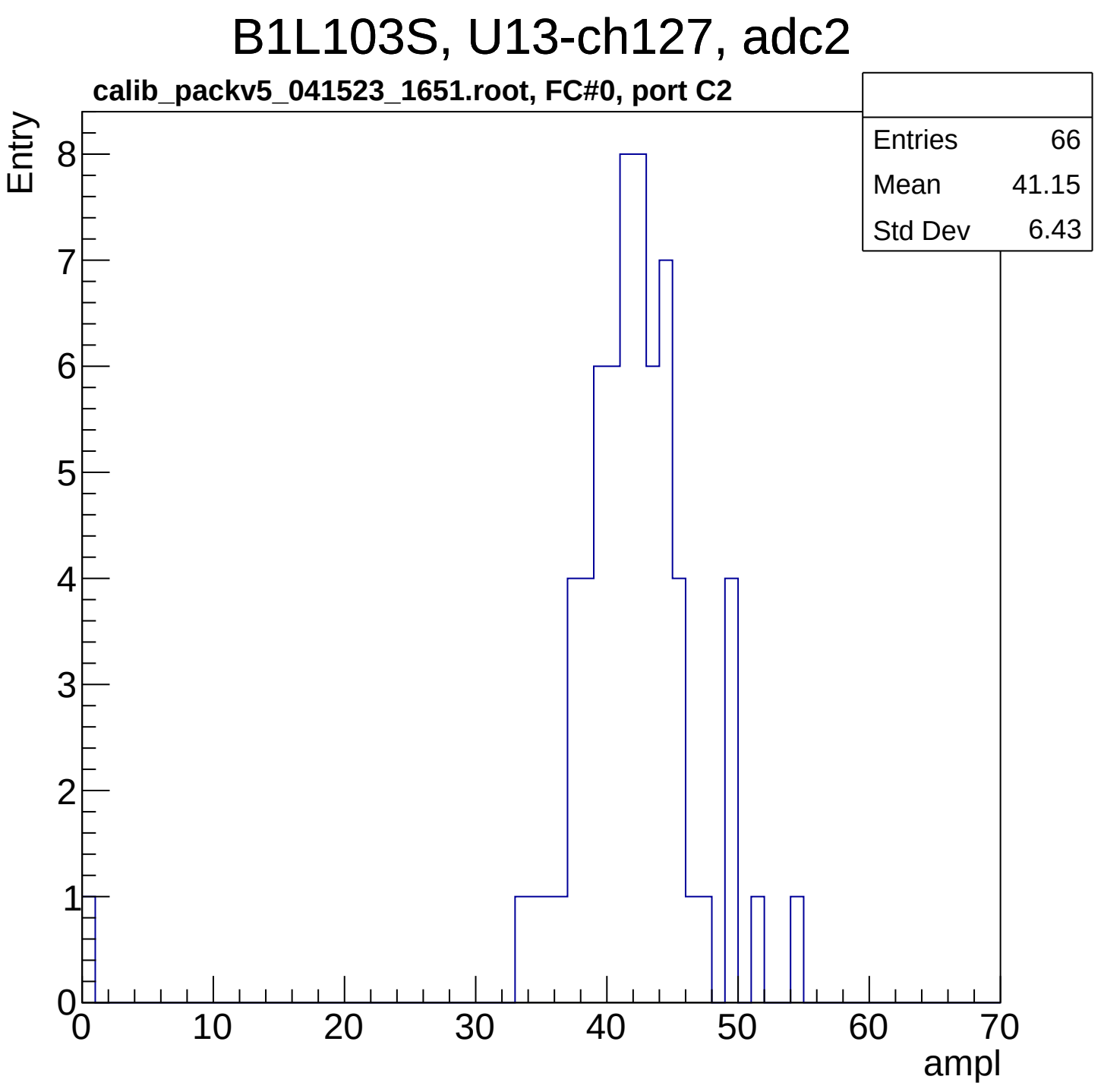
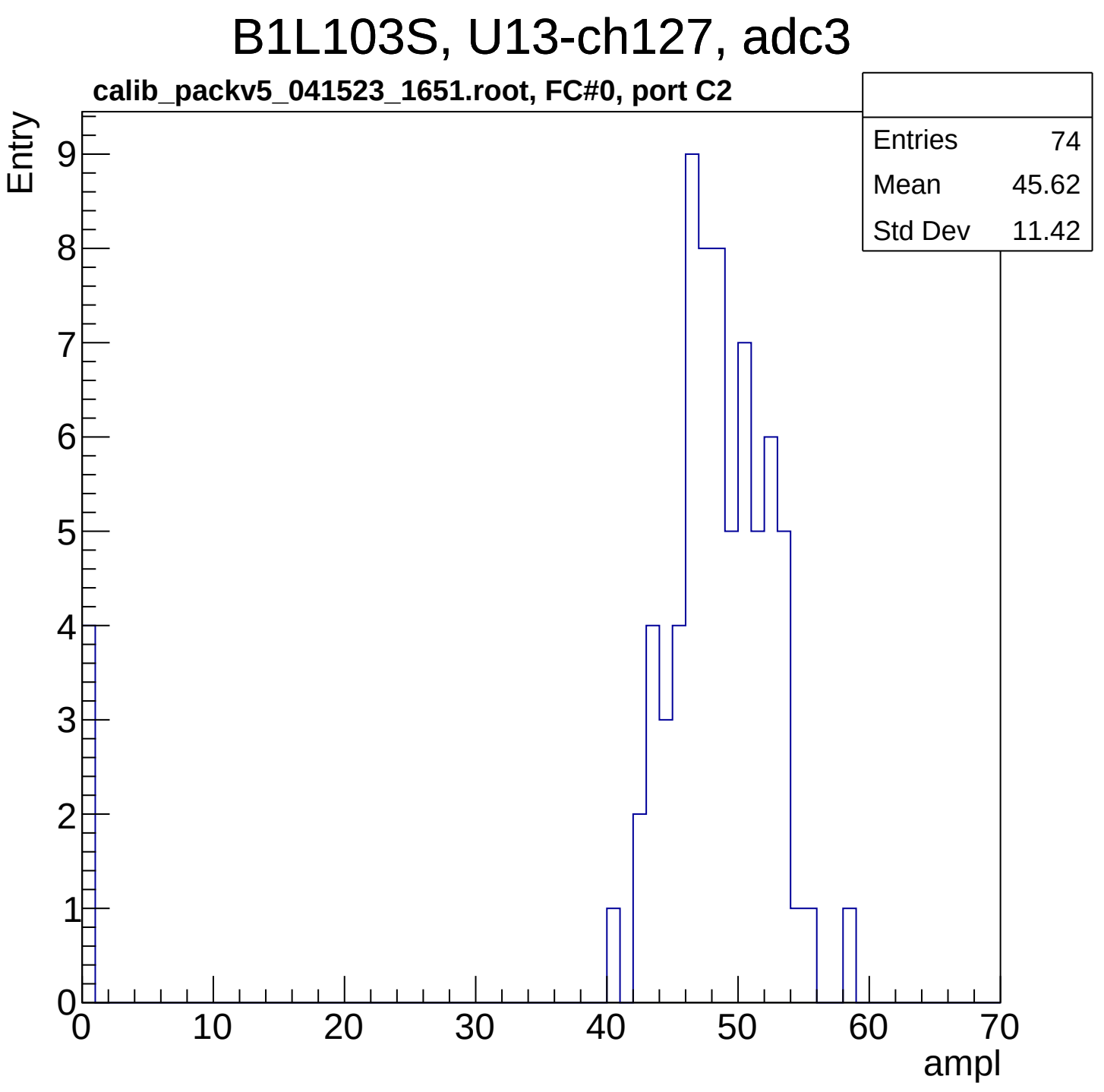
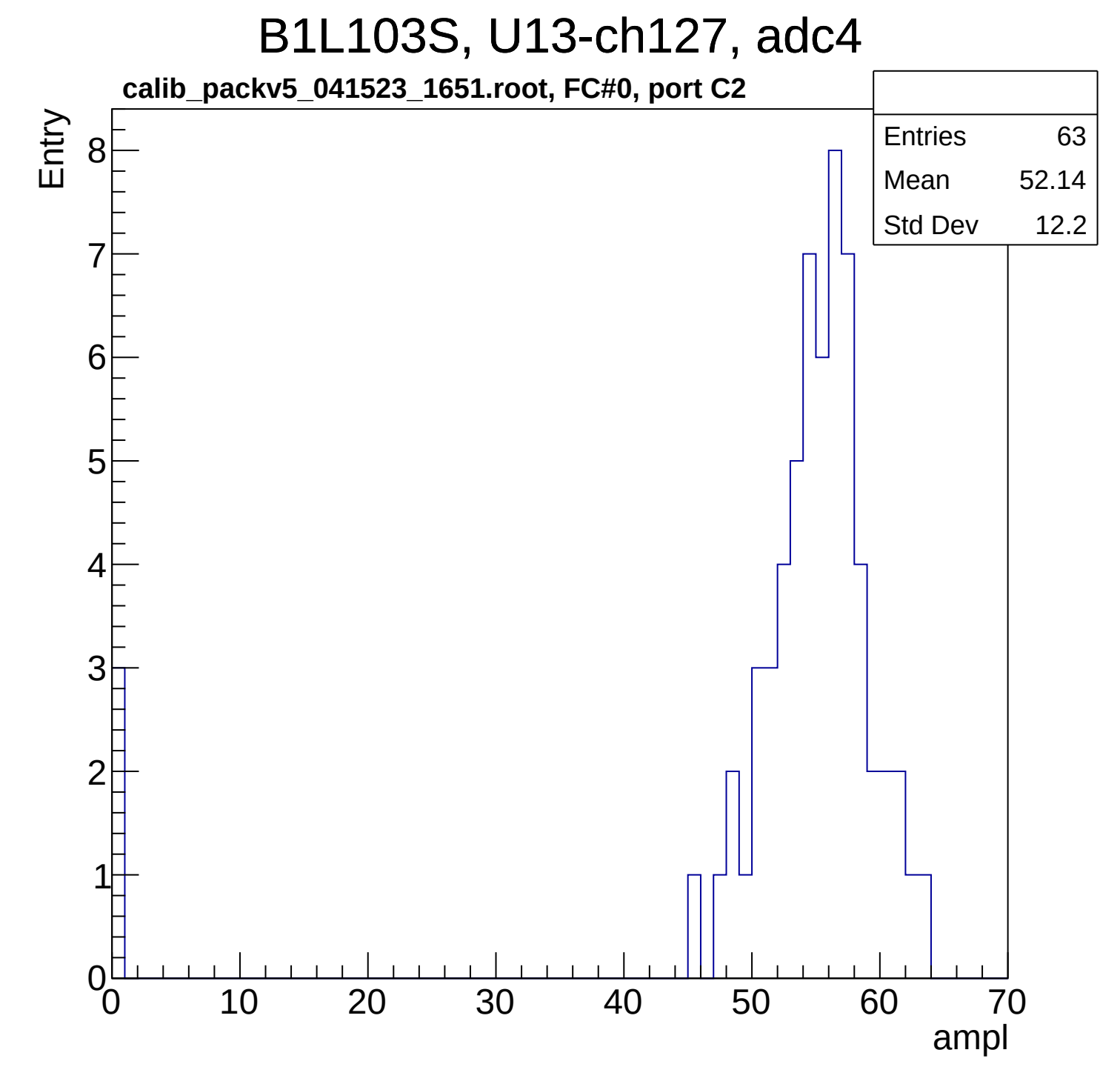
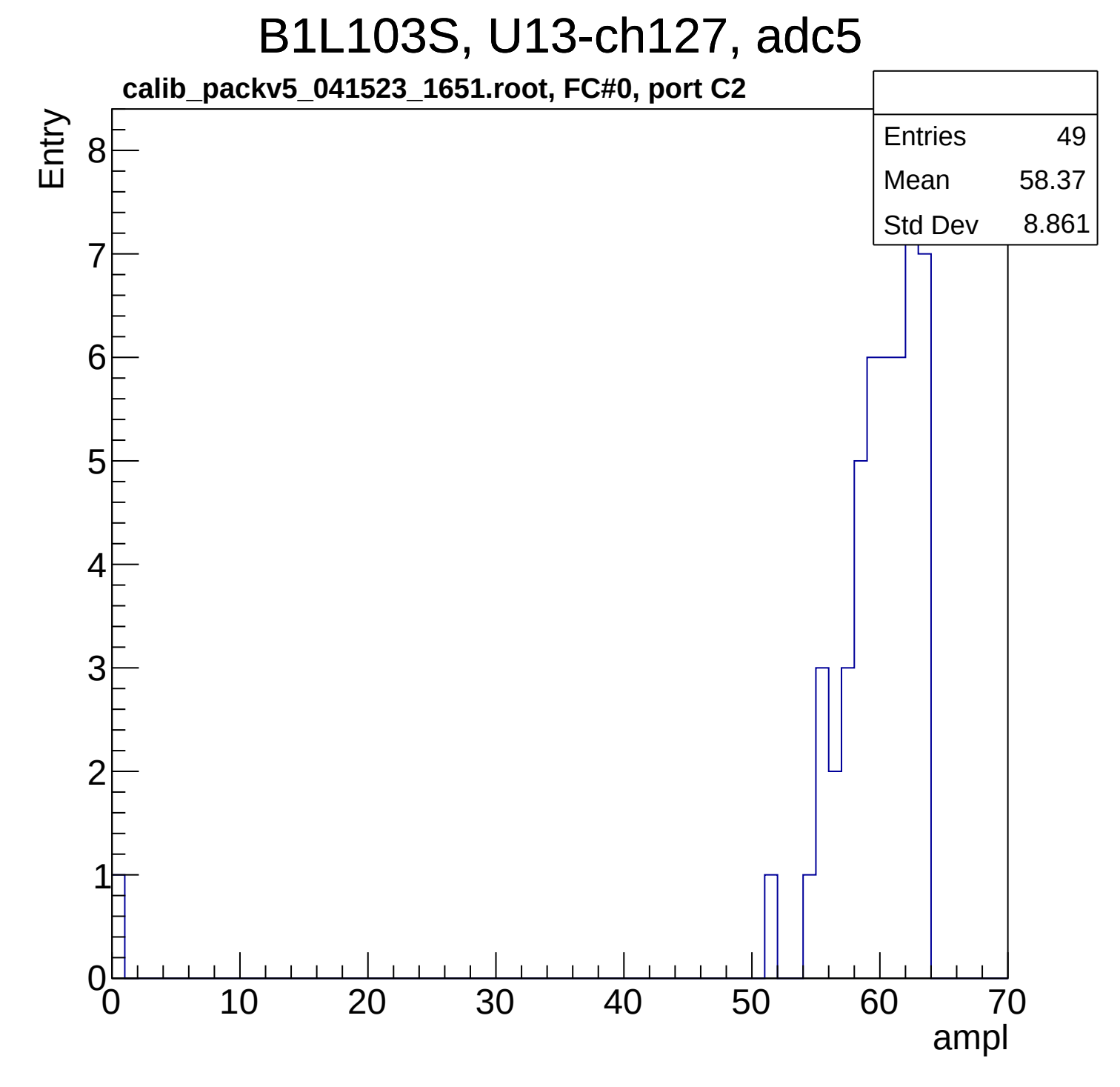
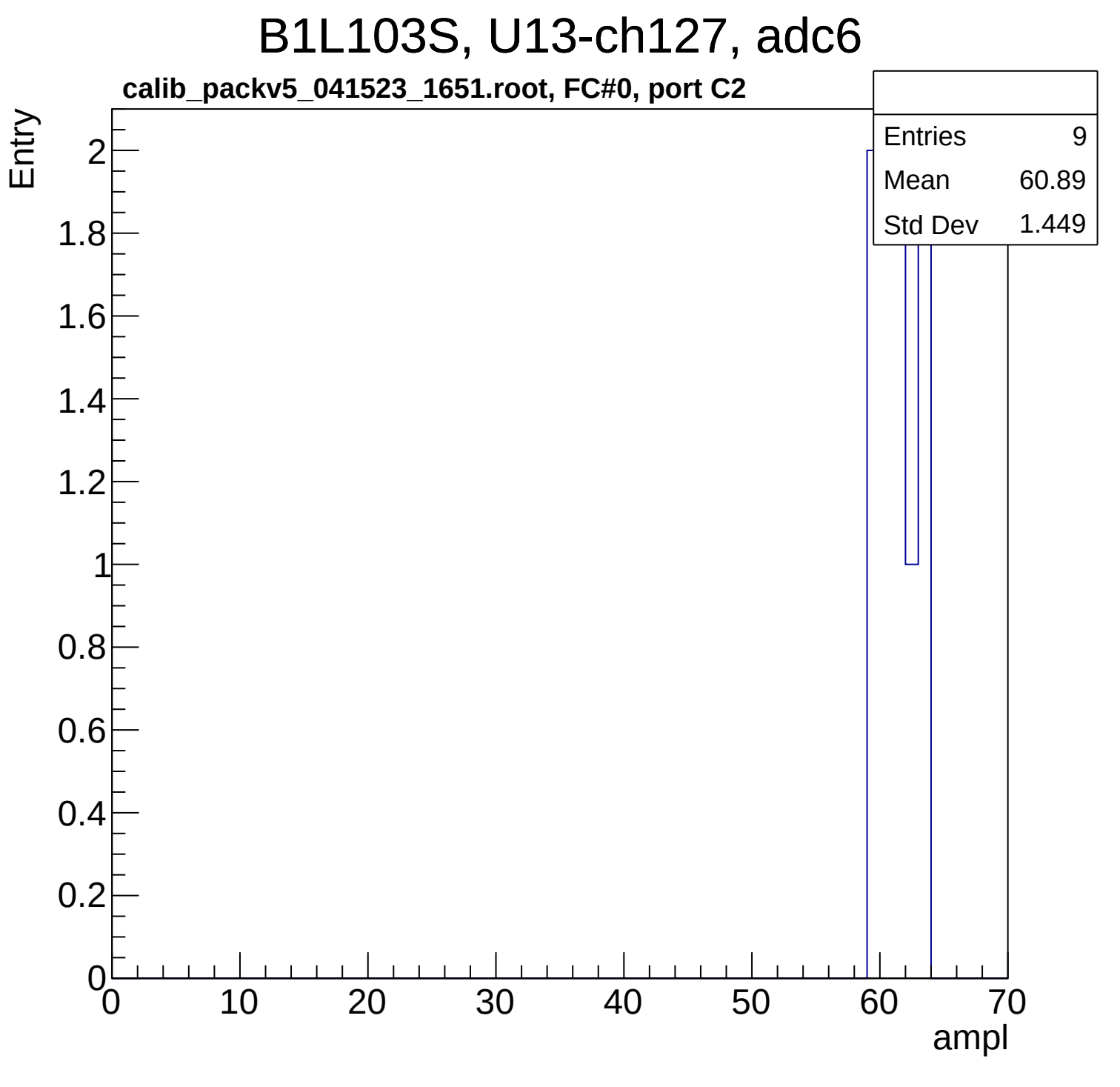
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

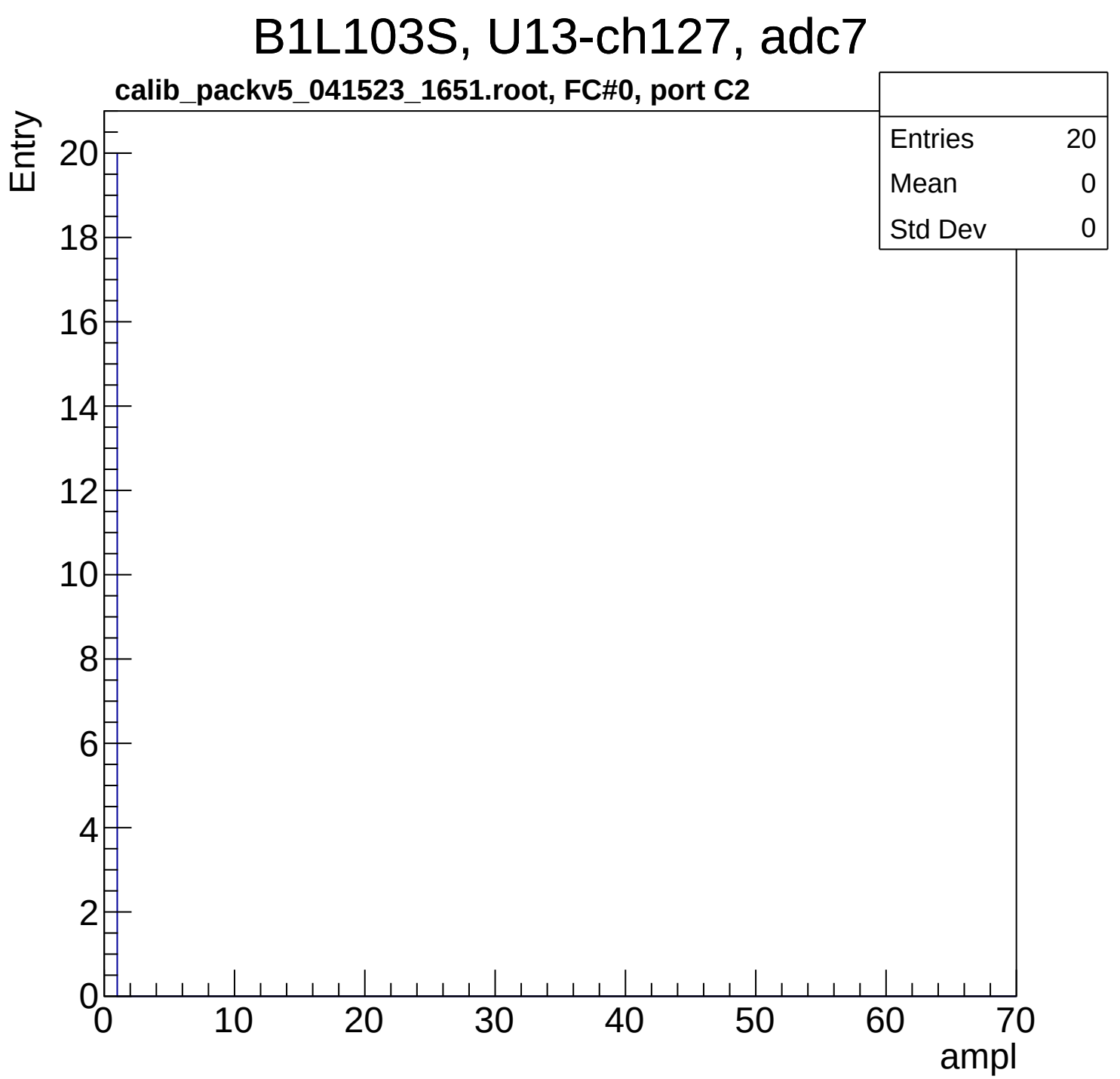

B1L103S, U13-ch127, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 41.15
Std Dev 6.43
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

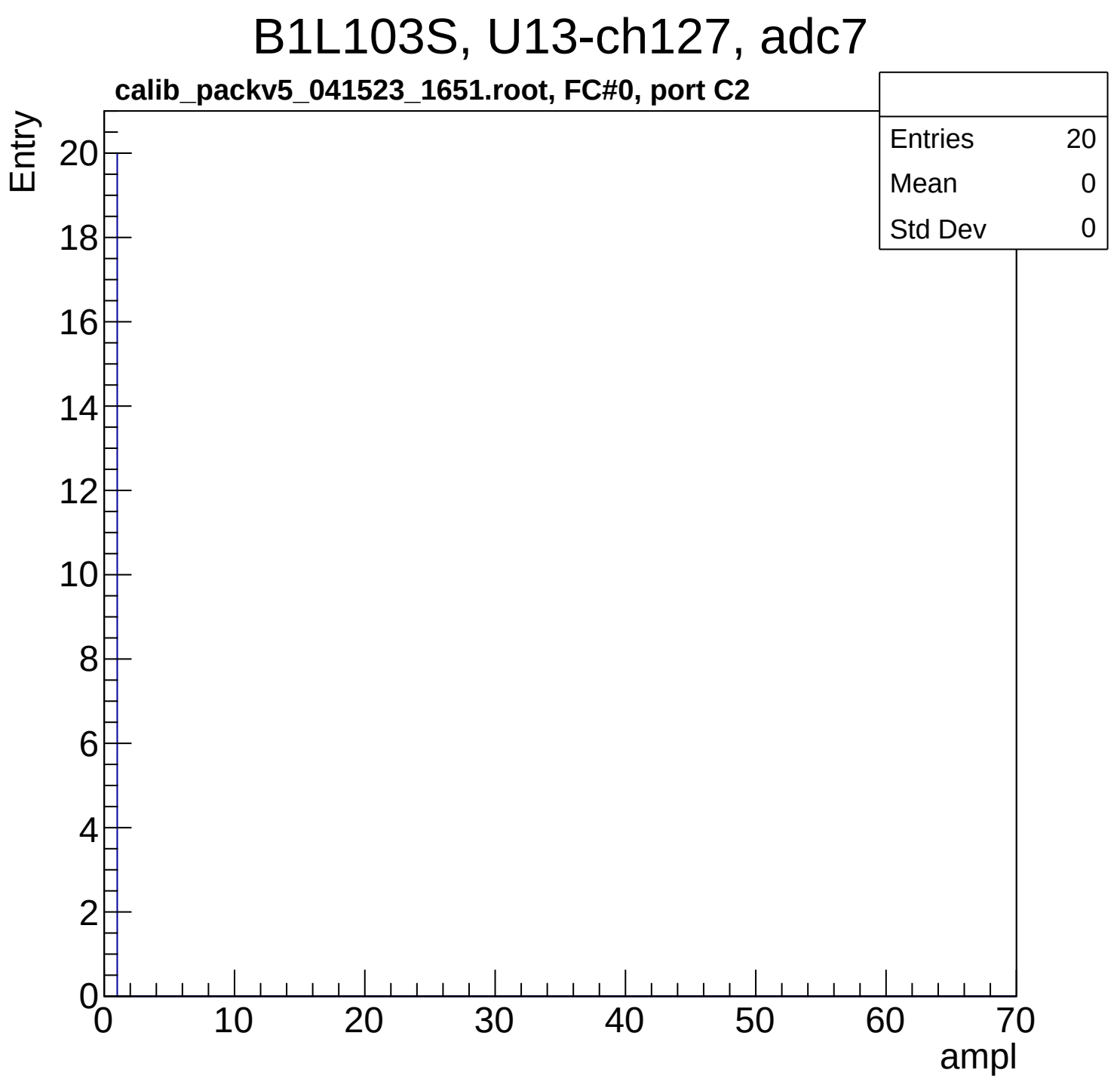

B1L103S, U13-ch127, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 45.62
Std Dev 11.42
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U13-ch127, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 52.14
Std Dev 12.2
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch127, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.37
Std Dev 8.861
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U13-ch127, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 60.89
Std Dev 1.449
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U13-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U13-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl