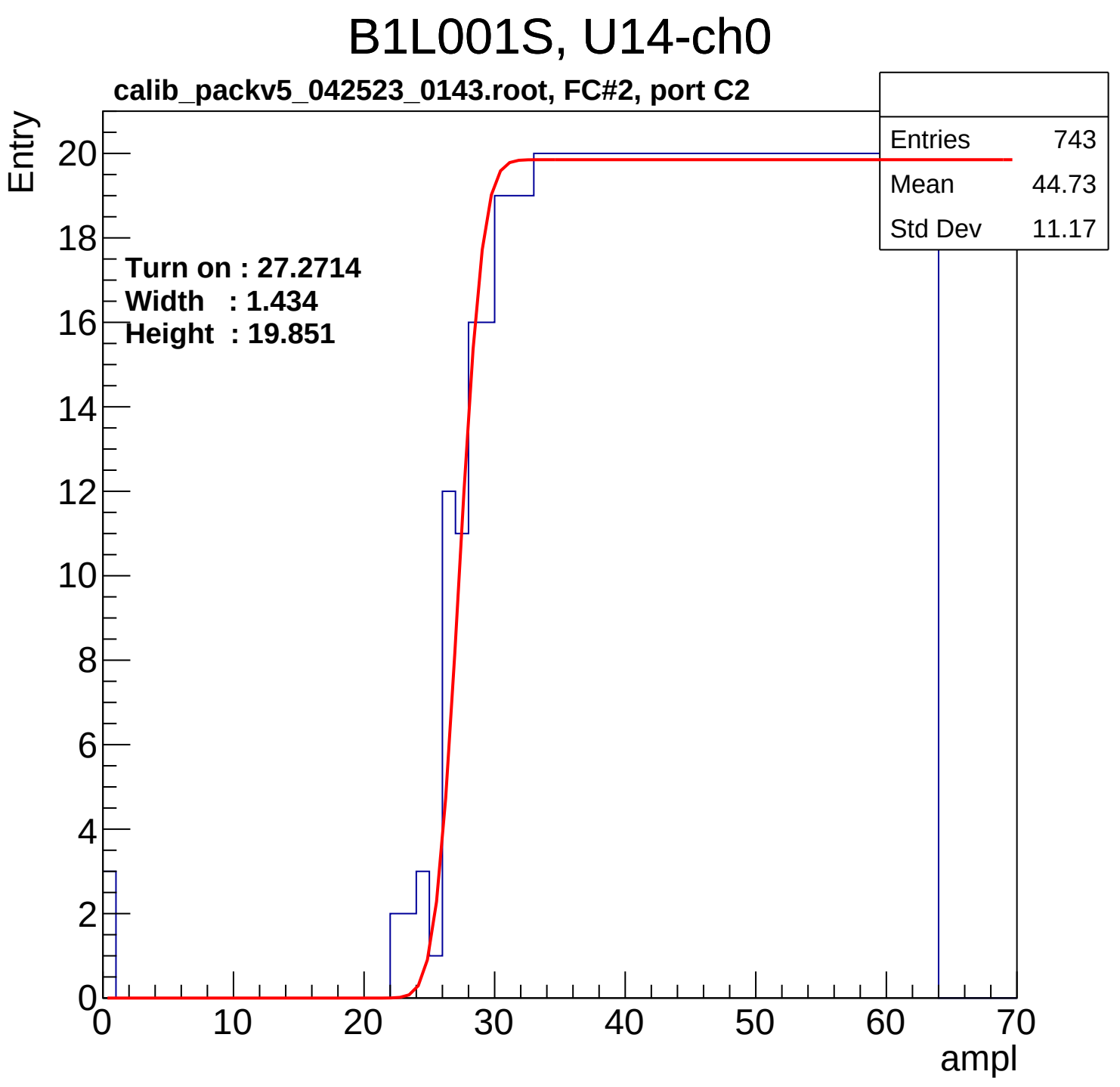
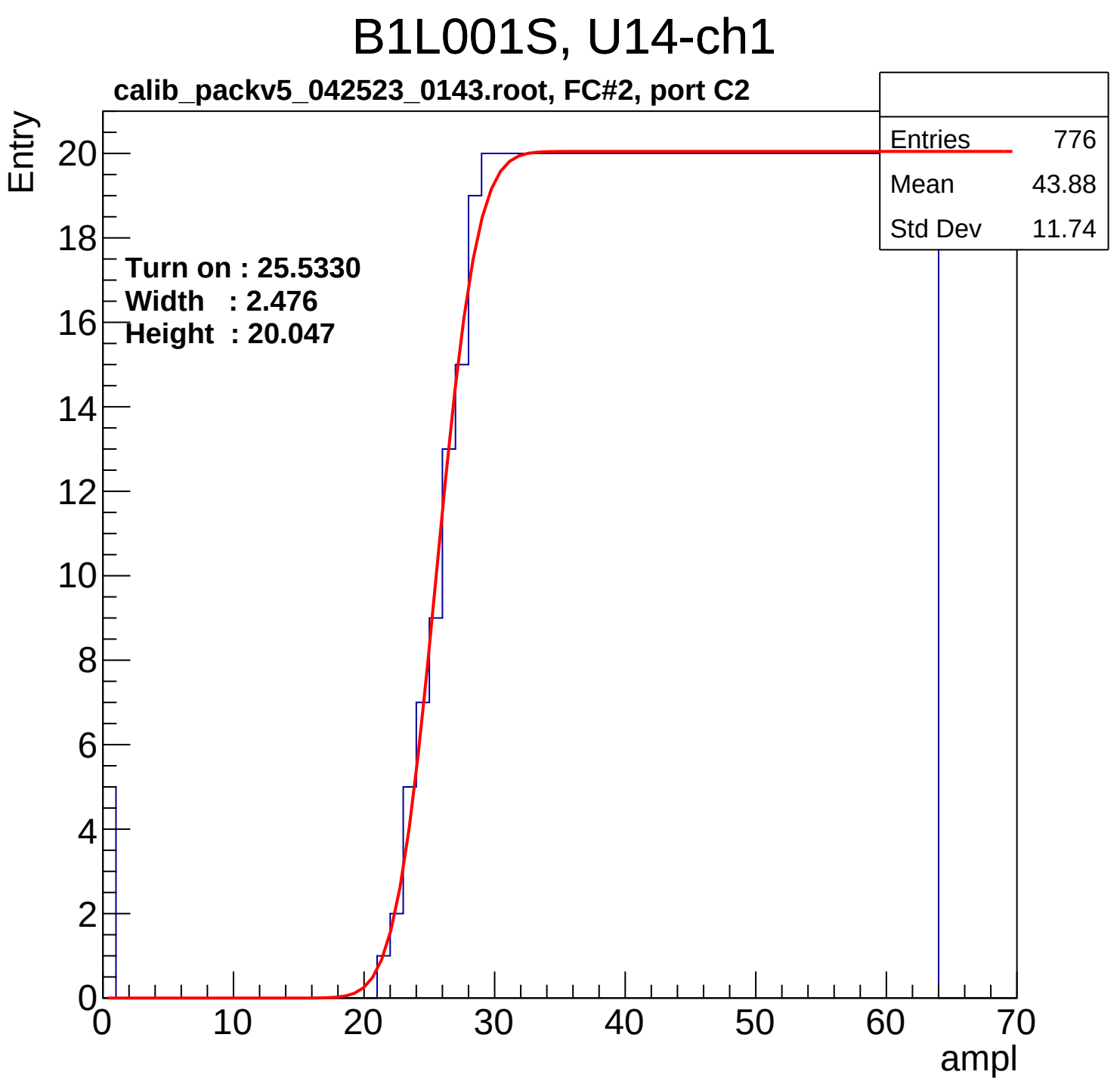
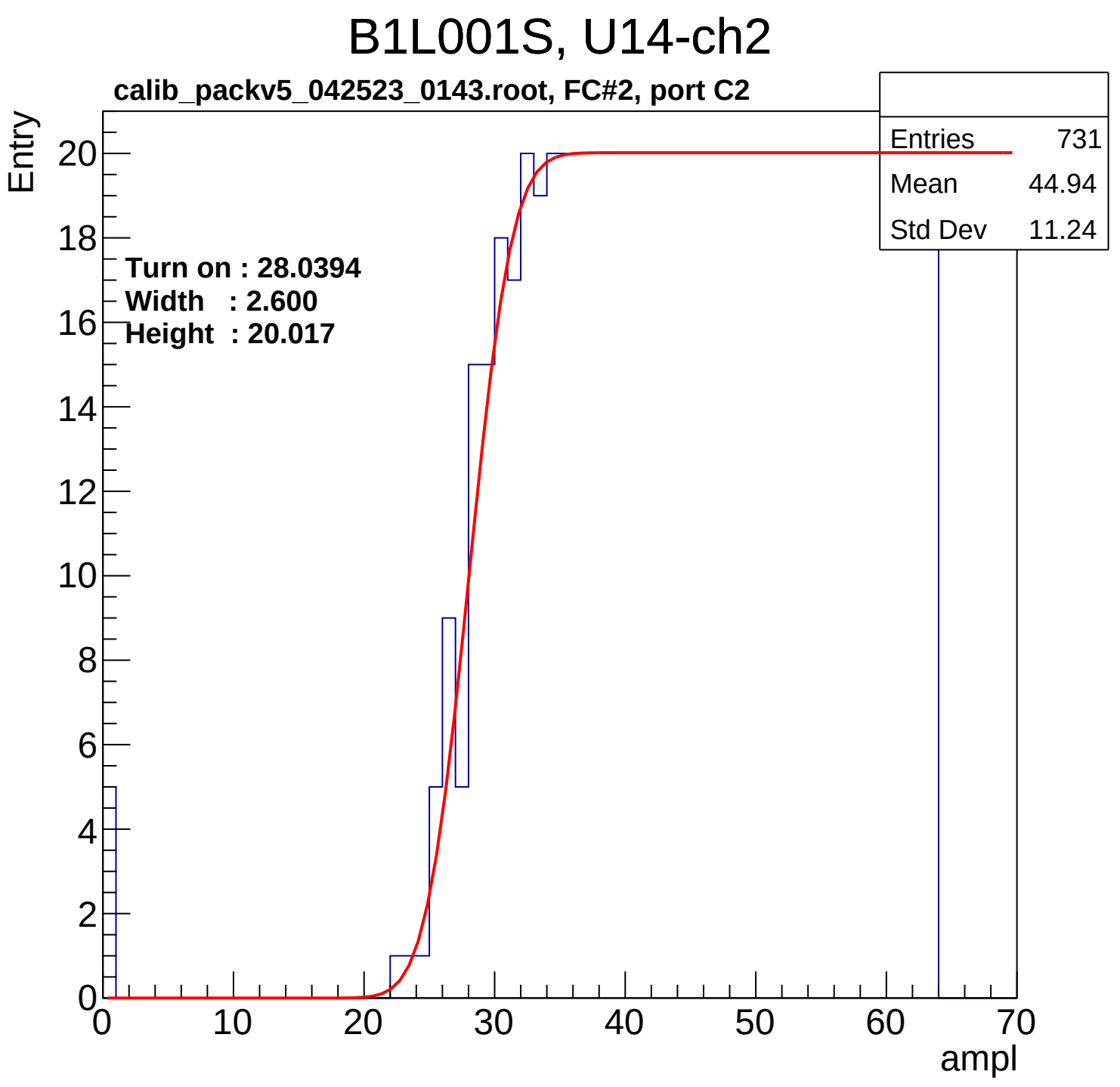
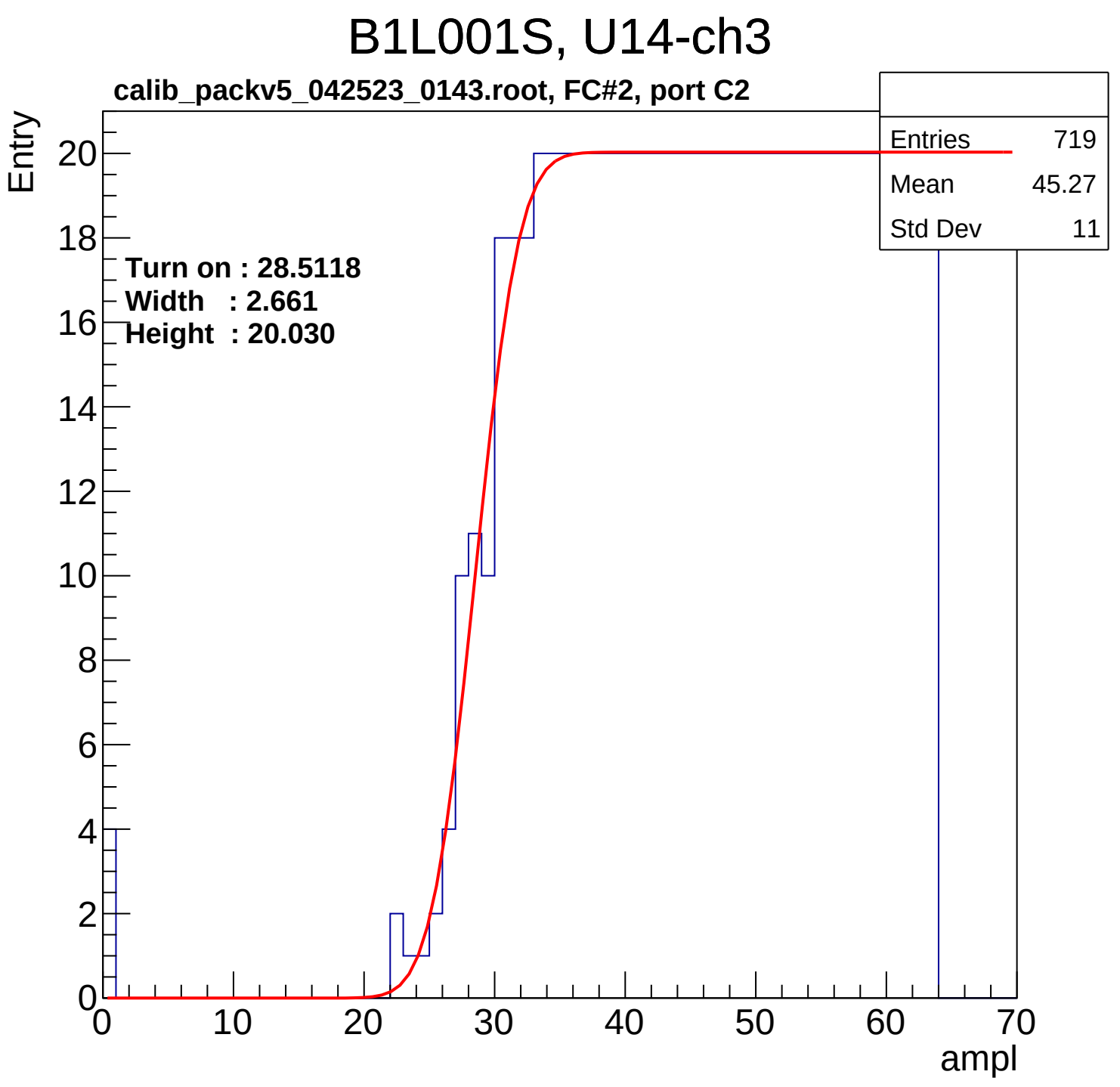
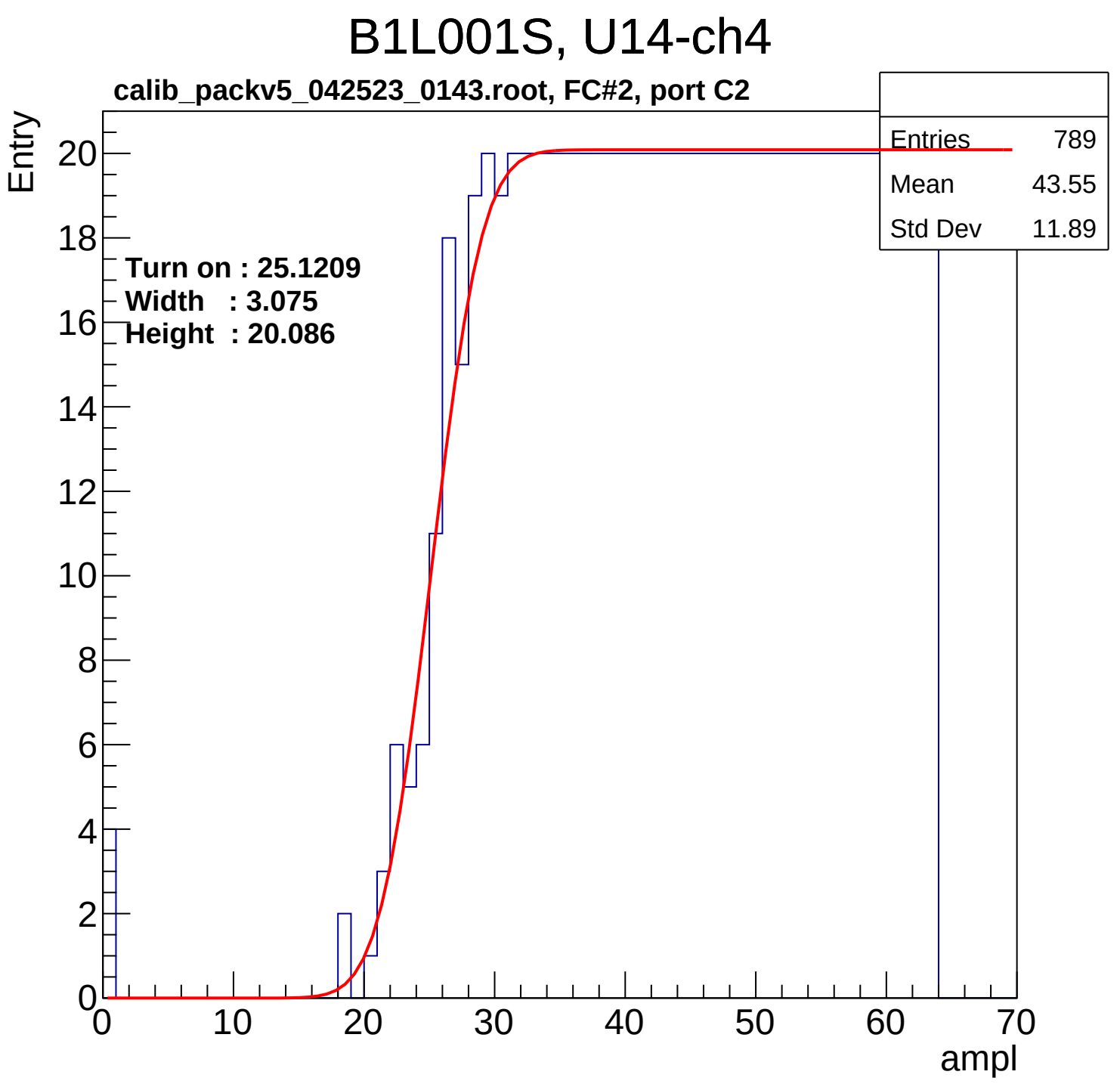
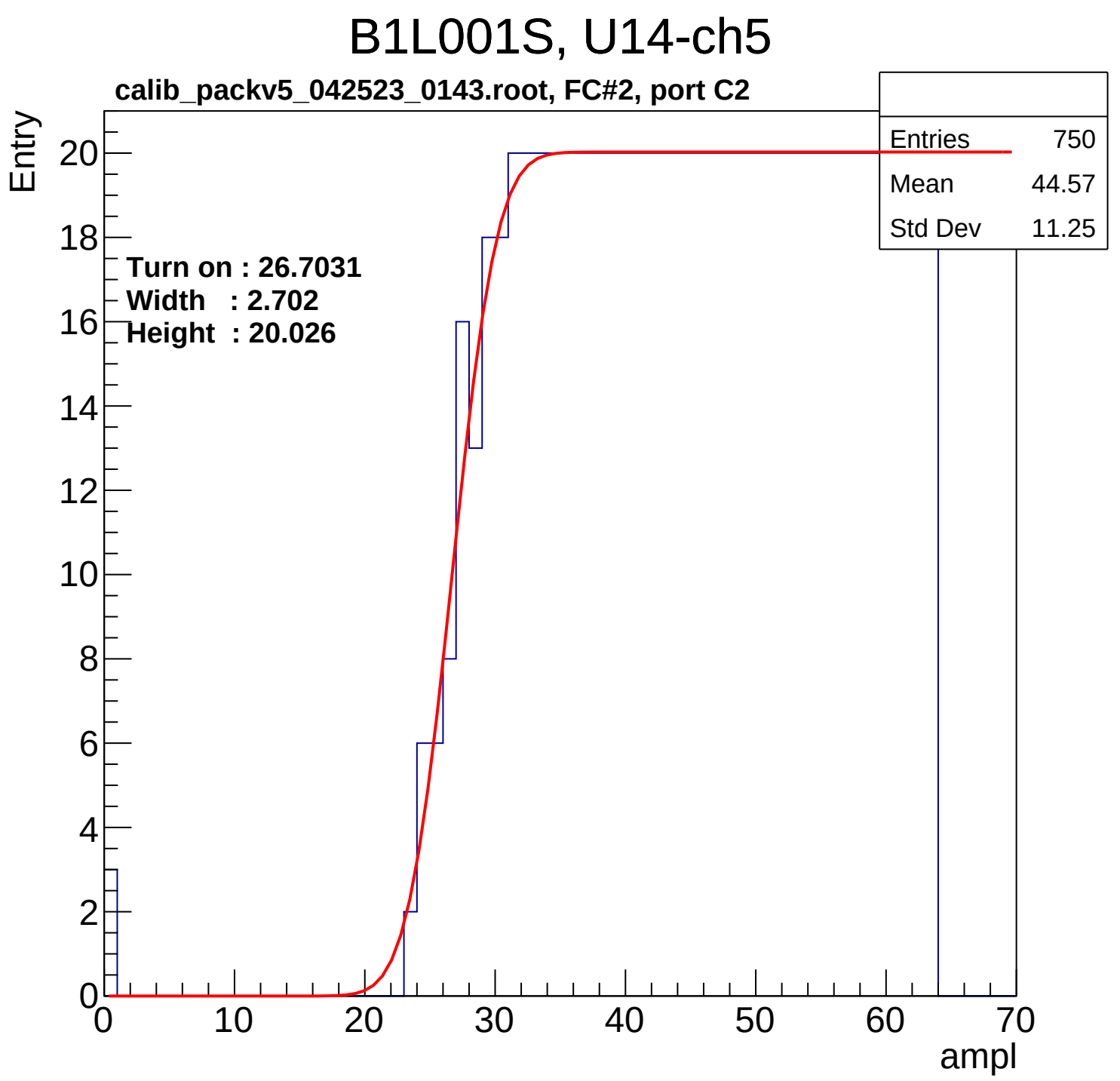

B1L001S, U14-ch0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.73
Std Dev 11.17
Turn on : 27.2714
Width : 1.434
Height : 19.851
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

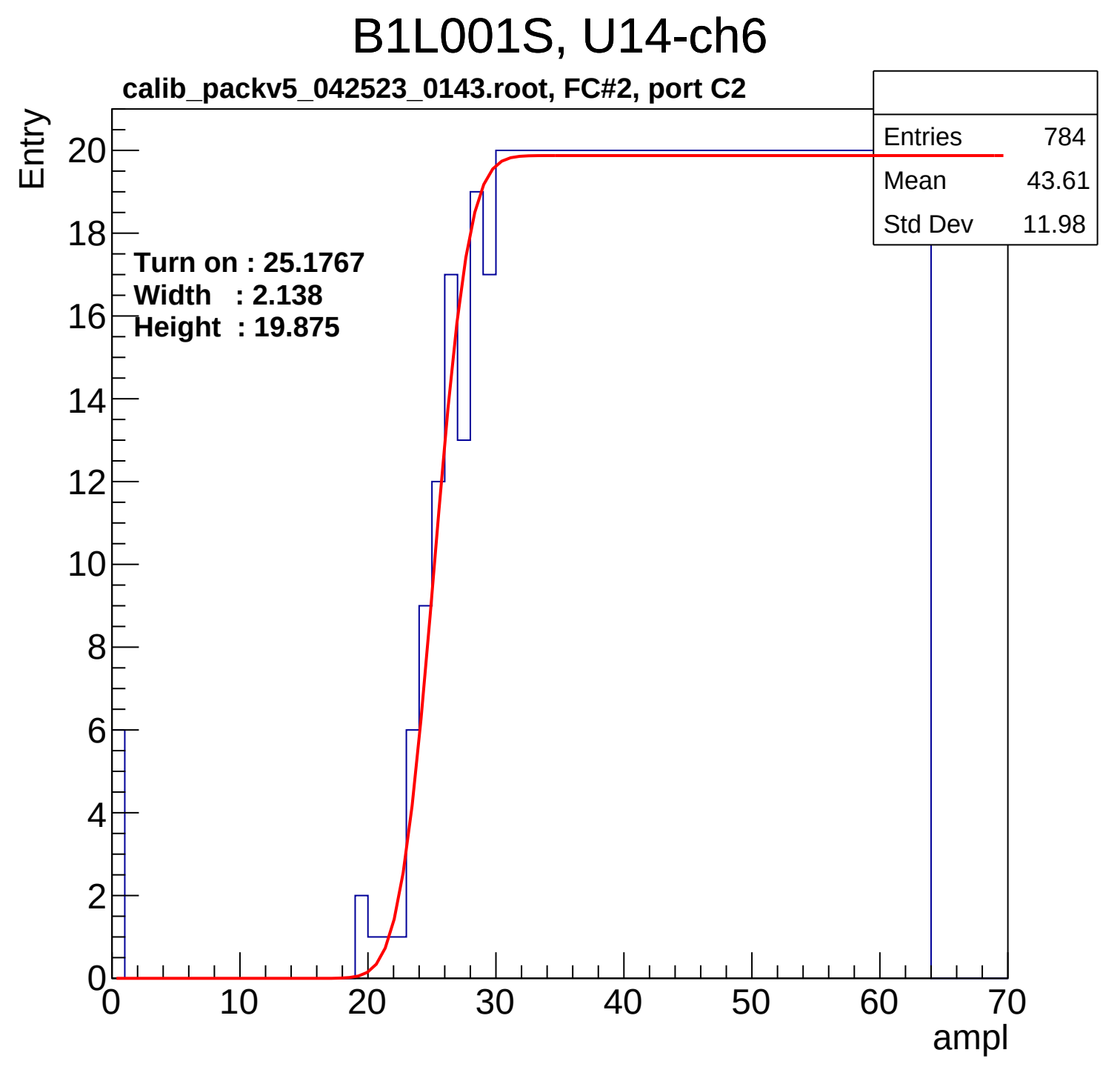

B1L001S, U14-ch1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 776
Mean 43.88
Std Dev 11.74
Turn on : 25.5330
Width : 2.476
Height : 20.047
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

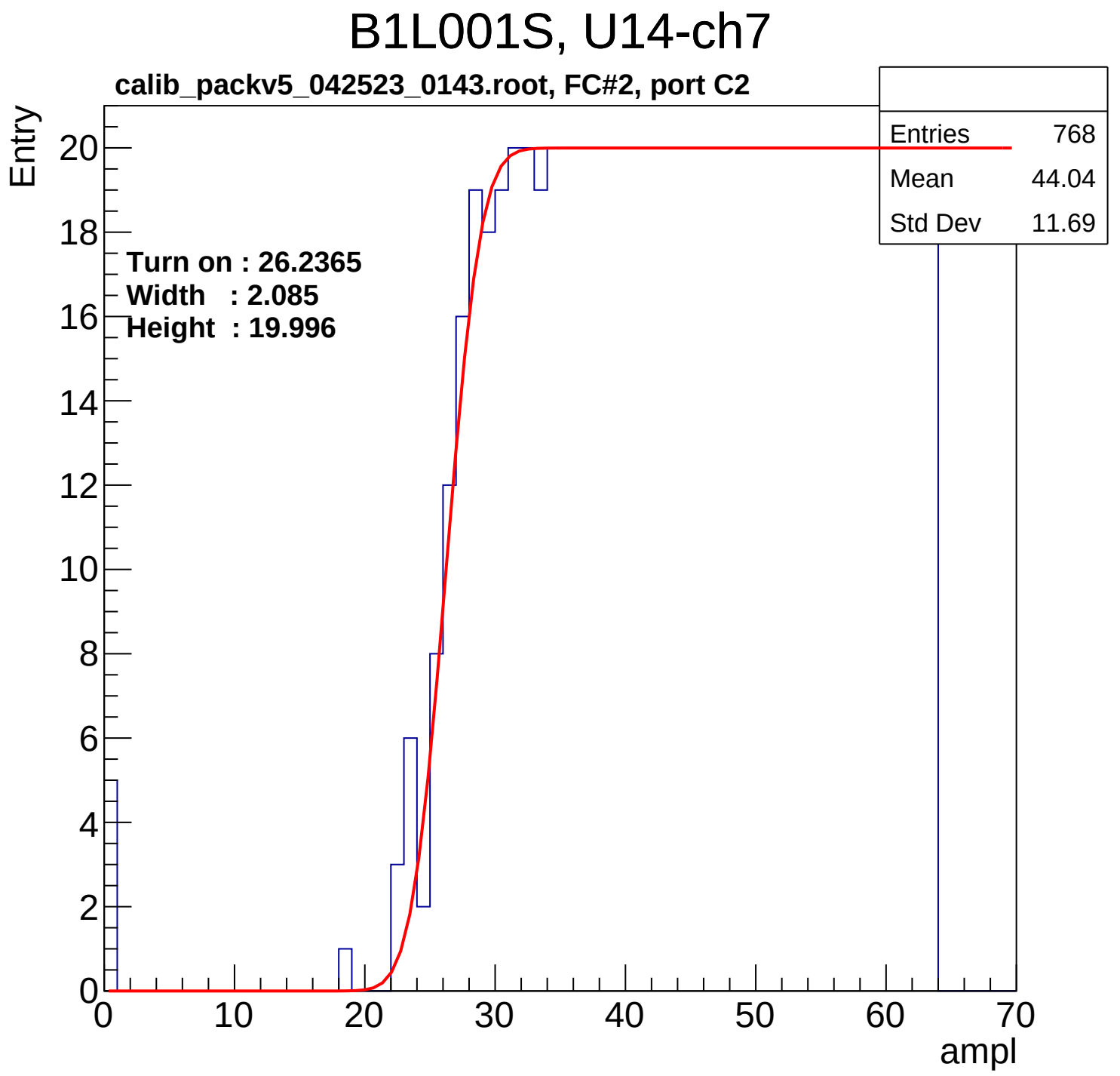

B1L001S, U14-ch2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 731
Mean 44.94
Std Dev 11.24
Turn on : 28.0394
Width : 2.600
Height : 20.017
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

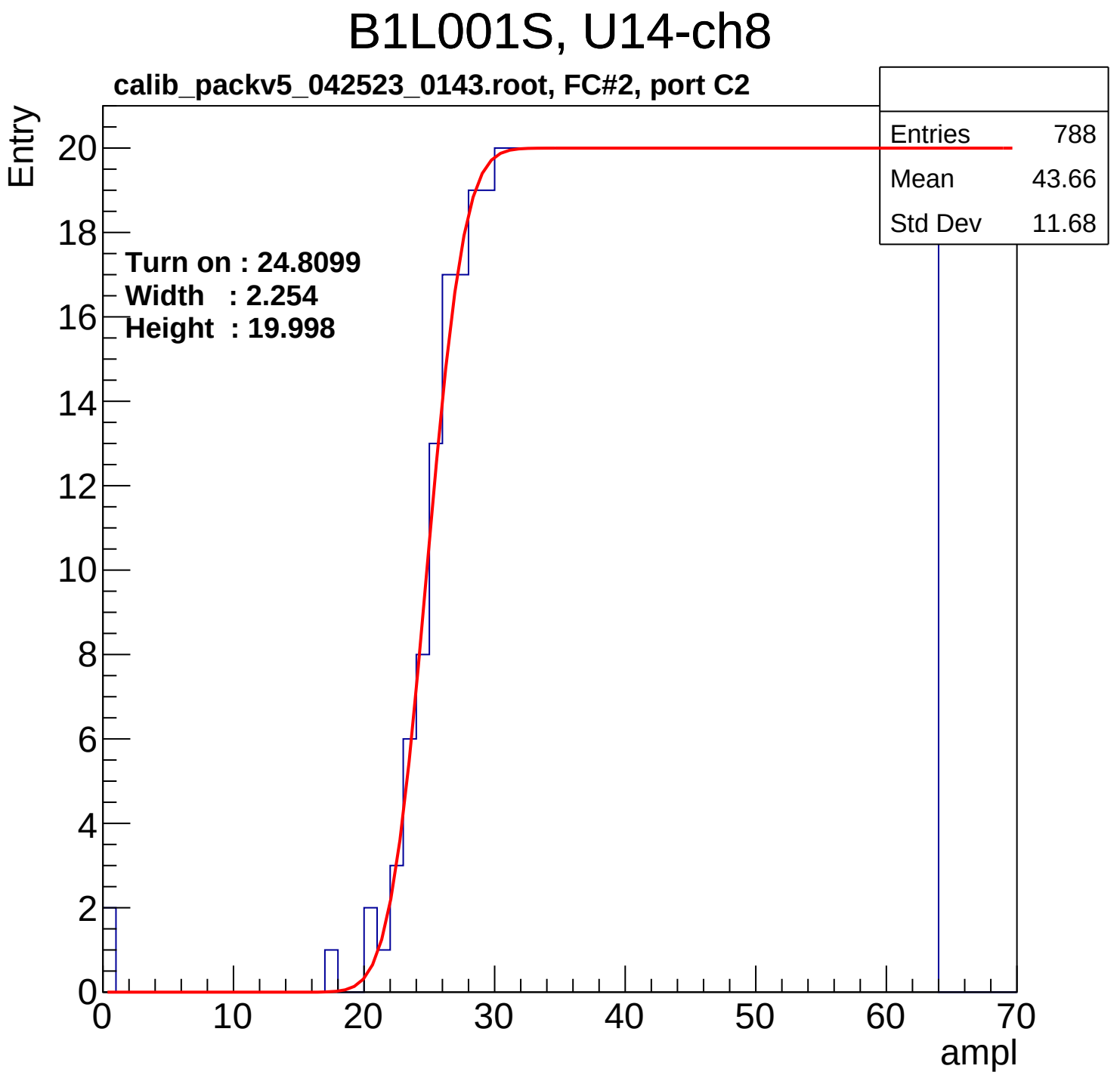

B1L001S, U14-ch3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 719
Mean 45.27
Std Dev 11
Turn on : 28.5118
Width : 2.661
Height : 20.030
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

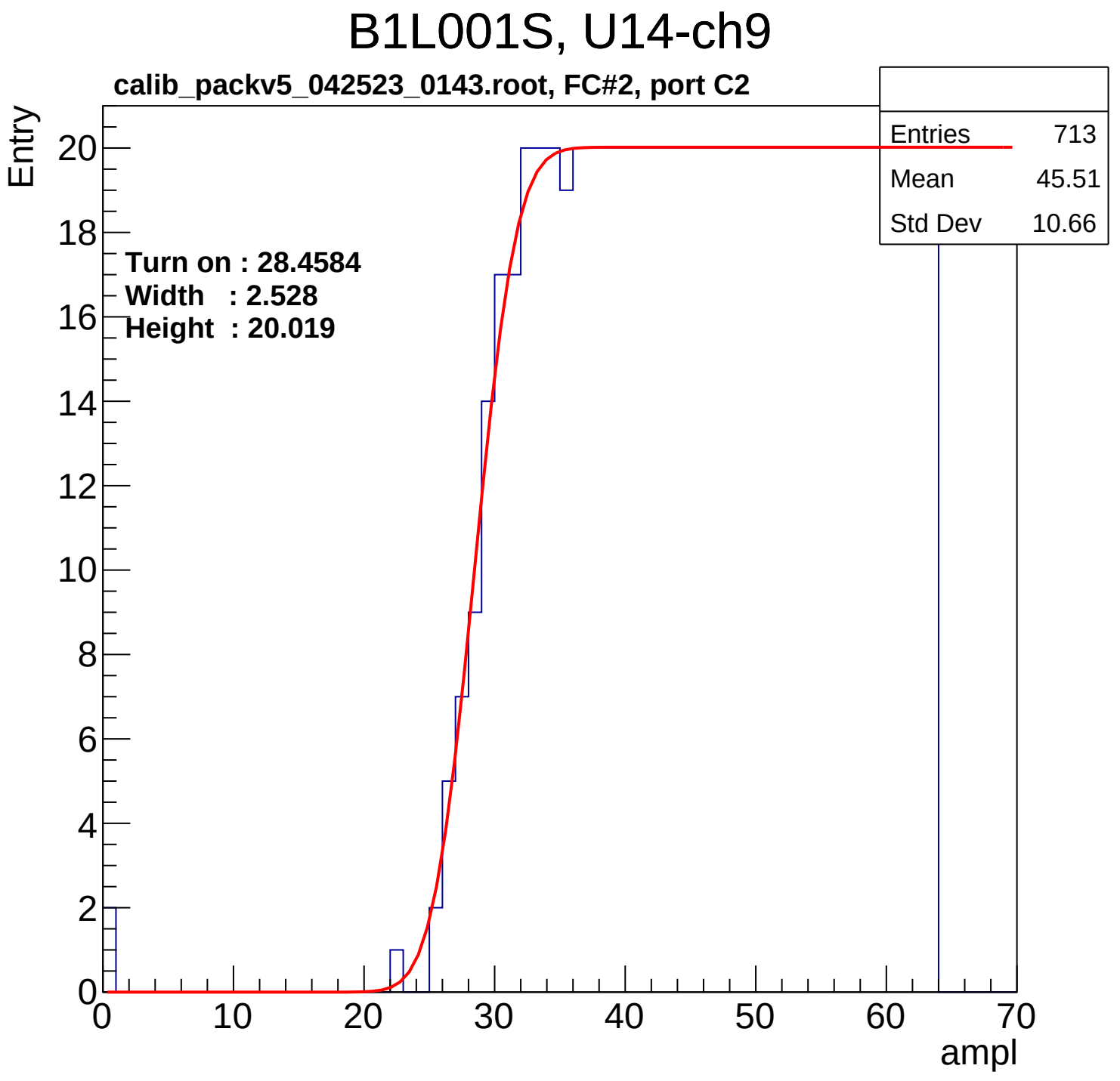

B1L001S, U14-ch4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 789
Mean 43.55
Std Dev 11.89
Turn on : 25.1209
Width : 3.075
Height : 20.086
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

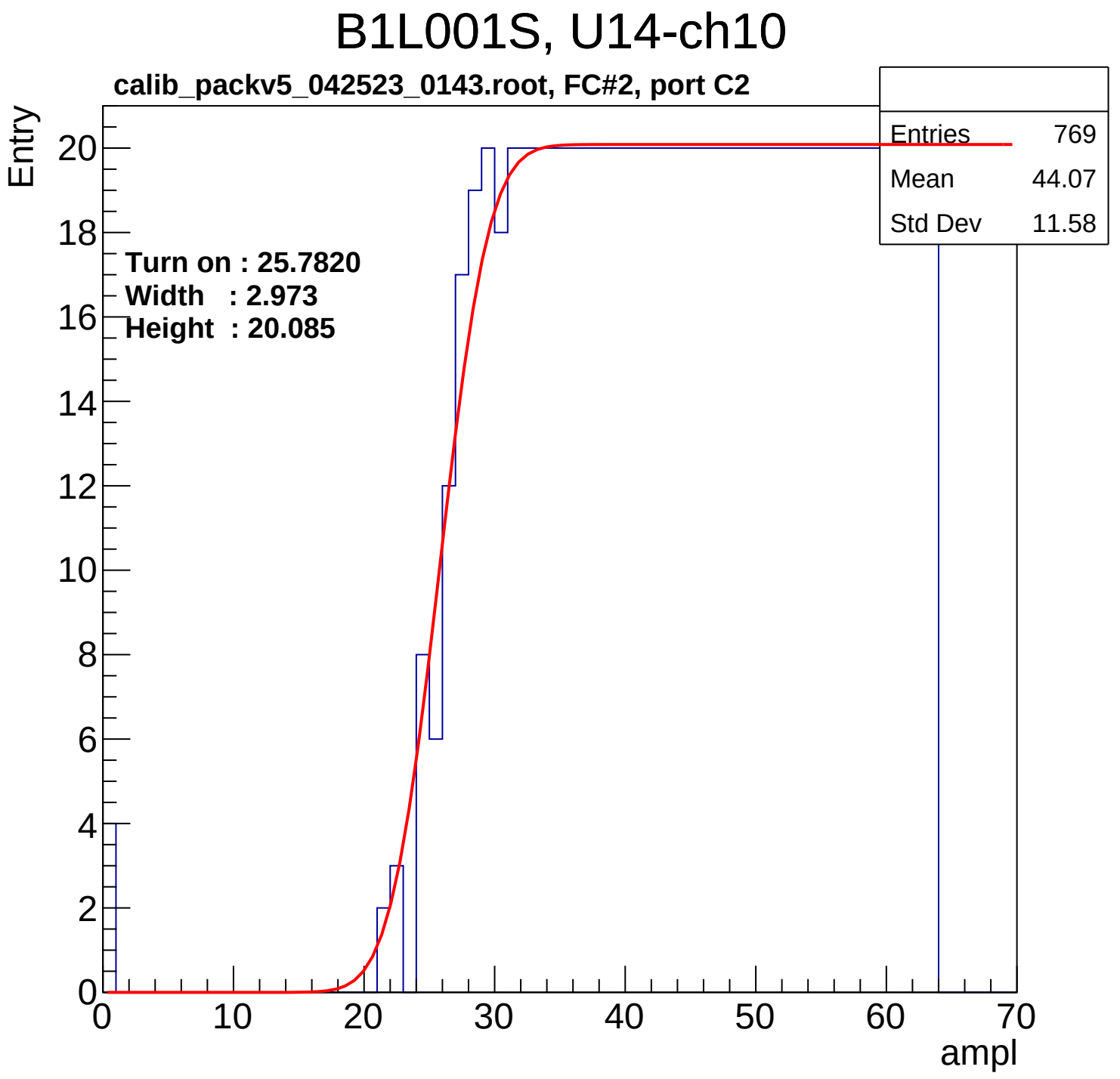

B1L001S, U14-ch5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 750
Mean 44.57
Std Dev 11.25
Turn on : 26.7031
Width : 2.702
Height : 20.026
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

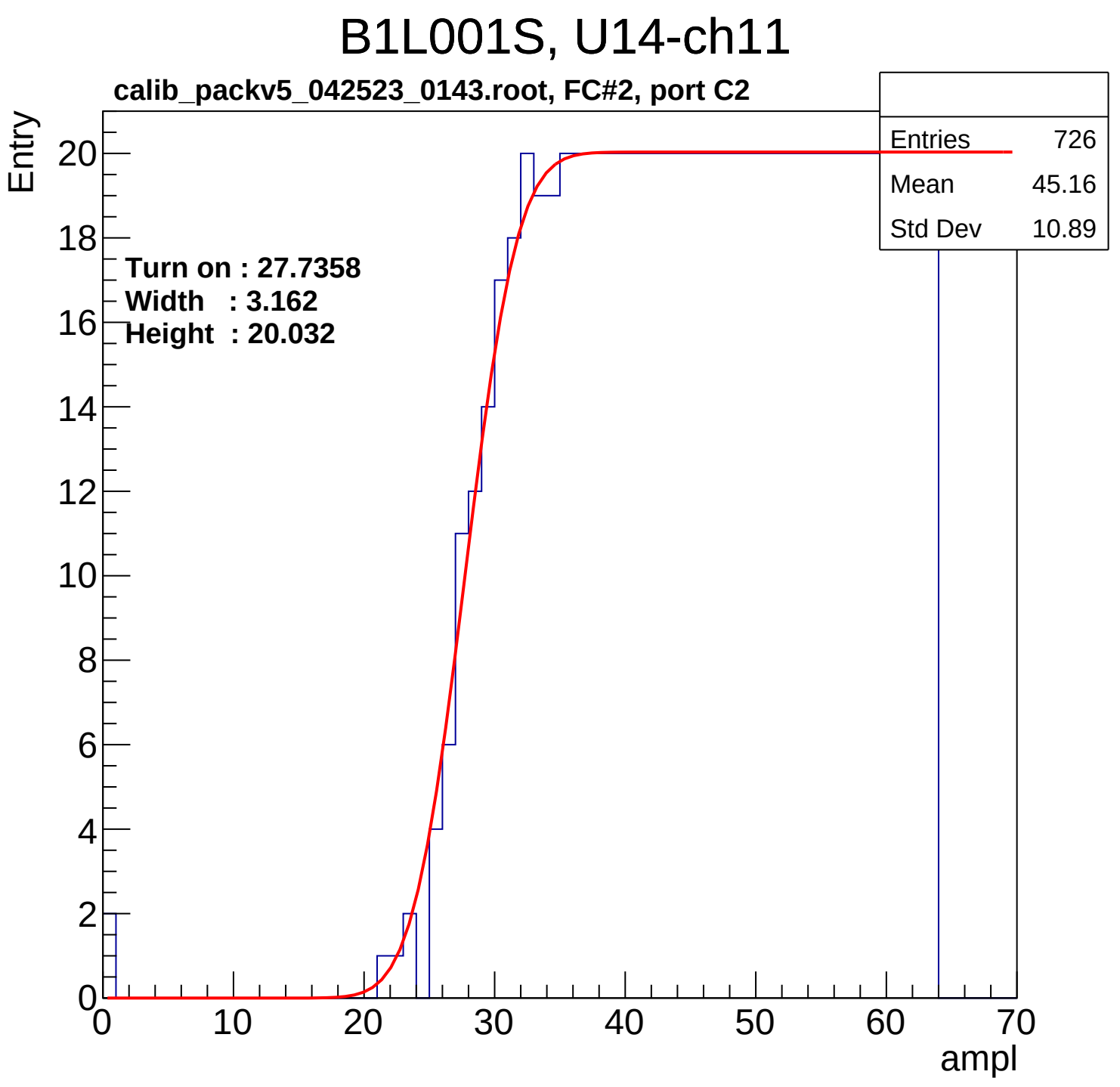

B1L001S, U14-ch6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 784
Mean 43.61
Std Dev 11.98
Turn on : 25.1767
Width : 2.138
Height : 19.875
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

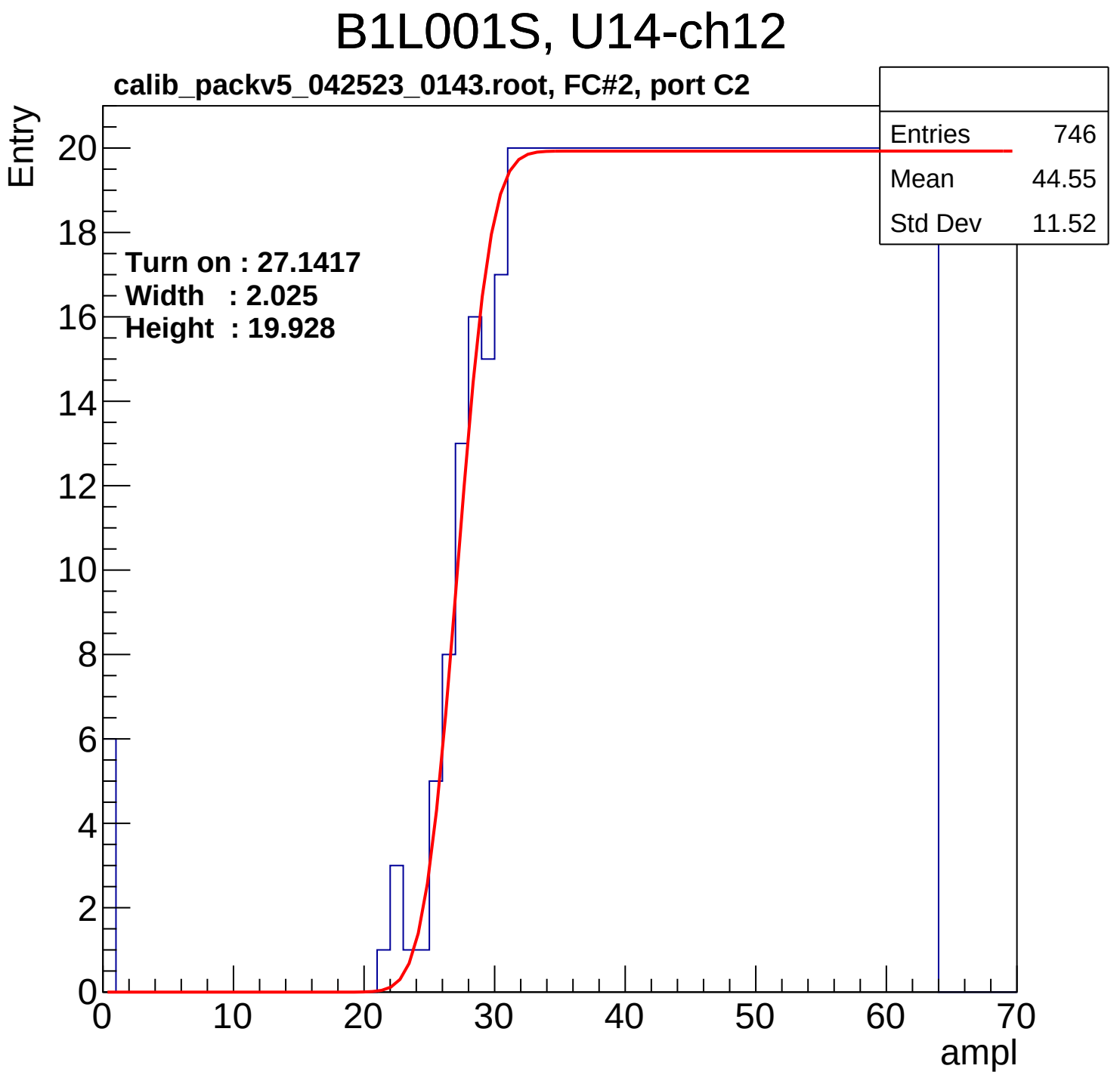

B1L001S, U14-ch7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 768
Mean 44.04
Std Dev 11.69
Turn on : 26.2365
Width : 2.085
Height : 19.996
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

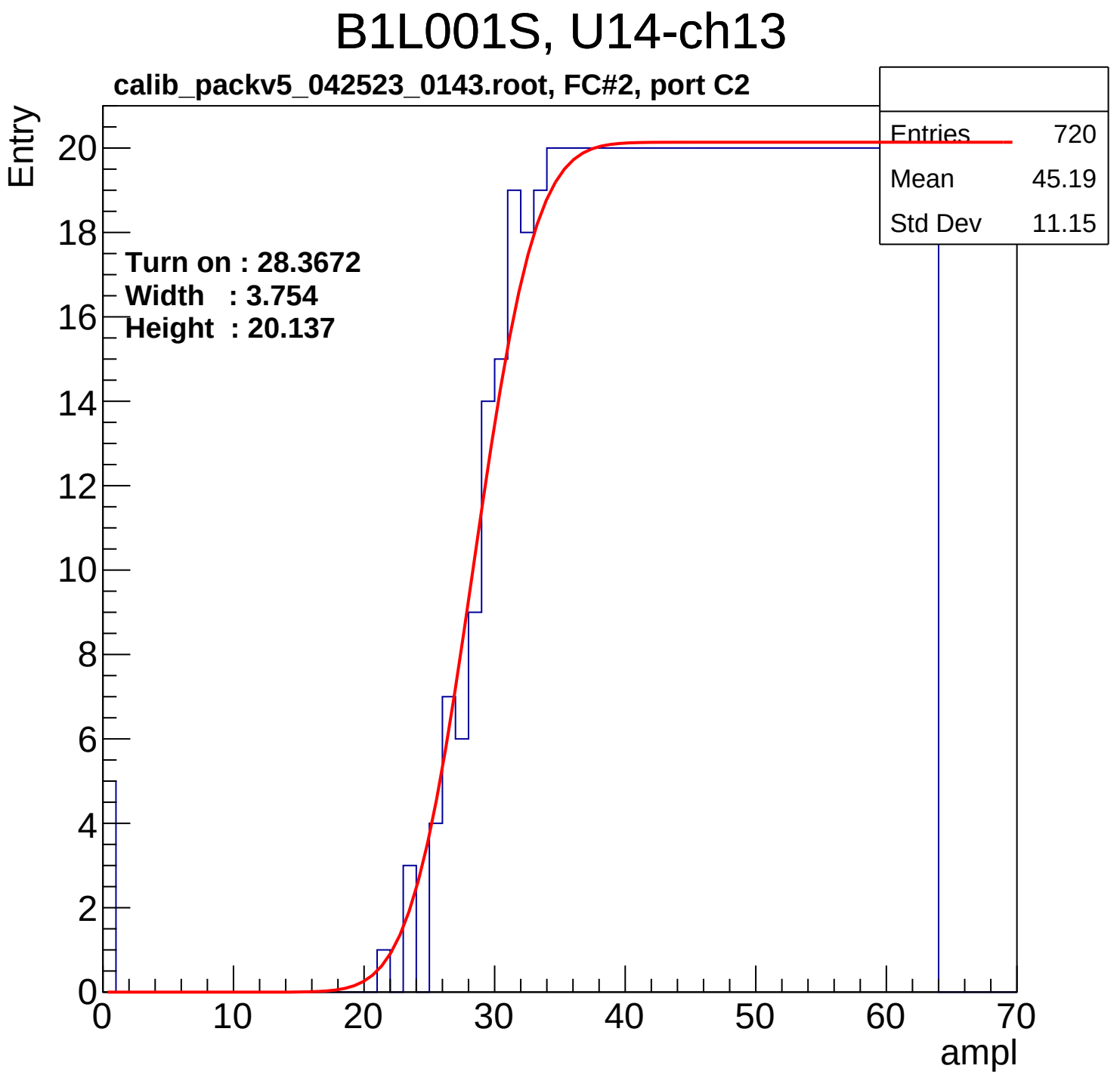

B1L001S, U14-ch8
calib_packv5_042523_0143.root, FC#2, port C2
Entries 788
Mean 43.66
Std Dev 11.68
Turn on : 24.8099
Width : 2.254
Height : 19.998
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

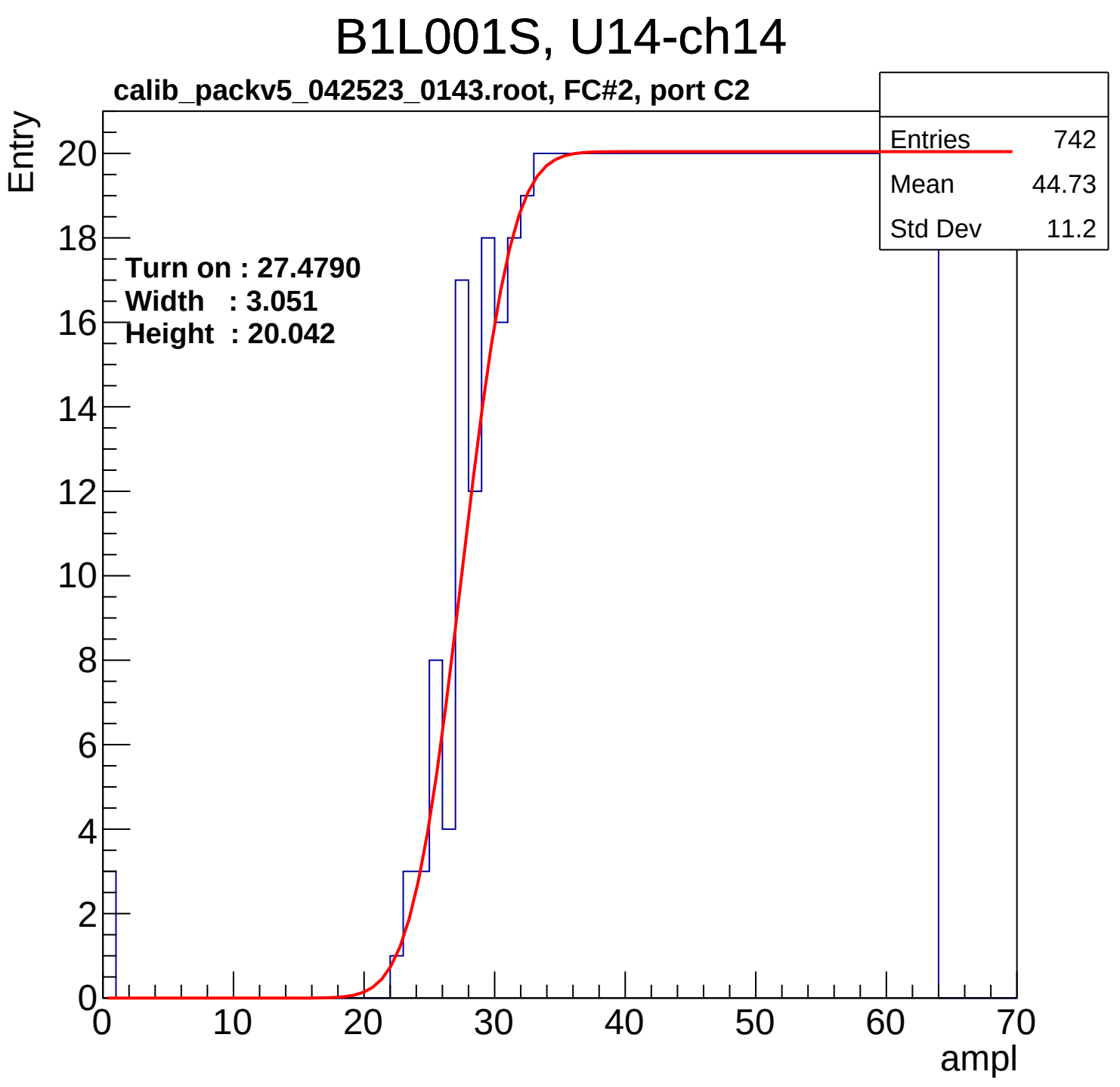

B1L001S, U14-ch9
calib_packv5_042523_0143.root, FC#2, port C2
Entries 713
Mean 45.51
Std Dev 10.66
Turn on : 28.4584
Width : 2.528
Height : 20.019
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

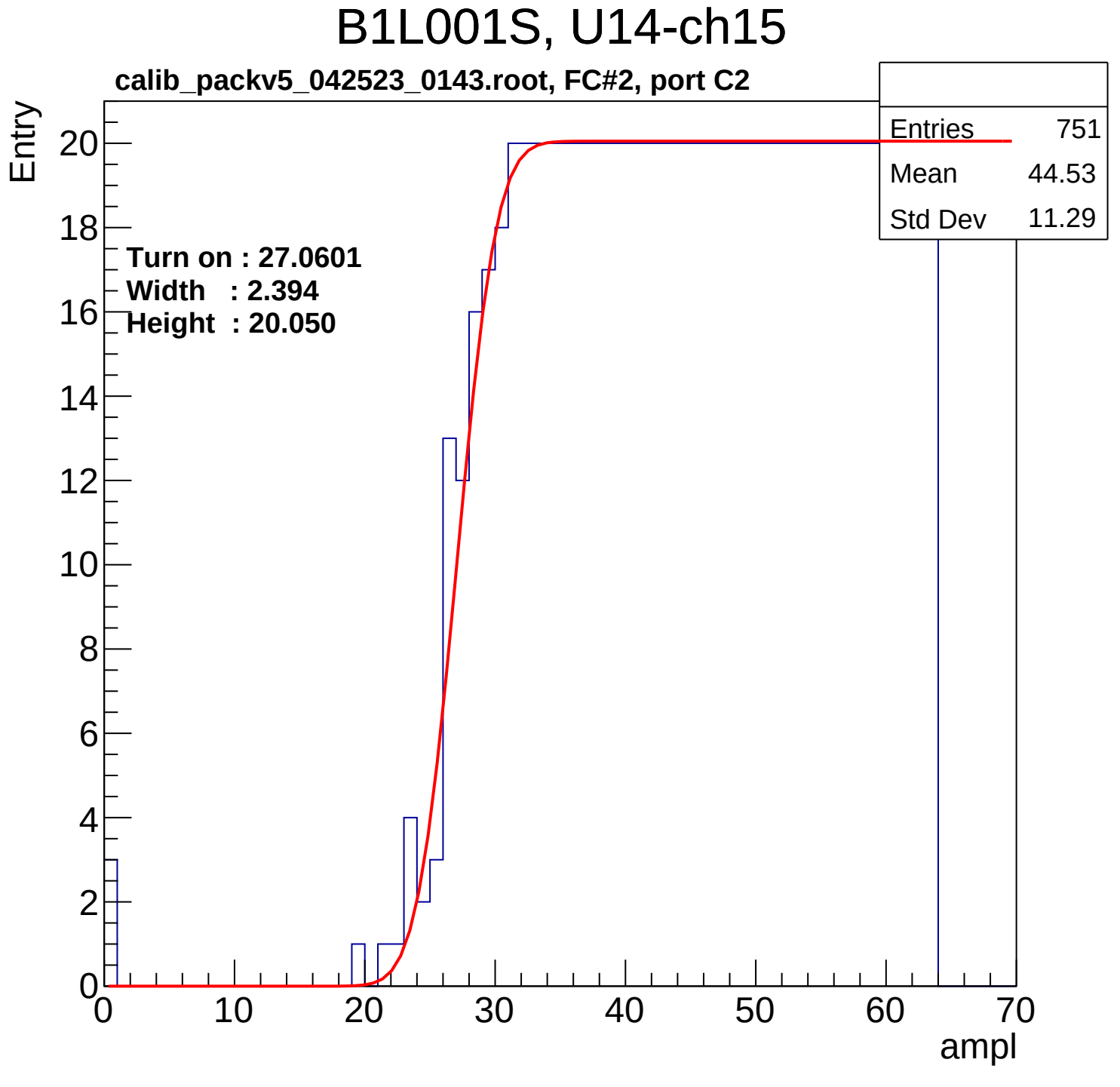

B1L001S, U14-ch10
calib_packv5_042523_0143.root, FC#2, port C2
Entries 769
Mean 44.07
Std Dev 11.58
Turn on : 25.7820
Width : 2.973
Height : 20.085
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

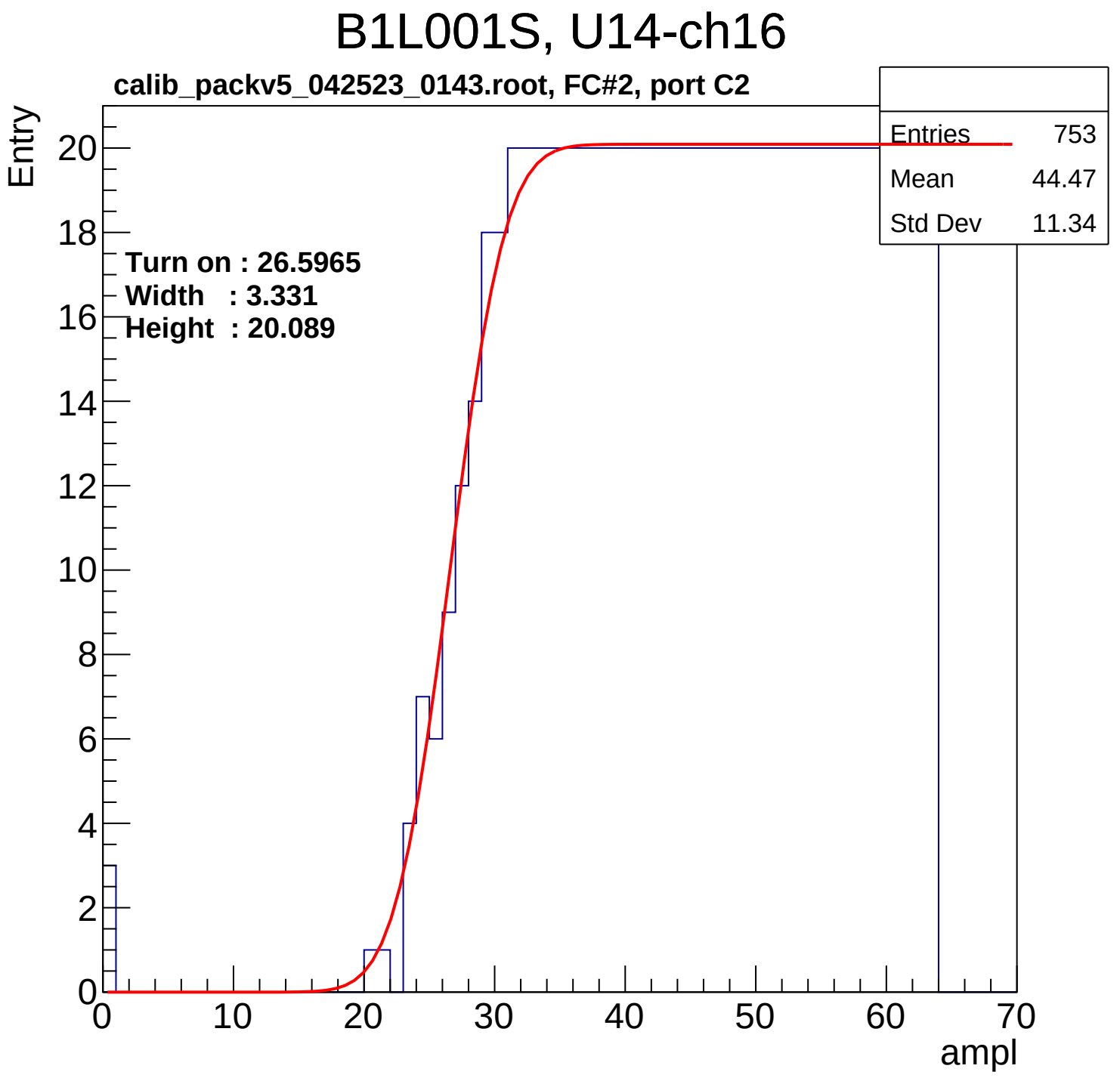

B1L001S, U14-ch11
calib_packv5_042523_0143.root, FC#2, port C2
Entries 726
Mean 45.16
Std Dev 10.89
Turn on : 27.7358
Width : 3.162
Height : 20.032
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

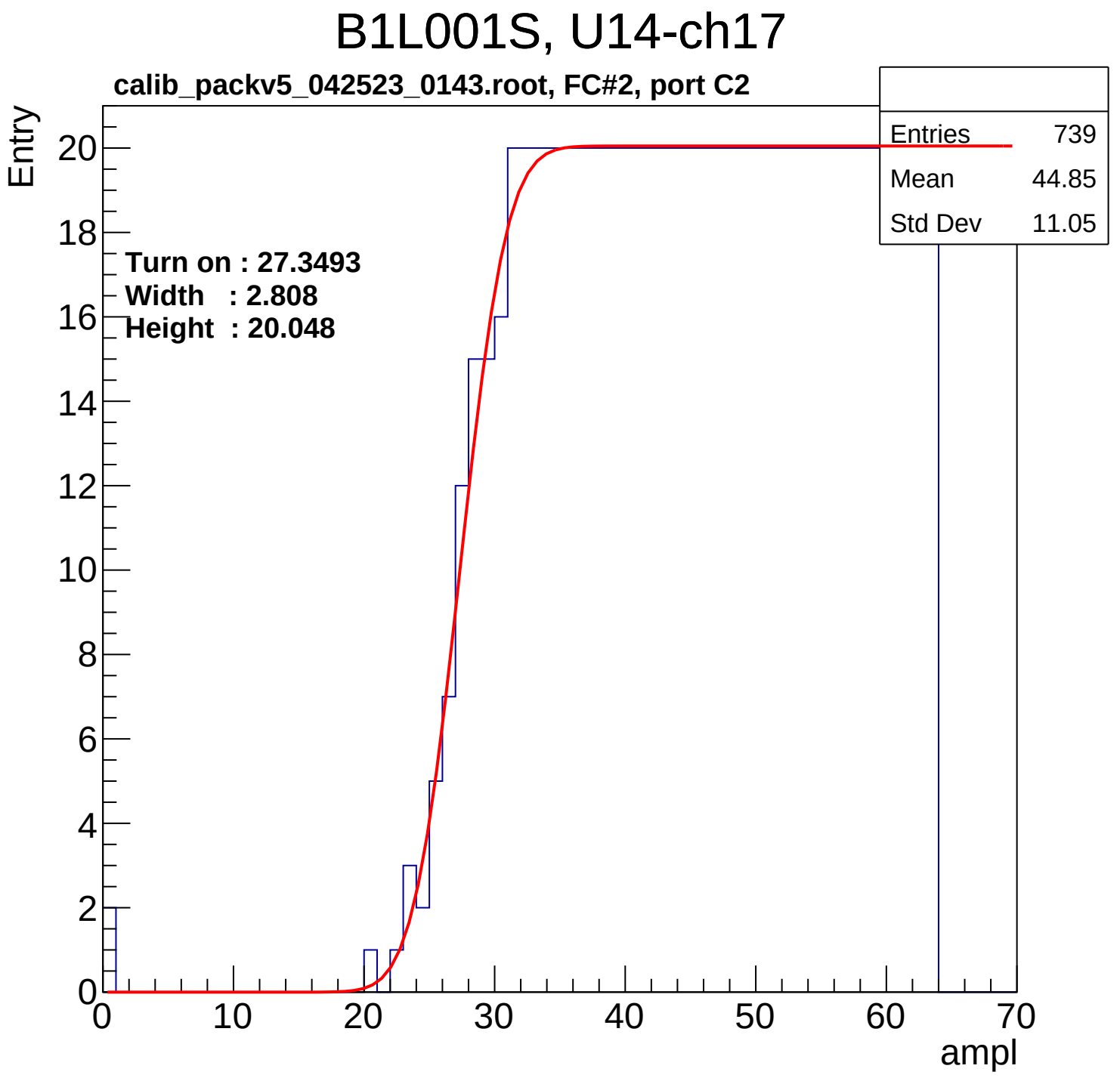

B1L001S, U14-ch12
calib_packv5_042523_0143.root, FC#2, port C2
Entries 746
Mean 44.55
Std Dev 11.52
Turn on : 27.1417
Width : 2.025
Height : 19.928
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

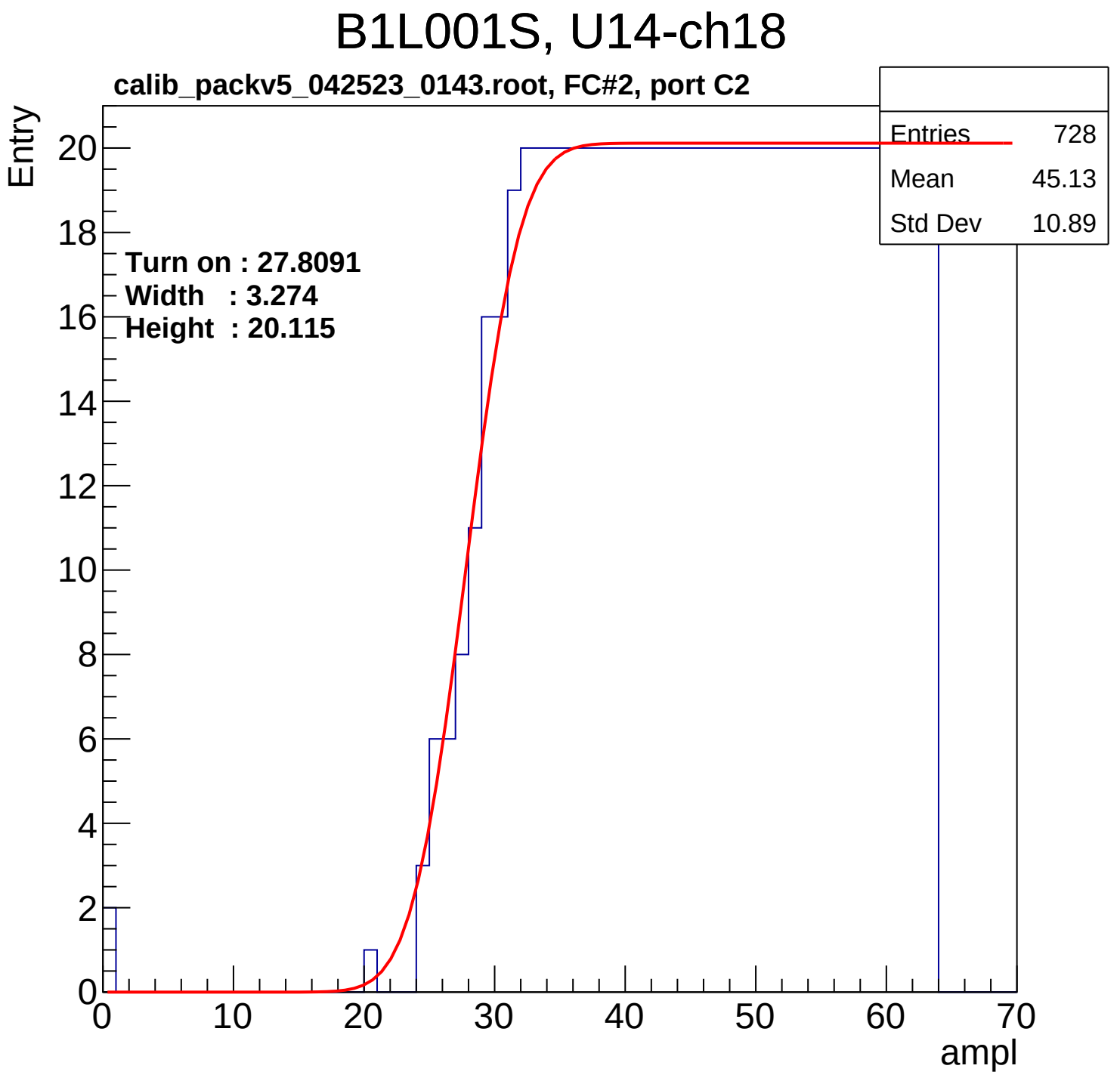

B1L001S, U14-ch13
calib_packv5_042523_0143.root, FC#2, port C2
Entries 720
Mean 45.19
Std Dev 11.15
Turn on : 28.3672
Width : 3.754
Height : 20.137
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

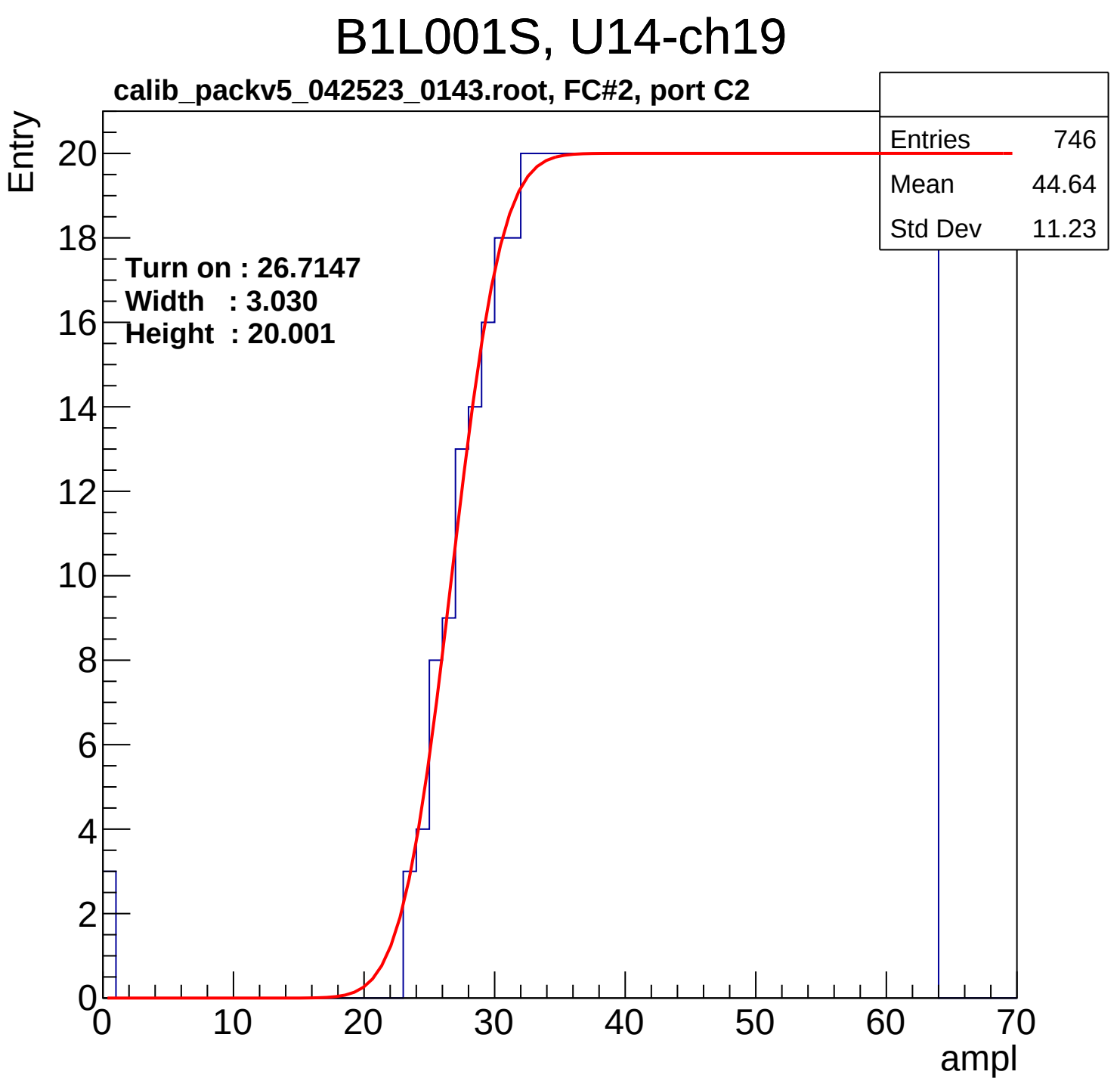

B1L001S, U14-ch14
calib_packv5_042523_0143.root, FC#2, port C2
Entries 742
Mean 44.73
Std Dev 11.2
Turn on : 27.4790
Width : 3.051
Height : 20.042
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

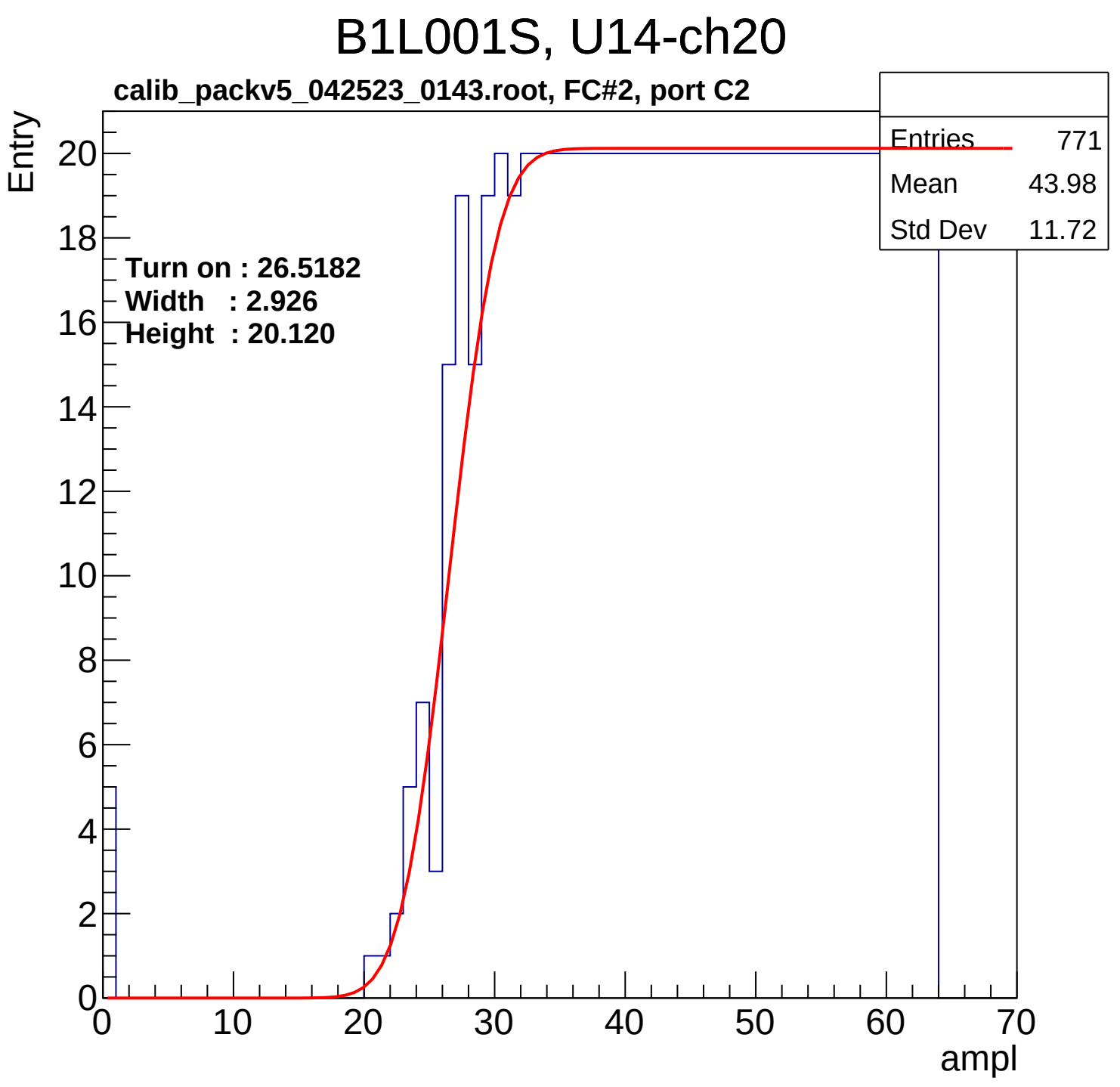

B1L001S, U14-ch15
calib_packv5_042523_0143.root, FC#2, port C2
Entries 751
Mean 44.53
Std Dev 11.29
Turn on : 27.0601
Width : 2.394
Height : 20.050
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

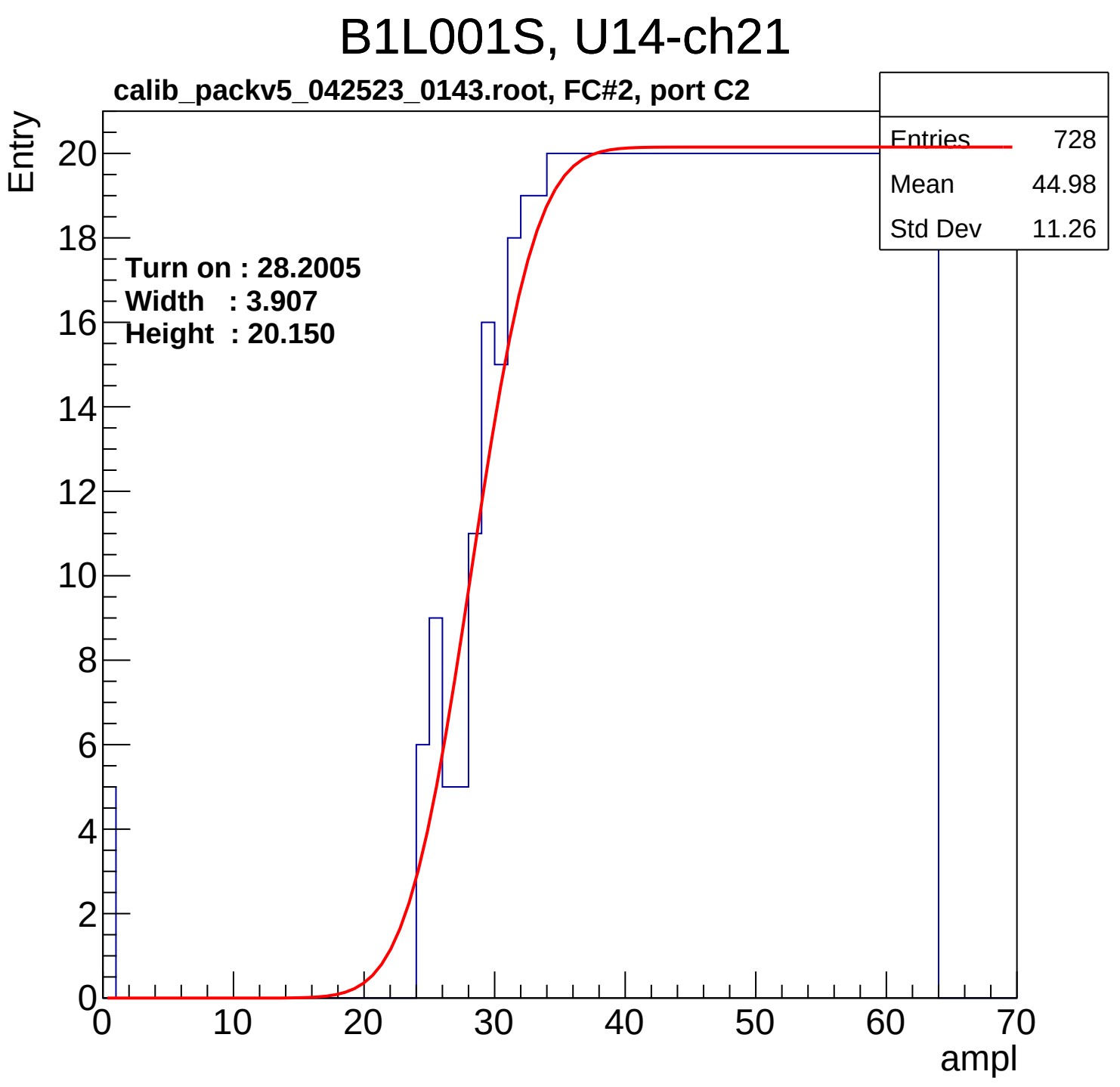

B1L001S, U14-ch16
calib_packv5_042523_0143.root, FC#2, port C2
Entries 753
Mean 44.47
Std Dev 11.34
Turn on : 26.5965
Width : 3.331
Height : 20.089
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

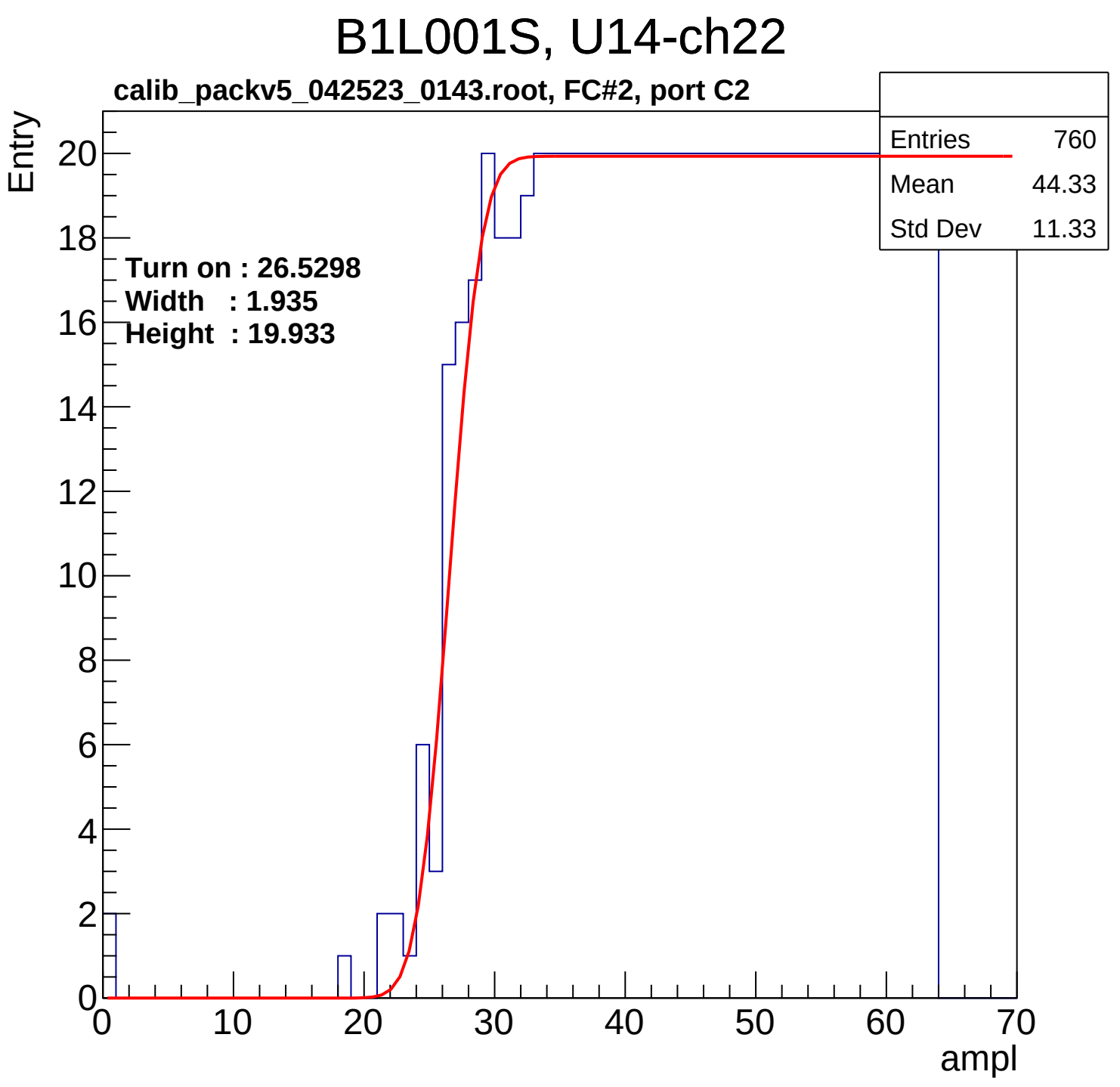

B1L001S, U14-ch17
calib_packv5_042523_0143.root, FC#2, port C2
Entries 739
Mean 44.85
Std Dev 11.05
Turn on : 27.3493
Width : 2.808
Height : 20.048
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

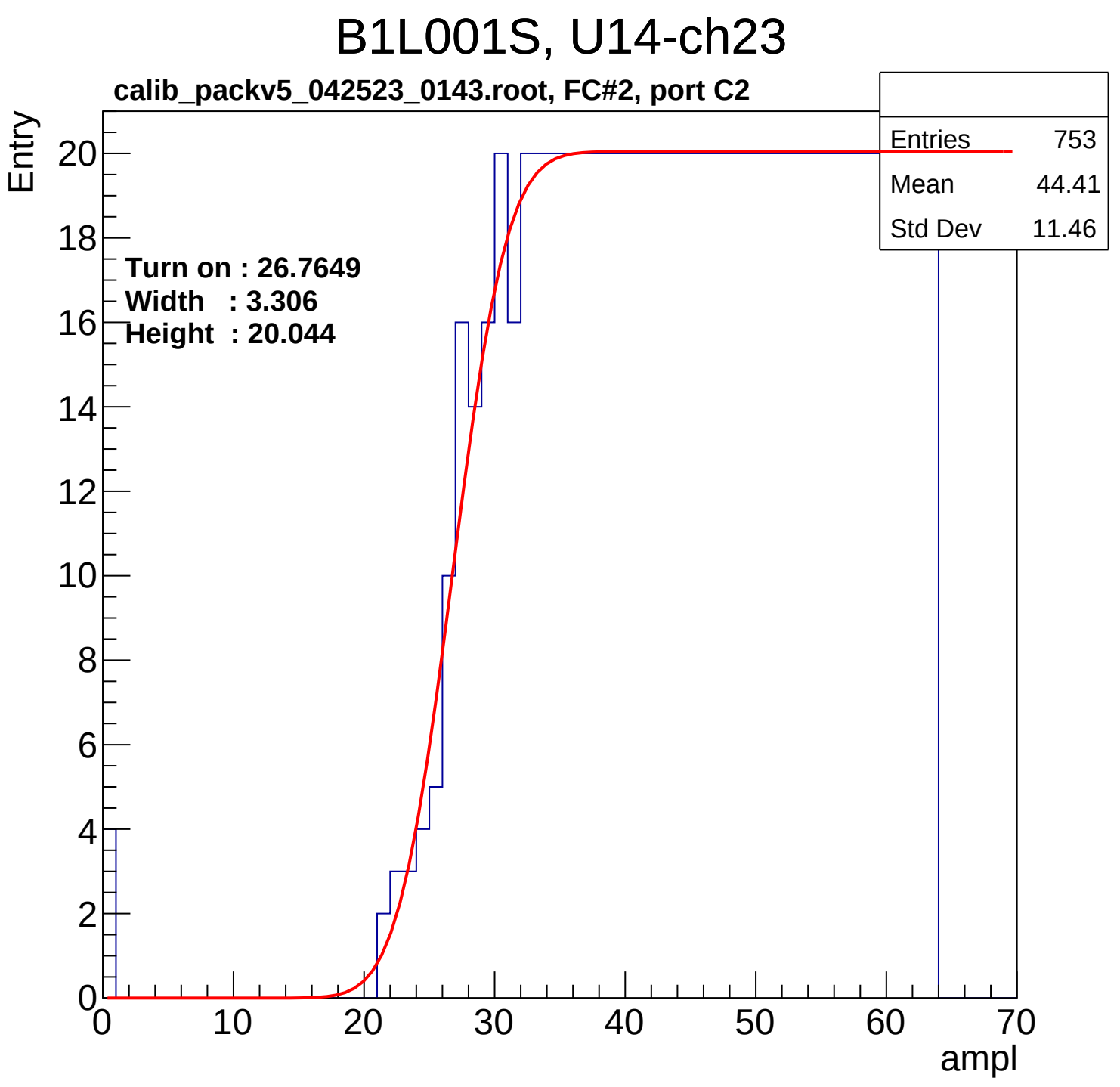

B1L001S, U14-ch18
calib_packv5_042523_0143.root, FC#2, port C2
Entries 728
Mean 45.13
Std Dev 10.89
Turn on : 27.8091
Width : 3.274
Height : 20.115
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

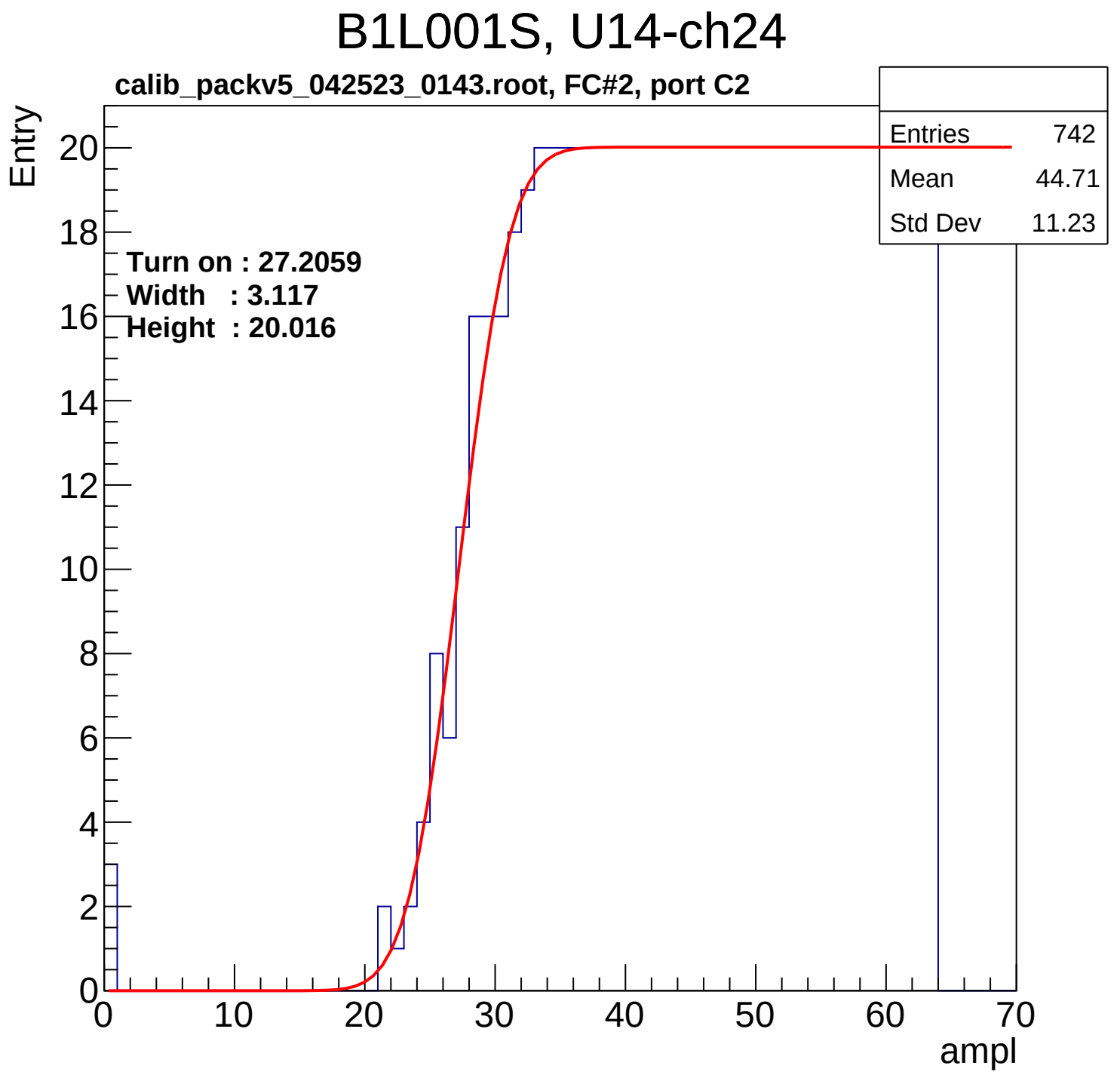

B1L001S, U14-ch19
calib_packv5_042523_0143.root, FC#2, port C2
Entries 746
Mean 44.64
Std Dev 11.23
Turn on : 26.7147
Width : 3.030
Height : 20.001
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

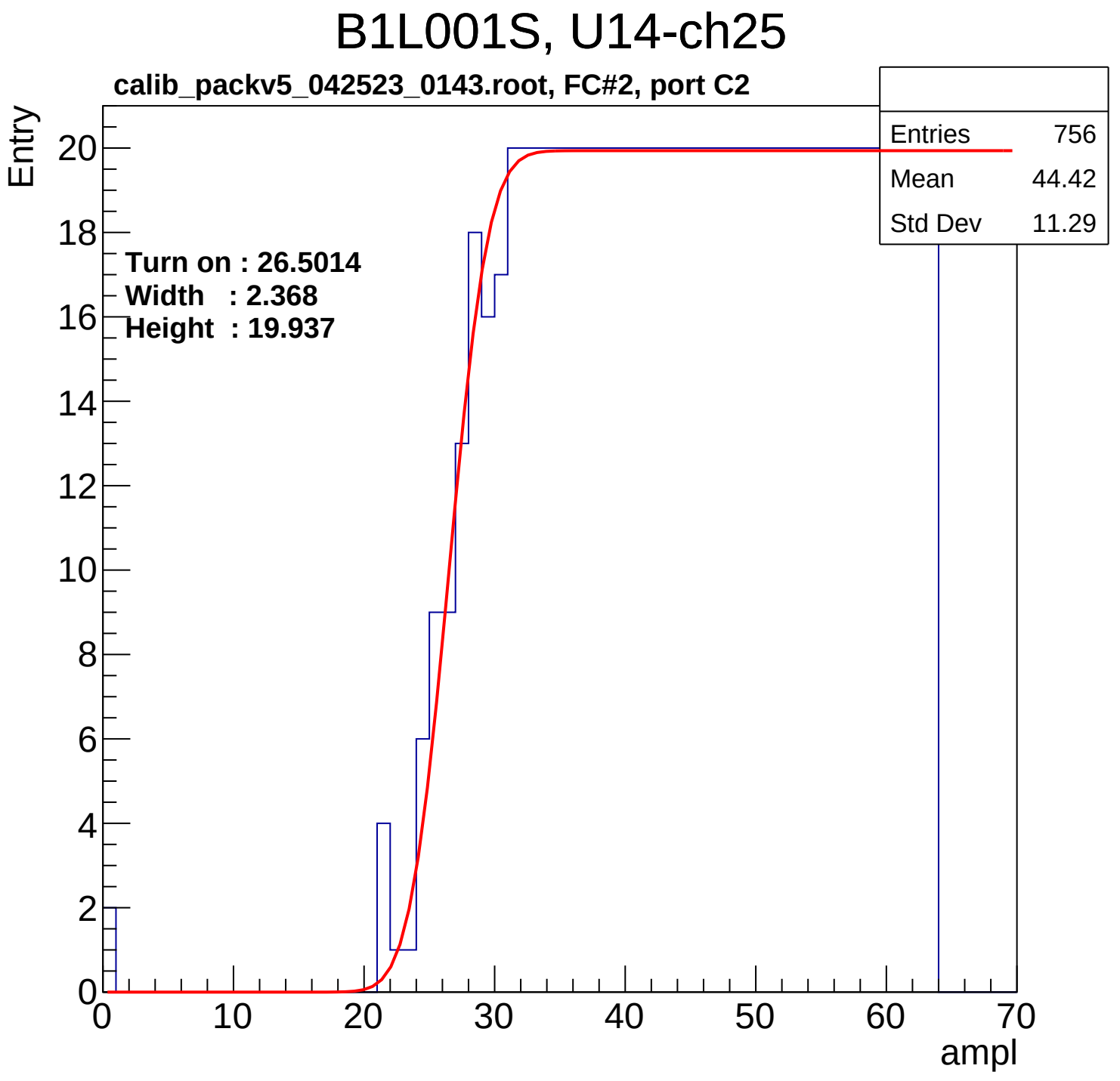

B1L001S, U14-ch20
calib_packv5_042523_0143.root, FC#2, port C2
Entries 771
Mean 43.98
Std Dev 11.72
Turn on : 26.5182
Width : 2.926
Height : 20.120
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

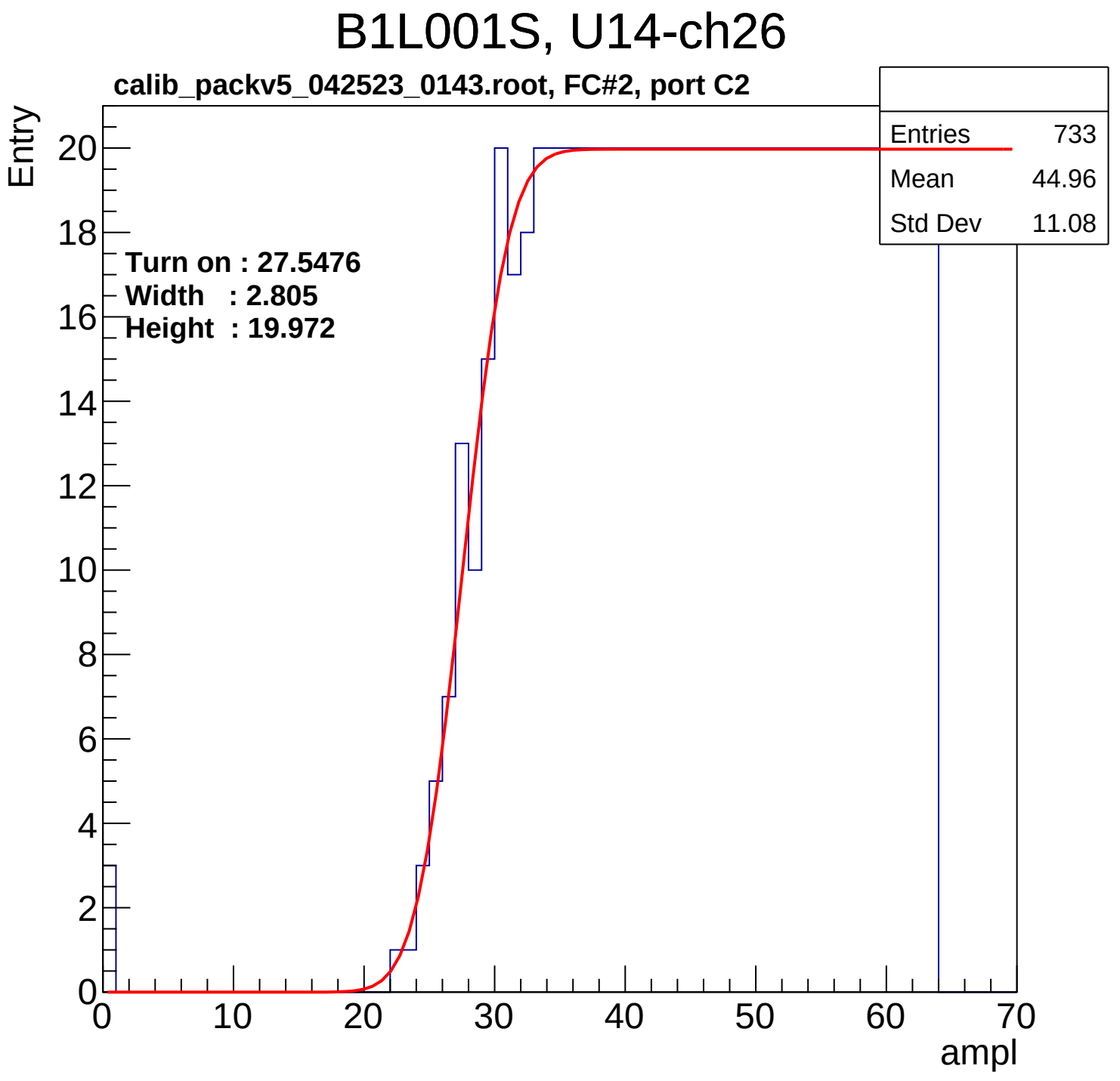

B1L001S, U14-ch21
calib_packv5_042523_0143.root, FC#2, port C2
Entries 728
Mean 44.98
Std Dev 11.26
Turn on : 28.2005
Width : 3.907
Height : 20.150
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

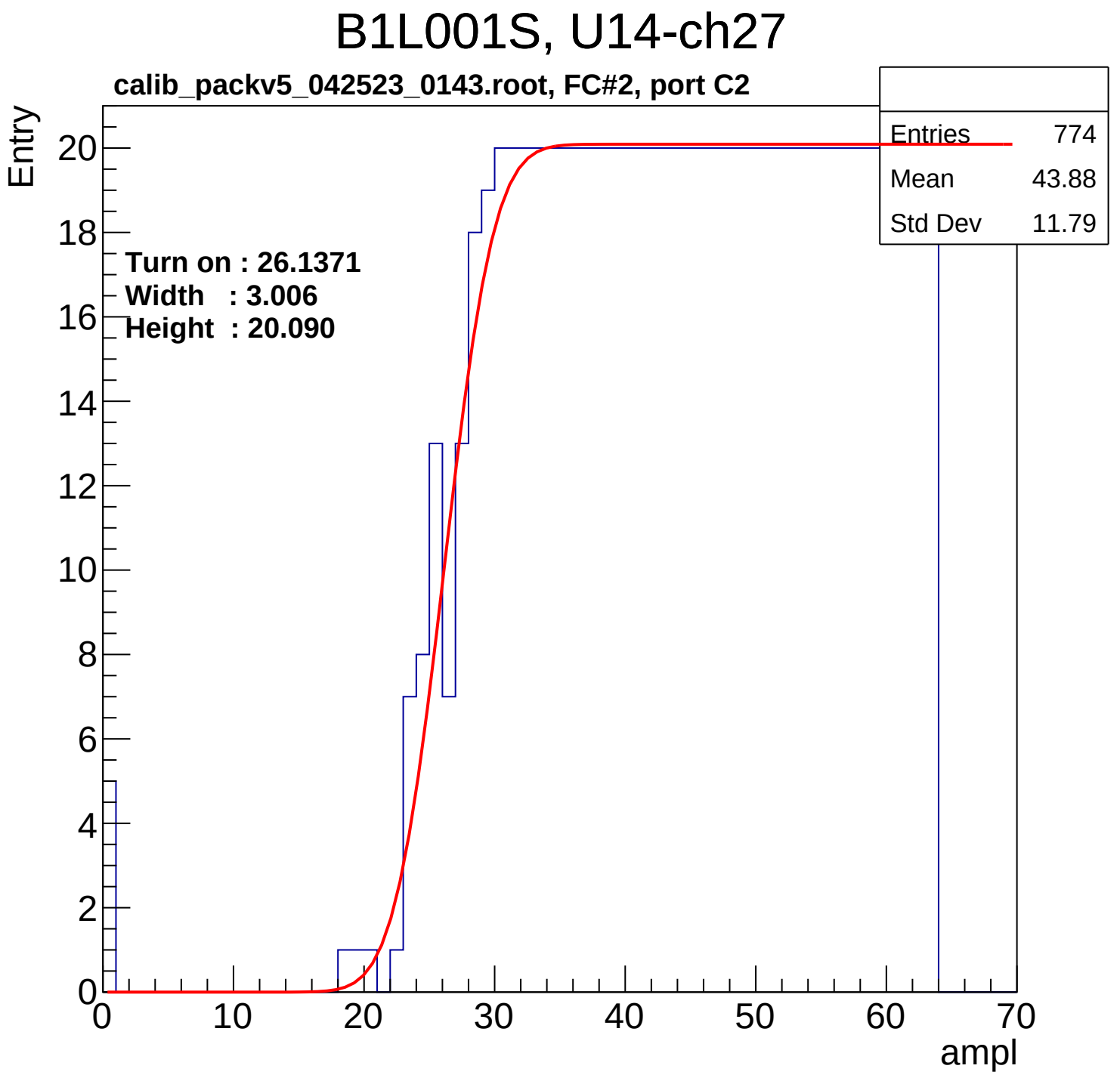

B1L001S, U14-ch22
calib_packv5_042523_0143.root, FC#2, port C2
Entries 760
Mean 44.33
Std Dev 11.33
Turn on : 26.5298
Width : 1.935
Height : 19.933
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

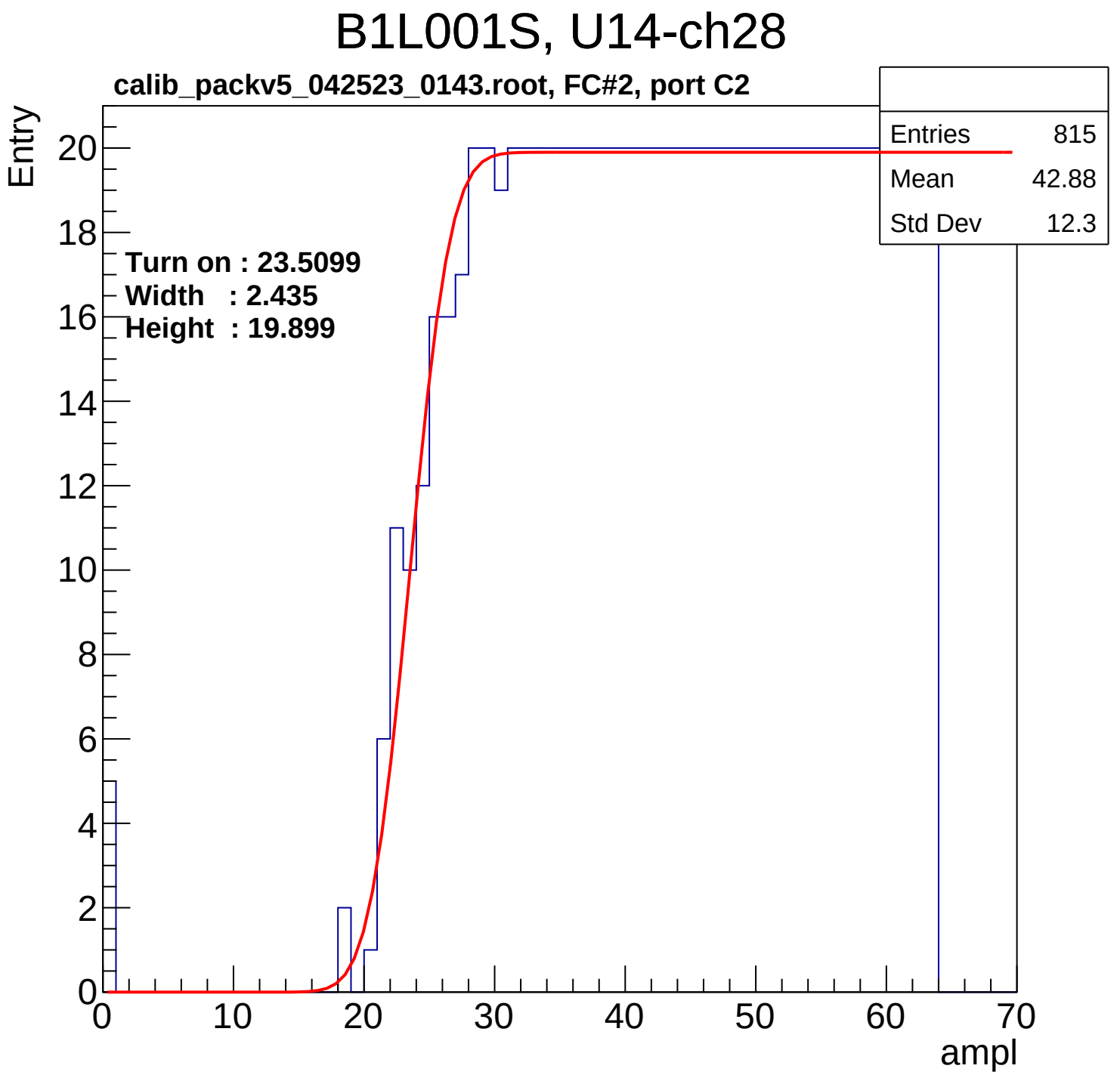

B1L001S, U14-ch23
calib_packv5_042523_0143.root, FC#2, port C2
Entries 753
Mean 44.41
Std Dev 11.46
Turn on : 26.7649
Width : 3.306
Height : 20.044
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

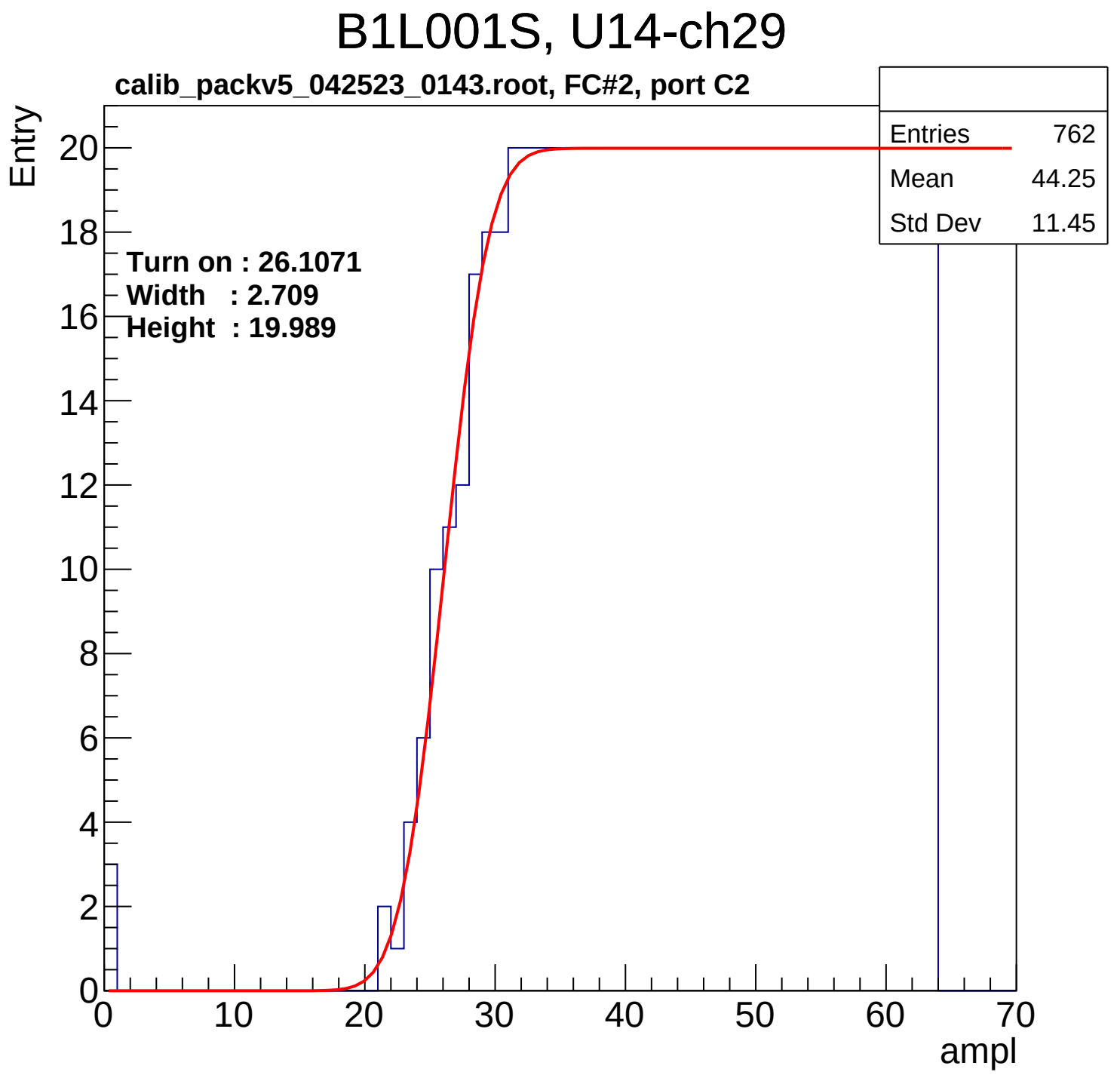

B1L001S, U14-ch24
calib_packv5_042523_0143.root, FC#2, port C2
Entries 742
Mean 44.71
Std Dev 11.23
Turn on : 27.2059
Width : 3.117
Height : 20.016
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

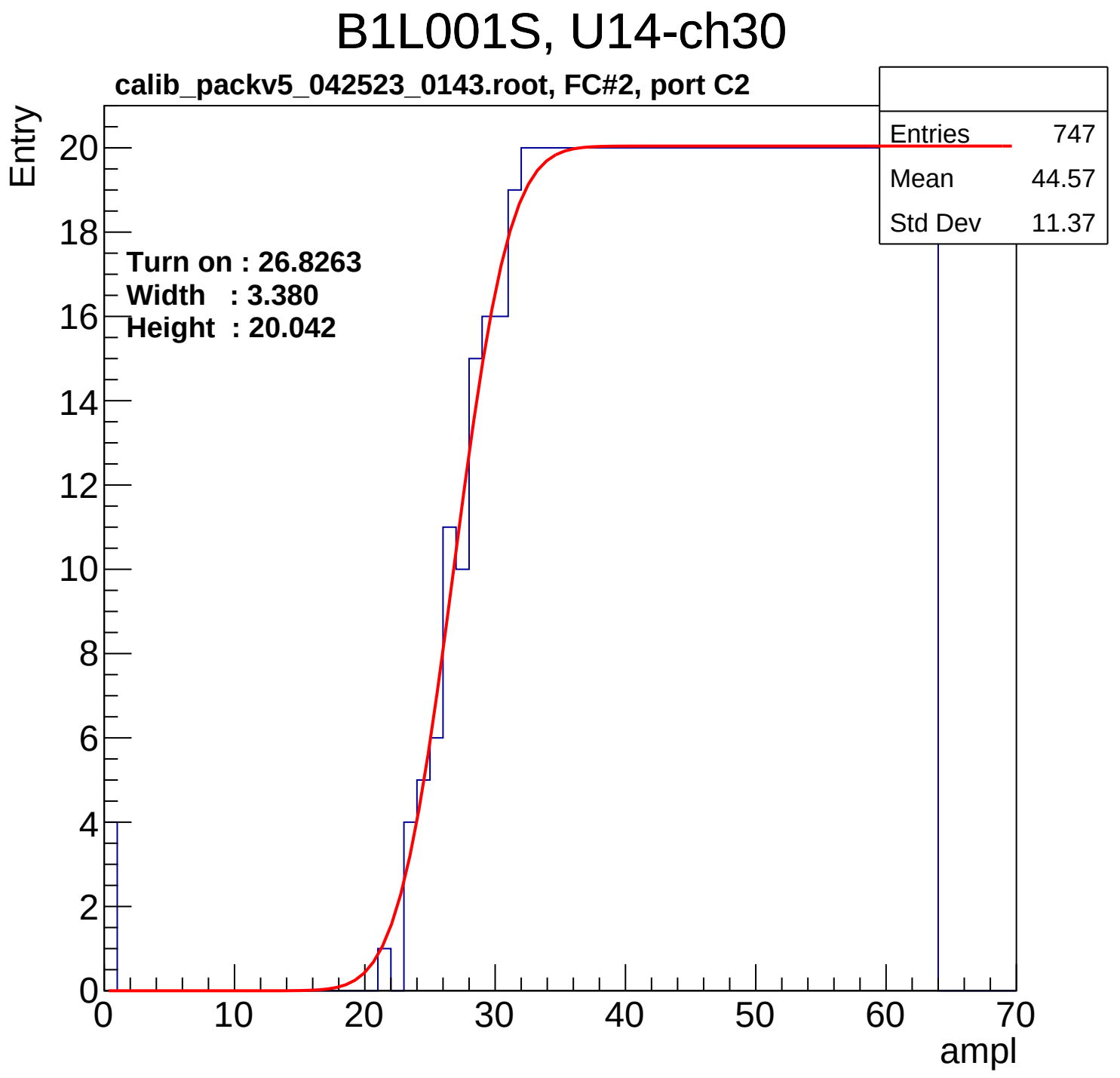

B1L001S, U14-ch25
calib_packv5_042523_0143.root, FC#2, port C2
Entries 756
Mean 44.42
Std Dev 11.29
Turn on : 26.5014
Width : 2.368
Height : 19.937
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

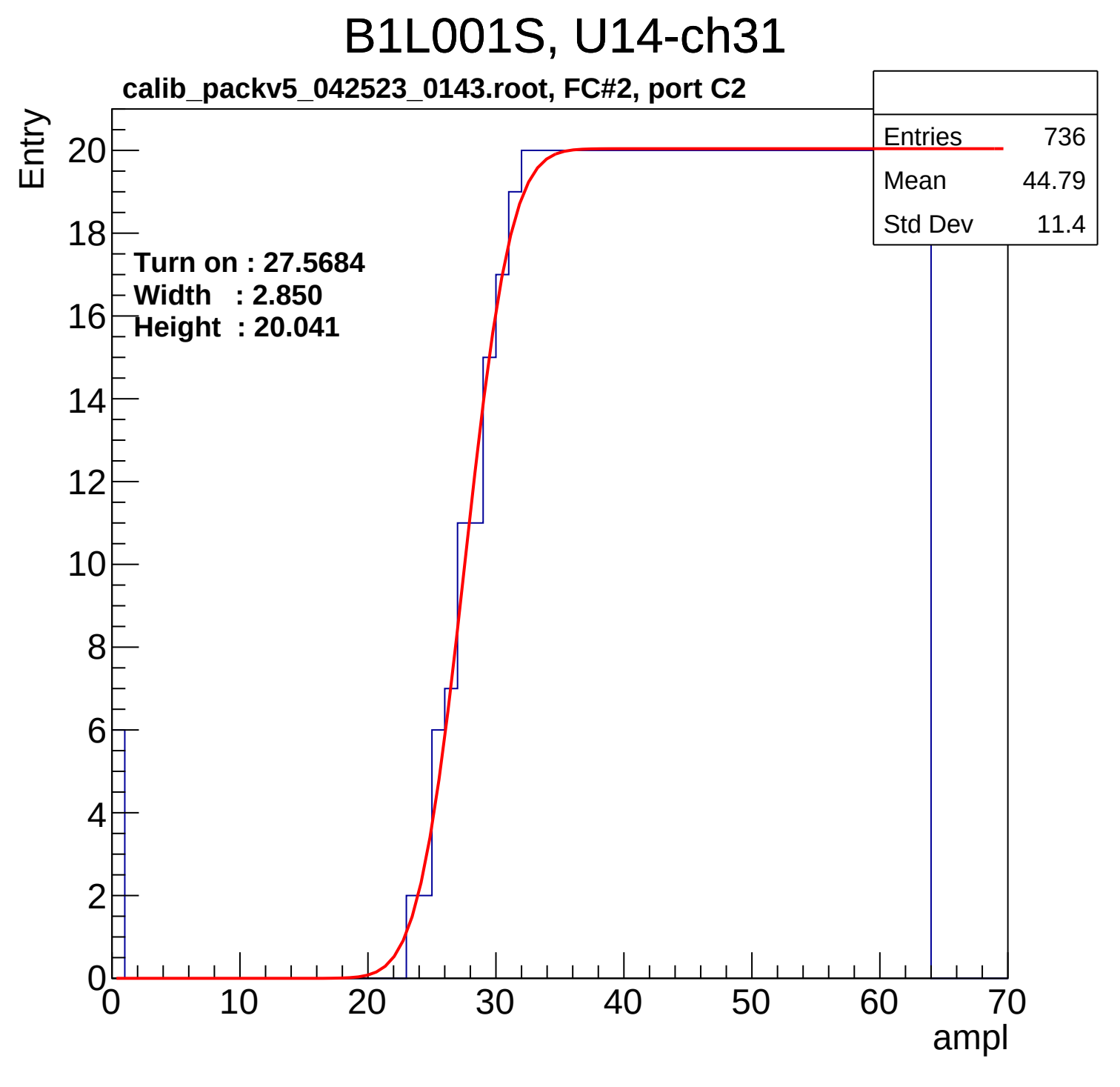

B1L001S, U14-ch26
calib_packv5_042523_0143.root, FC#2, port C2
Entries 733
Mean 44.96
Std Dev 11.08
Turn on : 27.5476
Width : 2.805
Height : 19.972
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

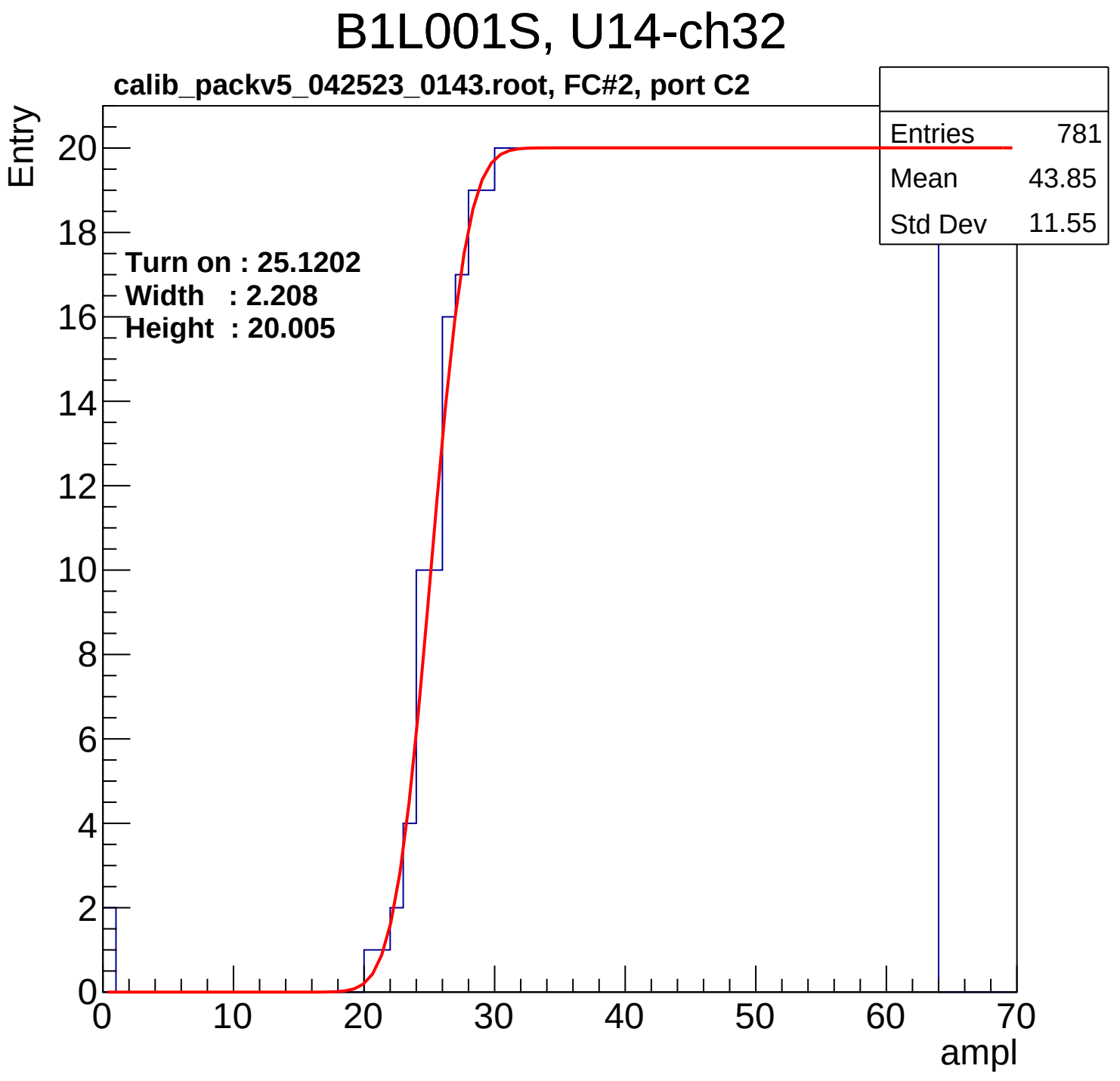

B1L001S, U14-ch27
calib_packv5_042523_0143.root, FC#2, port C2
Entries 774
Mean 43.88
Std Dev 11.79
Turn on : 26.1371
Width : 3.006
Height : 20.090
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

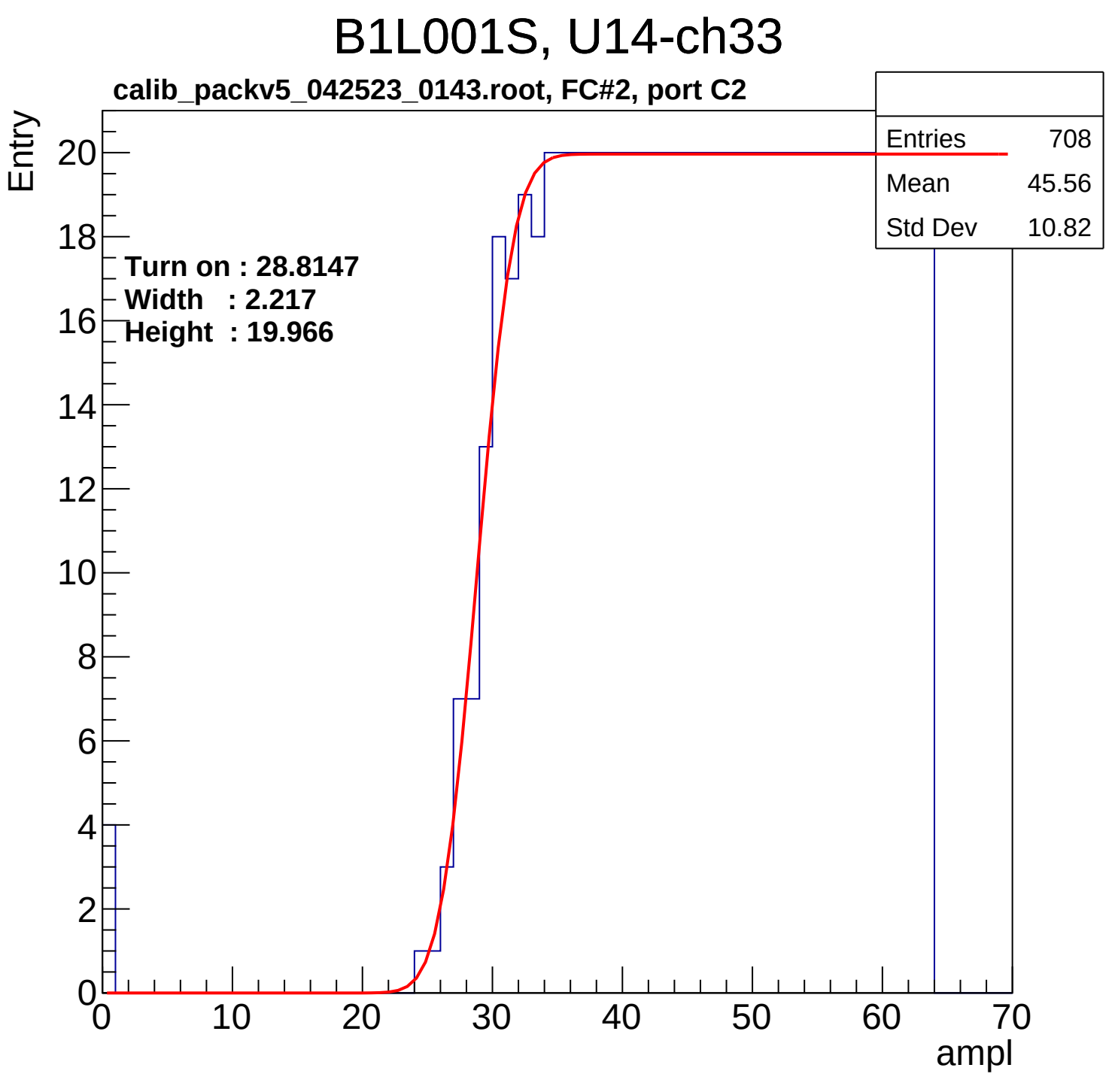

B1L001S, U14-ch28
calib_packv5_042523_0143.root, FC#2, port C2
Entries 815
Mean 42.88
Std Dev 12.3
Turn on : 23.5099
Width : 2.435
Height : 19.899
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

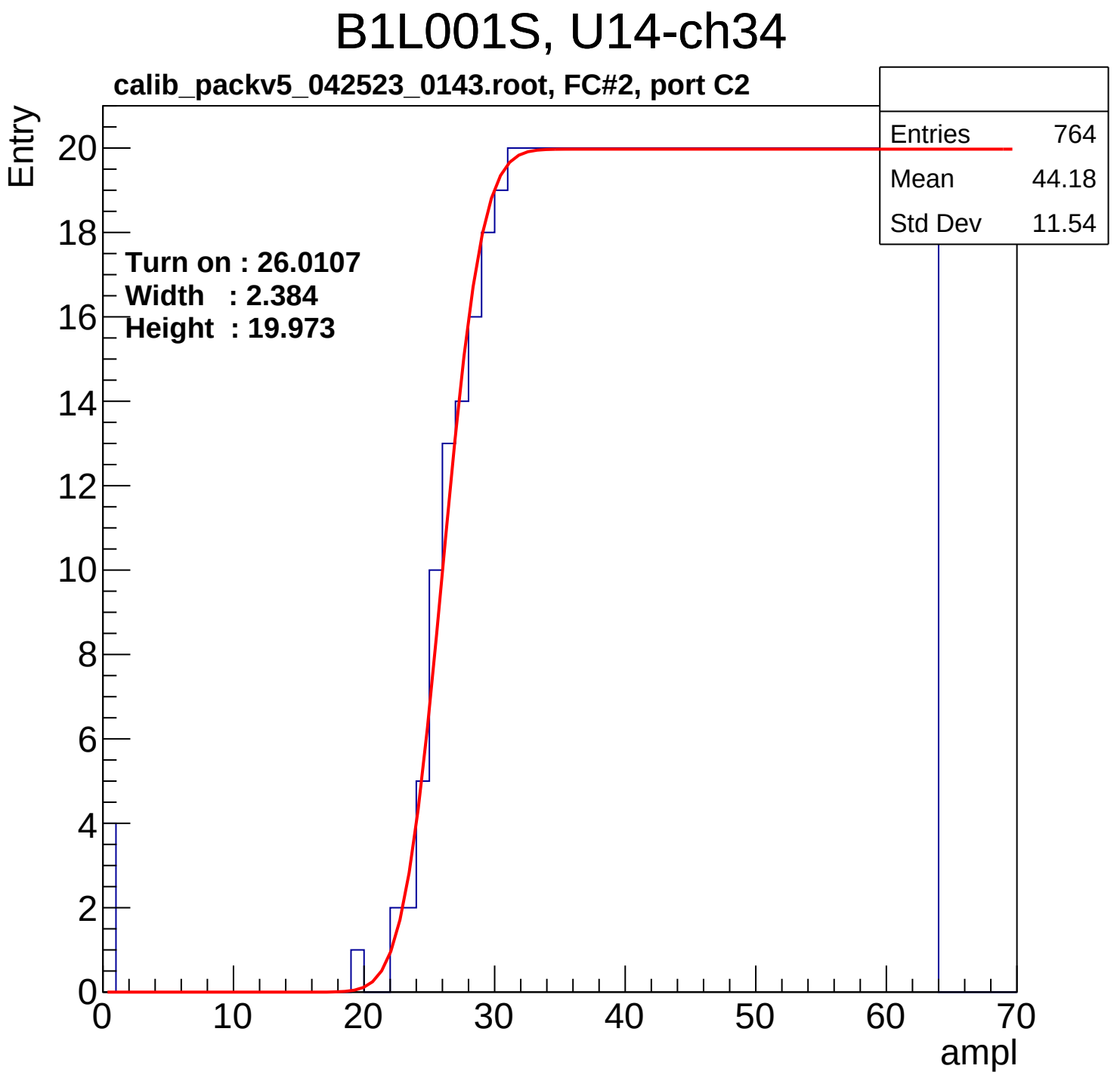

B1L001S, U14-ch29
calib_packv5_042523_0143.root, FC#2, port C2
Entries 762
Mean 44.25
Std Dev 11.45
Turn on : 26.1071
Width : 2.709
Height : 19.989
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

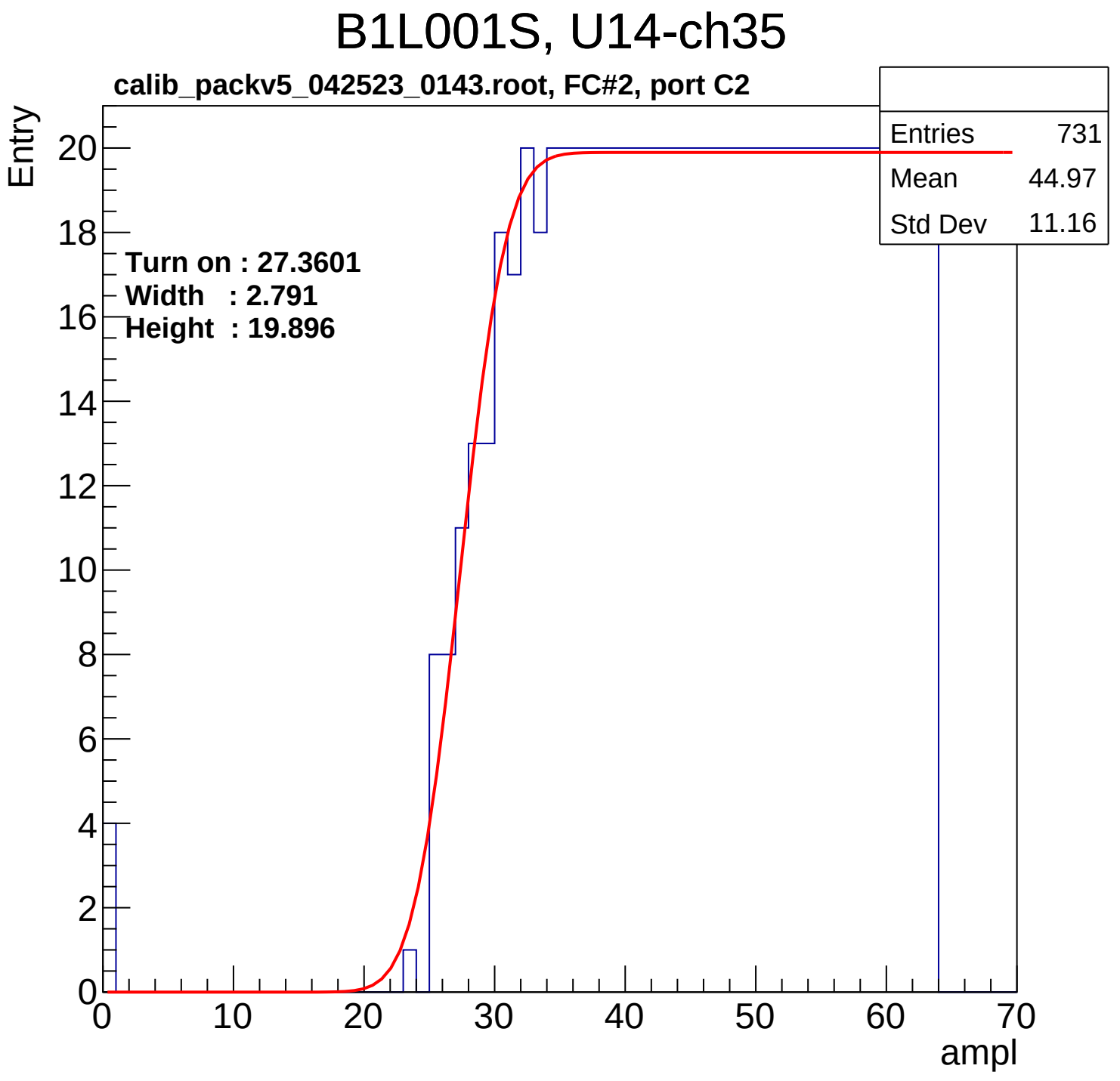

B1L001S, U14-ch30
calib_packv5_042523_0143.root, FC#2, port C2
Entries 747
Mean 44.57
Std Dev 11.37
Turn on : 26.8263
Width : 3.380
Height : 20.042
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

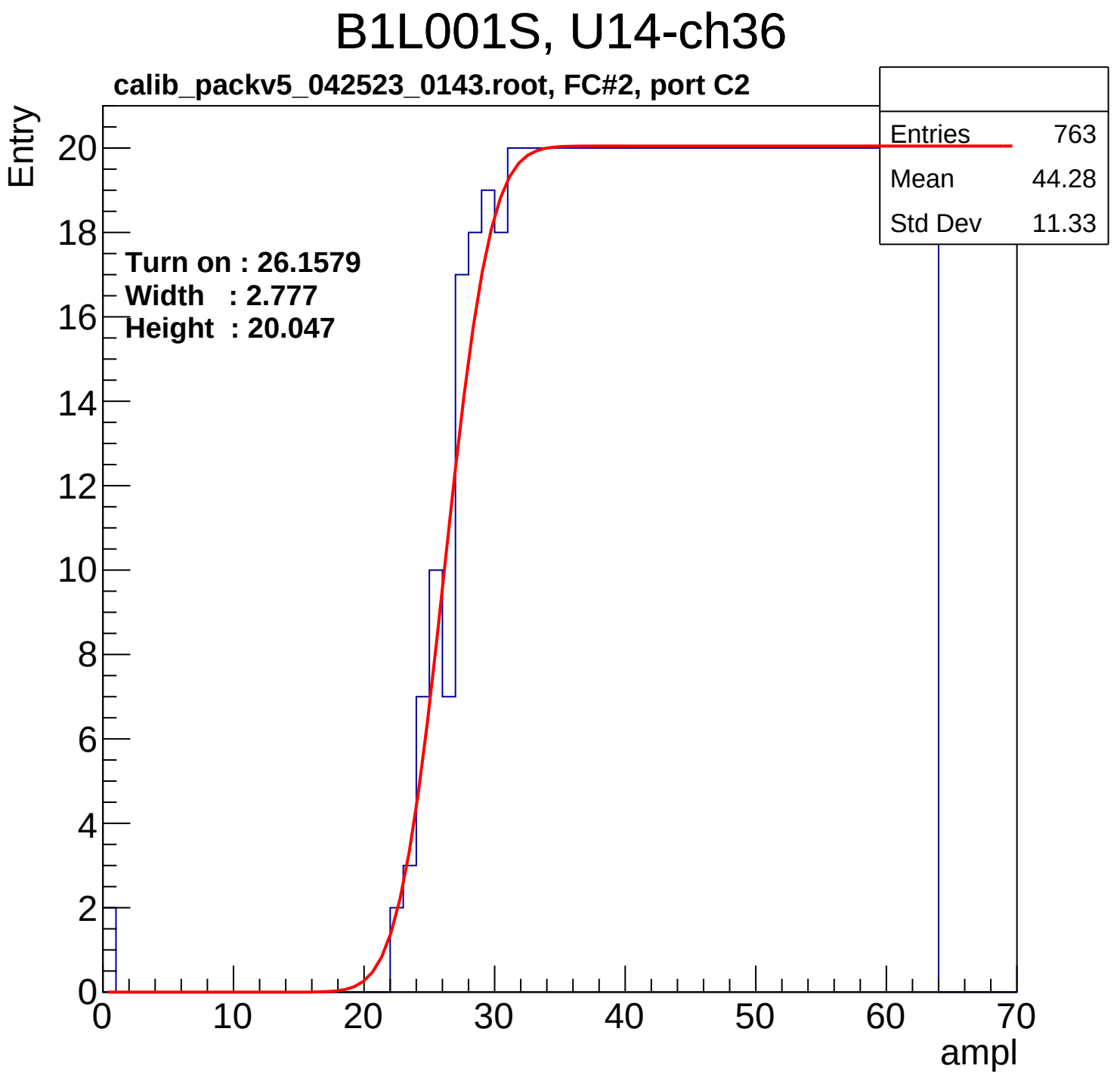

B1L001S, U14-ch31
calib_packv5_042523_0143.root, FC#2, port C2
Entries 736
Mean 44.79
Std Dev 11.4
Turn on : 27.5684
Width : 2.850
Height : 20.041
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

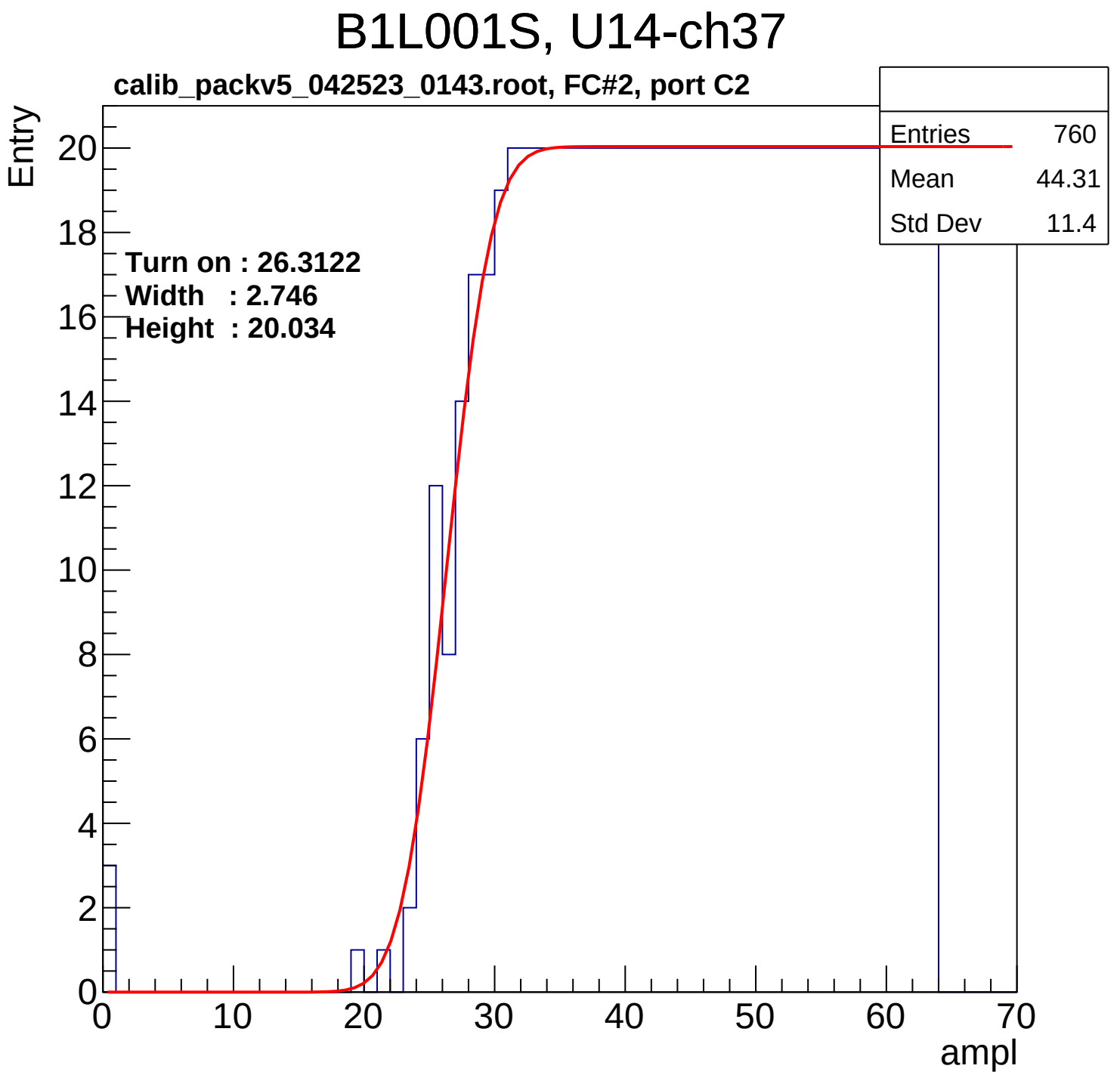

B1L001S, U14-ch32
calib_packv5_042523_0143.root, FC#2, port C2
Entries 781
Mean 43.85
Std Dev 11.55
Turn on : 25.1202
Width : 2.208
Height : 20.005
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

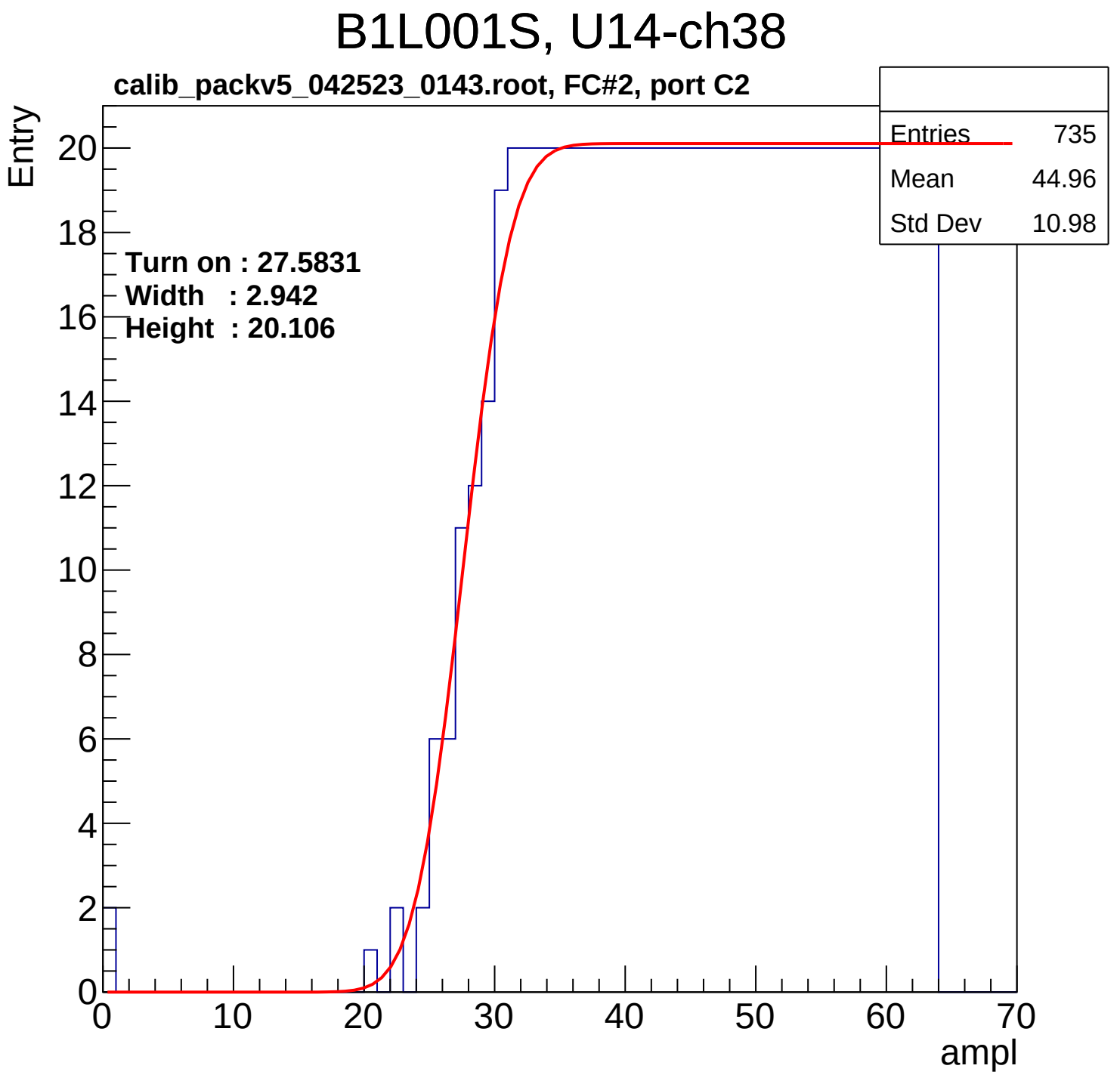

B1L001S, U14-ch33
calib_packv5_042523_0143.root, FC#2, port C2
Entries 708
Mean 45.56
Std Dev 10.82
Turn on : 28.8147
Width : 2.217
Height : 19.966
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

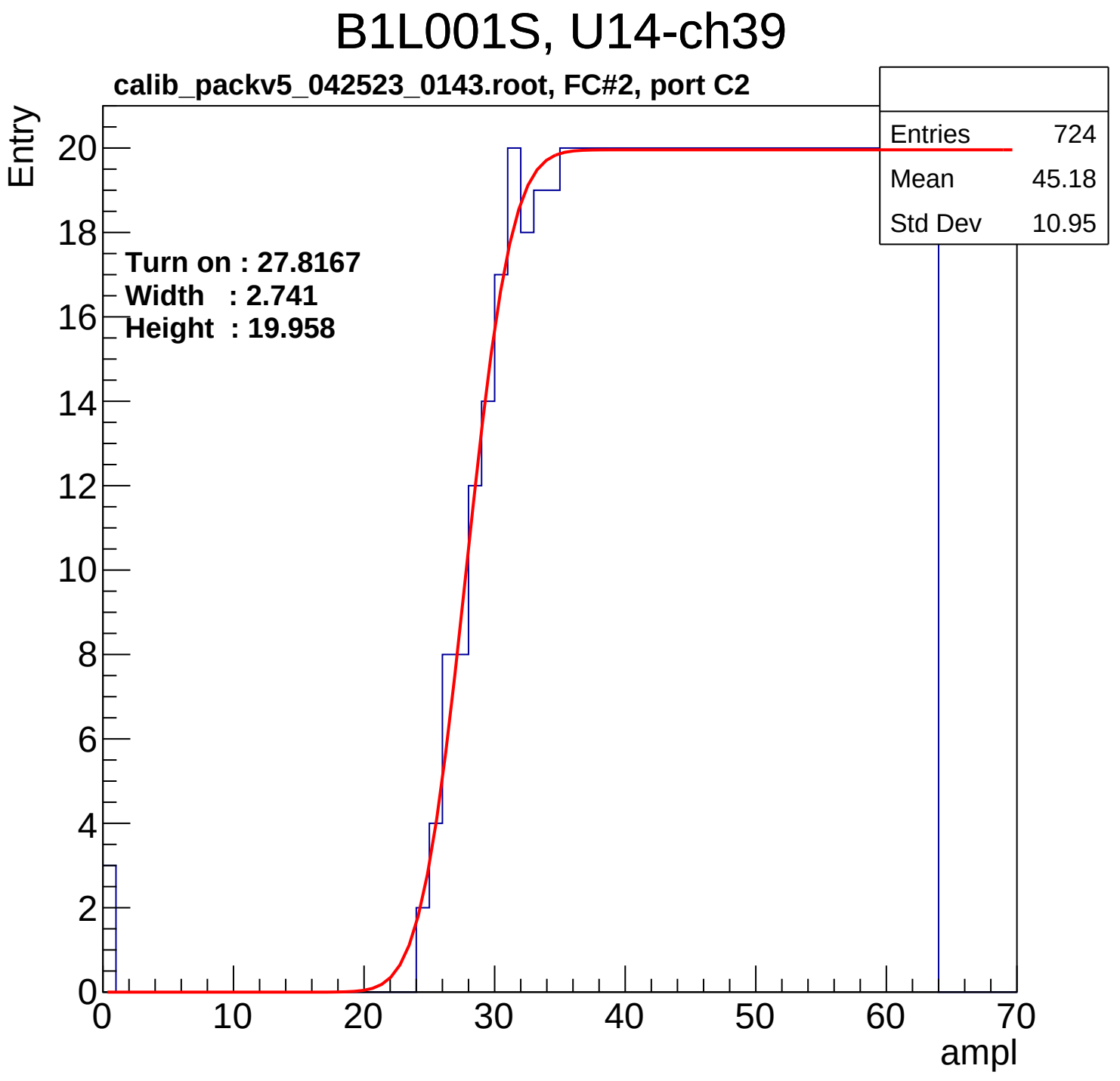

B1L001S, U14-ch34
calib_packv5_042523_0143.root, FC#2, port C2
Entries 764
Mean 44.18
Std Dev 11.54
Turn on : 26.0107
Width : 2.384
Height : 19.973
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

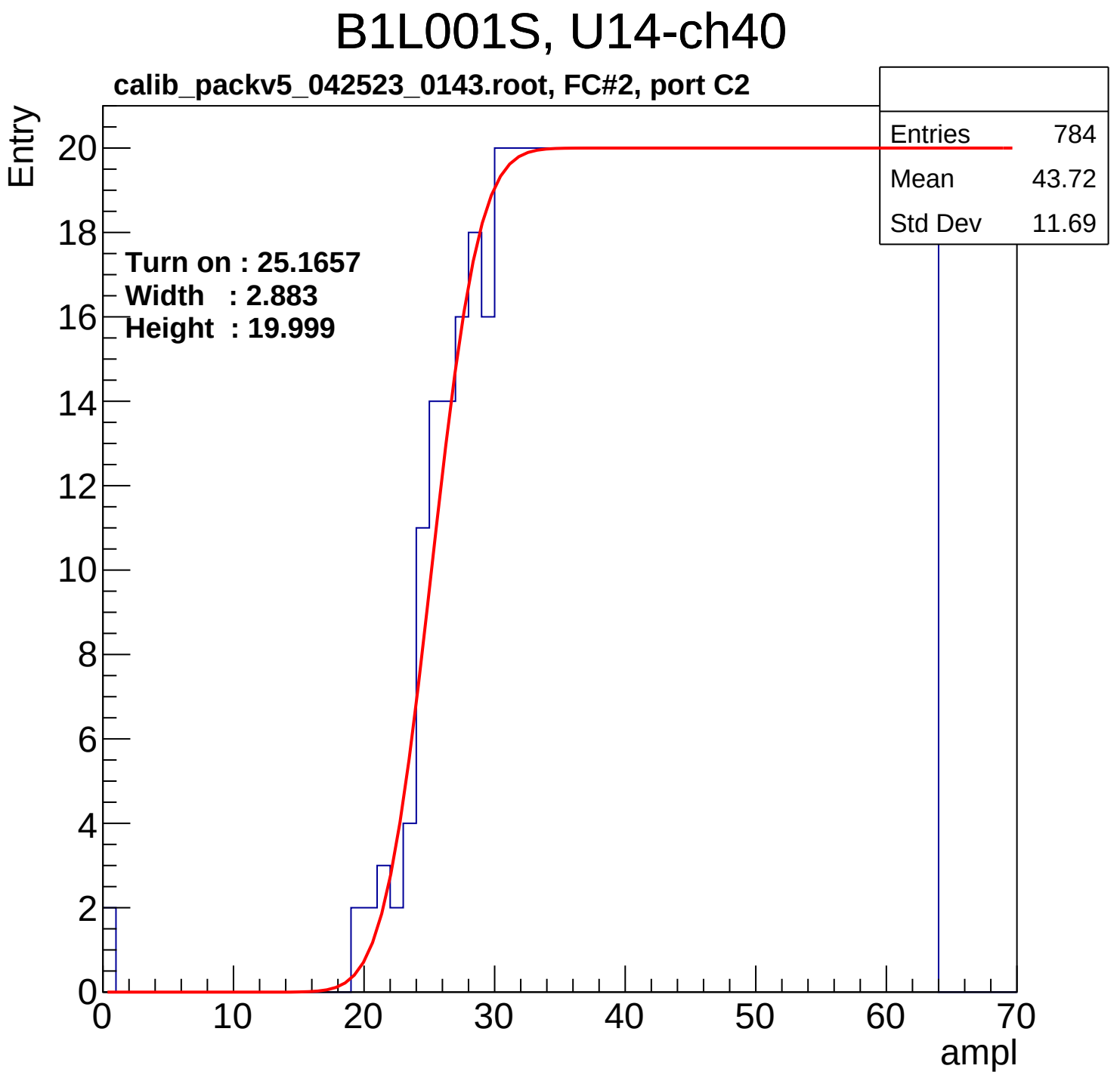

B1L001S, U14-ch35
calib_packv5_042523_0143.root, FC#2, port C2
Entries 731
Mean 44.97
Std Dev 11.16
Turn on : 27.3601
Width : 2.791
Height : 19.896
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

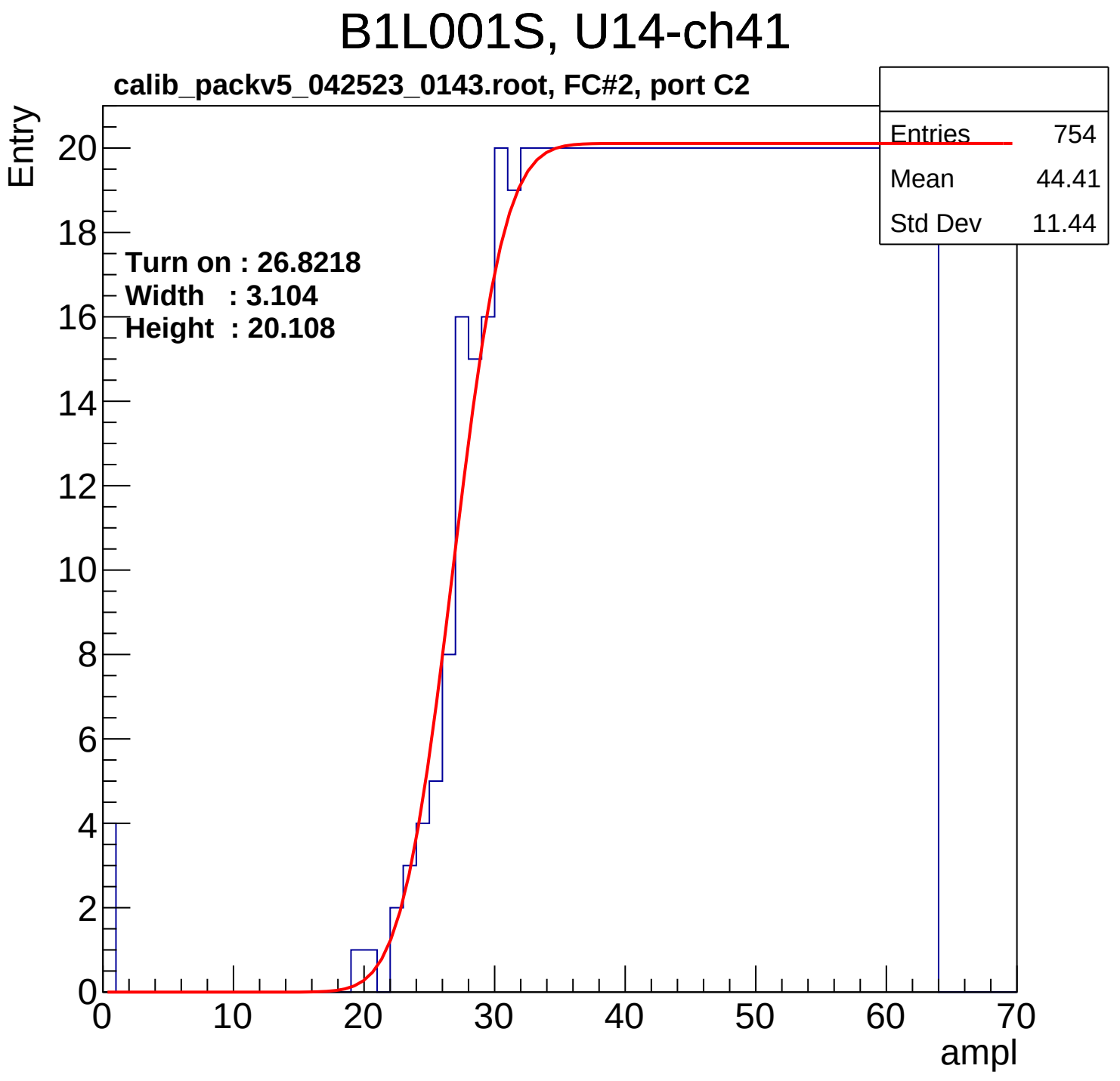

B1L001S, U14-ch36
calib_packv5_042523_0143.root, FC#2, port C2
Entries 763
Mean 44.28
Std Dev 11.33
Turn on : 26.1579
Width : 2.777
Height : 20.047
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

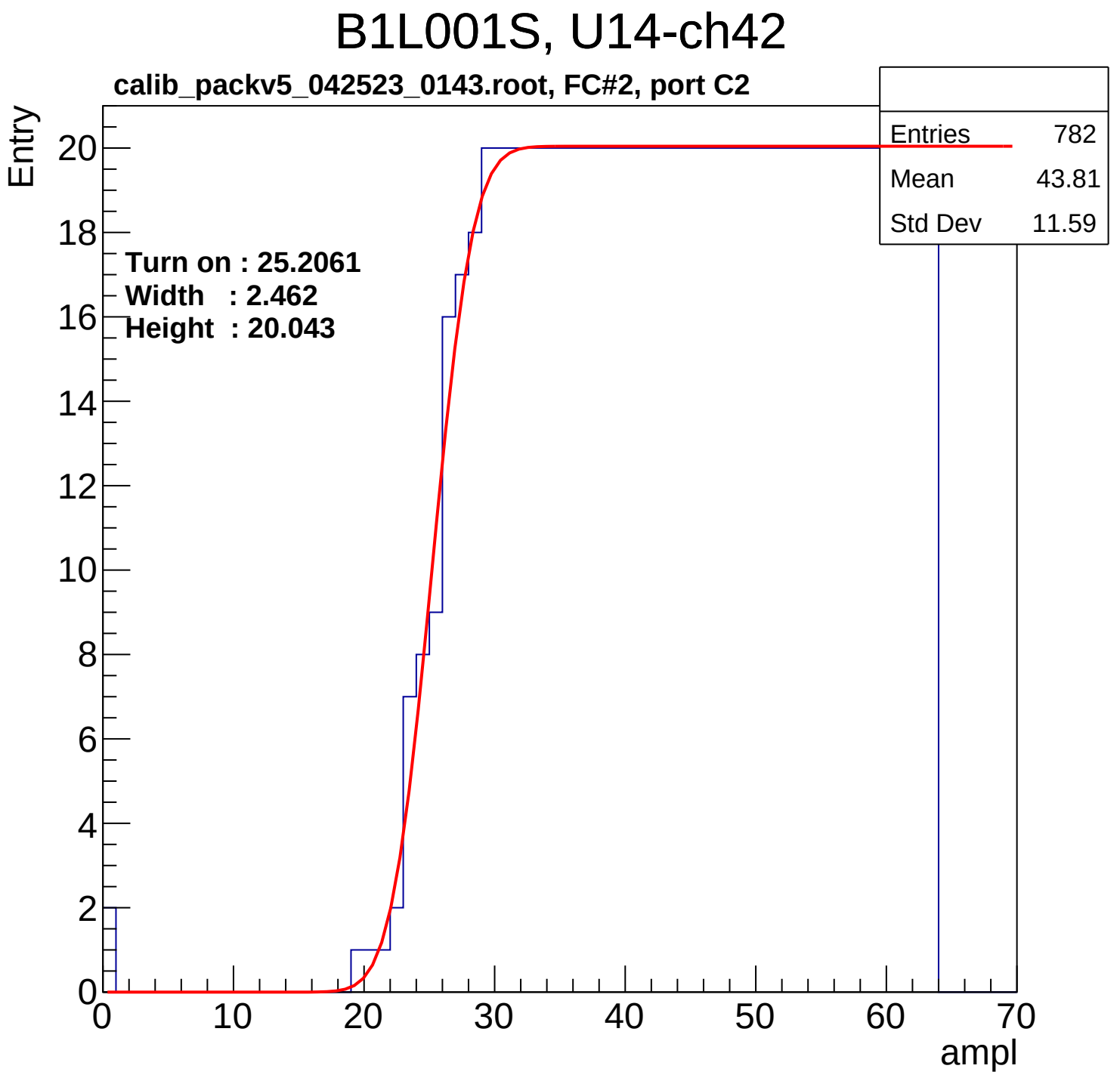

B1L001S, U14-ch37
calib_packv5_042523_0143.root, FC#2, port C2
Entries 760
Mean 44.31
Std Dev 11.4
Turn on : 26.3122
Width : 2.746
Height : 20.034
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

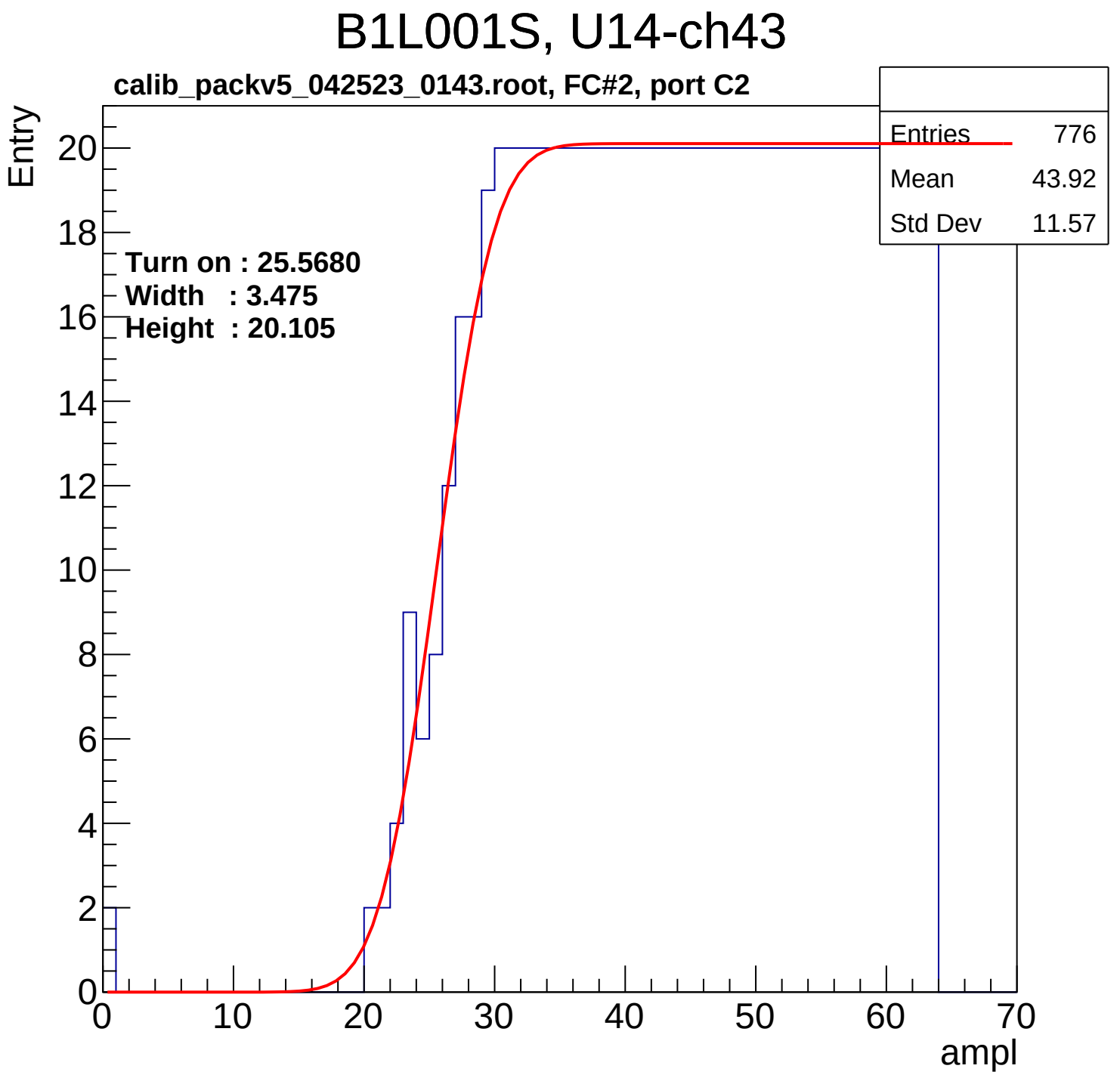

B1L001S, U14-ch38
calib_packv5_042523_0143.root, FC#2, port C2
Entries 735
Mean 44.96
Std Dev 10.98
Turn on : 27.5831
Width : 2.942
Height : 20.106
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

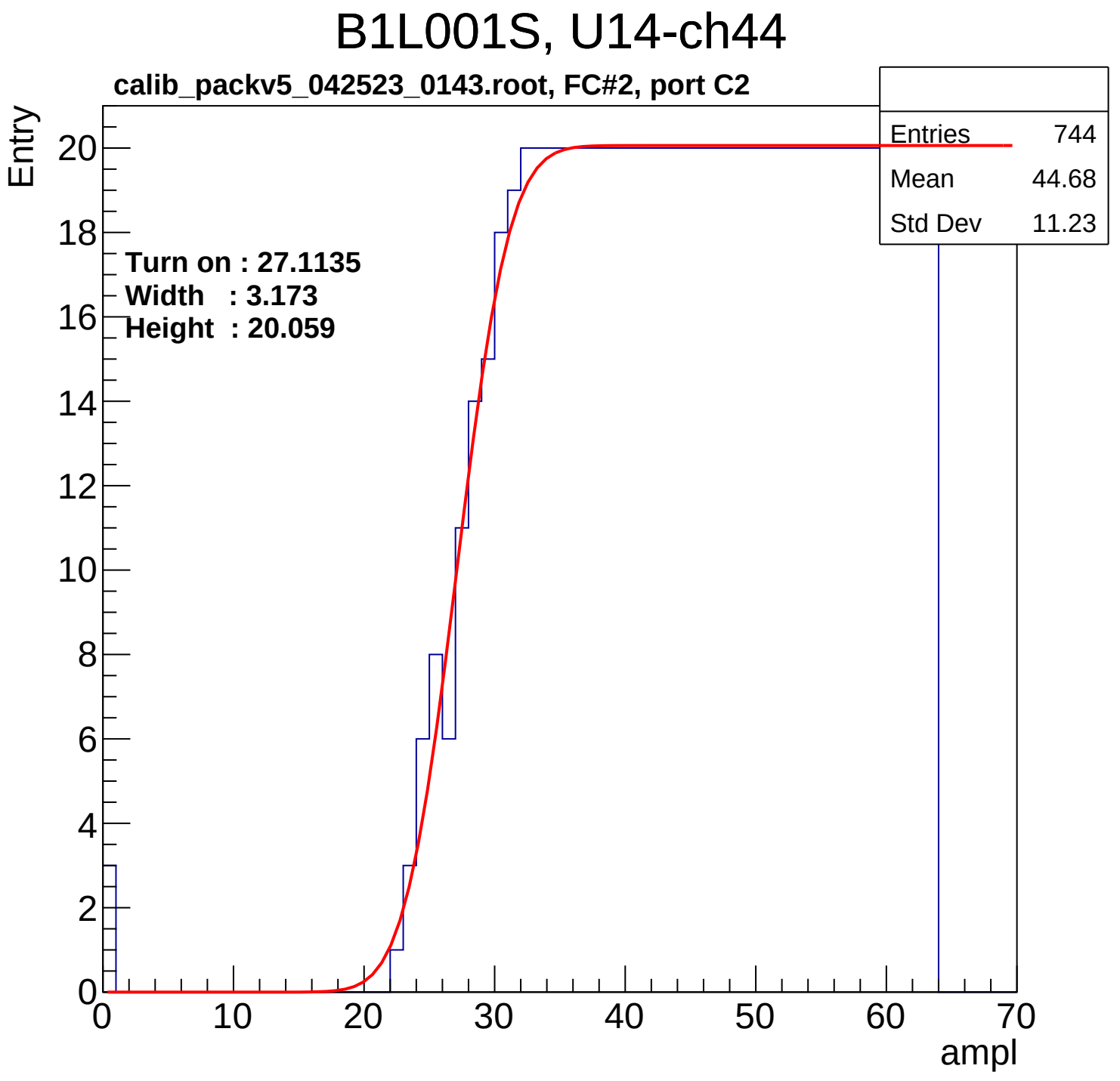

B1L001S, U14-ch39
calib_packv5_042523_0143.root, FC#2, port C2
Entries 724
Mean 45.18
Std Dev 10.95
Turn on : 27.8167
Width : 2.741
Height : 19.958
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

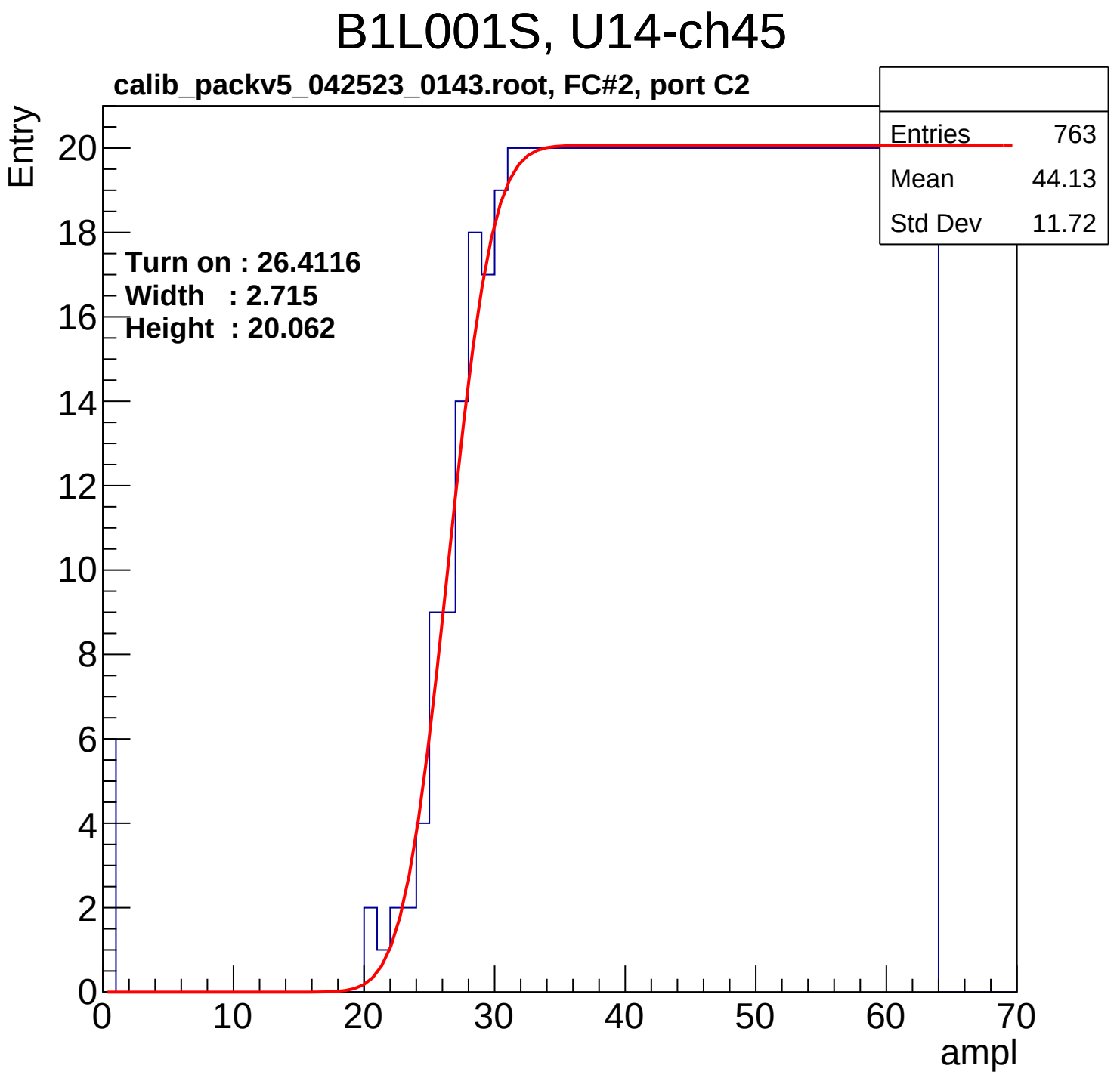

B1L001S, U14-ch40
calib_packv5_042523_0143.root, FC#2, port C2
Entries 784
Mean 43.72
Std Dev 11.69
Turn on : 25.1657
Width : 2.883
Height : 19.999
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

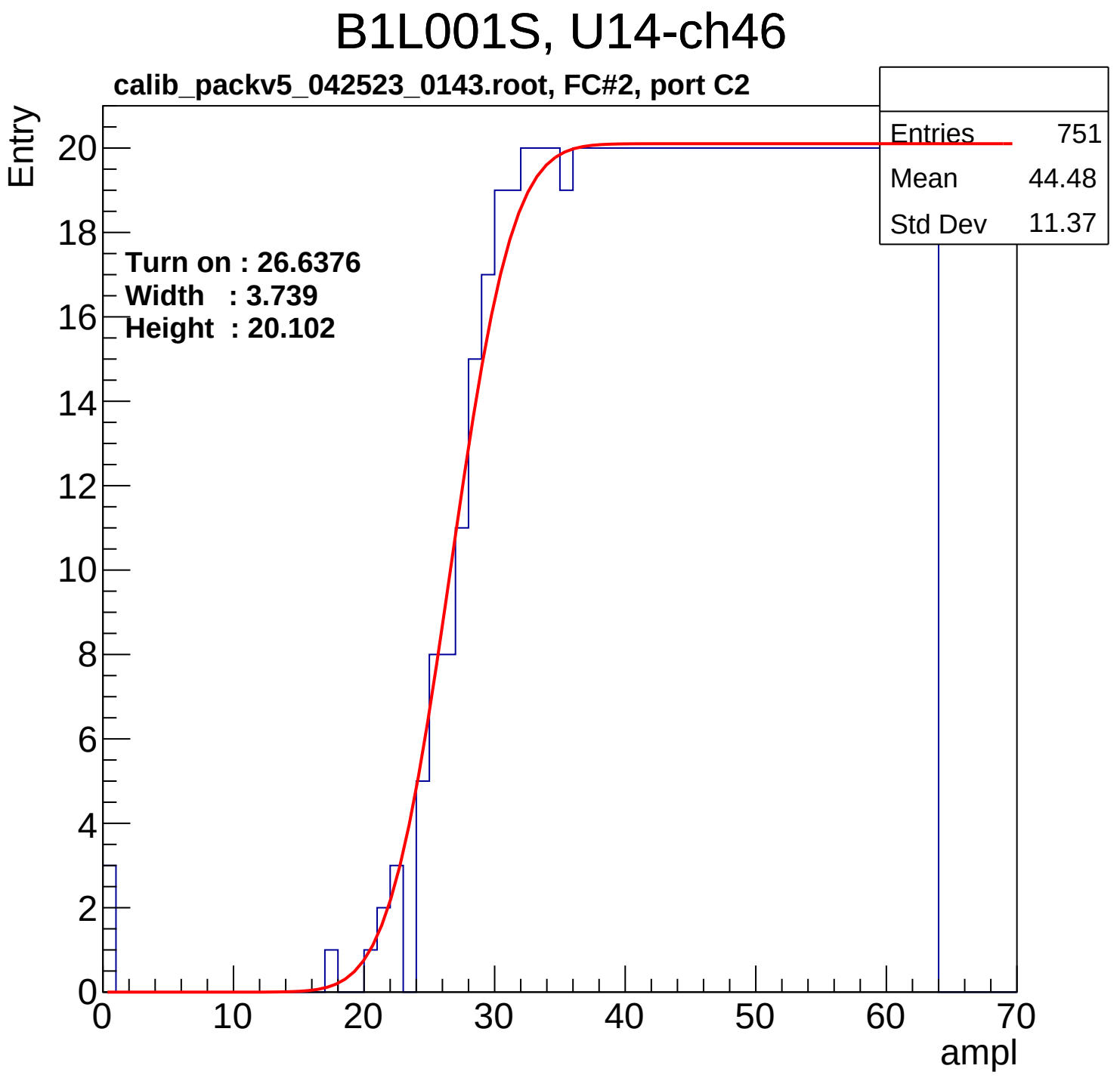

B1L001S, U14-ch41
calib_packv5_042523_0143.root, FC#2, port C2
Entries 754
Mean 44.41
Std Dev 11.44
Turn on : 26.8218
Width : 3.104
Height : 20.108
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

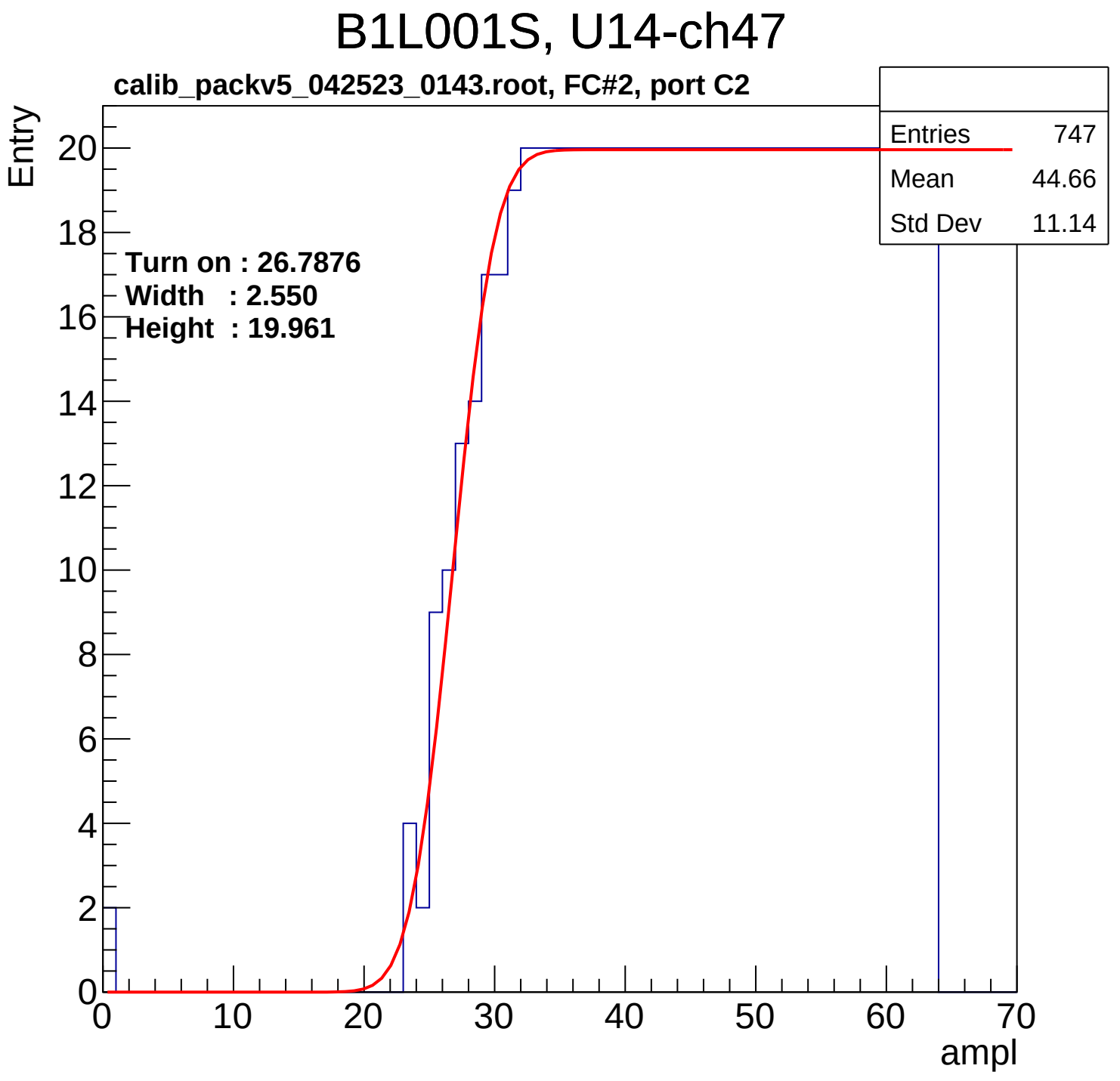

B1L001S, U14-ch42
calib_packv5_042523_0143.root, FC#2, port C2
Entries 782
Mean 43.81
Std Dev 11.59
Turn on : 25.2061
Width : 2.462
Height : 20.043
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

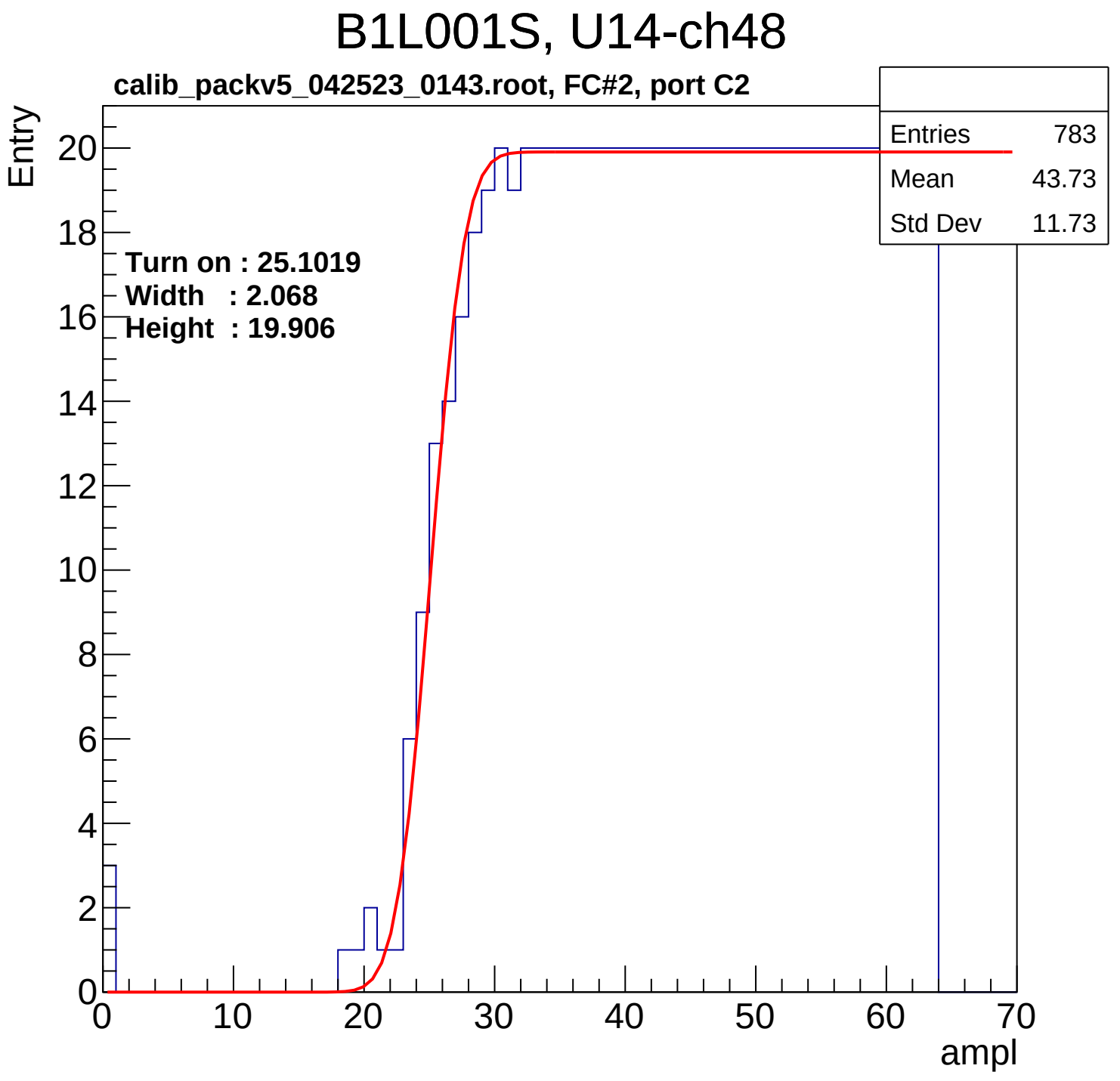

B1L001S, U14-ch43
calib_packv5_042523_0143.root, FC#2, port C2
Entries 776
Mean 43.92
Std Dev 11.57
Turn on : 25.5680
Width : 3.475
Height : 20.105
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

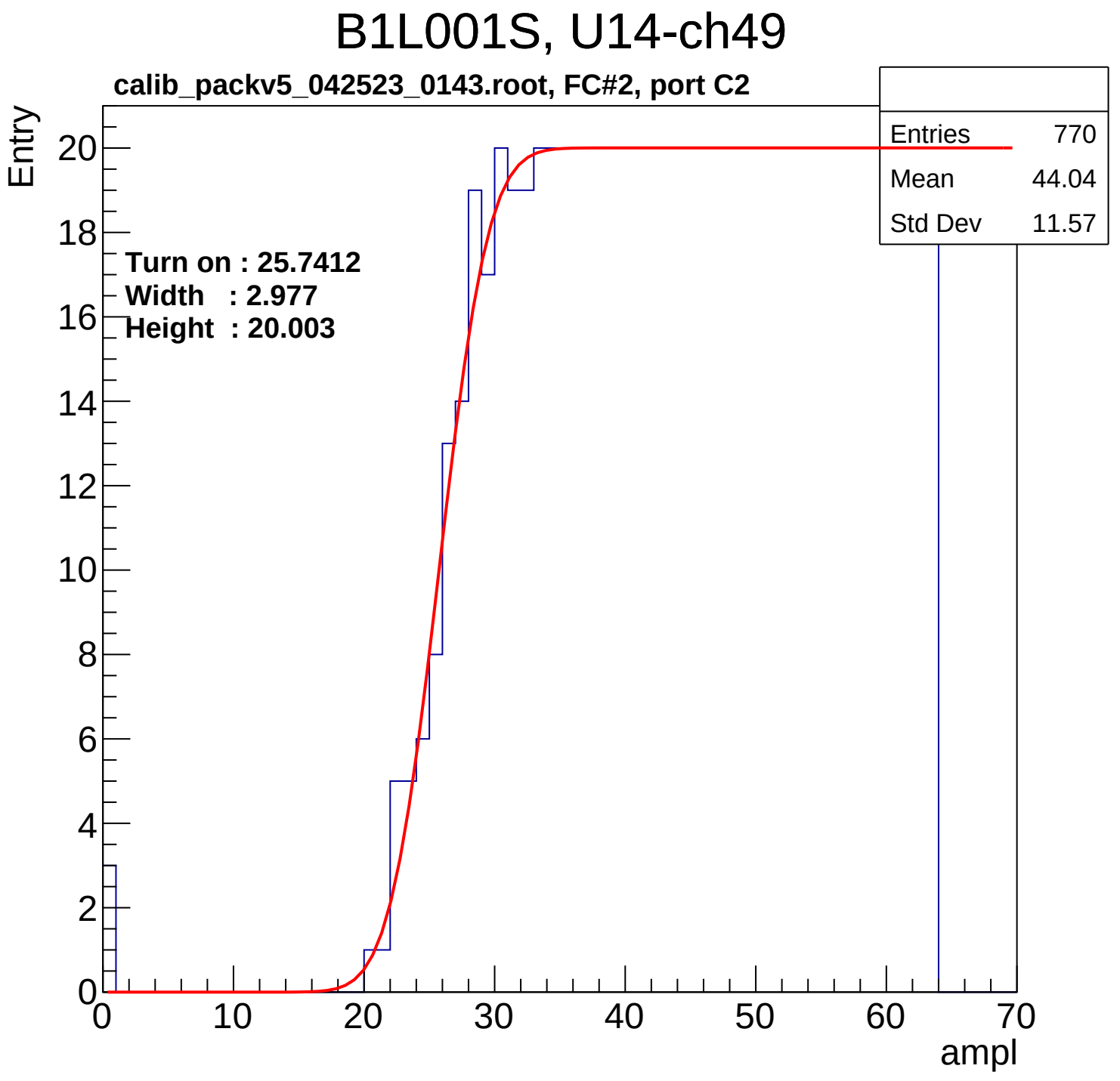

B1L001S, U14-ch44
calib_packv5_042523_0143.root, FC#2, port C2
Entries 744
Mean 44.68
Std Dev 11.23
Turn on : 27.1135
Width : 3.173
Height : 20.059
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

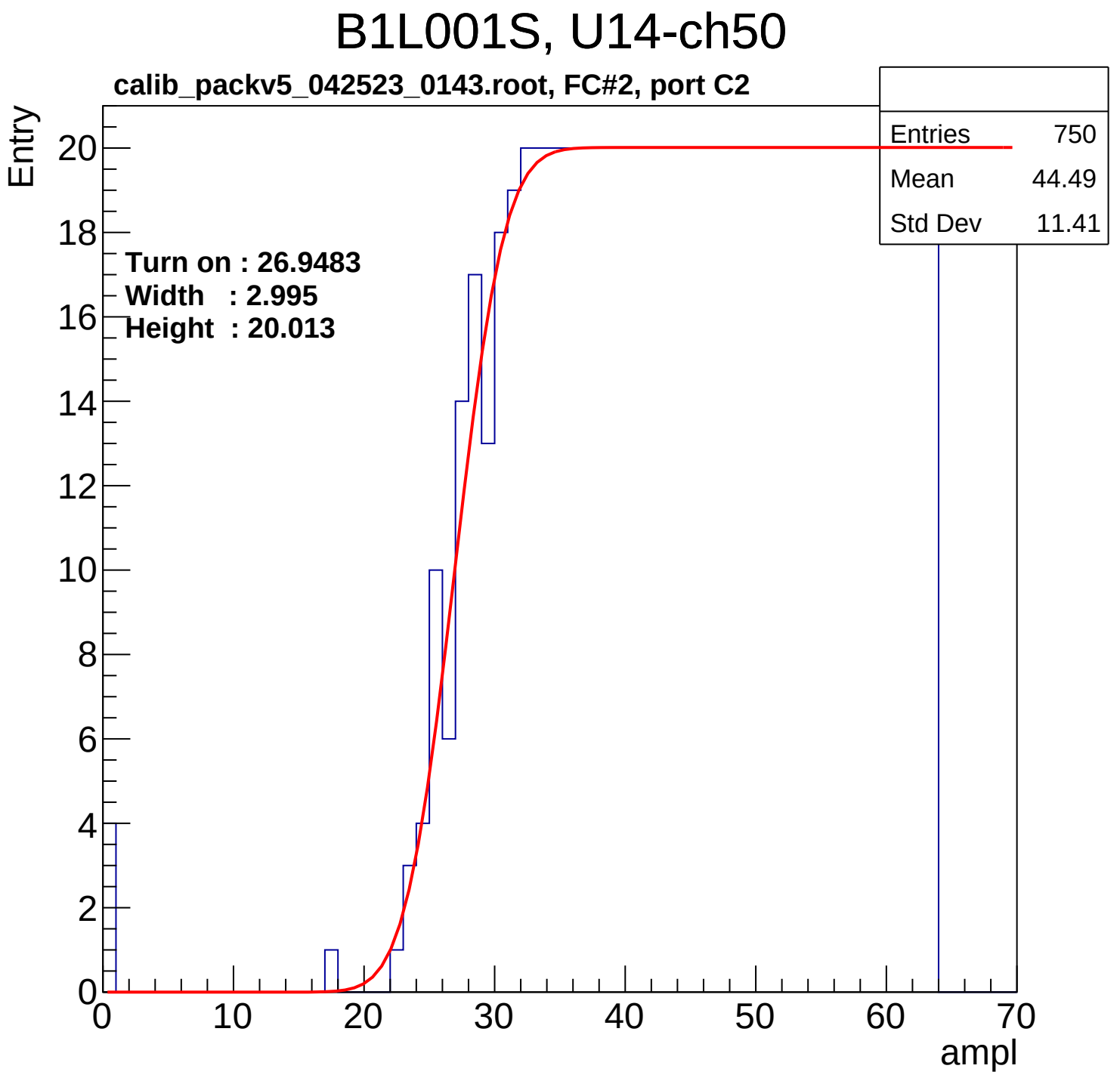

B1L001S, U14-ch45
calib_packv5_042523_0143.root, FC#2, port C2
Entries 763
Mean 44.13
Std Dev 11.72
Turn on : 26.4116
Width : 2.715
Height : 20.062
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

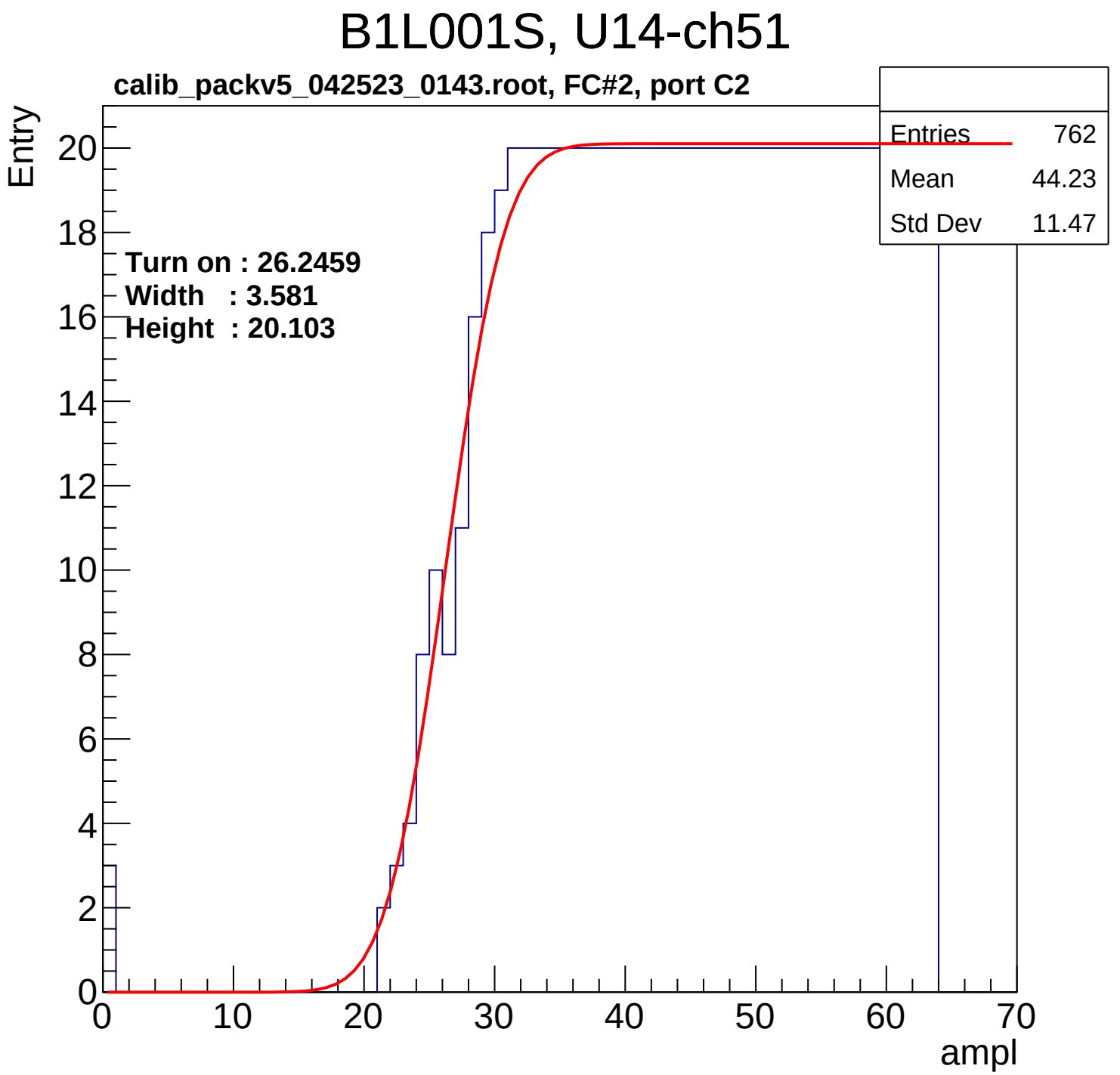

B1L001S, U14-ch46
calib_packv5_042523_0143.root, FC#2, port C2
Entries 751
Mean 44.48
Std Dev 11.37
Turn on : 26.6376
Width : 3.739
Height : 20.102
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

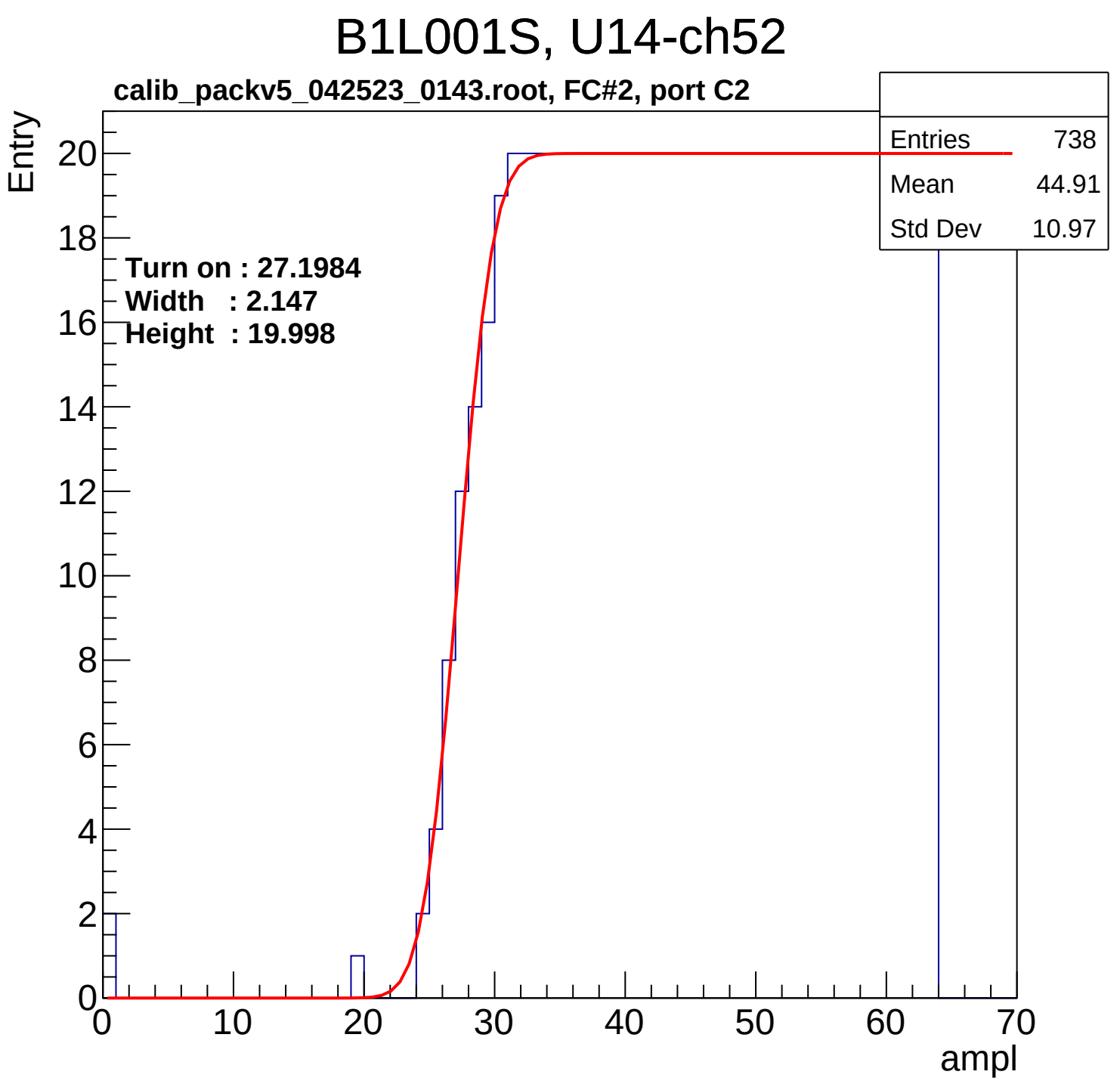

B1L001S, U14-ch47
calib_packv5_042523_0143.root, FC#2, port C2
Entries 747
Mean 44.66
Std Dev 11.14
Turn on : 26.7876
Width : 2.550
Height : 19.961
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

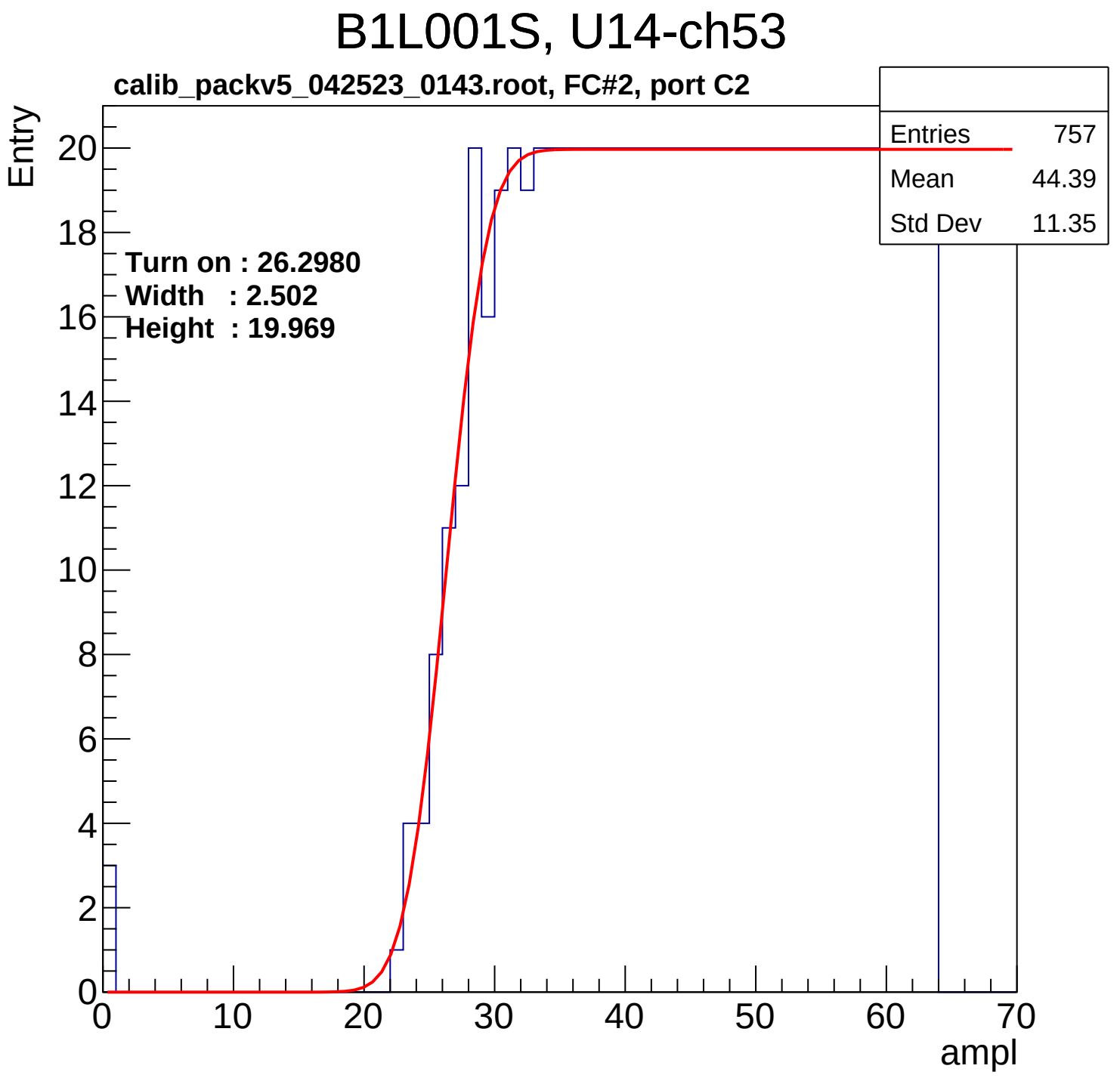

B1L001S, U14-ch48
calib_packv5_042523_0143.root, FC#2, port C2
Entries 783
Mean 43.73
Std Dev 11.73
Turn on : 25.1019
Width : 2.068
Height : 19.906
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

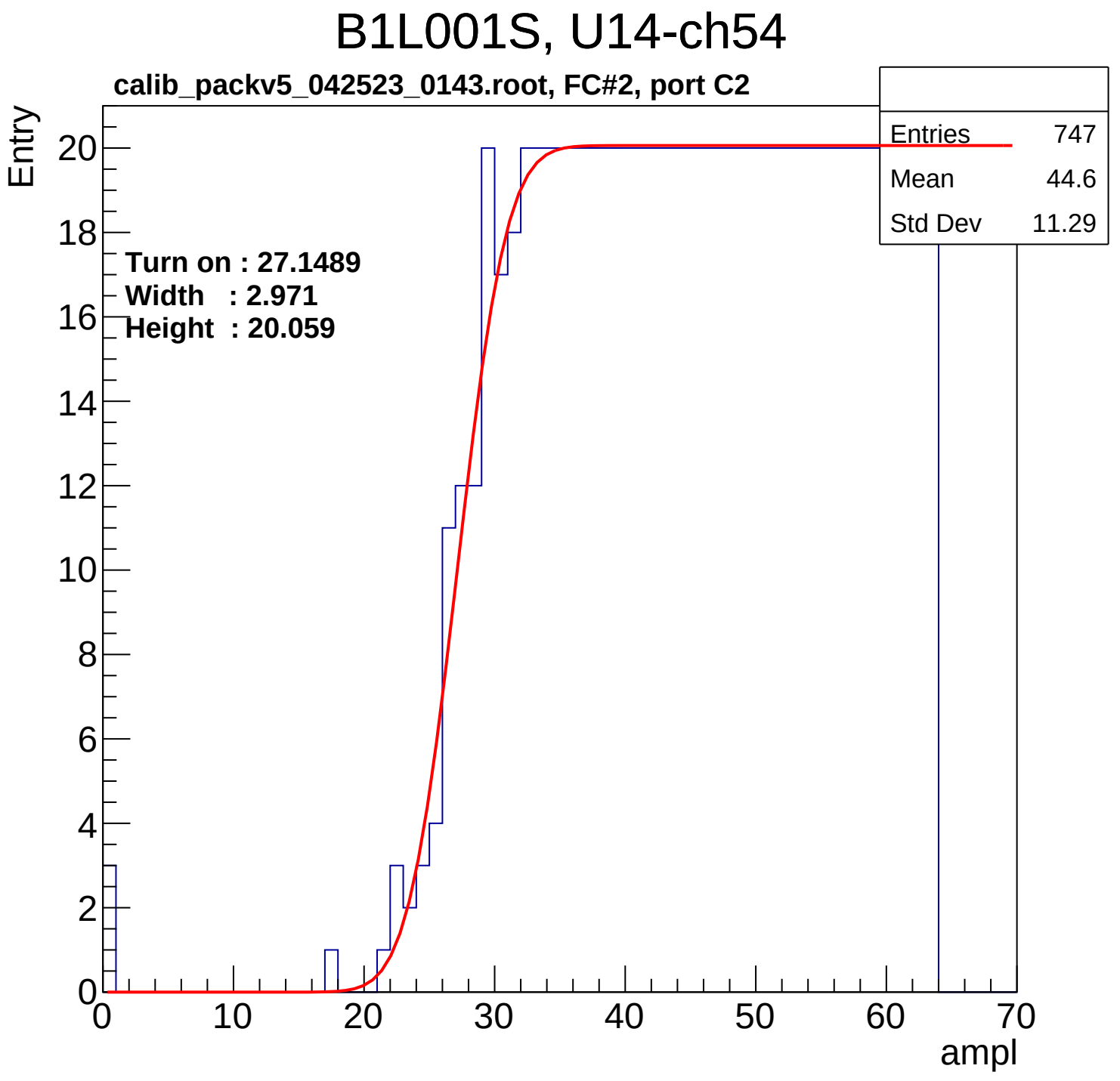

B1L001S, U14-ch49
calib_packv5_042523_0143.root, FC#2, port C2
Entries 770
Mean 44.04
Std Dev 11.57
Turn on : 25.7412
Width : 2.977
Height : 20.003
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

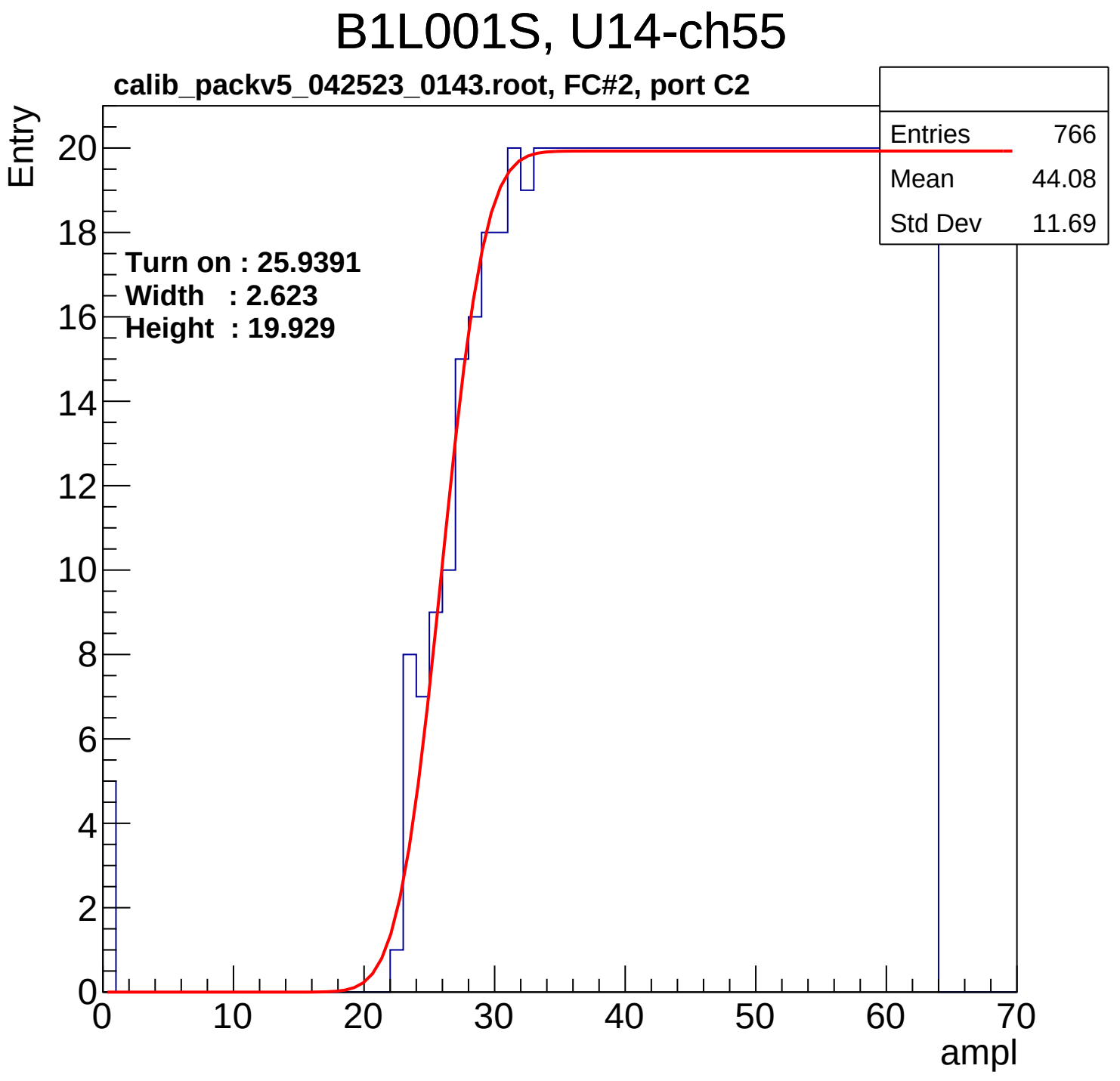

B1L001S, U14-ch50
calib_packv5_042523_0143.root, FC#2, port C2
Entries 750
Mean 44.49
Std Dev 11.41
Turn on : 26.9483
Width : 2.995
Height : 20.013
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

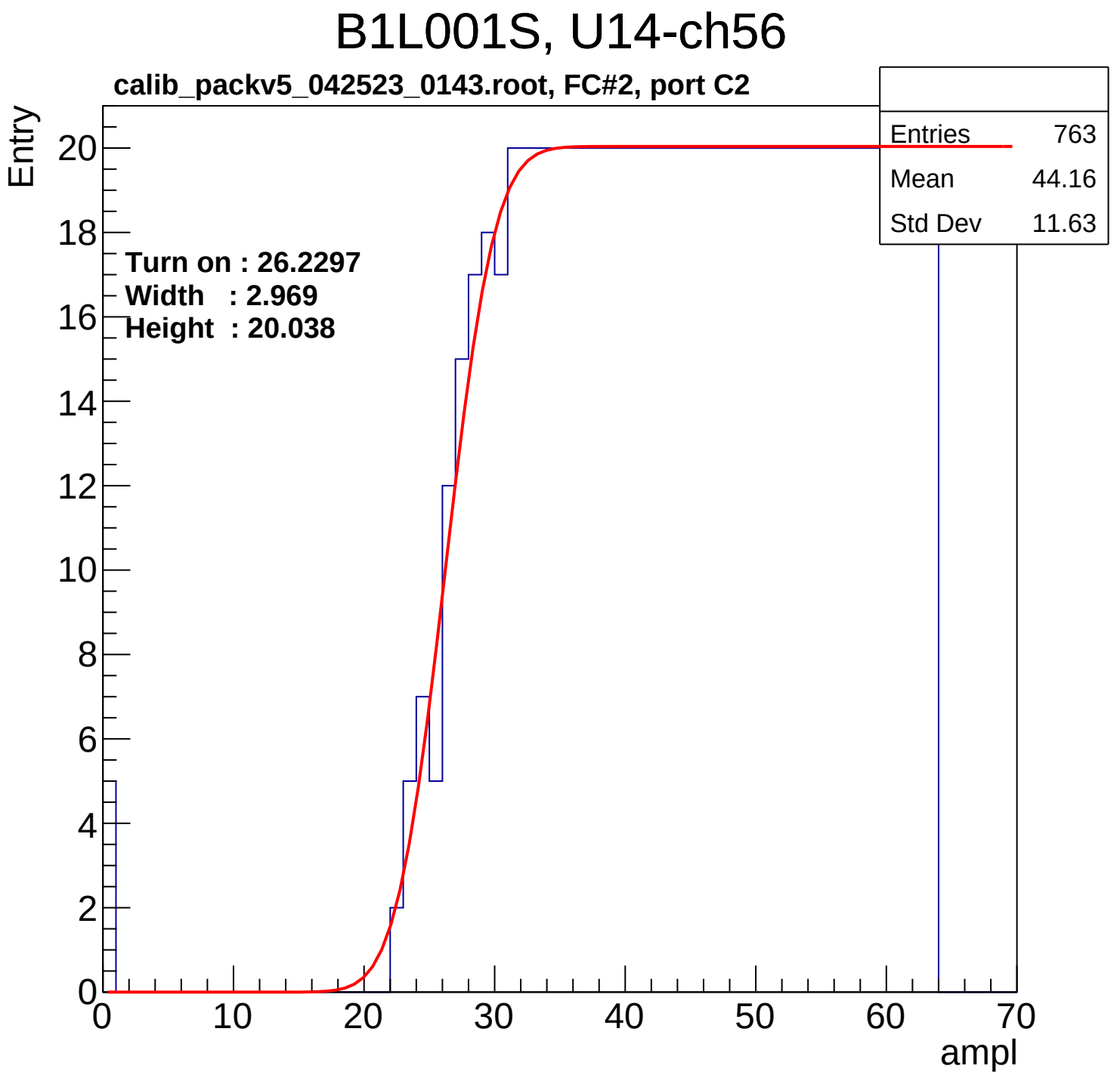

B1L001S, U14-ch51
calib_packv5_042523_0143.root, FC#2, port C2
Entries 762
Mean 44.23
Std Dev 11.47
Turn on : 26.2459
Width : 3.581
Height : 20.103
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

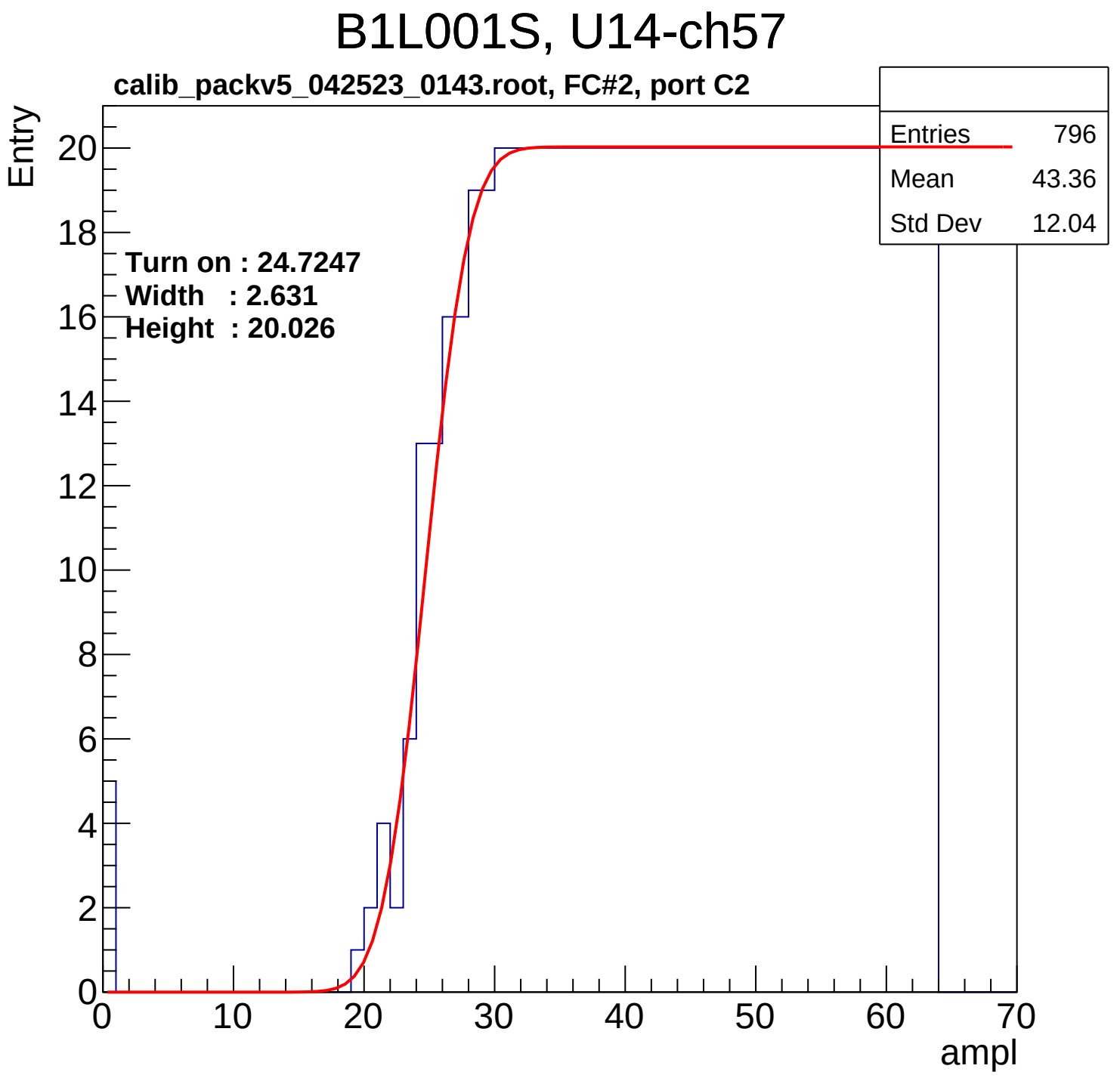

B1L001S, U14-ch52
calib_packv5_042523_0143.root, FC#2, port C2
Entries 738
Mean 44.91
Std Dev 10.97
Turn on : 27.1984
Width : 2.147
Height : 19.998
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

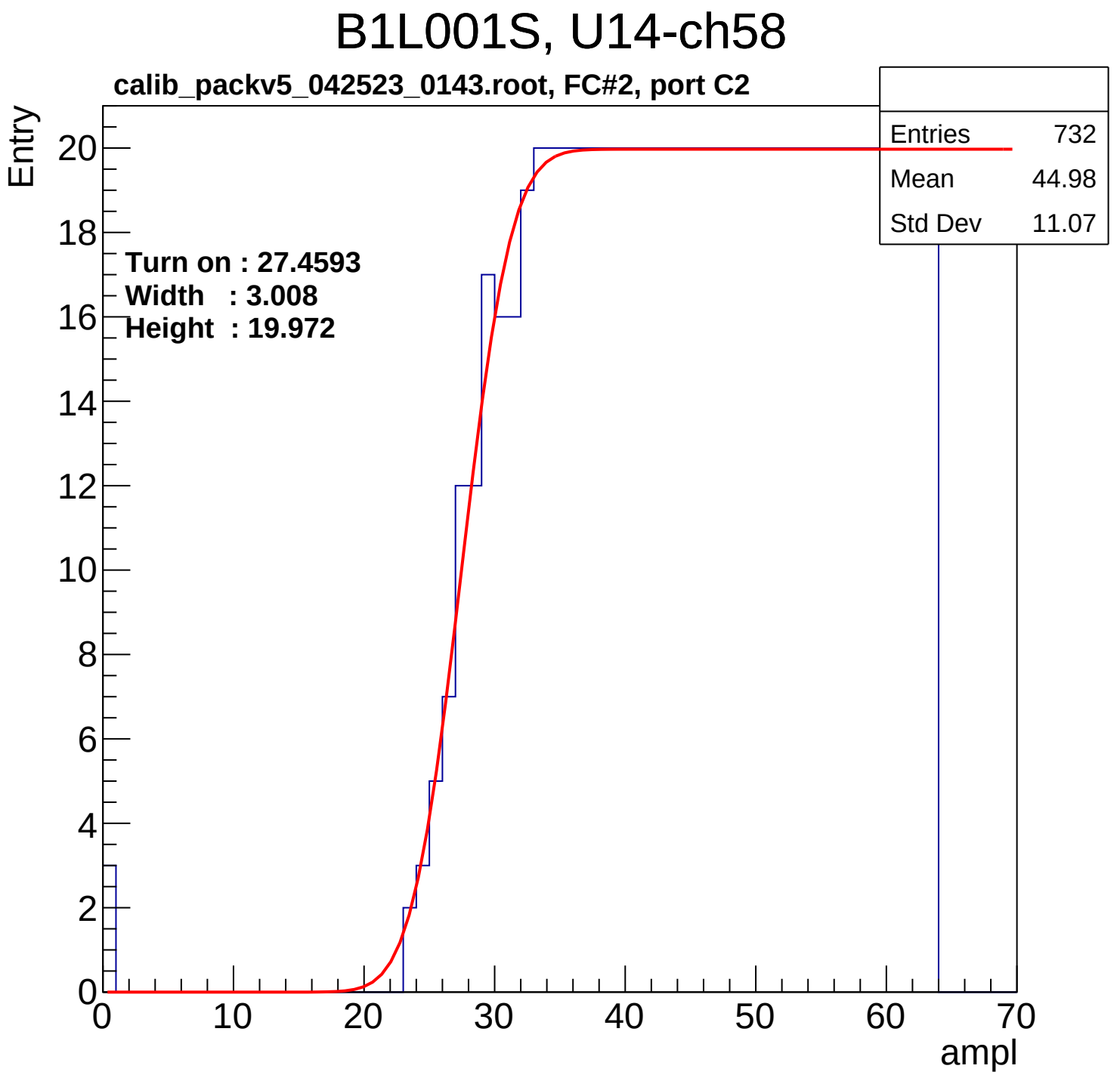

B1L001S, U14-ch53
calib_packv5_042523_0143.root, FC#2, port C2
Entries 757
Mean 44.39
Std Dev 11.35
Turn on : 26.2980
Width : 2.502
Height : 19.969
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

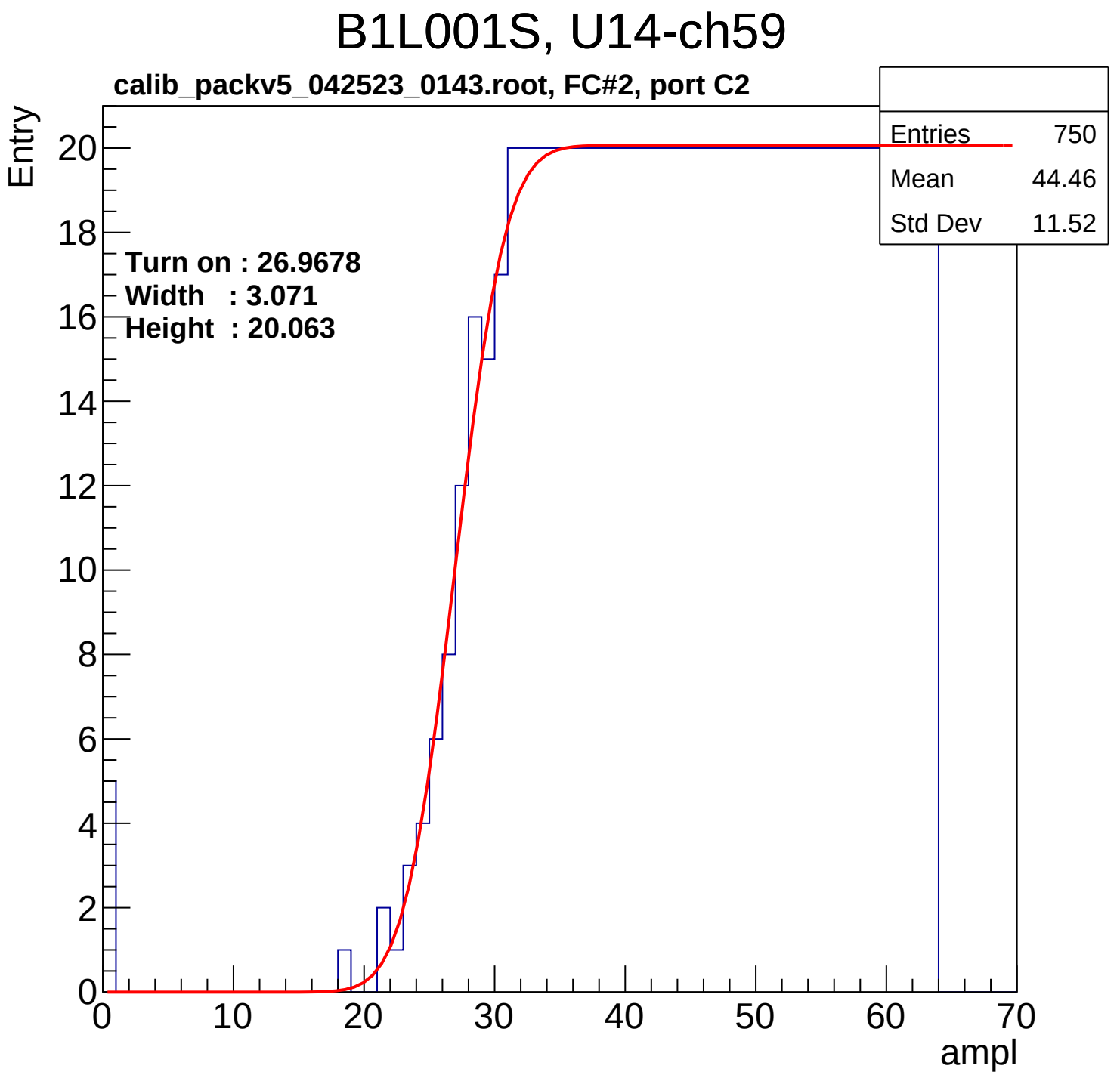

B1L001S, U14-ch54
calib_packv5_042523_0143.root, FC#2, port C2
Entries 747
Mean 44.6
Std Dev 11.29
Turn on : 27.1489
Width : 2.971
Height : 20.059
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

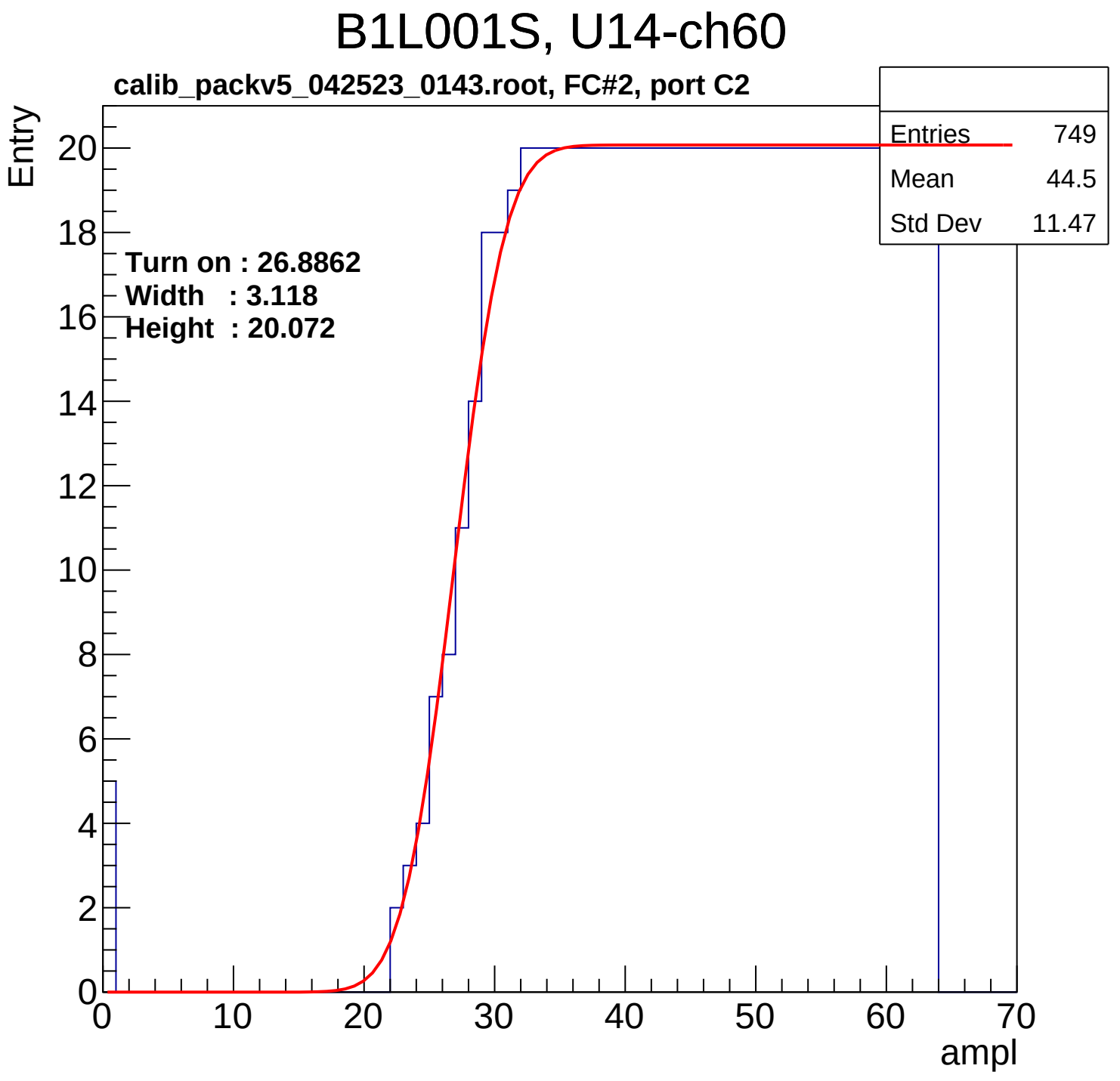

B1L001S, U14-ch55
calib_packv5_042523_0143.root, FC#2, port C2
Entries 766
Mean 44.08
Std Dev 11.69
Turn on : 25.9391
Width : 2.623
Height : 19.929
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

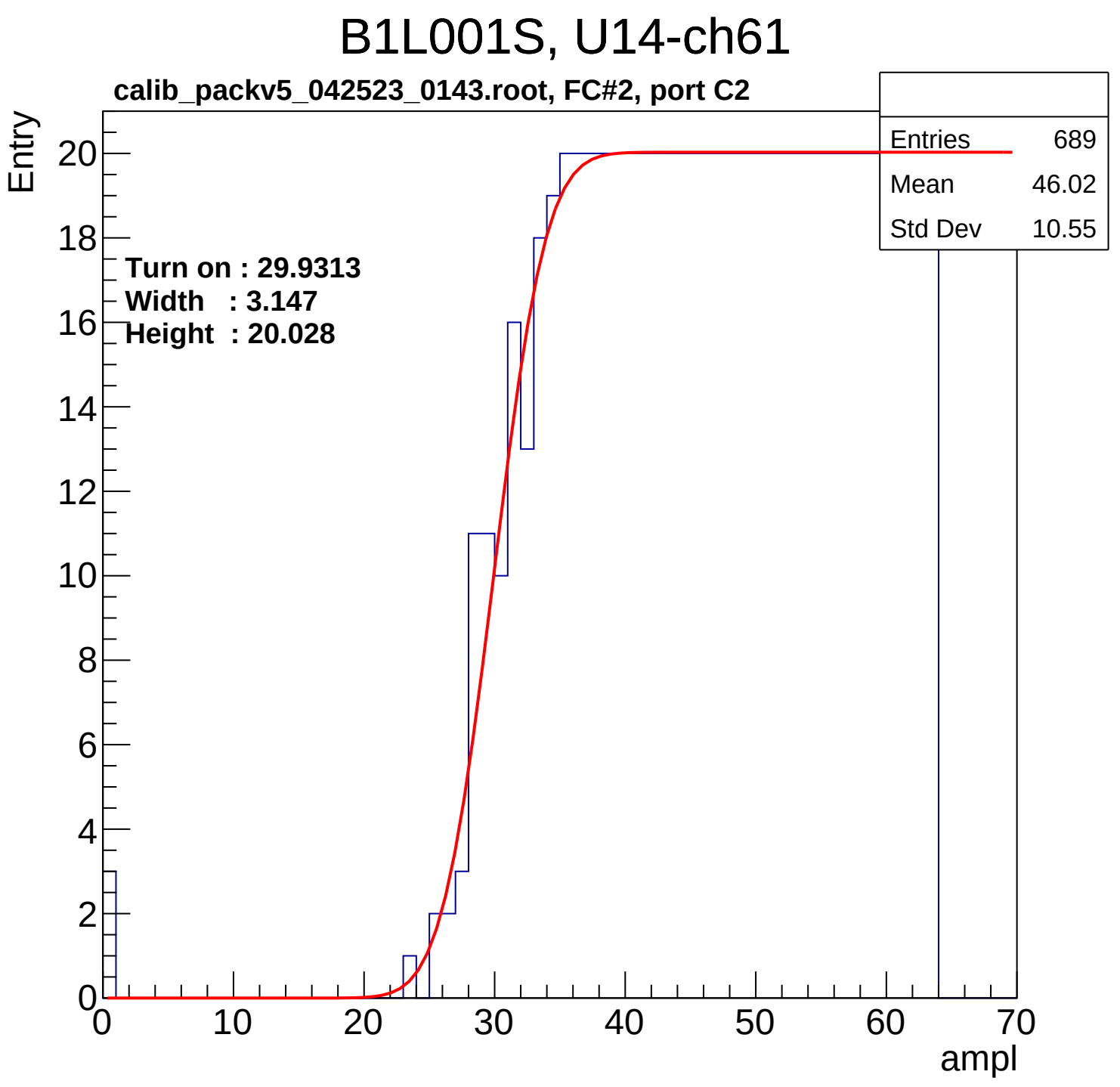

B1L001S, U14-ch56
calib_packv5_042523_0143.root, FC#2, port C2
Entries 763
Mean 44.16
Std Dev 11.63
Turn on : 26.2297
Width : 2.969
Height : 20.038
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

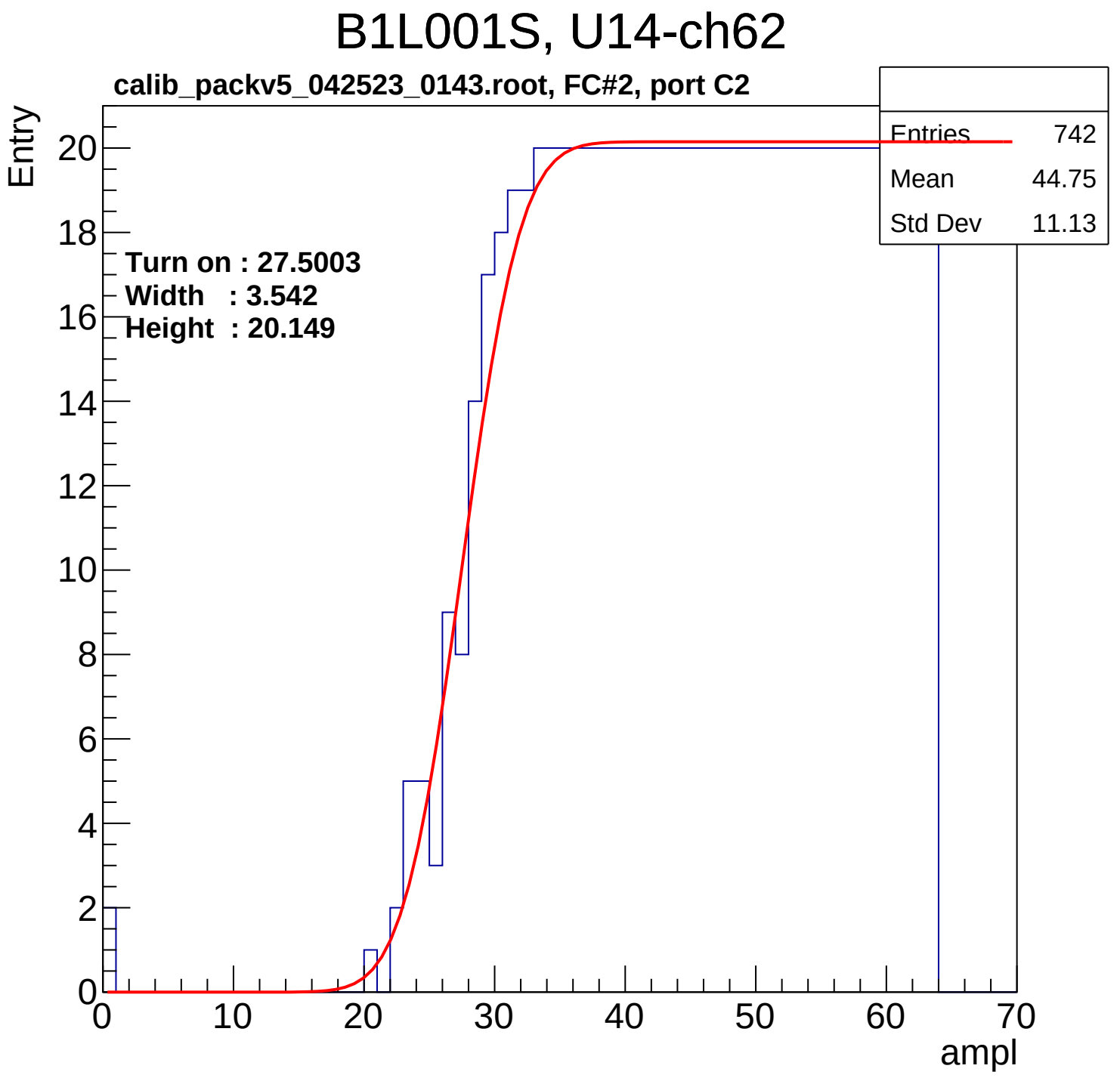

B1L001S, U14-ch57
calib_packv5_042523_0143.root, FC#2, port C2
Entries 796
Mean 43.36
Std Dev 12.04
Turn on : 24.7247
Width : 2.631
Height : 20.026
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

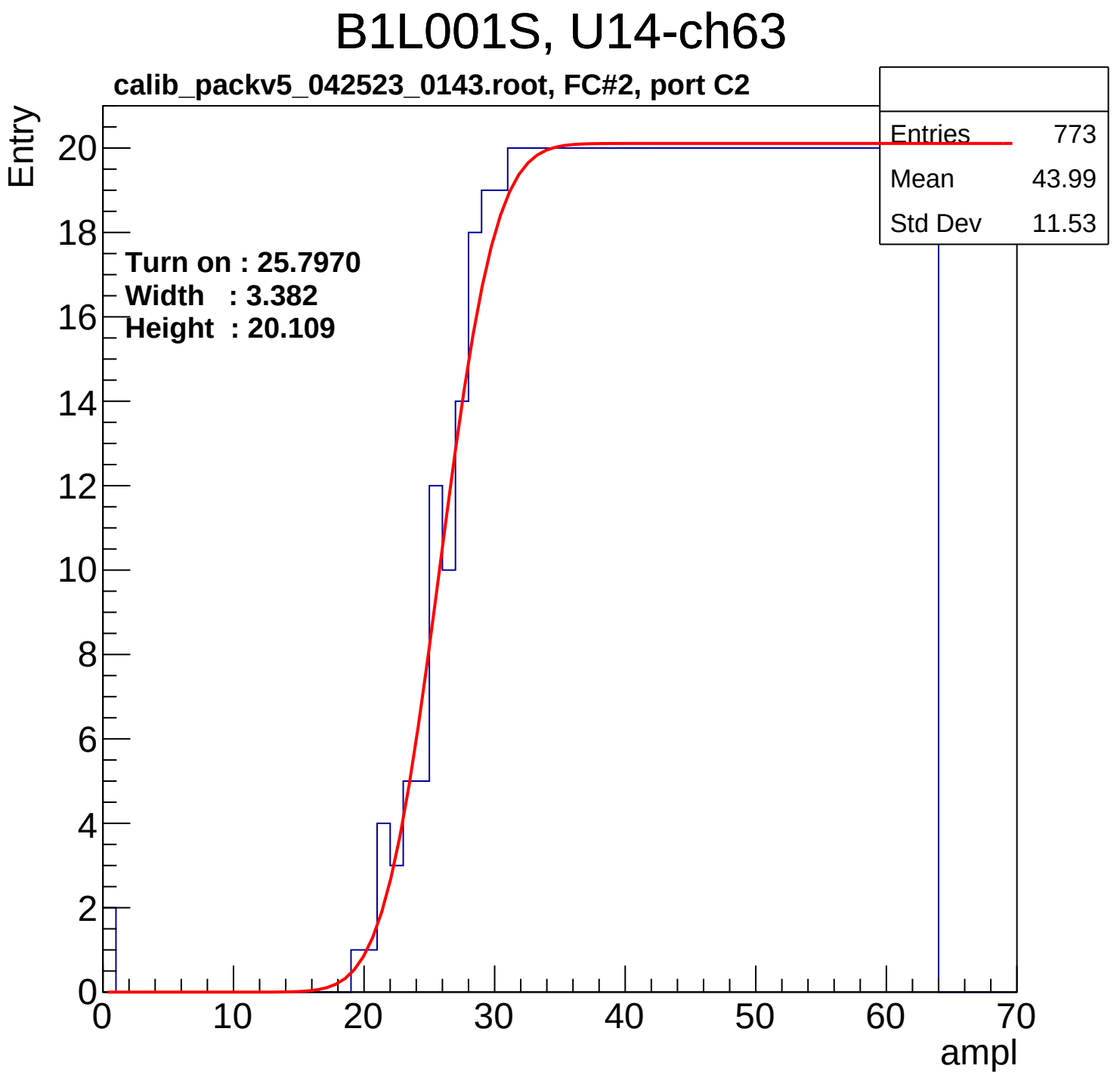

B1L001S, U14-ch58
calib_packv5_042523_0143.root, FC#2, port C2
Entries 732
Mean 44.98
Std Dev 11.07
Turn on : 27.4593
Width : 3.008
Height : 19.972
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

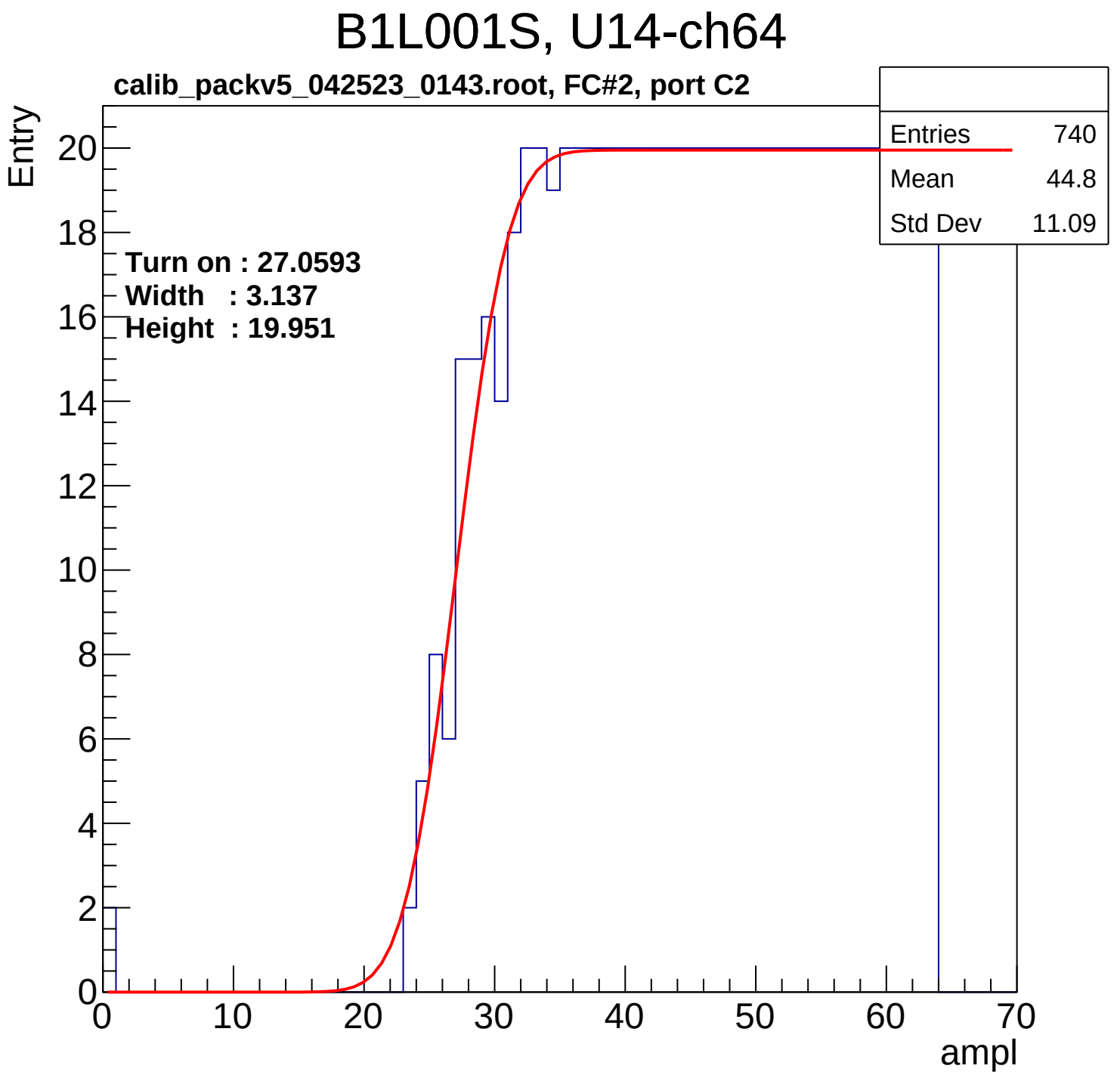

B1L001S, U14-ch59
calib_packv5_042523_0143.root, FC#2, port C2
Entries 750
Mean 44.46
Std Dev 11.52
Turn on : 26.9678
Width : 3.071
Height : 20.063
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

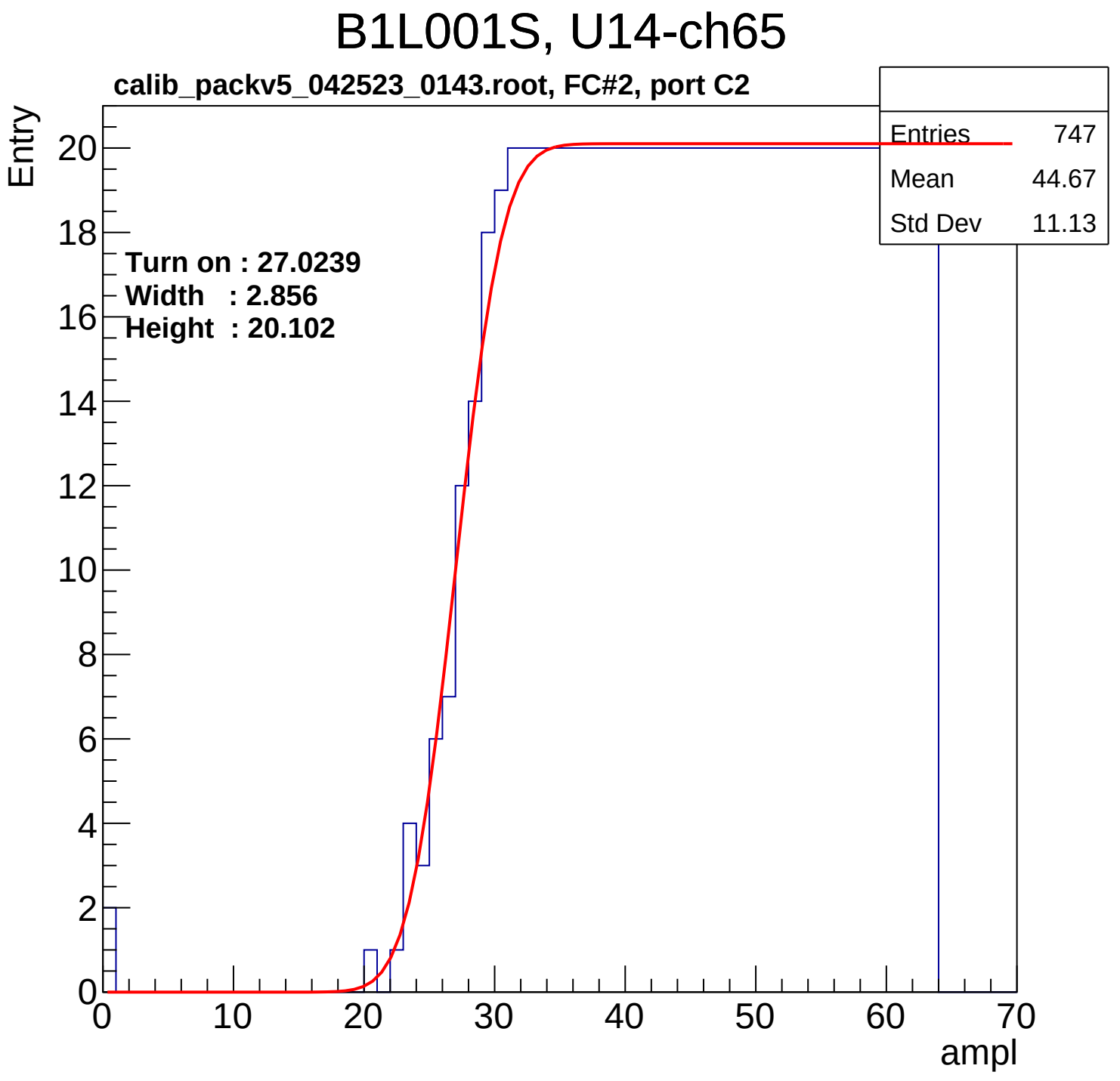

B1L001S, U14-ch60
calib_packv5_042523_0143.root, FC#2, port C2
Entries 749
Mean 44.5
Std Dev 11.47
Turn on : 26.8862
Width : 3.118
Height : 20.072
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

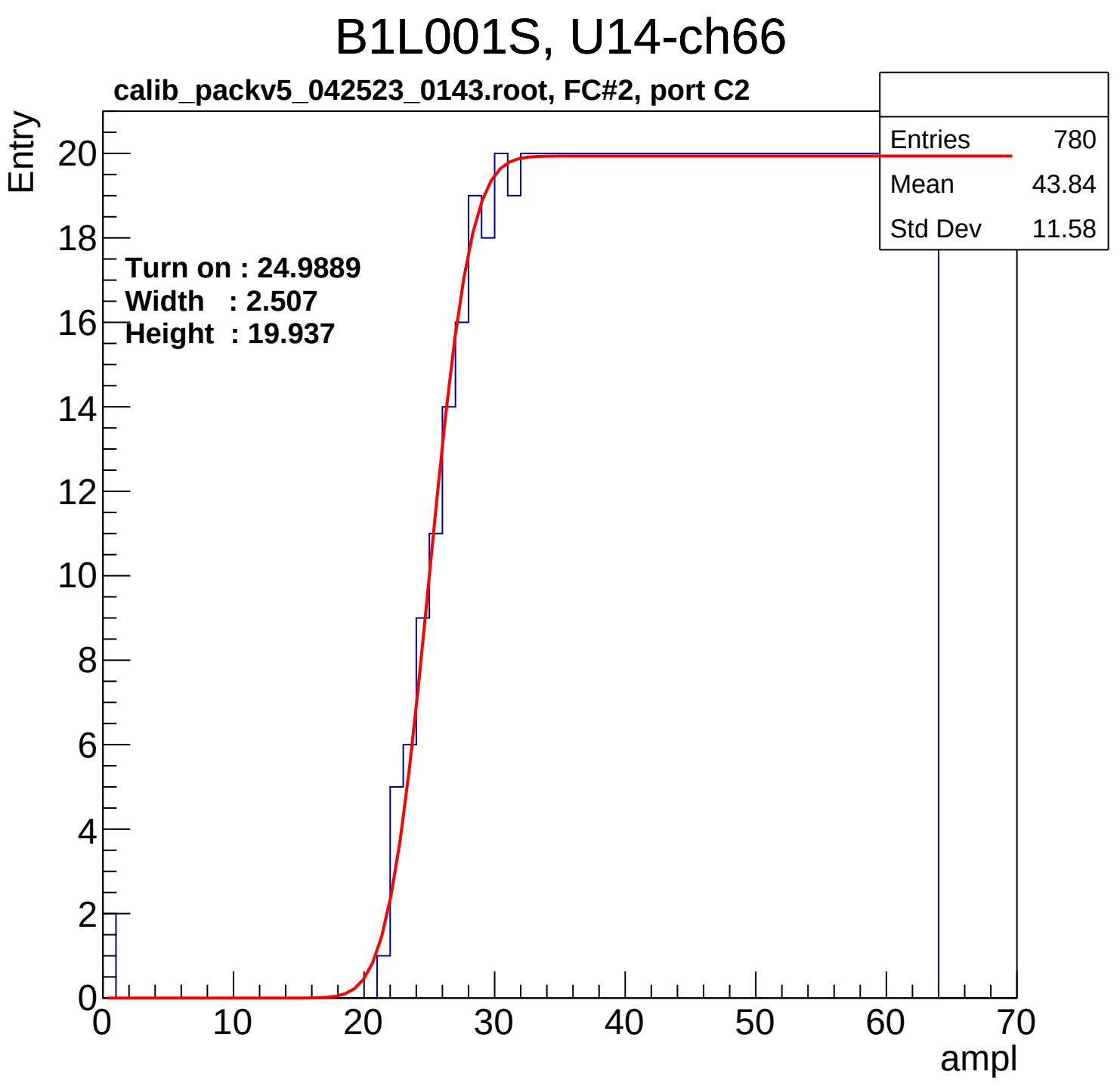

B1L001S, U14-ch61
calib_packv5_042523_0143.root, FC#2, port C2
Entries 689
Mean 46.02
Std Dev 10.55
Turn on : 29.9313
Width : 3.147
Height : 20.028
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

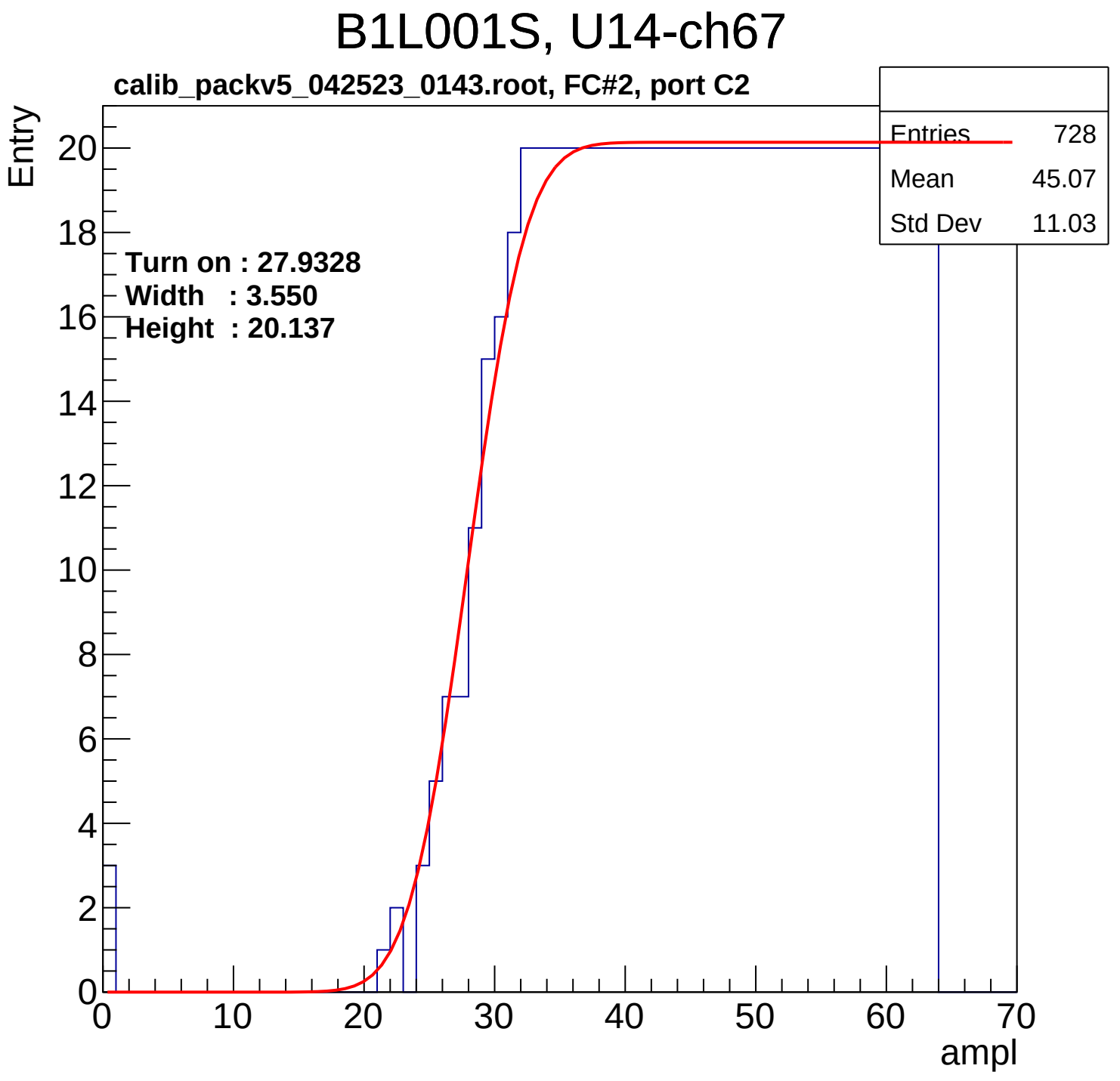

B1L001S, U14-ch62
calib_packv5_042523_0143.root, FC#2, port C2
Entries 742
Mean 44.75
Std Dev 11.13
Turn on : 27.5003
Width : 3.542
Height : 20.149
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

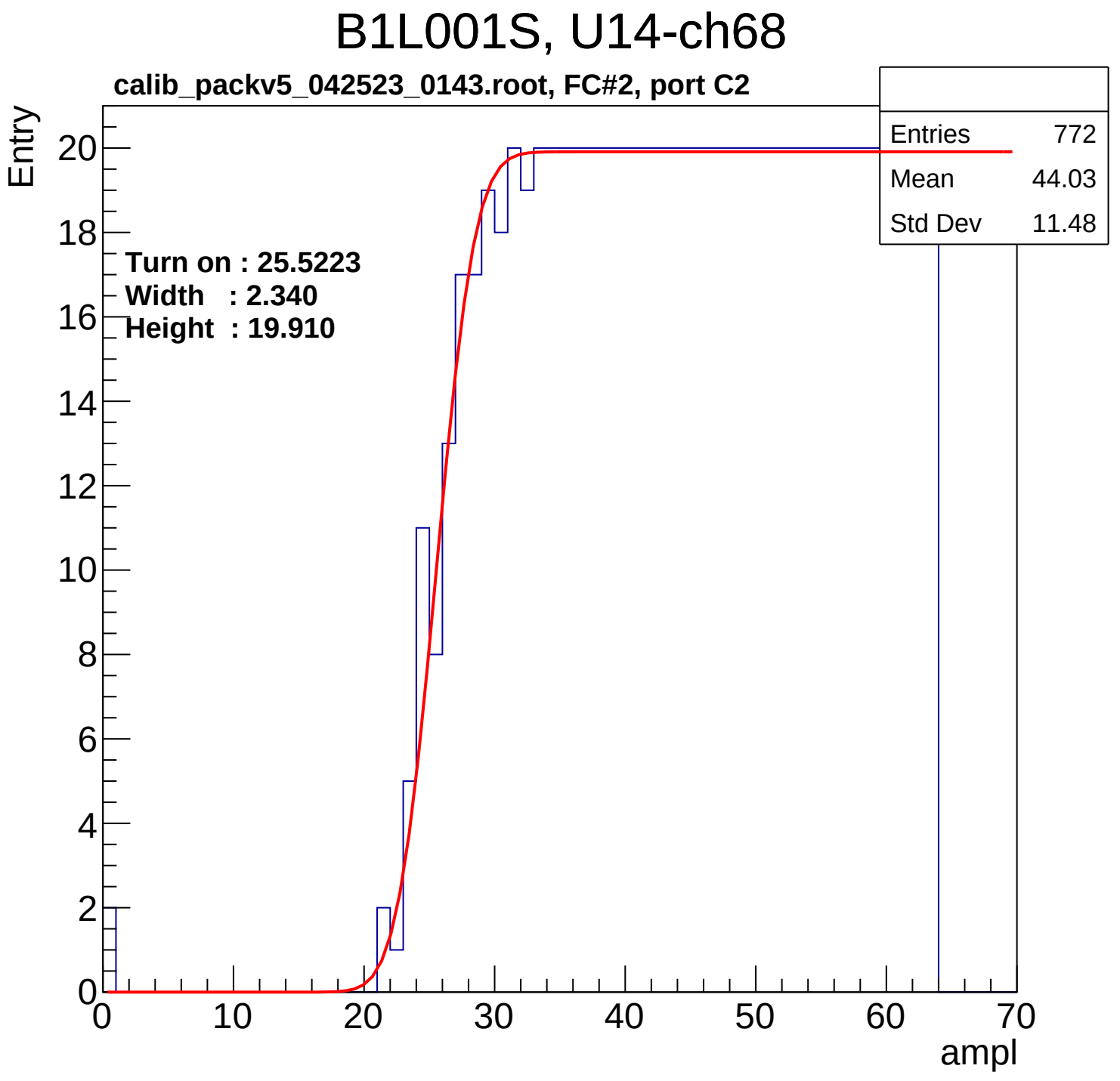

B1L001S, U14-ch63
calib_packv5_042523_0143.root, FC#2, port C2
Entries 773
Mean 43.99
Std Dev 11.53
Turn on : 25.7970
Width : 3.382
Height : 20.109
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

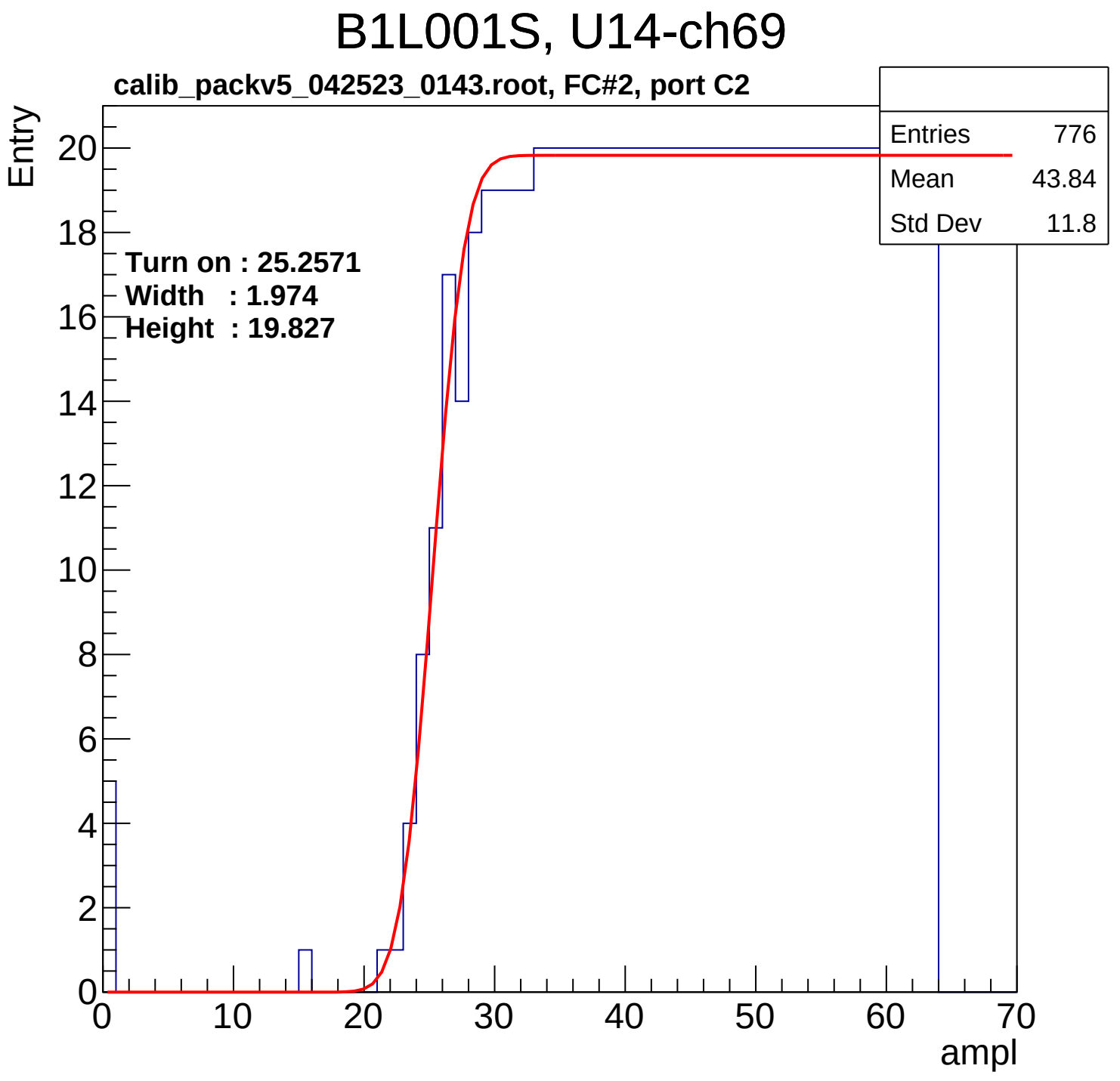

B1L001S, U14-ch64
calib_packv5_042523_0143.root, FC#2, port C2
Entries 740
Mean 44.8
Std Dev 11.09
Turn on : 27.0593
Width : 3.137
Height : 19.951
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

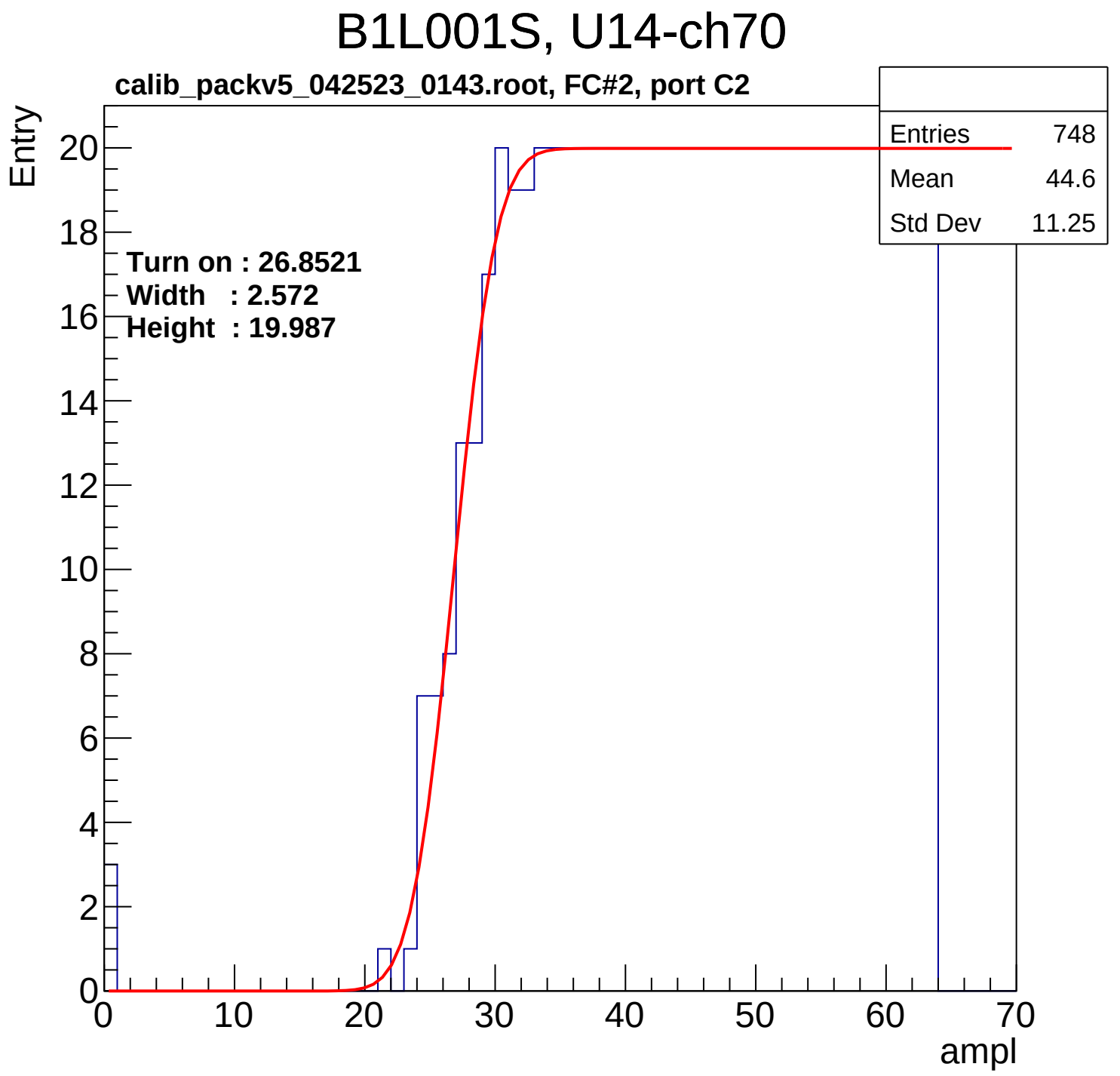

B1L001S, U14-ch65
calib_packv5_042523_0143.root, FC#2, port C2
Entries 747
Mean 44.67
Std Dev 11.13
Turn on : 27.0239
Width : 2.856
Height : 20.102
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

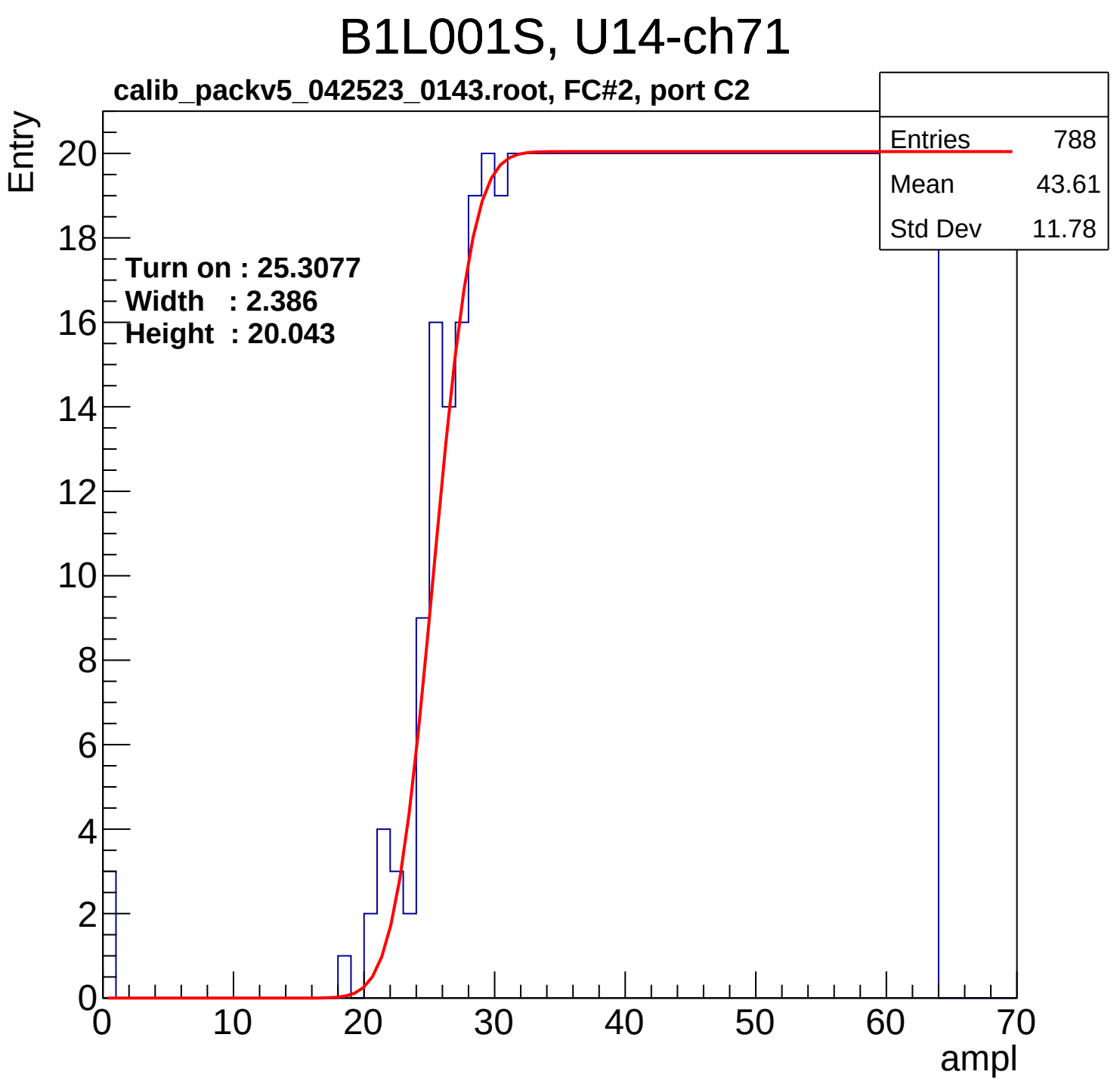

B1L001S, U14-ch66
calib_packv5_042523_0143.root, FC#2, port C2
Entries 780
Mean 43.84
Std Dev 11.58
Turn on : 24.9889
Width : 2.507
Height : 19.937
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

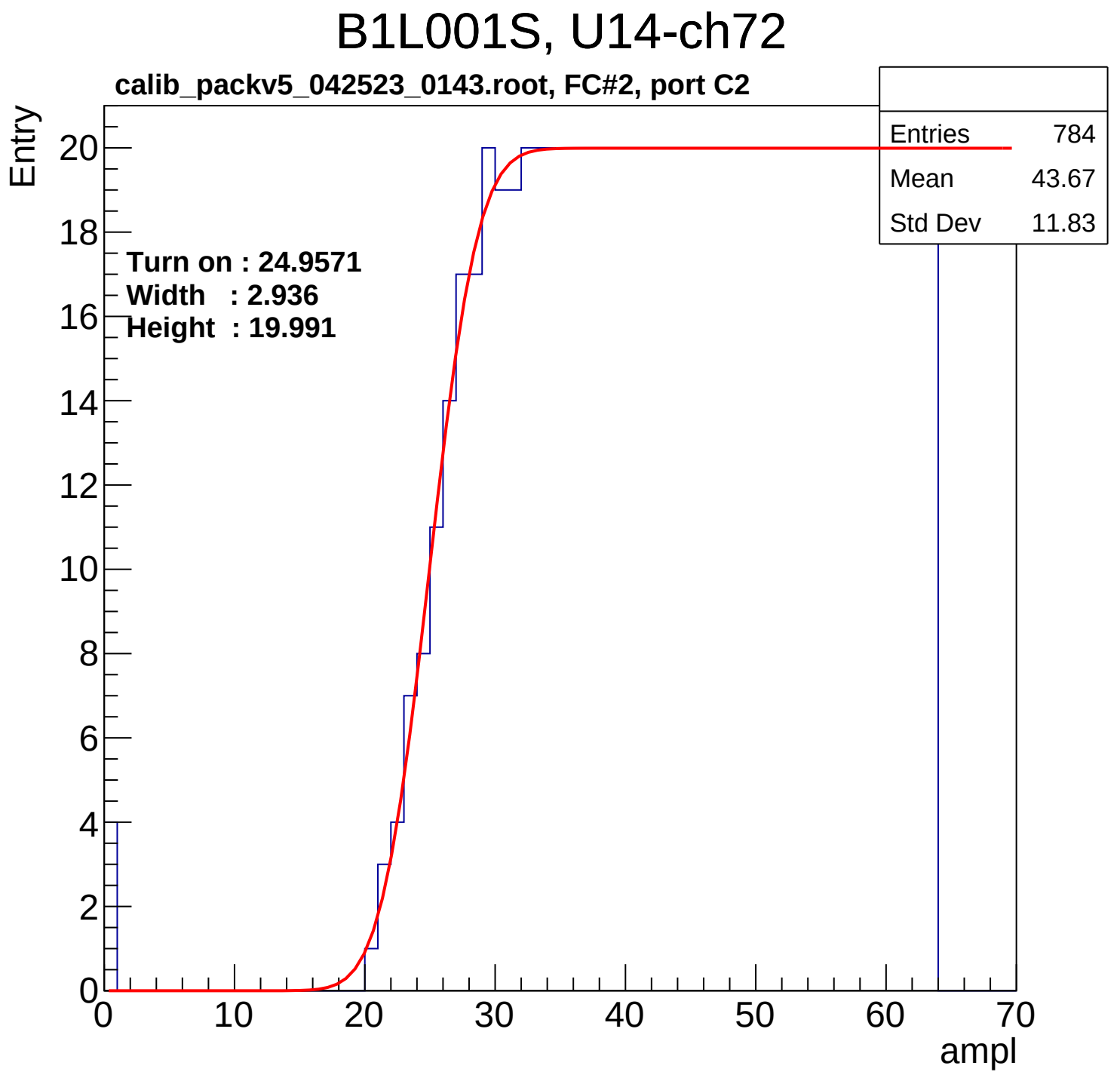

B1L001S, U14-ch67
calib_packv5_042523_0143.root, FC#2, port C2
Entries 728
Mean 45.07
Std Dev 11.03
Turn on : 27.9328
Width : 3.550
Height : 20.137
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

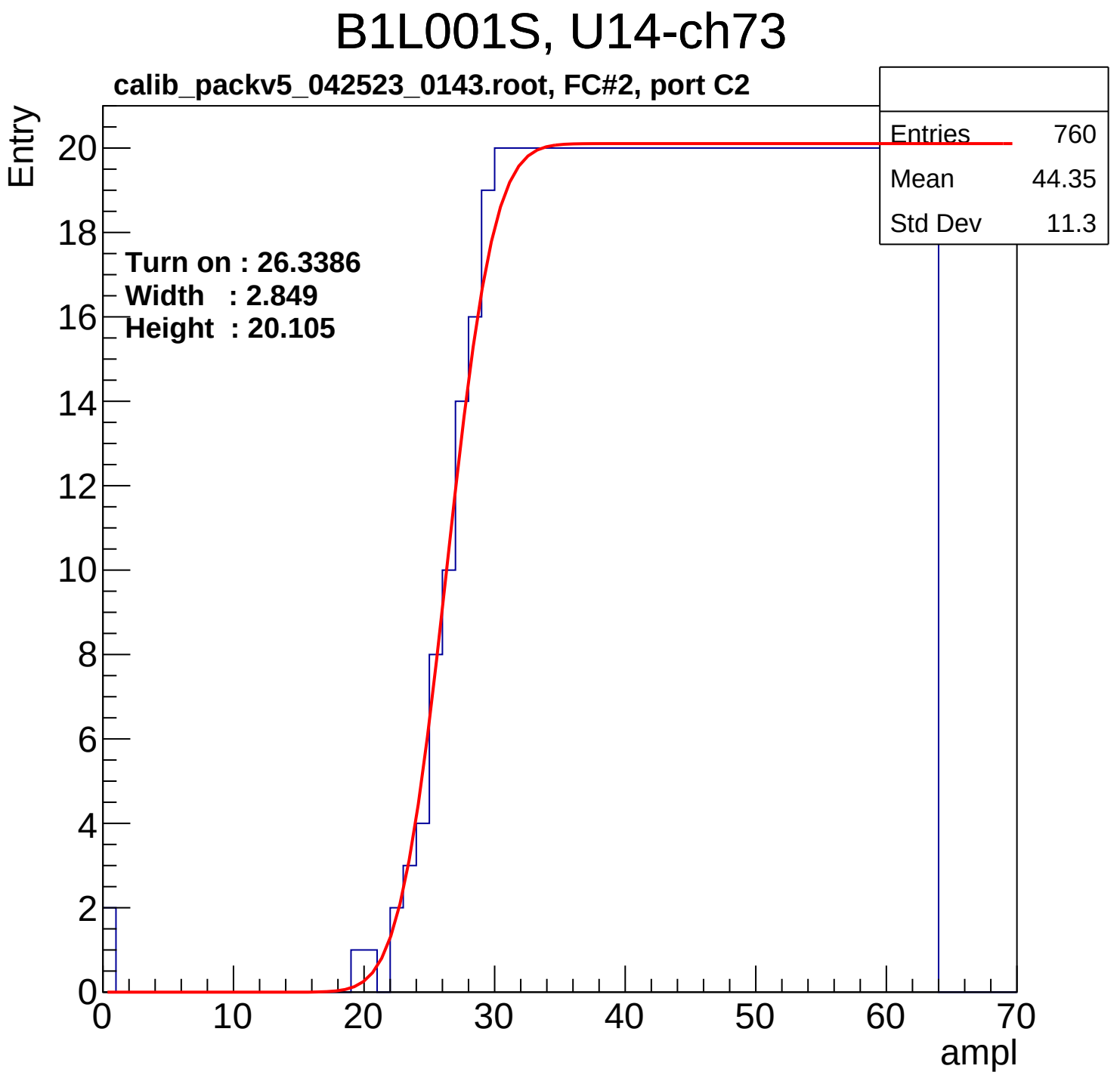

B1L001S, U14-ch68
calib_packv5_042523_0143.root, FC#2, port C2
Entries 772
Mean 44.03
Std Dev 11.48
Turn on : 25.5223
Width : 2.340
Height : 19.910
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

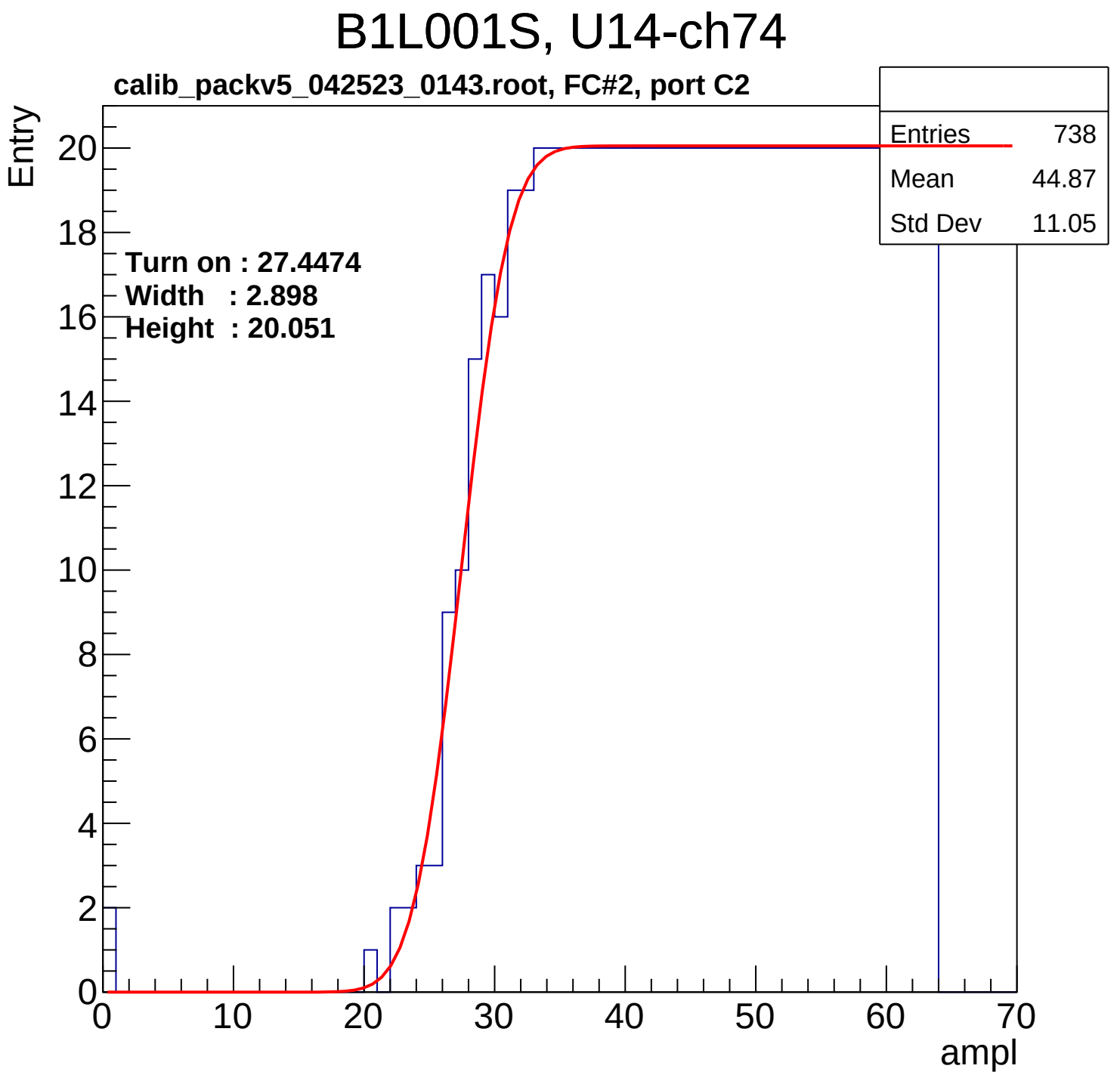

B1L001S, U14-ch69
calib_packv5_042523_0143.root, FC#2, port C2
Entries 776
Mean 43.84
Std Dev 11.8
Turn on : 25.2571
Width : 1.974
Height : 19.827
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

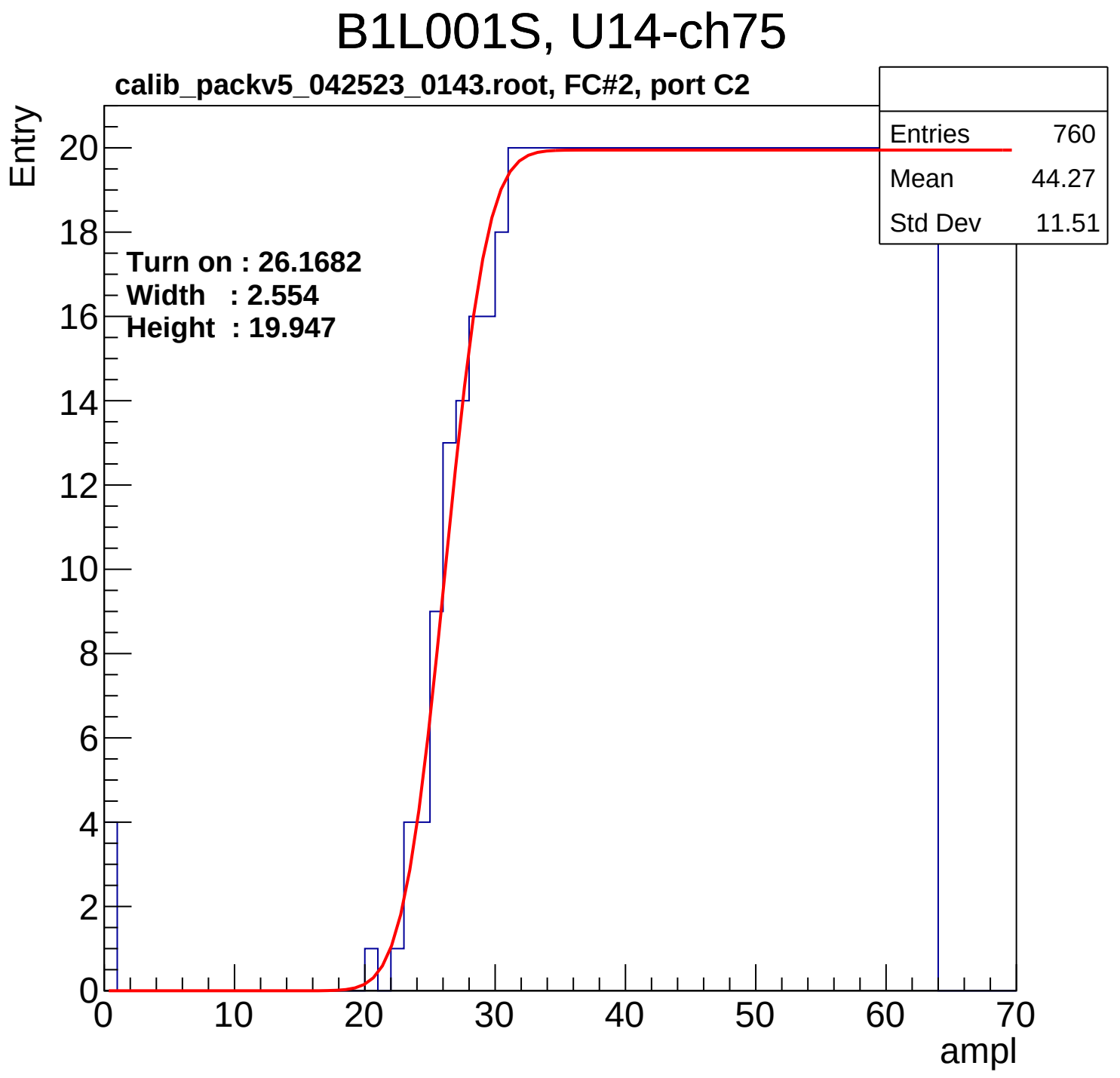

B1L001S, U14-ch70
calib_packv5_042523_0143.root, FC#2, port C2
Entries 748
Mean 44.6
Std Dev 11.25
Turn on : 26.8521
Width : 2.572
Height : 19.987
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

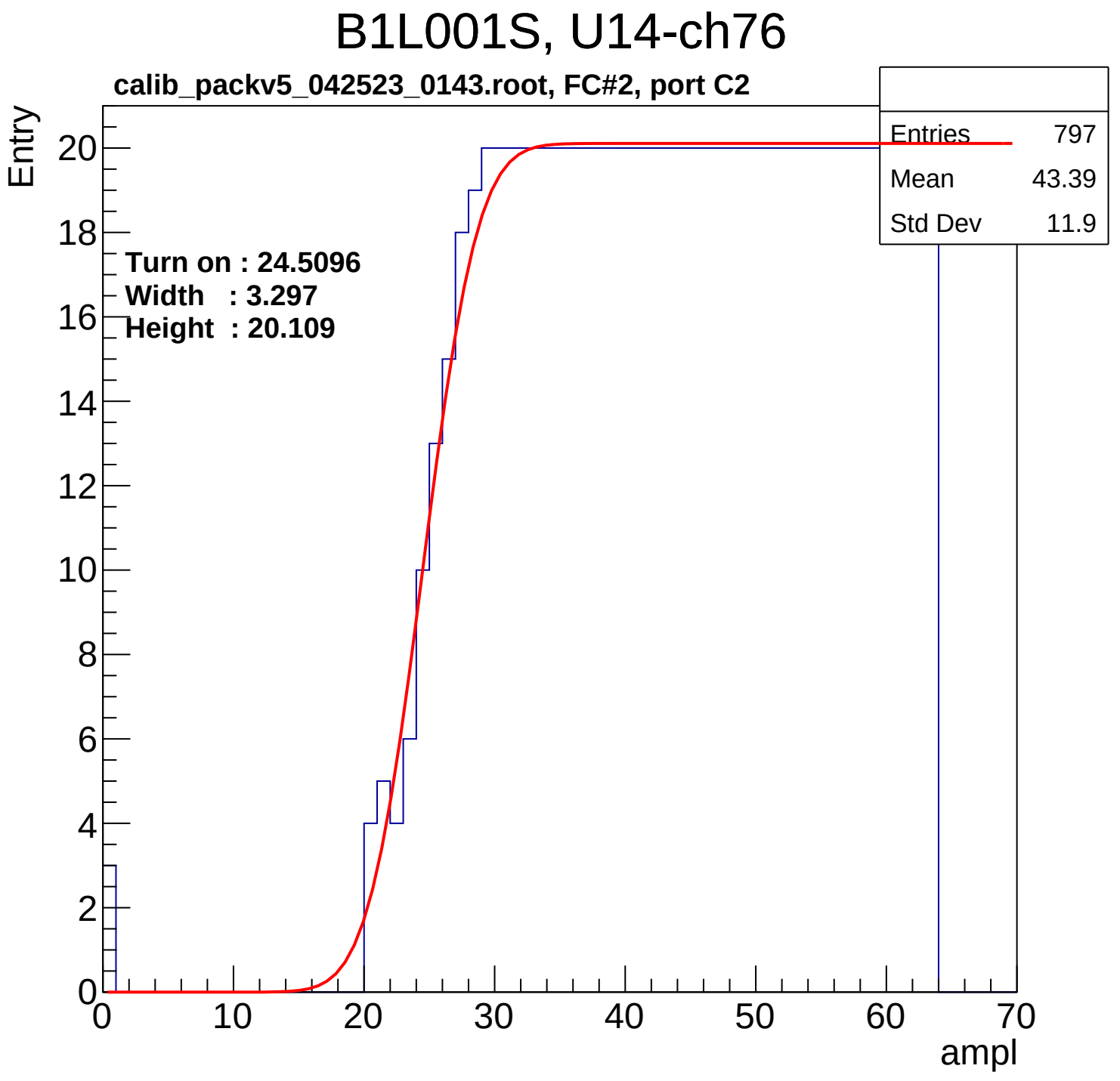

B1L001S, U14-ch71
calib_packv5_042523_0143.root, FC#2, port C2
Entries 788
Mean 43.61
Std Dev 11.78
Turn on : 25.3077
Width : 2.386
Height : 20.043
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

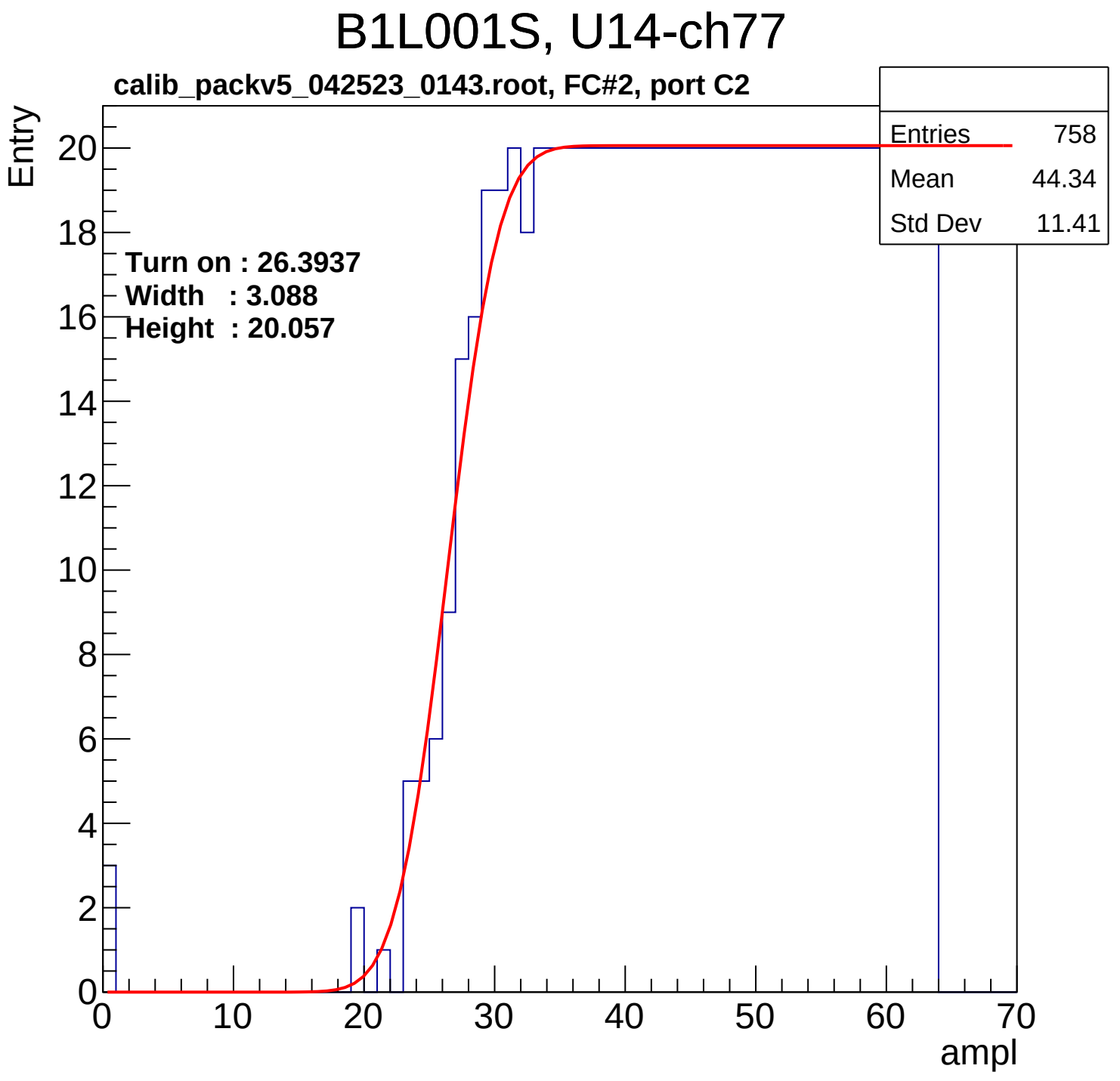

B1L001S, U14-ch72
calib_packv5_042523_0143.root, FC#2, port C2
Entries 784
Mean 43.67
Std Dev 11.83
Turn on : 24.9571
Width : 2.936
Height : 19.991
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

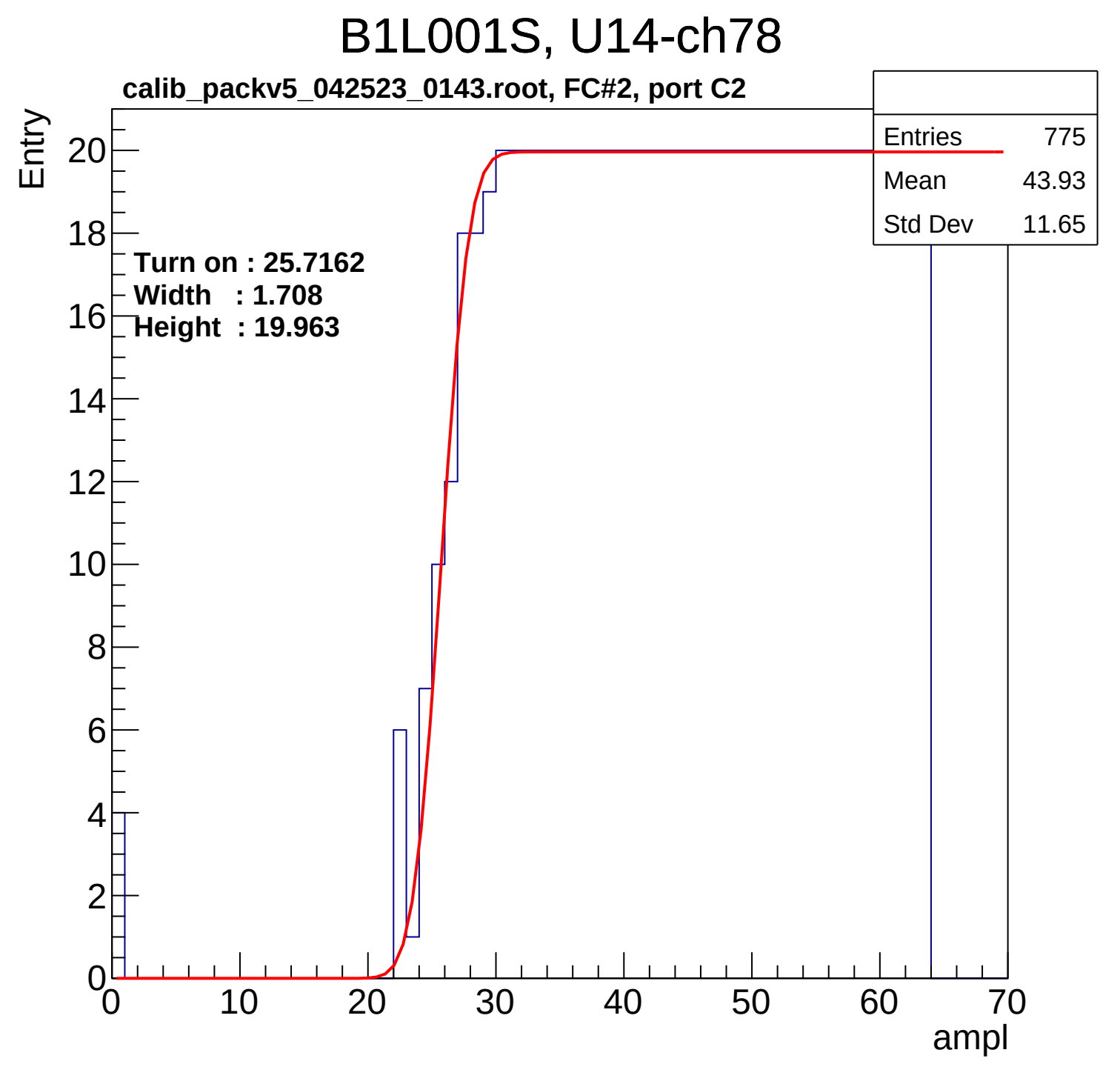

B1L001S, U14-ch73
calib_packv5_042523_0143.root, FC#2, port C2
Entries 760
Mean 44.35
Std Dev 11.3
Turn on : 26.3386
Width : 2.849
Height : 20.105
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

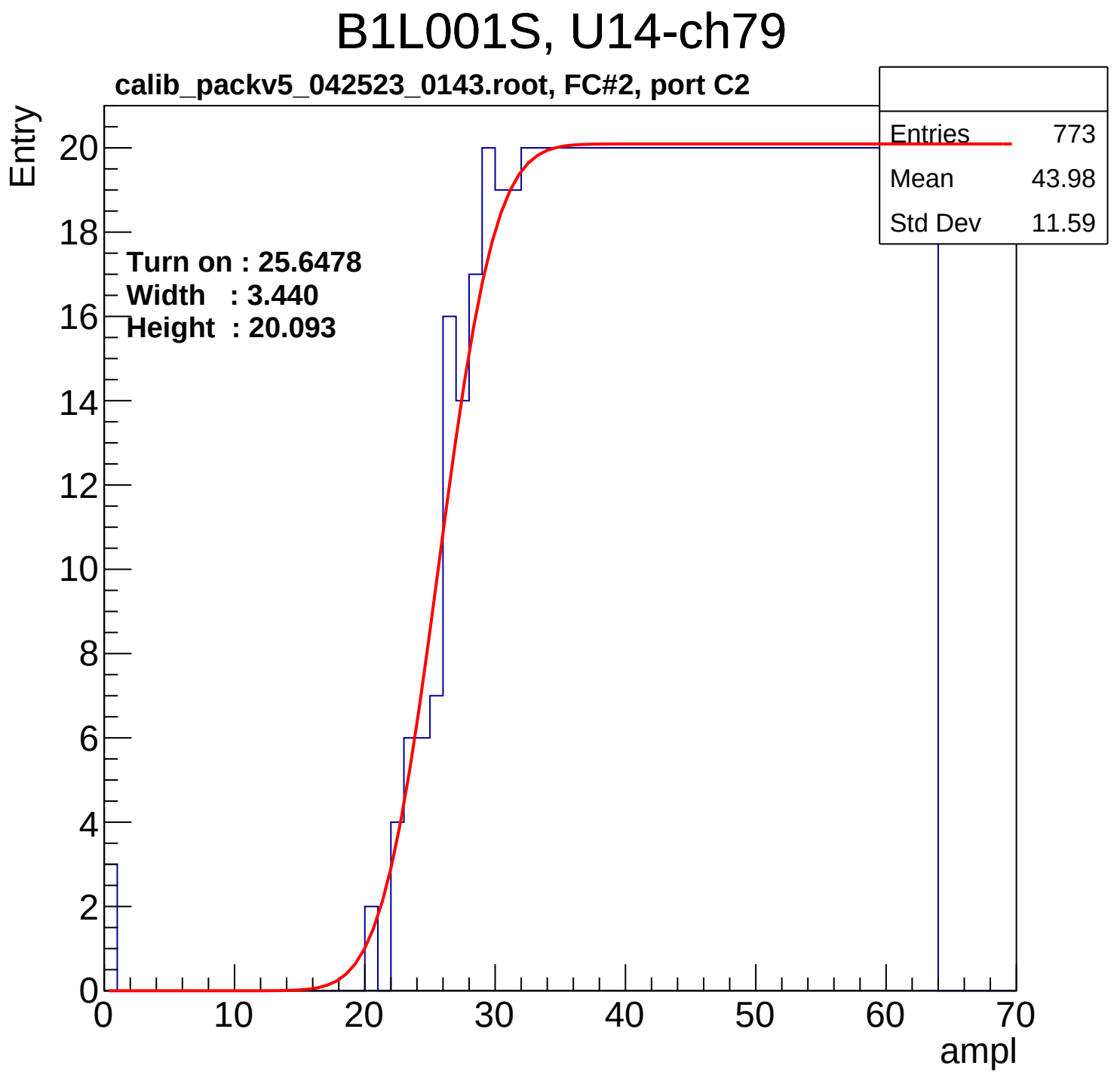

B1L001S, U14-ch74
calib_packv5_042523_0143.root, FC#2, port C2
Entries 738
Mean 44.87
Std Dev 11.05
Turn on : 27.4474
Width : 2.898
Height : 20.051
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

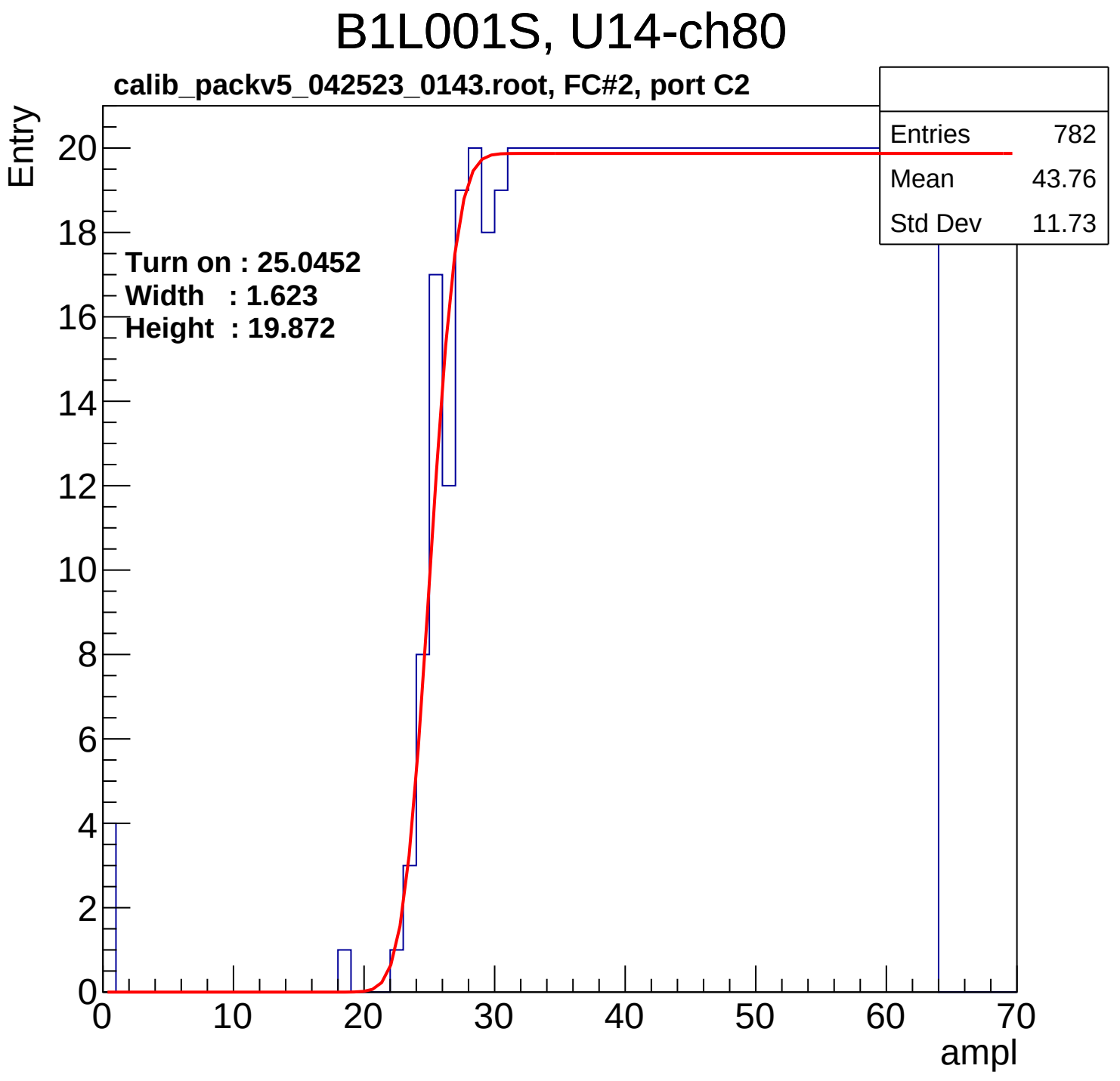

B1L001S, U14-ch75
calib_packv5_042523_0143.root, FC#2, port C2
Entries 760
Mean 44.27
Std Dev 11.51
Turn on : 26.1682
Width : 2.554
Height : 19.947
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

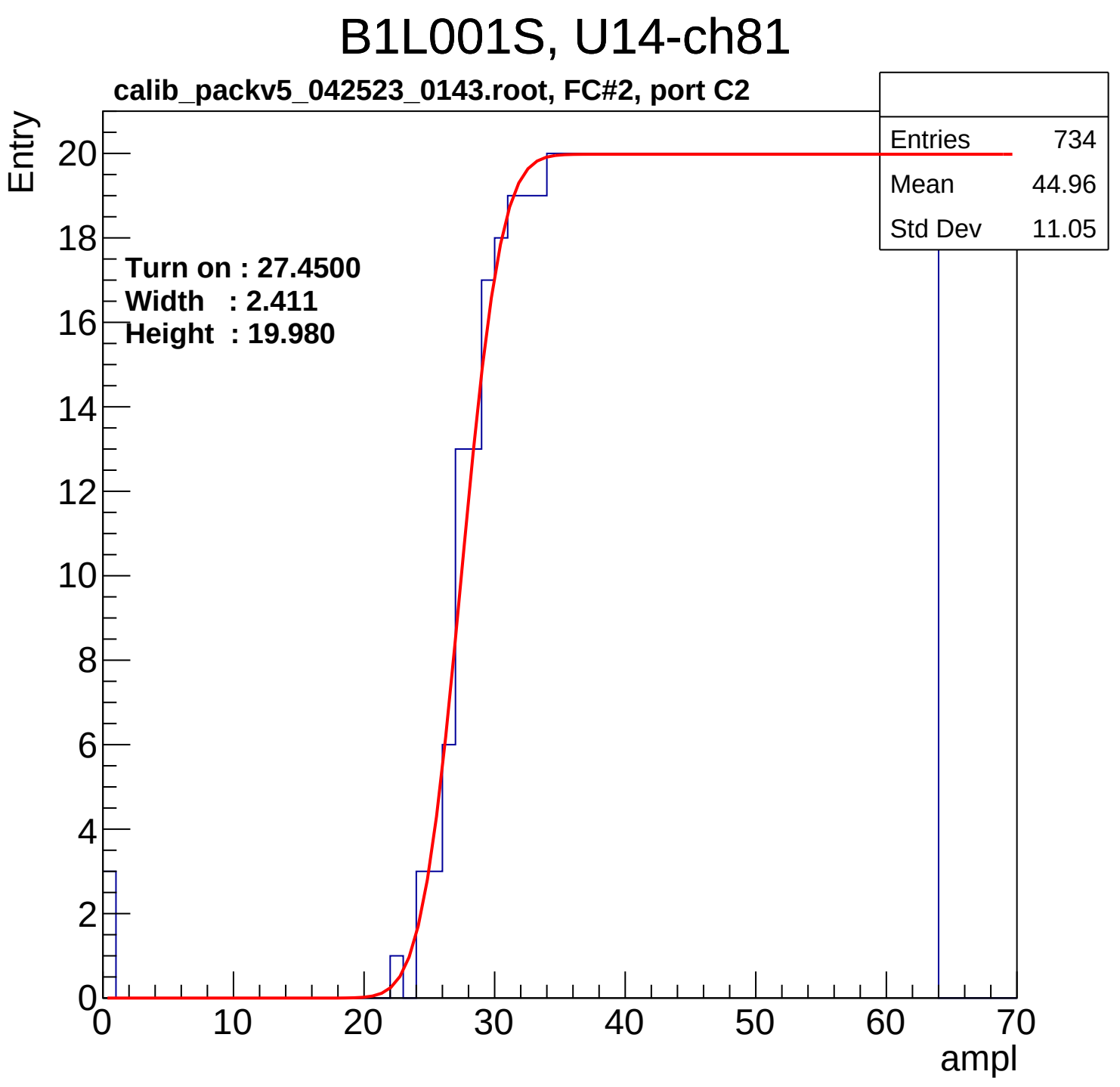

B1L001S, U14-ch76
calib_packv5_042523_0143.root, FC#2, port C2
Entries 797
Mean 43.39
Std Dev 11.9
Turn on : 24.5096
Width : 3.297
Height : 20.109
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

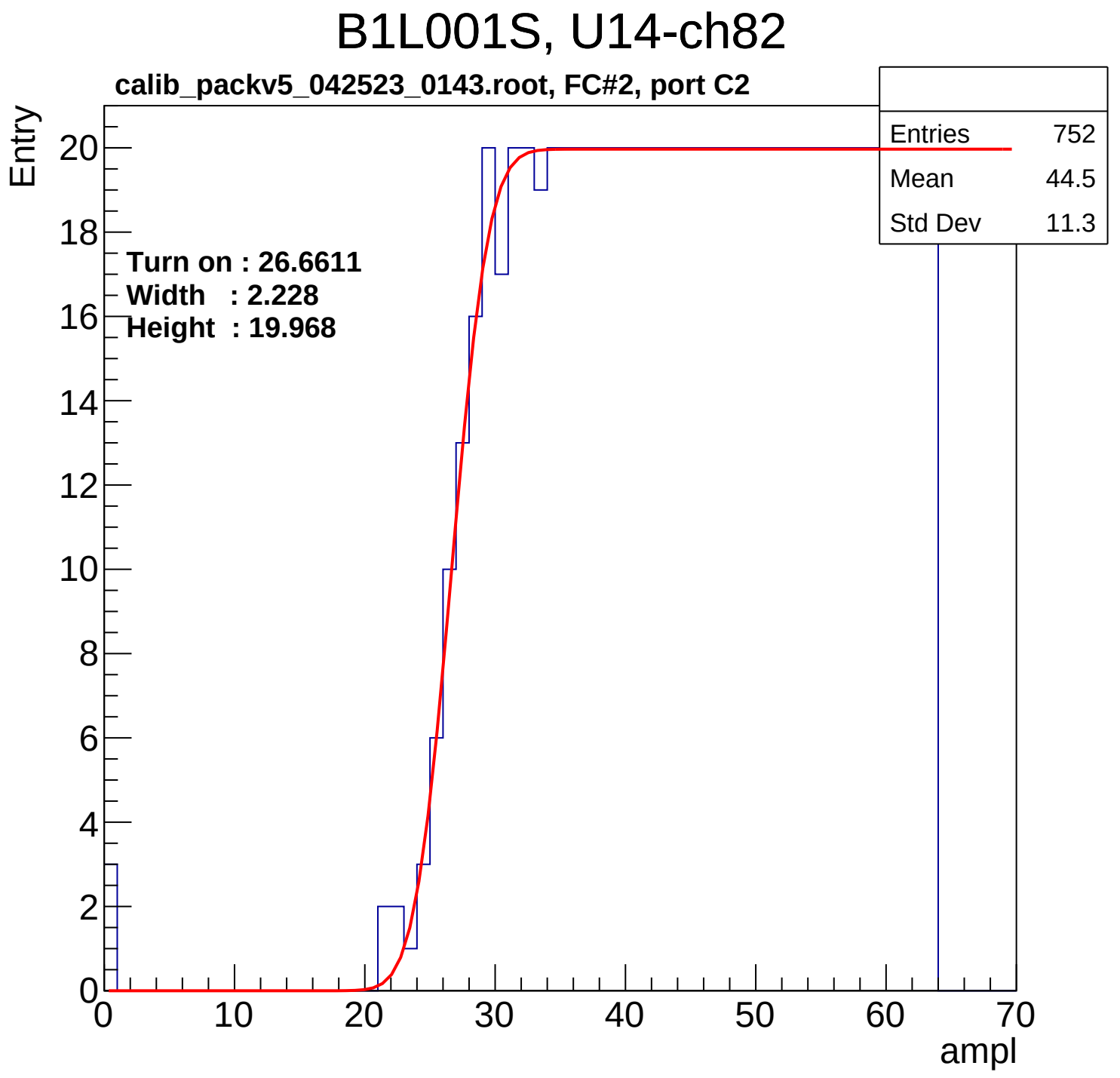

B1L001S, U14-ch77
calib_packv5_042523_0143.root, FC#2, port C2
Entries 758
Mean 44.34
Std Dev 11.41
Turn on : 26.3937
Width : 3.088
Height : 20.057
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

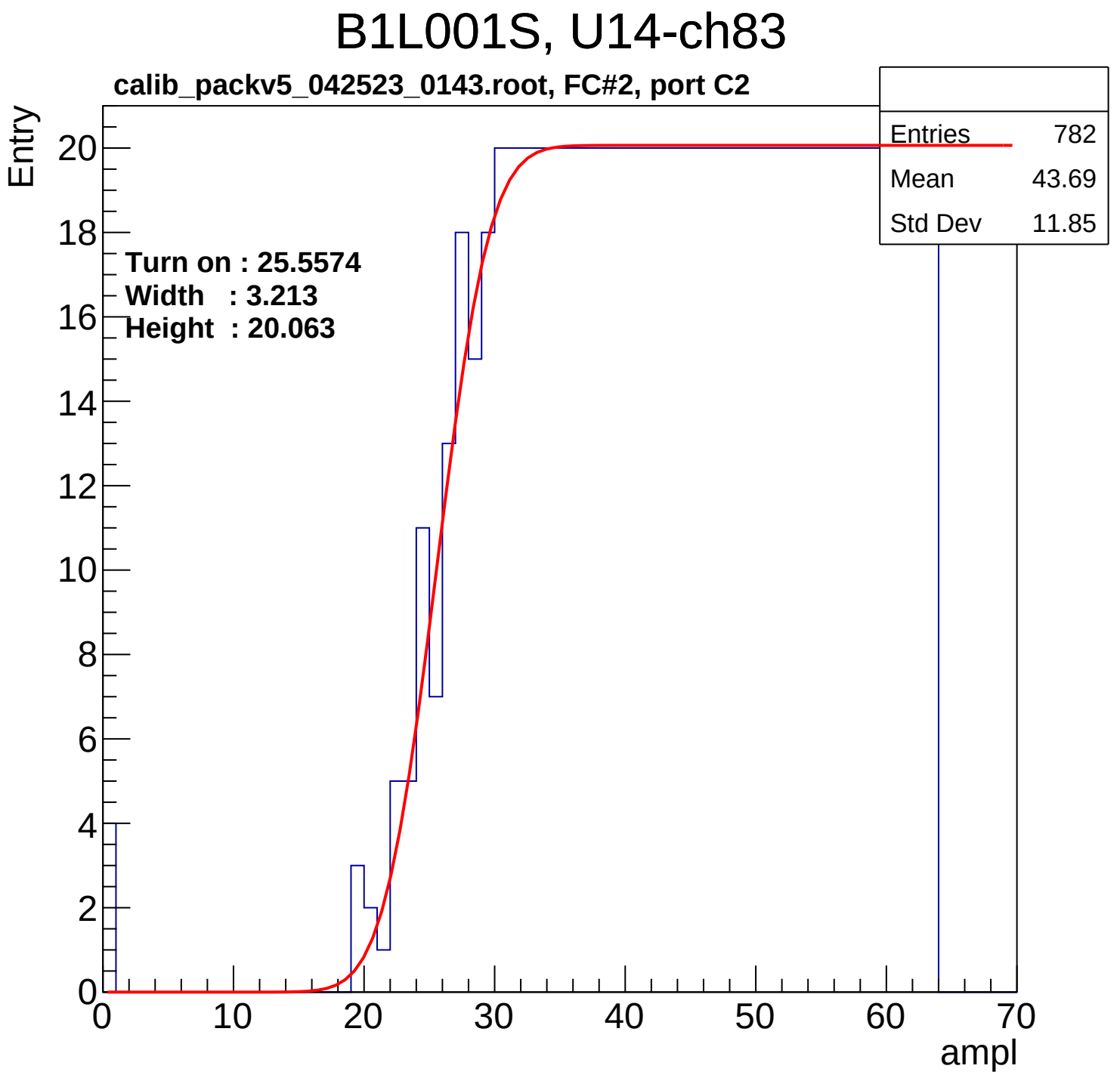

B1L001S, U14-ch78
calib_packv5_042523_0143.root, FC#2, port C2
Entries 775
Mean 43.93
Std Dev 11.65
Turn on : 25.7162
Width : 1.708
Height : 19.963
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

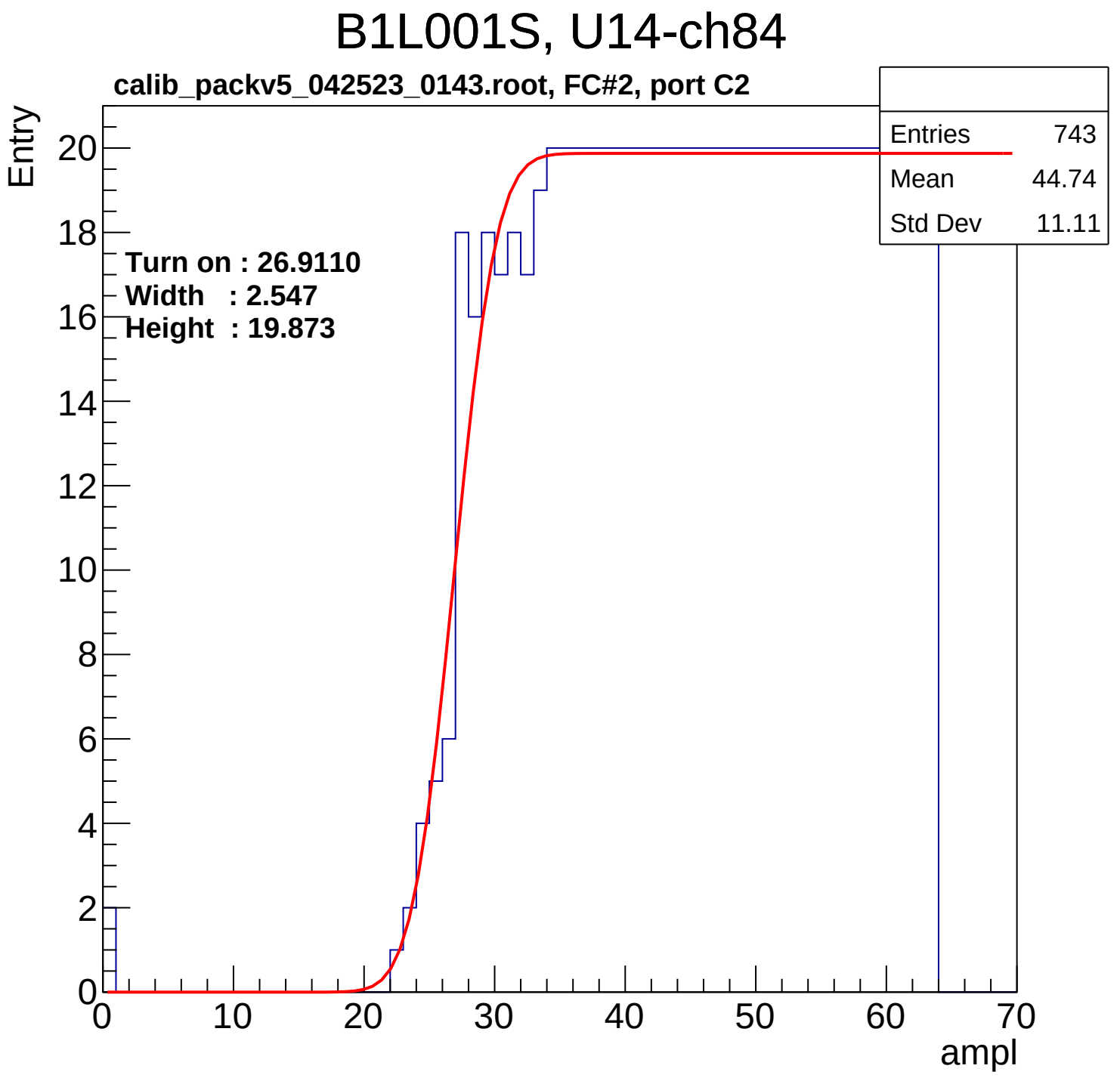

B1L001S, U14-ch79
calib_packv5_042523_0143.root, FC#2, port C2
Entries 773
Mean 43.98
Std Dev 11.59
Turn on : 25.6478
Width : 3.440
Height : 20.093
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

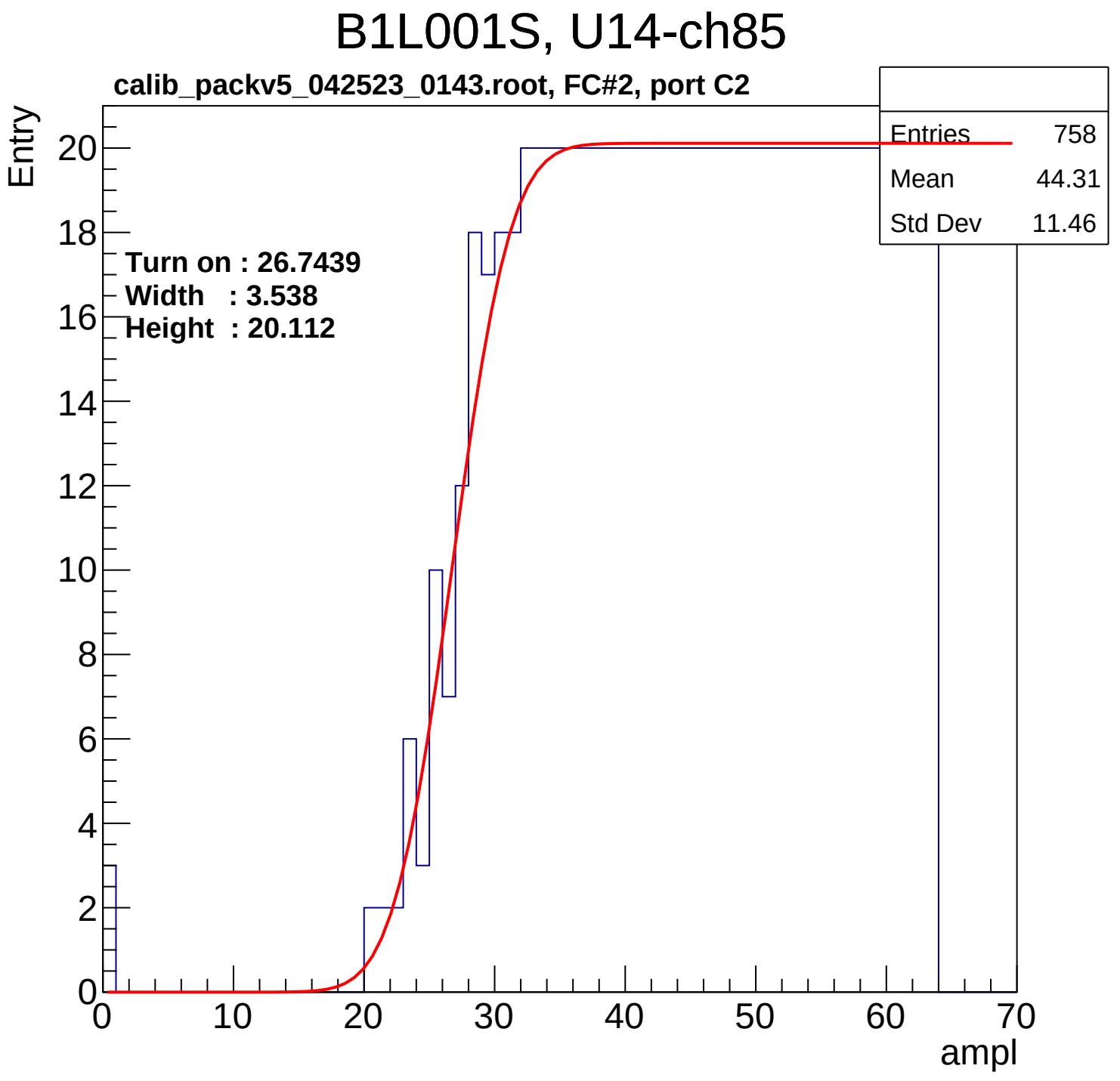

B1L001S, U14-ch80
calib_packv5_042523_0143.root, FC#2, port C2
Entries 782
Mean 43.76
Std Dev 11.73
Turn on : 25.0452
Width : 1.623
Height : 19.872
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

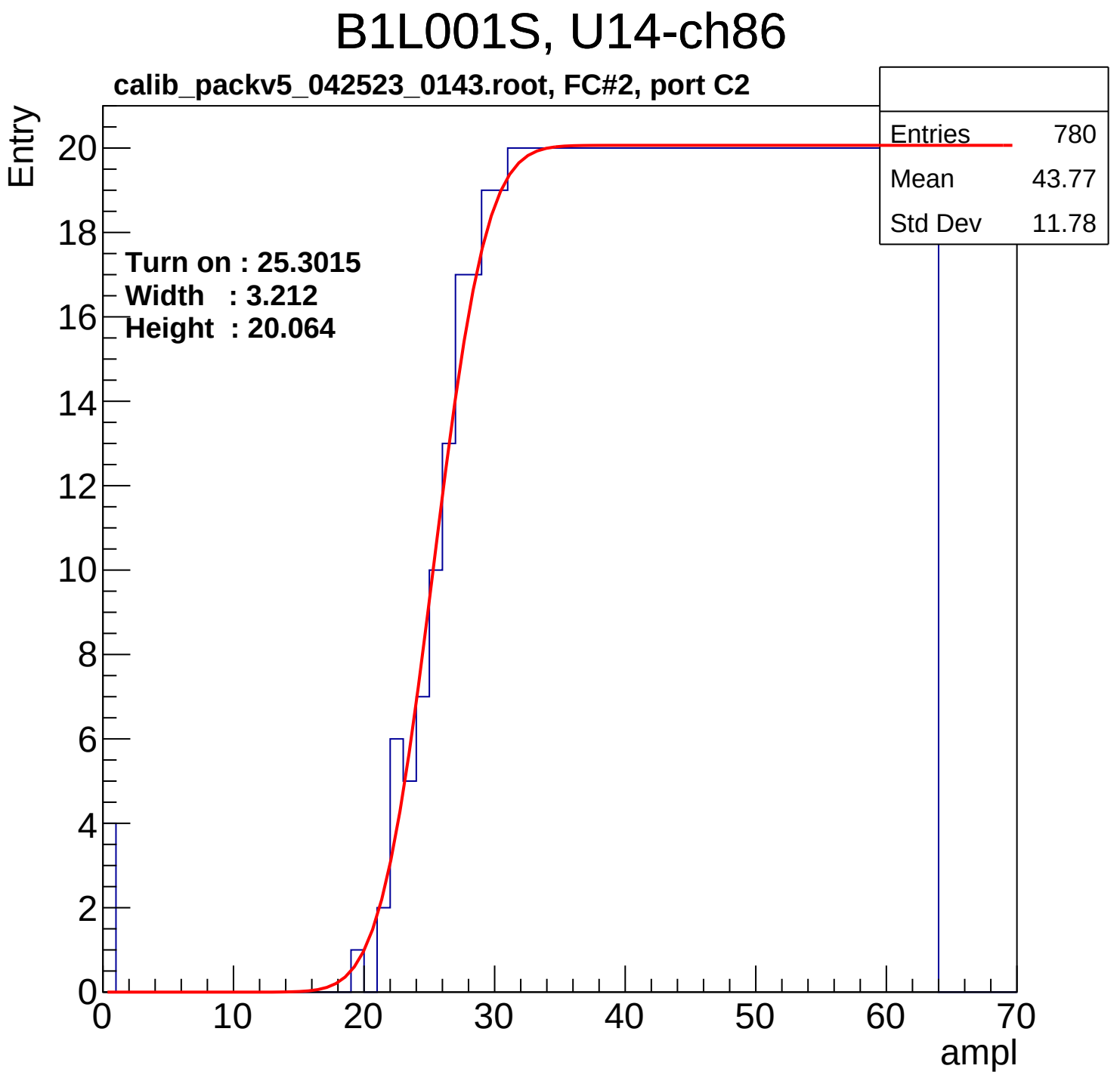

B1L001S, U14-ch81
calib_packv5_042523_0143.root, FC#2, port C2
Entries 734
Mean 44.96
Std Dev 11.05
Turn on : 27.4500
Width : 2.411
Height : 19.980
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

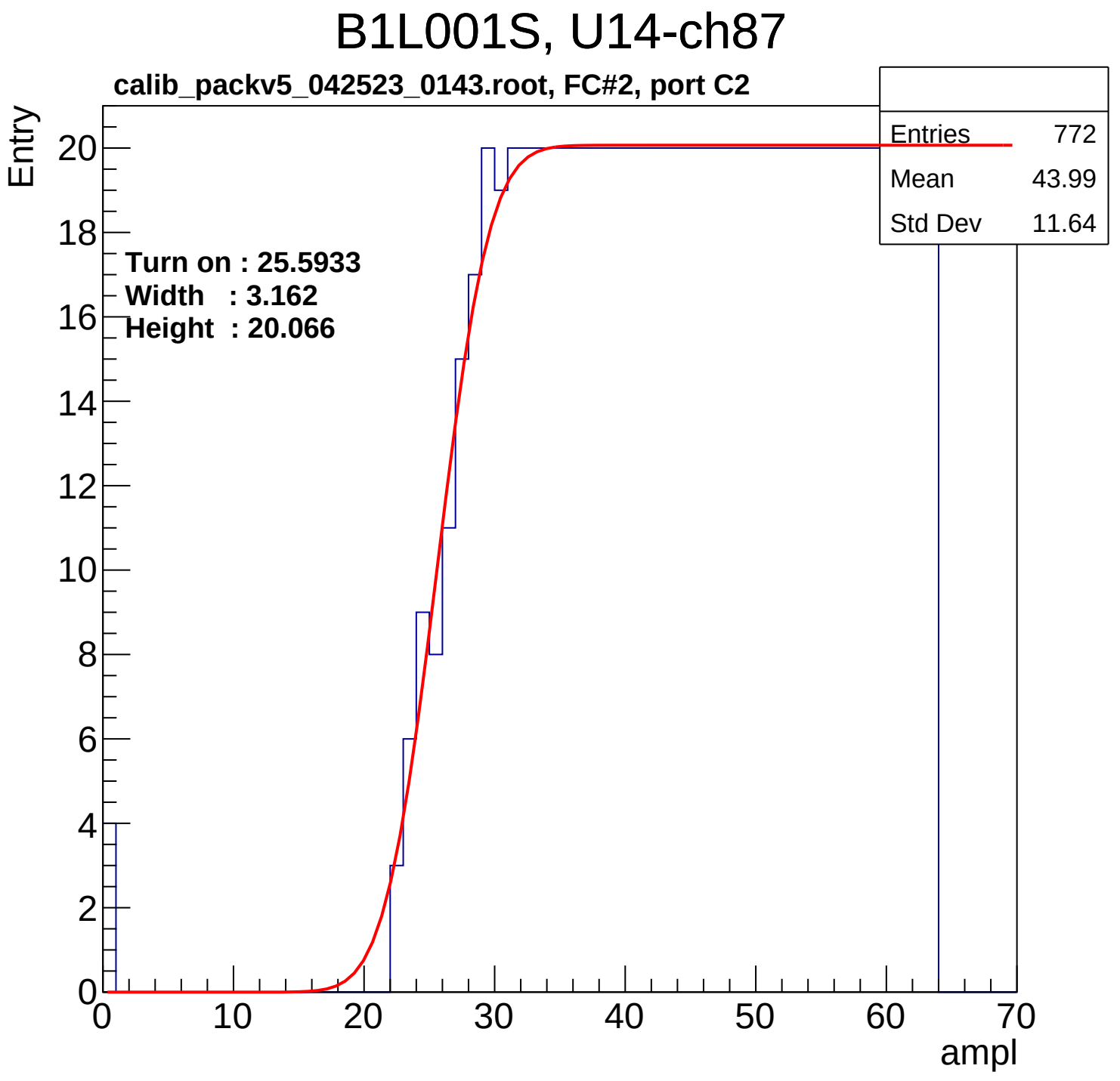

B1L001S, U14-ch82
calib_packv5_042523_0143.root, FC#2, port C2
Entries 752
Mean 44.5
Std Dev 11.3
Turn on : 26.6611
Width : 2.228
Height : 19.968
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

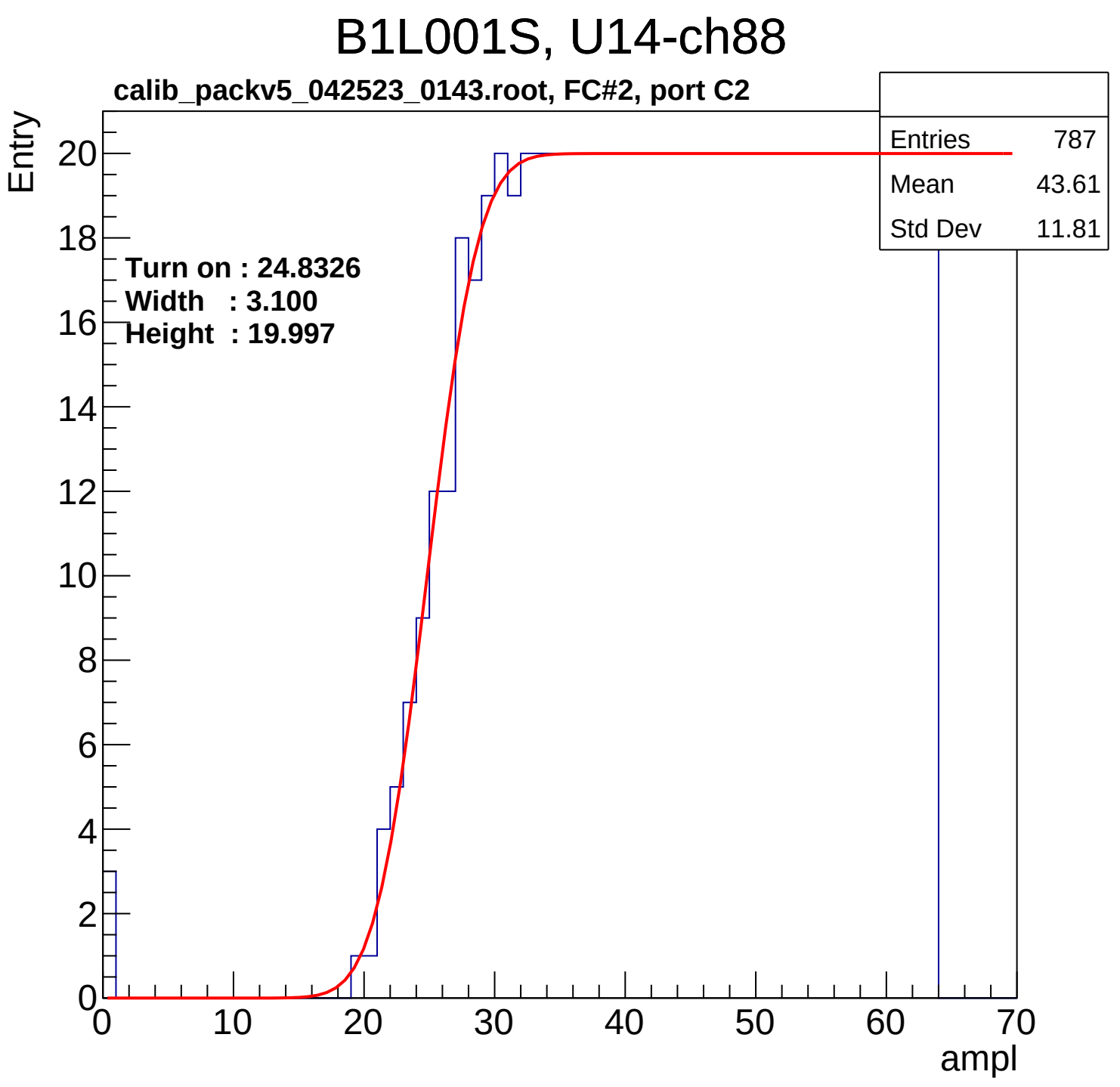

B1L001S, U14-ch83
calib_packv5_042523_0143.root, FC#2, port C2
Entries 782
Mean 43.69
Std Dev 11.85
Turn on : 25.5574
Width : 3.213
Height : 20.063
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

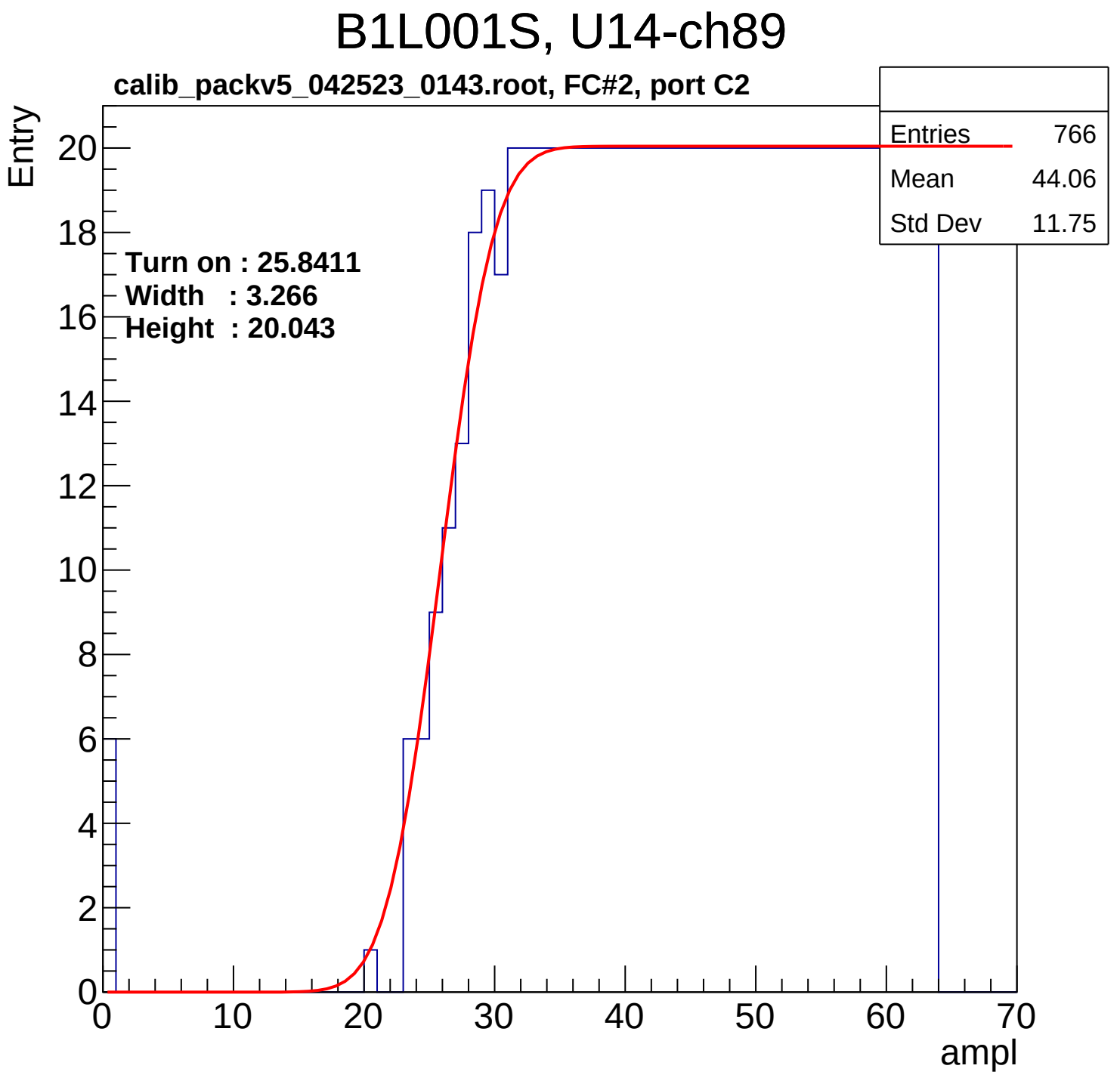

B1L001S, U14-ch84
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.74
Std Dev 11.11
Turn on : 26.9110
Width : 2.547
Height : 19.873
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

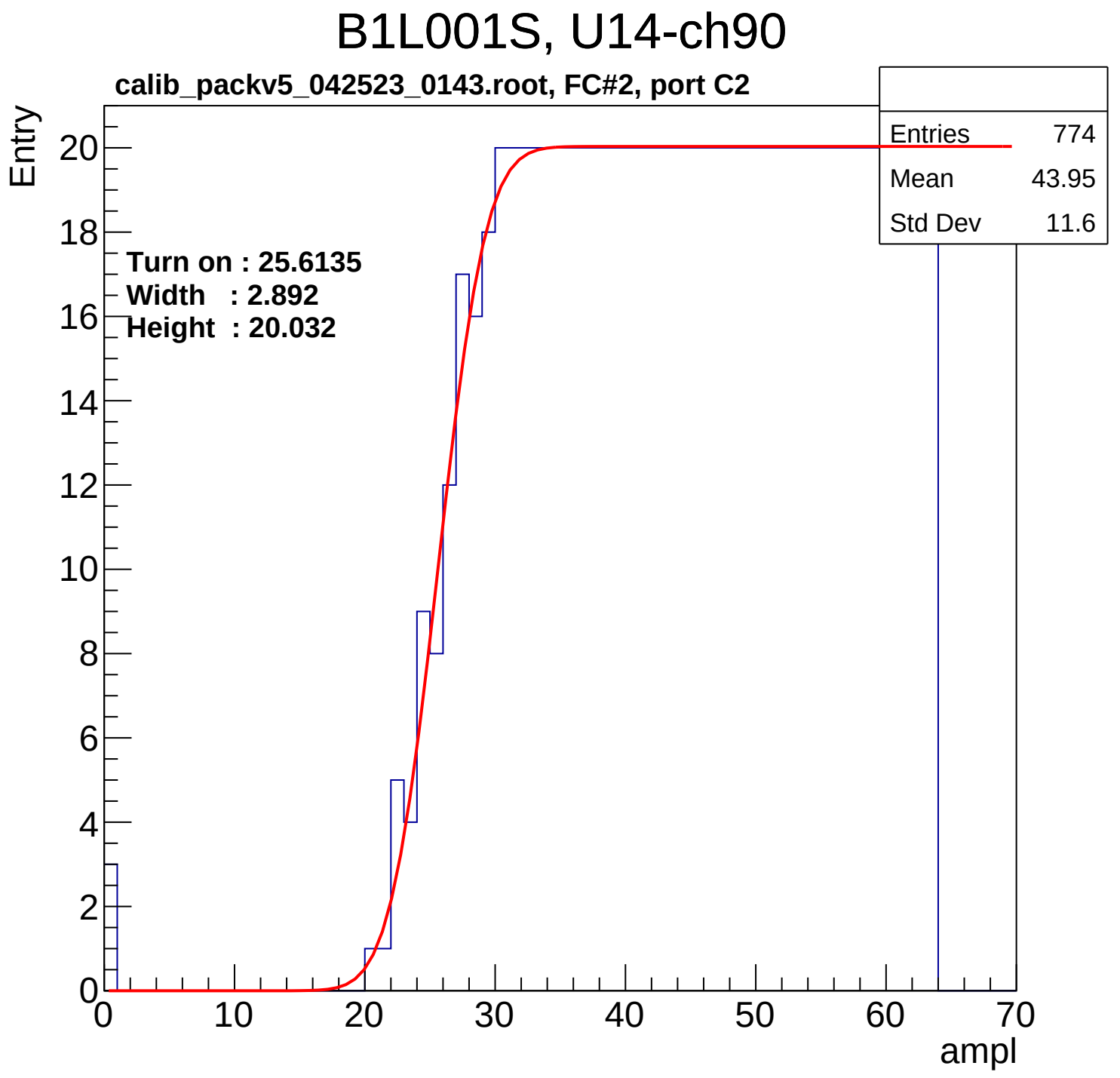

B1L001S, U14-ch85
calib_packv5_042523_0143.root, FC#2, port C2
Entries 758
Mean 44.31
Std Dev 11.46
Turn on : 26.7439
Width : 3.538
Height : 20.112
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

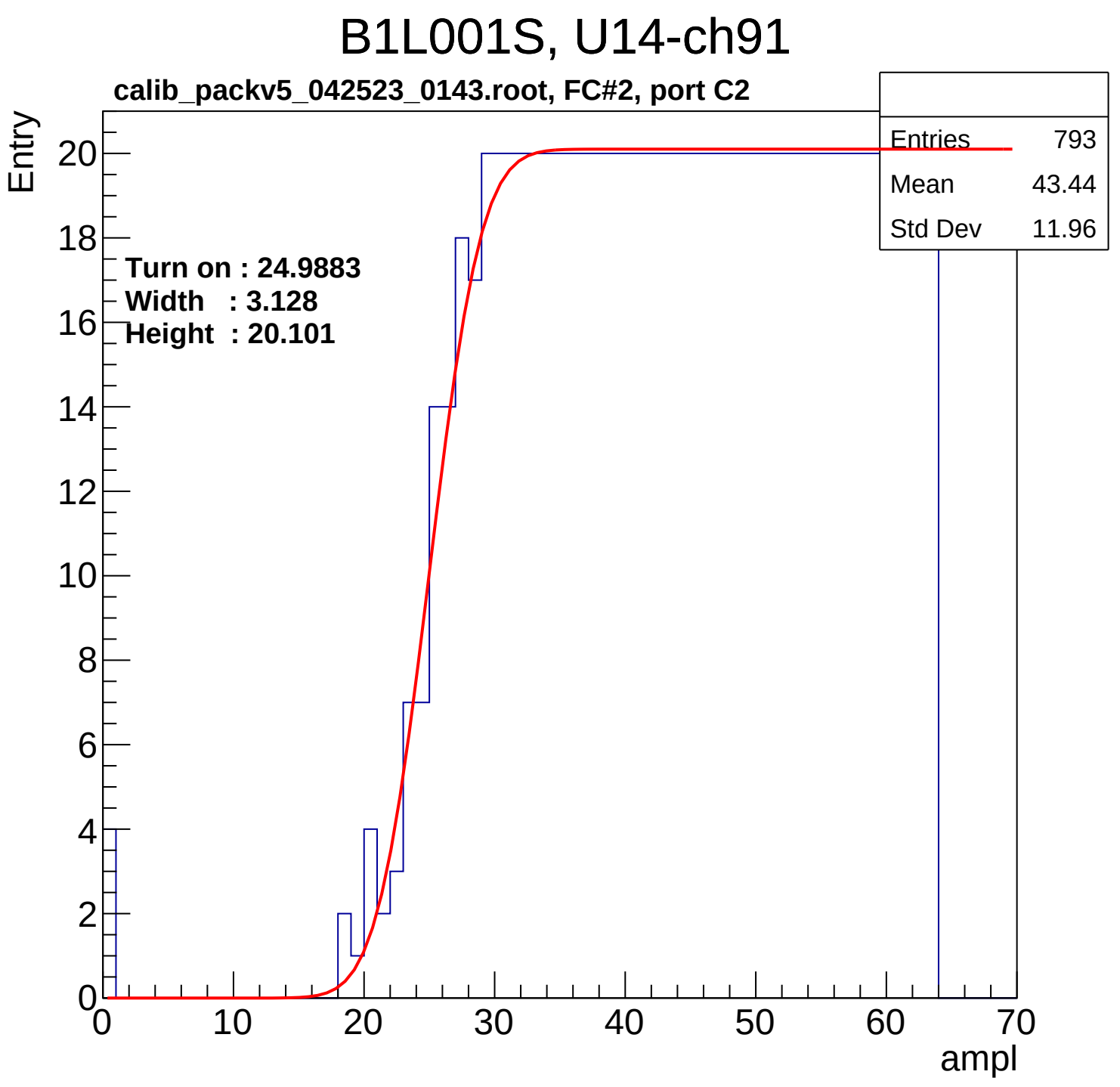

B1L001S, U14-ch86
calib_packv5_042523_0143.root, FC#2, port C2
Entries 780
Mean 43.77
Std Dev 11.78
Turn on : 25.3015
Width : 3.212
Height : 20.064
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

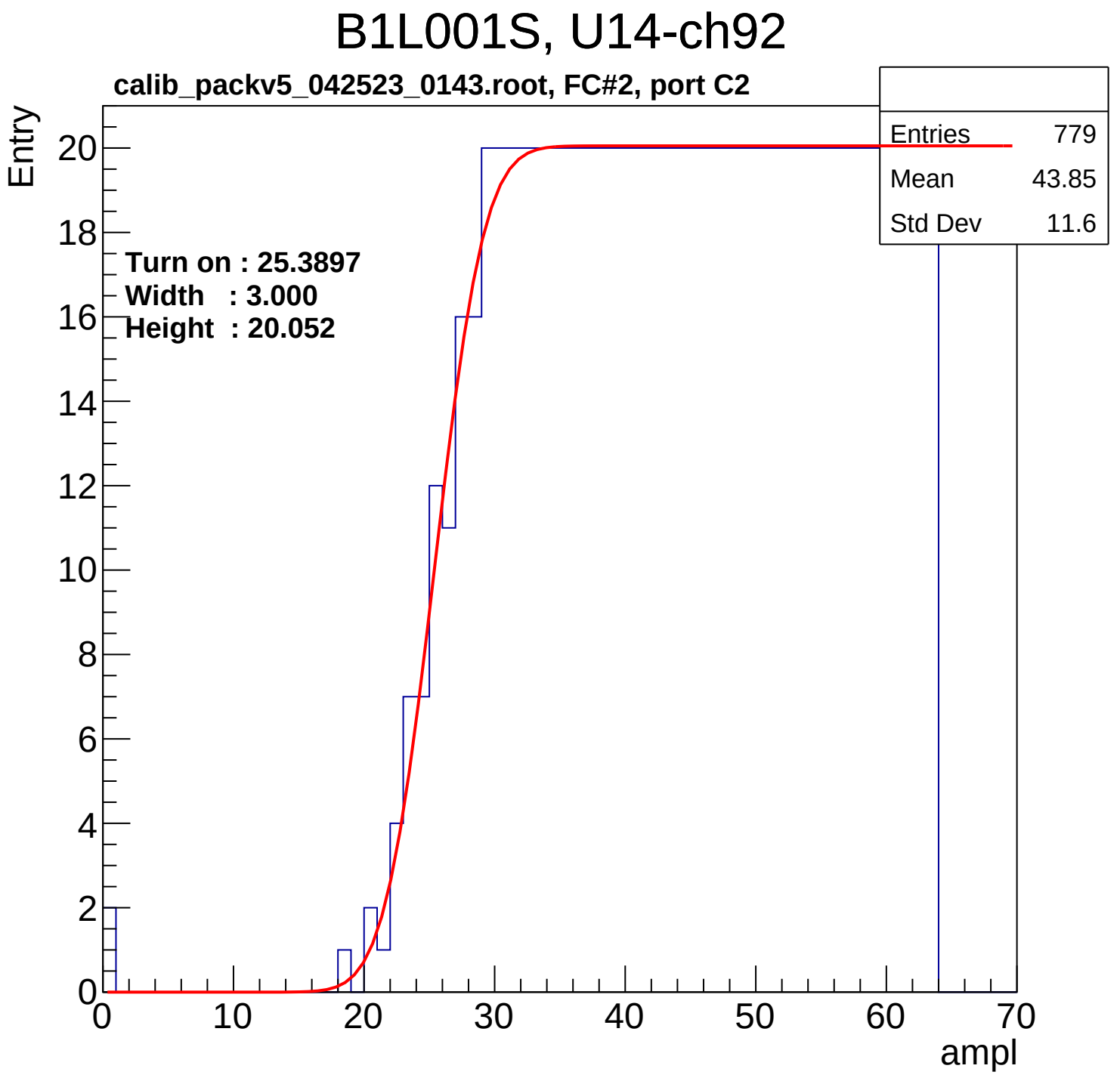

B1L001S, U14-ch87
calib_packv5_042523_0143.root, FC#2, port C2
Entries 772
Mean 43.99
Std Dev 11.64
Turn on : 25.5933
Width : 3.162
Height : 20.066
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

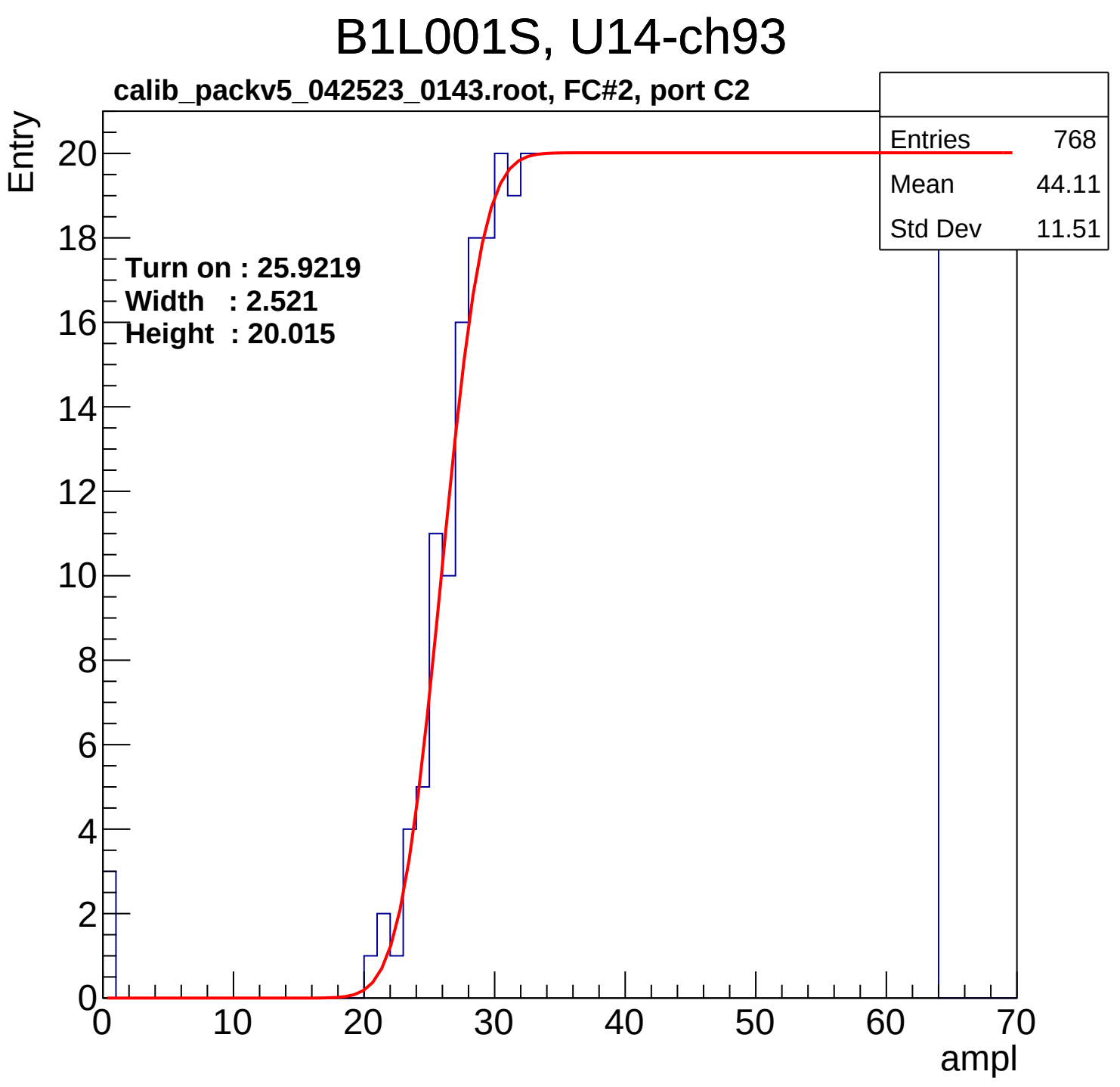

B1L001S, U14-ch88
calib_packv5_042523_0143.root, FC#2, port C2
Entries 787
Mean 43.61
Std Dev 11.81
Turn on : 24.8326
Width : 3.100
Height : 19.997
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

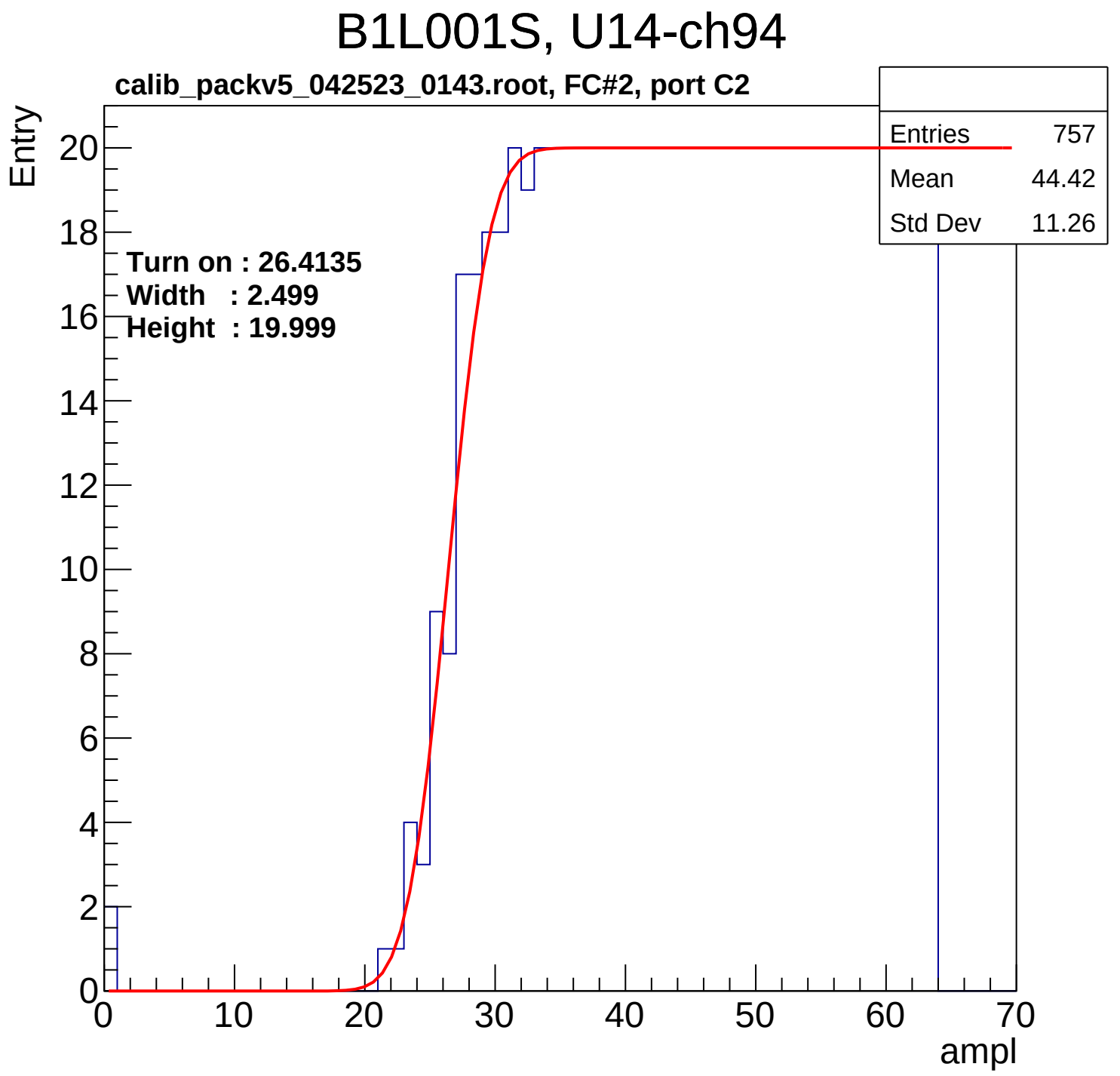

B1L001S, U14-ch89
calib_packv5_042523_0143.root, FC#2, port C2
Entries 766
Mean 44.06
Std Dev 11.75
Turn on : 25.8411
Width : 3.266
Height : 20.043
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

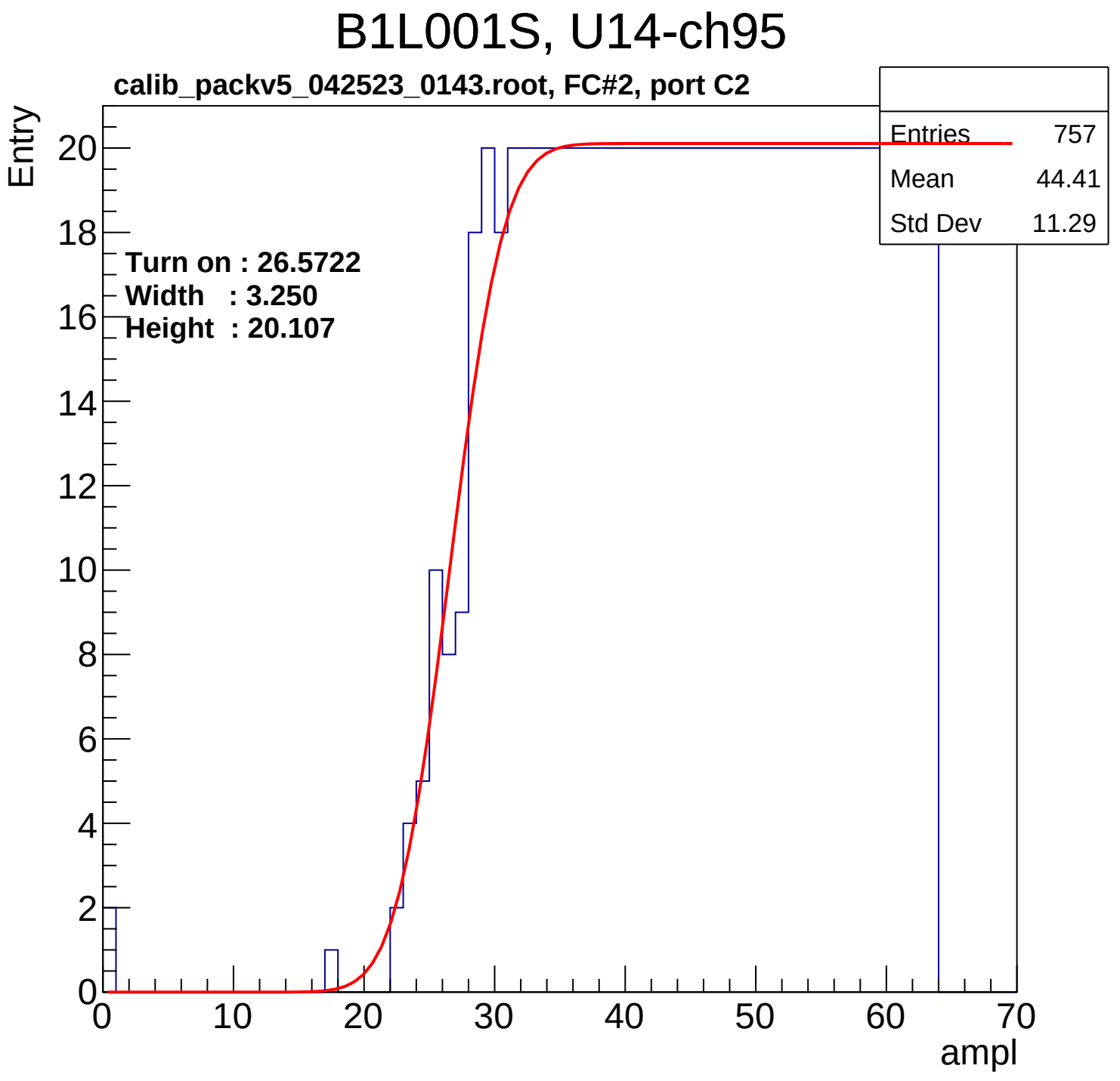

B1L001S, U14-ch90
calib_packv5_042523_0143.root, FC#2, port C2
Entries 774
Mean 43.95
Std Dev 11.6
Turn on : 25.6135
Width : 2.892
Height : 20.032
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

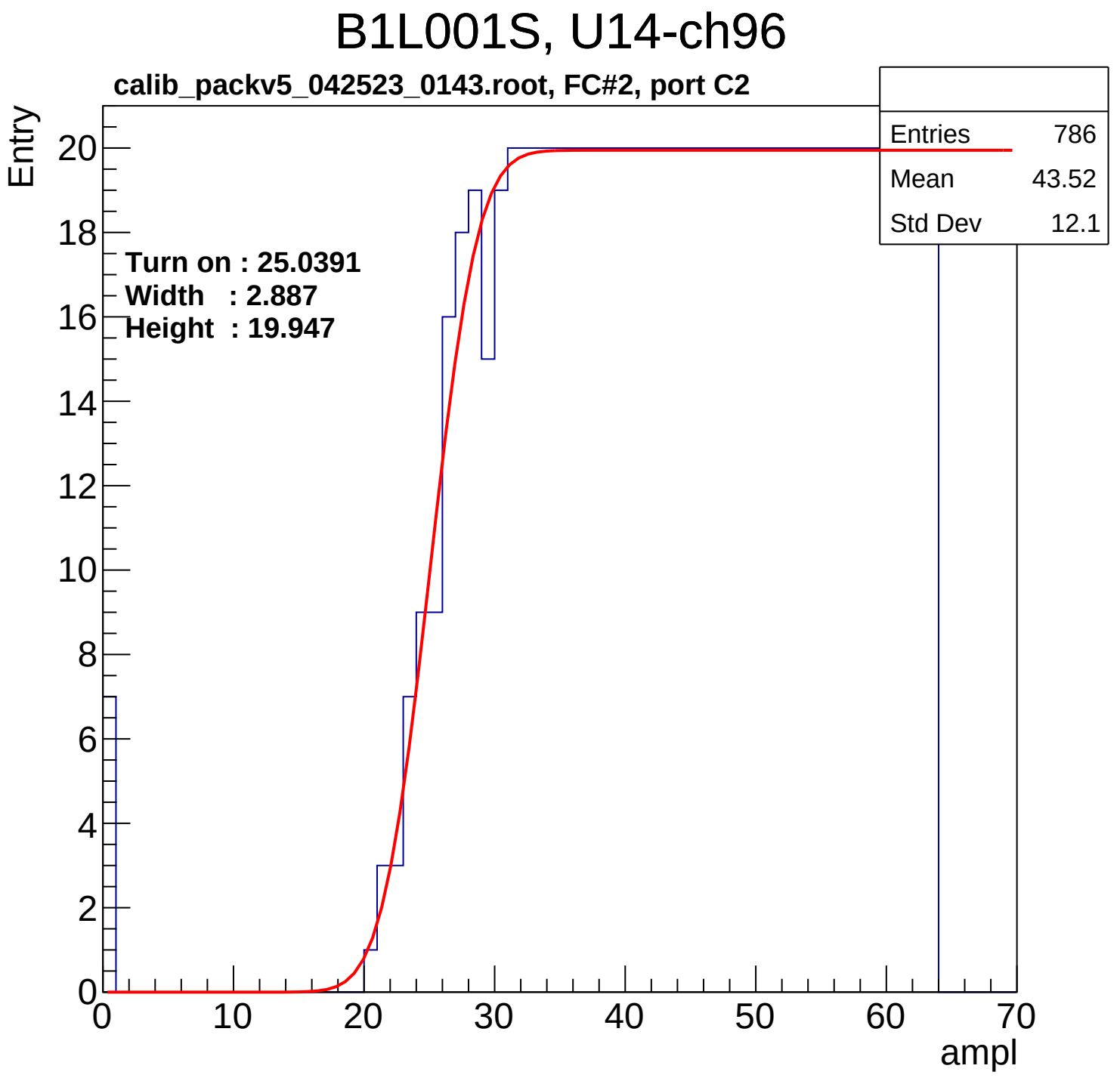

B1L001S, U14-ch91
calib_packv5_042523_0143.root, FC#2, port C2
Entries 793
Mean 43.44
Std Dev 11.96
Turn on : 24.9883
Width : 3.128
Height : 20.101
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

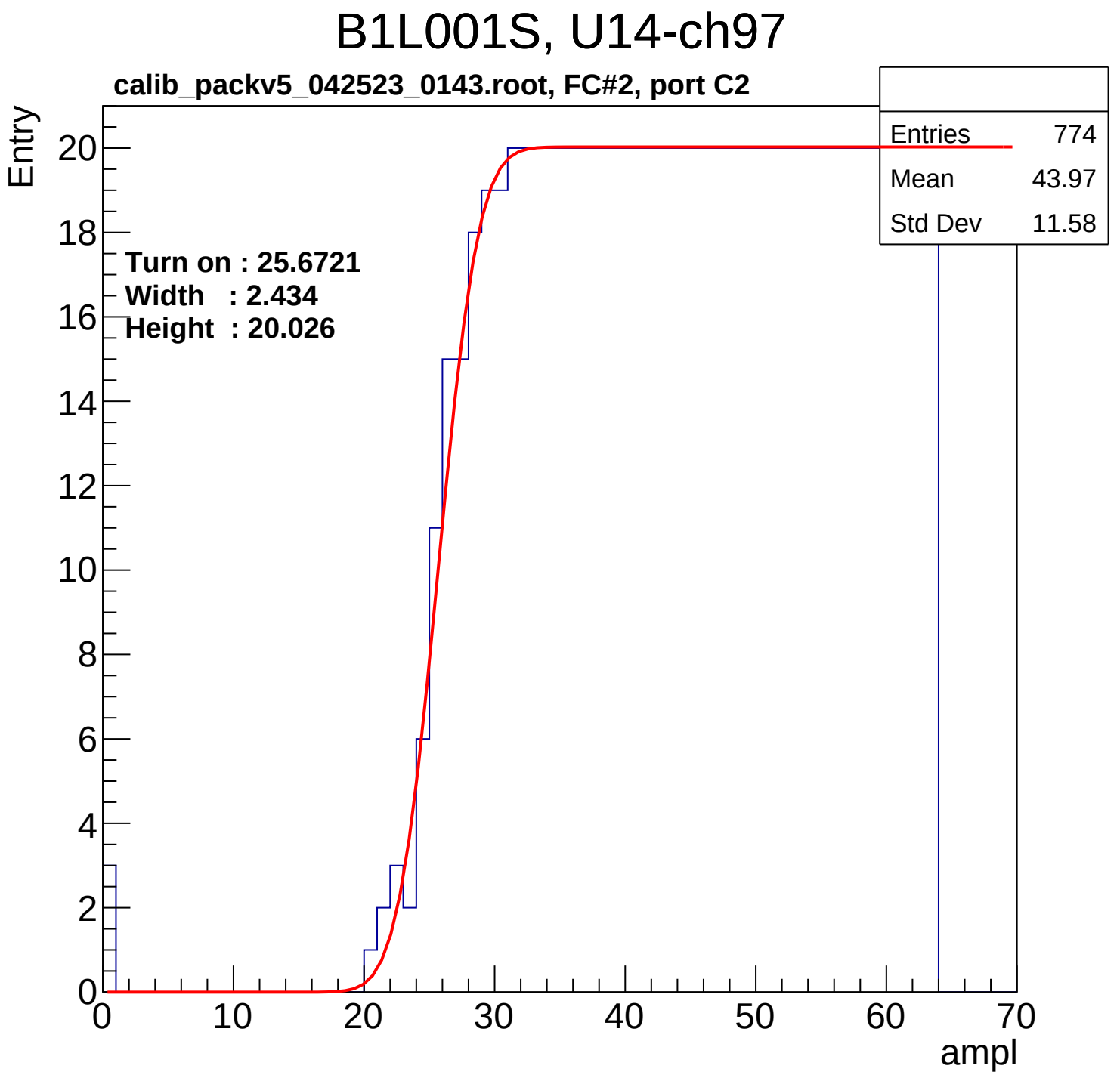

B1L001S, U14-ch92
calib_packv5_042523_0143.root, FC#2, port C2
Entries 779
Mean 43.85
Std Dev 11.6
Turn on : 25.3897
Width : 3.000
Height : 20.052
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

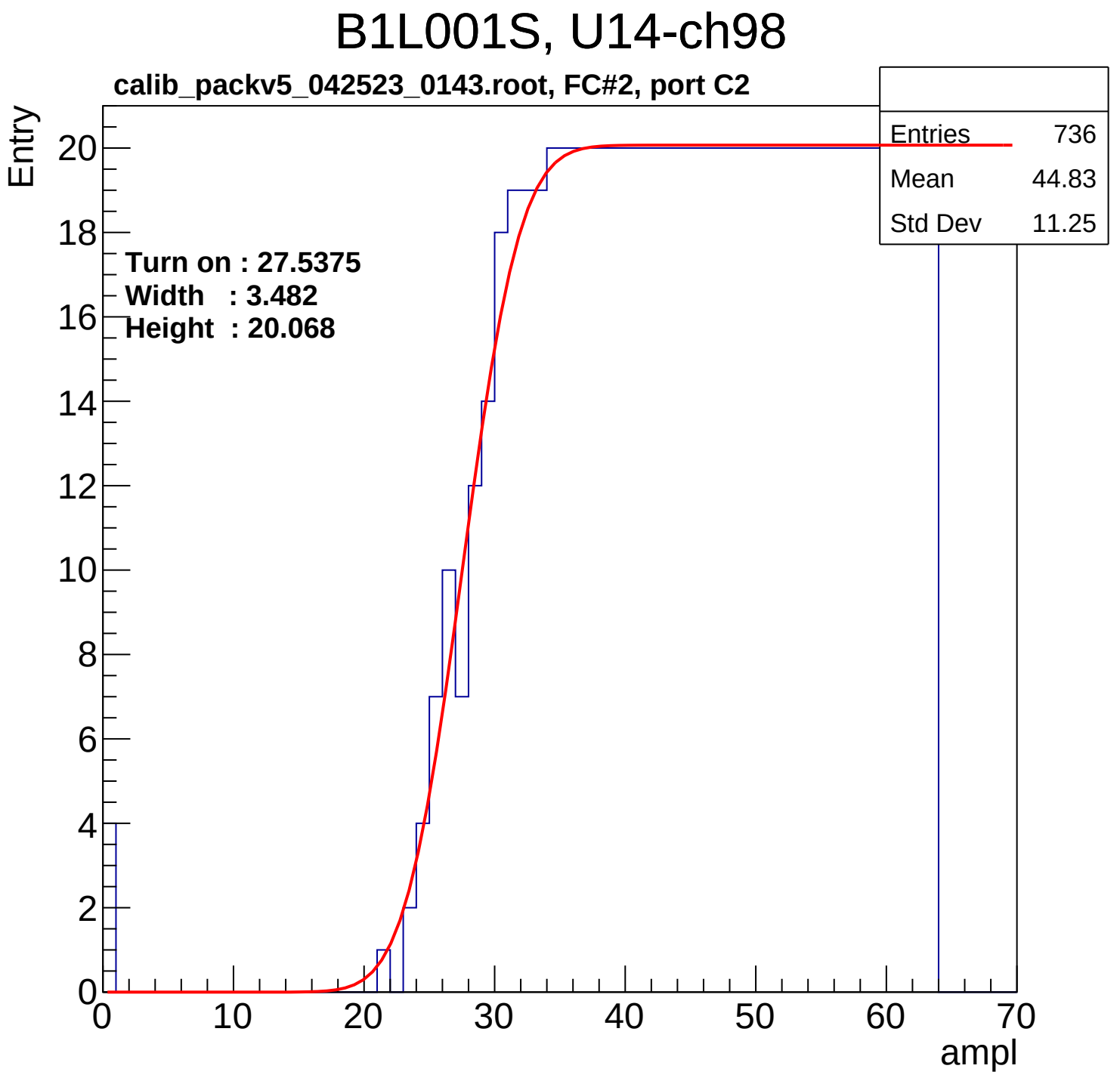

B1L001S, U14-ch93
calib_packv5_042523_0143.root, FC#2, port C2
Entries 768
Mean 44.11
Std Dev 11.51
Turn on : 25.9219
Width : 2.521
Height : 20.015
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

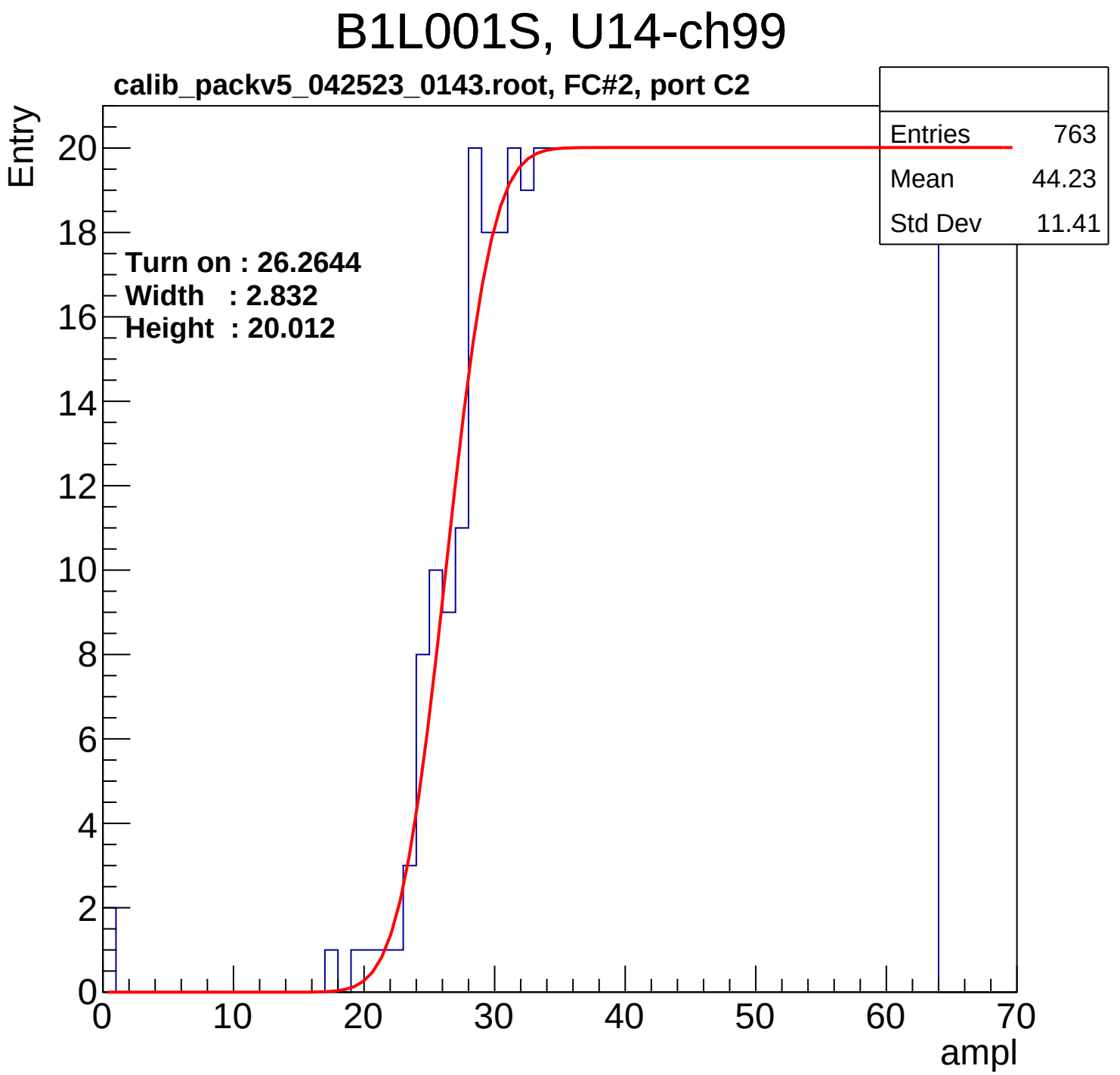

B1L001S, U14-ch94
calib_packv5_042523_0143.root, FC#2, port C2
Entries 757
Mean 44.42
Std Dev 11.26
Turn on : 26.4135
Width : 2.499
Height : 19.999
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

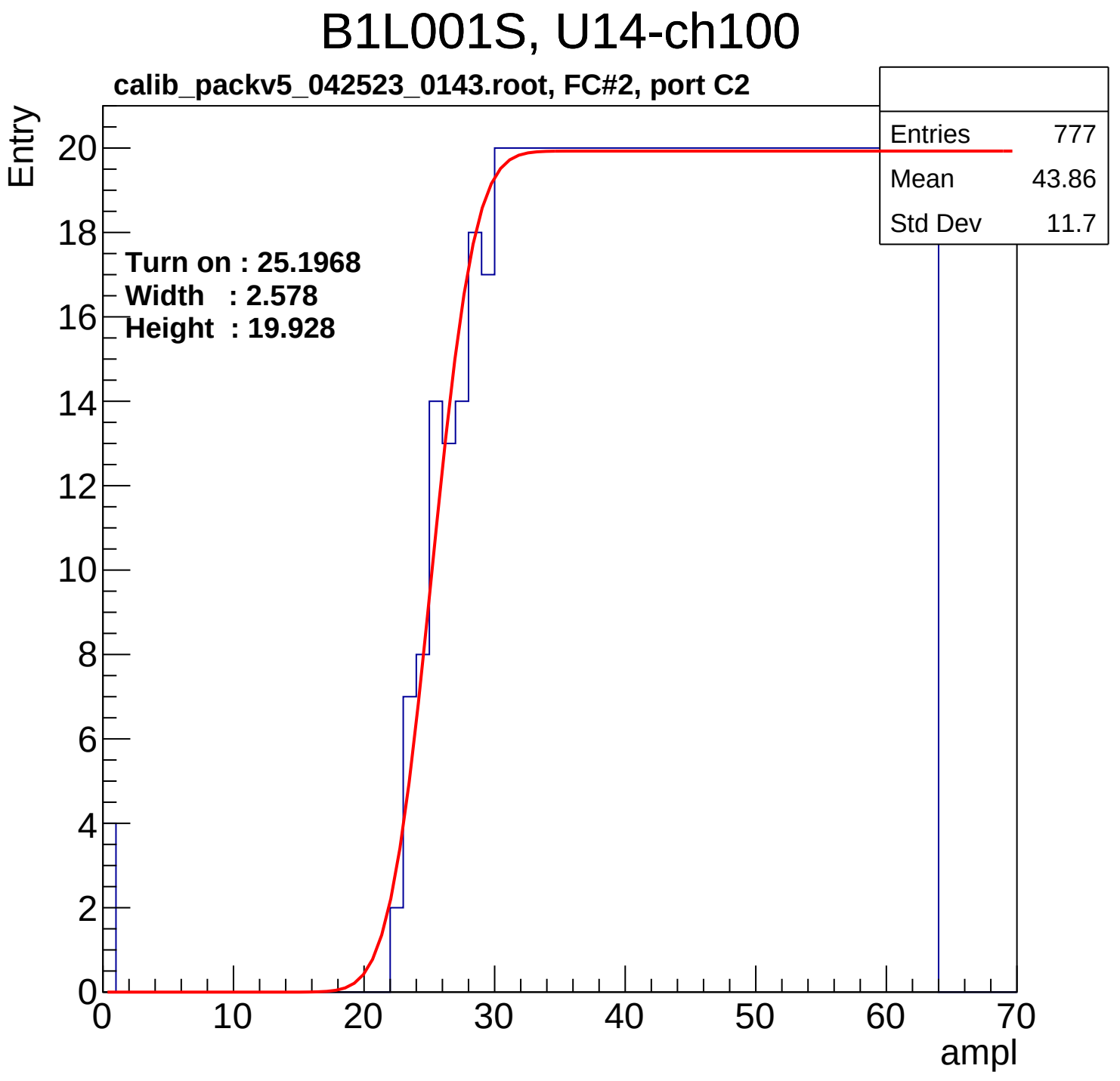

B1L001S, U14-ch95
calib_packv5_042523_0143.root, FC#2, port C2
Entries 757
Mean 44.41
Std Dev 11.29
Turn on : 26.5722
Width : 3.250
Height : 20.107
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

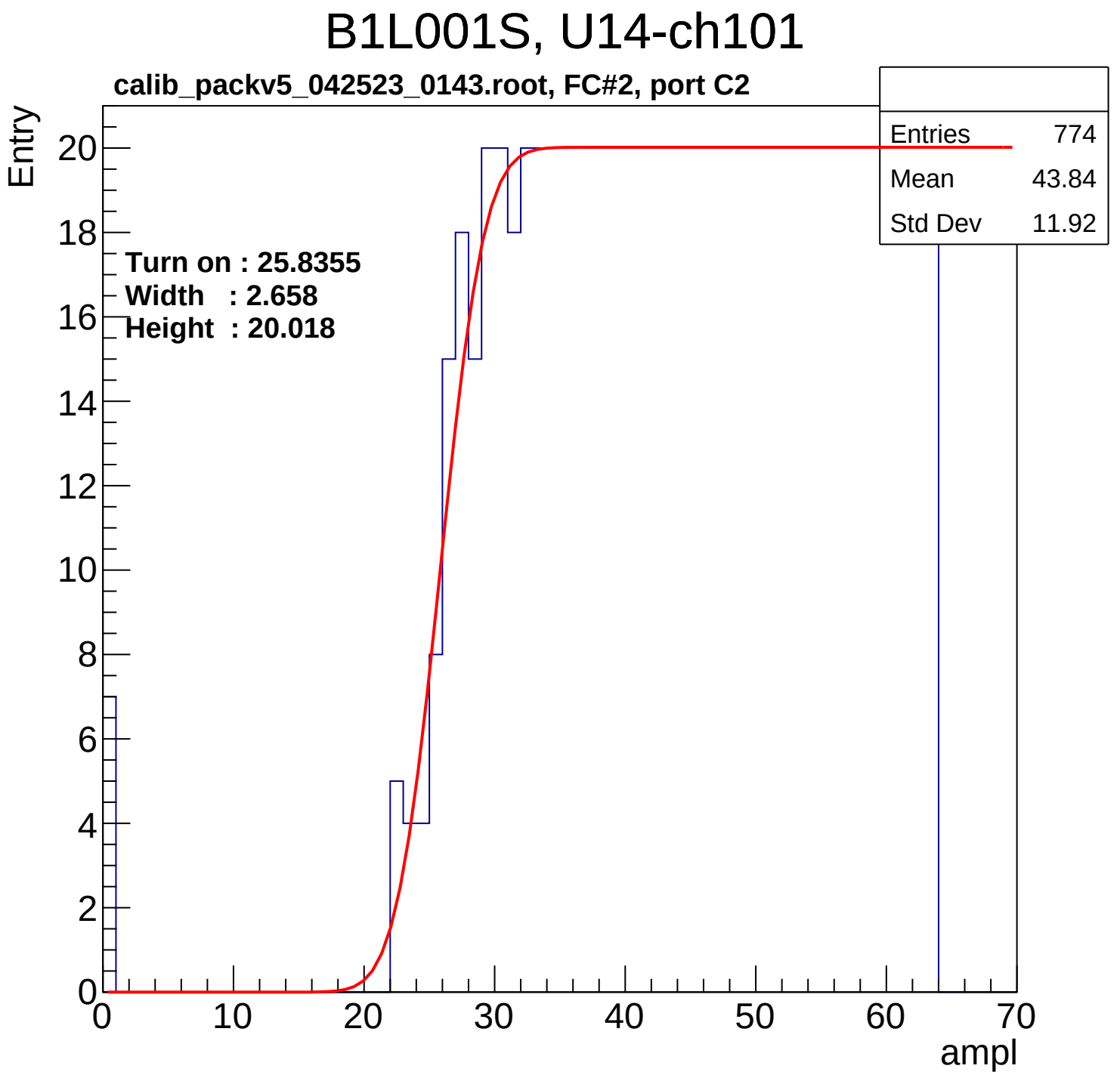

B1L001S, U14-ch96
calib_packv5_042523_0143.root, FC#2, port C2
Entries 786
Mean 43.52
Std Dev 12.1
Turn on : 25.0391
Width : 2.887
Height : 19.947
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

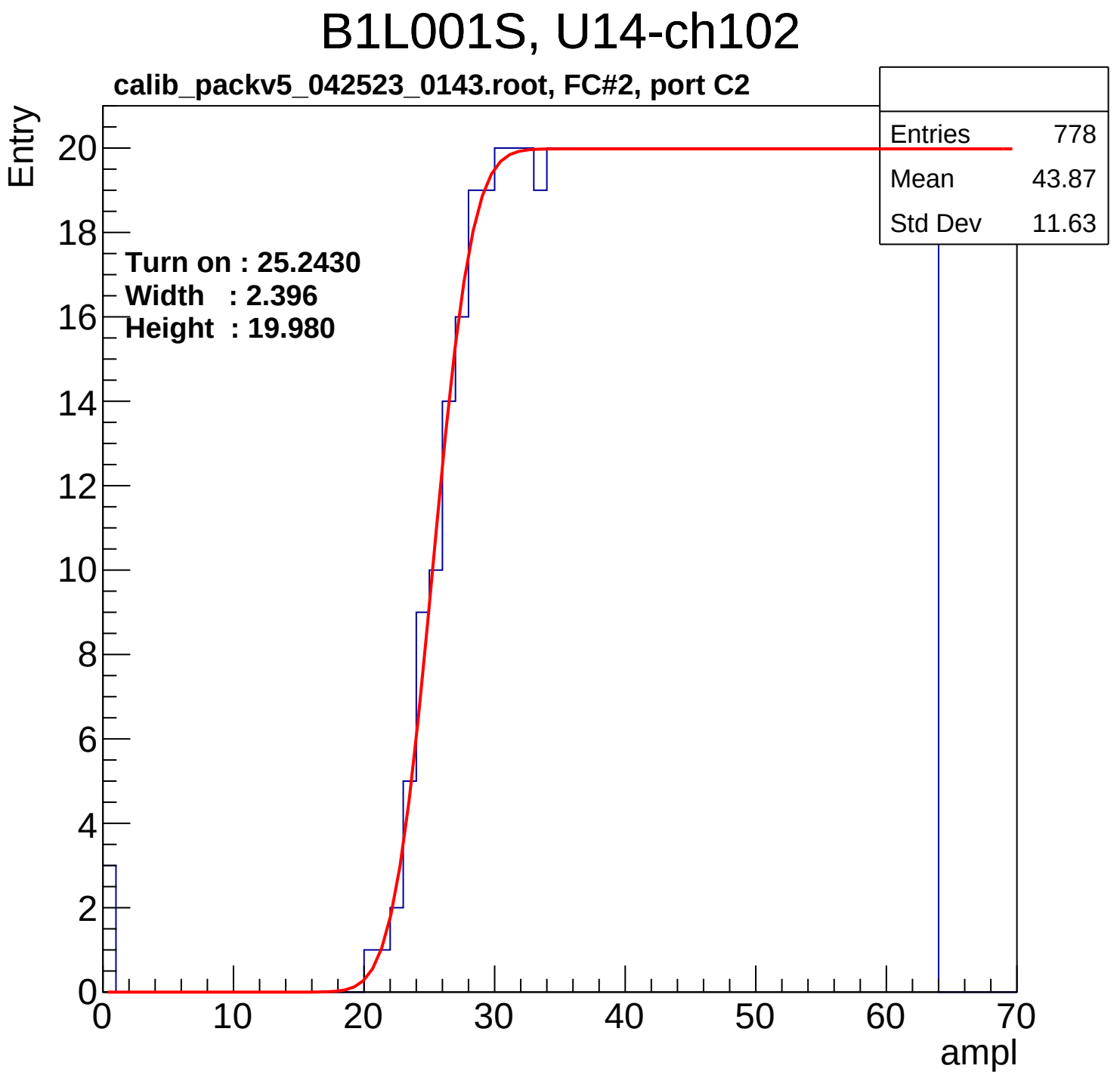

B1L001S, U14-ch97
calib_packv5_042523_0143.root, FC#2, port C2
Entries 774
Mean 43.97
Std Dev 11.58
Turn on : 25.6721
Width : 2.434
Height : 20.026
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

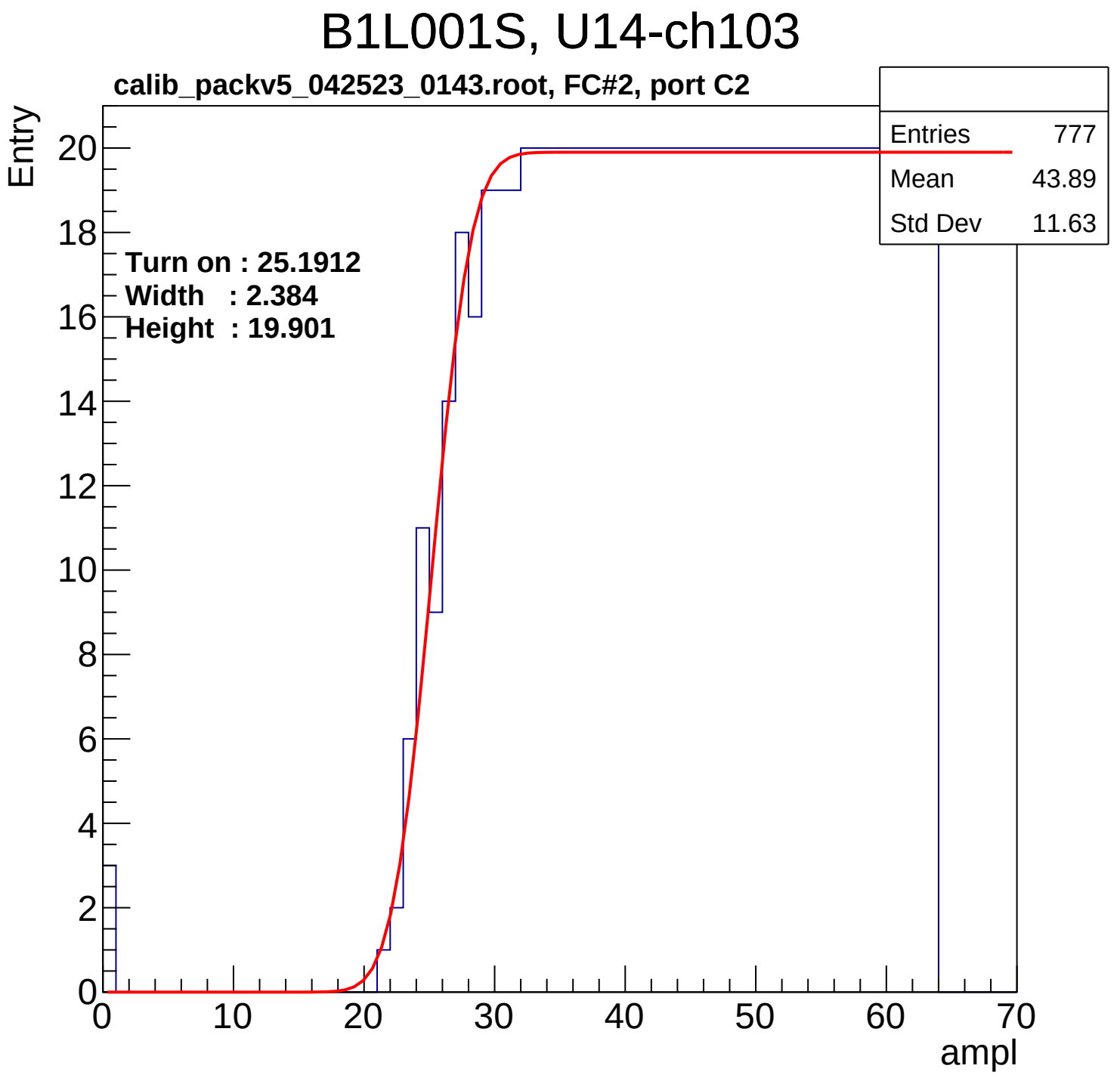

B1L001S, U14-ch98
calib_packv5_042523_0143.root, FC#2, port C2
Entries 736
Mean 44.83
Std Dev 11.25
Turn on : 27.5375
Width : 3.482
Height : 20.068
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

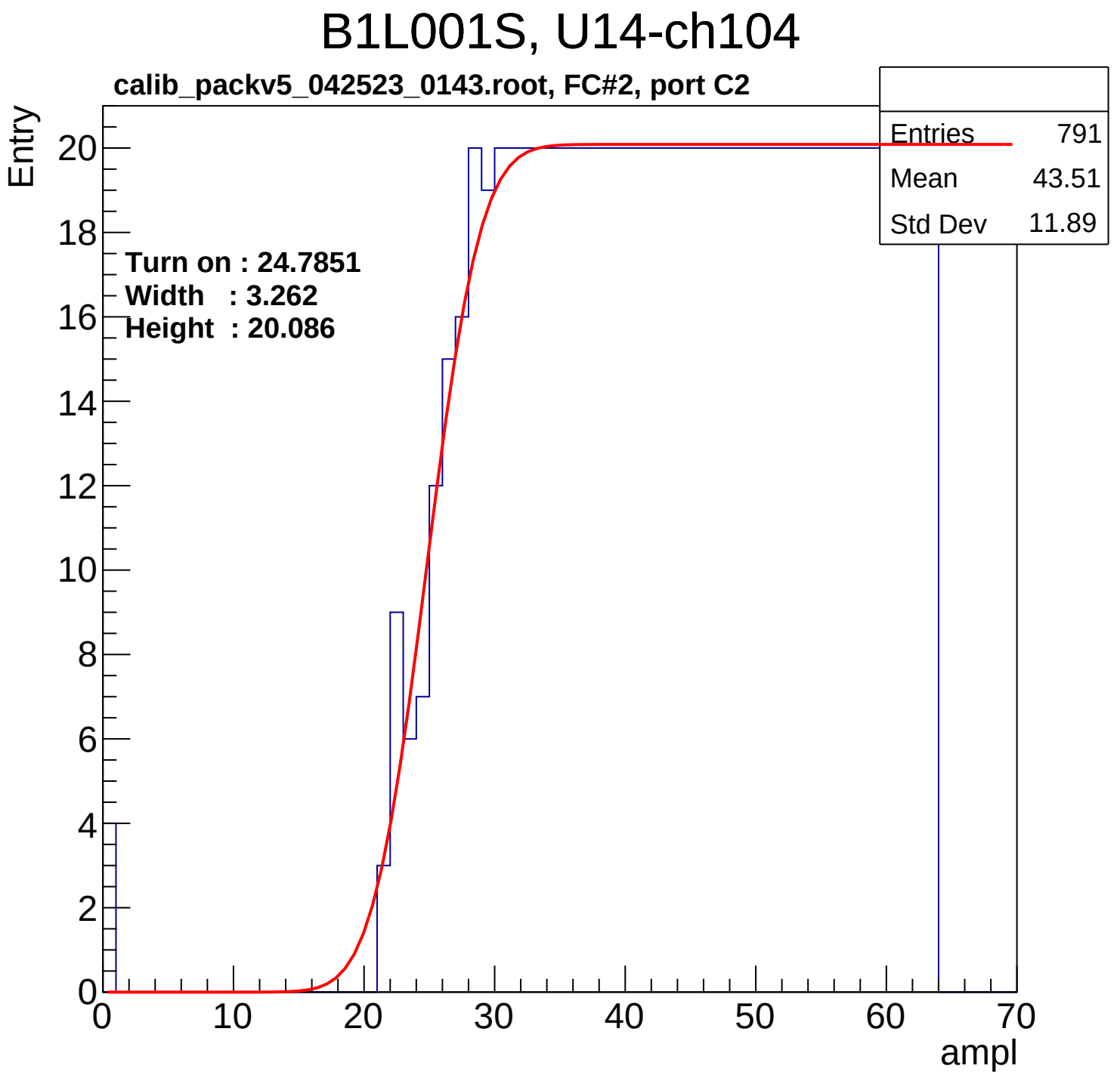

B1L001S, U14-ch99
calib_packv5_042523_0143.root, FC#2, port C2
Entries 763
Mean 44.23
Std Dev 11.41
Turn on : 26.2644
Width : 2.832
Height : 20.012
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

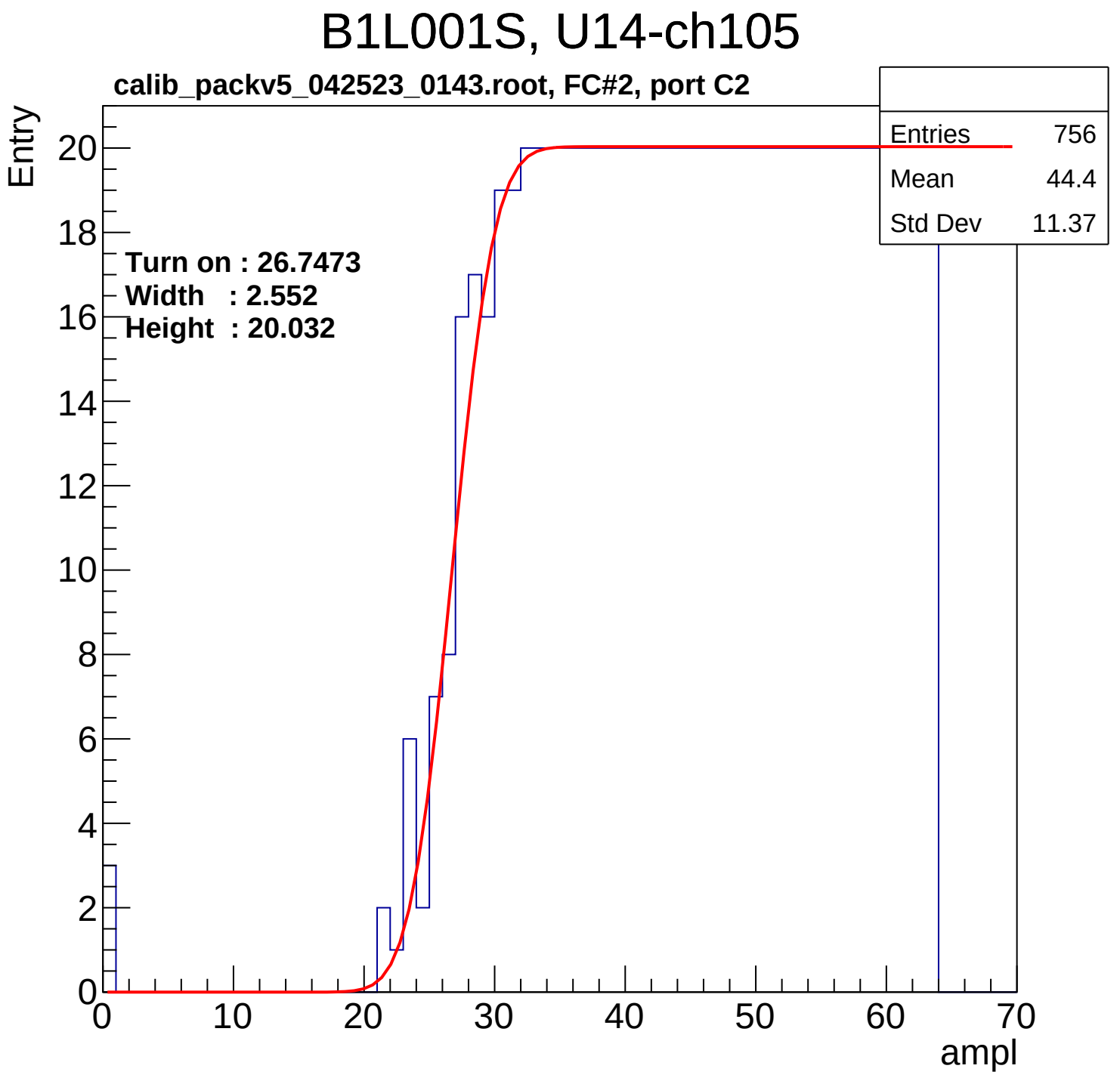

B1L001S, U14-ch100
calib_packv5_042523_0143.root, FC#2, port C2
Entries 777
Mean 43.86
Std Dev 11.7
Turn on : 25.1968
Width : 2.578
Height : 19.928
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

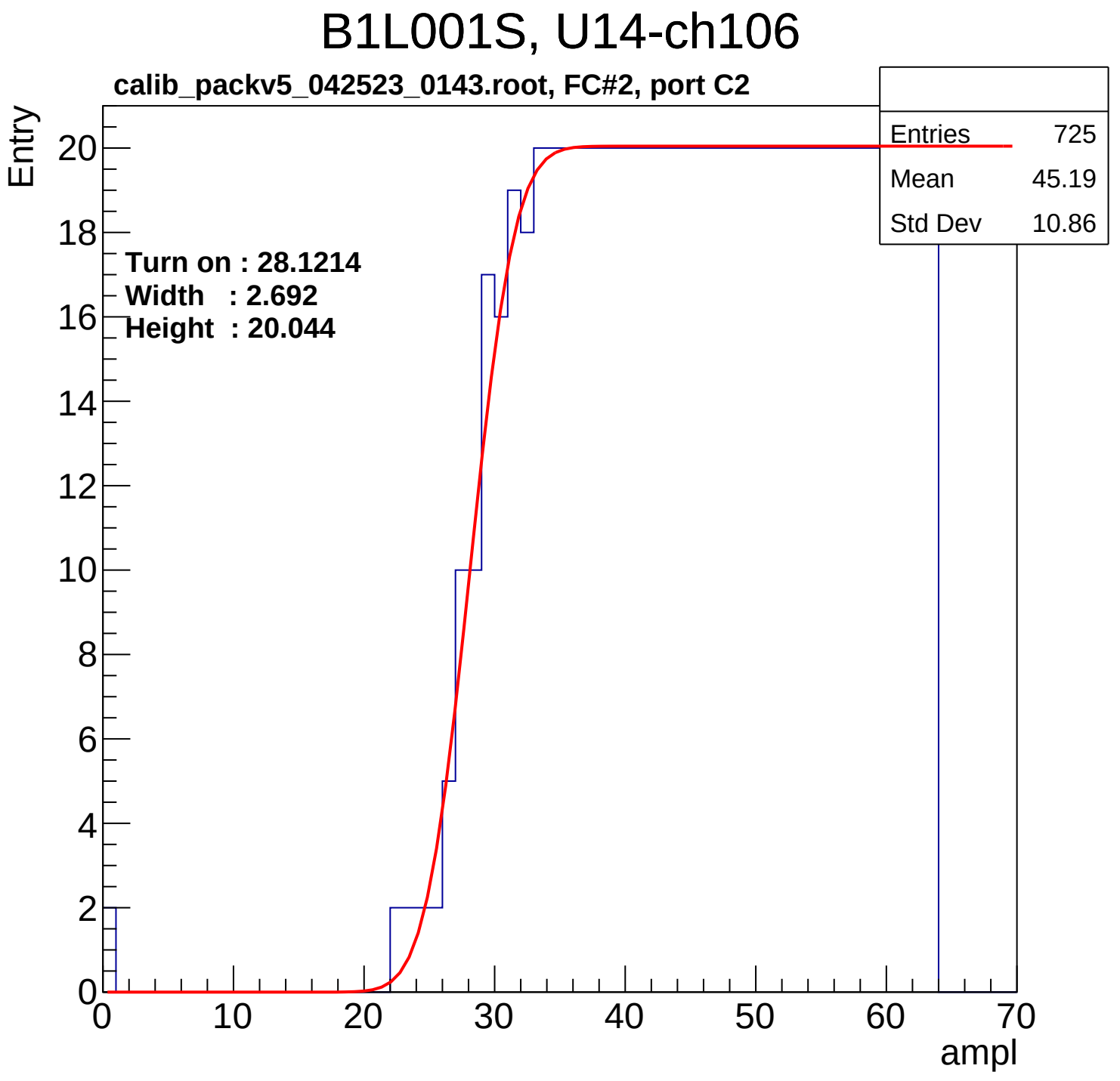

B1L001S, U14-ch101
calib_packv5_042523_0143.root, FC#2, port C2
Entries 774
Mean 43.84
Std Dev 11.92
Turn on : 25.8355
Width : 2.658
Height : 20.018
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

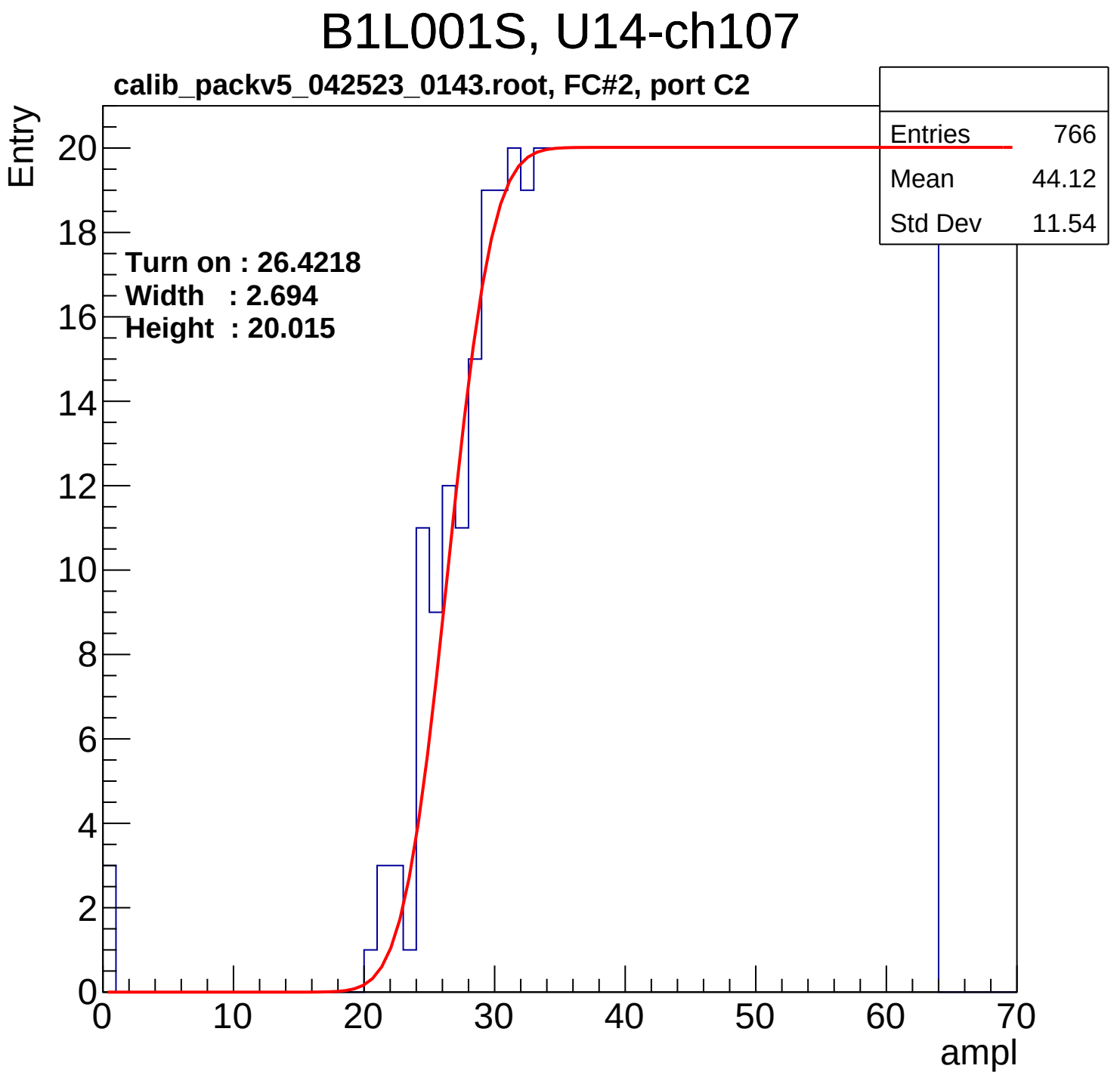

B1L001S, U14-ch102
calib_packv5_042523_0143.root, FC#2, port C2
Entries 778
Mean 43.87
Std Dev 11.63
Turn on : 25.2430
Width : 2.396
Height : 19.980
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

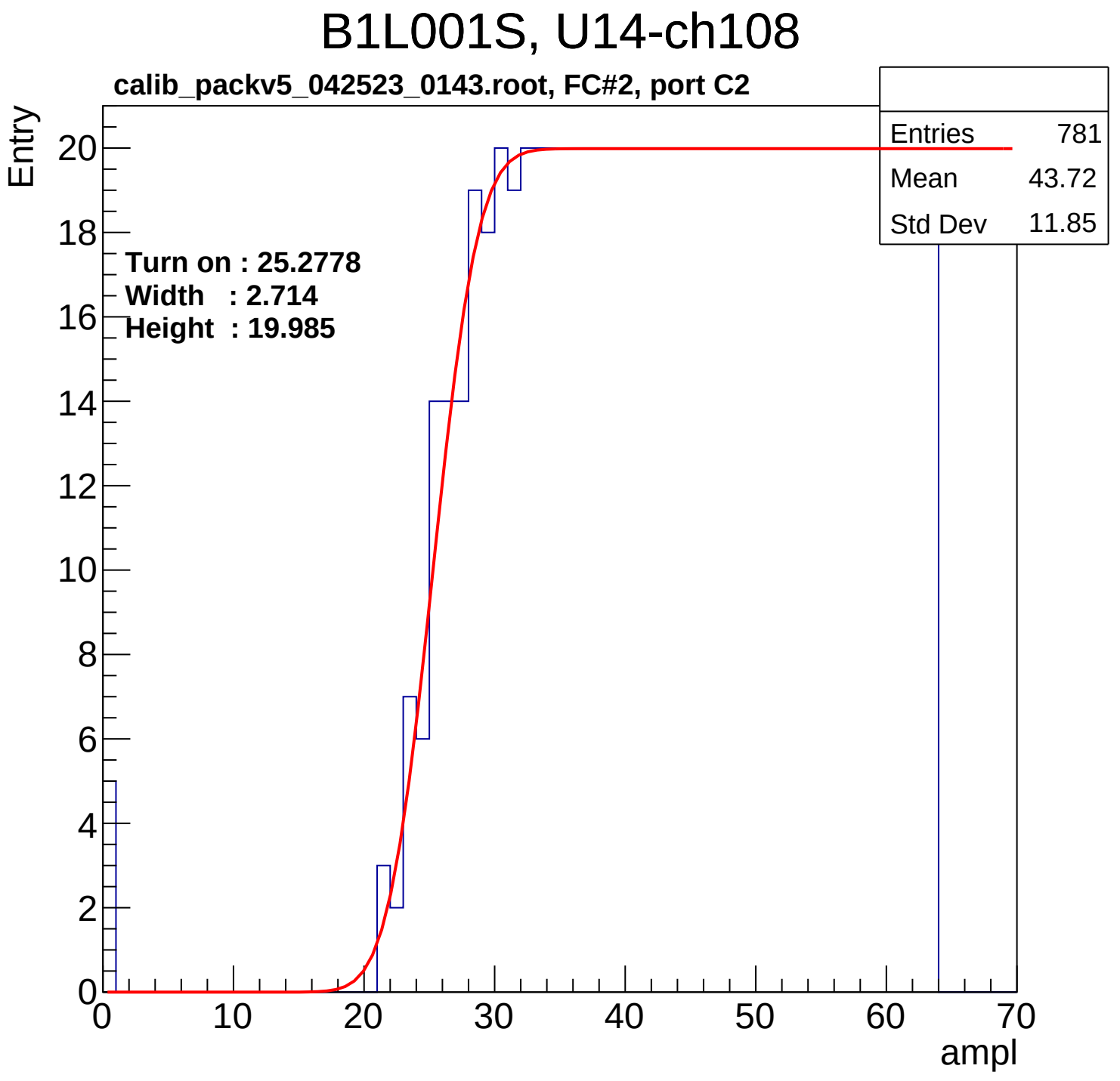

B1L001S, U14-ch103
calib_packv5_042523_0143.root, FC#2, port C2
Entries 777
Mean 43.89
Std Dev 11.63
Turn on : 25.1912
Width : 2.384
Height : 19.901
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

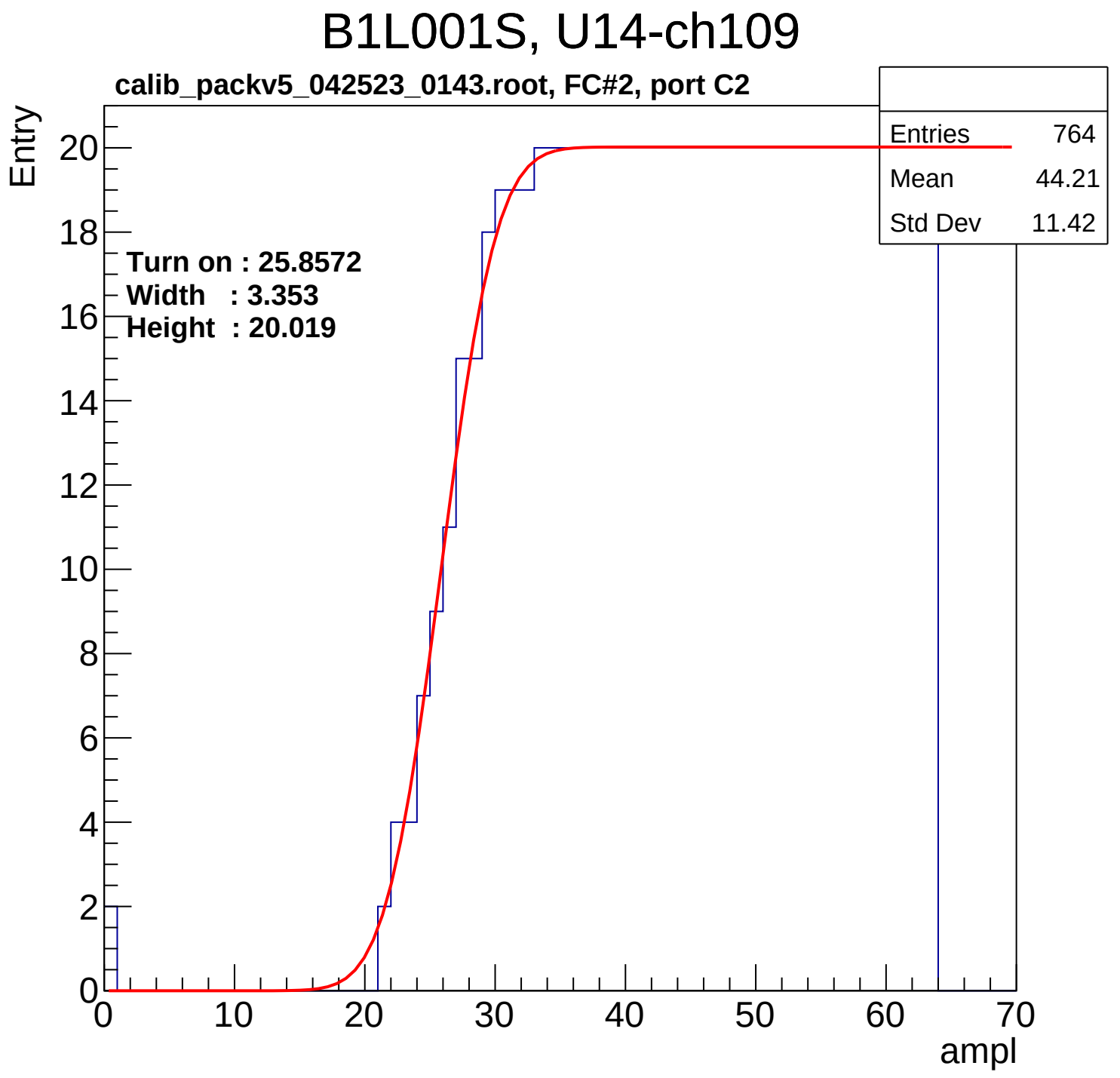

B1L001S, U14-ch104
calib_packv5_042523_0143.root, FC#2, port C2
Entries 791
Mean 43.51
Std Dev 11.89
Turn on : 24.7851
Width : 3.262
Height : 20.086
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

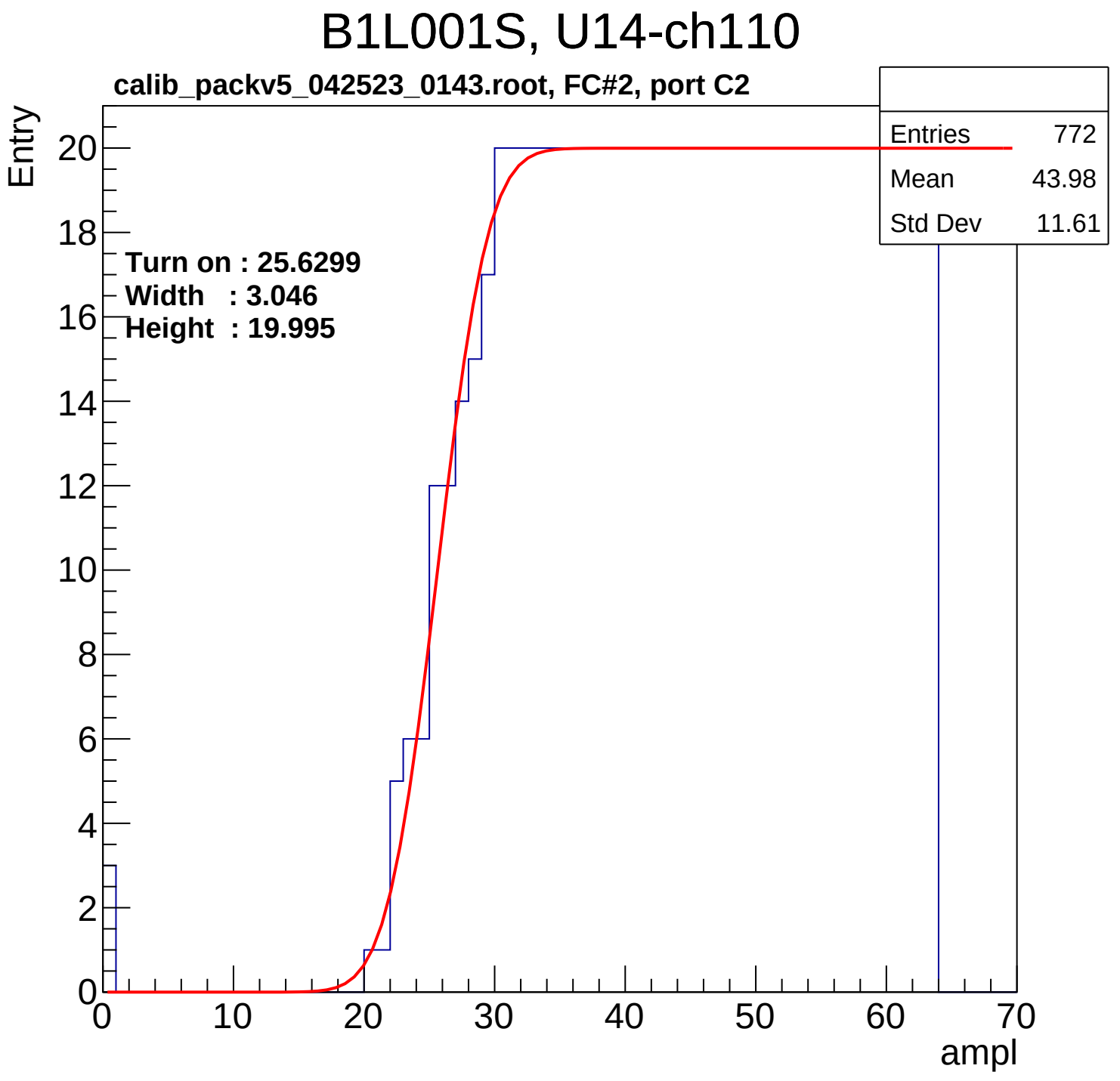

B1L001S, U14-ch105
calib_packv5_042523_0143.root, FC#2, port C2
Entries 756
Mean 44.4
Std Dev 11.37
Turn on : 26.7473
Width : 2.552
Height : 20.032
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

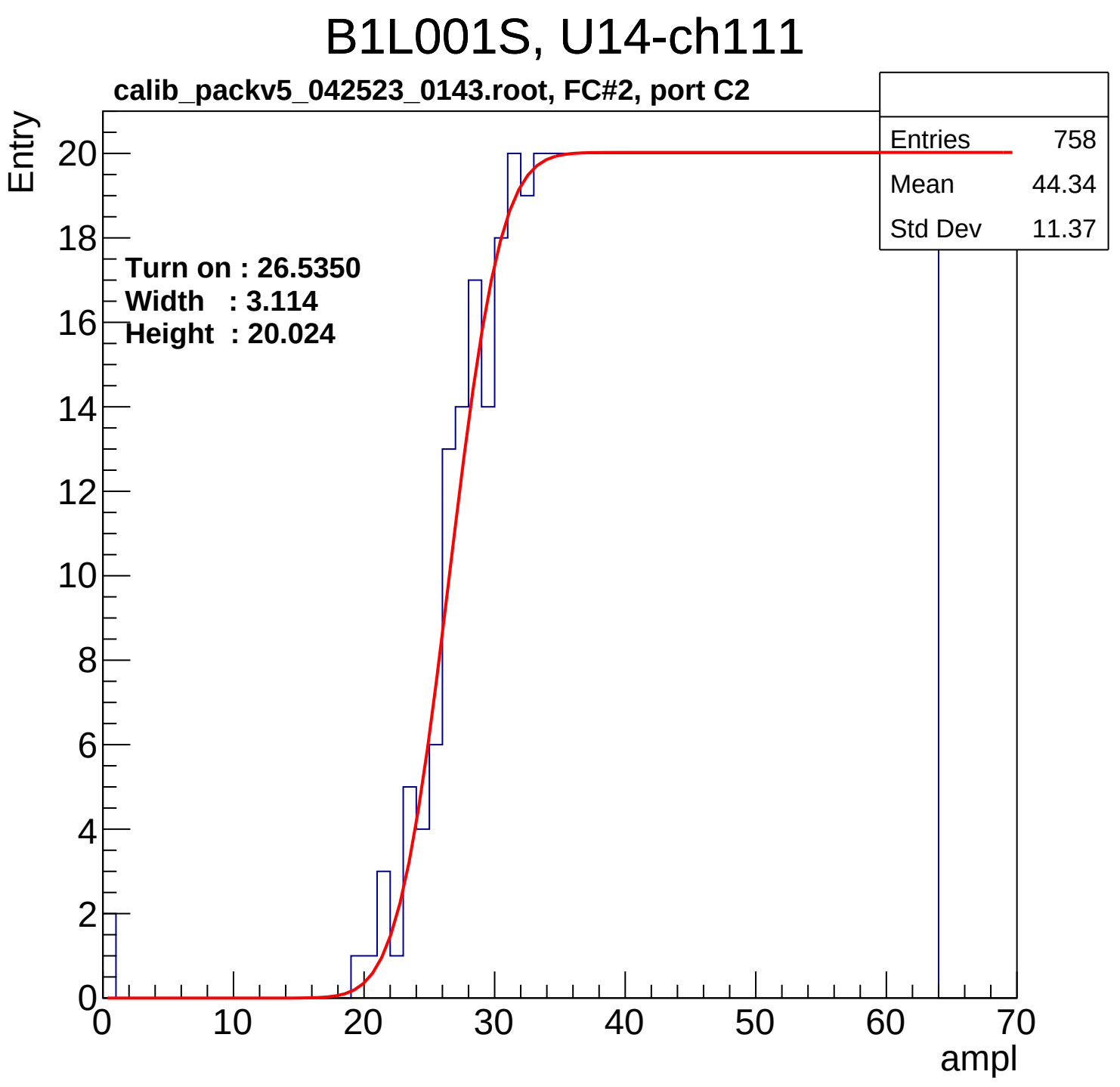

B1L001S, U14-ch106
calib_packv5_042523_0143.root, FC#2, port C2
Entries 725
Mean 45.19
Std Dev 10.86
Turn on : 28.1214
Width : 2.692
Height : 20.044
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

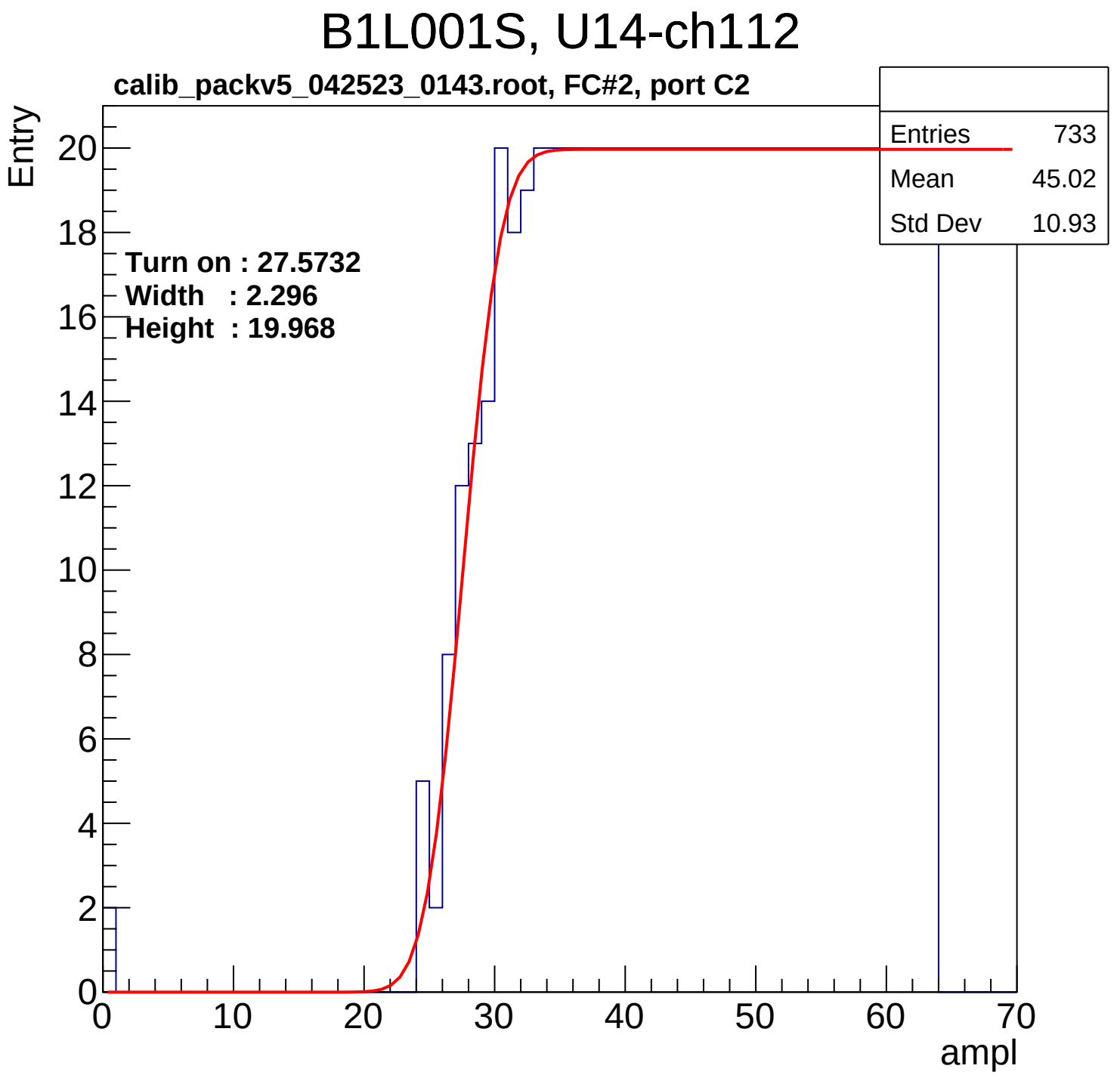

B1L001S, U14-ch107
calib_packv5_042523_0143.root, FC#2, port C2
Entries 766
Mean 44.12
Std Dev 11.54
Turn on : 26.4218
Width : 2.694
Height : 20.015
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

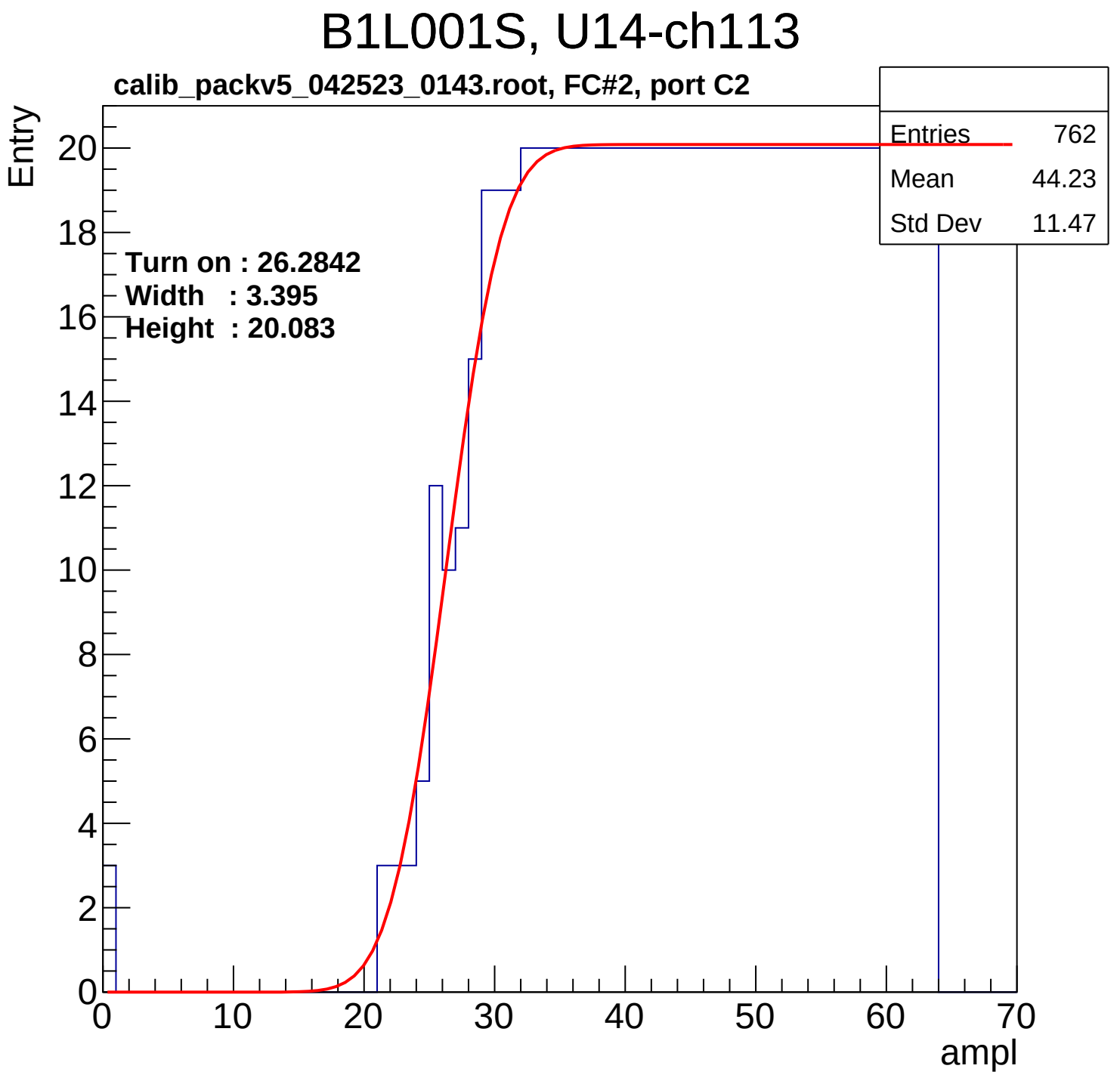

B1L001S, U14-ch108
calib_packv5_042523_0143.root, FC#2, port C2
Entries 781
Mean 43.72
Std Dev 11.85
Turn on : 25.2778
Width : 2.714
Height : 19.985
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

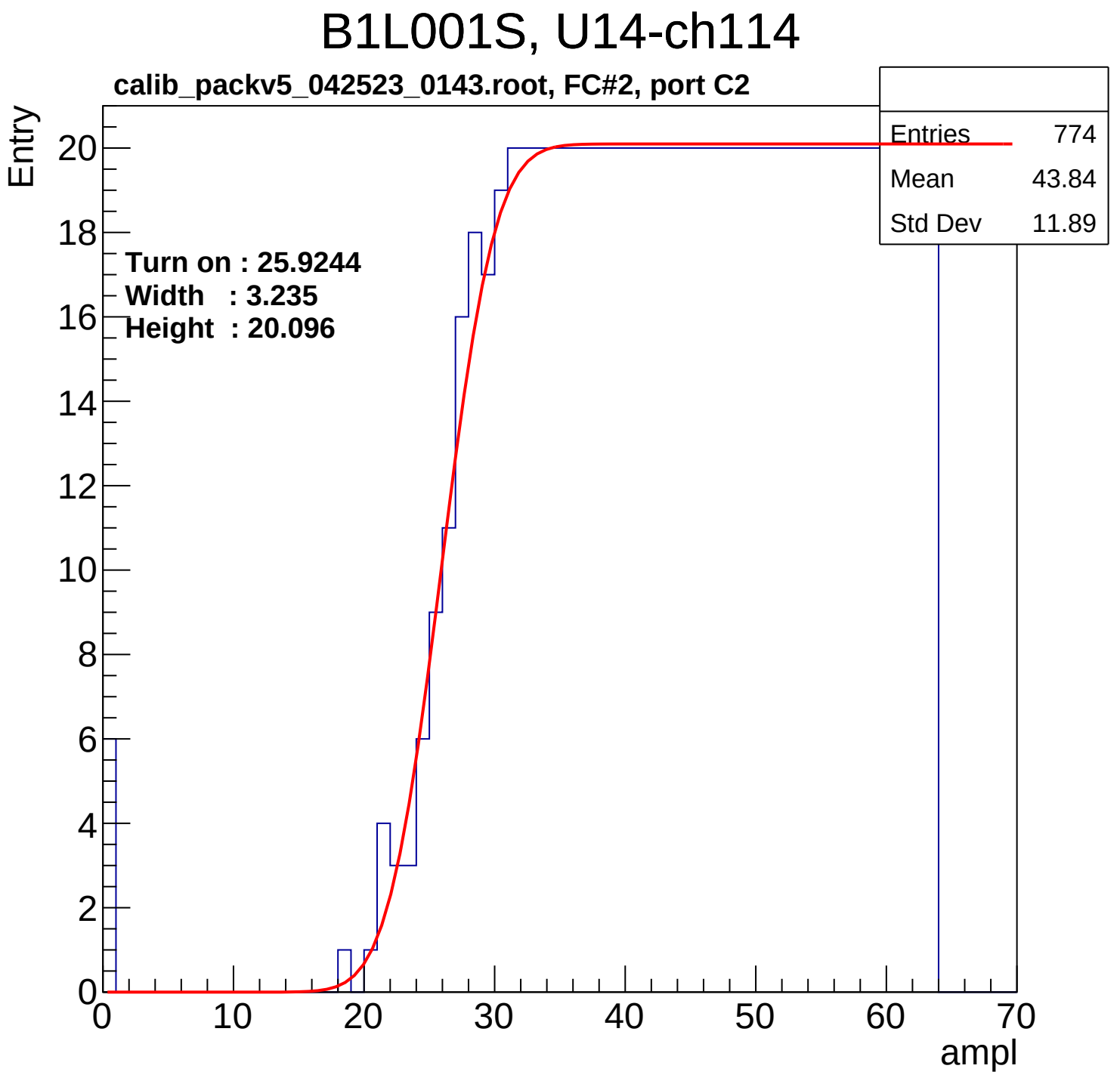

B1L001S, U14-ch109
calib_packv5_042523_0143.root, FC#2, port C2
Entries 764
Mean 44.21
Std Dev 11.42
Turn on : 25.8572
Width : 3.353
Height : 20.019
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

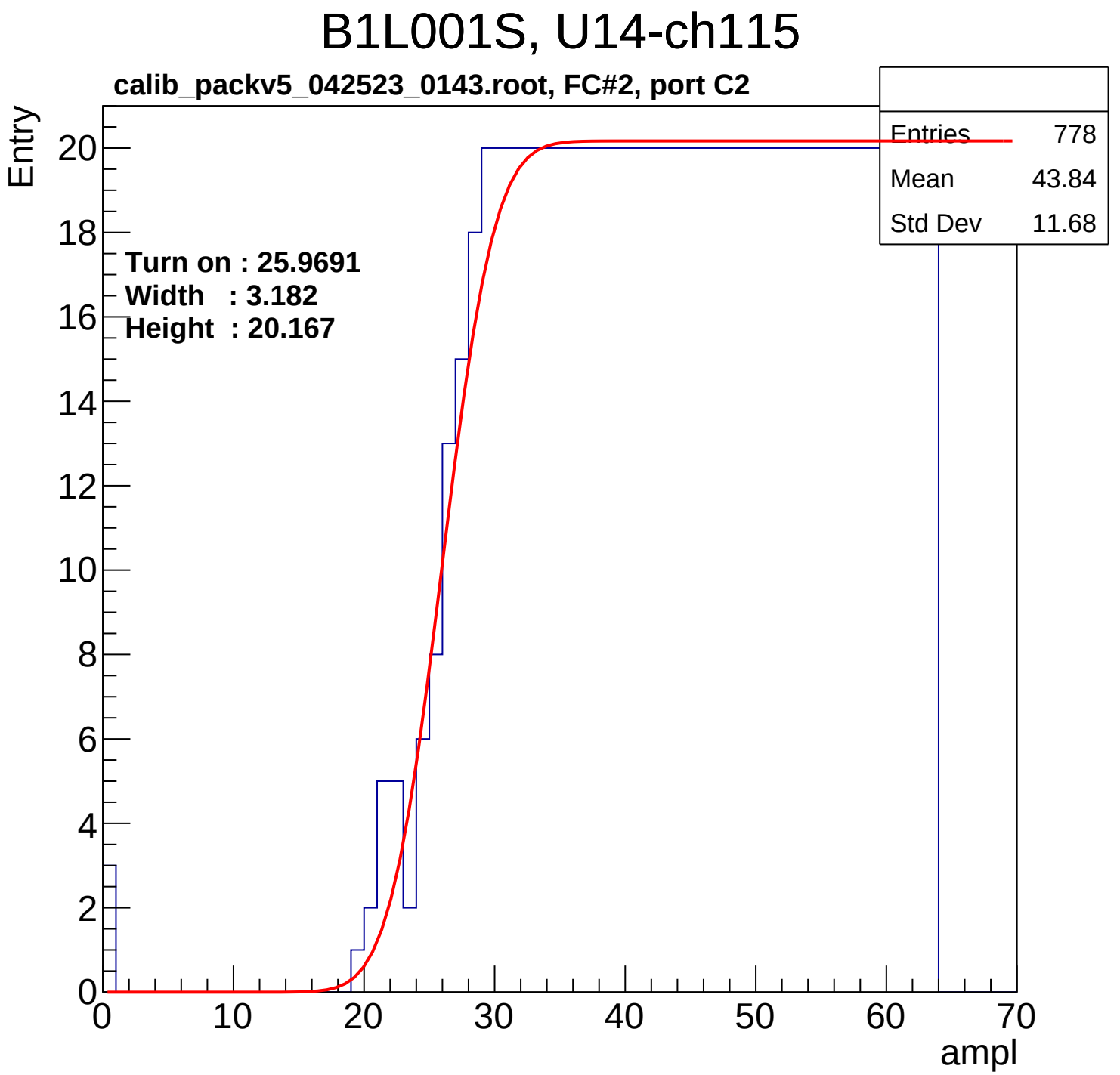

B1L001S, U14-ch110
calib_packv5_042523_0143.root, FC#2, port C2
Entries 772
Mean 43.98
Std Dev 11.61
Turn on : 25.6299
Width : 3.046
Height : 19.995
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

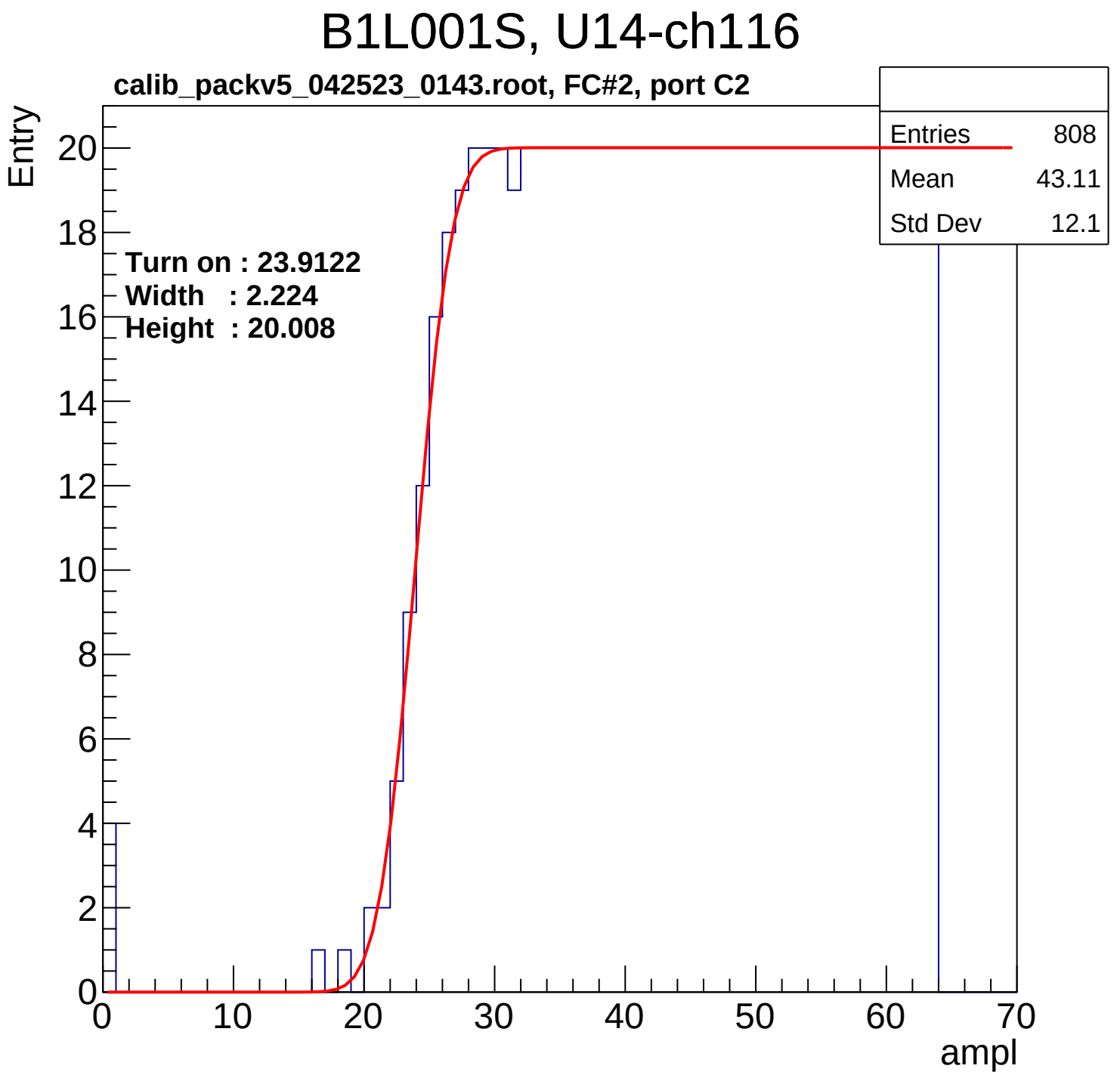

B1L001S, U14-ch111
calib_packv5_042523_0143.root, FC#2, port C2
Entries 758
Mean 44.34
Std Dev 11.37
Turn on : 26.5350
Width : 3.114
Height : 20.024
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

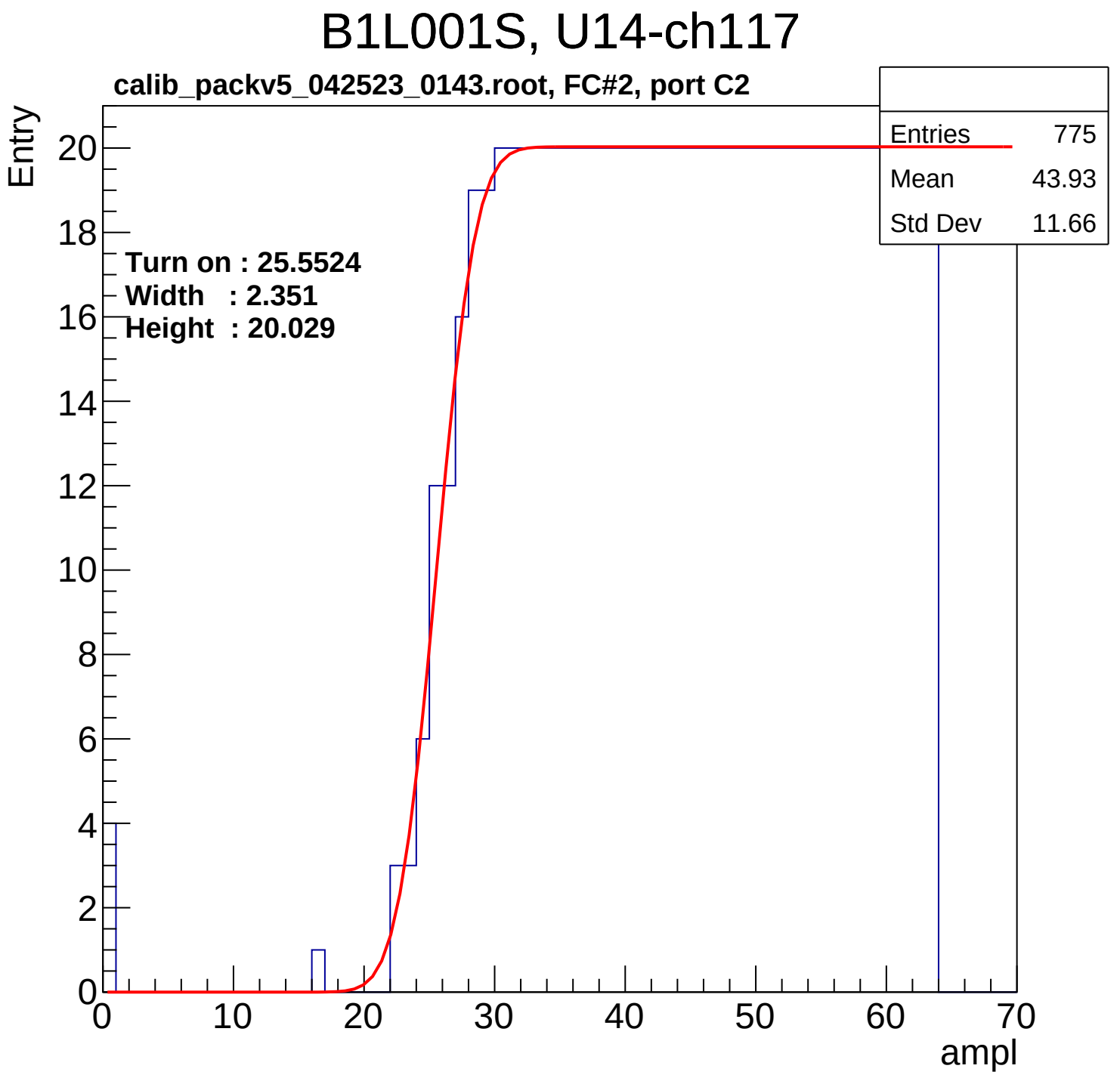

B1L001S, U14-ch112
calib_packv5_042523_0143.root, FC#2, port C2
Entries 733
Mean 45.02
Std Dev 10.93
Turn on : 27.5732
Width : 2.296
Height : 19.968
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

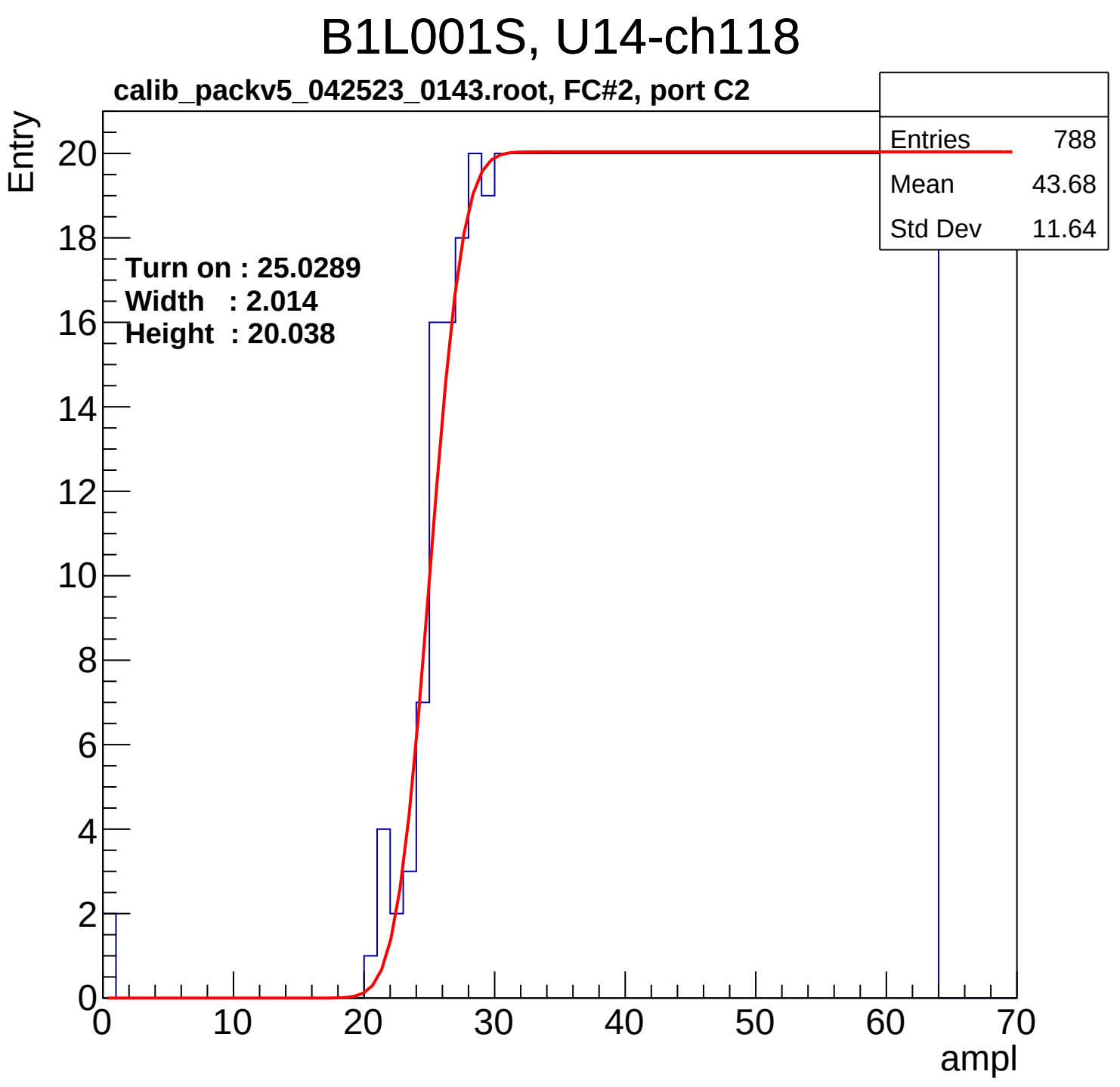

B1L001S, U14-ch113
calib_packv5_042523_0143.root, FC#2, port C2
Entries 762
Mean 44.23
Std Dev 11.47
Turn on : 26.2842
Width : 3.395
Height : 20.083
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

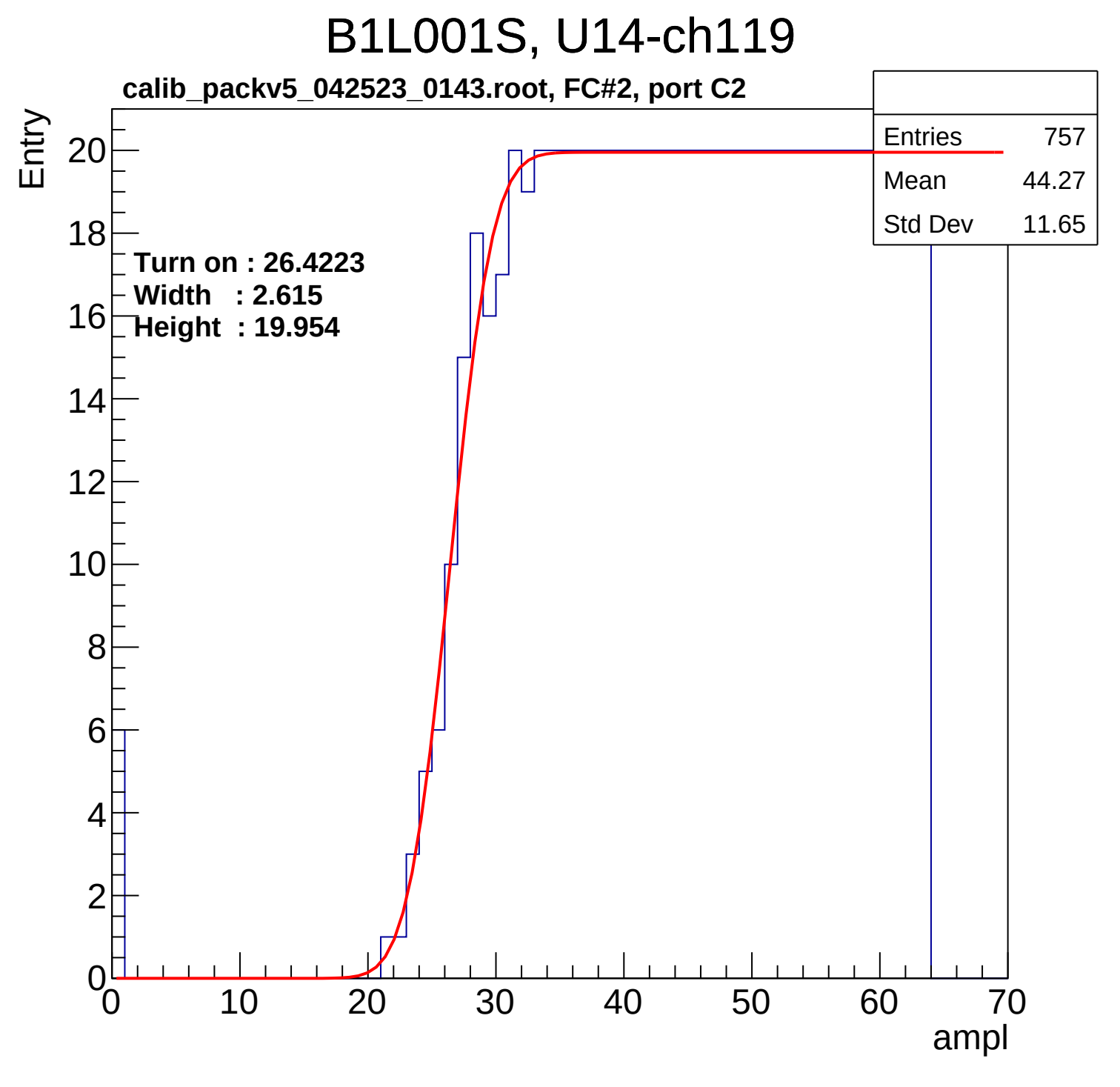

B1L001S, U14-ch114
calib_packv5_042523_0143.root, FC#2, port C2
Entries 774
Mean 43.84
Std Dev 11.89
Turn on : 25.9244
Width : 3.235
Height : 20.096
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

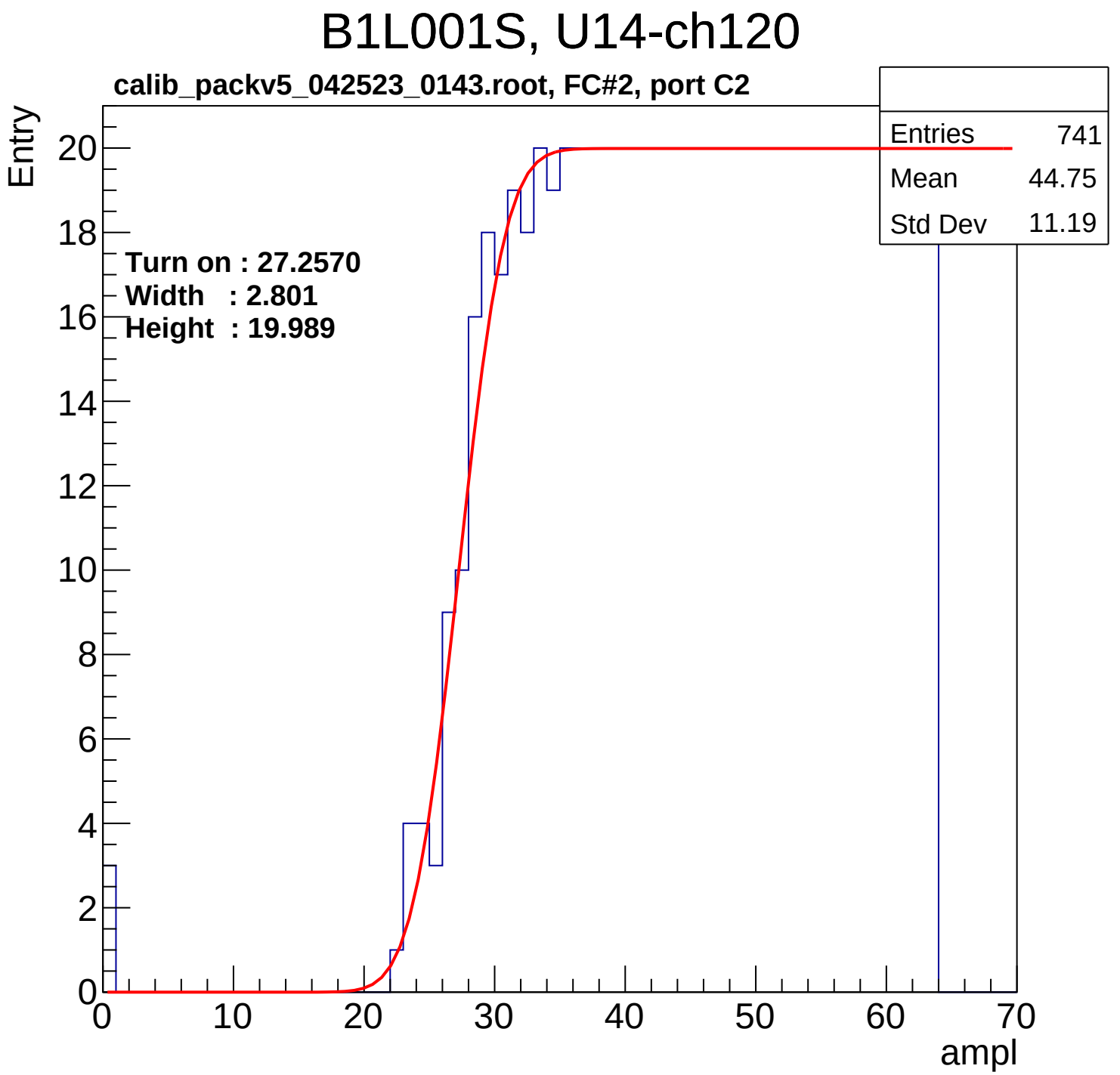

B1L001S, U14-ch115
calib_packv5_042523_0143.root, FC#2, port C2
Entries 778
Mean 43.84
Std Dev 11.68
Turn on : 25.9691
Width : 3.182
Height : 20.167
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

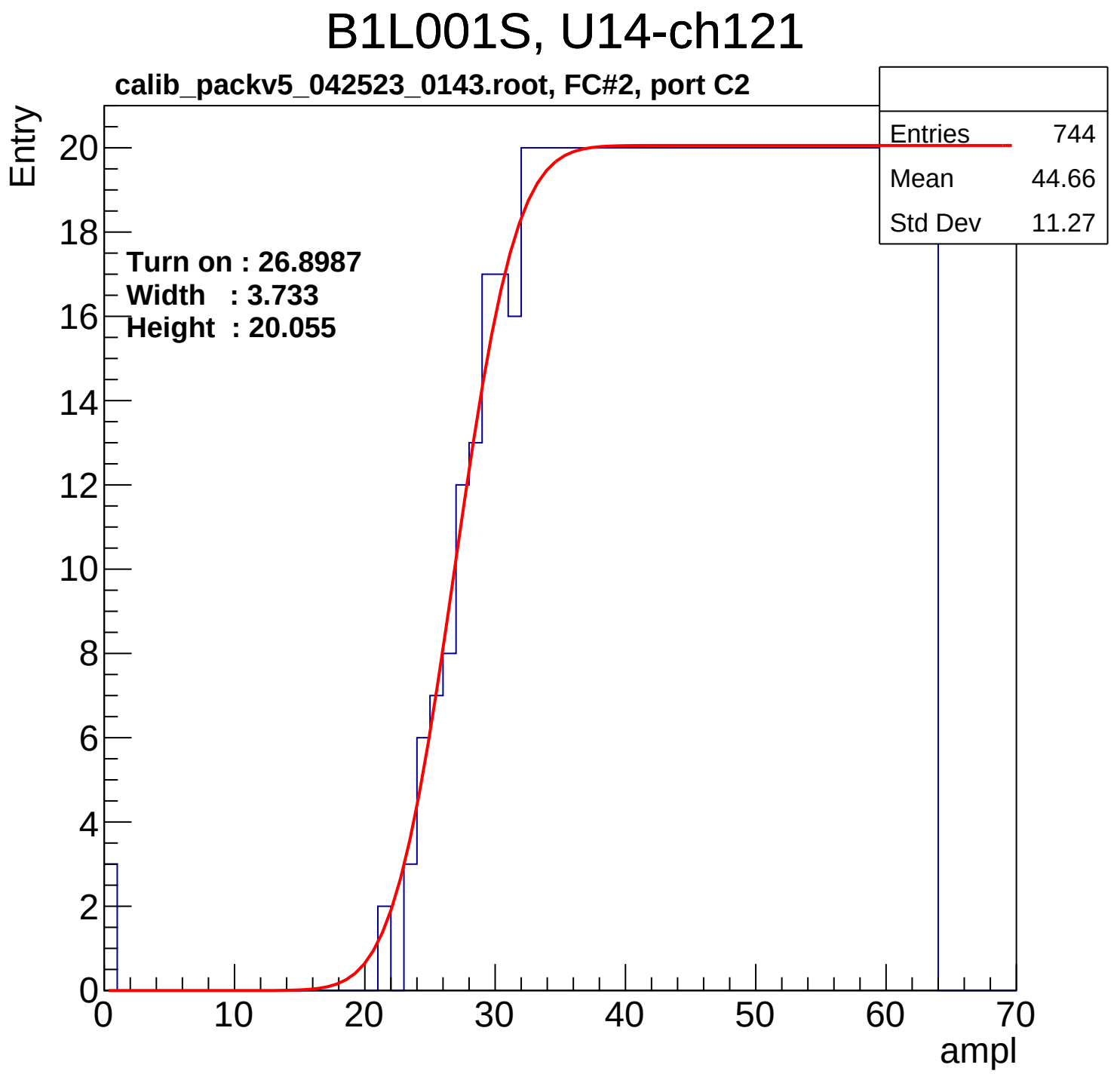

B1L001S, U14-ch116
calib_packv5_042523_0143.root, FC#2, port C2
Entries 808
Mean 43.11
Std Dev 12.1
Turn on : 23.9122
Width : 2.224
Height : 20.008
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

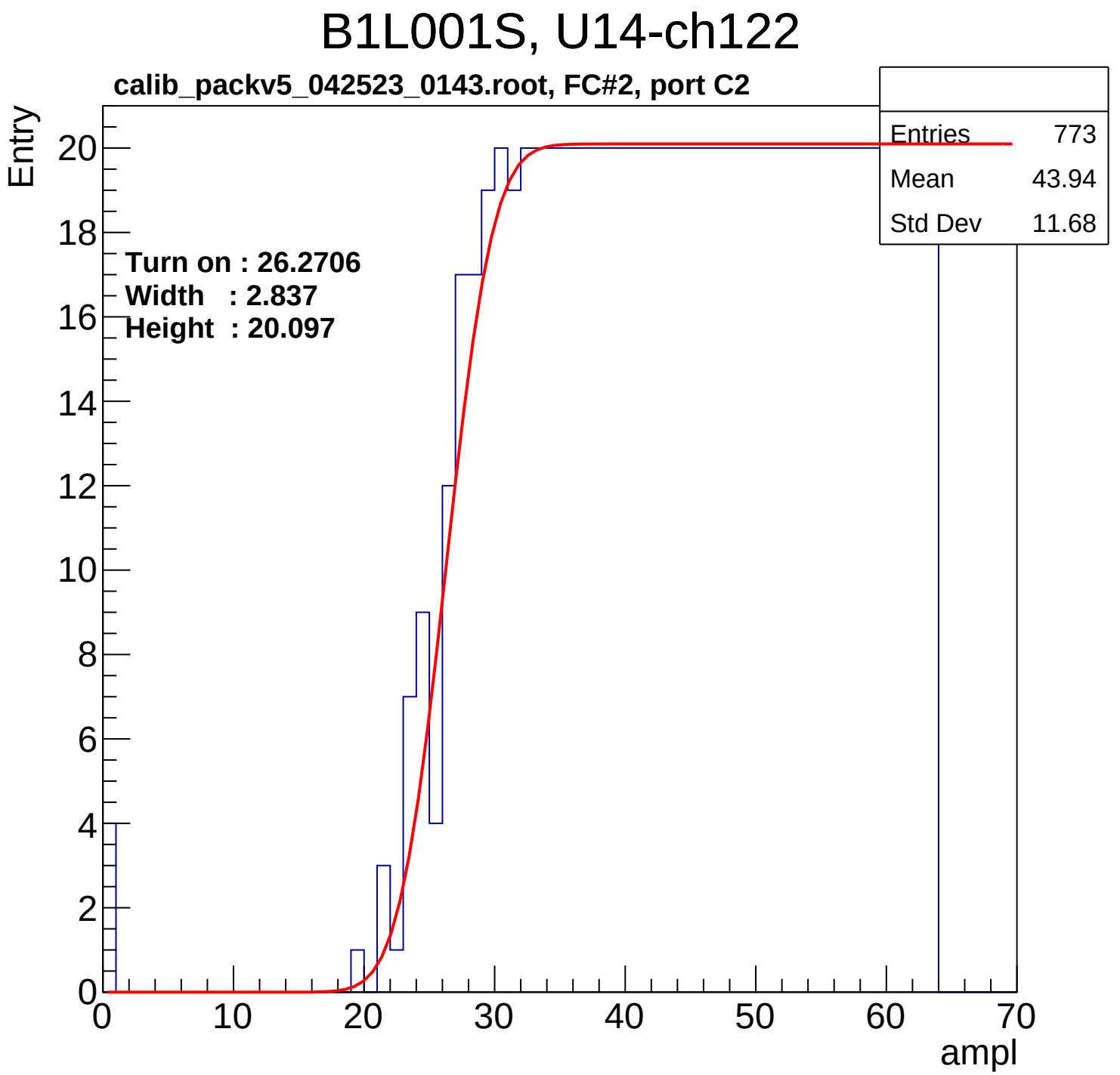

B1L001S, U14-ch117
calib_packv5_042523_0143.root, FC#2, port C2
Entries 775
Mean 43.93
Std Dev 11.66
Turn on : 25.5524
Width : 2.351
Height : 20.029
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

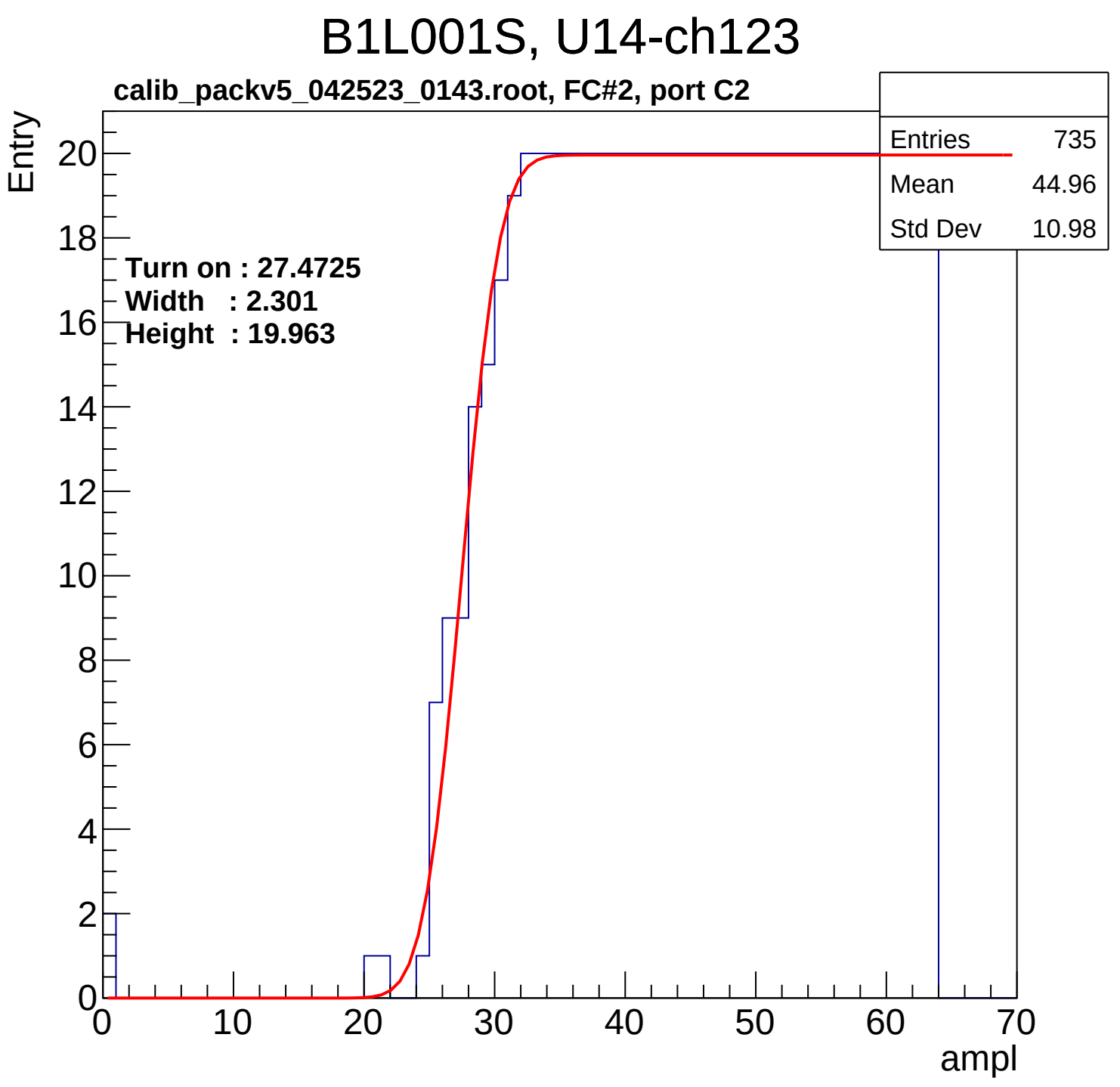

B1L001S, U14-ch118
calib_packv5_042523_0143.root, FC#2, port C2
Entries 788
Mean 43.68
Std Dev 11.64
Turn on : 25.0289
Width : 2.014
Height : 20.038
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

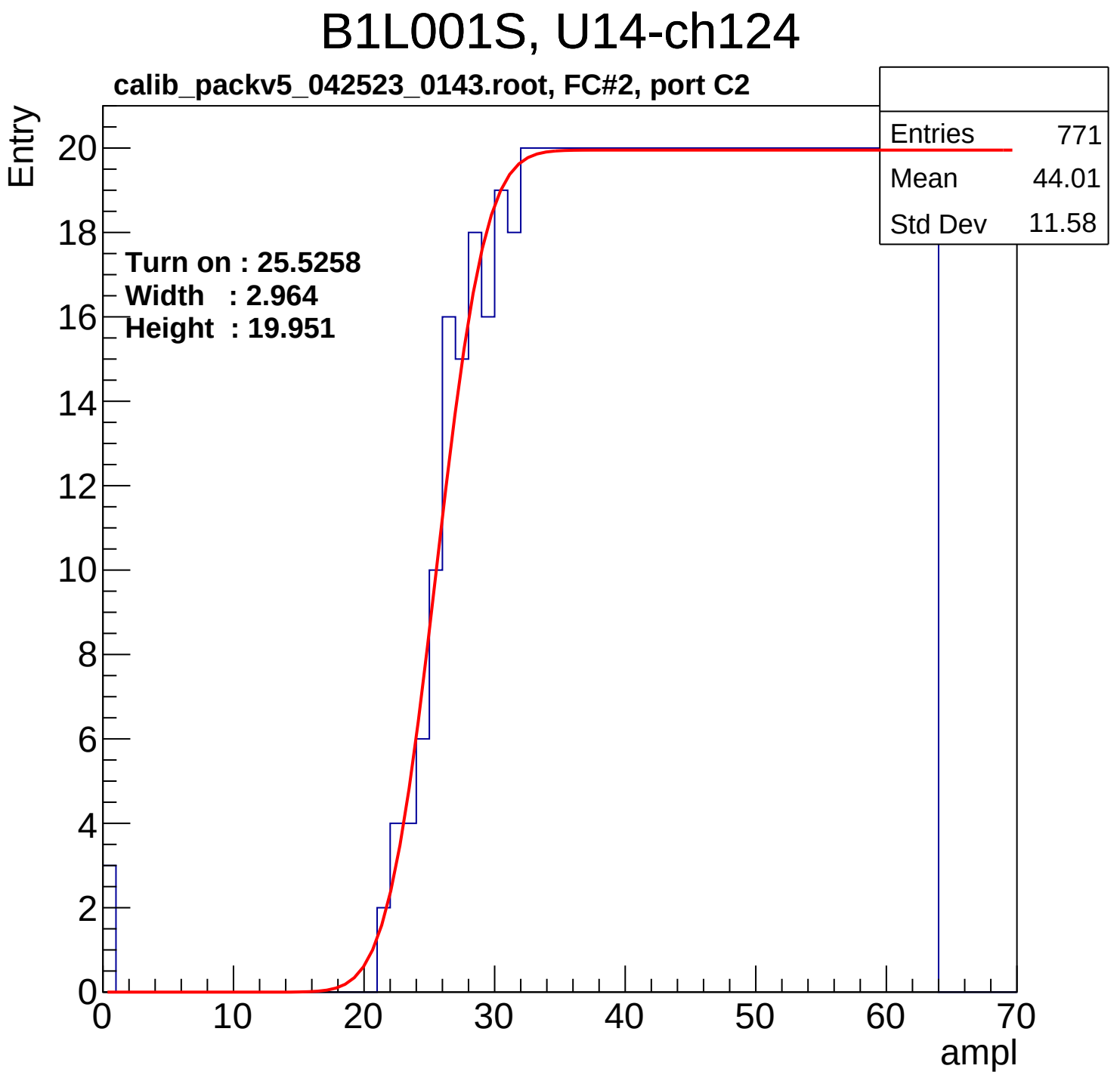

B1L001S, U14-ch119
calib_packv5_042523_0143.root, FC#2, port C2
Entries 757
Mean 44.27
Std Dev 11.65
Turn on : 26.4223
Width : 2.615
Height : 19.954
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

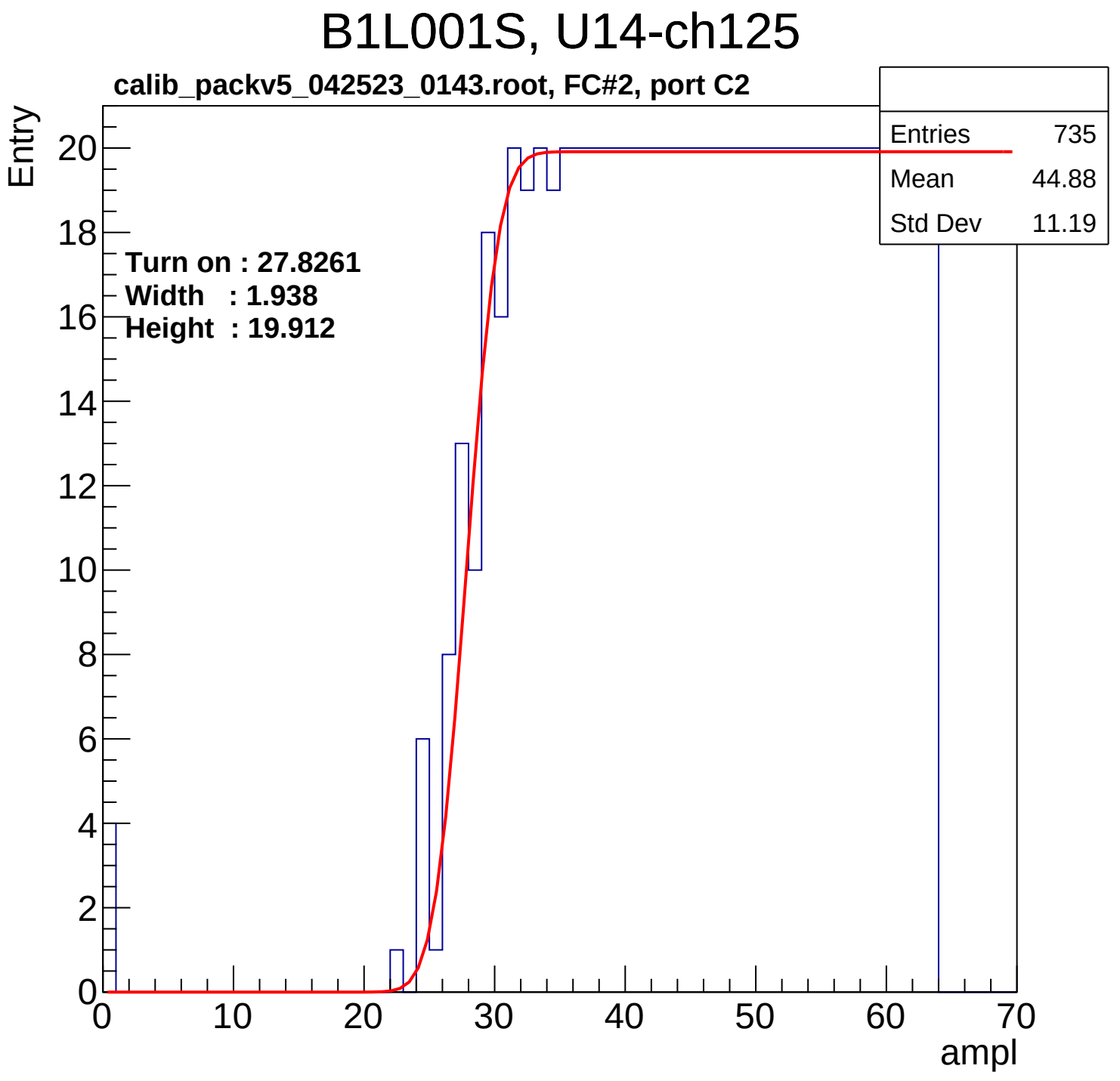

B1L001S, U14-ch120
calib_packv5_042523_0143.root, FC#2, port C2
Entries 741
Mean 44.75
Std Dev 11.19
Turn on : 27.2570
Width : 2.801
Height : 19.989
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

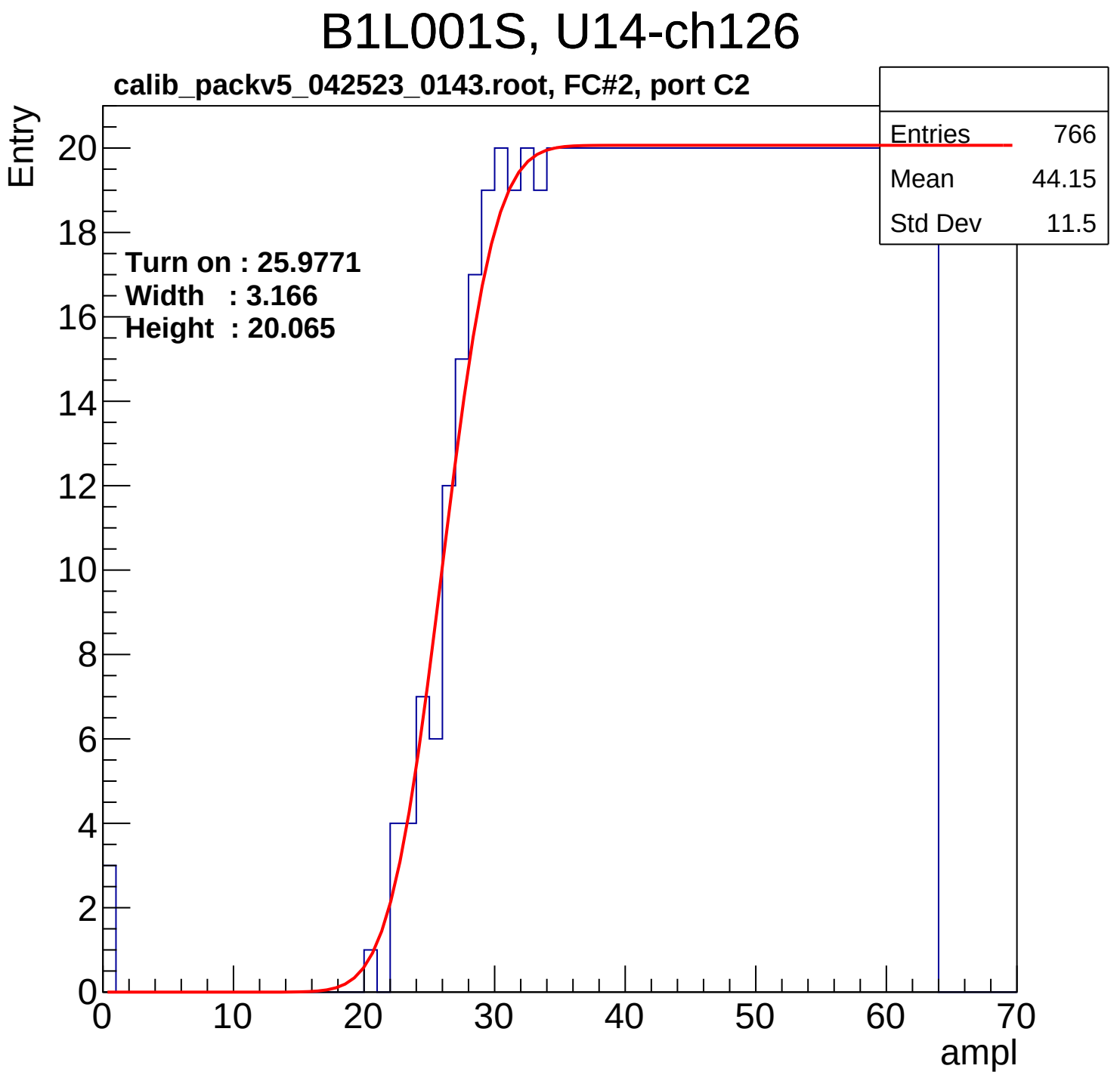

B1L001S, U14-ch121
calib_packv5_042523_0143.root, FC#2, port C2
Entries 744
Mean 44.66
Std Dev 11.27
Turn on : 26.8987
Width : 3.733
Height : 20.055
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

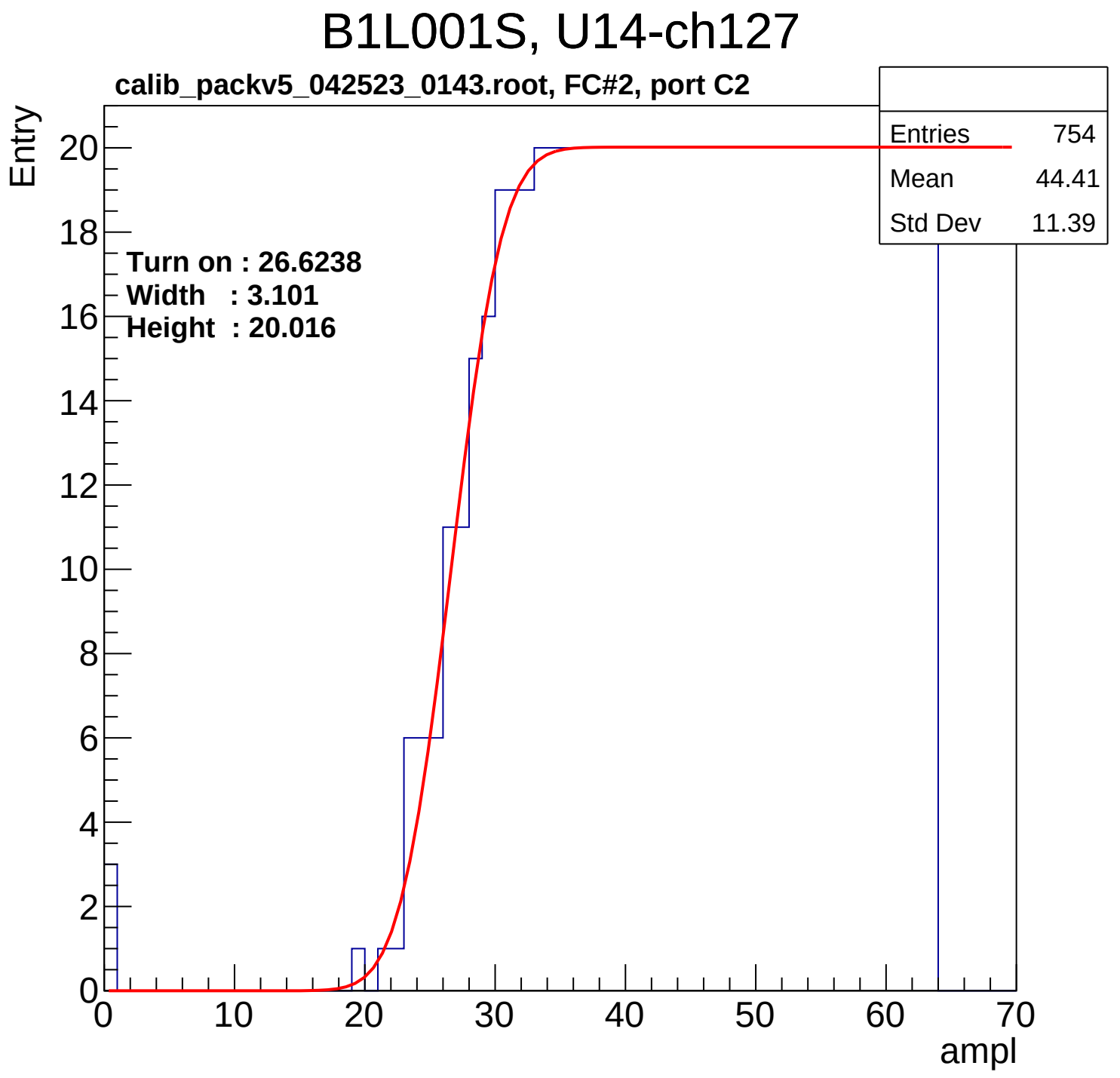

B1L001S, U14-ch122
calib_packv5_042523_0143.root, FC#2, port C2
Entries 773
Mean 43.94
Std Dev 11.68
Turn on : 26.2706
Width : 2.837
Height : 20.097
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

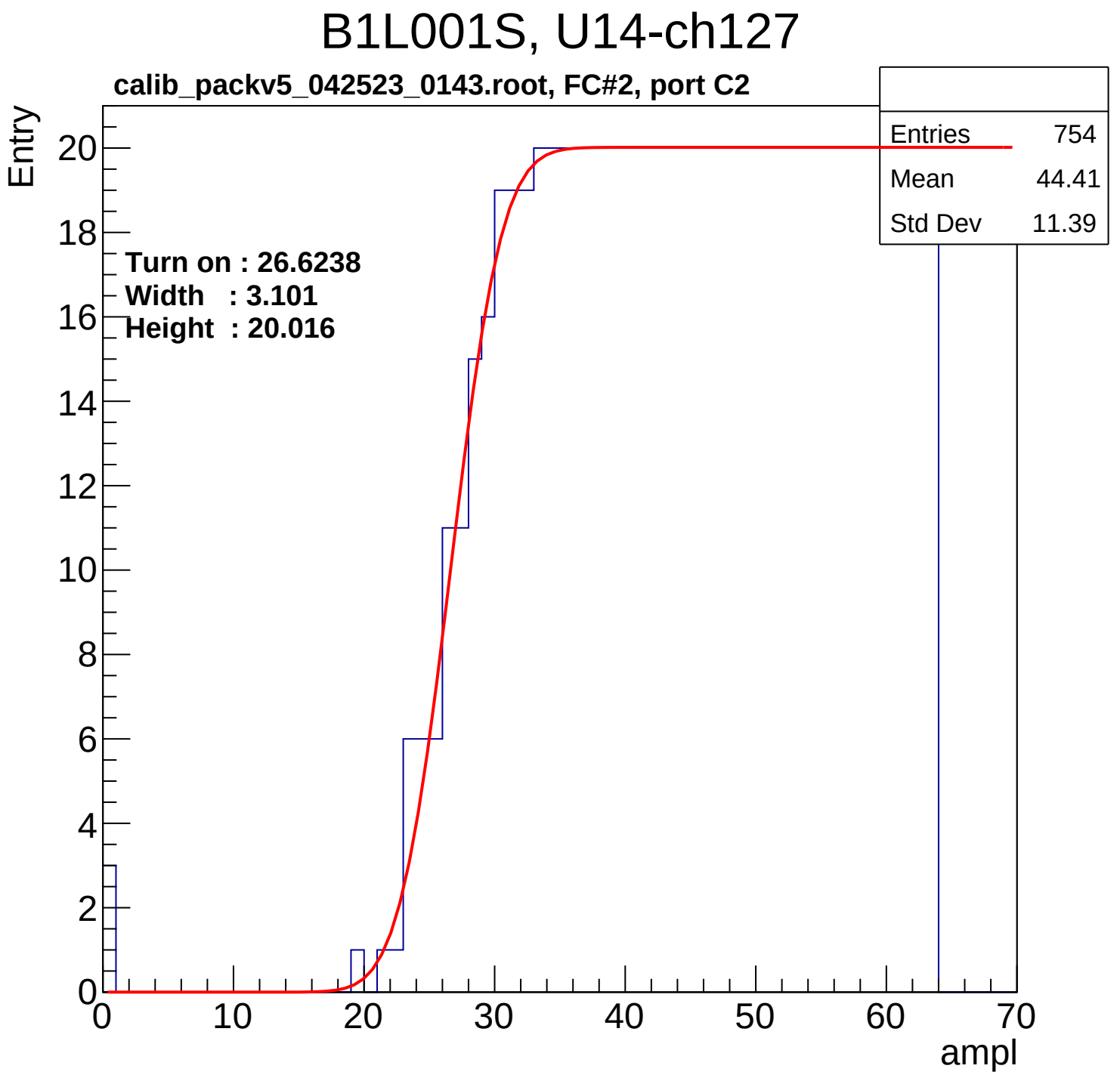

B1L001S, U14-ch123
calib_packv5_042523_0143.root, FC#2, port C2
Entries 735
Mean 44.96
Std Dev 10.98
Turn on : 27.4725
Width : 2.301
Height : 19.963
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L001S, U14-ch124
calib_packv5_042523_0143.root, FC#2, port C2
Entries 771
Mean 44.01
Std Dev 11.58
Turn on : 25.5258
Width : 2.964
Height : 19.951
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L001S, U14-ch125
calib_packv5_042523_0143.root, FC#2, port C2
Entries 735
Mean 44.88
Std Dev 11.19
Turn on : 27.8261
Width : 1.938
Height : 19.912
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L001S, U14-ch126
calib_packv5_042523_0143.root, FC#2, port C2
Entries 766
Mean 44.15
Std Dev 11.5
Turn on : 25.9771
Width : 3.166
Height : 20.065
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L001S, U14-ch127
calib_packv5_042523_0143.root, FC#2, port C2
Entries 754
Mean 44.41
Std Dev 11.39
Turn on : 26.6238
Width : 3.101
Height : 20.016
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L001S, U14-ch127
calib_packv5_042523_0143.root, FC#2, port C2
Entries 754
Mean 44.41
Std Dev 11.39
Turn on : 26.6238
Width : 3.101
Height : 20.016
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70