



# B1L103S, U3-ch0, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	82
Mean	19.4
Std Dev	12.08

**Gaus mean : 27.3812**

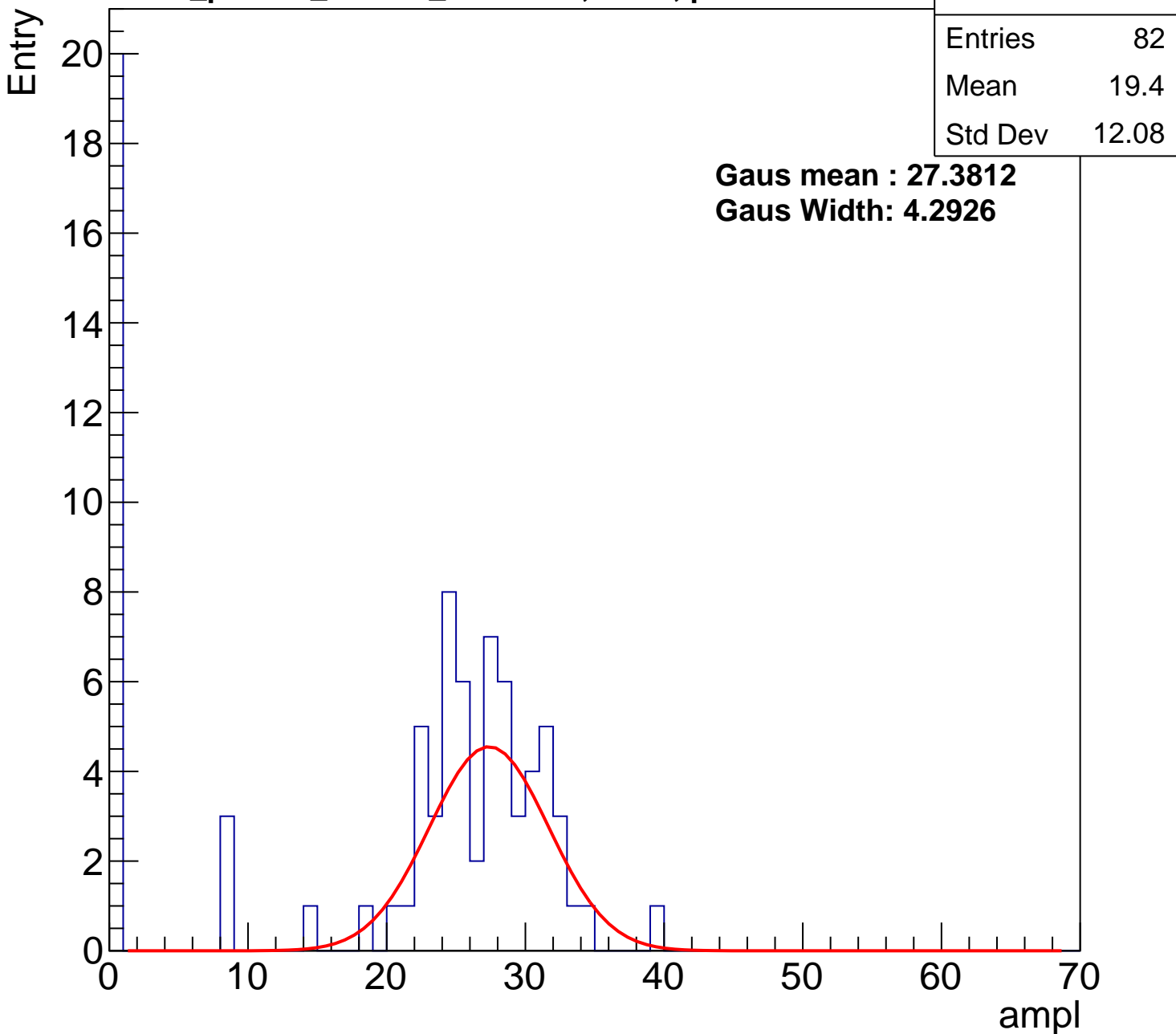
**Gaus Width: 4.2926**

Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch0, adc1

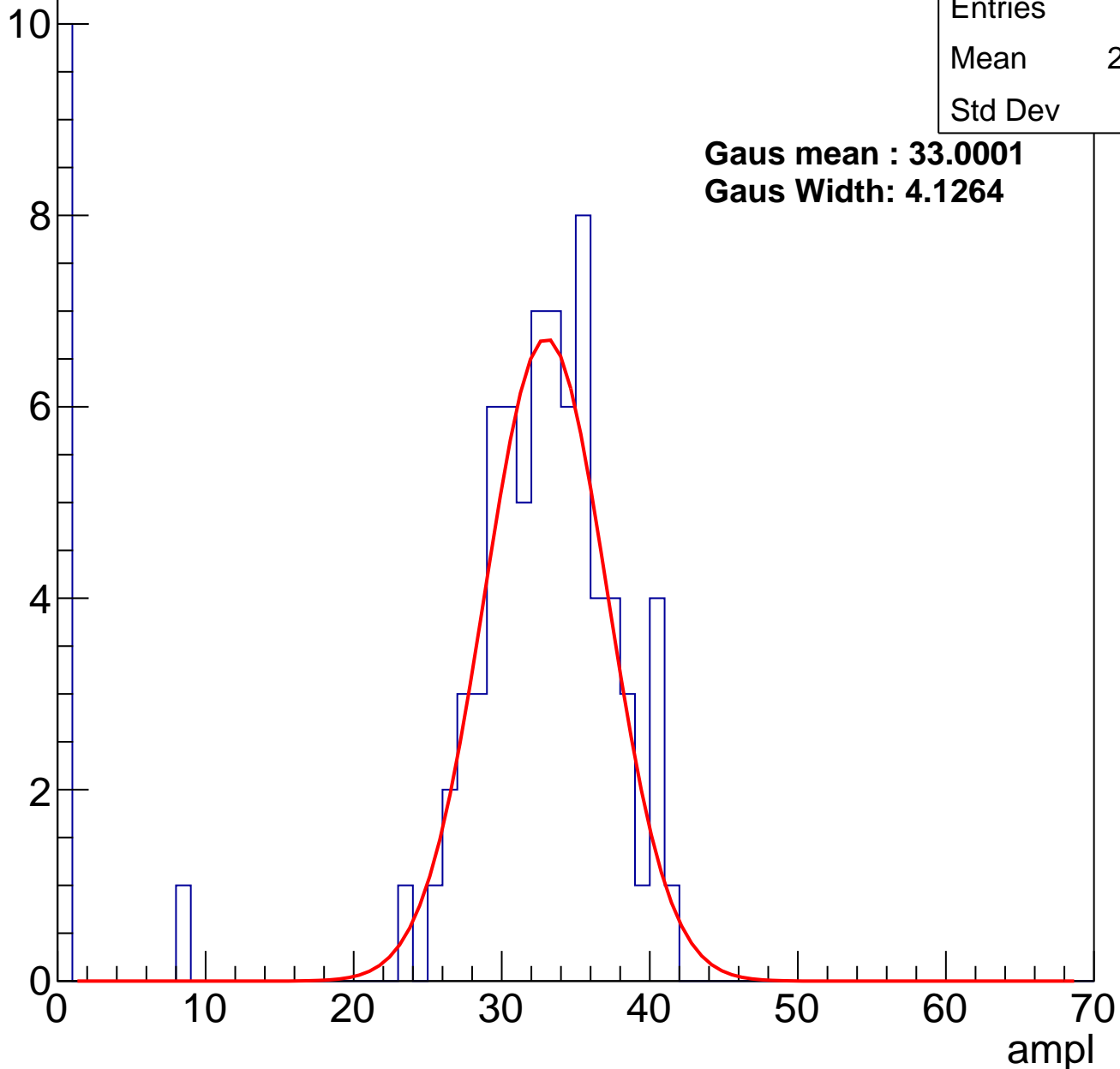
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	83
Mean	28.52
Std Dev	11.5

**Gaus mean : 33.0001**

**Gaus Width: 4.1264**

Entry



# B1L103S, U3-ch0, adc2

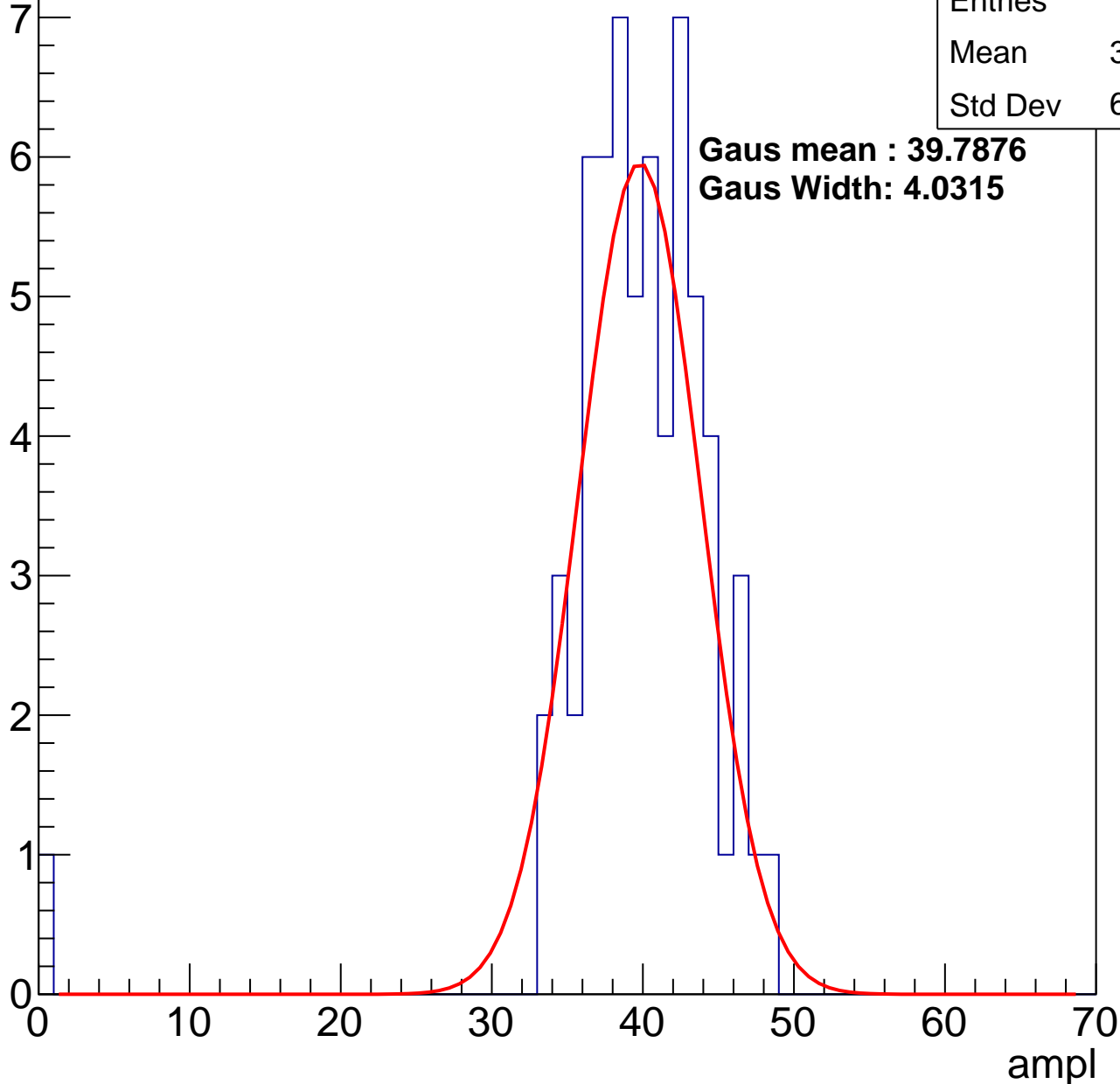
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	39.12
Std Dev	6.094

**Gaus mean : 39.7876**

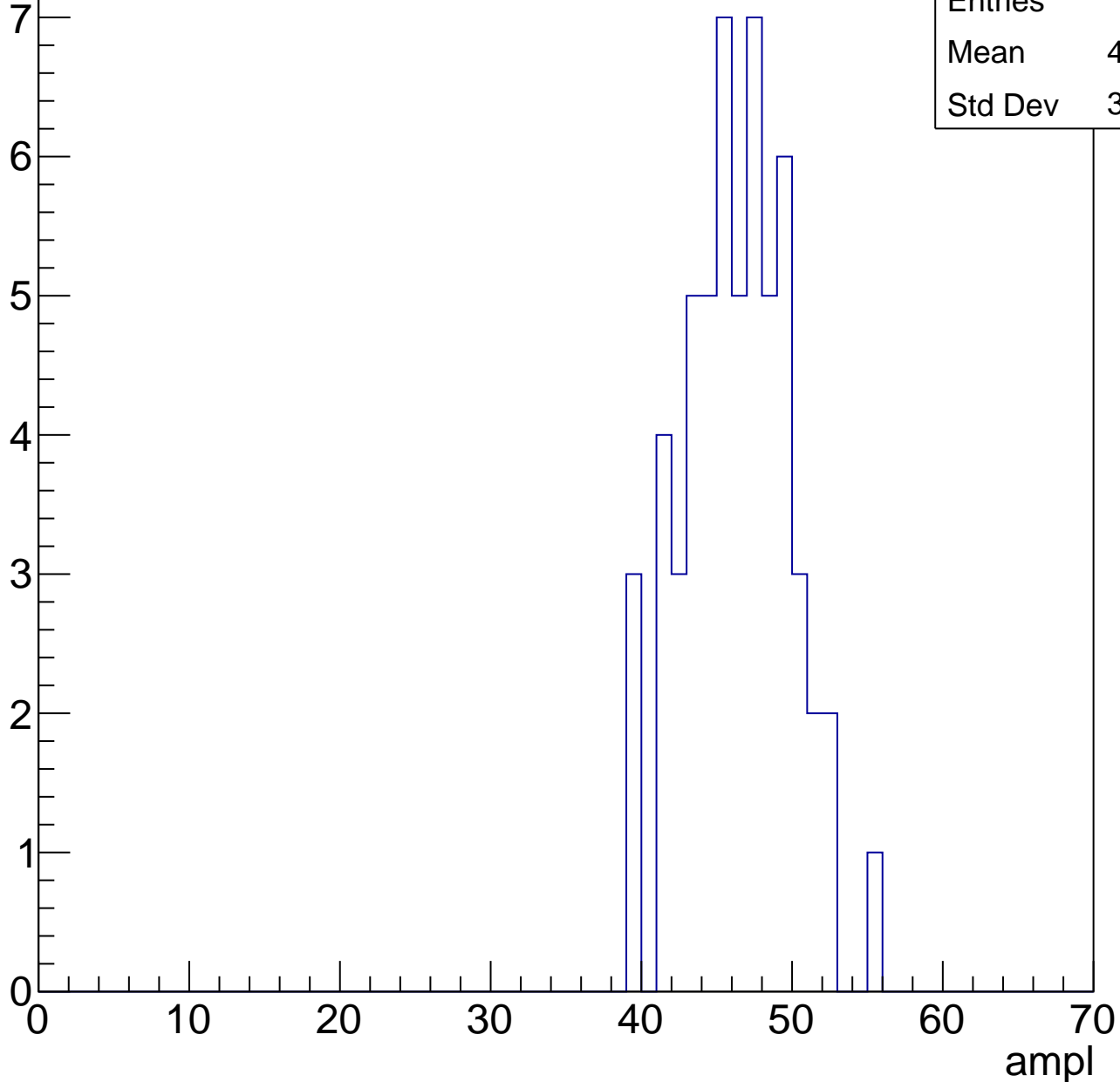
**Gaus Width: 4.0315**



# B1L103S, U3-ch0, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

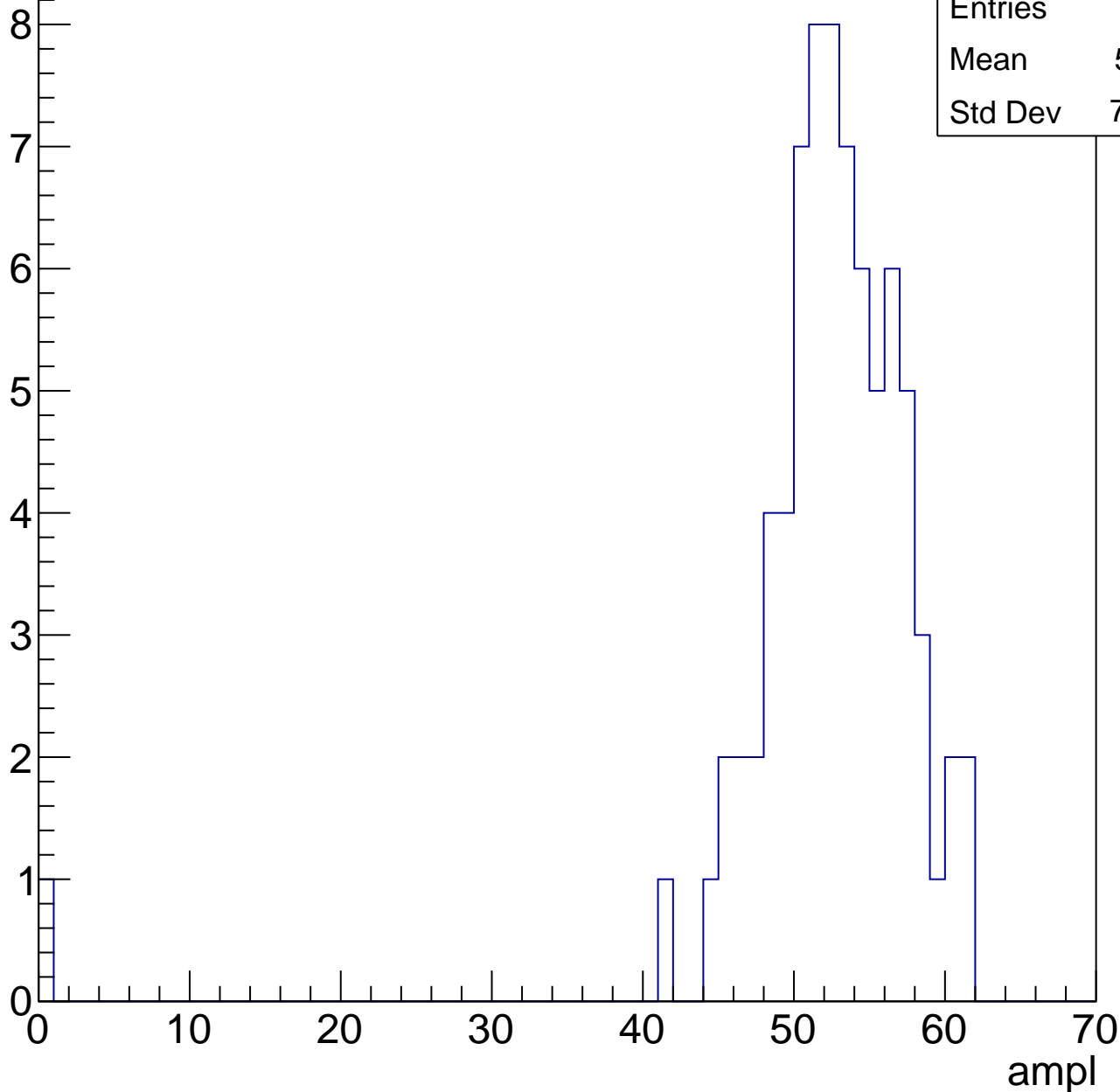


# B1L103S, U3-ch0, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	77
Mean	51.81
Std Dev	7.195



# B1L103S, U3-ch0, adc5

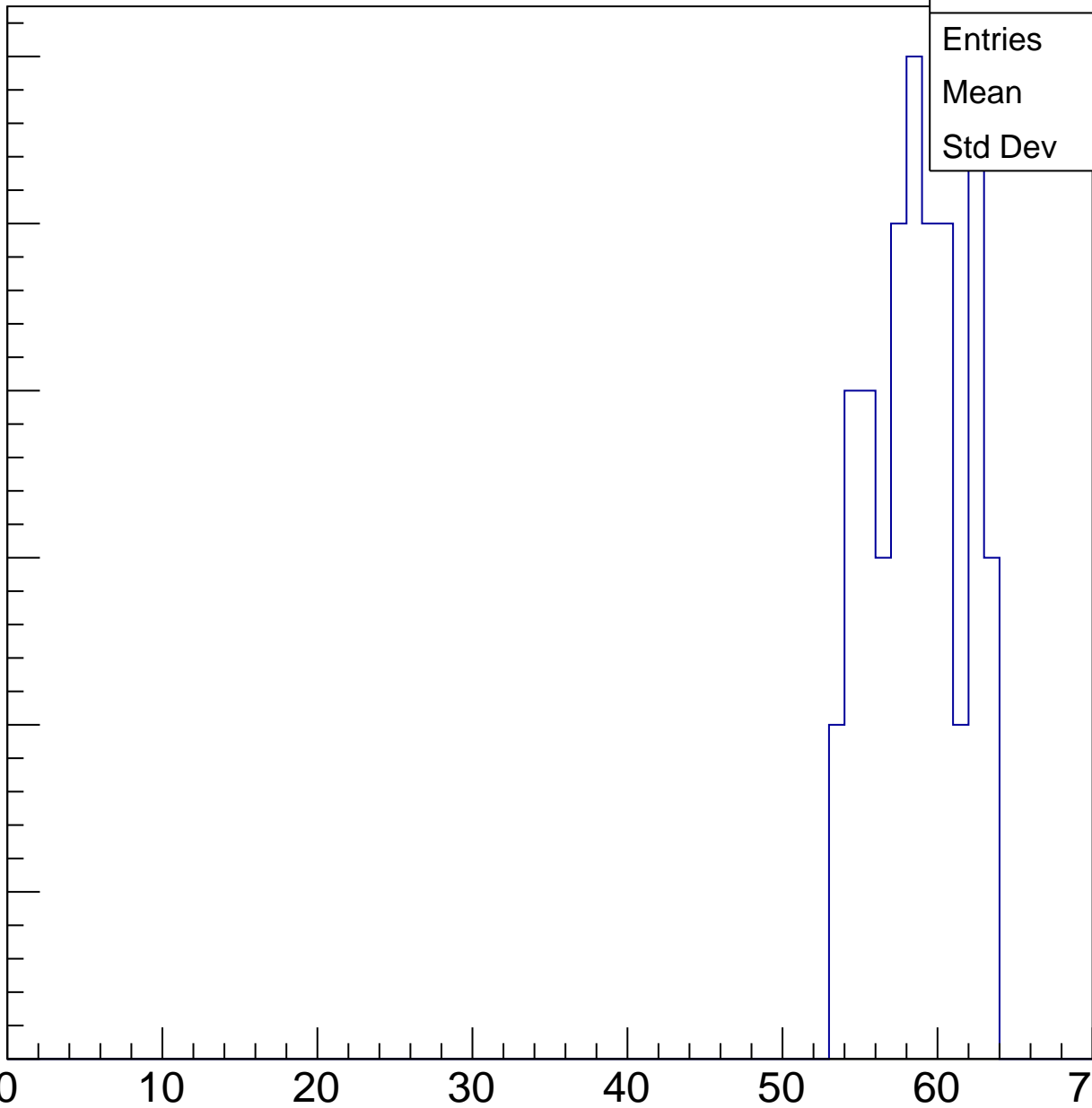
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

6  
5  
4  
3  
2  
1  
0

Entries	45
Mean	58.24
Std Dev	2.899

ampl

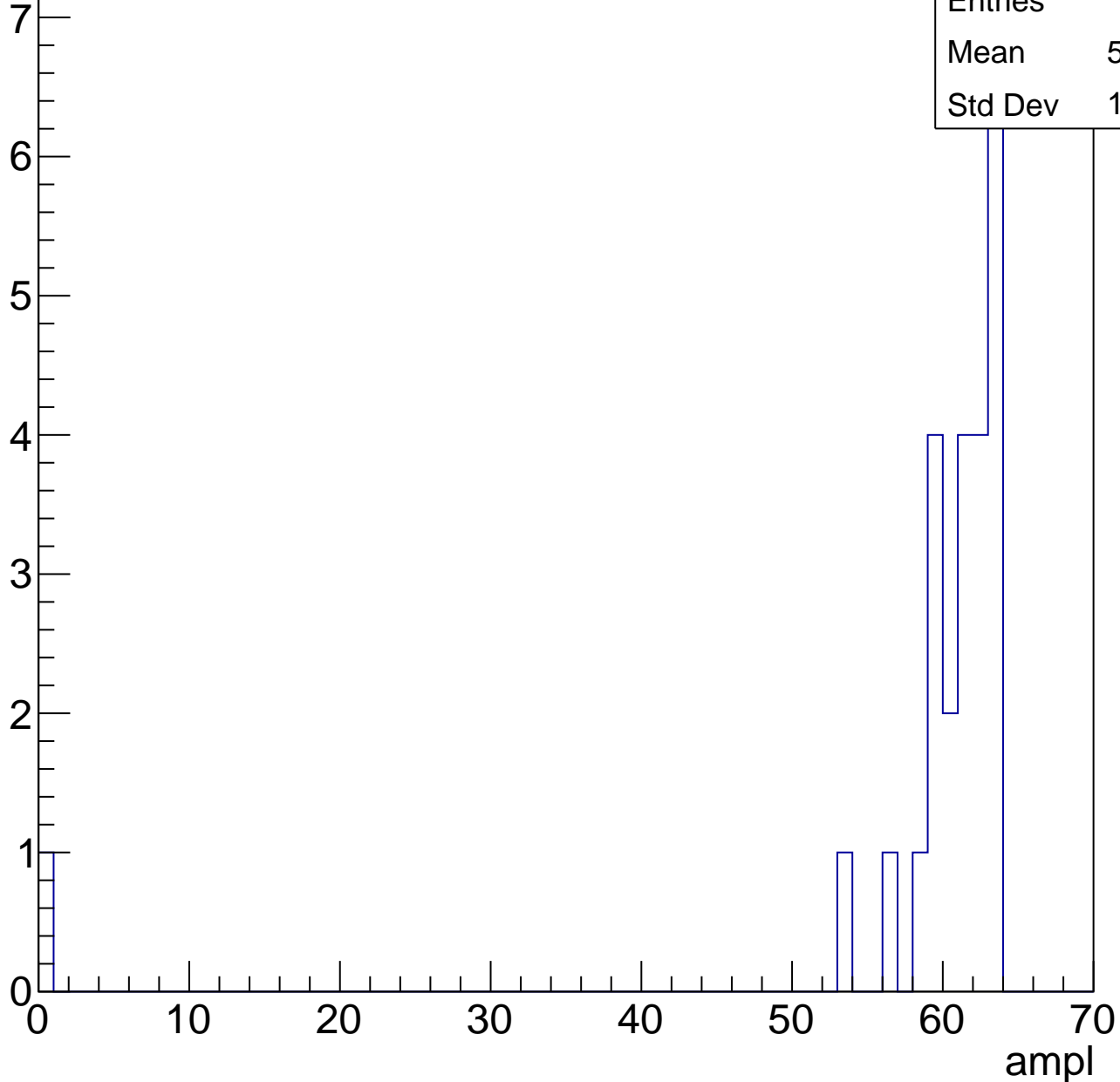


# B1L103S, U3-ch0, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	25
Mean	58.24
Std Dev	12.13



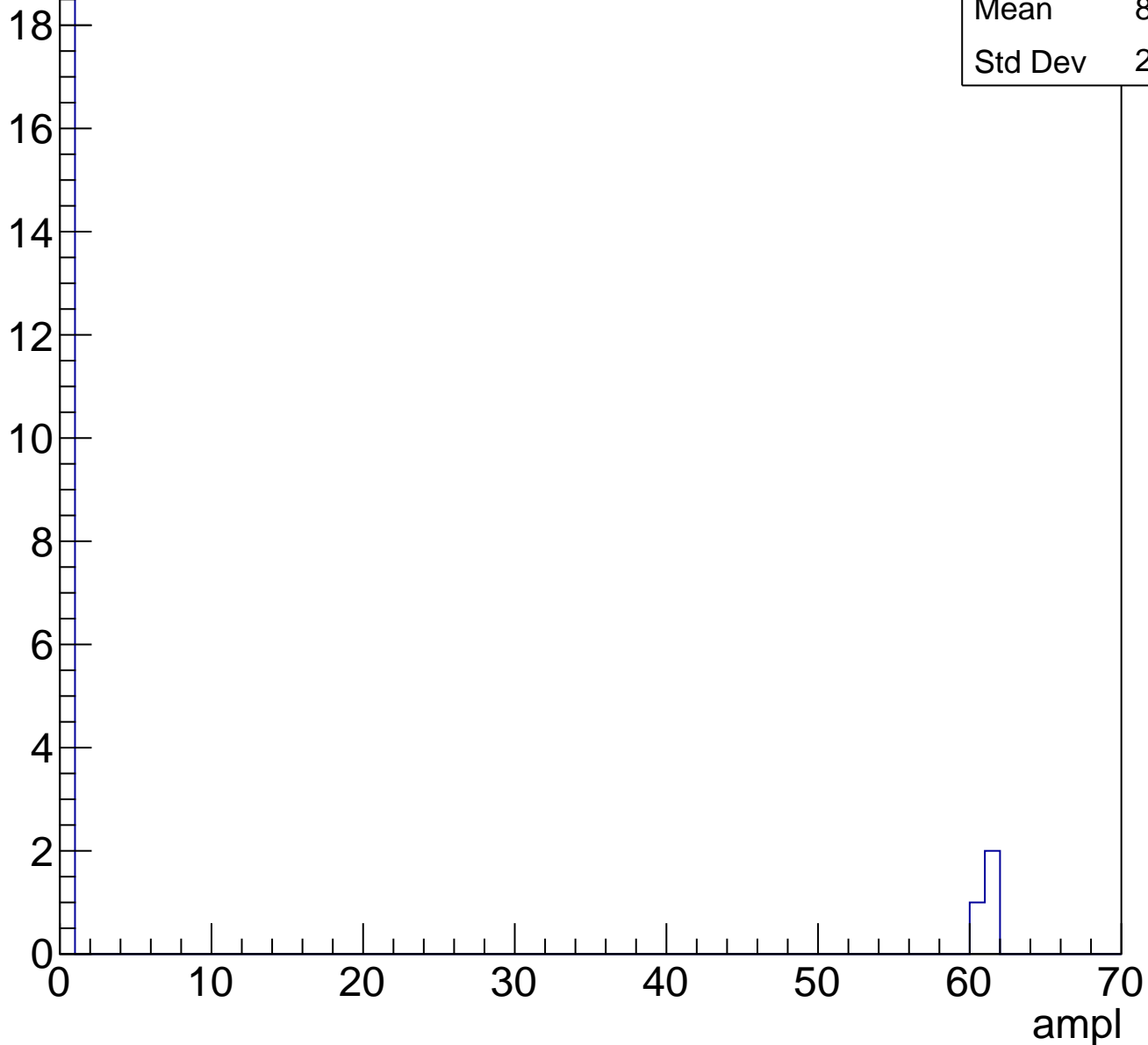


# B1L103S, U3-ch0, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	22
Mean	8.273
Std Dev	20.82

Entry



# B1L103S, U3-ch1, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	78
Mean	22.01
Std Dev	11.1

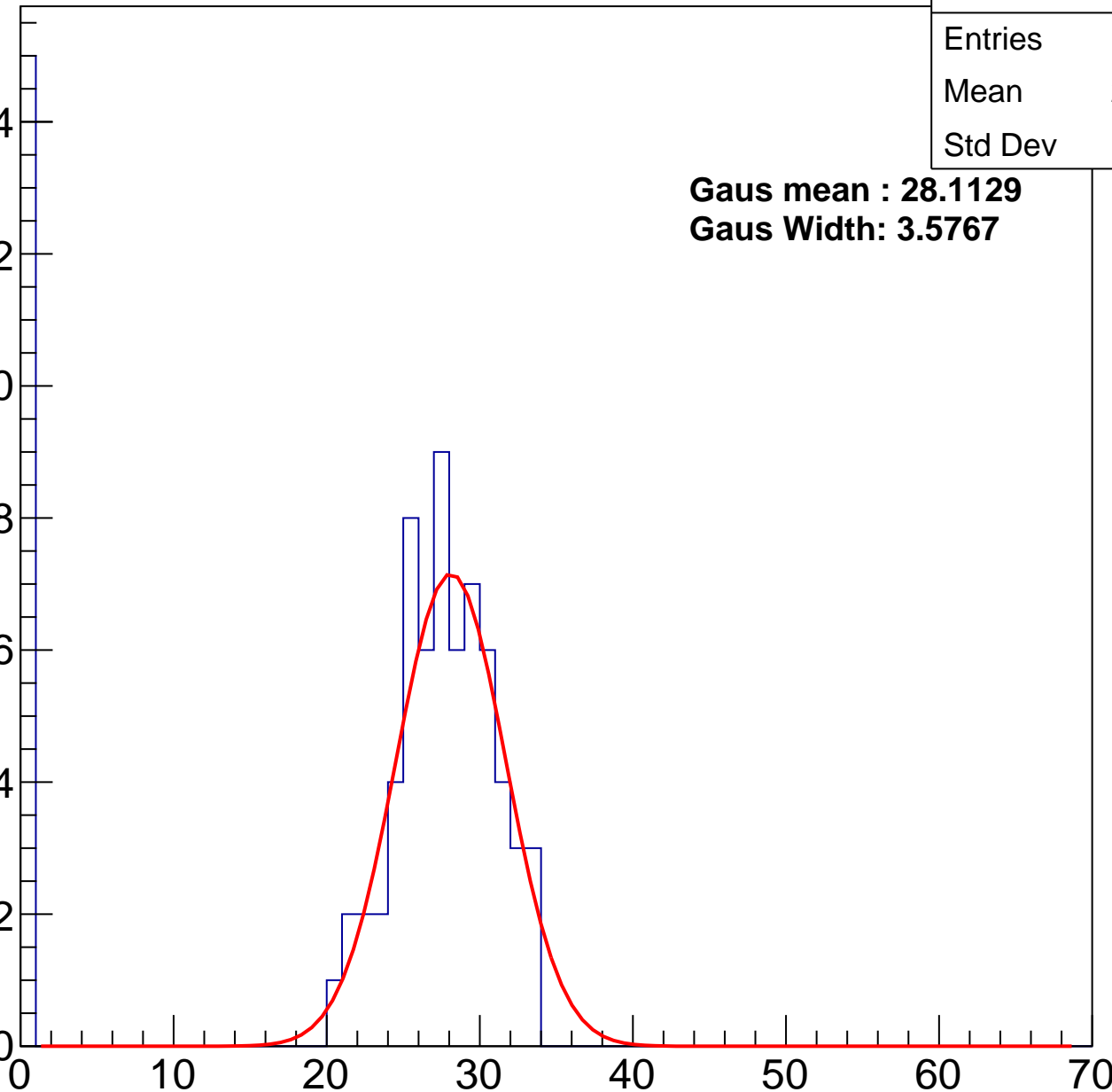
**Gaus mean : 28.1129**

**Gaus Width: 3.5767**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U3-ch1, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	76
Mean	34
Std Dev	5.132

**Gaus mean : 35.2611**

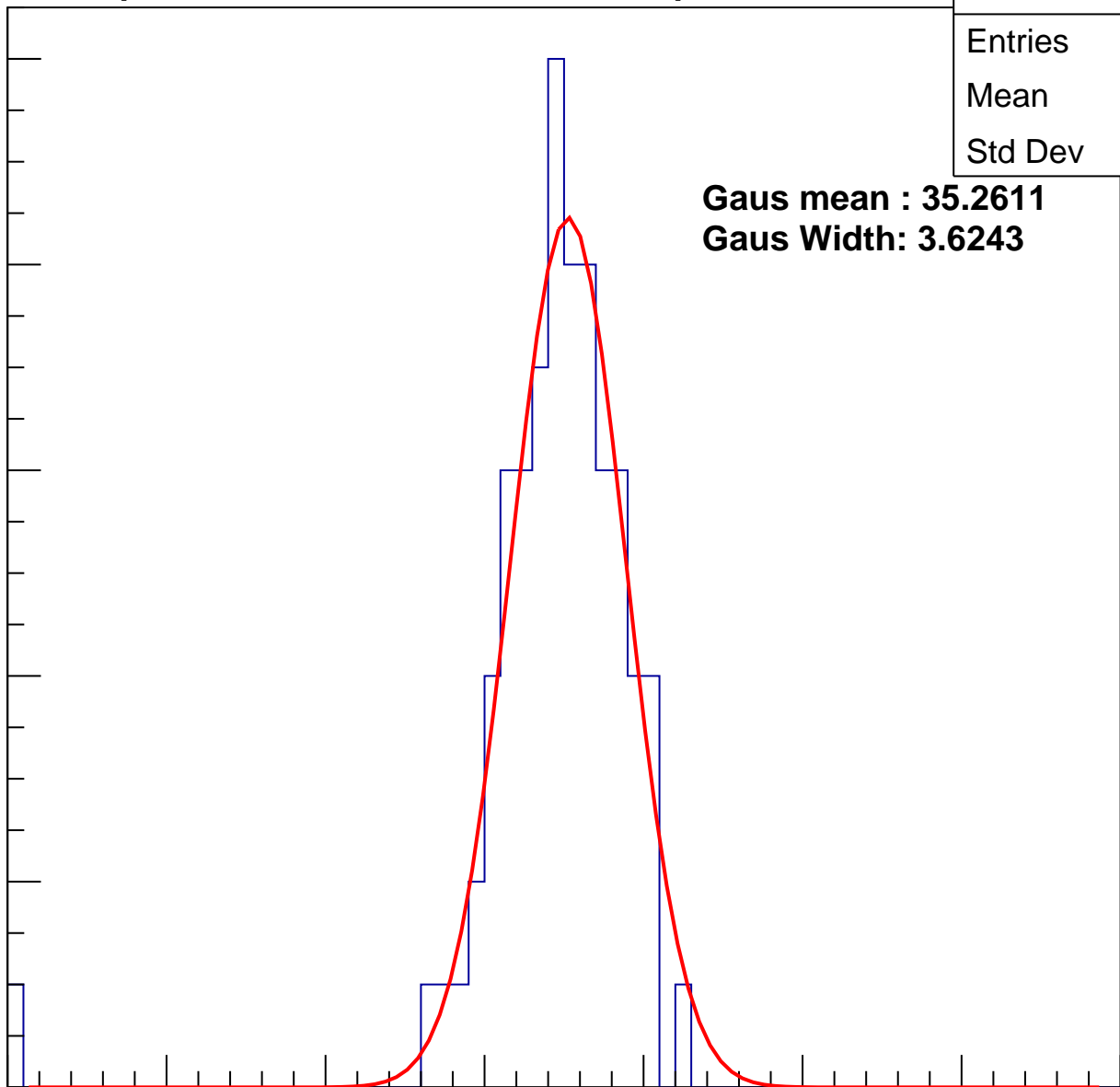
**Gaus Width: 3.6243**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch1, adc2

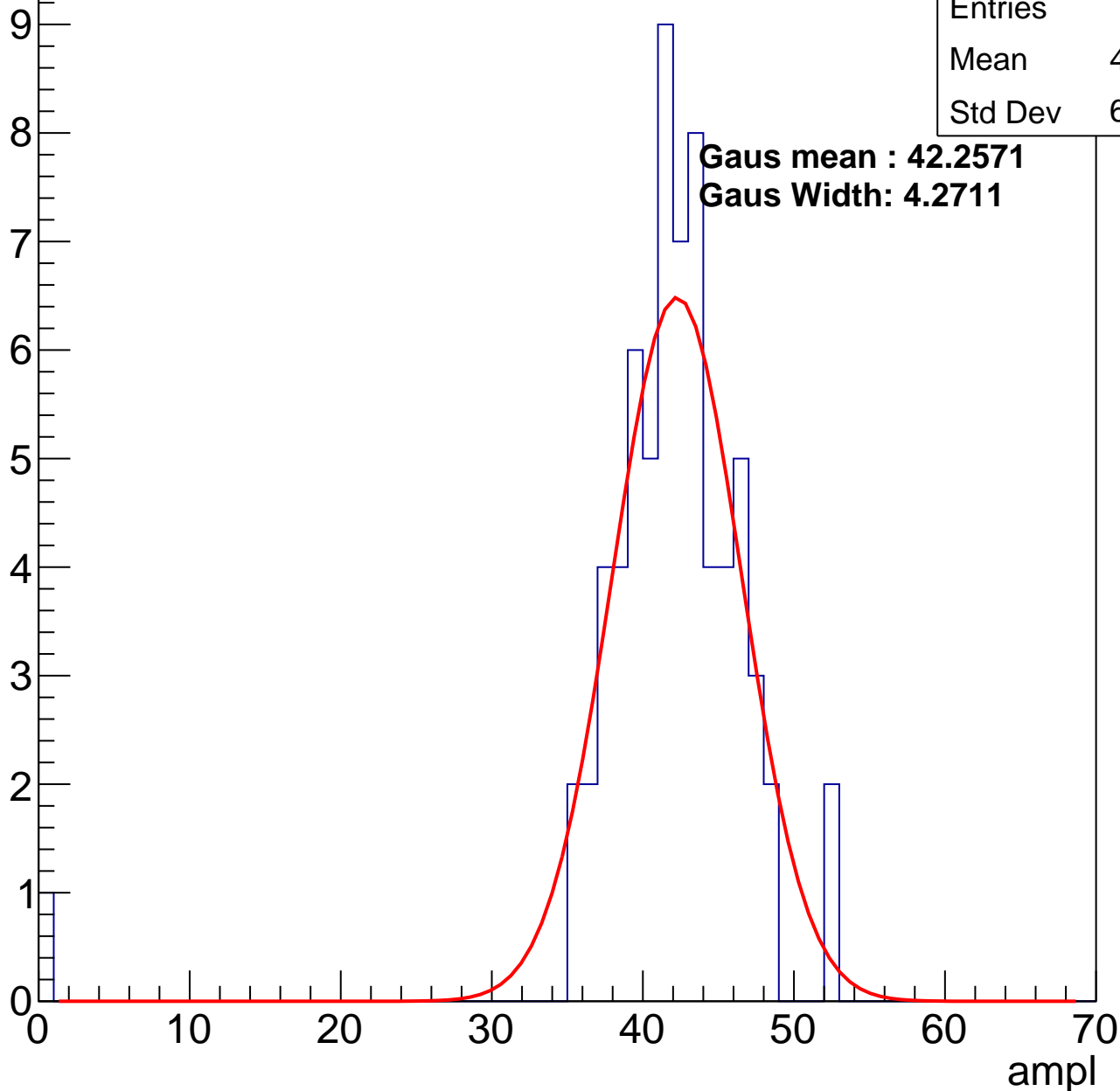
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	41.32
Std Dev	6.227

**Gaus mean : 42.2571**

**Gaus Width: 4.2711**



# B1L103S, U3-ch1, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	75
Mean	40.83
Std Dev	17.23

Entry

10

8

6

4

2

0

0

10

20

30

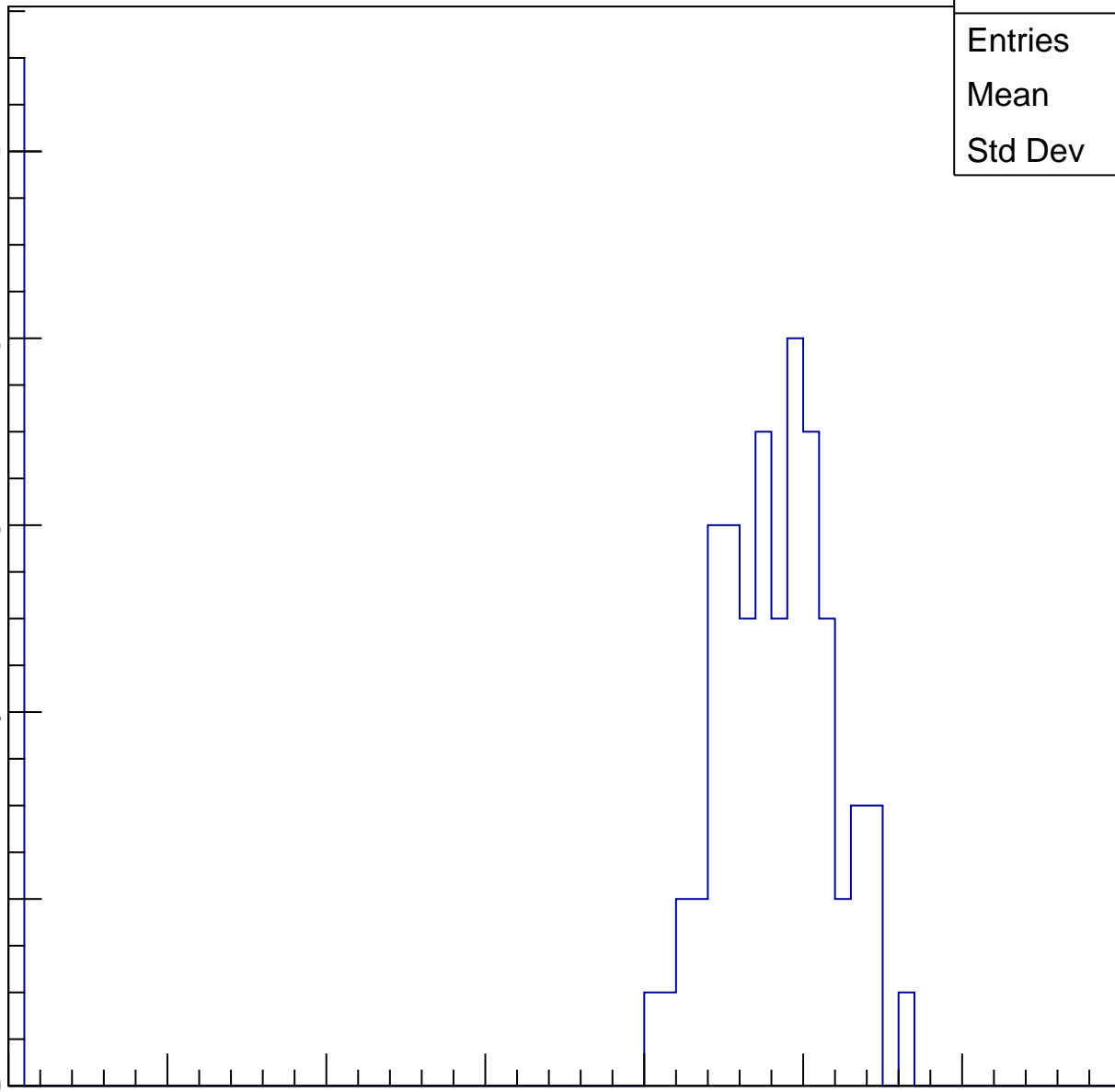
40

50

60

70

ampl

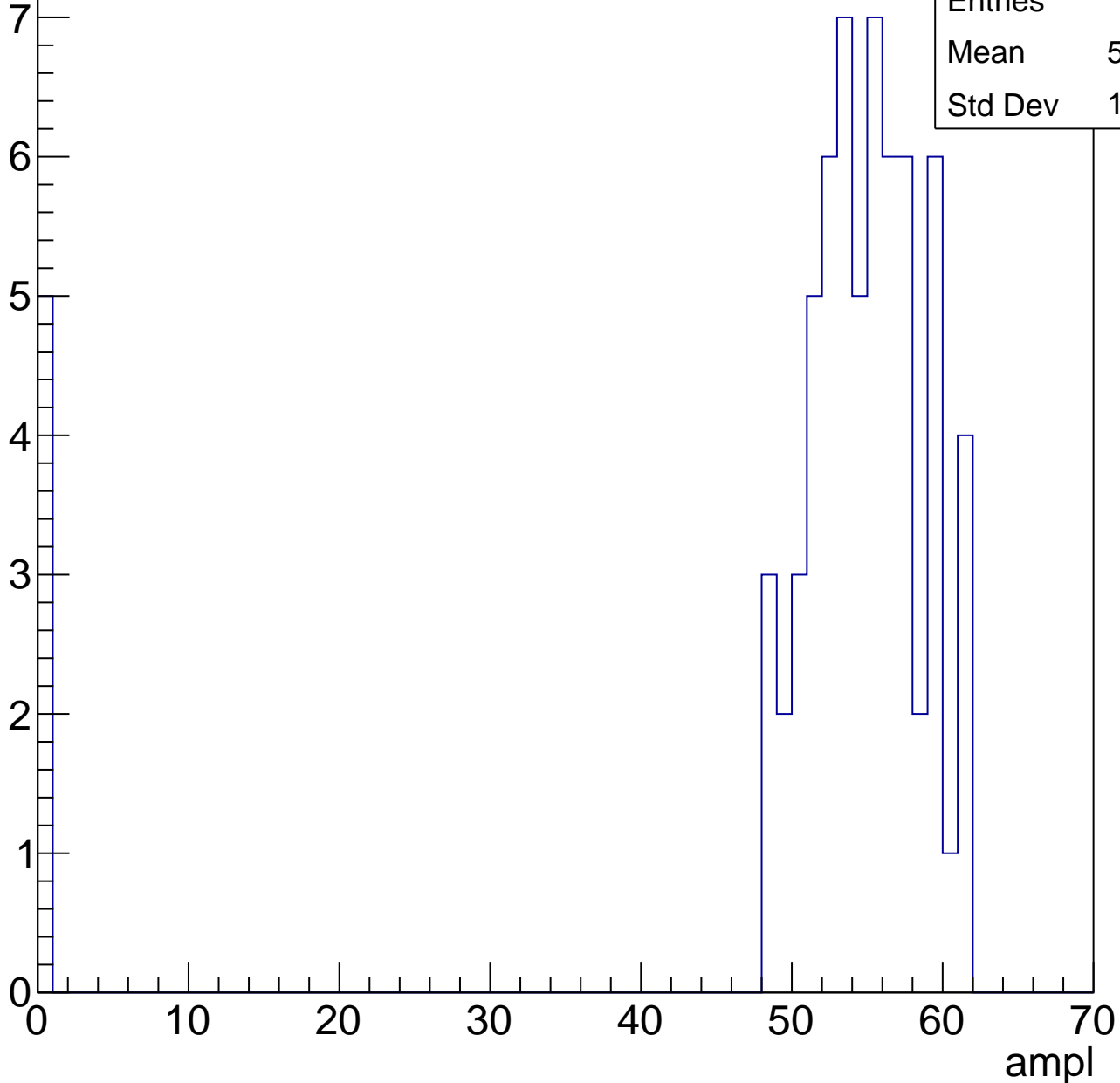


# B1L103S, U3-ch1, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

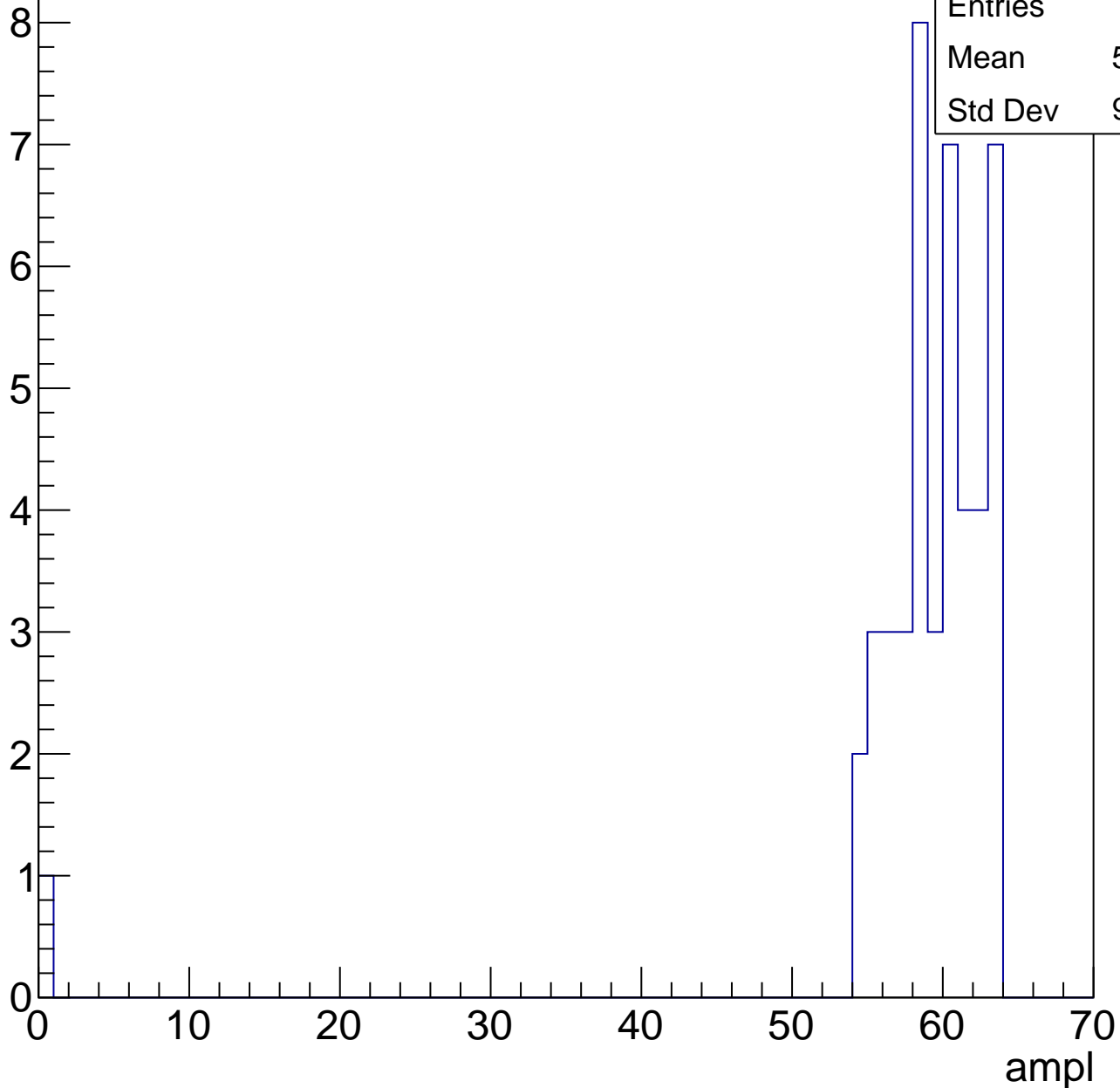
Entries	68
Mean	50.54
Std Dev	14.63



# B1L103S, U3-ch1, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

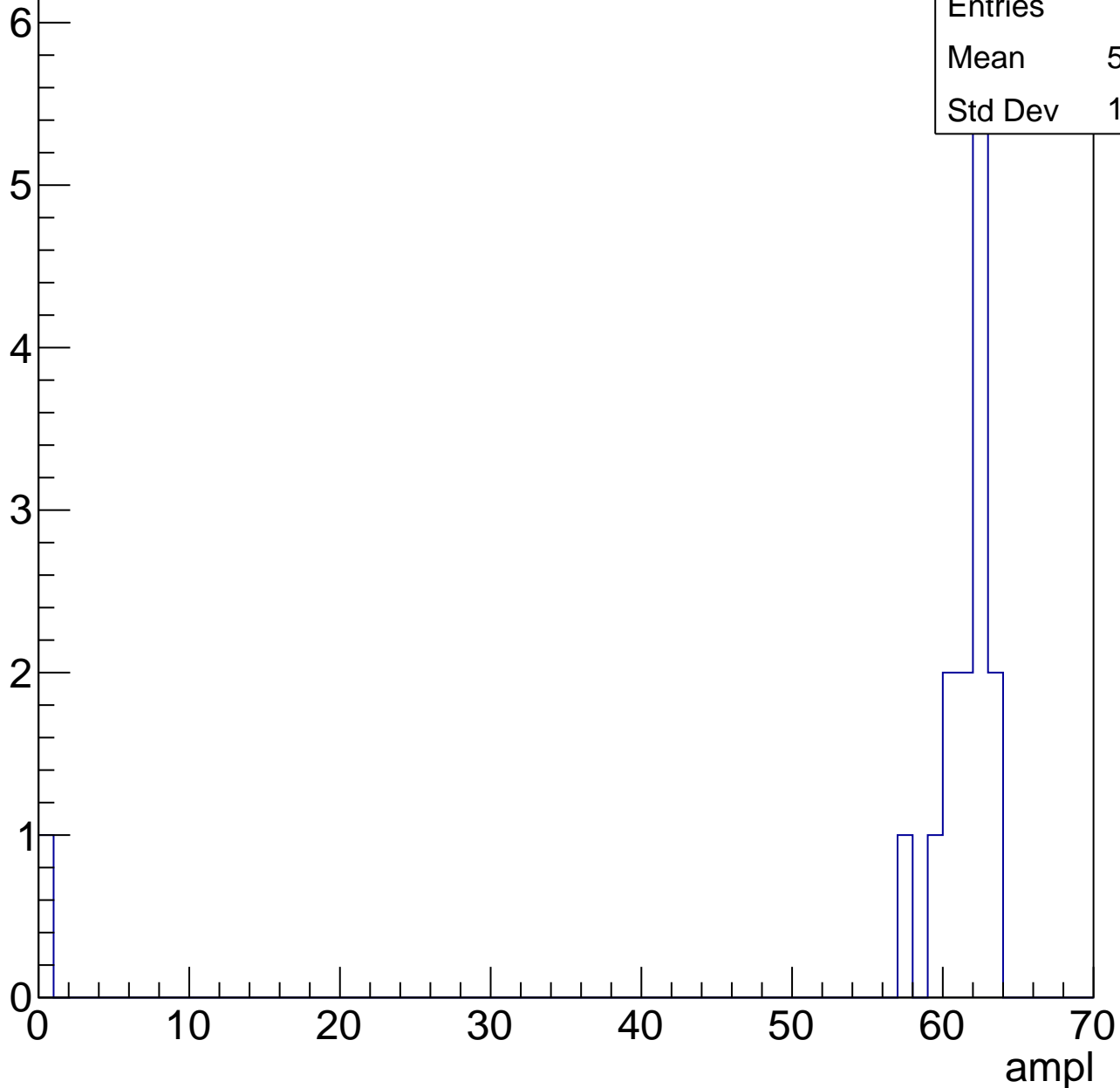


# B1L103S, U3-ch1, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	15
Mean	57.07
Std Dev	15.33





# B1L103S, U3-ch1, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73



# B1L103S, U3-ch2, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	78
Mean	25.37
Std Dev	10.73

**Gaus mean : 29.9617**

**Gaus Width: 3.1350**

Entry

10

8

6

4

2

0

0

10

20

30

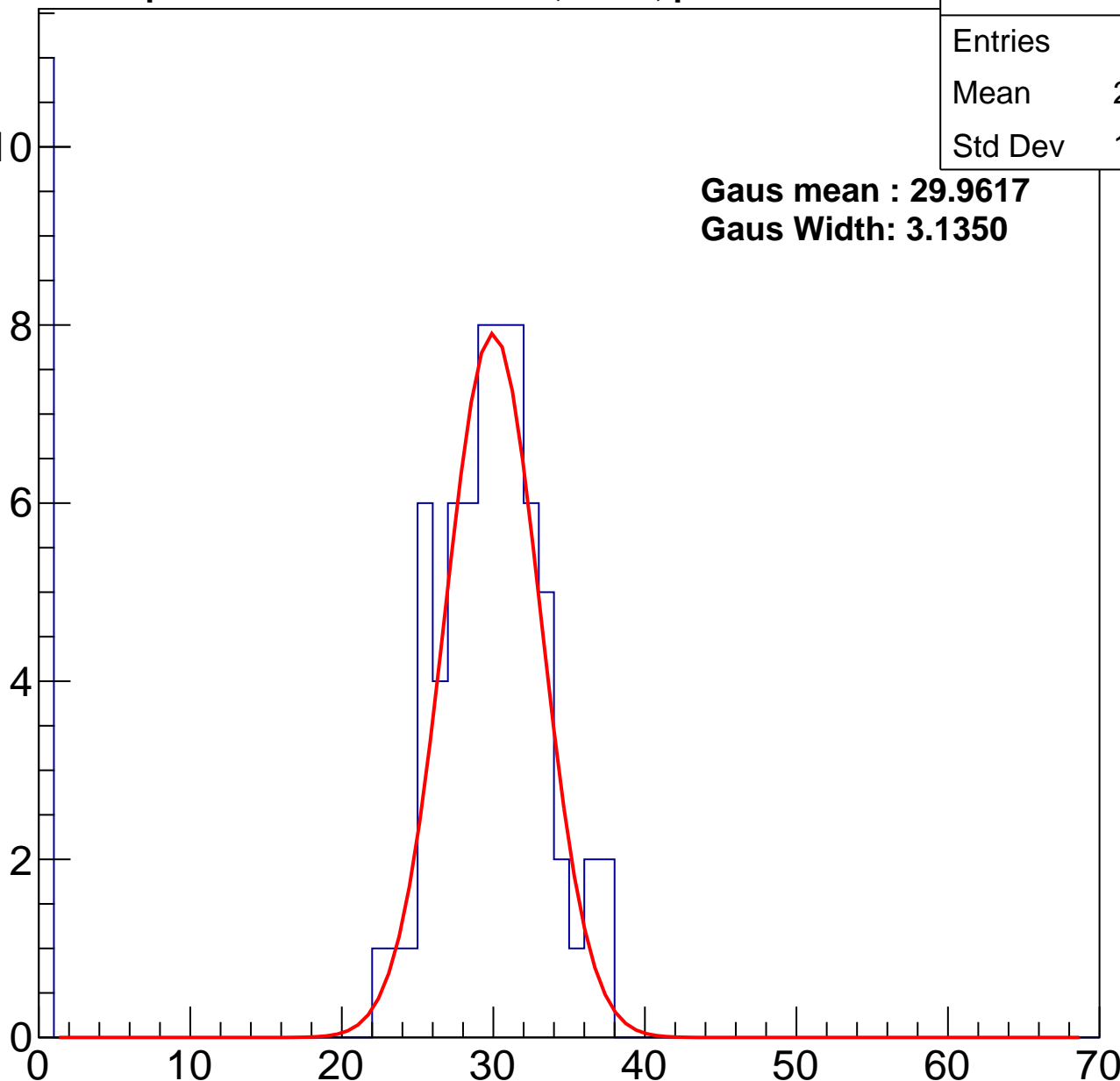
40

50

60

70

ampl



# B1L103S, U3-ch2, adc1

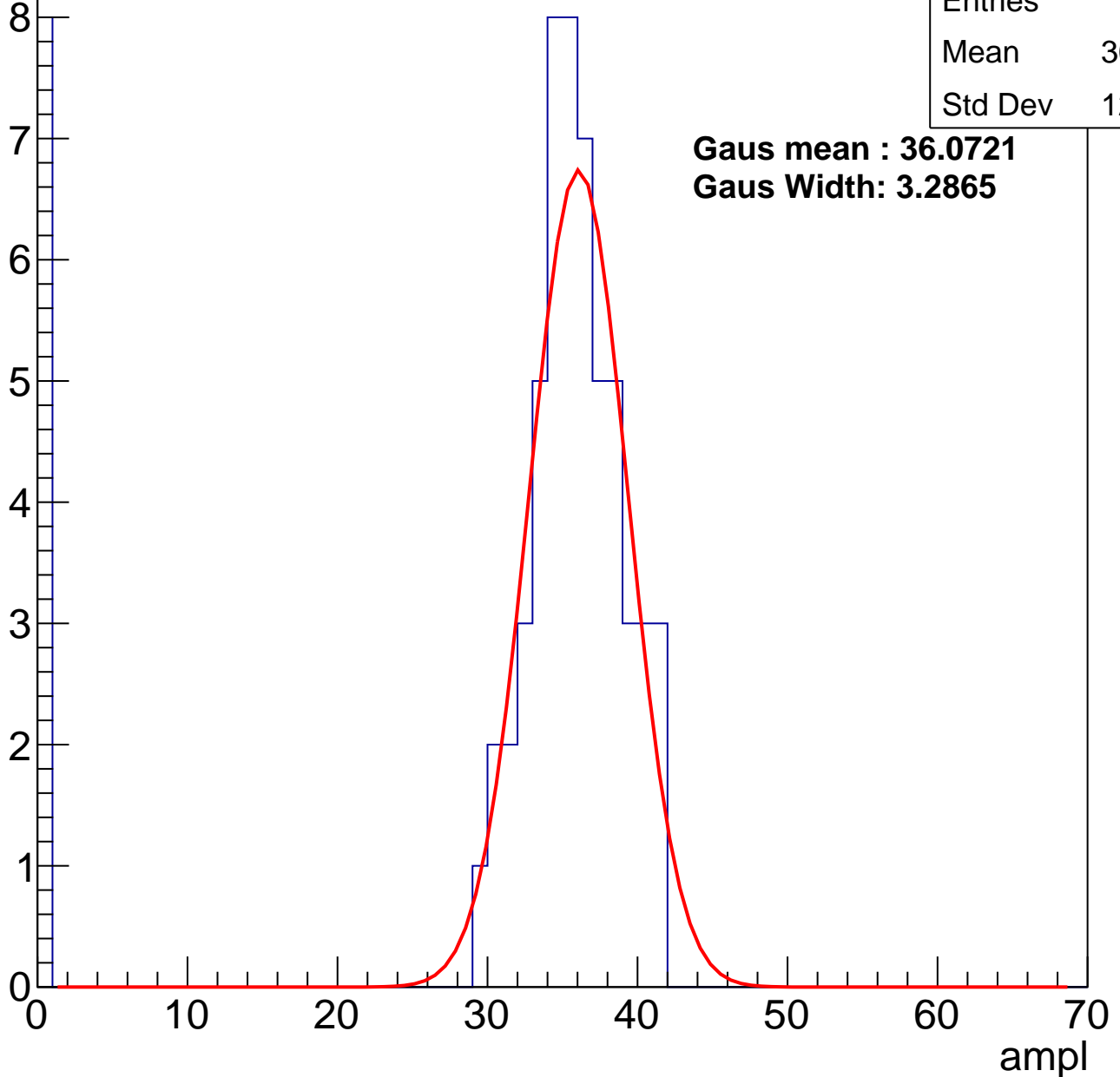
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	30.97
Std Dev	12.12

**Gaus mean : 36.0721**

**Gaus Width: 3.2865**



# B1L103S, U3-ch2, adc2

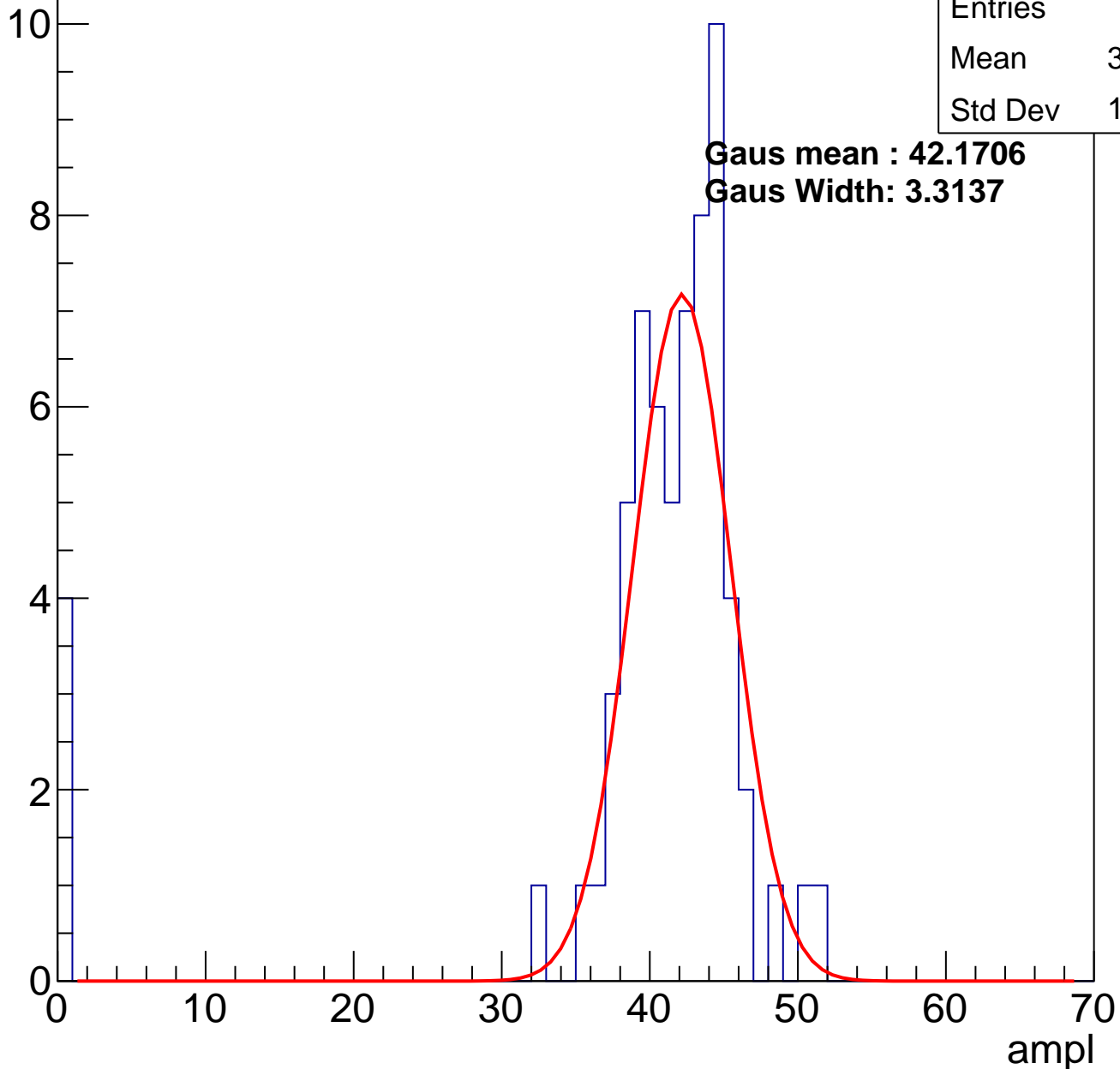
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	67
Mean	39.12
Std Dev	10.39

**Gaus mean : 42.1706**

**Gaus Width: 3.3137**

Entry

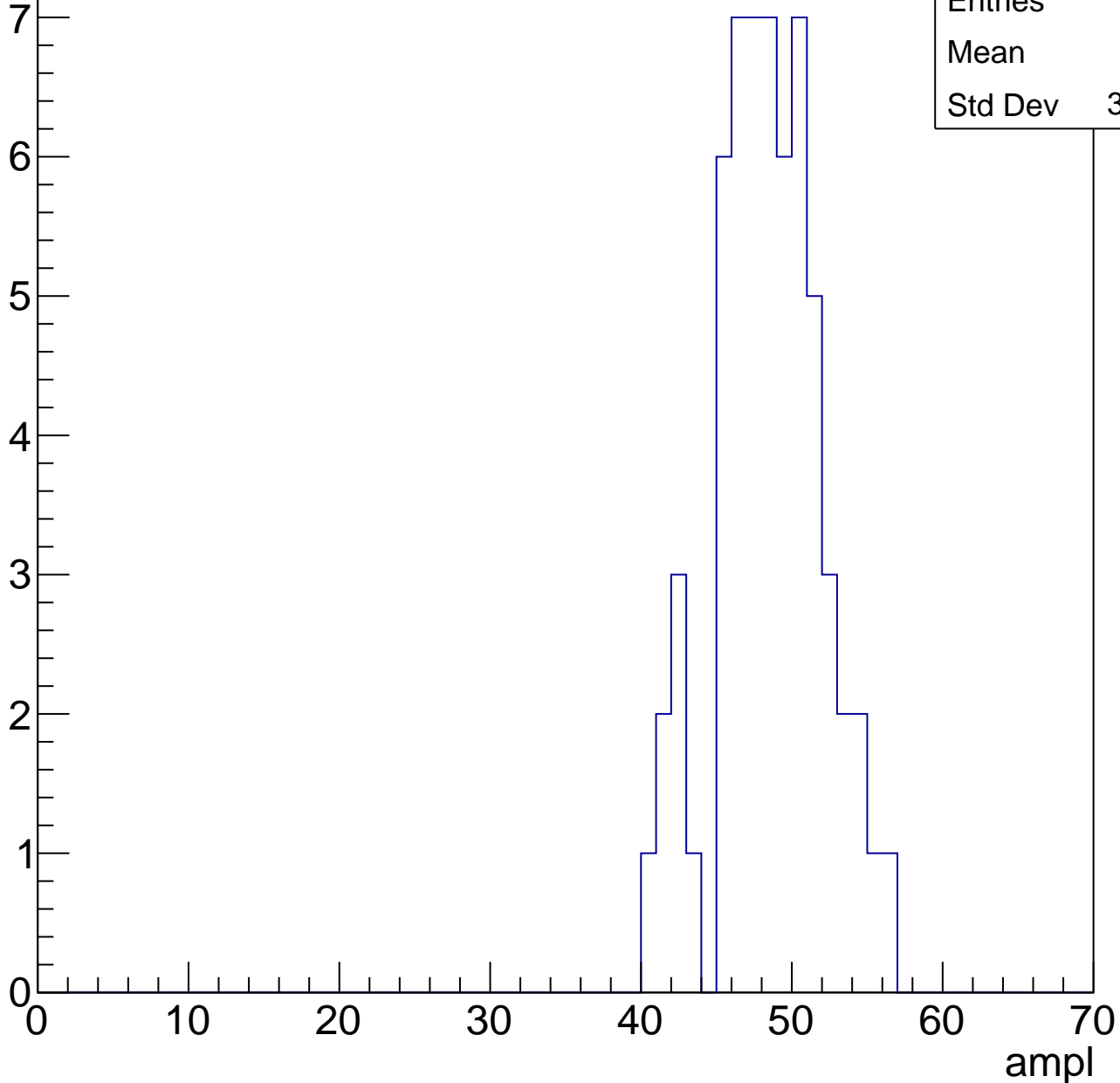


# B1L103S, U3-ch2, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	48
Std Dev	3.497

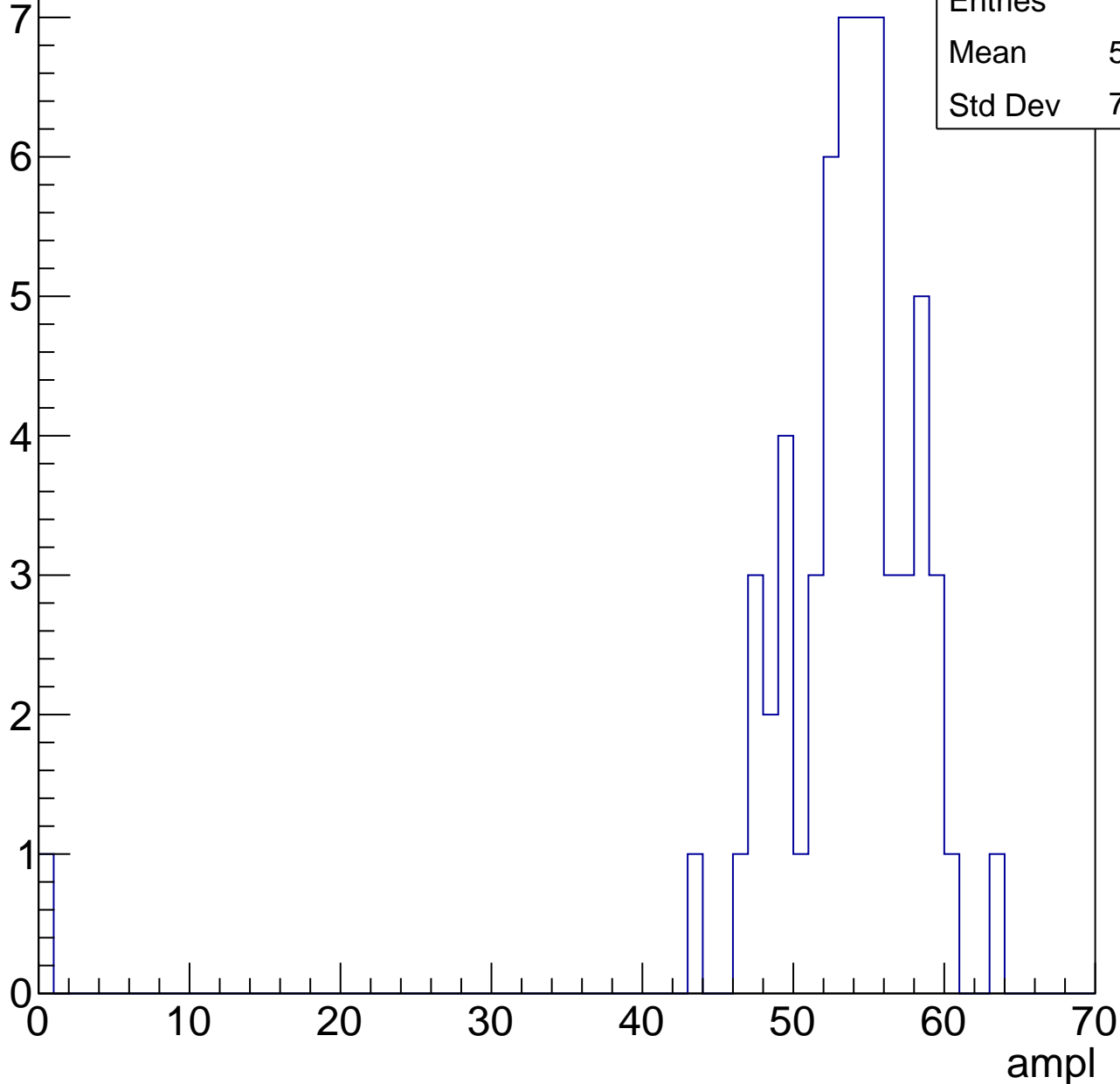


# B1L103S, U3-ch2, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	52.54
Std Dev	7.905

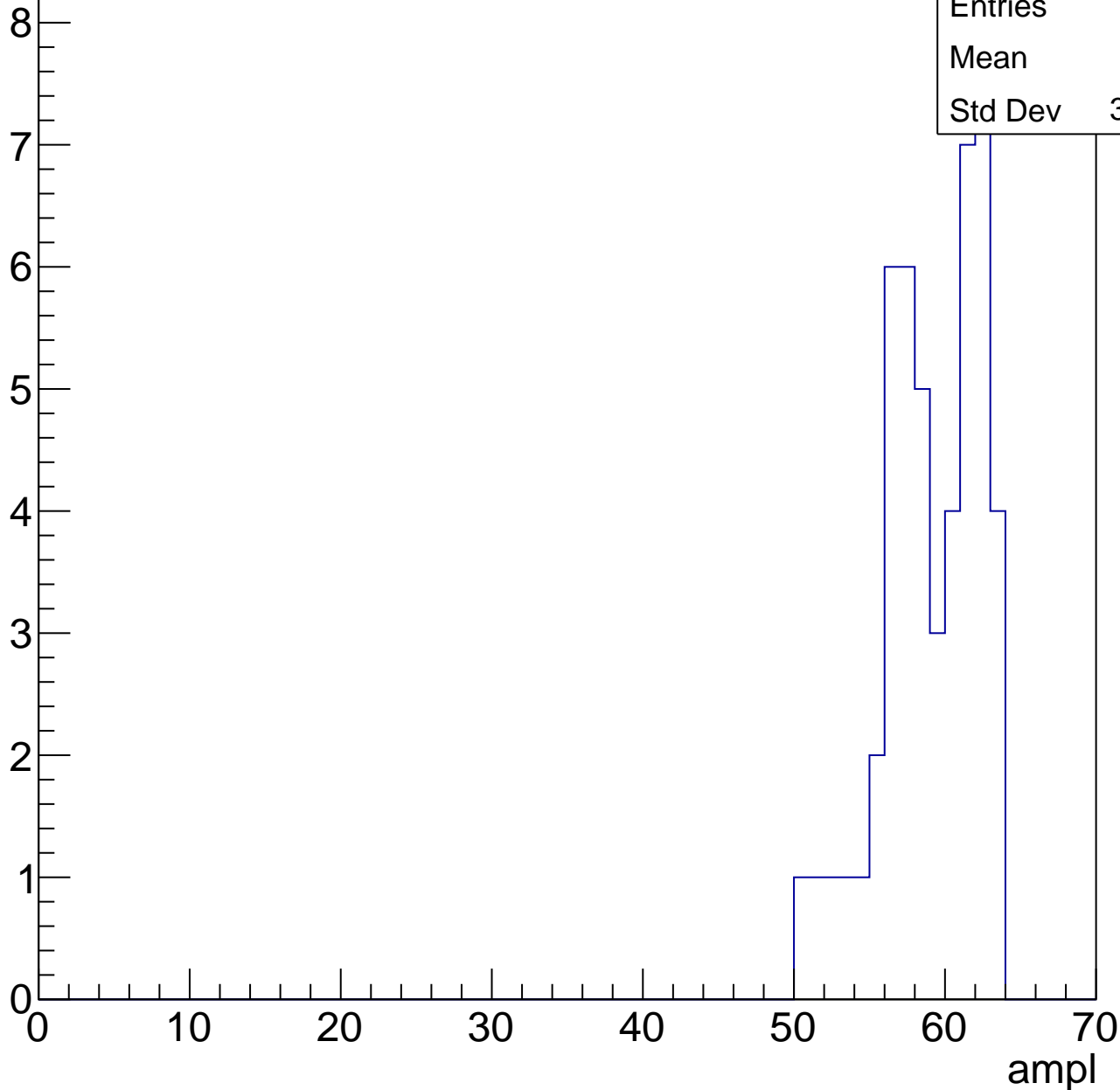


# B1L103S, U3-ch2, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	50
Mean	58.6
Std Dev	3.256

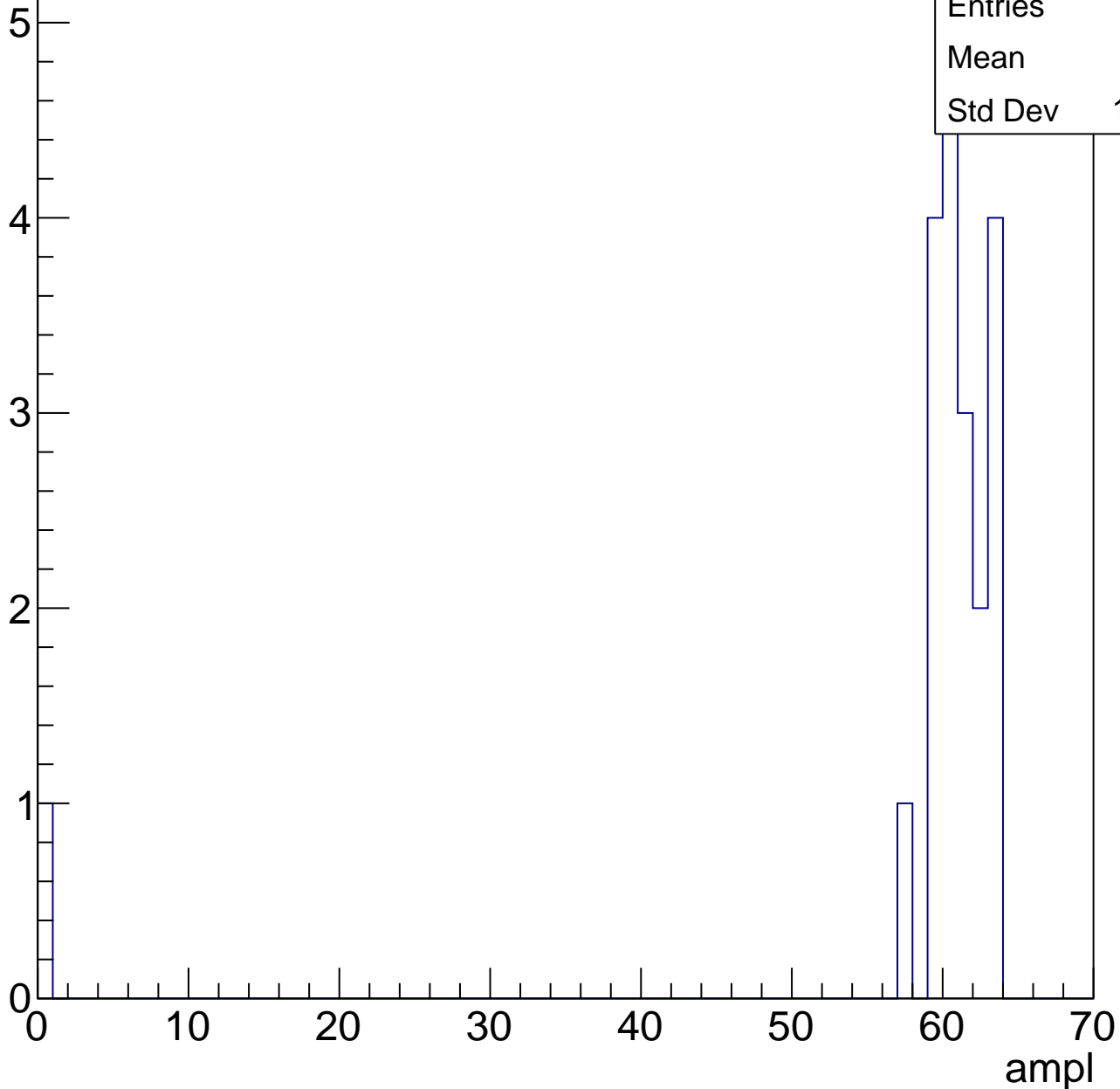


# B1L103S, U3-ch2, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	20
Mean	57.6
Std Dev	13.31



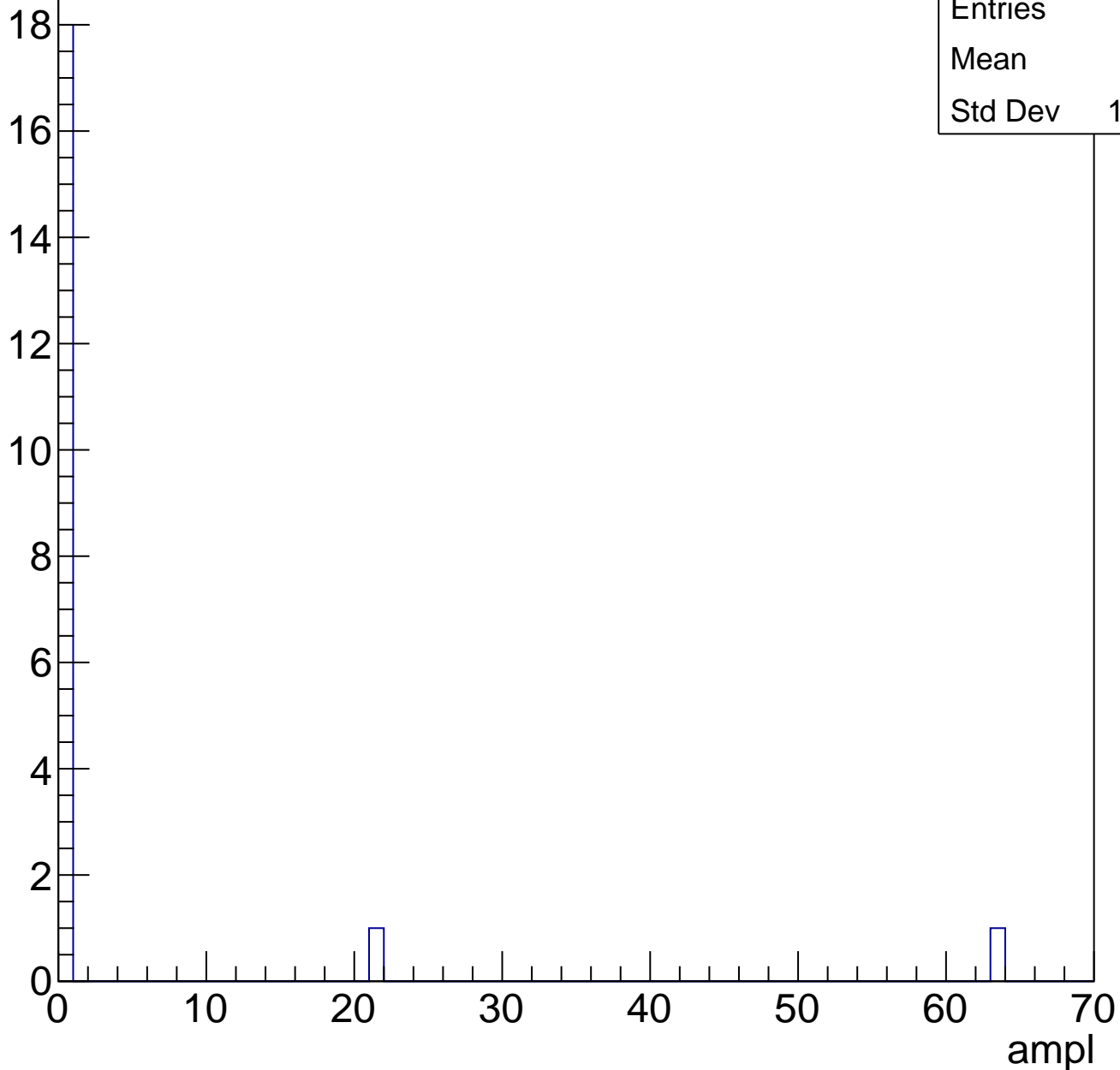


# B1L103S, U3-ch2, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	4.2
Std Dev	14.24

Entry



# B1L103S, U3-ch3, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	72
Mean	21.74
Std Dev	13.86

**Gaus mean : 31.3337**

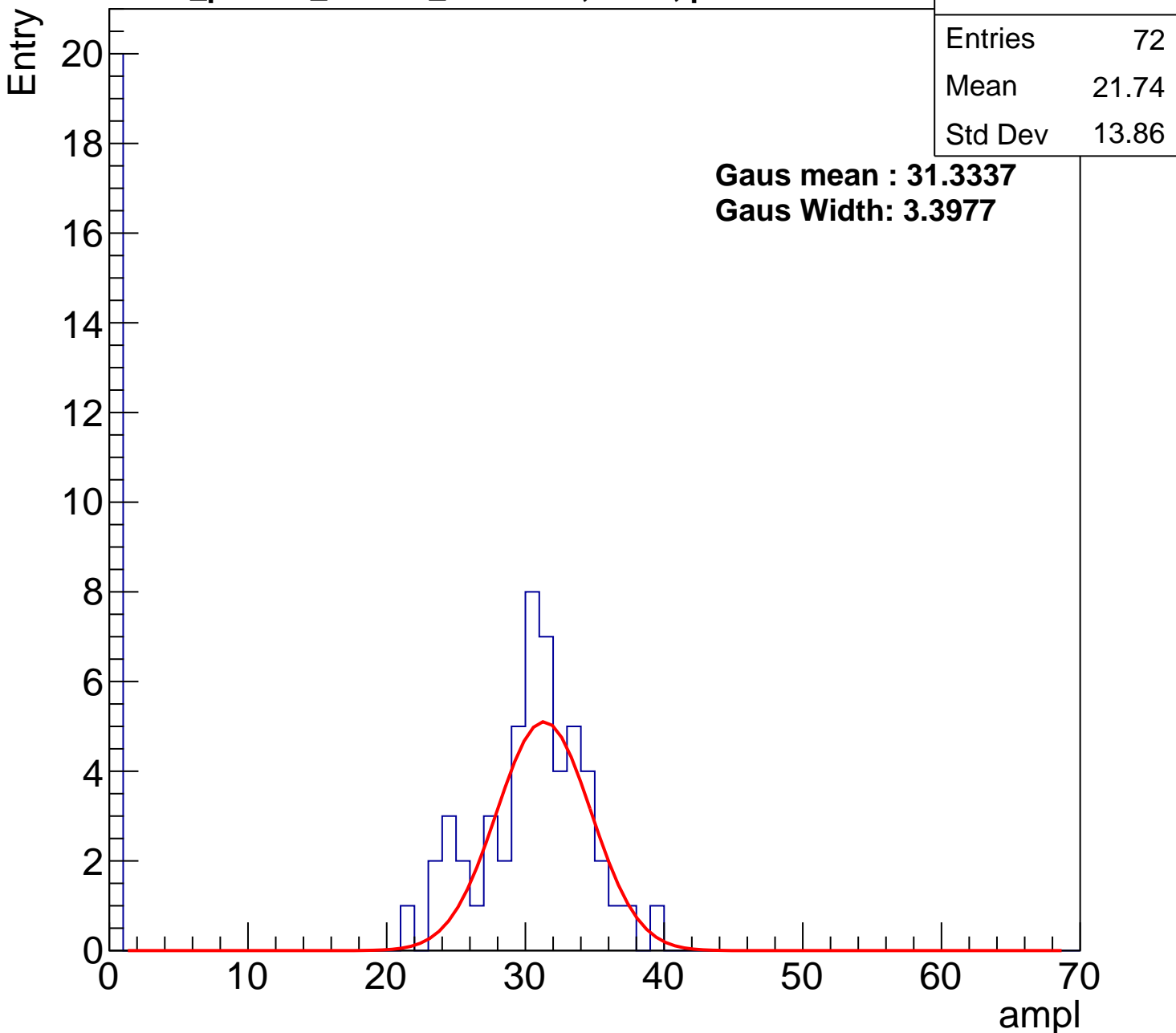
**Gaus Width: 3.3977**

Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch3, adc1

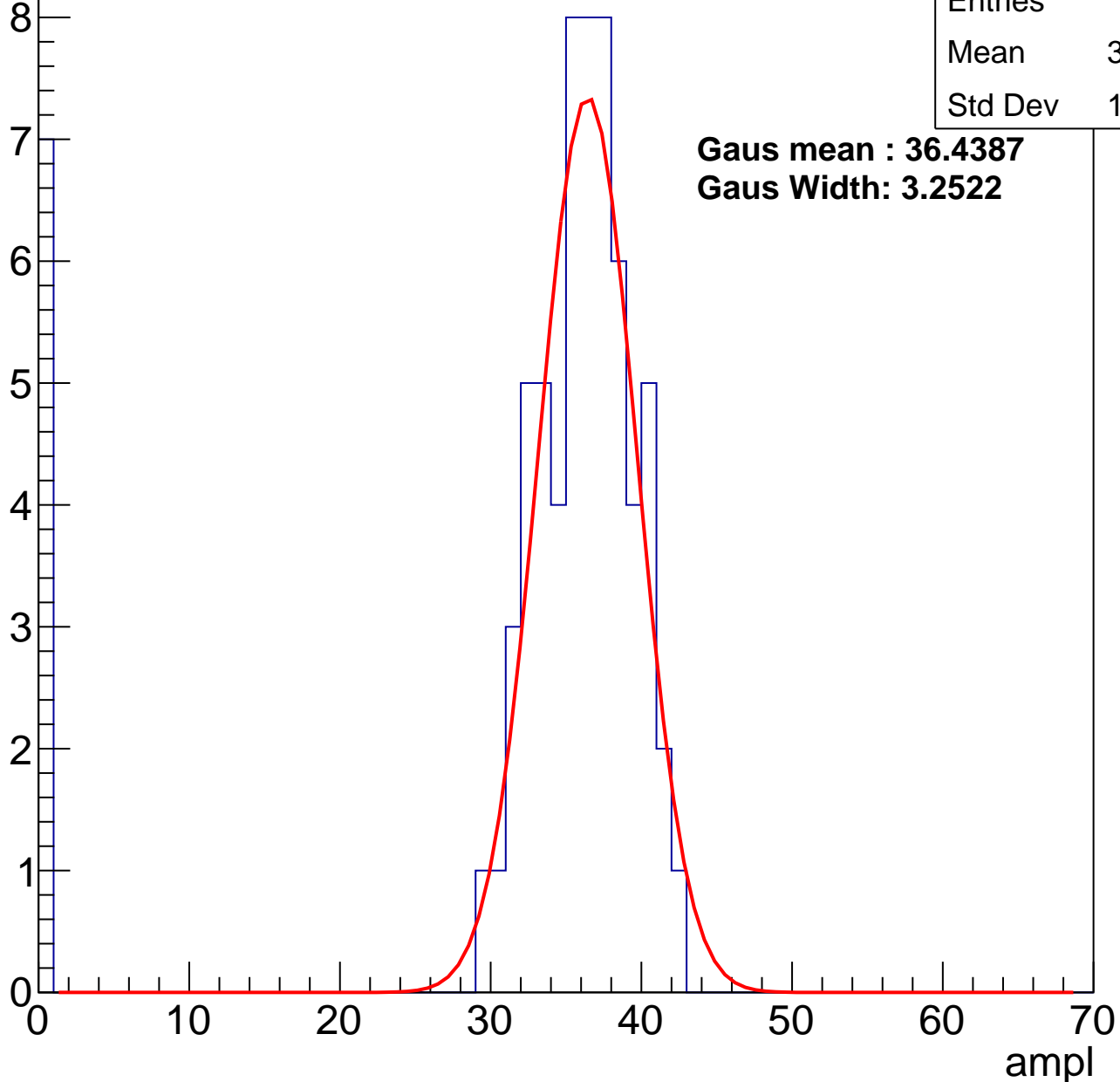
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	32.13
Std Dev	11.24

**Gaus mean : 36.4387**

**Gaus Width: 3.2522**



# B1L103S, U3-ch3, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	76
Mean	35.89
Std Dev	15.08

**Gaus mean : 42.7570**

**Gaus Width: 2.8235**

Entry

10

8

6

4

2

0

0

10

20

30

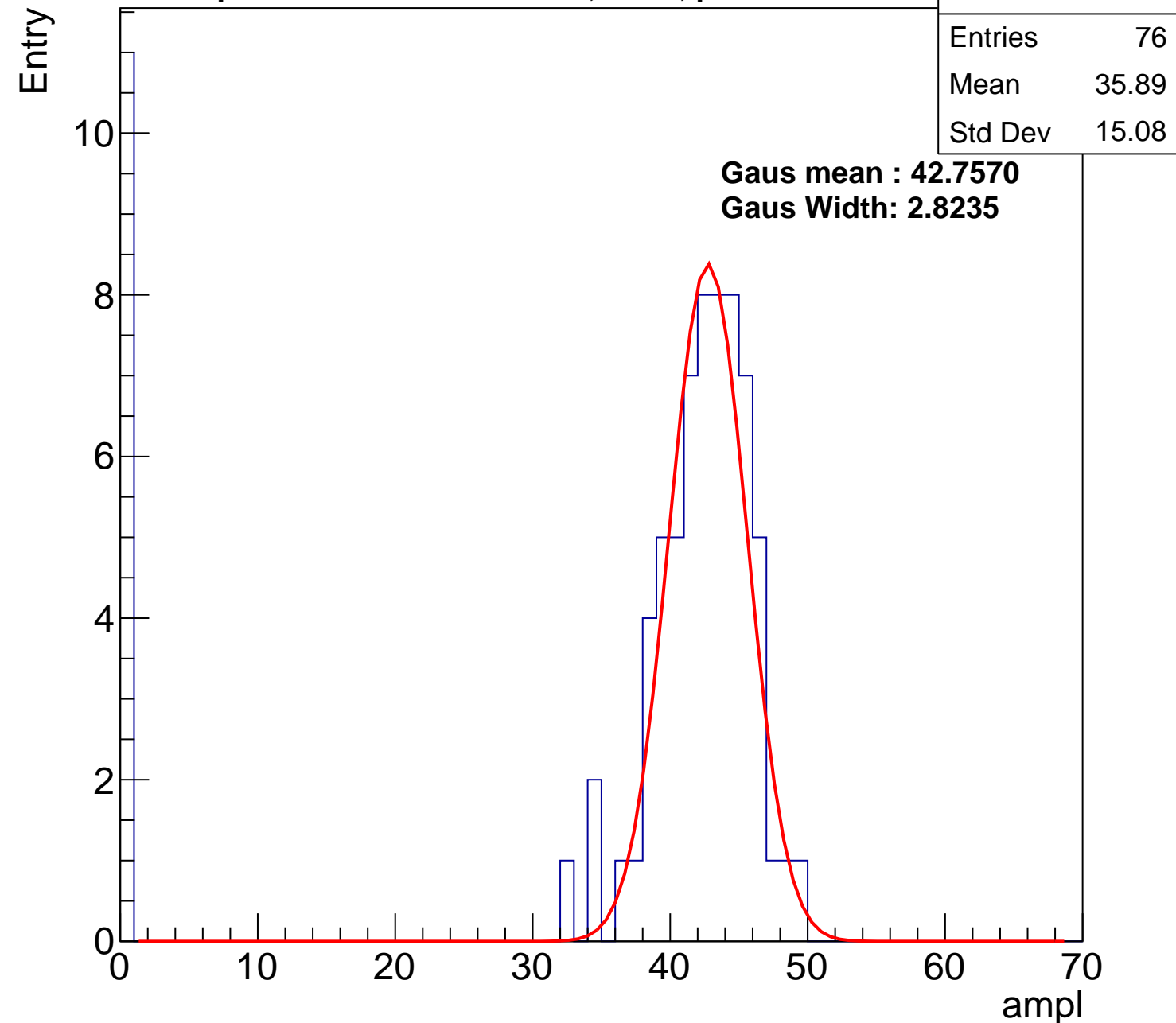
40

50

60

70

ampl

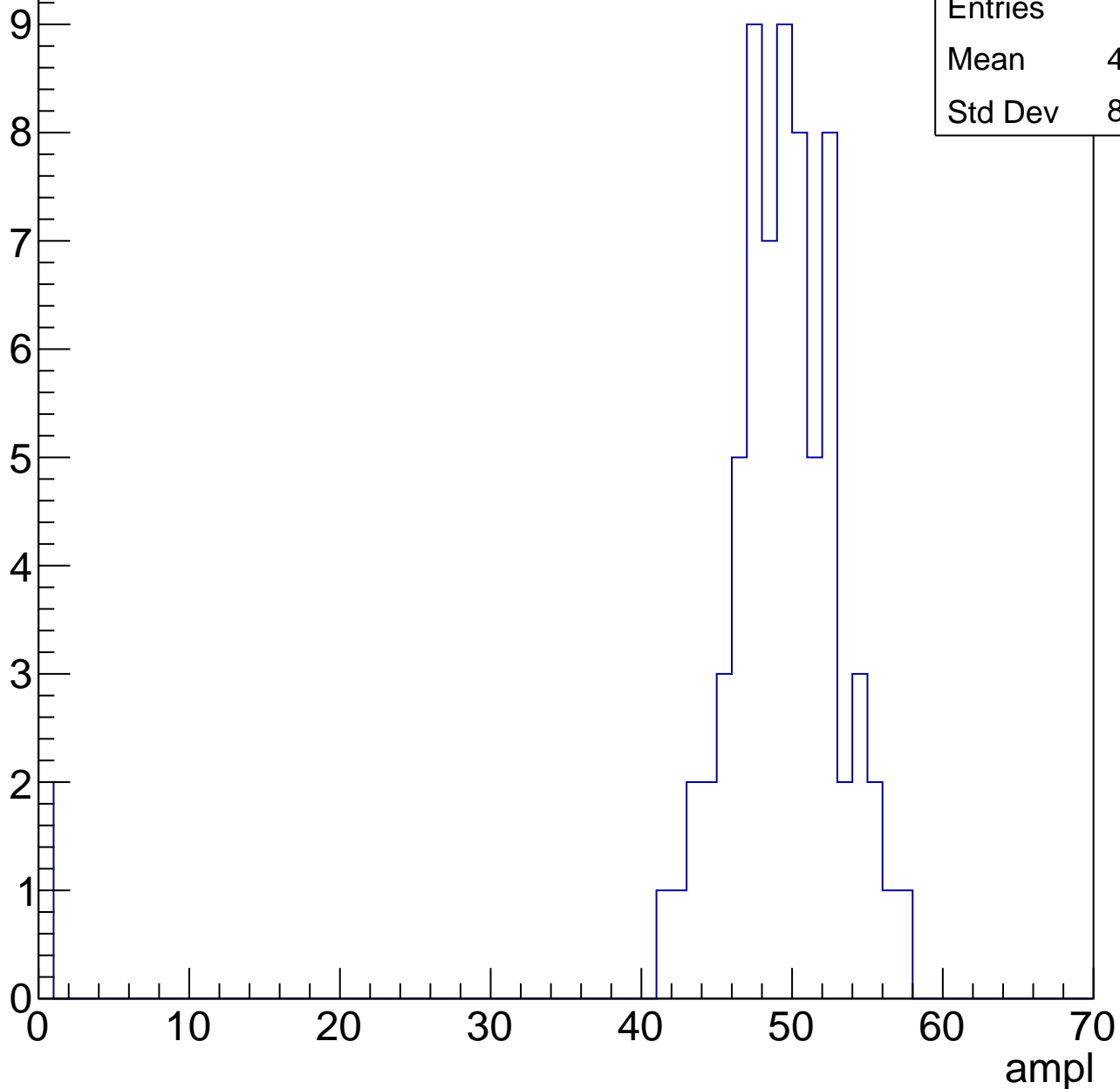


# B1L103S, U3-ch3, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	71
Mean	47.66
Std Dev	8.752

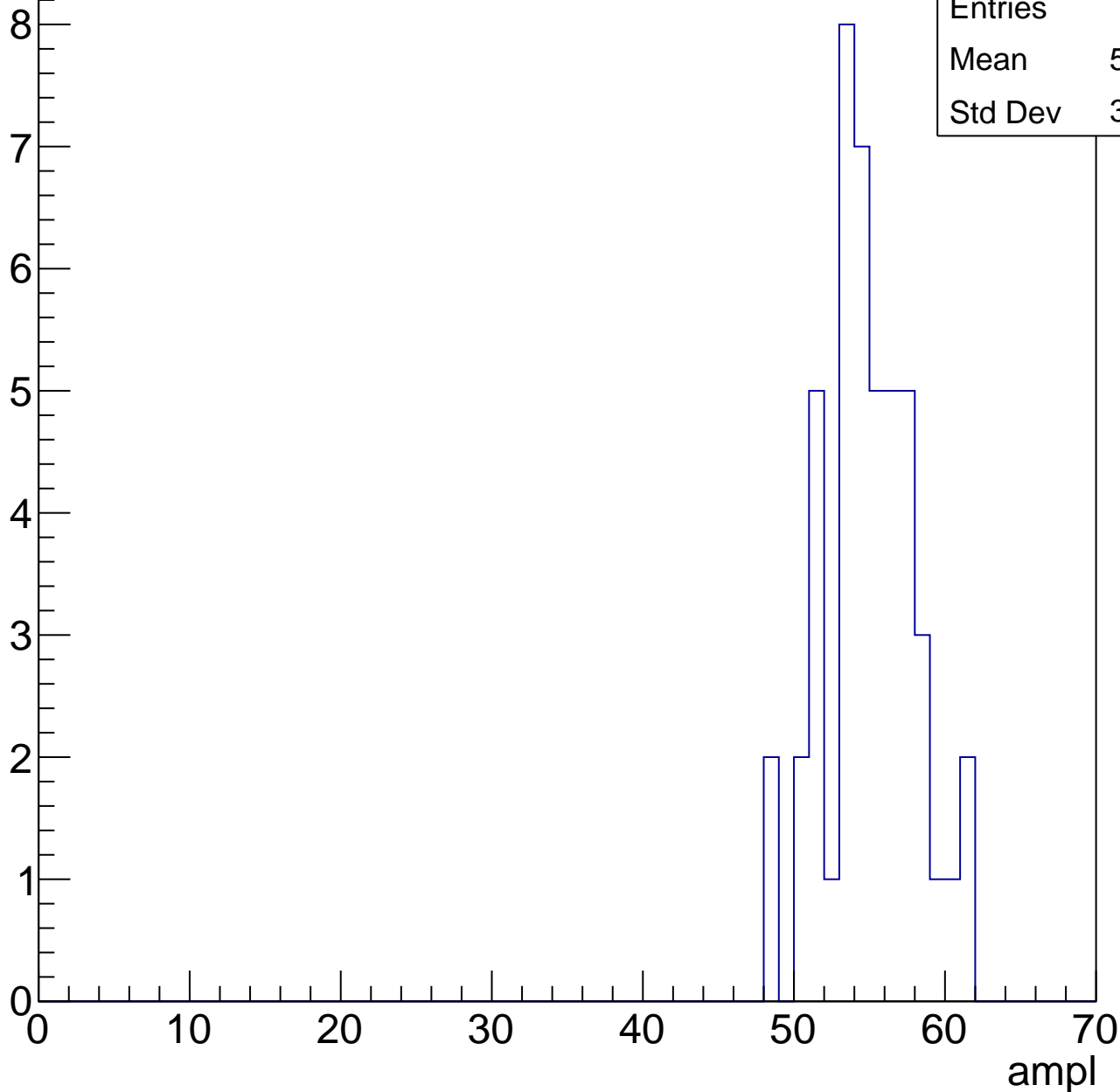


# B1L103S, U3-ch3, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

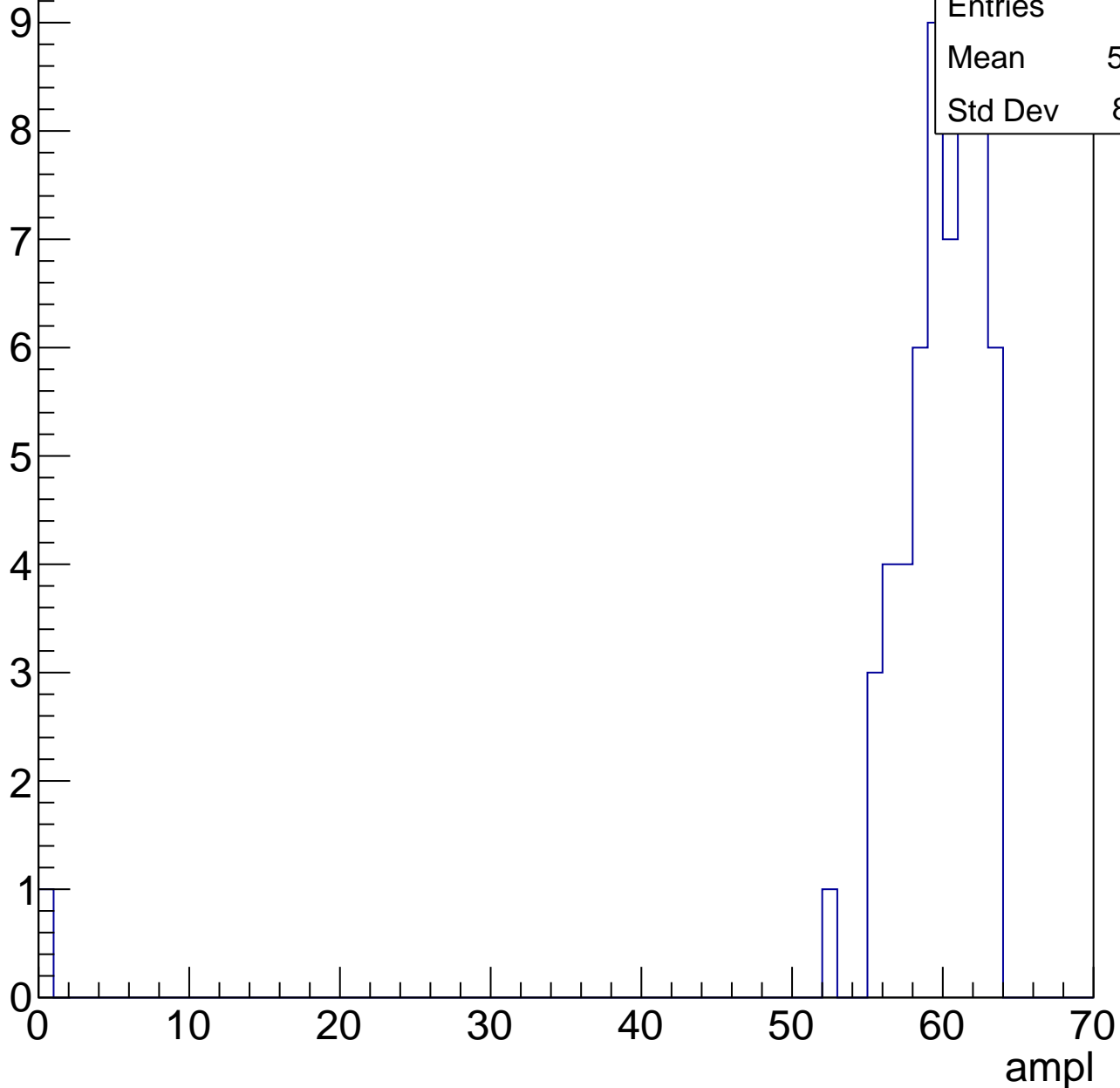
Entries	47
Mean	54.47
Std Dev	3.017



# B1L103S, U3-ch3, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

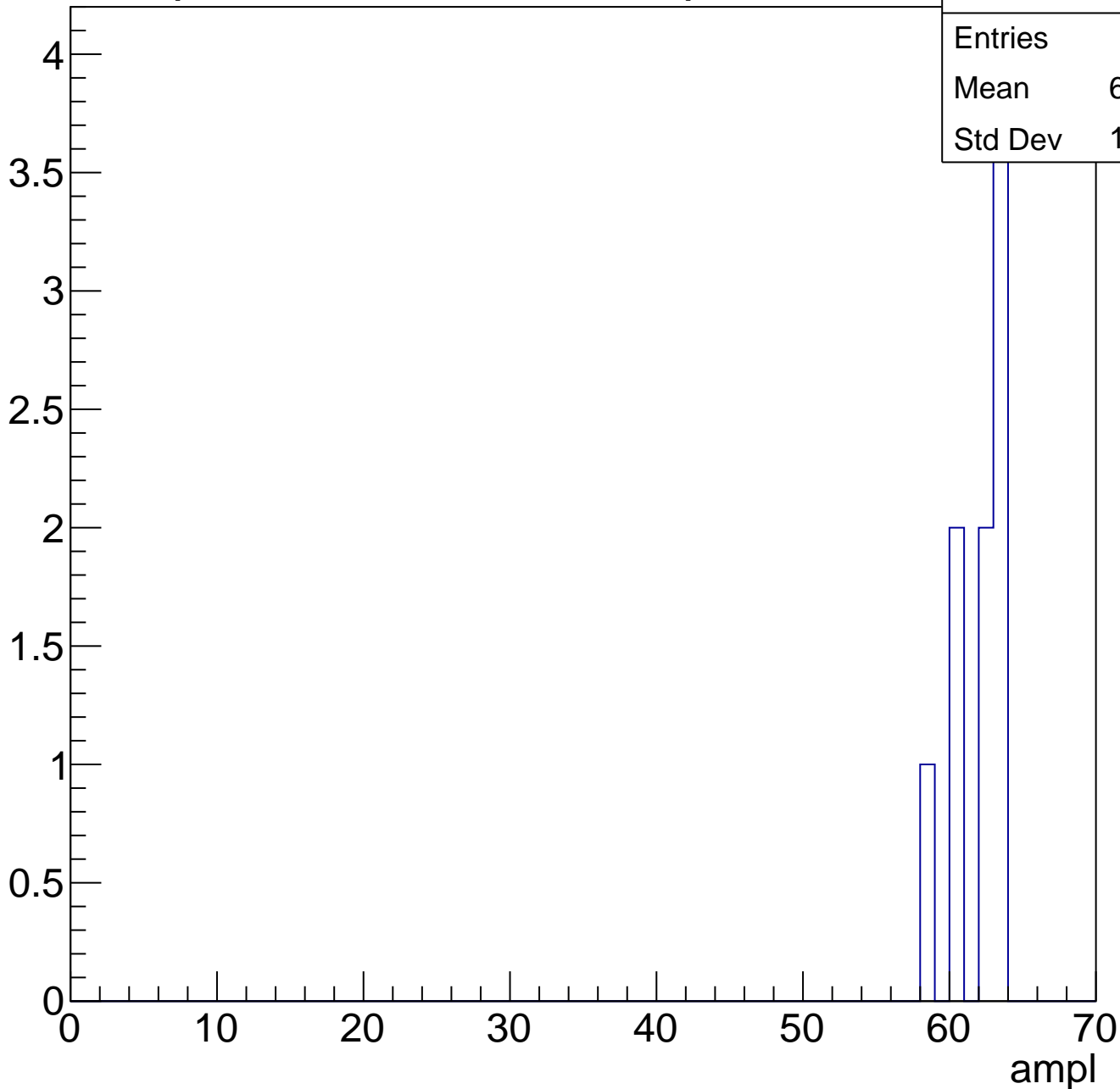
Entry



# B1L103S, U3-ch3, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

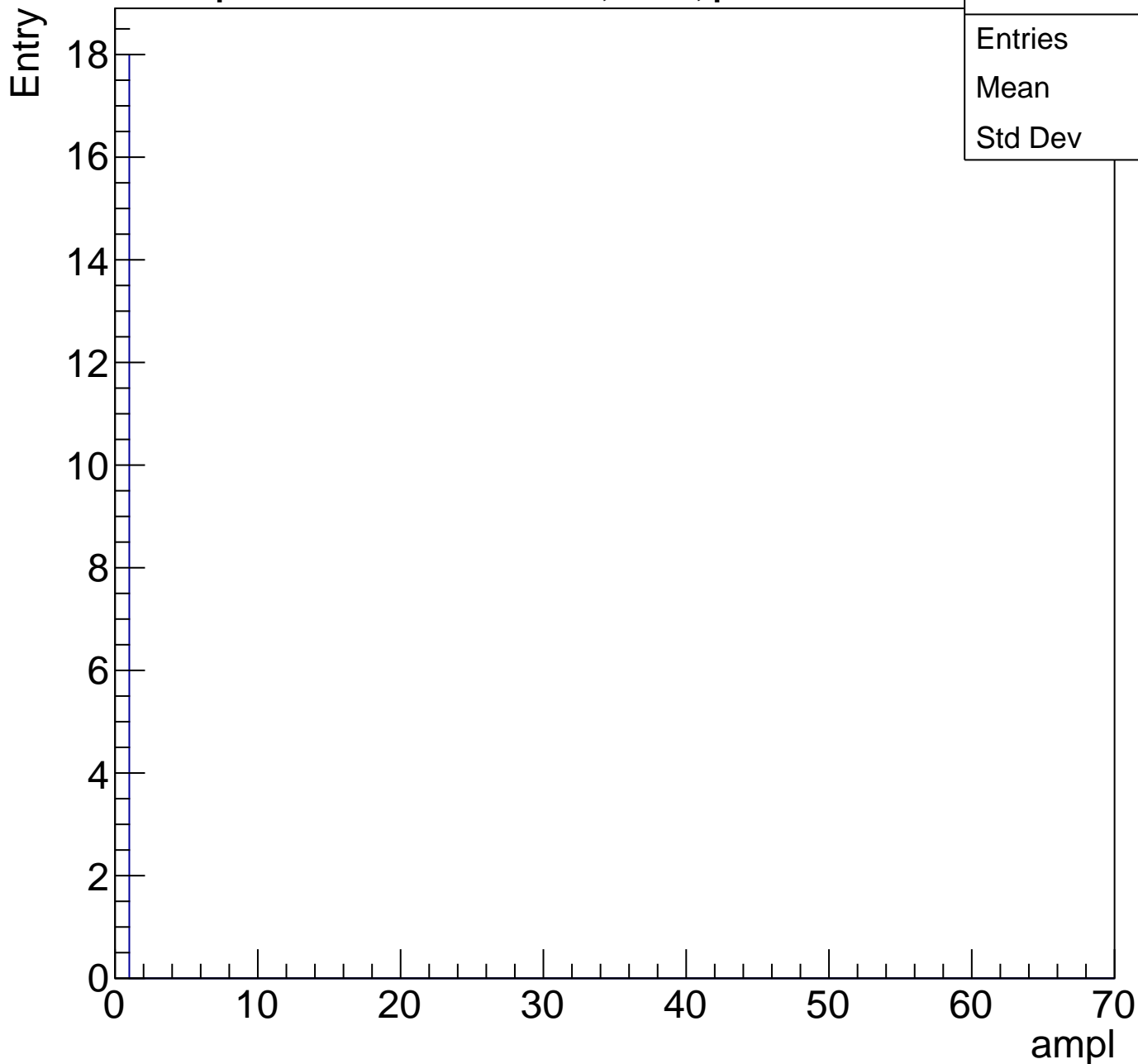




# B1L103S, U3-ch3, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	18
Mean	0
Std Dev	0



# B1L103S, U3-ch4, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	66
Mean	22.45
Std Dev	10.44

**Gaus mean : 27.5574**

**Gaus Width: 3.8130**

Entry

10

8

6

4

2

0

0

10

20

30

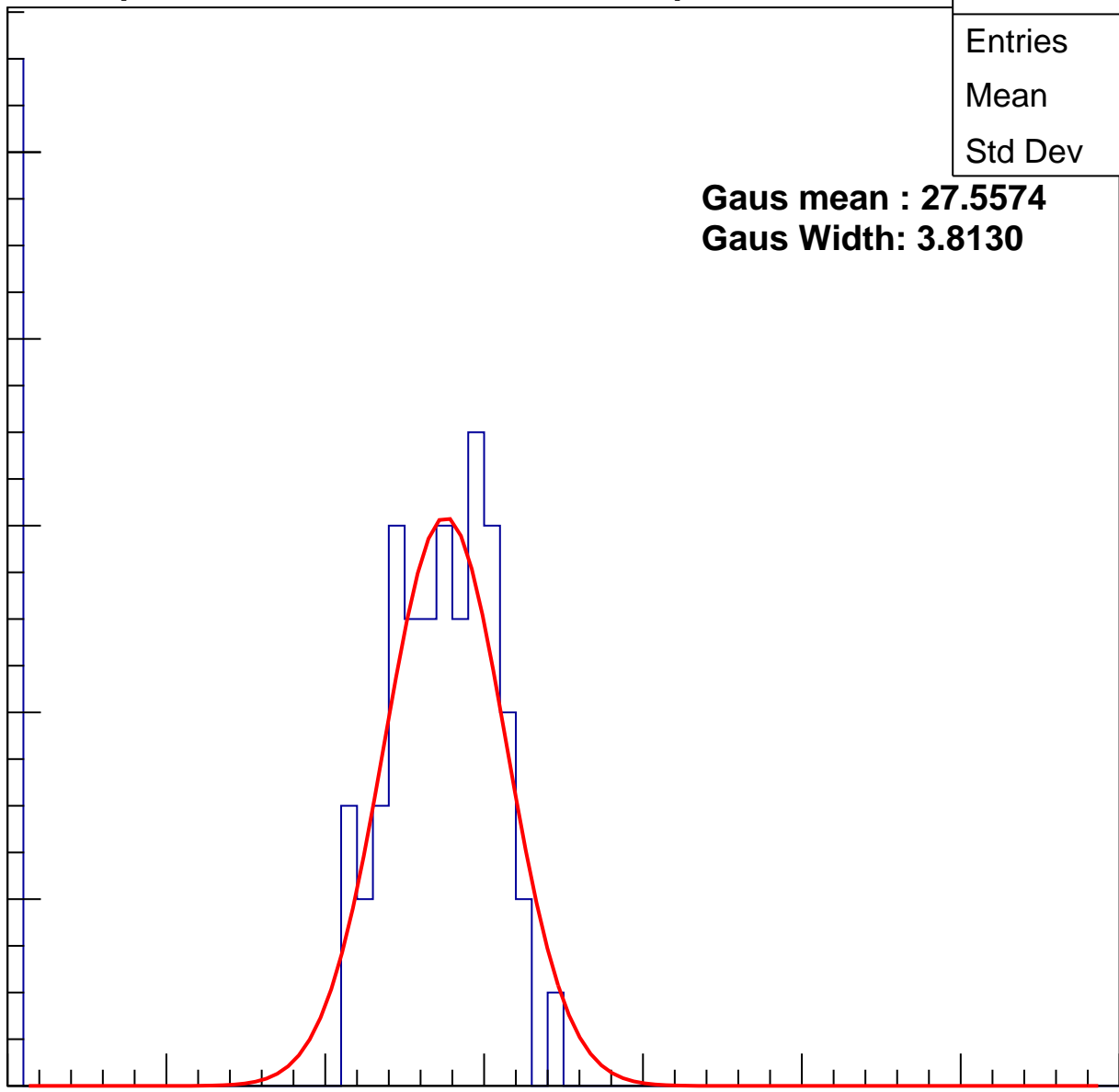
40

50

60

70

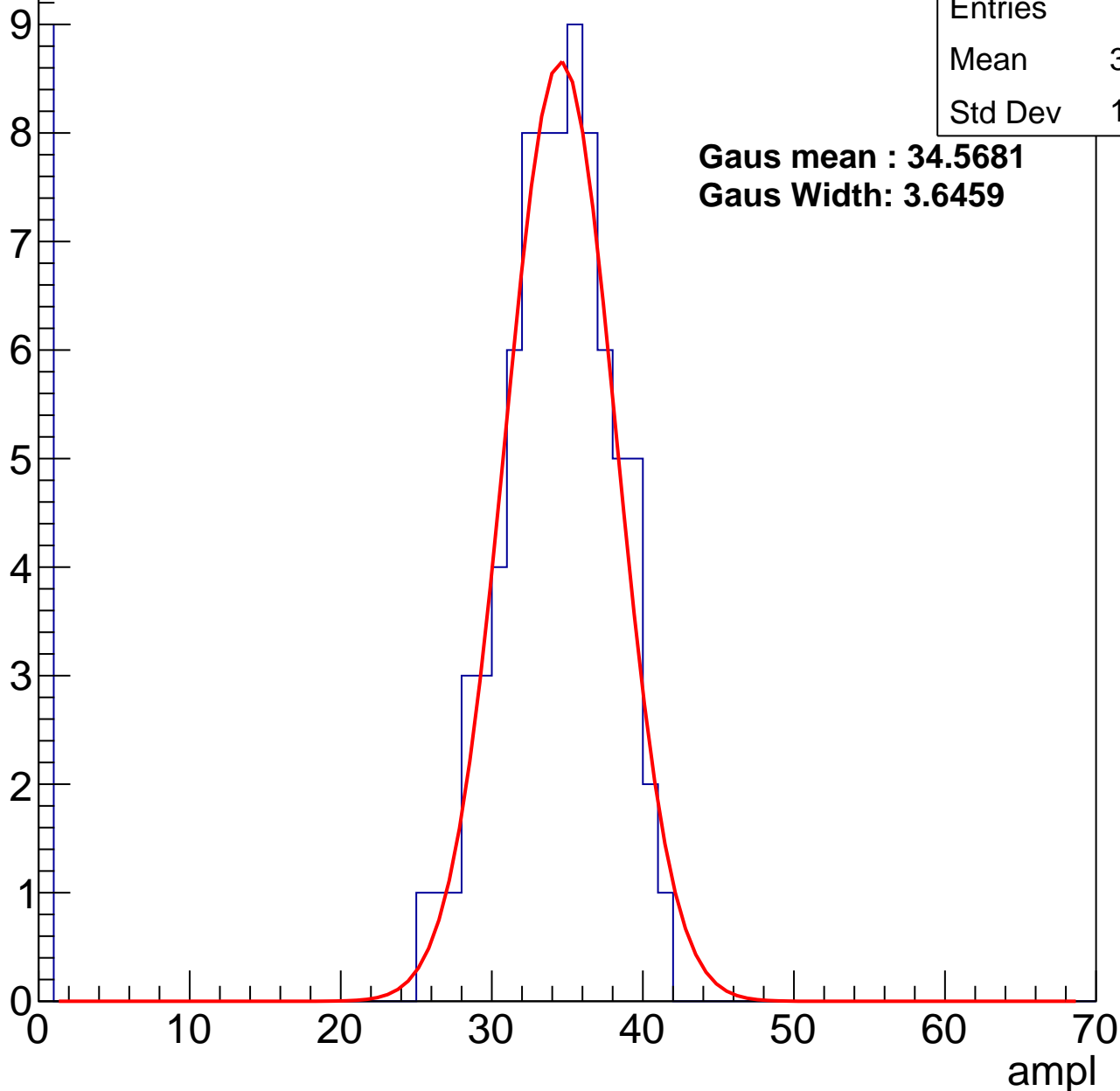
ampl



# B1L103S, U3-ch4, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U3-ch4, adc2

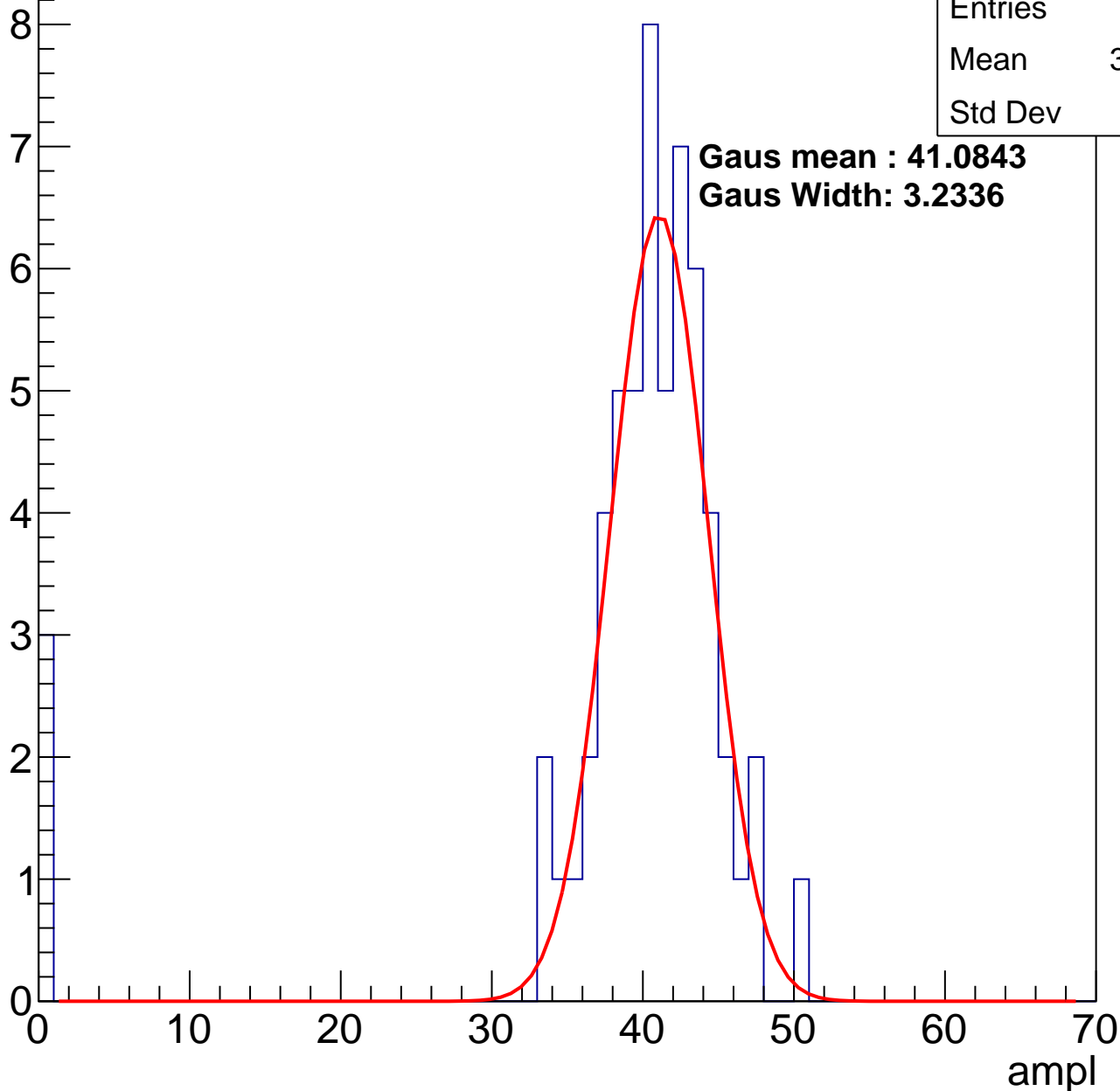
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	38.53
Std Dev	9.53

**Gaus mean : 41.0843**

**Gaus Width: 3.2336**

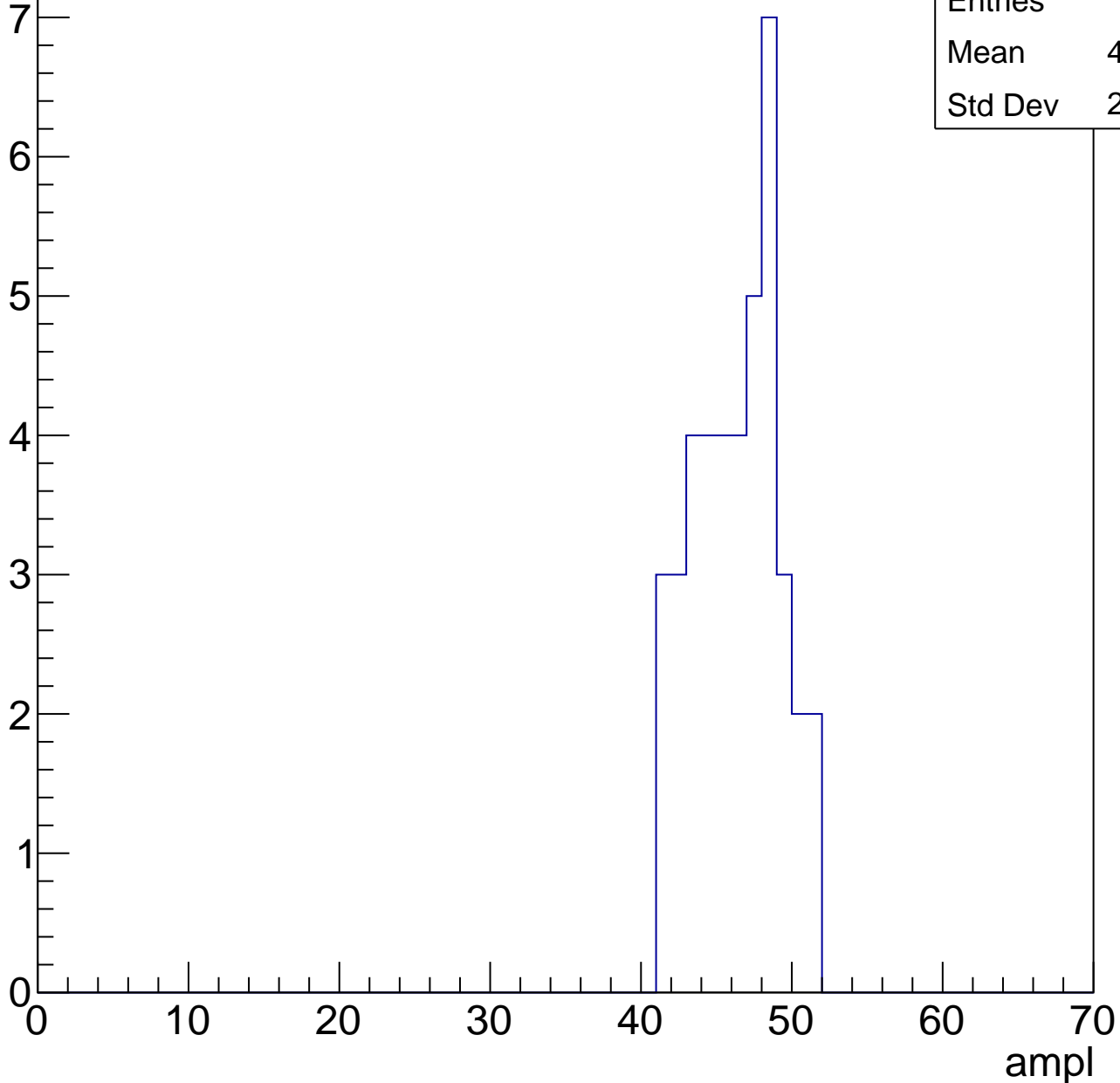


# B1L103S, U3-ch4, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	41
Mean	45.88
Std Dev	2.795

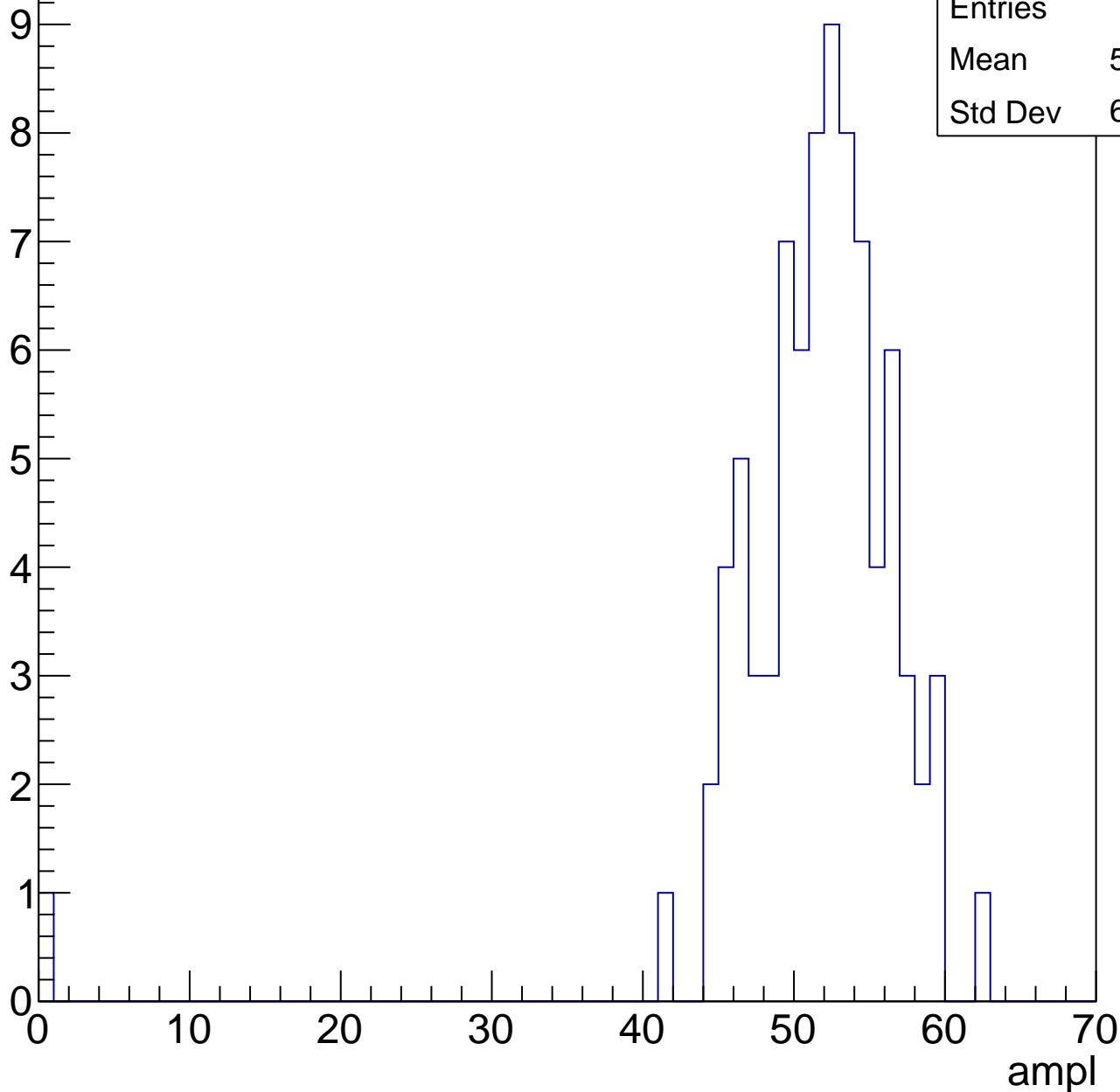


# B1L103S, U3-ch4, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	83
Mean	50.93
Std Dev	6.954

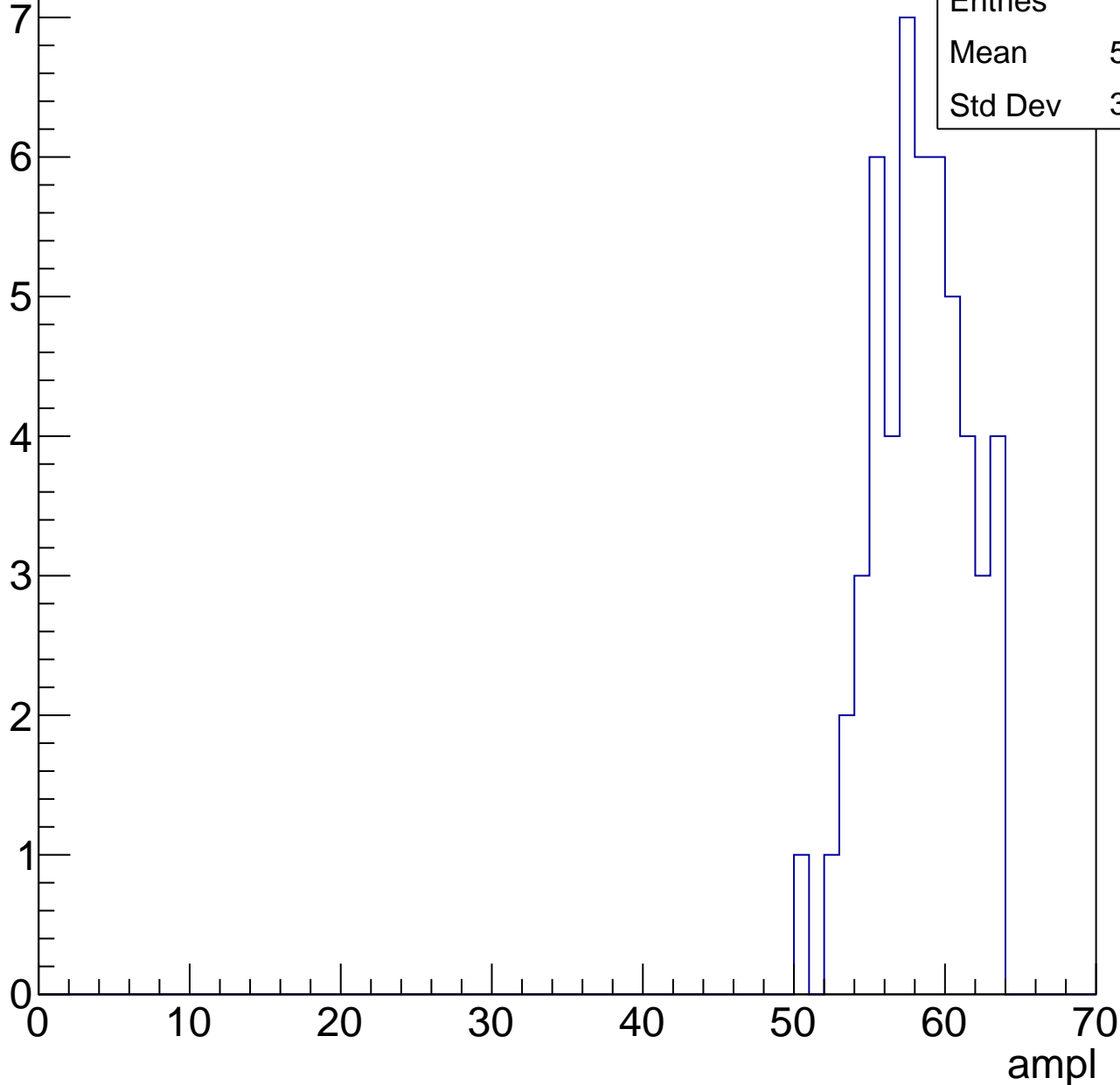


# B1L103S, U3-ch4, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	52
Mean	57.83
Std Dev	3.049

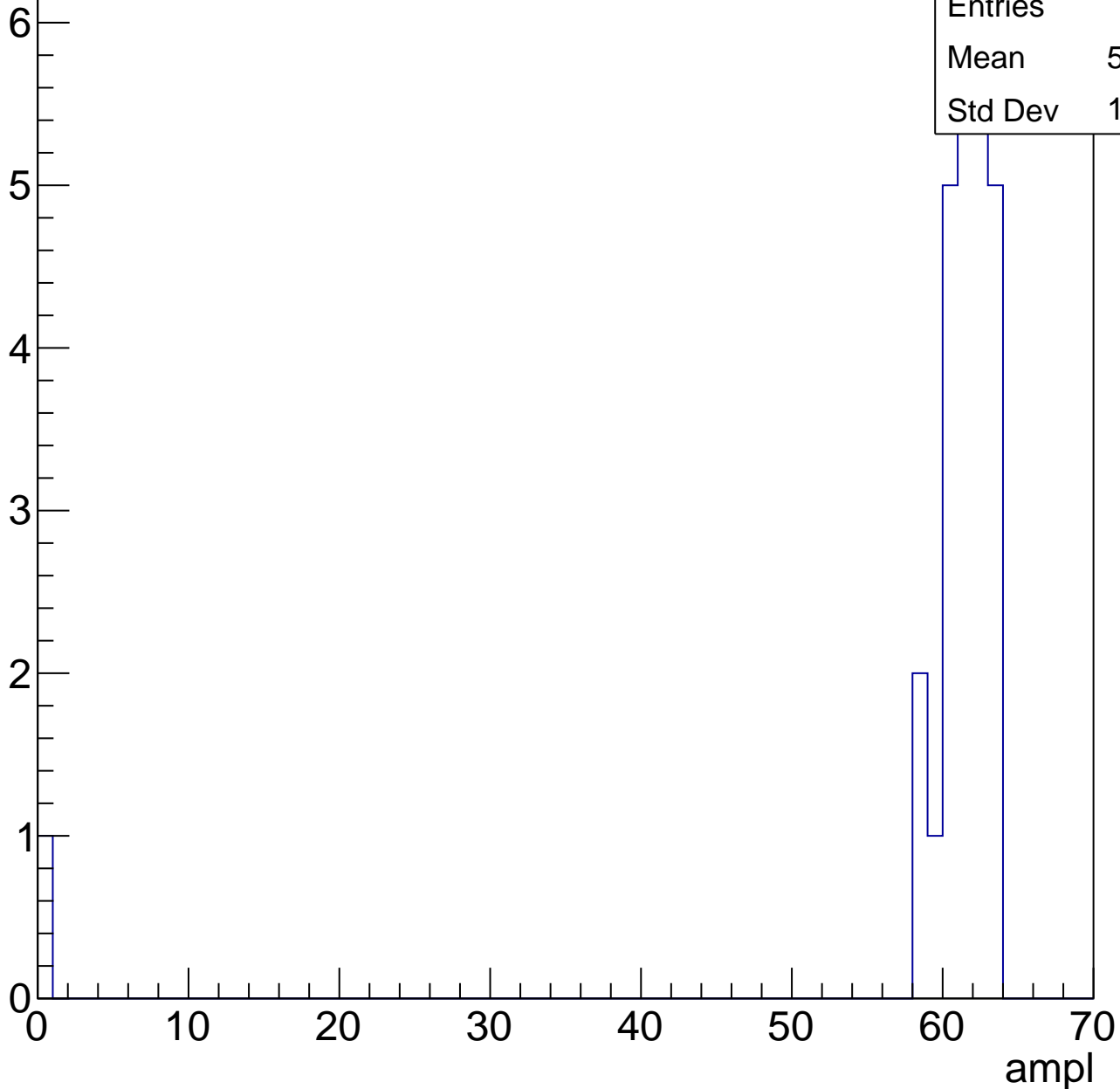


# B1L103S, U3-ch4, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	26
Mean	58.77
Std Dev	11.84

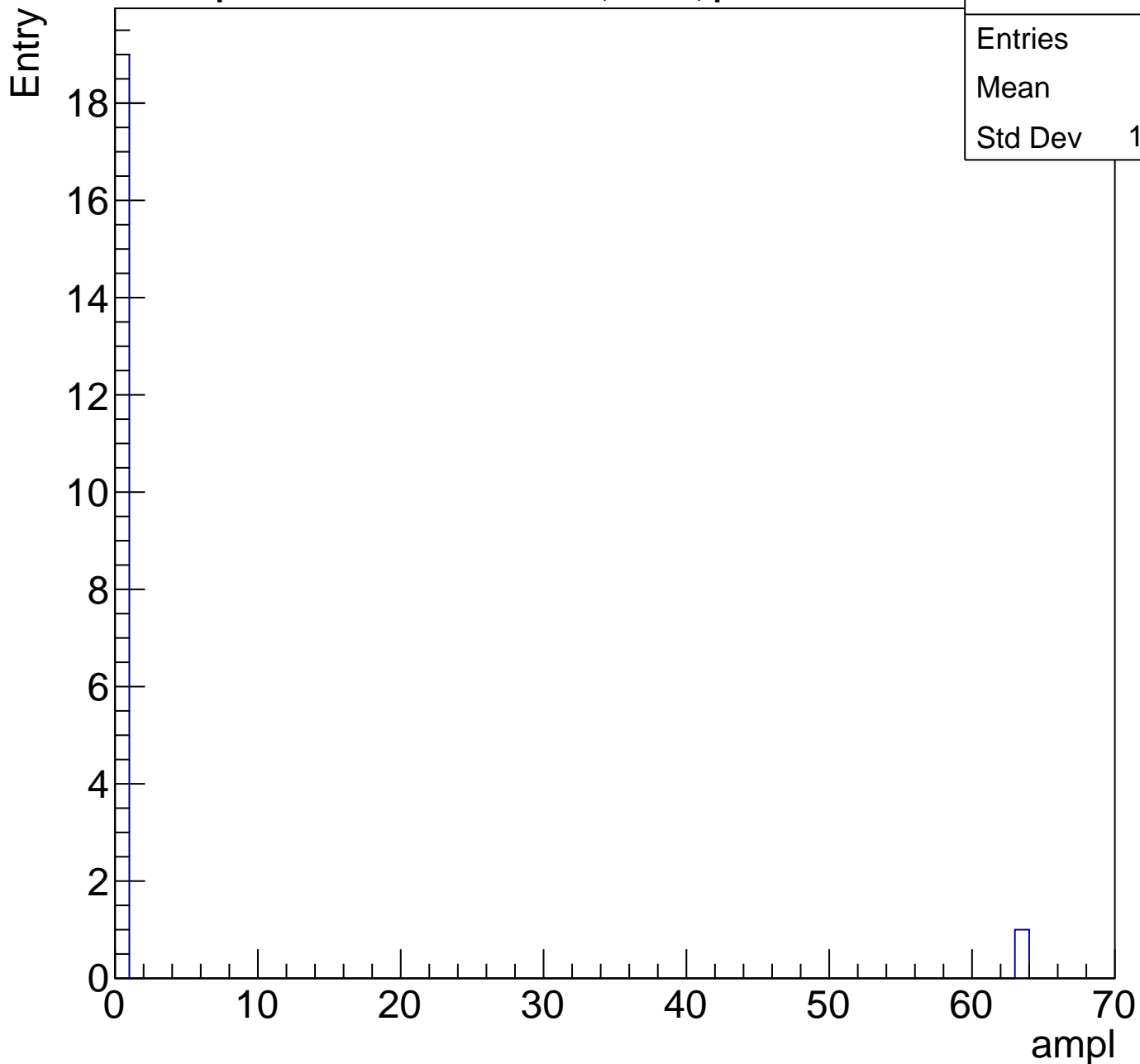




# B1L103S, U3-ch4, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73



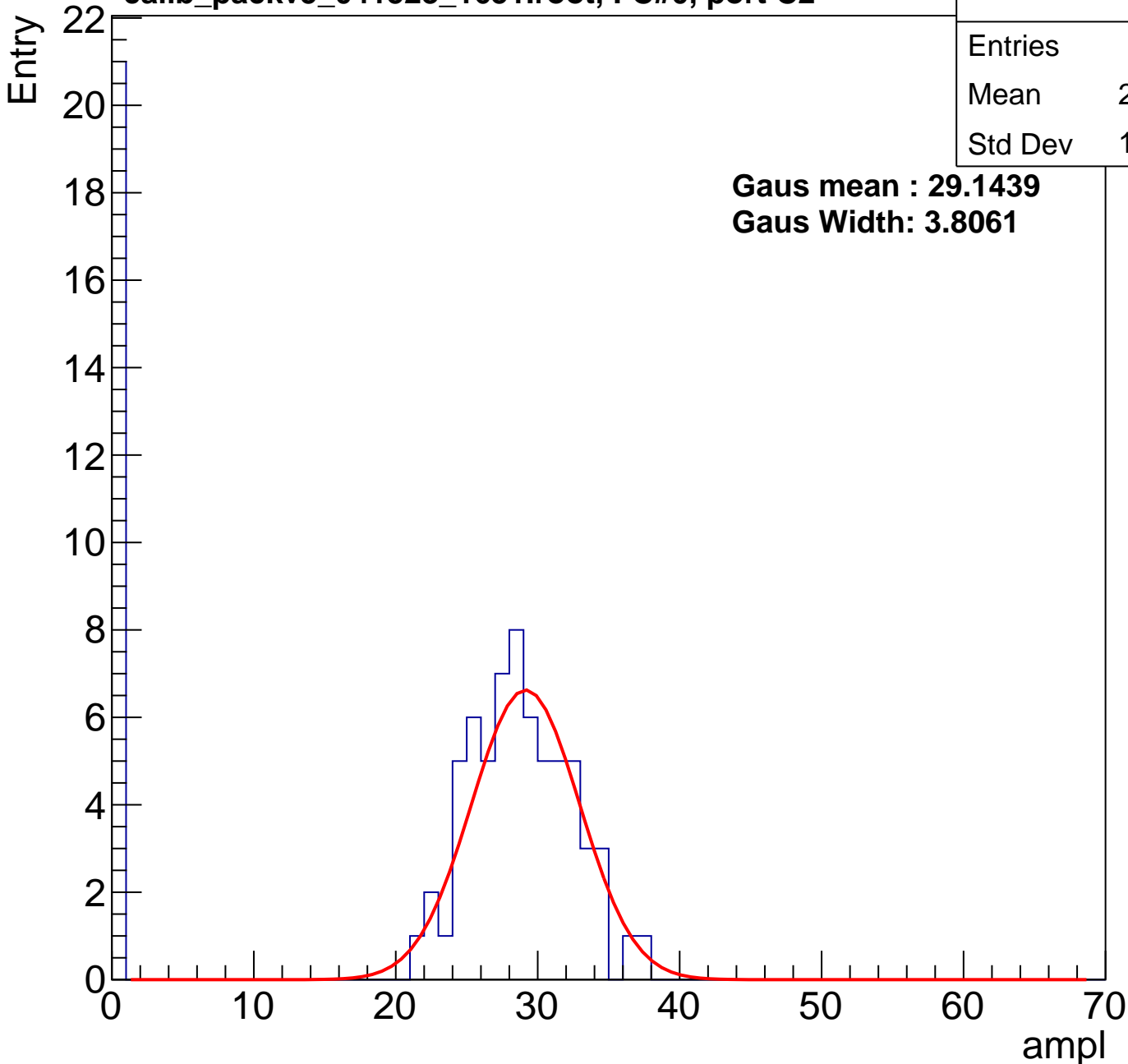
# B1L103S, U3-ch5, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	85
Mean	21.34
Std Dev	12.59

**Gaus mean : 29.1439**

**Gaus Width: 3.8061**



# B1L103S, U3-ch5, adc1

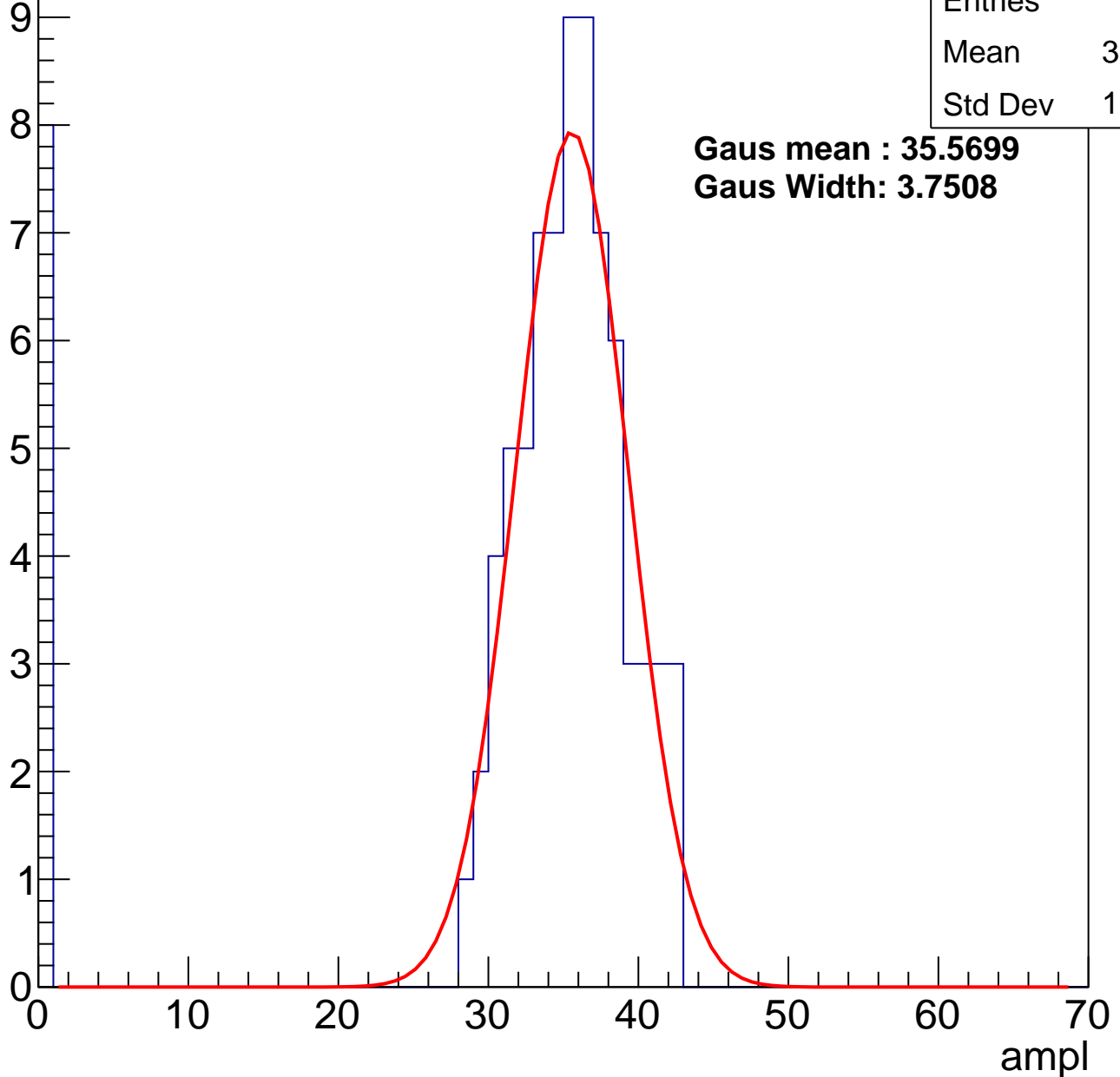
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	82
Mean	31.73
Std Dev	10.92

**Gaus mean : 35.5699**

**Gaus Width: 3.7508**



# B1L103S, U3-ch5, adc2

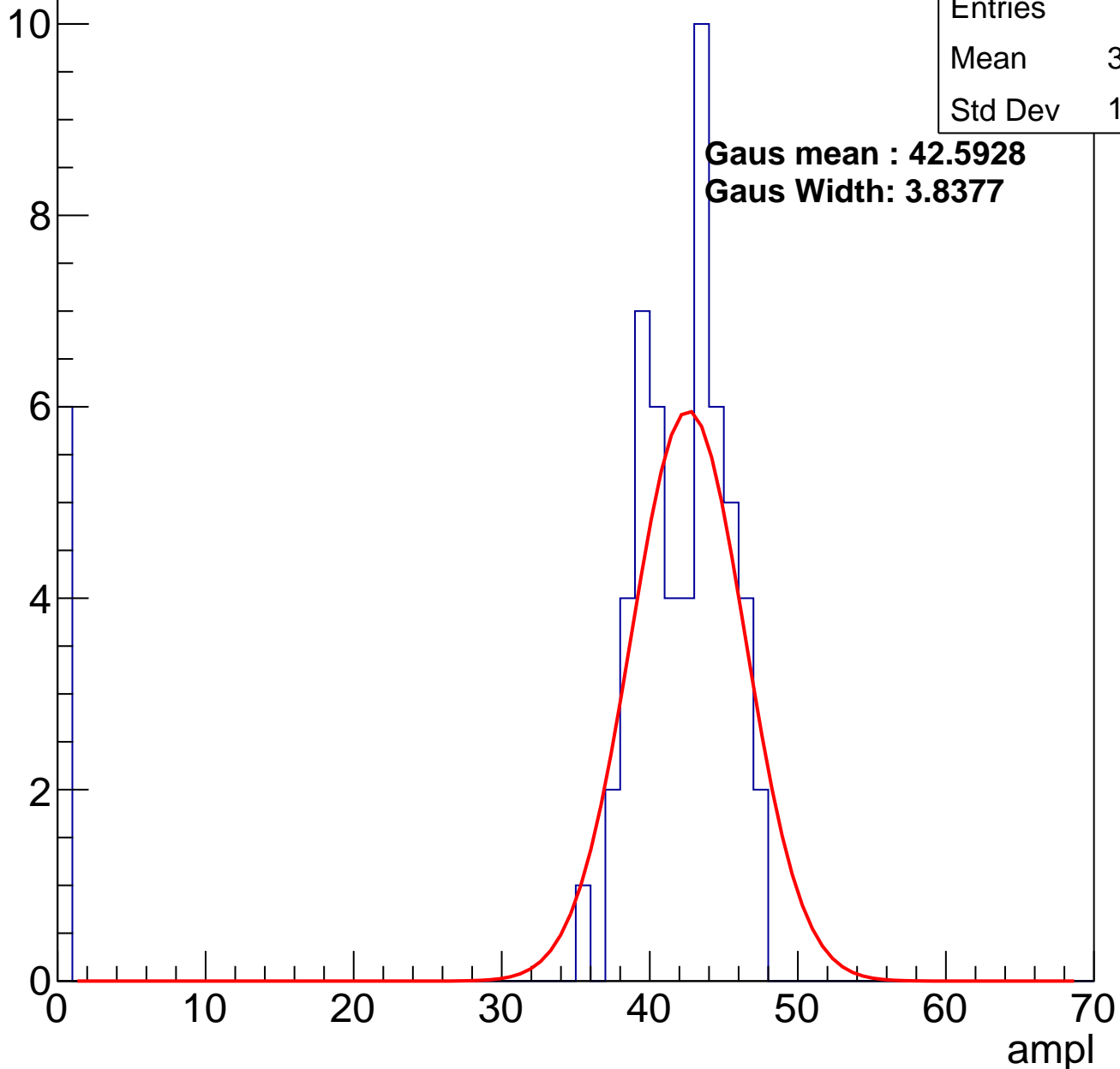
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	61
Mean	37.75
Std Dev	12.76

**Gaus mean : 42.5928**

**Gaus Width: 3.8377**

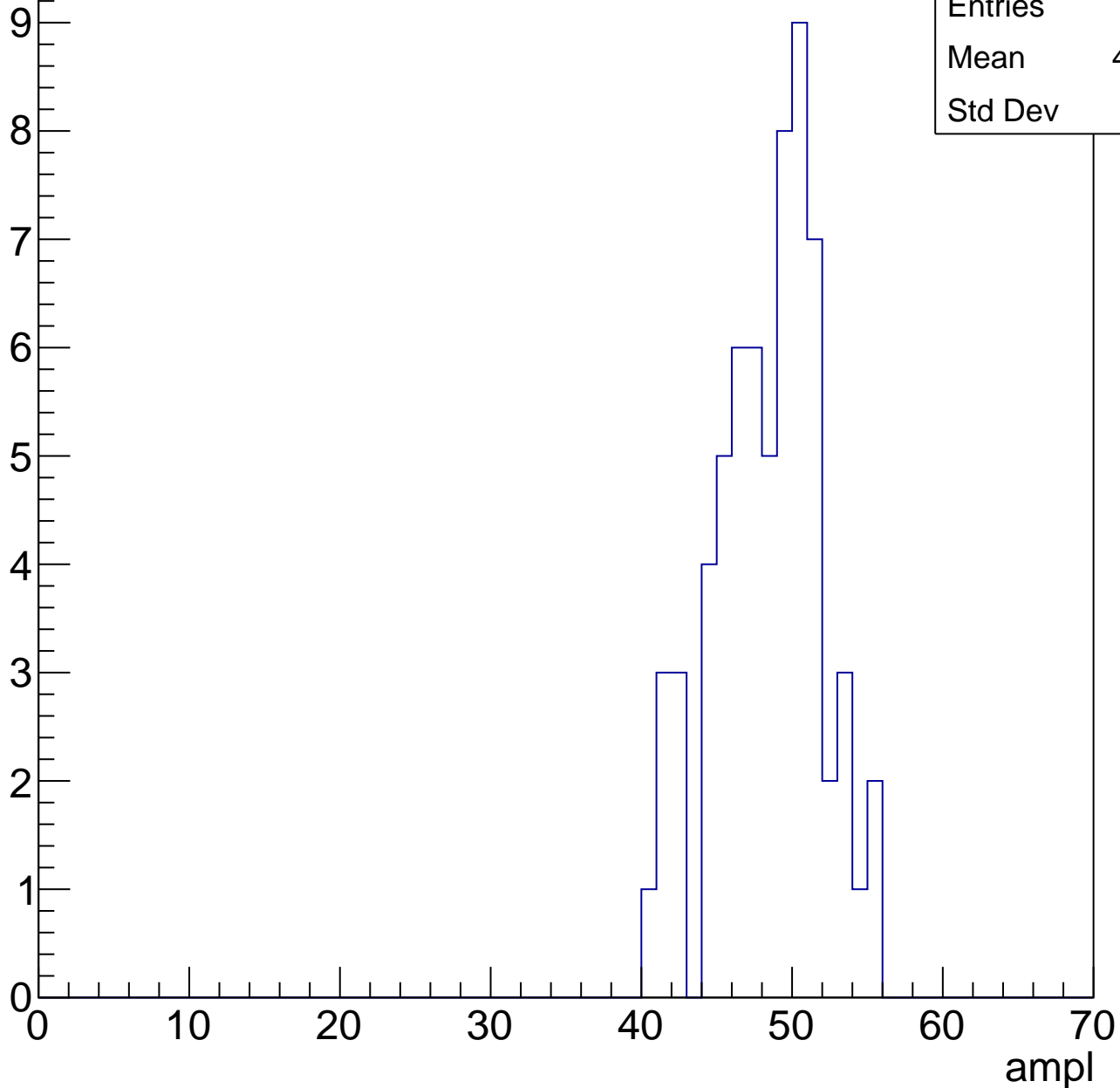
Entry



# B1L103S, U3-ch5, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

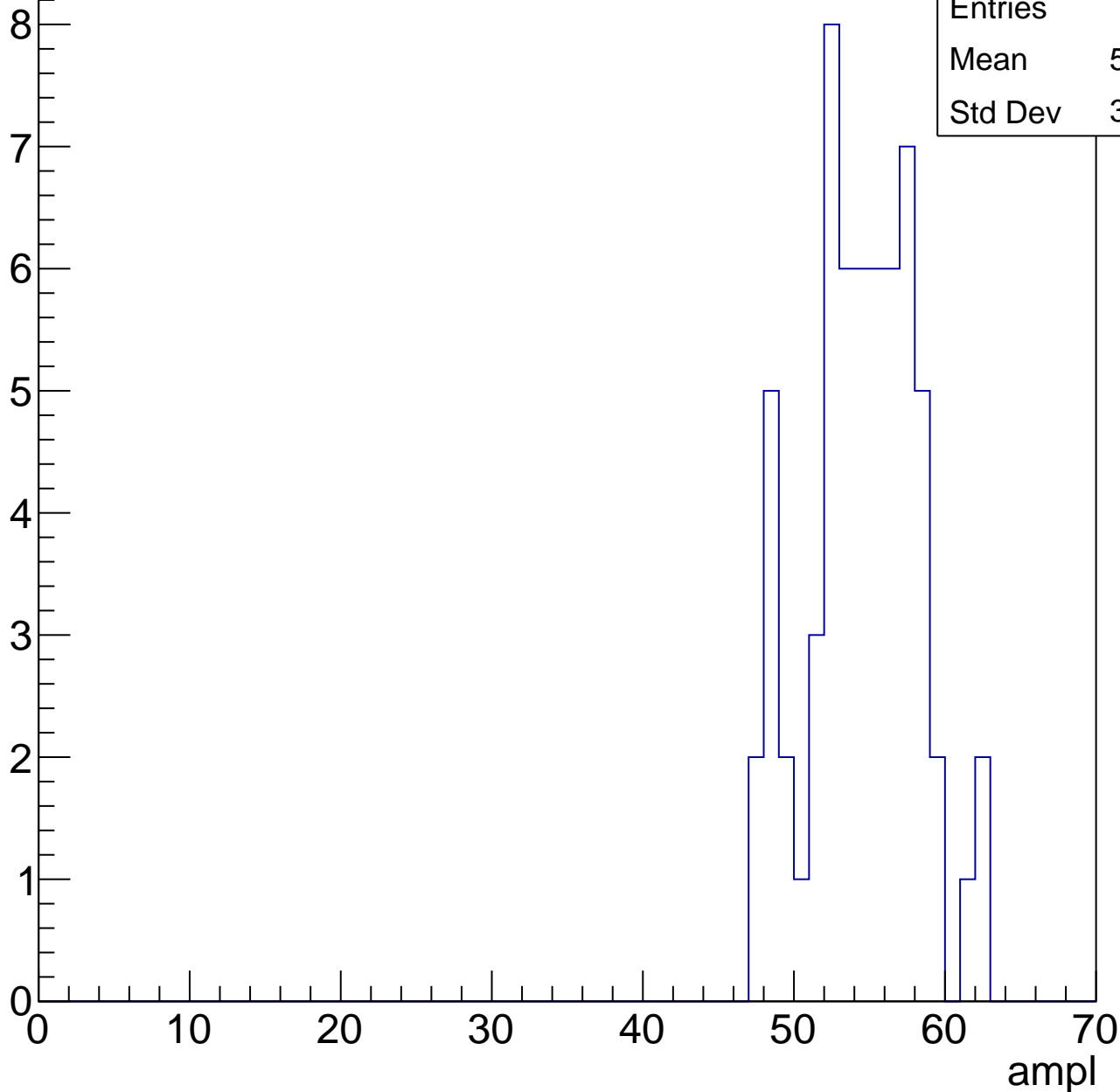


# B1L103S, U3-ch5, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	54.05
Std Dev	3.612



# B1L103S, U3-ch5, adc5

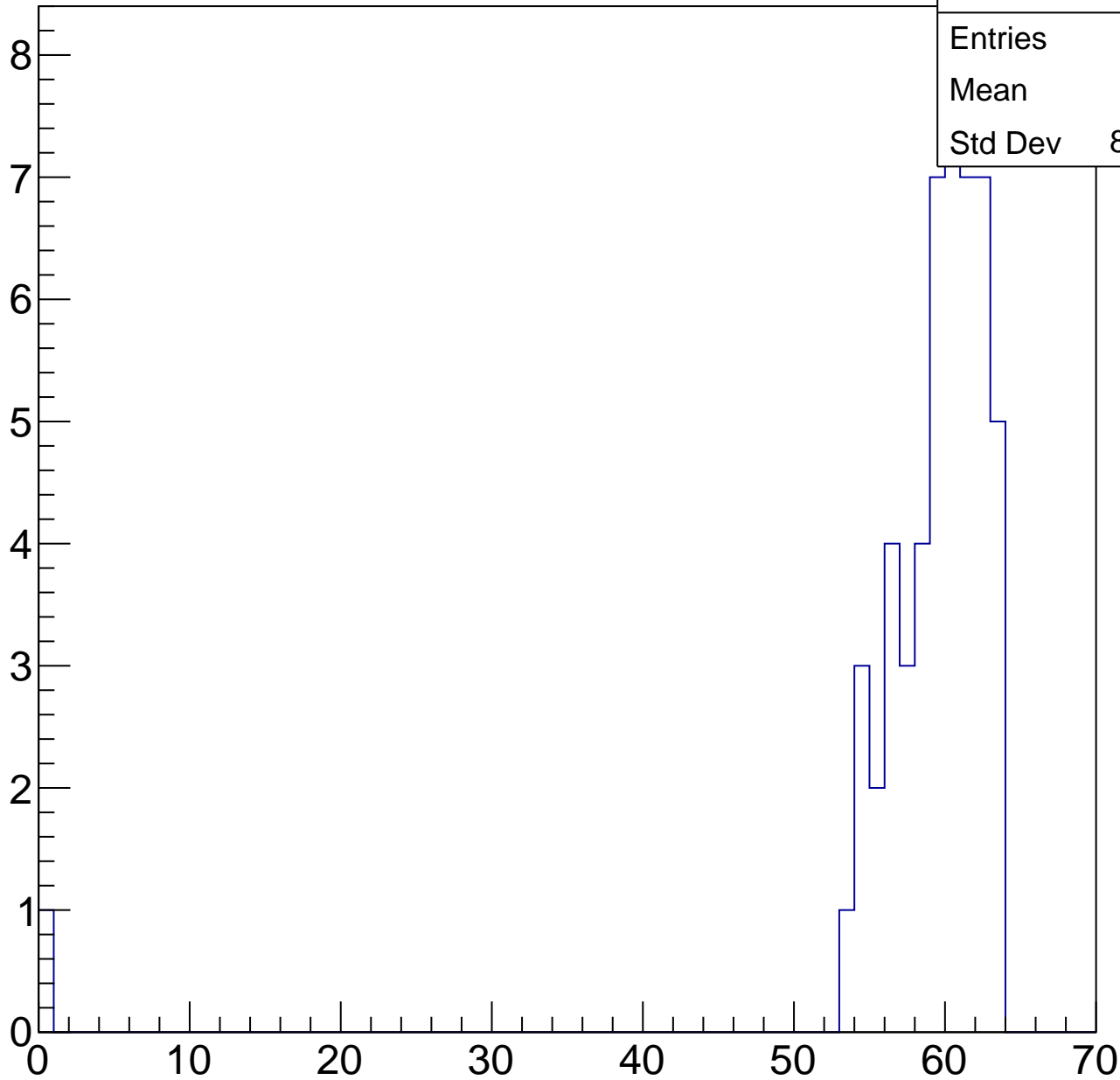
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	52
Mean	58.1
Std Dev	8.563

ampl

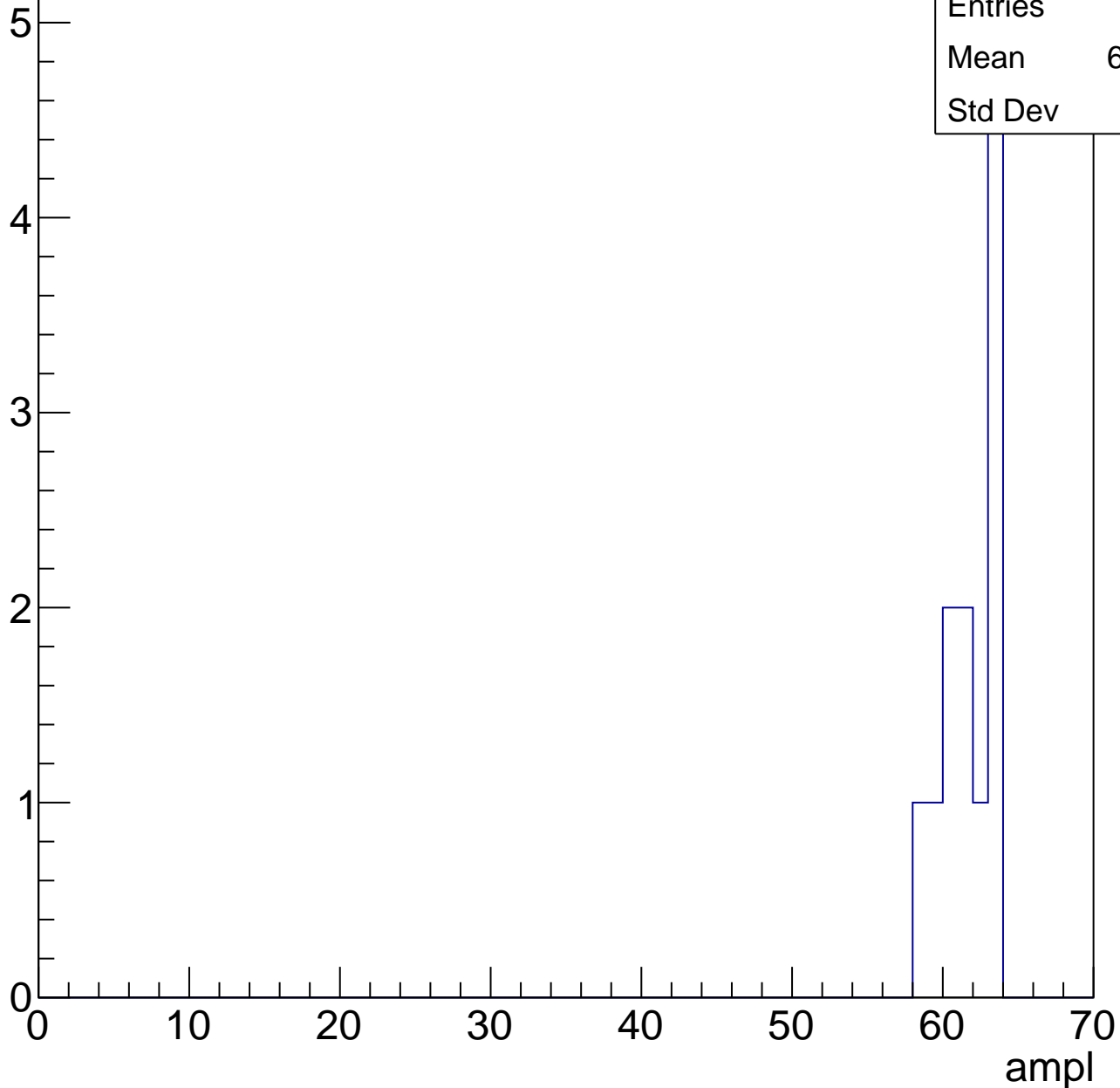


# B1L103S, U3-ch5, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	12
Mean	61.33
Std Dev	1.7

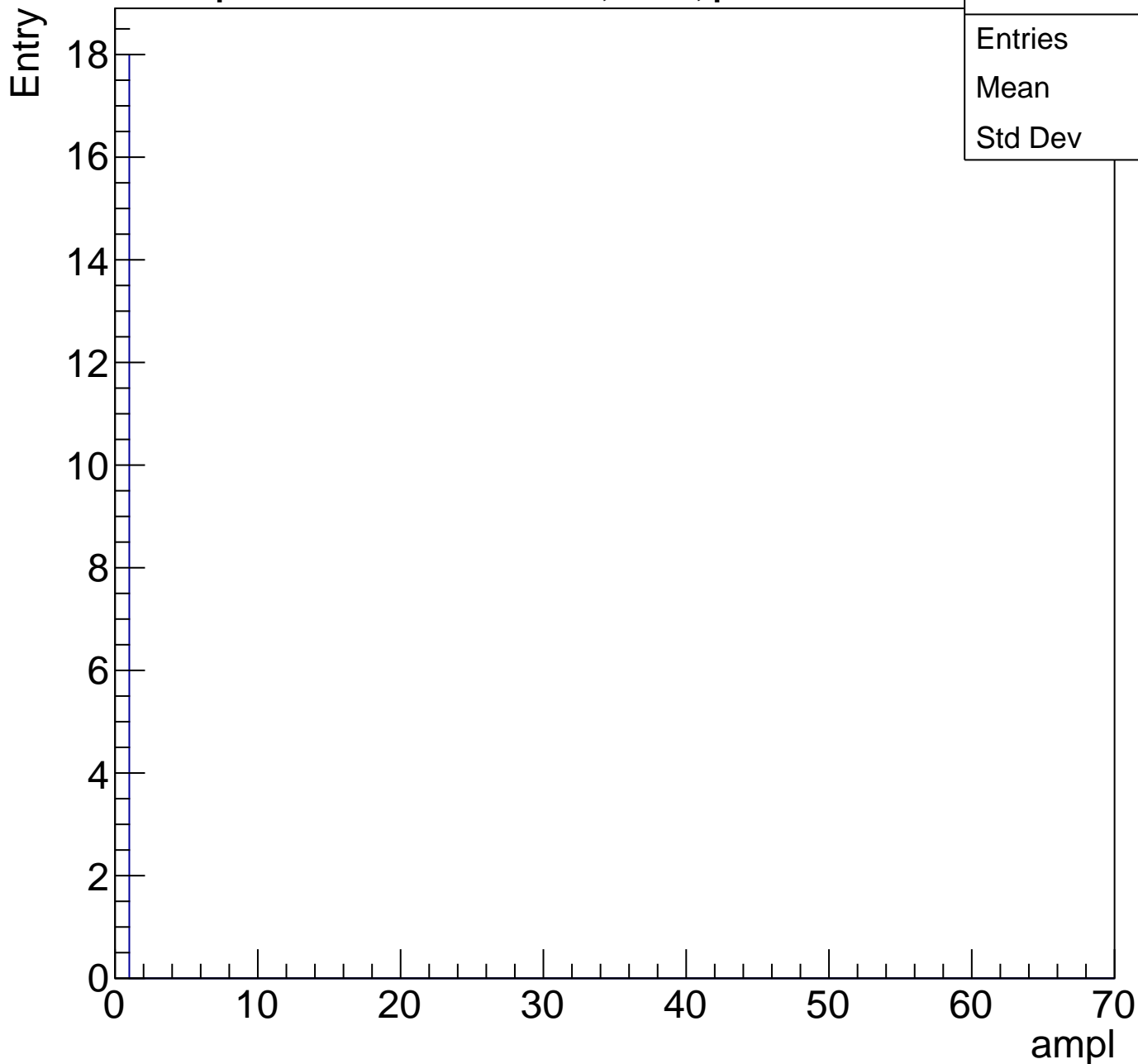




# B1L103S, U3-ch5, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	18
Mean	0
Std Dev	0



# B1L103S, U3-ch6, adc0

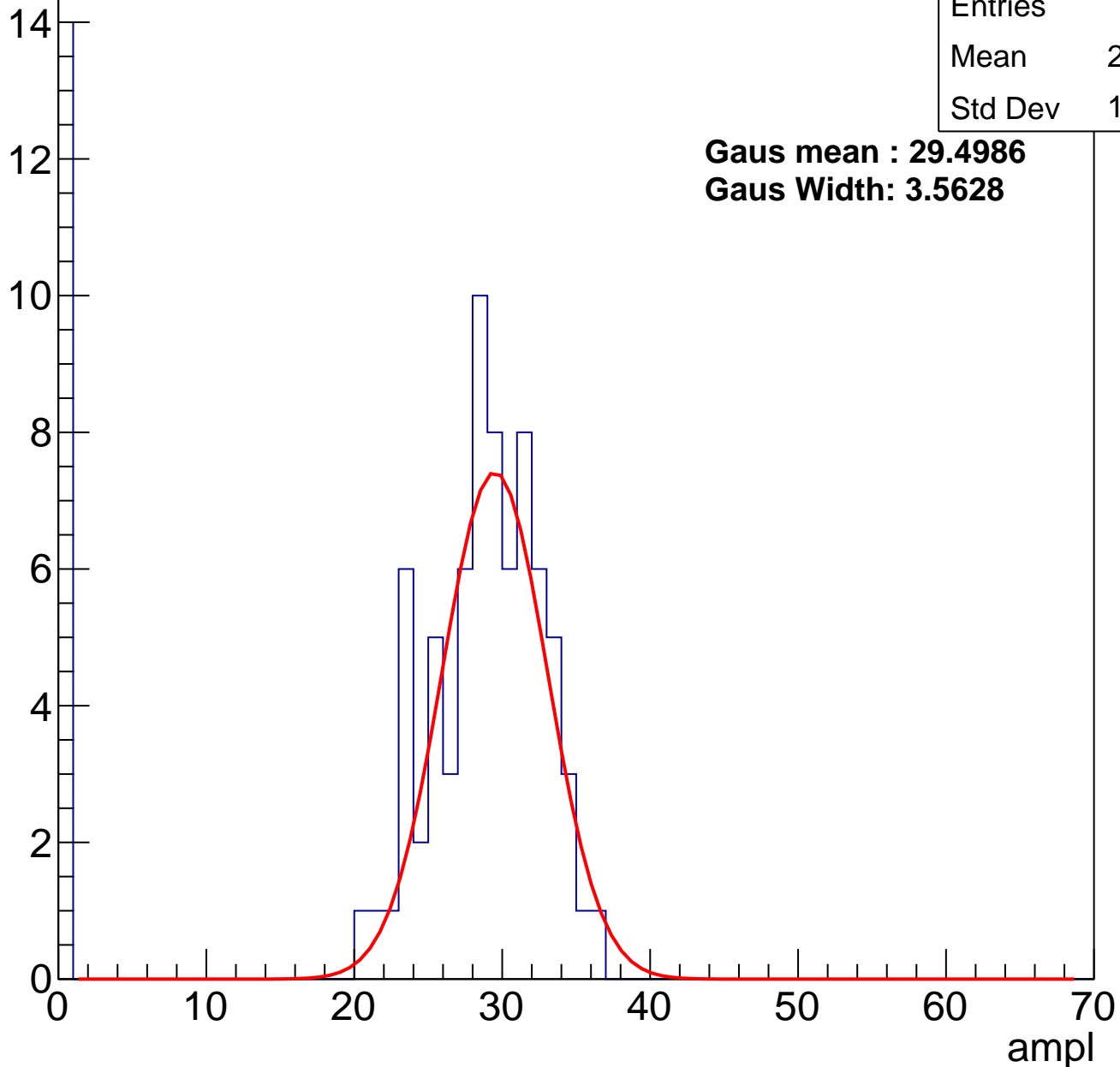
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	87
Mean	23.95
Std Dev	10.98

**Gaus mean : 29.4986**

**Gaus Width: 3.5628**

Entry



# B1L103S, U3-ch6, adc1

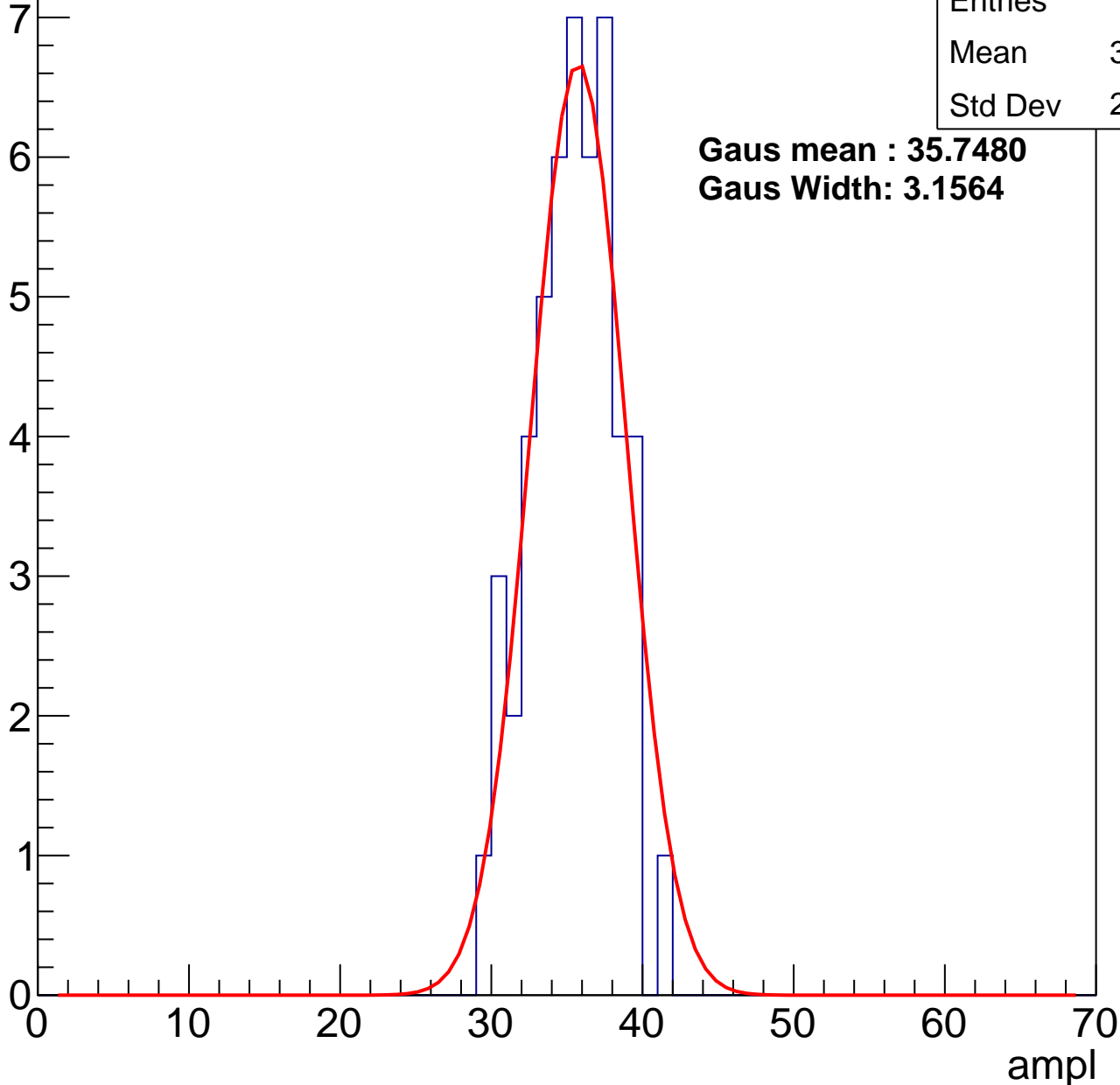
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	50
Mean	34.94
Std Dev	2.738

**Gaus mean : 35.7480**

**Gaus Width: 3.1564**



# B1L103S, U3-ch6, adc2

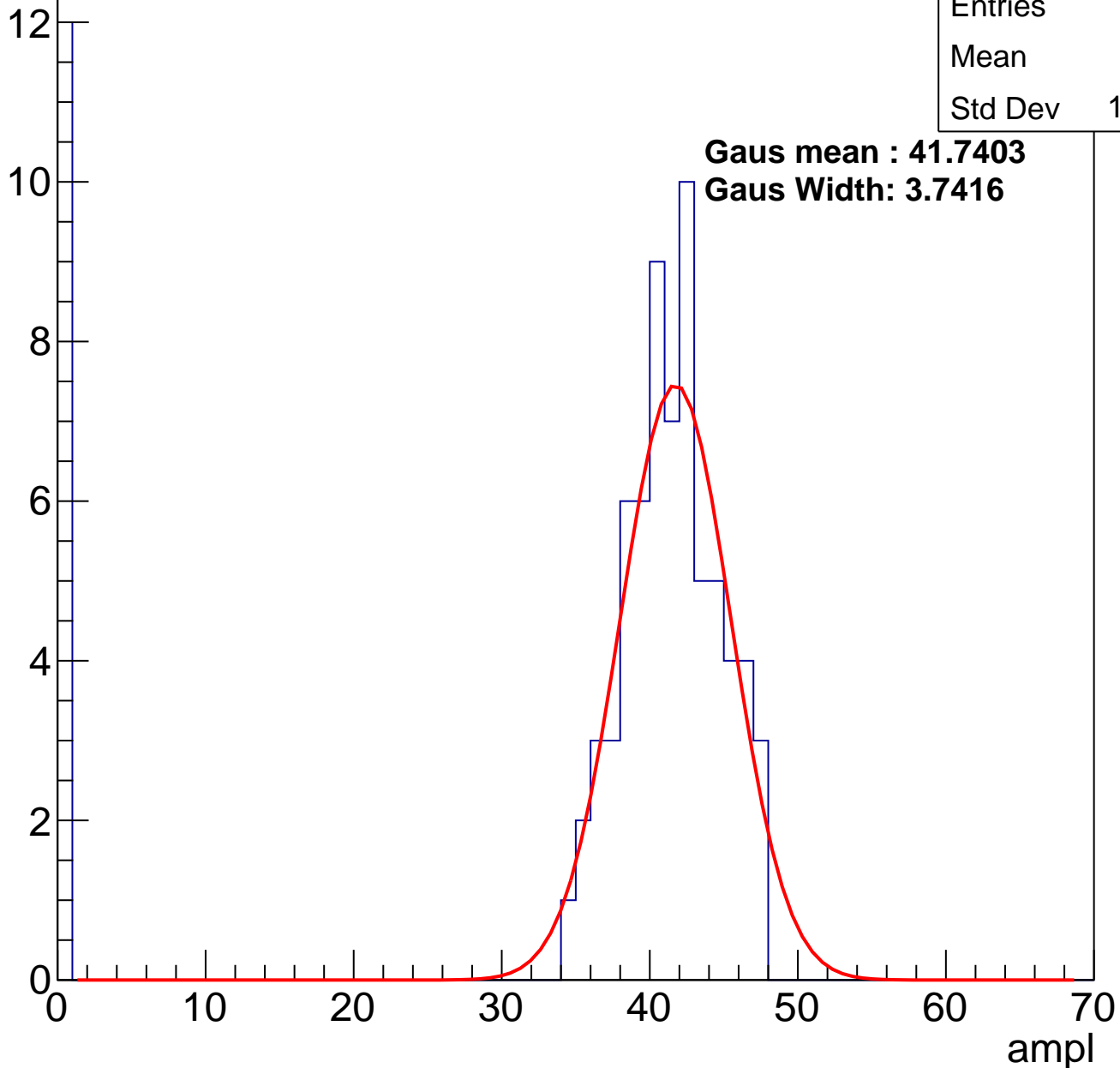
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	80
Mean	34.9
Std Dev	14.95

**Gaus mean : 41.7403**

**Gaus Width: 3.7416**

Entry



# B1L103S, U3-ch6, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

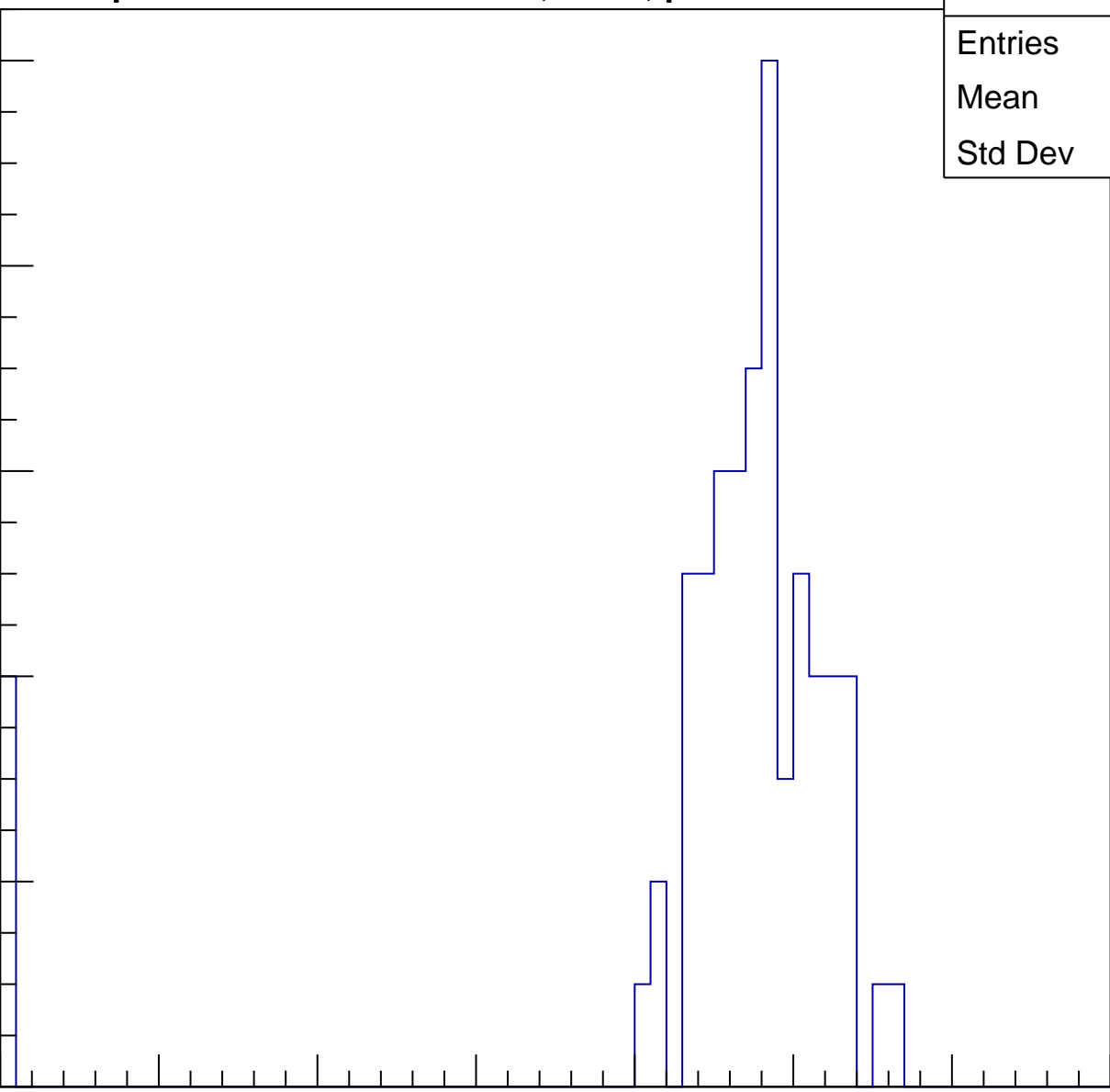
Entries	68
Mean	44.76
Std Dev	11.69

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U3-ch6, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

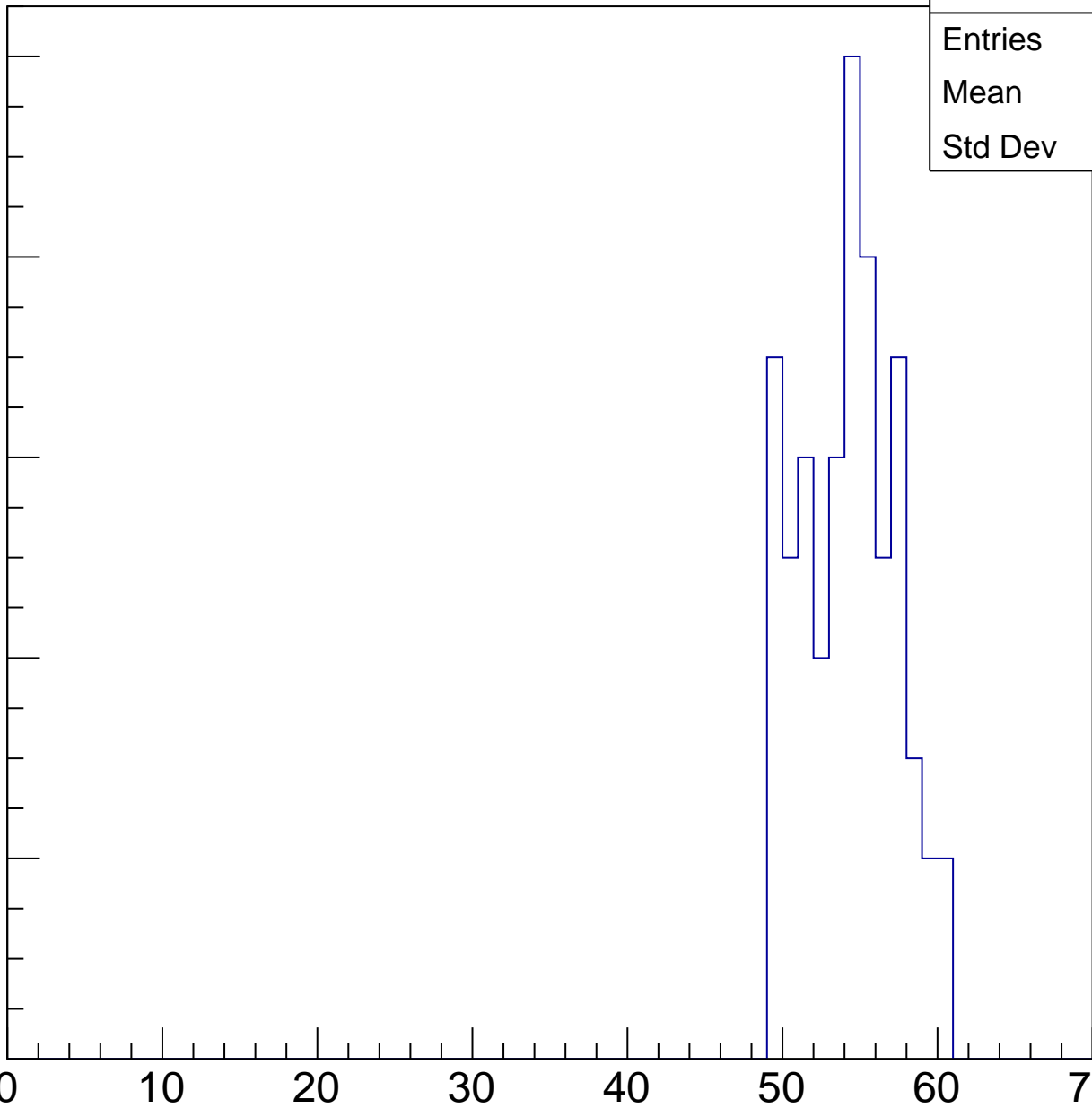
Entries	65
Mean	53.78
Std Dev	3.01

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U3-ch6, adc5

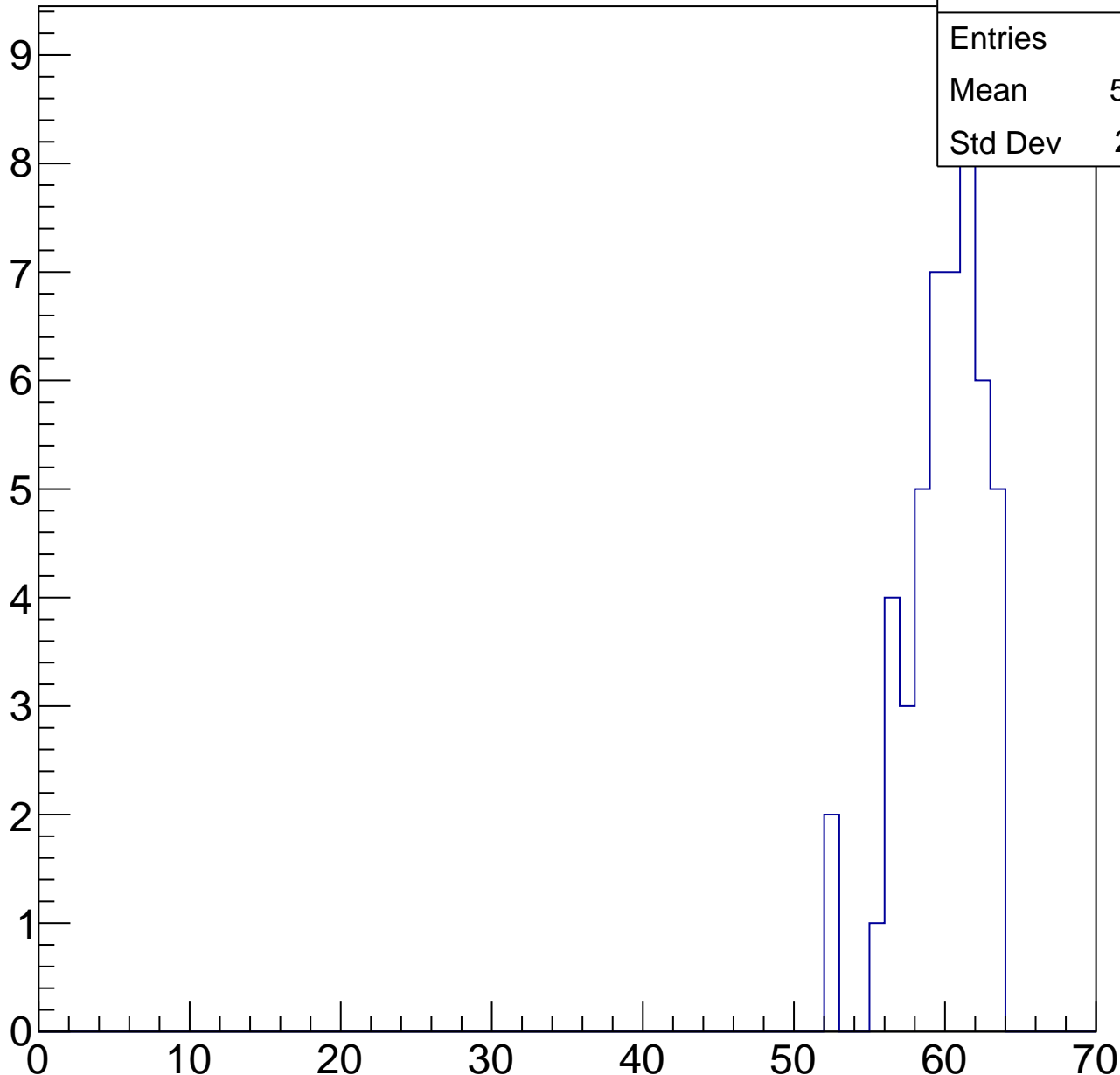
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	59.45
Std Dev	2.611

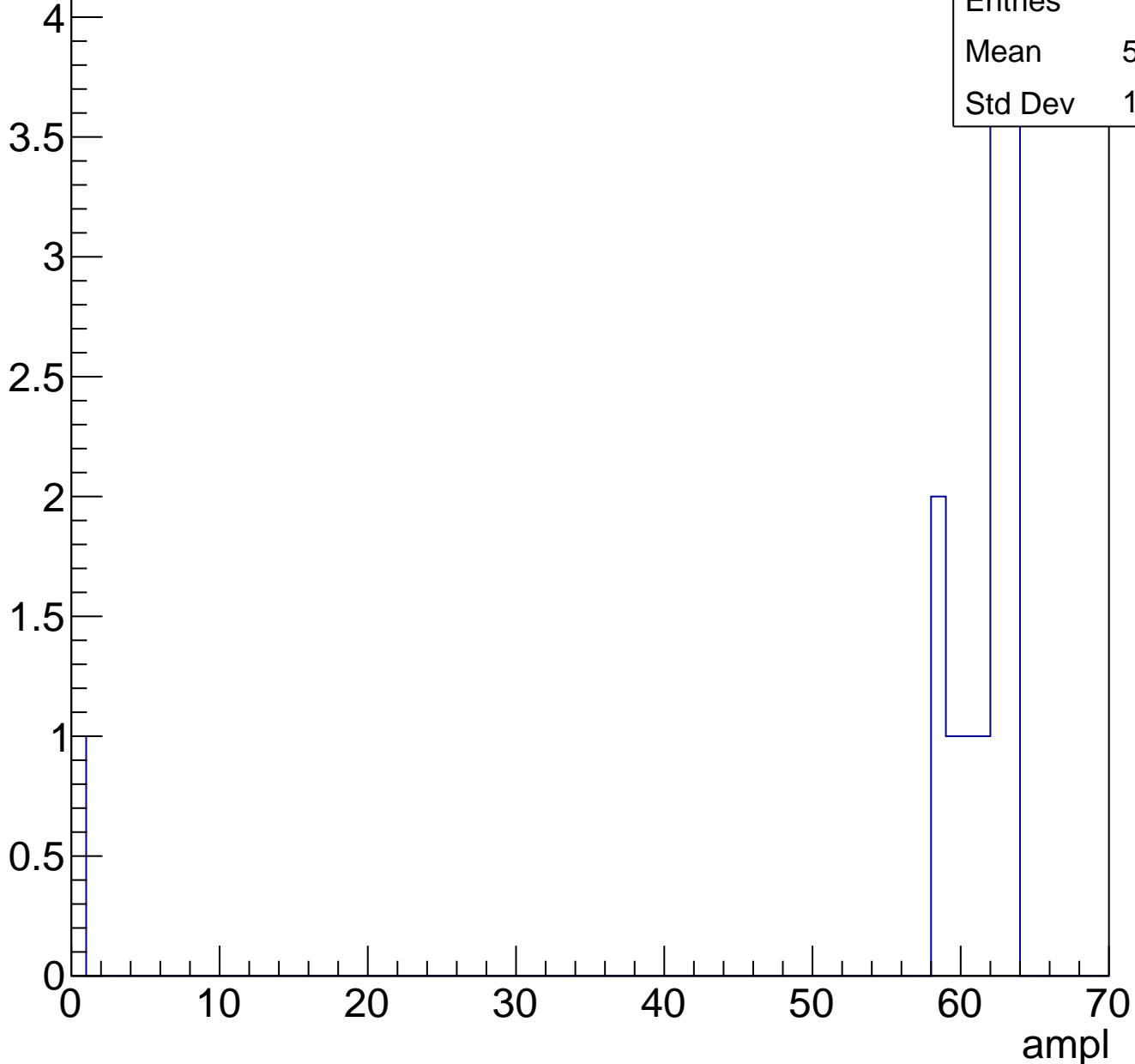
ampl



# B1L103S, U3-ch6, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



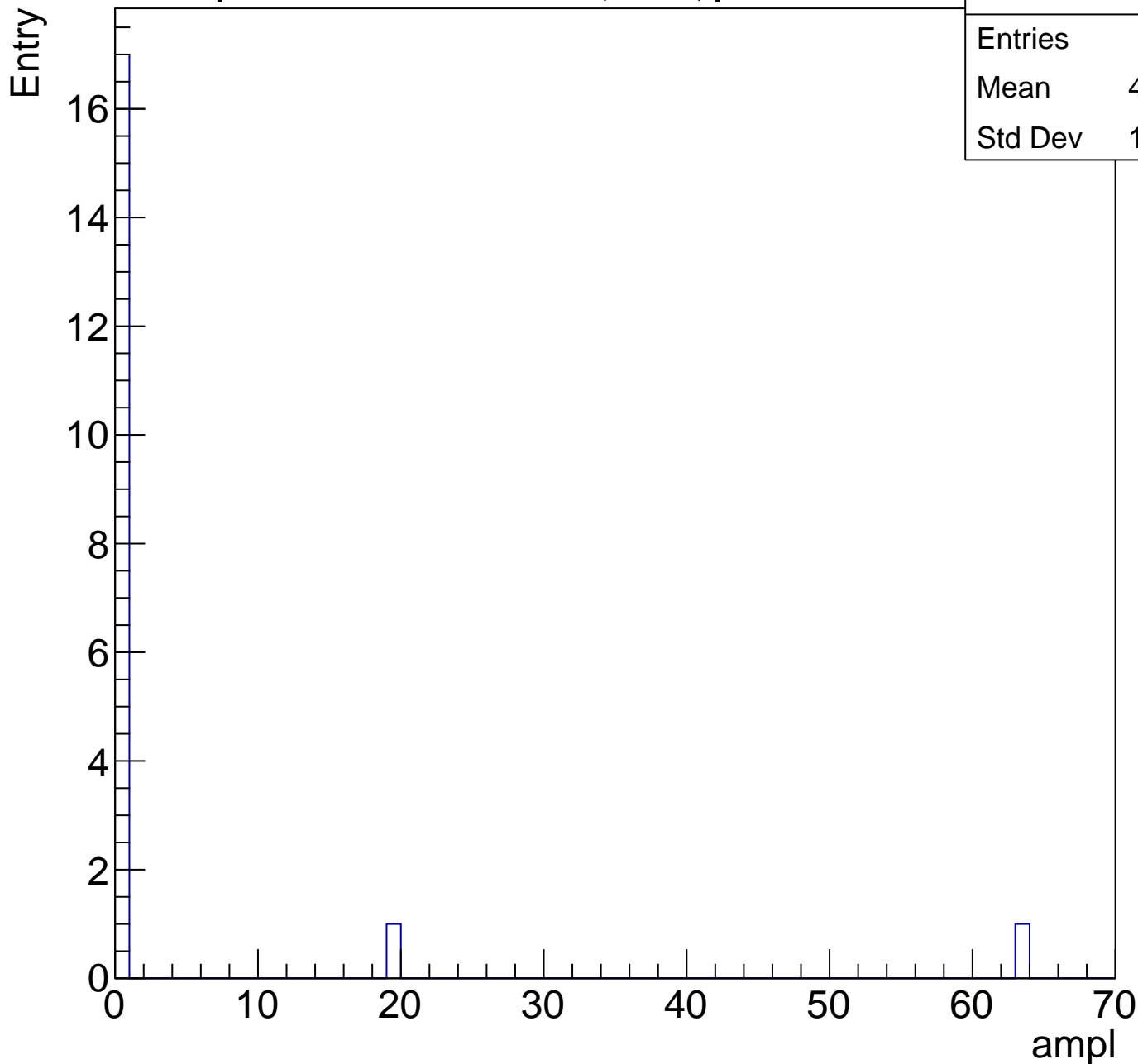
Entries	14
Mean	56.86
Std Dev	15.86



# B1L103S, U3-ch6, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	4.316
Std Dev	14.47



# B1L103S, U3-ch7, adc0

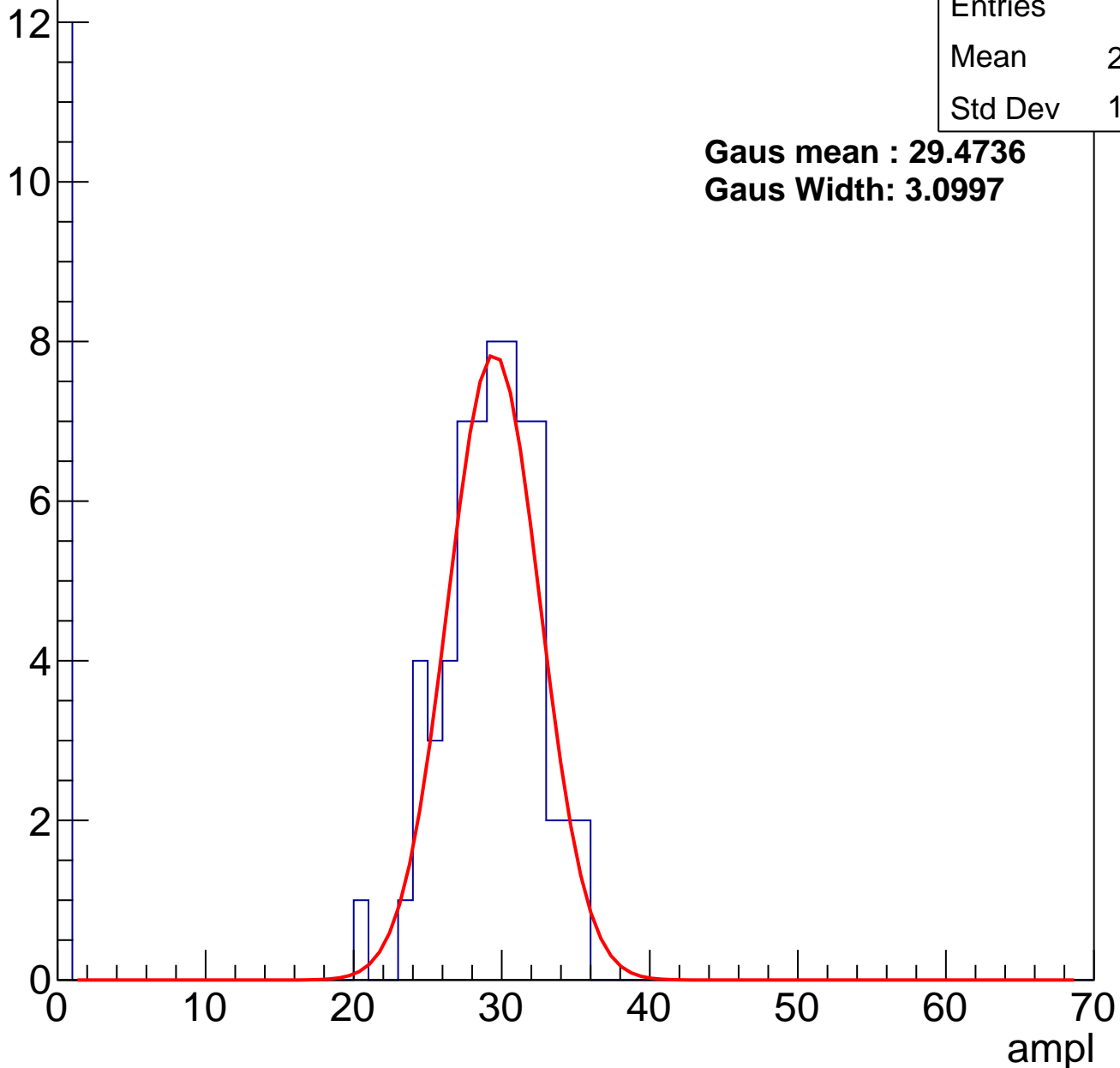
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	75
Mean	24.27
Std Dev	10.95

**Gaus mean : 29.4736**

**Gaus Width: 3.0997**

Entry



# B1L103S, U3-ch7, adc1

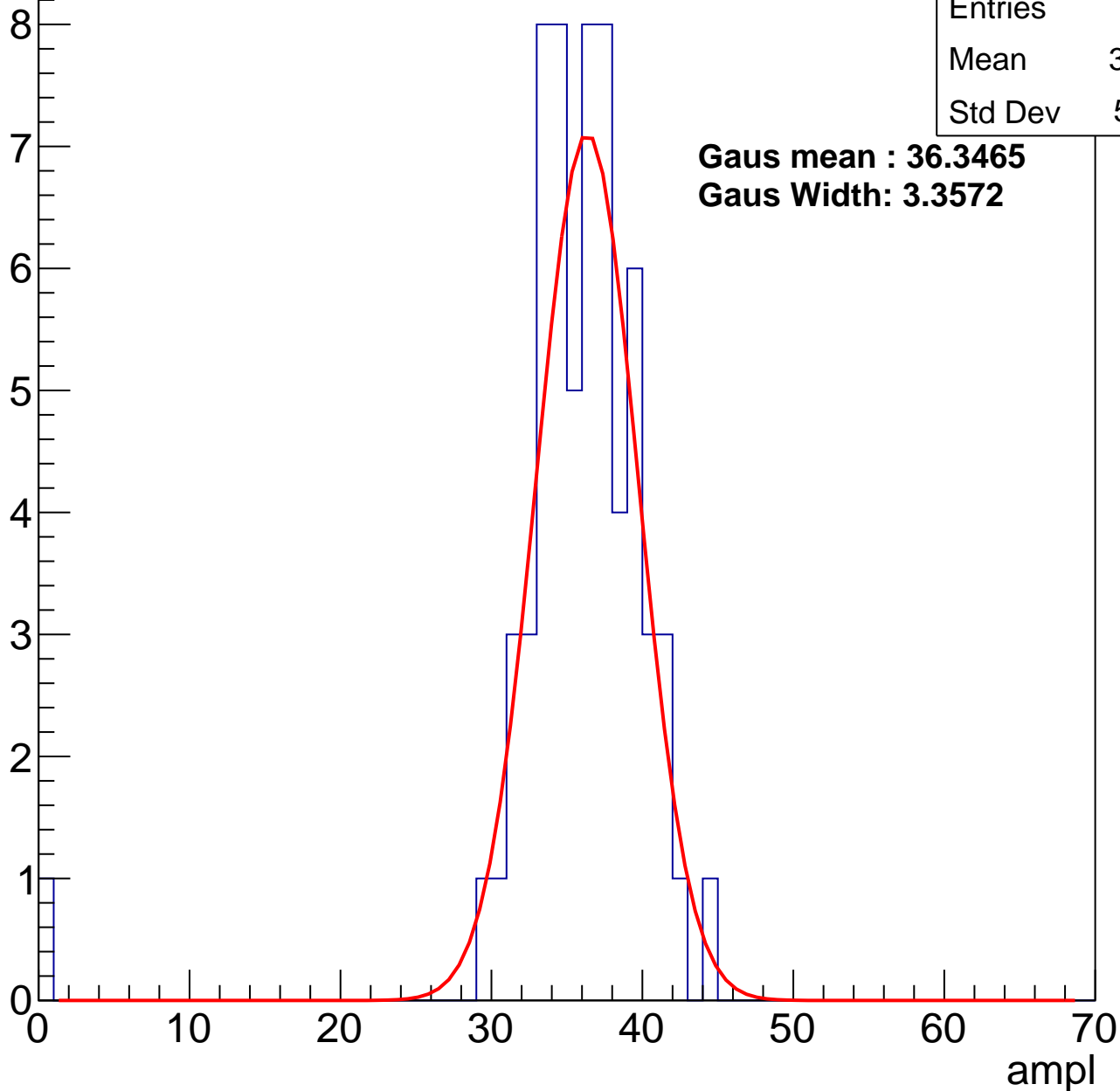
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	35.28
Std Dev	5.421

**Gaus mean : 36.3465**

**Gaus Width: 3.3572**



# B1L103S, U3-ch7, adc2

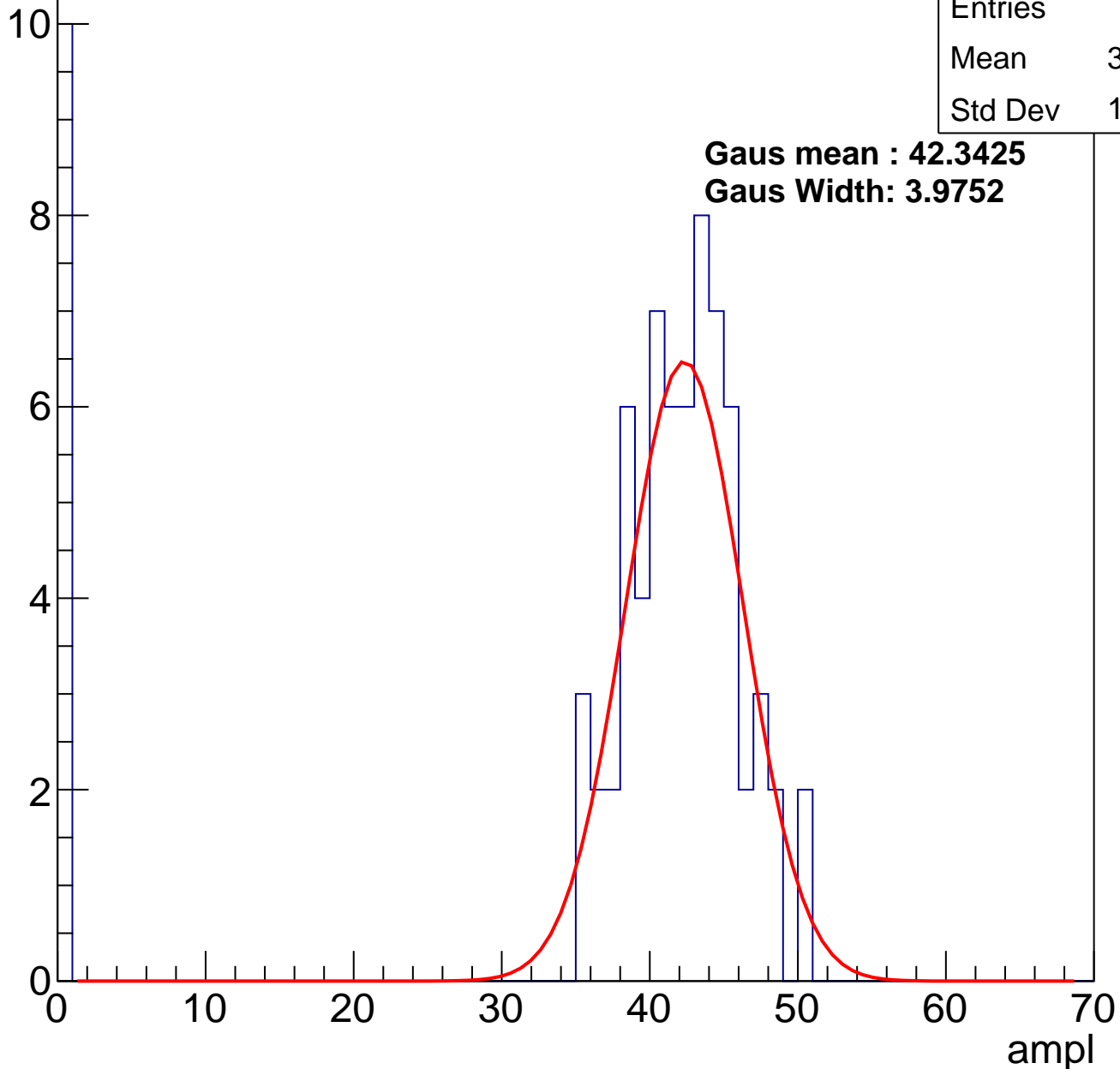
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	76
Mean	36.37
Std Dev	14.54

**Gaus mean : 42.3425**

**Gaus Width: 3.9752**

Entry

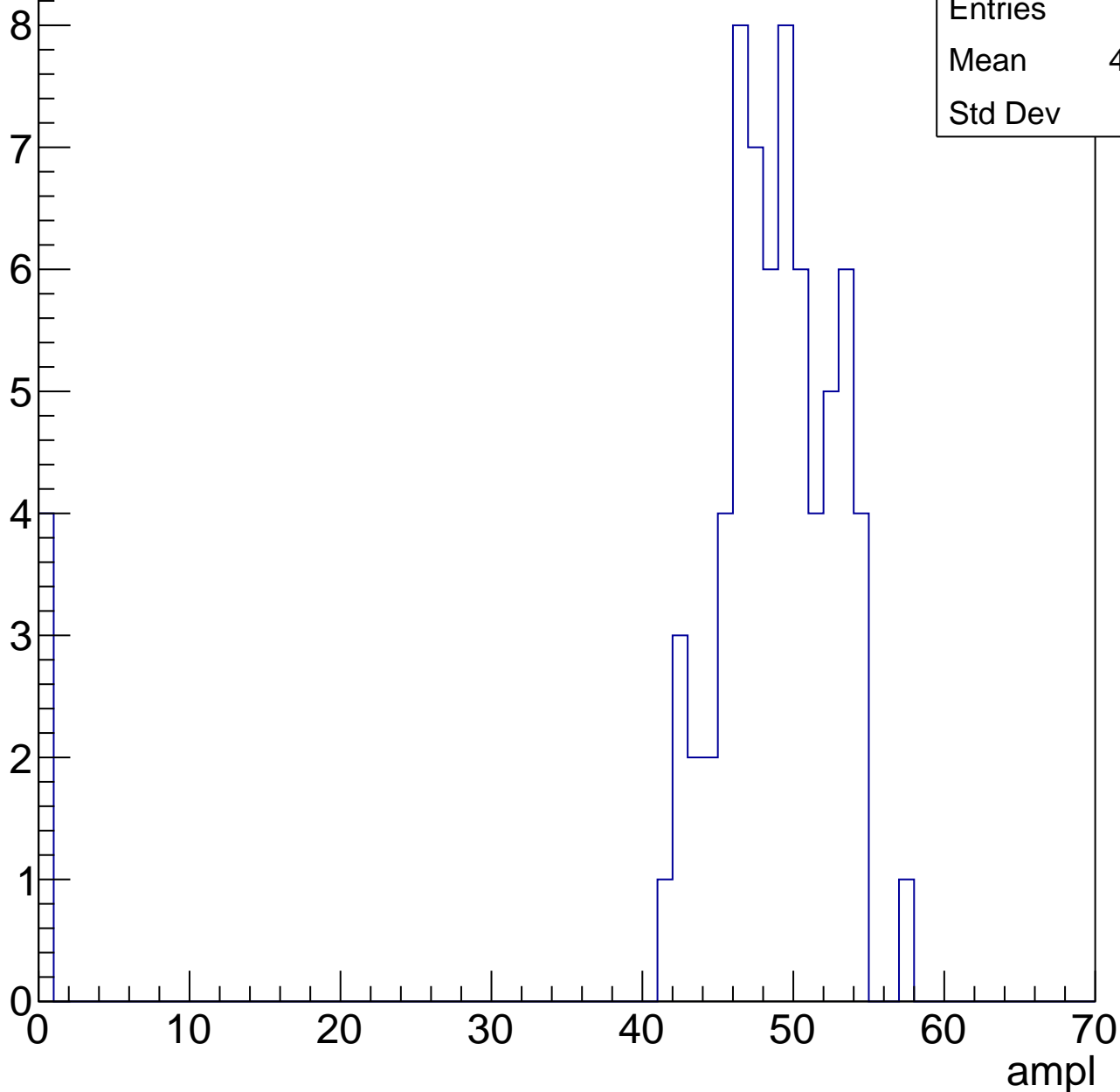


# B1L103S, U3-ch7, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

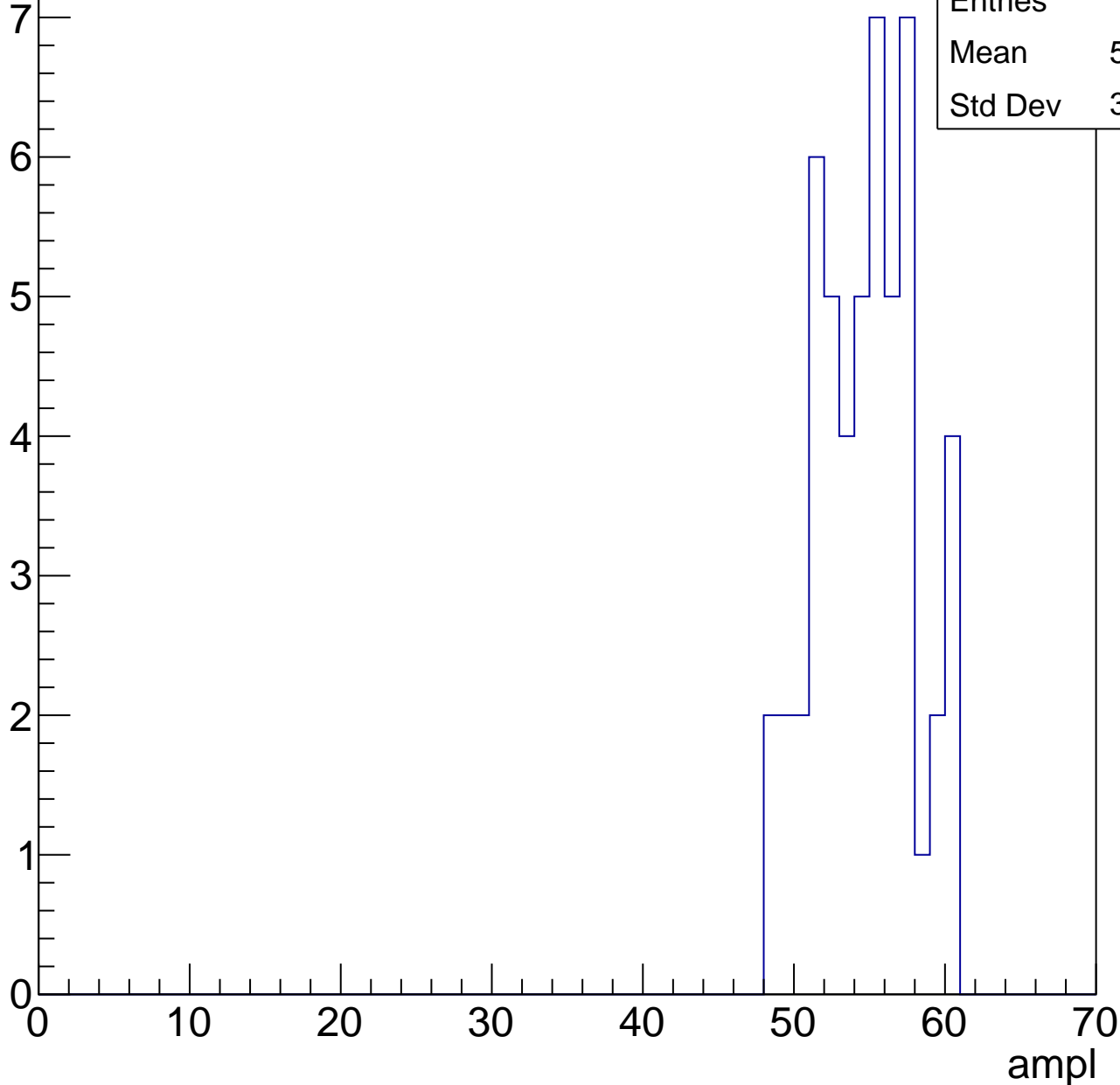
Entries	71
Mean	45.82
Std Dev	11.7



# B1L103S, U3-ch7, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

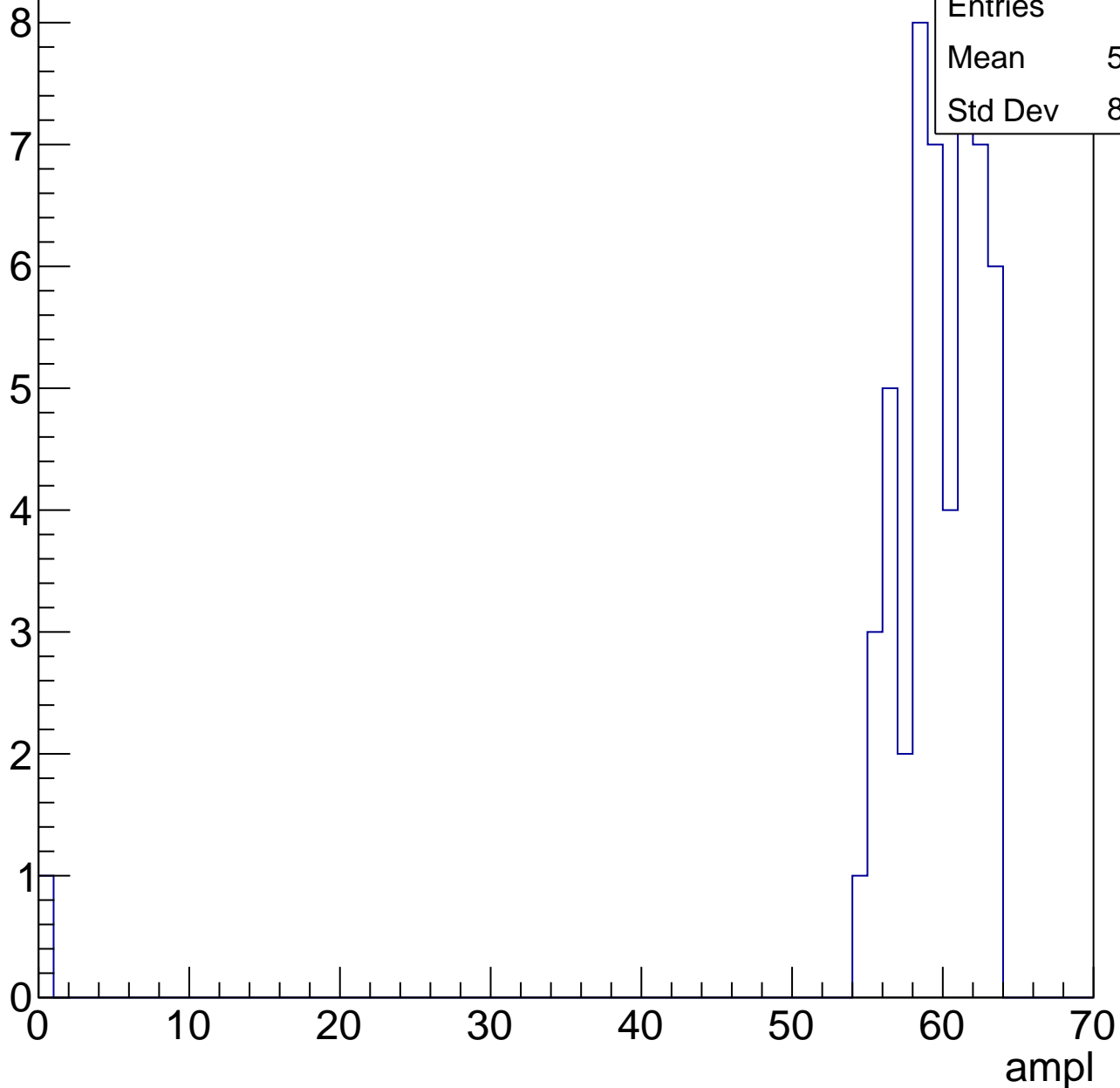


# B1L103S, U3-ch7, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

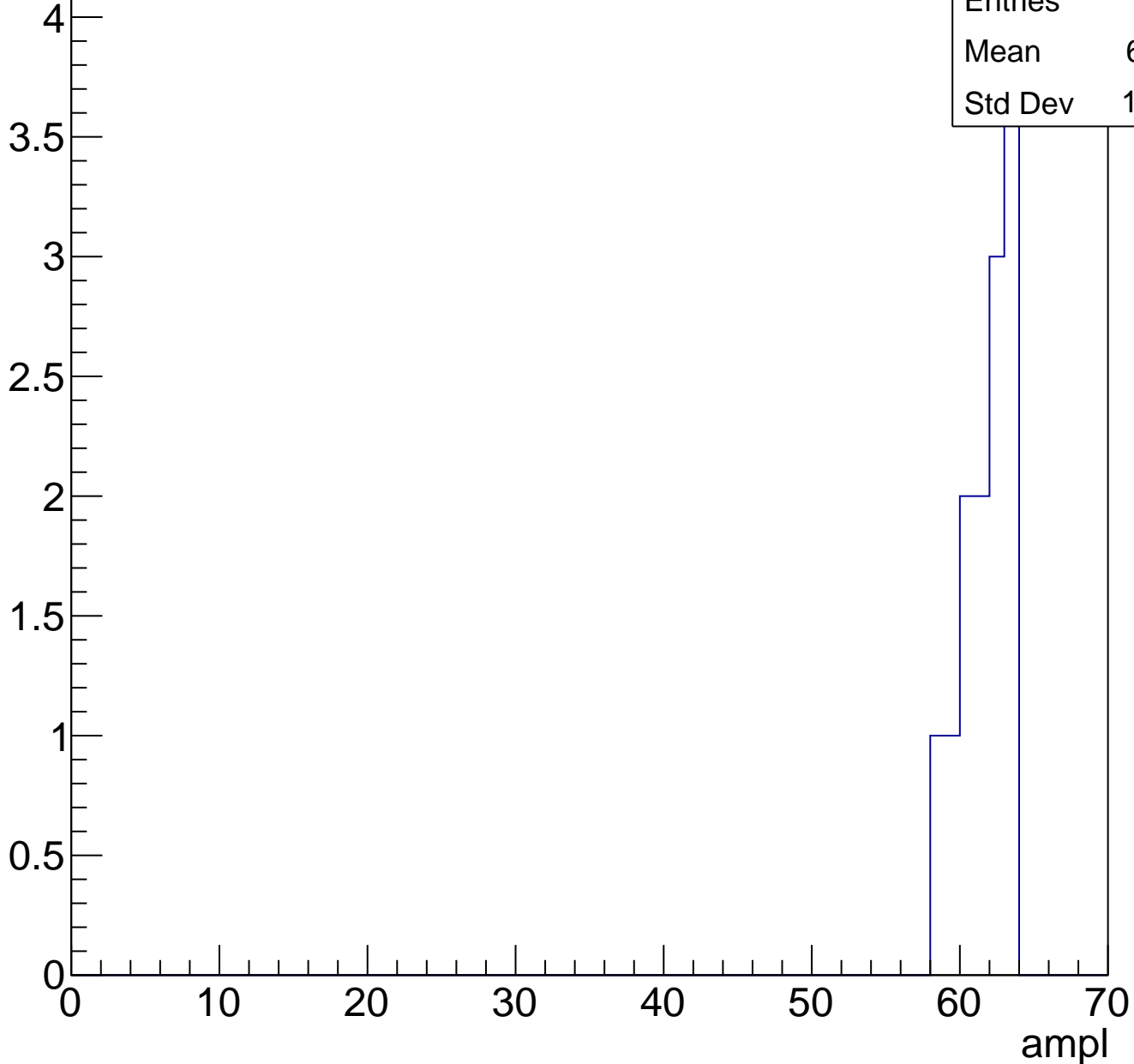
Entries	52
Mean	58.27
Std Dev	8.528



# B1L103S, U3-ch7, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	13
Mean	61.31
Std Dev	1.588



# B1L103S, U3-ch7, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	0
Std Dev	0



# B1L103S, U3-ch8, adc0

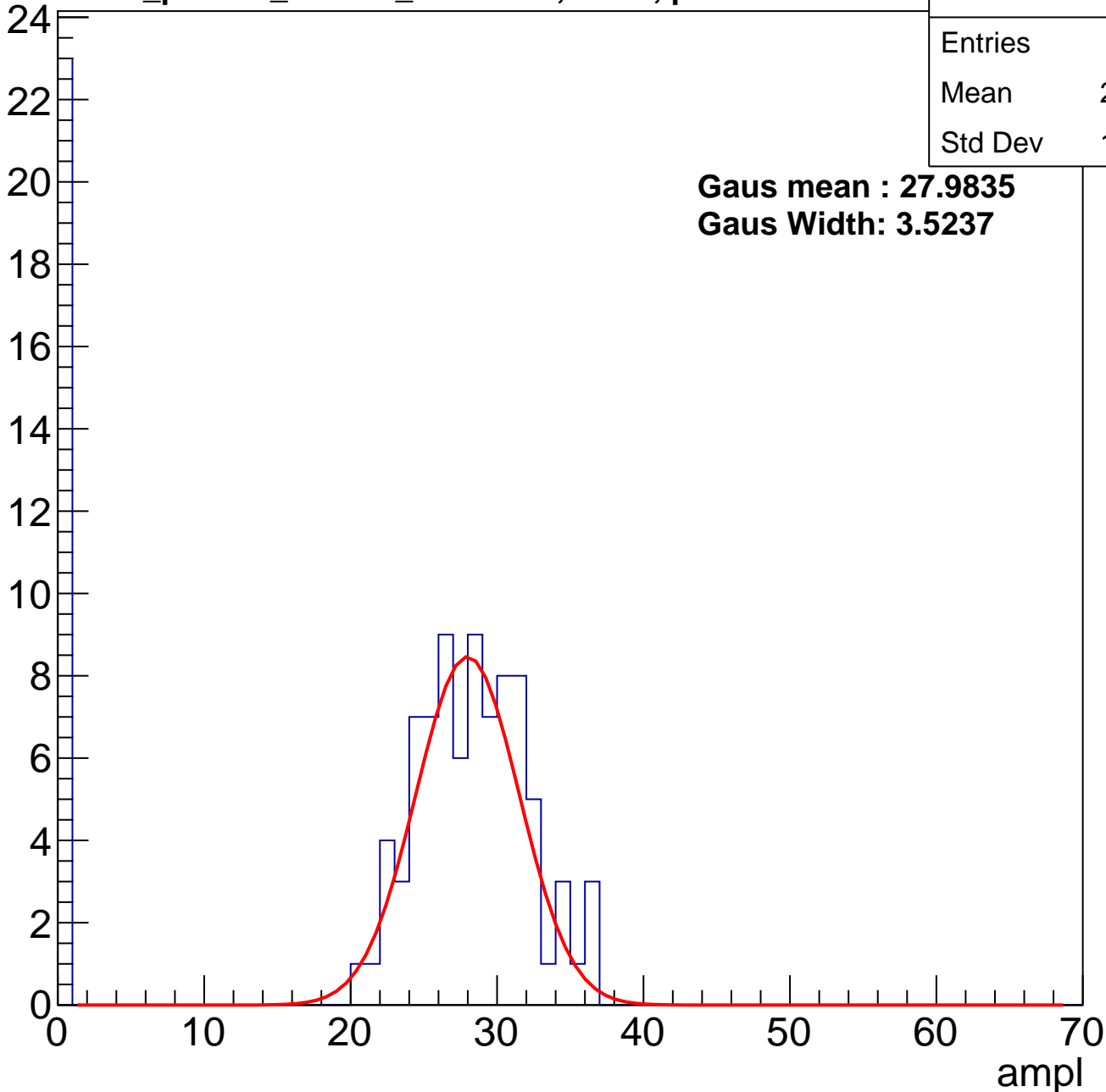
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	106
Mean	21.87
Std Dev	11.96

**Gaus mean : 27.9835**

**Gaus Width: 3.5237**

Entry



# B1L103S, U3-ch8, adc1

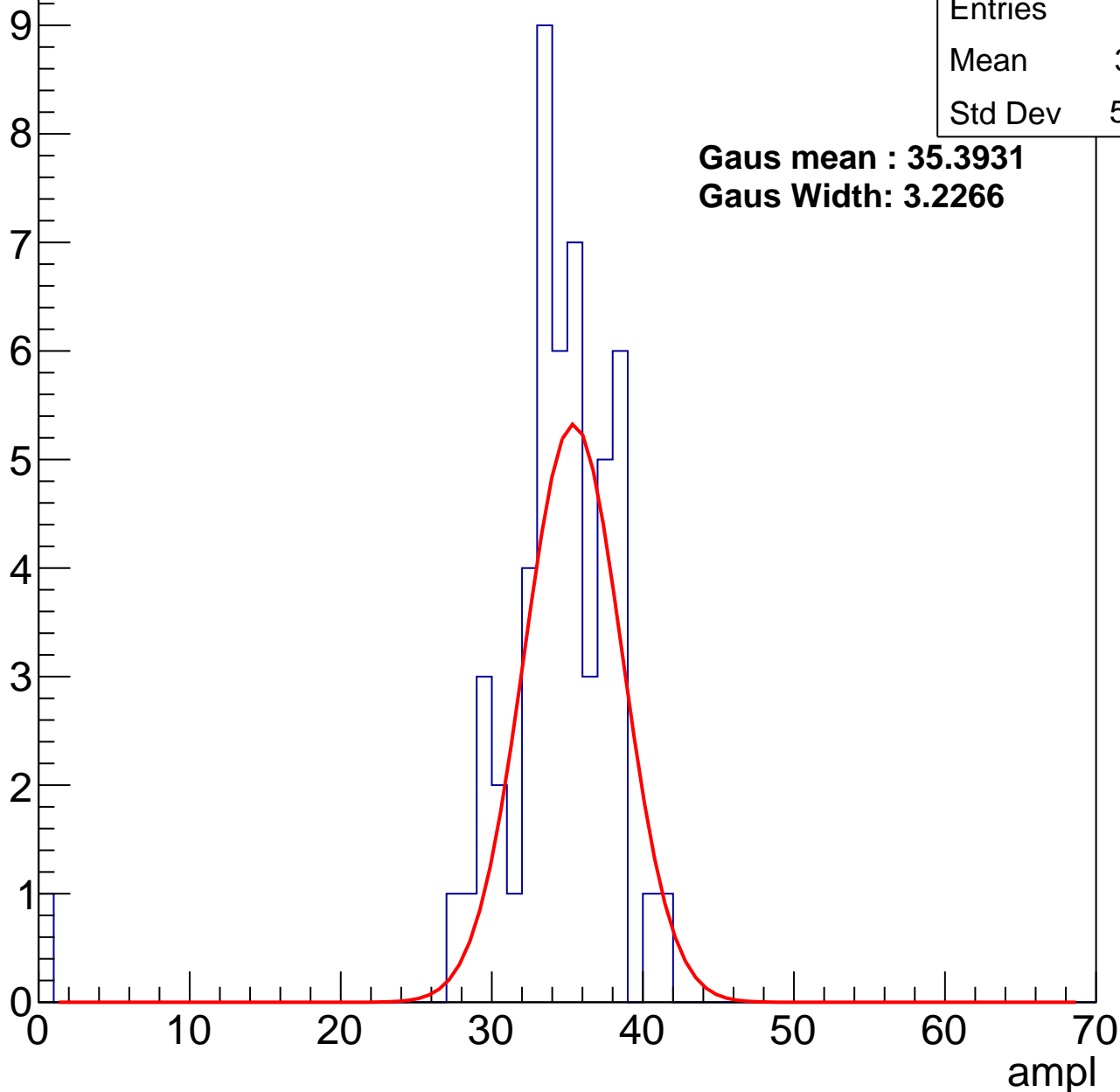
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	51
Mean	33.51
Std Dev	5.627

**Gaus mean : 35.3931**

**Gaus Width: 3.2266**



# B1L103S, U3-ch8, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	71
Mean	33.65
Std Dev	14.69

**Gaus mean : 40.4796**

**Gaus Width: 3.0346**

Entry

10

8

6

4

2

0

0

10

20

30

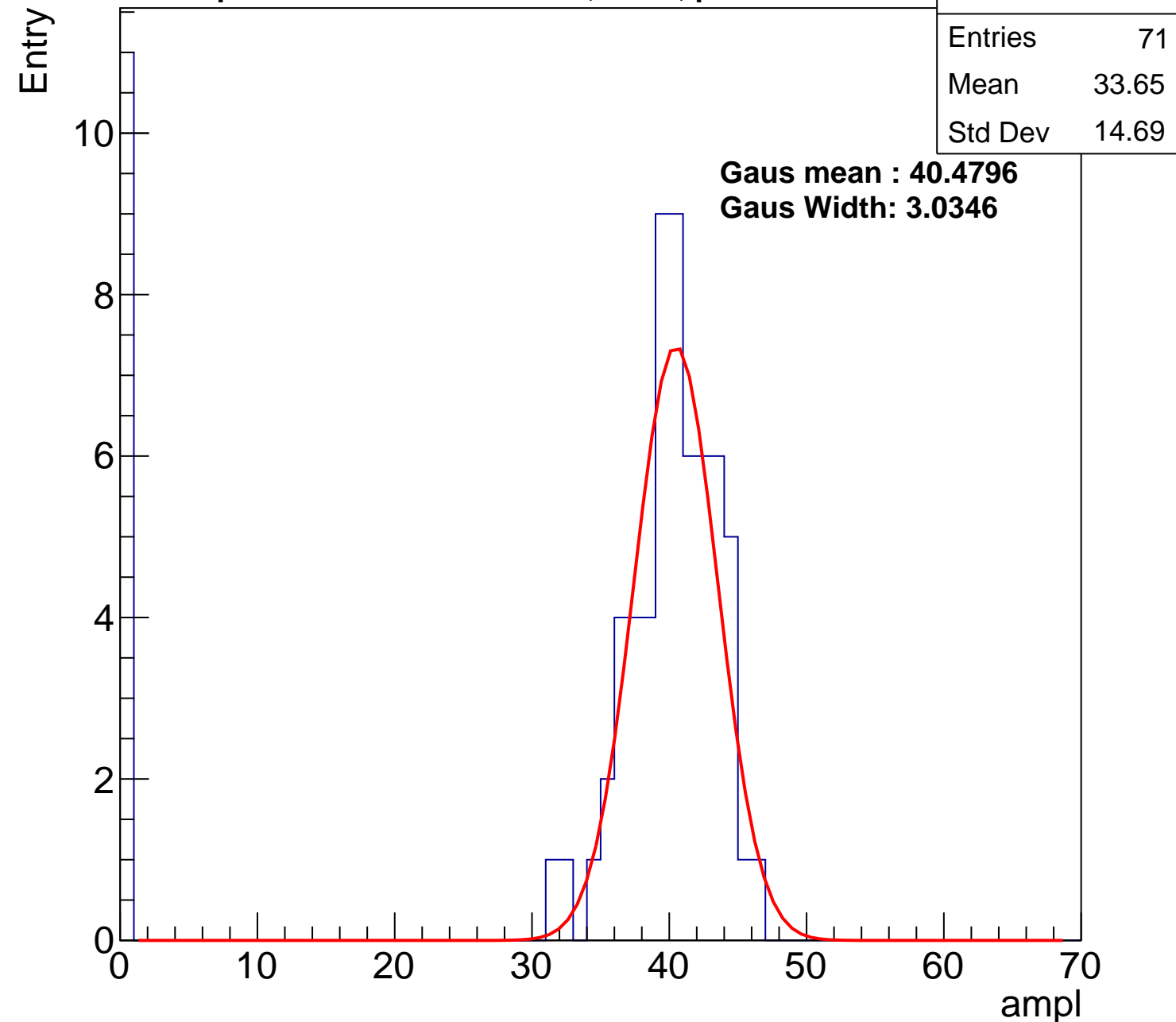
40

50

60

70

ampl

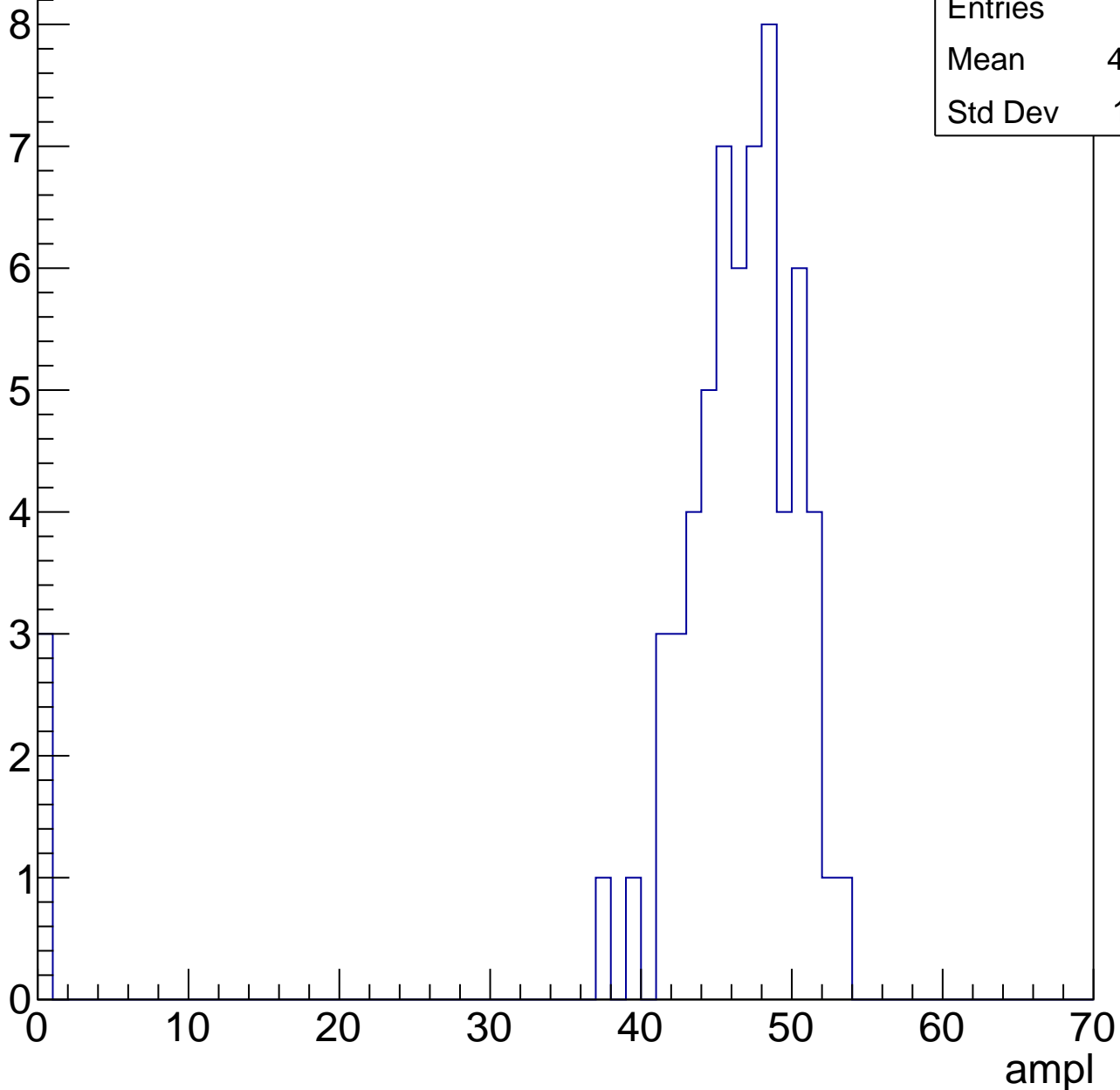


# B1L103S, U3-ch8, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

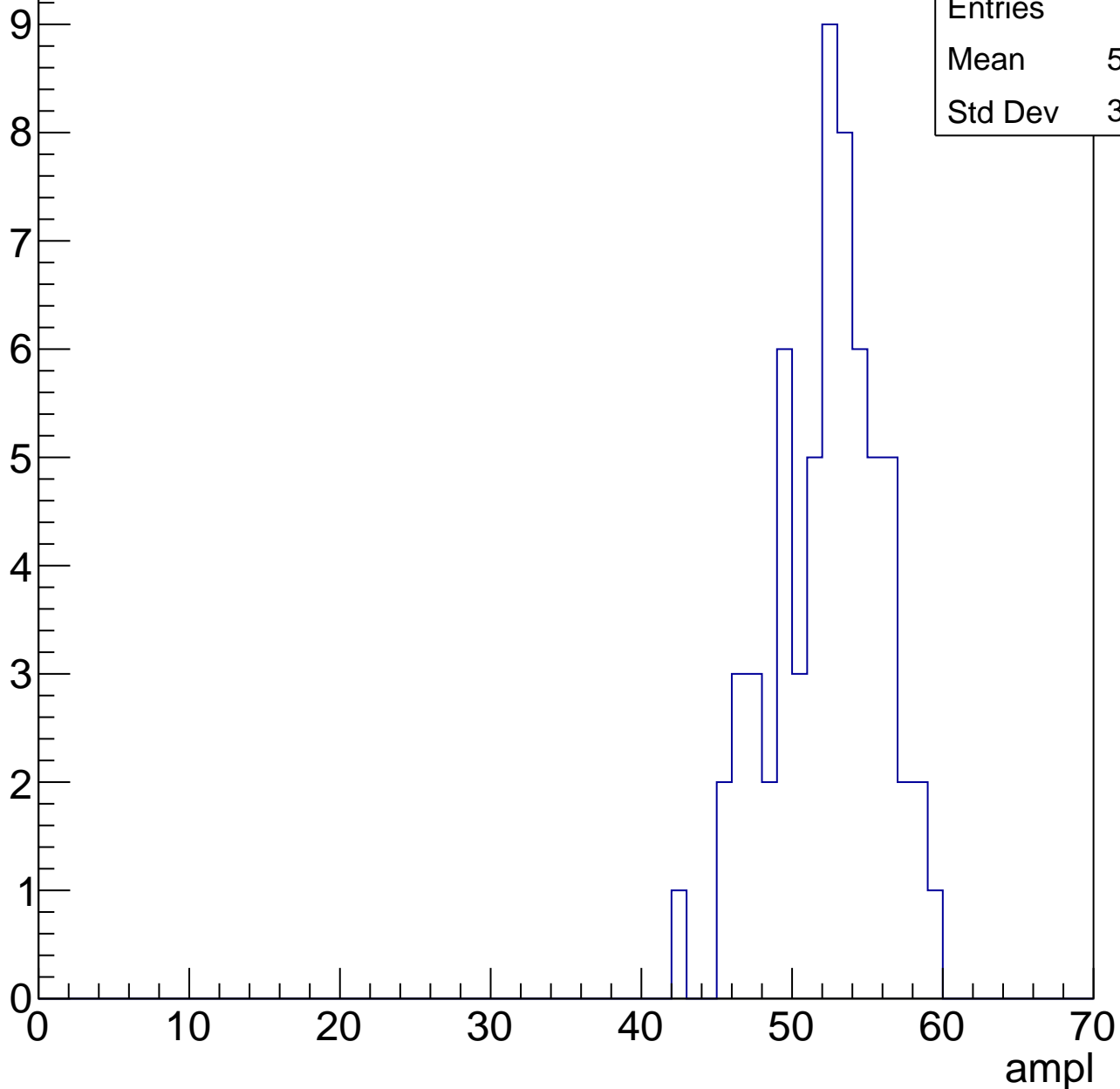
Entries	64
Mean	44.16
Std Dev	10.31



# B1L103S, U3-ch8, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

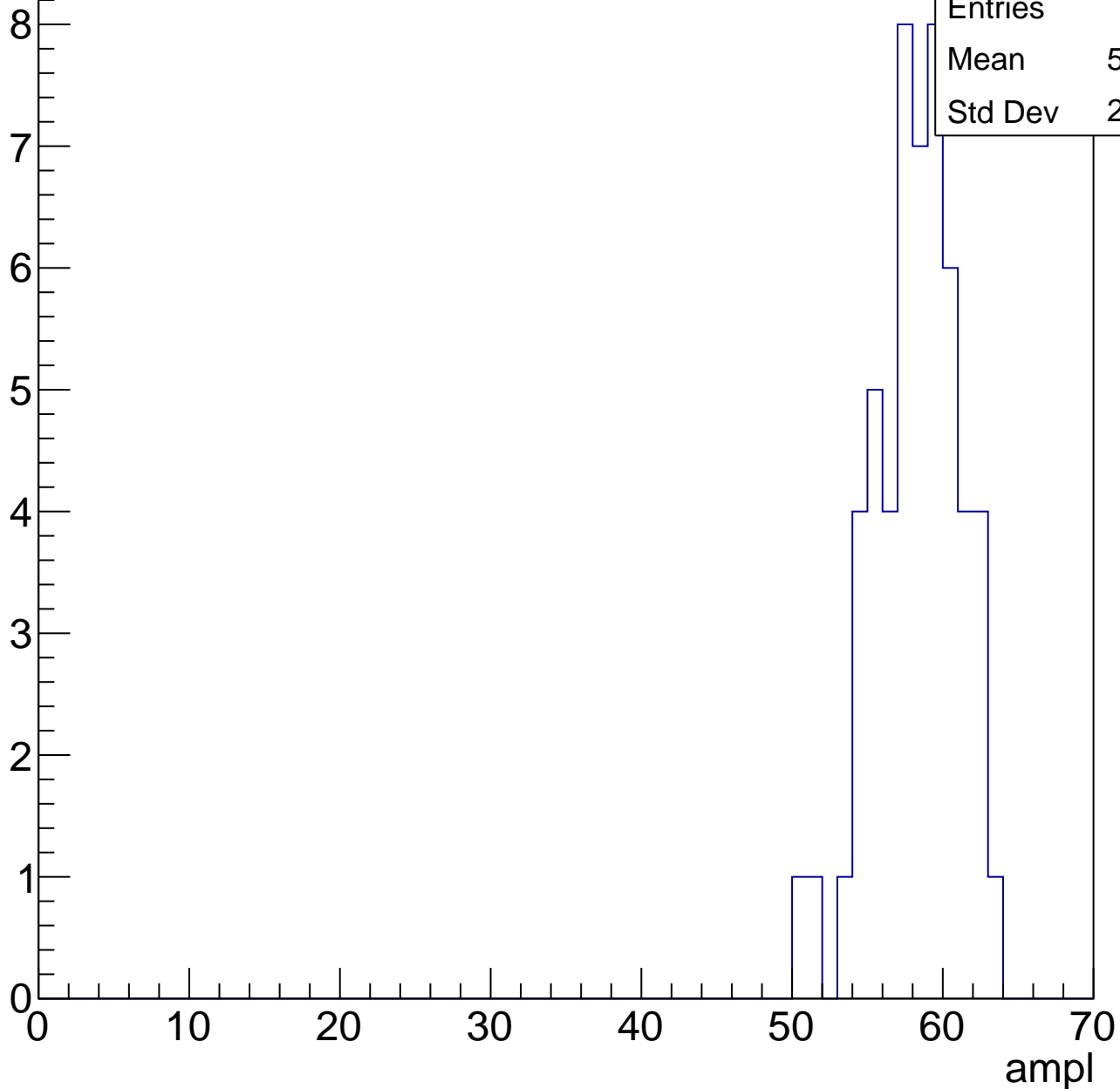
Entry



# B1L103S, U3-ch8, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

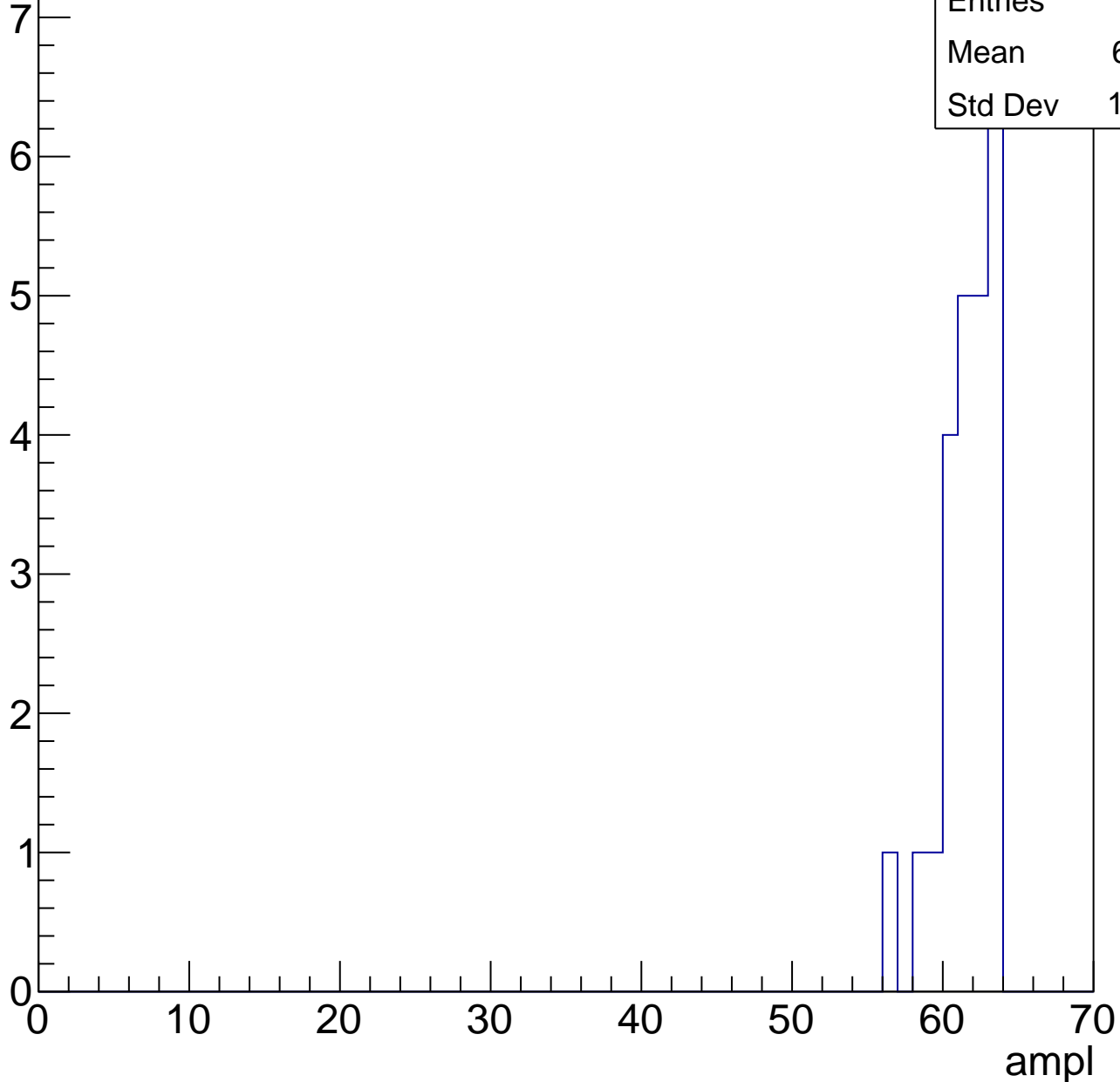


# B1L103S, U3-ch8, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	24
Mean	61.21
Std Dev	1.755





# B1L103S, U3-ch8, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

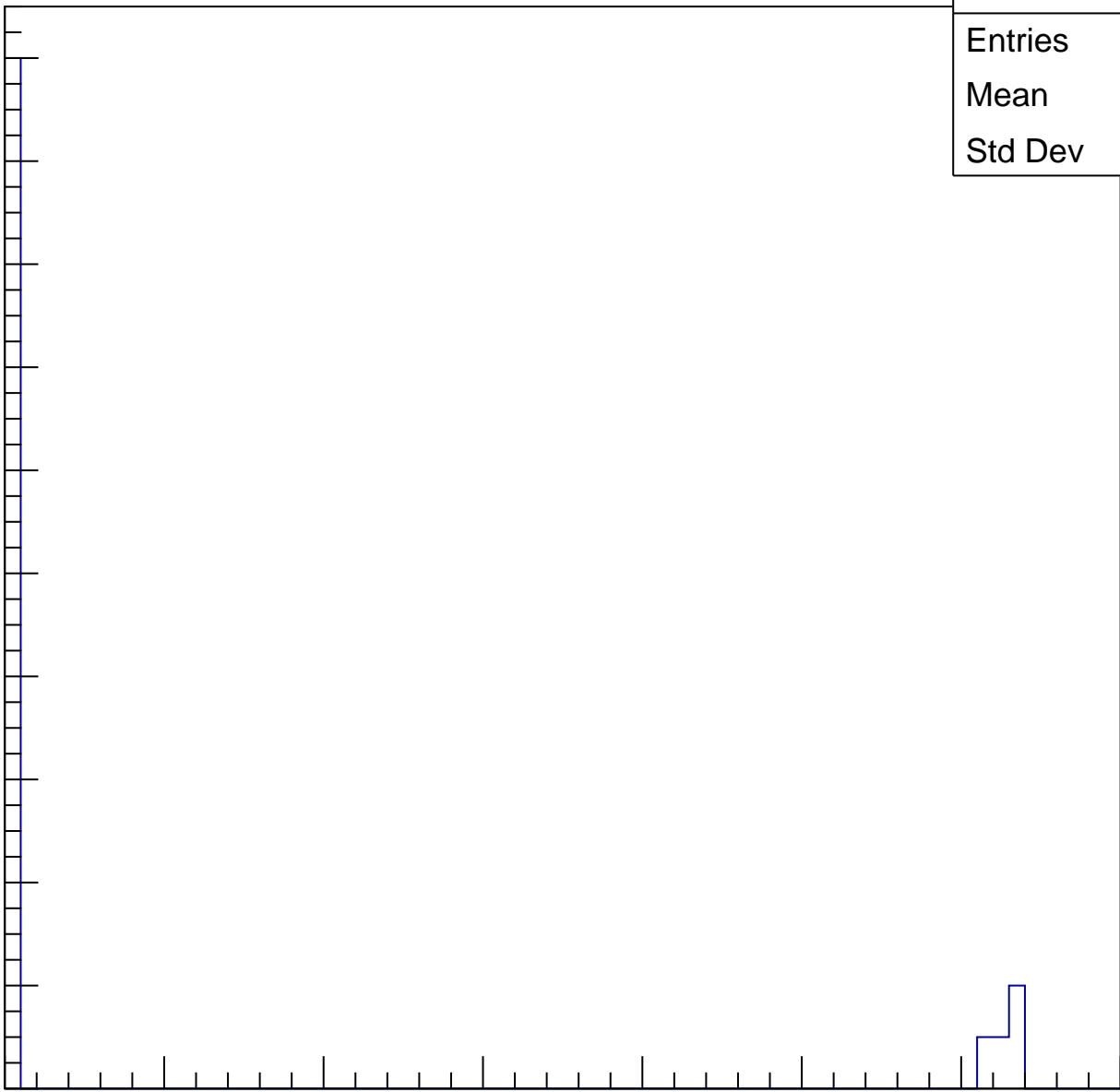
Entries	24
Mean	10.38
Std Dev	23.2

Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U3-ch9, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	77
Mean	24.69
Std Dev	10.64

**Gaus mean : 29.4579**

**Gaus Width: 4.2939**

Entry

10

8

6

4

2

0

ampl

0

10

20

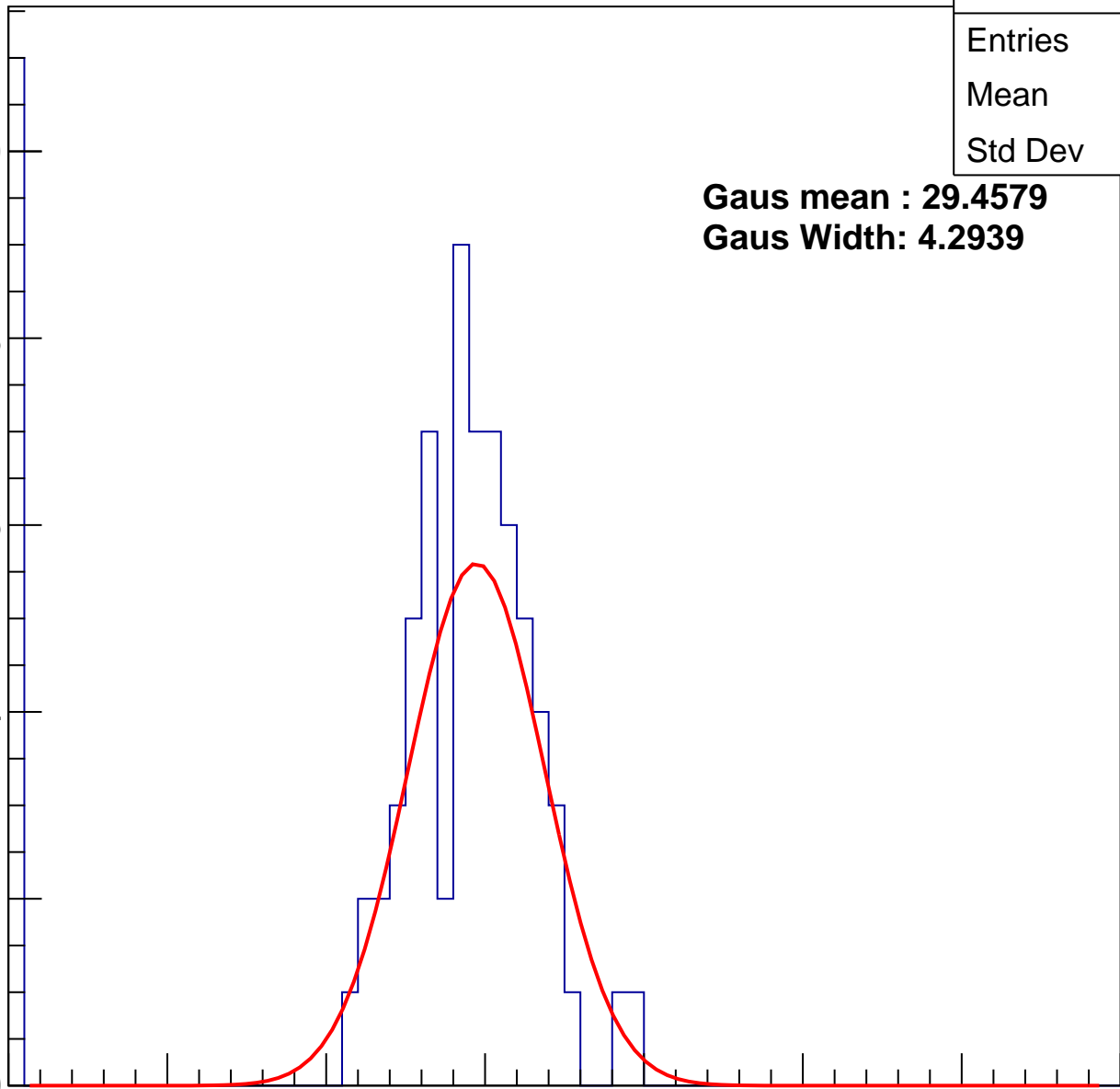
30

40

50

60

70



# B1L103S, U3-ch9, adc1

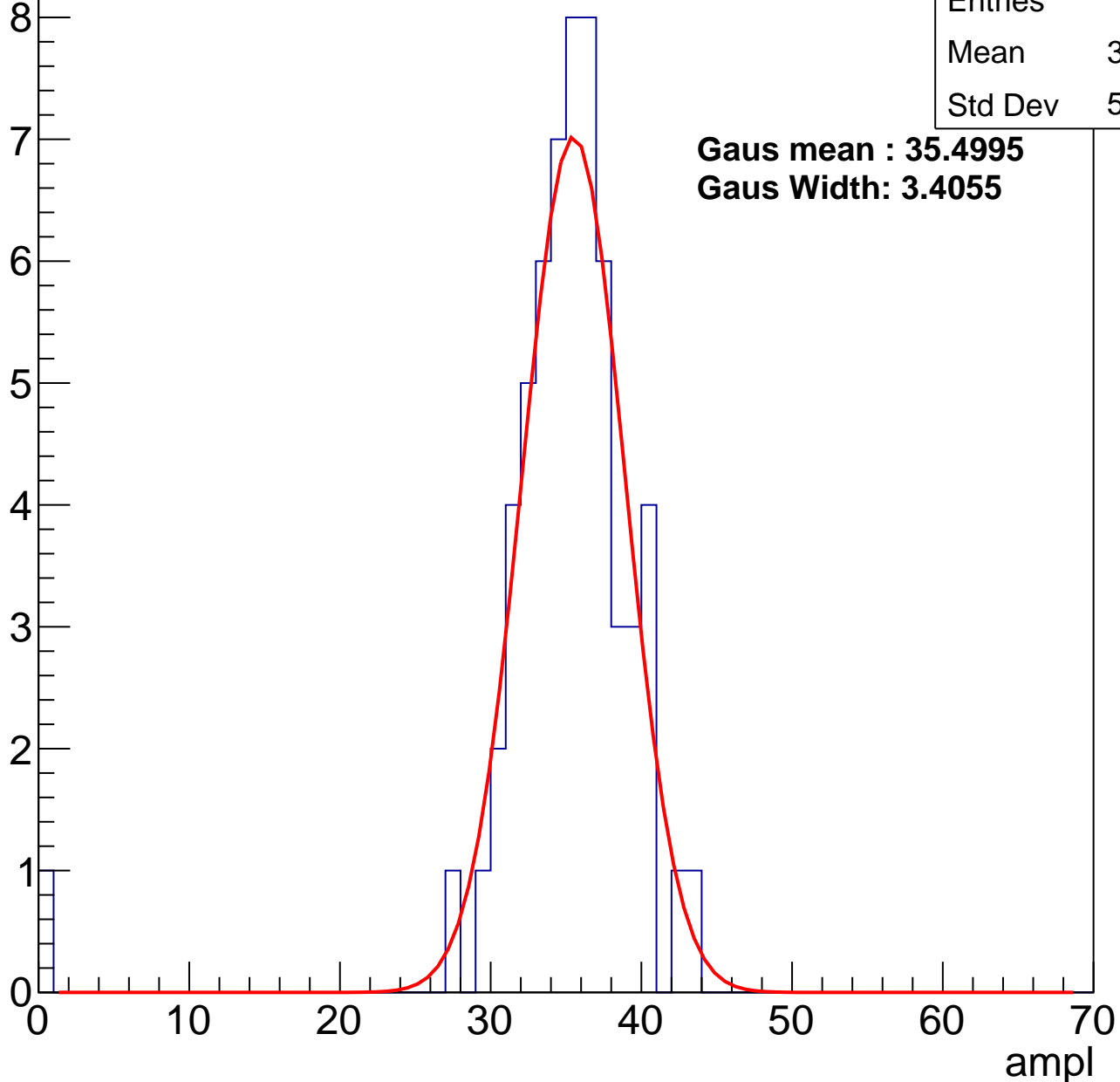
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	34.46
Std Dev	5.458

**Gaus mean : 35.4995**

**Gaus Width: 3.4055**



# B1L103S, U3-ch9, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	75
Mean	35.45
Std Dev	14.97

**Gaus mean : 41.9525**

**Gaus Width: 3.3452**

Entry

10

8

6

4

2

0

0

10

20

30

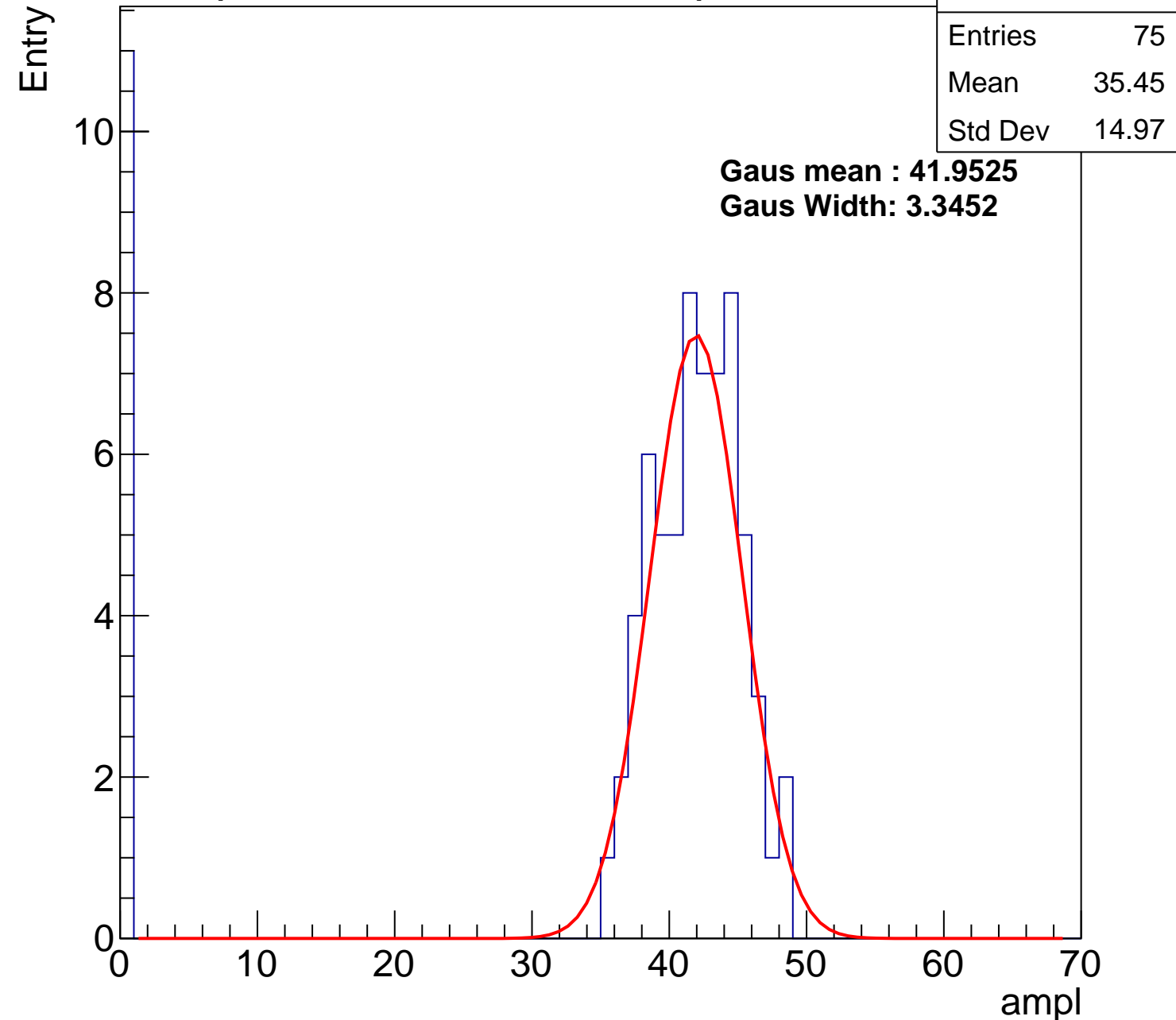
40

50

60

70

ampl

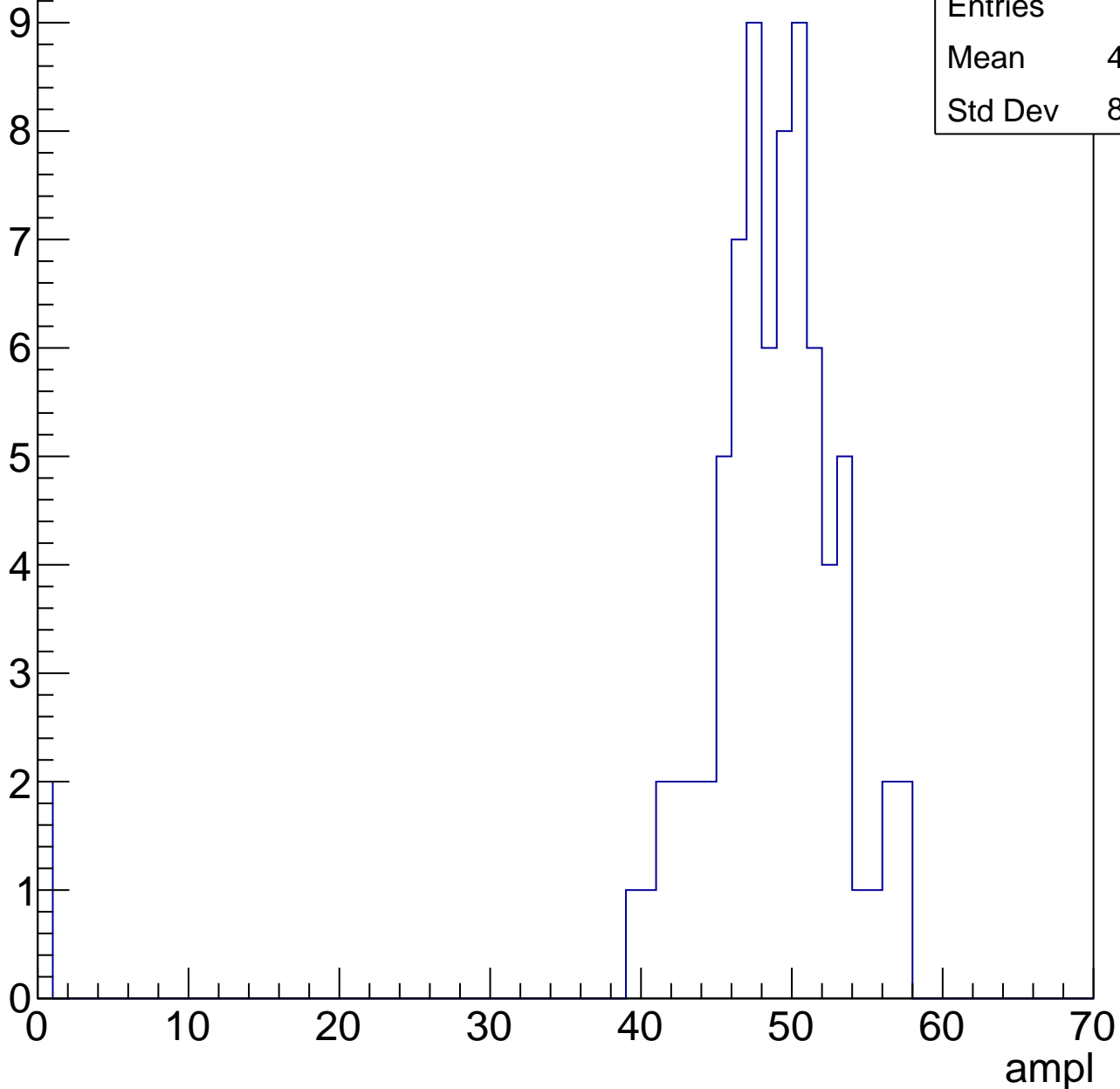


# B1L103S, U3-ch9, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	77
Mean	47.18
Std Dev	8.602

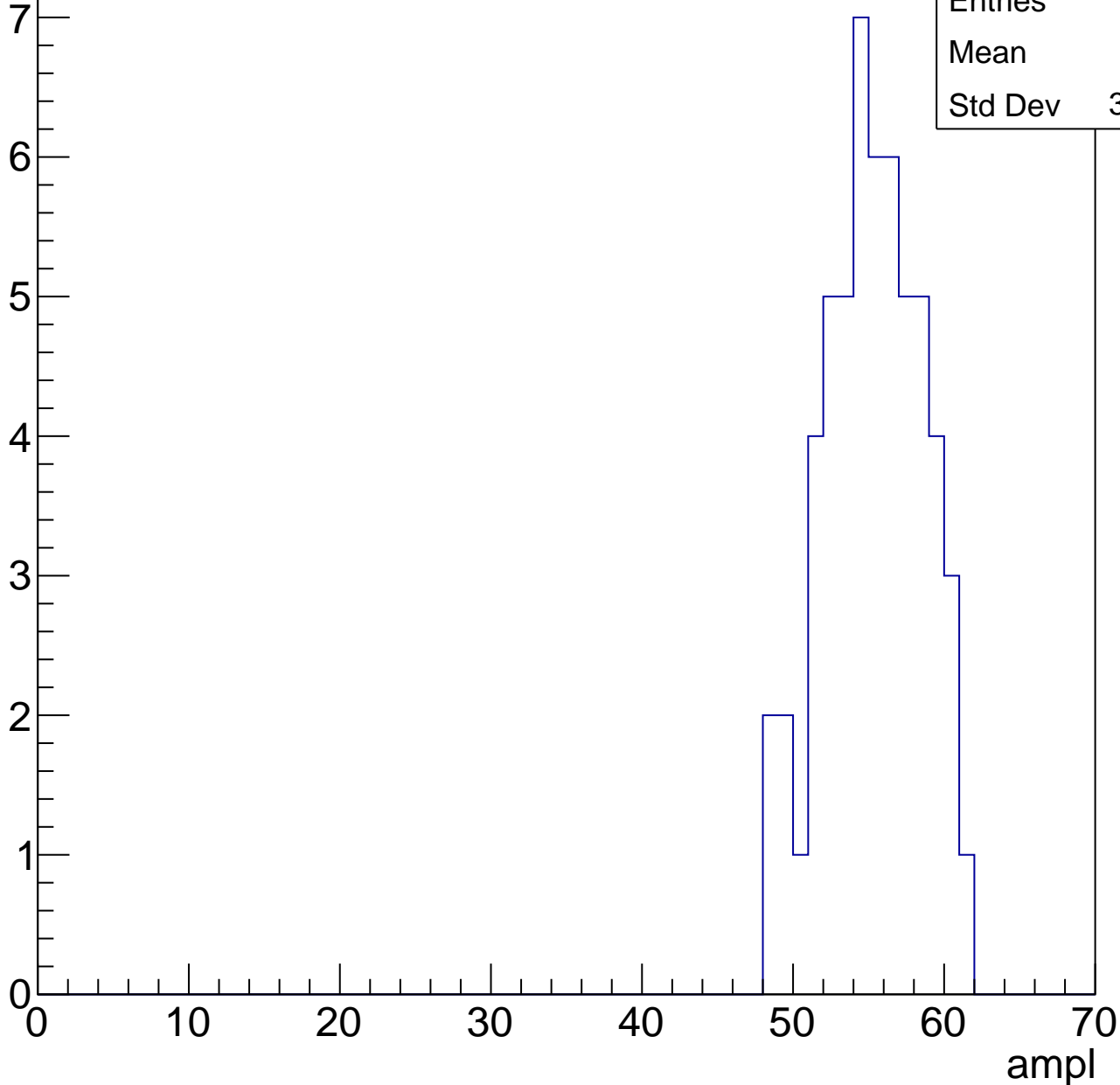


# B1L103S, U3-ch9, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	56
Mean	54.8
Std Dev	3.204

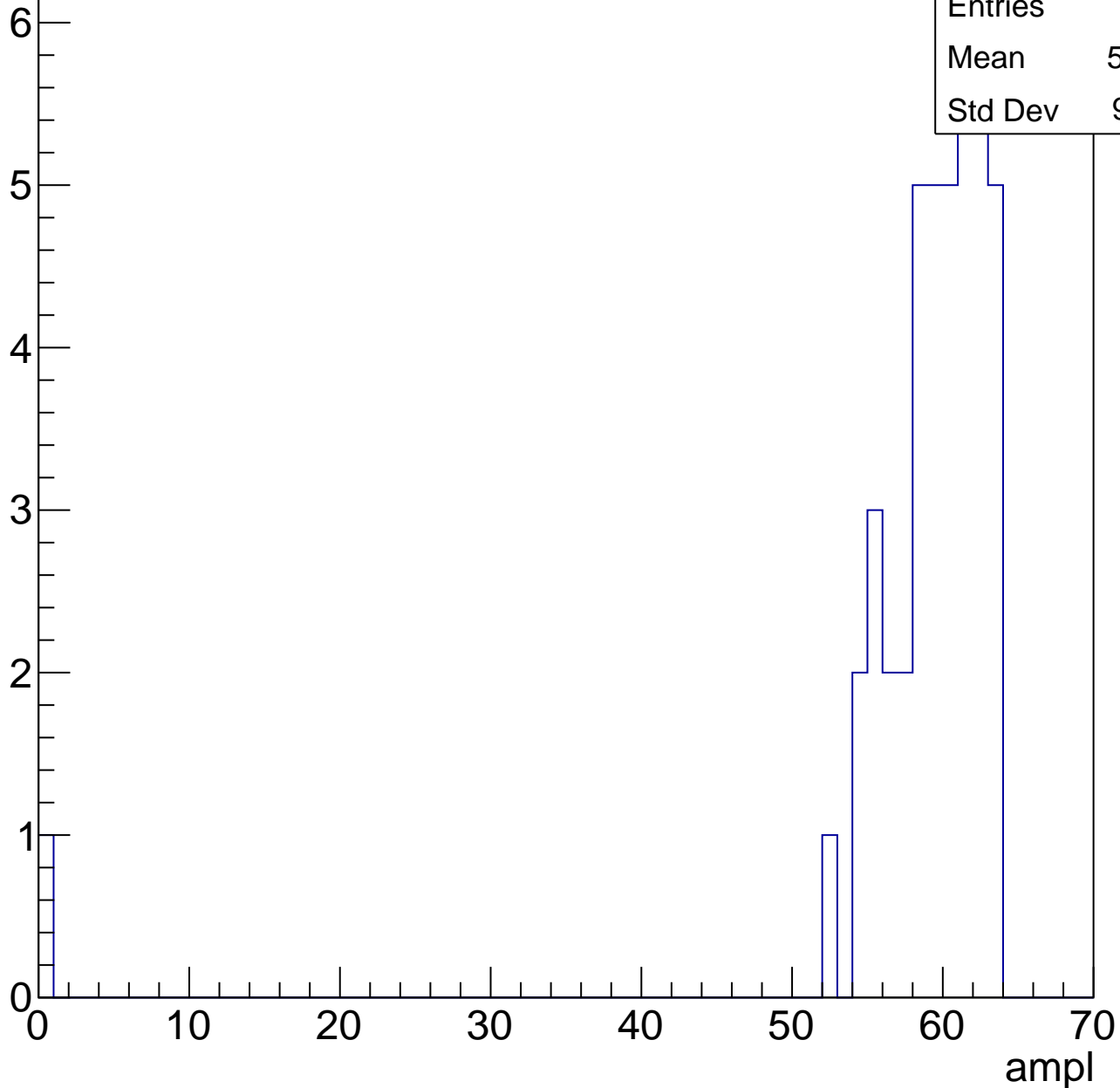


# B1L103S, U3-ch9, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

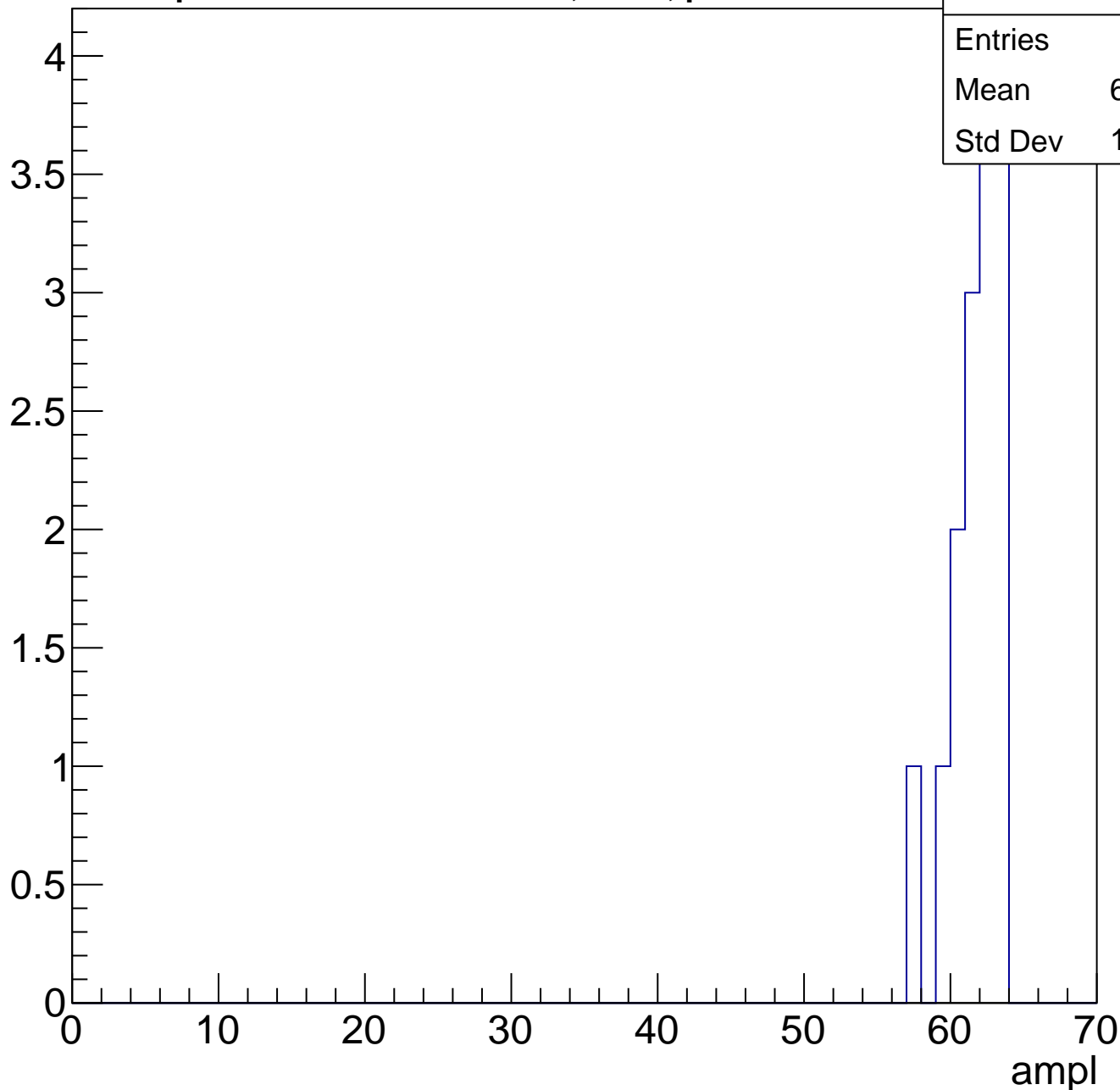
Entries	43
Mean	57.88
Std Dev	9.361



# B1L103S, U3-ch9, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



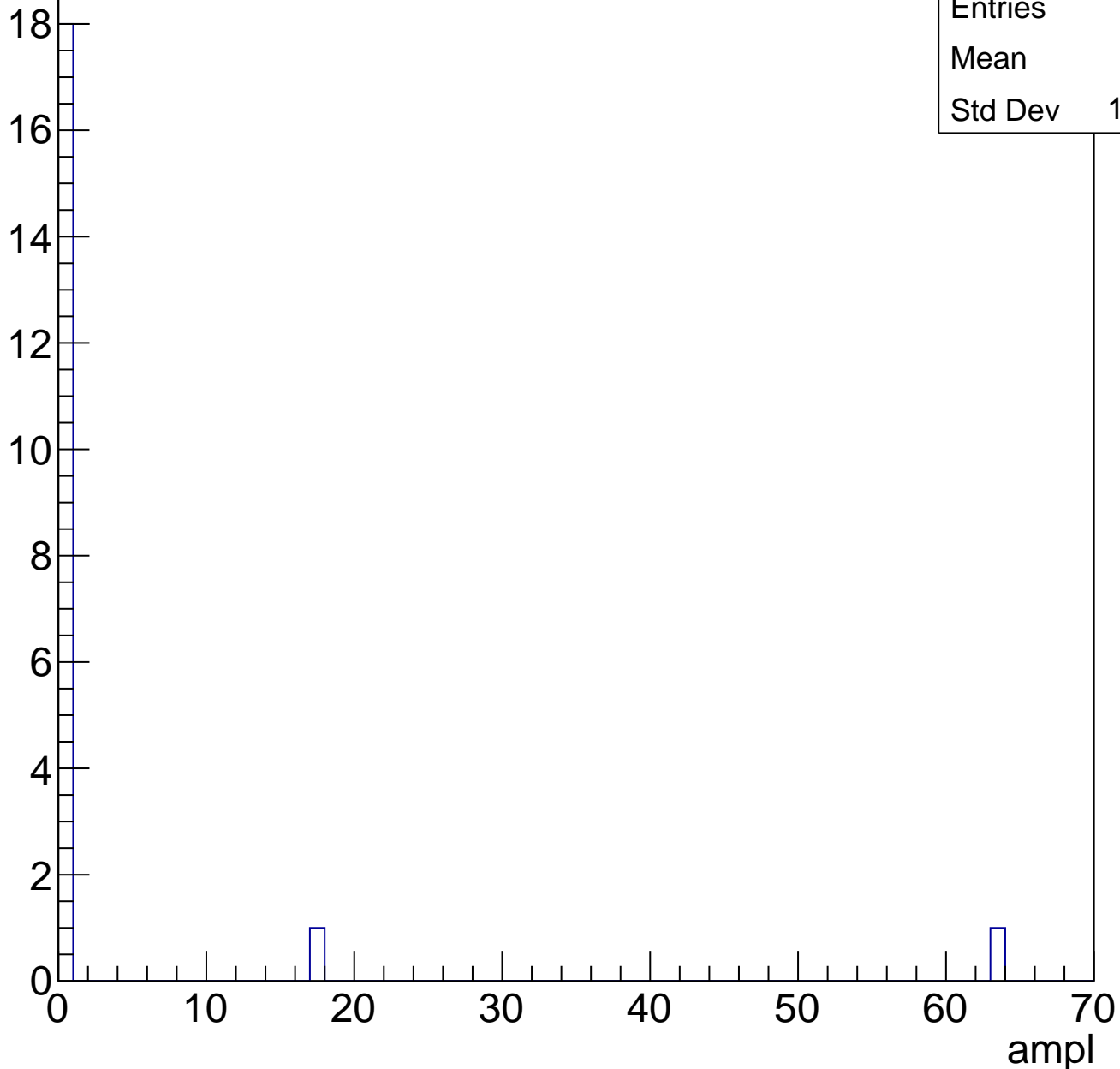


# B1L103S, U3-ch9, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	4
Std Dev	14.03

Entry



# B1L103S, U3-ch10, adc0

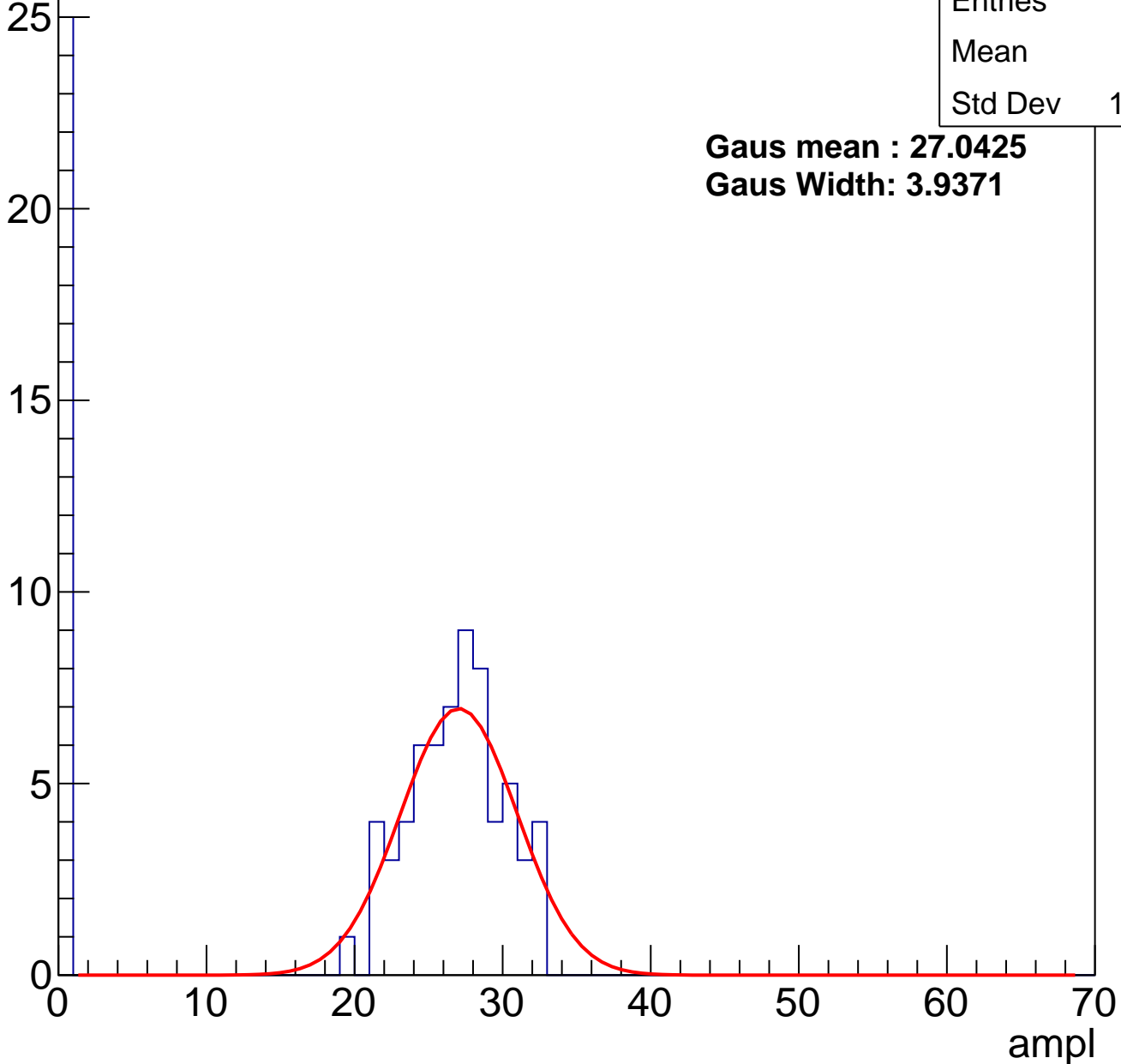
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	89
Mean	19
Std Dev	12.17

**Gaus mean : 27.0425**

**Gaus Width: 3.9371**

Entry



# B1L103S, U3-ch10, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	97
Mean	29.79
Std Dev	11.75

**Gaus mean : 34.3099**

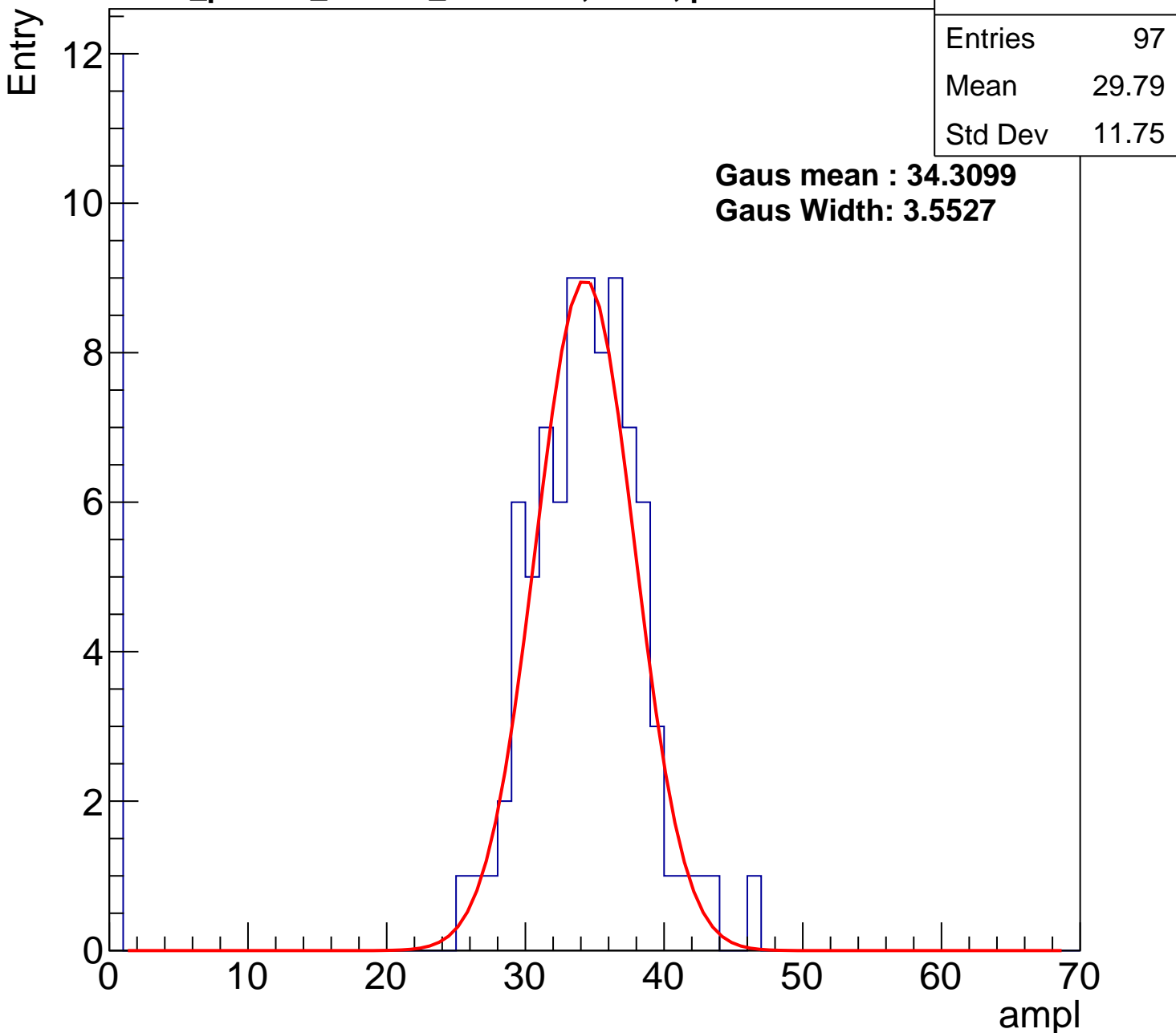
**Gaus Width: 3.5527**

Entry

12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch10, adc2

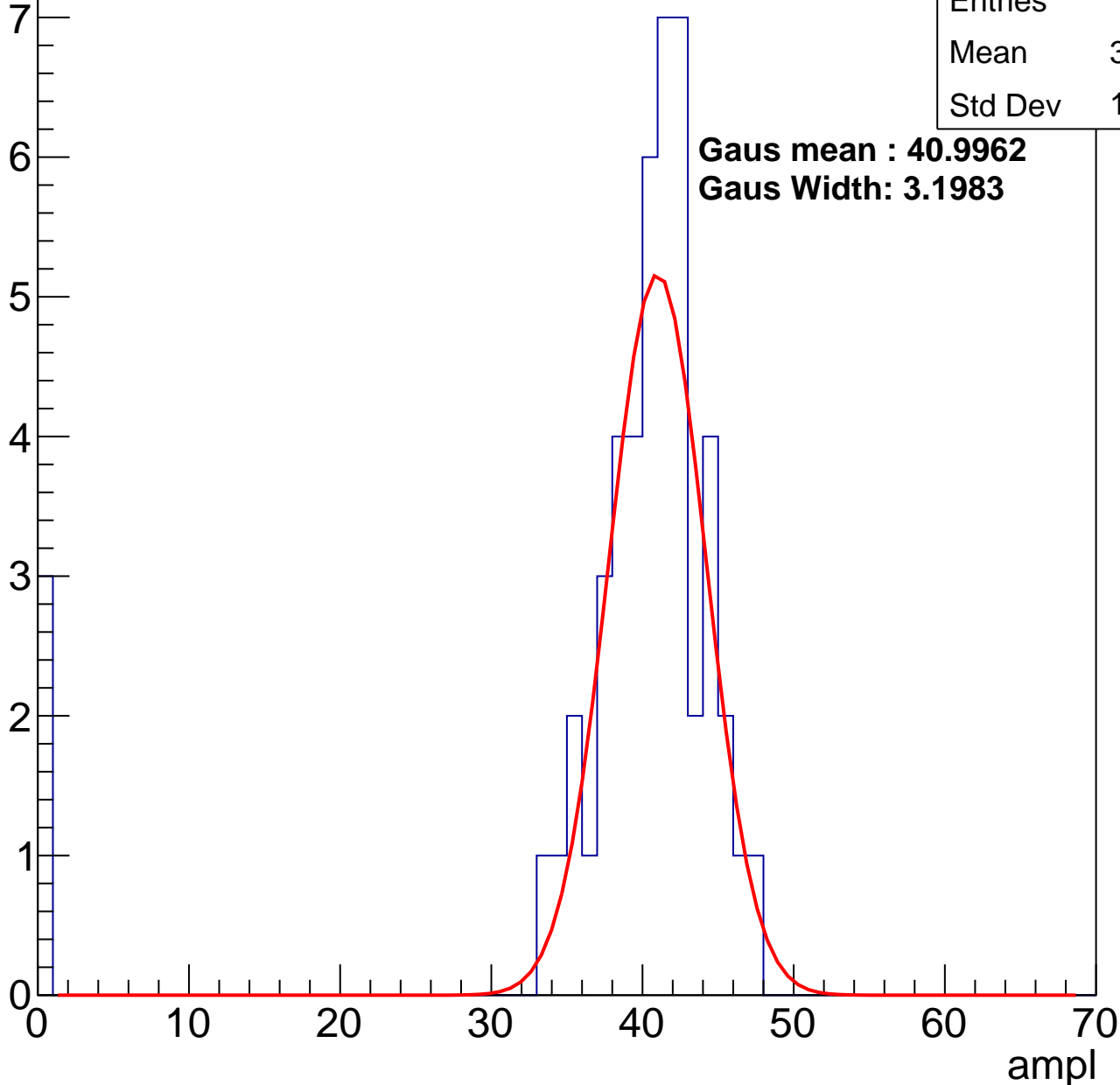
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	49
Mean	37.92
Std Dev	10.14

**Gaus mean : 40.9962**

**Gaus Width: 3.1983**

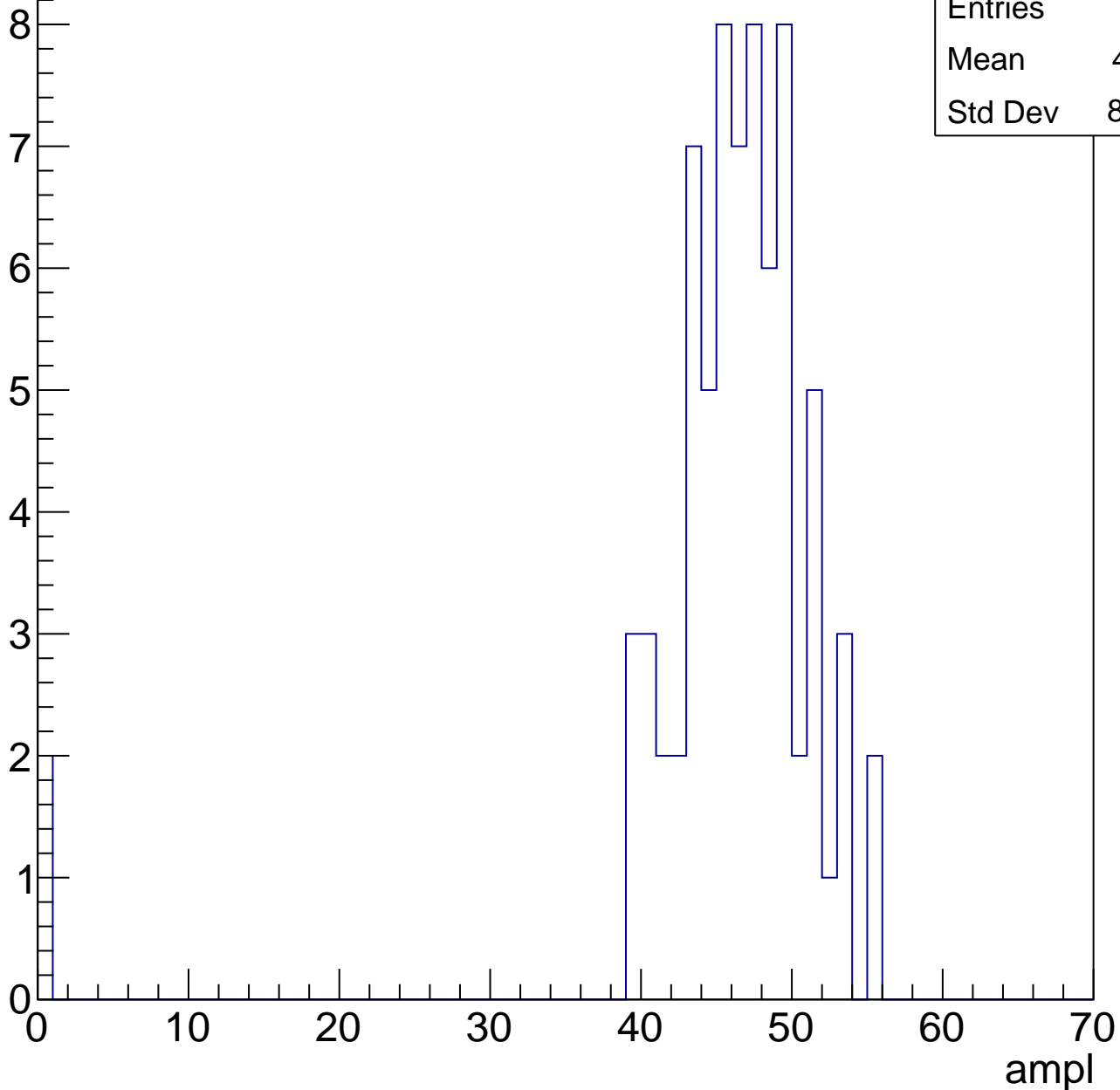


# B1L103S, U3-ch10, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	74
Mean	45.11
Std Dev	8.388

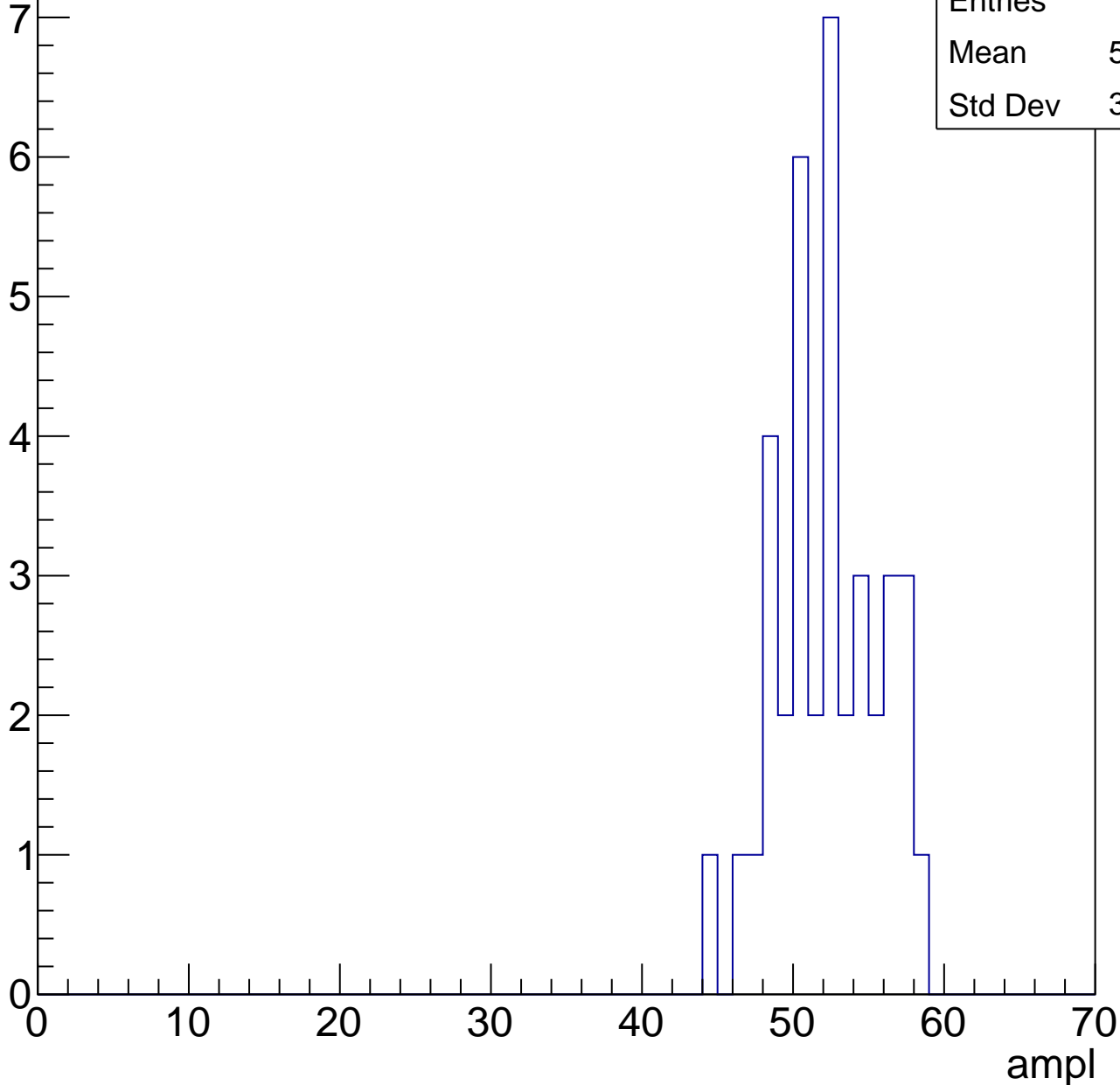


# B1L103S, U3-ch10, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	38
Mean	51.79
Std Dev	3.334

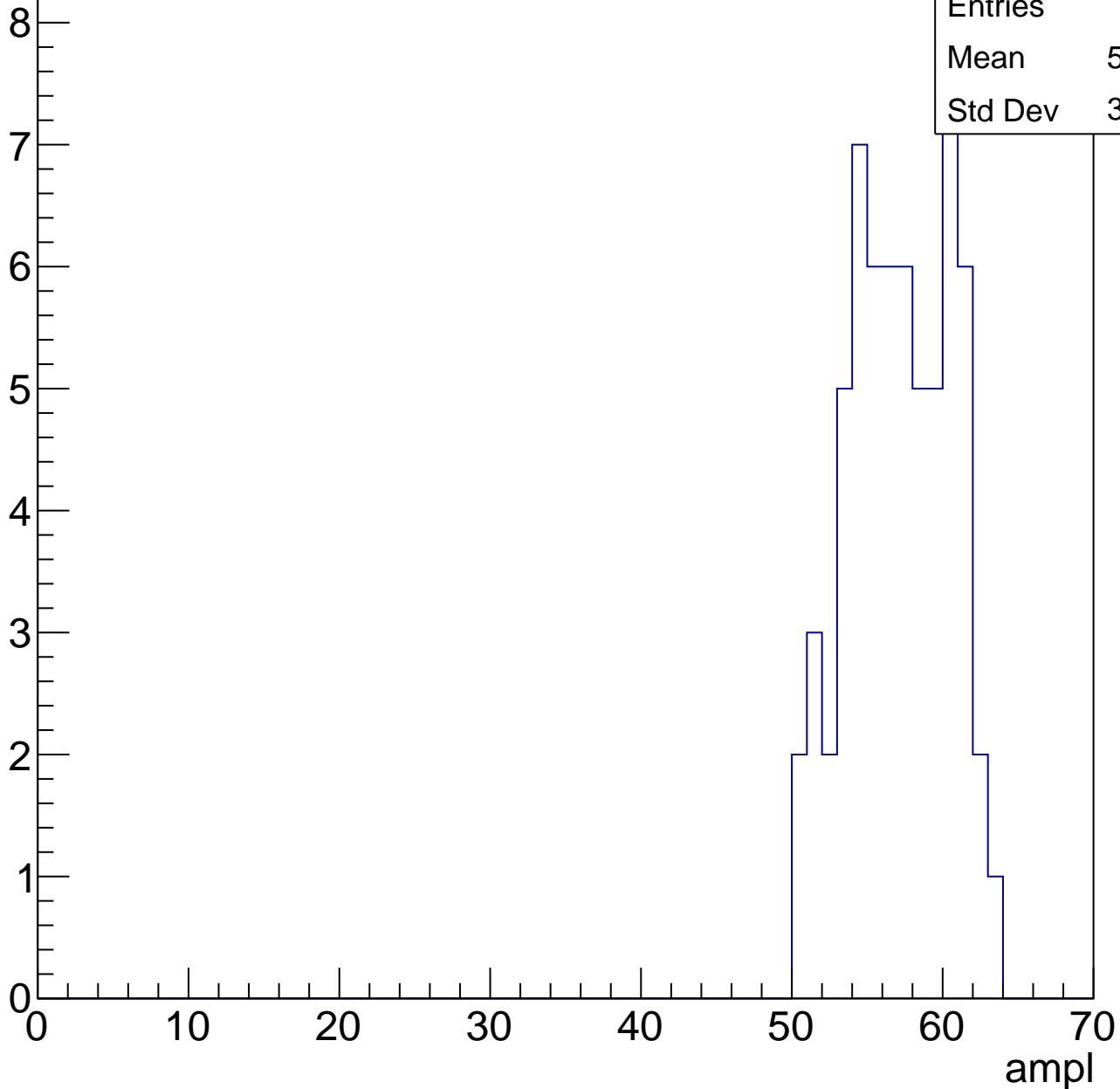


# B1L103S, U3-ch10, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	56.66
Std Dev	3.308

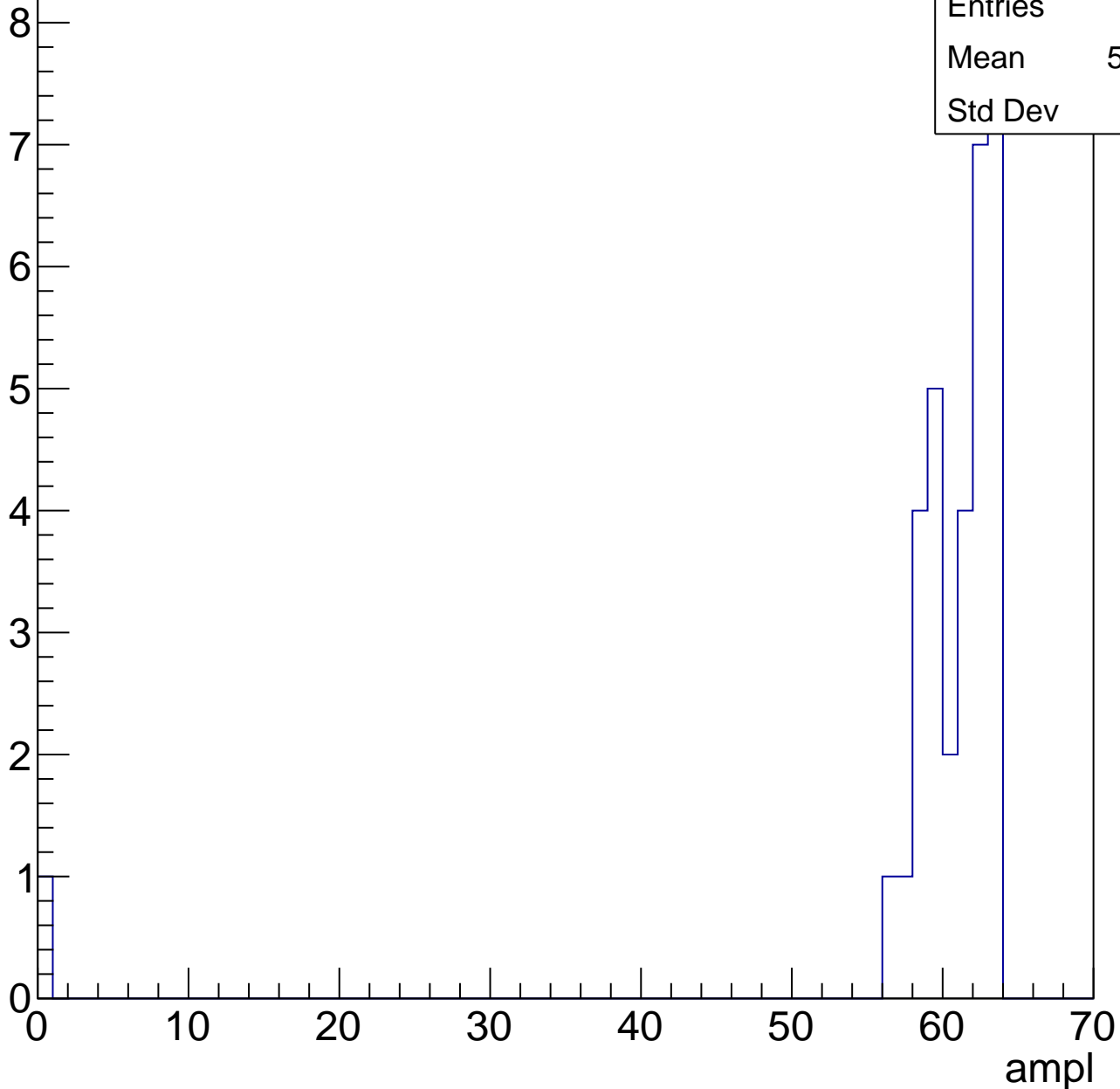


# B1L103S, U3-ch10, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	33
Mean	58.85
Std Dev	10.6





# B1L103S, U3-ch10, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	5.952
Std Dev	18.35

Entry



# B1L103S, U3-ch11, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	77
Mean	24.57
Std Dev	12.53

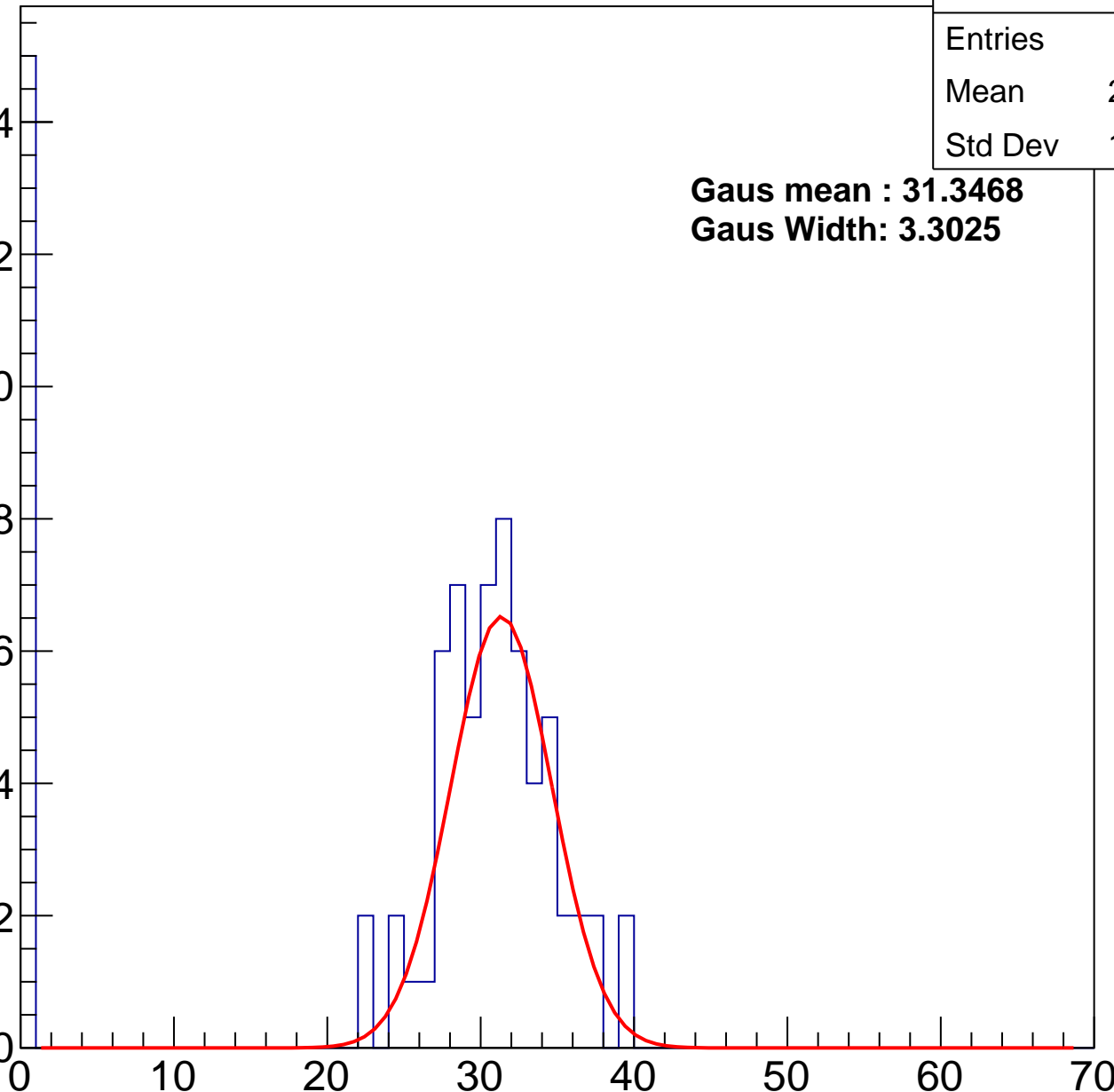
**Gaus mean : 31.3468**

**Gaus Width: 3.3025**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U3-ch11, adc1

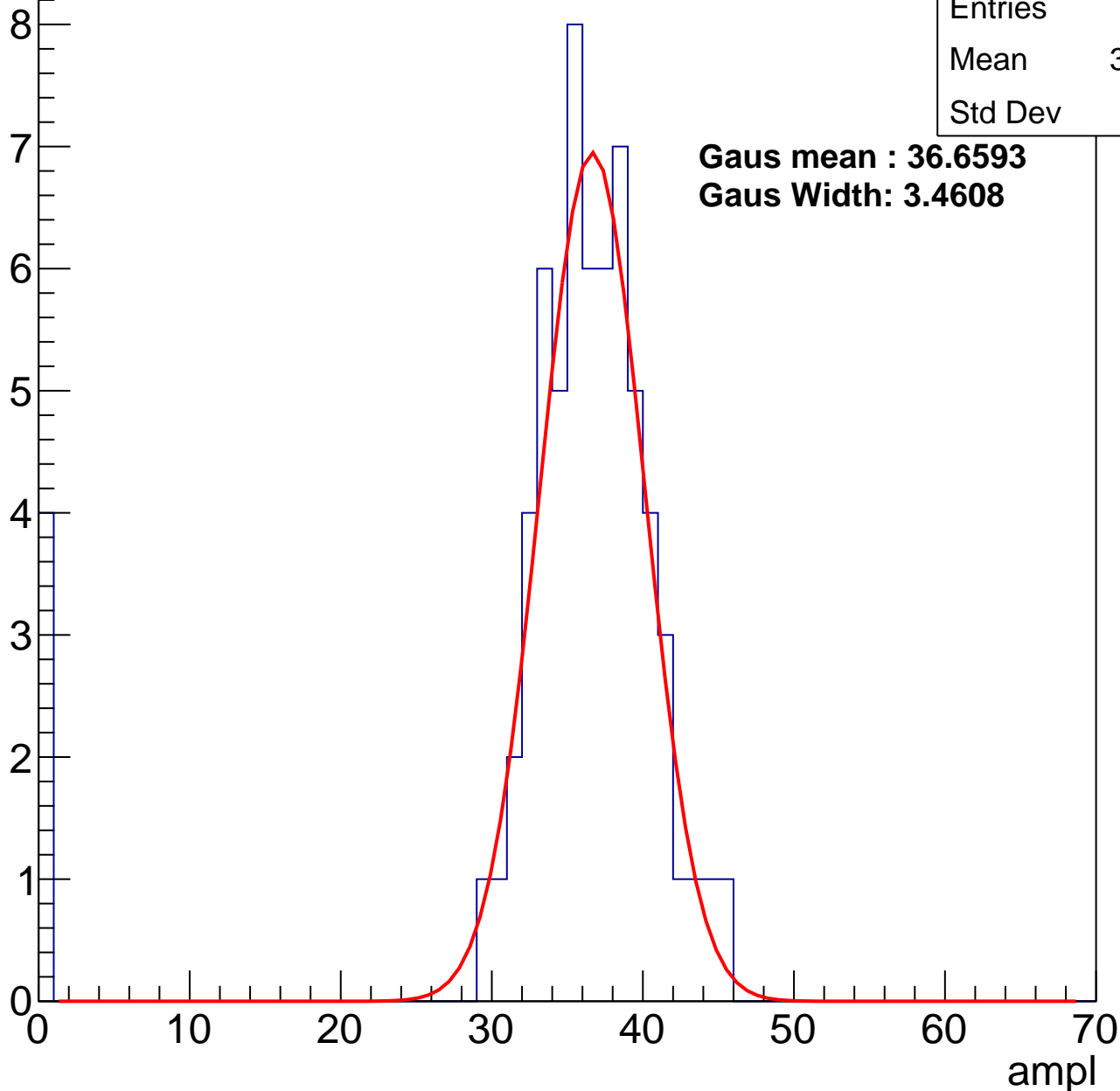
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	34.14
Std Dev	9.28

**Gaus mean : 36.6593**

**Gaus Width: 3.4608**



# B1L103S, U3-ch11, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	83
Mean	36.47
Std Dev	16.06

**Gaus mean : 43.4369**

**Gaus Width: 3.6350**

Entry

12

10

8

6

4

2

0

0

10

20

30

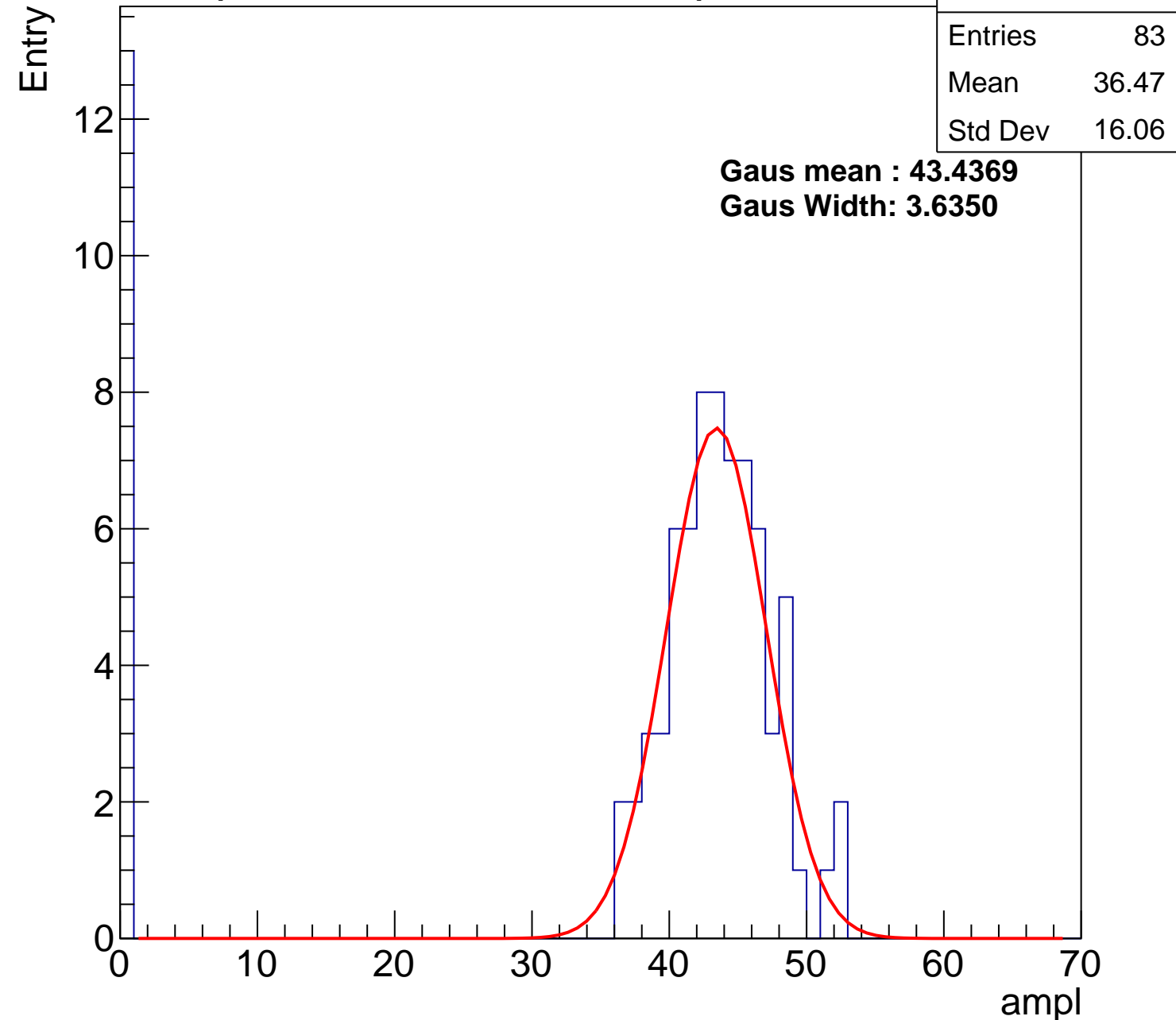
40

50

60

70

ampl

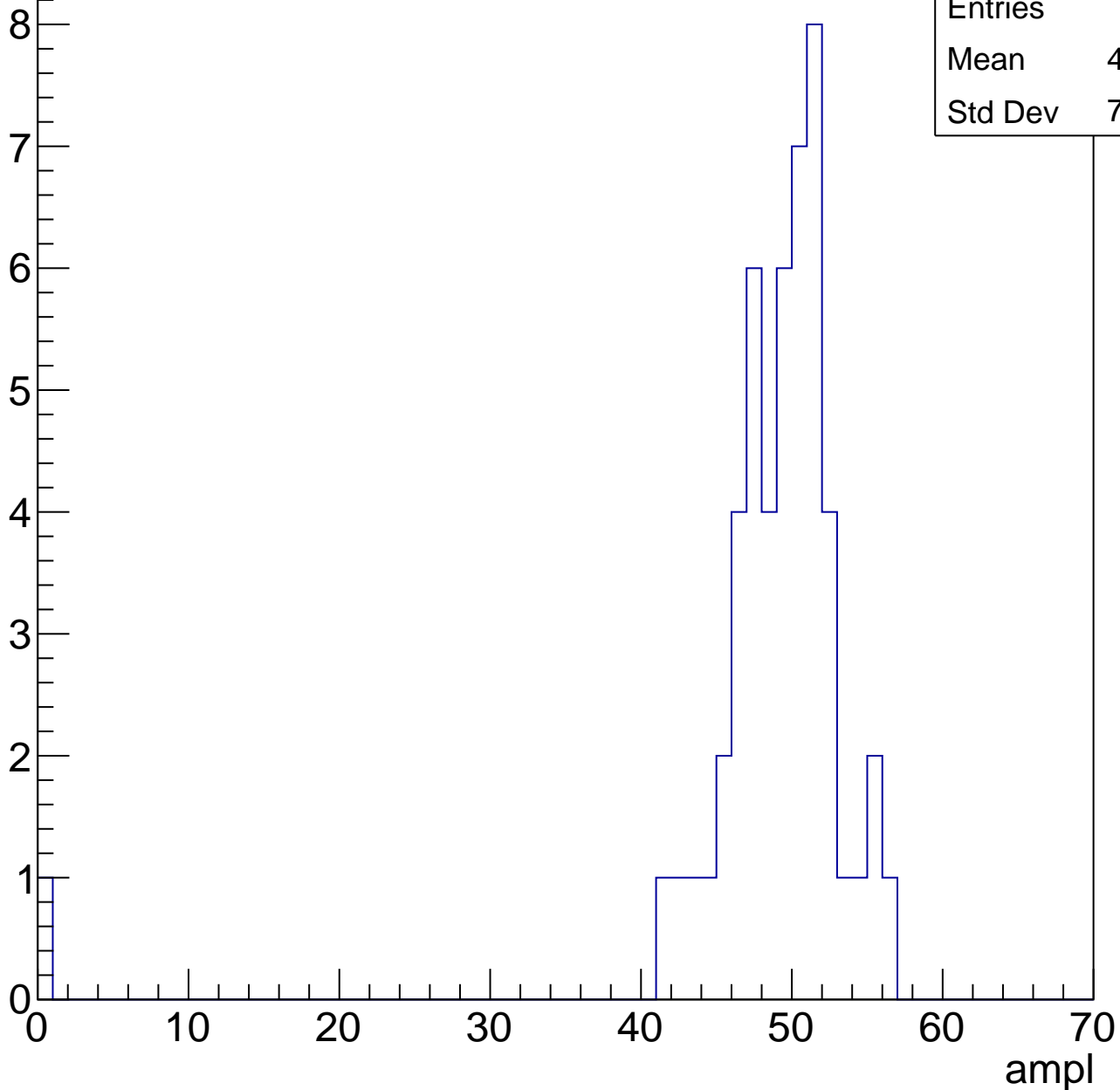


# B1L103S, U3-ch11, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	51
Mean	48.06
Std Dev	7.492

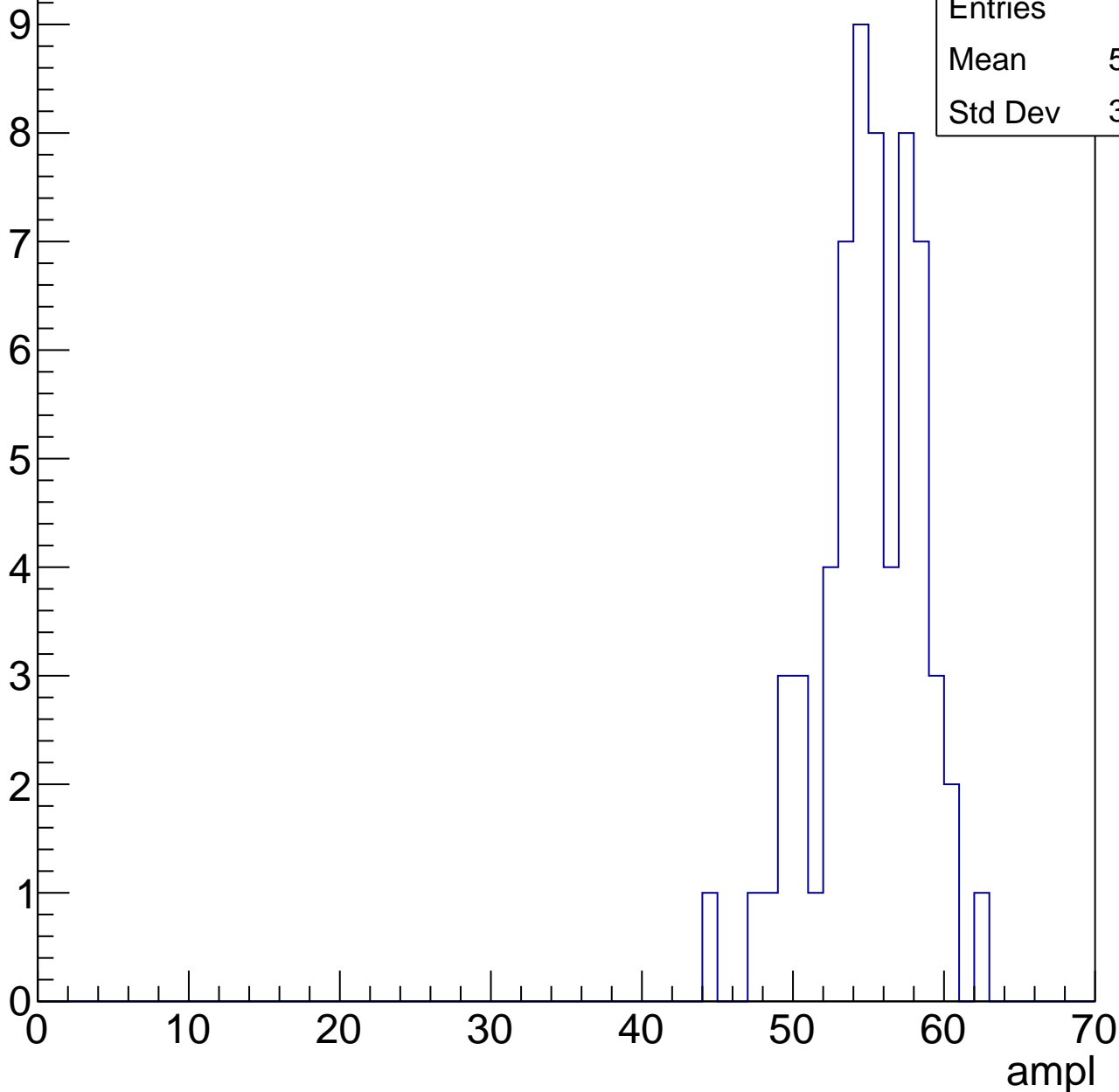


# B1L103S, U3-ch11, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	54.56
Std Dev	3.426



# B1L103S, U3-ch11, adc5

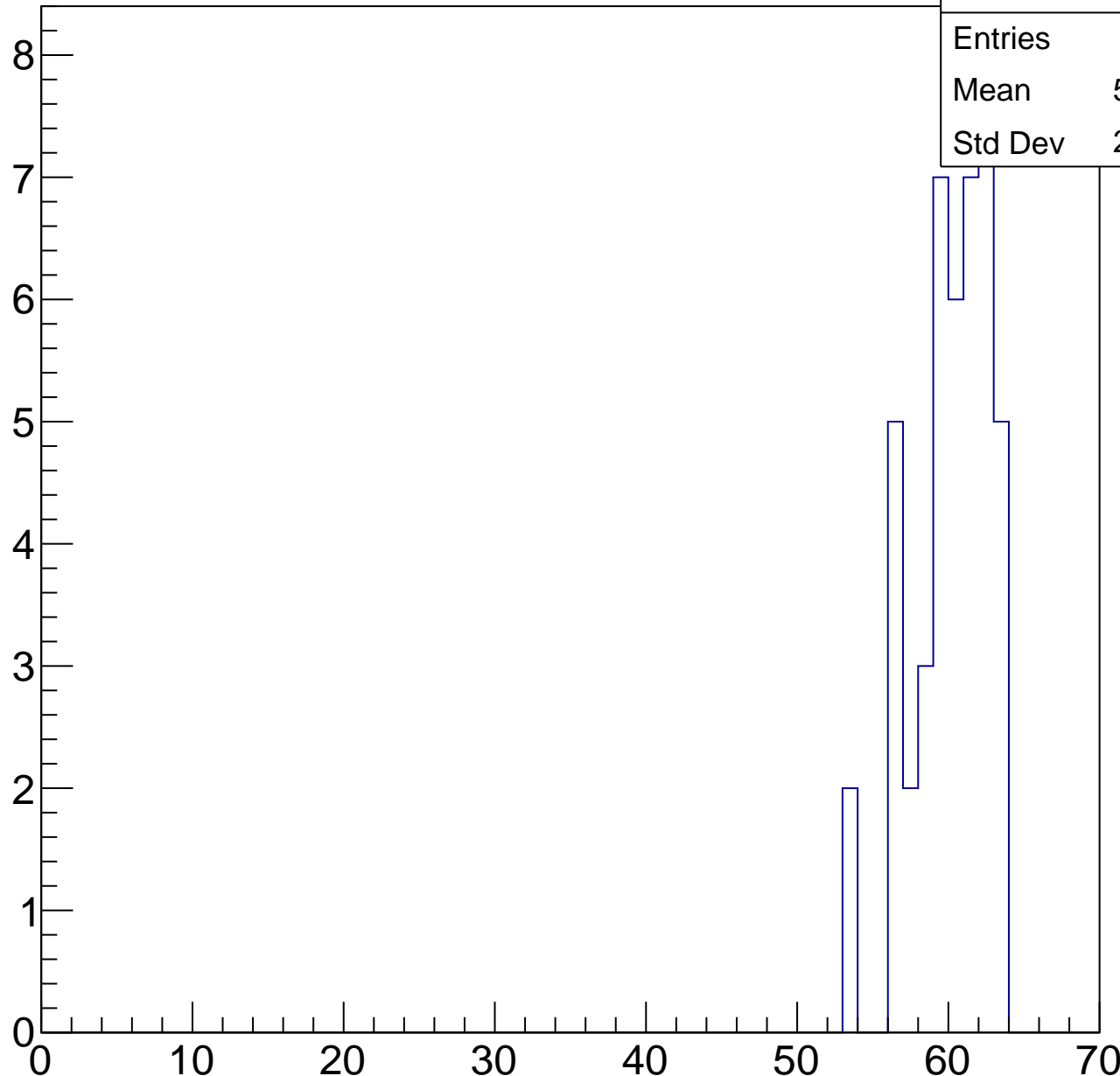
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	45
Mean	59.67
Std Dev	2.556

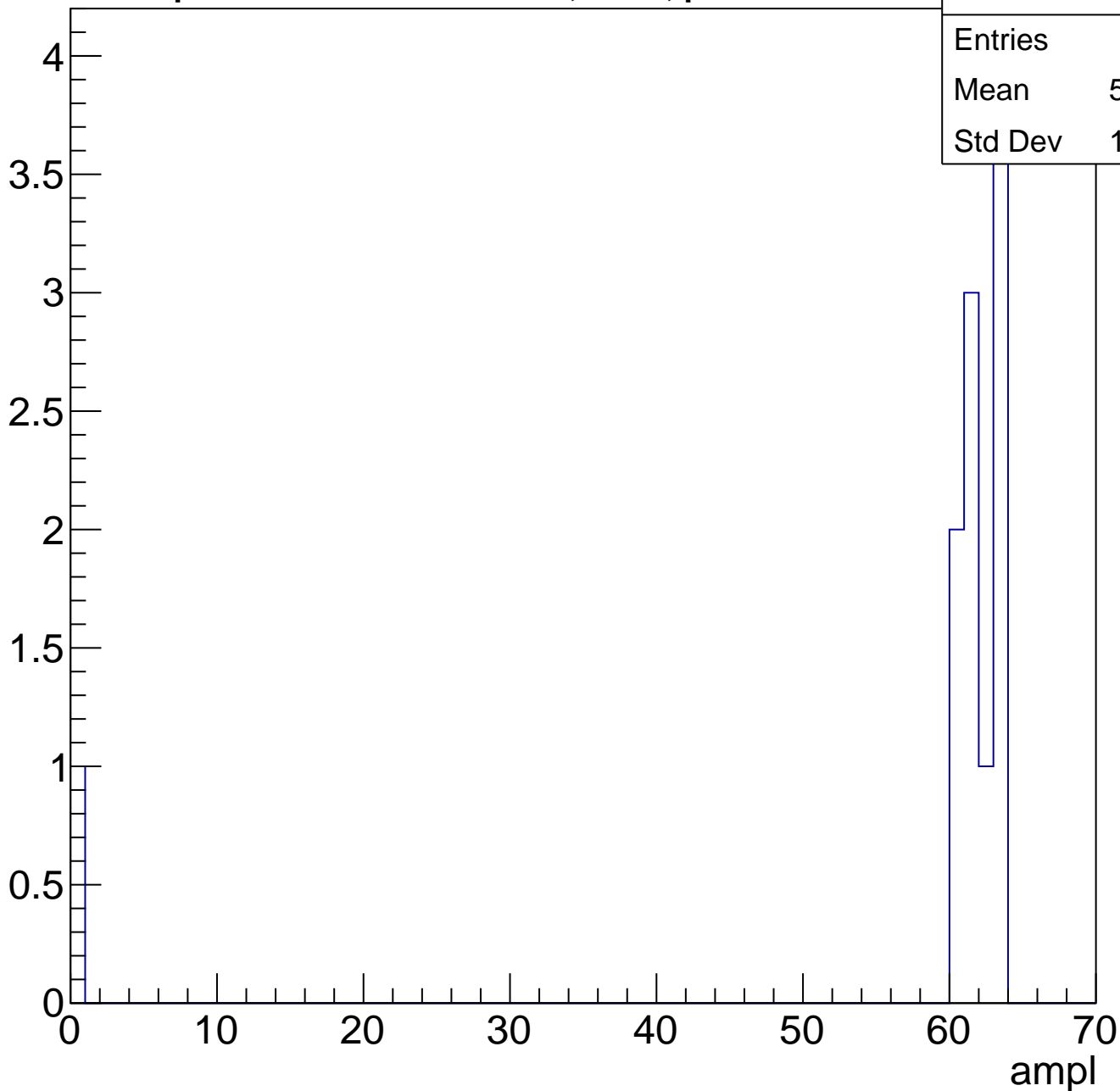
ampl



# B1L103S, U3-ch11, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

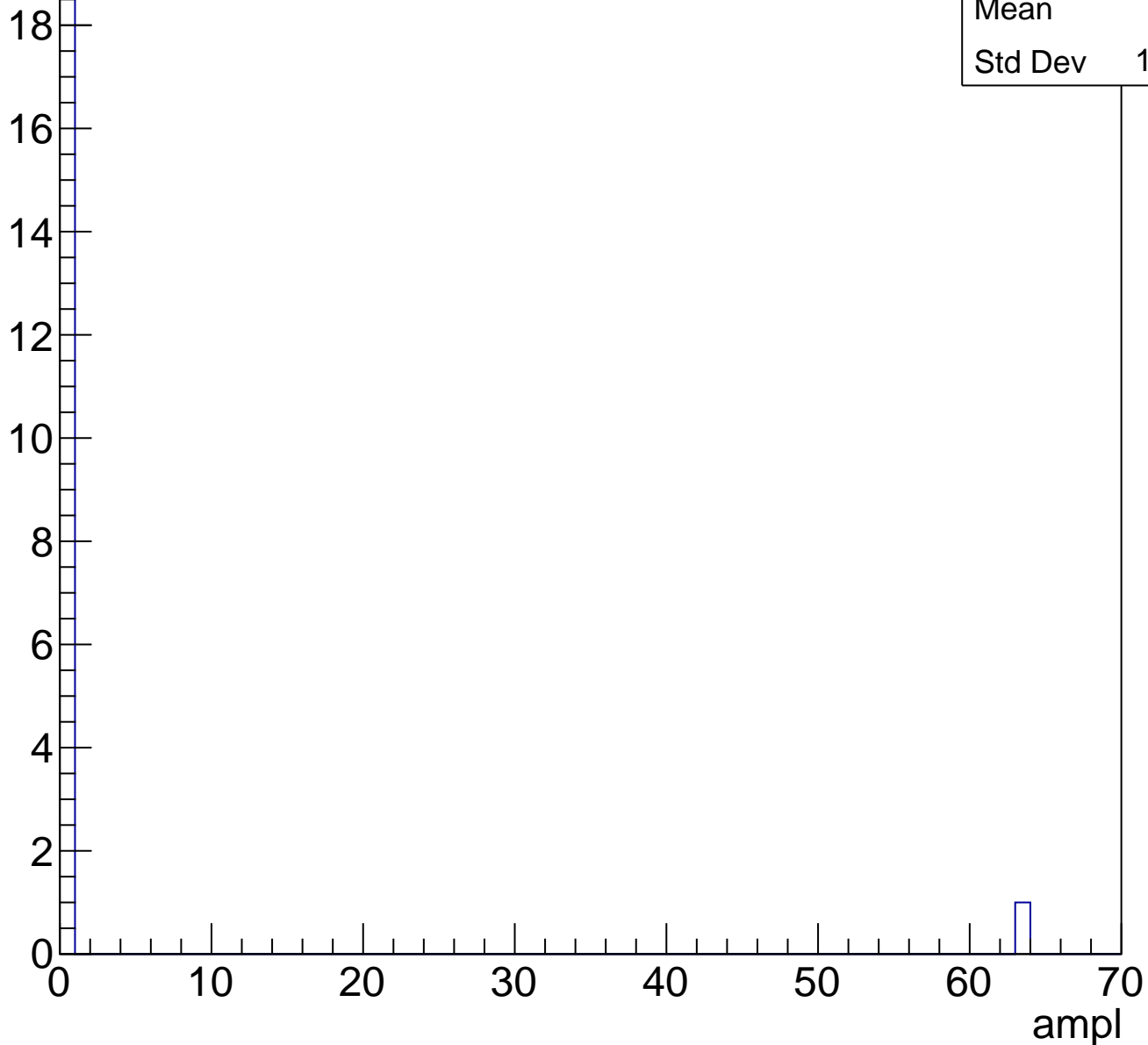




# B1L103S, U3-ch11, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U3-ch12, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	95
Mean	23.44
Std Dev	10.38

**Gaus mean : 28.1030**

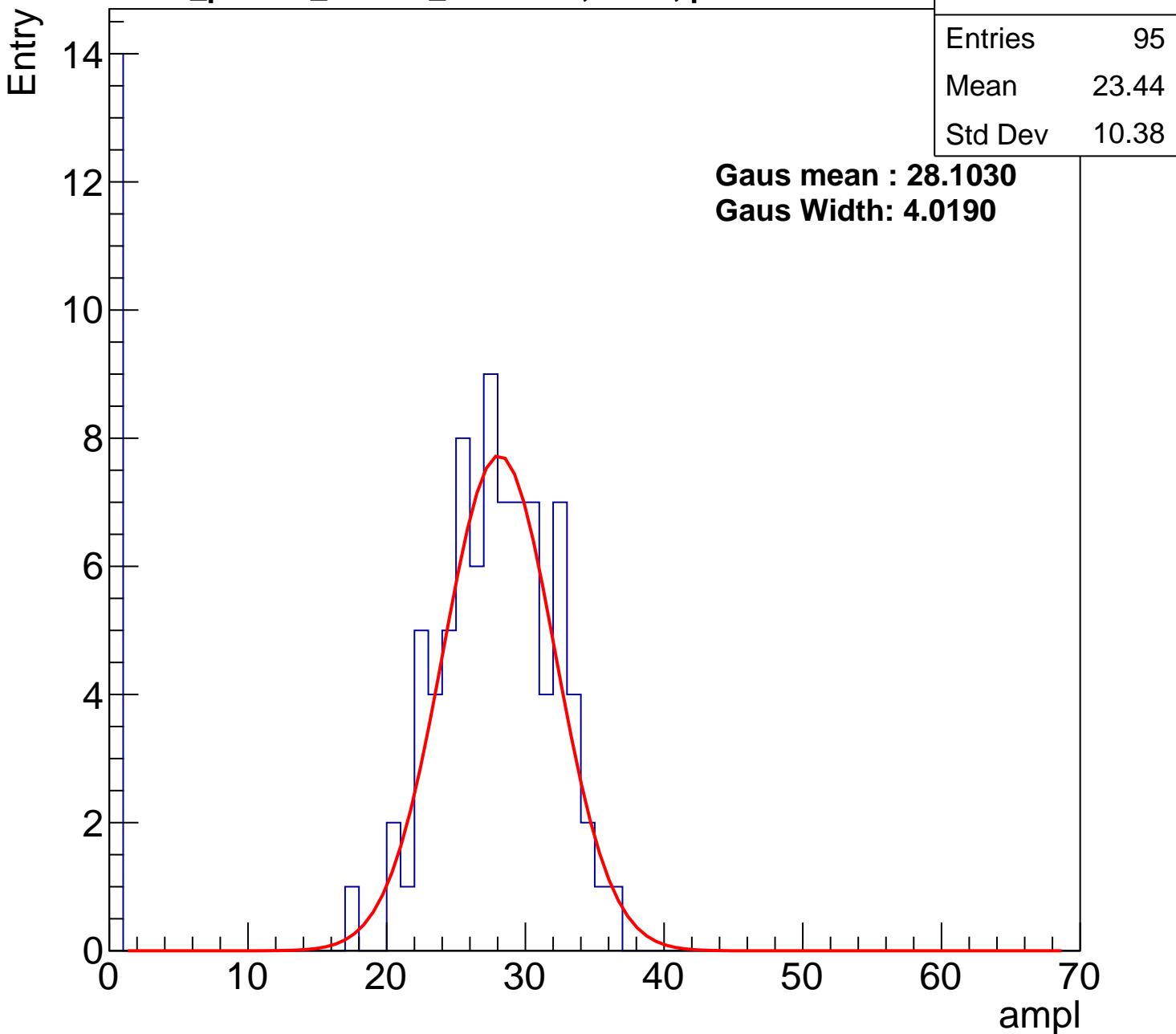
**Gaus Width: 4.0190**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch12, adc1

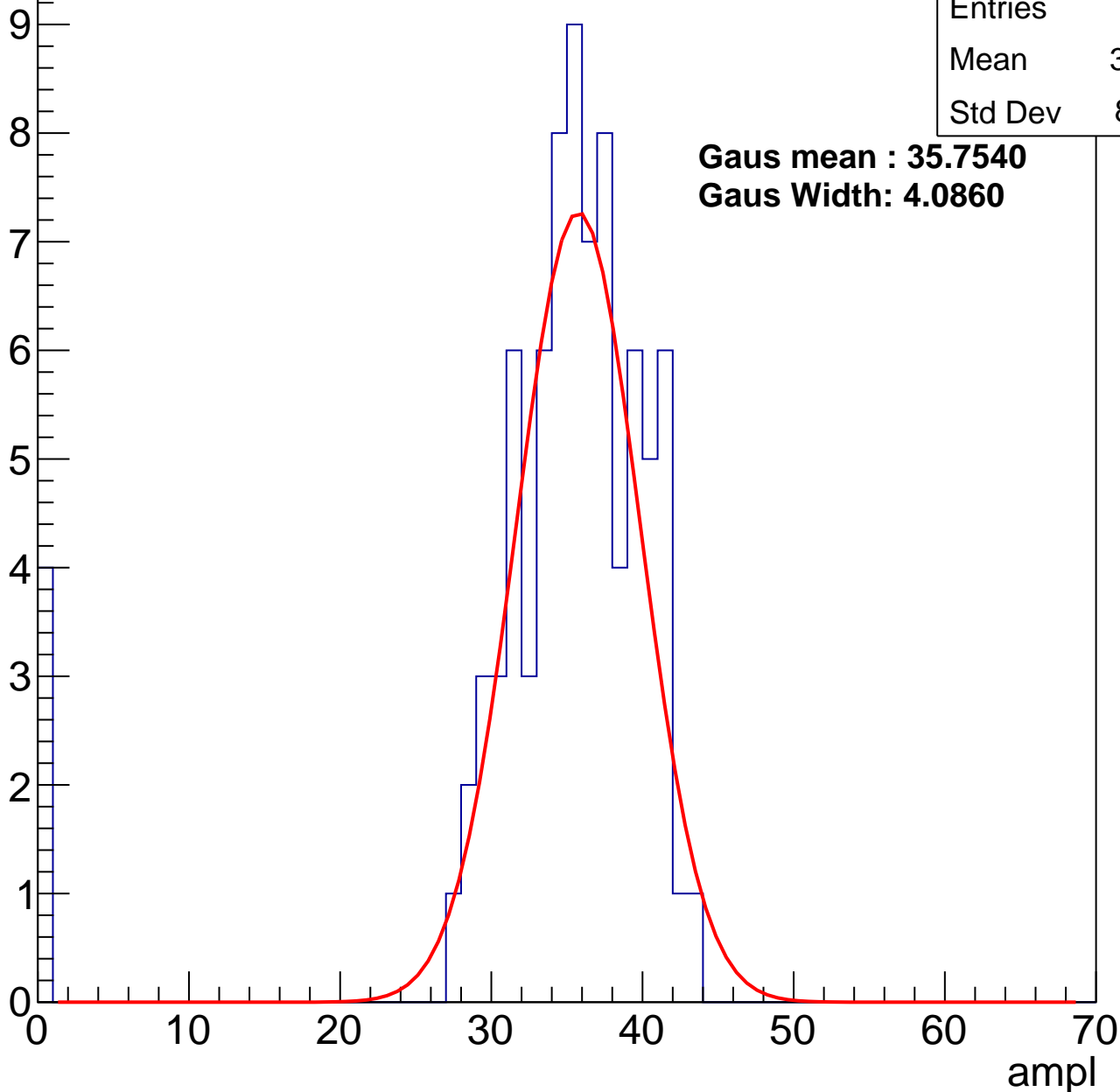
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	83
Mean	33.64
Std Dev	8.411

**Gaus mean : 35.7540**

**Gaus Width: 4.0860**



# B1L103S, U3-ch12, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	64
Mean	34.95
Std Dev	16.25

**Gaus mean : 42.1552**

**Gaus Width: 4.4714**

Entry

10

8

6

4

2

0

0

10

20

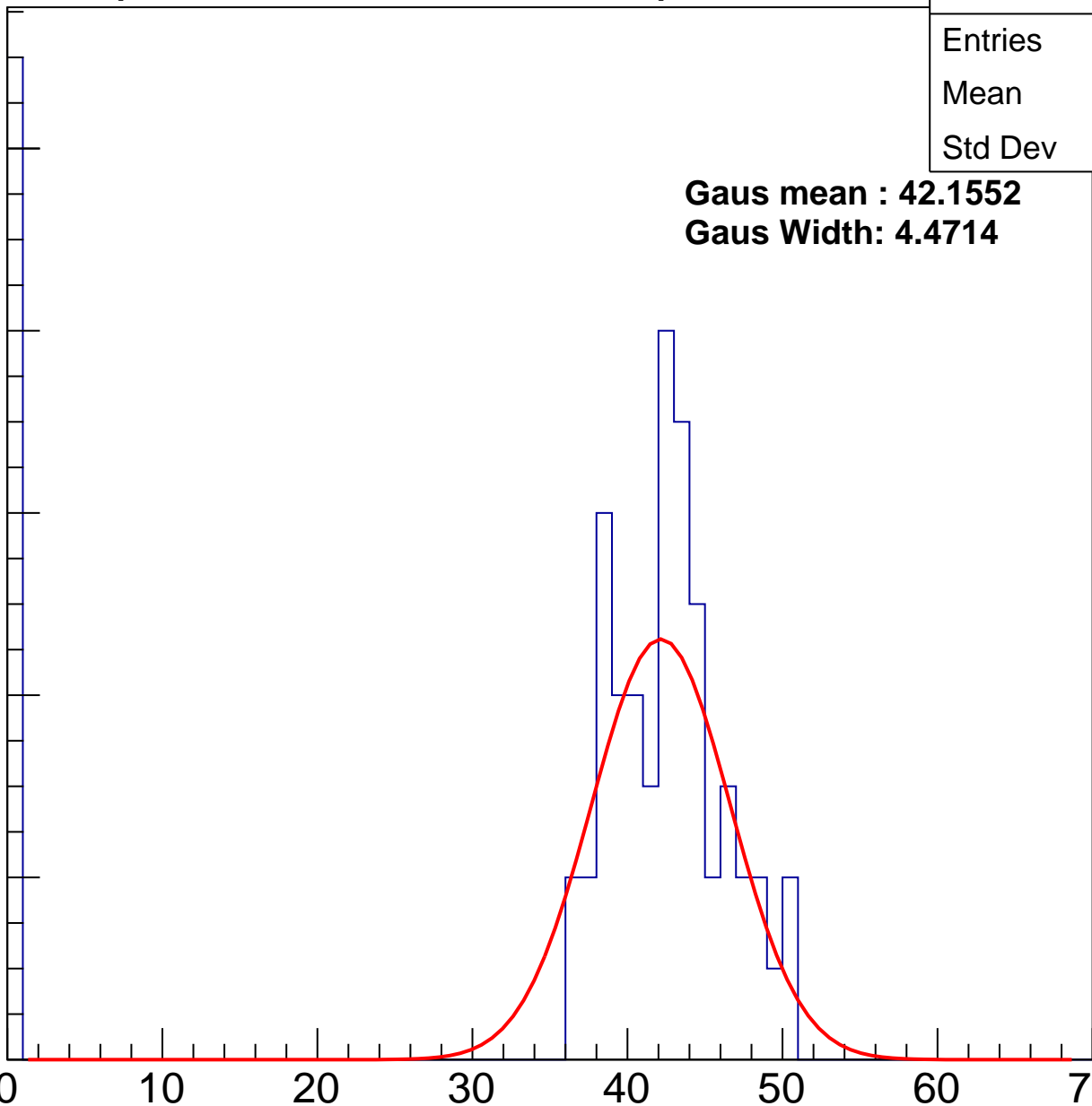
30

40

50

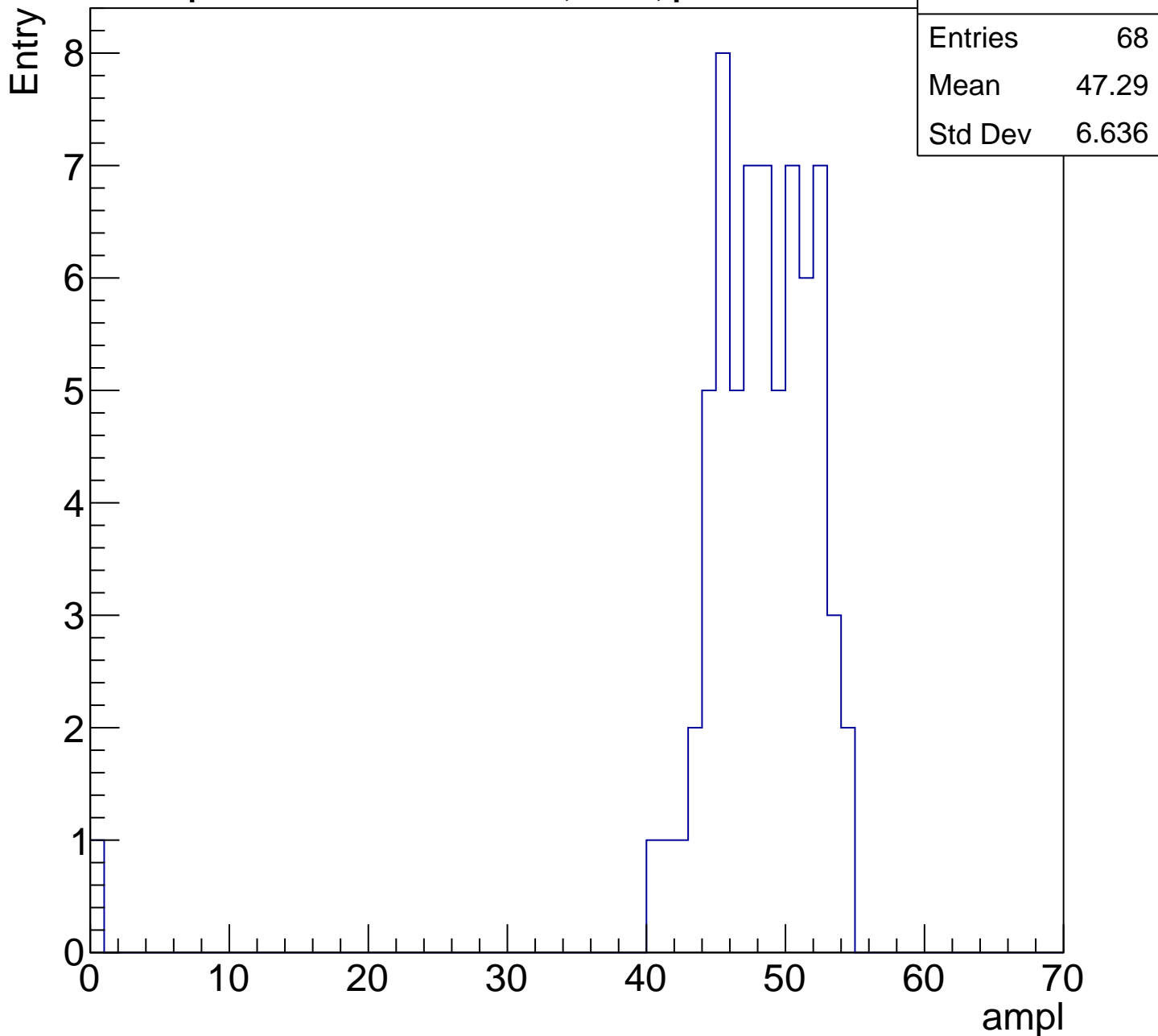
60

ampl



# B1L103S, U3-ch12, adc3

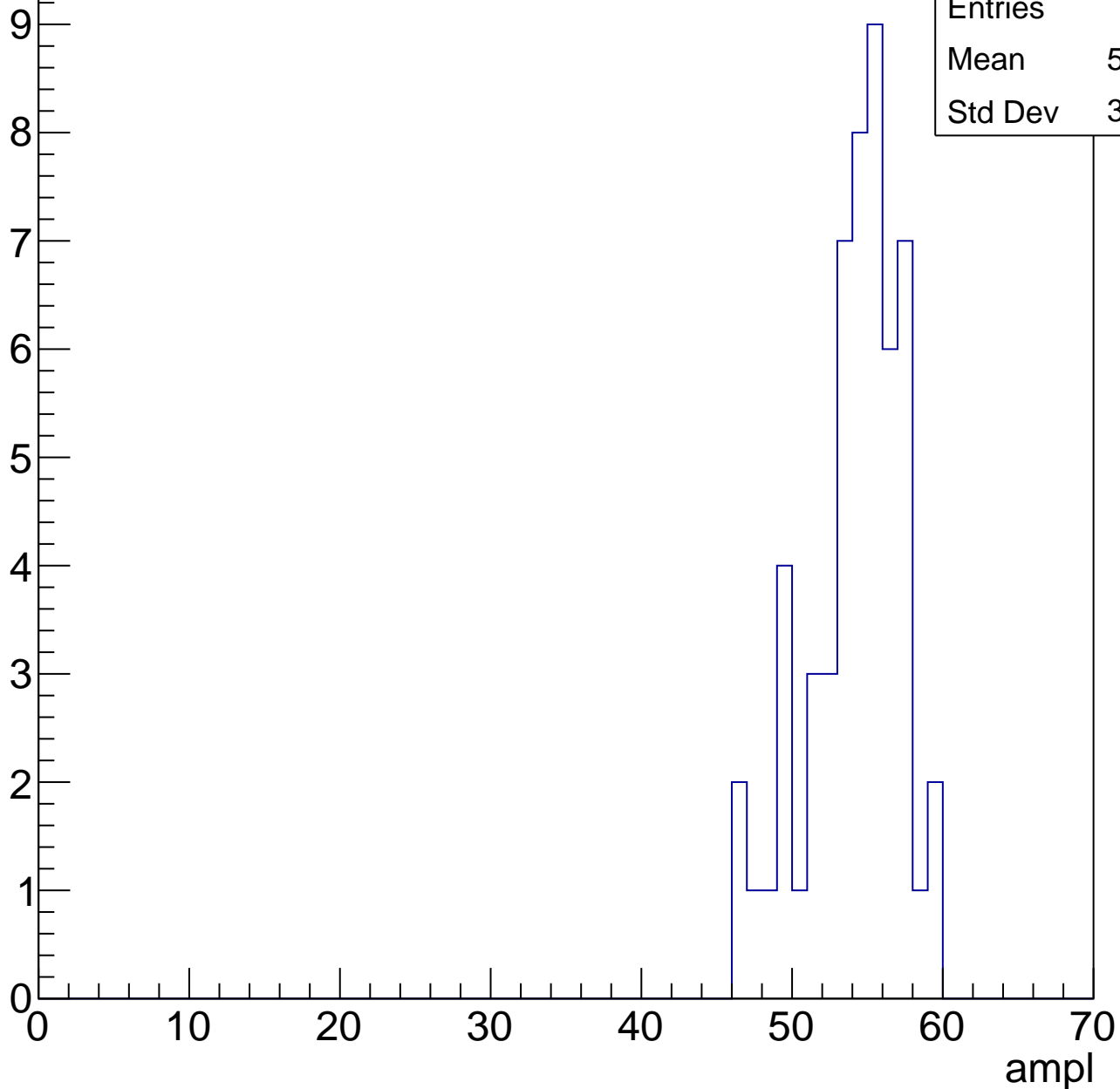
calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U3-ch12, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



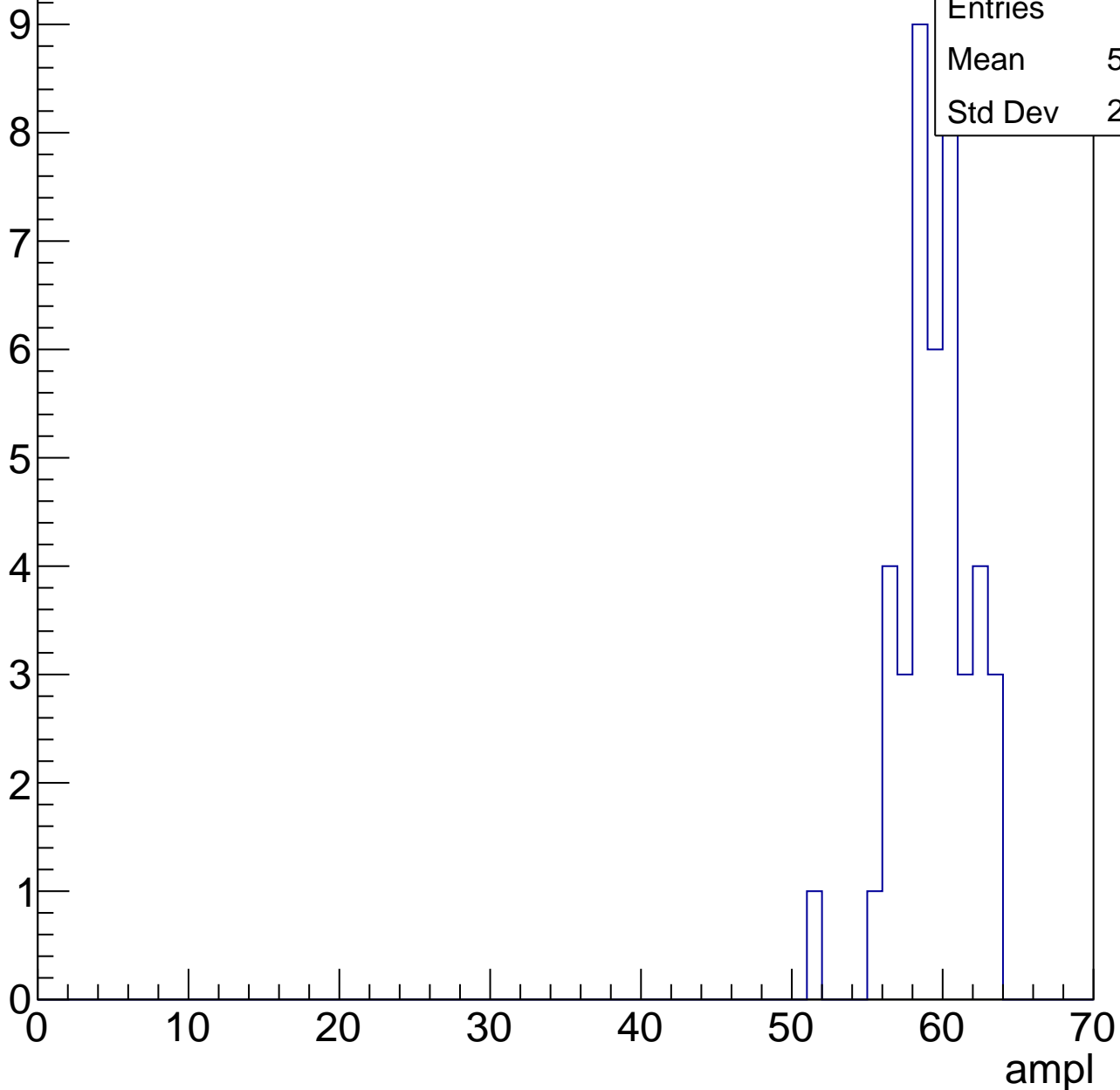
Entries	55
Mean	53.65
Std Dev	3.106

# B1L103S, U3-ch12, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

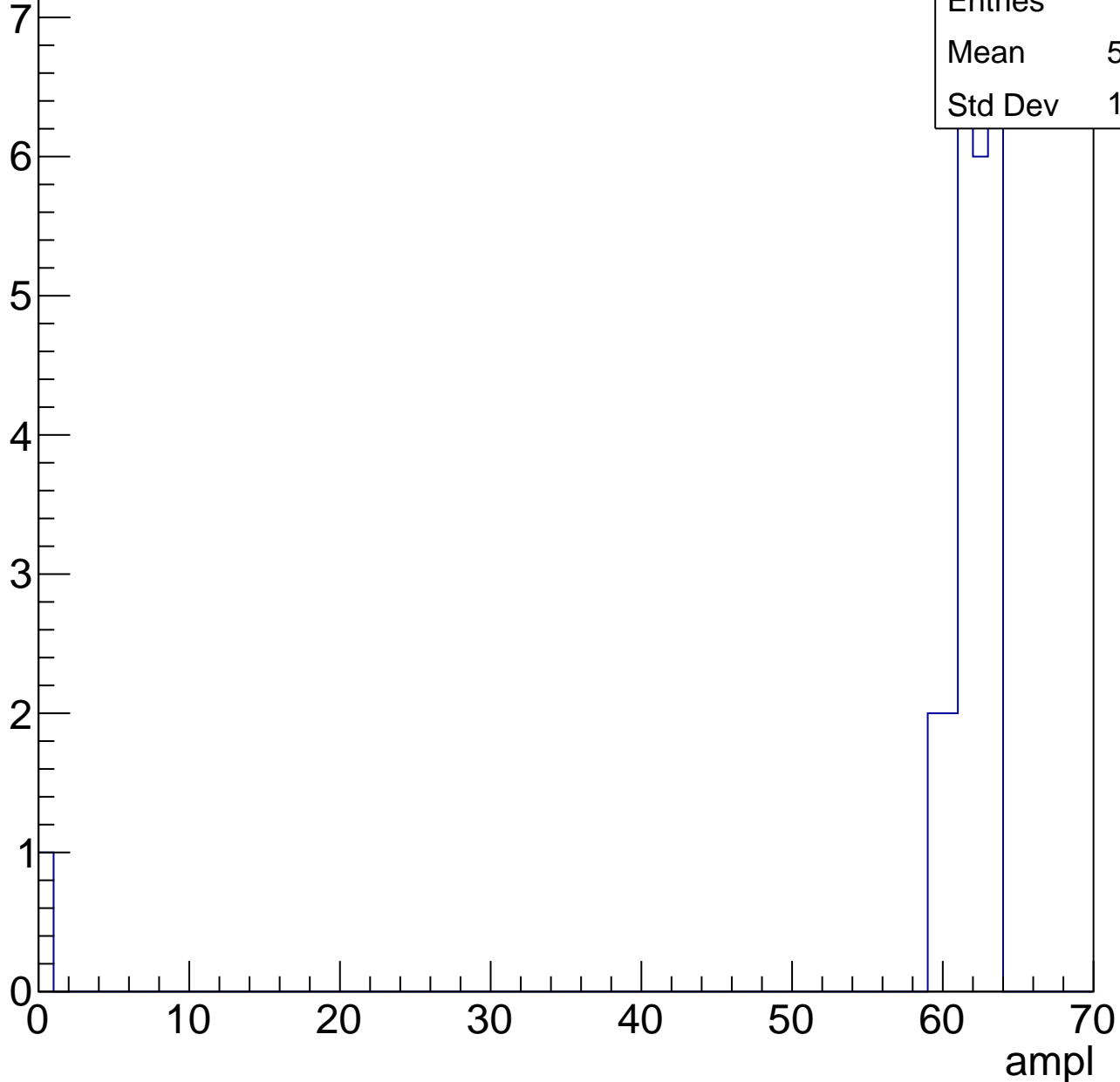
Entries	42
Mean	58.98
Std Dev	2.395



# B1L103S, U3-ch12, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U3-ch12, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U3-ch13, adc0

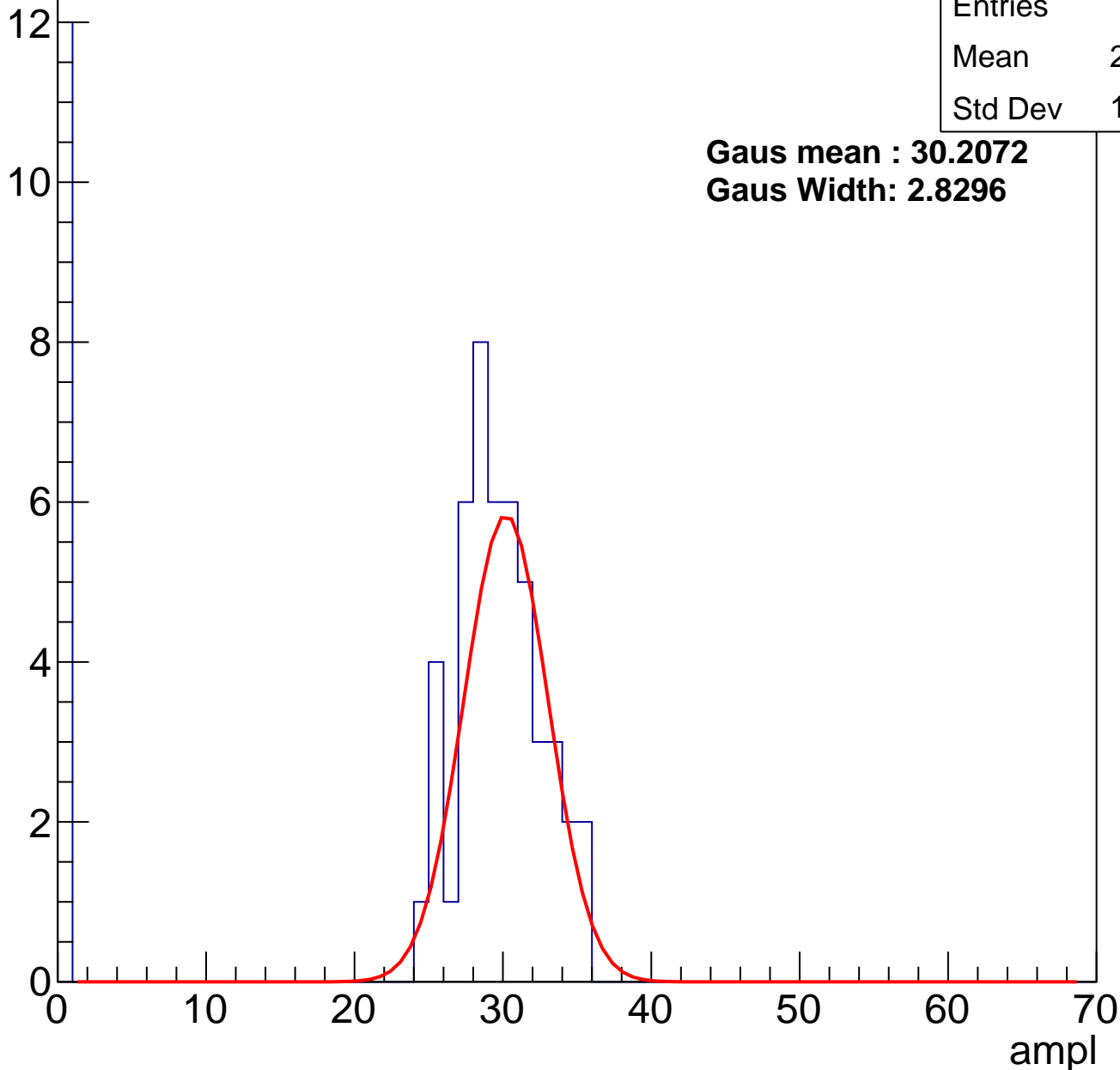
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	59
Mean	23.36
Std Dev	12.05

**Gaus mean : 30.2072**

**Gaus Width: 2.8296**

Entry



# B1L103S, U3-ch13, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	79
Mean	34.99
Std Dev	5.352

**Gaus mean : 36.0327**

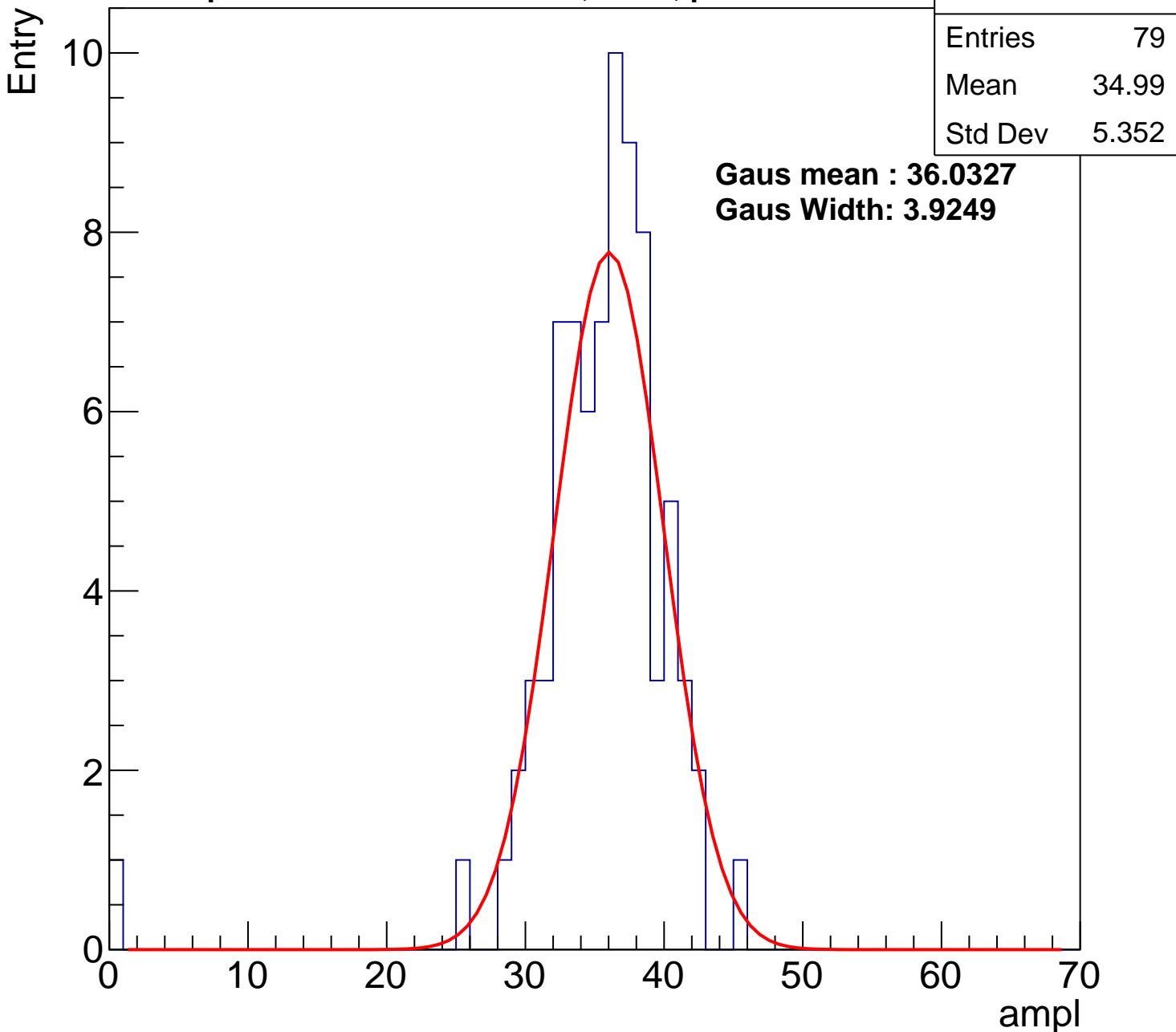
**Gaus Width: 3.9249**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U3-ch13, adc2

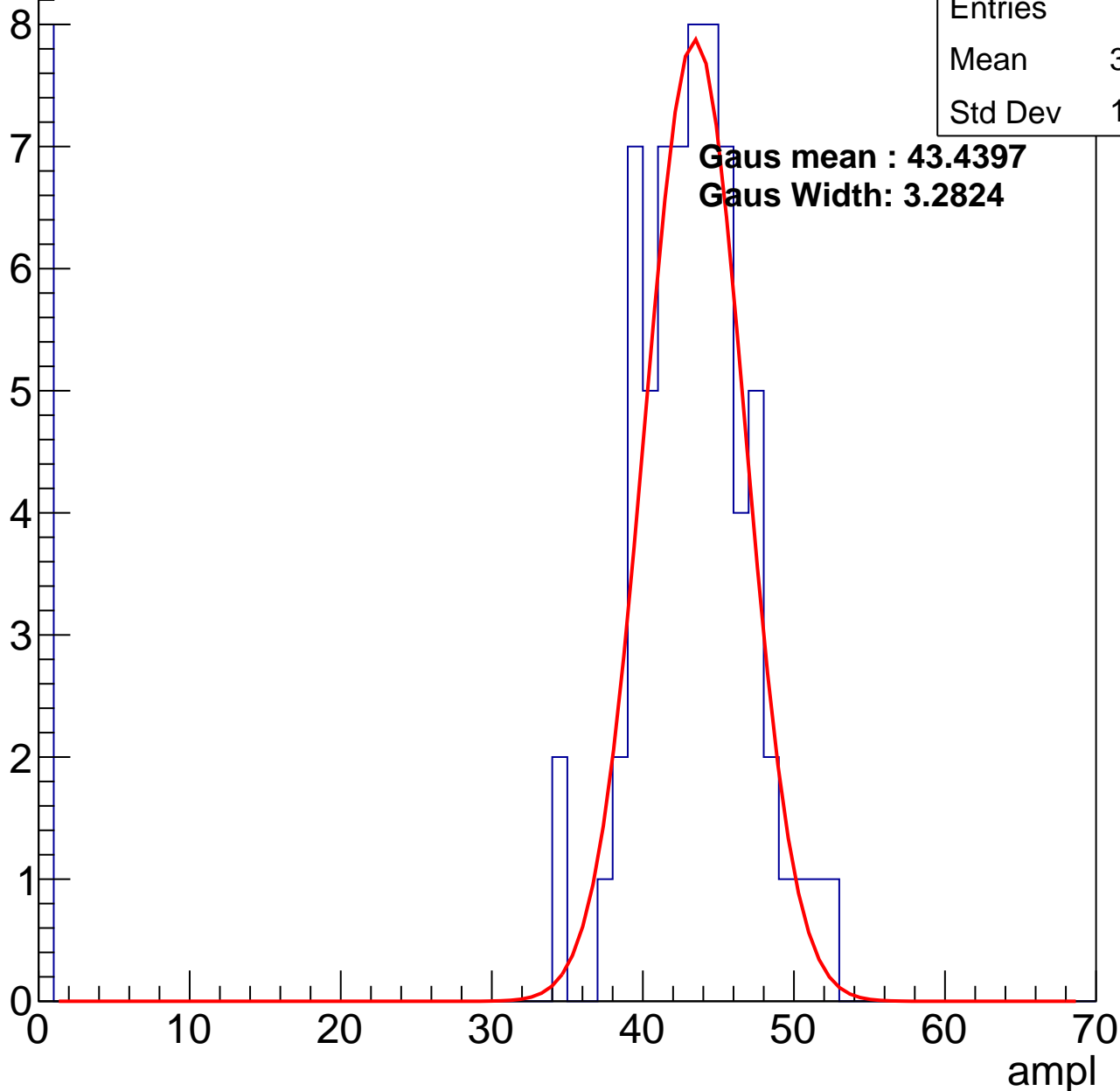
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	77
Mean	38.48
Std Dev	13.53

**Gaus mean : 43.4397**

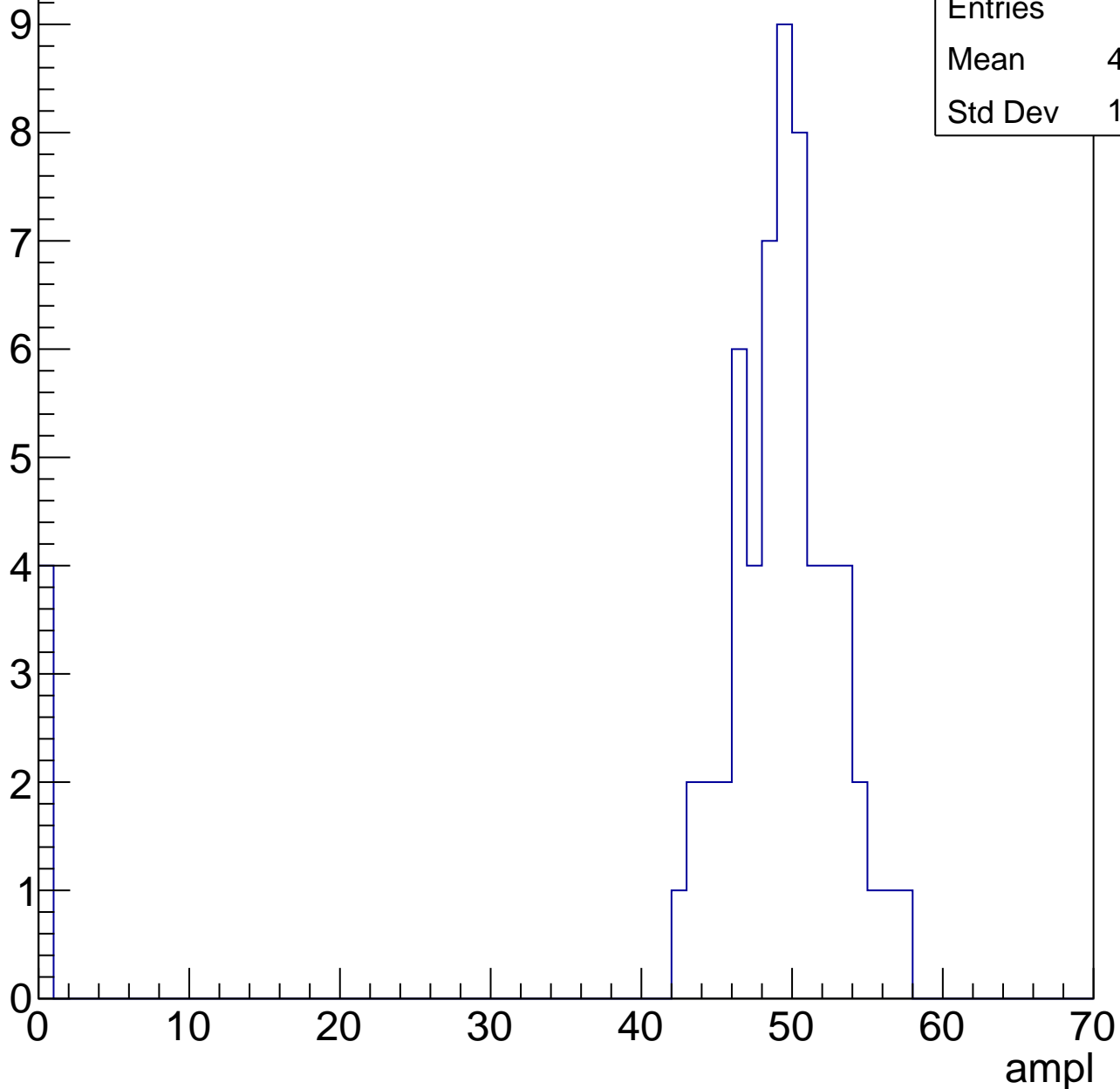
**Gaus Width: 3.2824**



# B1L103S, U3-ch13, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

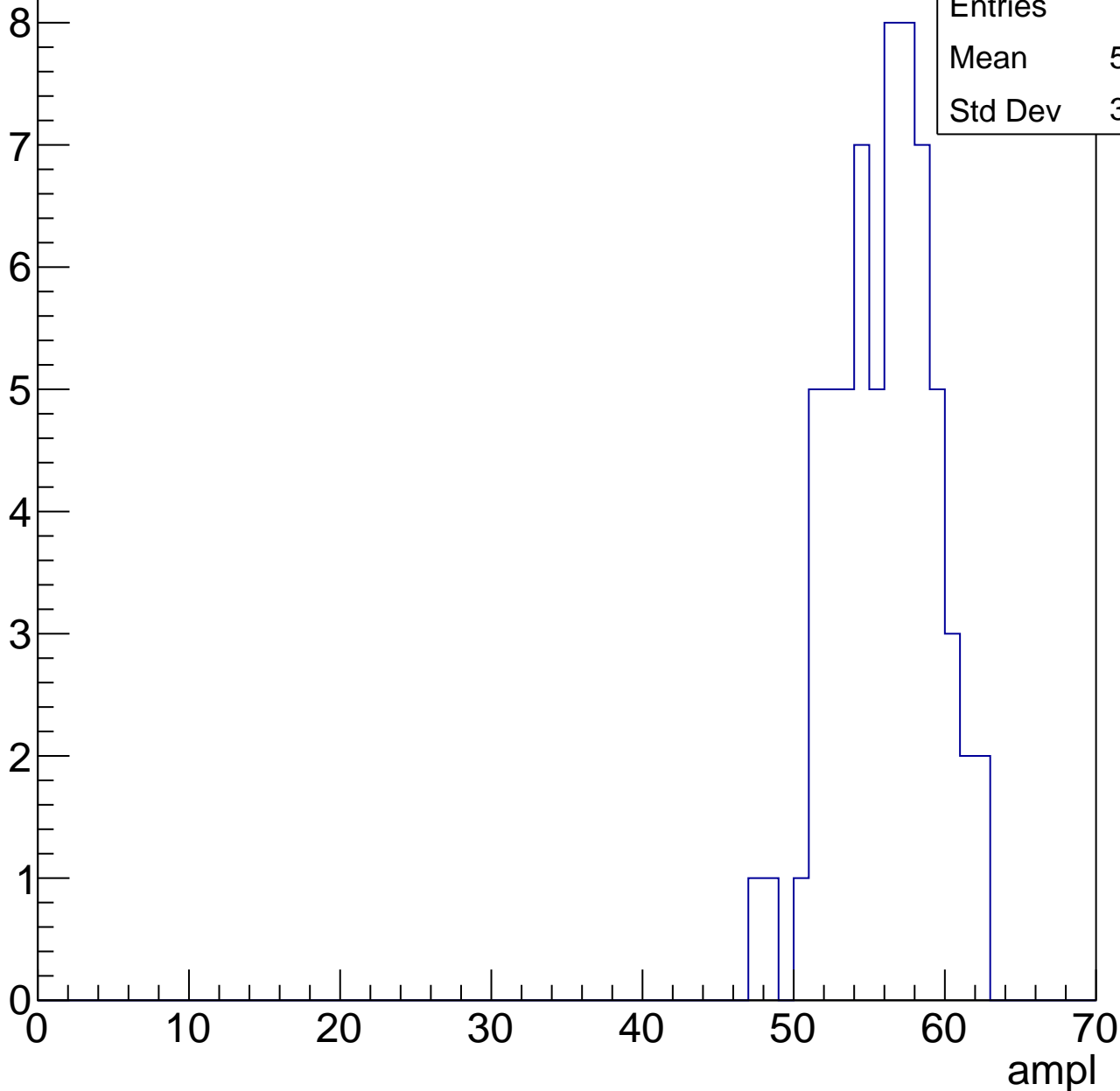


# B1L103S, U3-ch13, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	65
Mean	55.52
Std Dev	3.282

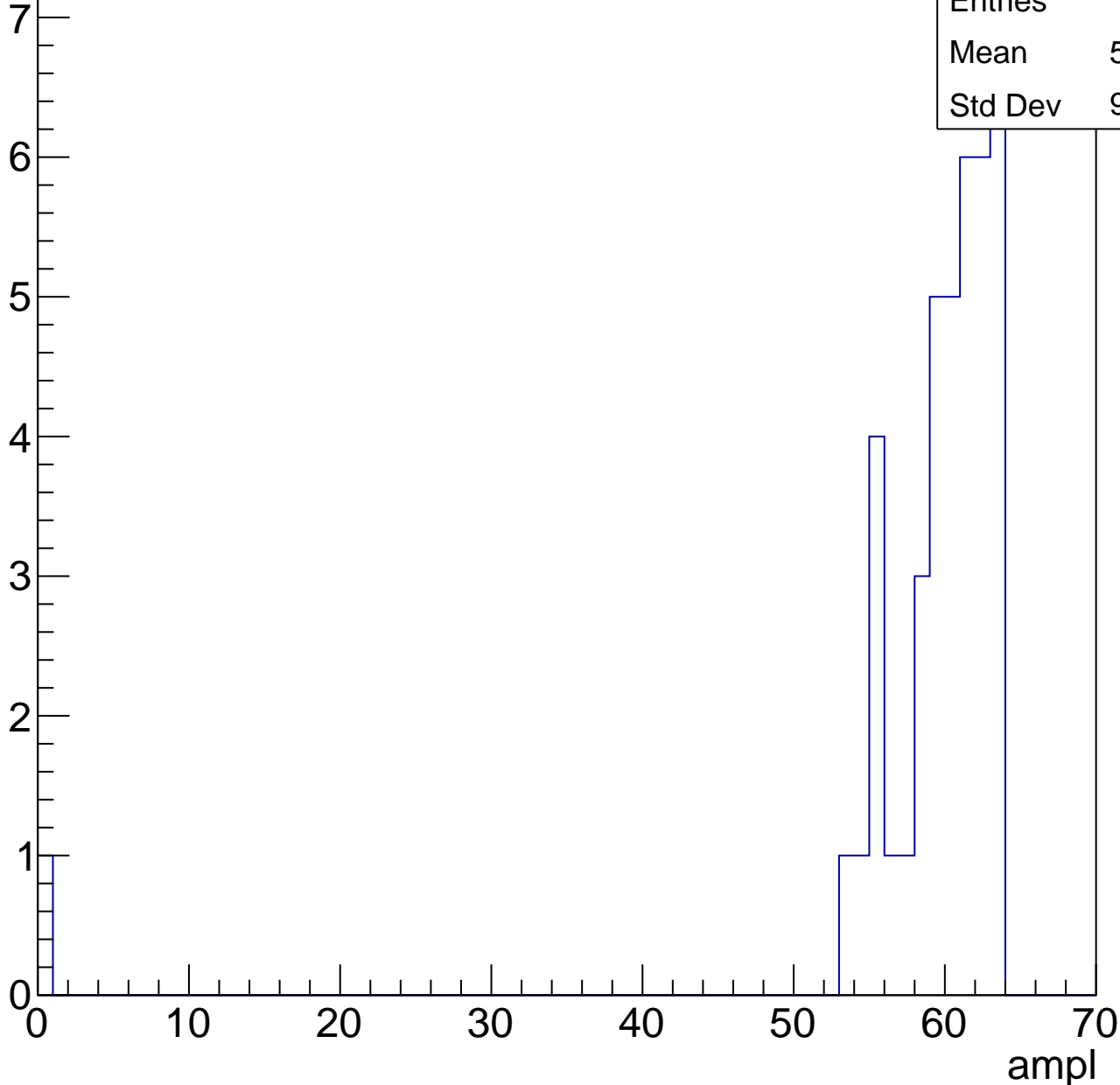


# B1L103S, U3-ch13, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

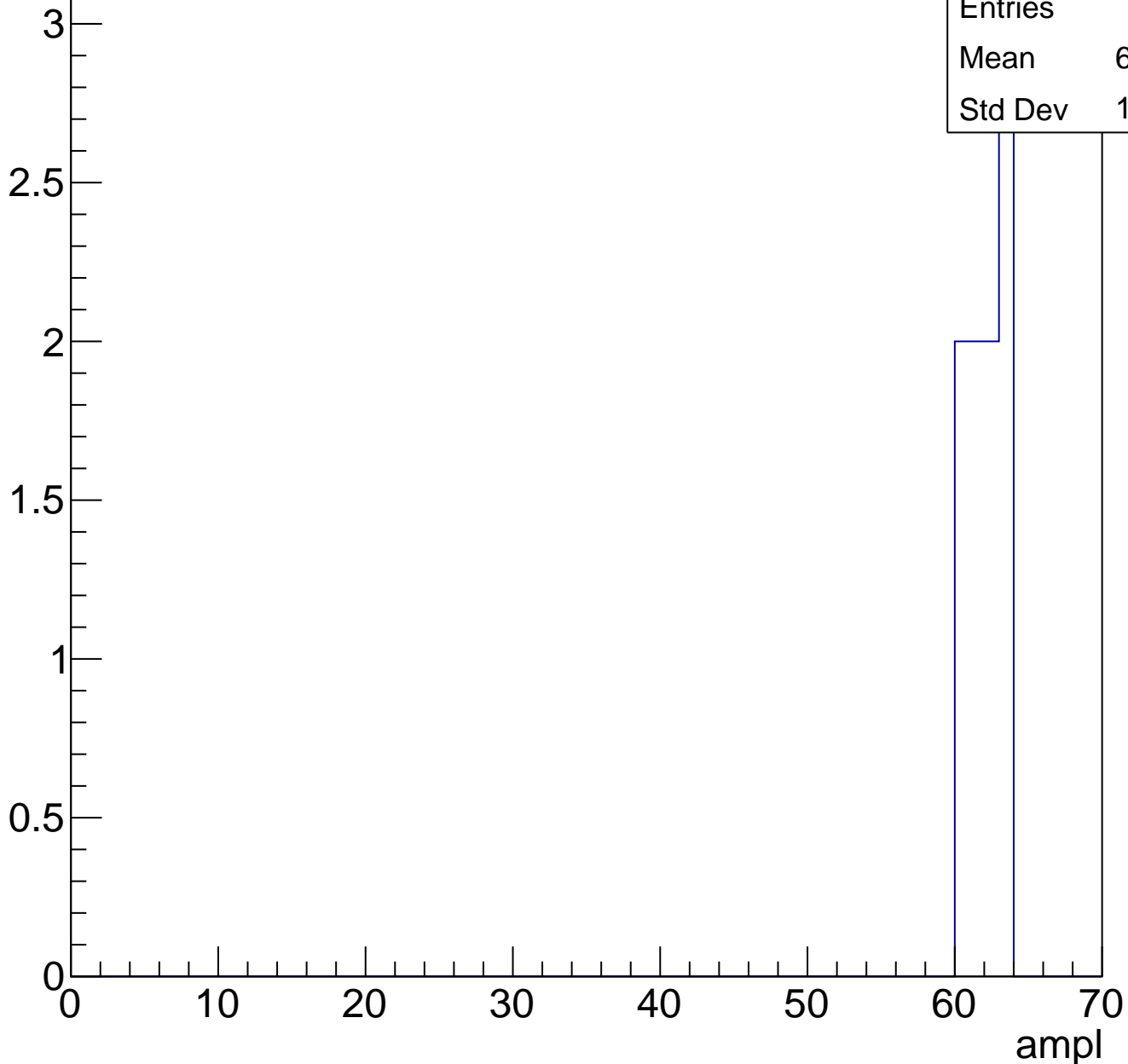
Entries	41
Mean	58.24
Std Dev	9.619



# B1L103S, U3-ch13, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U3-ch13, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U3-ch14, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	77
Mean	24.42
Std Dev	11.44

**Gaus mean : 29.5734**

**Gaus Width: 4.1580**

Entry

12

10

8

6

4

2

0

0

10

20

30

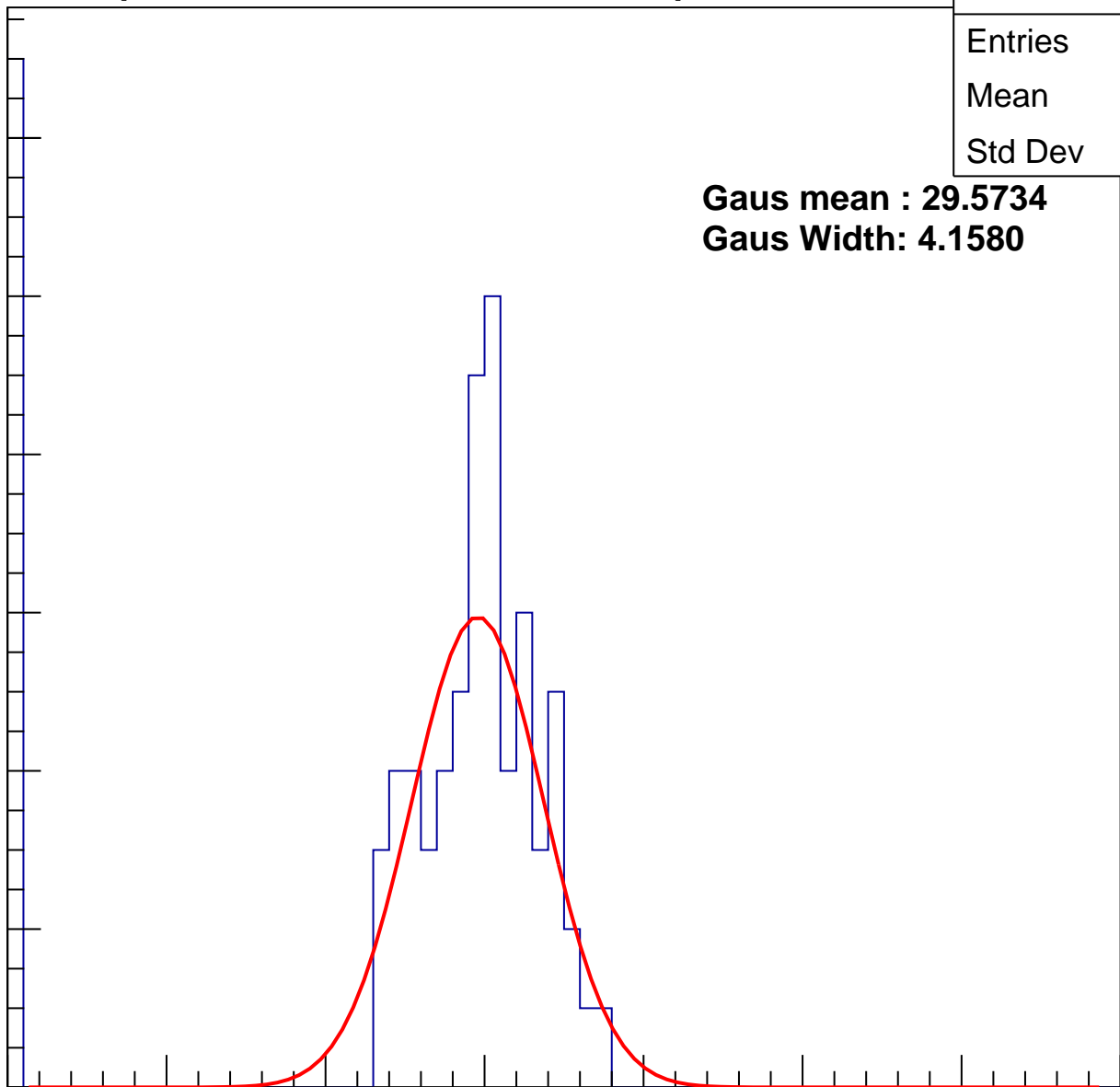
40

50

60

70

ampl



# B1L103S, U3-ch14, adc1

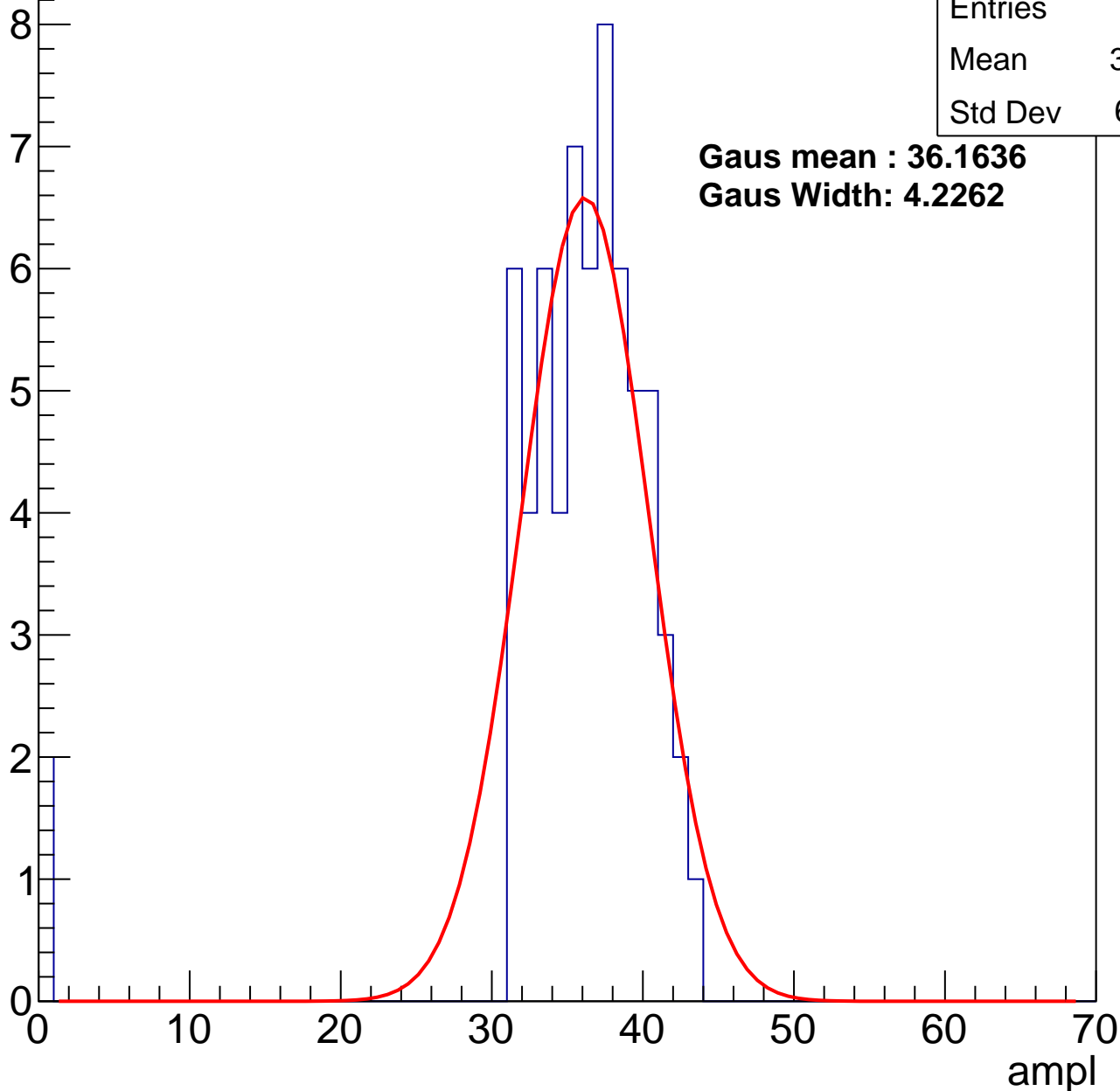
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	65
Mean	35.05
Std Dev	6.991

**Gaus mean : 36.1636**

**Gaus Width: 4.2262**



# B1L103S, U3-ch14, adc2

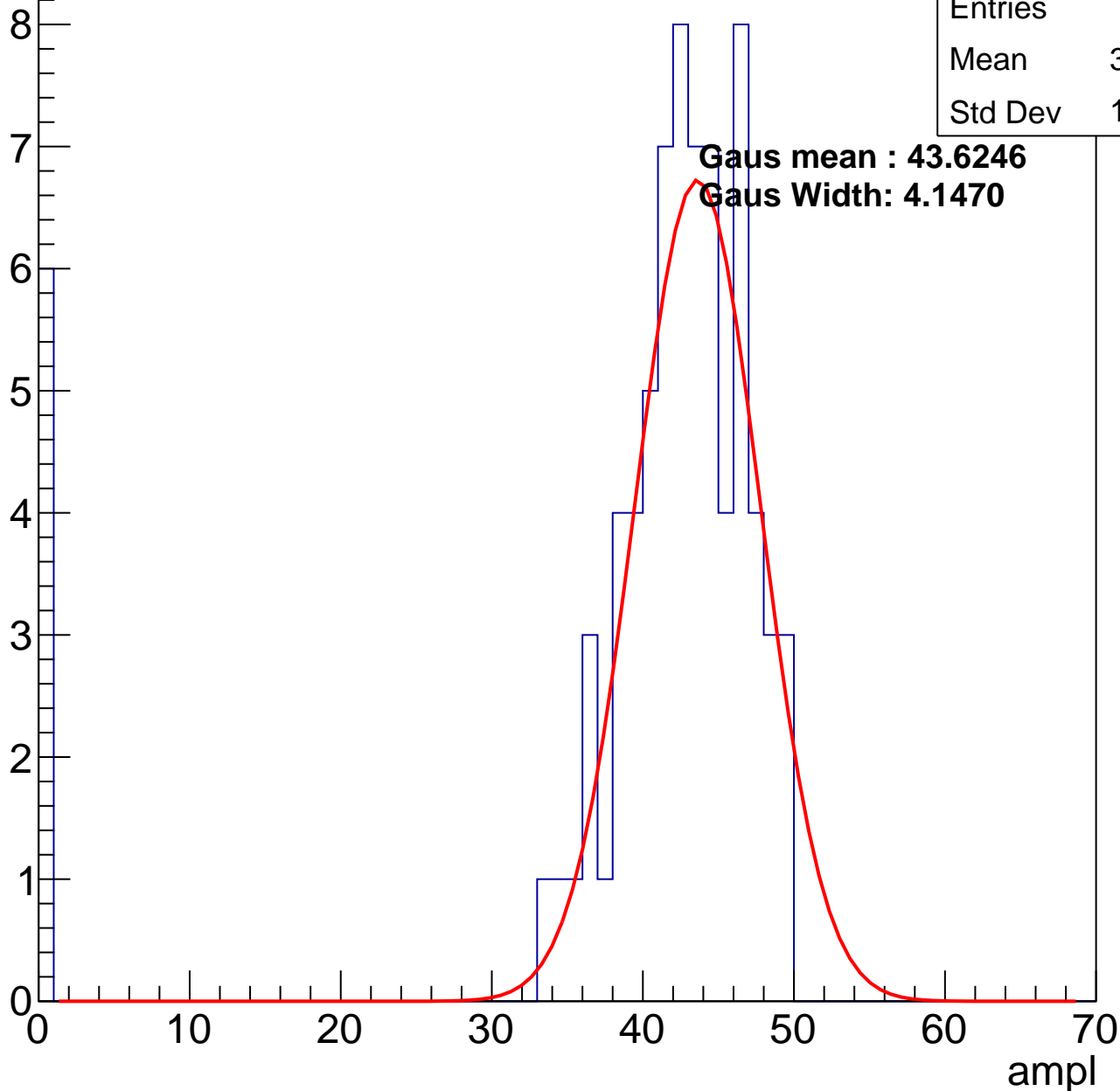
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	77
Mean	39.14
Std Dev	11.93

**Gaus mean : 43.6246**

**Gaus Width: 4.1470**

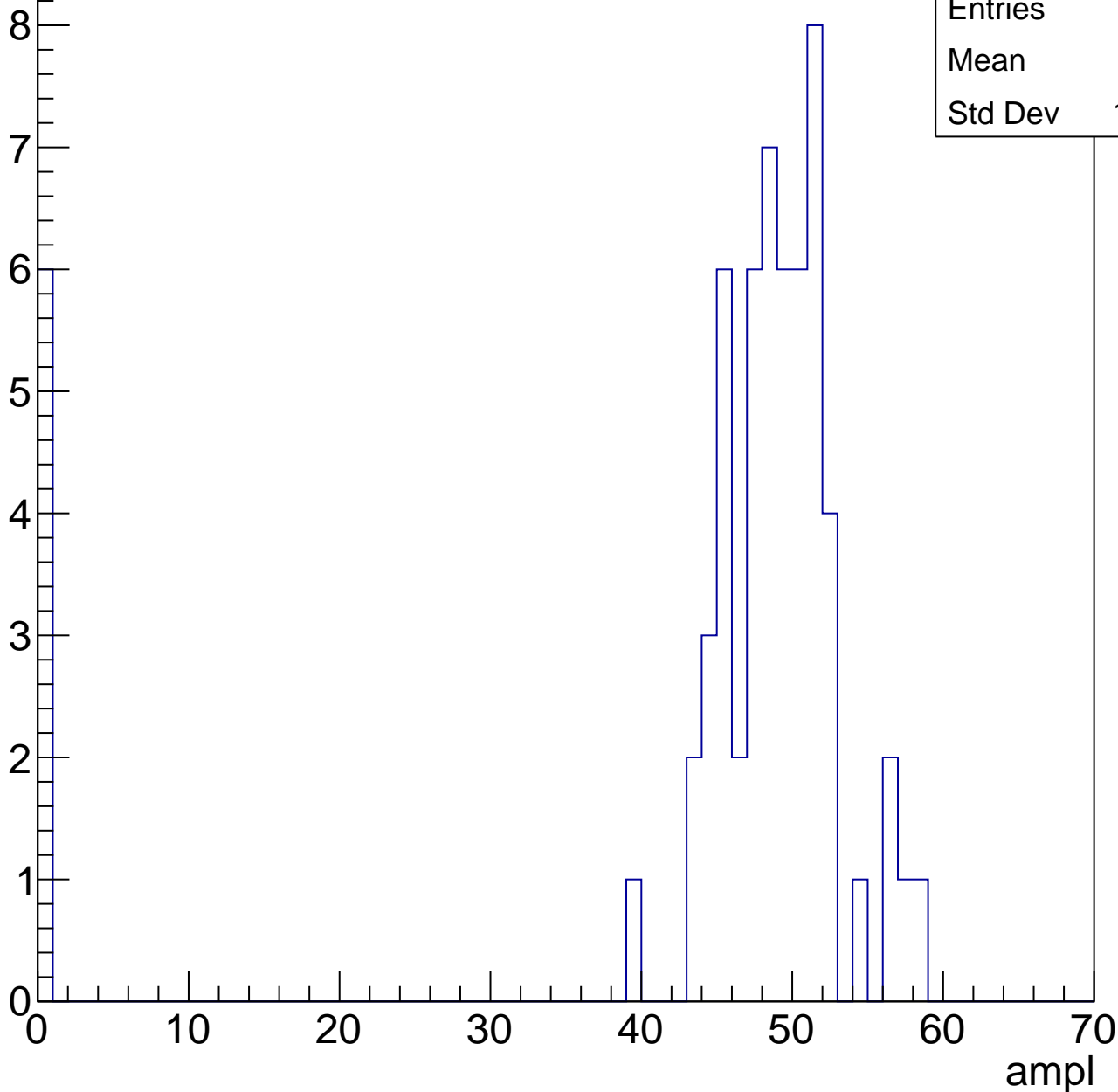


# B1L103S, U3-ch14, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	44
Std Dev	14.81

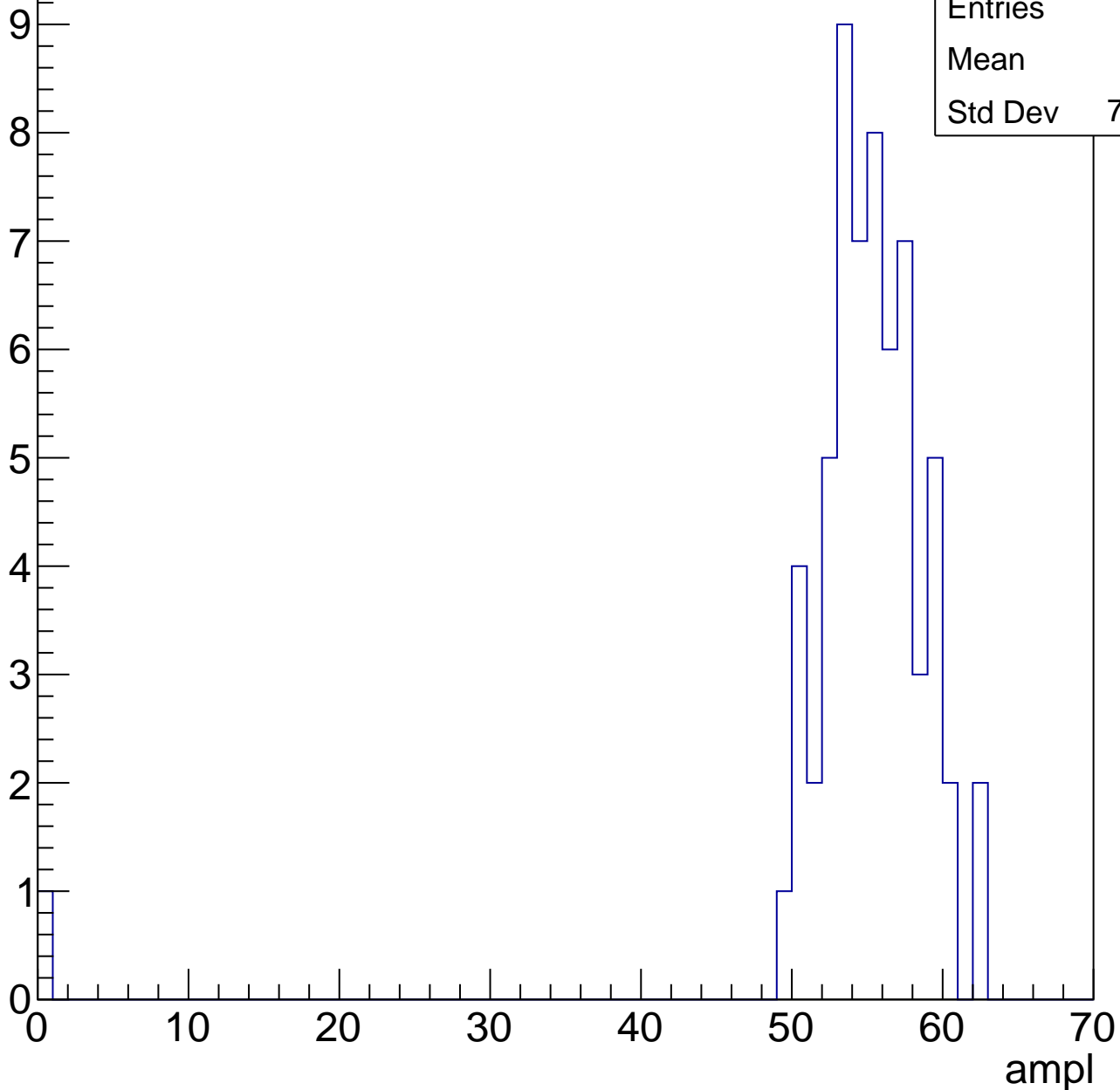


# B1L103S, U3-ch14, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	54.1
Std Dev	7.534



# B1L103S, U3-ch14, adc5

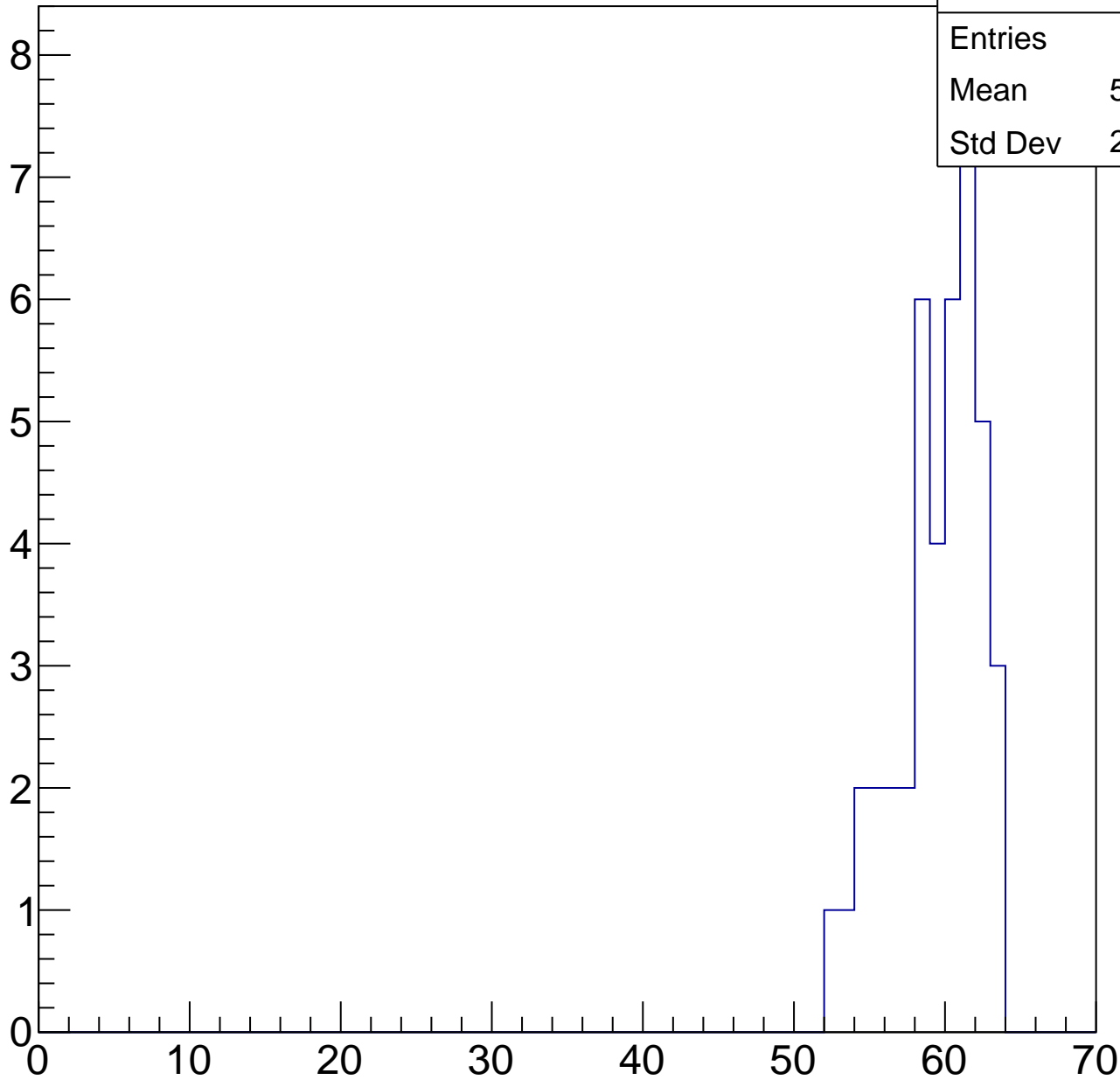
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	42
Mean	59.05
Std Dev	2.803

ampl

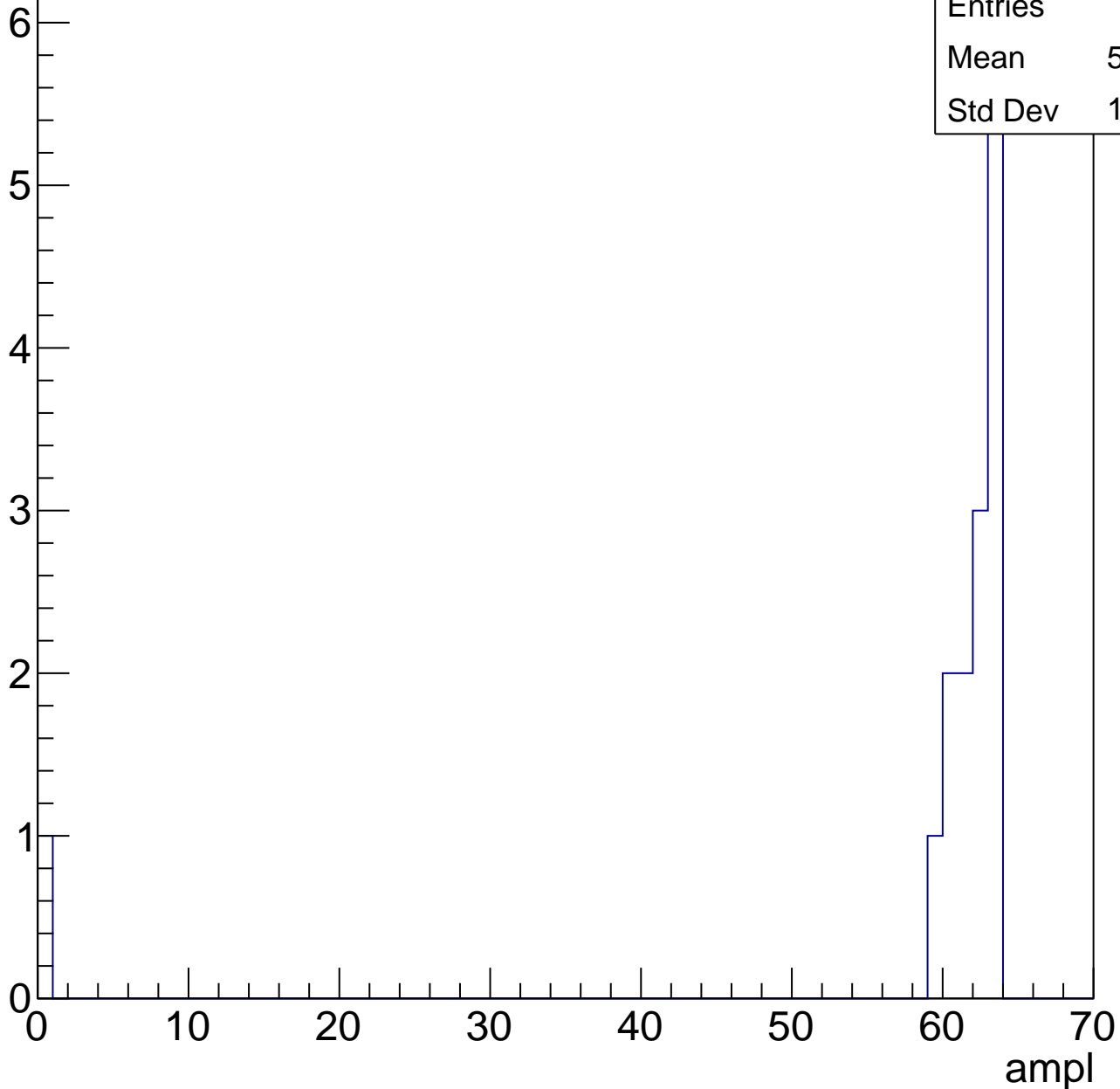


# B1L103S, U3-ch14, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	15
Mean	57.67
Std Dev	15.46





# B1L103S, U3-ch14, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

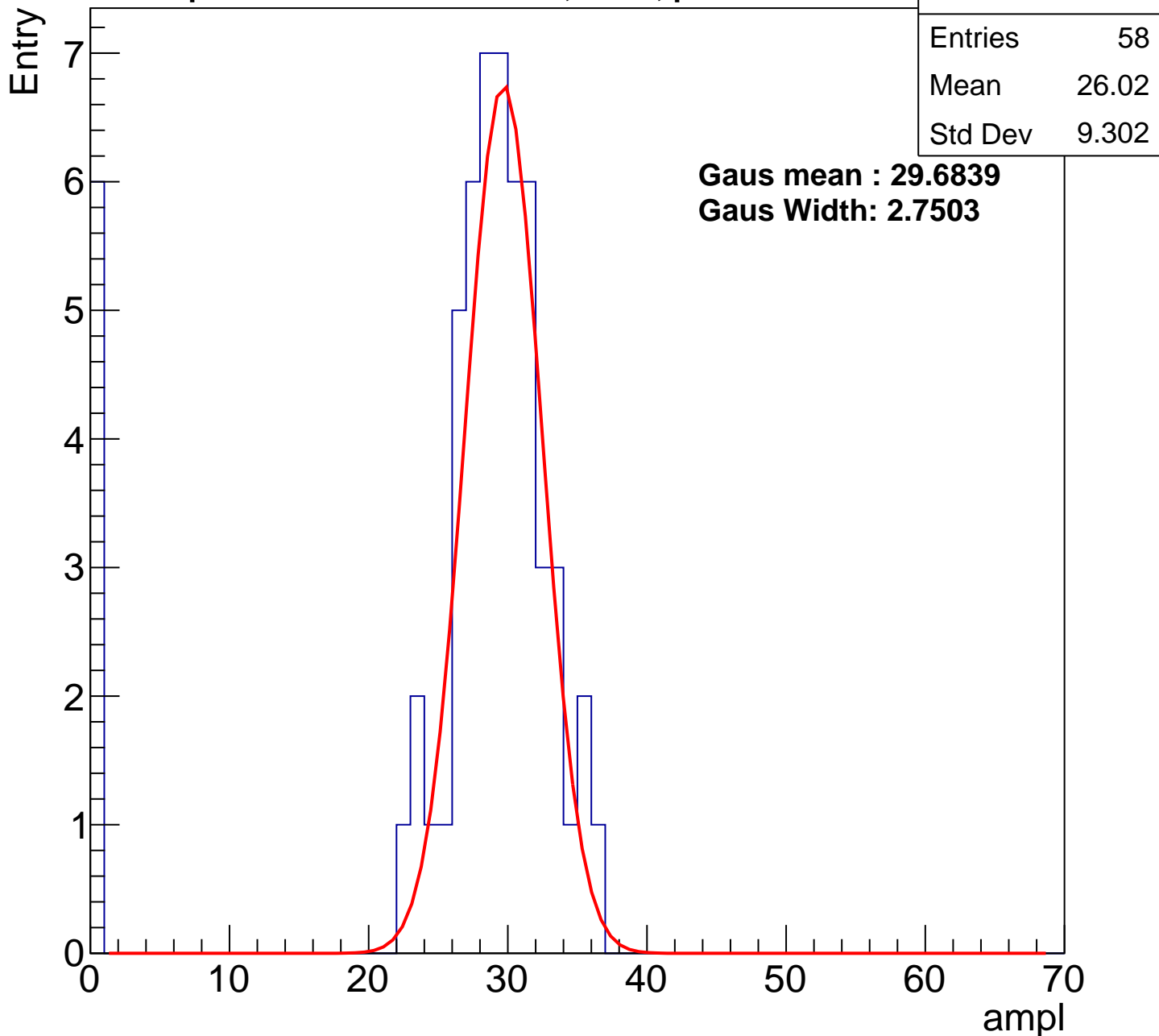
Entries	20
Mean	3.15
Std Dev	13.73

Entry



# B1L103S, U3-ch15, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U3-ch15, adc1

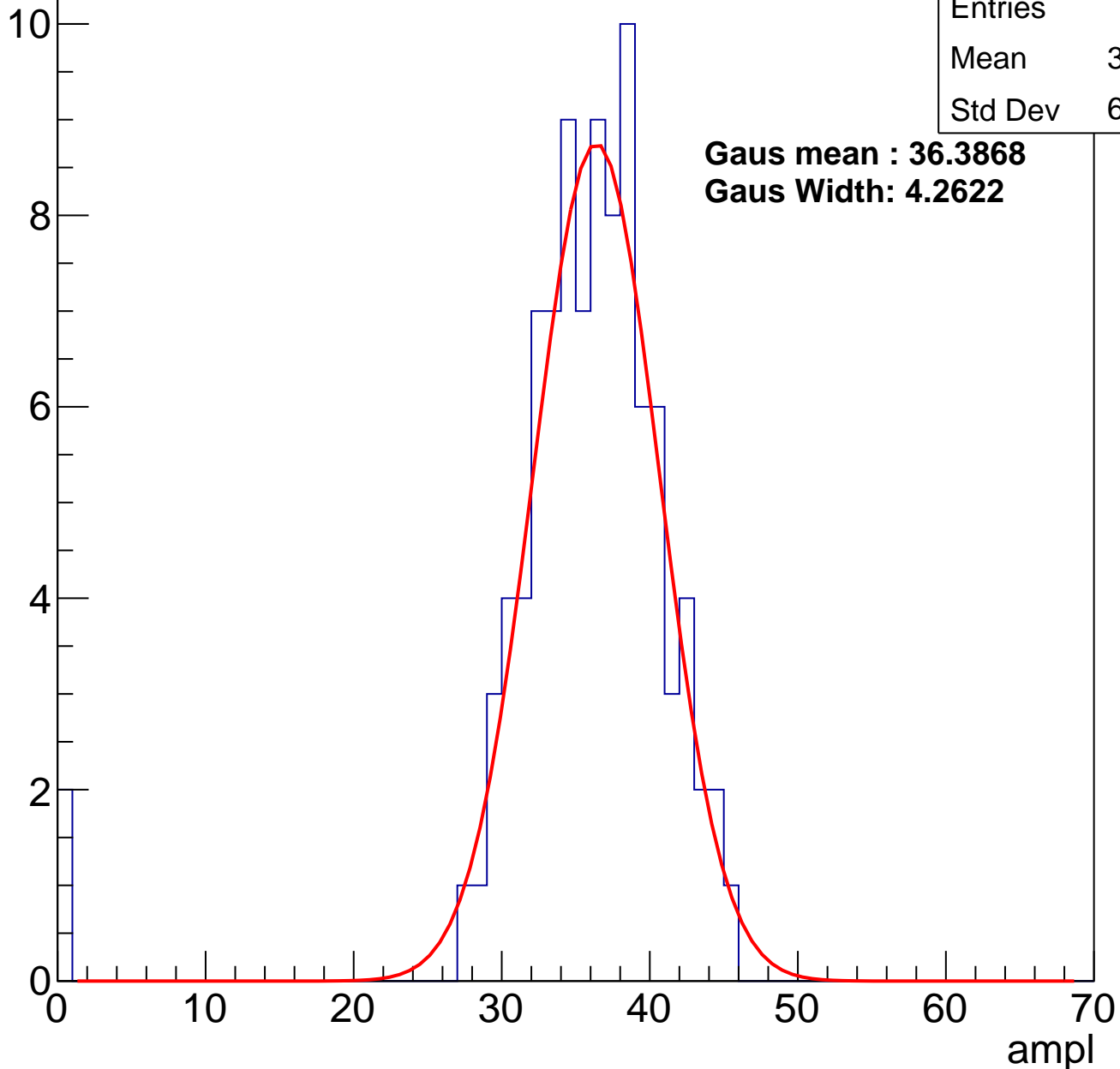
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	96
Mean	35.17
Std Dev	6.458

**Gaus mean : 36.3868**

**Gaus Width: 4.2622**

Entry



# B1L103S, U3-ch15, adc2

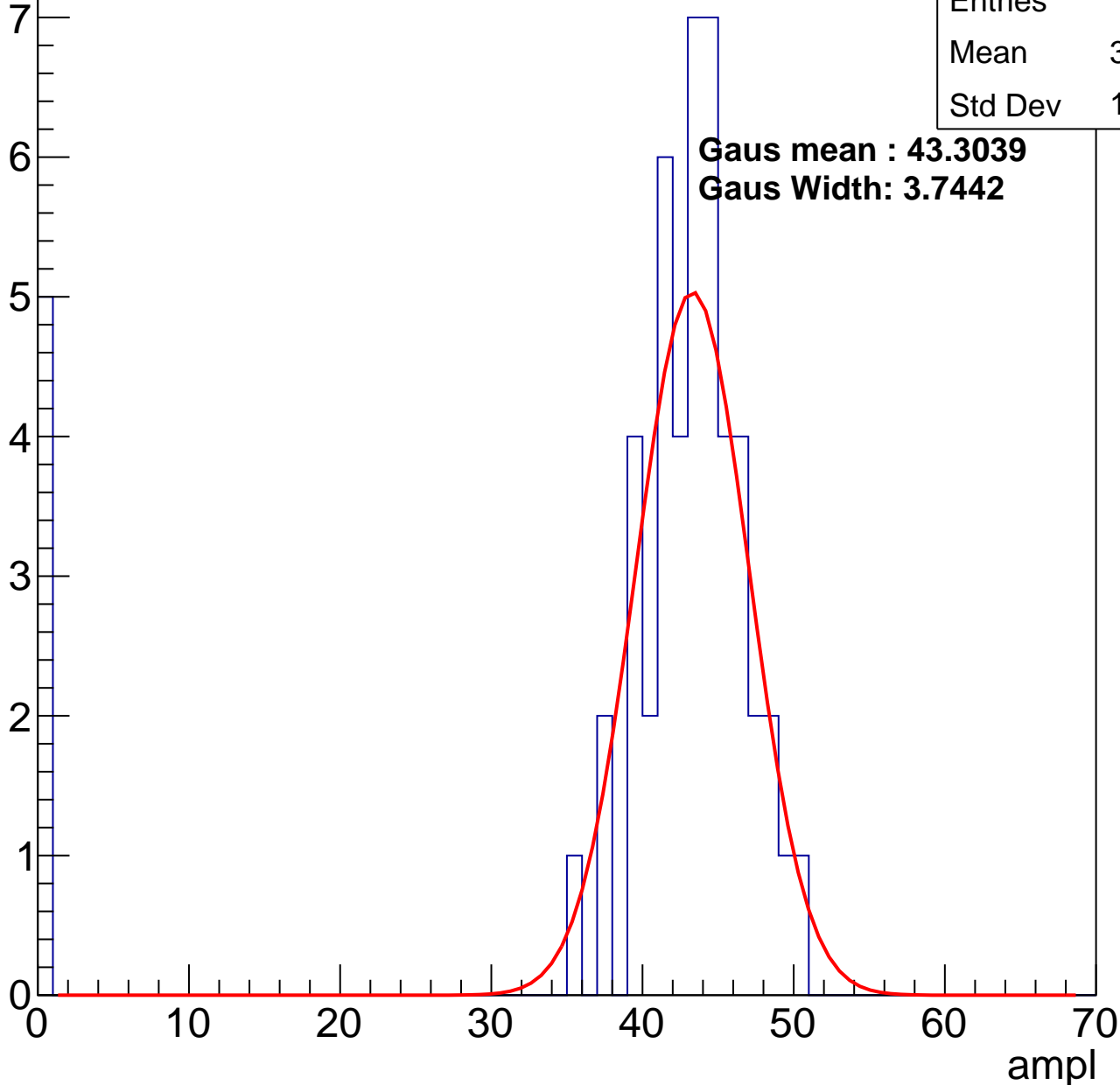
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	52
Mean	38.87
Std Dev	13.03

**Gaus mean : 43.3039**

**Gaus Width: 3.7442**

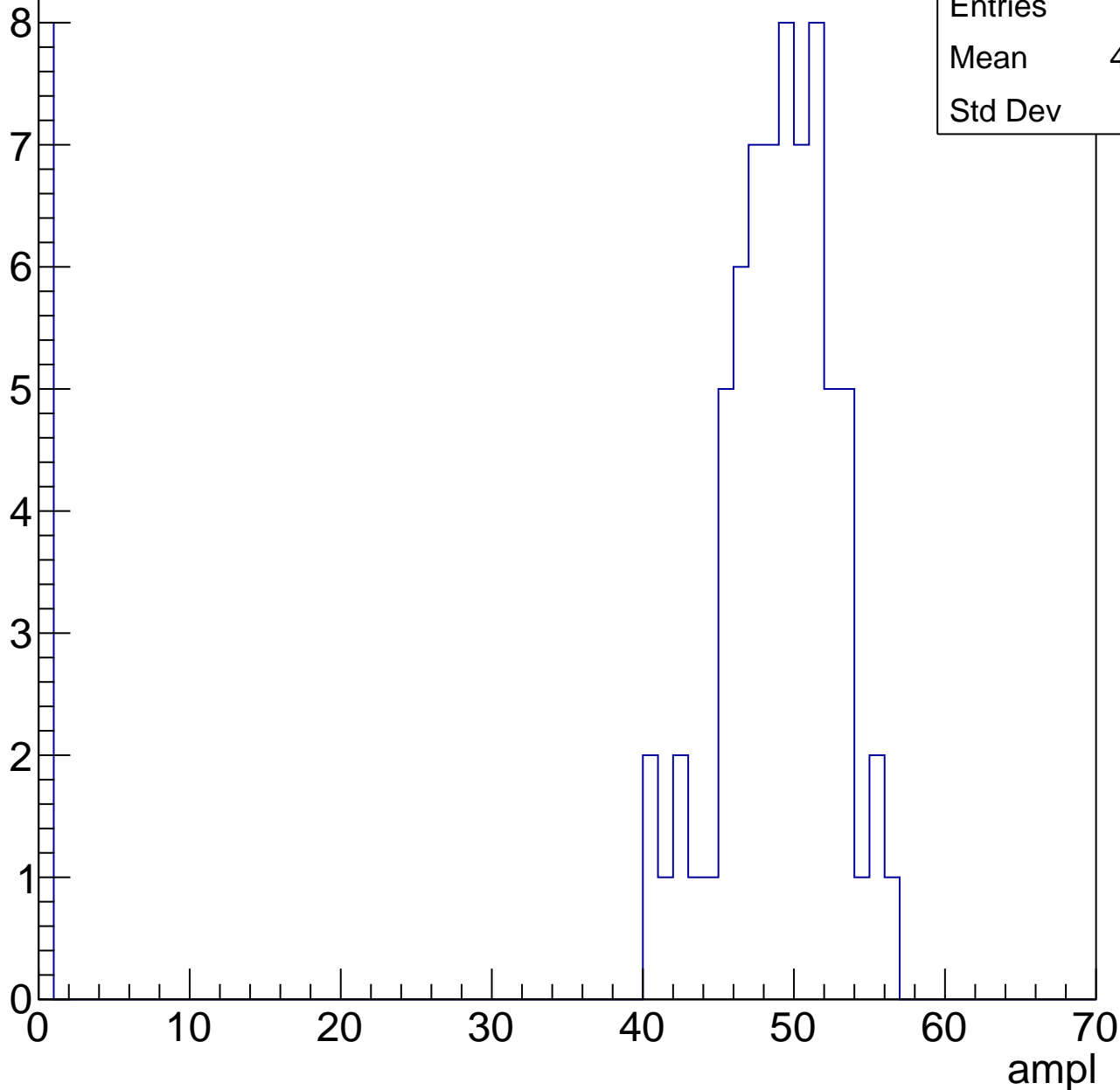


# B1L103S, U3-ch15, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	77
Mean	43.55
Std Dev	15.2

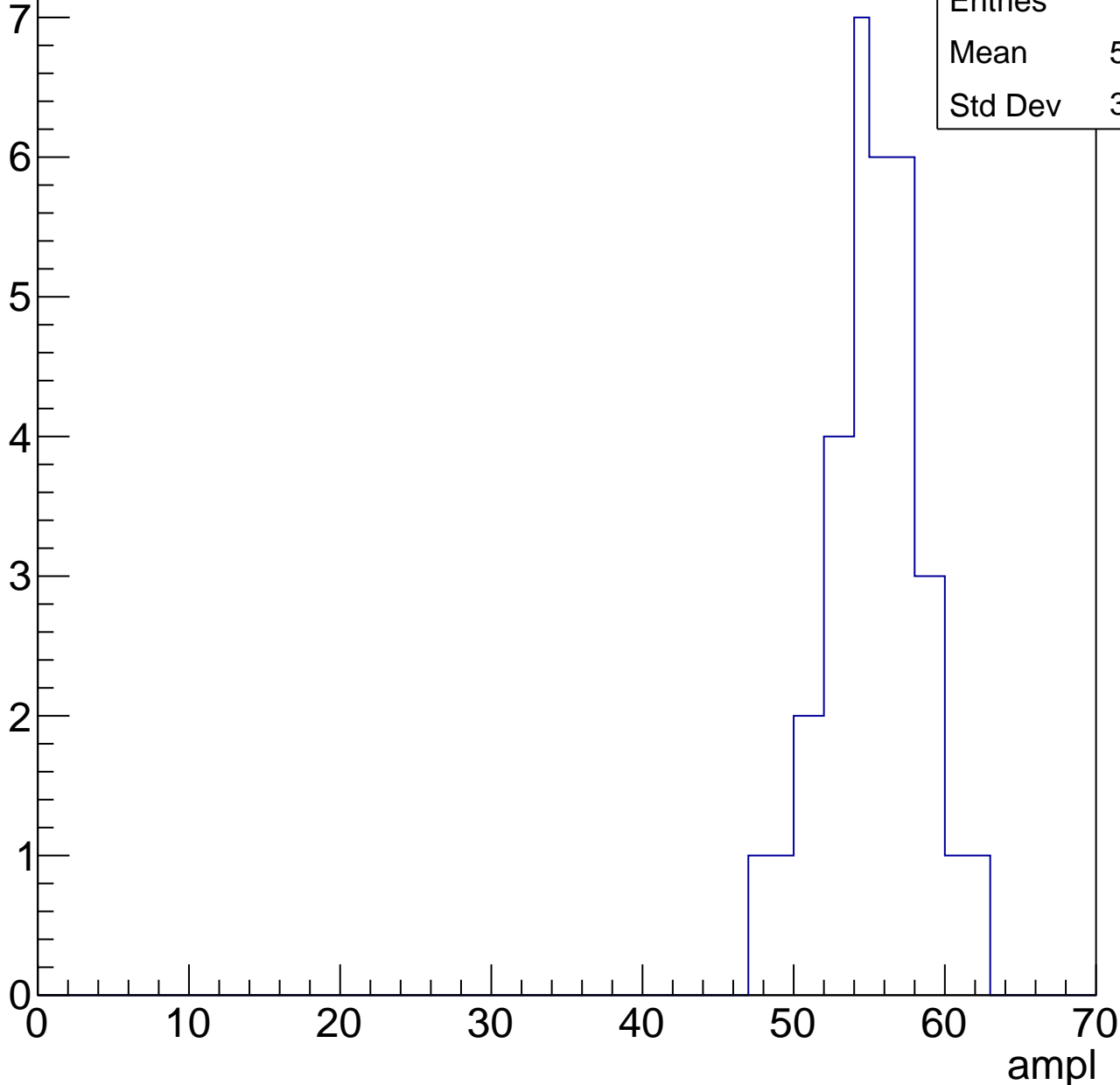


# B1L103S, U3-ch15, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

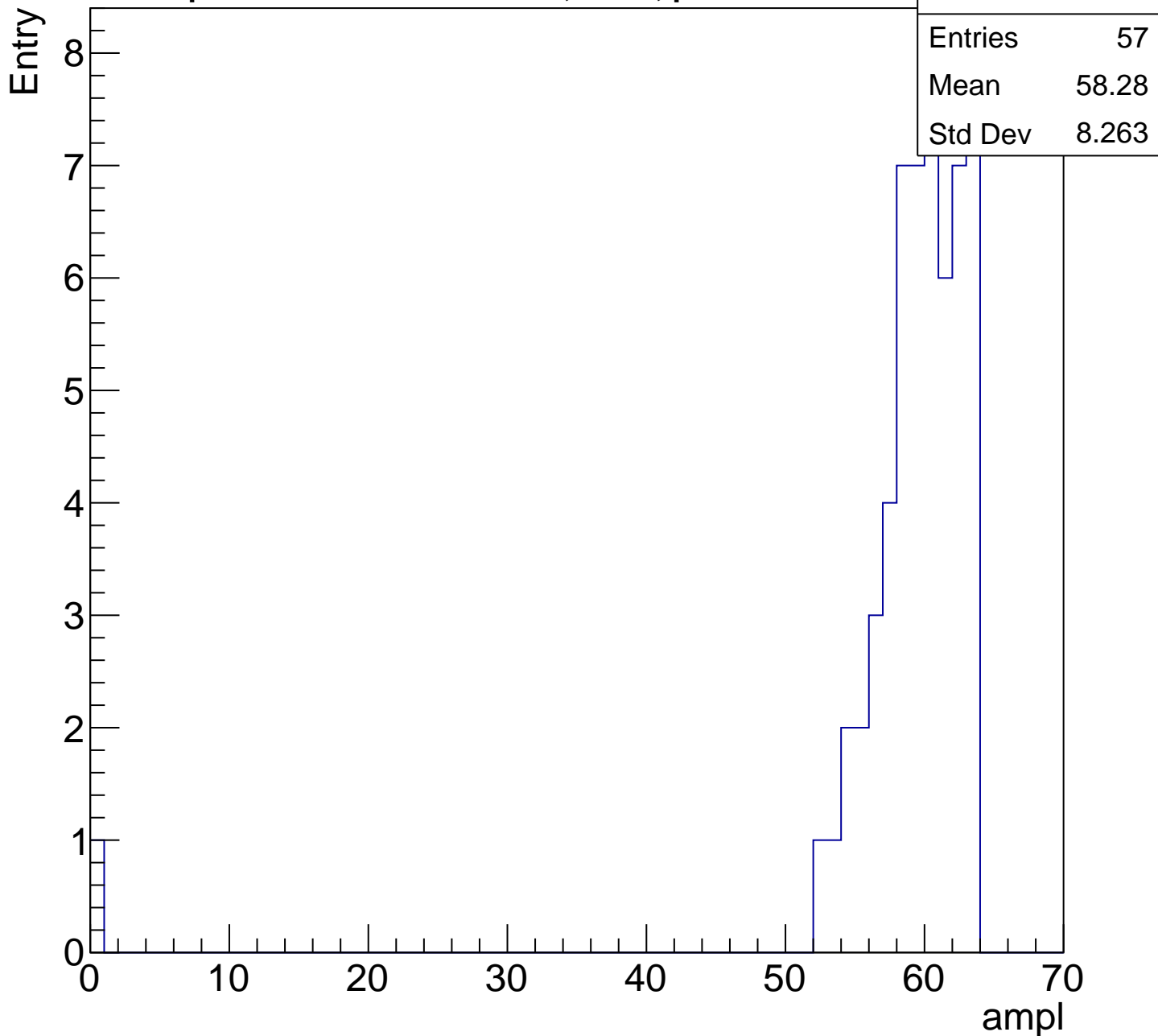
Entry

Entries	49
Mean	54.82
Std Dev	3.205



# B1L103S, U3-ch15, adc5

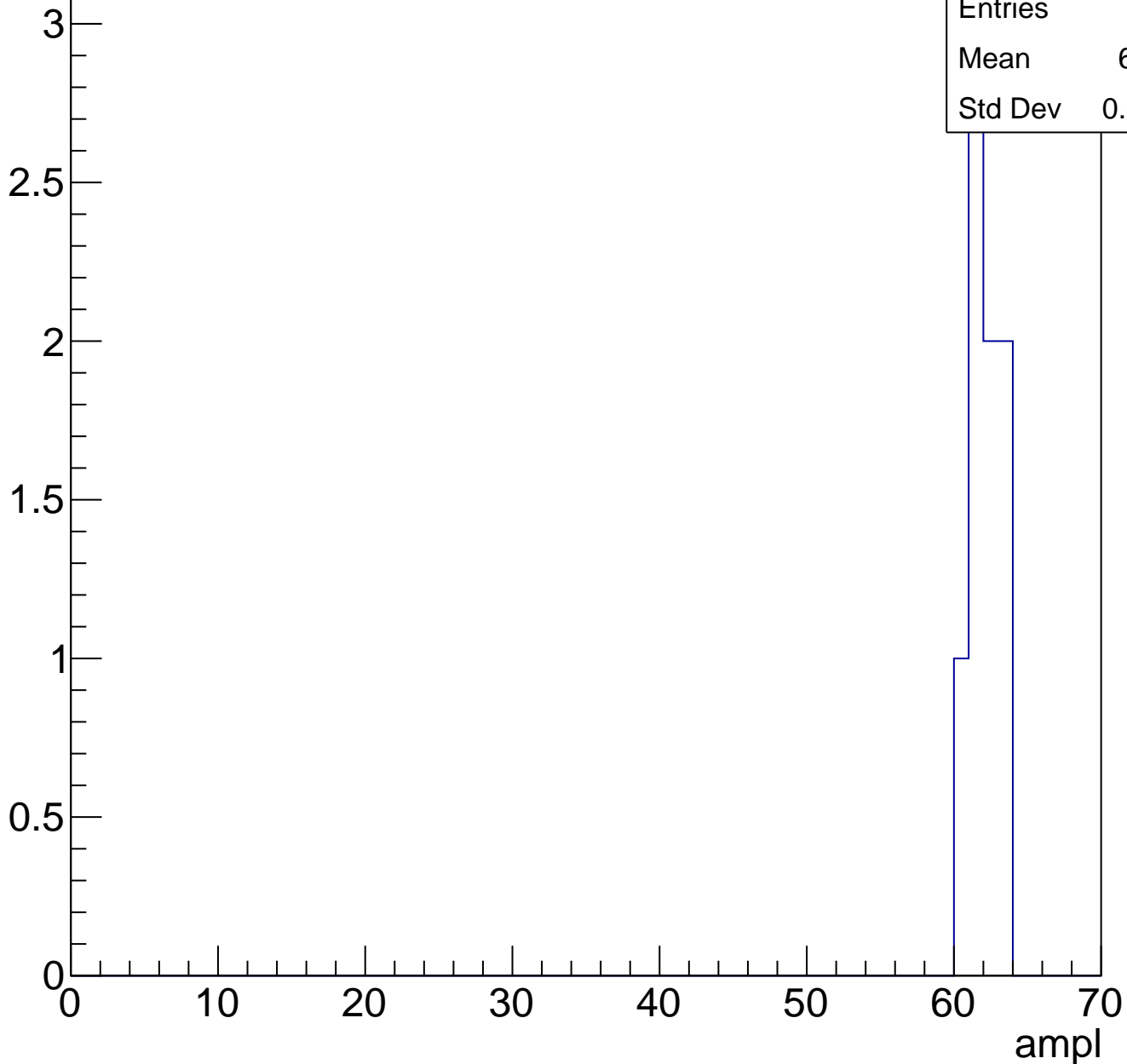
calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U3-ch15, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



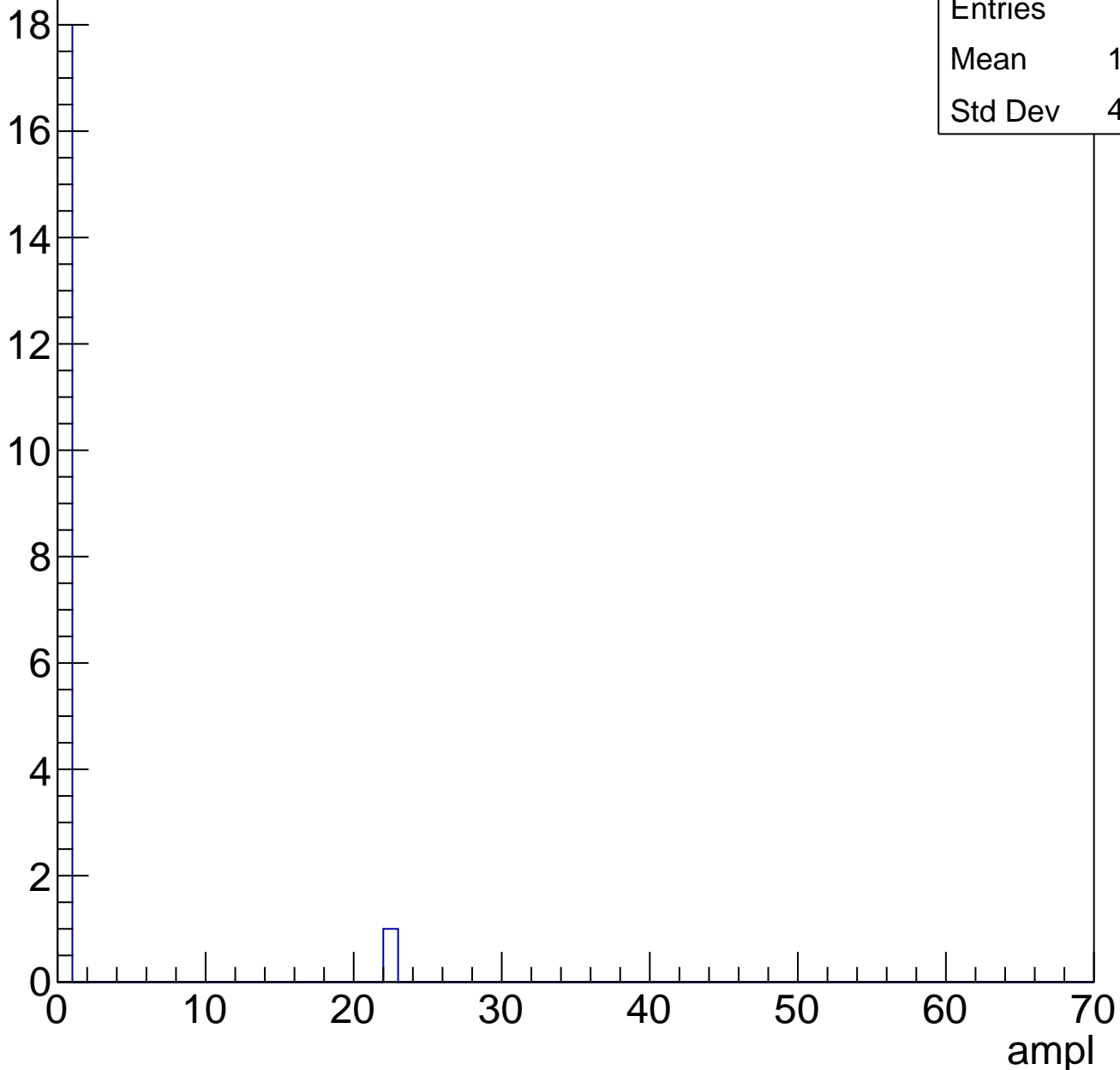


# B1L103S, U3-ch15, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	1.158
Std Dev	4.913

Entry



# B1L103S, U3-ch16, adc0

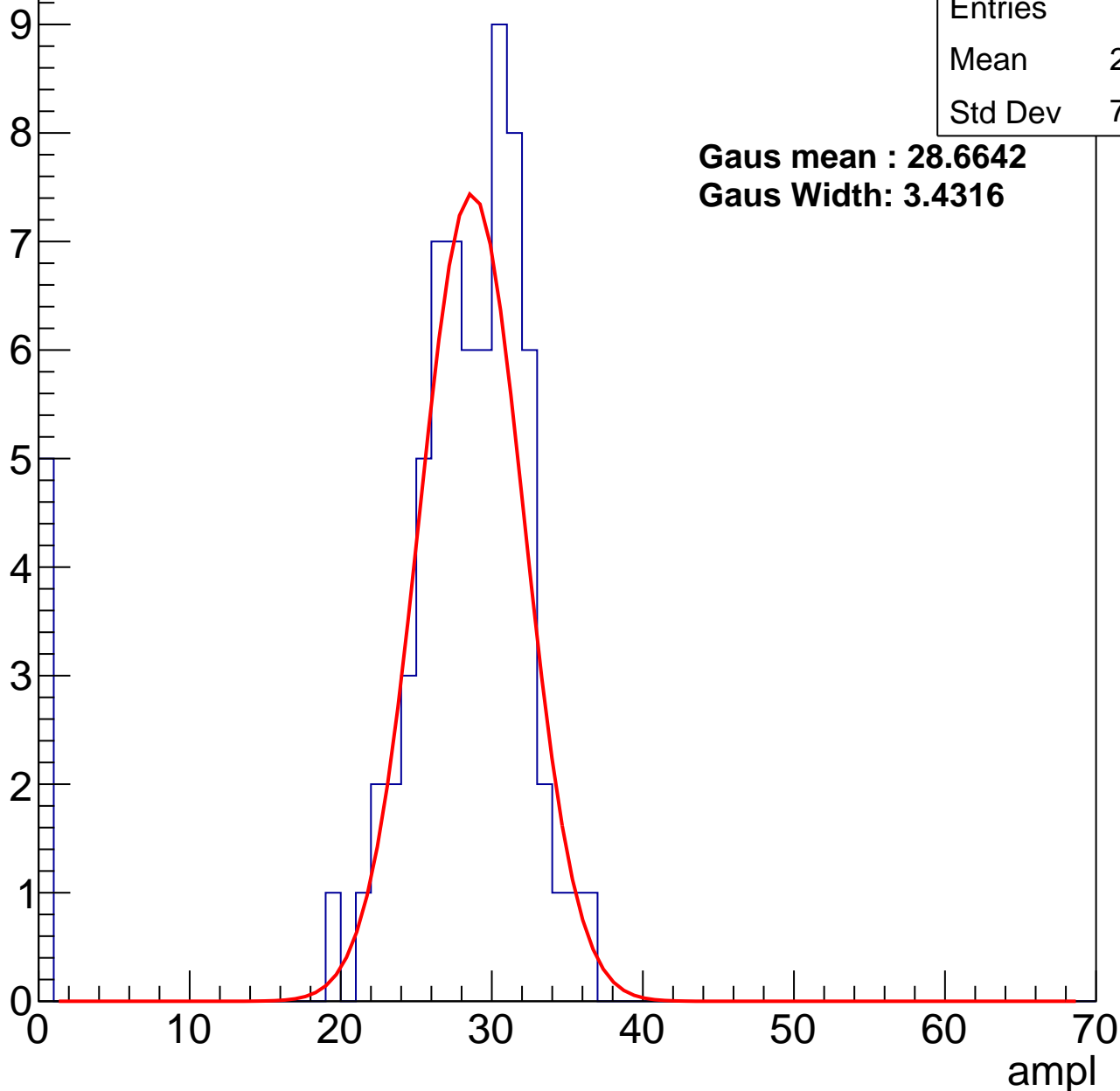
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	26.32
Std Dev	7.853

**Gaus mean : 28.6642**

**Gaus Width: 3.4316**



# B1L103S, U3-ch16, adc1

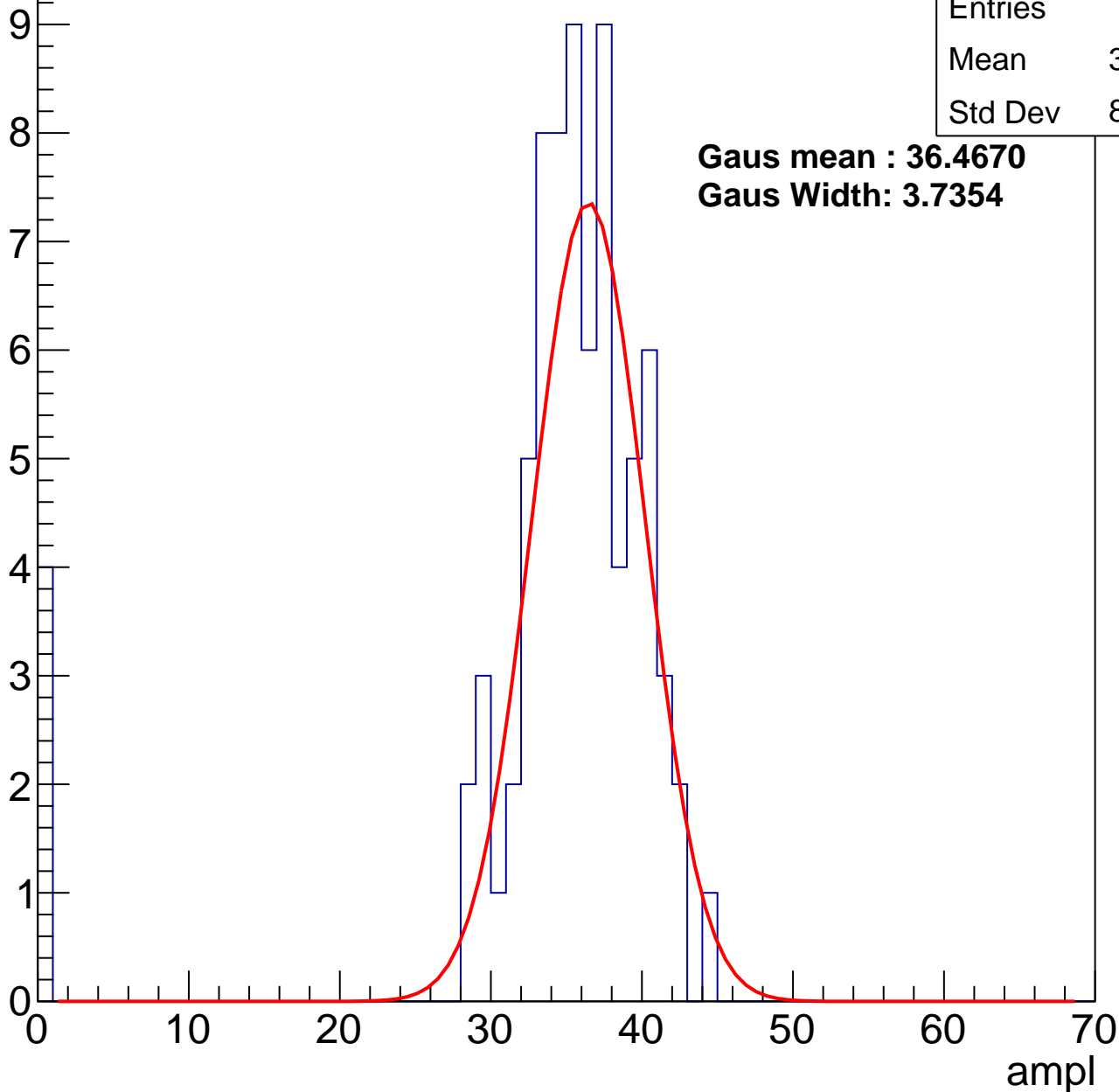
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	78
Mean	33.76
Std Dev	8.565

**Gaus mean : 36.4670**

**Gaus Width: 3.7354**



# B1L103S, U3-ch16, adc2

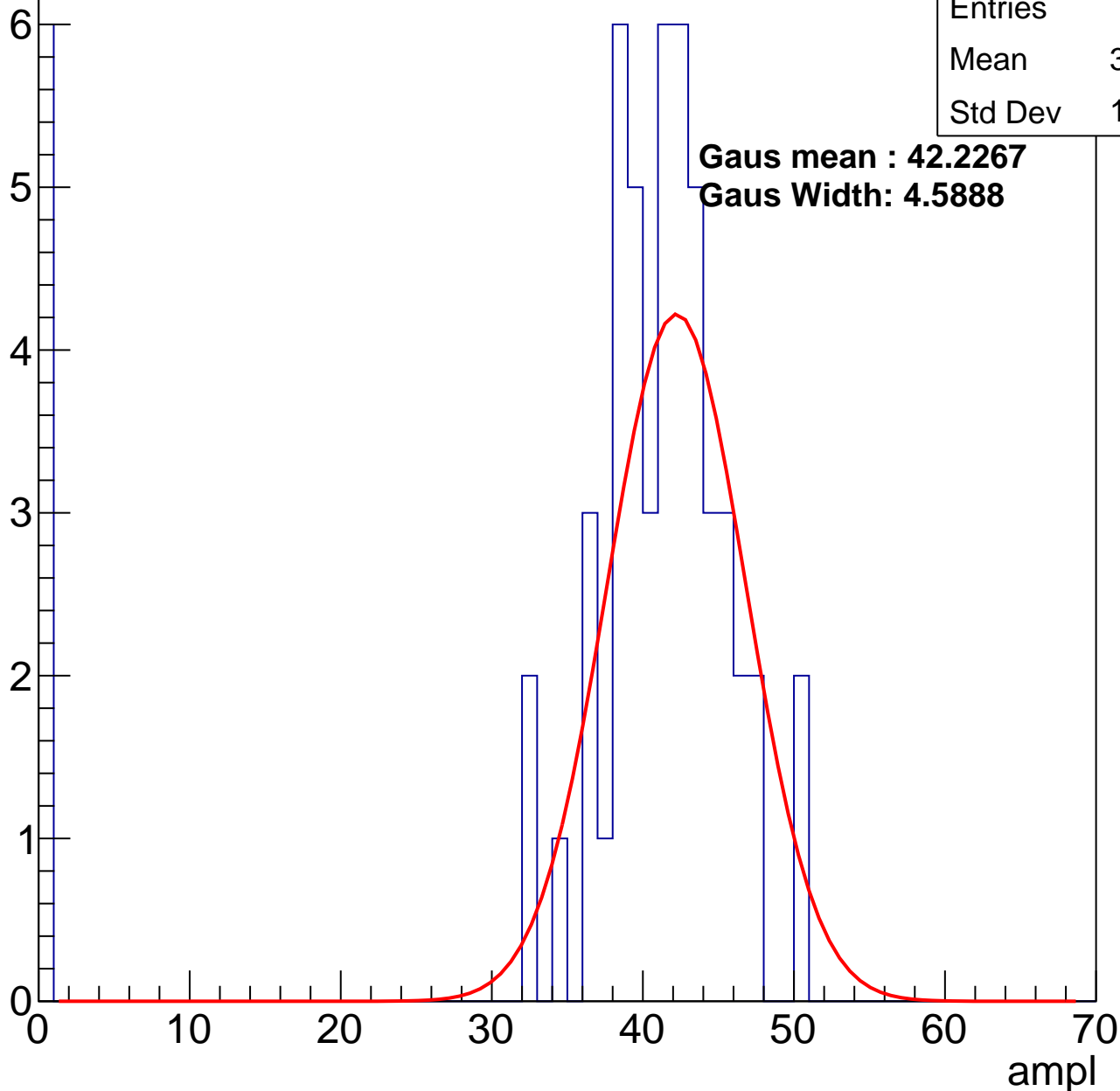
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	56
Mean	36.64
Std Dev	13.22

**Gaus mean : 42.2267**

**Gaus Width: 4.5888**

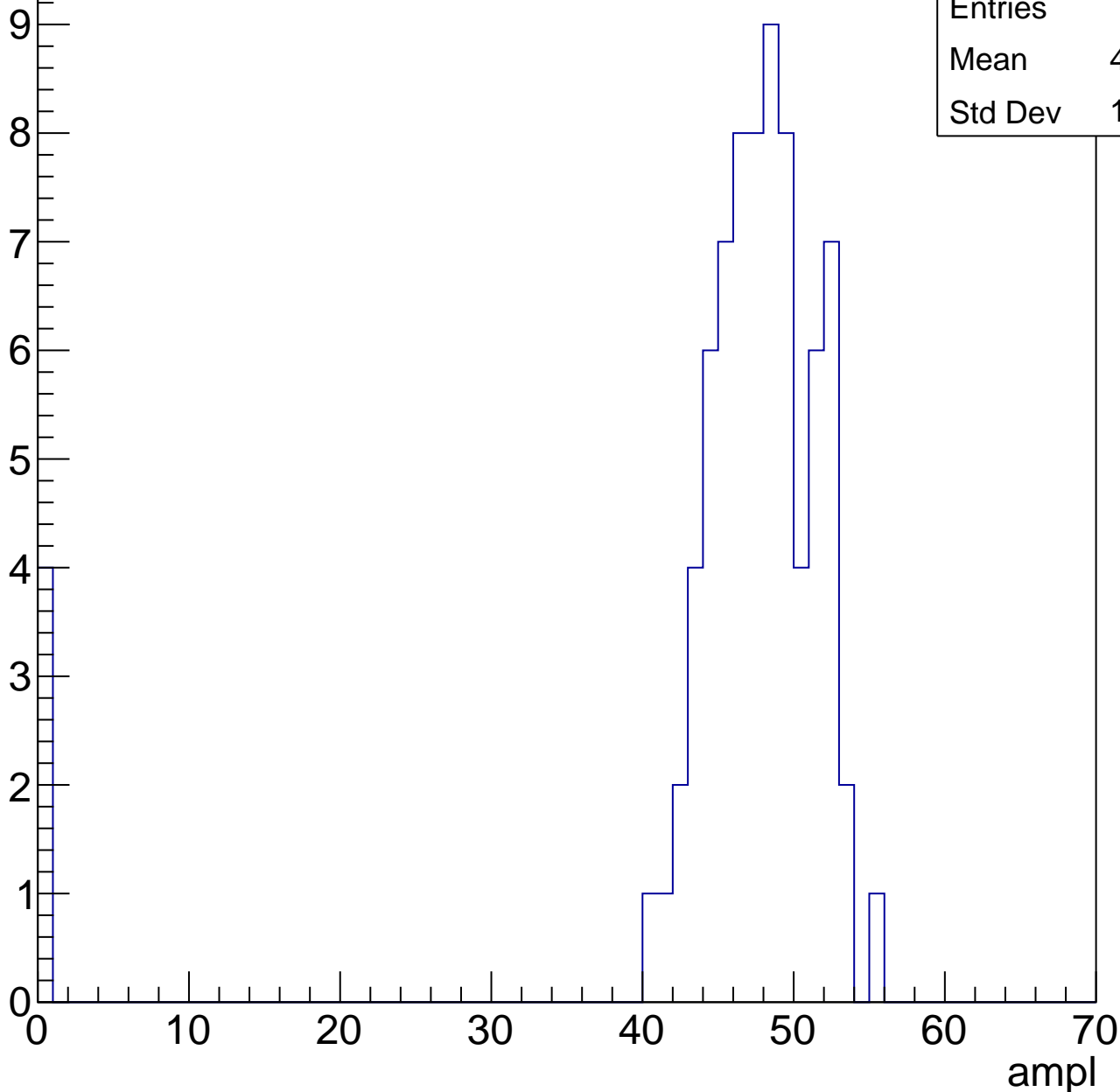


# B1L103S, U3-ch16, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	78
Mean	45.06
Std Dev	10.93

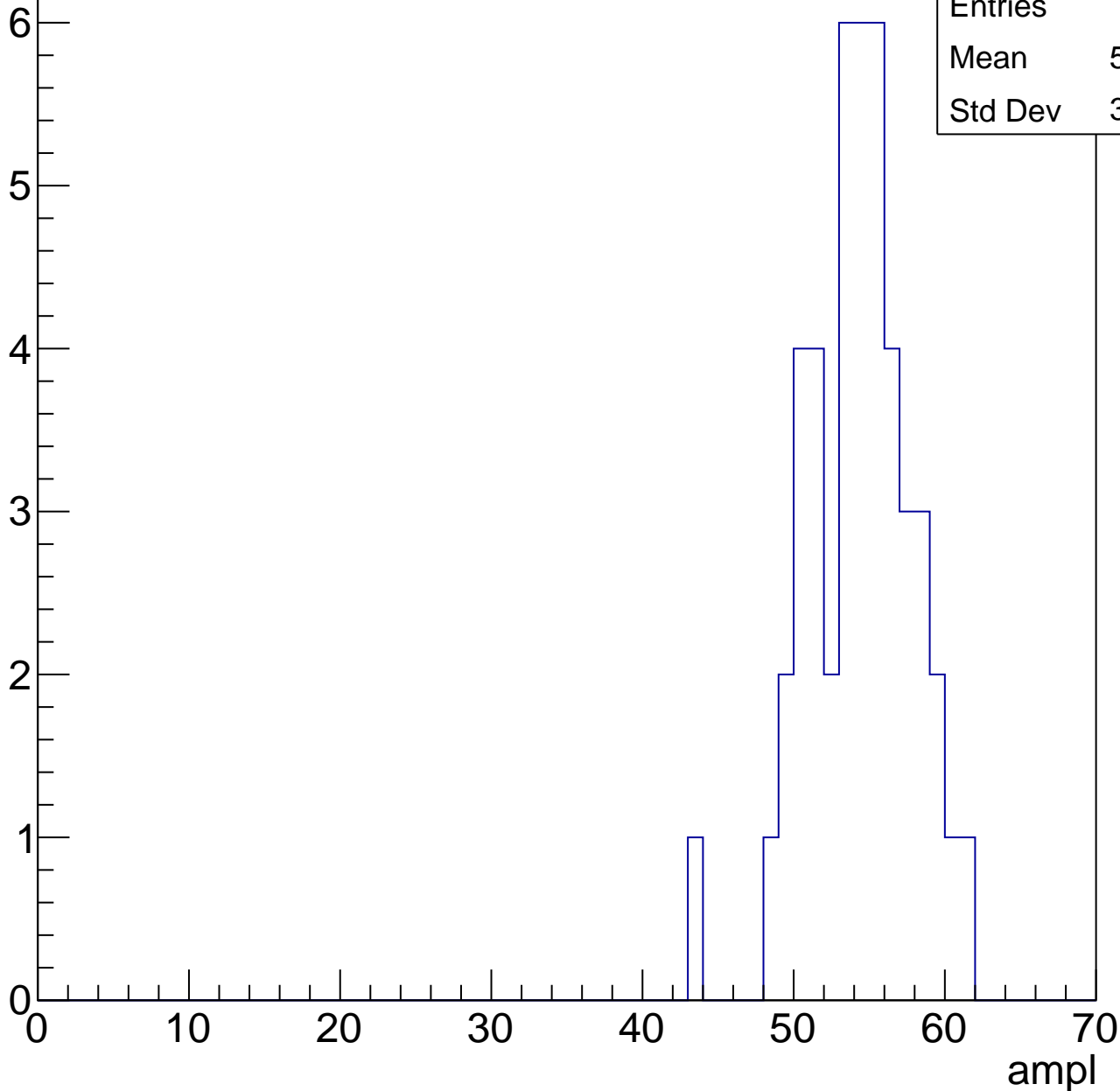


# B1L103S, U3-ch16, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	46
Mean	53.85
Std Dev	3.464

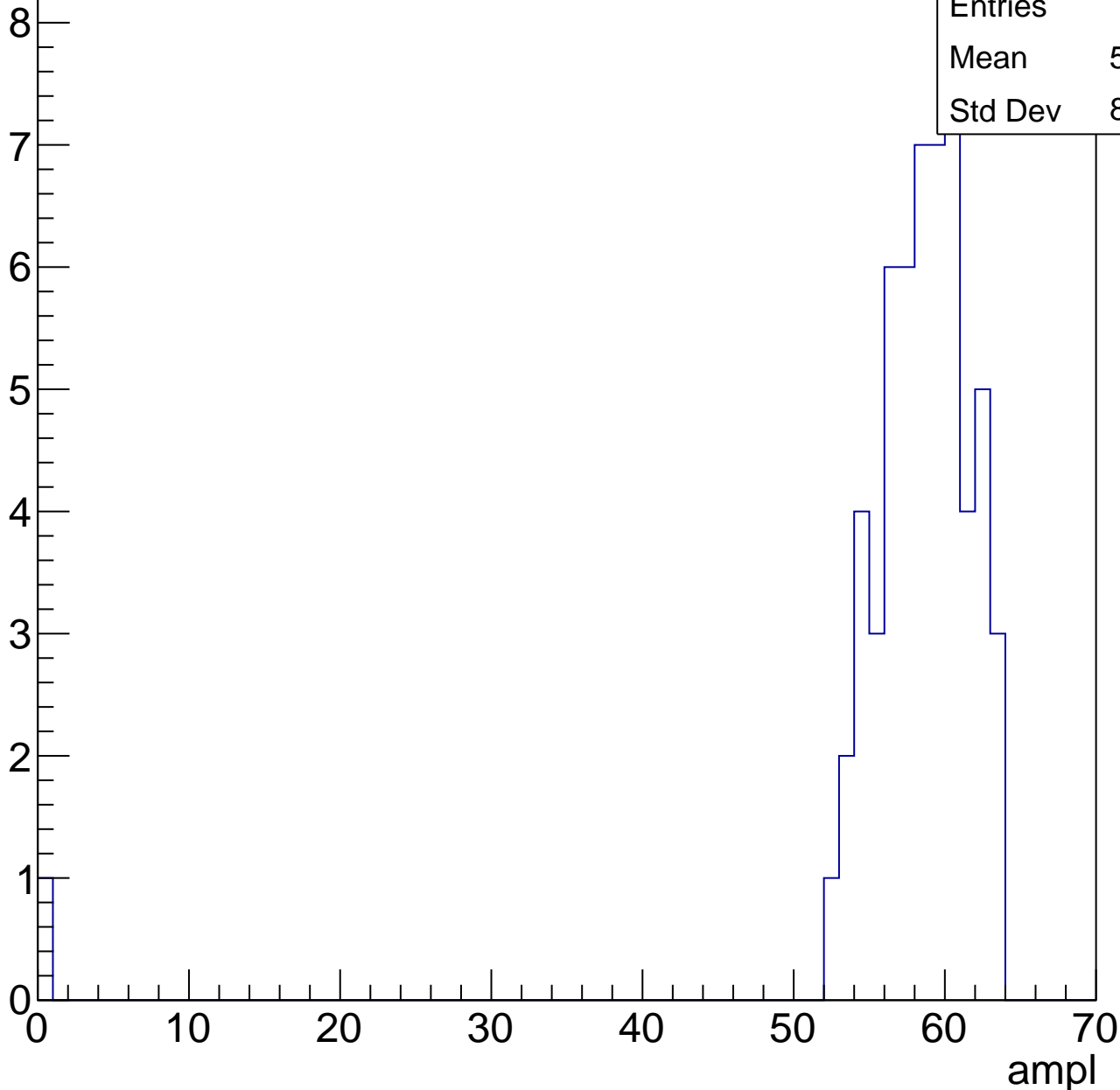


# B1L103S, U3-ch16, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	57
Mean	57.18
Std Dev	8.124

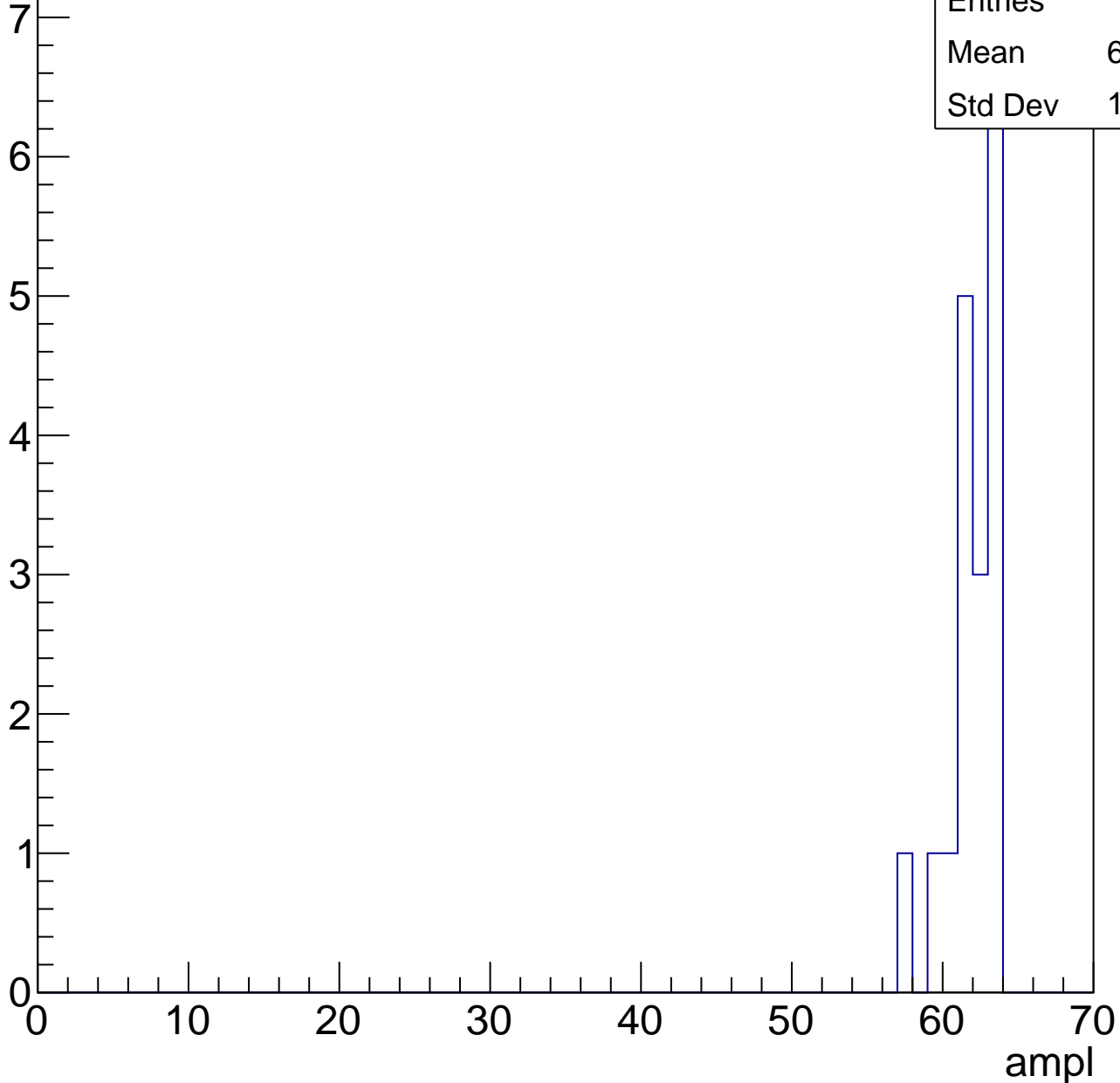


# B1L103S, U3-ch16, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	18
Mean	61.56
Std Dev	1.606



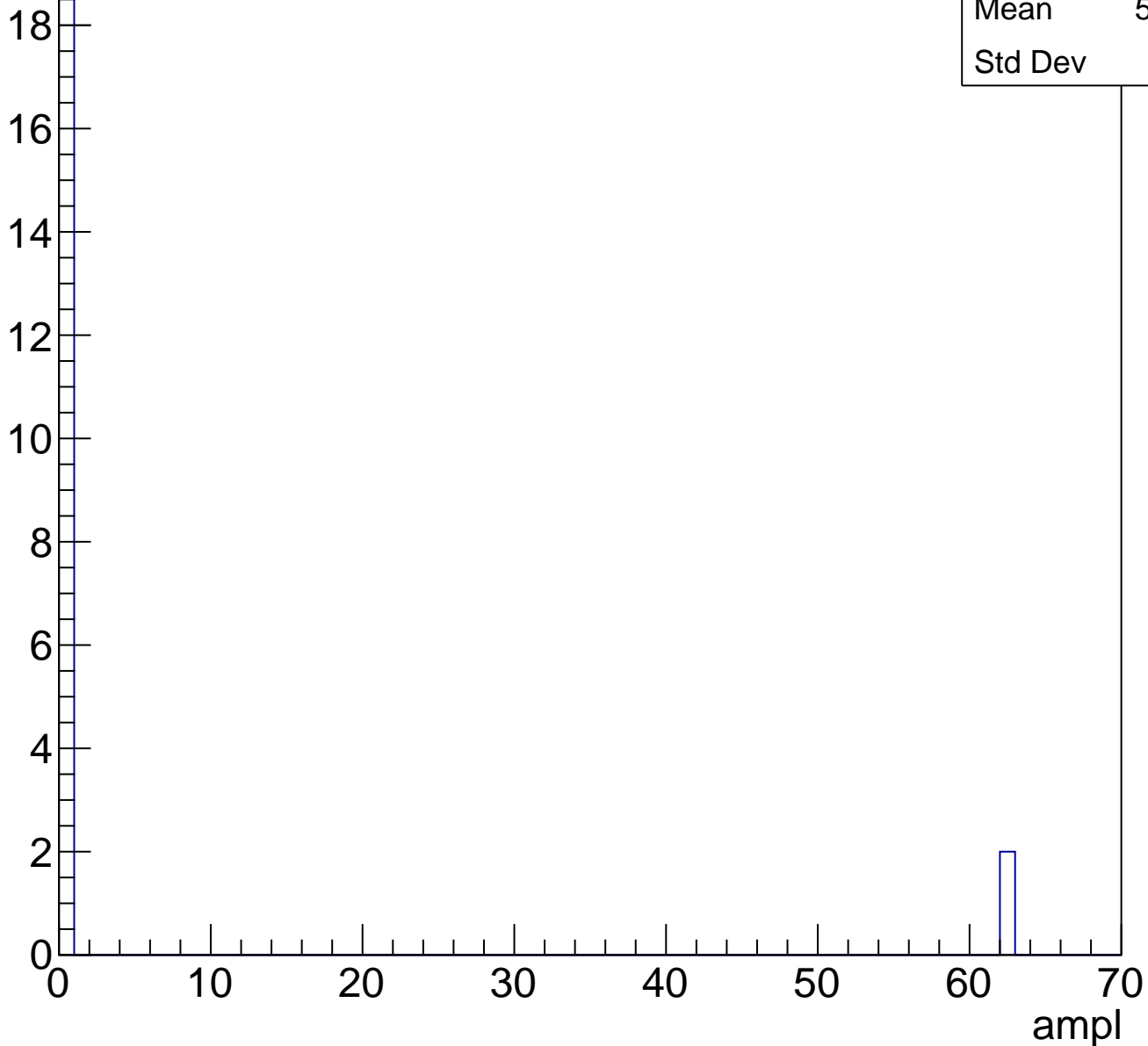


# B1L103S, U3-ch16, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	5.905
Std Dev	18.2

Entry



# B1L103S, U3-ch17, adc0

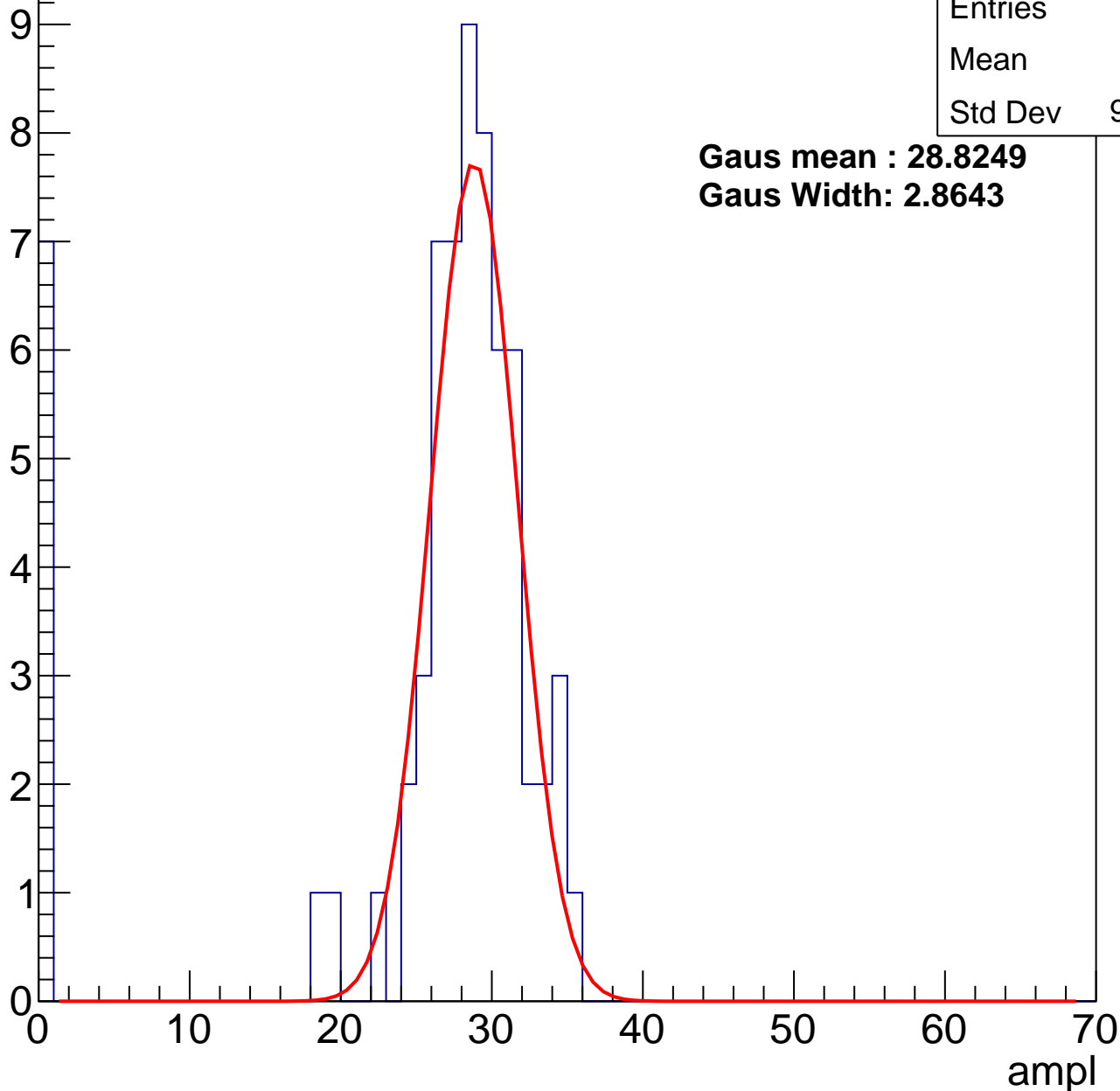
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	25.3
Std Dev	9.247

**Gaus mean : 28.8249**

**Gaus Width: 2.8643**



# B1L103S, U3-ch17, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	93
Mean	32.45
Std Dev	11.12

**Gaus mean : 36.5168**

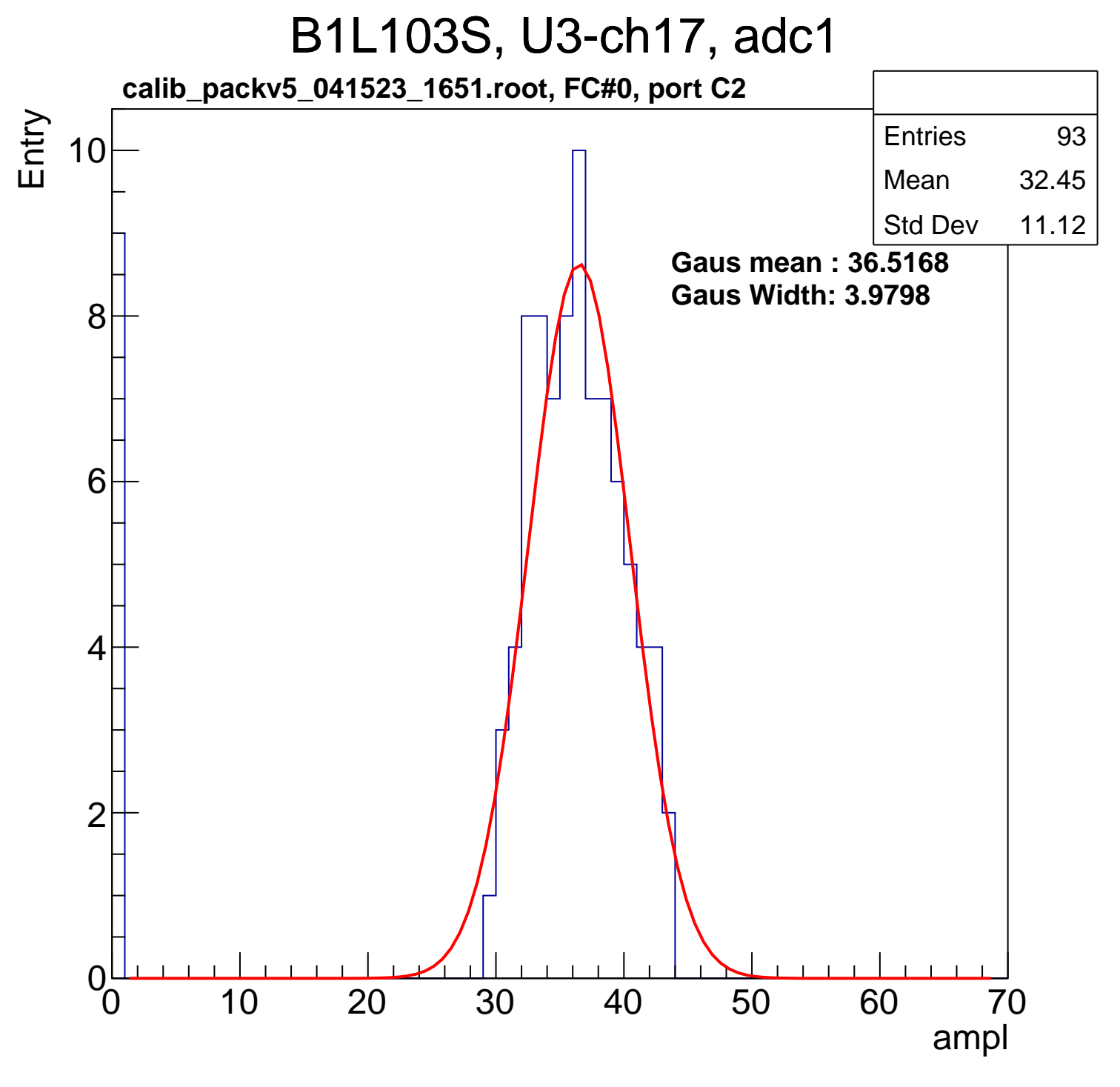
**Gaus Width: 3.9798**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch17, adc2

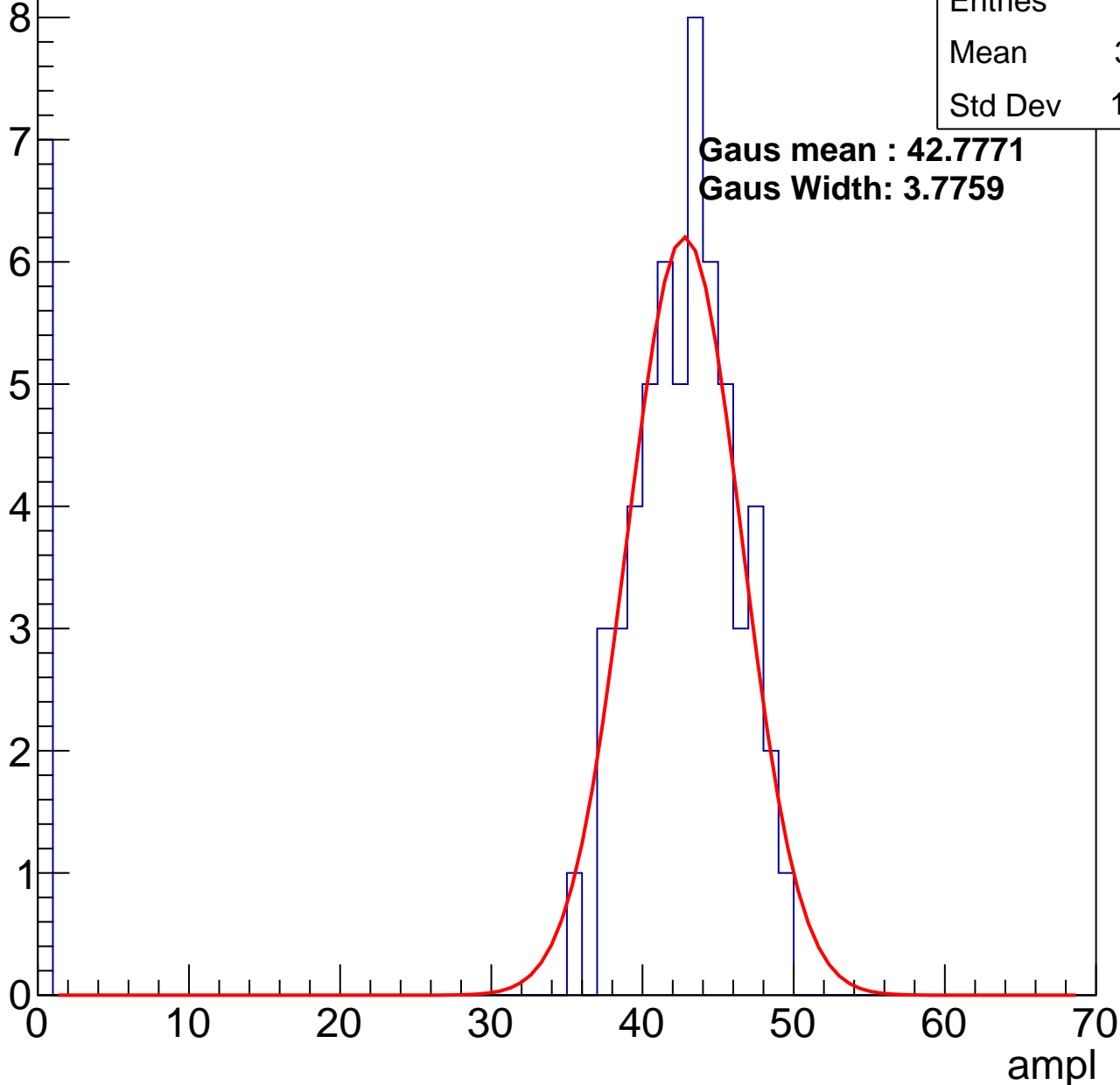
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	37.71
Std Dev	13.67

**Gaus mean : 42.7771**

**Gaus Width: 3.7759**

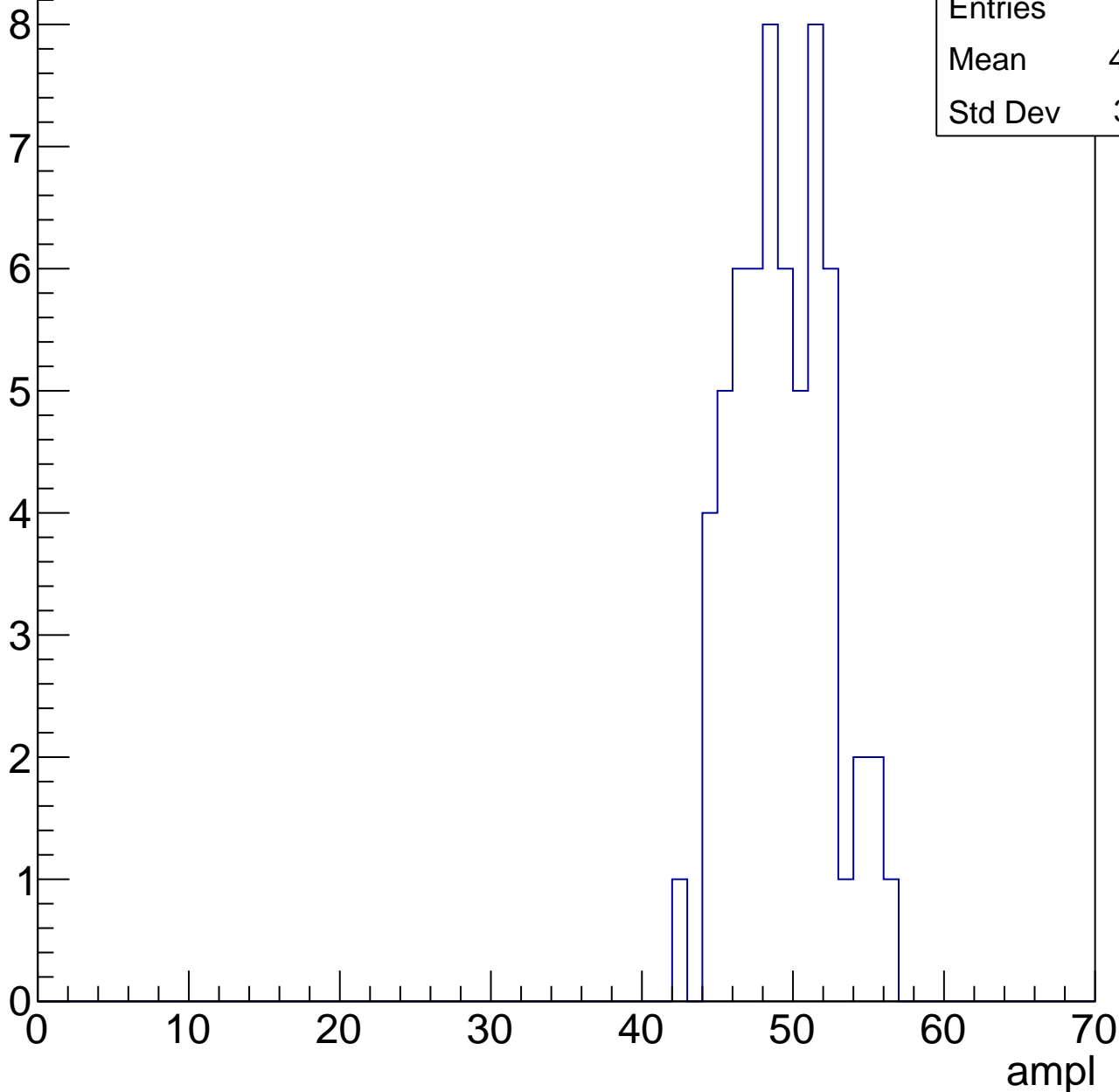


# B1L103S, U3-ch17, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

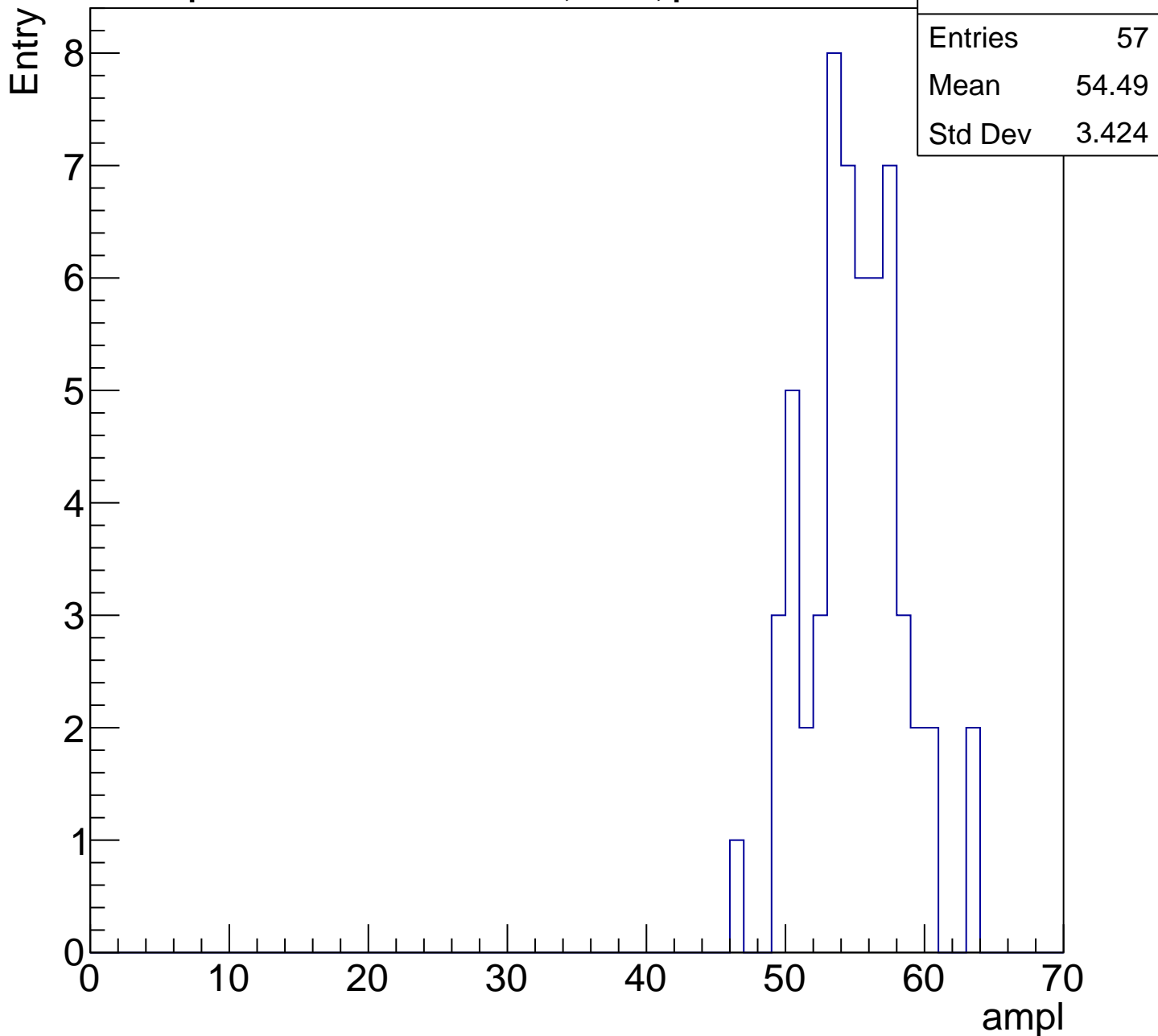
Entry

Entries	61
Mean	48.79
Std Dev	3.111



# B1L103S, U3-ch17, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U3-ch17, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

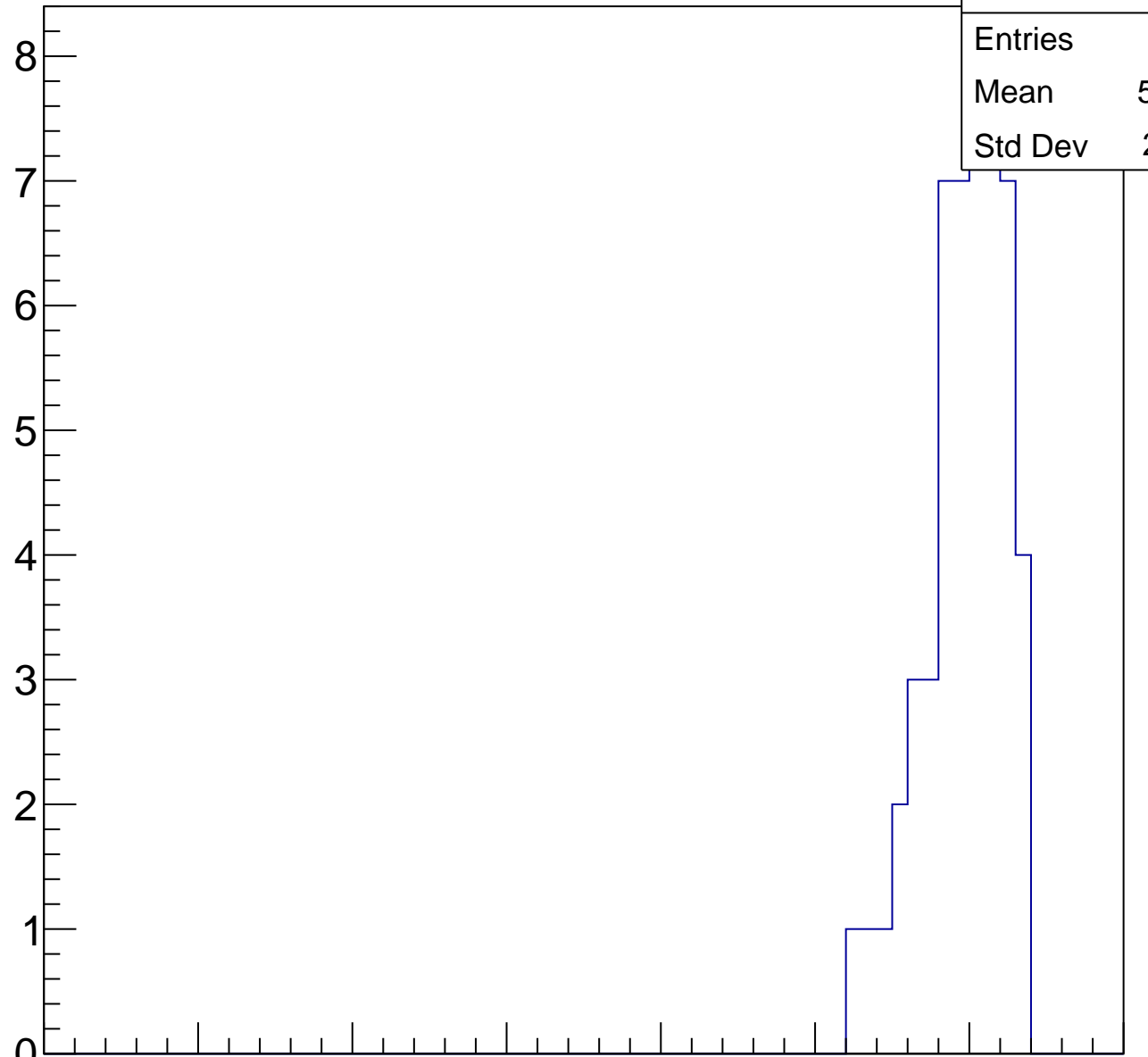
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	52
Mean	59.25
Std Dev	2.601

ampl

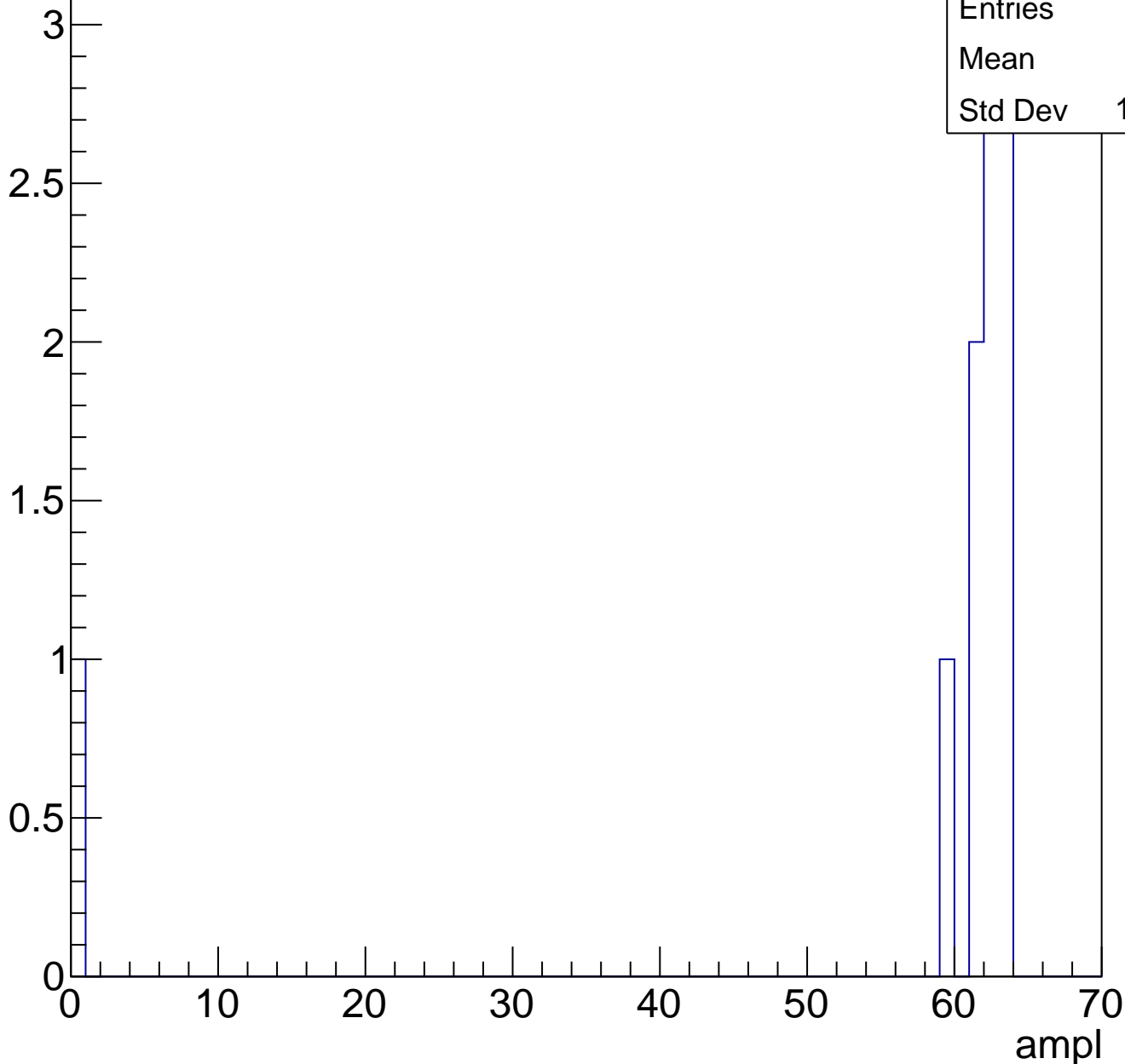
0 10 20 30 40 50 60 70



# B1L103S, U3-ch17, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U3-ch17, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	19
Mean	3.316
Std Dev	14.07

ampl

0 10 20 30 40 50 60 70

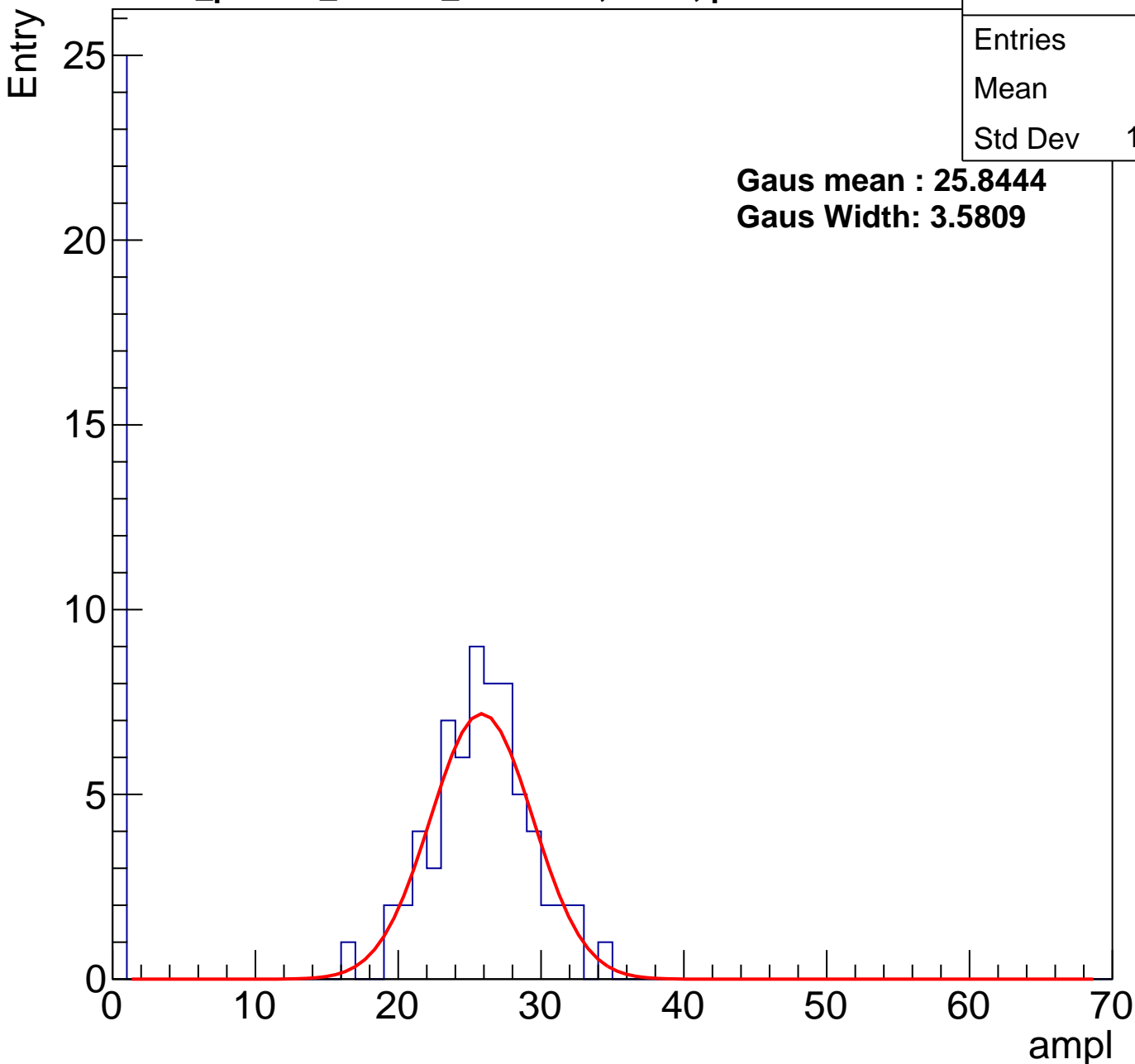
# B1L103S, U3-ch18, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	91
Mean	18.4
Std Dev	11.69

**Gaus mean : 25.8444**

**Gaus Width: 3.5809**



# B1L103S, U3-ch18, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	31.95
Std Dev	2.744

**Gaus mean : 32.2929**

**Gaus Width: 2.8649**

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

0

2

4

6

8

10

# B1L103S, U3-ch18, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	76
Mean	32.51
Std Dev	15.14

**Gaus mean : 39.6121**

**Gaus Width: 3.2240**

Entry

12

10

8

6

4

2

0

0

10

20

30

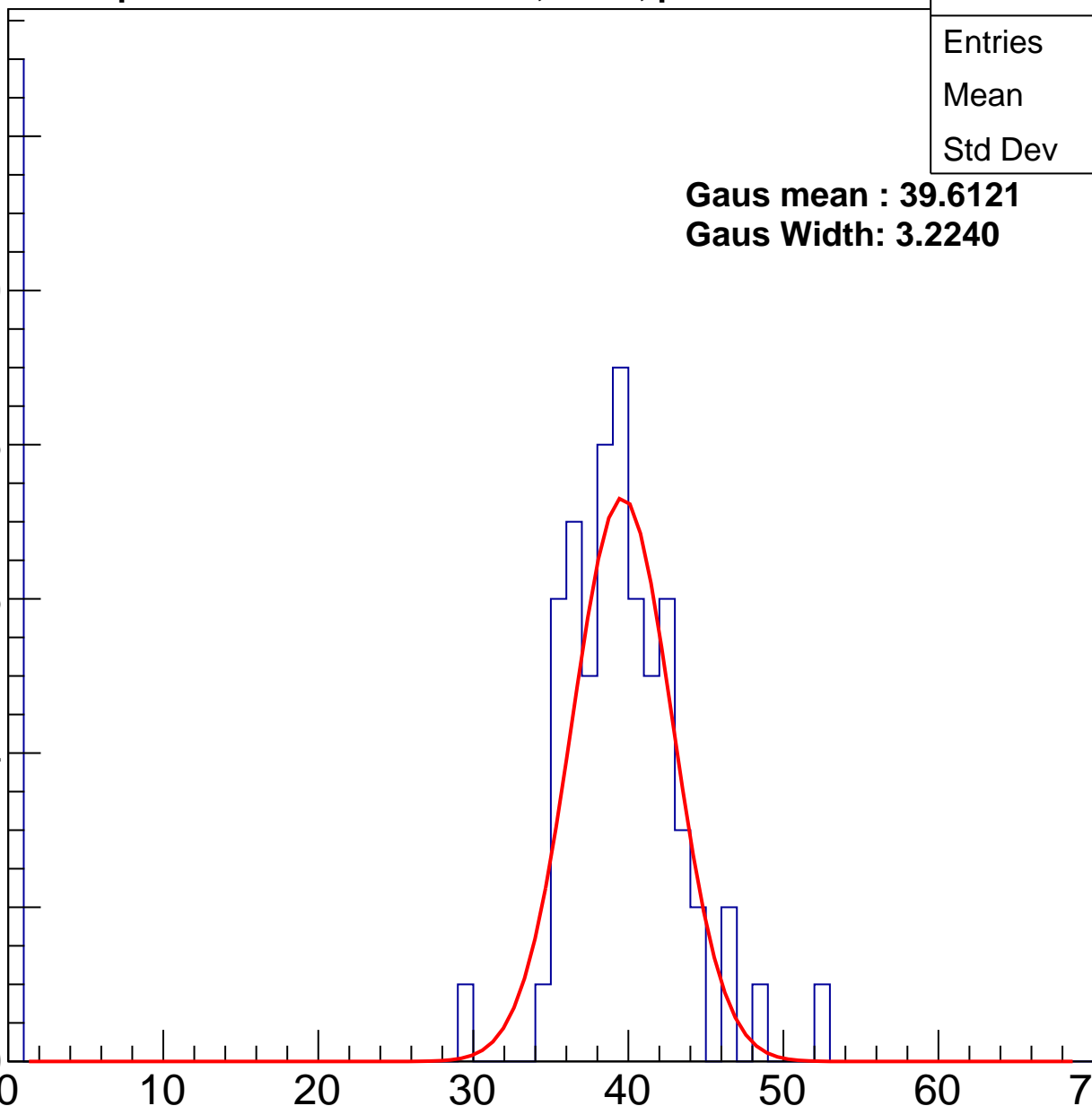
40

50

60

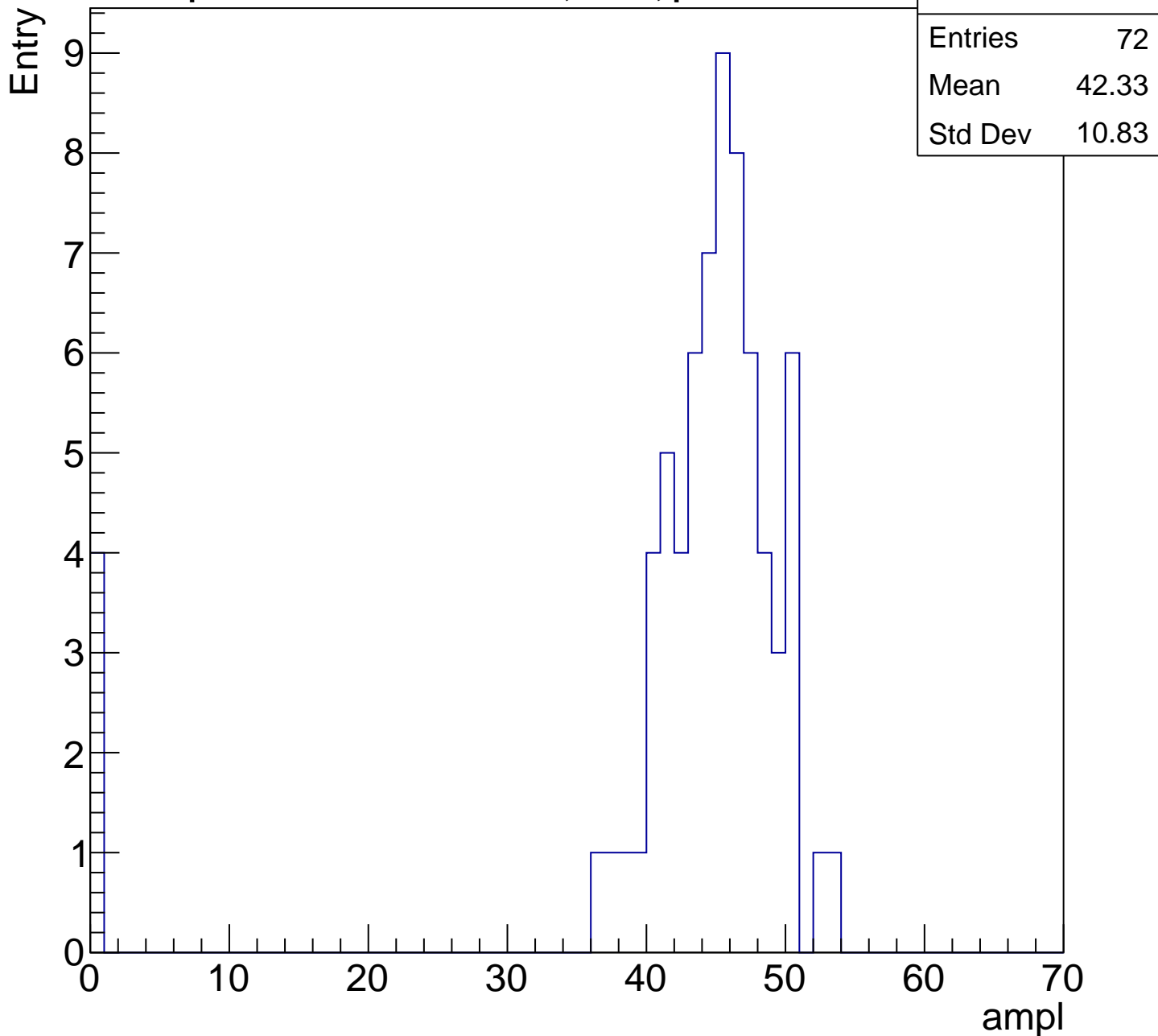
70

ampl



# B1L103S, U3-ch18, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

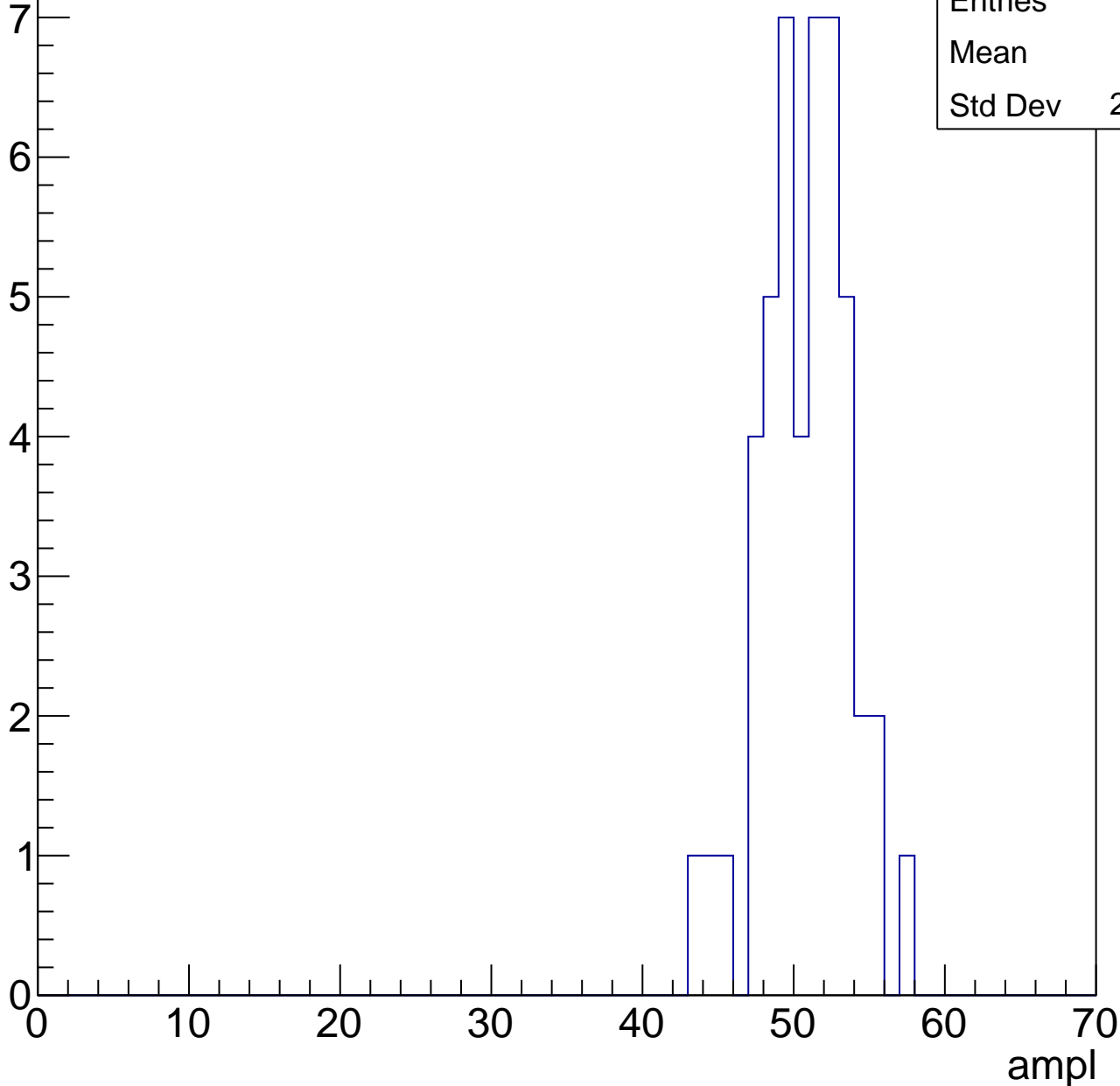


# B1L103S, U3-ch18, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

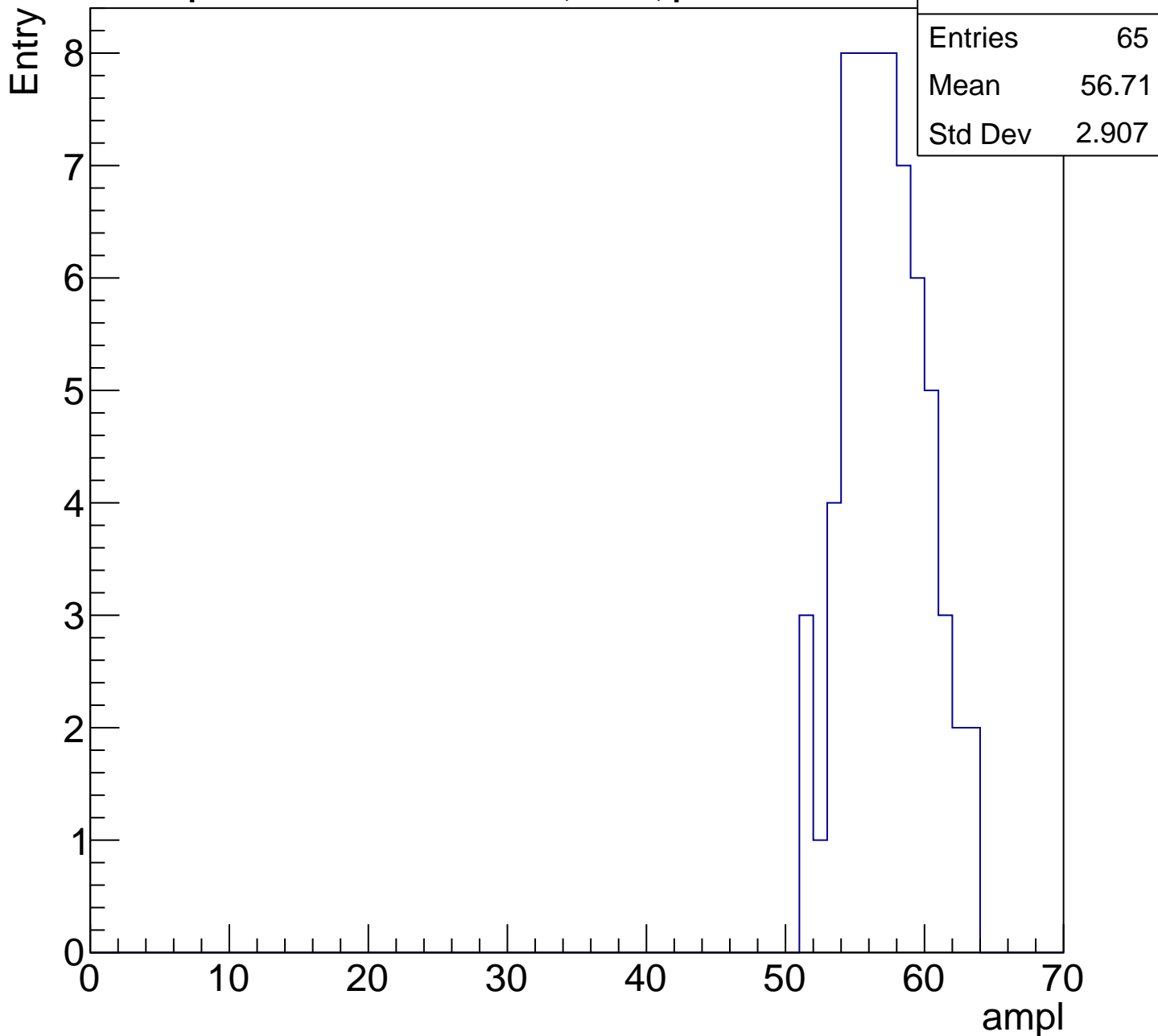
Entry

Entries	47
Mean	50.3
Std Dev	2.843



# B1L103S, U3-ch18, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

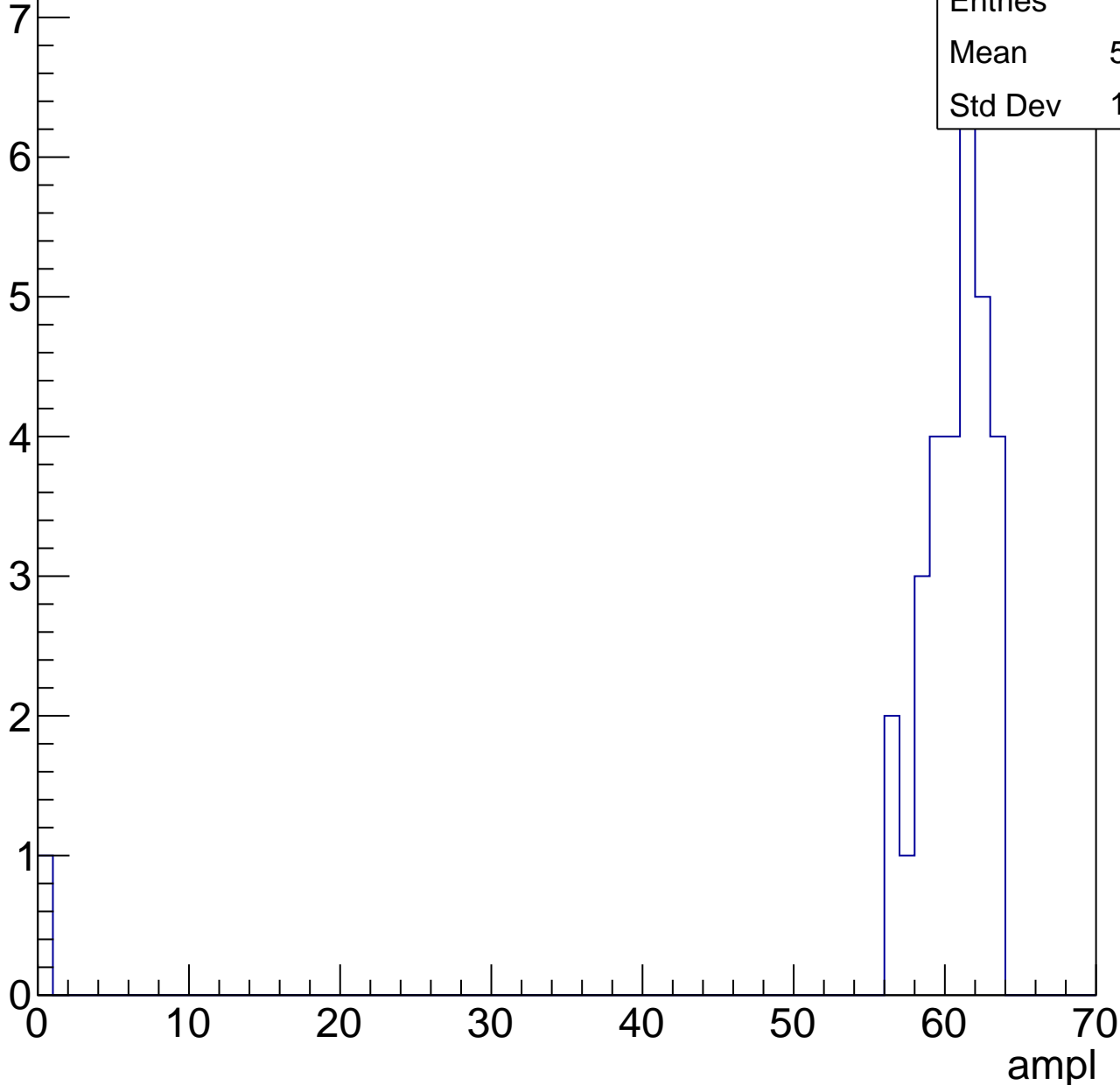


# B1L103S, U3-ch18, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	31
Mean	58.32
Std Dev	10.83



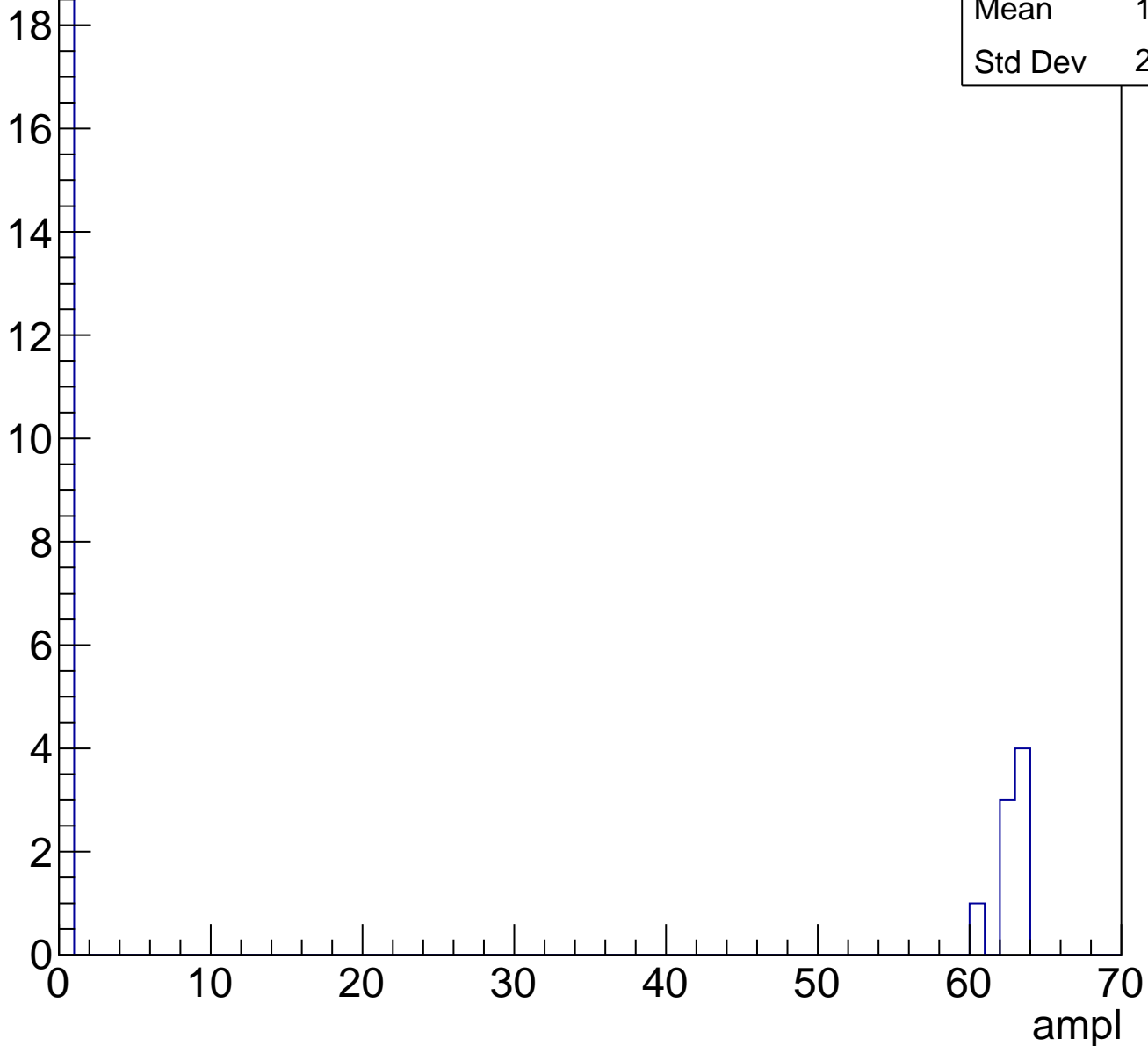


# B1L103S, U3-ch18, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	27
Mean	18.44
Std Dev	28.43

Entry



# B1L103S, U3-ch19, adc0

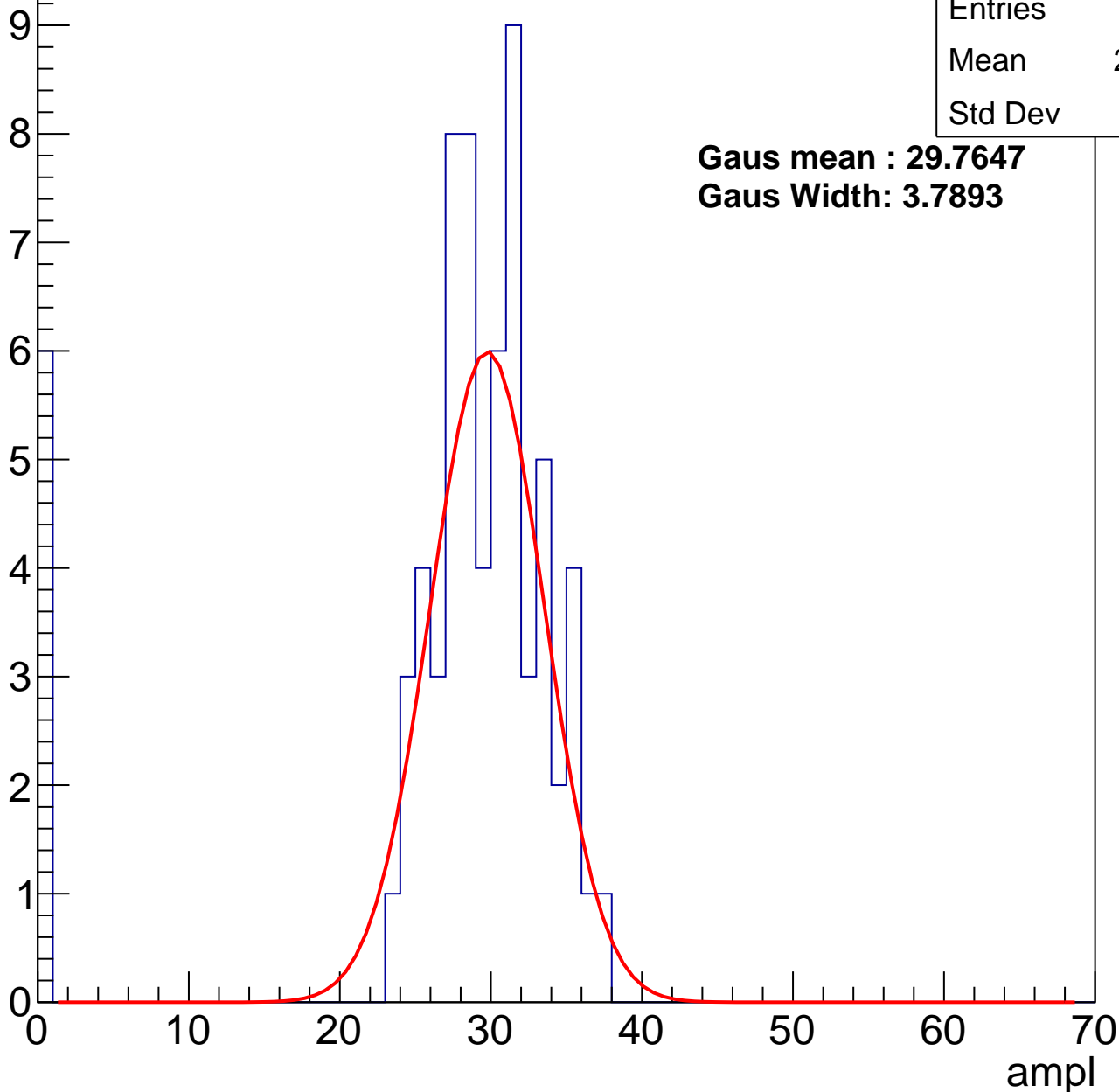
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	26.91
Std Dev	8.95

**Gaus mean : 29.7647**

**Gaus Width: 3.7893**



# B1L103S, U3-ch19, adc1

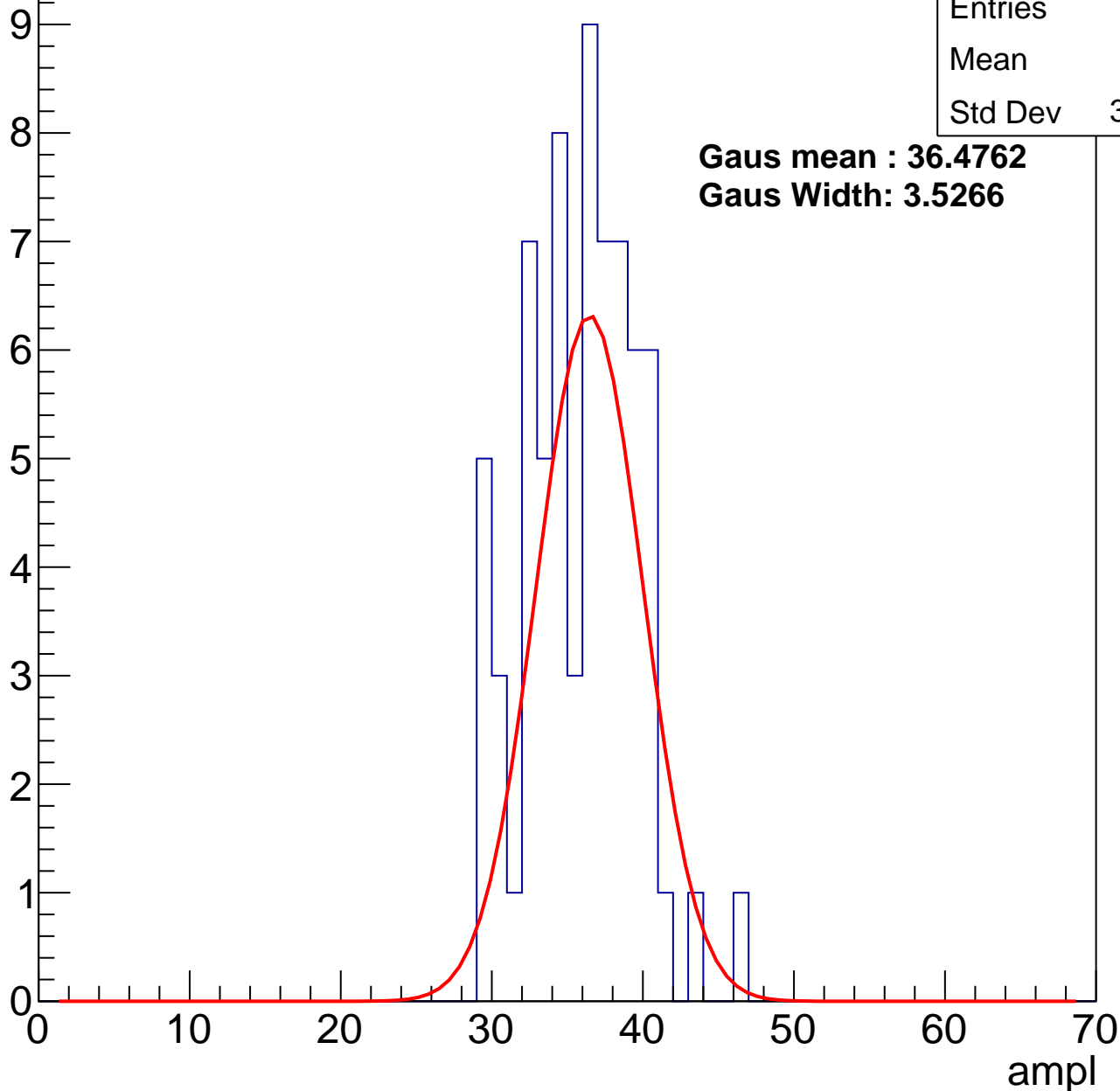
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	35.5
Std Dev	3.609

**Gaus mean : 36.4762**

**Gaus Width: 3.5266**



# B1L103S, U3-ch19, adc2

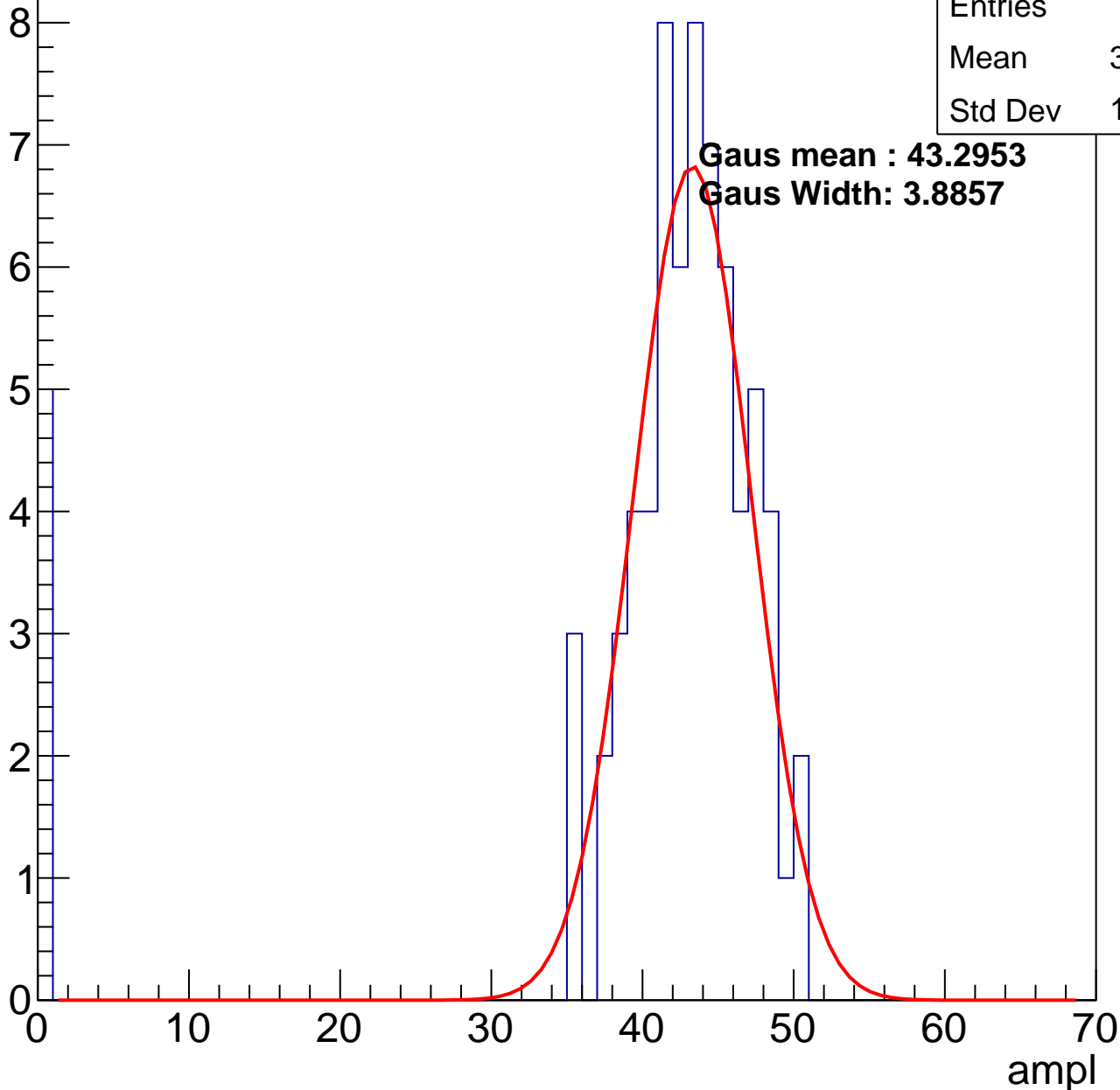
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	72
Mean	39.88
Std Dev	11.43

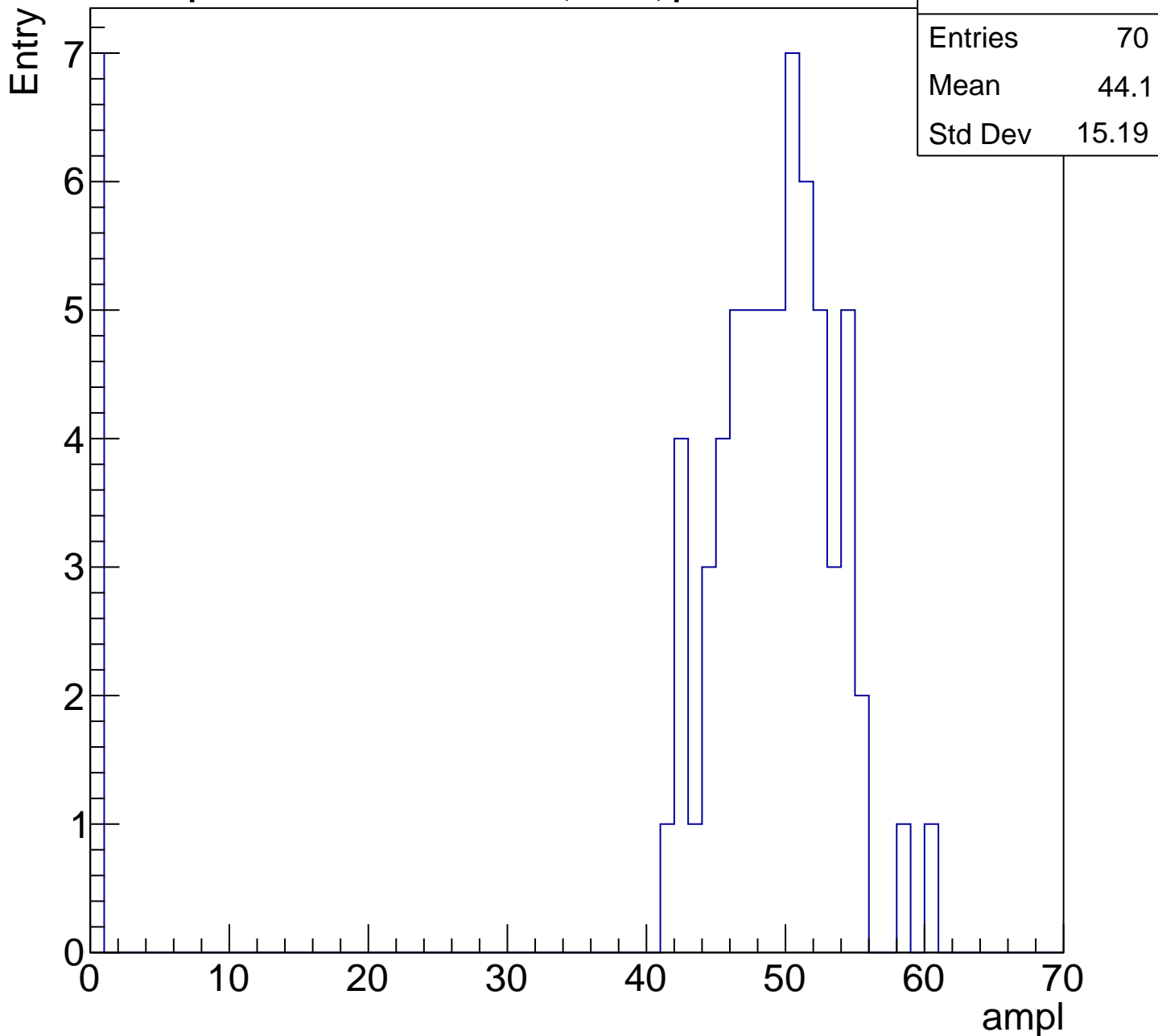
**Gaus mean : 43.2953**

**Gaus Width: 3.8857**



# B1L103S, U3-ch19, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

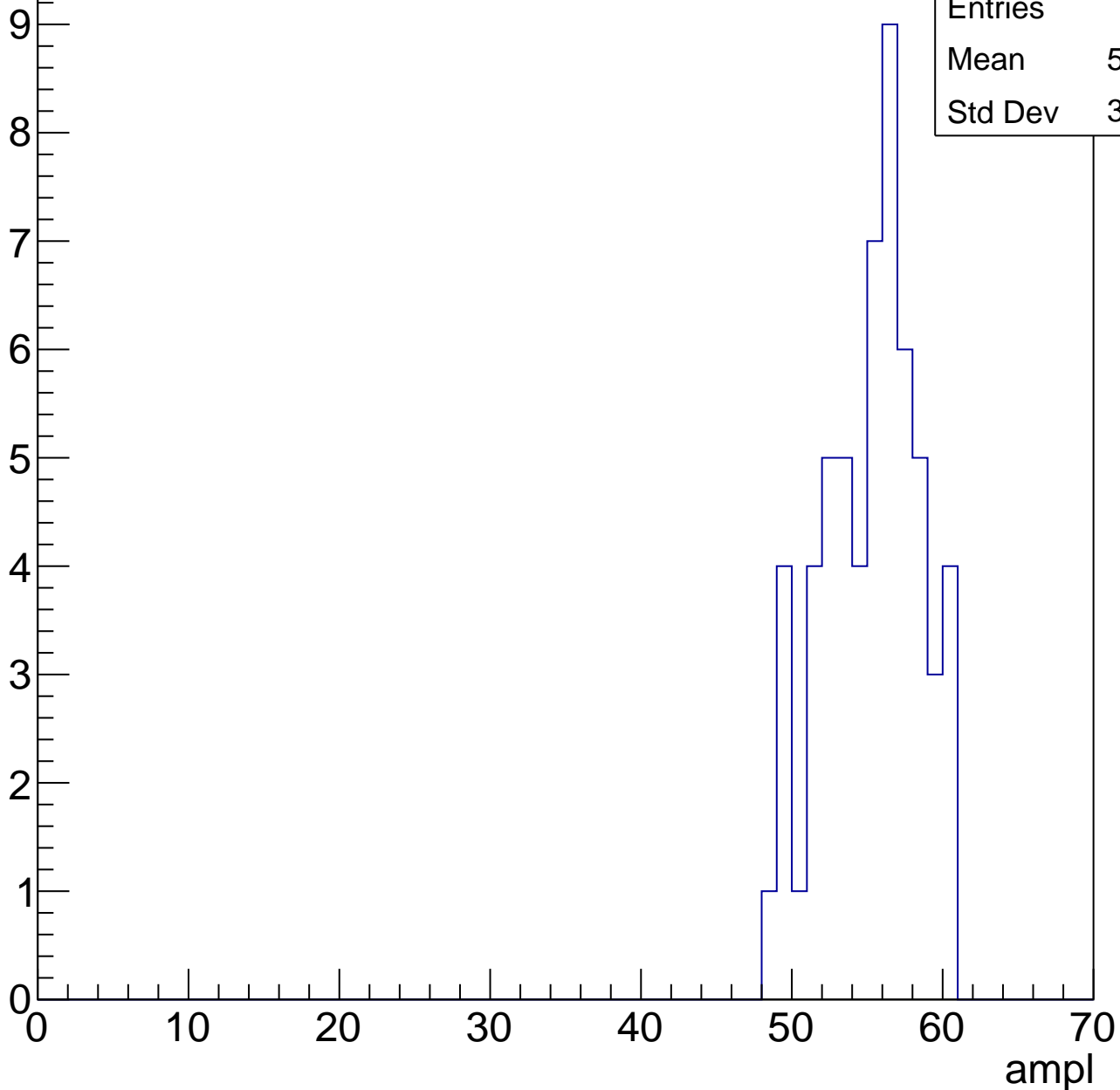


# B1L103S, U3-ch19, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	54.78
Std Dev	3.146

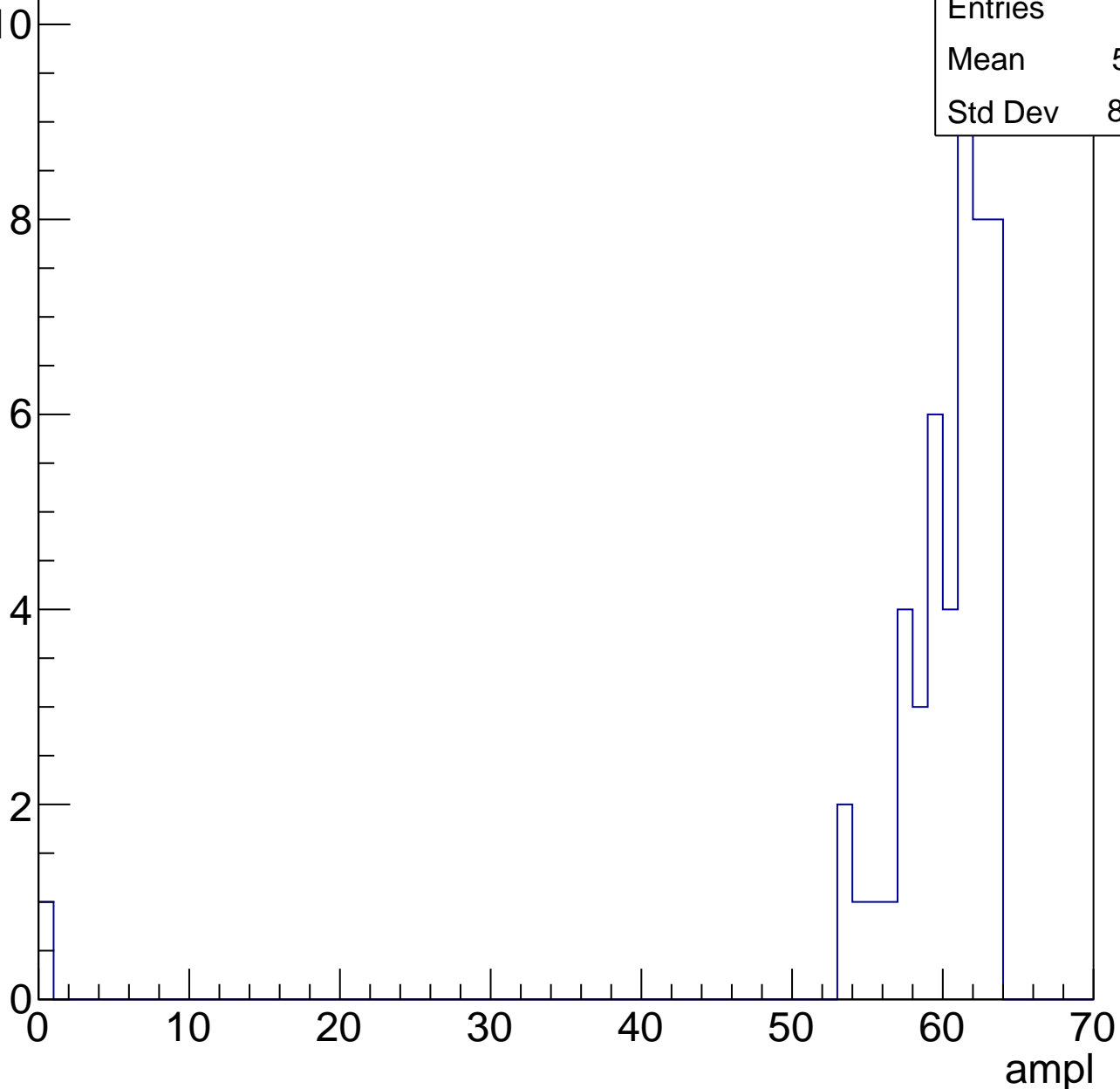


# B1L103S, U3-ch19, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

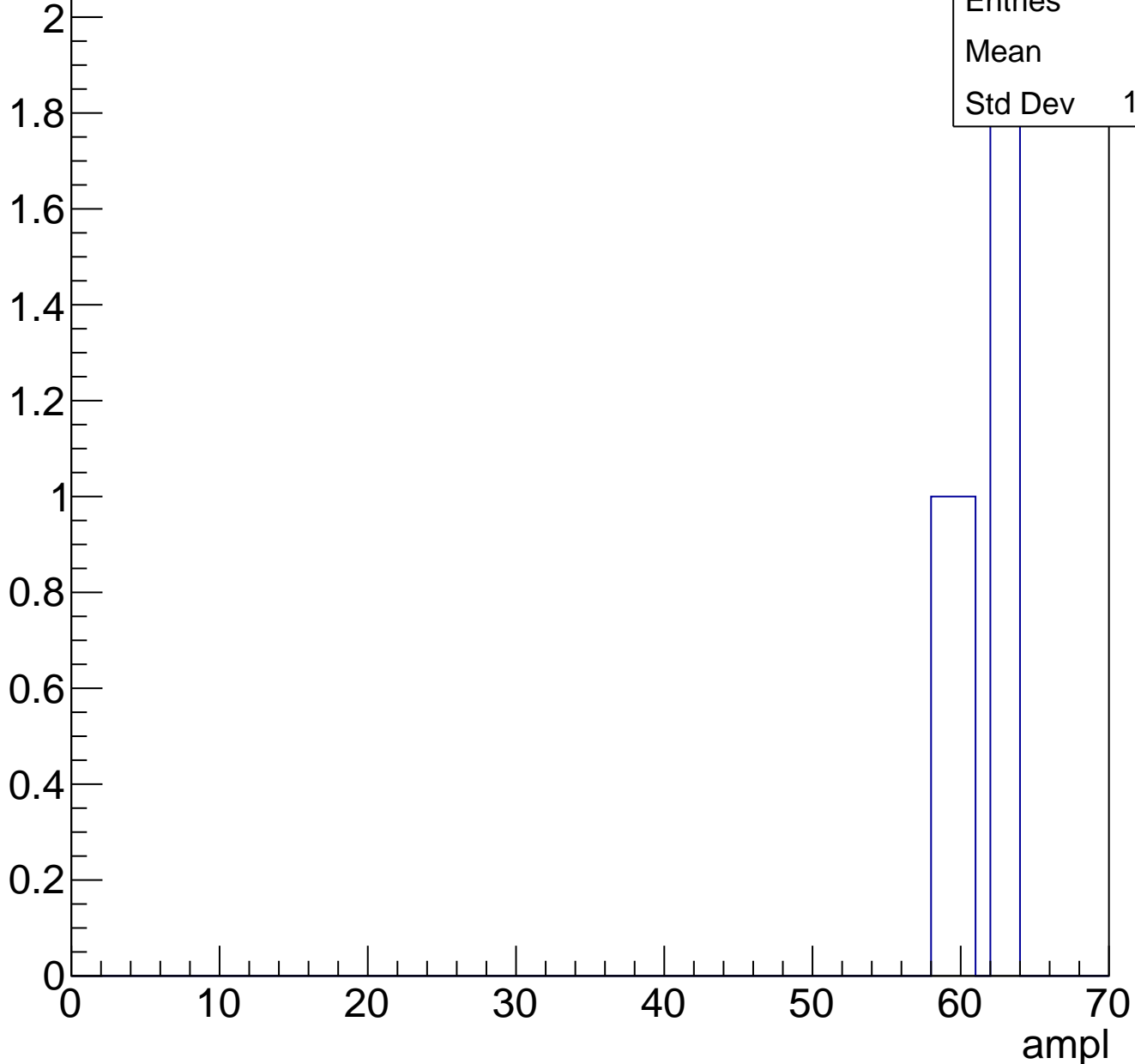
Entries	49
Mean	58.71
Std Dev	8.878



# B1L103S, U3-ch19, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U3-ch19, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U3-ch20, adc0

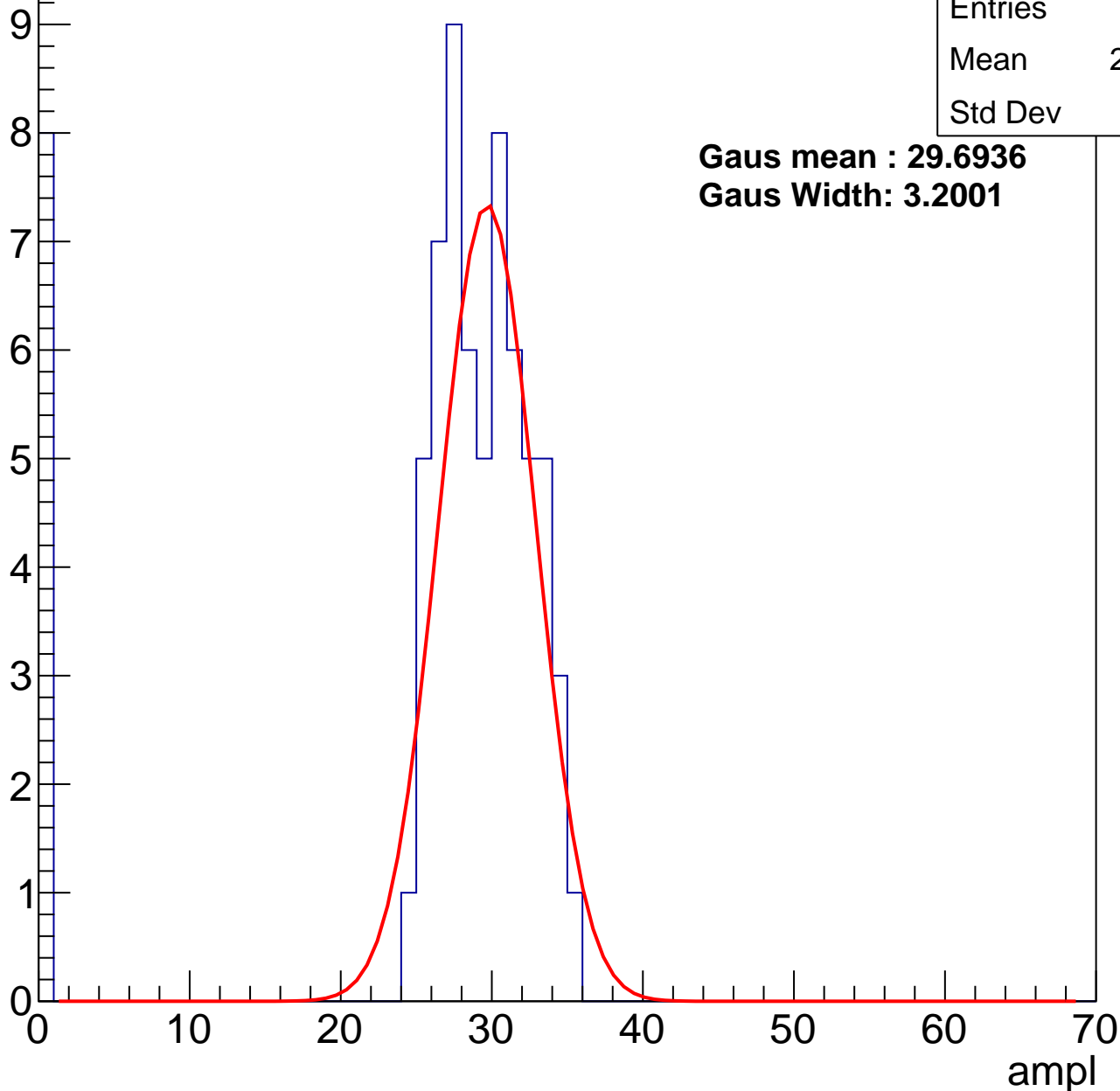
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	25.72
Std Dev	9.68

**Gaus mean : 29.6936**

**Gaus Width: 3.2001**



# B1L103S, U3-ch20, adc1

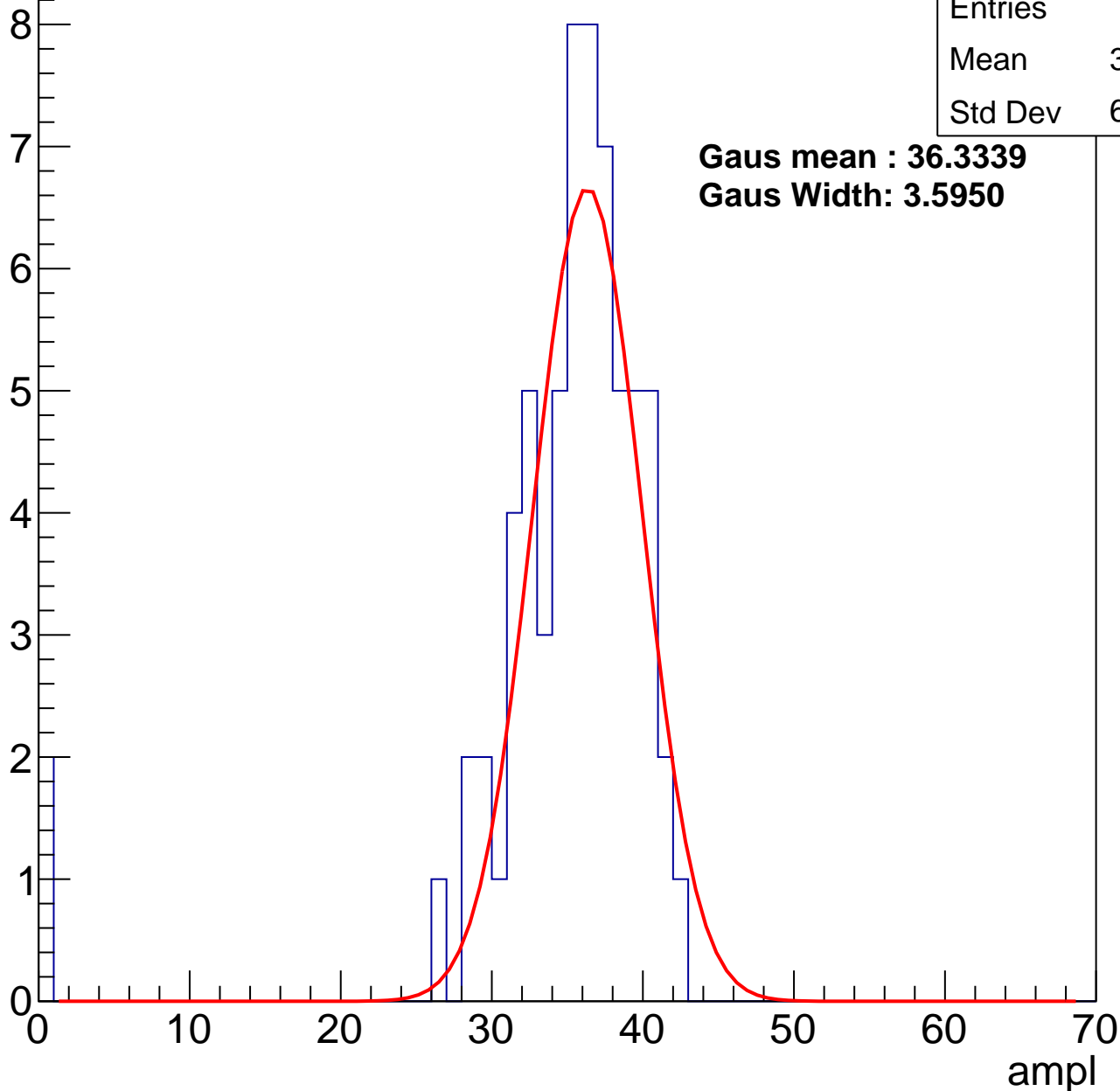
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	34.23
Std Dev	6.984

**Gaus mean : 36.3339**

**Gaus Width: 3.5950**



# B1L103S, U3-ch20, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	80
Mean	33.66
Std Dev	16.54

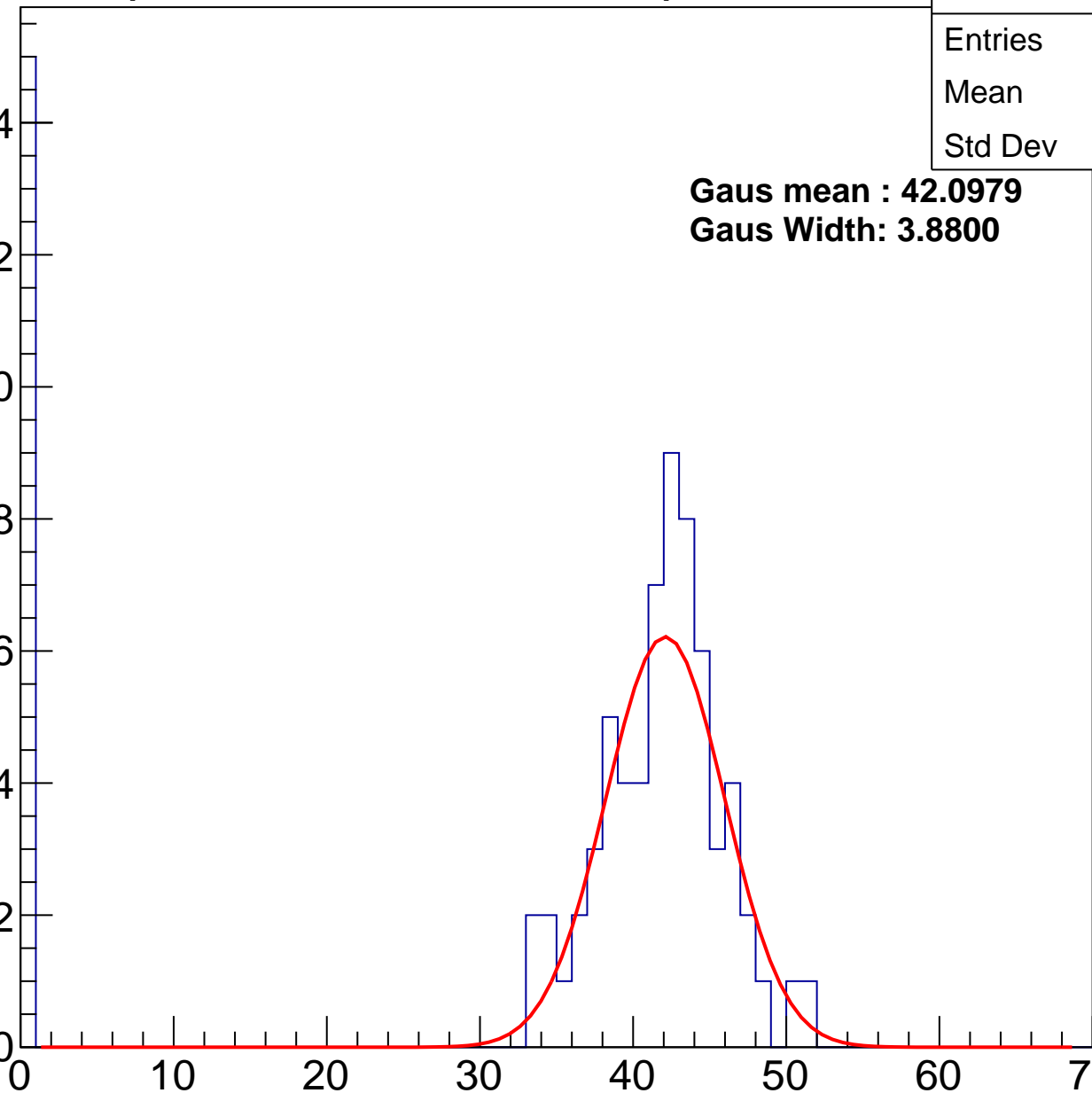
**Gaus mean : 42.0979**

**Gaus Width: 3.8800**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

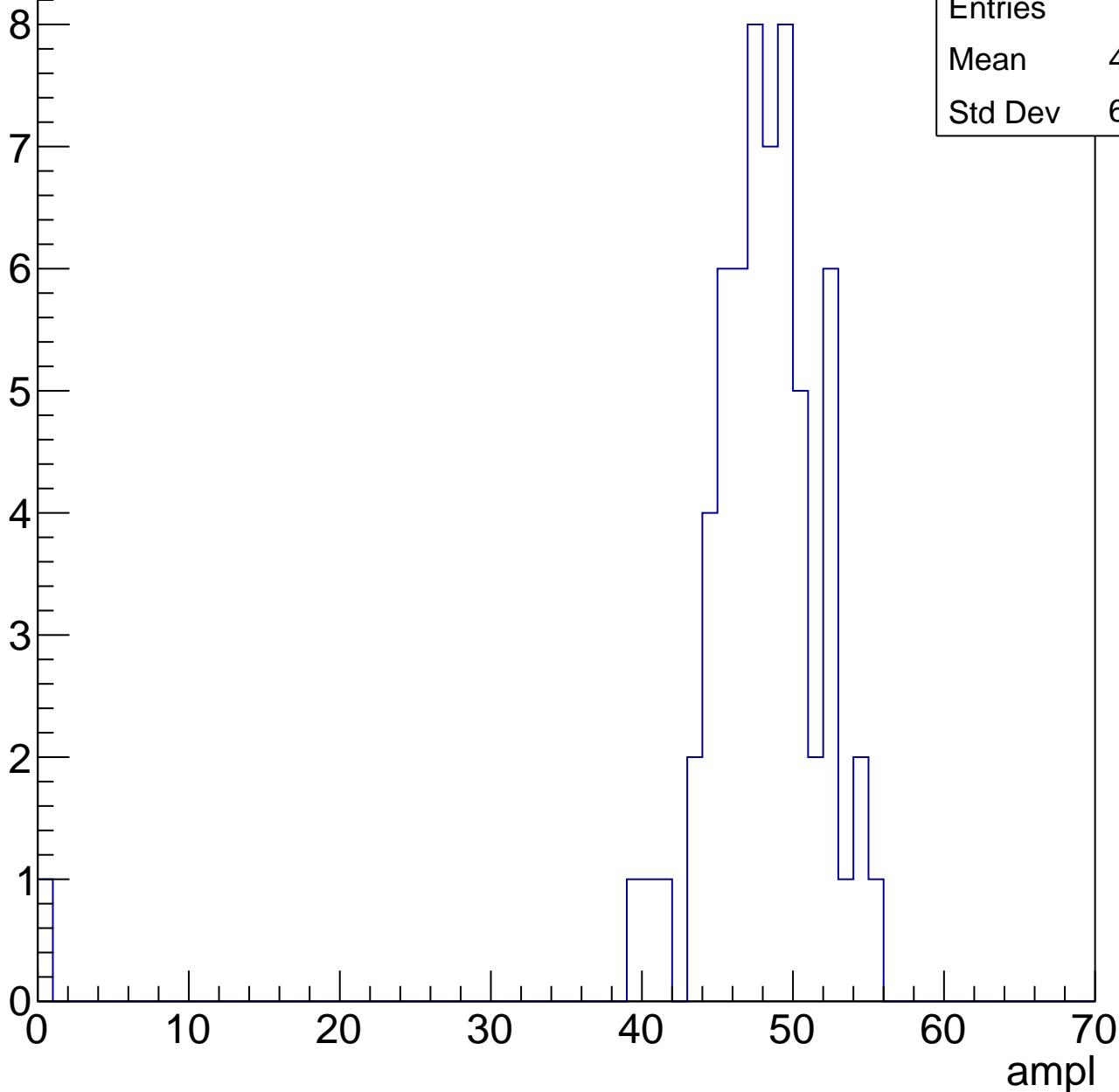


# B1L103S, U3-ch20, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	46.97
Std Dev	6.863

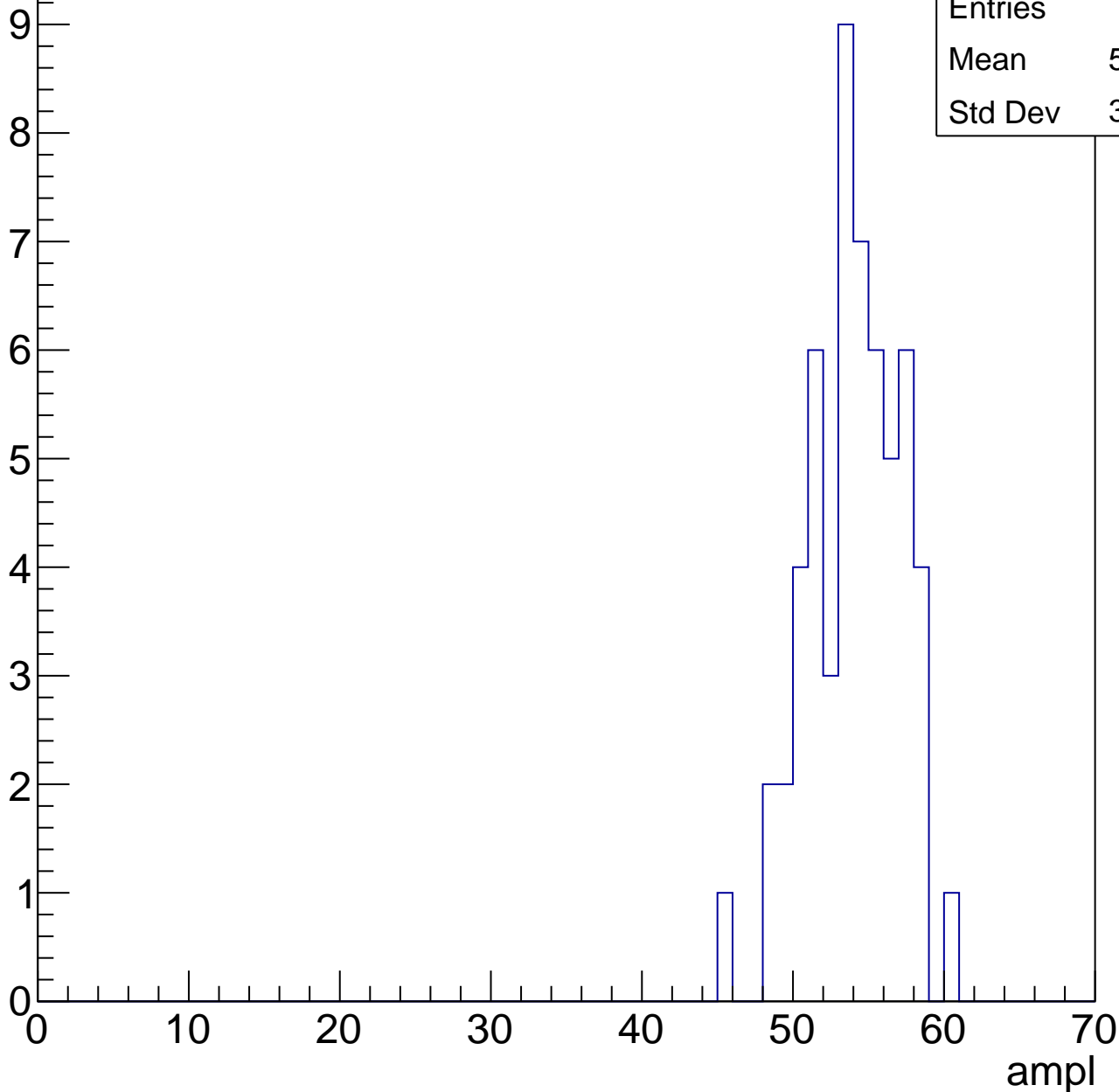


# B1L103S, U3-ch20, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	56
Mean	53.57
Std Dev	3.023

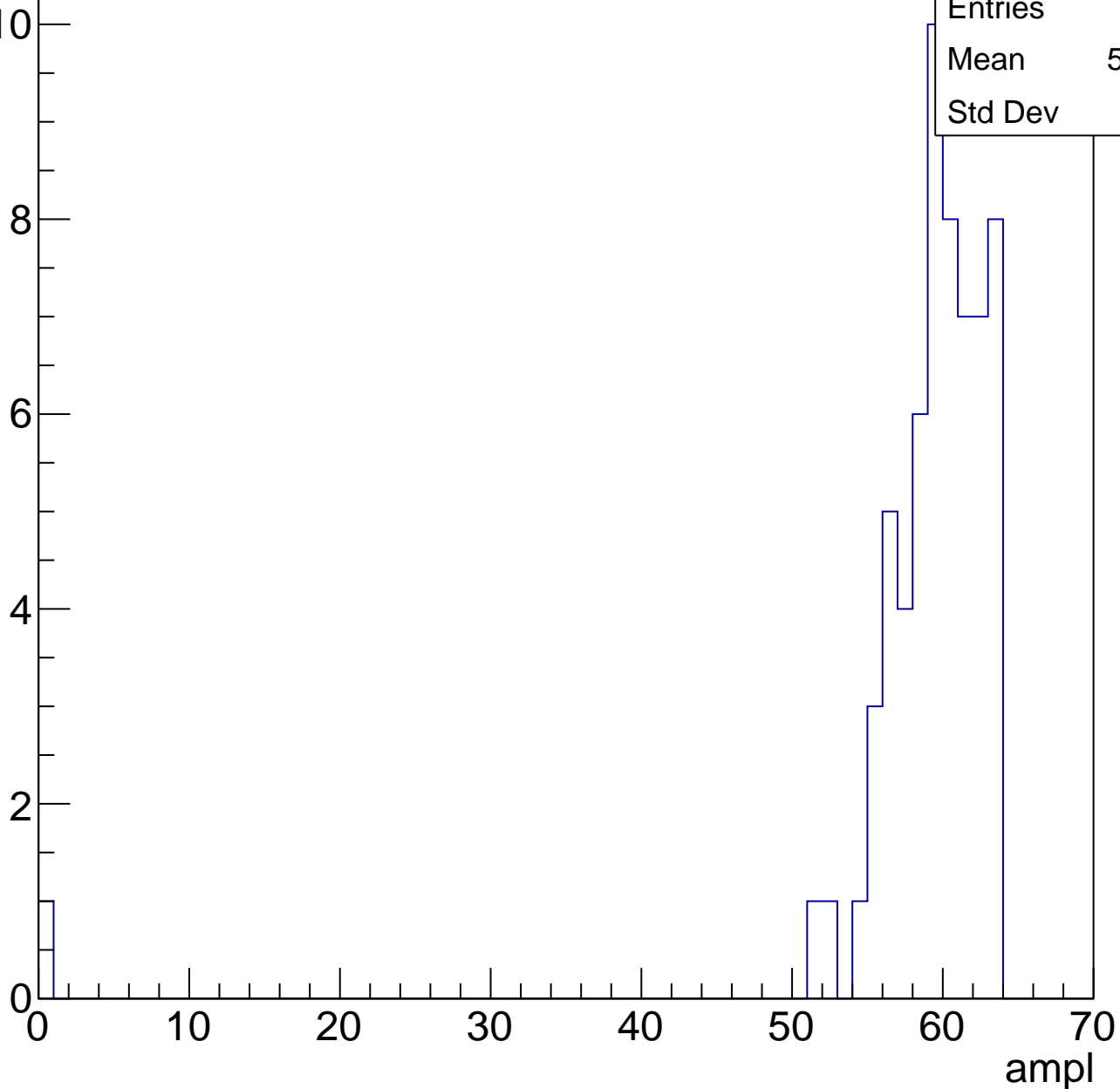


# B1L103S, U3-ch20, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	58.27
Std Dev	7.96



# B1L103S, U3-ch20, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

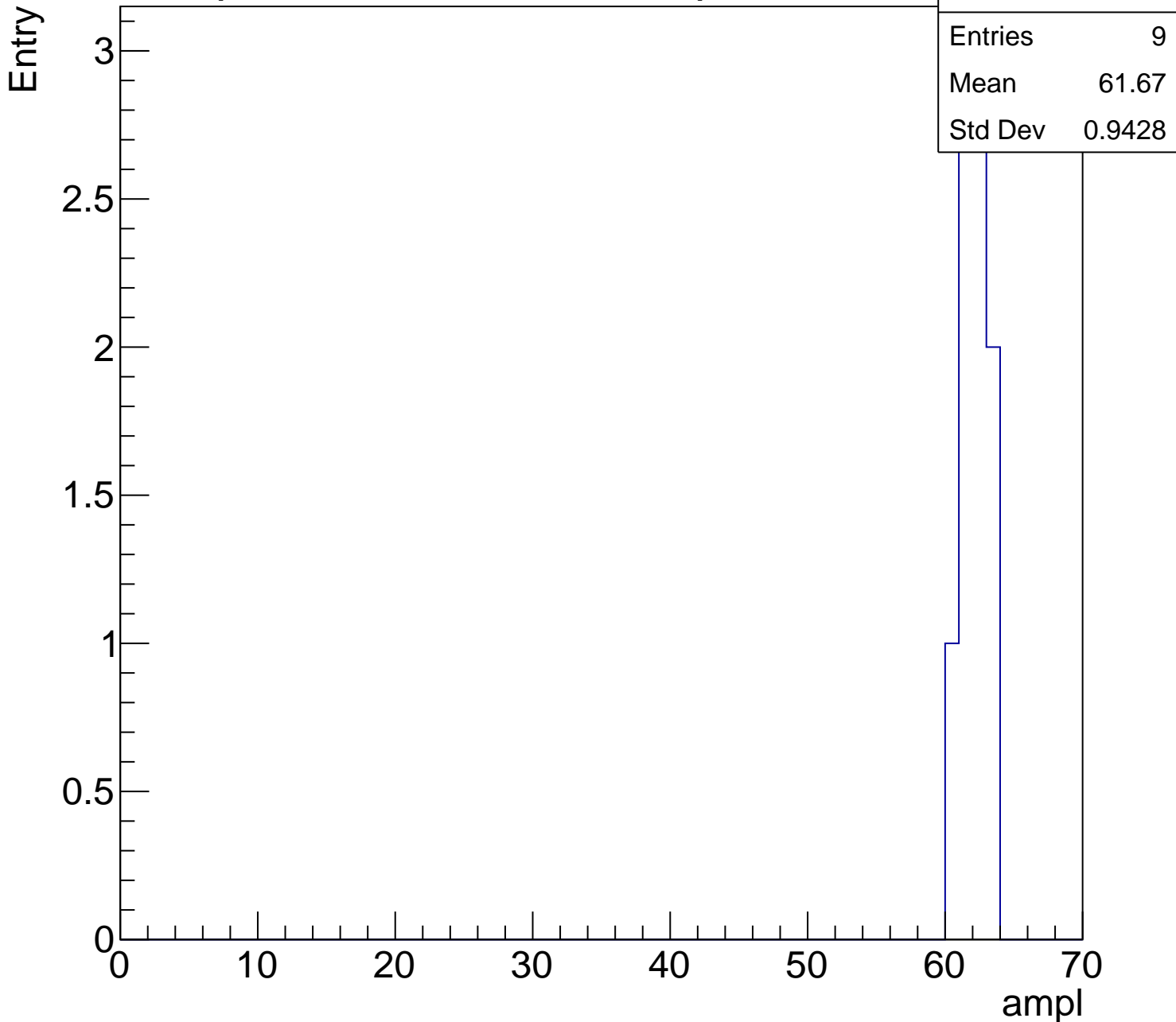
9

Mean

61.67

Std Dev

0.9428





# B1L103S, U3-ch20, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	19
Mean	0
Std Dev	0

# B1L103S, U3-ch21, adc0

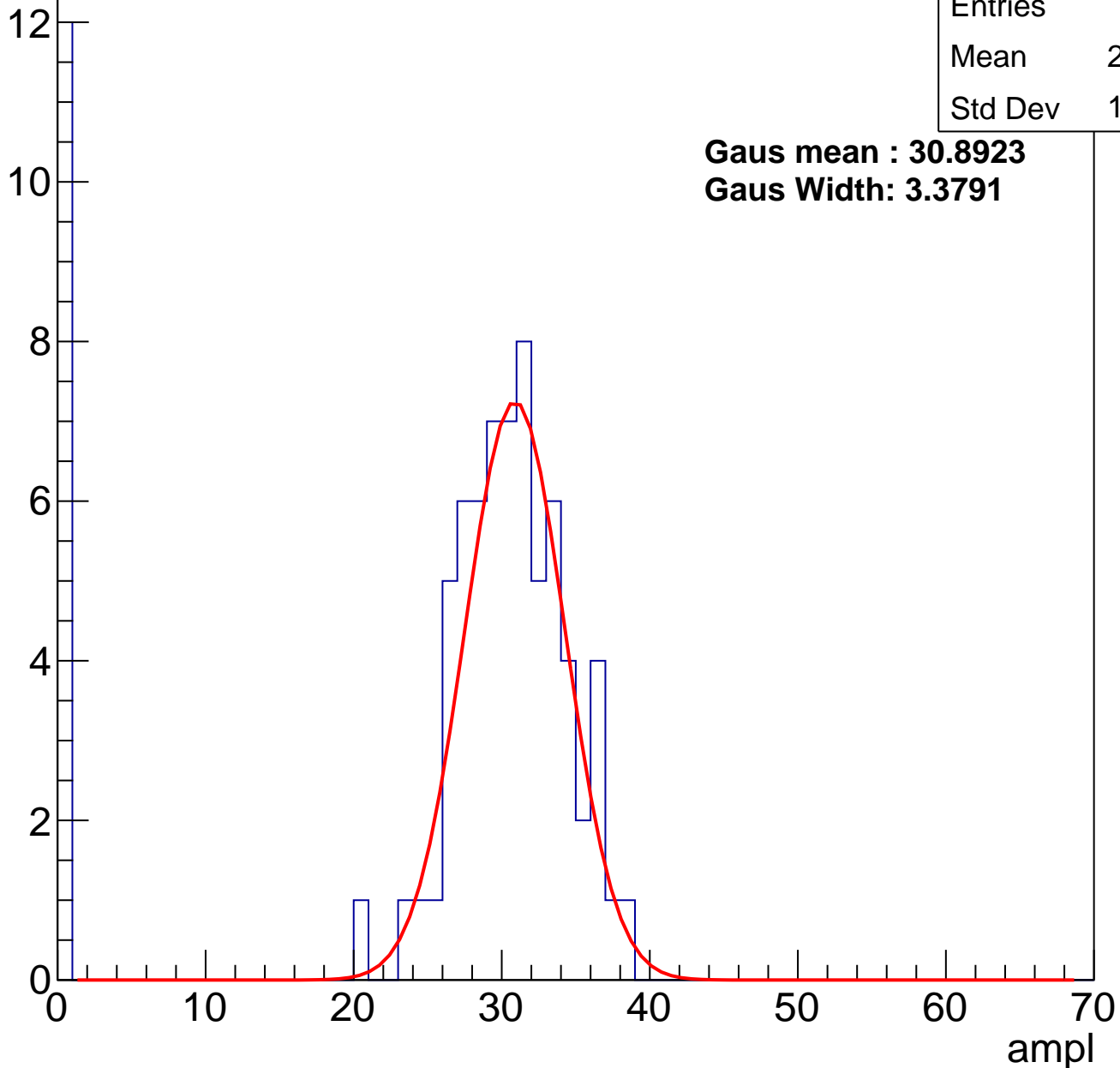
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	78
Mean	25.59
Std Dev	11.39

**Gaus mean : 30.8923**

**Gaus Width: 3.3791**

Entry



# B1L103S, U3-ch21, adc1

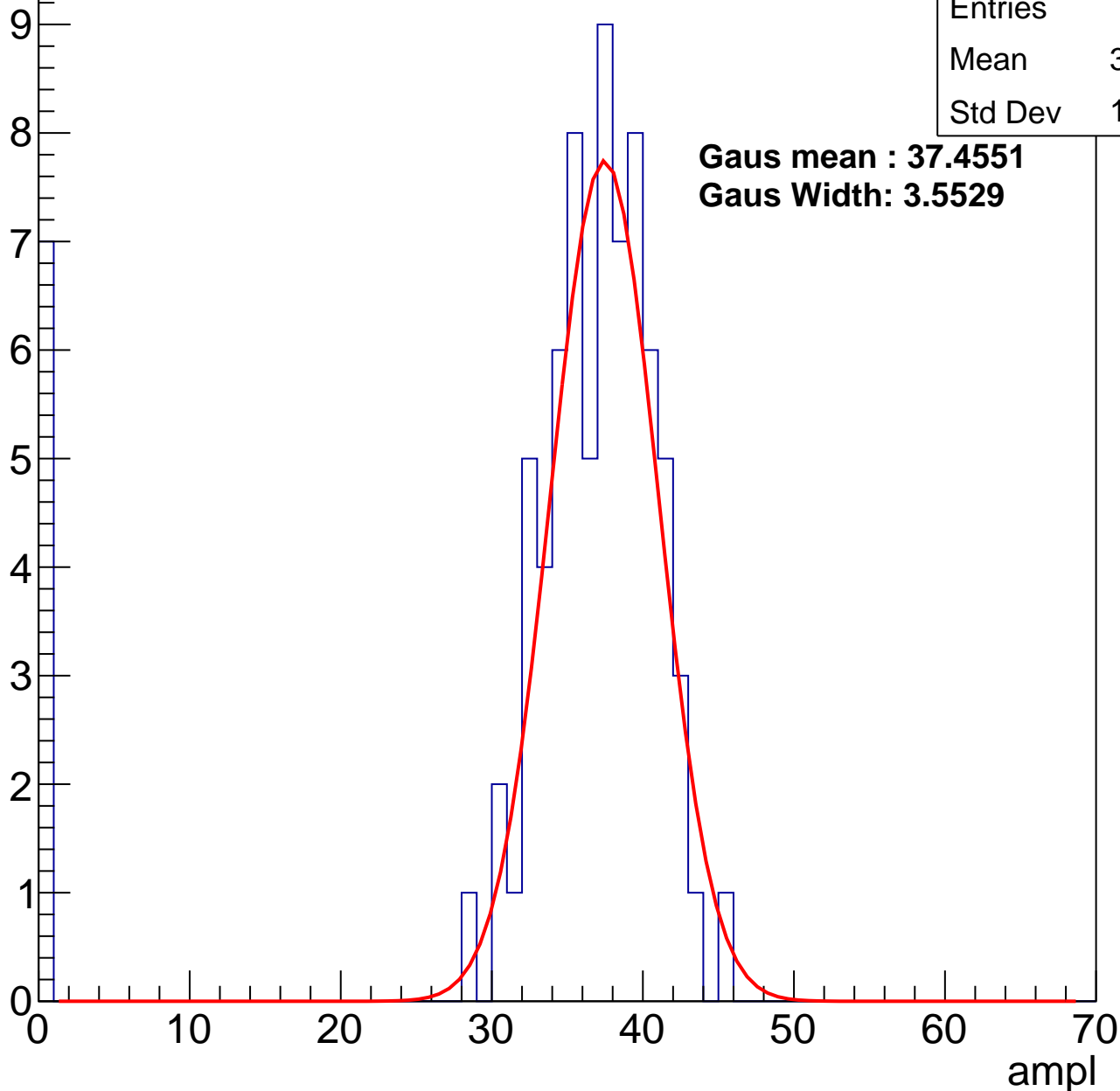
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	79
Mean	33.48
Std Dev	10.94

**Gaus mean : 37.4551**

**Gaus Width: 3.5529**



# B1L103S, U3-ch21, adc2

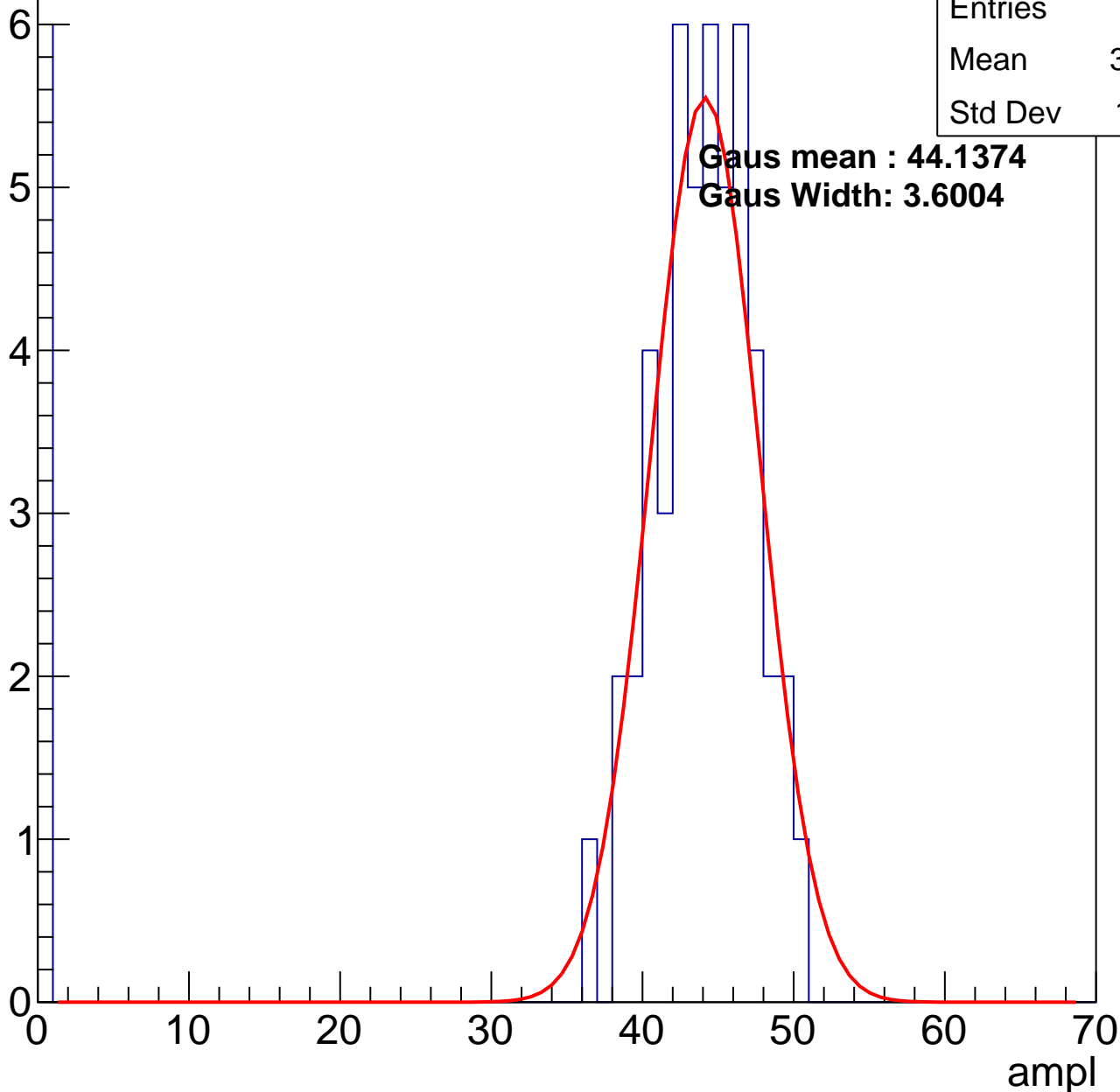
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	55
Mean	38.85
Std Dev	13.91

**Gaus mean : 44.1374**

**Gaus Width: 3.6004**

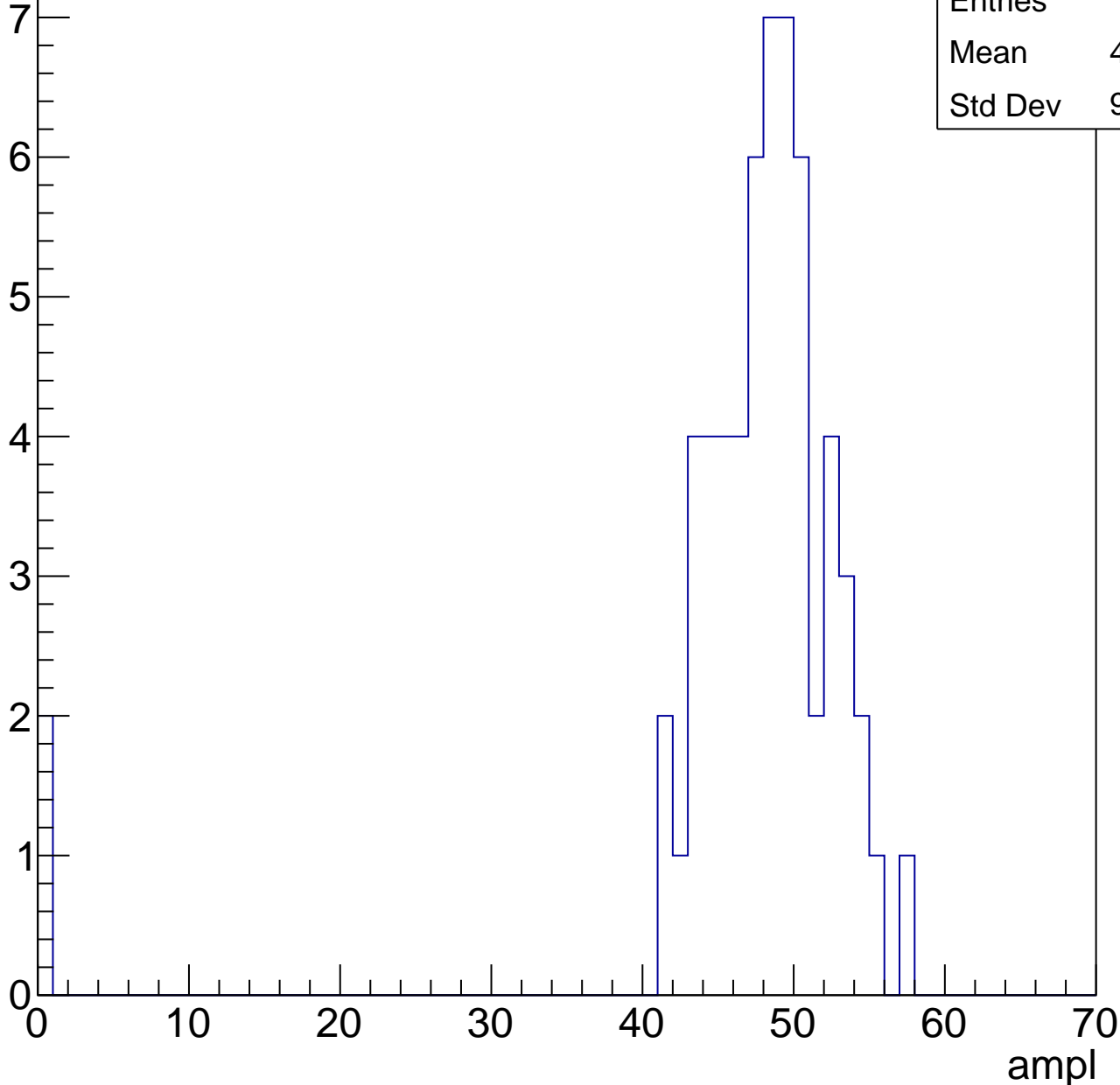


# B1L103S, U3-ch21, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	60
Mean	46.43
Std Dev	9.316

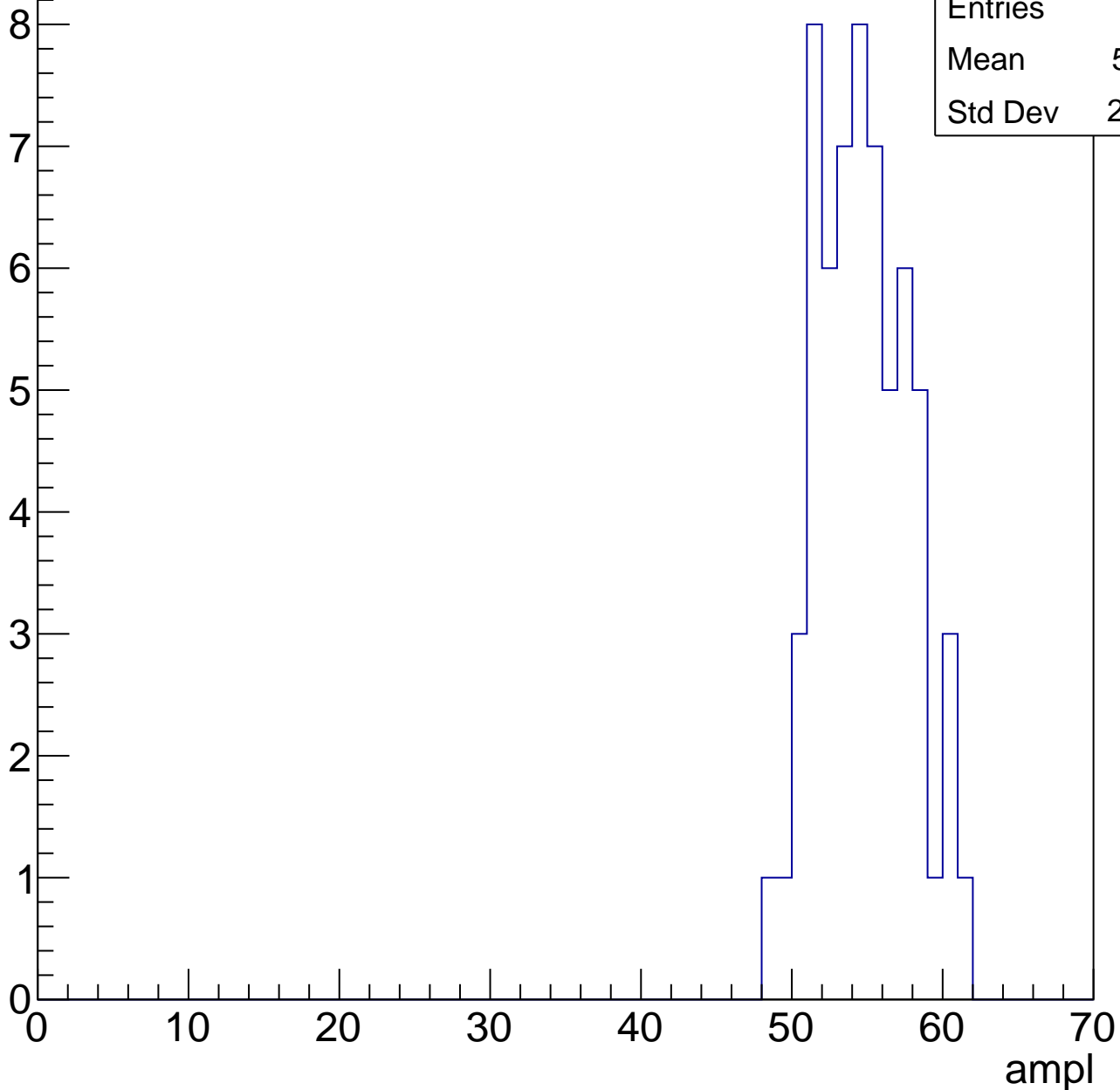


# B1L103S, U3-ch21, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	54.31
Std Dev	2.976



# B1L103S, U3-ch21, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

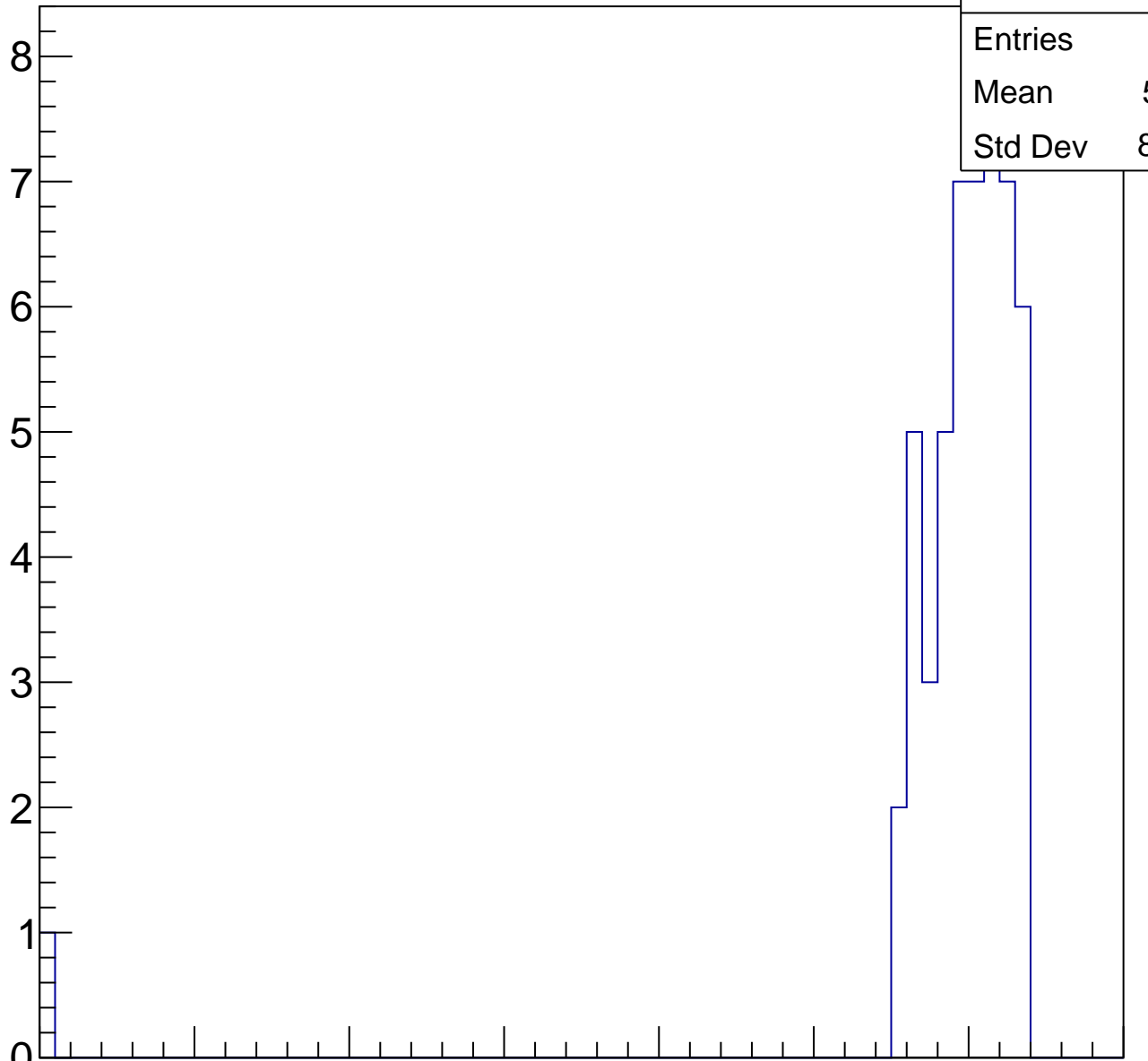
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	58.51
Std Dev	8.587

ampl

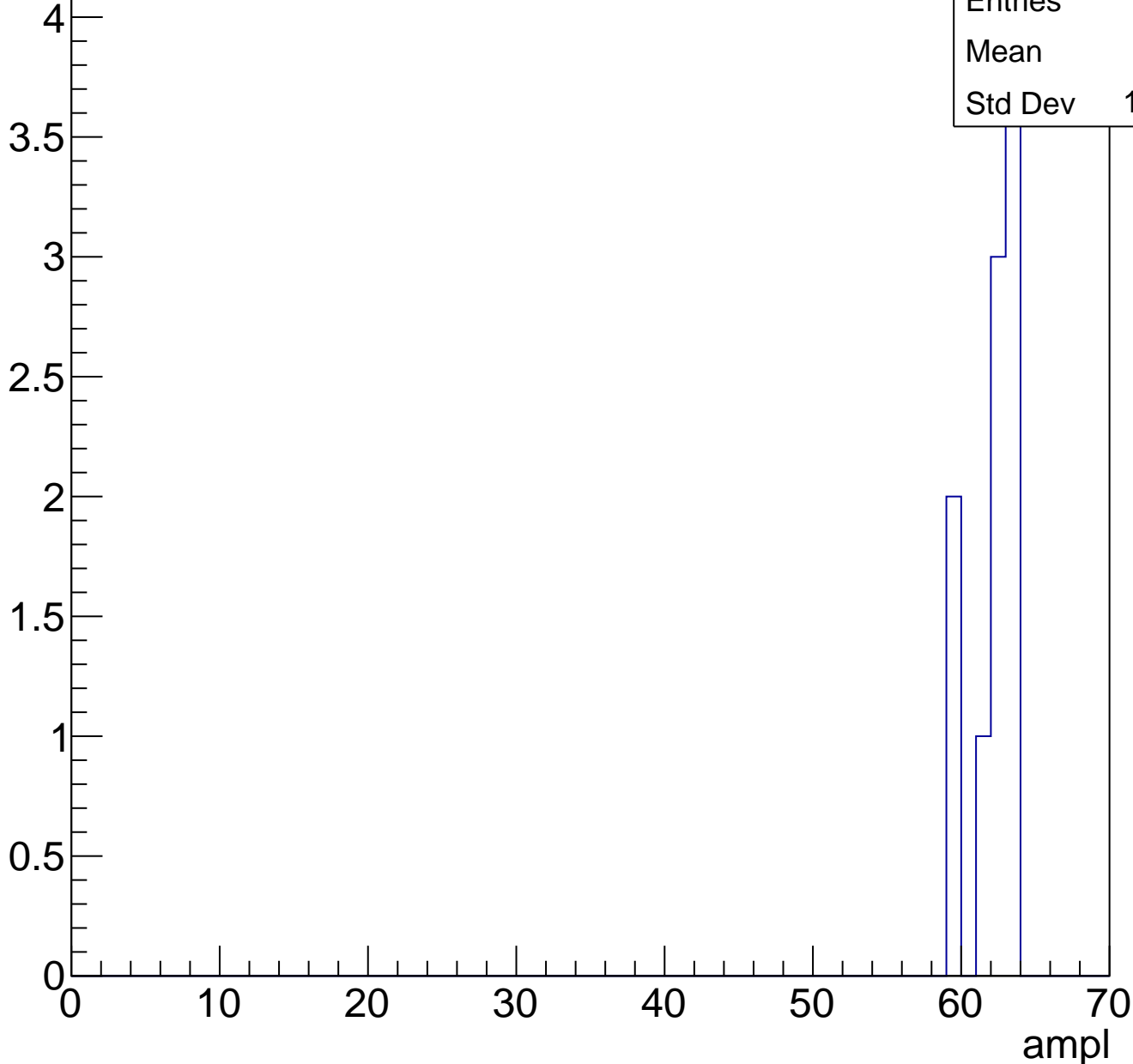
0 10 20 30 40 50 60 70



# B1L103S, U3-ch21, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	10
Mean	61.7
Std Dev	1.487



# B1L103S, U3-ch21, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	18
Mean	0
Std Dev	0

ampl

# B1L103S, U3-ch22, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	109
Mean	26.06
Std Dev	8.646

**Gaus mean : 28.9916**

**Gaus Width: 4.0178**

Entry

10  
8  
6  
4  
2  
0

ampl

0

10

20

30

40

50

60

70

# B1L103S, U3-ch22, adc1

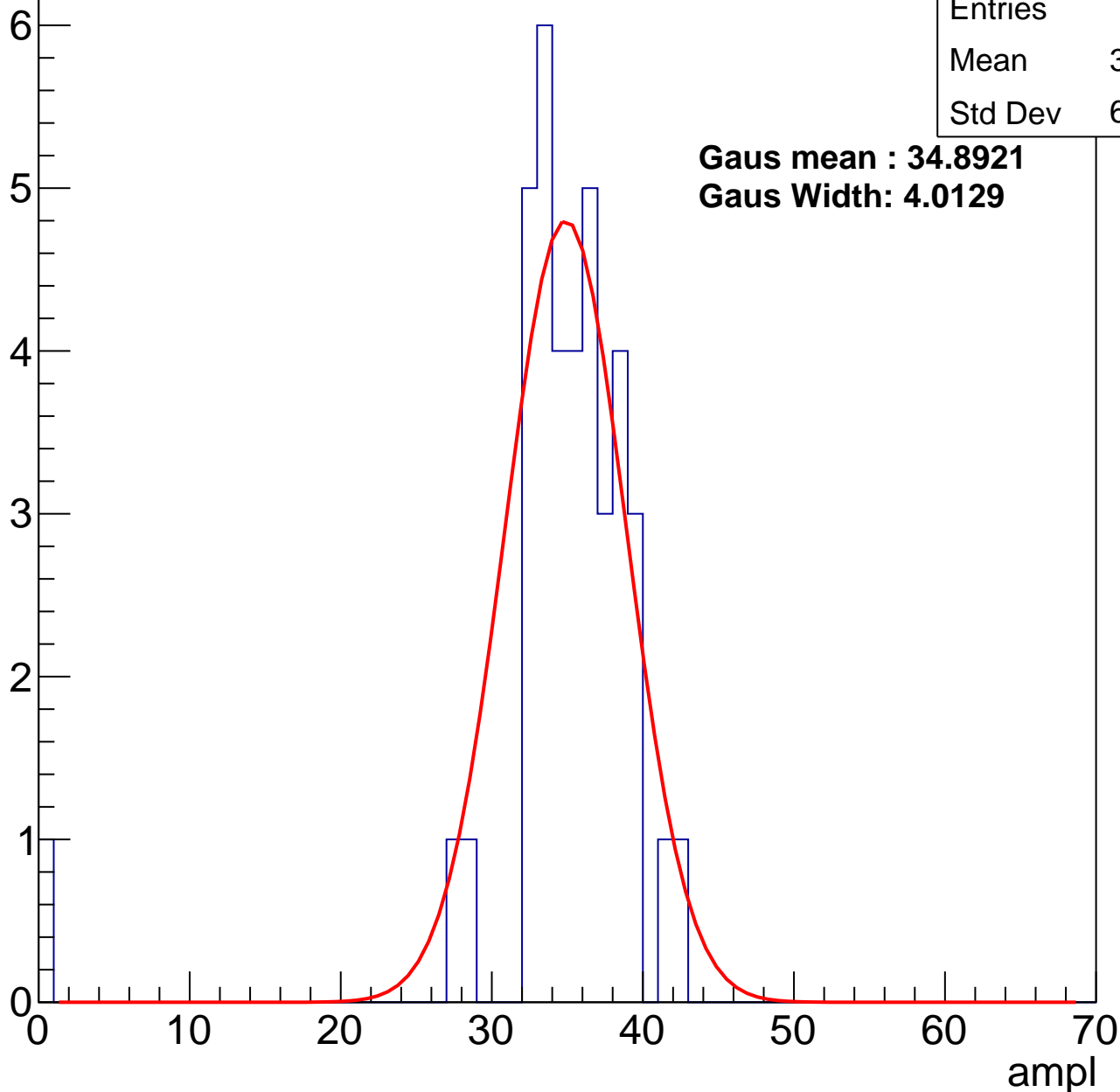
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	39
Mean	34.15
Std Dev	6.343

**Gaus mean : 34.8921**

**Gaus Width: 4.0129**



# B1L103S, U3-ch22, adc2

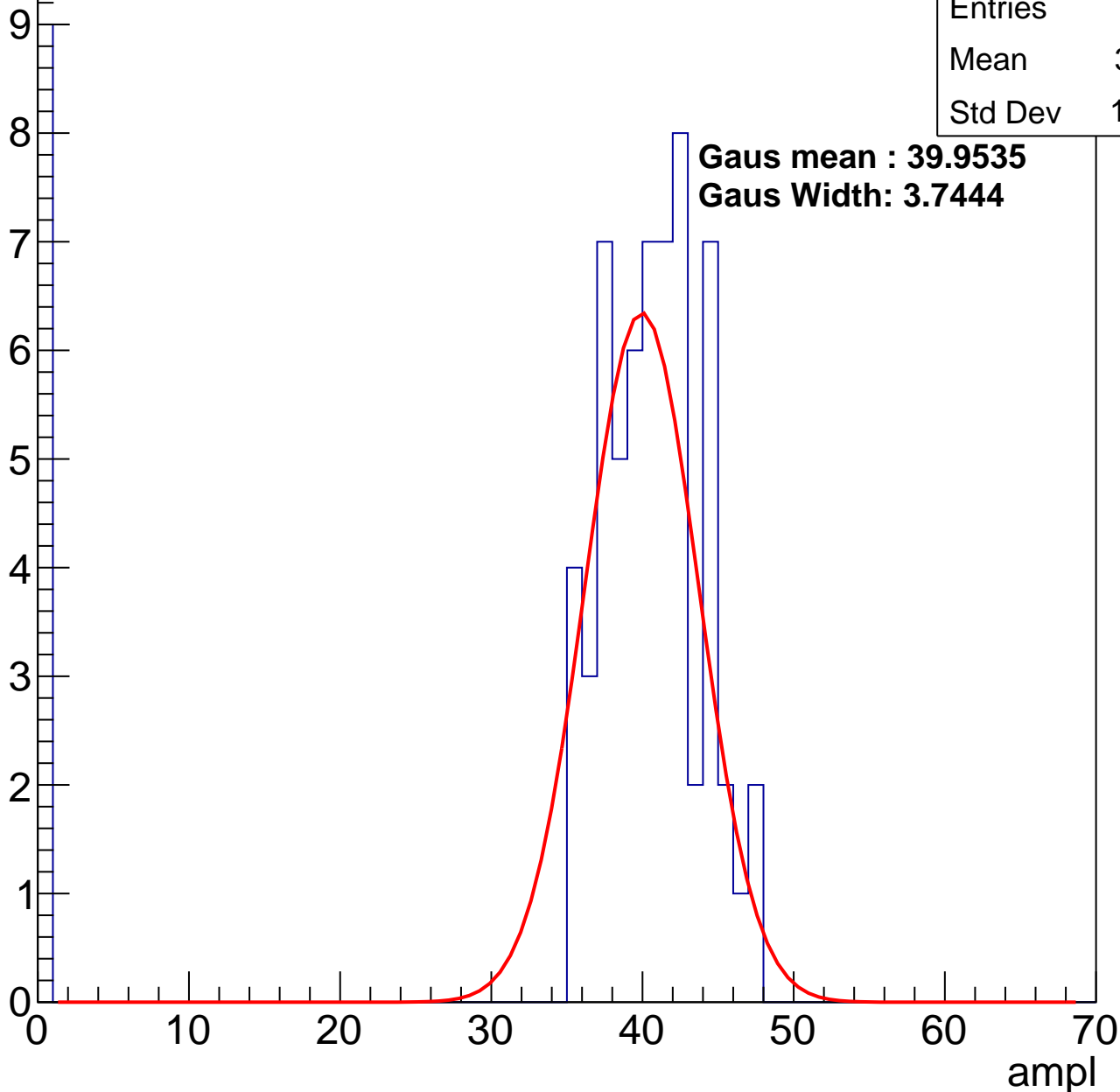
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	35.11
Std Dev	13.79

**Gaus mean : 39.9535**

**Gaus Width: 3.7444**

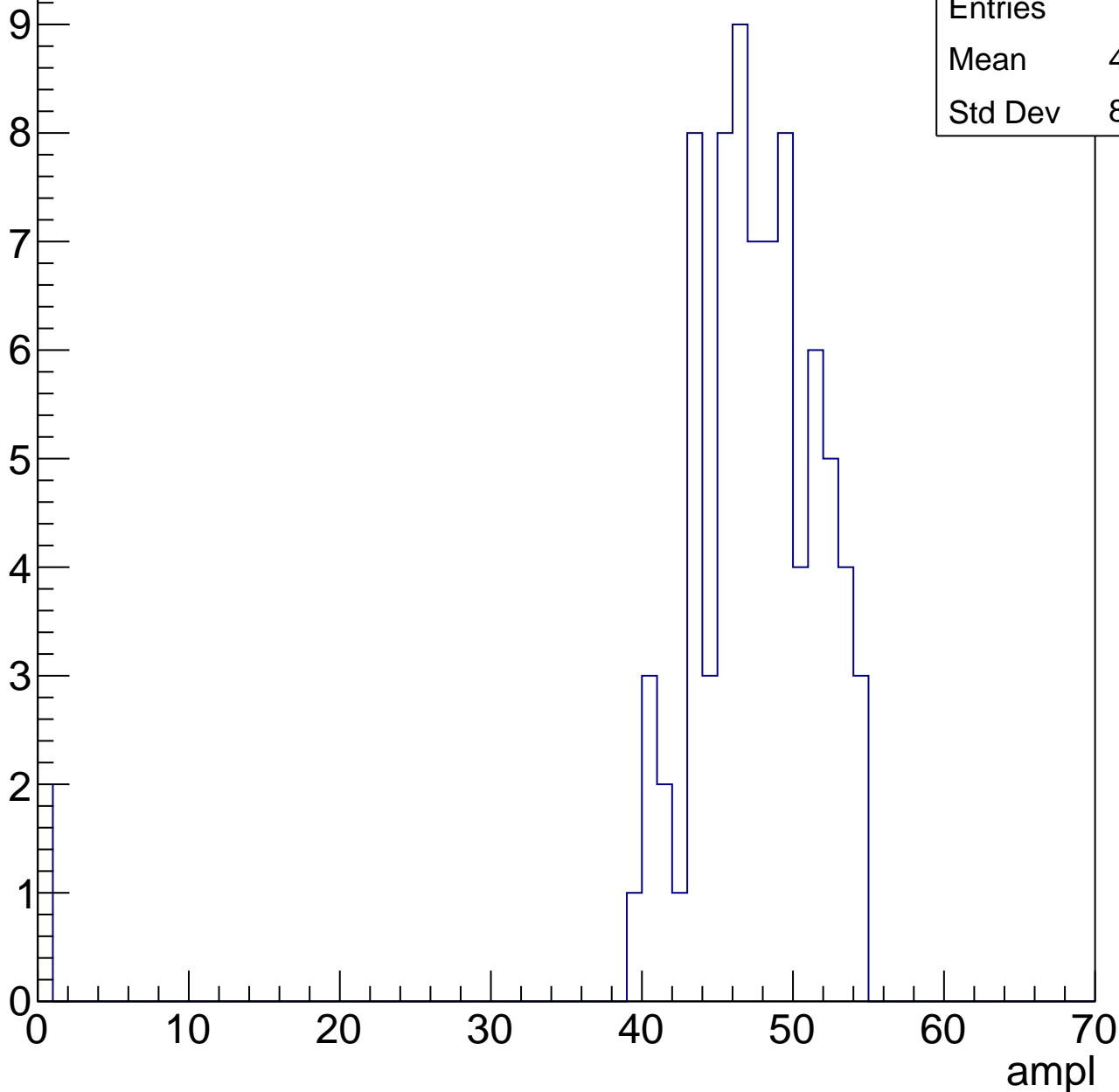


# B1L103S, U3-ch22, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	81
Mean	46.05
Std Dev	8.192

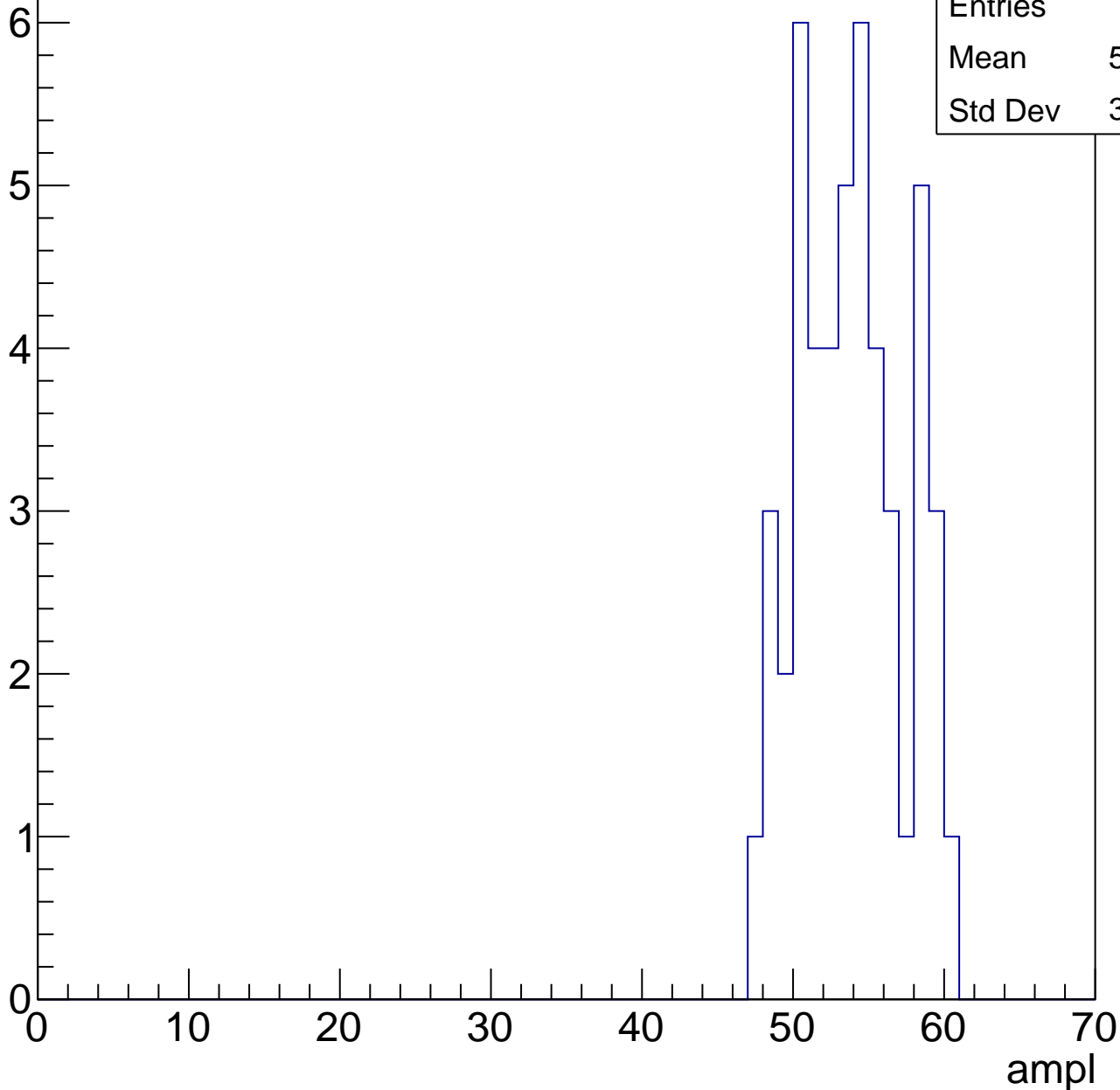


# B1L103S, U3-ch22, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	48
Mean	53.38
Std Dev	3.407

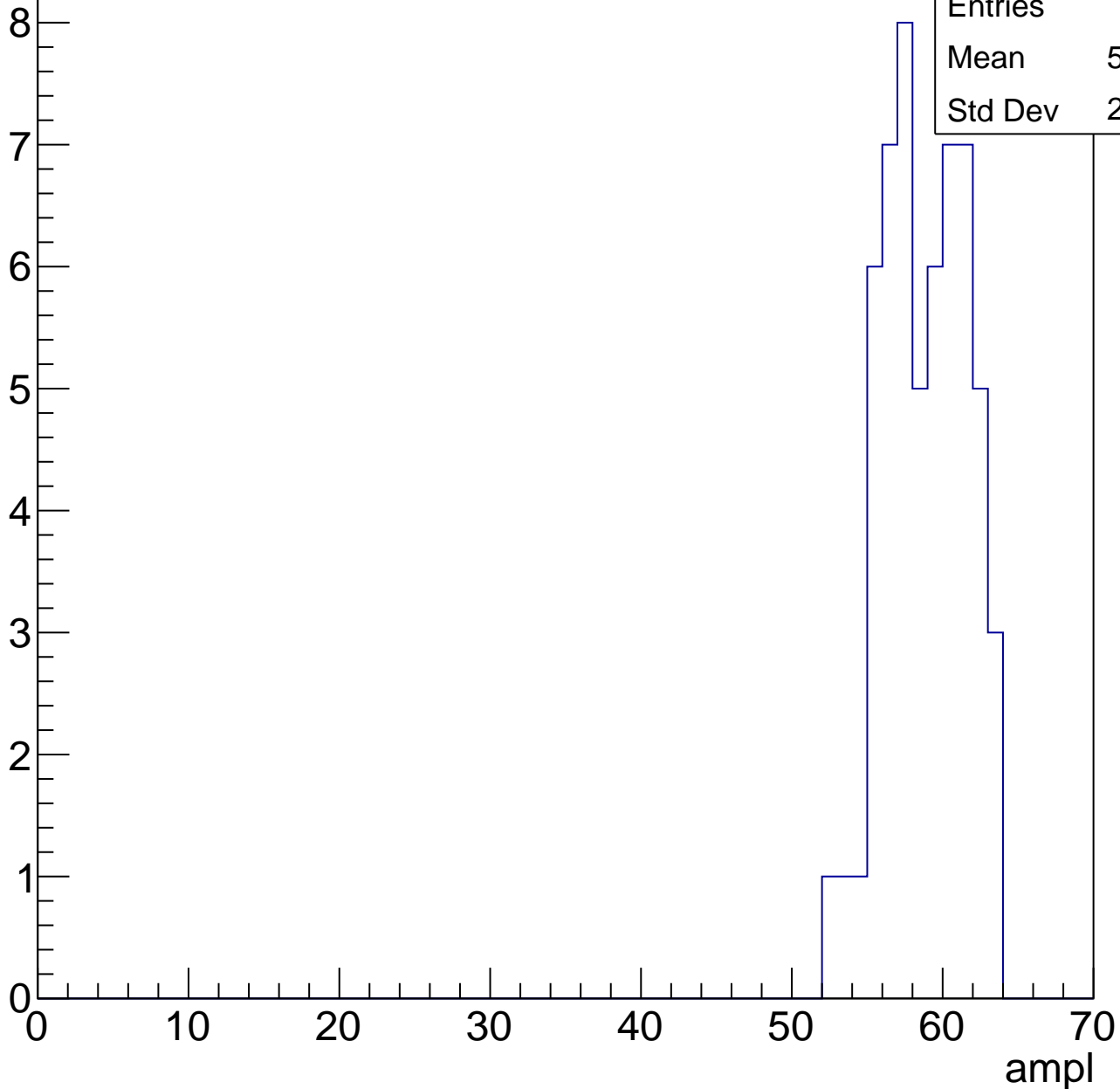


# B1L103S, U3-ch22, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	57
Mean	58.37
Std Dev	2.686

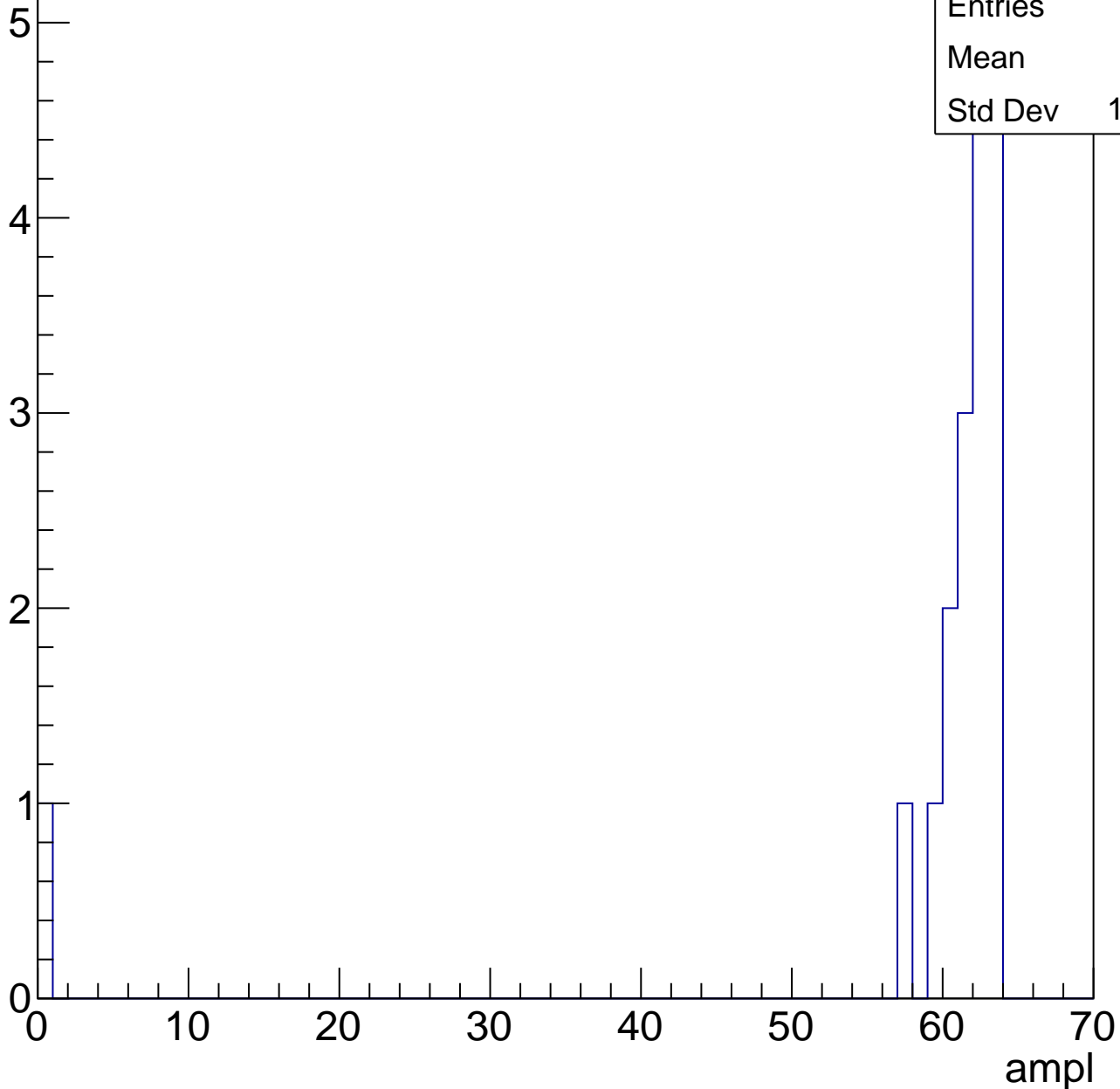


# B1L103S, U3-ch22, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	18
Mean	58
Std Dev	14.15





# B1L103S, U3-ch22, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	21
Mean	6
Std Dev	18.49

# B1L103S, U3-ch23, adc0

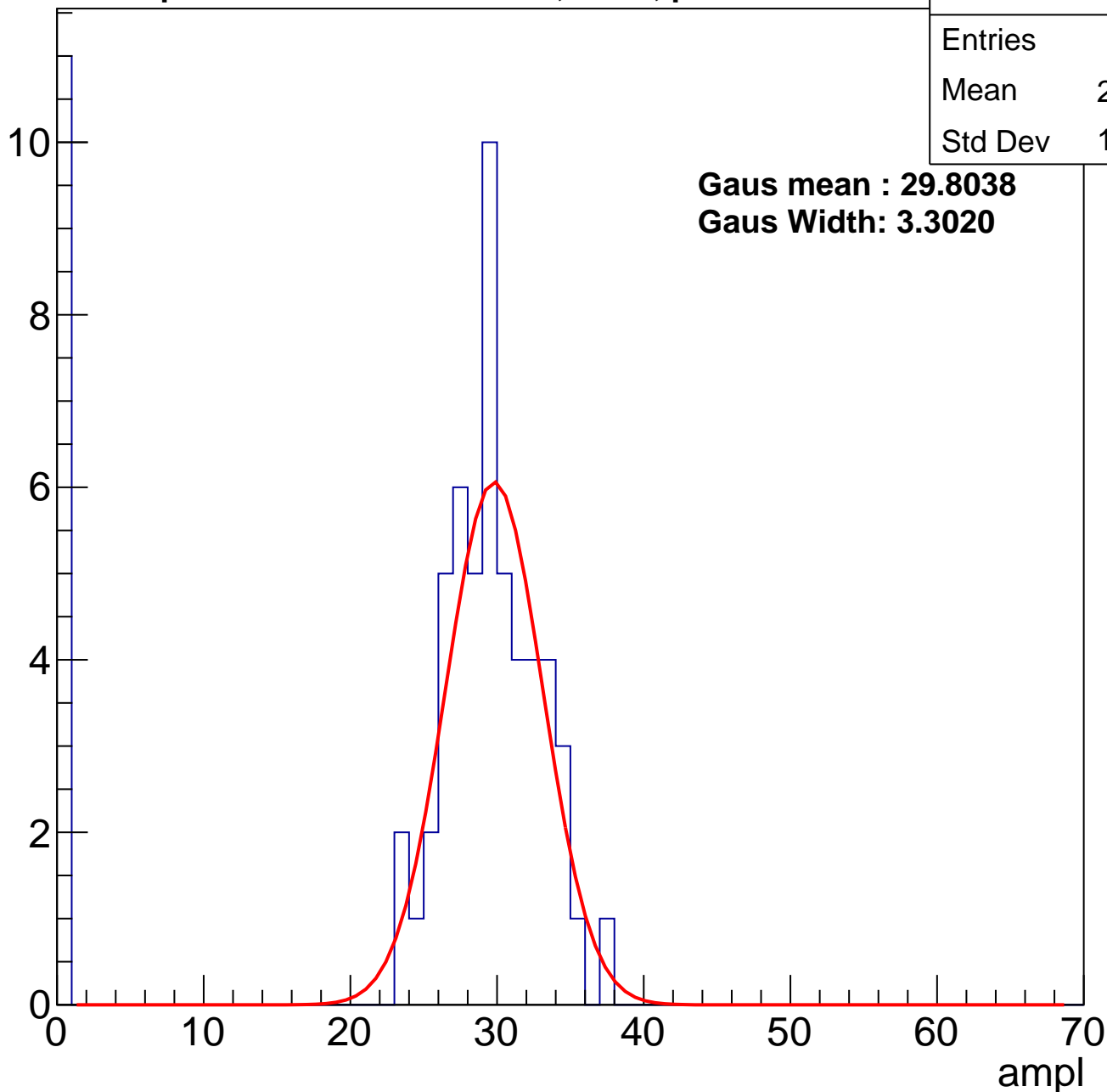
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	64
Mean	24.22
Std Dev	11.38

**Gaus mean : 29.8038**

**Gaus Width: 3.3020**

Entry



# B1L103S, U3-ch23, adc1

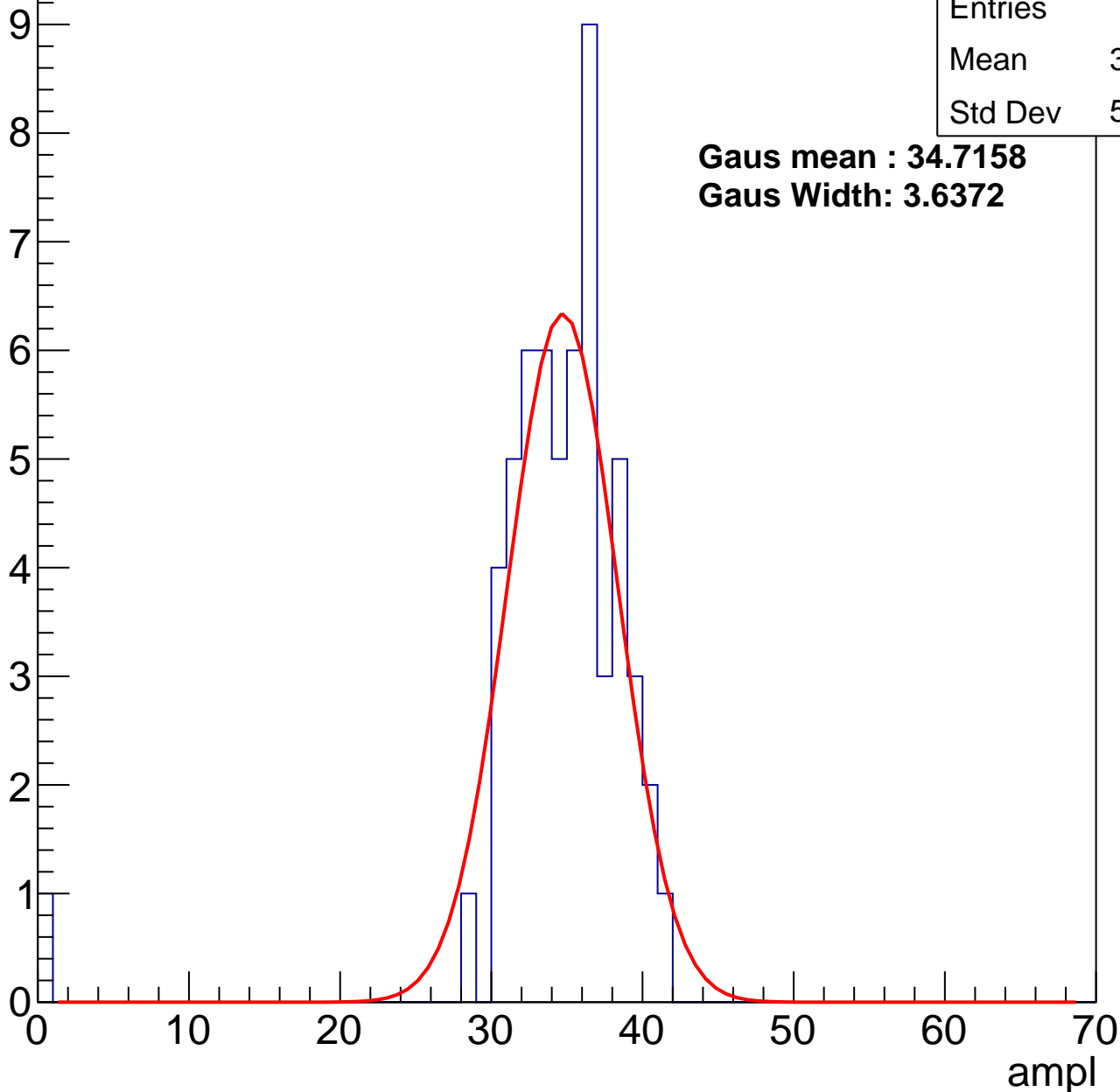
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	57
Mean	33.96
Std Dev	5.422

**Gaus mean : 34.7158**

**Gaus Width: 3.6372**



# B1L103S, U3-ch23, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	80
Mean	35.45
Std Dev	14.49

**Gaus mean : 41.9178**

**Gaus Width: 3.4513**

Entry

10

8

6

4

2

0

0

10

20

30

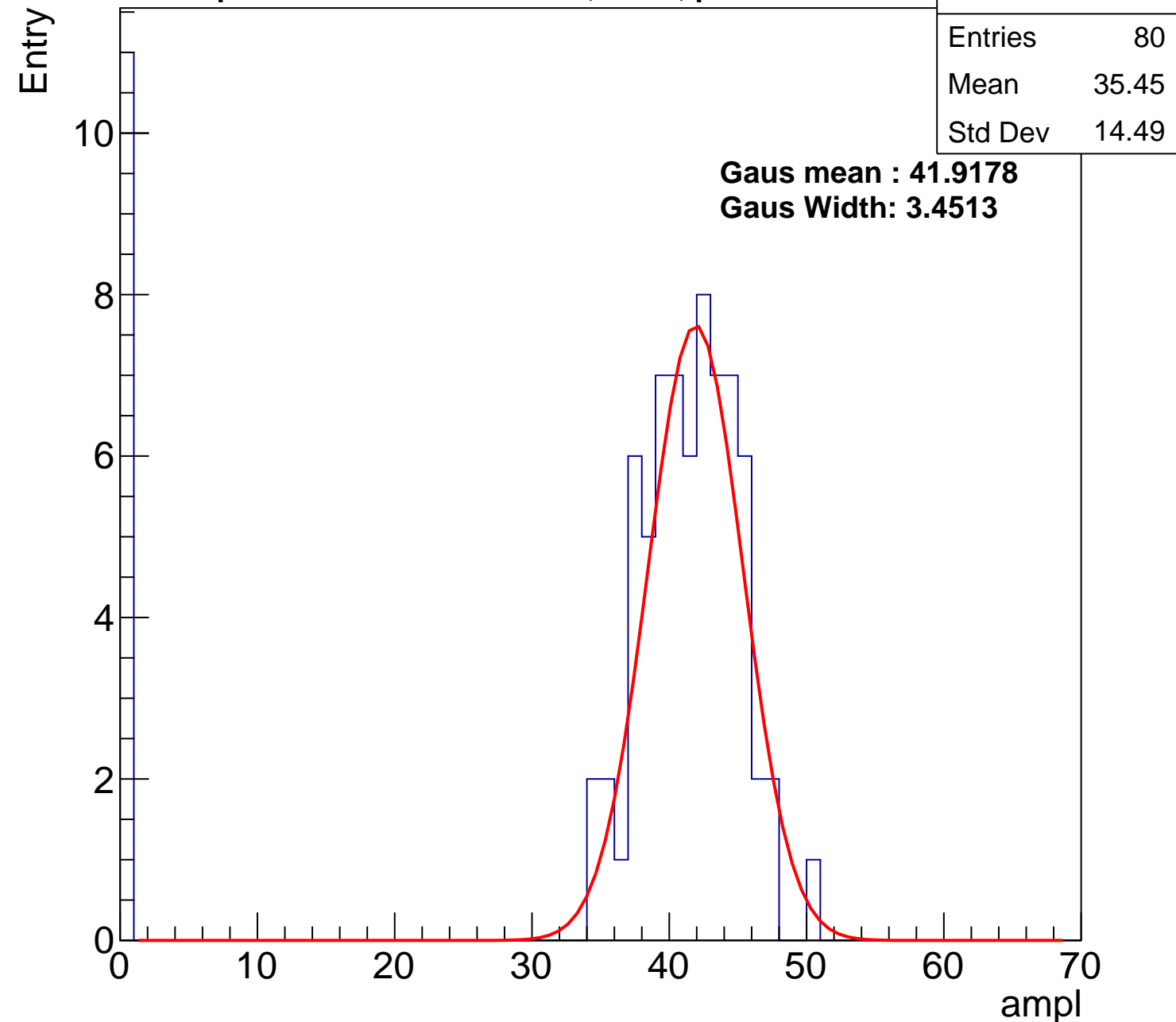
40

50

60

70

ampl



# B1L103S, U3-ch23, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

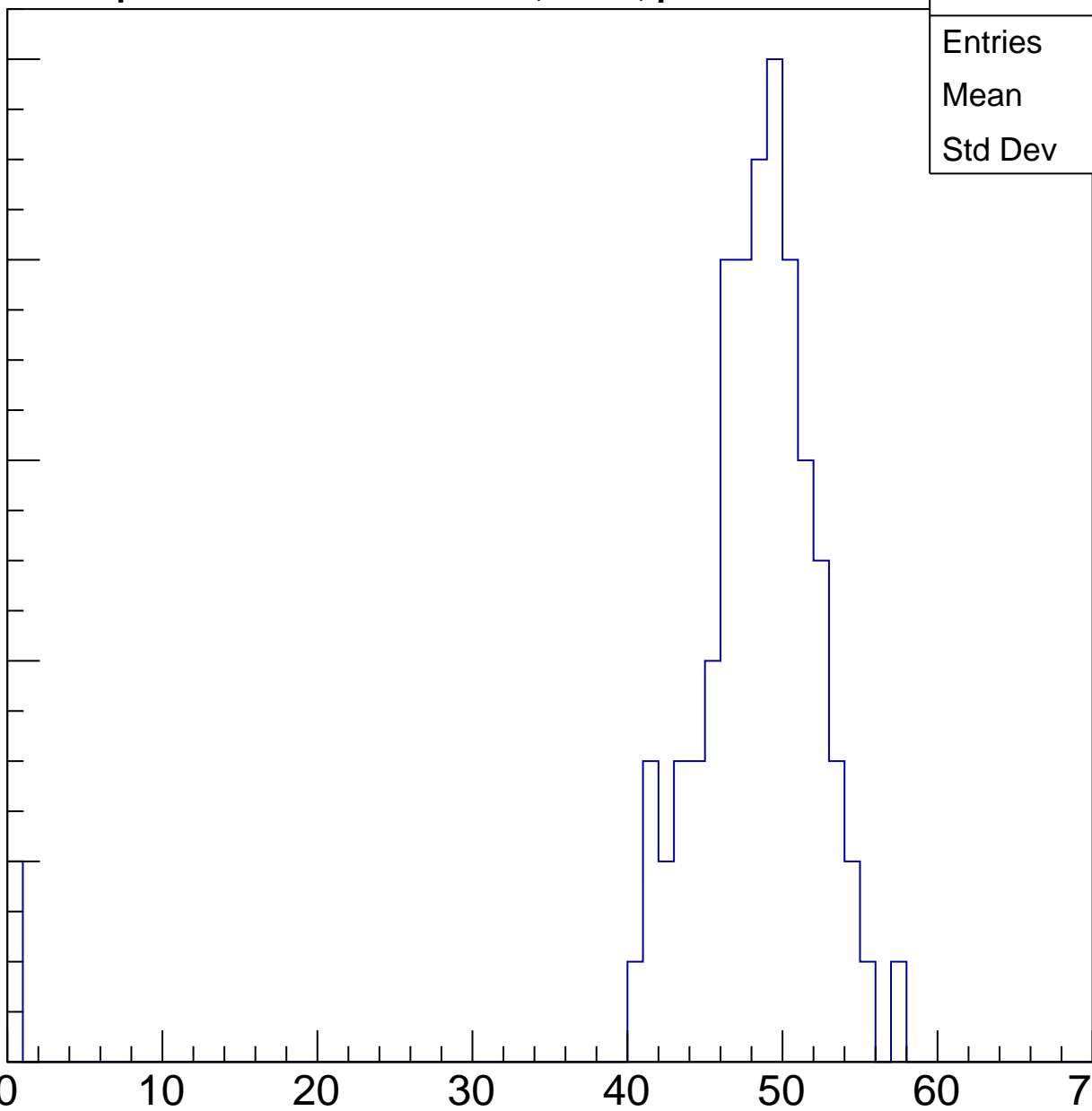
Entries	79
Mean	46.82
Std Dev	8.293

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

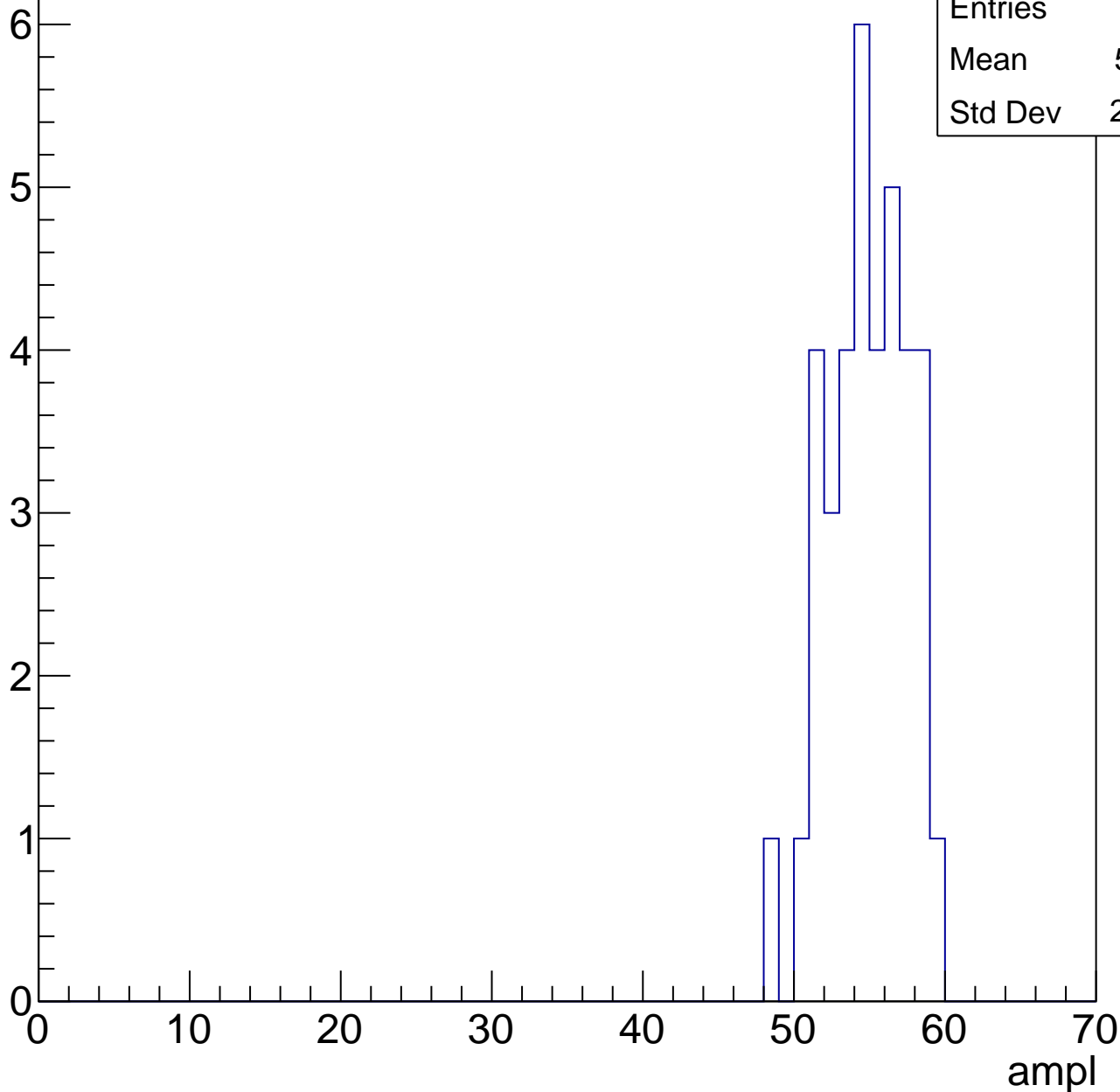


# B1L103S, U3-ch23, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

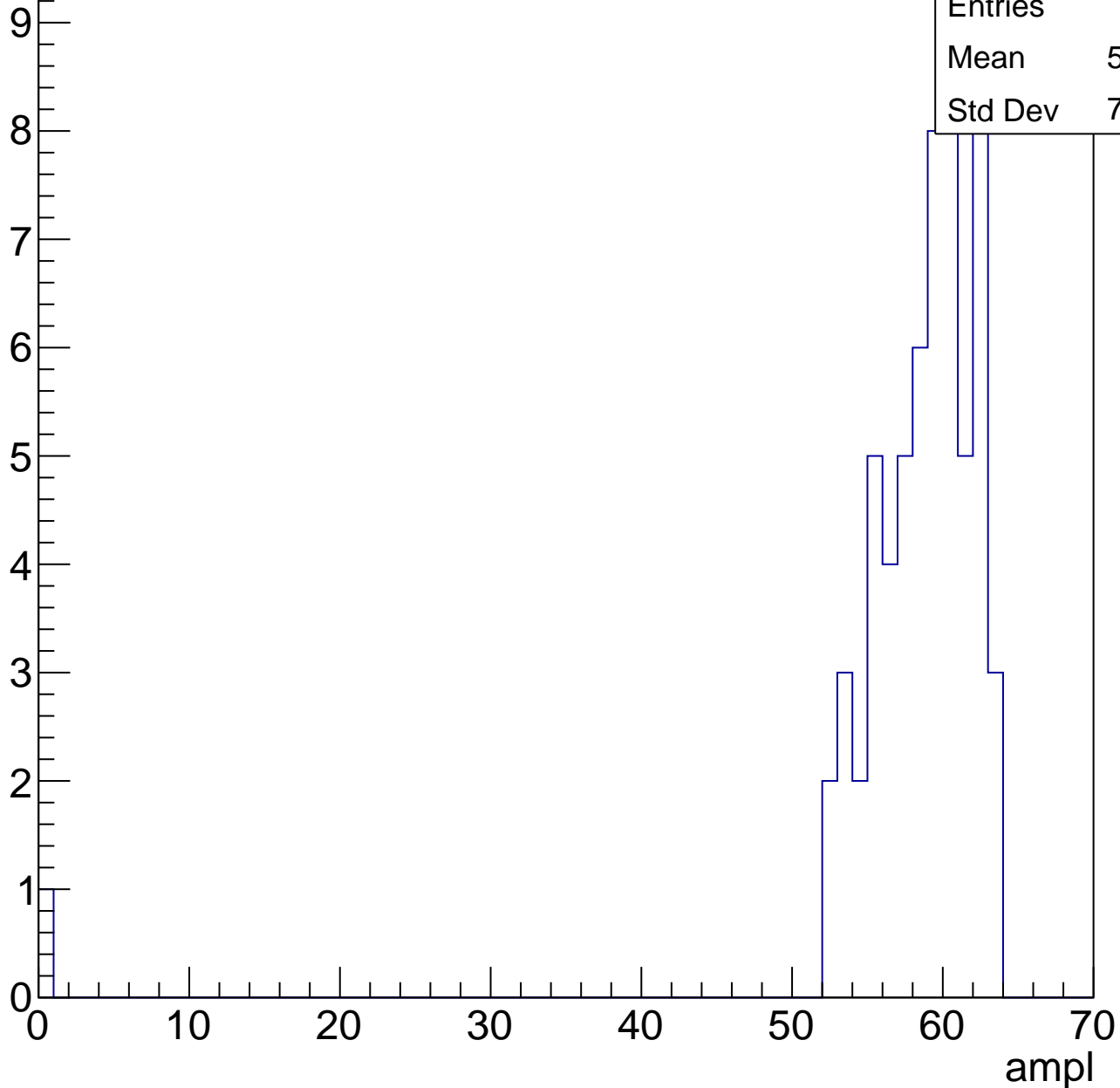
Entries	37
Mean	54.41
Std Dev	2.583



# B1L103S, U3-ch23, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

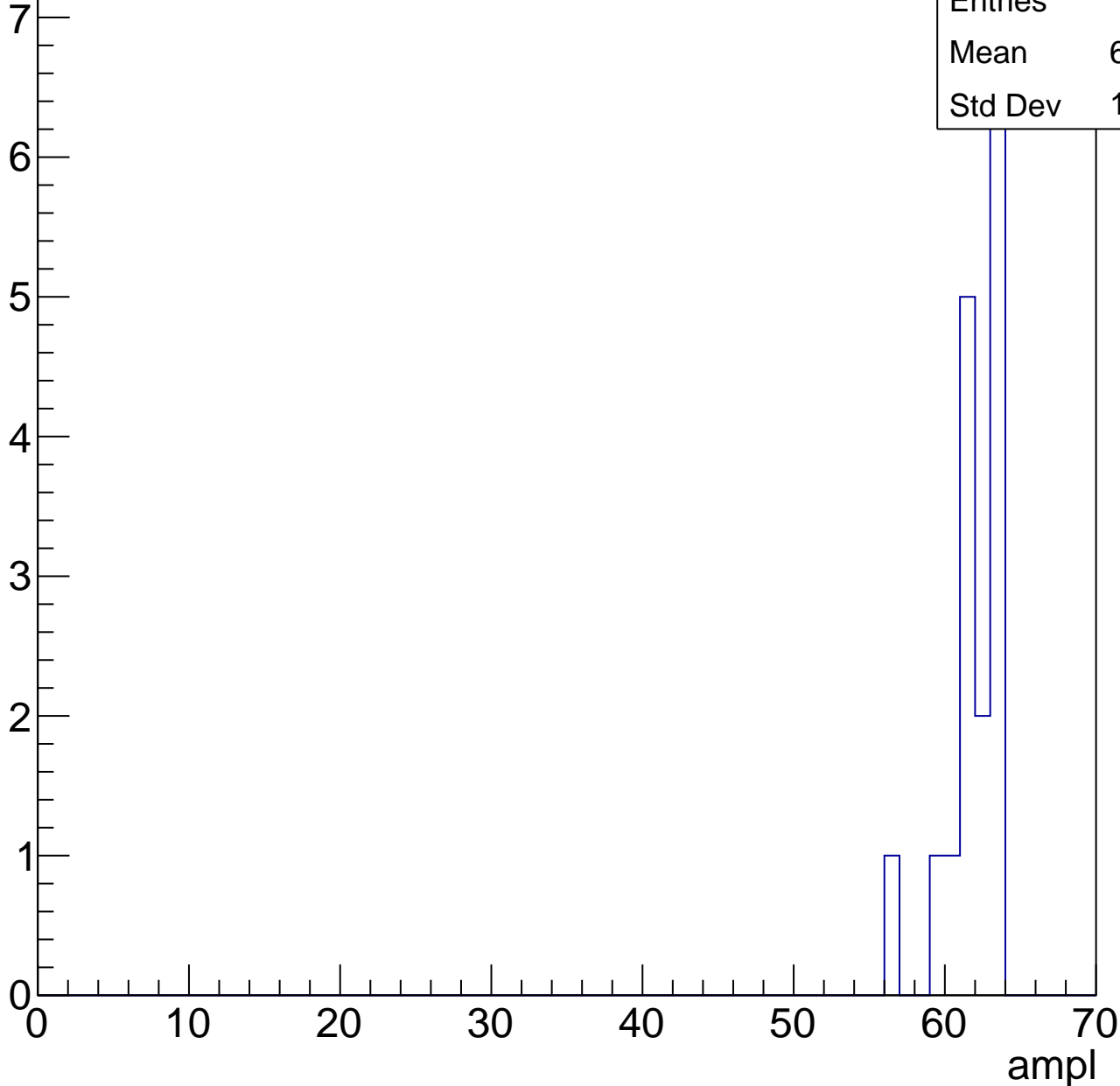


# B1L103S, U3-ch23, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	17
Mean	61.47
Std Dev	1.819





# B1L103S, U3-ch23, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U3-ch24, adc0

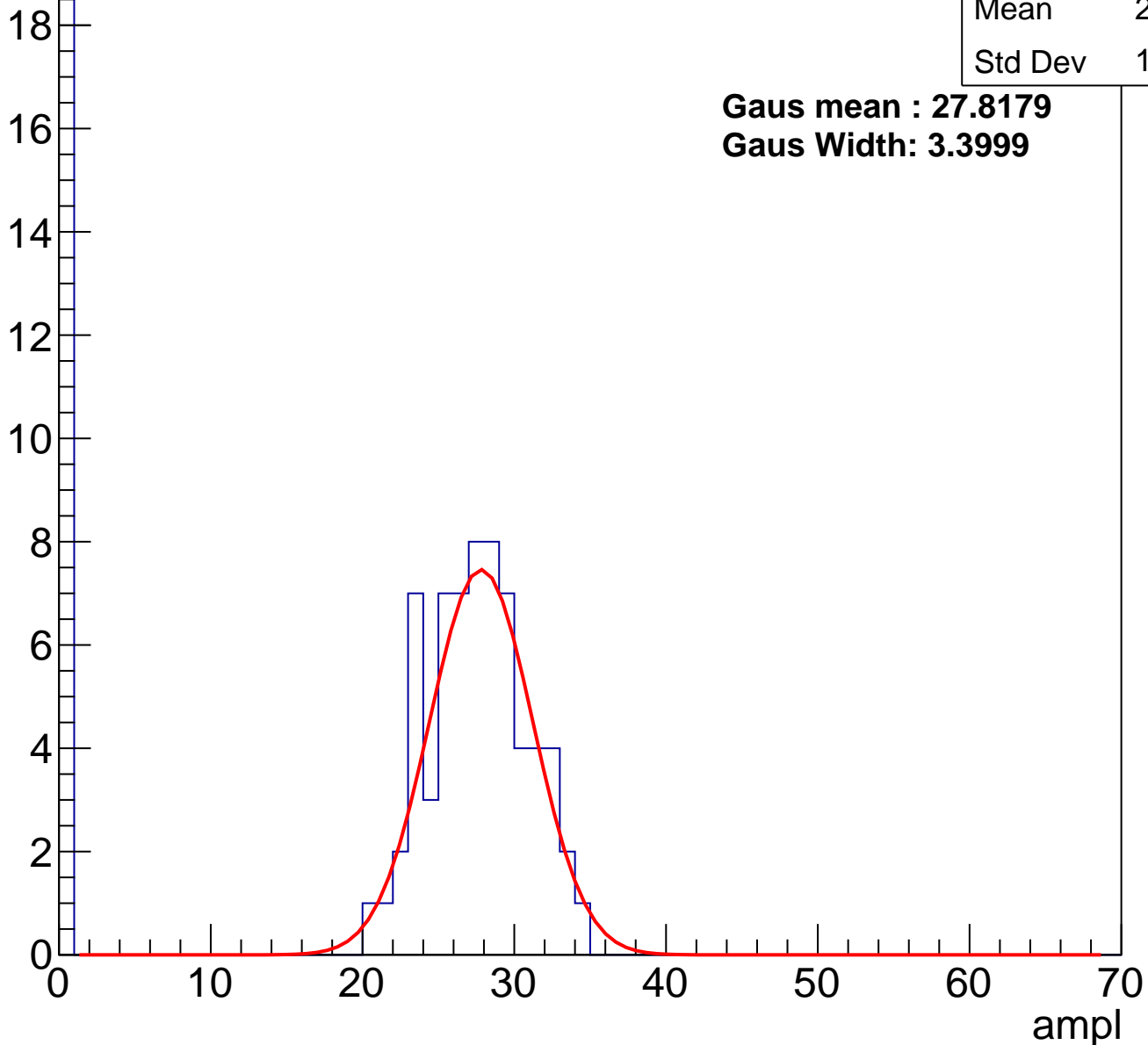
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	85
Mean	21.06
Std Dev	11.64

**Gaus mean : 27.8179**

**Gaus Width: 3.3999**

Entry



# B1L103S, U3-ch24, adc1

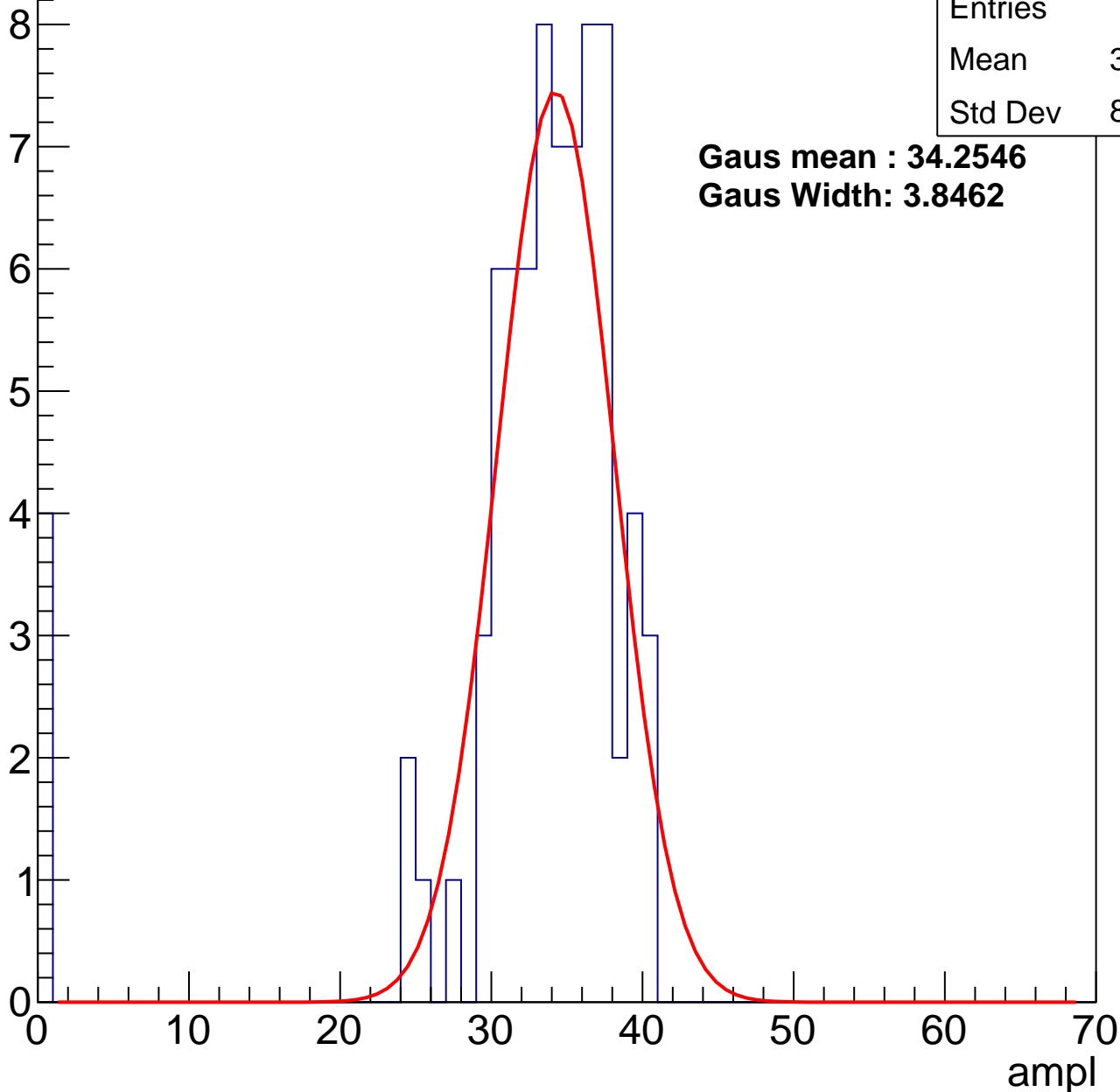
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	76
Mean	31.95
Std Dev	8.305

**Gaus mean : 34.2546**

**Gaus Width: 3.8462**



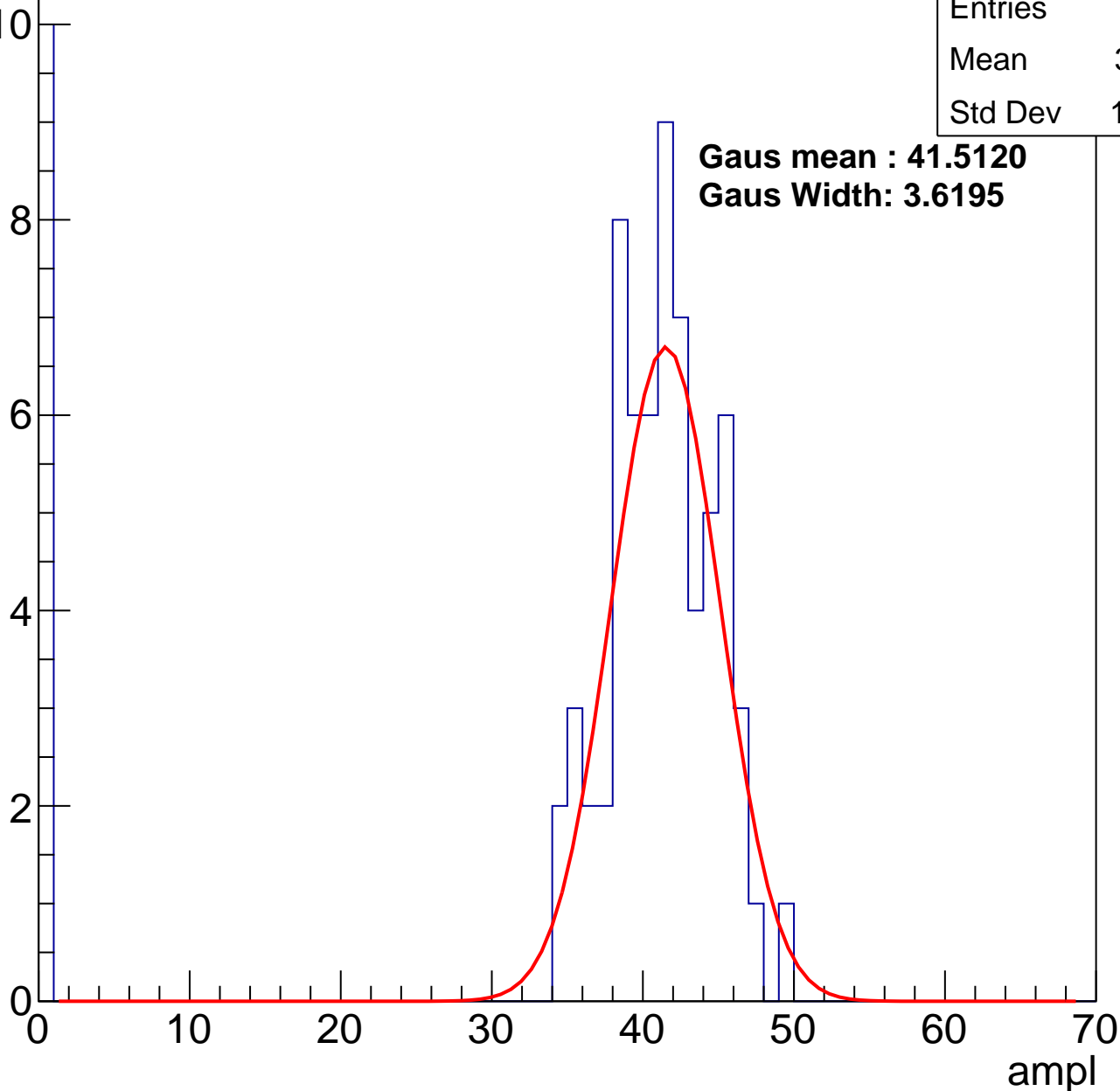
# B1L103S, U3-ch24, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	75
Mean	35.41
Std Dev	14.24

**Gaus mean : 41.5120**  
**Gaus Width: 3.6195**

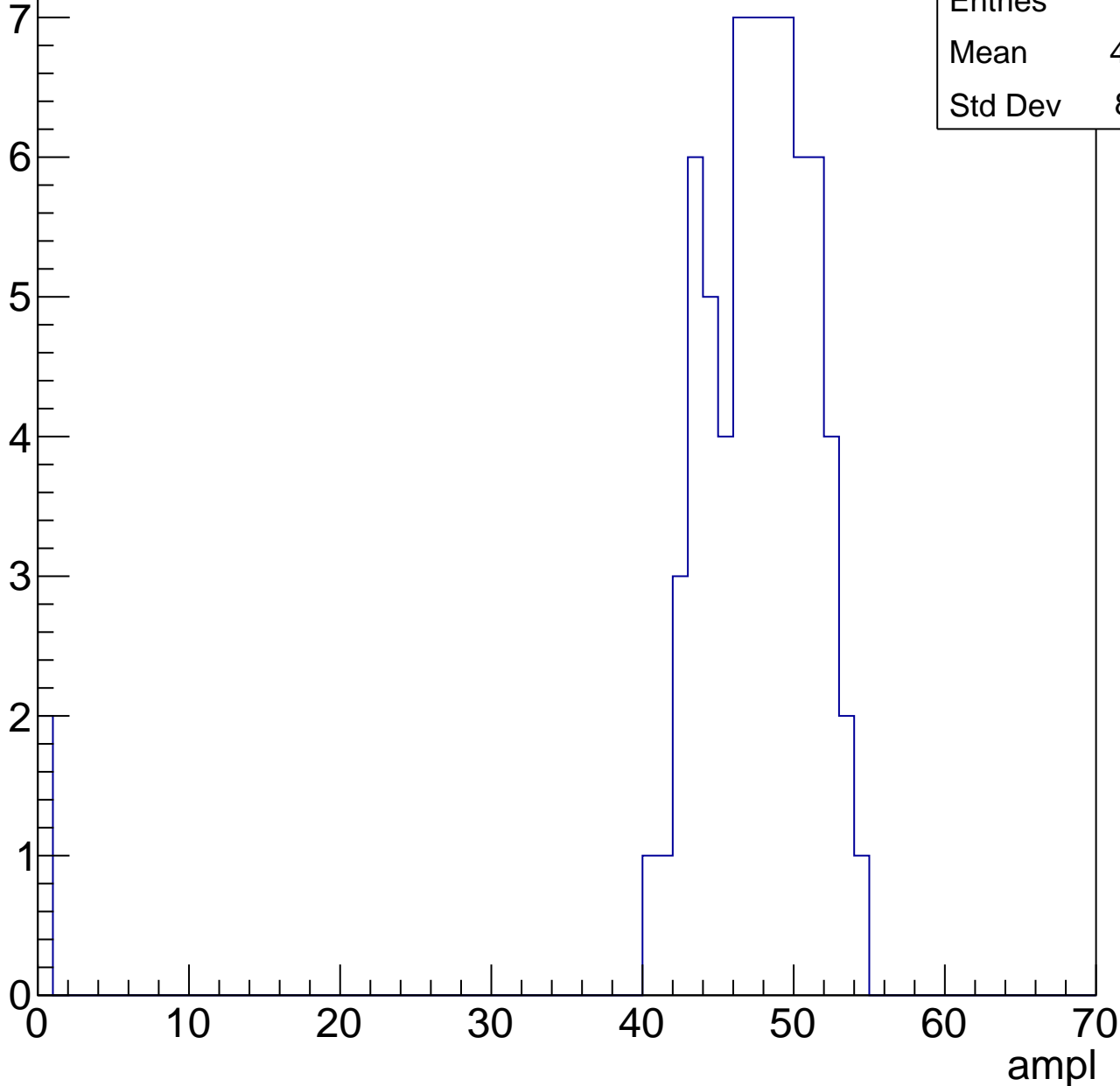


# B1L103S, U3-ch24, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	45.93
Std Dev	8.571

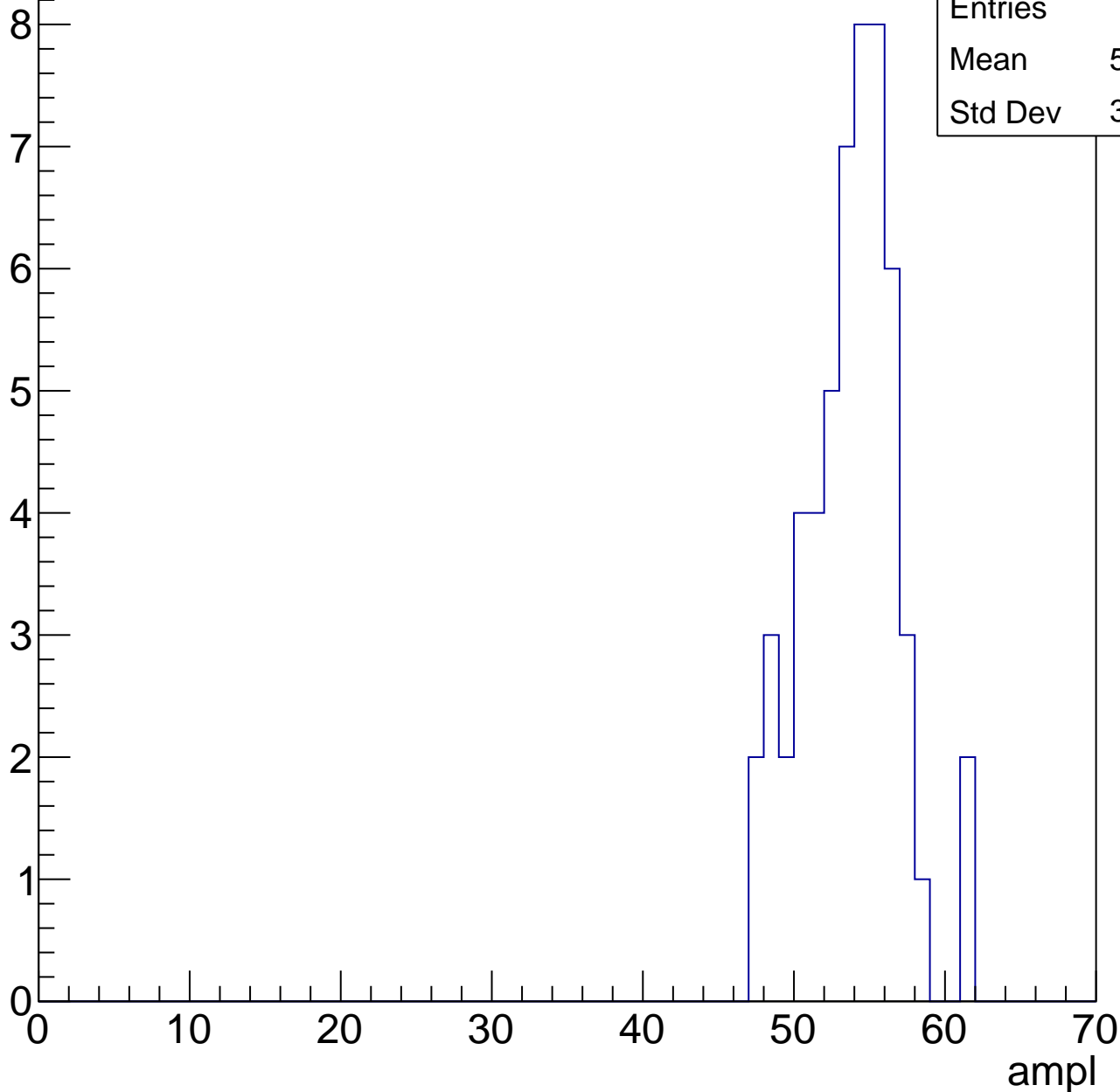


# B1L103S, U3-ch24, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

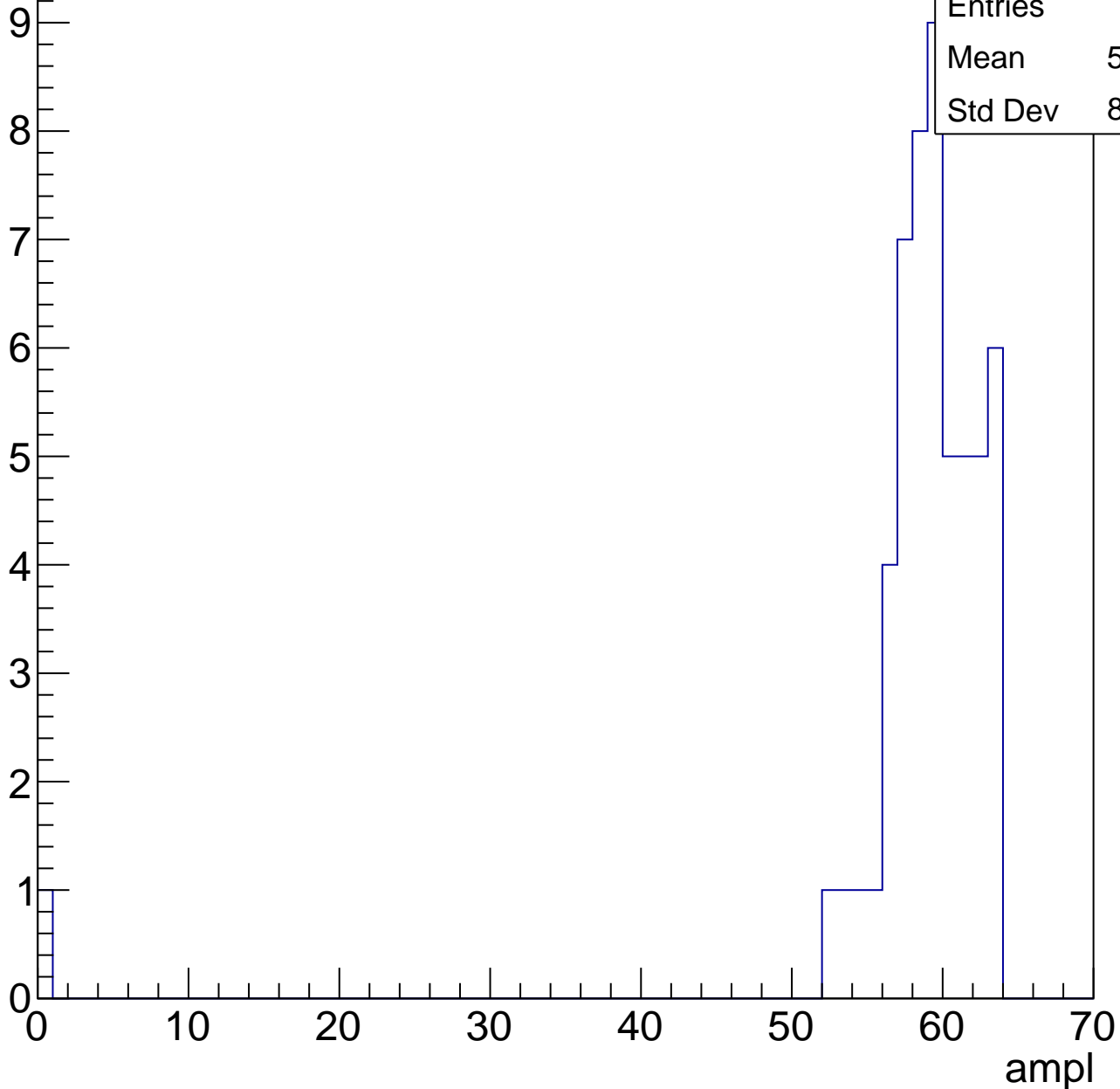
Entries	55
Mean	53.27
Std Dev	3.095



# B1L103S, U3-ch24, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

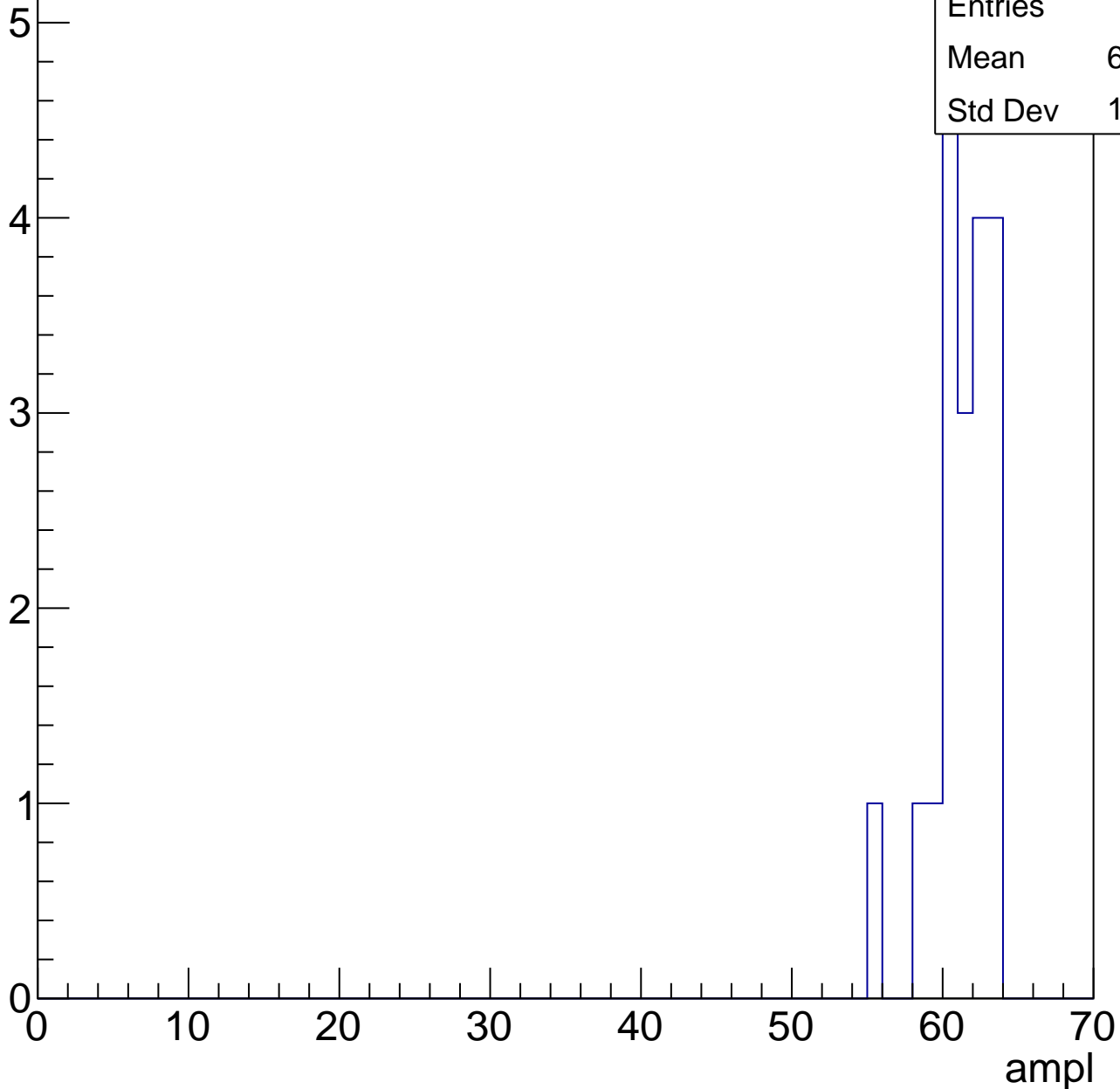


# B1L103S, U3-ch24, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	19
Mean	60.79
Std Dev	1.962





# B1L103S, U3-ch24, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51

Entry



# B1L103S, U3-ch25, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	79
Mean	22.18
Std Dev	11.52

**Gaus mean : 28.4825**

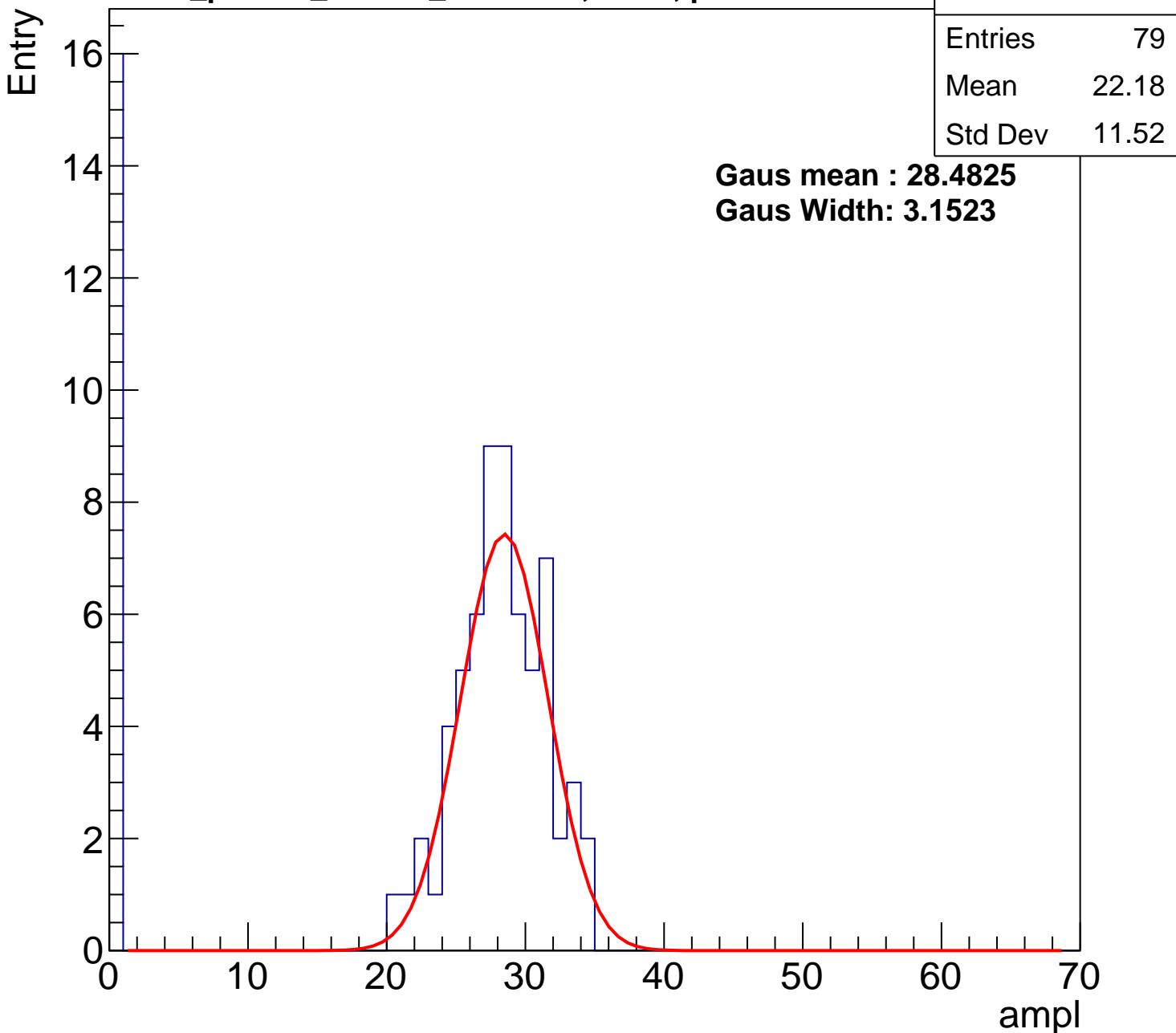
**Gaus Width: 3.1523**

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch25, adc1

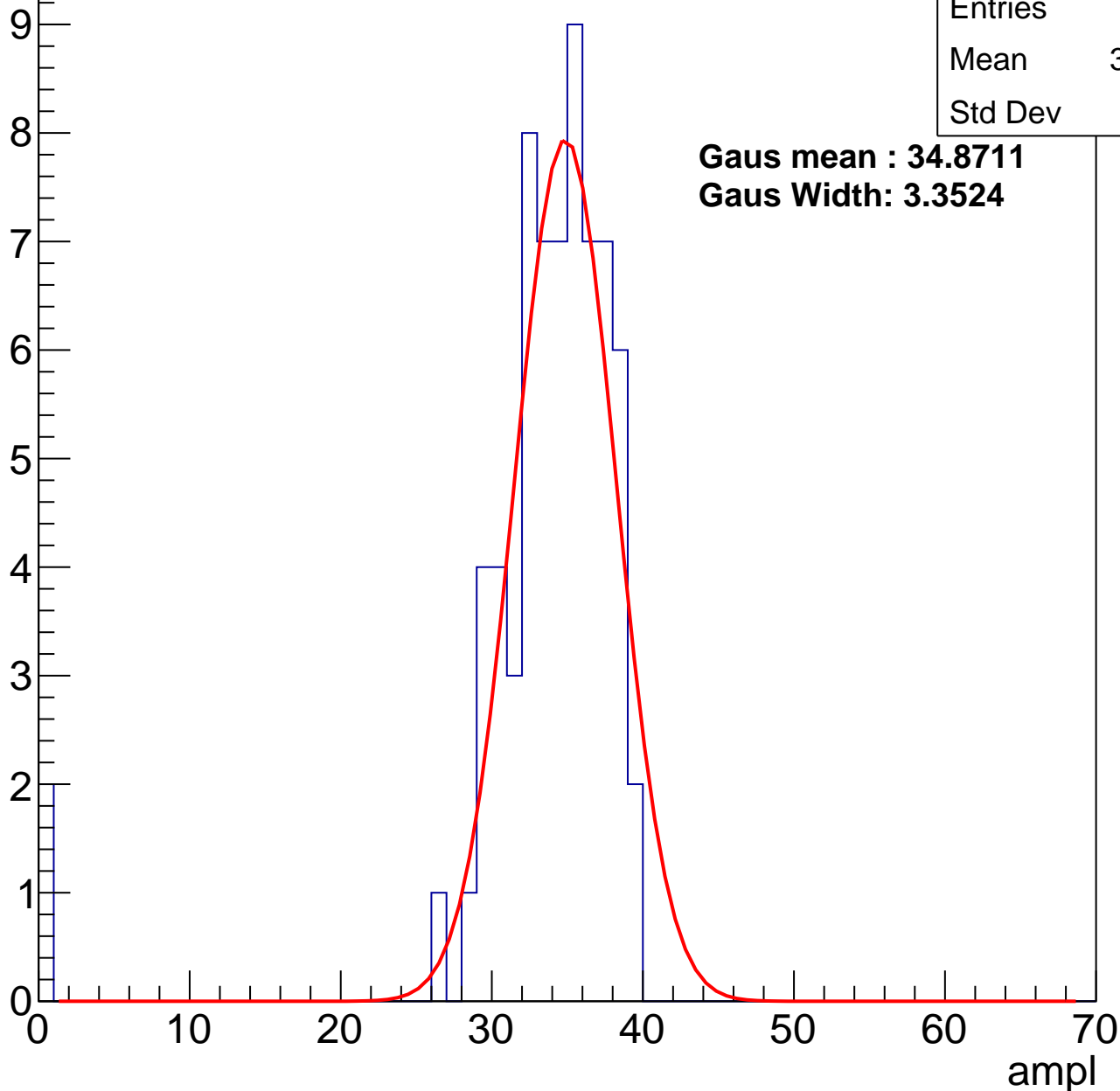
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	32.94
Std Dev	6.43

**Gaus mean : 34.8711**

**Gaus Width: 3.3524**



# B1L103S, U3-ch25, adc2

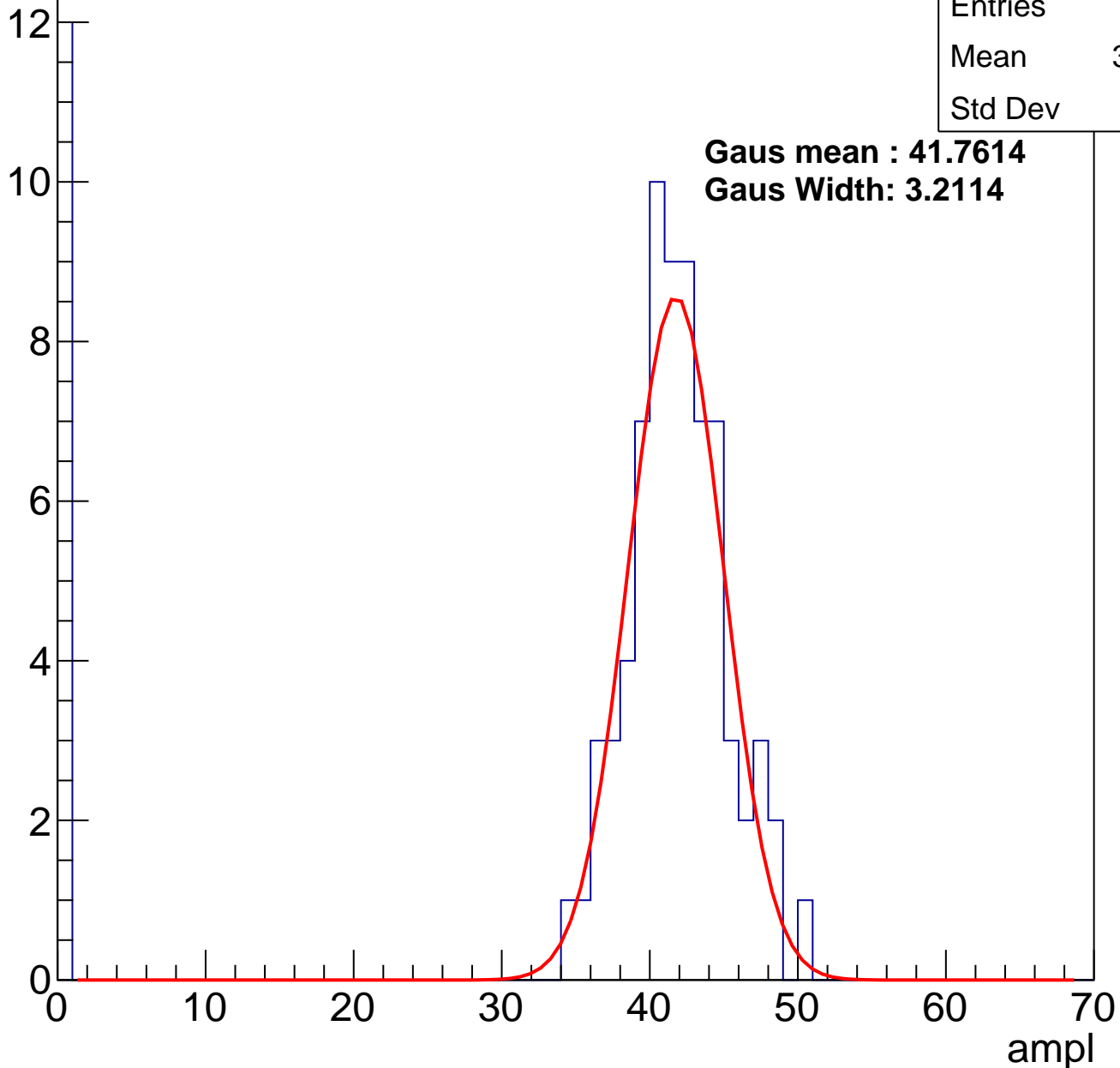
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	84
Mean	35.51
Std Dev	14.8

**Gaus mean : 41.7614**

**Gaus Width: 3.2114**

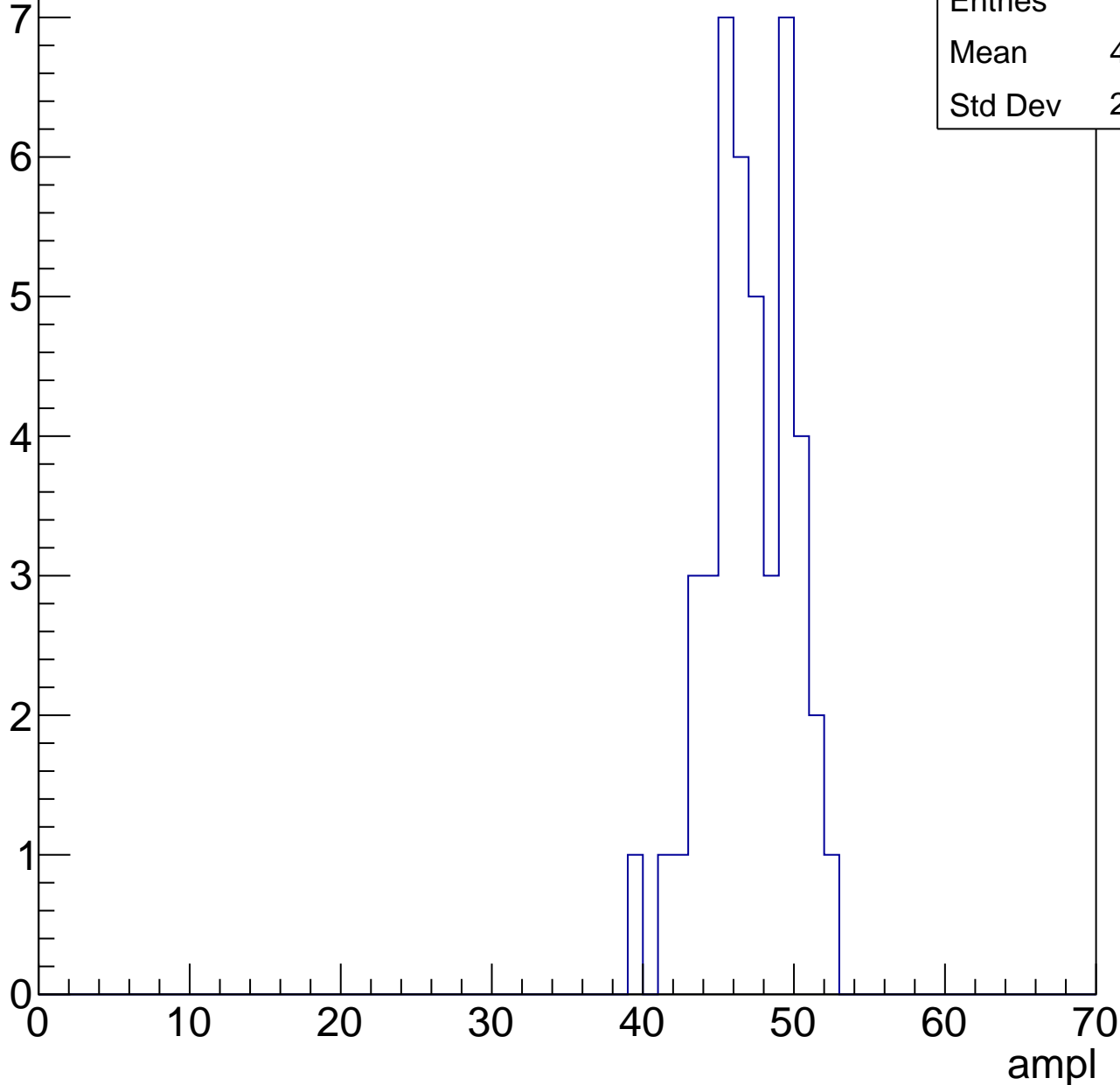
Entry



# B1L103S, U3-ch25, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

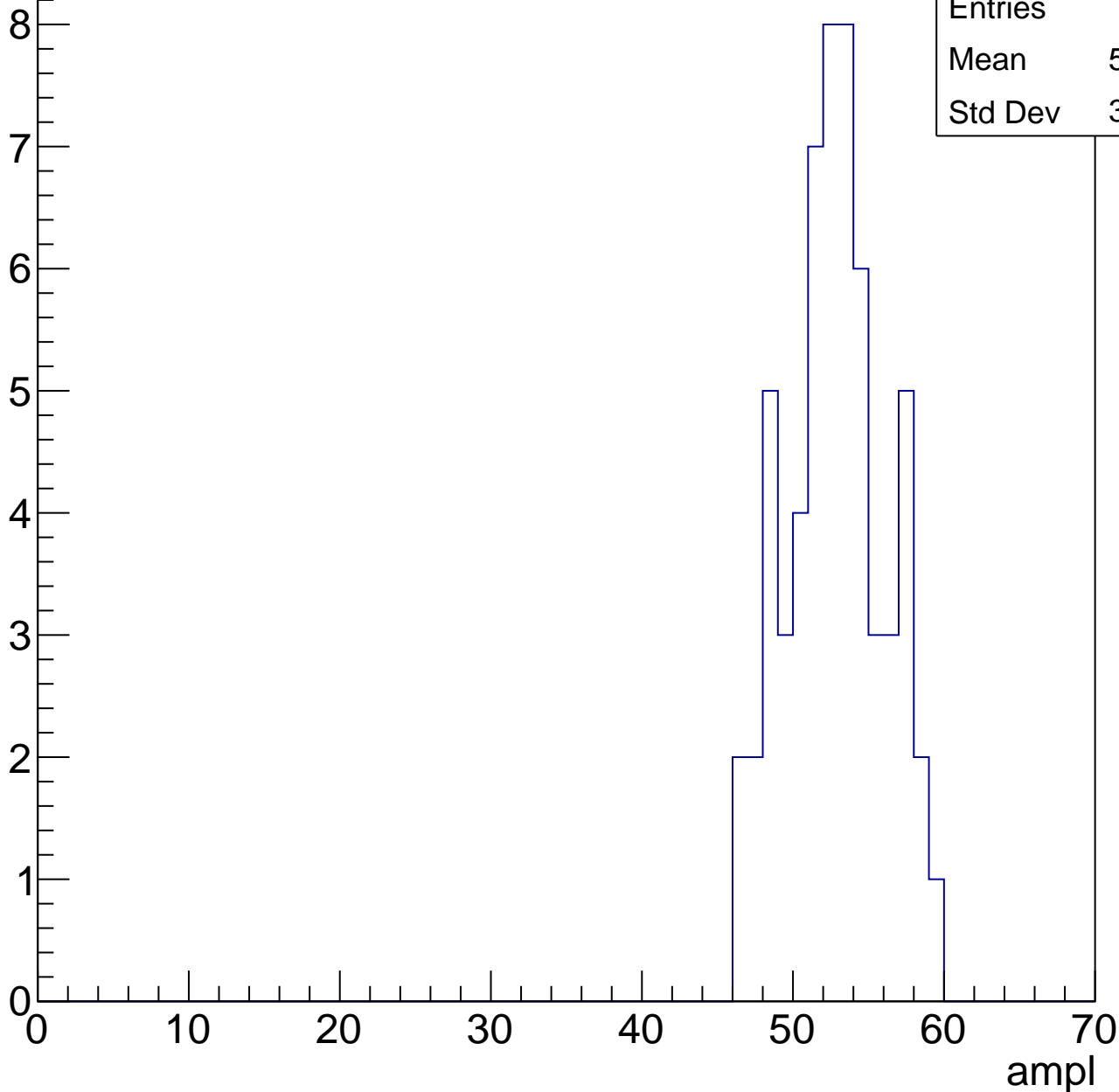


# B1L103S, U3-ch25, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	52.32
Std Dev	3.186



# B1L103S, U3-ch25, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	71
Mean	57.38
Std Dev	7.548

ampl

0

10

20

30

40

50

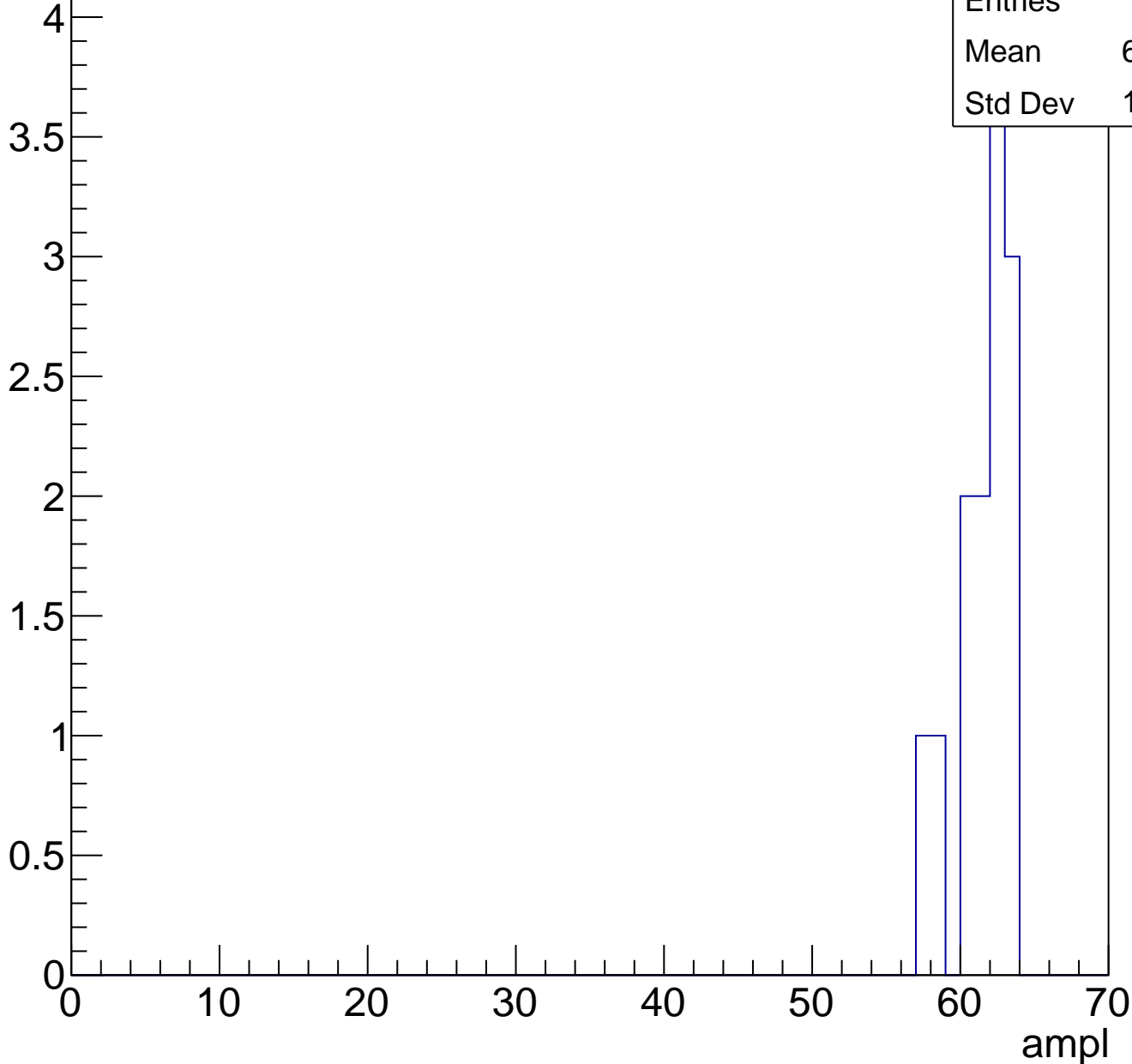
60

70

# B1L103S, U3-ch25, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U3-ch25, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	5.905
Std Dev	18.2

Entry



# B1L103S, U3-ch26, adc0

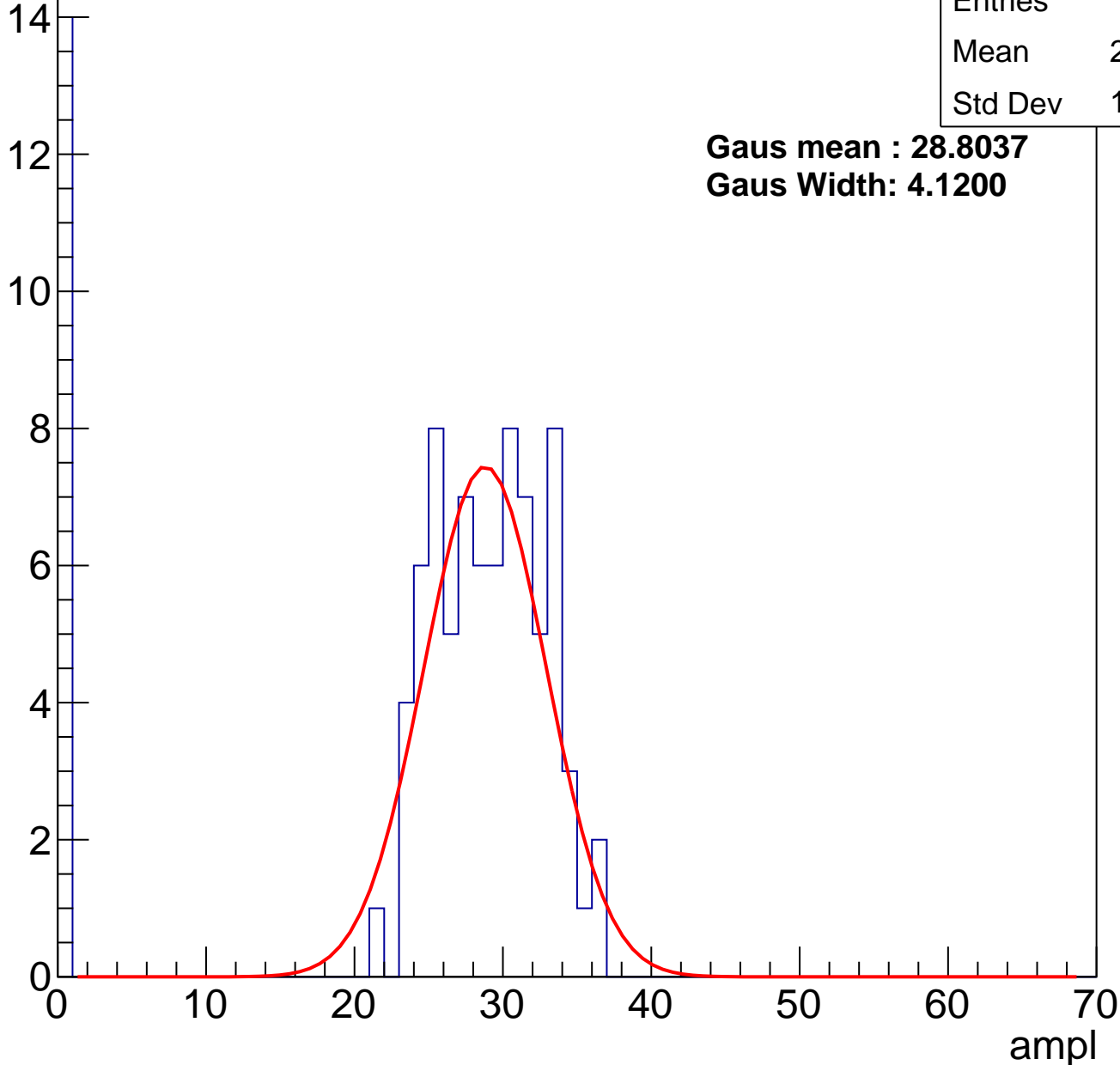
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	91
Mean	24.26
Std Dev	10.85

**Gaus mean : 28.8037**

**Gaus Width: 4.1200**

Entry



# B1L103S, U3-ch26, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	86
Mean	31.78
Std Dev	12.6

**Gaus mean : 37.2835**

**Gaus Width: 3.8968**

Entry

10

8

6

4

2

0

0

10

20

30

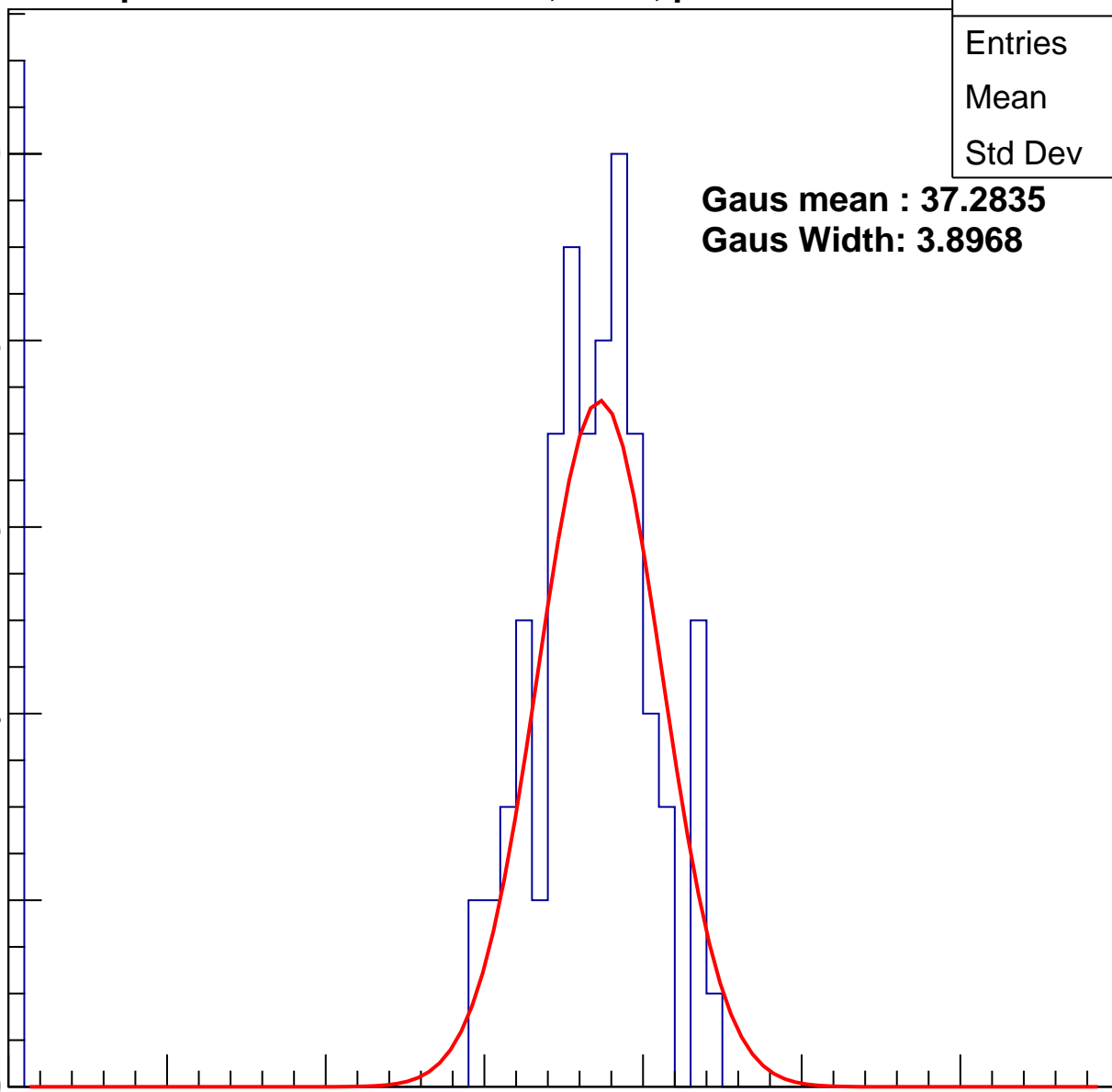
40

50

60

70

ampl



# B1L103S, U3-ch26, adc2

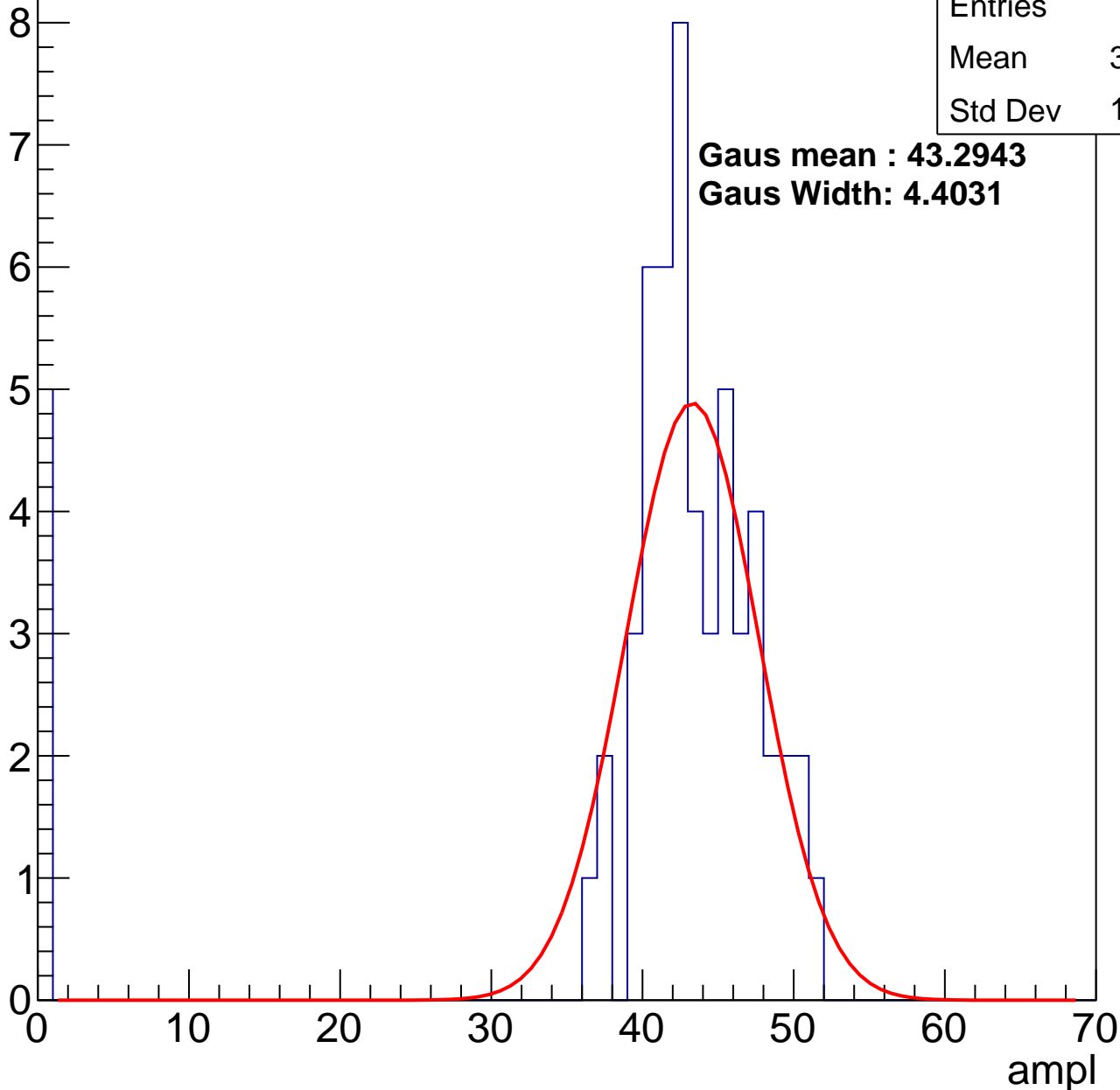
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	57
Mean	39.46
Std Dev	12.69

**Gaus mean : 43.2943**

**Gaus Width: 4.4031**

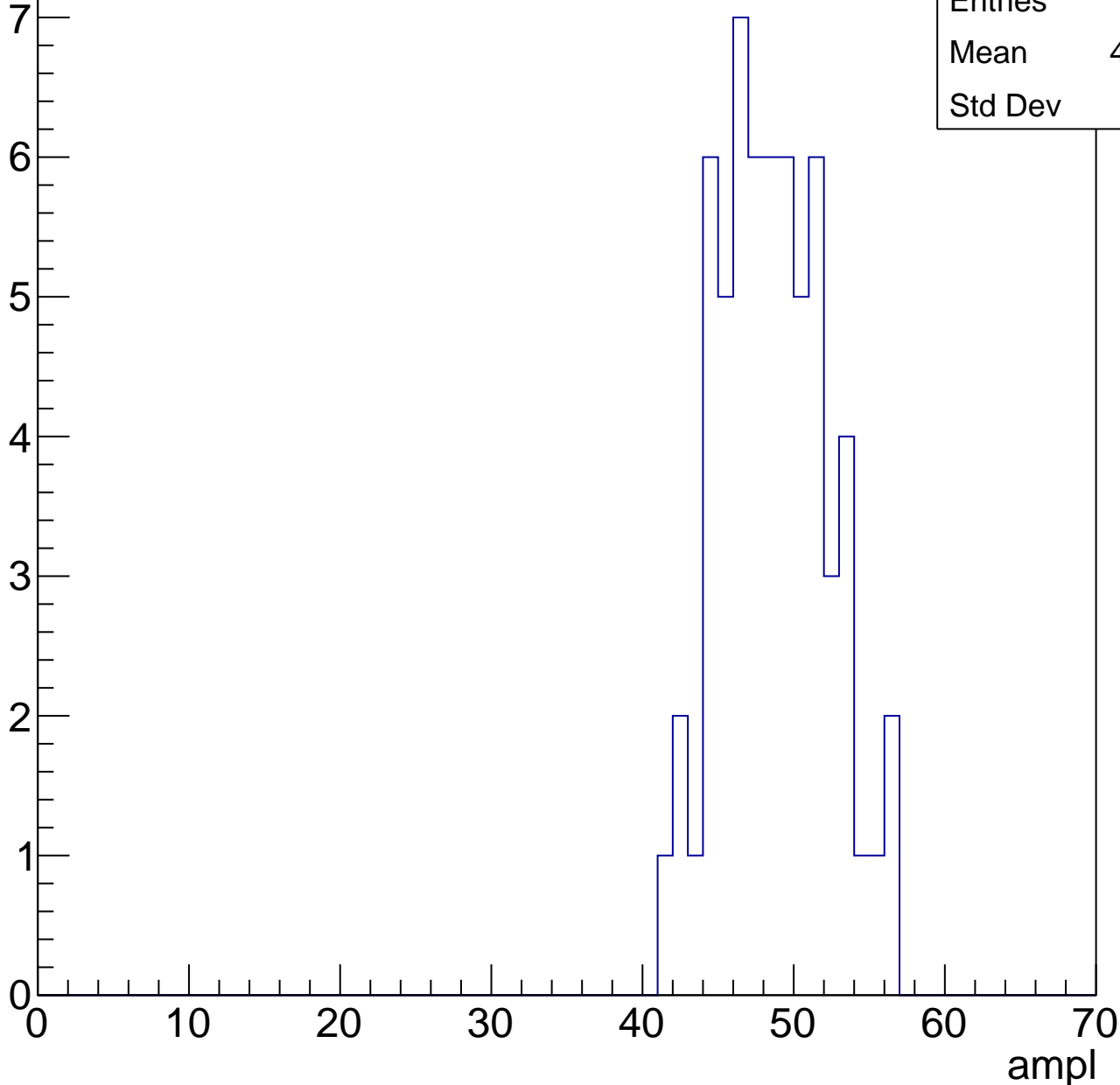


# B1L103S, U3-ch26, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	48.19
Std Dev	3.5

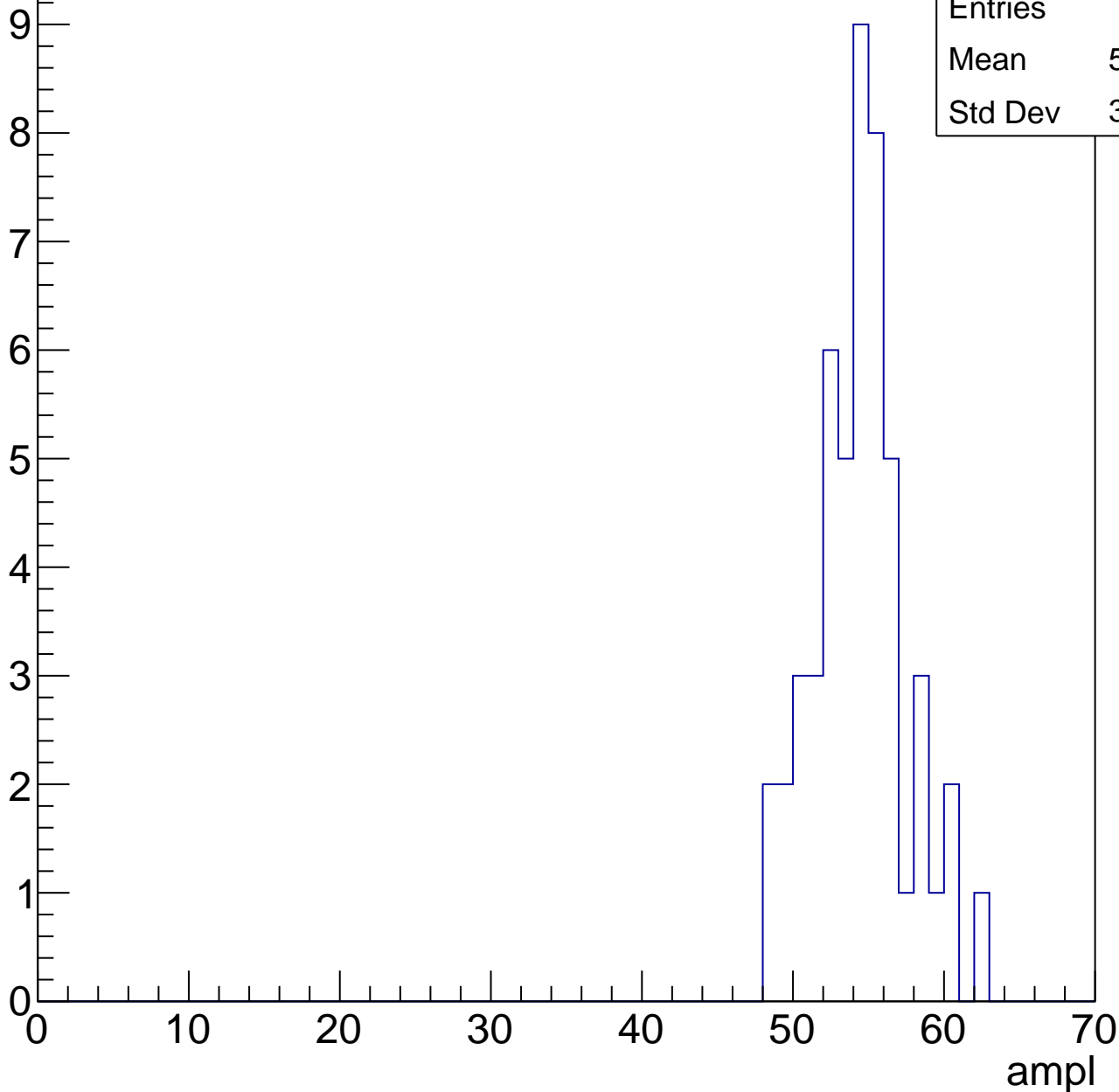


# B1L103S, U3-ch26, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	51
Mean	53.96
Std Dev	3.042

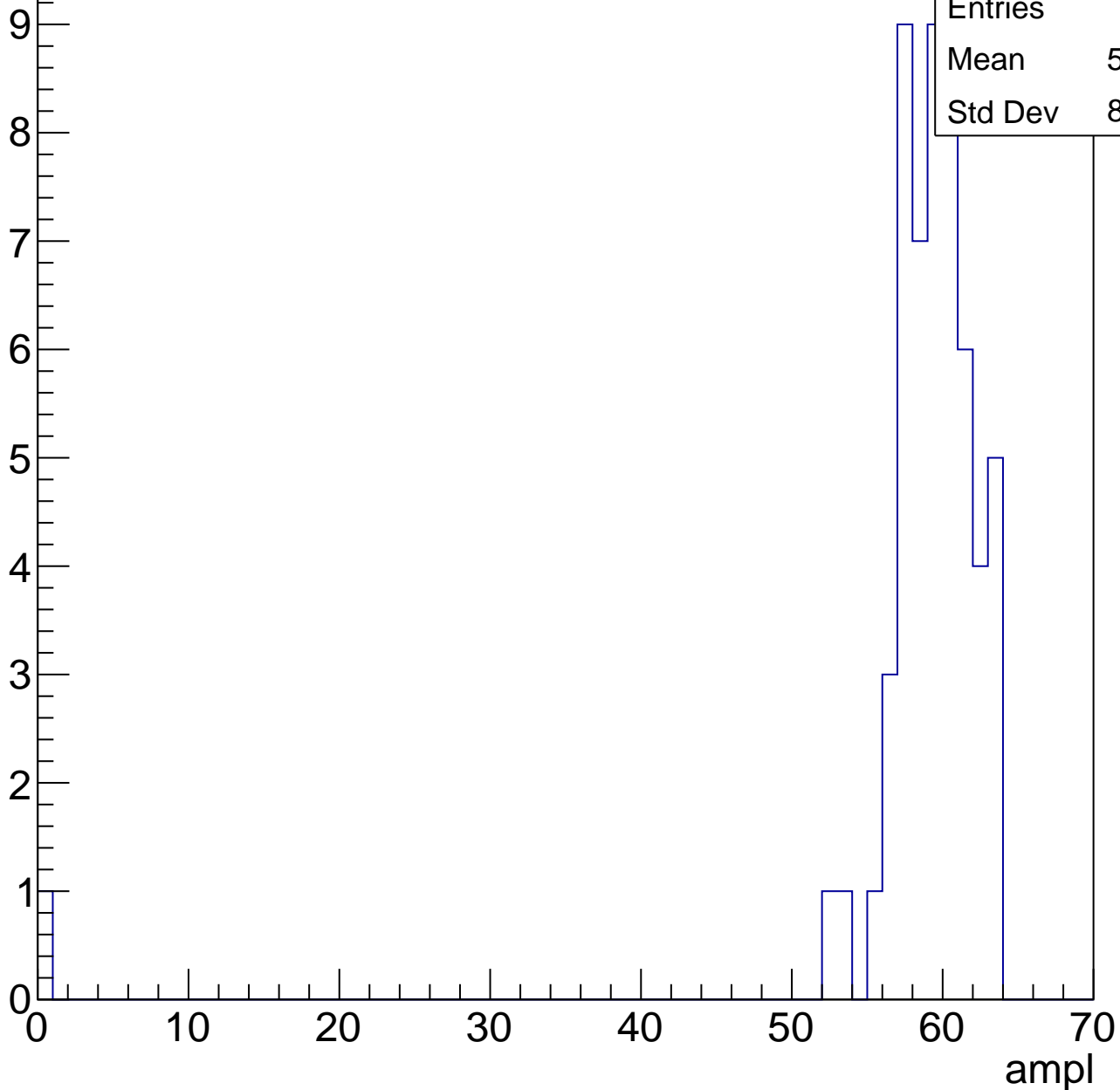


# B1L103S, U3-ch26, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	55
Mean	57.95
Std Dev	8.245

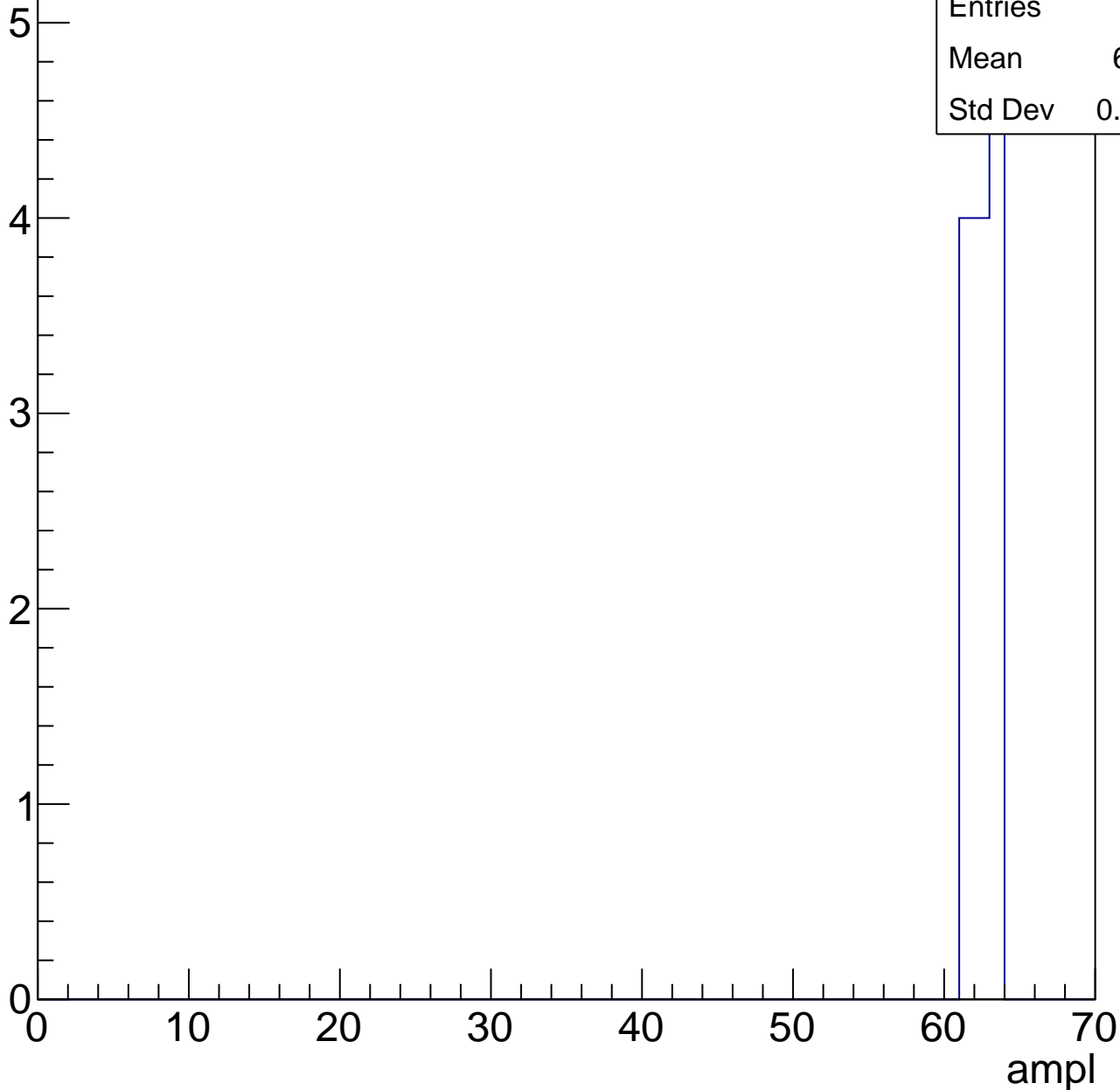


# B1L103S, U3-ch26, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	13
Mean	62.08
Std Dev	0.8285





# B1L103S, U3-ch26, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51

Entry



# B1L103S, U3-ch27, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	103
Mean	24.57
Std Dev	11.1

**Gaus mean : 28.9723**

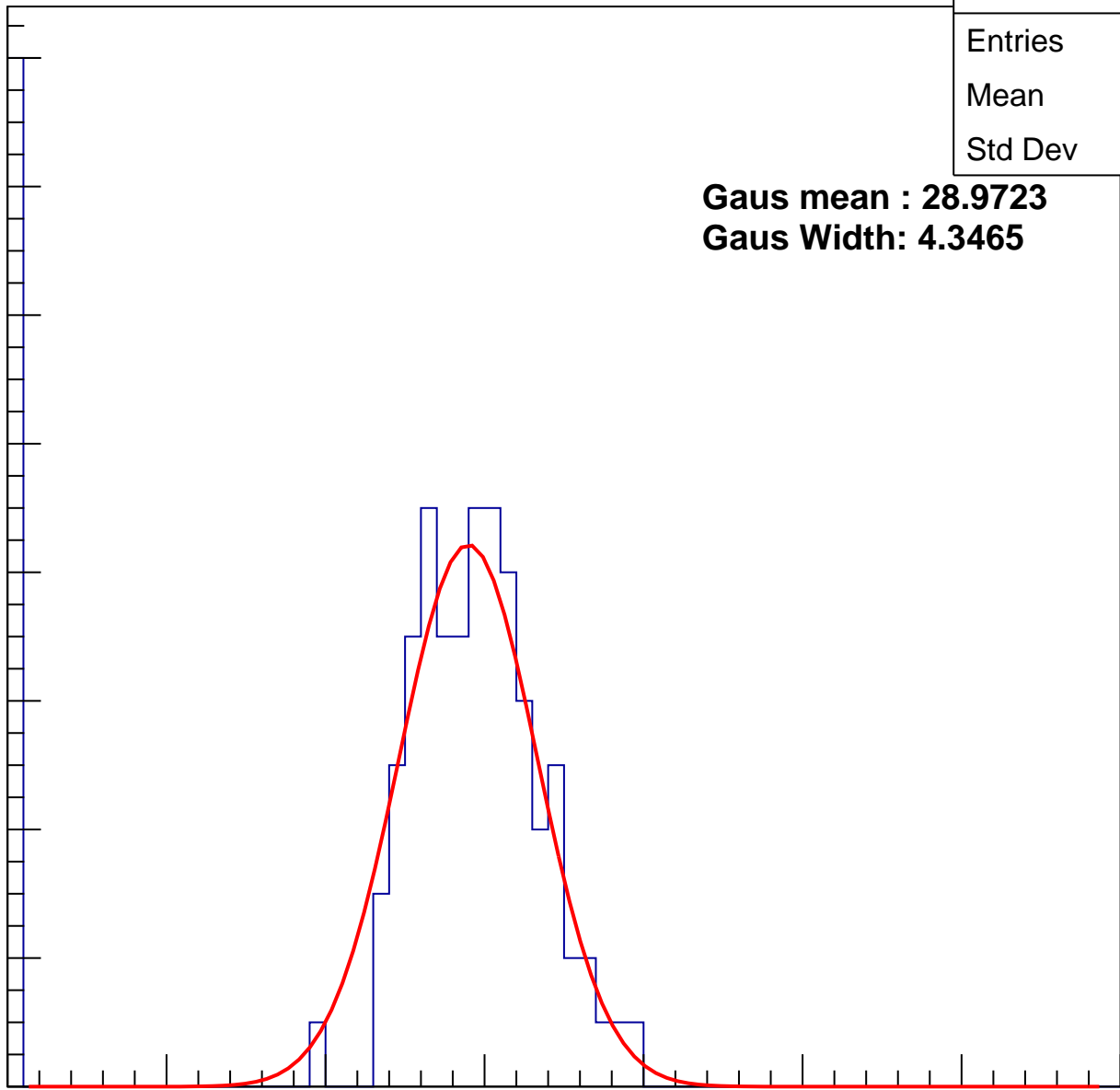
**Gaus Width: 4.3465**

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch27, adc1

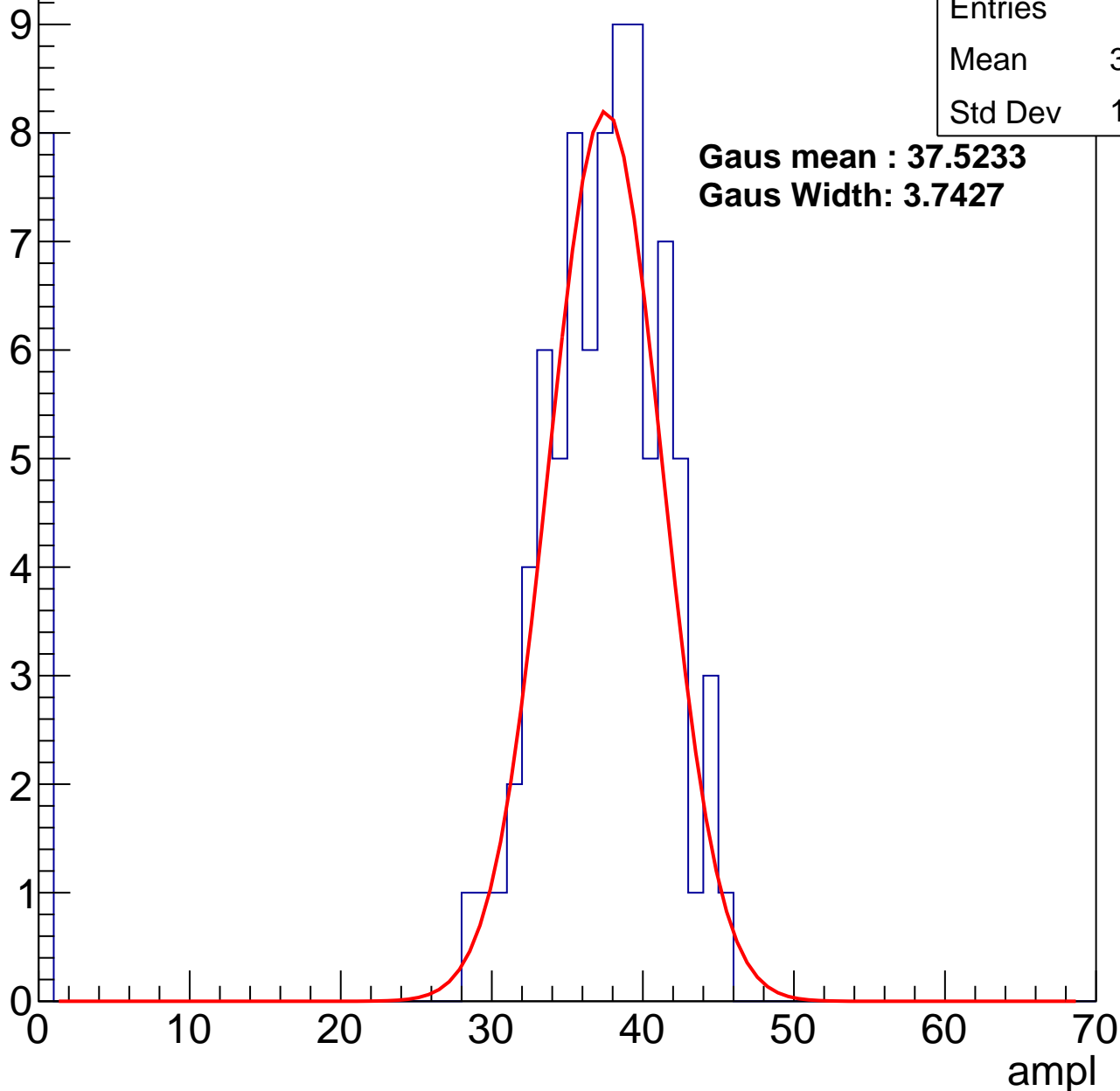
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	90
Mean	33.86
Std Dev	11.15

**Gaus mean : 37.5233**

**Gaus Width: 3.7427**

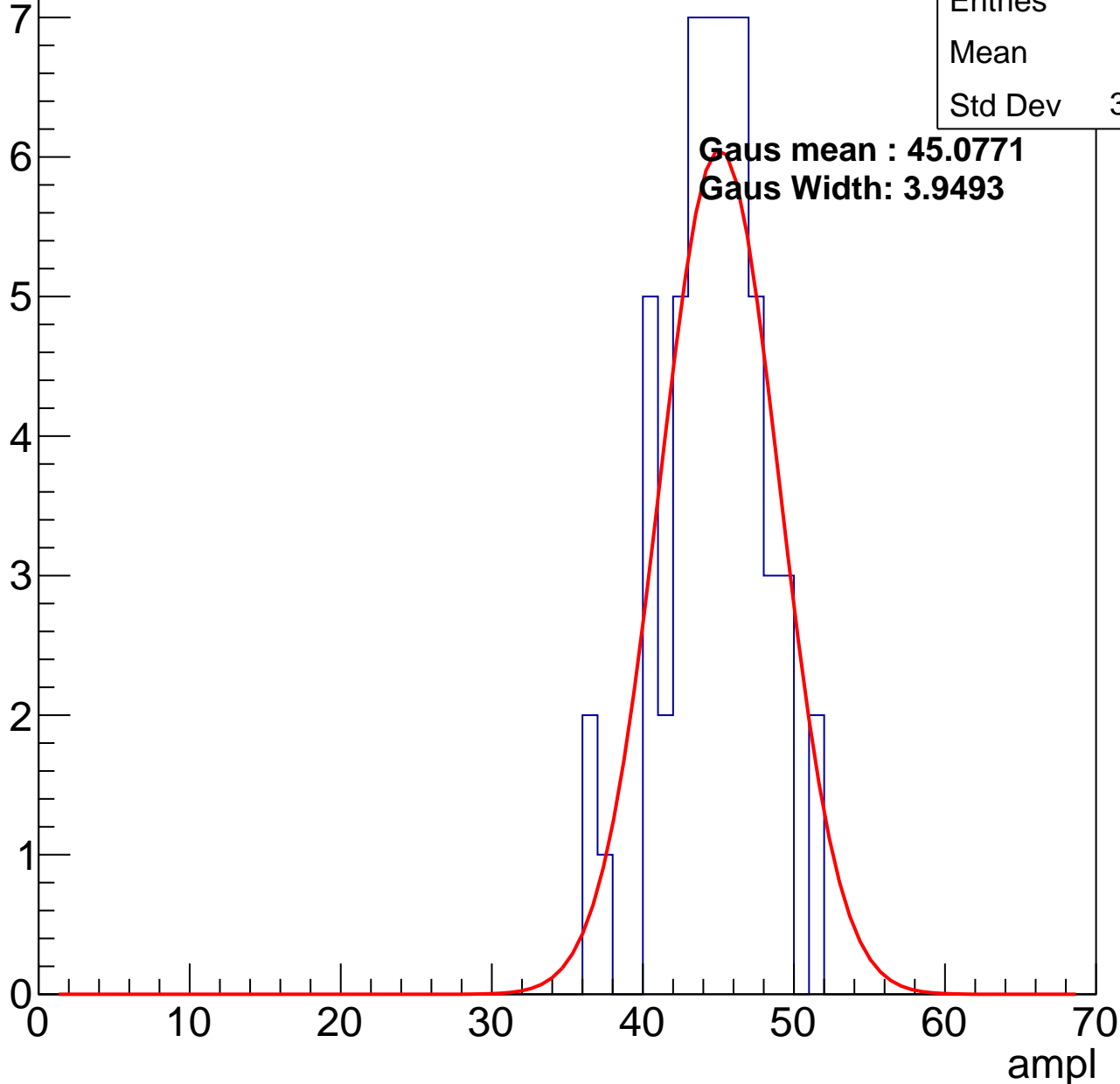


# B1L103S, U3-ch27, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	56
Mean	44.2
Std Dev	3.276

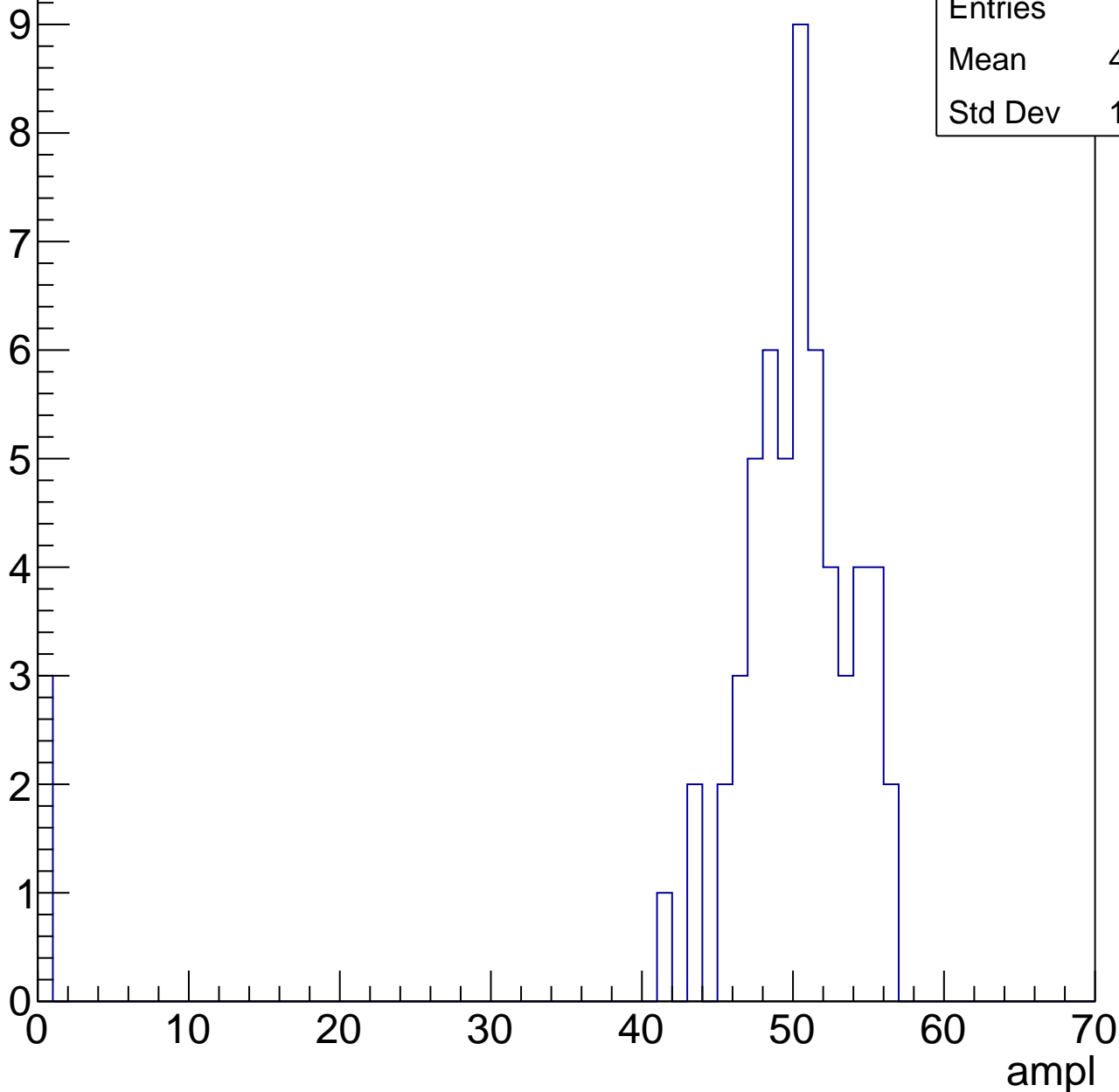


# B1L103S, U3-ch27, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	47.36
Std Dev	11.44

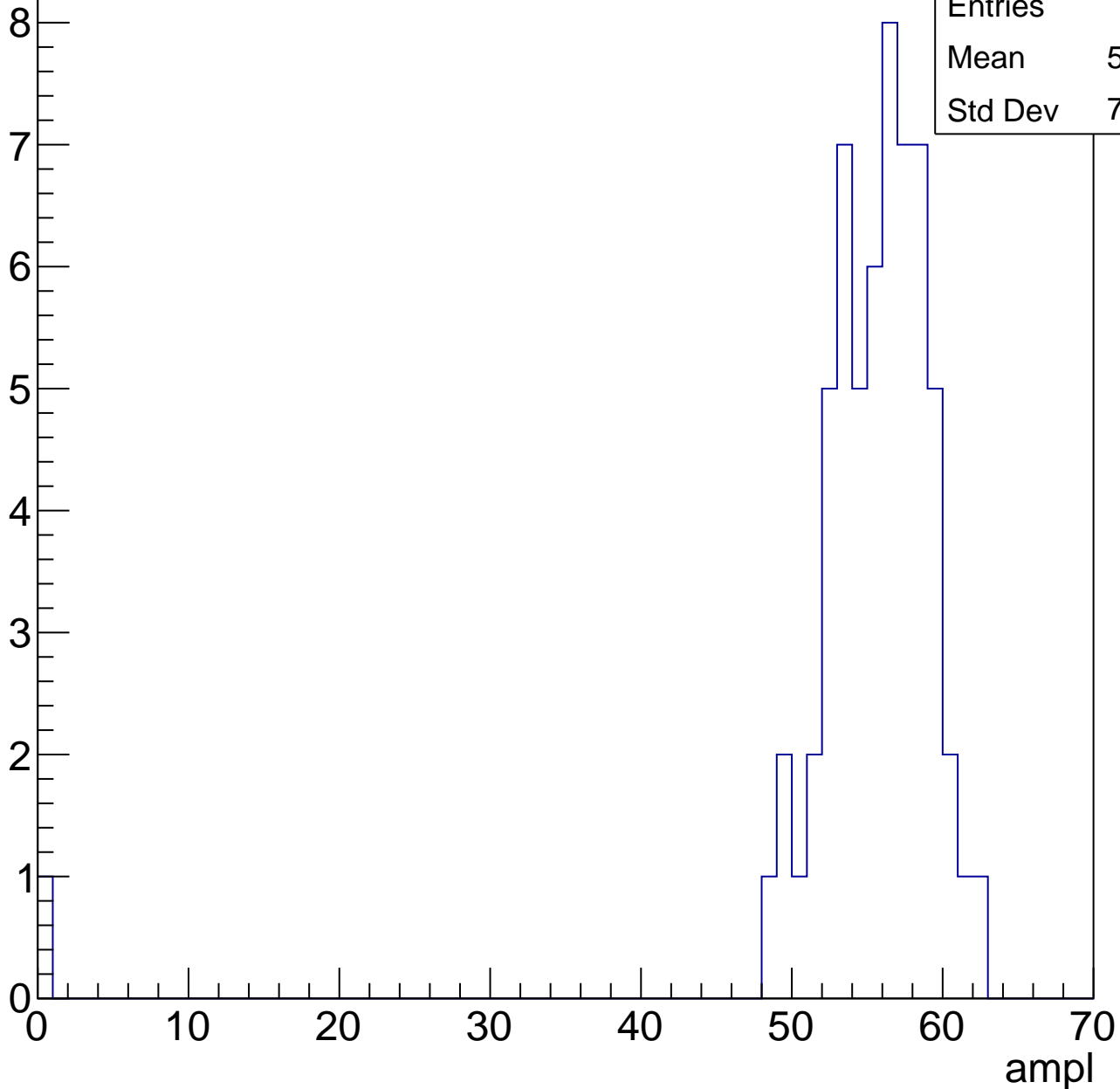


# B1L103S, U3-ch27, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	54.43
Std Dev	7.655



# B1L103S, U3-ch27, adc5

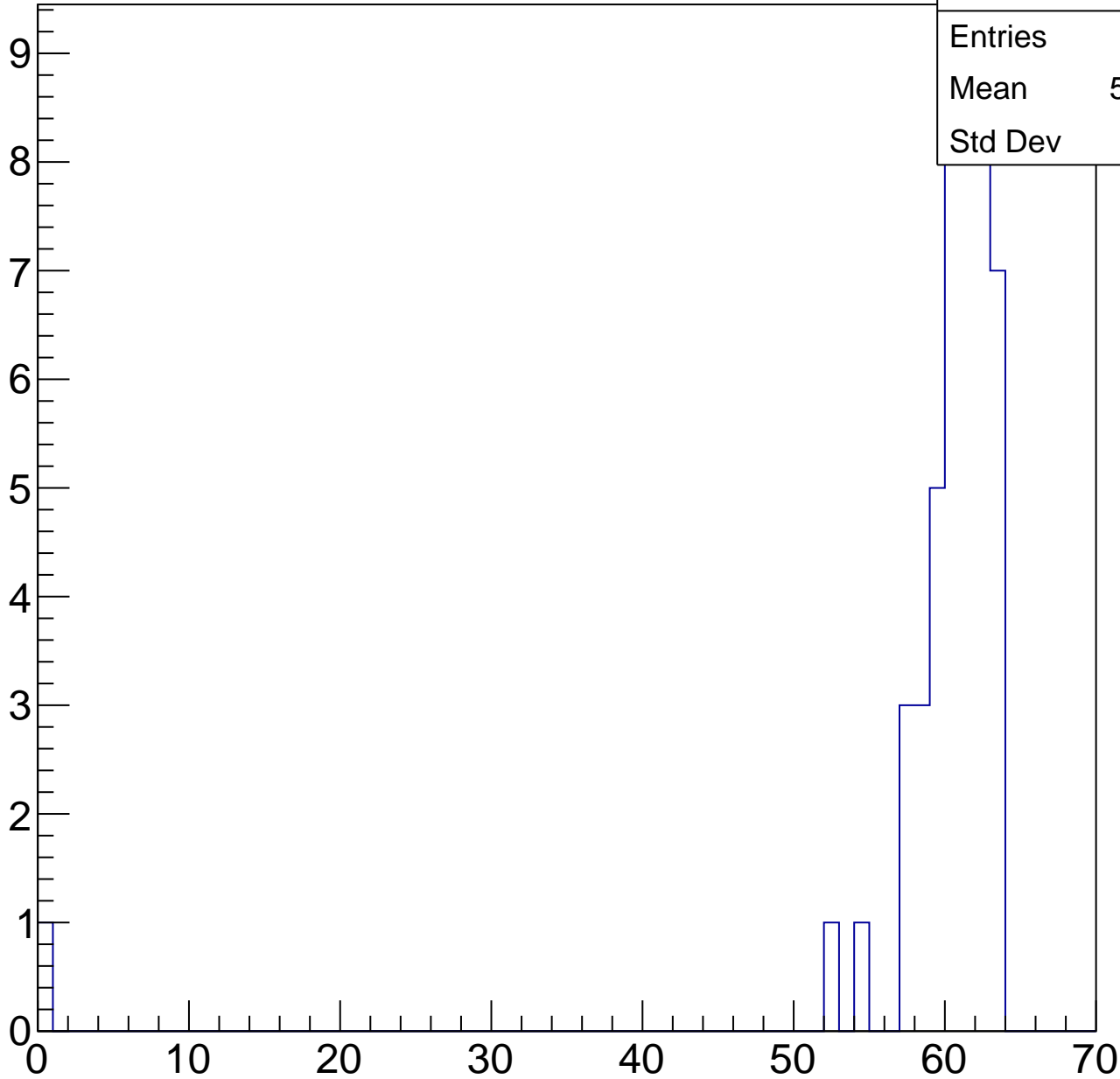
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	47
Mean	59.02
Std Dev	9

ampl



# B1L103S, U3-ch27, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U3-ch27, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	18
Mean	0
Std Dev	0

ampl

# B1L103S, U3-ch28, adc0

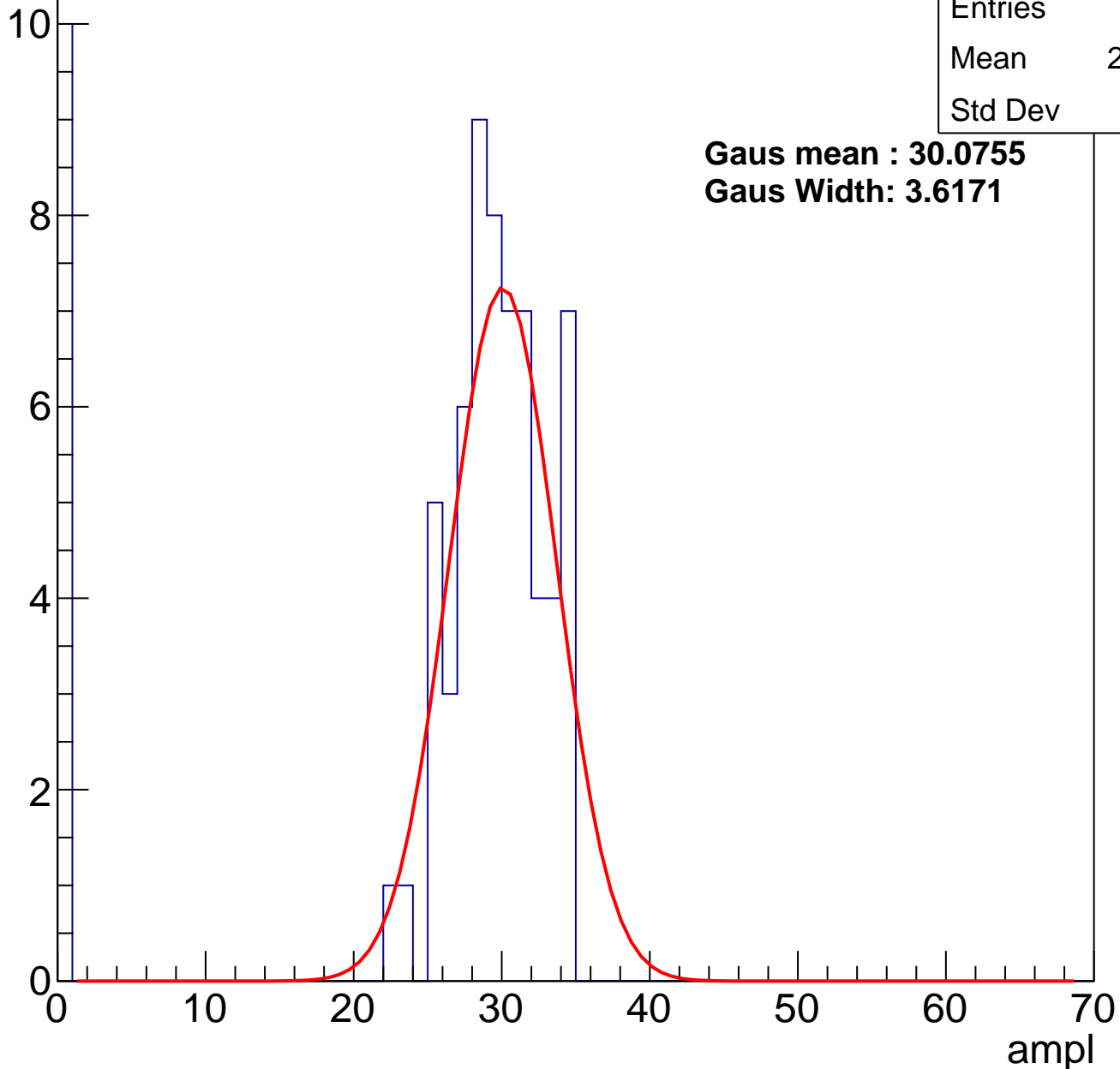
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	72
Mean	25.26
Std Dev	10.5

**Gaus mean : 30.0755**

**Gaus Width: 3.6171**

Entry



# B1L103S, U3-ch28, adc1

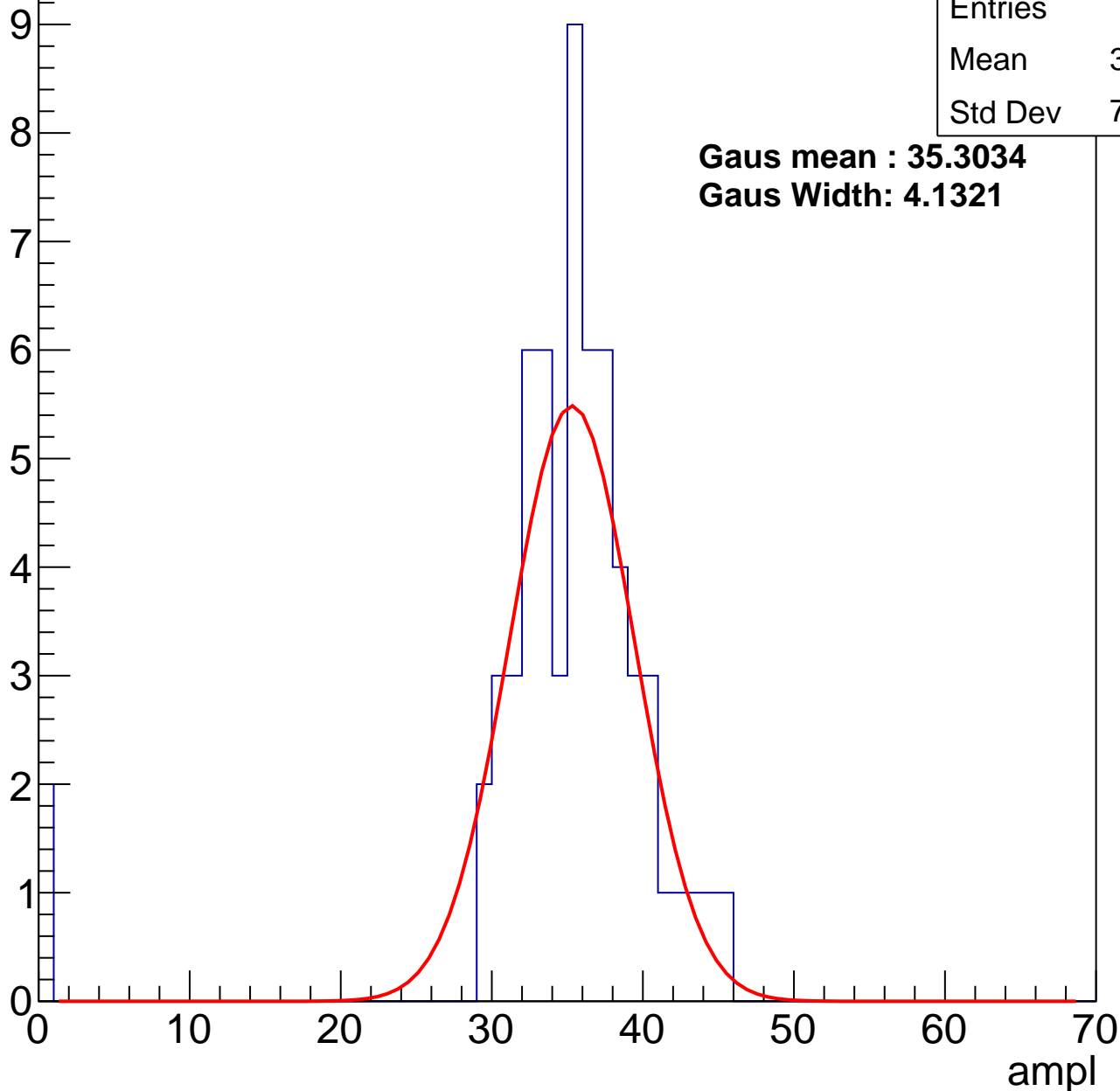
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	34.26
Std Dev	7.256

**Gaus mean : 35.3034**

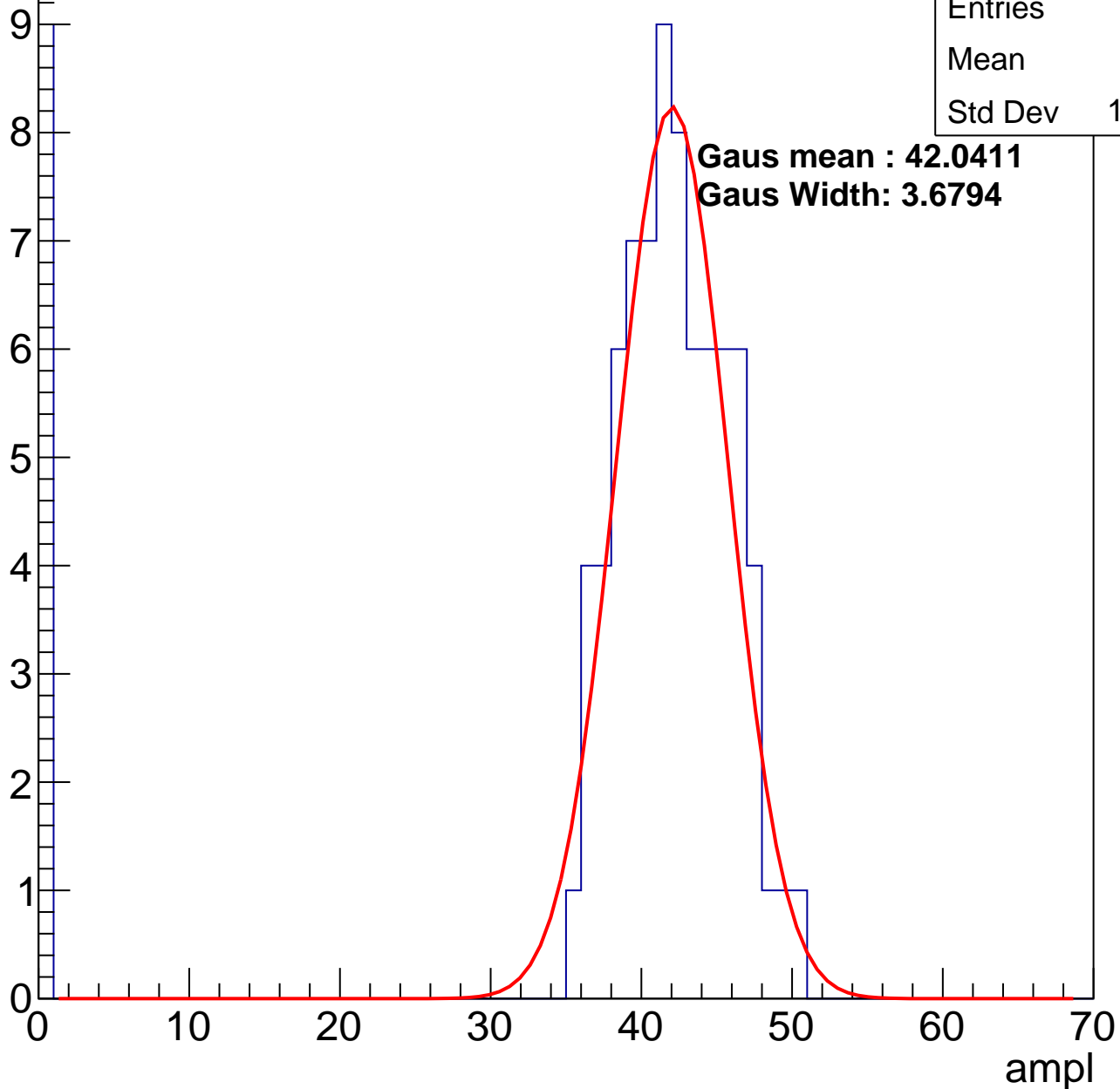
**Gaus Width: 4.1321**



# B1L103S, U3-ch28, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

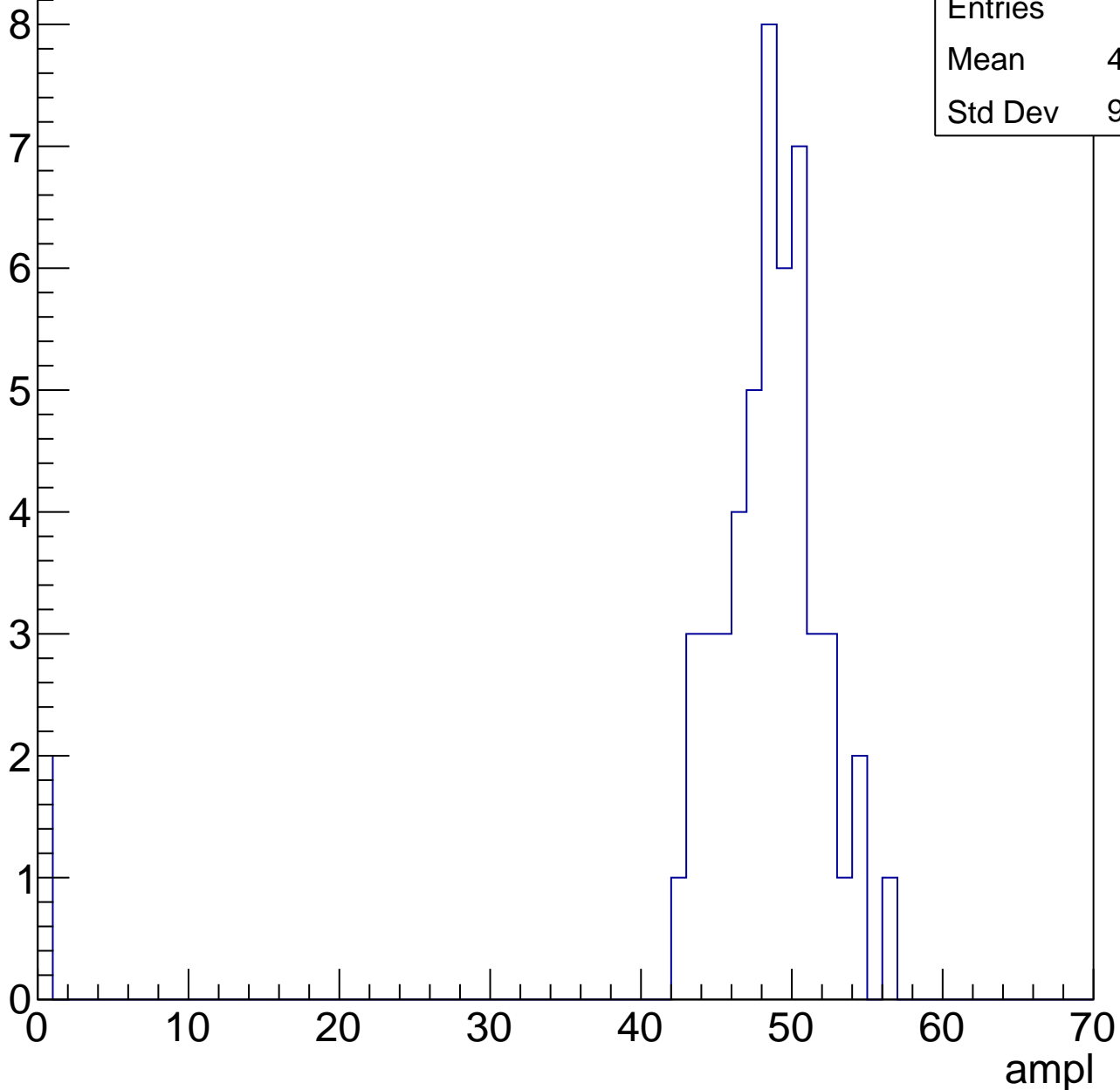


# B1L103S, U3-ch28, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

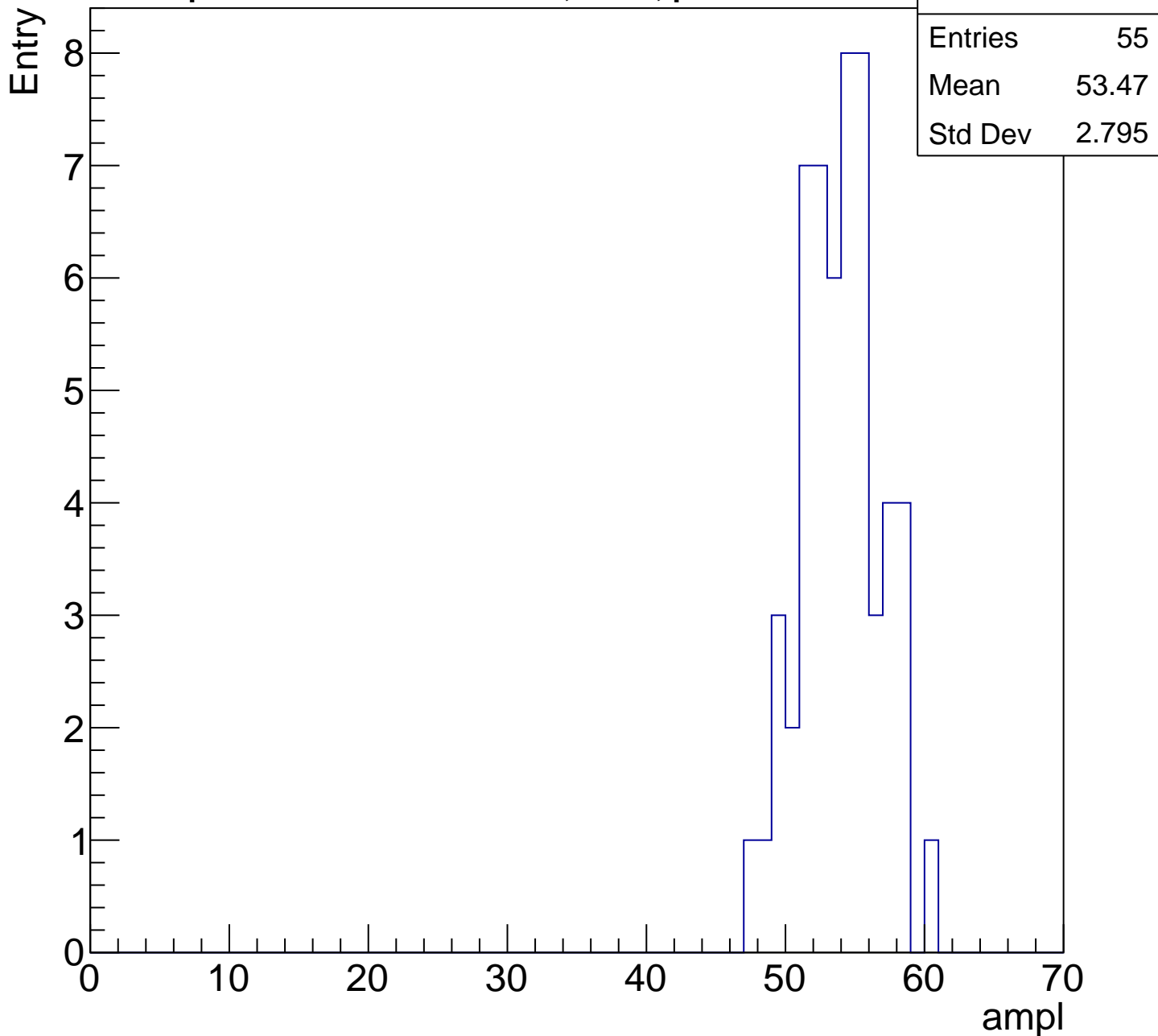
Entry

Entries	52
Mean	46.37
Std Dev	9.753



# B1L103S, U3-ch28, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

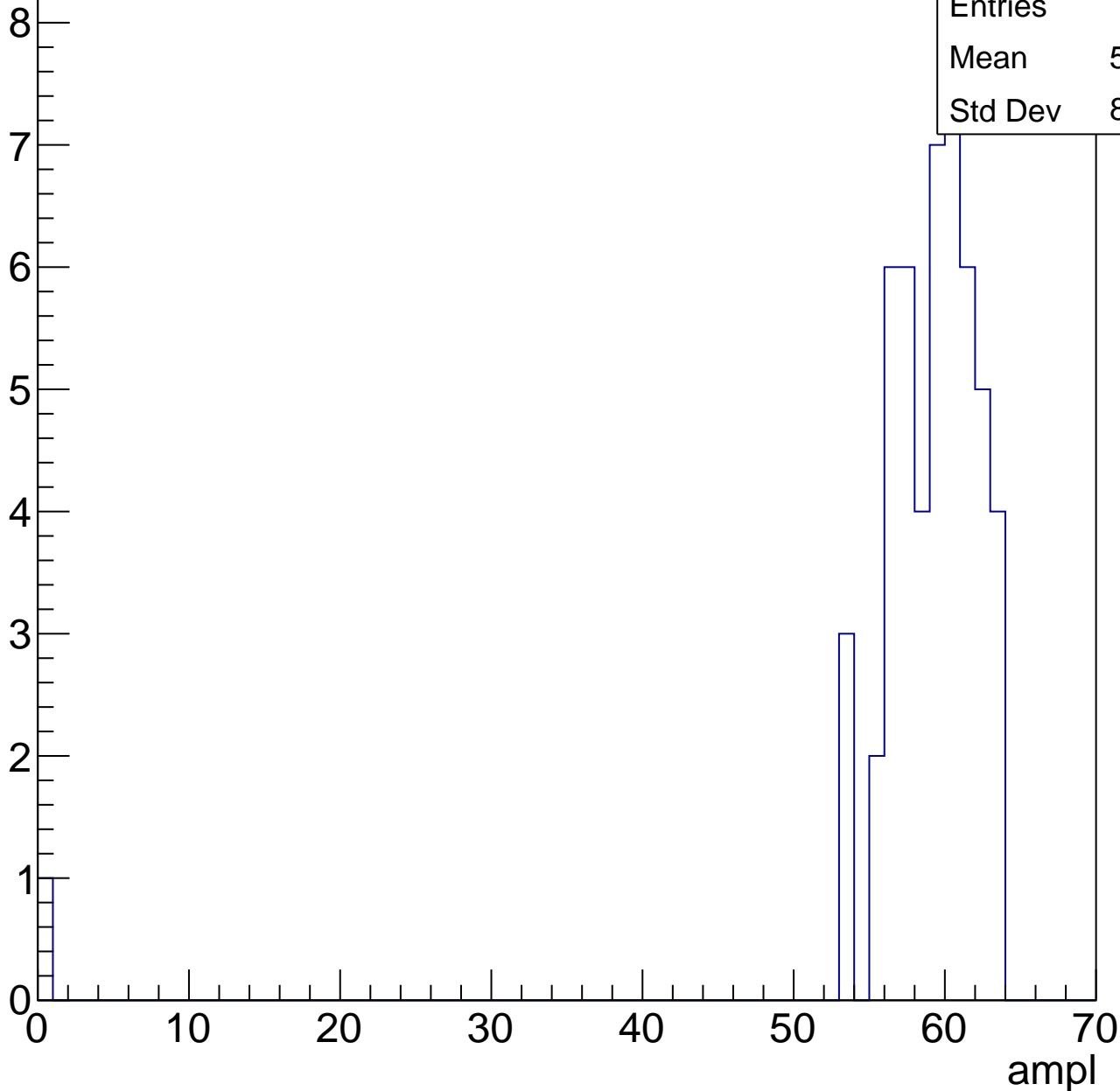


# B1L103S, U3-ch28, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	52
Mean	57.69
Std Dev	8.498

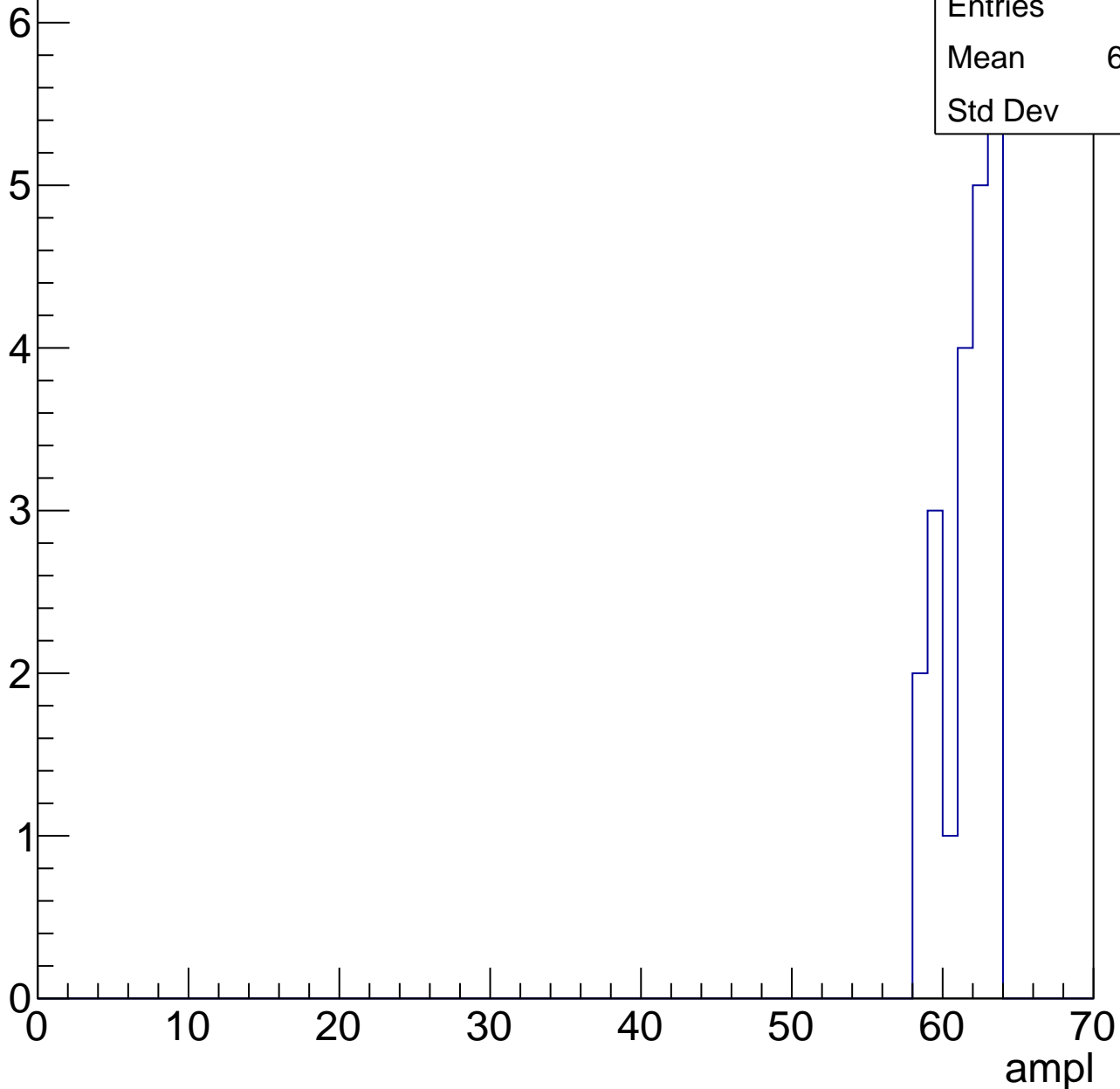


# B1L103S, U3-ch28, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	21
Mean	61.19
Std Dev	1.68





# B1L103S, U3-ch28, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	19
Mean	0
Std Dev	0

ampl

# B1L103S, U3-ch29, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	91
Mean	20.52
Std Dev	13.61

**Gaus mean : 29.6952**

**Gaus Width: 3.4240**

Entry

25

20

15

10

5

0

0

10

20

30

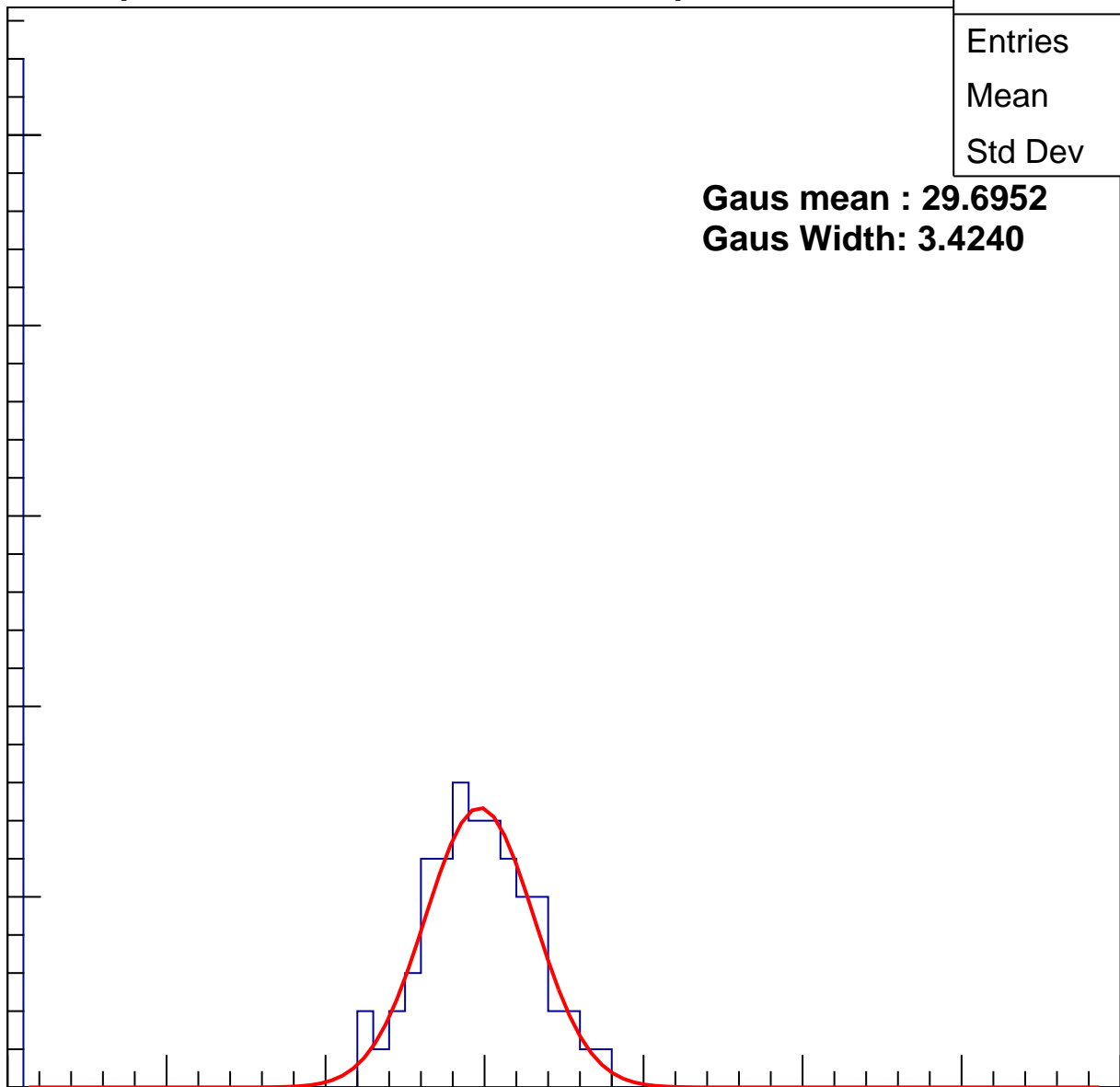
40

50

60

70

ampl



# B1L103S, U3-ch29, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	84
Mean	29.44
Std Dev	14.04

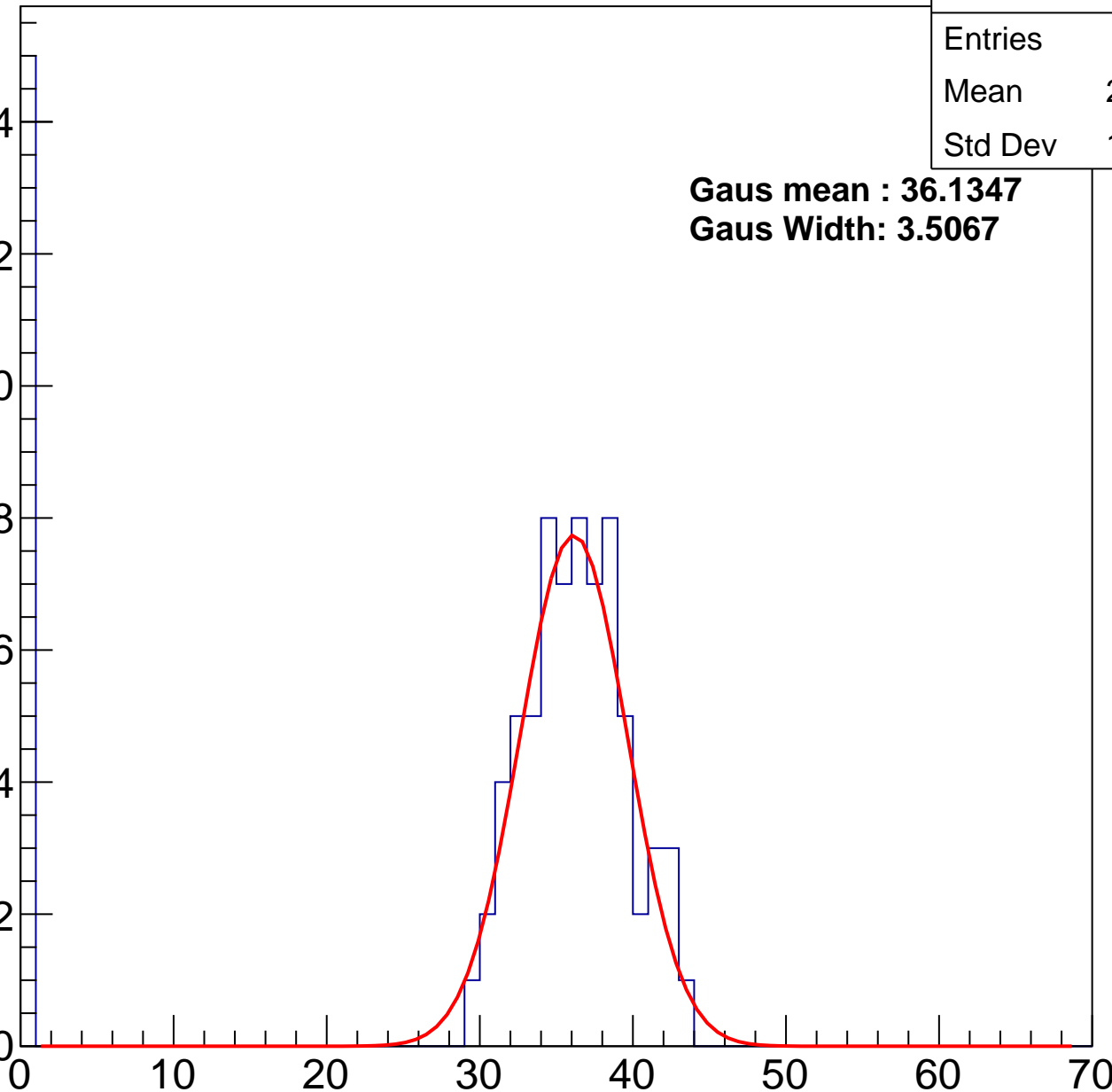
**Gaus mean : 36.1347**

**Gaus Width: 3.5067**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U3-ch29, adc2

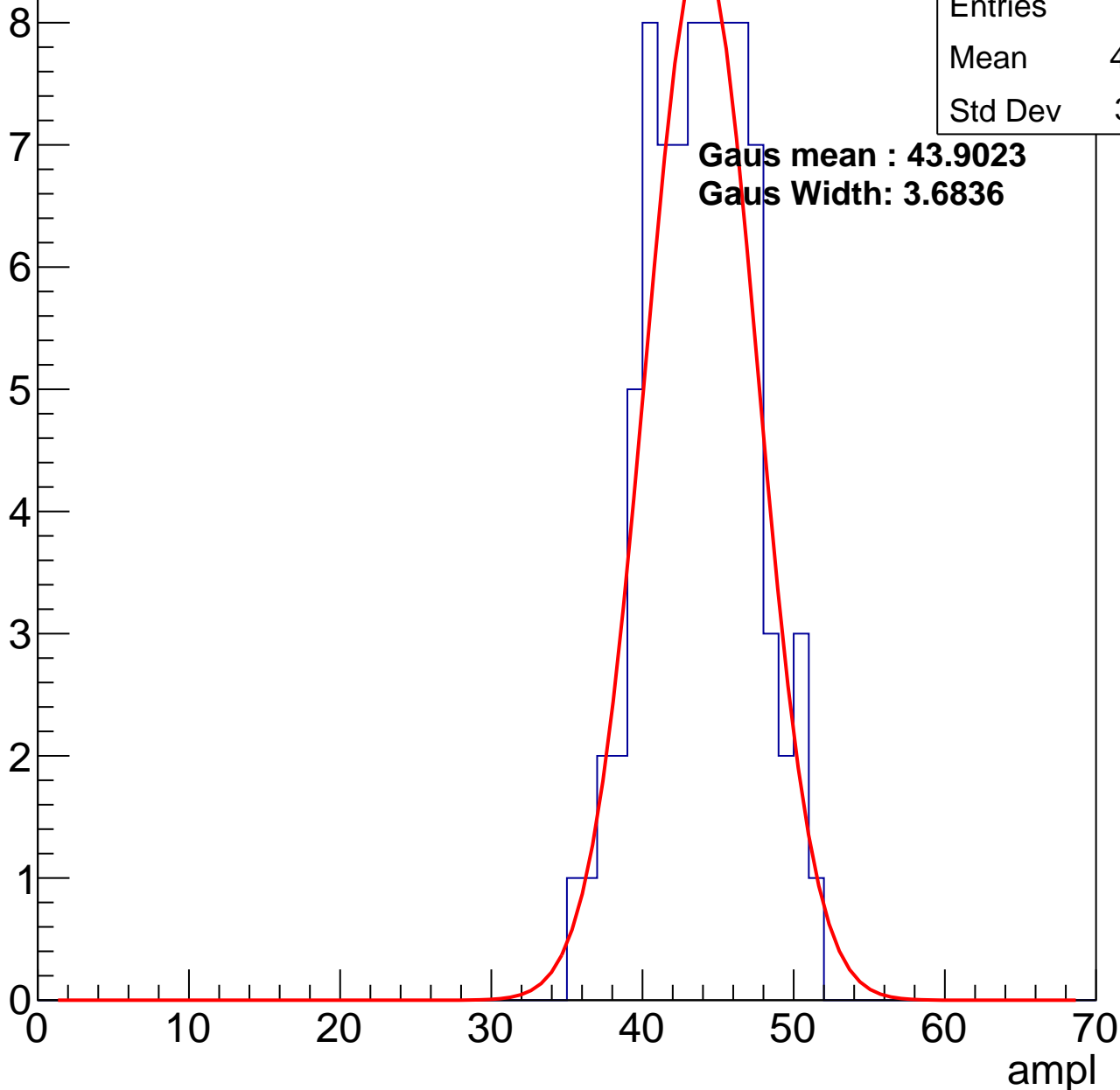
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	81
Mean	43.37
Std Dev	3.501

**Gaus mean : 43.9023**

**Gaus Width: 3.6836**

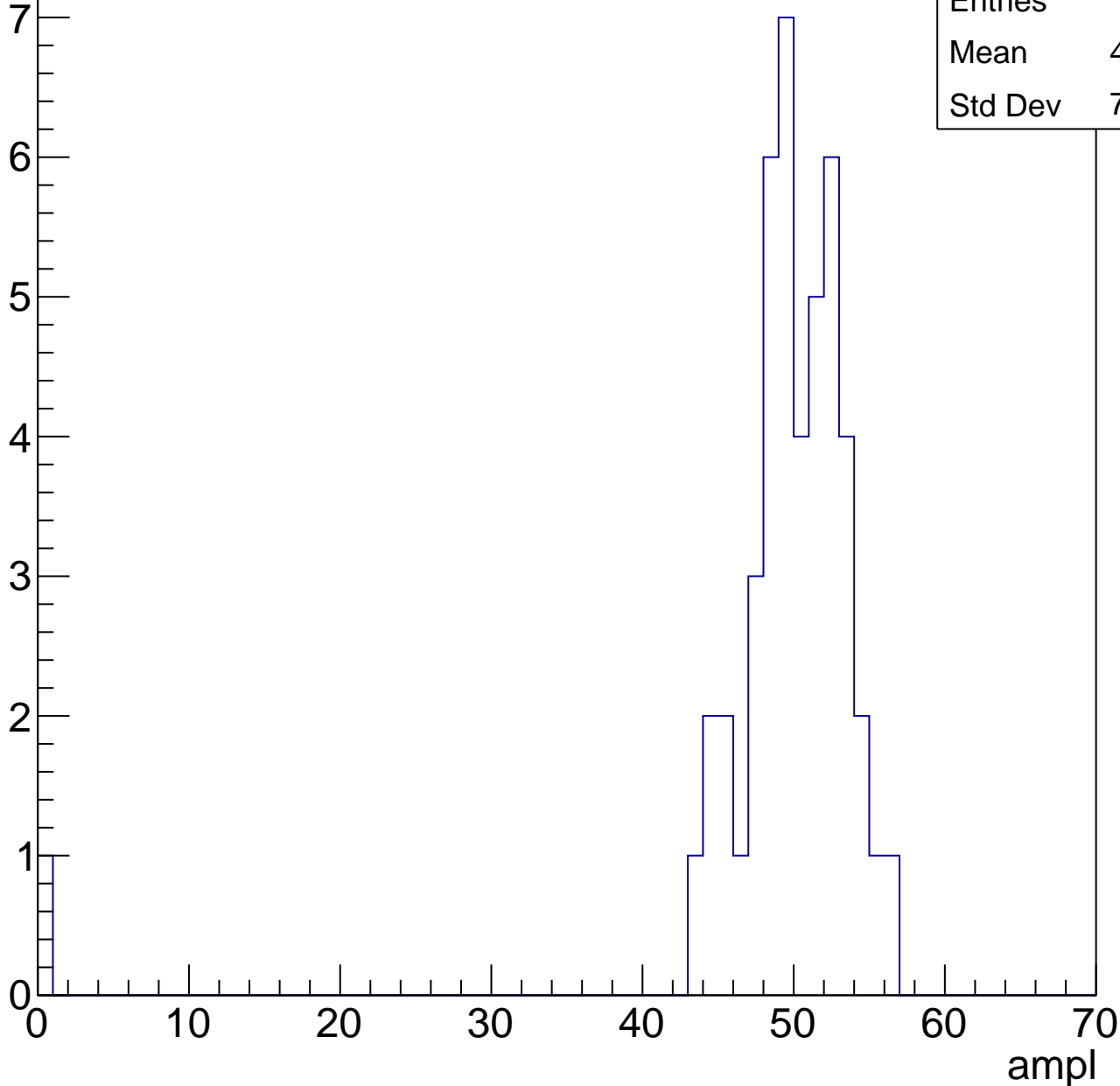


# B1L103S, U3-ch29, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	46
Mean	48.63
Std Dev	7.825

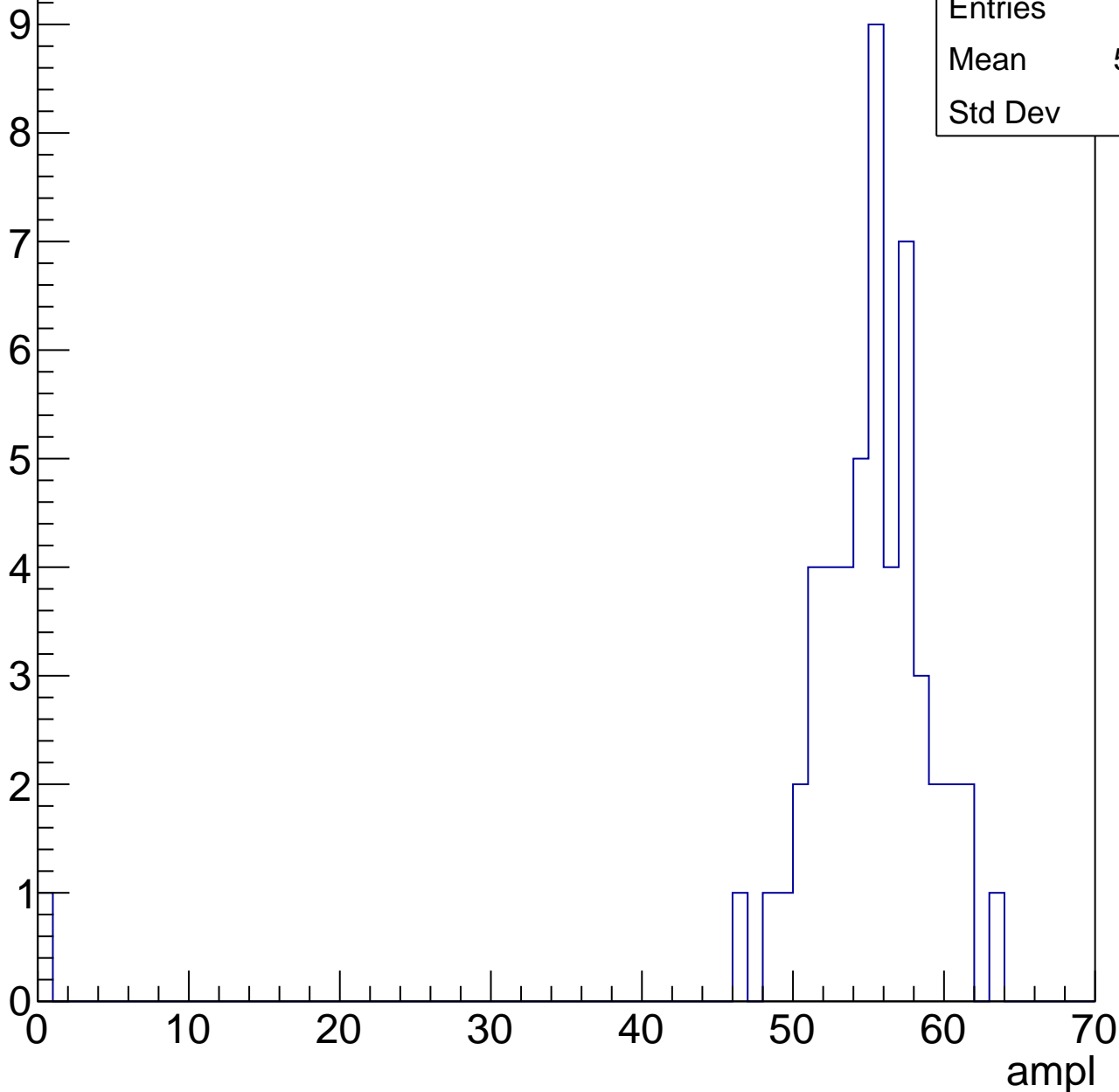


# B1L103S, U3-ch29, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

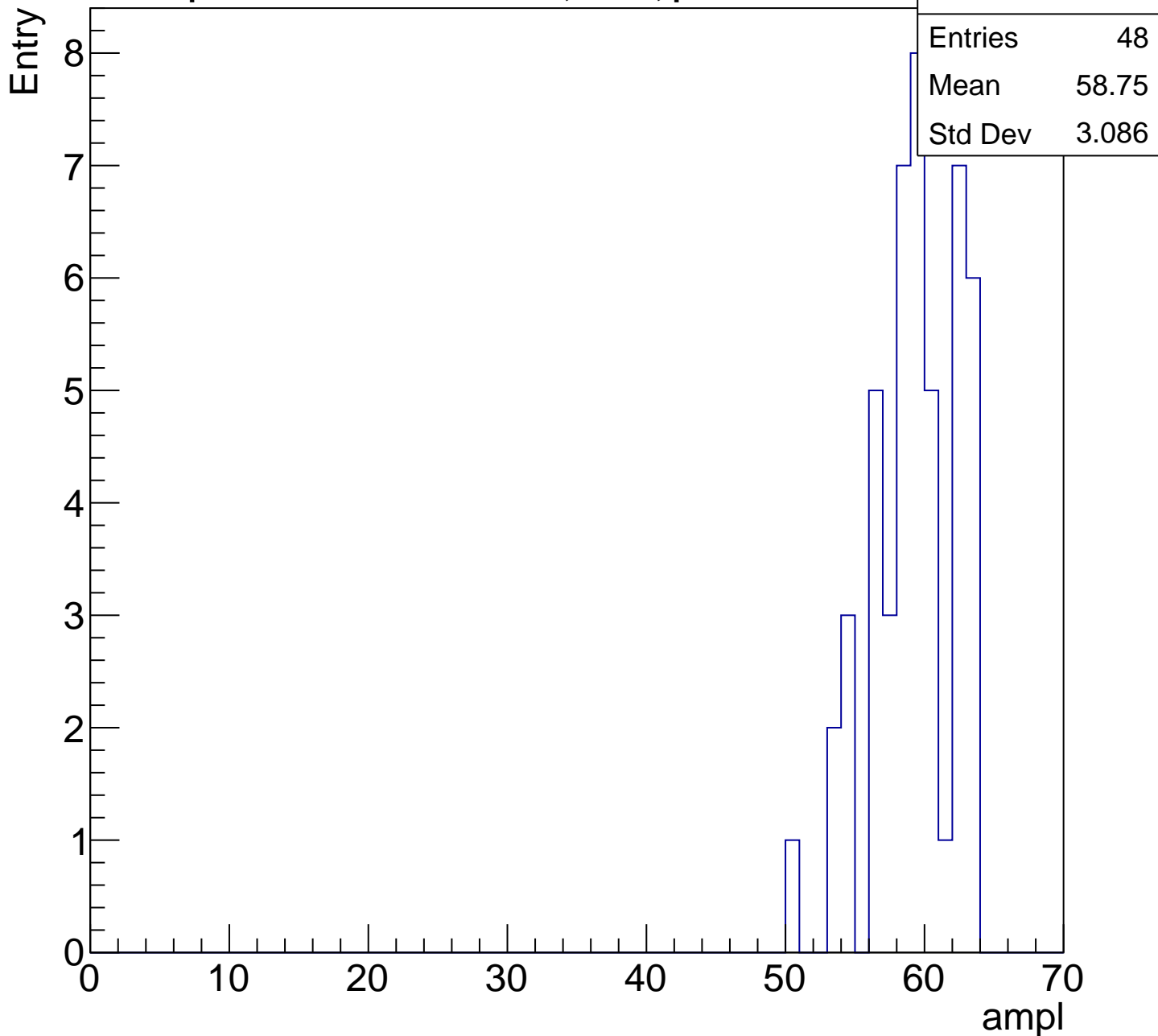
Entry

Entries	53
Mean	53.81
Std Dev	8.2



# B1L103S, U3-ch29, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

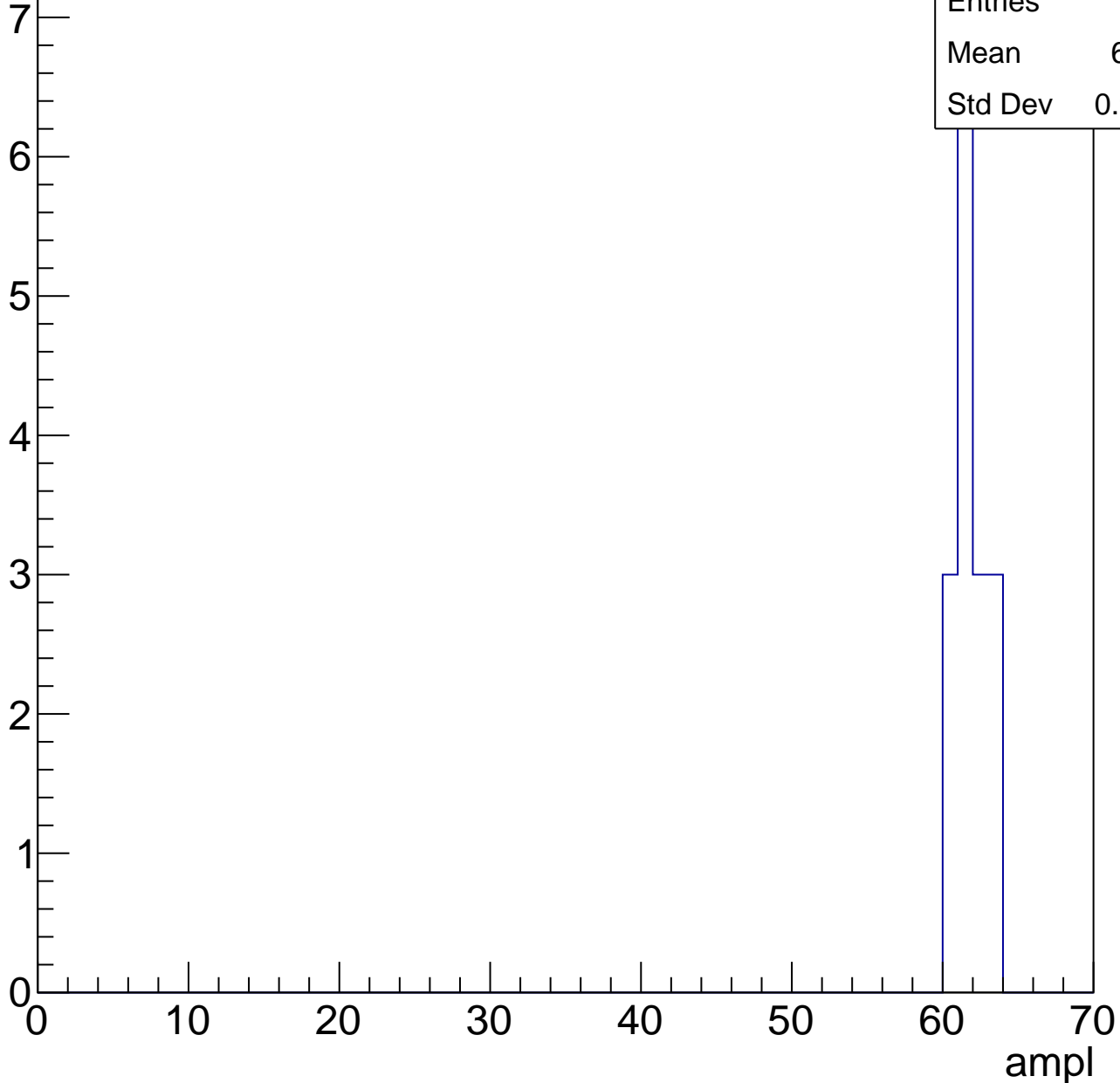


# B1L103S, U3-ch29, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	16
Mean	61.38
Std Dev	0.9922





# B1L103S, U3-ch29, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	19
Mean	0
Std Dev	0

ampl

# B1L103S, U3-ch30, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	88
Mean	19.48
Std Dev	12.57

**Gaus mean : 27.6018**

**Gaus Width: 3.2351**

Entry

25

20

15

10

5

0

0

10

20

30

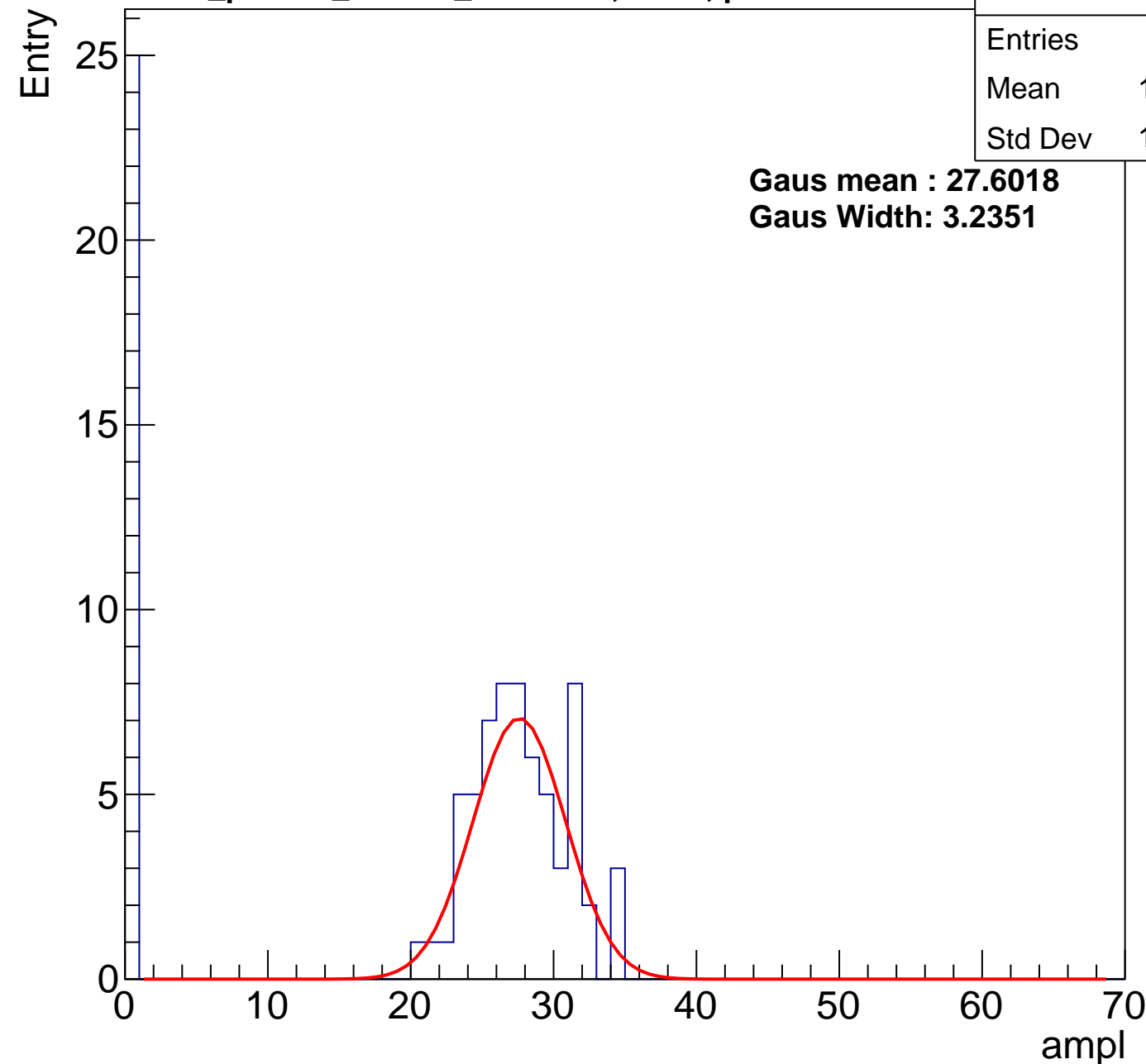
40

50

60

70

ampl



# B1L103S, U3-ch30, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	86
Mean	29.88
Std Dev	11.89

**Gaus mean : 35.0141**

**Gaus Width: 3.8527**

Entry

10

8

6

4

2

0

0

10

20

30

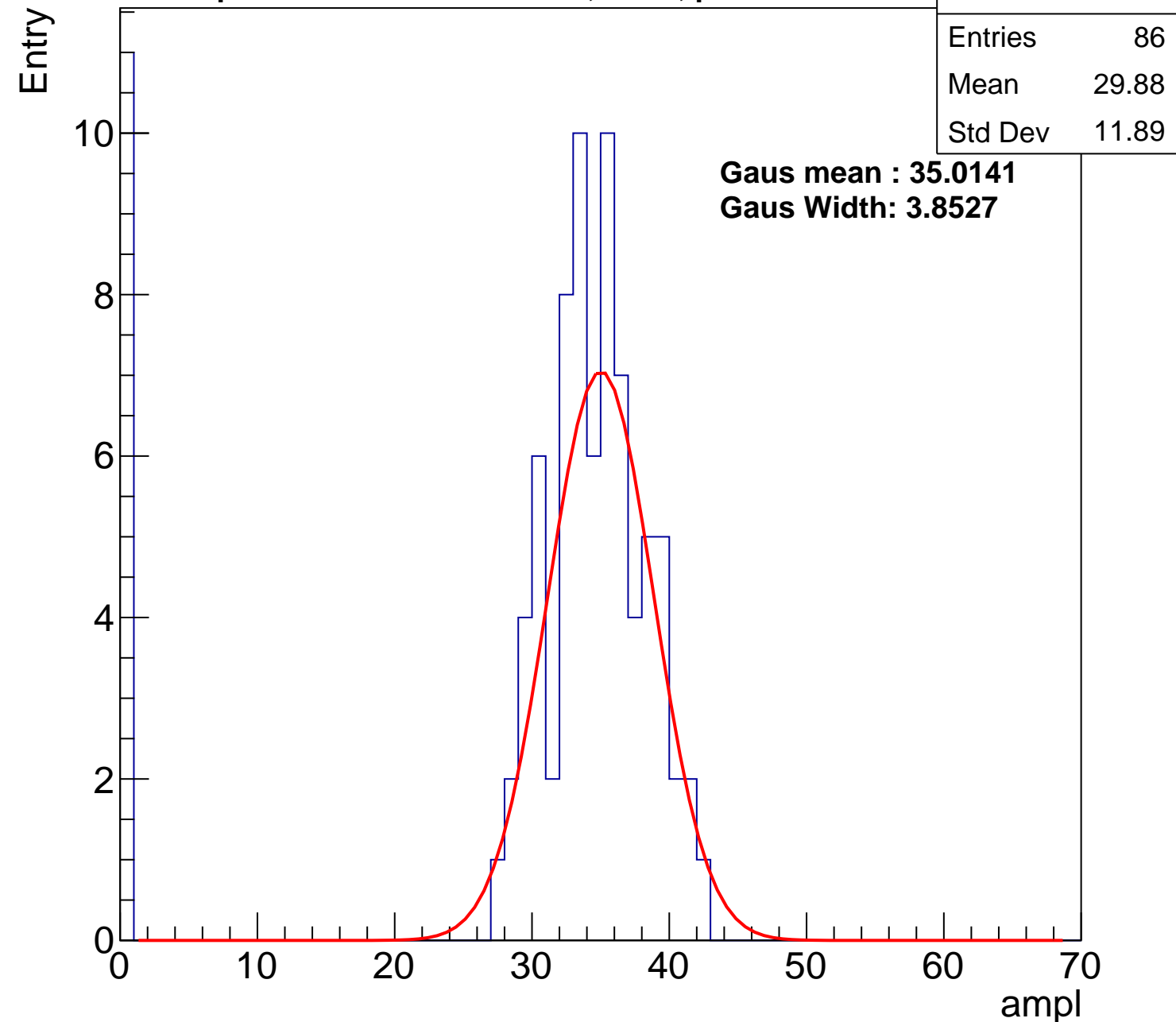
40

50

60

70

ampl



# B1L103S, U3-ch30, adc2

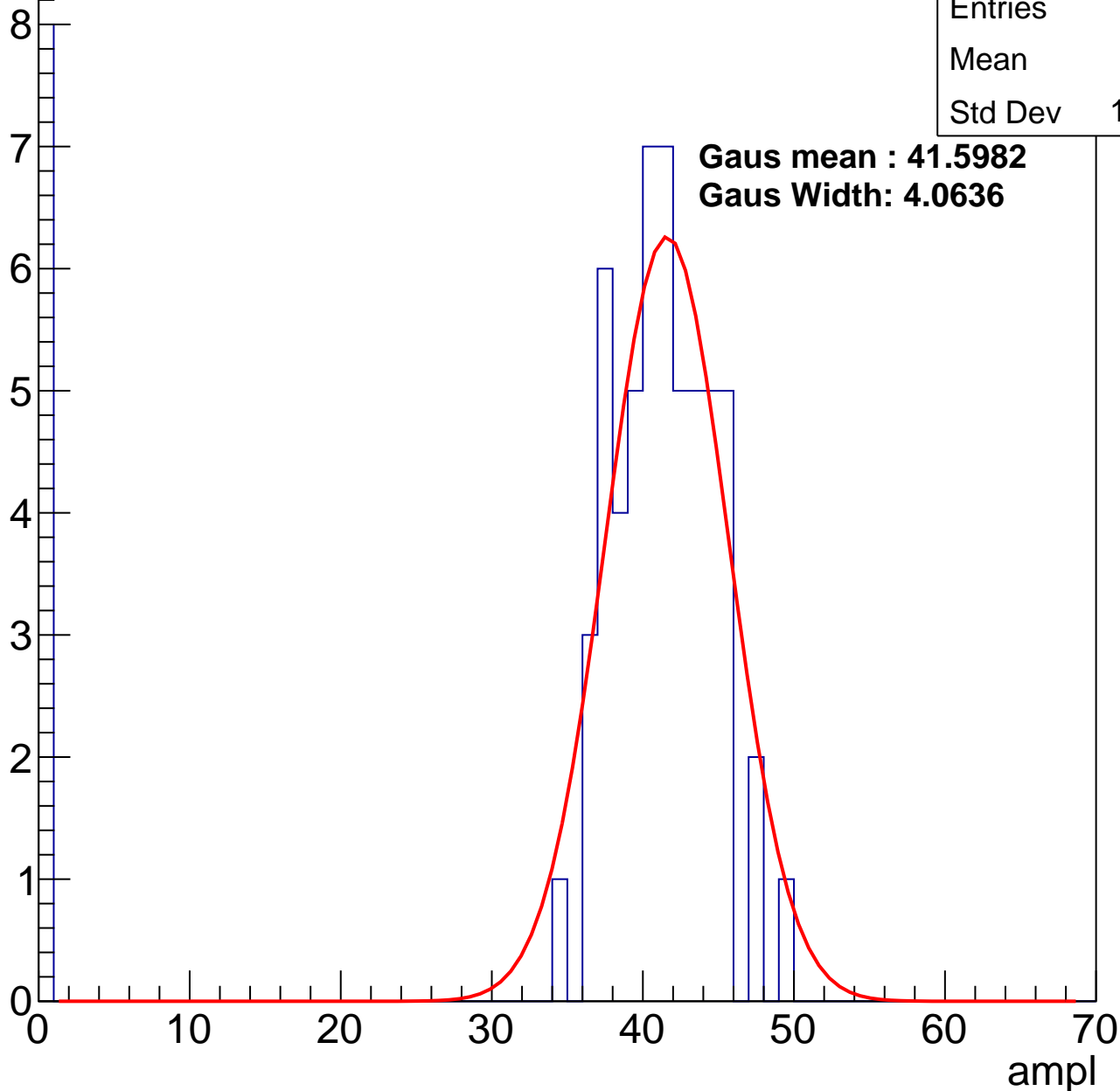
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	35.8
Std Dev	13.85

**Gaus mean : 41.5982**

**Gaus Width: 4.0636**

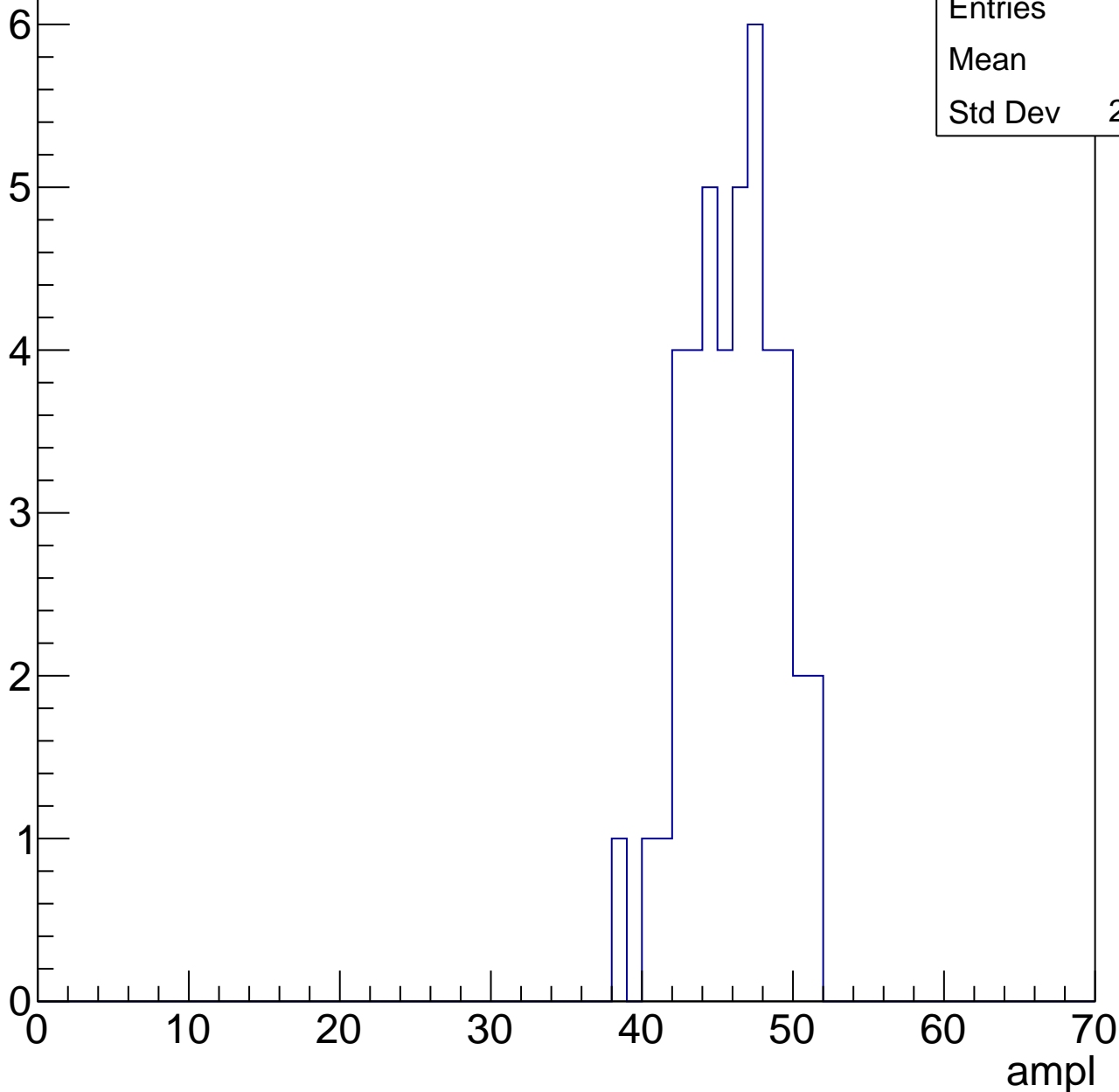


# B1L103S, U3-ch30, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

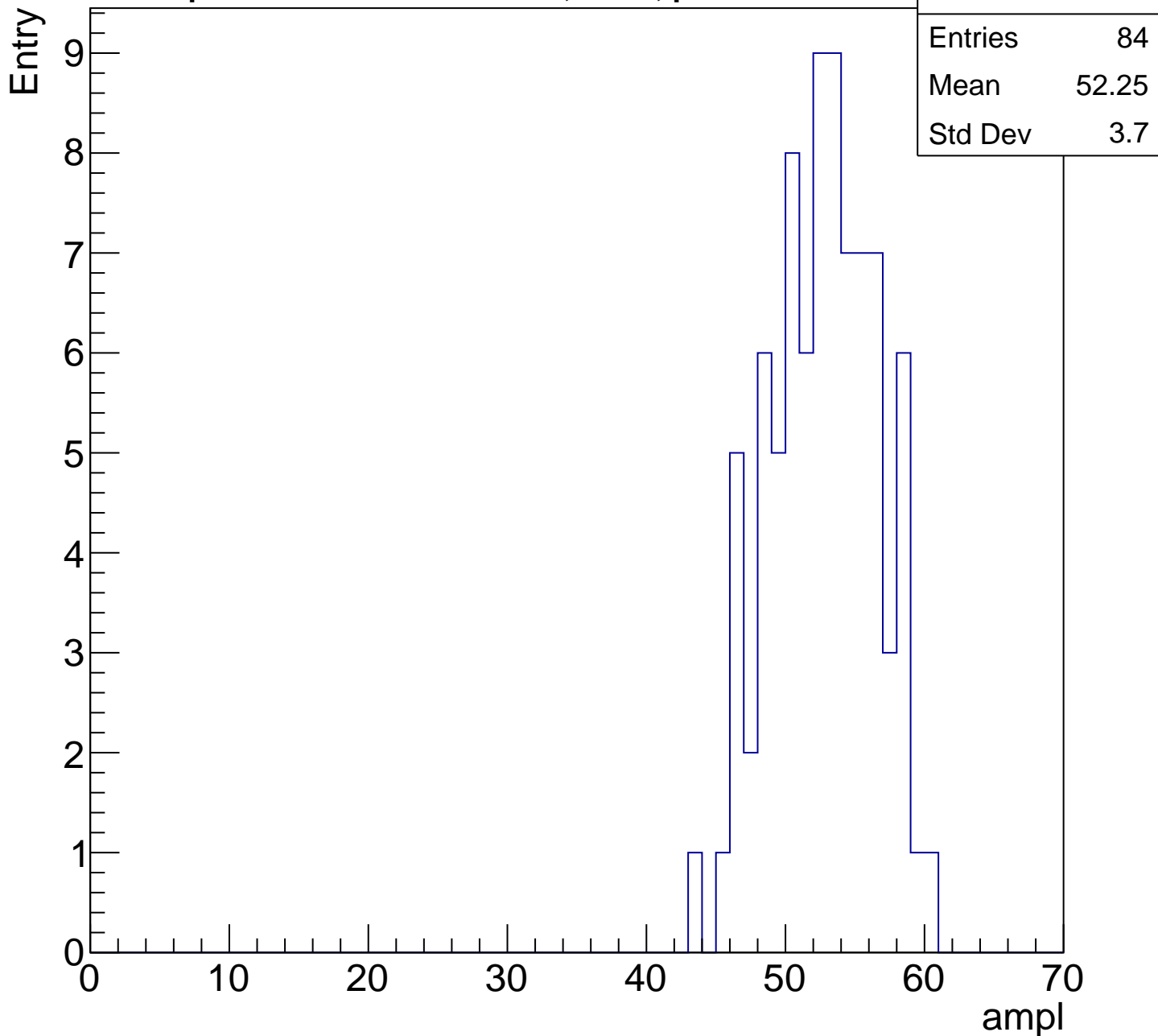
Entry

Entries	43
Mean	45.6
Std Dev	2.982



# B1L103S, U3-ch30, adc4

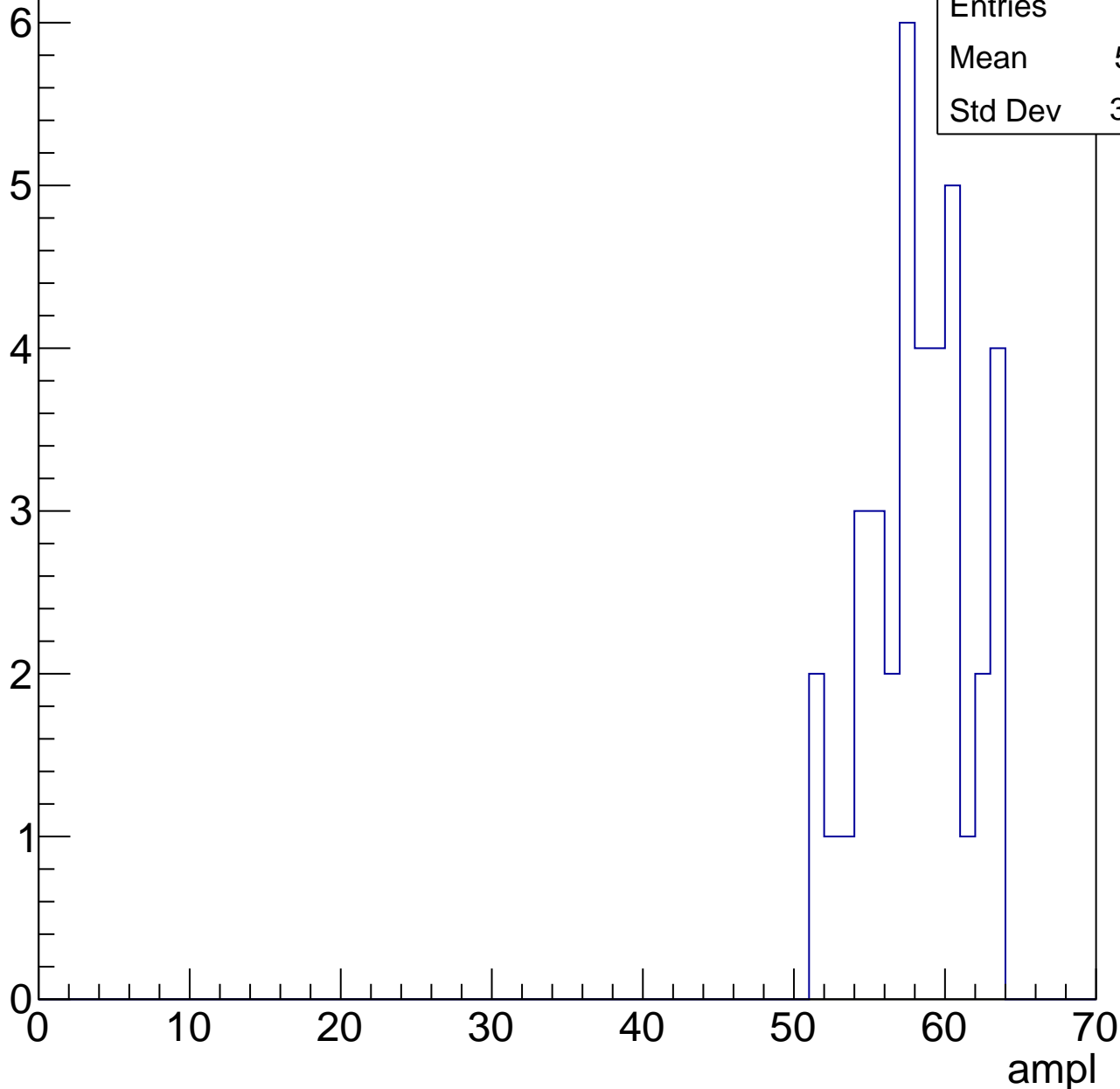
calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U3-ch30, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



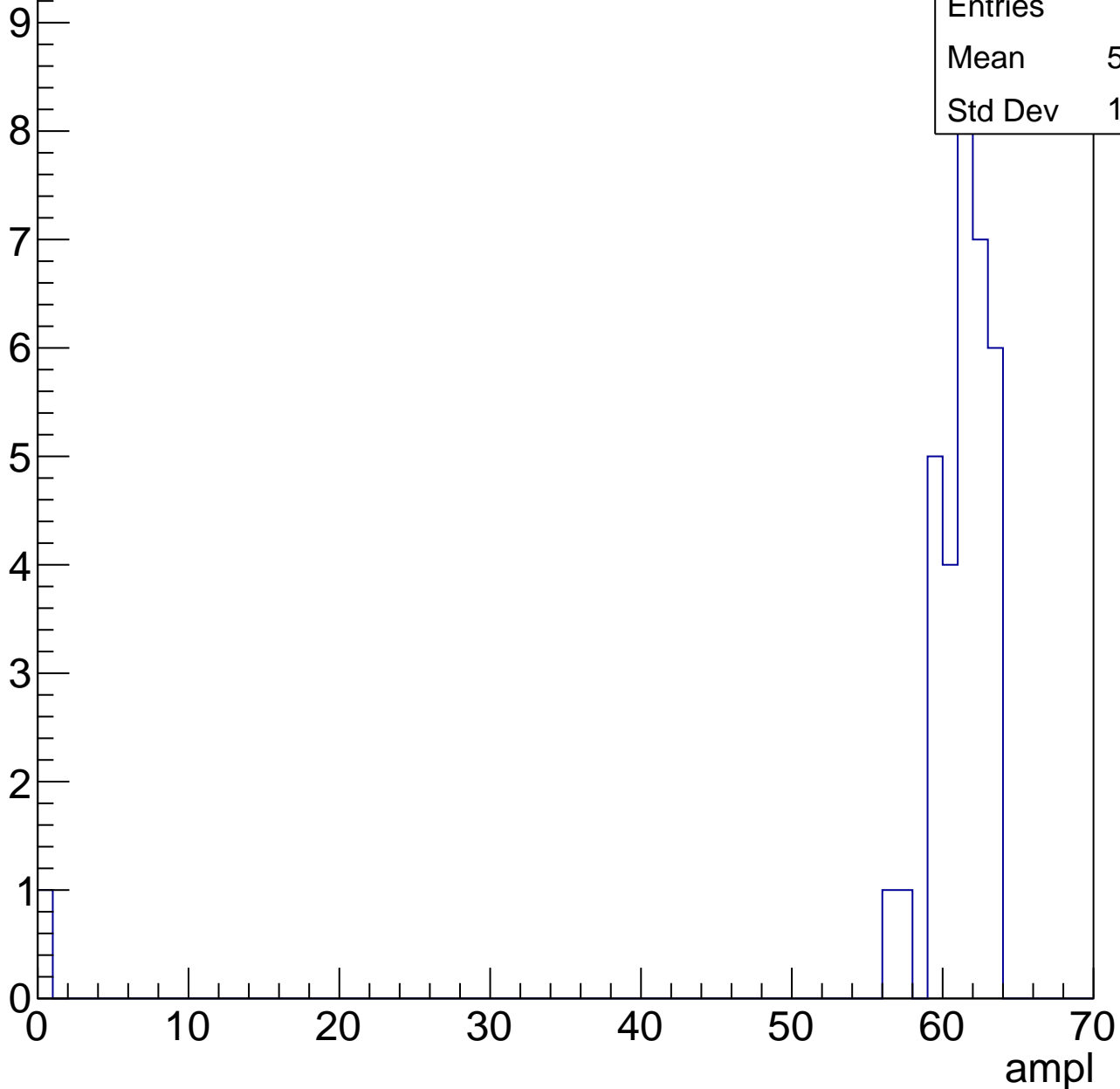
Entries	38
Mean	57.71
Std Dev	3.284

# B1L103S, U3-ch30, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	34
Mean	59.09
Std Dev	10.42





# B1L103S, U3-ch30, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51

Entry



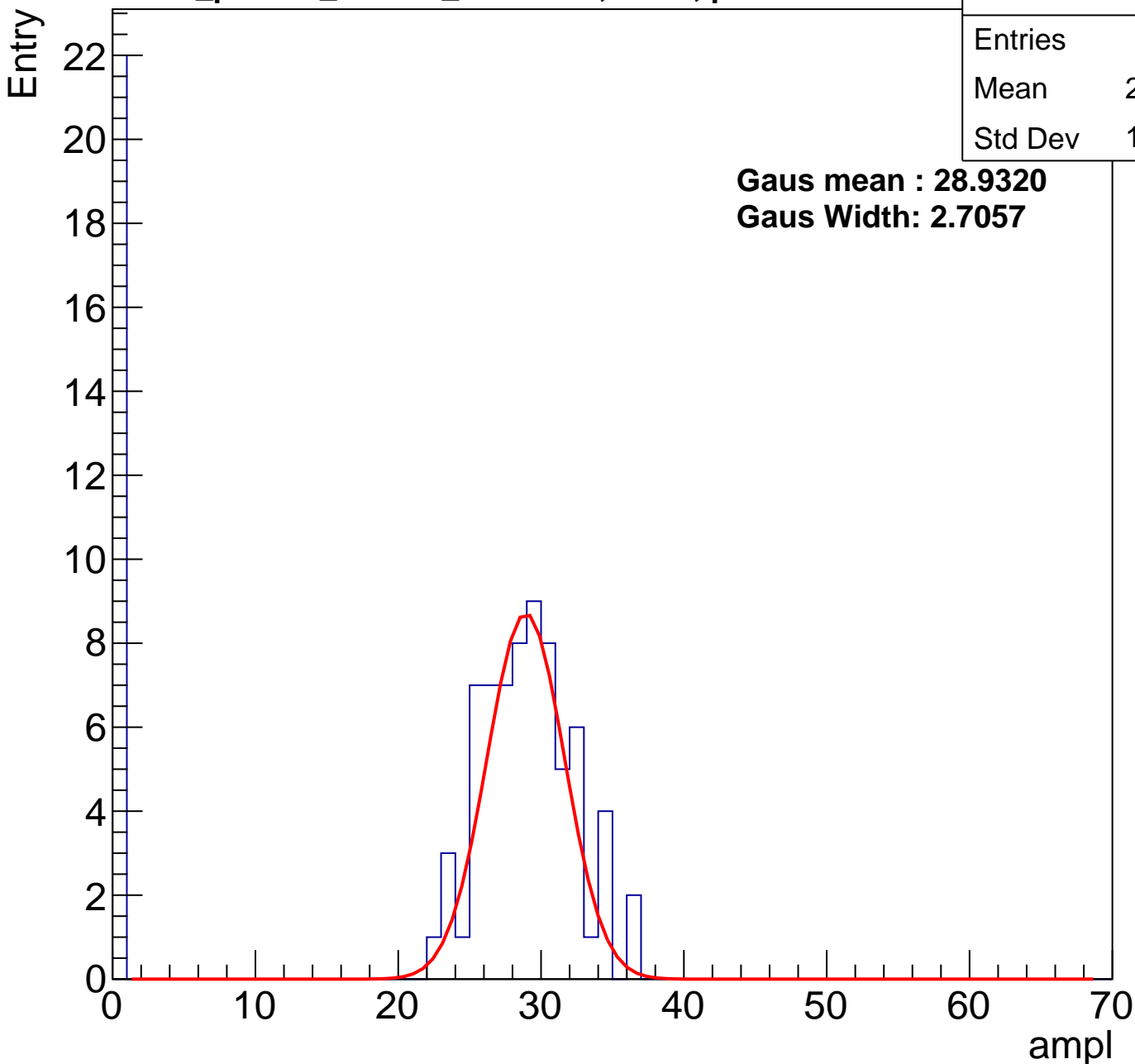
# B1L103S, U3-ch31, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	91
Mean	21.69
Std Dev	12.55

**Gaus mean : 28.9320**

**Gaus Width: 2.7057**



# B1L103S, U3-ch31, adc1

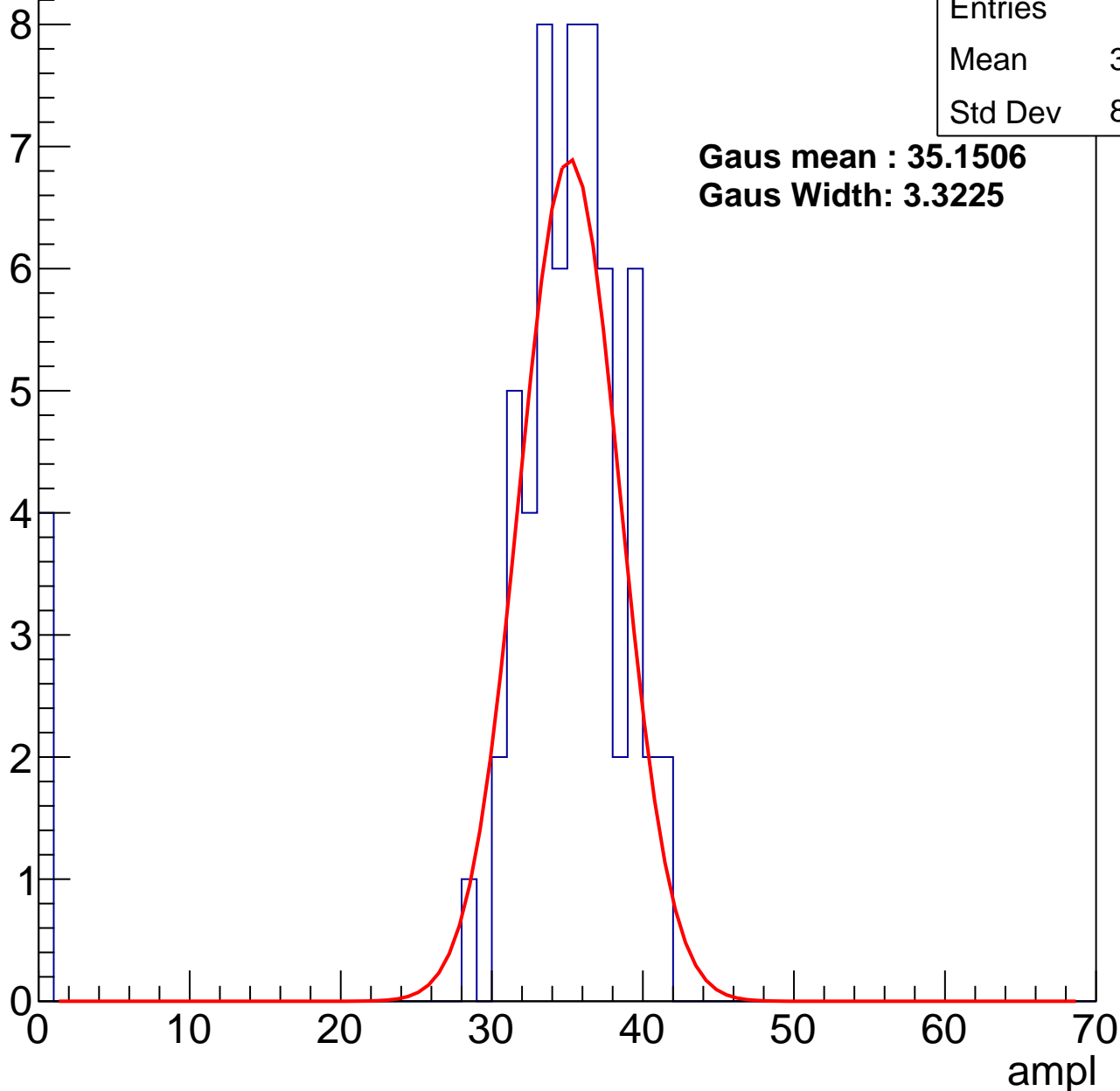
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	32.83
Std Dev	8.943

**Gaus mean : 35.1506**

**Gaus Width: 3.3225**



# B1L103S, U3-ch31, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	78
Mean	35.54
Std Dev	14.69

**Gaus mean : 41.6670**

**Gaus Width: 3.7475**

Entry

10

8

6

4

2

0

0

10

20

30

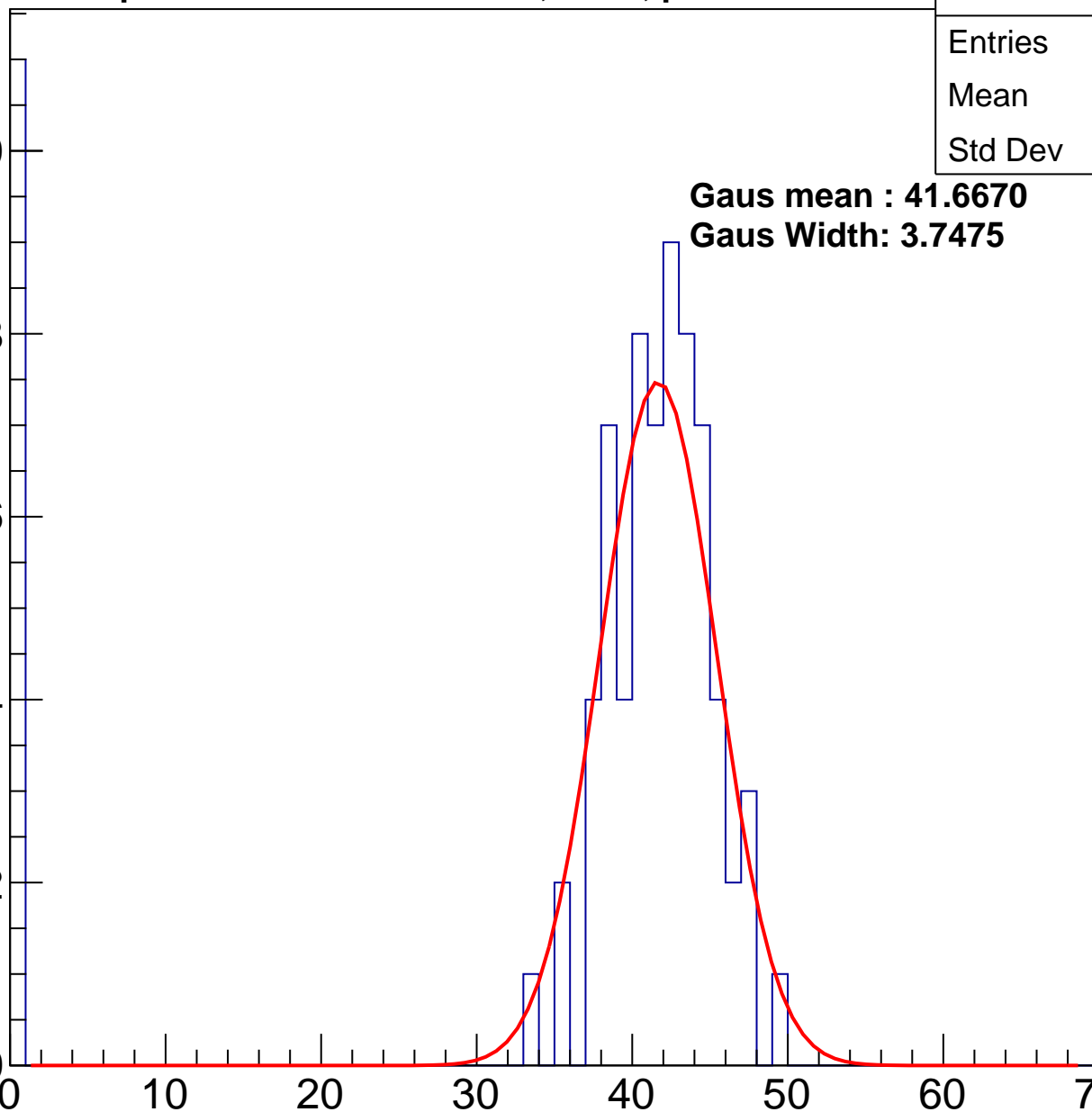
40

50

60

70

ampl

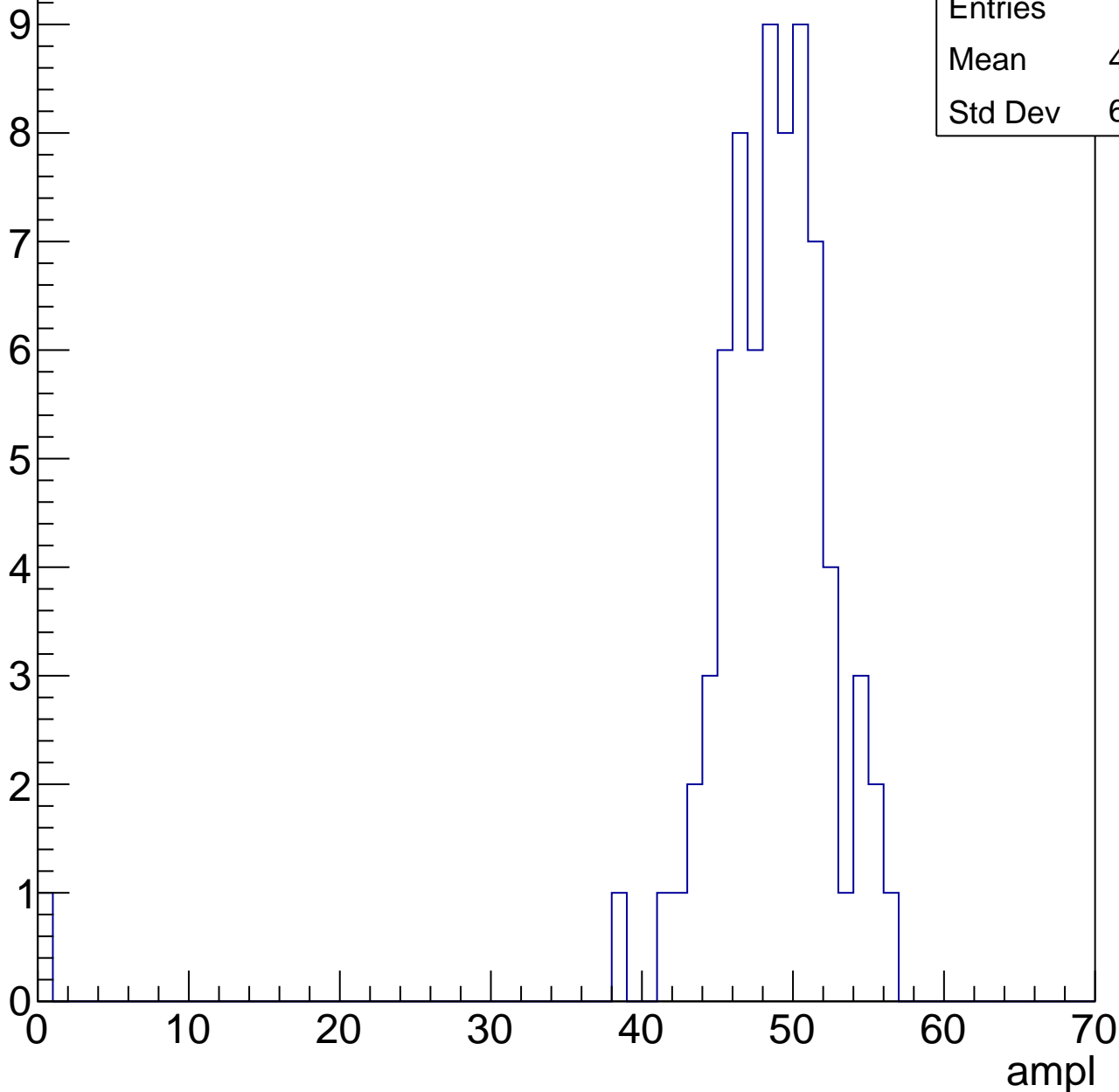


# B1L103S, U3-ch31, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

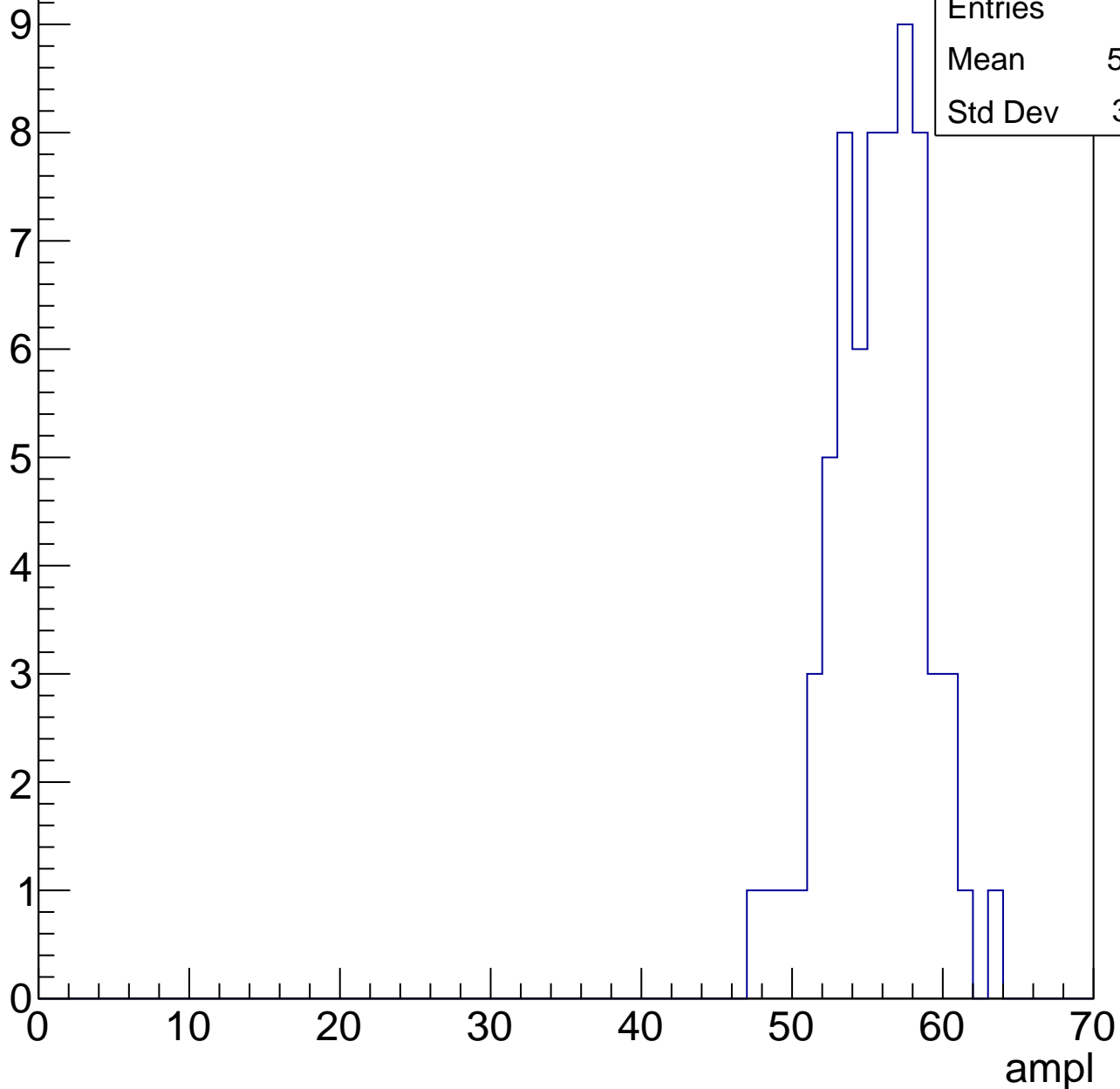
Entries	73
Mean	47.66
Std Dev	6.555



# B1L103S, U3-ch31, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

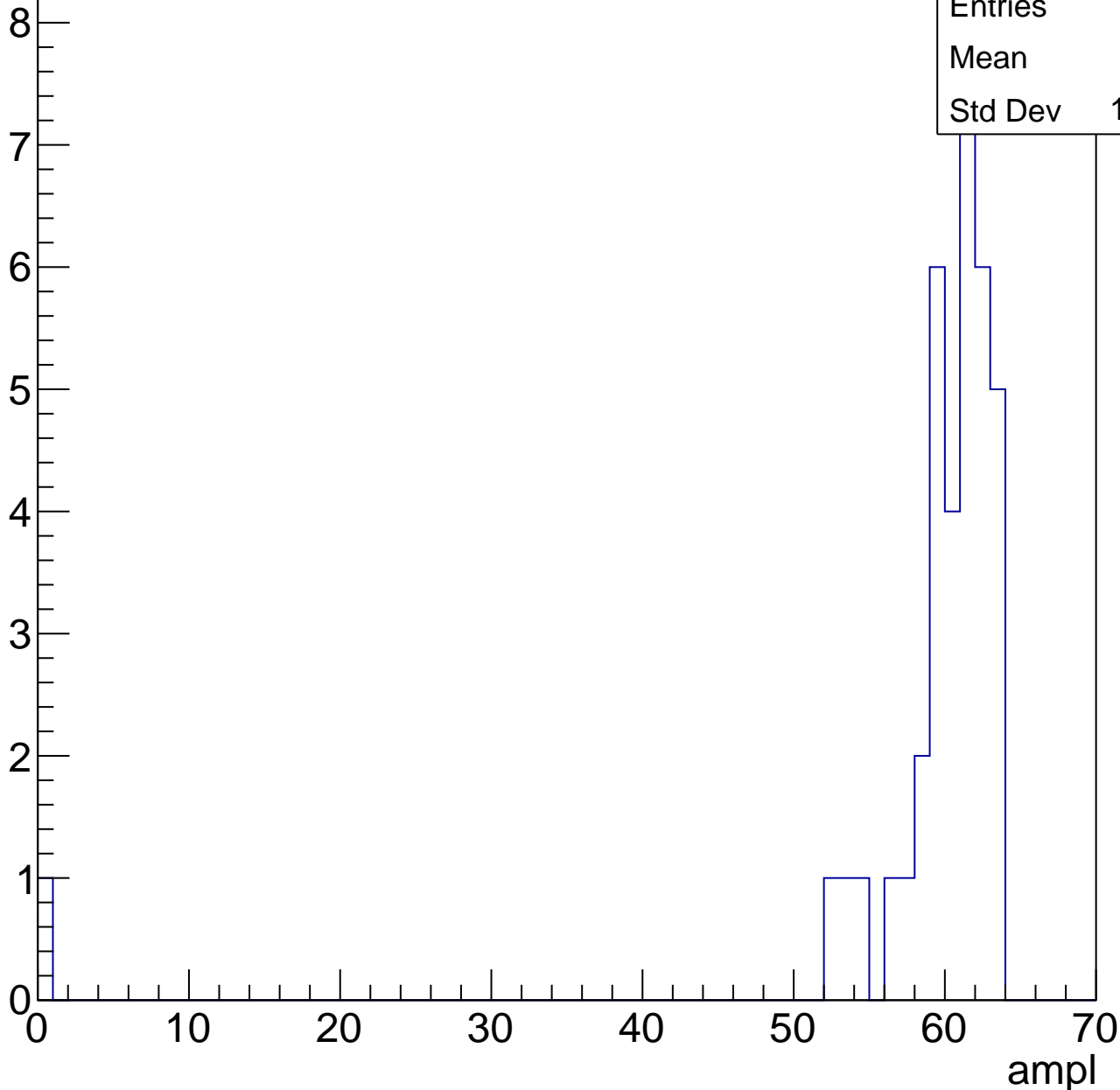


# B1L103S, U3-ch31, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

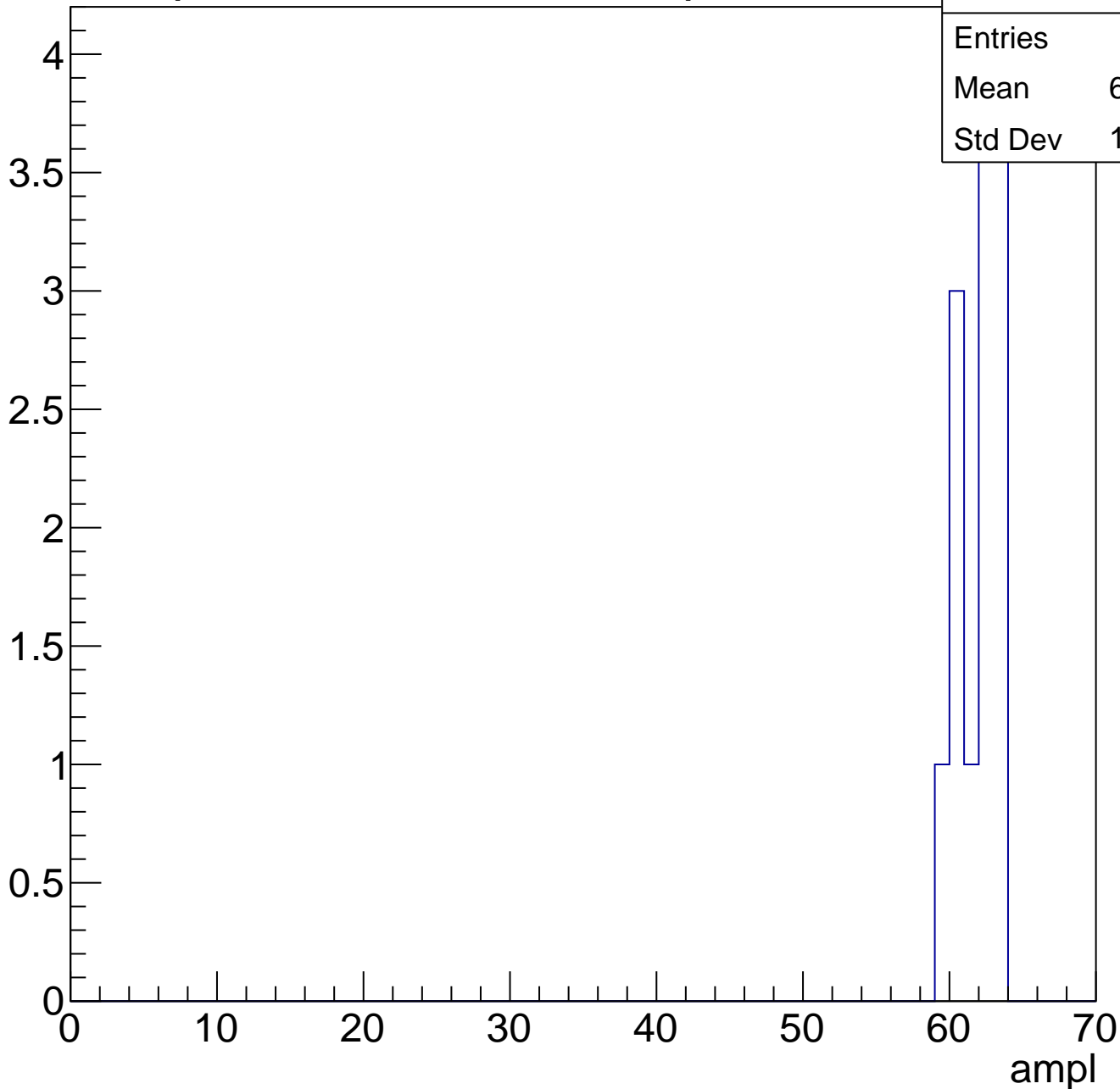
Entries	37
Mean	58.3
Std Dev	10.08



# B1L103S, U3-ch31, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U3-ch31, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	19
Mean	0
Std Dev	0

# B1L103S, U3-ch32, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	109
Mean	19.28
Std Dev	12.37

**Gaus mean : 26.6892**

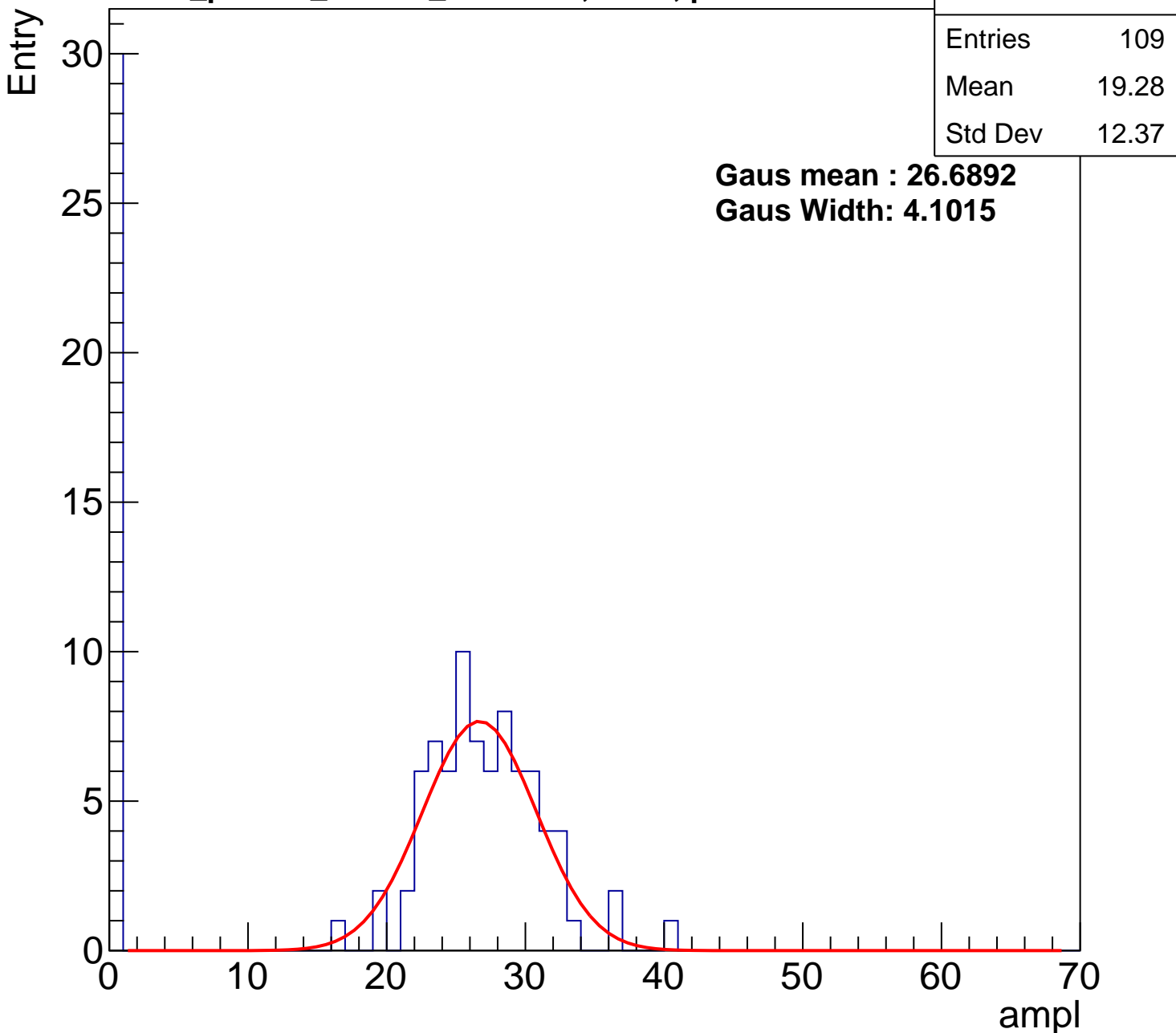
**Gaus Width: 4.1015**

Entry

30  
25  
20  
15  
10  
5  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch32, adc1

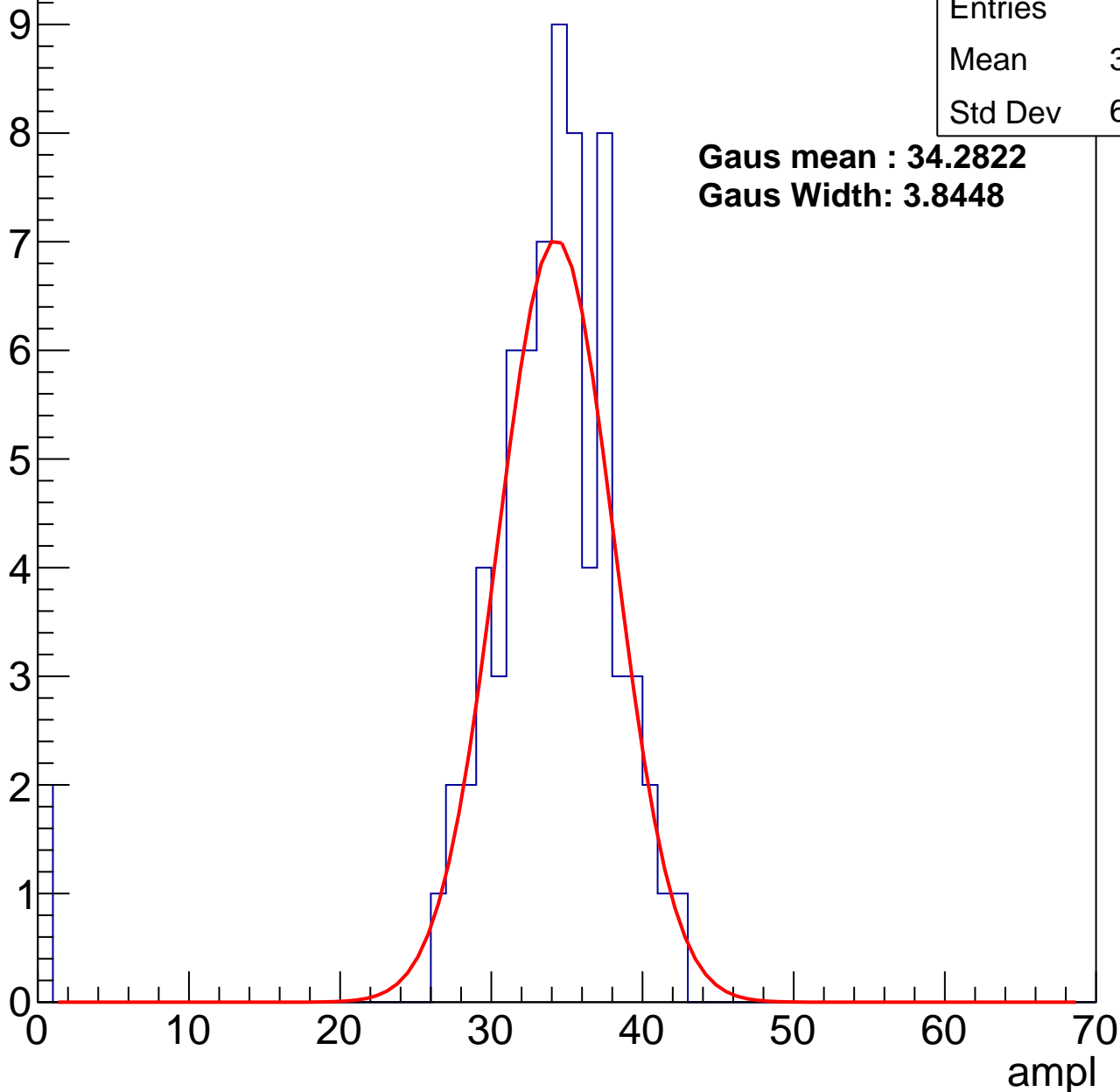
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	72
Mean	32.93
Std Dev	6.562

**Gaus mean : 34.2822**

**Gaus Width: 3.8448**



# B1L103S, U3-ch32, adc2

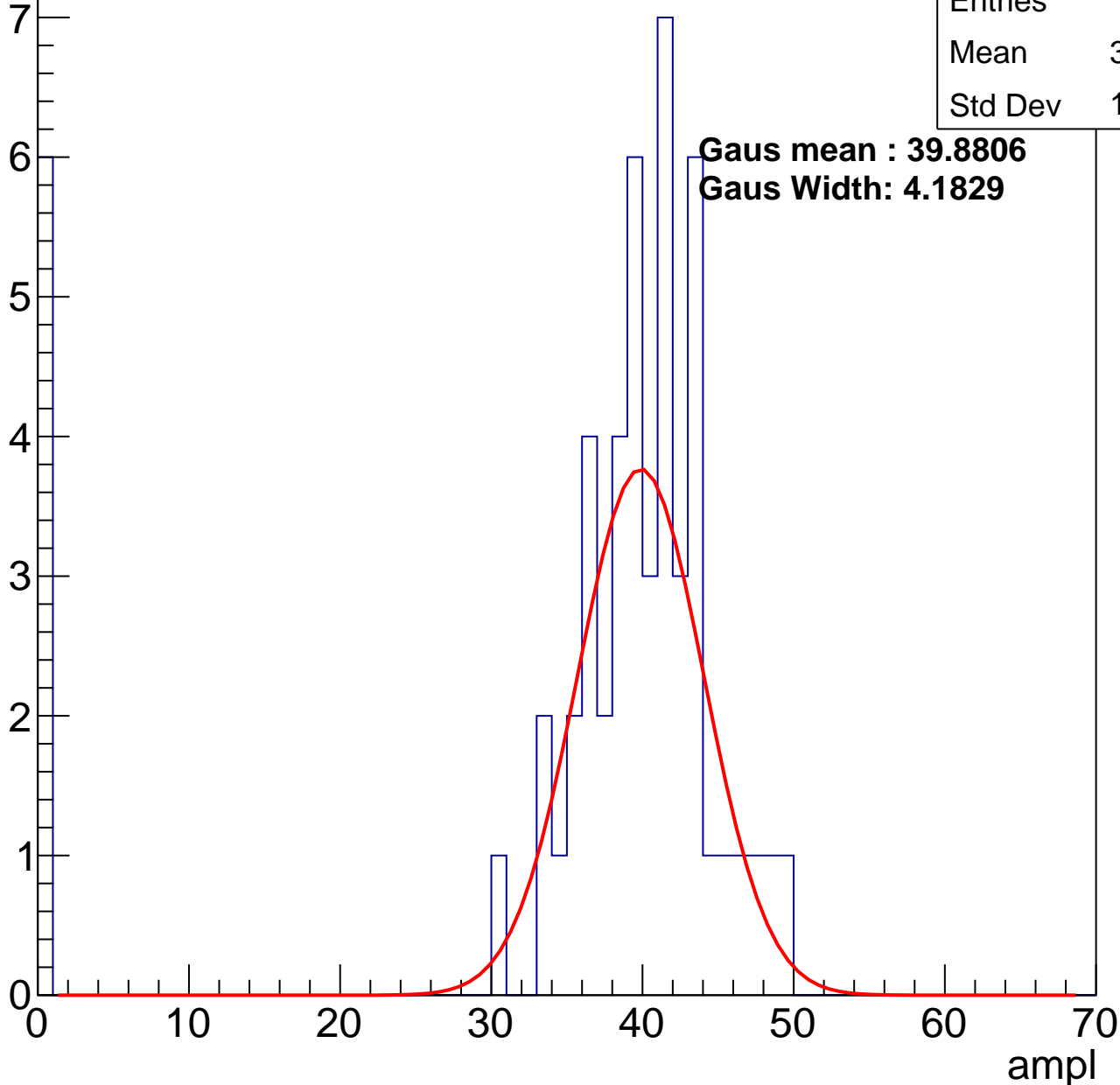
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	53
Mean	35.36
Std Dev	13.17

**Gaus mean : 39.8806**

**Gaus Width: 4.1829**



# B1L103S, U3-ch32, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

10

8

6

4

2

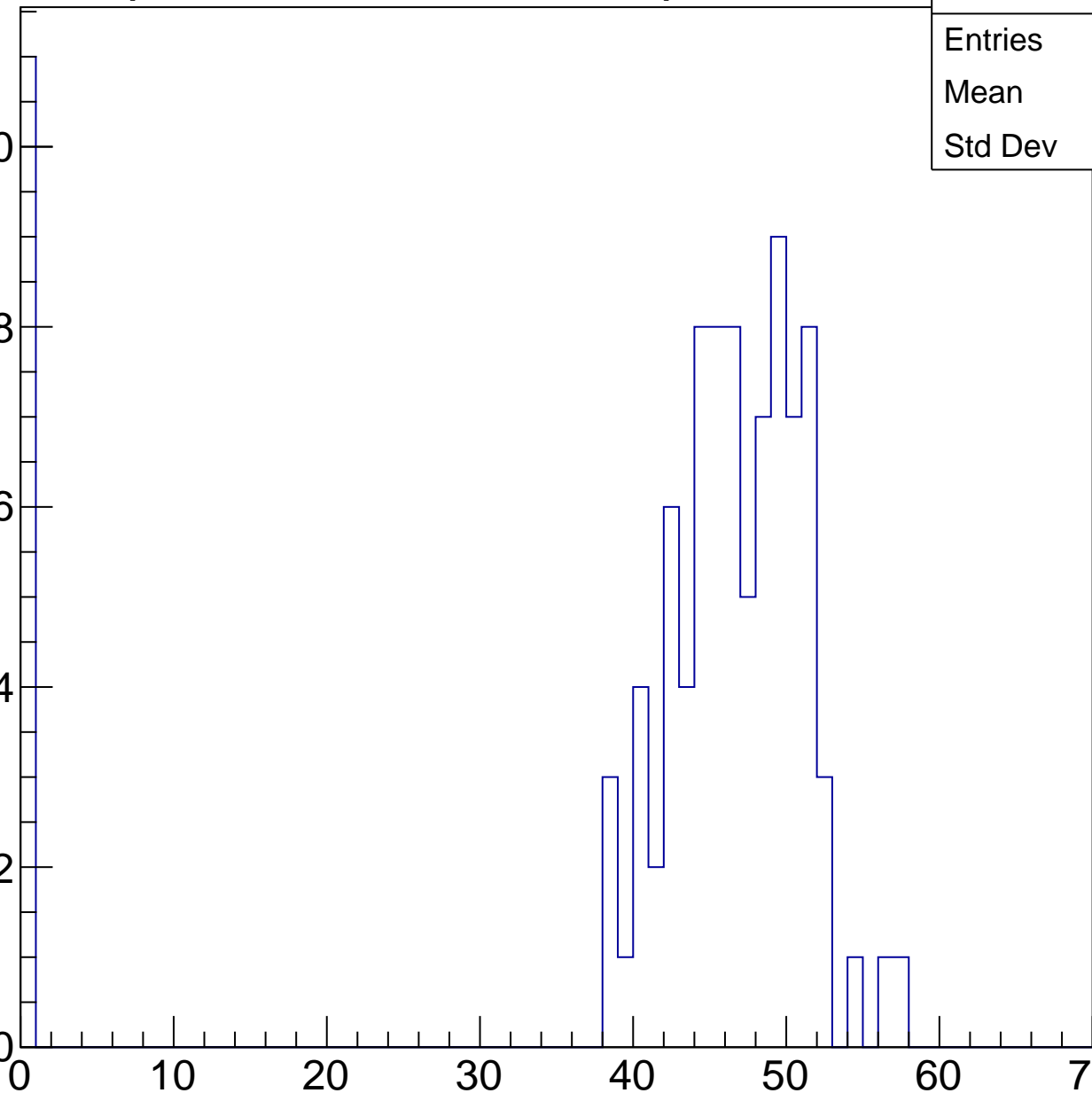
0

Entries 97

Mean 41.15

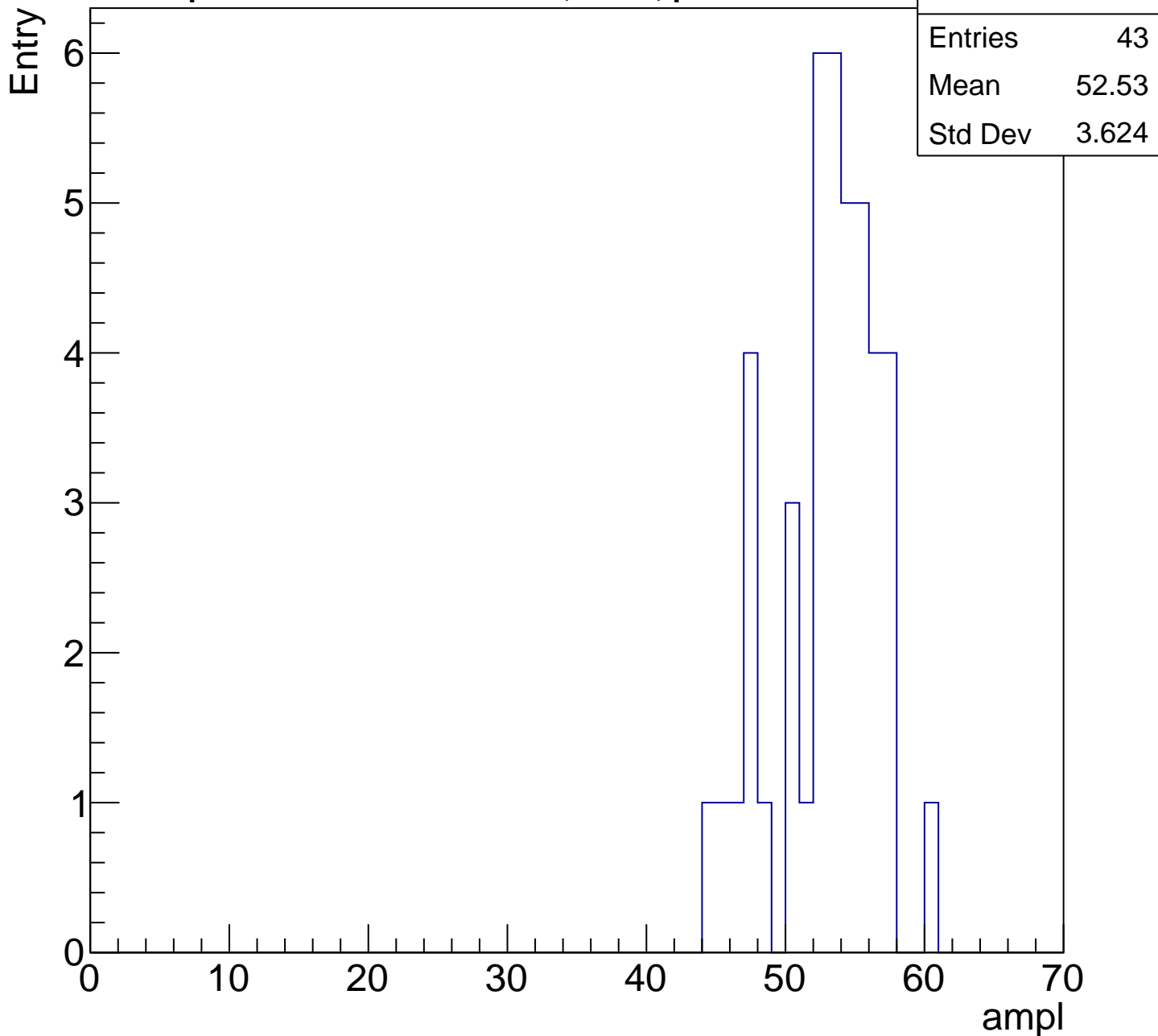
Std Dev 15.2

ampl



# B1L103S, U3-ch32, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

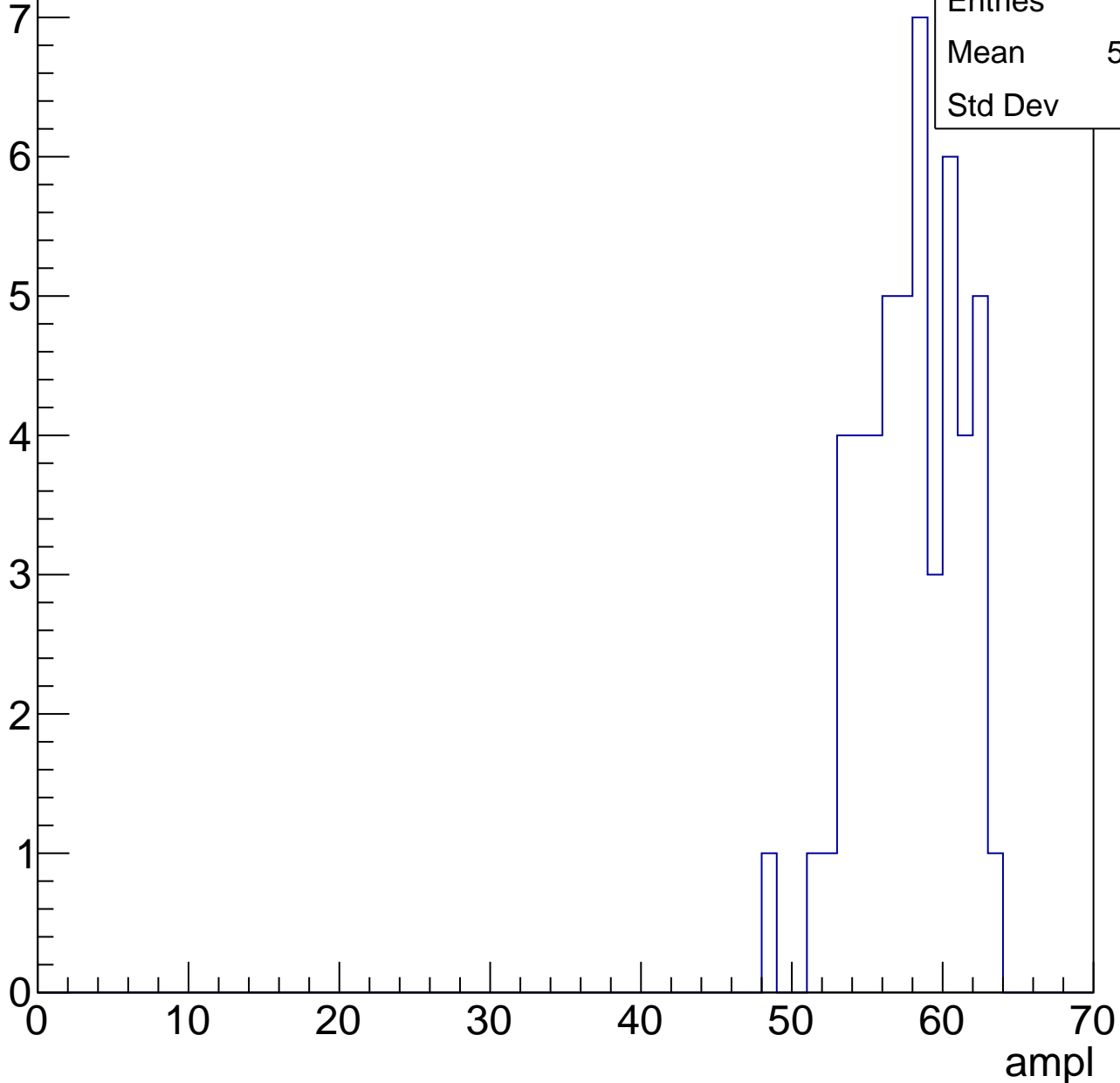


# B1L103S, U3-ch32, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

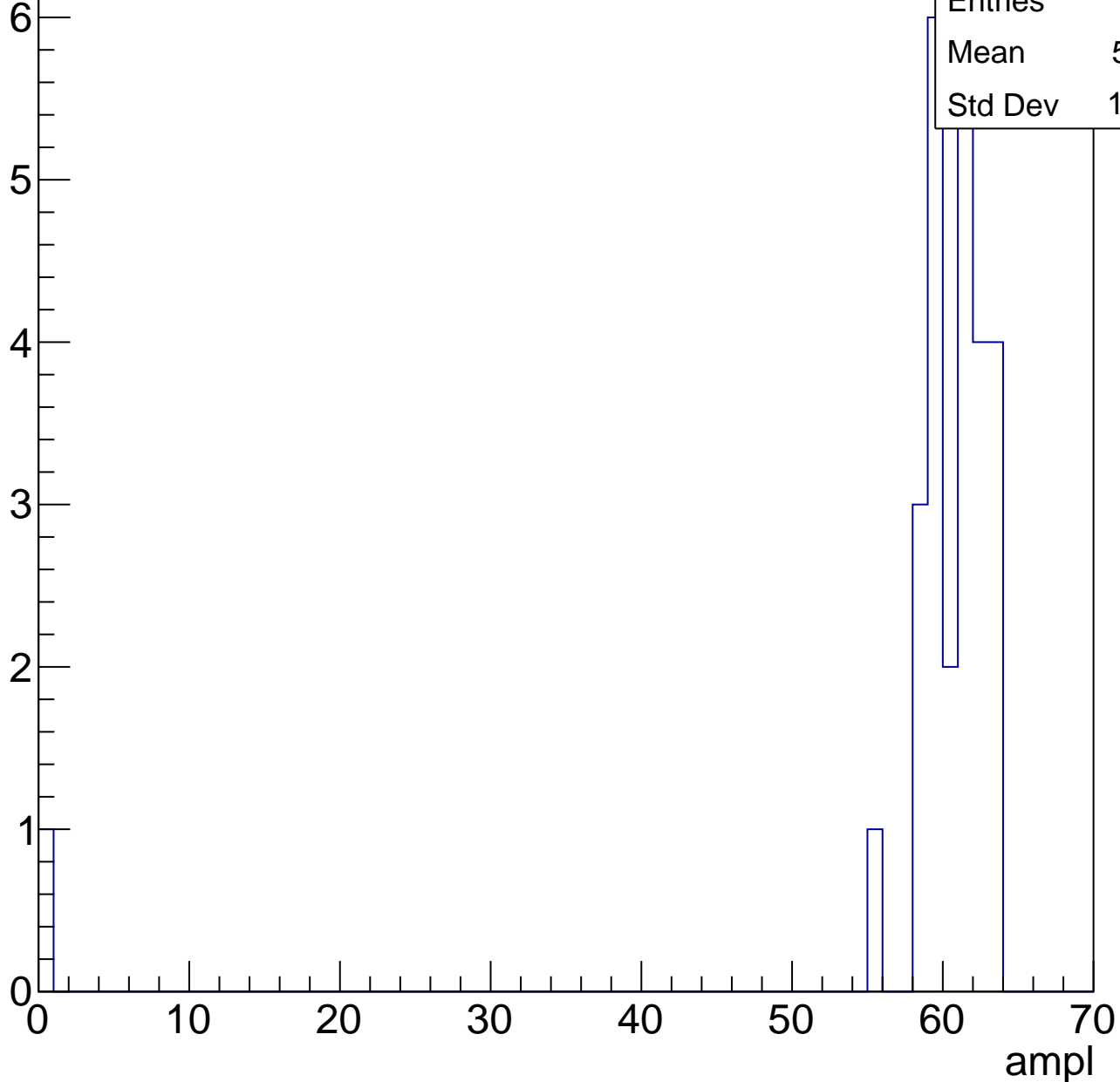
Entries	51
Mean	57.33
Std Dev	3.3



# B1L103S, U3-ch32, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

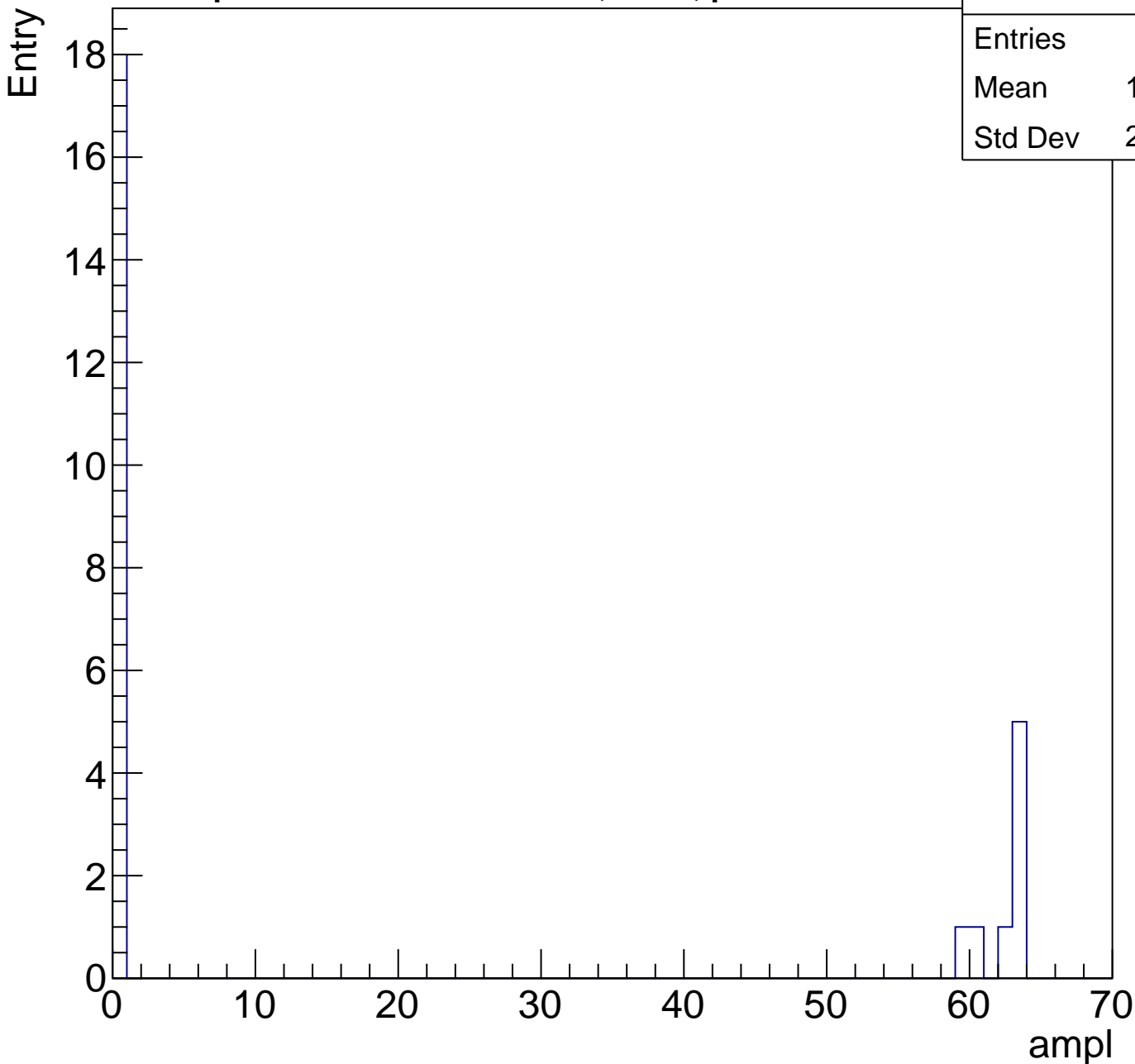




# B1L103S, U3-ch32, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	26
Mean	19.08
Std Dev	28.63



# B1L103S, U3-ch33, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	110
Mean	23.19
Std Dev	13.29

**Gaus mean : 31.2123**

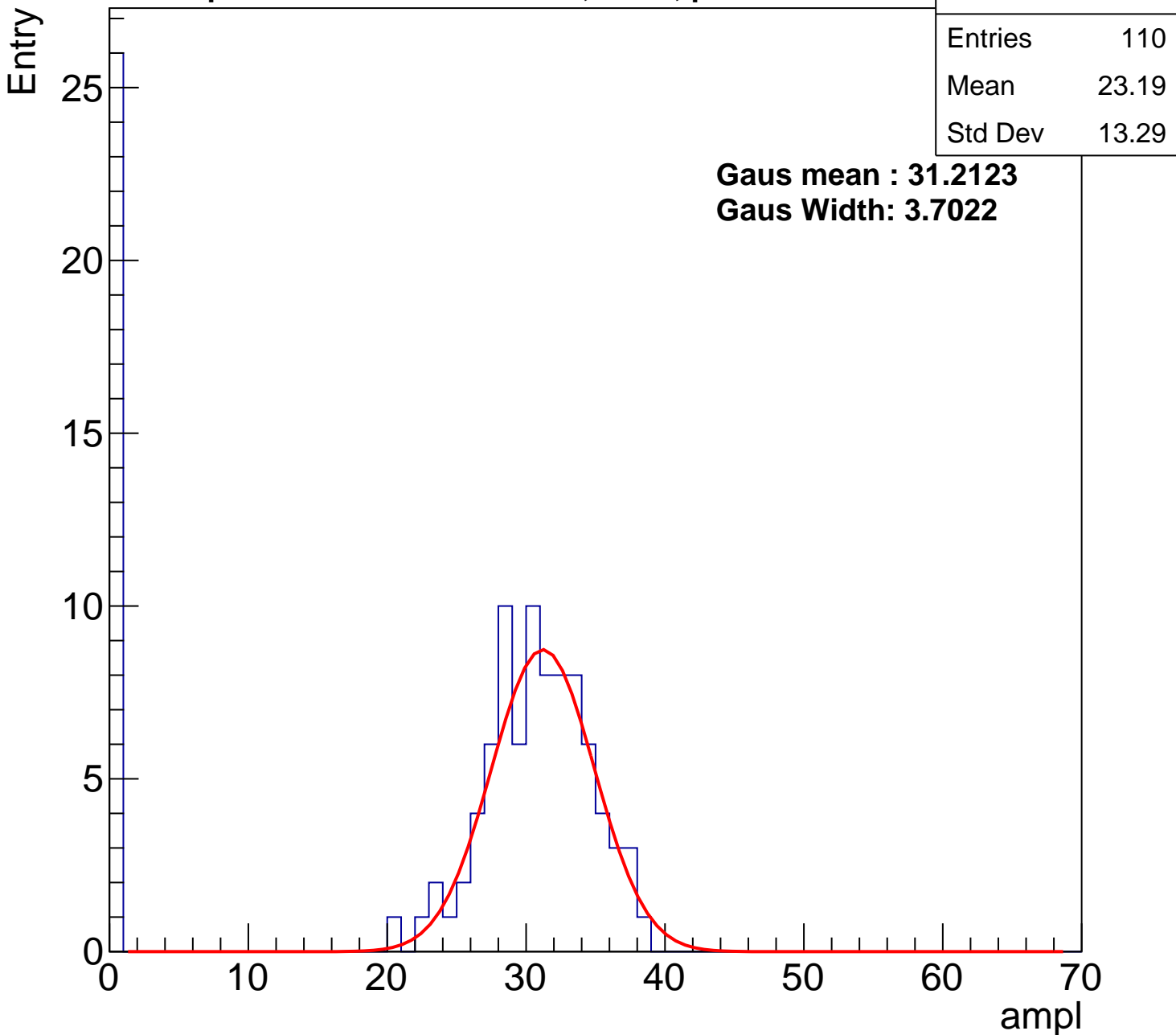
**Gaus Width: 3.7022**

Entry

25  
20  
15  
10  
5  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U3-ch33, adc1

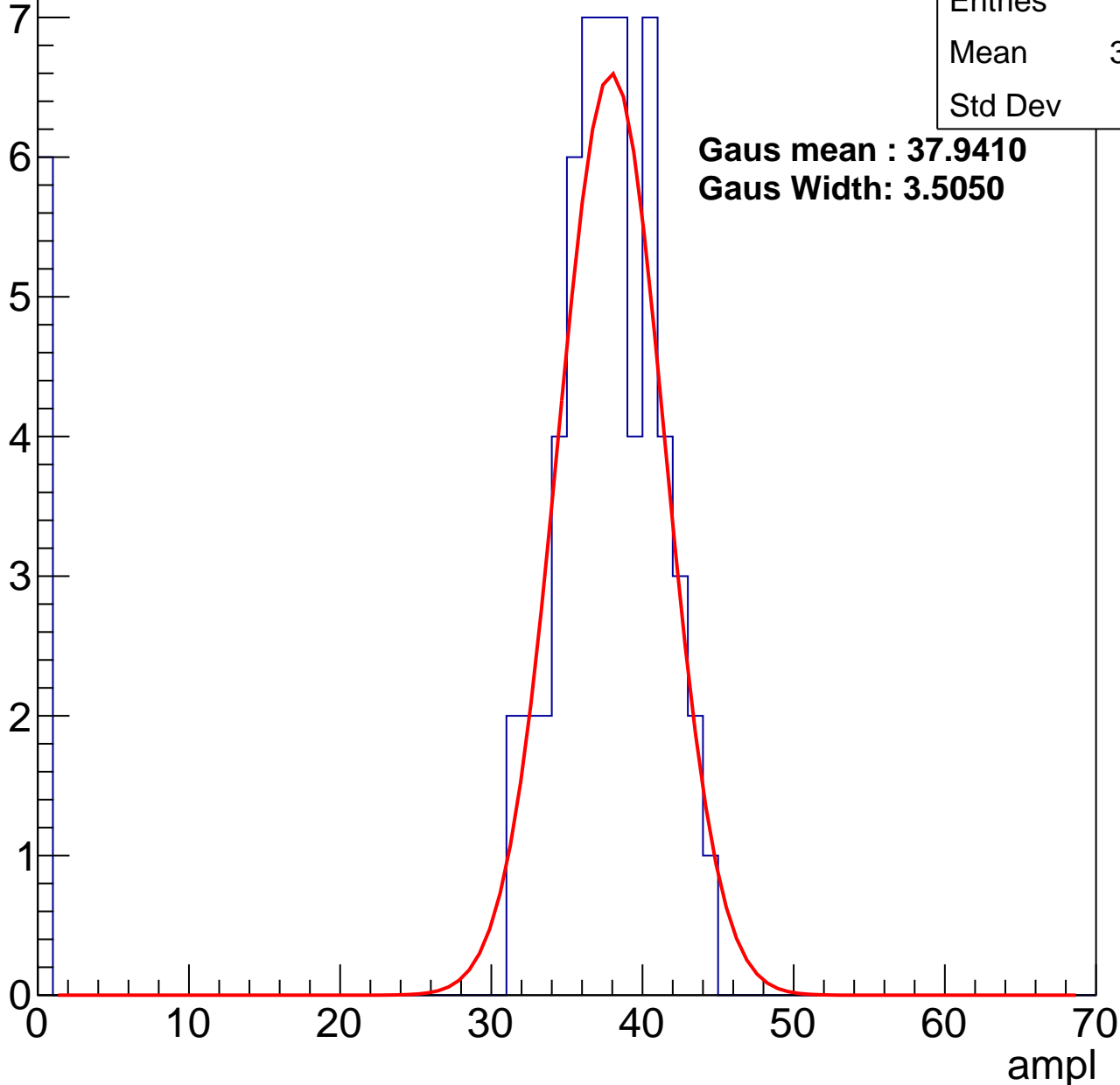
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	33.92
Std Dev	11.3

**Gaus mean : 37.9410**

**Gaus Width: 3.5050**



# B1L103S, U3-ch33, adc2

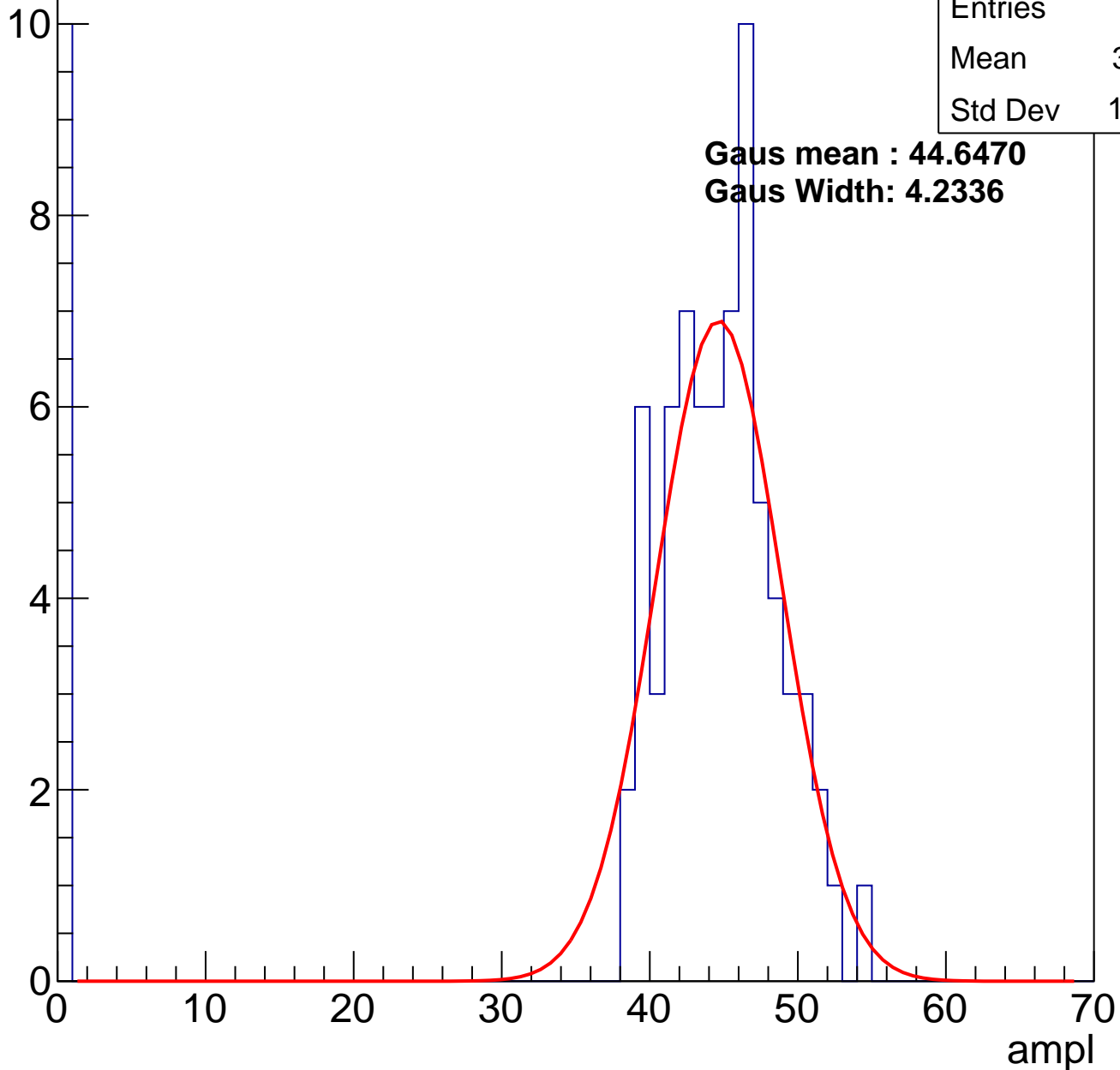
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	82
Mean	39.01
Std Dev	14.93

**Gaus mean : 44.6470**

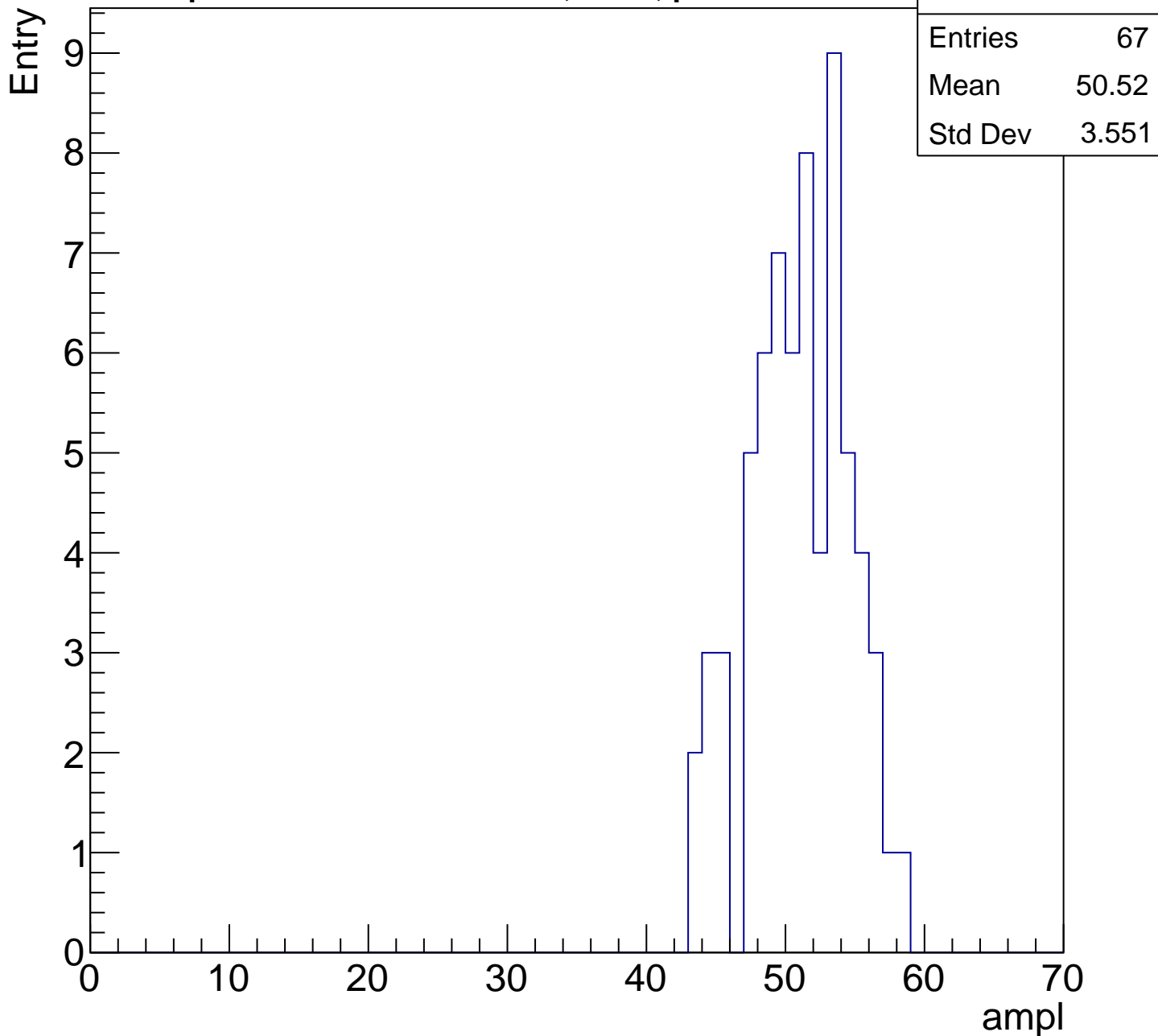
**Gaus Width: 4.2336**

Entry



# B1L103S, U3-ch33, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

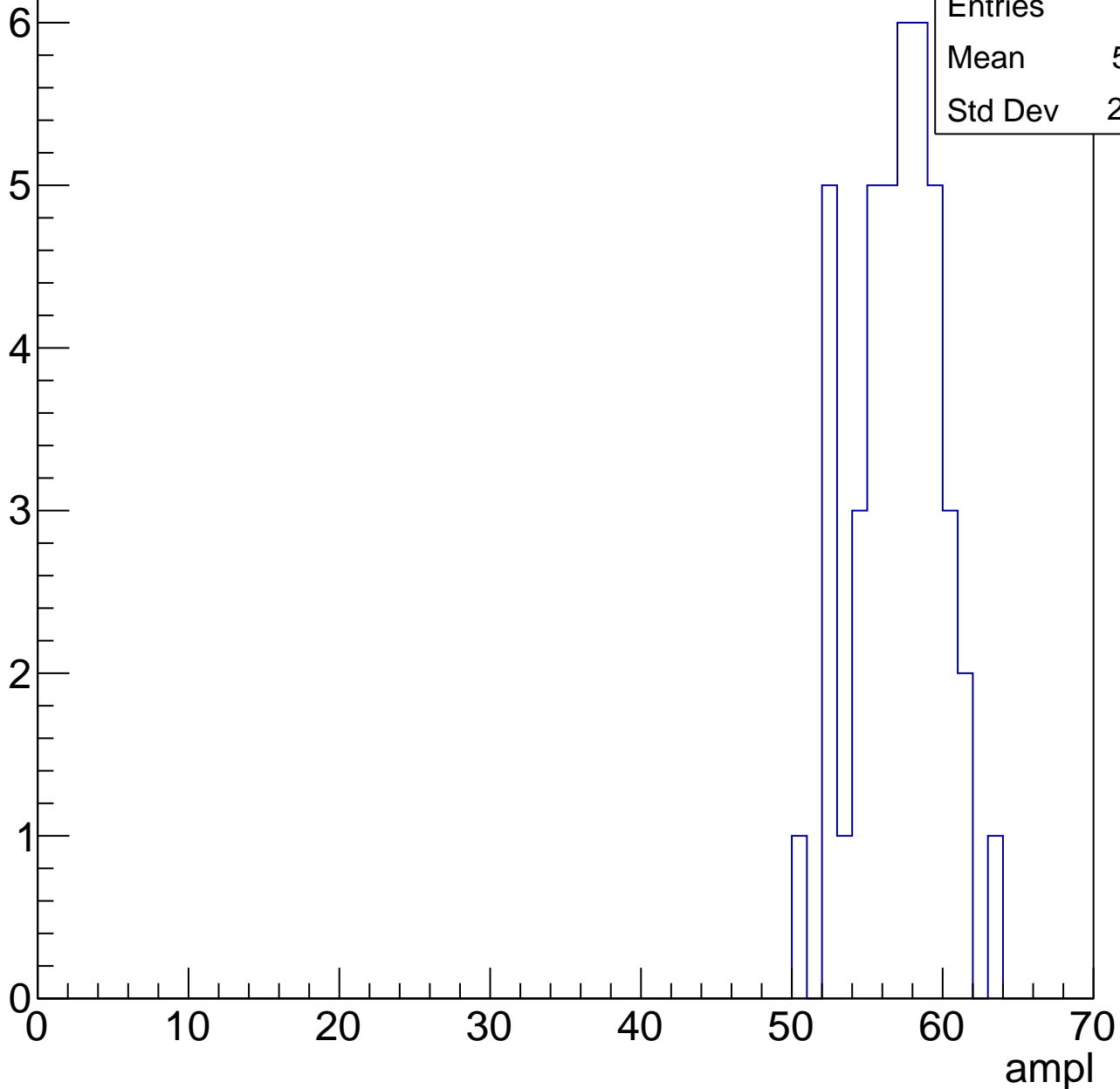


# B1L103S, U3-ch33, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	43
Mean	56.51
Std Dev	2.864

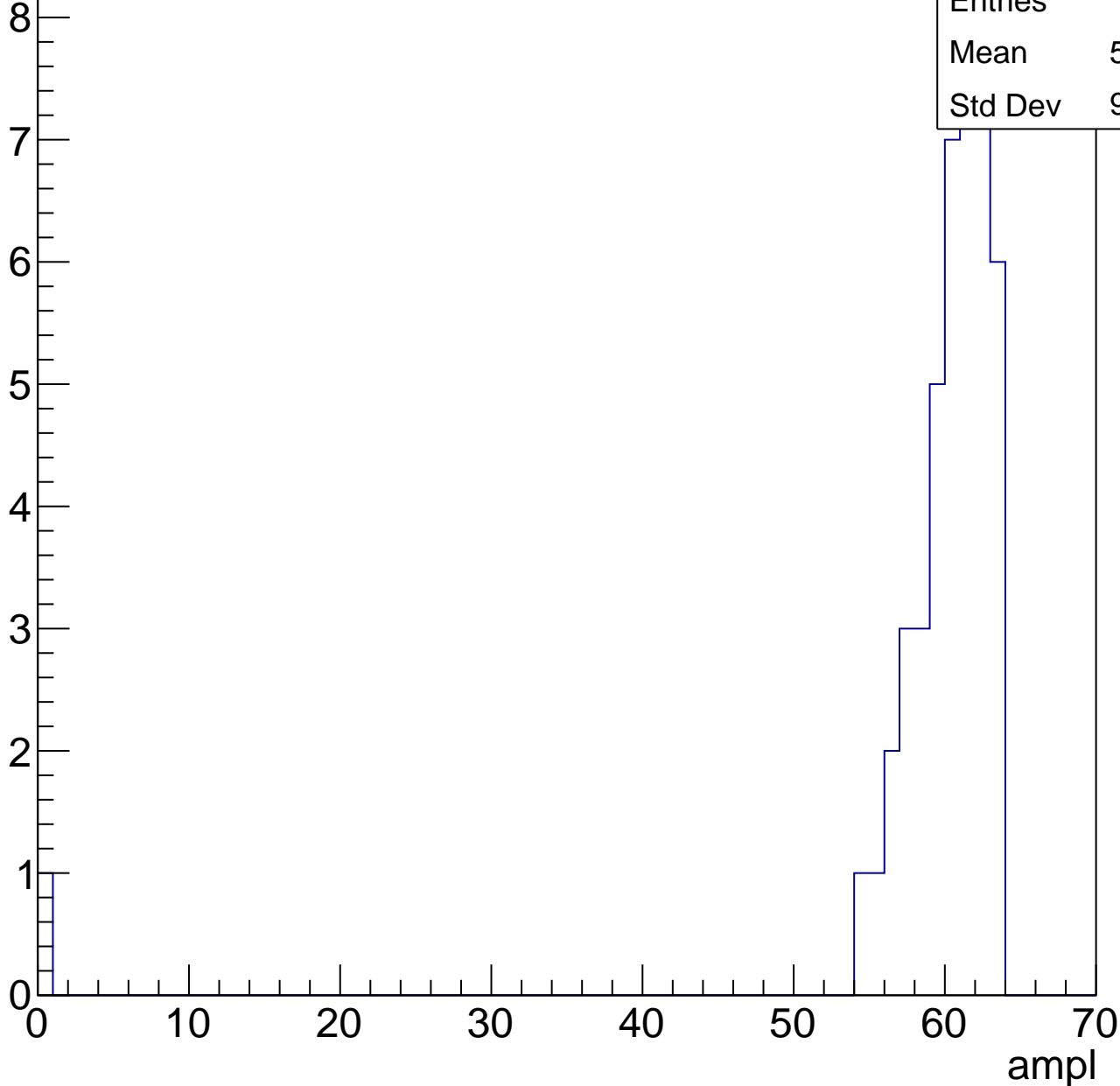


# B1L103S, U3-ch33, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

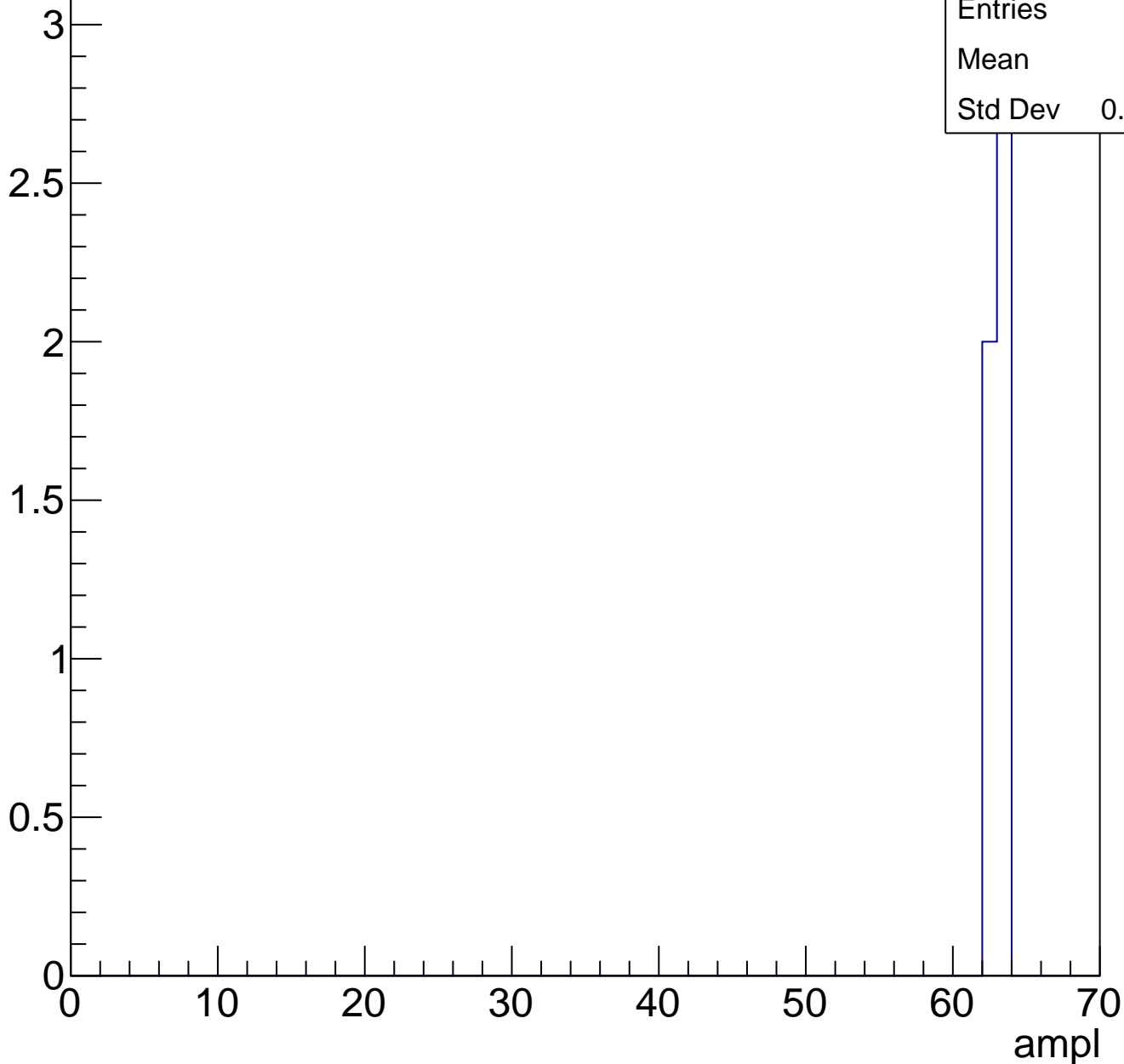
Entries	45
Mean	58.73
Std Dev	9.139



# B1L103S, U3-ch33, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U3-ch33, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	19
Mean	0
Std Dev	0

ampl

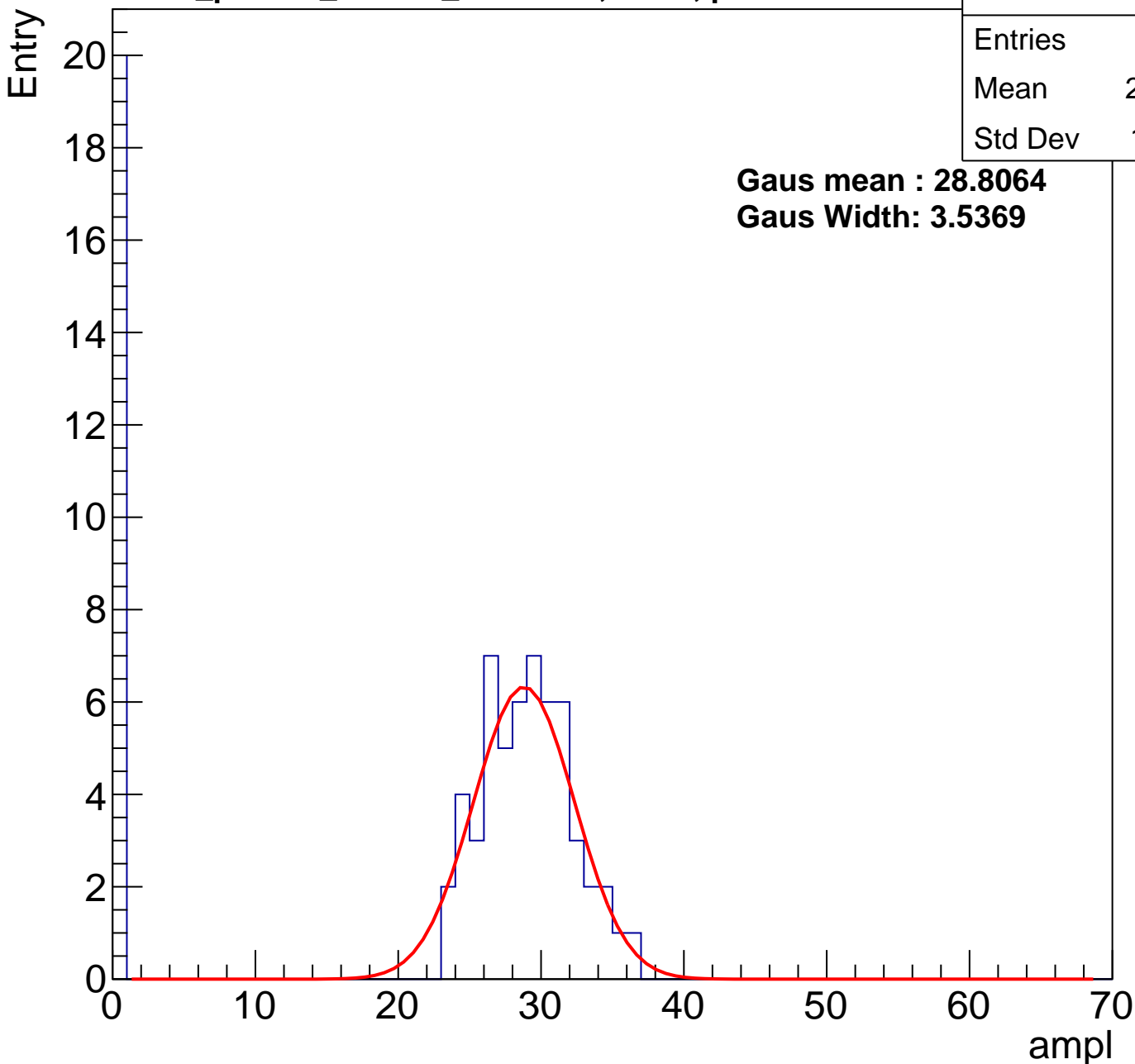
# B1L103S, U3-ch34, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	75
Mean	20.96
Std Dev	12.91

**Gaus mean : 28.8064**

**Gaus Width: 3.5369**



# B1L103S, U3-ch34, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	74
Mean	27.07
Std Dev	14.03

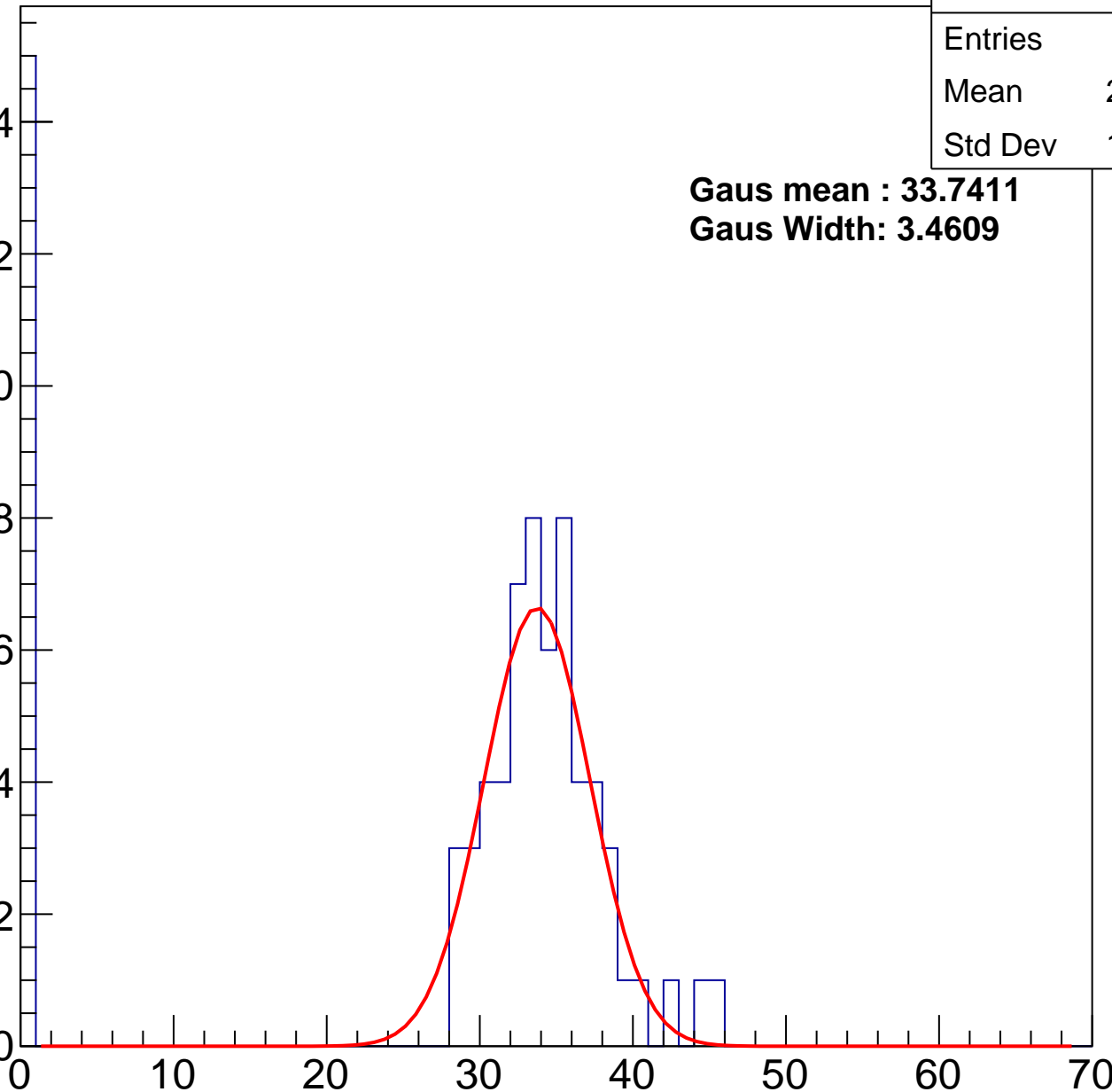
**Gaus mean : 33.7411**

**Gaus Width: 3.4609**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U3-ch34, adc2

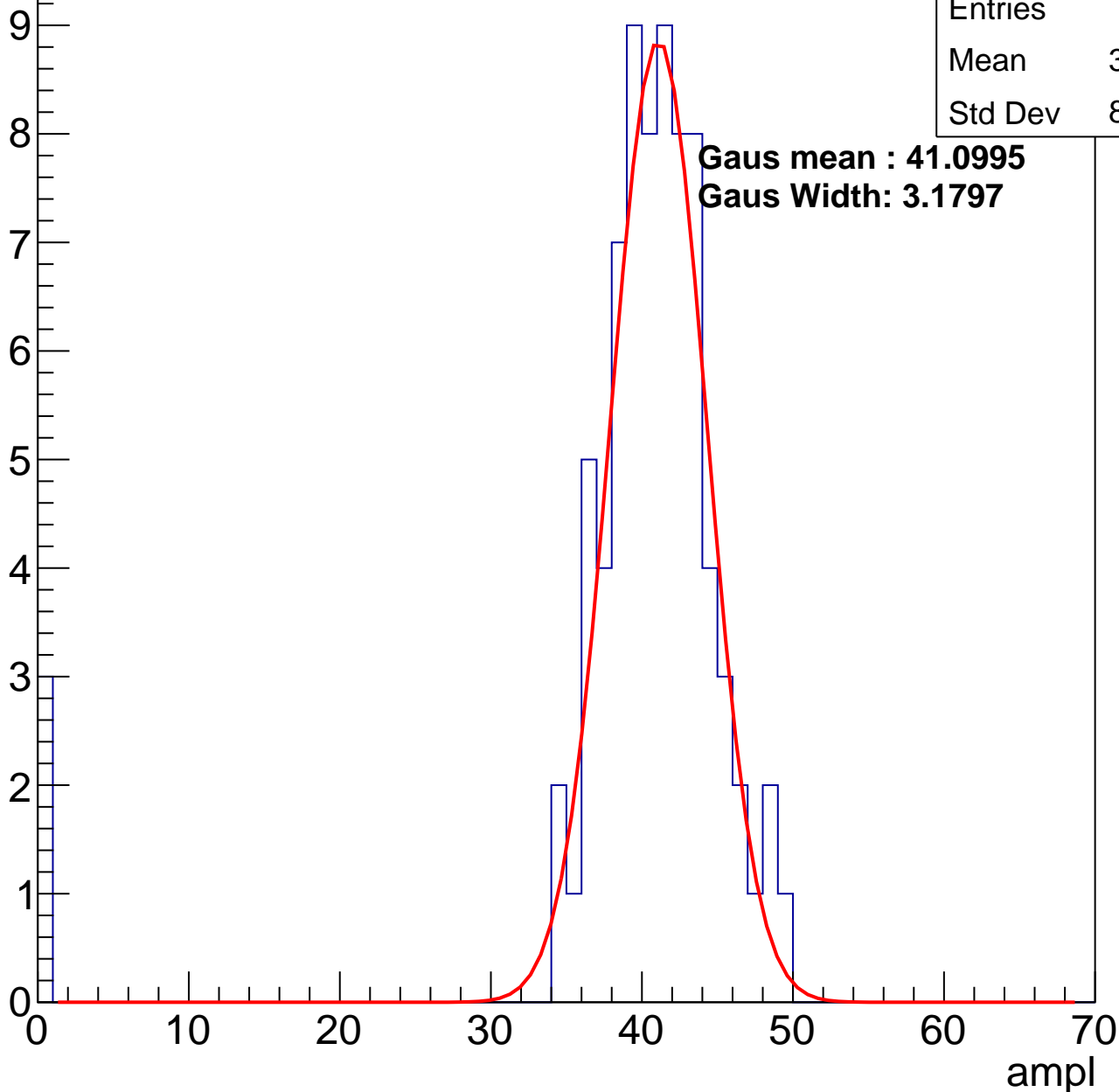
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	77
Mean	39.12
Std Dev	8.507

**Gaus mean : 41.0995**

**Gaus Width: 3.1797**

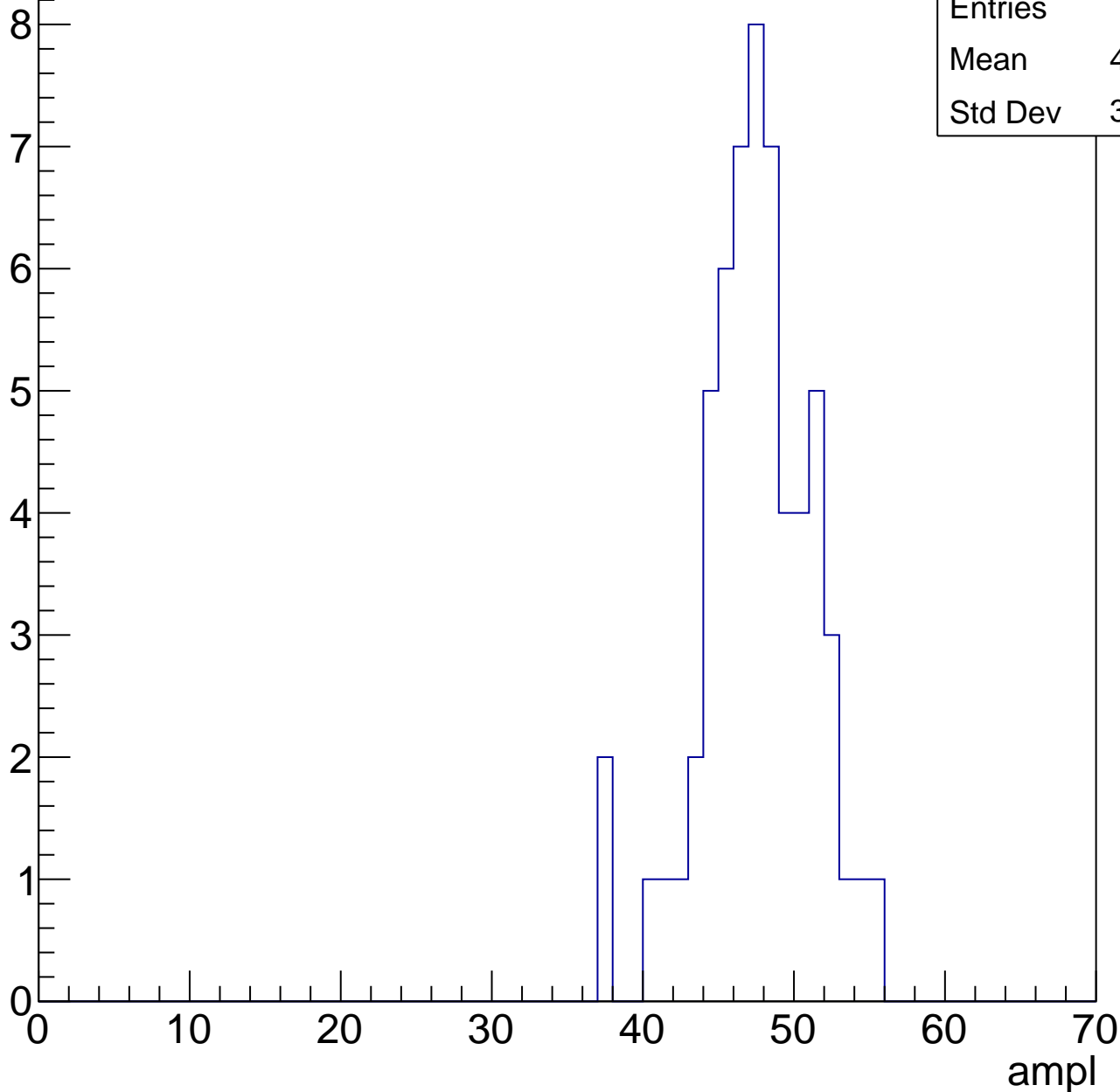


# B1L103S, U3-ch34, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

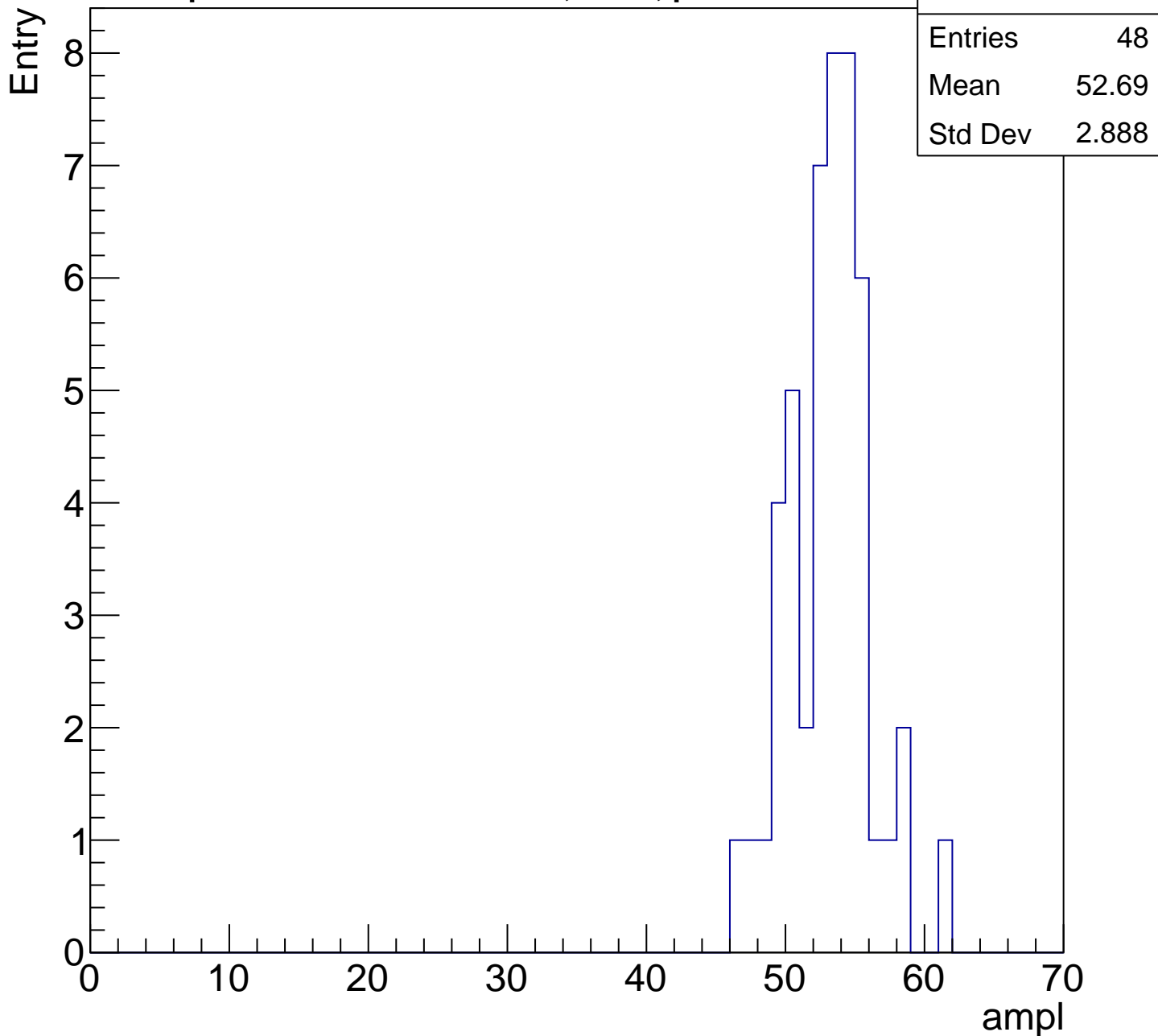
Entry

Entries	59
Mean	47.05
Std Dev	3.638



# B1L103S, U3-ch34, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

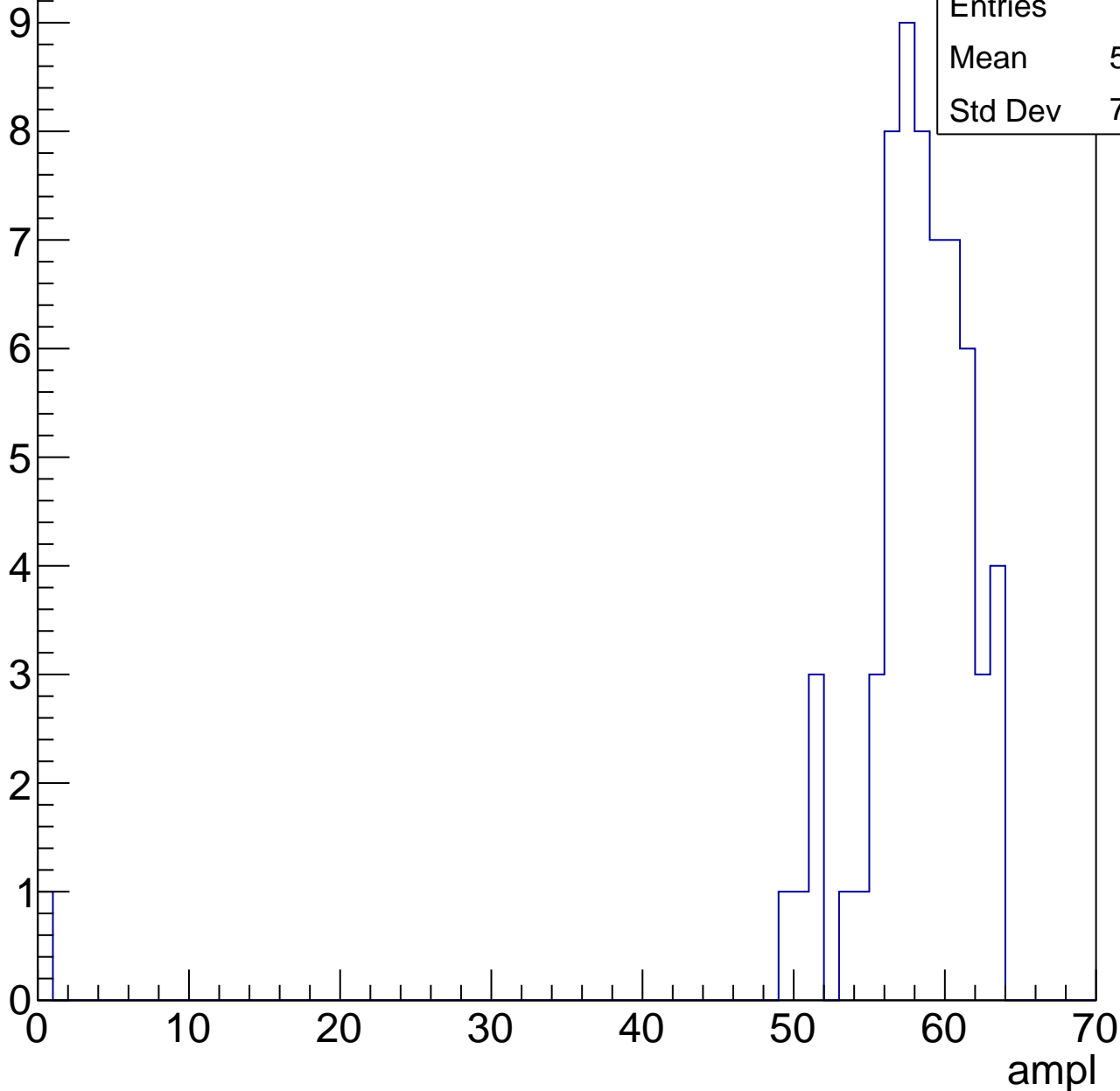


# B1L103S, U3-ch34, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	56.92
Std Dev	7.897

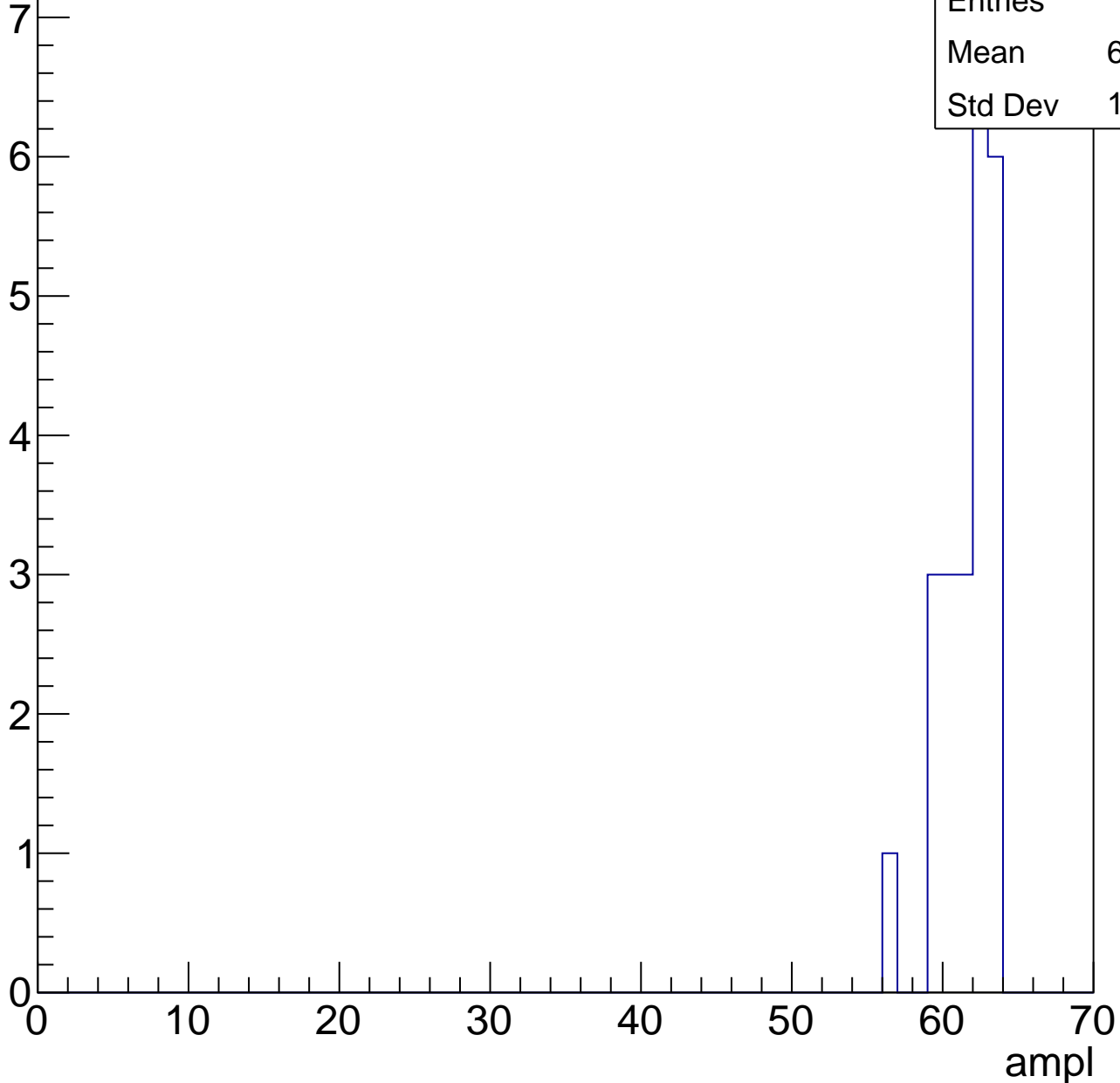


# B1L103S, U3-ch34, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	23
Mean	61.22
Std Dev	1.743





# B1L103S, U3-ch34, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	18
Mean	0
Std Dev	0

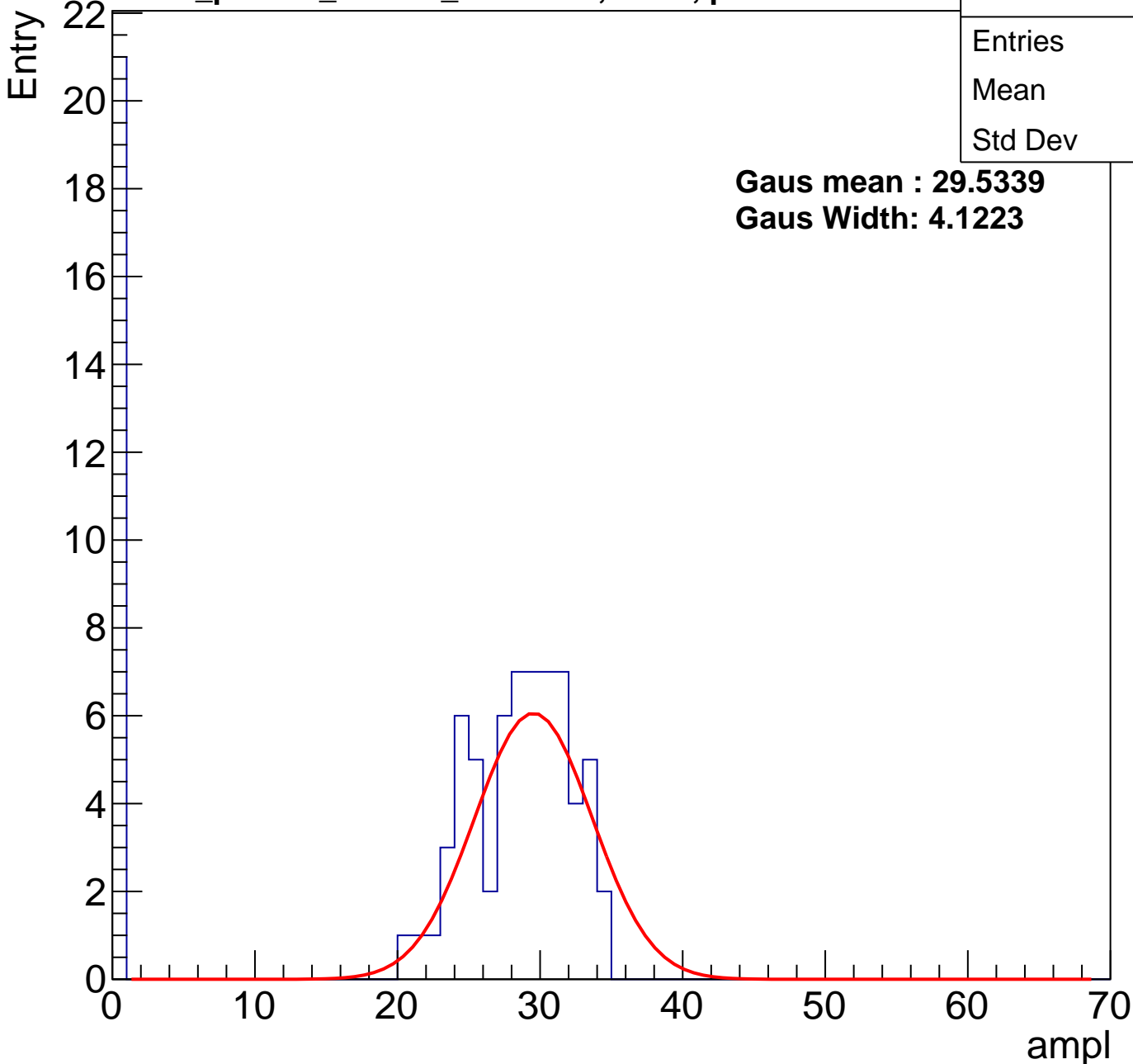
# B1L103S, U3-ch35, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	85
Mean	21.2
Std Dev	12.5

**Gaus mean : 29.5339**

**Gaus Width: 4.1223**



# B1L103S, U3-ch35, adc1

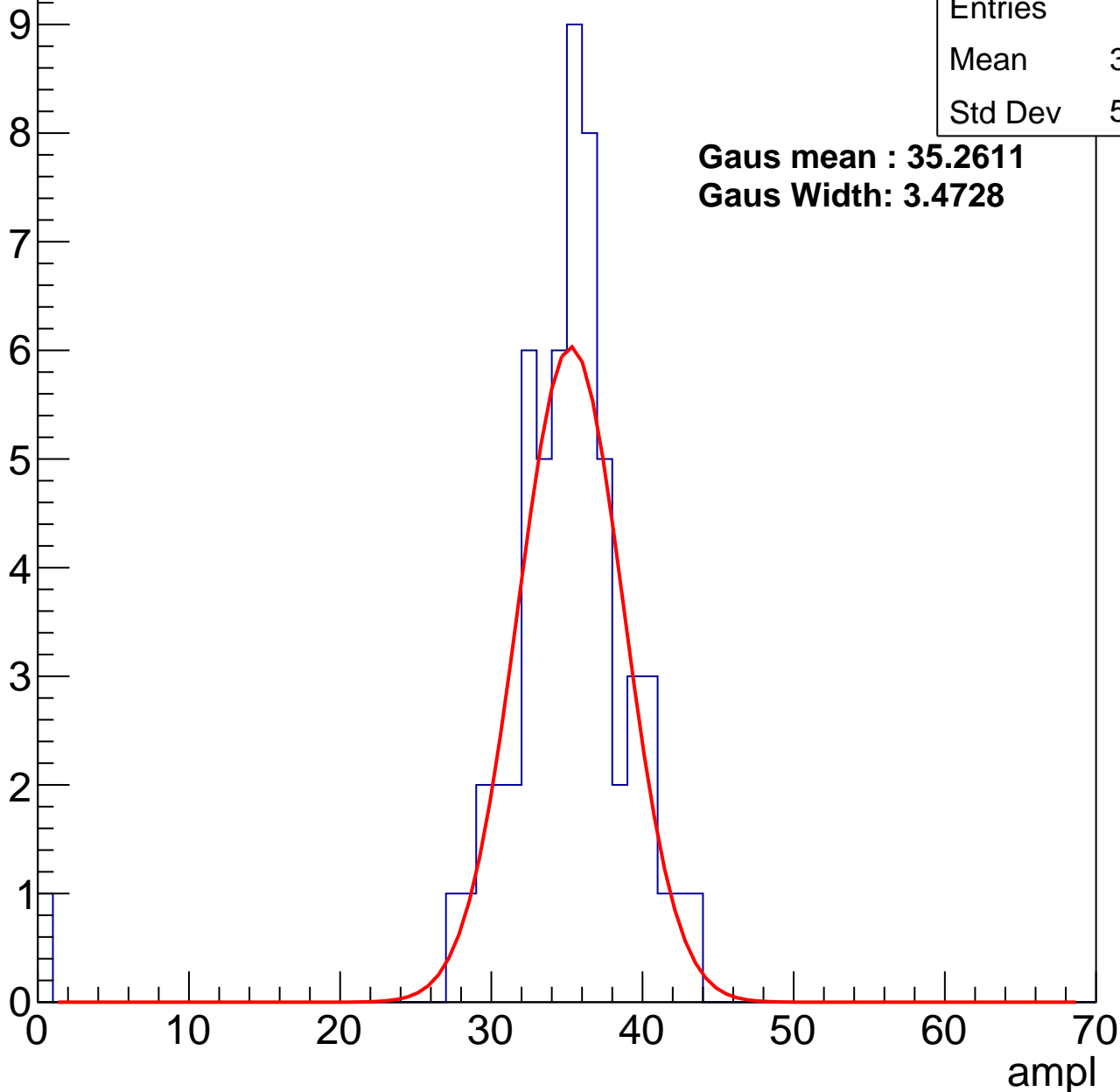
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	34.29
Std Dev	5.615

**Gaus mean : 35.2611**

**Gaus Width: 3.4728**



# B1L103S, U3-ch35, adc2

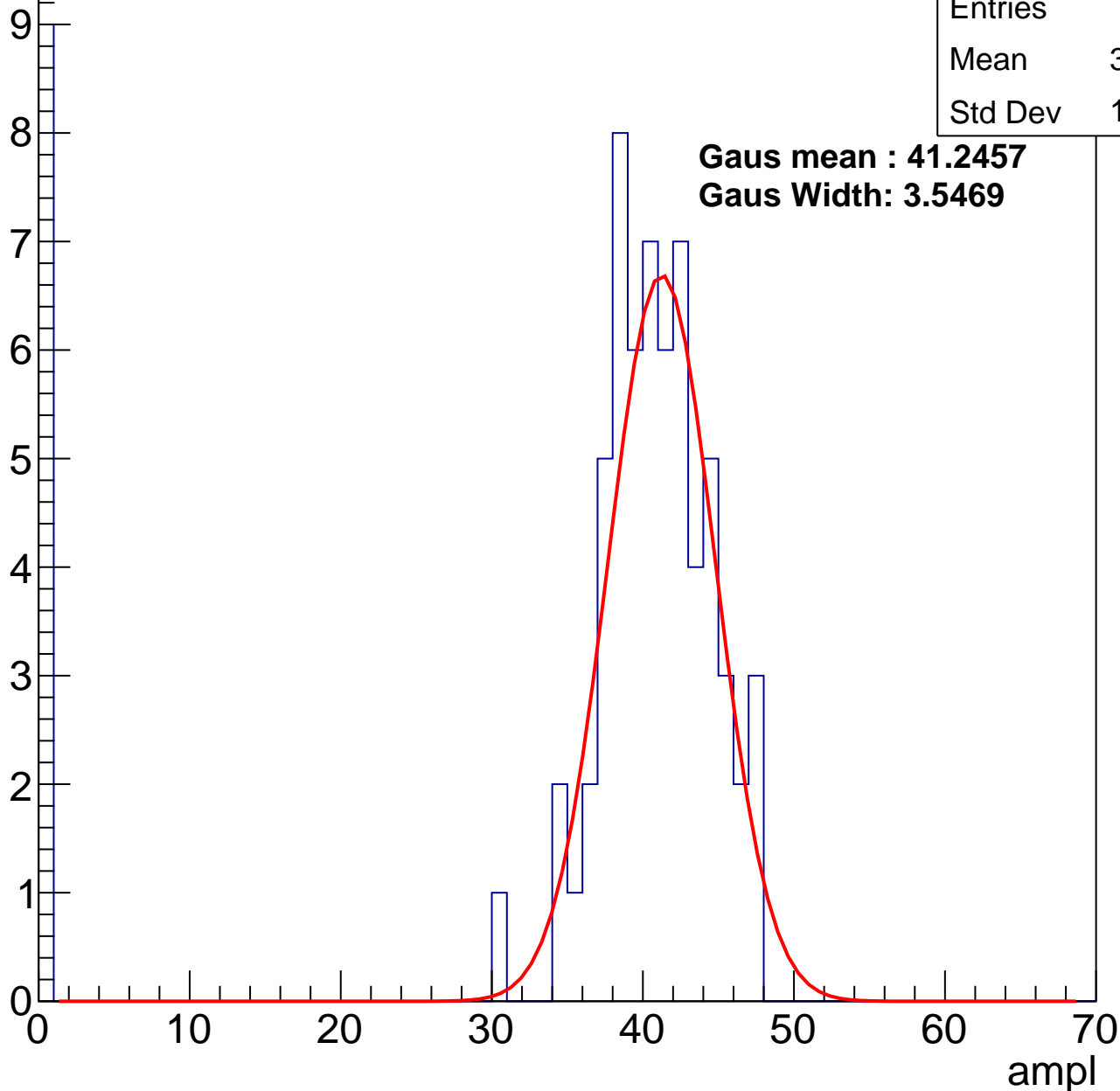
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	71
Mean	35.32
Std Dev	13.84

**Gaus mean : 41.2457**

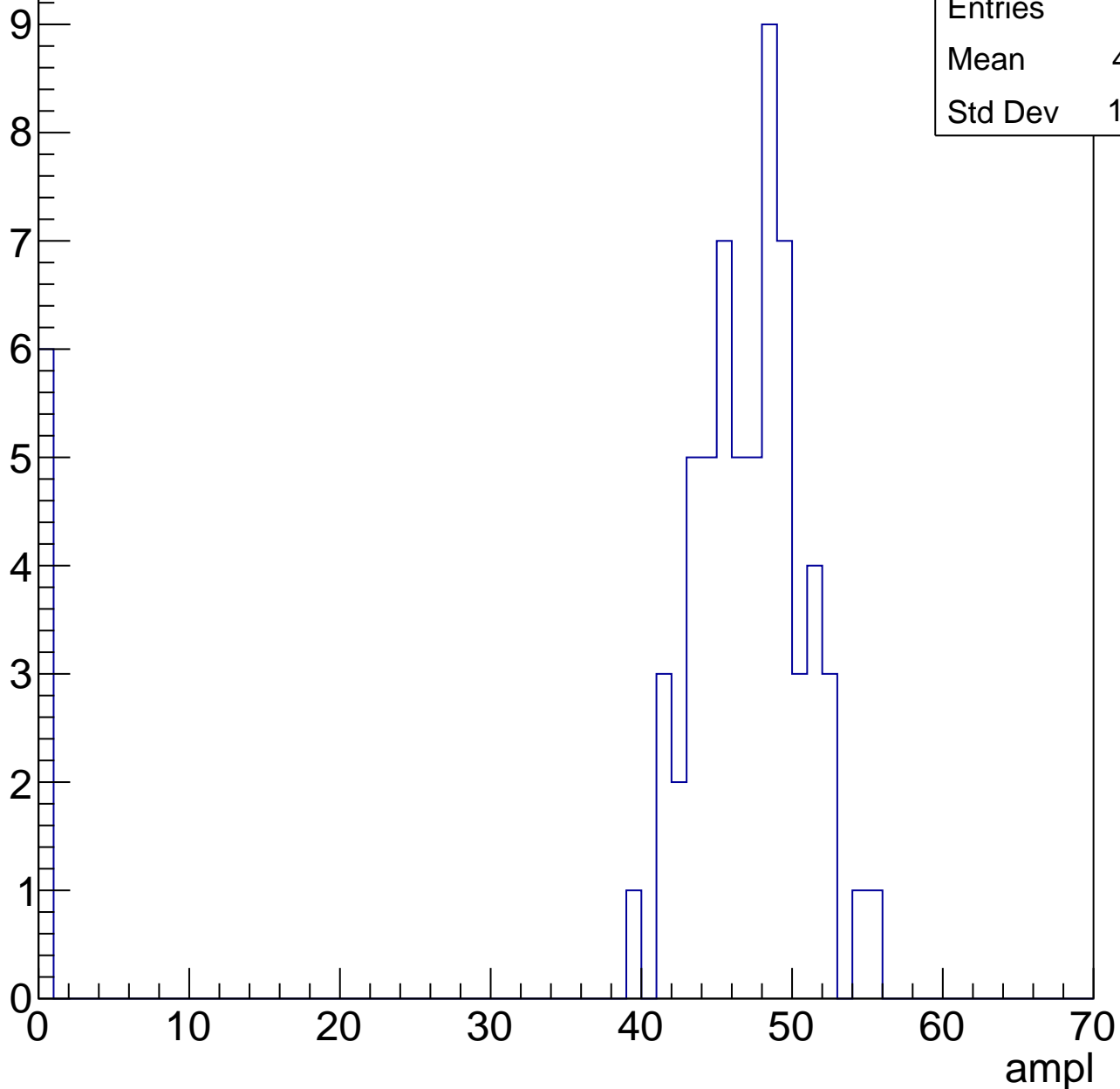
**Gaus Width: 3.5469**



# B1L103S, U3-ch35, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

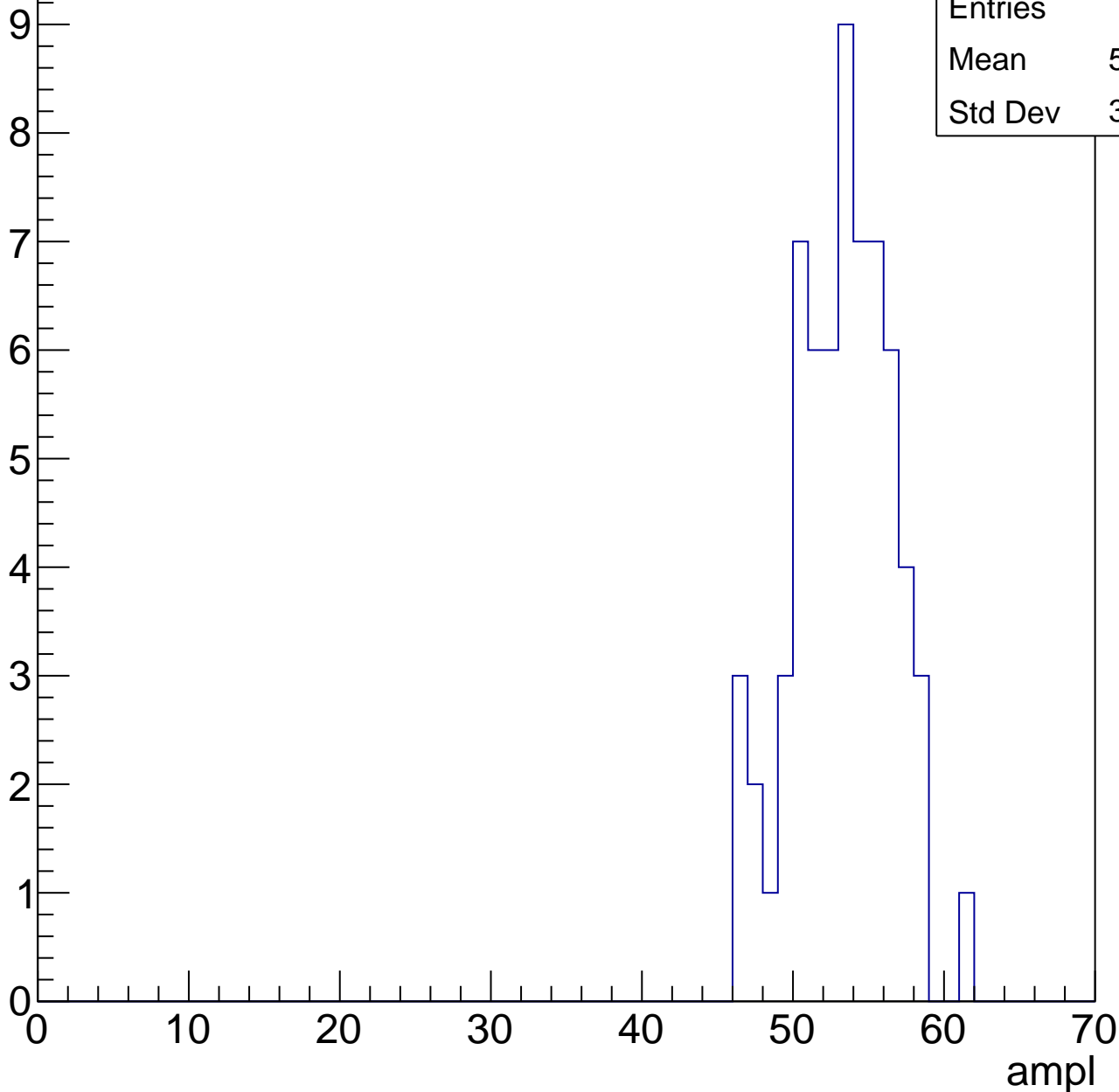


# B1L103S, U3-ch35, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

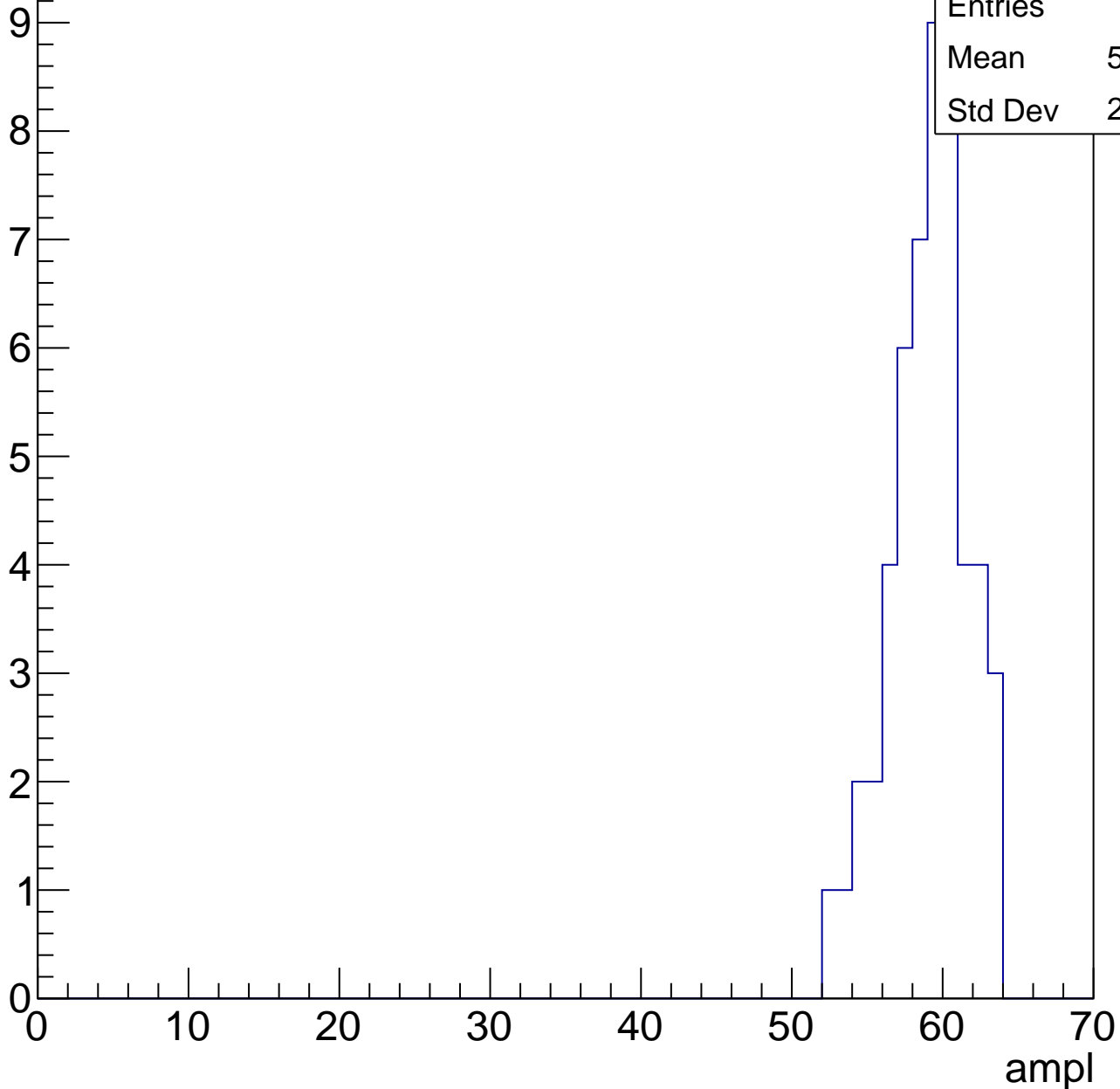
Entries	65
Mean	52.83
Std Dev	3.223



# B1L103S, U3-ch35, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

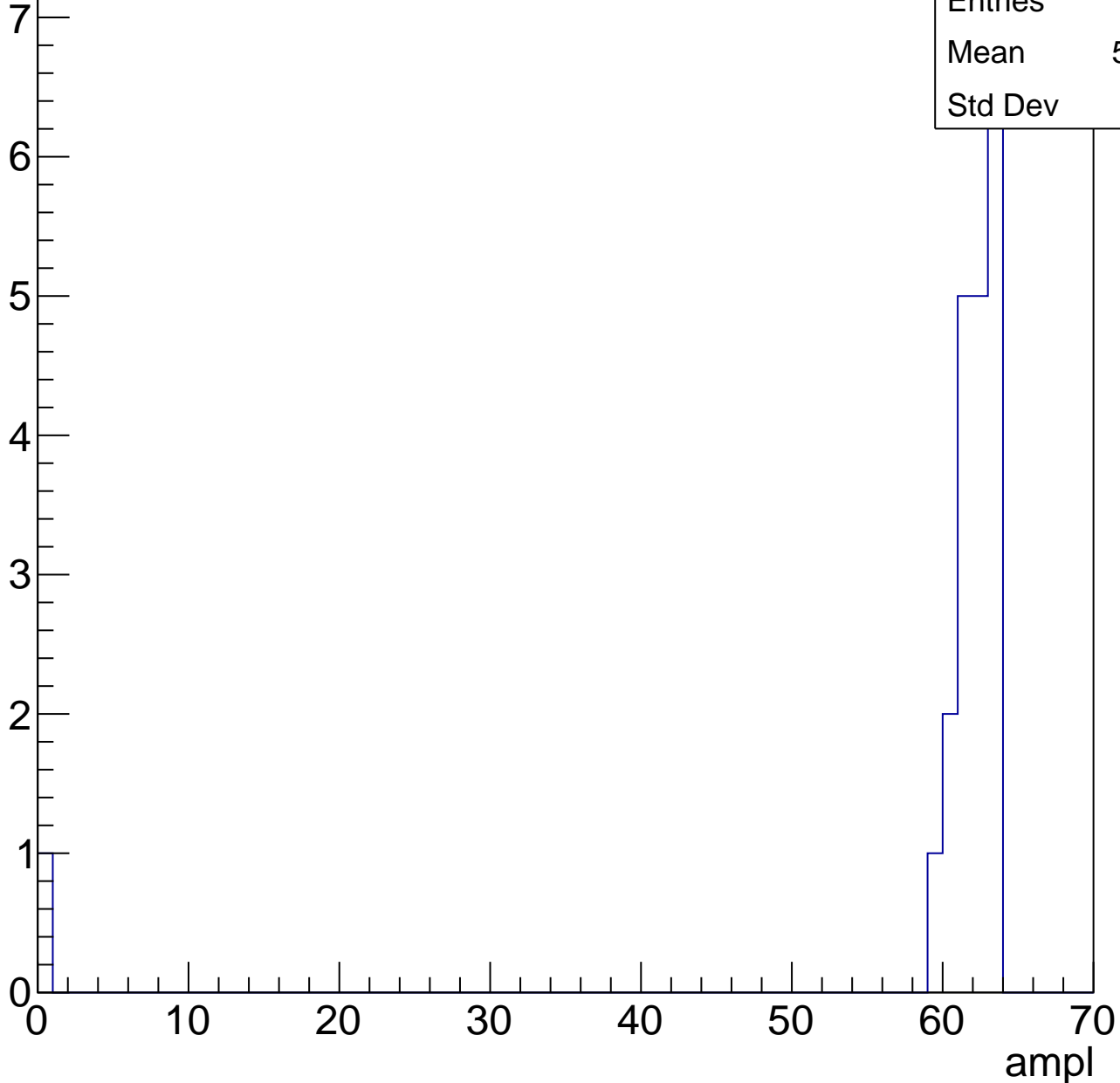


# B1L103S, U3-ch35, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	21
Mean	58.81
Std Dev	13.2

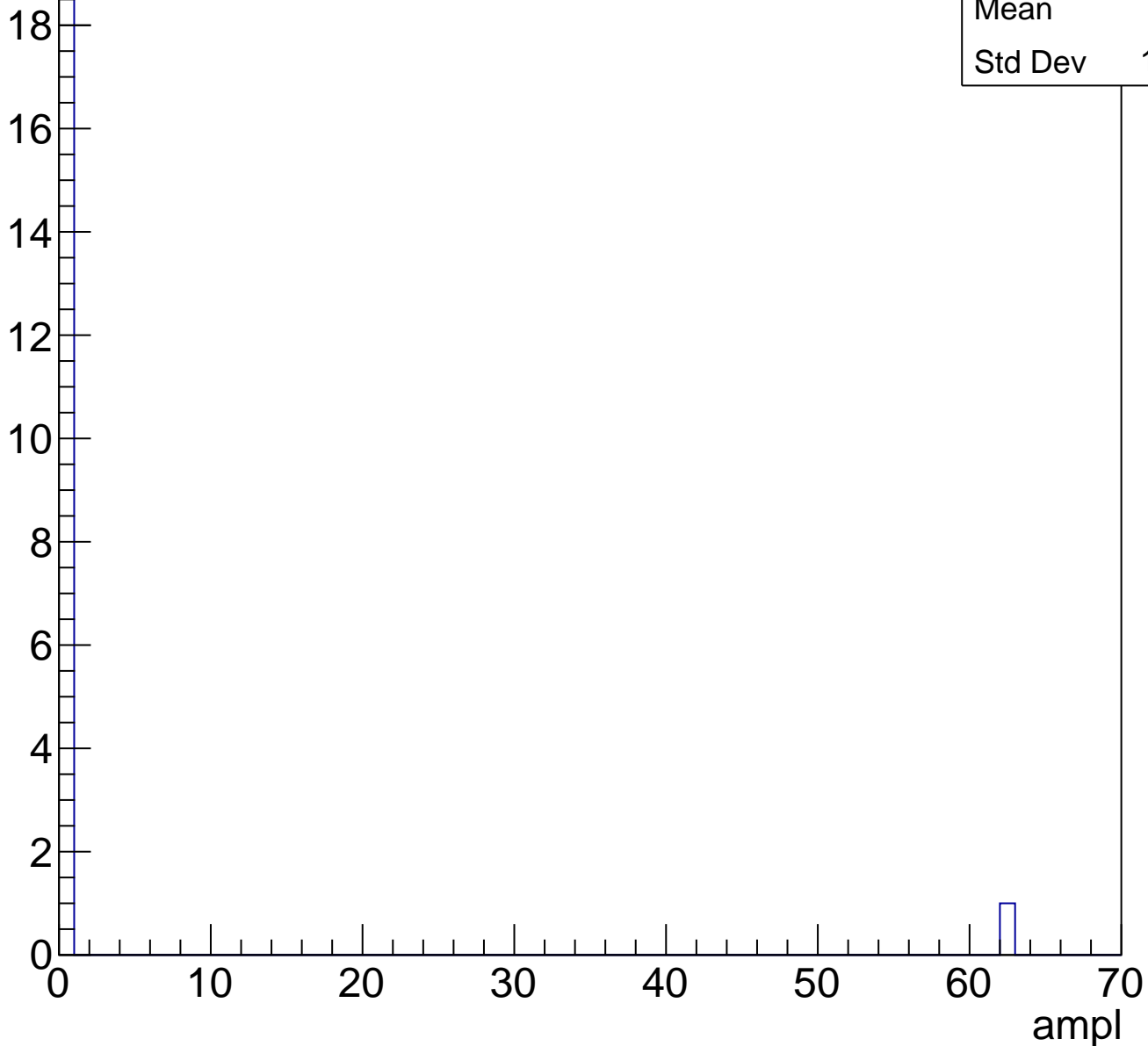




# B1L103S, U3-ch35, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	20
Mean	3.1
Std Dev	13.51

# B1L103S, U3-ch36, adc0

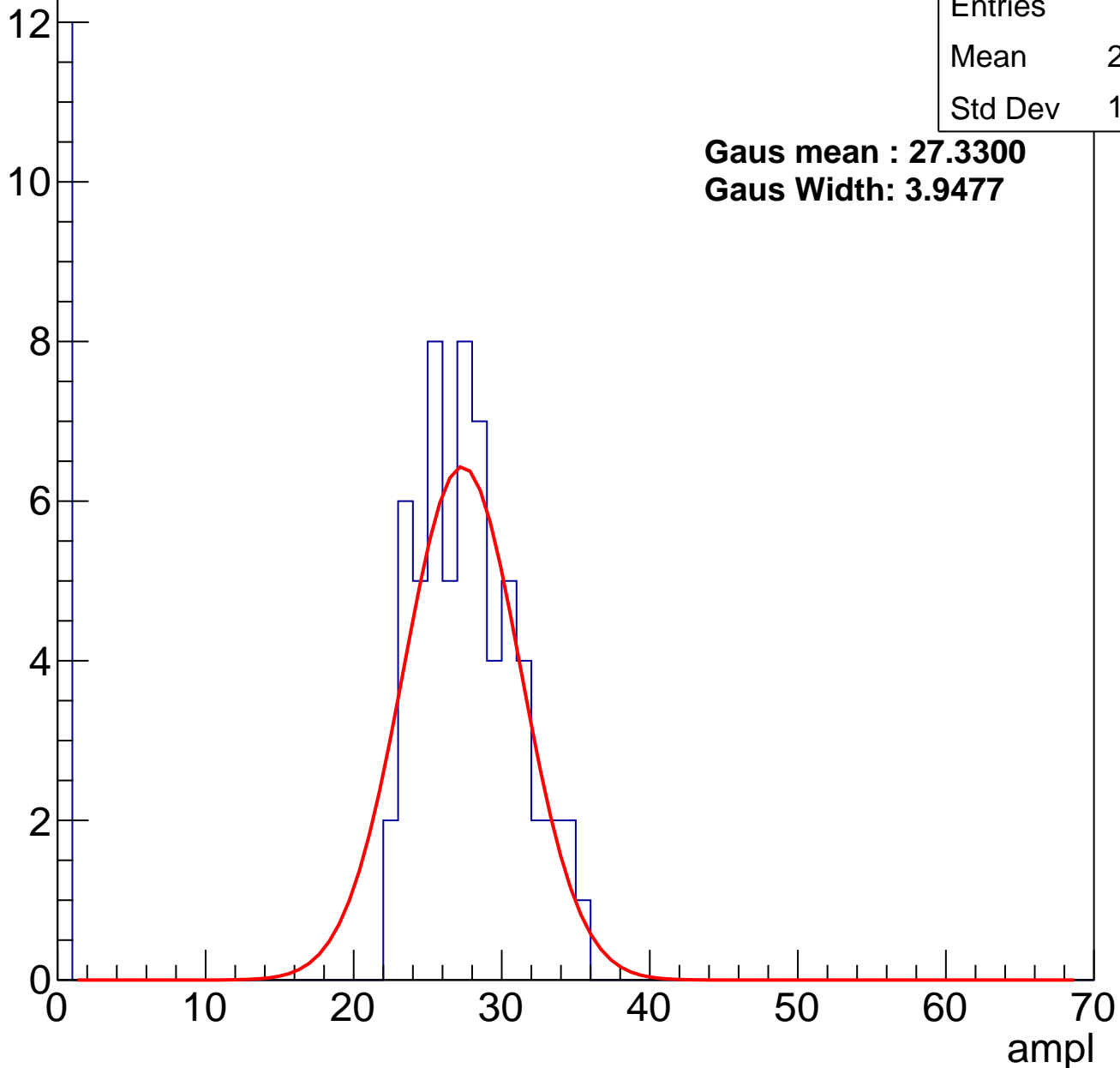
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	73
Mean	22.84
Std Dev	10.55

**Gaus mean : 27.3300**

**Gaus Width: 3.9477**

Entry



# B1L103S, U3-ch36, adc1

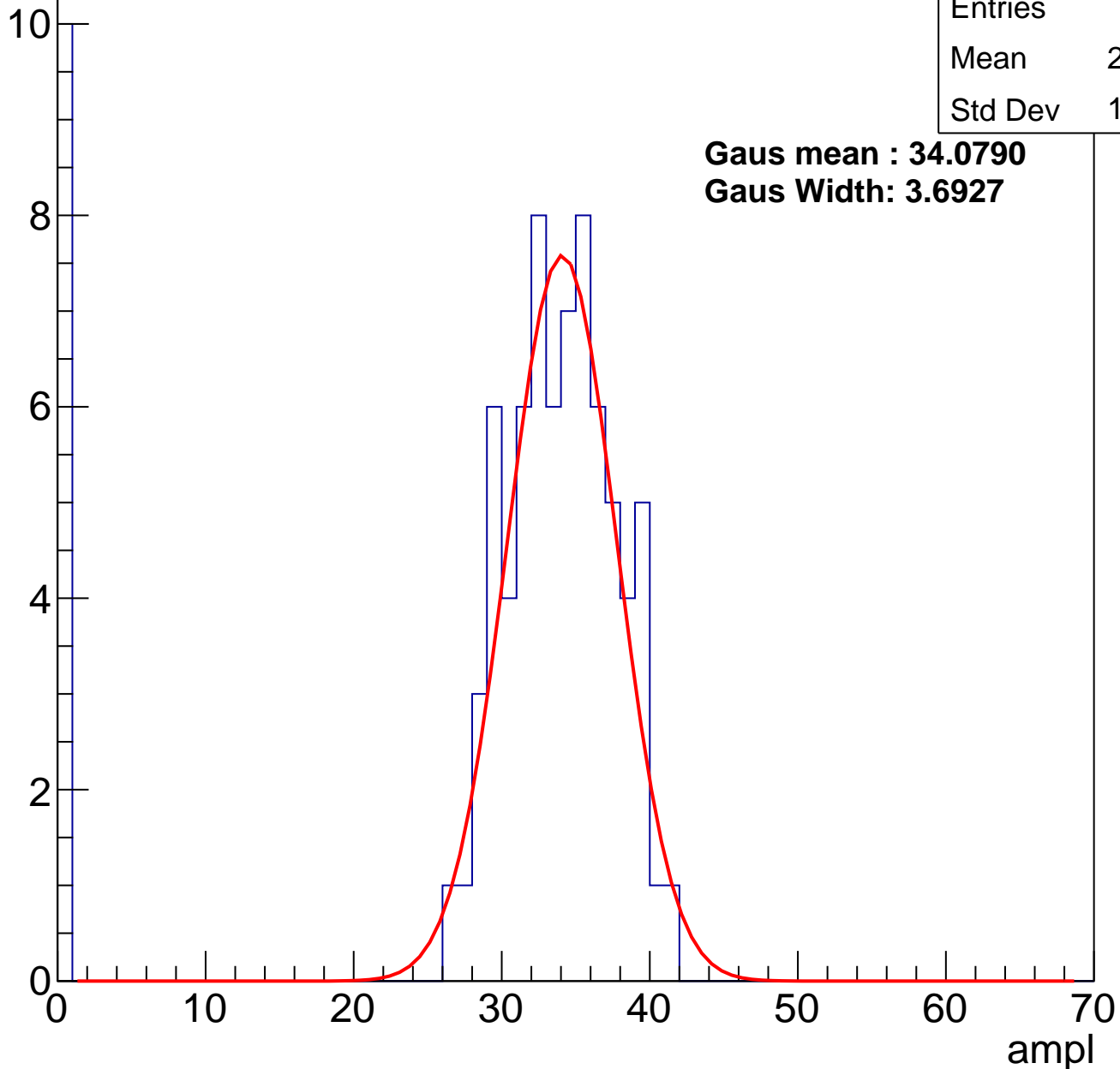
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	82
Mean	29.49
Std Dev	11.46

**Gaus mean : 34.0790**

**Gaus Width: 3.6927**

Entry



# B1L103S, U3-ch36, adc2

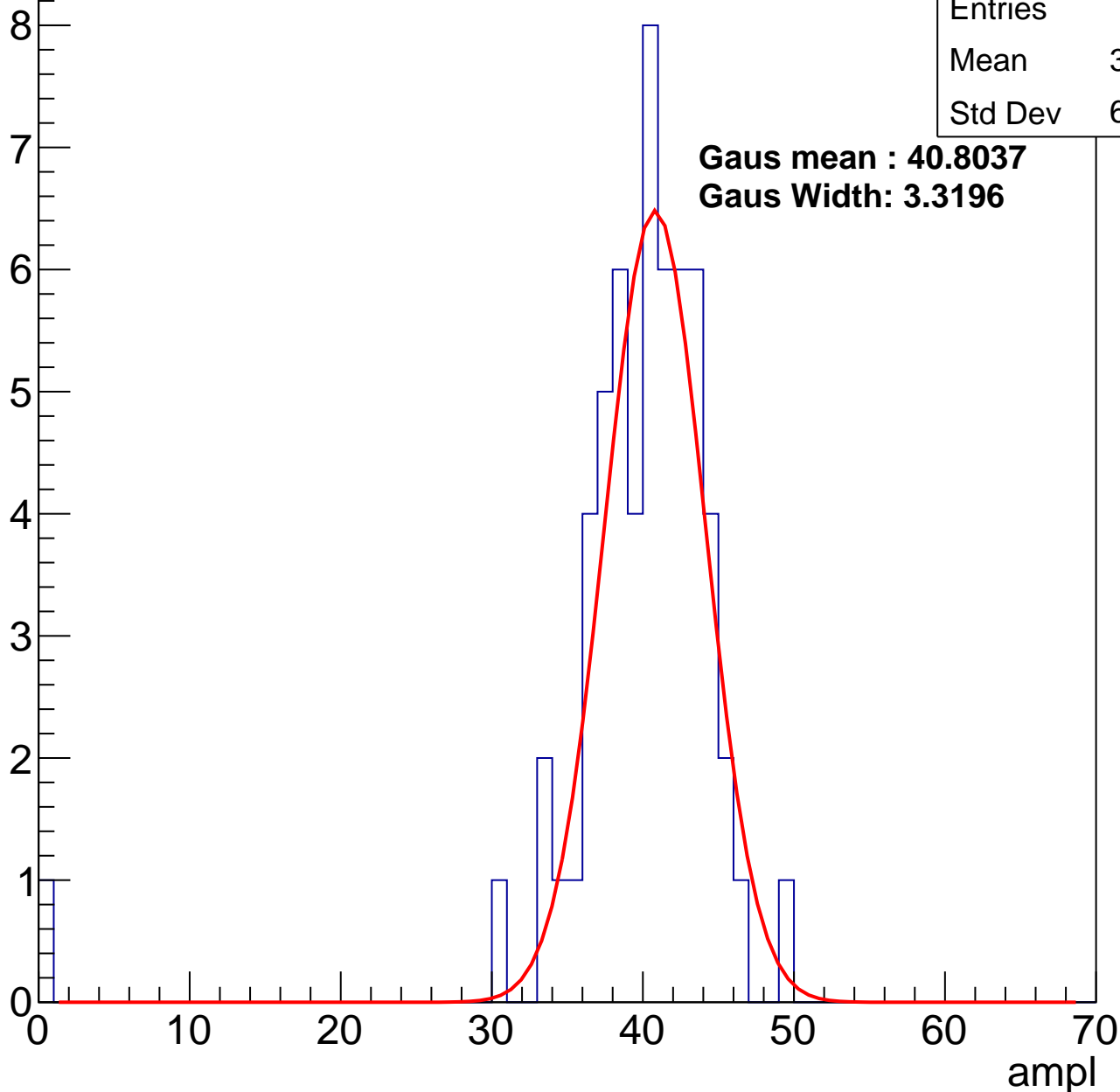
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	39.24
Std Dev	6.212

**Gaus mean : 40.8037**

**Gaus Width: 3.3196**

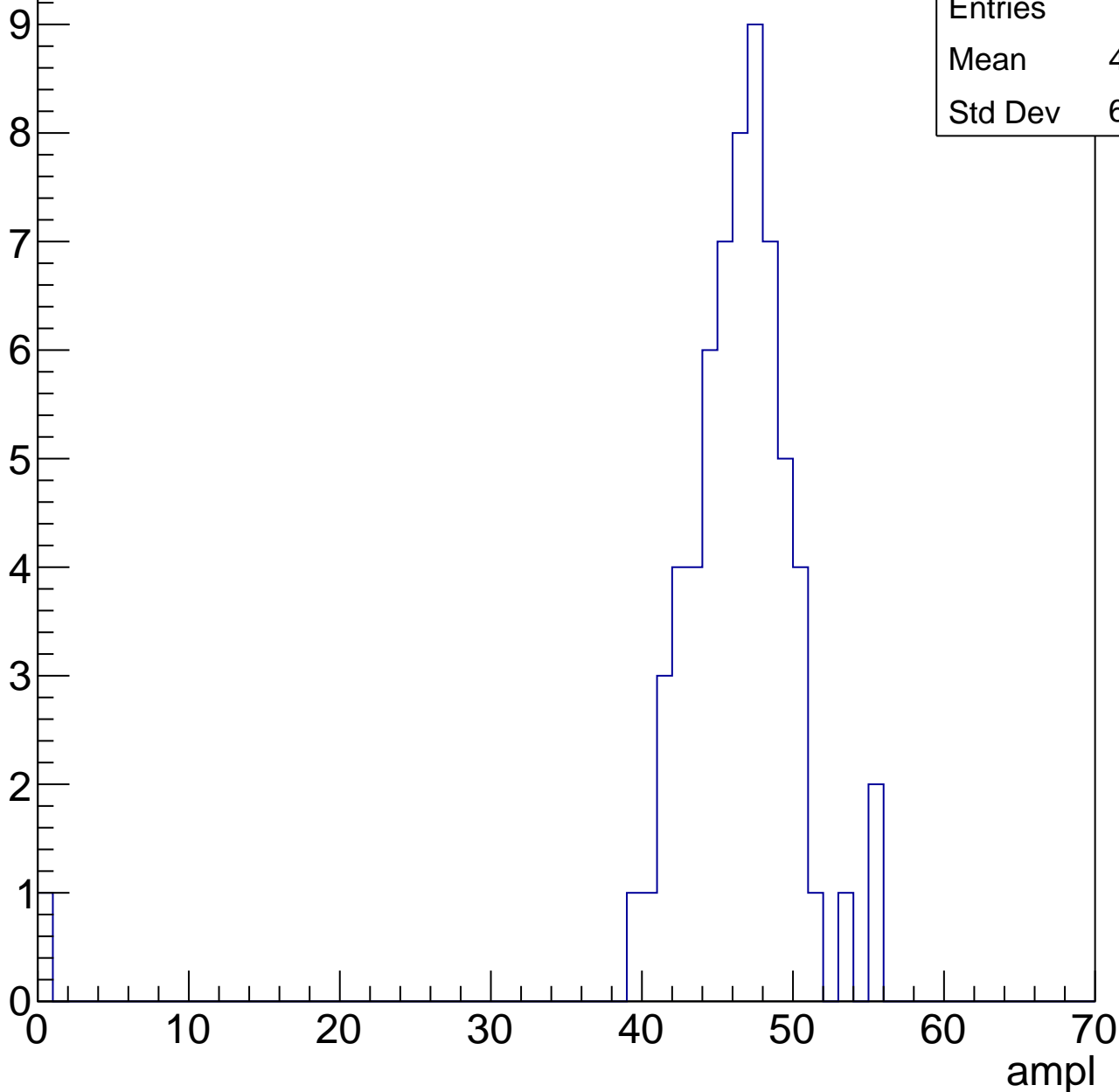


# B1L103S, U3-ch36, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	45.42
Std Dev	6.576

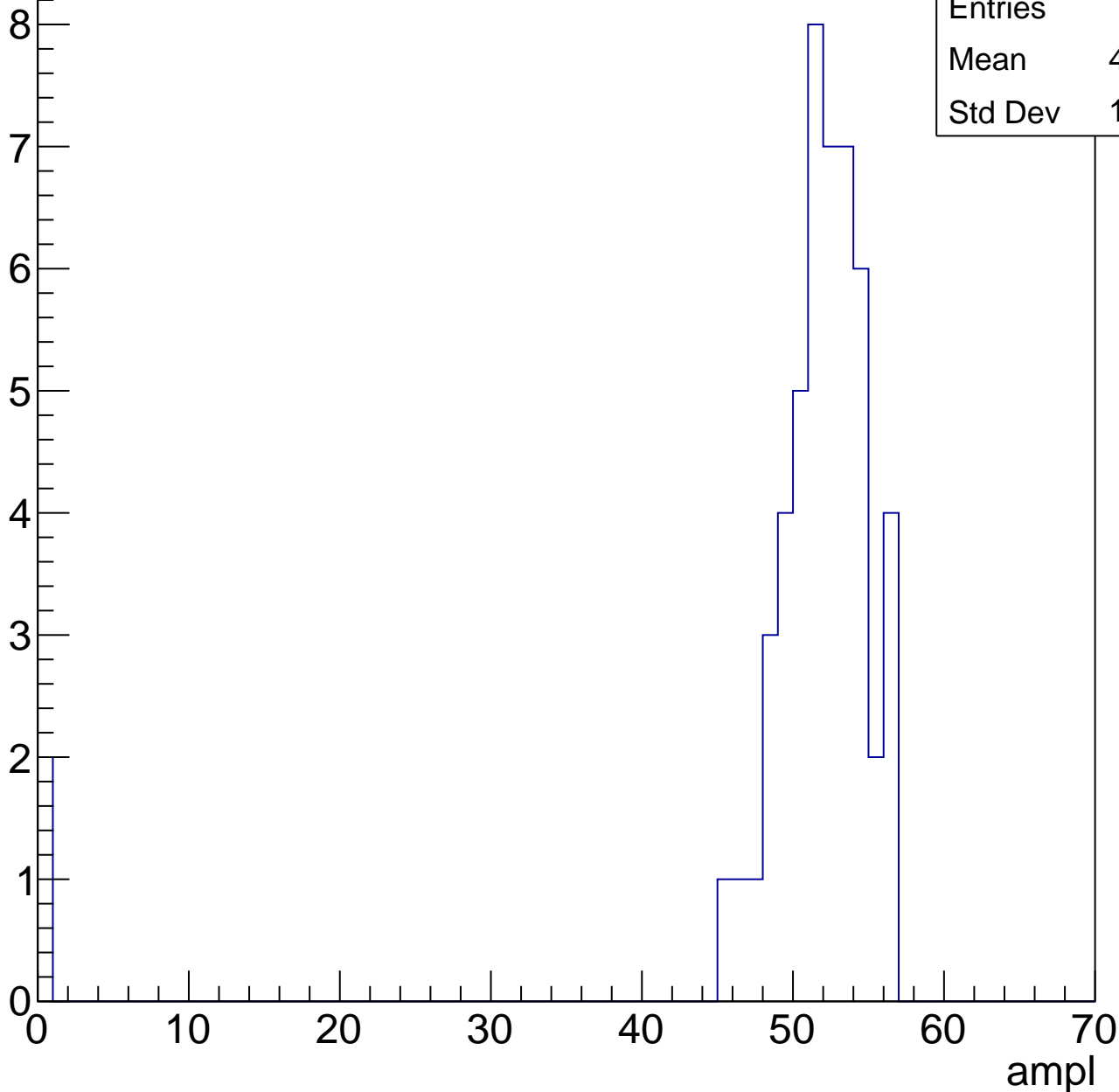


# B1L103S, U3-ch36, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

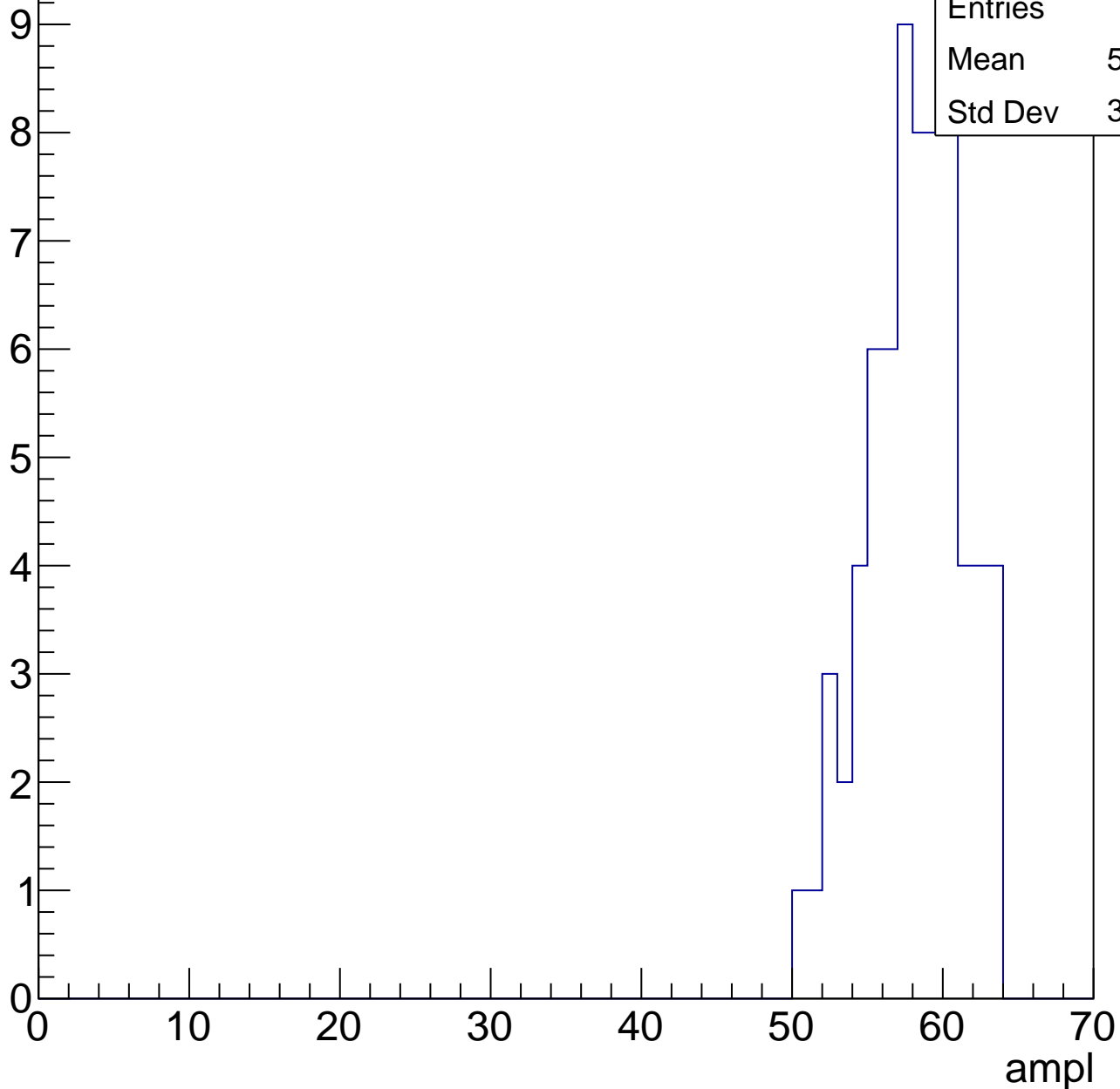
Entries	51
Mean	49.59
Std Dev	10.33



# B1L103S, U3-ch36, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



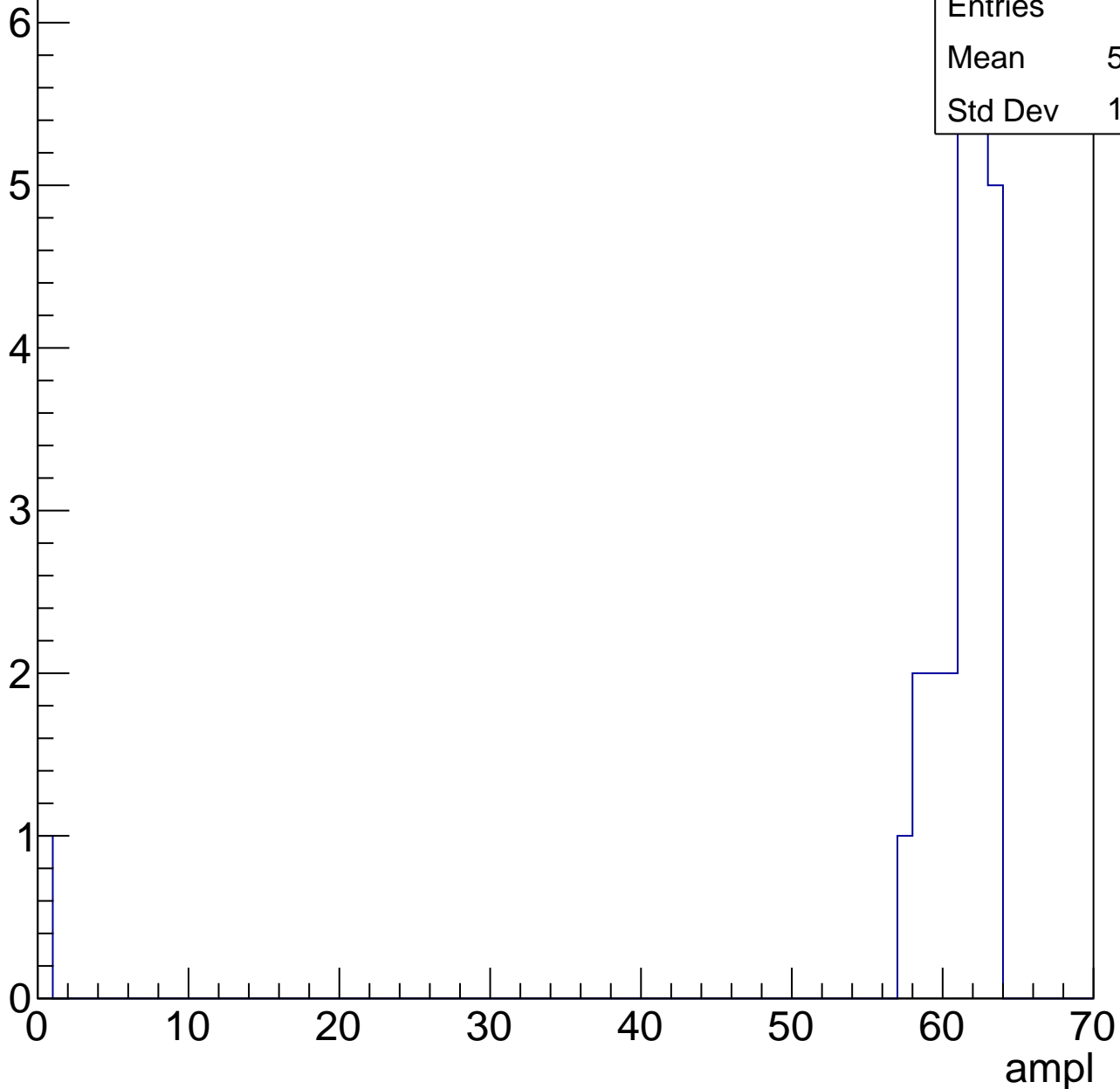
Entries	68
Mean	57.62
Std Dev	3.097

# B1L103S, U3-ch36, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	25
Mean	58.56
Std Dev	12.07



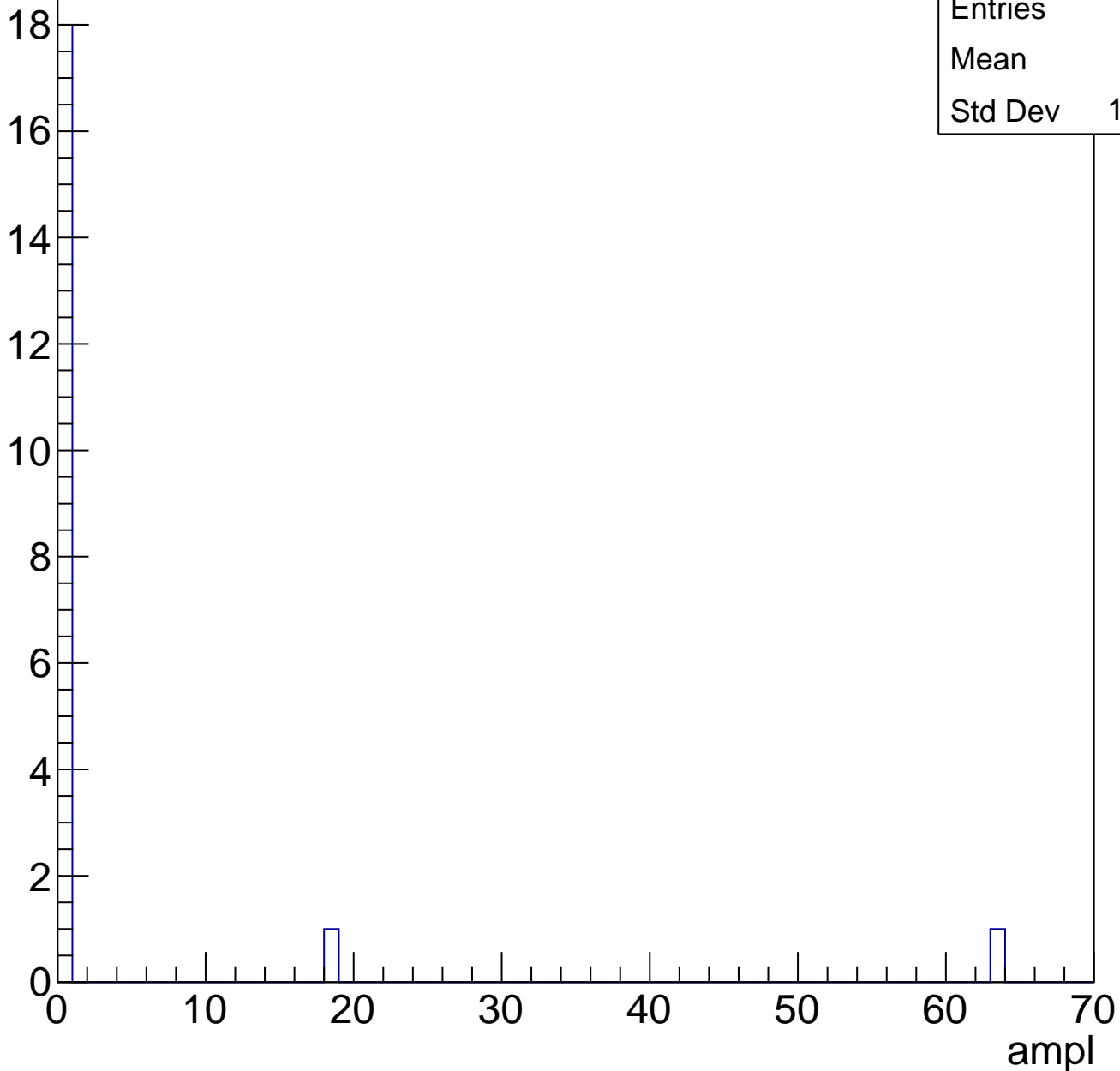


# B1L103S, U3-ch36, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	4.05
Std Dev	14.08

Entry



# B1L103S, U3-ch37, adc0

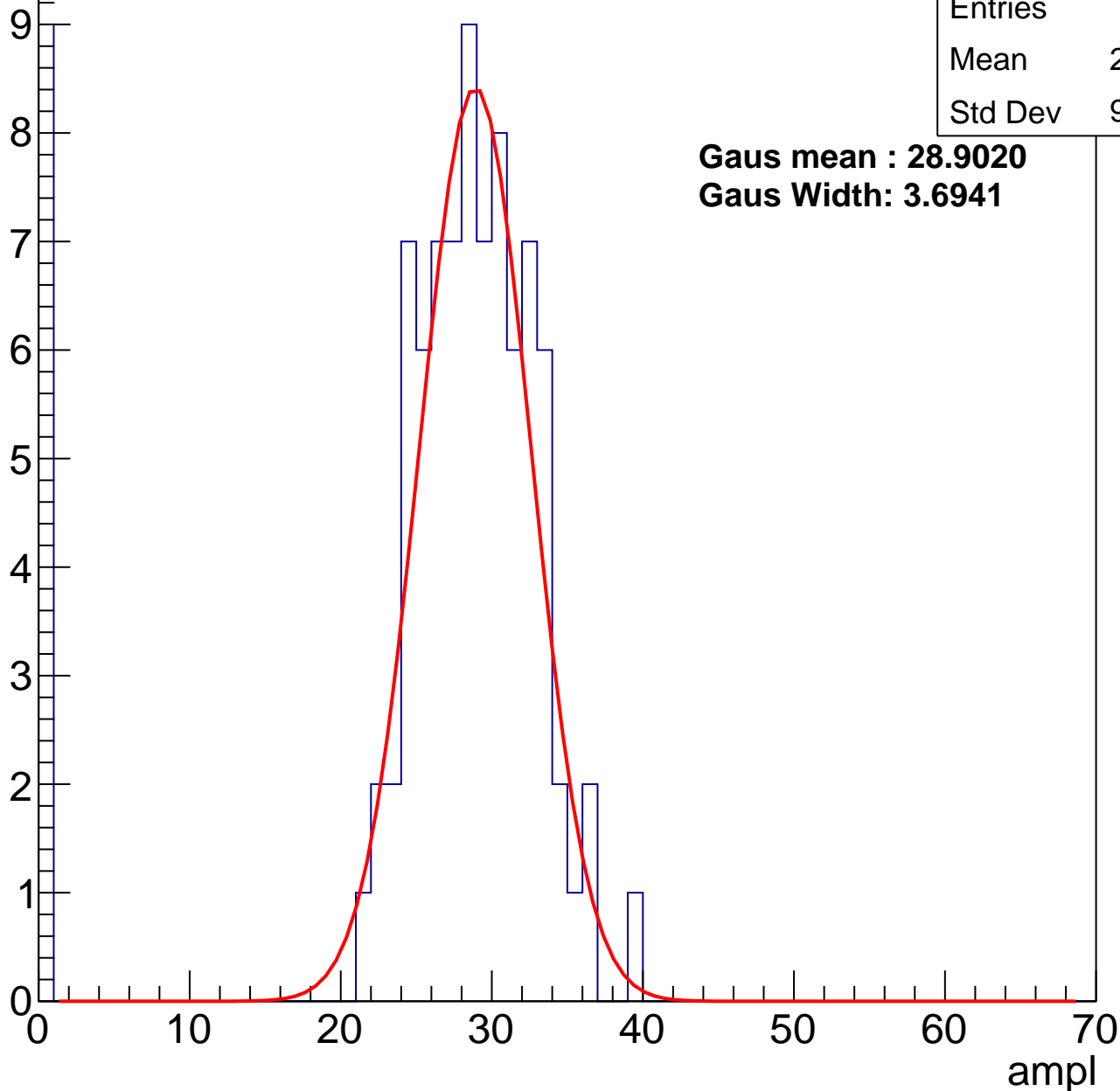
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	90
Mean	25.74
Std Dev	9.247

**Gaus mean : 28.9020**

**Gaus Width: 3.6941**



# B1L103S, U3-ch37, adc1

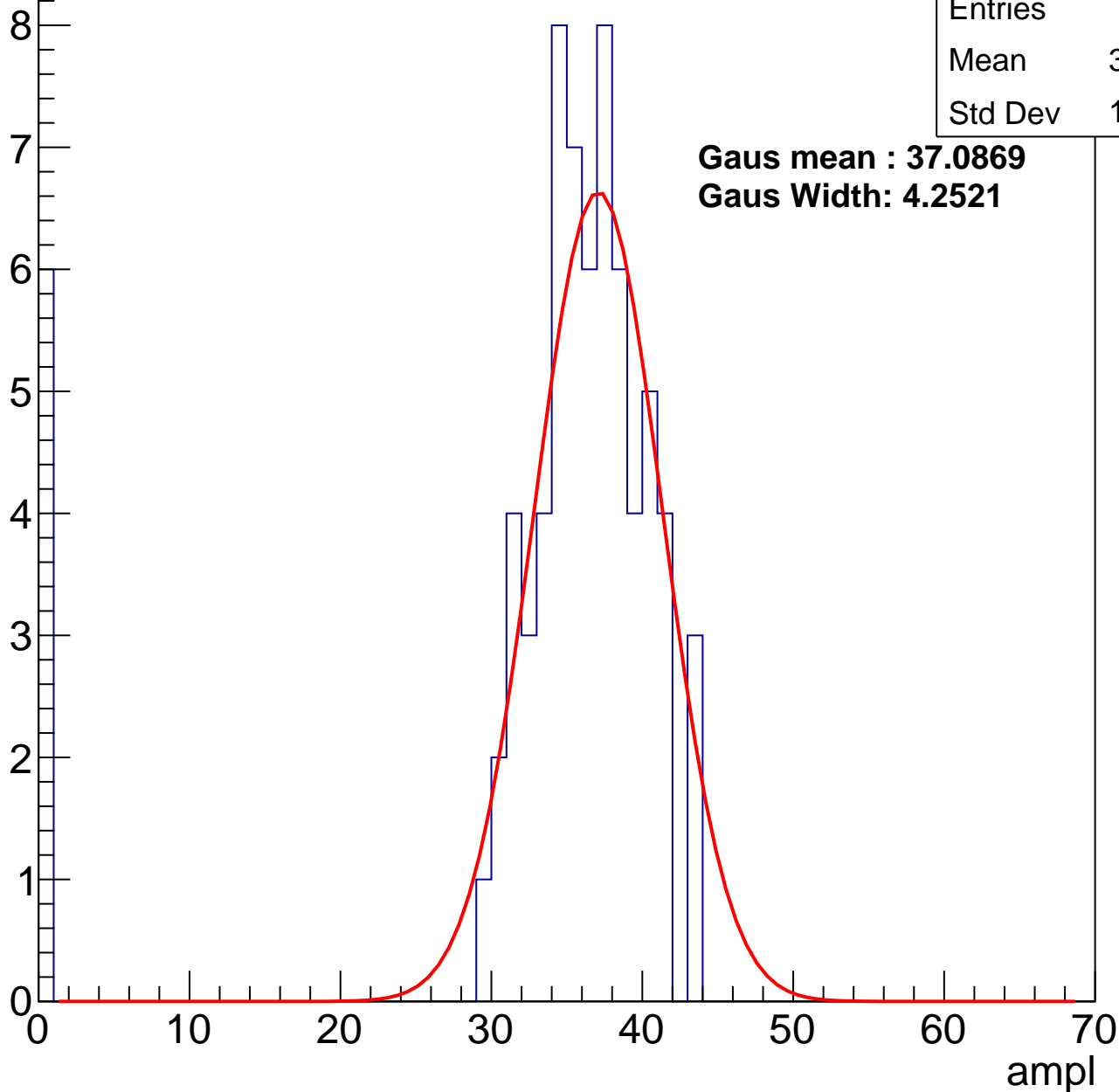
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	71
Mean	33.06
Std Dev	10.55

**Gaus mean : 37.0869**

**Gaus Width: 4.2521**



# B1L103S, U3-ch37, adc2

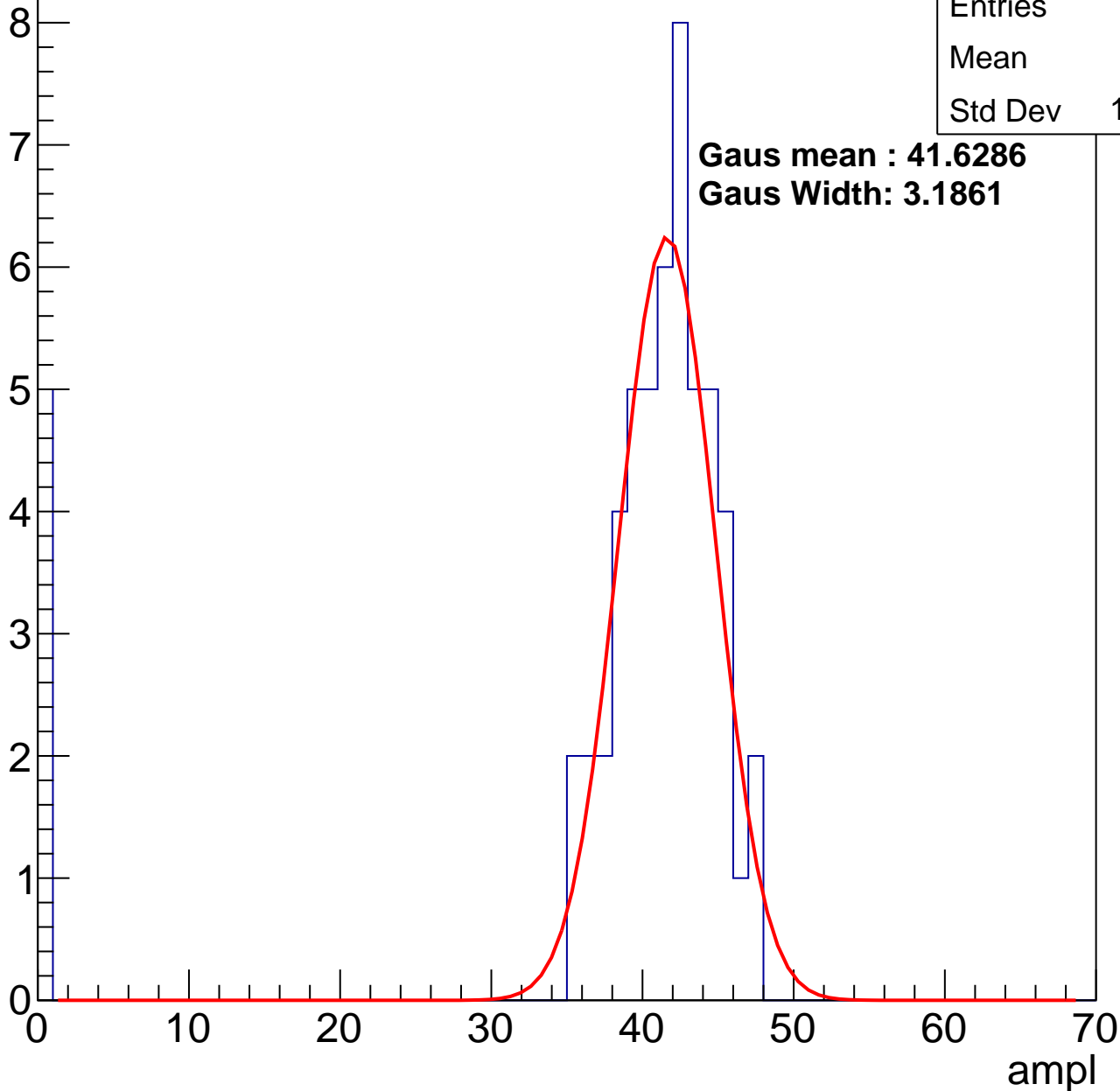
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	56
Mean	37.5
Std Dev	12.08

**Gaus mean : 41.6286**

**Gaus Width: 3.1861**

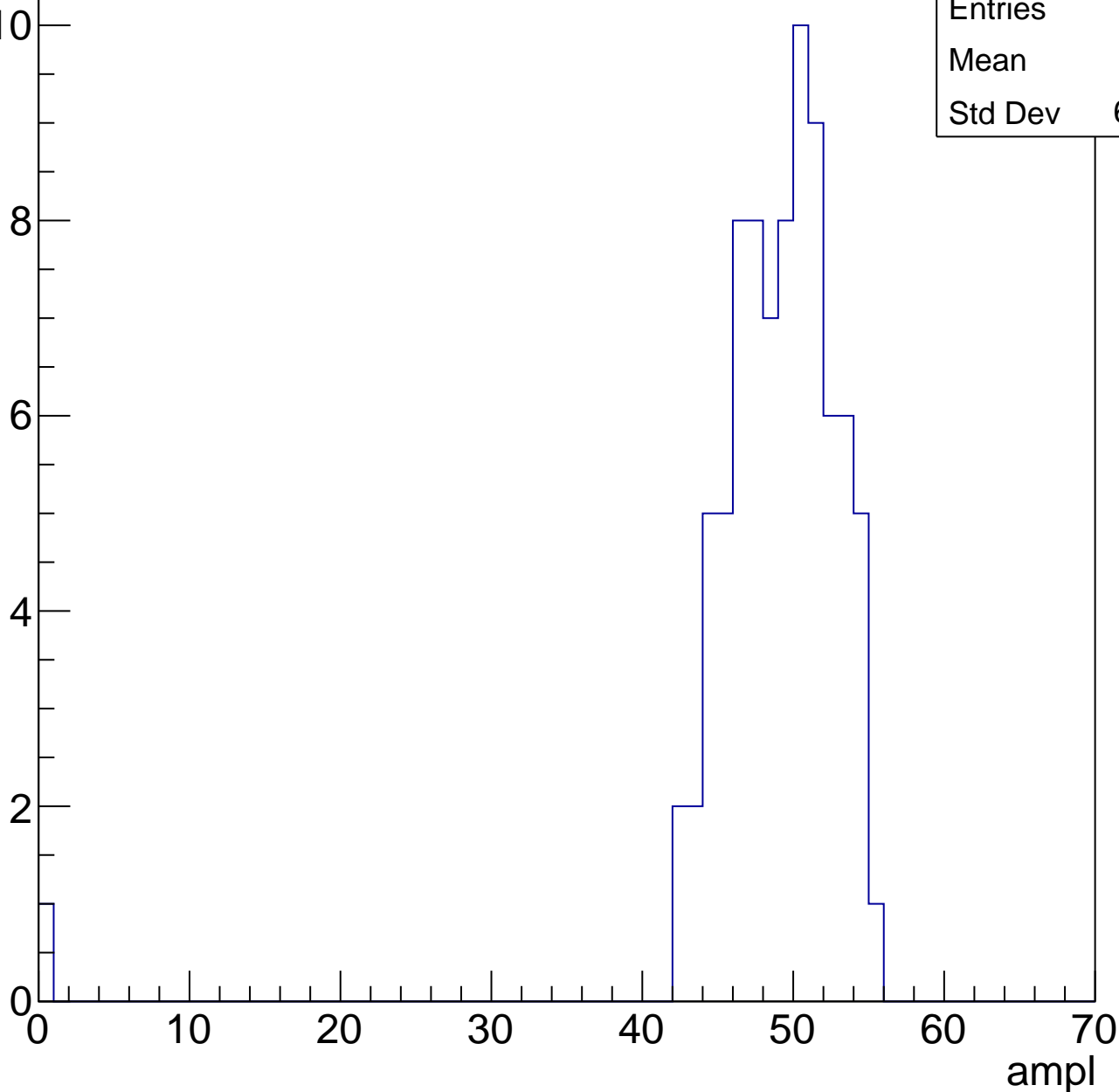


# B1L103S, U3-ch37, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

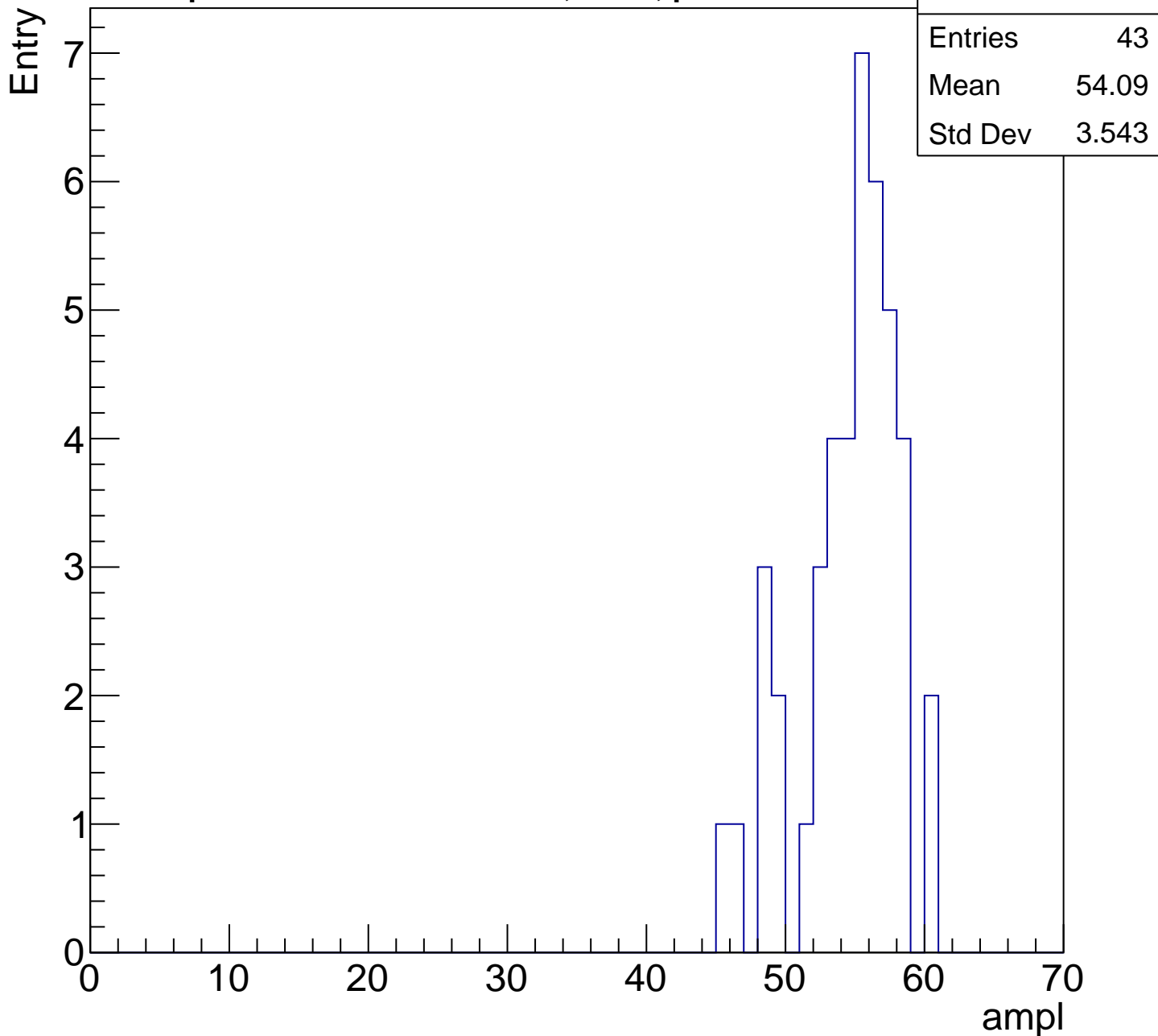
Entry

Entries	83
Mean	48.2
Std Dev	6.201



# B1L103S, U3-ch37, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

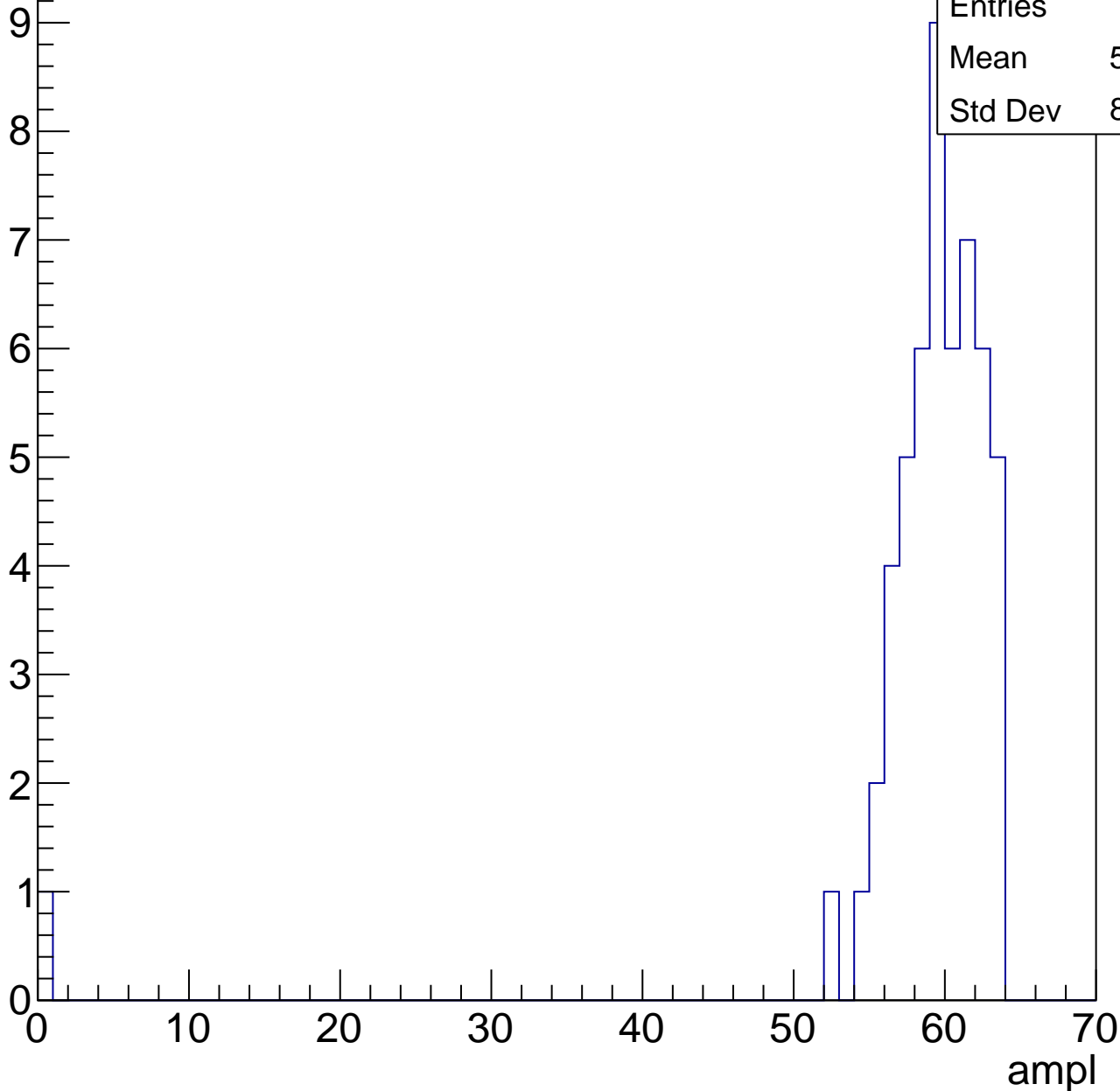


# B1L103S, U3-ch37, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	53
Mean	58.08
Std Dev	8.436

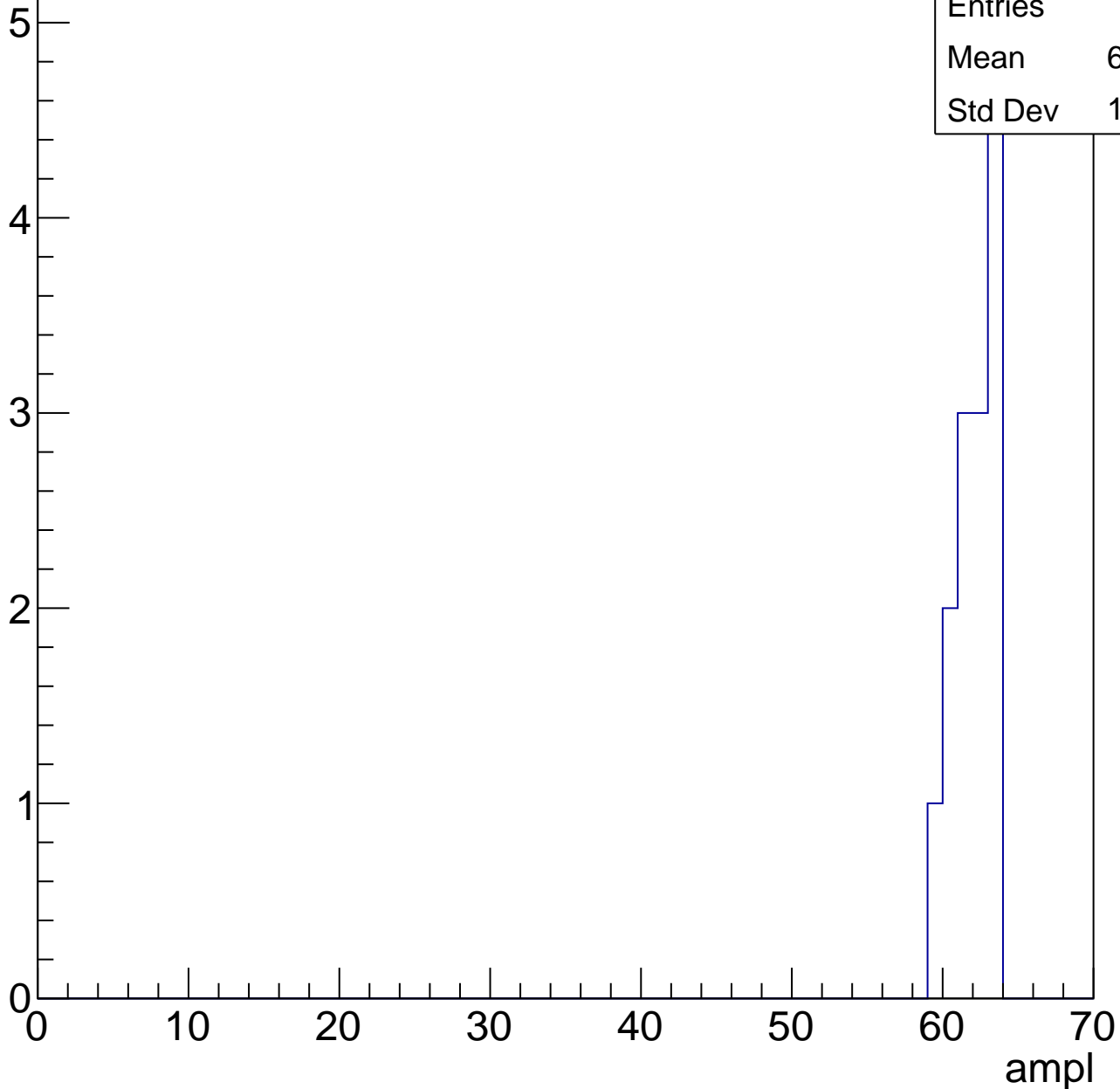


# B1L103S, U3-ch37, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	14
Mean	61.64
Std Dev	1.288





# B1L103S, U3-ch37, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51

Entry



# B1L103S, U3-ch38, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	86
Mean	19.03
Std Dev	13.14

**Gaus mean : 28.2070**

**Gaus Width: 3.5297**

Entry

25

20

15

10

5

0

0

10

20

30

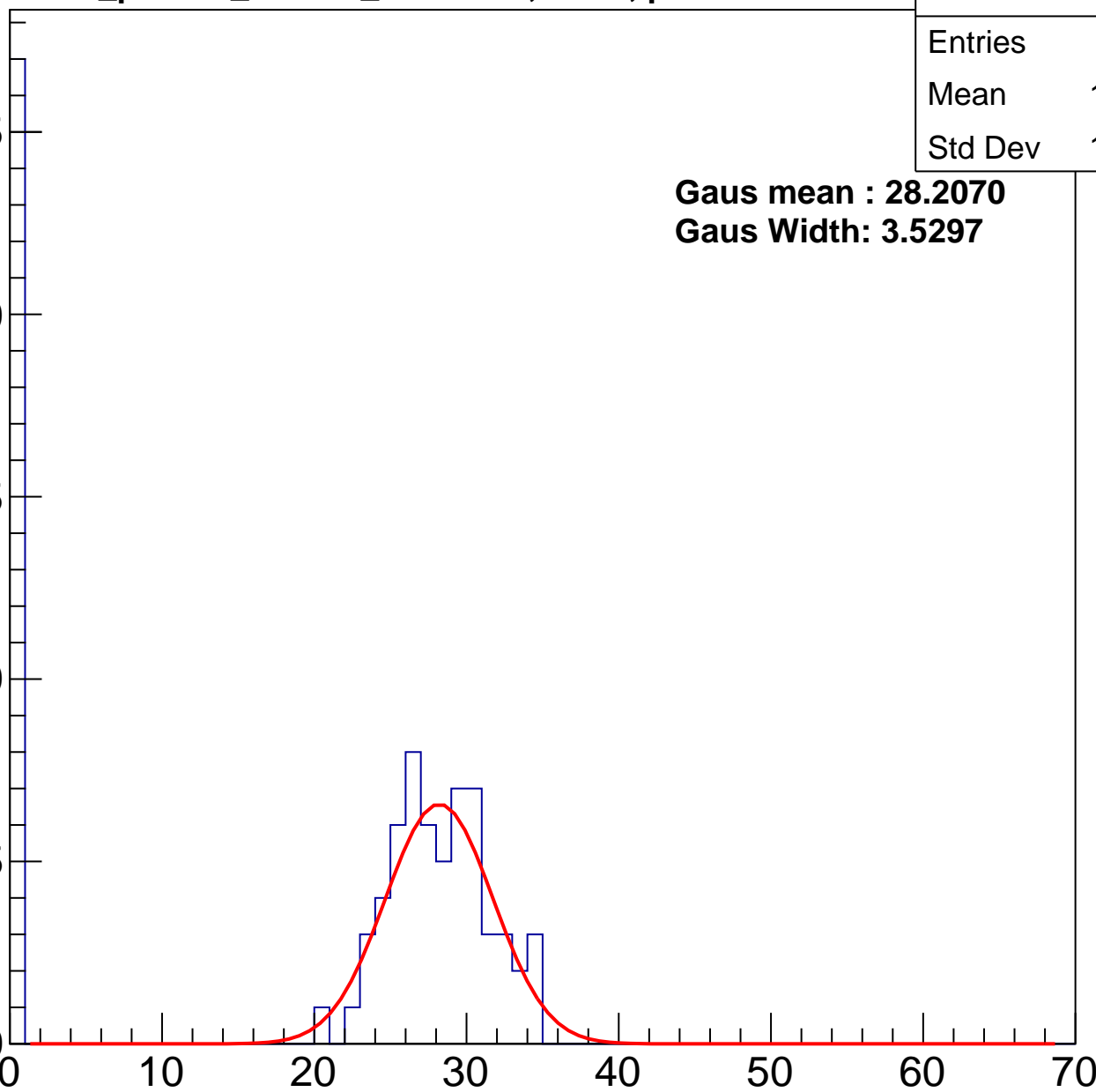
40

50

60

70

ampl



# B1L103S, U3-ch38, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	90
Mean	28.69
Std Dev	13.3

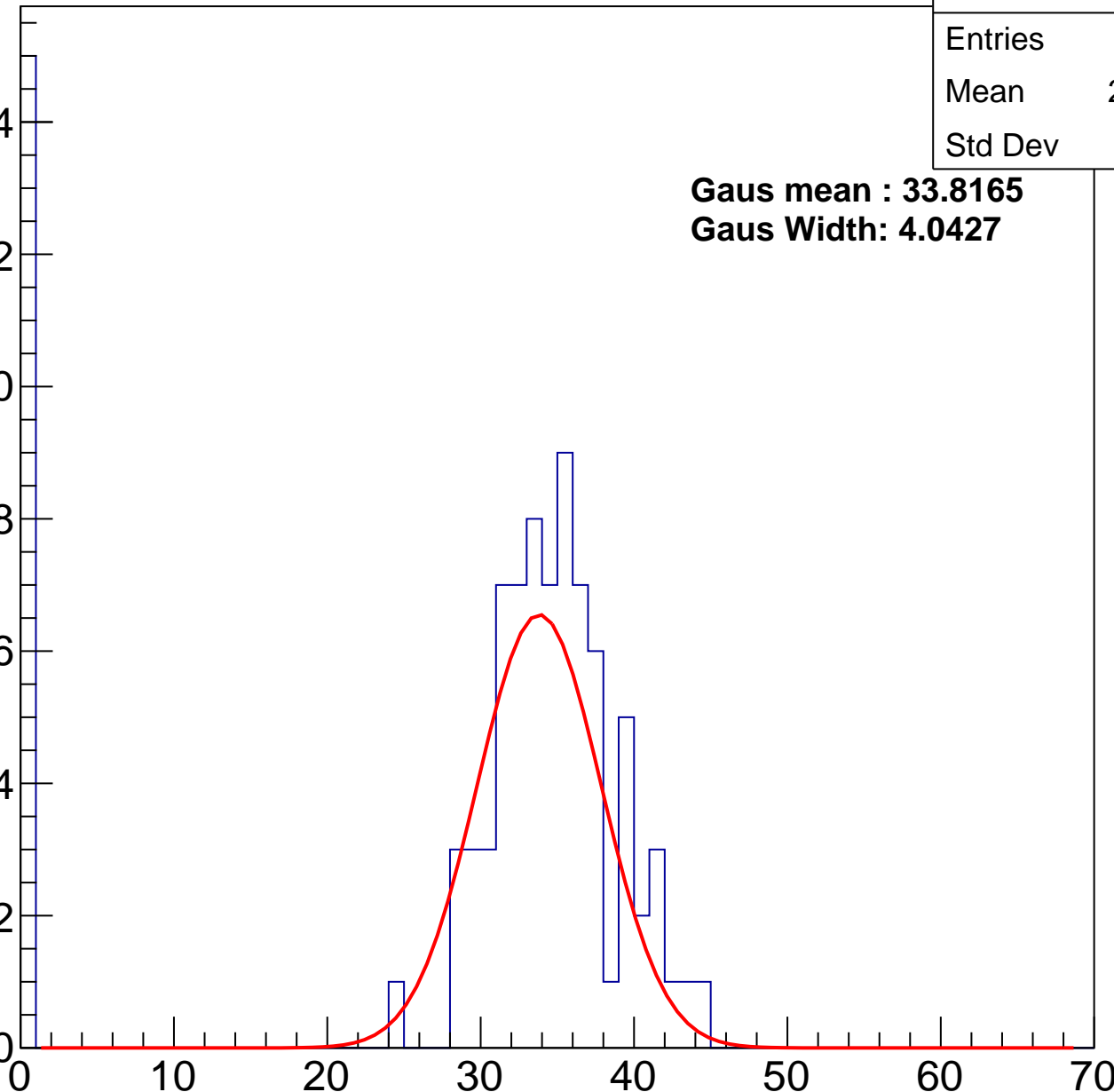
**Gaus mean : 33.8165**

**Gaus Width: 4.0427**

Entry

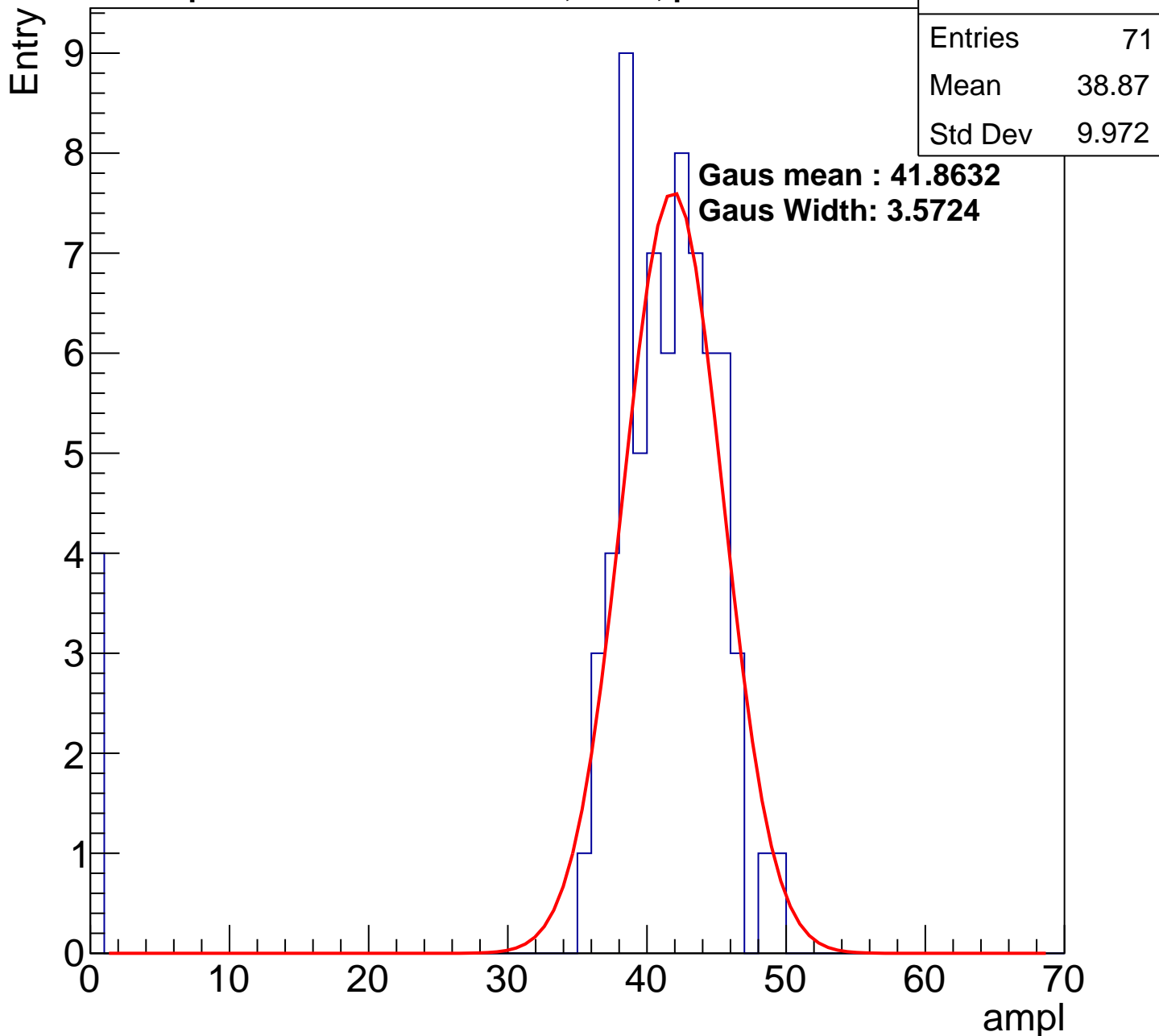
14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U3-ch38, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

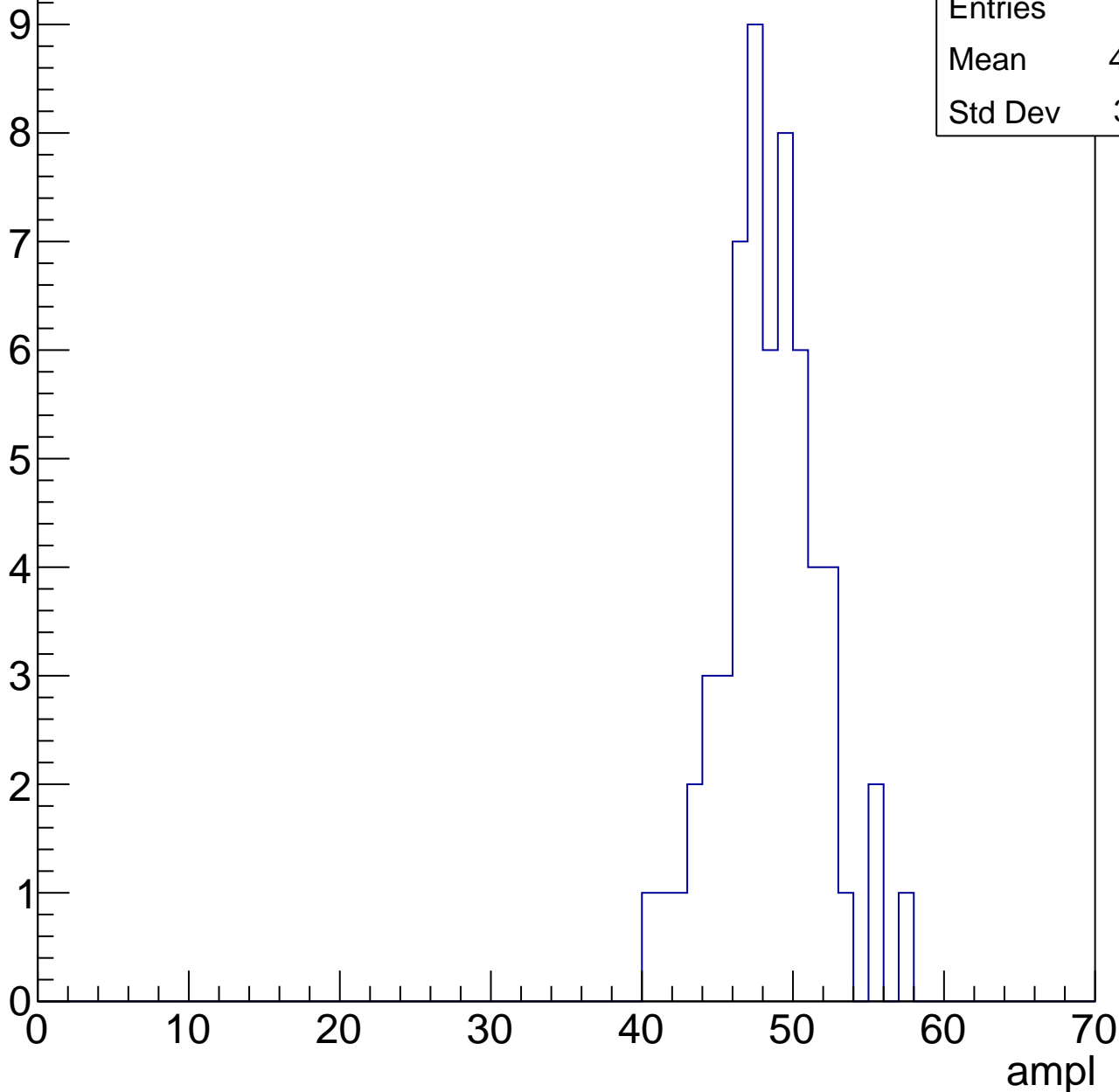


# B1L103S, U3-ch38, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	48.02
Std Dev	3.311

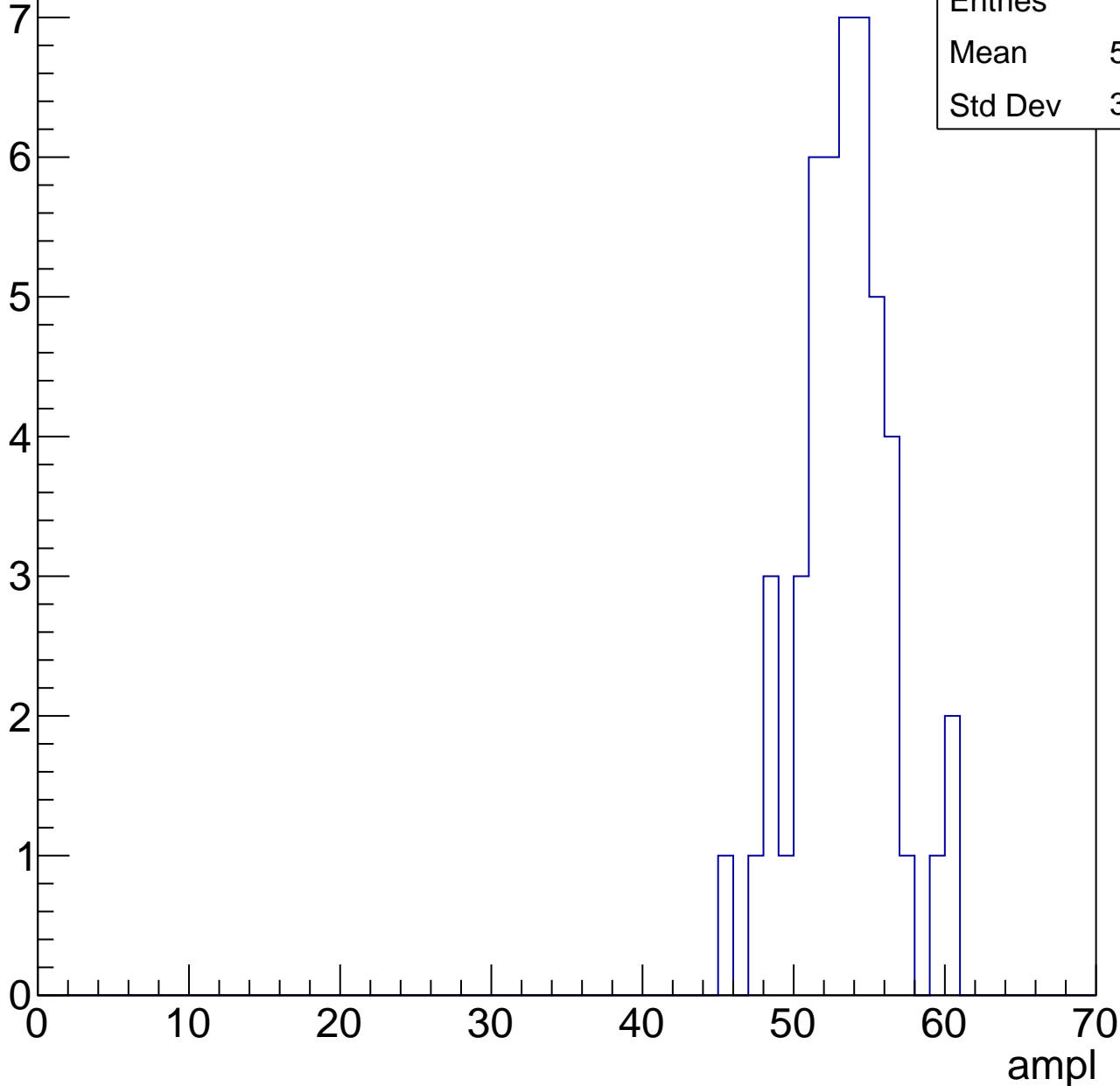


# B1L103S, U3-ch38, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	48
Mean	52.85
Std Dev	3.096

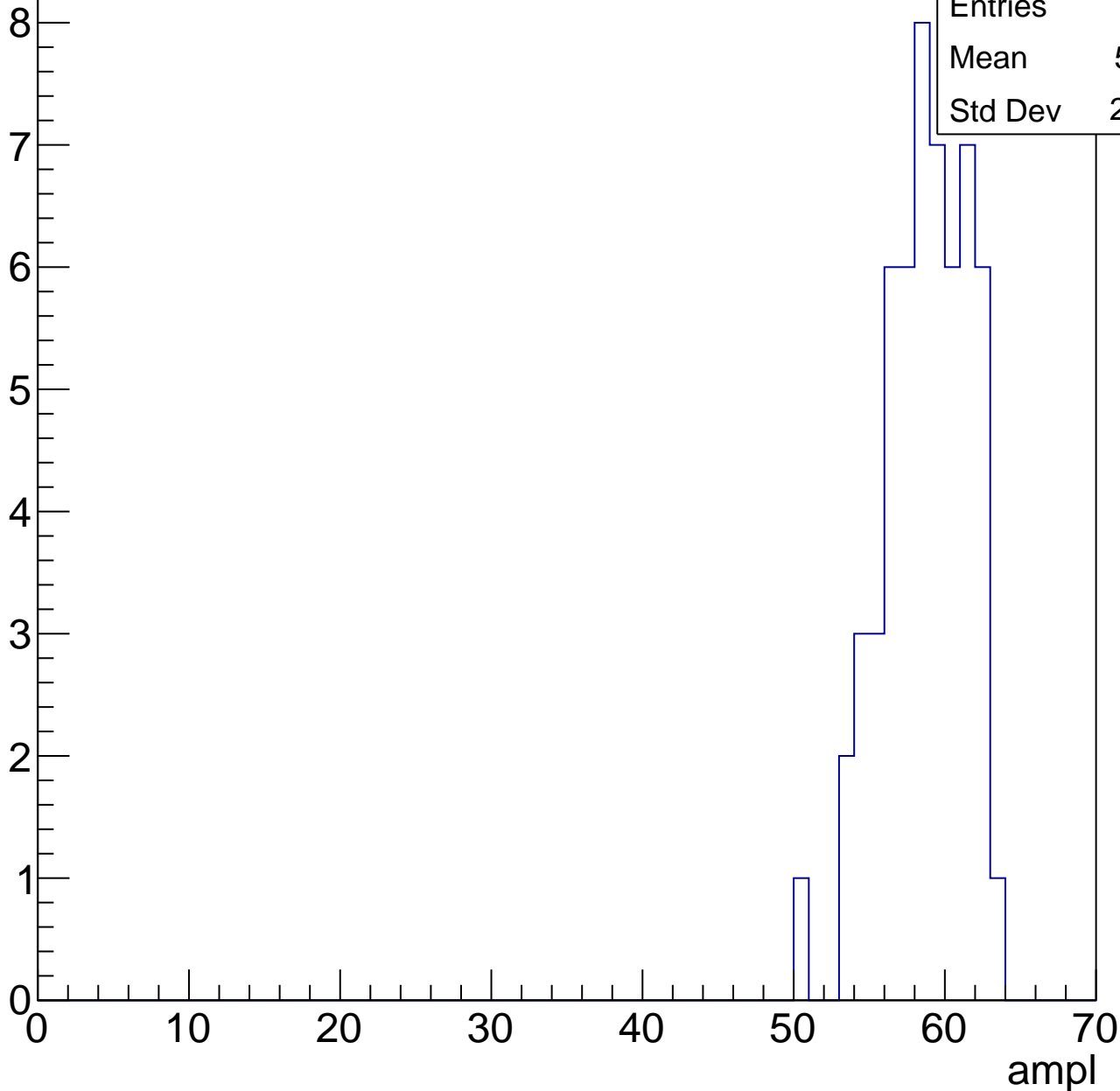


# B1L103S, U3-ch38, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	56
Mean	58.21
Std Dev	2.776

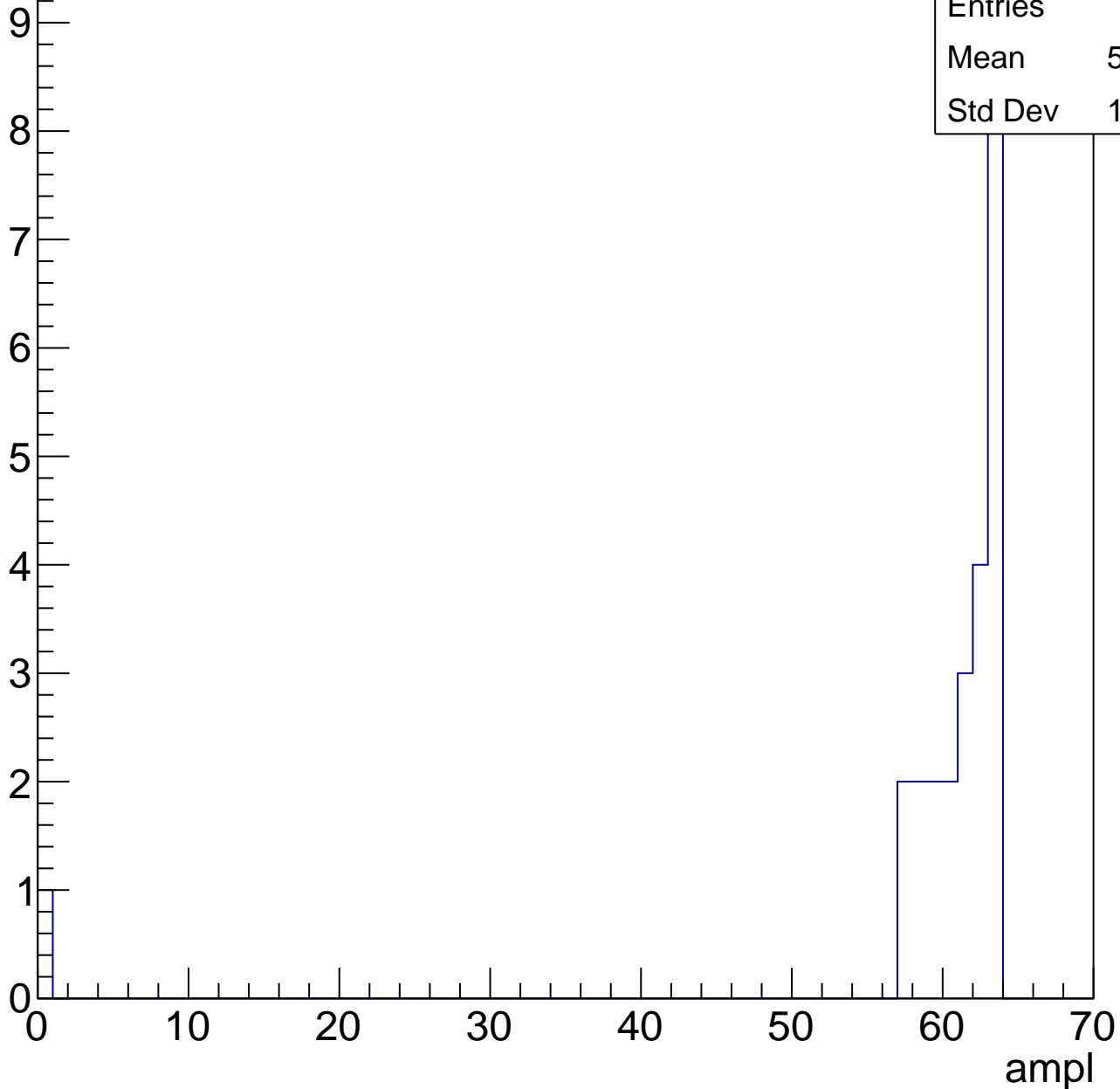


# B1L103S, U3-ch38, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	25
Mean	58.64
Std Dev	12.14





# B1L103S, U3-ch38, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	19
Mean	0
Std Dev	0

ampl

# B1L103S, U3-ch39, adc0

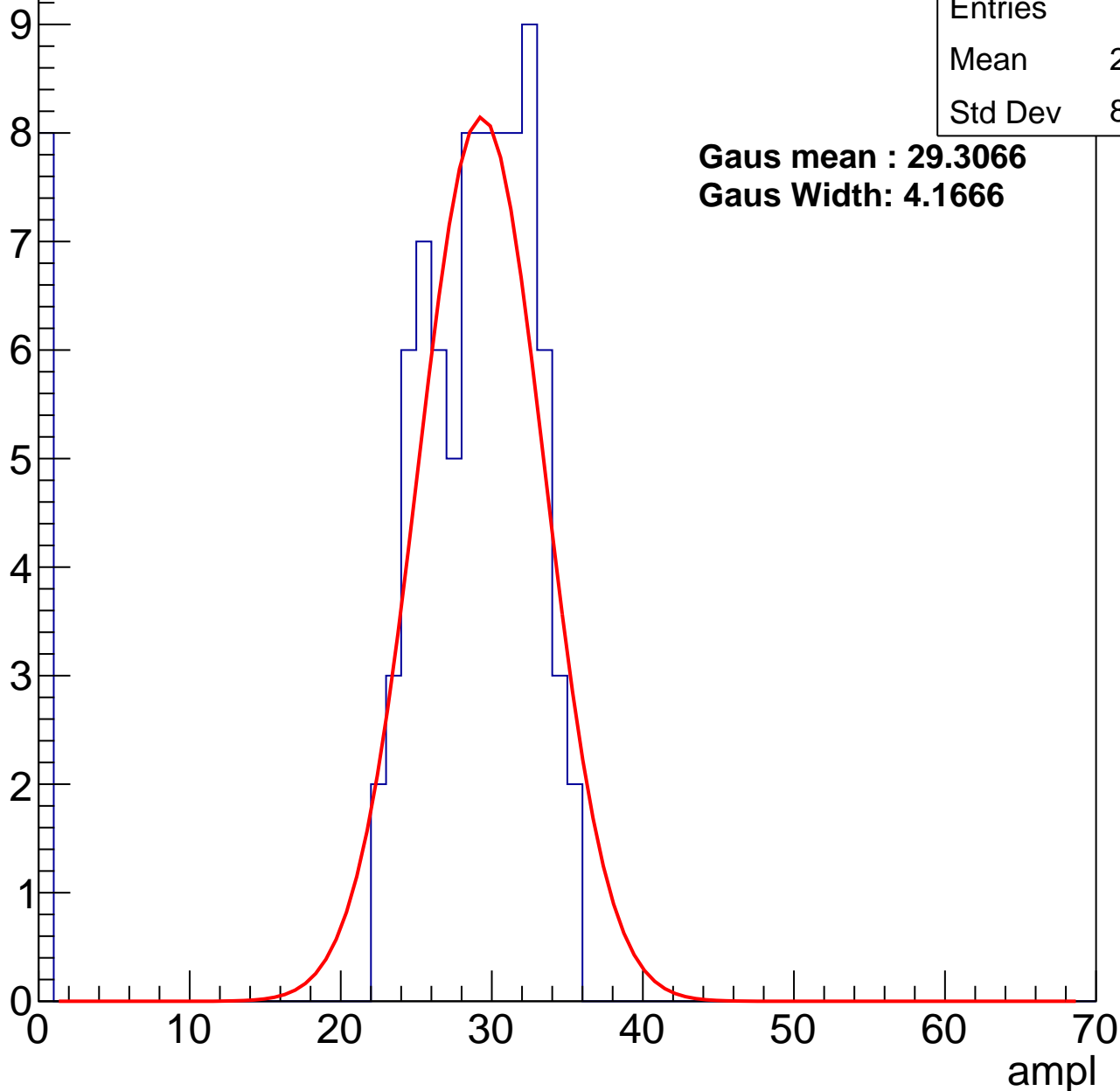
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	89
Mean	26.12
Std Dev	8.809

**Gaus mean : 29.3066**

**Gaus Width: 4.1666**



# B1L103S, U3-ch39, adc1

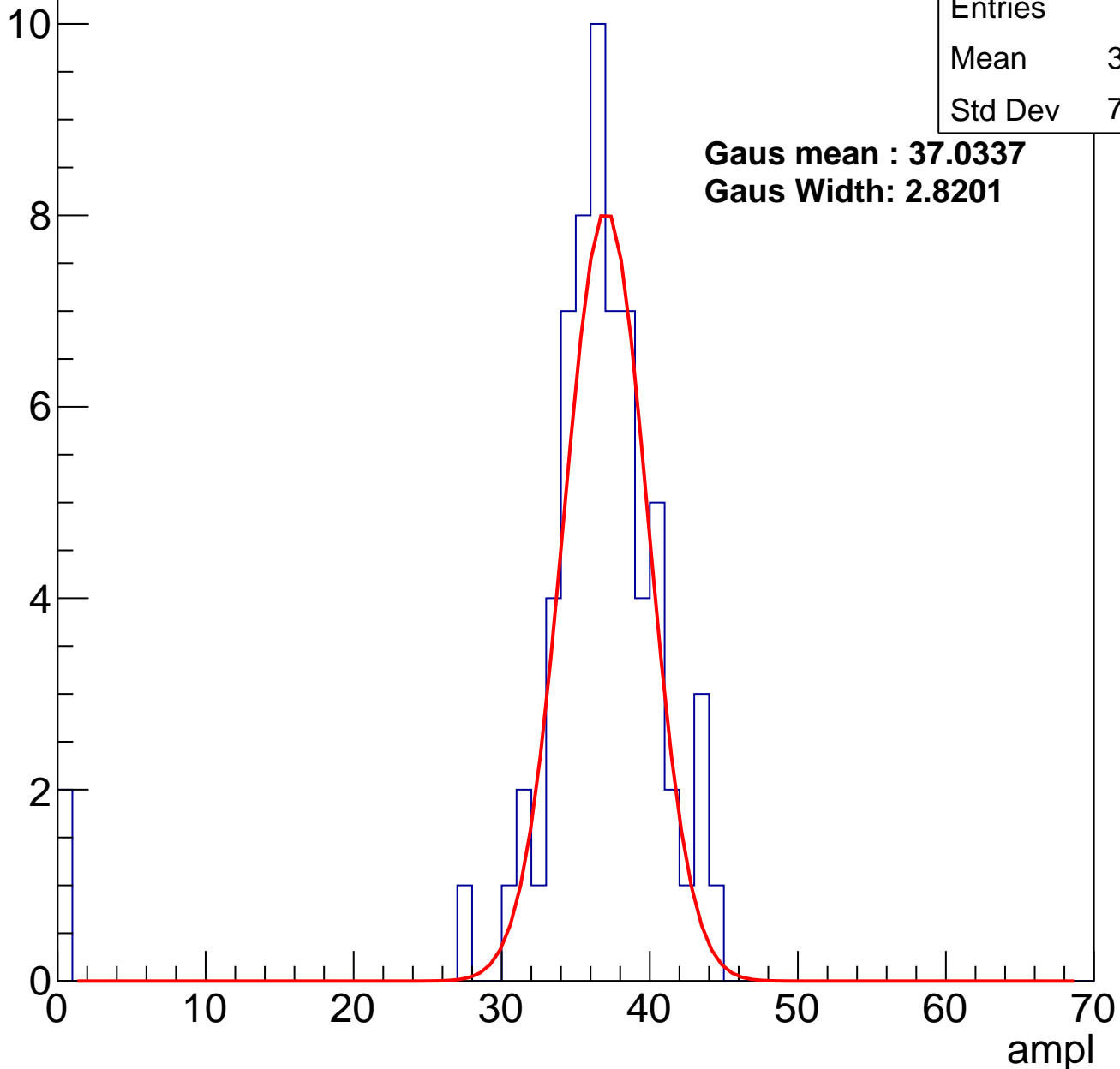
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	66
Mean	35.44
Std Dev	7.043

**Gaus mean : 37.0337**

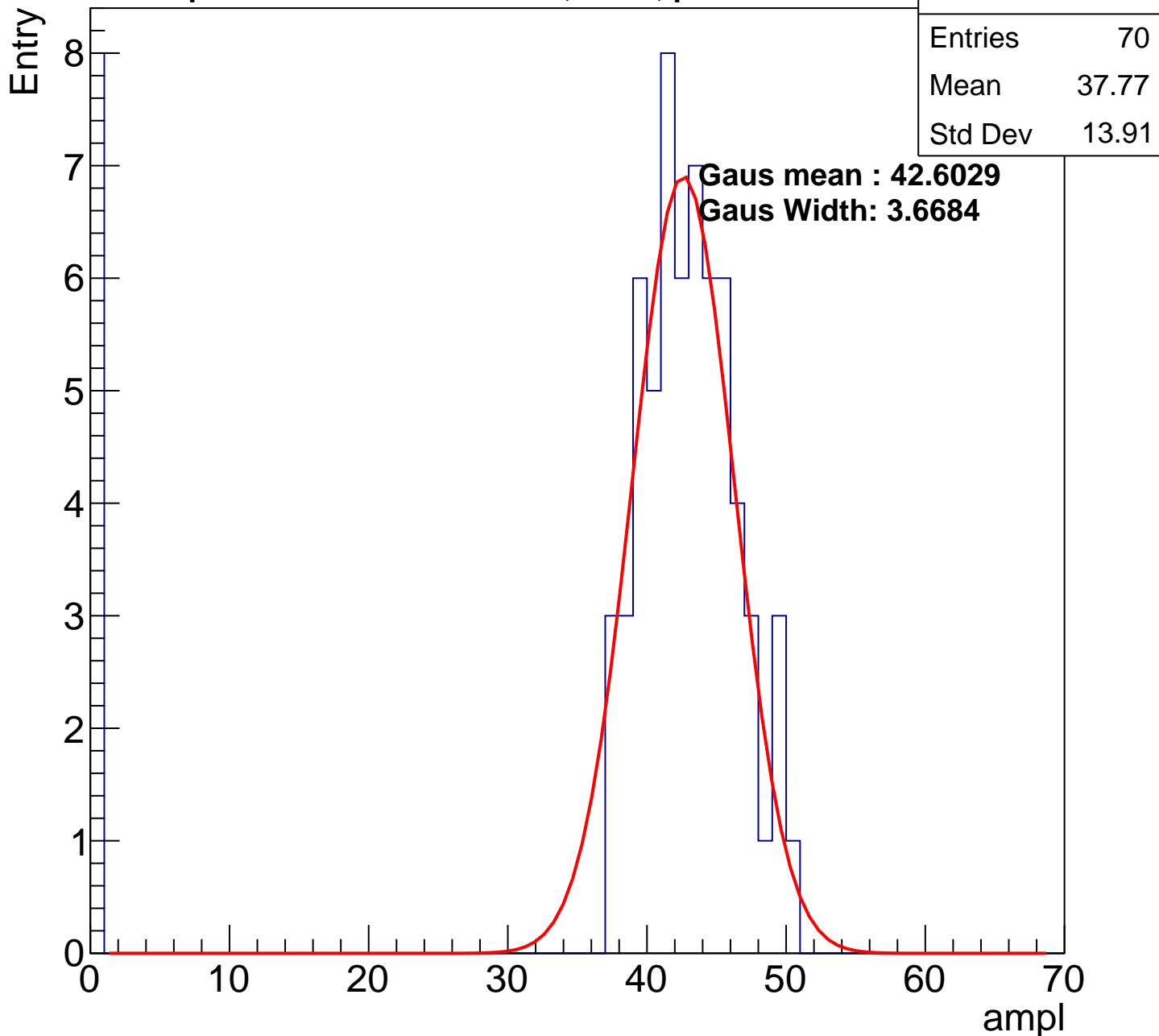
**Gaus Width: 2.8201**

Entry



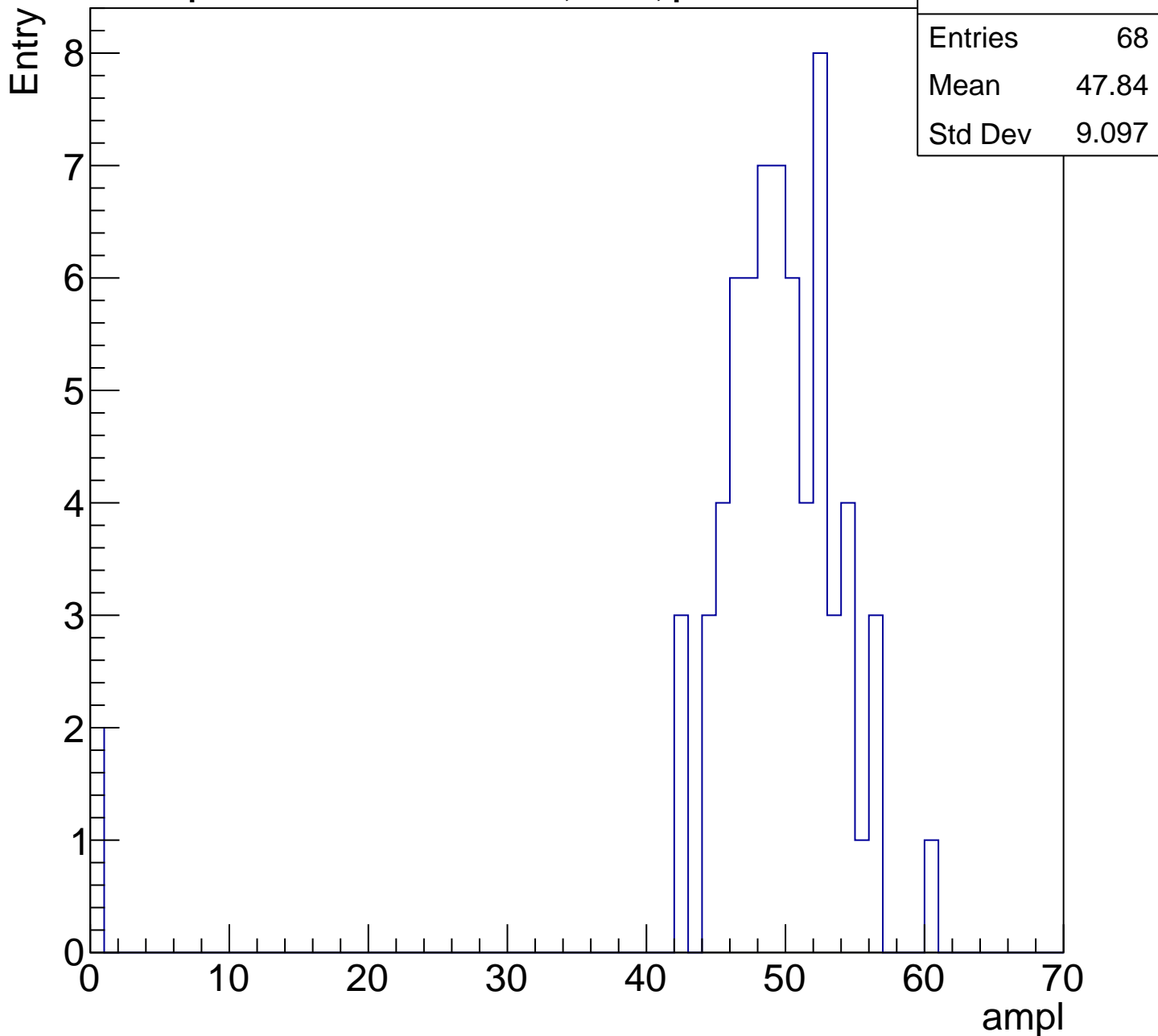
# B1L103S, U3-ch39, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U3-ch39, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

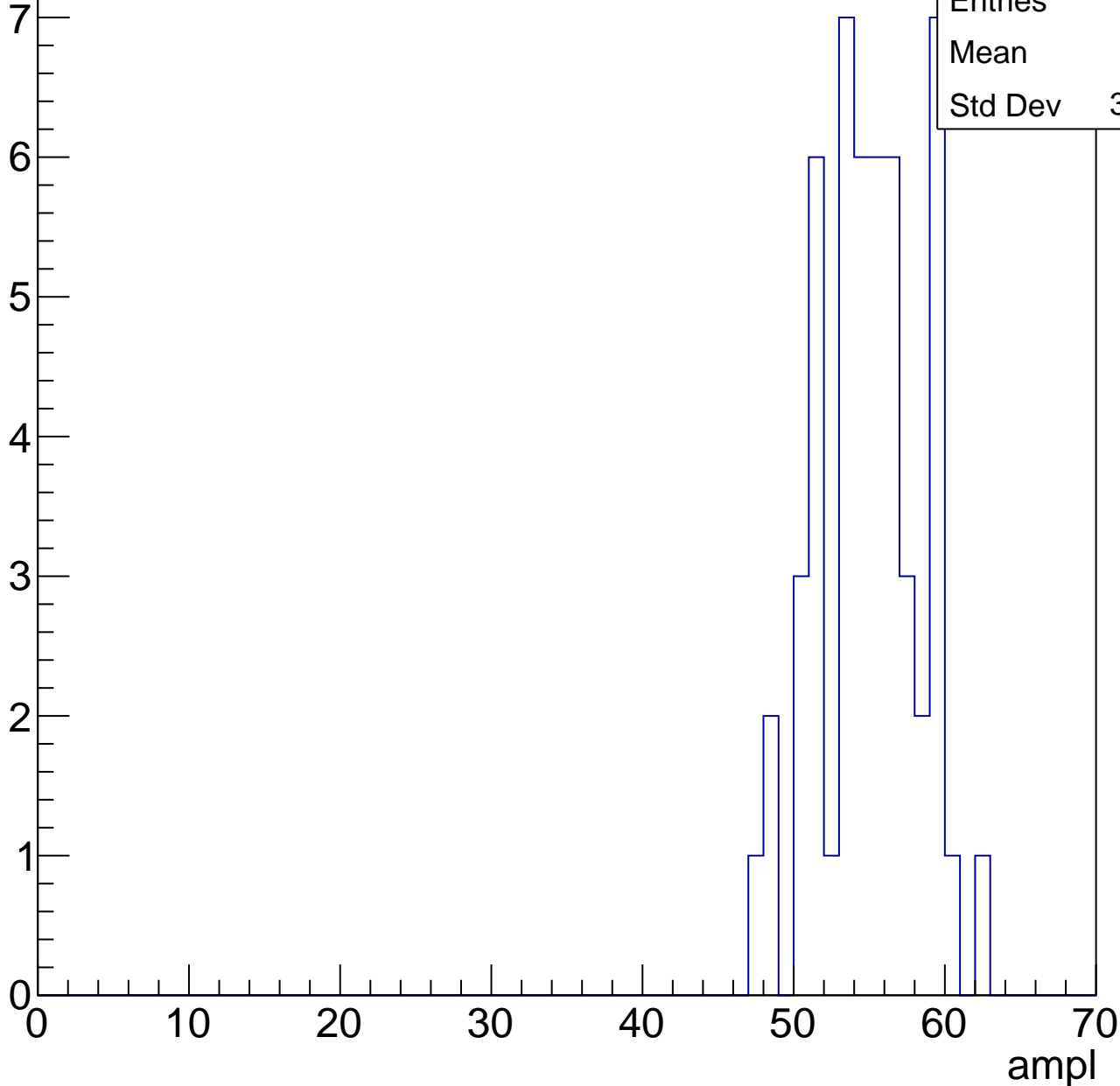


# B1L103S, U3-ch39, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	52
Mean	54.5
Std Dev	3.354

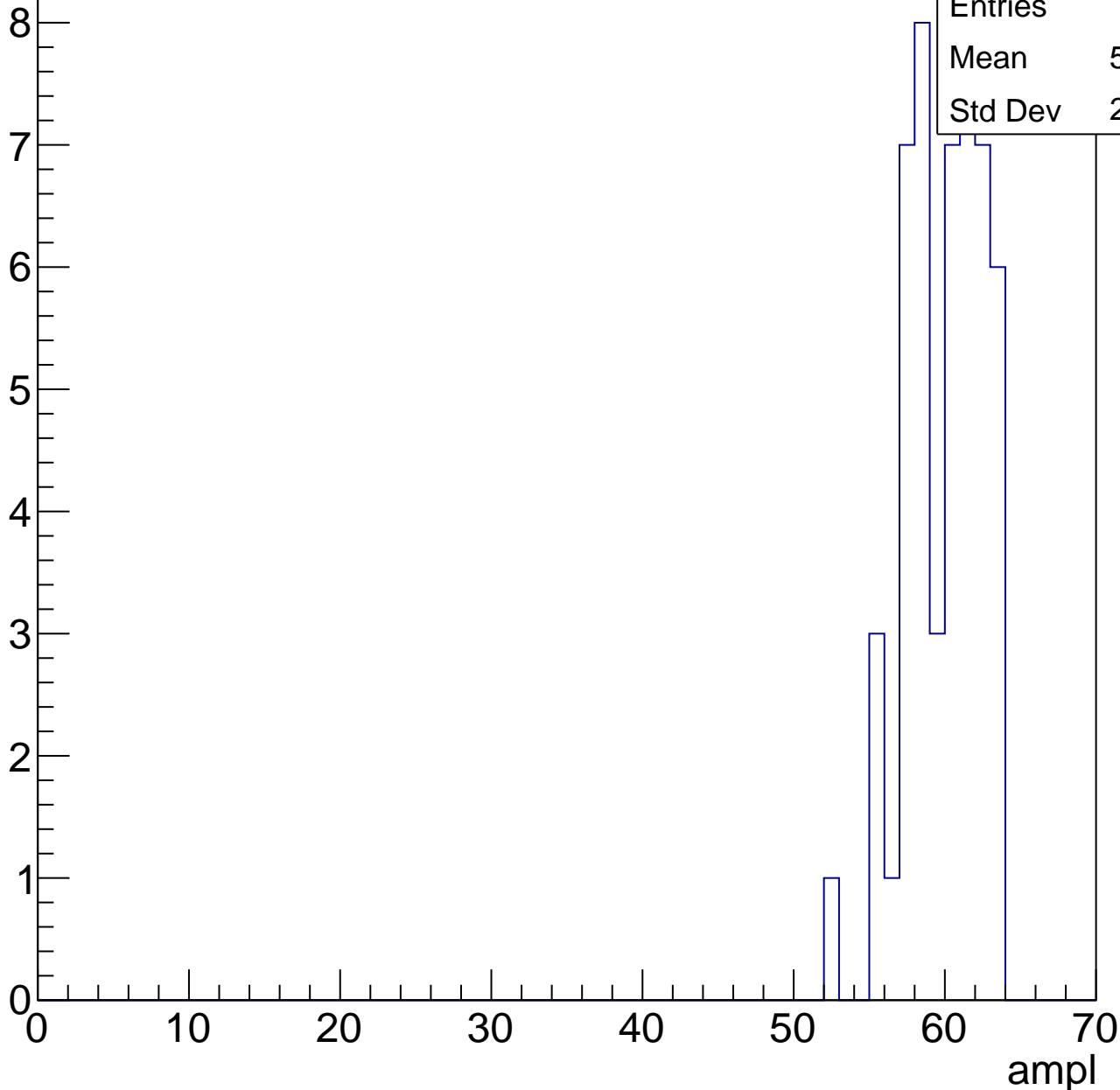


# B1L103S, U3-ch39, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

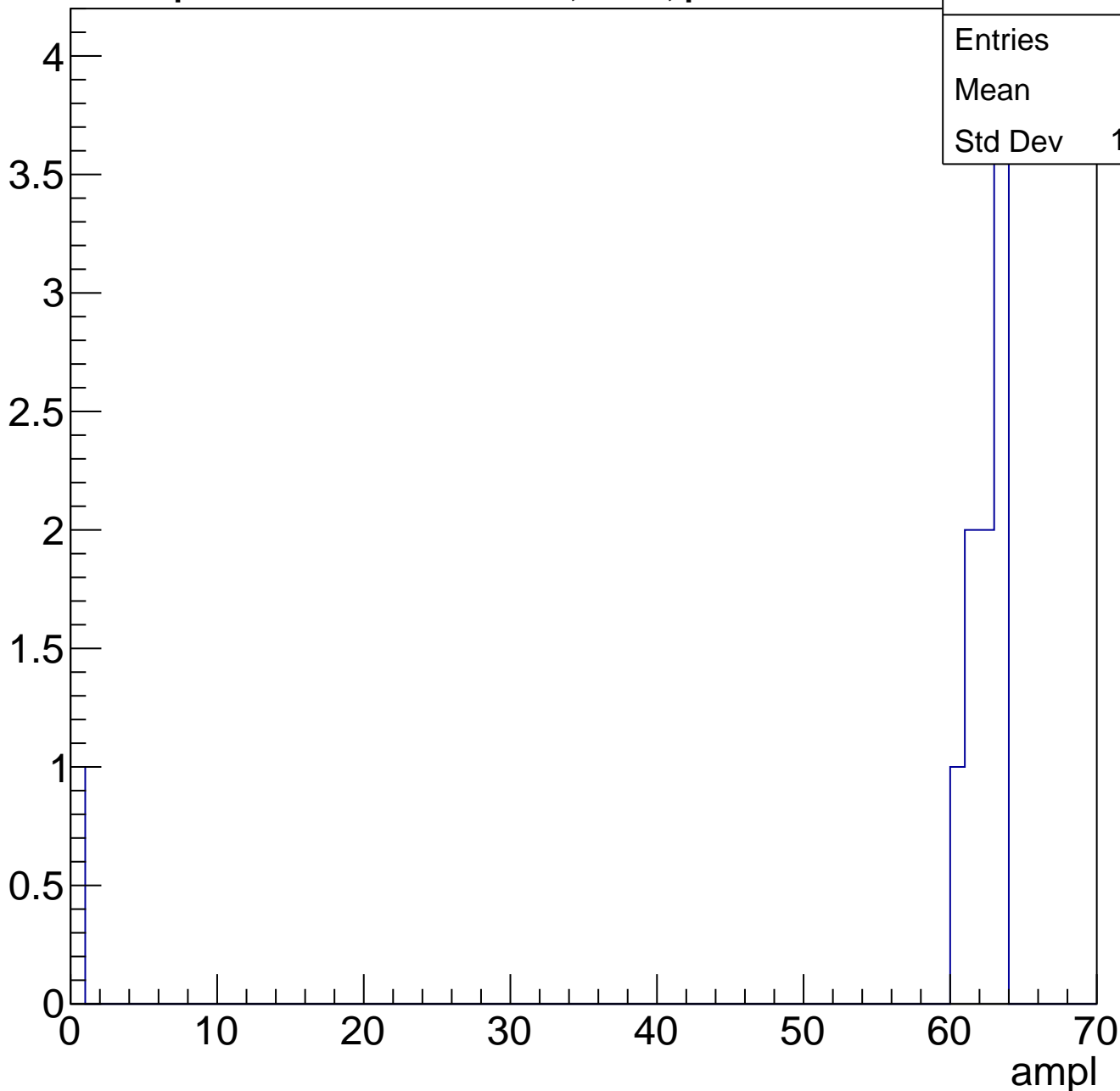
Entries	51
Mean	59.47
Std Dev	2.539



# B1L103S, U3-ch39, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

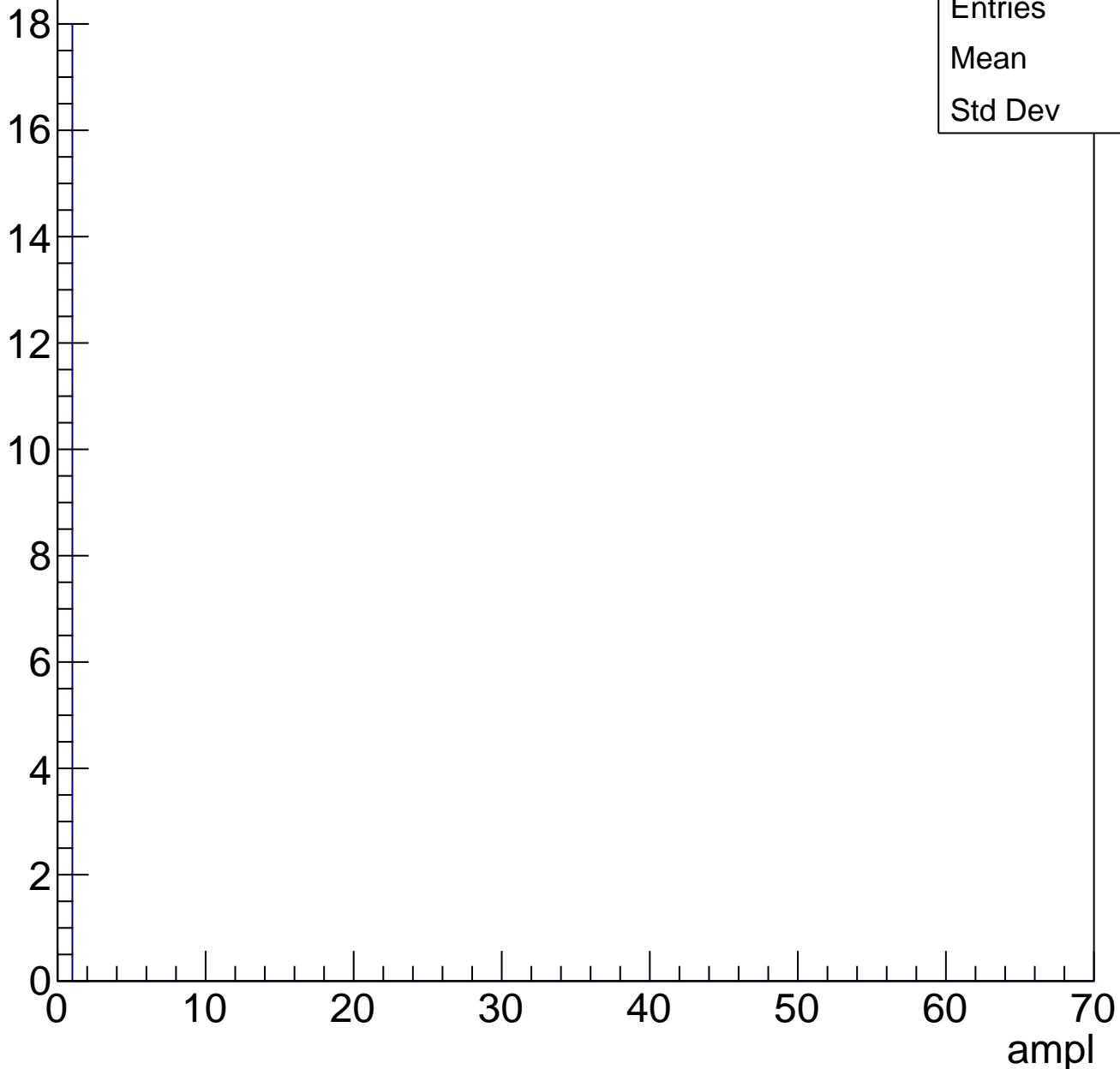




# B1L103S, U3-ch39, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	18
Mean	0
Std Dev	0

# B1L103S, U3-ch40, adc0

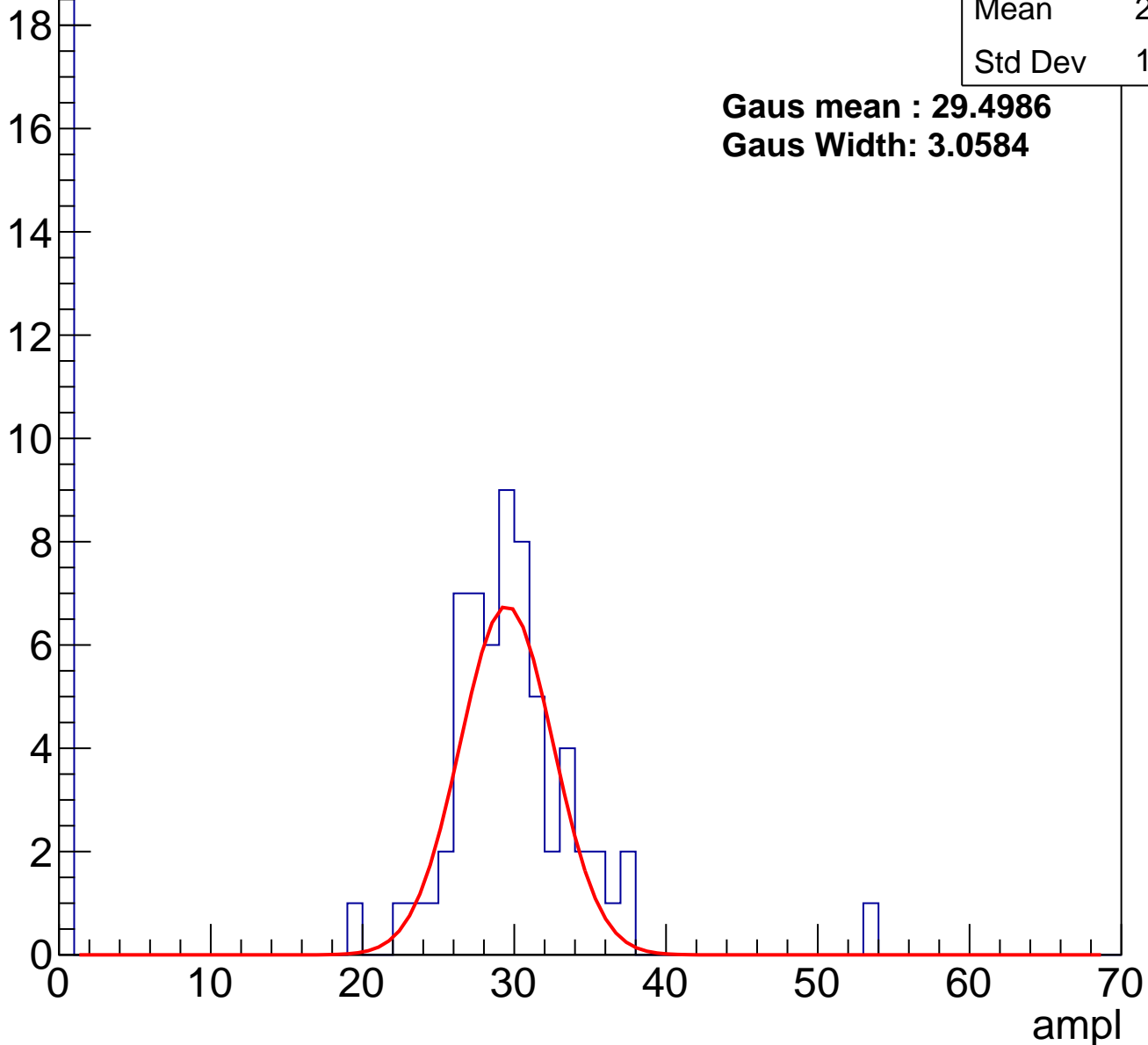
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	81
Mean	22.59
Std Dev	13.14

**Gaus mean : 29.4986**

**Gaus Width: 3.0584**

Entry



# B1L103S, U3-ch40, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	87
Mean	30.26
Std Dev	13.25

**Gaus mean : 36.3962**

**Gaus Width: 3.7850**

Entry

12

10

8

6

4

2

0

0

10

20

30

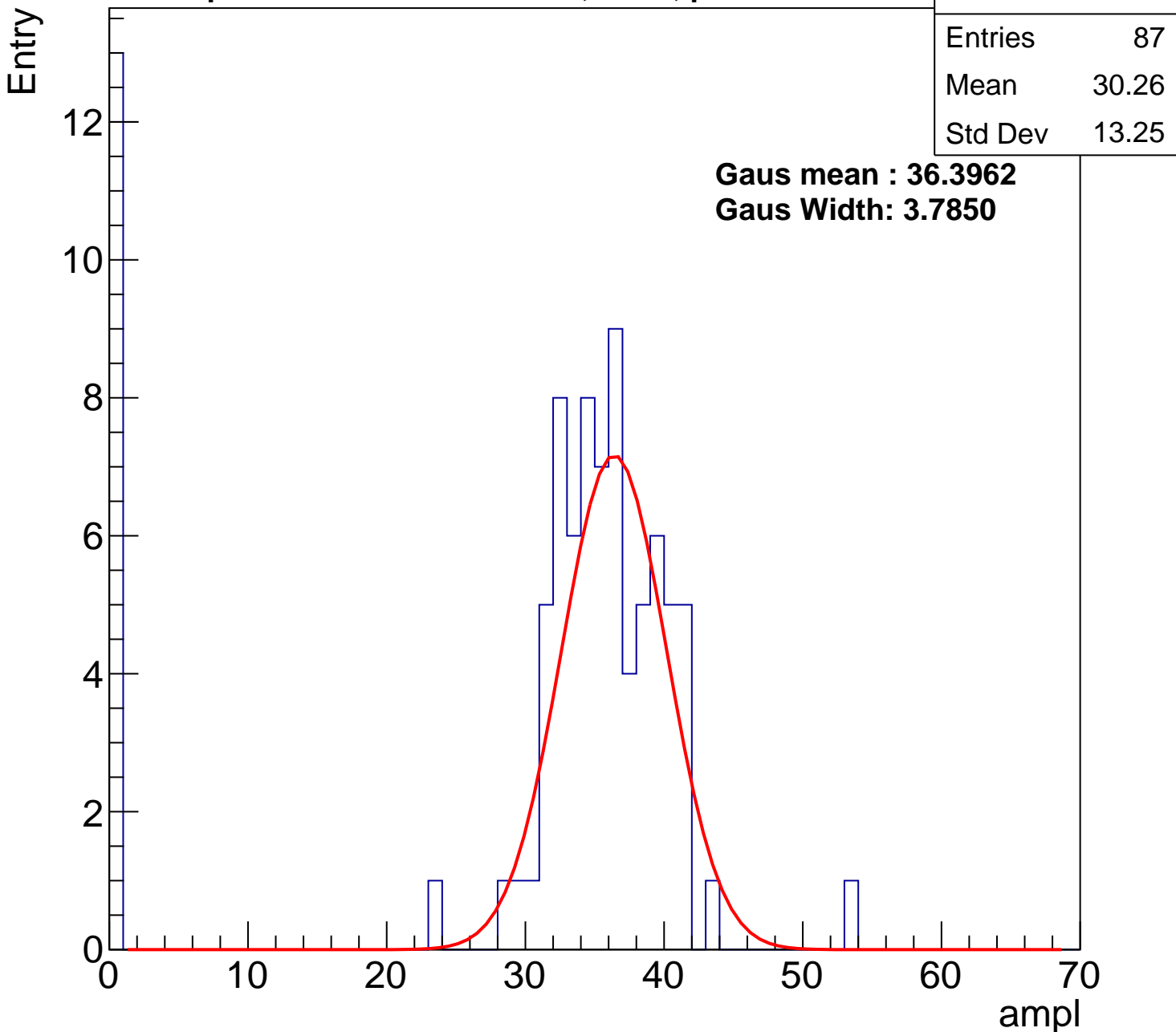
40

50

60

70

ampl



# B1L103S, U3-ch40, adc2

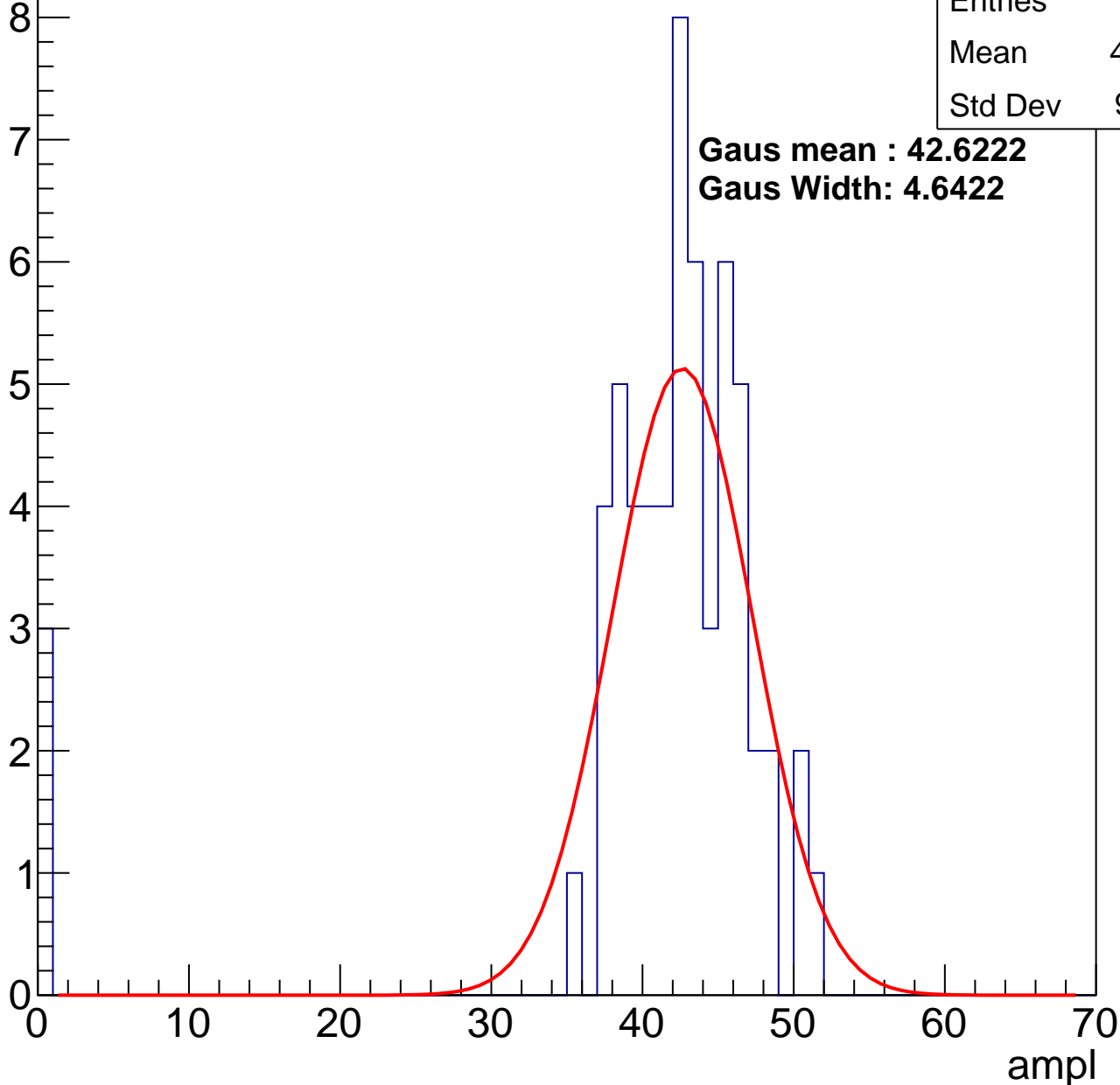
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	60
Mean	40.33
Std Dev	9.911

**Gaus mean : 42.6222**

**Gaus Width: 4.6422**

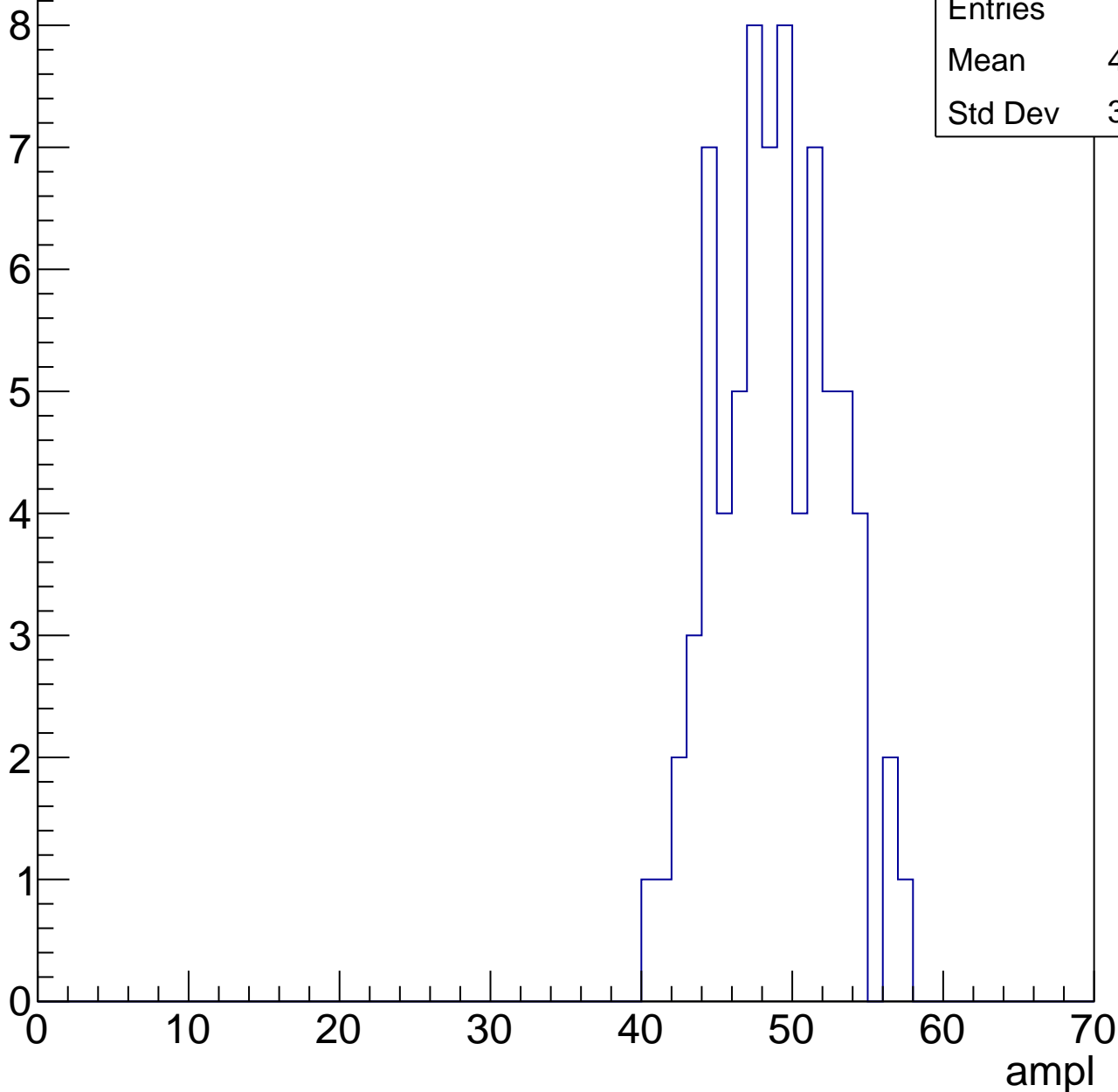


# B1L103S, U3-ch40, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

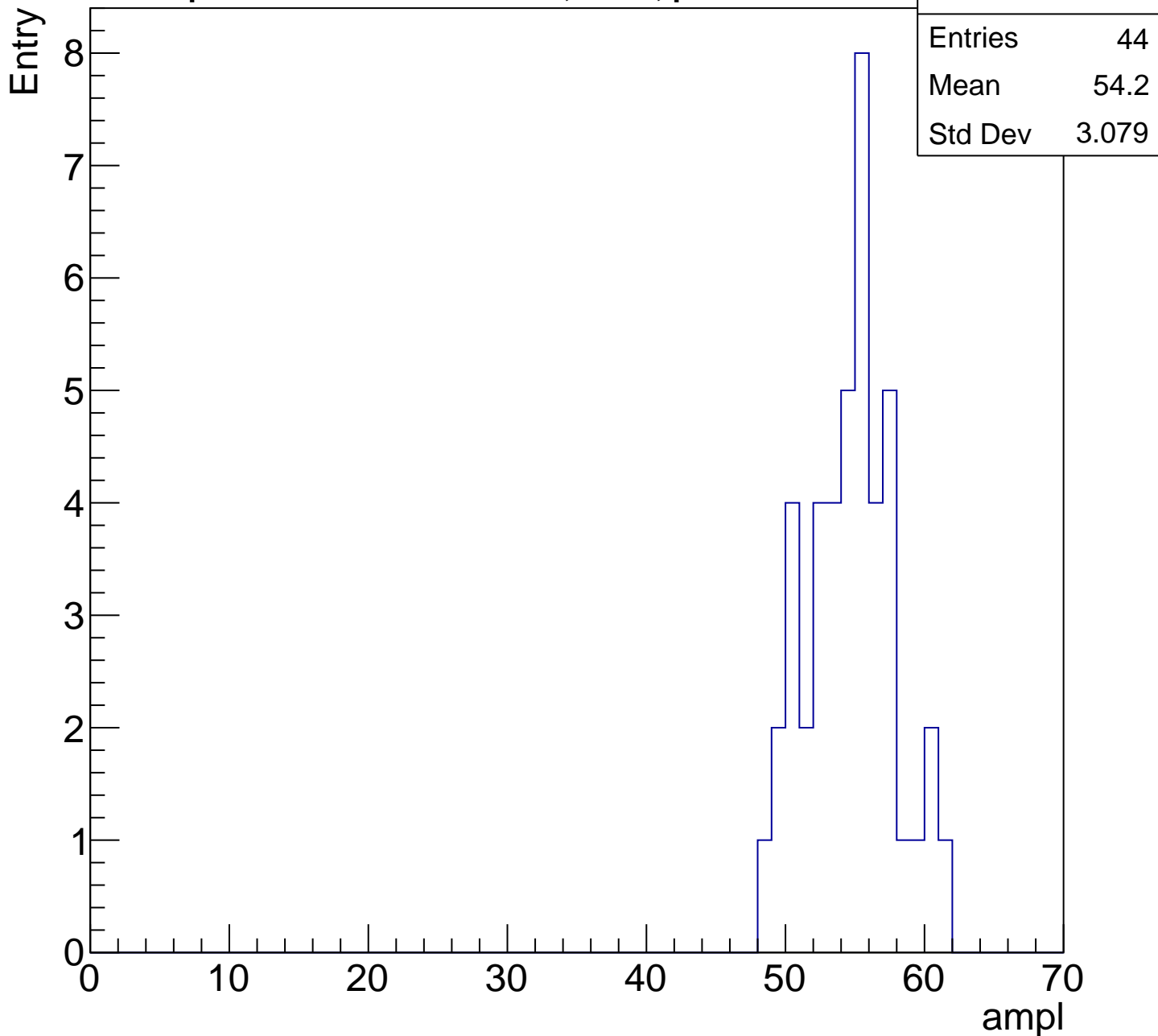
Entry

Entries	74
Mean	48.42
Std Dev	3.799



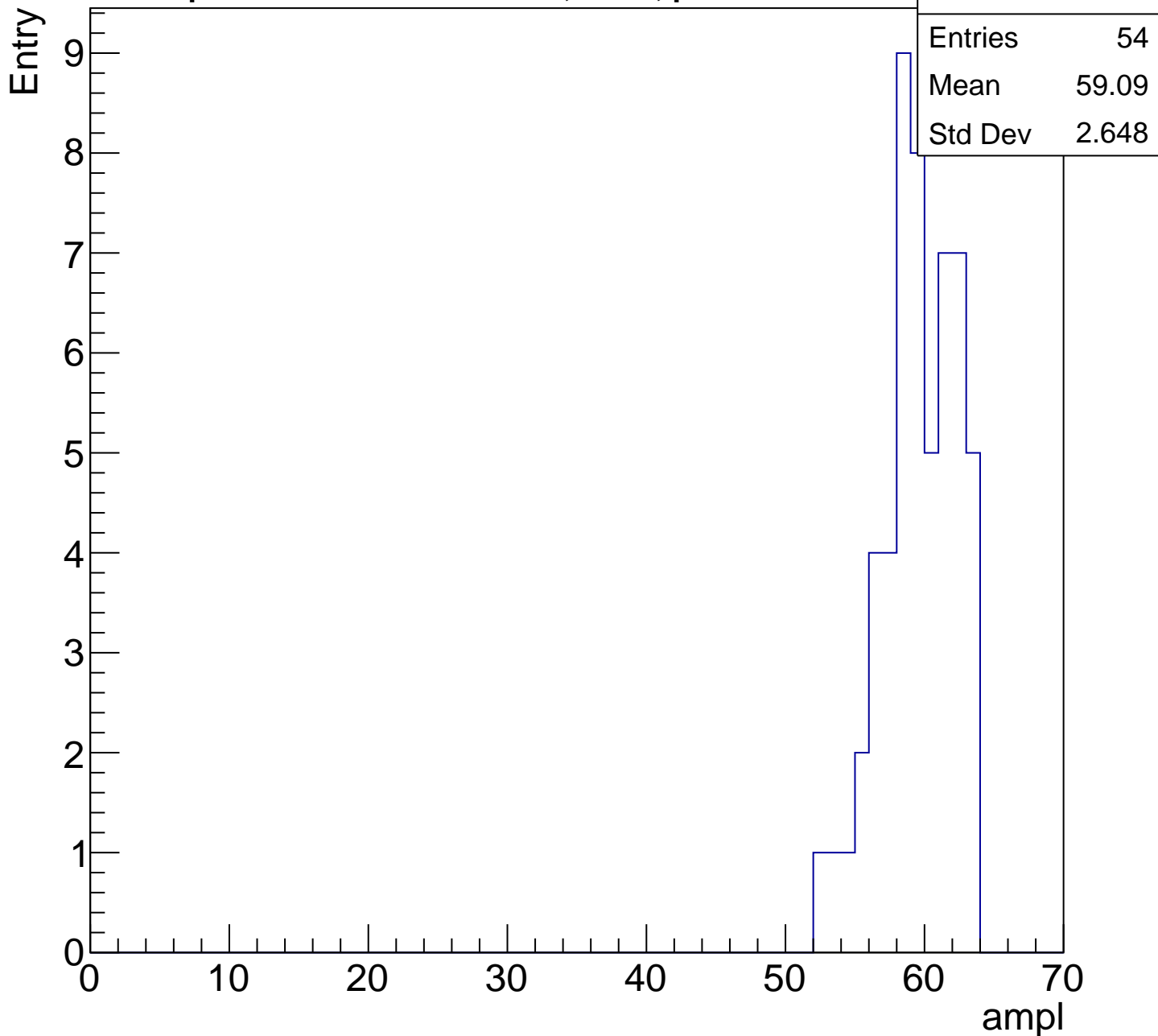
# B1L103S, U3-ch40, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U3-ch40, adc5

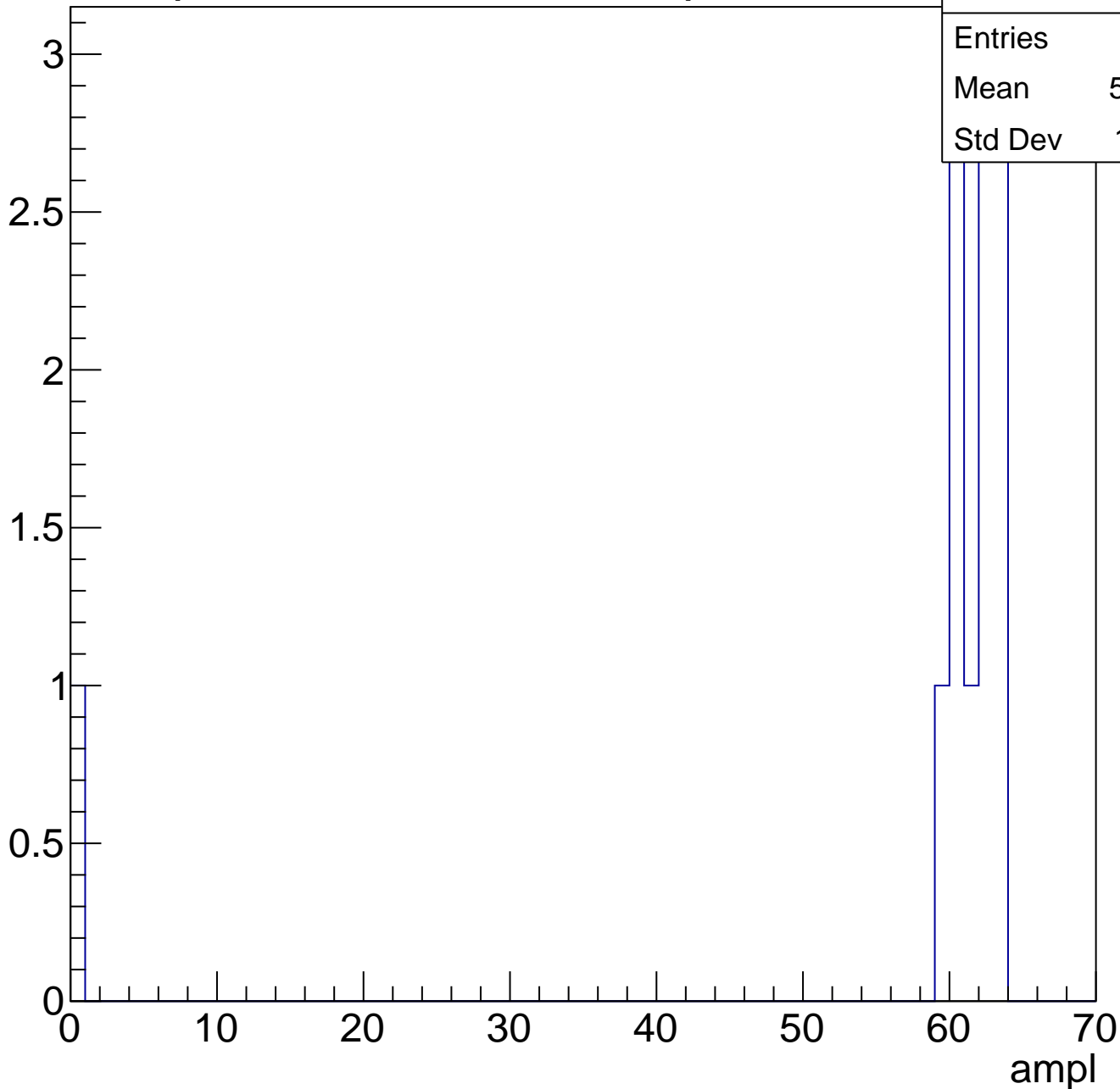
calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U3-ch40, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

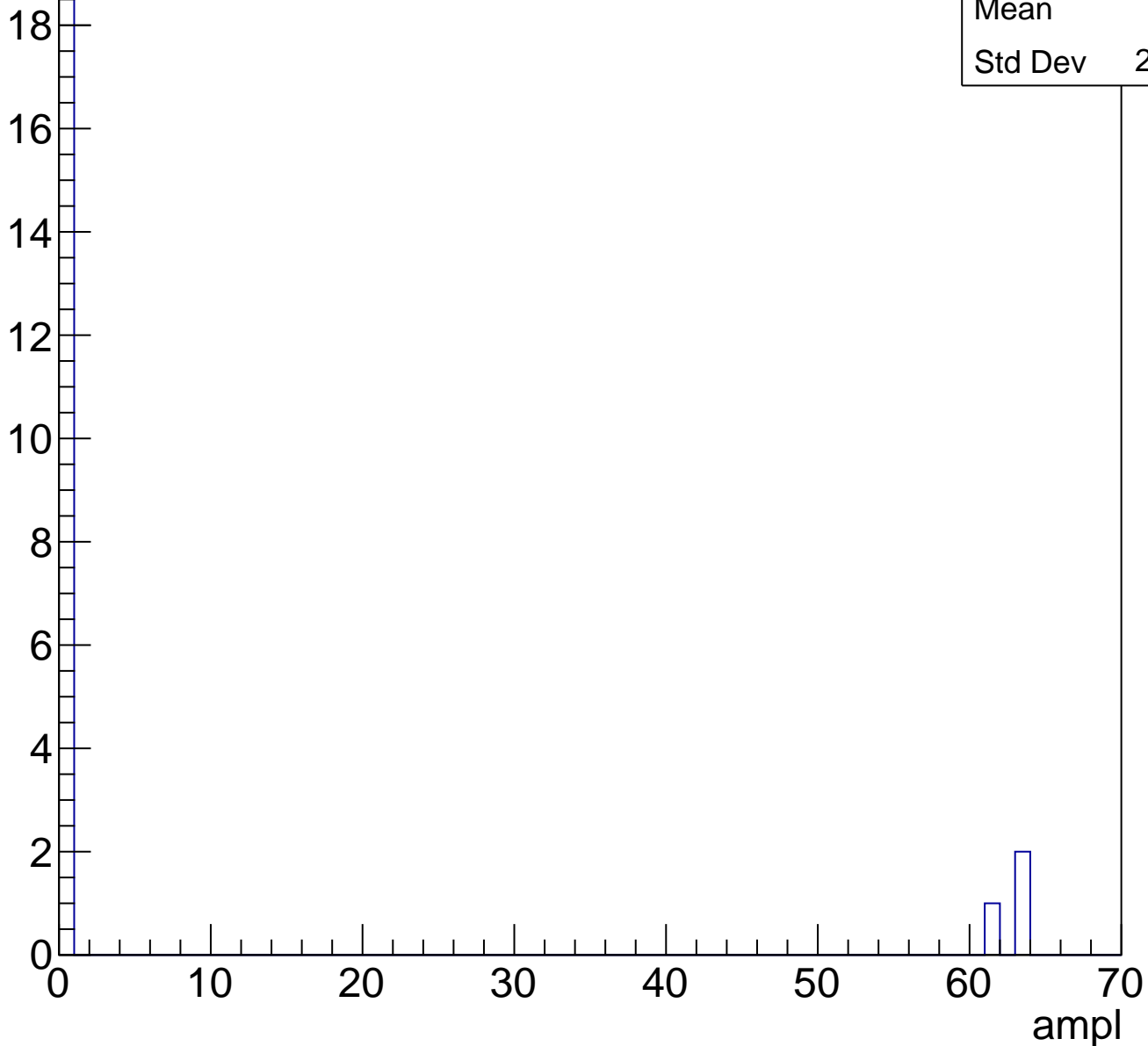




# B1L103S, U3-ch40, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	22
Mean	8.5
Std Dev	21.39

# B1L103S, U3-ch41, adc0

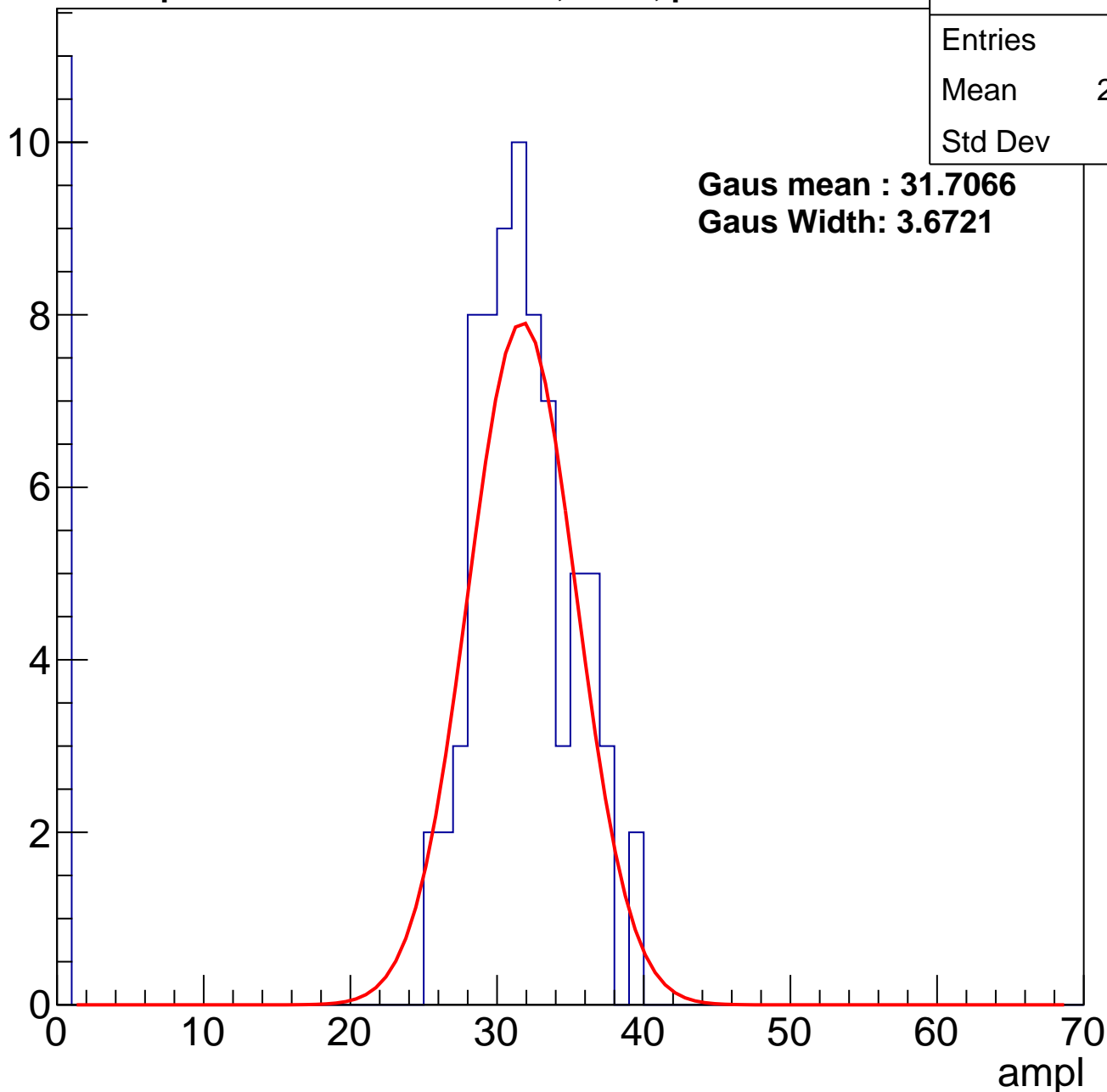
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	86
Mean	27.35
Std Dev	10.9

**Gaus mean : 31.7066**

**Gaus Width: 3.6721**

Entry



# B1L103S, U3-ch41, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	74
Mean	32.12
Std Dev	13.79

**Gaus mean : 37.9553**

**Gaus Width: 4.1992**

Entry

10

8

6

4

2

0

0

10

20

30

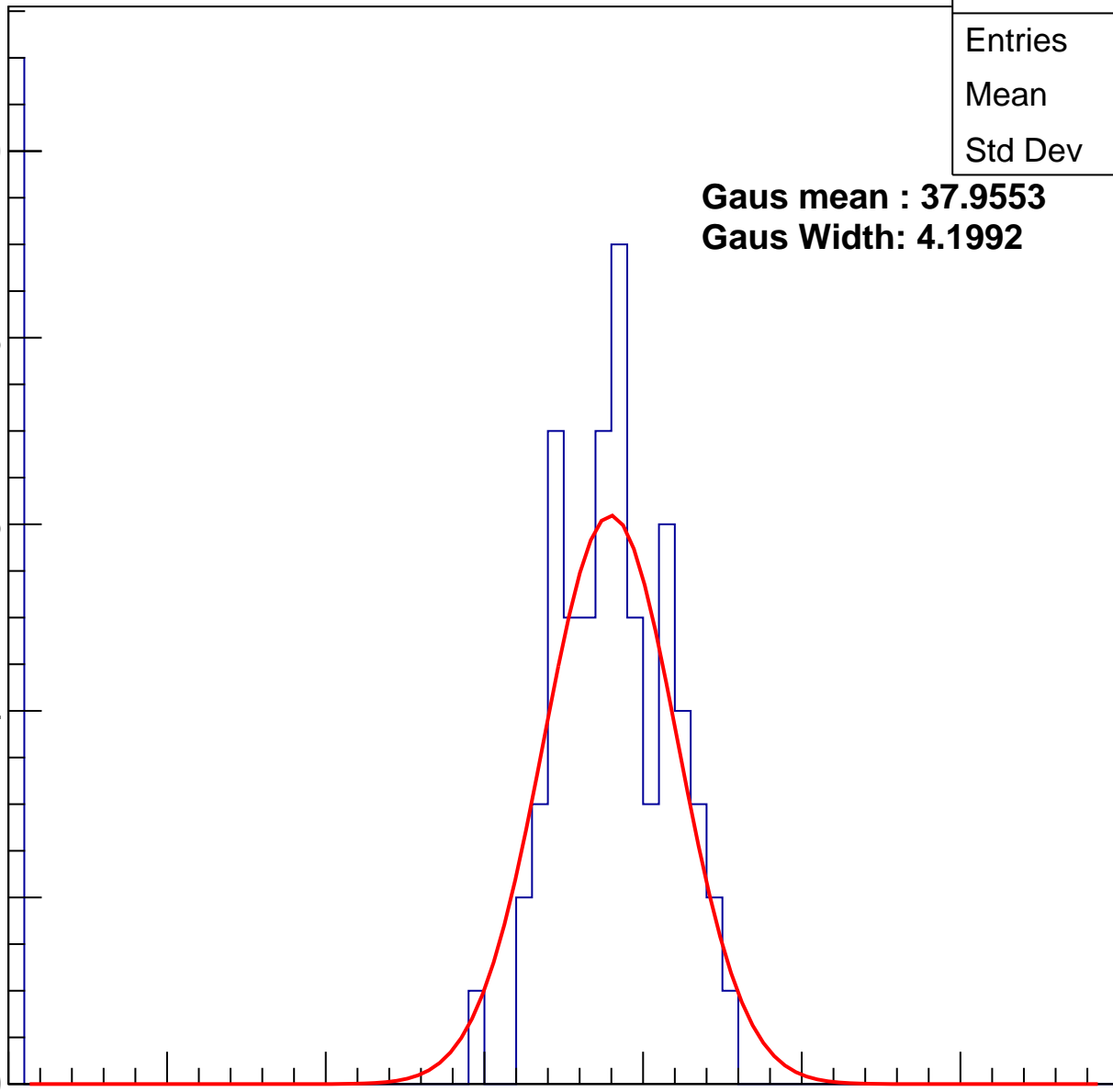
40

50

60

70

ampl



# B1L103S, U3-ch41, adc2

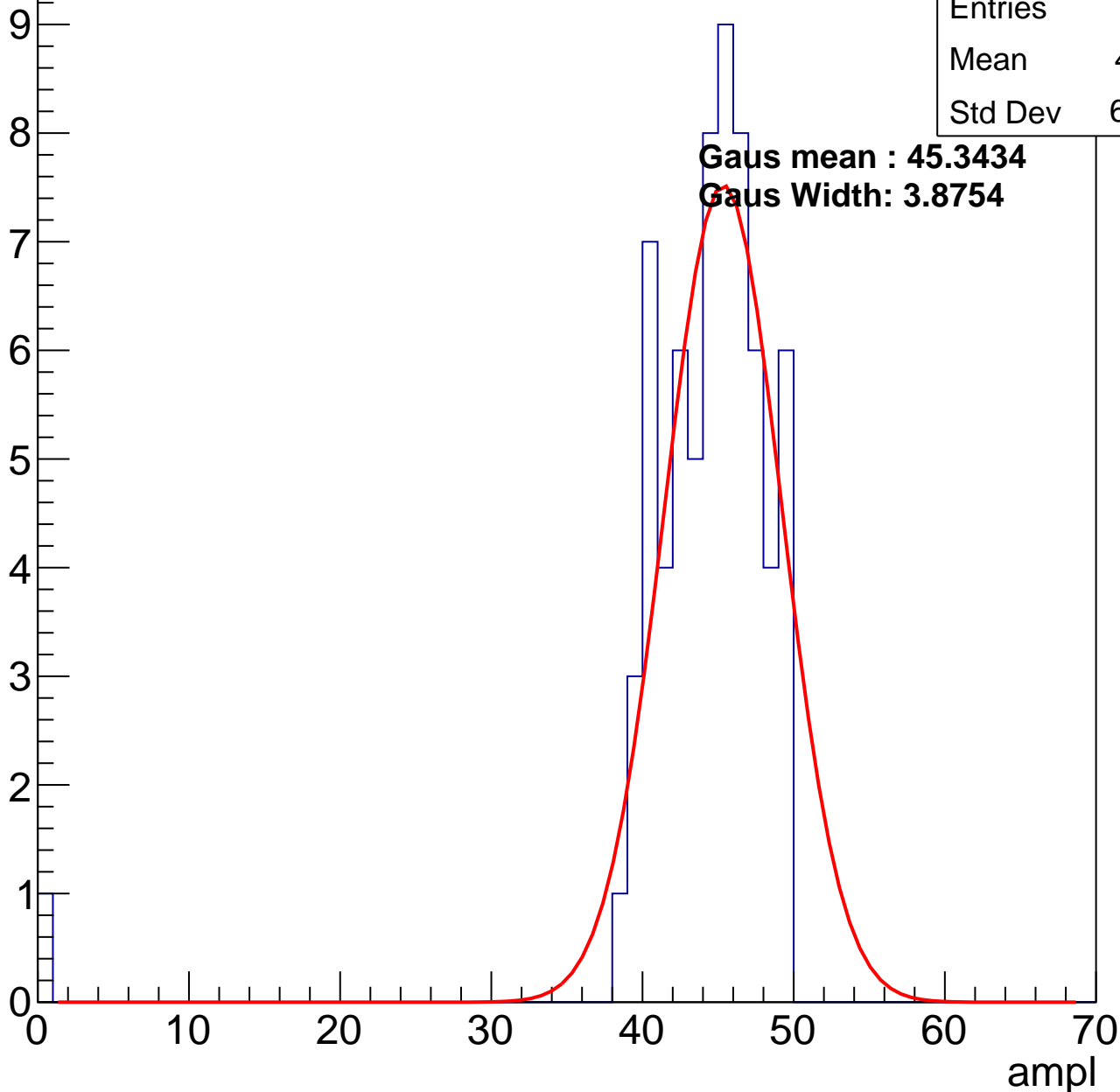
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	43.51
Std Dev	6.084

Gaus mean : 45.3434

Gaus Width: 3.8754

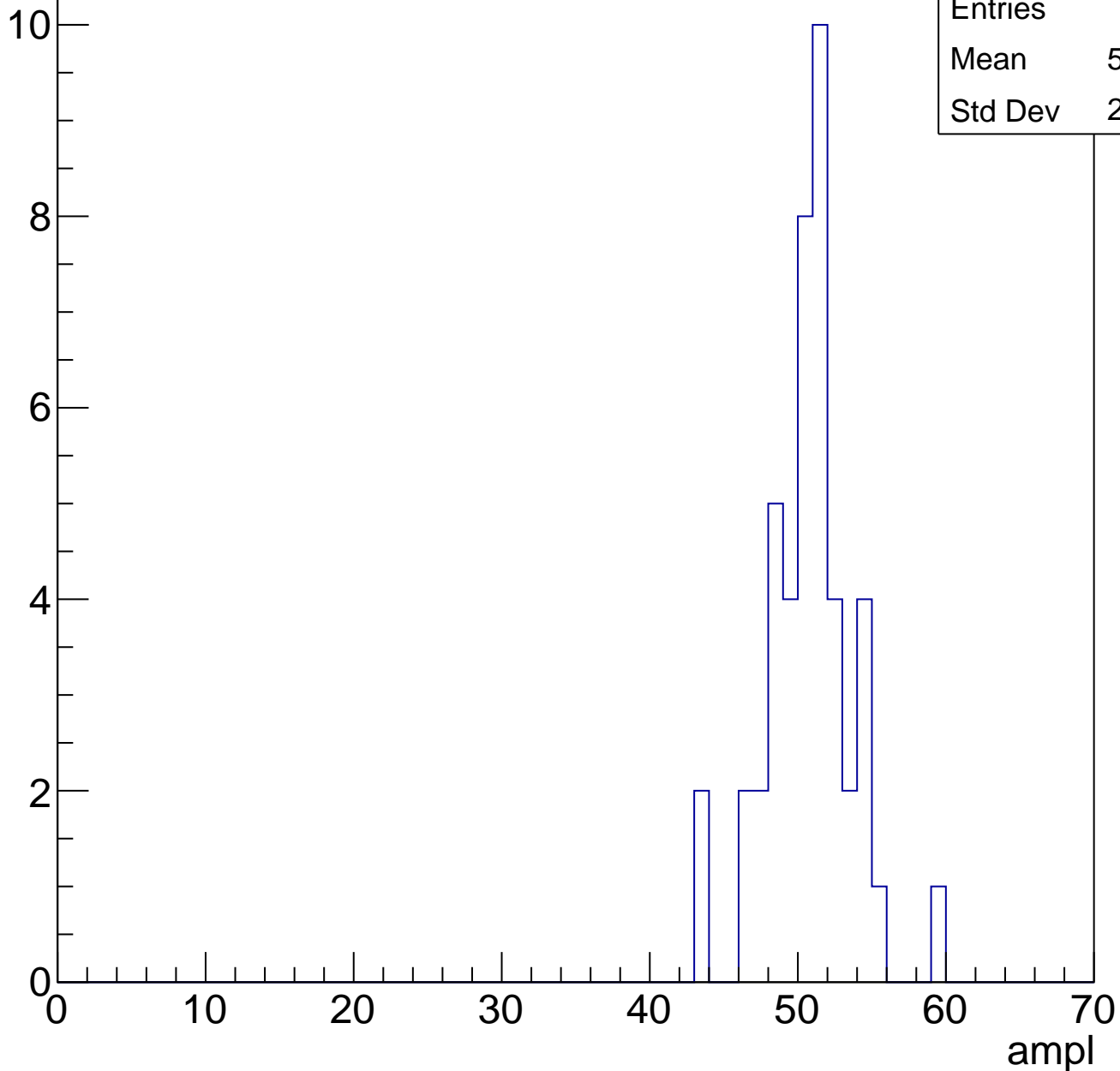


# B1L103S, U3-ch41, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

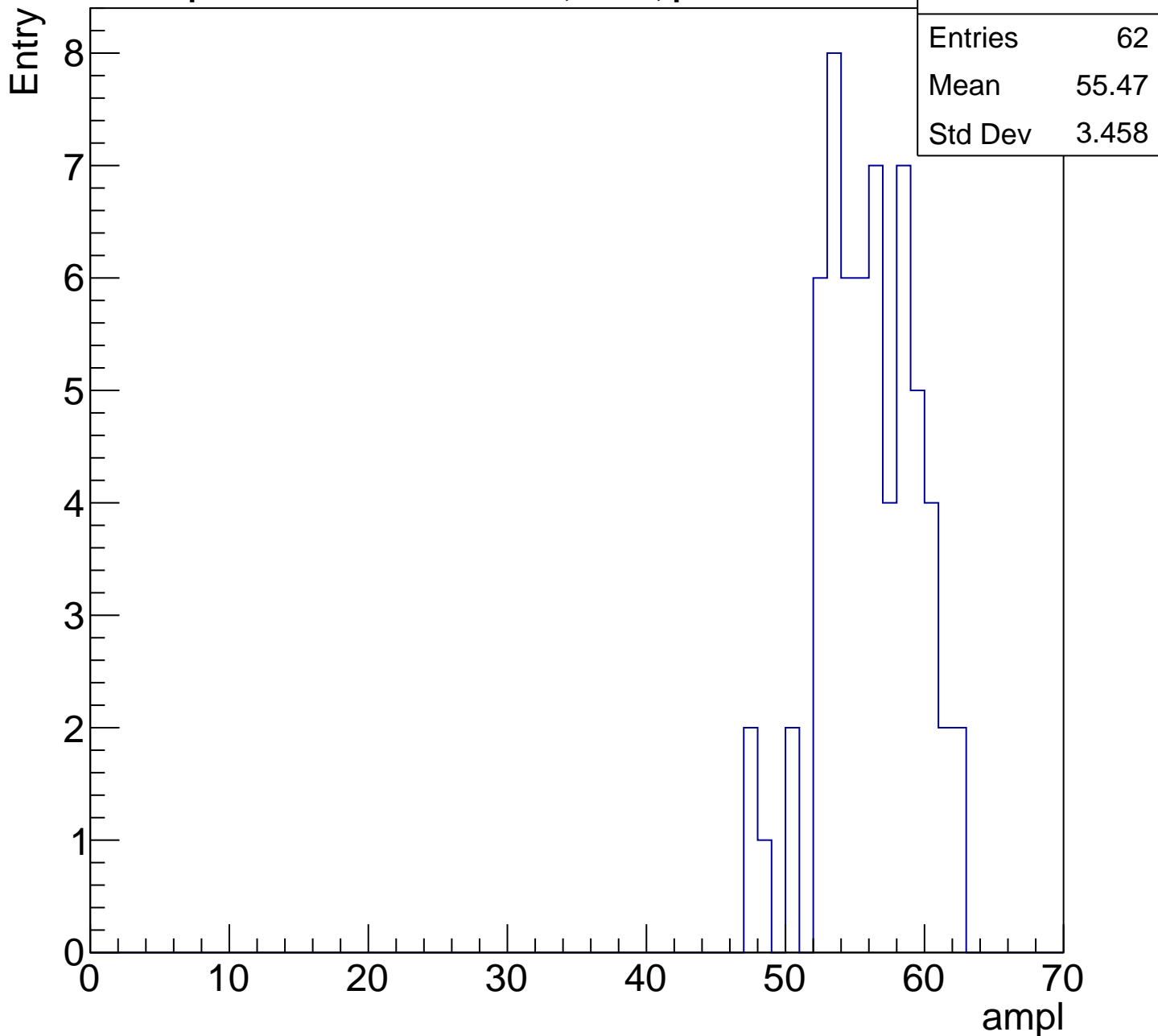
Entries	45
Mean	50.27
Std Dev	2.917

Entry



# B1L103S, U3-ch41, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

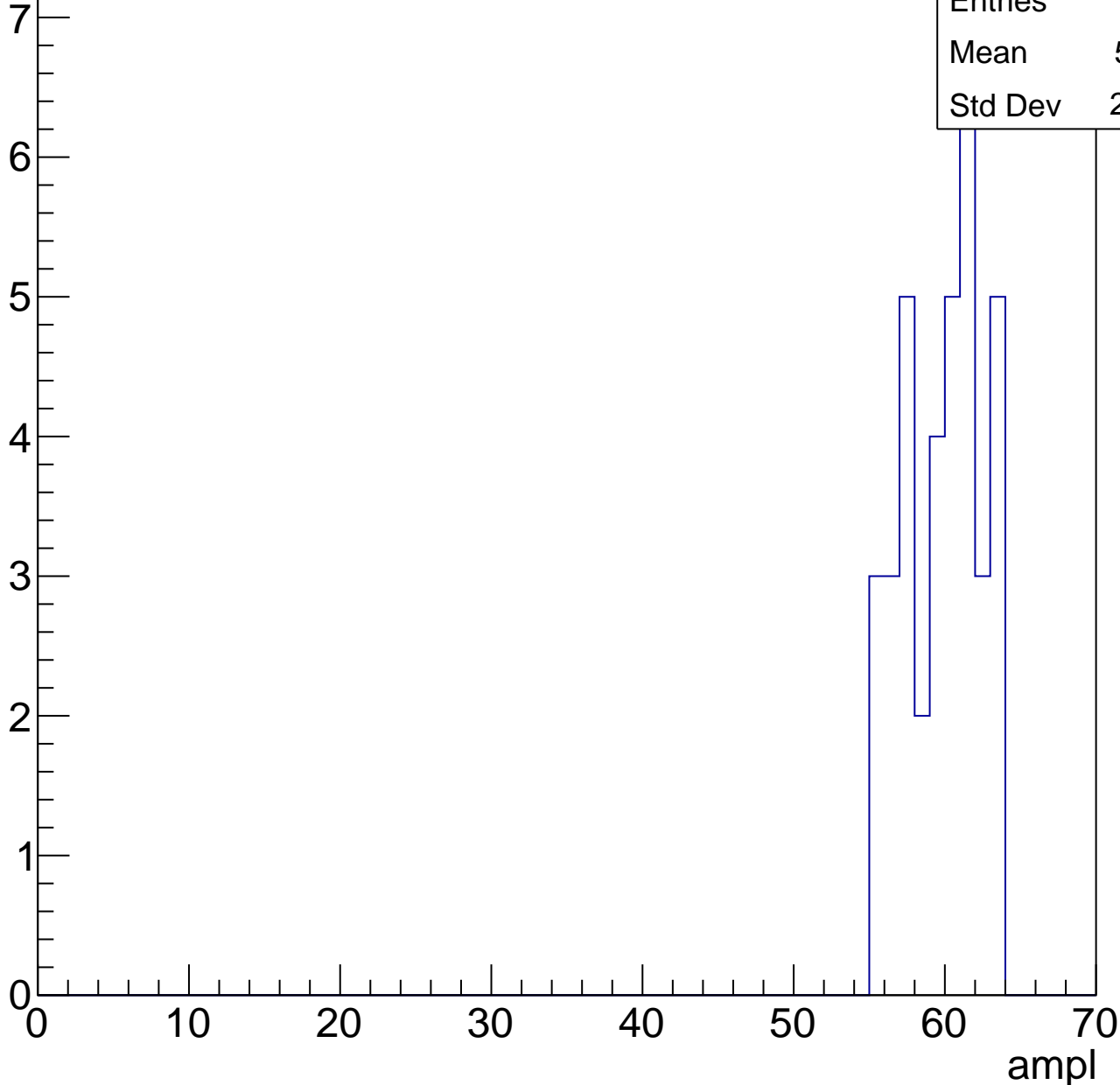


# B1L103S, U3-ch41, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	37
Mean	59.41
Std Dev	2.498

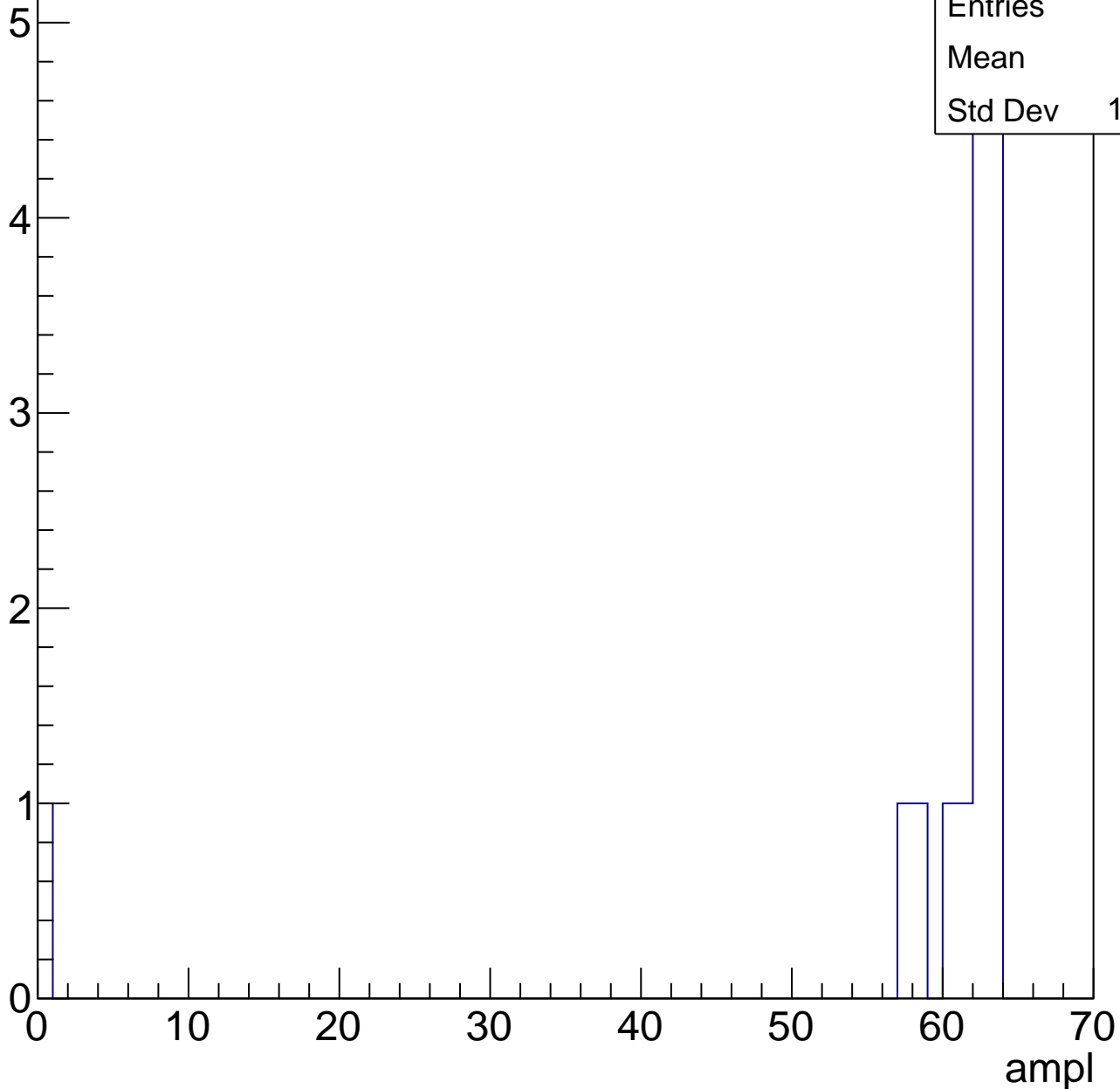


# B1L103S, U3-ch41, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	15
Mean	57.4
Std Dev	15.44





# B1L103S, U3-ch41, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	19
Mean	0
Std Dev	0

ampl

# B1L103S, U3-ch42, adc0

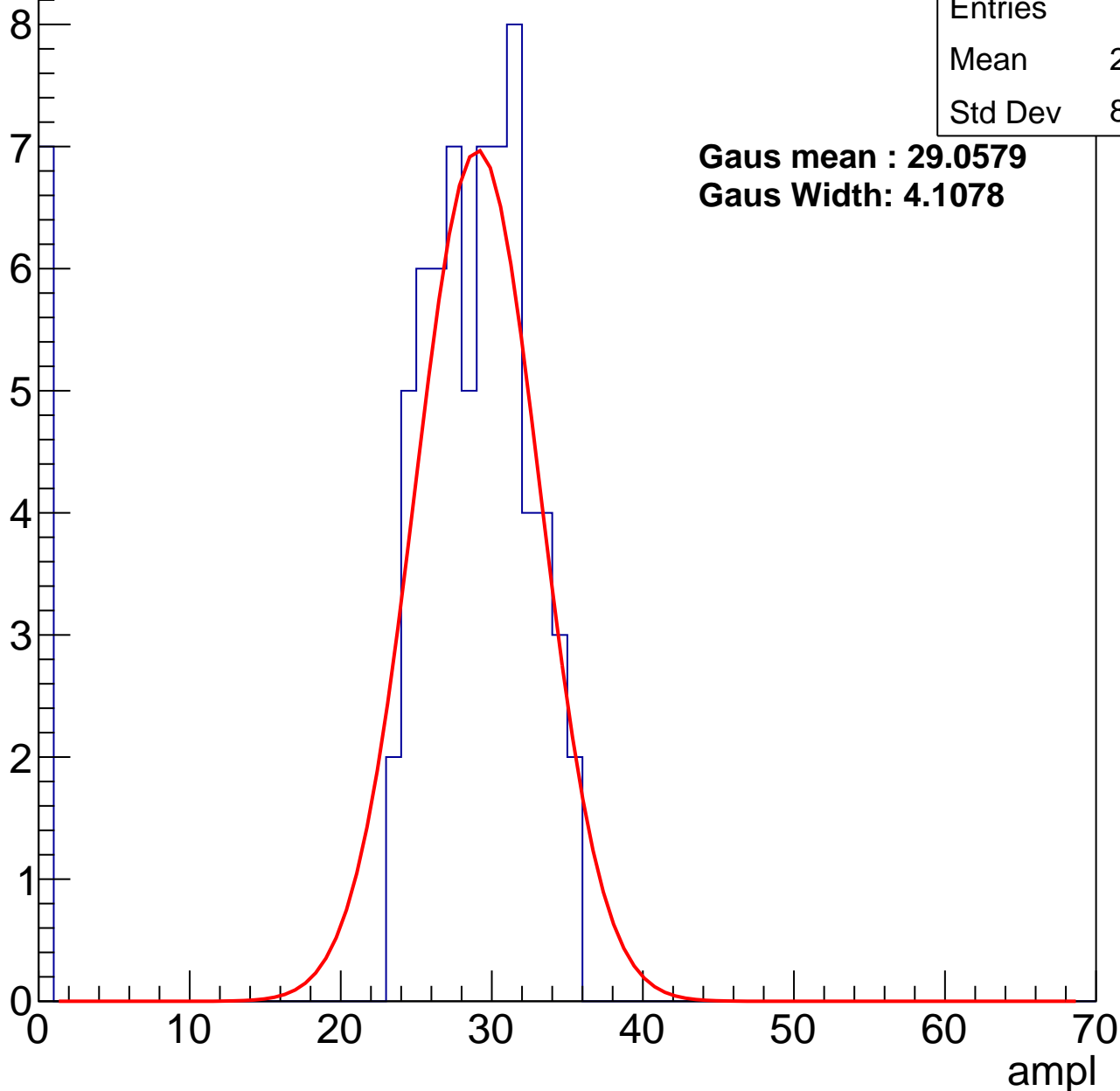
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	25.95
Std Dev	8.969

**Gaus mean : 29.0579**

**Gaus Width: 4.1078**



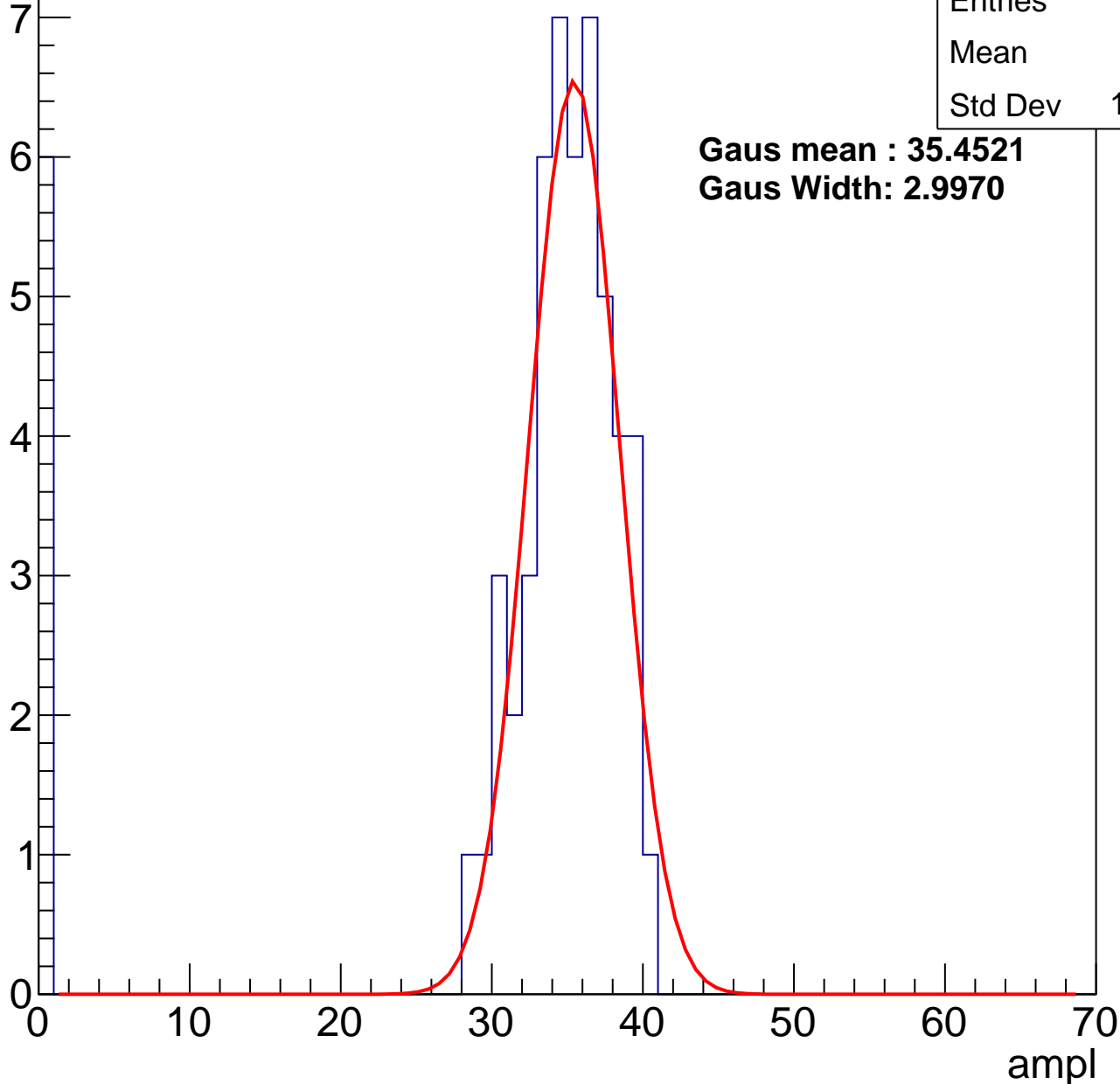
# B1L103S, U3-ch42, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	56
Mean	31
Std Dev	11.06

**Gaus mean : 35.4521**  
**Gaus Width: 2.9970**



# B1L103S, U3-ch42, adc2

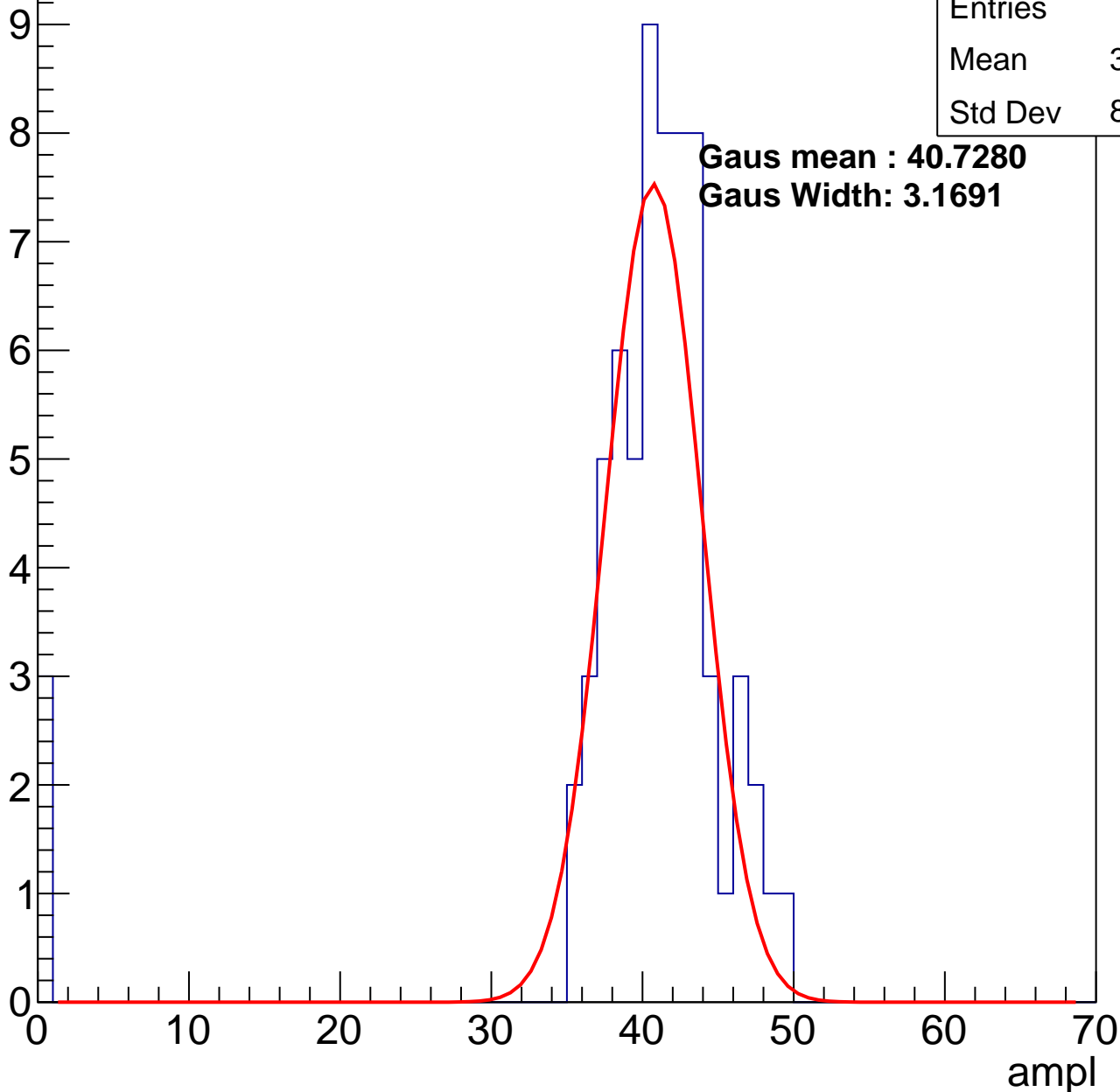
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	39.12
Std Dev	8.957

**Gaus mean : 40.7280**

**Gaus Width: 3.1691**

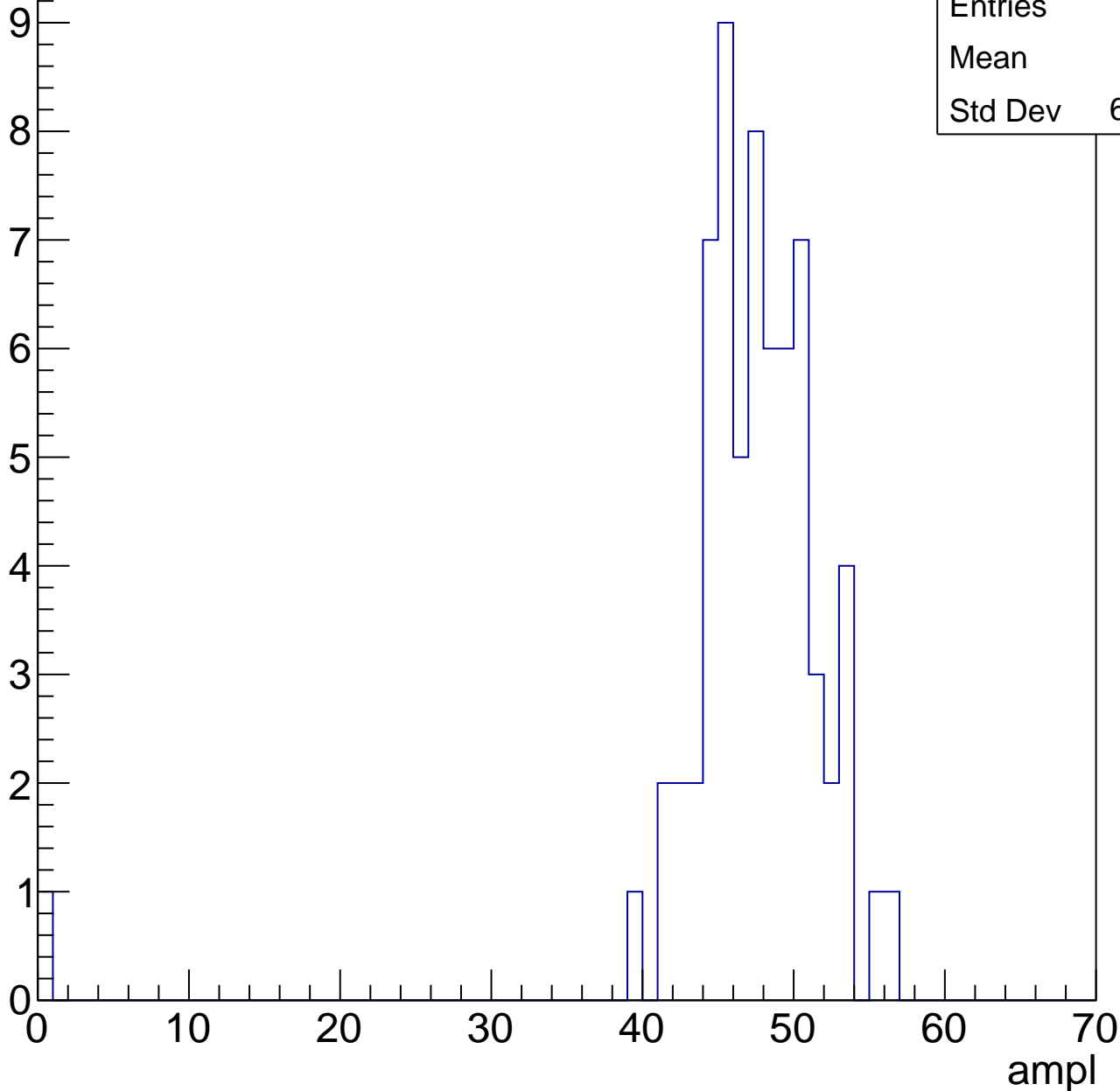


# B1L103S, U3-ch42, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

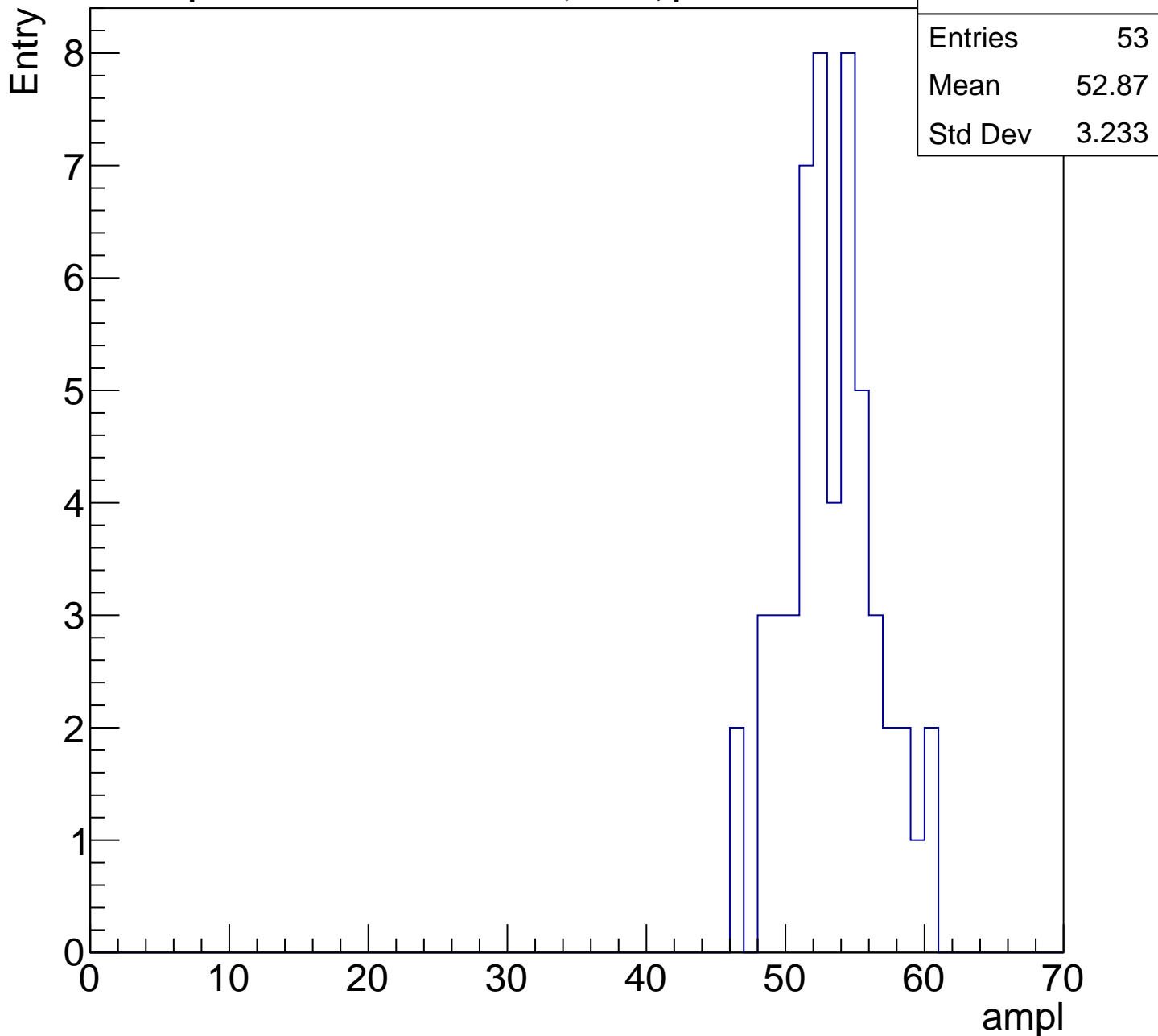
Entry

Entries	67
Mean	46.6
Std Dev	6.692



# B1L103S, U3-ch42, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U3-ch42, adc5

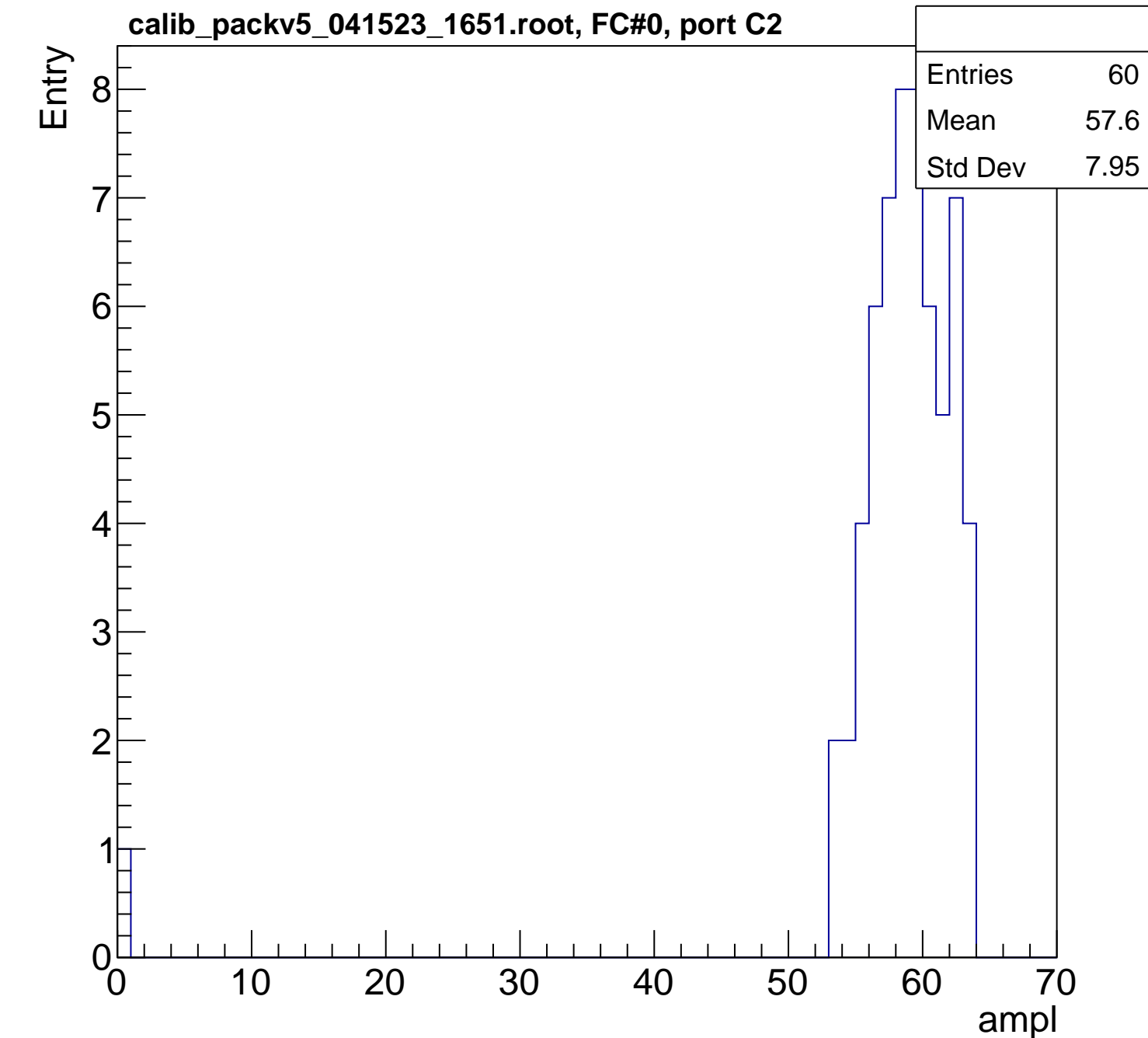
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	60
Mean	57.6
Std Dev	7.95

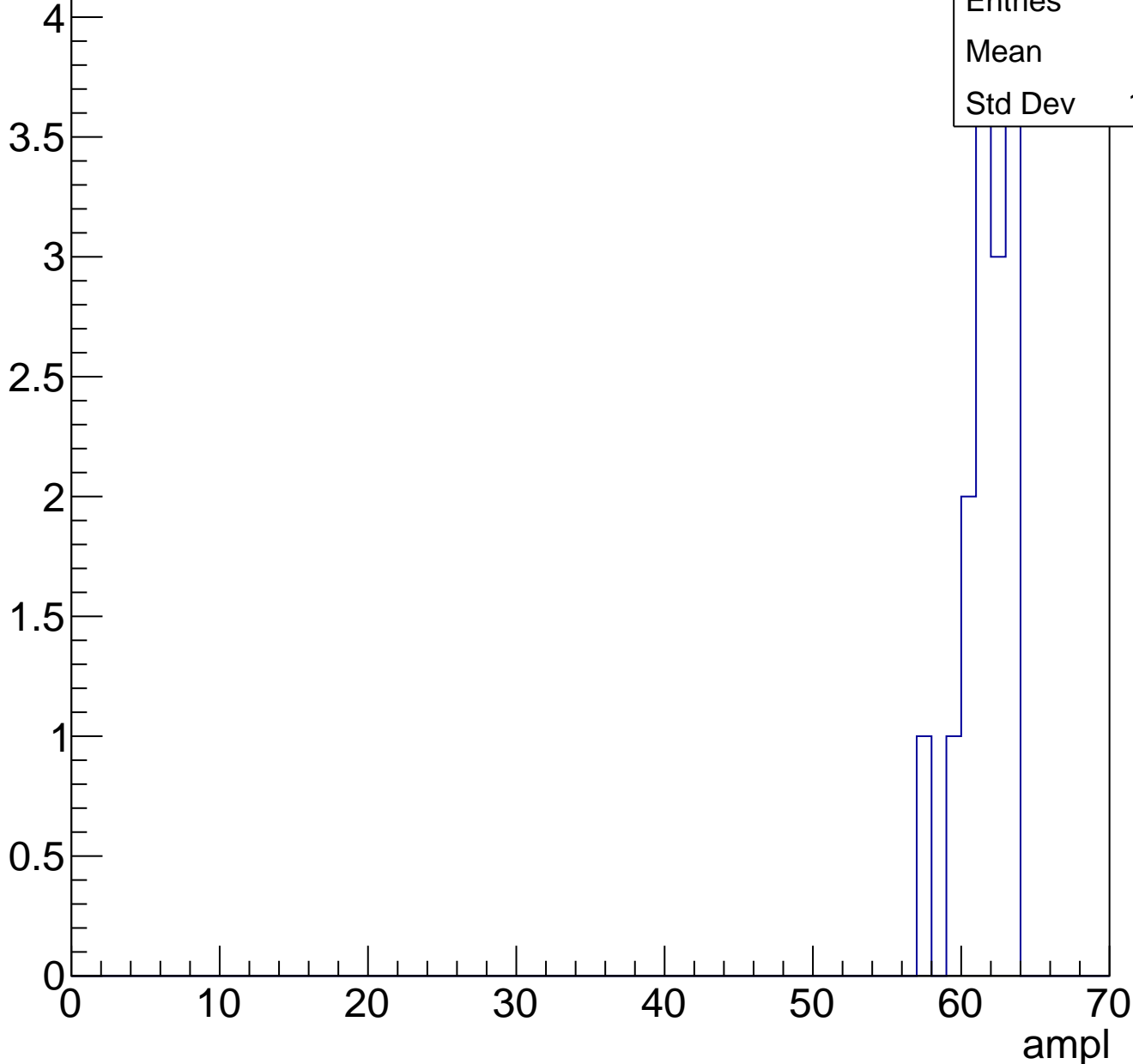
ampl



# B1L103S, U3-ch42, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



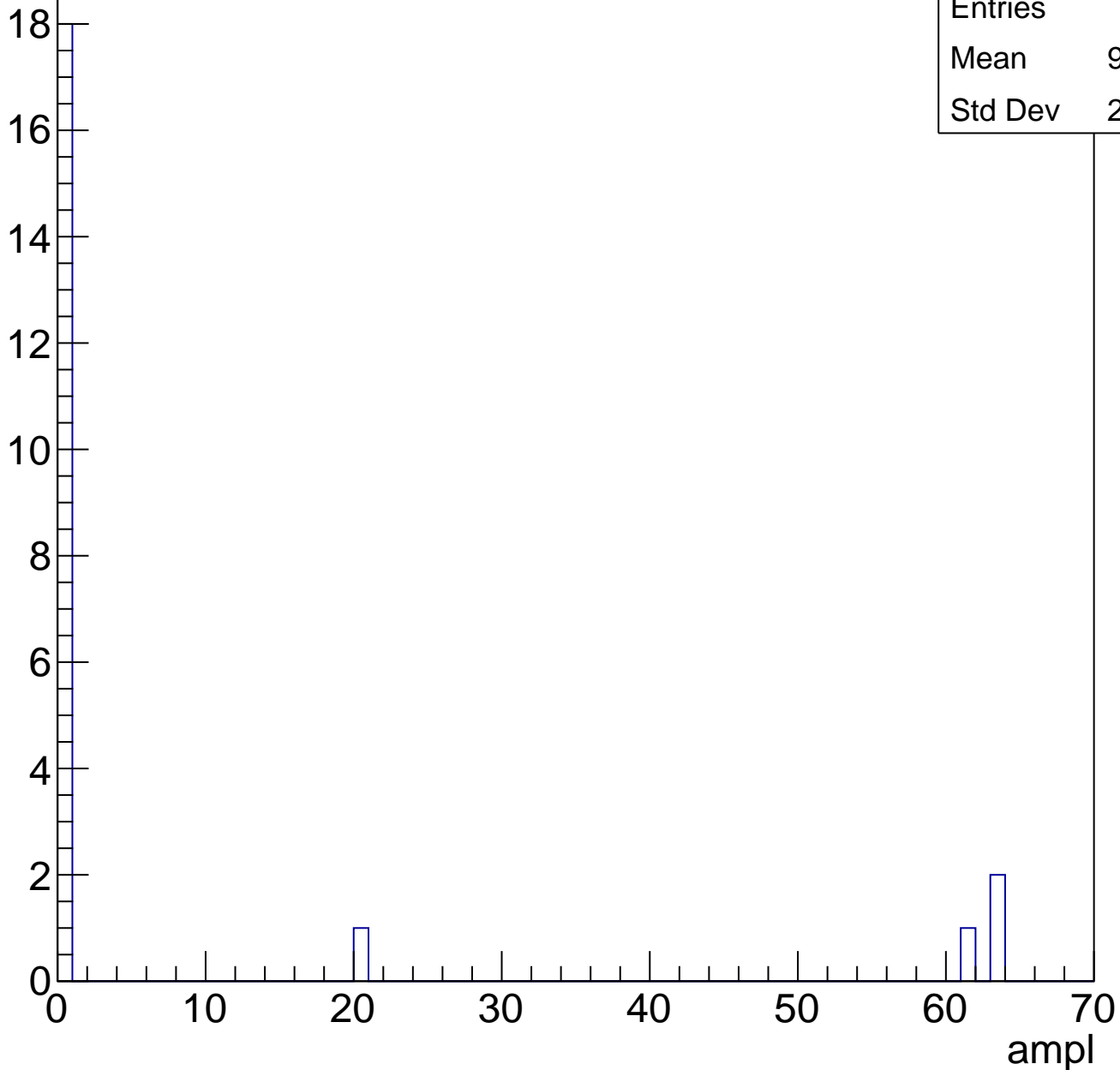


# B1L103S, U3-ch42, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	22
Mean	9.409
Std Dev	21.44

Entry



# B1L103S, U3-ch43, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	105
Mean	23.78
Std Dev	10.8

**Gaus mean : 28.4067**

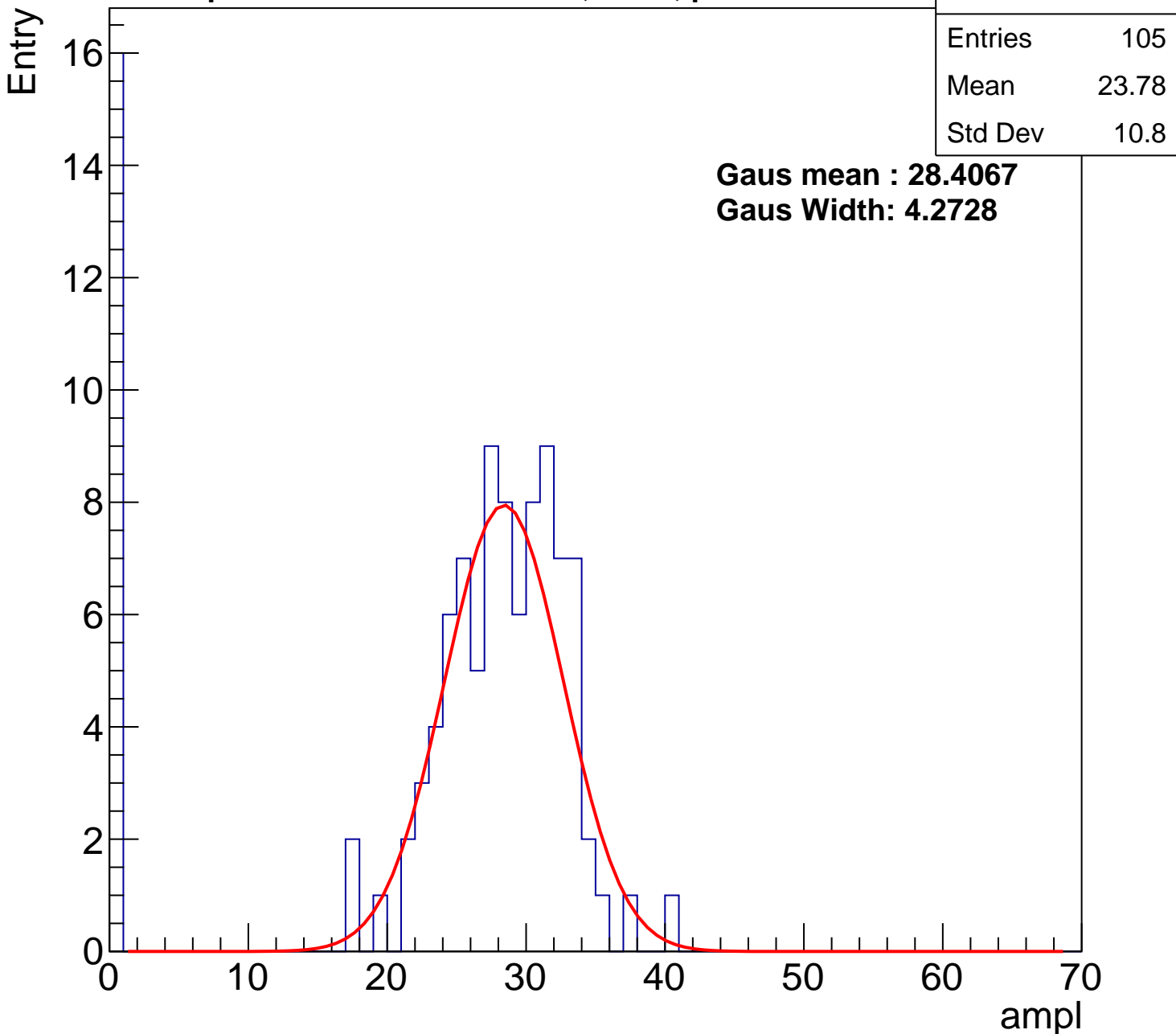
**Gaus Width: 4.2728**

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch43, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	62
Mean	34.39
Std Dev	6.992

**Gaus mean : 36.5988**

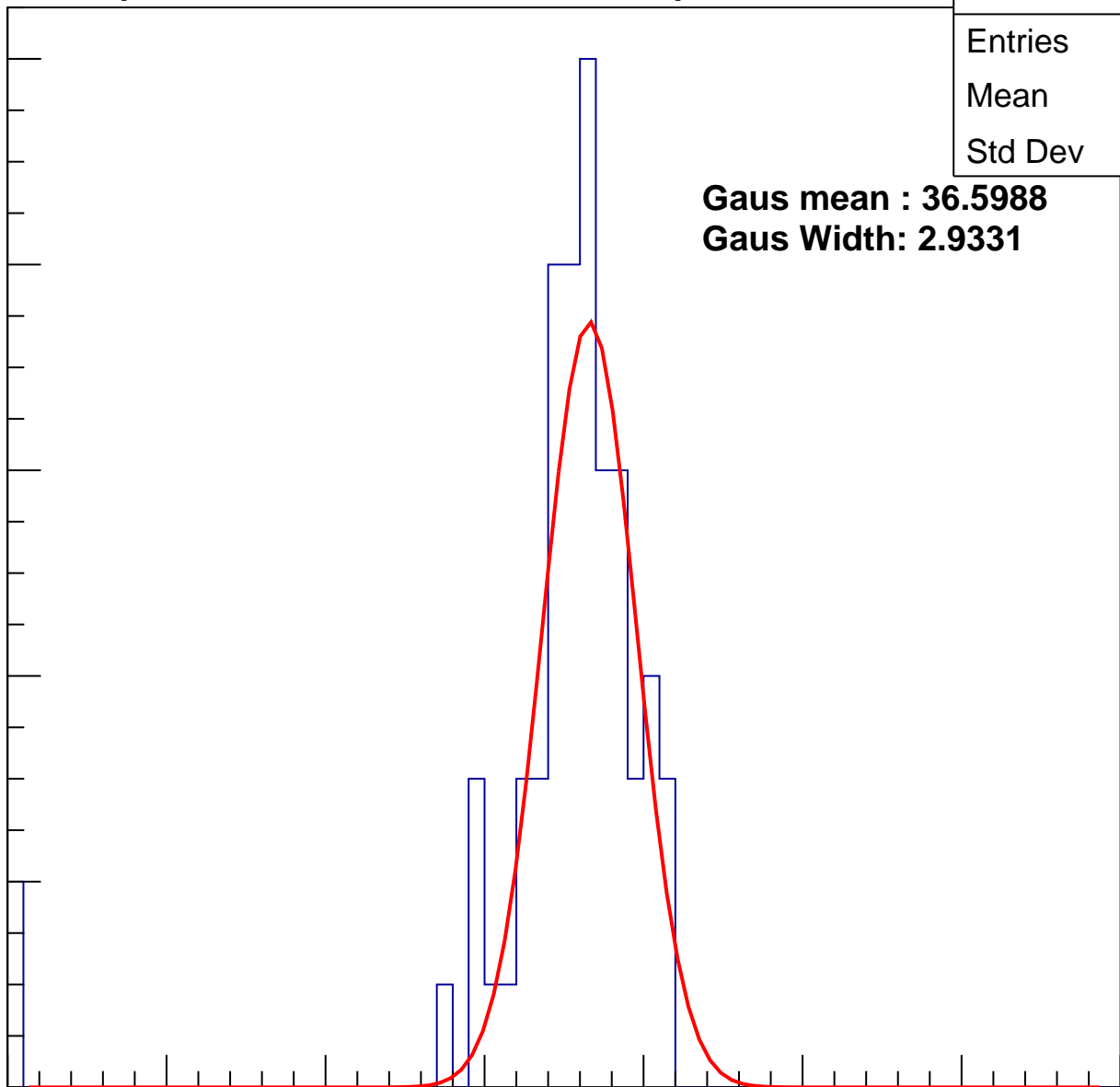
**Gaus Width: 2.9331**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch43, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	70
Mean	35.61
Std Dev	15.63

**Gaus mean : 42.6330**

**Gaus Width: 3.6131**

Entry

10

8

6

4

2

0

0

10

20

30

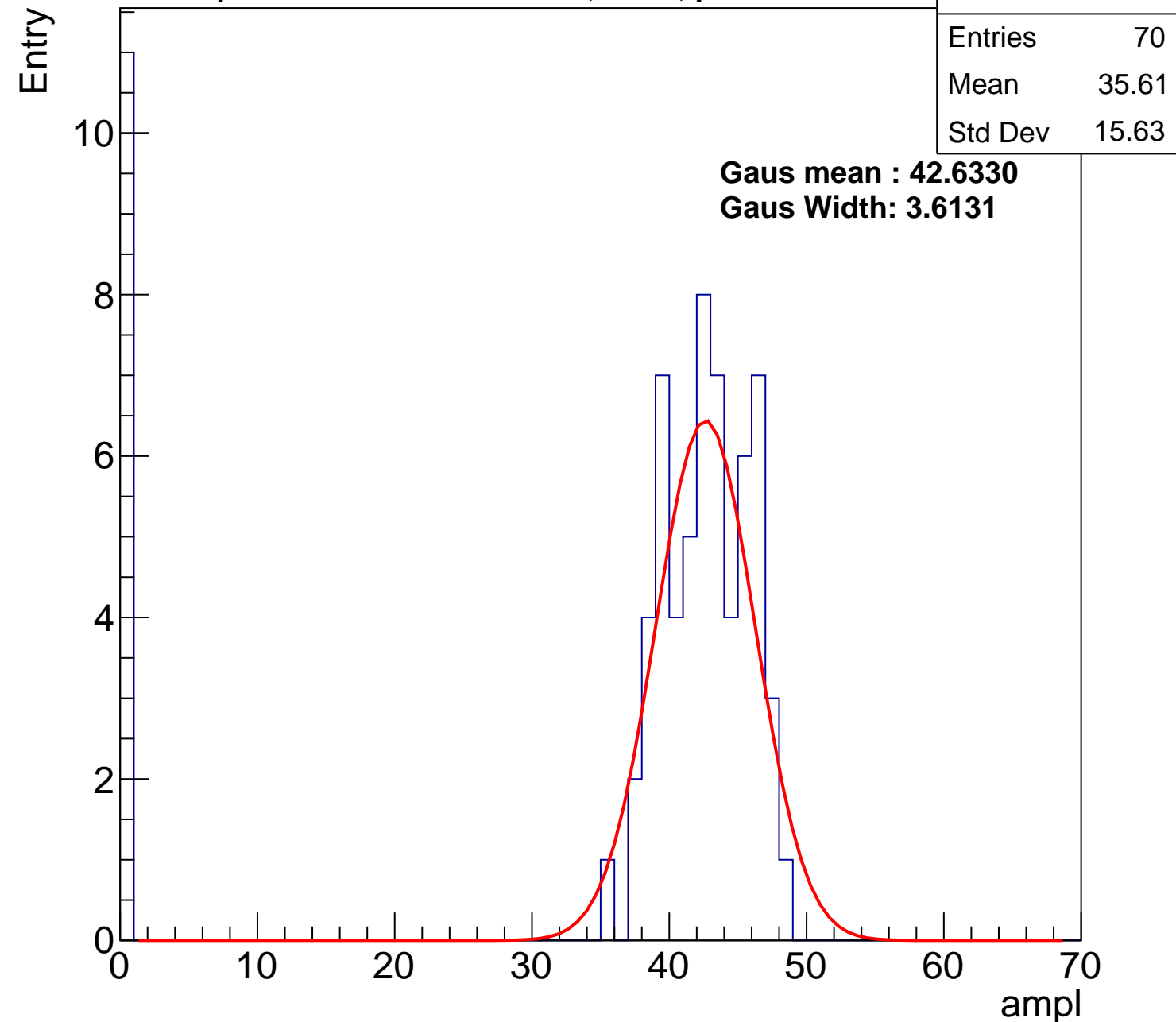
40

50

60

70

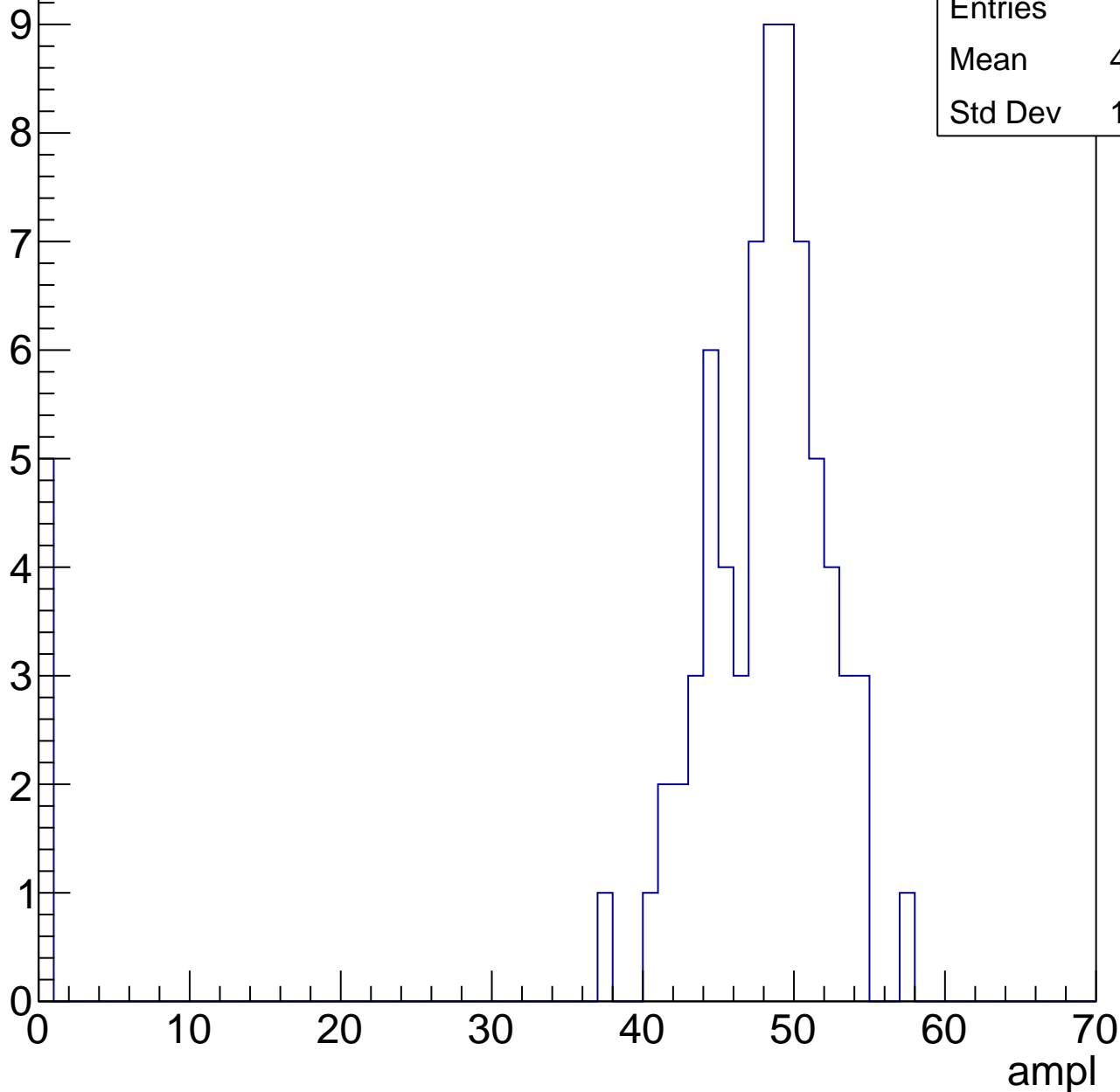
ampl



# B1L103S, U3-ch43, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

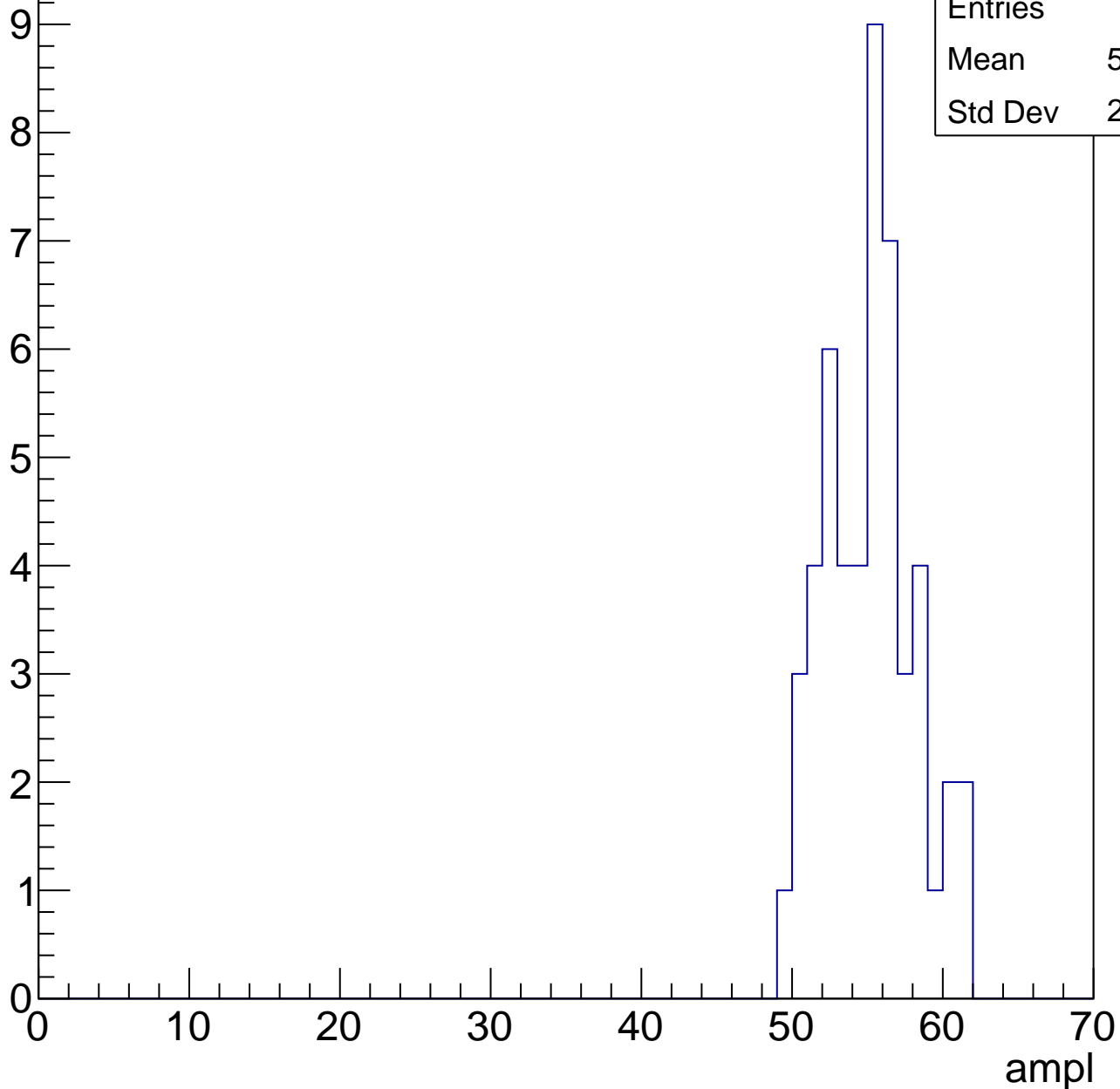
Entry



# B1L103S, U3-ch43, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



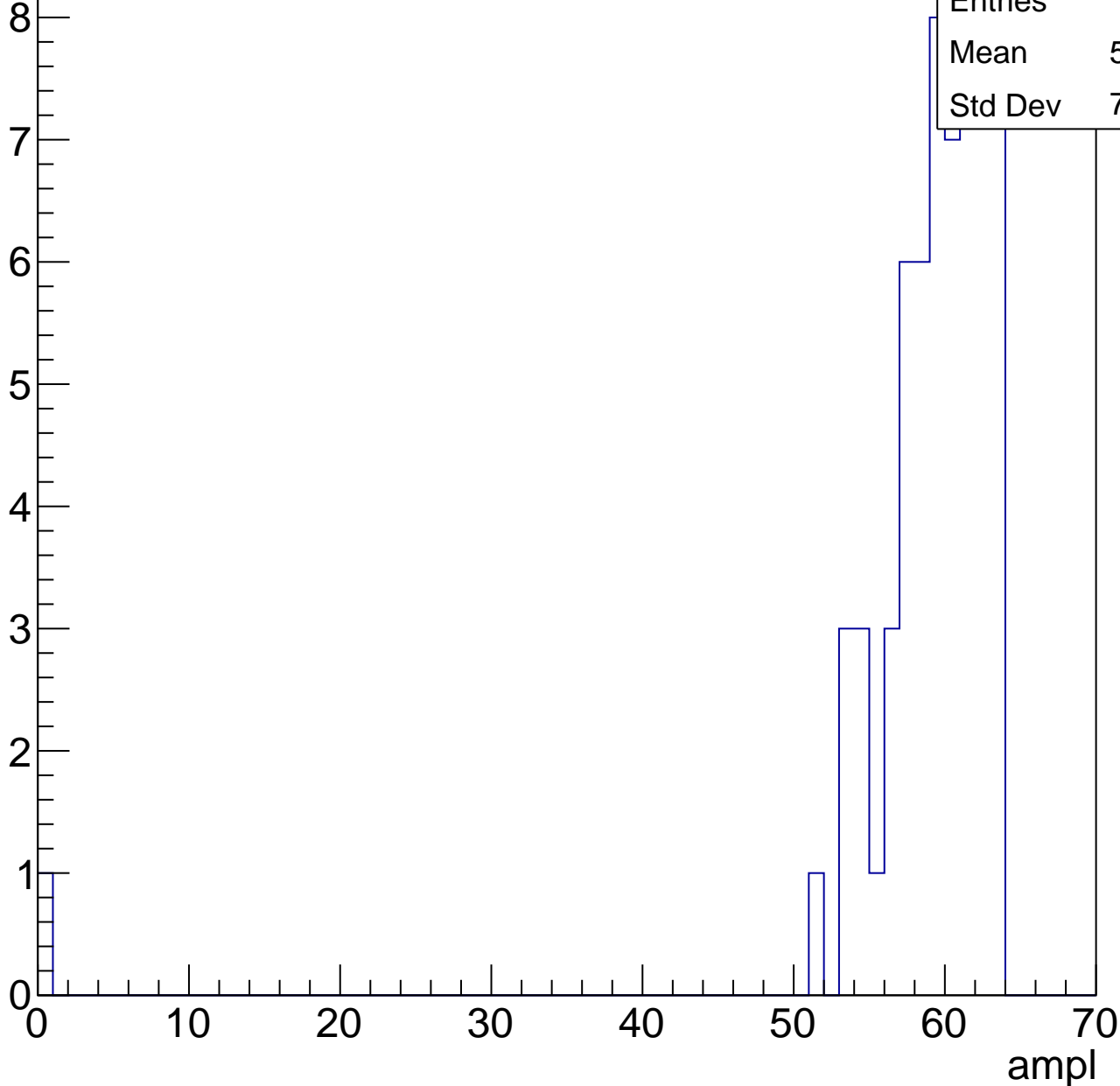
Entries	50
Mean	54.68
Std Dev	2.956

# B1L103S, U3-ch43, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	58.17
Std Dev	7.965



# B1L103S, U3-ch43, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.5
Std Dev	1.5

0 10 20 30 40 50 60 70

ampl

1



# B1L103S, U3-ch43, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	19
Mean	0
Std Dev	0

ampl

# B1L103S, U3-ch44, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

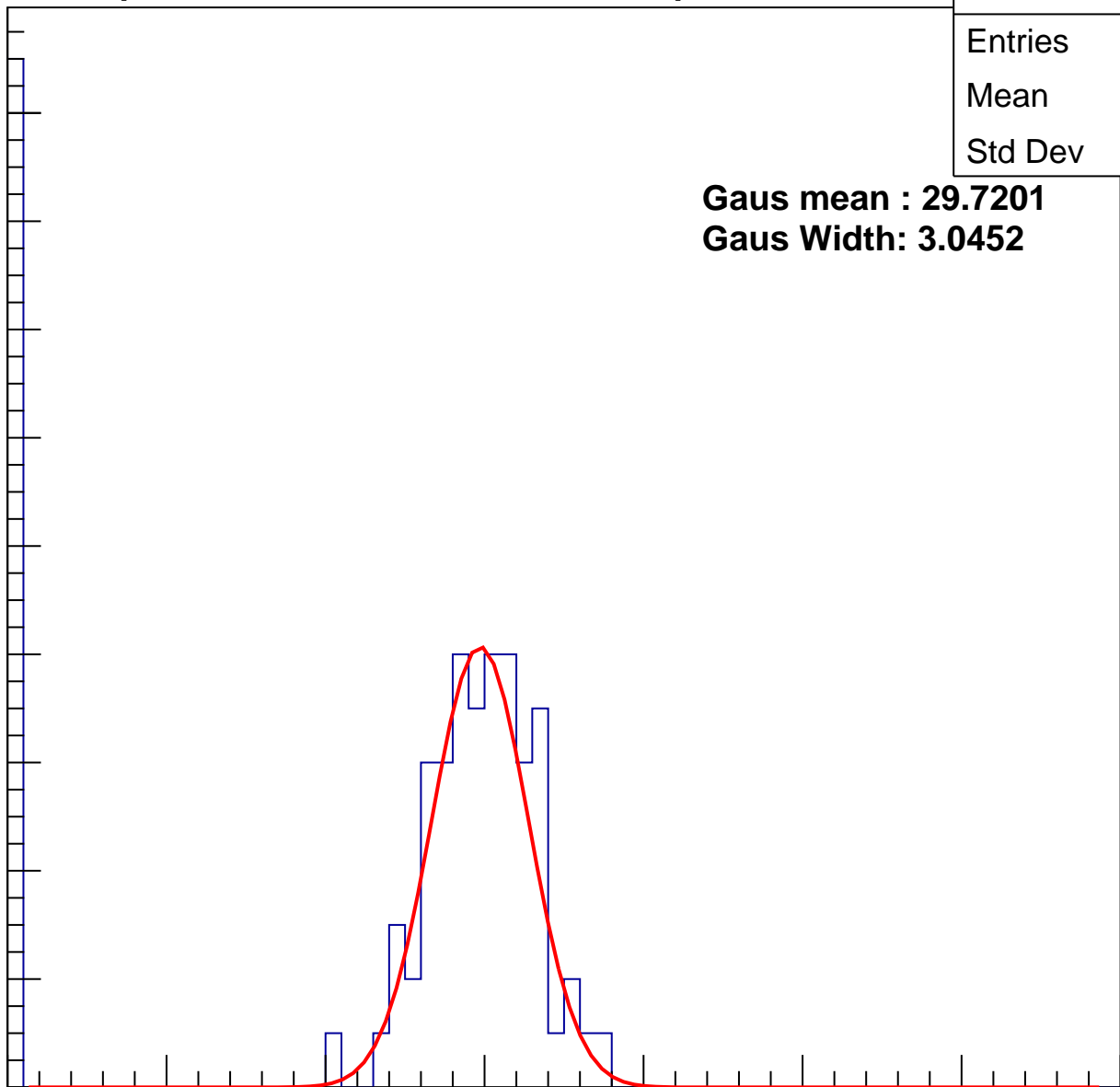
Entries	87
Mean	22.97
Std Dev	12.47

**Gaus mean : 29.7201**

**Gaus Width: 3.0452**

0 10 20 30 40 50 60 70

ampl



# B1L103S, U3-ch44, adc1

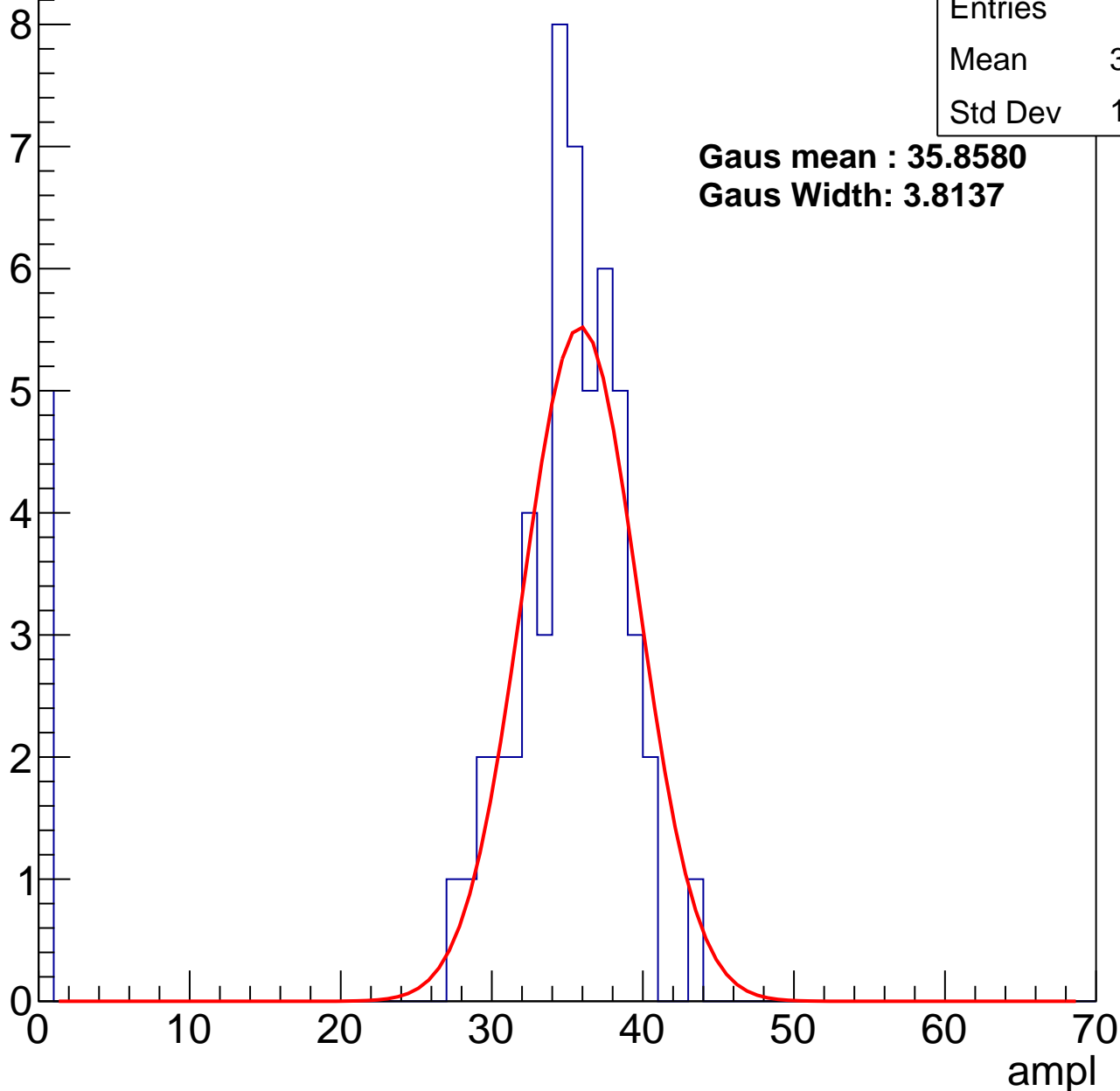
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	57
Mean	31.77
Std Dev	10.34

**Gaus mean : 35.8580**

**Gaus Width: 3.8137**

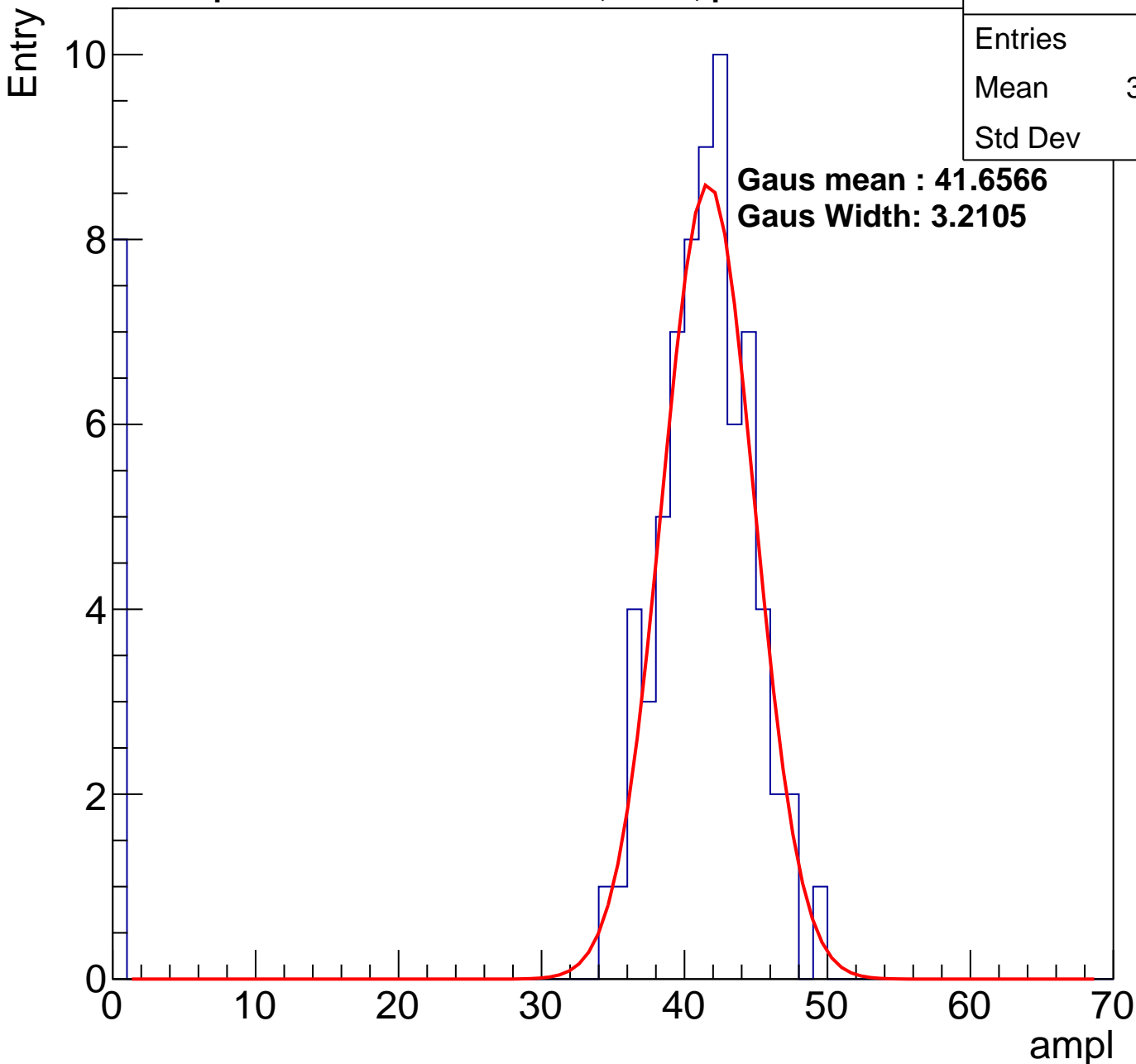


# B1L103S, U3-ch44, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	78
Mean	36.88
Std Dev	12.8

**Gaus mean : 41.6566**  
**Gaus Width: 3.2105**



# B1L103S, U3-ch44, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	67
Mean	47.75
Std Dev	6.763

Entry

10  
8  
6  
4  
2  
0

ampl

0

10

20

30

40

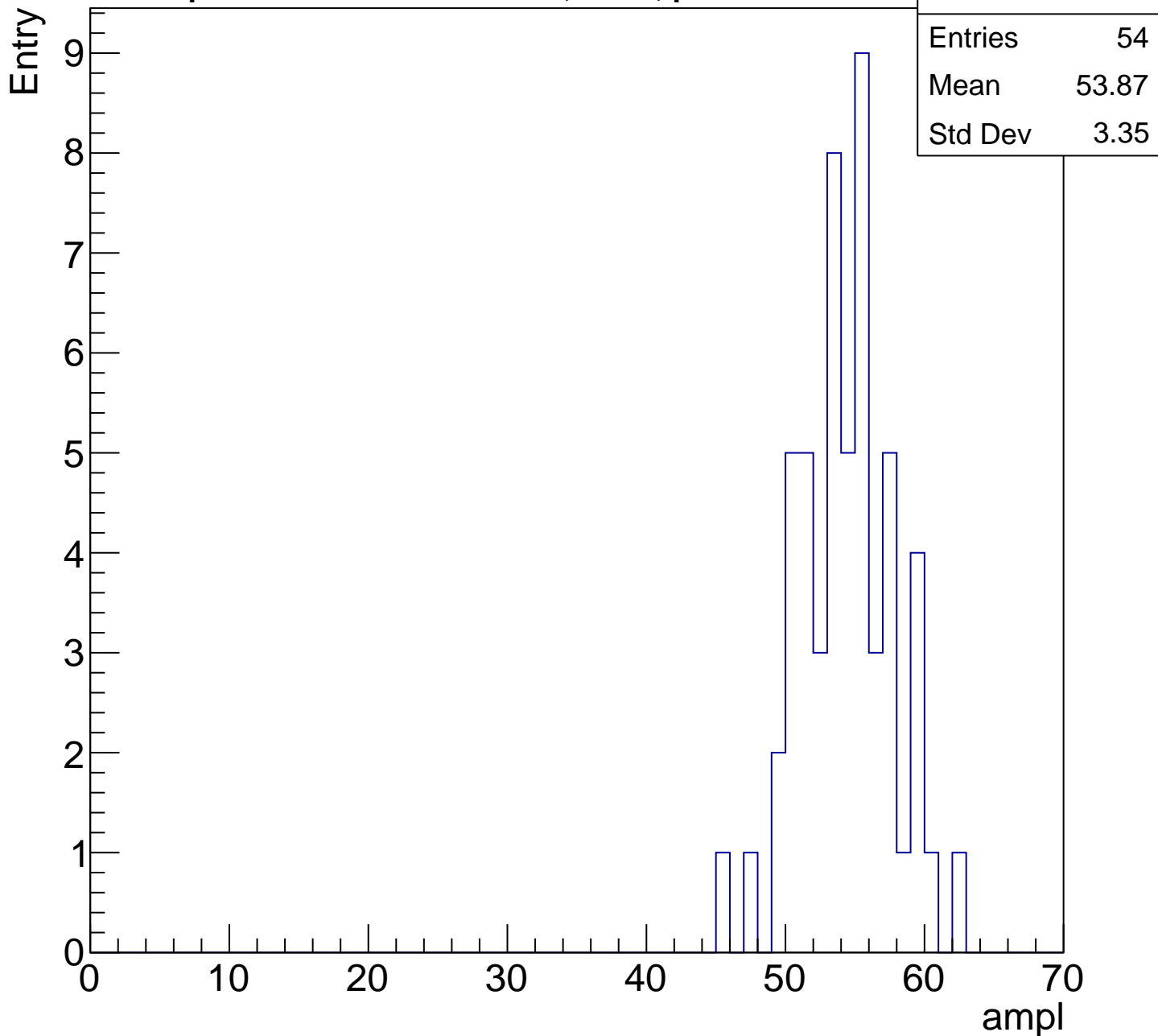
50

60

70

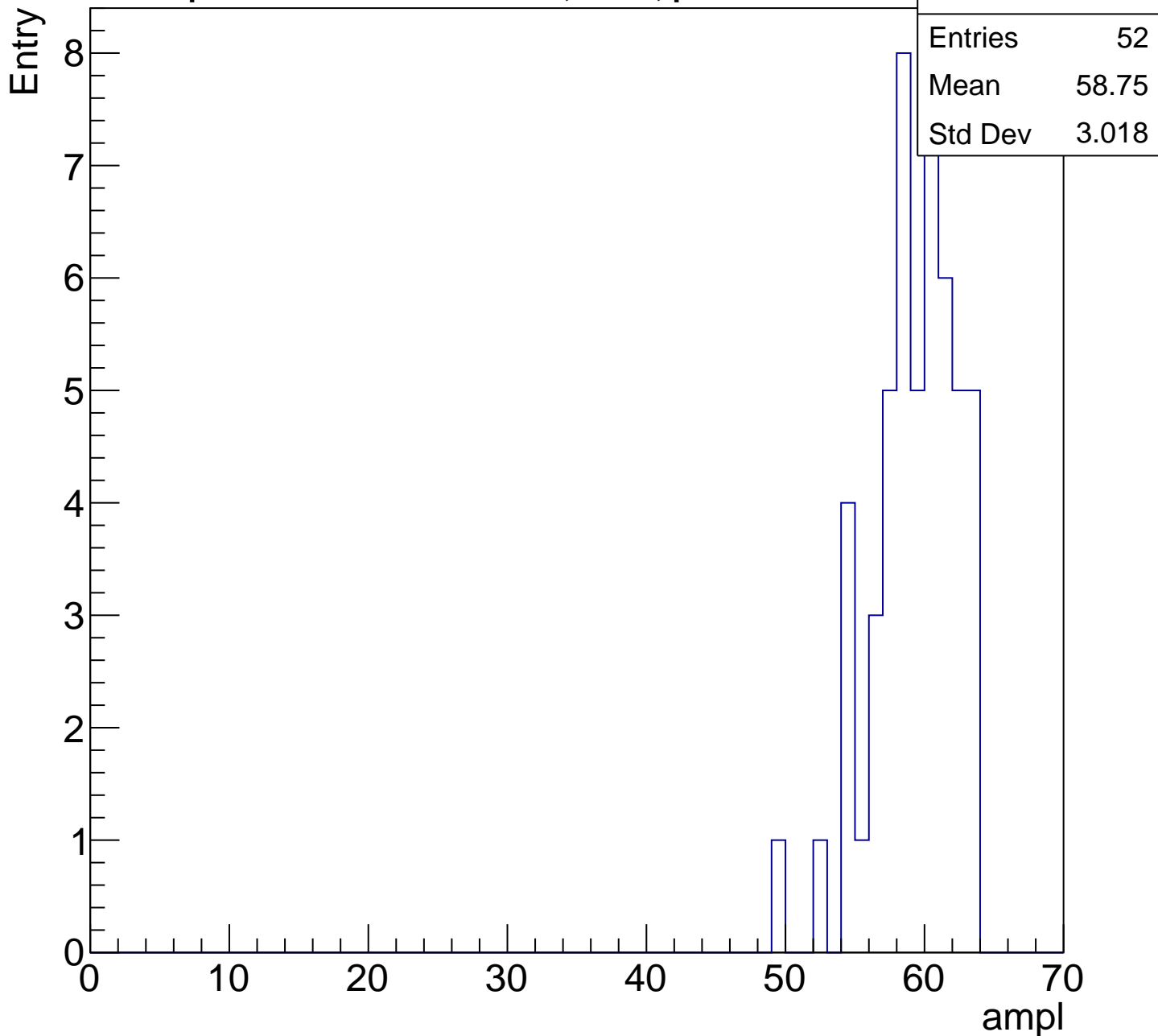
# B1L103S, U3-ch44, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U3-ch44, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

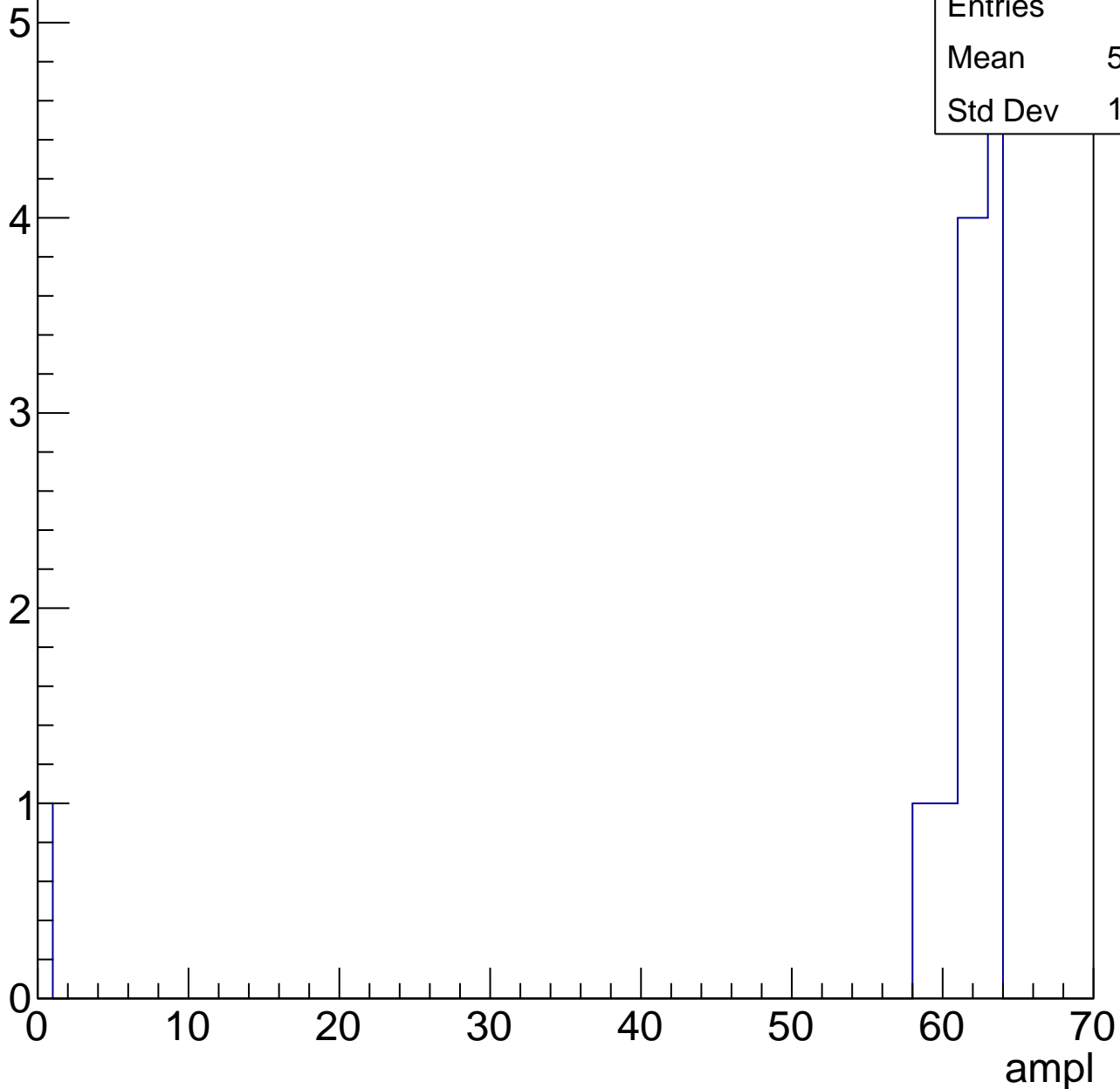


# B1L103S, U3-ch44, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	17
Mean	57.88
Std Dev	14.54





# B1L103S, U3-ch44, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	19
Mean	0
Std Dev	0

ampl

# B1L103S, U3-ch45, adc0

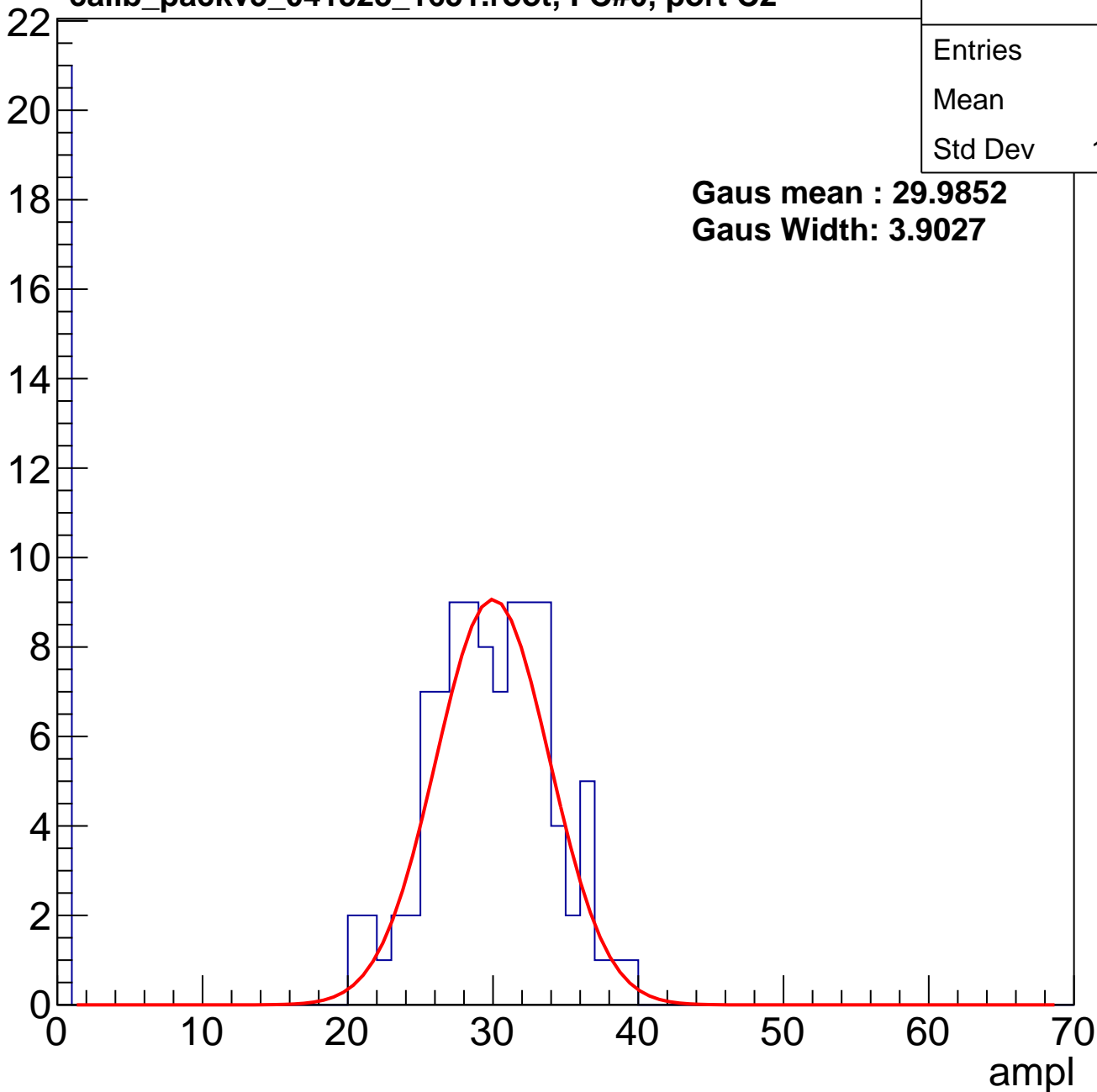
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	118
Mean	24.2
Std Dev	11.85

**Gaus mean : 29.9852**

**Gaus Width: 3.9027**

Entry



# B1L103S, U3-ch45, adc1

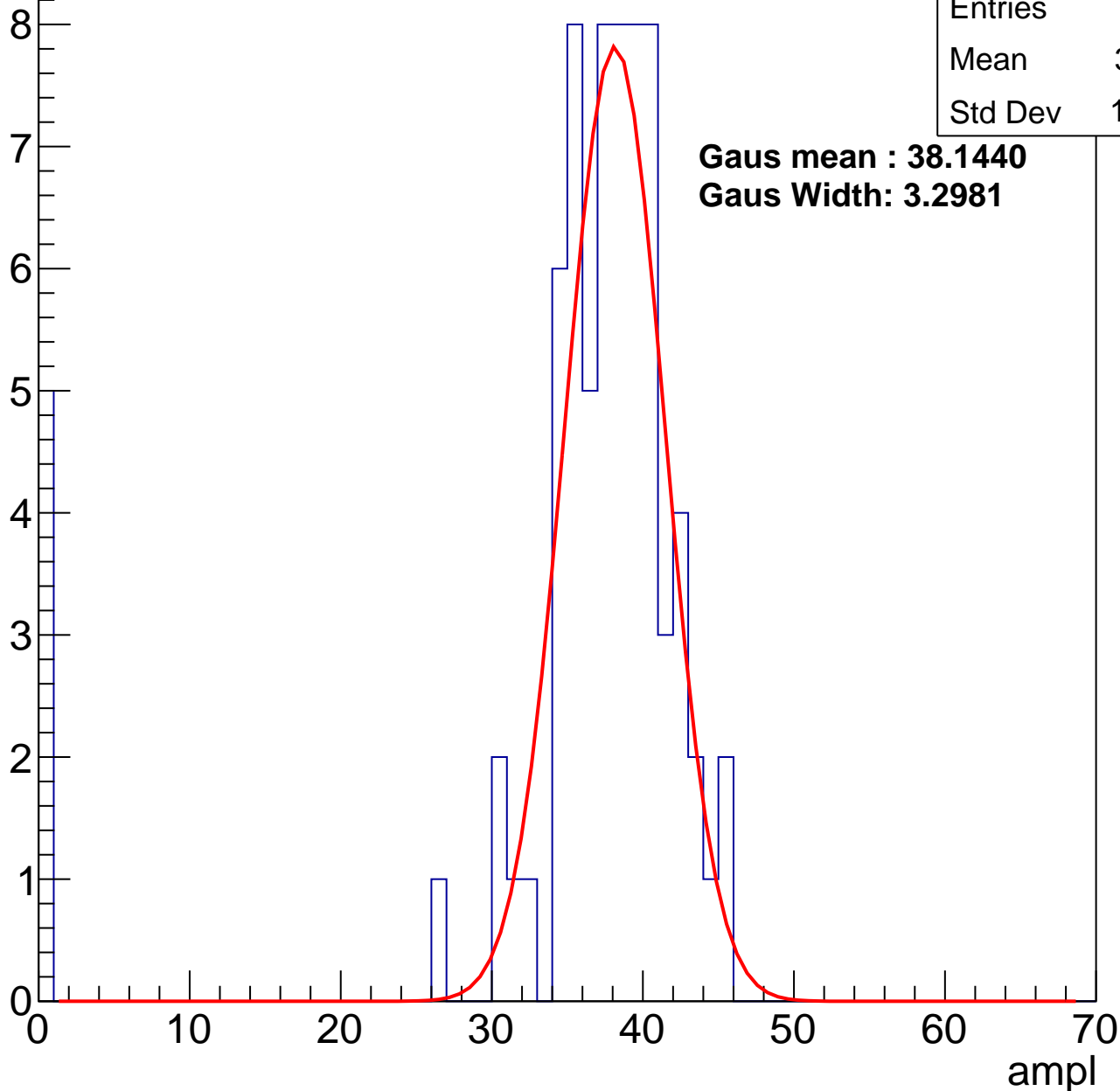
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	35.01
Std Dev	10.09

**Gaus mean : 38.1440**

**Gaus Width: 3.2981**



# B1L103S, U3-ch45, adc2

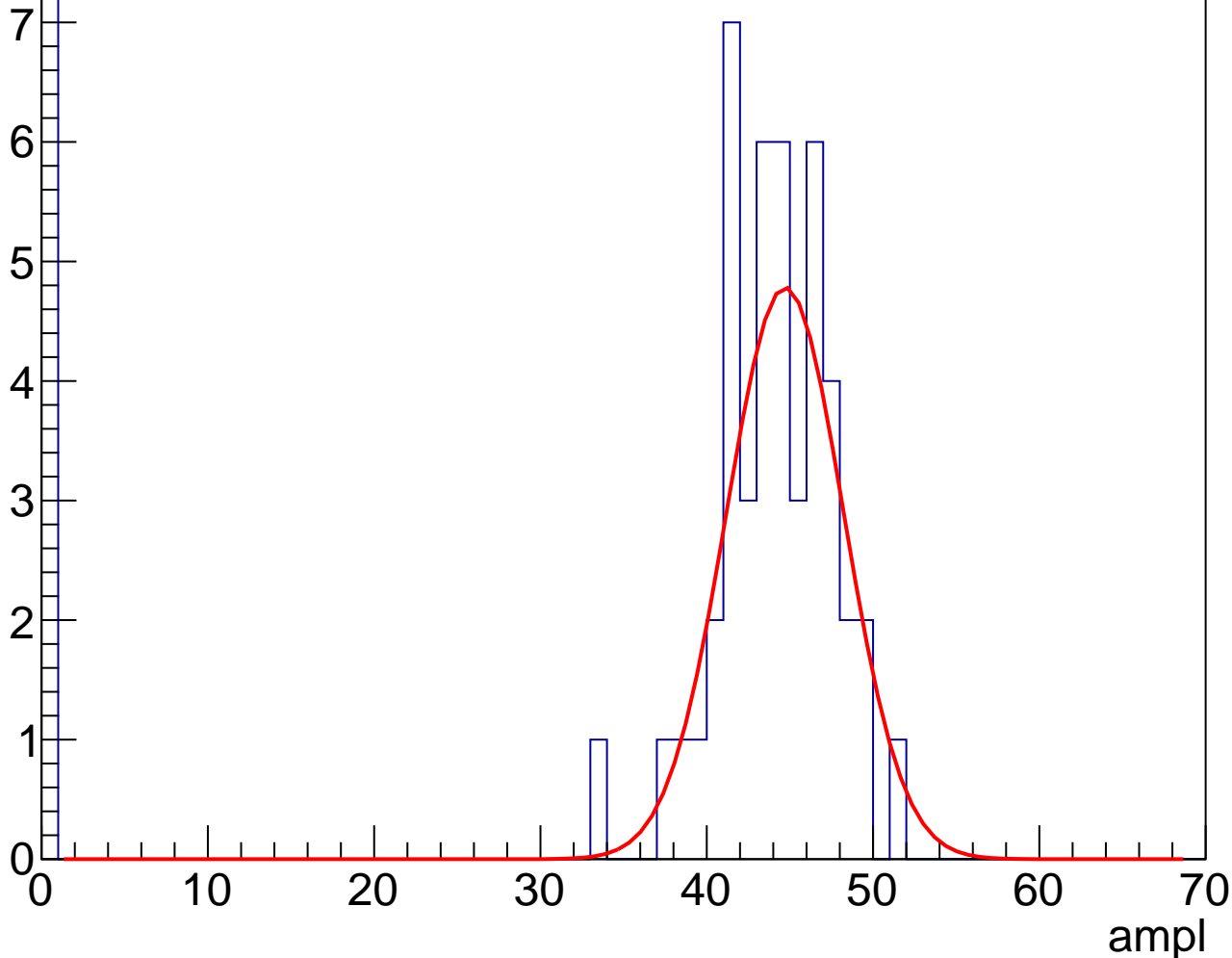
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	55
Mean	36.47
Std Dev	16.43

**Gaus mean : 44.7096**

**Gaus Width: 3.5216**

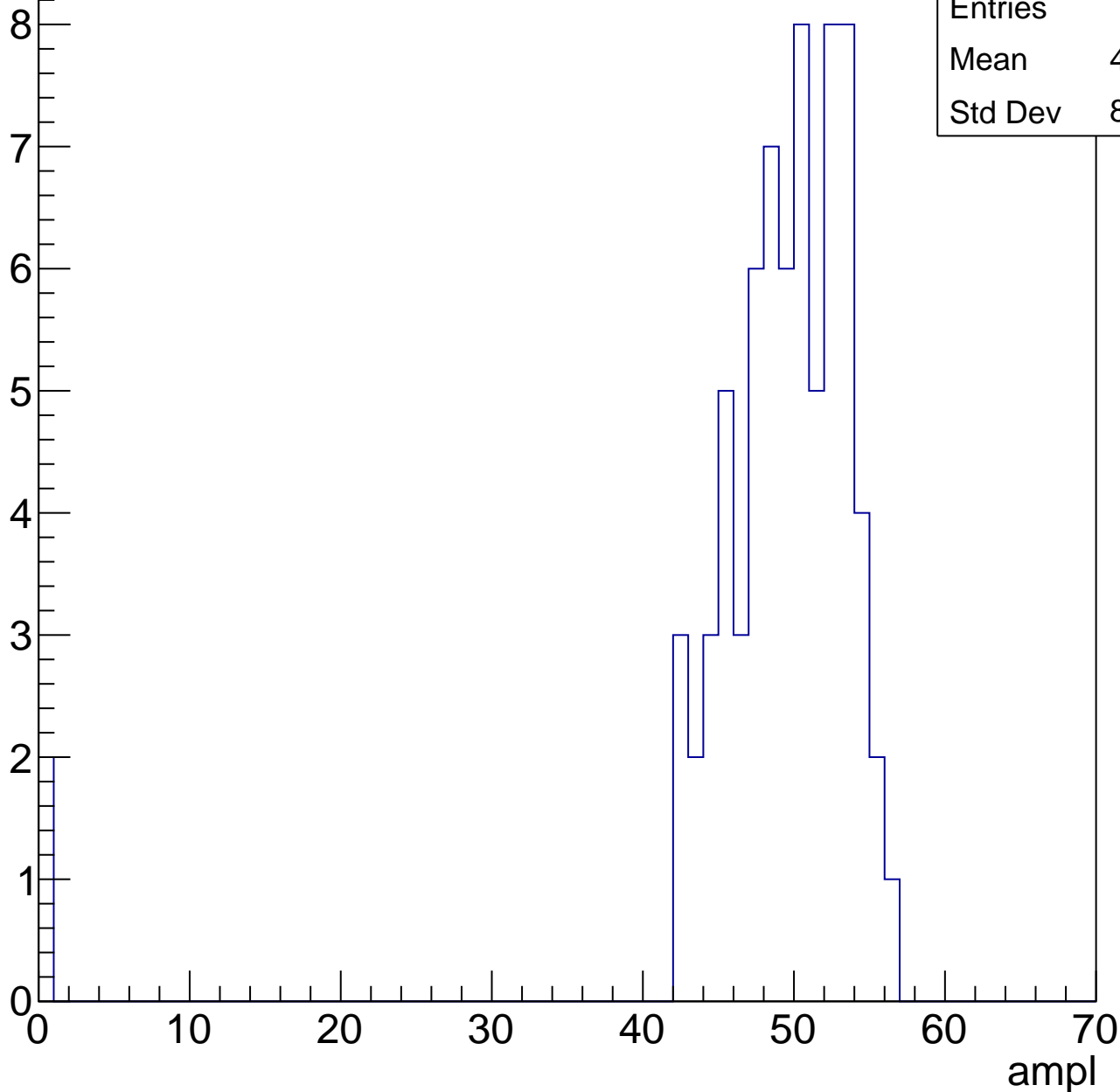


# B1L103S, U3-ch45, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	47.89
Std Dev	8.753

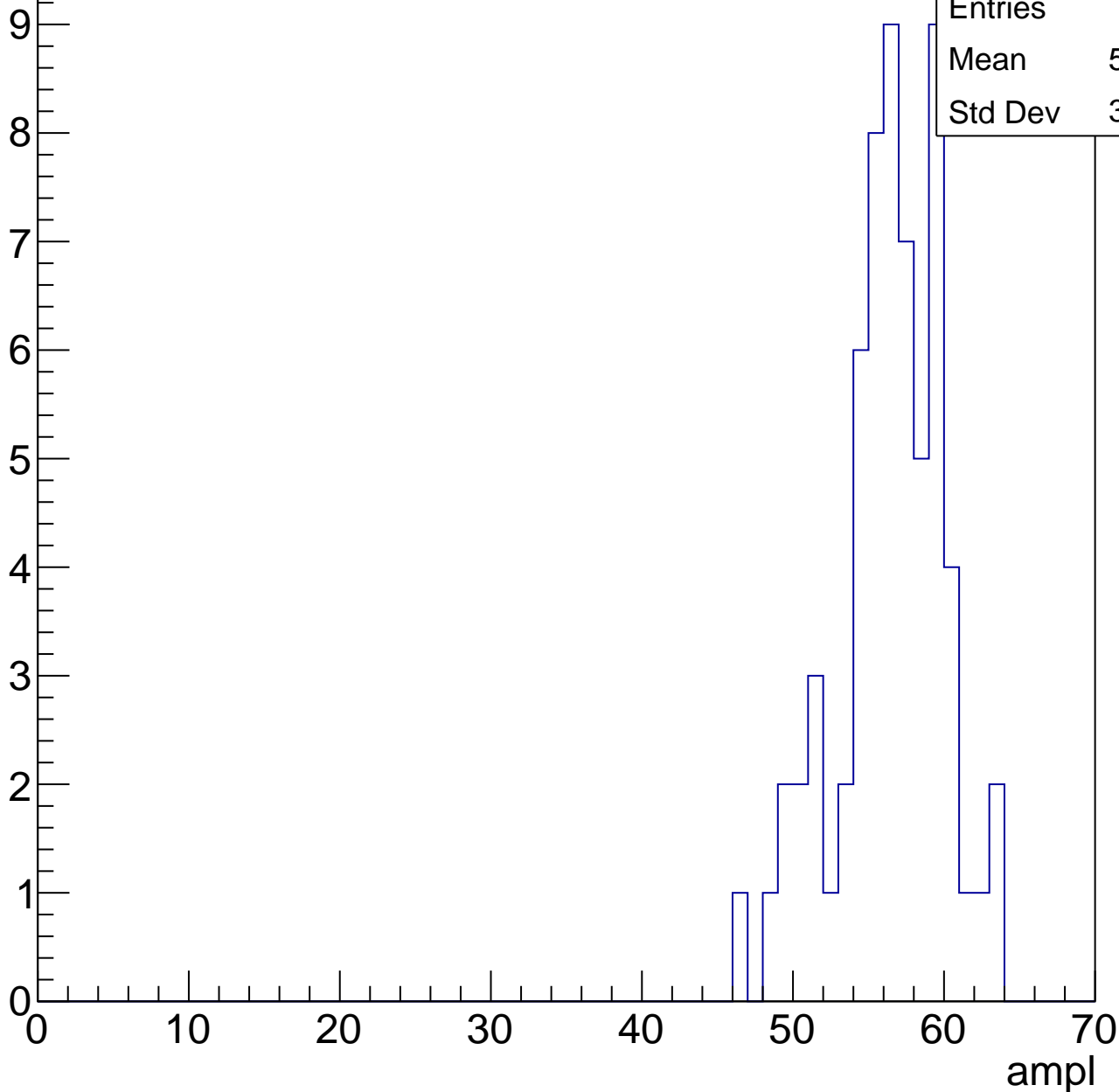


# B1L103S, U3-ch45, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	55.94
Std Dev	3.548

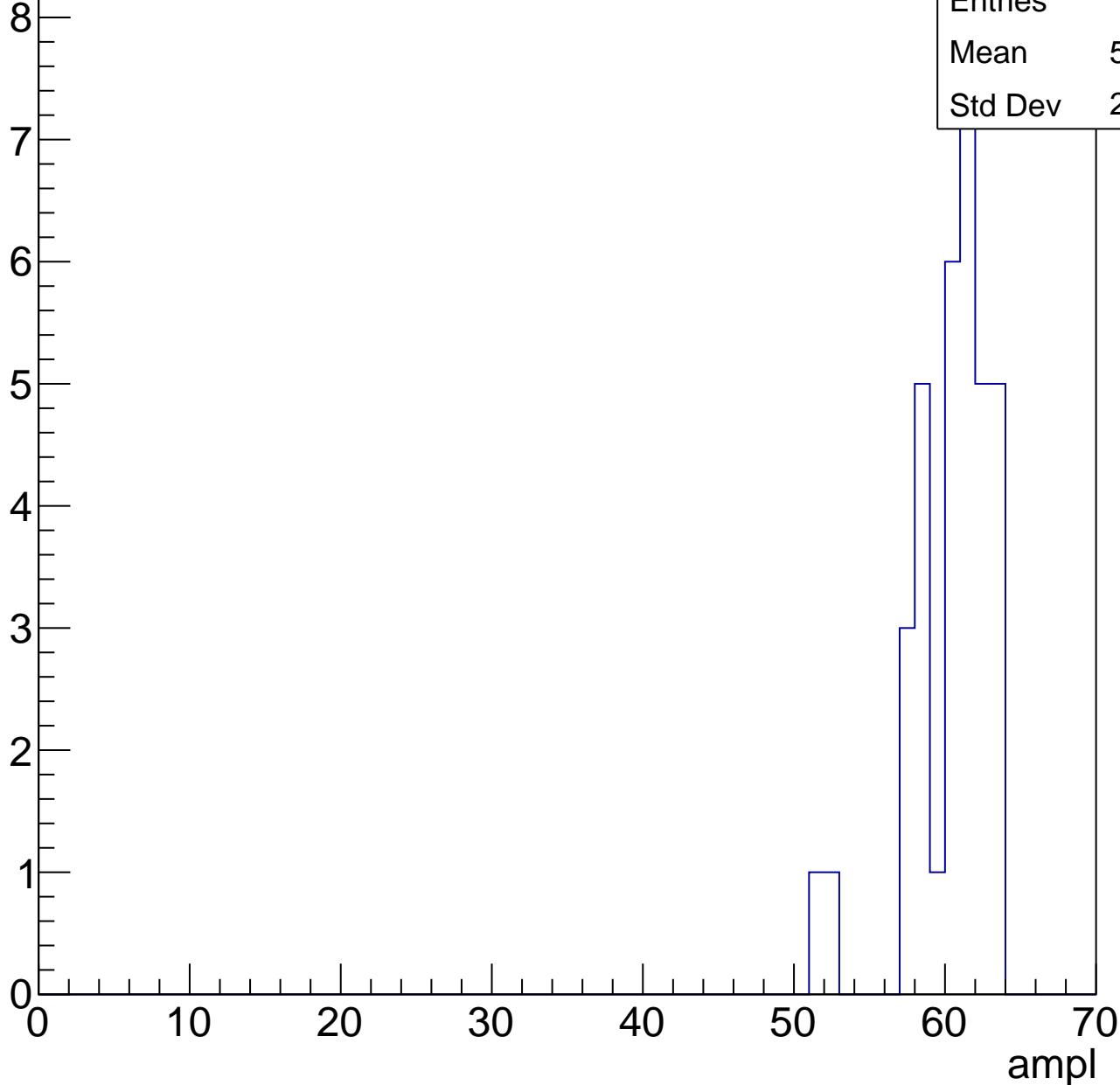


# B1L103S, U3-ch45, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

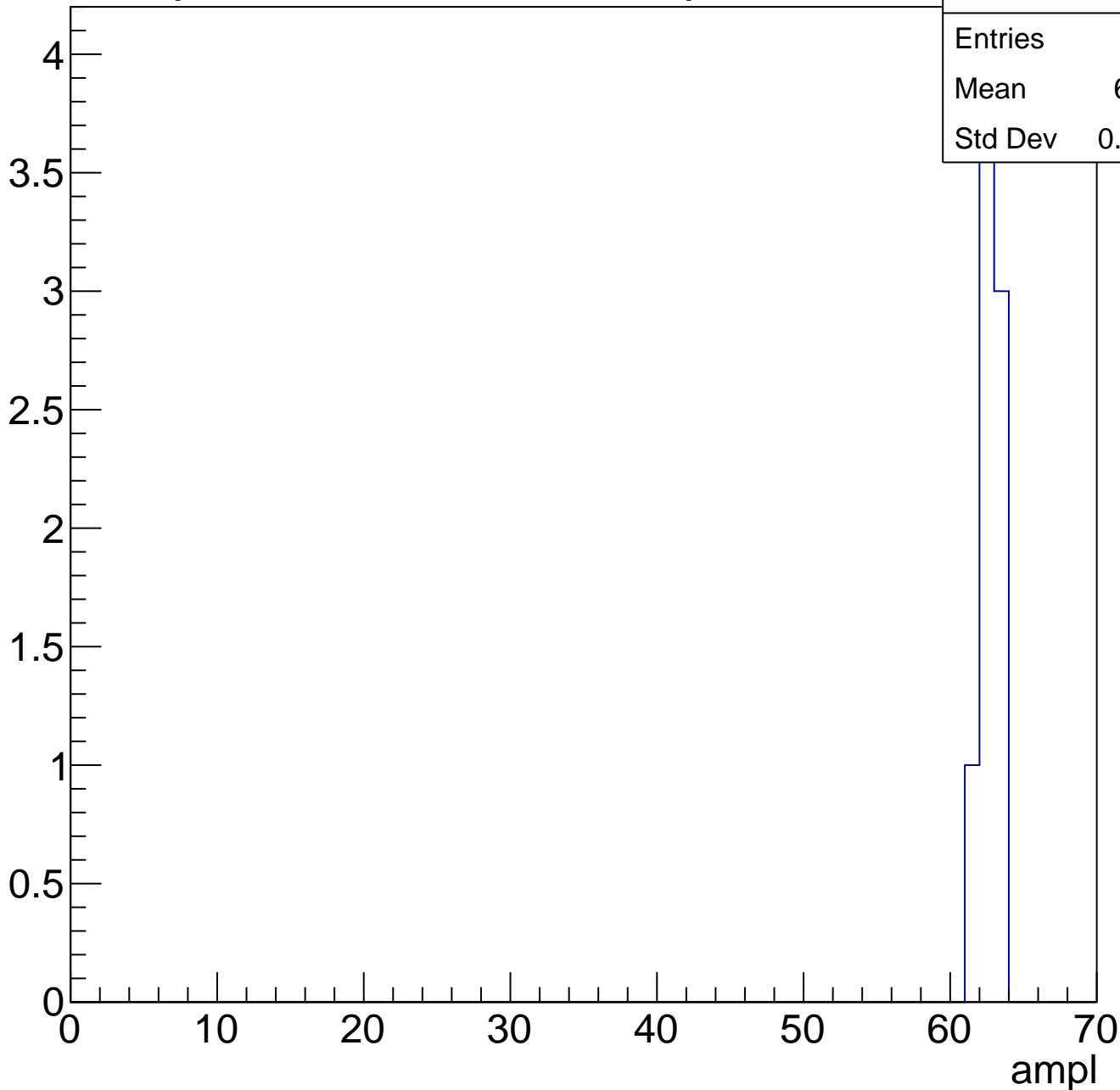
Entries	35
Mean	59.89
Std Dev	2.754



# B1L103S, U3-ch45, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U3-ch45, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	20
Mean	0
Std Dev	0

ampl

# B1L103S, U3-ch46, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	86
Mean	19.22
Std Dev	13.6

**Gaus mean : 28.7633**

**Gaus Width: 3.7645**

Entry

25

20

15

10

5

0

0

10

20

30

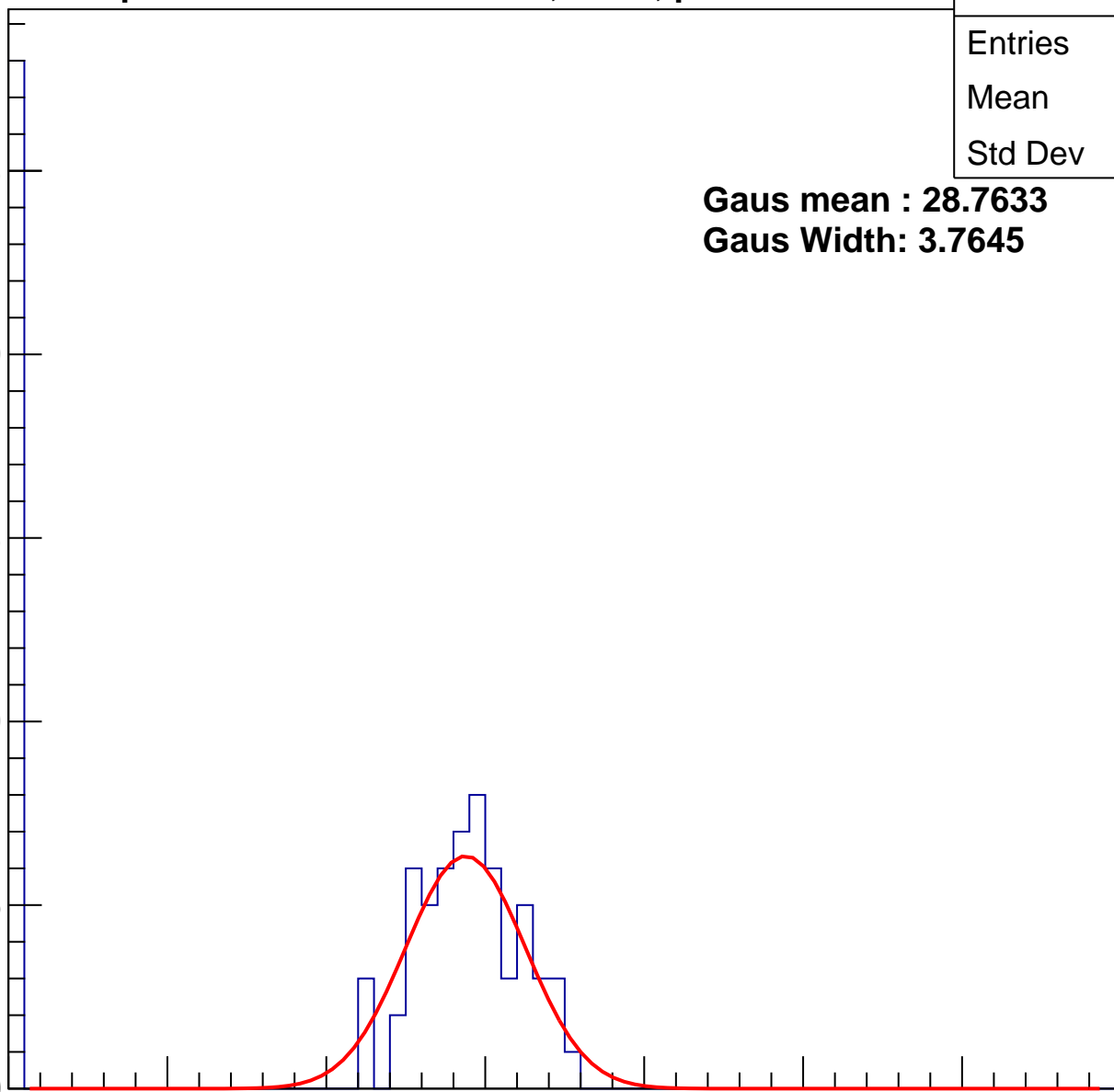
40

50

60

70

ampl



# B1L103S, U3-ch46, adc1

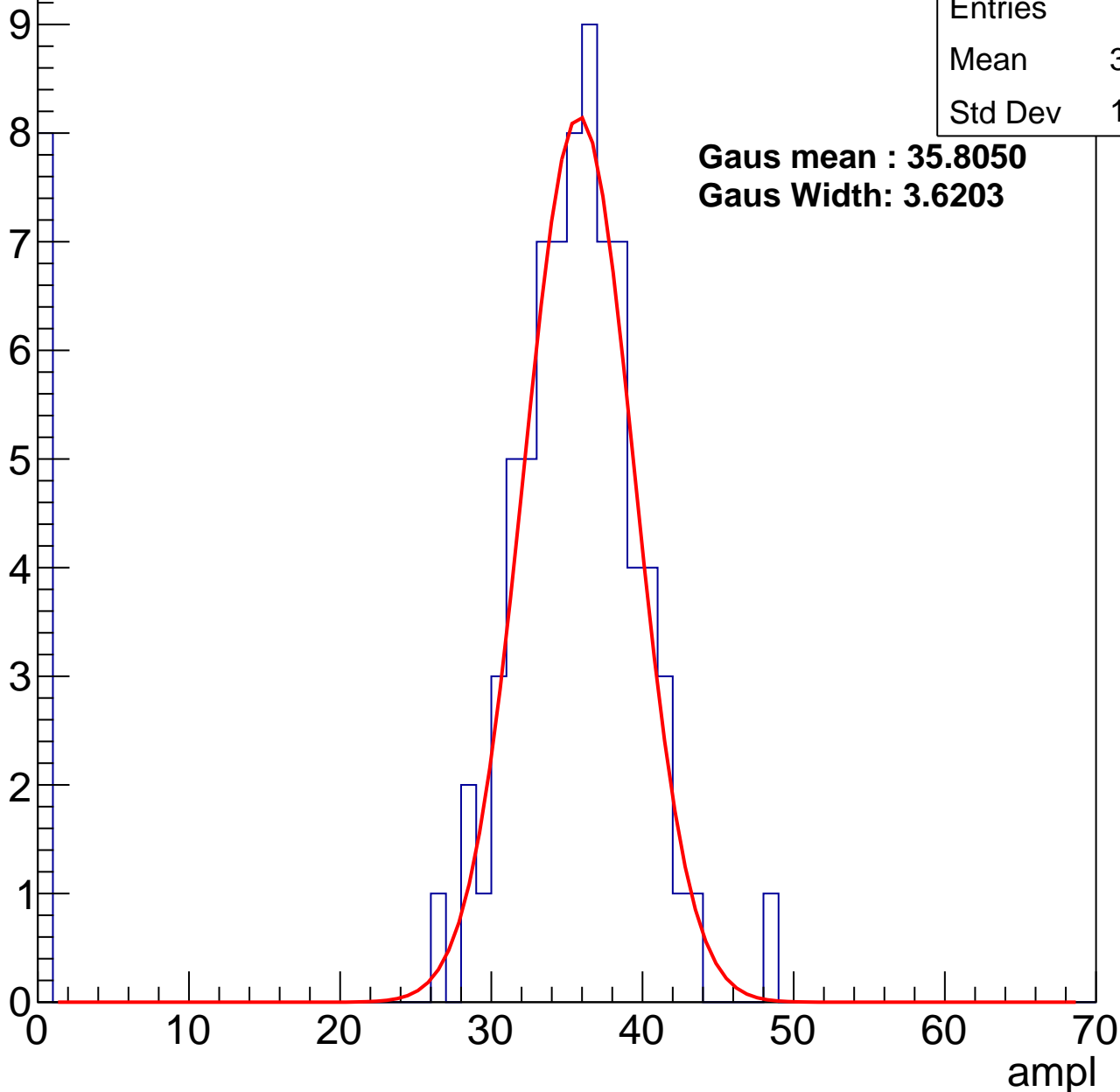
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	84
Mean	31.98
Std Dev	10.98

**Gaus mean : 35.8050**

**Gaus Width: 3.6203**



# B1L103S, U3-ch46, adc2

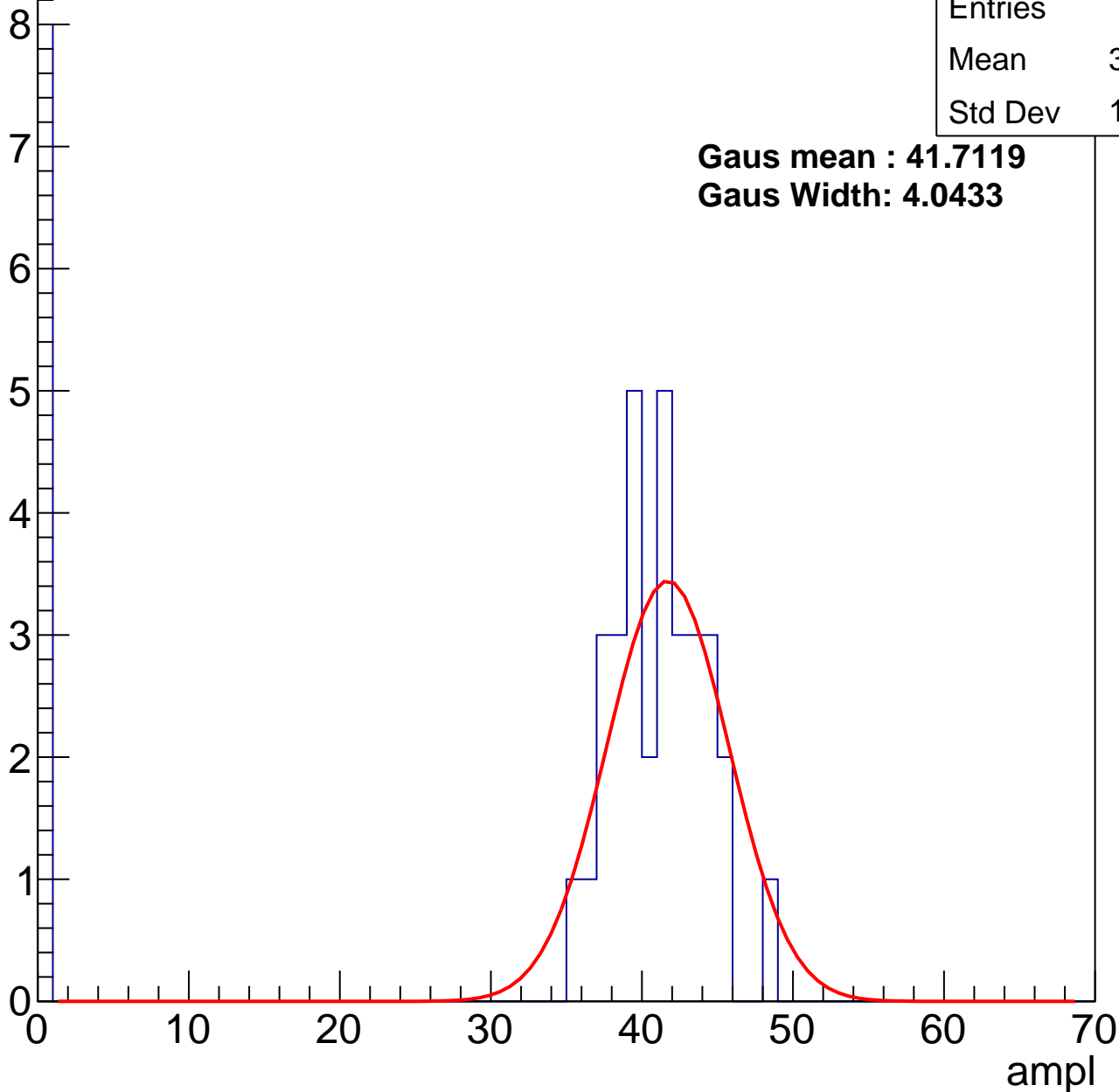
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	40
Mean	32.52
Std Dev	16.47

**Gaus mean : 41.7119**

**Gaus Width: 4.0433**



# B1L103S, U3-ch46, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	90
Mean	45.14
Std Dev	9.171

Entry

10

8

6

4

2

0

0

10

20

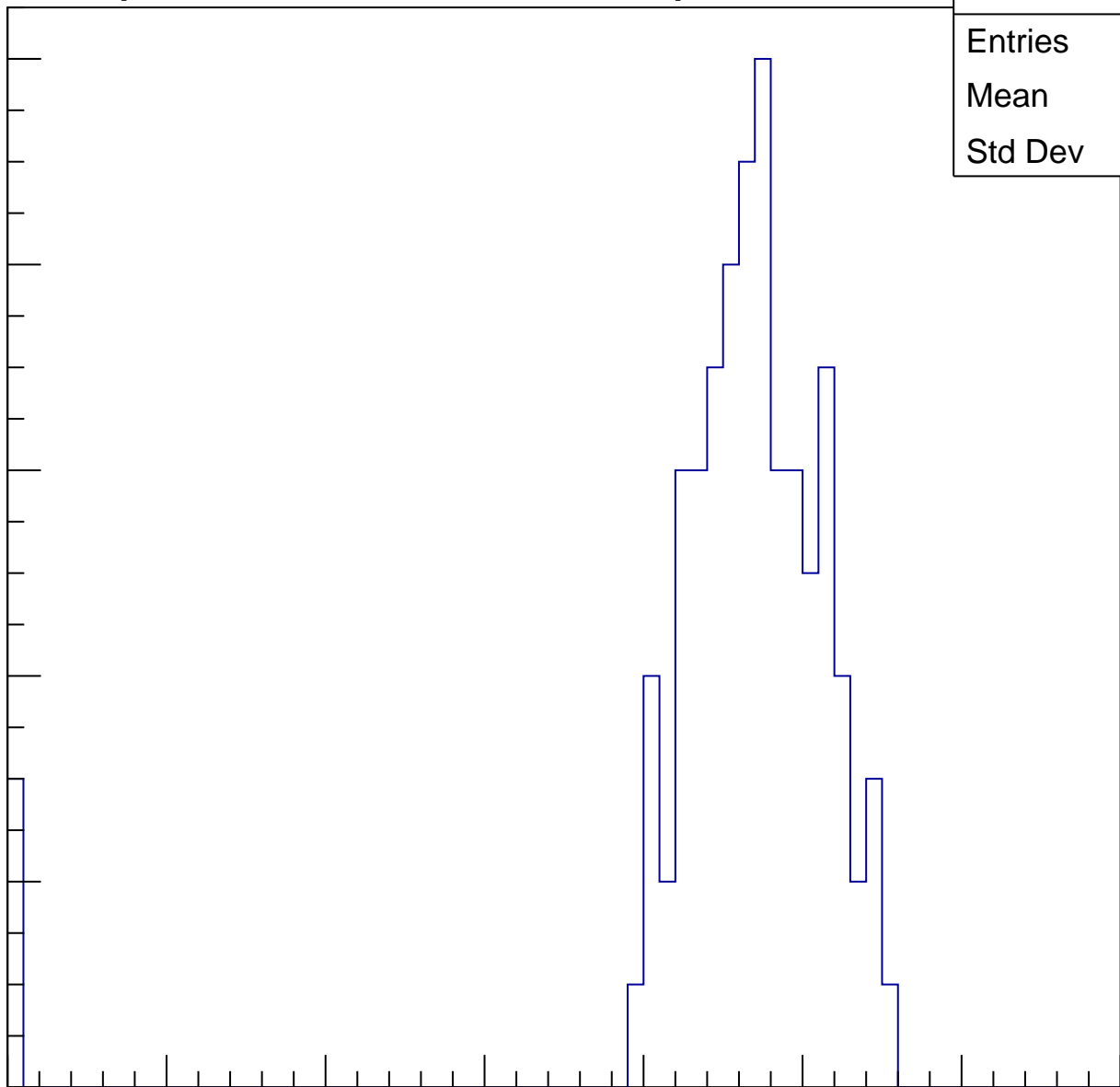
30

40

50

60

ampl

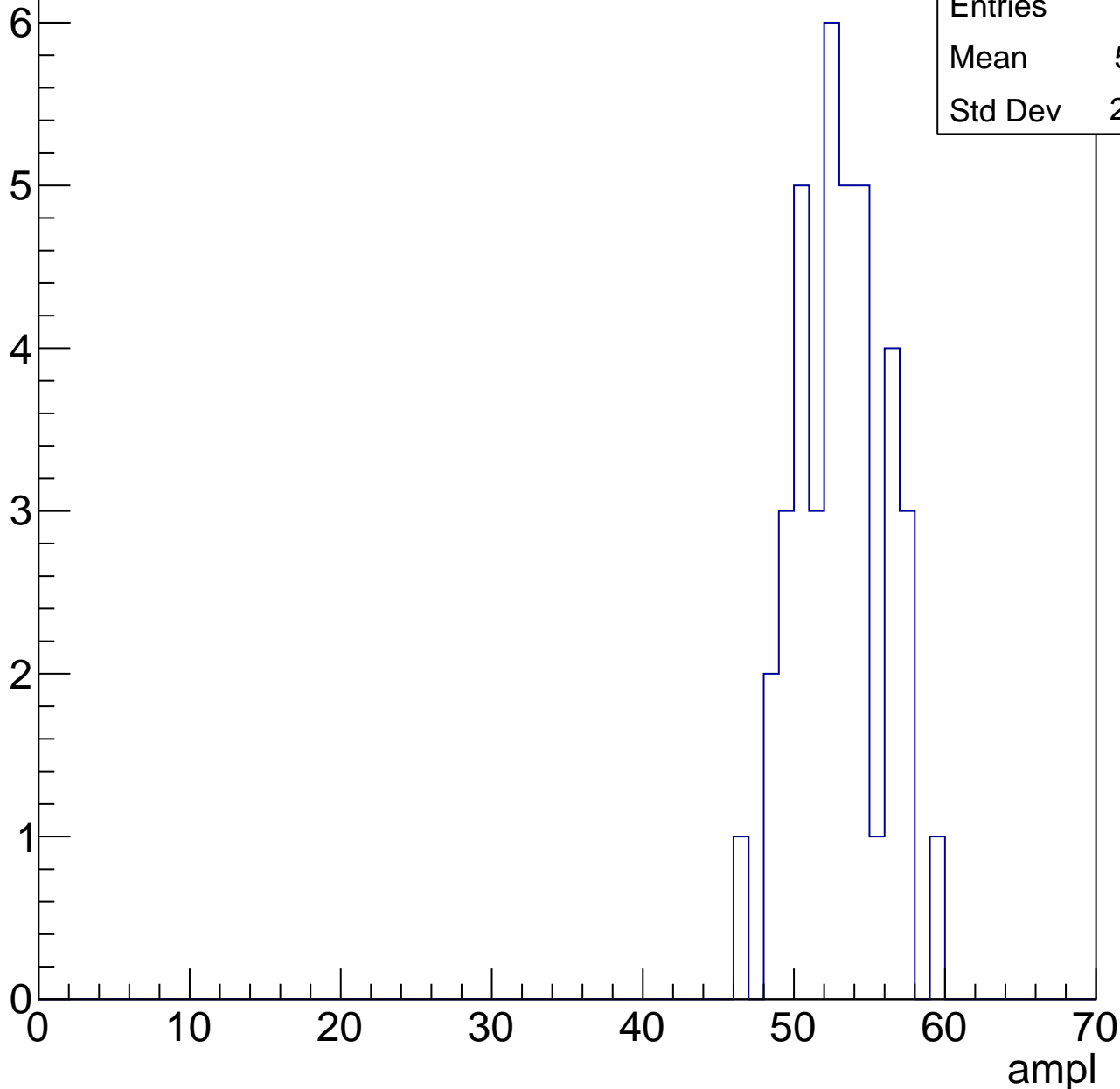


# B1L103S, U3-ch46, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	39
Mean	52.51
Std Dev	2.908

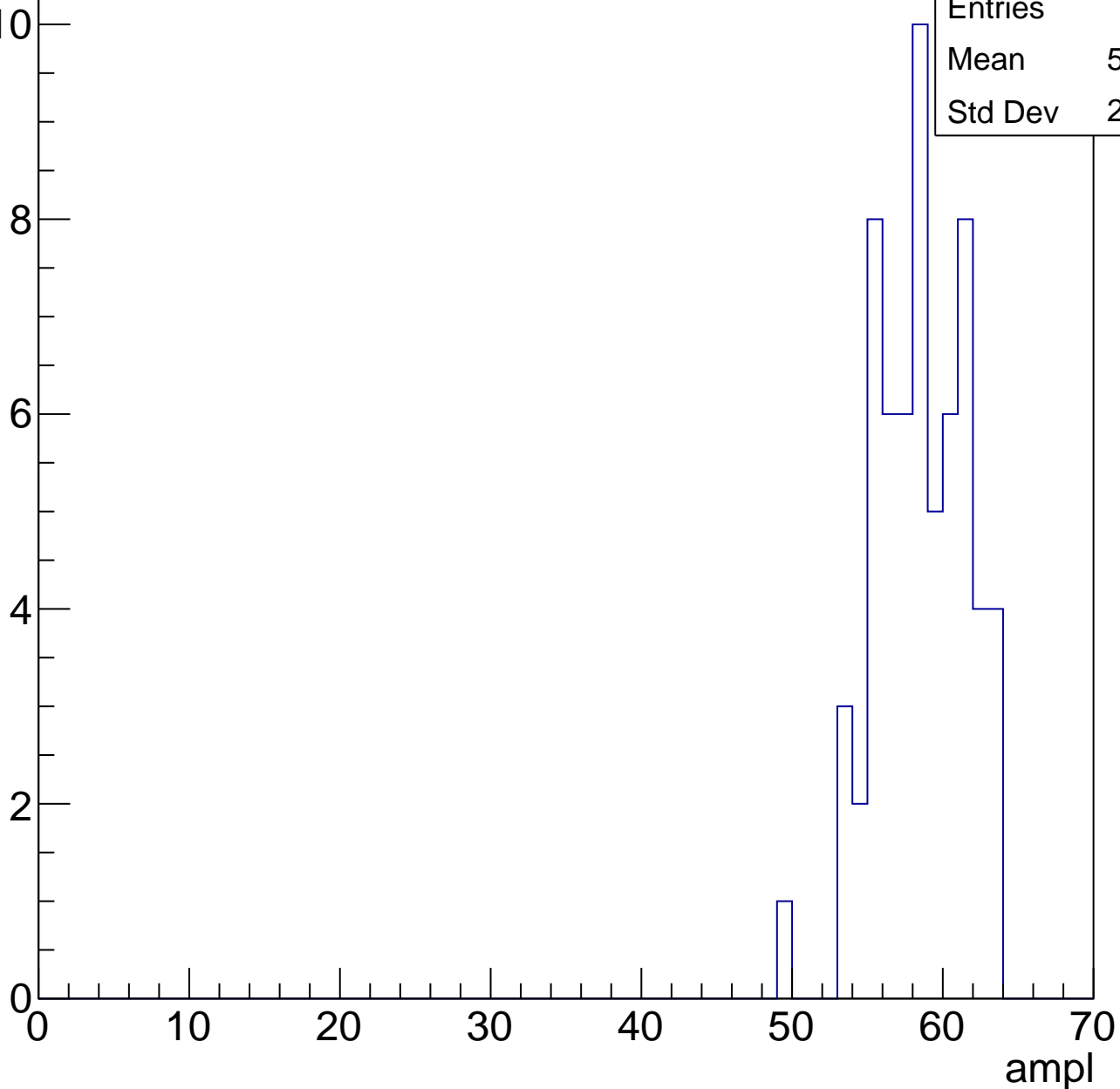


# B1L103S, U3-ch46, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	58.05
Std Dev	2.968

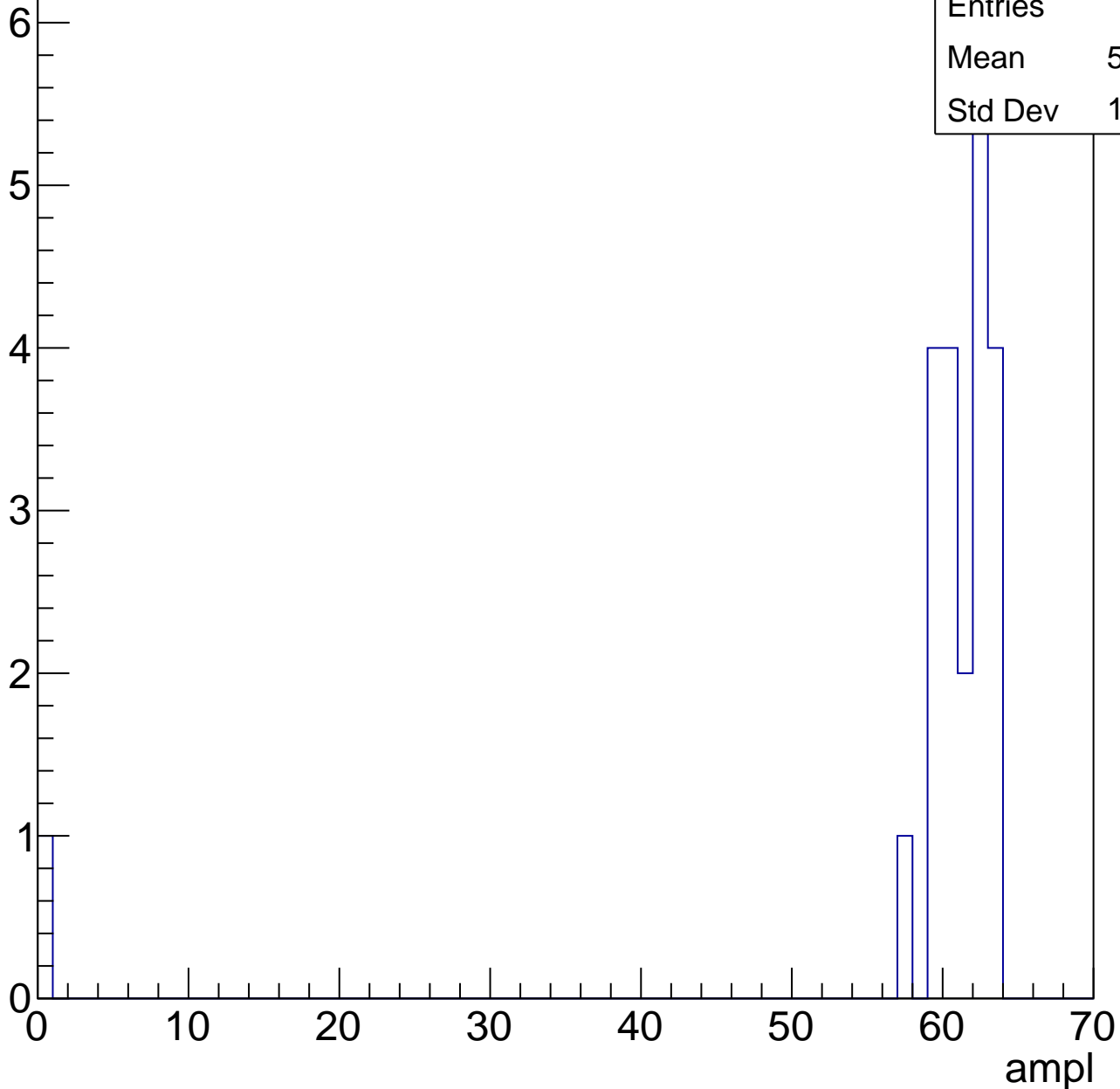


# B1L103S, U3-ch46, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	22
Mean	58.14
Std Dev	12.79





# B1L103S, U3-ch46, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U3-ch47, adc0

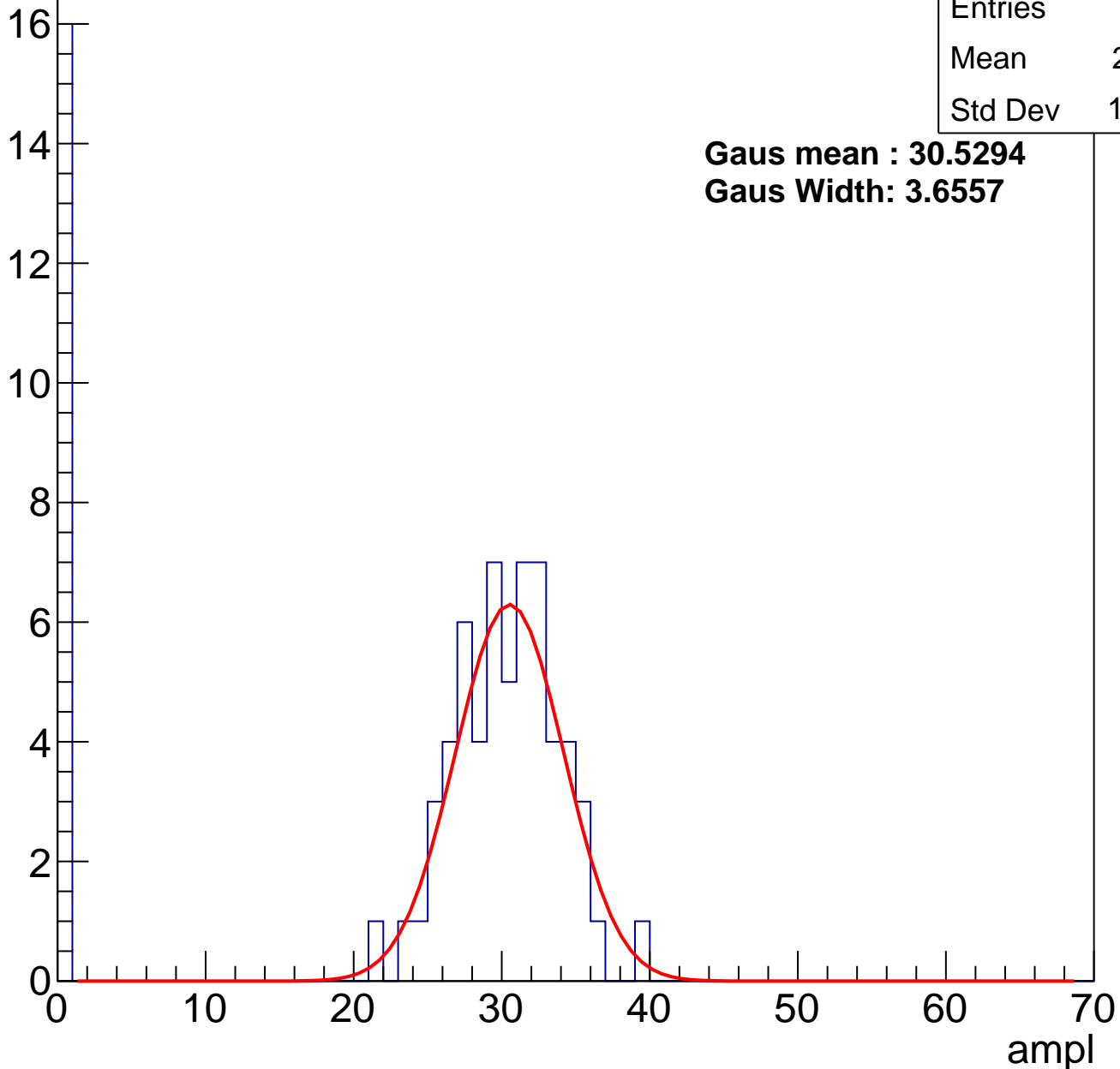
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	75
Mean	23.51
Std Dev	12.62

**Gaus mean : 30.5294**

**Gaus Width: 3.6557**

Entry



# B1L103S, U3-ch47, adc1

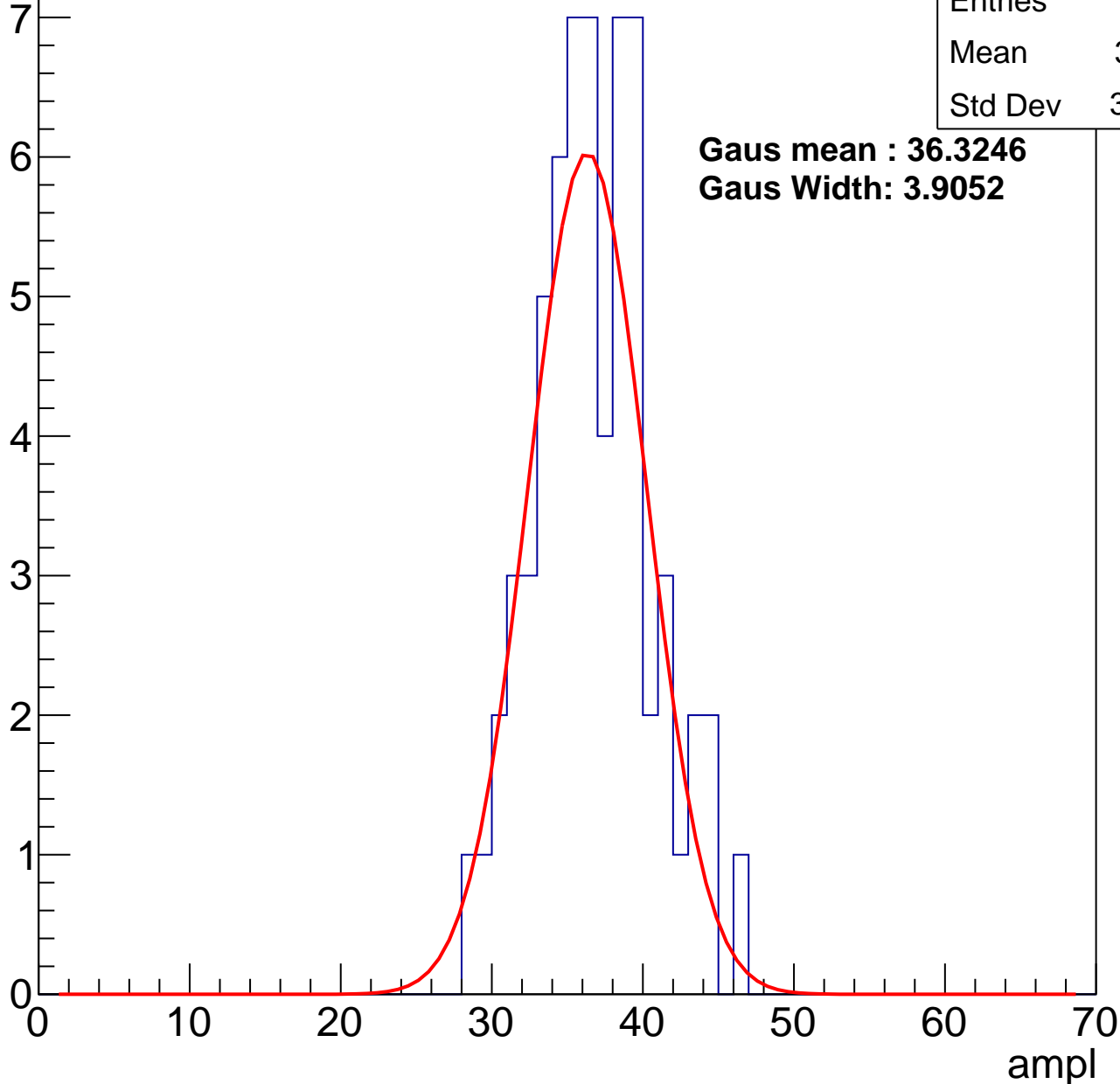
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	36.31
Std Dev	3.836

**Gaus mean : 36.3246**

**Gaus Width: 3.9052**



# B1L103S, U3-ch47, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	81
Mean	36.64
Std Dev	14.87

**Gaus mean : 42.9901**

**Gaus Width: 3.2308**

Entry

10

8

6

4

2

0

0

10

20

30

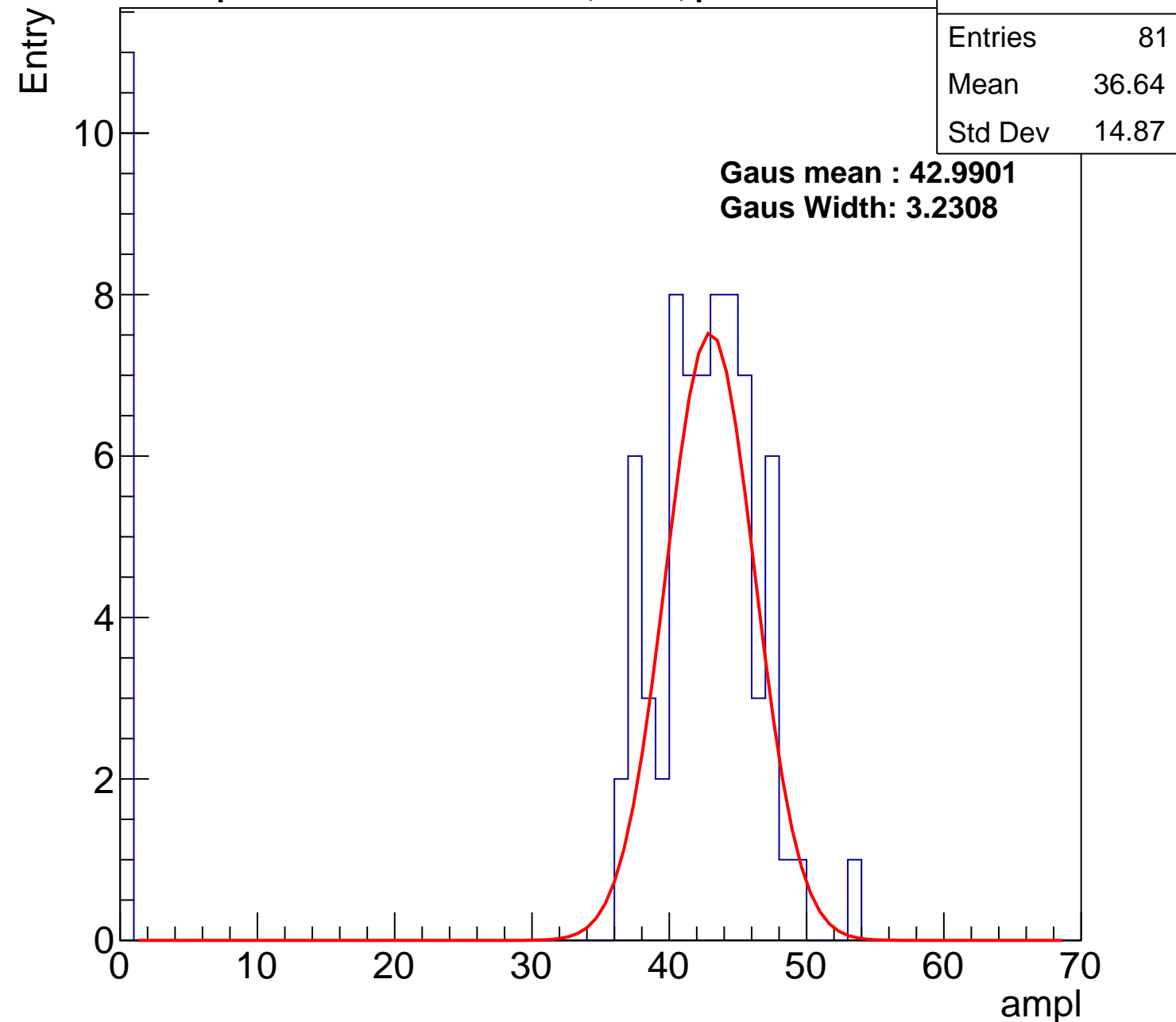
40

50

60

70

ampl

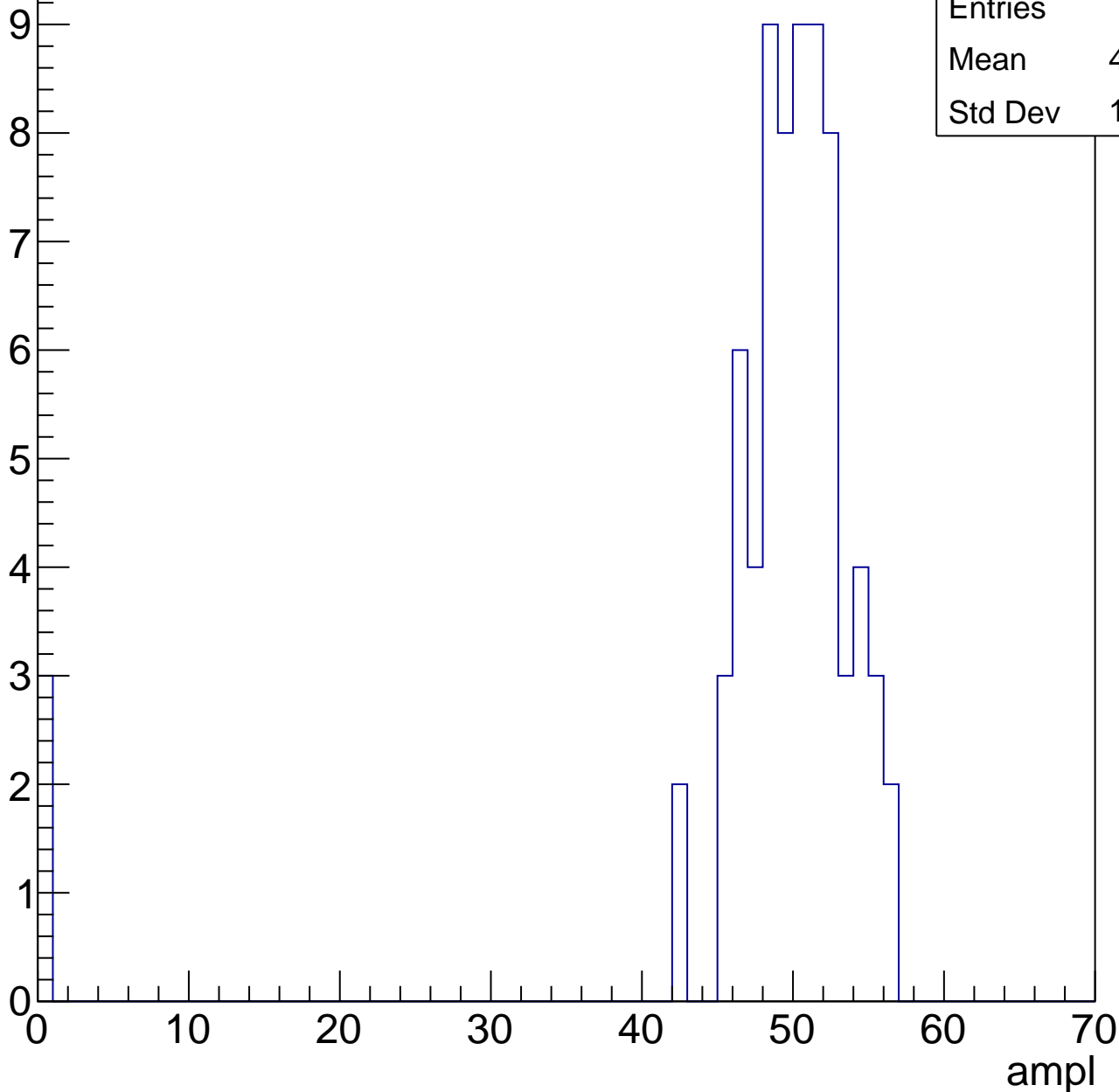


# B1L103S, U3-ch47, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	47.73
Std Dev	10.32

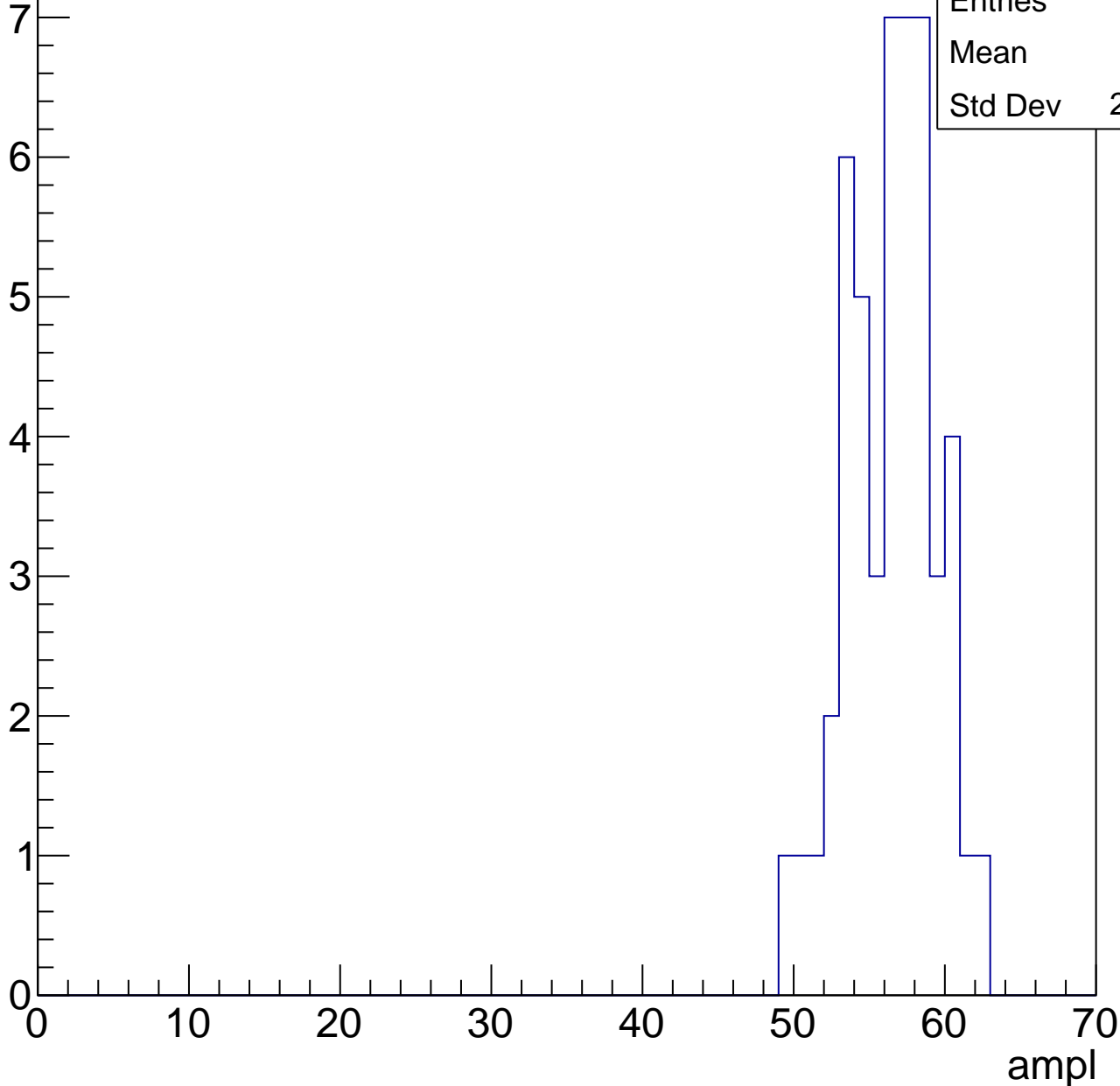


# B1L103S, U3-ch47, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	49
Mean	56
Std Dev	2.878

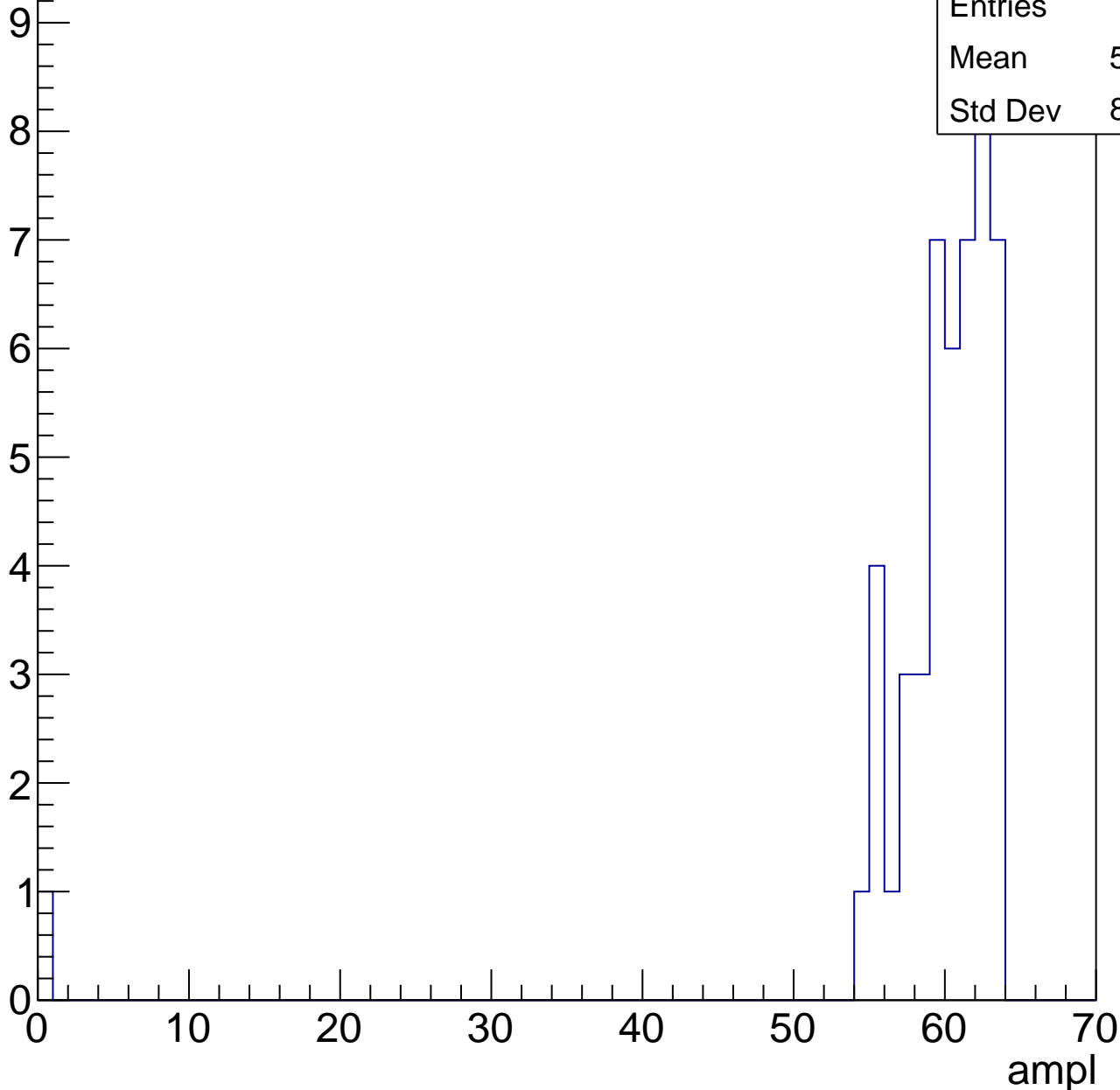


# B1L103S, U3-ch47, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

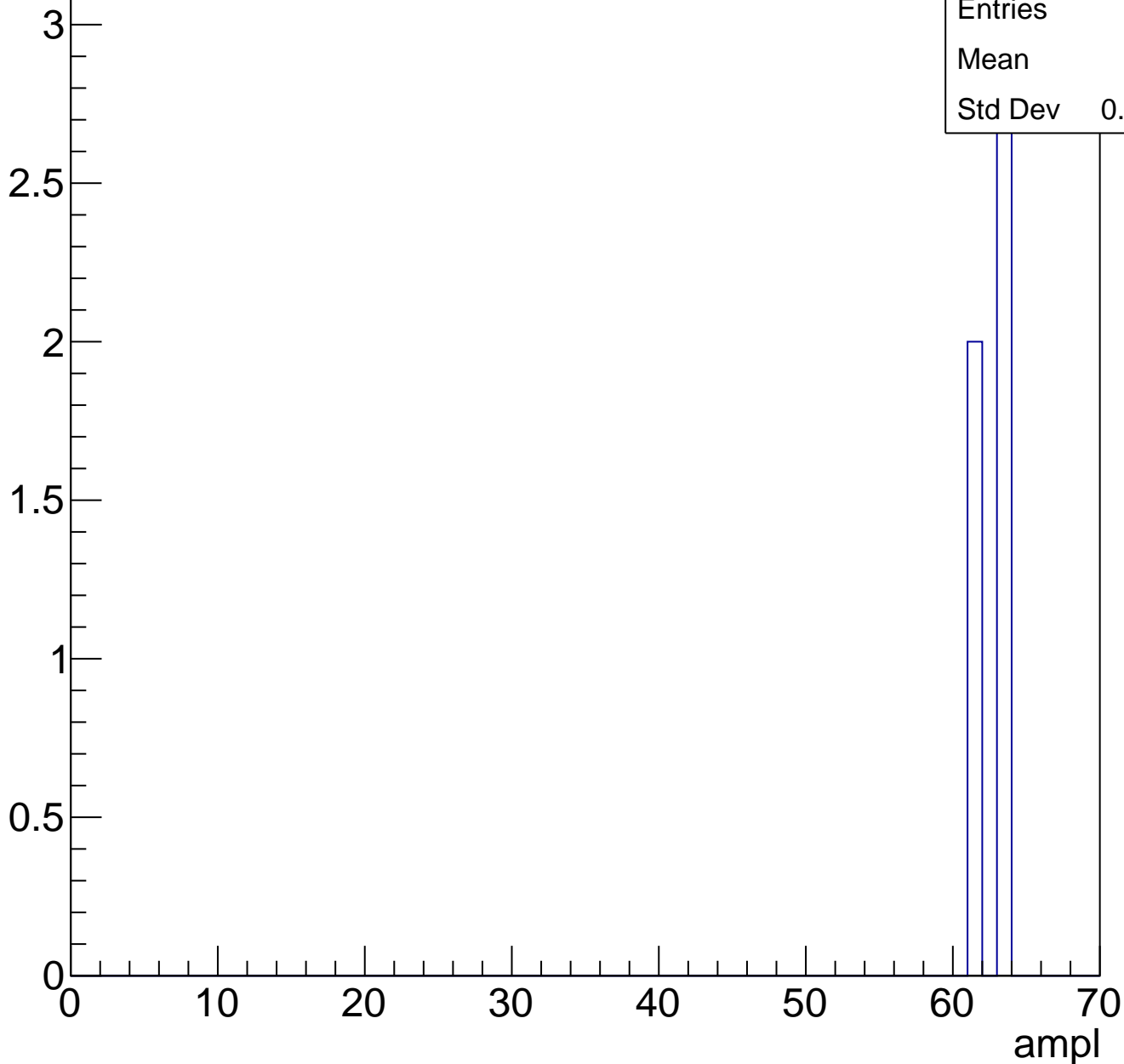
Entries	49
Mean	58.65
Std Dev	8.824



# B1L103S, U3-ch47, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U3-ch47, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	19
Mean	0
Std Dev	0

ampl

# B1L103S, U3-ch48, adc0

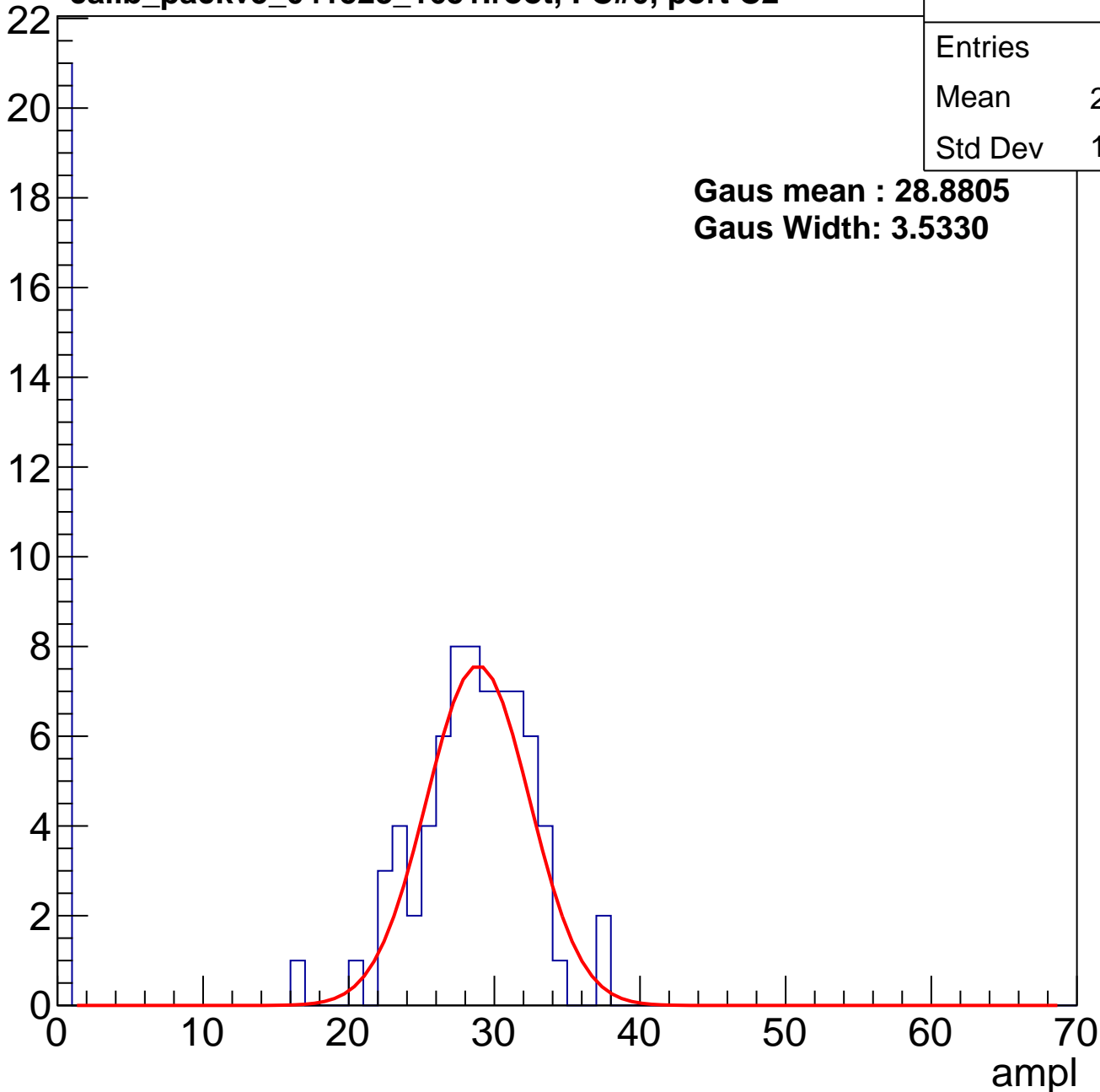
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	92
Mean	21.74
Std Dev	12.28

**Gaus mean : 28.8805**

**Gaus Width: 3.5330**

Entry



# B1L103S, U3-ch48, adc1

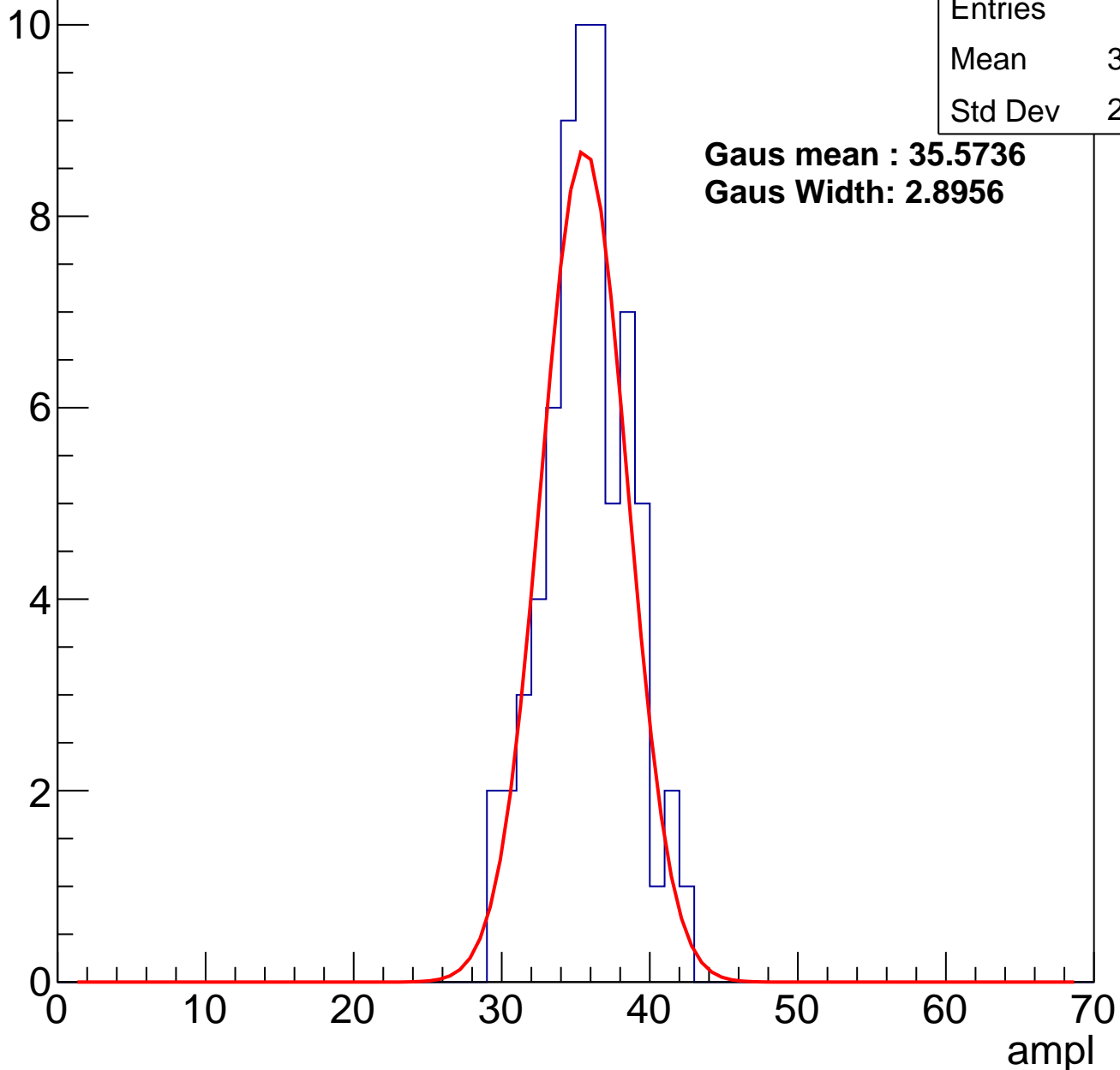
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	67
Mean	35.27
Std Dev	2.873

**Gaus mean : 35.5736**

**Gaus Width: 2.8956**

Entry



# B1L103S, U3-ch48, adc2

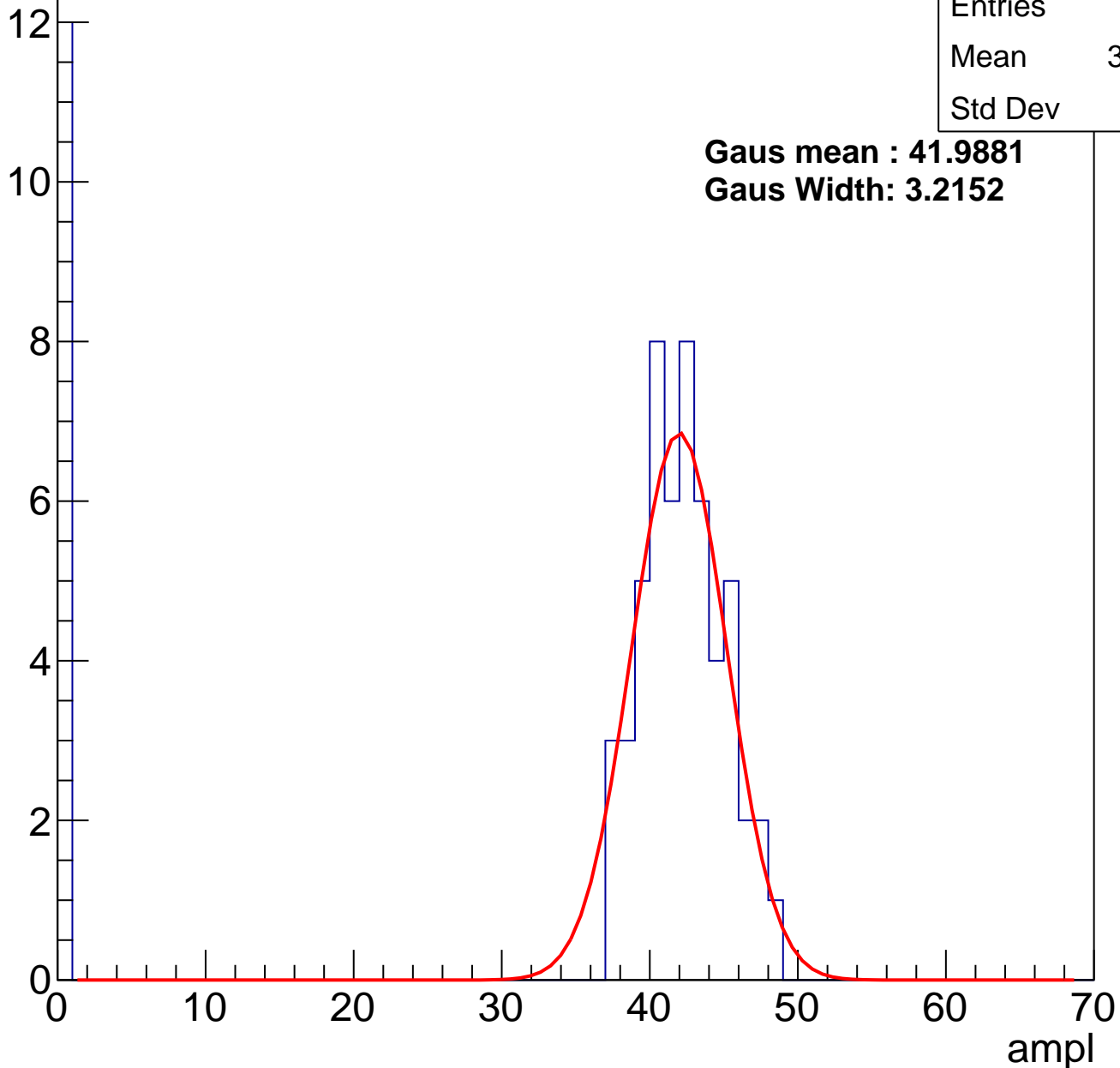
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	65
Mean	34.08
Std Dev	16.4

**Gaus mean : 41.9881**

**Gaus Width: 3.2152**

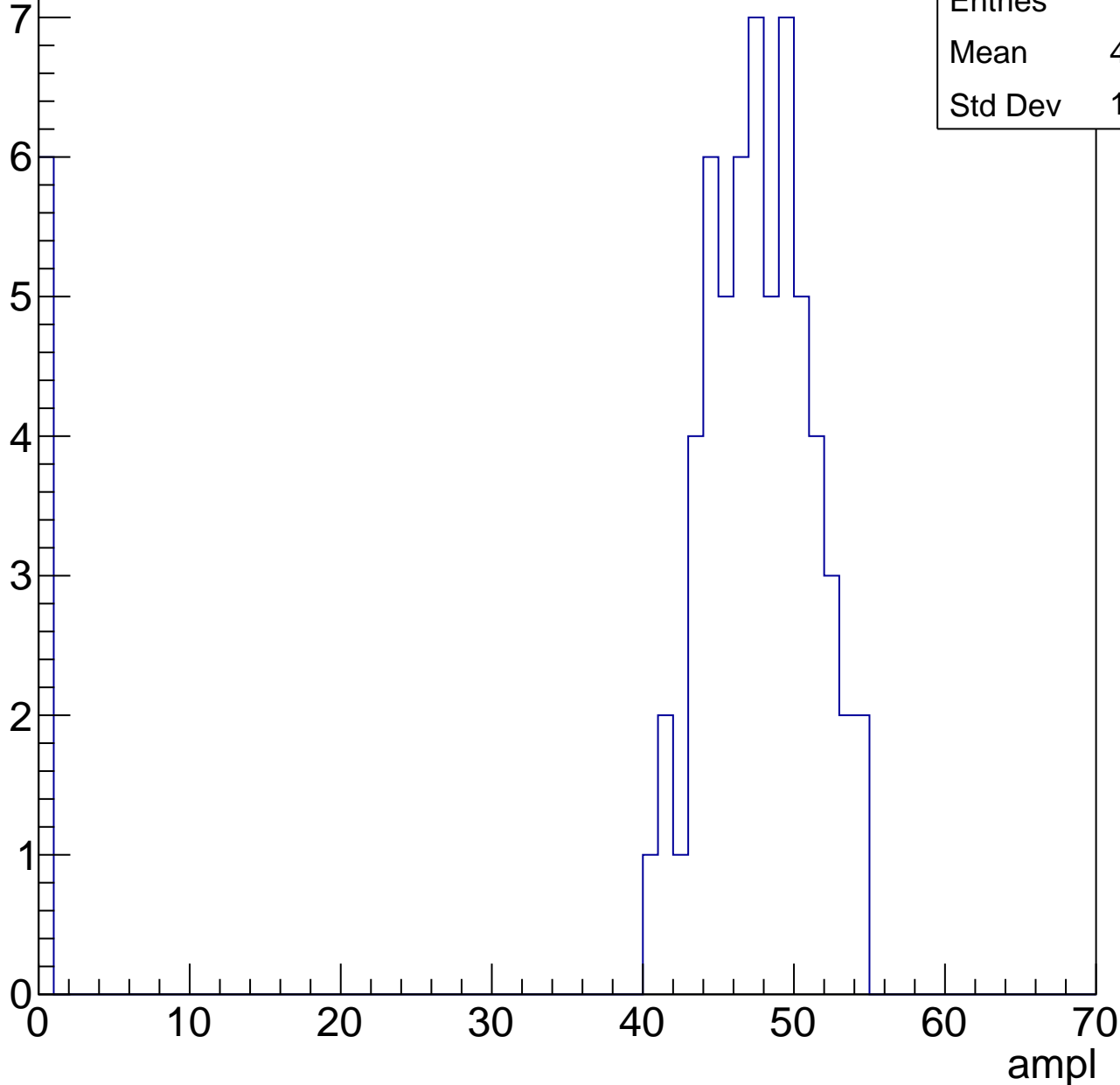
Entry



# B1L103S, U3-ch48, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

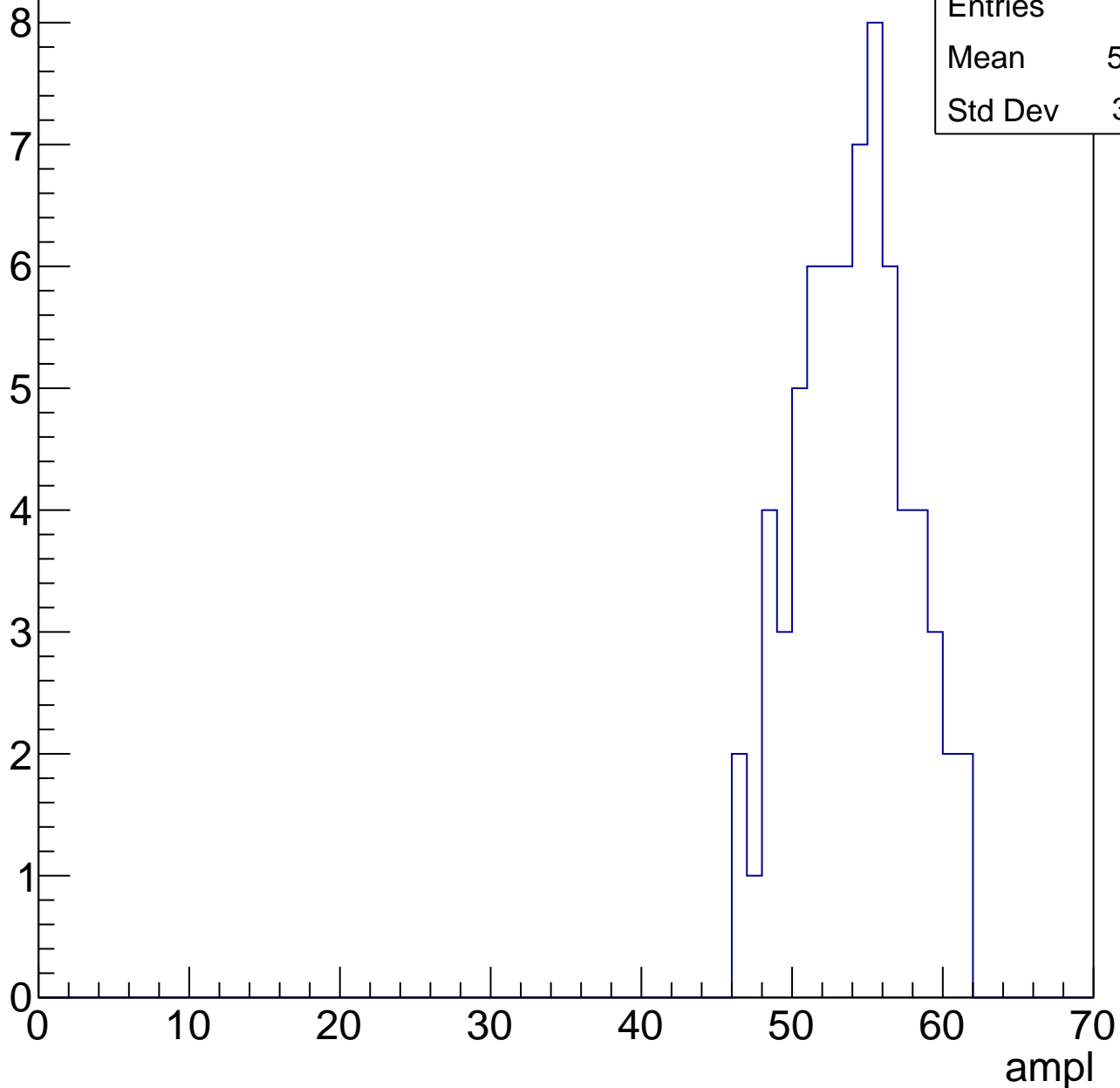
Entry



# B1L103S, U3-ch48, adc4

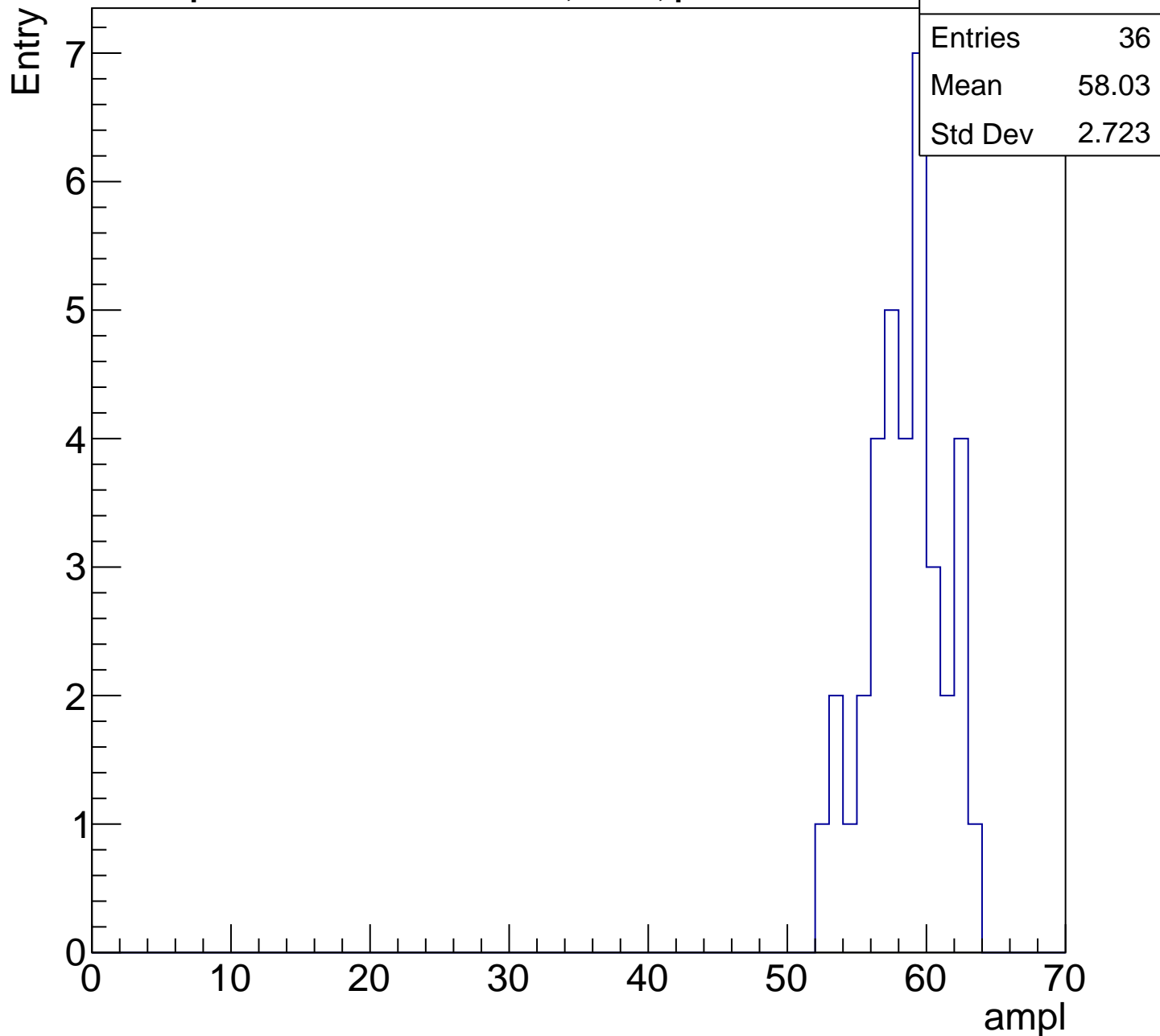
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U3-ch48, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

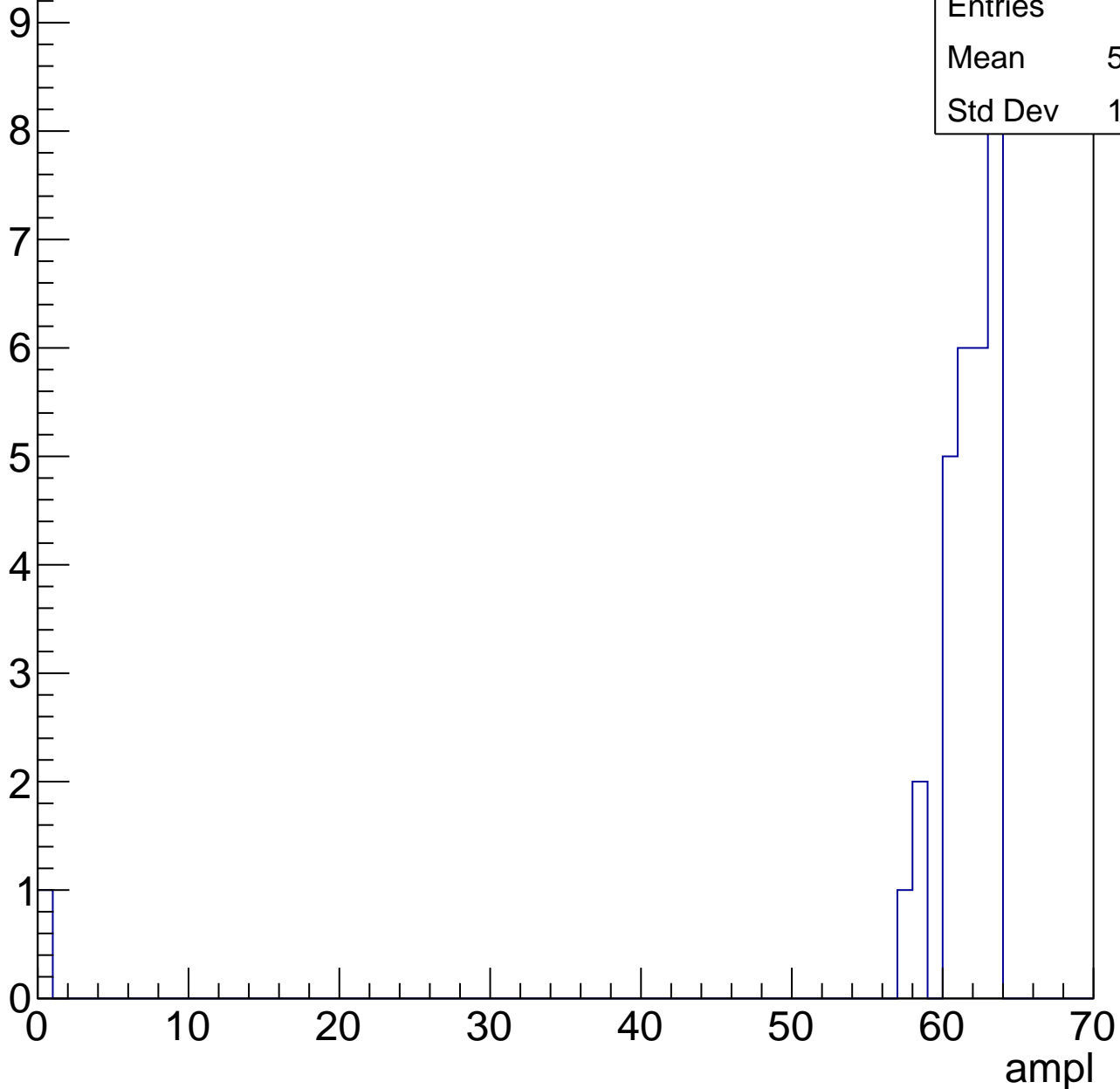


# B1L103S, U3-ch48, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	30
Mean	59.27
Std Dev	11.12

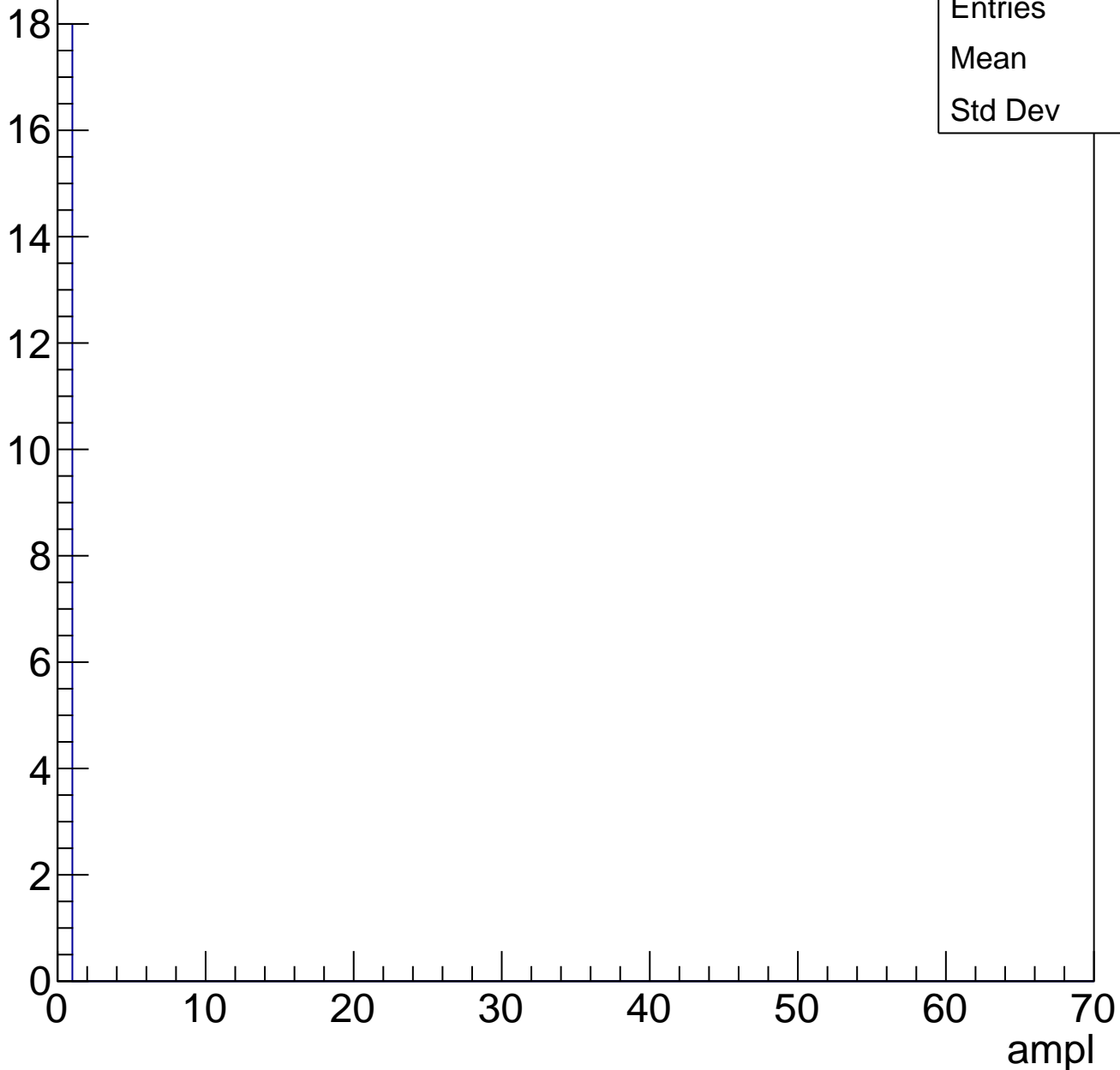




# B1L103S, U3-ch48, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U3-ch49, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	81
Mean	24.85
Std Dev	10.31

**Gaus mean : 29.2720**

**Gaus Width: 3.7049**

Entry

10

8

6

4

2

0

0

10

20

30

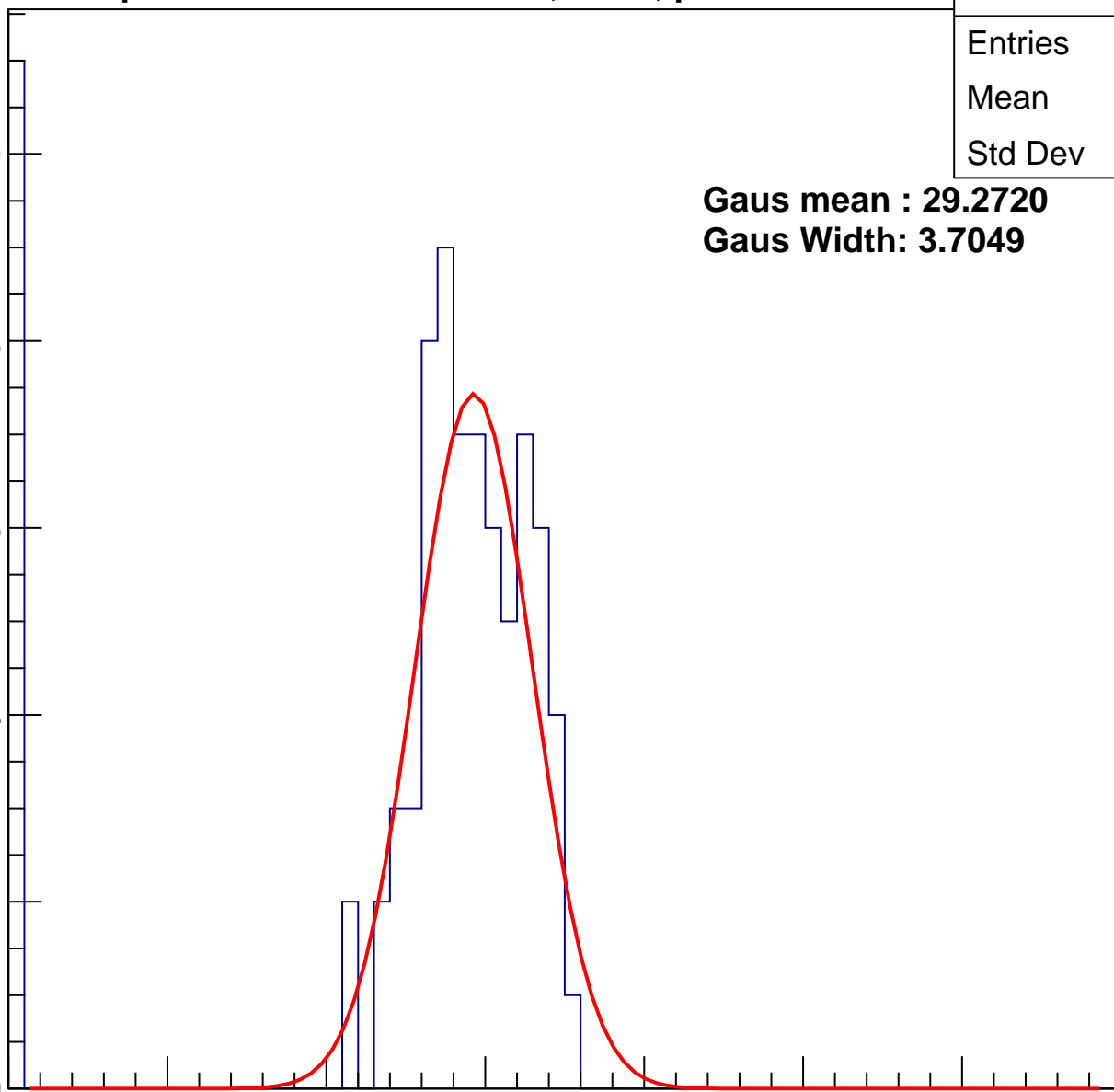
40

50

60

70

ampl



# B1L103S, U3-ch49, adc1

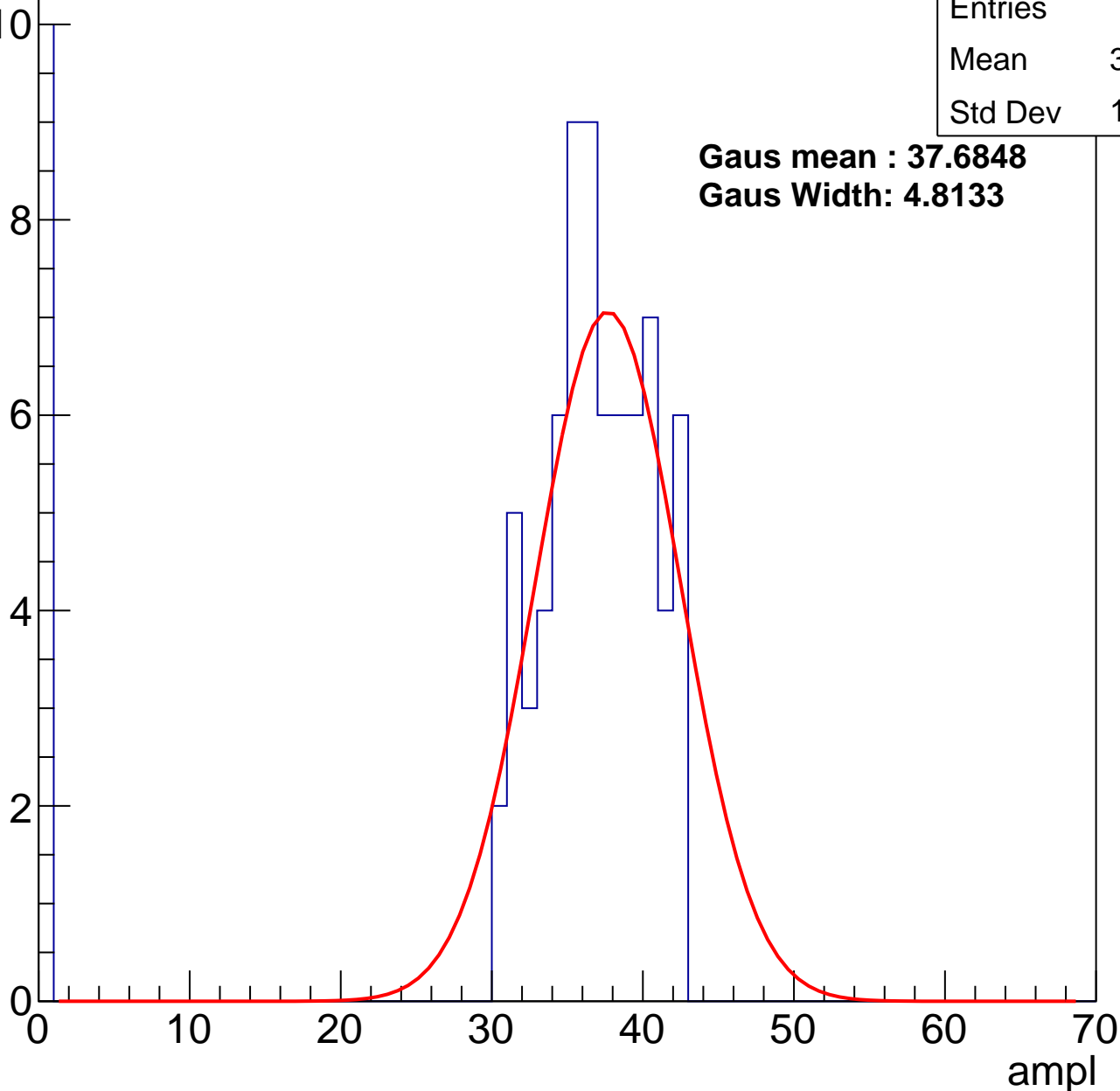
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	83
Mean	32.12
Std Dev	12.29

**Gaus mean : 37.6848**

**Gaus Width: 4.8133**



# B1L103S, U3-ch49, adc2

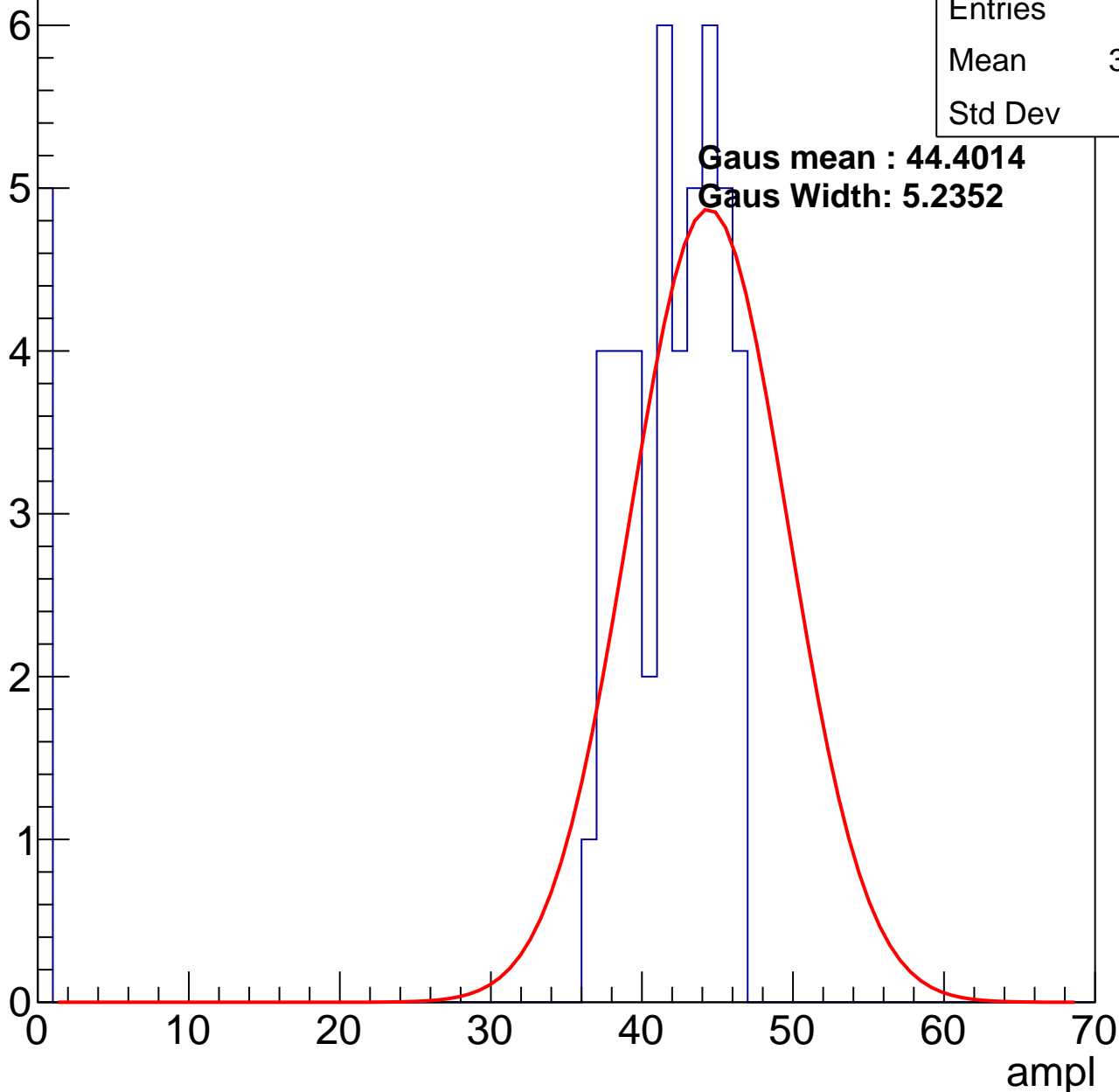
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	50
Mean	37.48
Std Dev	12.8

**Gaus mean : 44.4014**

**Gaus Width: 5.2352**

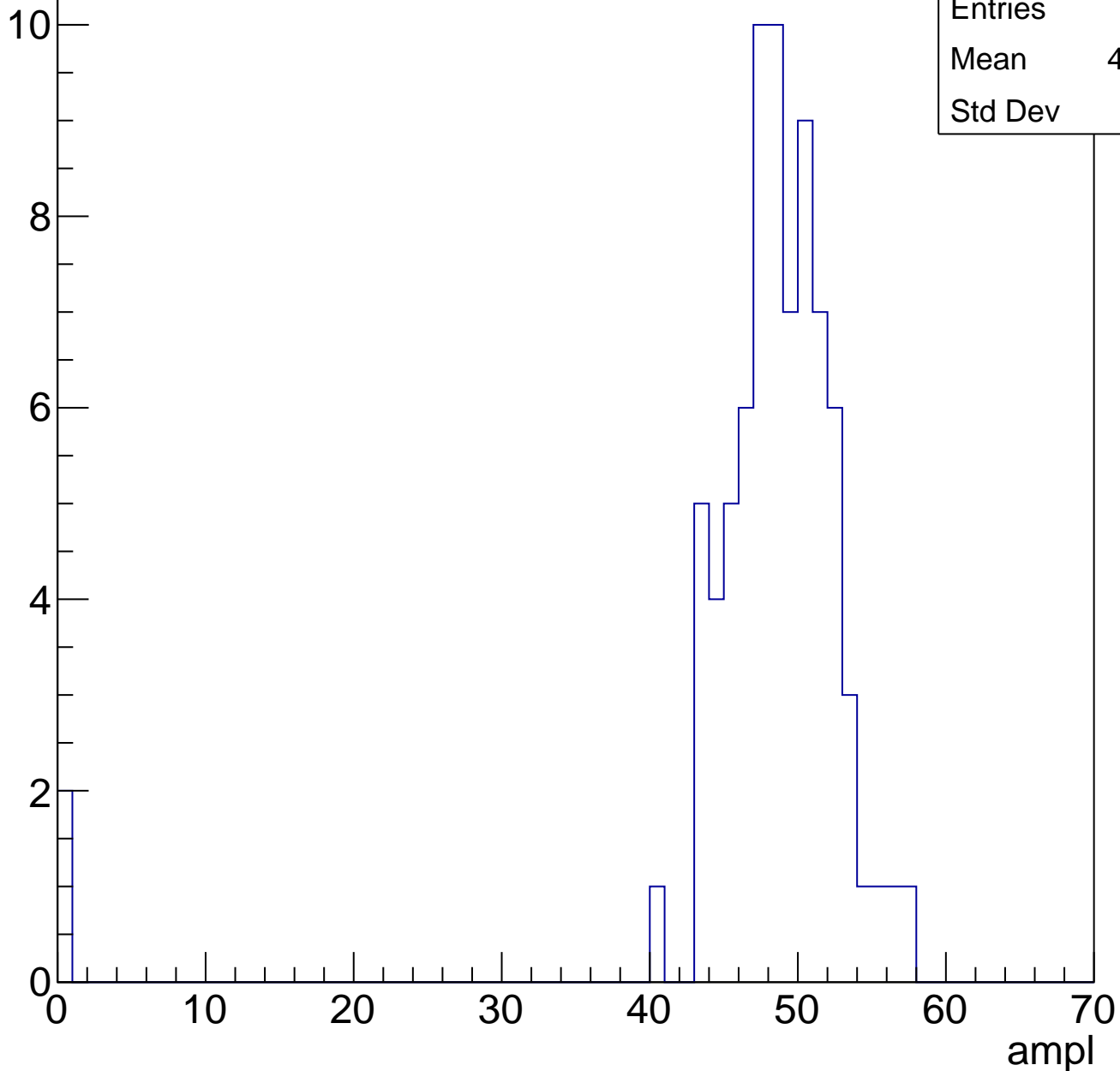


# B1L103S, U3-ch49, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	79
Mean	47.15
Std Dev	8.26

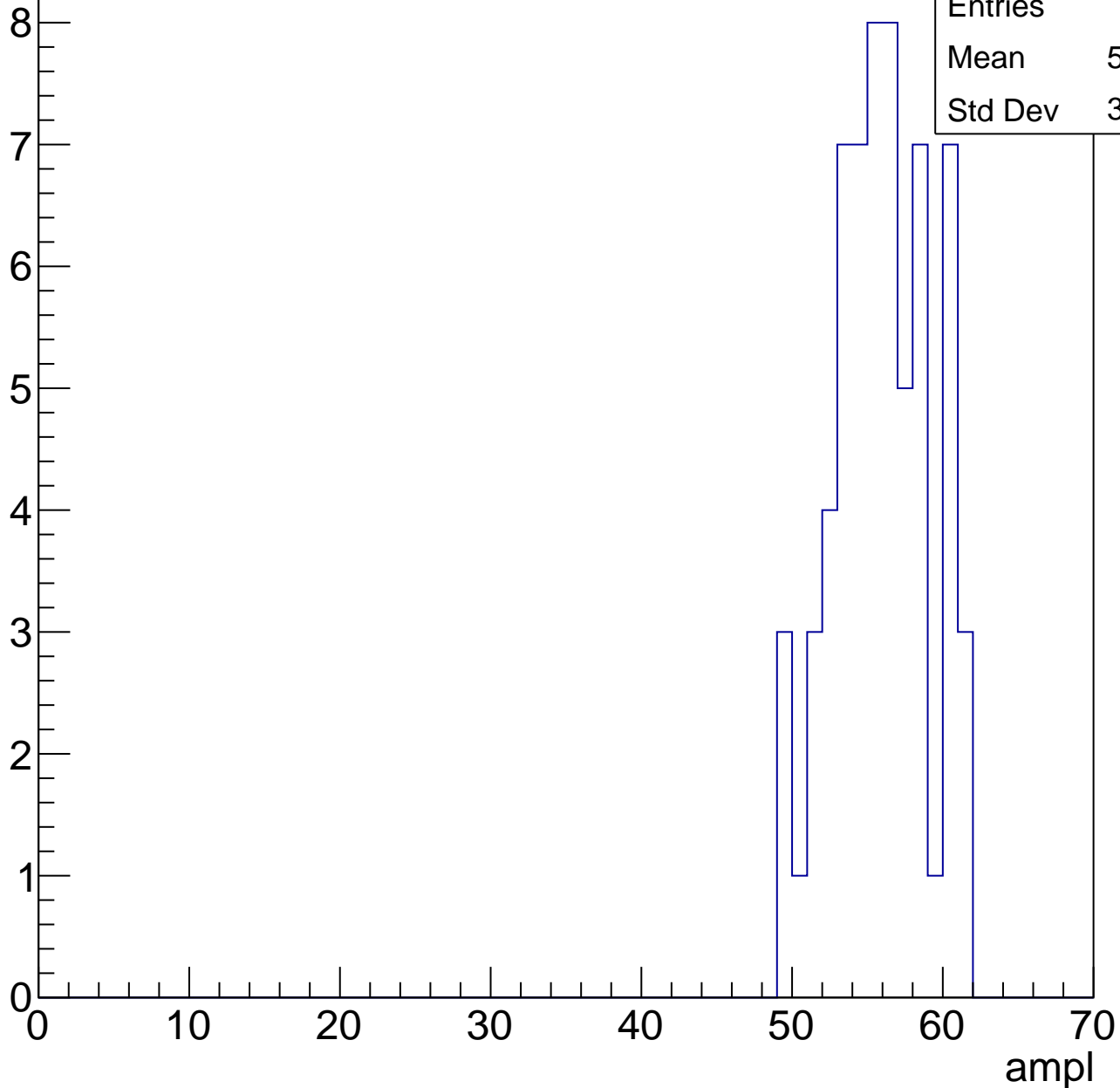
Entry



# B1L103S, U3-ch49, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

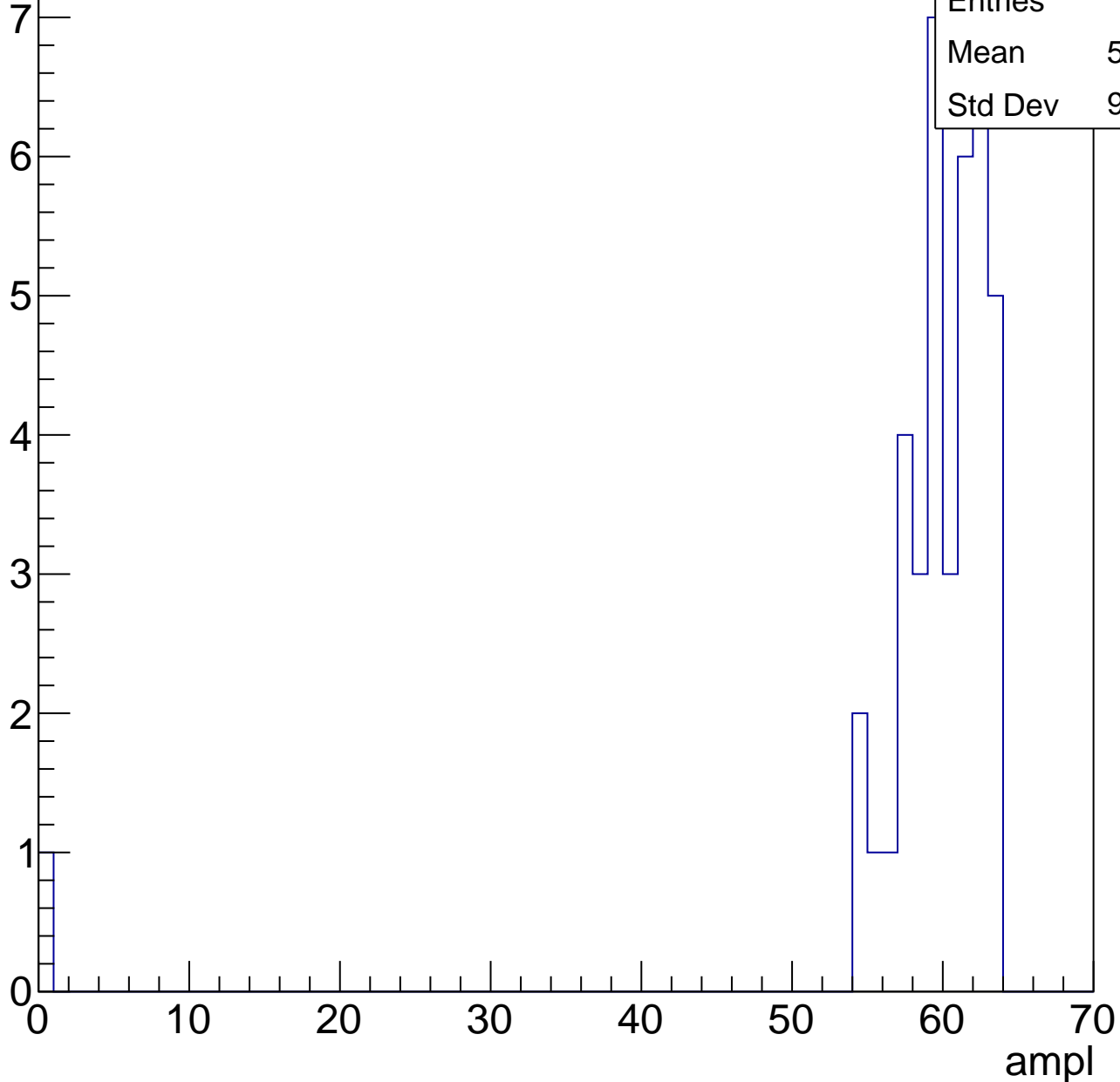


Entries	64
Mean	55.44
Std Dev	3.137

# B1L103S, U3-ch49, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

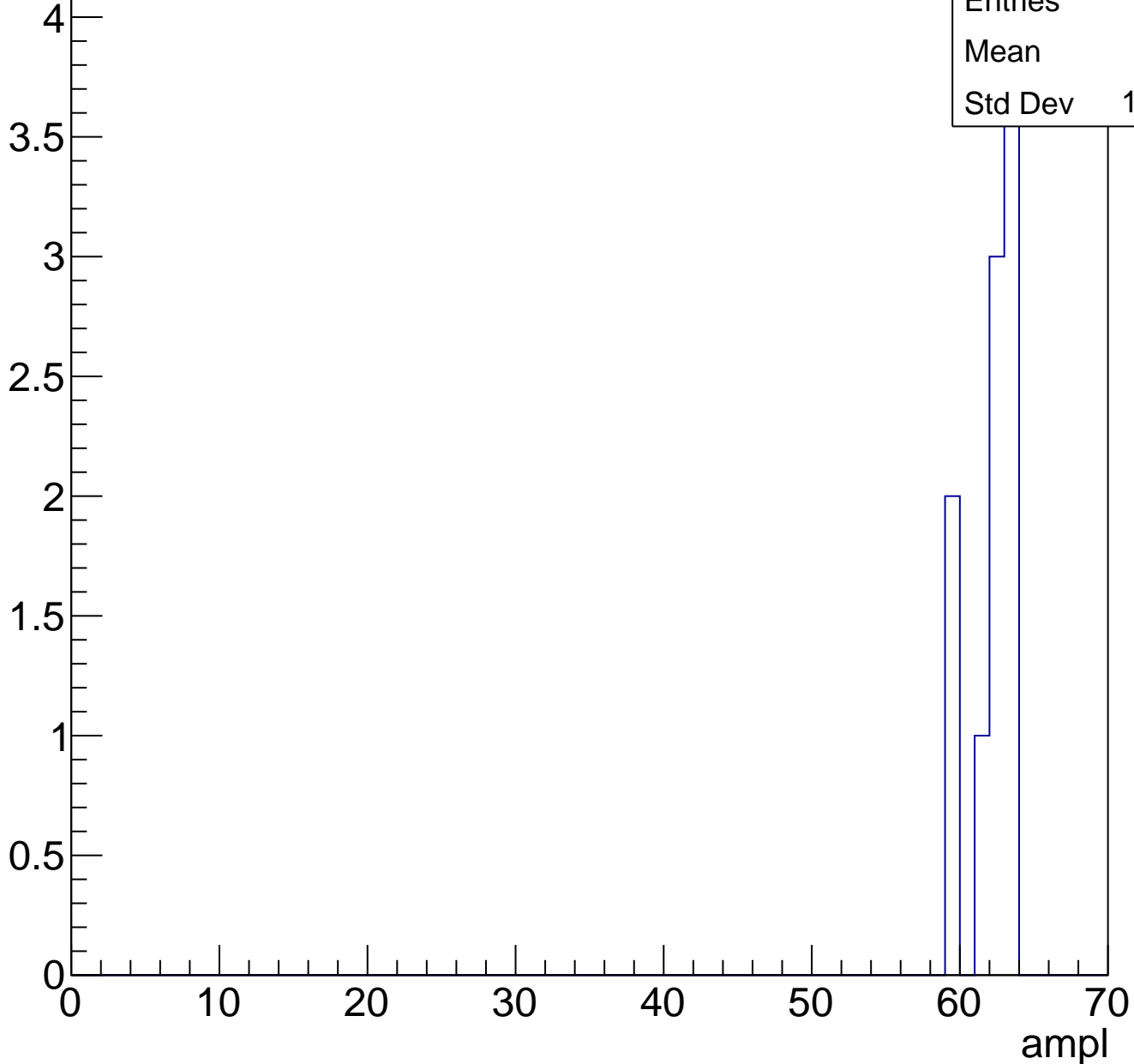
Entry



# B1L103S, U3-ch49, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



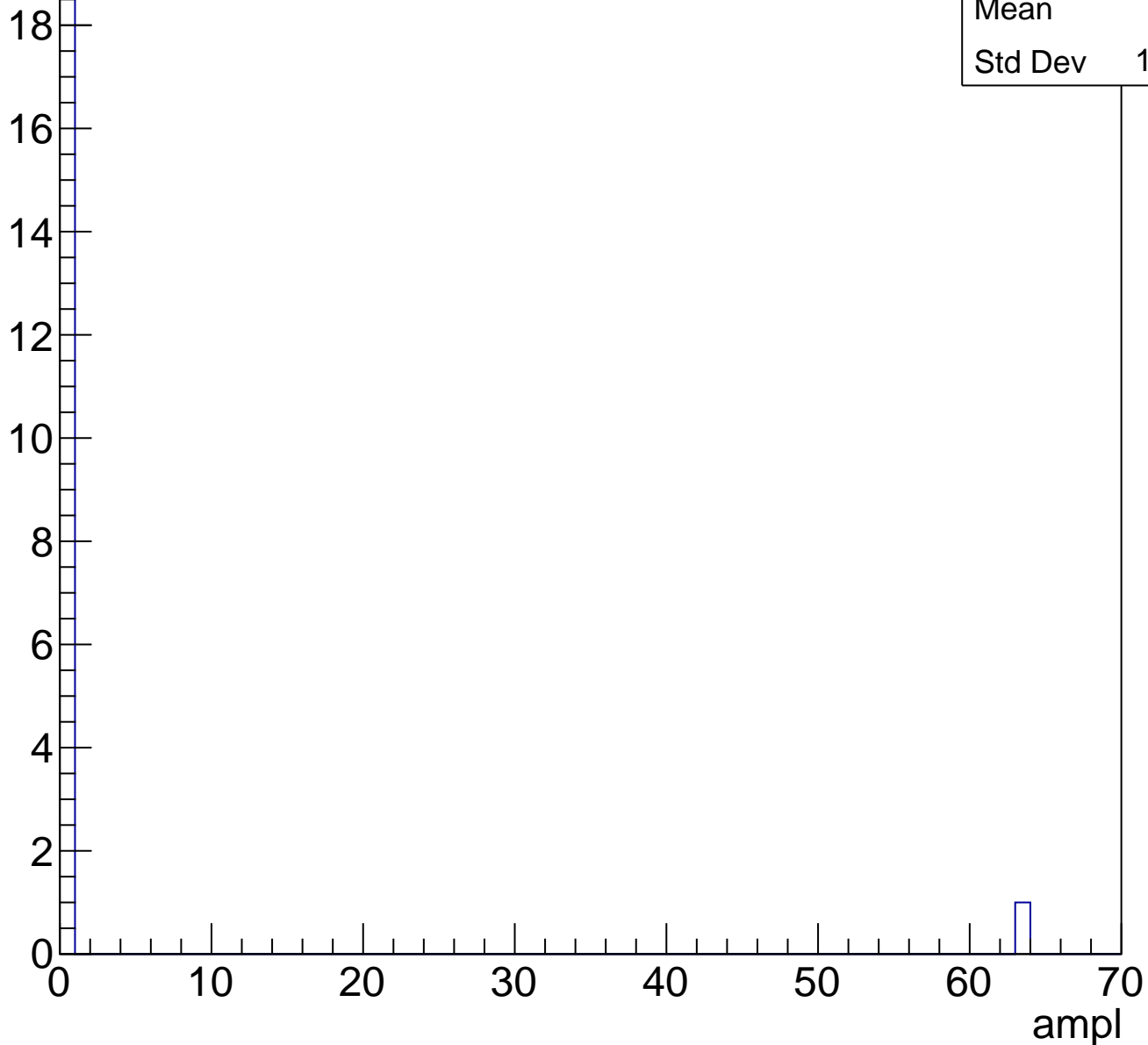
Entries	10
Mean	61.7
Std Dev	1.487



# B1L103S, U3-ch49, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U3-ch50, adc0

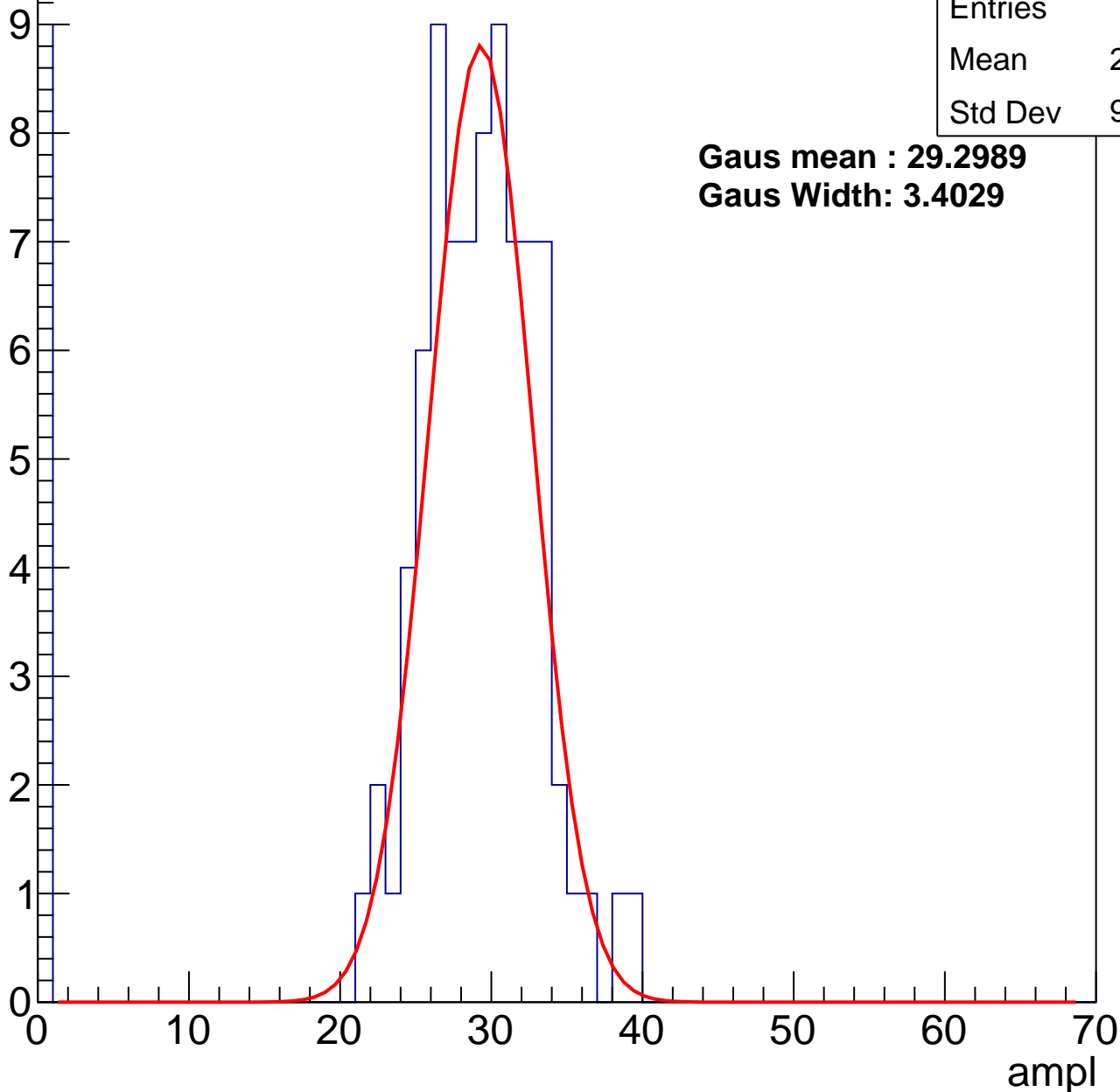
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	90
Mean	26.03
Std Dev	9.318

**Gaus mean : 29.2989**

**Gaus Width: 3.4029**



# B1L103S, U3-ch50, adc1

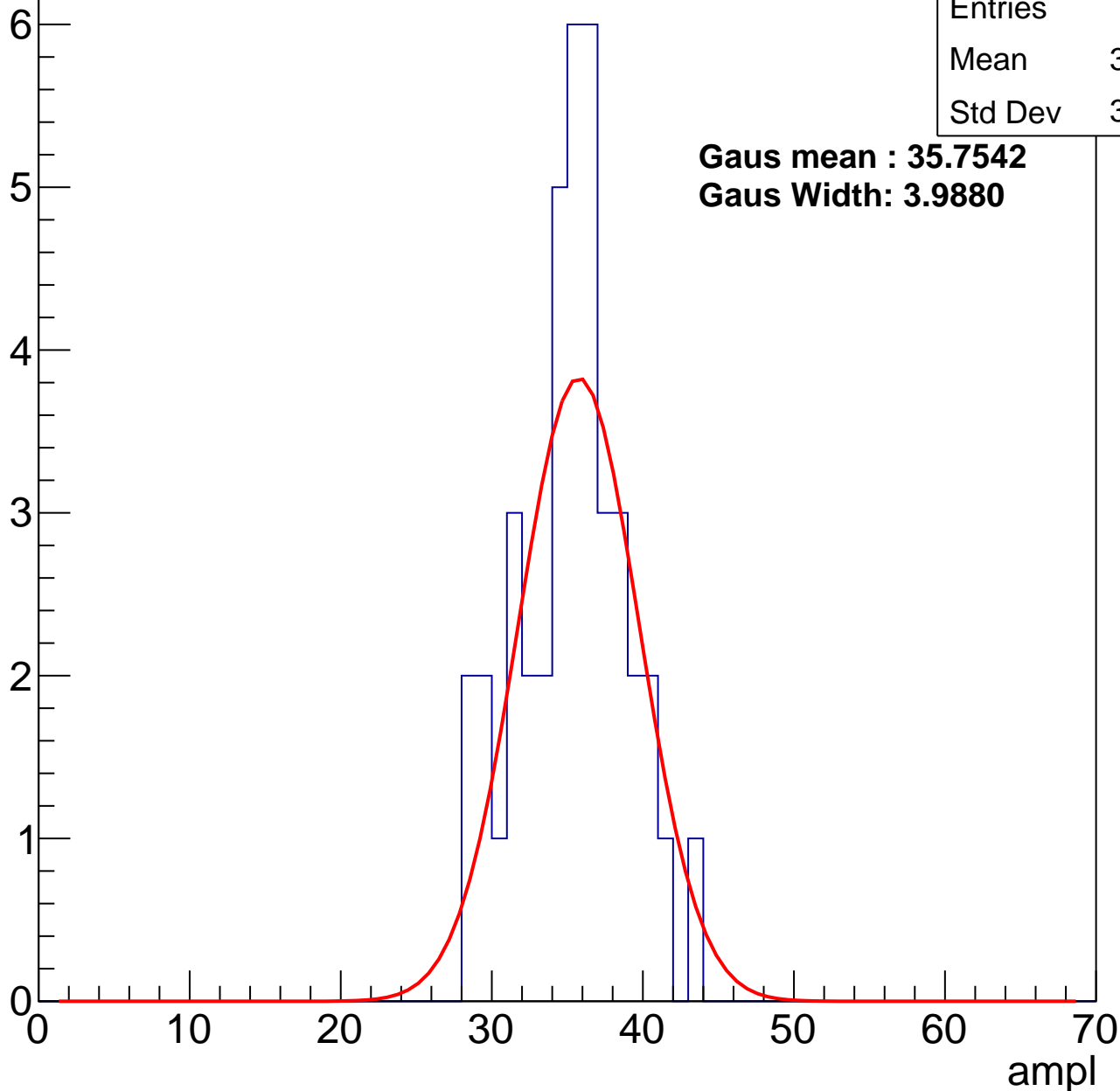
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	41
Mean	34.88
Std Dev	3.494

**Gaus mean : 35.7542**

**Gaus Width: 3.9880**



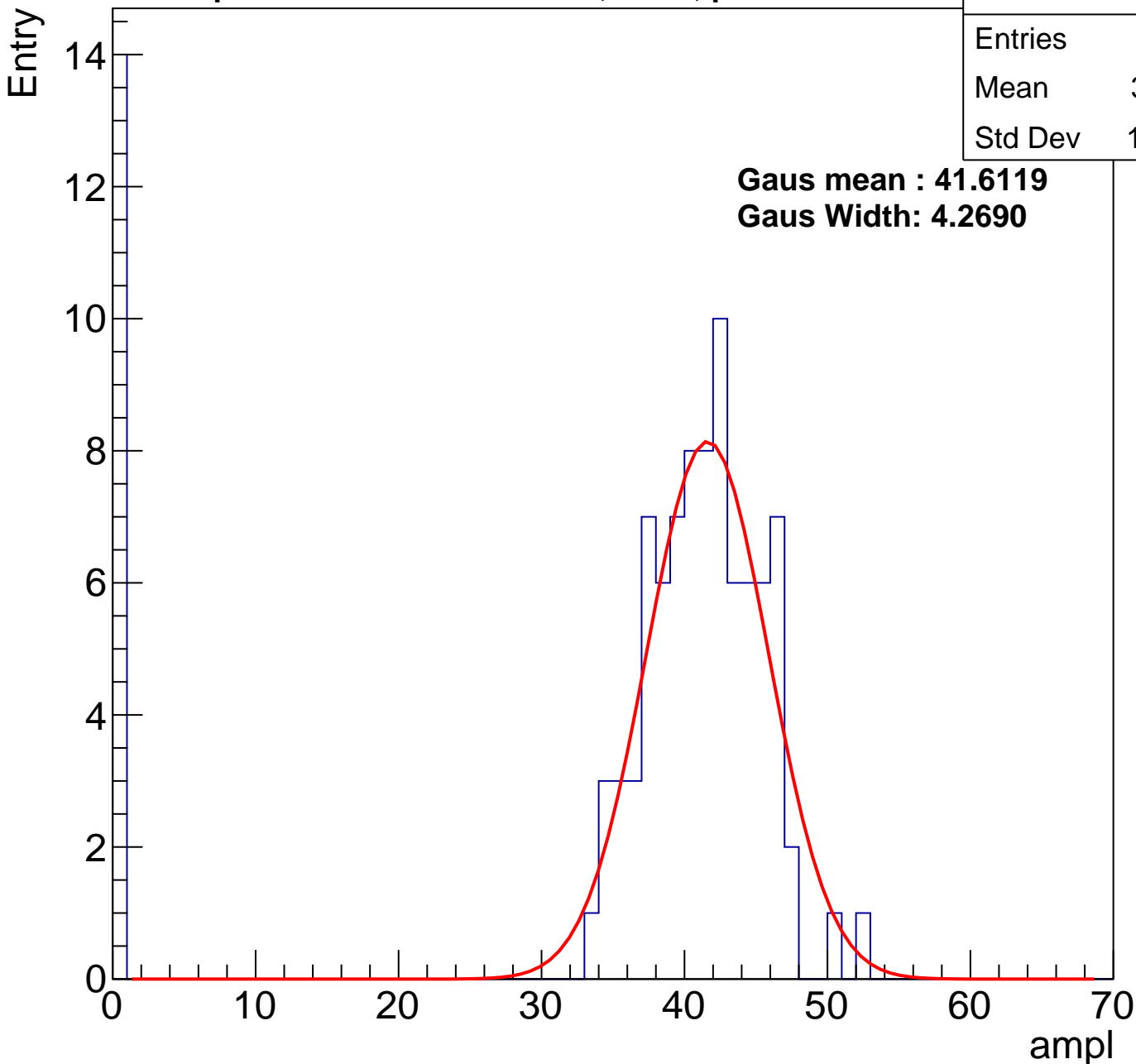
# B1L103S, U3-ch50, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	99
Mean	35.21
Std Dev	14.72

**Gaus mean : 41.6119**

**Gaus Width: 4.2690**

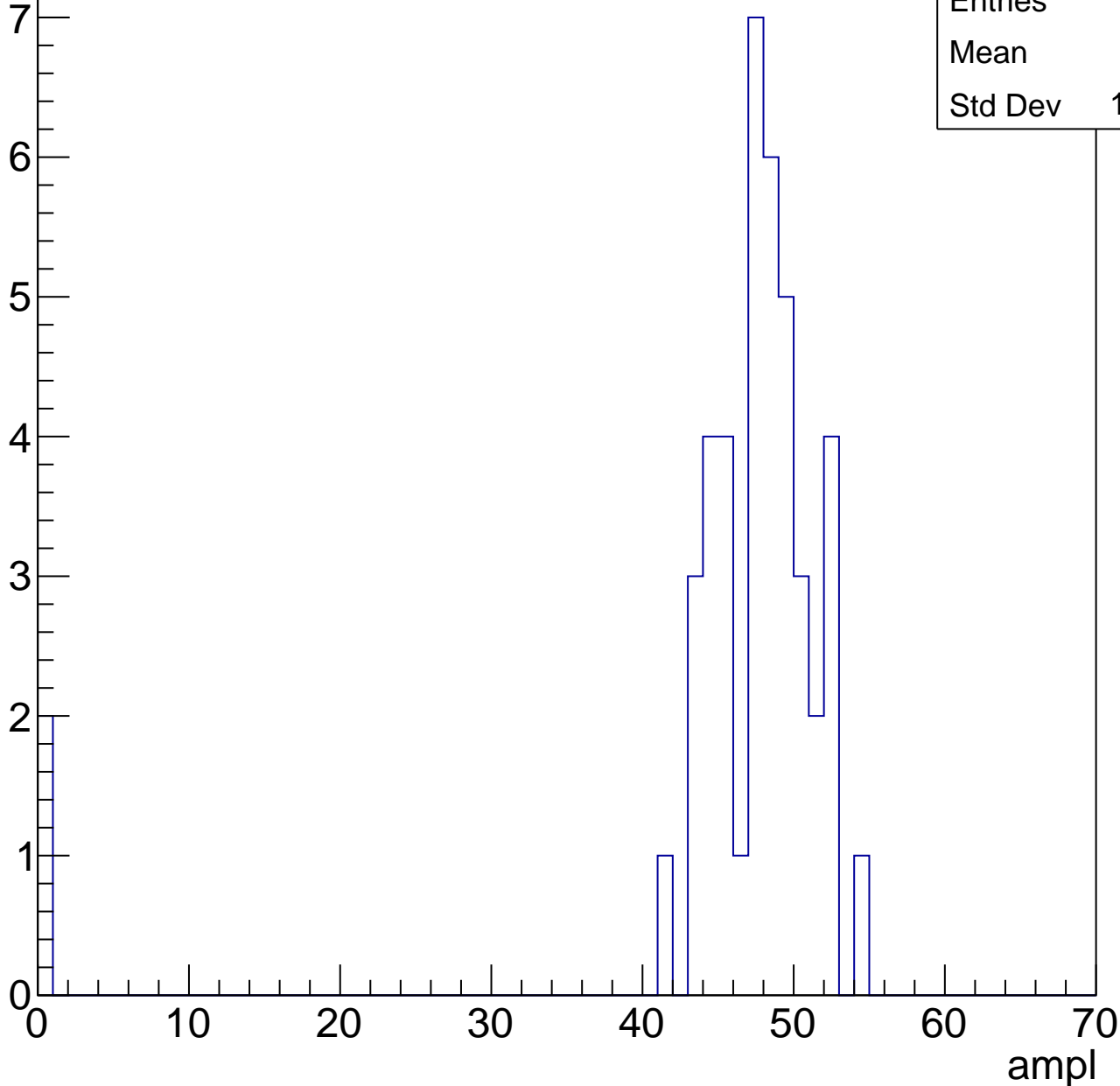


# B1L103S, U3-ch50, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	43
Mean	45.3
Std Dev	10.42

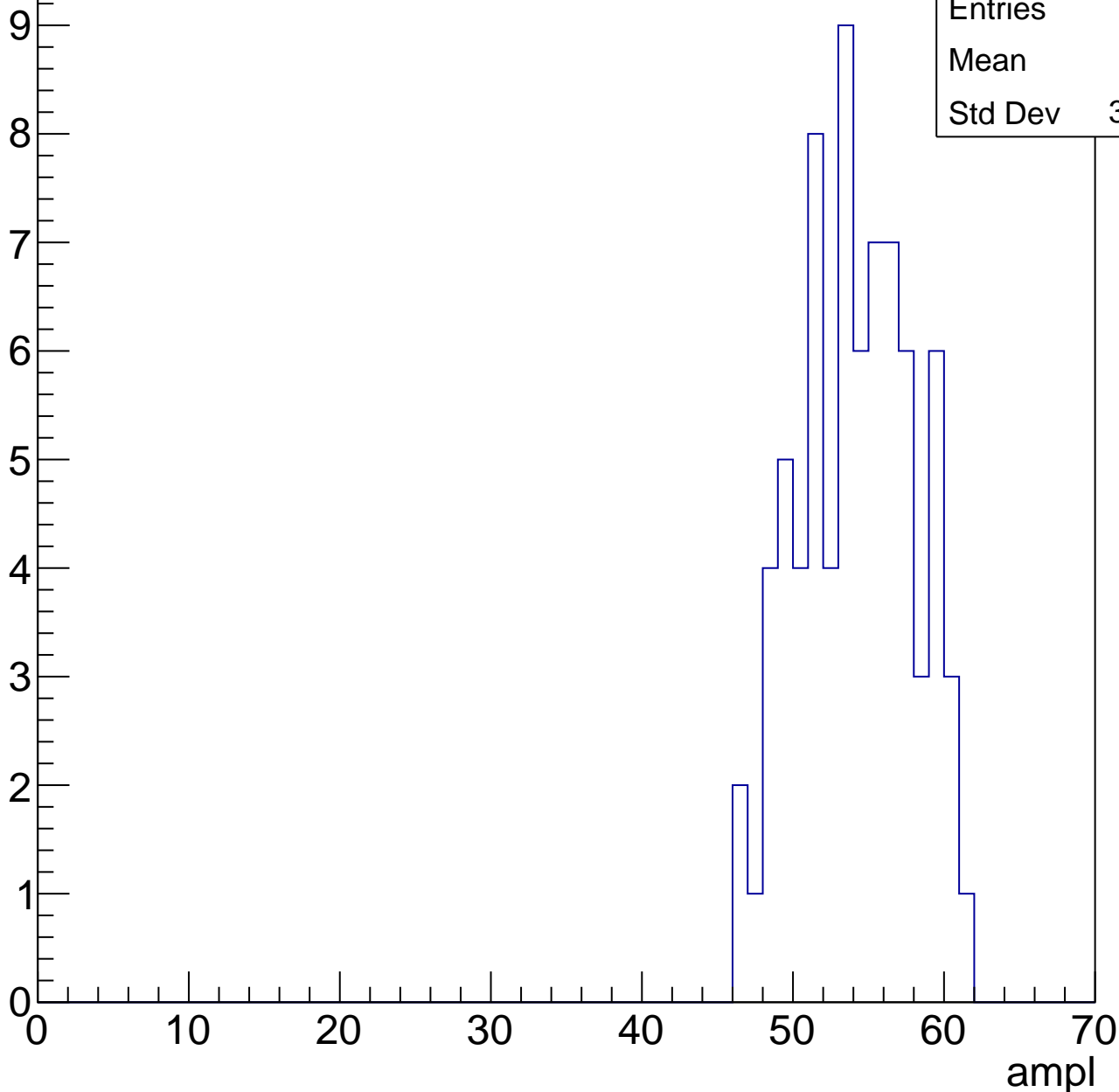


# B1L103S, U3-ch50, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

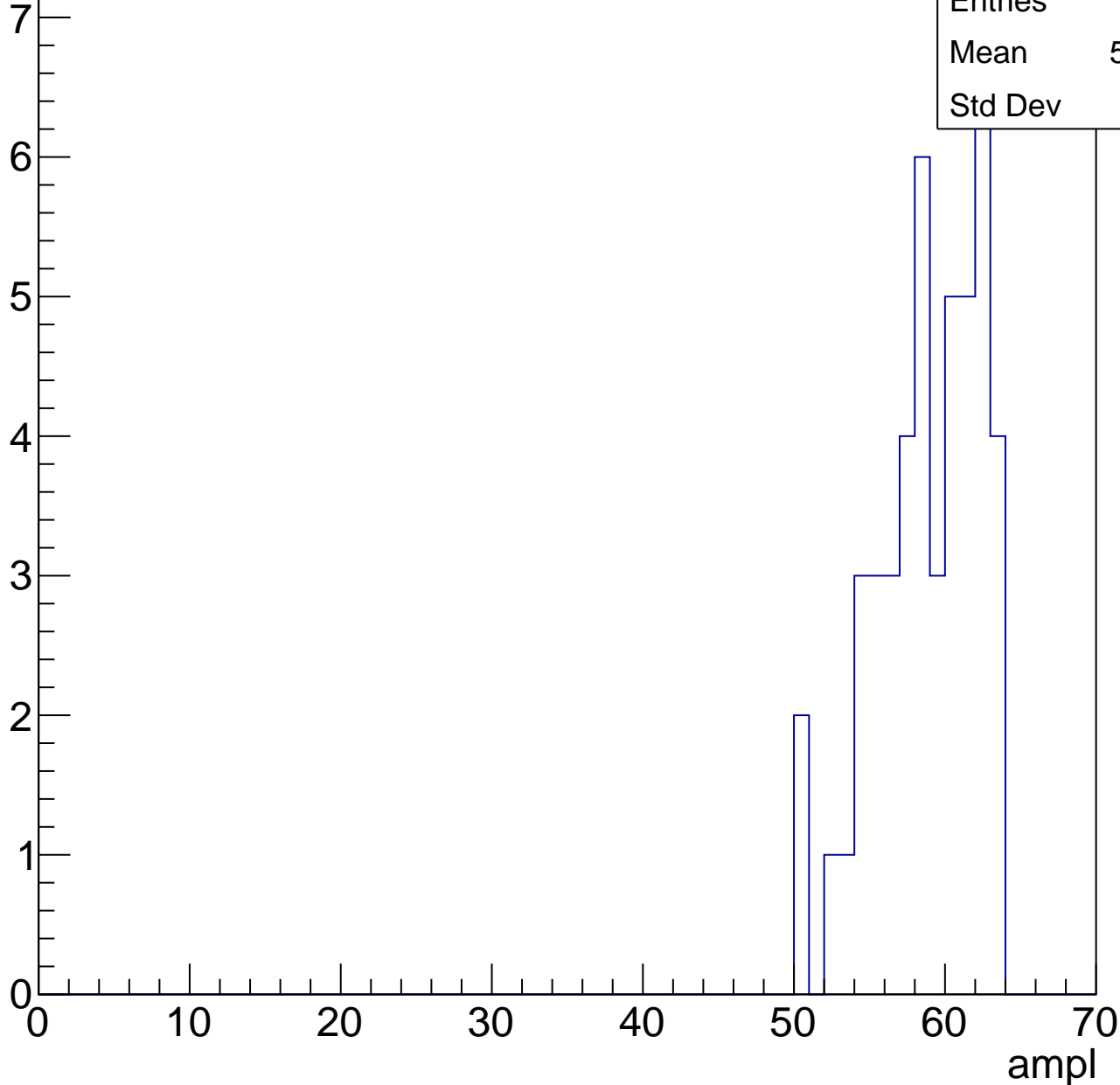
Entries	76
Mean	53.7
Std Dev	3.706



# B1L103S, U3-ch50, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

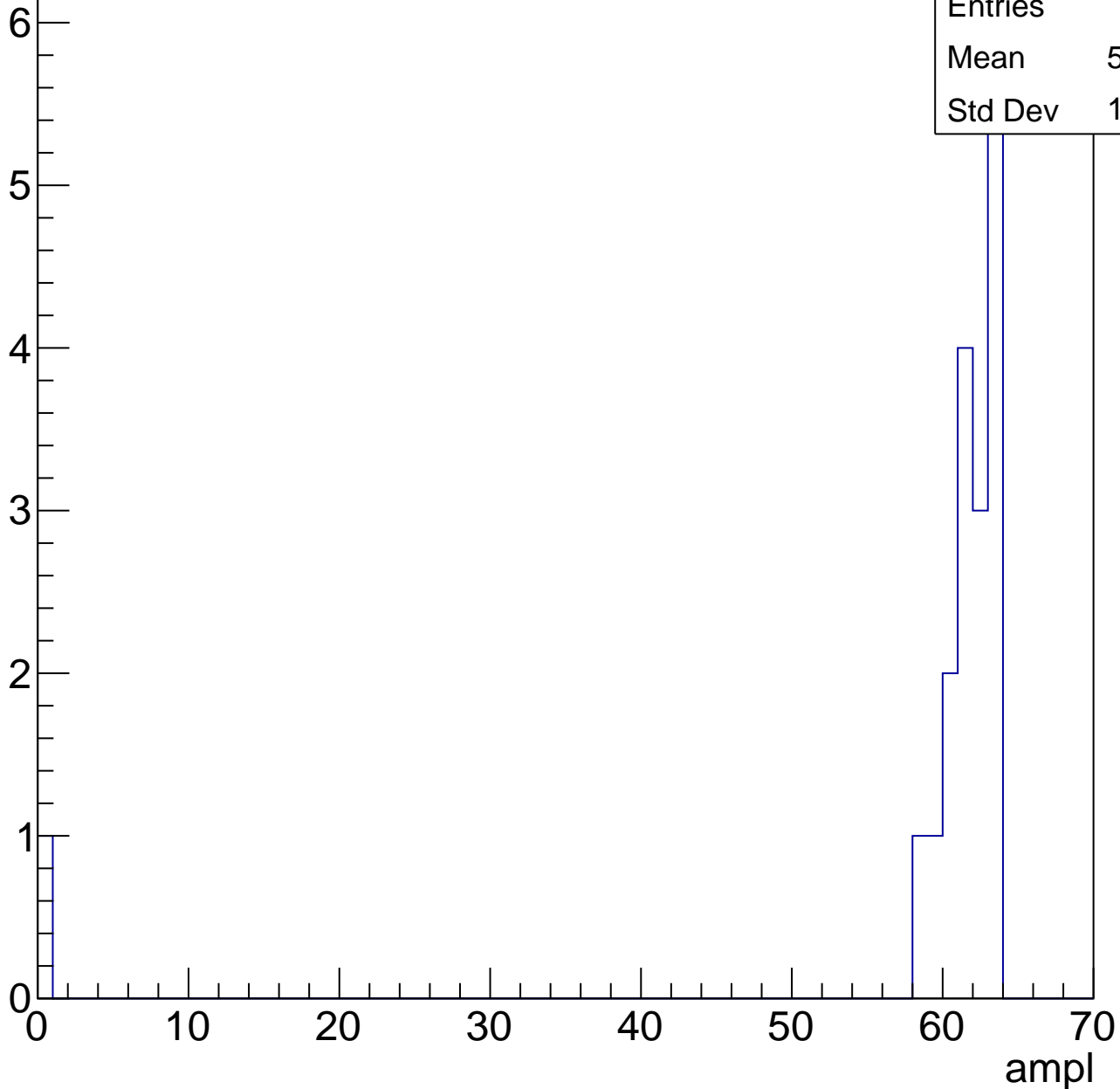


# B1L103S, U3-ch50, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	18
Mean	58.06
Std Dev	14.16





# B1L103S, U3-ch50, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	1.053
Std Dev	4.466

Entry



# B1L103S, U3-ch51, adc0

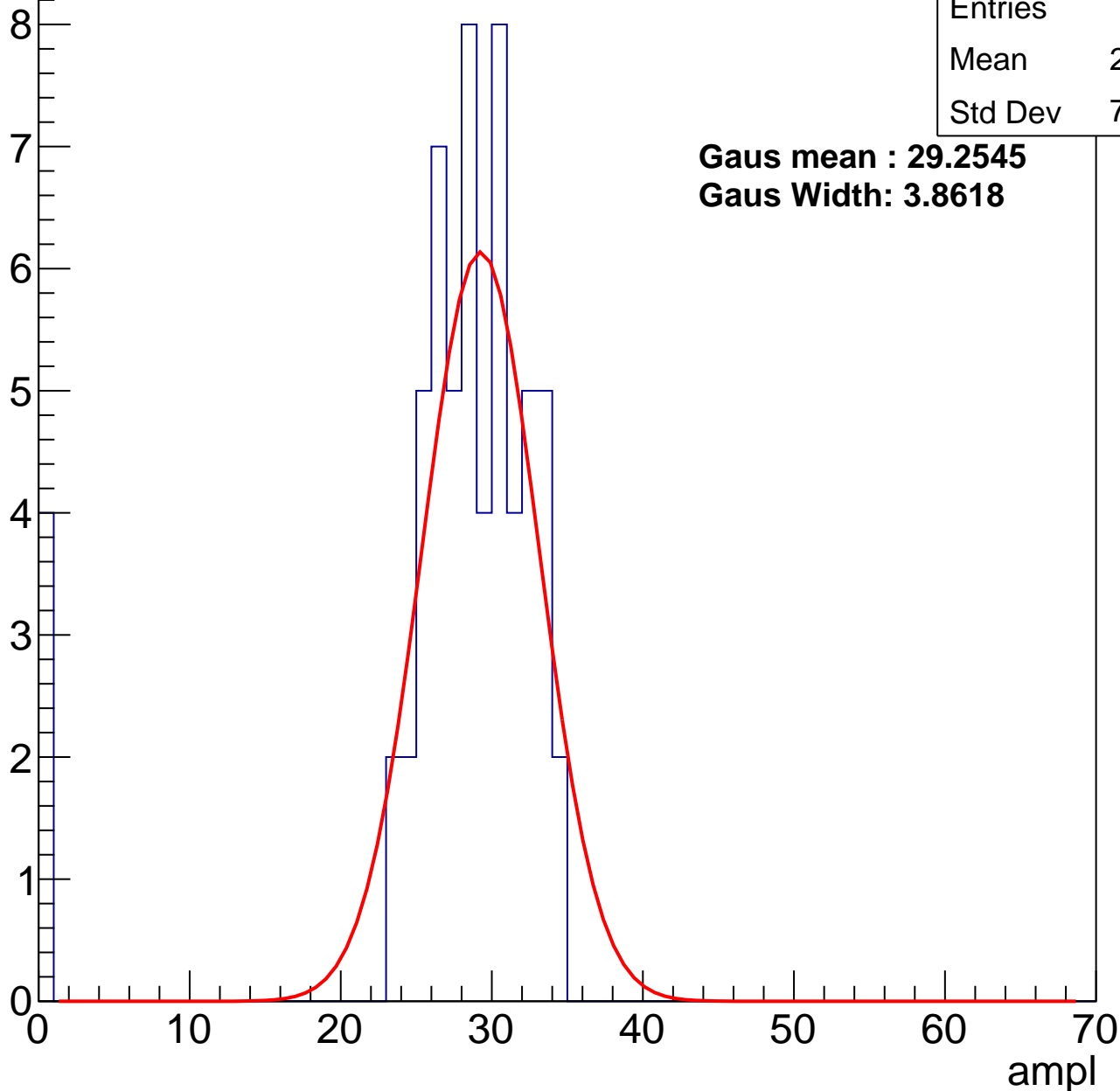
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	26.77
Std Dev	7.632

**Gaus mean : 29.2545**

**Gaus Width: 3.8618**



# B1L103S, U3-ch51, adc1

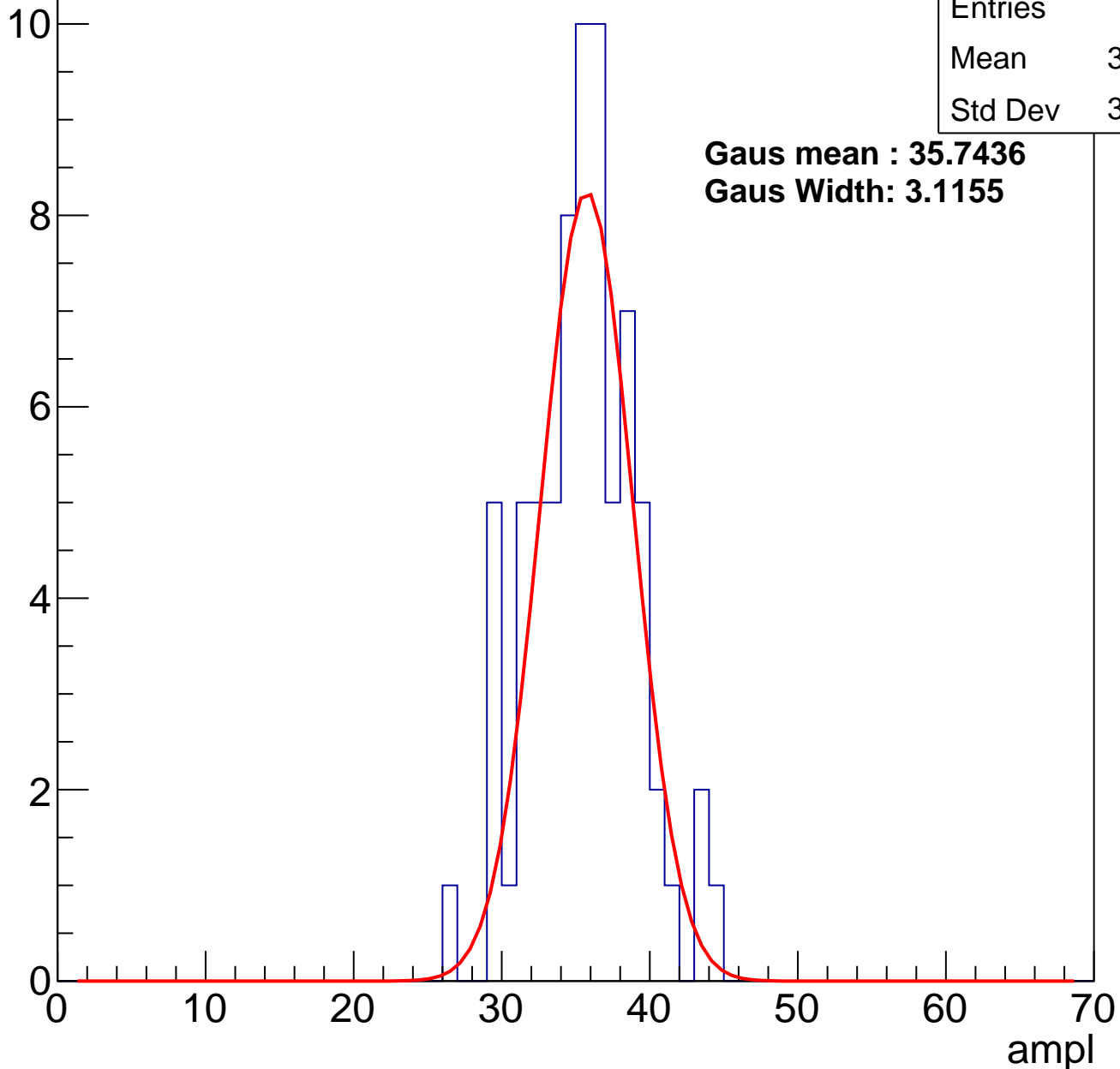
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	73
Mean	35.07
Std Dev	3.524

**Gaus mean : 35.7436**

**Gaus Width: 3.1155**

Entry



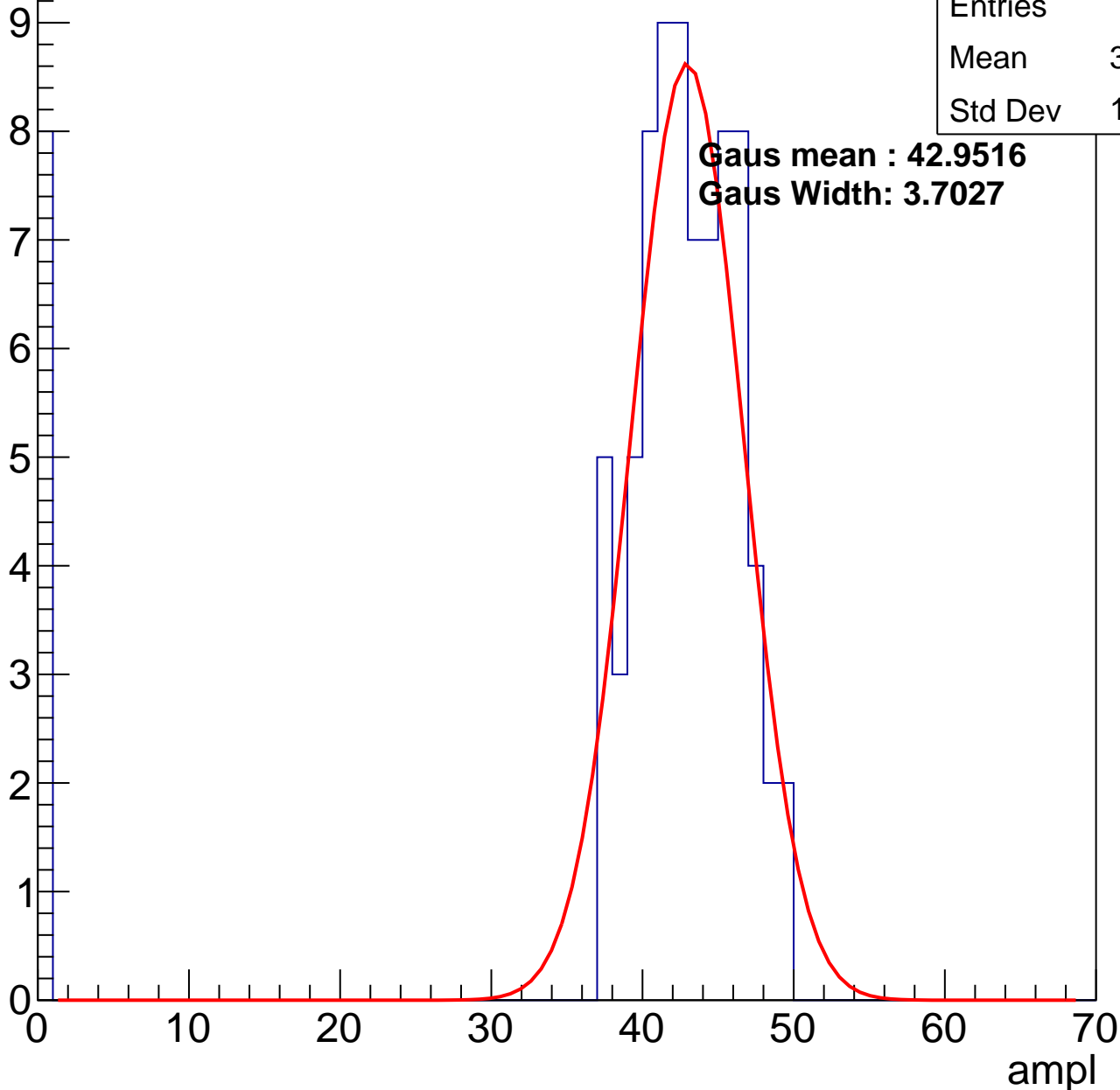
# B1L103S, U3-ch51, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	85
Mean	38.59
Std Dev	12.78

**Gaus mean : 42.9516**  
**Gaus Width: 3.7027**

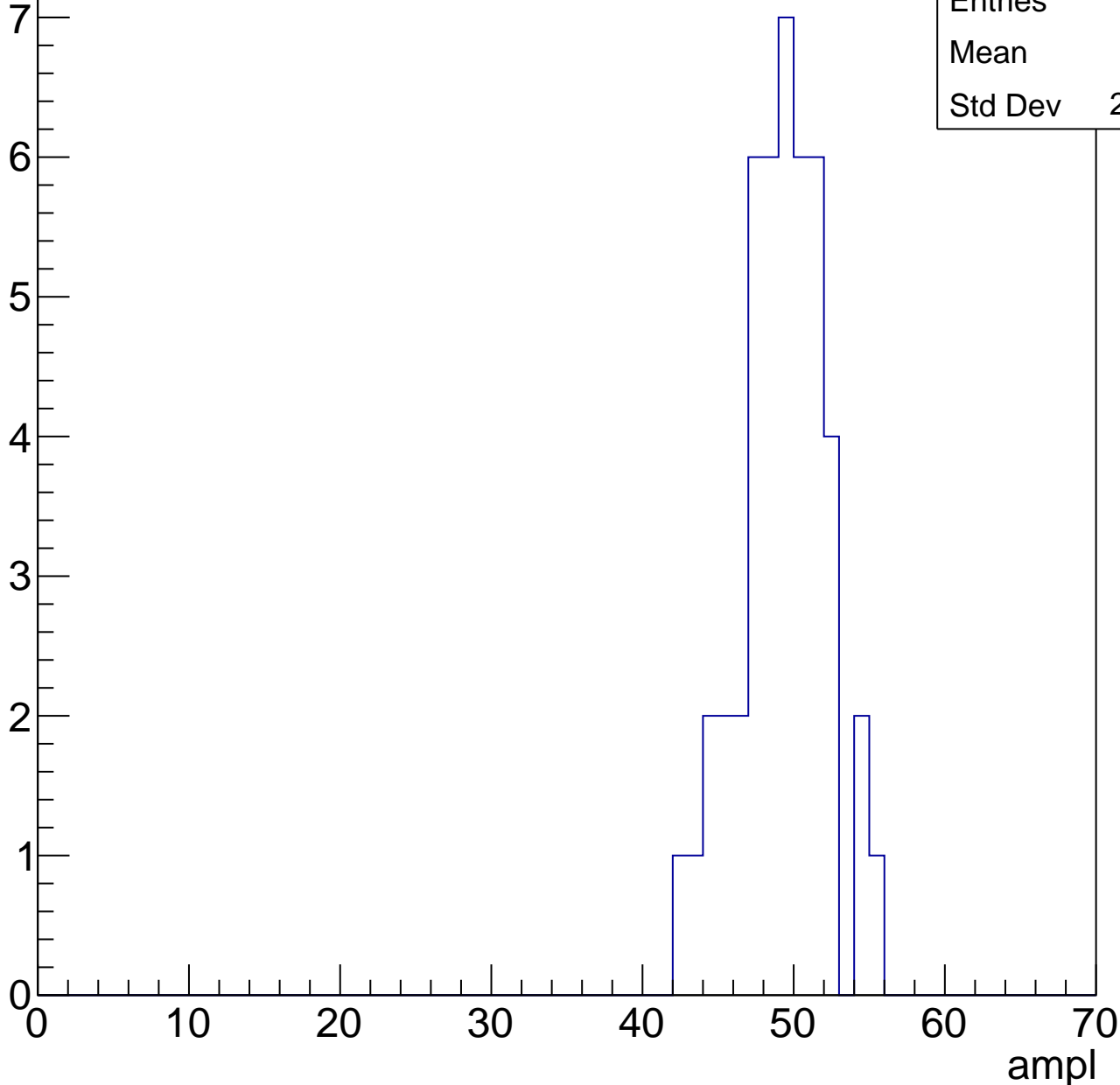


# B1L103S, U3-ch51, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

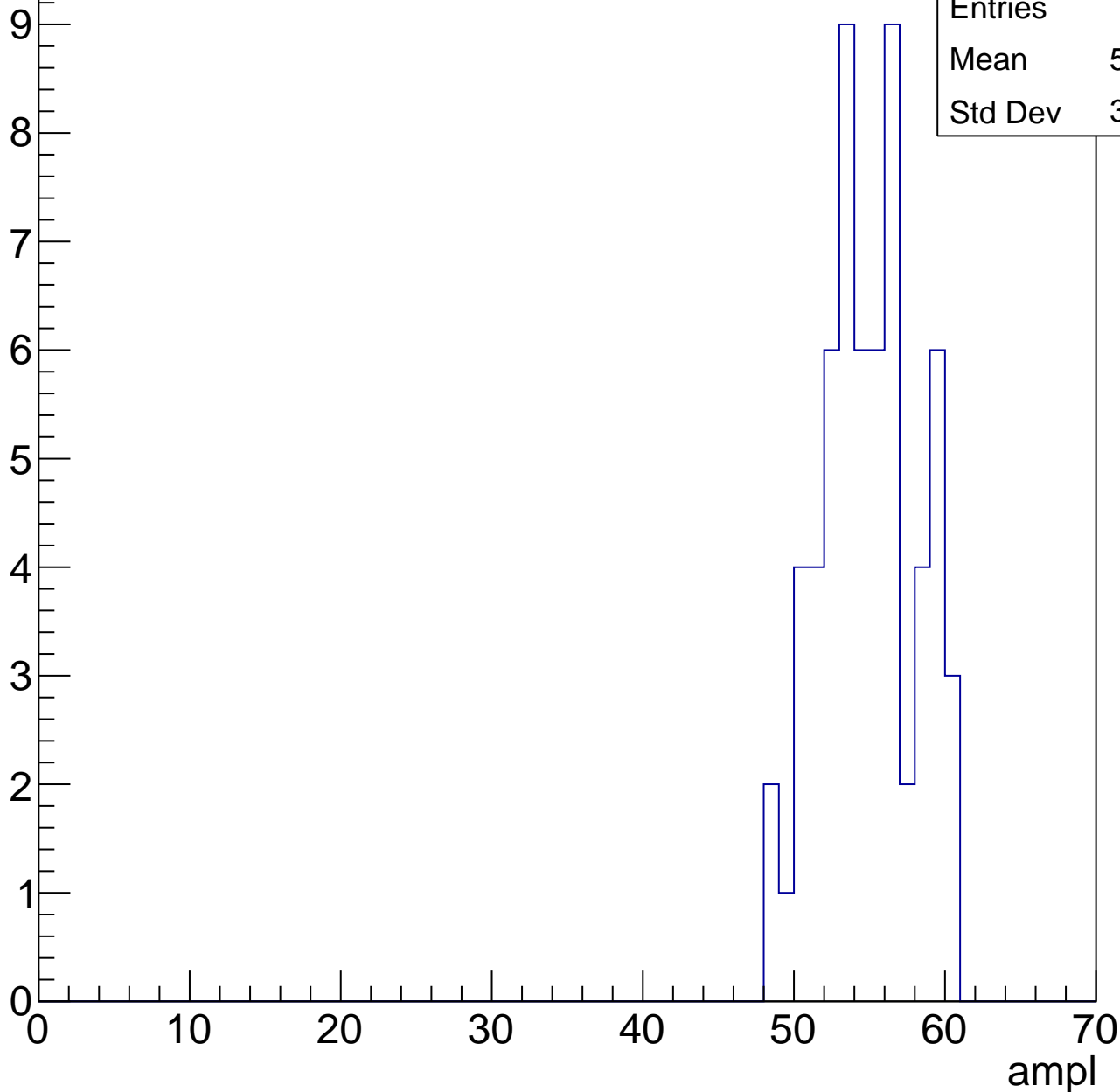
Entries	46
Mean	48.8
Std Dev	2.818



# B1L103S, U3-ch51, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

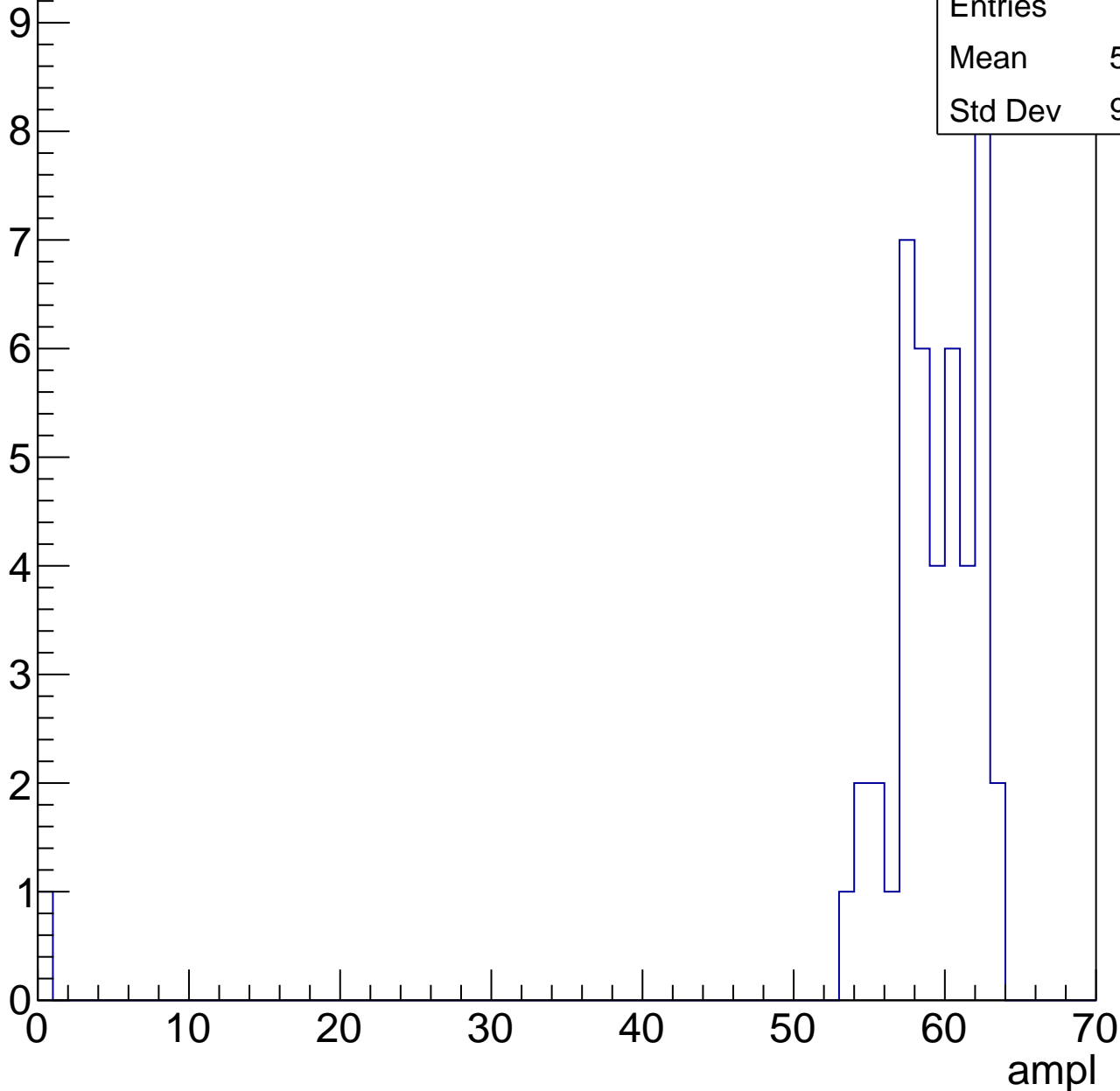


# B1L103S, U3-ch51, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	45
Mean	57.73
Std Dev	9.074

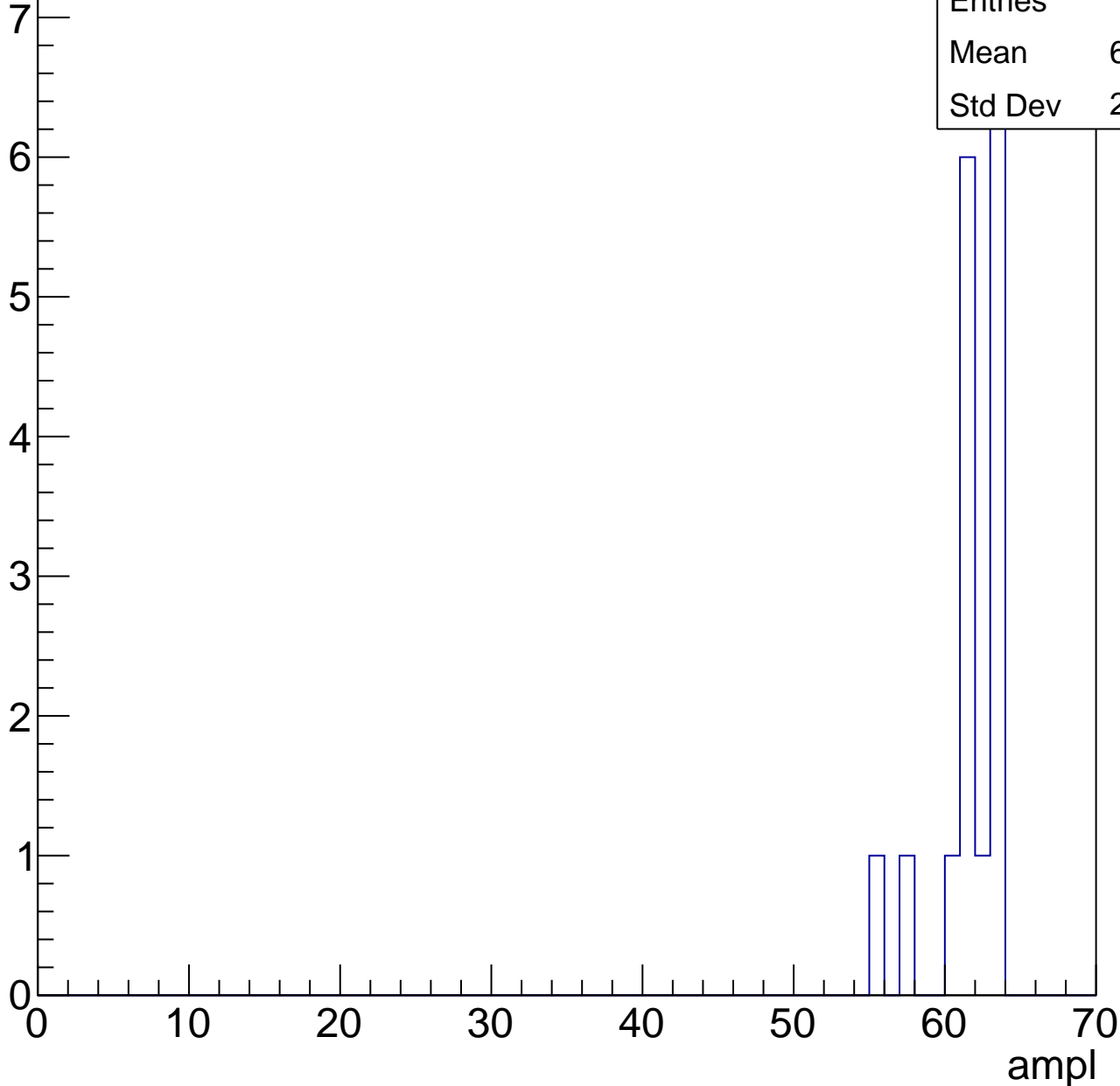


# B1L103S, U3-ch51, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	17
Mean	61.24
Std Dev	2.184

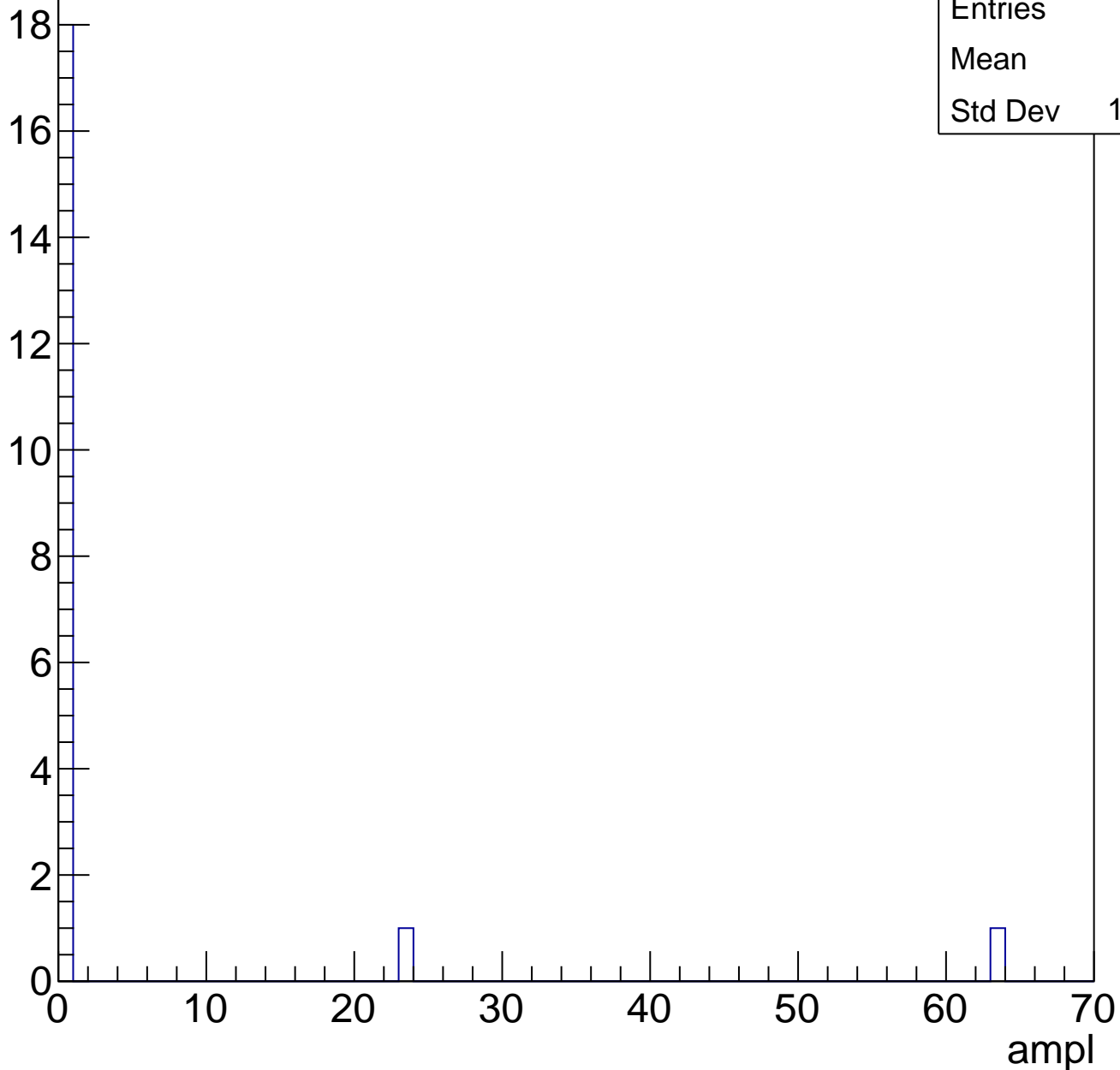




# B1L103S, U3-ch51, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U3-ch52, adc0

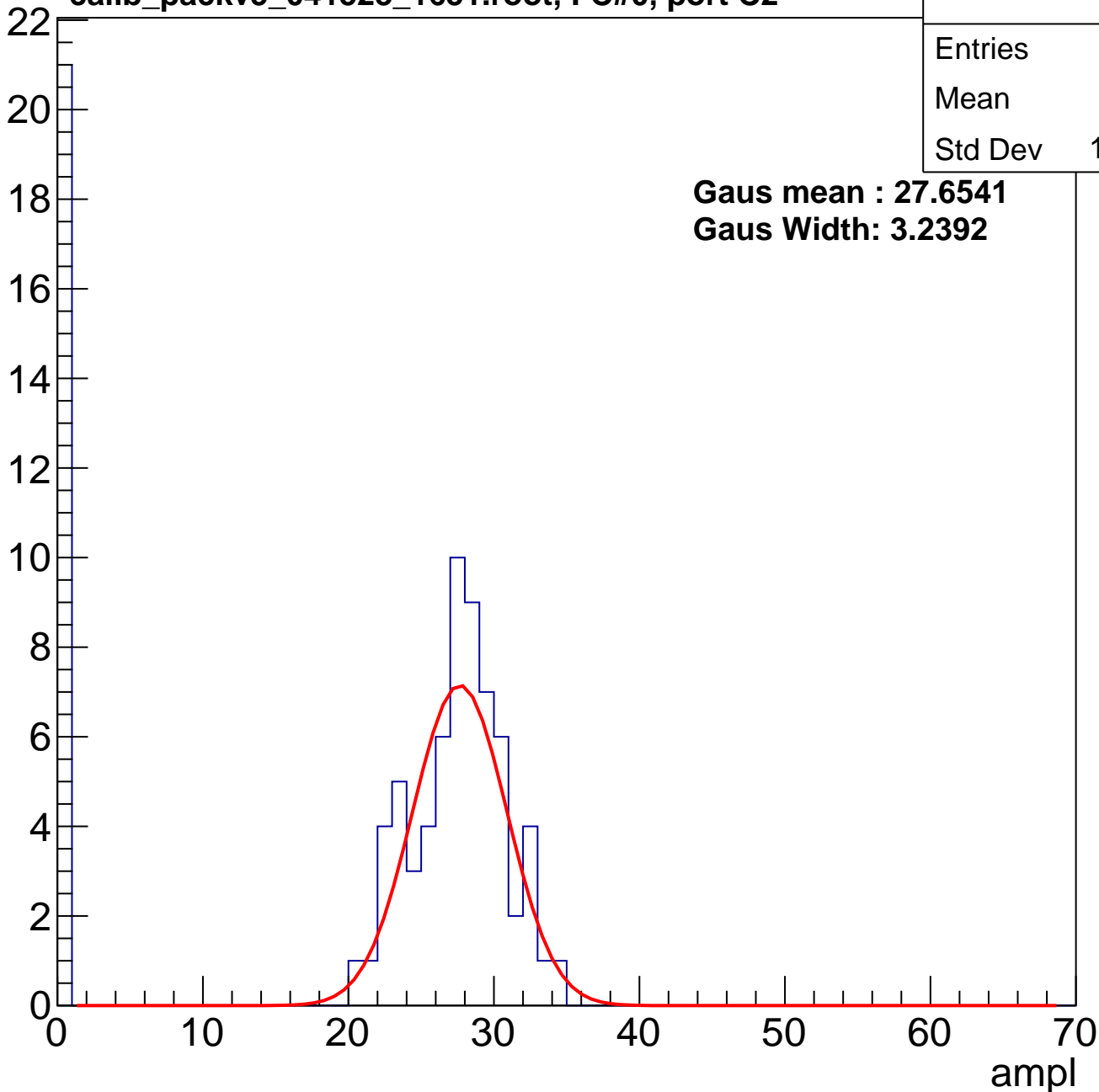
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	85
Mean	20.4
Std Dev	11.99

**Gaus mean : 27.6541**

**Gaus Width: 3.2392**

Entry



# B1L103S, U3-ch52, adc1

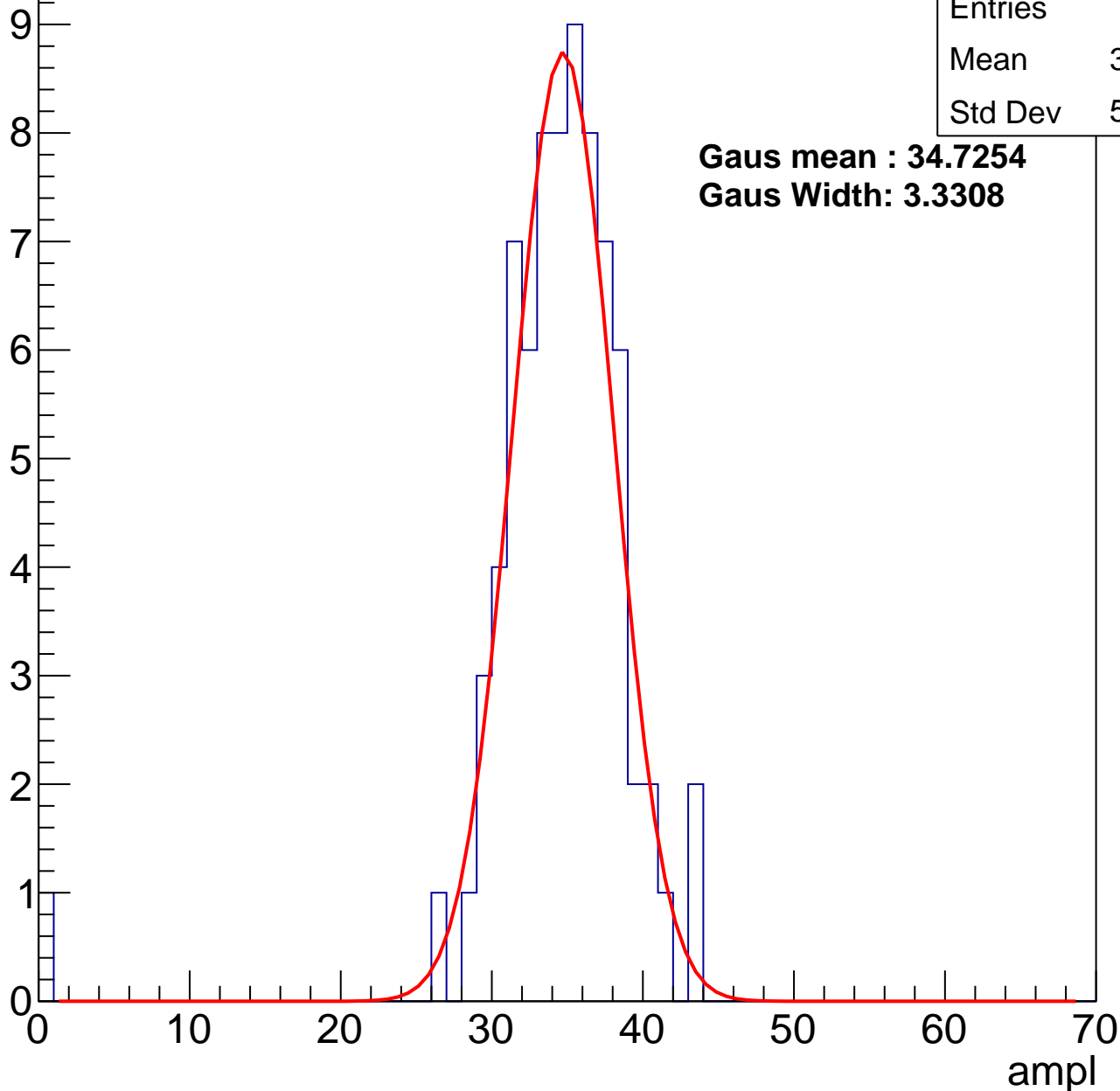
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	76
Mean	33.96
Std Dev	5.159

**Gaus mean : 34.7254**

**Gaus Width: 3.3308**



# B1L103S, U3-ch52, adc2

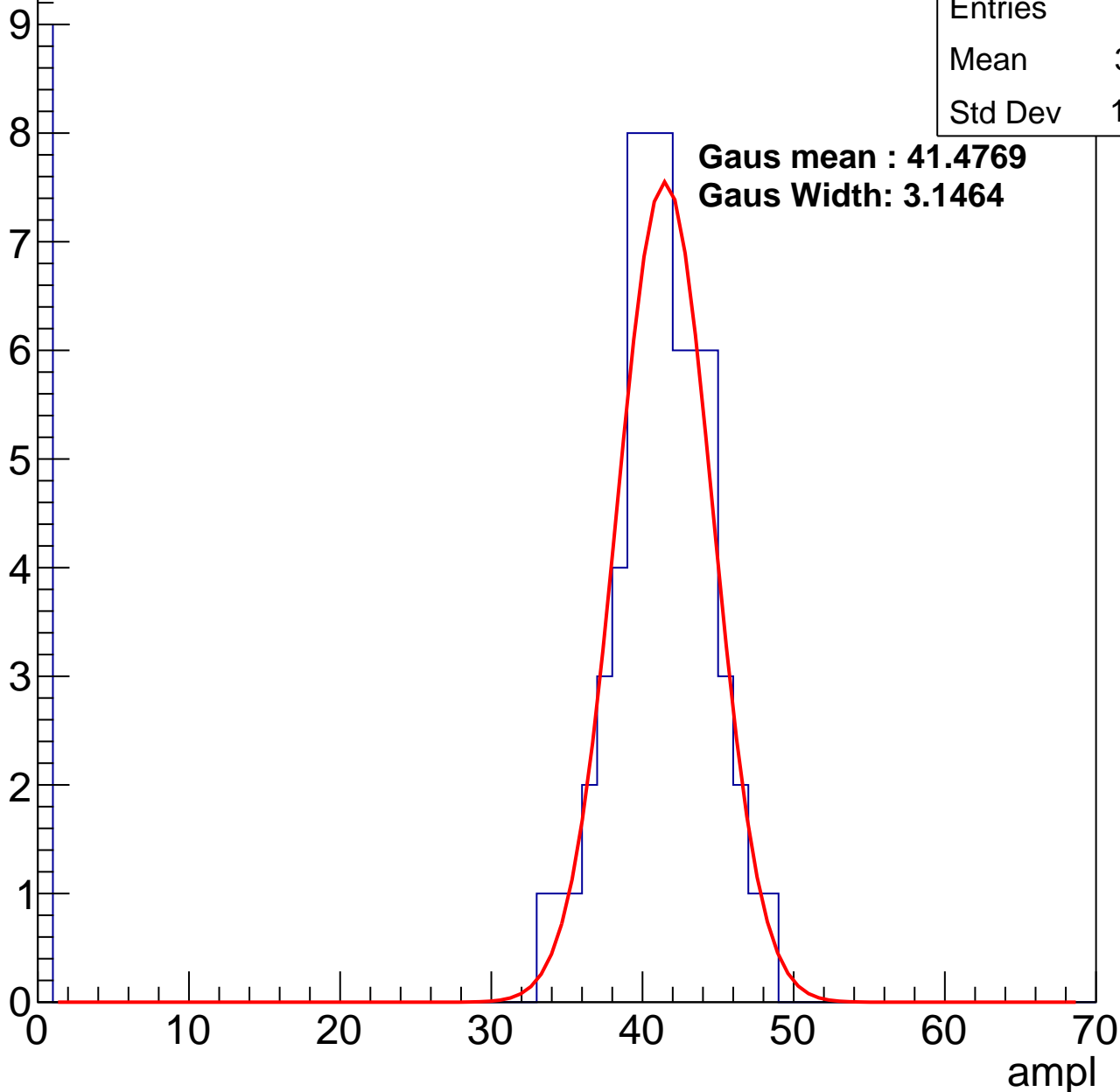
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	35.61
Std Dev	13.98

**Gaus mean : 41.4769**

**Gaus Width: 3.1464**

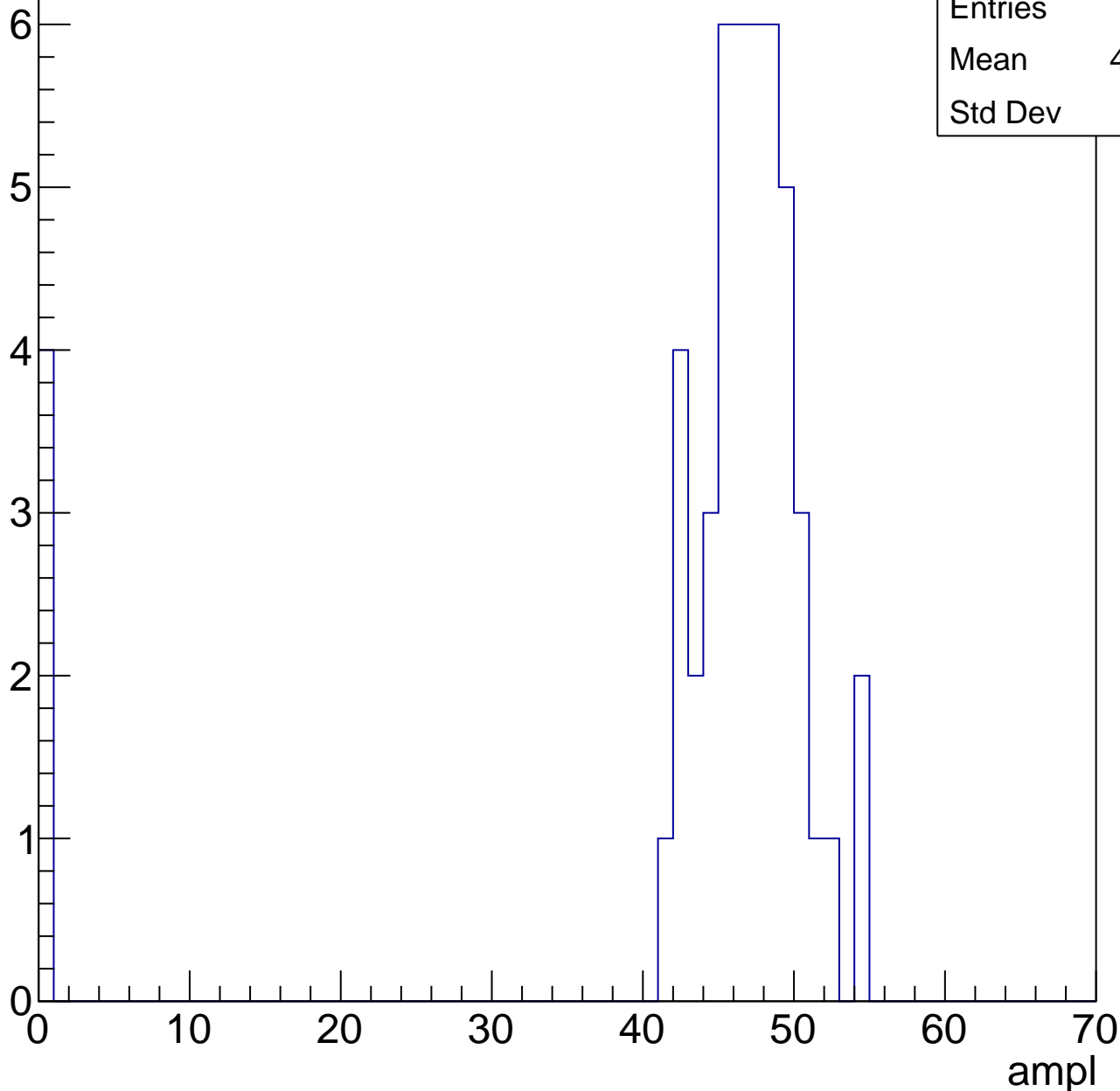


# B1L103S, U3-ch52, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	50
Mean	42.98
Std Dev	13

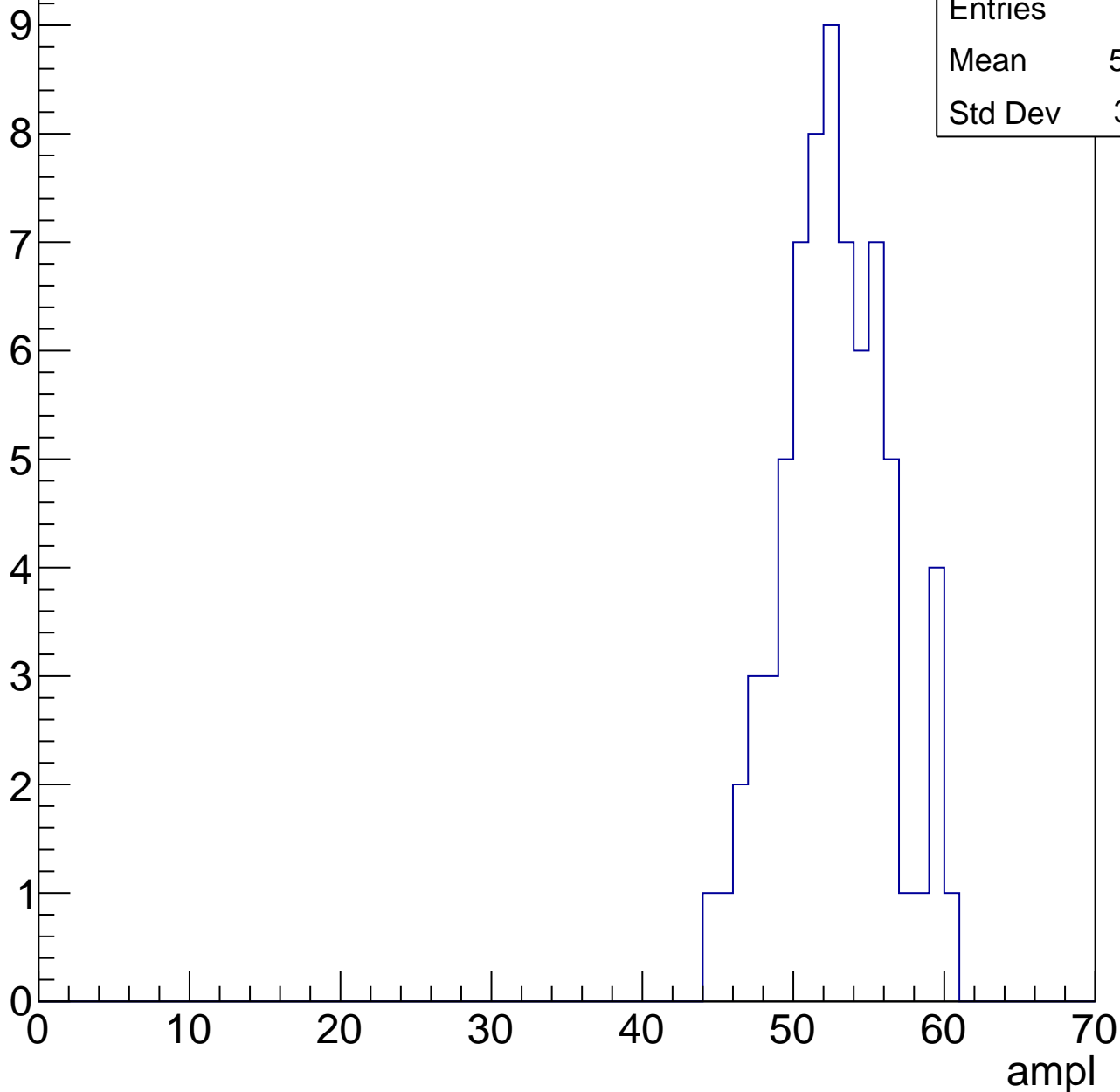


# B1L103S, U3-ch52, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	71
Mean	52.23
Std Dev	3.521

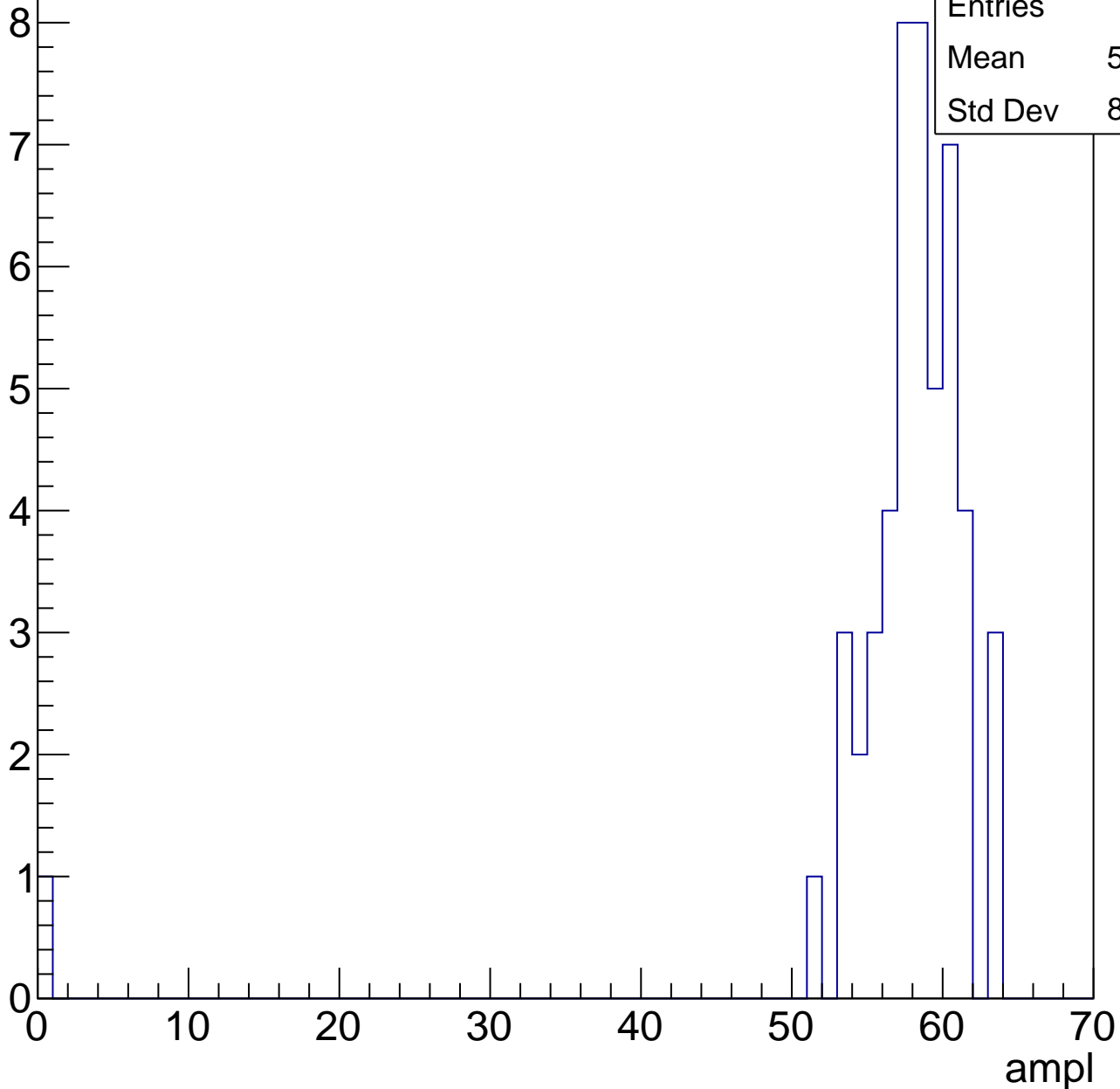


# B1L103S, U3-ch52, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	49
Mean	56.63
Std Dev	8.599

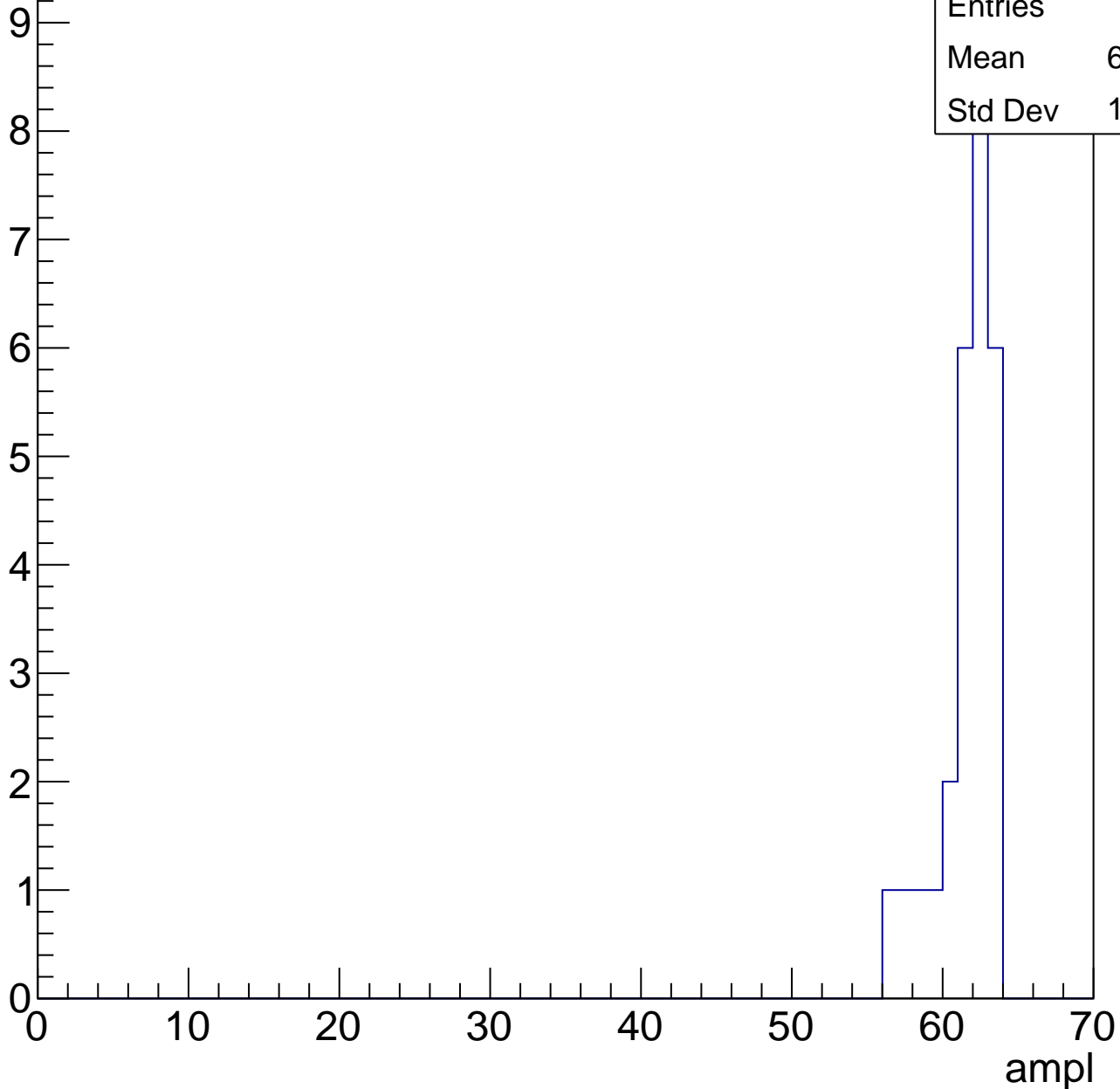


# B1L103S, U3-ch52, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	27
Mean	61.19
Std Dev	1.806



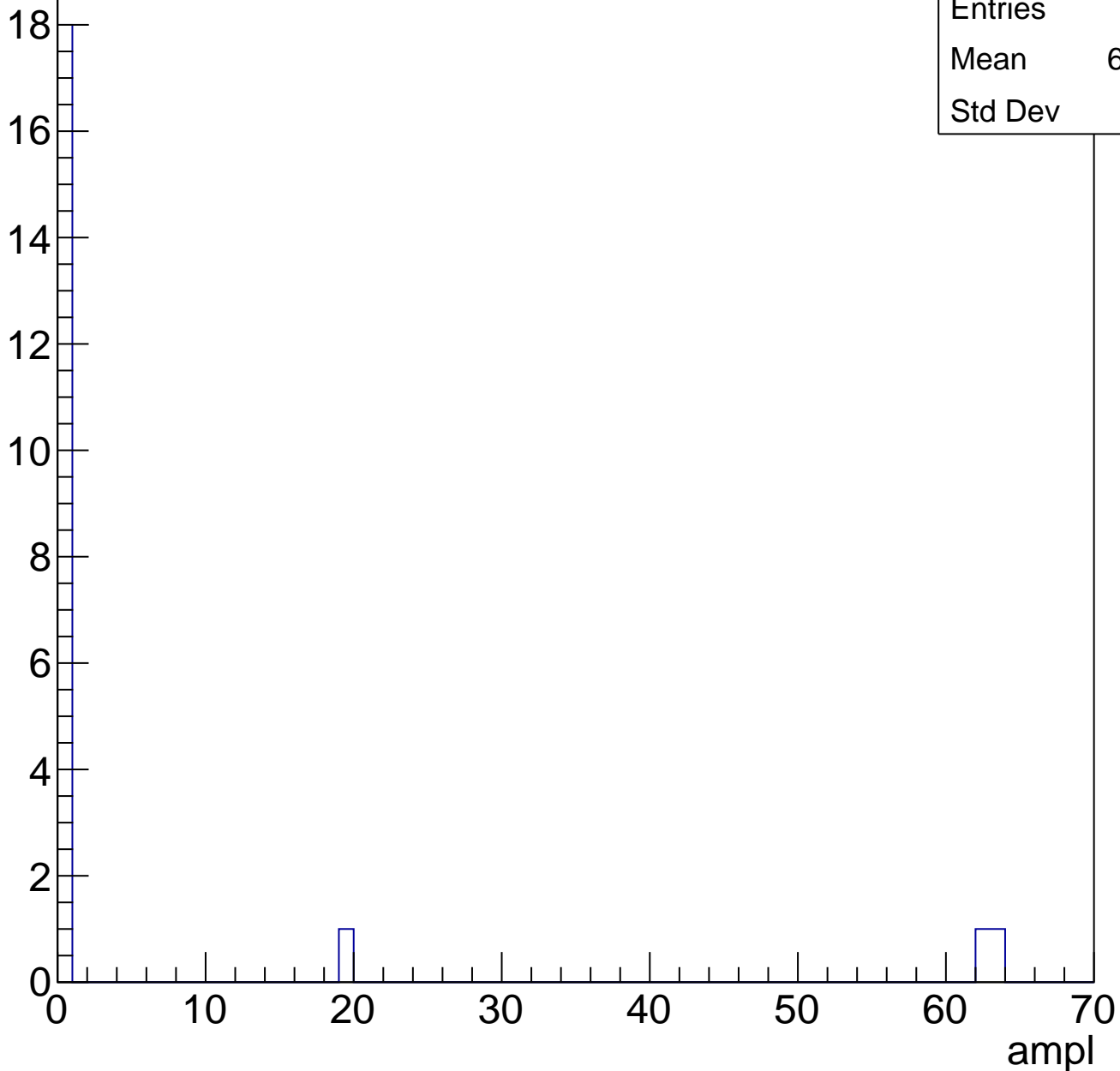


# B1L103S, U3-ch52, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	6.857
Std Dev	18.5

Entry



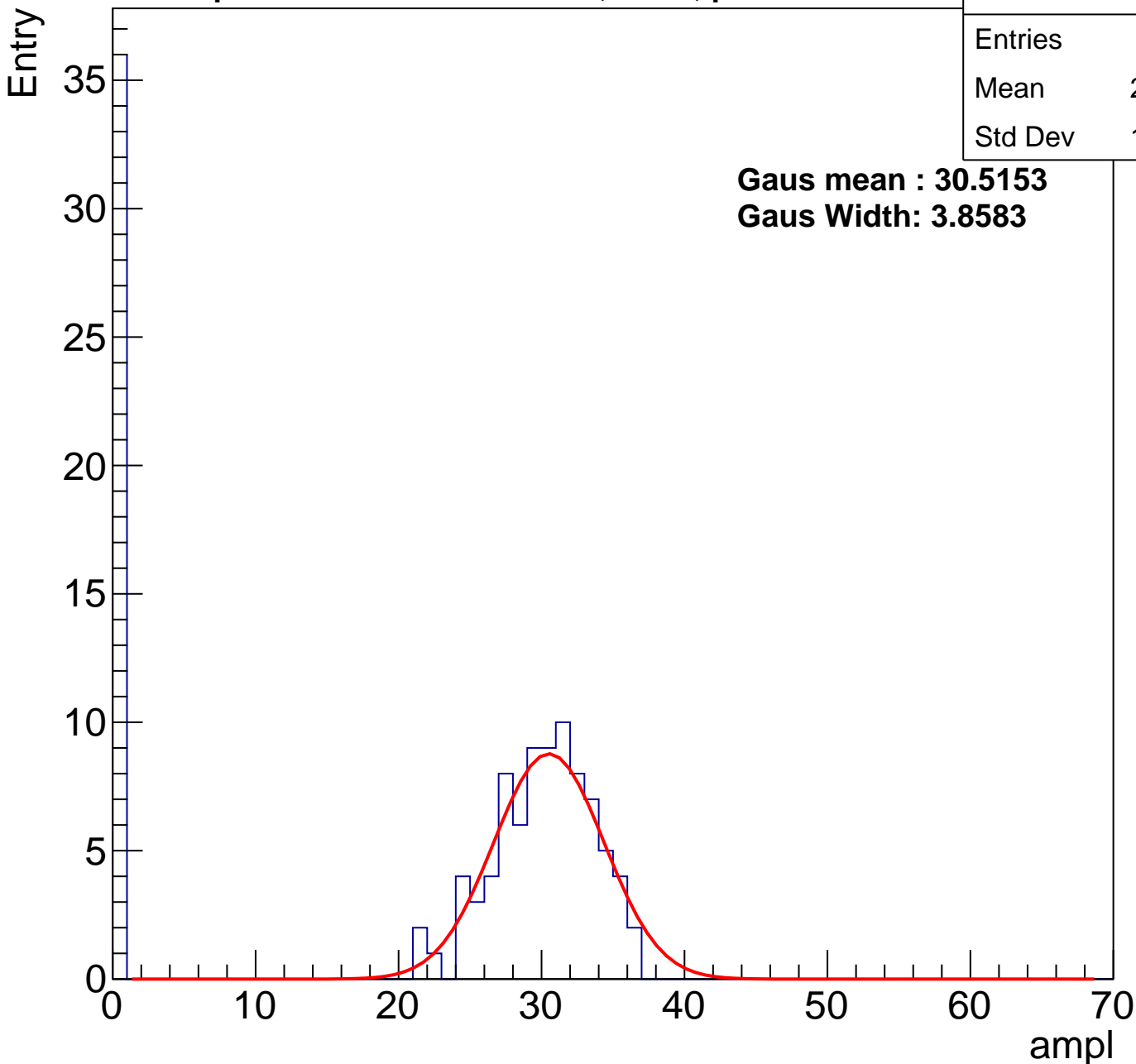
# B1L103S, U3-ch53, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	118
Mean	20.62
Std Dev	13.96

**Gaus mean : 30.5153**

**Gaus Width: 3.8583**



# B1L103S, U3-ch53, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	67
Mean	28.84
Std Dev	15.76

**Gaus mean : 36.8464**

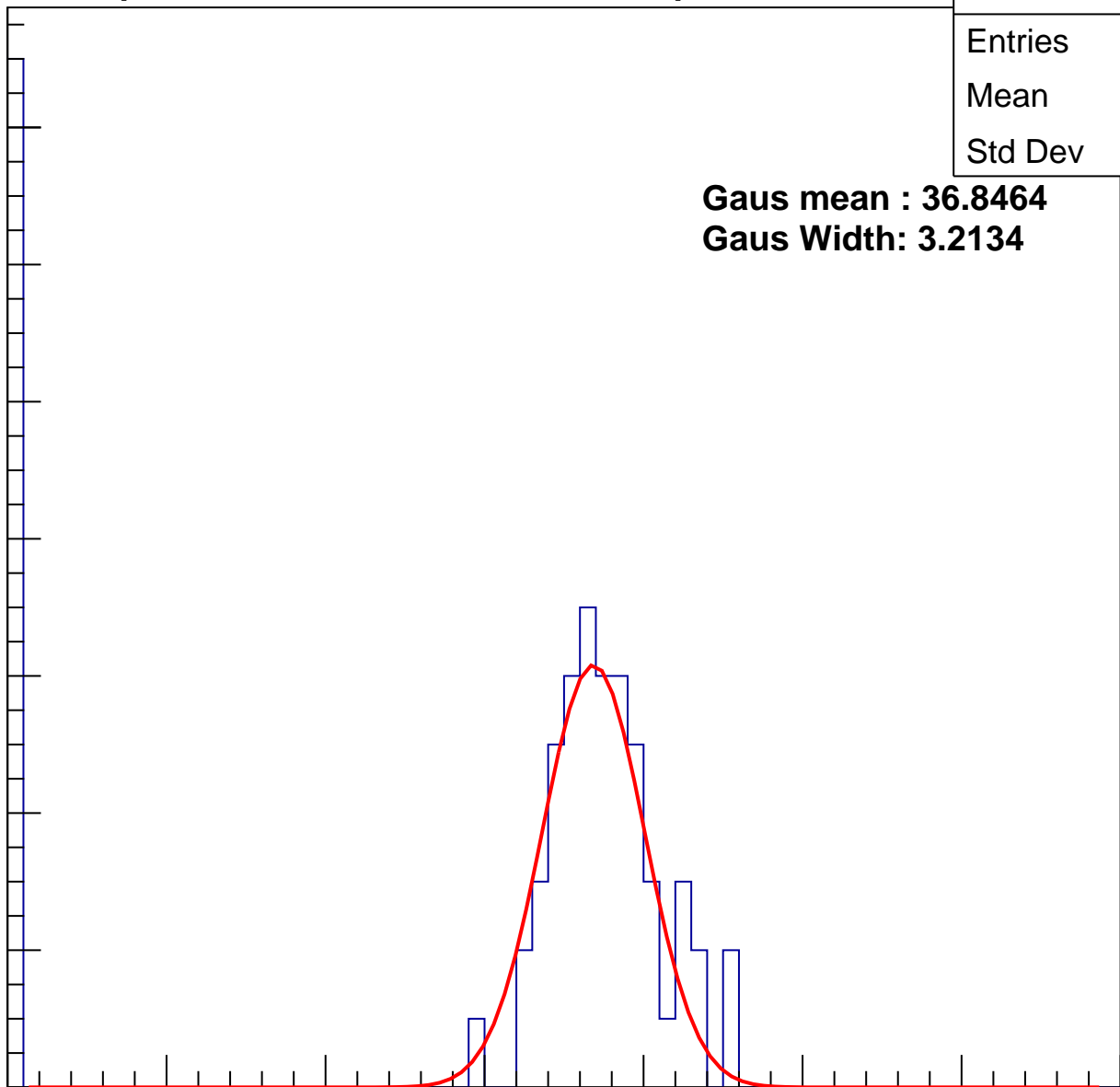
**Gaus Width: 3.2134**

Entry

14  
12  
10  
8  
6  
4  
2  
0

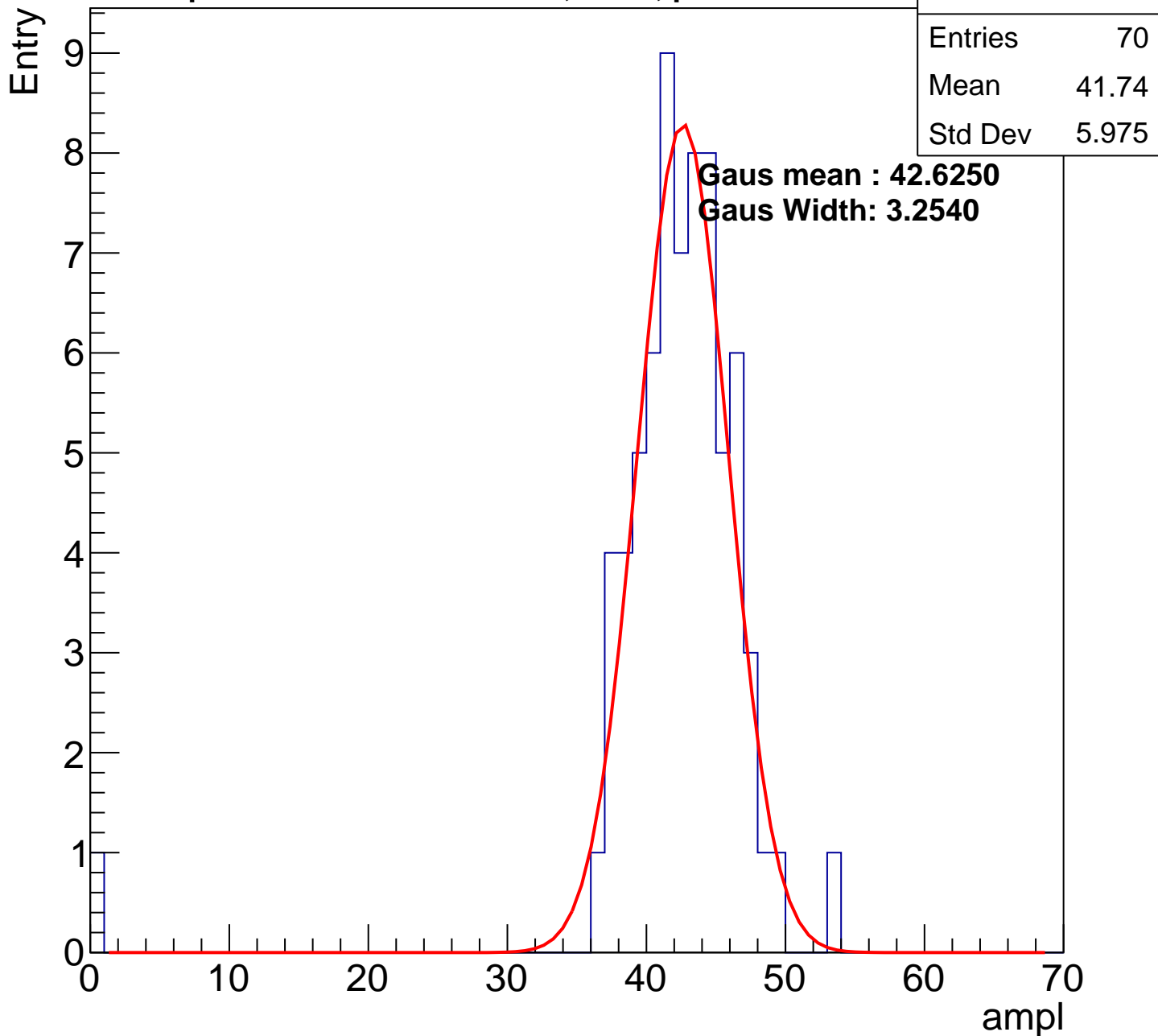
0 10 20 30 40 50 60 70

ampl



# B1L103S, U3-ch53, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

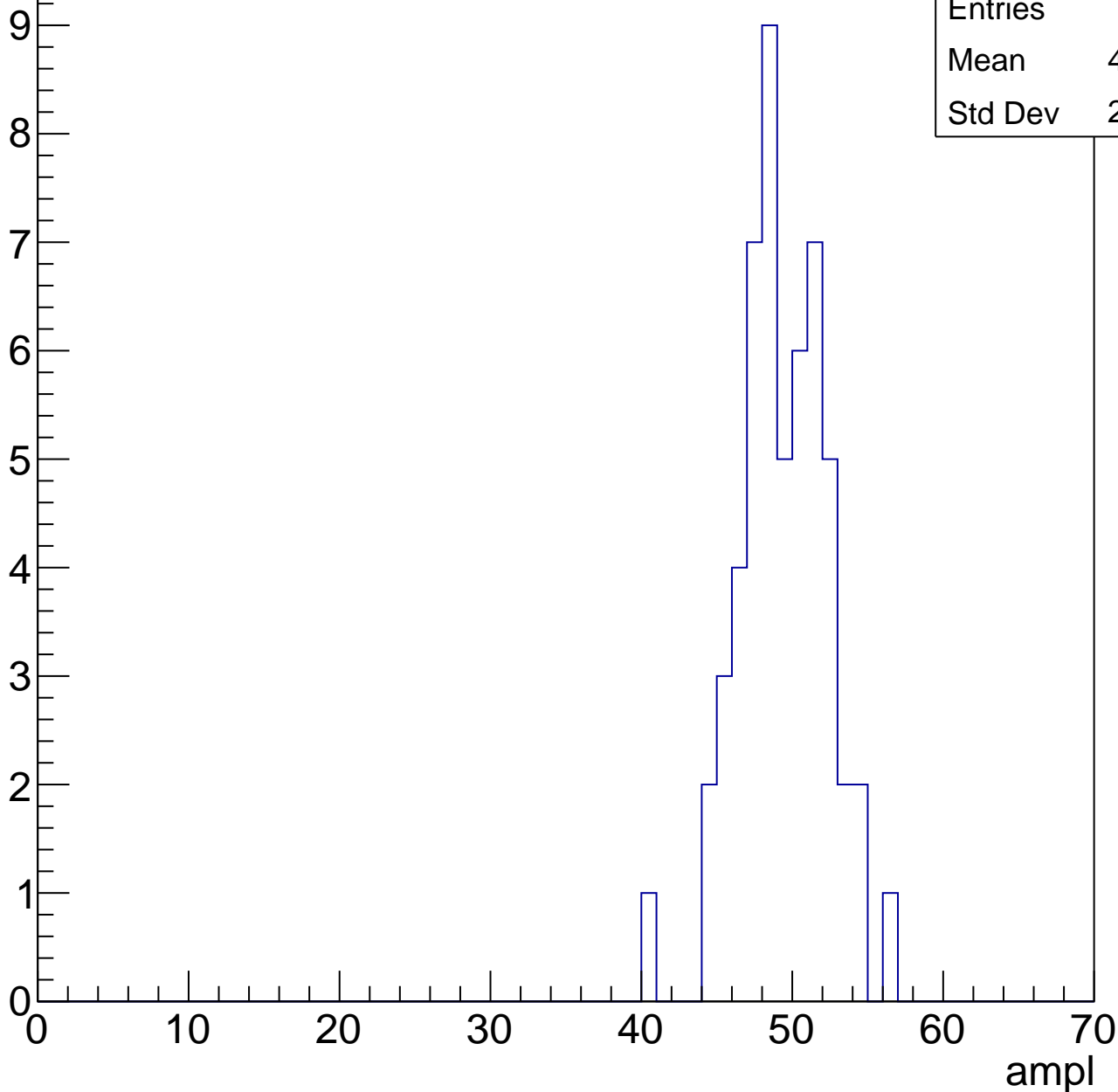


# B1L103S, U3-ch53, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

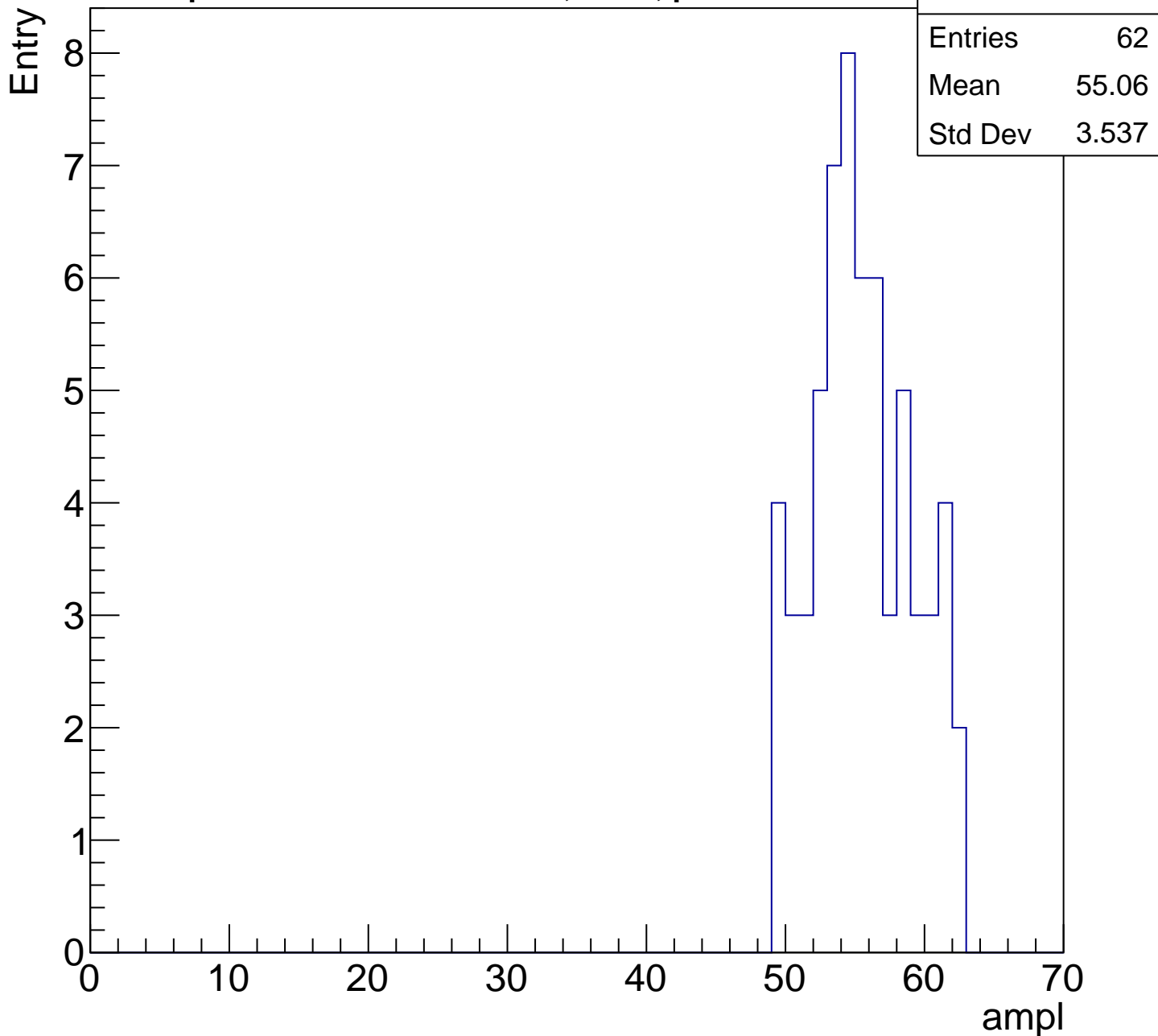
Entry

Entries	54
Mean	48.89
Std Dev	2.923



# B1L103S, U3-ch53, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

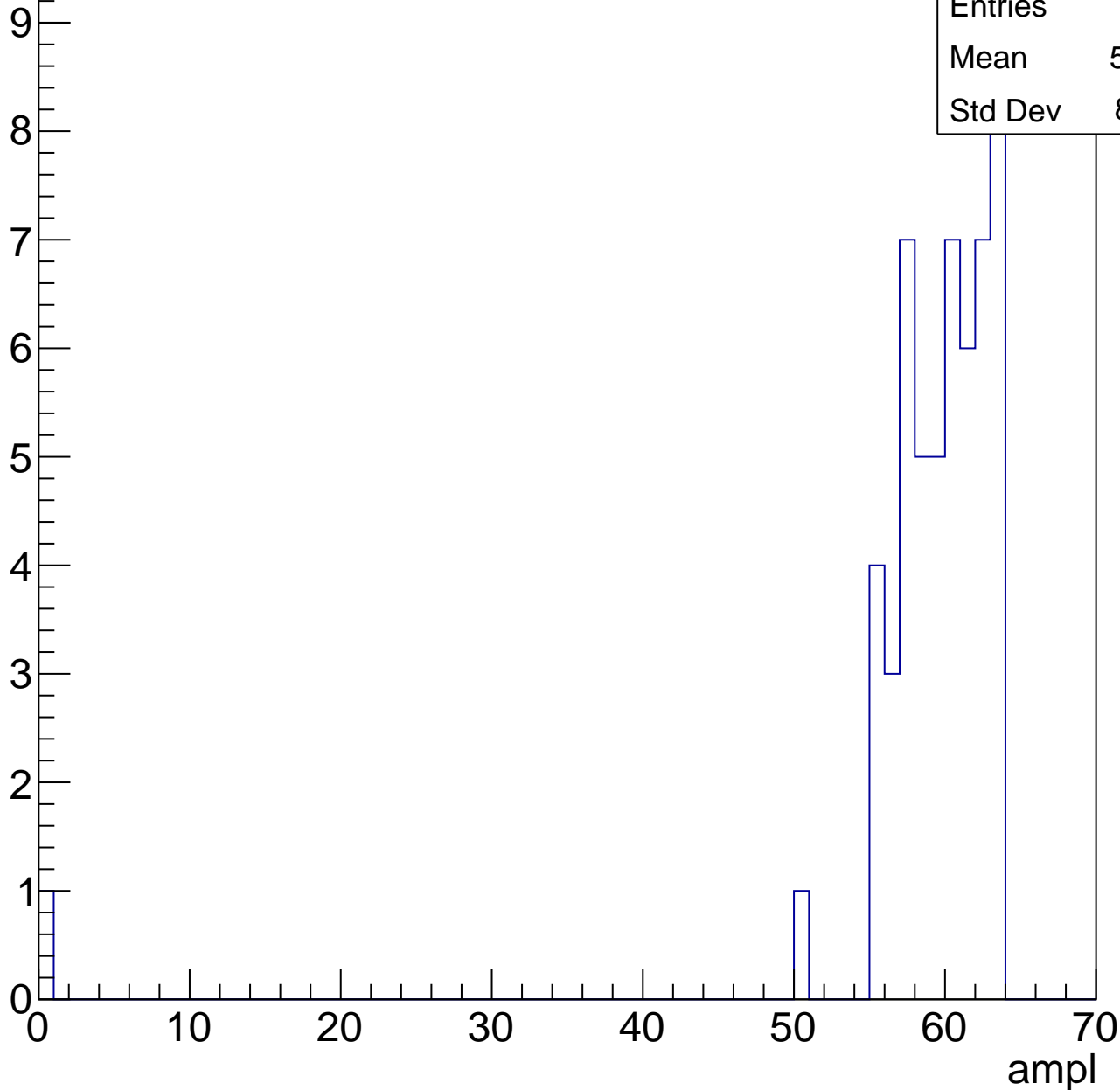


# B1L103S, U3-ch53, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

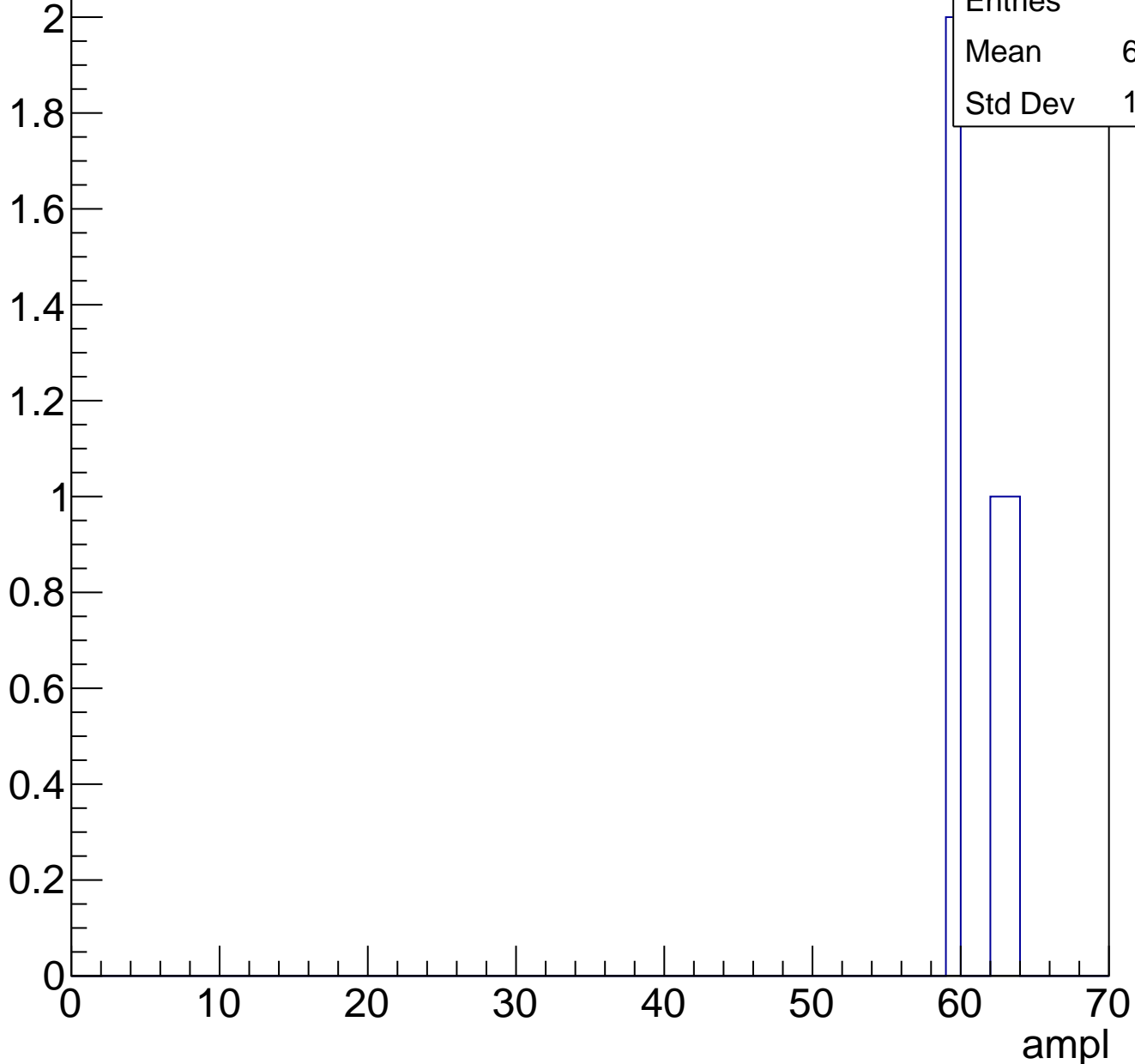
Entries	55
Mean	58.35
Std Dev	8.421



# B1L103S, U3-ch53, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U3-ch53, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U3-ch54, adc0

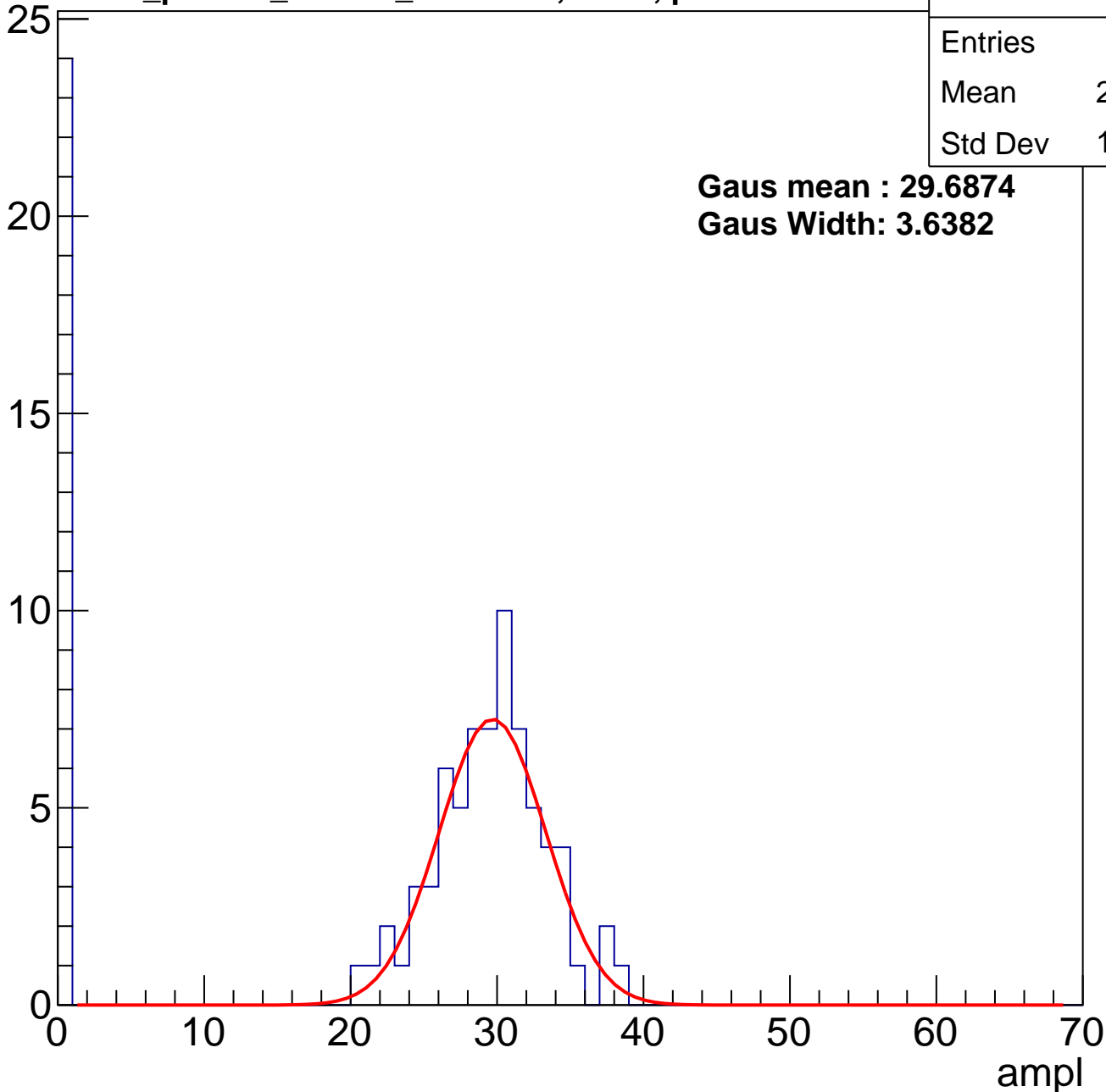
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	94
Mean	21.67
Std Dev	13.09

**Gaus mean : 29.6874**

**Gaus Width: 3.6382**

Entry



# B1L103S, U3-ch54, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	57
Mean	29.96
Std Dev	12.4

**Gaus mean : 35.2866**

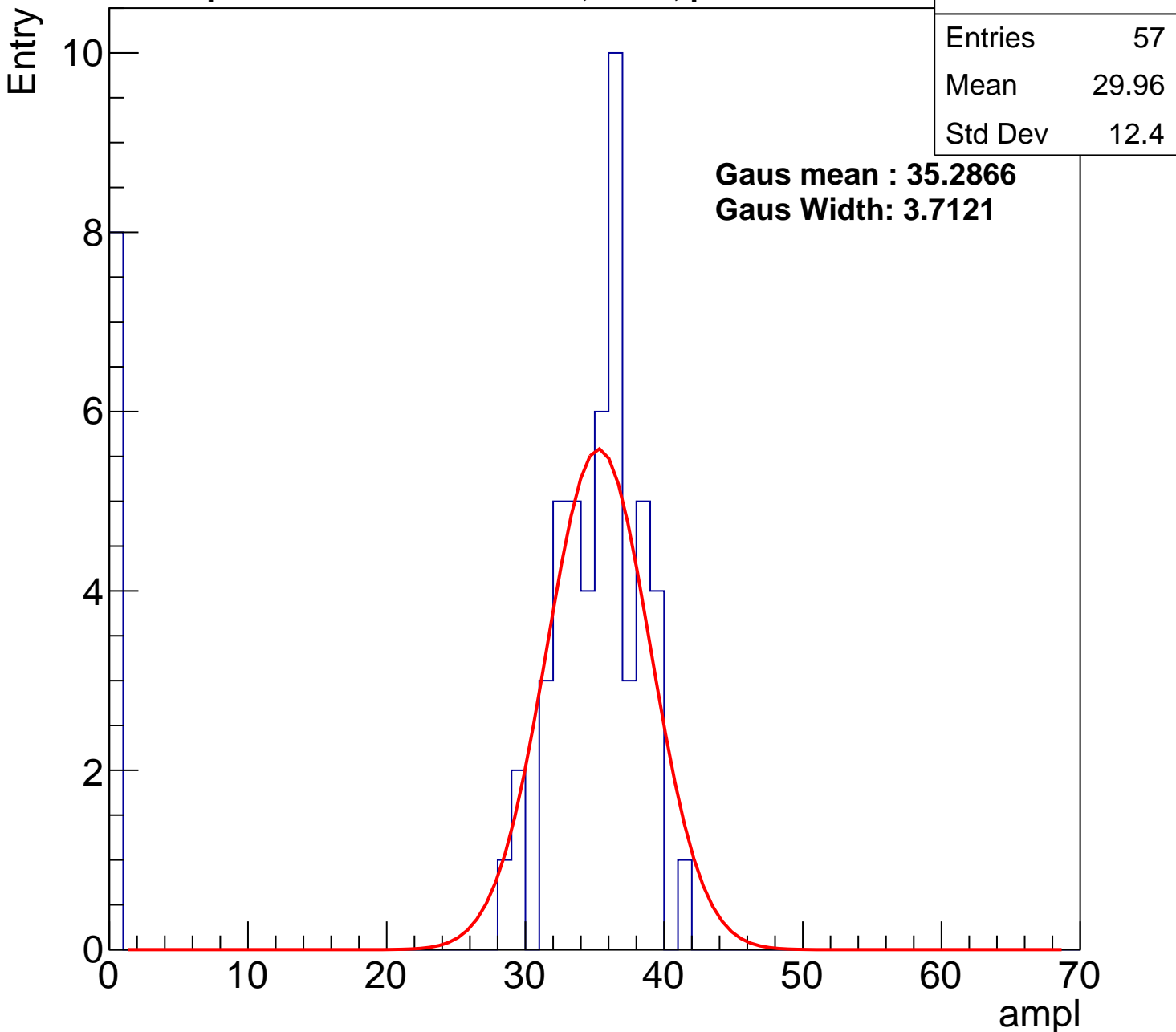
**Gaus Width: 3.7121**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch54, adc2

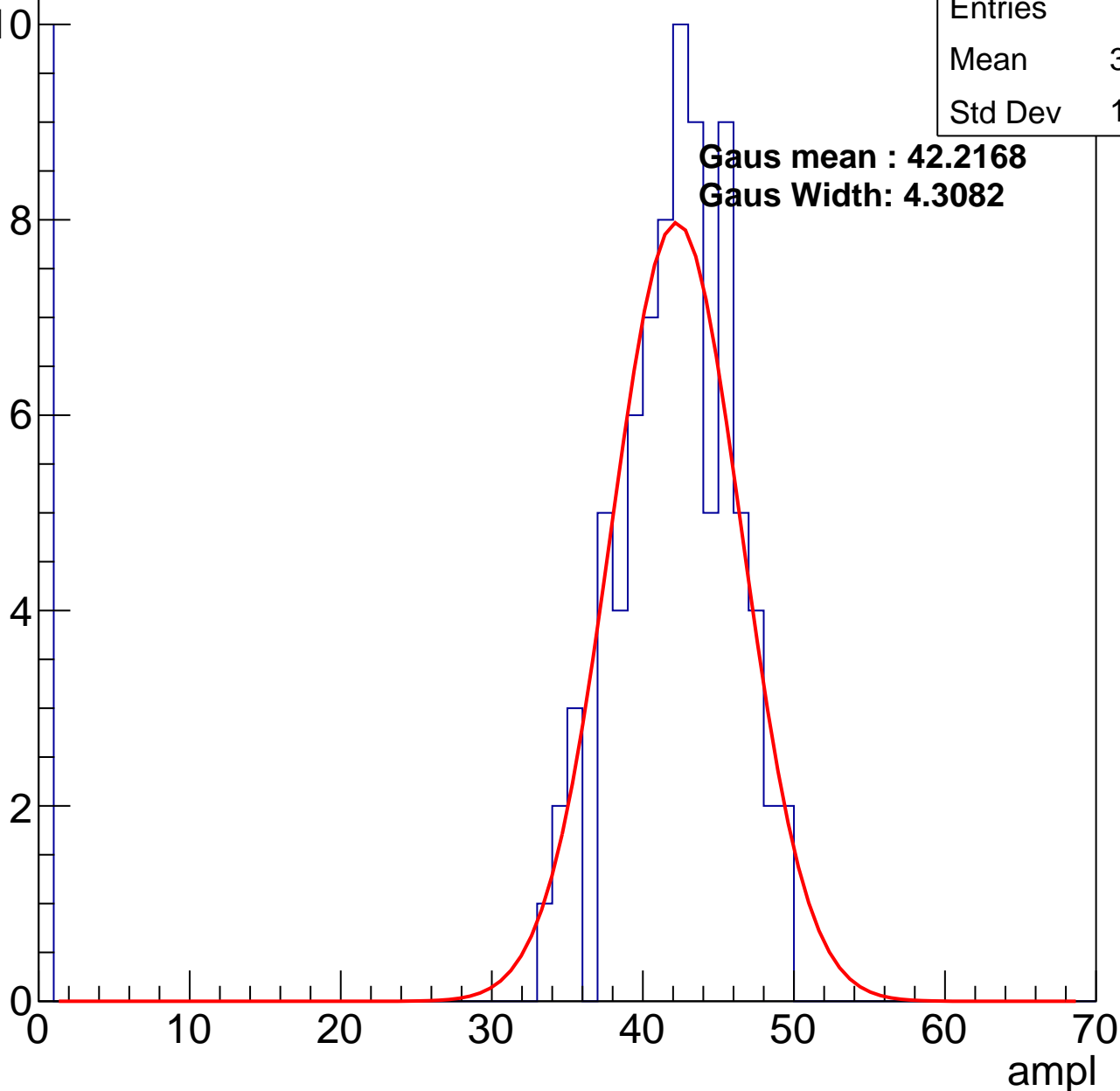
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	92
Mean	37.27
Std Dev	13.46

**Gaus mean : 42.2168**

**Gaus Width: 4.3082**

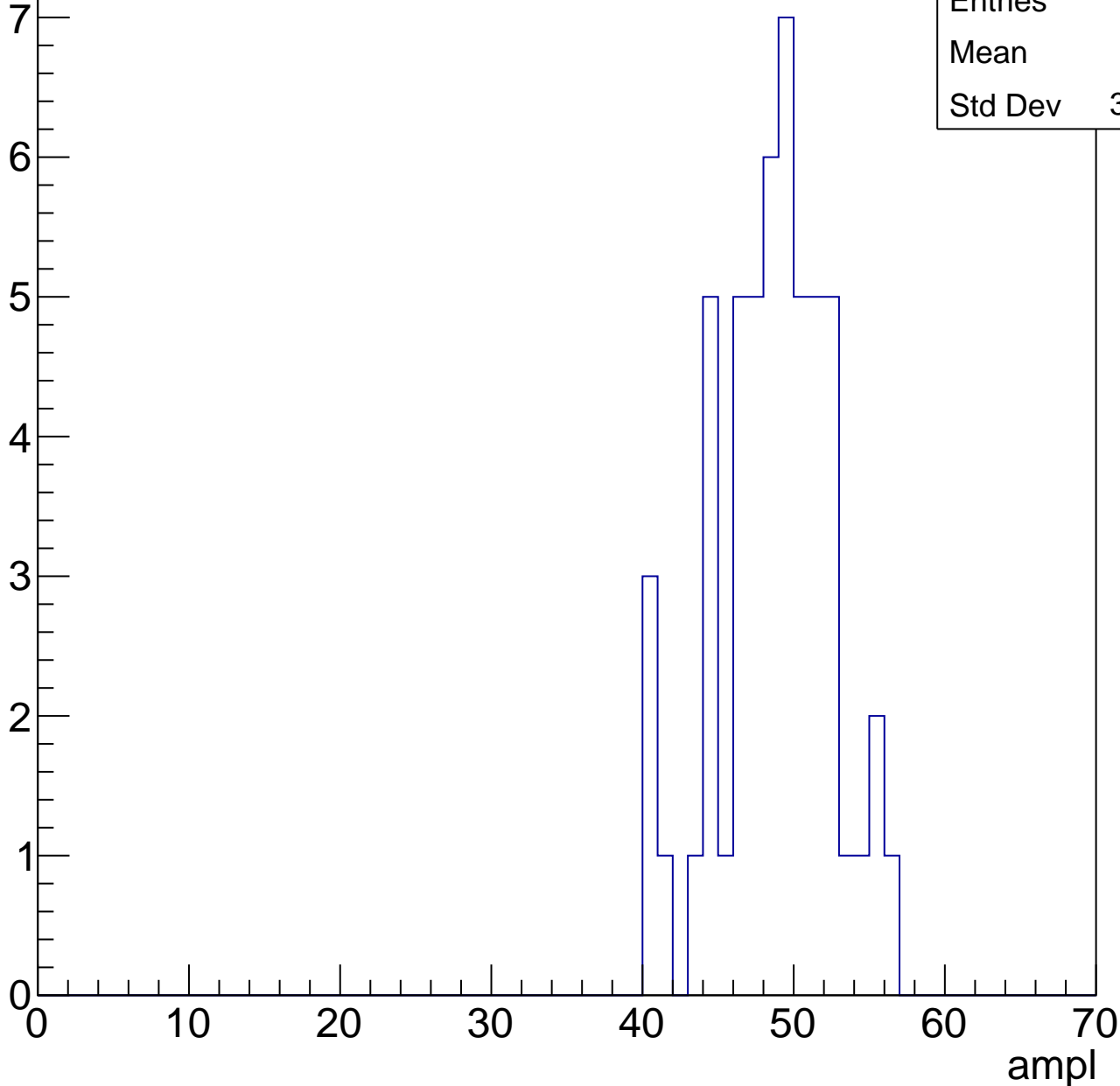


# B1L103S, U3-ch54, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	54
Mean	48.2
Std Dev	3.734

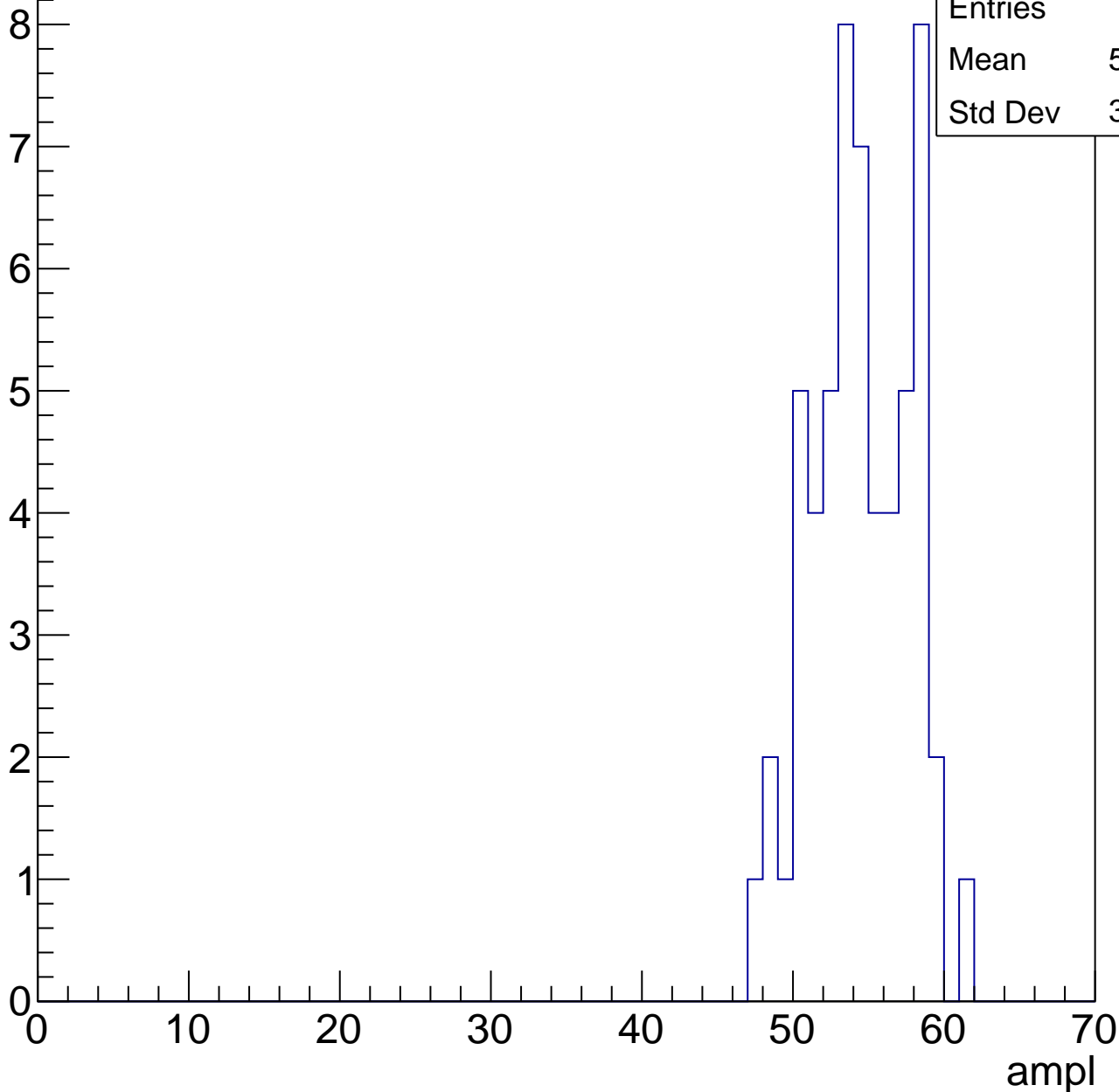


# B1L103S, U3-ch54, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	57
Mean	54.04
Std Dev	3.195

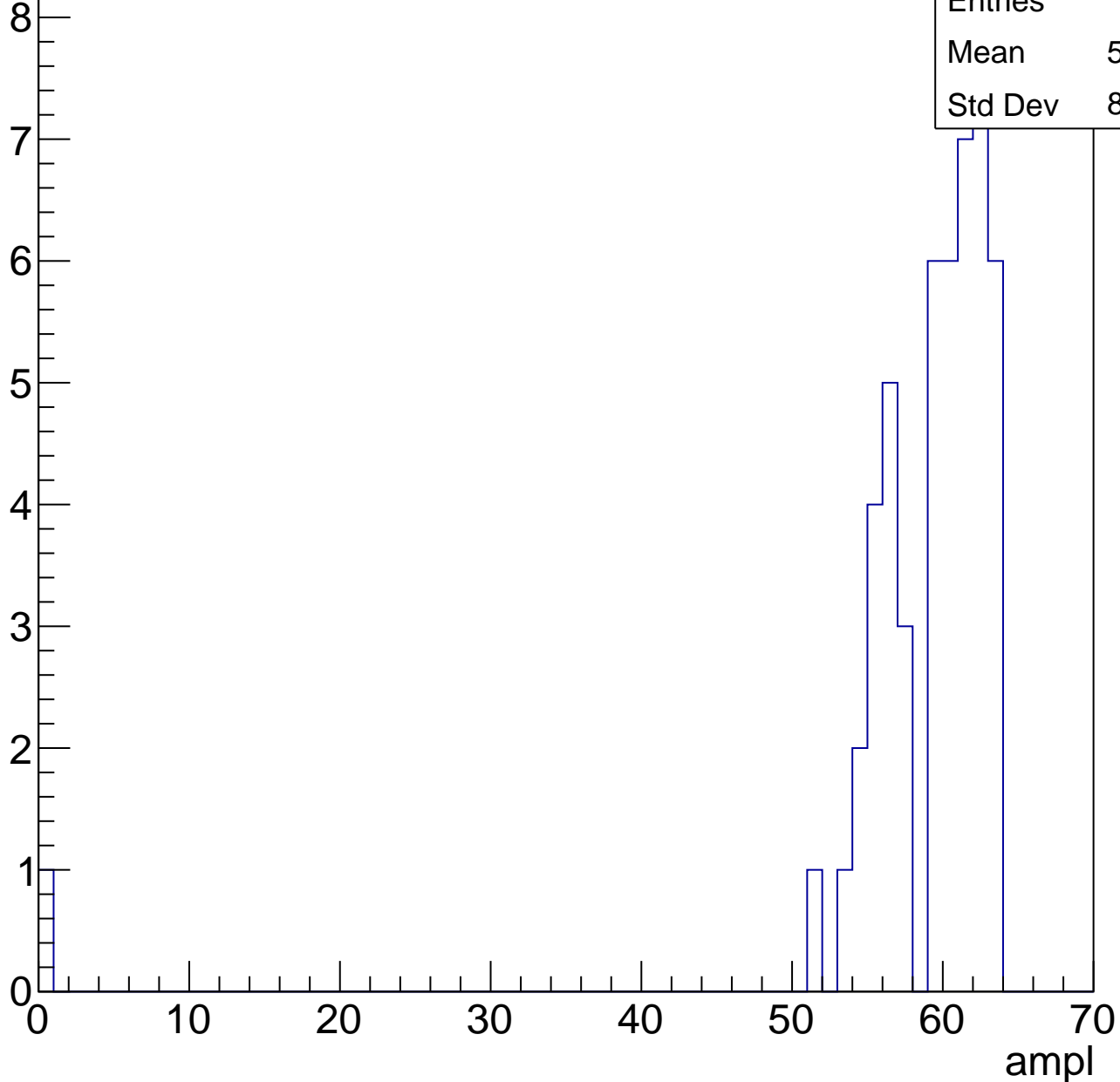


# B1L103S, U3-ch54, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	50
Mean	57.96
Std Dev	8.832



# B1L103S, U3-ch54, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

4  
3.5  
3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	18
Mean	60.33
Std Dev	2

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch54, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



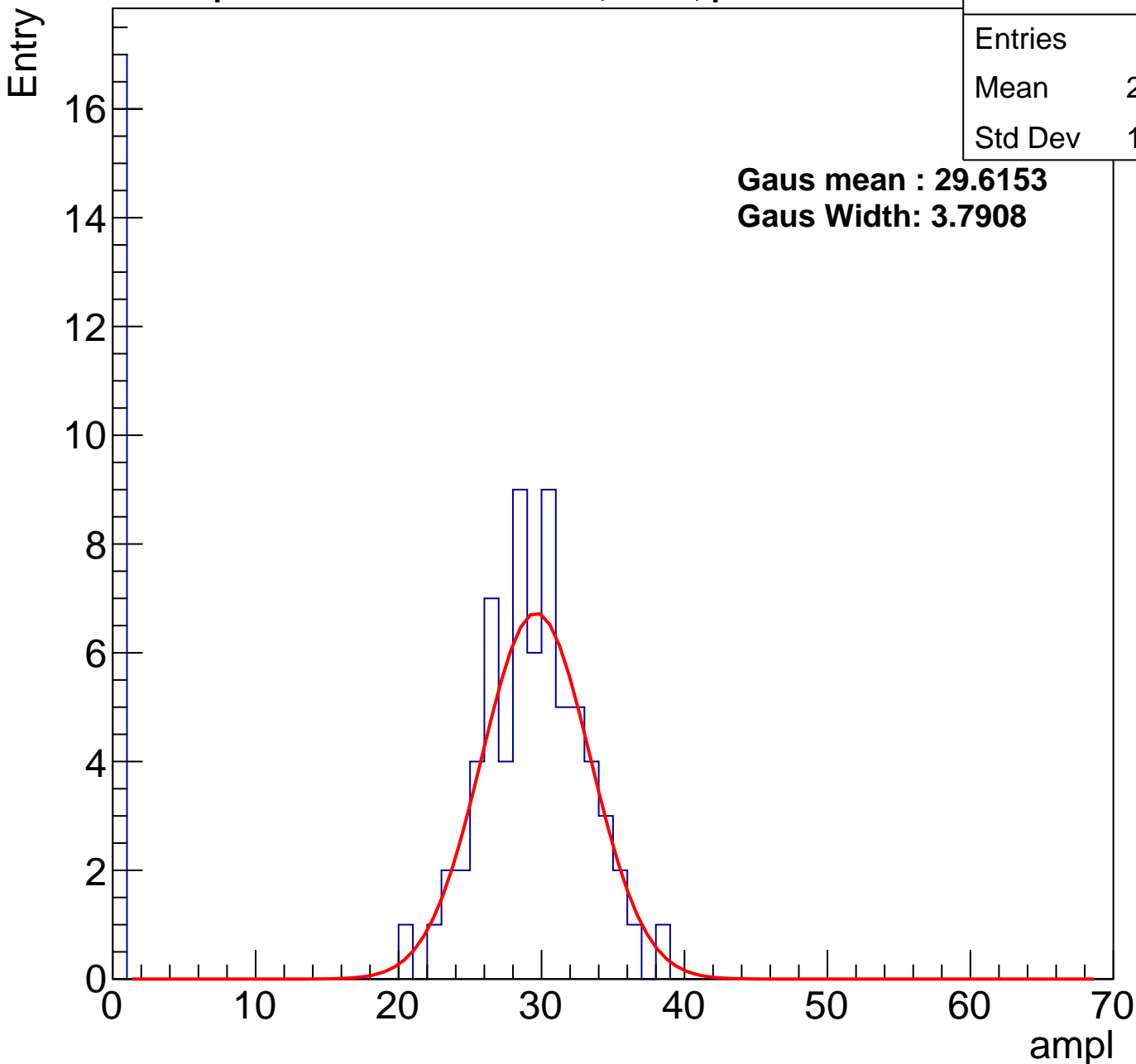
# B1L103S, U3-ch55, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	83
Mean	23.07
Std Dev	12.12

**Gaus mean : 29.6153**

**Gaus Width: 3.7908**



# B1L103S, U3-ch55, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	86
Mean	31.27
Std Dev	12.44

**Gaus mean : 36.1361**

**Gaus Width: 3.1159**

Entry

10

8

6

4

2

0

0

10

20

30

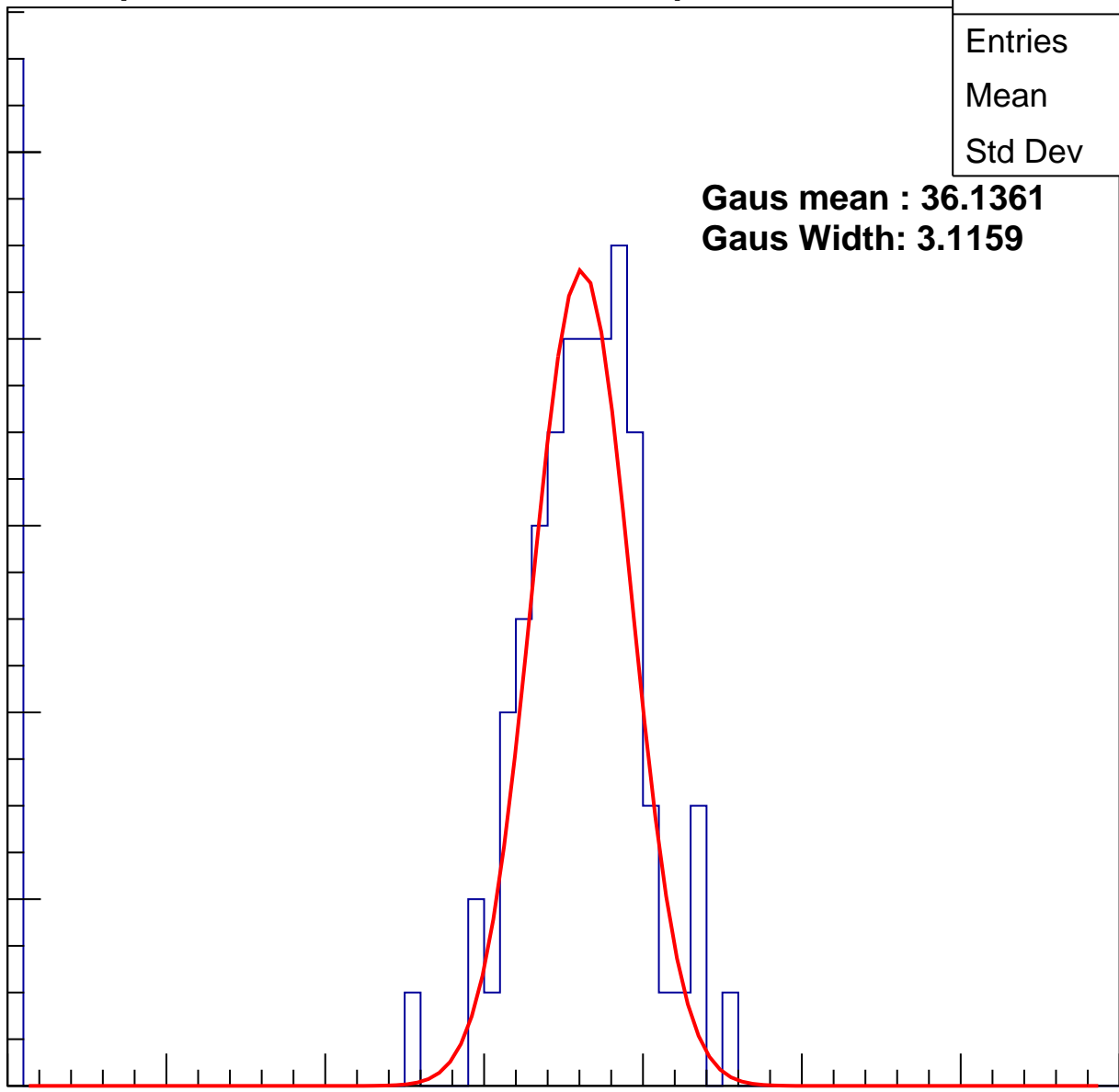
40

50

60

70

ampl



# B1L103S, U3-ch55, adc2

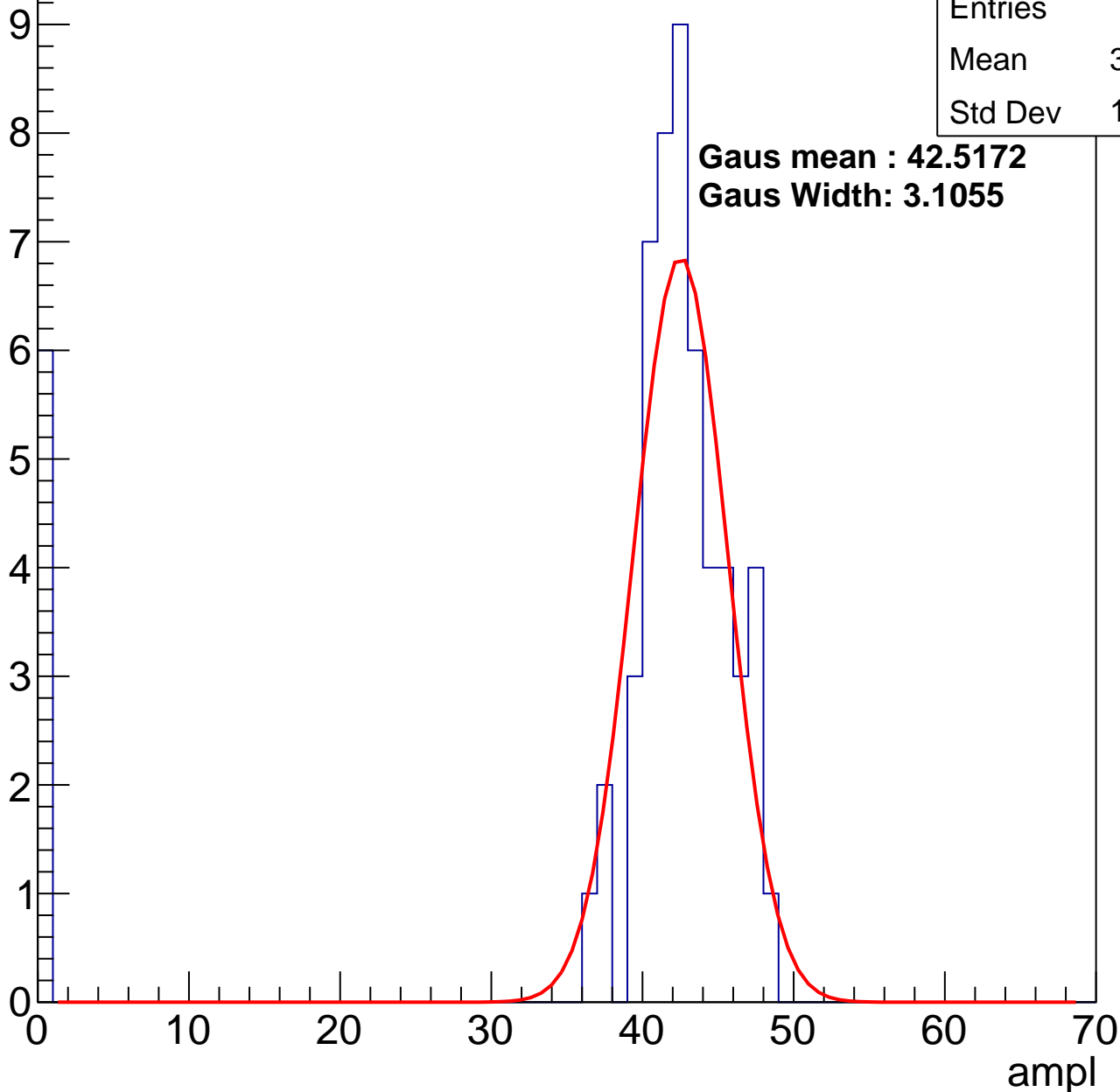
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	37.95
Std Dev	13.15

**Gaus mean : 42.5172**

**Gaus Width: 3.1055**

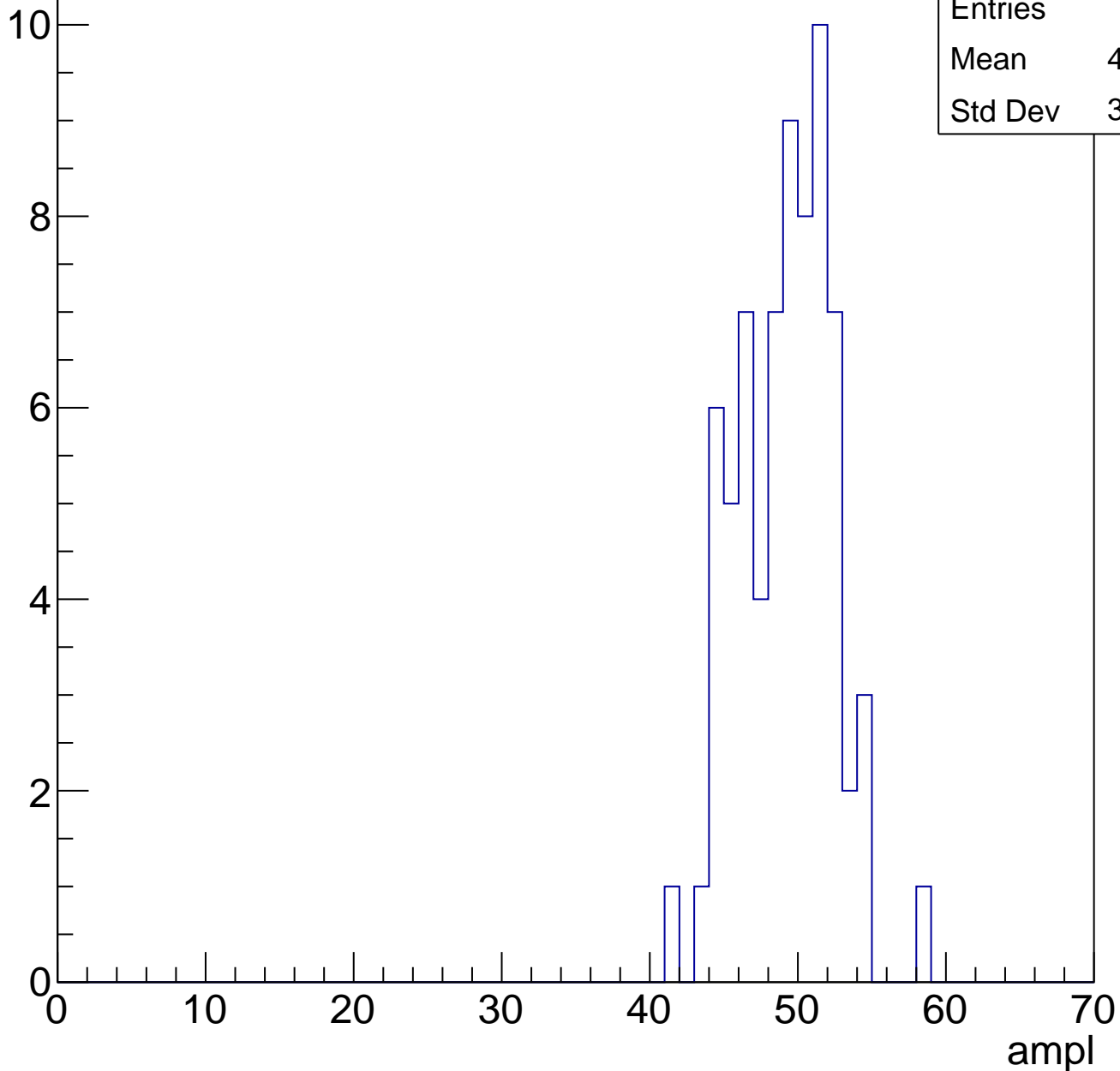


# B1L103S, U3-ch55, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	71
Mean	48.73
Std Dev	3.162

Entry

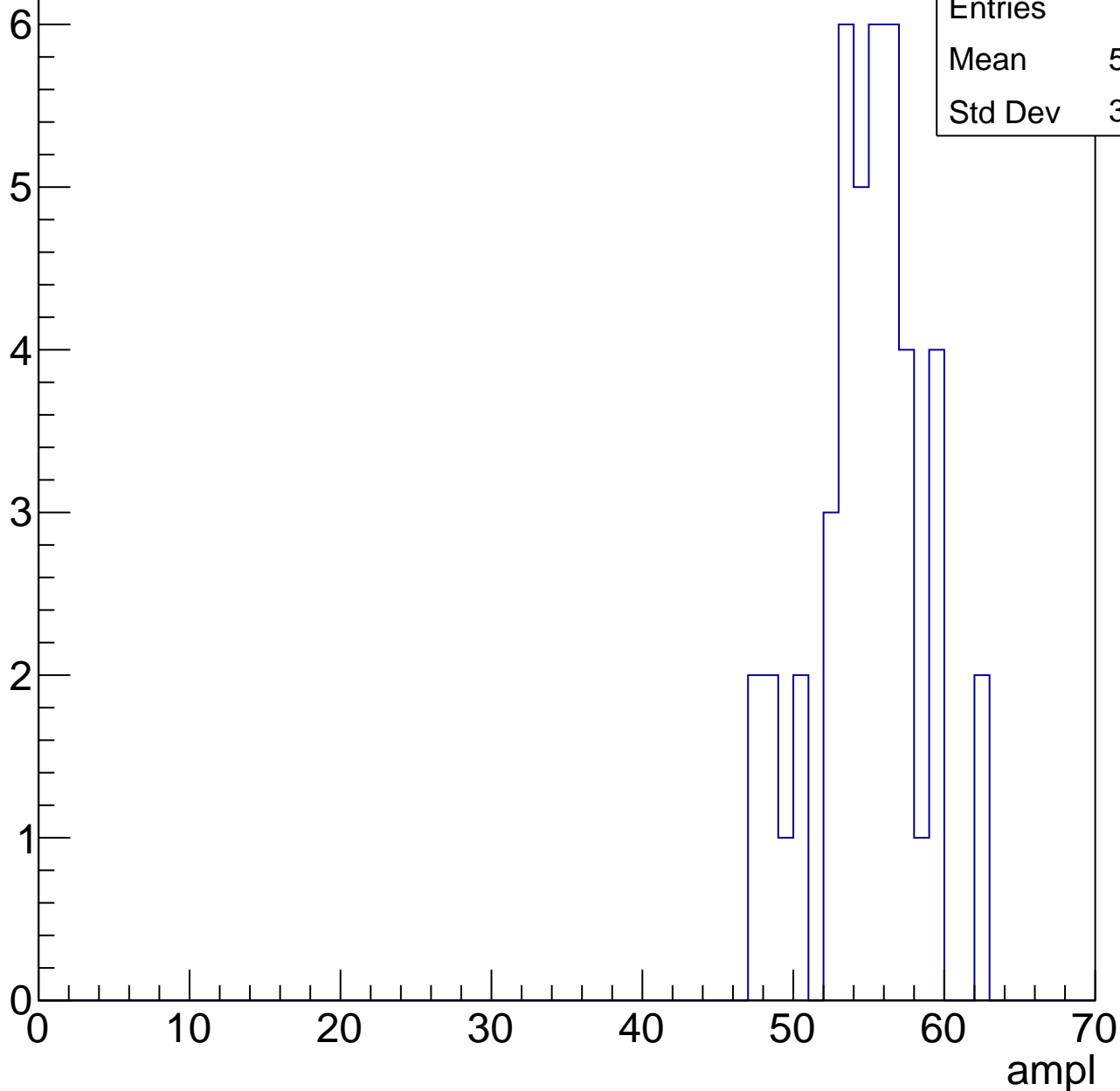


# B1L103S, U3-ch55, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	44
Mean	54.43
Std Dev	3.525



# B1L103S, U3-ch55, adc5

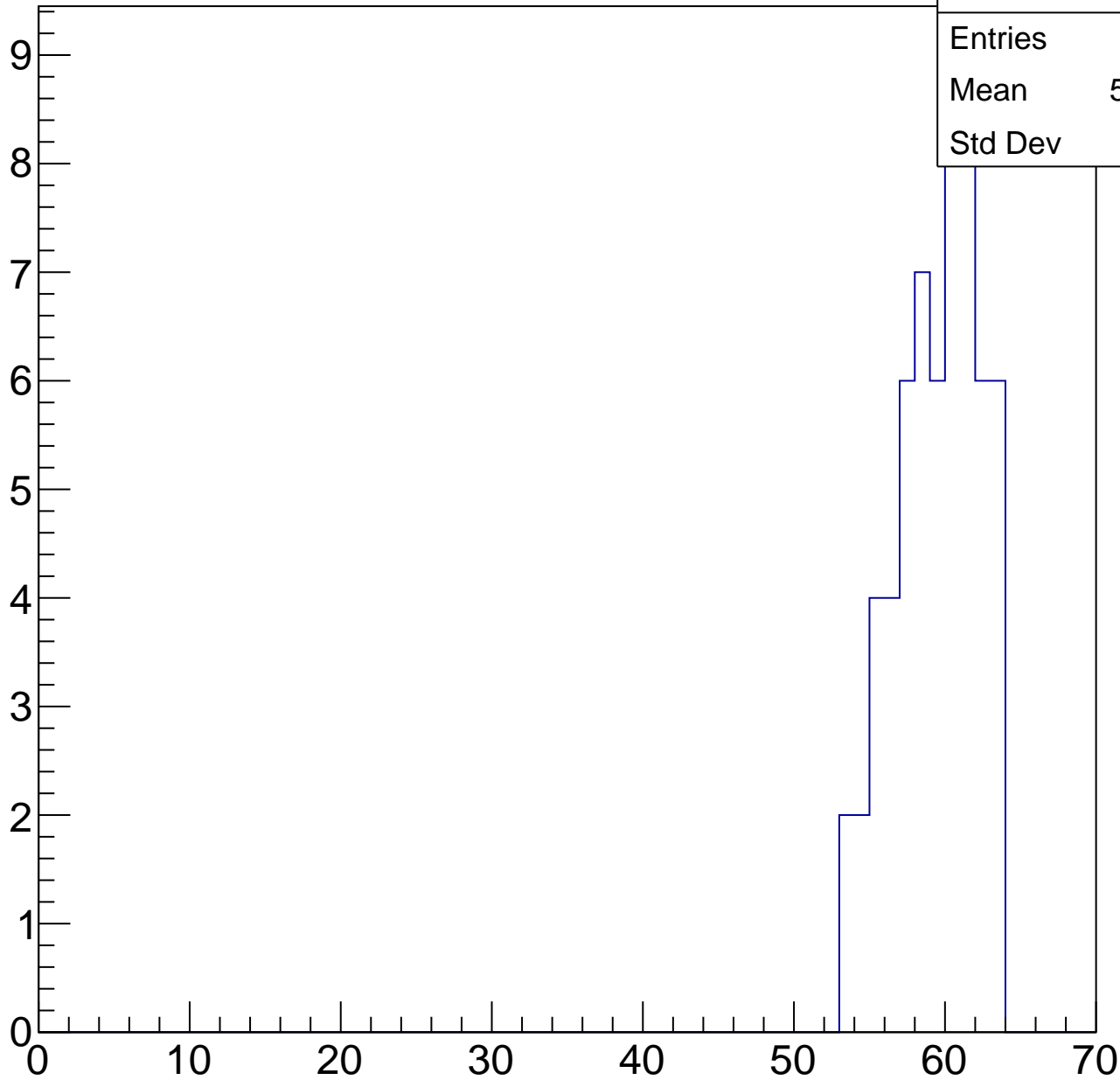
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	60
Mean	58.97
Std Dev	2.72

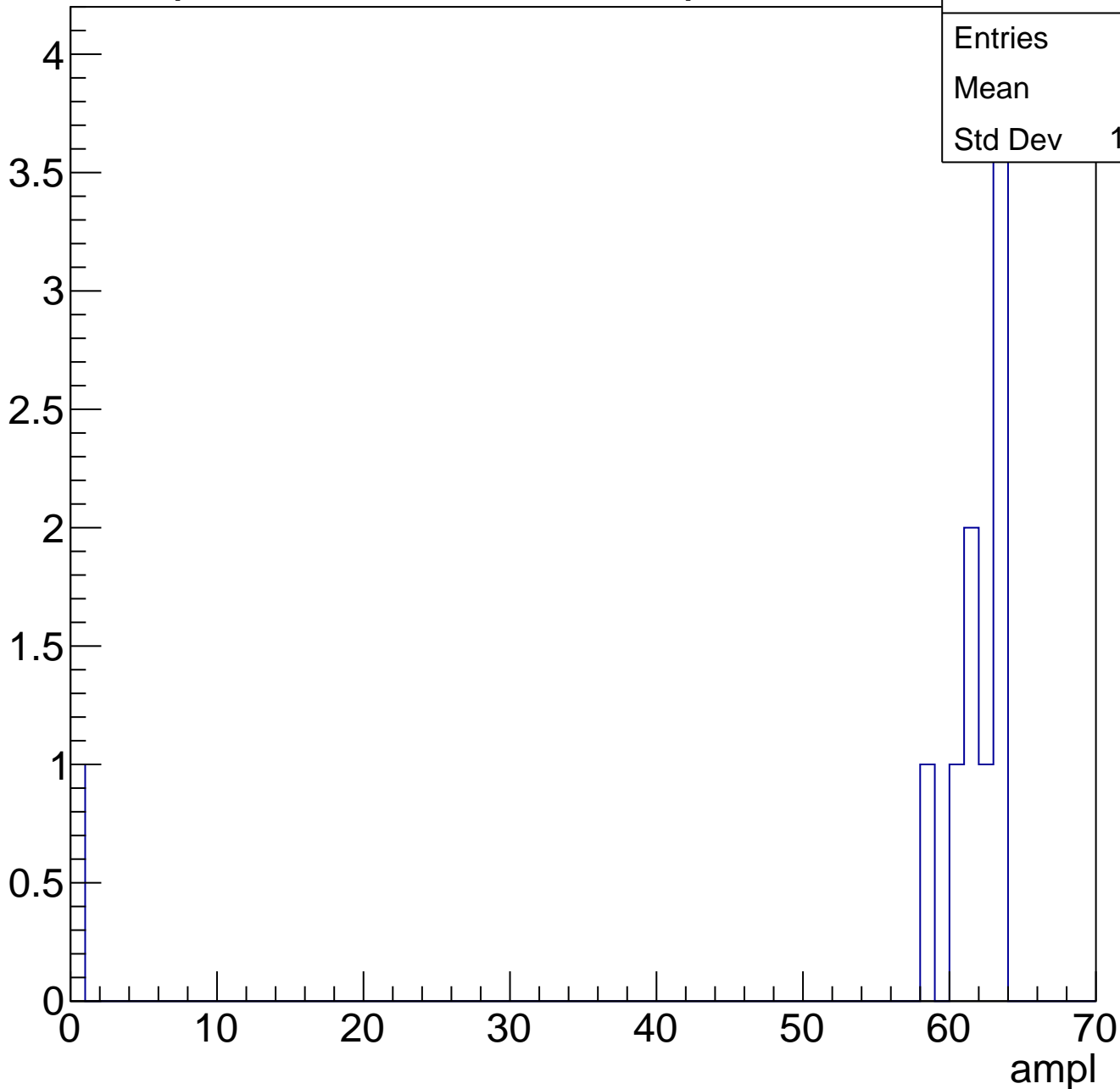
ampl



# B1L103S, U3-ch55, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



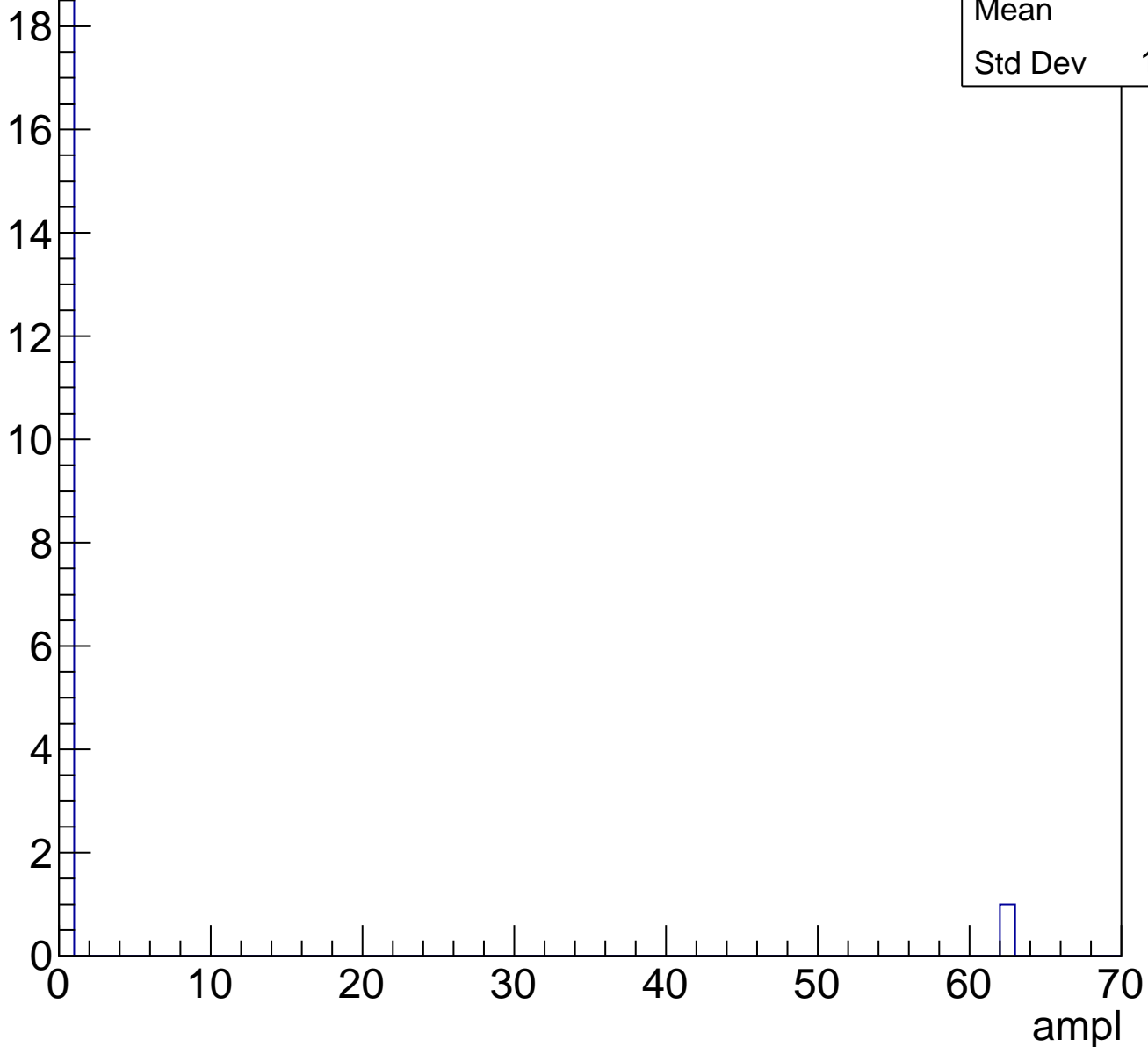


# B1L103S, U3-ch55, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51

Entry



# B1L103S, U3-ch56, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	87
Mean	21.87
Std Dev	11.22

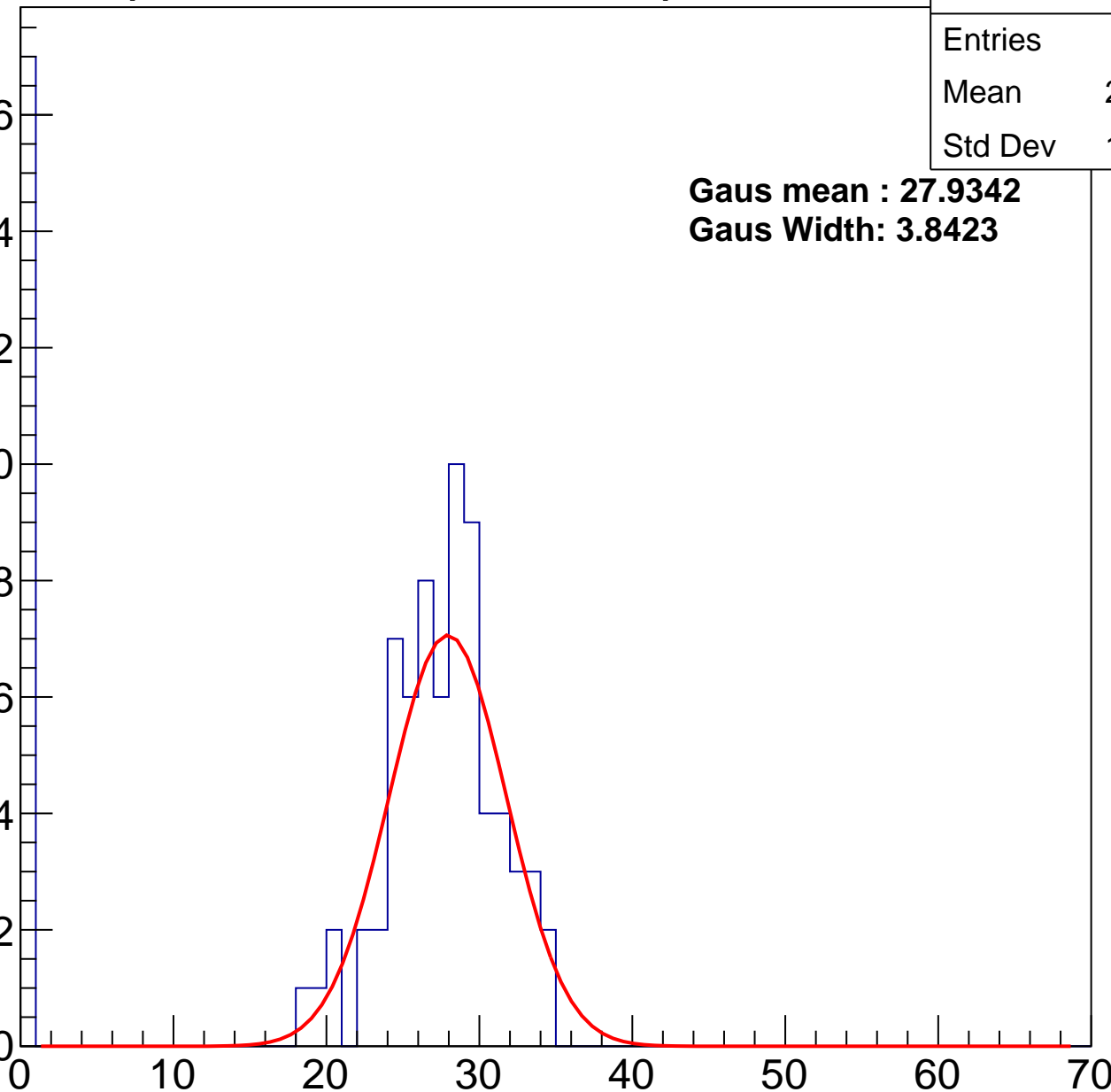
**Gaus mean : 27.9342**

**Gaus Width: 3.8423**

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U3-ch56, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	79
Mean	31.99
Std Dev	9.018

**Gaus mean : 34.8914**

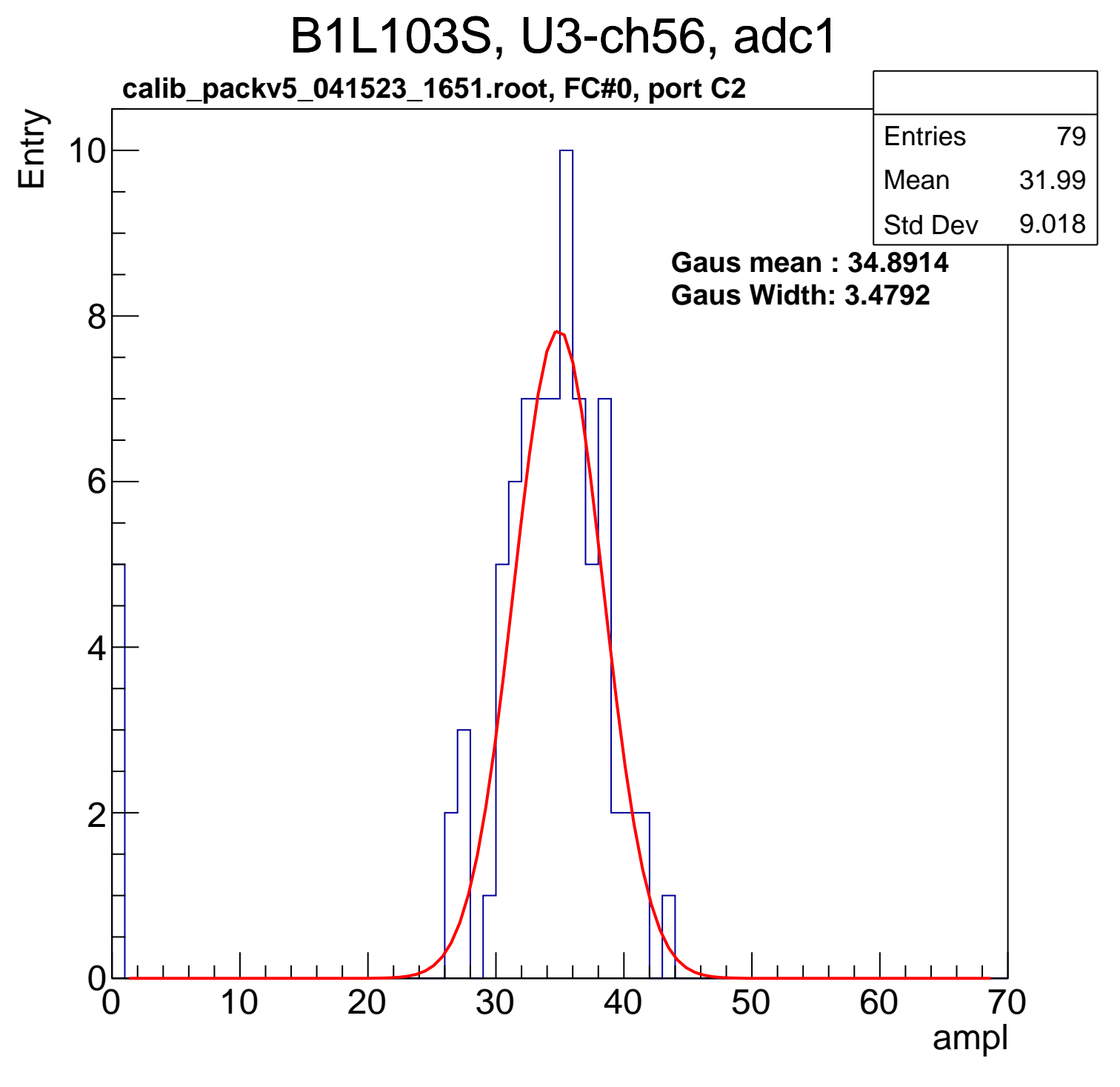
**Gaus Width: 3.4792**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch56, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	65
Mean	34.4
Std Dev	15.81

**Gaus mean : 41.6671**

**Gaus Width: 4.0779**

Entry

10

8

6

4

2

0

0

10

20

30

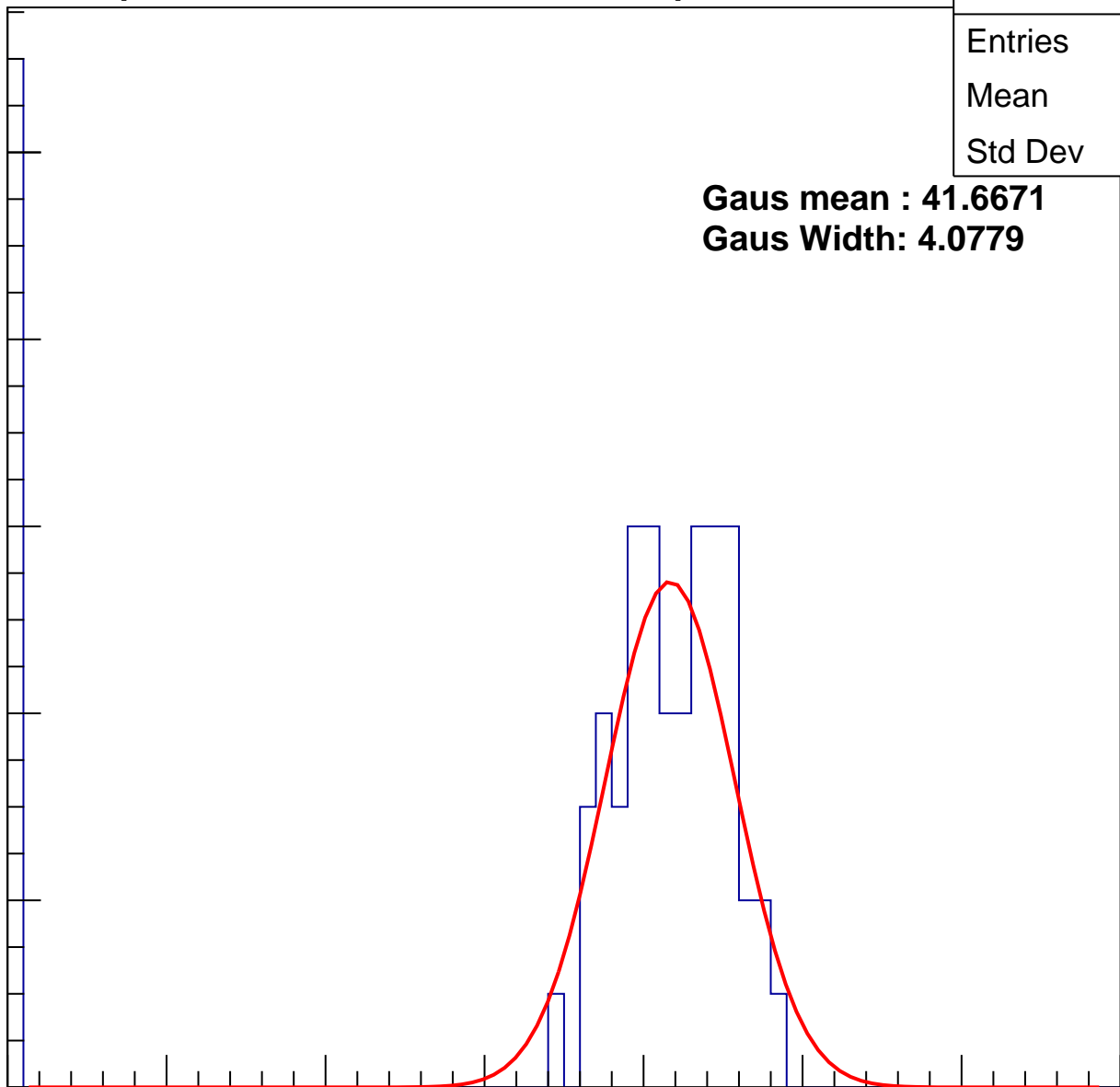
40

50

60

70

ampl

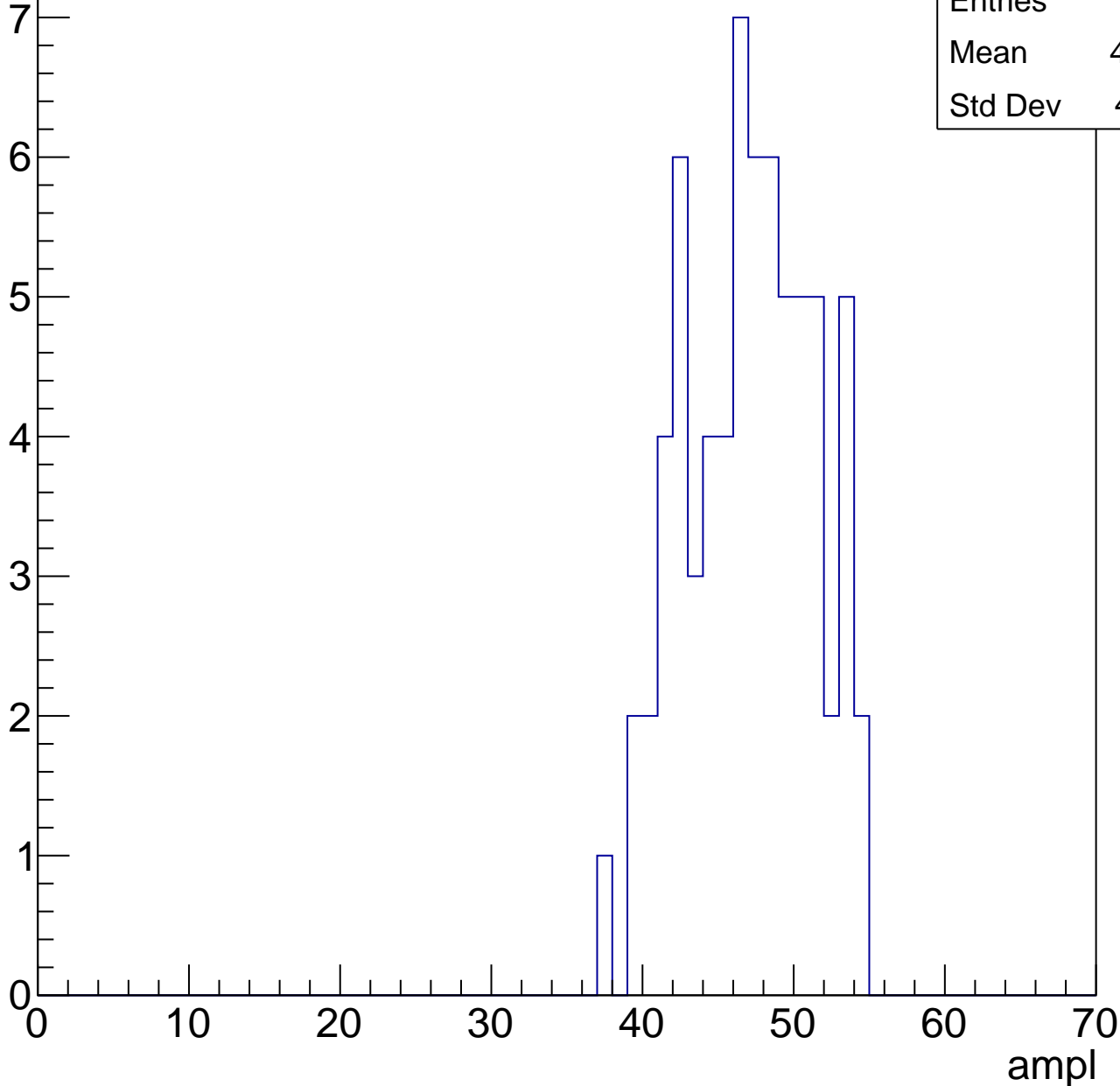


# B1L103S, U3-ch56, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	46.59
Std Dev	4.161

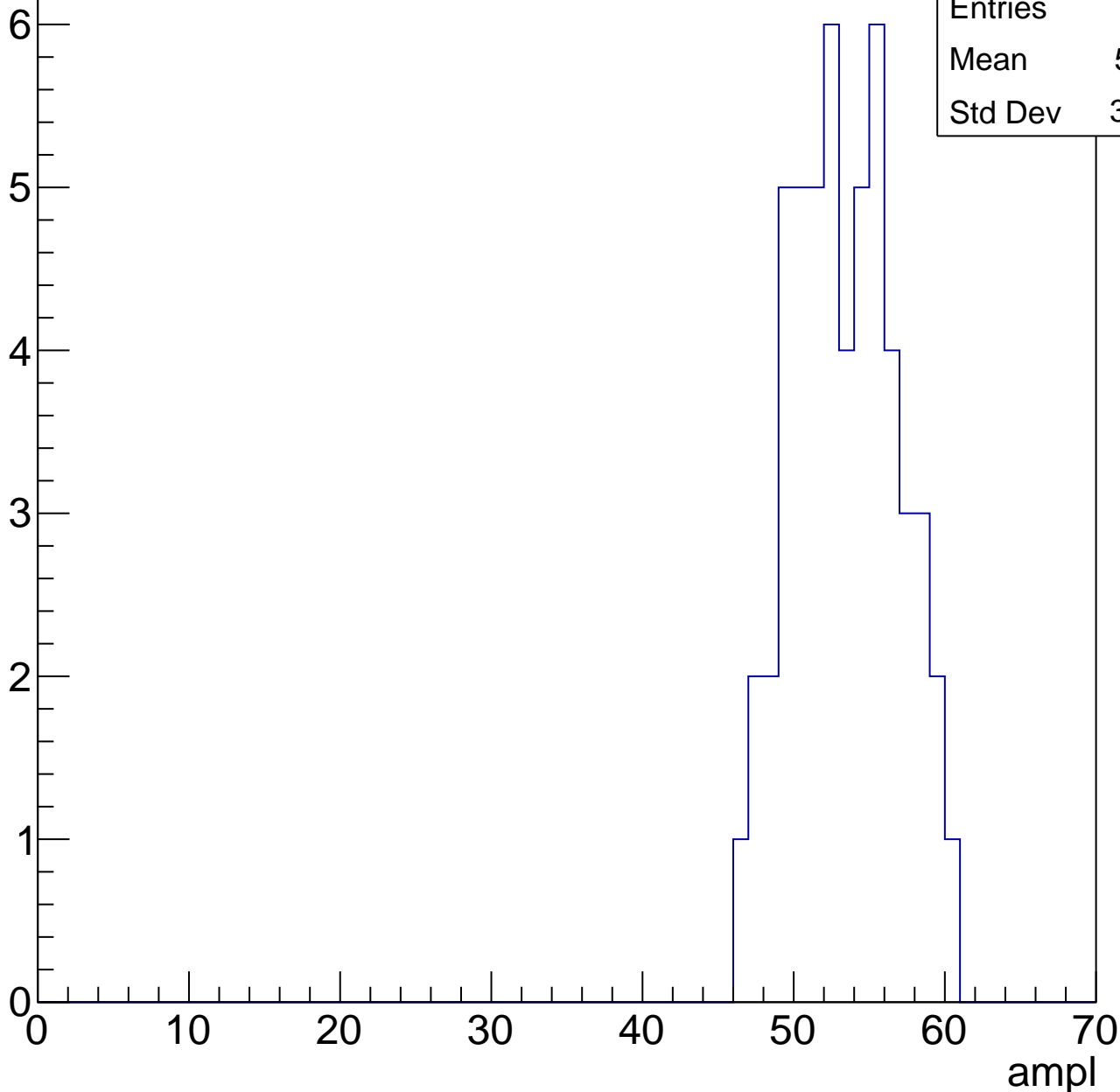


# B1L103S, U3-ch56, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	54
Mean	52.91
Std Dev	3.417

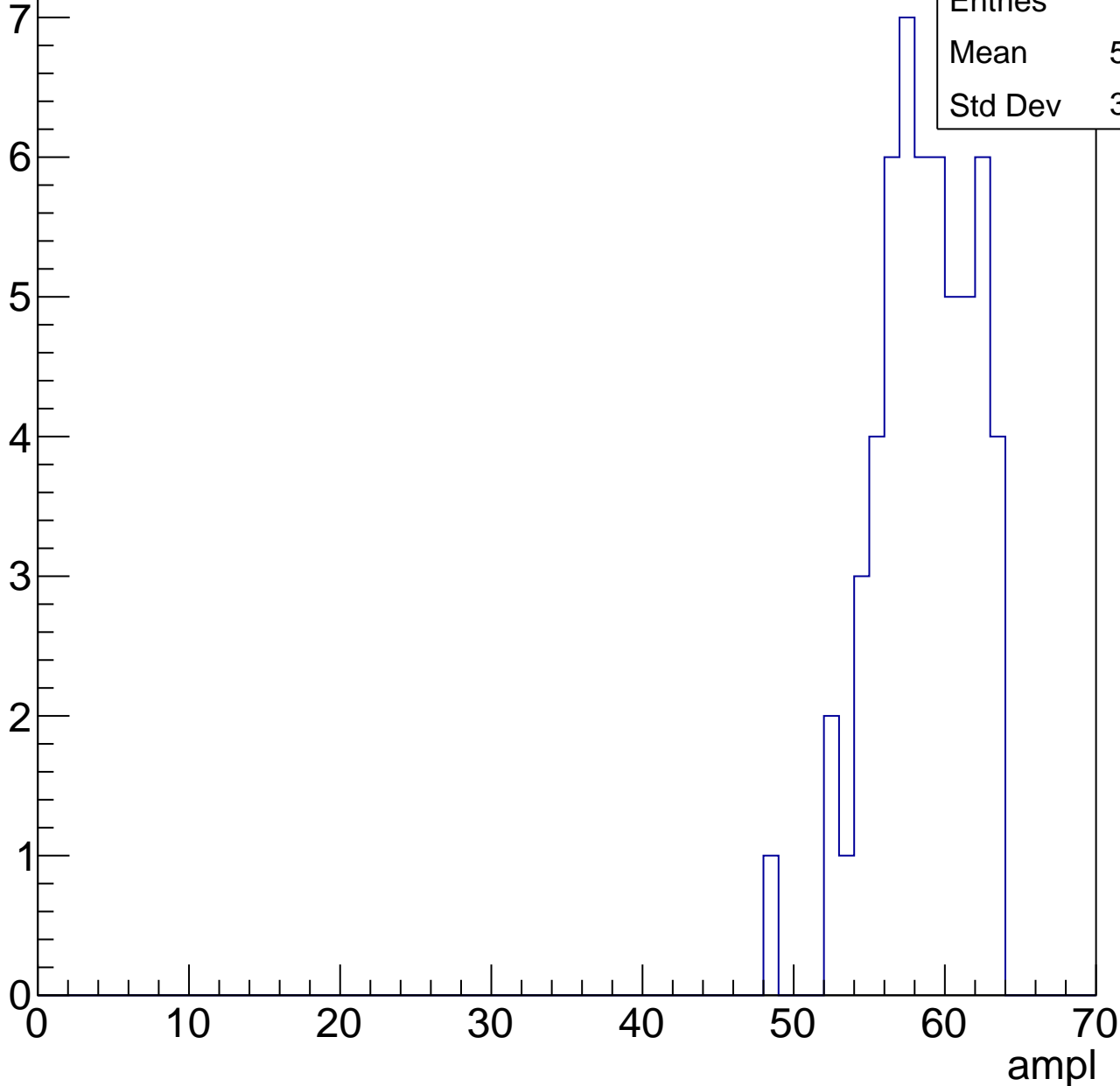


# B1L103S, U3-ch56, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	56
Mean	58.09
Std Dev	3.214

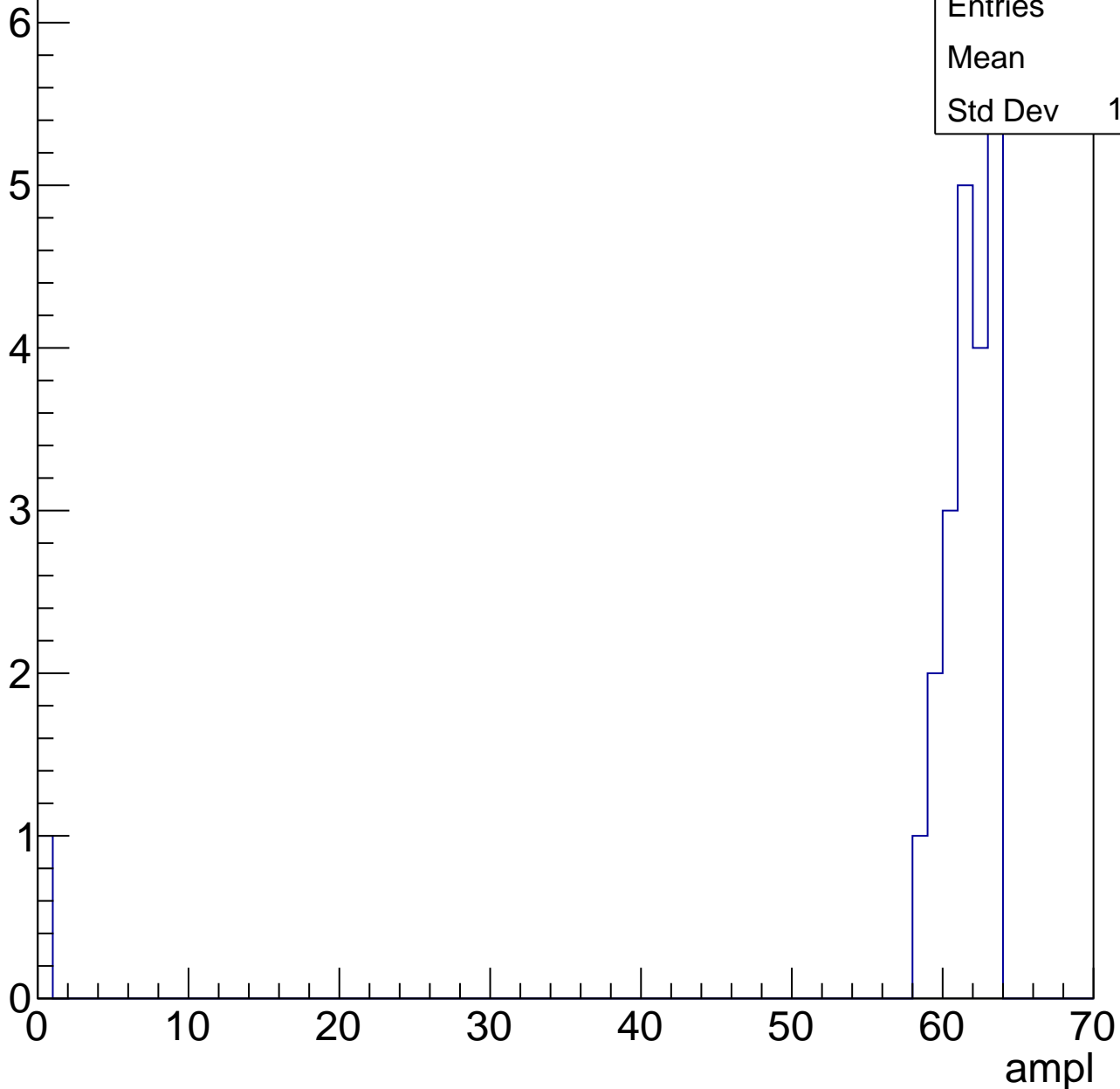


# B1L103S, U3-ch56, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	22
Mean	58.5
Std Dev	12.85

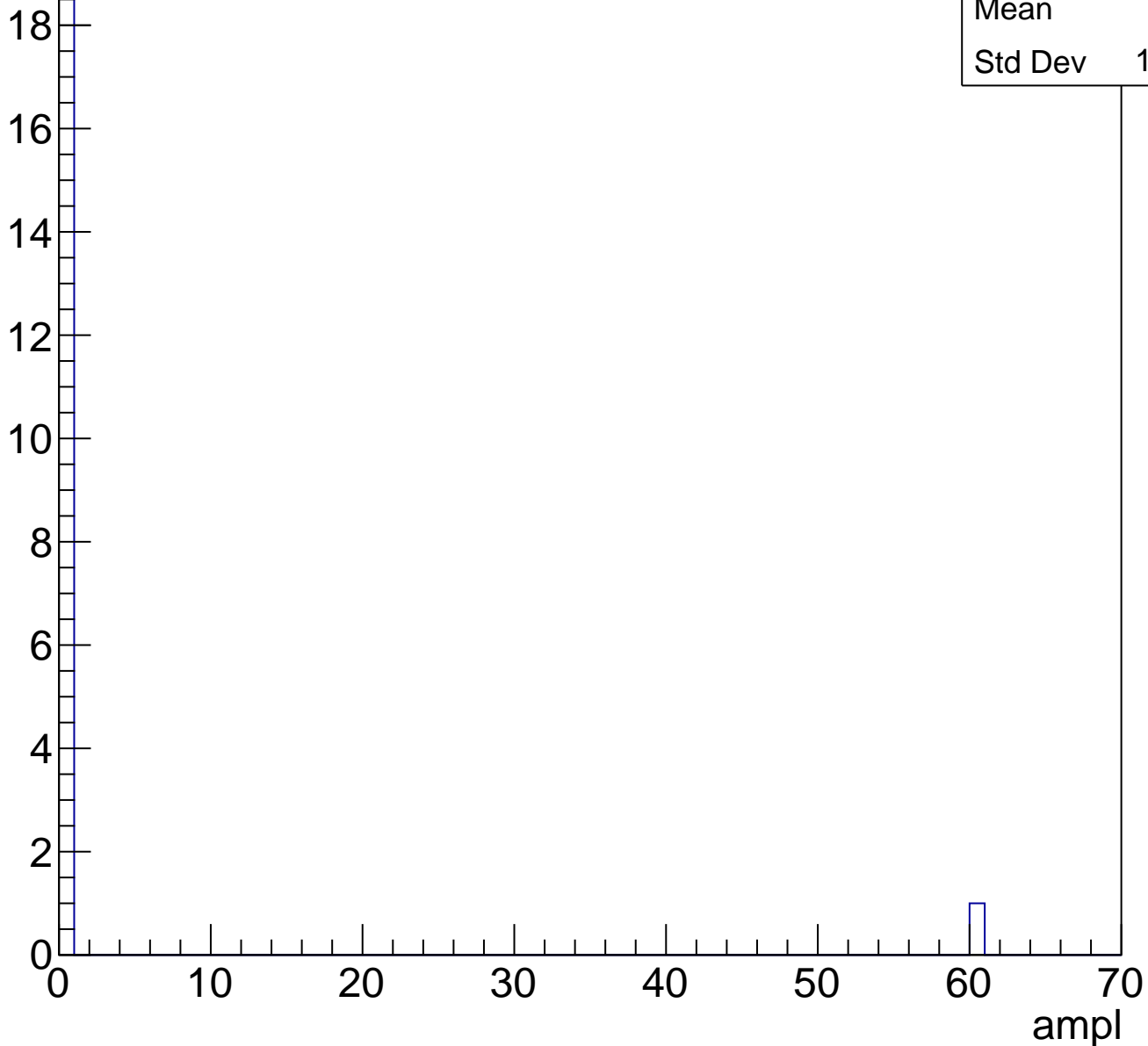




# B1L103S, U3-ch56, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	20
Mean	3
Std Dev	13.08

# B1L103S, U3-ch57, adc0

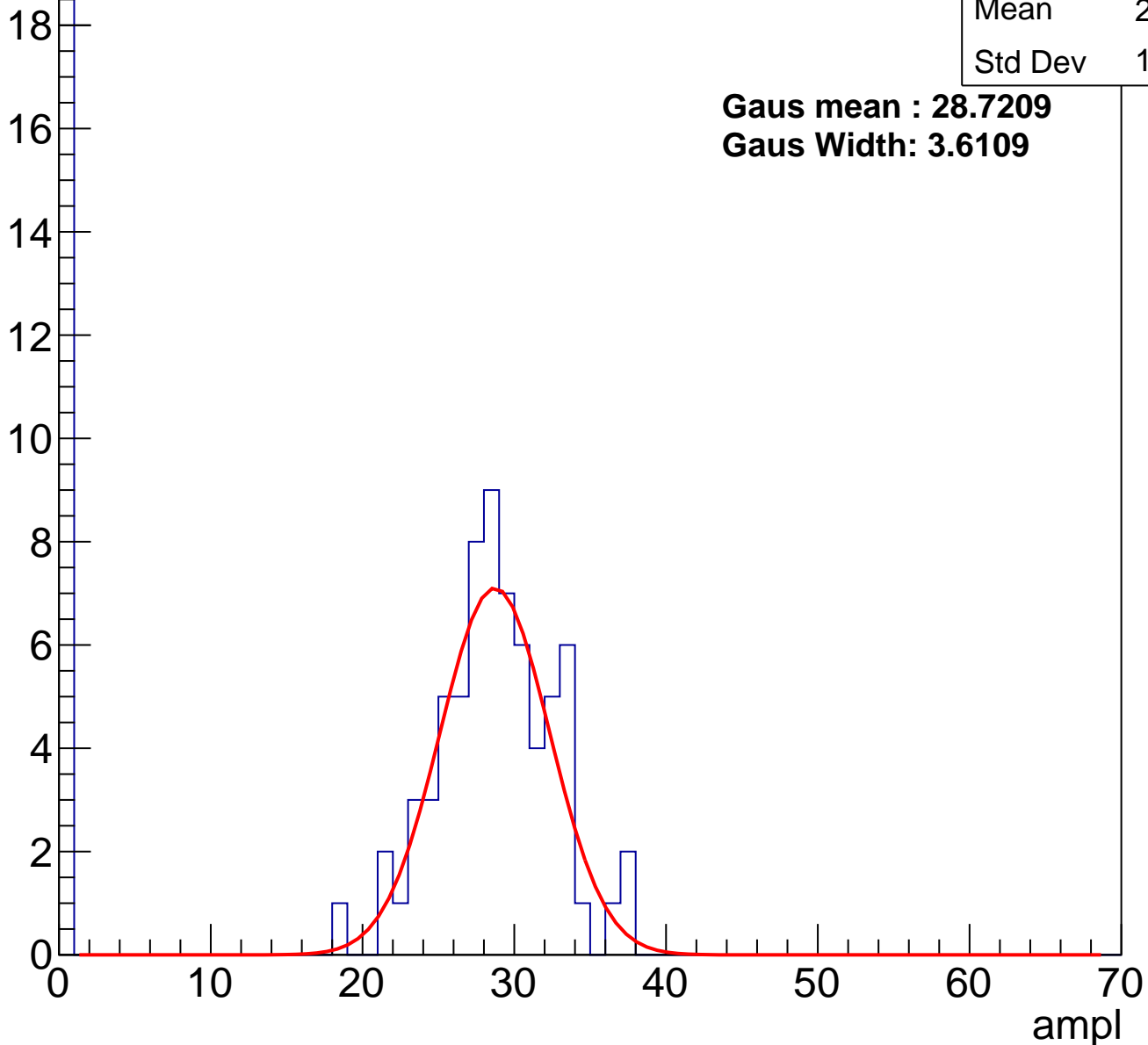
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	88
Mean	22.22
Std Dev	12.13

**Gaus mean : 28.7209**

**Gaus Width: 3.6109**

Entry



# B1L103S, U3-ch57, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	80
Mean	31.19
Std Dev	11.61

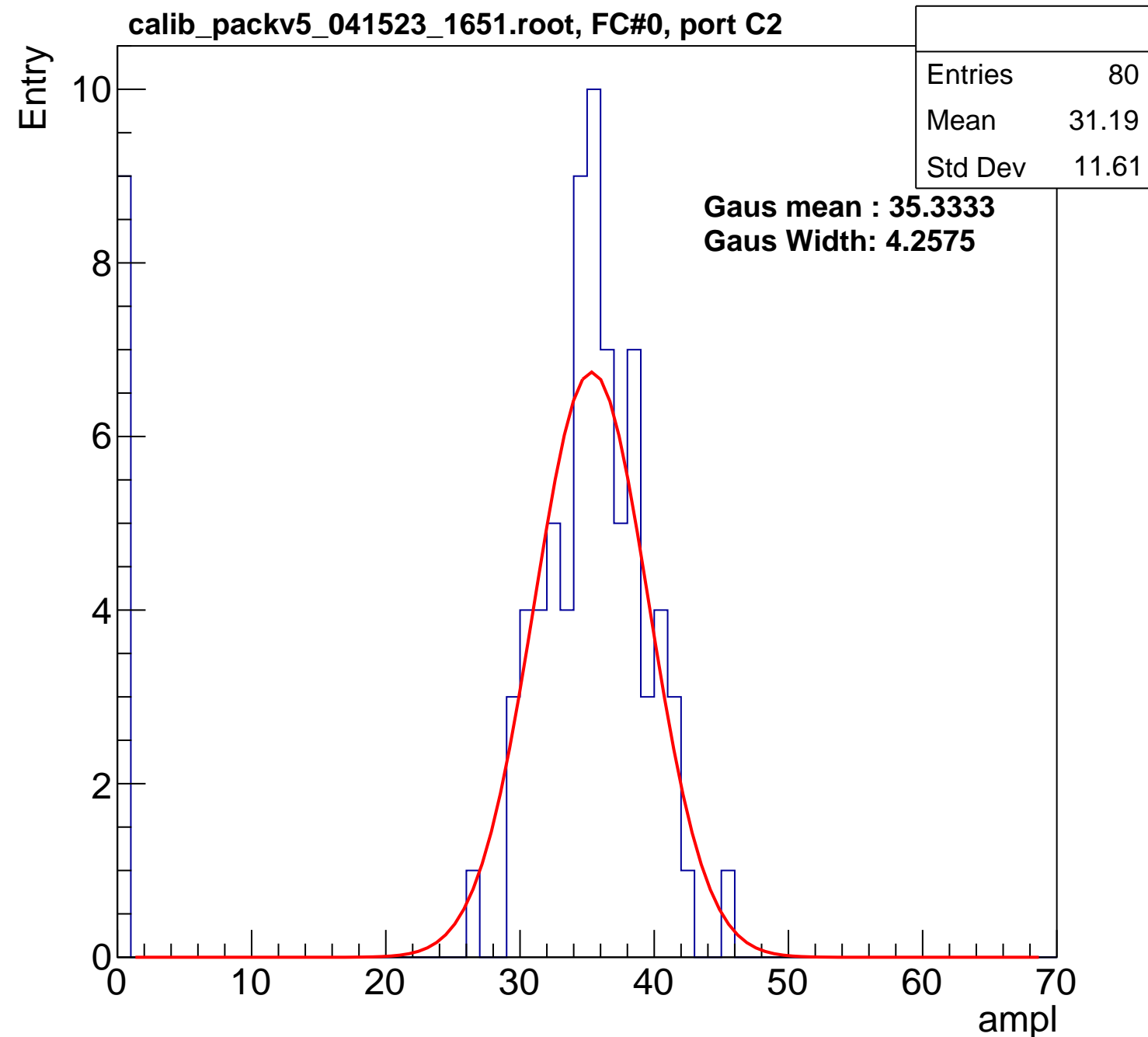
**Gaus mean : 35.3333**

**Gaus Width: 4.2575**

Entry

10  
8  
6  
4  
2  
0

ampl



# B1L103S, U3-ch57, adc2

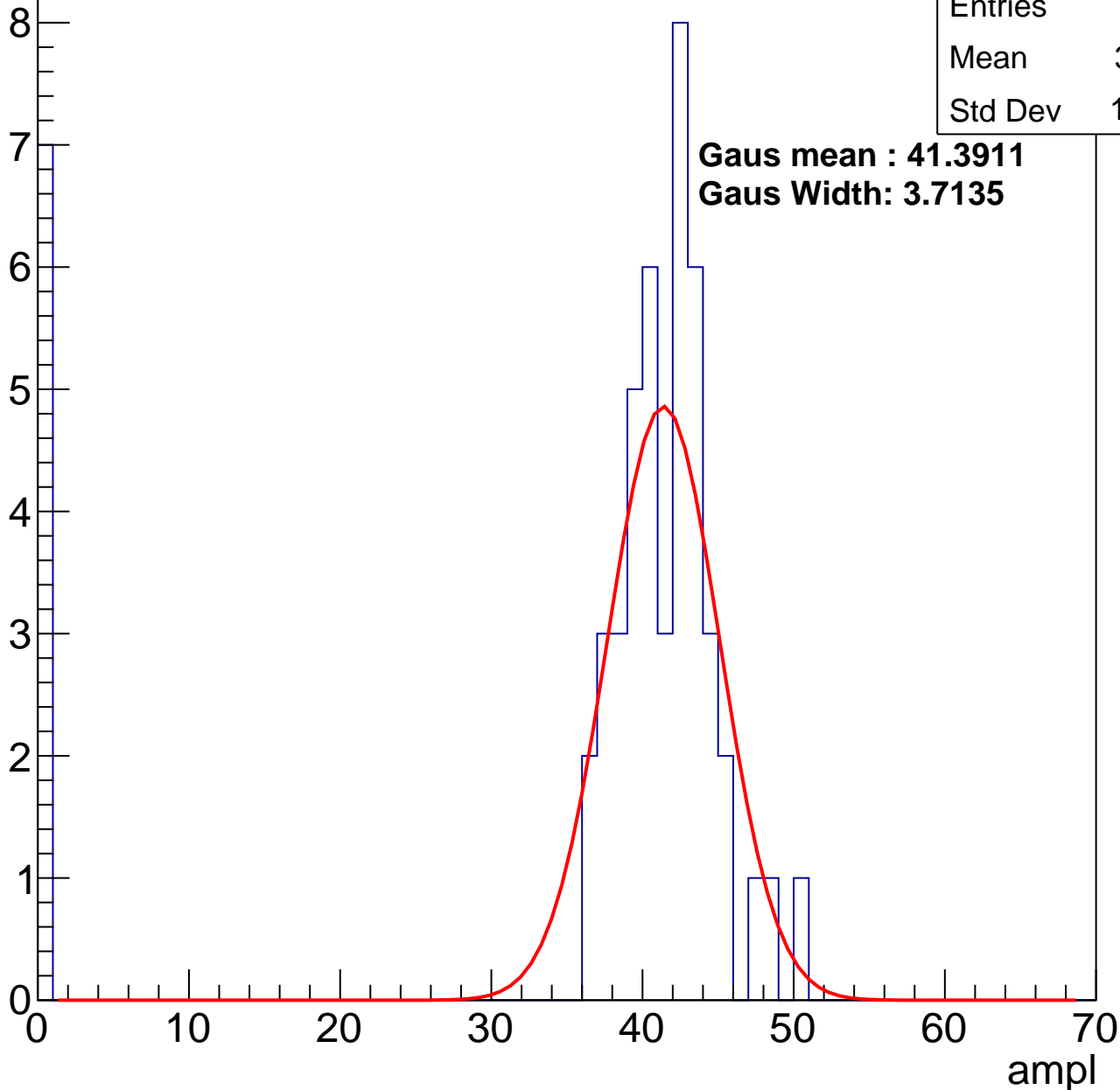
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	51
Mean	35.61
Std Dev	14.48

**Gaus mean : 41.3911**

**Gaus Width: 3.7135**



# B1L103S, U3-ch57, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

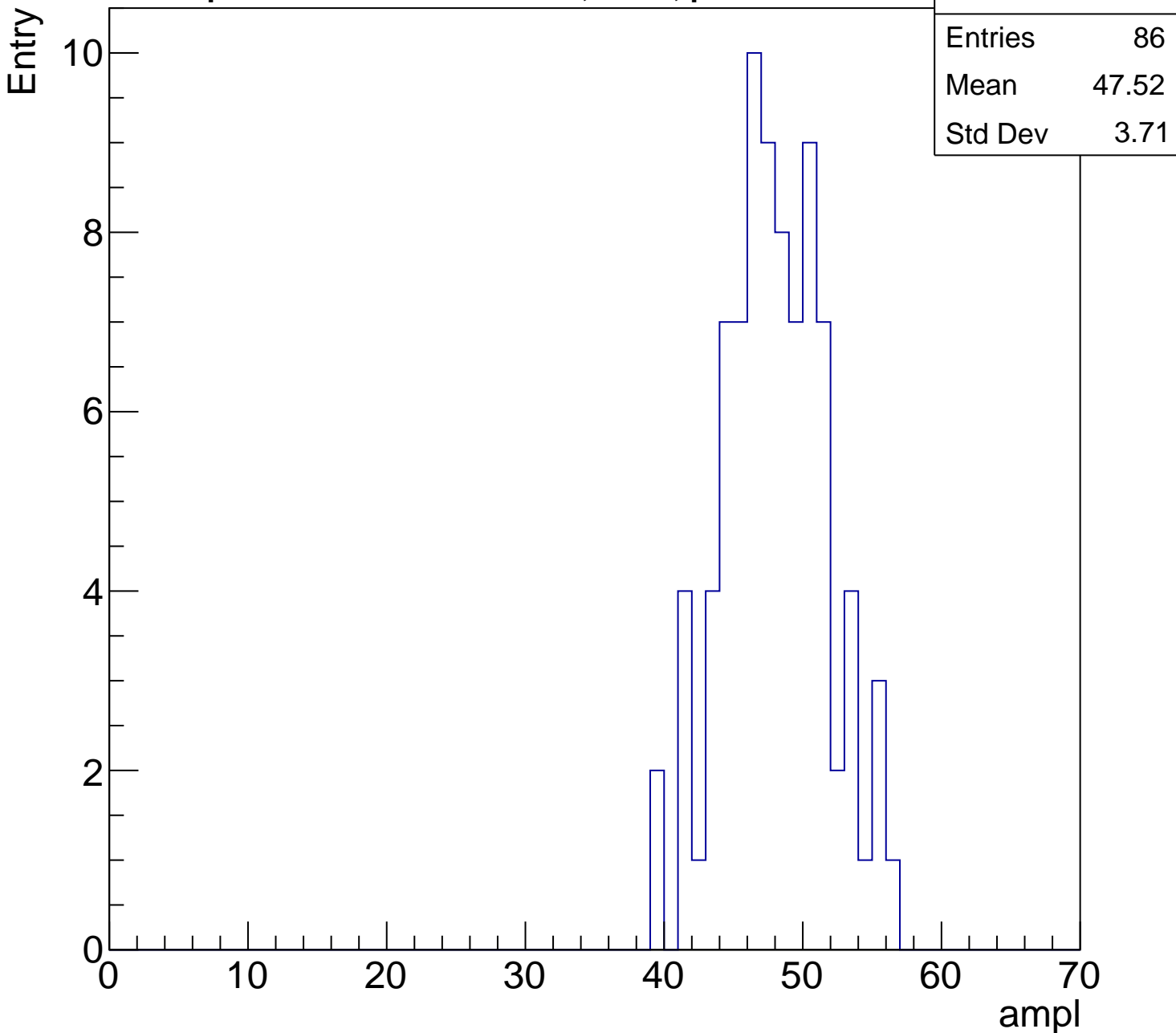
Entries	86
Mean	47.52
Std Dev	3.71

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

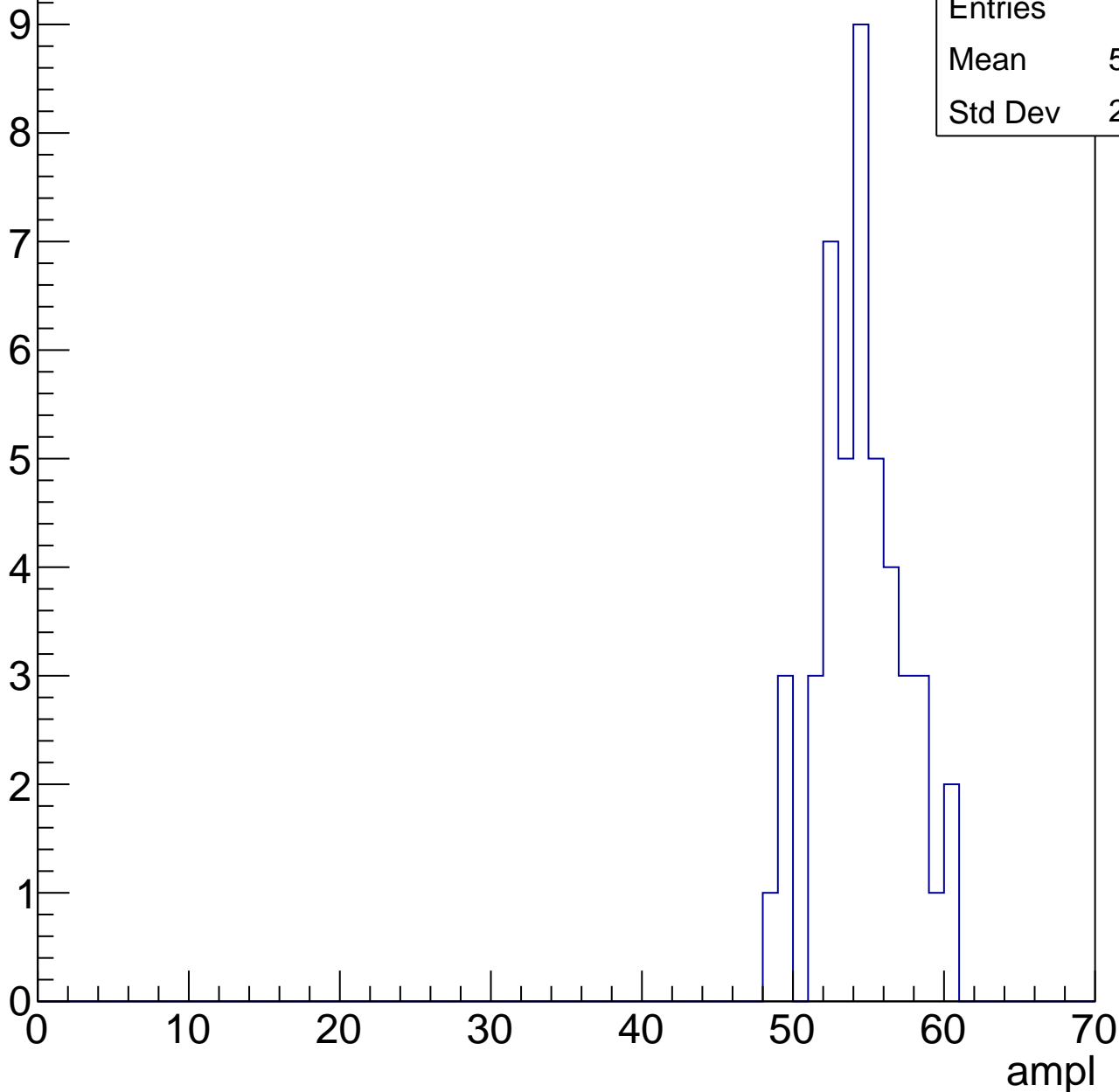


# B1L103S, U3-ch57, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	46
Mean	54.04
Std Dev	2.813

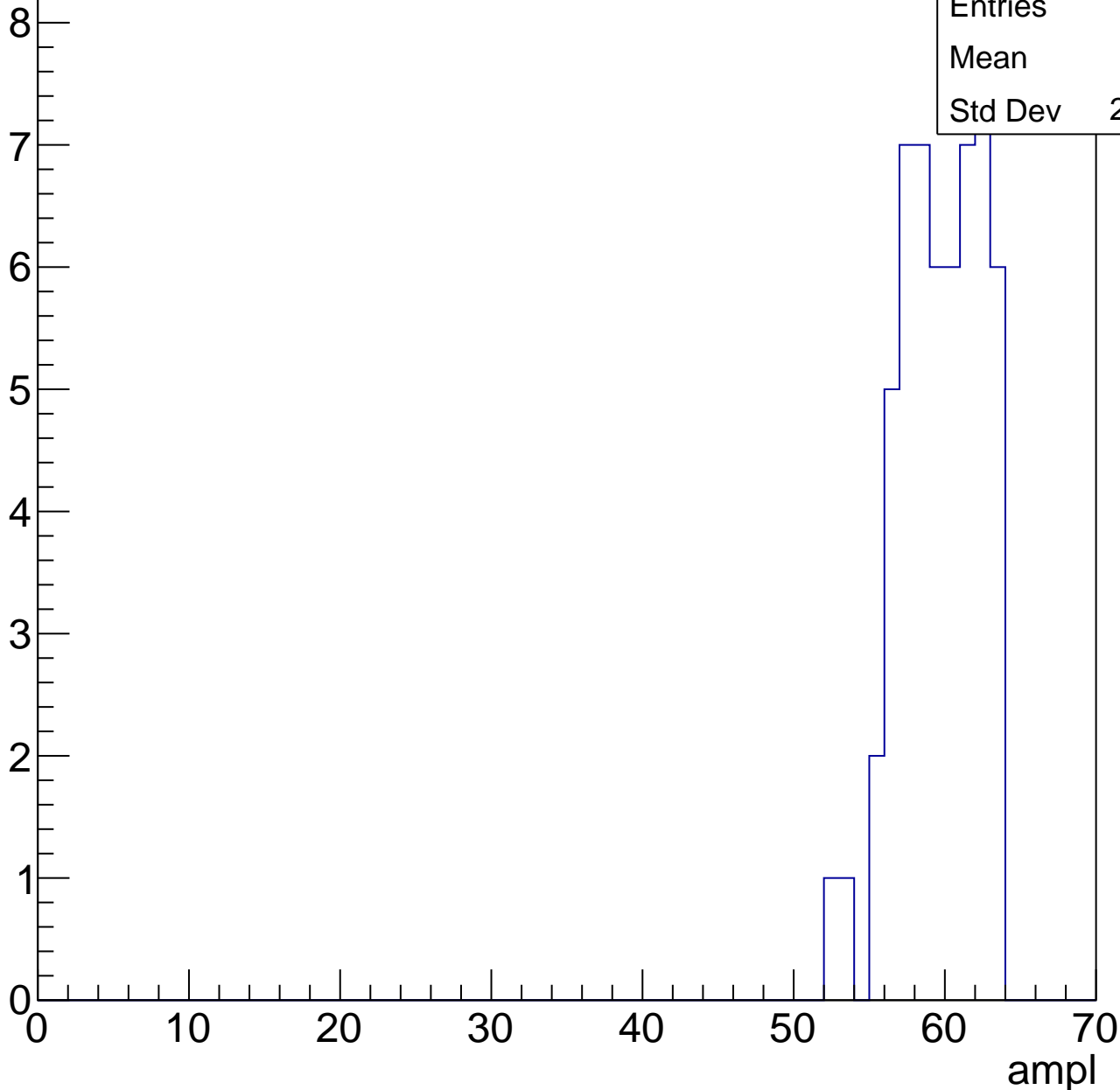


# B1L103S, U3-ch57, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

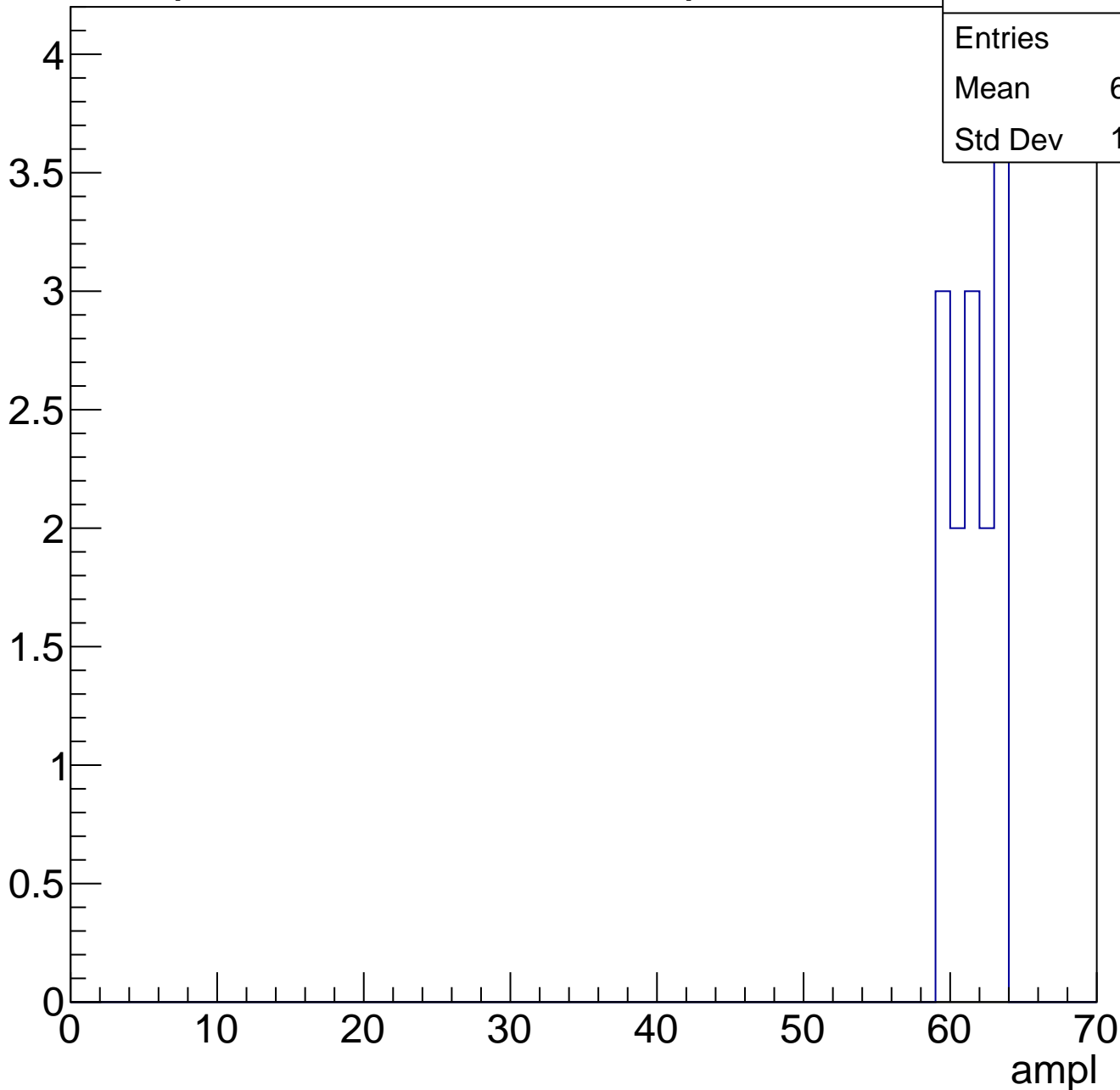
Entries	56
Mean	59.2
Std Dev	2.662



# B1L103S, U3-ch57, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U3-ch57, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	20
Mean	0
Std Dev	0

ampl

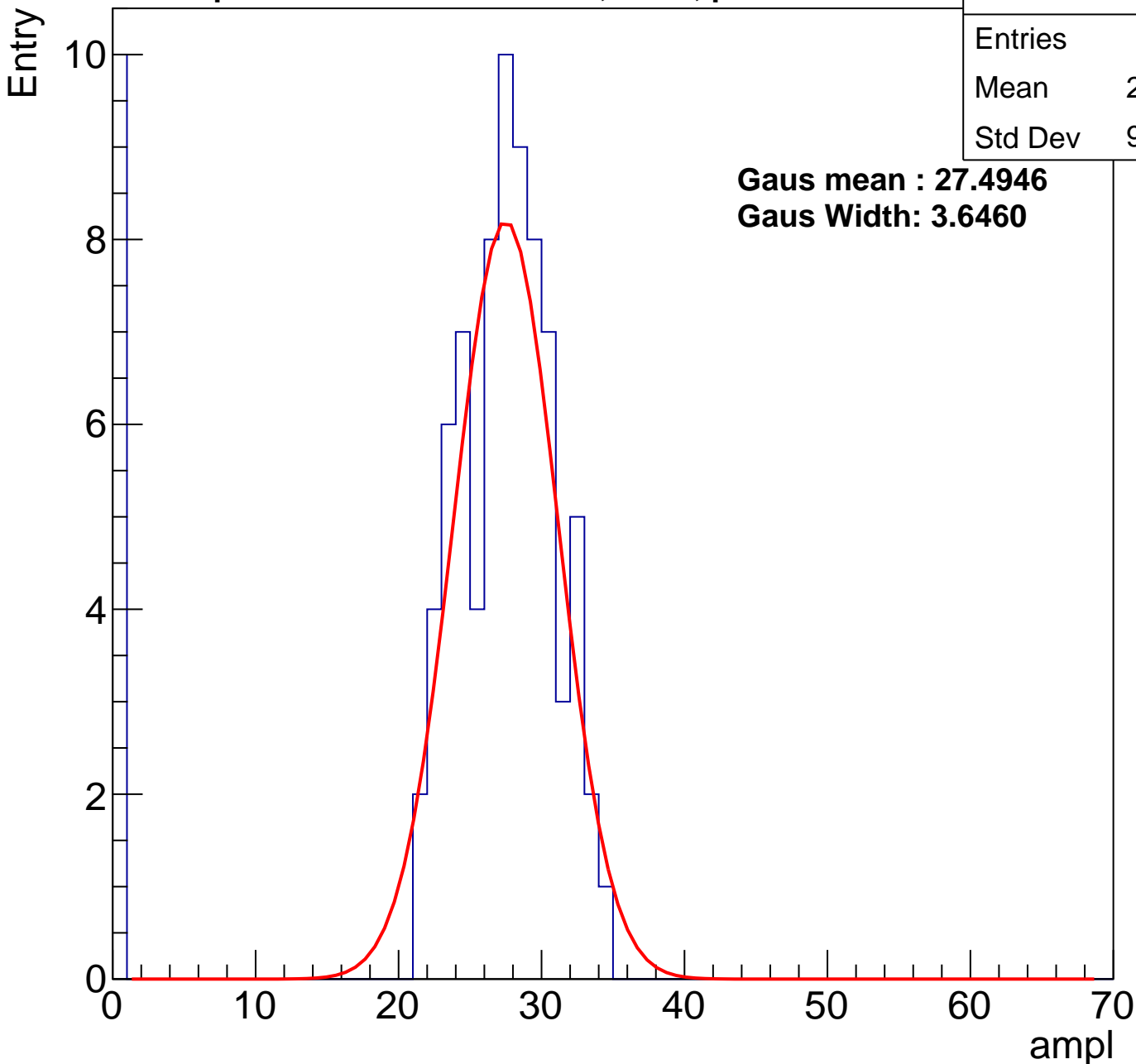
# B1L103S, U3-ch58, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	86
Mean	23.97
Std Dev	9.182

**Gaus mean : 27.4946**

**Gaus Width: 3.6460**



# B1L103S, U3-ch58, adc1

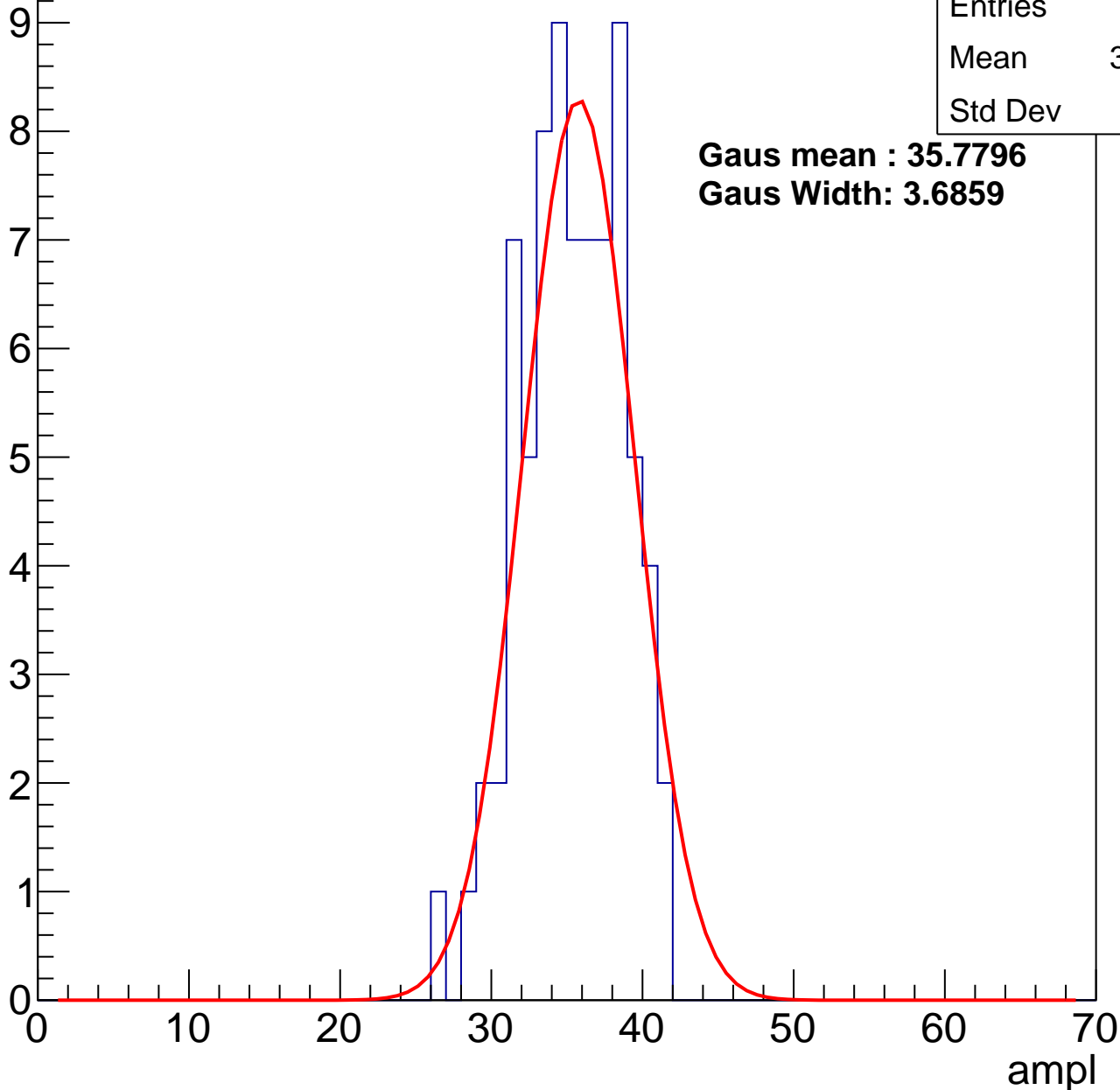
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	76
Mean	34.92
Std Dev	3.28

**Gaus mean : 35.7796**

**Gaus Width: 3.6859**



# B1L103S, U3-ch58, adc2

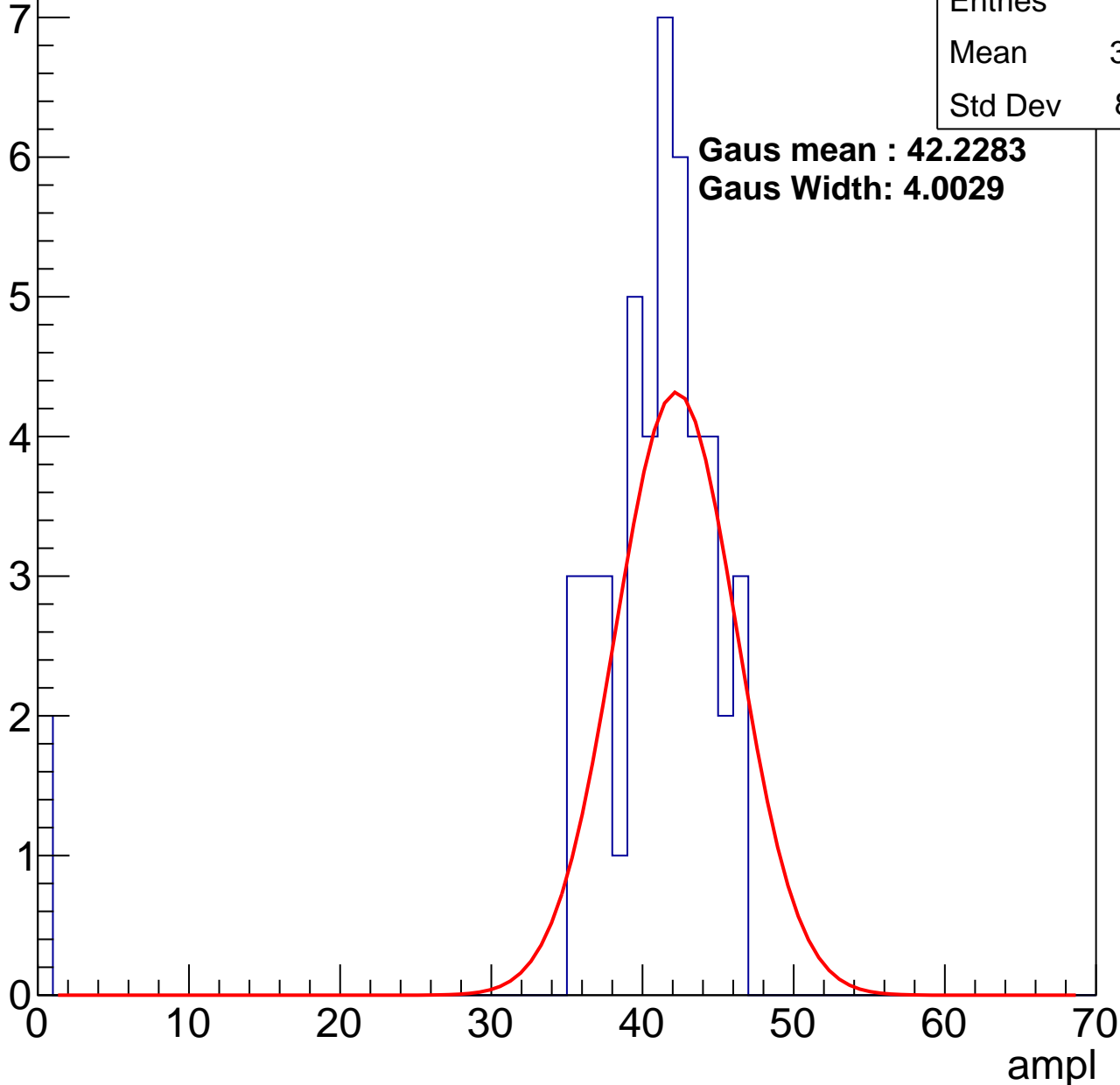
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	47
Mean	38.98
Std Dev	8.751

**Gaus mean : 42.2283**

**Gaus Width: 4.0029**

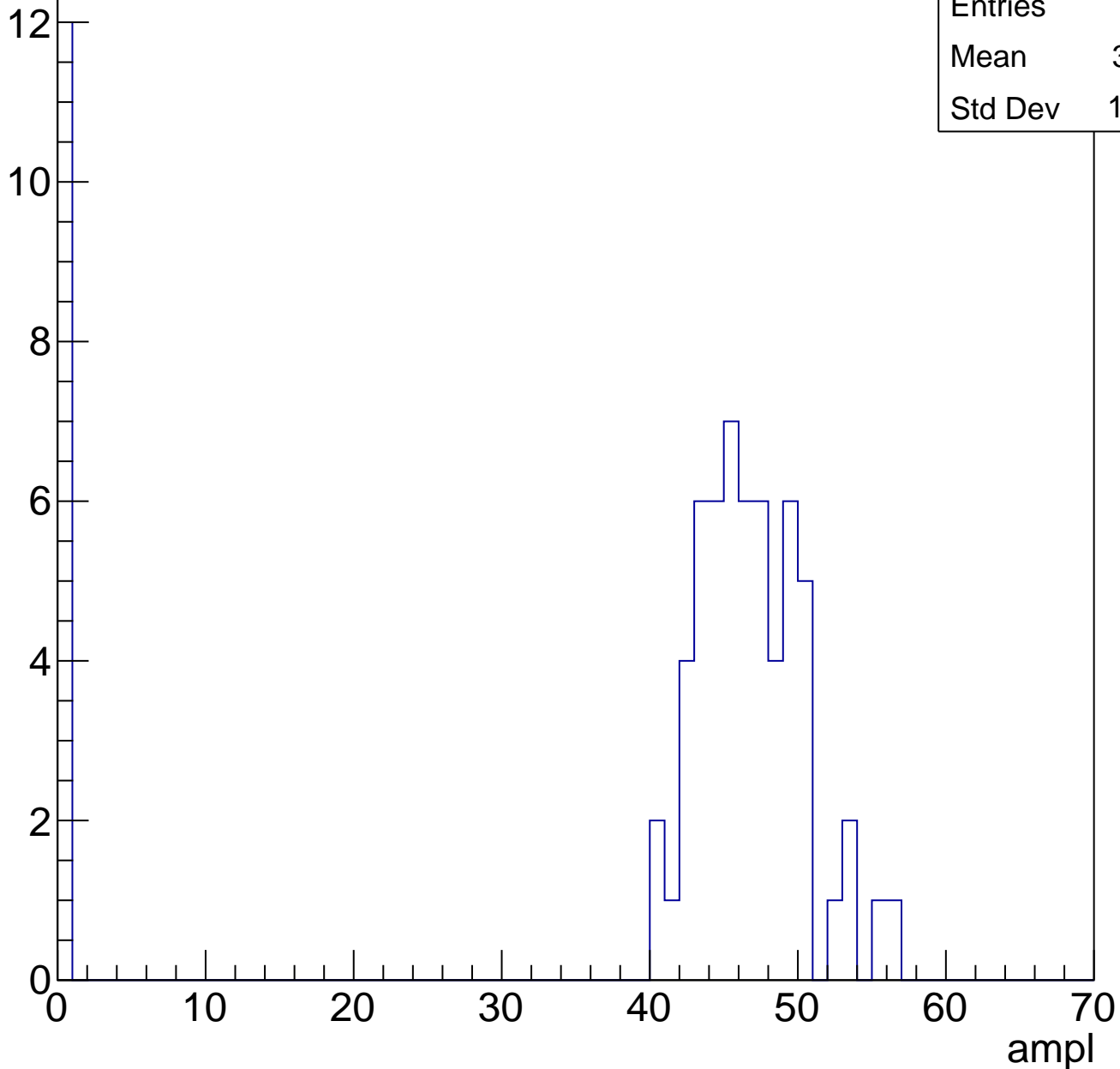


# B1L103S, U3-ch58, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	70
Mean	38.41
Std Dev	17.76

Entry



# B1L103S, U3-ch58, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

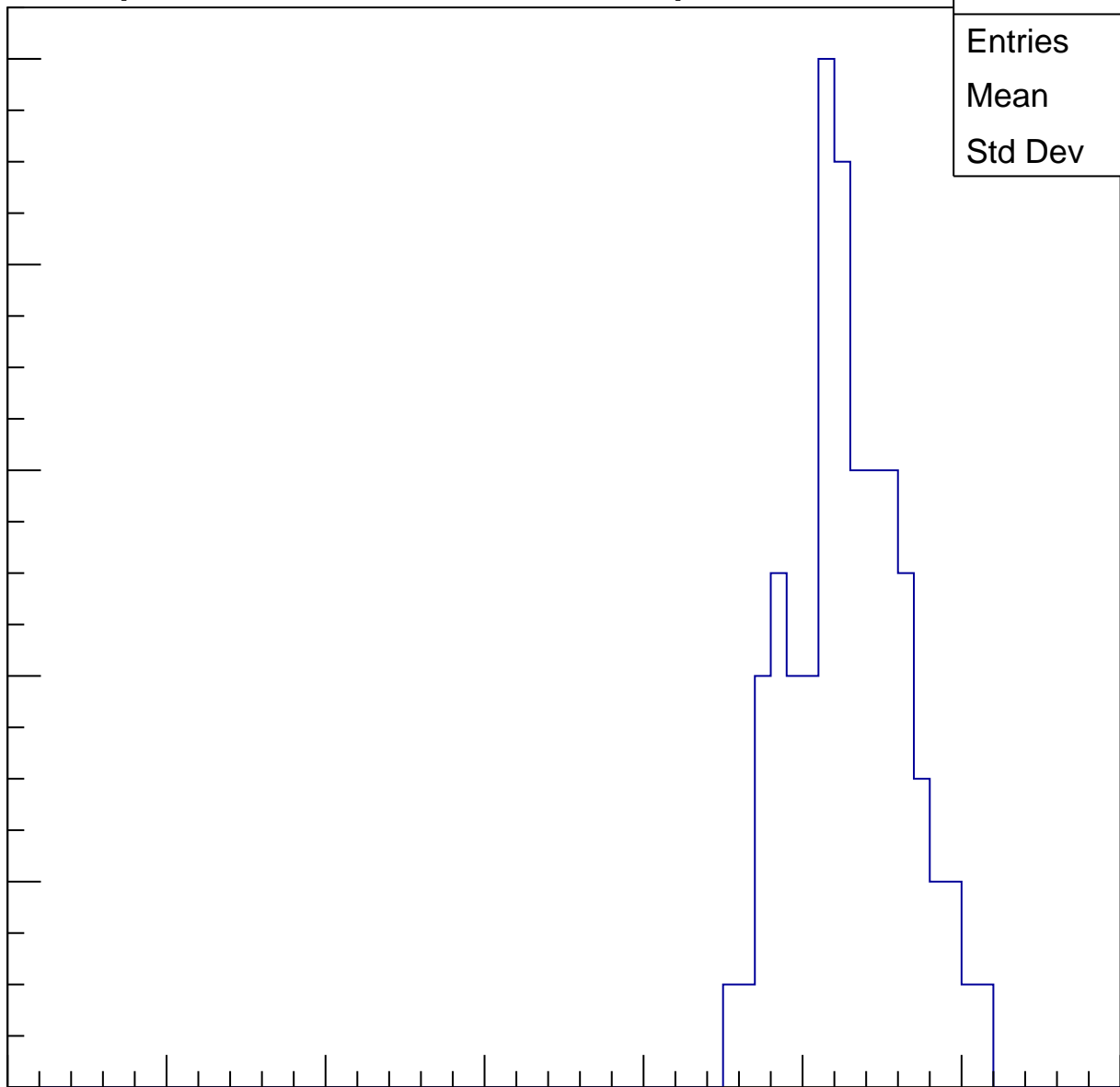
Entries	70
Mean	52.44
Std Dev	3.52

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

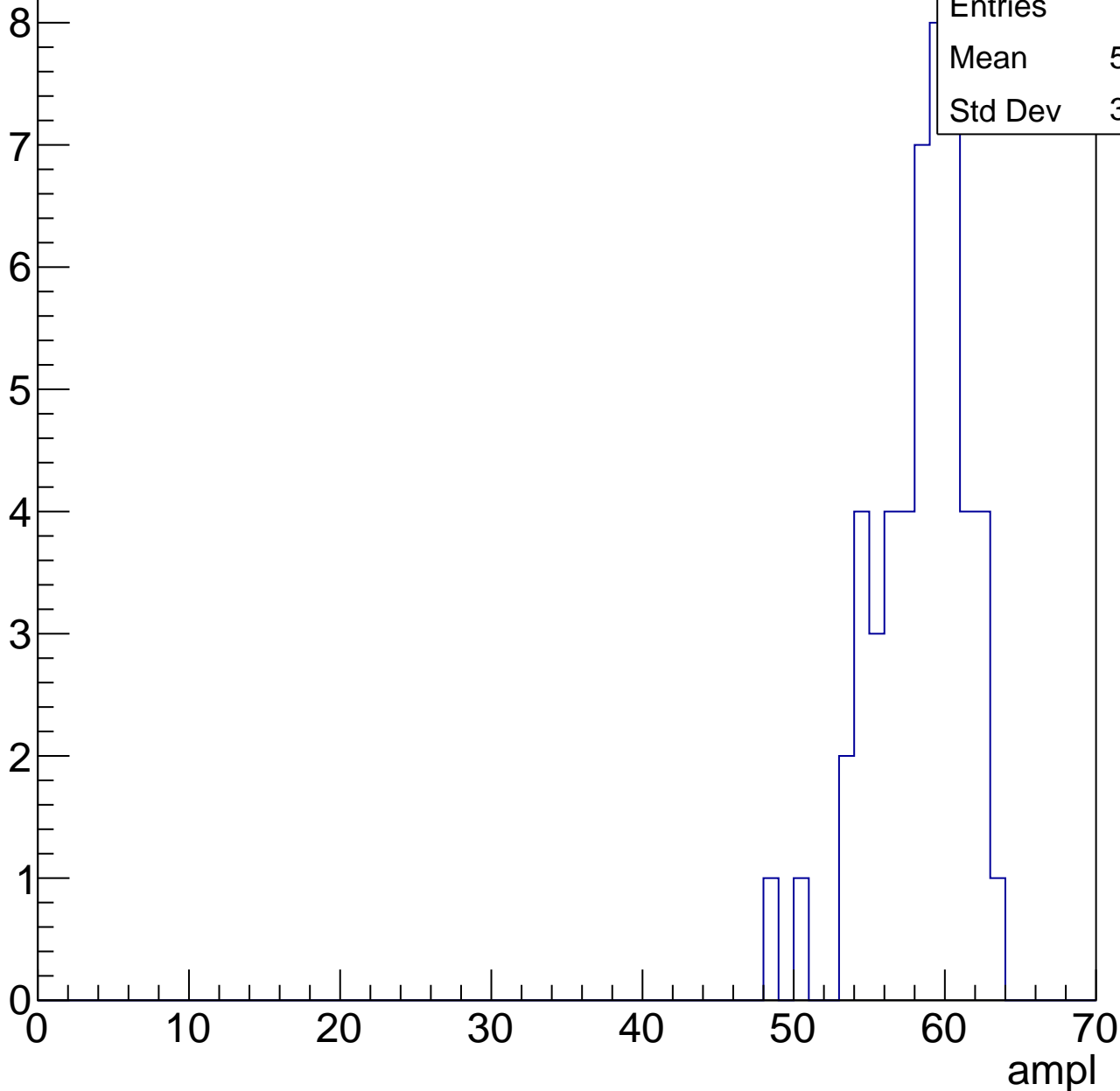


# B1L103S, U3-ch58, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	51
Mean	57.84
Std Dev	3.096

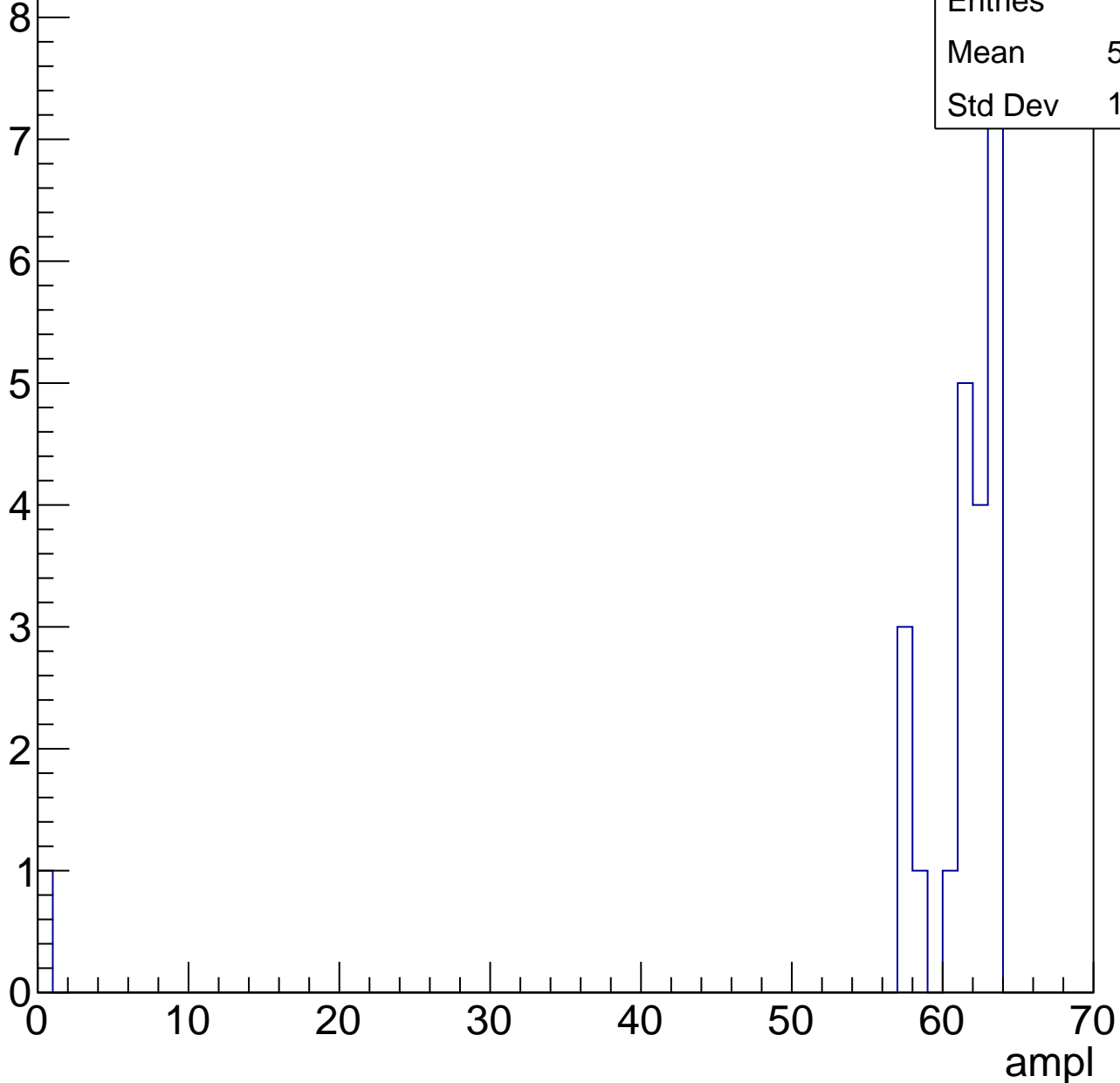


# B1L103S, U3-ch58, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	23
Mean	58.52
Std Dev	12.64



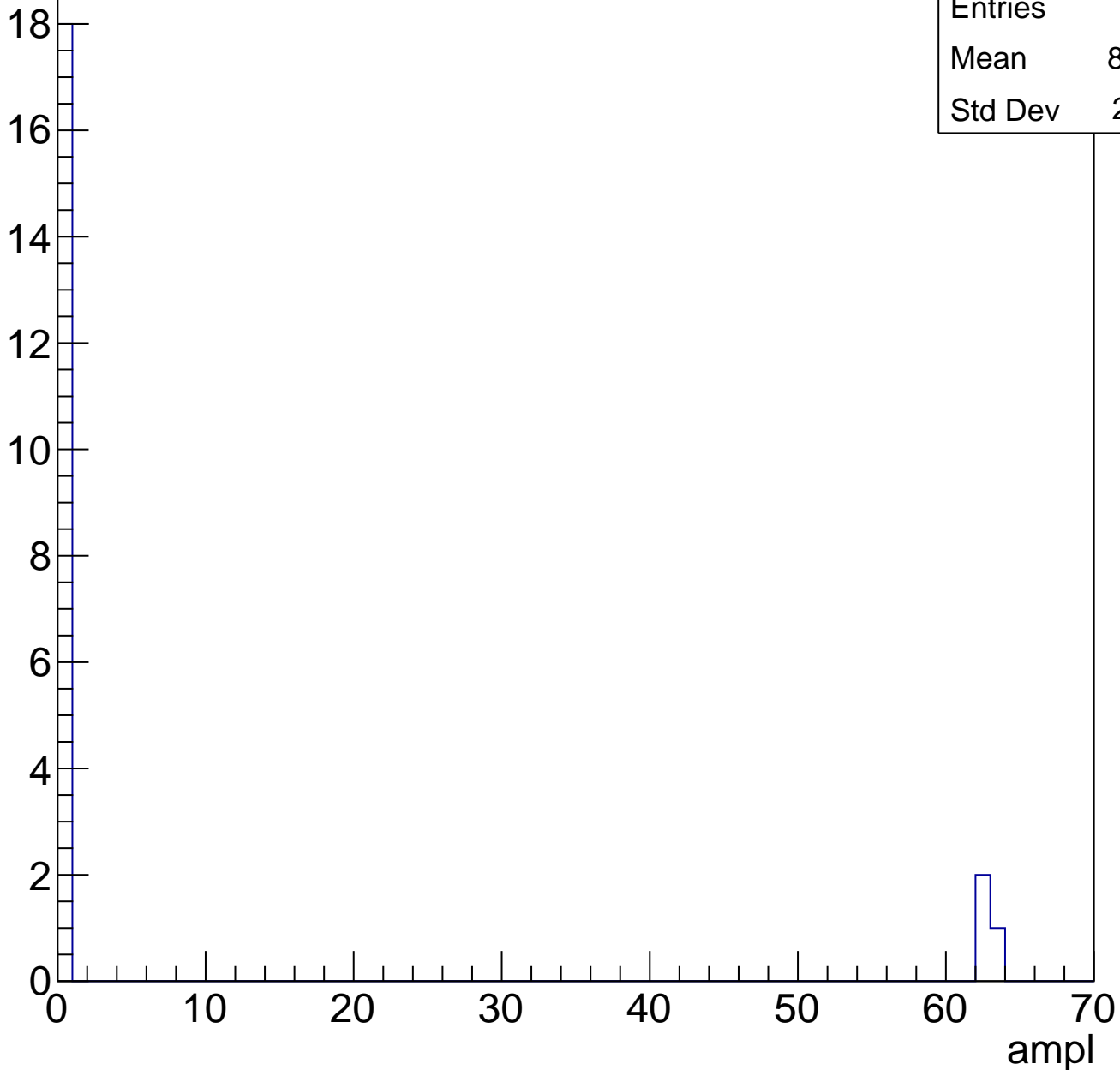


# B1L103S, U3-ch58, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	8.905
Std Dev	21.81

Entry



# B1L103S, U3-ch59, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	74
Mean	22.77
Std Dev	11.78

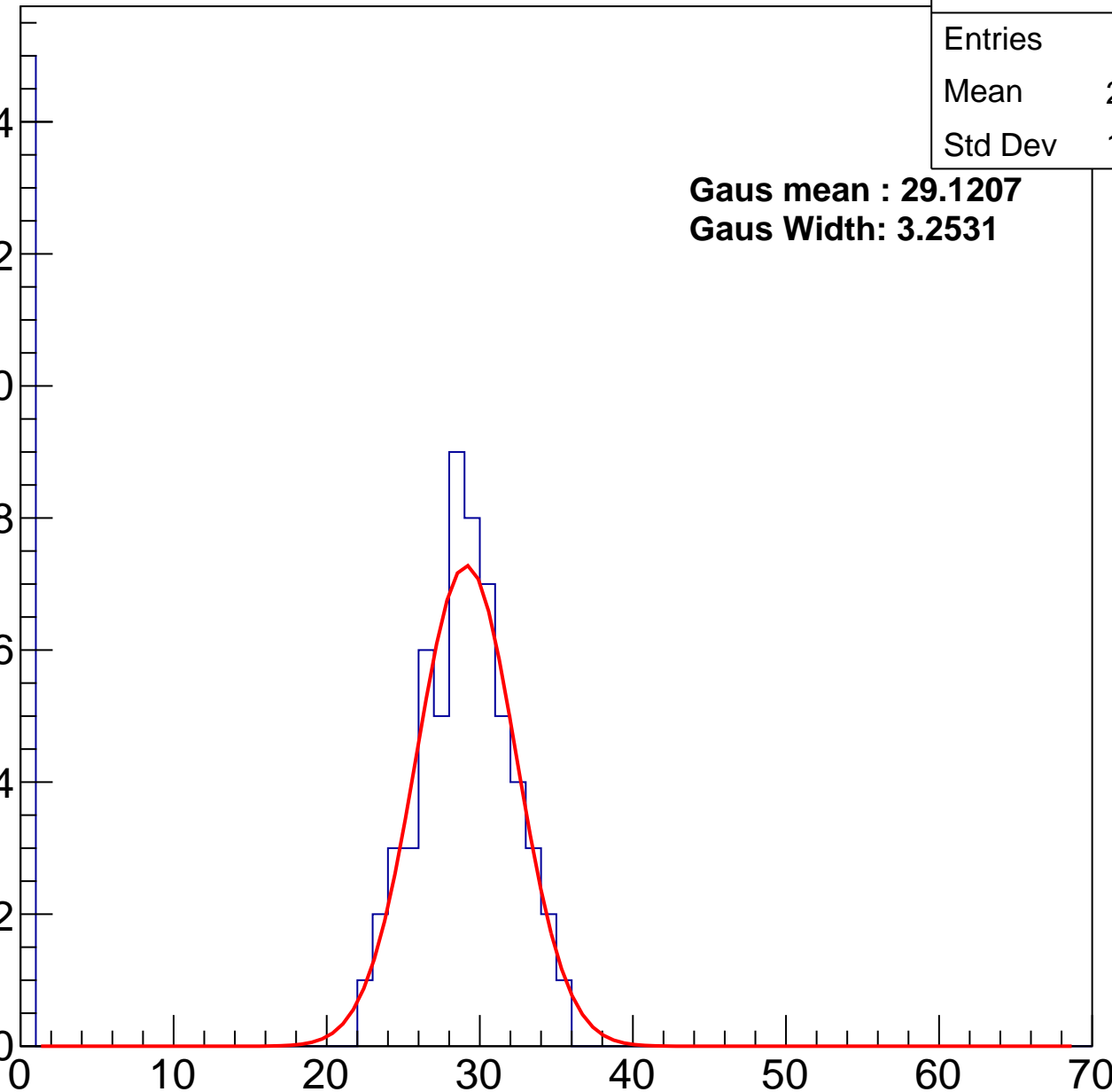
**Gaus mean : 29.1207**

**Gaus Width: 3.2531**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U3-ch59, adc1

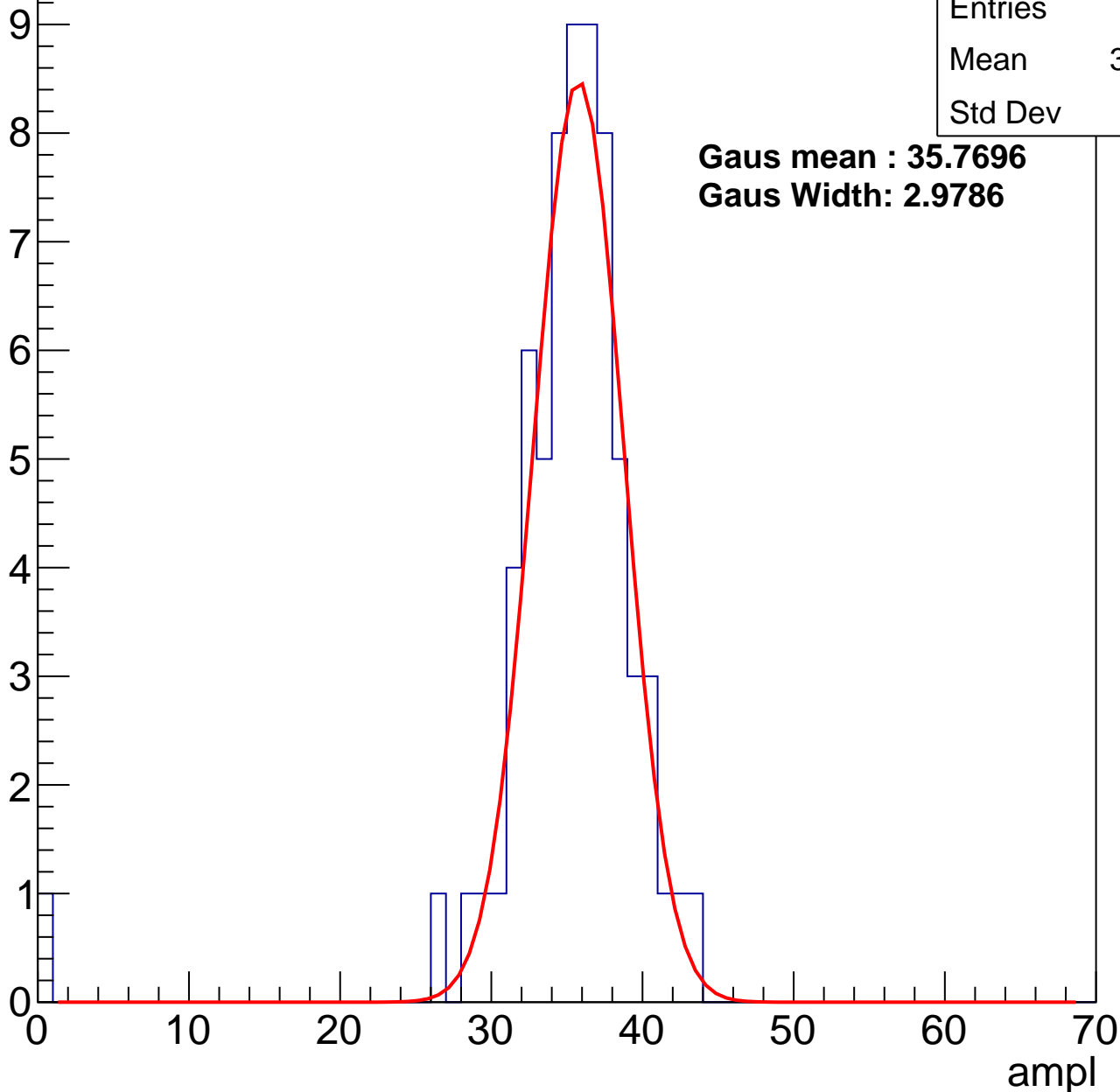
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	34.62
Std Dev	5.3

**Gaus mean : 35.7696**

**Gaus Width: 2.9786**



# B1L103S, U3-ch59, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	68
Mean	34.57
Std Dev	15.43

**Gaus mean : 42.0580**

**Gaus Width: 2.9741**

Entry

10

8

6

4

2

0

0

10

20

30

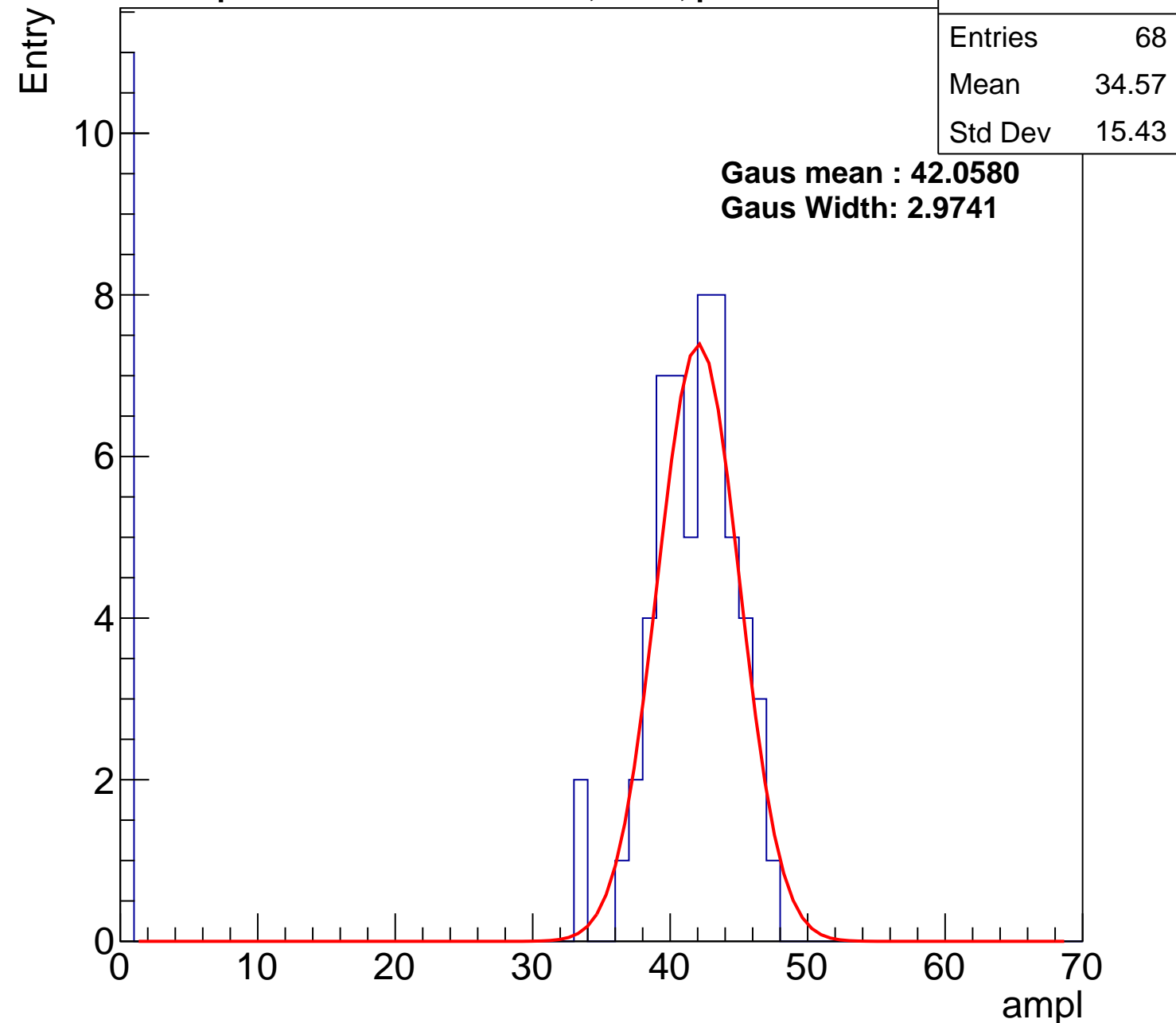
40

50

60

70

ampl

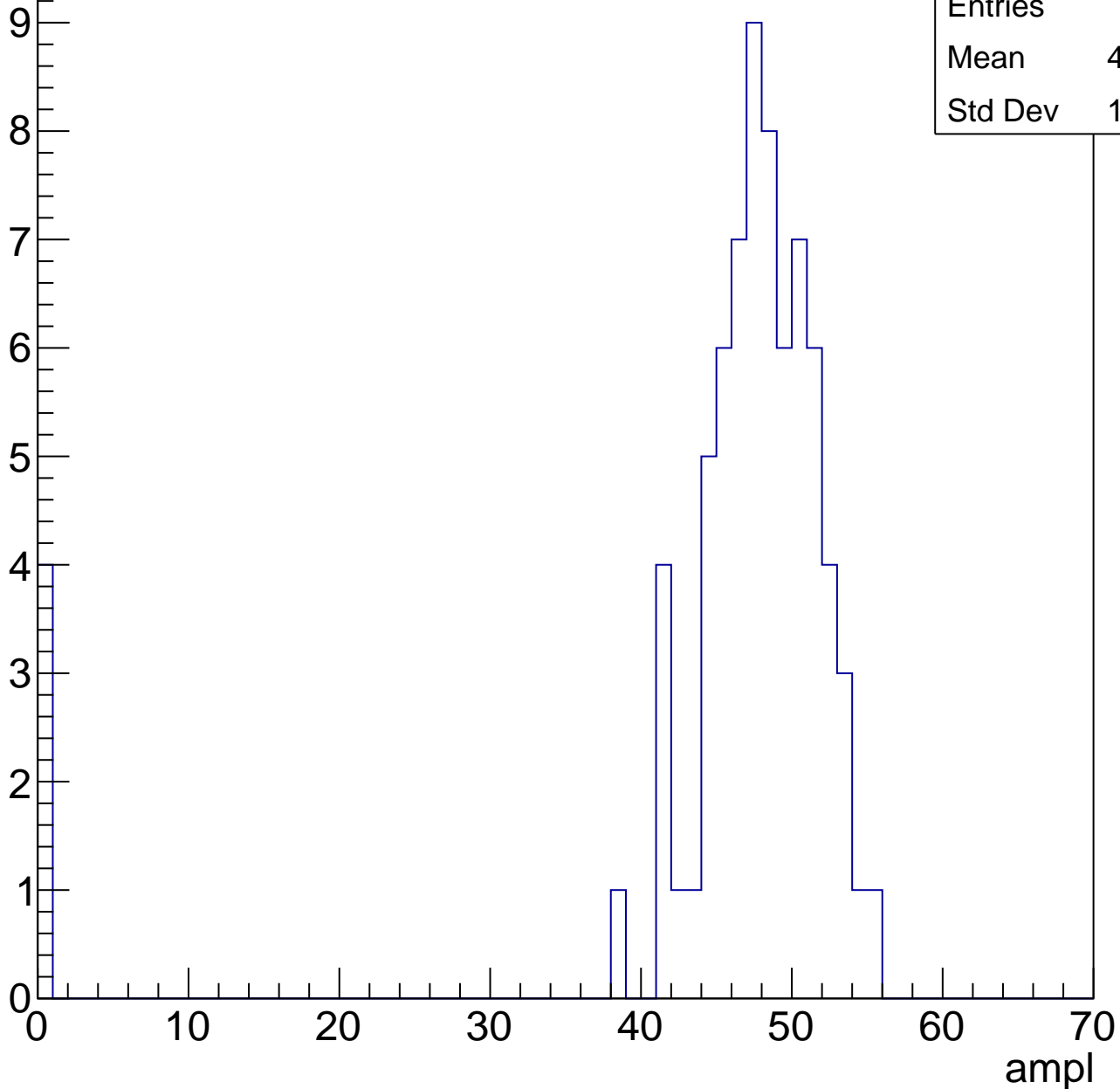


# B1L103S, U3-ch59, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	74
Mean	45.03
Std Dev	11.27

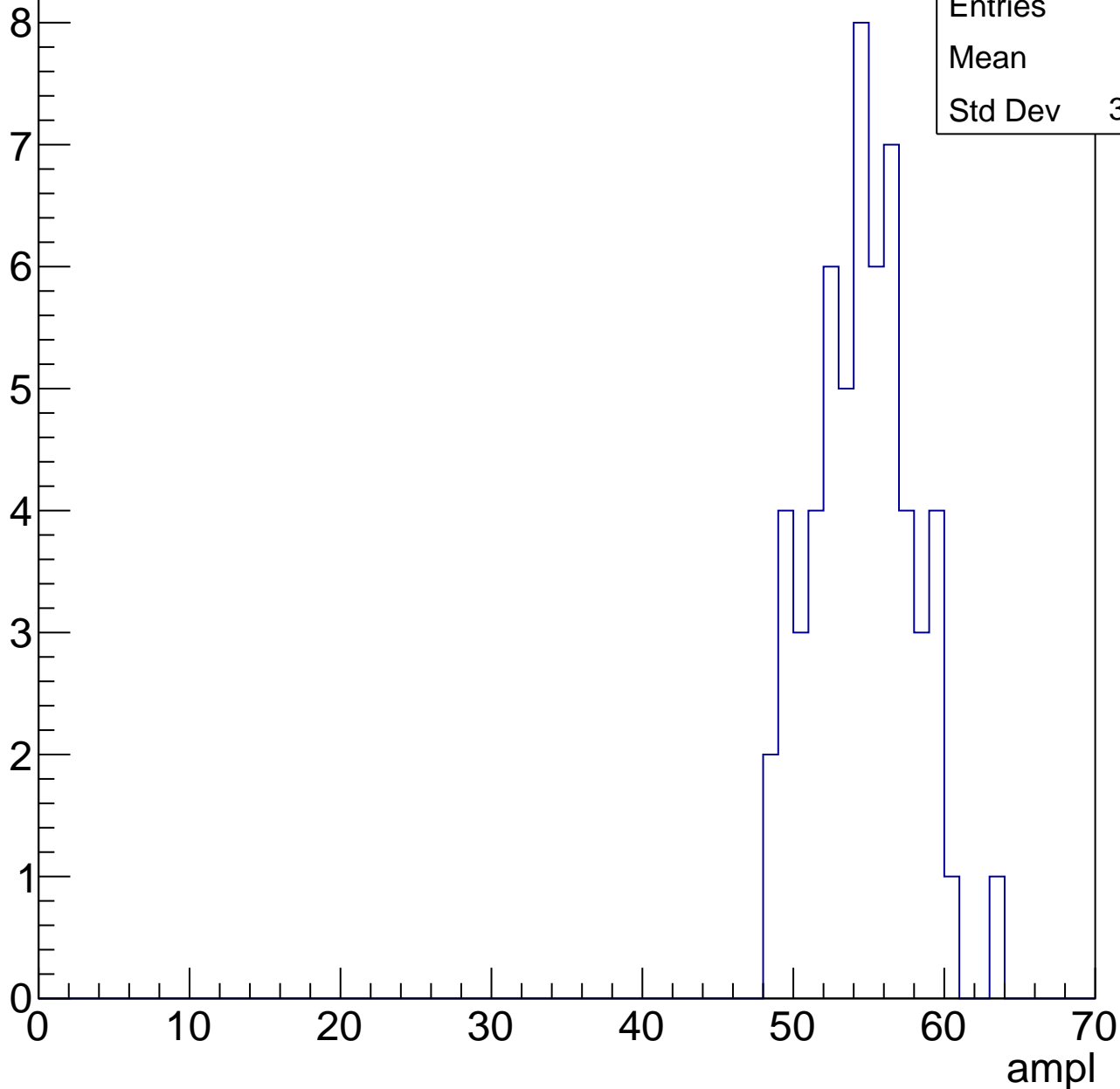


# B1L103S, U3-ch59, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	54.1
Std Dev	3.268



# B1L103S, U3-ch59, adc5

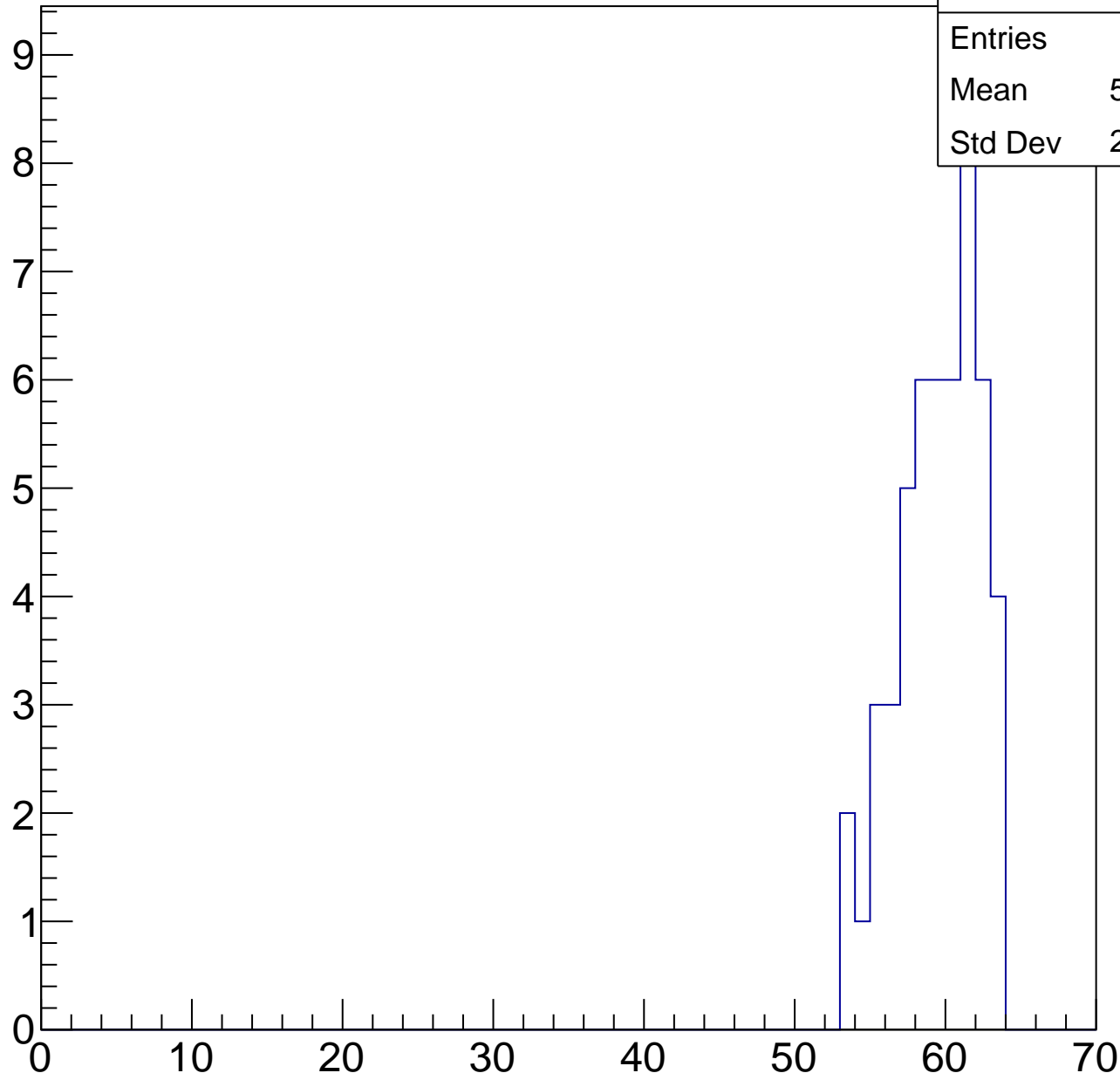
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	59.08
Std Dev	2.648

ampl

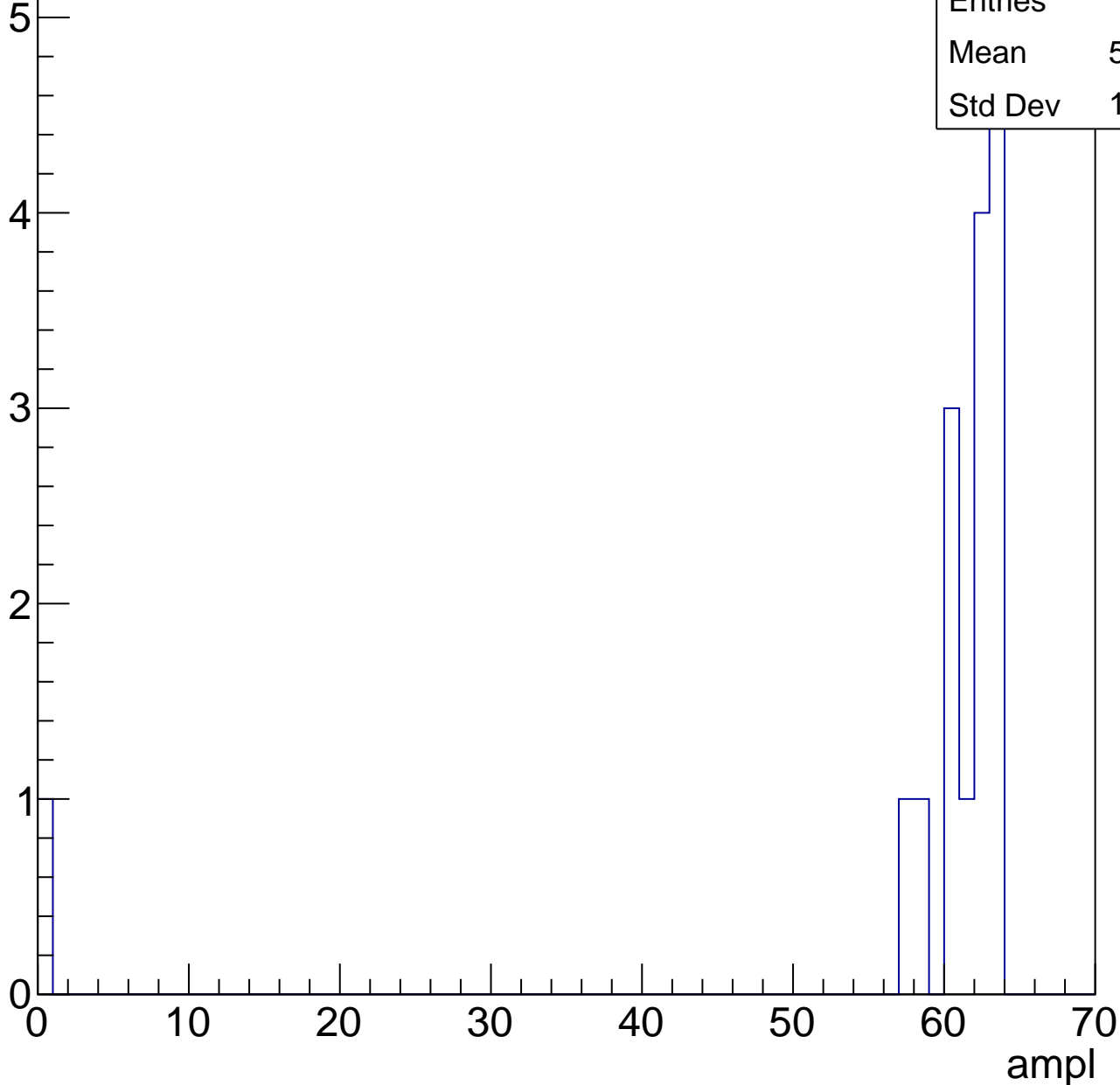


# B1L103S, U3-ch59, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	16
Mean	57.44
Std Dev	14.94





# B1L103S, U3-ch59, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	19
Mean	0
Std Dev	0

ampl

# B1L103S, U3-ch60, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	65
Mean	21.98
Std Dev	10.3

**Gaus mean : 26.8072**

**Gaus Width: 3.9984**

Entry

10

8

6

4

2

0

0

10

20

30

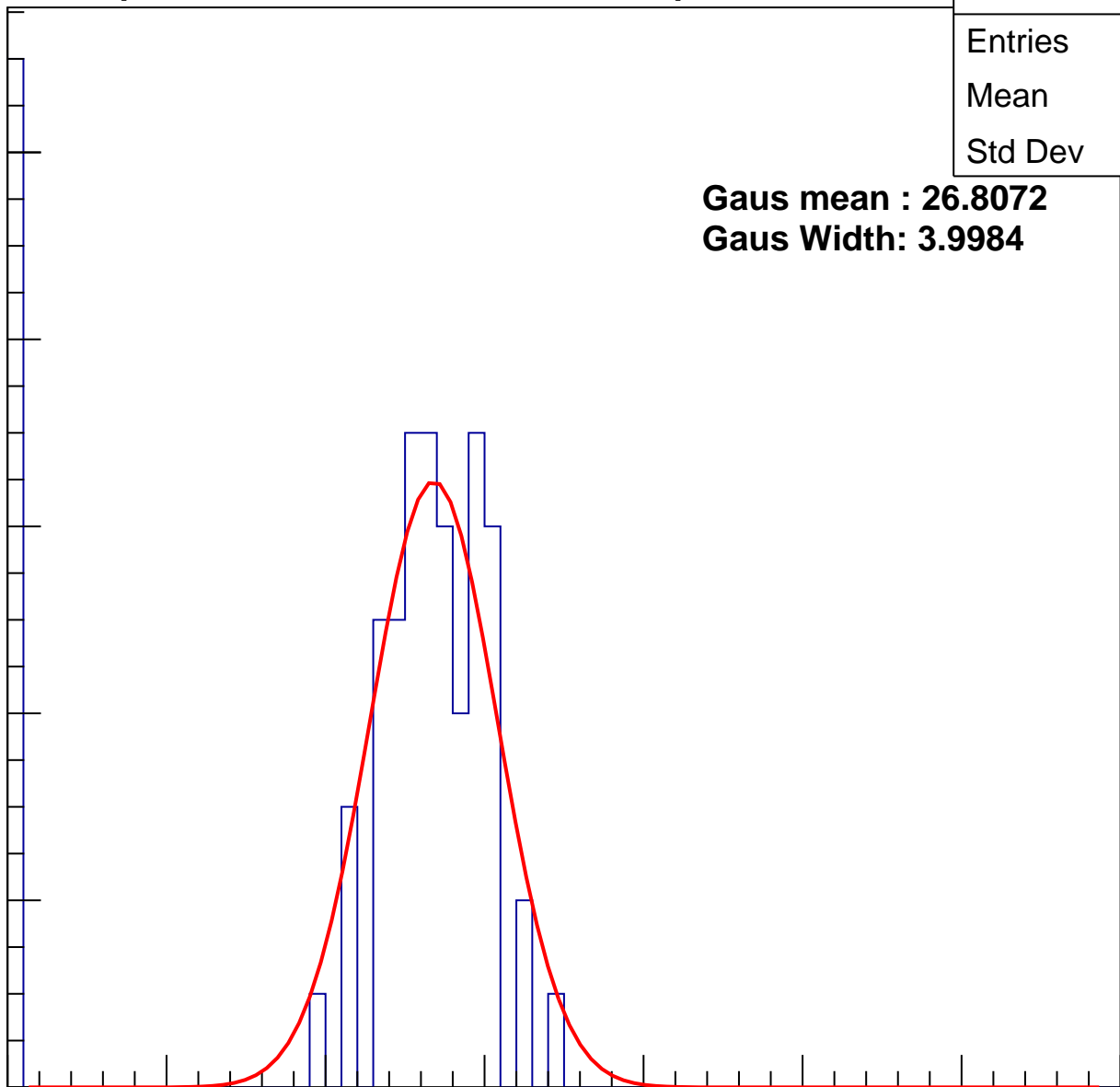
40

50

60

70

ampl



# B1L103S, U3-ch60, adc1

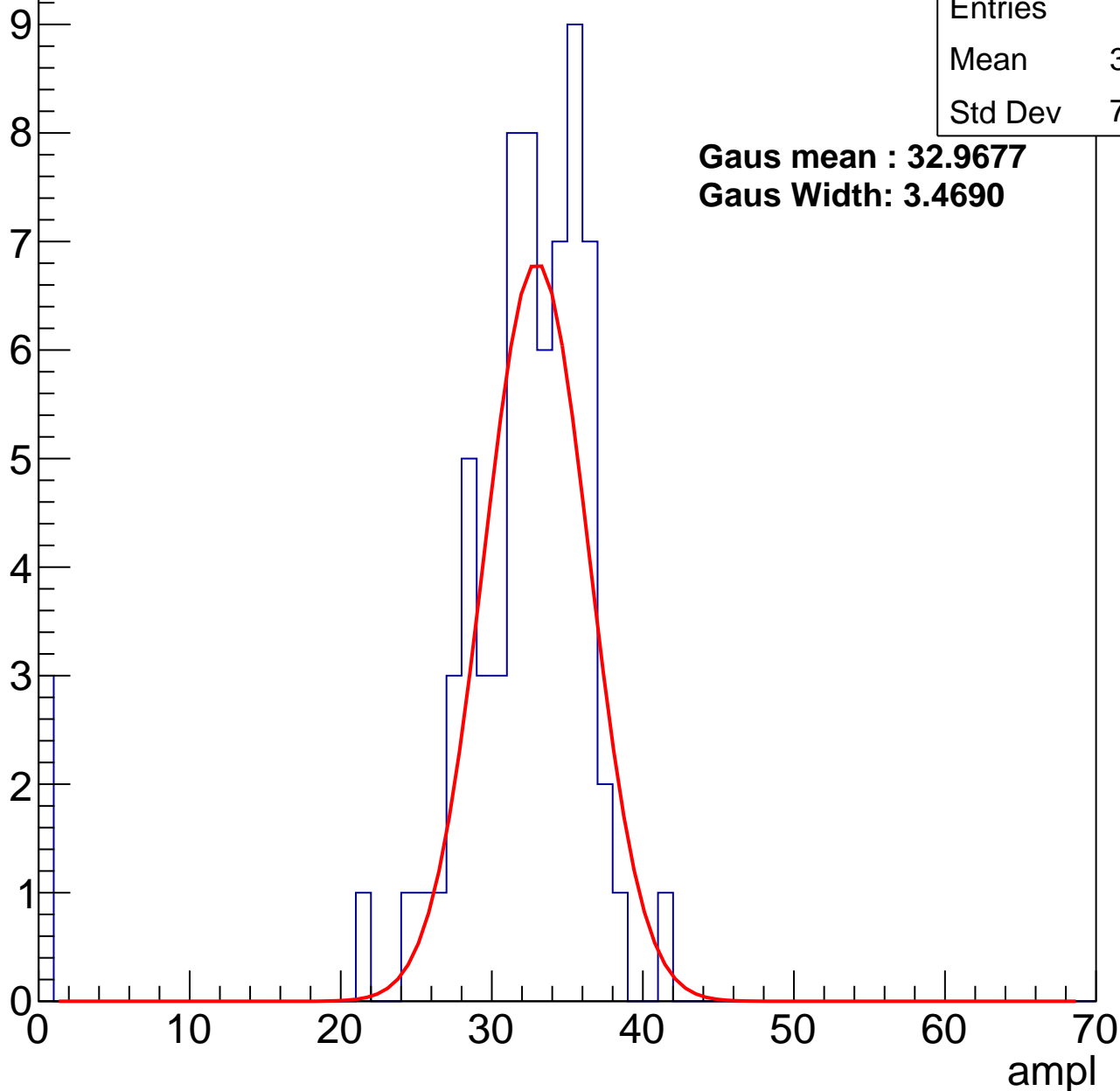
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	30.77
Std Dev	7.399

**Gaus mean : 32.9677**

**Gaus Width: 3.4690**



# B1L103S, U3-ch60, adc2

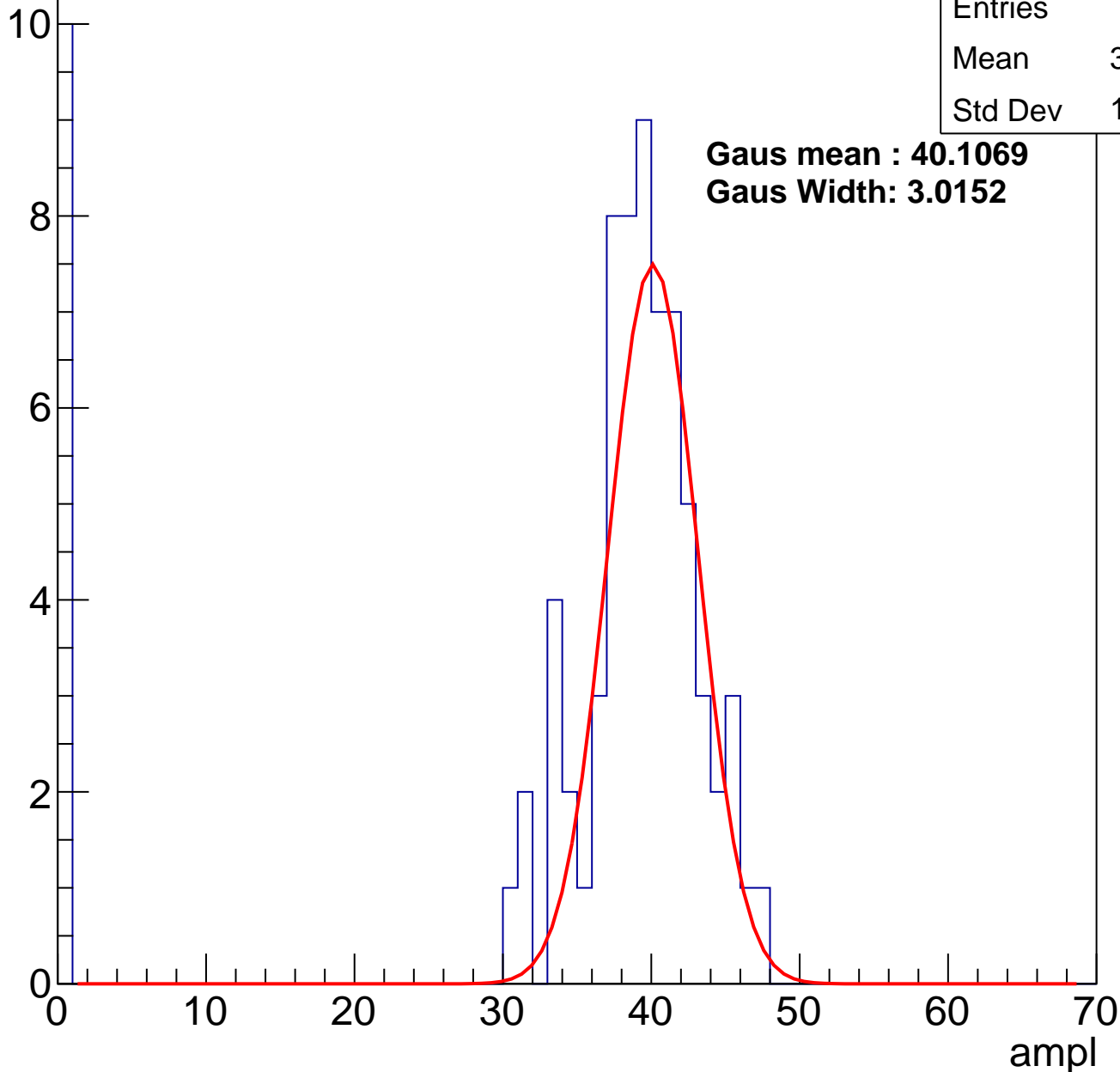
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	77
Mean	33.87
Std Dev	13.52

**Gaus mean : 40.1069**

**Gaus Width: 3.0152**

Entry

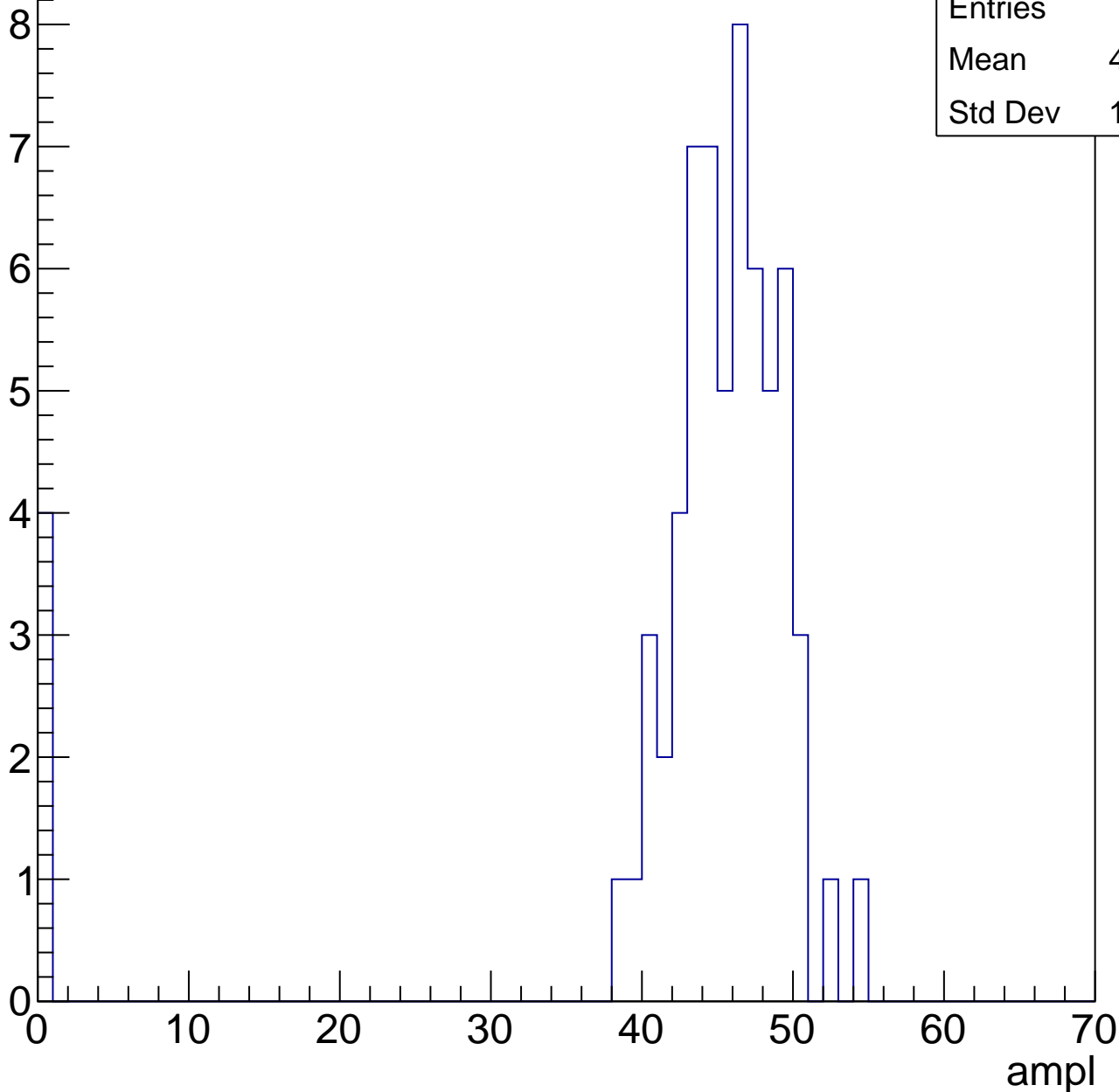


# B1L103S, U3-ch60, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	42.52
Std Dev	11.42

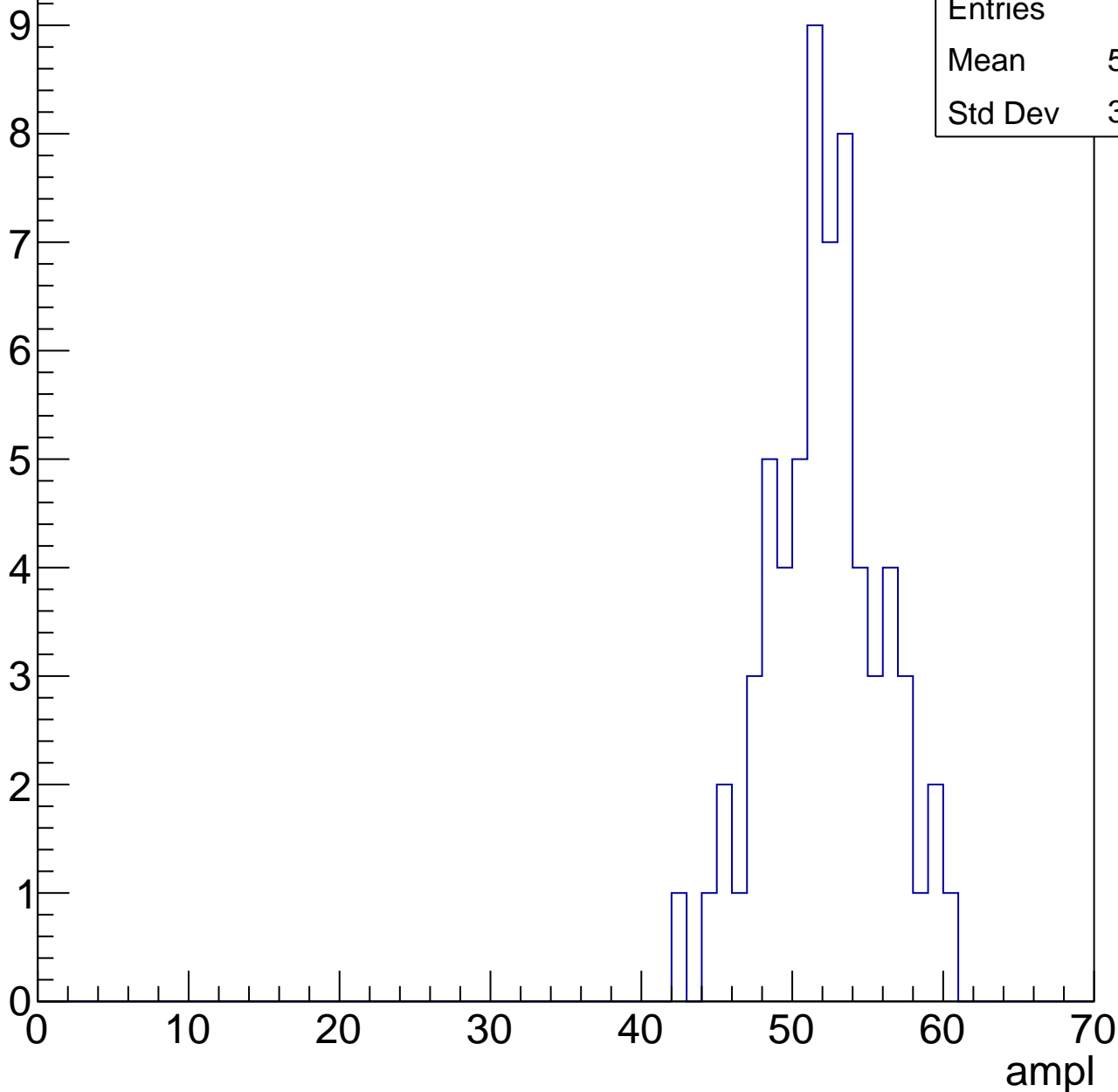


# B1L103S, U3-ch60, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	51.69
Std Dev	3.749



# B1L103S, U3-ch60, adc5

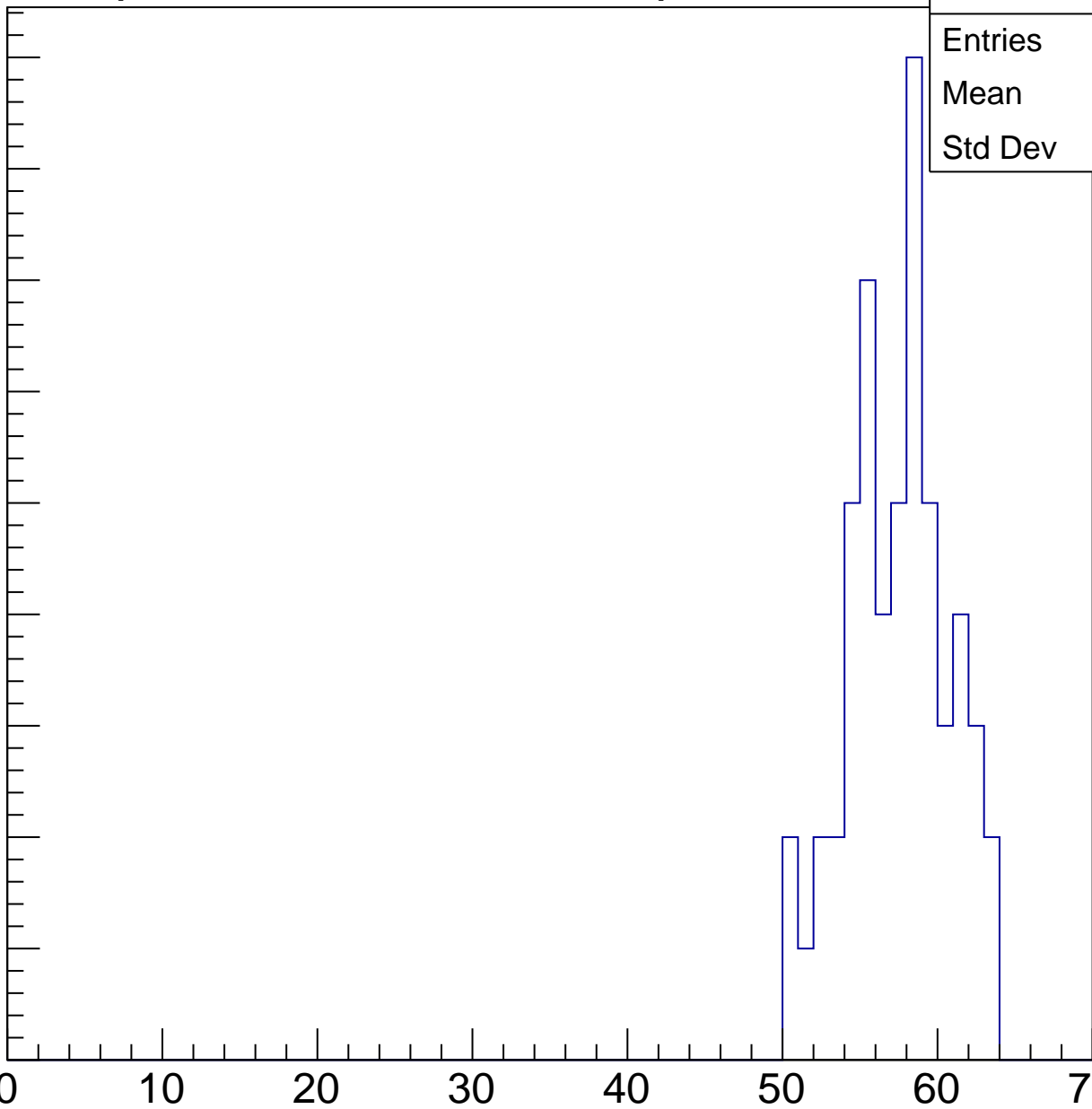
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	54
Mean	57
Std Dev	3.22

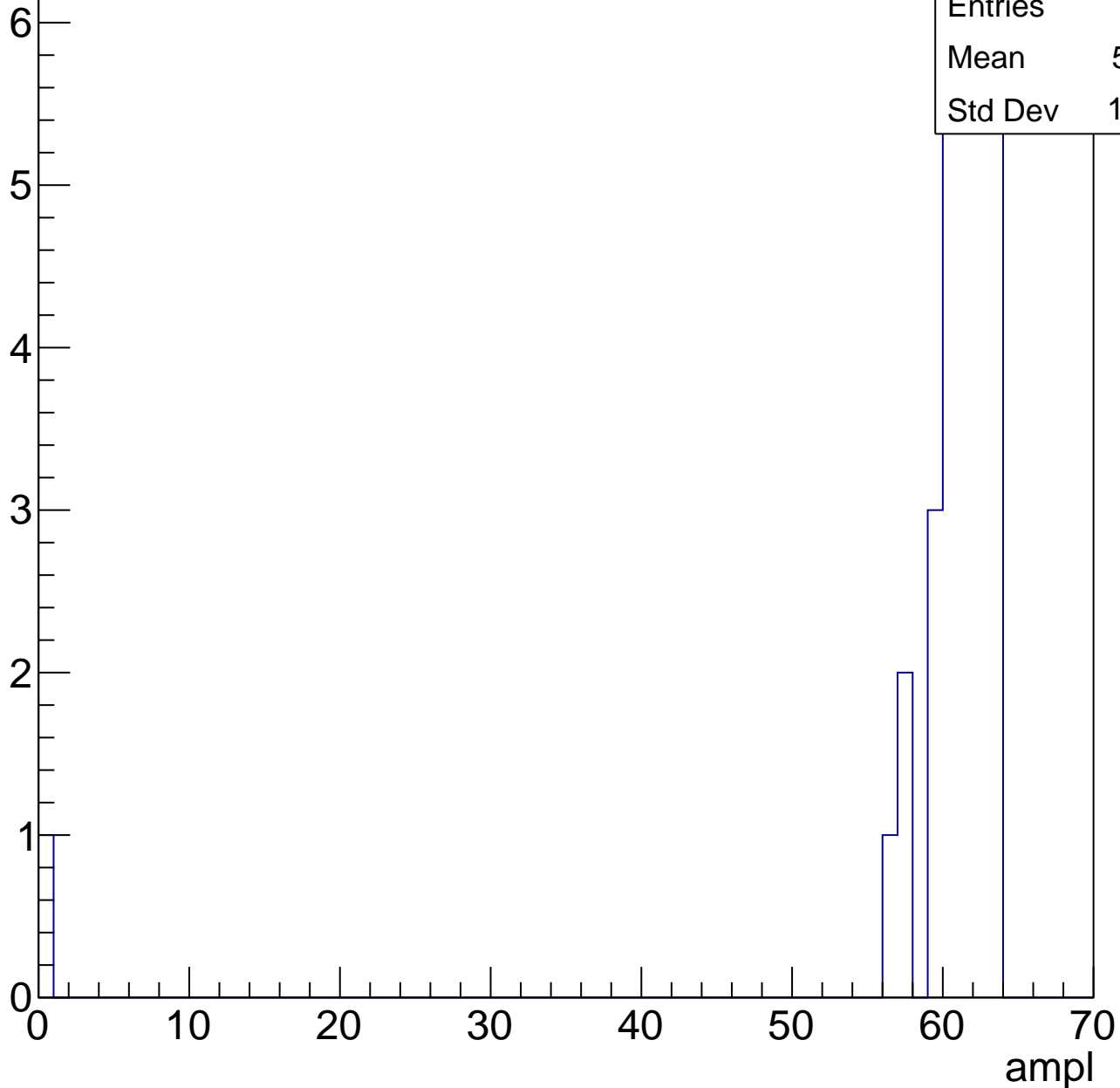
ampl



# B1L103S, U3-ch60, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



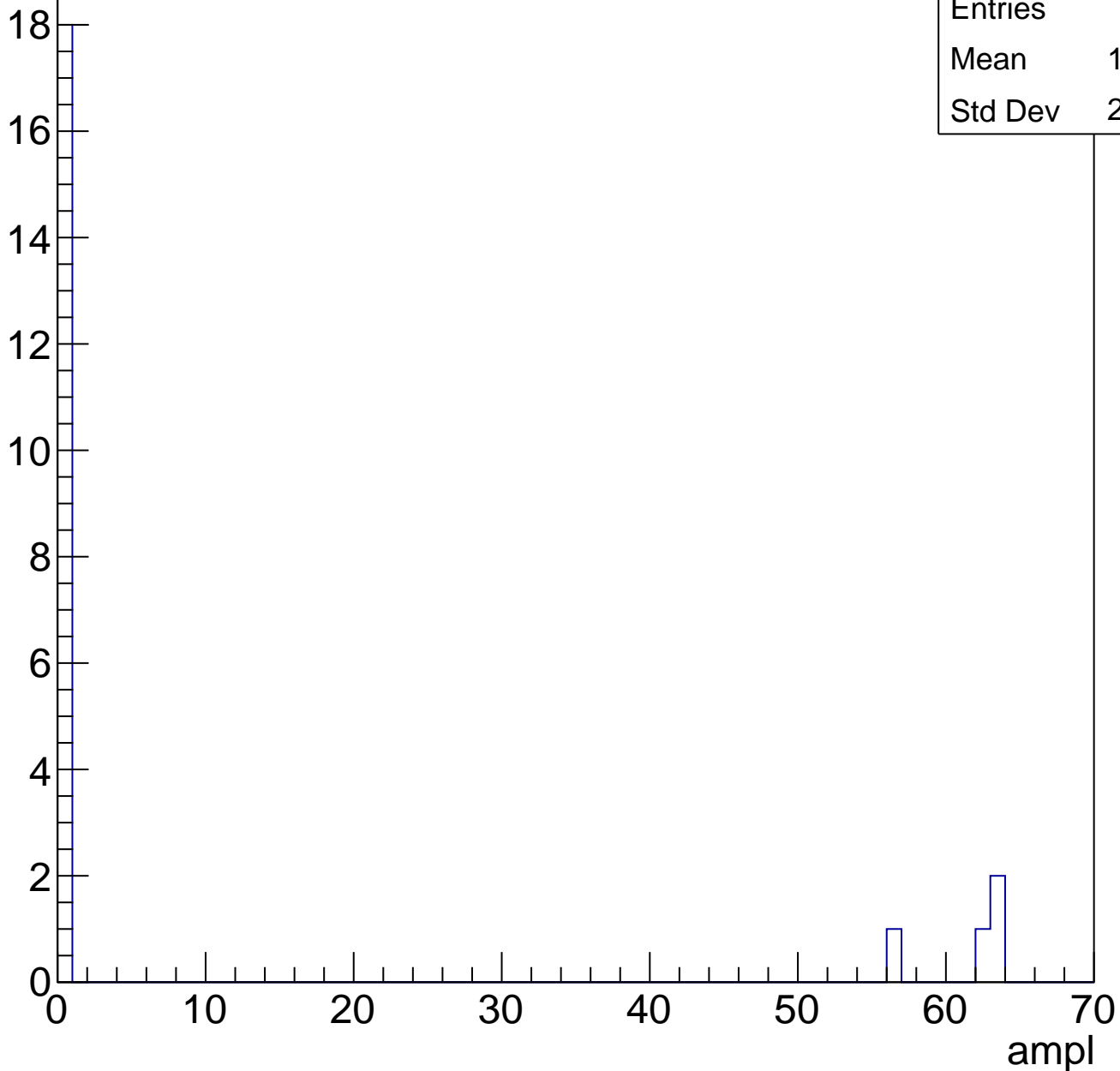


# B1L103S, U3-ch60, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	22
Mean	11.09
Std Dev	23.56

Entry



# B1L103S, U3-ch61, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	138
Mean	17.8
Std Dev	14.57

**Gaus mean : 29.6972**

**Gaus Width: 3.2614**

Entry

50

40

30

20

10

0

0

10

20

30

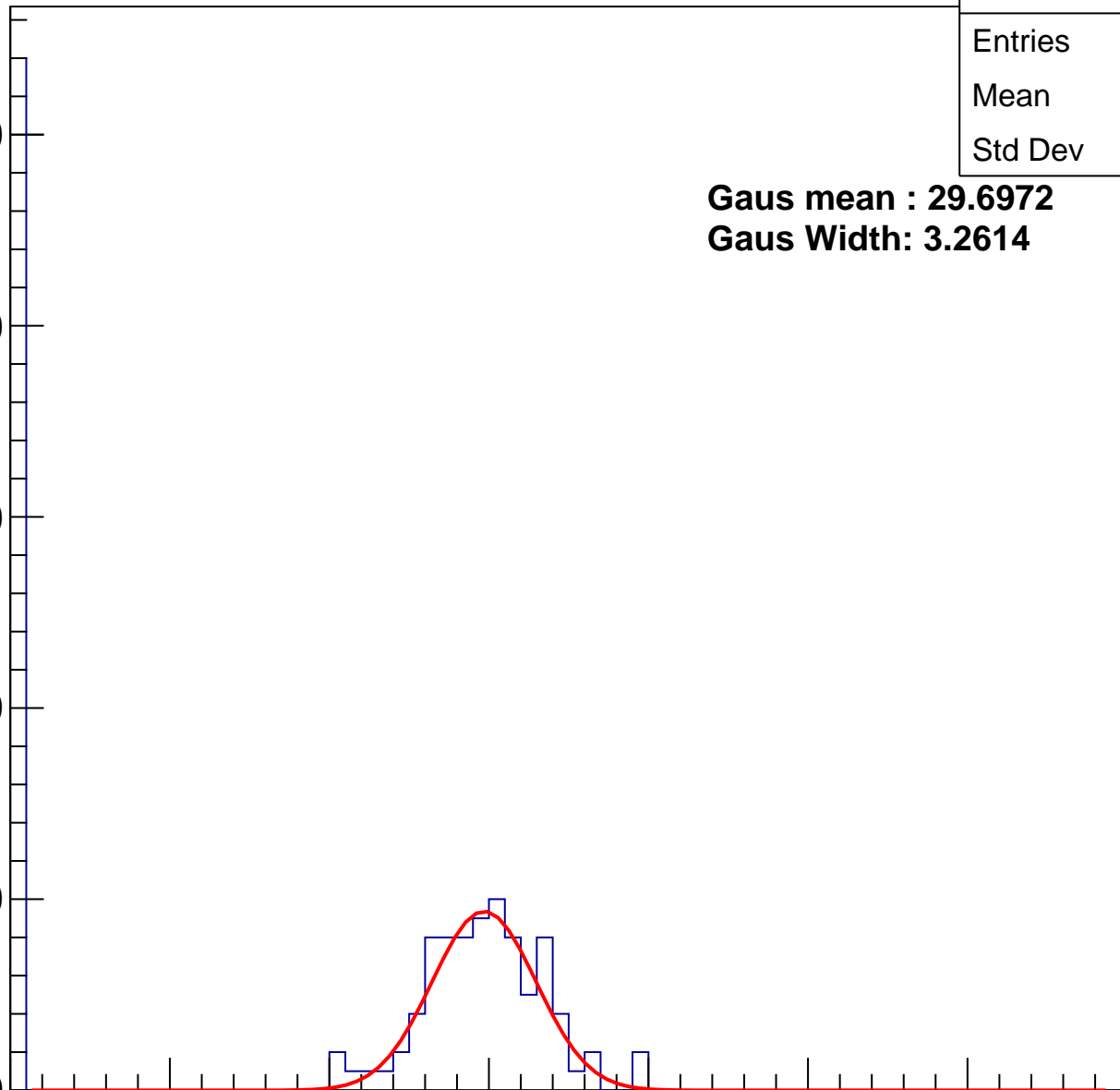
40

50

60

70

ampl



# B1L103S, U3-ch61, adc1

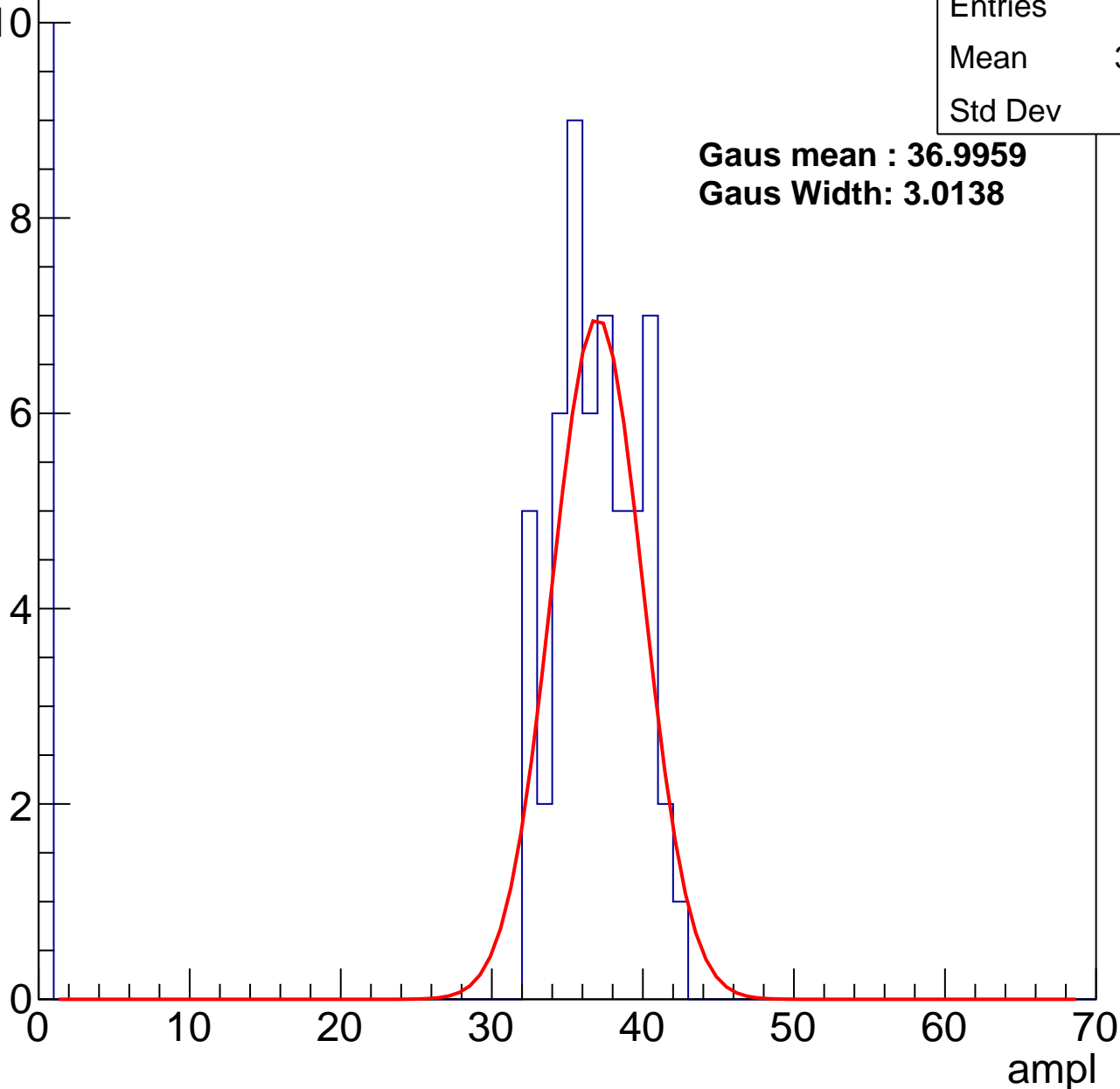
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	65
Mean	30.91
Std Dev	13.4

**Gaus mean : 36.9959**

**Gaus Width: 3.0138**



# B1L103S, U3-ch61, adc2

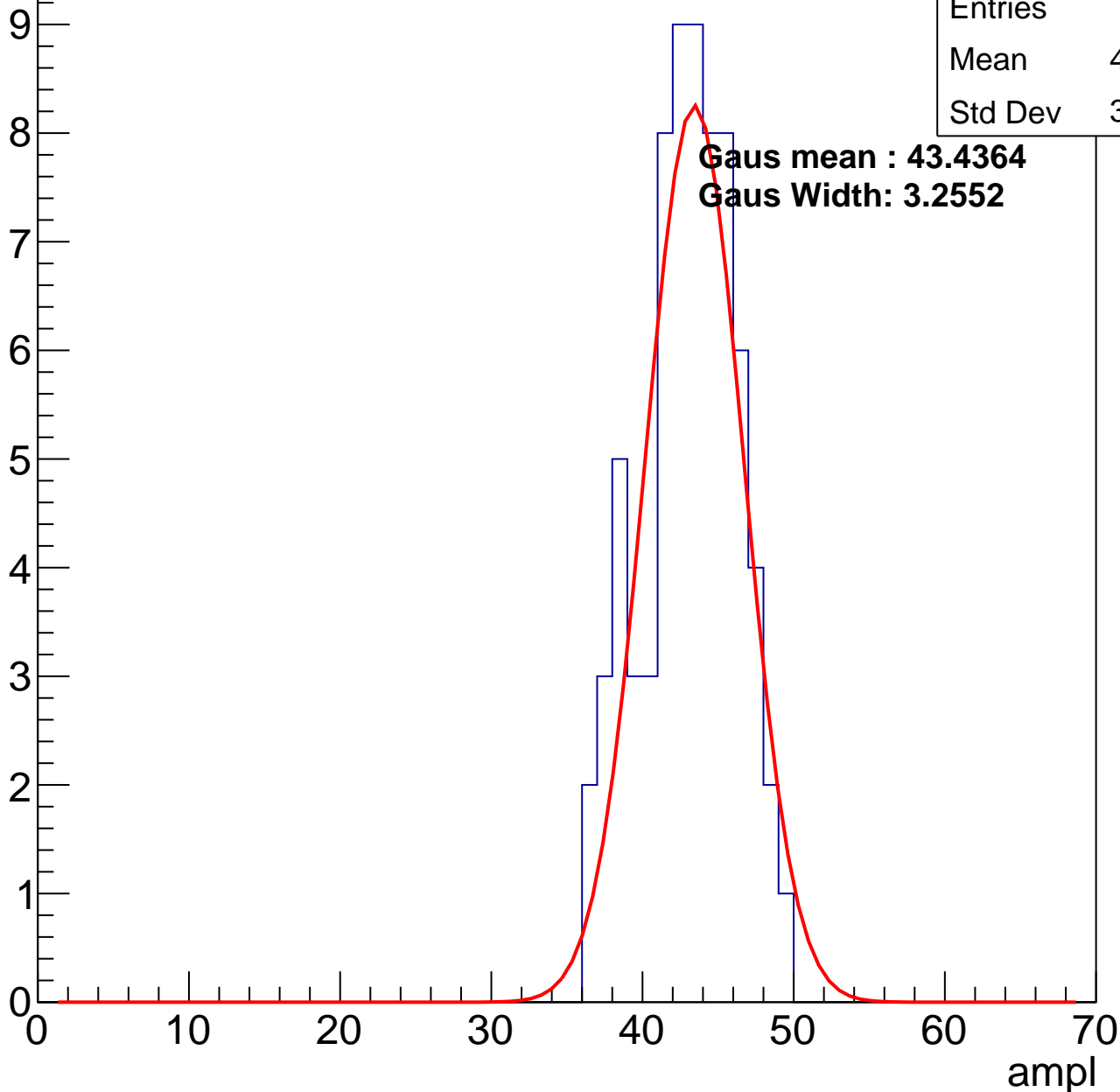
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	71
Mean	42.59
Std Dev	3.093

**Gaus mean : 43.4364**

**Gaus Width: 3.2552**



# B1L103S, U3-ch61, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

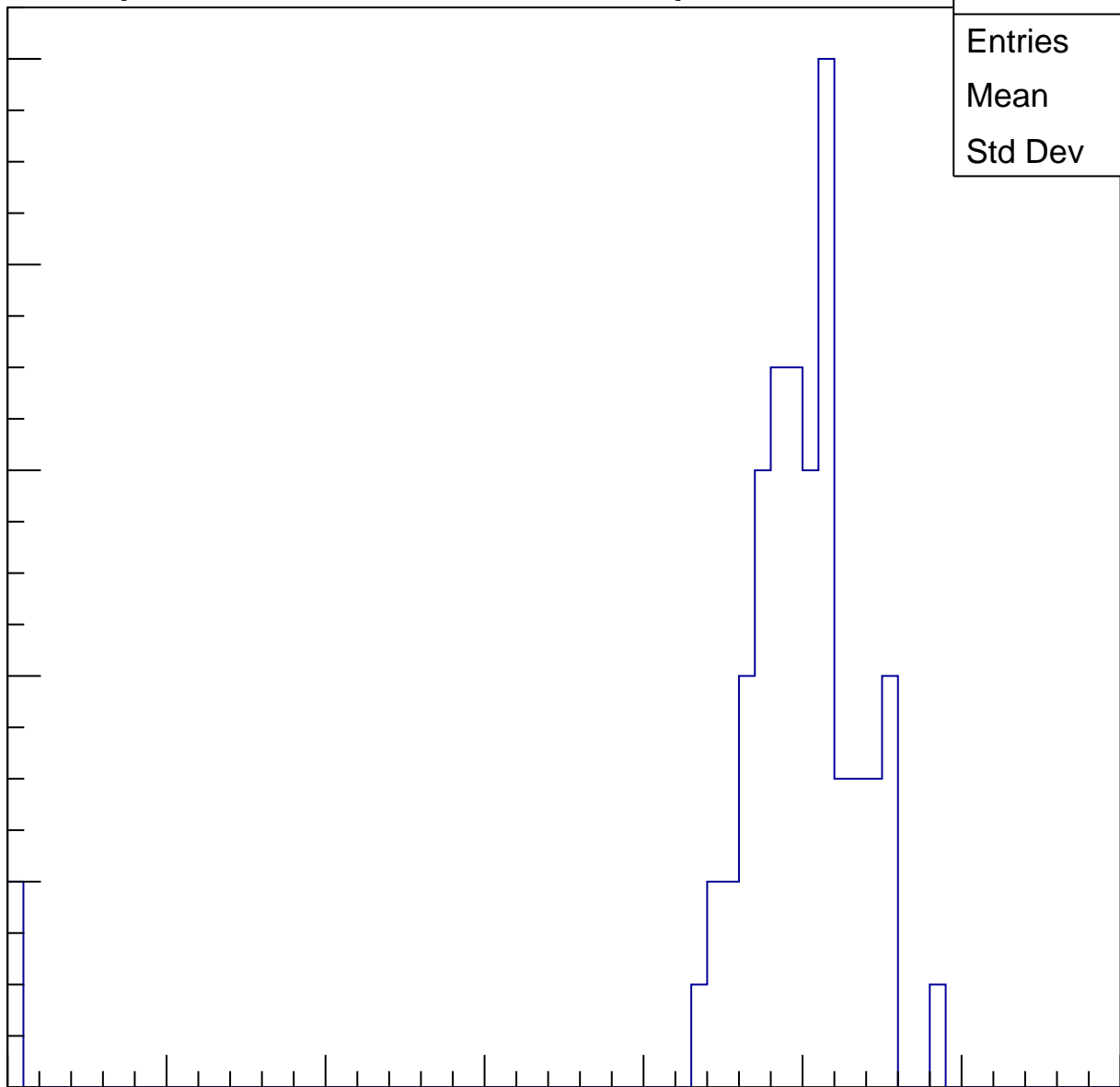
Entries	61
Mean	48.05
Std Dev	9.368

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

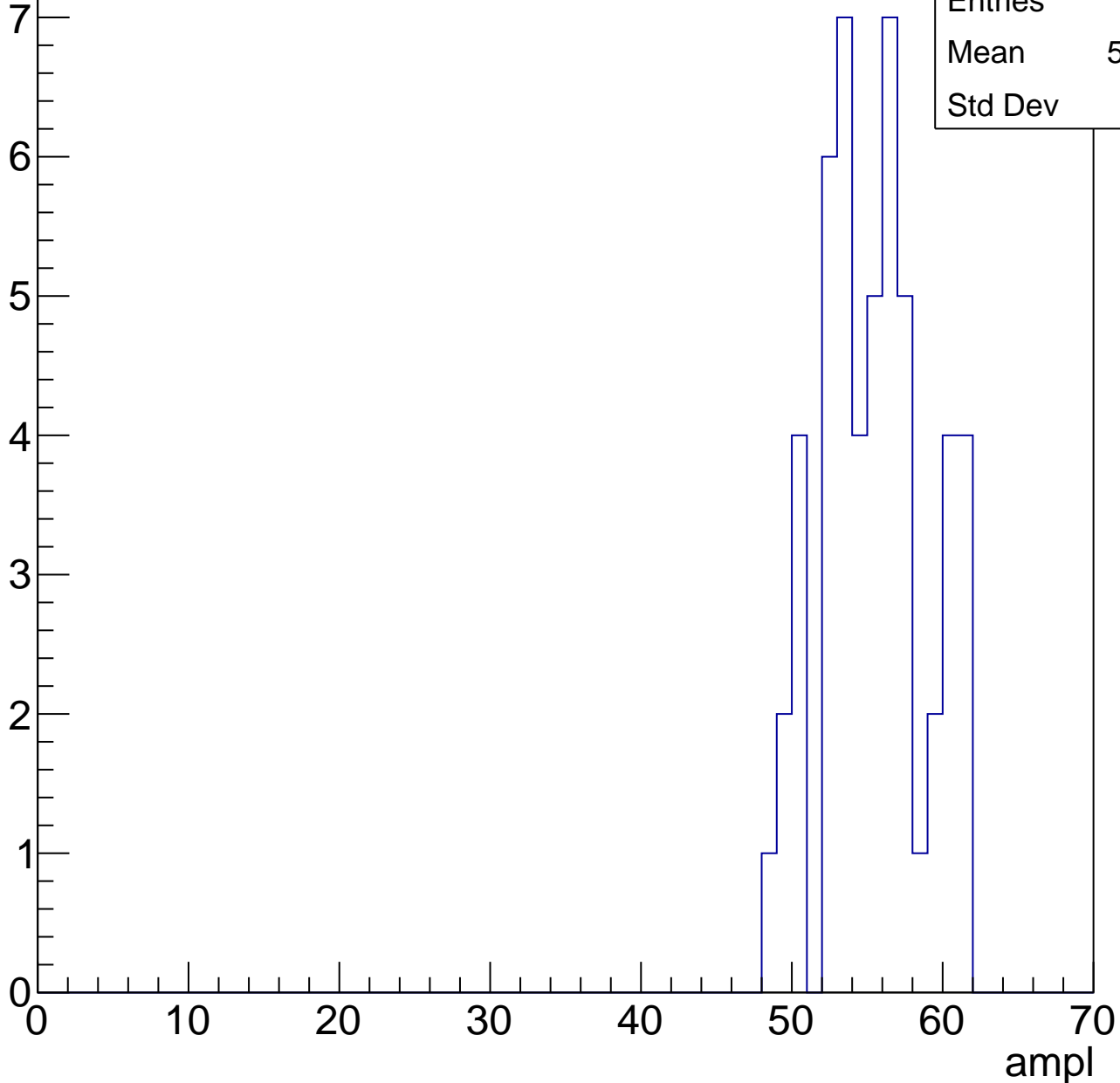


# B1L103S, U3-ch61, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	52
Mean	54.94
Std Dev	3.45



# B1L103S, U3-ch61, adc5

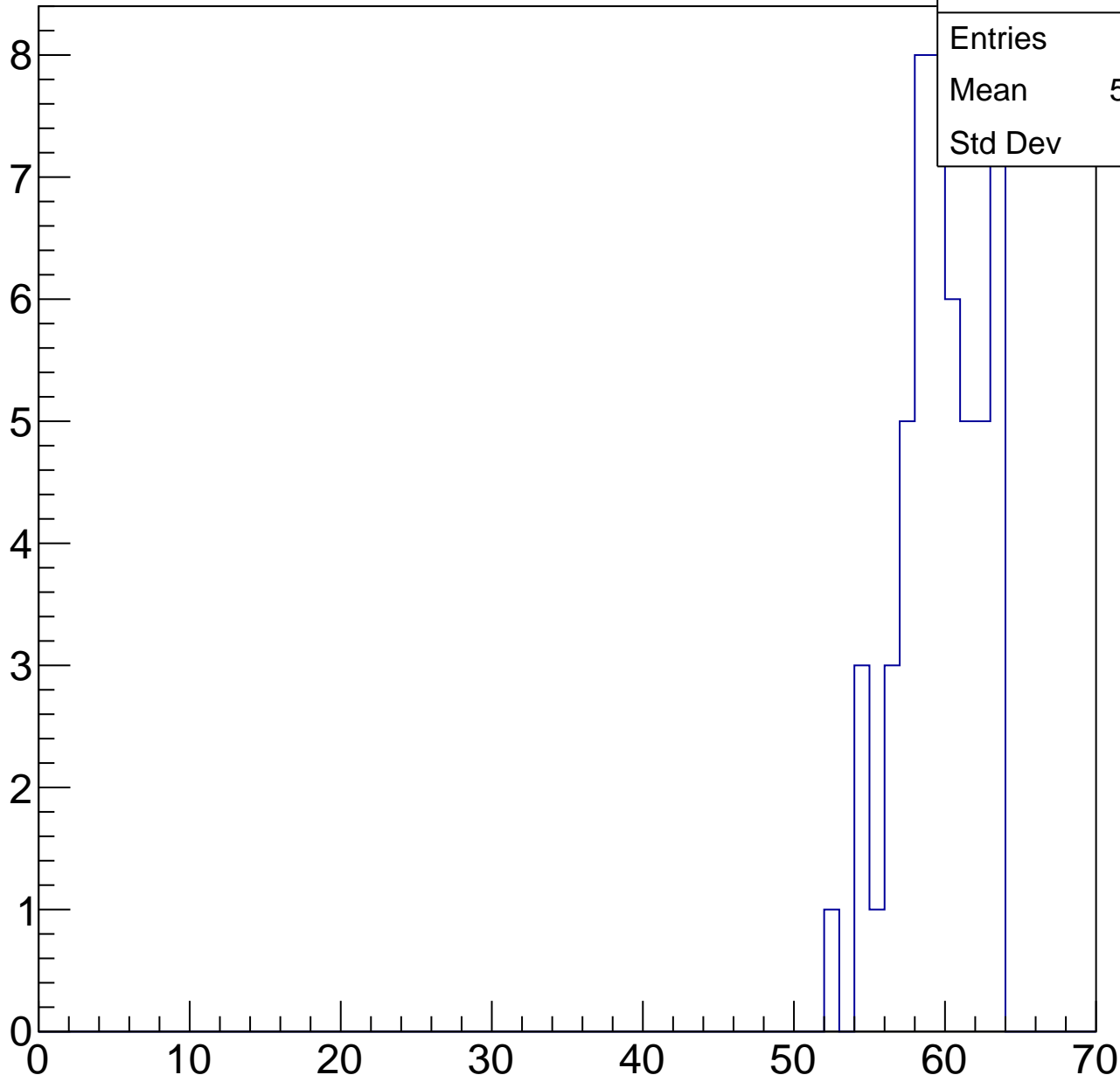
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	53
Mean	59.19
Std Dev	2.72

ampl

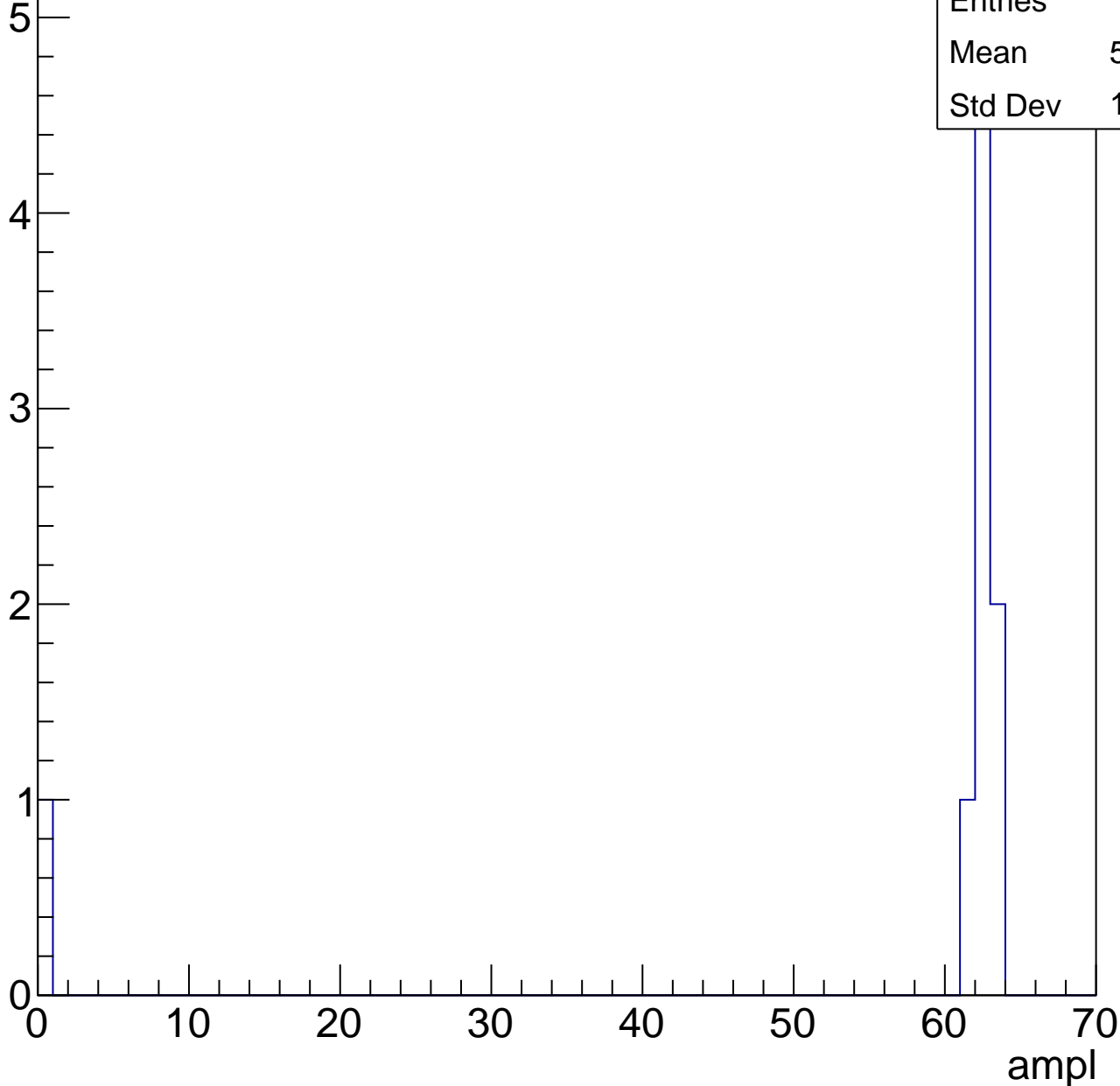


# B1L103S, U3-ch61, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	9
Mean	55.22
Std Dev	19.53





# B1L103S, U3-ch61, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



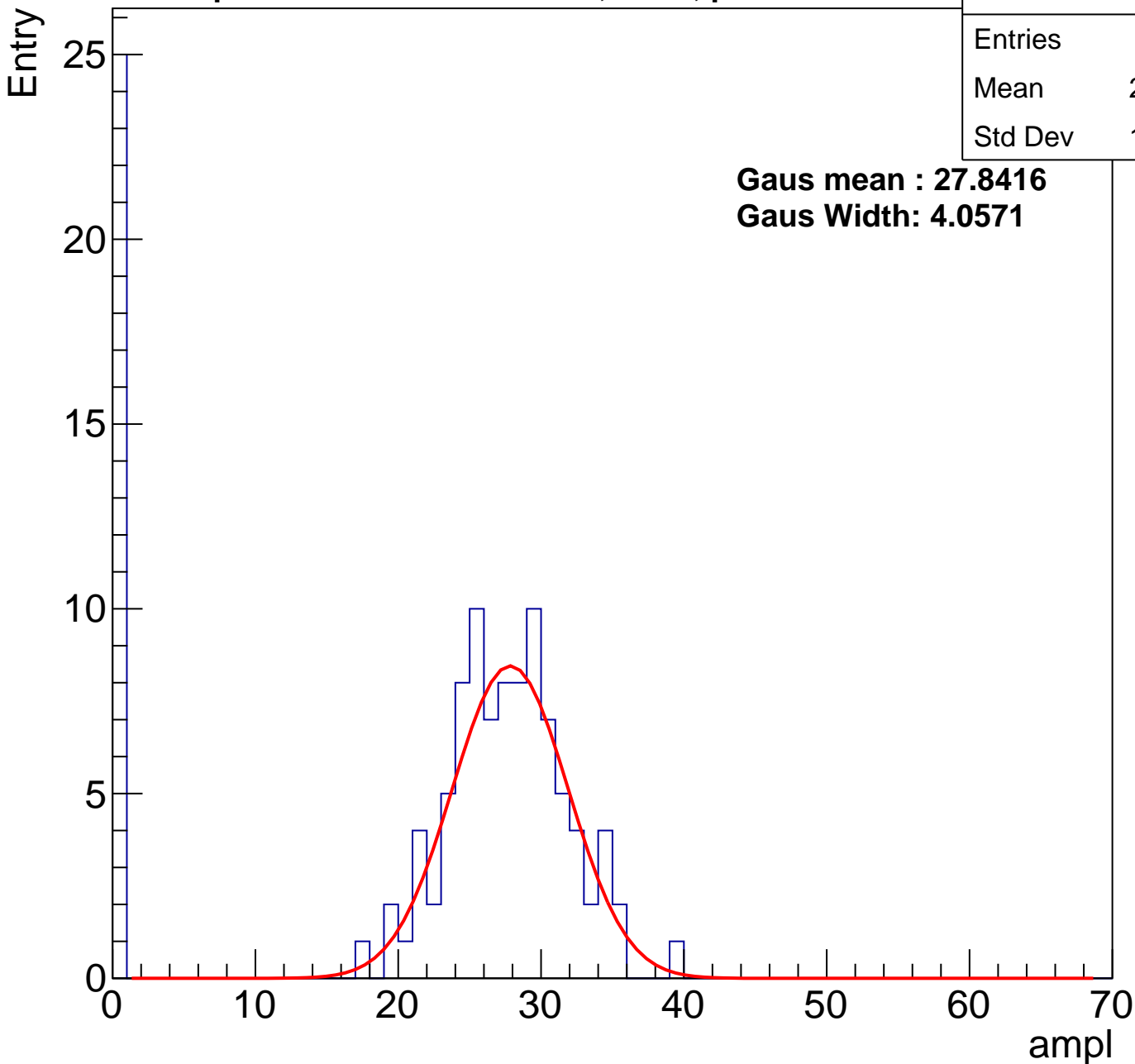
# B1L103S, U3-ch62, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	116
Mean	21.34
Std Dev	11.75

**Gaus mean : 27.8416**

**Gaus Width: 4.0571**



# B1L103S, U3-ch62, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	79
Mean	27.81
Std Dev	13.76

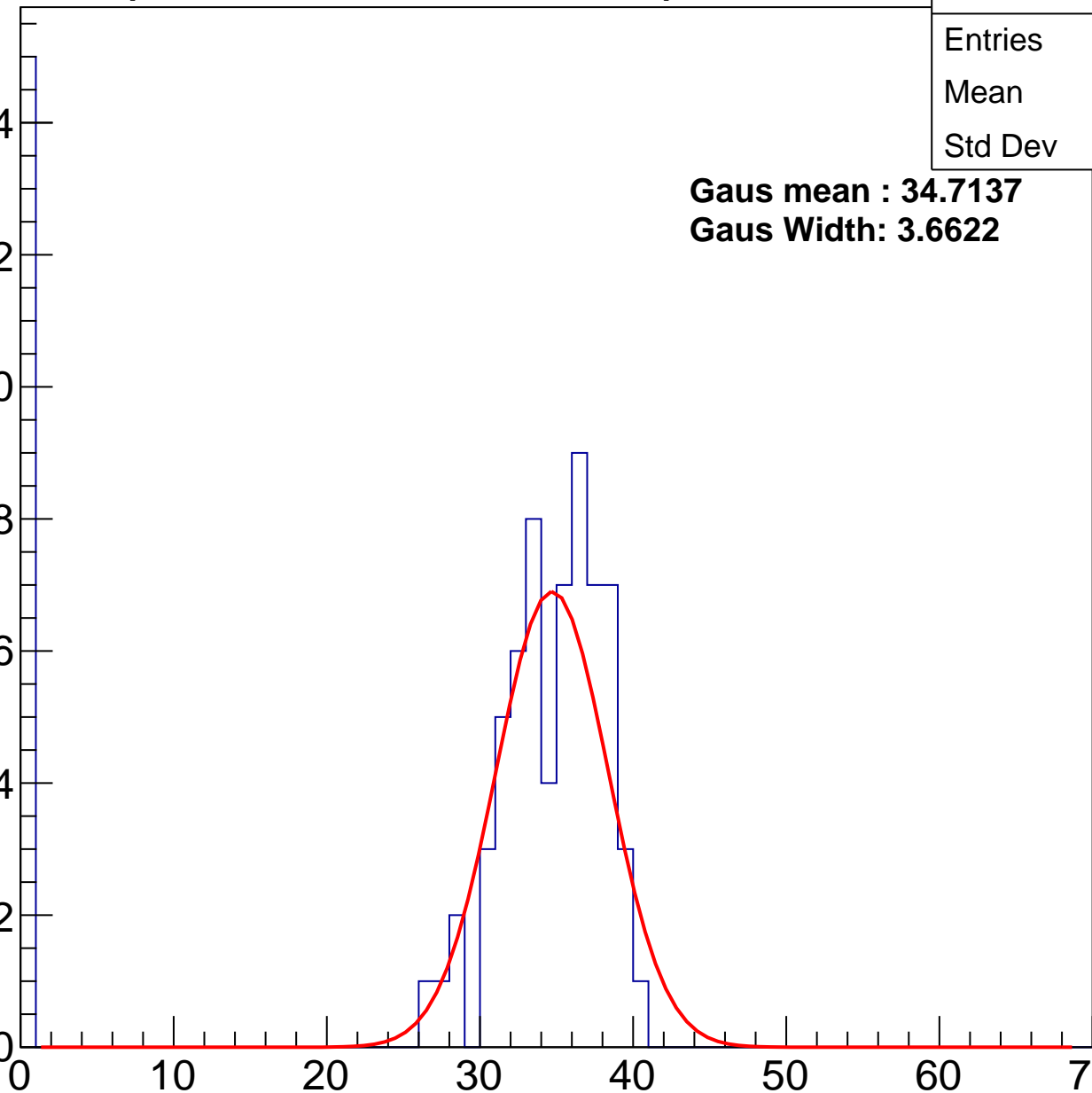
**Gaus mean : 34.7137**

**Gaus Width: 3.6622**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U3-ch62, adc2

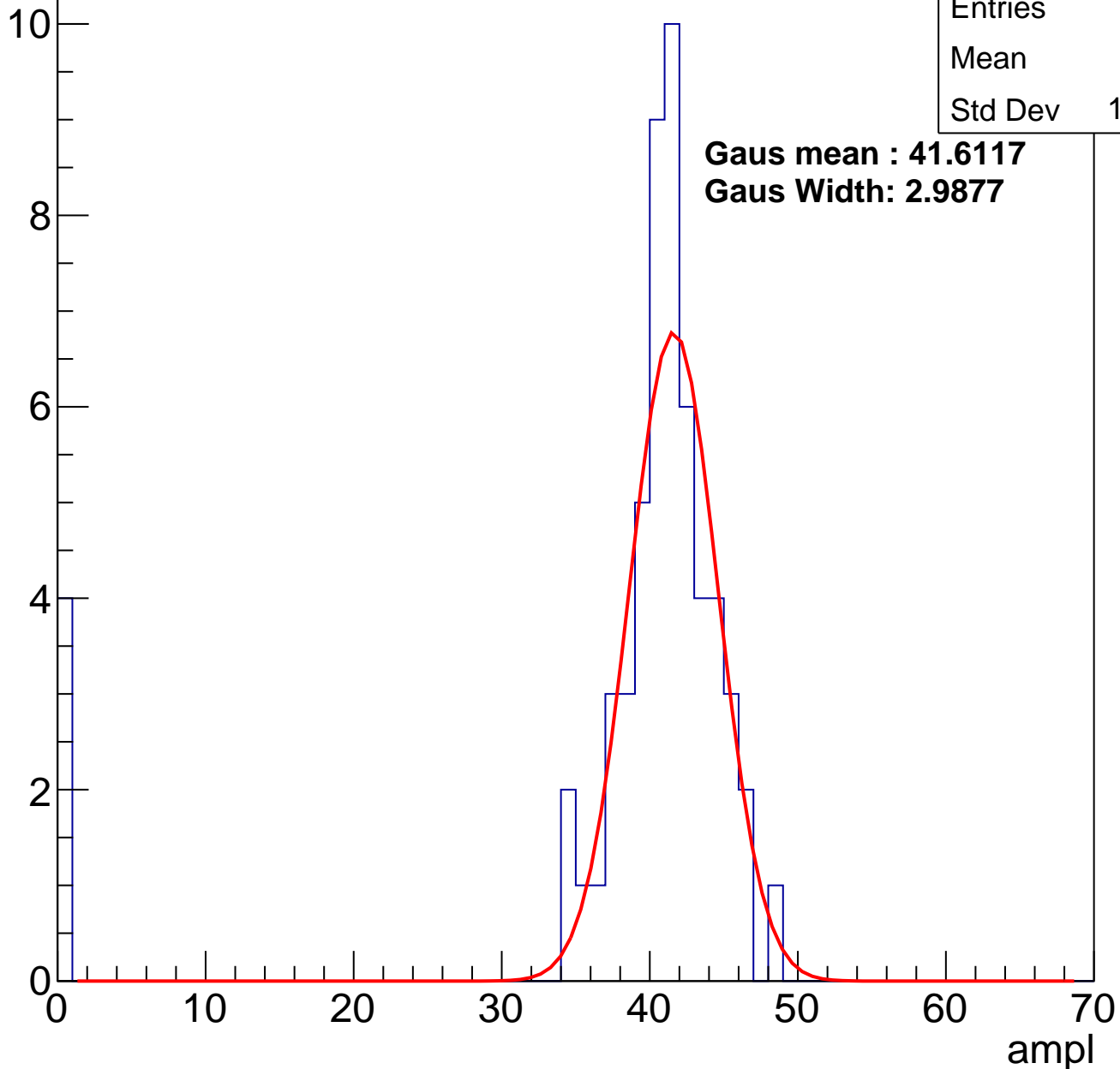
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	58
Mean	38
Std Dev	10.72

**Gaus mean : 41.6117**

**Gaus Width: 2.9877**

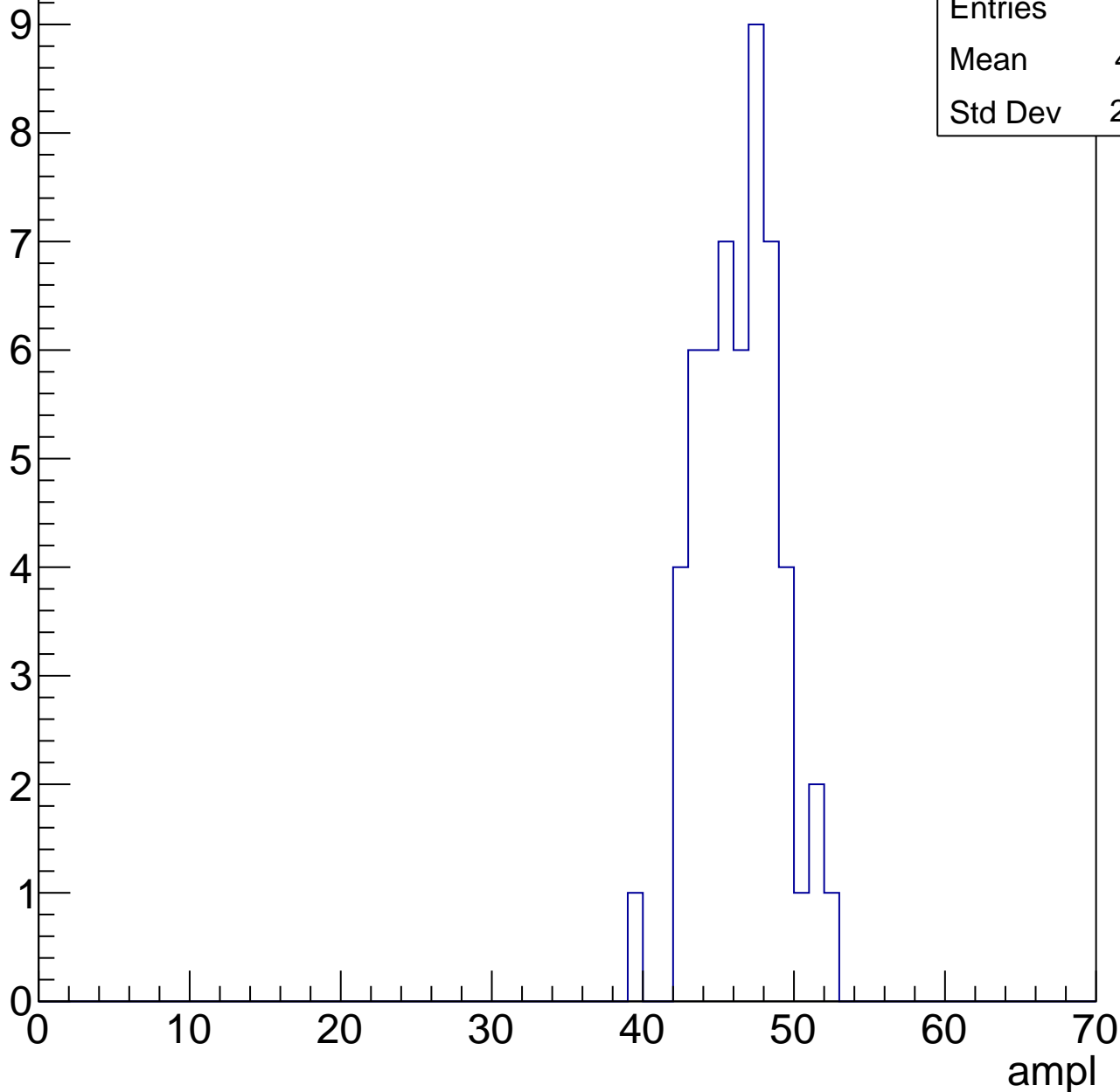
Entry



# B1L103S, U3-ch62, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

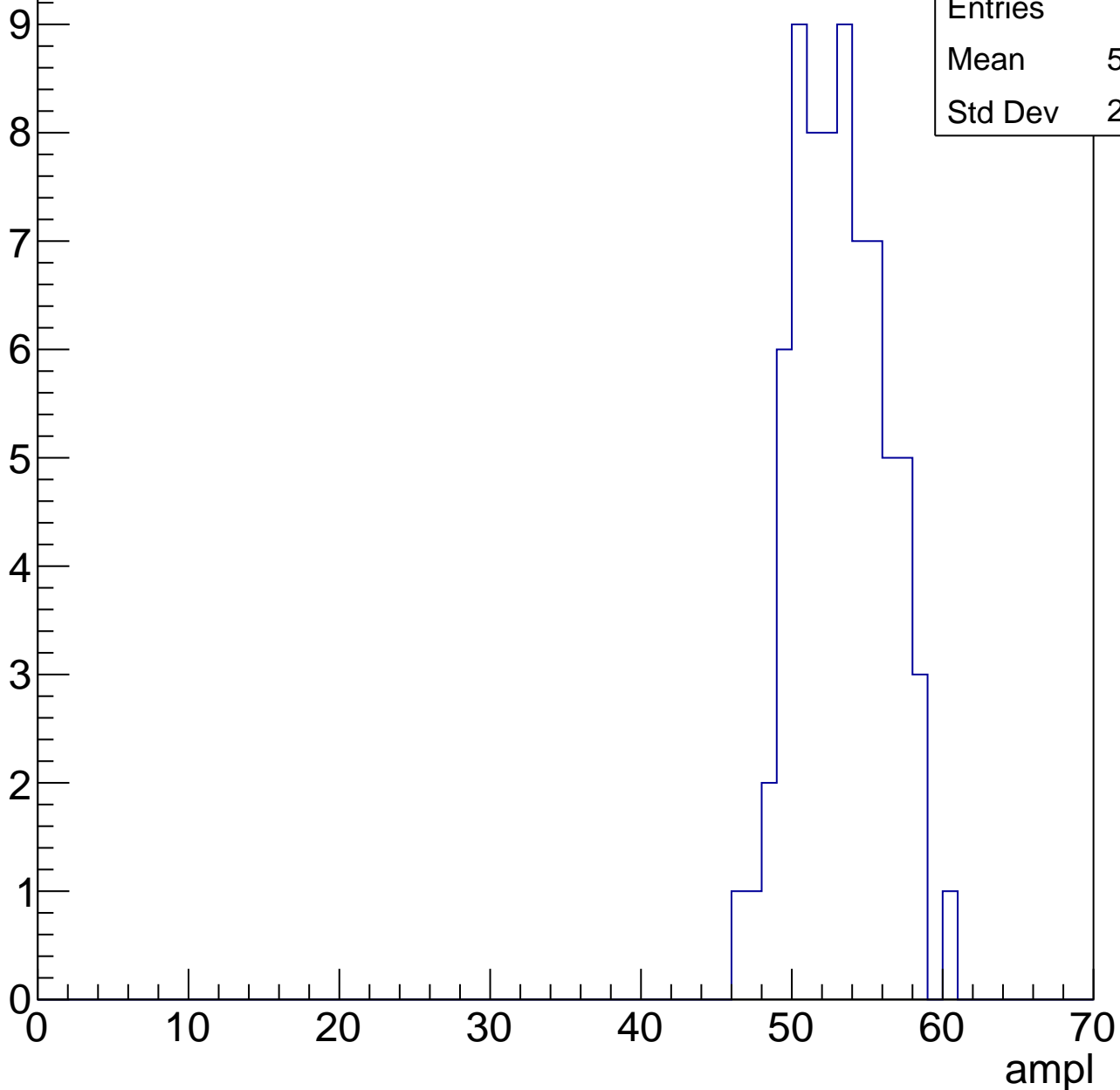
Entry



# B1L103S, U3-ch62, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

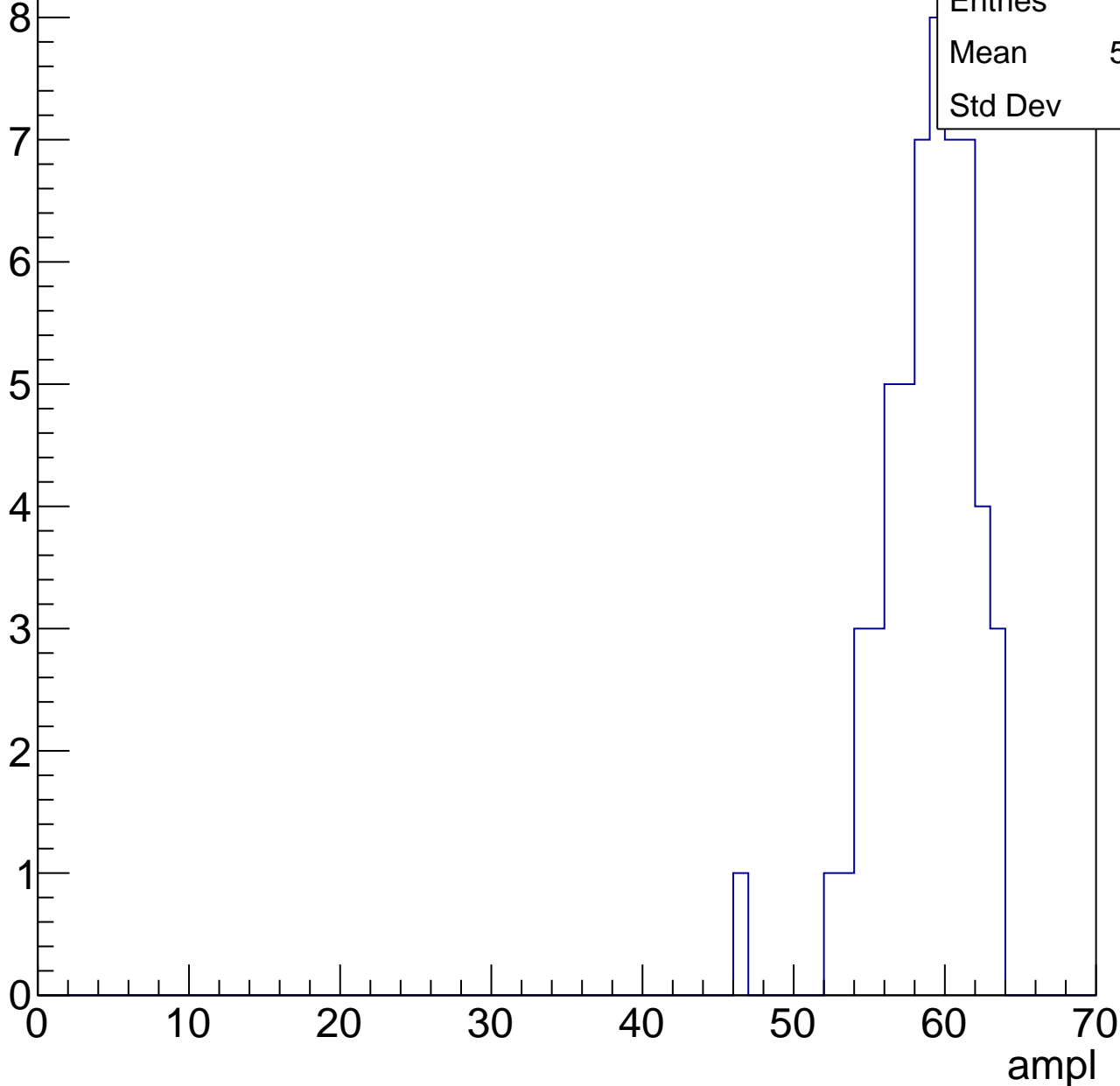


# B1L103S, U3-ch62, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	55
Mean	58.27
Std Dev	3.13

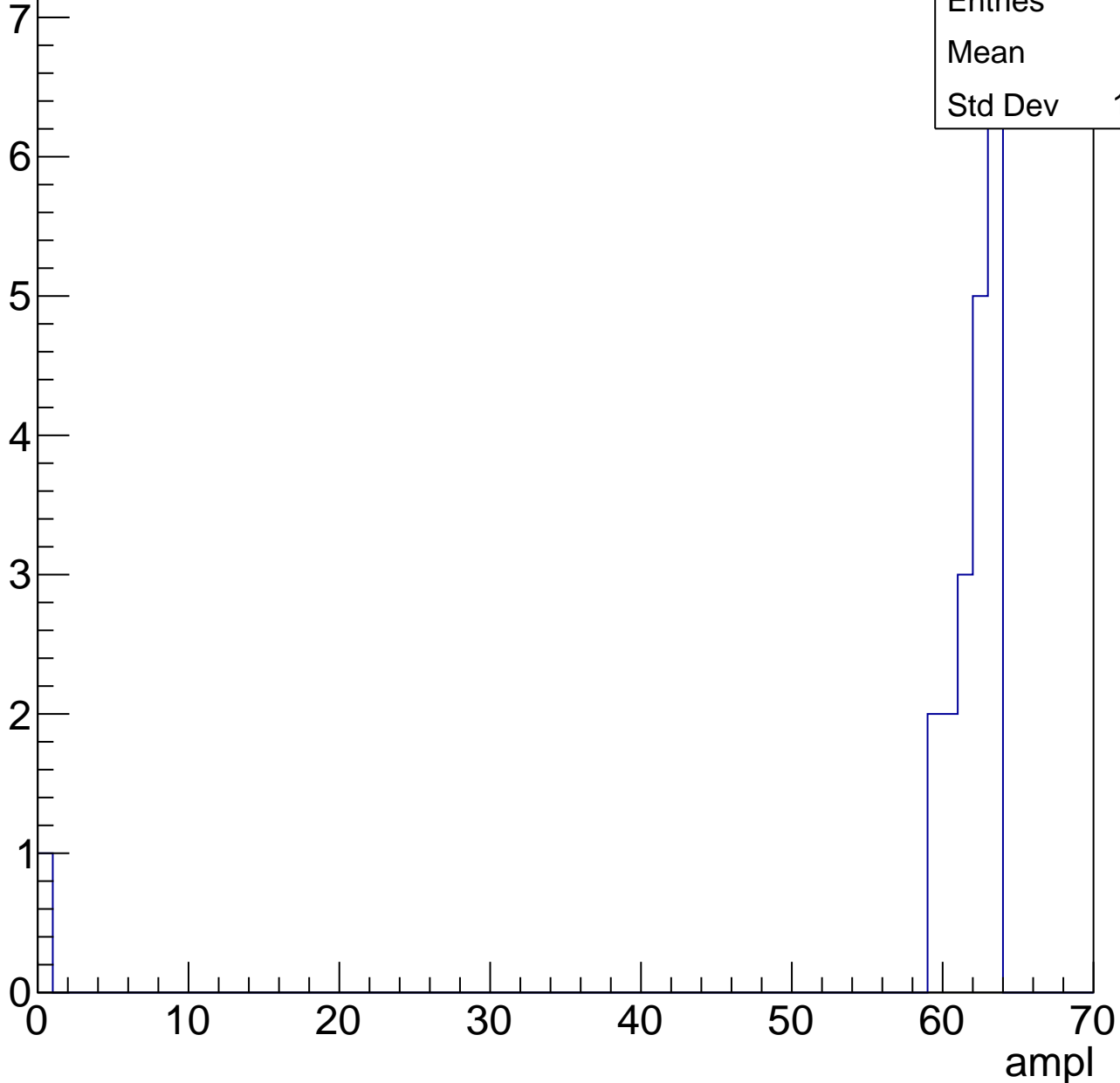


# B1L103S, U3-ch62, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	20
Mean	58.6
Std Dev	13.51





# B1L103S, U3-ch62, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51

Entry



# B1L103S, U3-ch63, adc0

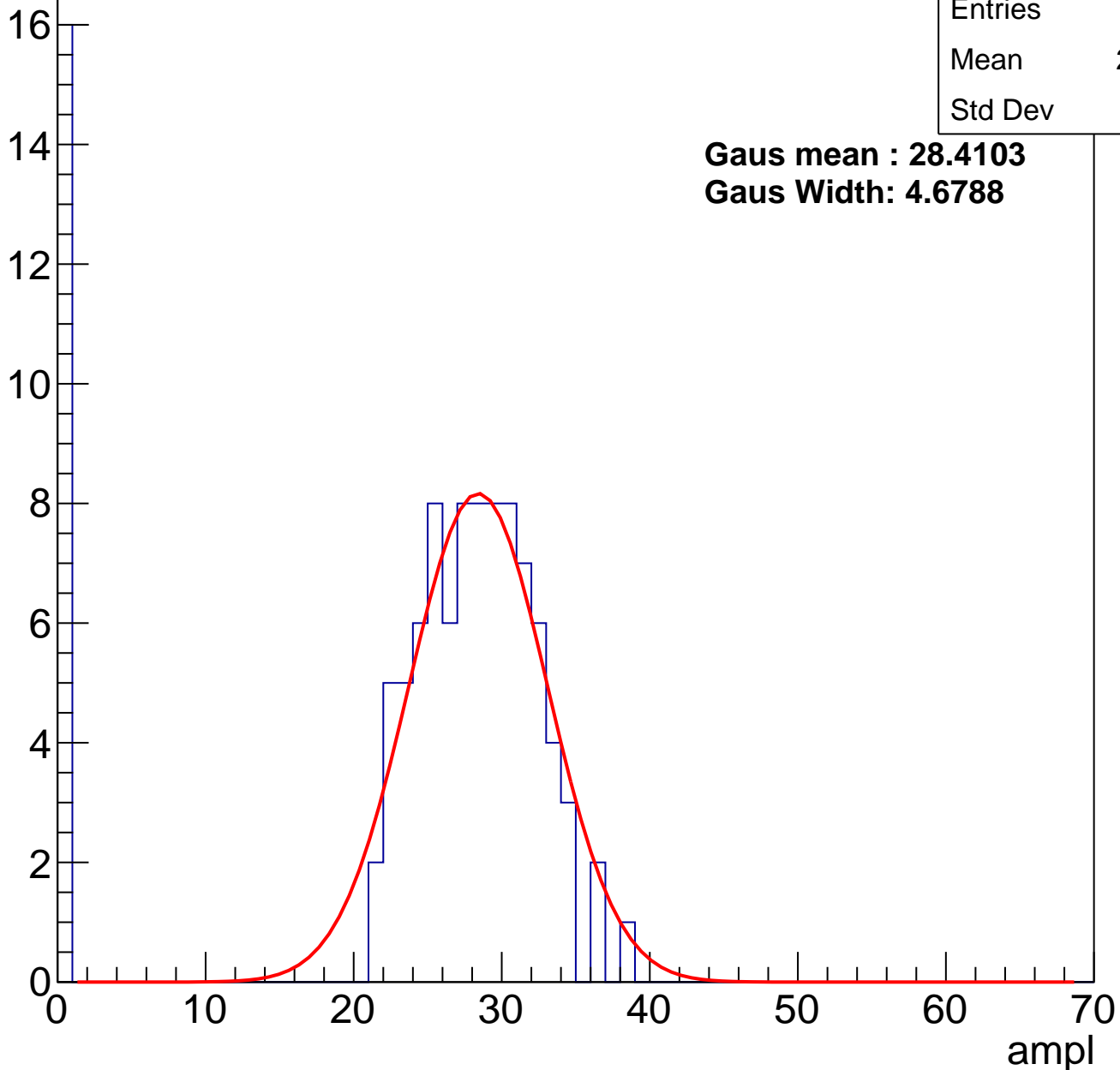
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	103
Mean	23.61
Std Dev	10.7

**Gaus mean : 28.4103**

**Gaus Width: 4.6788**

Entry



# B1L103S, U3-ch63, adc1

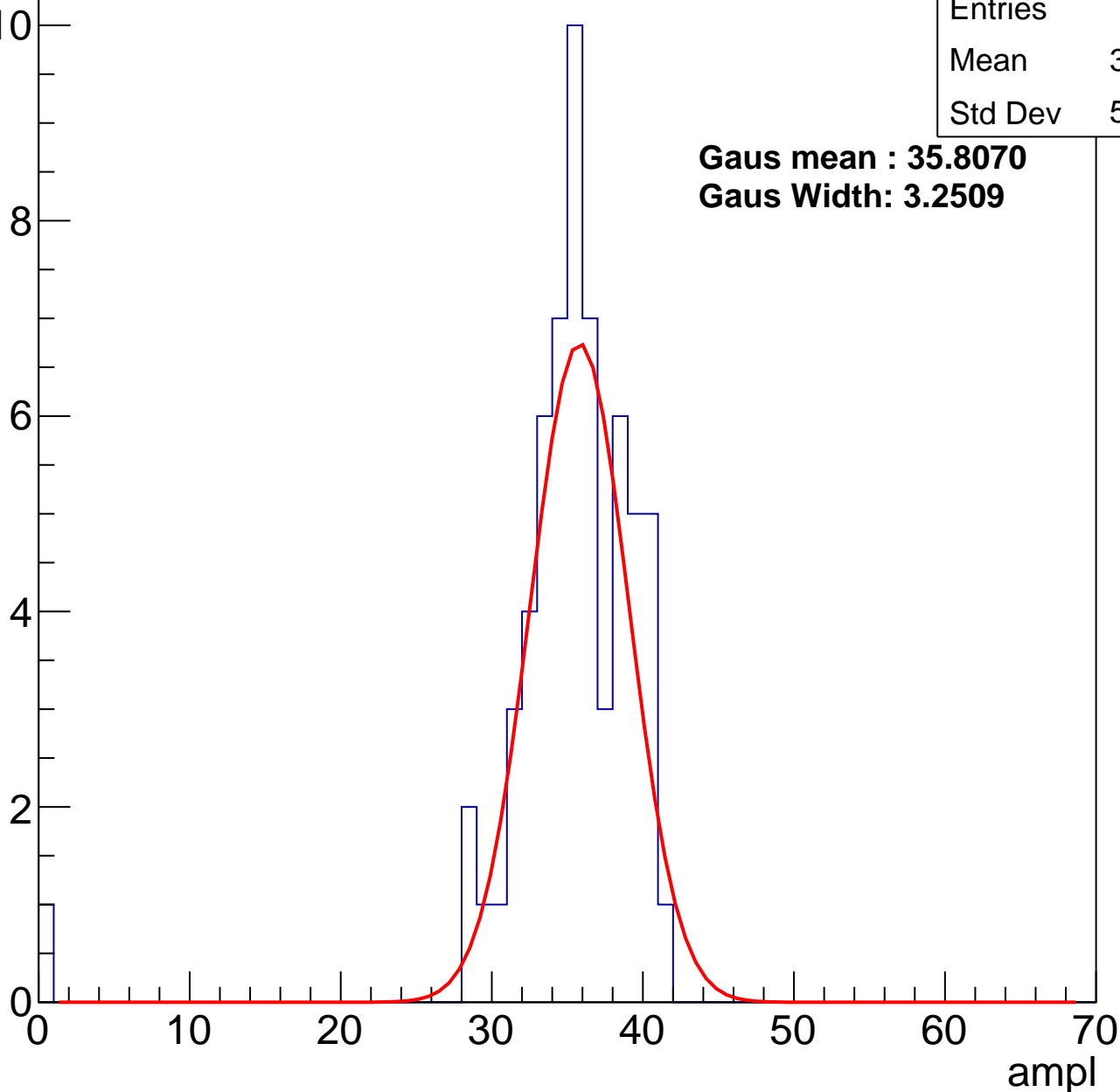
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	34.66
Std Dev	5.397

**Gaus mean : 35.8070**

**Gaus Width: 3.2509**



# B1L103S, U3-ch63, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	70
Mean	32.31
Std Dev	17.13

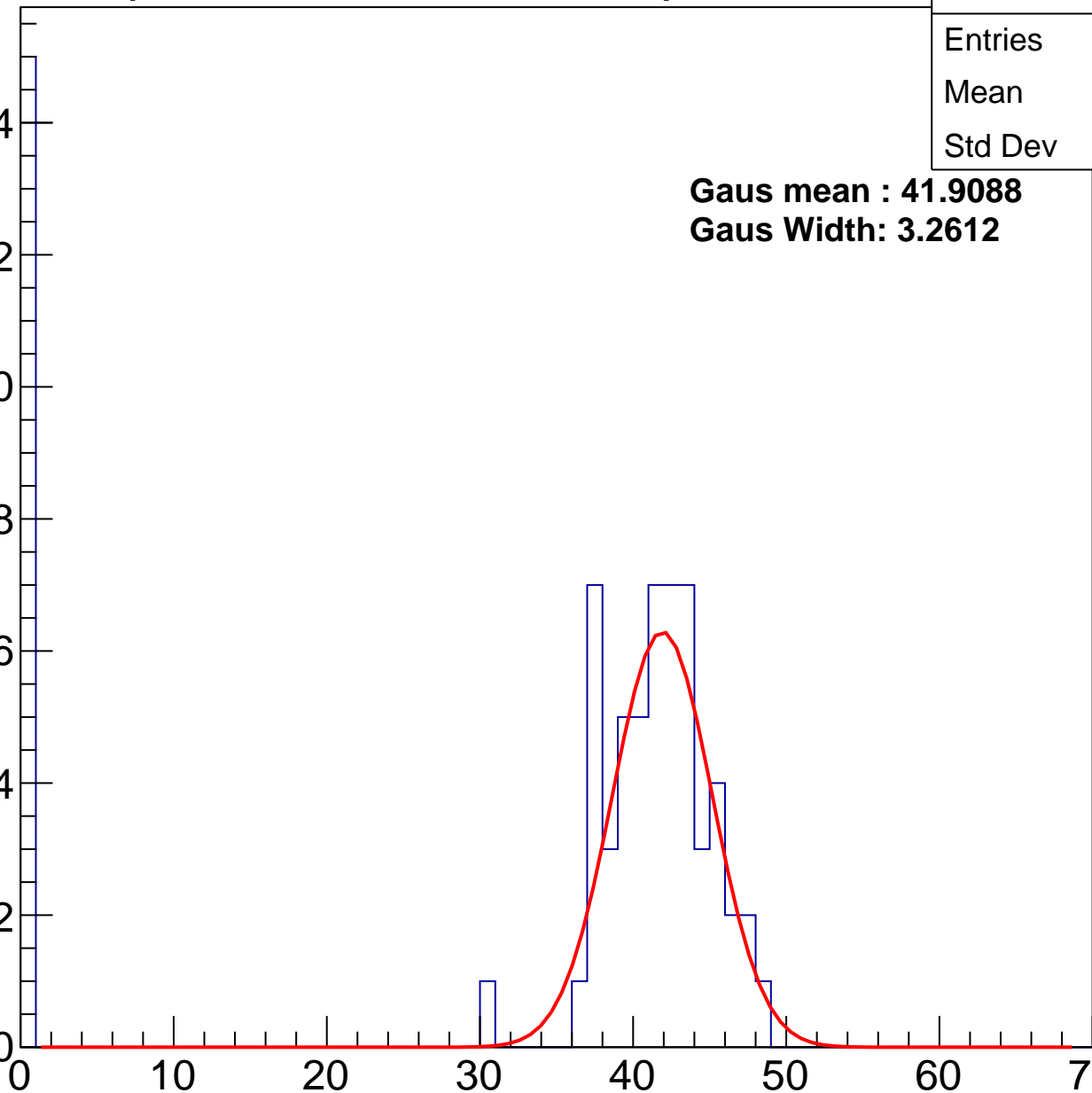
**Gaus mean : 41.9088**

**Gaus Width: 3.2612**

Entry

14  
12  
10  
8  
6  
4  
2  
0

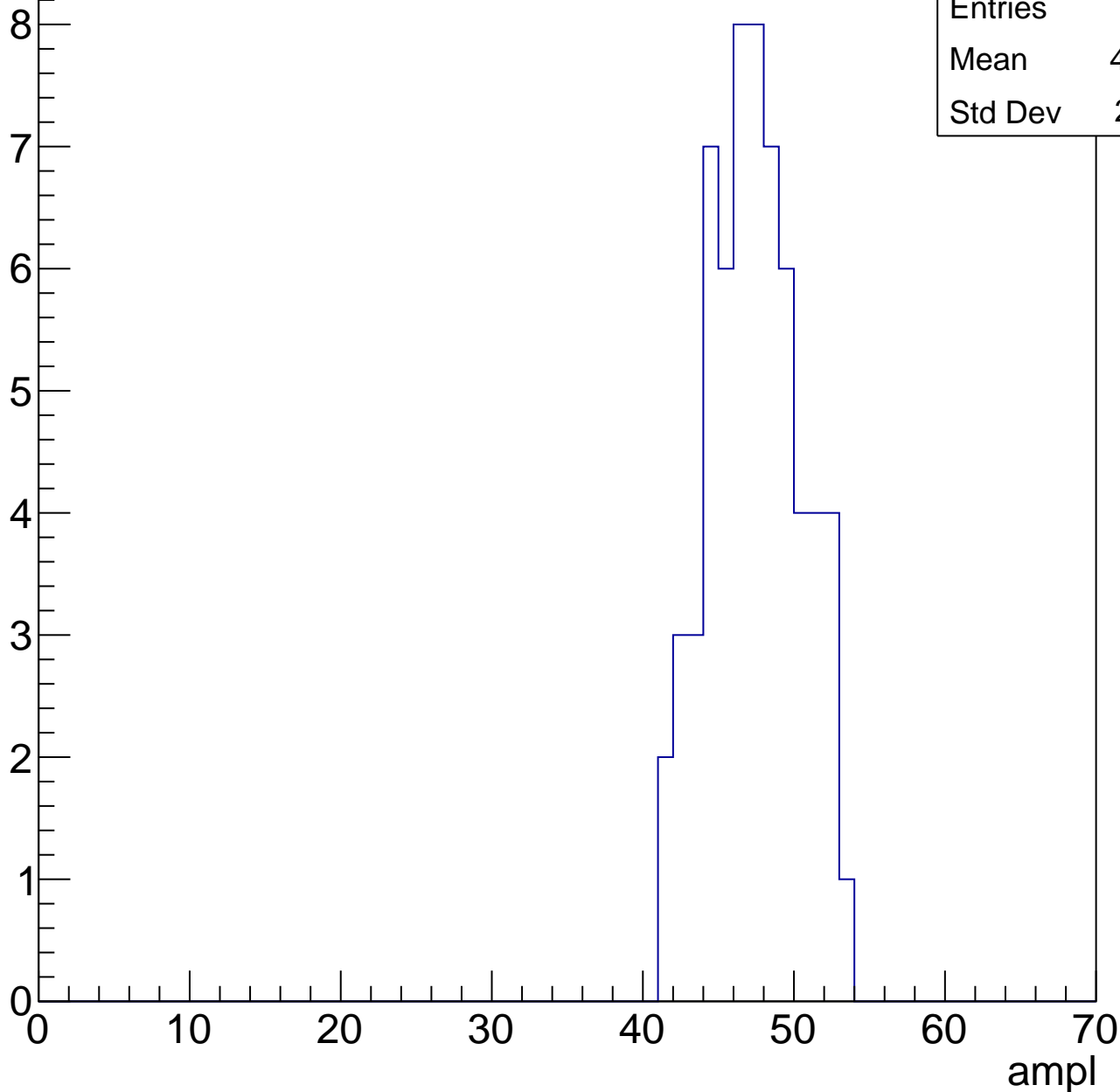
ampl



# B1L103S, U3-ch63, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

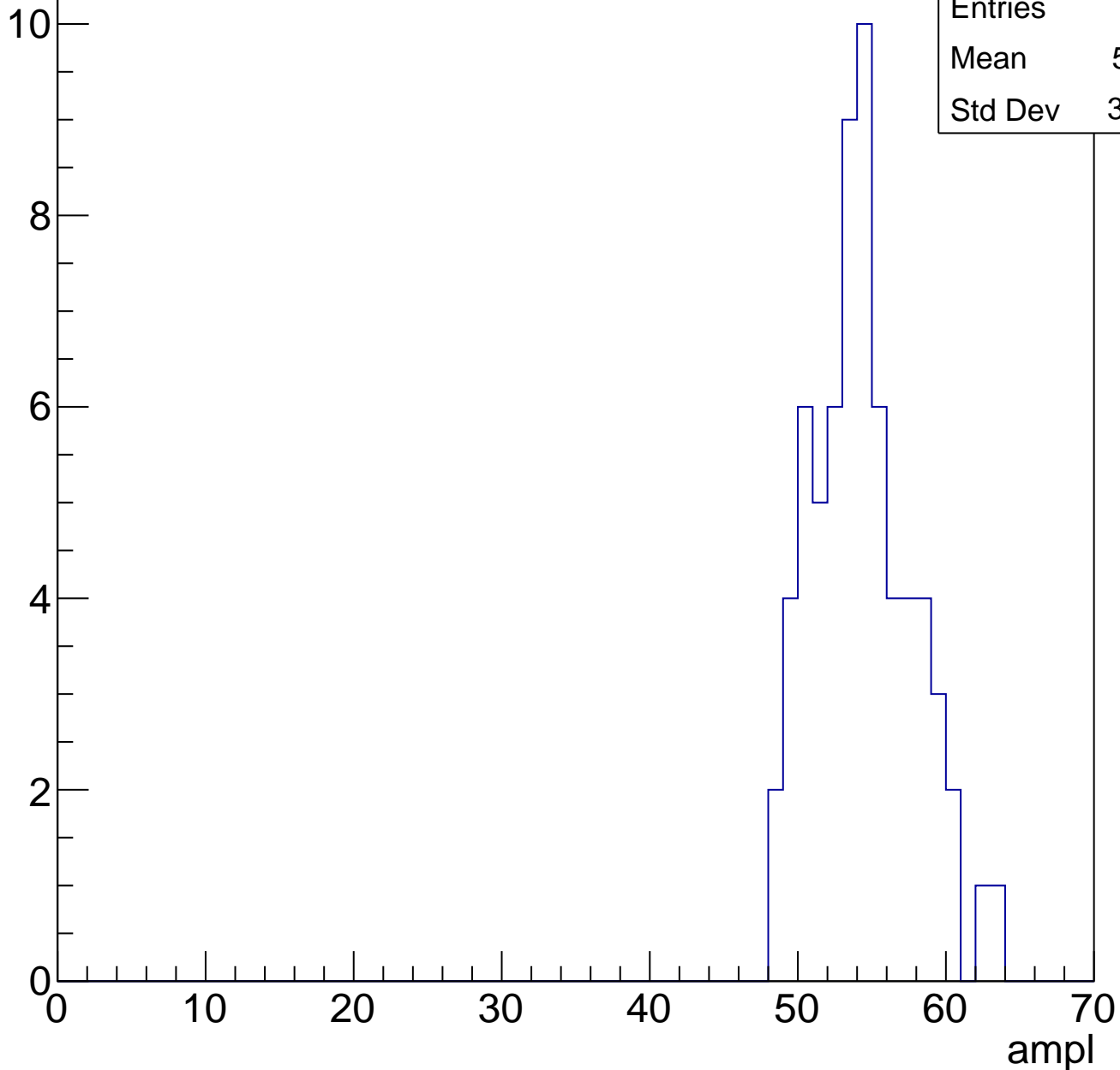


# B1L103S, U3-ch63, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	67
Mean	53.91
Std Dev	3.367

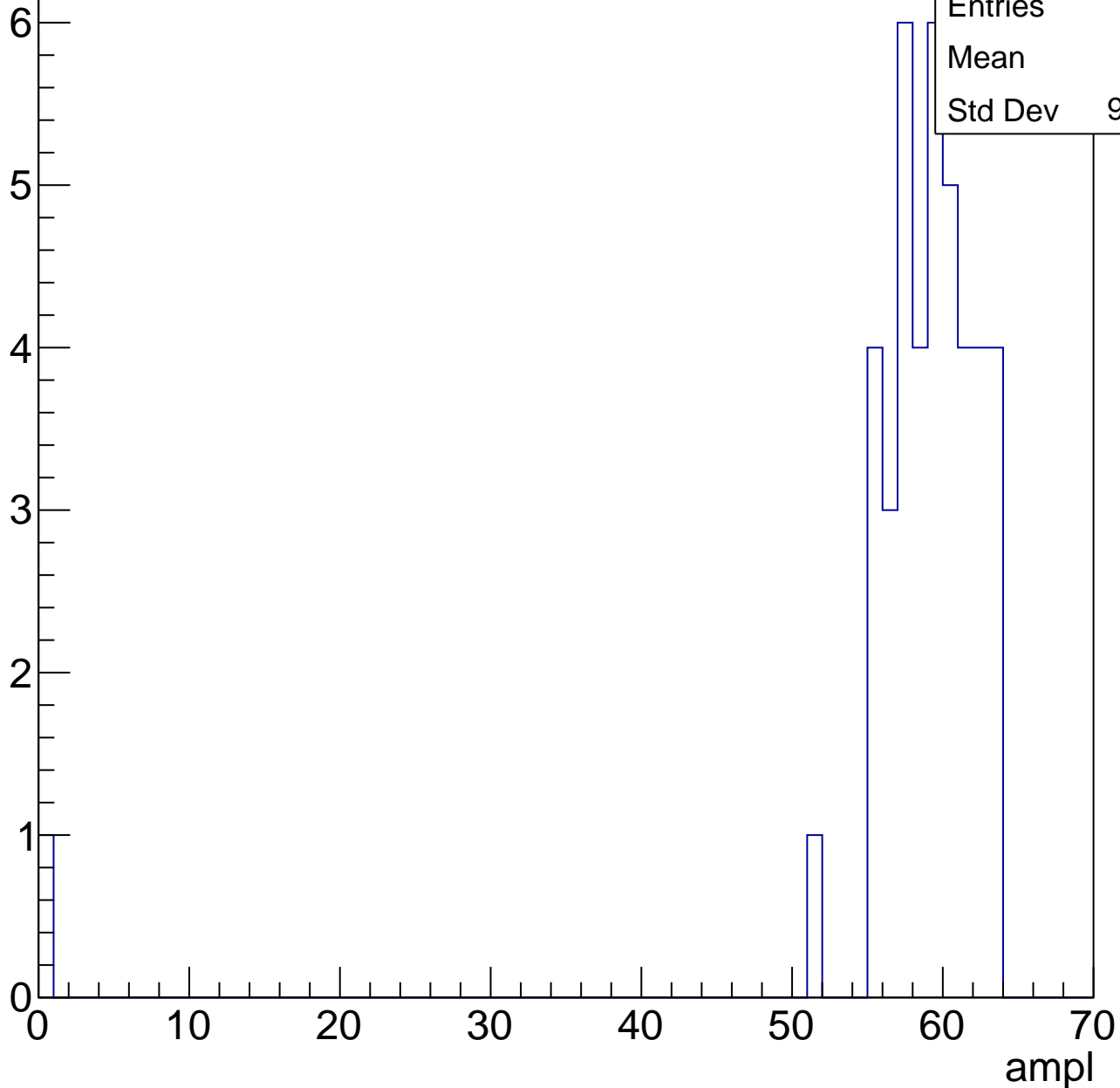
Entry



# B1L103S, U3-ch63, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

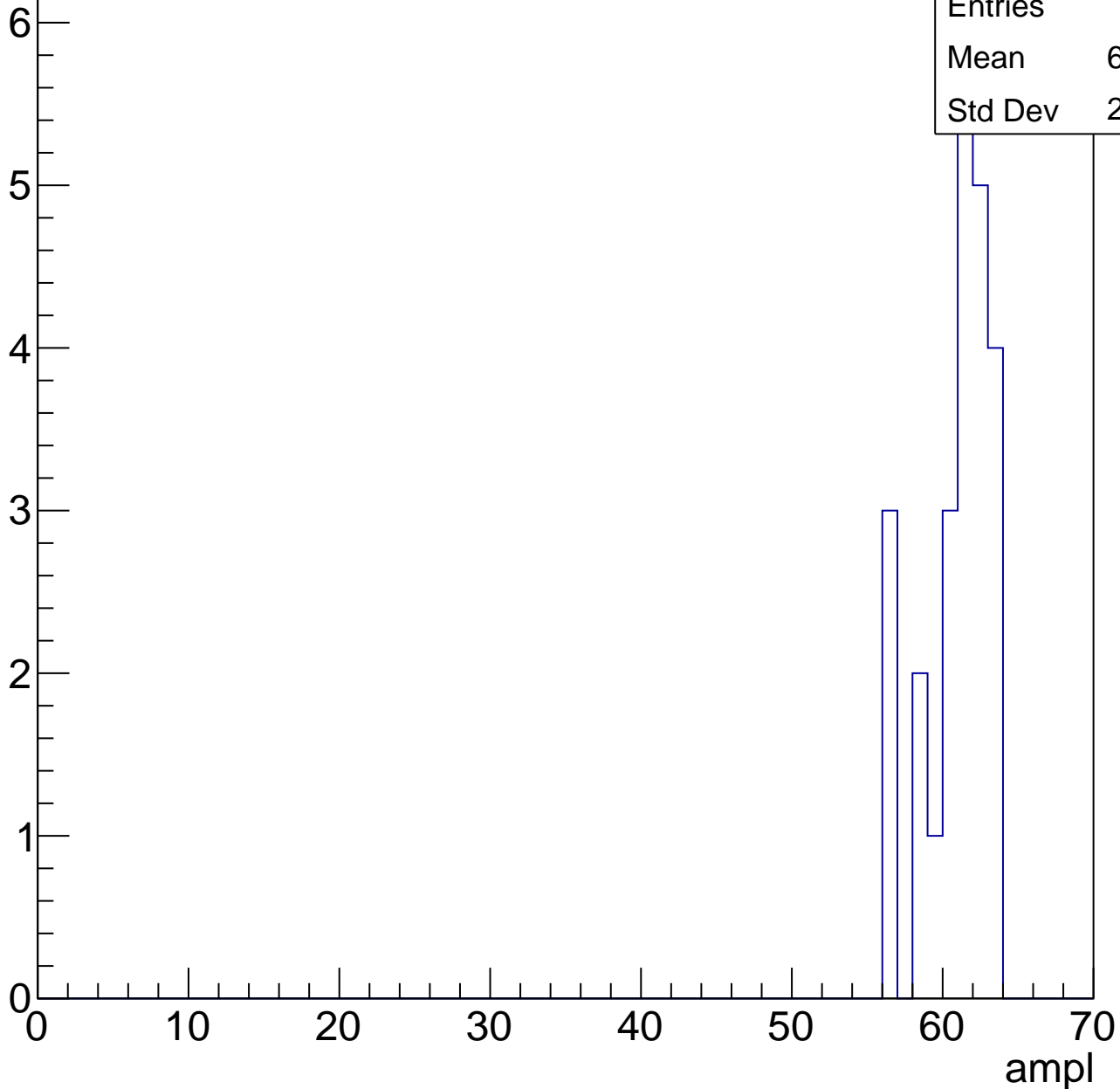


# B1L103S, U3-ch63, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	24
Mean	60.46
Std Dev	2.179

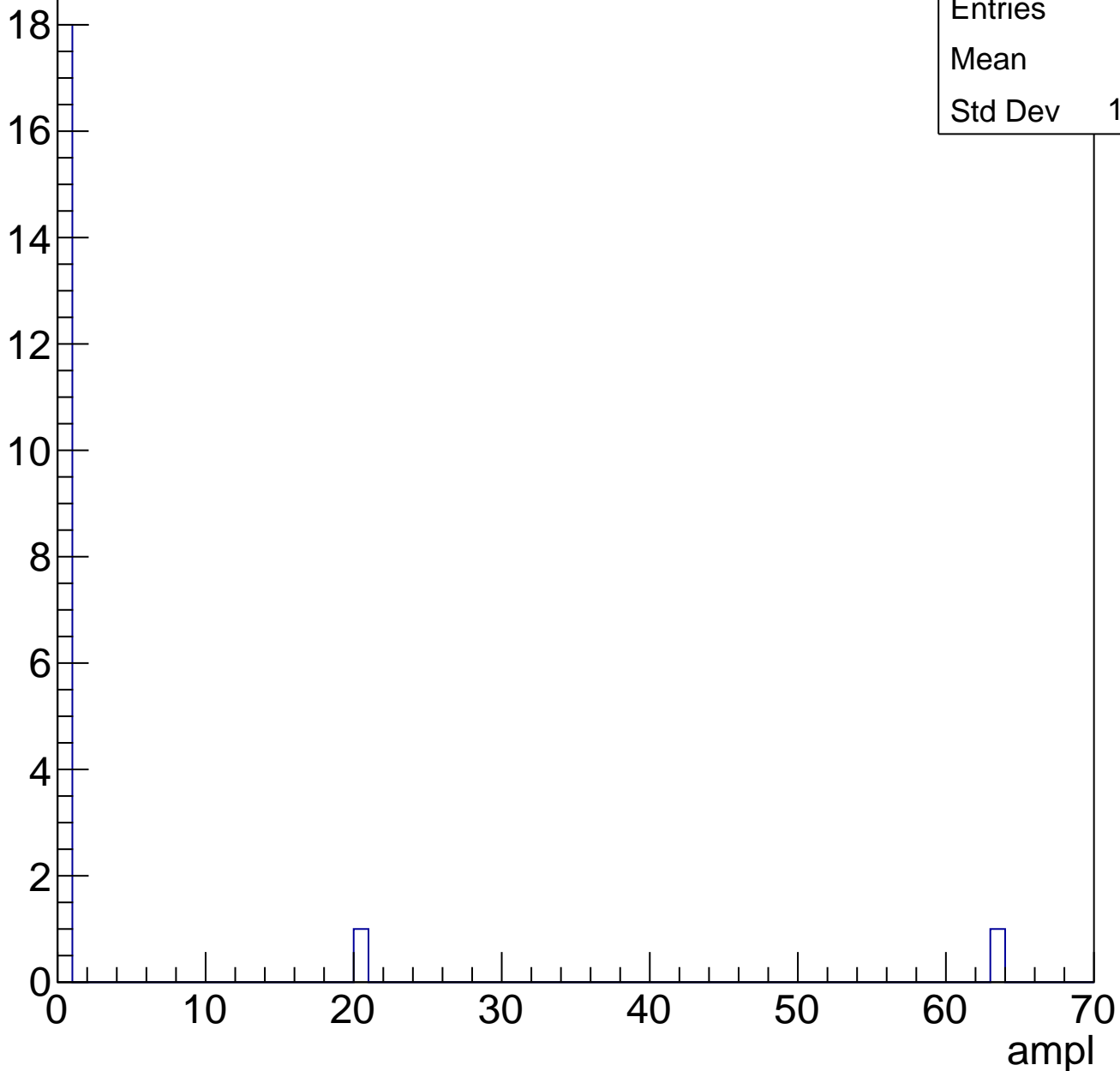




# B1L103S, U3-ch63, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	20
Mean	4.15
Std Dev	14.19

# B1L103S, U3-ch64, adc0

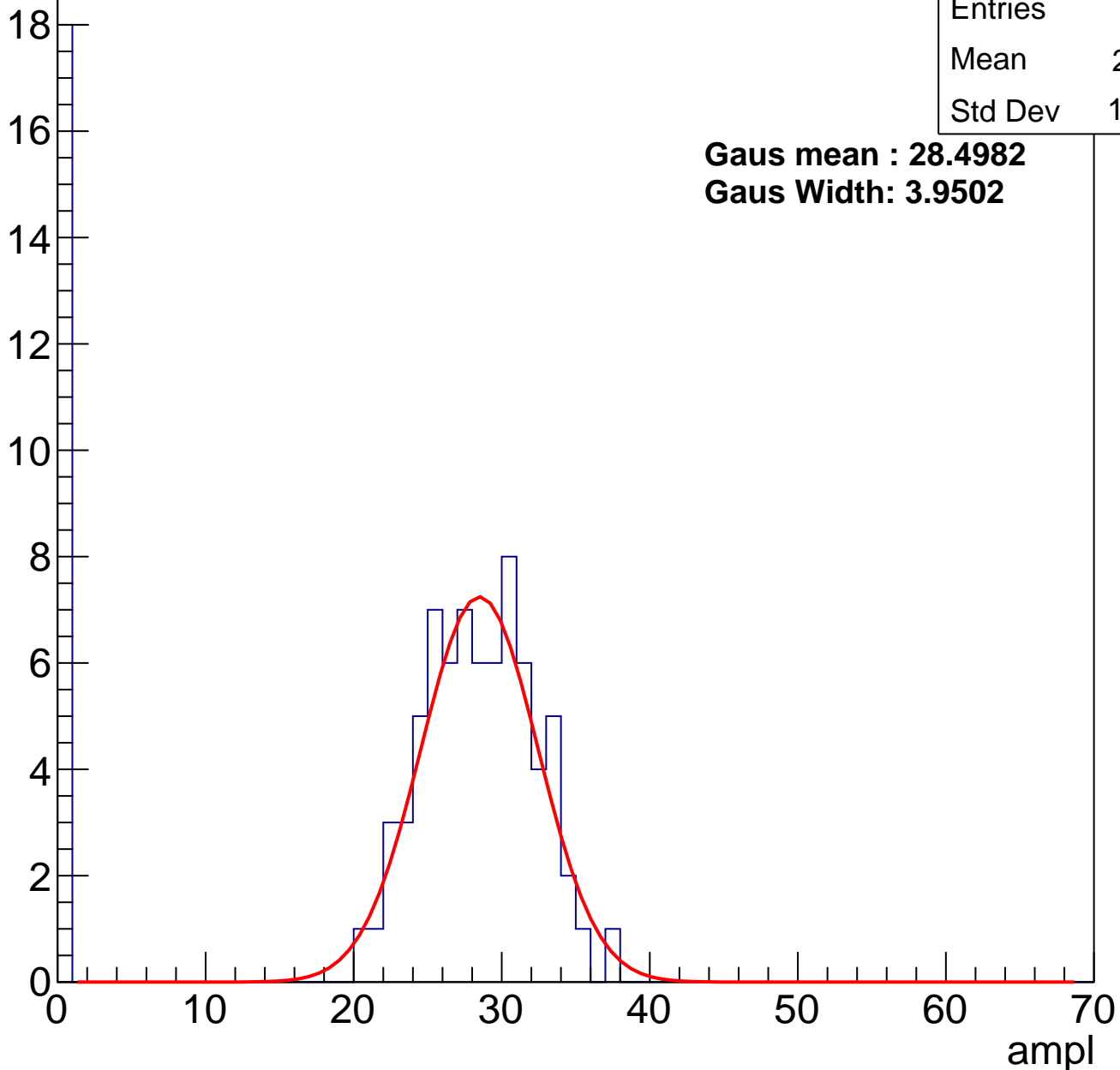
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	90
Mean	22.41
Std Dev	11.67

**Gaus mean : 28.4982**

**Gaus Width: 3.9502**

Entry



# B1L103S, U3-ch64, adc1

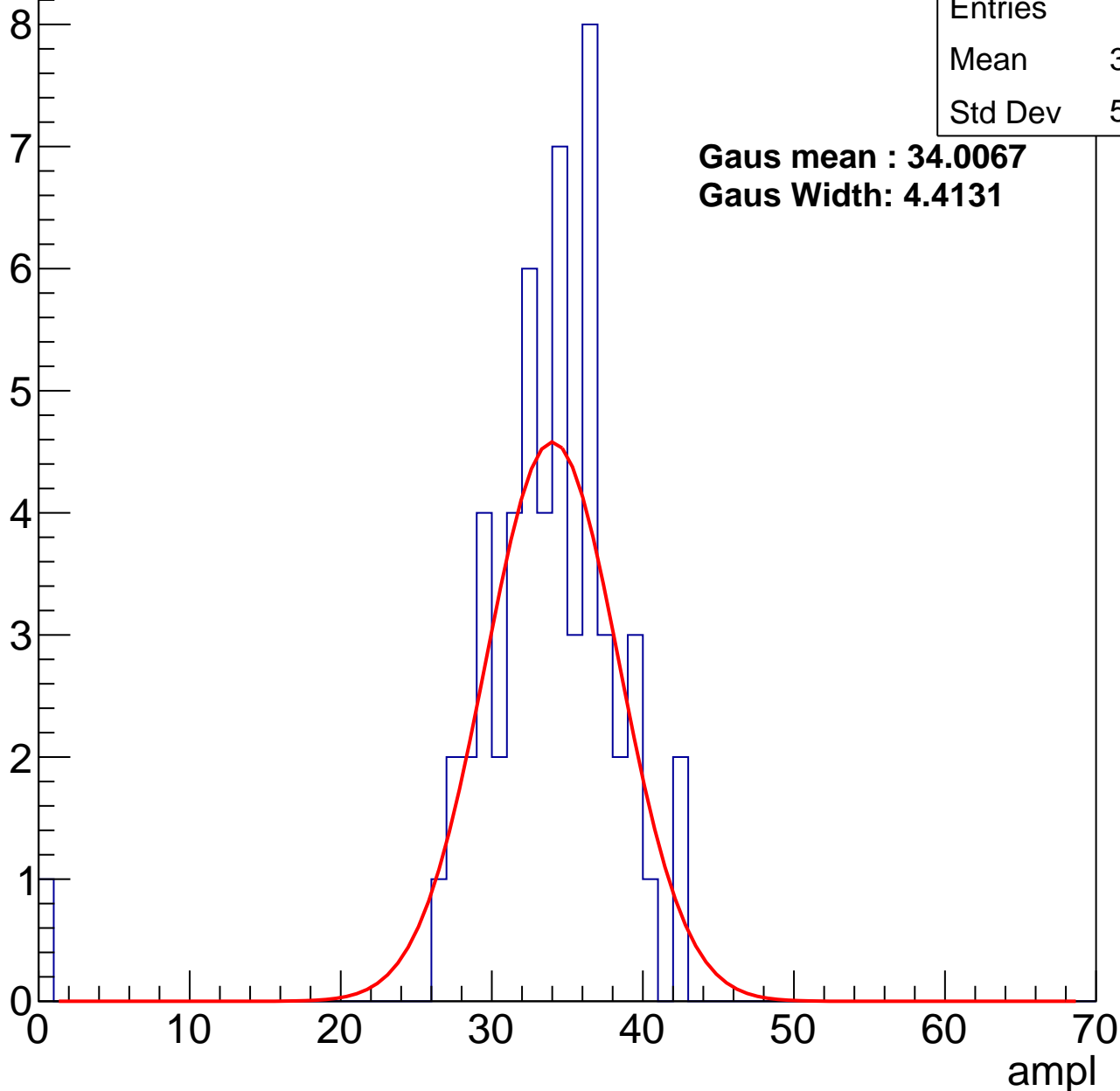
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	55
Mean	33.07
Std Dev	5.834

**Gaus mean : 34.0067**

**Gaus Width: 4.4131**



# B1L103S, U3-ch64, adc2

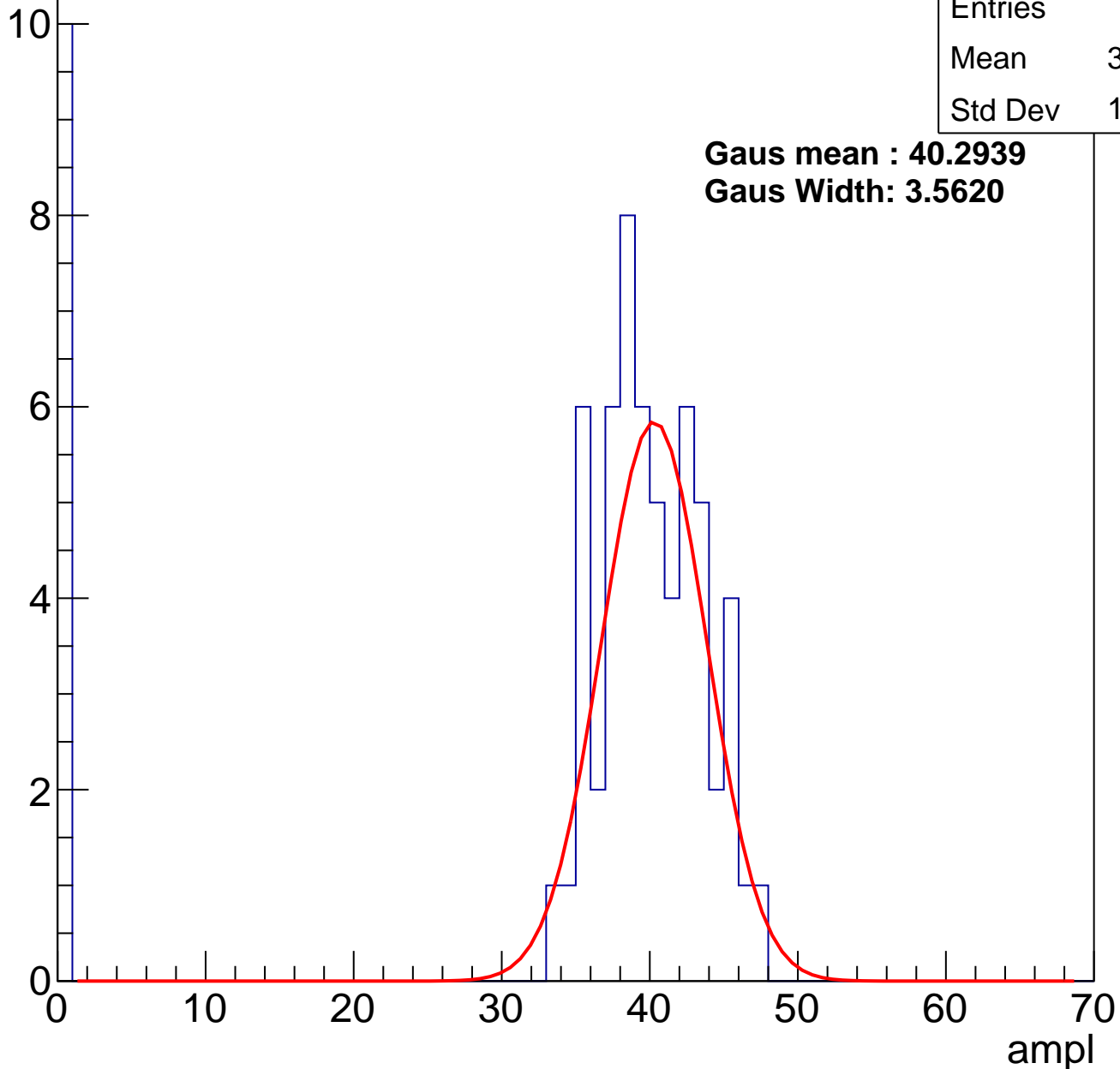
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	68
Mean	33.84
Std Dev	14.38

**Gaus mean : 40.2939**

**Gaus Width: 3.5620**

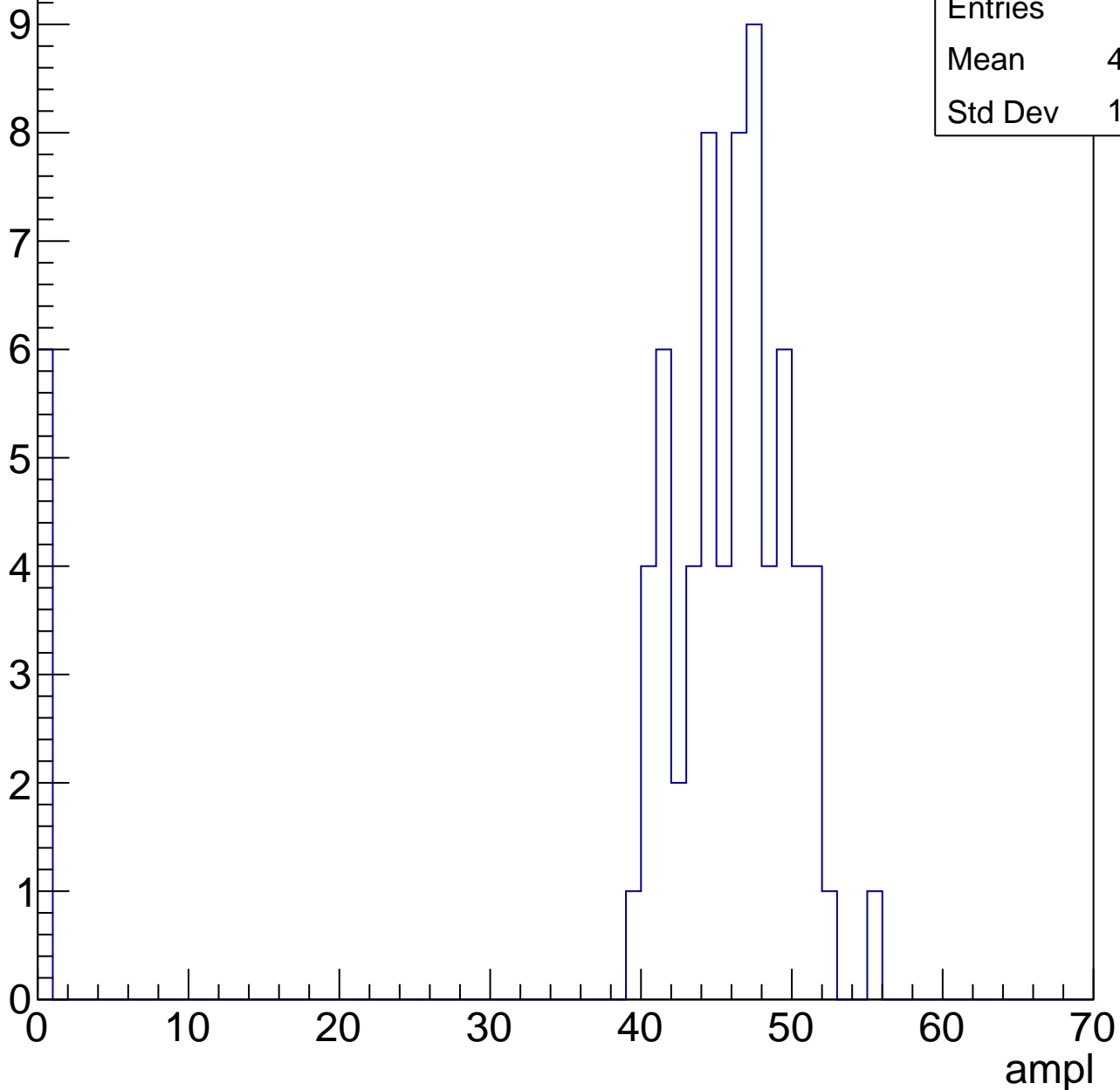
Entry



# B1L103S, U3-ch64, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

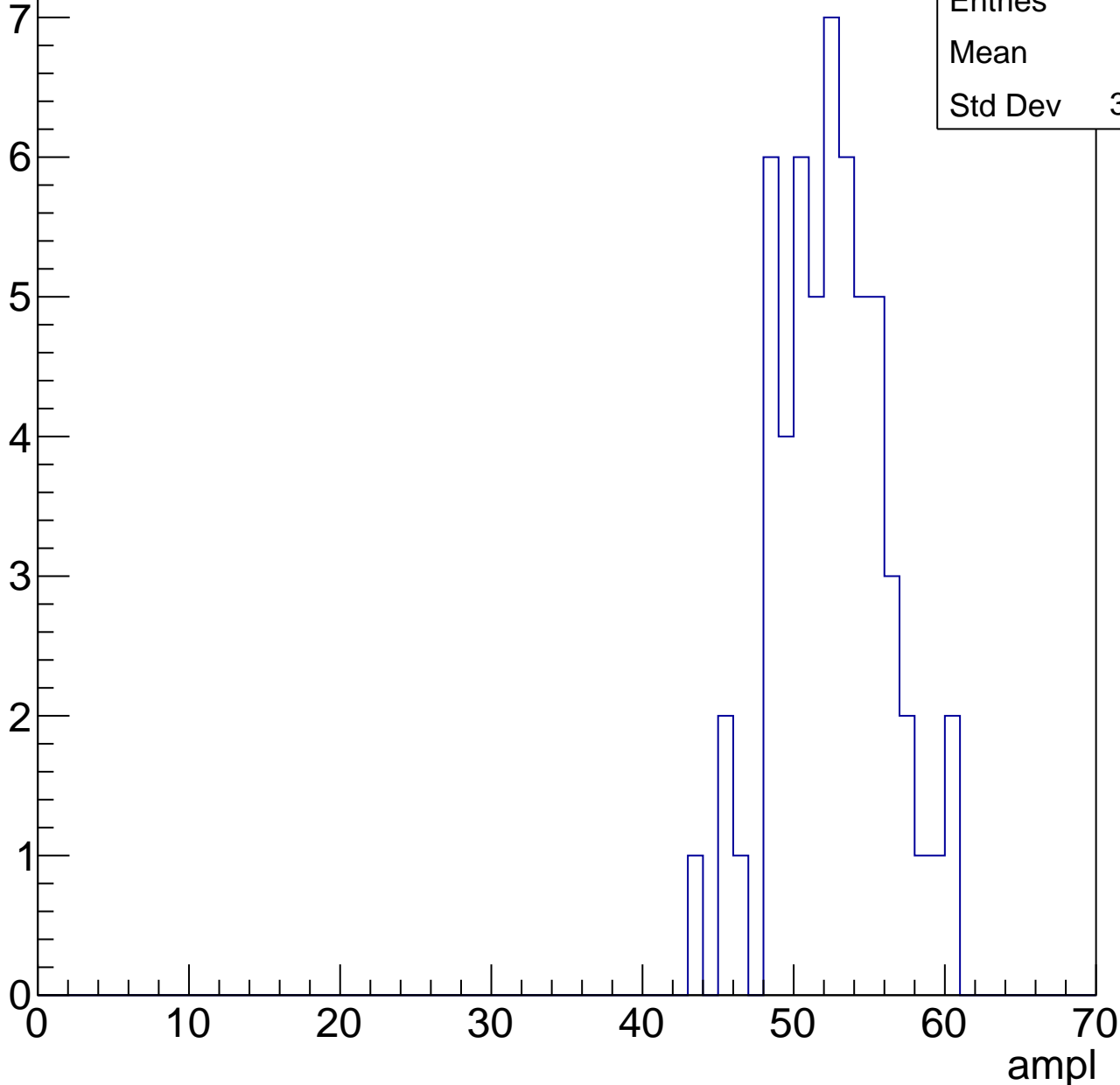


# B1L103S, U3-ch64, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	57
Mean	52
Std Dev	3.647

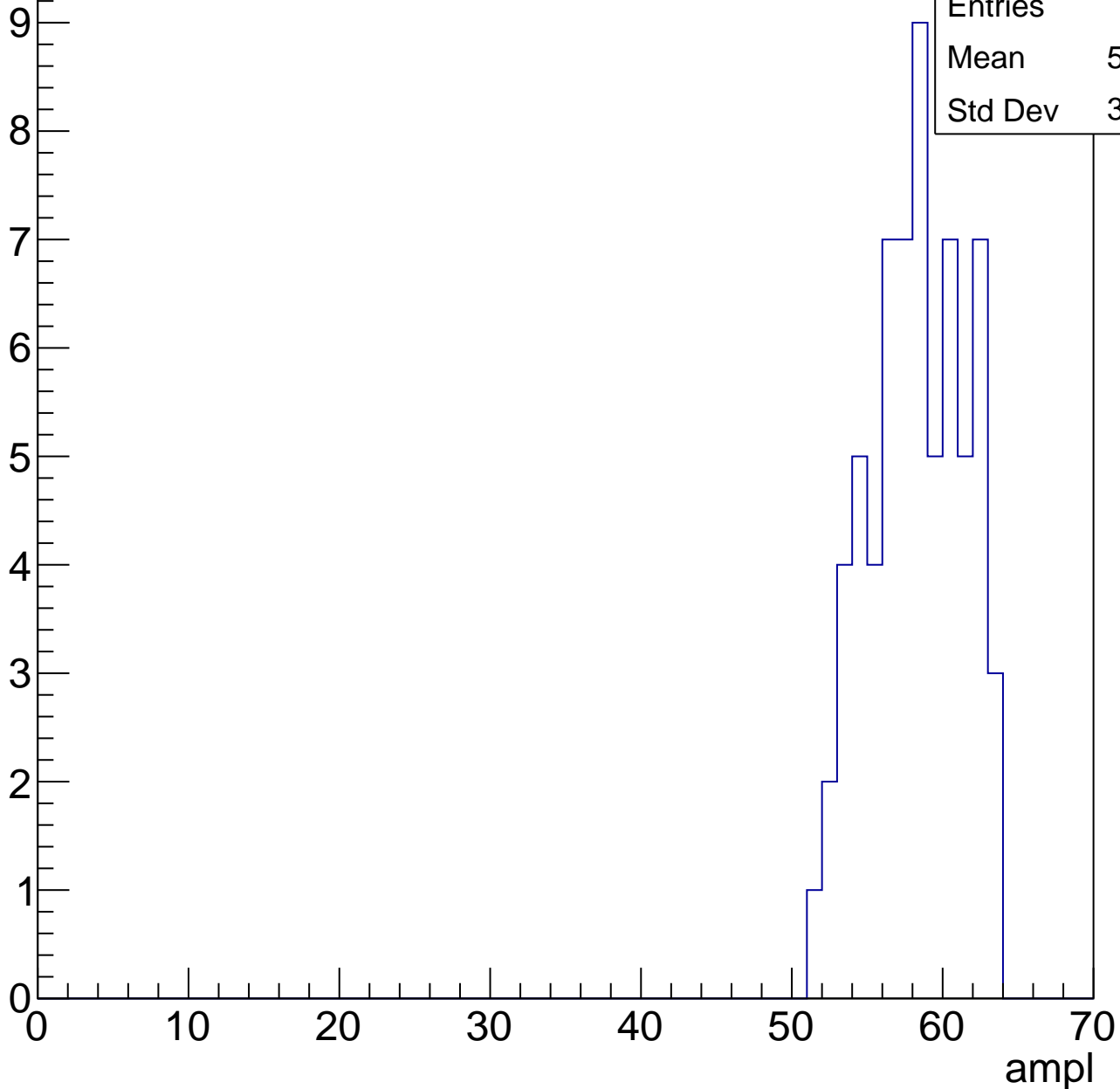


# B1L103S, U3-ch64, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	57.77
Std Dev	3.098

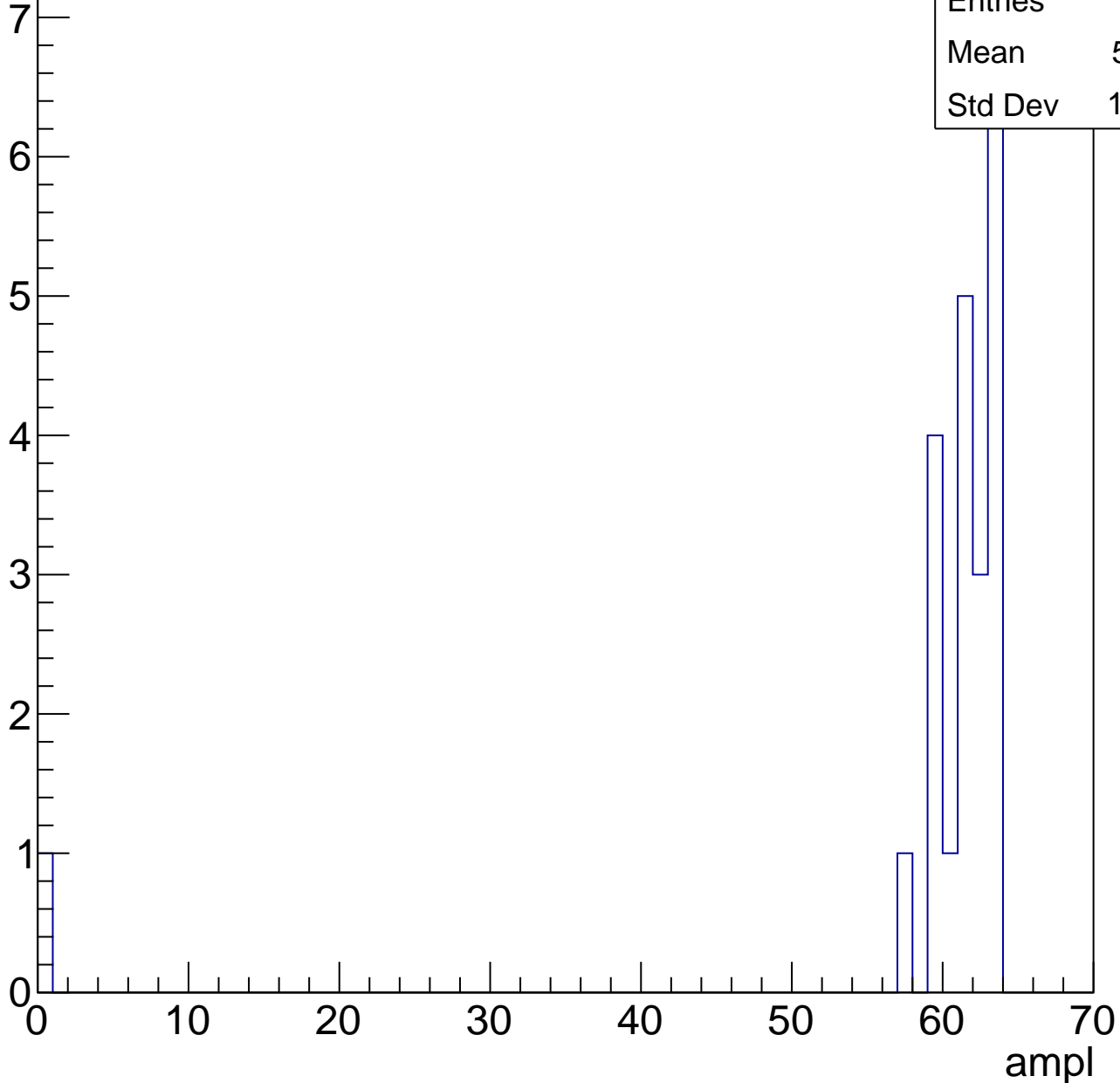


# B1L103S, U3-ch64, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	22
Mean	58.41
Std Dev	12.86





# B1L103S, U3-ch64, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	1.053
Std Dev	4.466

Entry



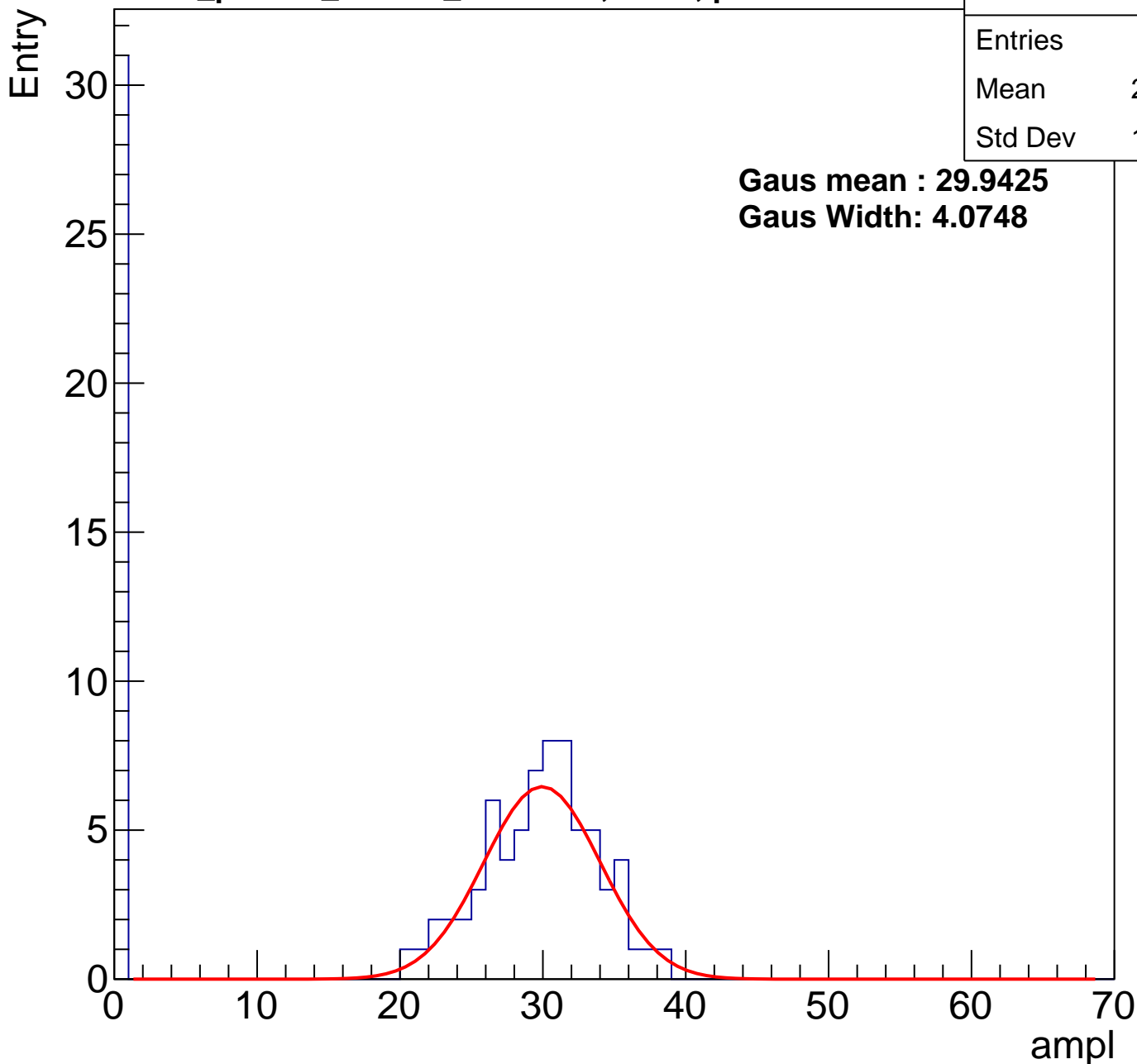
# B1L103S, U3-ch65, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	100
Mean	20.27
Std Dev	13.97

**Gaus mean : 29.9425**

**Gaus Width: 4.0748**



# B1L103S, U3-ch65, adc1

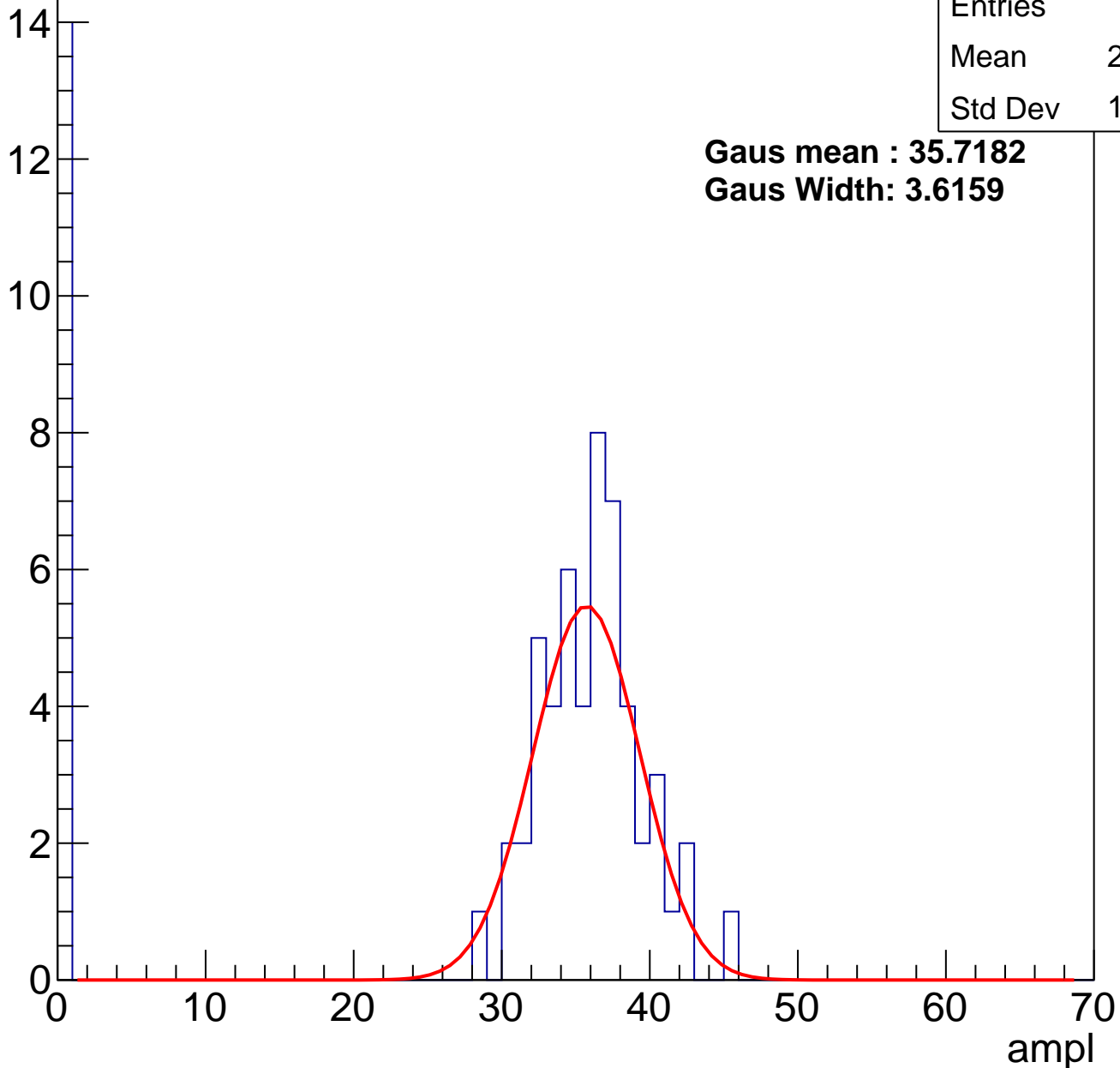
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	66
Mean	28.08
Std Dev	14.87

**Gaus mean : 35.7182**

**Gaus Width: 3.6159**

Entry



# B1L103S, U3-ch65, adc2

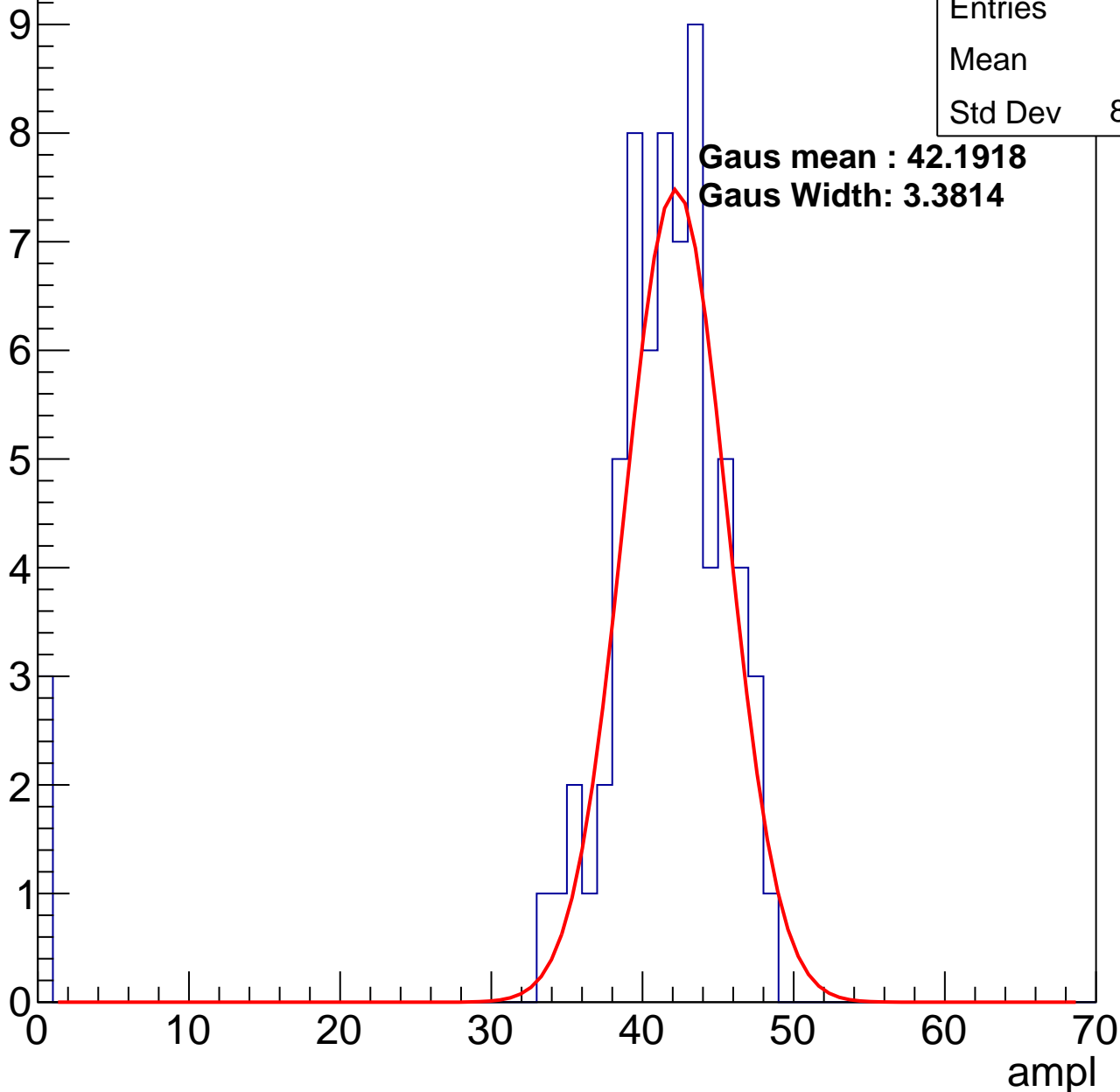
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	39.6
Std Dev	8.982

**Gaus mean : 42.1918**

**Gaus Width: 3.3814**

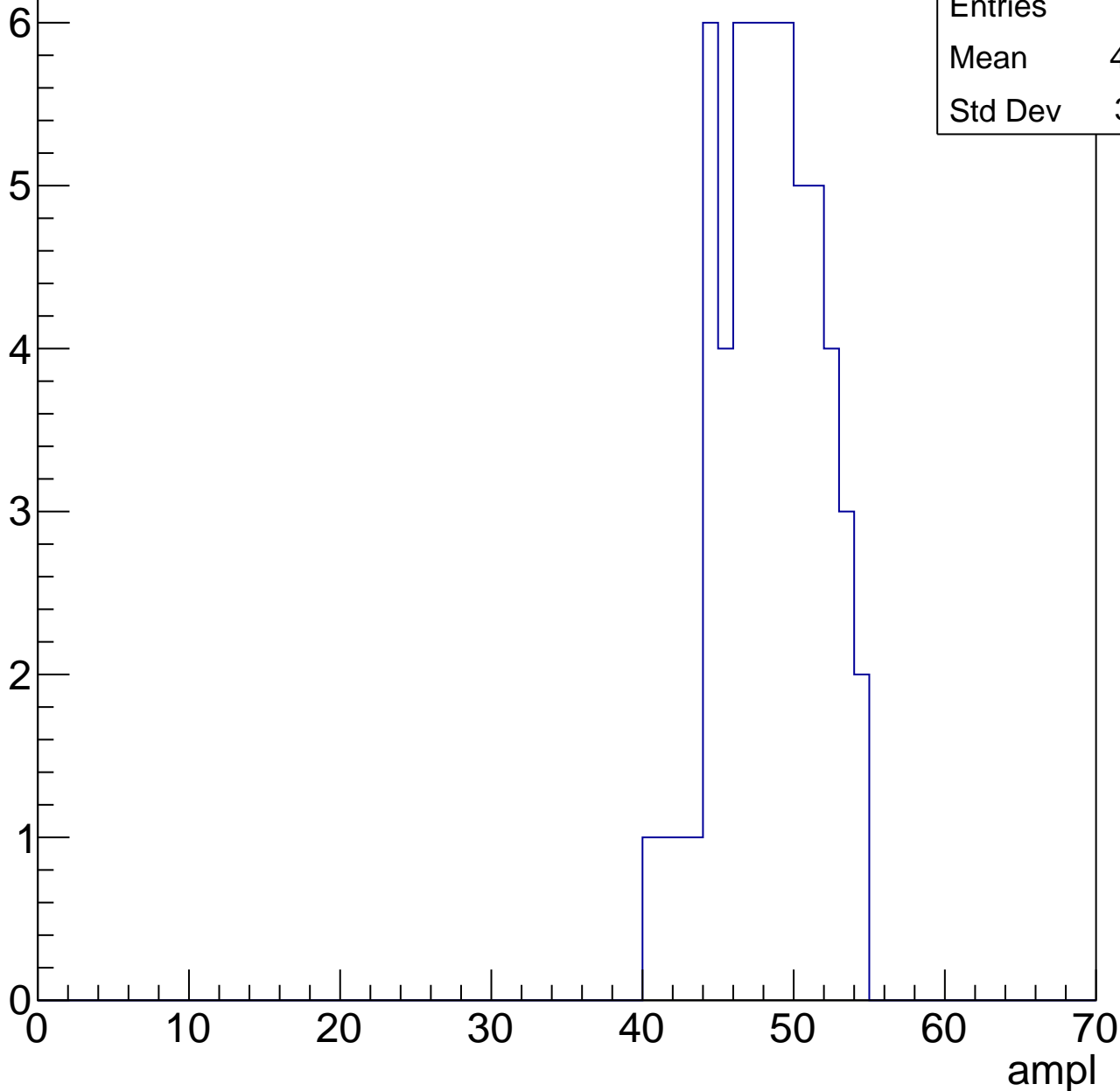


# B1L103S, U3-ch65, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	57
Mean	47.89
Std Dev	3.291

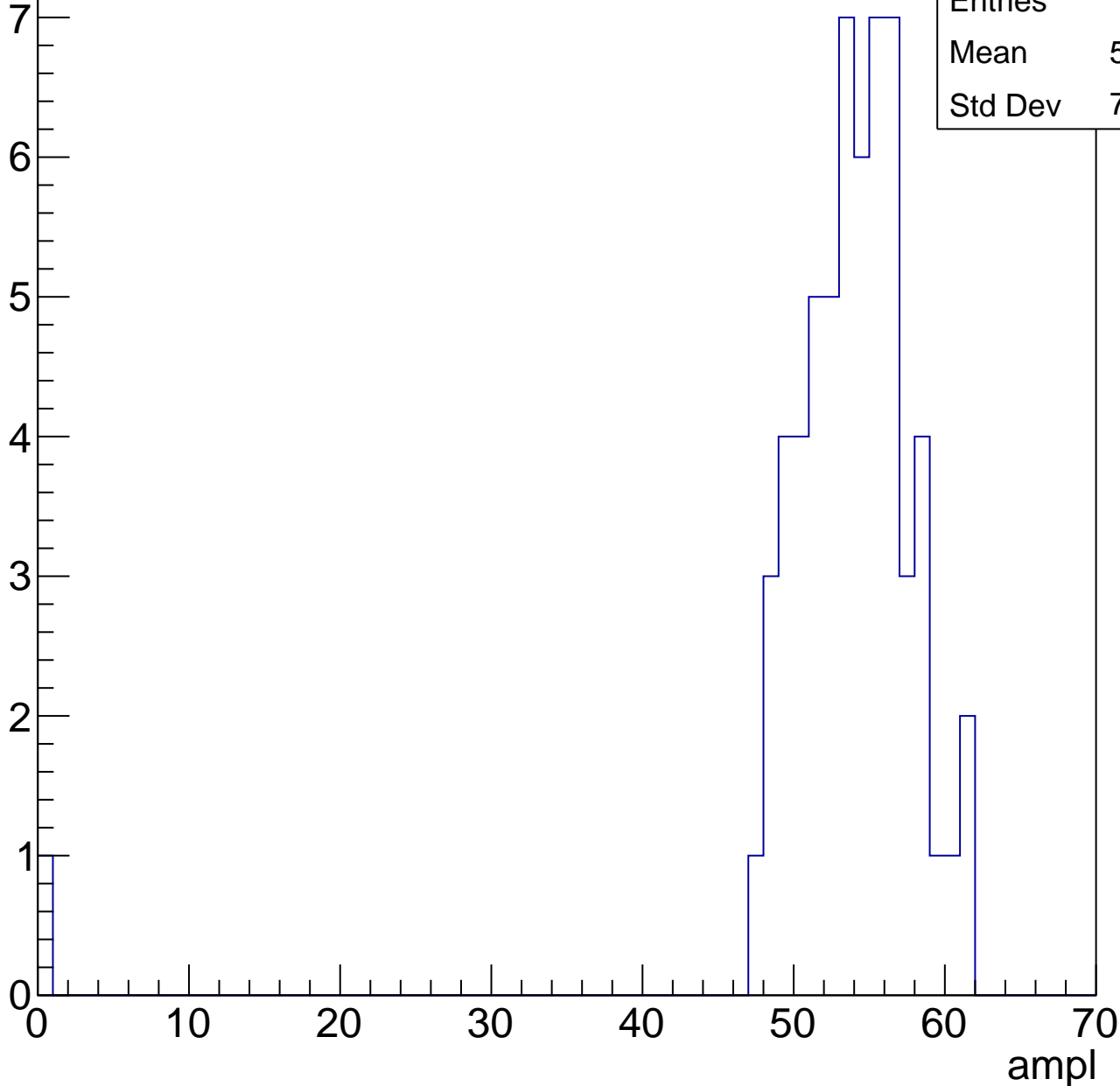


# B1L103S, U3-ch65, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

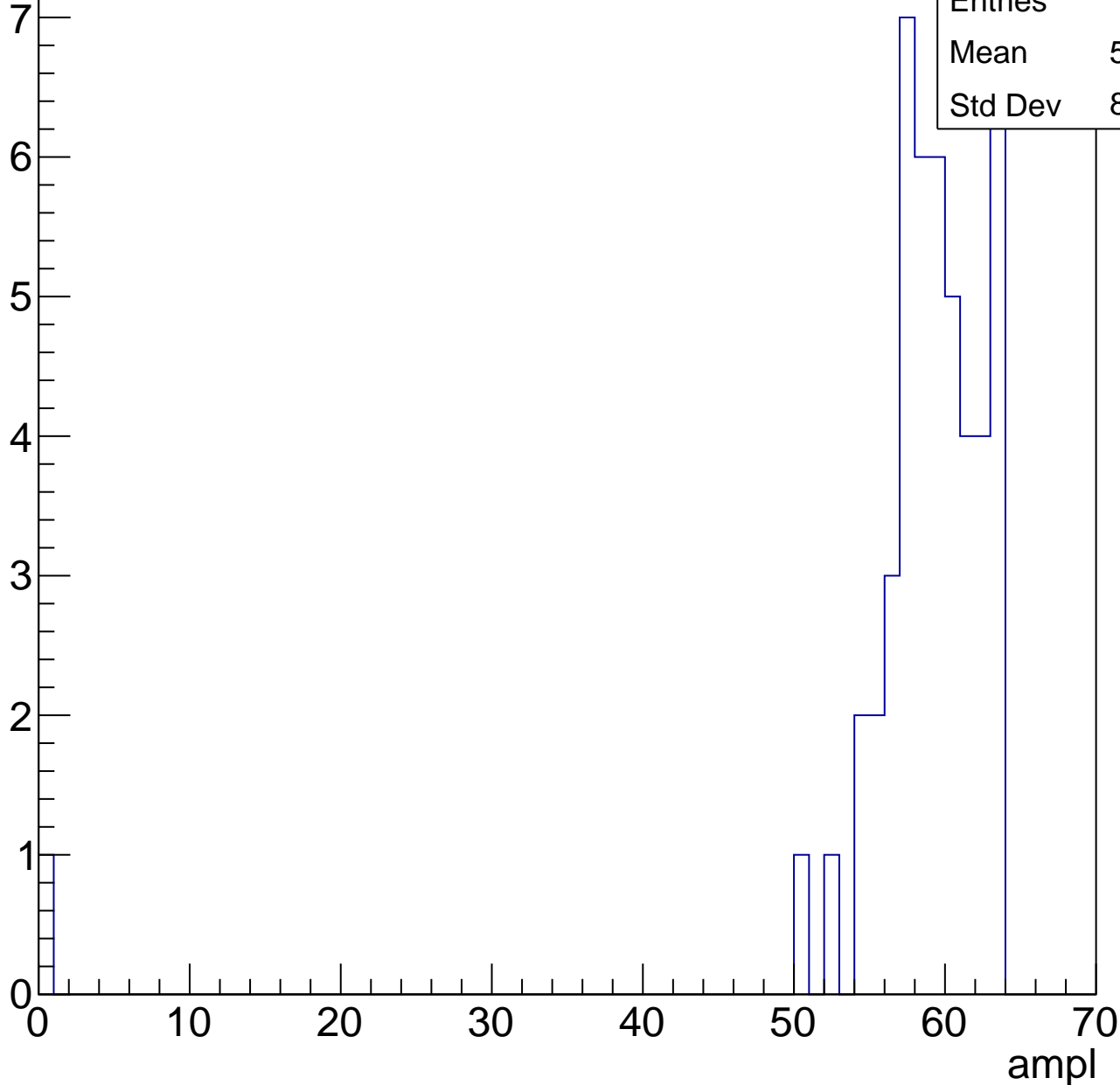
Entries	61
Mean	52.75
Std Dev	7.574



# B1L103S, U3-ch65, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

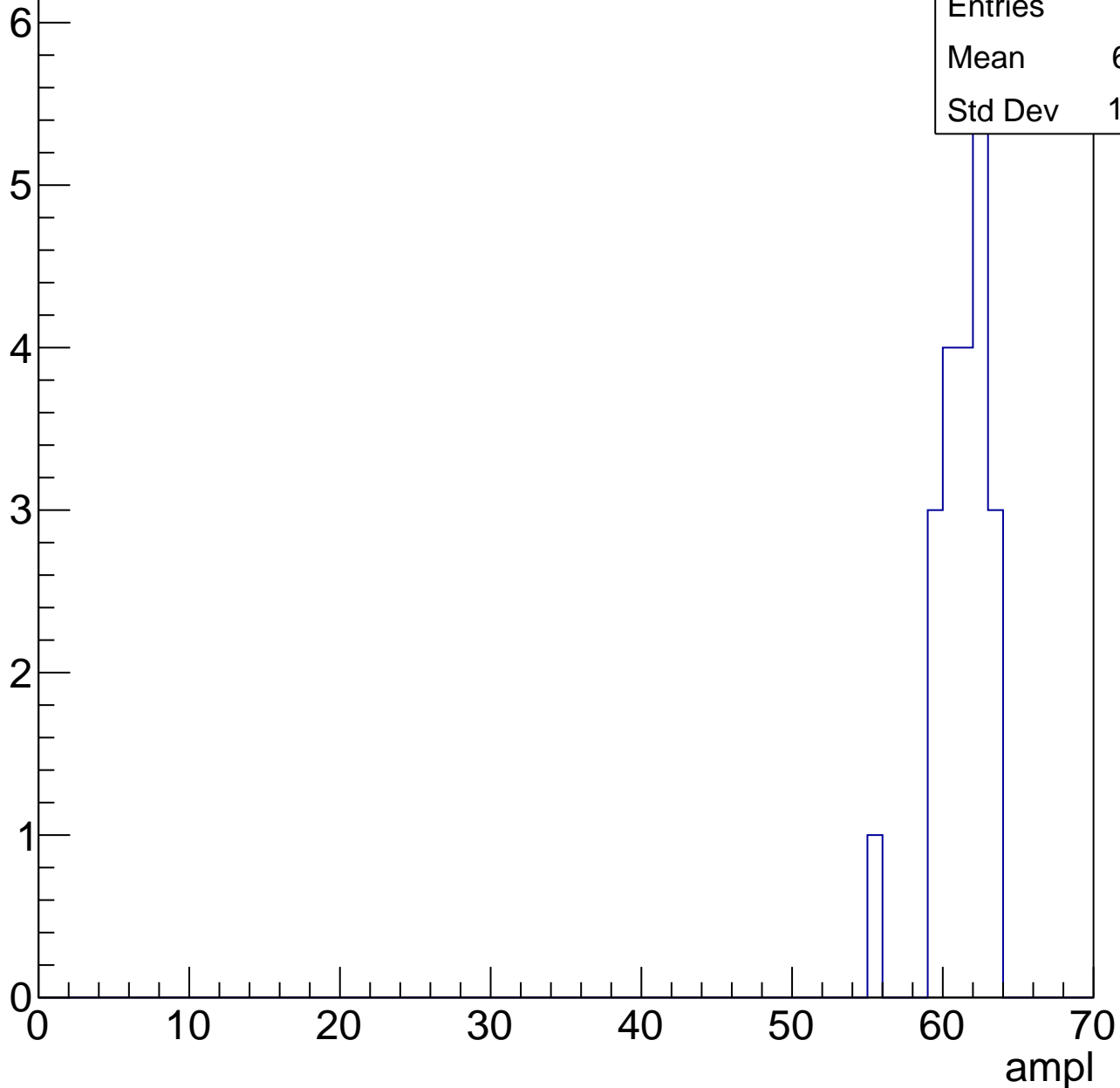


# B1L103S, U3-ch65, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	21
Mean	60.81
Std Dev	1.816





# B1L103S, U3-ch65, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



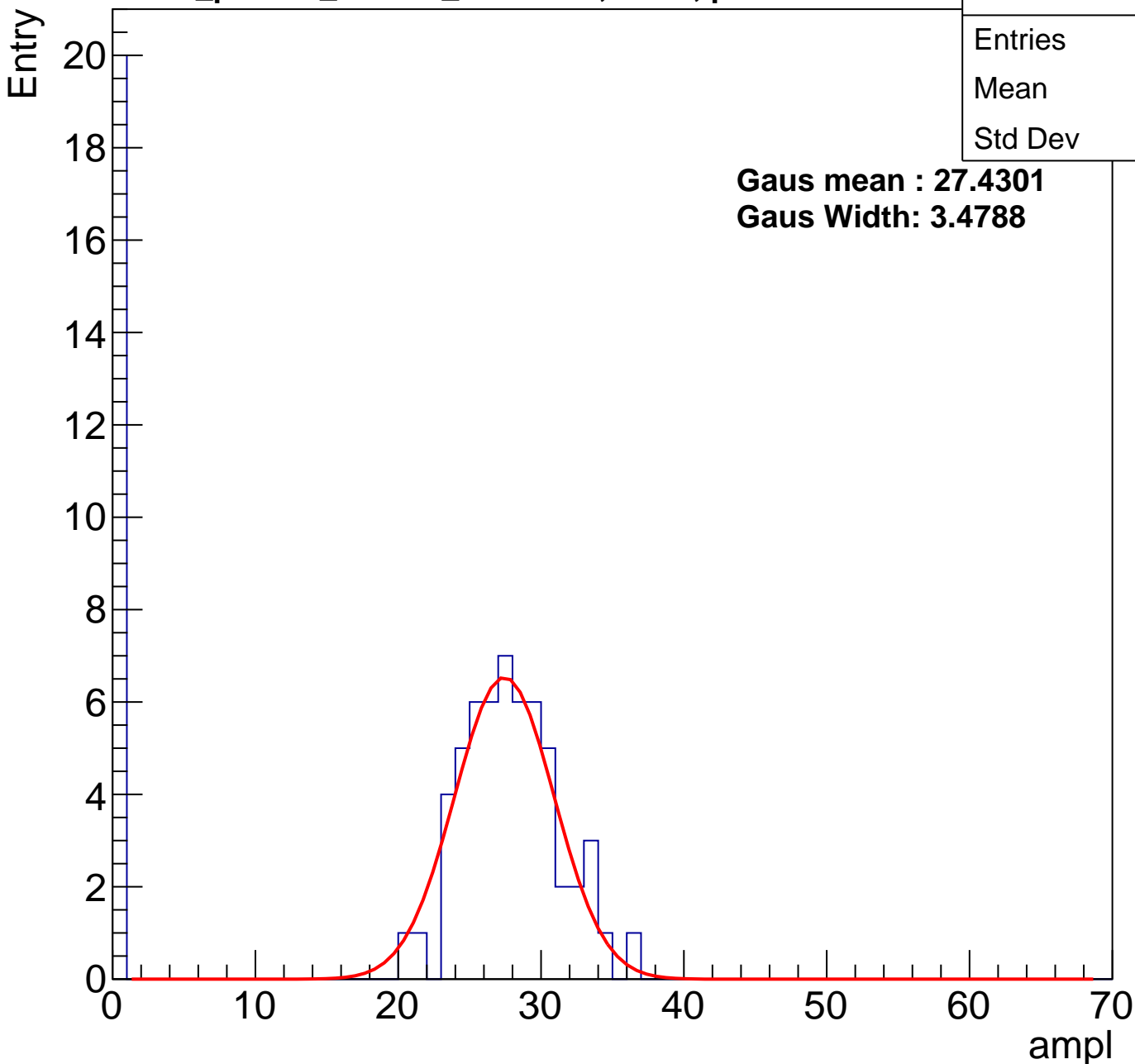
# B1L103S, U3-ch66, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	76
Mean	20.2
Std Dev	12.4

**Gaus mean : 27.4301**

**Gaus Width: 3.4788**



# B1L103S, U3-ch66, adc1

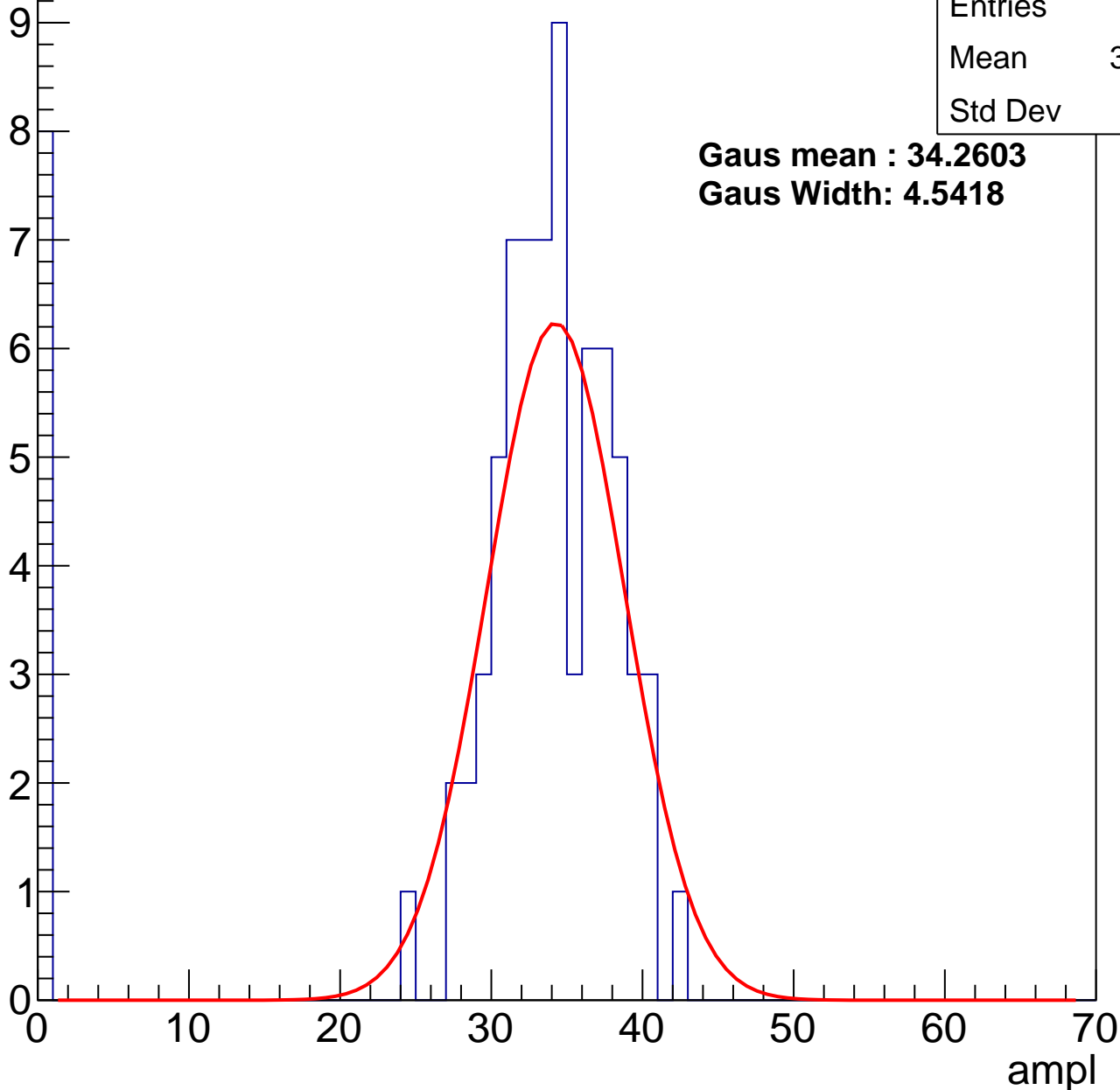
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	78
Mean	30.27
Std Dev	10.8

**Gaus mean : 34.2603**

**Gaus Width: 4.5418**



# B1L103S, U3-ch66, adc2

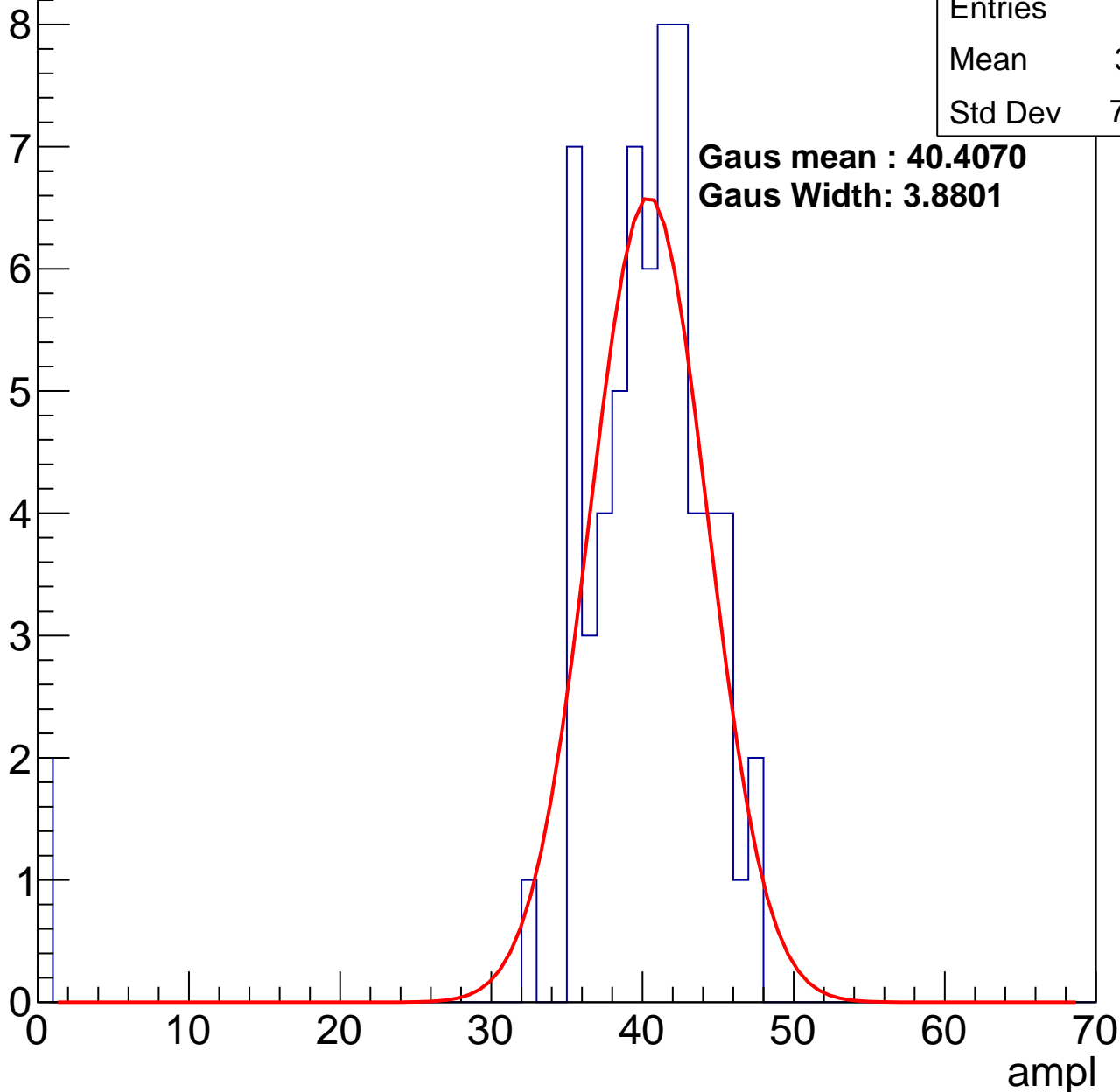
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	38.91
Std Dev	7.633

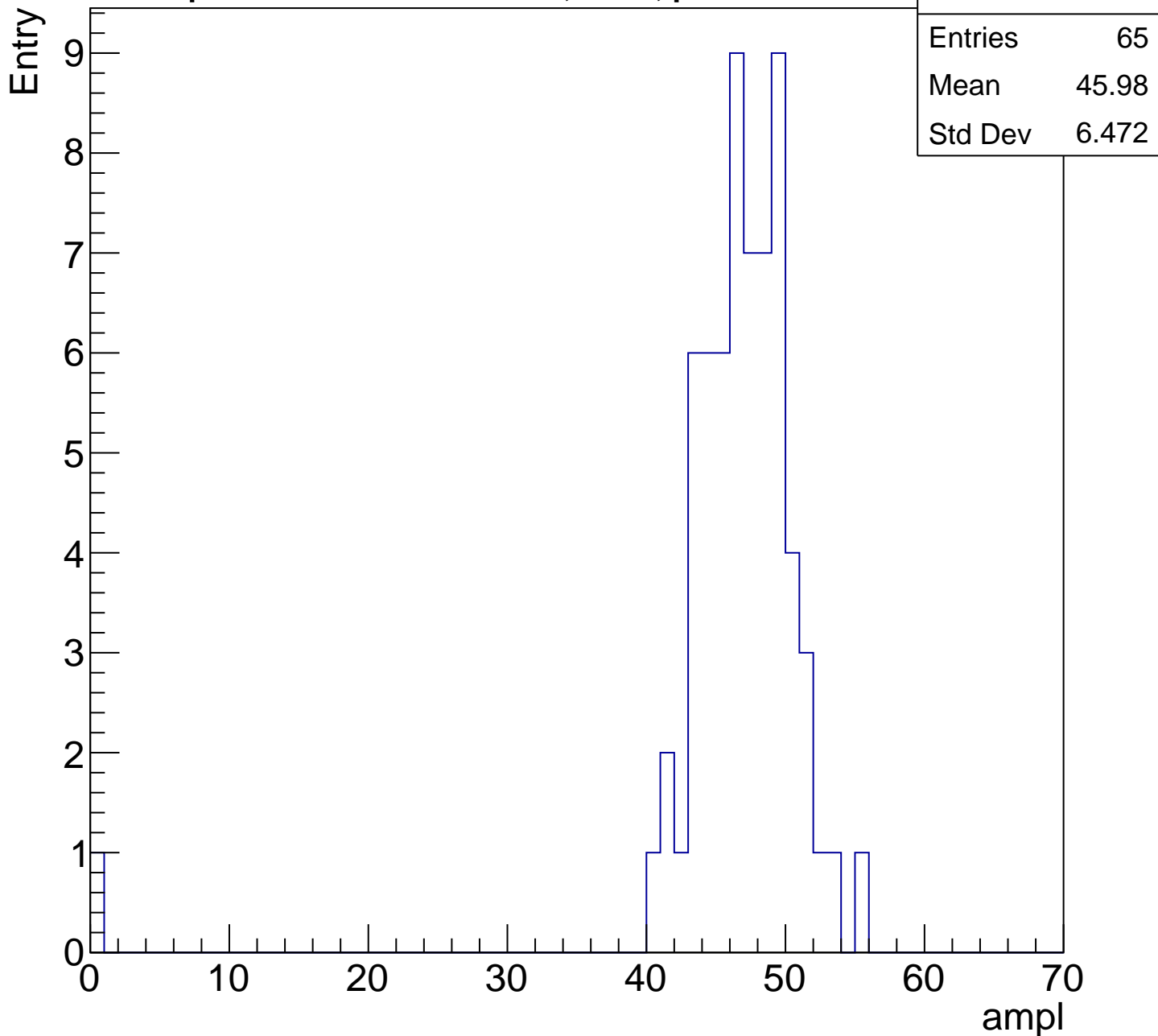
**Gaus mean : 40.4070**

**Gaus Width: 3.8801**



# B1L103S, U3-ch66, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

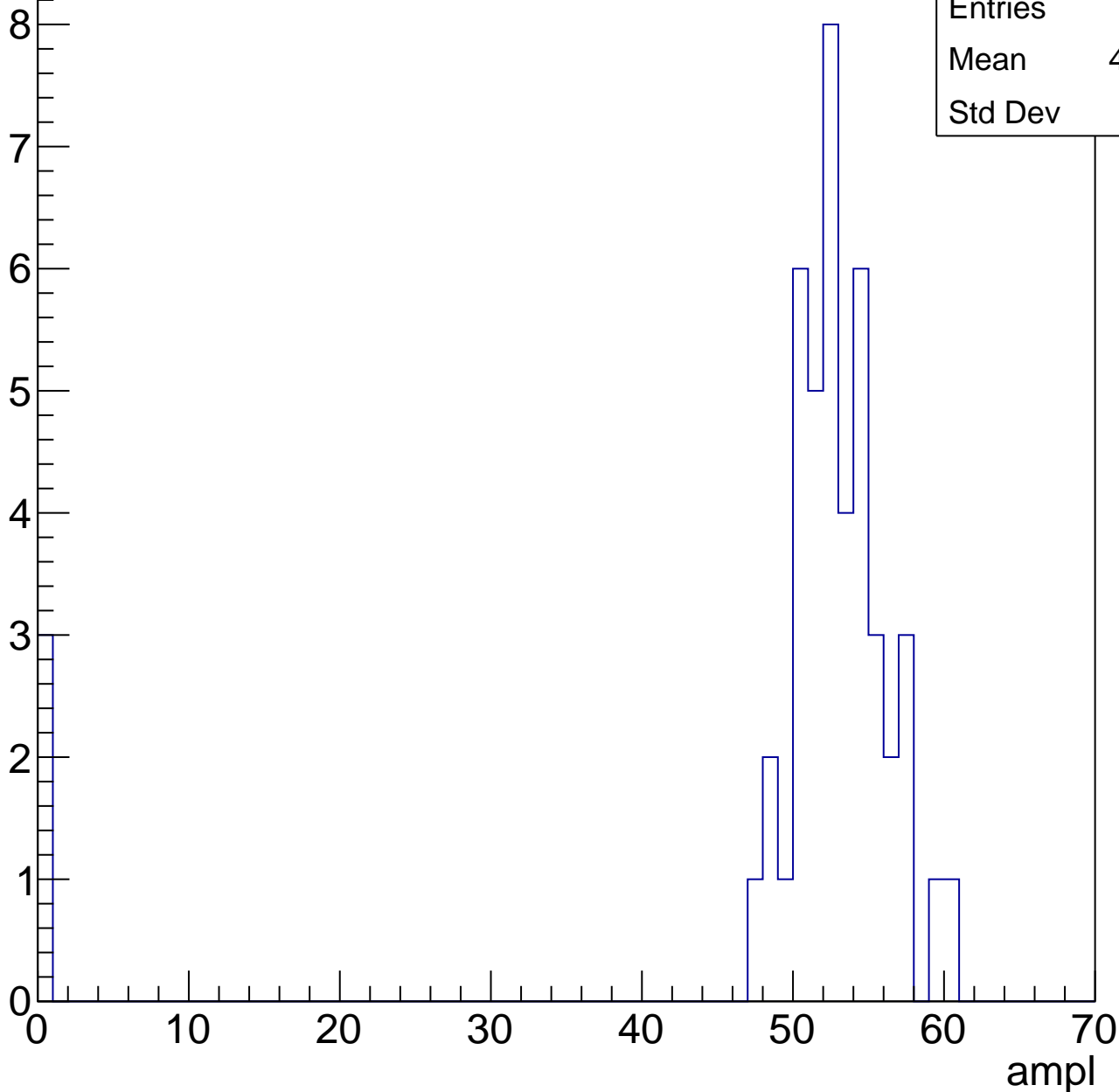


# B1L103S, U3-ch66, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	46
Mean	49.26
Std Dev	13.3



# B1L103S, U3-ch66, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

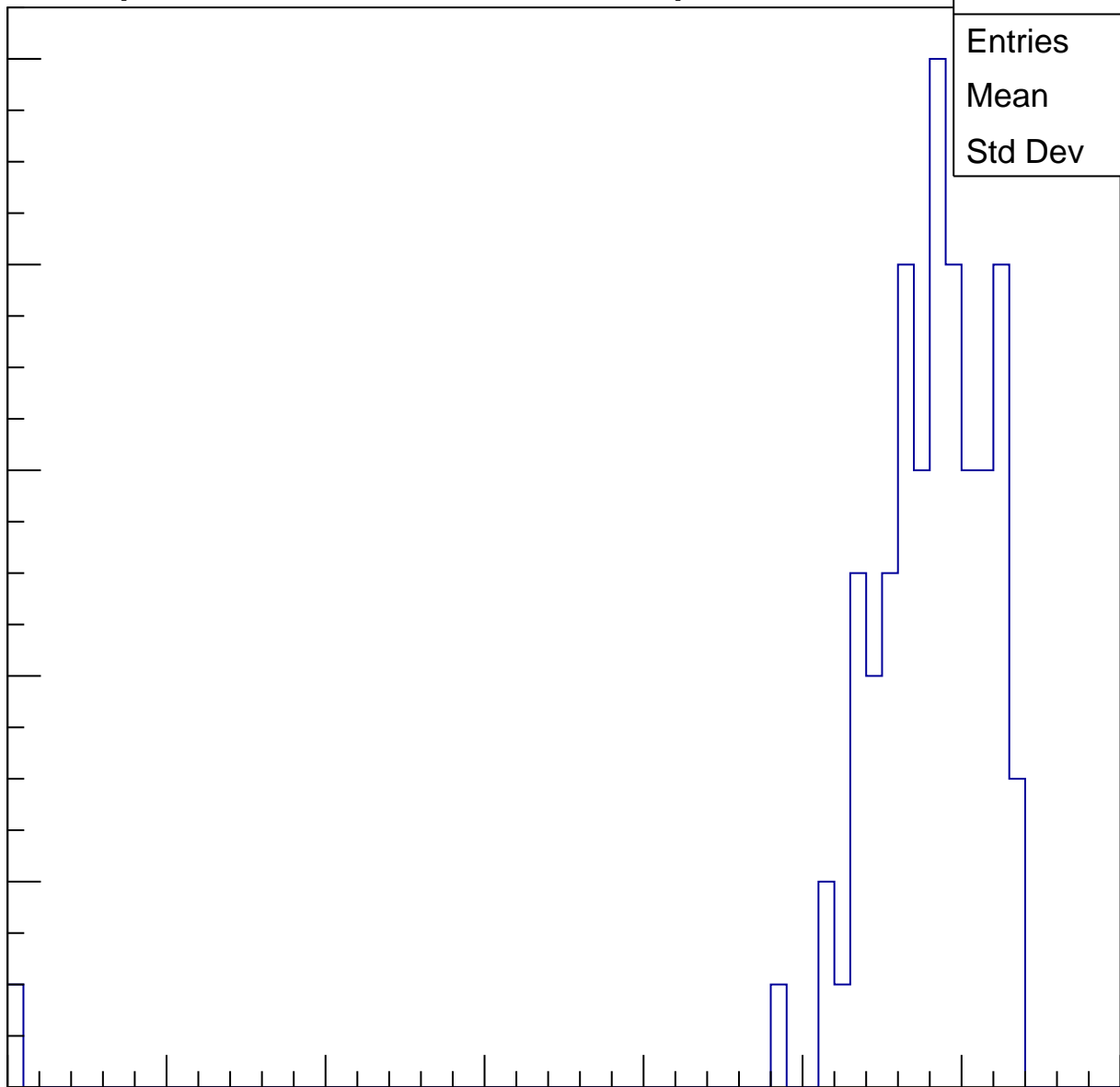
Entries	74
Mean	56.91
Std Dev	7.417

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

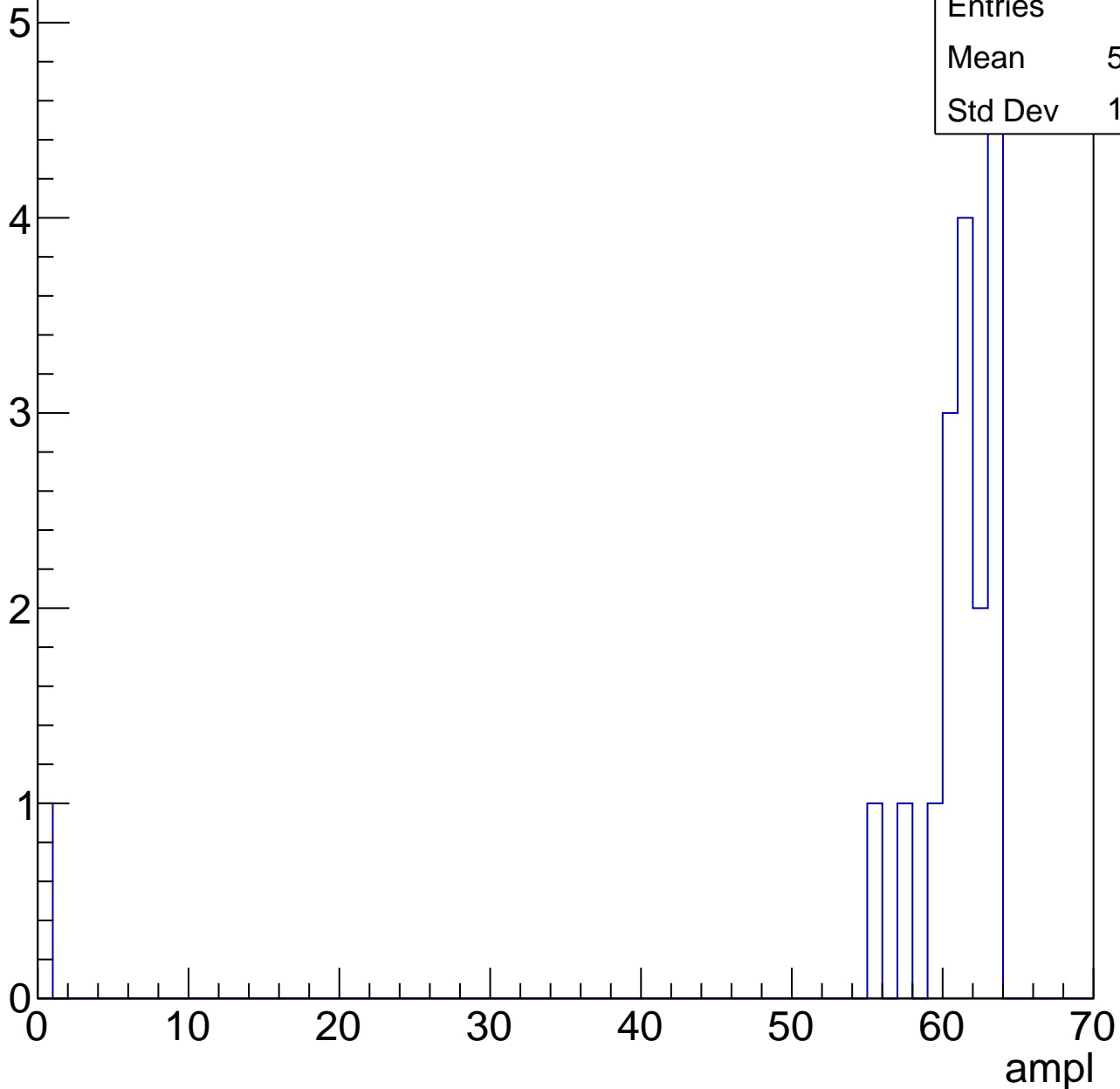


# B1L103S, U3-ch66, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	18
Mean	57.44
Std Dev	14.09





# B1L103S, U3-ch66, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U3-ch67, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	75
Mean	23.57
Std Dev	11.09

**Gaus mean : 28.8971**

**Gaus Width: 2.8182**

Entry

12

10

8

6

4

2

0

0

10

20

30

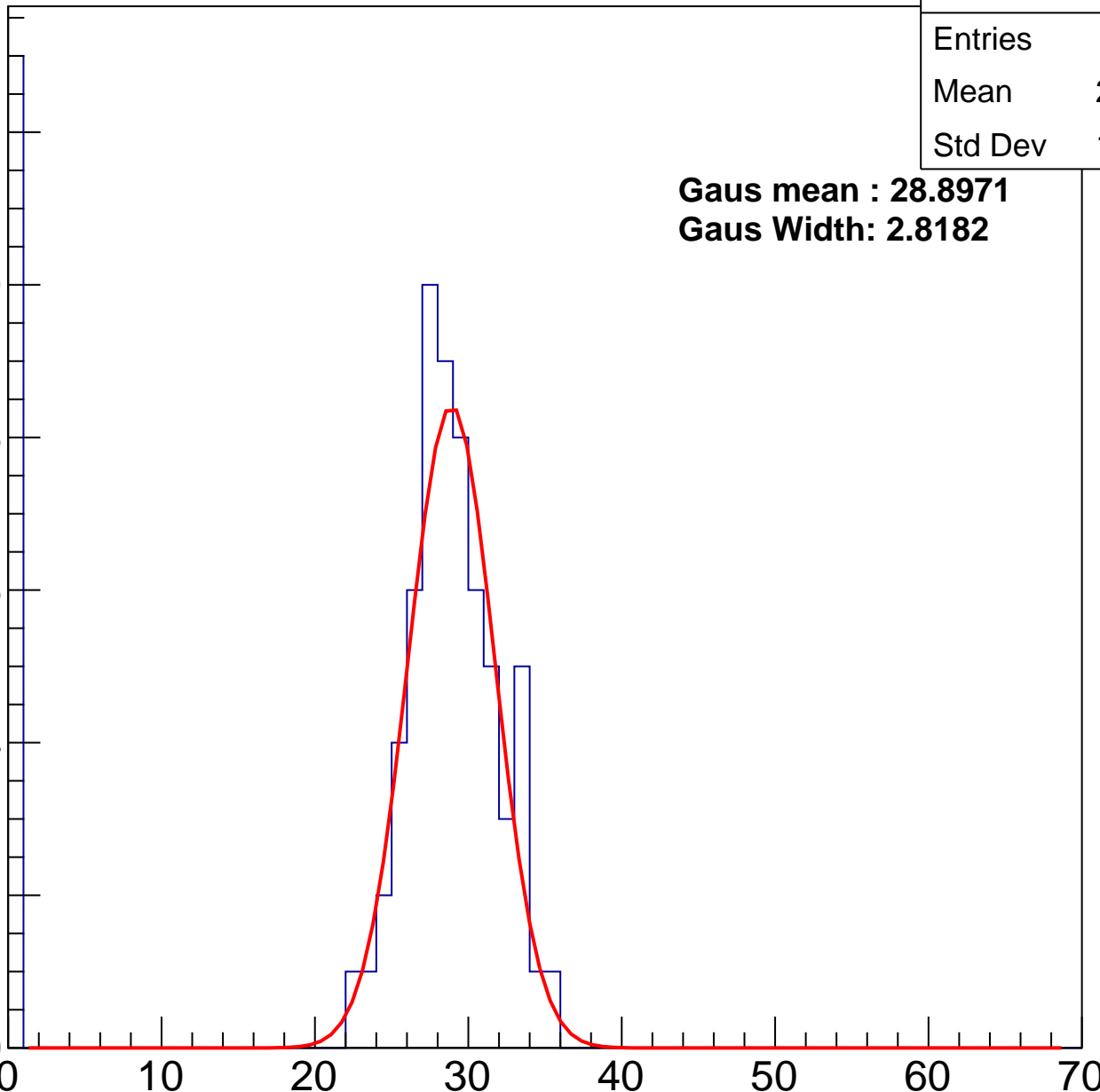
40

50

60

70

ampl



# B1L103S, U3-ch67, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	96
Mean	34.24
Std Dev	8.764

**Gaus mean : 36.7793**

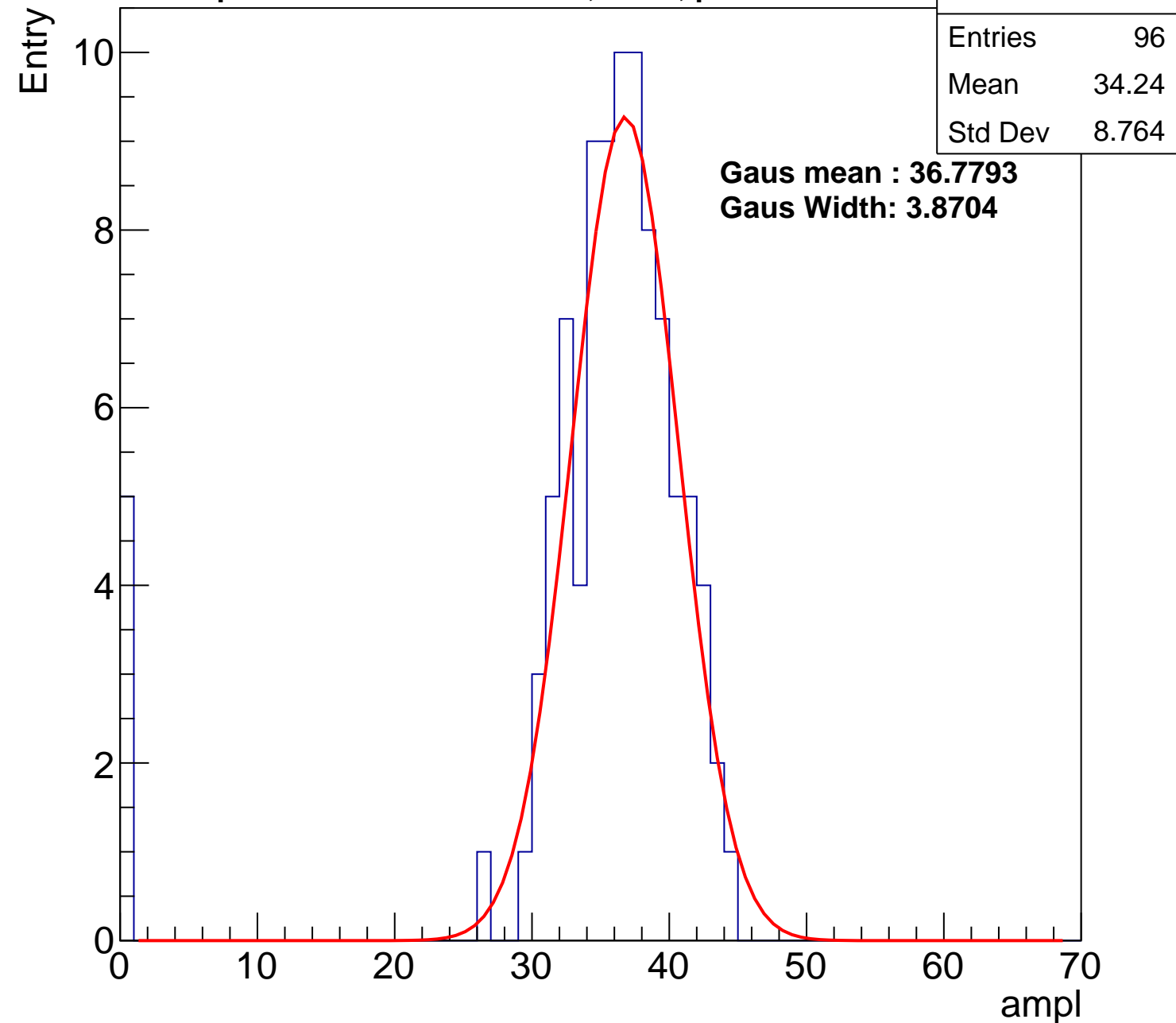
**Gaus Width: 3.8704**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch67, adc2

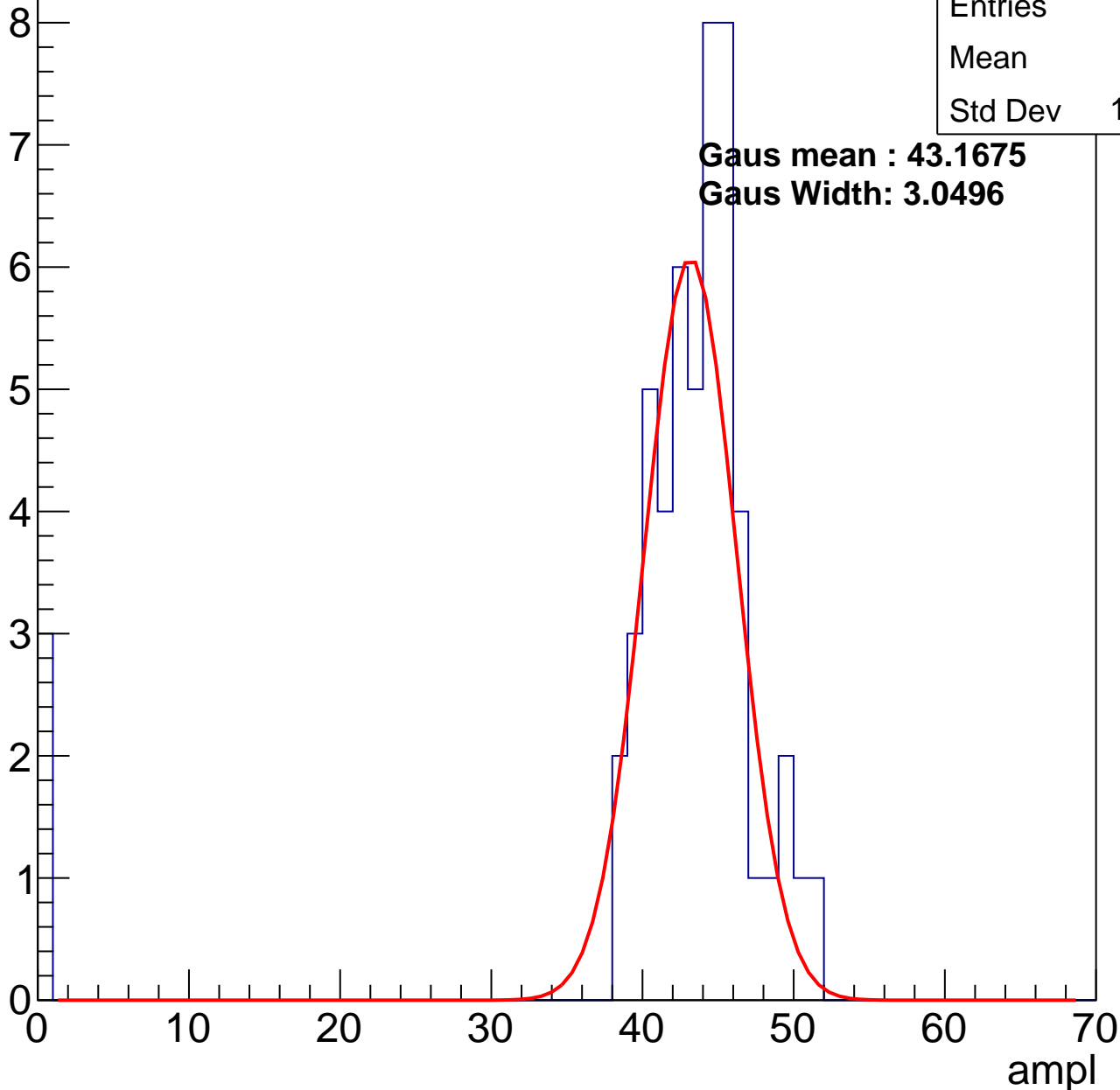
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	54
Mean	41
Std Dev	10.36

**Gaus mean : 43.1675**

**Gaus Width: 3.0496**

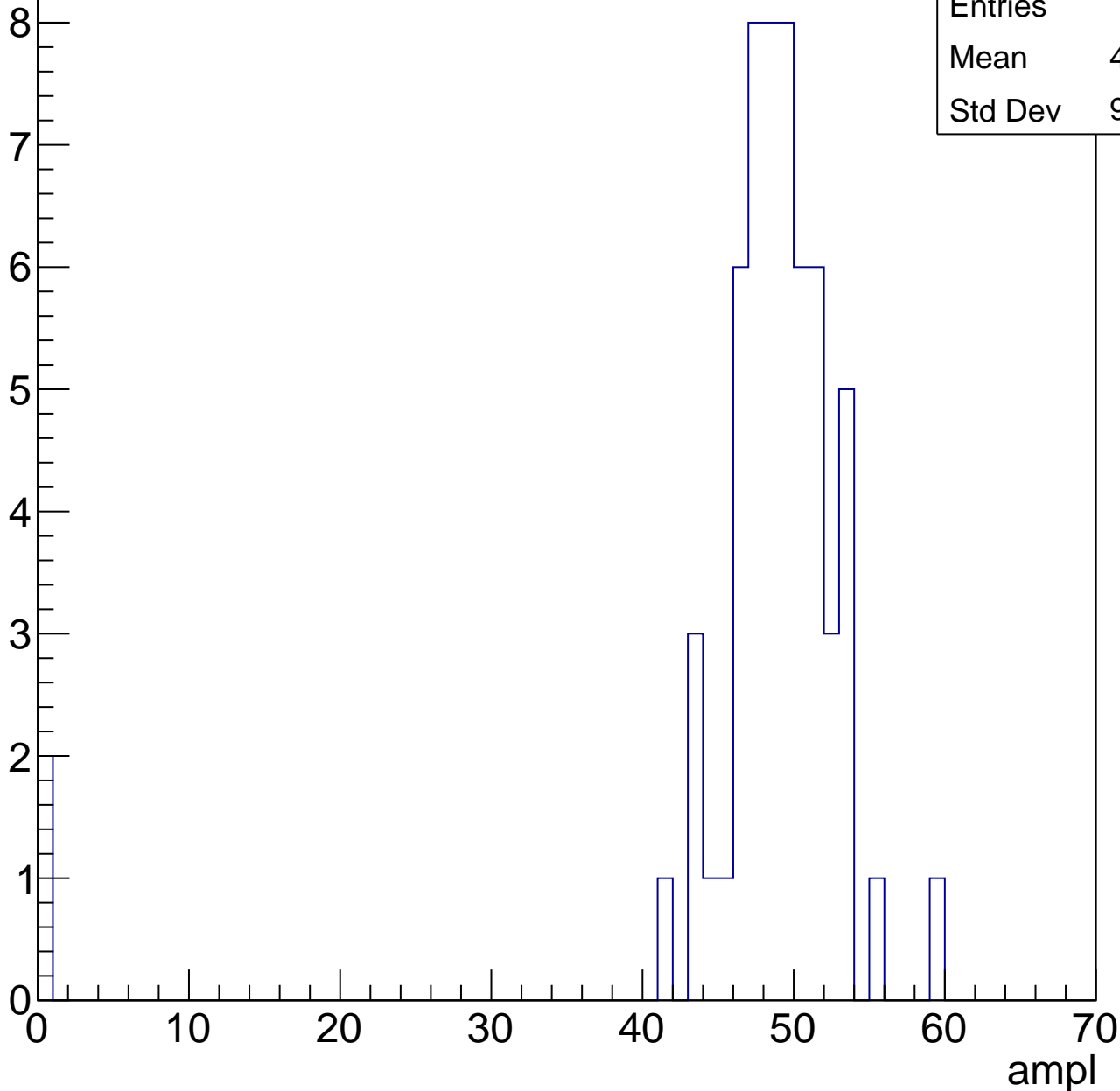


# B1L103S, U3-ch67, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

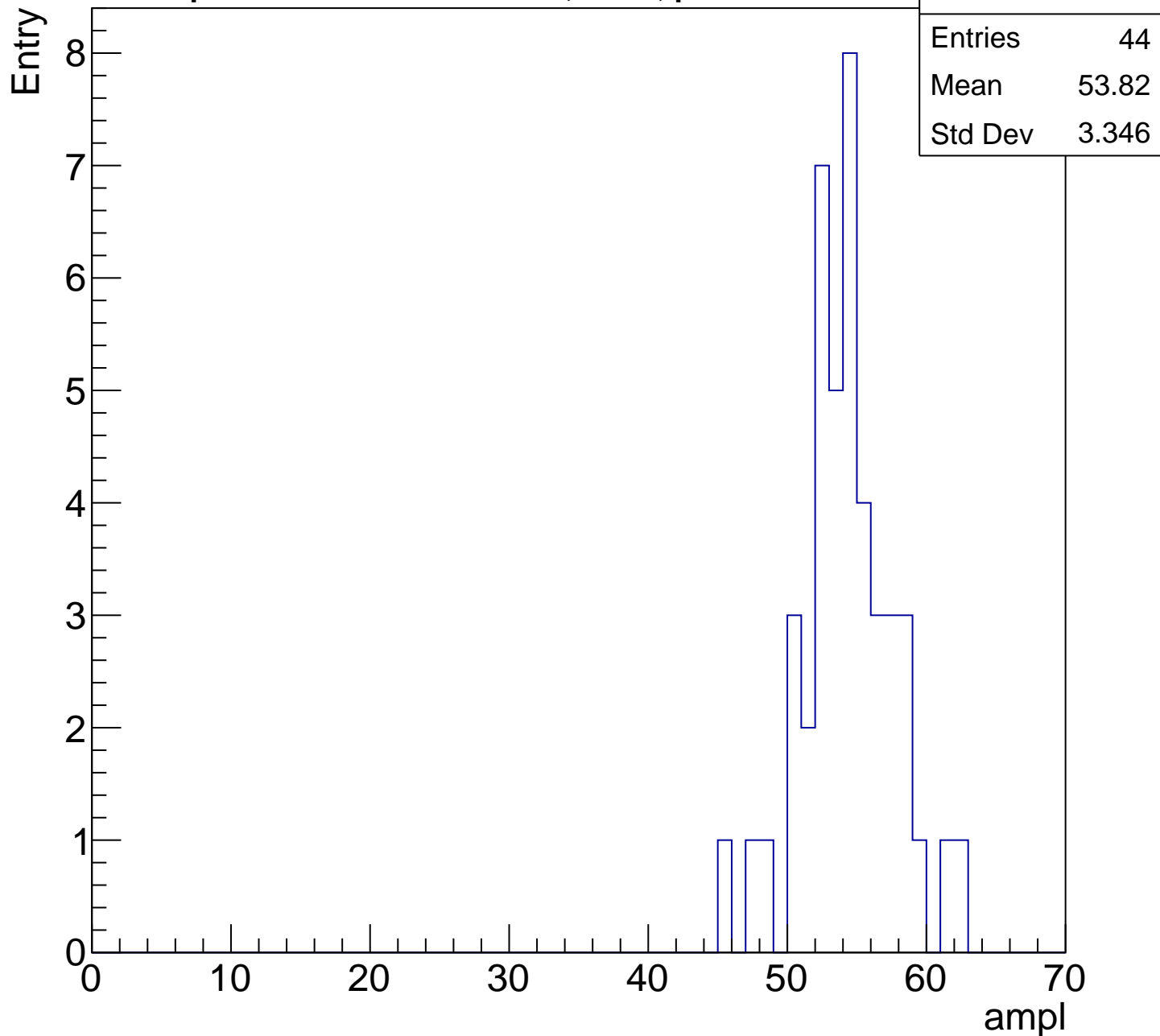
Entry

Entries	60
Mean	47.13
Std Dev	9.285



# B1L103S, U3-ch67, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U3-ch67, adc5

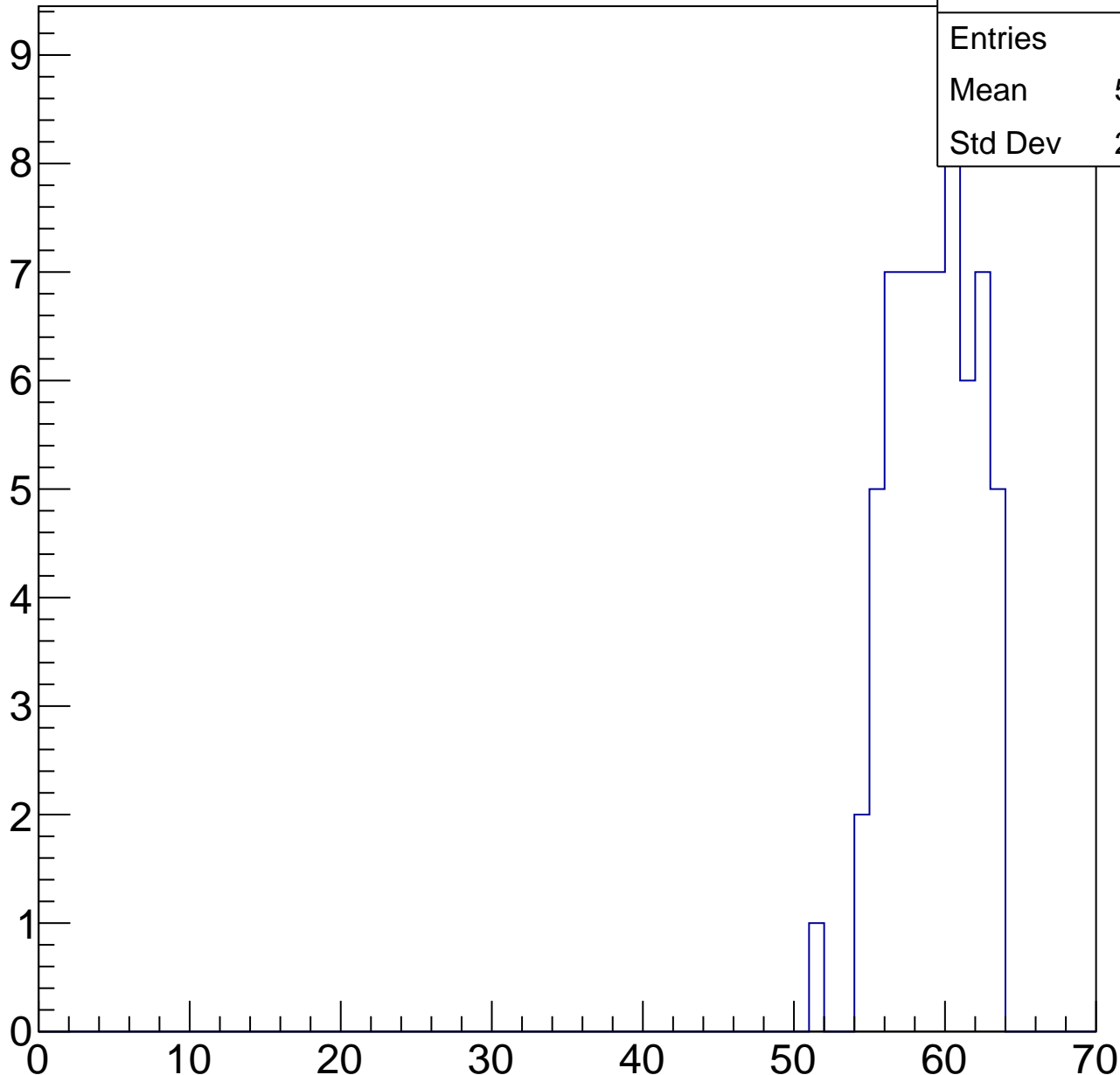
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	63
Mean	58.71
Std Dev	2.711

ampl

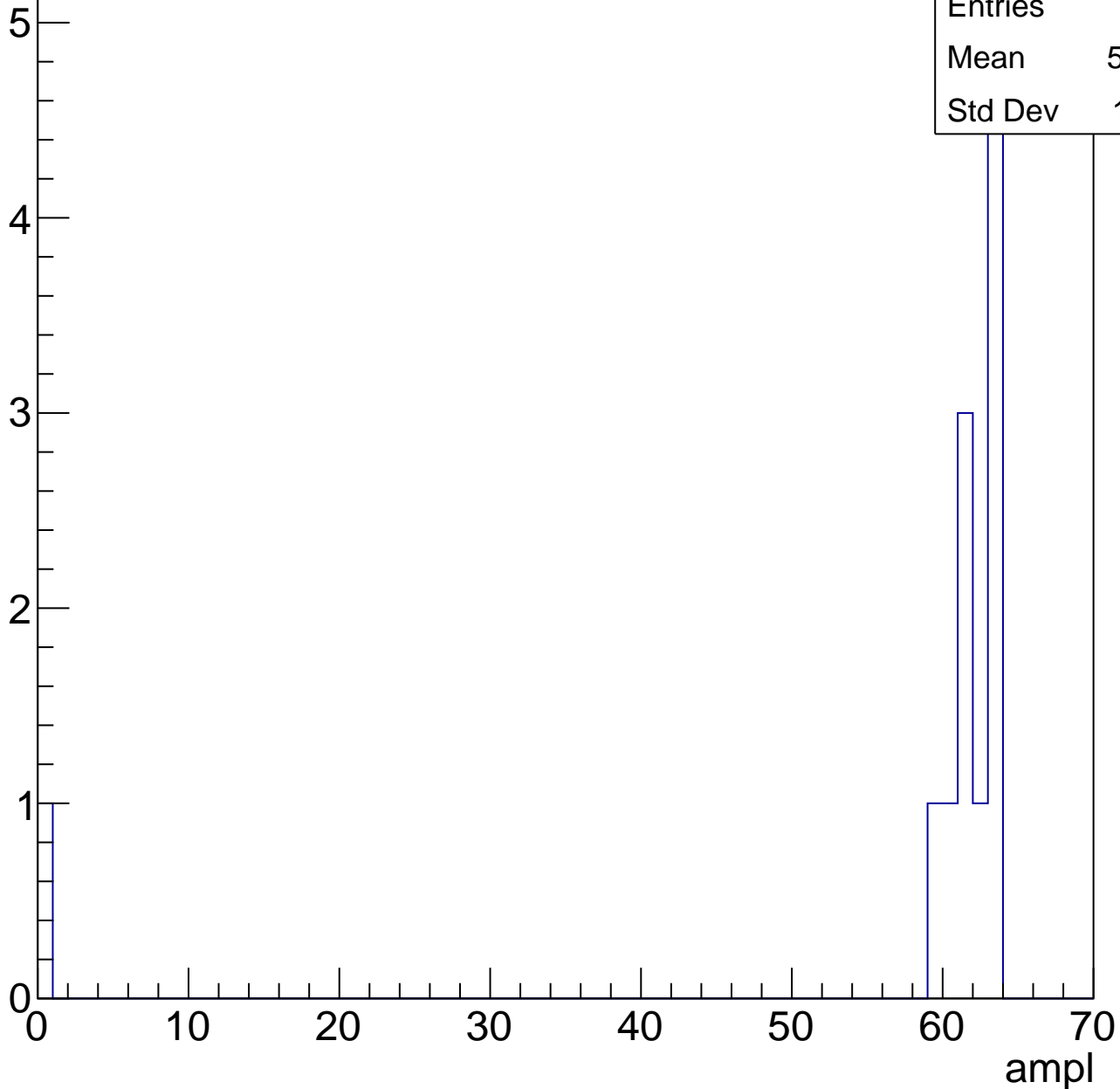


# B1L103S, U3-ch67, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	12
Mean	56.58
Std Dev	17.11





# B1L103S, U3-ch67, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51

Entry



# B1L103S, U3-ch68, adc0

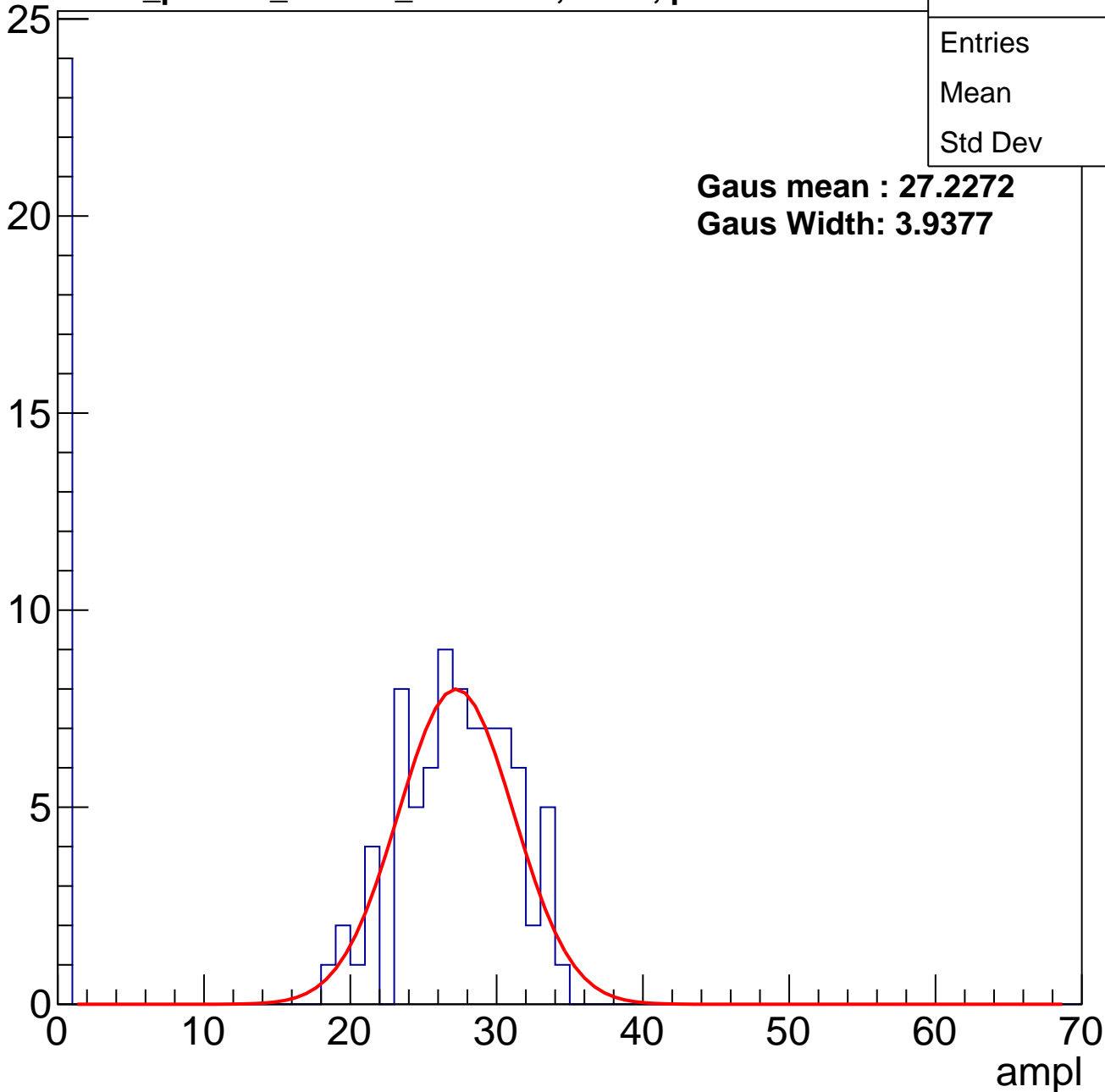
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	103
Mean	20.6
Std Dev	11.81

**Gaus mean : 27.2272**

**Gaus Width: 3.9377**

Entry



# B1L103S, U3-ch68, adc1

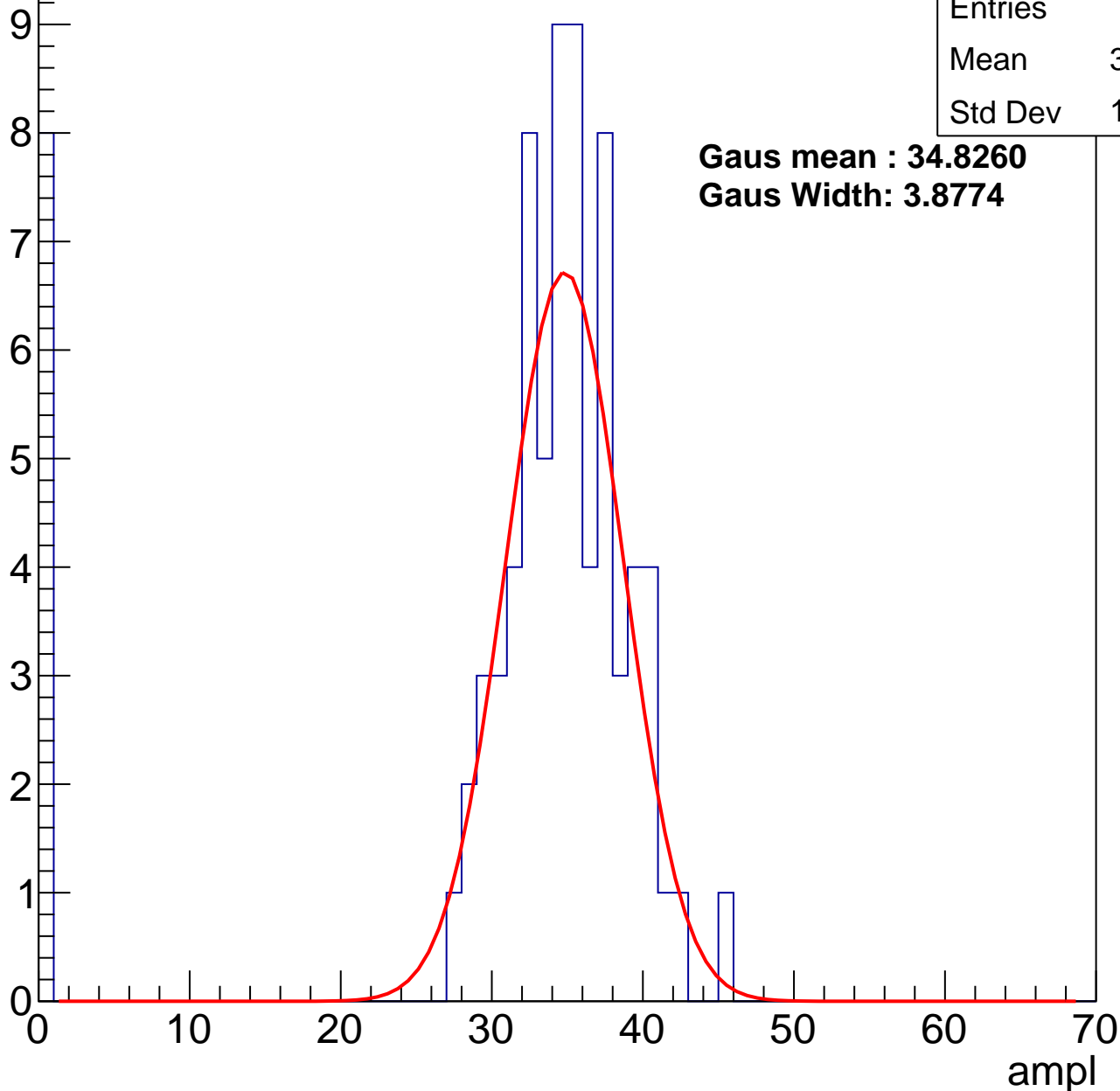
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	78
Mean	31.08
Std Dev	11.05

**Gaus mean : 34.8260**

**Gaus Width: 3.8774**



# B1L103S, U3-ch68, adc2

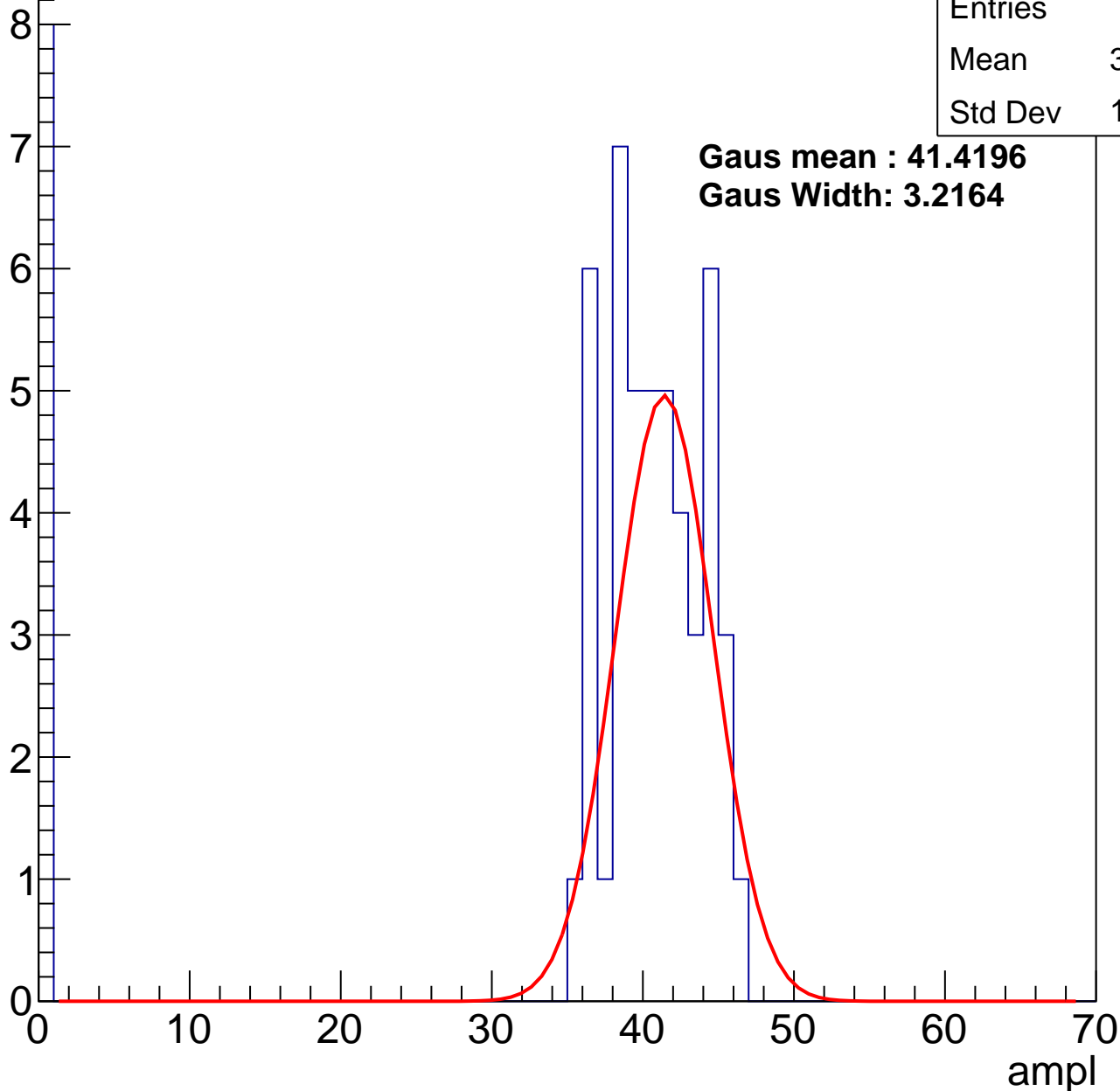
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	55
Mean	34.47
Std Dev	14.48

**Gaus mean : 41.4196**

**Gaus Width: 3.2164**

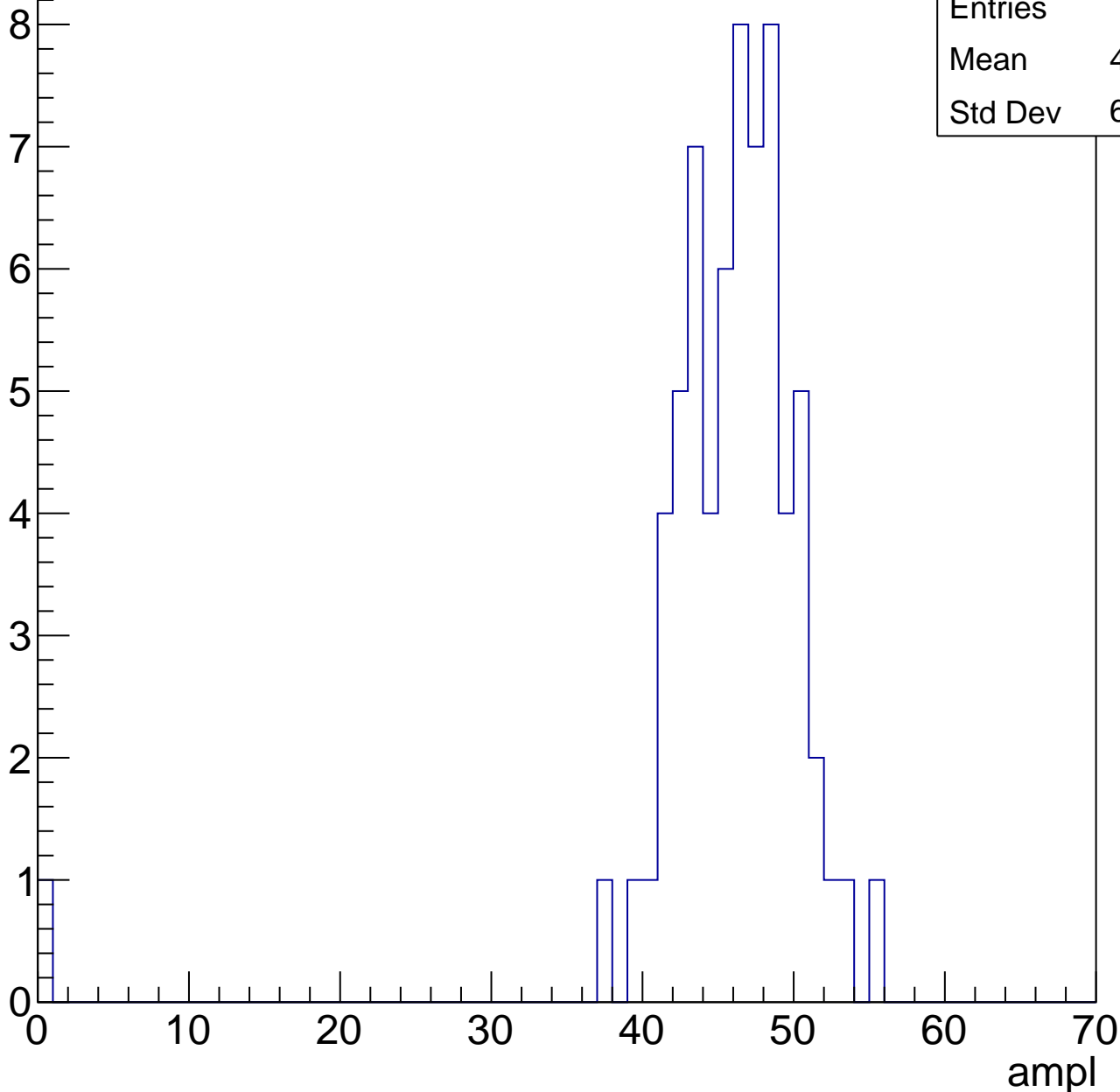


# B1L103S, U3-ch68, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	45.16
Std Dev	6.546

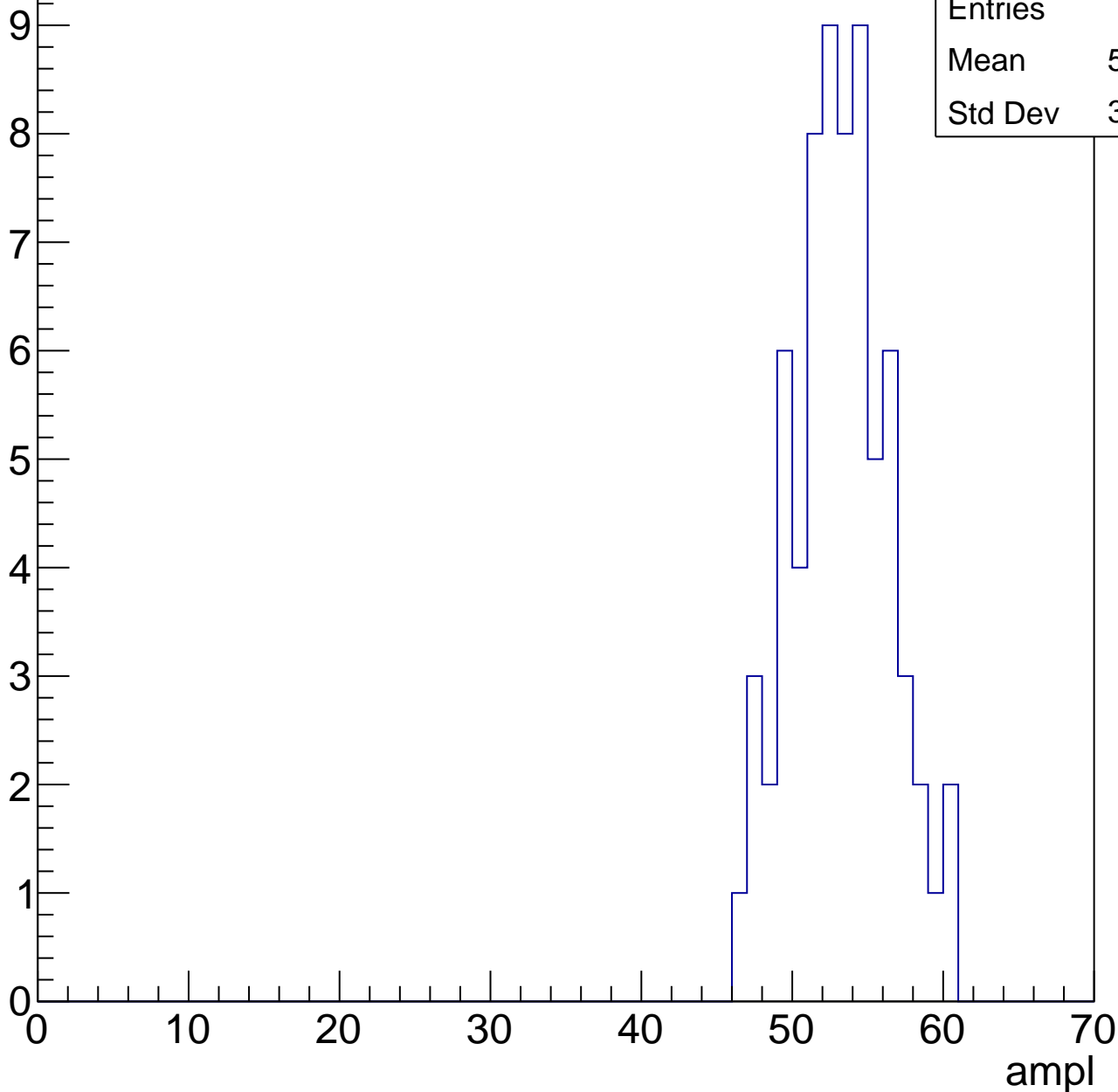


# B1L103S, U3-ch68, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	52.75
Std Dev	3.164

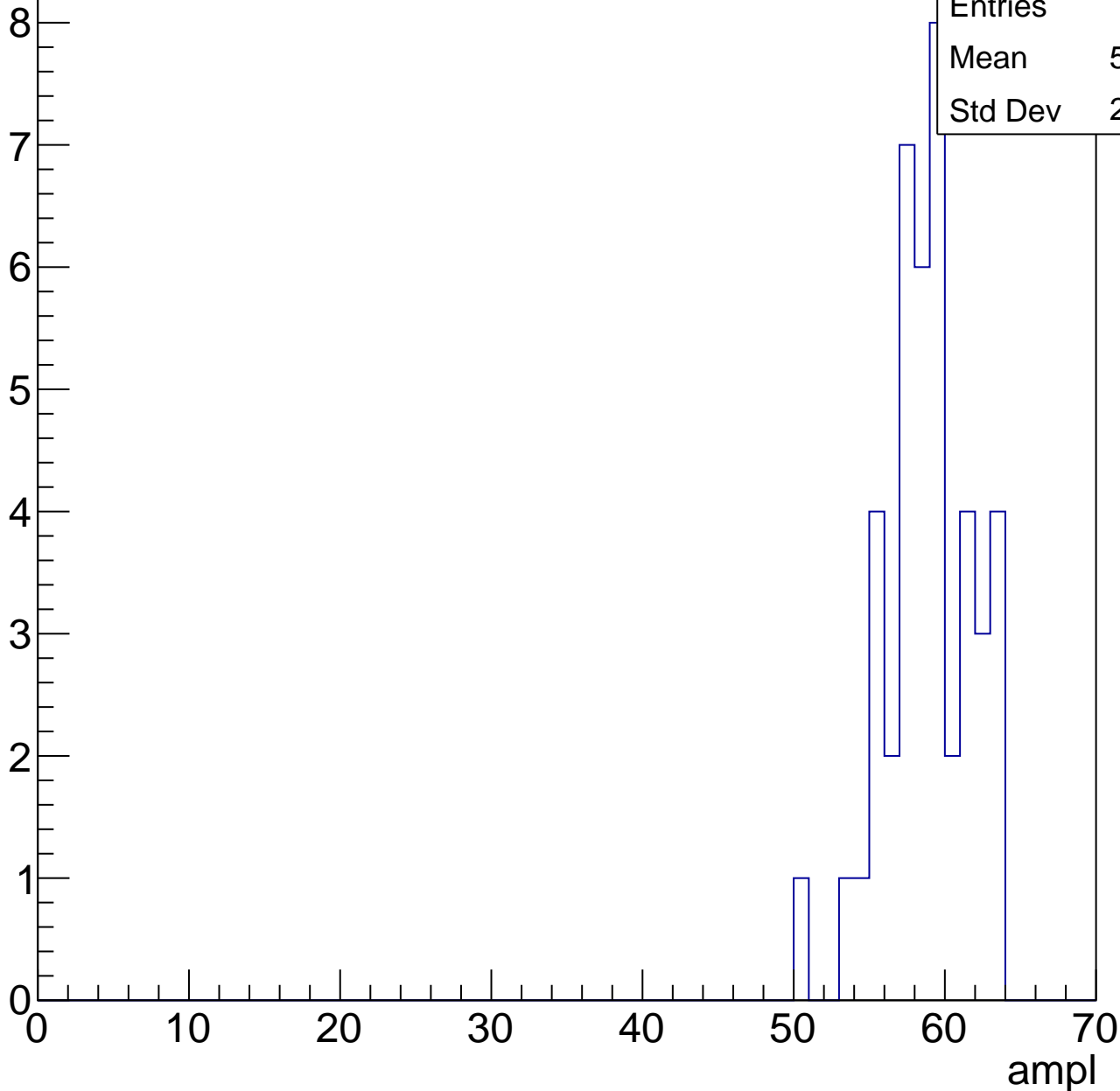


# B1L103S, U3-ch68, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	43
Mean	58.37
Std Dev	2.853

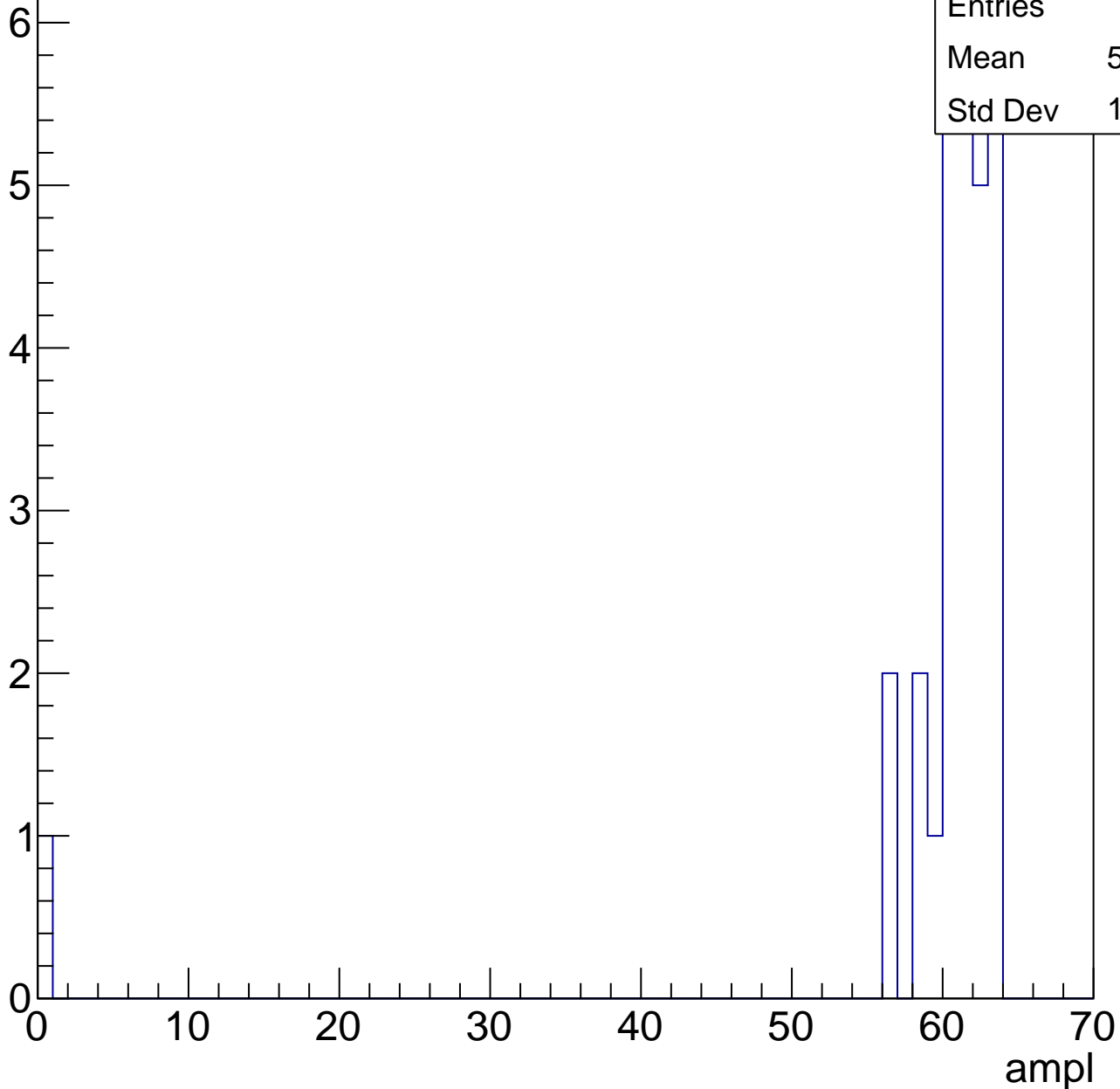


# B1L103S, U3-ch68, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	29
Mean	58.66
Std Dev	11.25



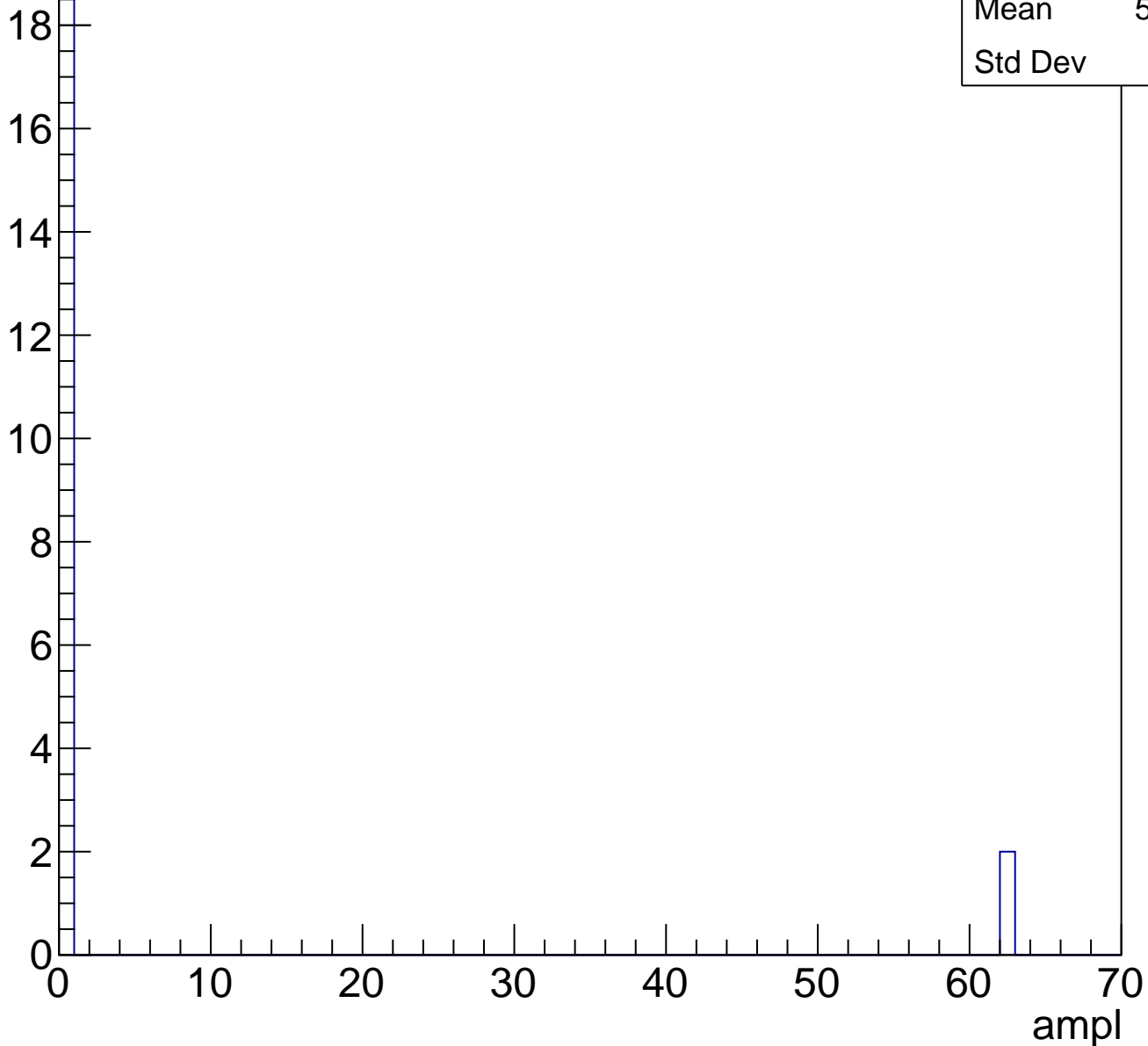


# B1L103S, U3-ch68, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	5.905
Std Dev	18.2

Entry



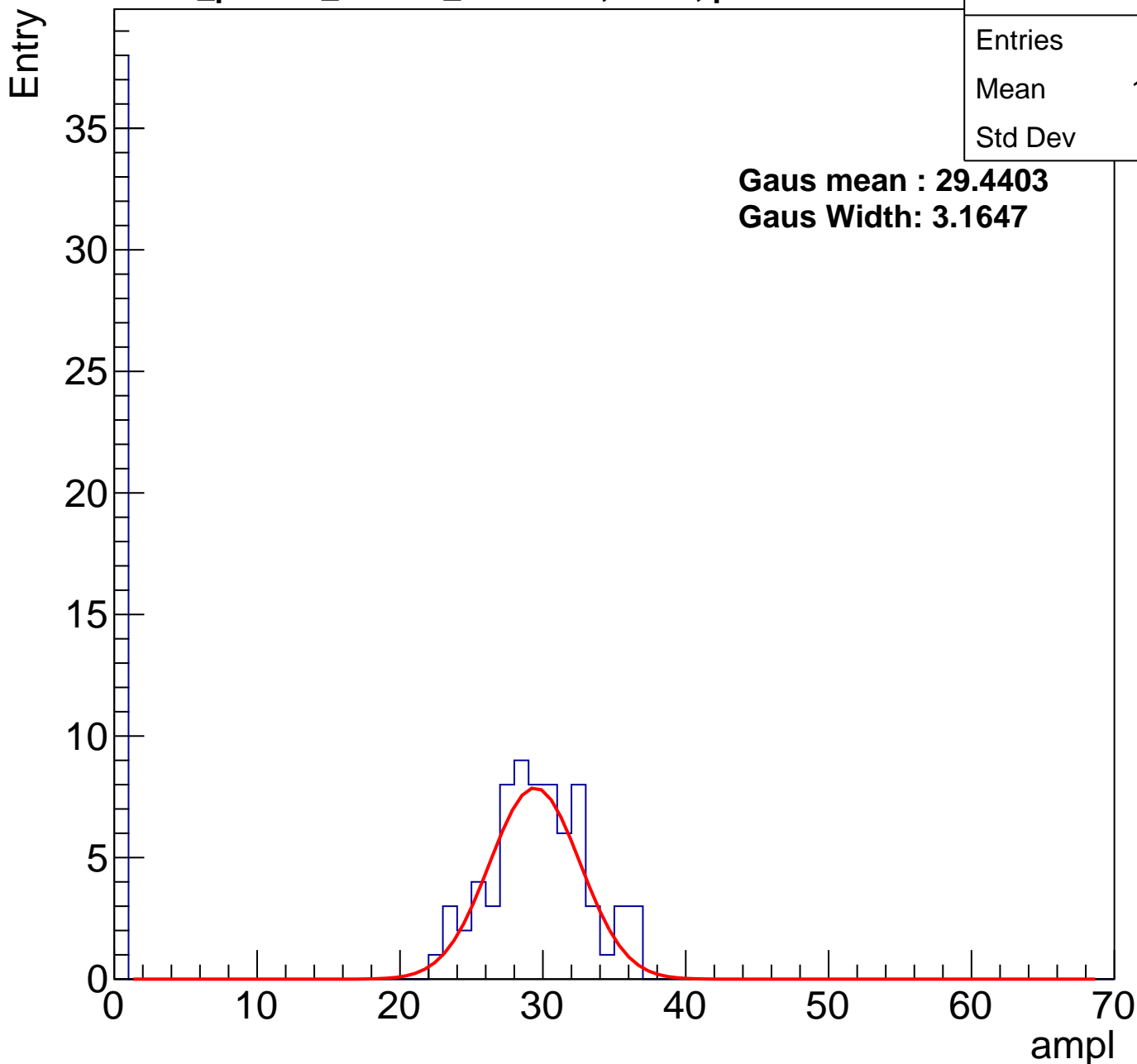
# B1L103S, U3-ch69, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	108
Mean	18.94
Std Dev	14.2

**Gaus mean : 29.4403**

**Gaus Width: 3.1647**



# B1L103S, U3-ch69, adc1

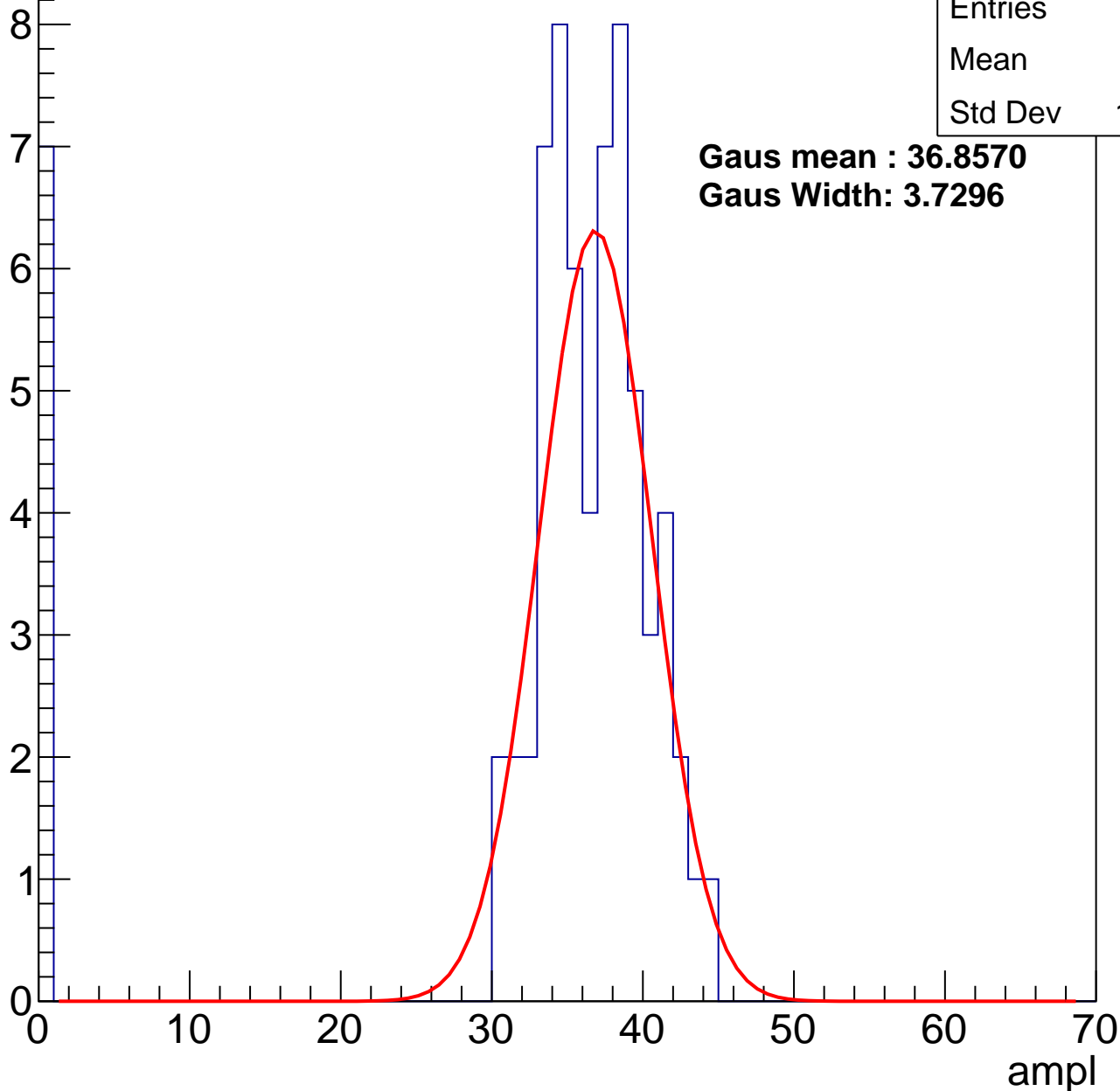
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	32.7
Std Dev	11.41

**Gaus mean : 36.8570**

**Gaus Width: 3.7296**



# B1L103S, U3-ch69, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	79
Mean	36.56
Std Dev	15.11

**Gaus mean : 42.9065**

**Gaus Width: 3.9404**

Entry

10

8

6

4

2

0

0

10

20

30

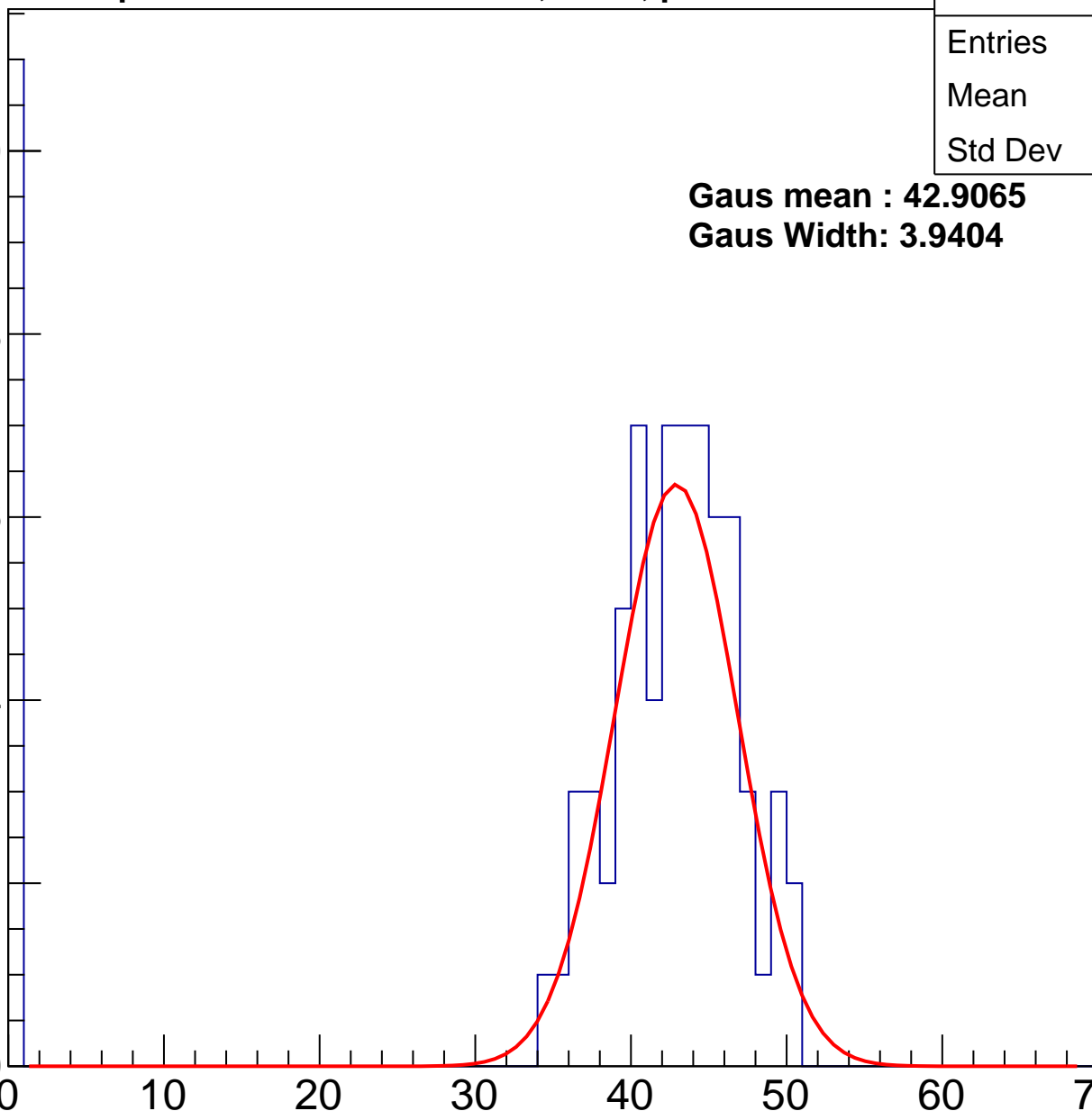
40

50

60

70

ampl

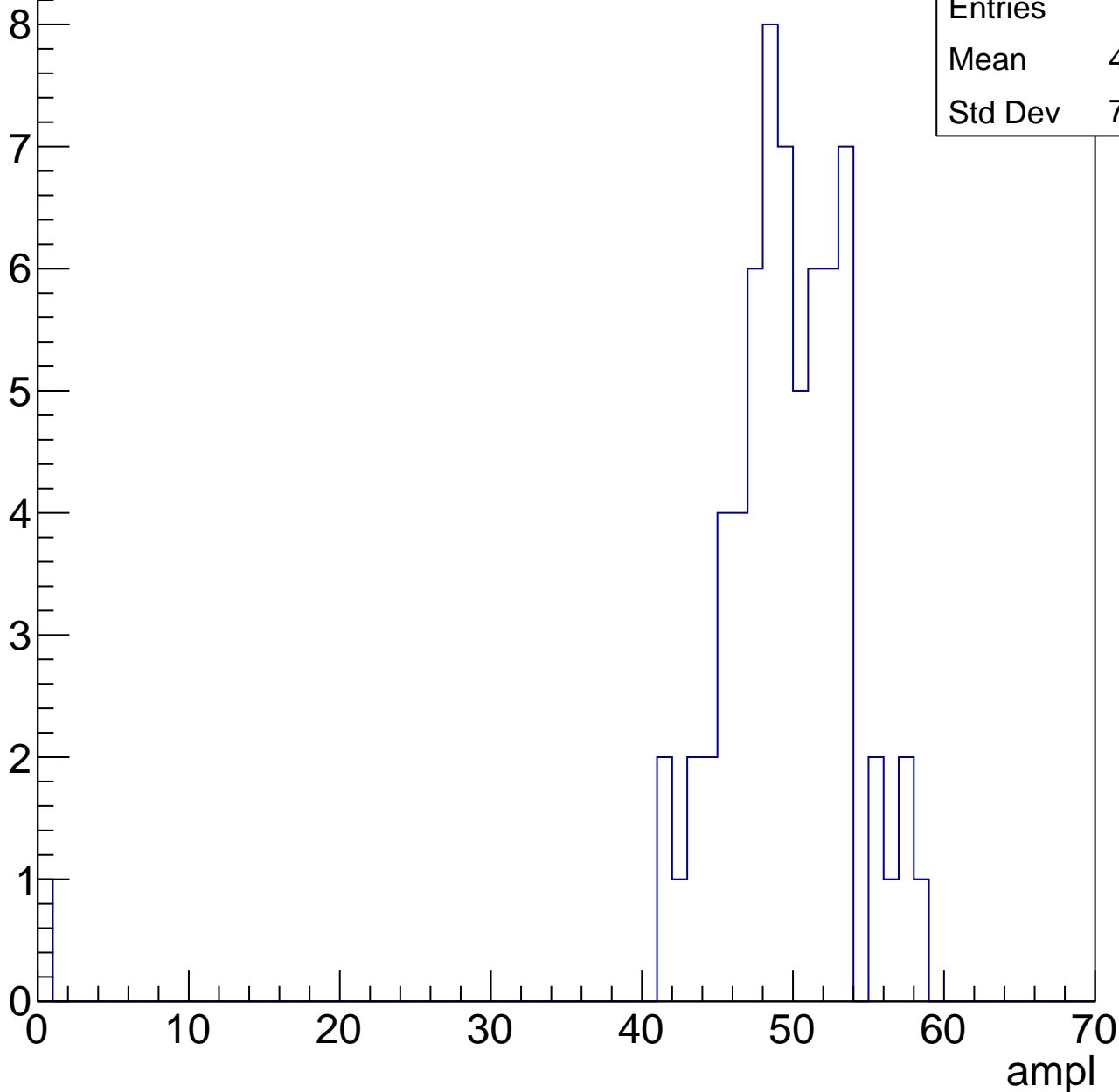


# B1L103S, U3-ch69, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	48.48
Std Dev	7.059

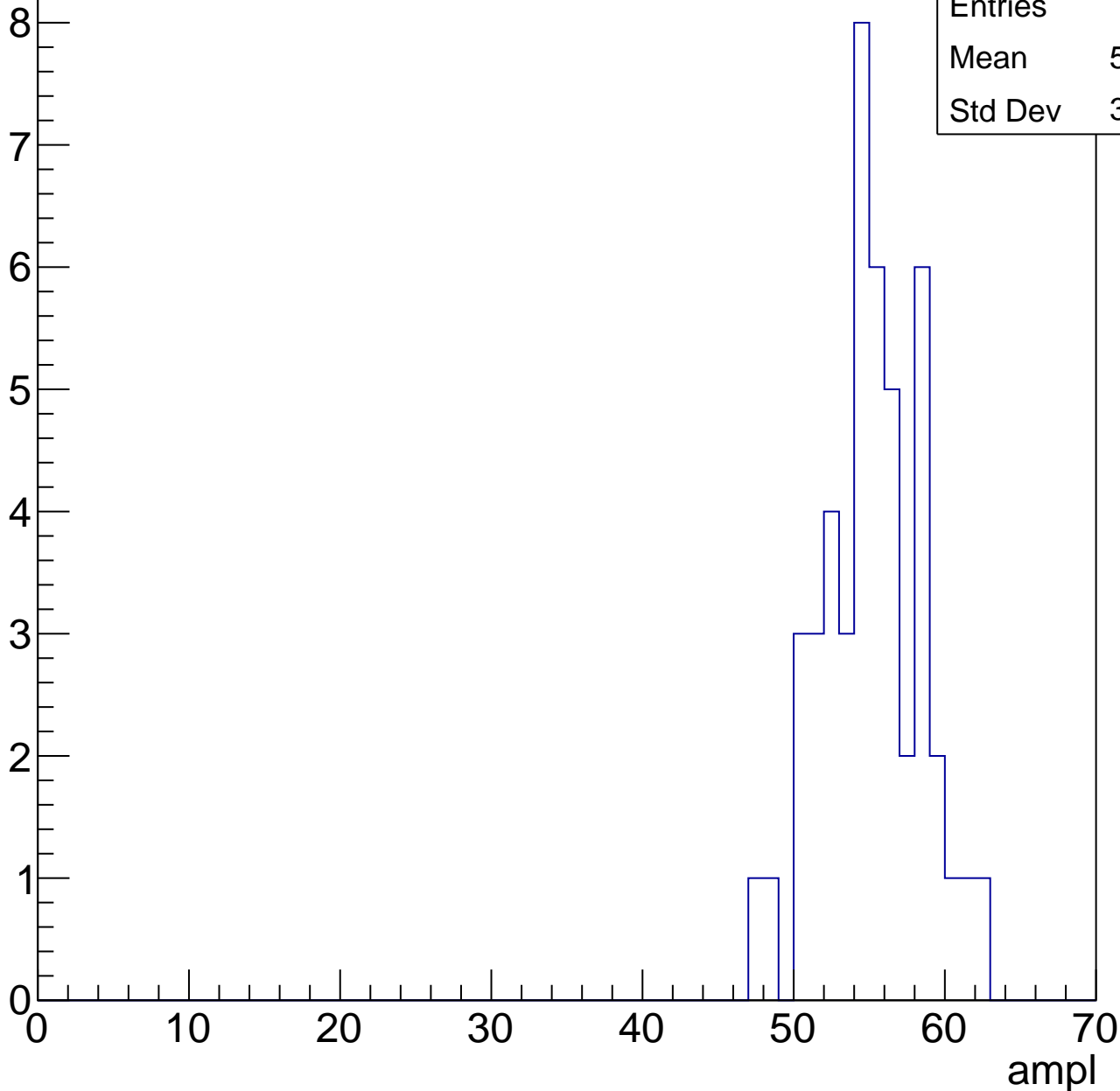


# B1L103S, U3-ch69, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

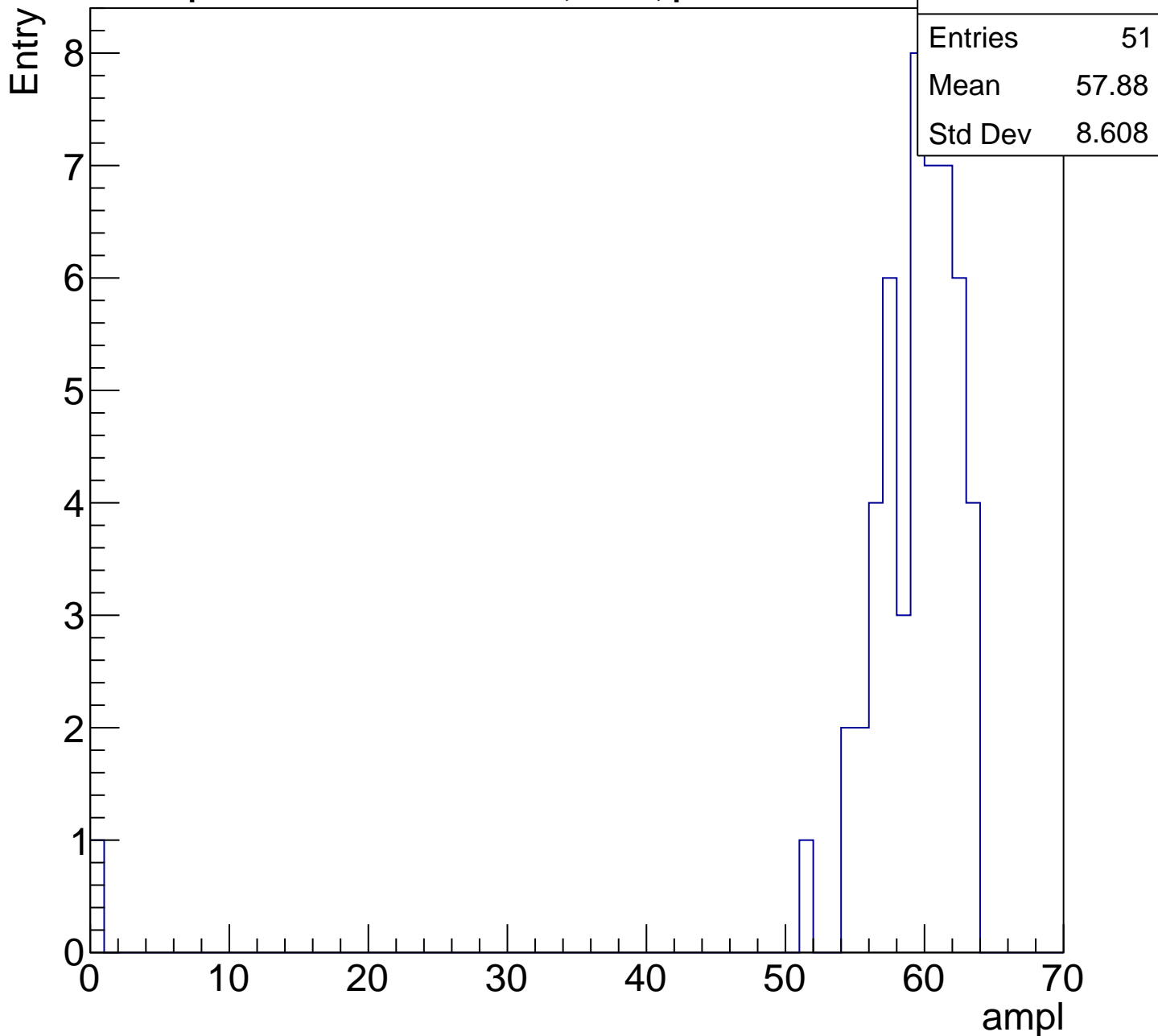
Entry

Entries	47
Mean	54.68
Std Dev	3.249



# B1L103S, U3-ch69, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

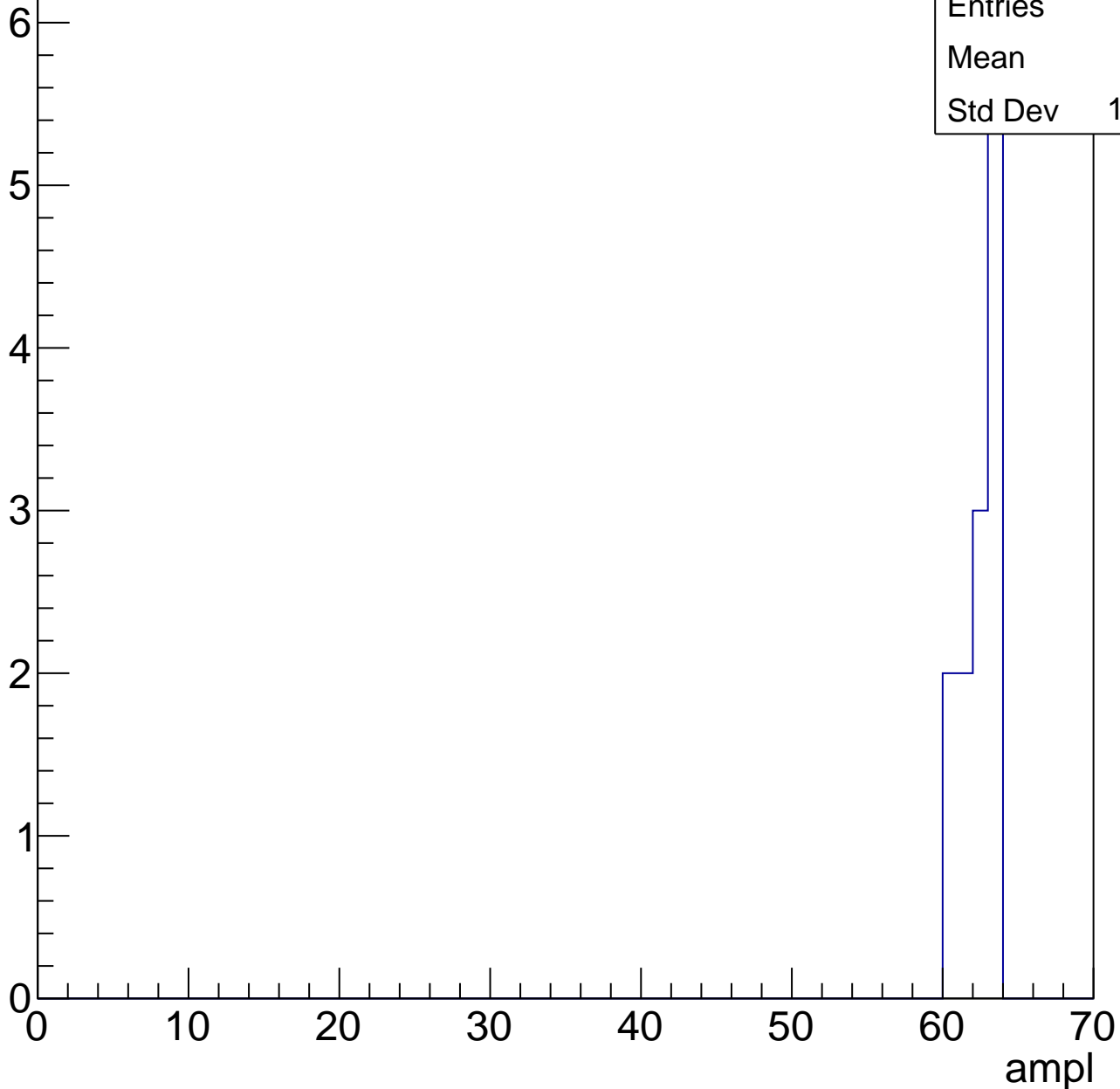


# B1L103S, U3-ch69, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	13
Mean	62
Std Dev	1.109





# B1L103S, U3-ch69, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	1.105
Std Dev	4.689

Entry



# B1L103S, U3-ch70, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	75
Mean	20.8
Std Dev	10.8

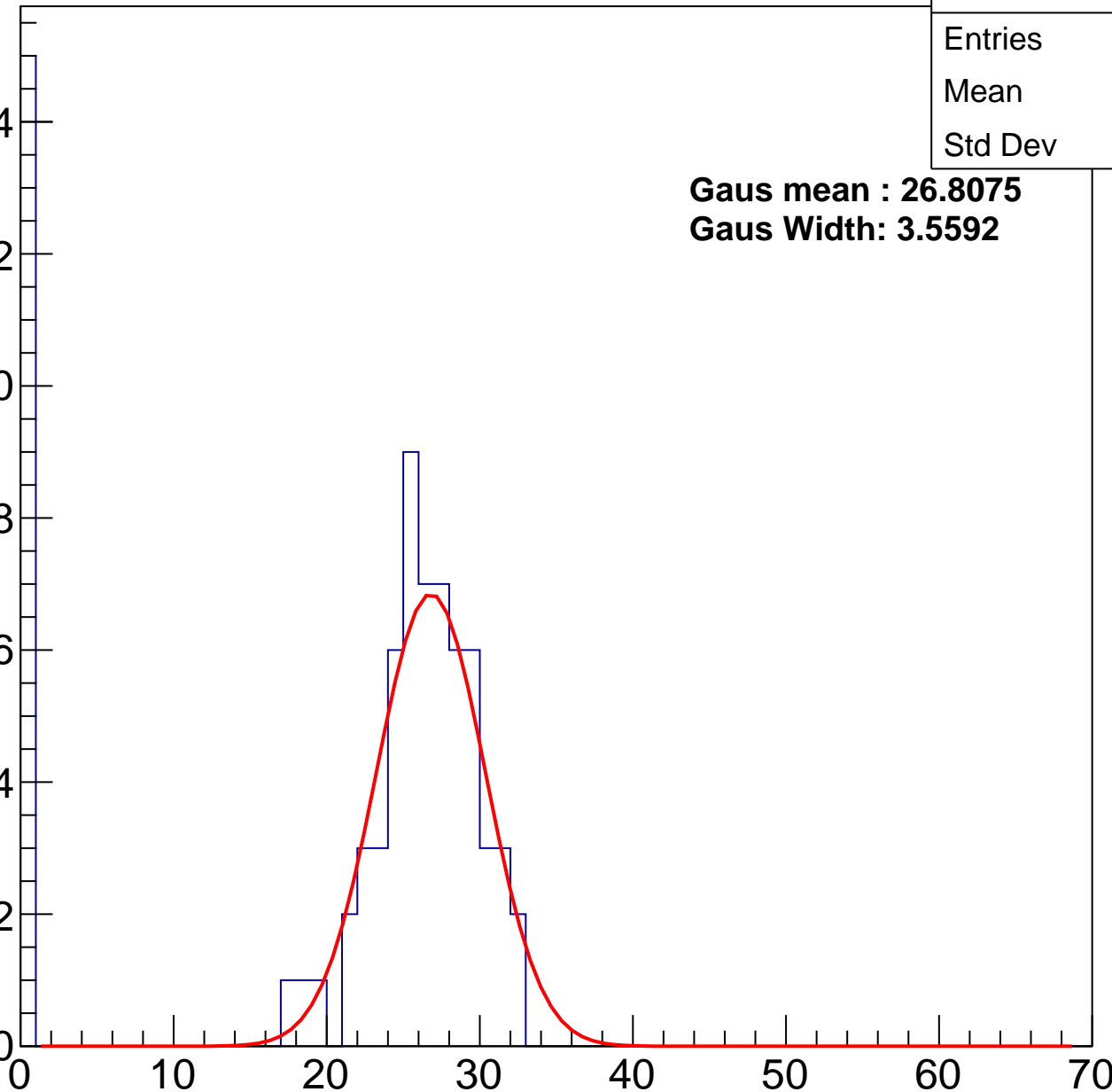
**Gaus mean : 26.8075**

**Gaus Width: 3.5592**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U3-ch70, adc1

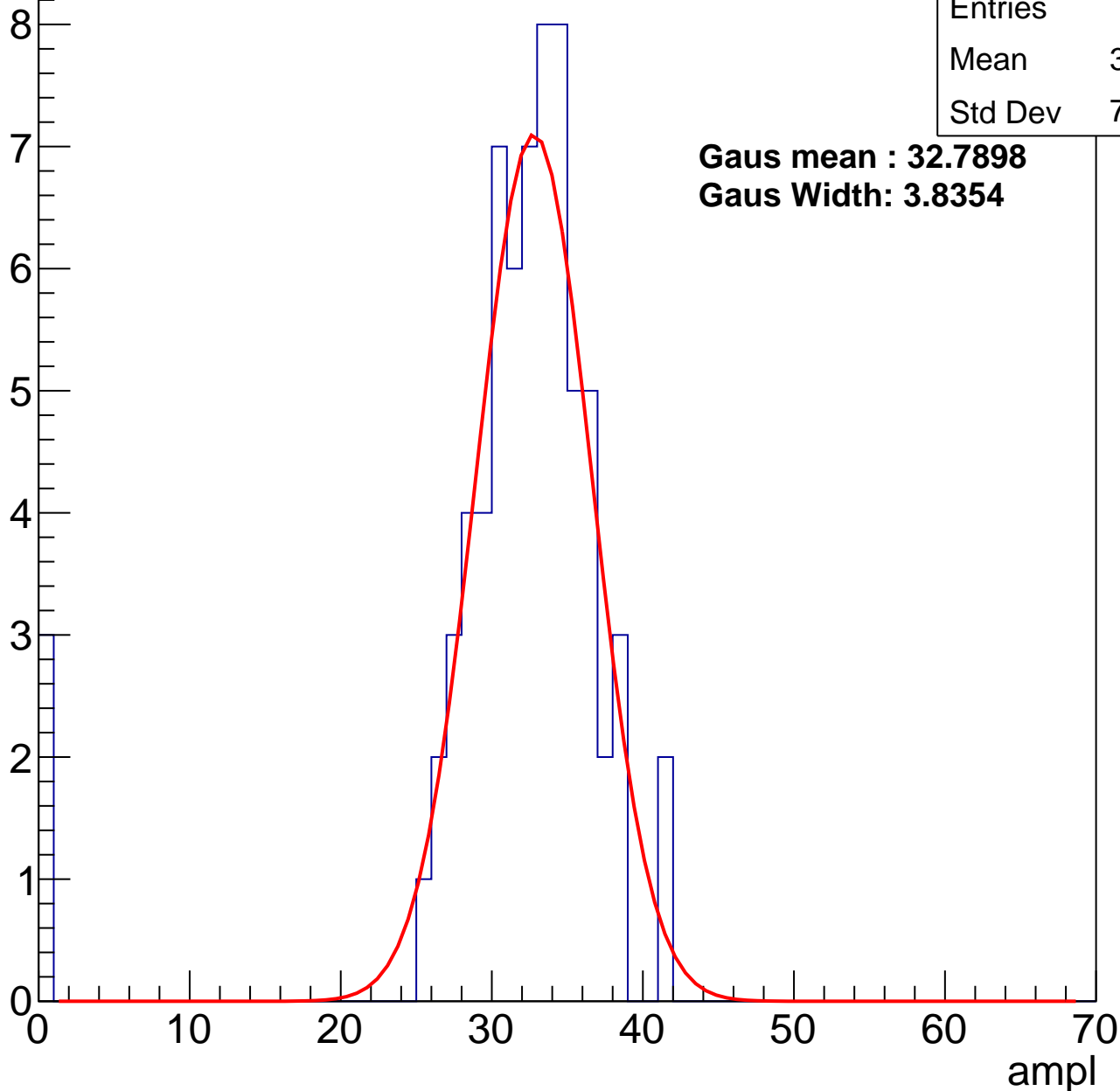
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	30.96
Std Dev	7.378

**Gaus mean : 32.7898**

**Gaus Width: 3.8354**



# B1L103S, U3-ch70, adc2

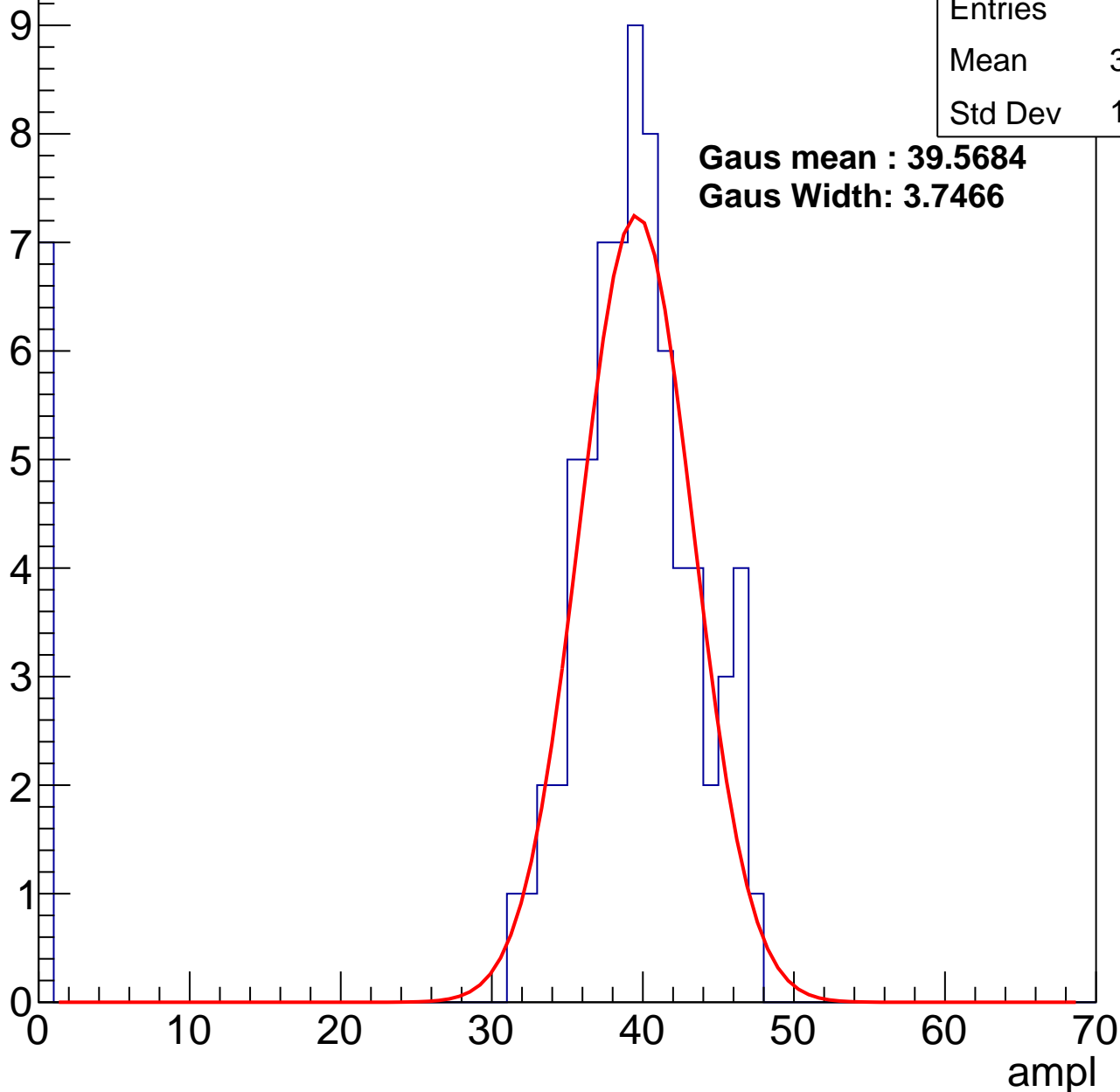
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	78
Mean	35.74
Std Dev	11.75

**Gaus mean : 39.5684**

**Gaus Width: 3.7466**

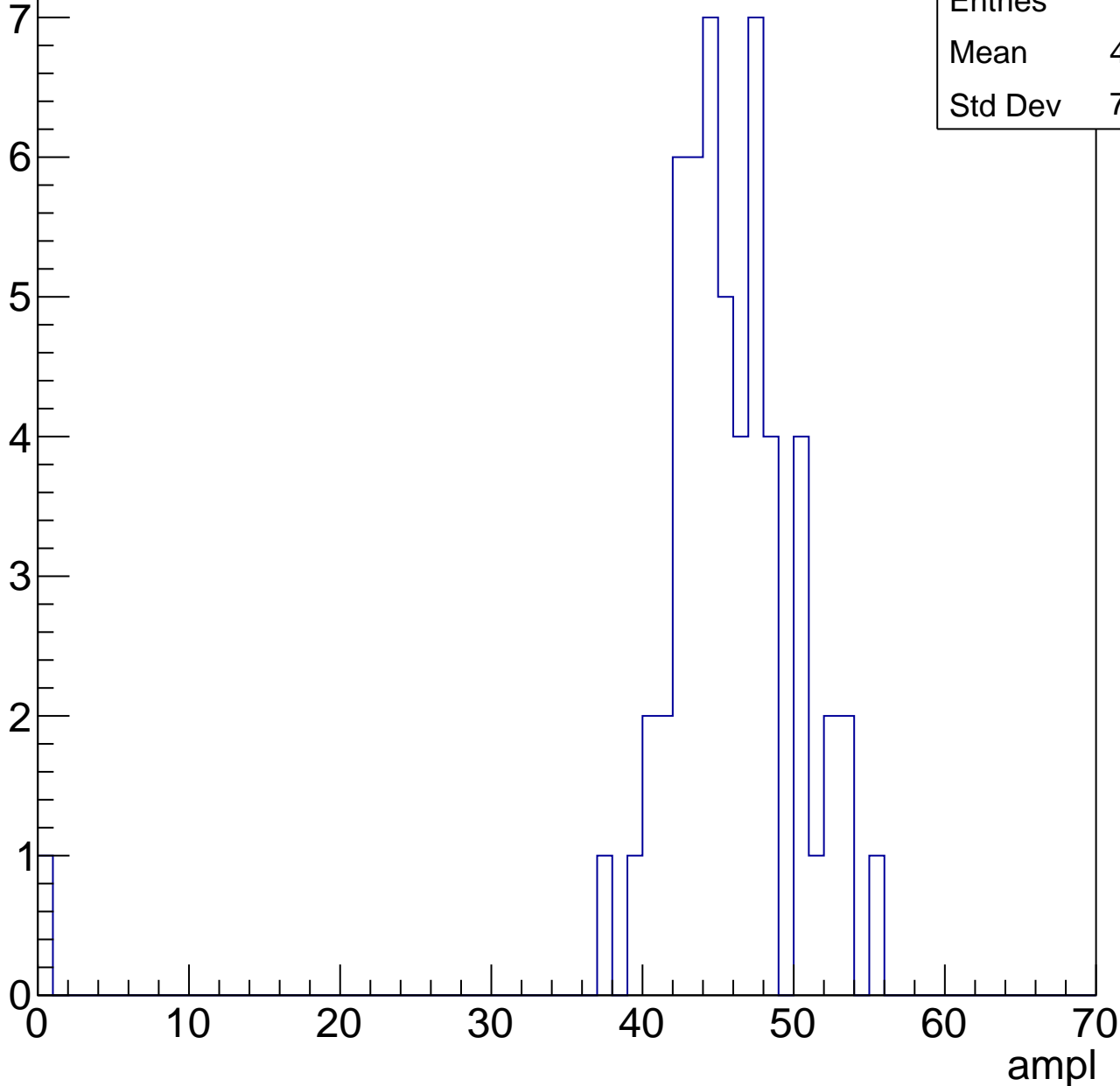


# B1L103S, U3-ch70, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

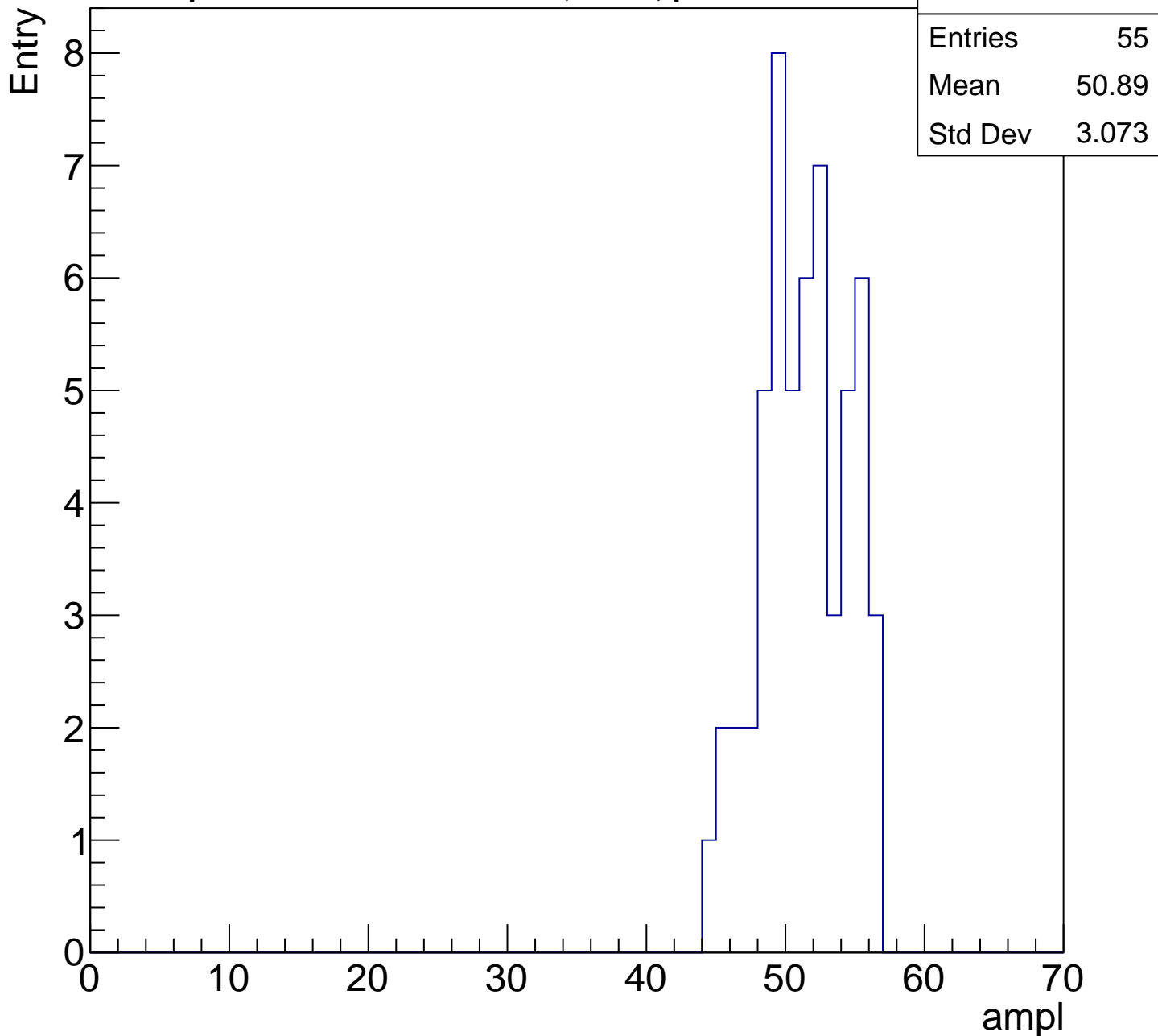
Entry

Entries	56
Mean	44.68
Std Dev	7.092



# B1L103S, U3-ch70, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

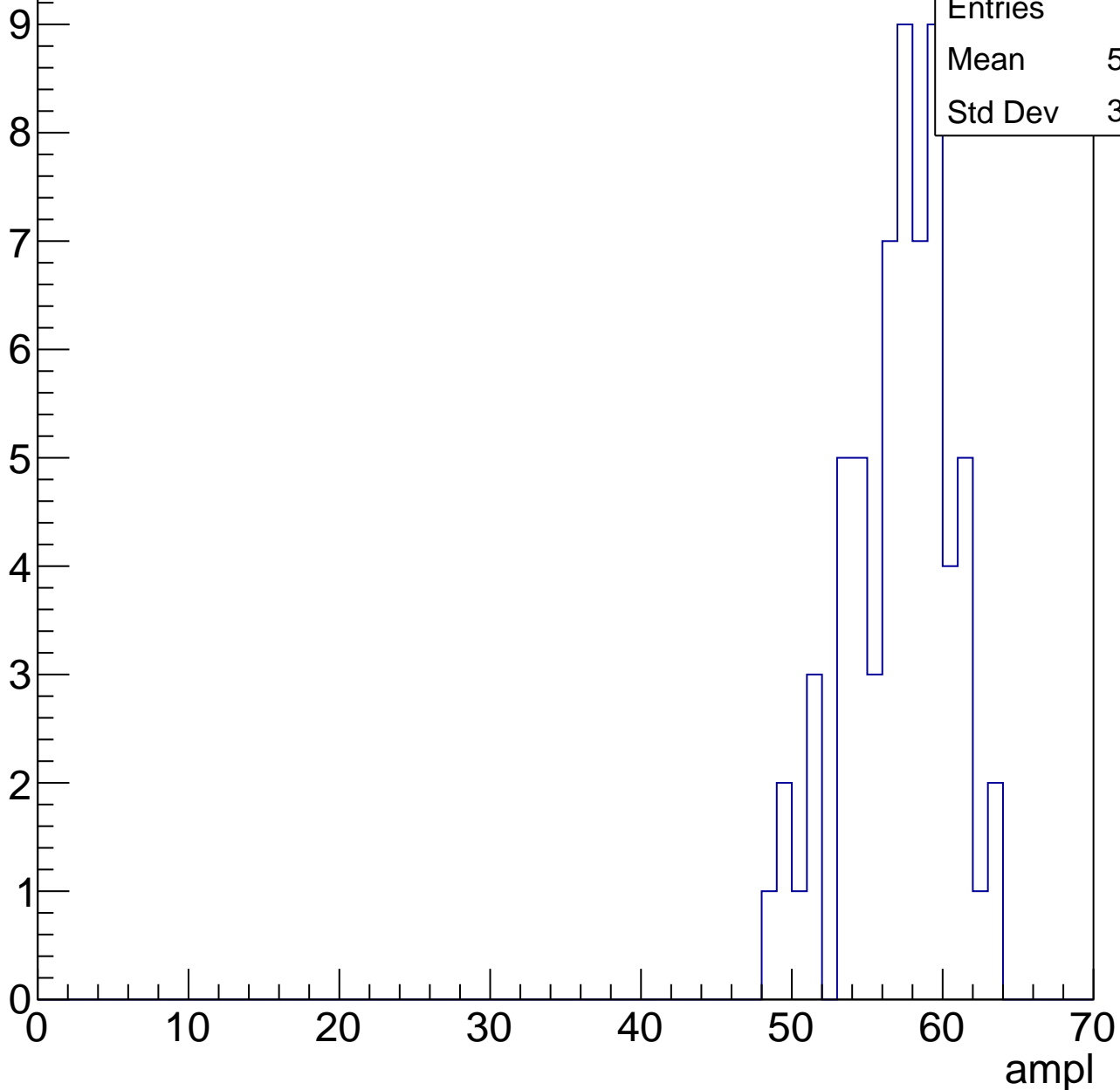


# B1L103S, U3-ch70, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	56.62
Std Dev	3.439

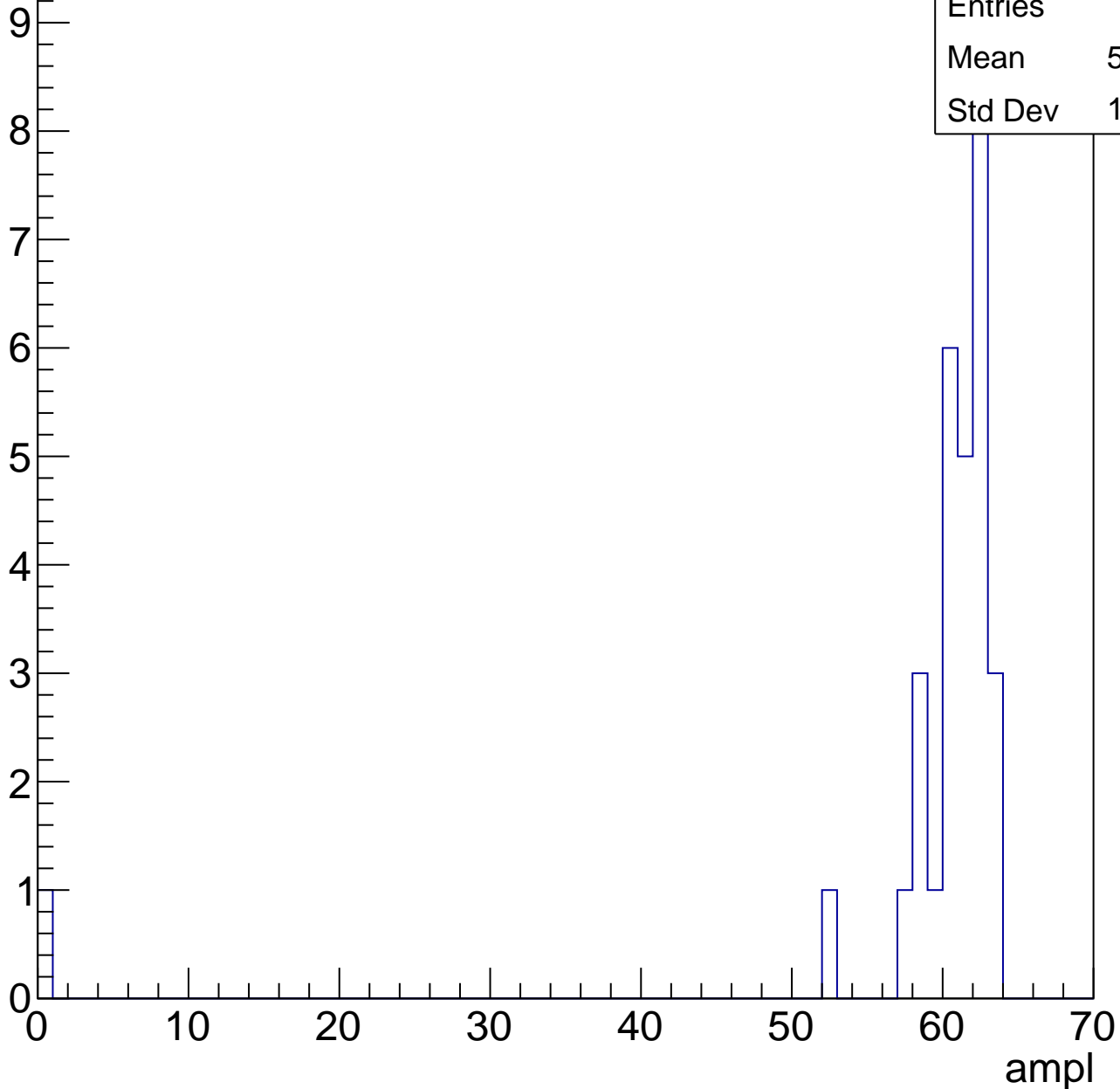


# B1L103S, U3-ch70, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	30
Mean	58.47
Std Dev	11.08

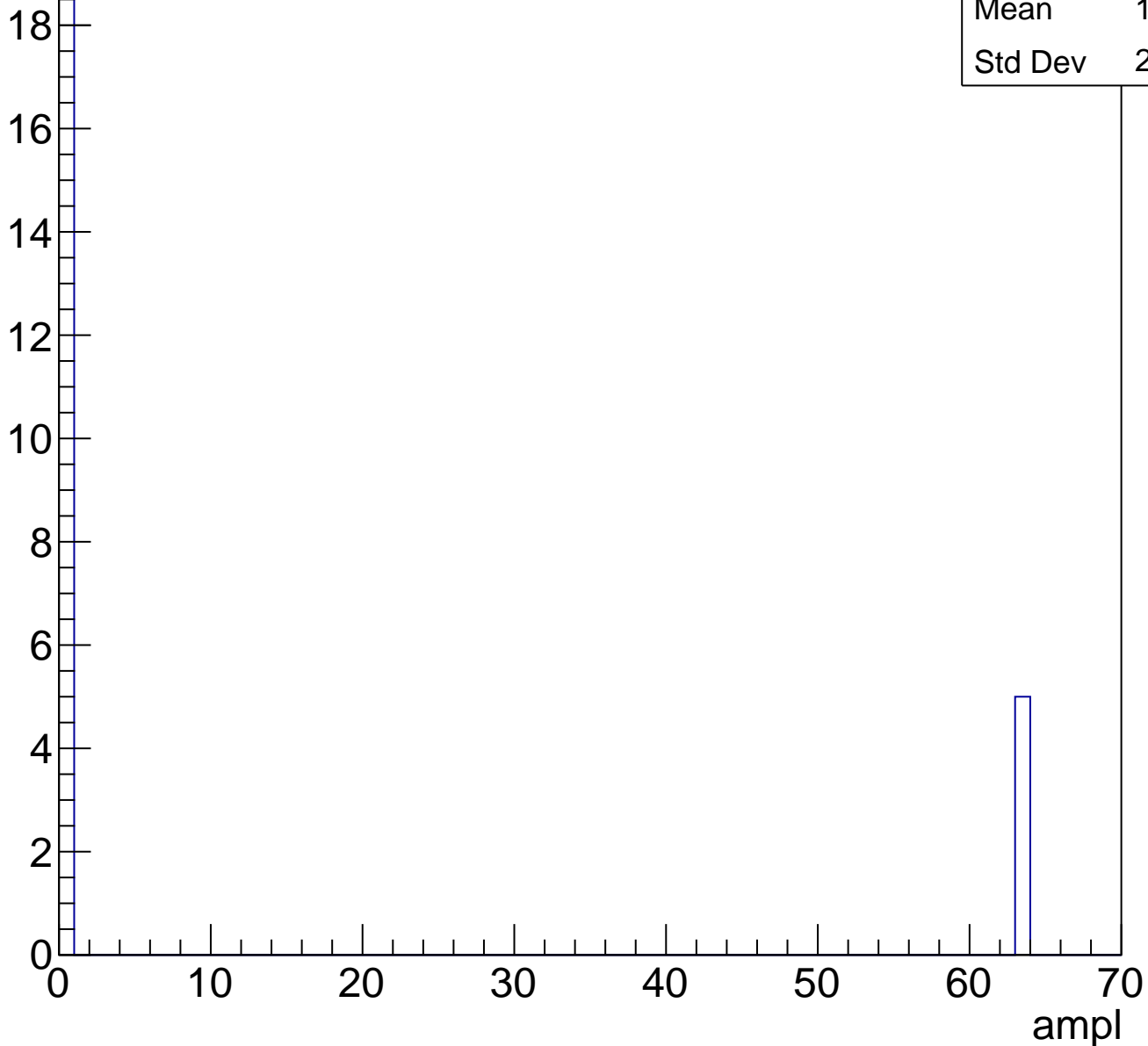




# B1L103S, U3-ch70, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



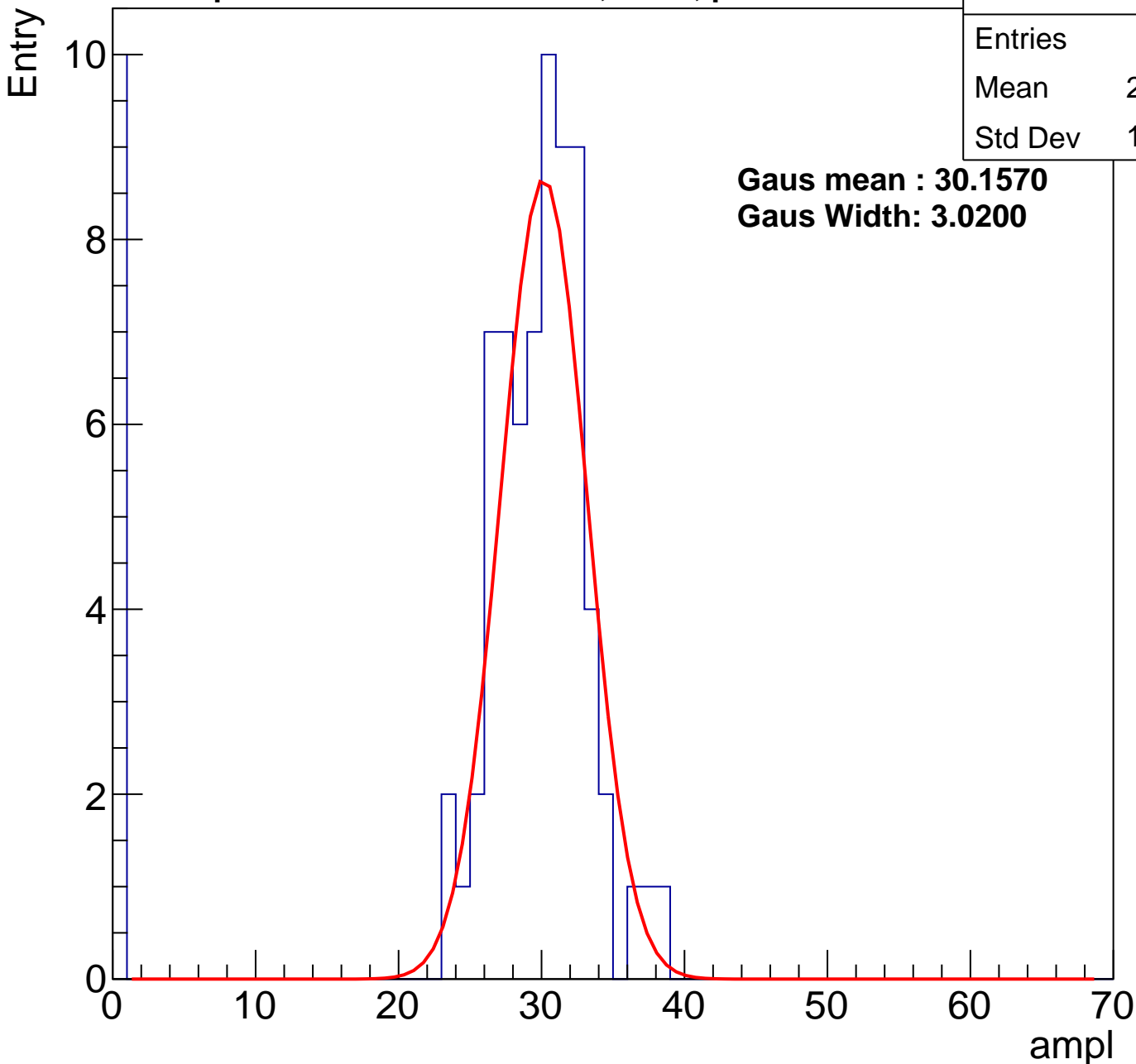
# B1L103S, U3-ch71, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	79
Mean	25.82
Std Dev	10.23

**Gaus mean : 30.1570**

**Gaus Width: 3.0200**



# B1L103S, U3-ch71, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	79
Mean	34.66
Std Dev	10.43

**Gaus mean : 37.8553**

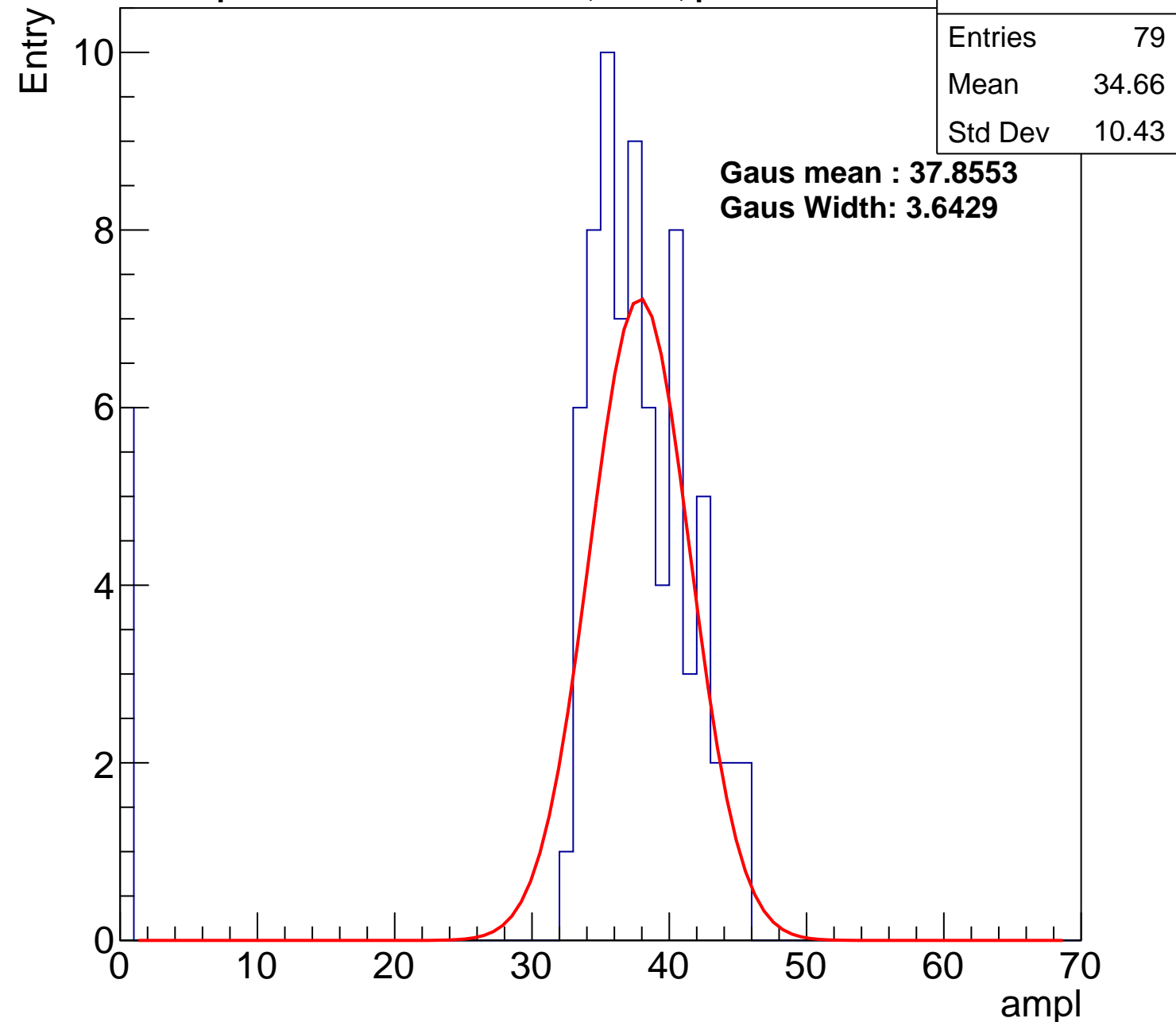
**Gaus Width: 3.6429**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U3-ch71, adc2

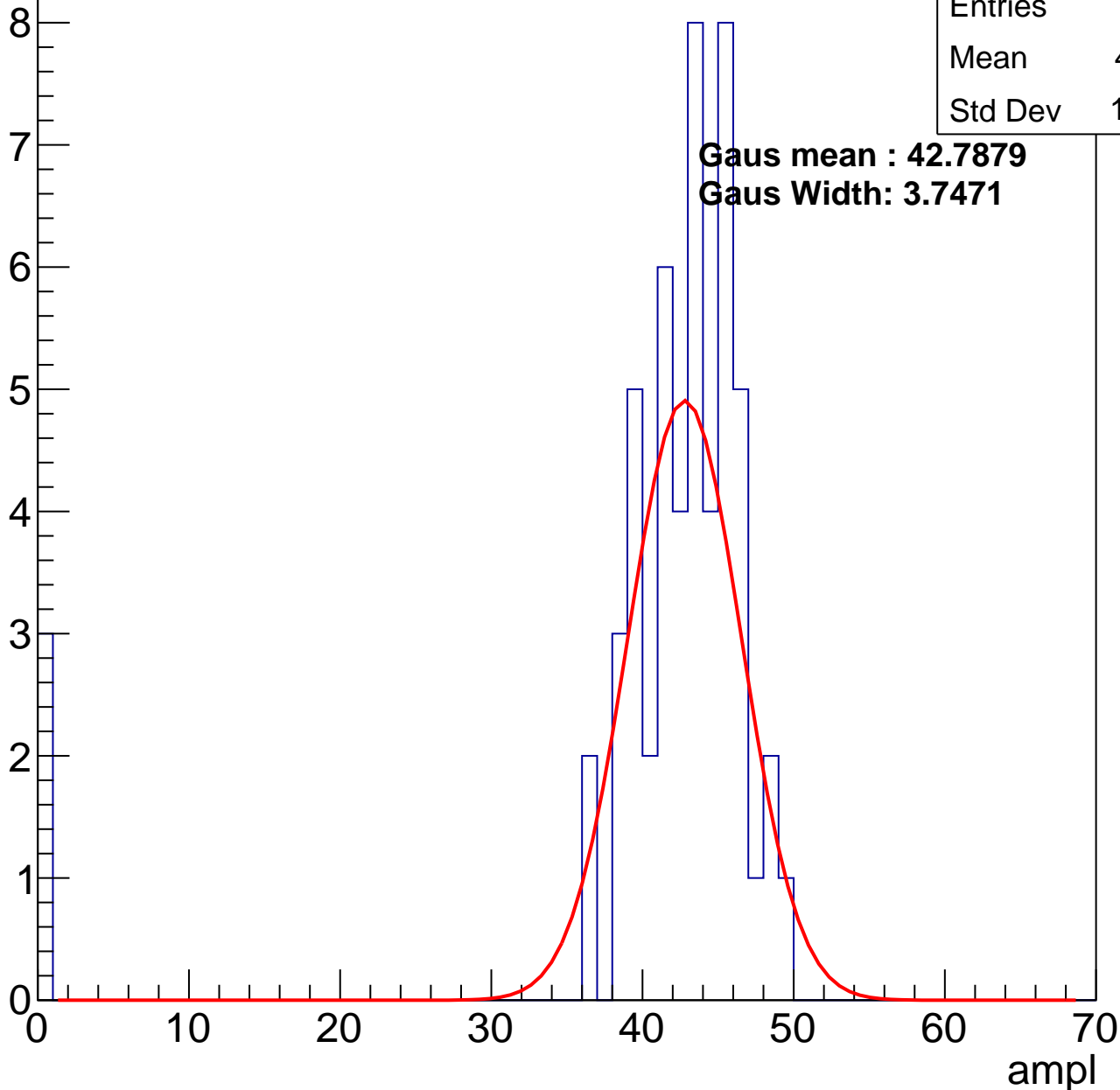
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	54
Mean	40.31
Std Dev	10.22

**Gaus mean : 42.7879**

**Gaus Width: 3.7471**

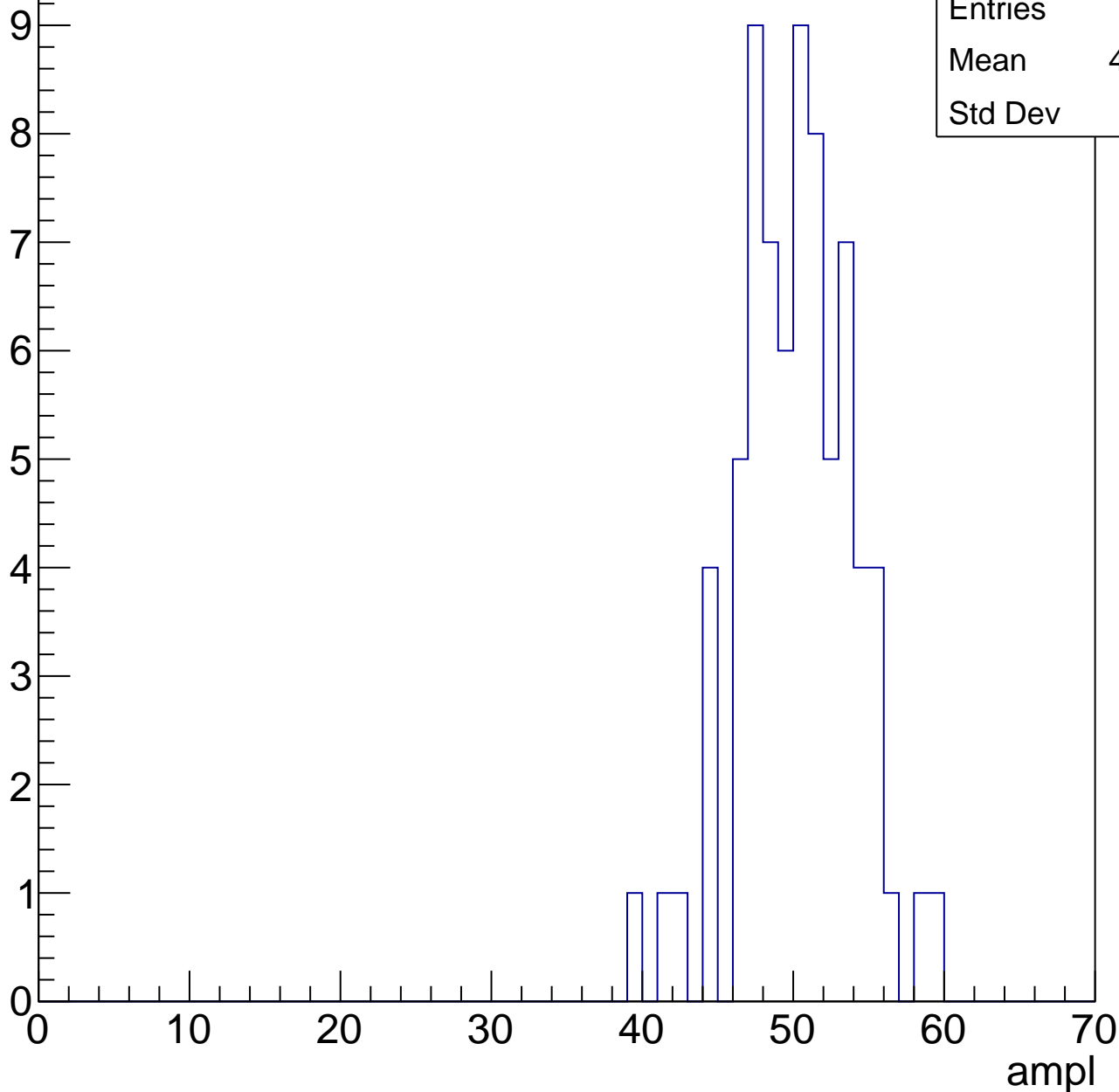


# B1L103S, U3-ch71, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	74
Mean	49.72
Std Dev	3.74

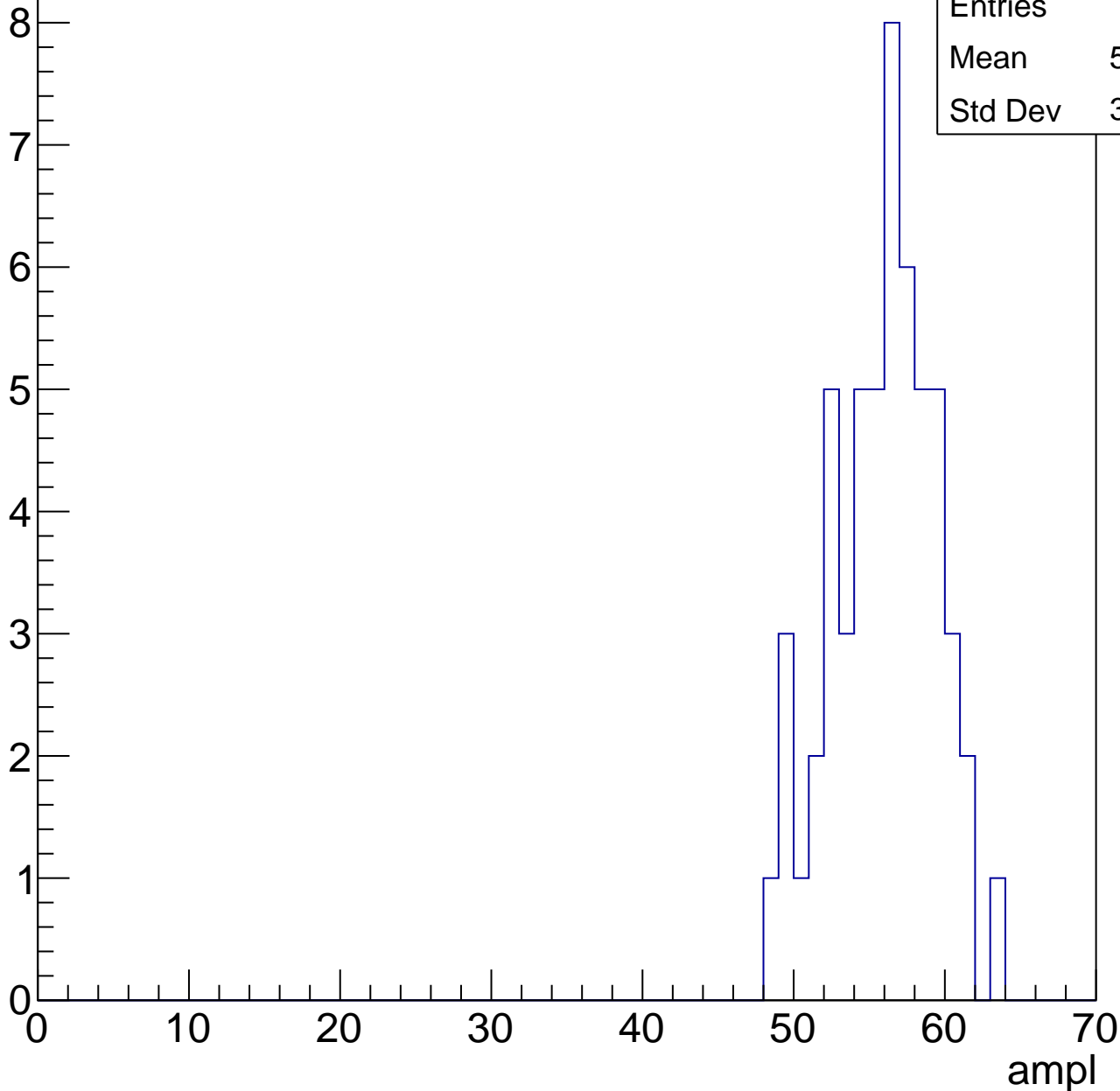


# B1L103S, U3-ch71, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

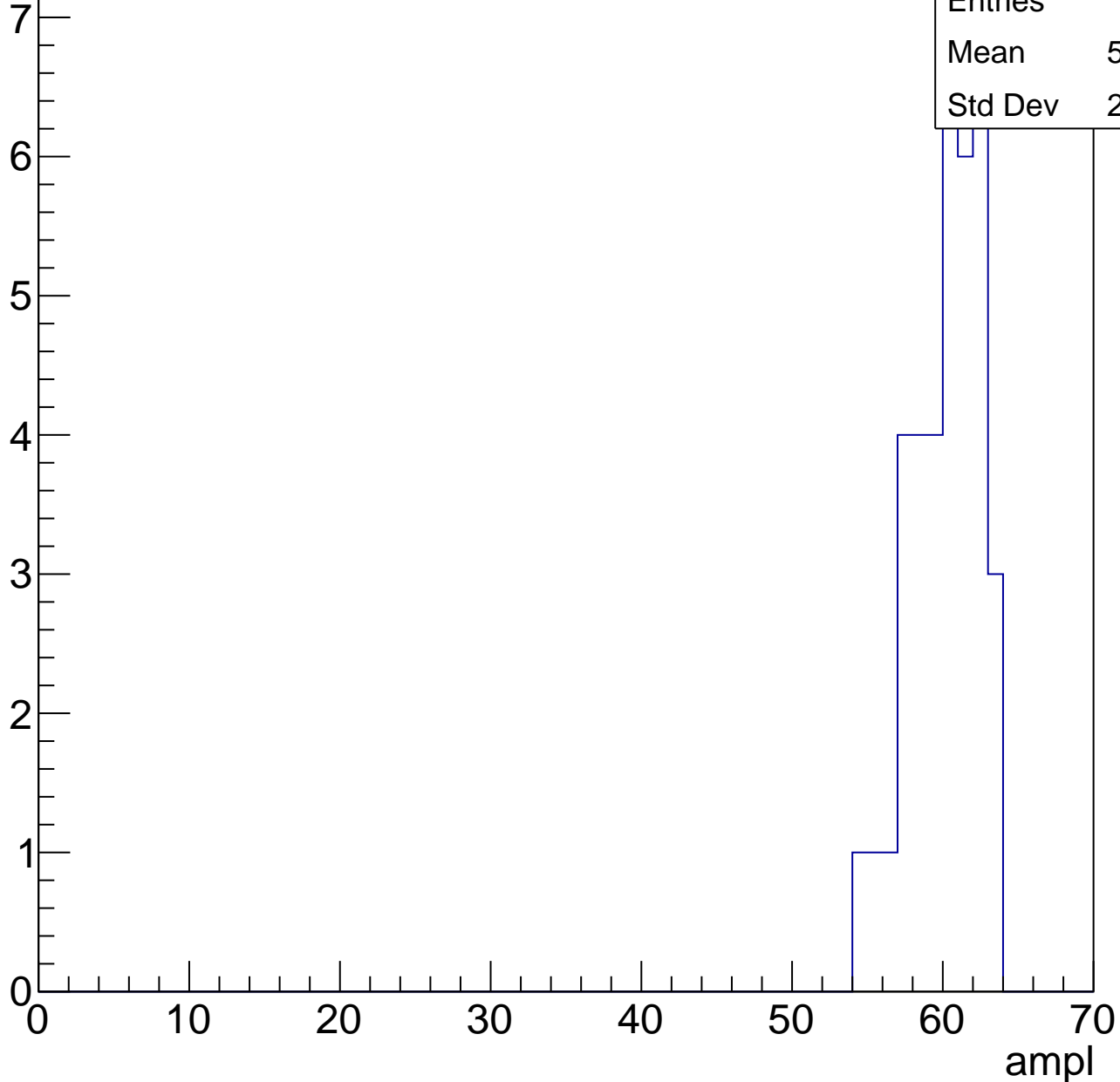
Entries	55
Mean	55.47
Std Dev	3.389



# B1L103S, U3-ch71, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



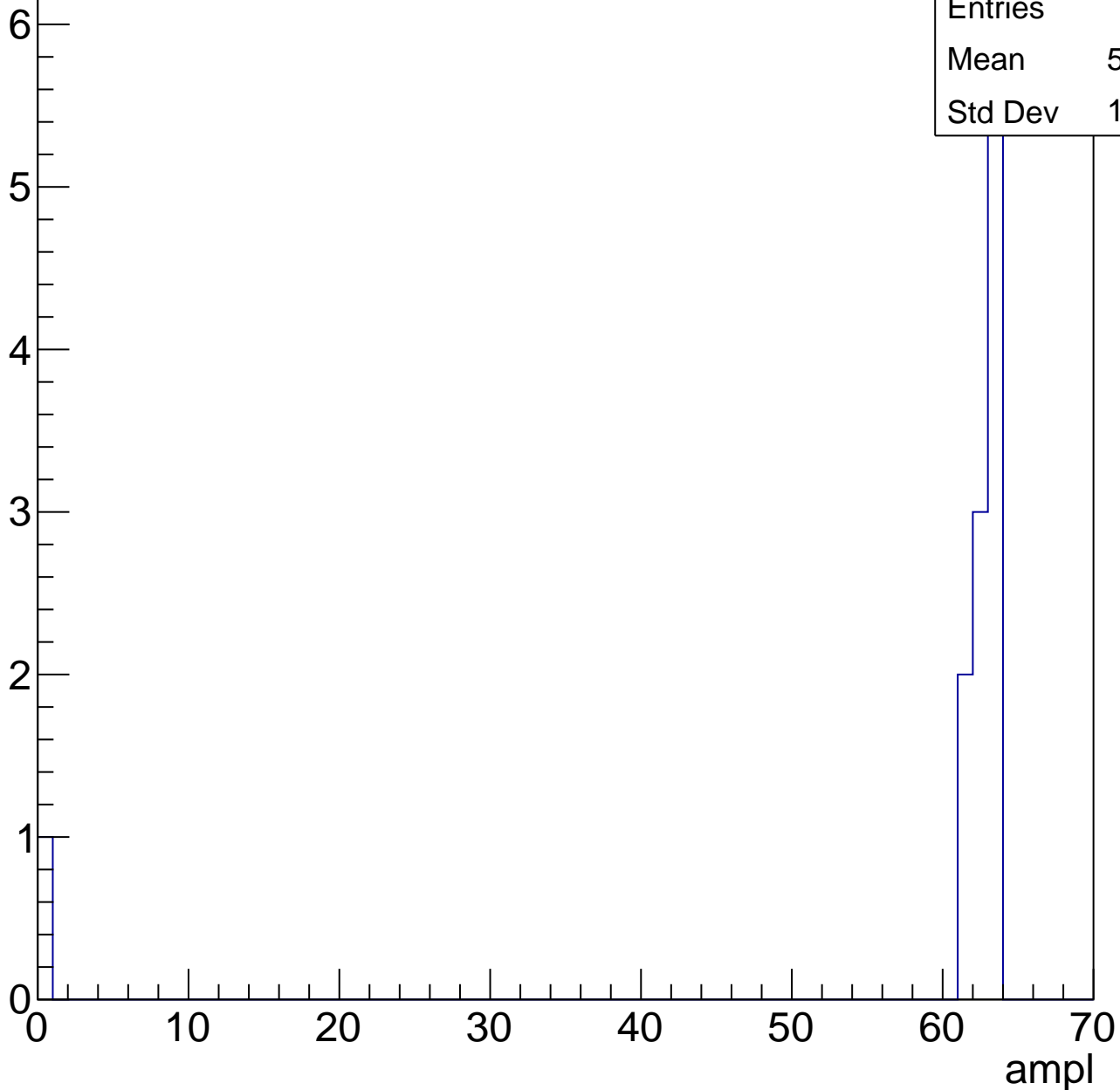
Entries	38
Mean	59.74
Std Dev	2.244

# B1L103S, U3-ch71, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	12
Mean	57.17
Std Dev	17.25





# B1L103S, U3-ch71, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	1.158
Std Dev	4.913

Entry



# B1L103S, U3-ch72, adc0

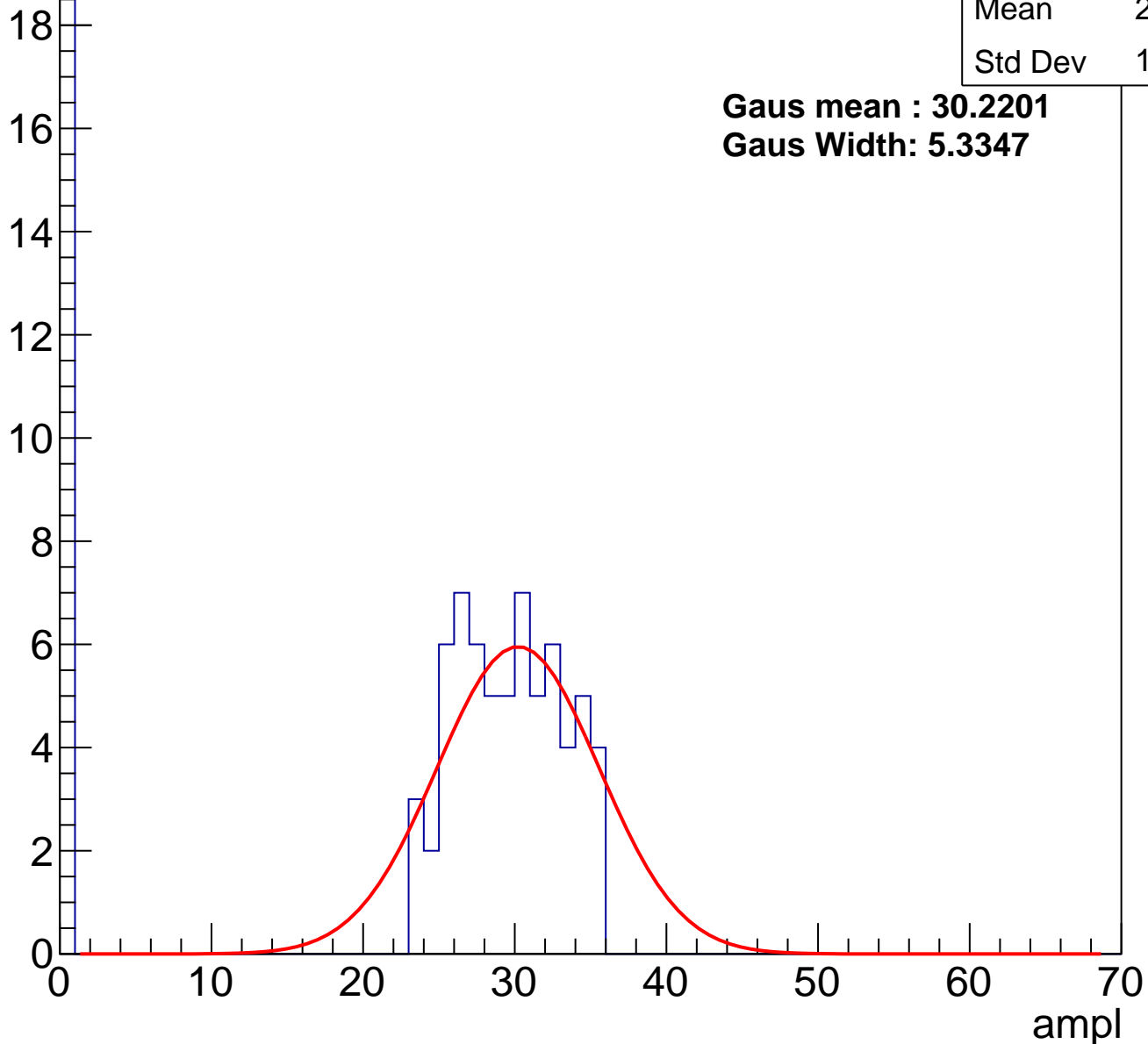
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	84
Mean	22.56
Std Dev	12.56

**Gaus mean : 30.2201**

**Gaus Width: 5.3347**

Entry



# B1L103S, U3-ch72, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	67
Mean	28.31
Std Dev	14.23

**Gaus mean : 35.8279**

**Gaus Width: 3.6609**

Entry

12

10

8

6

4

2

0

0

10

20

30

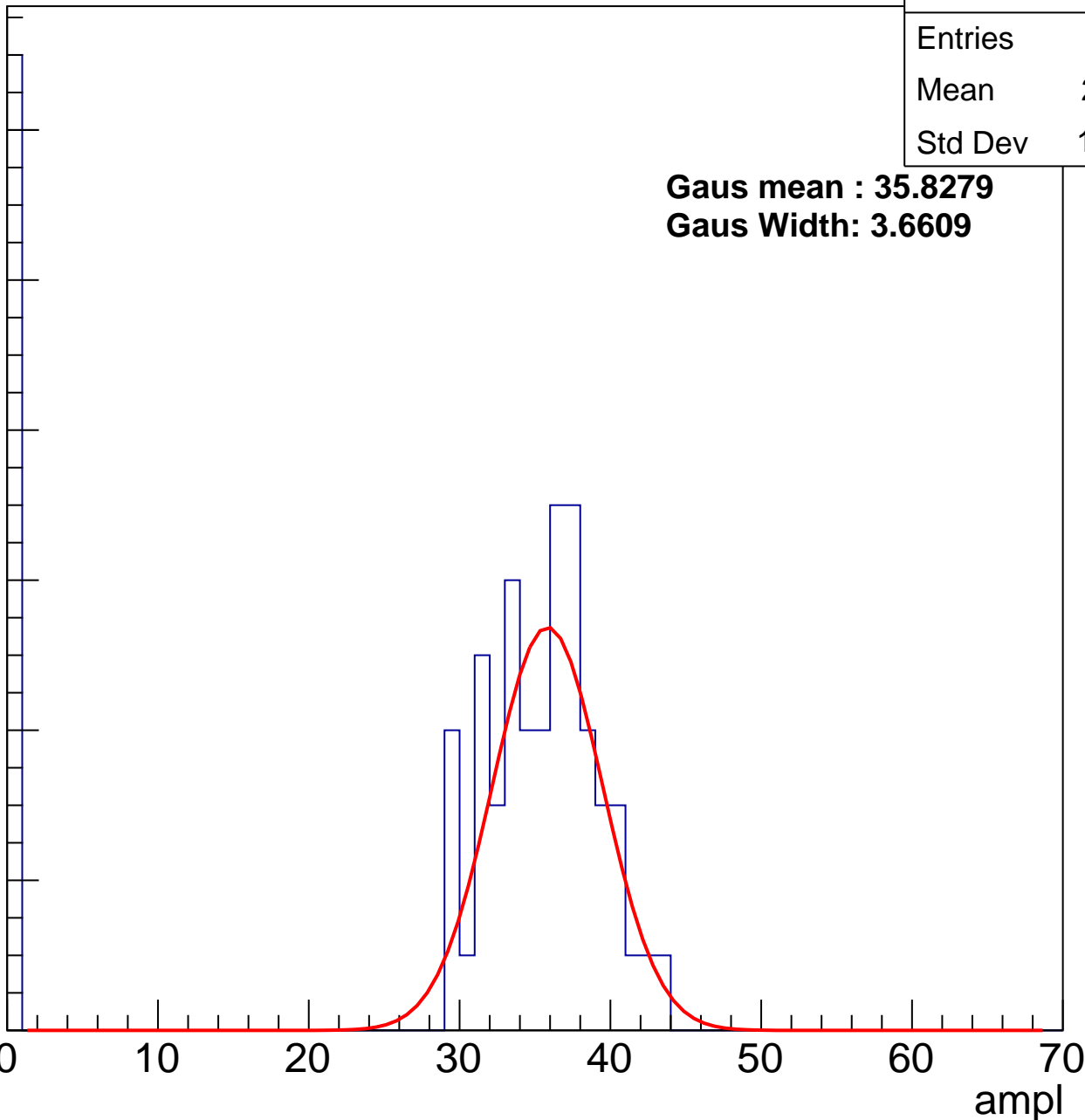
40

50

60

70

ampl



# B1L103S, U3-ch72, adc2

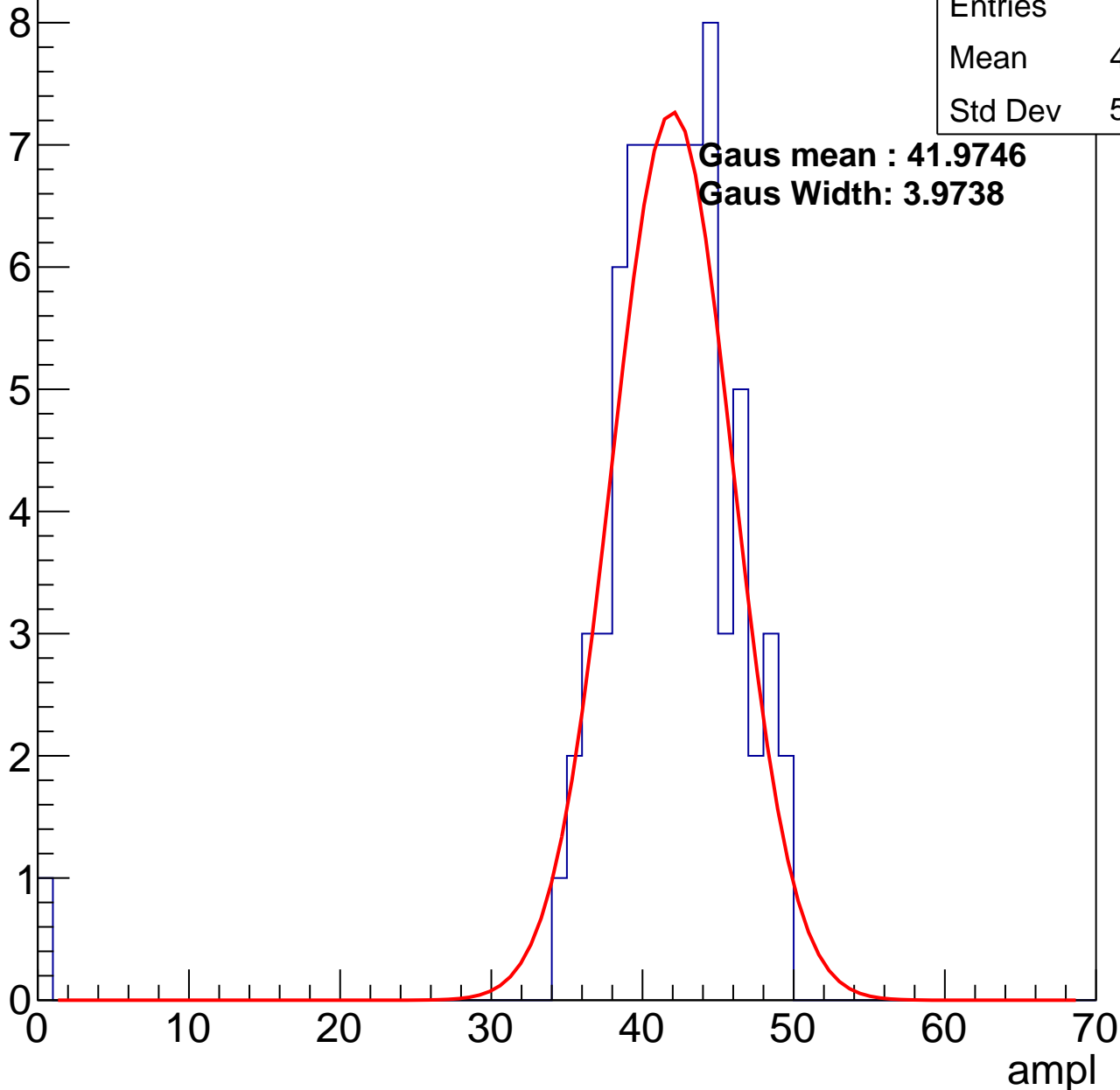
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	74
Mean	41.07
Std Dev	5.974

**Gaus mean : 41.9746**

**Gaus Width: 3.9738**

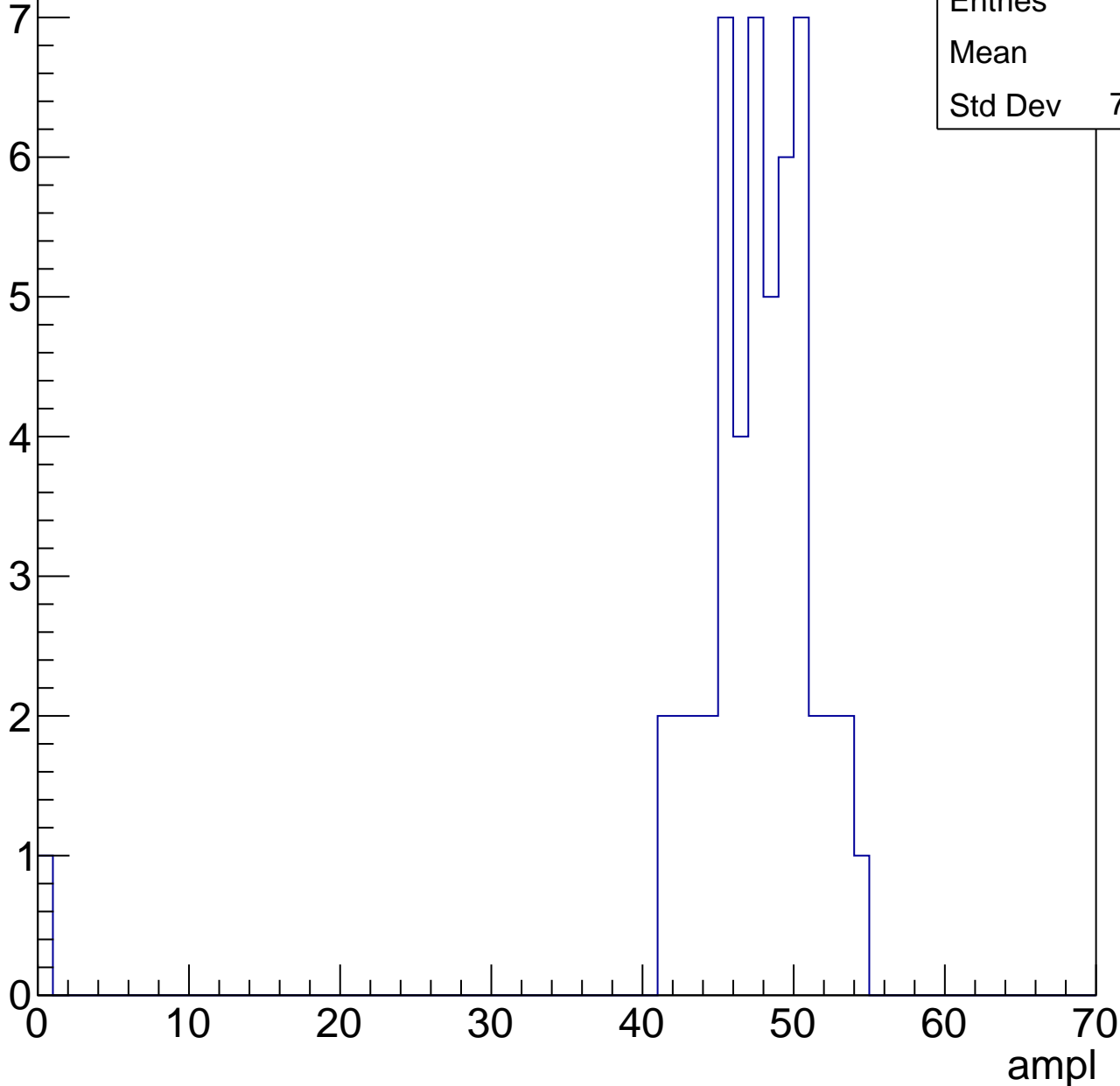


# B1L103S, U3-ch72, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	52
Mean	46.5
Std Dev	7.199

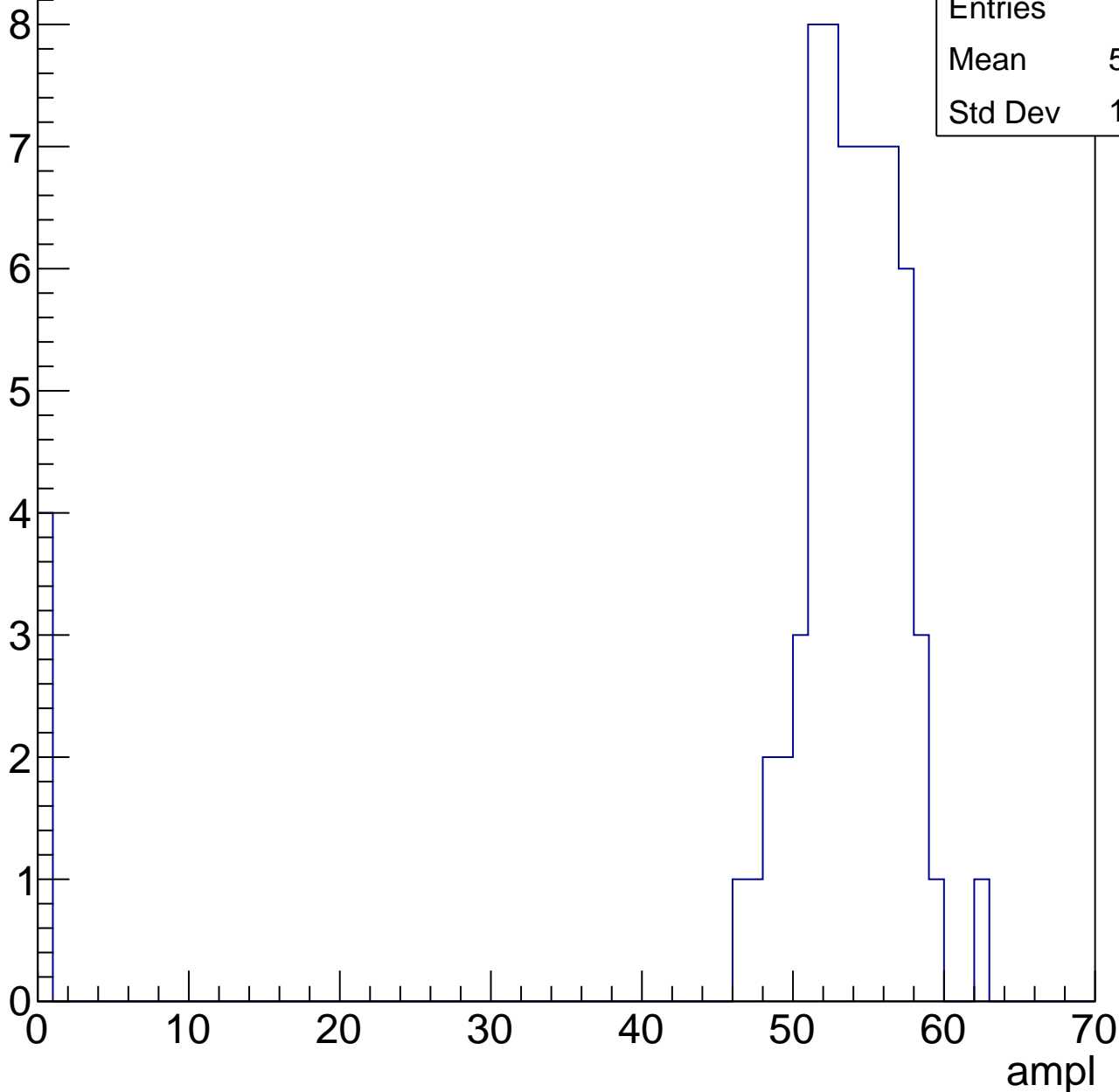


# B1L103S, U3-ch72, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	50.35
Std Dev	12.94

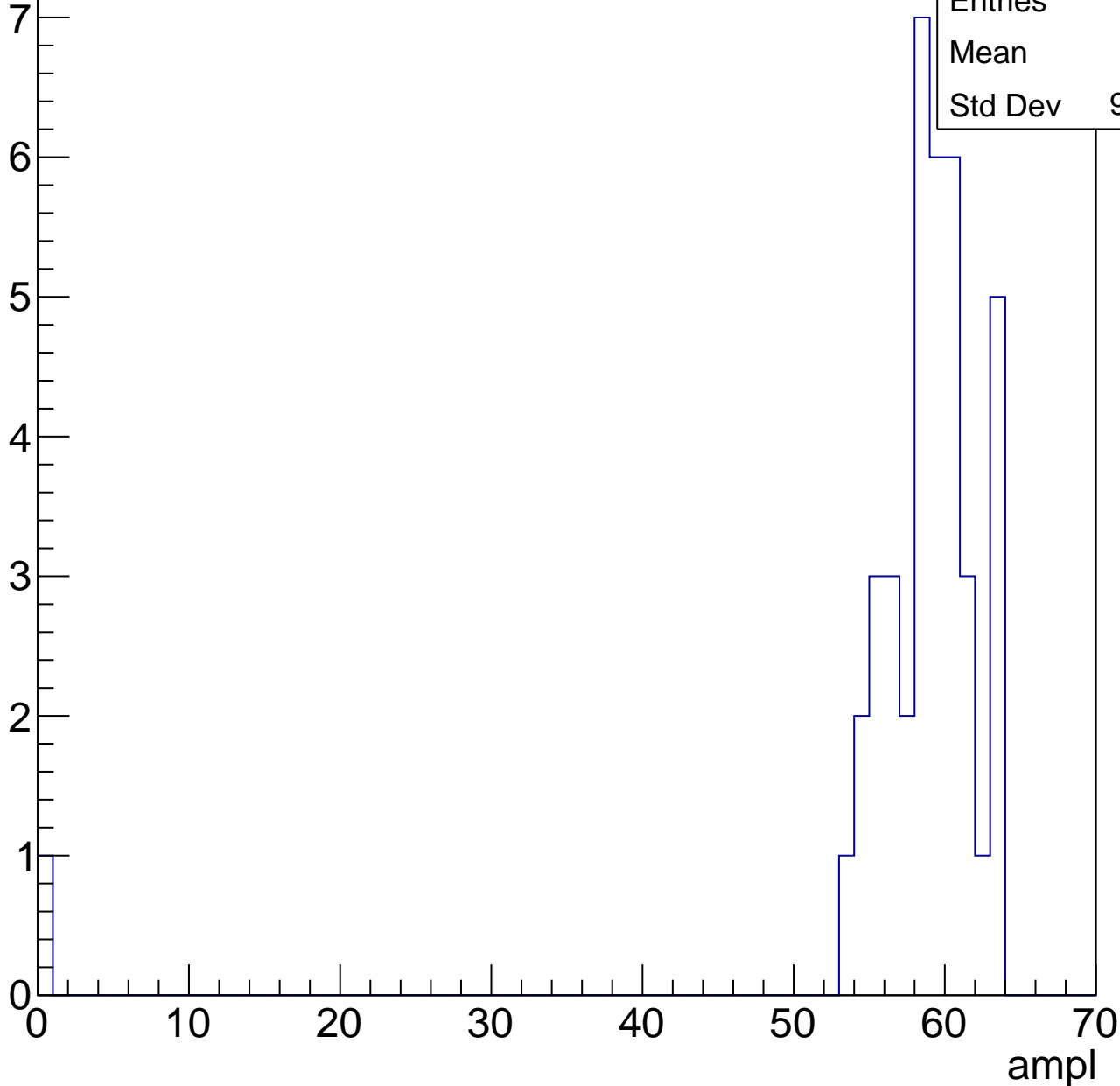


# B1L103S, U3-ch72, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	40
Mean	57.2
Std Dev	9.532

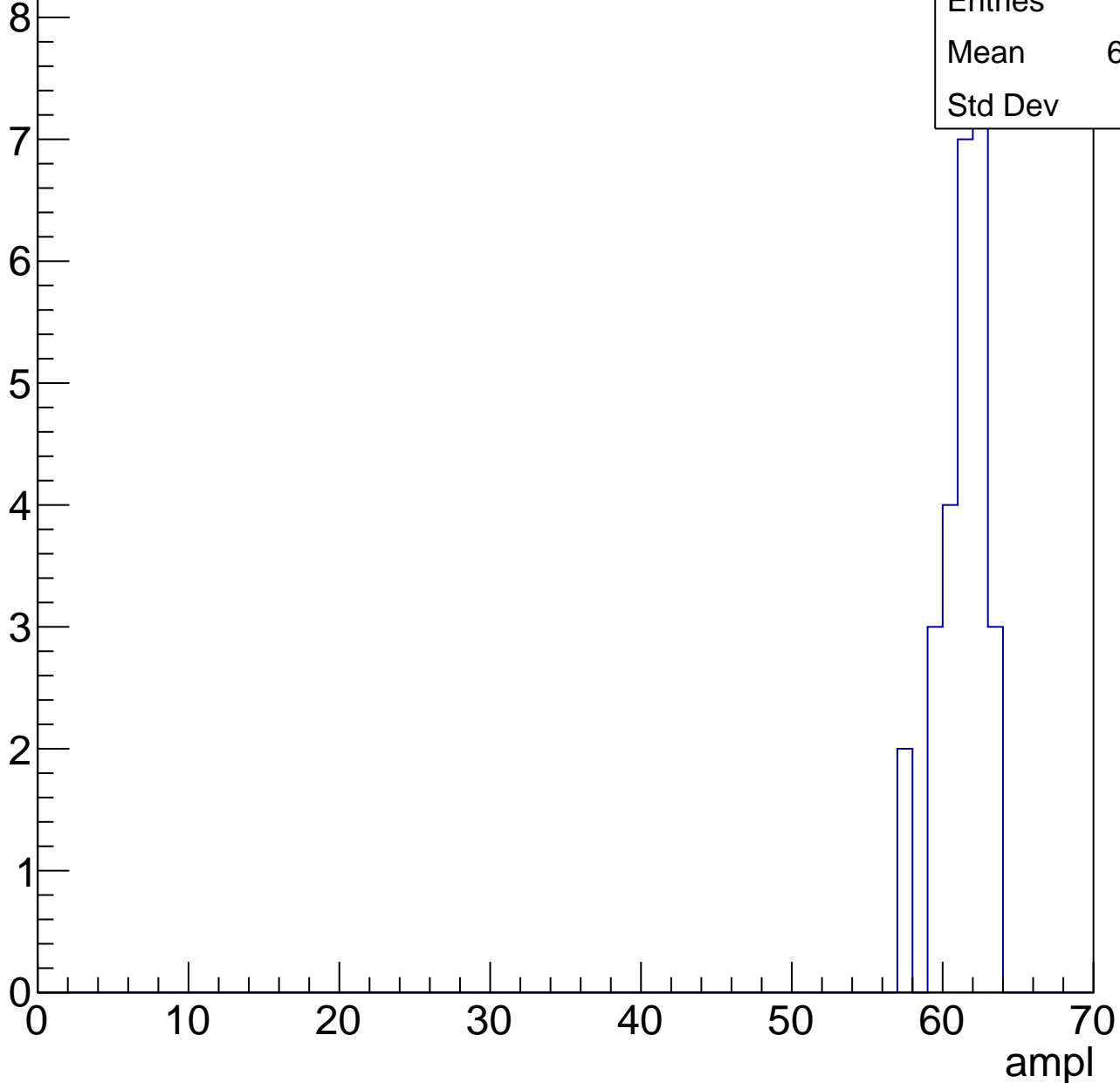


# B1L103S, U3-ch72, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	27
Mean	60.85
Std Dev	1.58

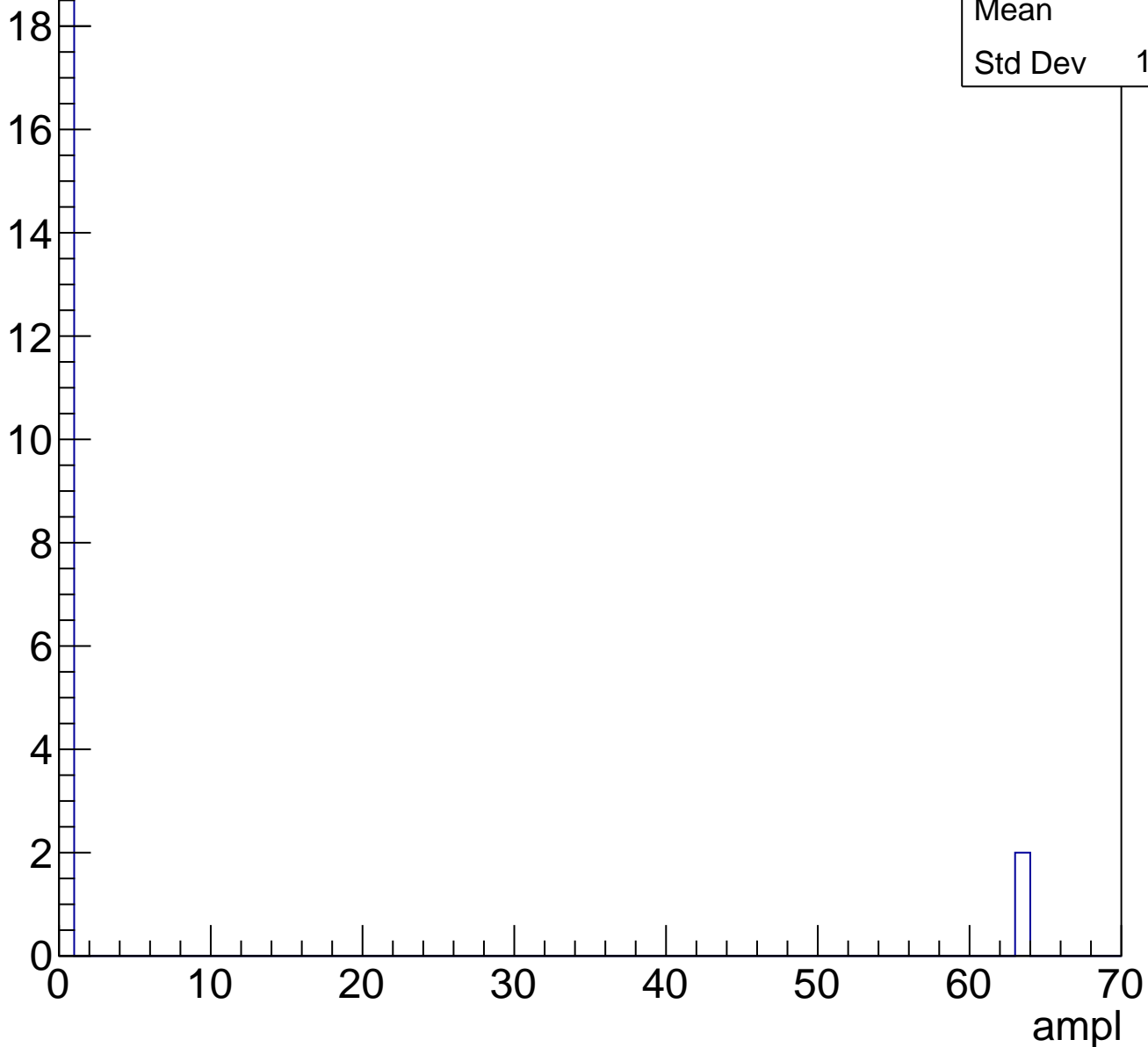




# B1L103S, U3-ch72, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U3-ch73, adc0

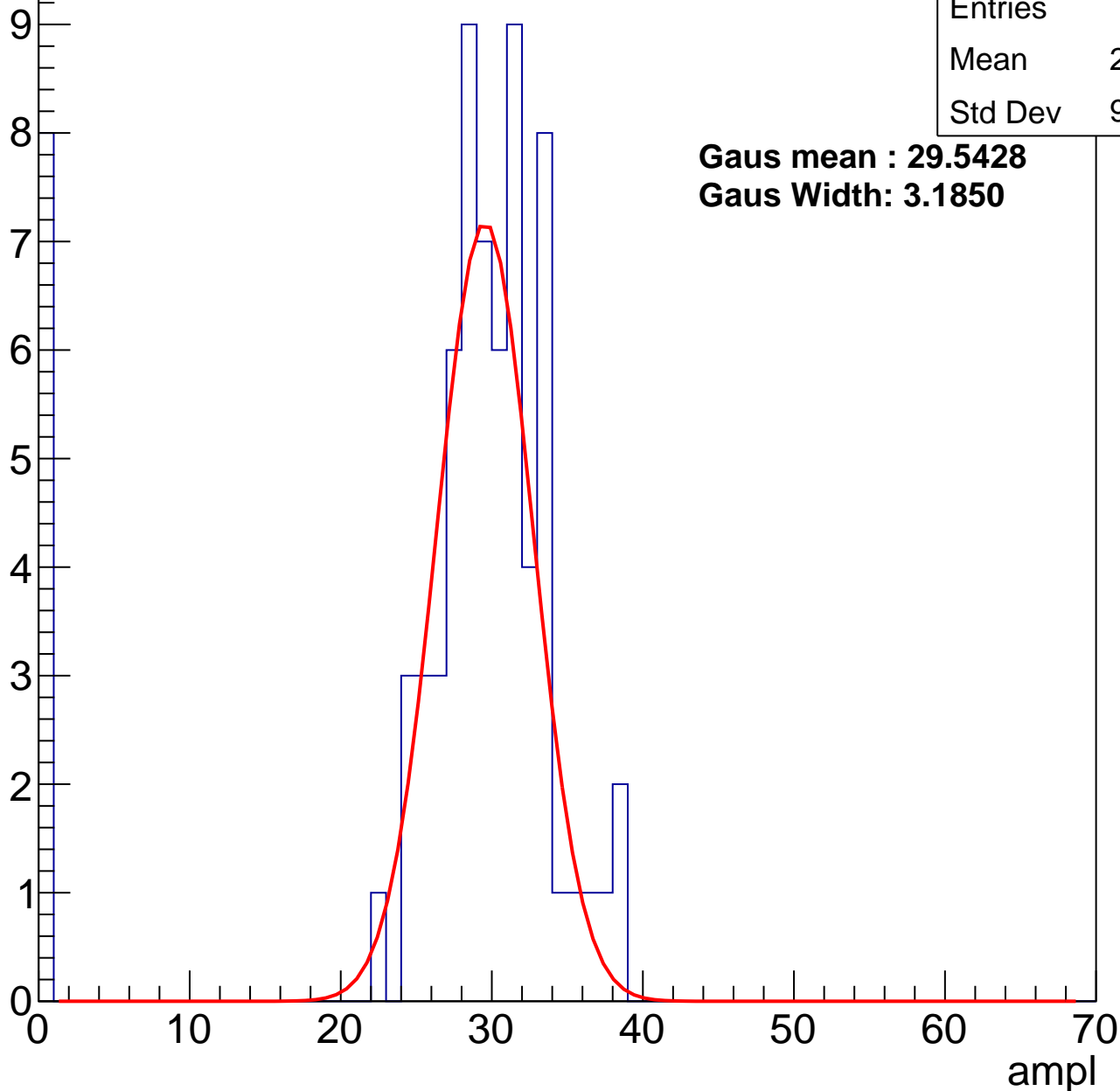
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	26.48
Std Dev	9.819

**Gaus mean : 29.5428**

**Gaus Width: 3.1850**



# B1L103S, U3-ch73, adc1

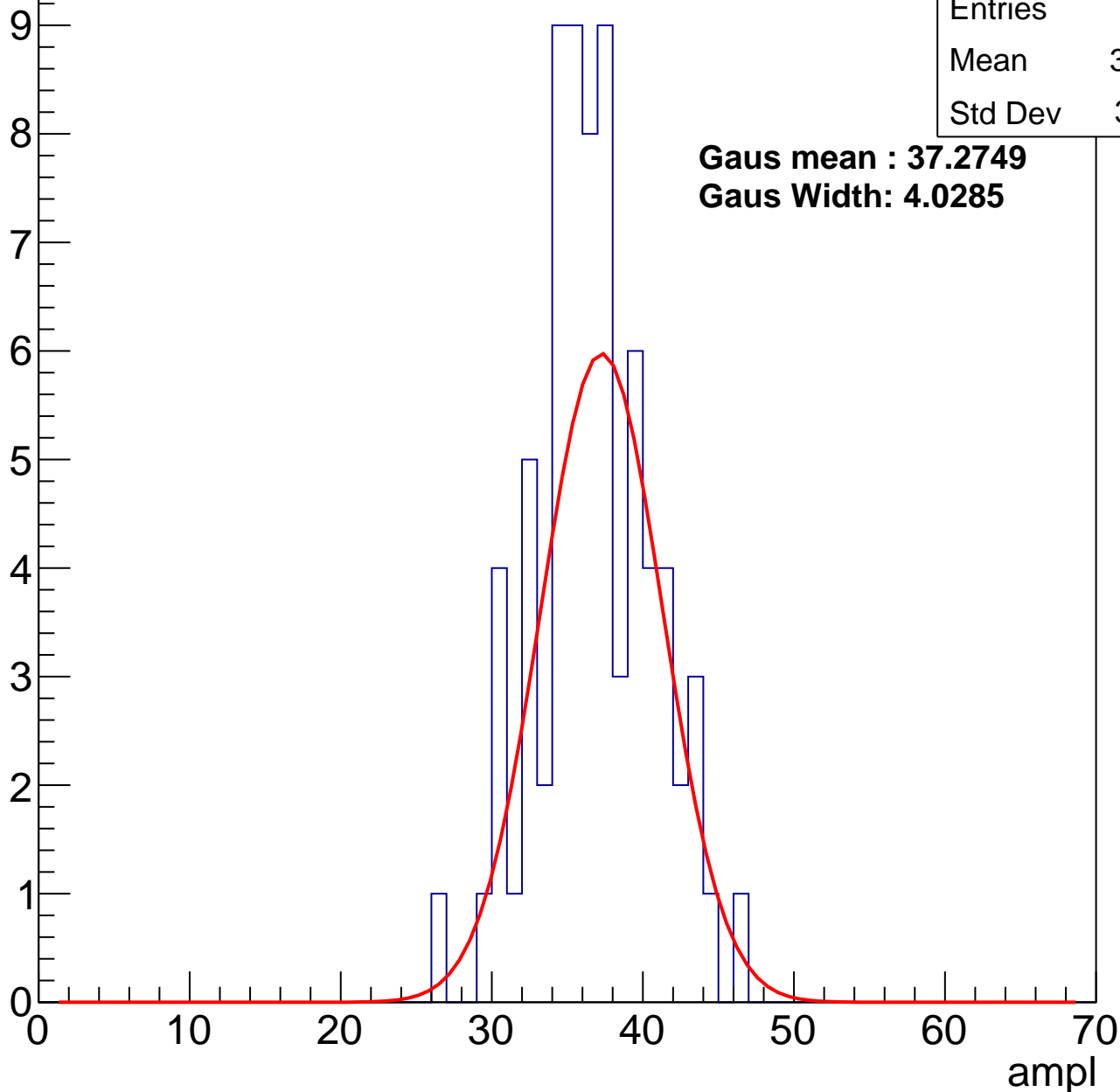
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	36.29
Std Dev	3.841

**Gaus mean : 37.2749**

**Gaus Width: 4.0285**



# B1L103S, U3-ch73, adc2

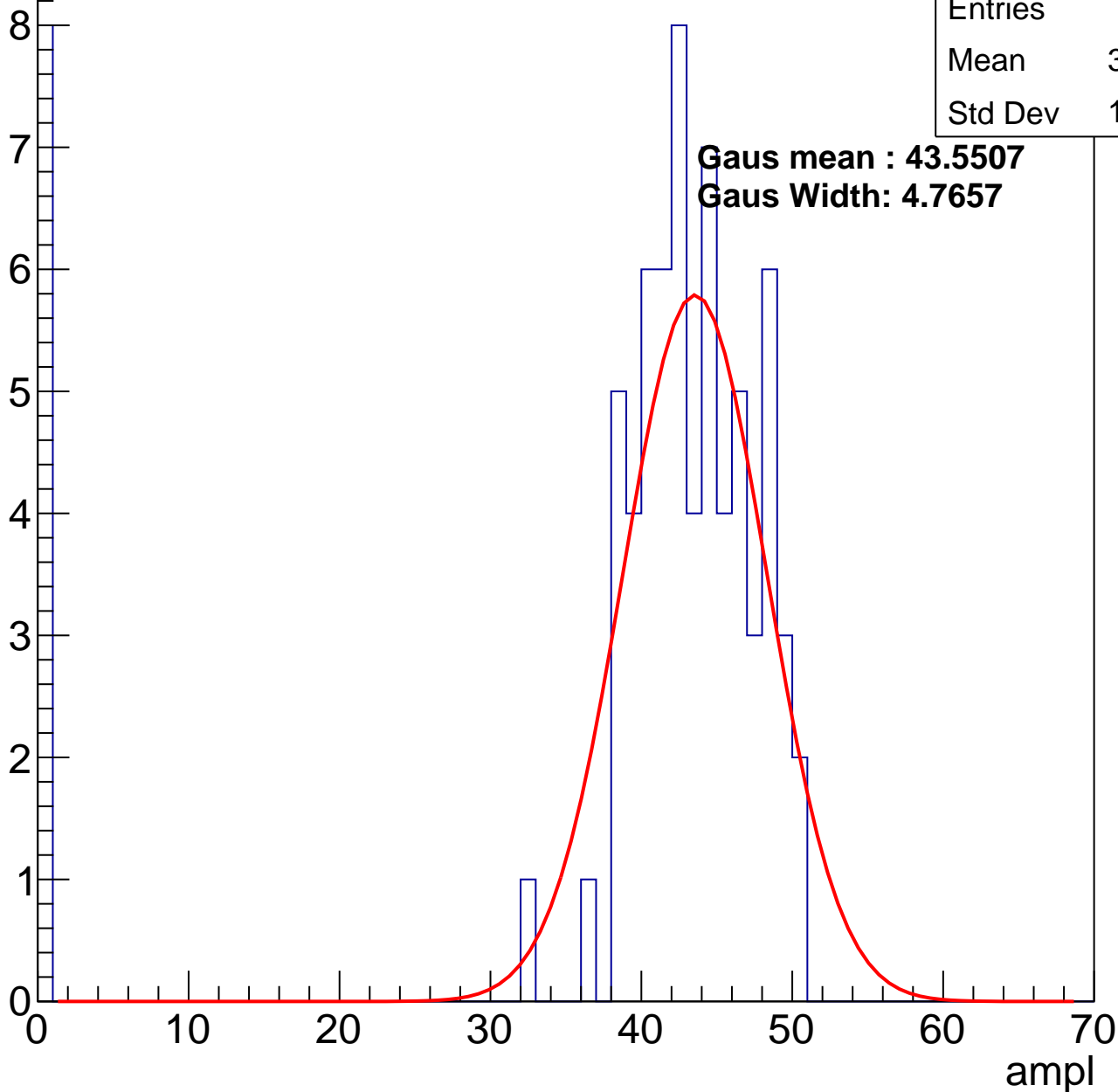
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	38.38
Std Dev	13.92

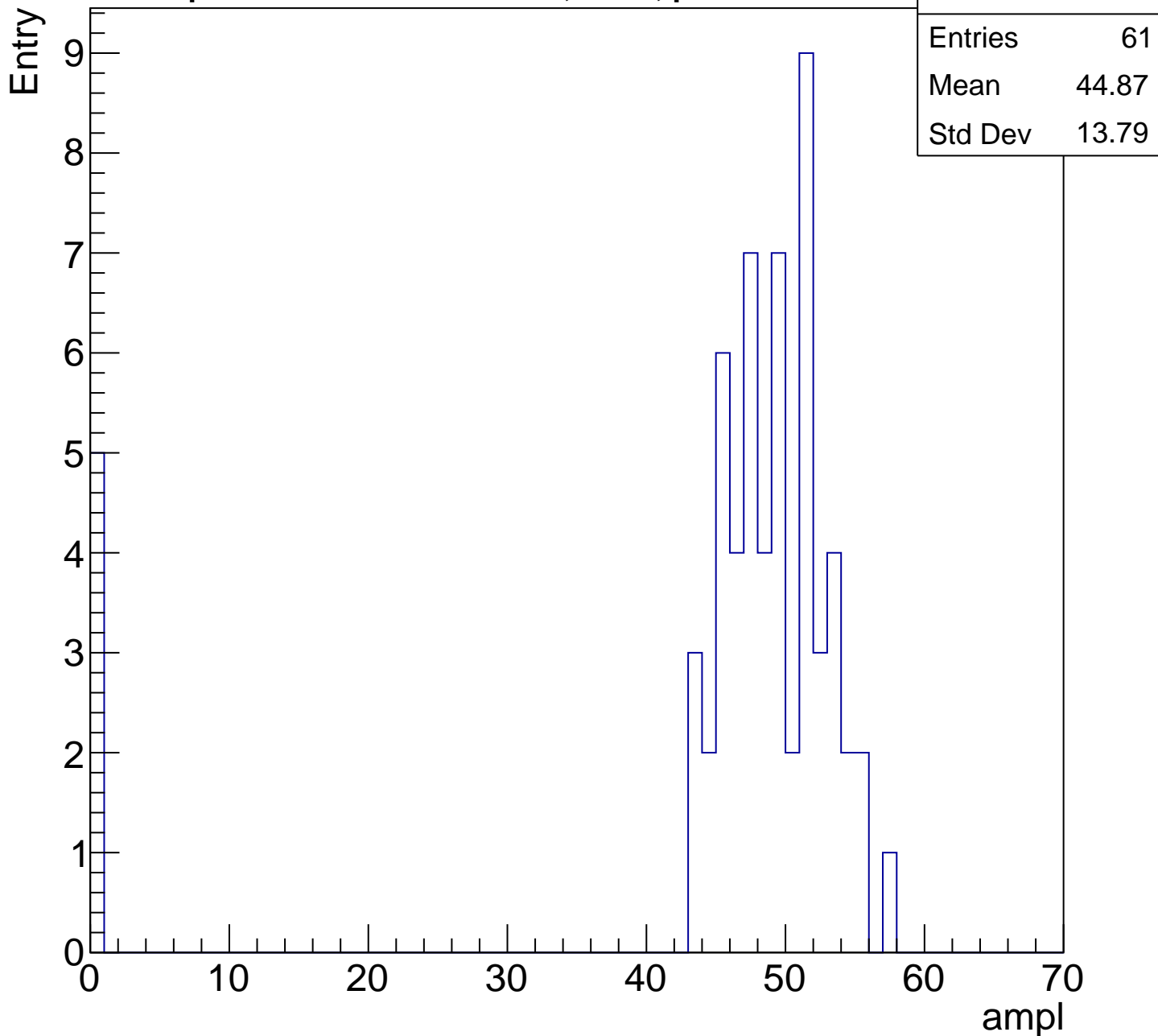
**Gaus mean : 43.5507**

**Gaus Width: 4.7657**



# B1L103S, U3-ch73, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

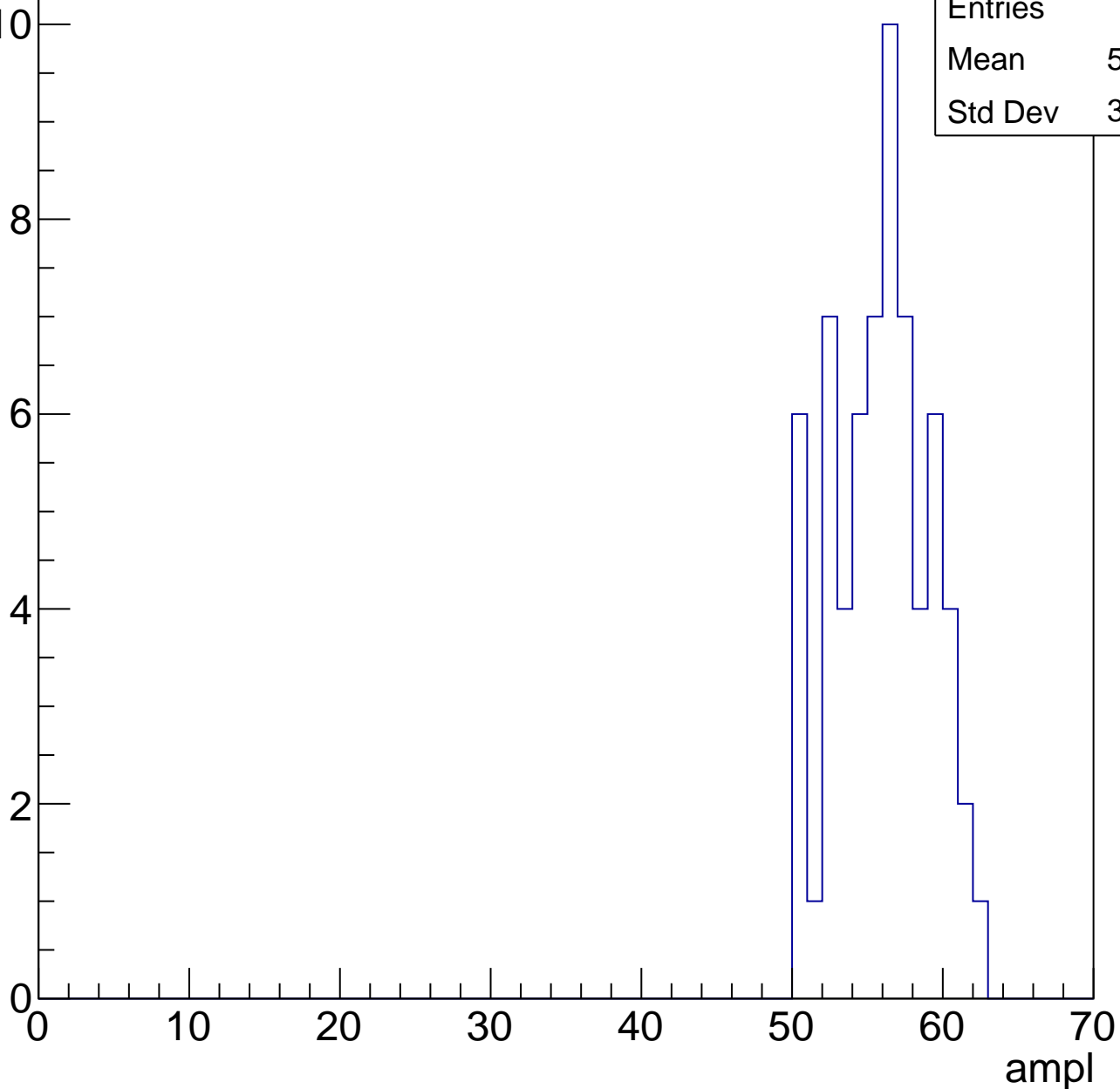


# B1L103S, U3-ch73, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

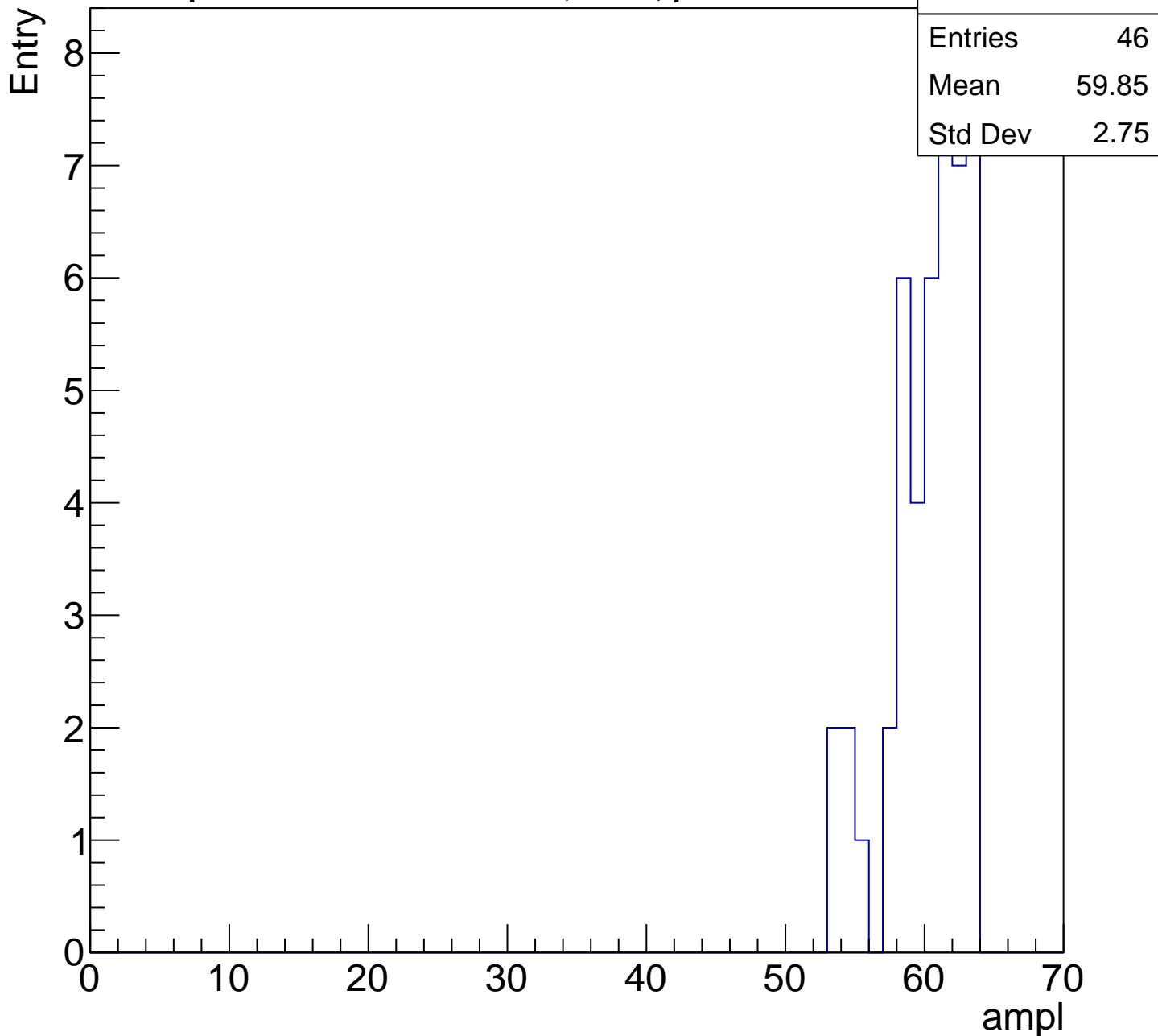
Entry

Entries	65
Mean	55.46
Std Dev	3.109



# B1L103S, U3-ch73, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U3-ch73, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	46.75
Std Dev	26.99

ampl

0 10 20 30 40 50 60 70

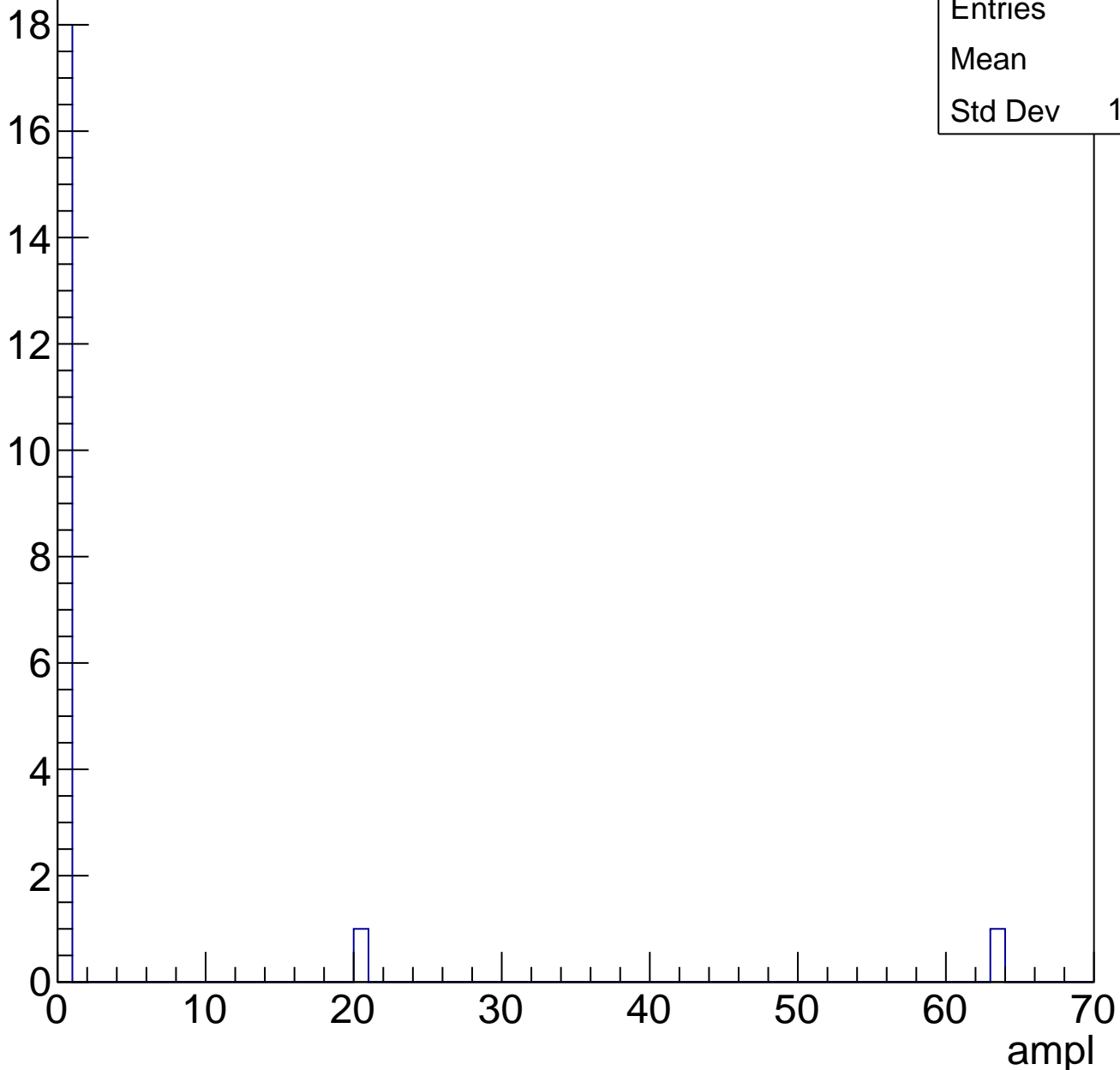


# B1L103S, U3-ch73, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	4.15
Std Dev	14.19

Entry



# B1L103S, U3-ch74, adc0

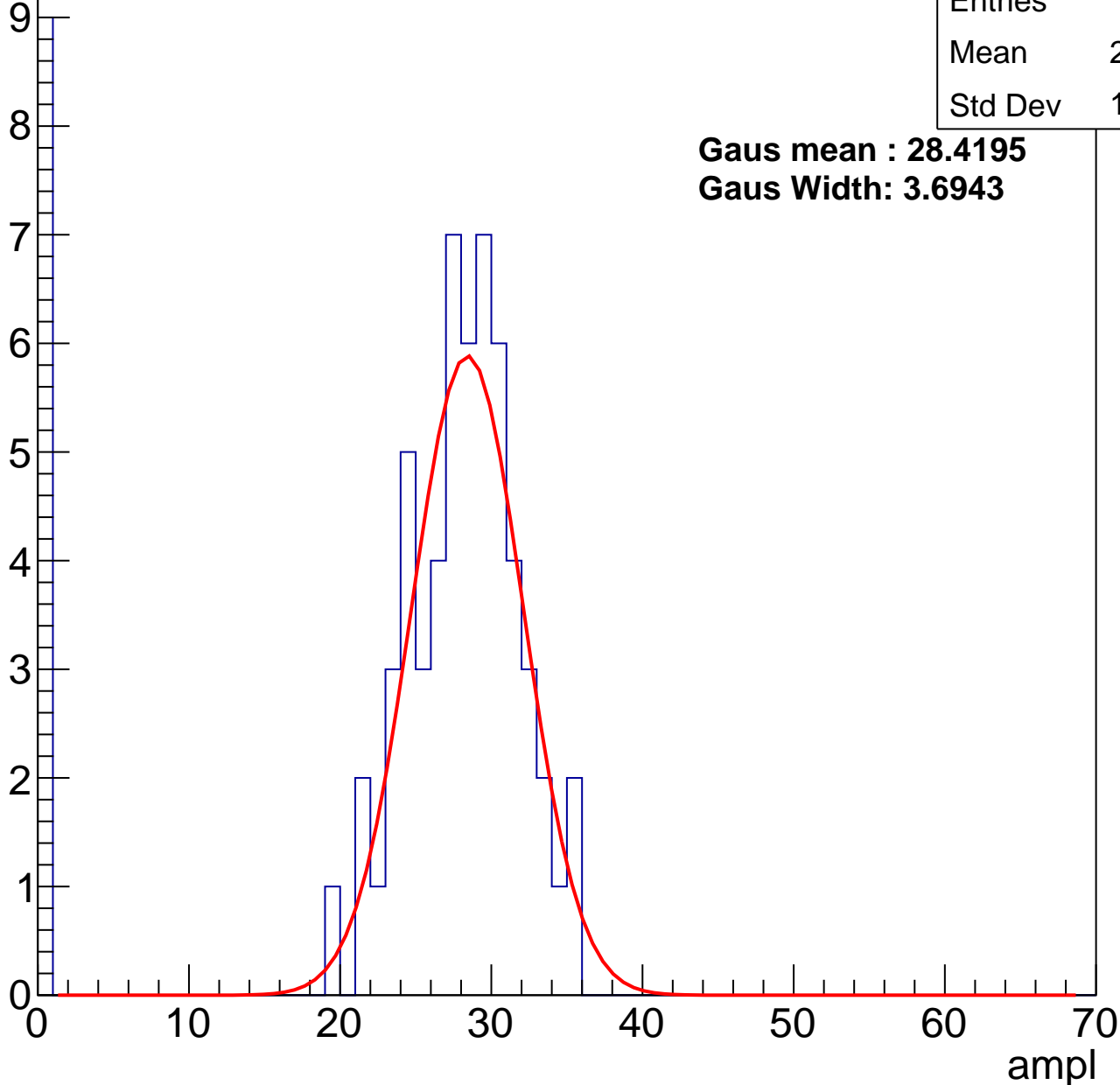
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	23.95
Std Dev	10.07

**Gaus mean : 28.4195**

**Gaus Width: 3.6943**



# B1L103S, U3-ch74, adc1

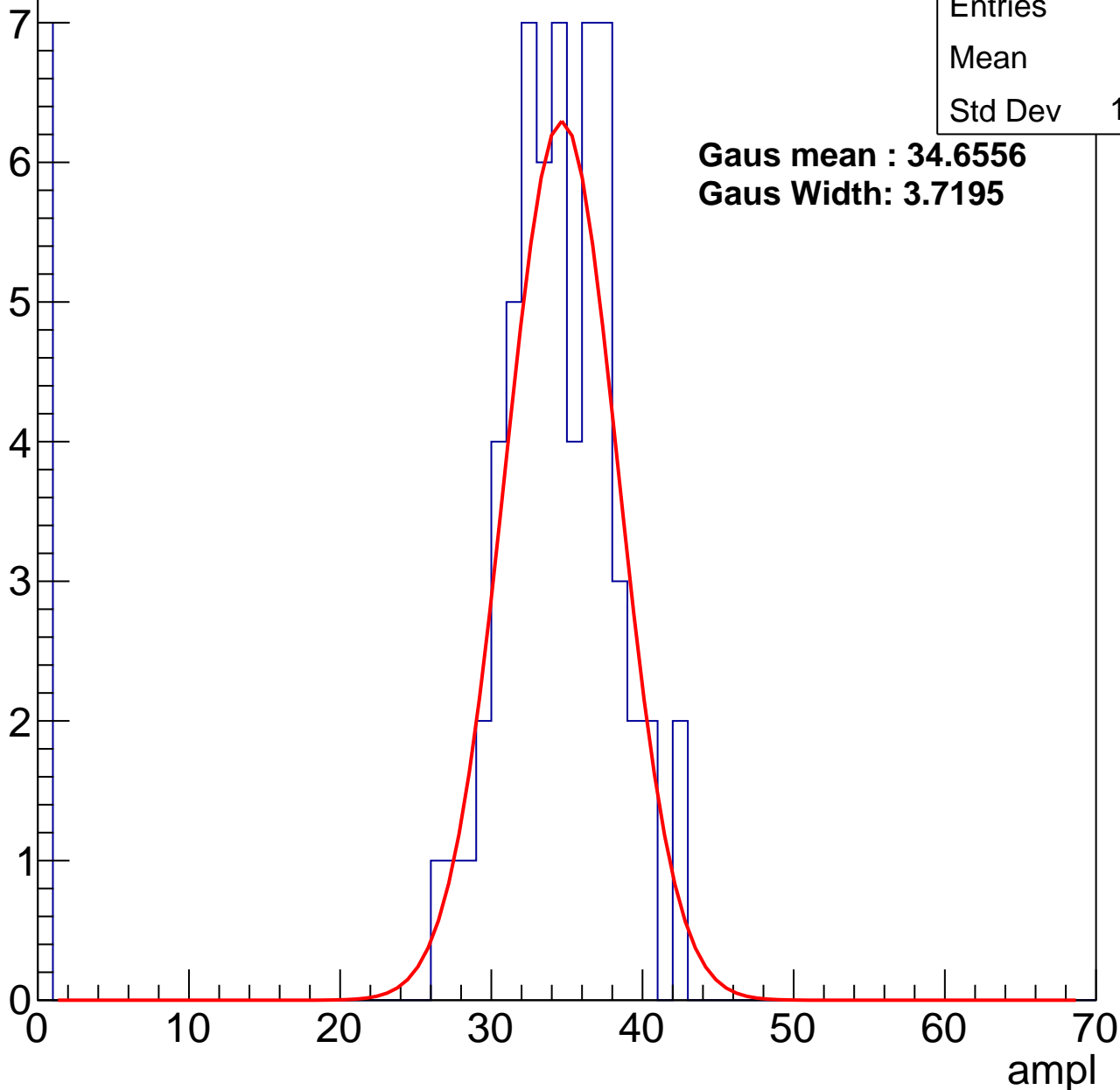
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	30.6
Std Dev	10.88

**Gaus mean : 34.6556**

**Gaus Width: 3.7195**



# B1L103S, U3-ch74, adc2

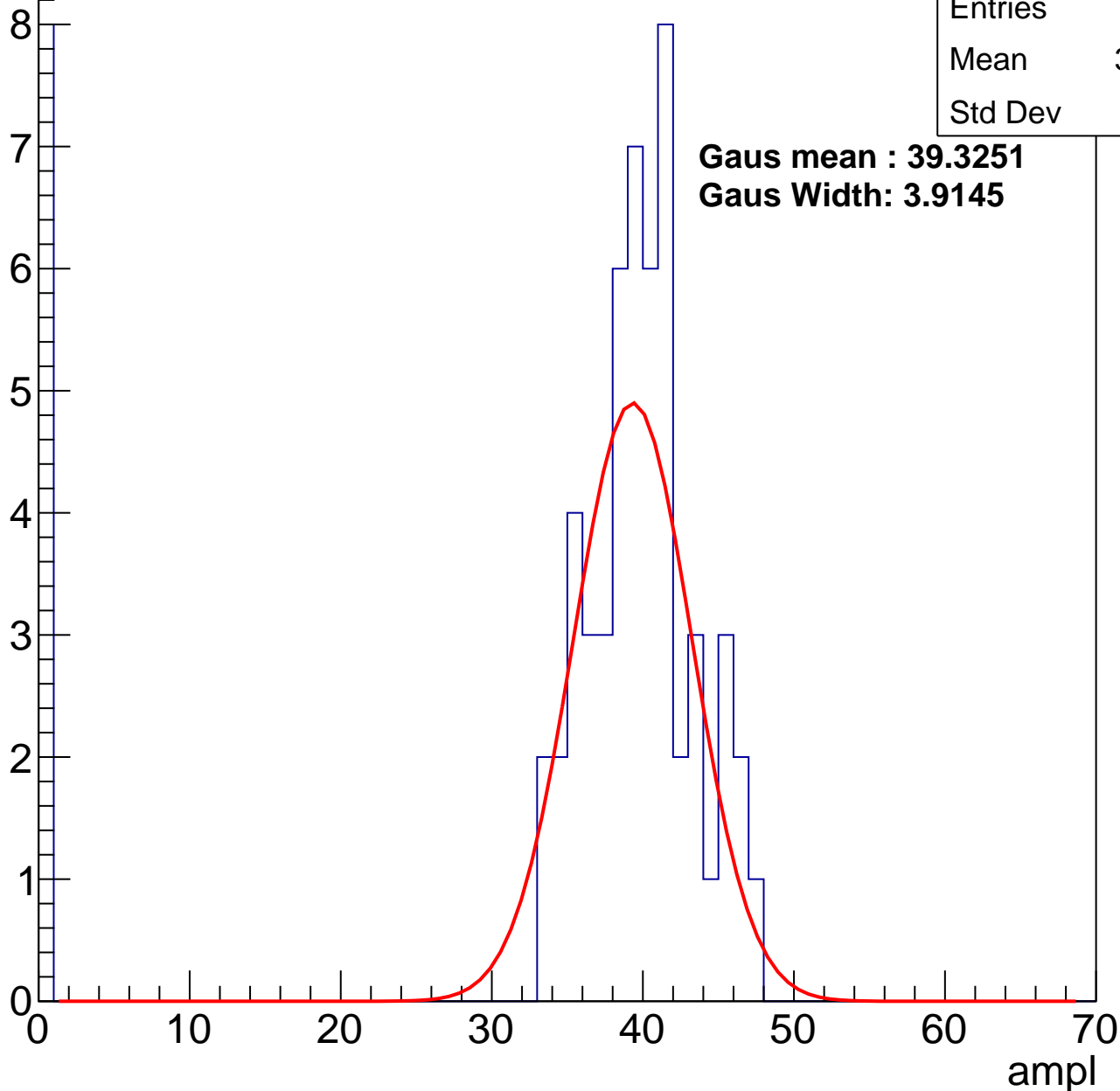
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	34.31
Std Dev	13.7

**Gaus mean : 39.3251**

**Gaus Width: 3.9145**

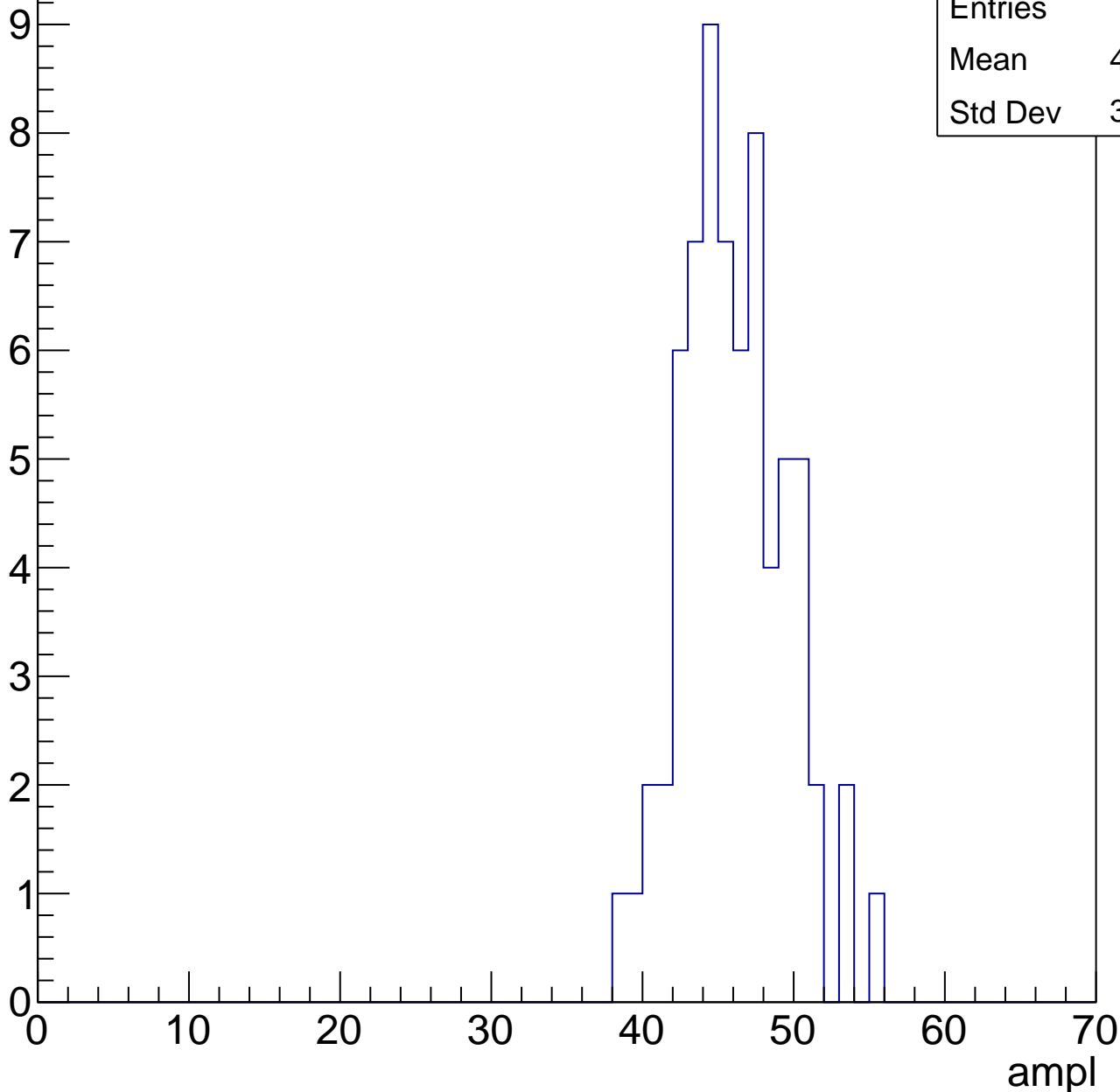


# B1L103S, U3-ch74, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	45.66
Std Dev	3.445

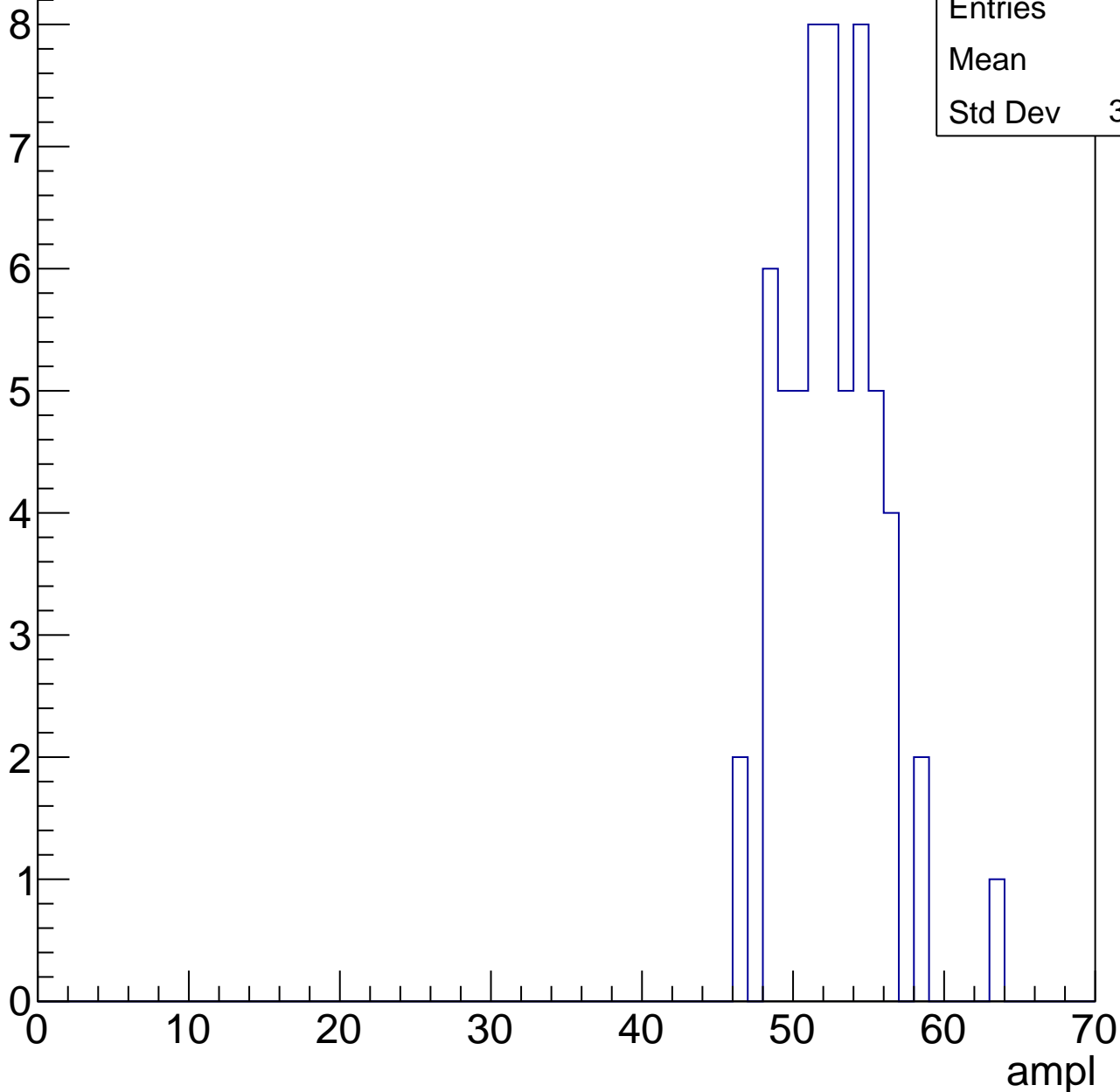


# B1L103S, U3-ch74, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	52.1
Std Dev	3.134

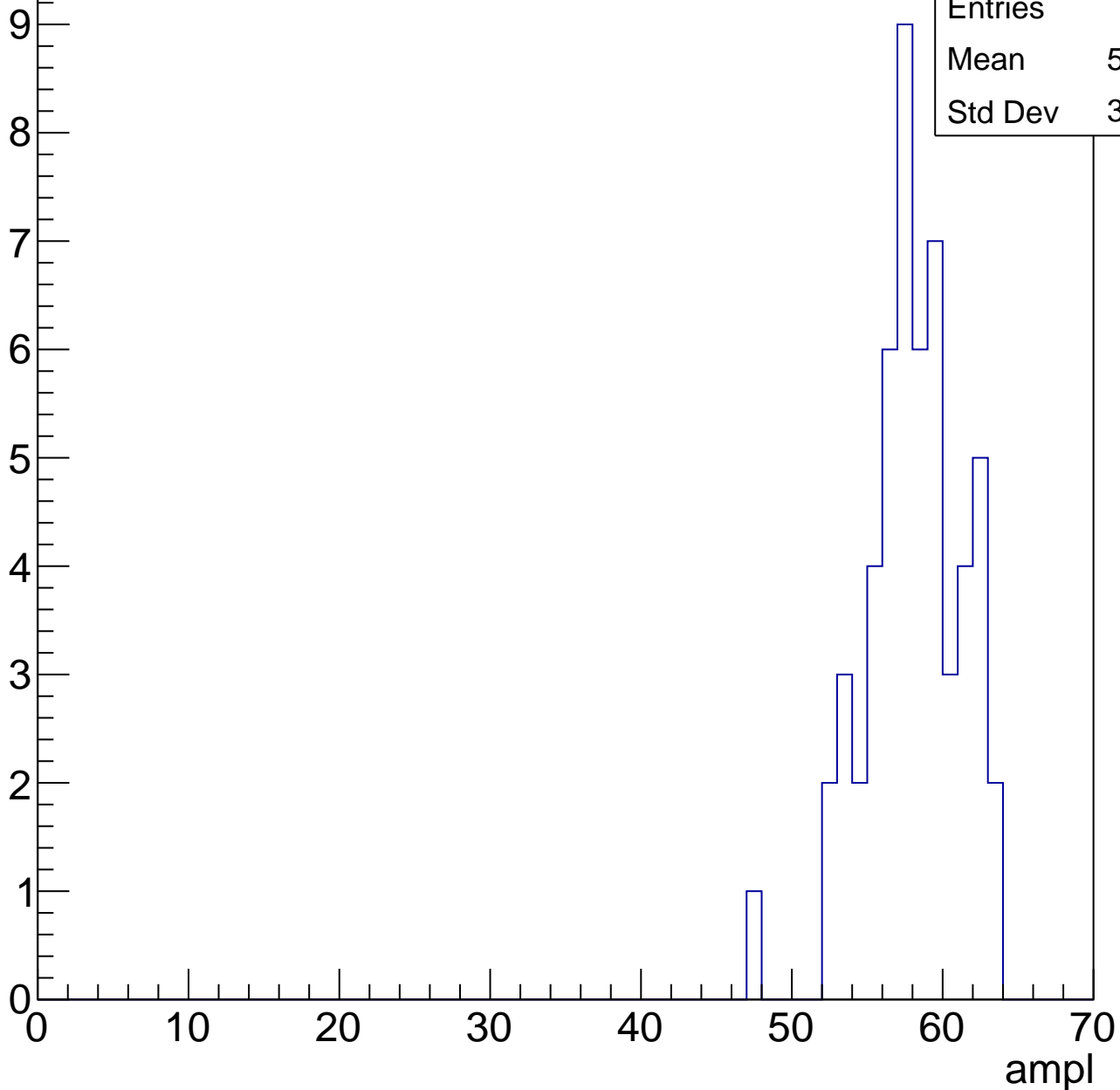


# B1L103S, U3-ch74, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	54
Mean	57.56
Std Dev	3.172

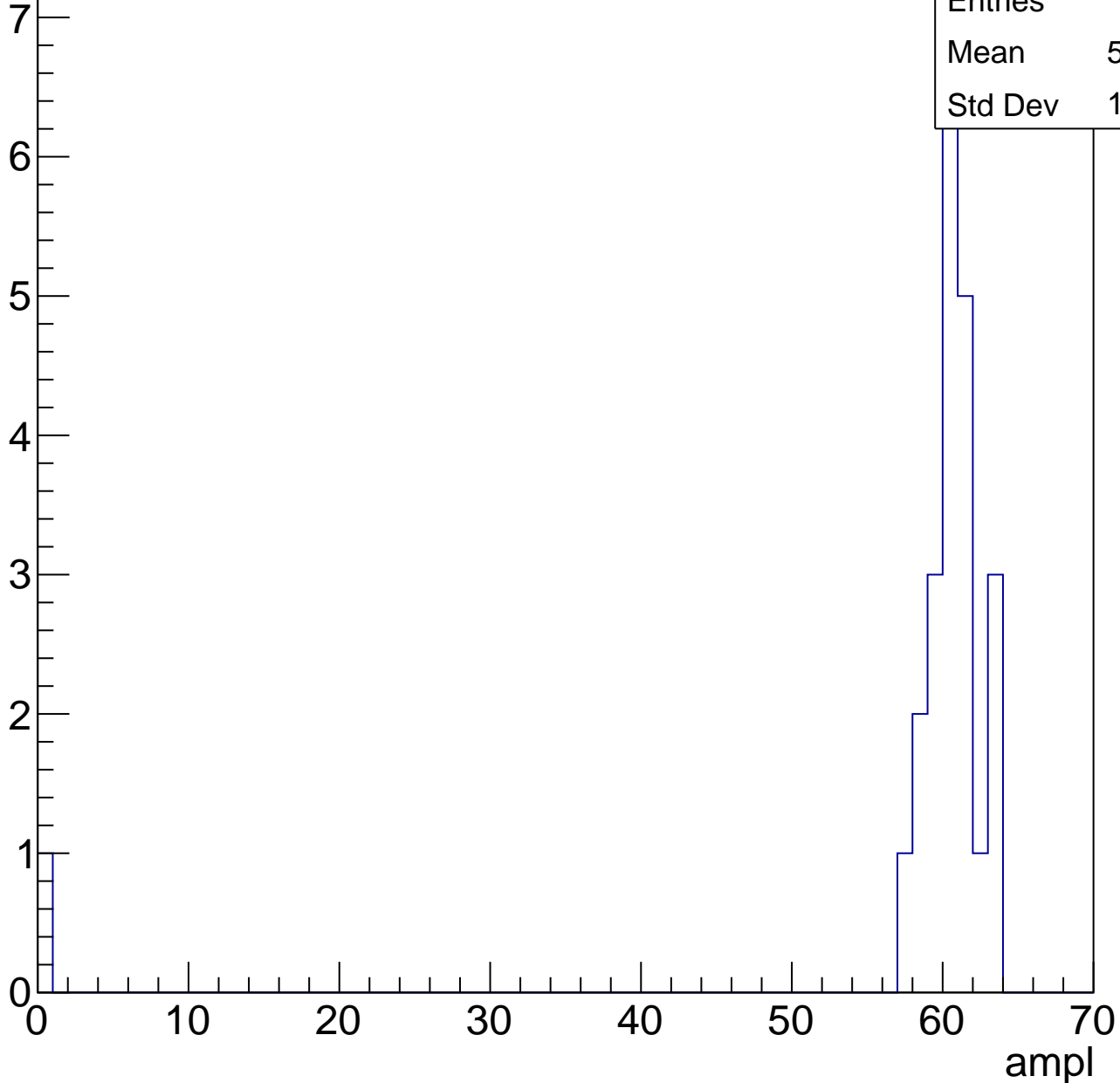


# B1L103S, U3-ch74, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	23
Mean	57.65
Std Dev	12.39



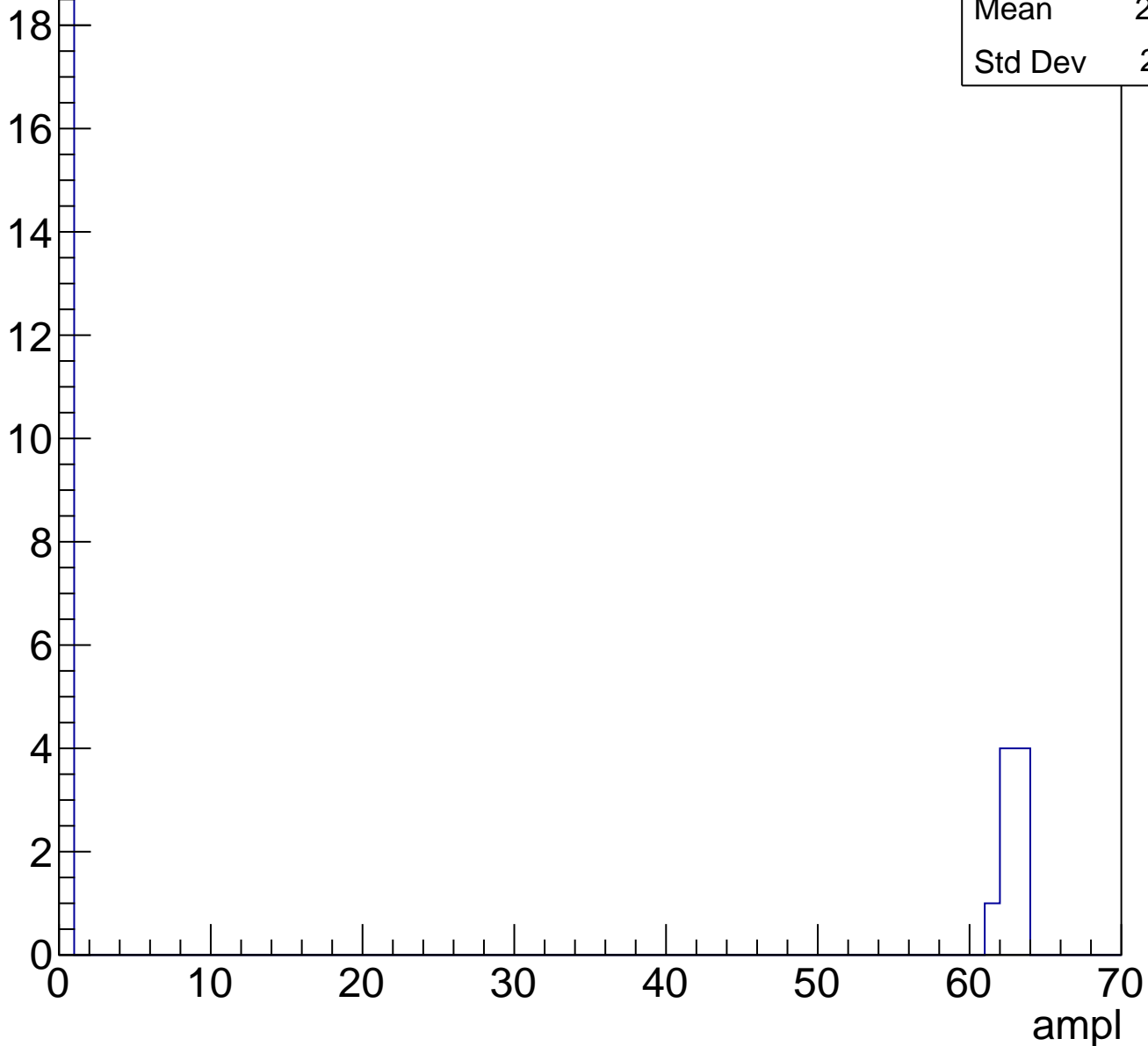


# B1L103S, U3-ch74, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	28
Mean	20.04
Std Dev	29.11

Entry



# B1L103S, U3-ch75, adc0

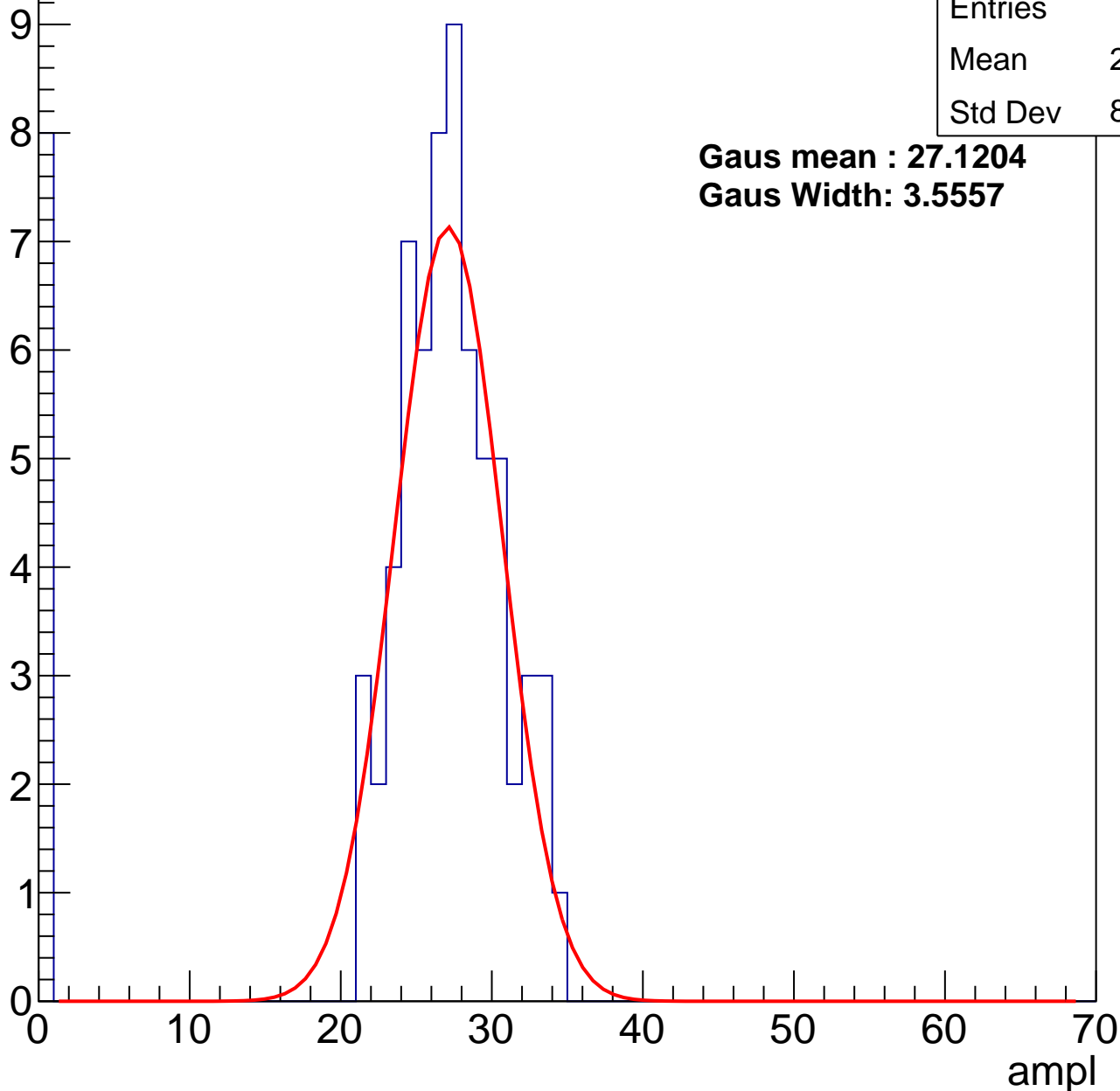
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	72
Mean	23.92
Std Dev	8.975

**Gaus mean : 27.1204**

**Gaus Width: 3.5557**



# B1L103S, U3-ch75, adc1

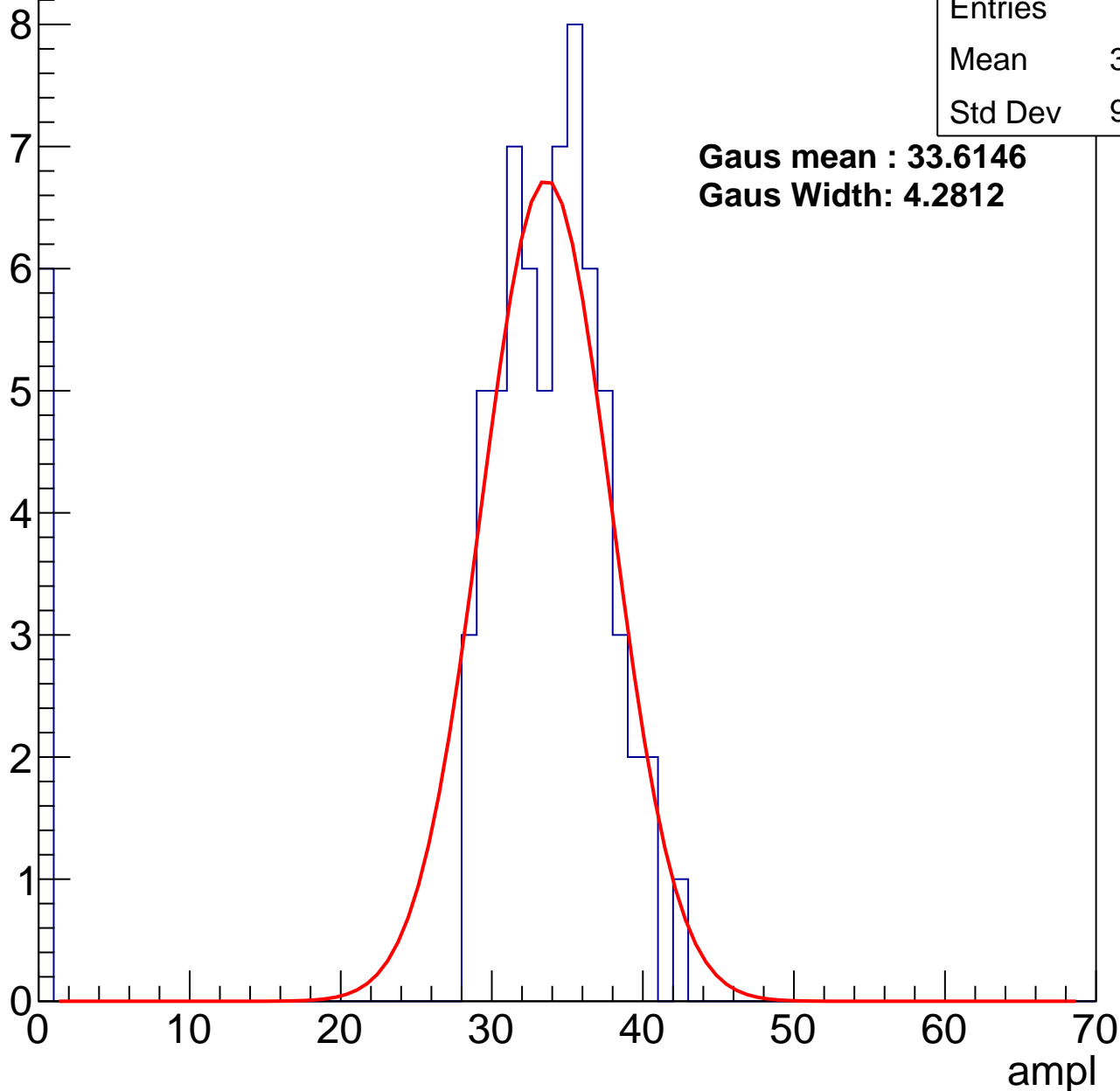
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	71
Mean	30.79
Std Dev	9.872

**Gaus mean : 33.6146**

**Gaus Width: 4.2812**



# B1L103S, U3-ch75, adc2

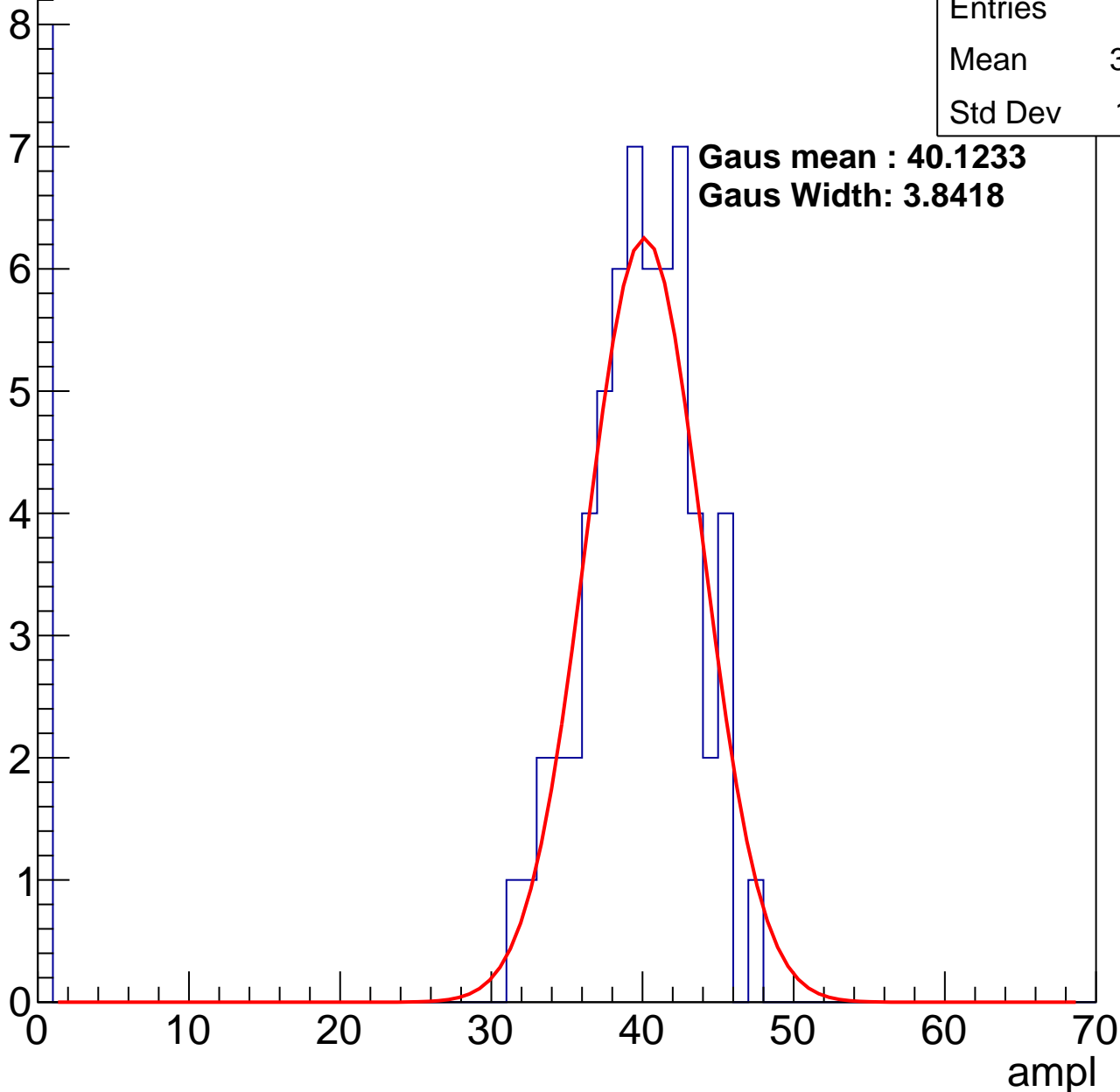
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	34.76
Std Dev	13.11

**Gaus mean : 40.1233**

**Gaus Width: 3.8418**

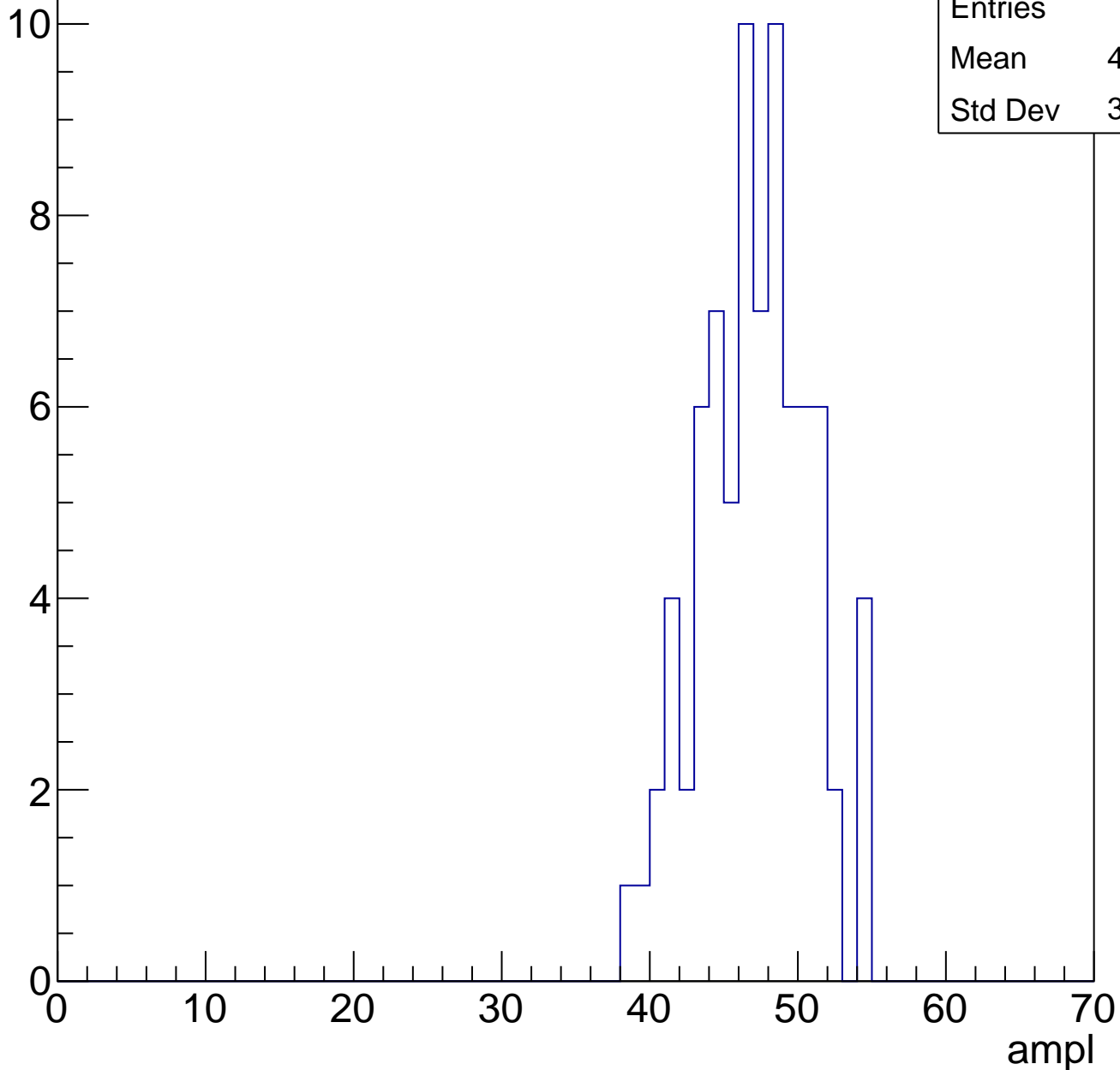


# B1L103S, U3-ch75, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	79
Mean	46.65
Std Dev	3.639

Entry

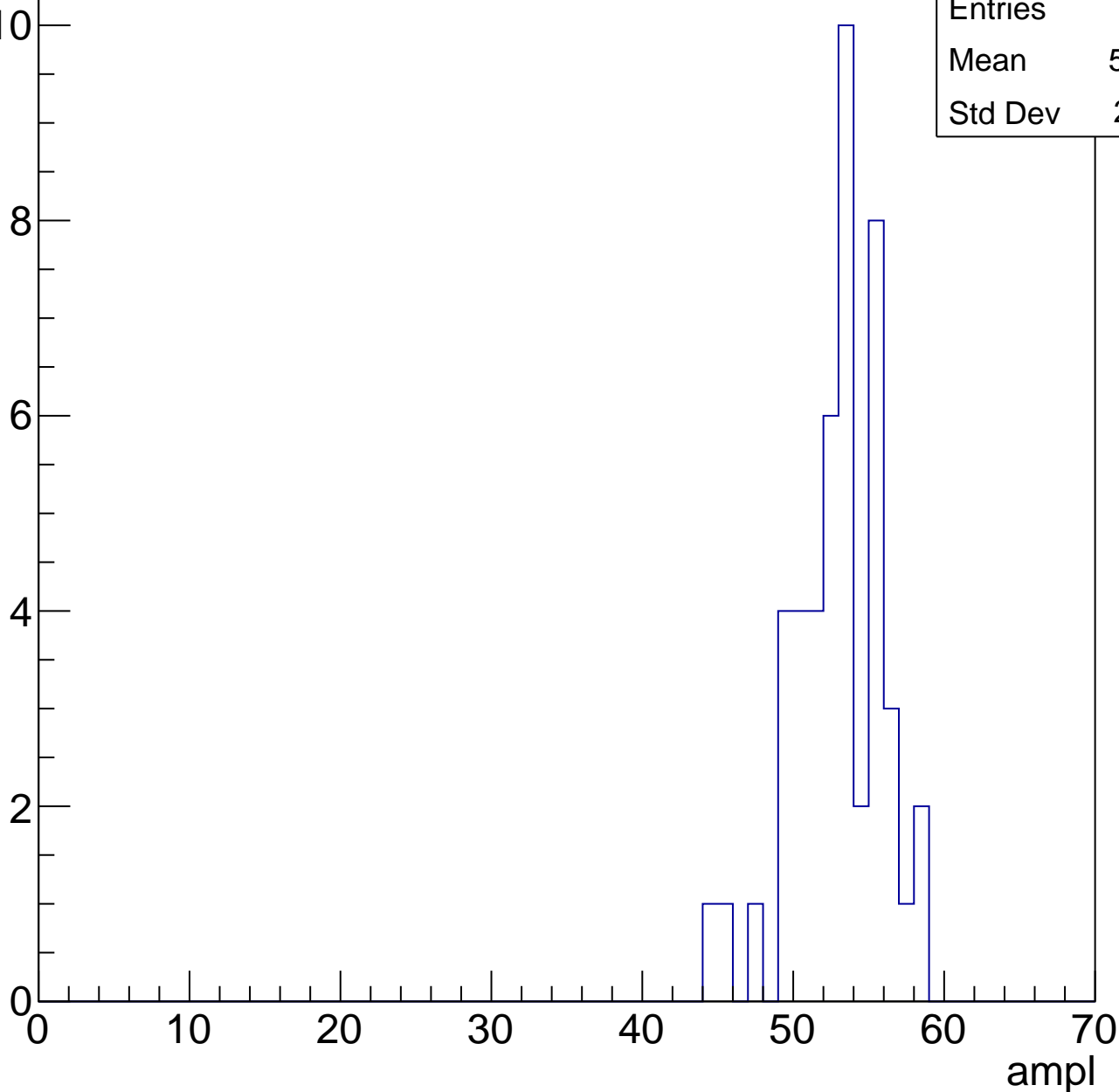


# B1L103S, U3-ch75, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

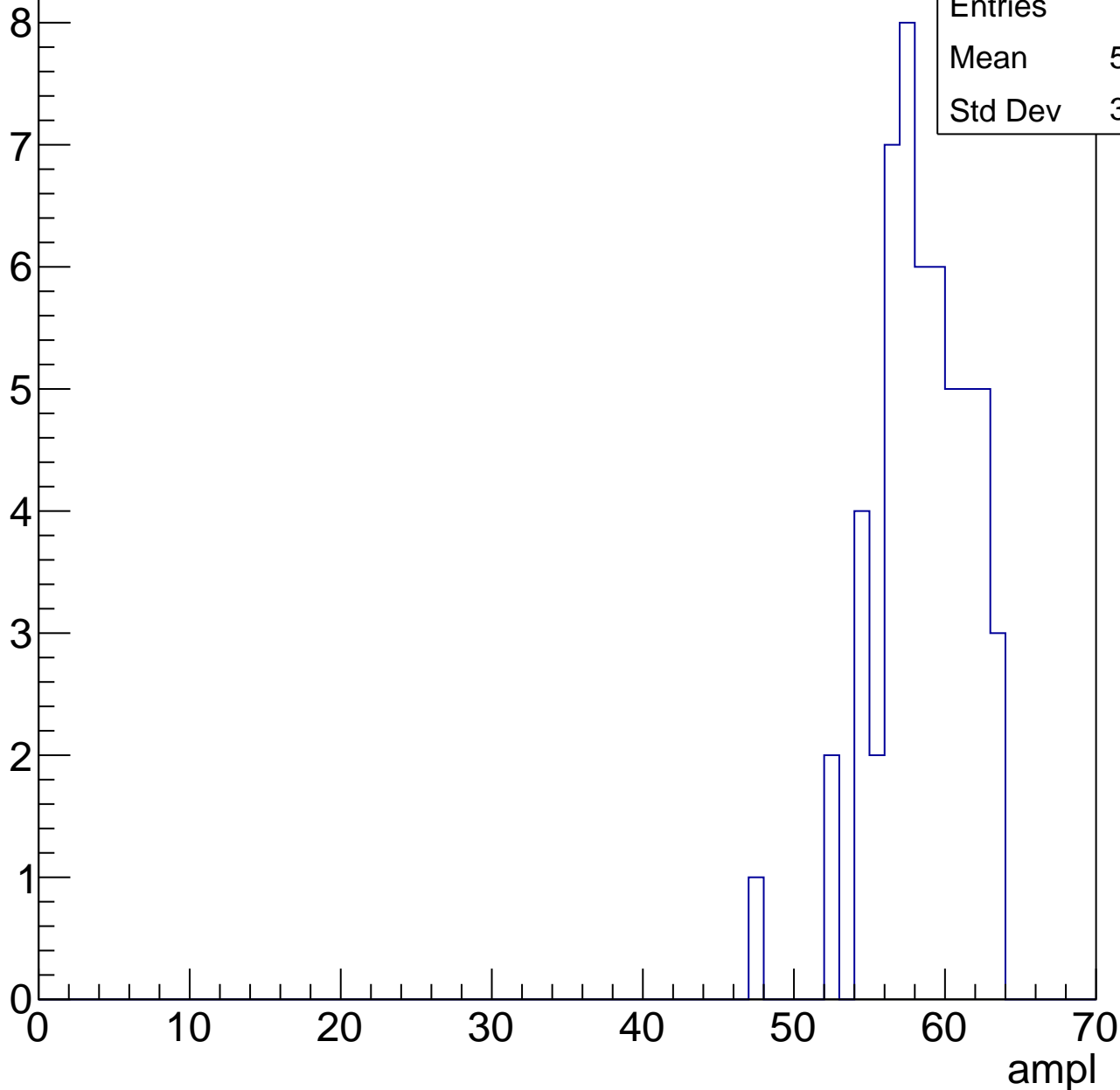
Entries	47
Mean	52.49
Std Dev	2.981



# B1L103S, U3-ch75, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

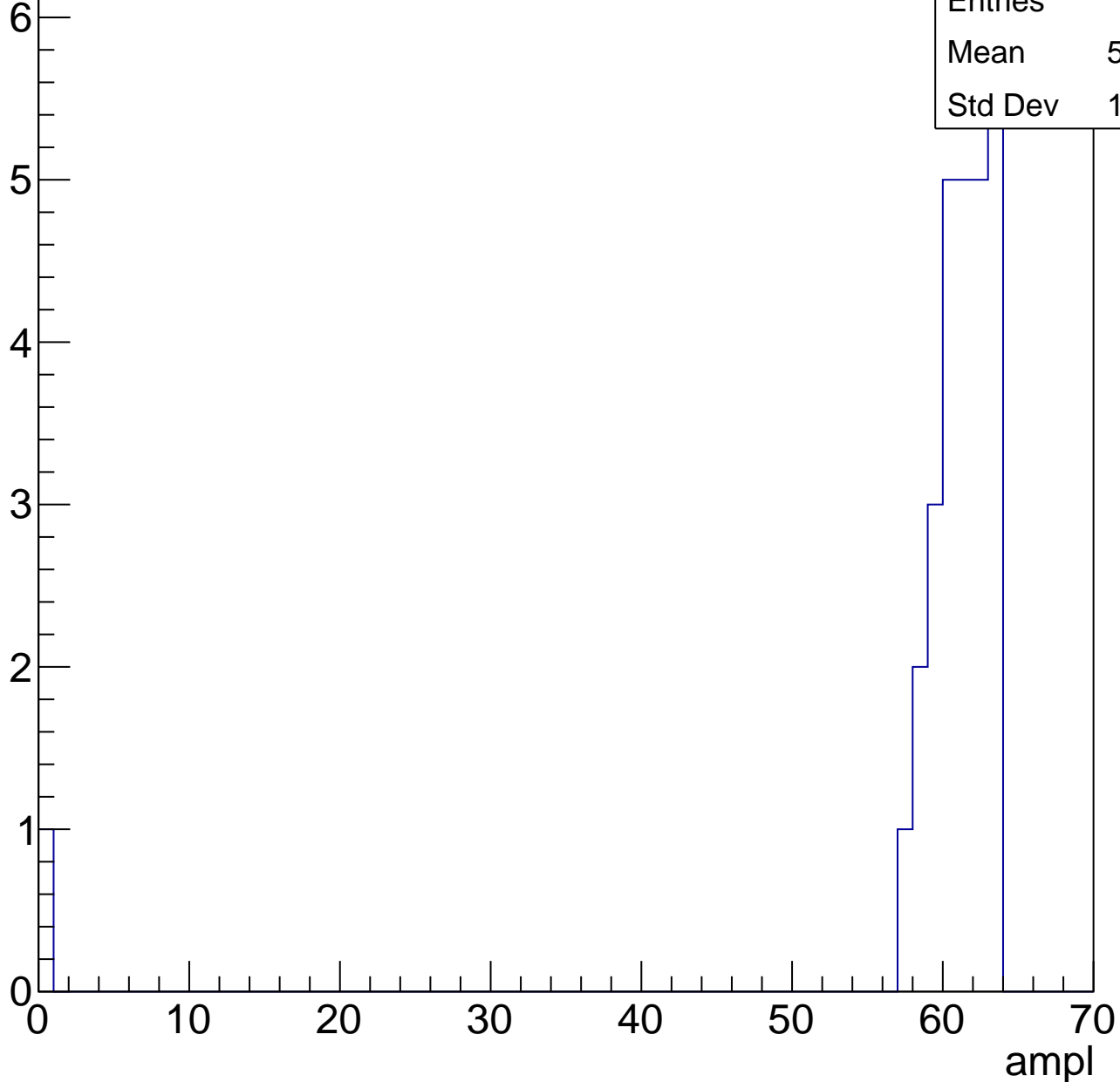


Entries	54
Mean	57.98
Std Dev	3.153

# B1L103S, U3-ch75, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U3-ch75, adc7

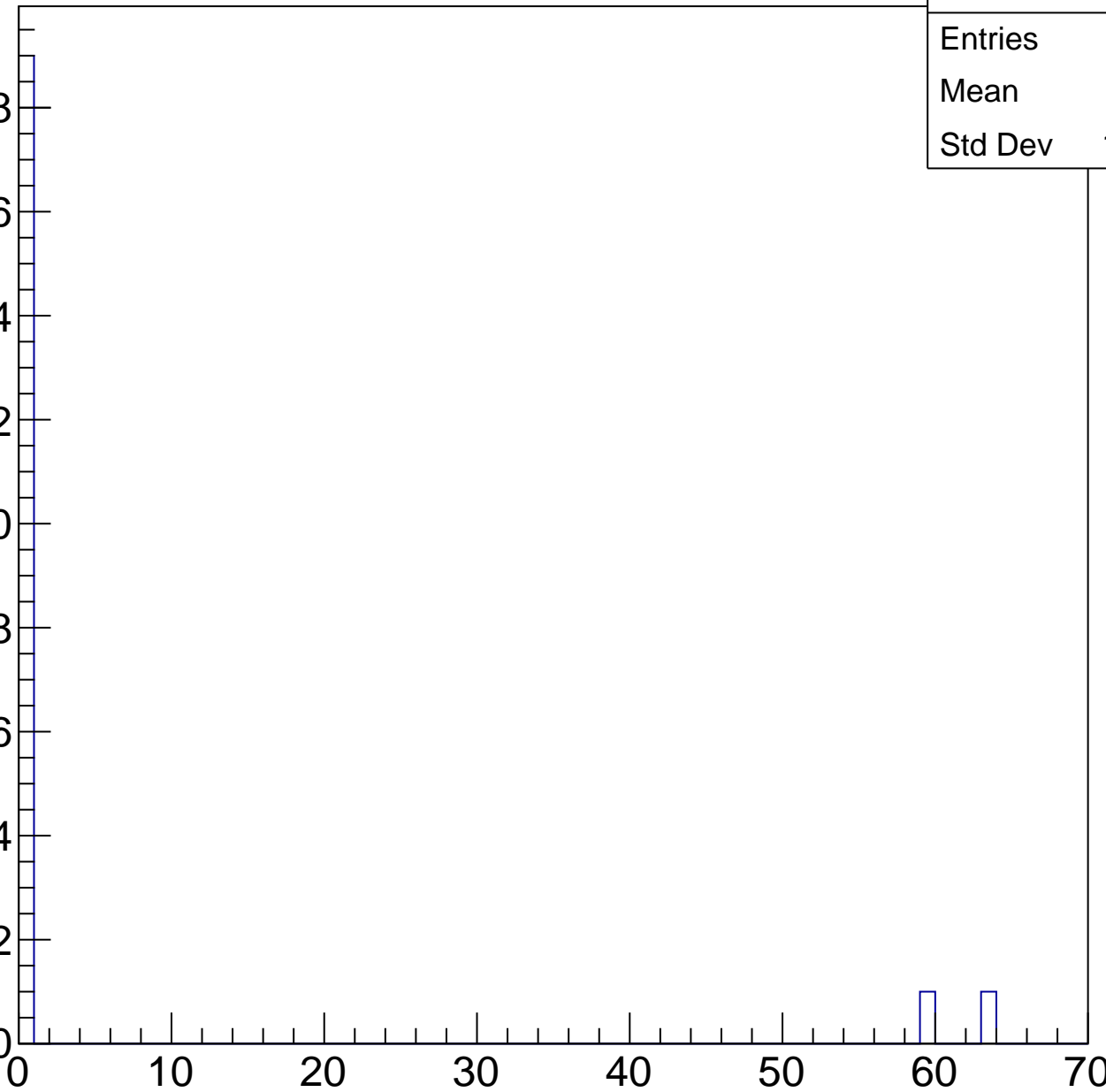
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	21
Mean	5.81
Std Dev	17.92

ampl



# B1L103S, U3-ch76, adc0

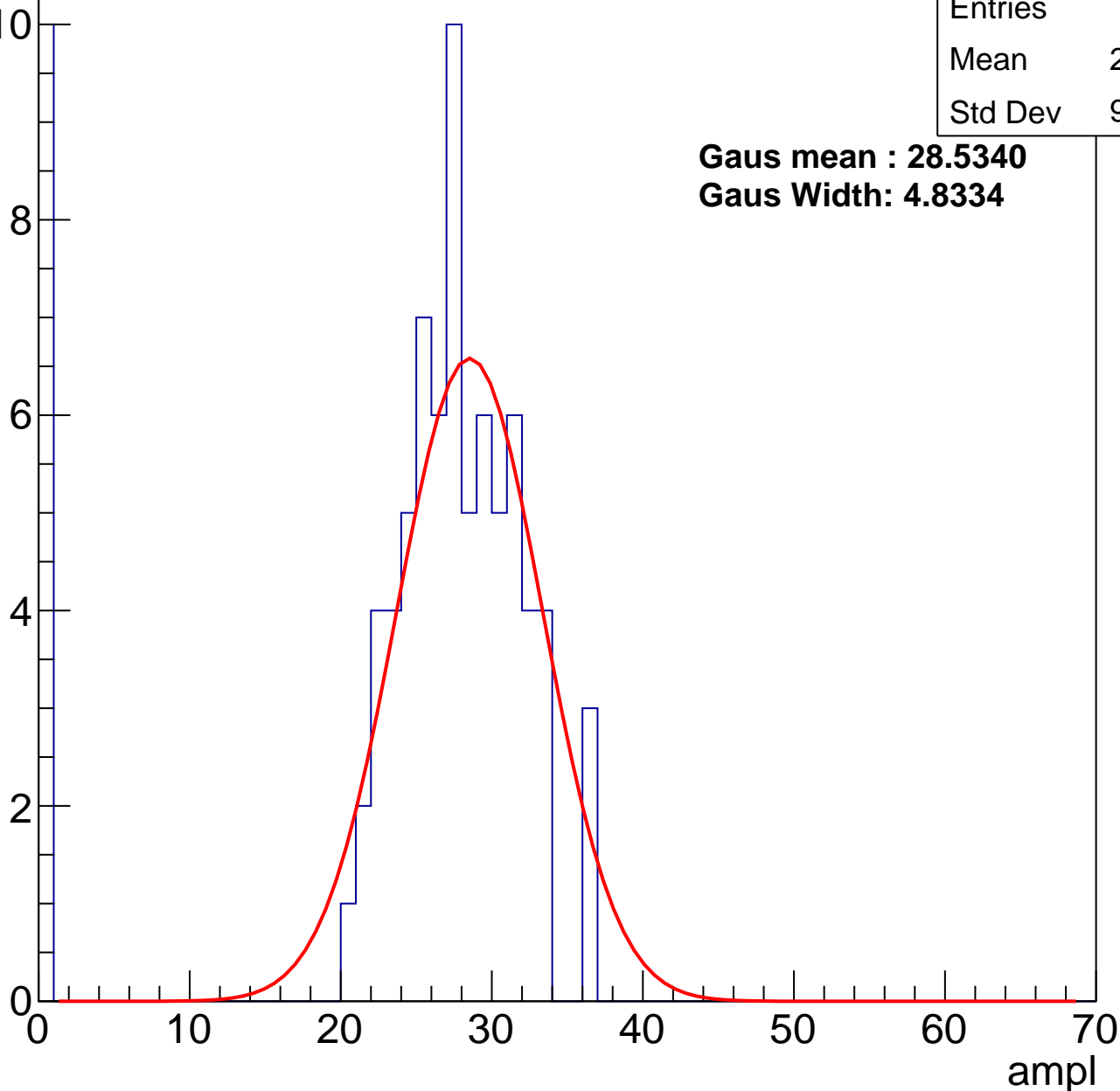
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	82
Mean	24.16
Std Dev	9.658

**Gaus mean : 28.5340**

**Gaus Width: 4.8334**



# B1L103S, U3-ch76, adc1

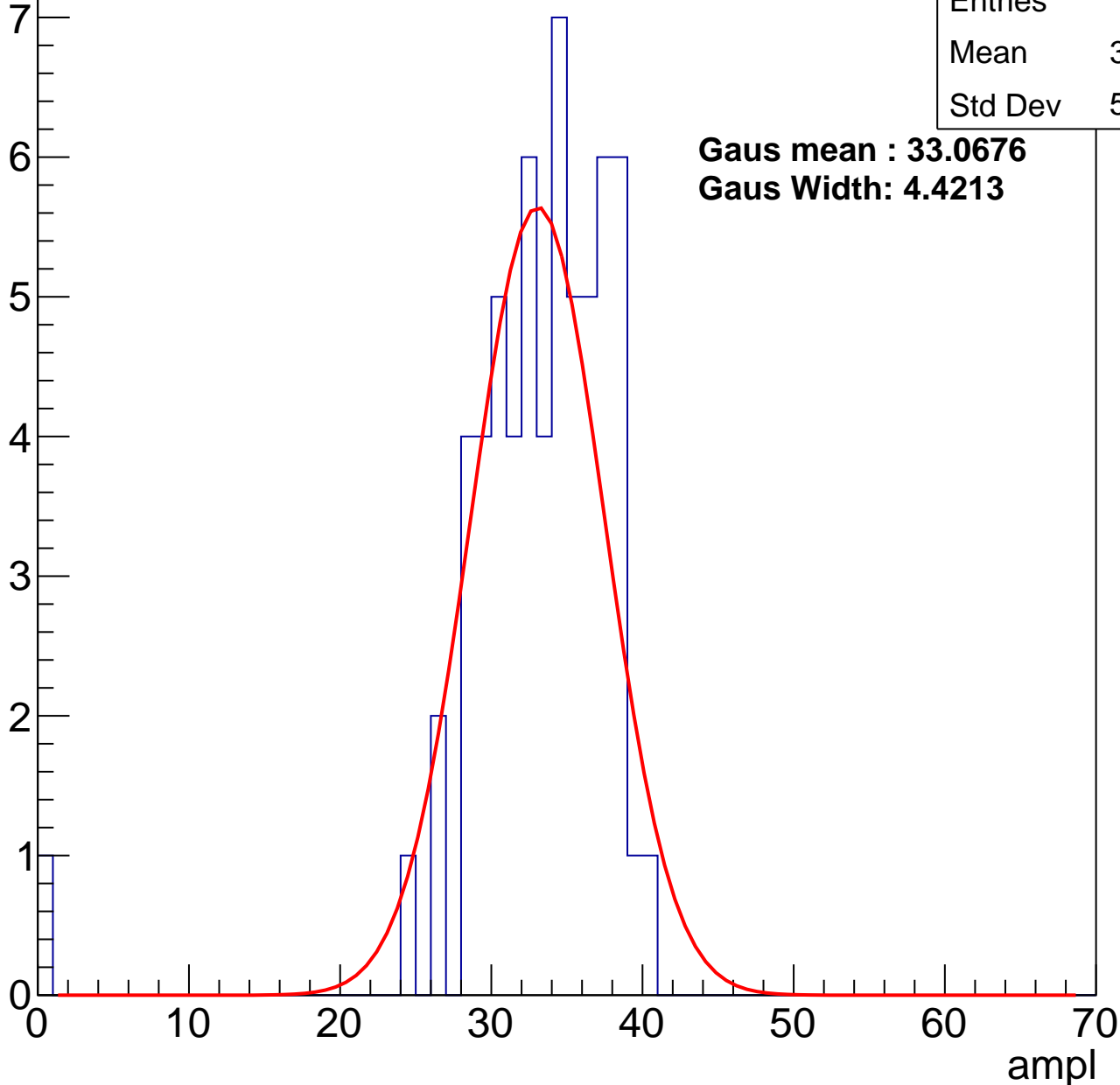
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	32.65
Std Dev	5.527

**Gaus mean : 33.0676**

**Gaus Width: 4.4213**



# B1L103S, U3-ch76, adc2

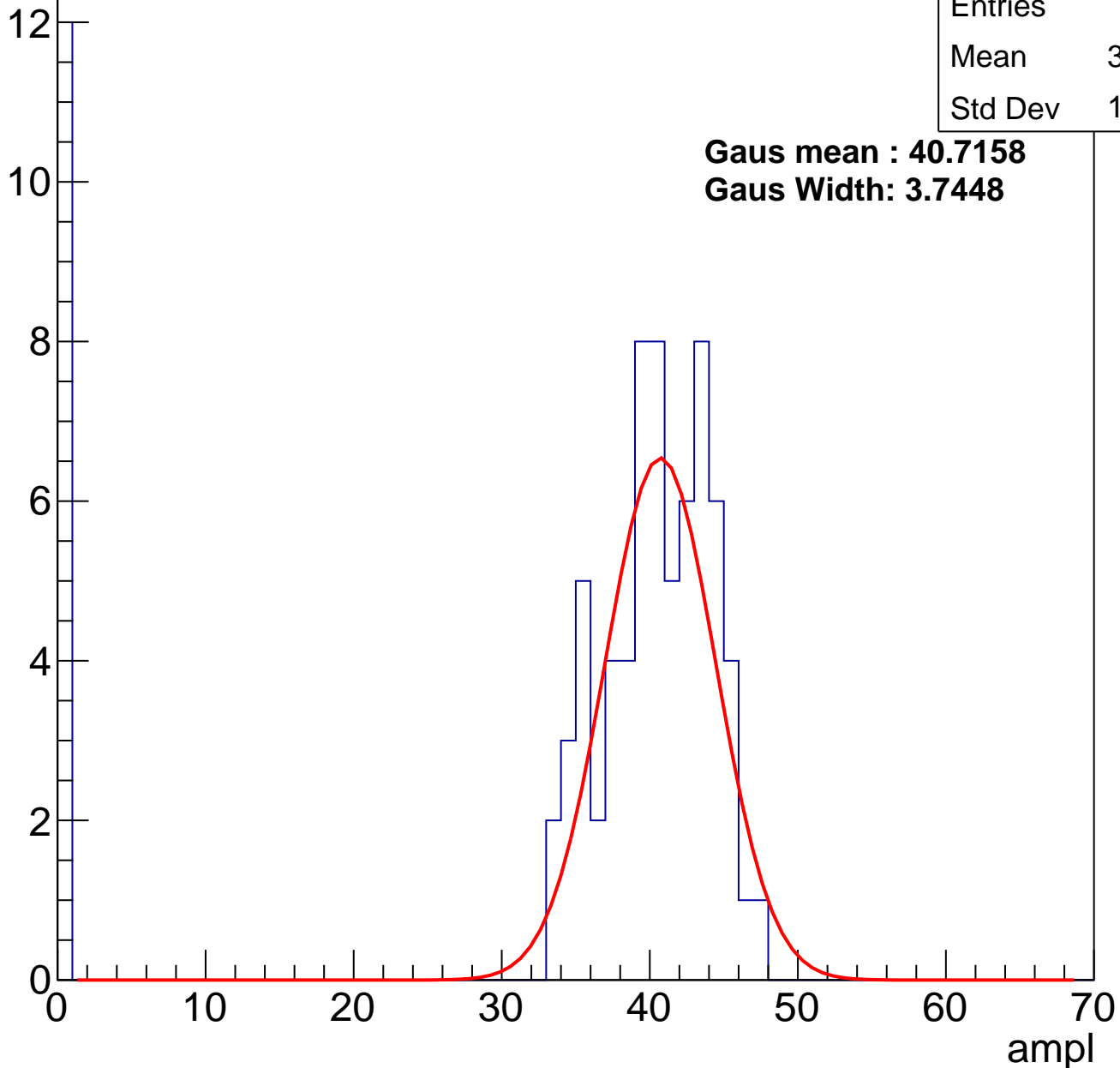
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	79
Mean	33.99
Std Dev	14.73

**Gaus mean : 40.7158**

**Gaus Width: 3.7448**

Entry

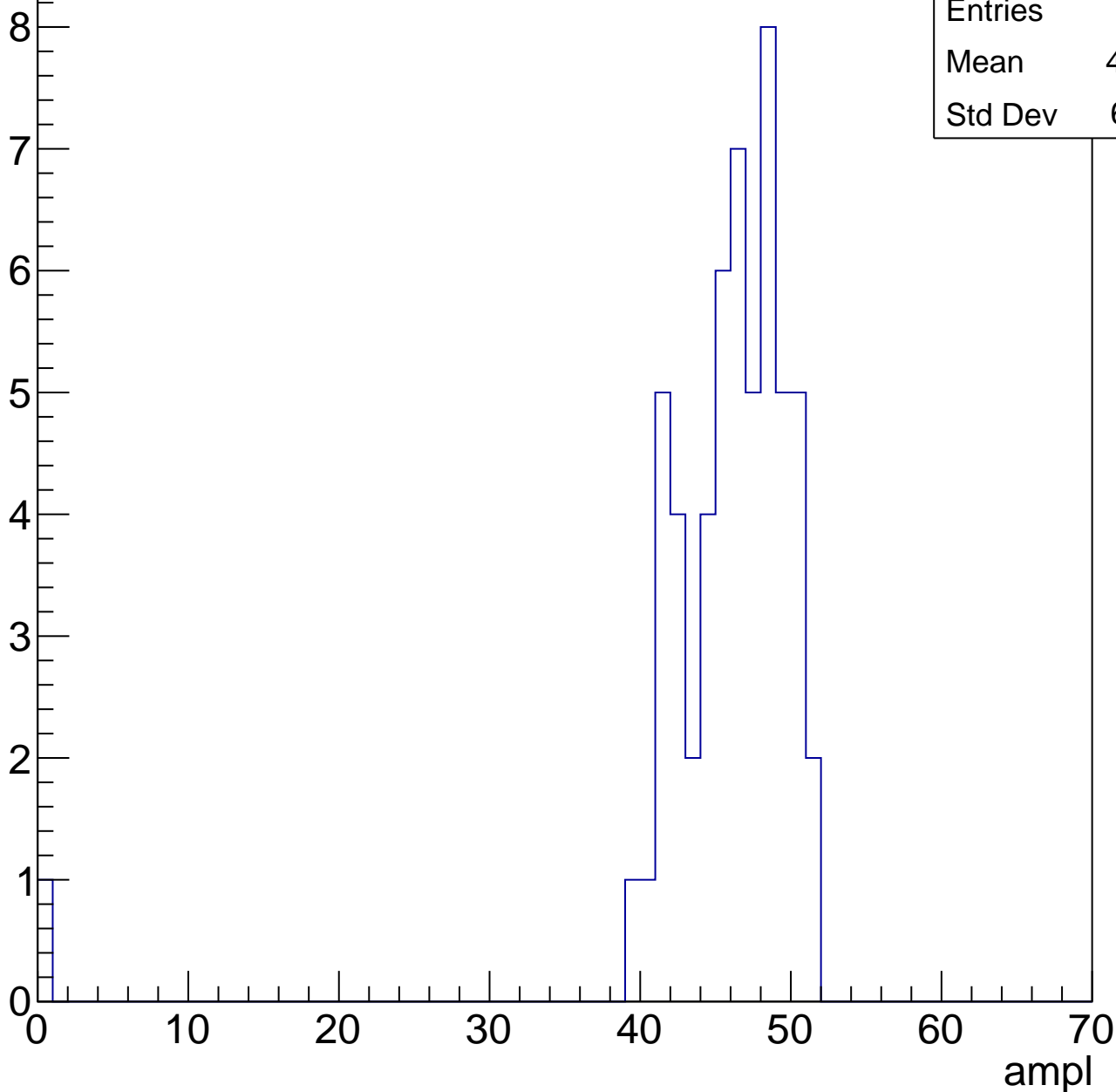


# B1L103S, U3-ch76, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	56
Mean	45.04
Std Dev	6.801

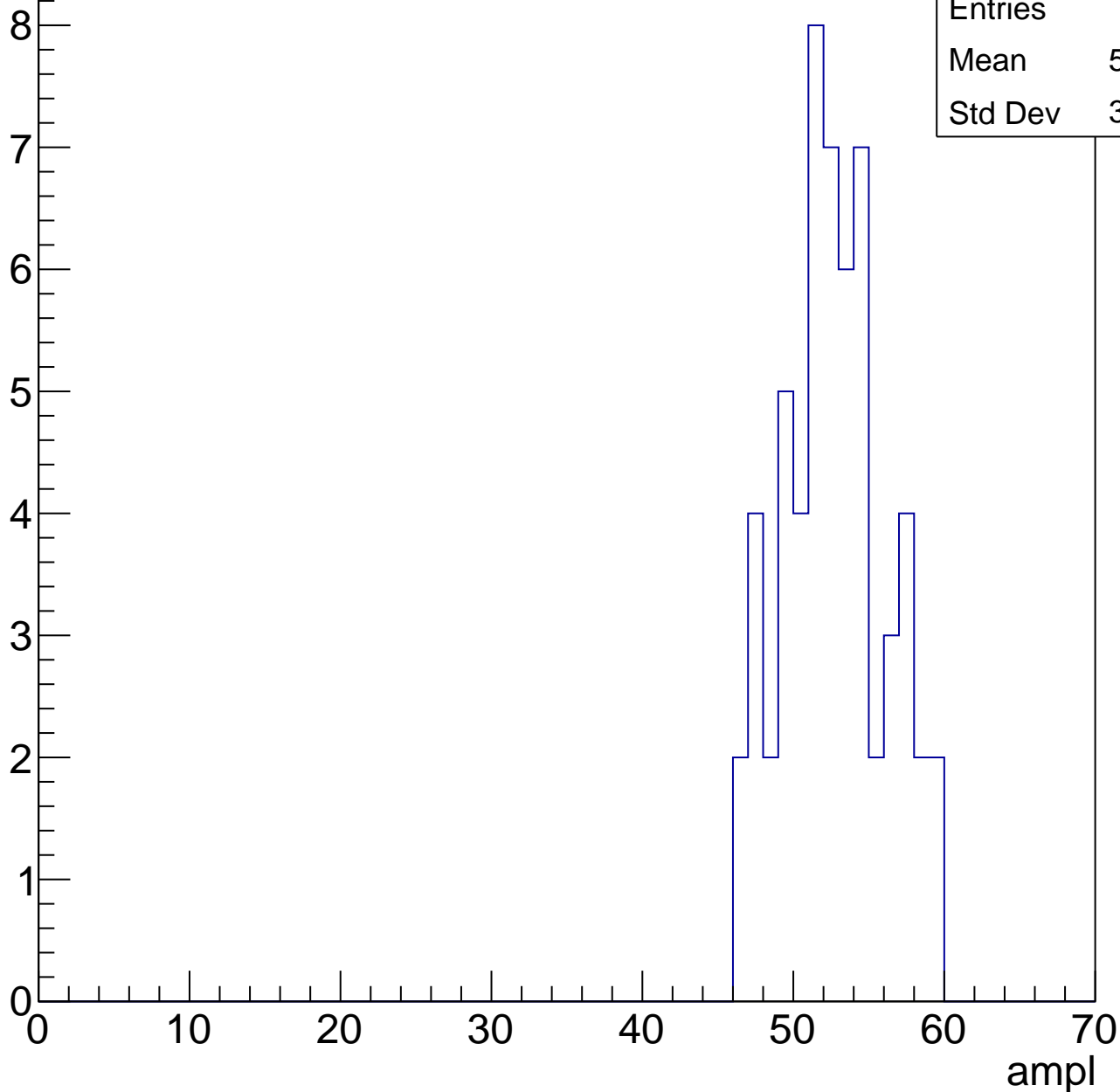


# B1L103S, U3-ch76, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	52.22
Std Dev	3.322

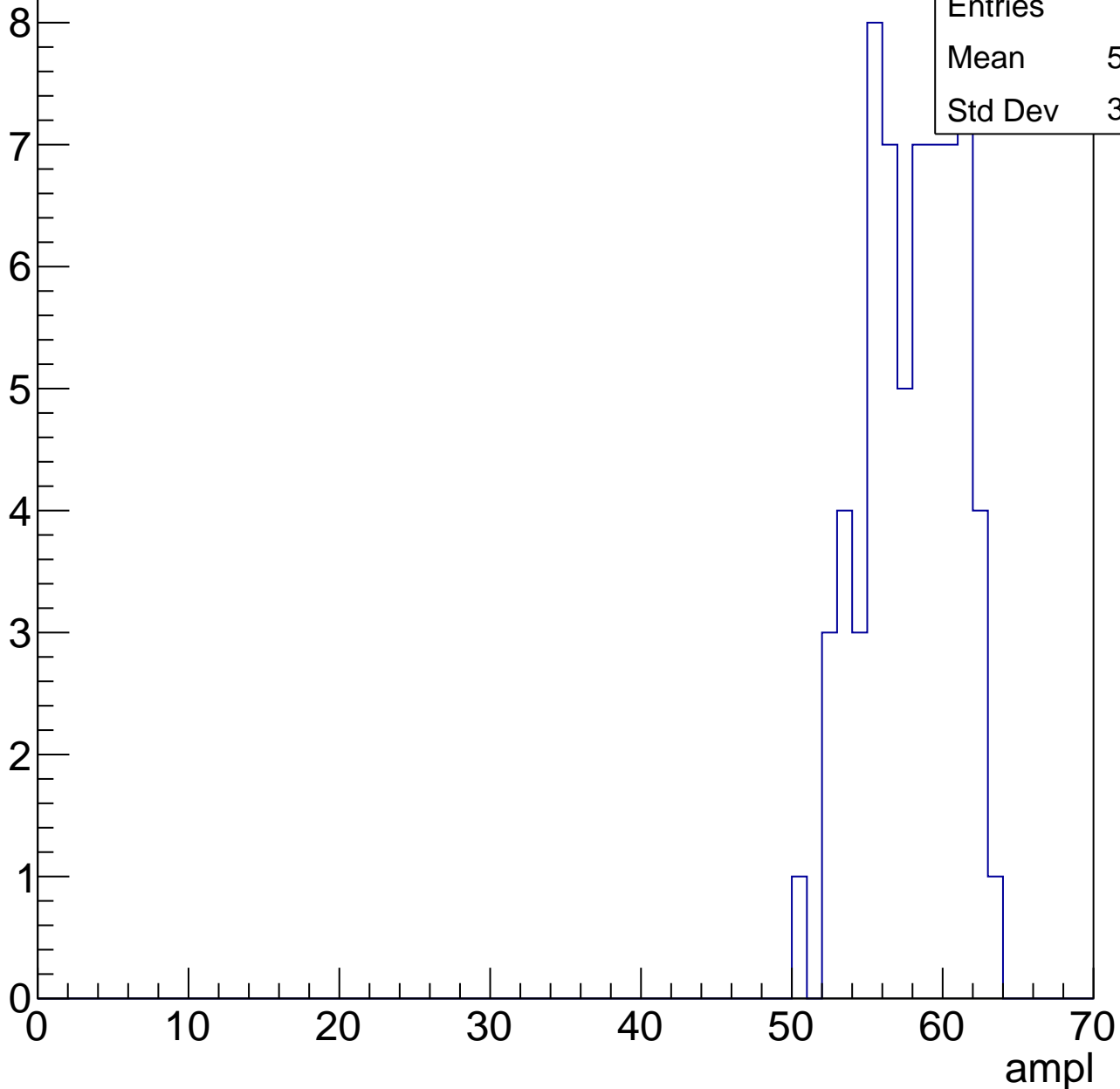


# B1L103S, U3-ch76, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	65
Mean	57.46
Std Dev	3.044

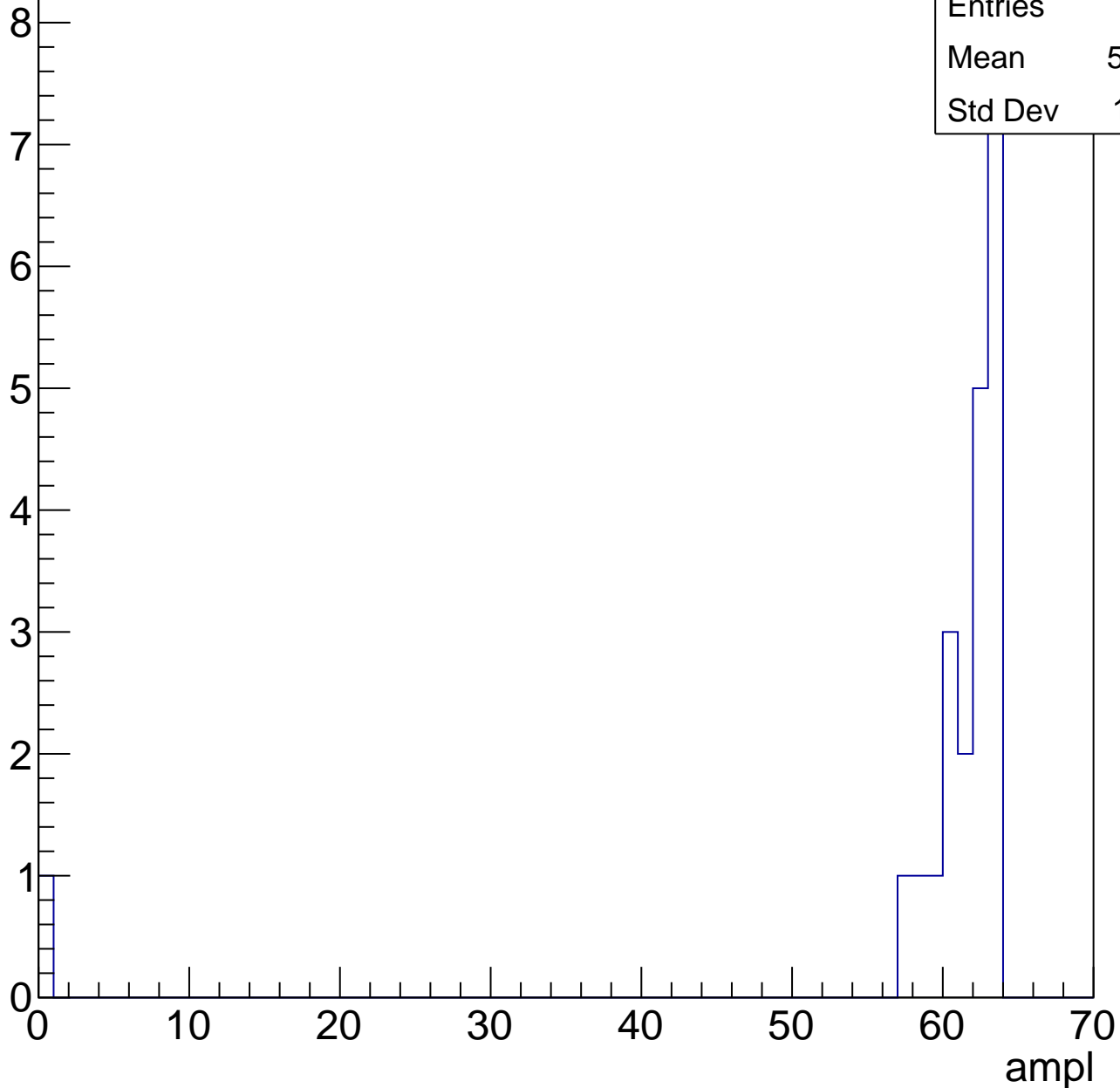


# B1L103S, U3-ch76, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	22
Mean	58.64
Std Dev	12.91





# B1L103S, U3-ch76, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	5.952
Std Dev	18.35

Entry



# B1L103S, U3-ch77, adc0

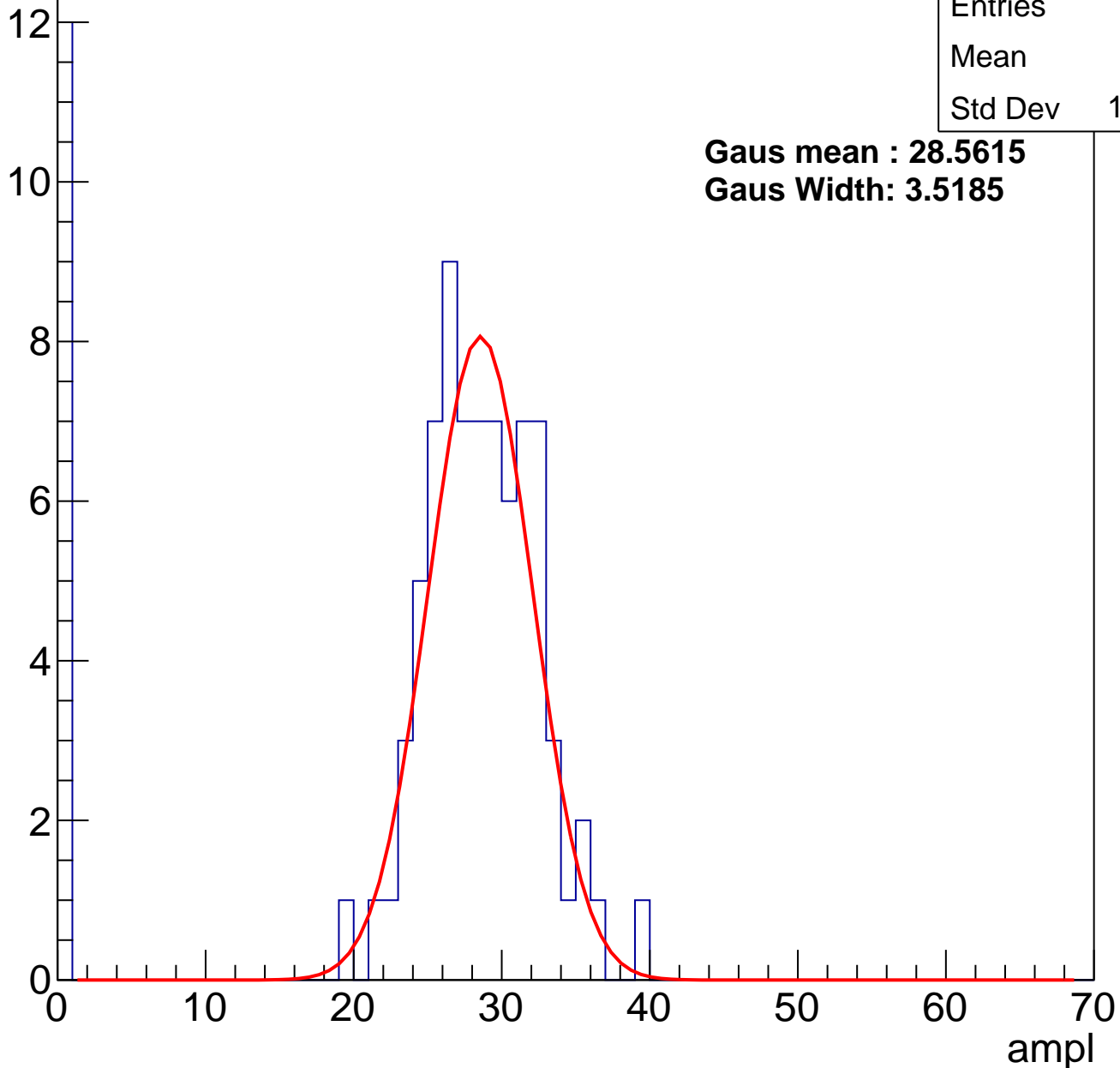
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	88
Mean	24.4
Std Dev	10.28

**Gaus mean : 28.5615**

**Gaus Width: 3.5185**

Entry



# B1L103S, U3-ch77, adc1

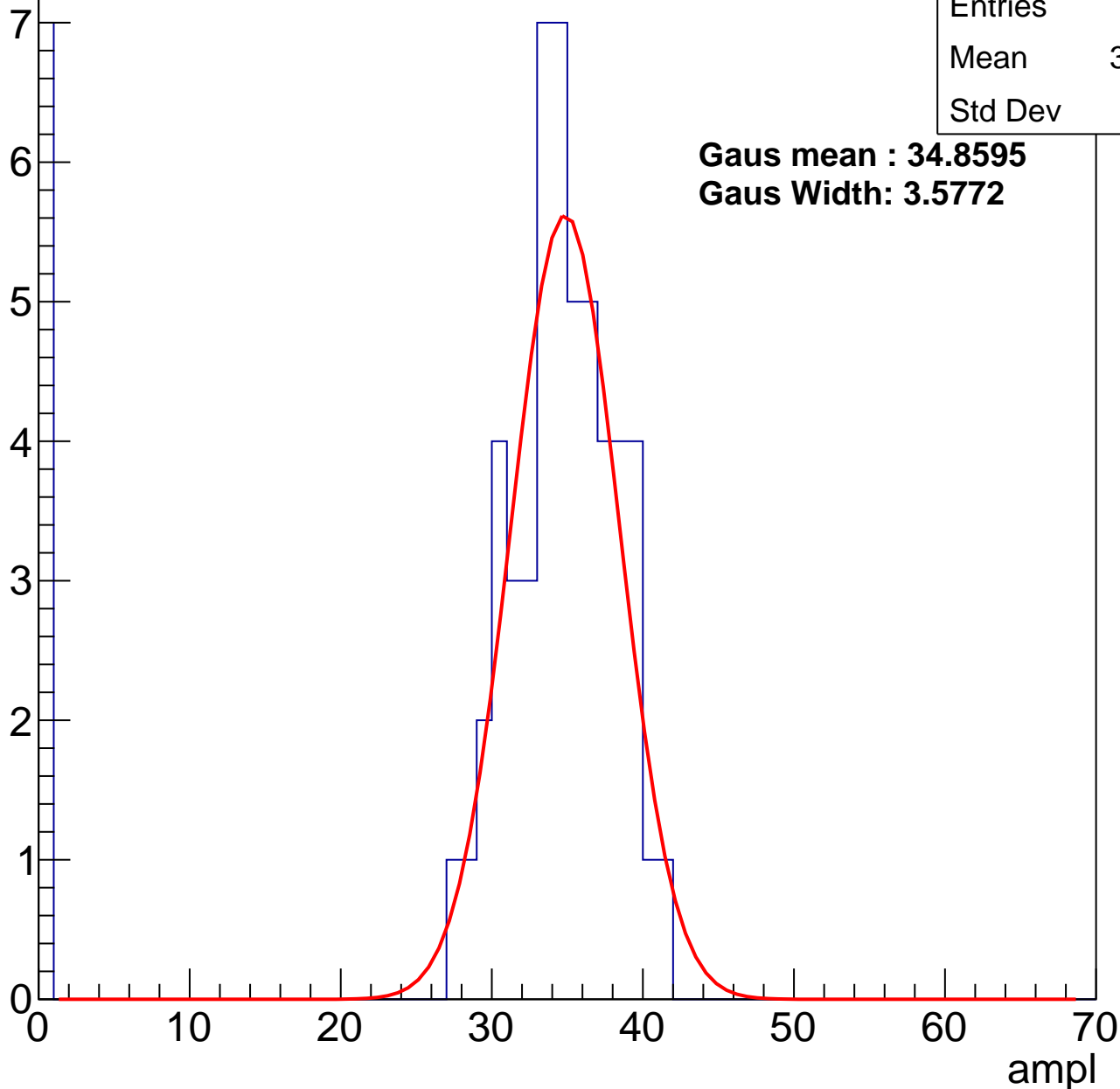
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	30.22
Std Dev	11.5

**Gaus mean : 34.8595**

**Gaus Width: 3.5772**



# B1L103S, U3-ch77, adc2

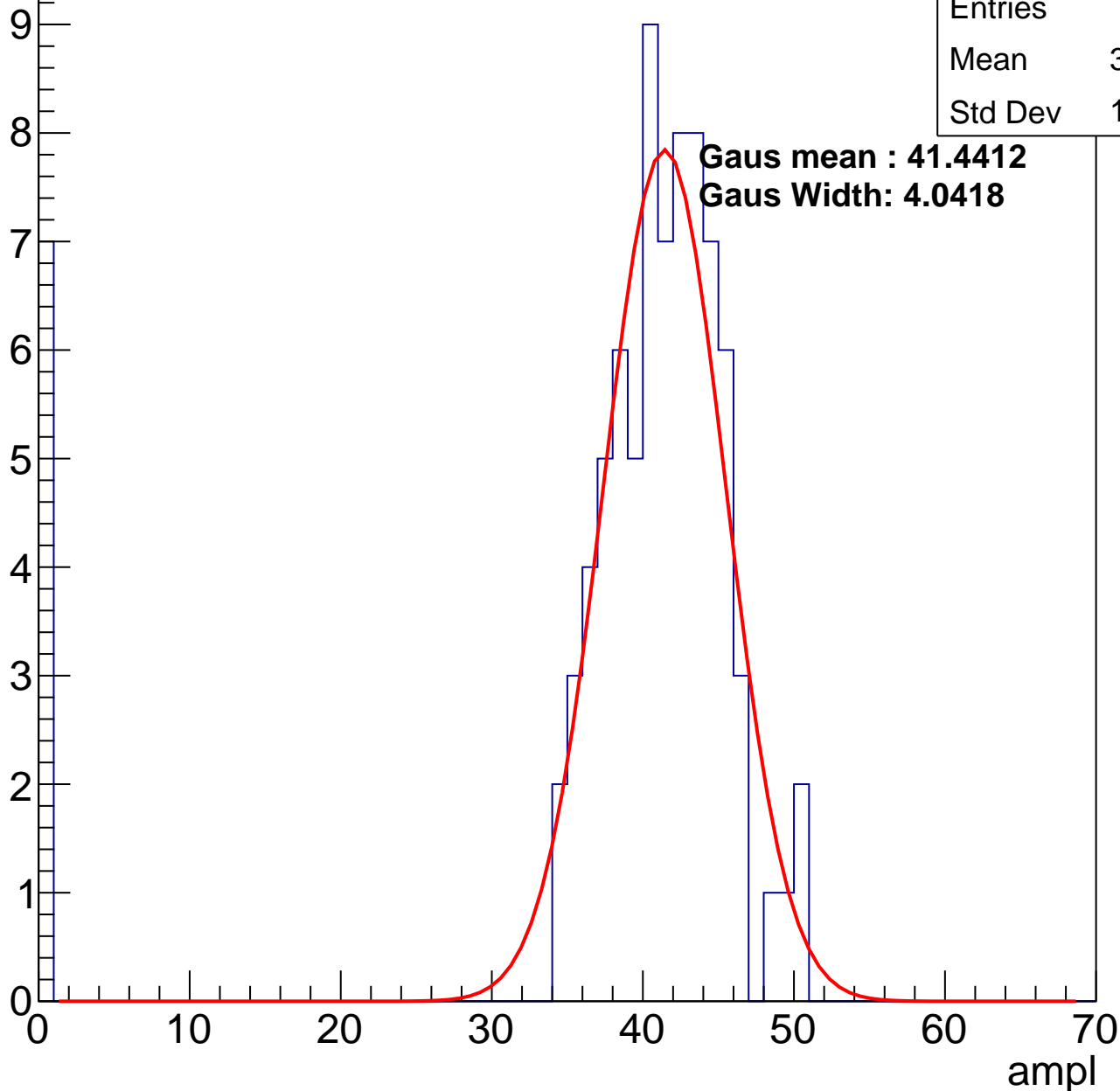
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	84
Mean	37.68
Std Dev	11.88

**Gaus mean : 41.4412**

**Gaus Width: 4.0418**

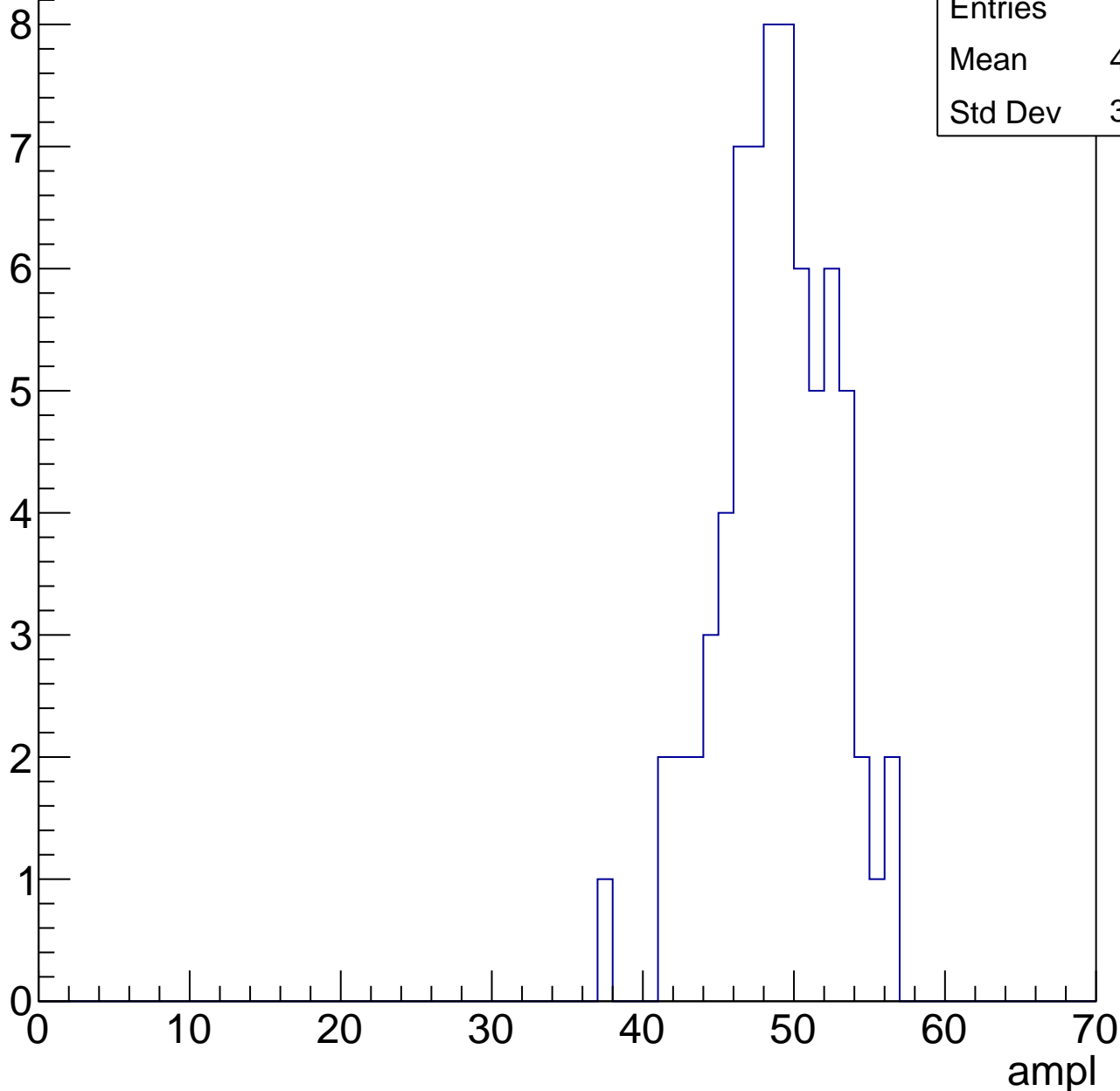


# B1L103S, U3-ch77, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	71
Mean	48.38
Std Dev	3.747

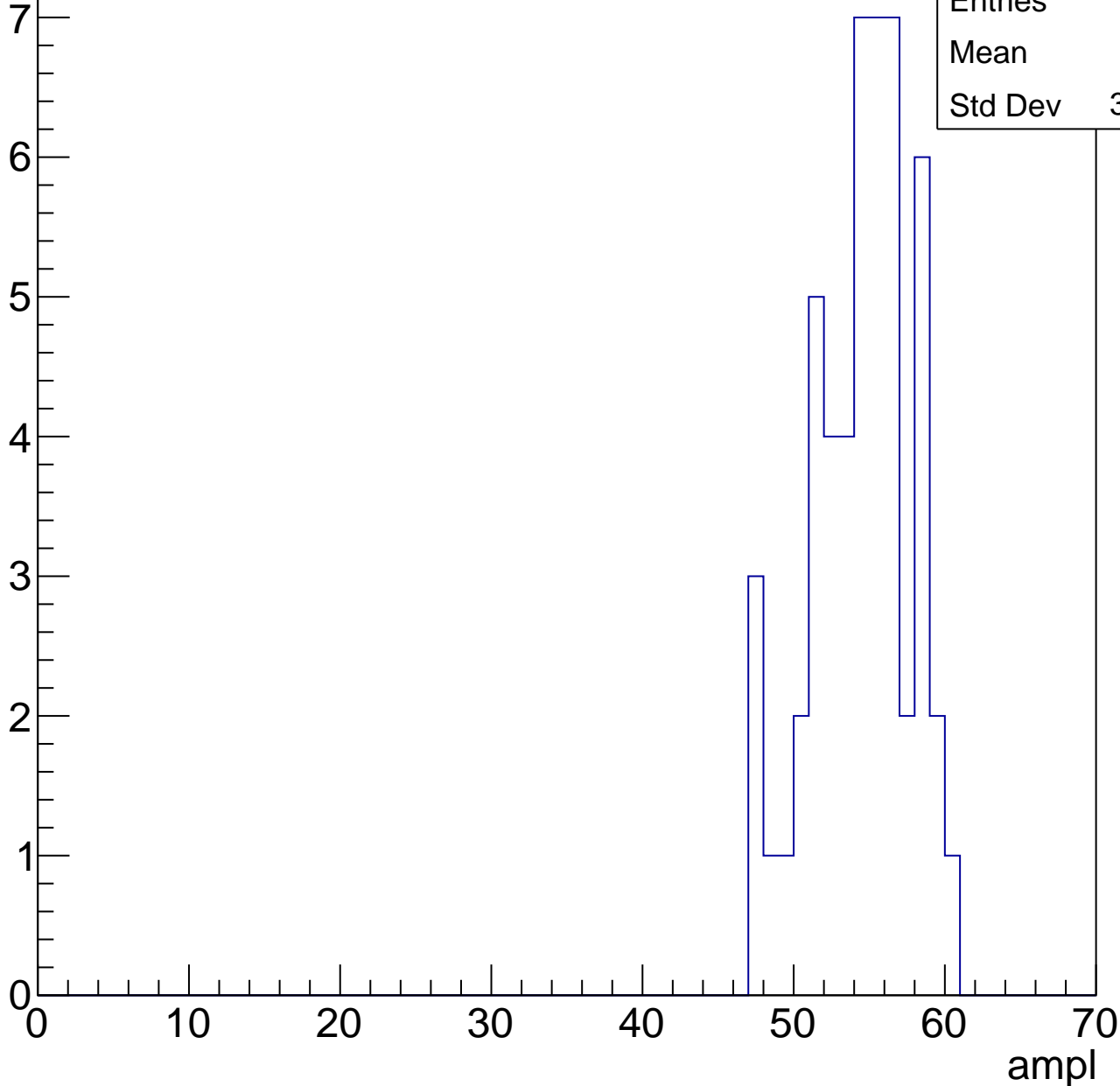


# B1L103S, U3-ch77, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	52
Mean	54
Std Dev	3.223



# B1L103S, U3-ch77, adc5

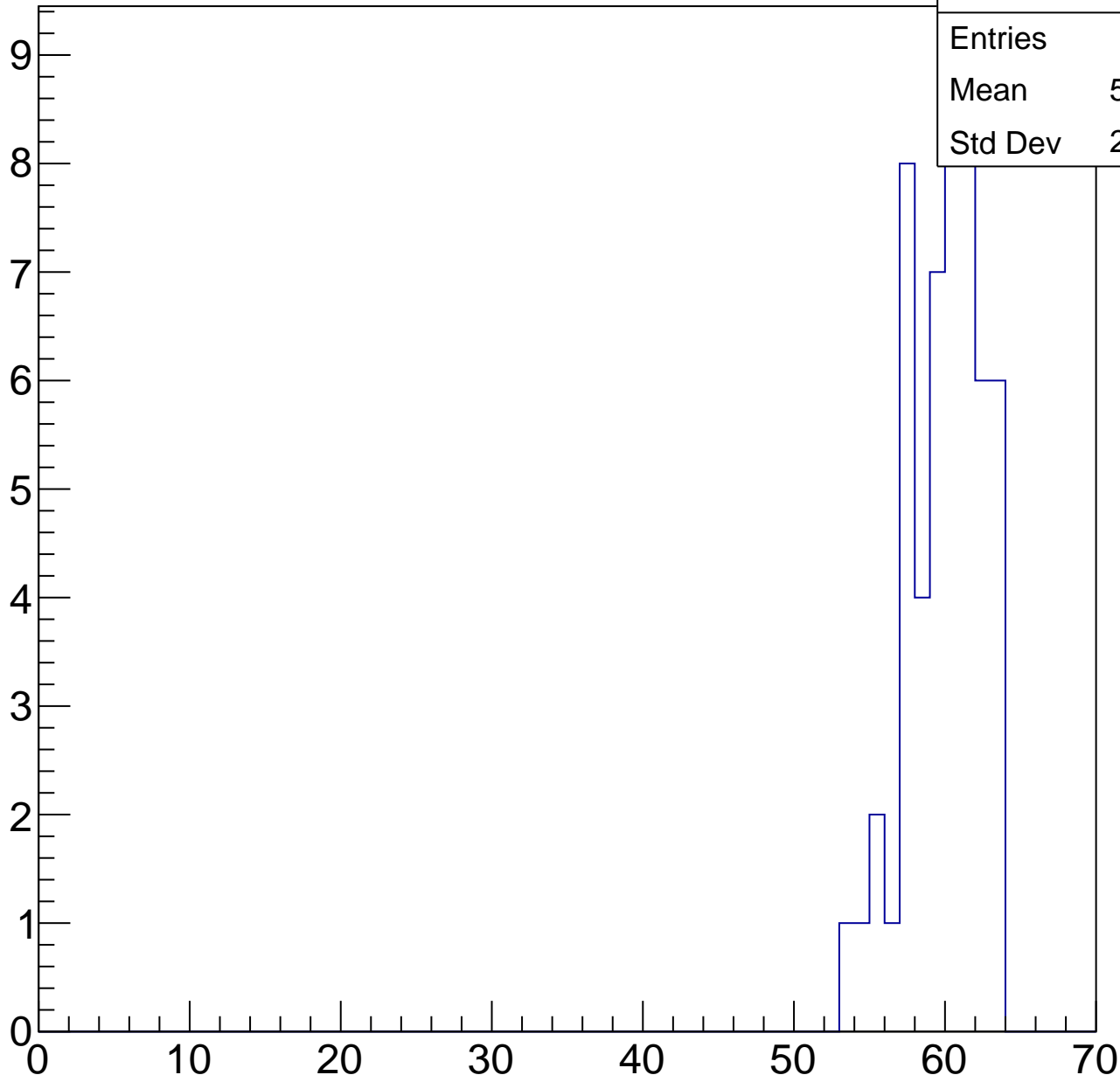
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	53
Mean	59.49
Std Dev	2.454

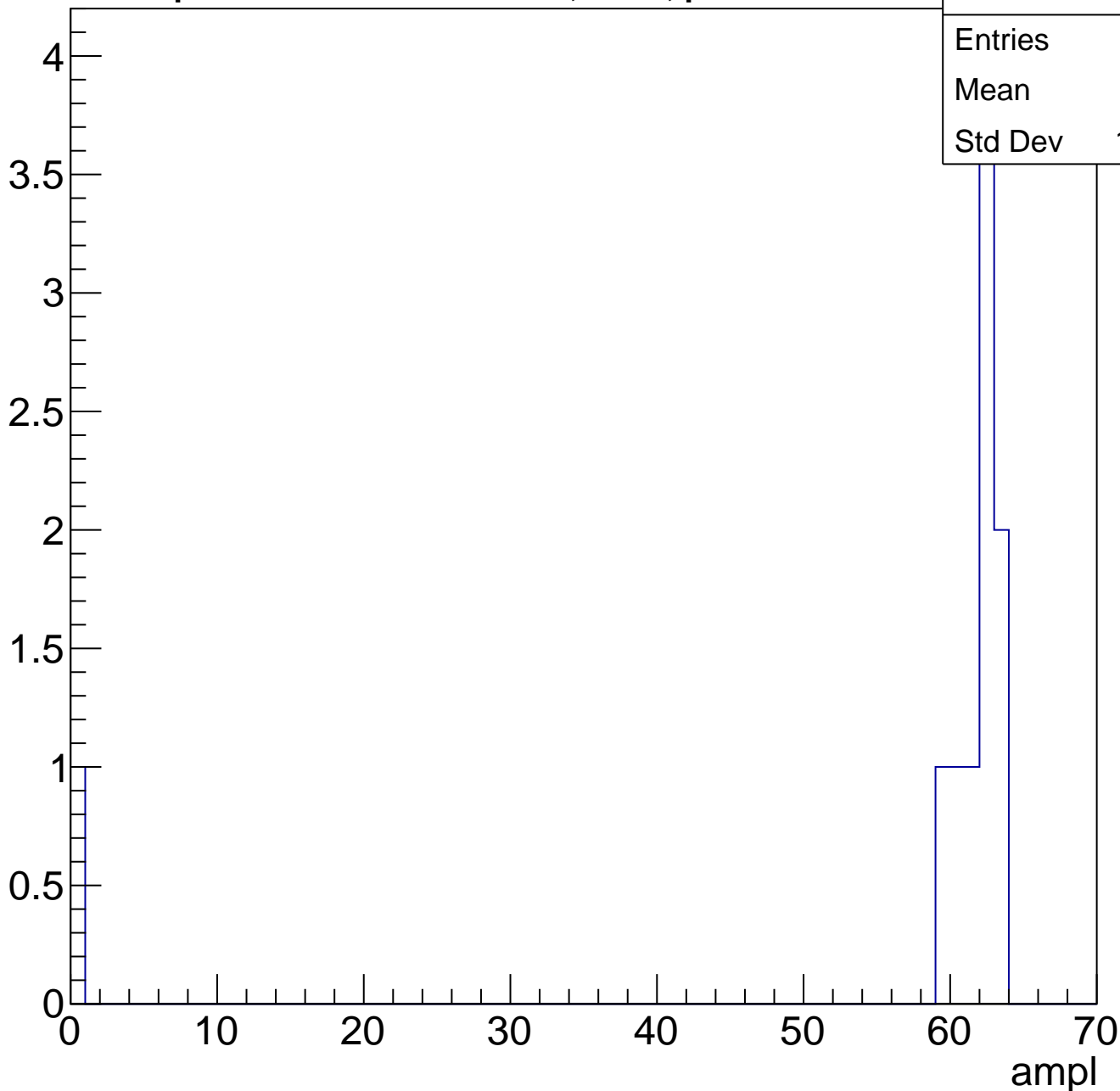
ampl



# B1L103S, U3-ch77, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U3-ch77, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U3-ch78, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	79
Mean	23.27
Std Dev	10.97

**Gaus mean : 28.8392**

**Gaus Width: 4.2623**

Entry

12

10

8

6

4

2

0

0

10

20

30

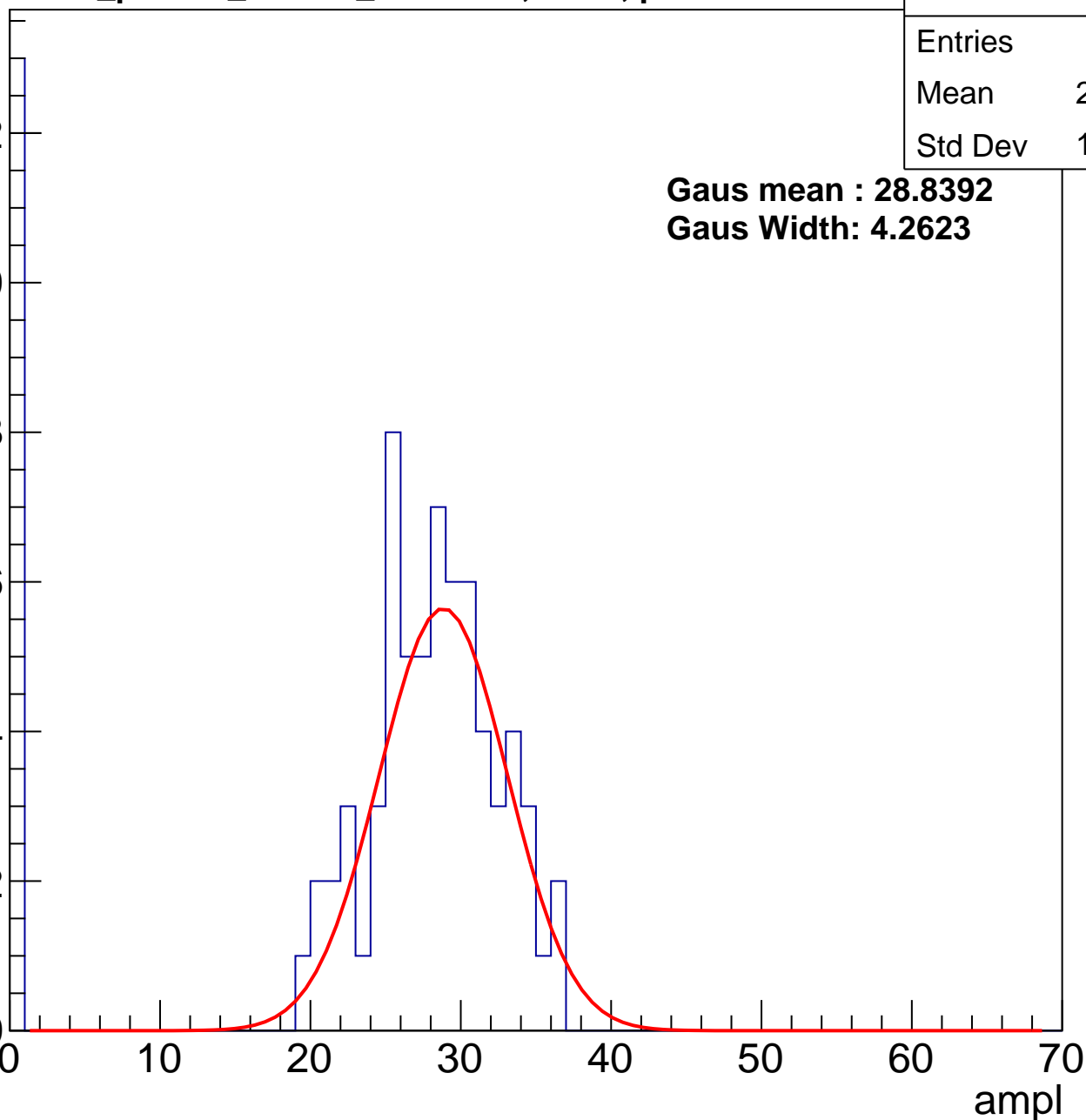
40

50

60

70

ampl



# B1L103S, U3-ch78, adc1

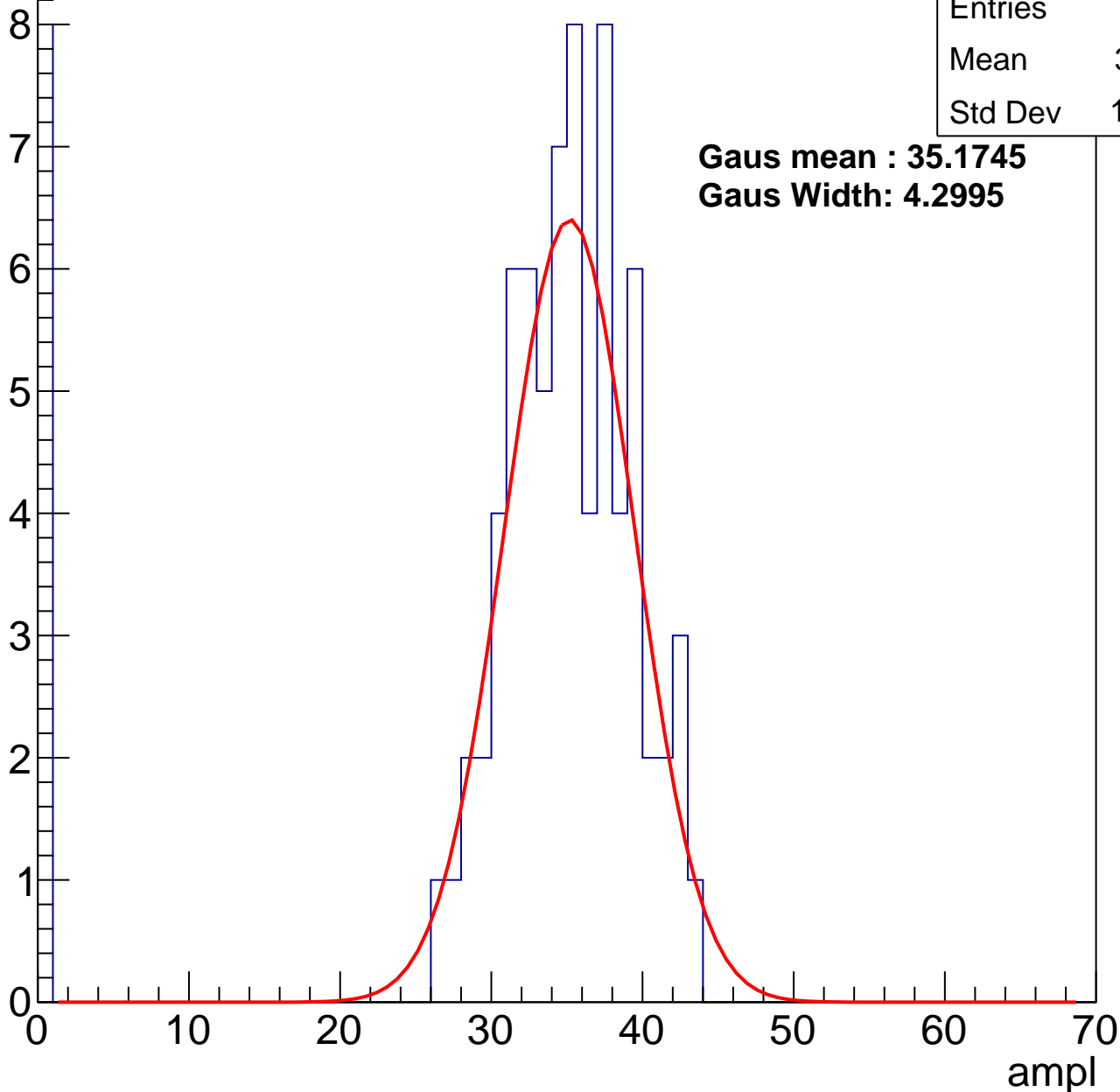
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	80
Mean	31.31
Std Dev	11.07

**Gaus mean : 35.1745**

**Gaus Width: 4.2995**



# B1L103S, U3-ch78, adc2

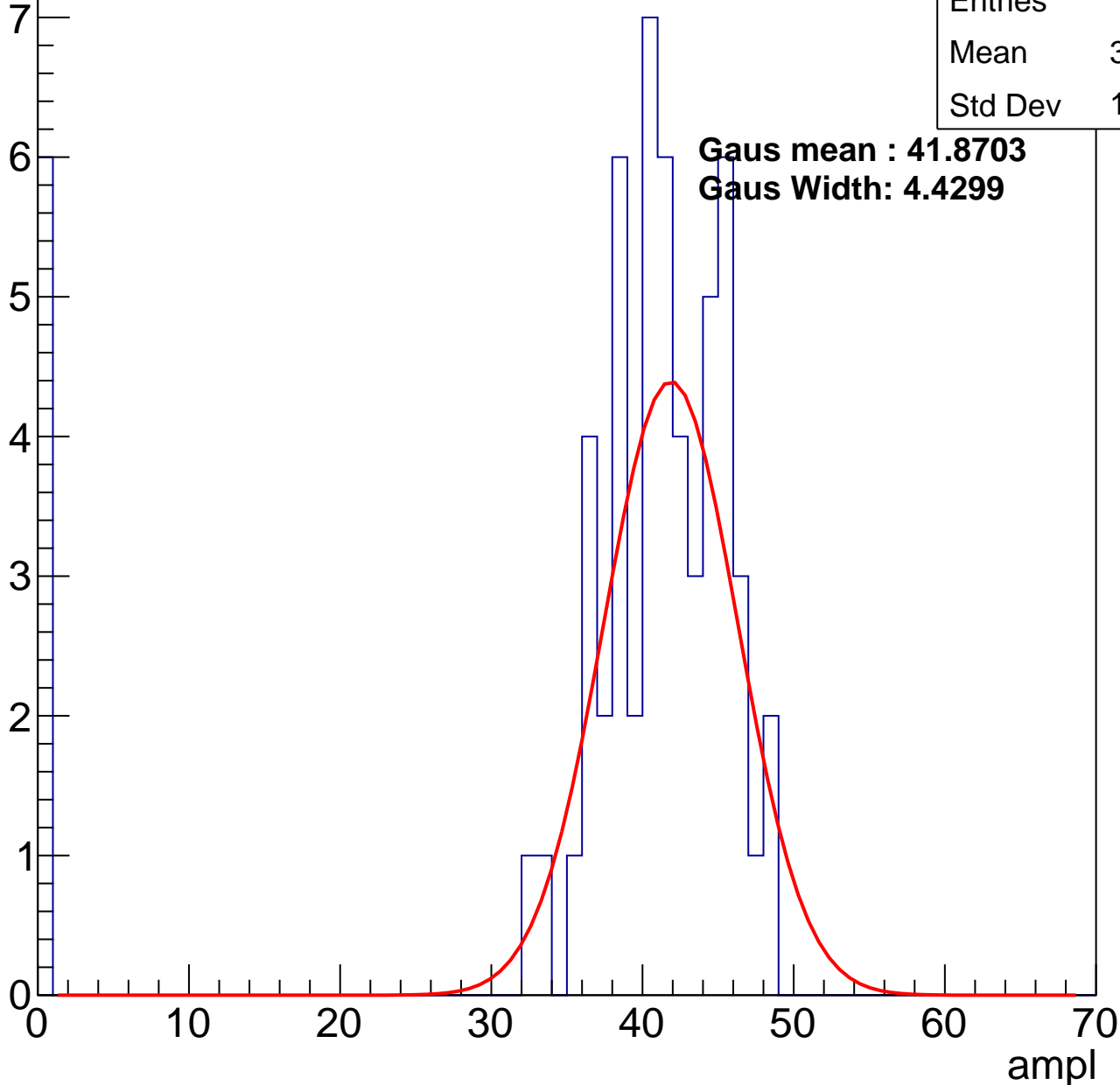
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	60
Mean	36.97
Std Dev	12.82

**Gaus mean : 41.8703**

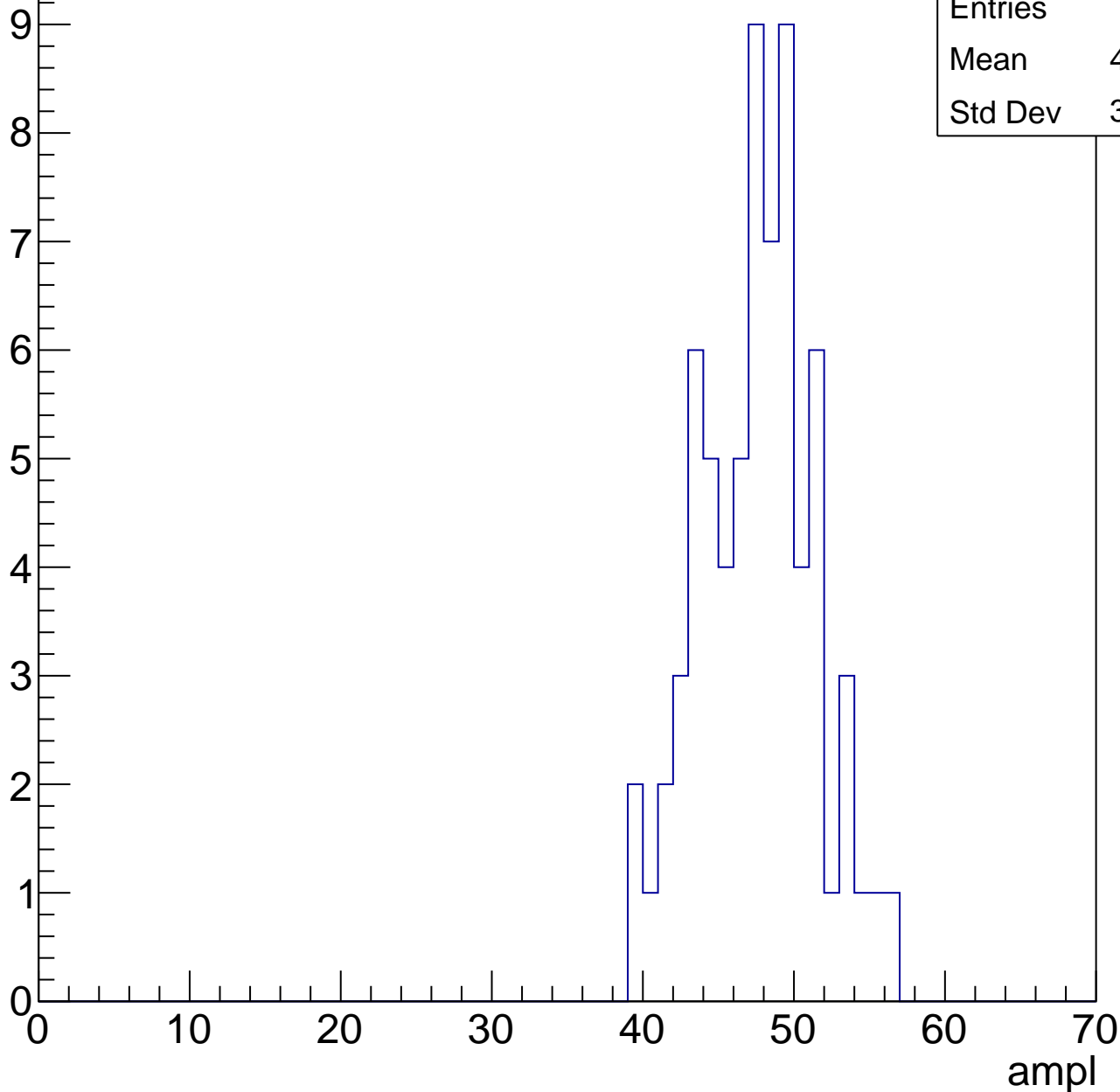
**Gaus Width: 4.4299**



# B1L103S, U3-ch78, adc3

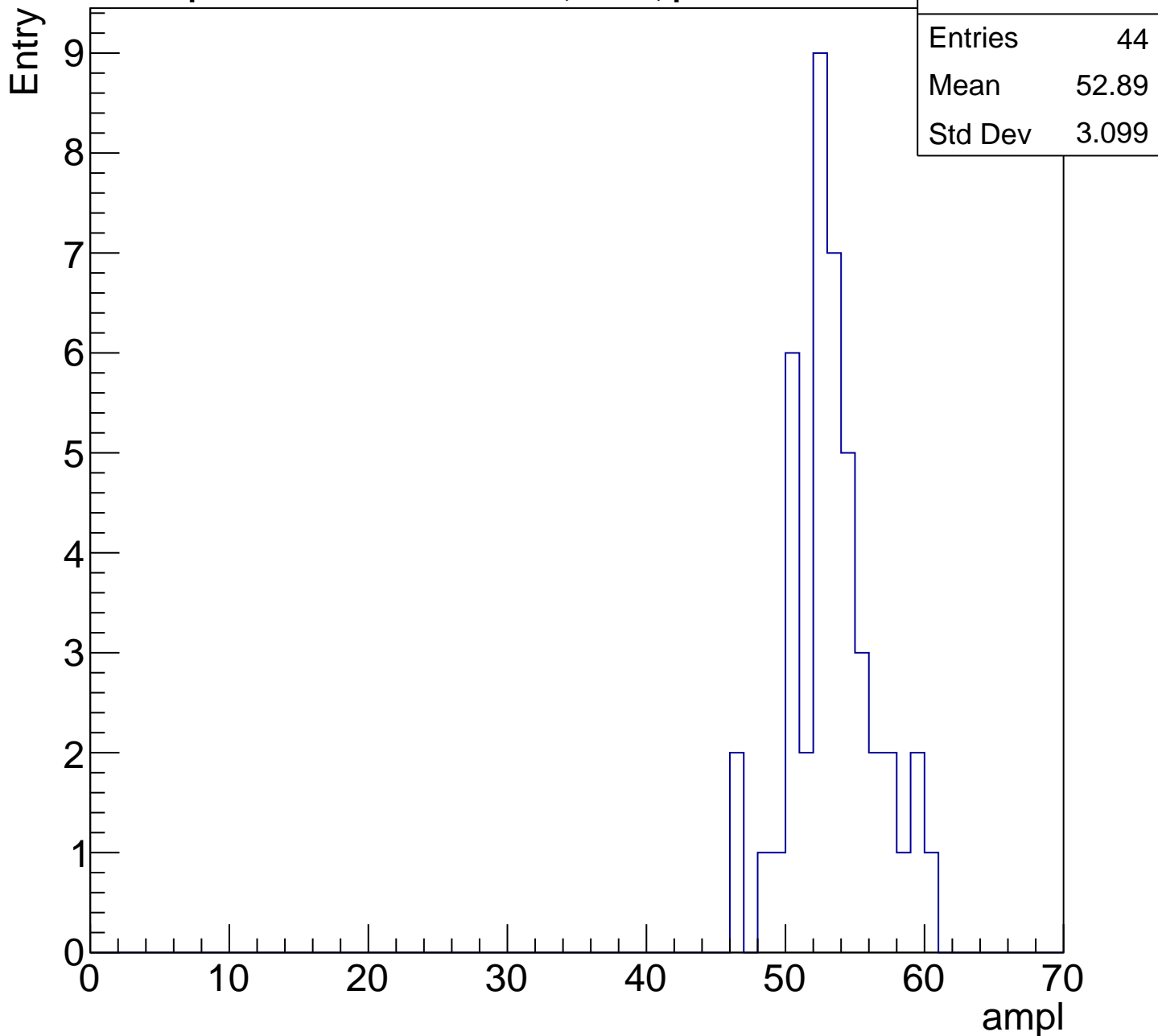
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



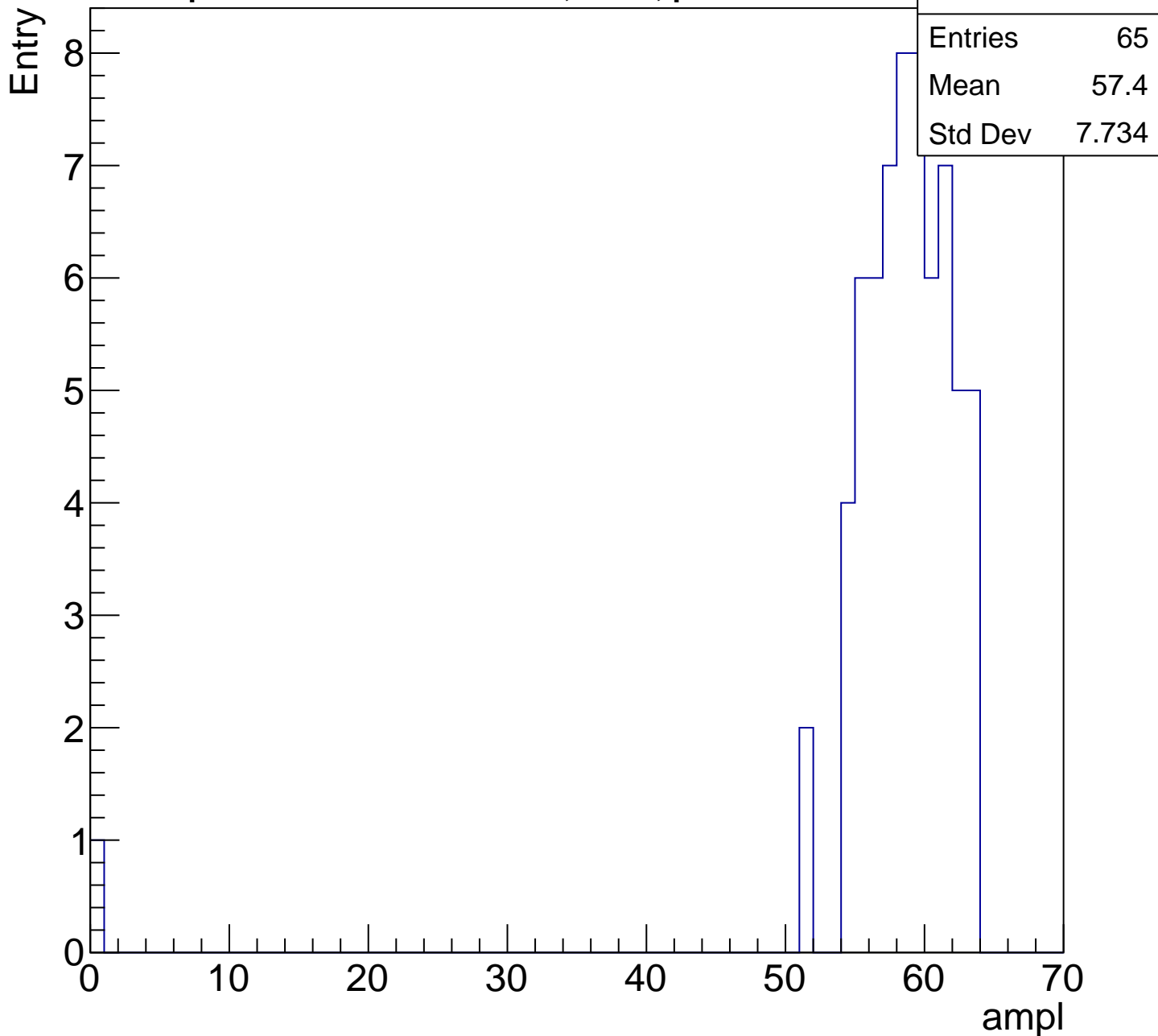
# B1L103S, U3-ch78, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U3-ch78, adc5

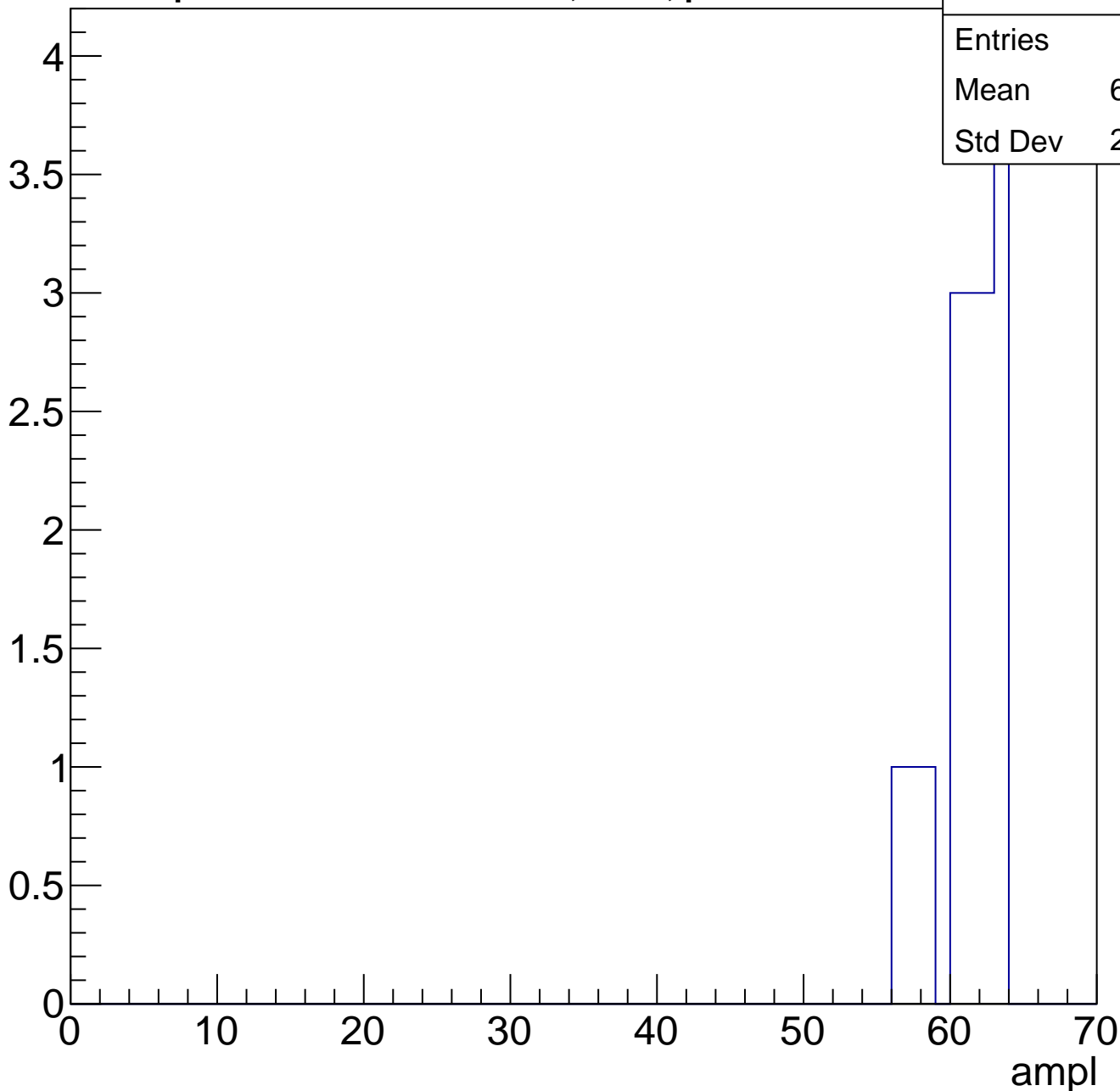
calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U3-ch78, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



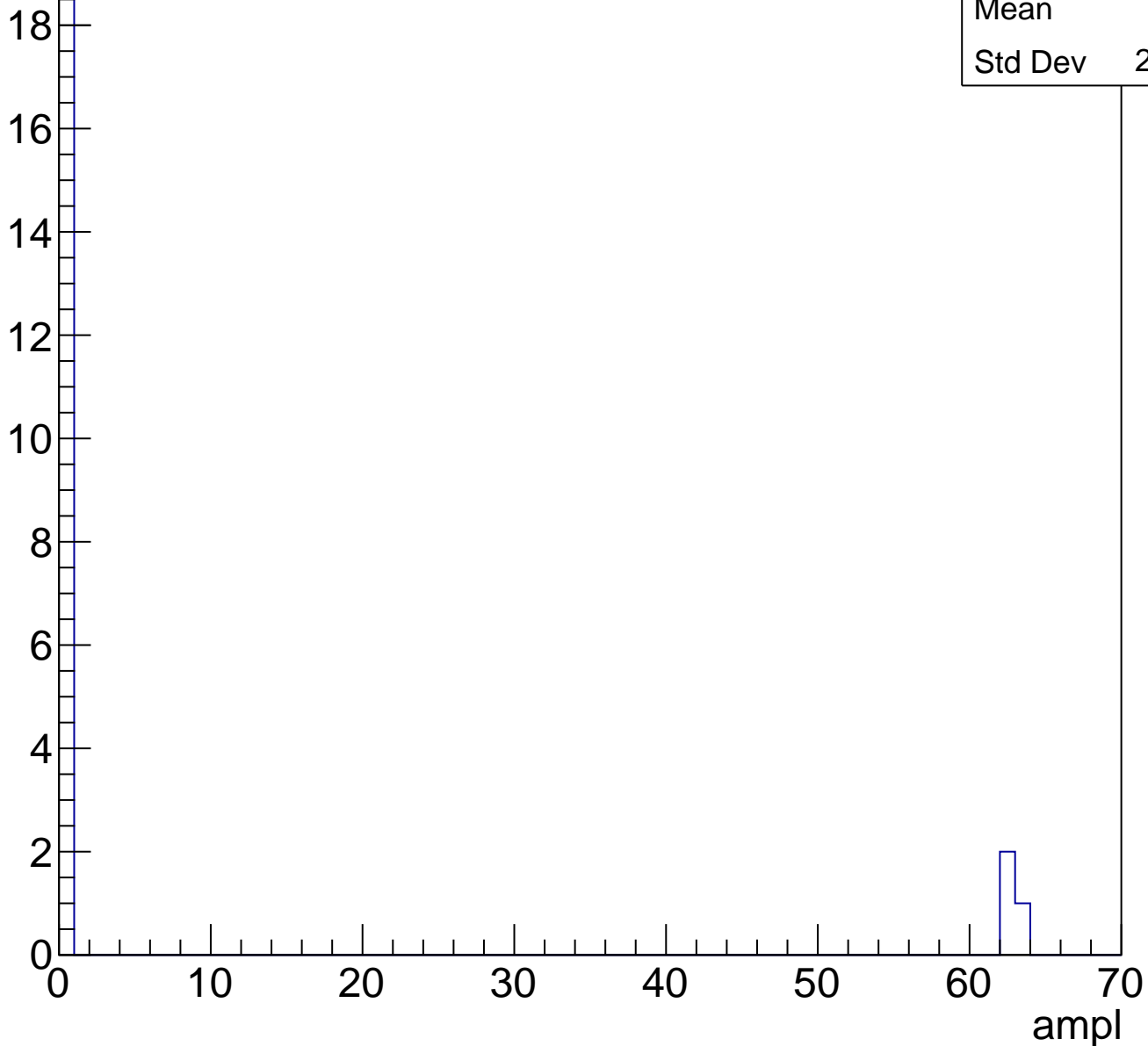
Entries	16
Mean	60.75
Std Dev	2.107



# B1L103S, U3-ch78, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	22
Mean	8.5
Std Dev	21.39

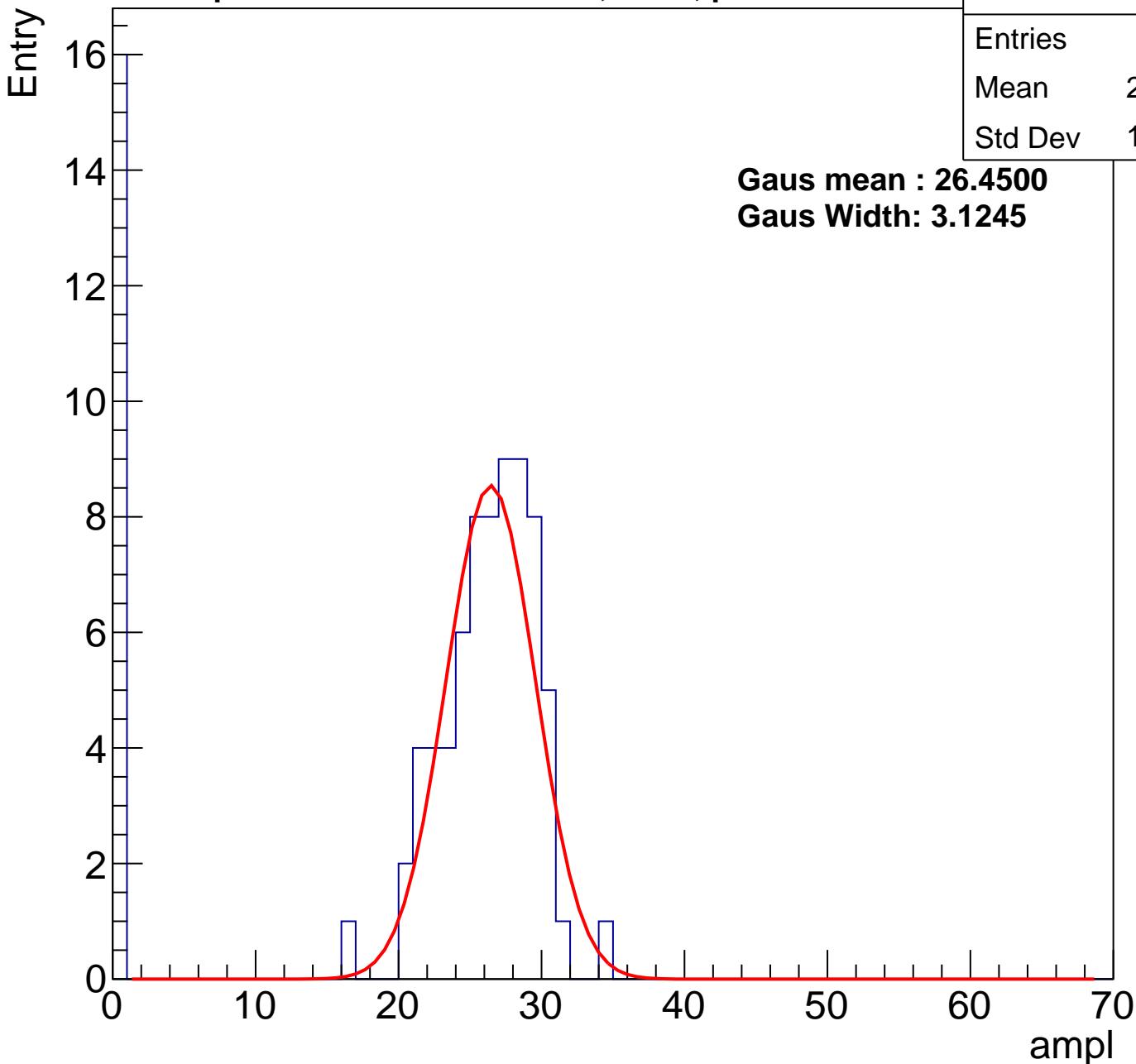
# B1L103S, U3-ch79, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	86
Mean	21.09
Std Dev	10.47

**Gaus mean : 26.4500**

**Gaus Width: 3.1245**



# B1L103S, U3-ch79, adc1

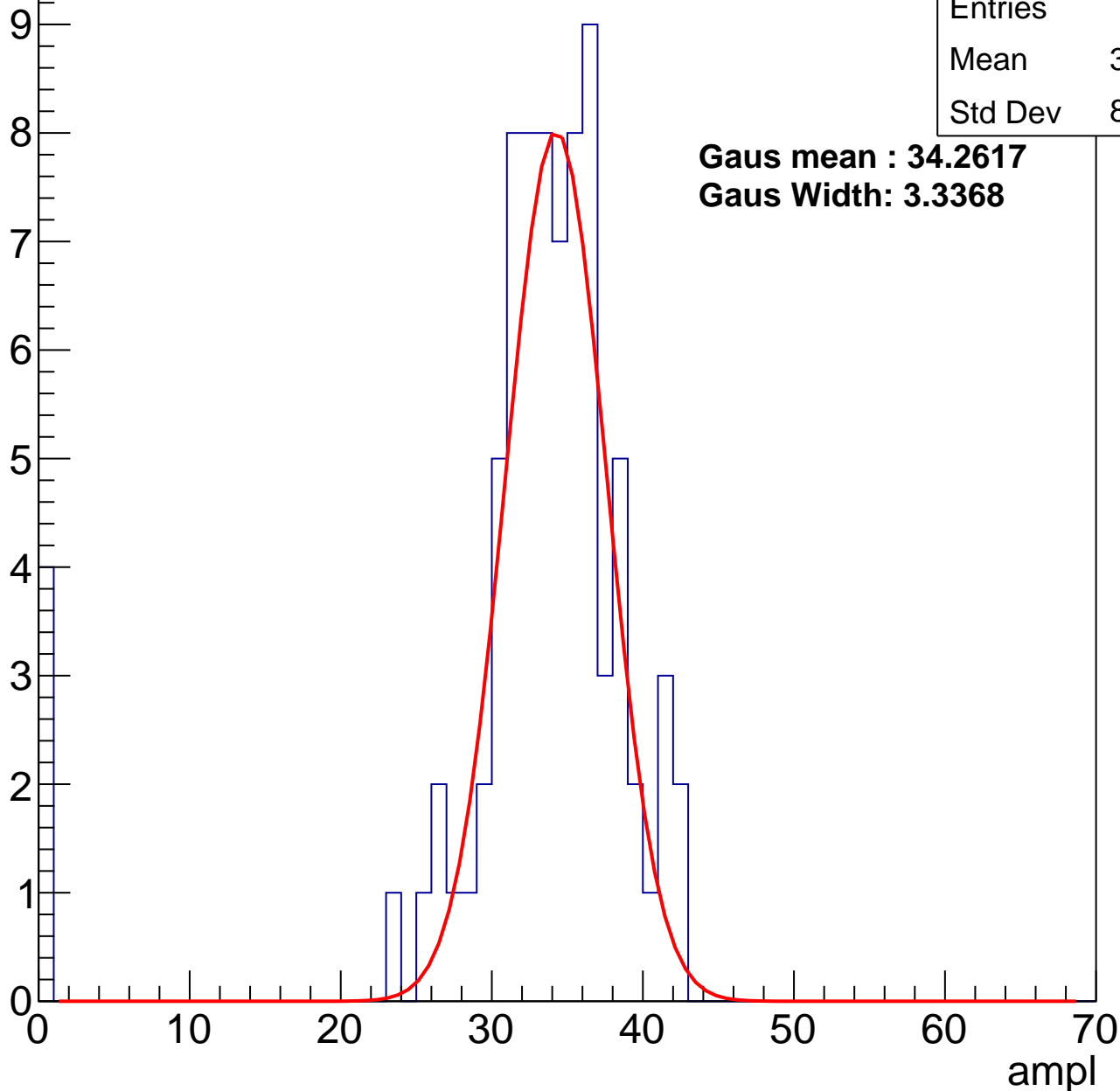
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	81
Mean	32.09
Std Dev	8.238

**Gaus mean : 34.2617**

**Gaus Width: 3.3368**



# B1L103S, U3-ch79, adc2

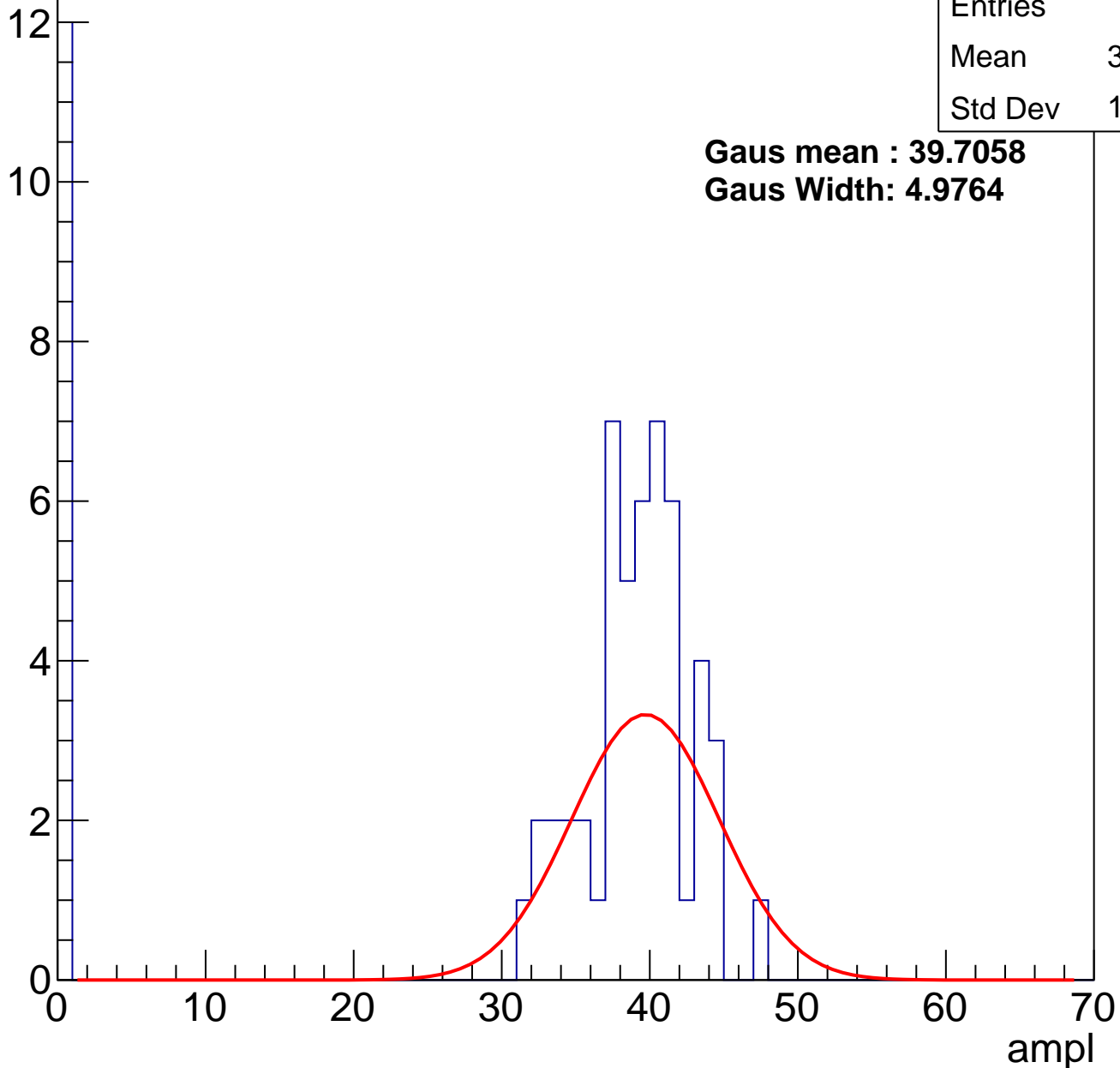
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	62
Mean	31.24
Std Dev	15.62

**Gaus mean : 39.7058**

**Gaus Width: 4.9764**

Entry

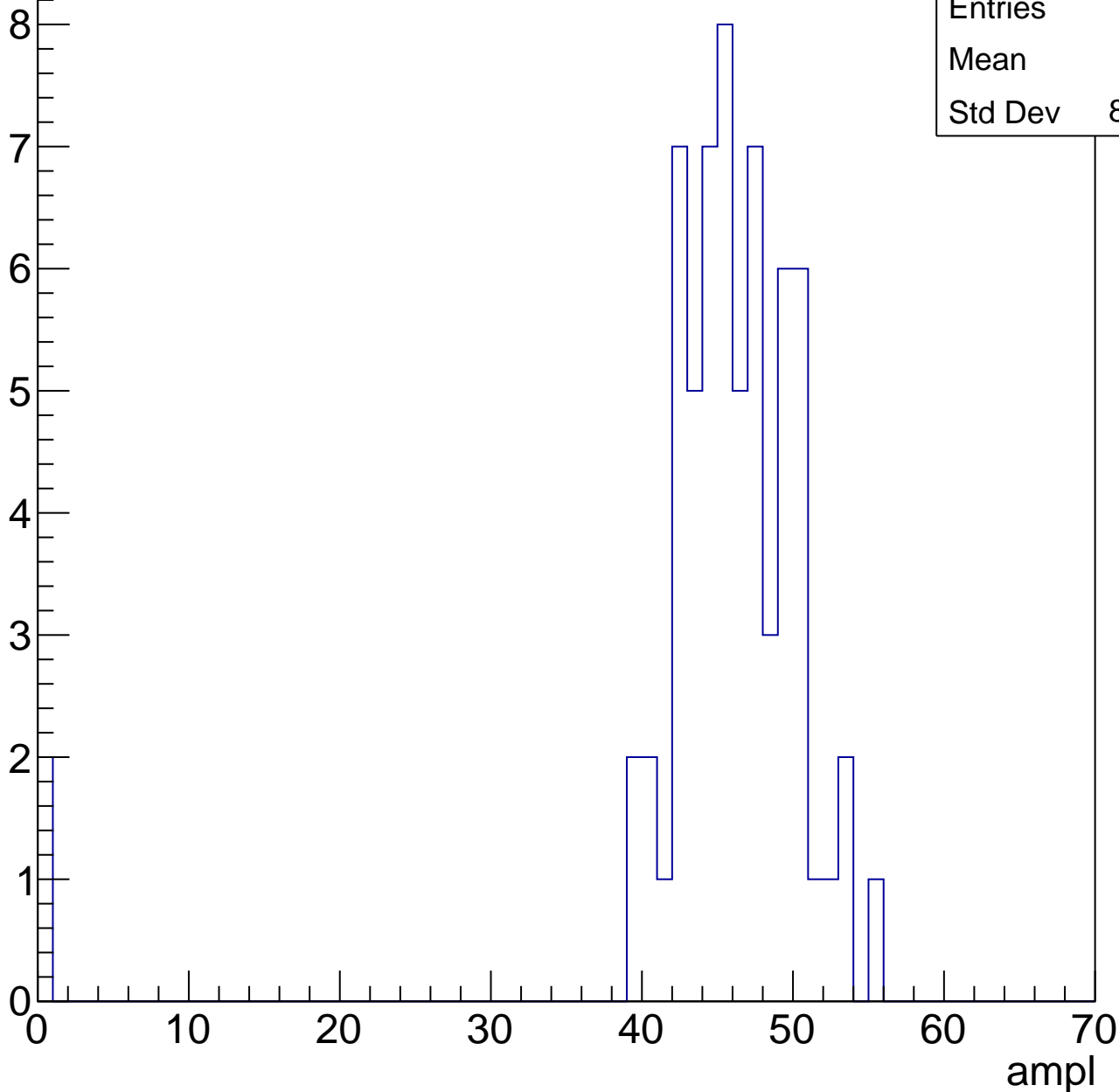


# B1L103S, U3-ch79, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	44.5
Std Dev	8.599

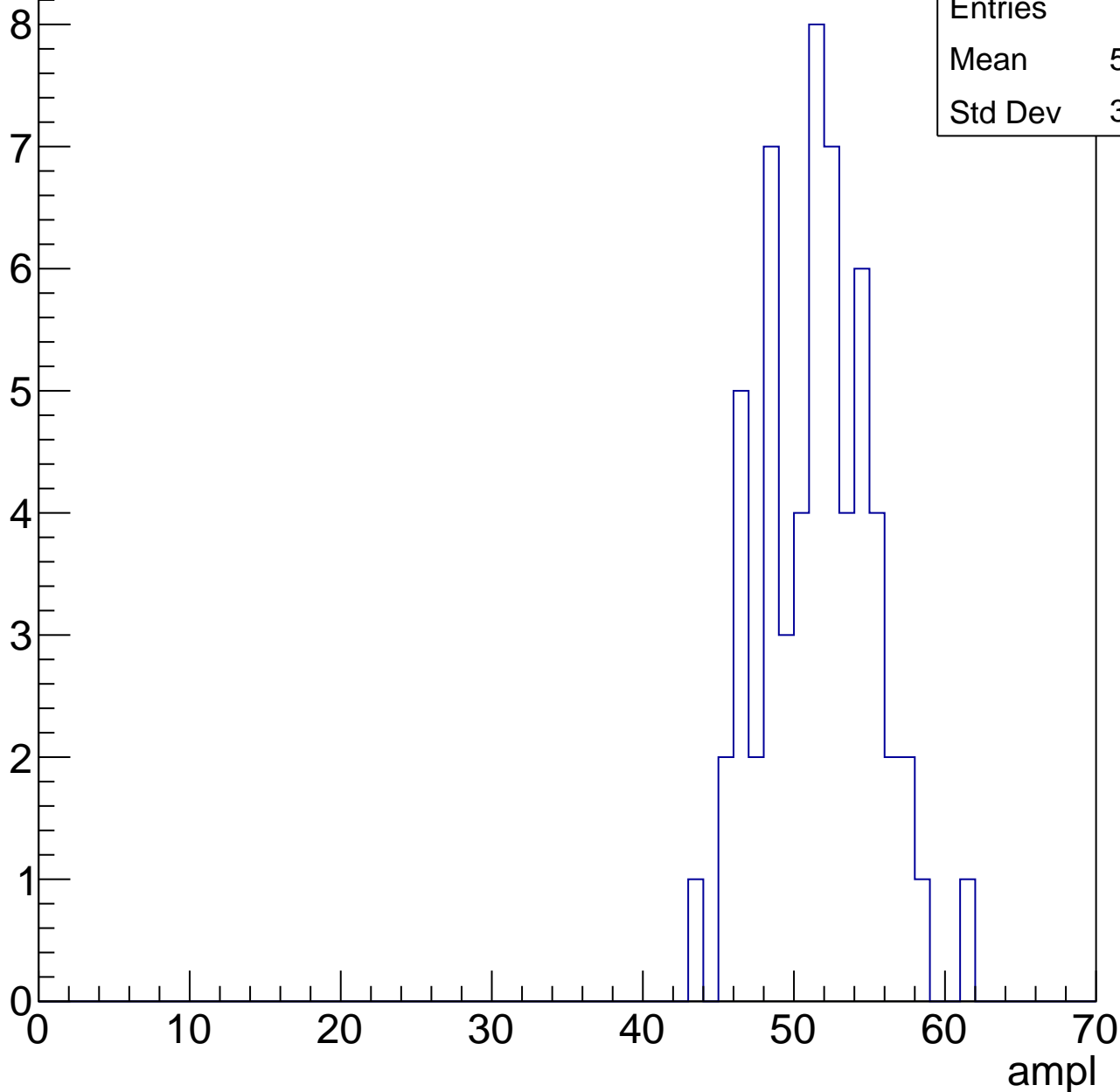


# B1L103S, U3-ch79, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	51.07
Std Dev	3.645

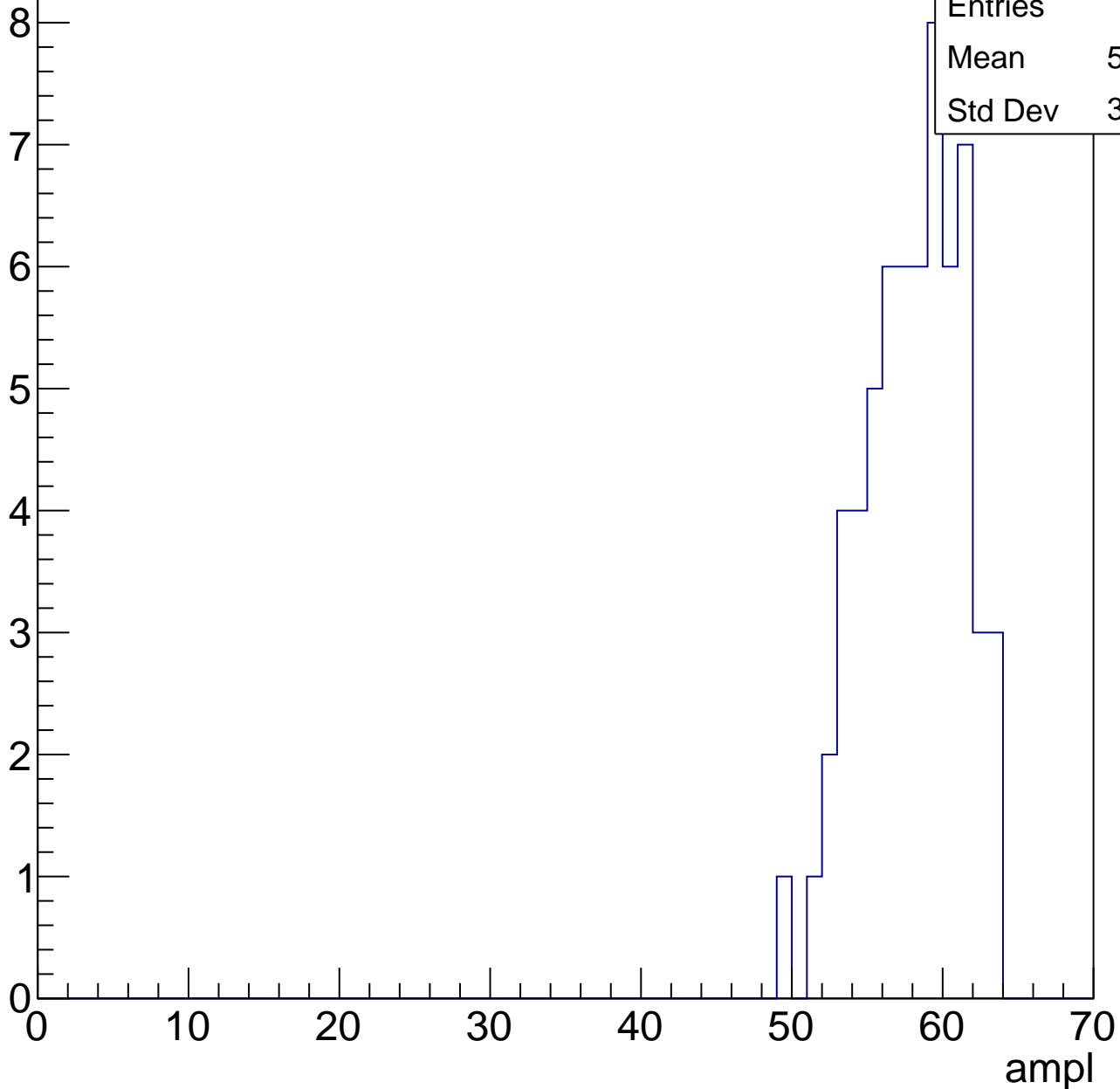


# B1L103S, U3-ch79, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

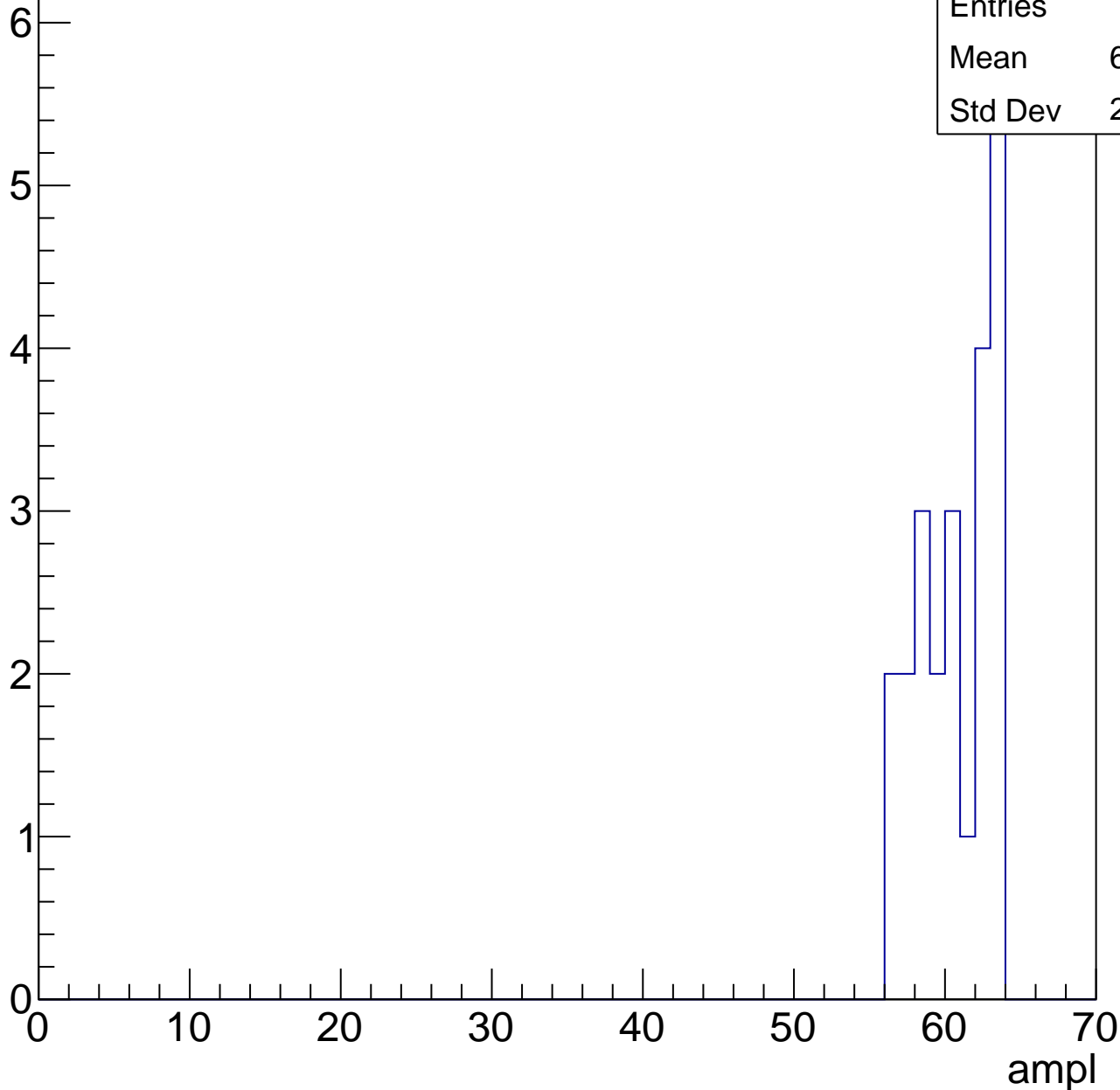
Entries	62
Mean	57.53
Std Dev	3.226



# B1L103S, U3-ch79, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



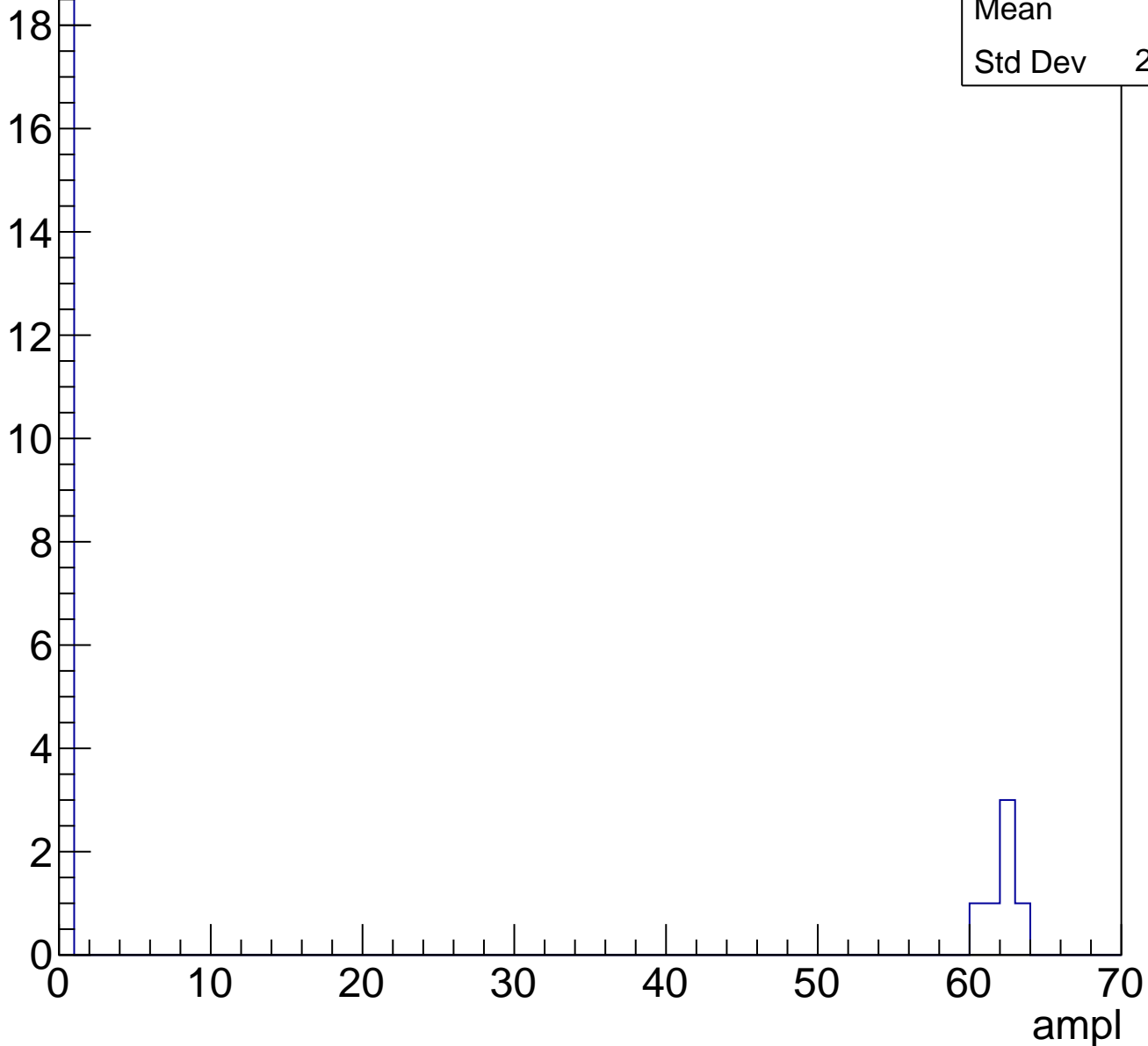


# B1L103S, U3-ch79, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	25
Mean	14.8
Std Dev	26.34

Entry



# B1L103S, U3-ch80, adc0

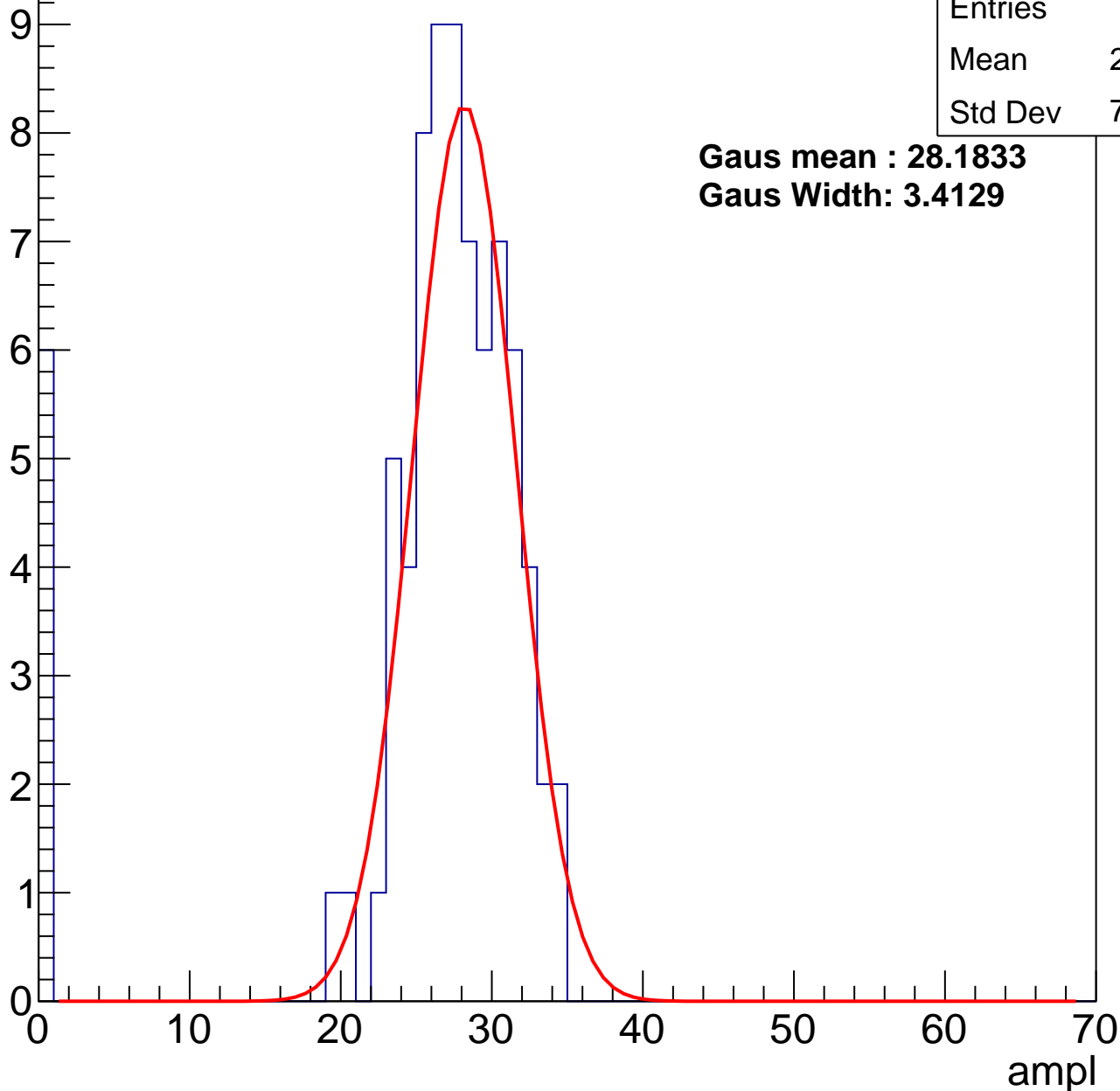
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	78
Mean	25.35
Std Dev	7.939

**Gaus mean : 28.1833**

**Gaus Width: 3.4129**



# B1L103S, U3-ch80, adc1

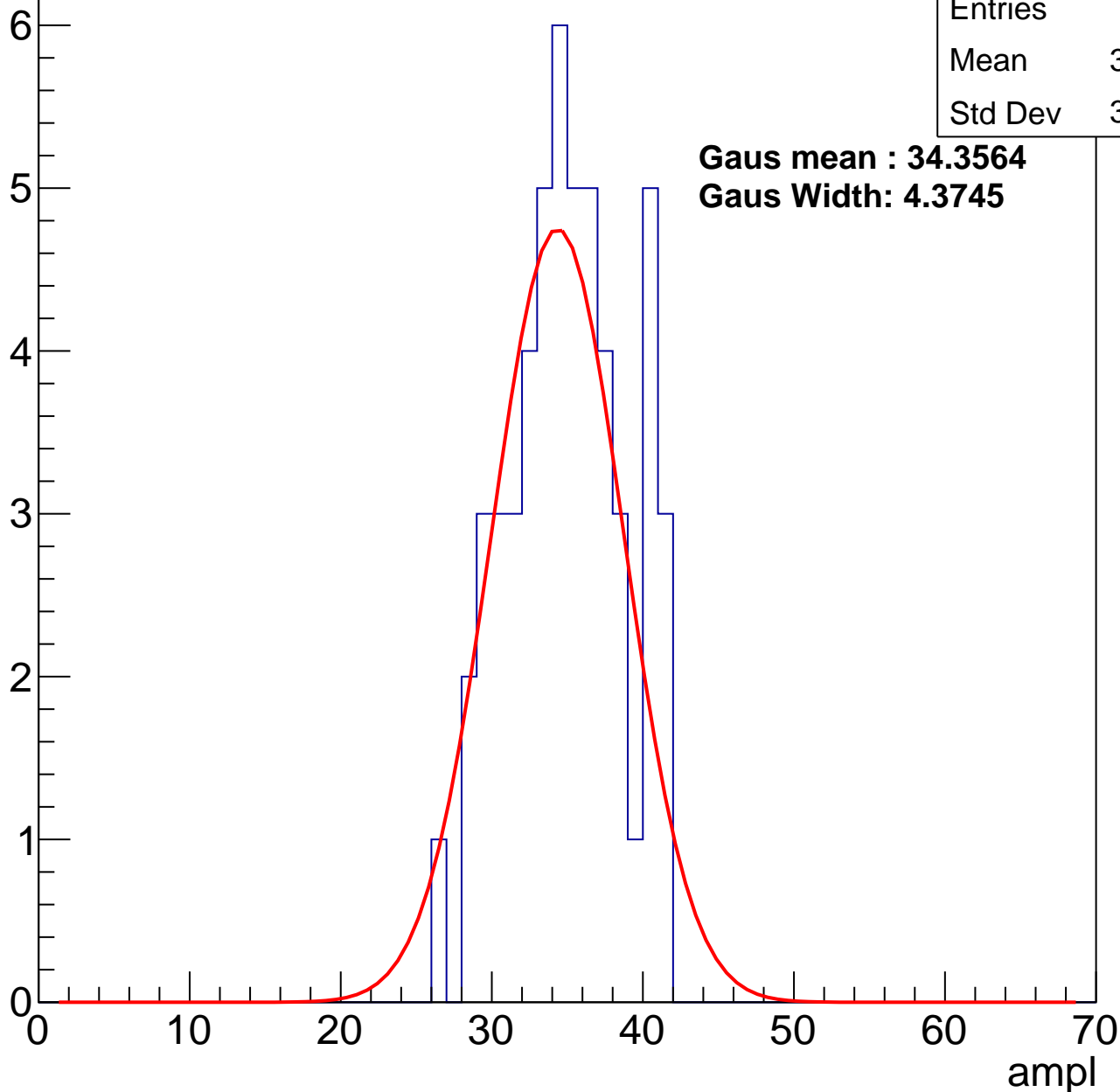
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	53
Mean	34.49
Std Dev	3.775

**Gaus mean : 34.3564**

**Gaus Width: 4.3745**



# B1L103S, U3-ch80, adc2

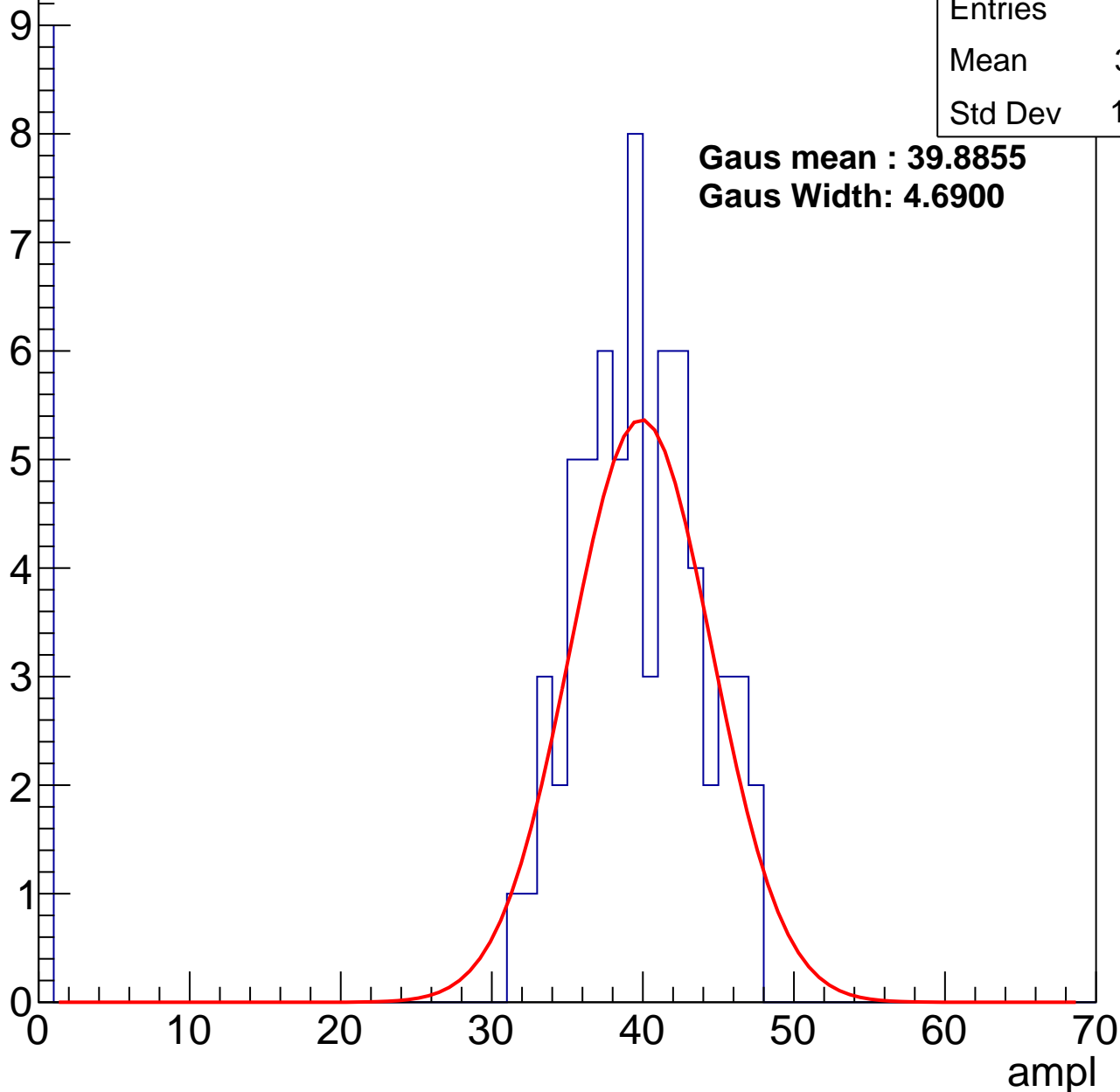
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	74
Mean	34.51
Std Dev	13.36

**Gaus mean : 39.8855**

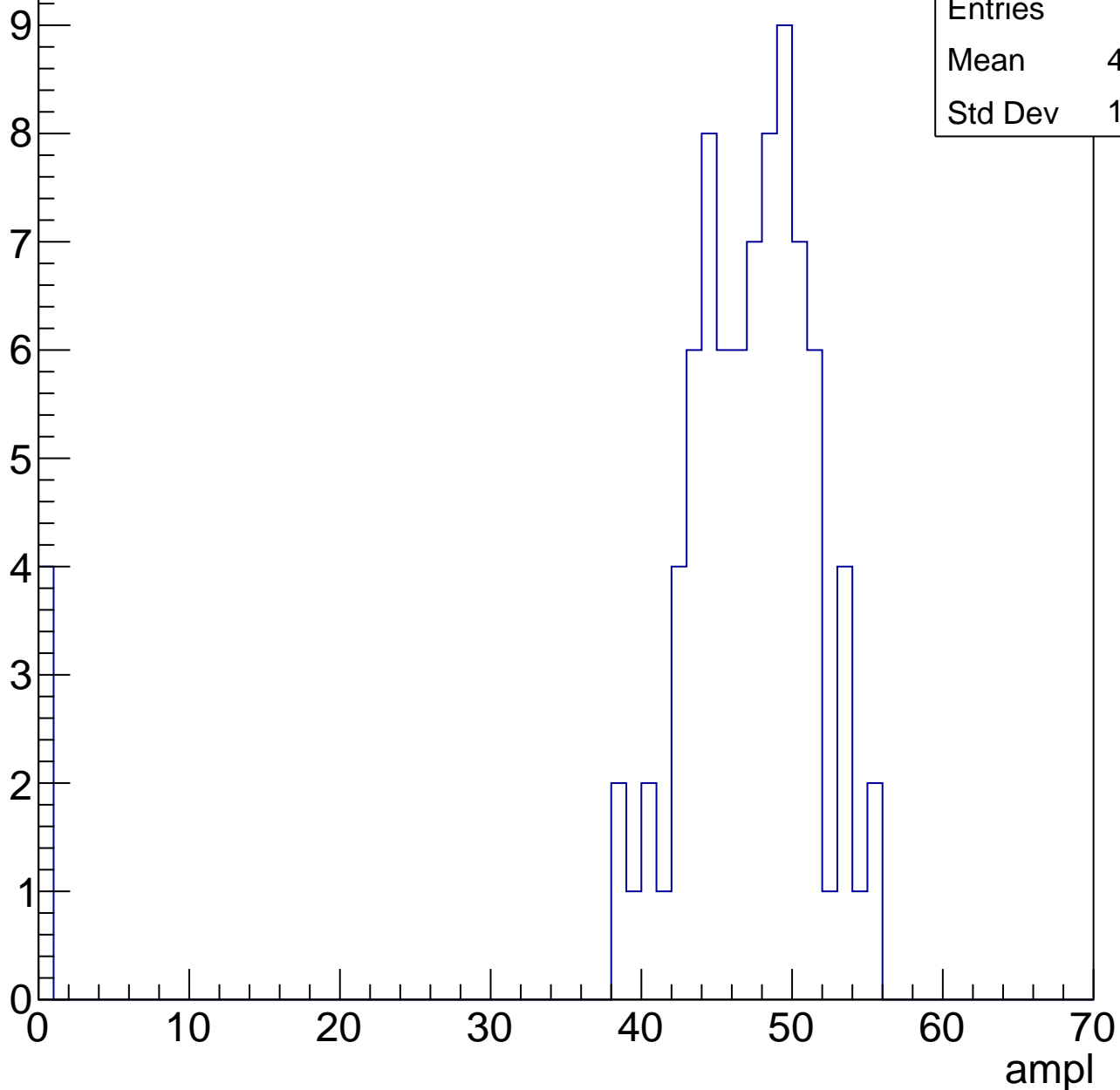
**Gaus Width: 4.6900**



# B1L103S, U3-ch80, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

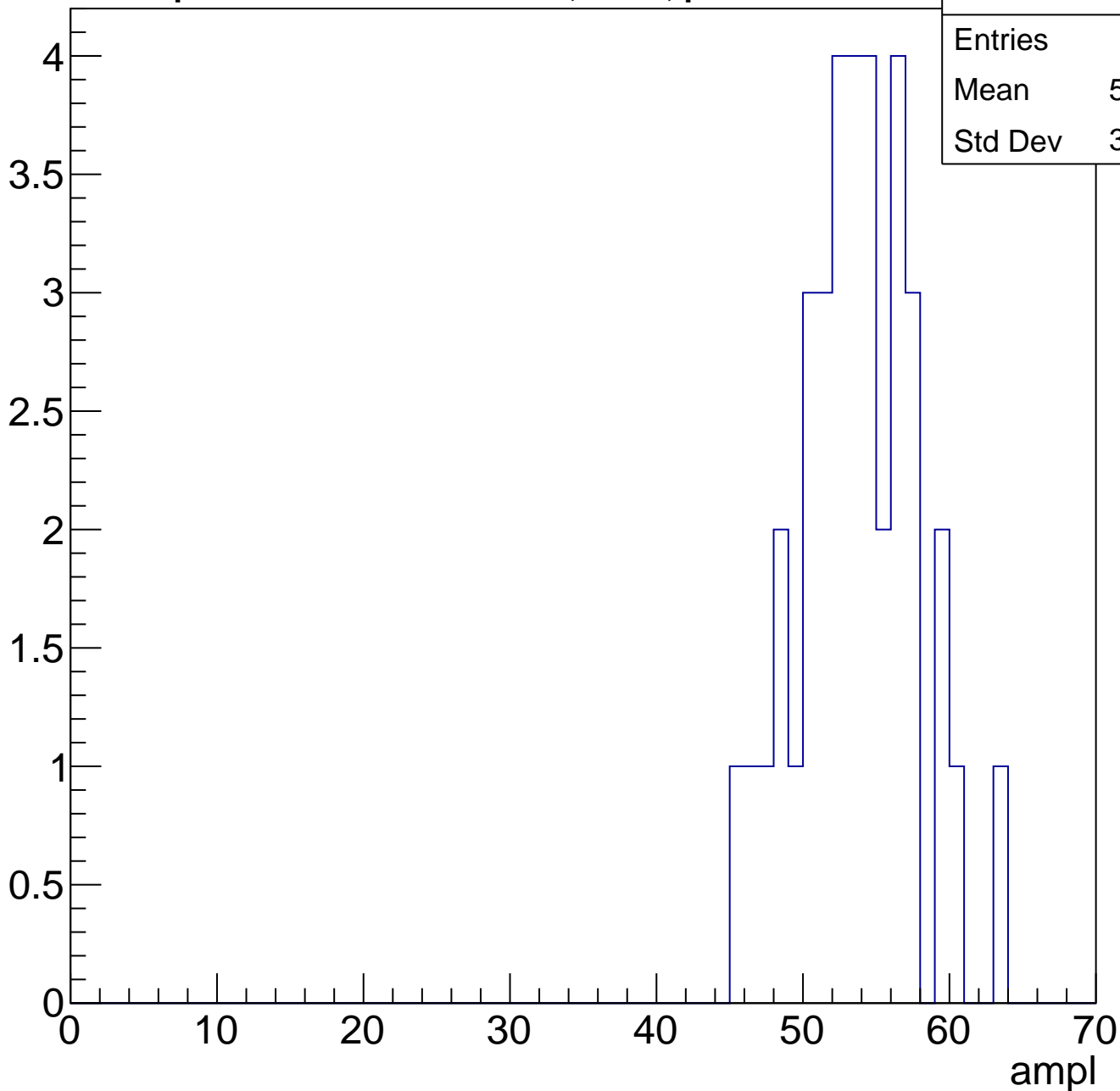
Entry



# B1L103S, U3-ch80, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

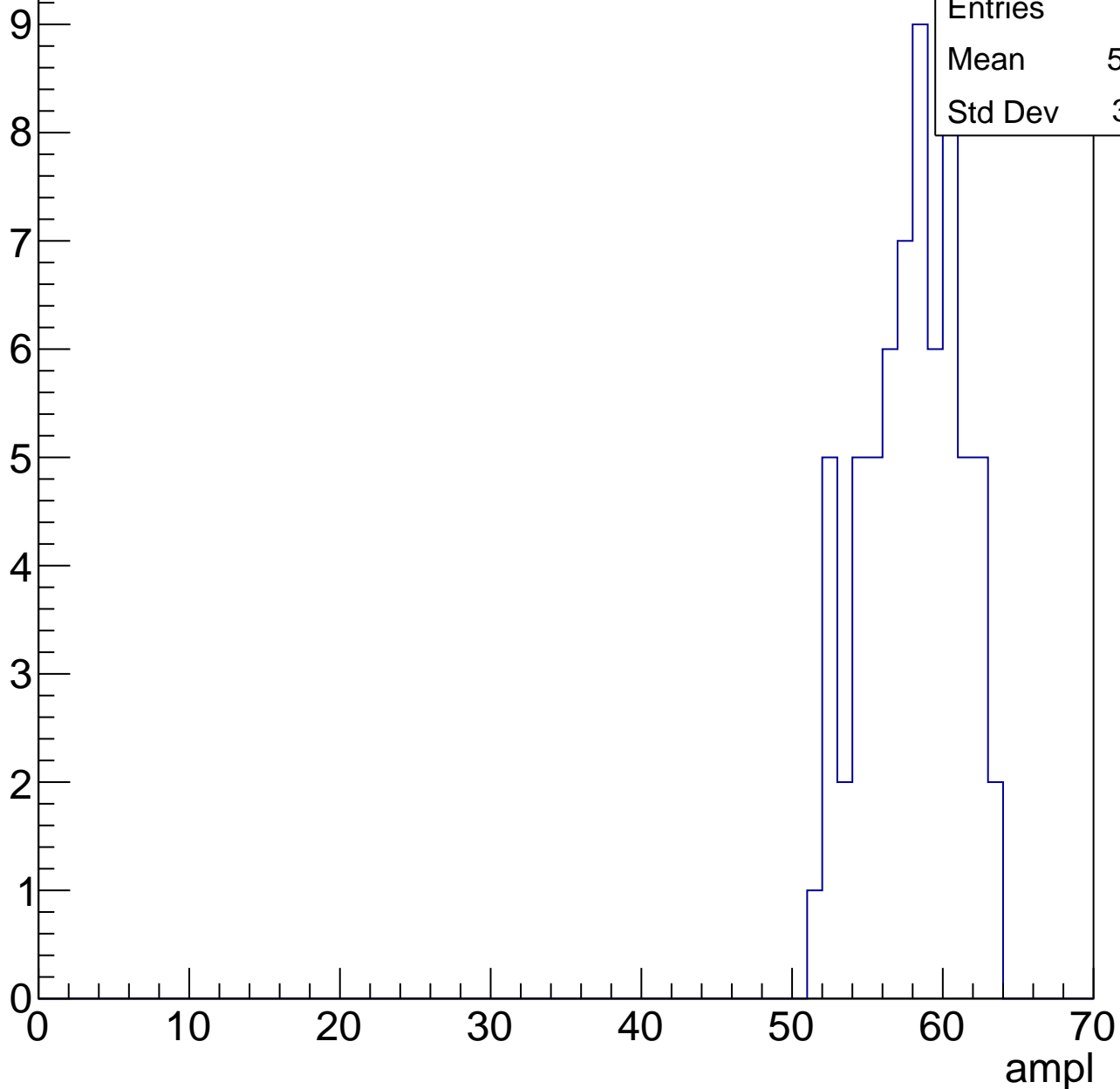
Entry



# B1L103S, U3-ch80, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



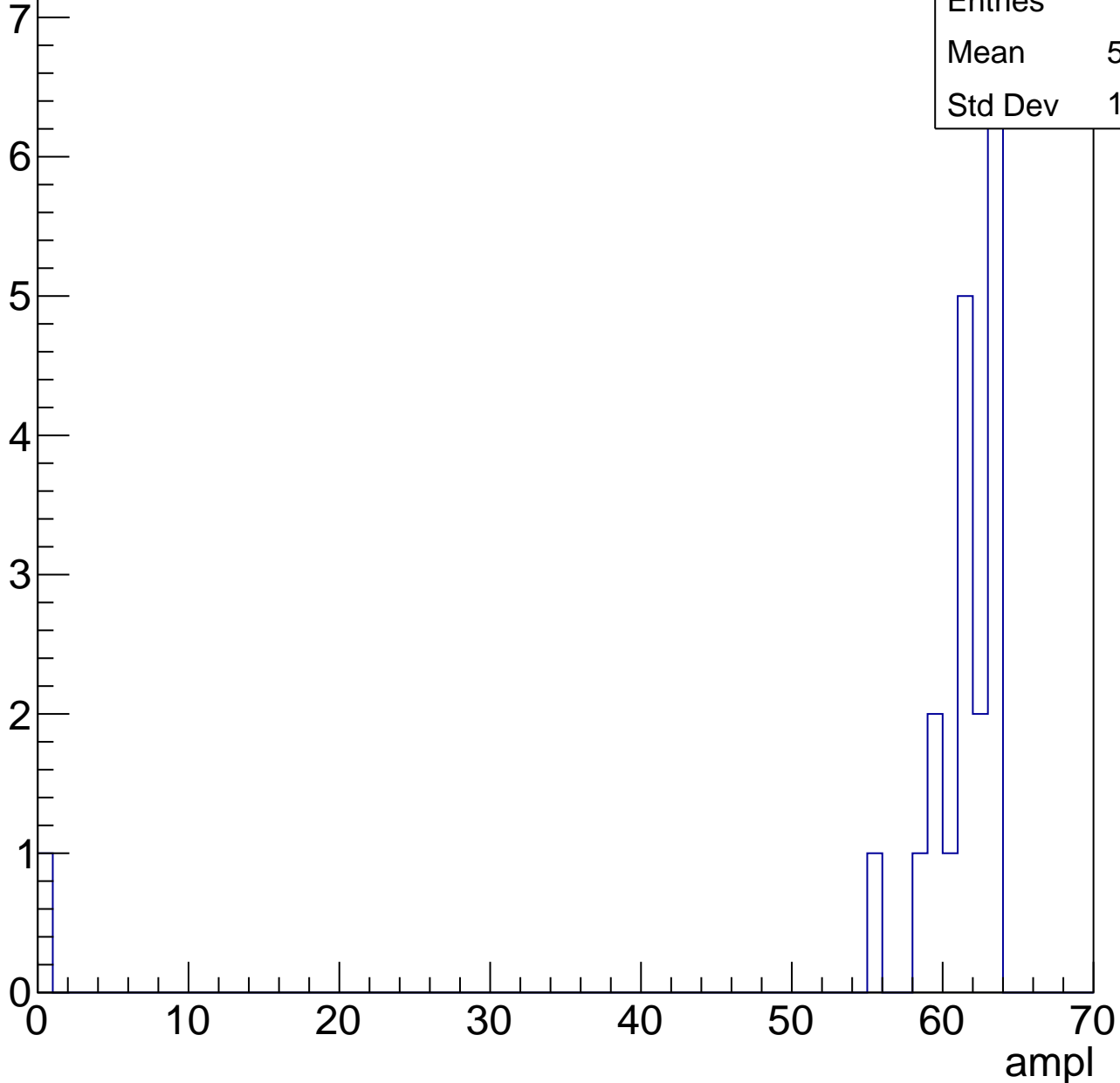
Entries	66
Mean	57.48
Std Dev	3.091

# B1L103S, U3-ch80, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	20
Mean	58.05
Std Dev	13.47



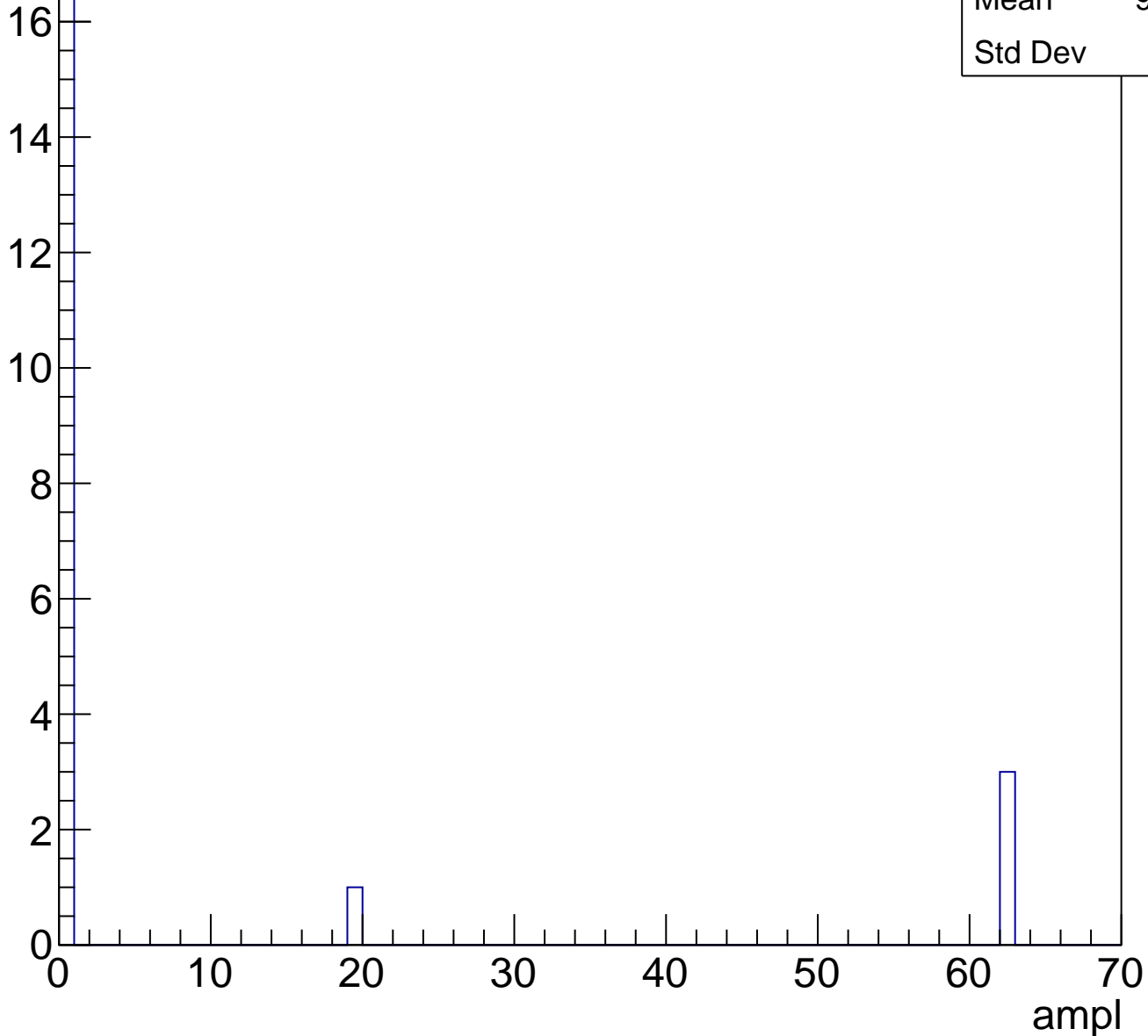


# B1L103S, U3-ch80, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	9.762
Std Dev	21.7

Entry



# B1L103S, U3-ch81, adc0

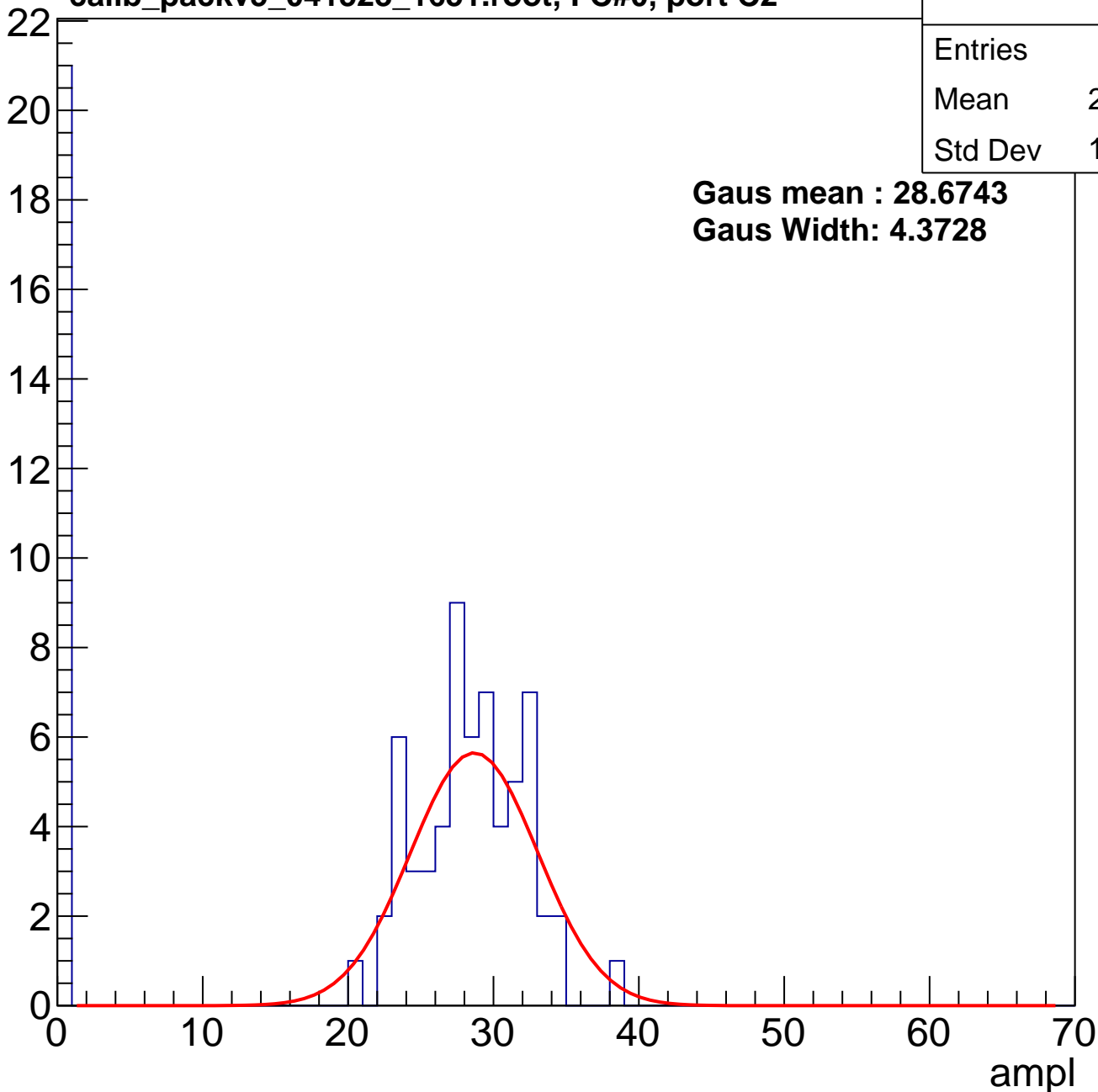
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	83
Mean	20.94
Std Dev	12.57

**Gaus mean : 28.6743**

**Gaus Width: 4.3728**

Entry



# B1L103S, U3-ch81, adc1

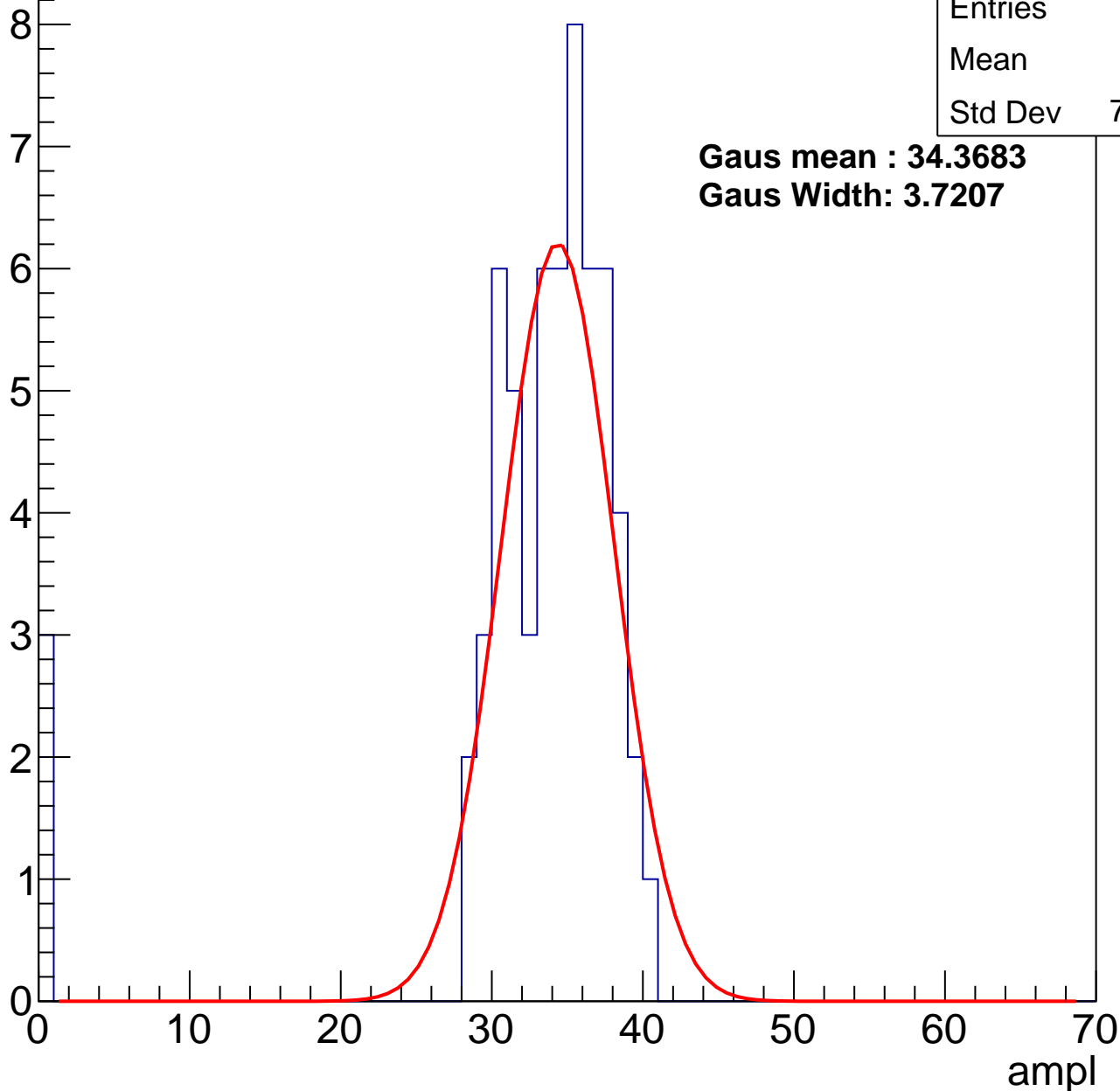
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	32.2
Std Dev	7.905

**Gaus mean : 34.3683**

**Gaus Width: 3.7207**



# B1L103S, U3-ch81, adc2

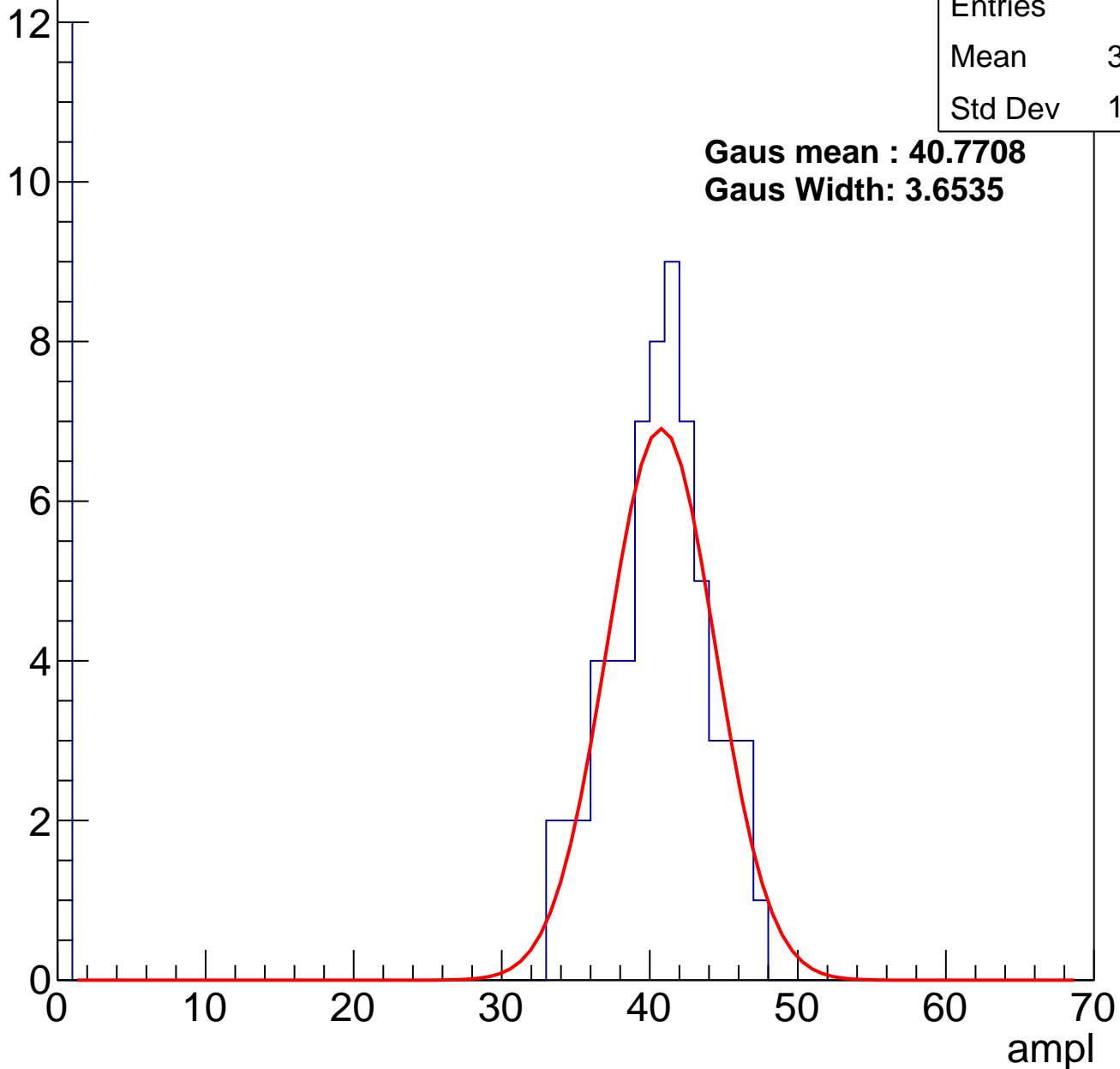
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	76
Mean	33.83
Std Dev	14.96

**Gaus mean : 40.7708**

**Gaus Width: 3.6535**

Entry

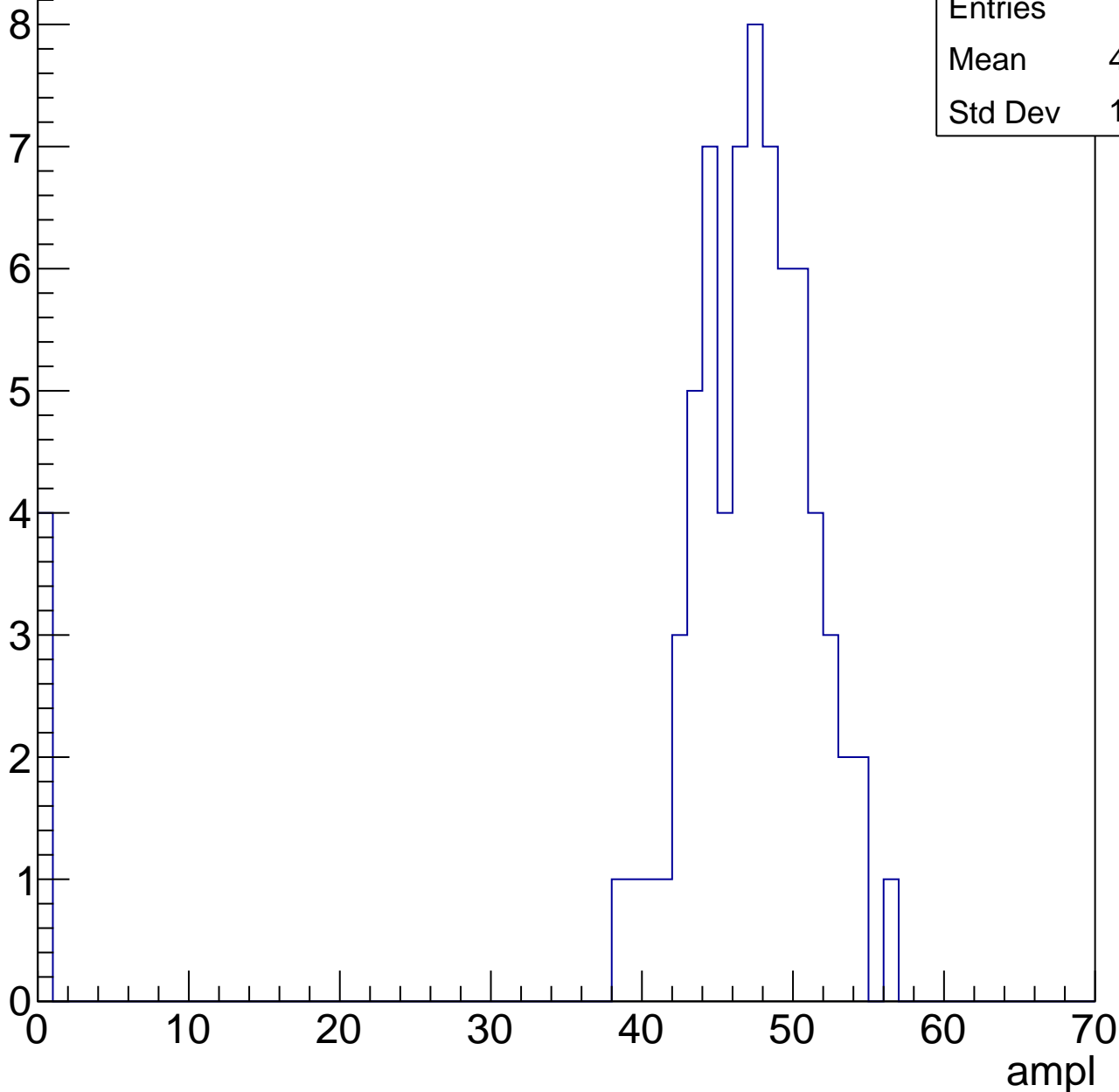


# B1L103S, U3-ch81, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	44.45
Std Dev	11.29

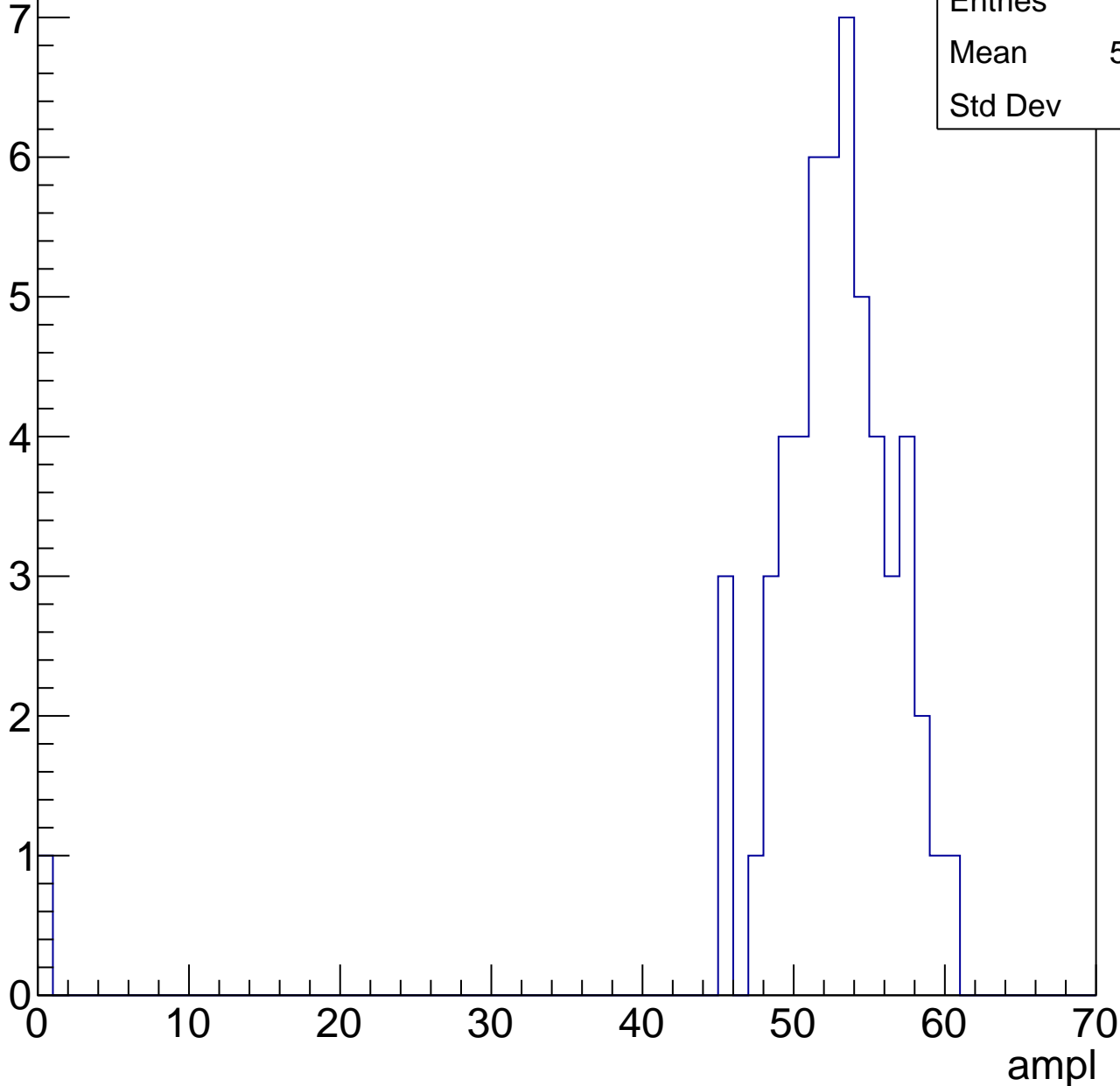


# B1L103S, U3-ch81, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

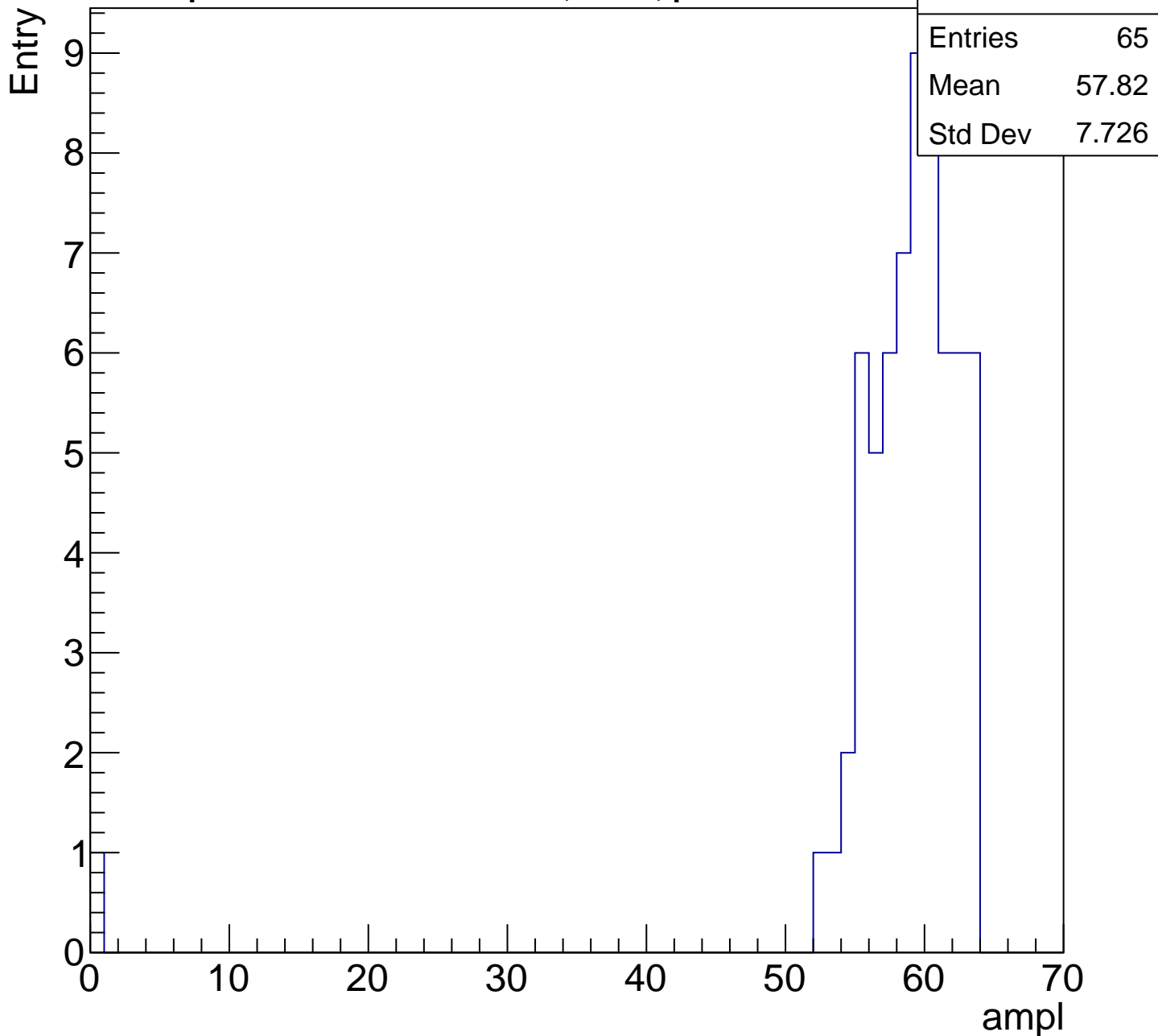
Entry

Entries	55
Mean	51.49
Std Dev	7.82



# B1L103S, U3-ch81, adc5

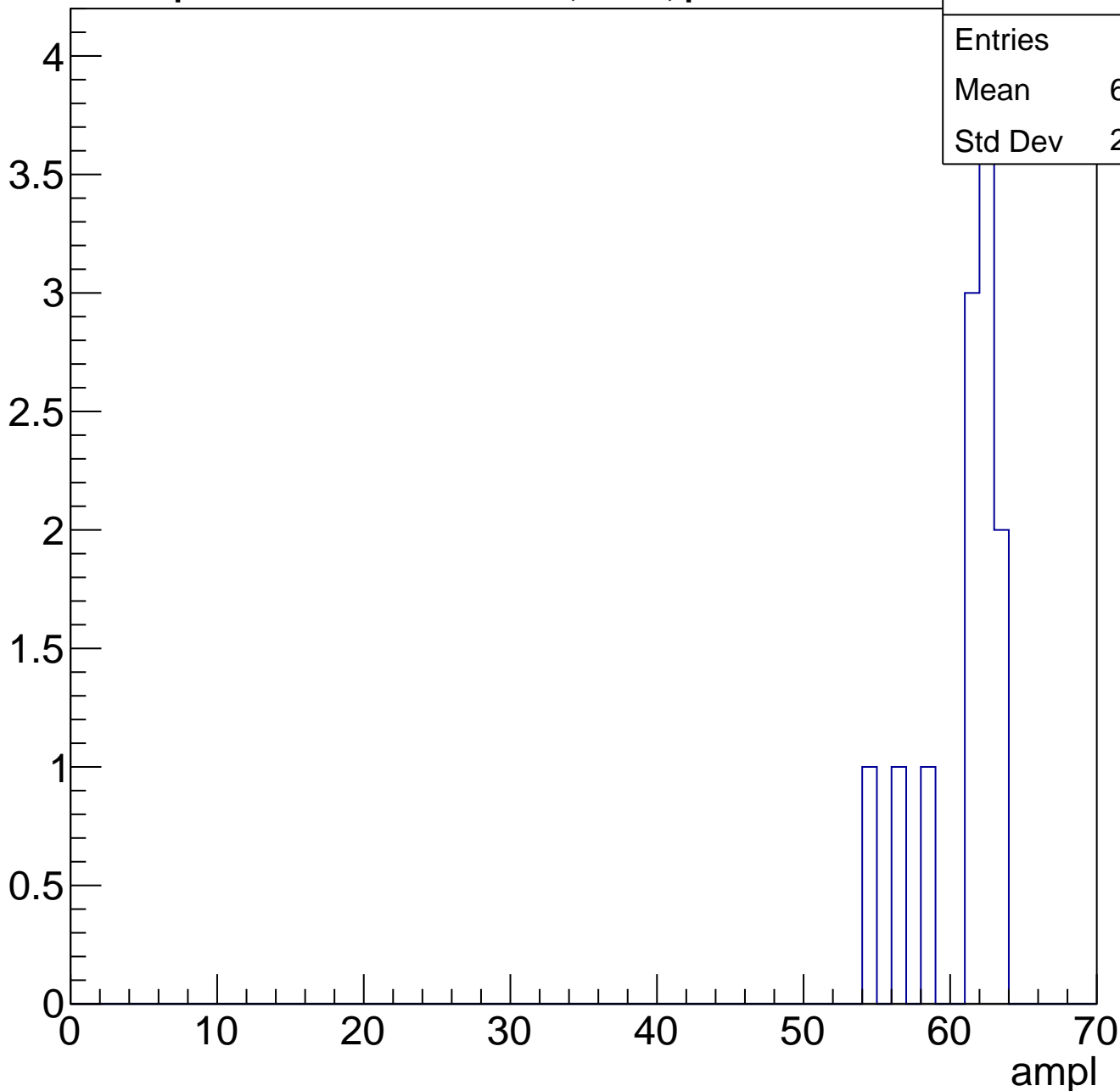
calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U3-ch81, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U3-ch81, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	22
Mean	8.5
Std Dev	21.39

ampl

0 10 20 30 40 50 60 70

# B1L103S, U3-ch82, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	189
Mean	10.37
Std Dev	12.17

**Gaus mean : 26.8588**

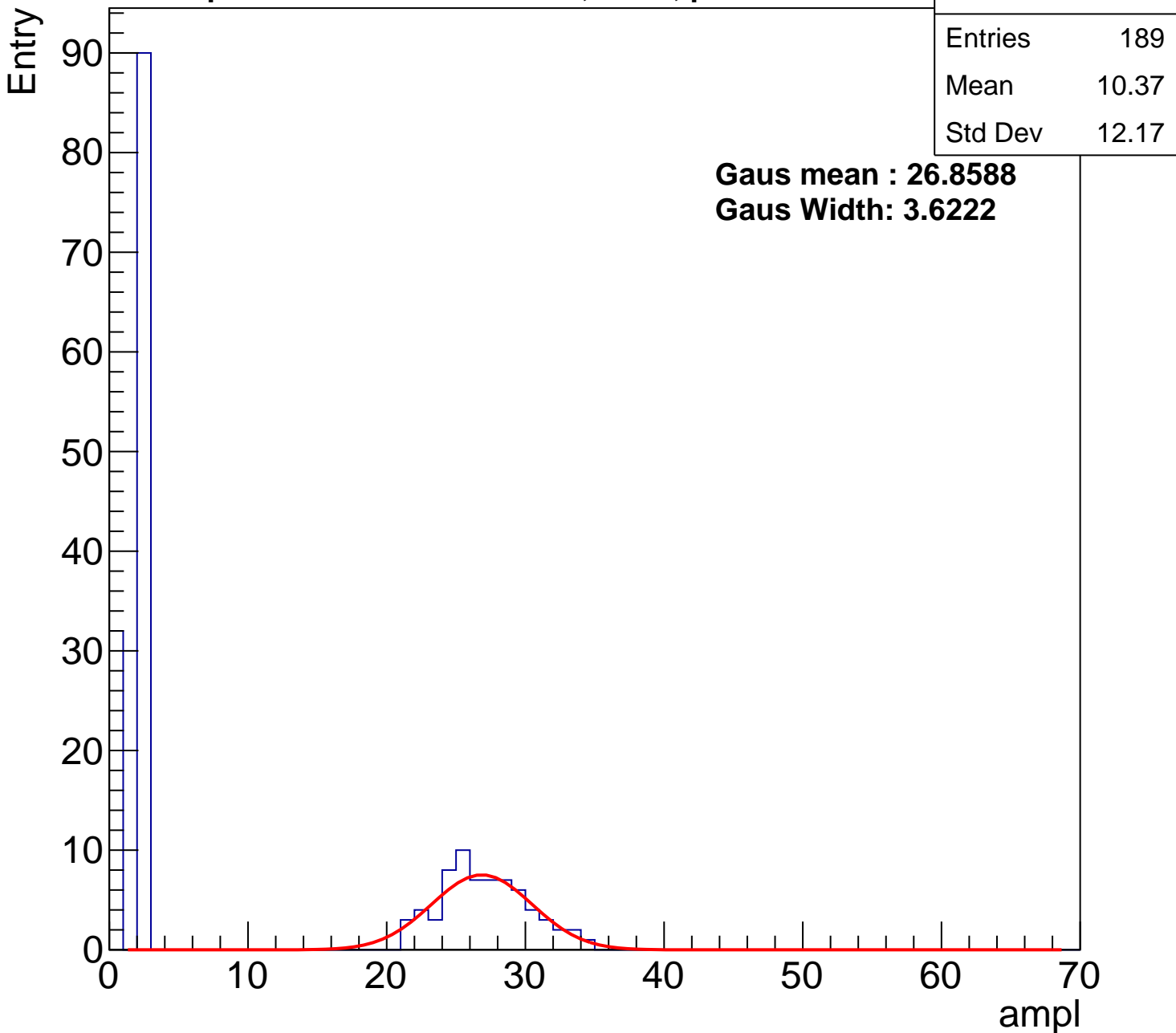
**Gaus Width: 3.6222**

Entry

90  
80  
70  
60  
50  
40  
30  
20  
10  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U3-ch82, adc1

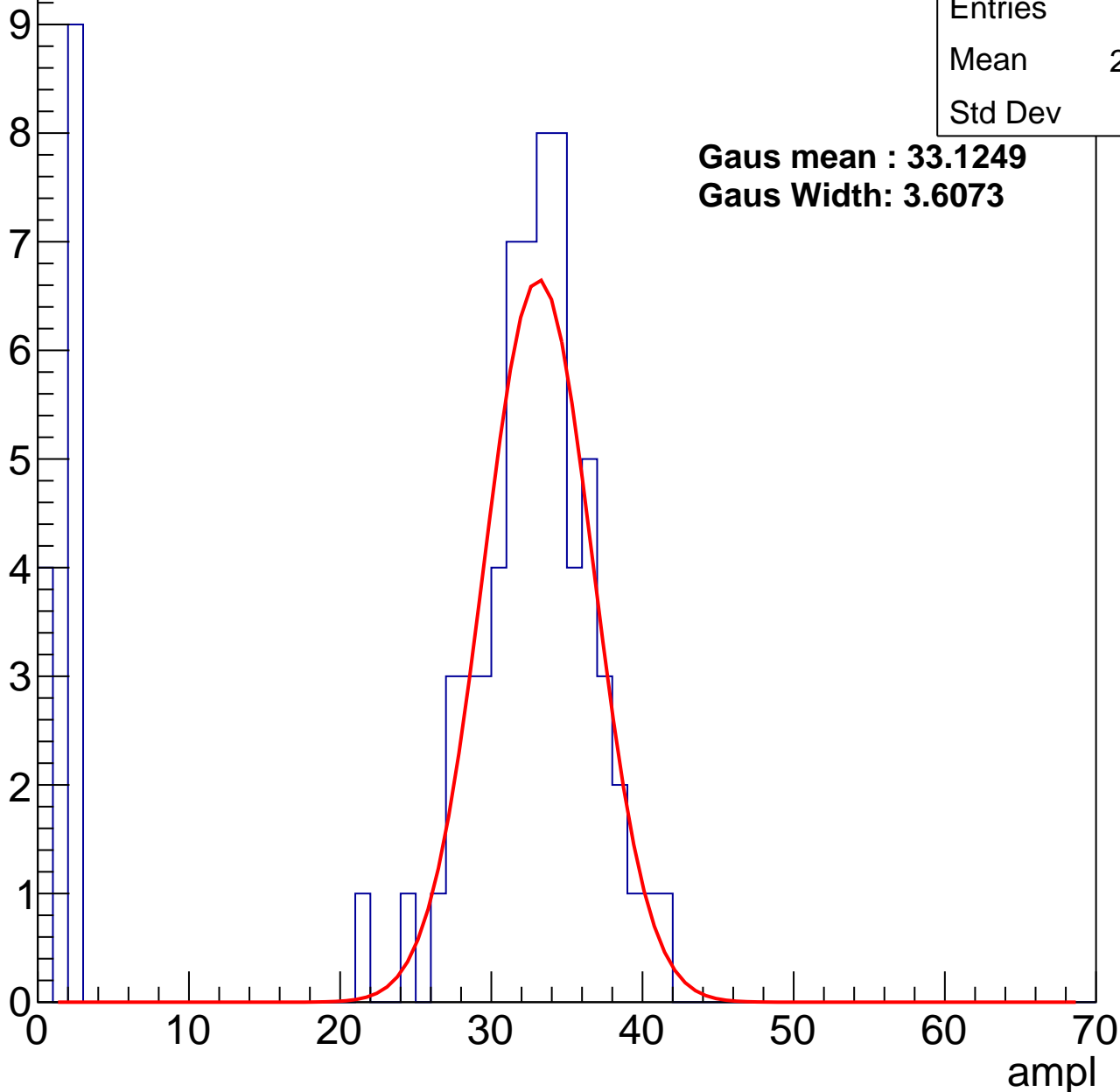
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	76
Mean	27.17
Std Dev	12.2

**Gaus mean : 33.1249**

**Gaus Width: 3.6073**



# B1L103S, U3-ch82, adc2

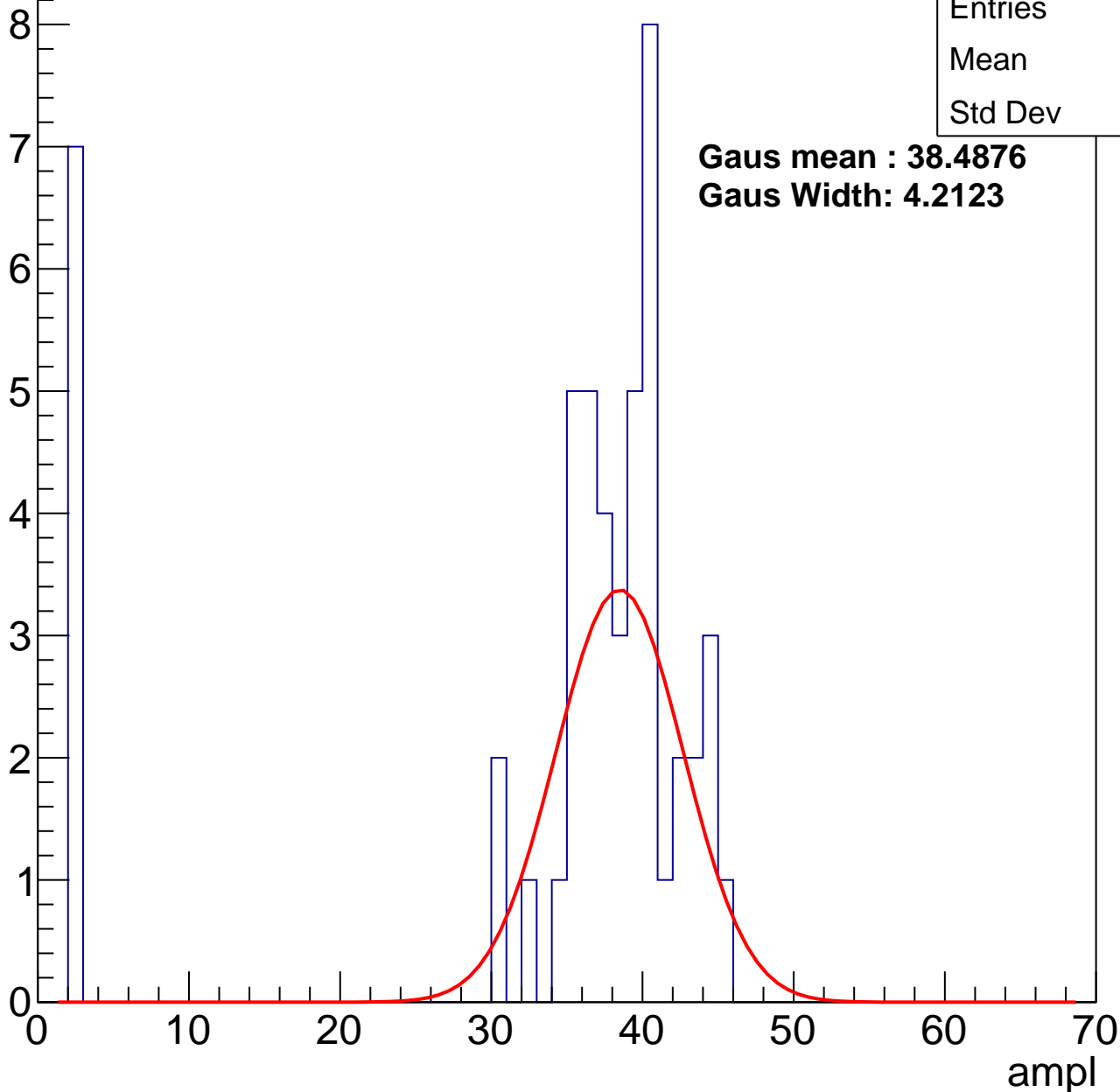
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	50
Mean	33.2
Std Dev	13

**Gaus mean : 38.4876**

**Gaus Width: 4.2123**

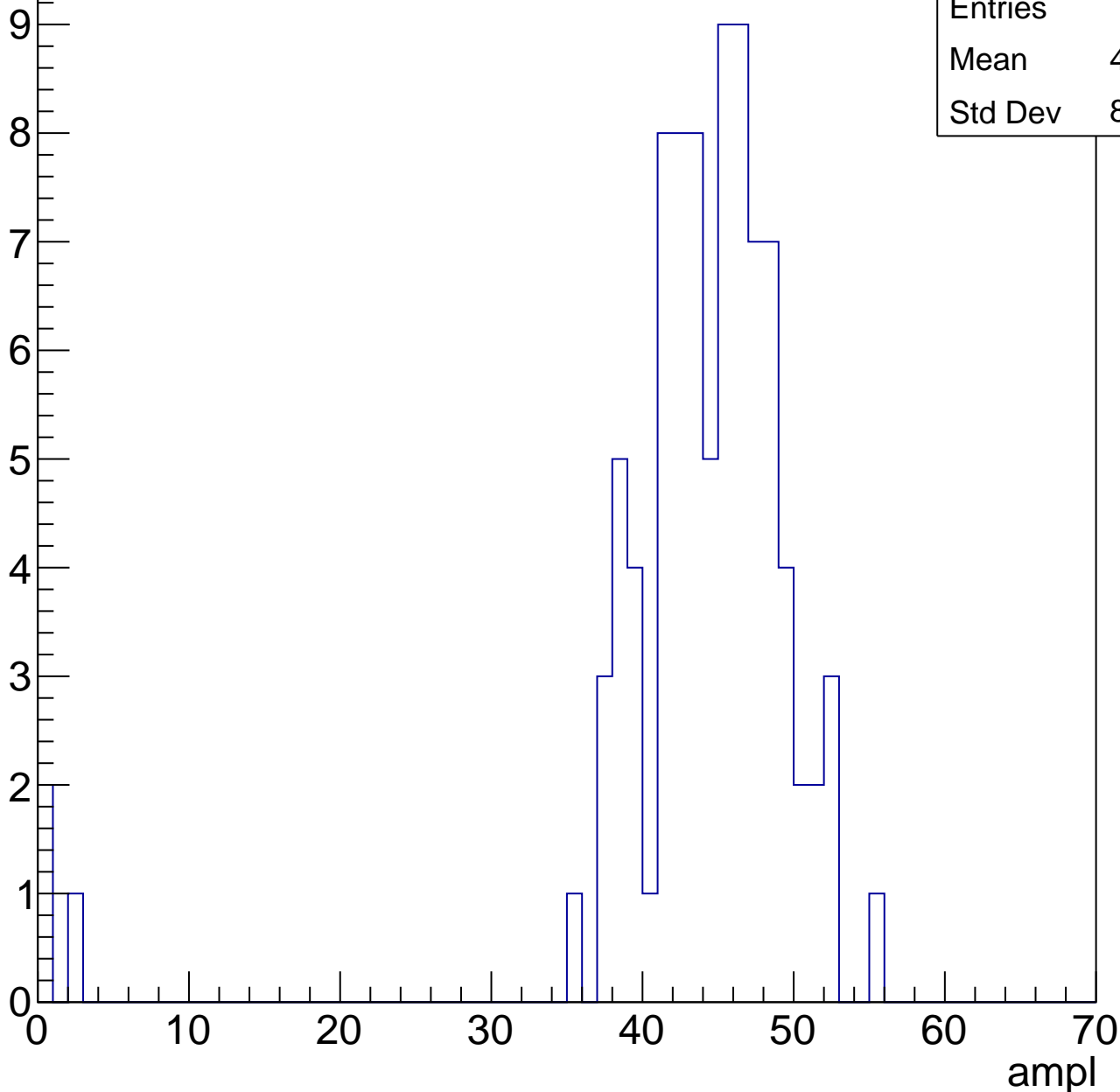


# B1L103S, U3-ch82, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	90
Mean	42.83
Std Dev	8.789

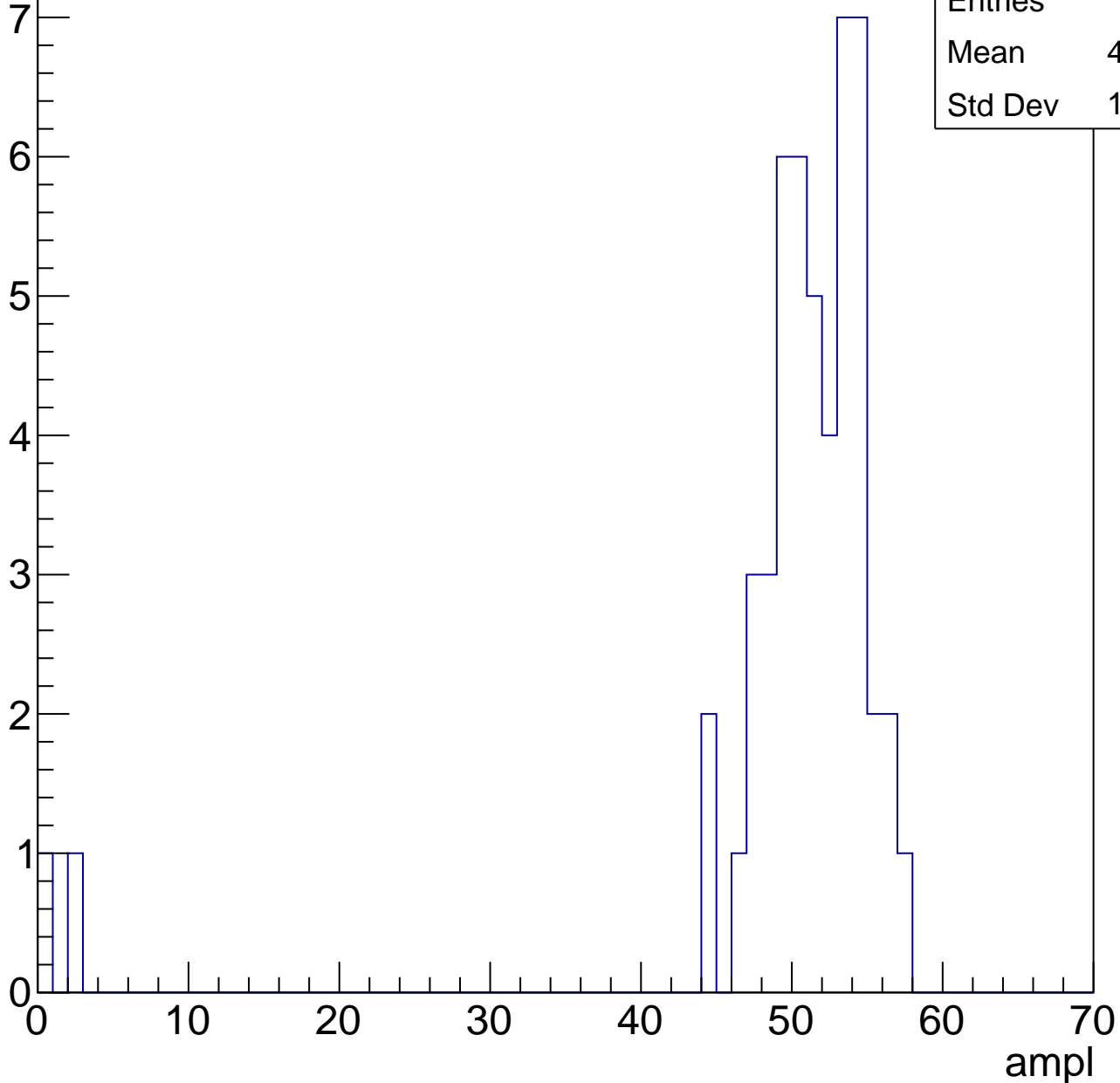


# B1L103S, U3-ch82, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	51
Mean	49.14
Std Dev	10.16

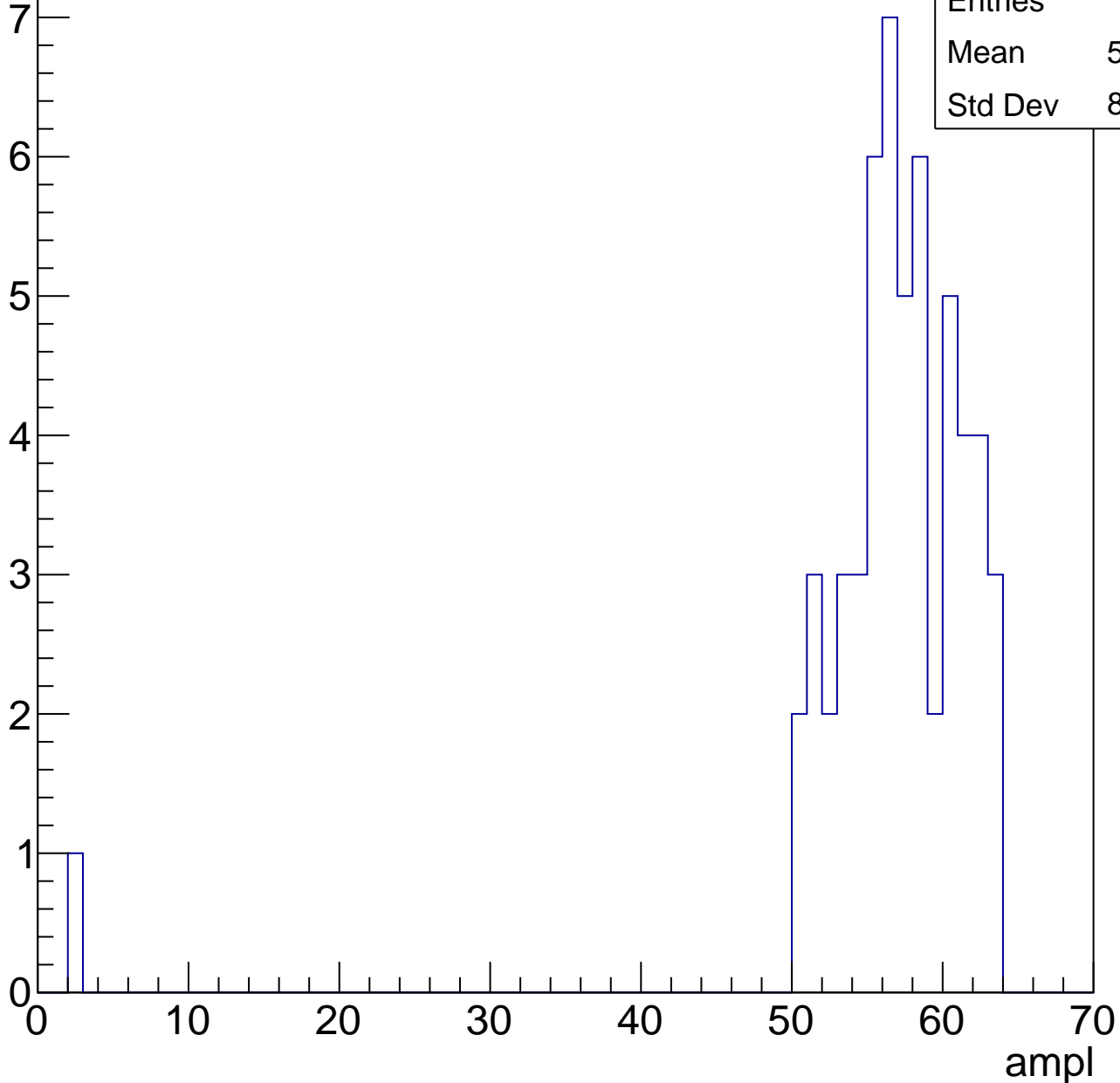


# B1L103S, U3-ch82, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

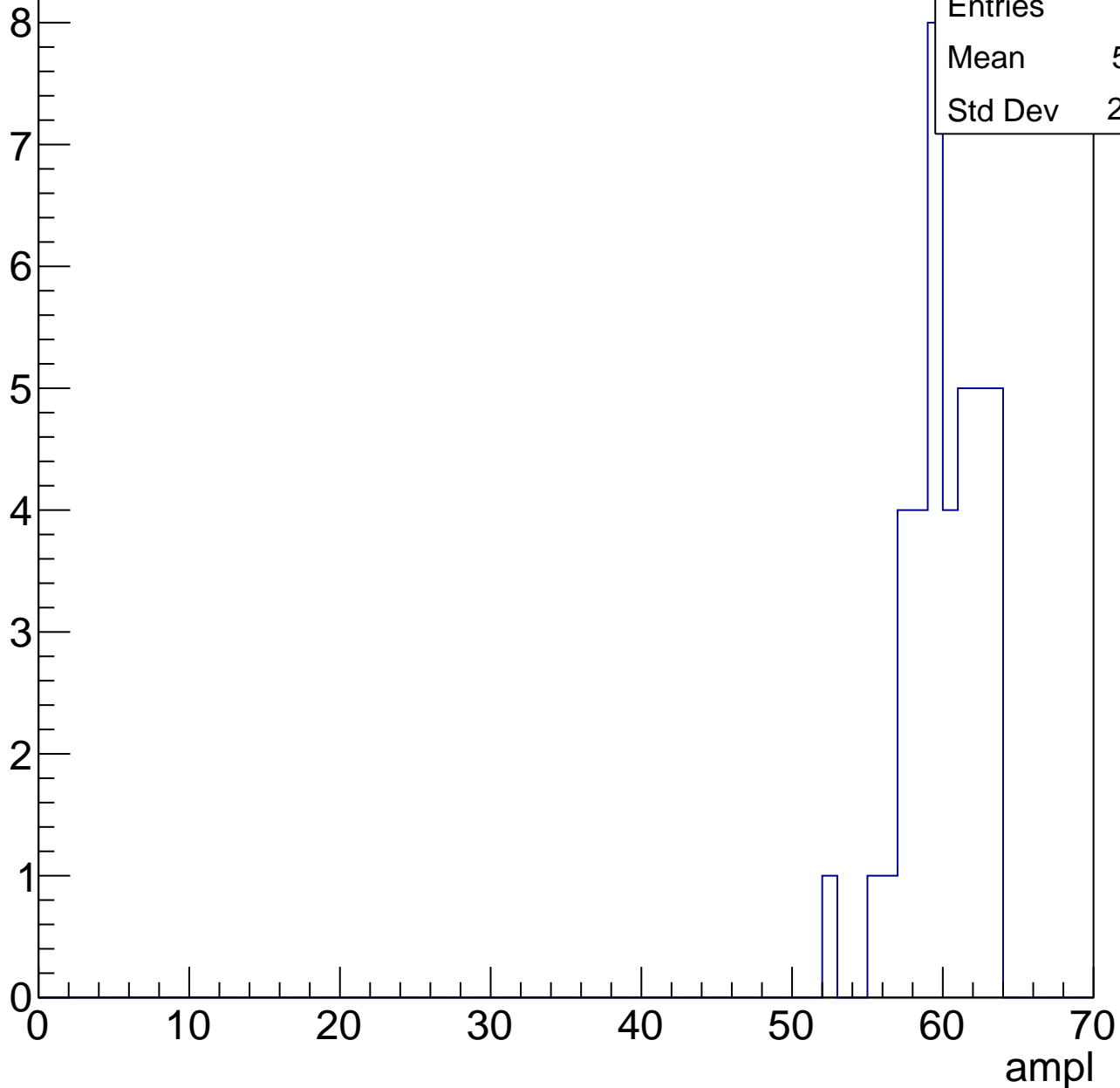
Entries	56
Mean	55.96
Std Dev	8.082



# B1L103S, U3-ch82, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

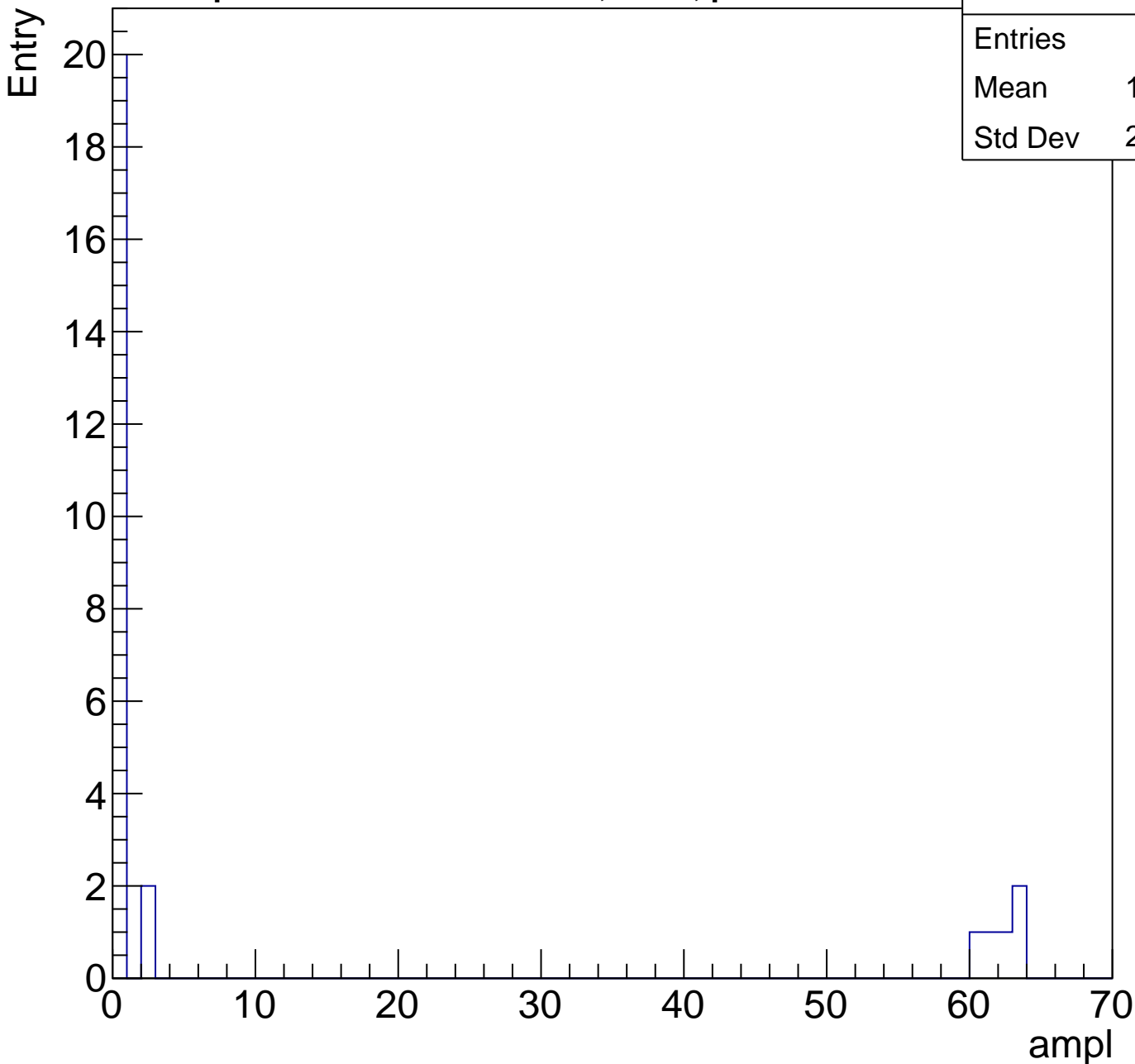




# B1L103S, U3-ch82, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	27
Mean	11.59
Std Dev	23.95



# B1L103S, U3-ch83, adc0

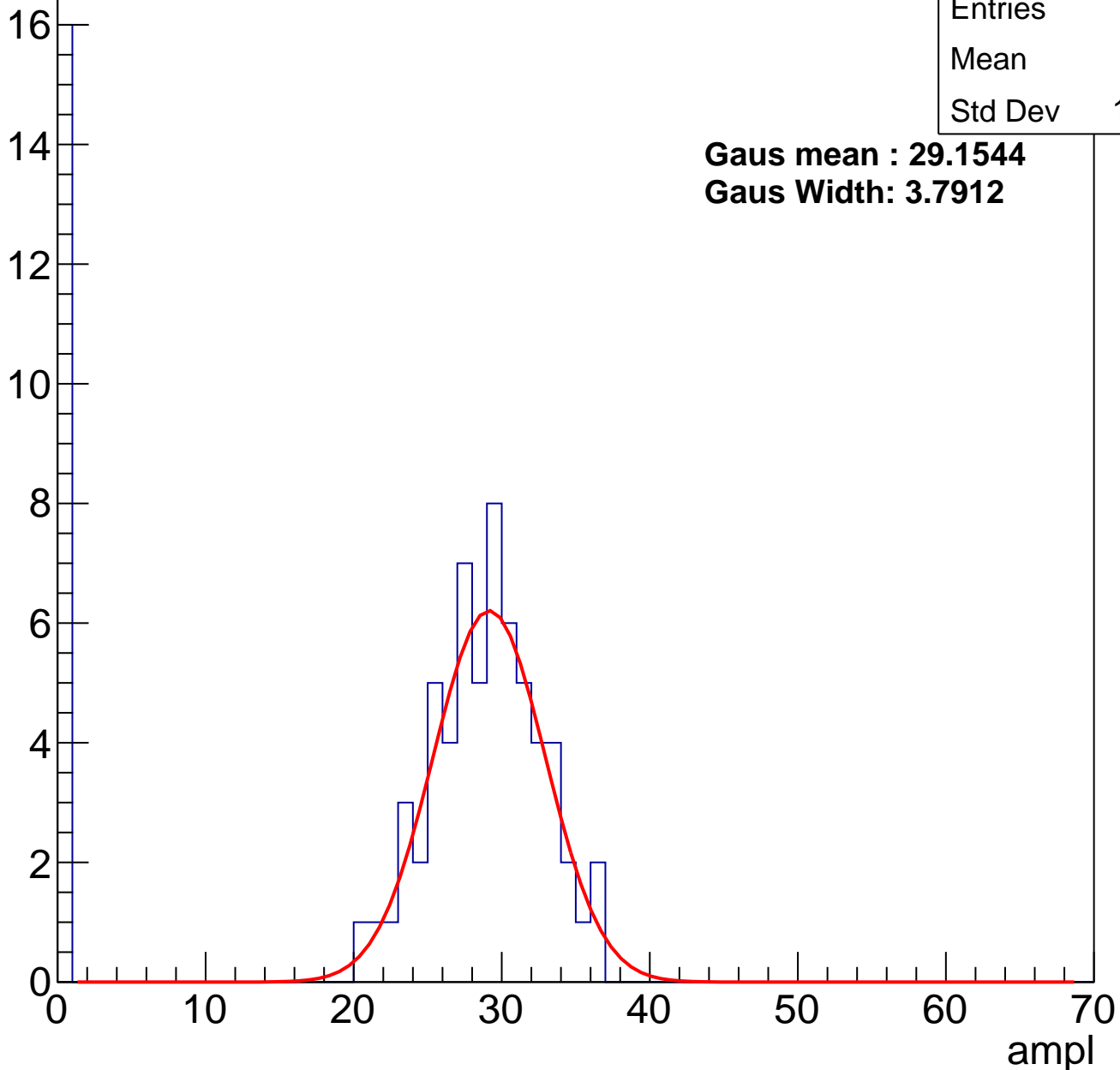
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	77
Mean	22.6
Std Dev	12.01

**Gaus mean : 29.1544**

**Gaus Width: 3.7912**

Entry



# B1L103S, U3-ch83, adc1

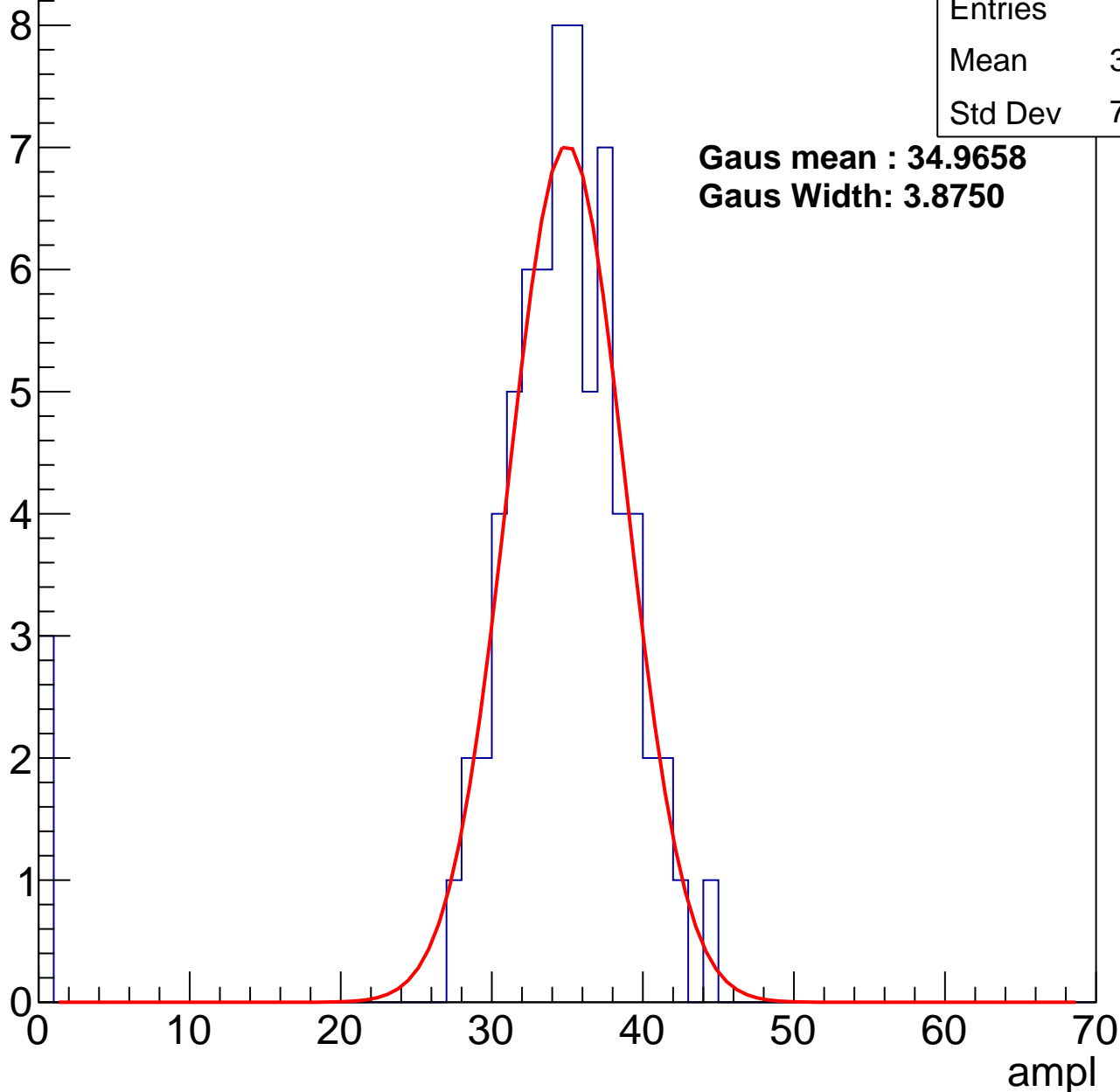
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	71
Mean	33.14
Std Dev	7.795

**Gaus mean : 34.9658**

**Gaus Width: 3.8750**



# B1L103S, U3-ch83, adc2

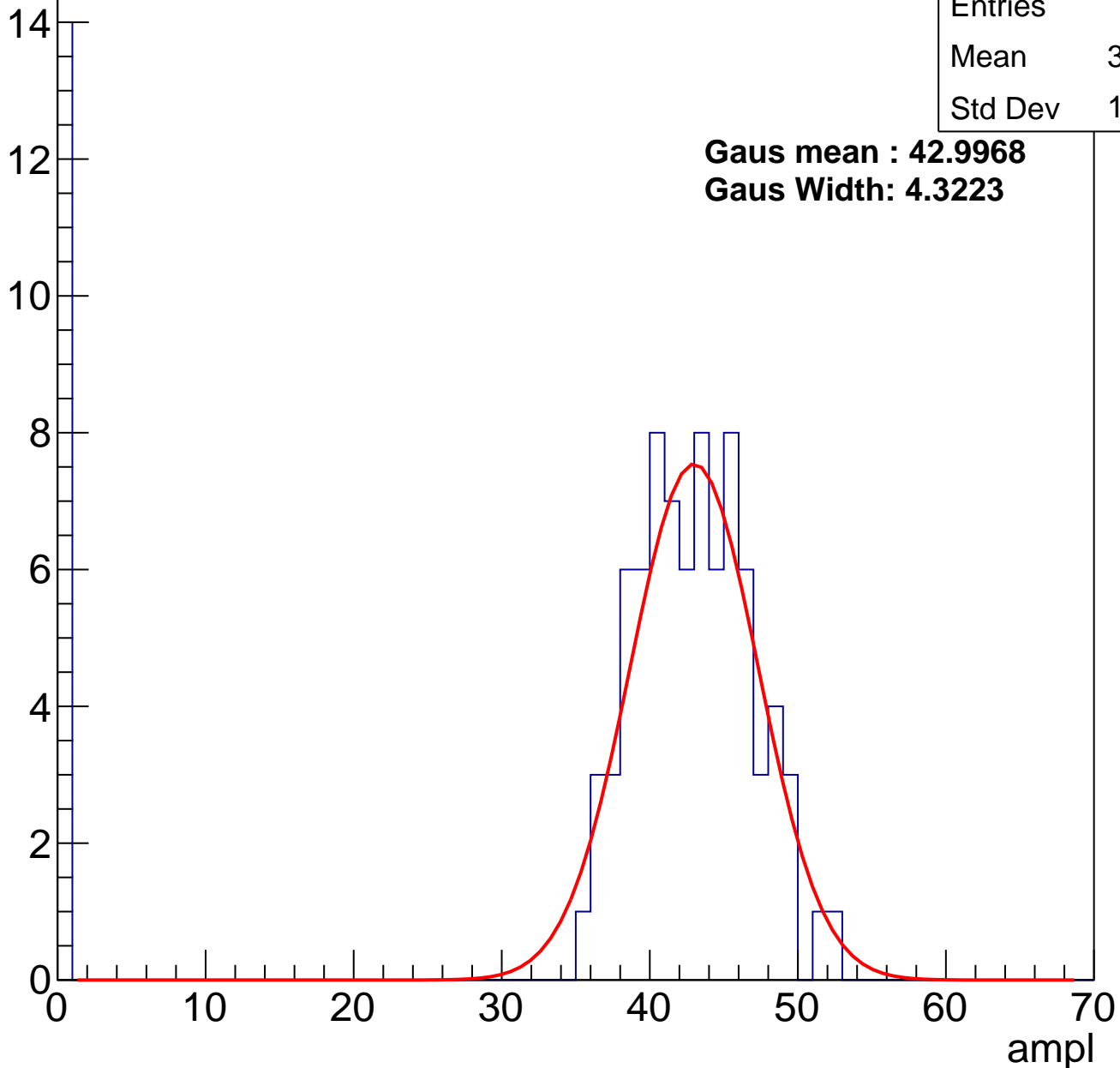
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	94
Mean	36.19
Std Dev	15.54

**Gaus mean : 42.9968**

**Gaus Width: 4.3223**

Entry

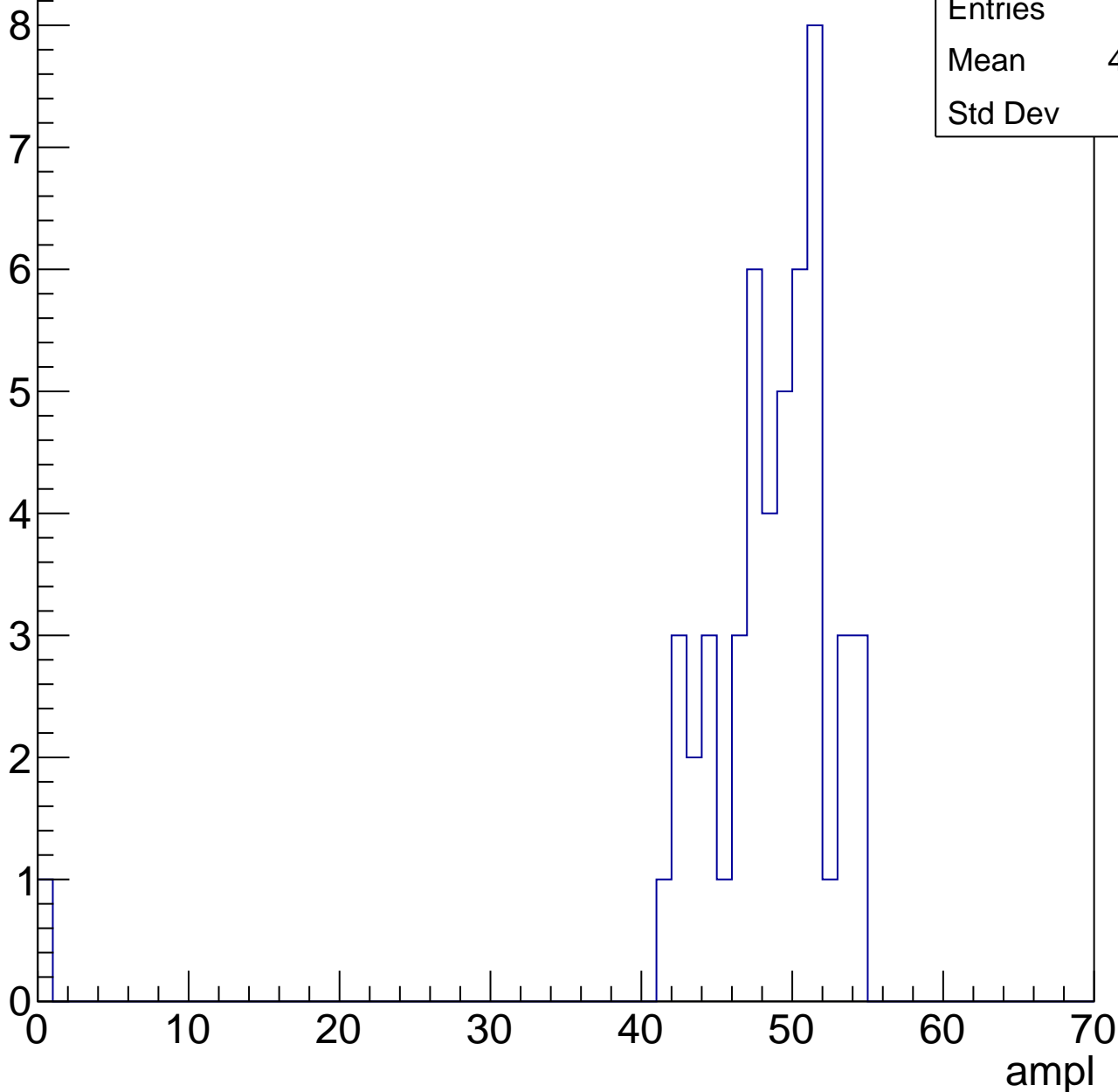


# B1L103S, U3-ch83, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	50
Mean	47.36
Std Dev	7.57

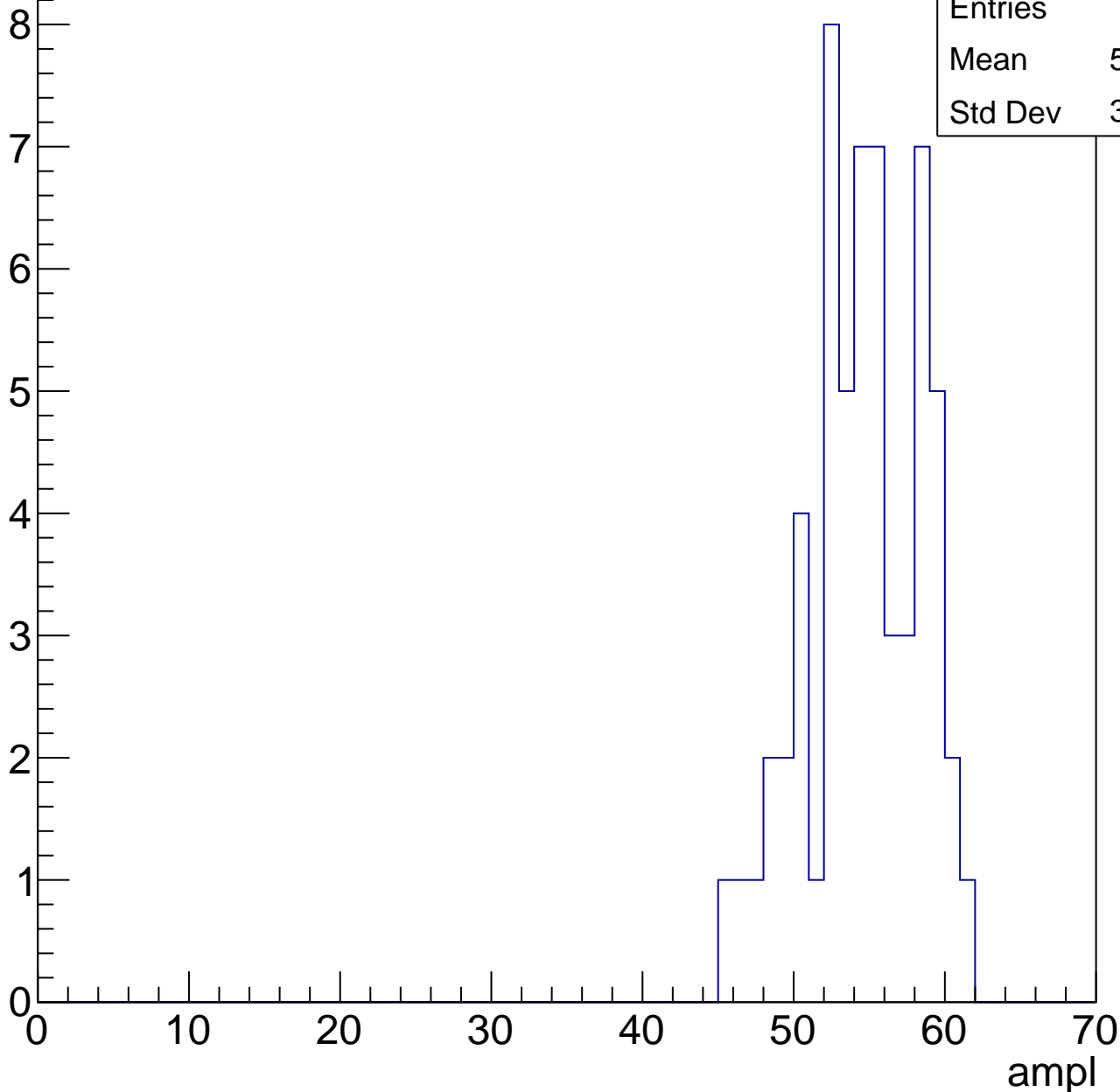


# B1L103S, U3-ch83, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

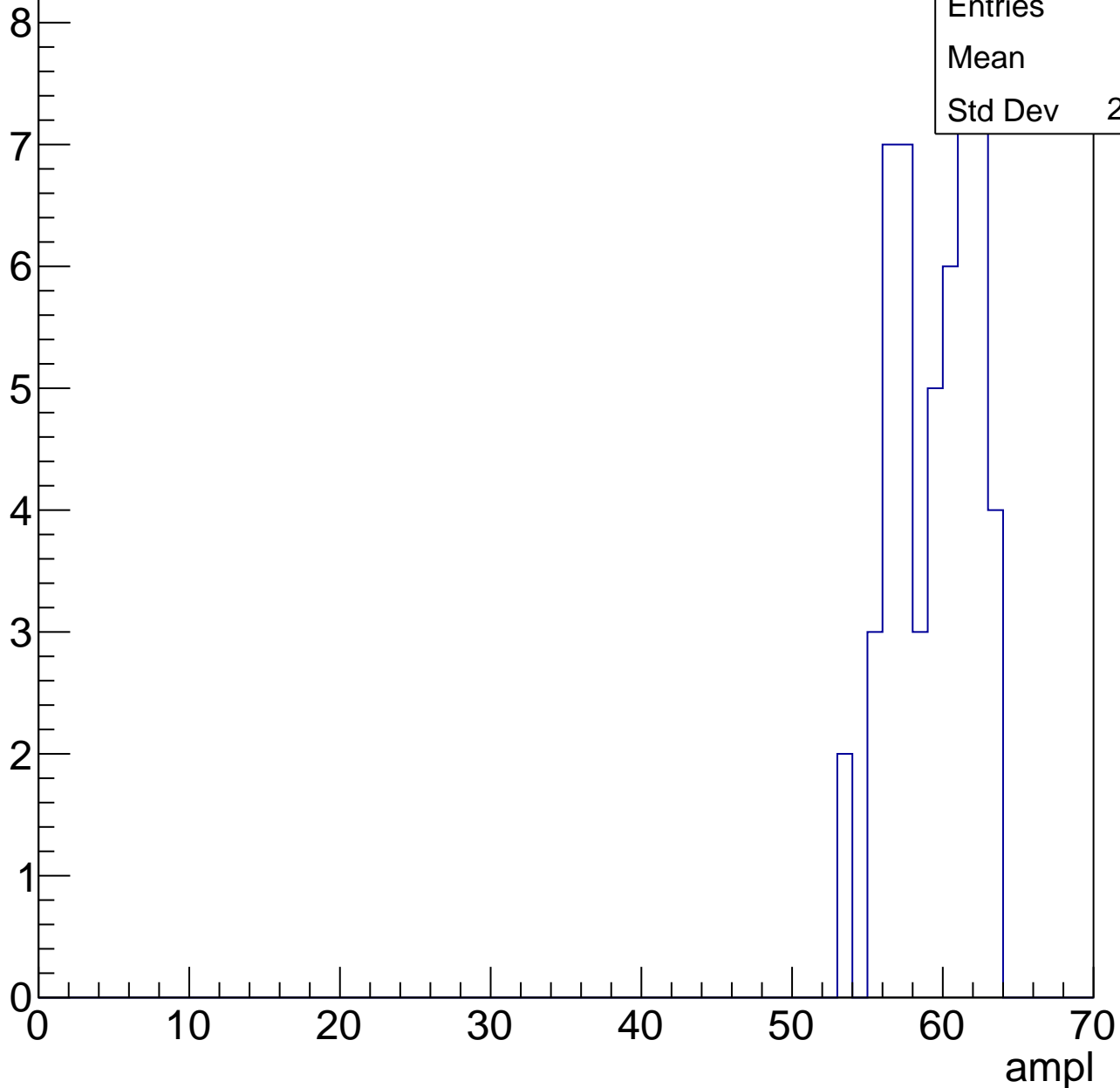
Entries	60
Mean	54.13
Std Dev	3.717



# B1L103S, U3-ch83, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

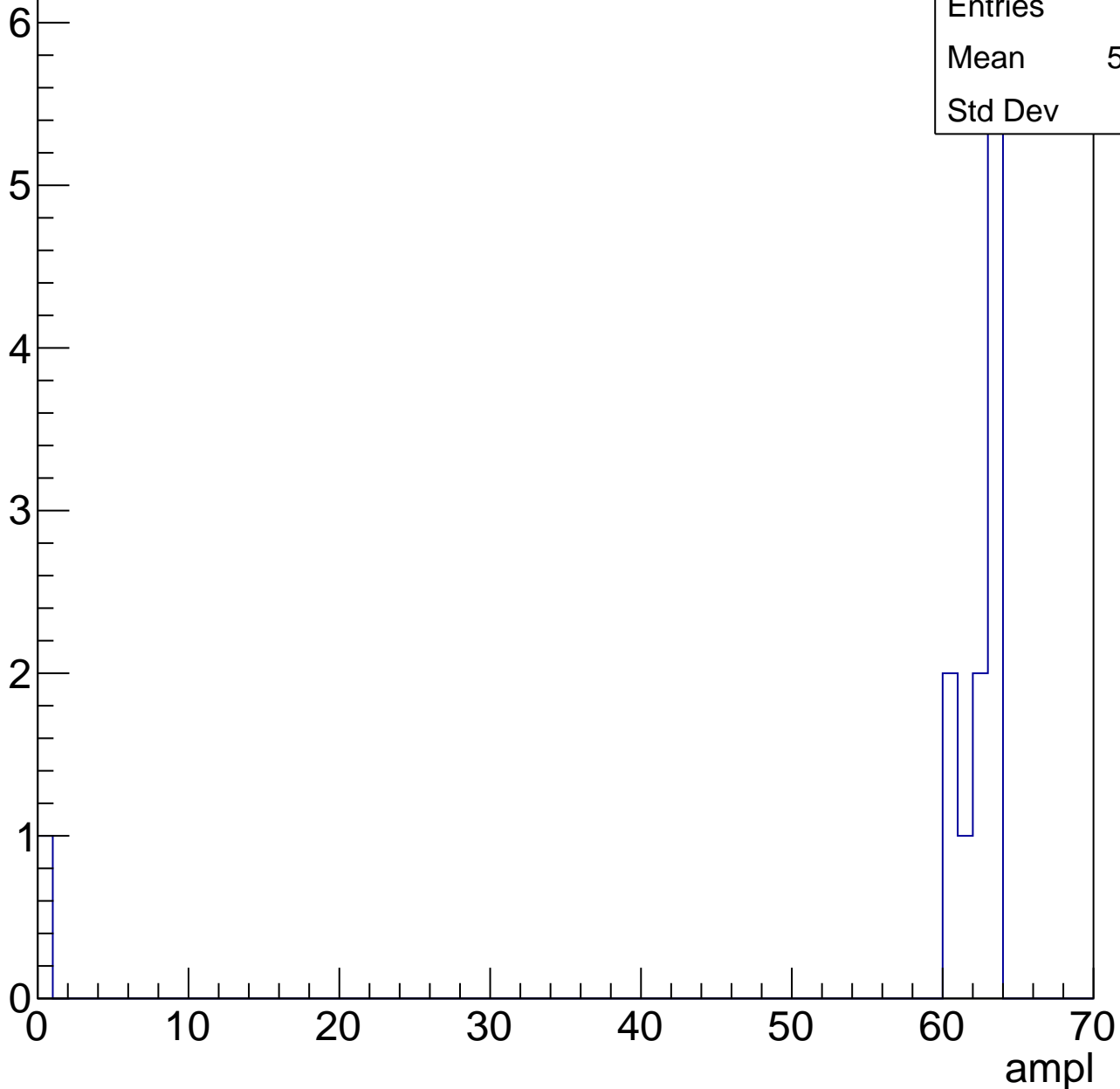


# B1L103S, U3-ch83, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	12
Mean	56.92
Std Dev	17.2





# B1L103S, U3-ch83, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

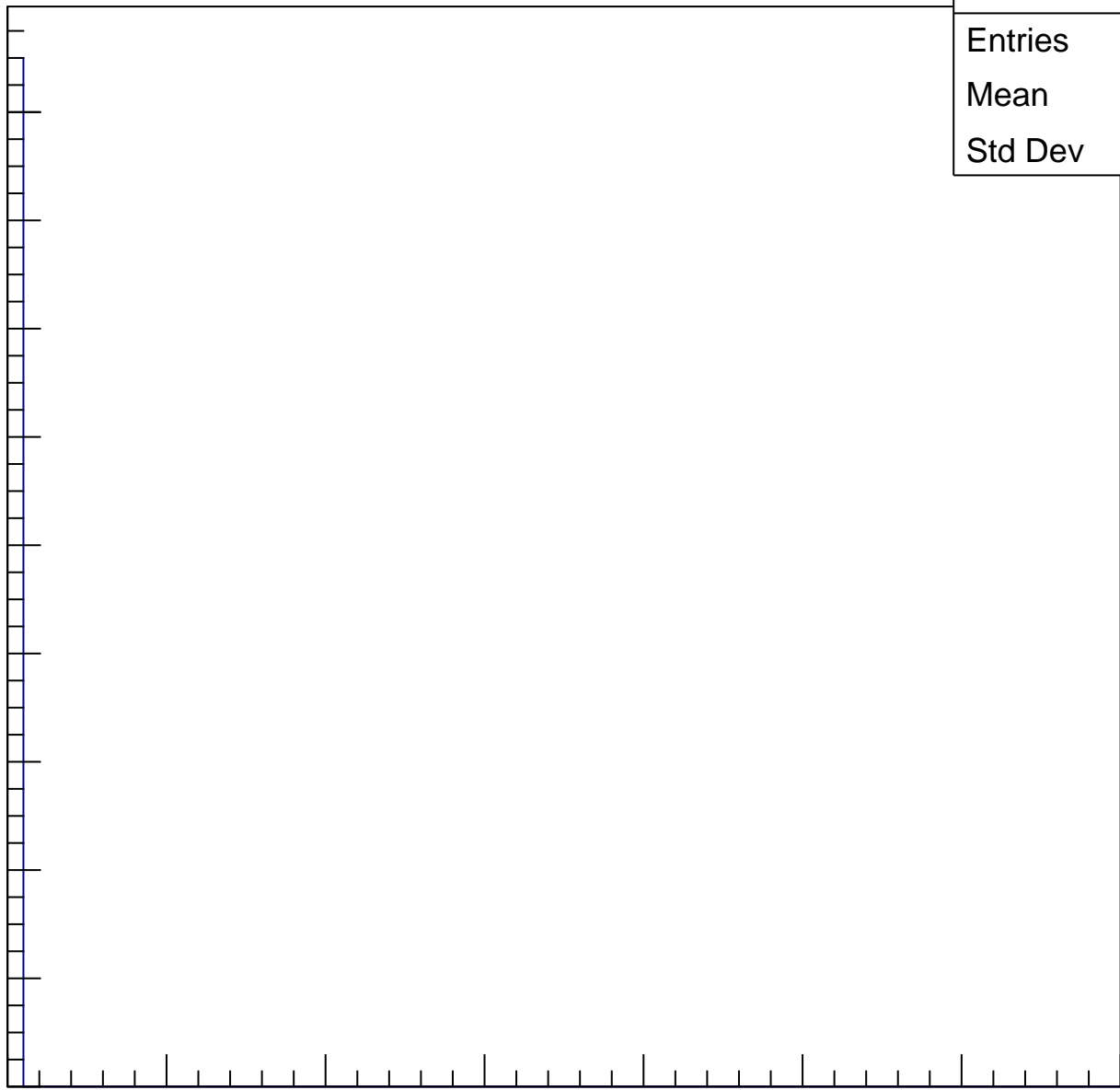
Entries	19
Mean	0
Std Dev	0

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



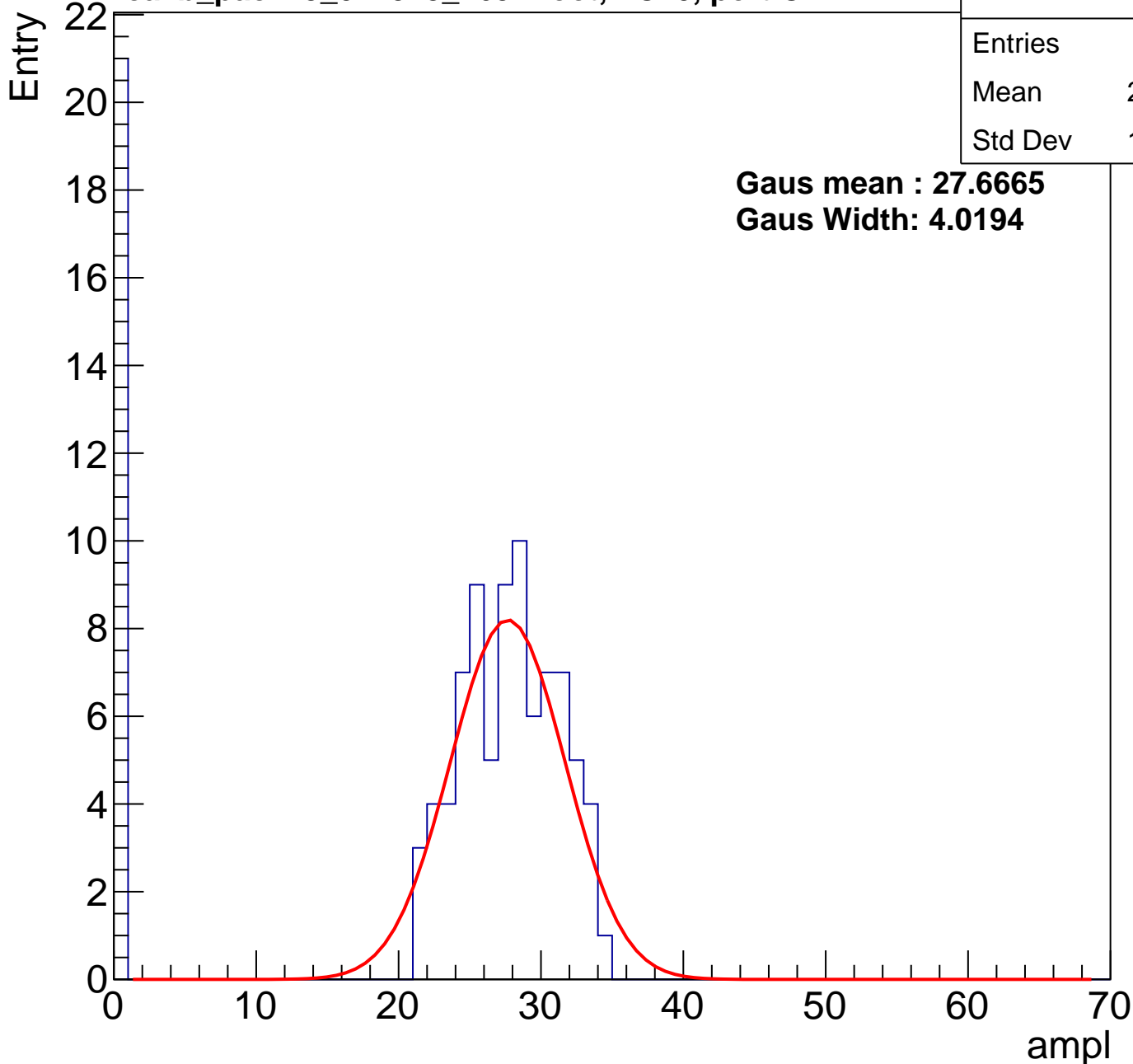
# B1L103S, U3-ch84, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	102
Mean	21.73
Std Dev	11.45

**Gaus mean : 27.6665**

**Gaus Width: 4.0194**



# B1L103S, U3-ch84, adc1

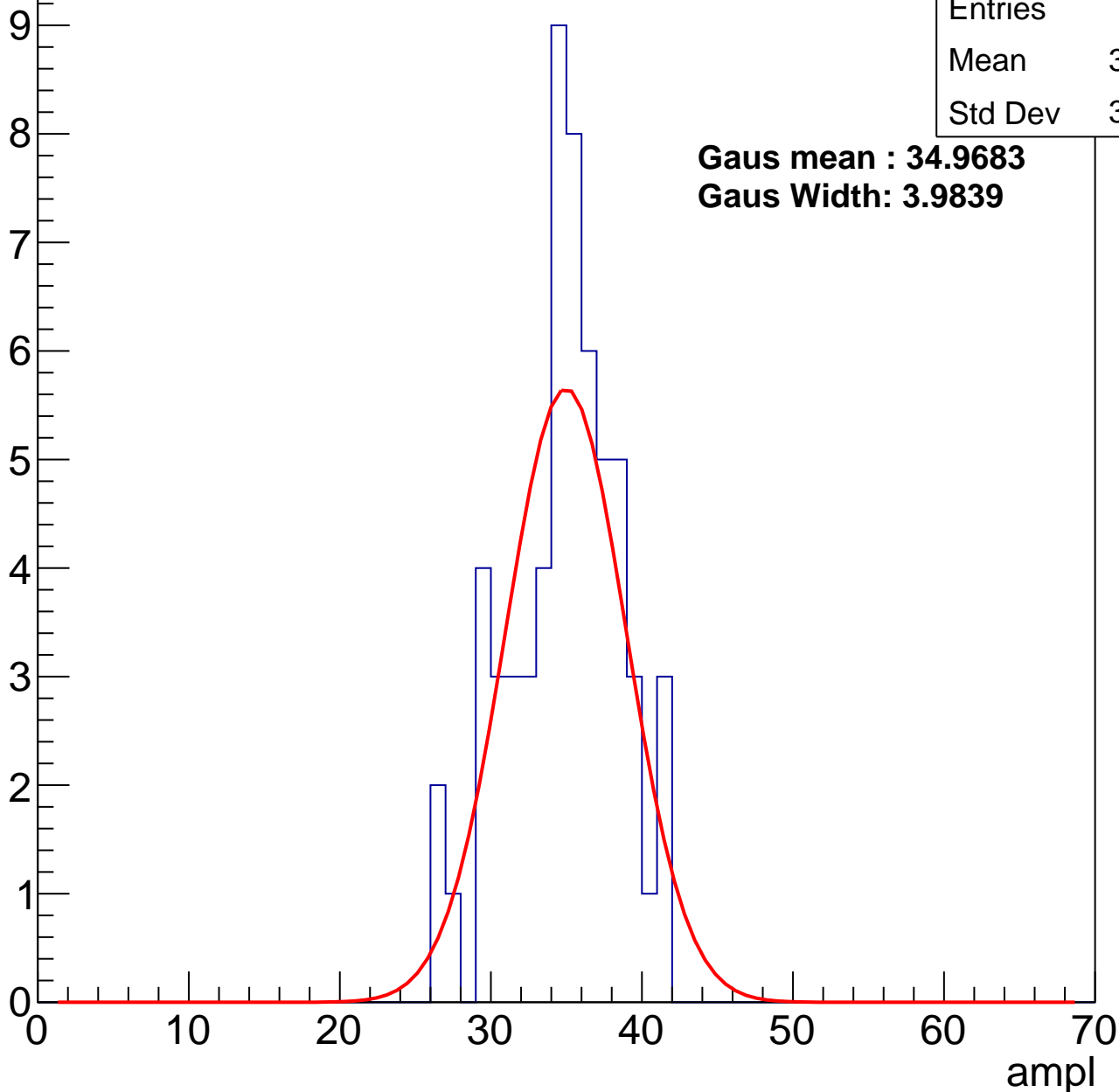
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	60
Mean	34.38
Std Dev	3.592

**Gaus mean : 34.9683**

**Gaus Width: 3.9839**



# B1L103S, U3-ch84, adc2

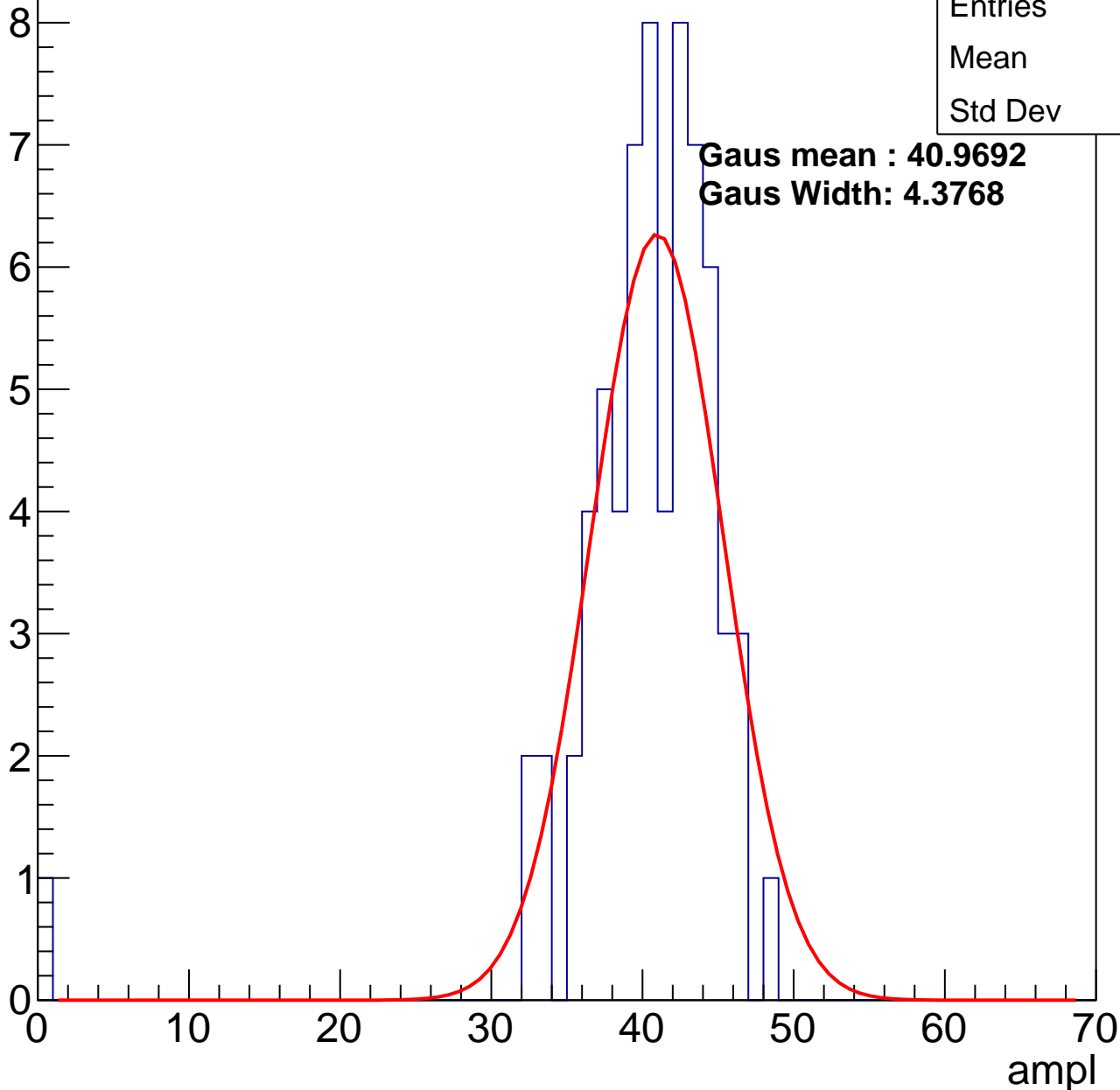
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	67
Mean	39.7
Std Dev	6.04

**Gaus mean : 40.9692**

**Gaus Width: 4.3768**



# B1L103S, U3-ch84, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	91
Mean	40.73
Std Dev	16.94

Entry

12

10

8

6

4

2

0

0

10

20

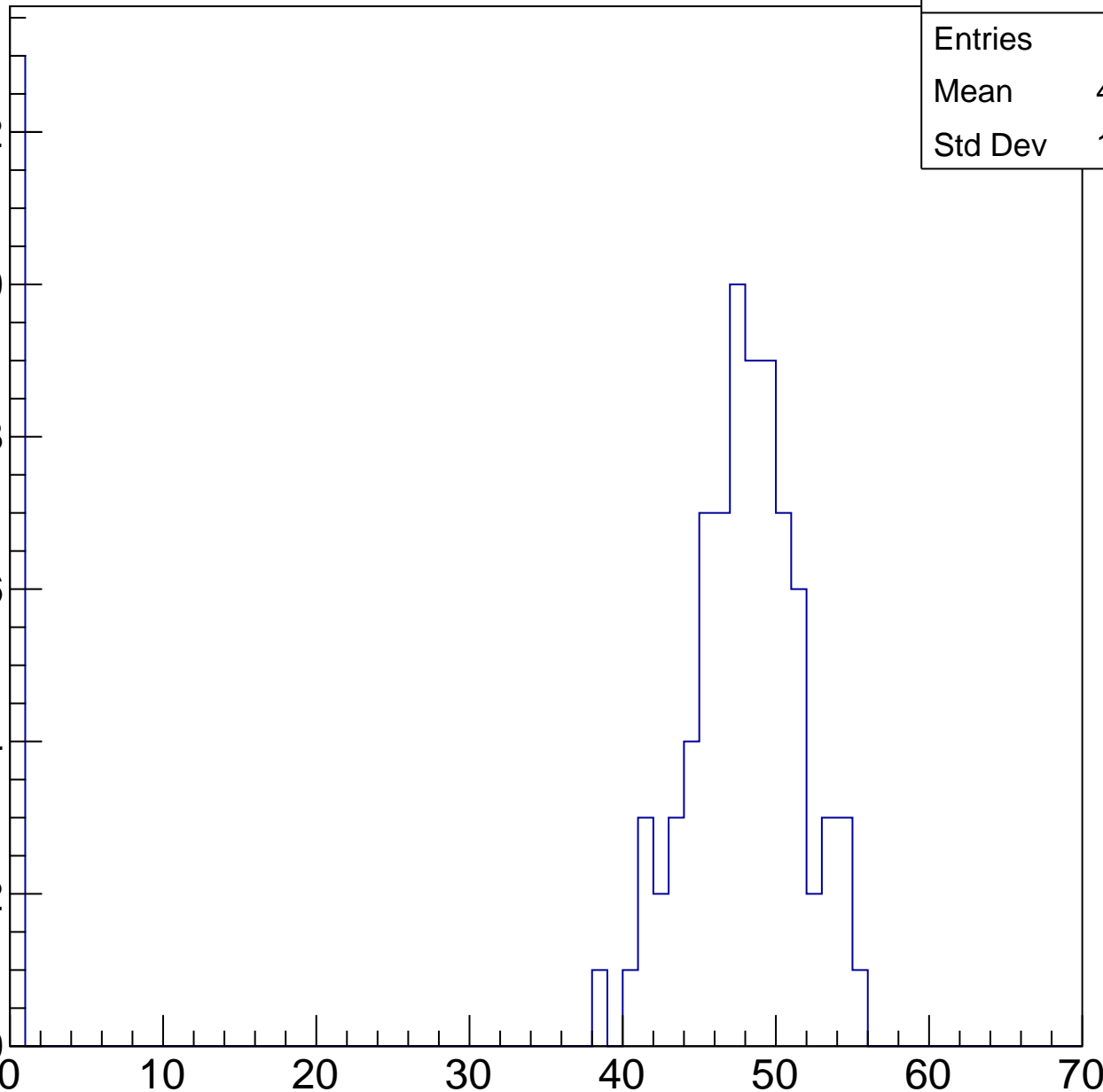
30

40

50

60

ampl

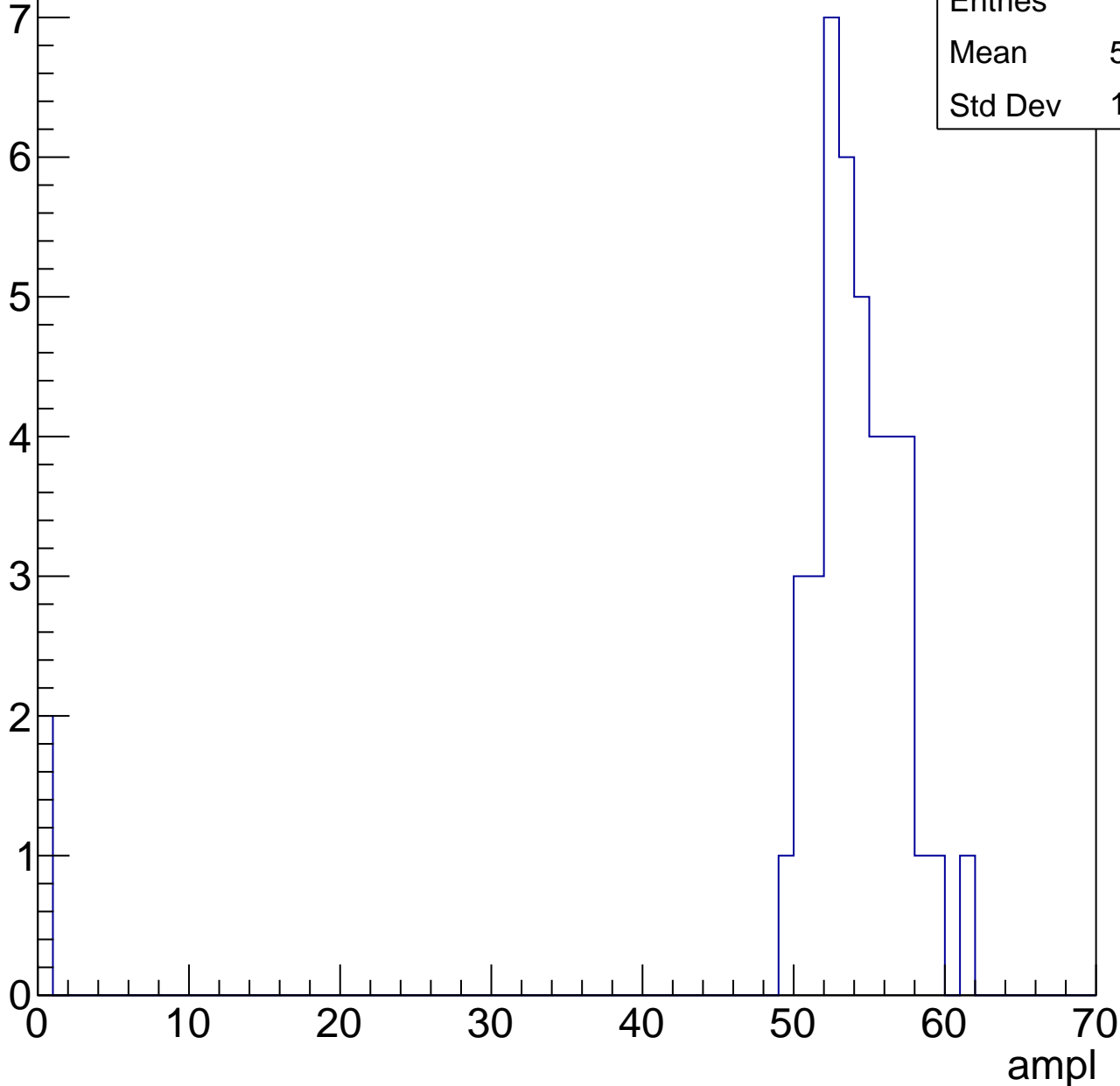


# B1L103S, U3-ch84, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	42
Mean	51.29
Std Dev	11.75

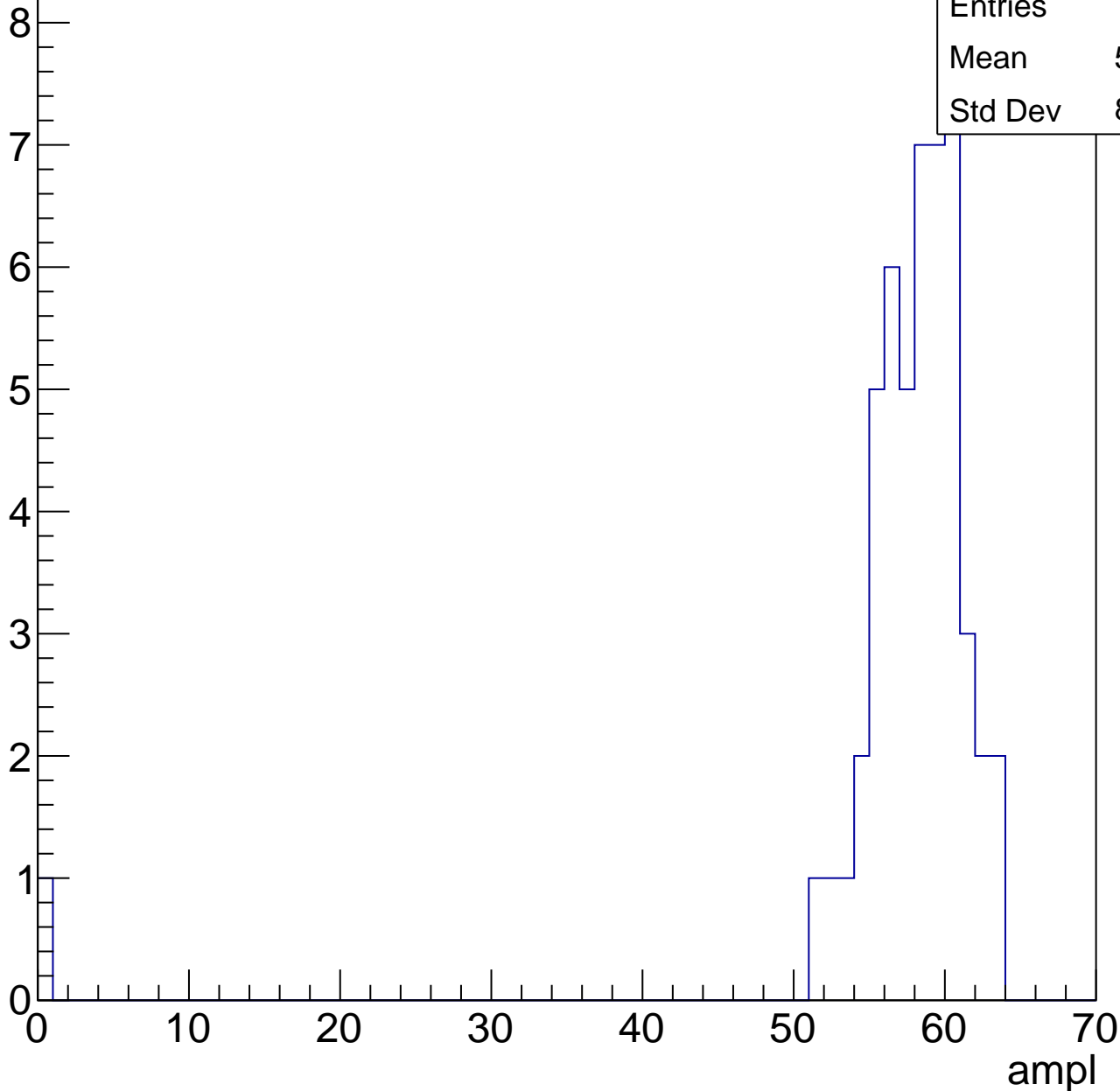


# B1L103S, U3-ch84, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	51
Mean	56.71
Std Dev	8.451

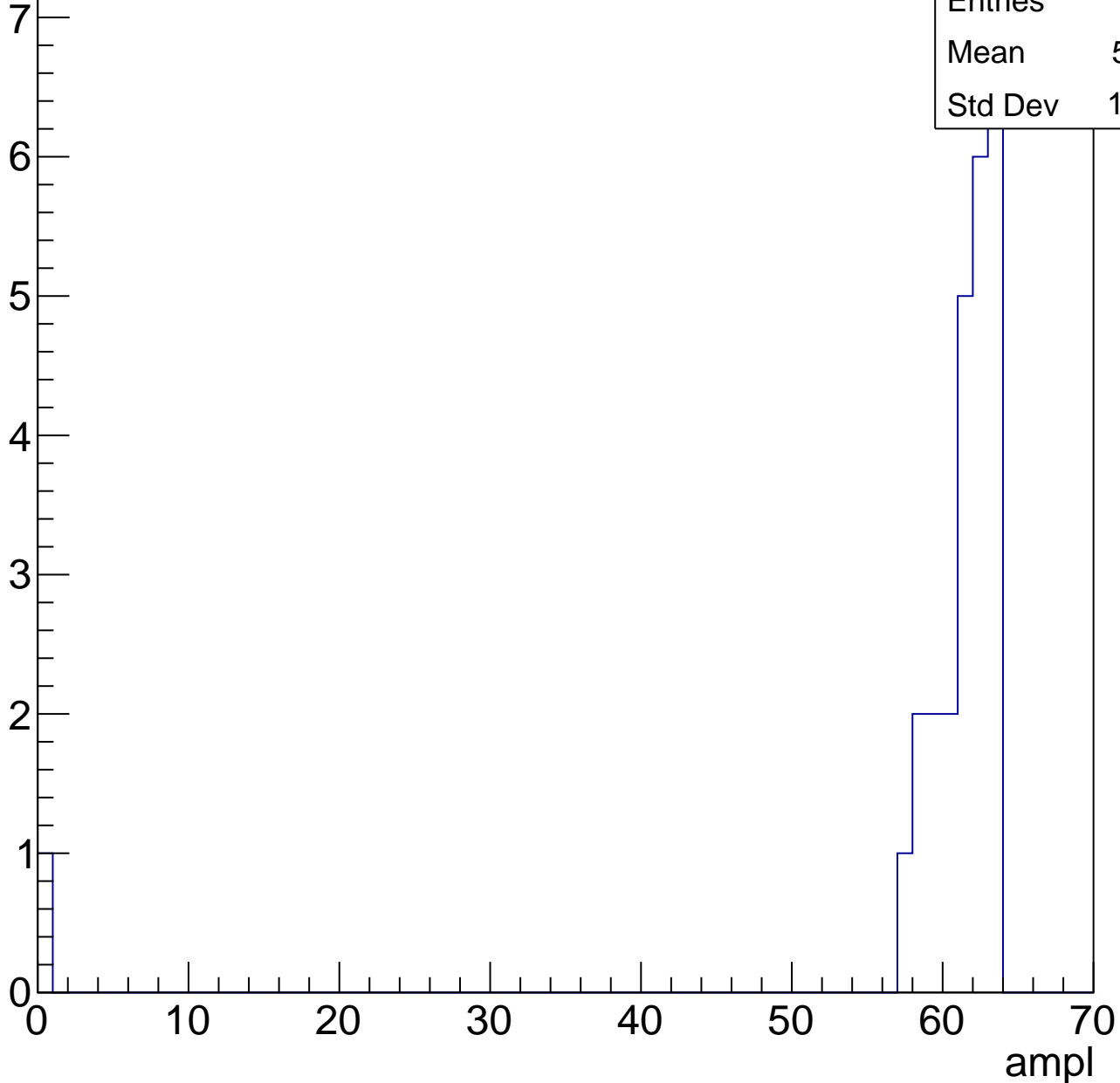


# B1L103S, U3-ch84, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	26
Mean	58.81
Std Dev	11.89



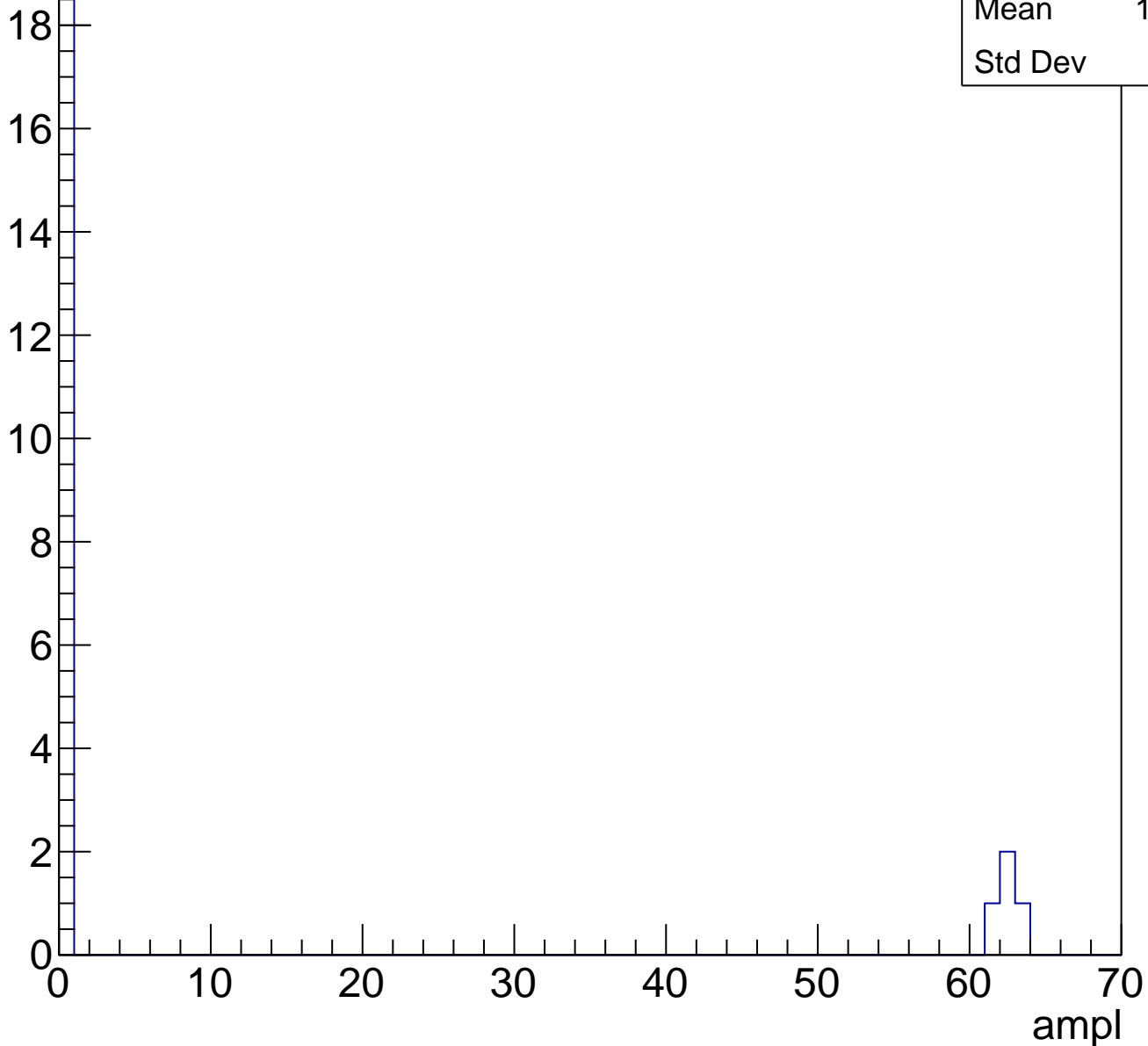


# B1L103S, U3-ch84, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	23
Mean	10.78
Std Dev	23.5

Entry



# B1L103S, U3-ch85, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	75
Mean	24.15
Std Dev	11.48

**Gaus mean : 29.6772**

**Gaus Width: 3.8414**

Entry

12

10

8

6

4

2

0

0

10

20

30

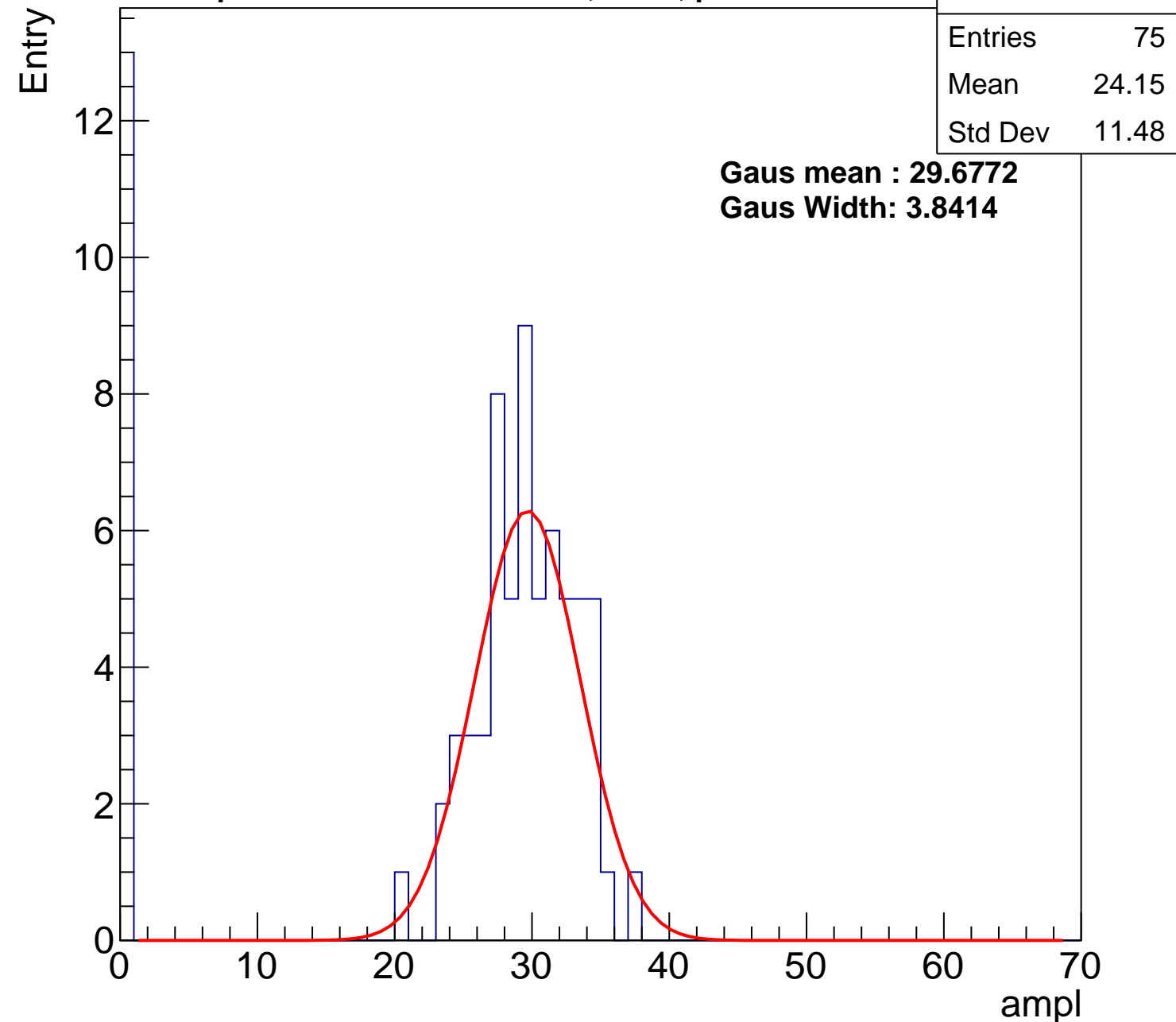
40

50

60

70

ampl



# B1L103S, U3-ch85, adc1

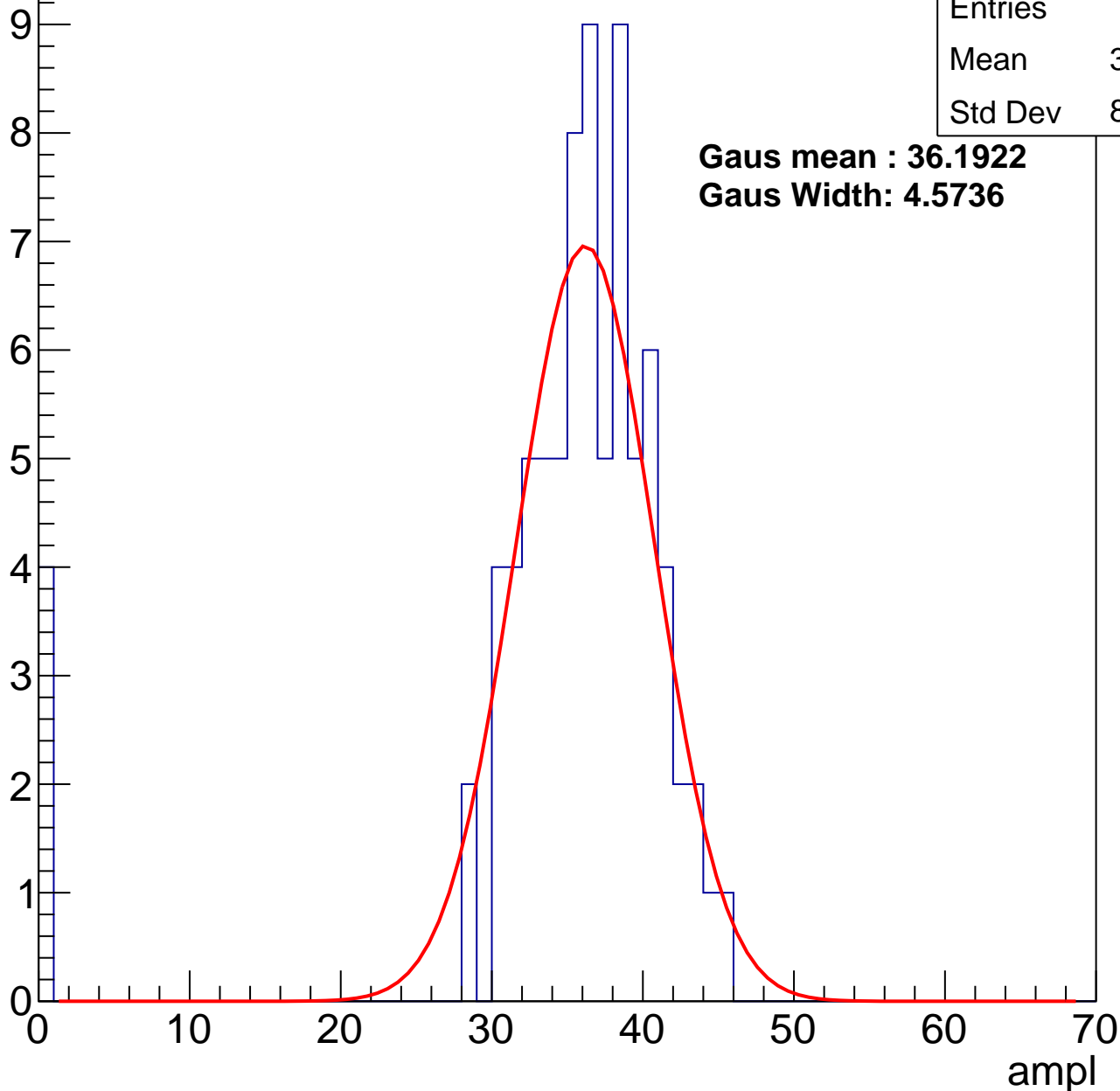
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	81
Mean	34.37
Std Dev	8.672

**Gaus mean : 36.1922**

**Gaus Width: 4.5736**



# B1L103S, U3-ch85, adc2

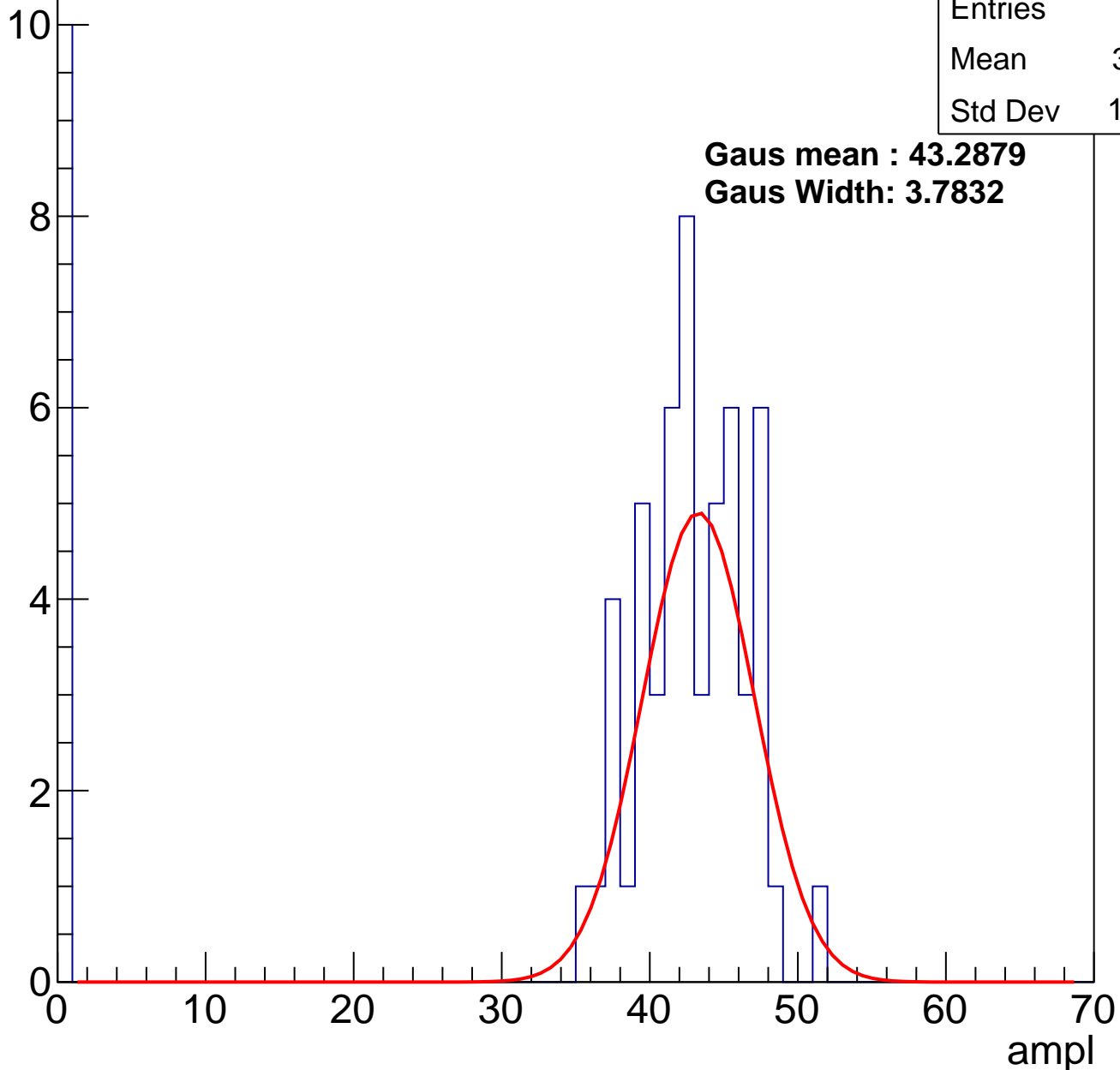
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	64
Mean	35.81
Std Dev	15.73

**Gaus mean : 43.2879**

**Gaus Width: 3.7832**

Entry

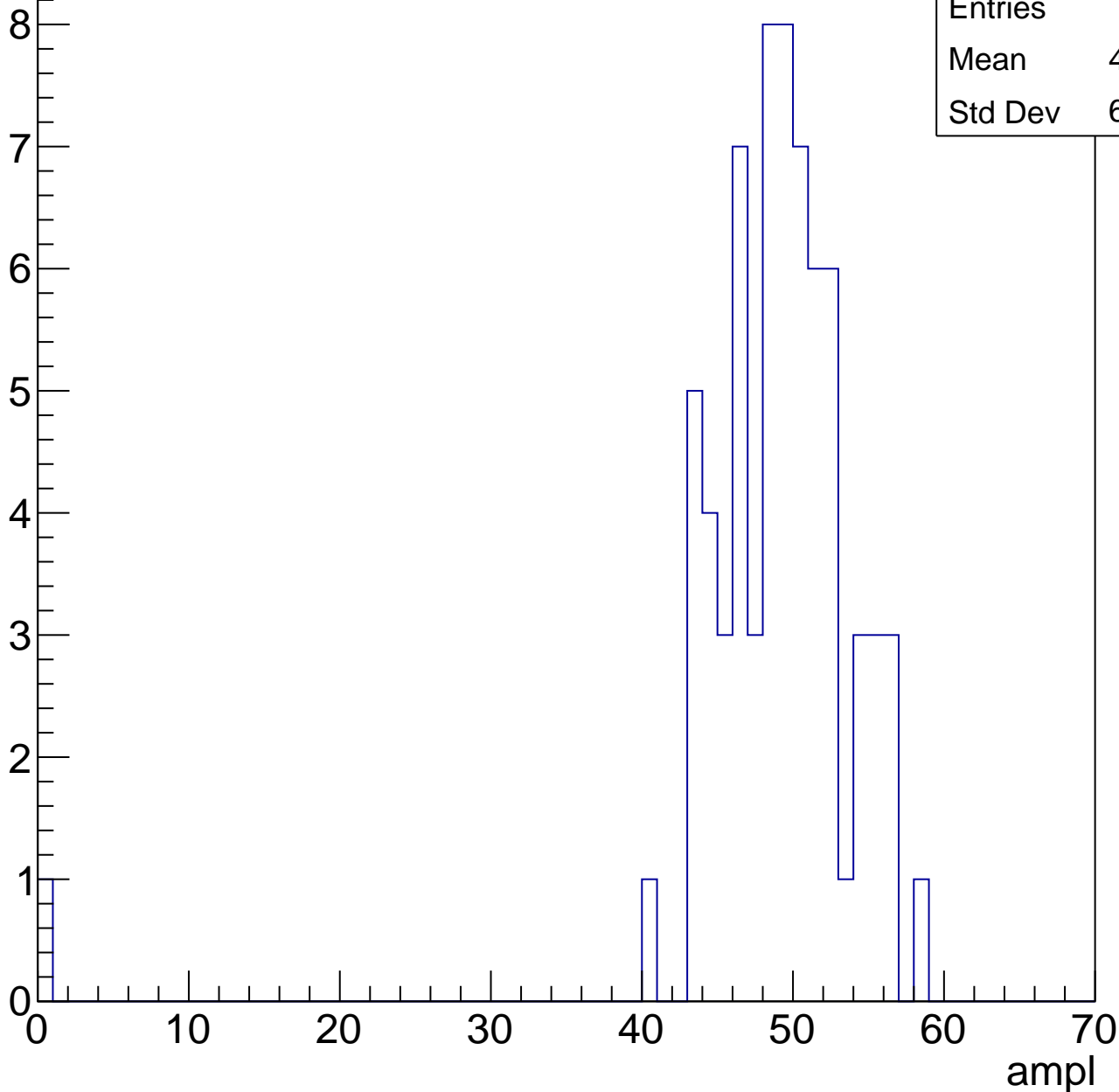


# B1L103S, U3-ch85, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	48.27
Std Dev	6.936

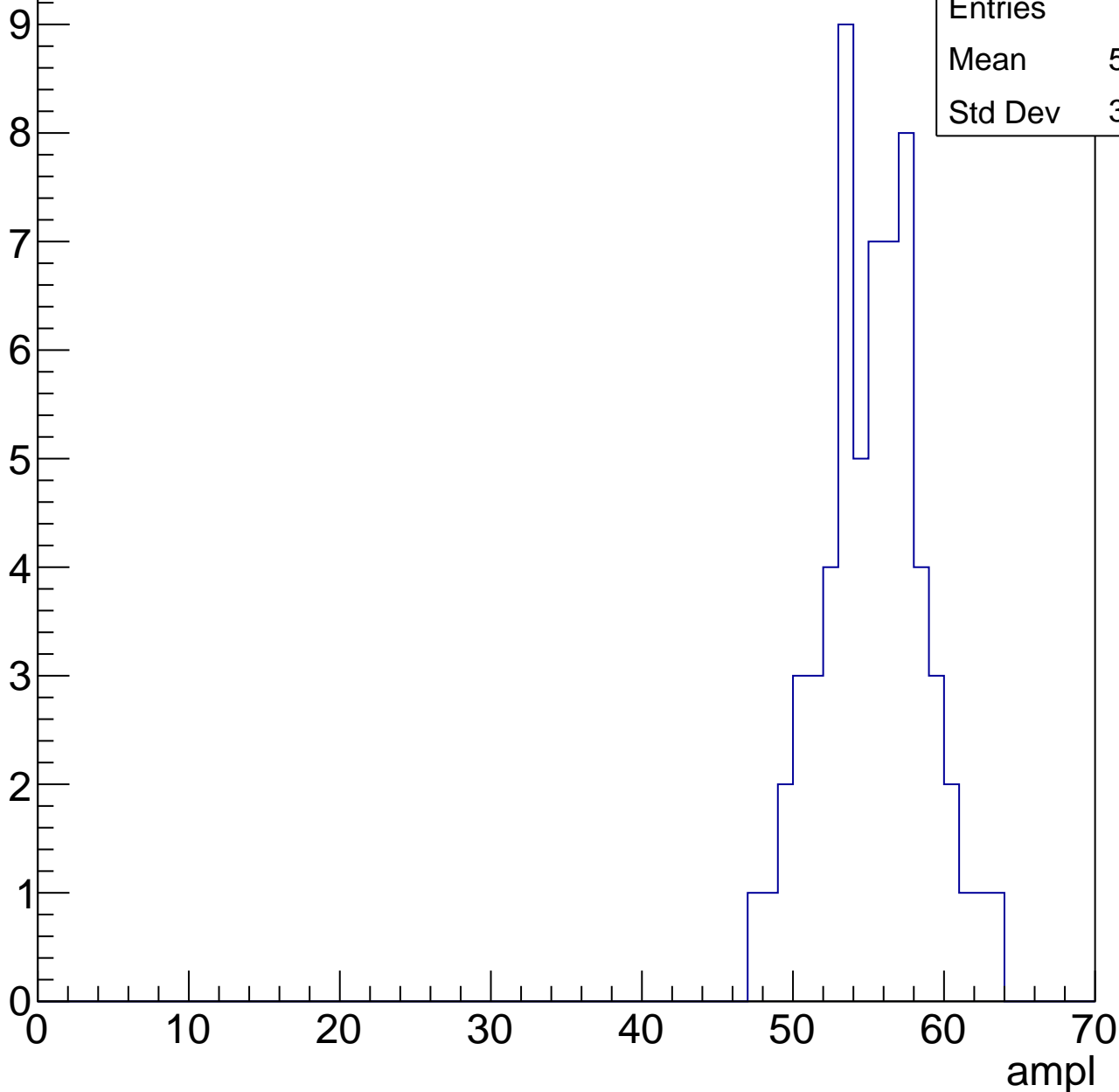


# B1L103S, U3-ch85, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	54.82
Std Dev	3.372

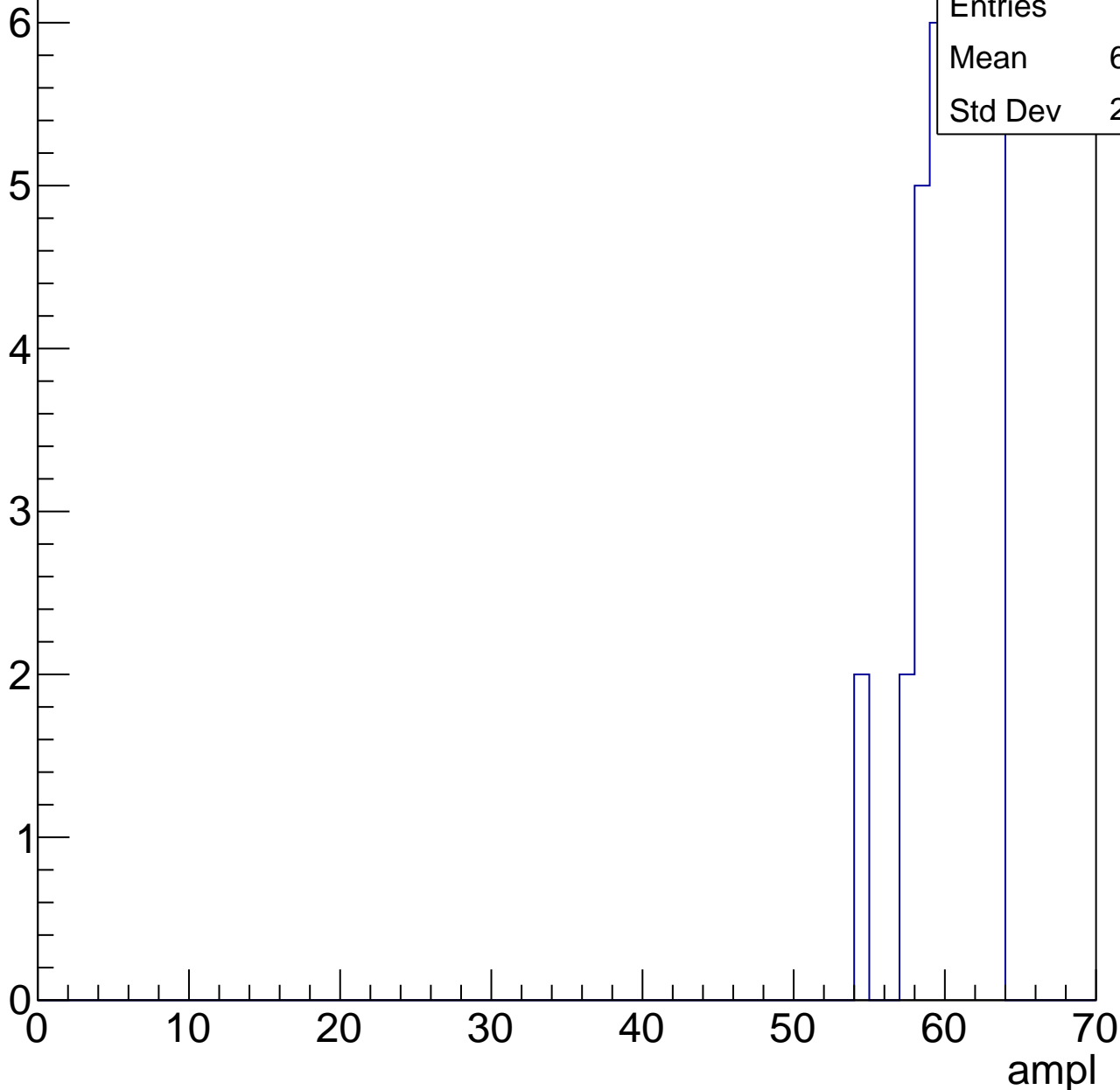


# B1L103S, U3-ch85, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

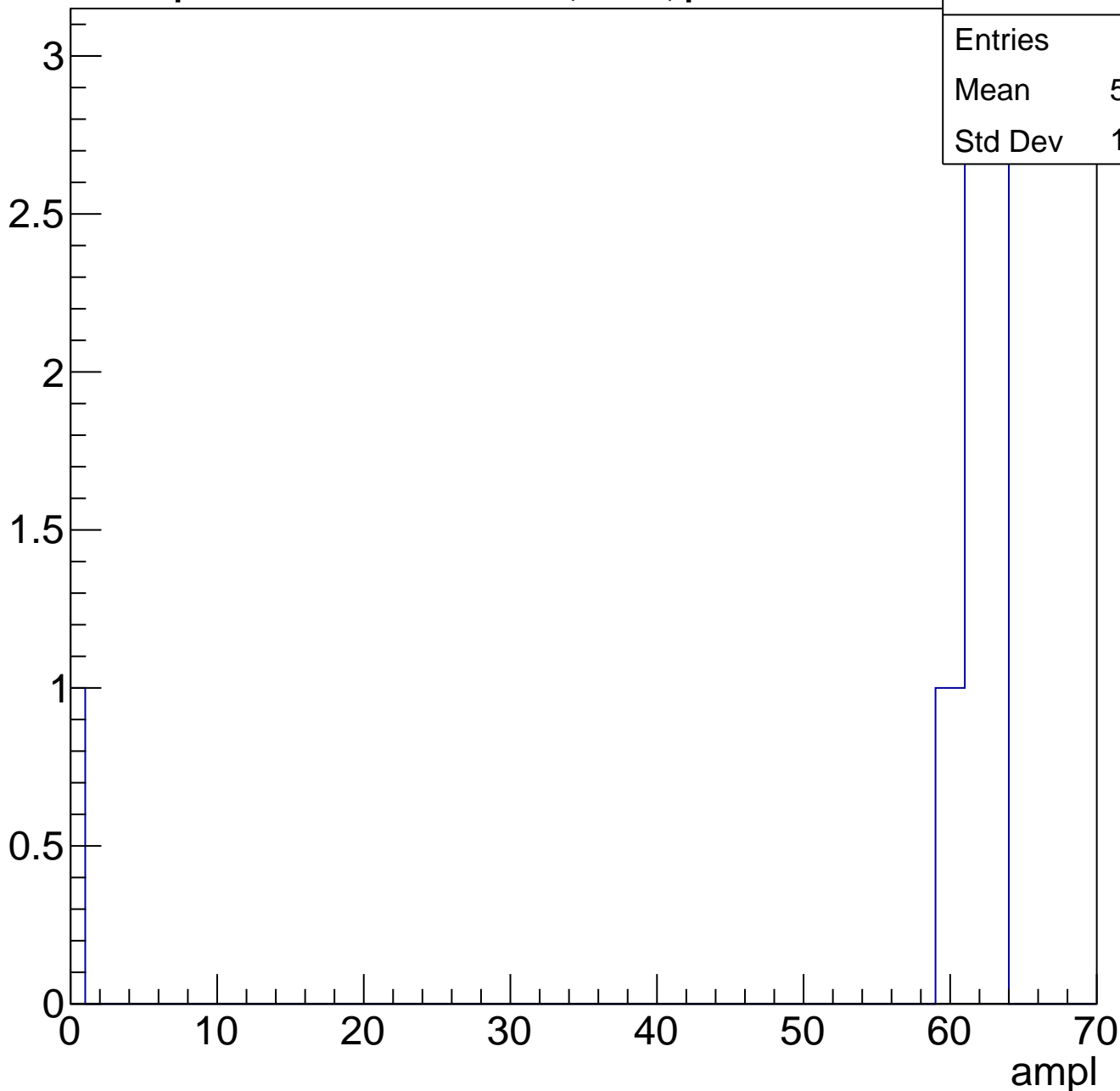
Entries	39
Mean	60.05
Std Dev	2.264



# B1L103S, U3-ch85, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



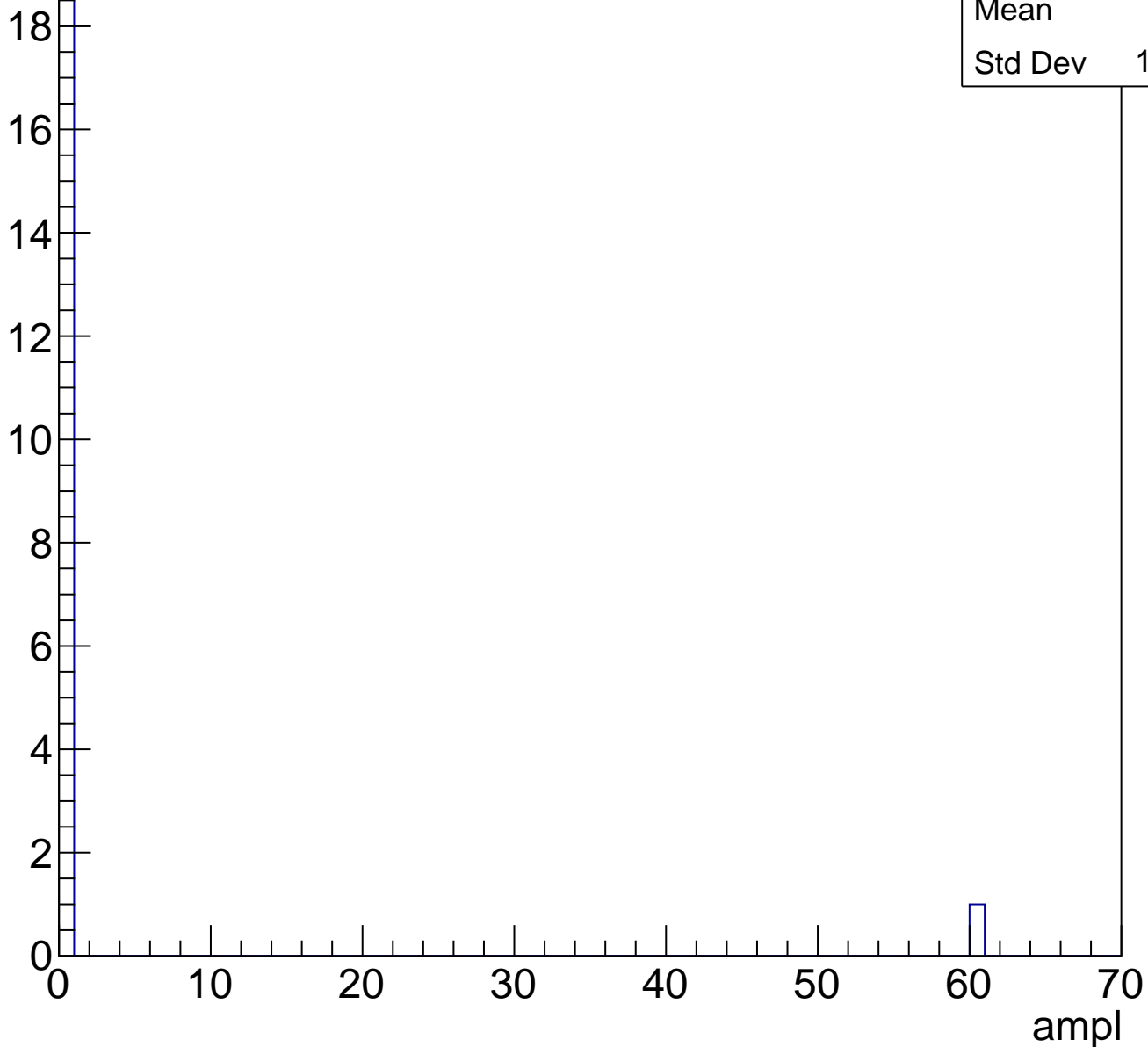


# B1L103S, U3-ch85, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3
Std Dev	13.08

Entry



# B1L103S, U3-ch86, adc0

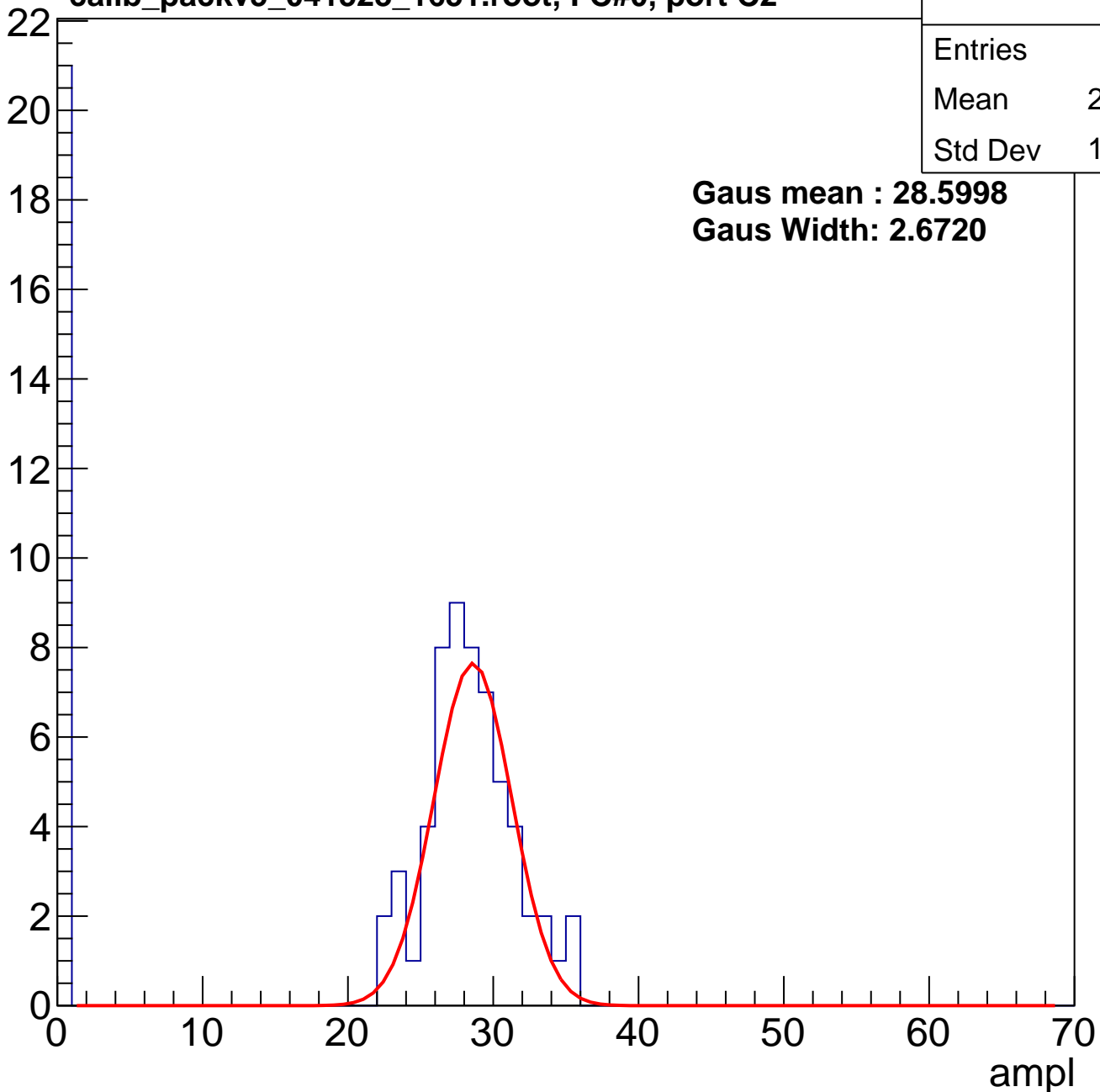
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	79
Mean	20.54
Std Dev	12.62

**Gaus mean : 28.5998**

**Gaus Width: 2.6720**

Entry



# B1L103S, U3-ch86, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	84
Mean	31.61
Std Dev	10.78

**Gaus mean : 34.6941**

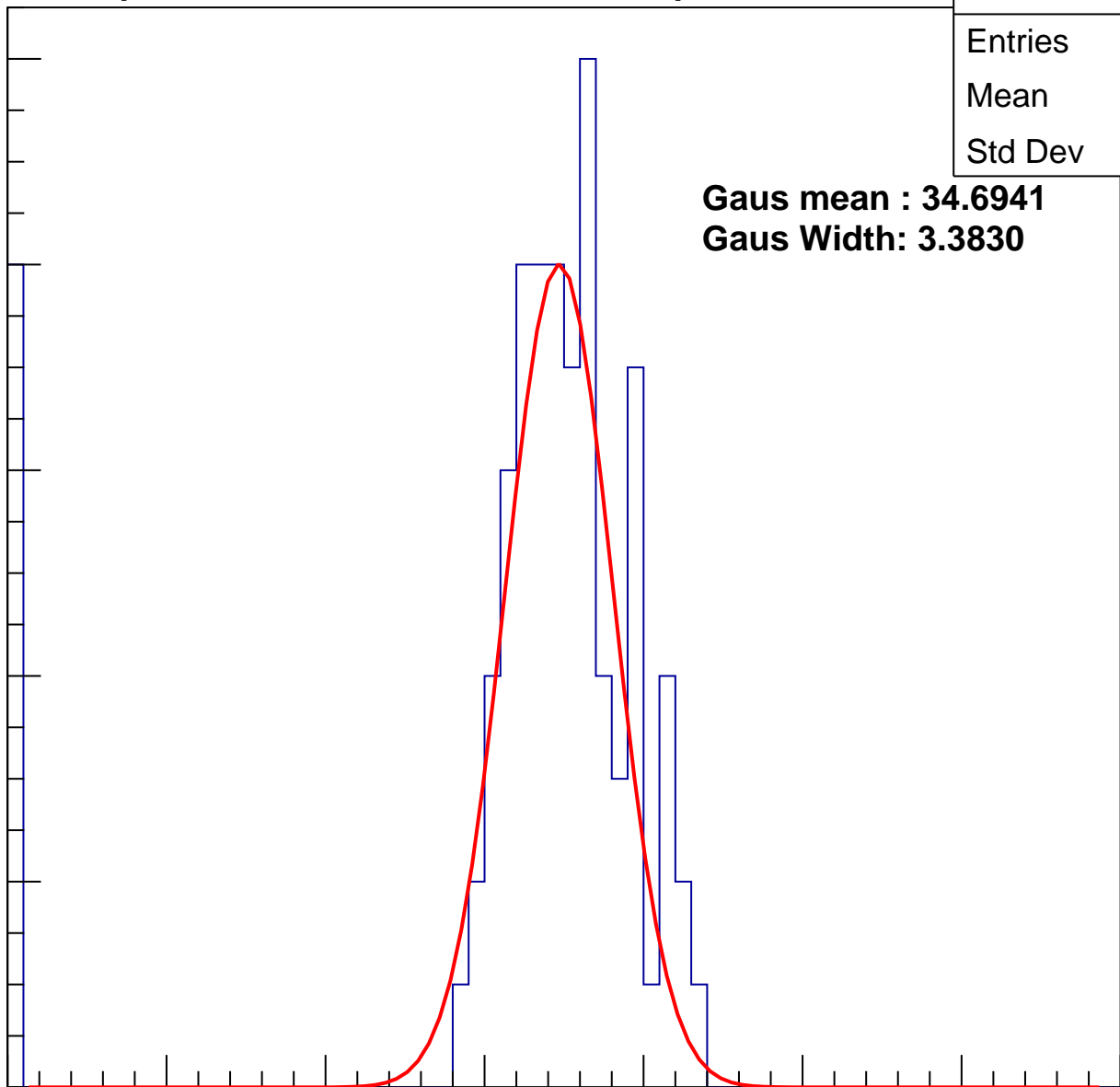
**Gaus Width: 3.3830**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch86, adc2

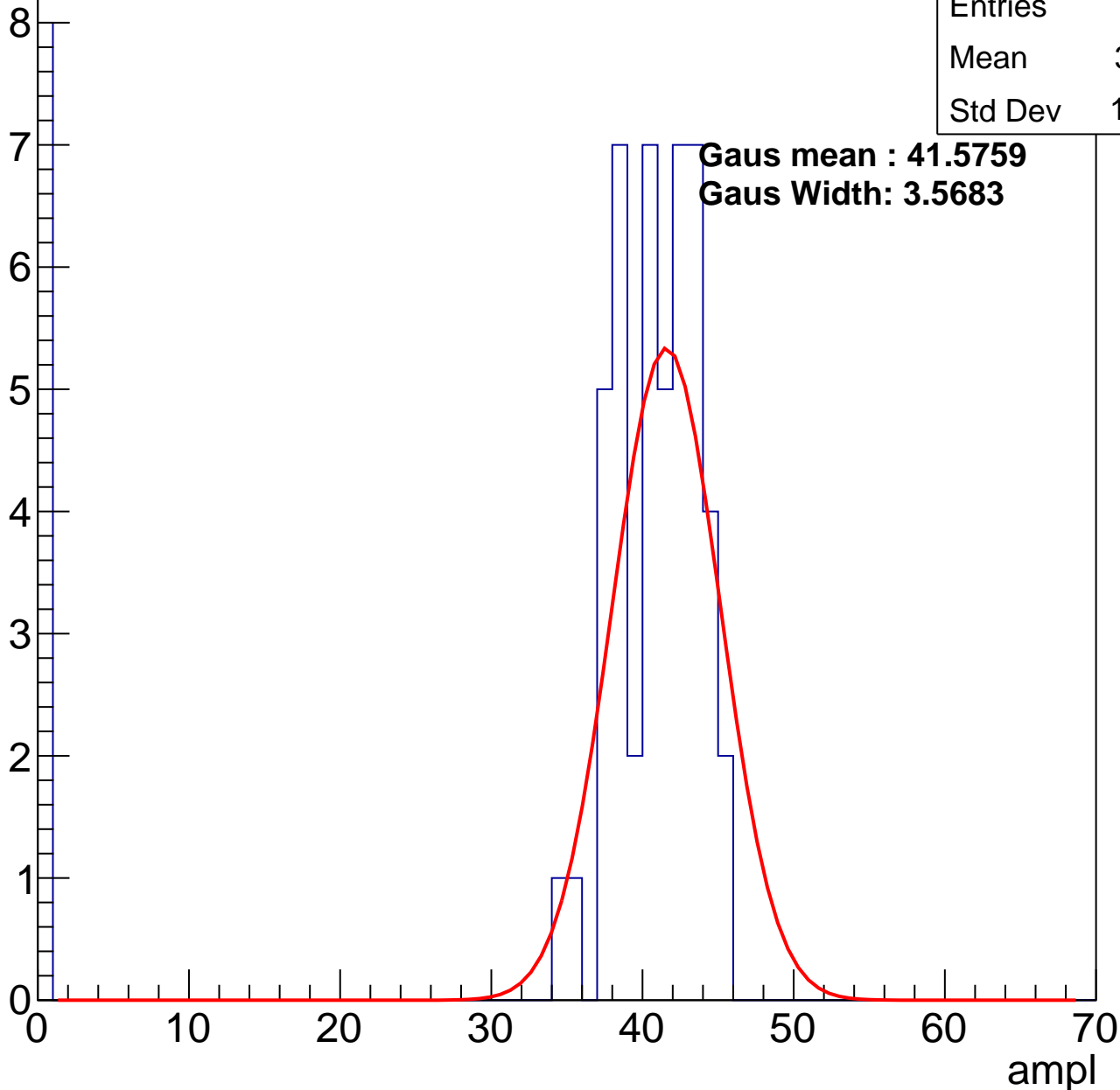
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	56
Mean	34.71
Std Dev	14.38

**Gaus mean : 41.5759**

**Gaus Width: 3.5683**

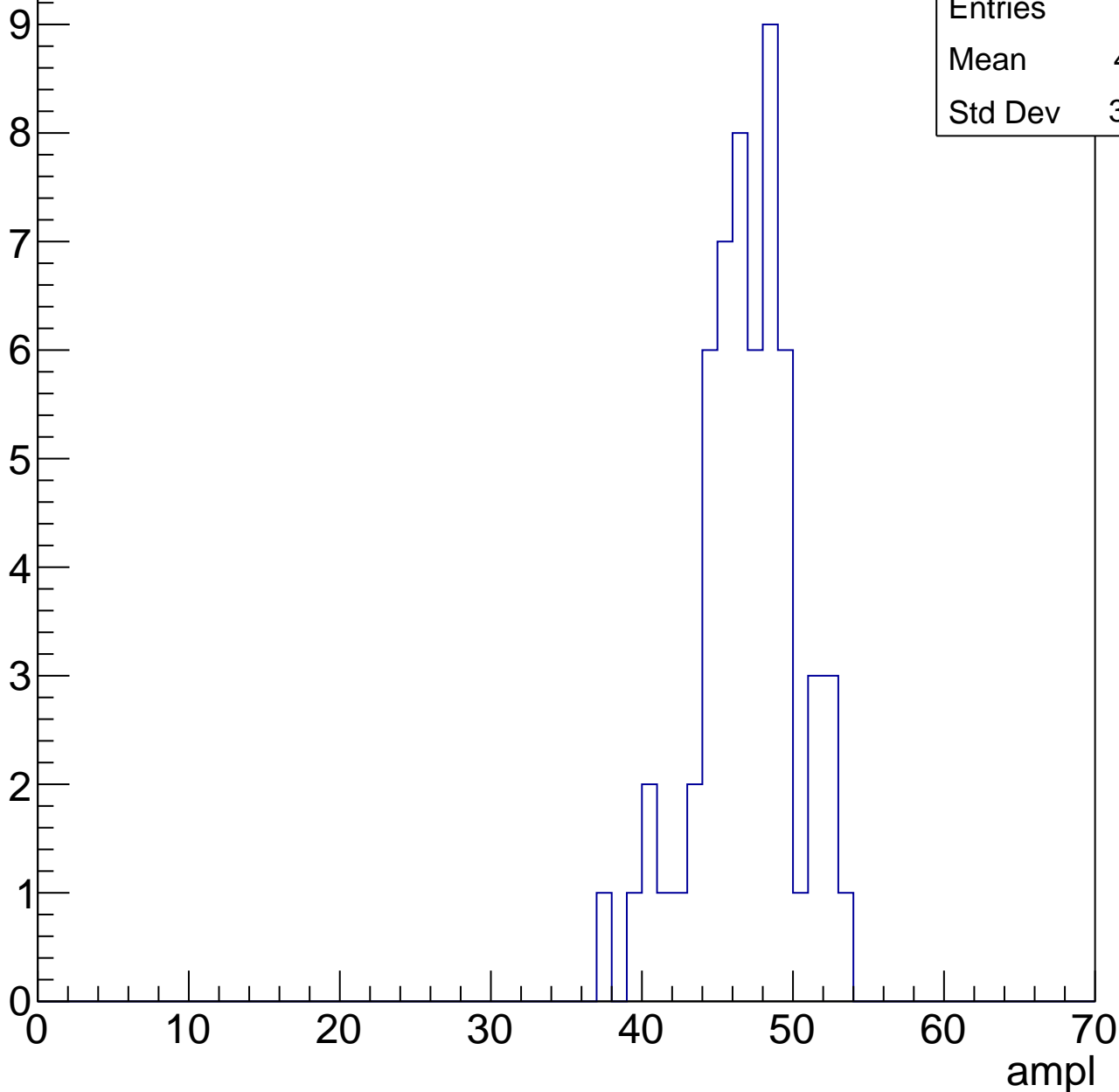


# B1L103S, U3-ch86, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	46.41
Std Dev	3.285

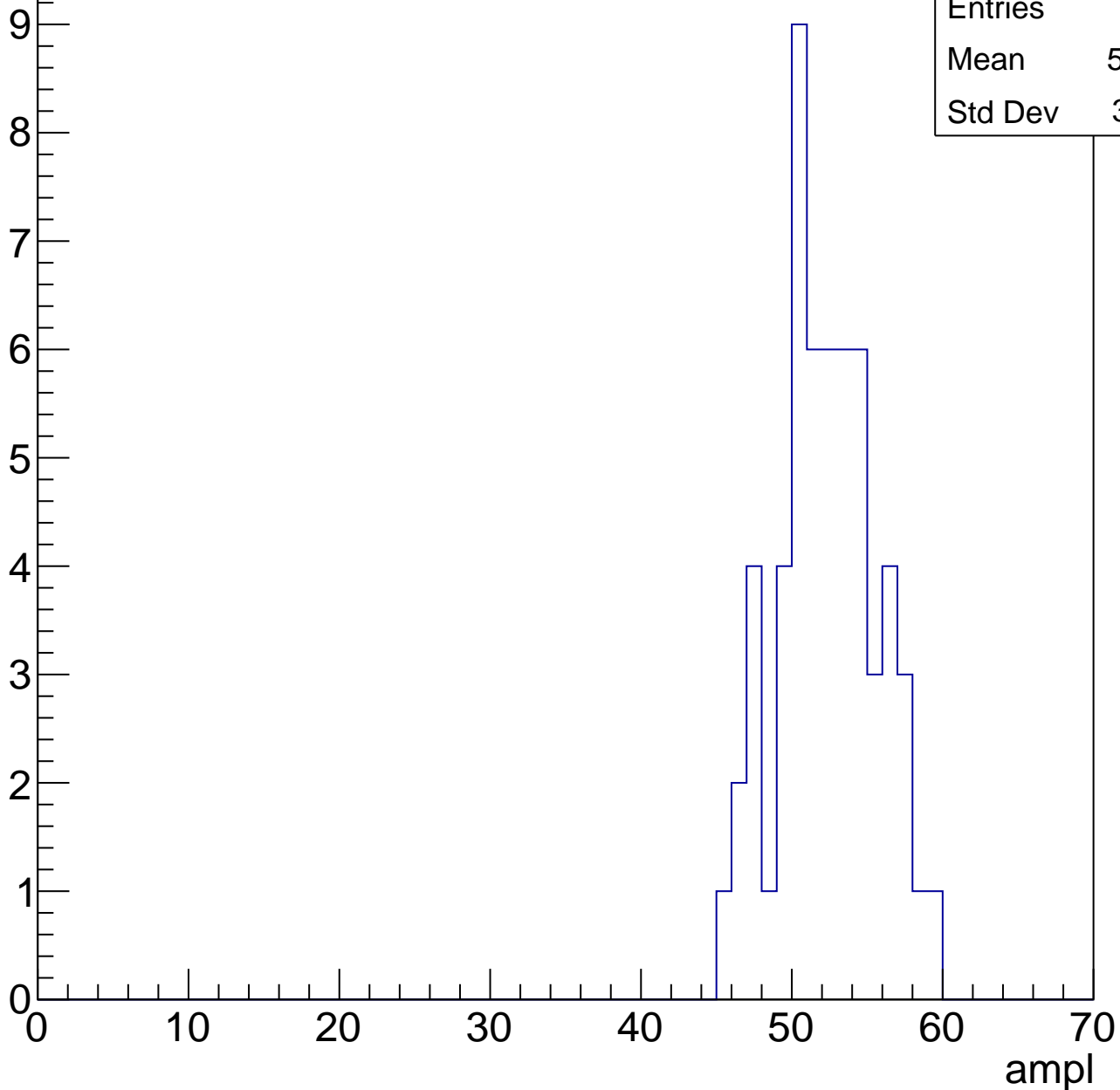


# B1L103S, U3-ch86, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	57
Mean	51.86
Std Dev	3.231

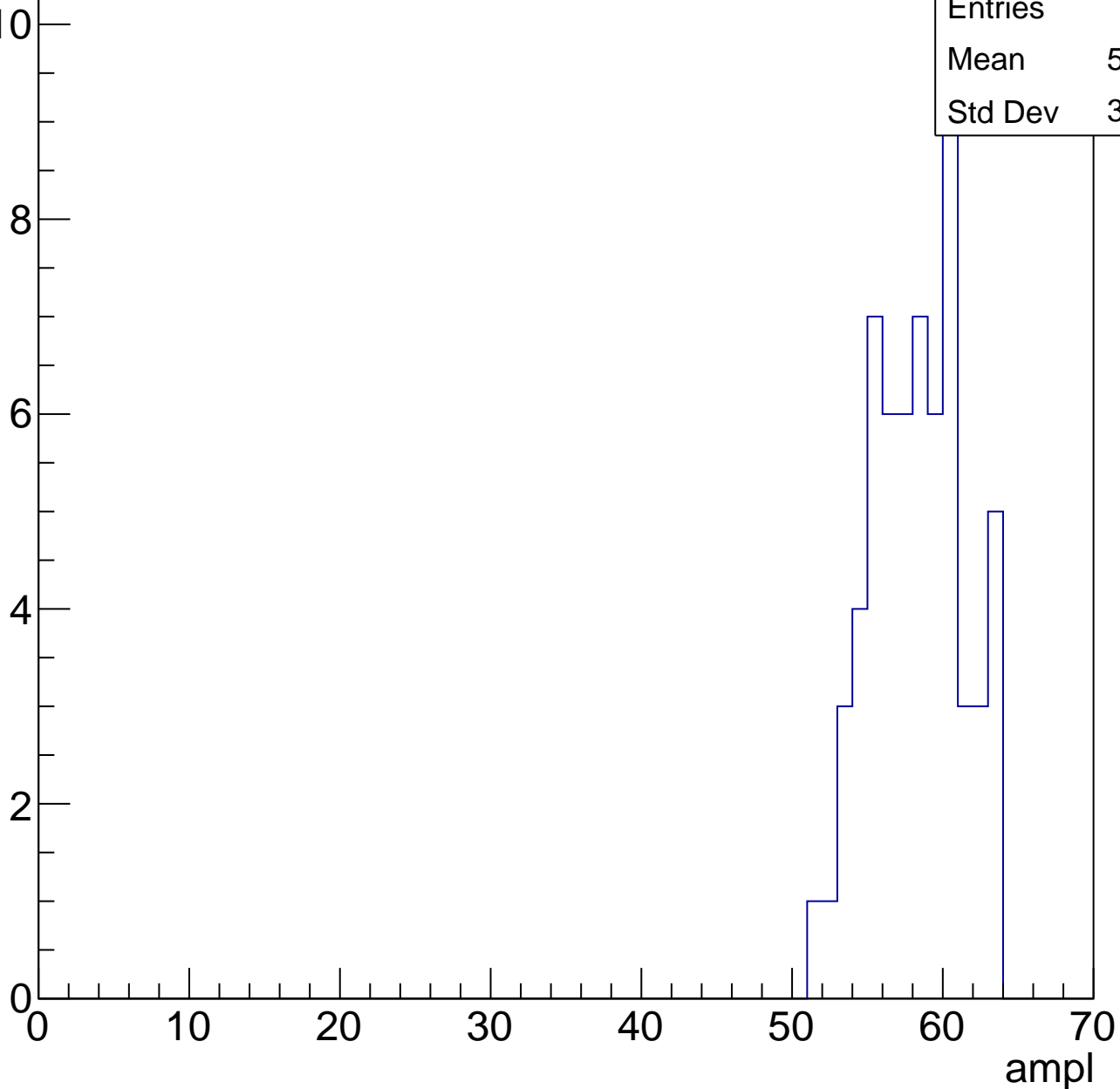


# B1L103S, U3-ch86, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	57.82
Std Dev	3.008

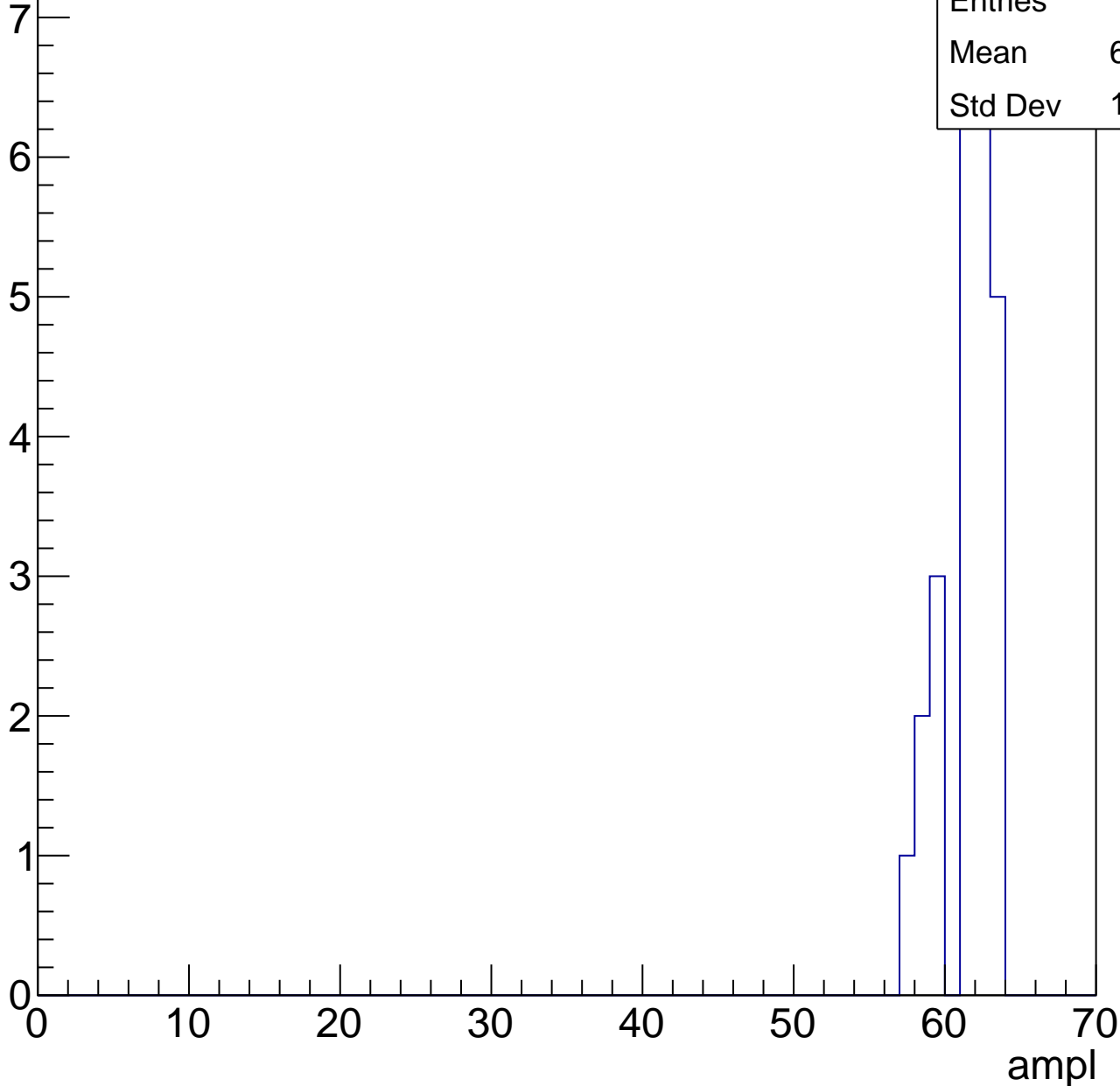


# B1L103S, U3-ch86, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	25
Mean	61.04
Std Dev	1.708



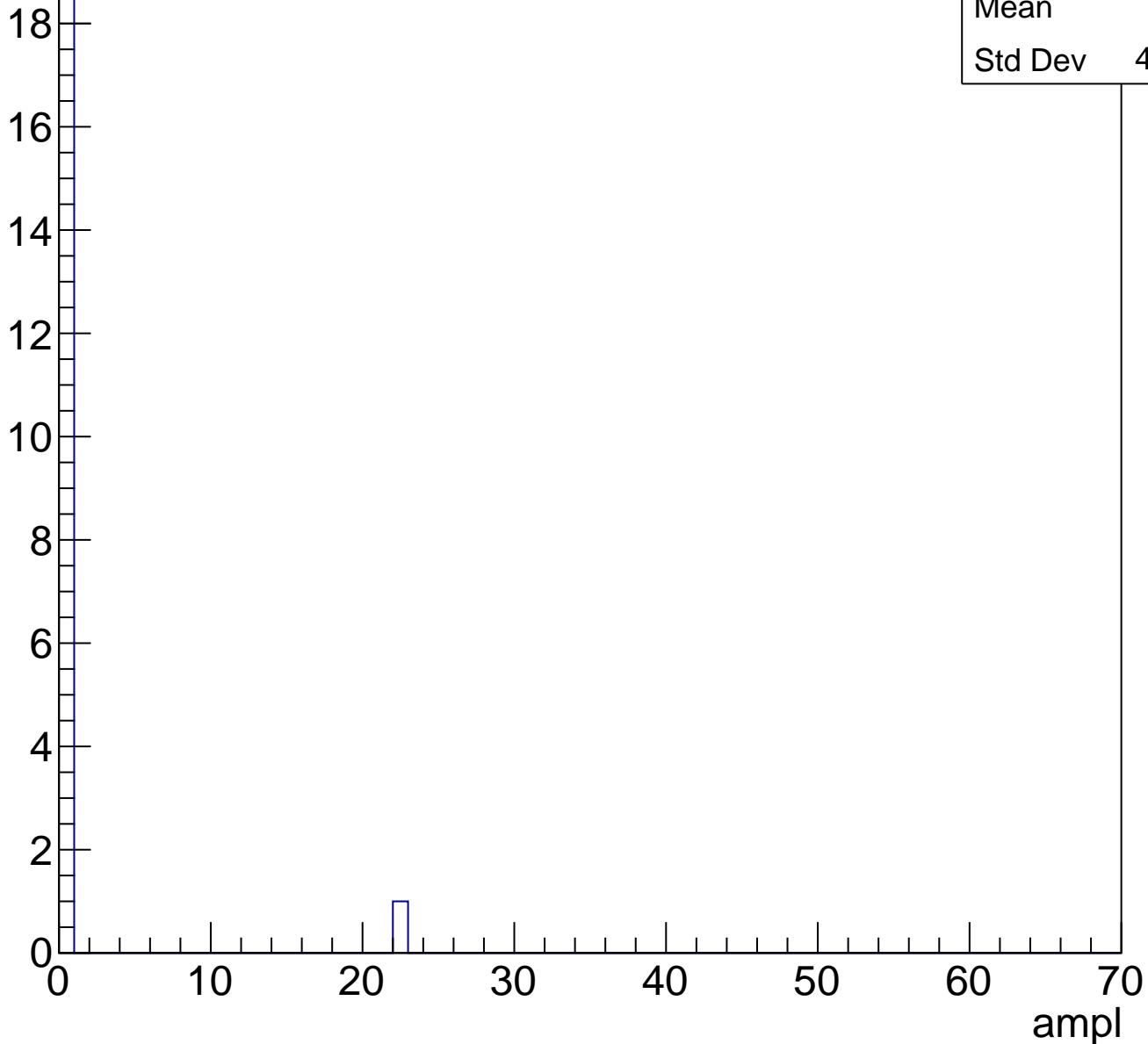


# B1L103S, U3-ch86, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	1.1
Std Dev	4.795

Entry



# B1L103S, U3-ch87, adc0

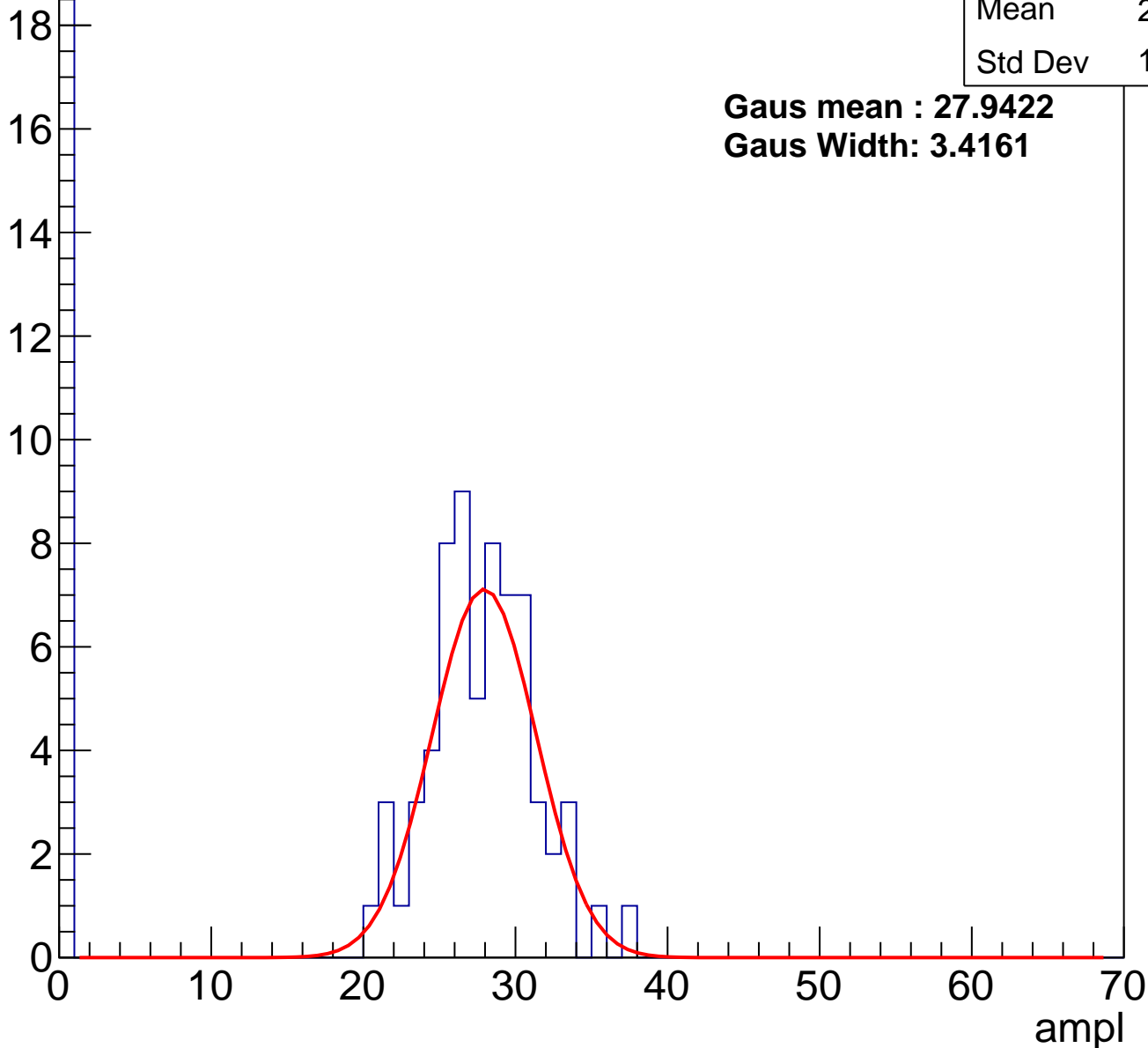
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	85
Mean	21.22
Std Dev	11.78

**Gaus mean : 27.9422**

**Gaus Width: 3.4161**

Entry



# B1L103S, U3-ch87, adc1

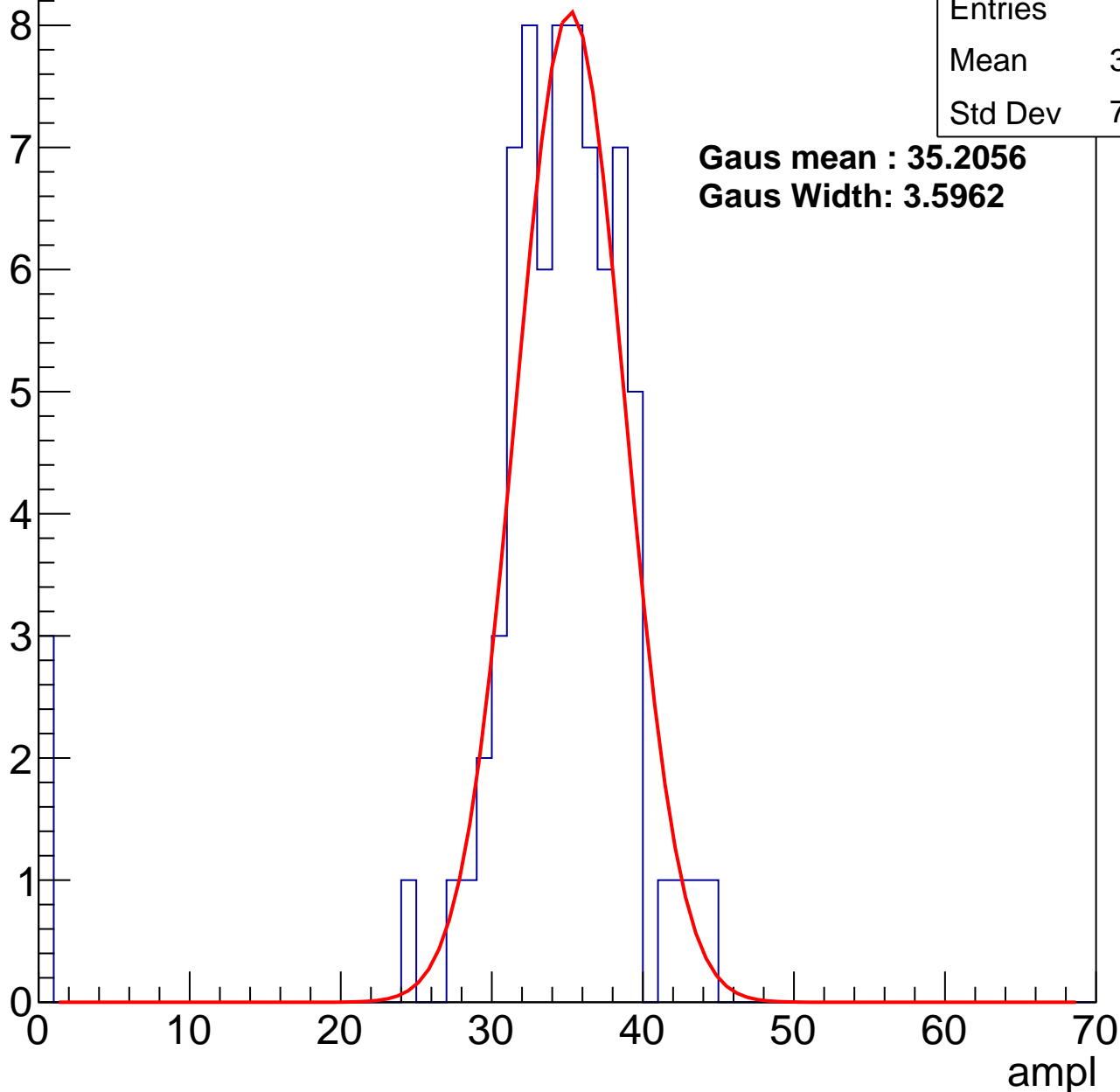
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	77
Mean	33.18
Std Dev	7.578

**Gaus mean : 35.2056**

**Gaus Width: 3.5962**



# B1L103S, U3-ch87, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	87
Mean	34.37
Std Dev	16.02

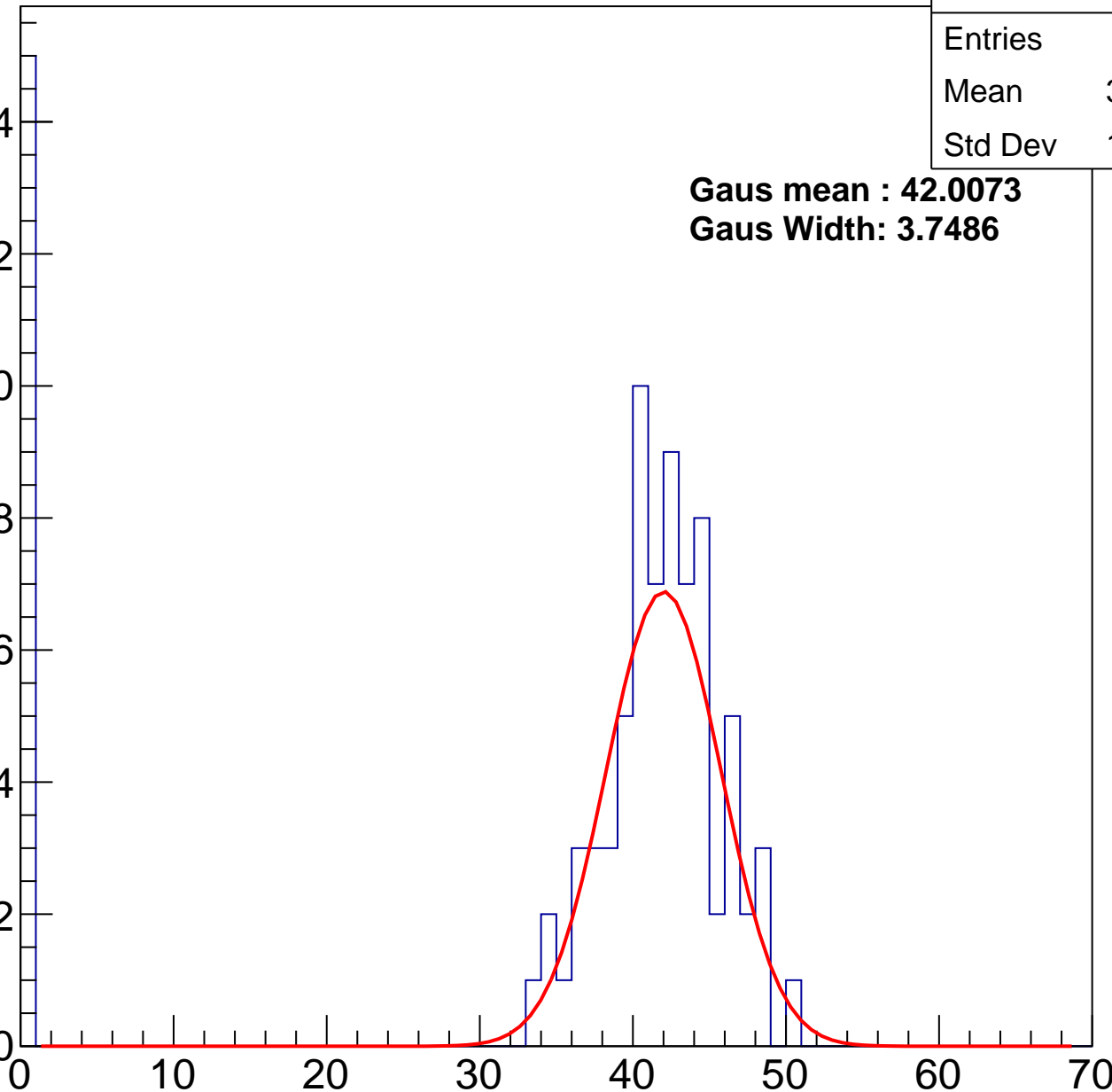
**Gaus mean : 42.0073**

**Gaus Width: 3.7486**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

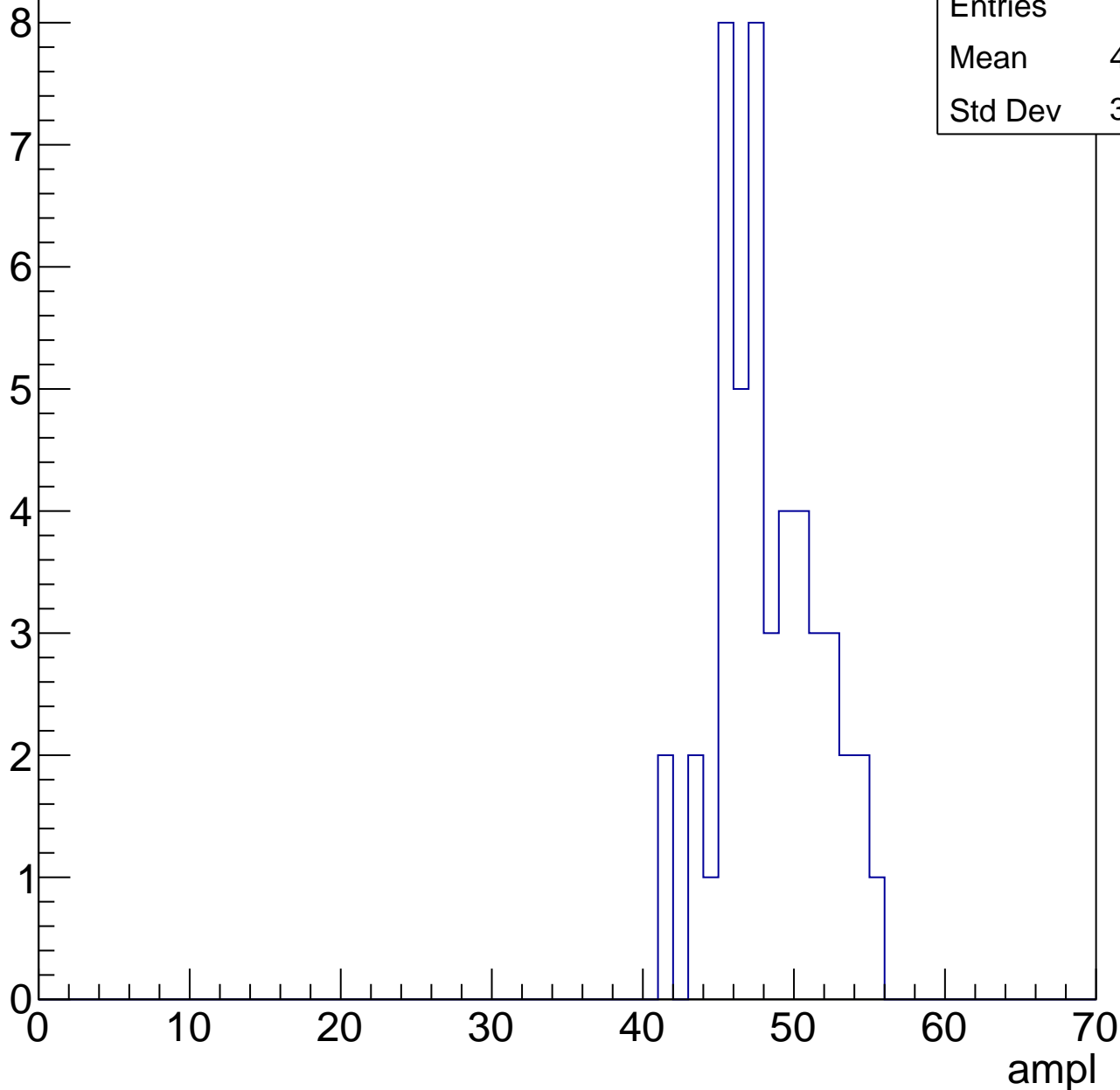


# B1L103S, U3-ch87, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

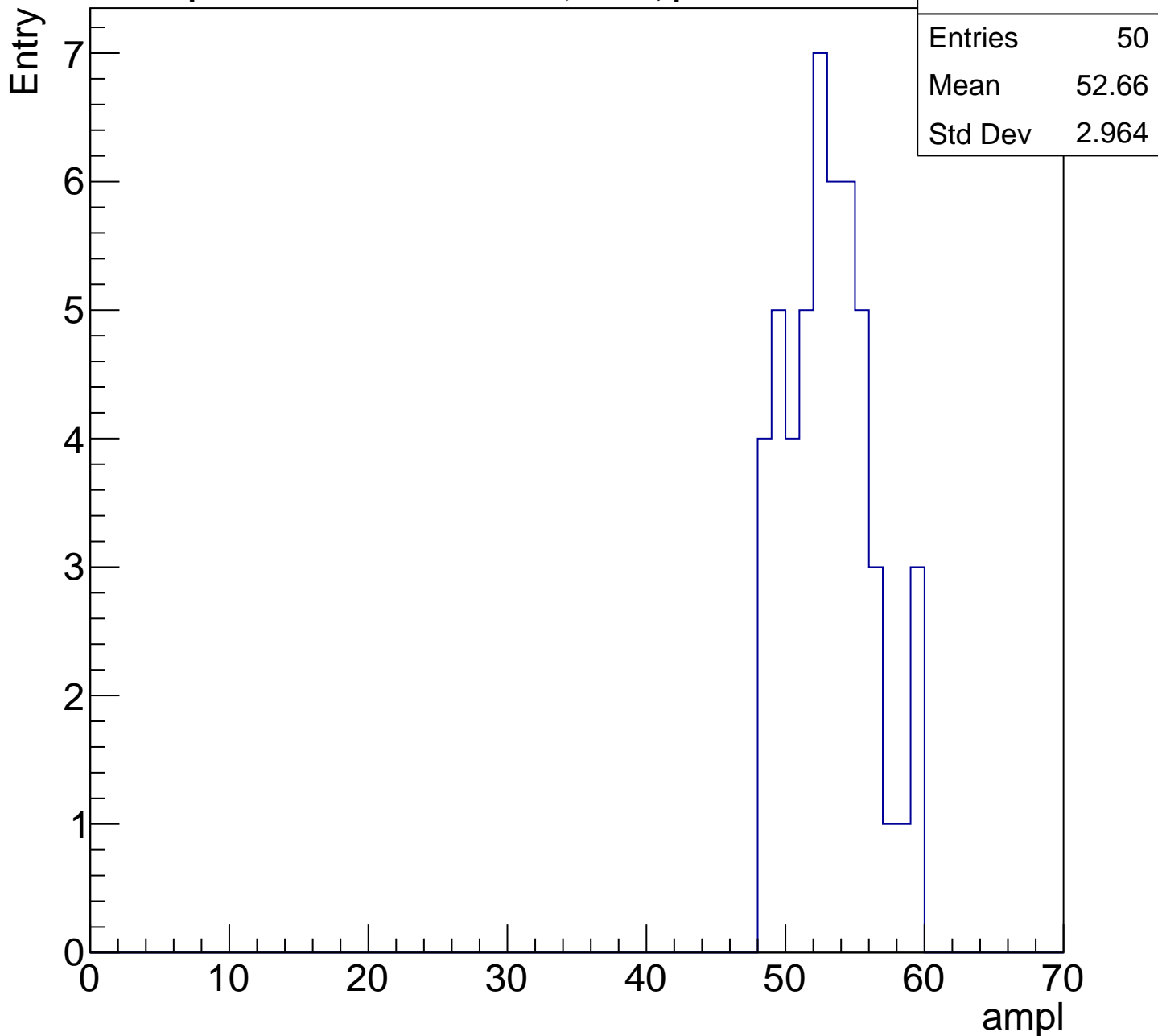
Entry

Entries	48
Mean	47.83
Std Dev	3.319



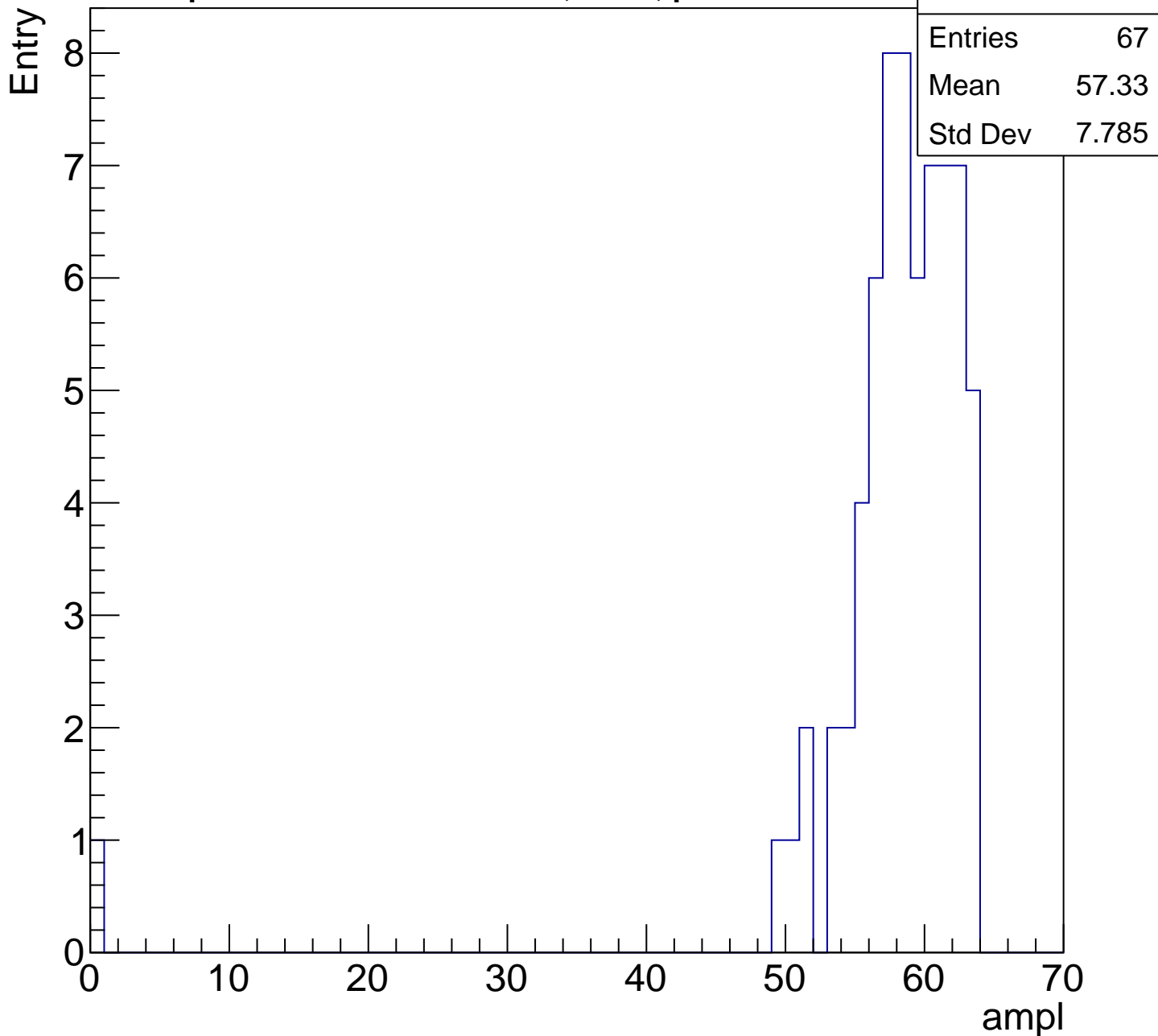
# B1L103S, U3-ch87, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U3-ch87, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

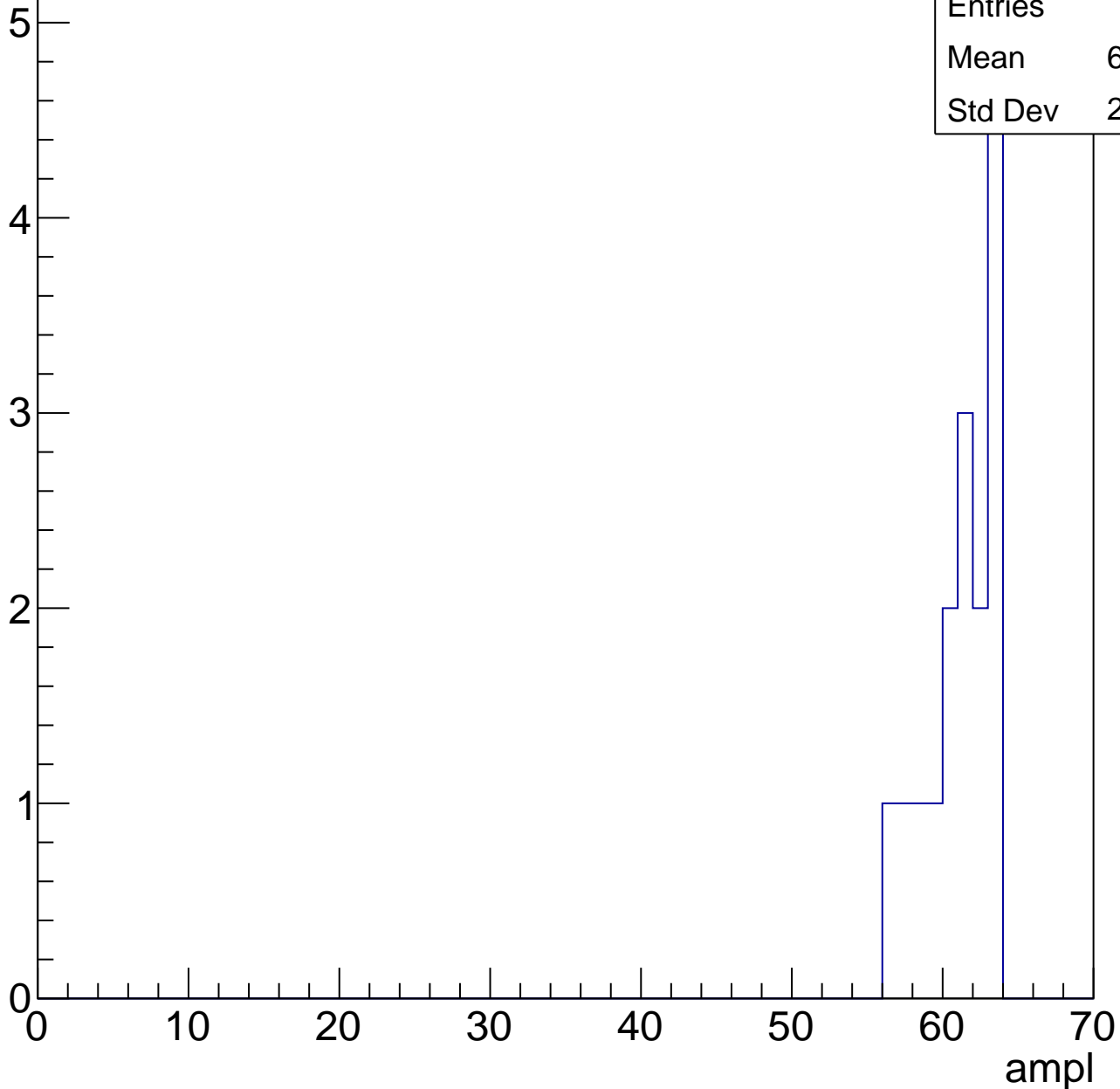


# B1L103S, U3-ch87, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	16
Mean	60.75
Std Dev	2.194



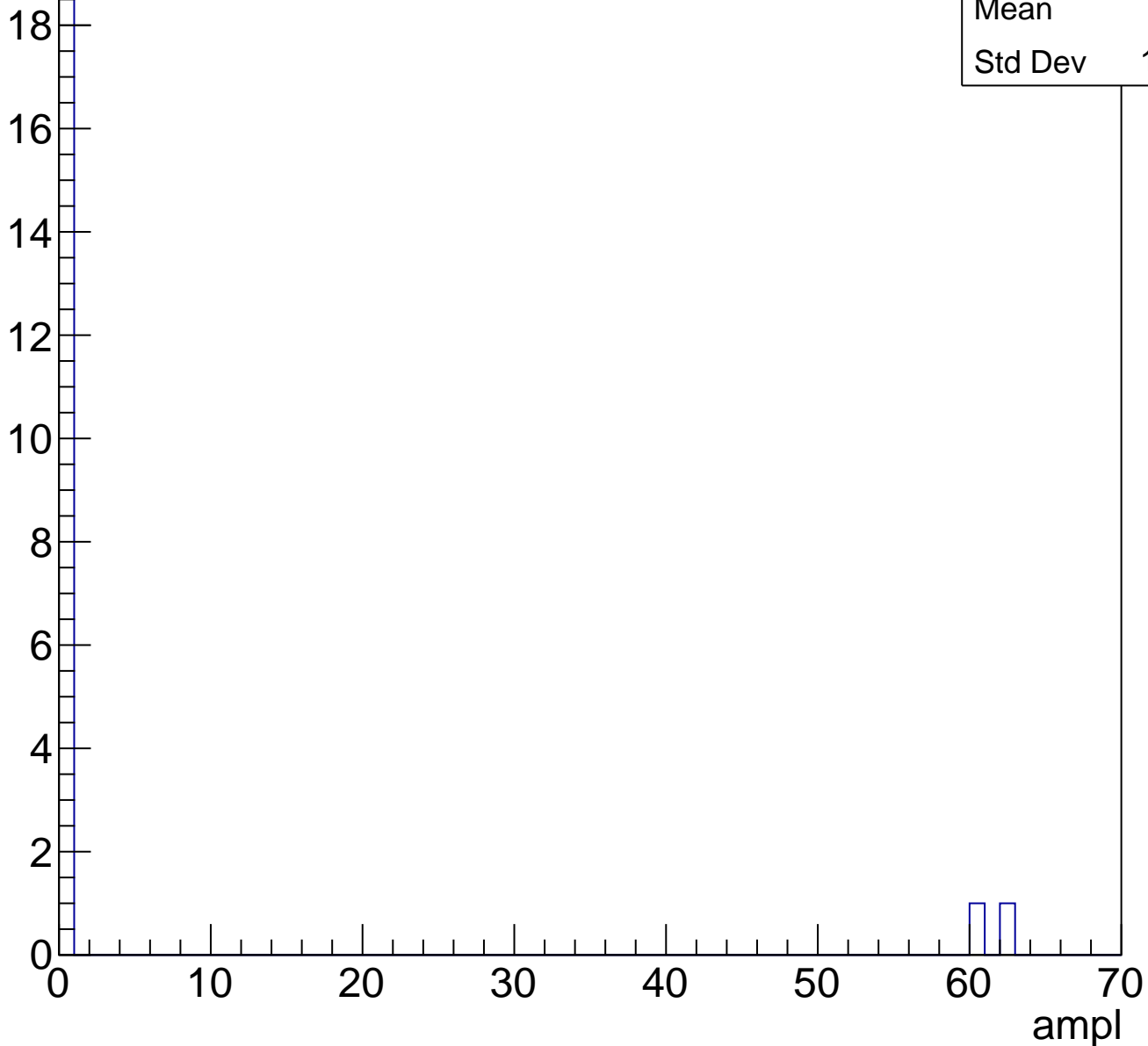


# B1L103S, U3-ch87, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	5.81
Std Dev	17.91

Entry



# B1L103S, U3-ch88, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	80
Mean	21.27
Std Dev	11.56

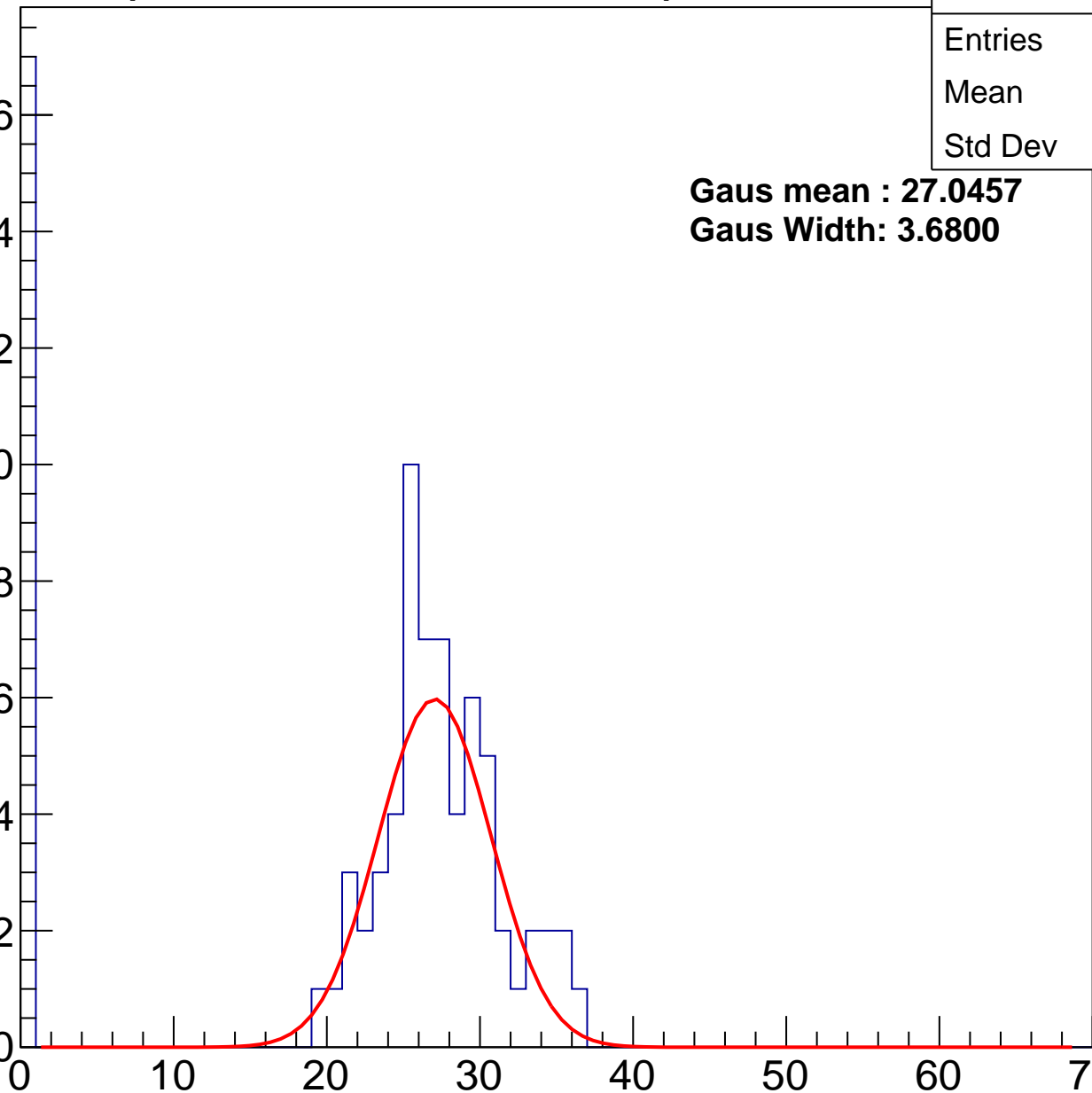
**Gaus mean : 27.0457**

**Gaus Width: 3.6800**

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U3-ch88, adc1

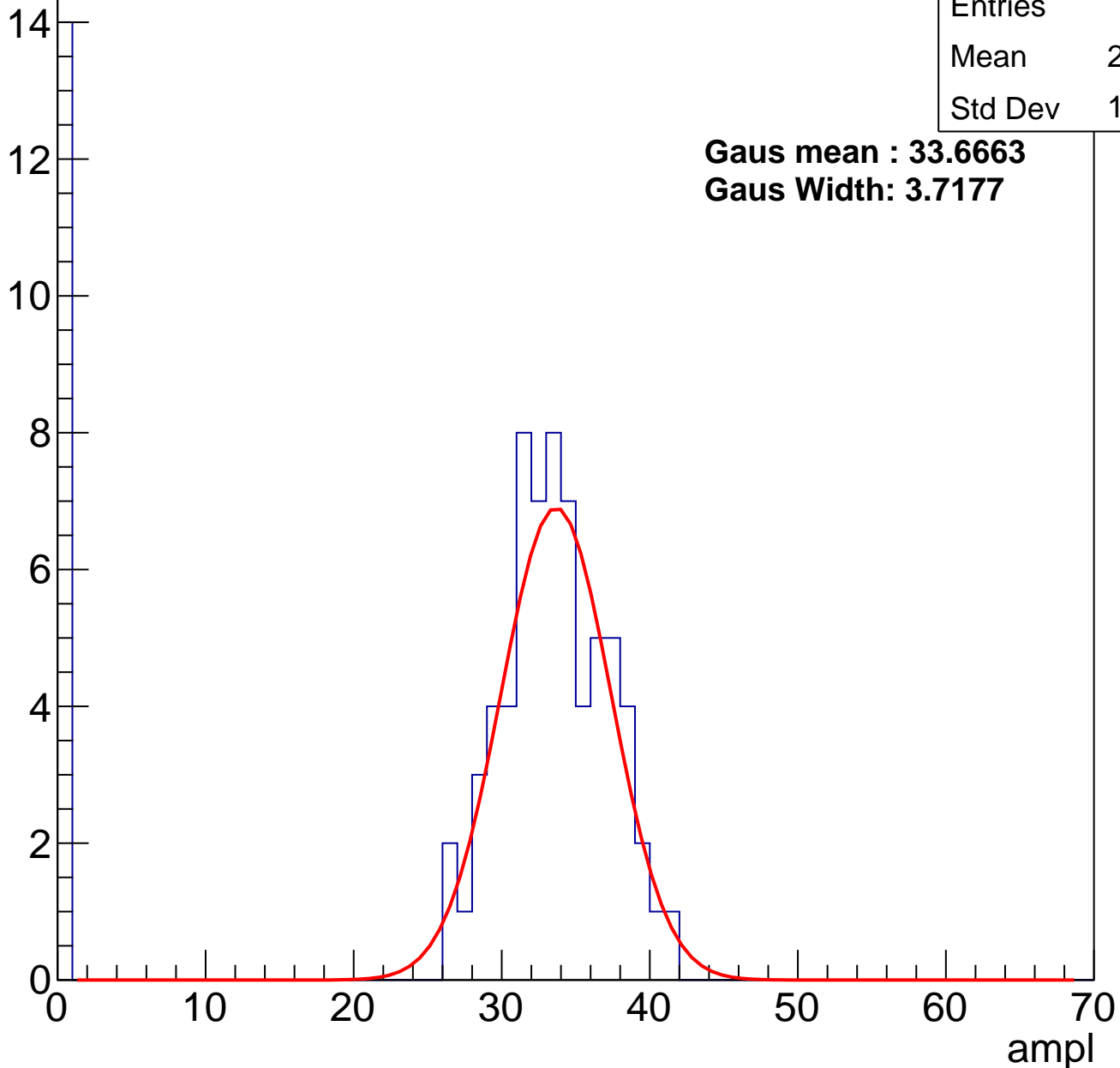
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	80
Mean	27.36
Std Dev	12.98

**Gaus mean : 33.6663**

**Gaus Width: 3.7177**

Entry



# B1L103S, U3-ch88, adc2

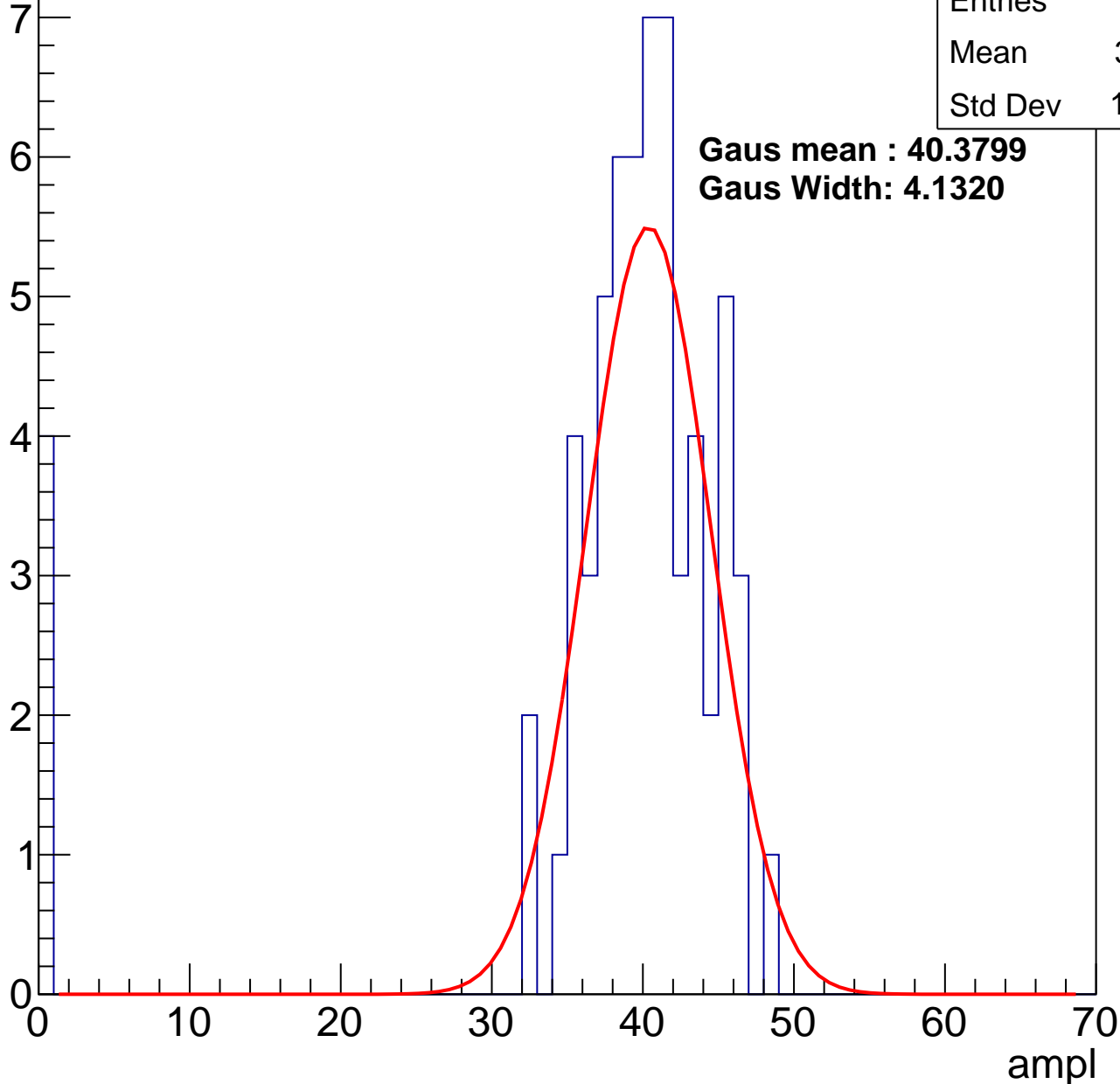
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	37.41
Std Dev	10.35

**Gaus mean : 40.3799**

**Gaus Width: 4.1320**

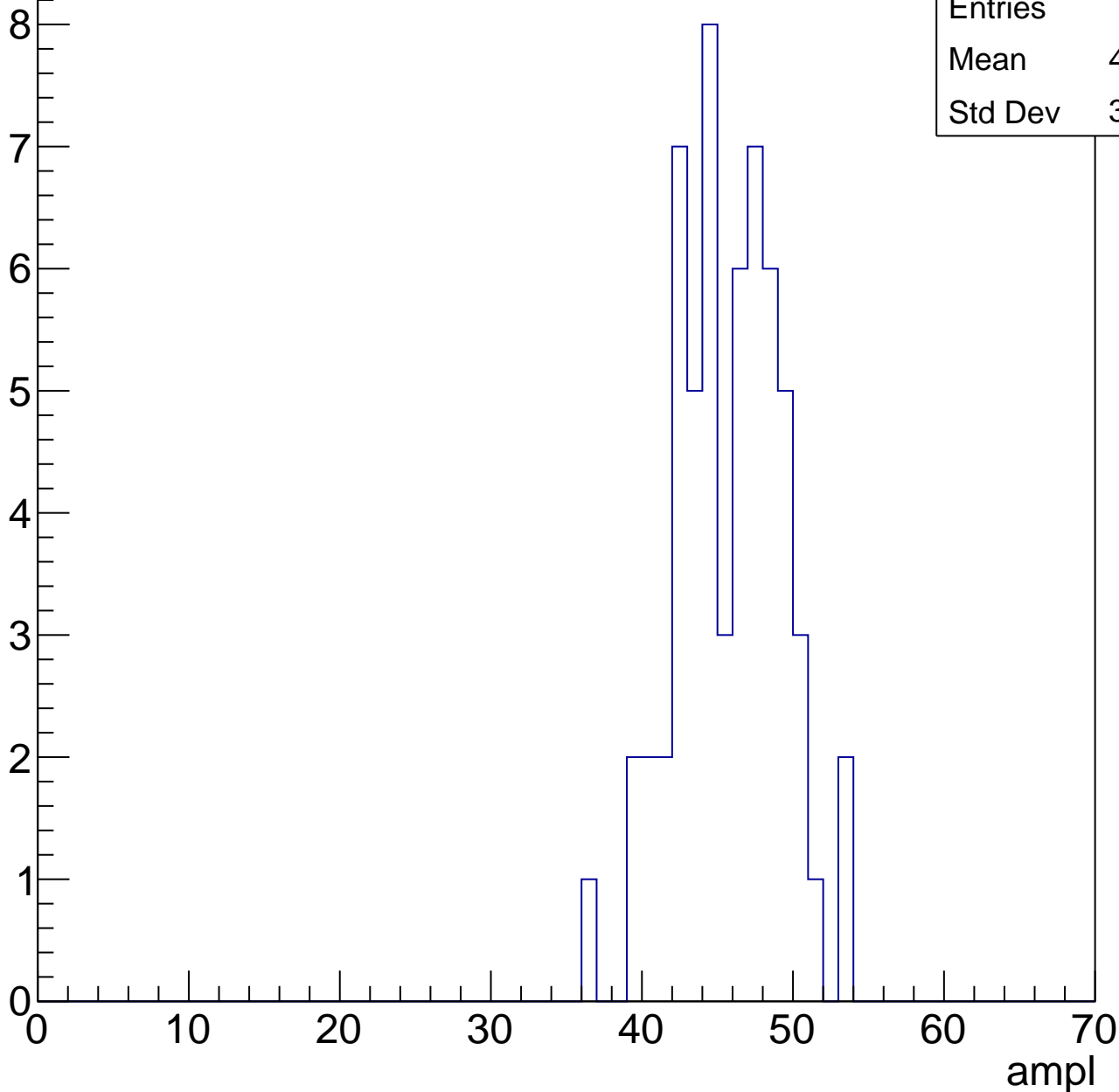


# B1L103S, U3-ch88, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

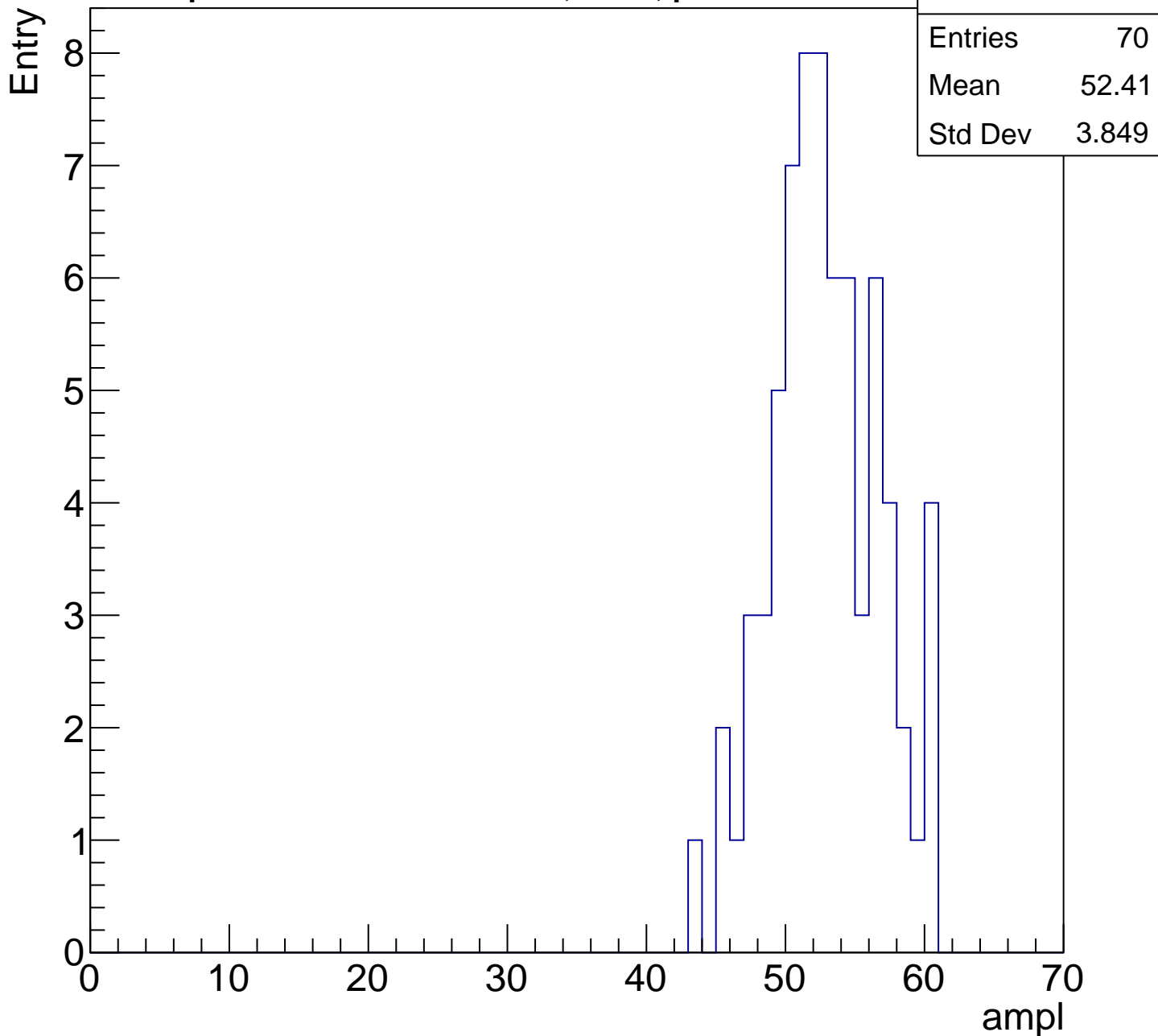
Entry

Entries	60
Mean	45.28
Std Dev	3.484



# B1L103S, U3-ch88, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

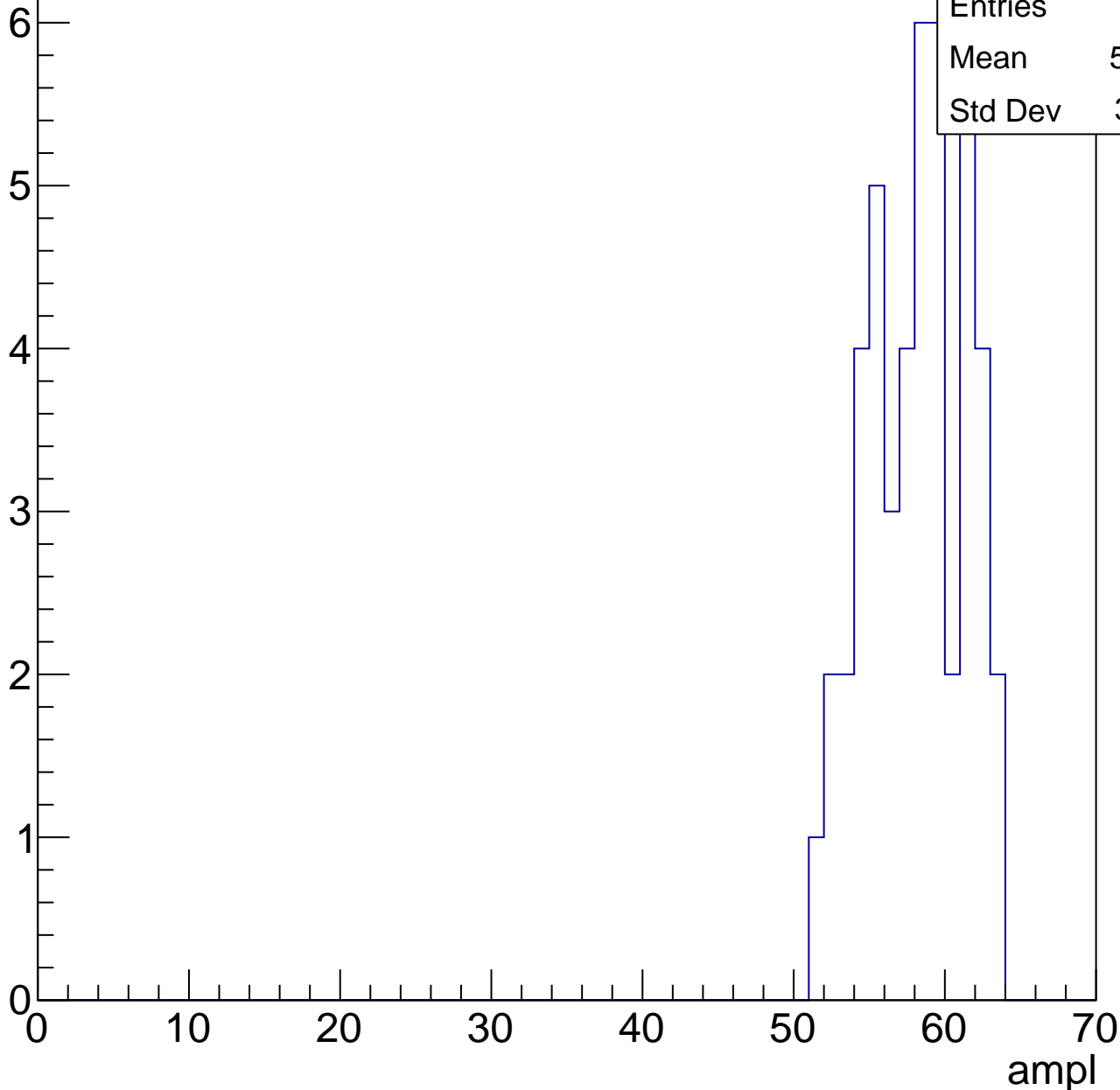


# B1L103S, U3-ch88, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	47
Mean	57.66
Std Dev	3.171

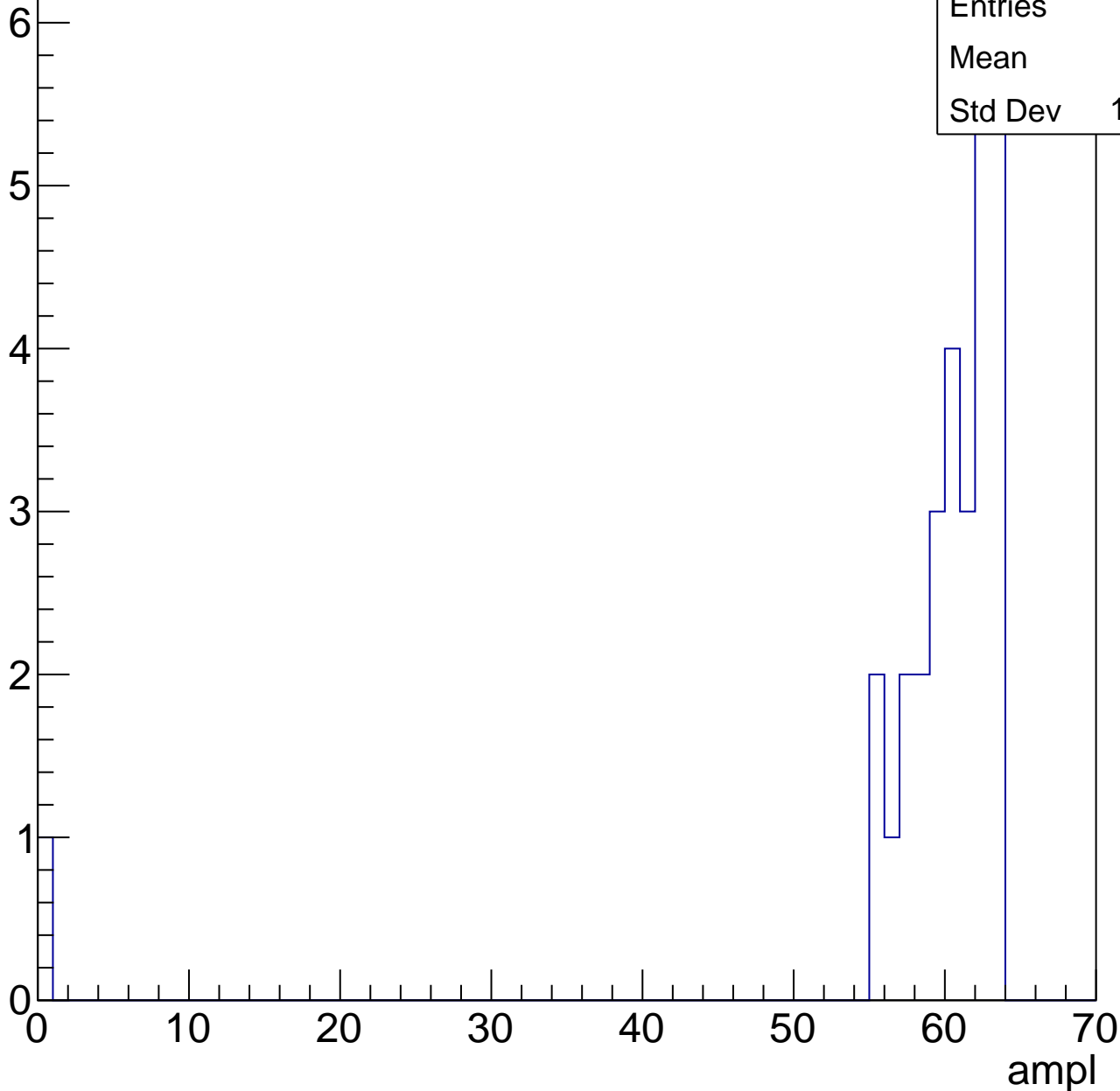


# B1L103S, U3-ch88, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	30
Mean	58.2
Std Dev	11.07



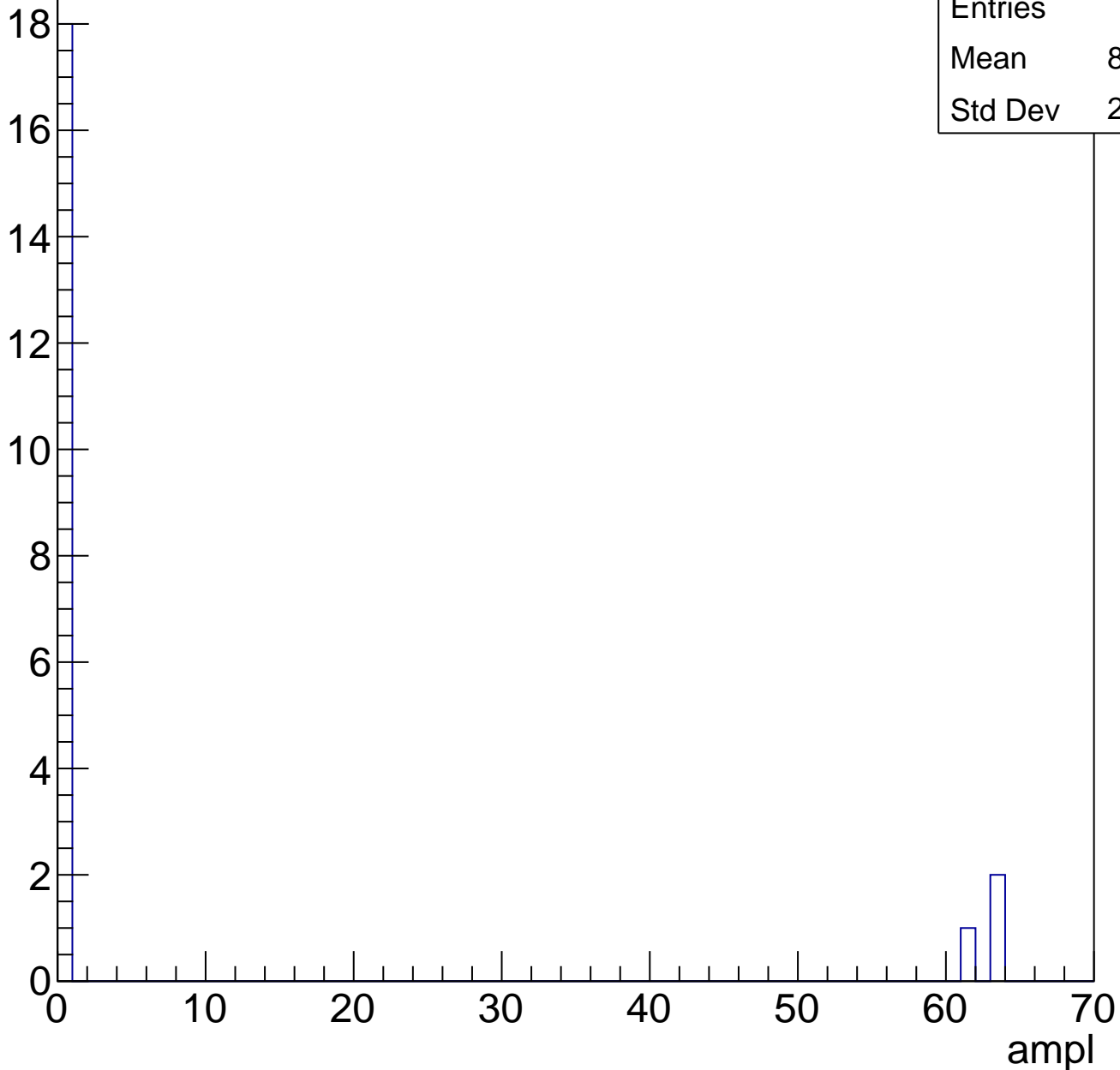


# B1L103S, U3-ch88, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	8.905
Std Dev	21.82

Entry



# B1L103S, U3-ch89, adc0

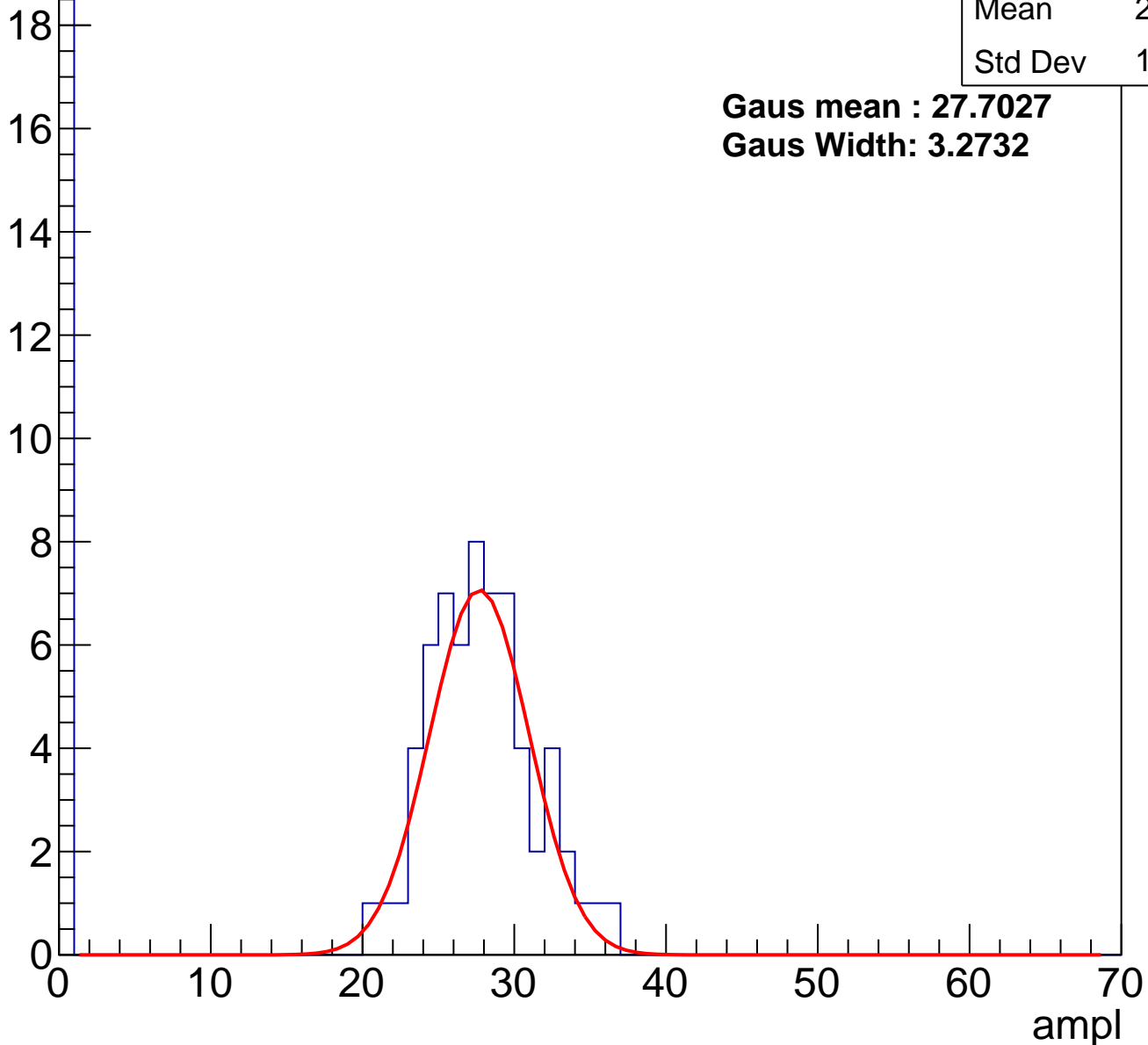
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	82
Mean	21.05
Std Dev	11.93

**Gaus mean : 27.7027**

**Gaus Width: 3.2732**

Entry



# B1L103S, U3-ch89, adc1

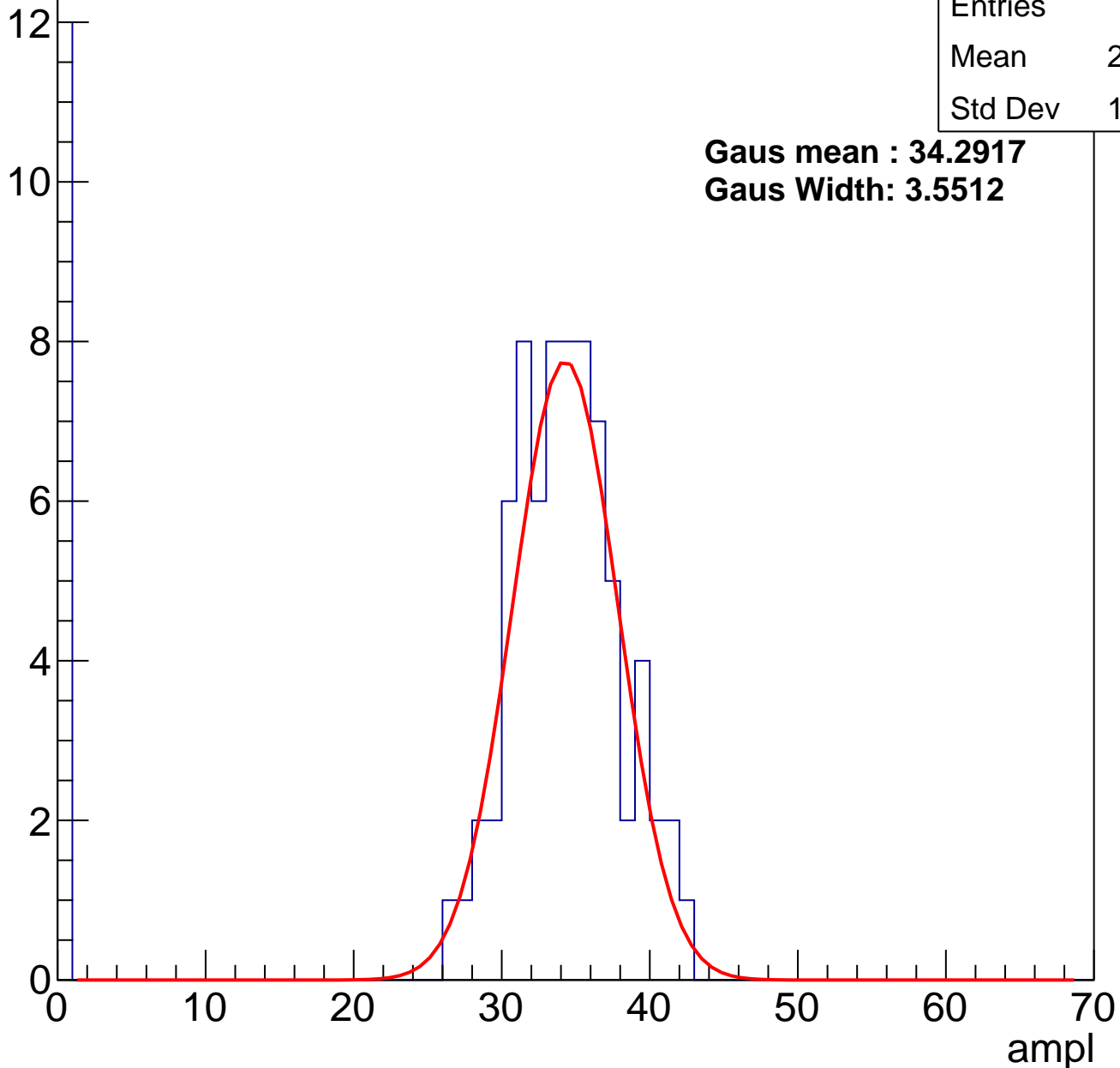
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	85
Mean	29.13
Std Dev	12.24

**Gaus mean : 34.2917**

**Gaus Width: 3.5512**

Entry



# B1L103S, U3-ch89, adc2

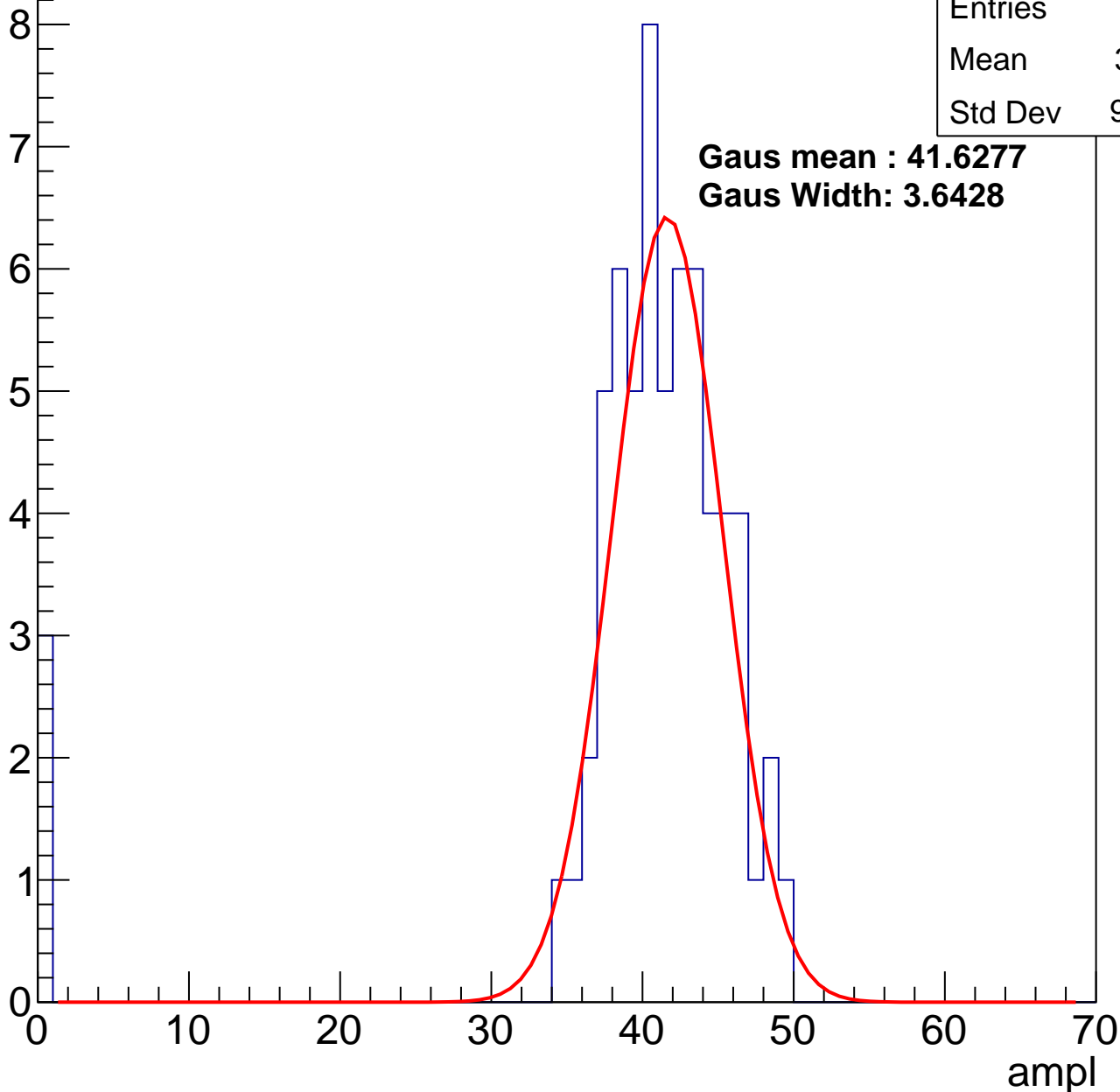
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	64
Mean	39.31
Std Dev	9.342

**Gaus mean : 41.6277**

**Gaus Width: 3.6428**

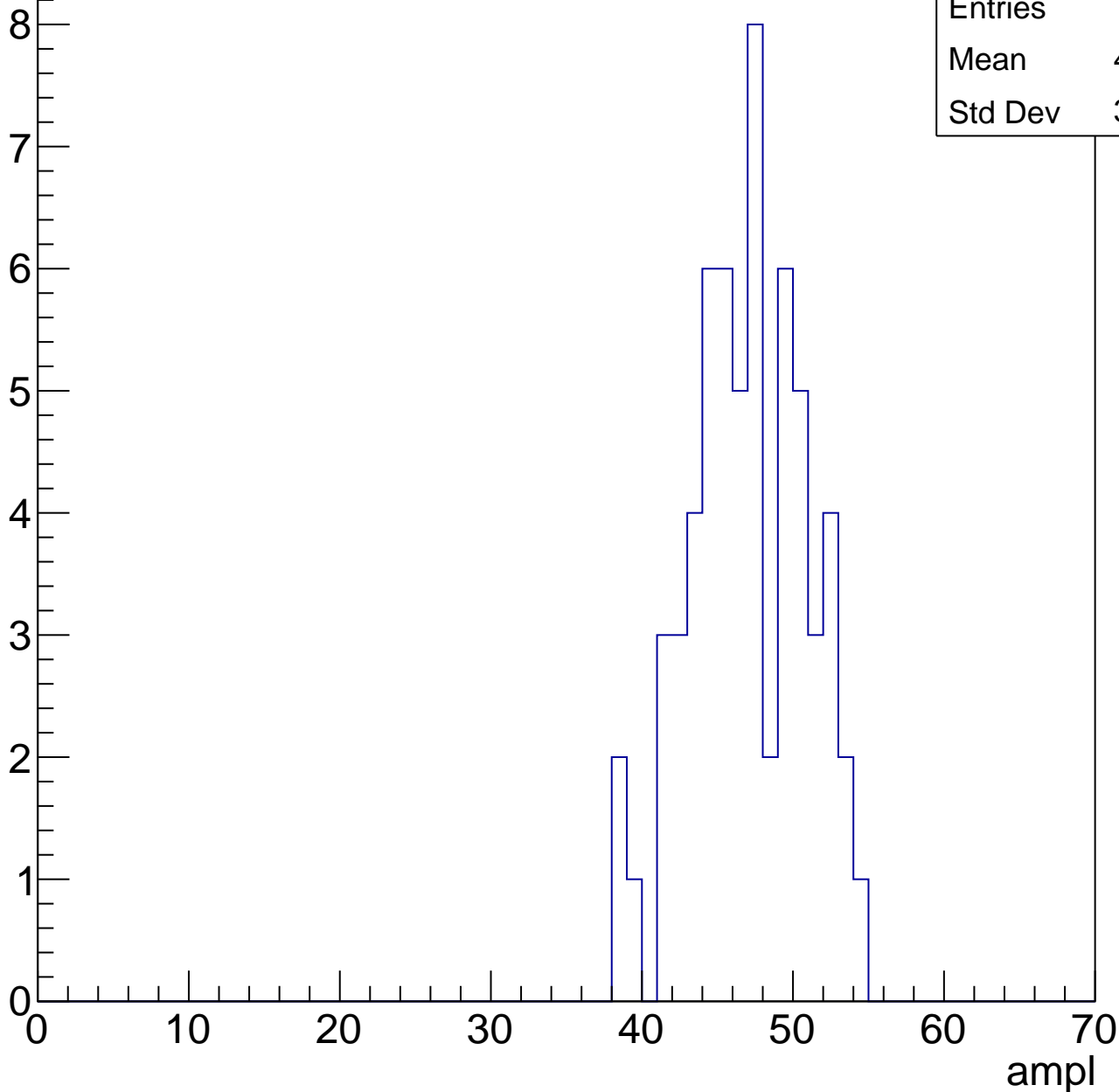


# B1L103S, U3-ch89, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	46.51
Std Dev	3.801

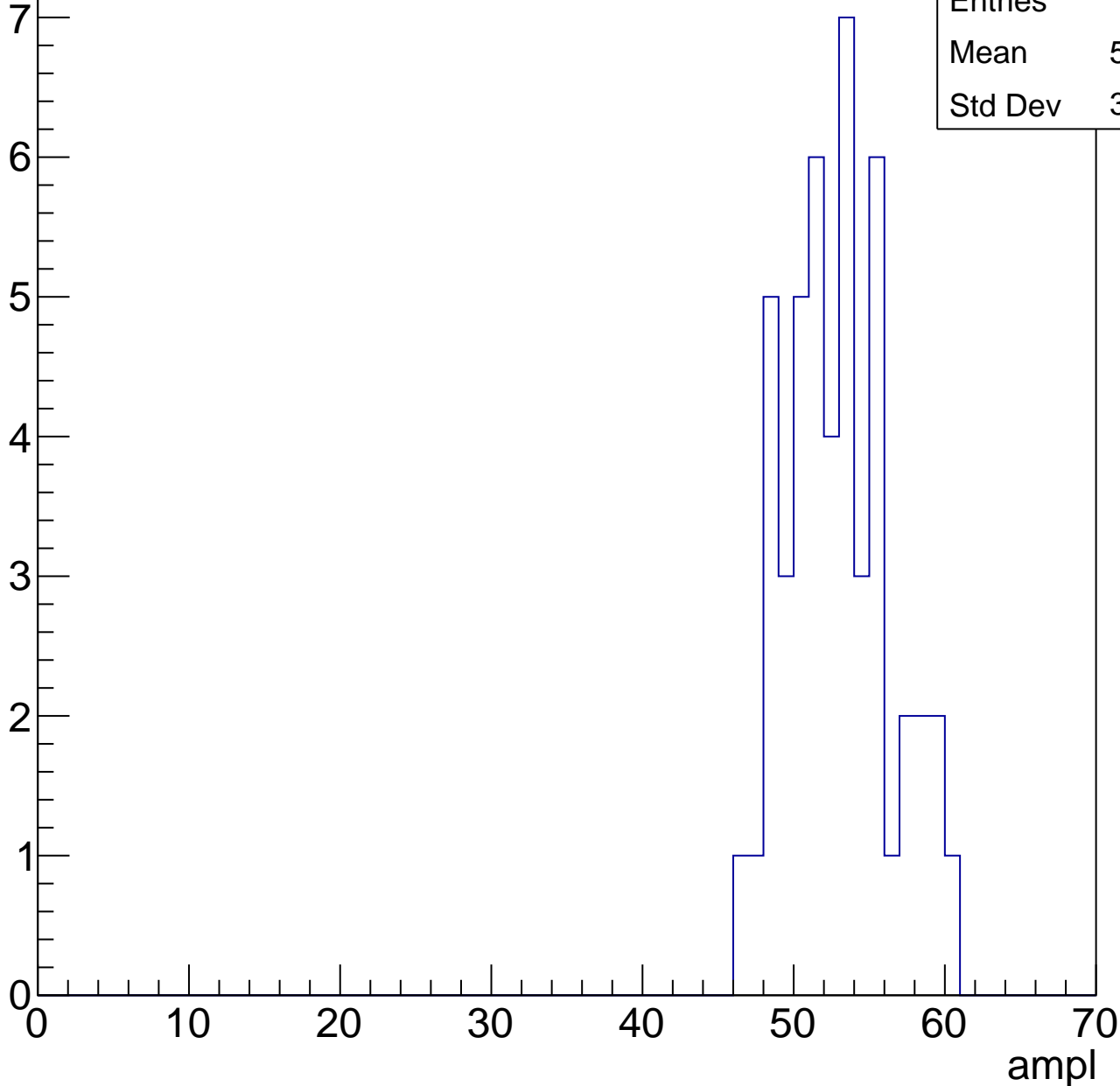


# B1L103S, U3-ch89, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

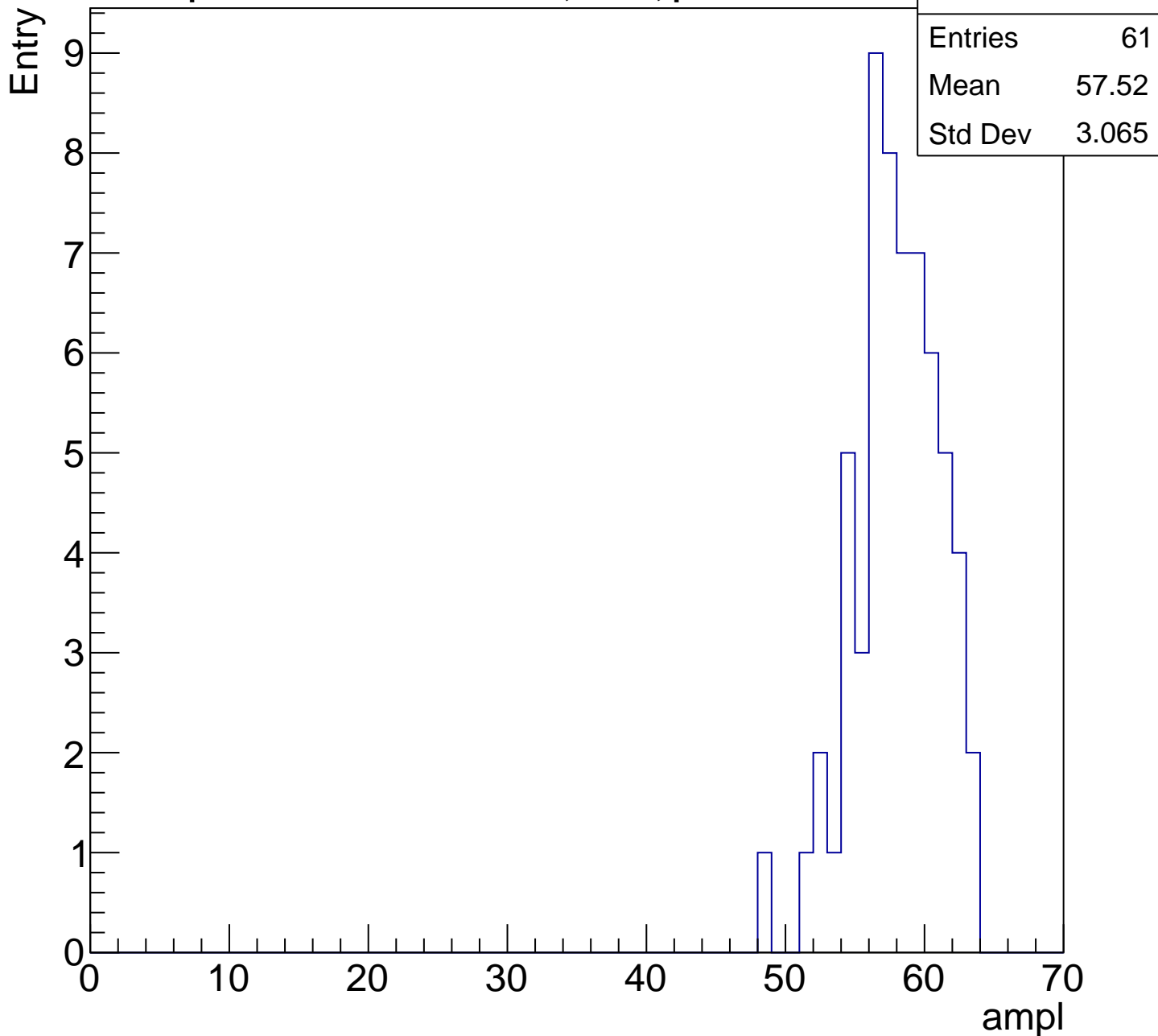
Entry

Entries	49
Mean	52.47
Std Dev	3.369



# B1L103S, U3-ch89, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

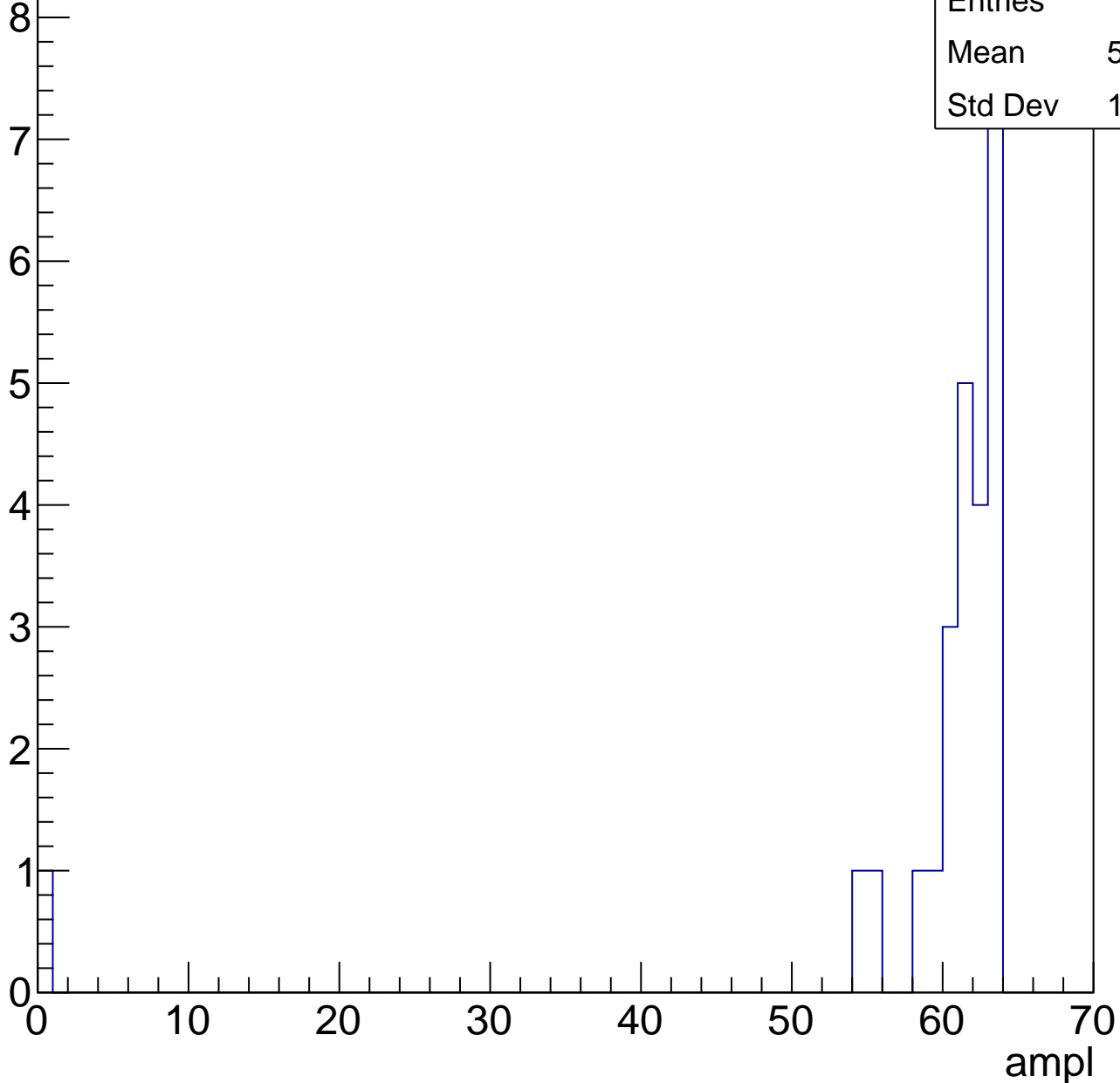


# B1L103S, U3-ch89, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	25
Mean	58.52
Std Dev	12.17



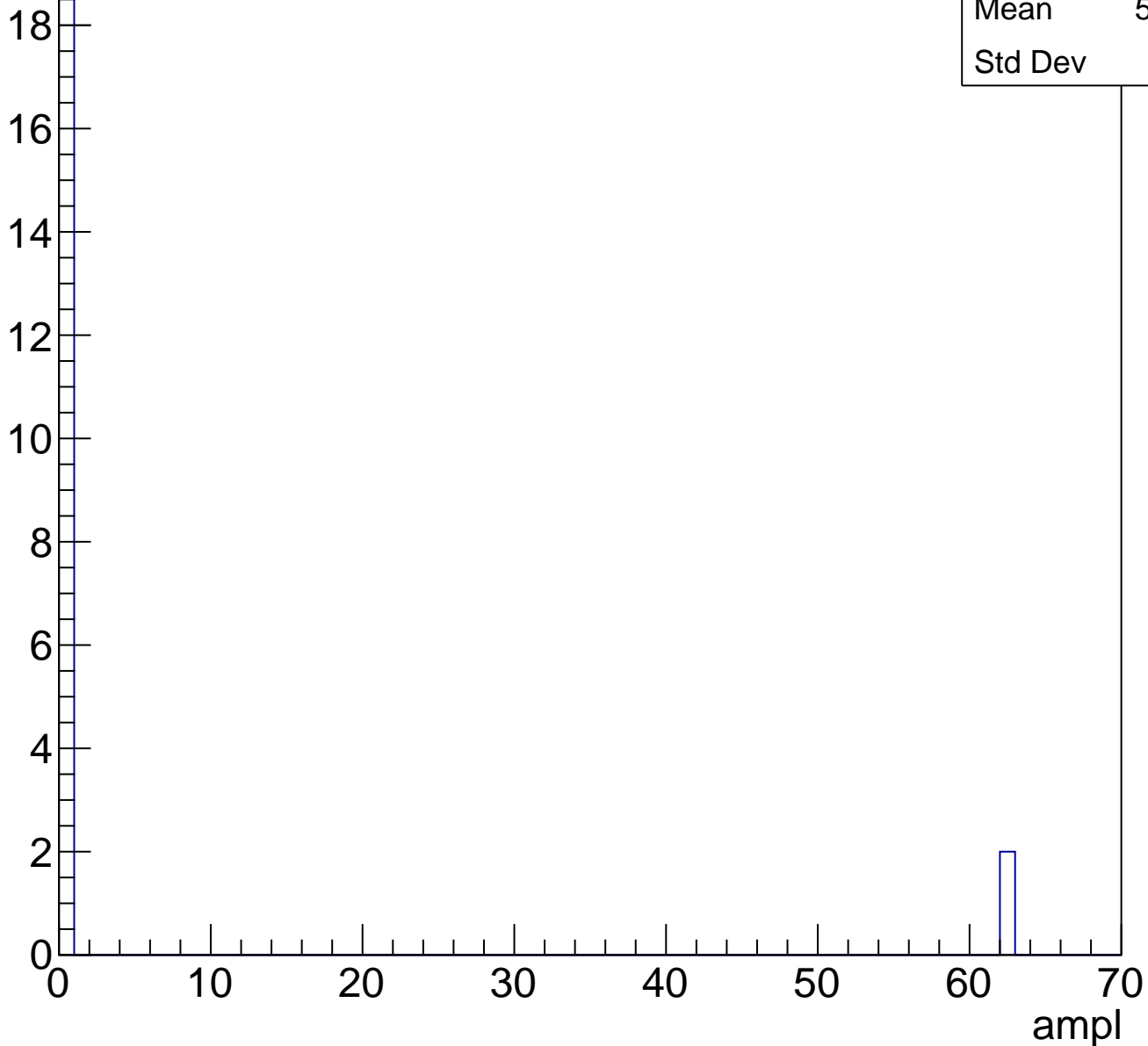


# B1L103S, U3-ch89, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	5.905
Std Dev	18.2

Entry



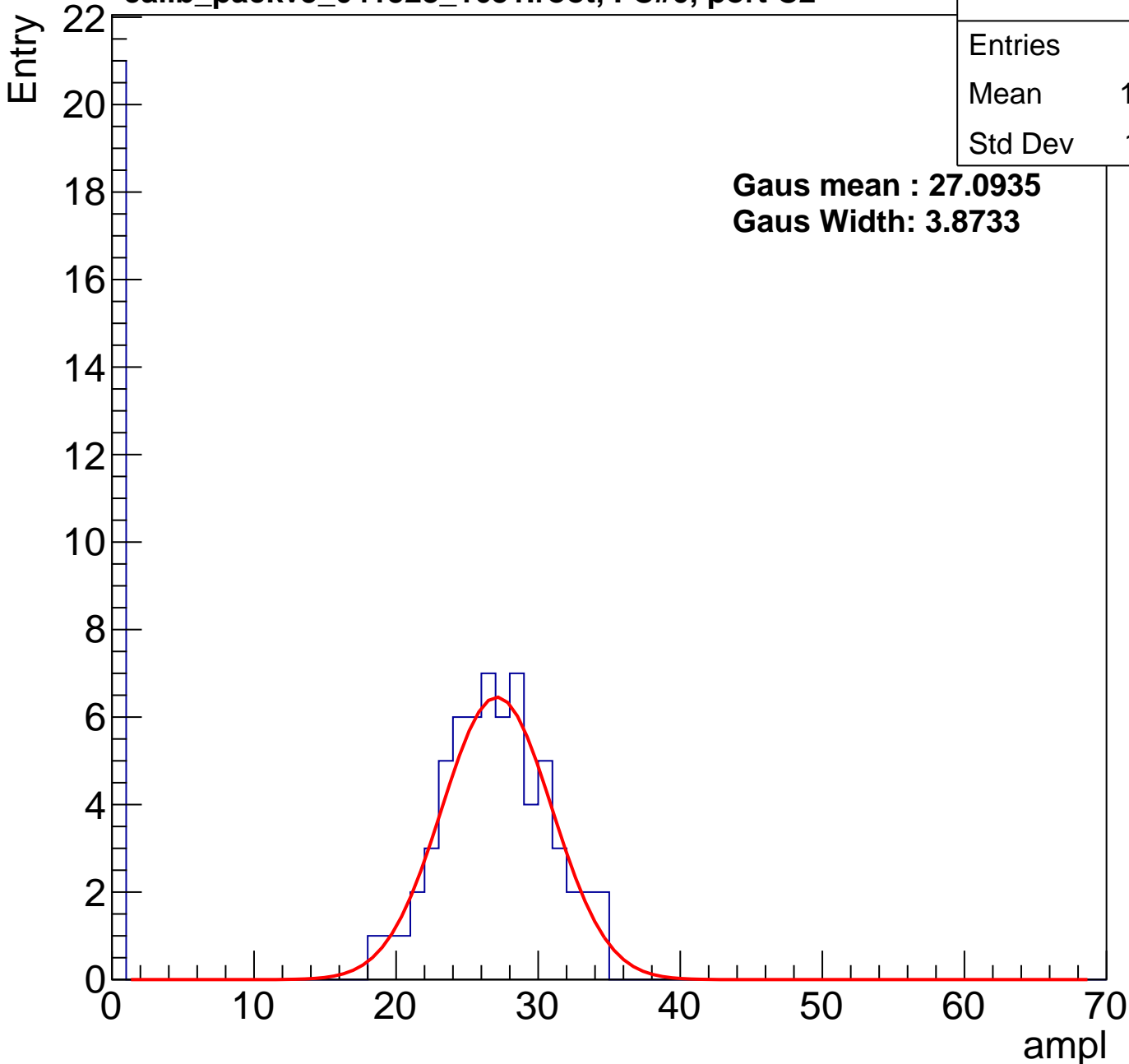
# B1L103S, U3-ch90, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	84
Mean	19.89
Std Dev	11.91

**Gaus mean : 27.0935**

**Gaus Width: 3.8733**



# B1L103S, U3-ch90, adc1

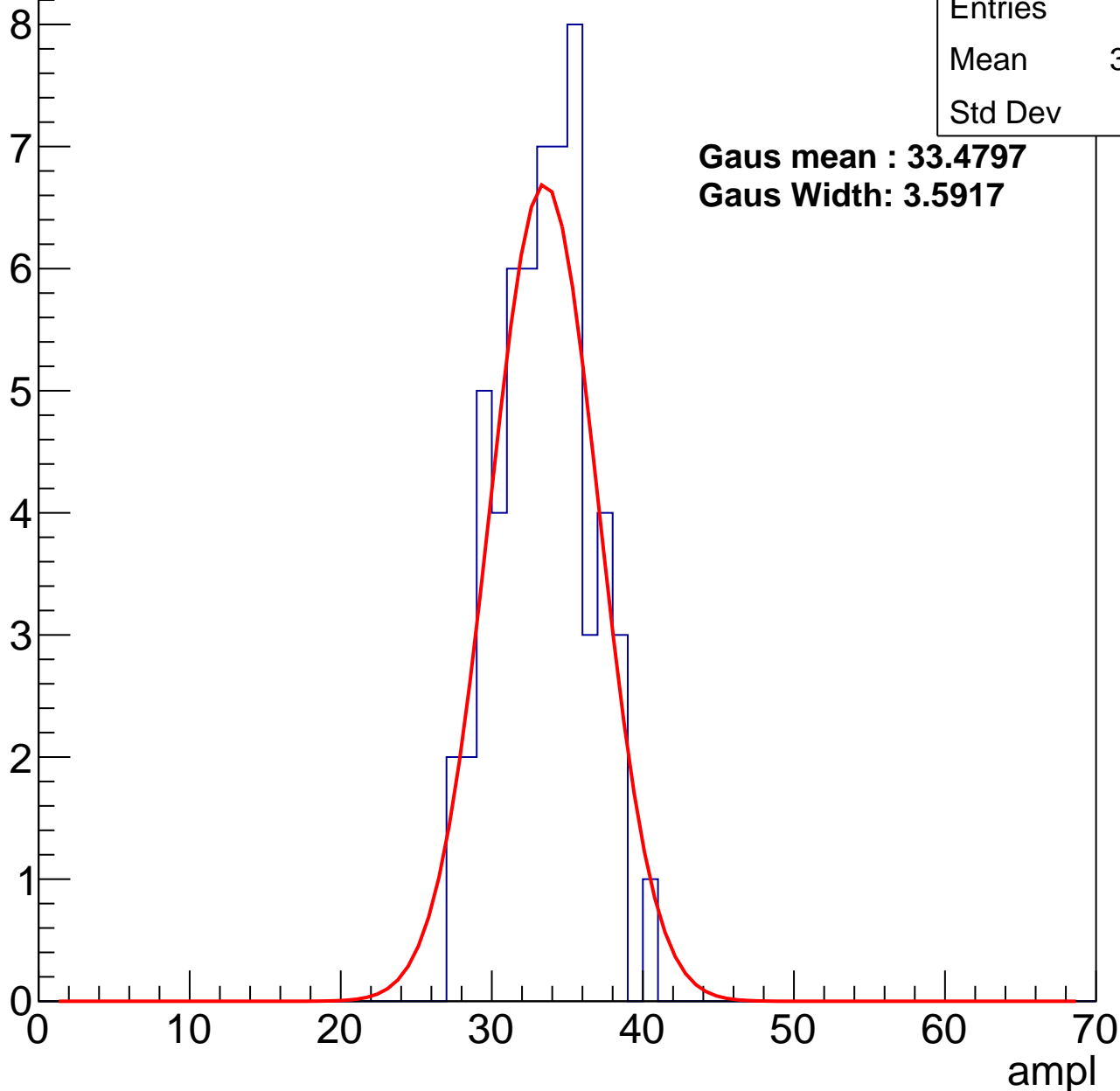
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	32.97
Std Dev	3

**Gaus mean : 33.4797**

**Gaus Width: 3.5917**



# B1L103S, U3-ch90, adc2

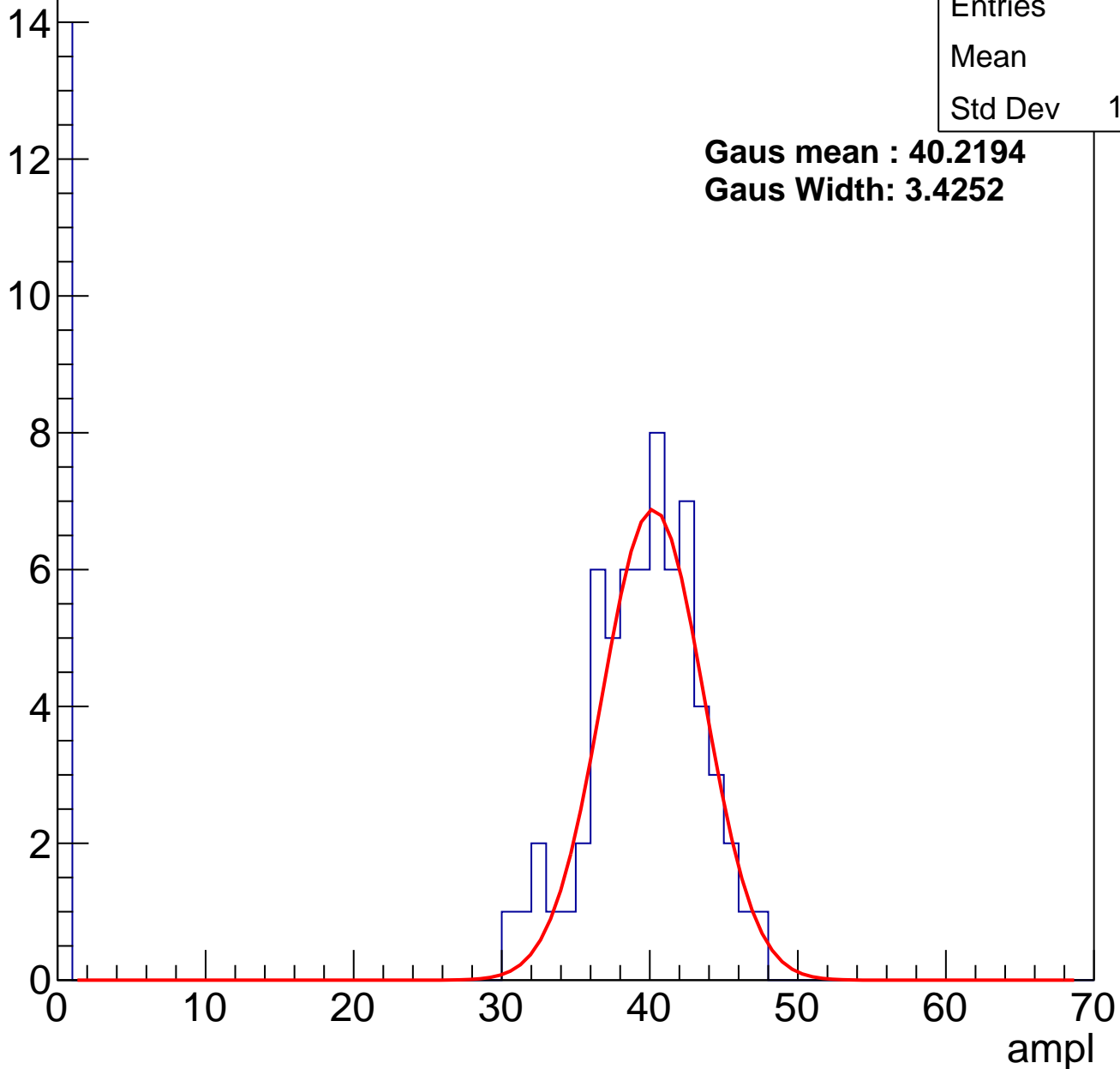
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	77
Mean	32.1
Std Dev	15.49

**Gaus mean : 40.2194**

**Gaus Width: 3.4252**

Entry

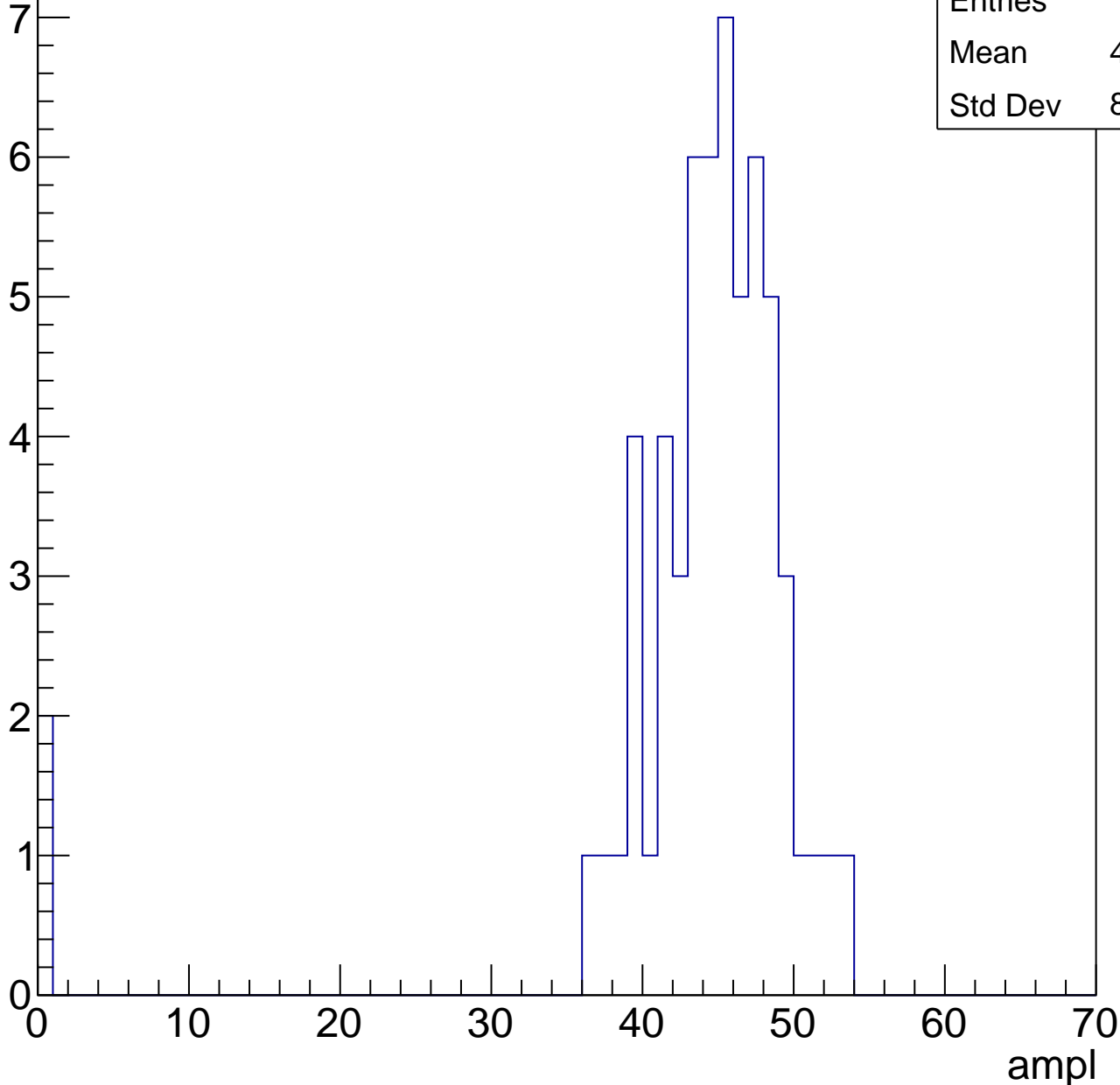


# B1L103S, U3-ch90, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

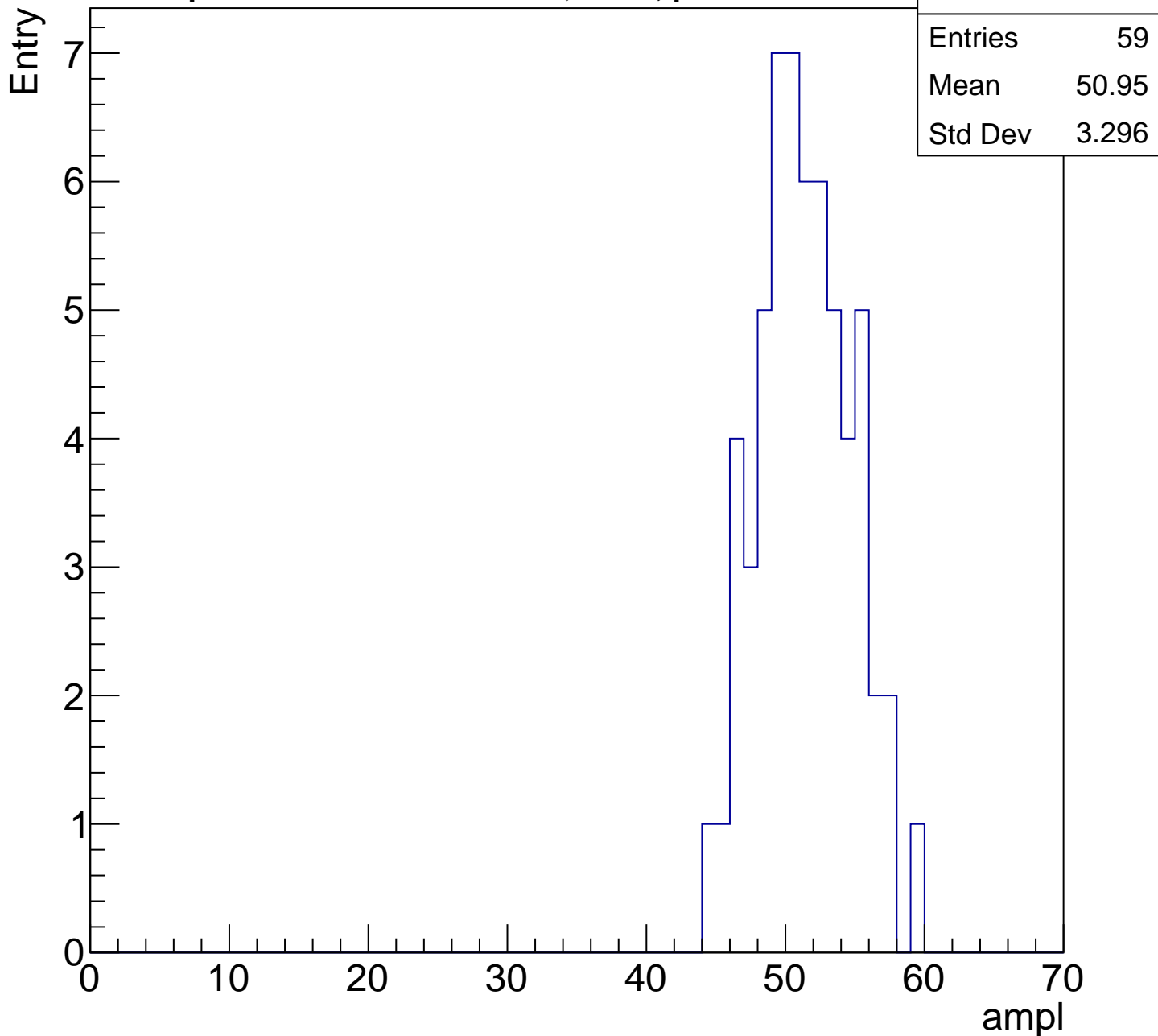
Entry

Entries	59
Mean	43.03
Std Dev	8.832



# B1L103S, U3-ch90, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

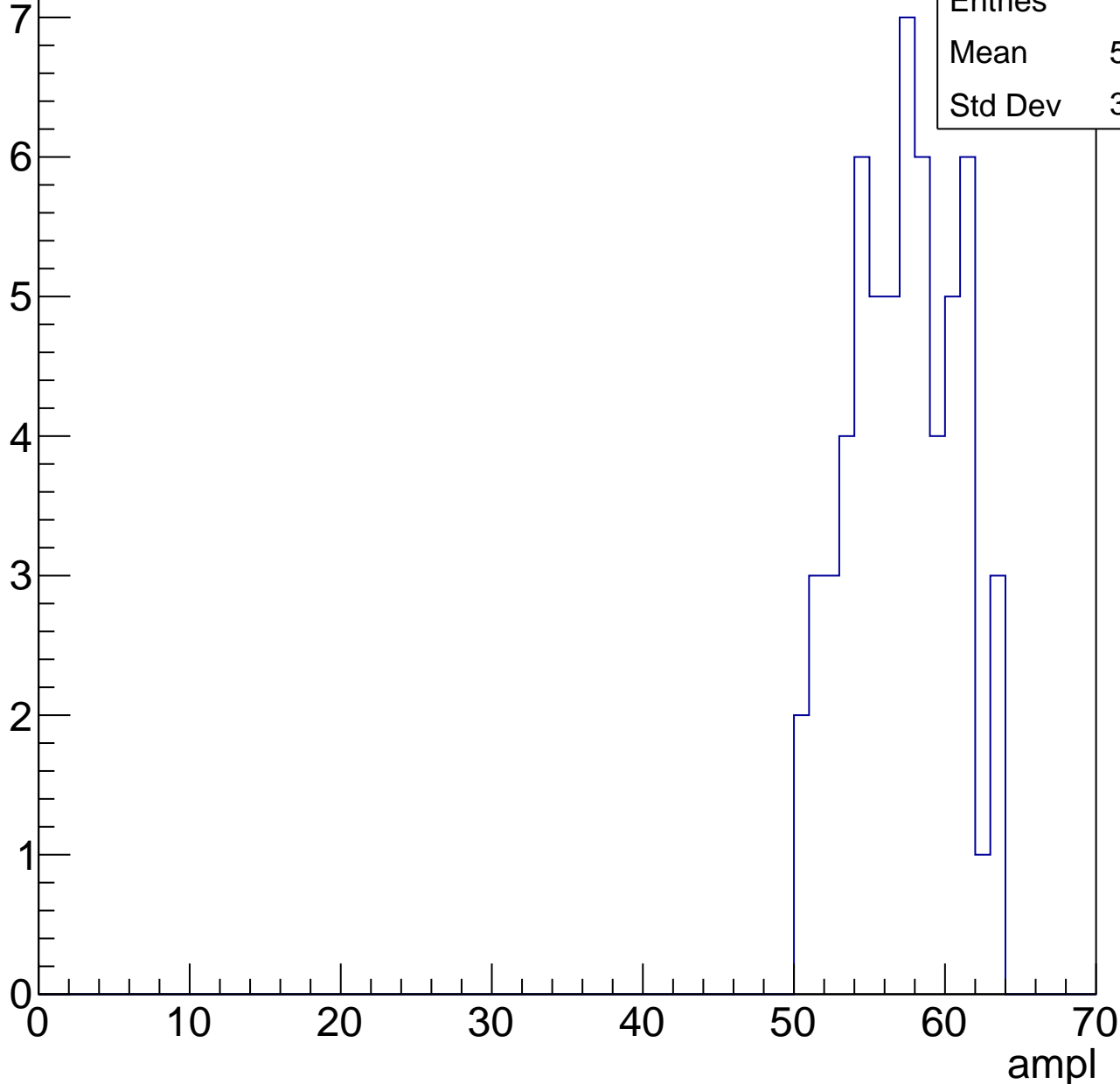


# B1L103S, U3-ch90, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	60
Mean	56.67
Std Dev	3.448

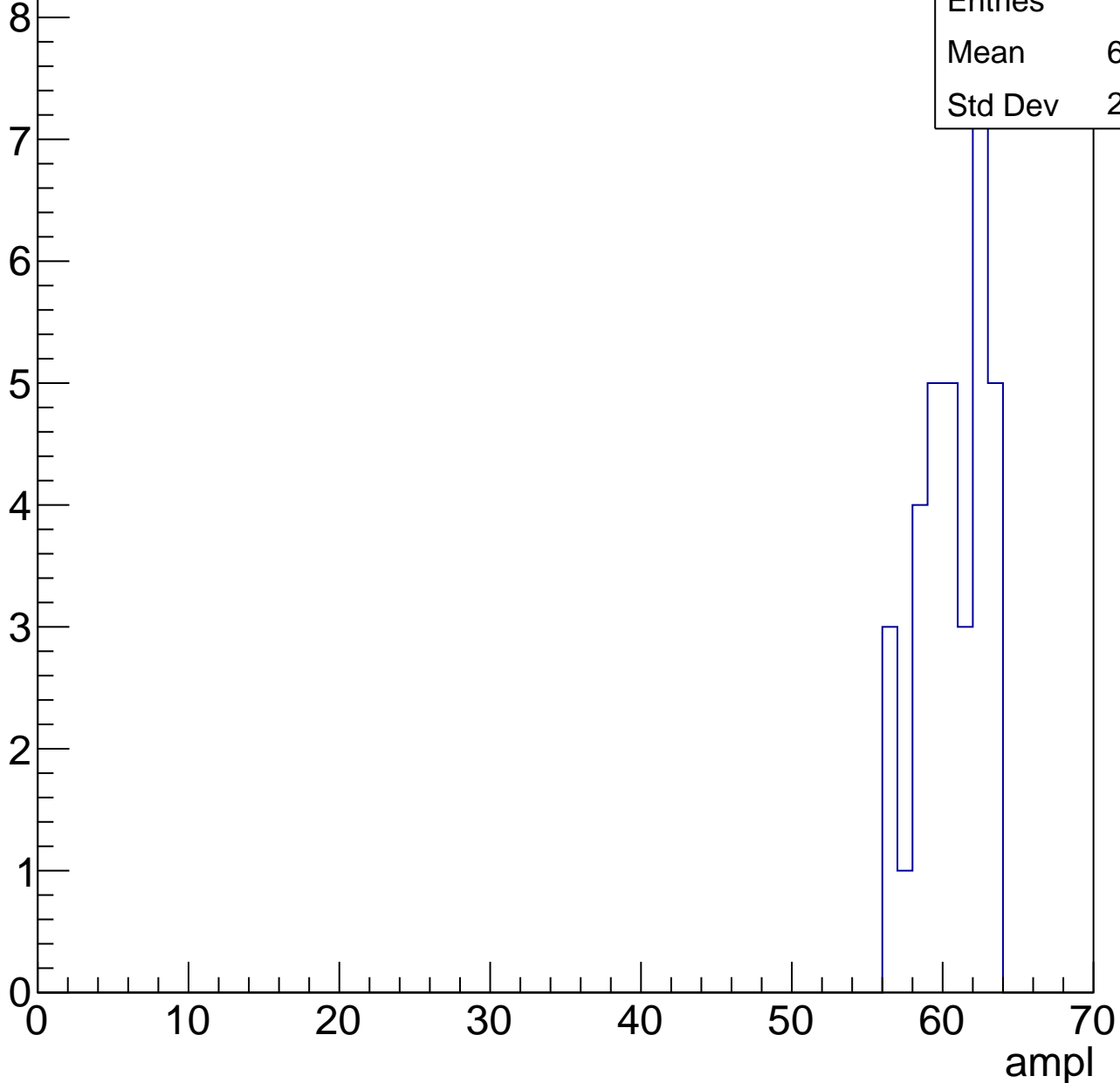


# B1L103S, U3-ch90, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	34
Mean	60.18
Std Dev	2.148





# B1L103S, U3-ch90, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

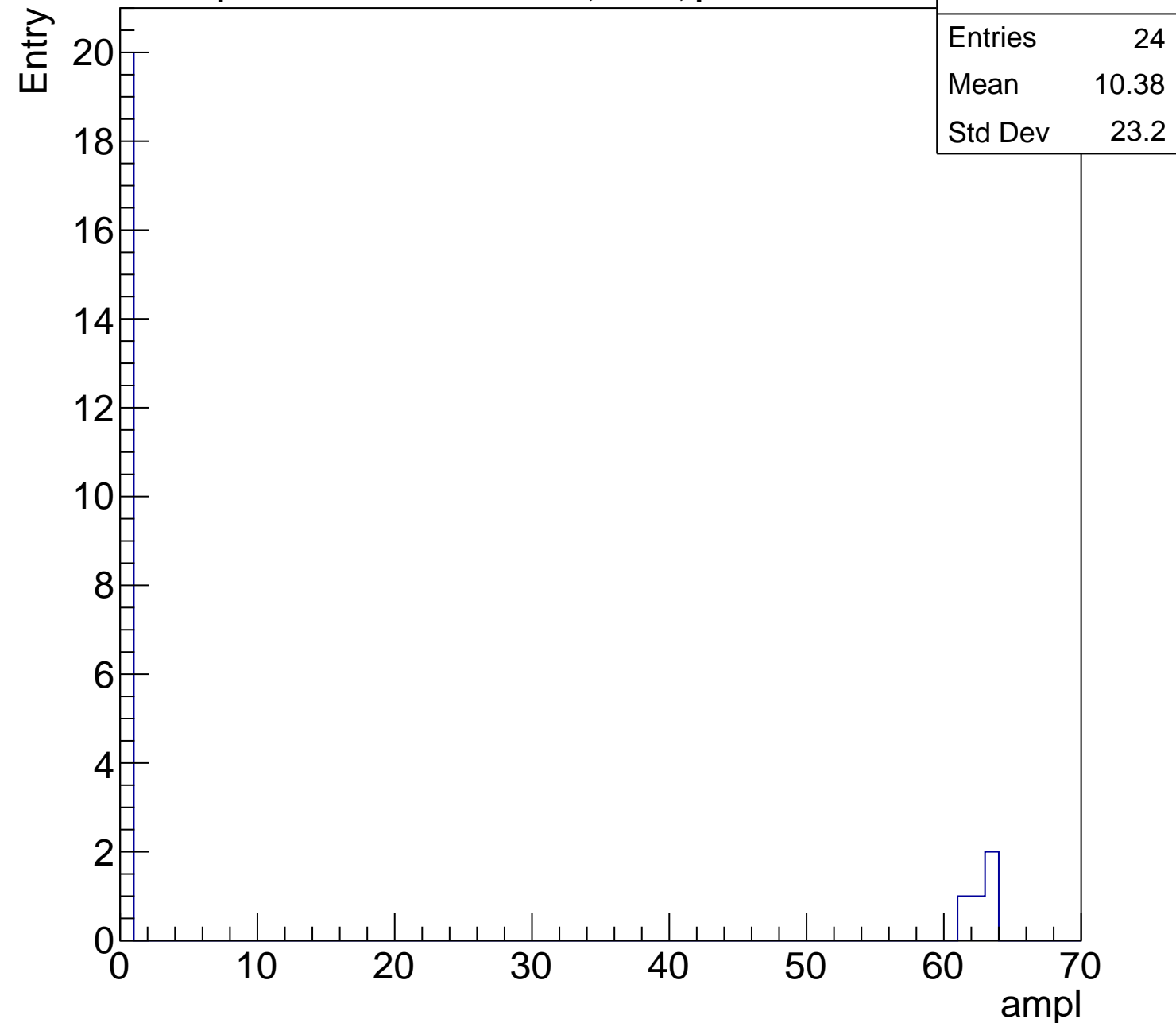
Entries	24
Mean	10.38
Std Dev	23.2

Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U3-ch91, adc0

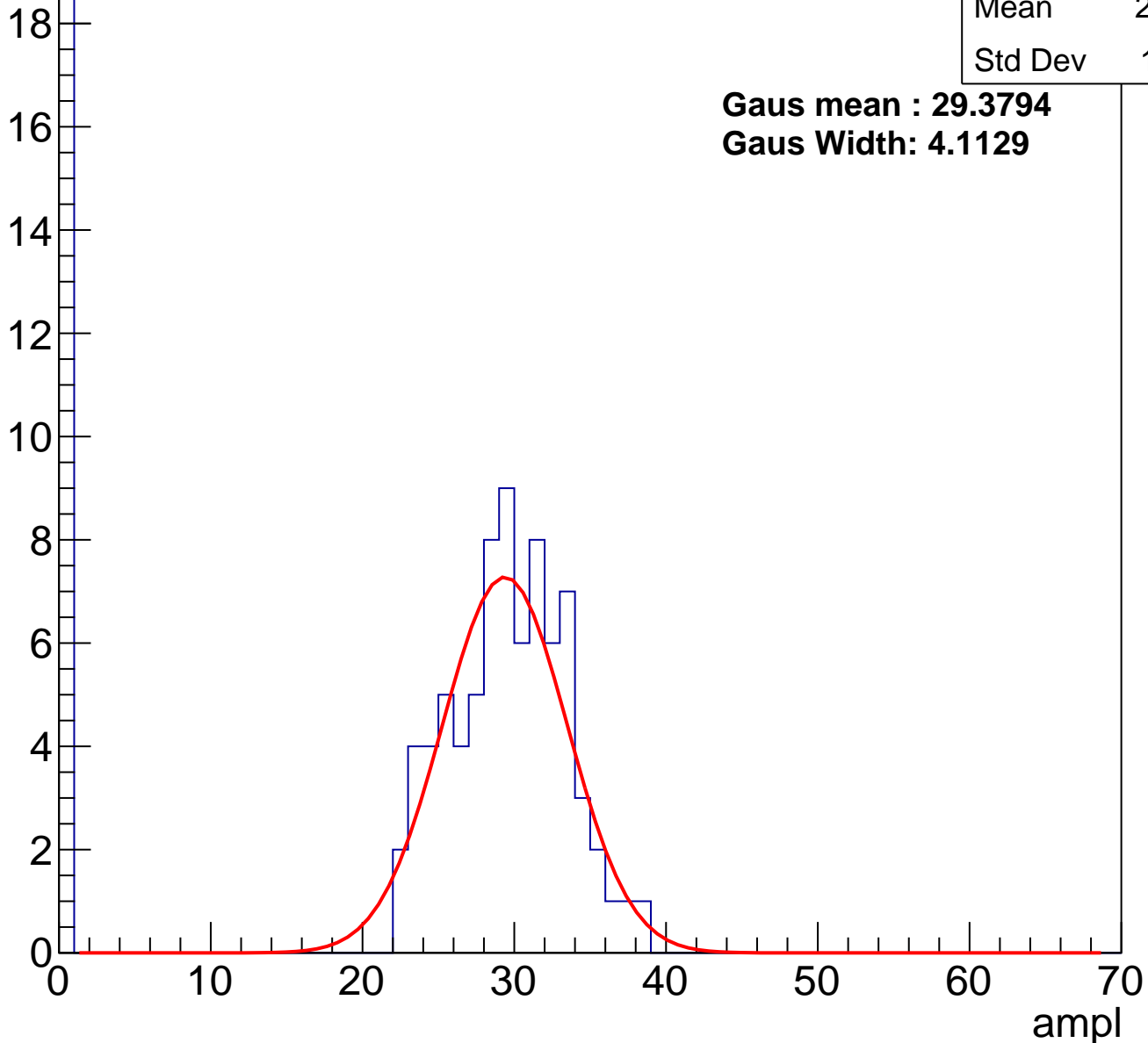
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	95
Mean	23.32
Std Dev	12.11

**Gaus mean : 29.3794**

**Gaus Width: 4.1129**

Entry



# B1L103S, U3-ch91, adc1

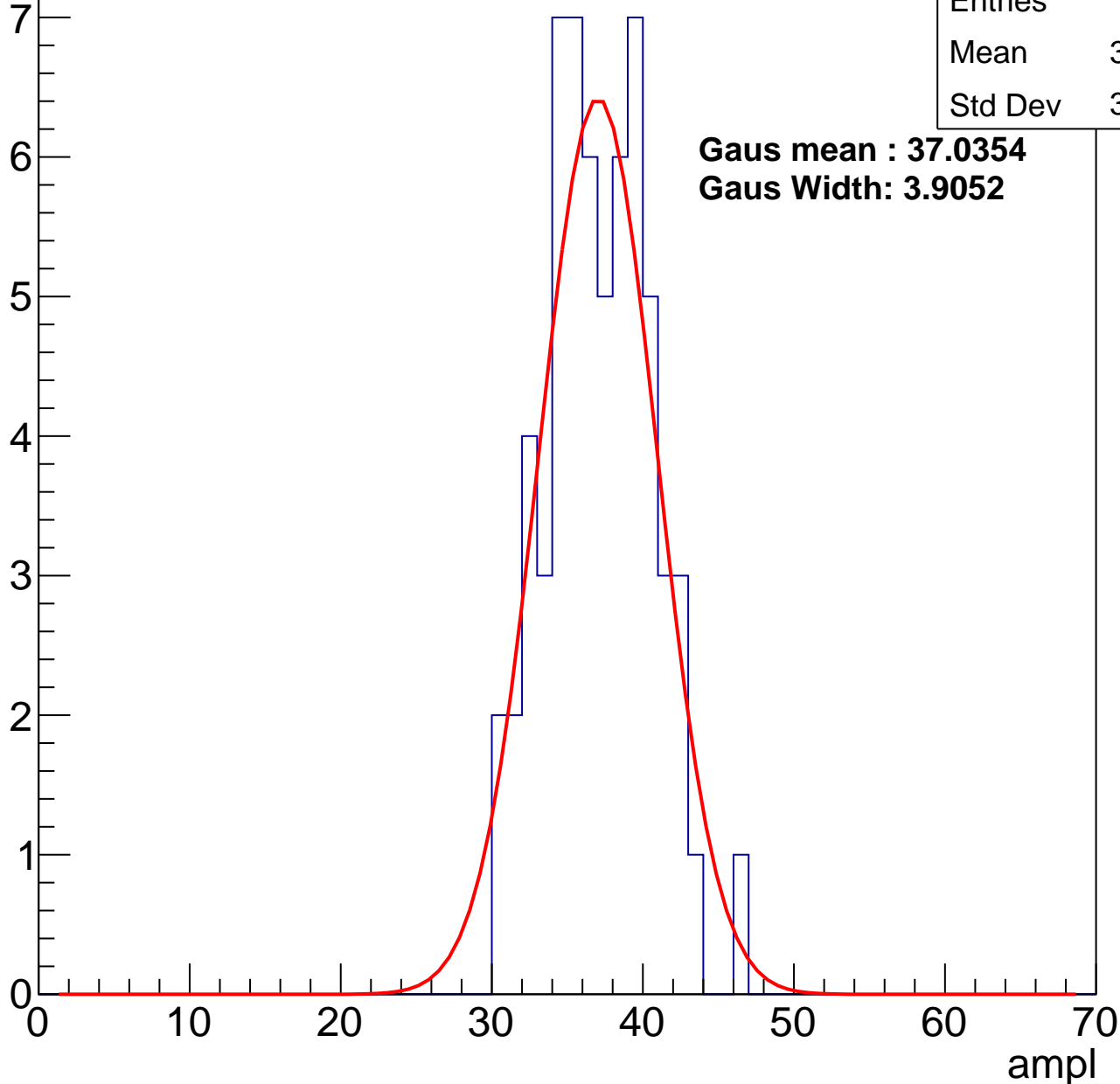
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	36.65
Std Dev	3.422

**Gaus mean : 37.0354**

**Gaus Width: 3.9052**



# B1L103S, U3-ch91, adc2

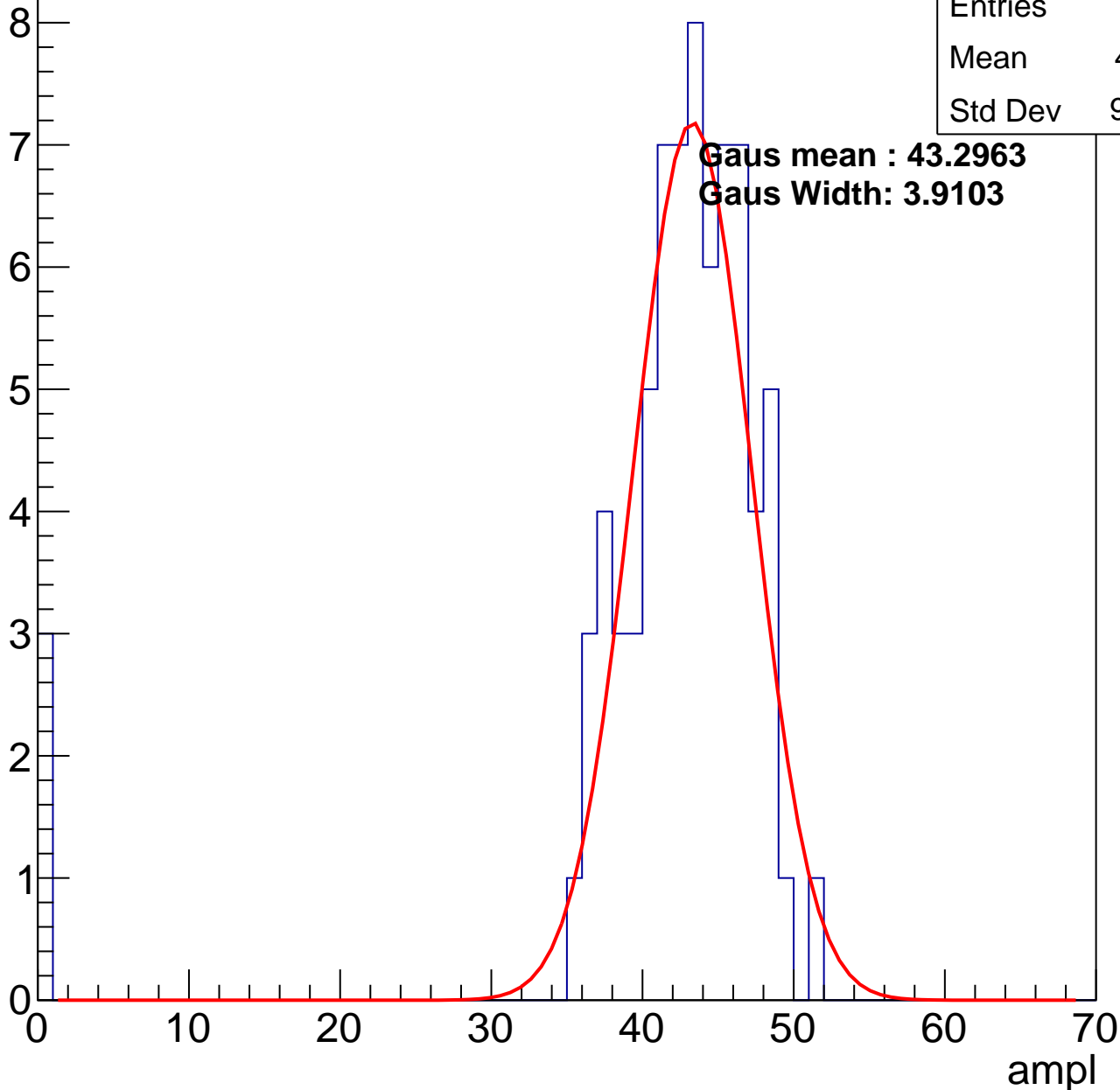
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	75
Mean	41.01
Std Dev	9.088

**Gaus mean : 43.2963**

**Gaus Width: 3.9103**



# B1L103S, U3-ch91, adc3

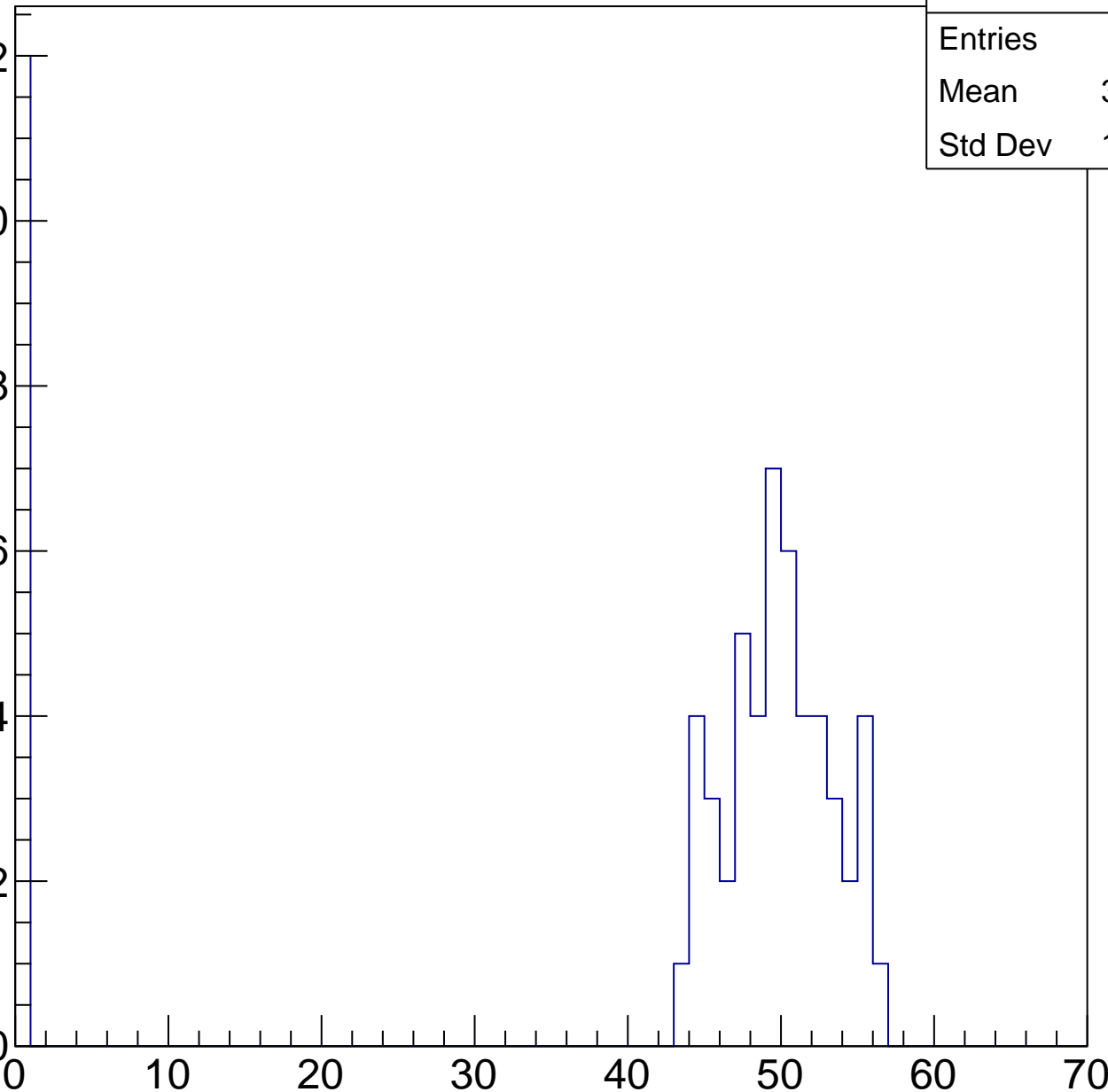
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

12  
10  
8  
6  
4  
2  
0

Entries	62
Mean	39.85
Std Dev	19.76

ampl

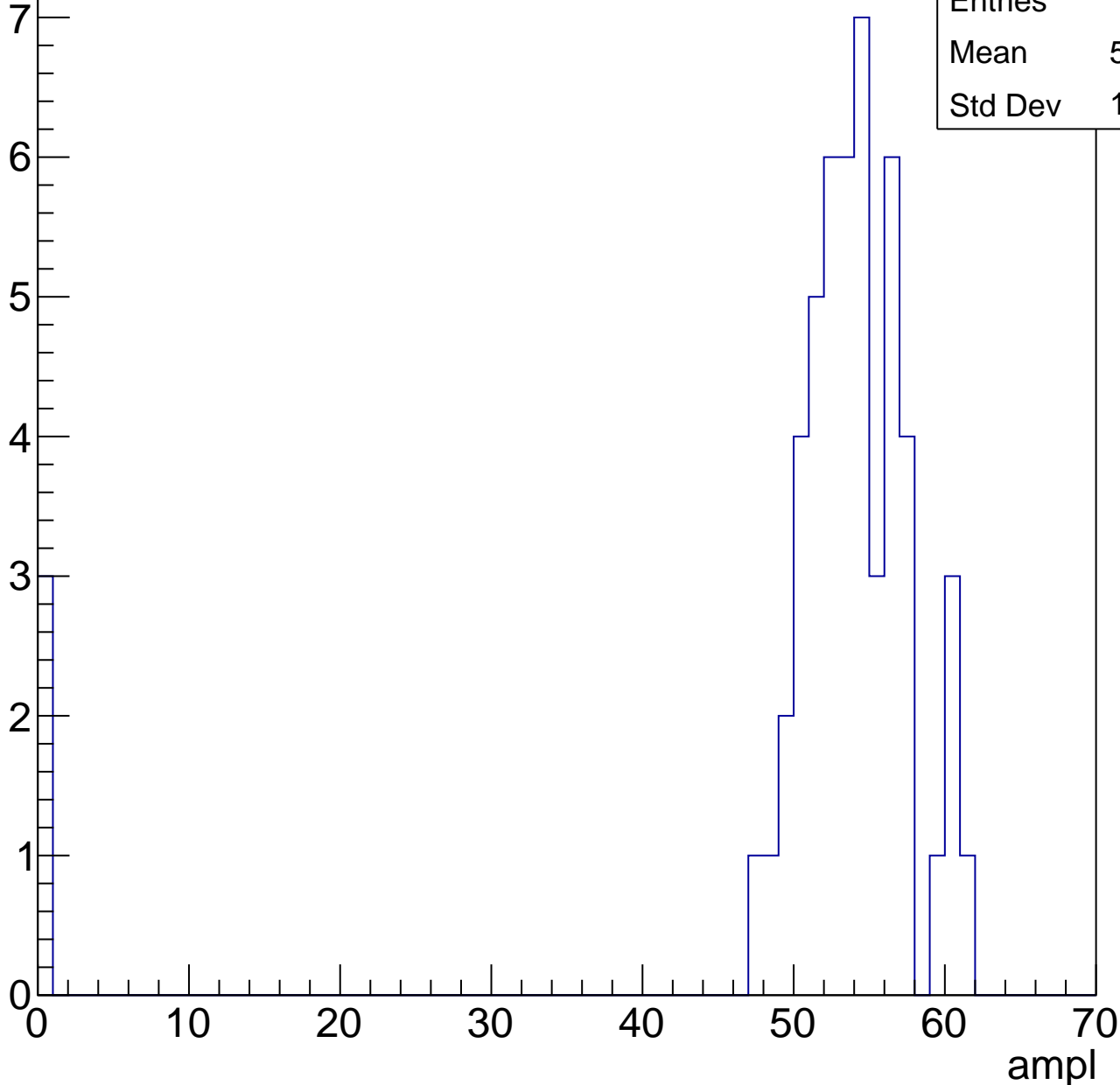


# B1L103S, U3-ch91, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	53
Mean	50.66
Std Dev	12.79



# B1L103S, U3-ch91, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	60
Mean	58.18
Std Dev	7.951

Entry

10

8

6

4

2

0

0

10

20

30

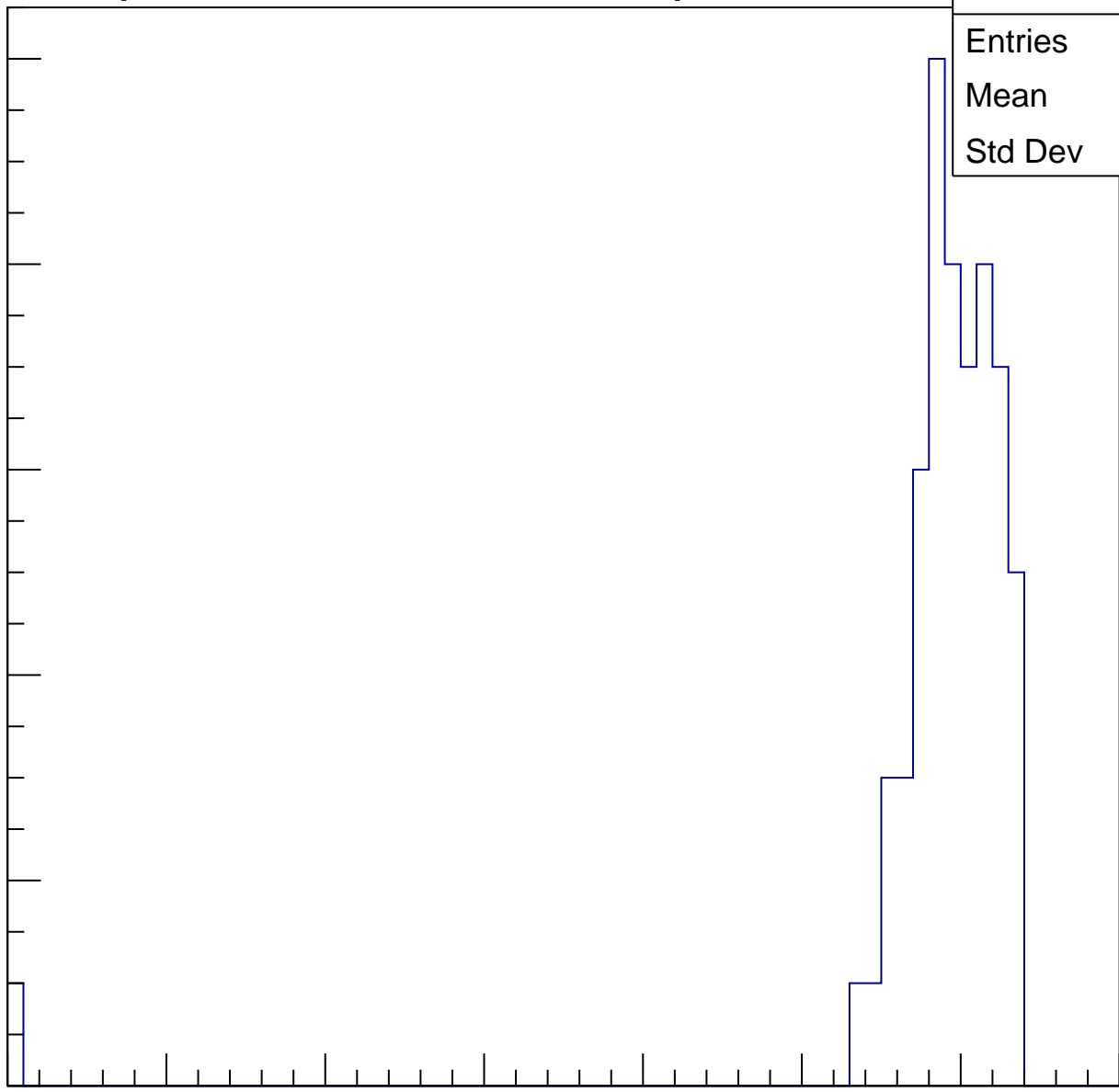
40

50

60

70

ampl

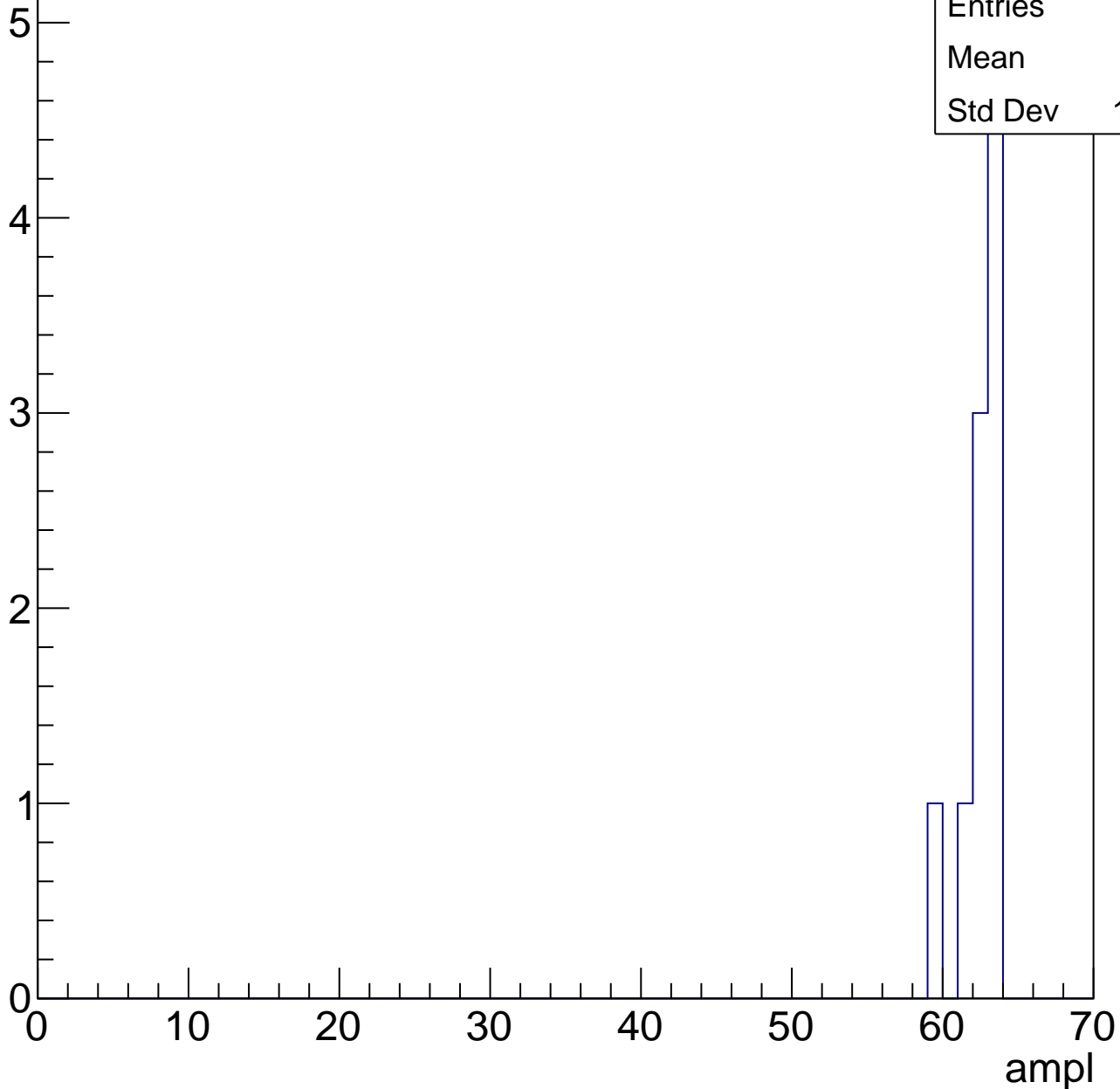


# B1L103S, U3-ch91, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	10
Mean	62.1
Std Dev	1.221





# B1L103S, U3-ch91, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	19
Mean	0
Std Dev	0

# B1L103S, U3-ch92, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	94
Mean	23.41
Std Dev	10.67

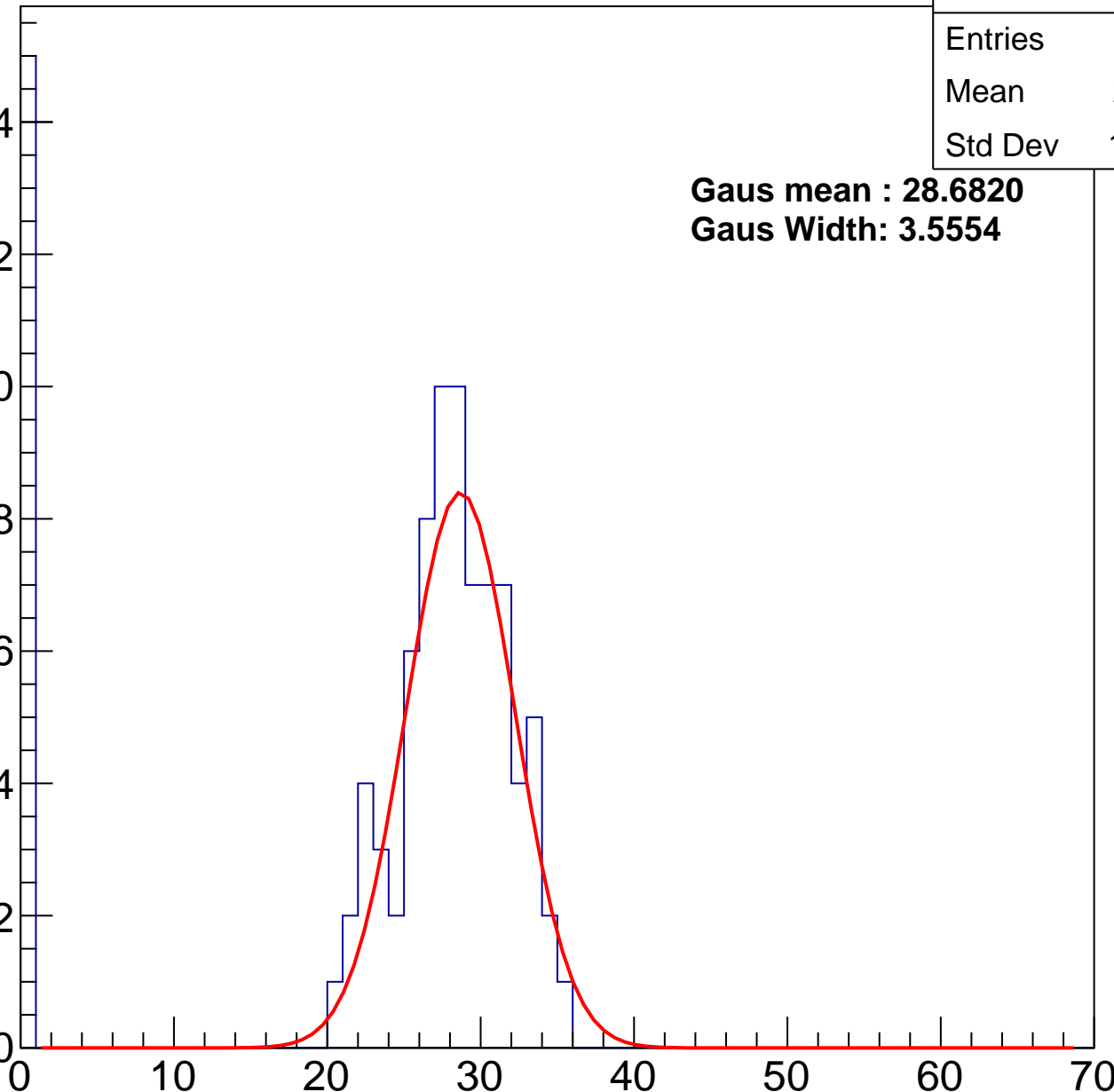
**Gaus mean : 28.6820**

**Gaus Width: 3.5554**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U3-ch92, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	66
Mean	28.26
Std Dev	14.24

**Gaus mean : 35.3698**

**Gaus Width: 2.9760**

Entry

12

10

8

6

4

2

0

0

10

20

30

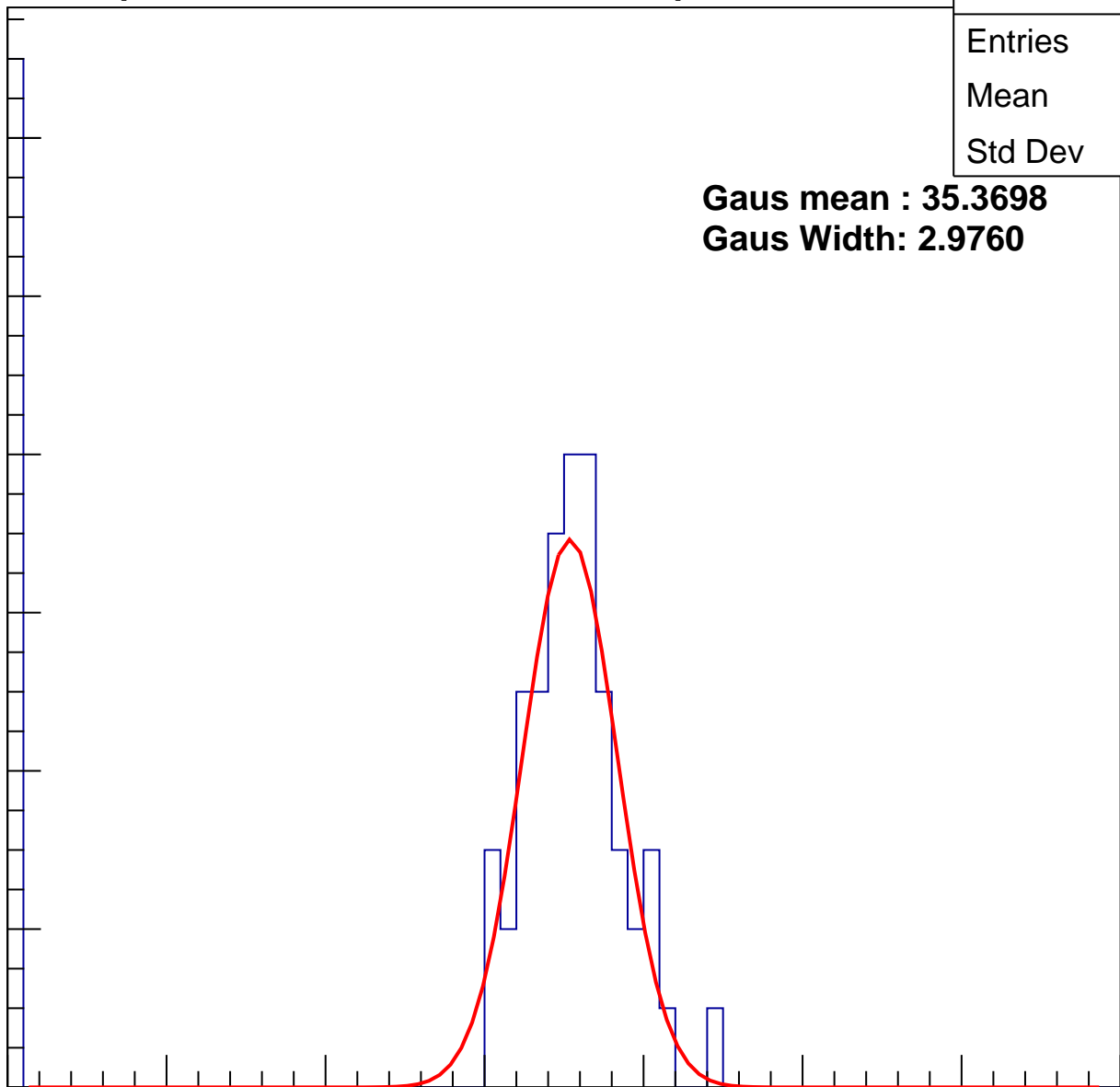
40

50

60

70

ampl



# B1L103S, U3-ch92, adc2

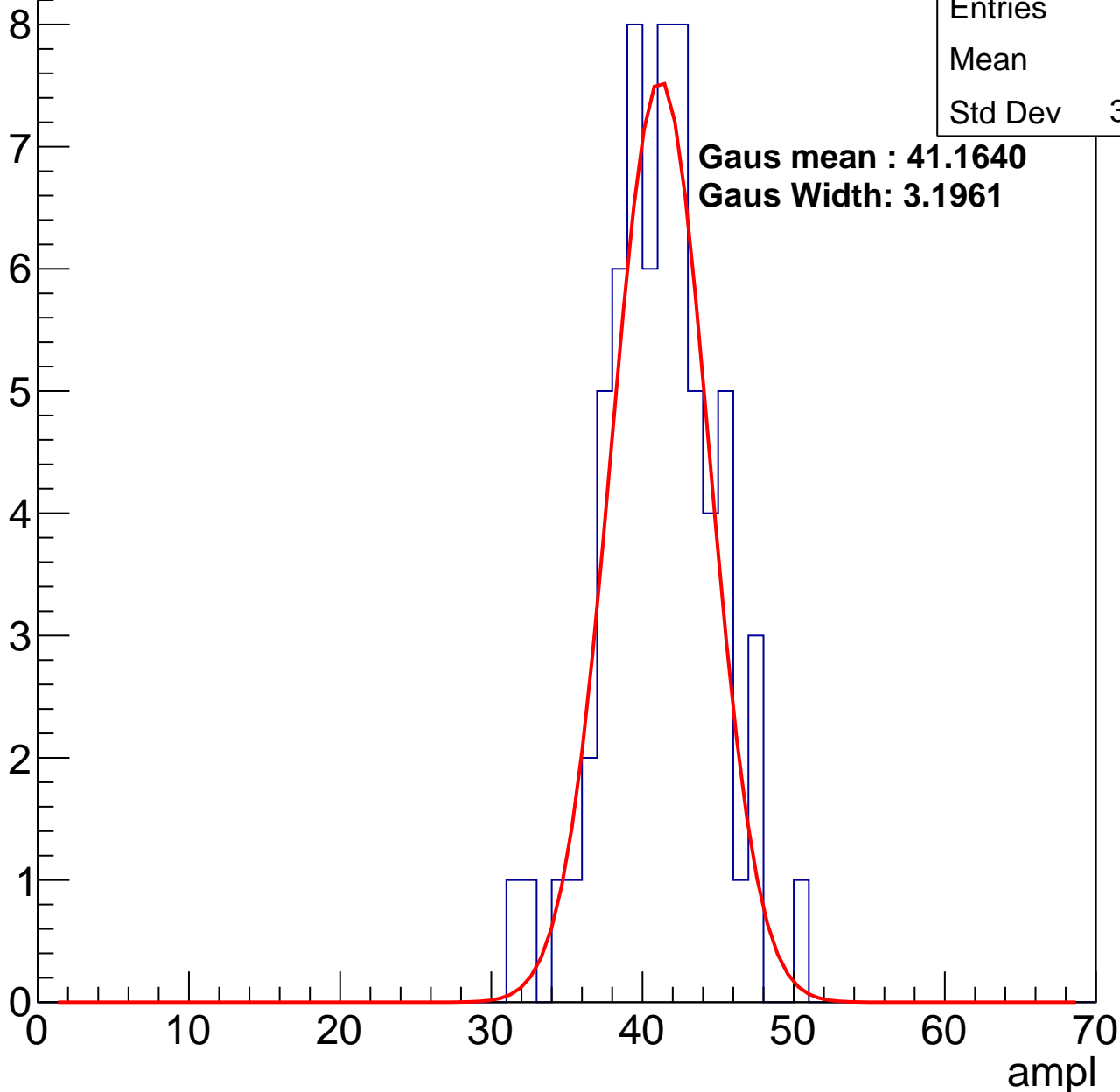
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	40.7
Std Dev	3.567

**Gaus mean : 41.1640**

**Gaus Width: 3.1961**

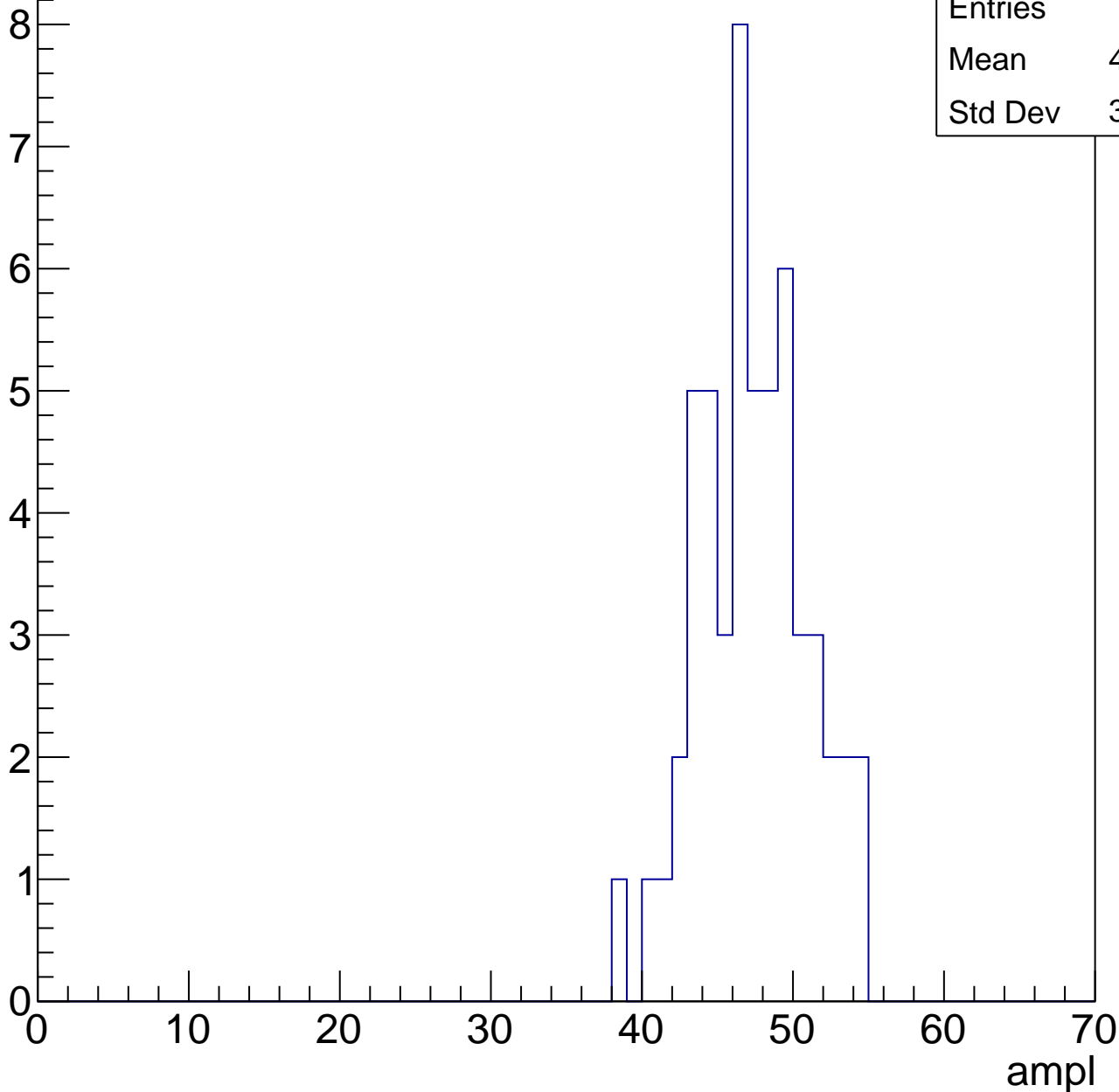


# B1L103S, U3-ch92, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	54
Mean	46.87
Std Dev	3.559

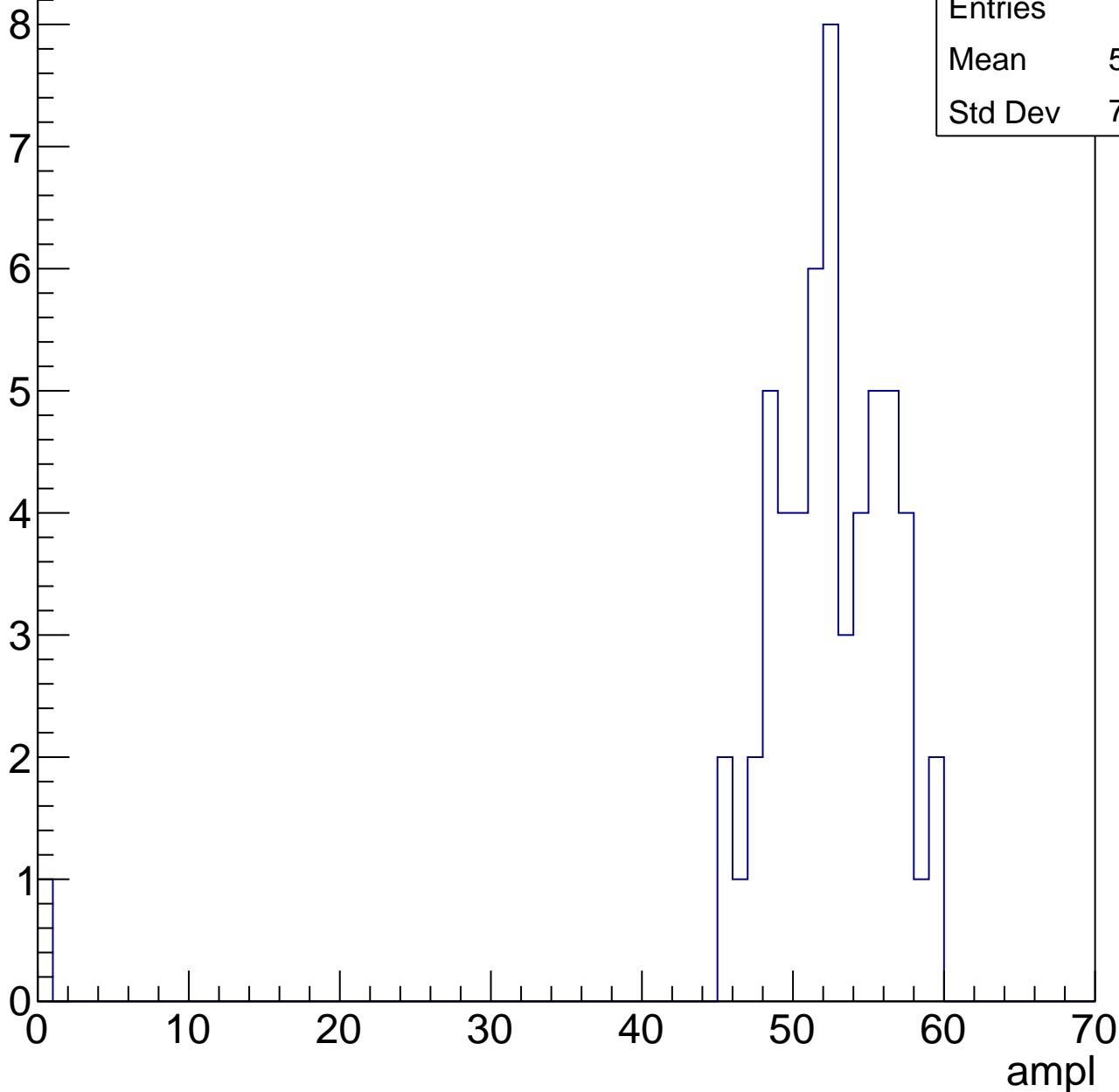


# B1L103S, U3-ch92, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	57
Mean	51.26
Std Dev	7.693



# B1L103S, U3-ch92, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

7

6

5

4

3

2

1

0

0

10

20

30

40

50

60

70

ampl

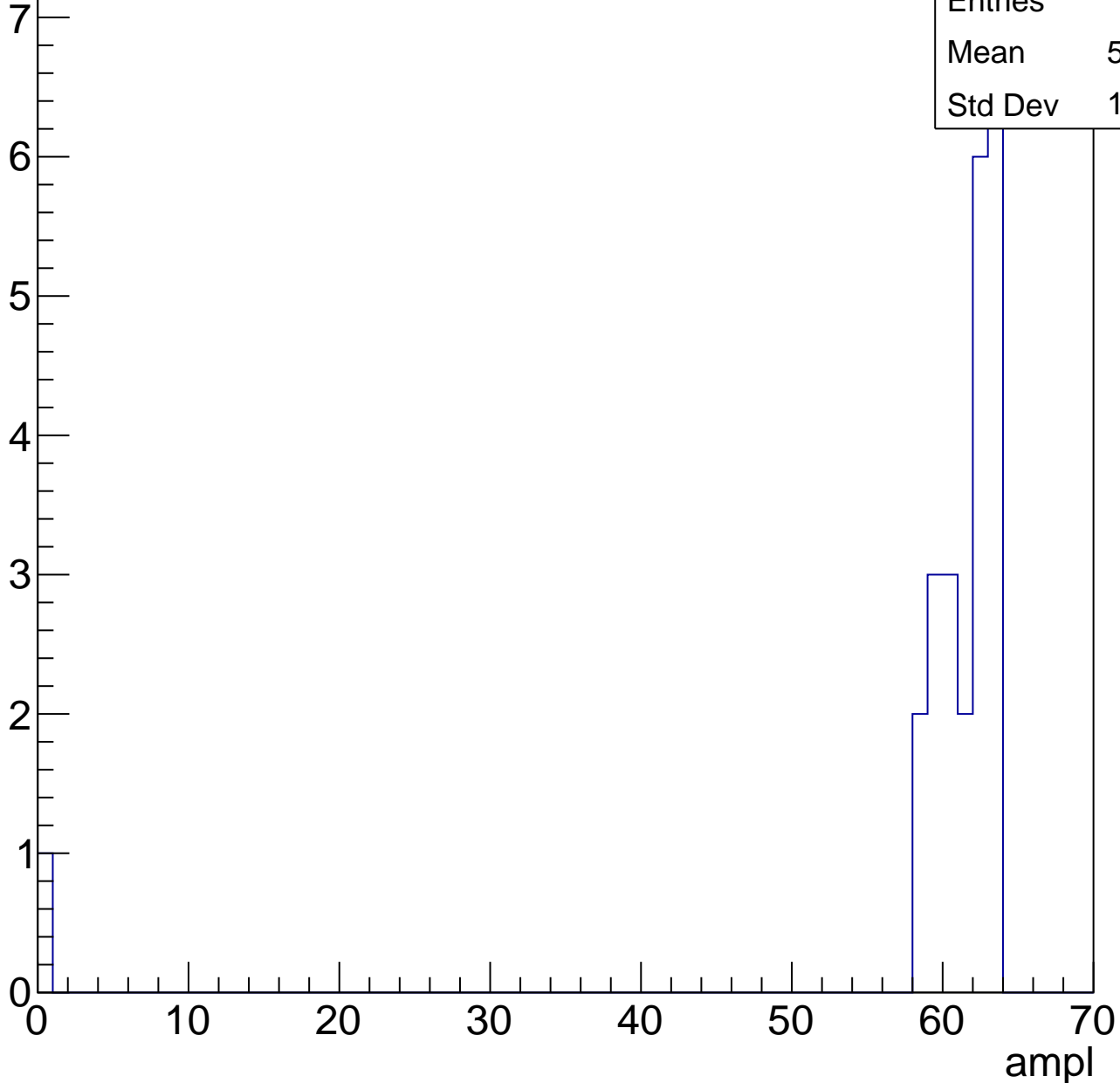
Entries	61
Mean	57.61
Std Dev	3.296

# B1L103S, U3-ch92, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	24
Mean	58.67
Std Dev	12.34





# B1L103S, U3-ch92, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.05
Std Dev	13.29

Entry



# B1L103S, U3-ch93, adc0

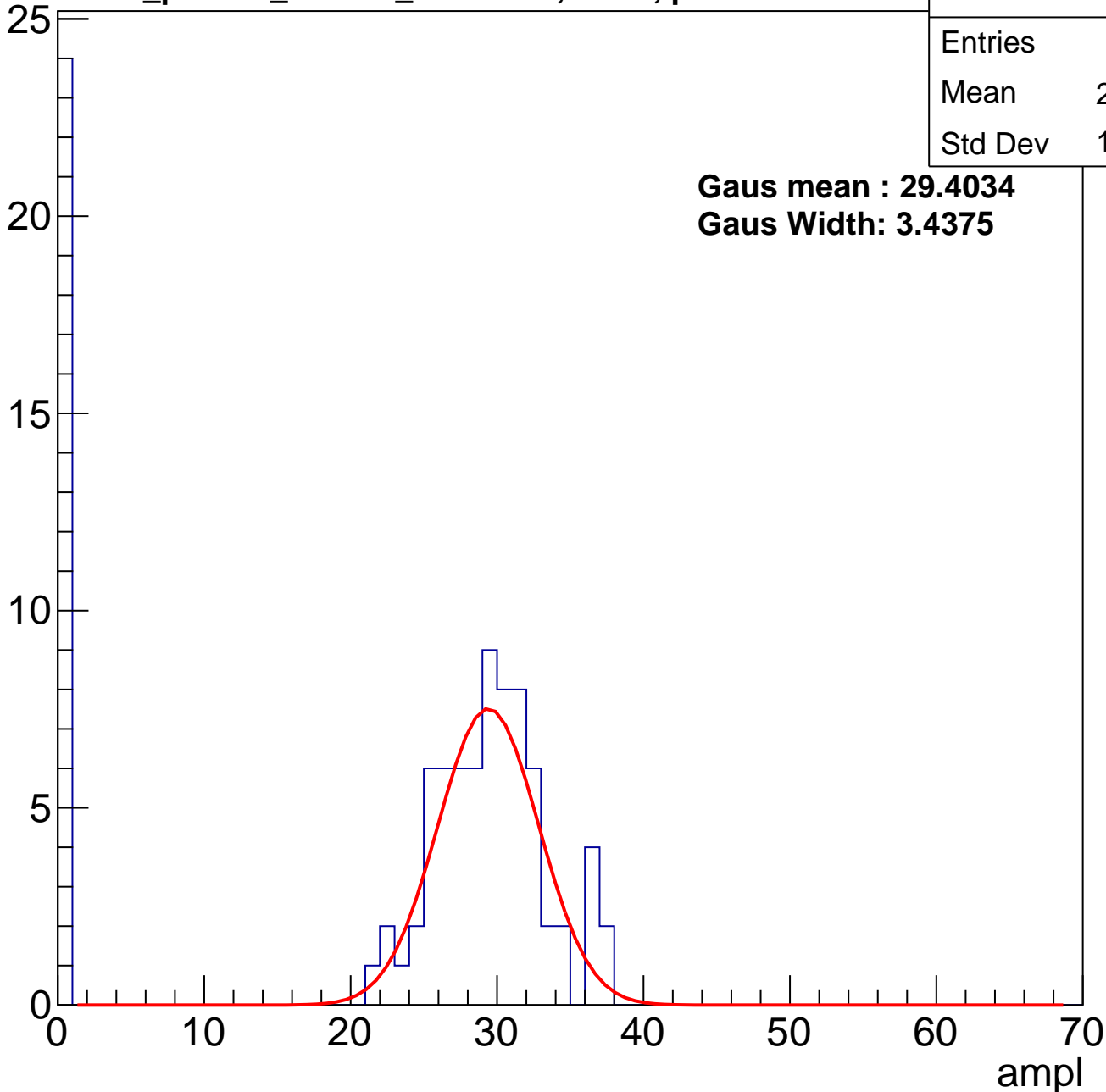
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	95
Mean	21.74
Std Dev	13.02

**Gaus mean : 29.4034**

**Gaus Width: 3.4375**

Entry



# B1L103S, U3-ch93, adc1

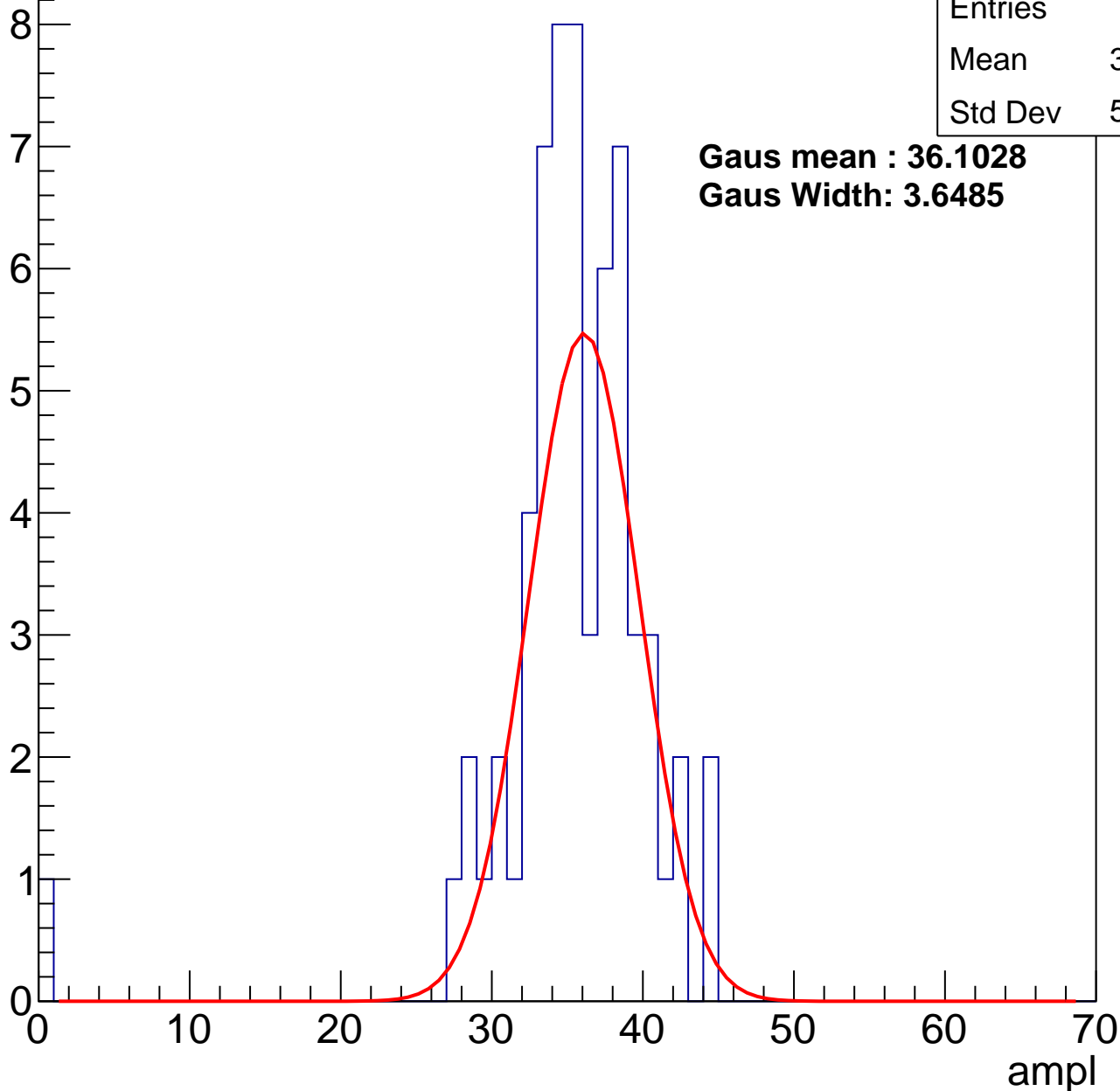
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	34.84
Std Dev	5.776

**Gaus mean : 36.1028**

**Gaus Width: 3.6485**



# B1L103S, U3-ch93, adc2

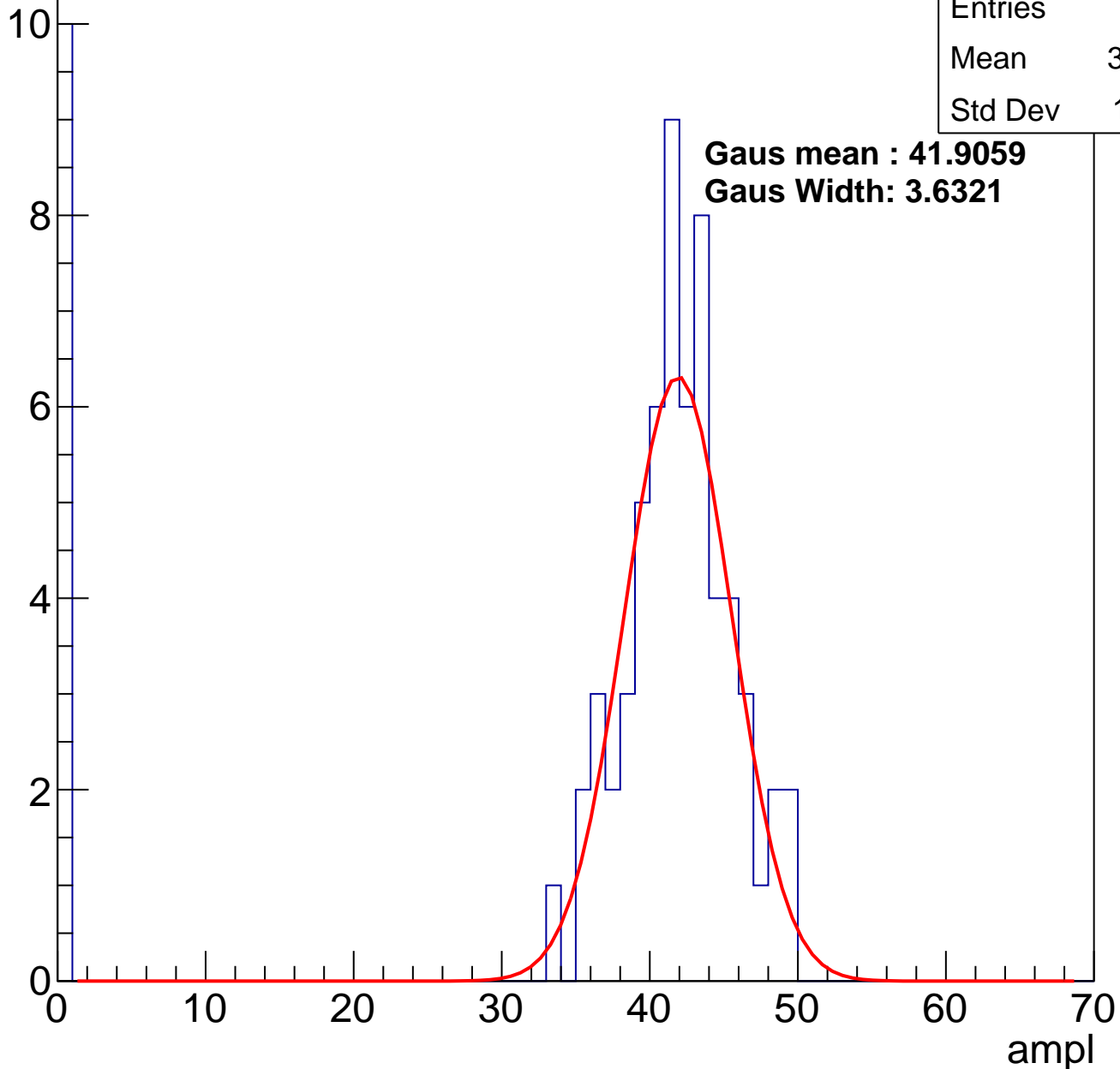
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	71
Mean	35.69
Std Dev	14.81

**Gaus mean : 41.9059**

**Gaus Width: 3.6321**

Entry

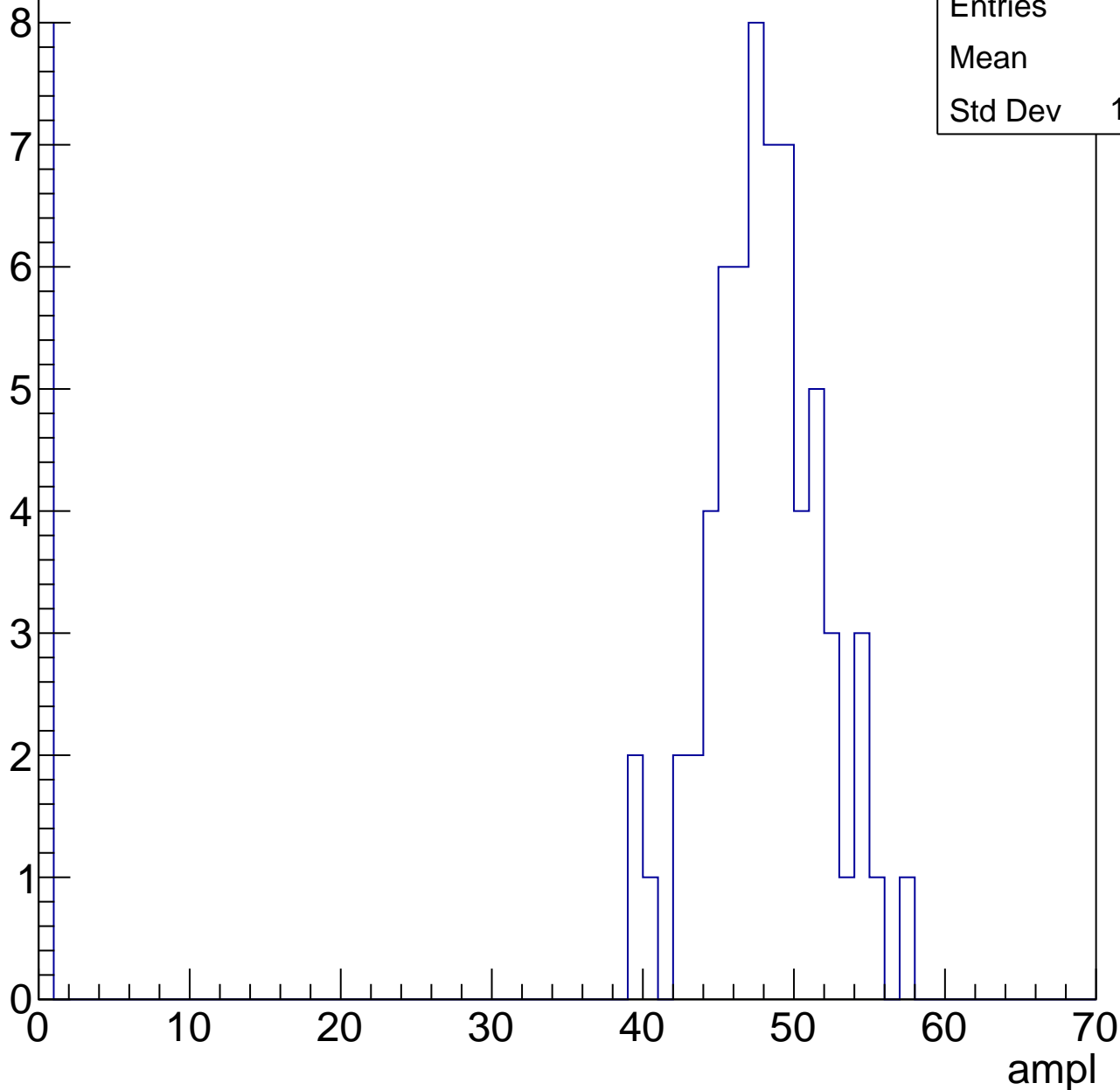


# B1L103S, U3-ch93, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

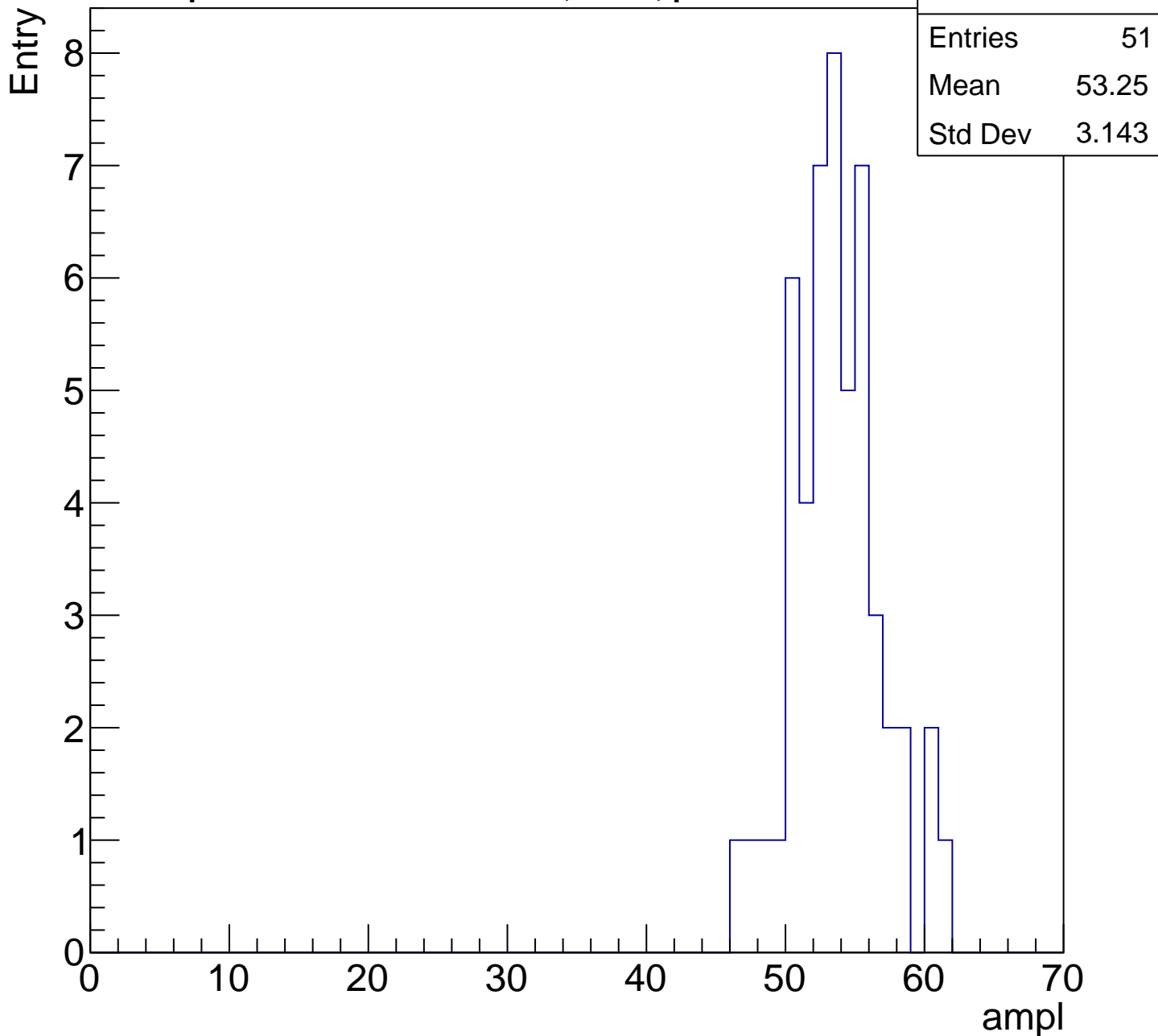
Entry

Entries	71
Mean	42.3
Std Dev	15.47



# B1L103S, U3-ch93, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

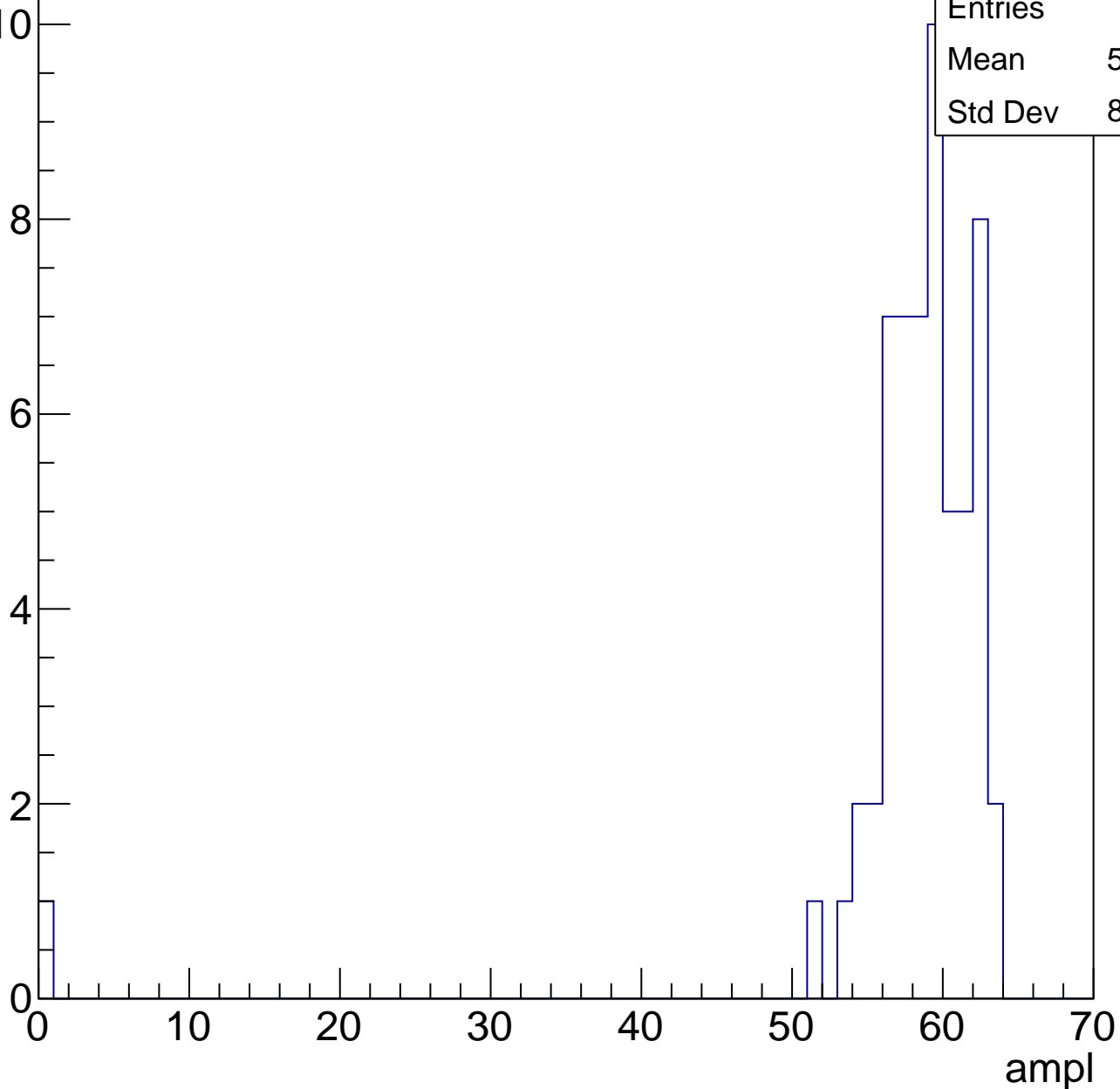


# B1L103S, U3-ch93, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	57.52
Std Dev	8.054

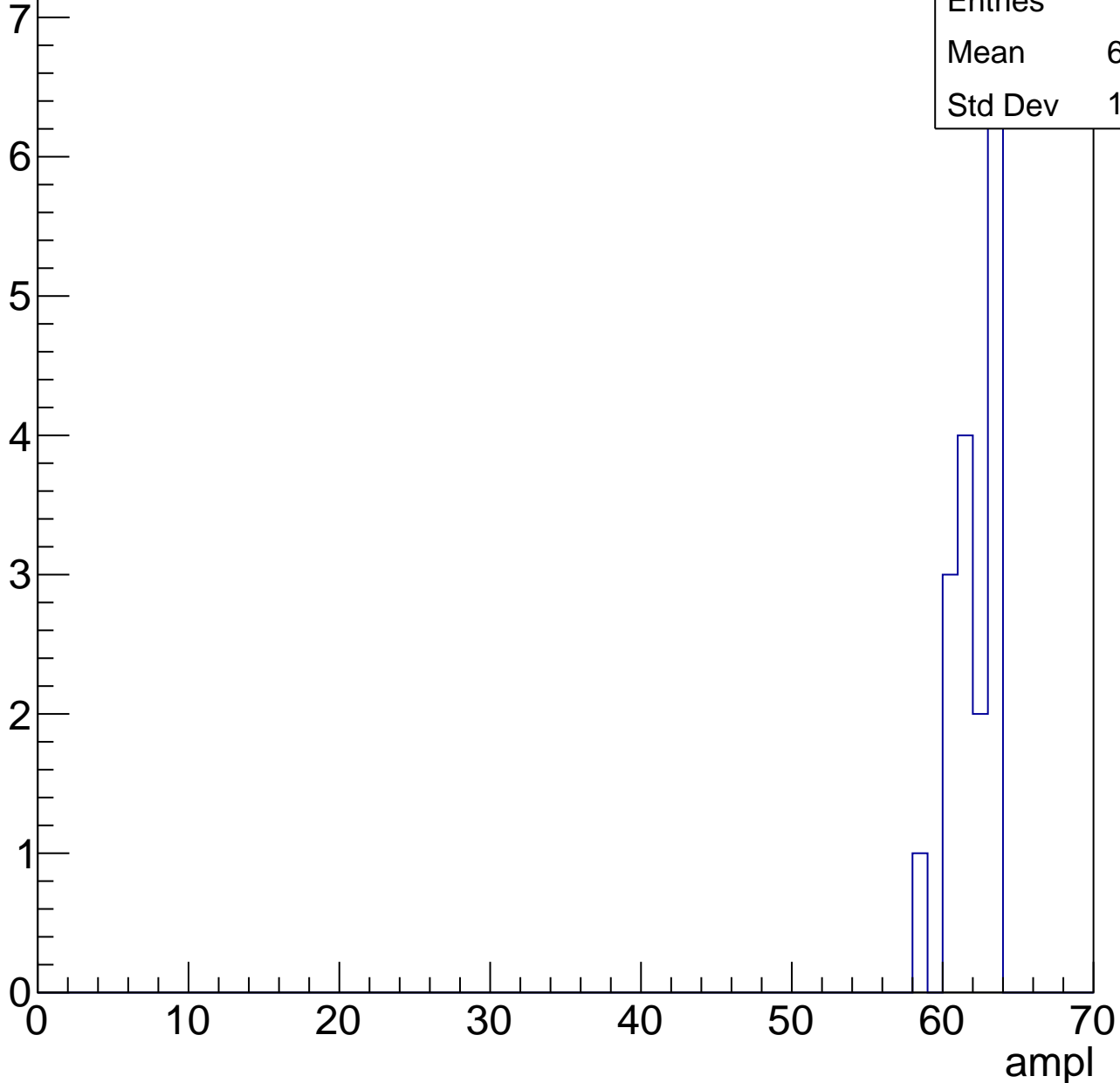


# B1L103S, U3-ch93, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	17
Mean	61.59
Std Dev	1.458





# B1L103S, U3-ch93, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



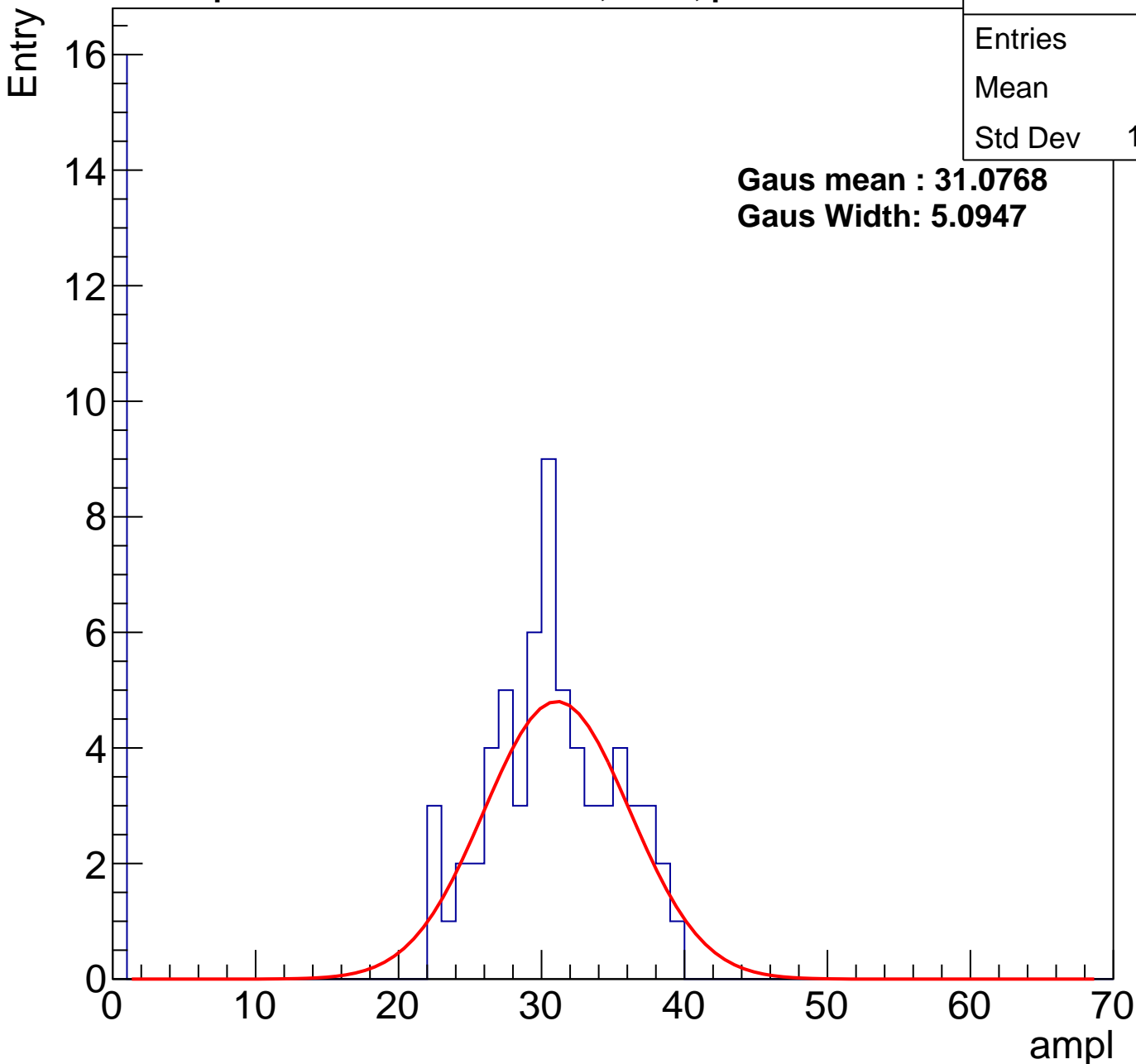
# B1L103S, U3-ch94, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	79
Mean	24.2
Std Dev	12.78

**Gaus mean : 31.0768**

**Gaus Width: 5.0947**



# B1L103S, U3-ch94, adc1

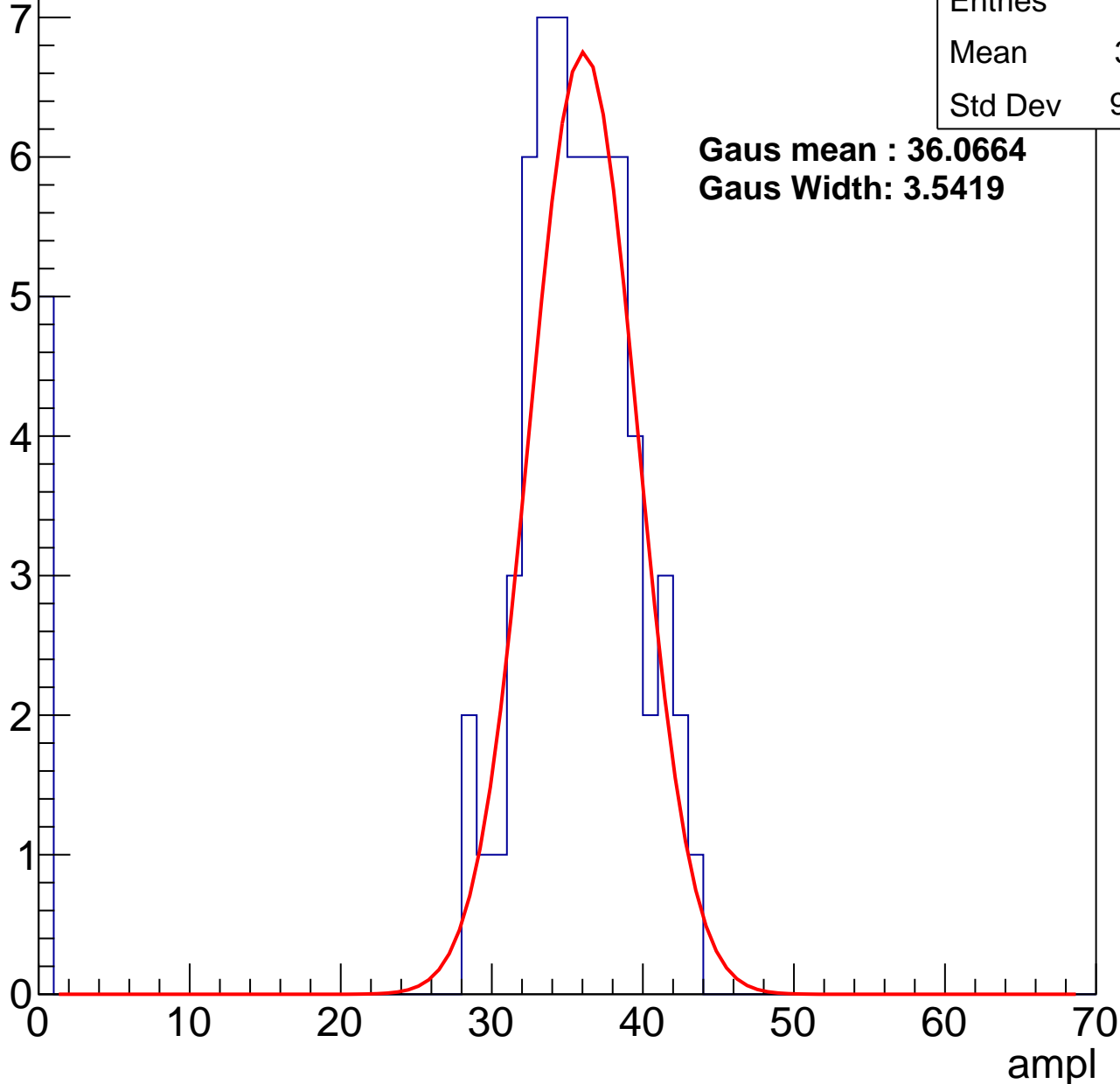
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	32.81
Std Dev	9.824

**Gaus mean : 36.0664**

**Gaus Width: 3.5419**



# B1L103S, U3-ch94, adc2

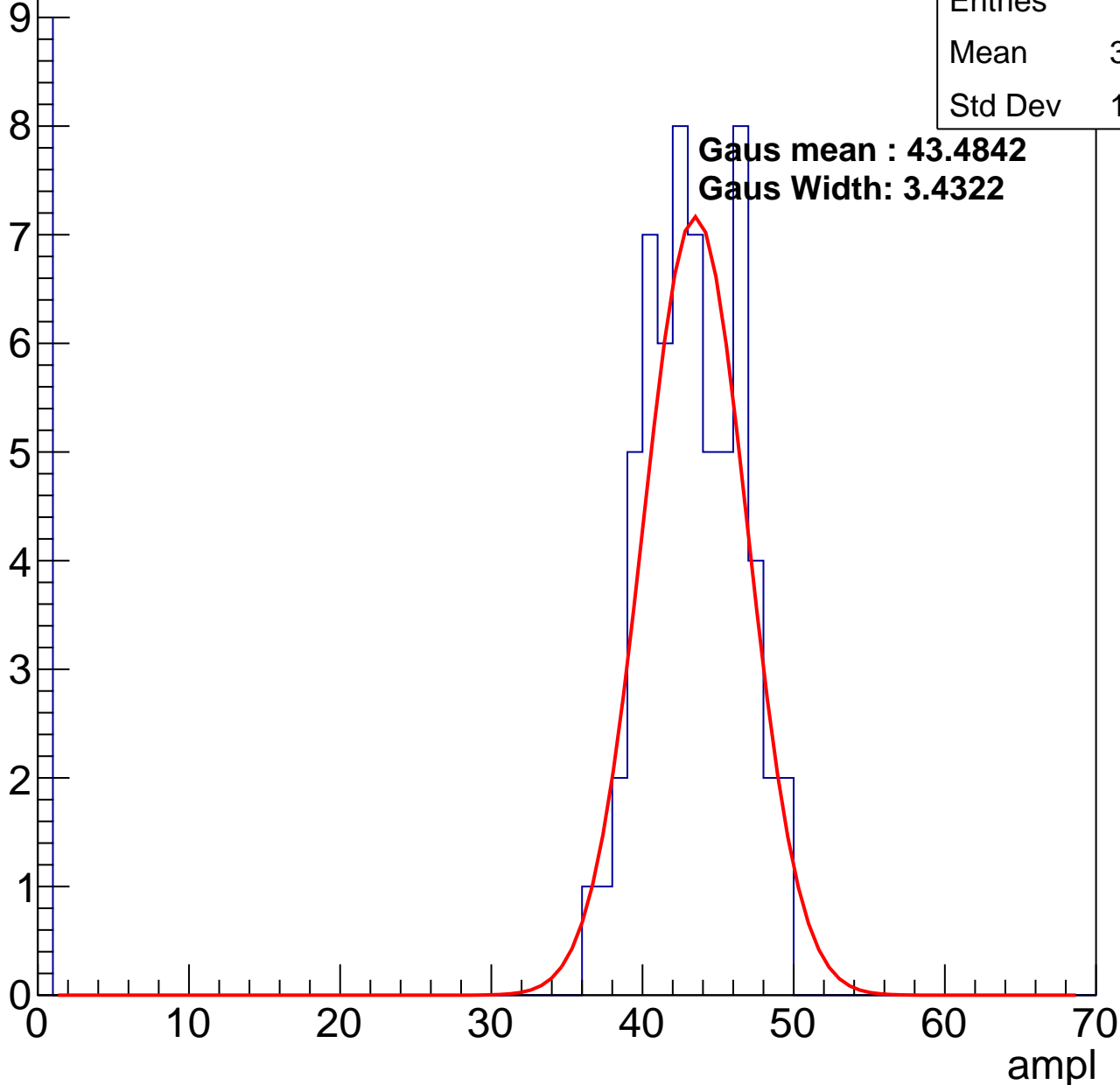
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	72
Mean	37.53
Std Dev	14.47

**Gaus mean : 43.4842**

**Gaus Width: 3.4322**

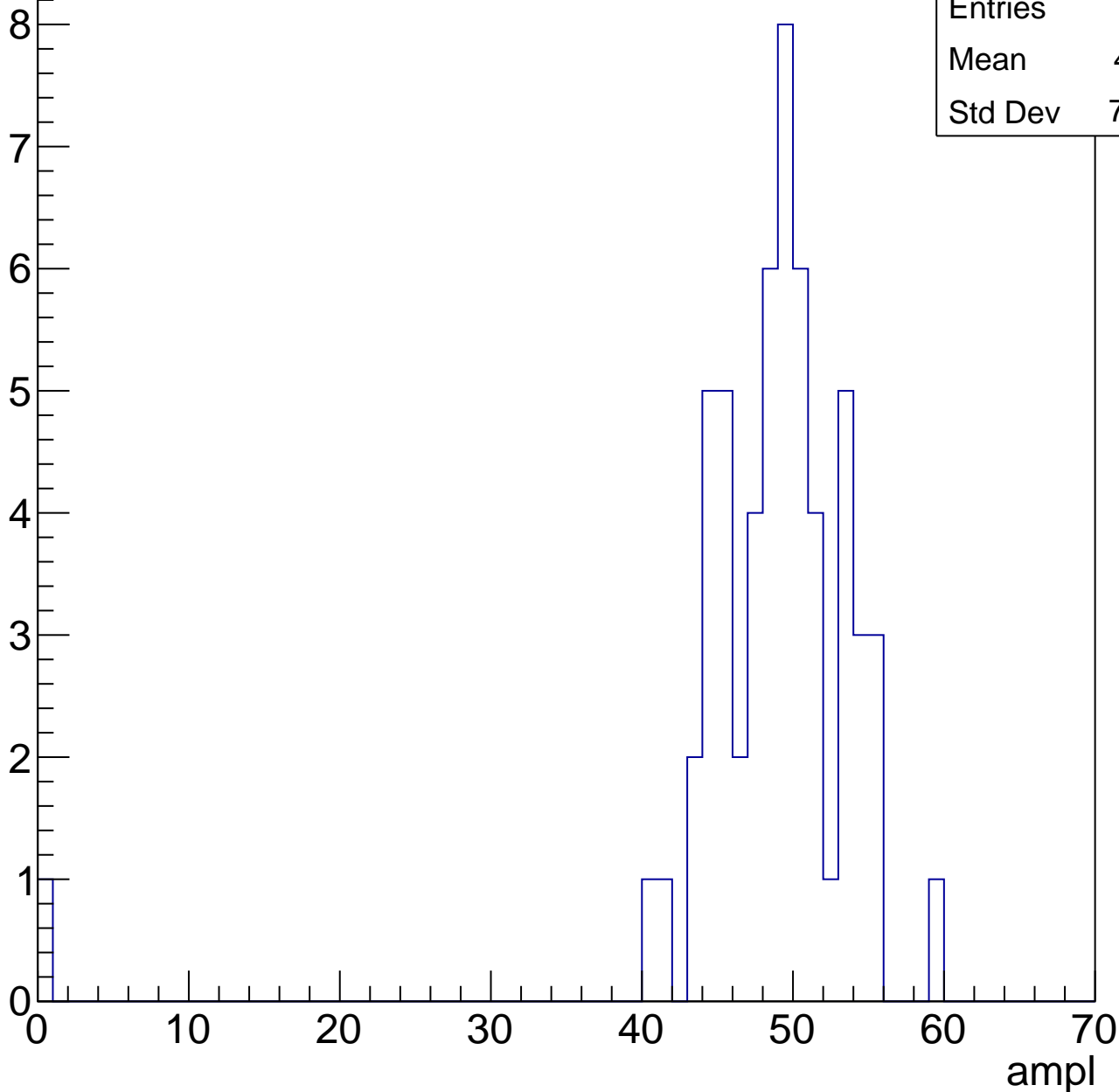


# B1L103S, U3-ch94, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

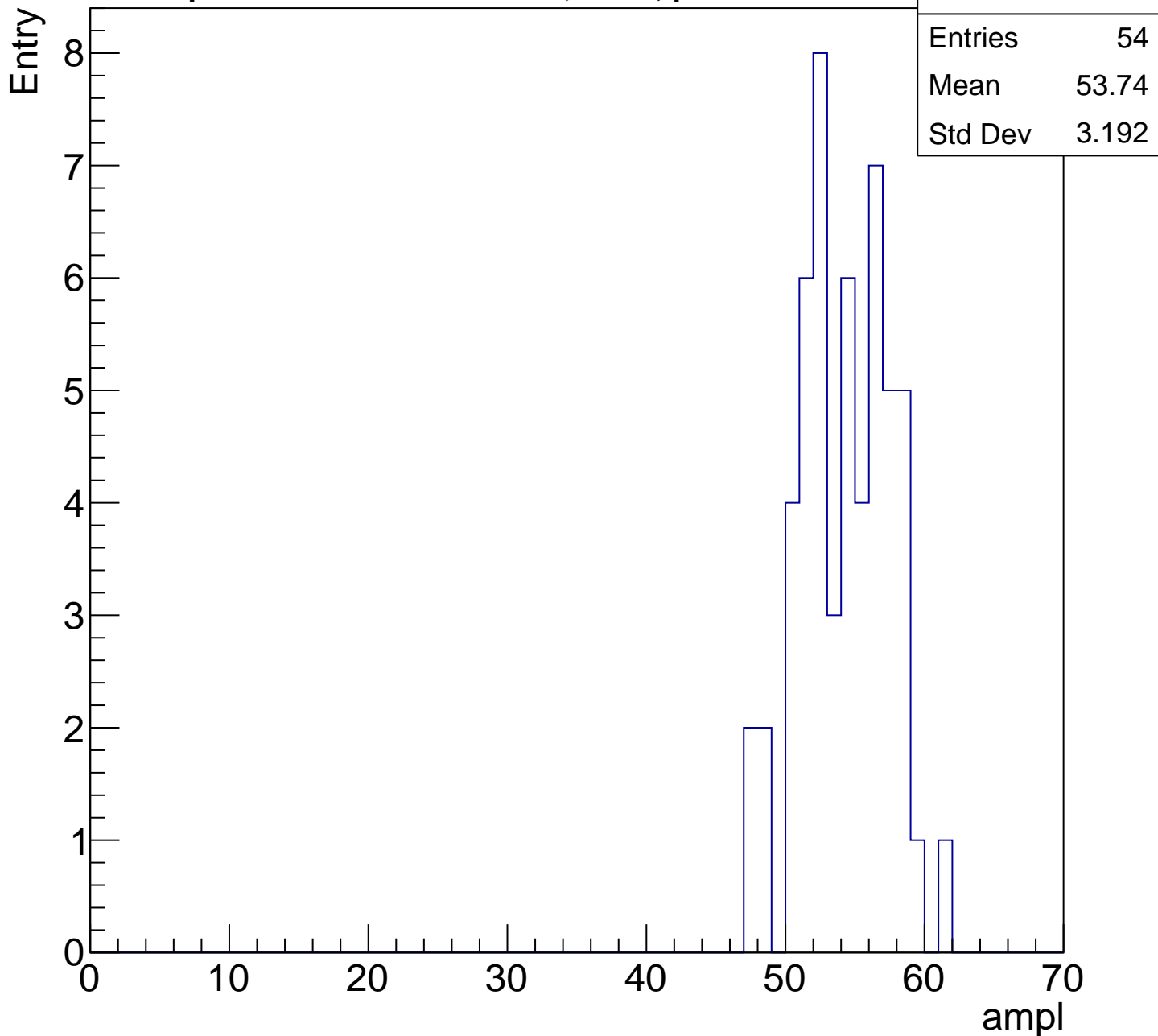
Entry

Entries	58
Mean	47.91
Std Dev	7.415



# B1L103S, U3-ch94, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U3-ch94, adc5

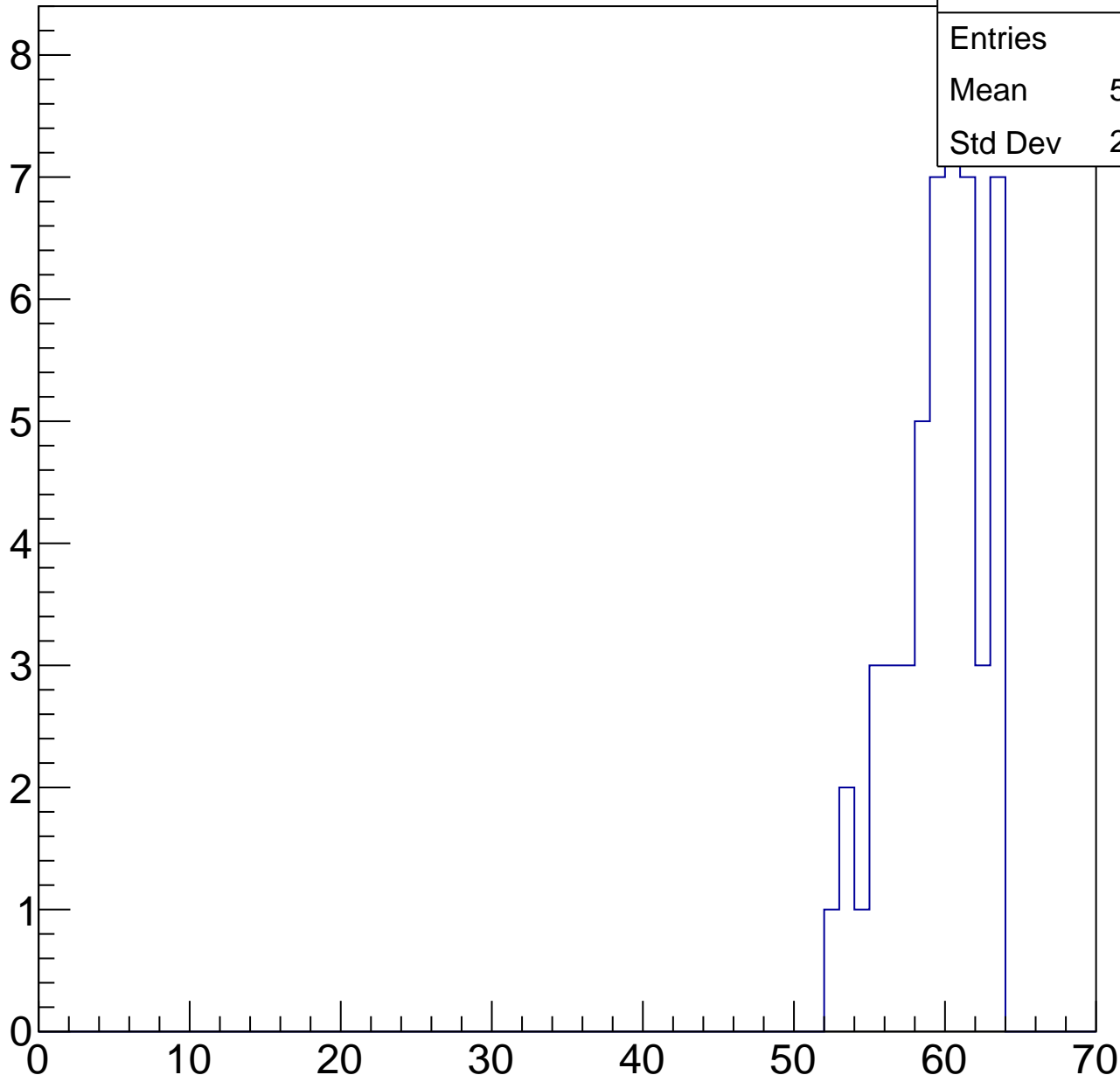
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	50
Mean	59.06
Std Dev	2.873

ampl

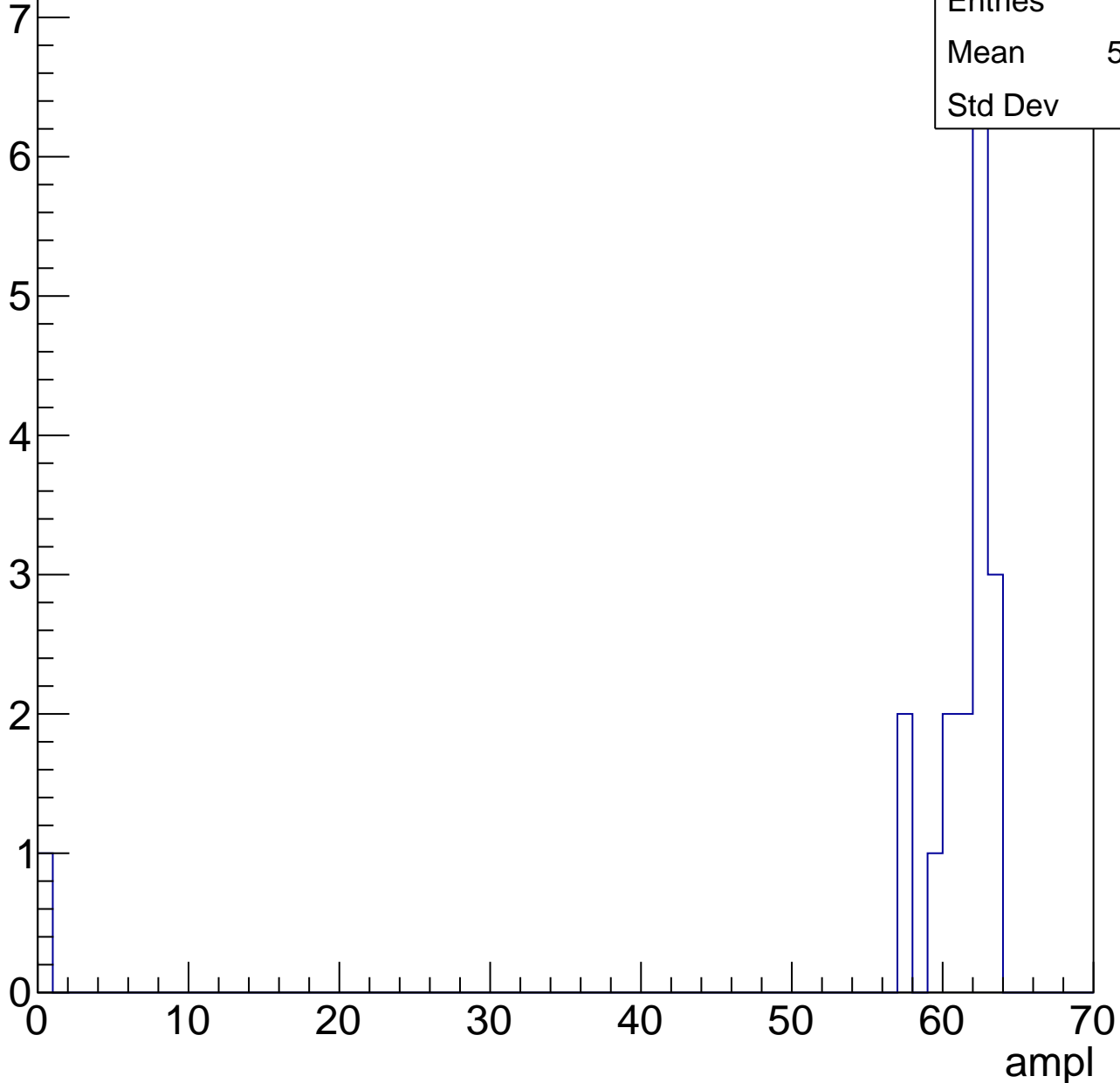


# B1L103S, U3-ch94, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	18
Mean	57.67
Std Dev	14.1





# B1L103S, U3-ch94, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	18
Mean	0
Std Dev	0

ampl

# B1L103S, U3-ch95, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	89
Mean	19.3
Std Dev	12.71

**Gaus mean : 27.1267**

**Gaus Width: 2.8165**

Entry

25

20

15

10

5

0

0

10

20

30

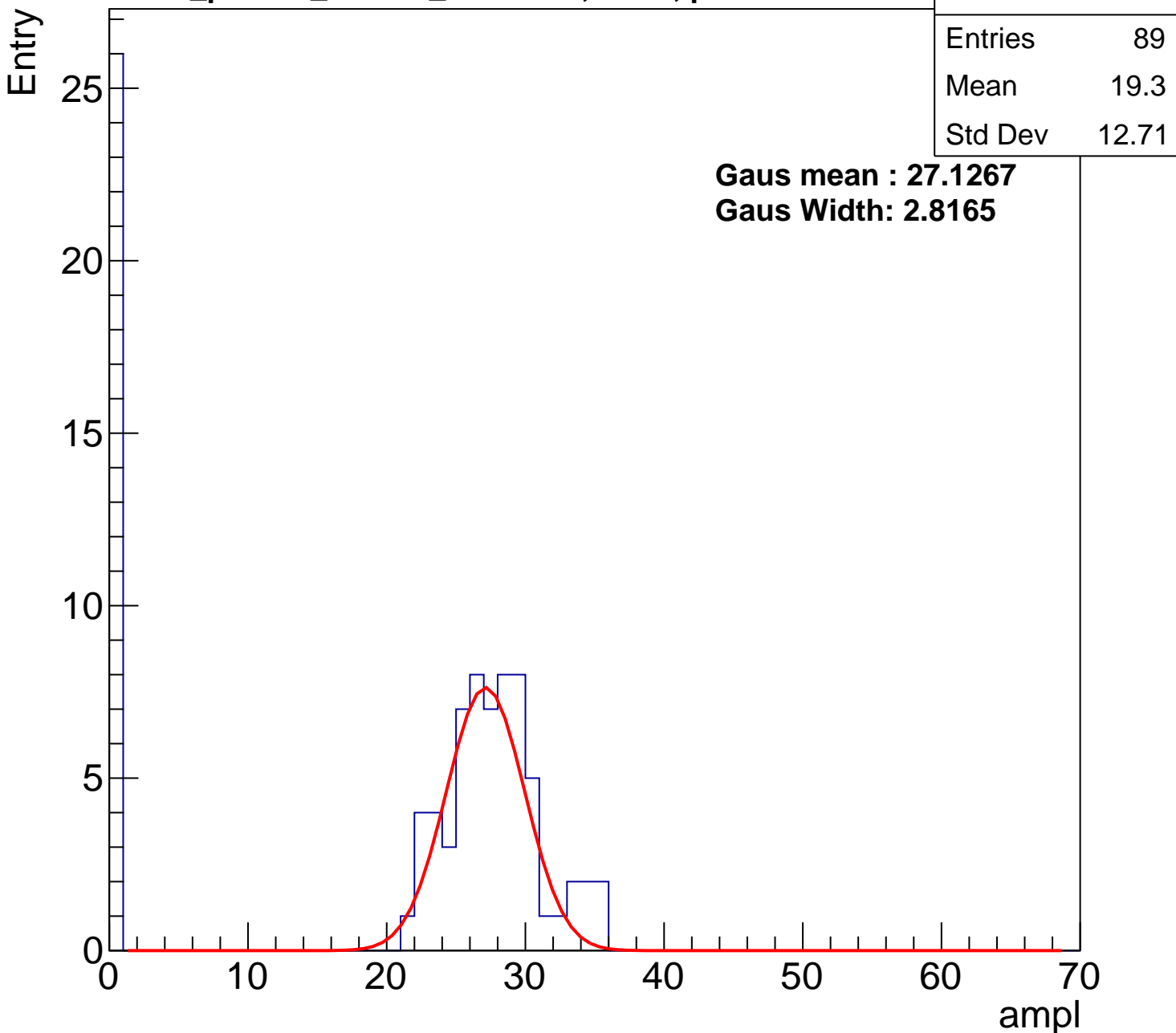
40

50

60

70

ampl



# B1L103S, U3-ch95, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	86
Mean	28.7
Std Dev	12.69

**Gaus mean : 34.1190**

**Gaus Width: 3.5149**

Entry

12

10

8

6

4

2

0

0

10

20

30

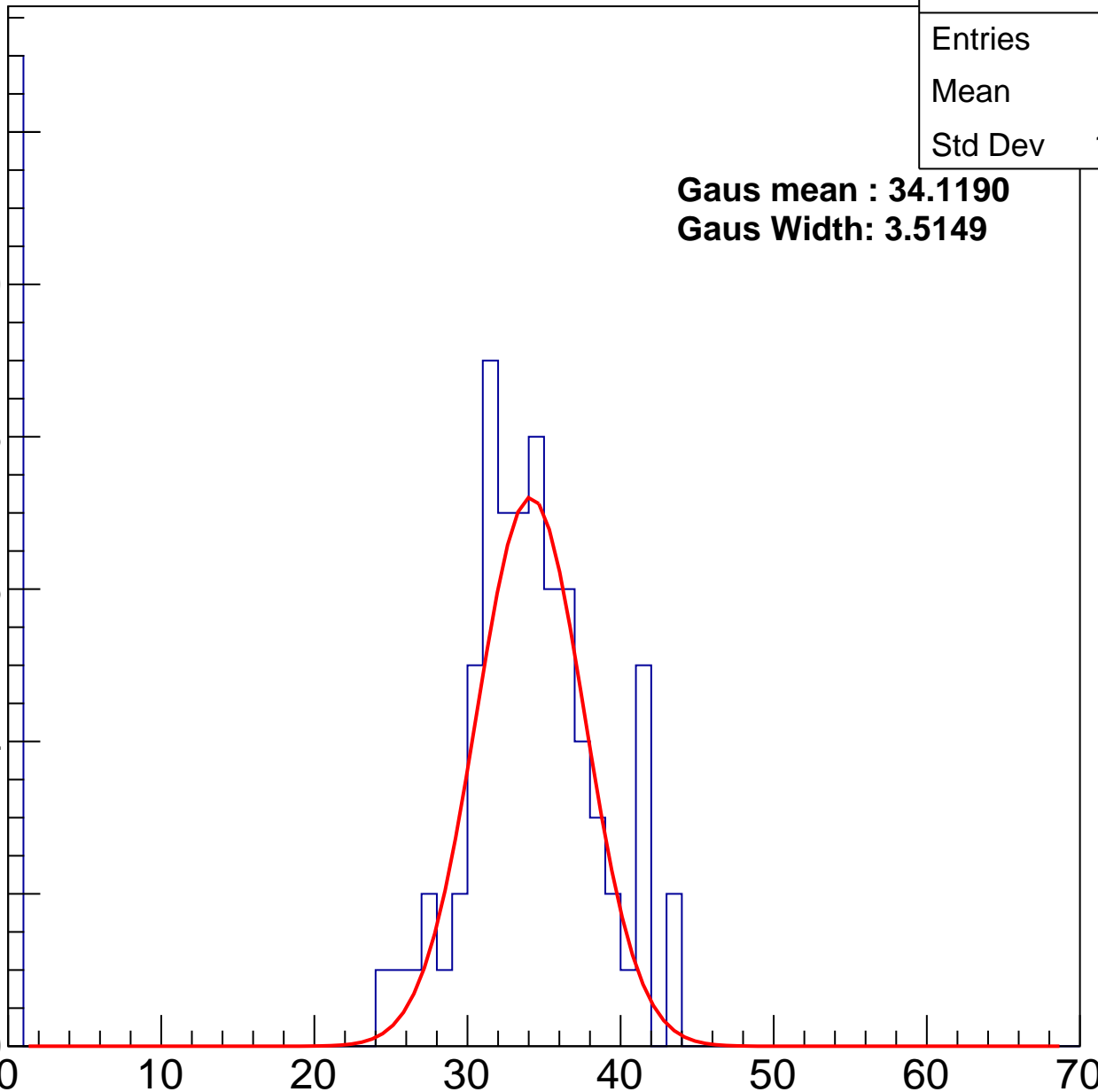
40

50

60

70

ampl



# B1L103S, U3-ch95, adc2

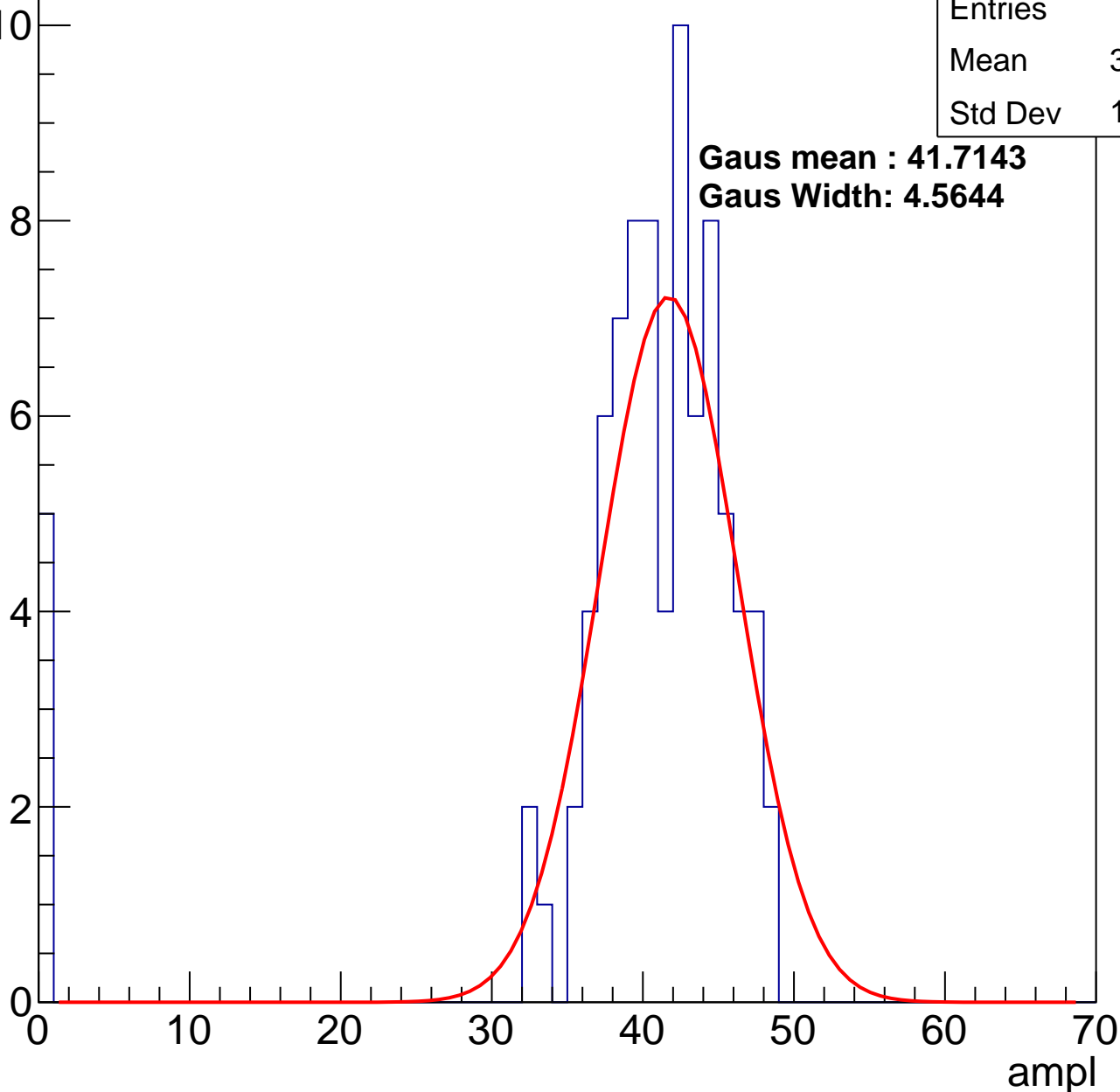
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	86
Mean	38.58
Std Dev	10.25

**Gaus mean : 41.7143**

**Gaus Width: 4.5644**

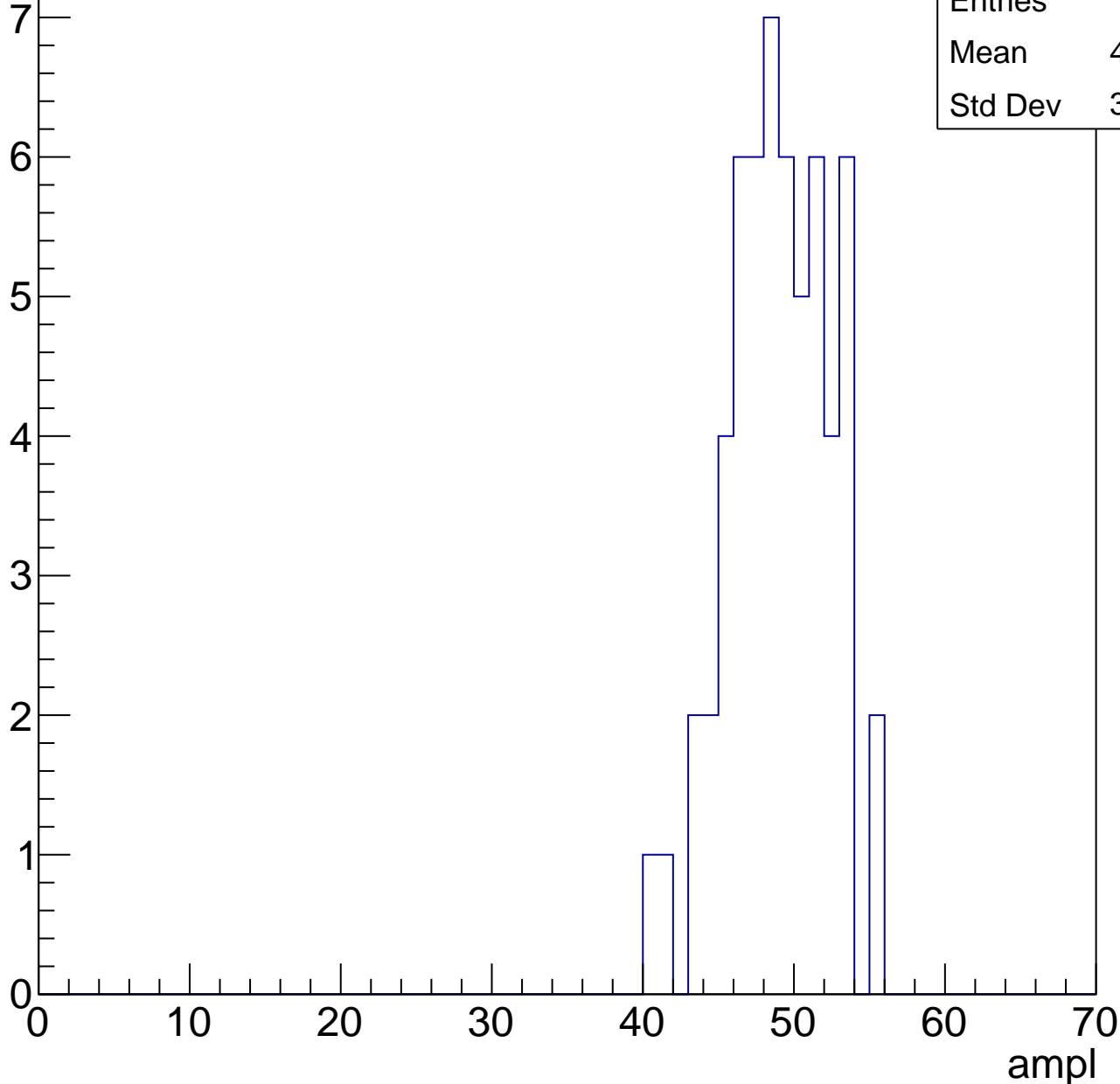


# B1L103S, U3-ch95, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	48.53
Std Dev	3.313

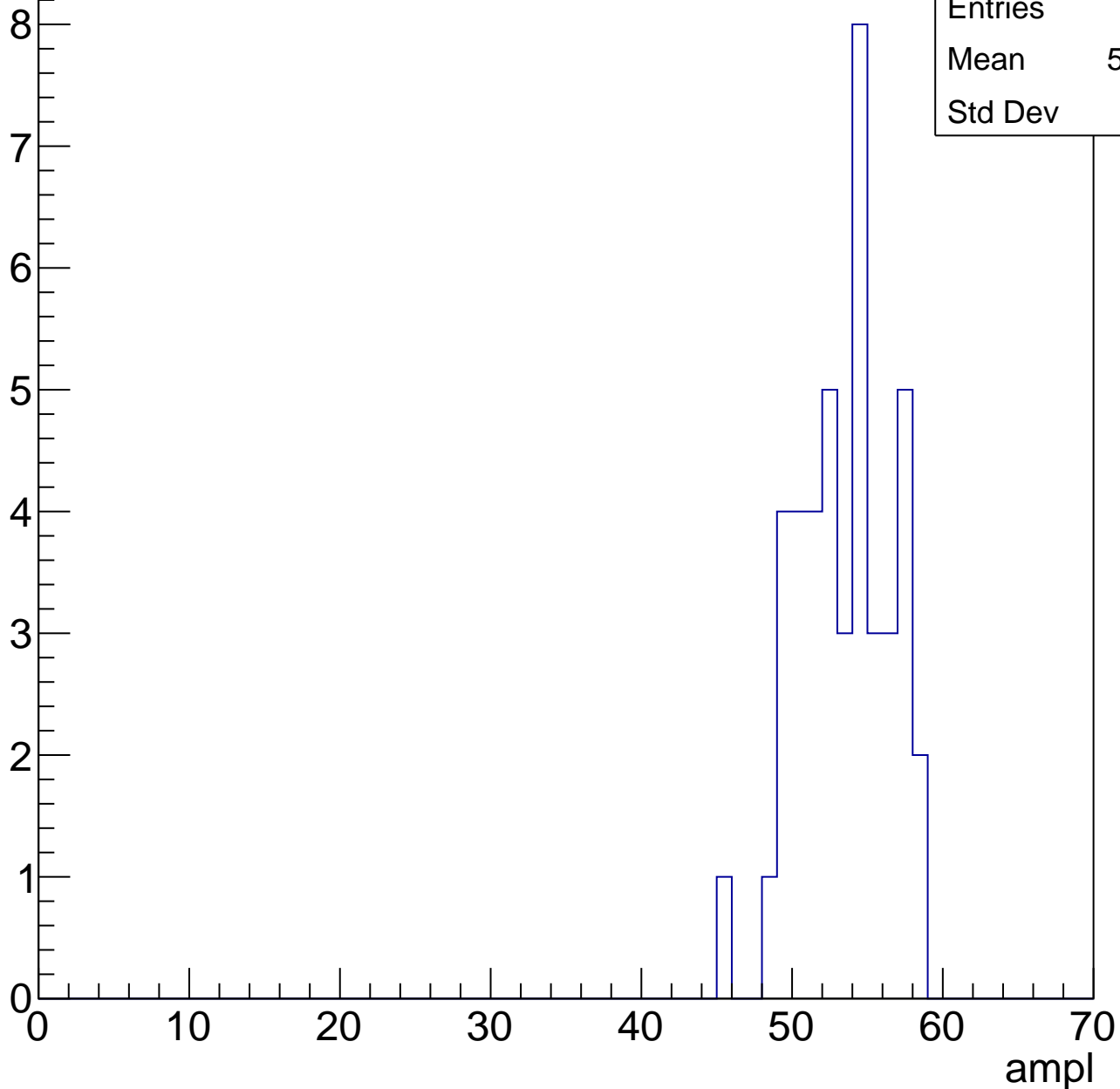


# B1L103S, U3-ch95, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

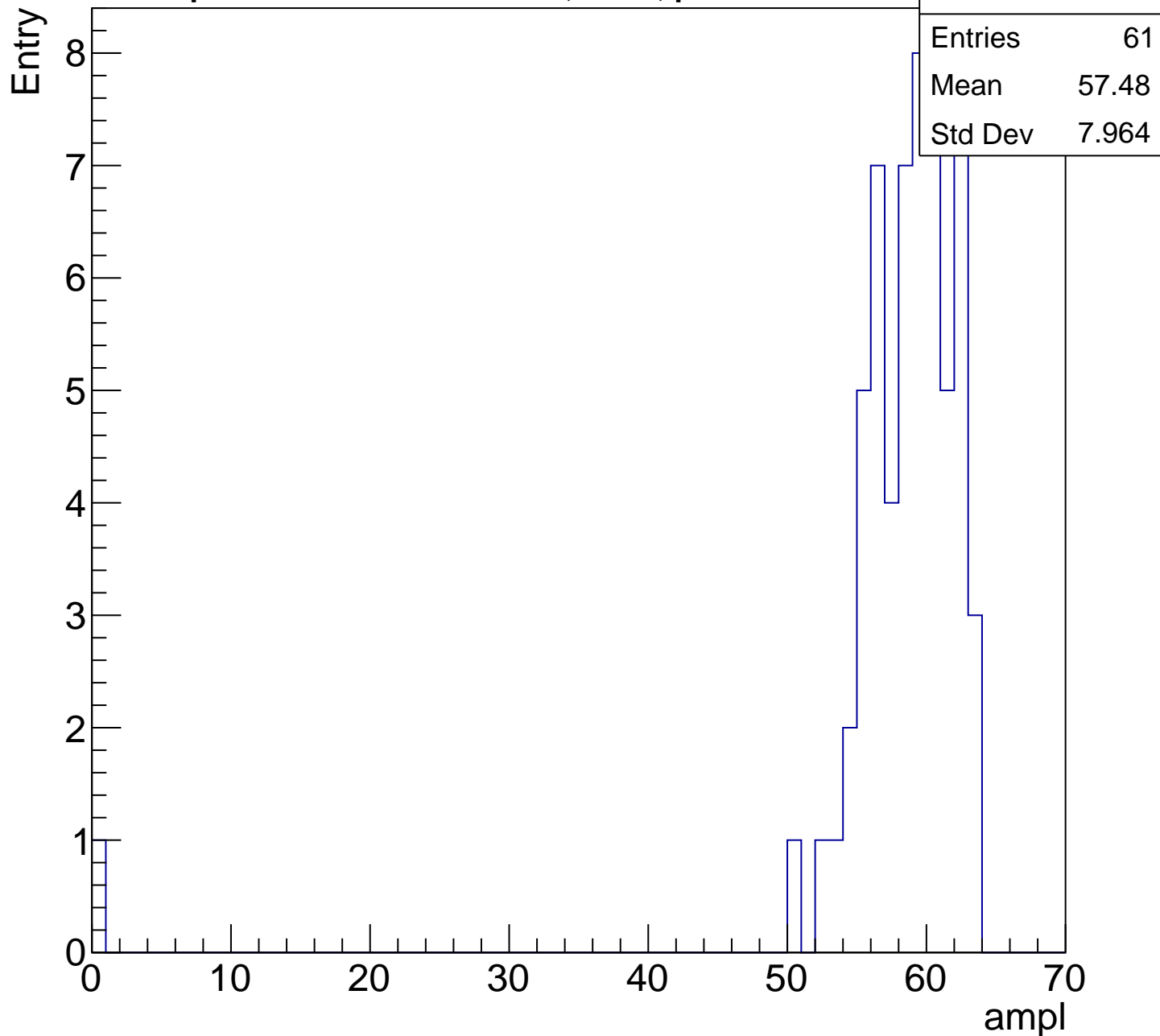
Entry

Entries	43
Mean	52.98
Std Dev	3



# B1L103S, U3-ch95, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

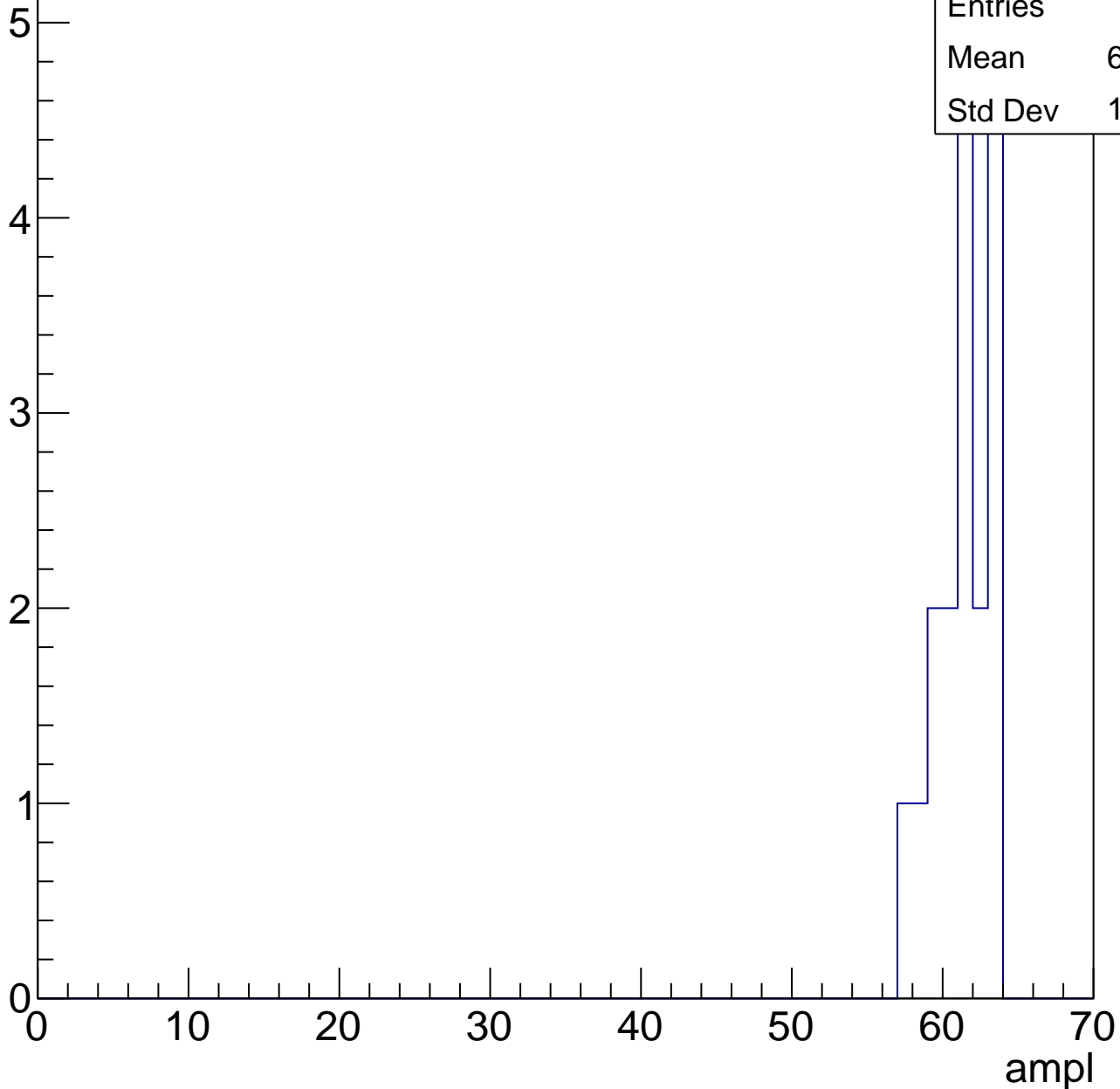


# B1L103S, U3-ch95, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	18
Mean	60.94
Std Dev	1.779





# B1L103S, U3-ch95, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U3-ch96, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	83
Mean	23.63
Std Dev	9.788

**Gaus mean : 27.6104**

**Gaus Width: 3.6889**

Entry

10

8

6

4

2

0

0

10

20

30

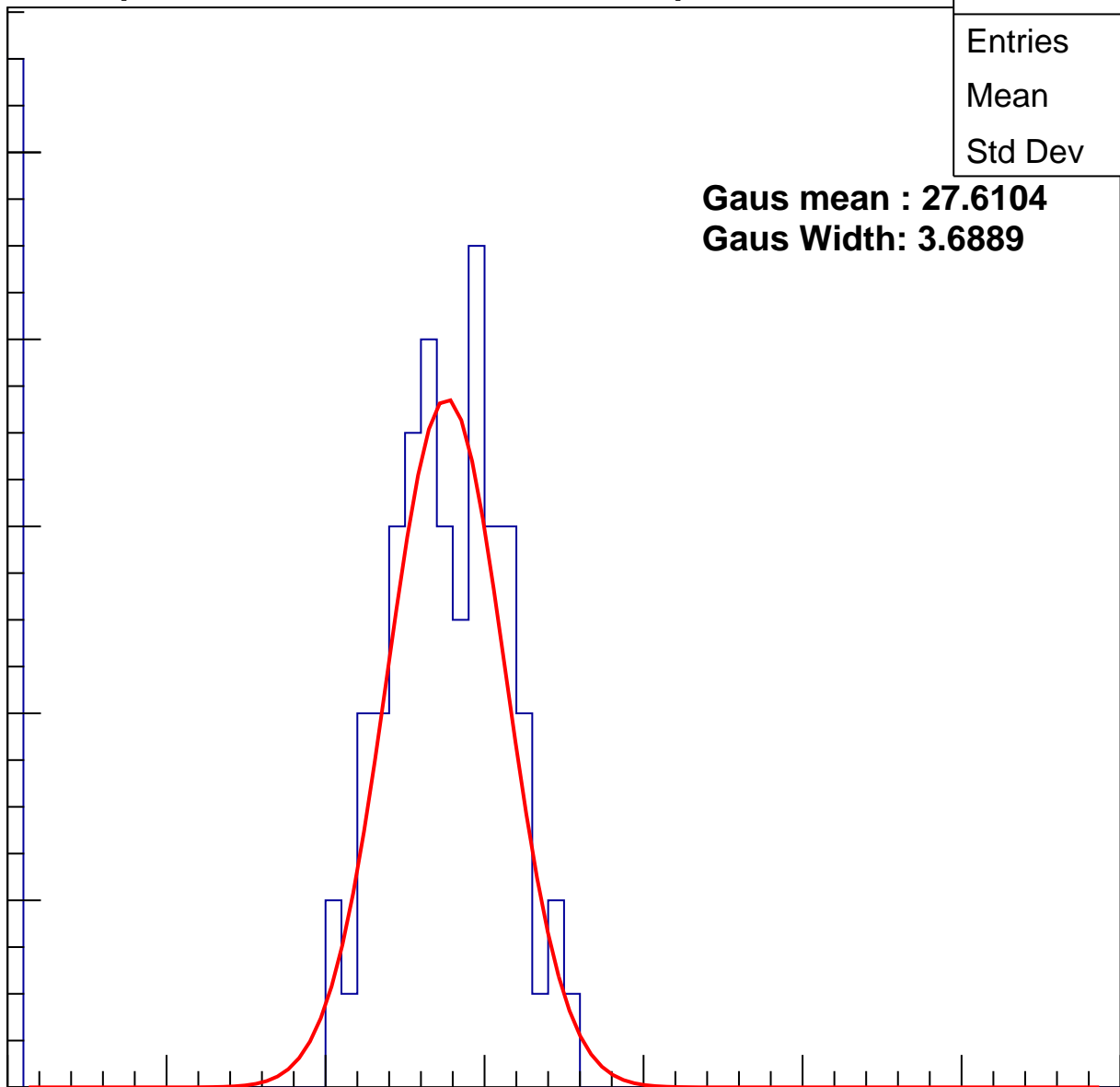
40

50

60

70

ampl



# B1L103S, U3-ch96, adc1

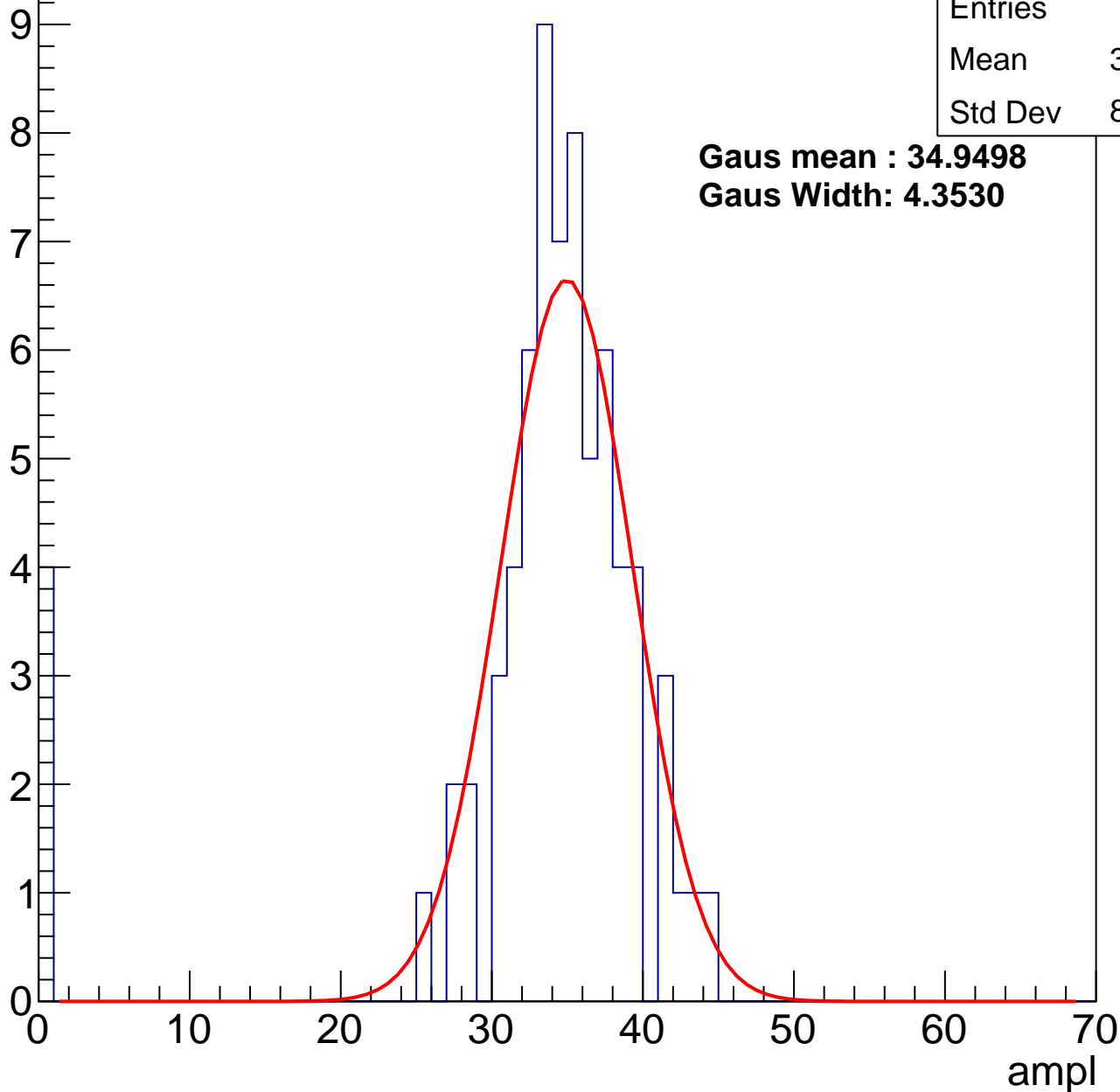
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	71
Mean	32.65
Std Dev	8.802

**Gaus mean : 34.9498**

**Gaus Width: 4.3530**



# B1L103S, U3-ch96, adc2

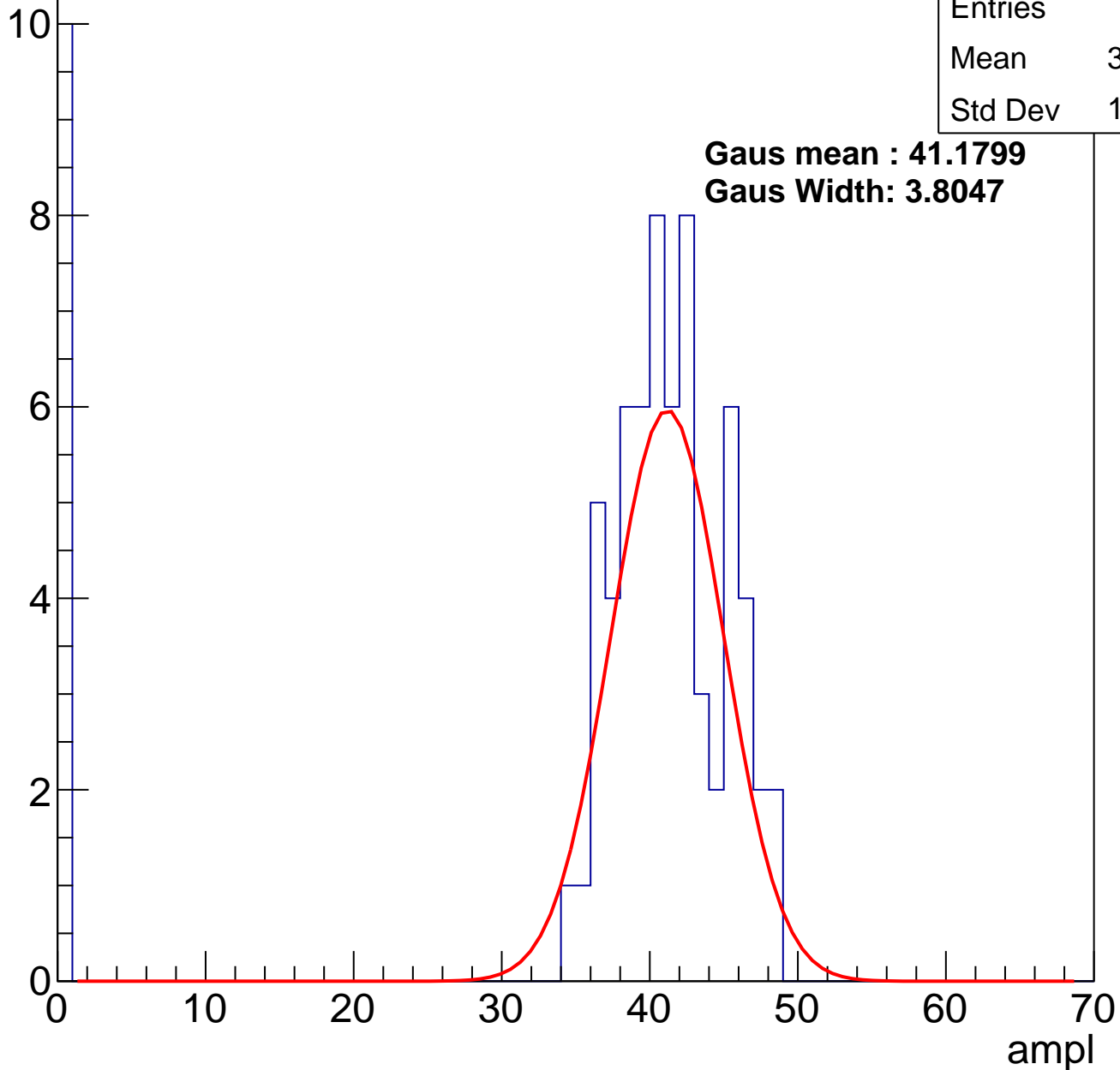
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	74
Mean	35.43
Std Dev	14.37

**Gaus mean : 41.1799**

**Gaus Width: 3.8047**

Entry

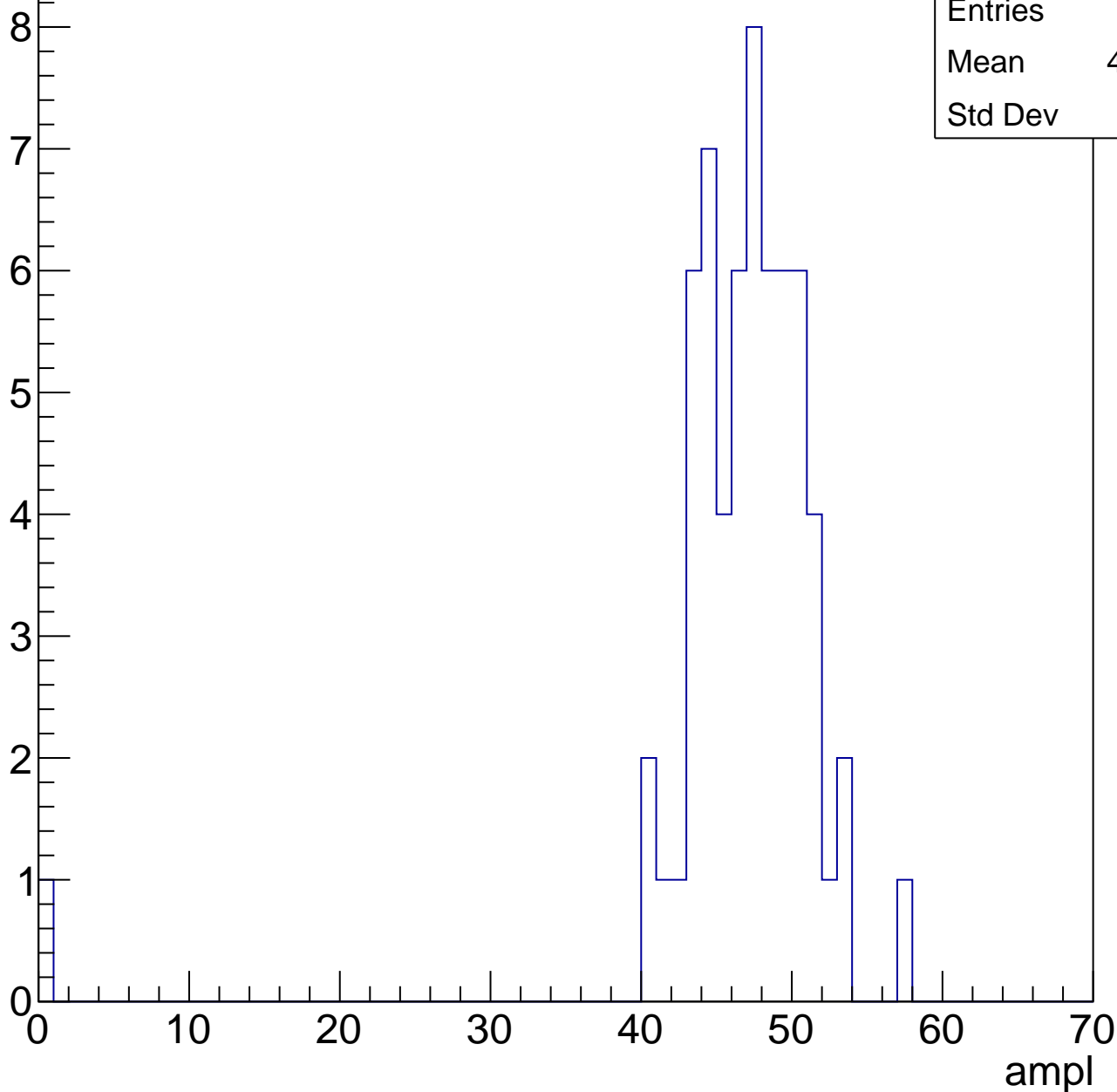


# B1L103S, U3-ch96, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

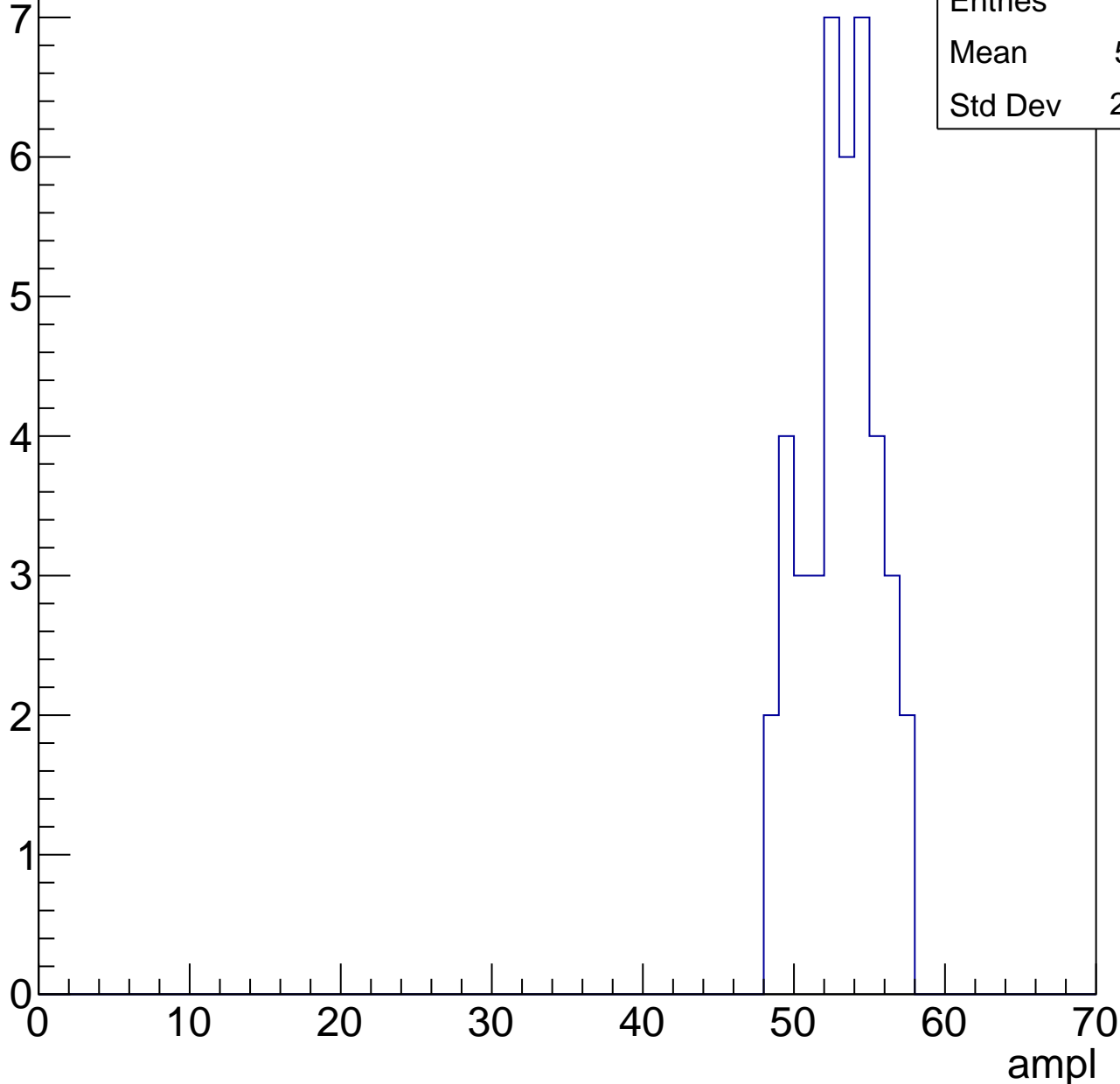
Entries	62
Mean	46.16
Std Dev	6.78



# B1L103S, U3-ch96, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



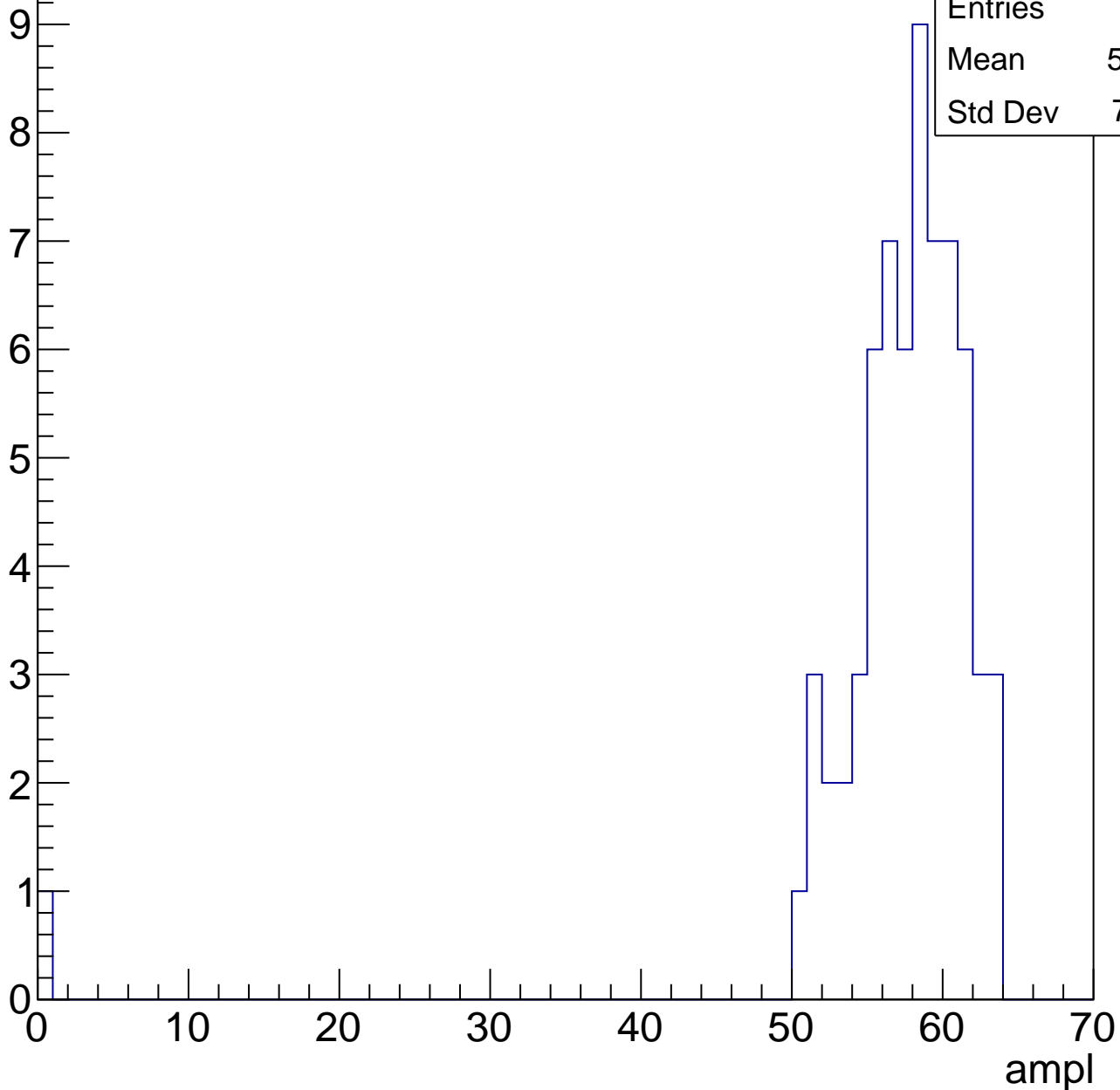
Entries	41
Mean	52.61
Std Dev	2.398

# B1L103S, U3-ch96, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	56.59
Std Dev	7.701

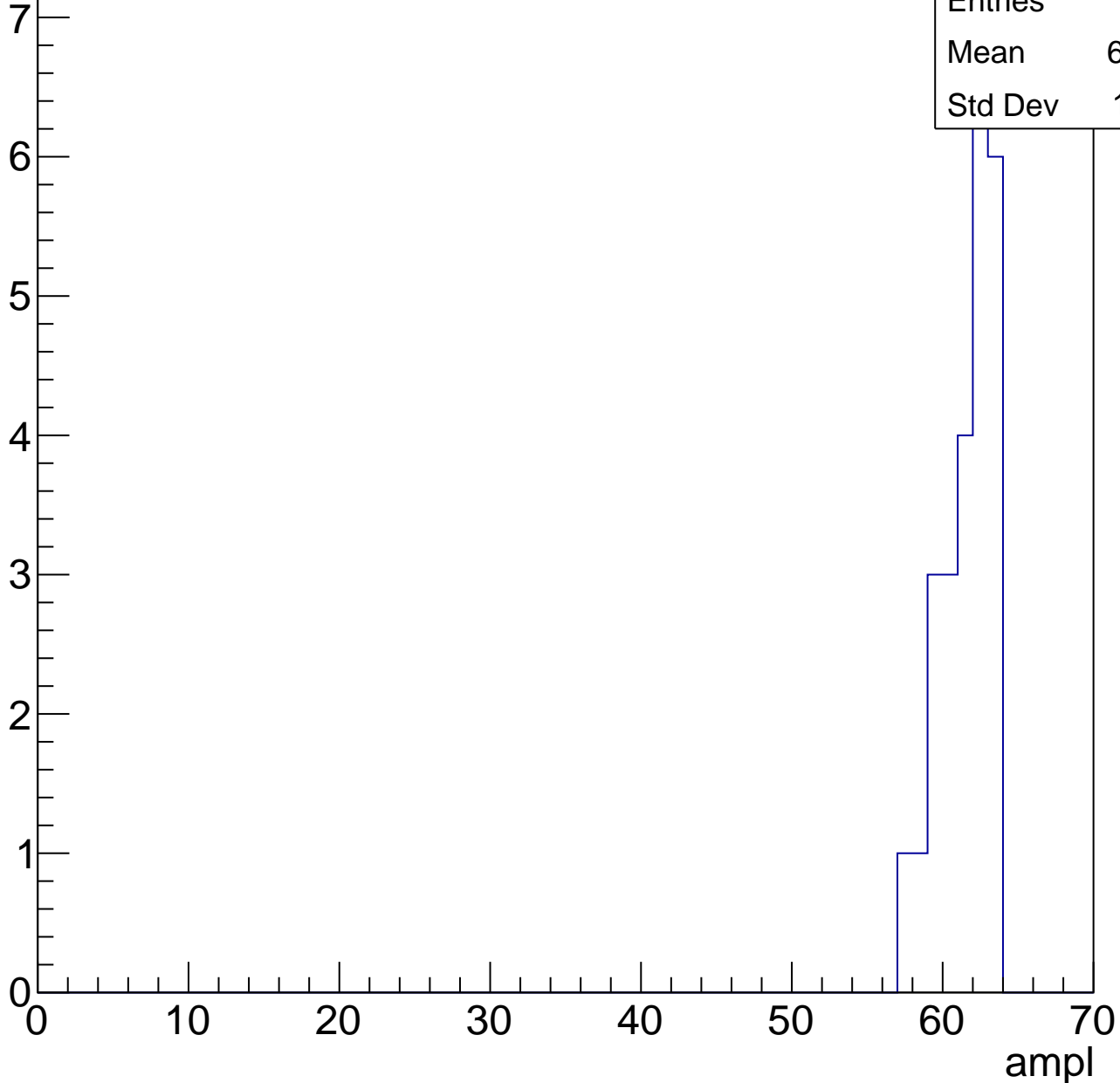


# B1L103S, U3-ch96, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	25
Mean	61.12
Std Dev	1.681

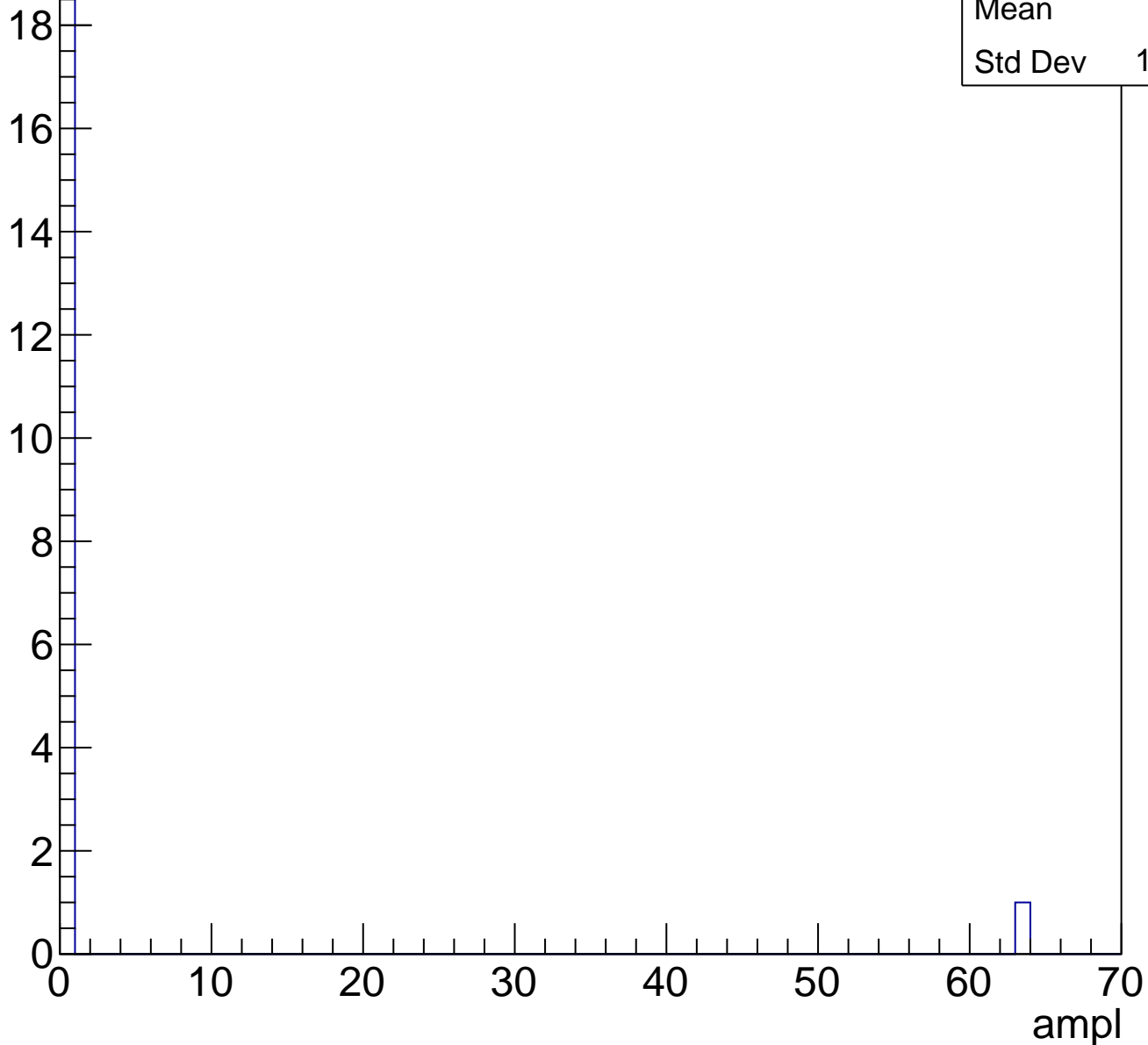




# B1L103S, U3-ch96, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



# B1L103S, U3-ch97, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	80
Mean	23.6
Std Dev	11.72

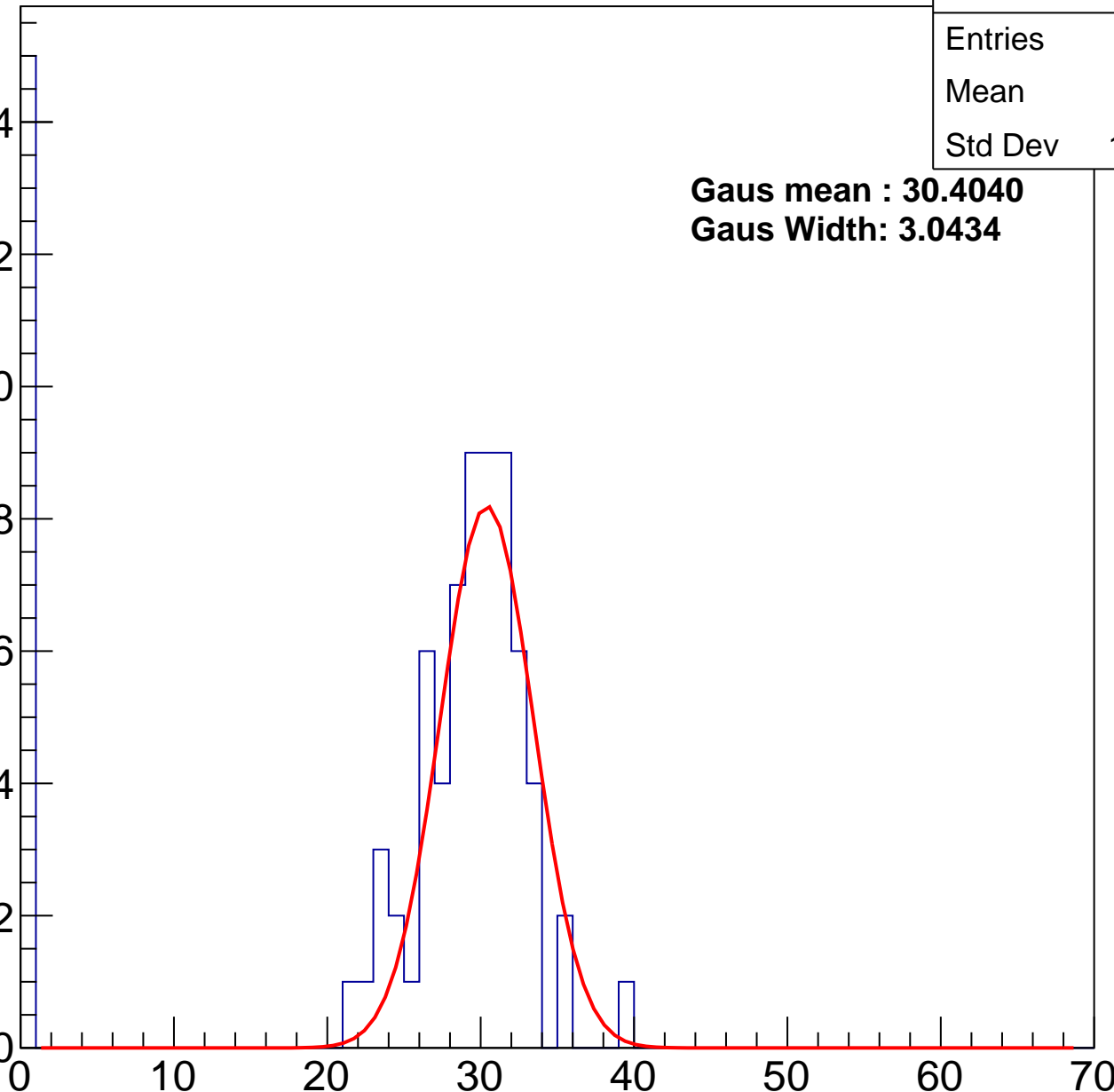
**Gaus mean : 30.4040**

**Gaus Width: 3.0434**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U3-ch97, adc1

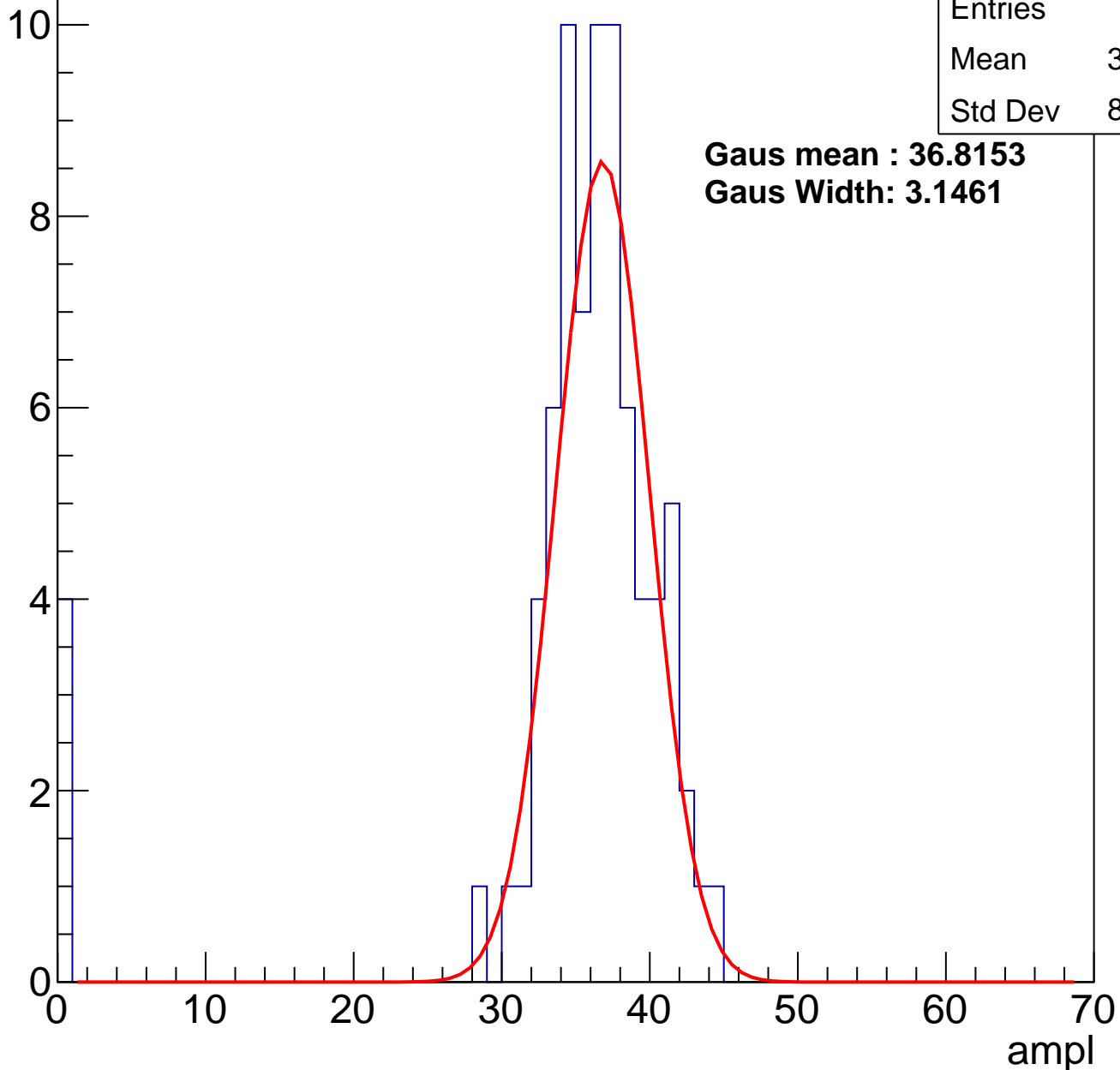
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	77
Mean	34.42
Std Dev	8.622

**Gaus mean : 36.8153**

**Gaus Width: 3.1461**

Entry



# B1L103S, U3-ch97, adc2

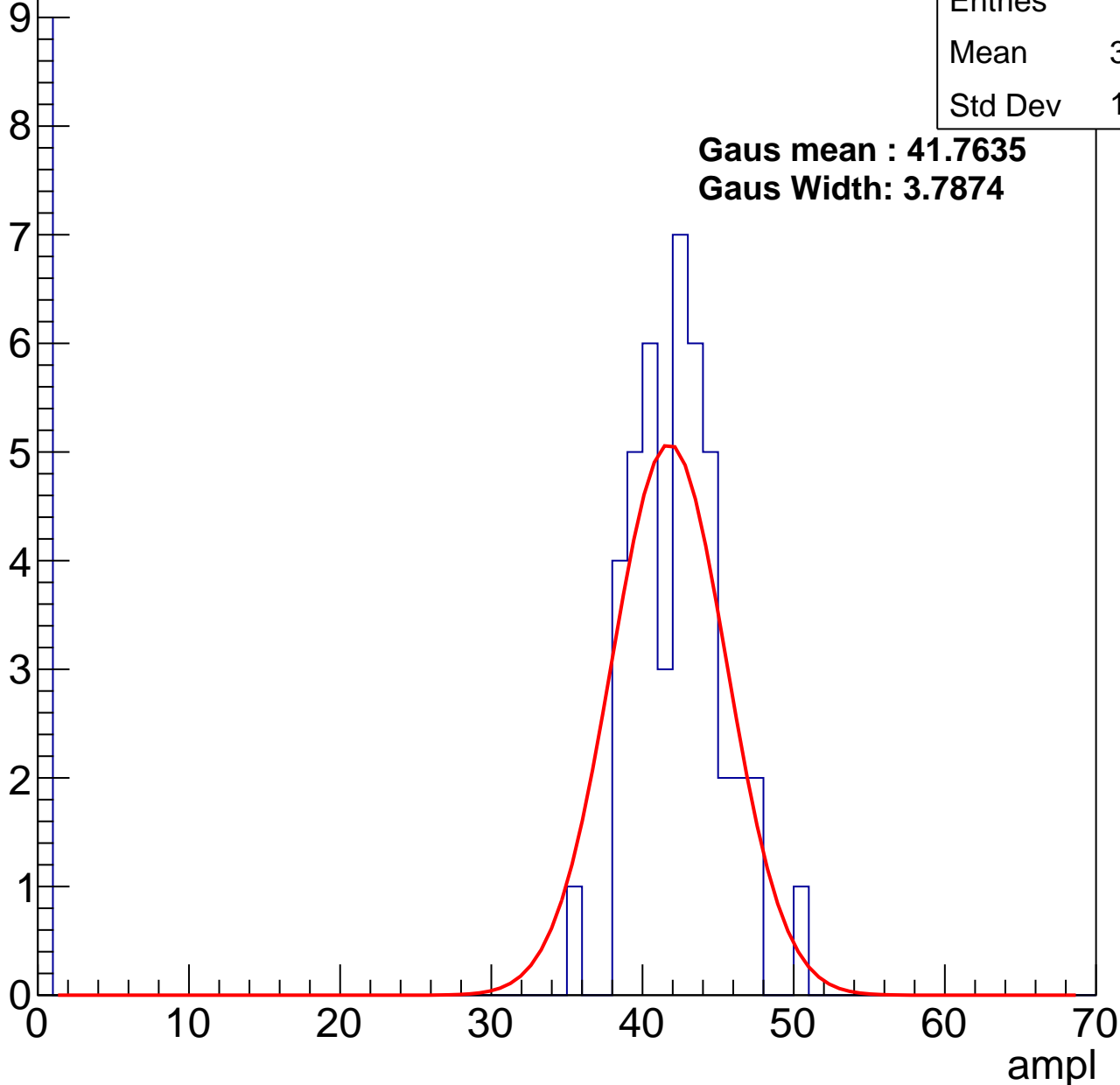
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	53
Mean	34.77
Std Dev	15.95

**Gaus mean : 41.7635**

**Gaus Width: 3.7874**

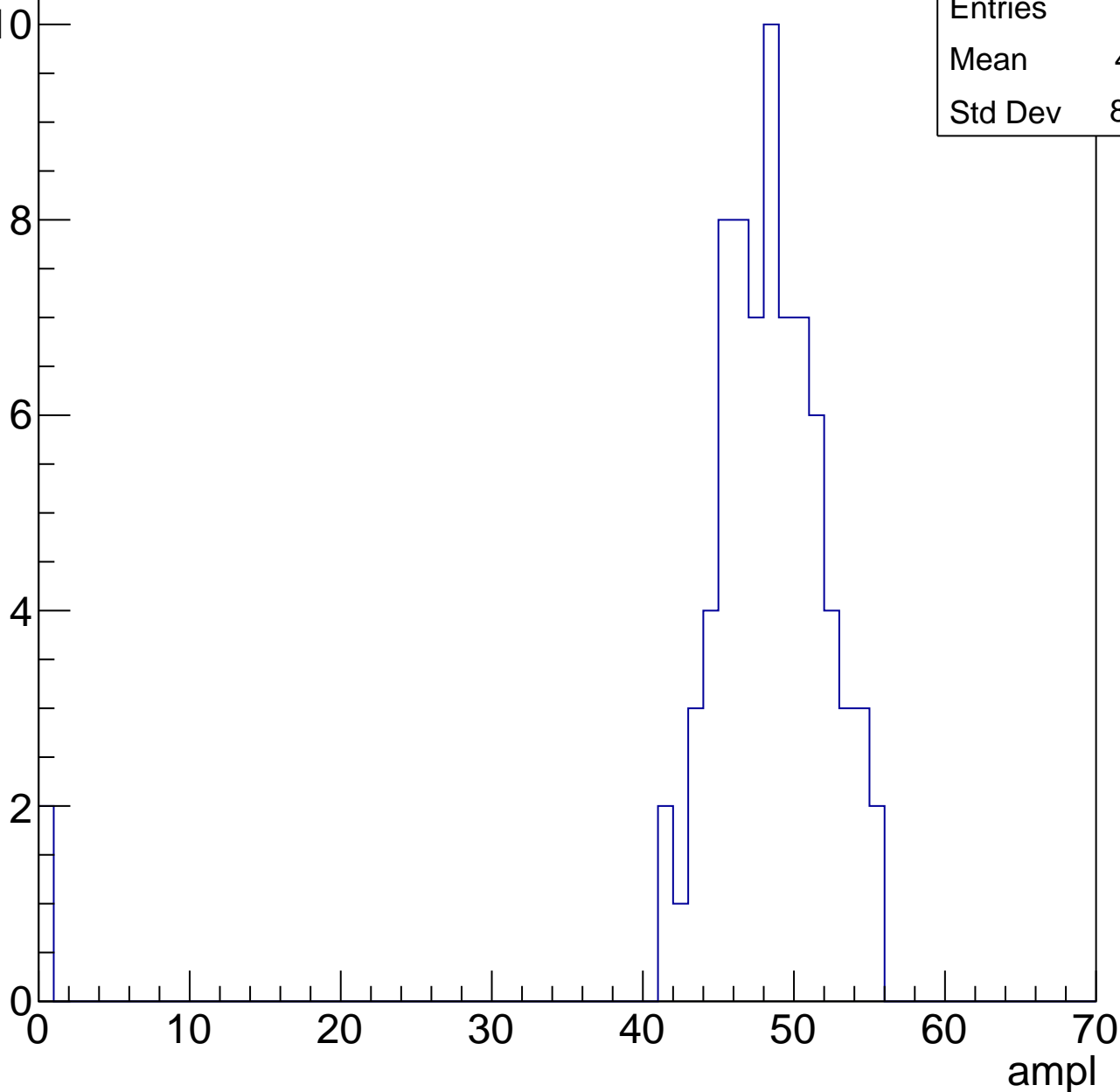


# B1L103S, U3-ch97, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

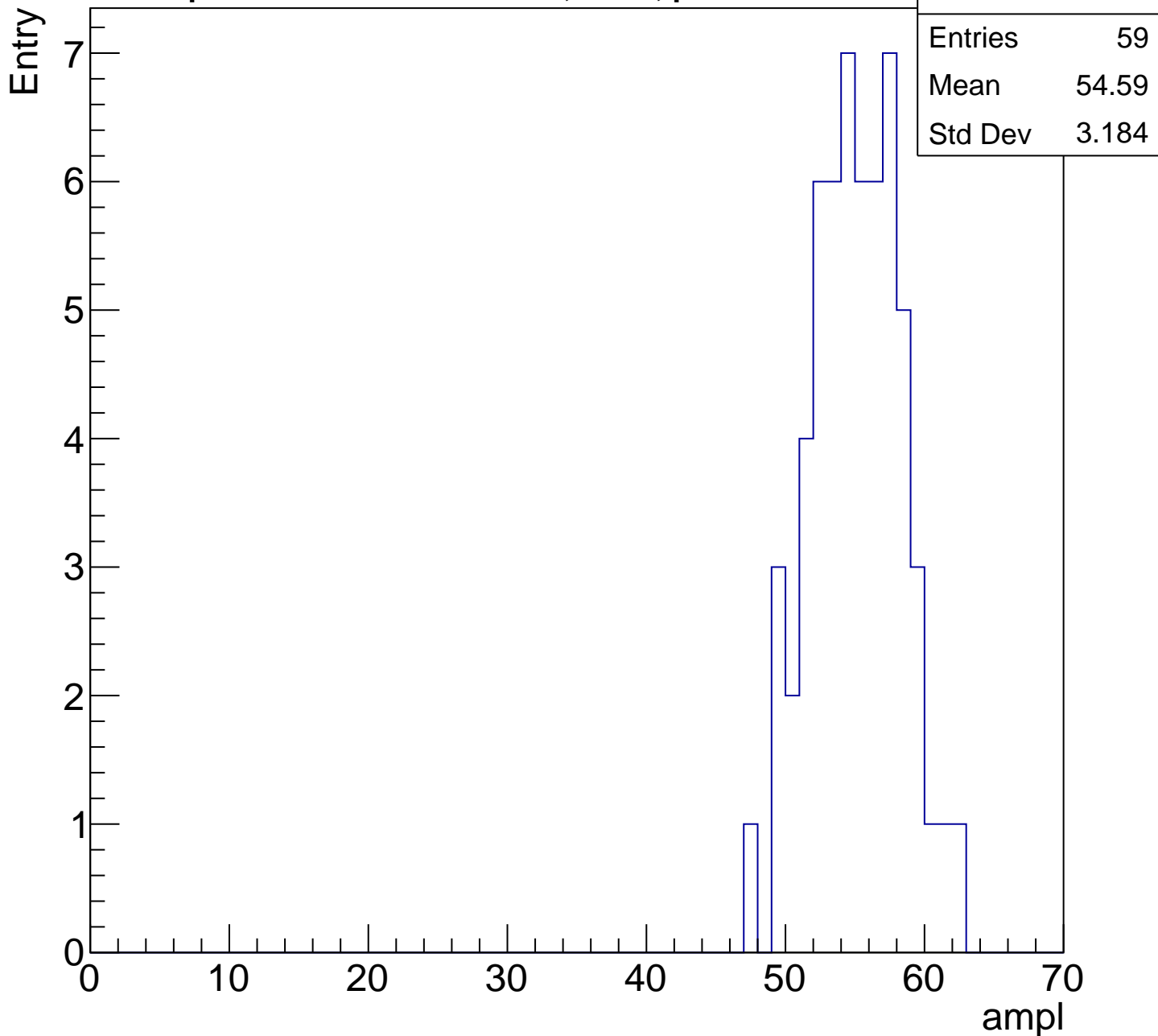
Entry

Entries	77
Mean	46.81
Std Dev	8.309



# B1L103S, U3-ch97, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U3-ch97, adc5

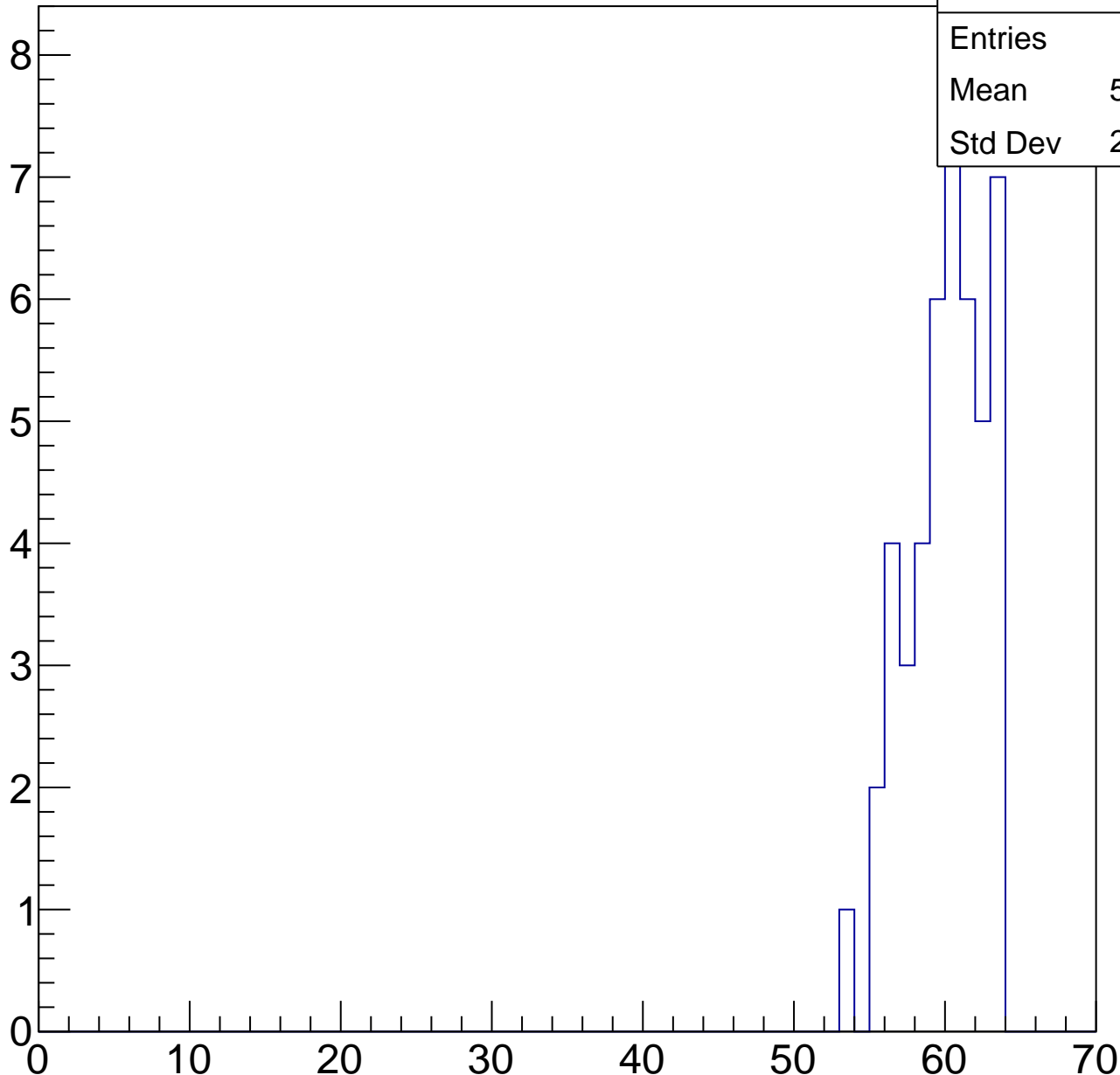
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	46
Mean	59.59
Std Dev	2.524

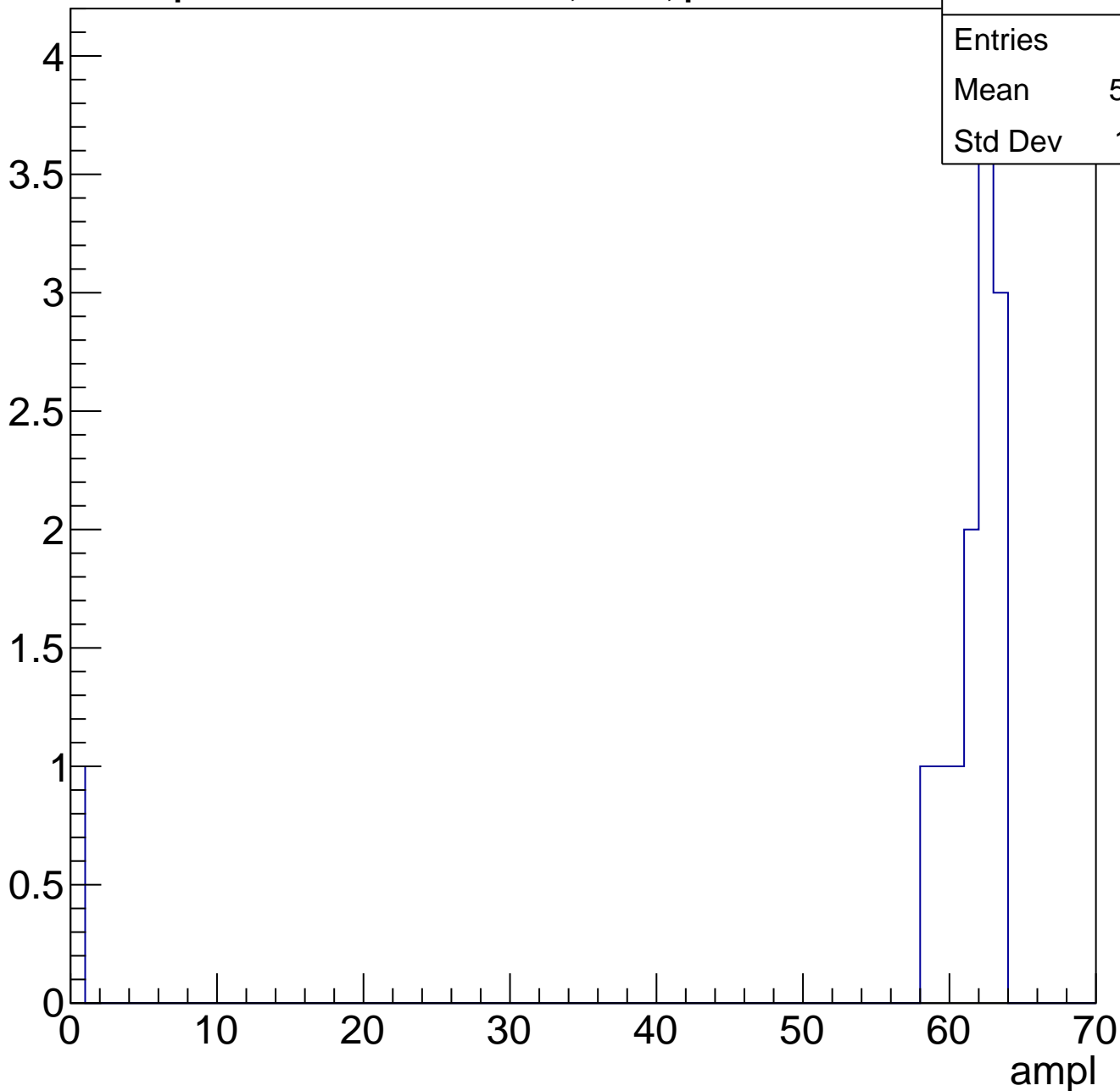
ampl



# B1L103S, U3-ch97, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U3-ch97, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.05
Std Dev	13.29

Entry



# B1L103S, U3-ch98, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	72
Mean	21.56
Std Dev	11.43

**Gaus mean : 27.7177**

**Gaus Width: 3.4743**

Entry

14

12

10

8

6

4

2

0

0

10

20

30

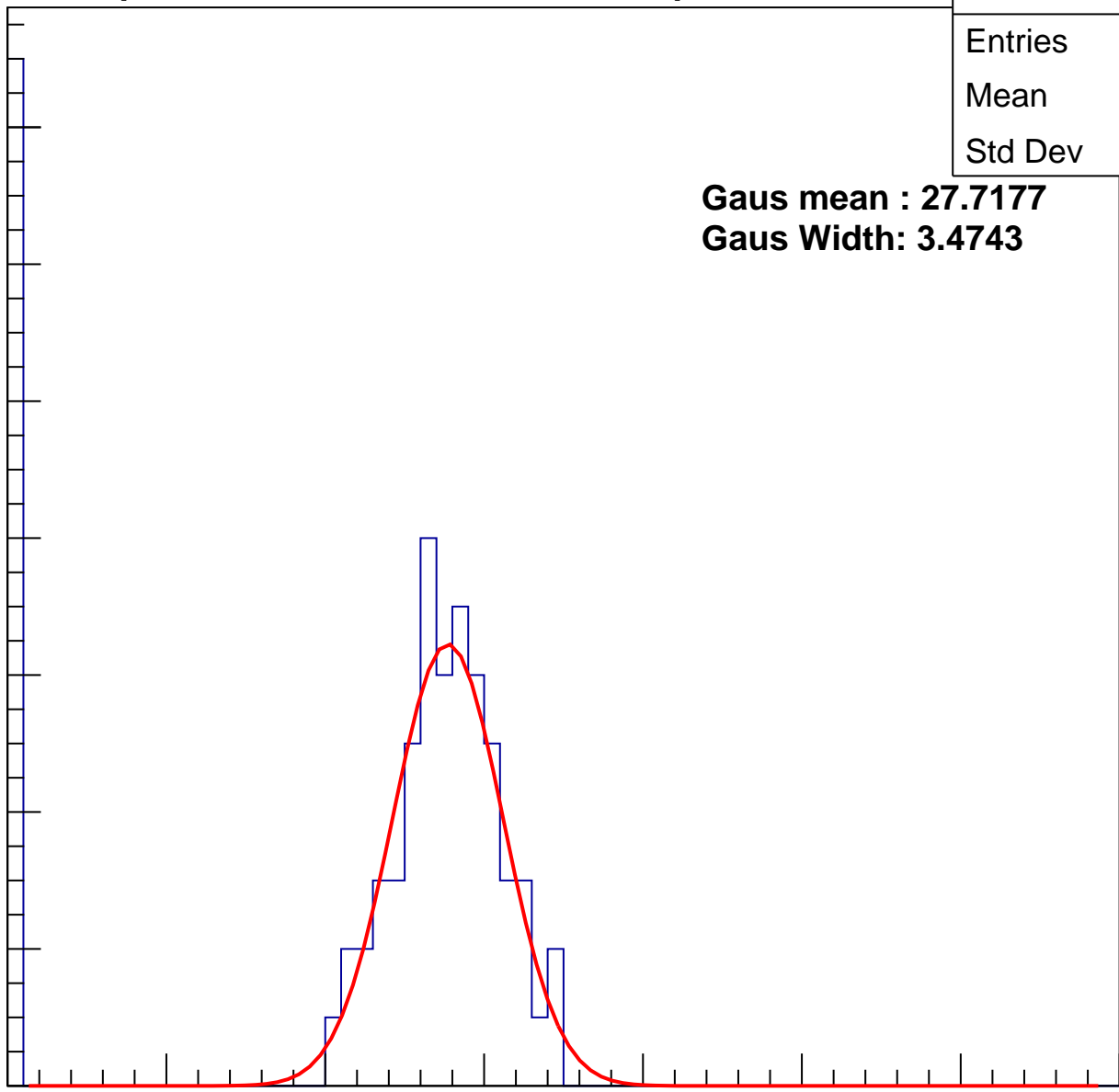
40

50

60

70

ampl



# B1L103S, U3-ch98, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	87
Mean	28.84
Std Dev	11.62

**Gaus mean : 33.9909**

**Gaus Width: 5.0130**

Entry

10

8

6

4

2

0

0

10

20

30

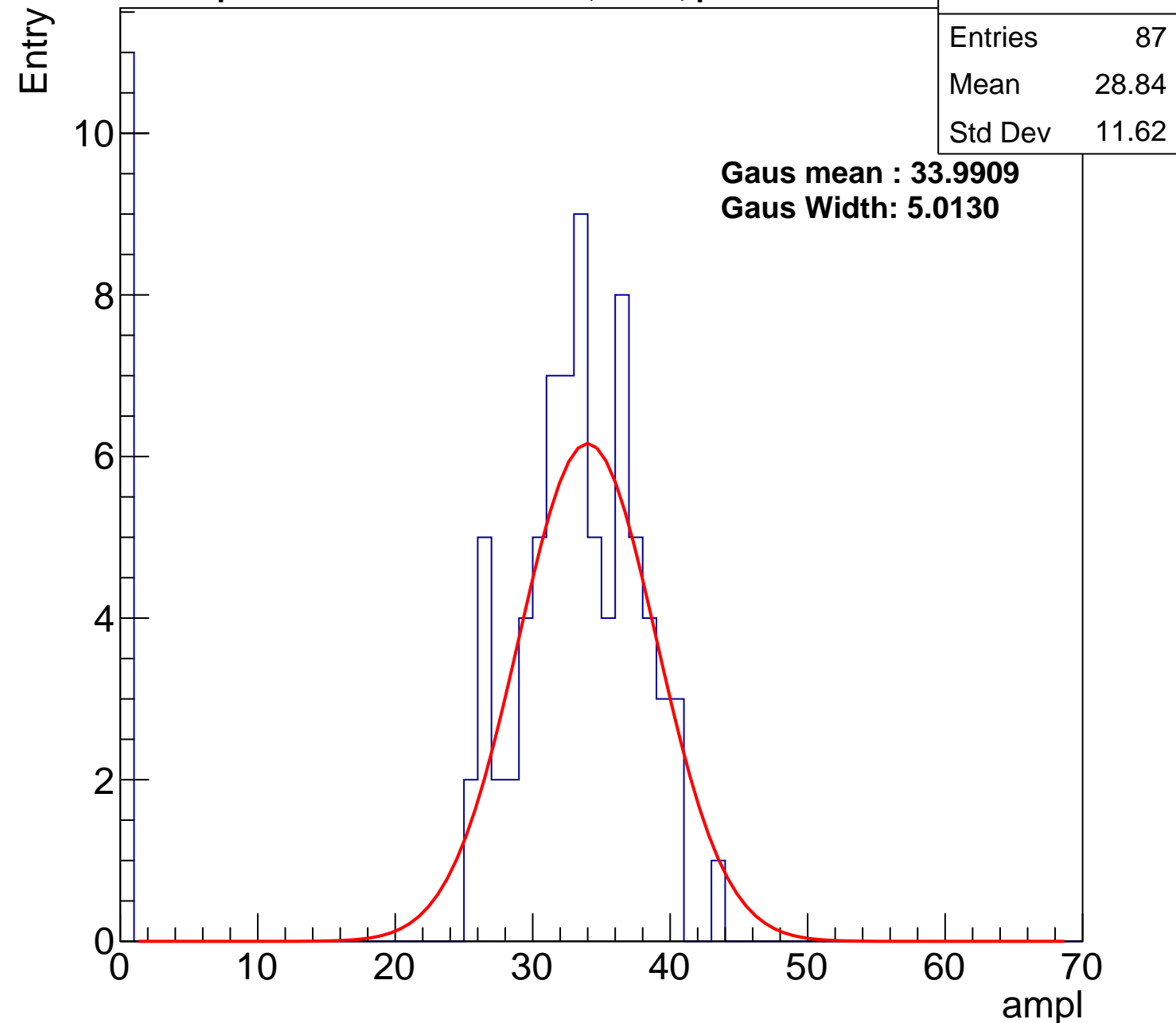
40

50

60

70

ampl



# B1L103S, U3-ch98, adc2

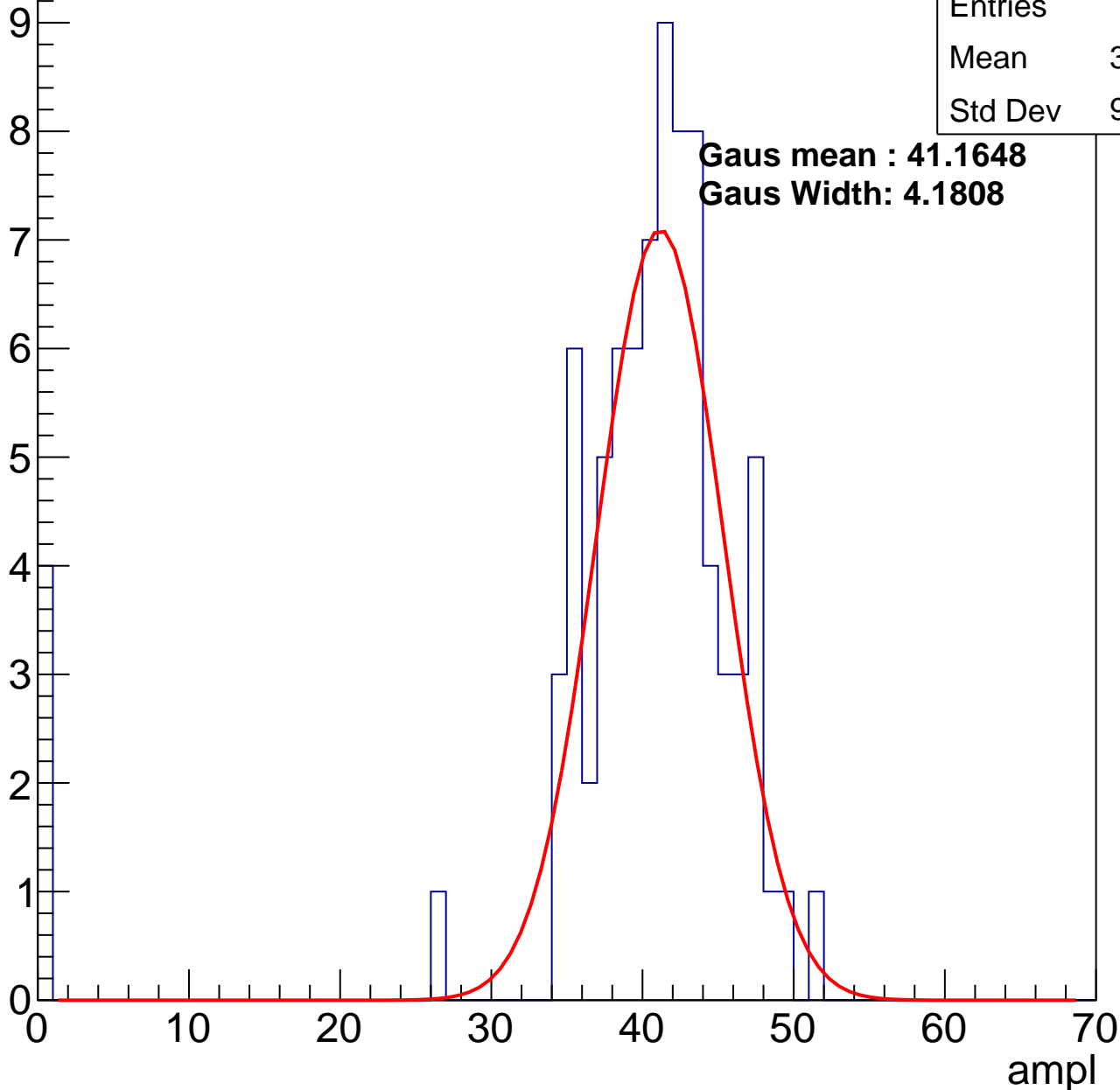
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	83
Mean	38.77
Std Dev	9.636

**Gaus mean : 41.1648**

**Gaus Width: 4.1808**

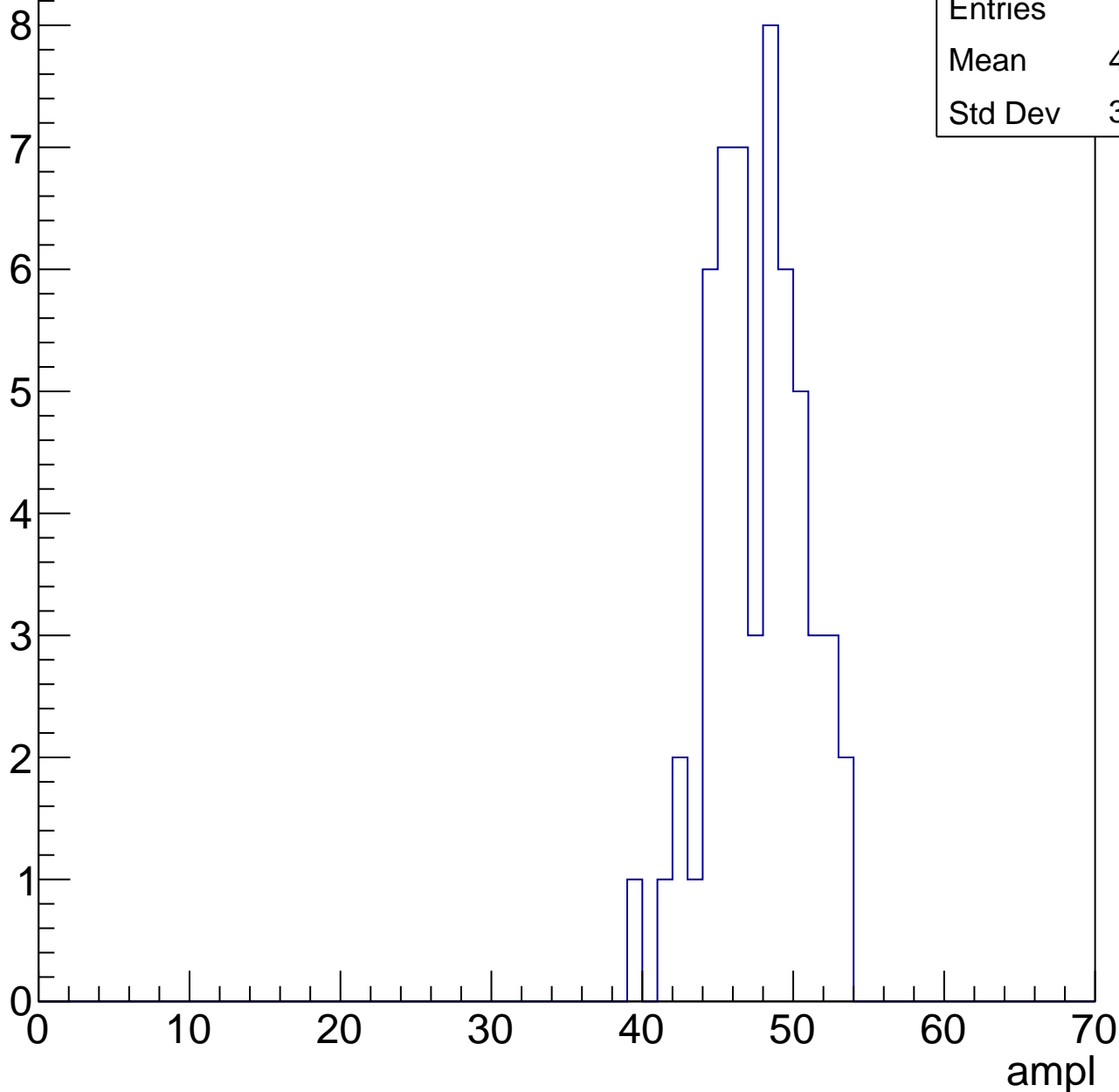


# B1L103S, U3-ch98, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	55
Mean	47.13
Std Dev	3.093

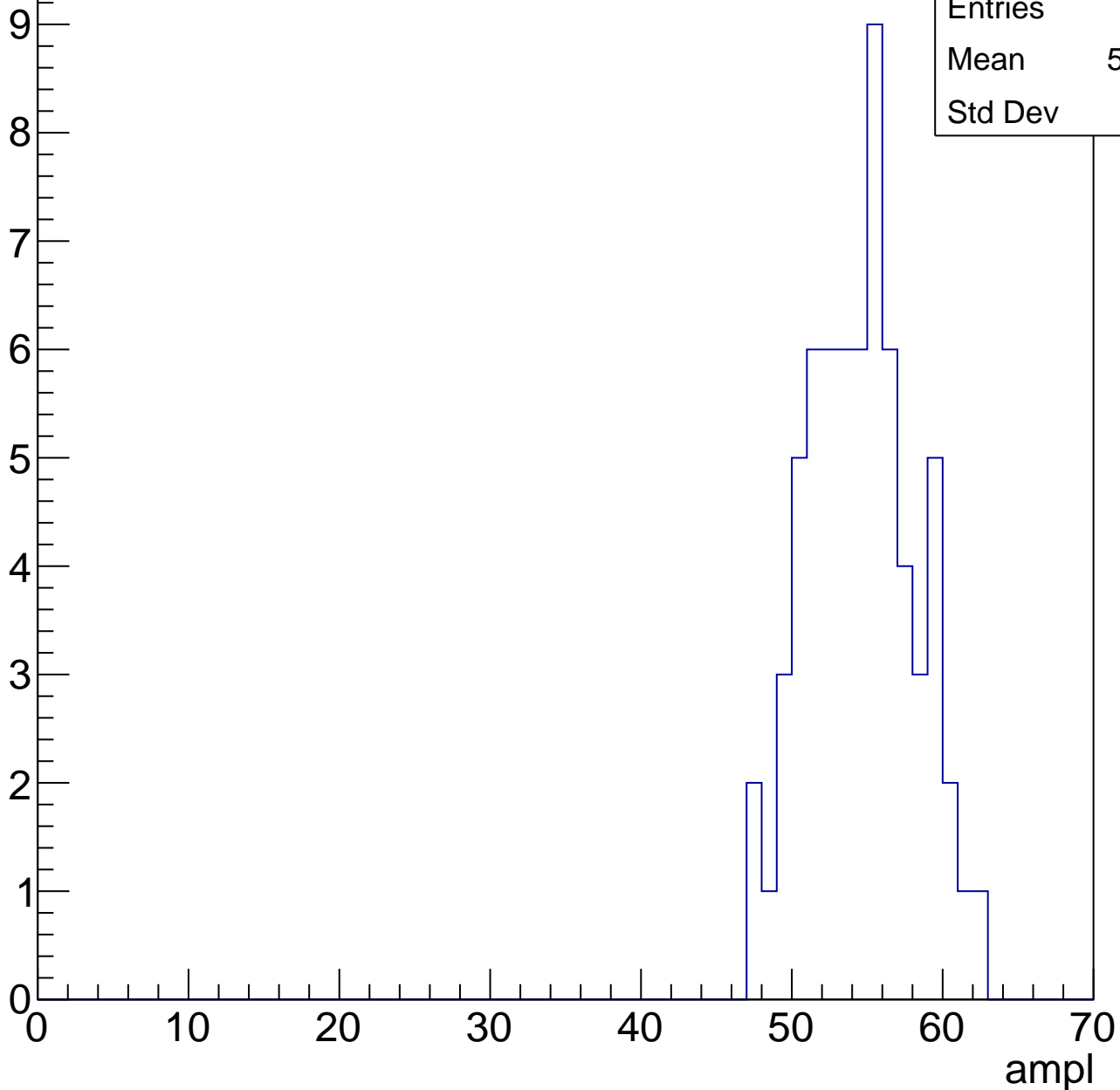


# B1L103S, U3-ch98, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	54.09
Std Dev	3.48

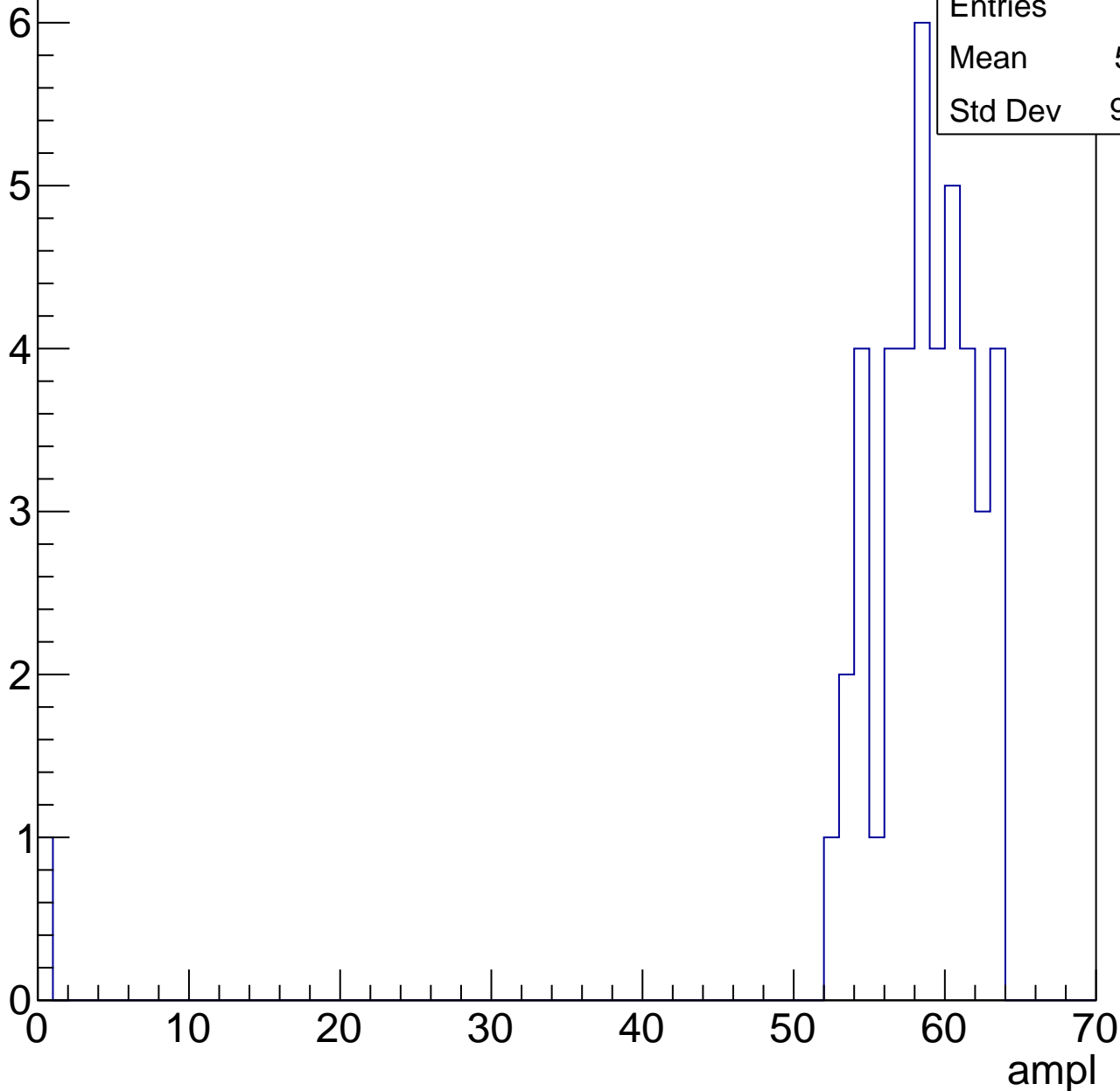


# B1L103S, U3-ch98, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	43
Mean	56.91
Std Dev	9.276

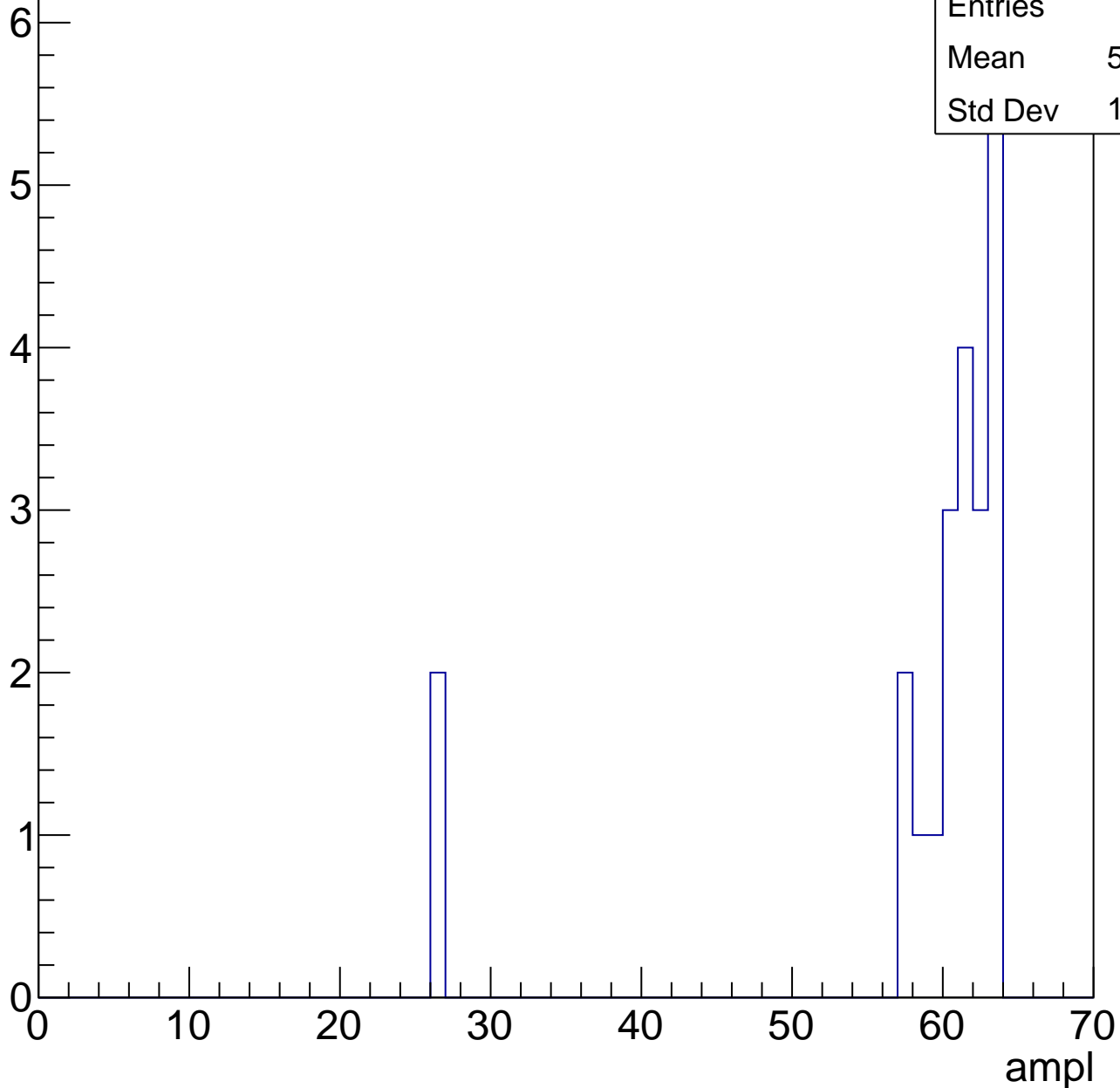


# B1L103S, U3-ch98, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	22
Mean	57.77
Std Dev	10.22

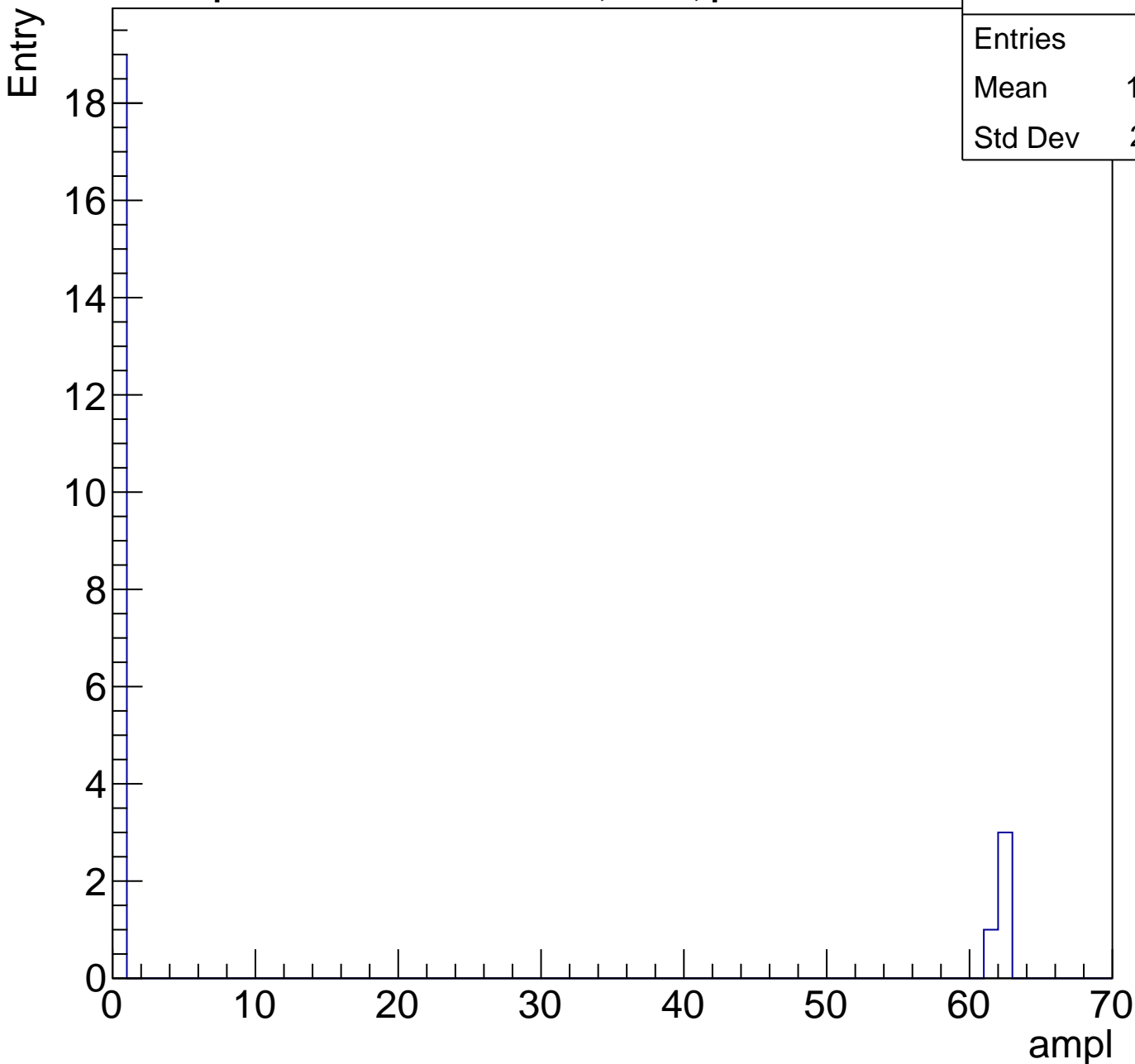




# B1L103S, U3-ch98, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	23
Mean	10.74
Std Dev	23.41



# B1L103S, U3-ch99, adc0

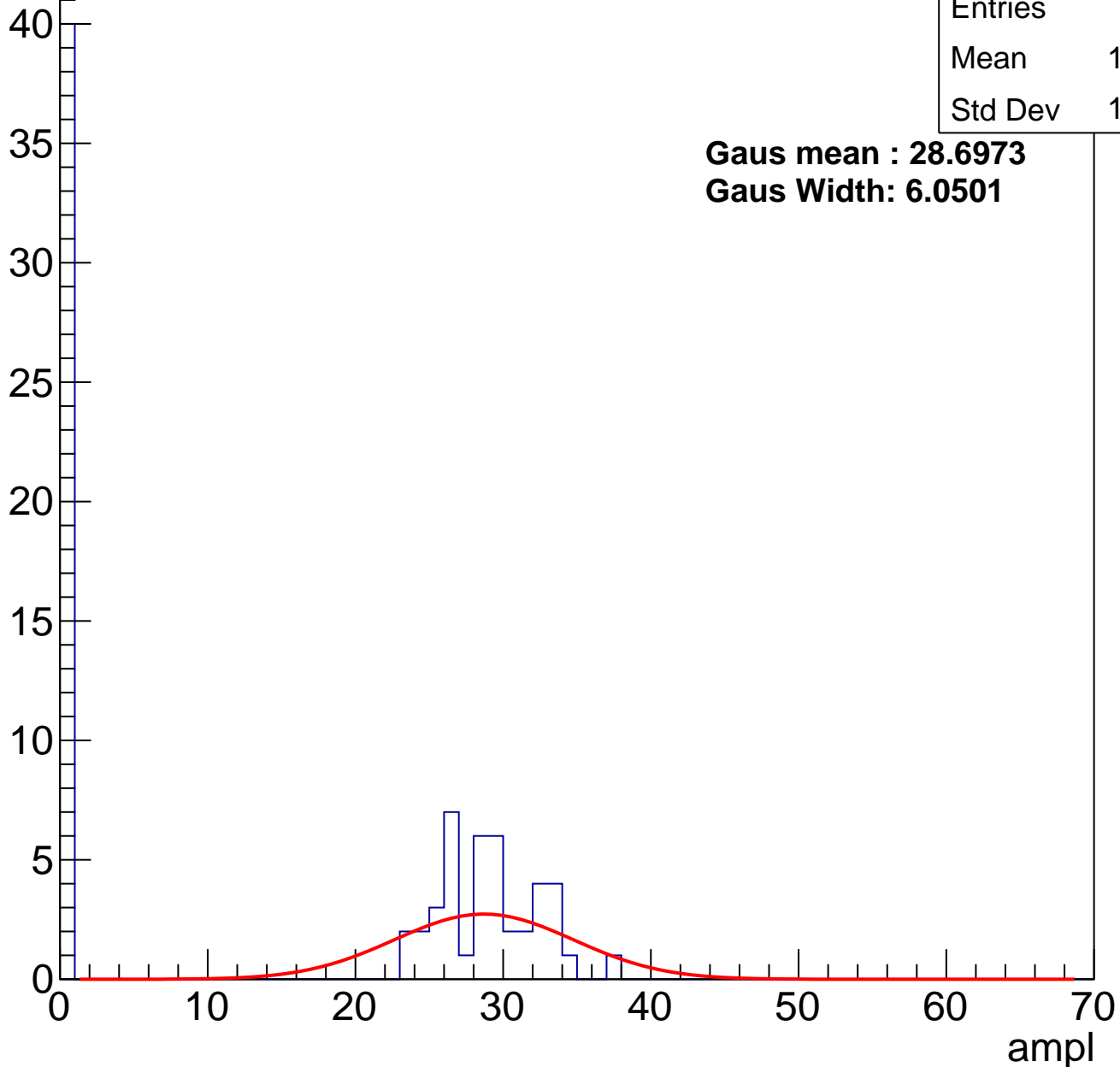
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	81
Mean	14.48
Std Dev	14.49

**Gaus mean : 28.6973**

**Gaus Width: 6.0501**

Entry



# B1L103S, U3-ch99, adc1

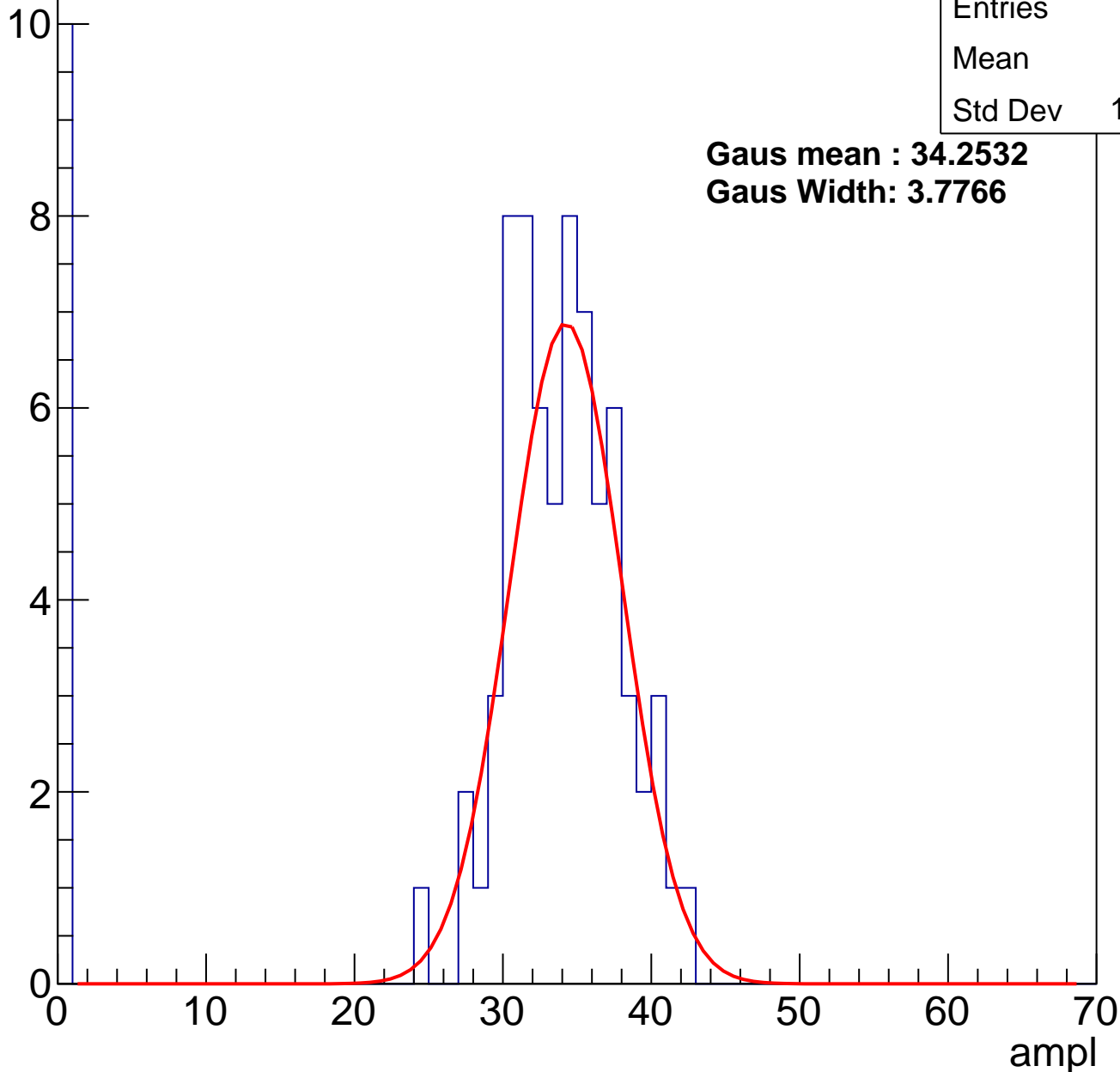
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	80
Mean	29.4
Std Dev	11.62

**Gaus mean : 34.2532**

**Gaus Width: 3.7766**

Entry



# B1L103S, U3-ch99, adc2

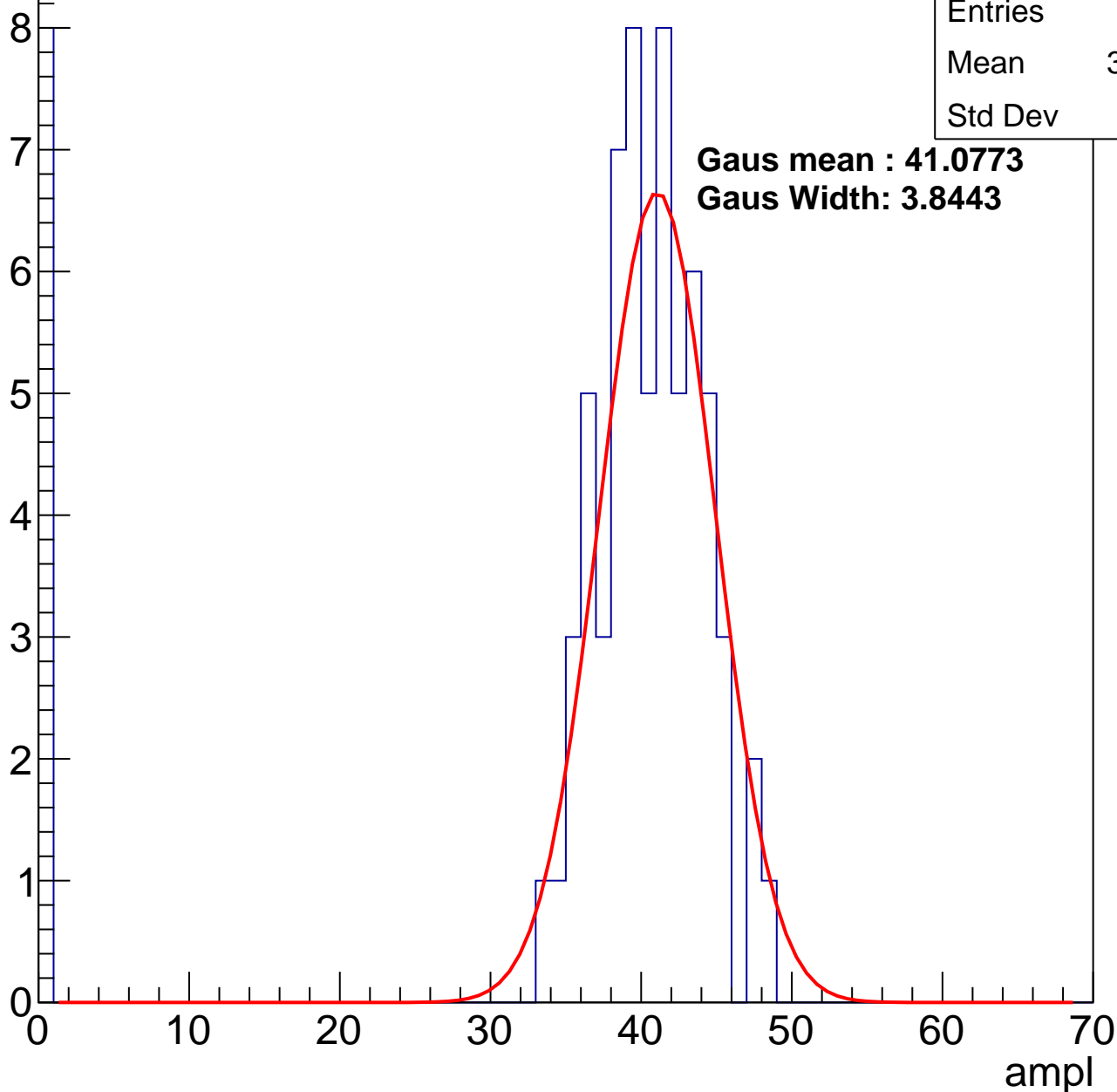
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	71
Mean	35.69
Std Dev	13.1

**Gaus mean : 41.0773**

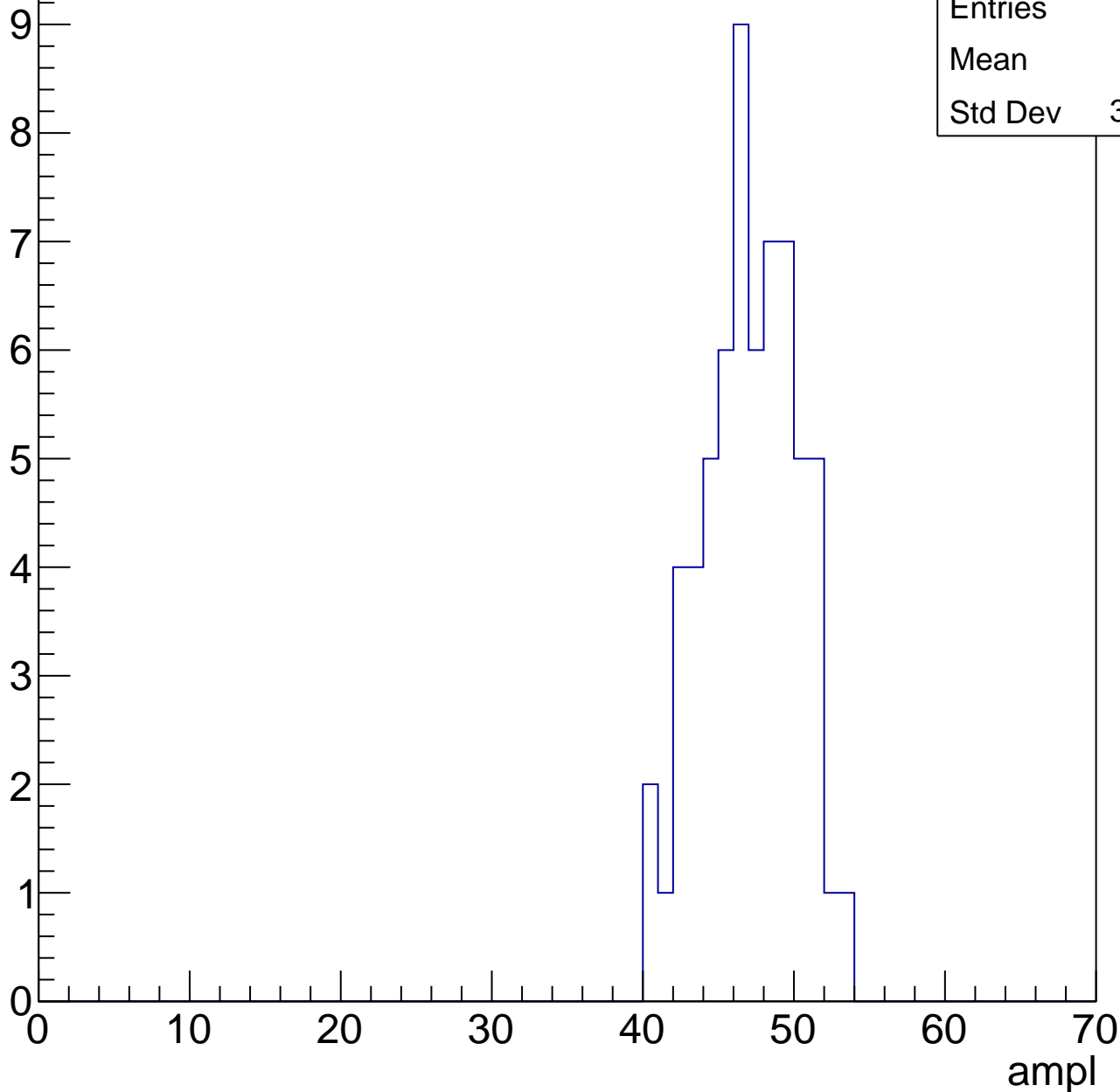
**Gaus Width: 3.8443**



# B1L103S, U3-ch99, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



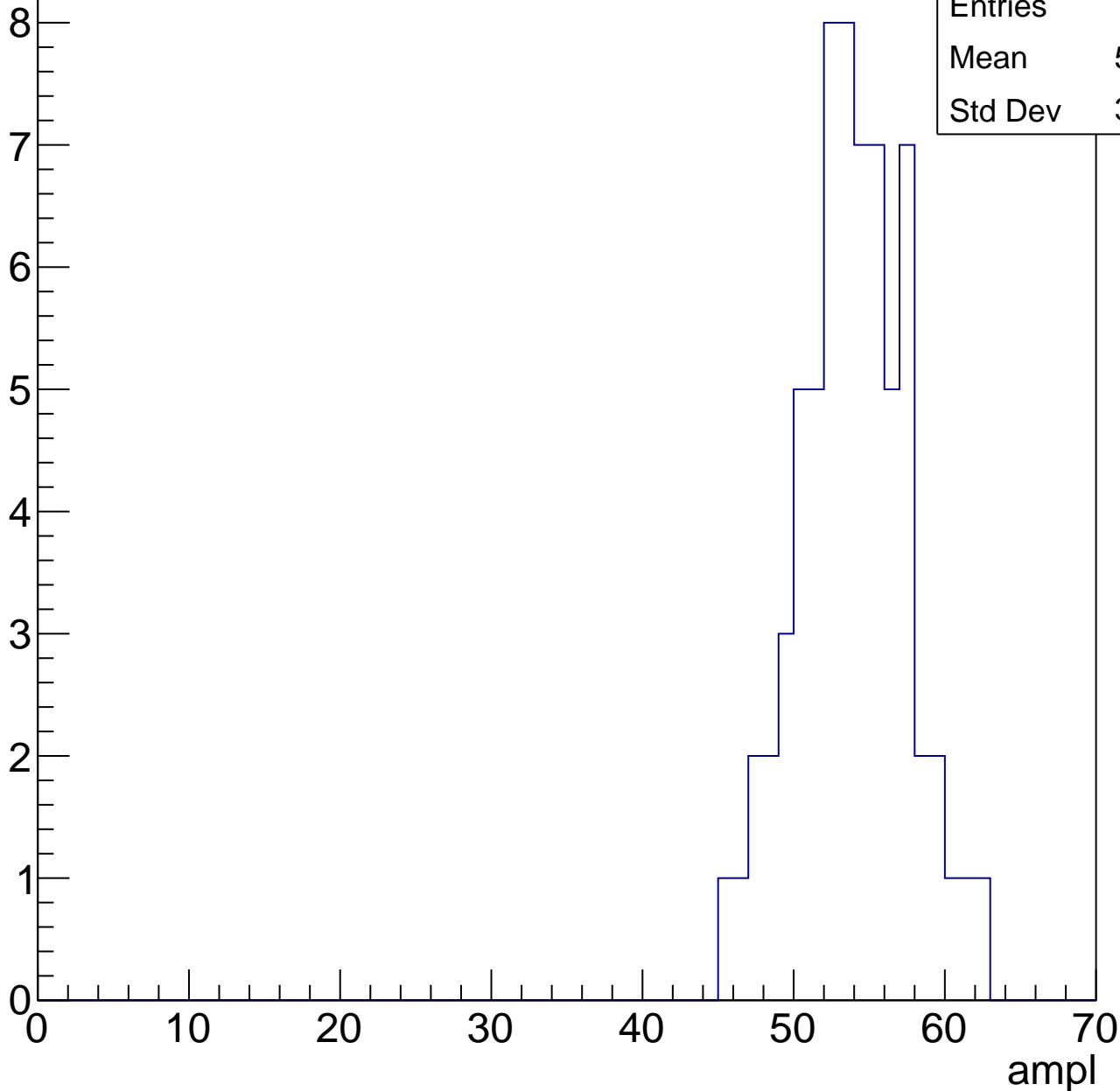
Entries	63
Mean	46.6
Std Dev	3.053

# B1L103S, U3-ch99, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	53.41
Std Dev	3.541

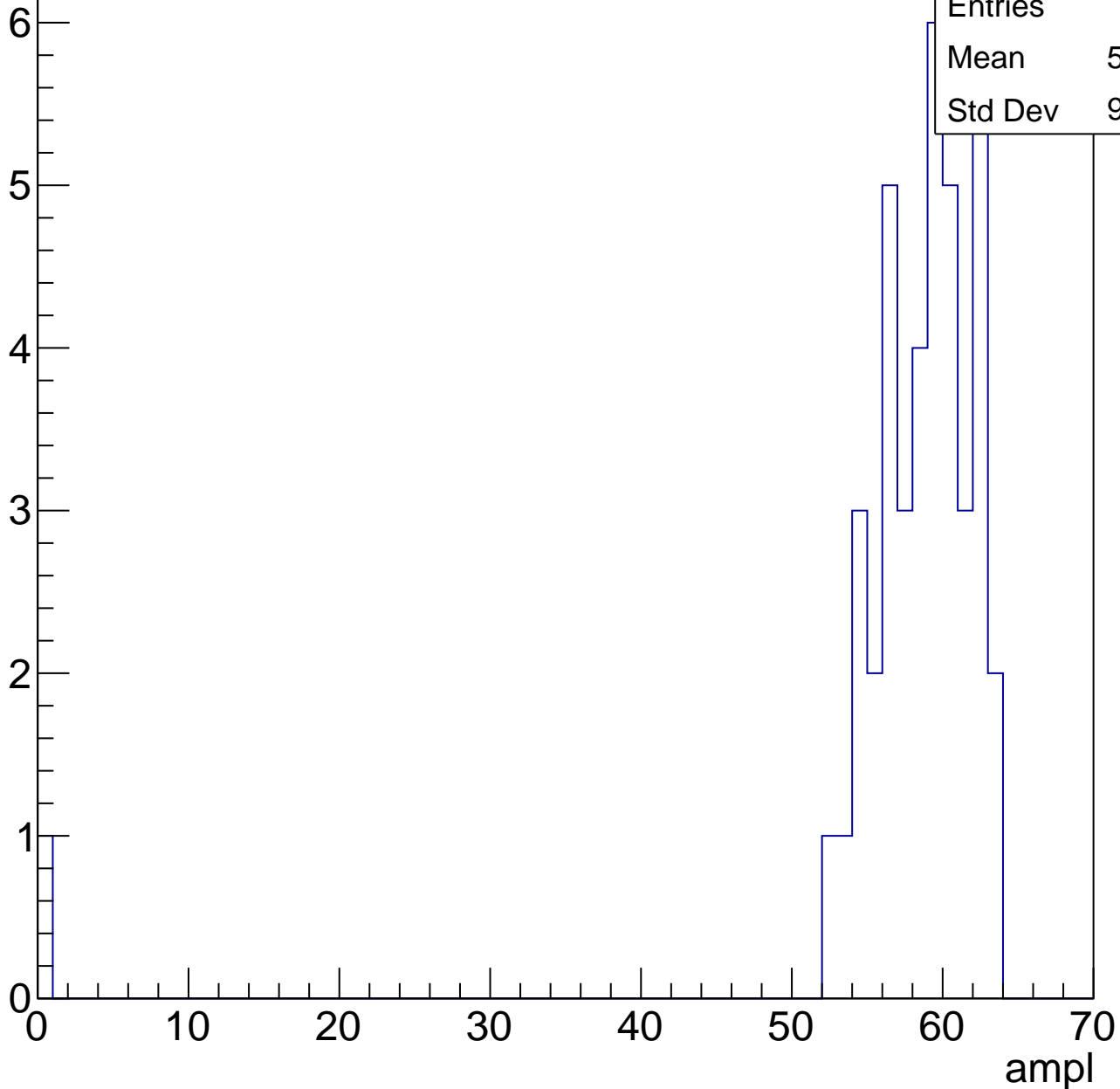


# B1L103S, U3-ch99, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	42
Mean	57.02
Std Dev	9.352

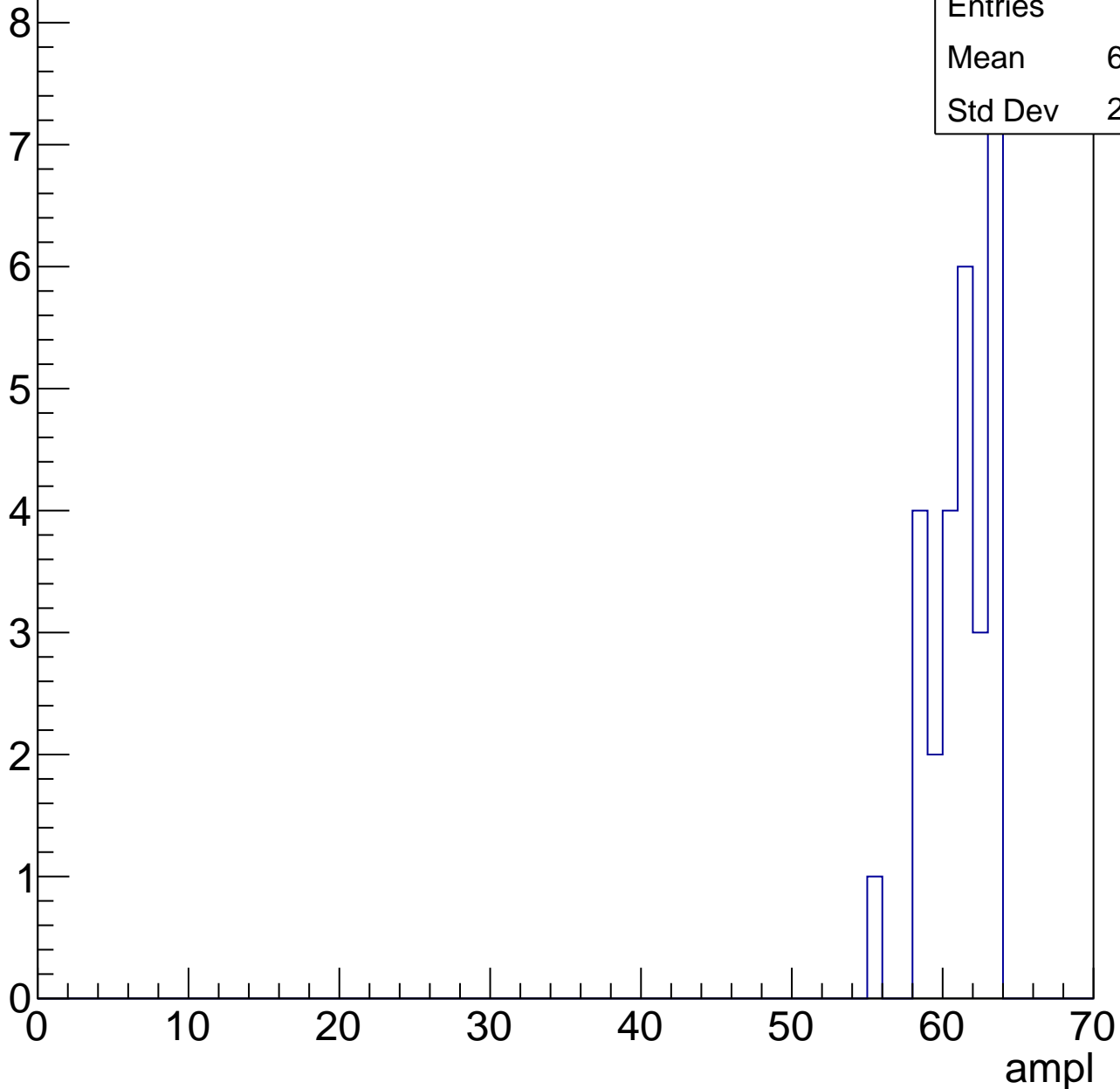


# B1L103S, U3-ch99, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	28
Mean	60.75
Std Dev	2.046





# B1L103S, U3-ch99, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Entries	19
Mean	0
Std Dev	0

ampl

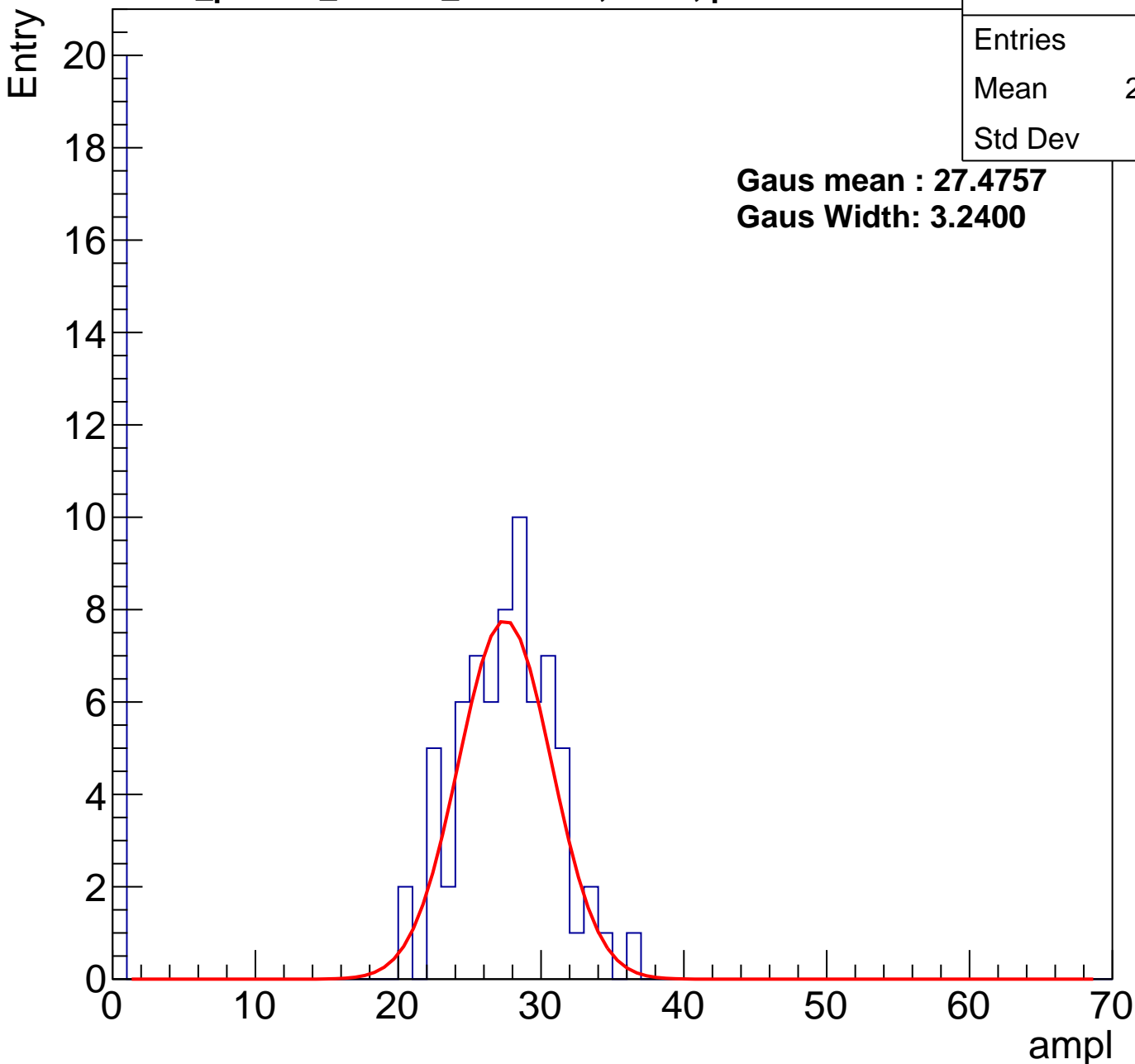
# B1L103S, U3-ch100, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	89
Mean	21.06
Std Dev	11.7

**Gaus mean : 27.4757**

**Gaus Width: 3.2400**



# B1L103S, U3-ch100, adc1

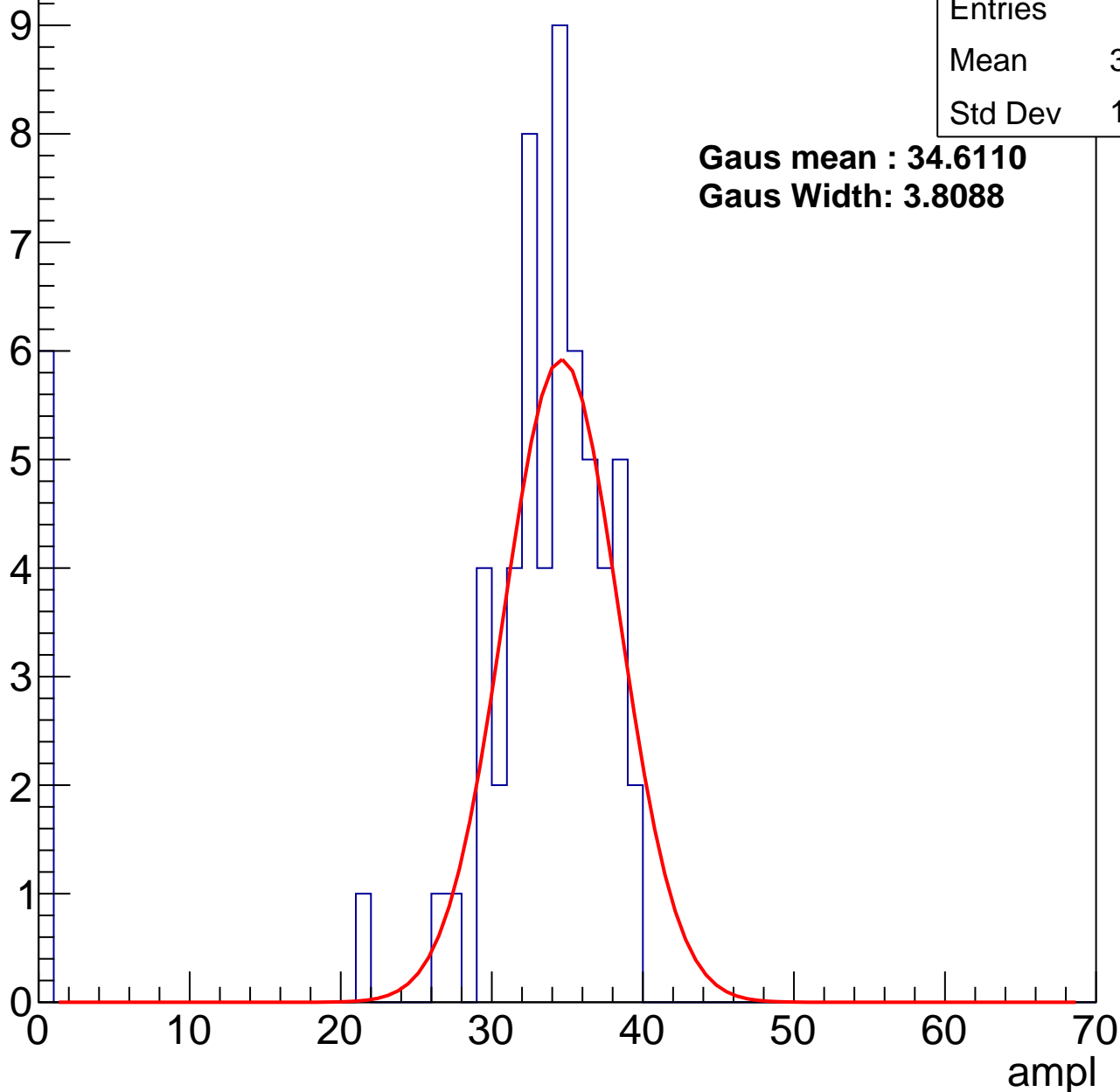
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	30.23
Std Dev	10.42

**Gaus mean : 34.6110**

**Gaus Width: 3.8088**



# B1L103S, U3-ch100, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	69
Mean	33.49
Std Dev	14.29

**Gaus mean : 39.2711**

**Gaus Width: 4.4896**

Entry

10

8

6

4

2

0

0

10

20

30

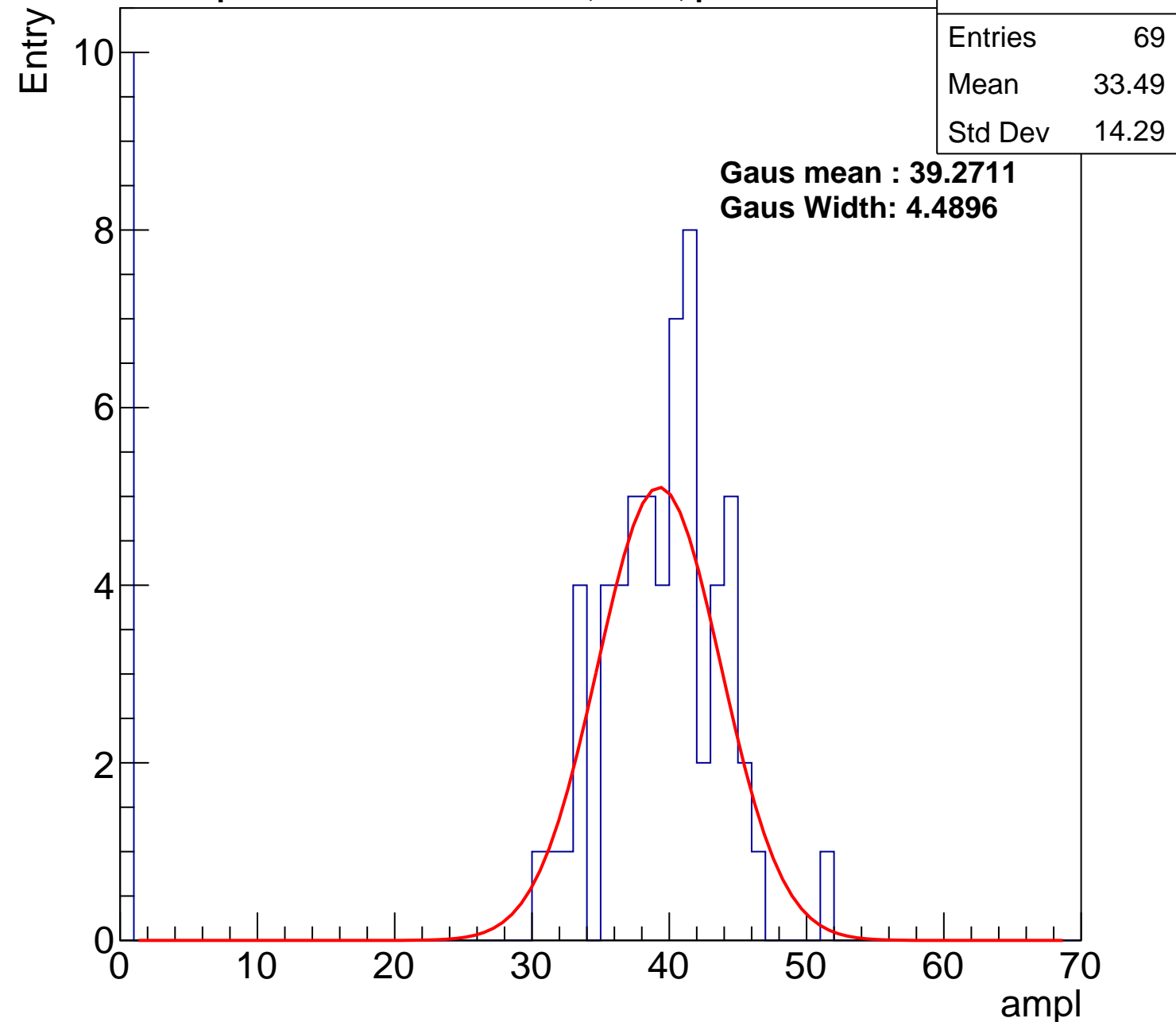
40

50

60

70

ampl

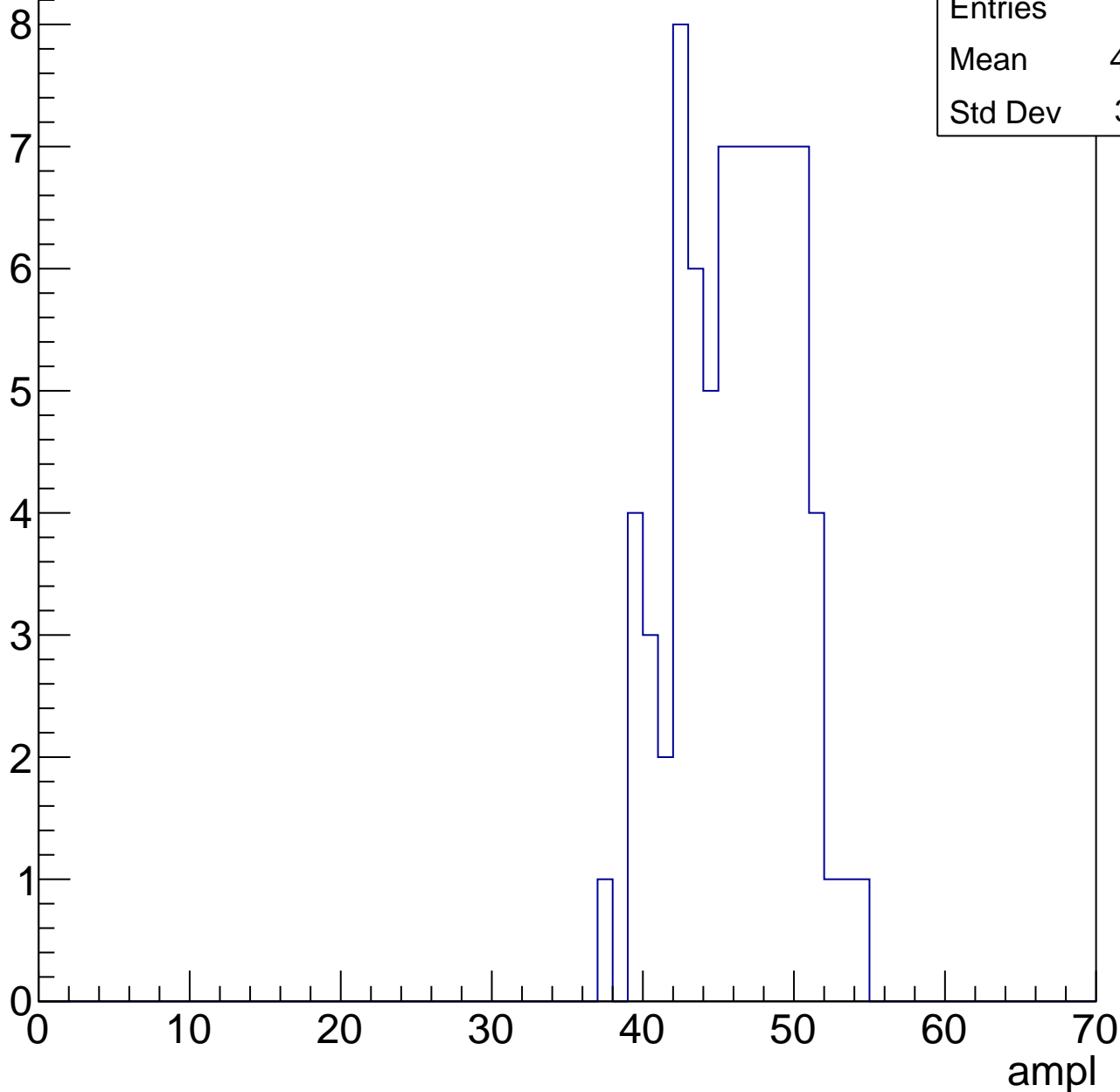


# B1L103S, U3-ch100, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	78
Mean	45.73
Std Dev	3.751

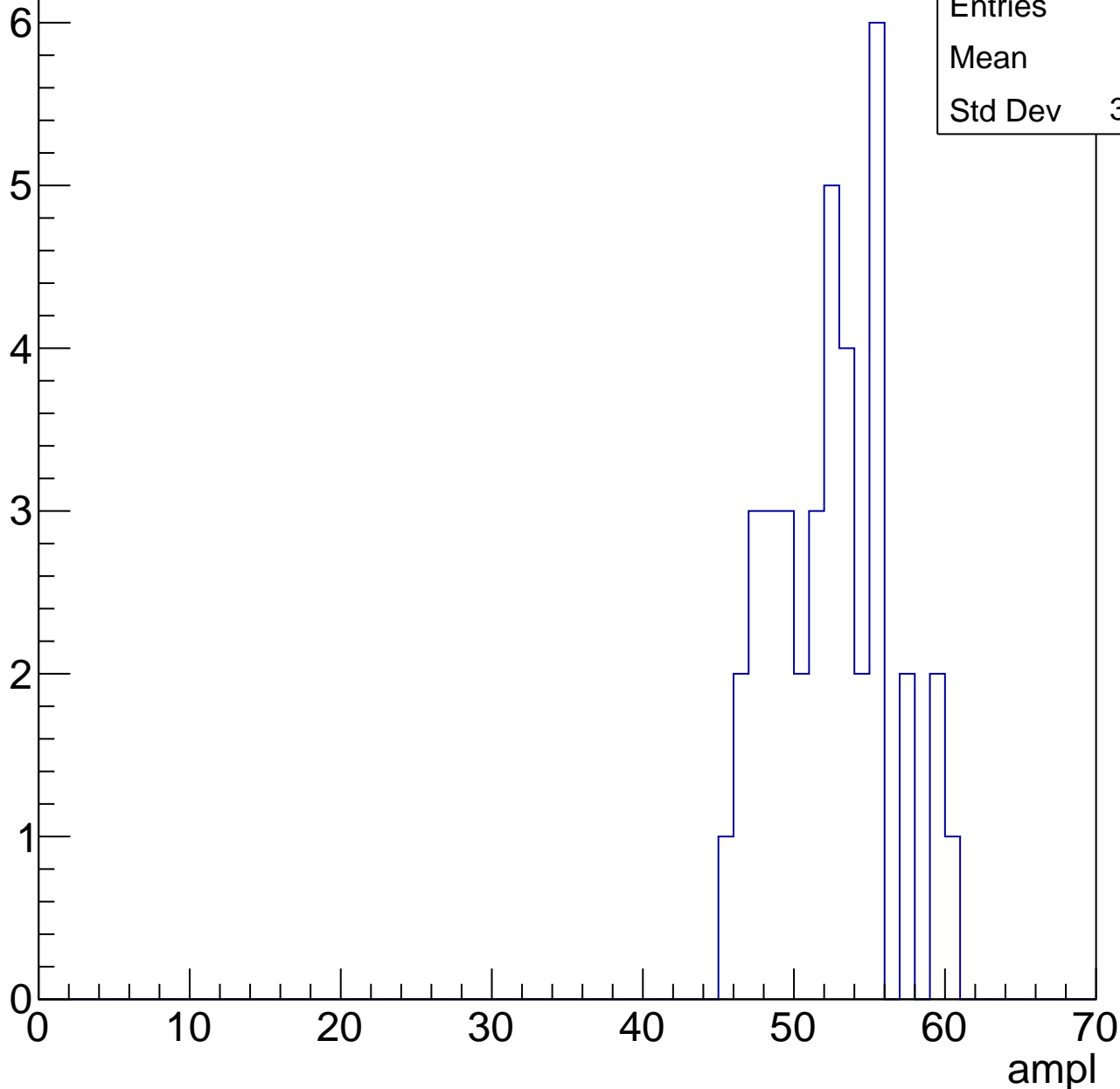


# B1L103S, U3-ch100, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	39
Mean	51.9
Std Dev	3.788



# B1L103S, U3-ch100, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	73
Mean	56.29
Std Dev	7.418

Entry

10

8

6

4

2

0

0

10

20

30

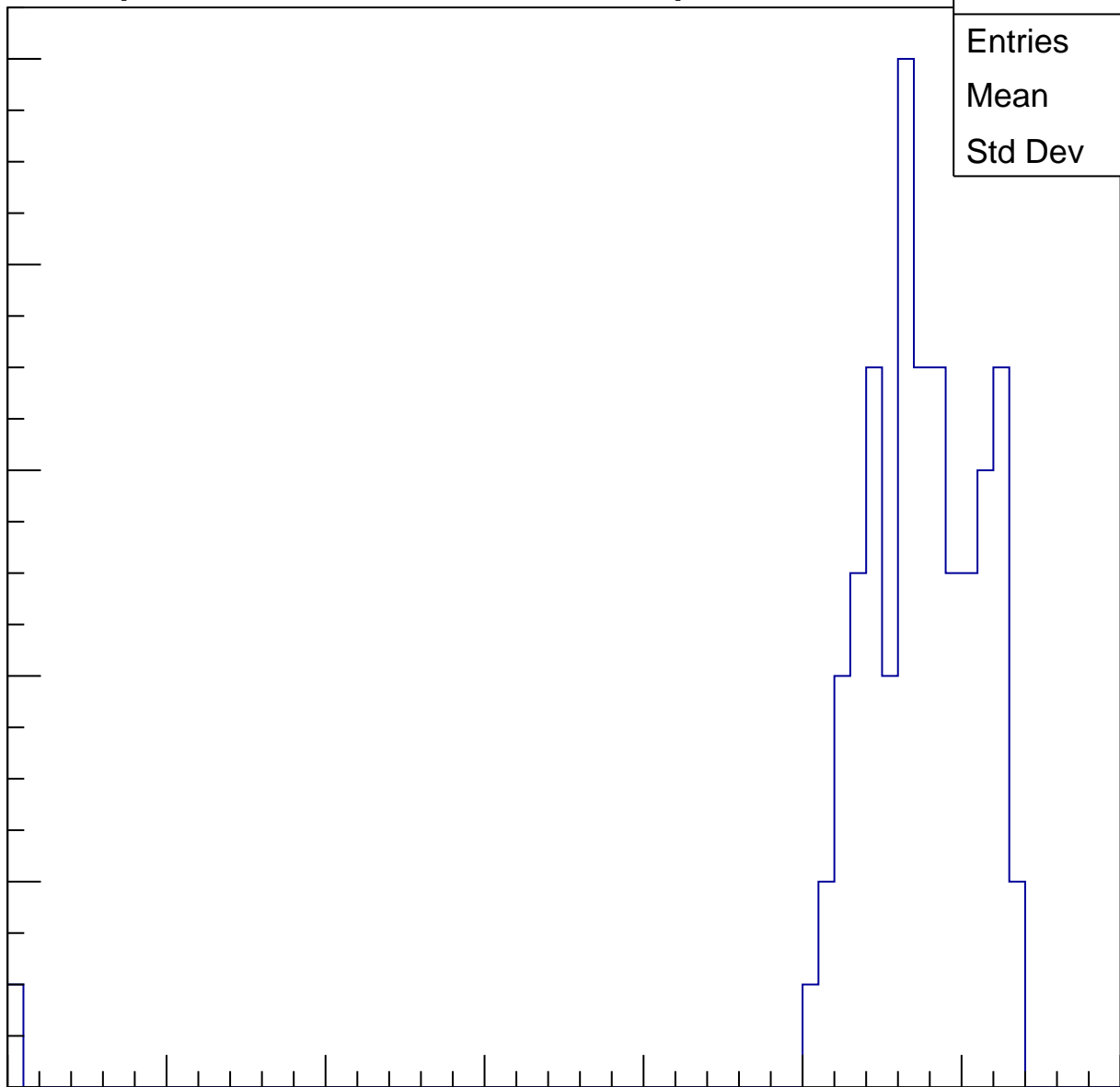
40

50

60

70

ampl

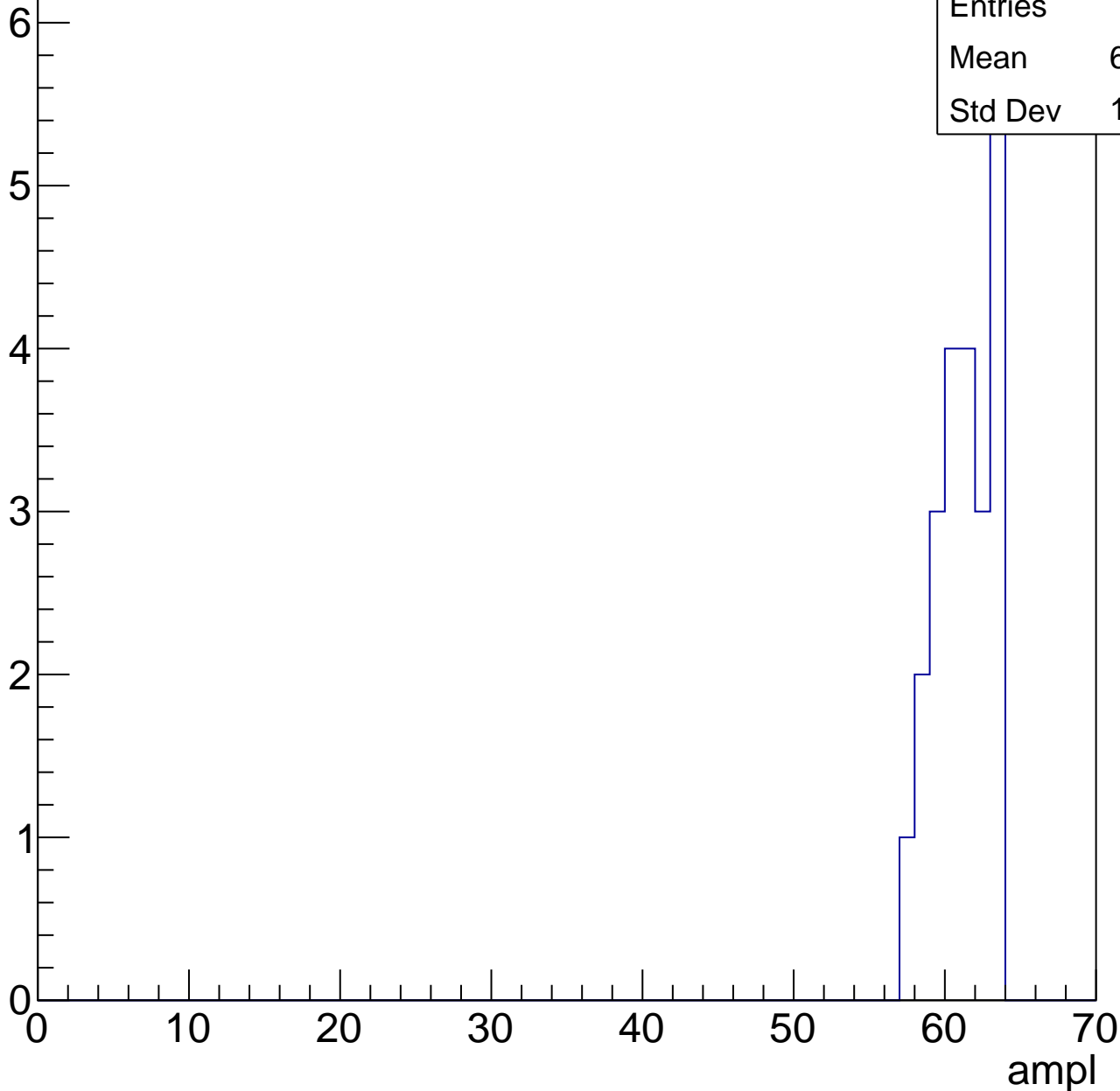


# B1L103S, U3-ch100, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	23
Mean	60.78
Std Dev	1.817



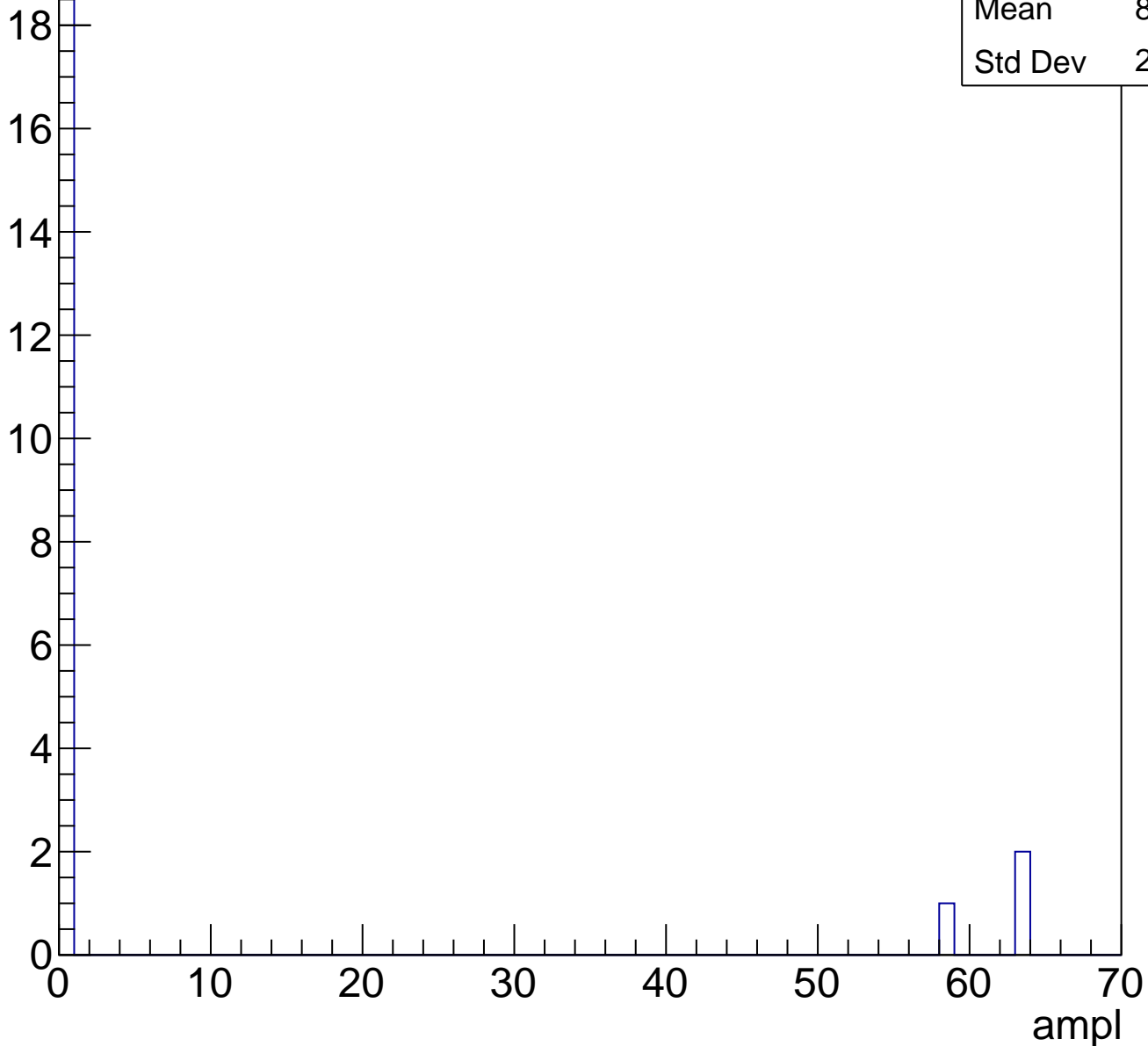


# B1L103S, U3-ch100, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	22
Mean	8.364
Std Dev	21.07

Entry



# B1L103S, U3-ch101, adc0

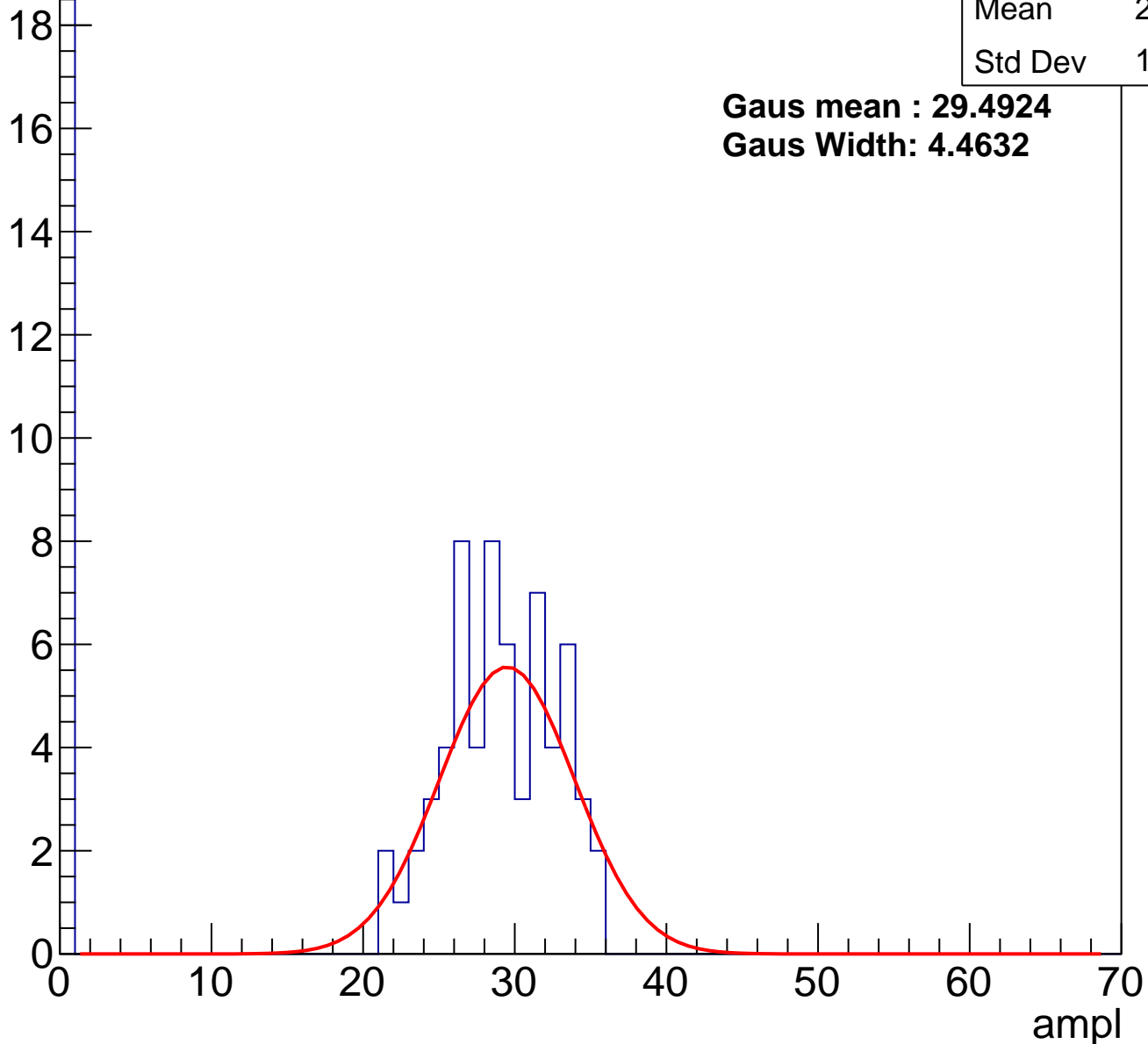
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	82
Mean	21.96
Std Dev	12.45

**Gaus mean : 29.4924**

**Gaus Width: 4.4632**

Entry



# B1L103S, U3-ch101, adc1

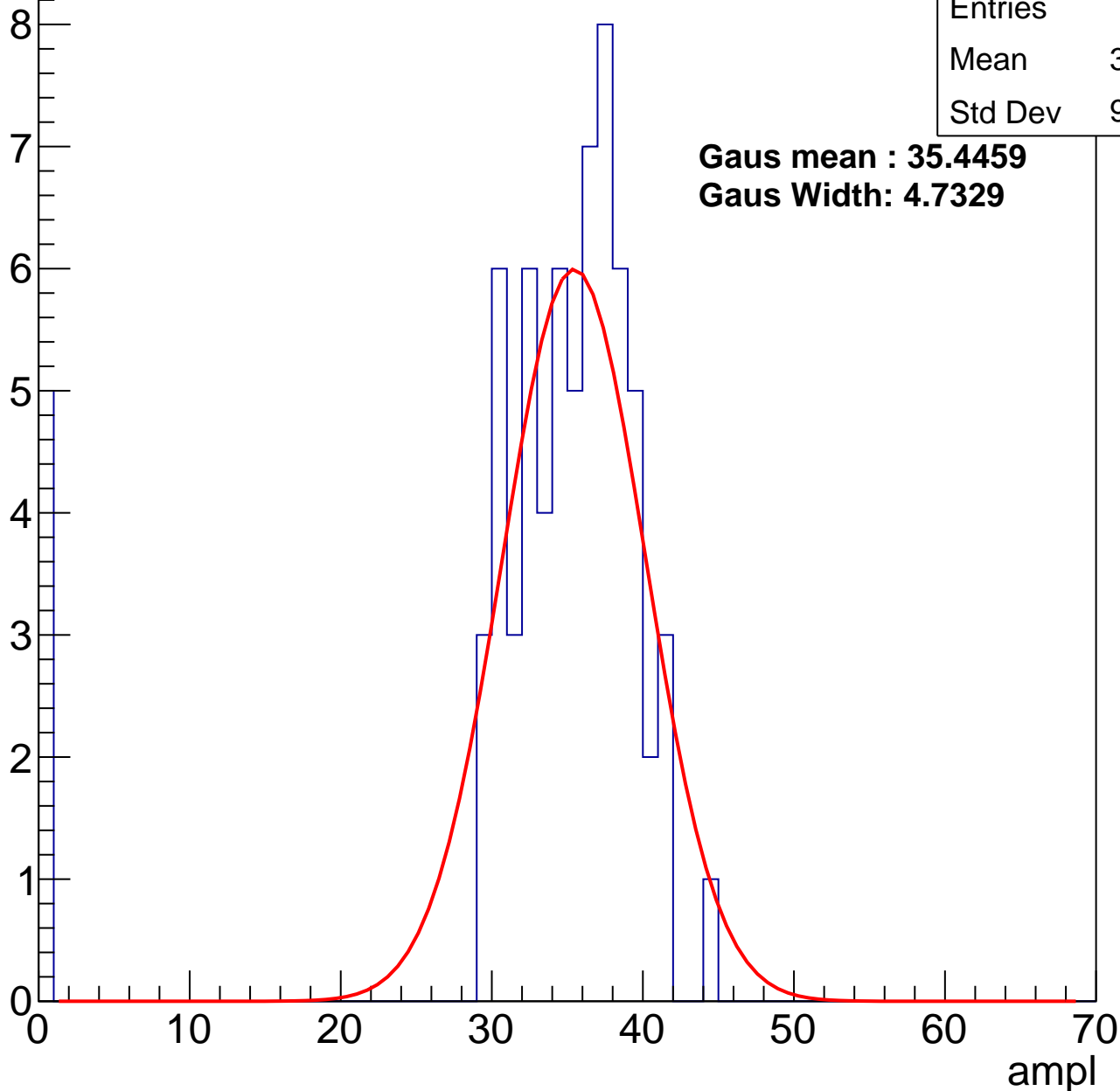
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	32.59
Std Dev	9.644

**Gaus mean : 35.4459**

**Gaus Width: 4.7329**



# B1L103S, U3-ch101, adc2

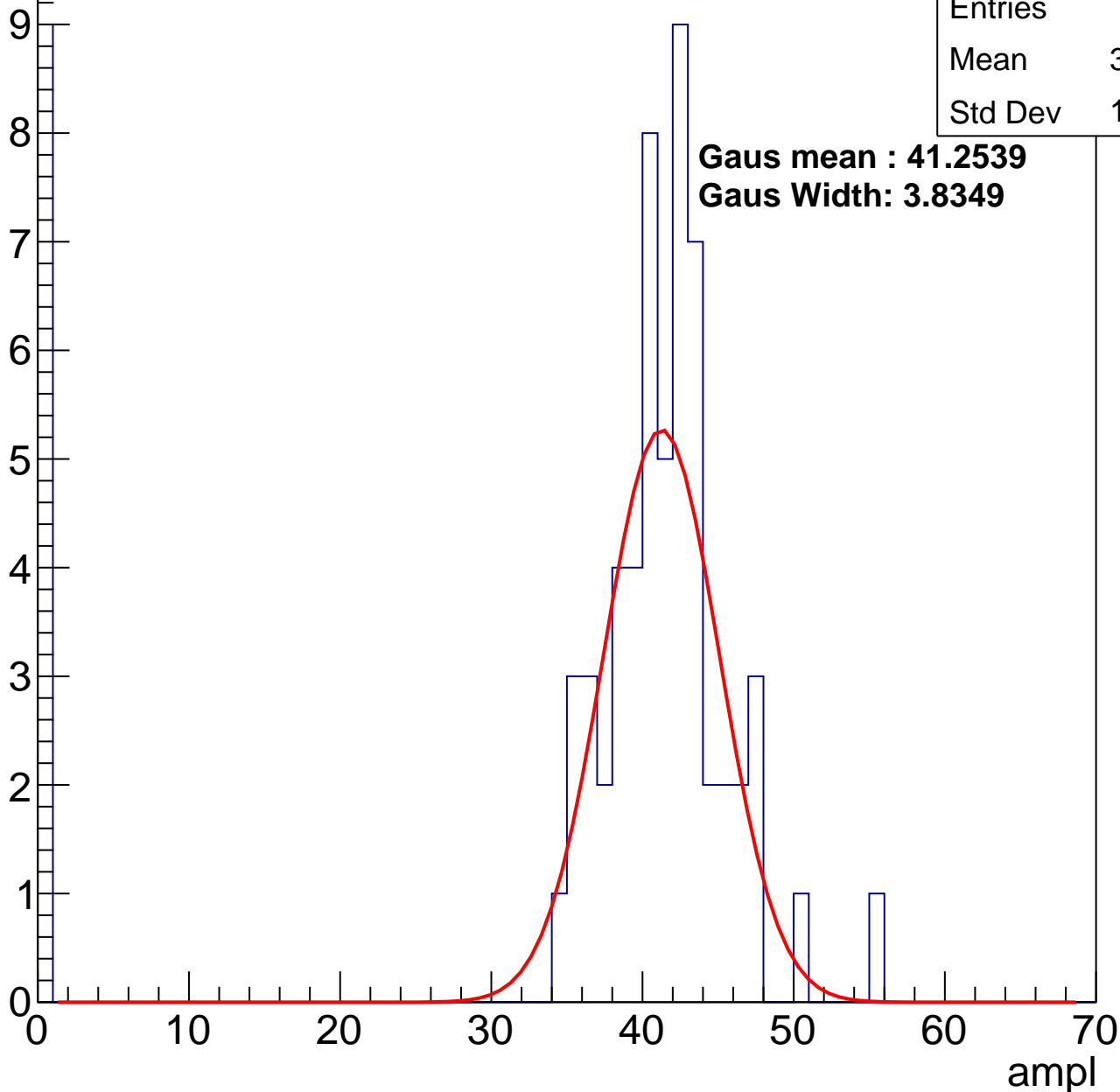
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	35.59
Std Dev	14.59

**Gaus mean : 41.2539**

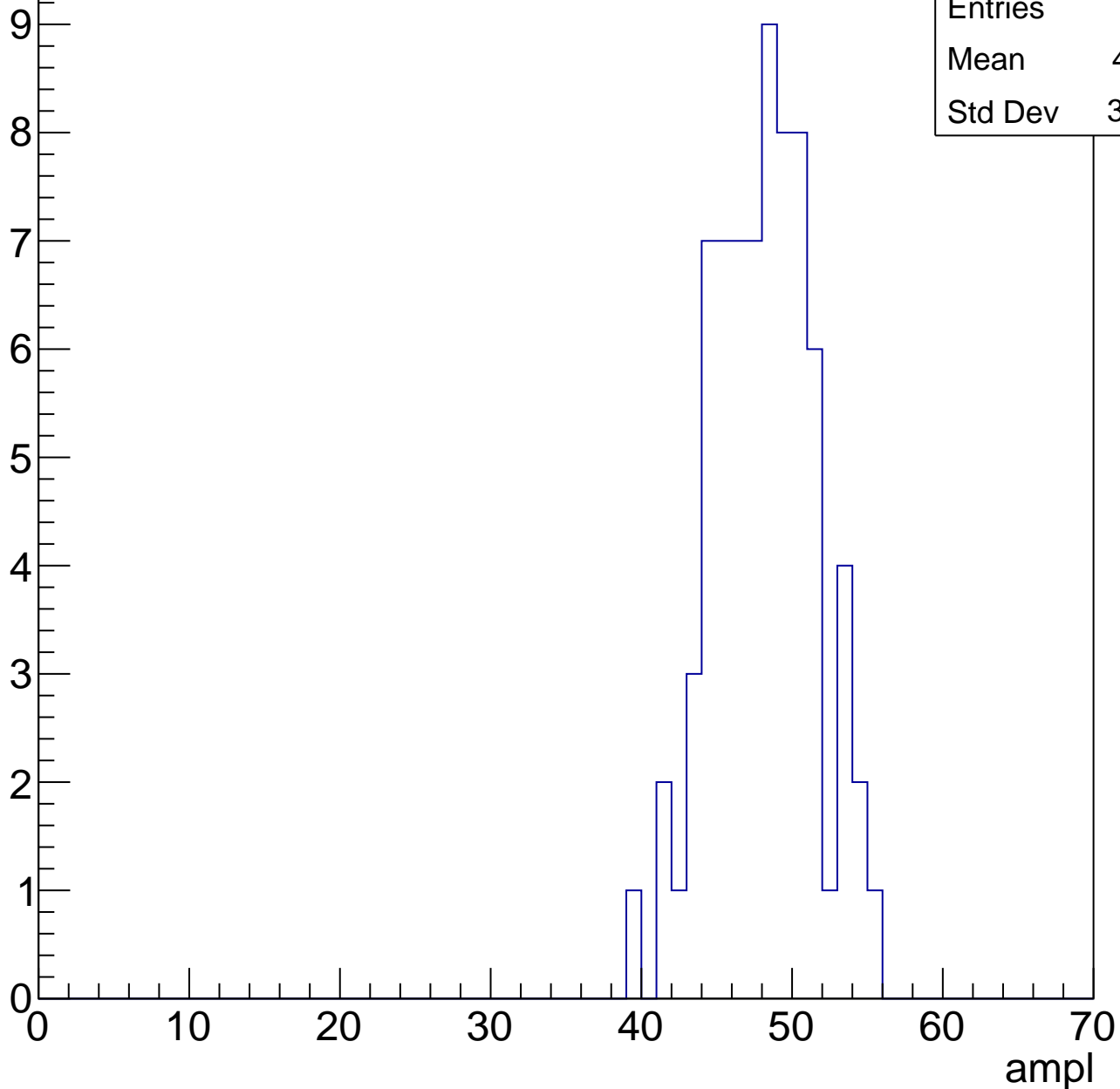
**Gaus Width: 3.8349**



# B1L103S, U3-ch101, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



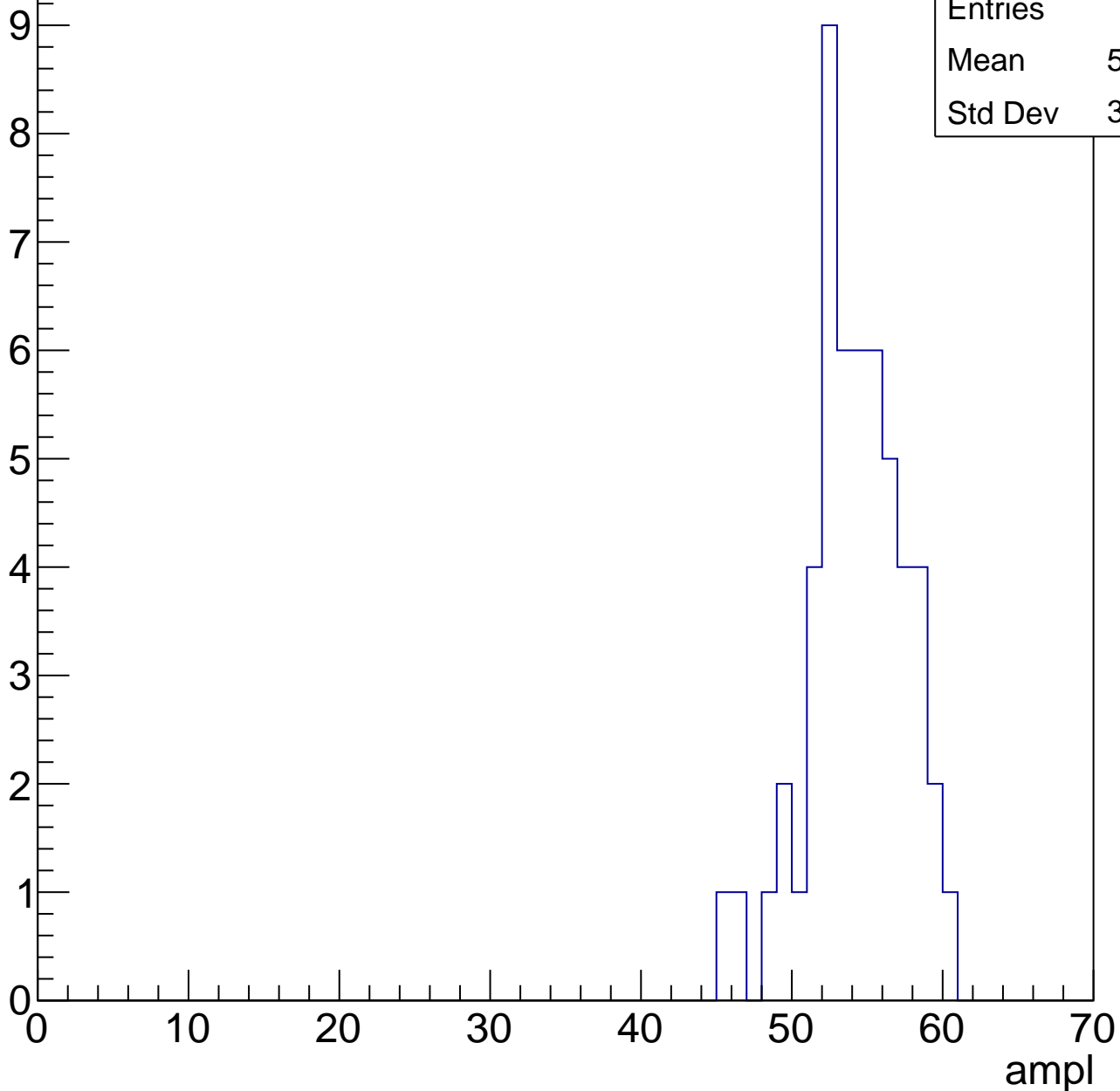
Entries	74
Mean	47.61
Std Dev	3.328

# B1L103S, U3-ch101, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	53
Mean	53.75
Std Dev	3.174



# B1L103S, U3-ch101, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	60
Mean	58.32
Std Dev	7.963

ampl

0

10

20

30

40

50

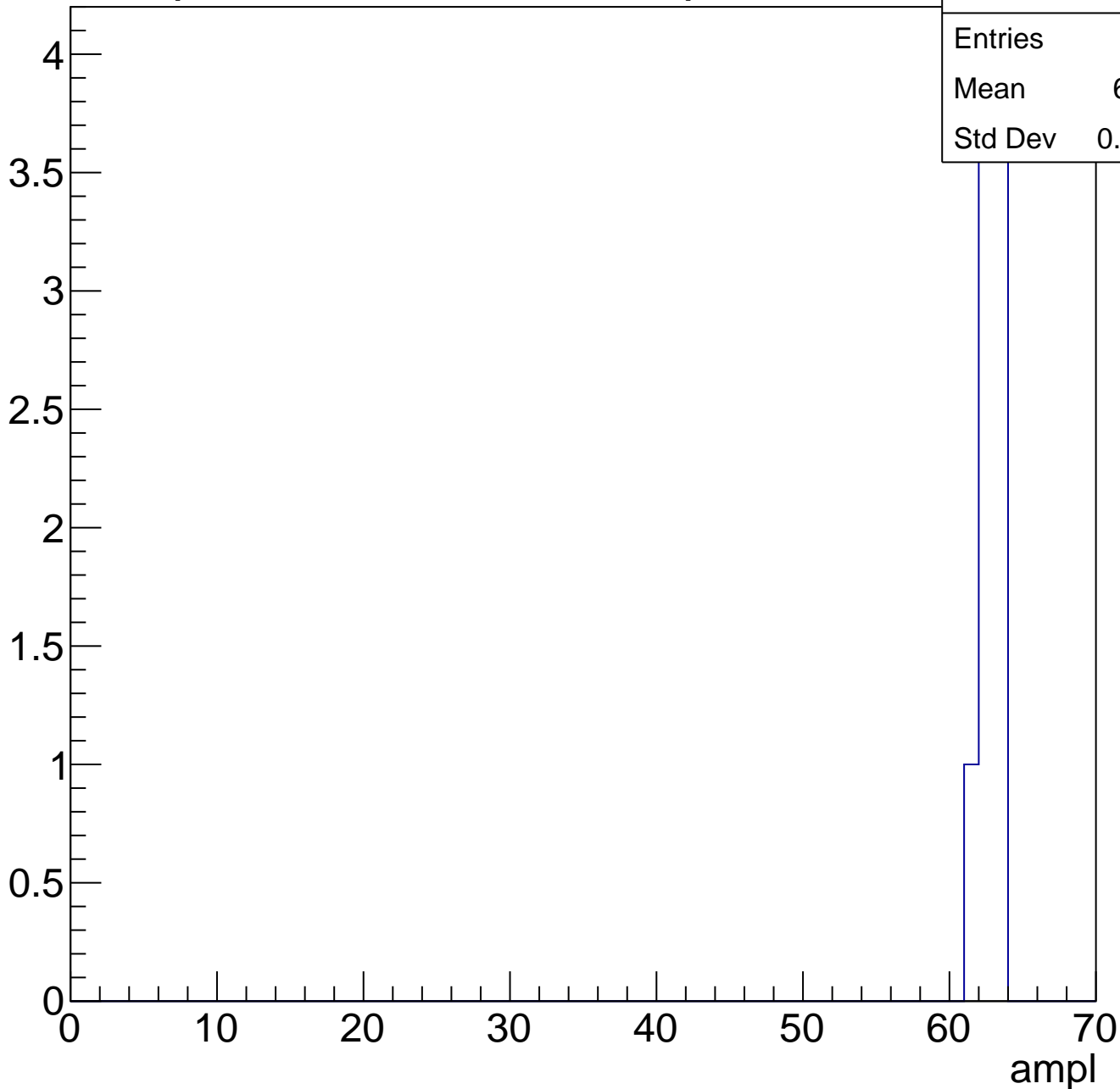
60

70

# B1L103S, U3-ch101, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U3-ch101, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U3-ch102, adc0

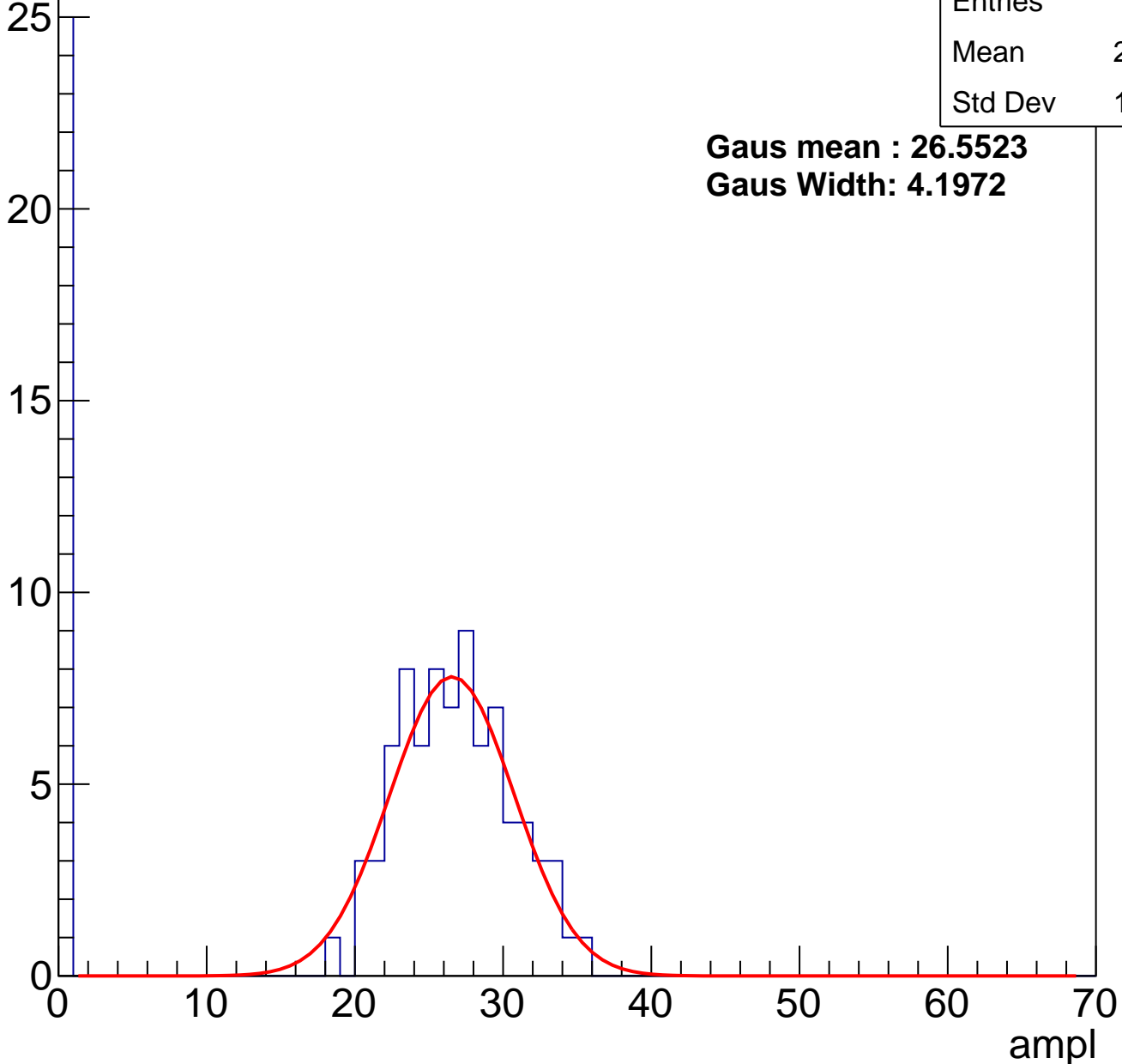
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	105
Mean	20.05
Std Dev	11.66

**Gaus mean : 26.5523**

**Gaus Width: 4.1972**

Entry



# B1L103S, U3-ch102, adc1

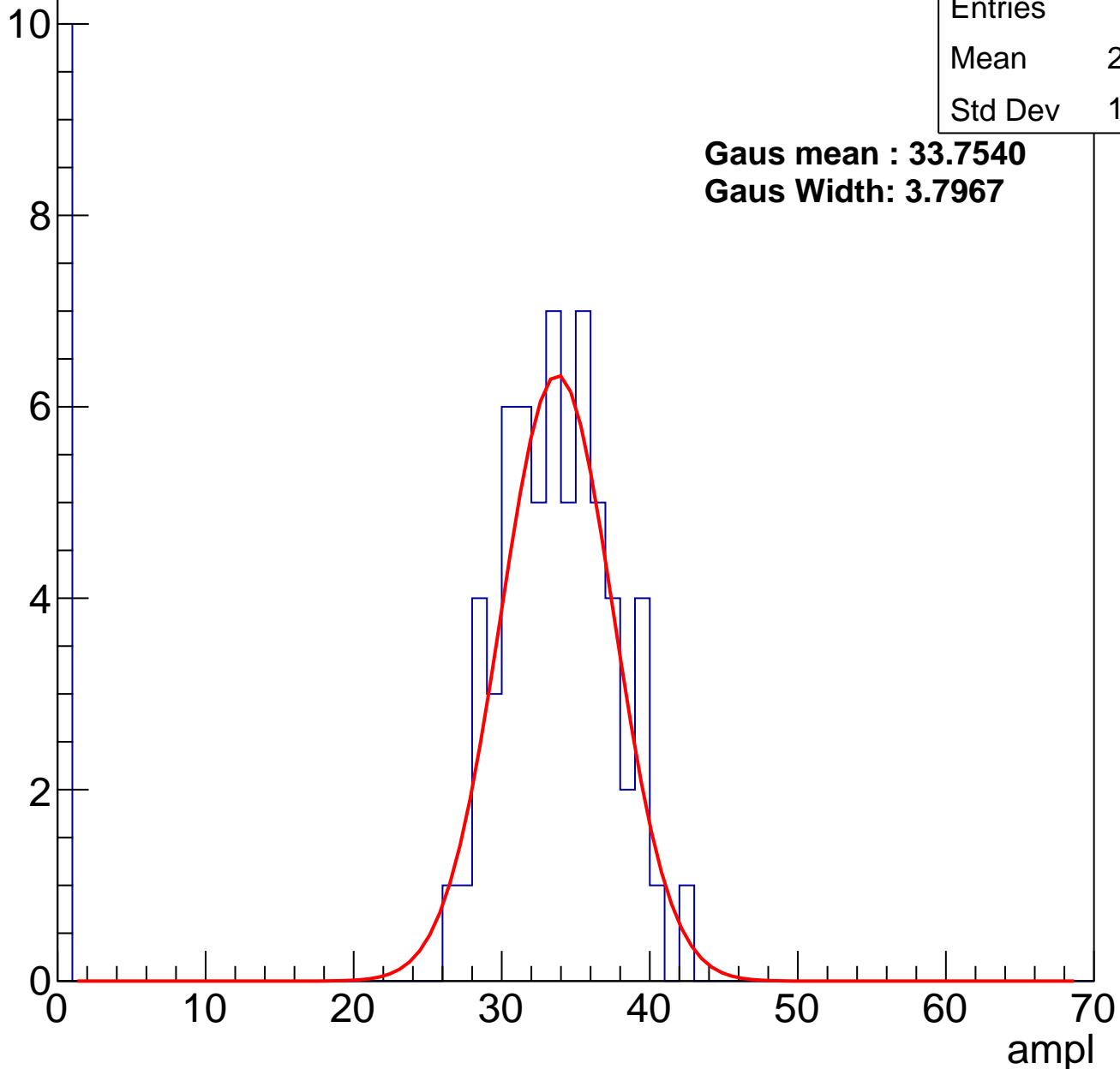
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	72
Mean	28.69
Std Dev	11.98

**Gaus mean : 33.7540**

**Gaus Width: 3.7967**

Entry



# B1L103S, U3-ch102, adc2

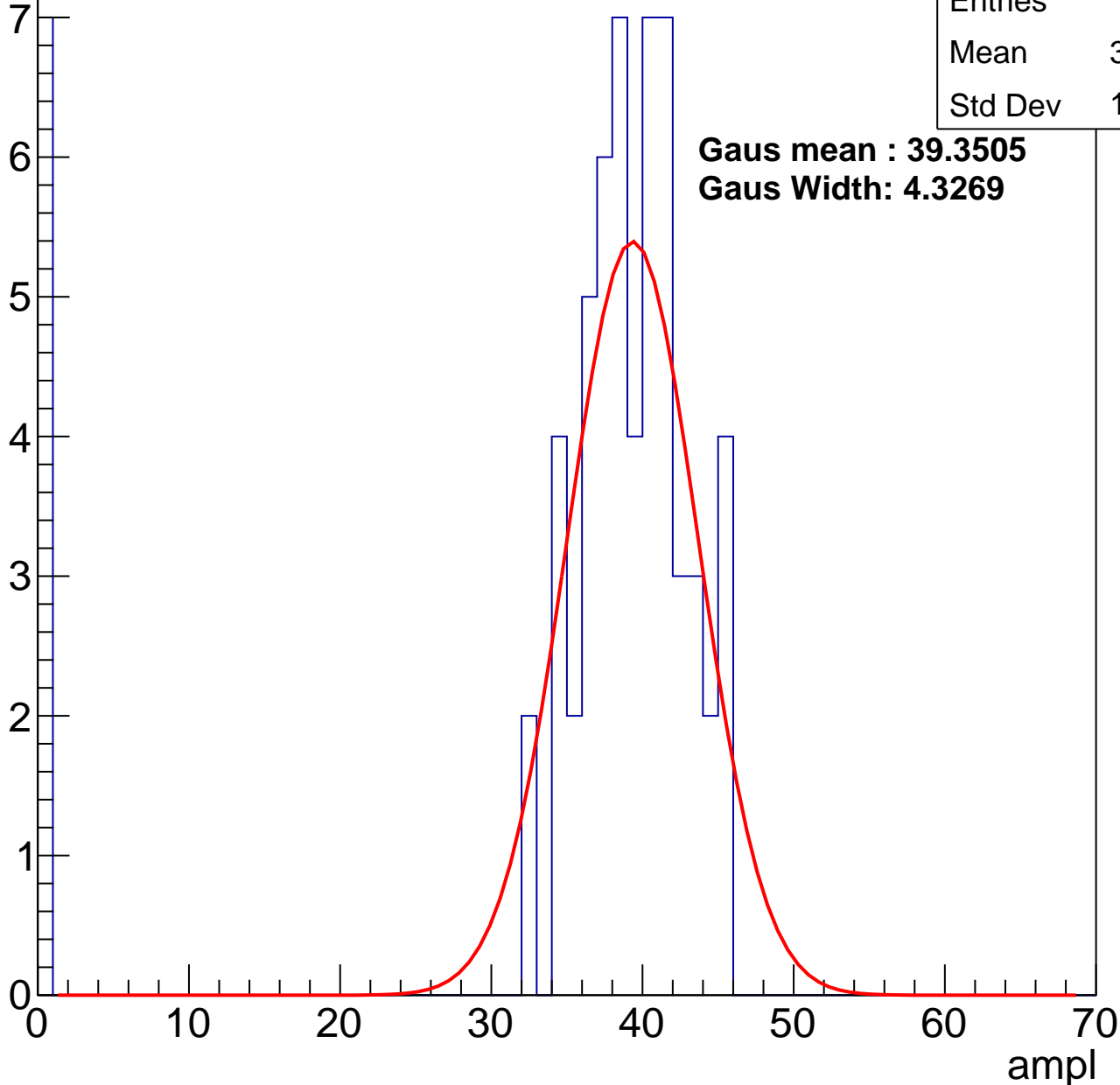
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	34.67
Std Dev	12.65

**Gaus mean : 39.3505**

**Gaus Width: 4.3269**

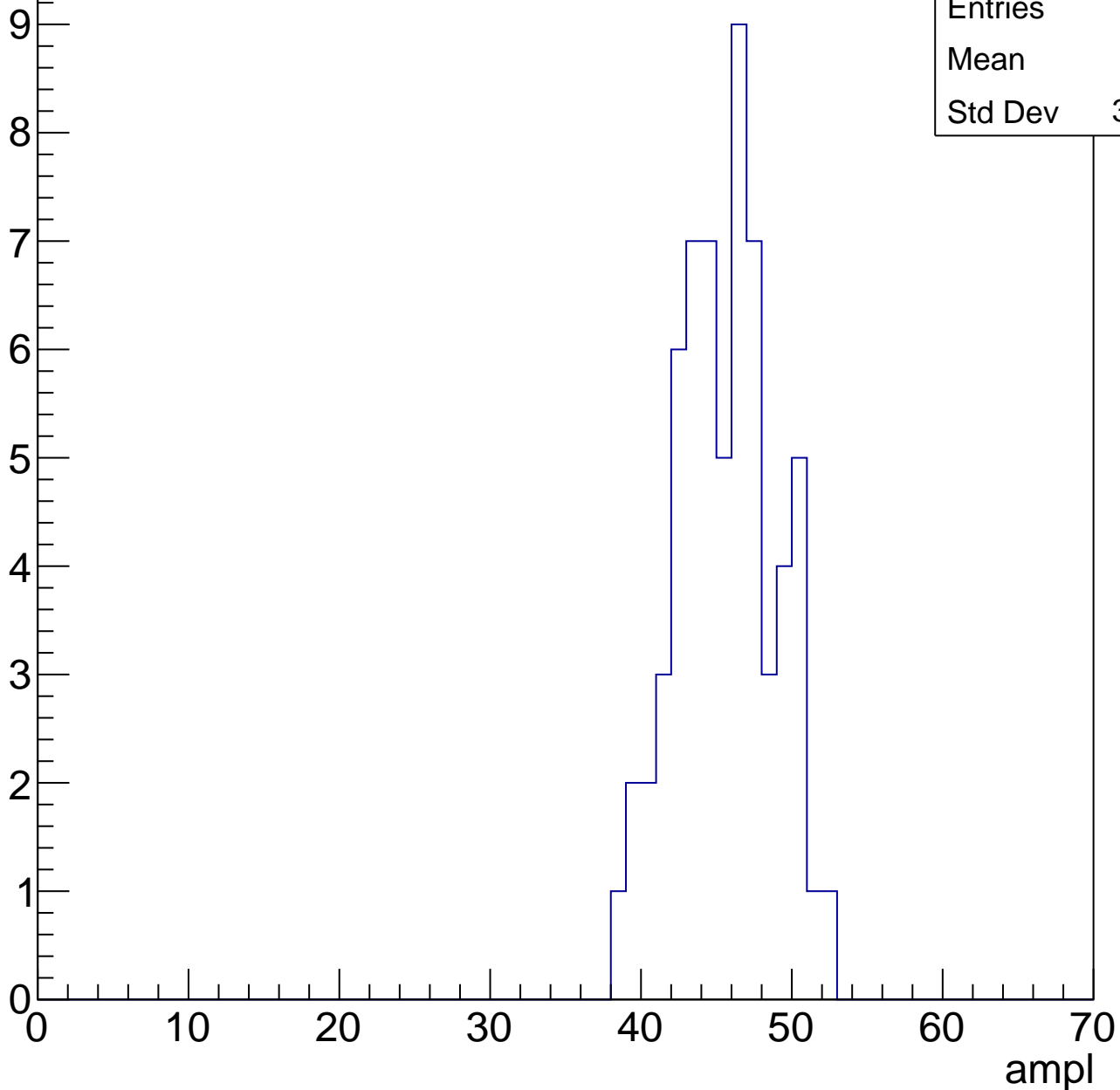


# B1L103S, U3-ch102, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	45.1
Std Dev	3.201

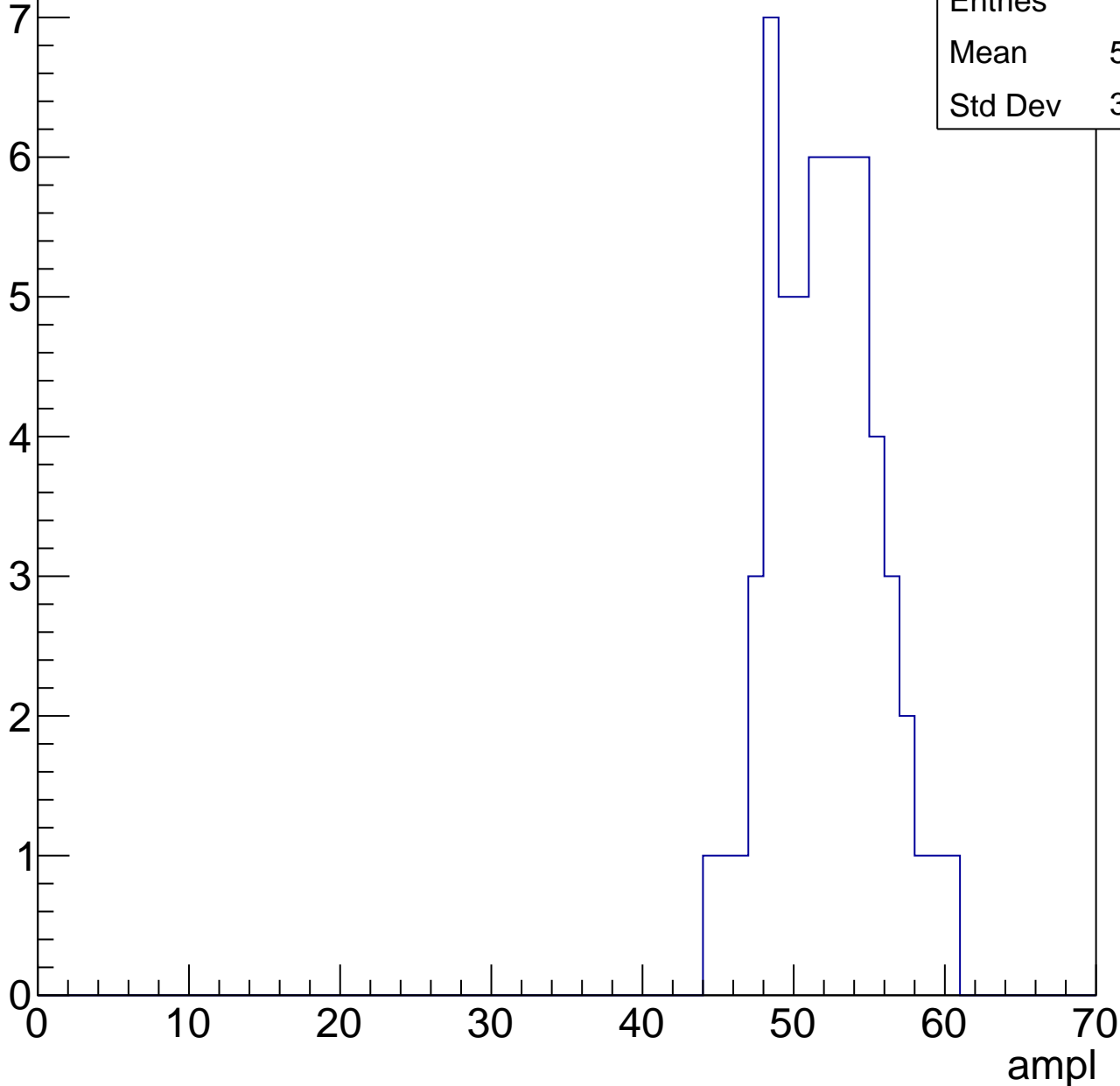


# B1L103S, U3-ch102, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	51.63
Std Dev	3.473

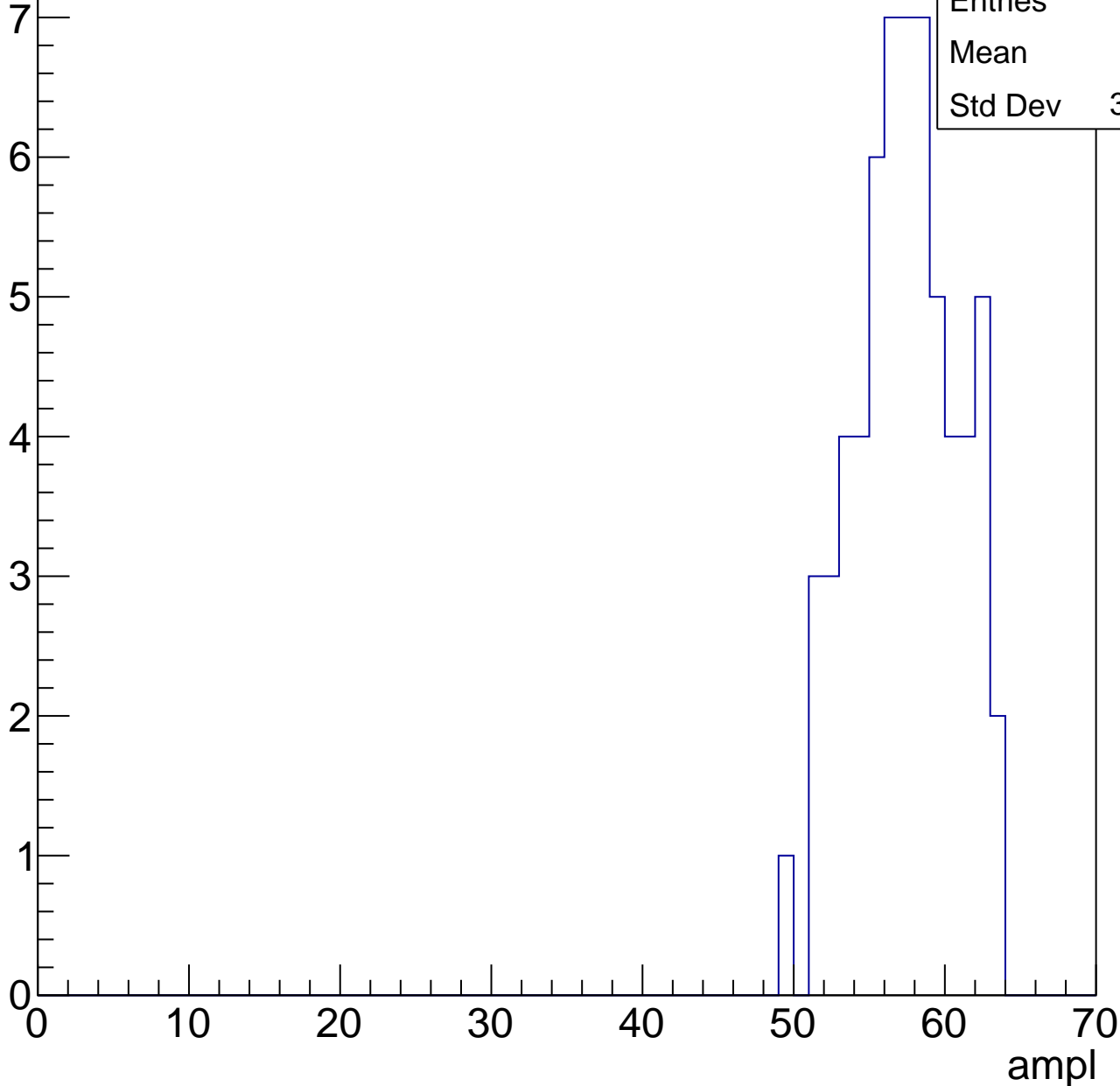


# B1L103S, U3-ch102, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

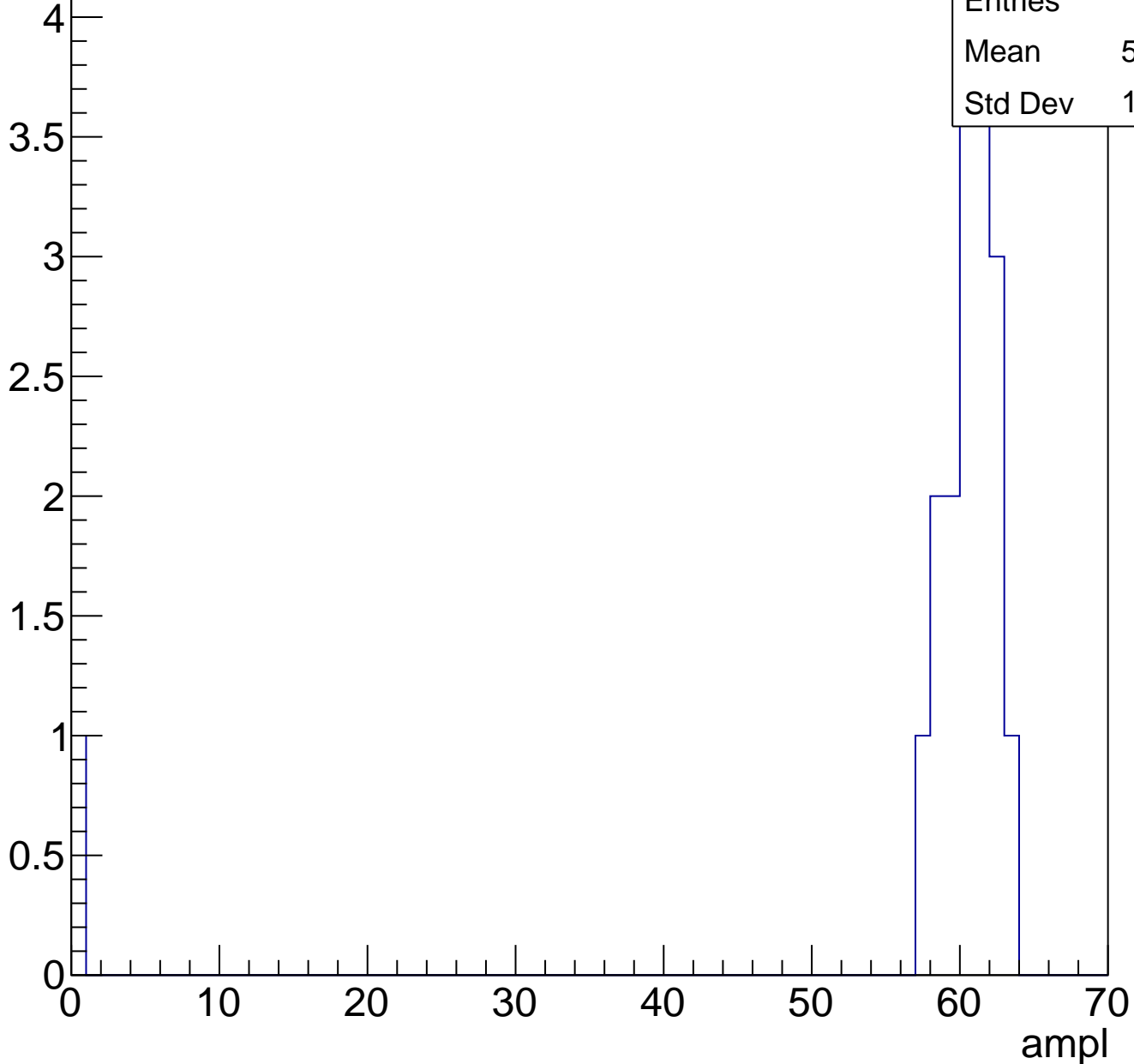
Entries	62
Mean	56.9
Std Dev	3.364



# B1L103S, U3-ch102, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



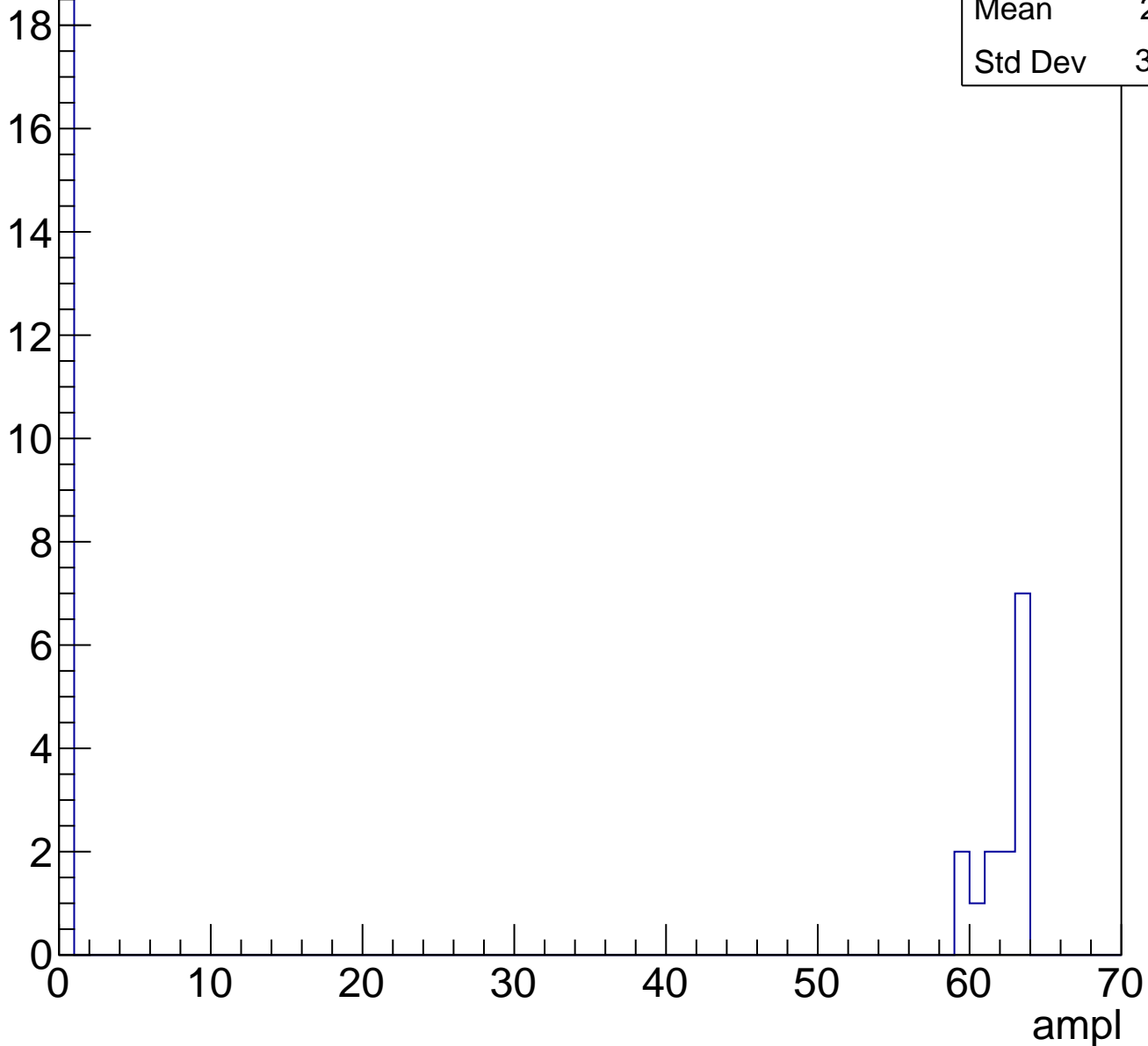


# B1L103S, U3-ch102, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	33
Mean	26.21
Std Dev	30.55

Entry



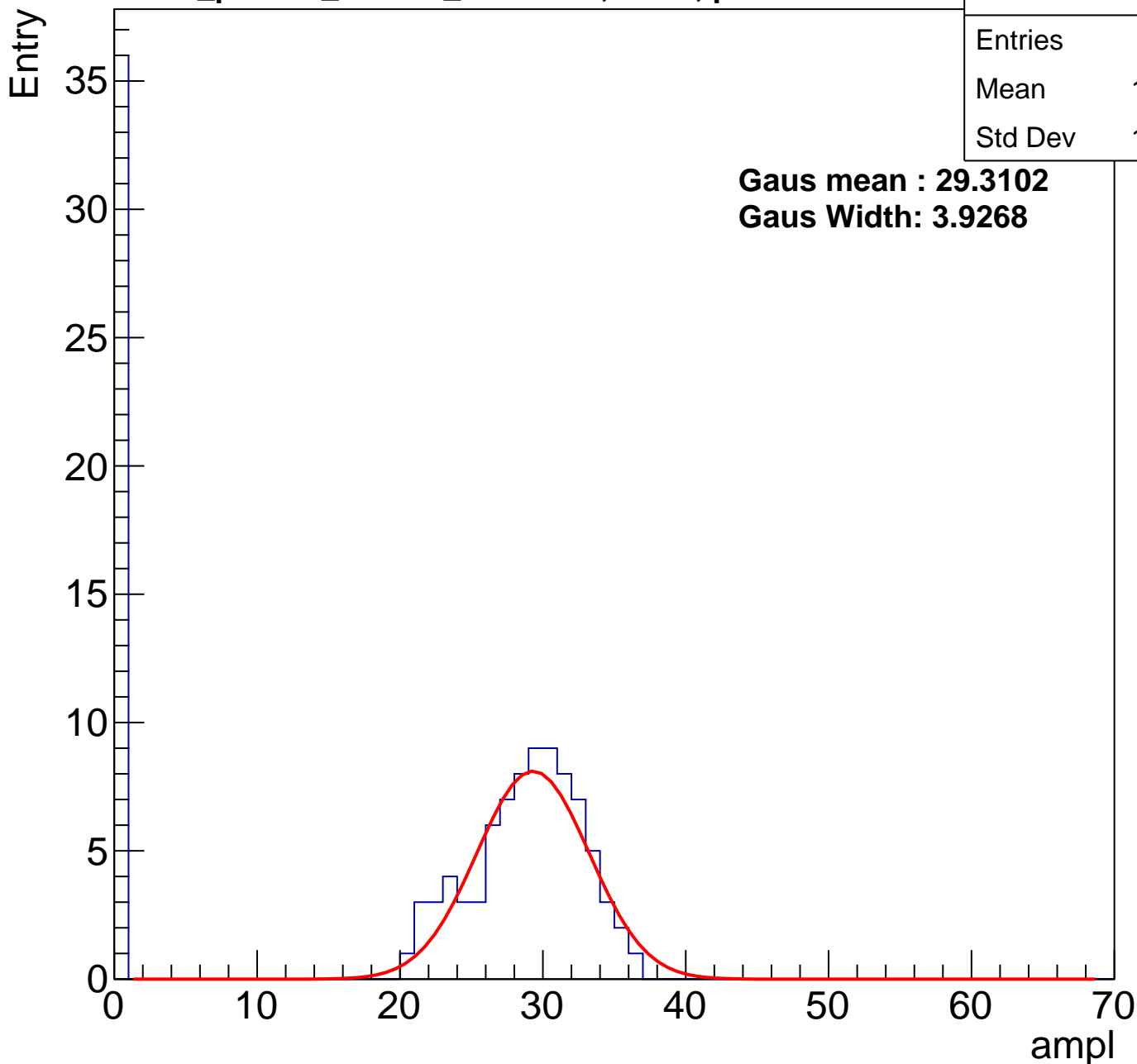
# B1L103S, U3-ch103, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	118
Mean	19.77
Std Dev	13.46

**Gaus mean : 29.3102**

**Gaus Width: 3.9268**



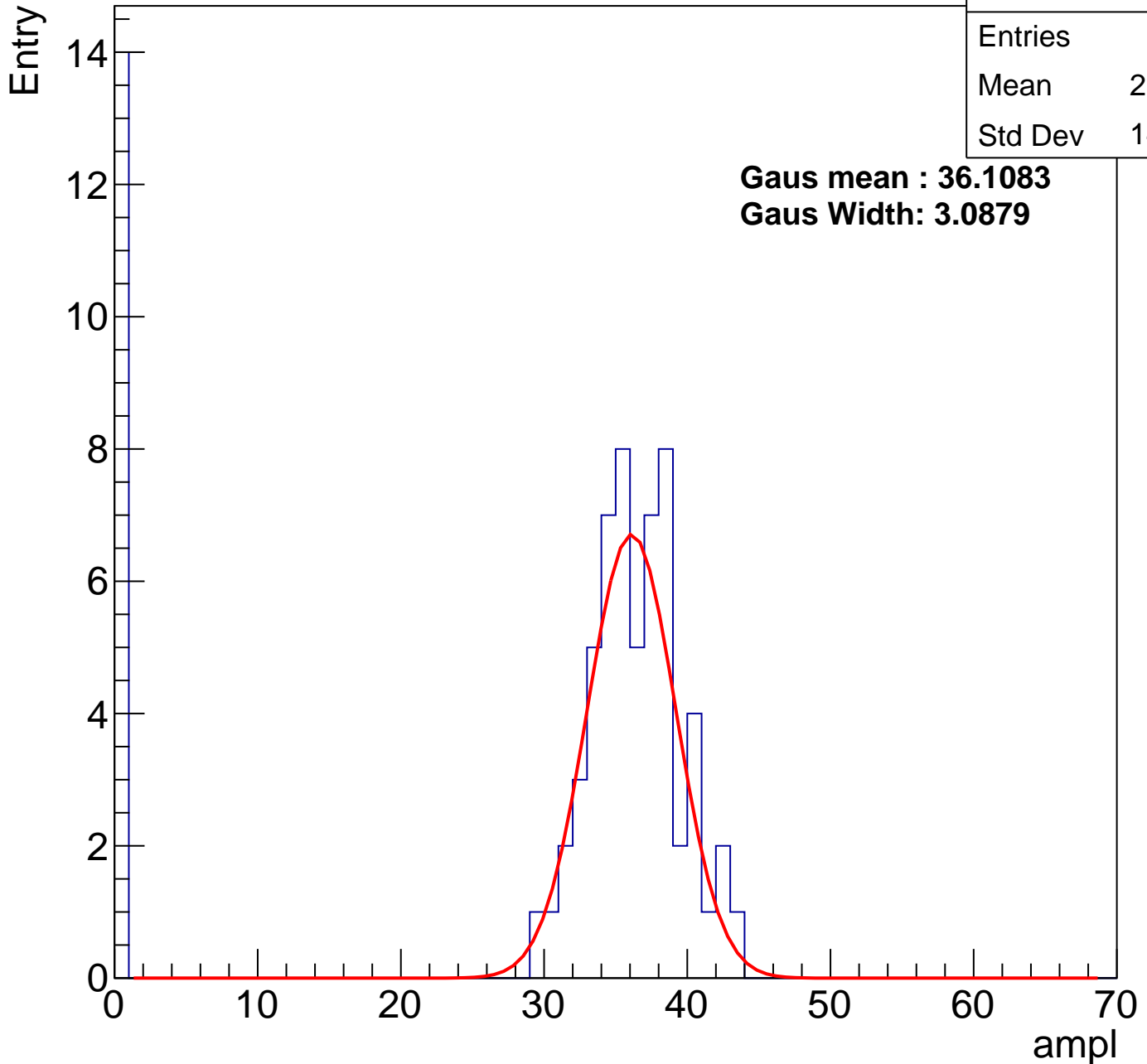
# B1L103S, U3-ch103, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	71
Mean	28.86
Std Dev	14.56

**Gaus mean : 36.1083**

**Gaus Width: 3.0879**



# B1L103S, U3-ch103, adc2

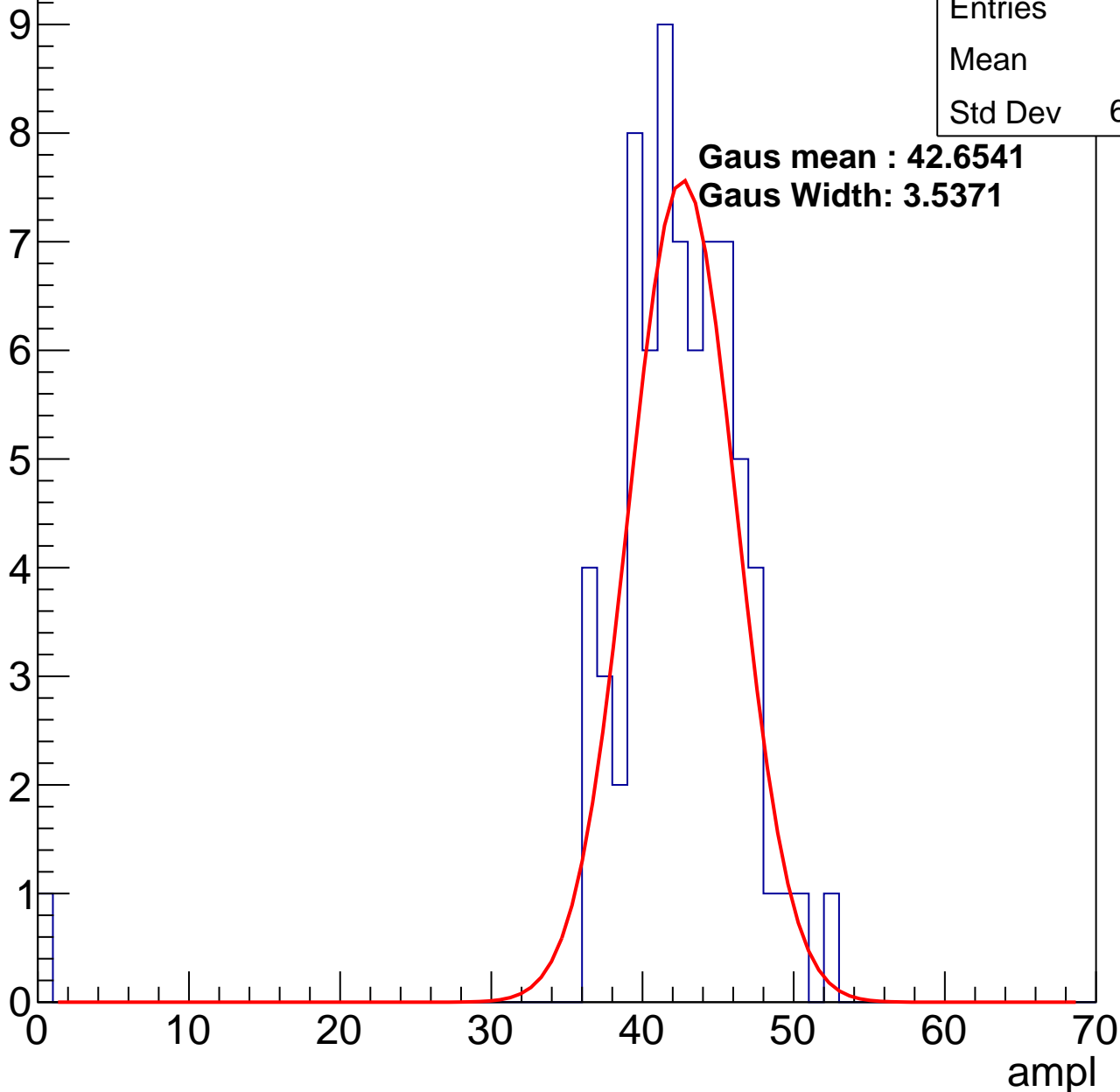
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	41.7
Std Dev	6.013

**Gaus mean : 42.6541**

**Gaus Width: 3.5371**

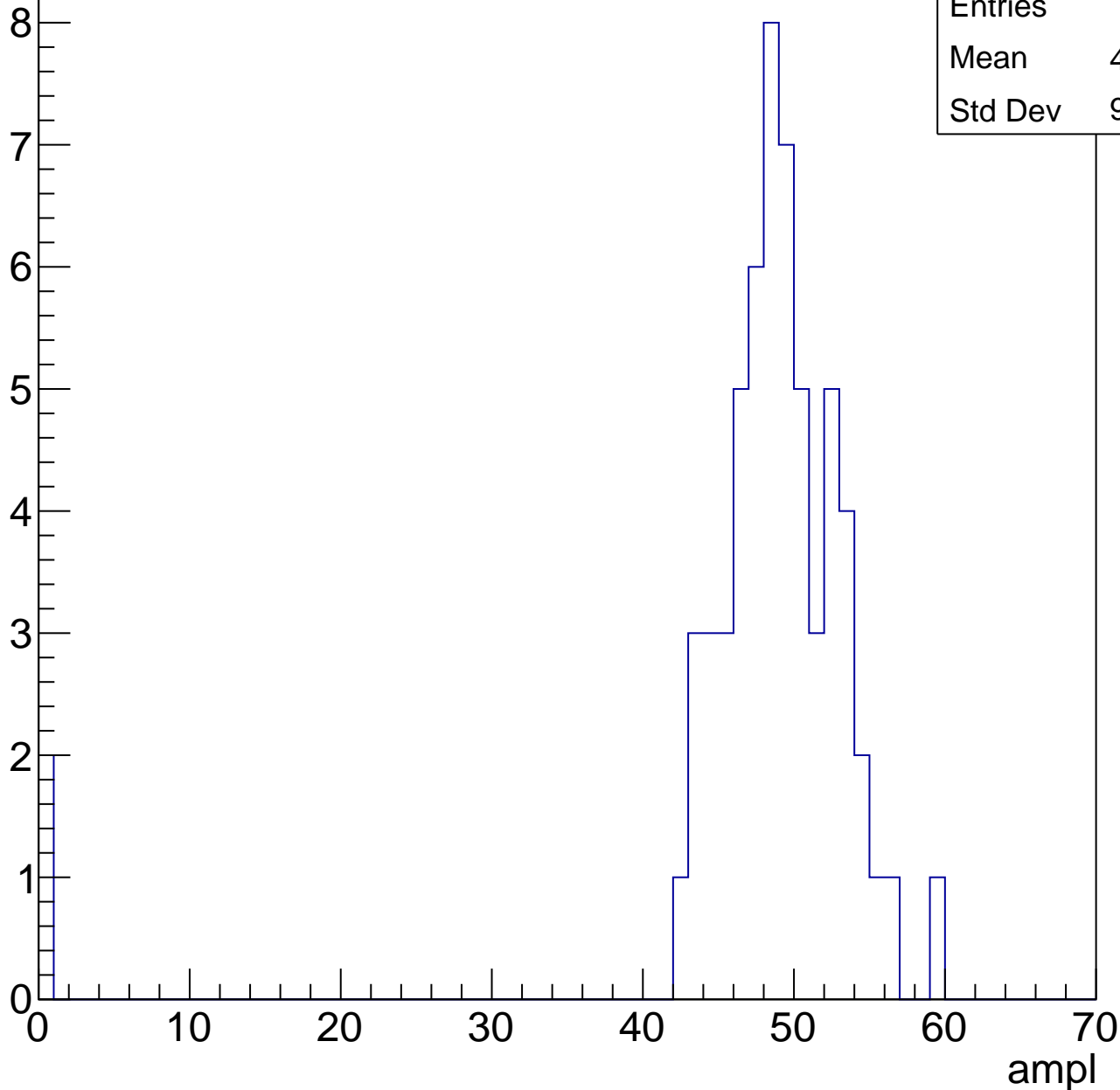


# B1L103S, U3-ch103, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	60
Mean	47.17
Std Dev	9.415

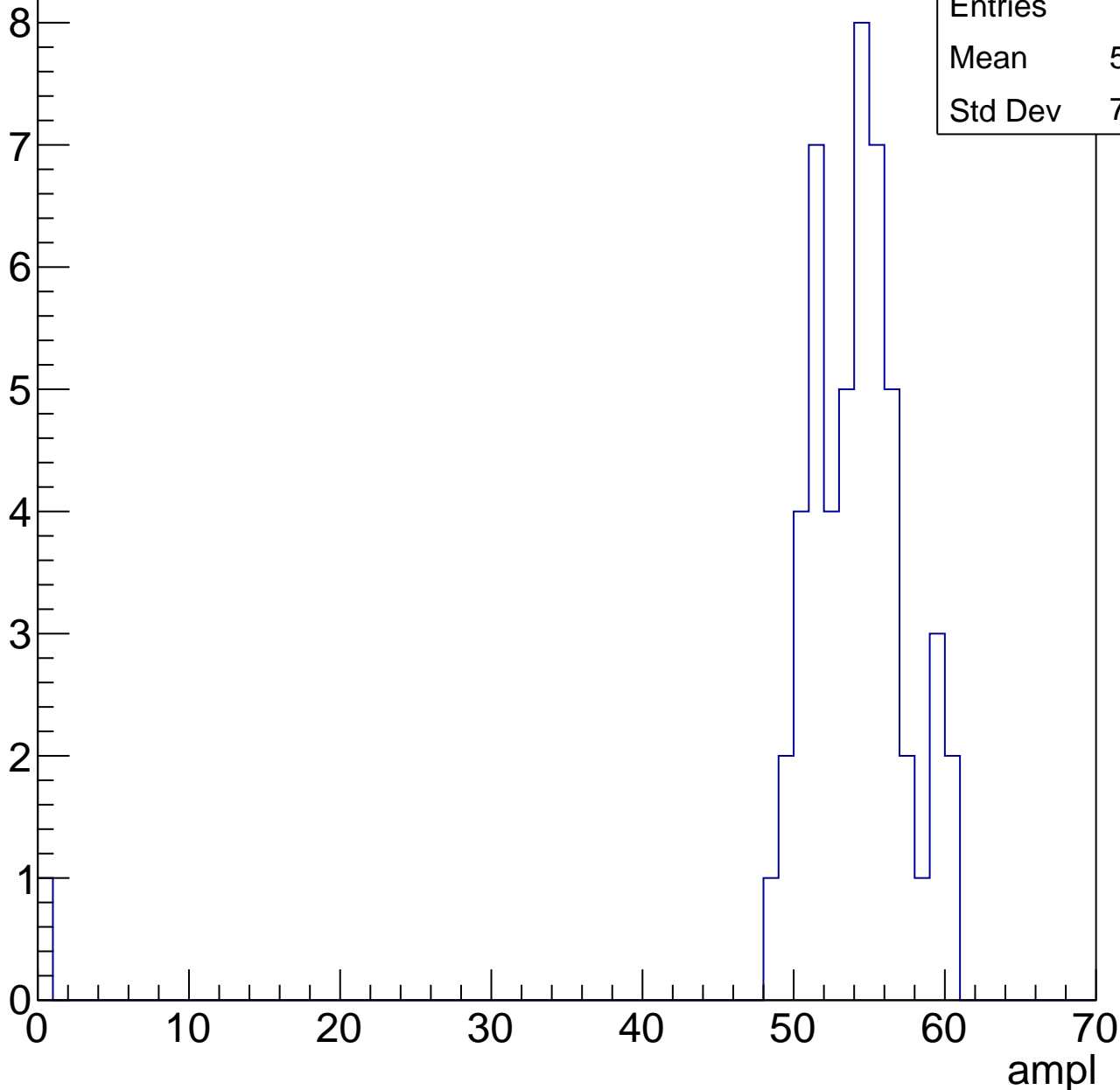


# B1L103S, U3-ch103, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

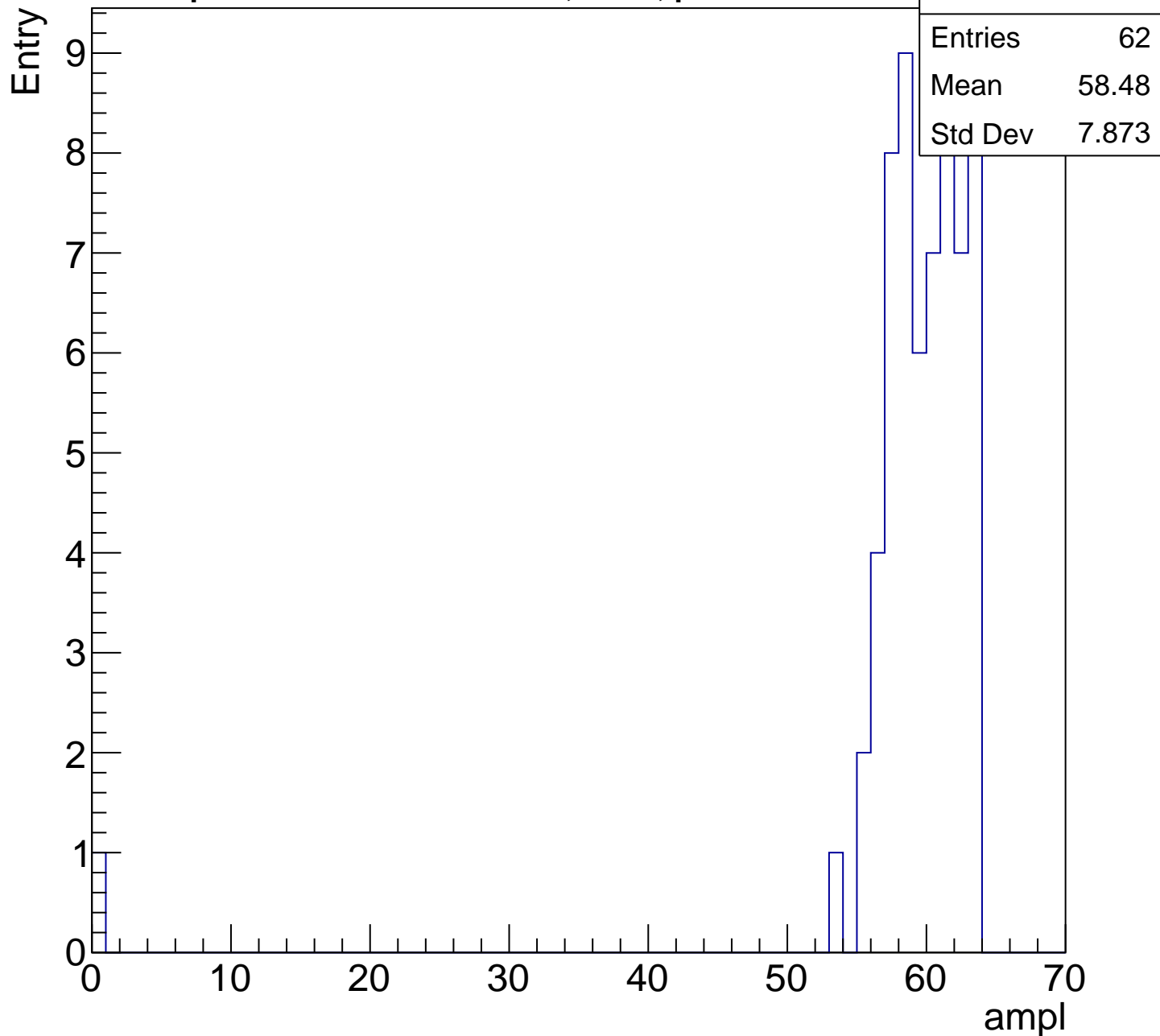
Entry

Entries	52
Mean	52.73
Std Dev	7.935



# B1L103S, U3-ch103, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2



# B1L103S, U3-ch103, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U3-ch103, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U3-ch104, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	86
Mean	21.98
Std Dev	11.2

**Gaus mean : 26.7072**

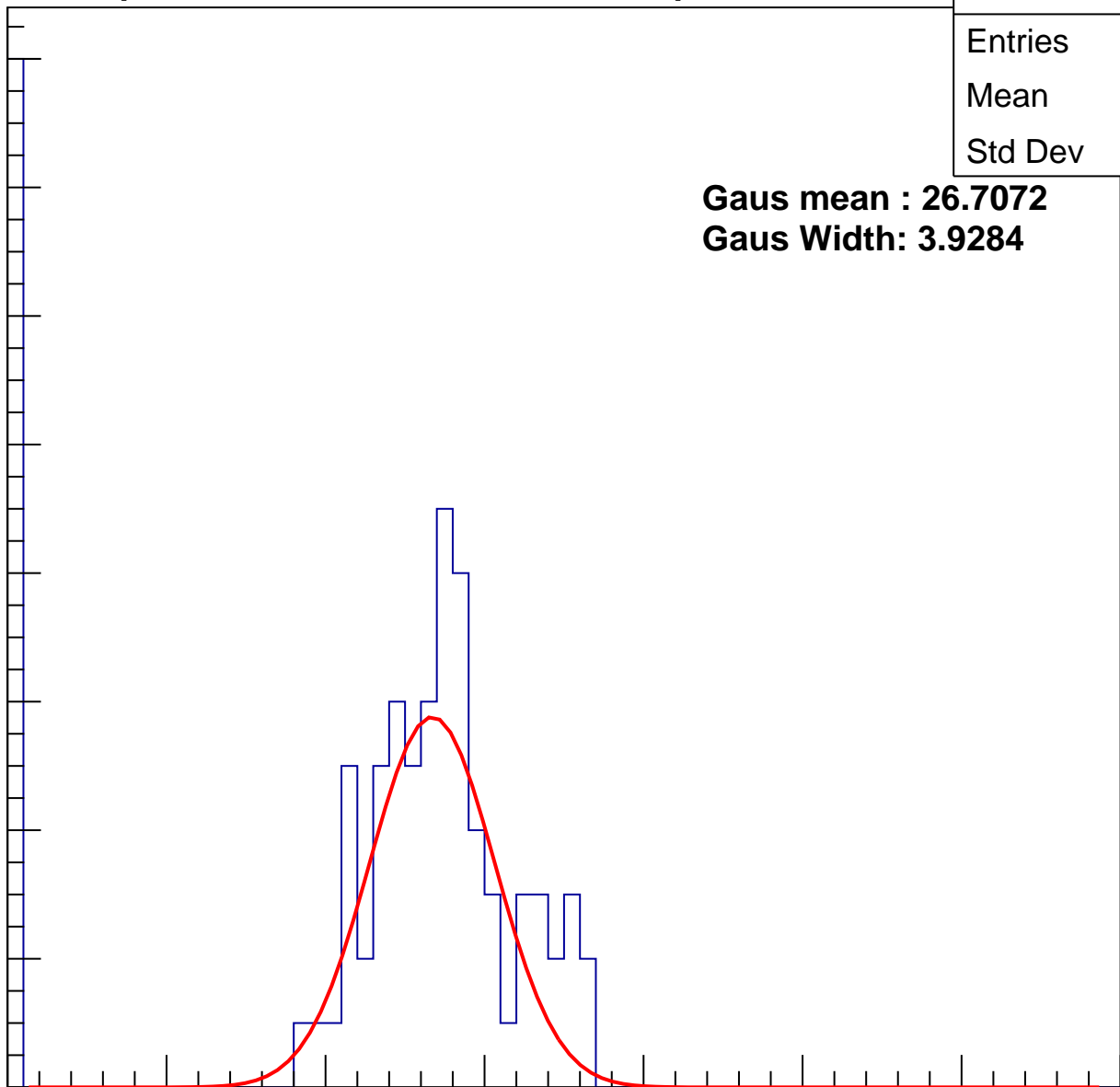
**Gaus Width: 3.9284**

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch104, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	88
Mean	29.06
Std Dev	12.53

**Gaus mean : 34.5029**

**Gaus Width: 3.6971**

Entry

12

10

8

6

4

2

0

0

10

20

30

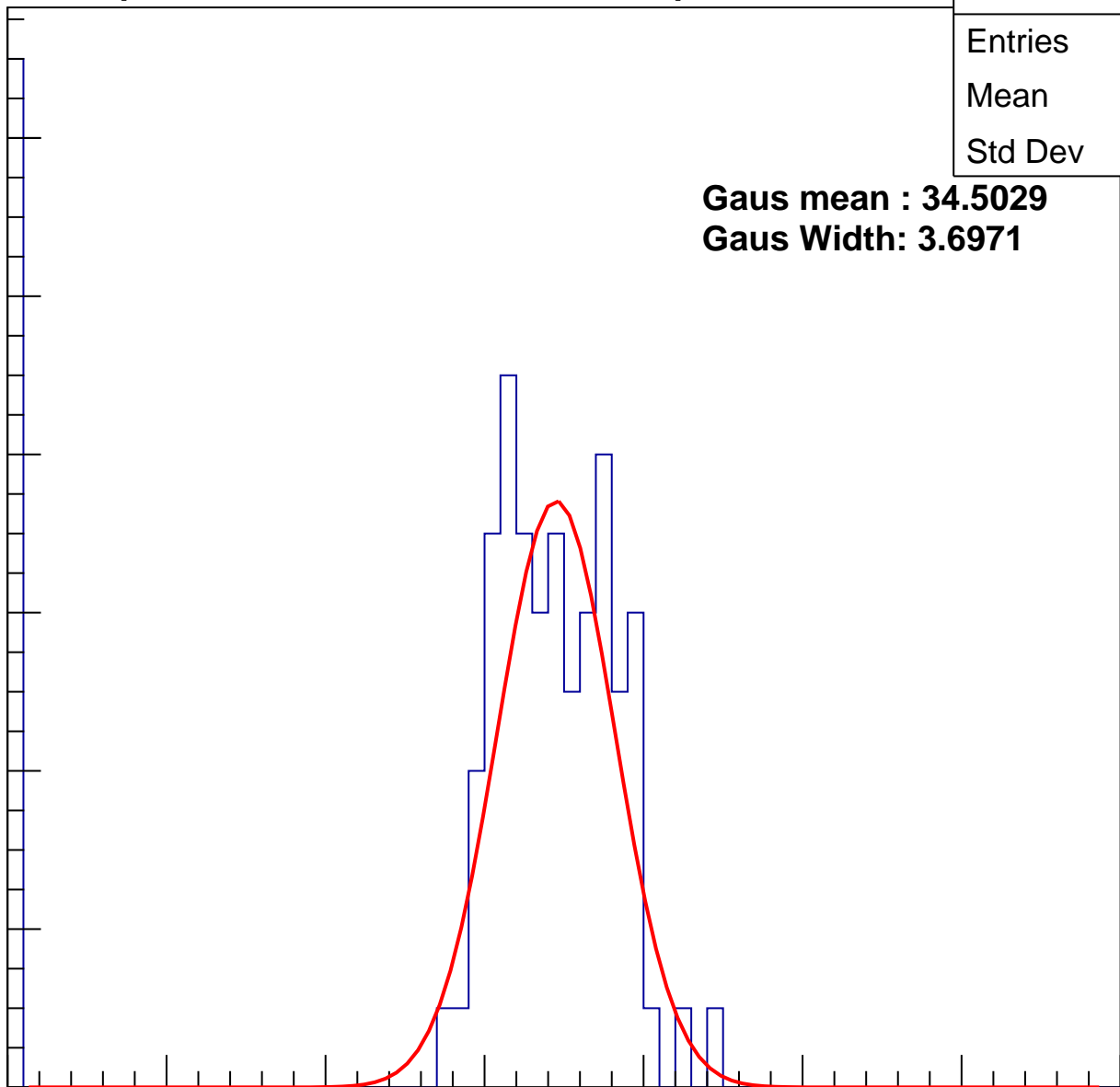
40

50

60

70

ampl



# B1L103S, U3-ch104, adc2

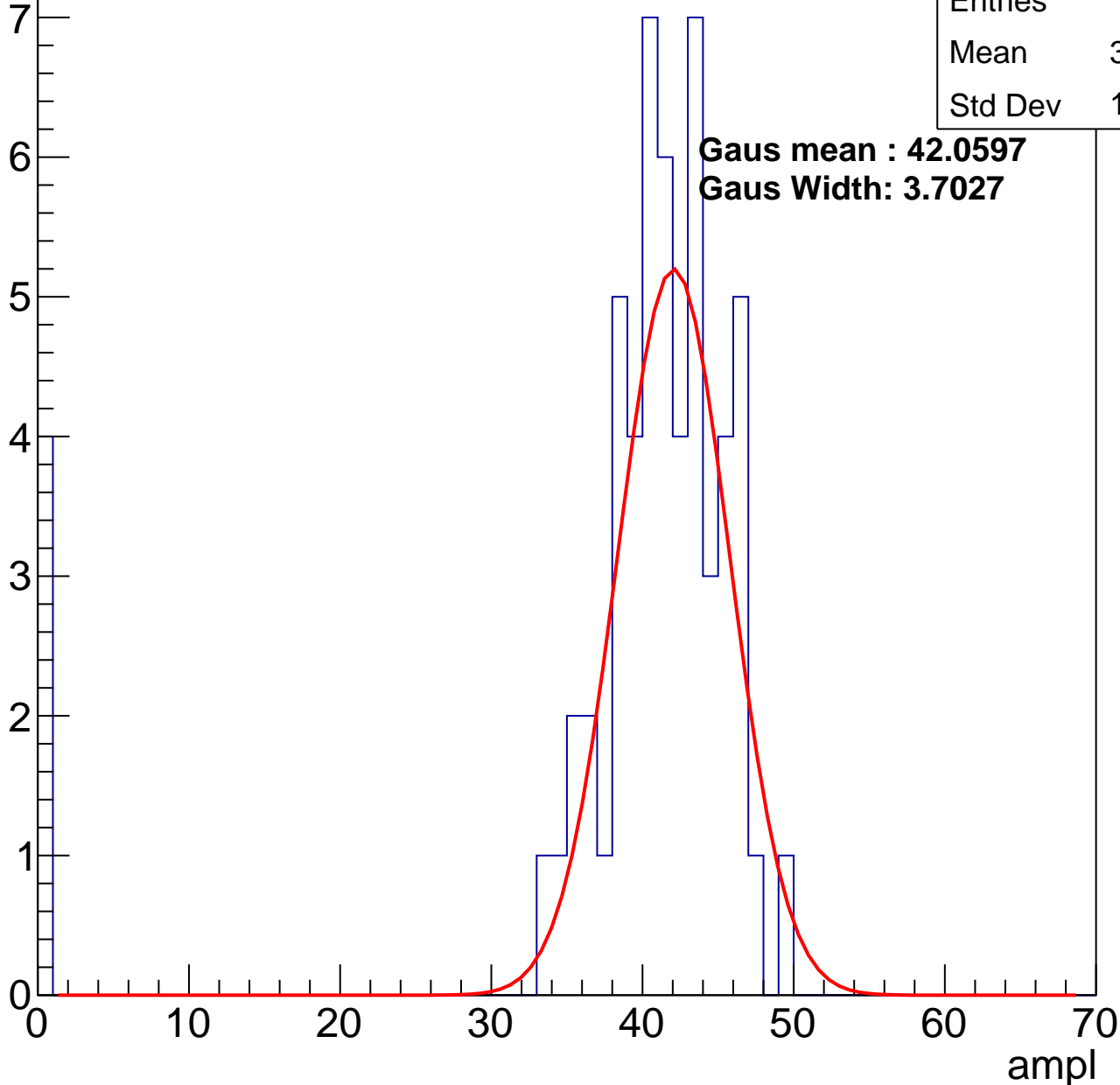
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	38.36
Std Dev	10.98

**Gaus mean : 42.0597**

**Gaus Width: 3.7027**

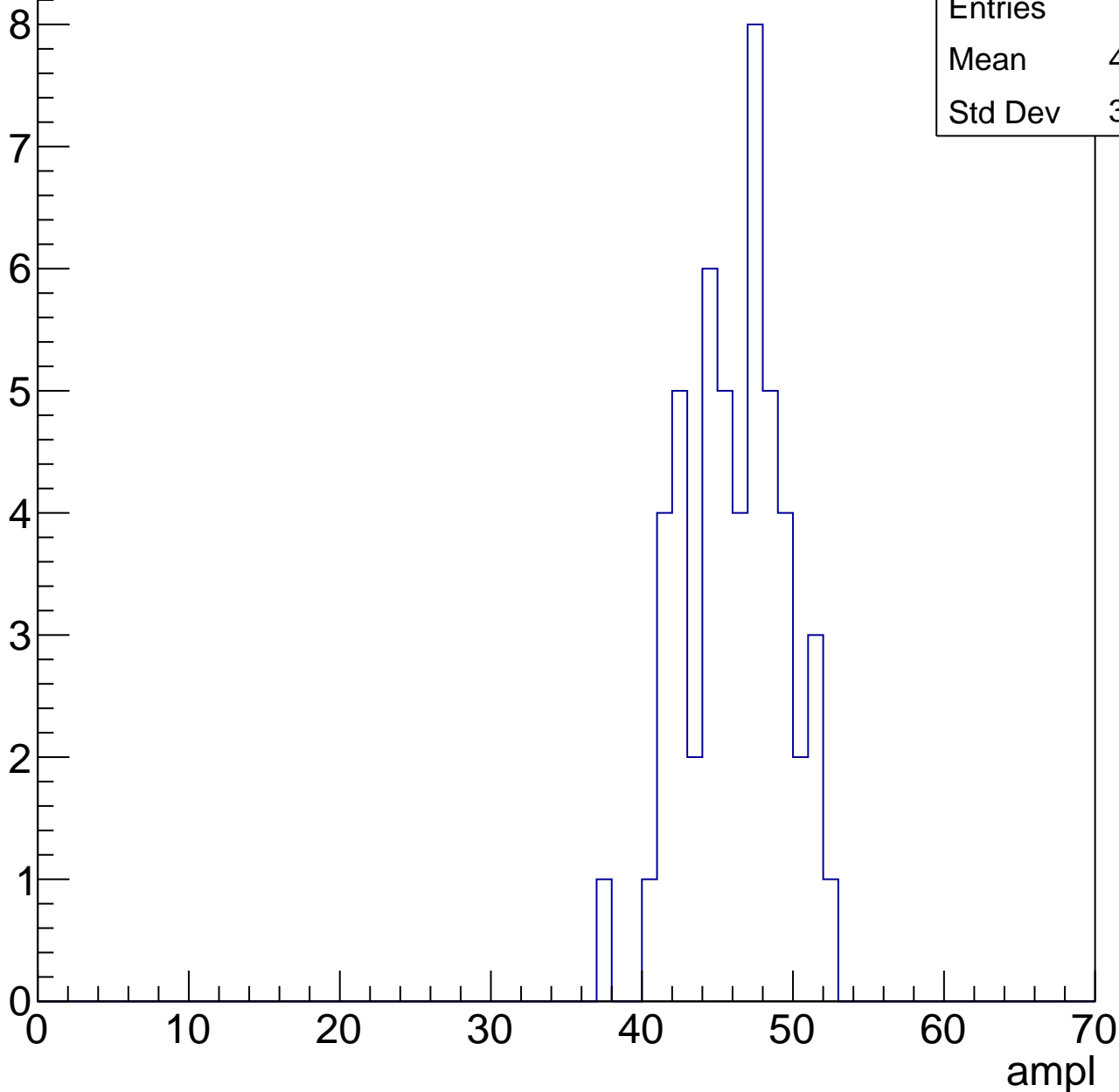


# B1L103S, U3-ch104, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	51
Mean	45.63
Std Dev	3.266

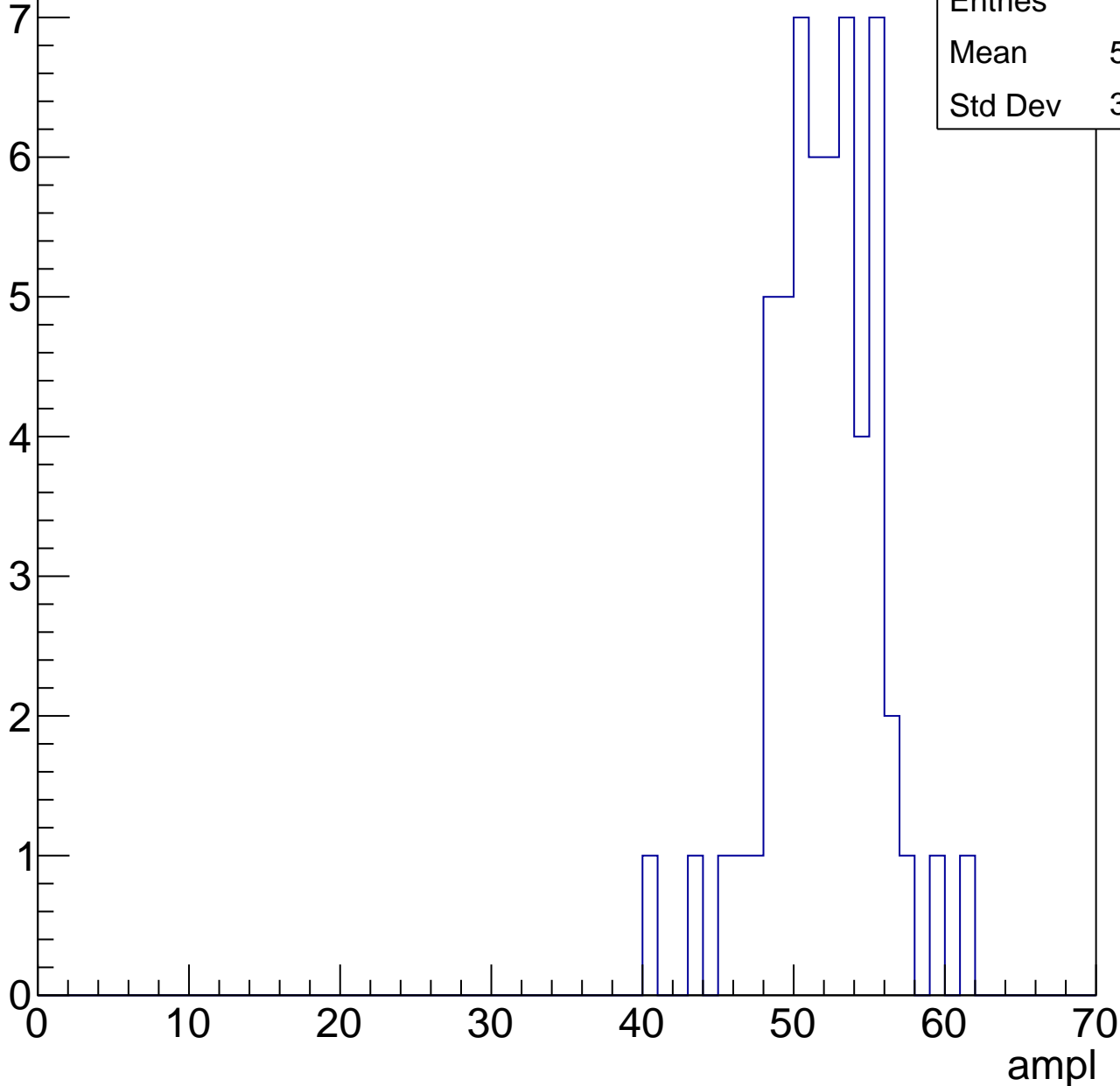


# B1L103S, U3-ch104, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

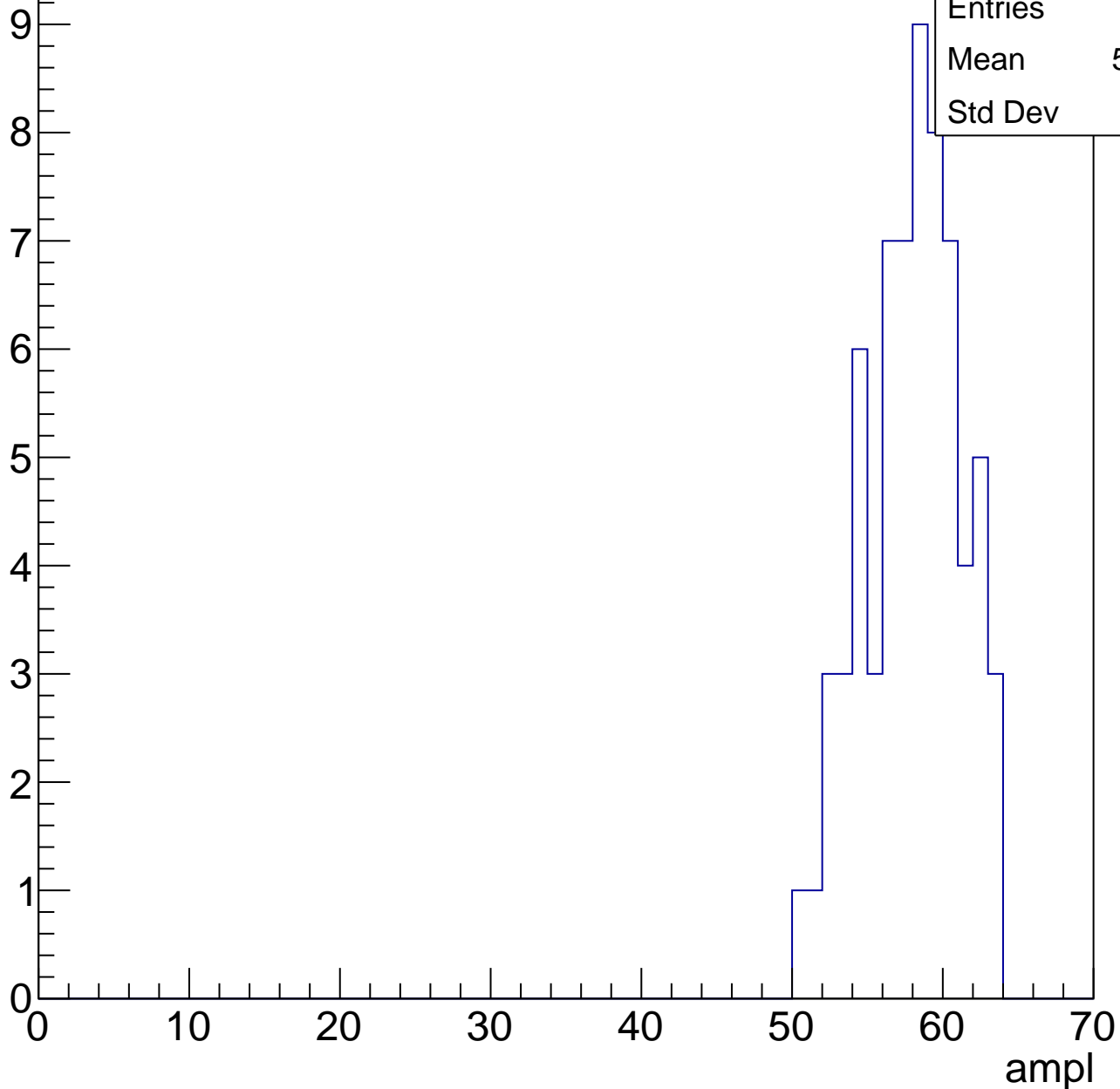
Entries	57
Mean	51.49
Std Dev	3.633



# B1L103S, U3-ch104, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



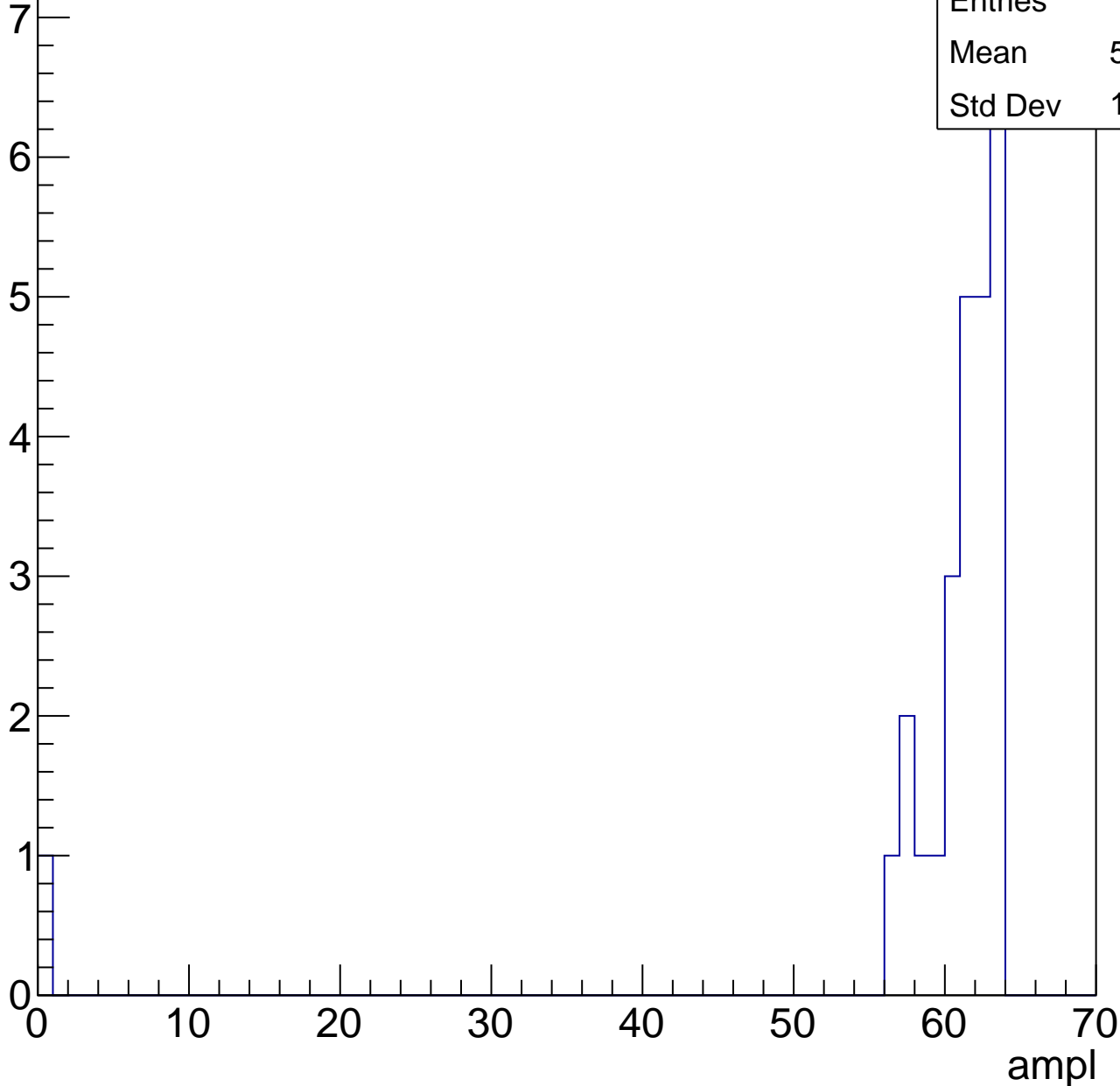
Entries	67
Mean	57.51
Std Dev	3.15

# B1L103S, U3-ch104, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	26
Mean	58.58
Std Dev	11.89





# B1L103S, U3-ch104, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	19
Mean	0
Std Dev	0

# B1L103S, U3-ch105, adc0

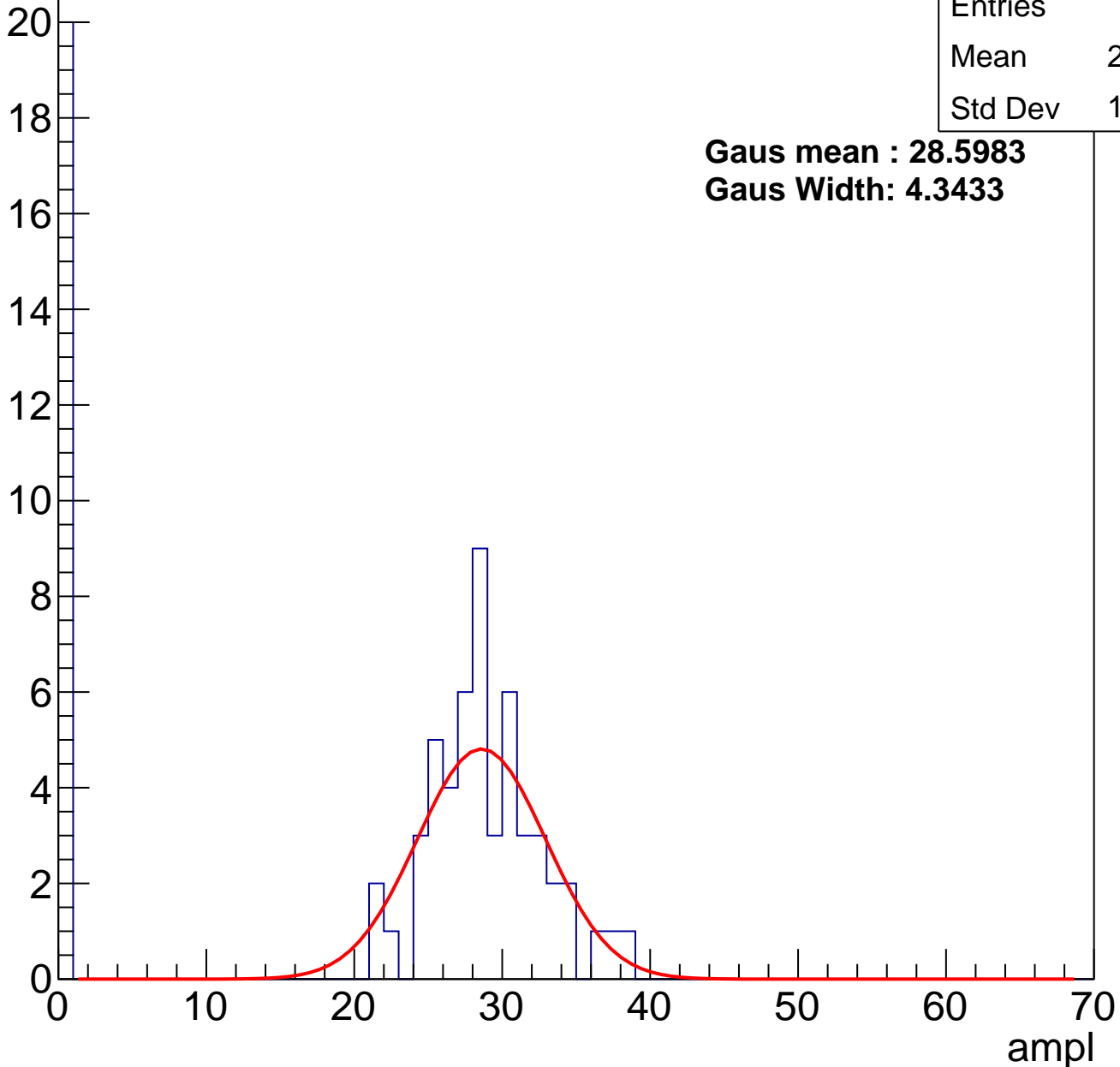
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	72
Mean	20.56
Std Dev	13.13

**Gaus mean : 28.5983**

**Gaus Width: 4.3433**

Entry



# B1L103S, U3-ch105, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	92
Mean	29.2
Std Dev	13.33

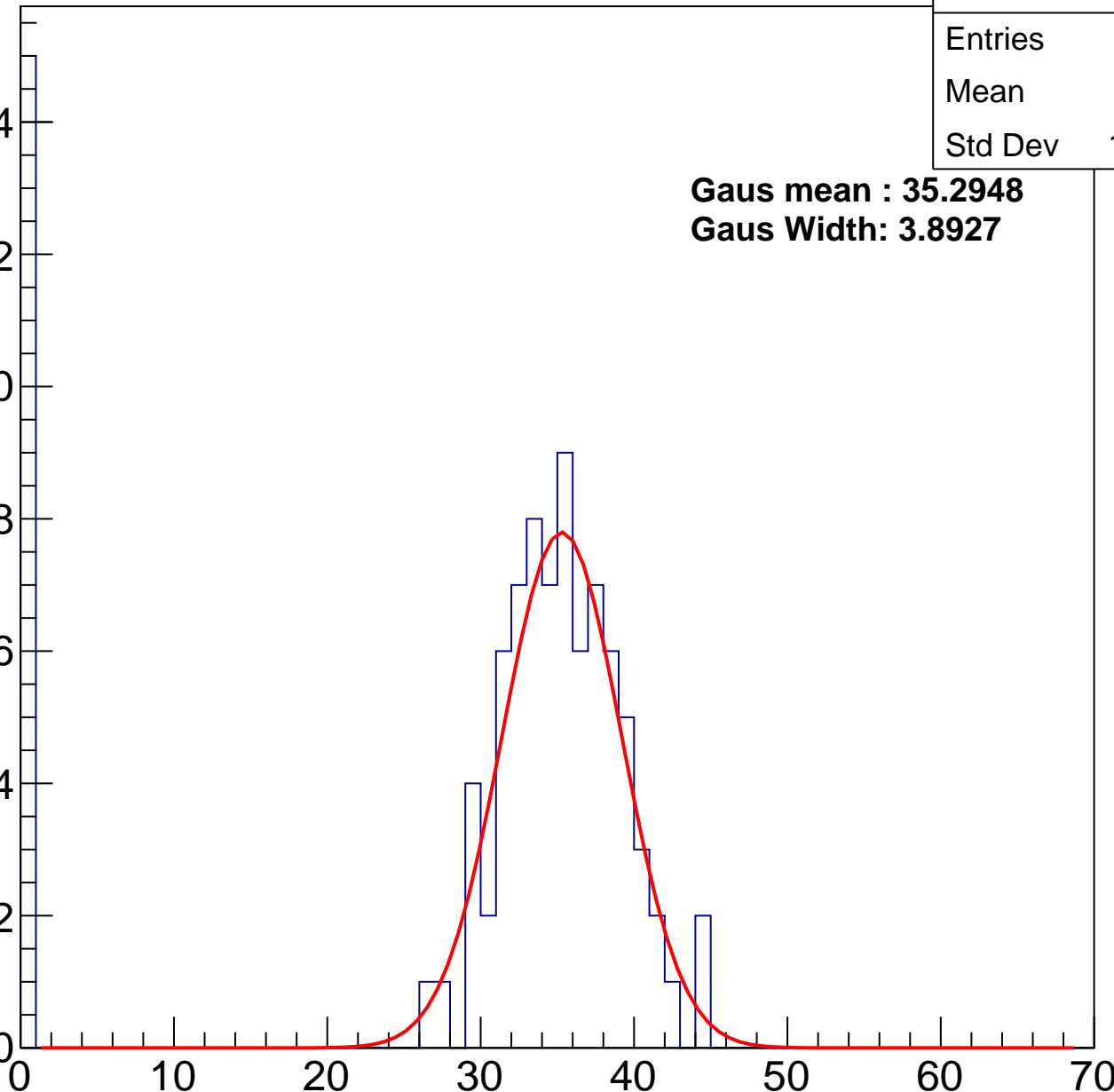
**Gaus mean : 35.2948**

**Gaus Width: 3.8927**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U3-ch105, adc2

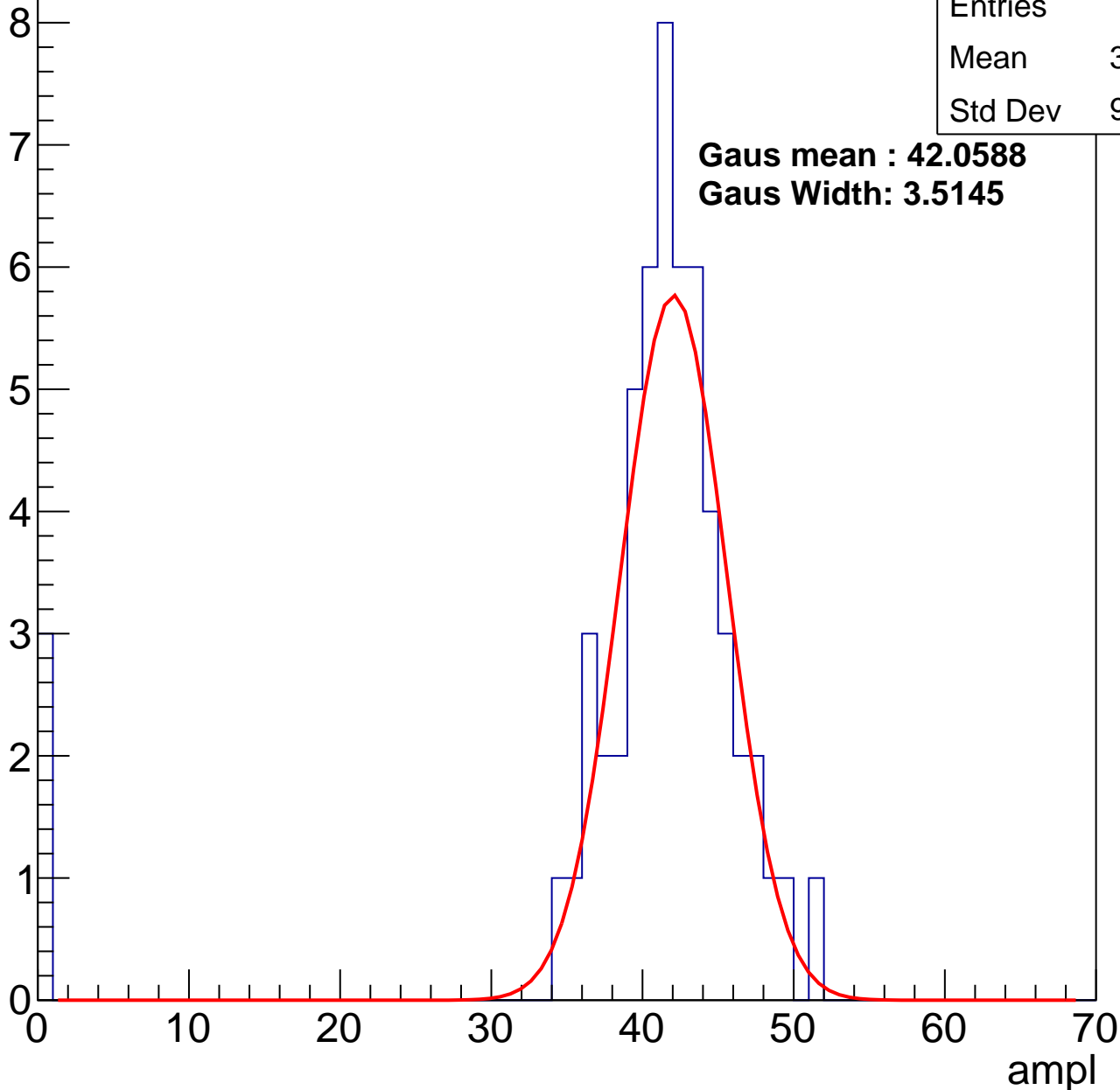
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	57
Mean	39.39
Std Dev	9.894

**Gaus mean : 42.0588**

**Gaus Width: 3.5145**

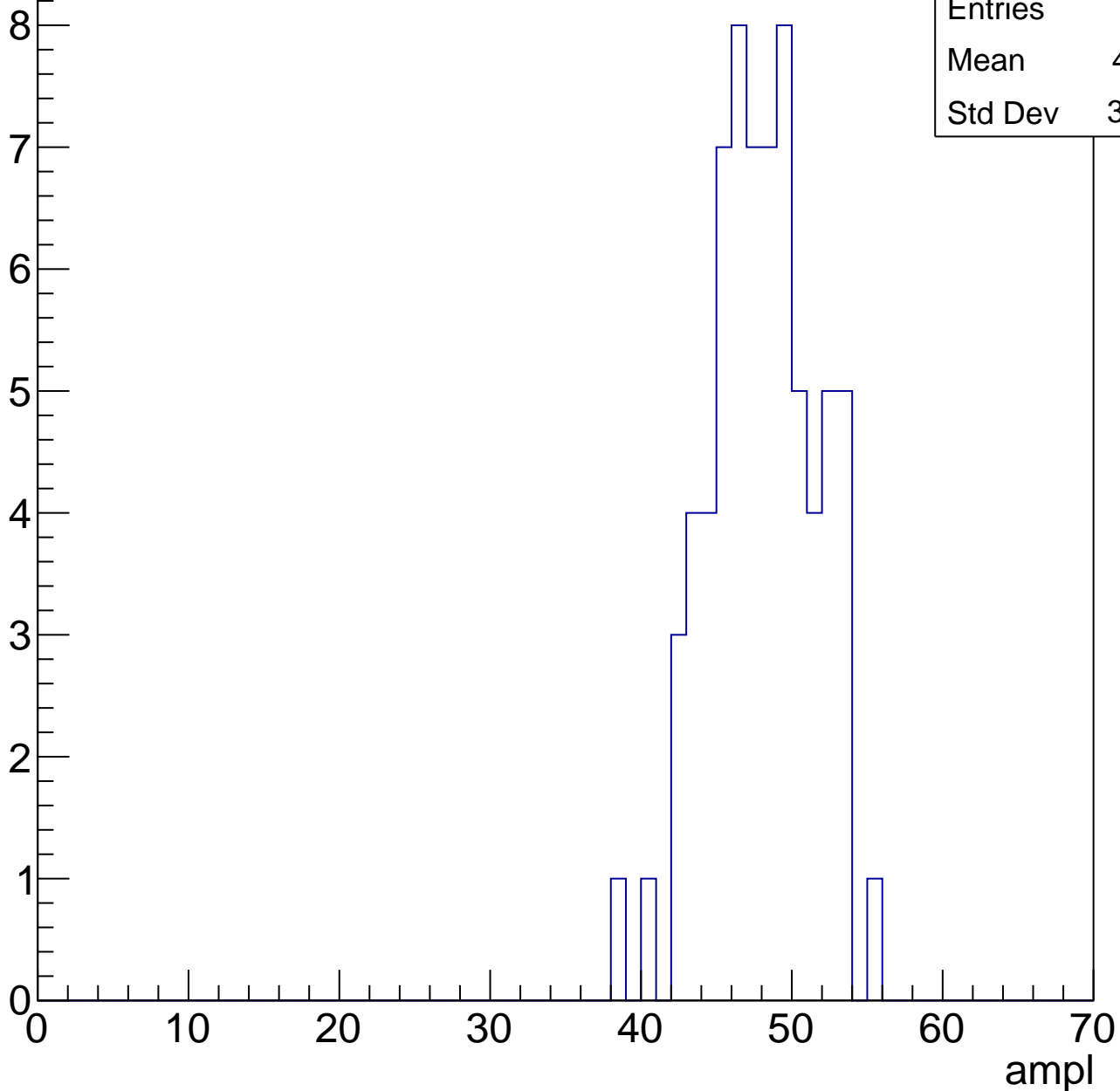


# B1L103S, U3-ch105, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	70
Mean	47.51
Std Dev	3.463

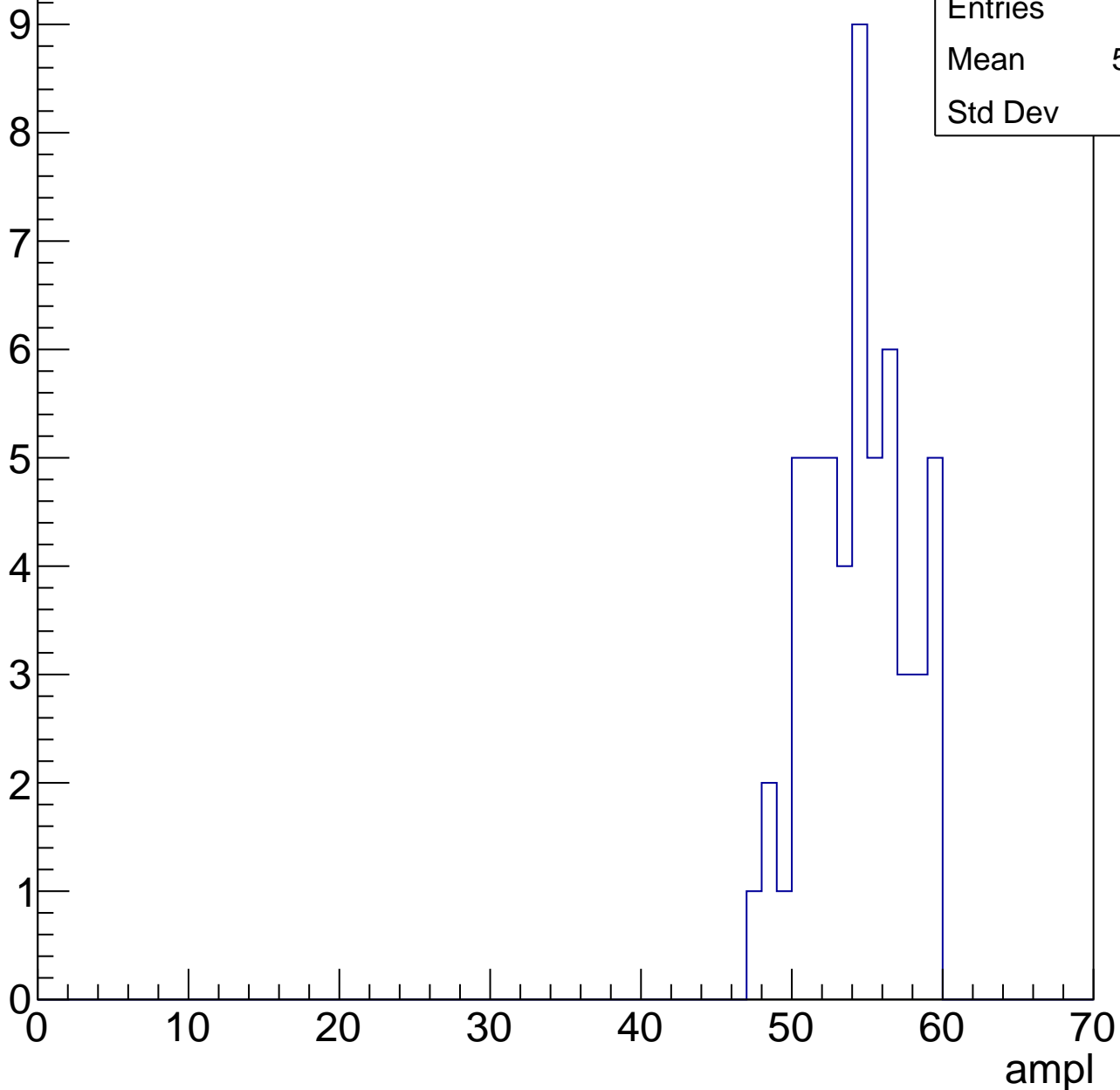


# B1L103S, U3-ch105, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	54
Mean	53.81
Std Dev	3.11



# B1L103S, U3-ch105, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

10

Entries 58

Mean 59.14

Std Dev 2.529

8

6

4

2

0

0

10

20

30

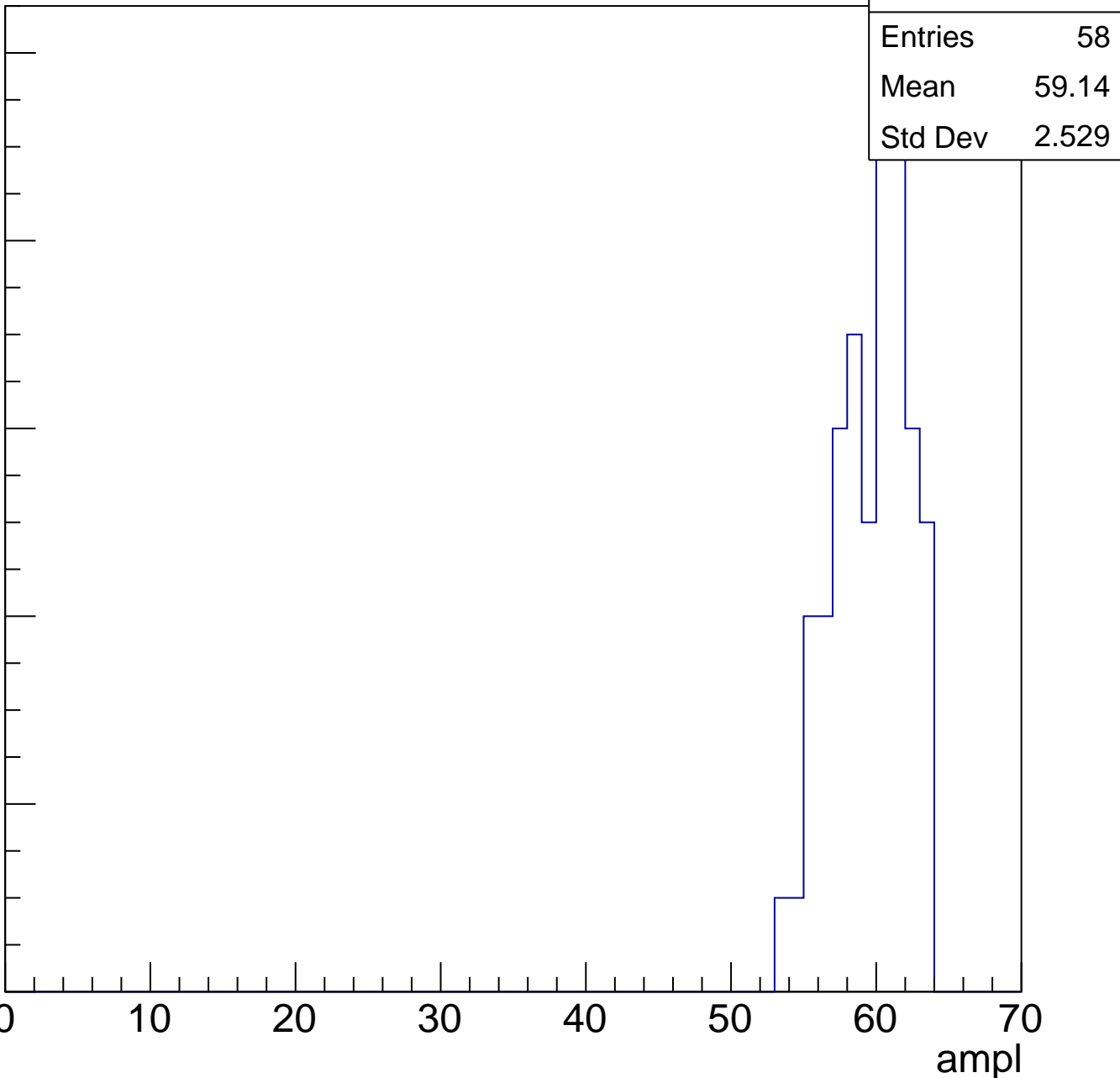
40

50

60

70

ampl

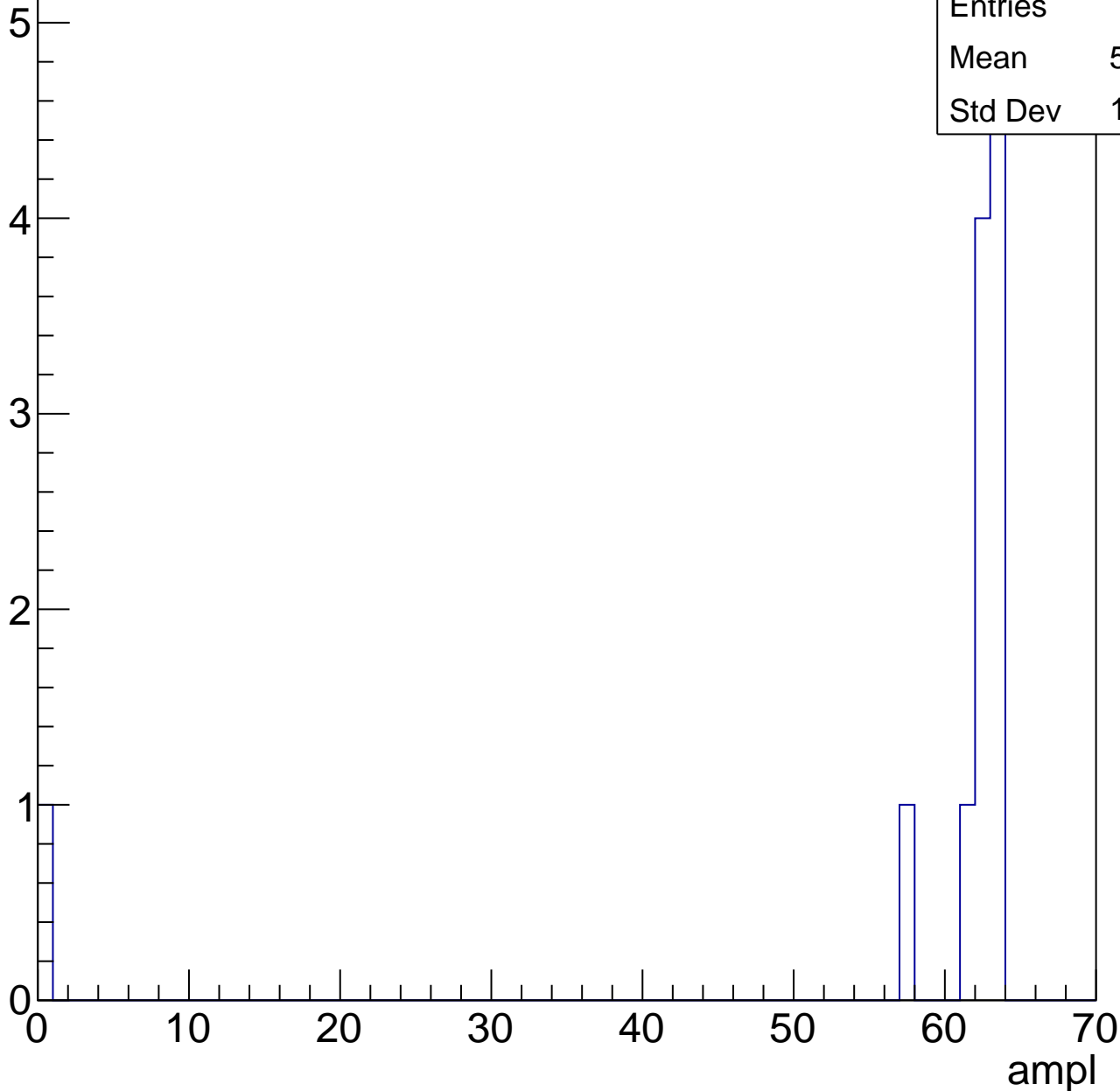


# B1L103S, U3-ch105, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	12
Mean	56.75
Std Dev	17.19





# B1L103S, U3-ch105, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	19
Mean	0
Std Dev	0

# B1L103S, U3-ch106, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	86
Mean	21.93
Std Dev	11.03

**Gaus mean : 27.6281**

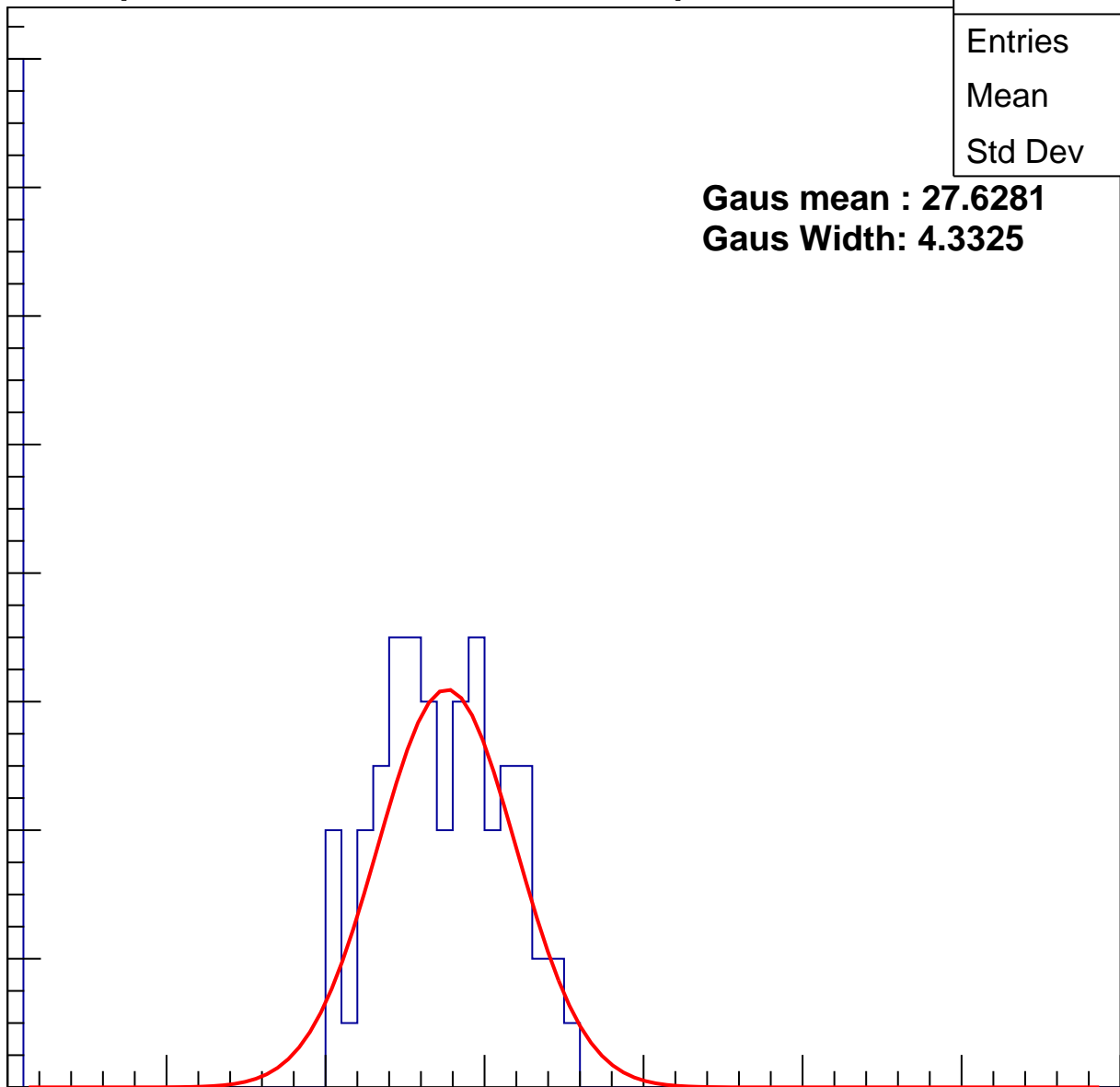
**Gaus Width: 4.3325**

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



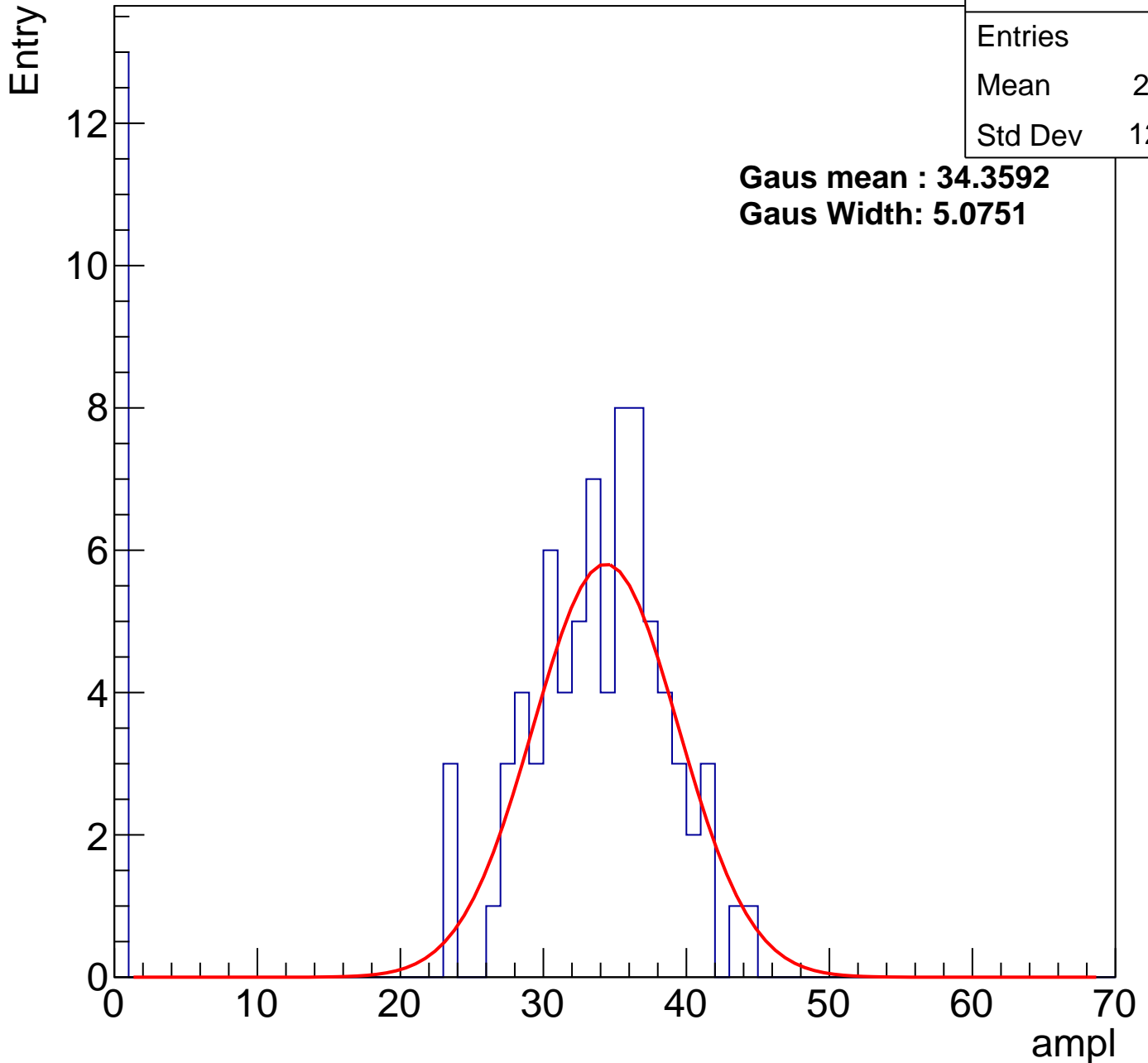
# B1L103S, U3-ch106, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	88
Mean	28.61
Std Dev	12.64

**Gaus mean : 34.3592**

**Gaus Width: 5.0751**



# B1L103S, U3-ch106, adc2

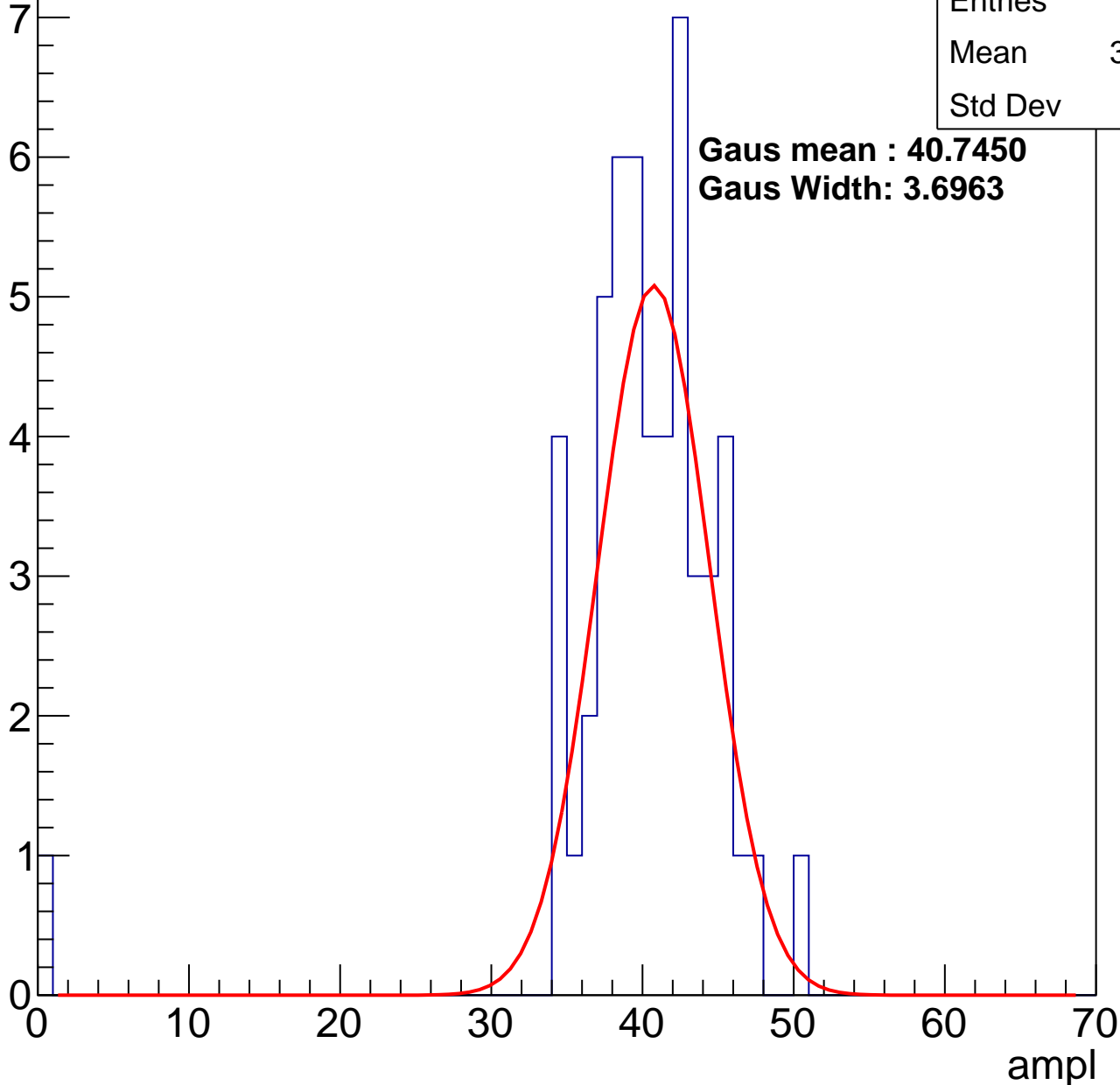
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	53
Mean	39.47
Std Dev	6.52

**Gaus mean : 40.7450**

**Gaus Width: 3.6963**

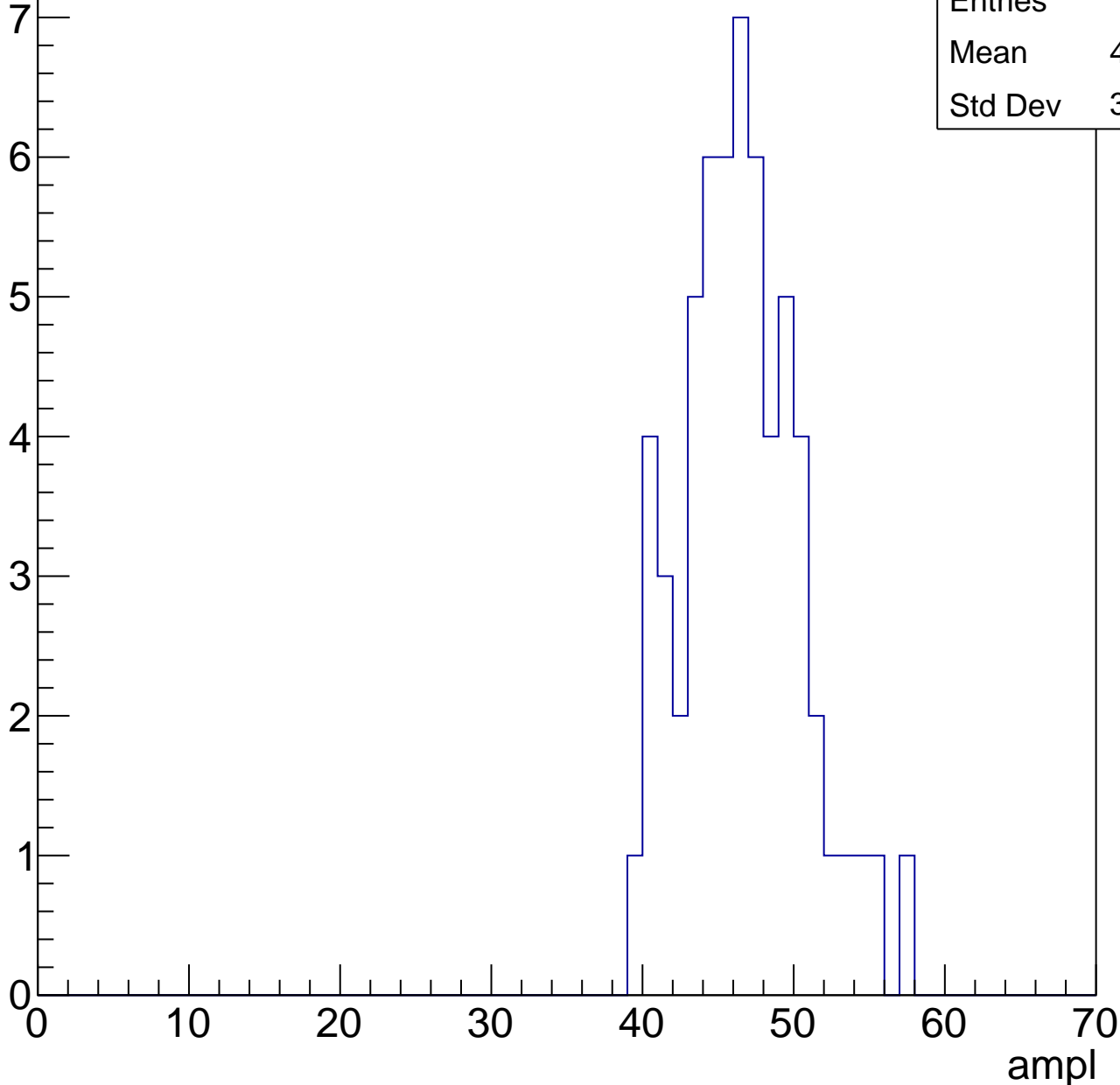


# B1L103S, U3-ch106, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	60
Mean	46.15
Std Dev	3.885

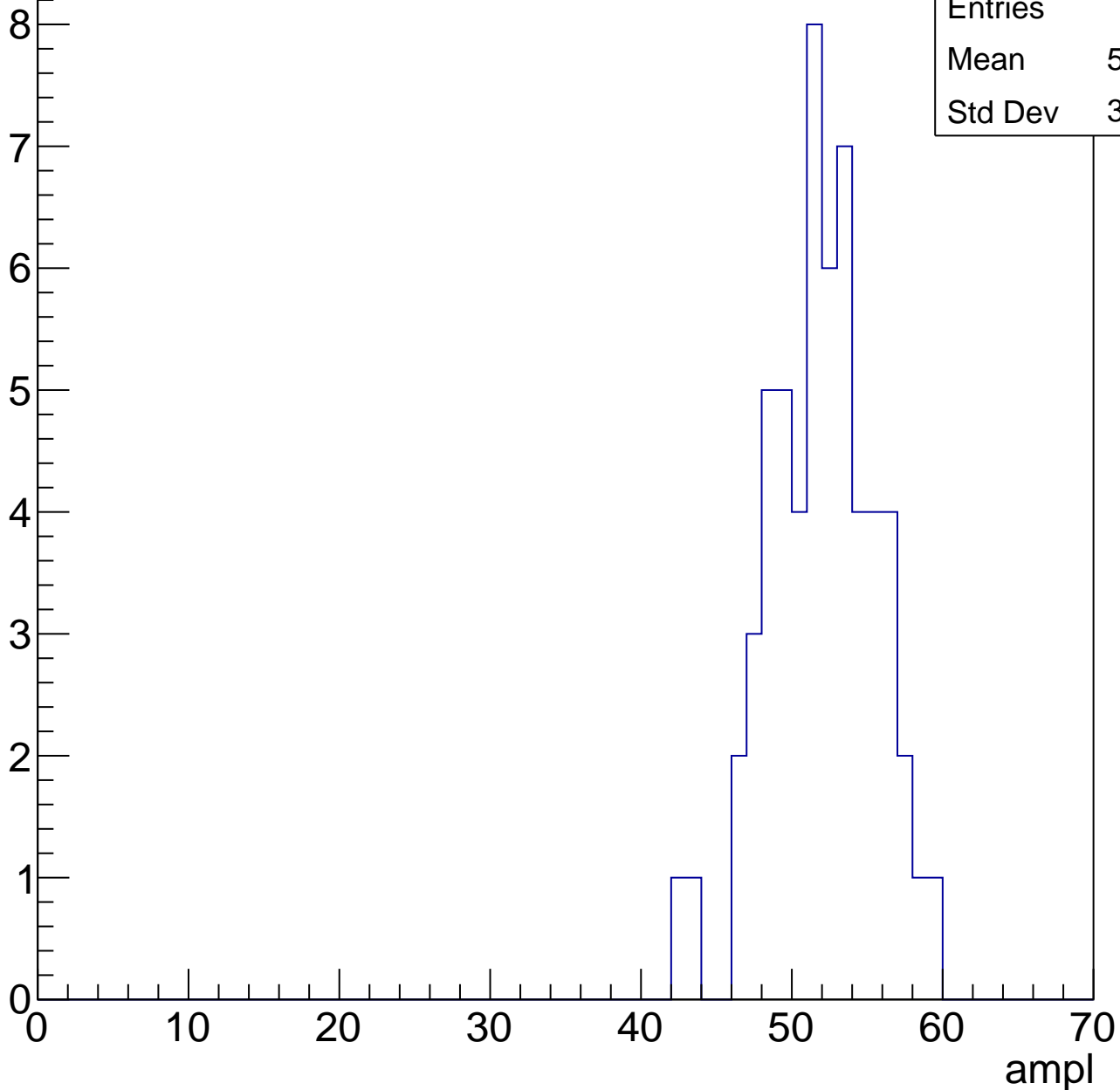


# B1L103S, U3-ch106, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	51.47
Std Dev	3.519

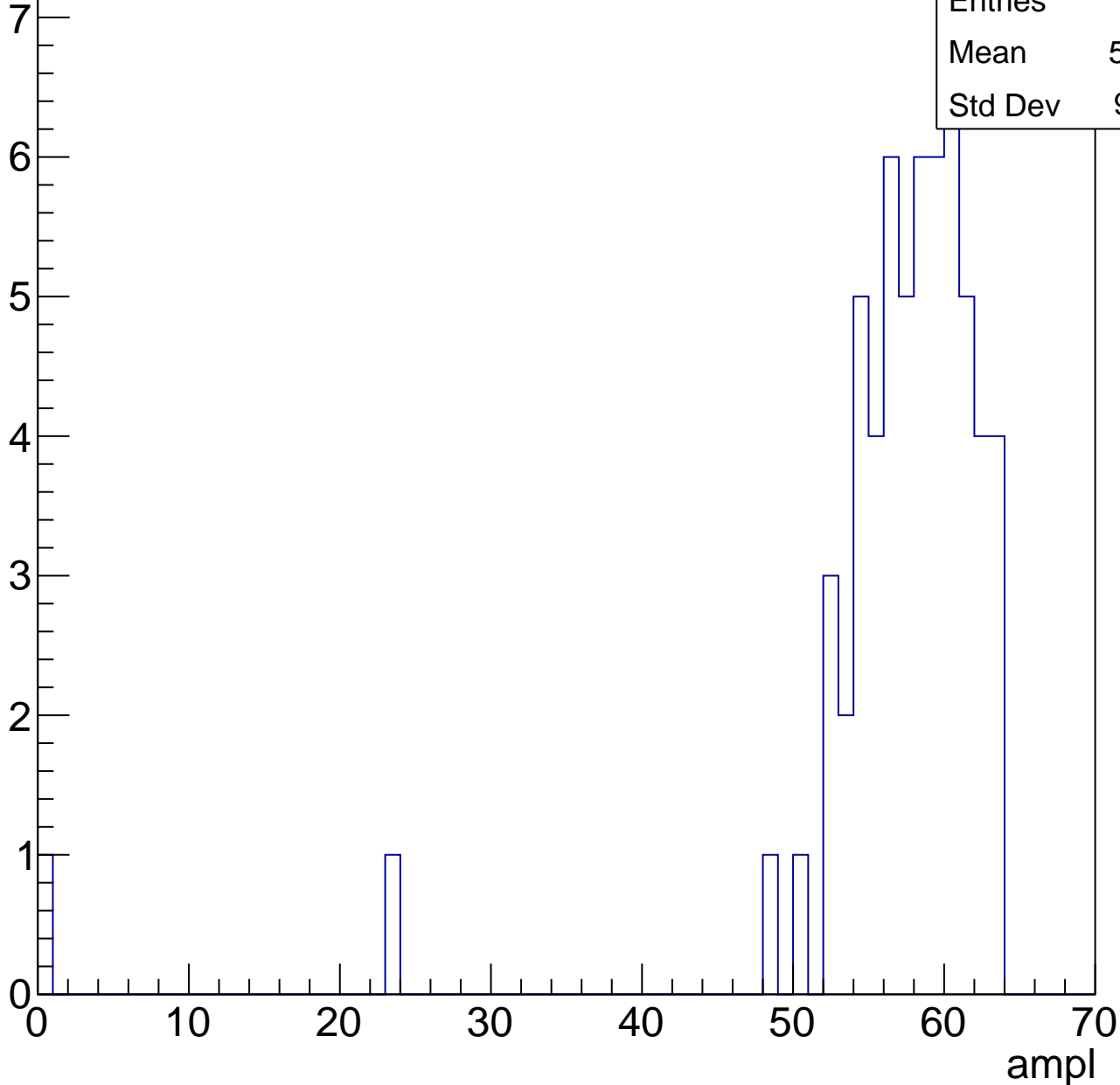


# B1L103S, U3-ch106, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	56.08
Std Dev	9.121

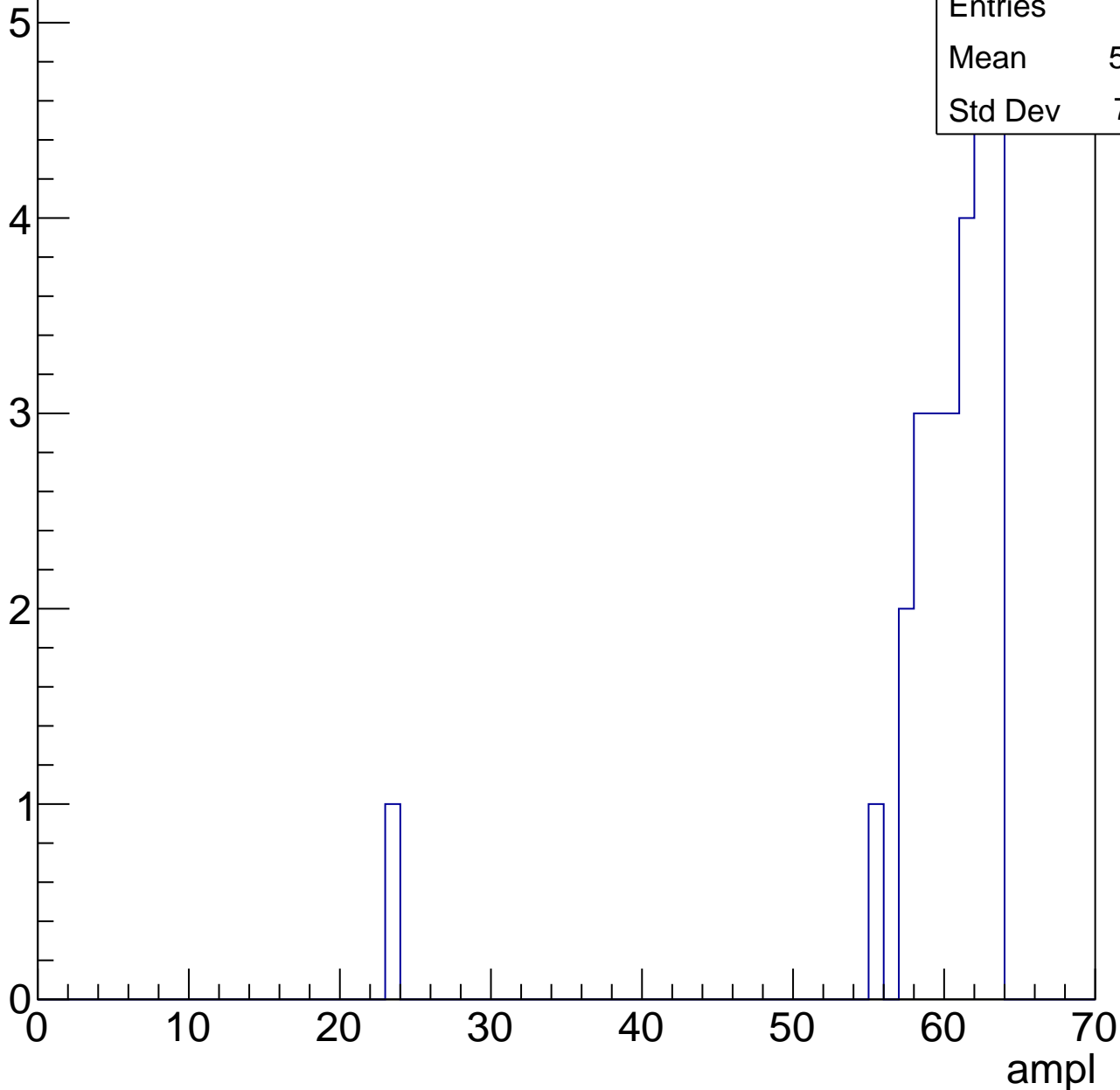


# B1L103S, U3-ch106, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	27
Mean	58.96
Std Dev	7.371

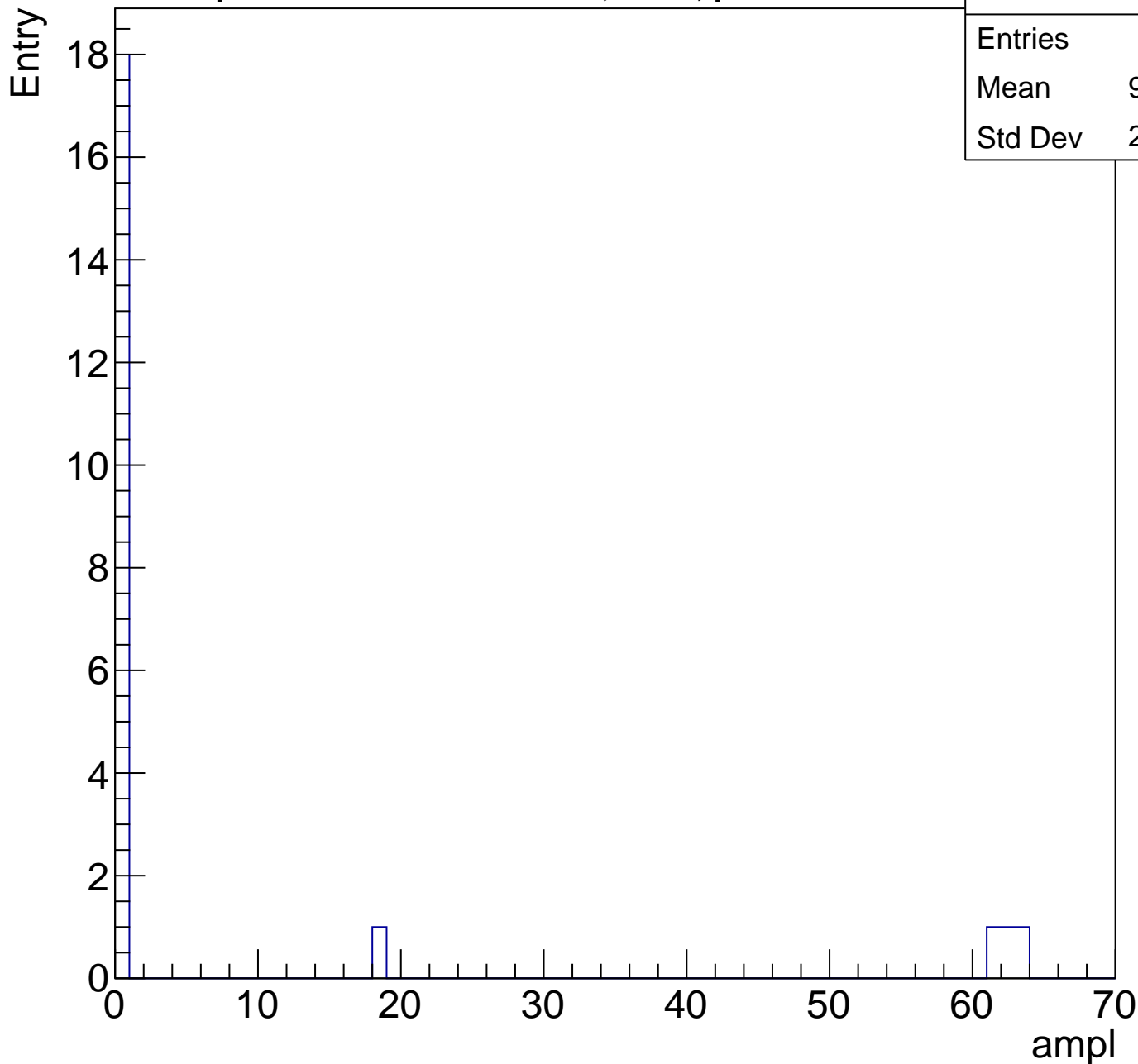




# B1L103S, U3-ch106, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	22
Mean	9.273
Std Dev	21.28



# B1L103S, U3-ch107, adc0

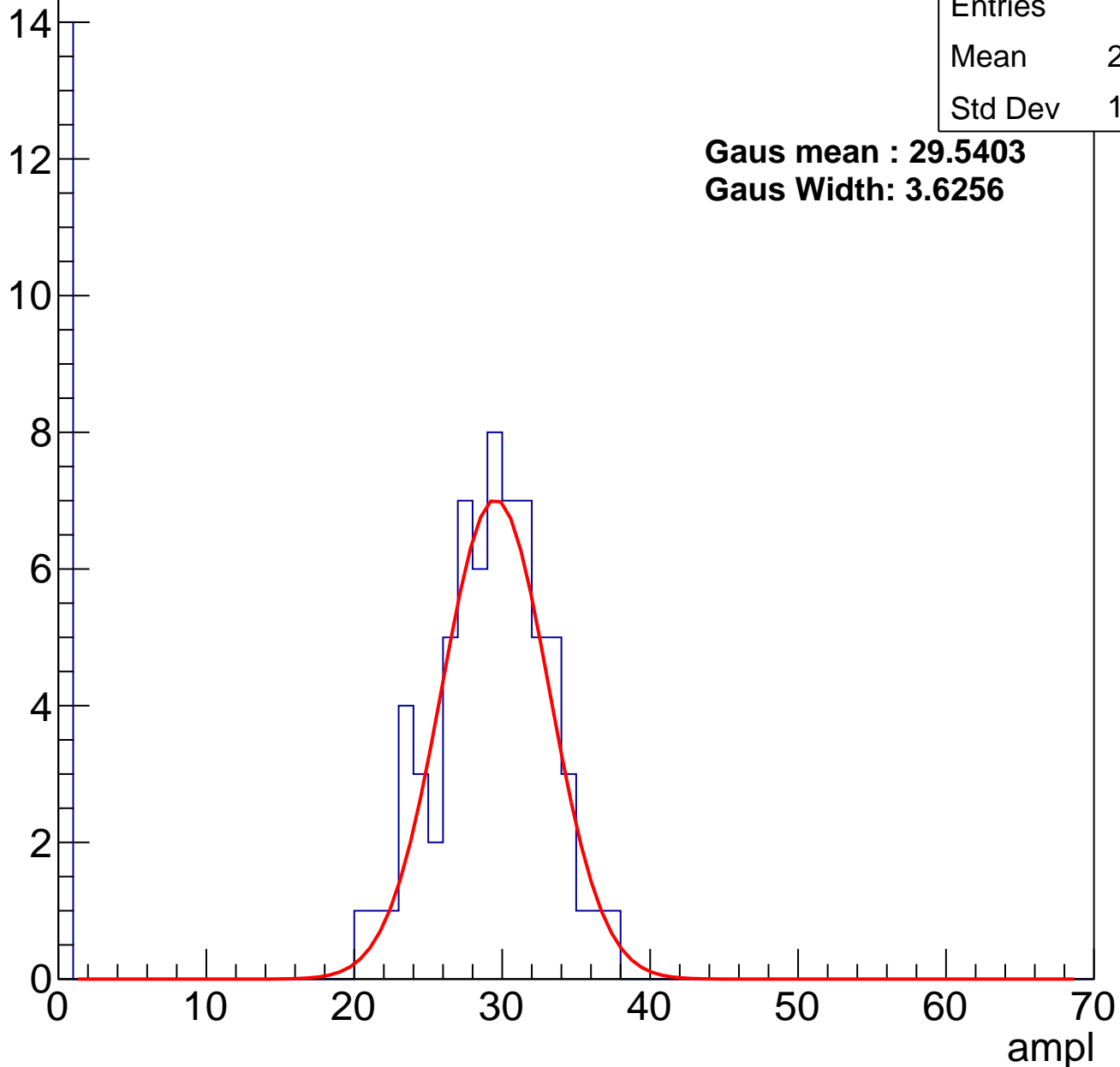
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	82
Mean	23.88
Std Dev	11.33

**Gaus mean : 29.5403**

**Gaus Width: 3.6256**

Entry



# B1L103S, U3-ch107, adc1

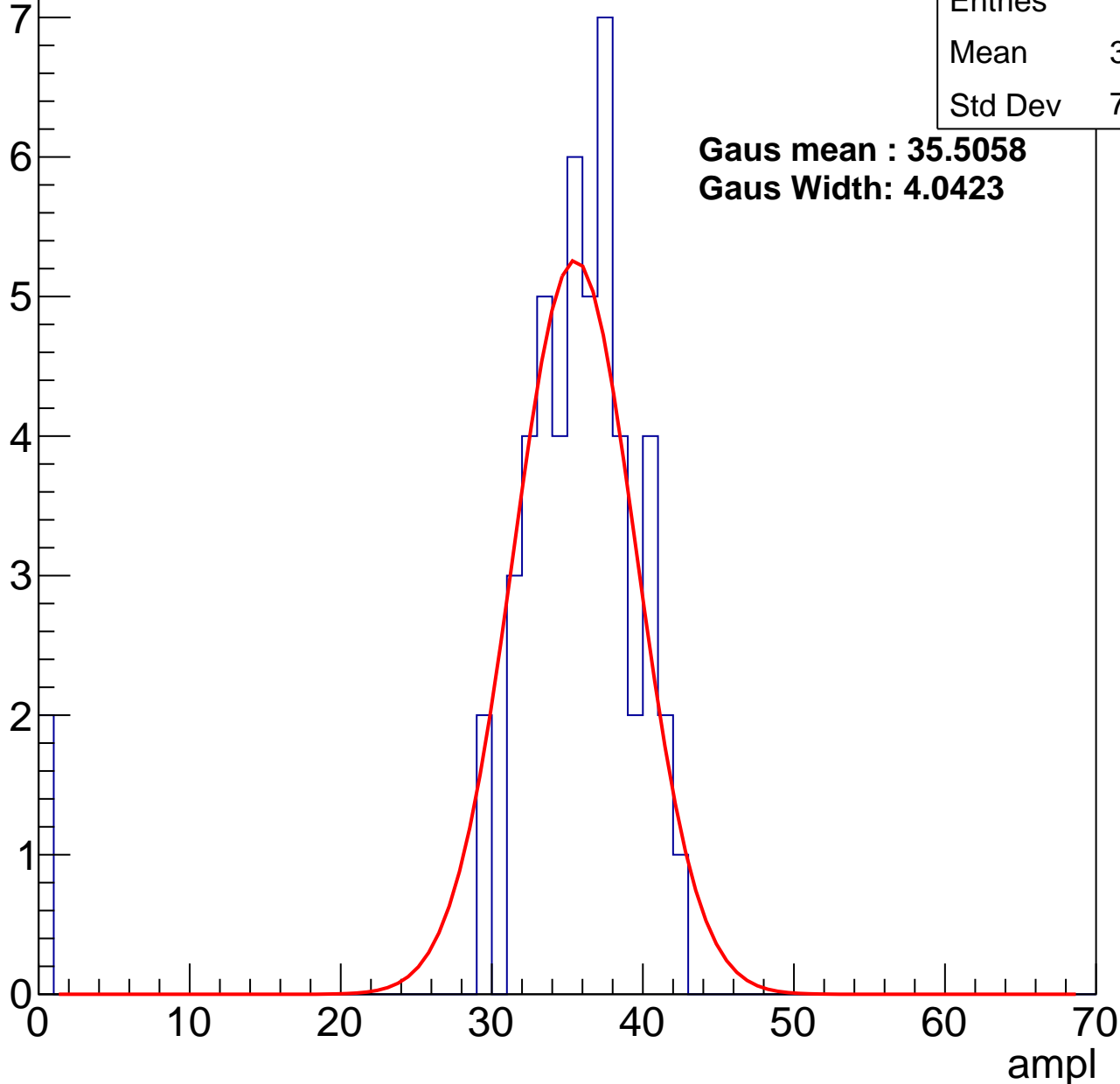
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	51
Mean	34.18
Std Dev	7.563

**Gaus mean : 35.5058**

**Gaus Width: 4.0423**



# B1L103S, U3-ch107, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	88
Mean	35.76
Std Dev	14

**Gaus mean : 41.6426**

**Gaus Width: 4.1563**

Entry

10

8

6

4

2

0

0

10

20

30

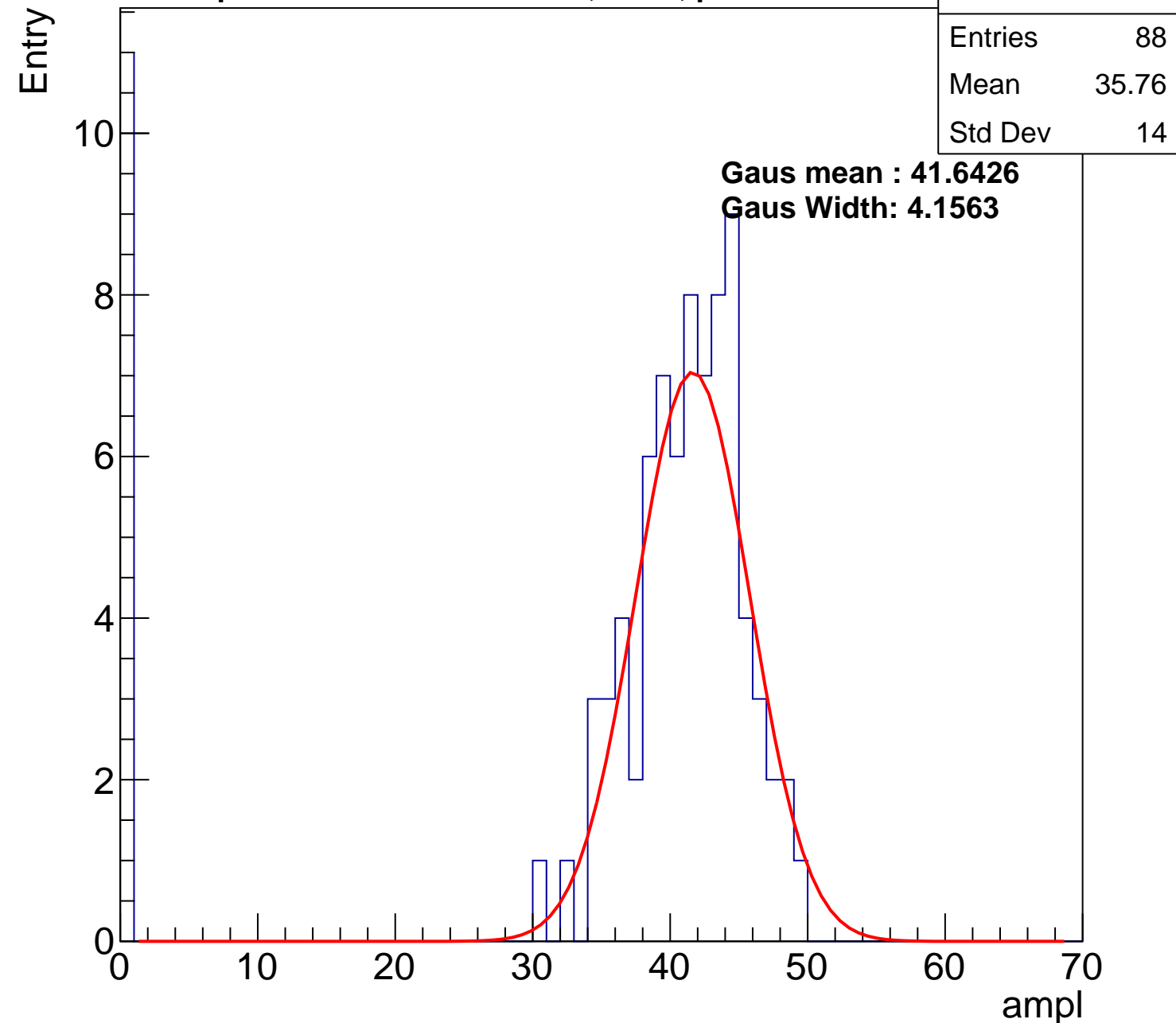
40

50

60

70

ampl

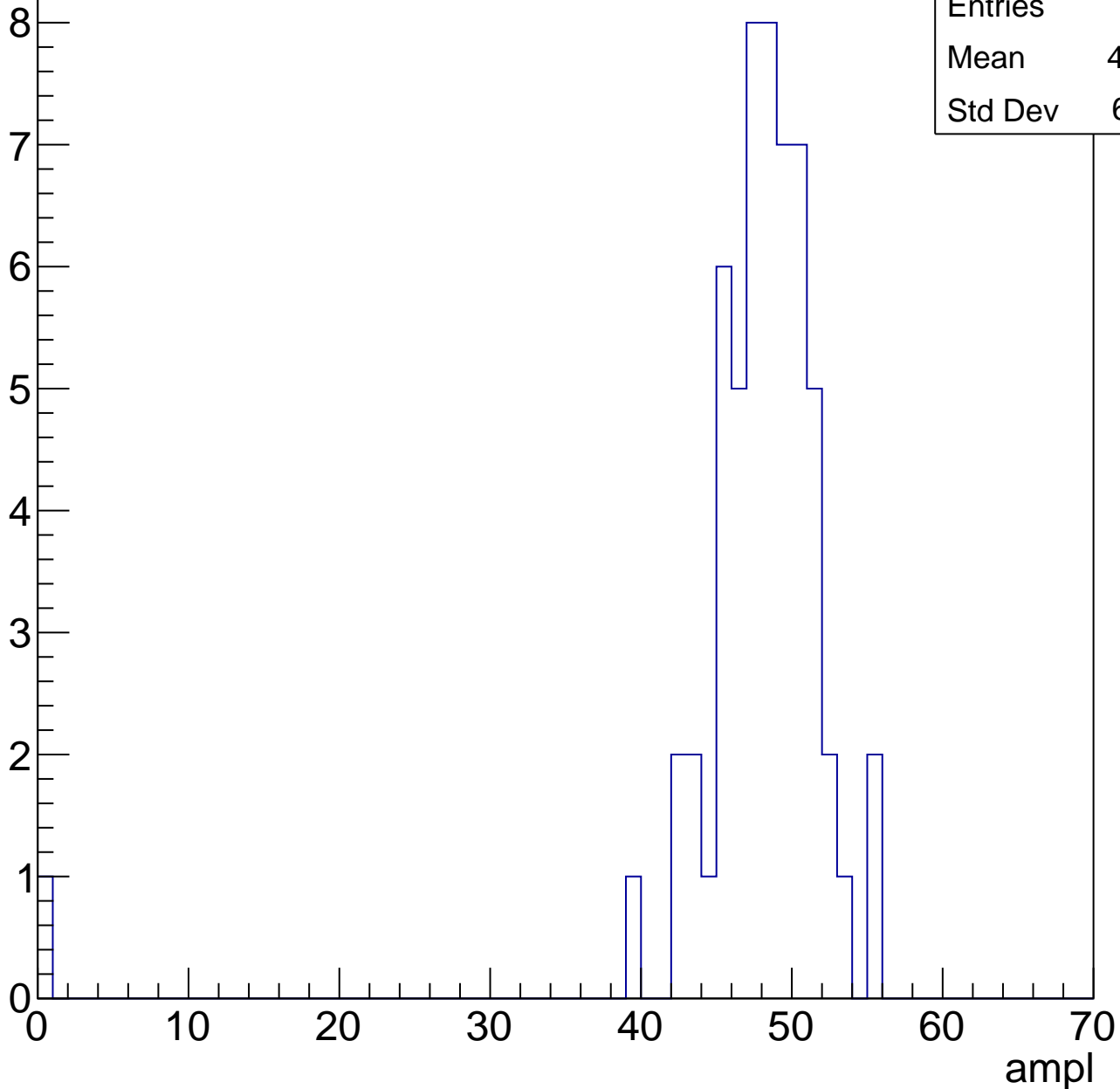


# B1L103S, U3-ch107, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

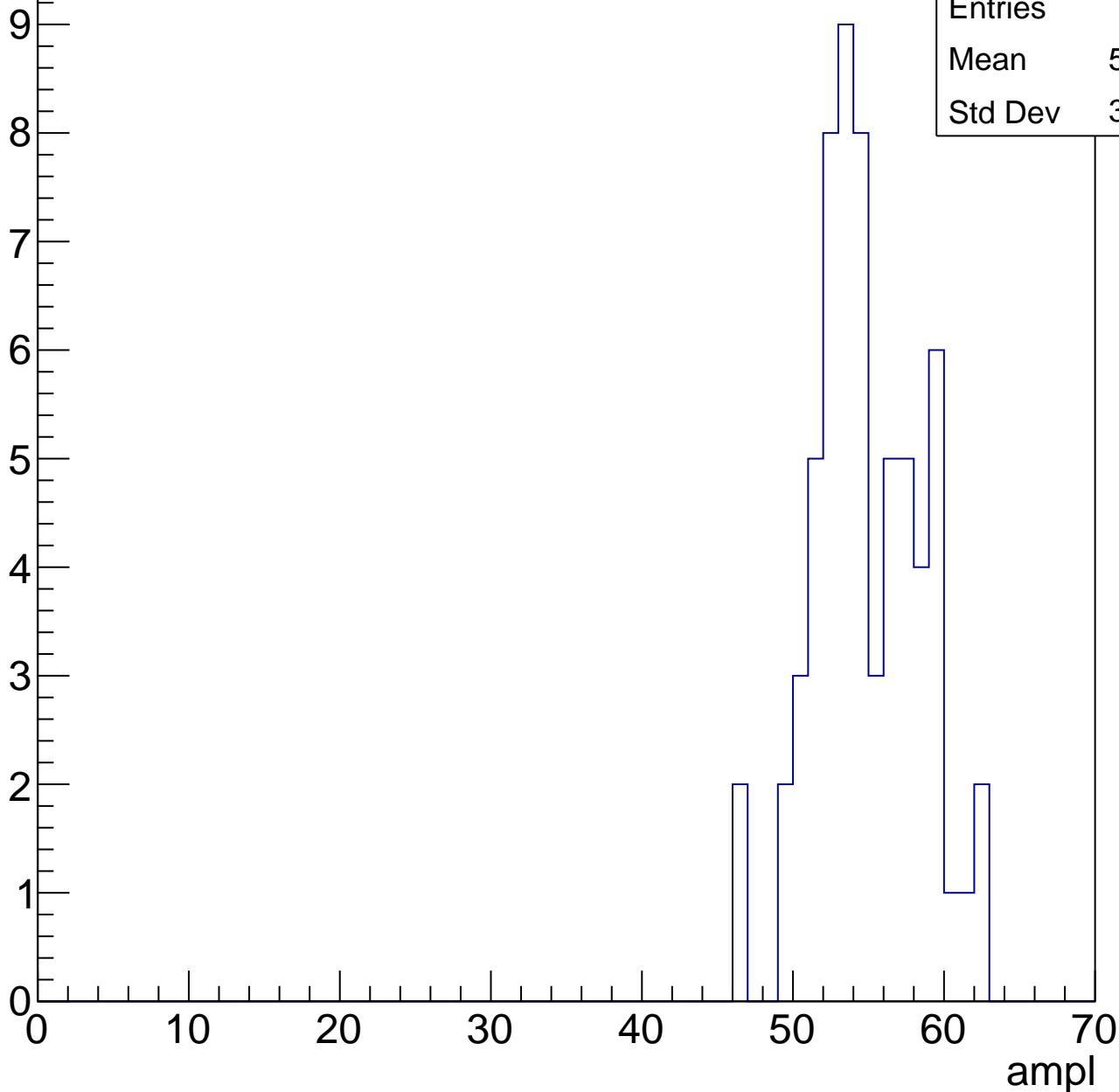
Entries	58
Mean	47.03
Std Dev	6.931



# B1L103S, U3-ch107, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



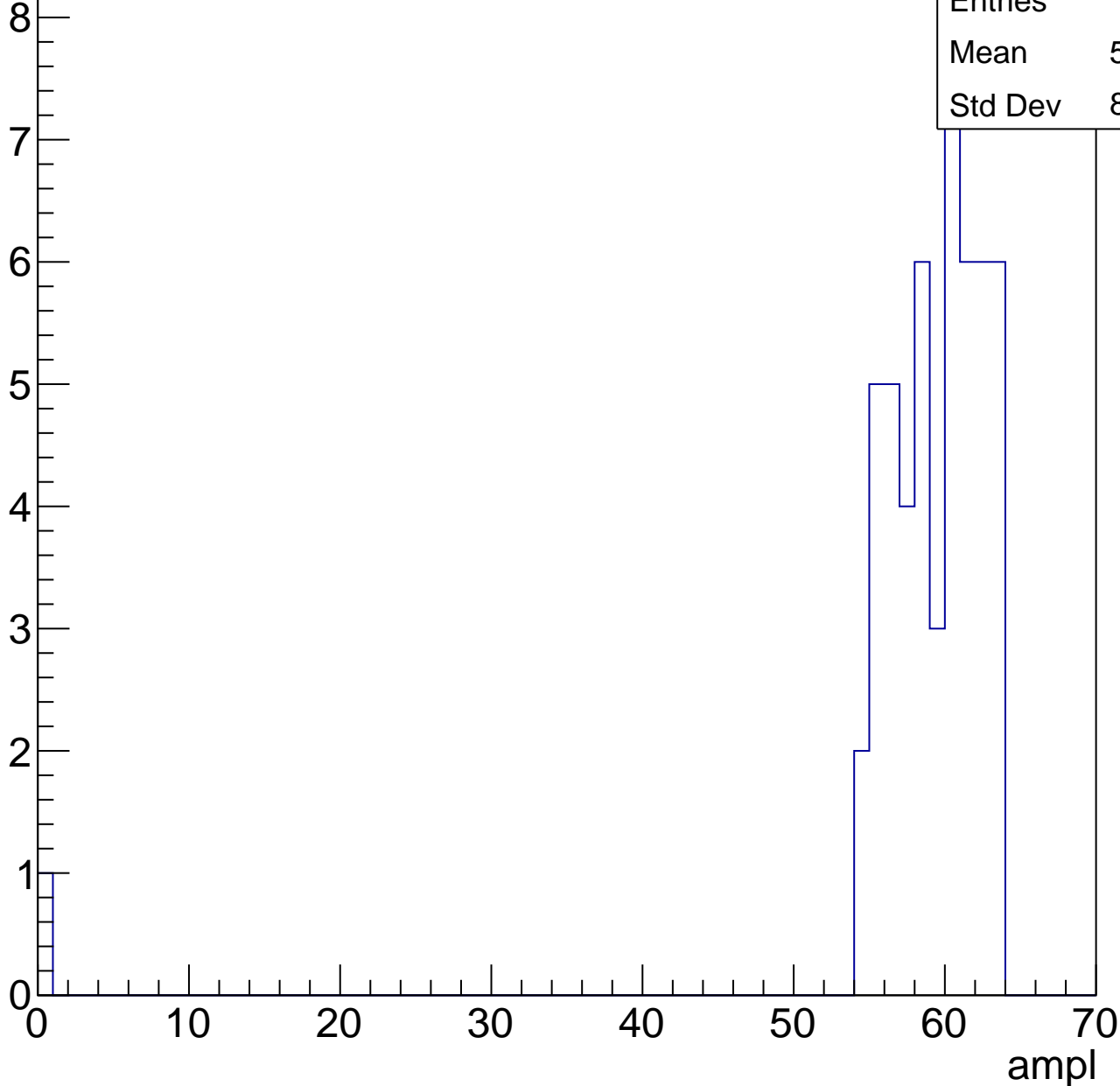
Entries	64
Mean	54.39
Std Dev	3.529

# B1L103S, U3-ch107, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

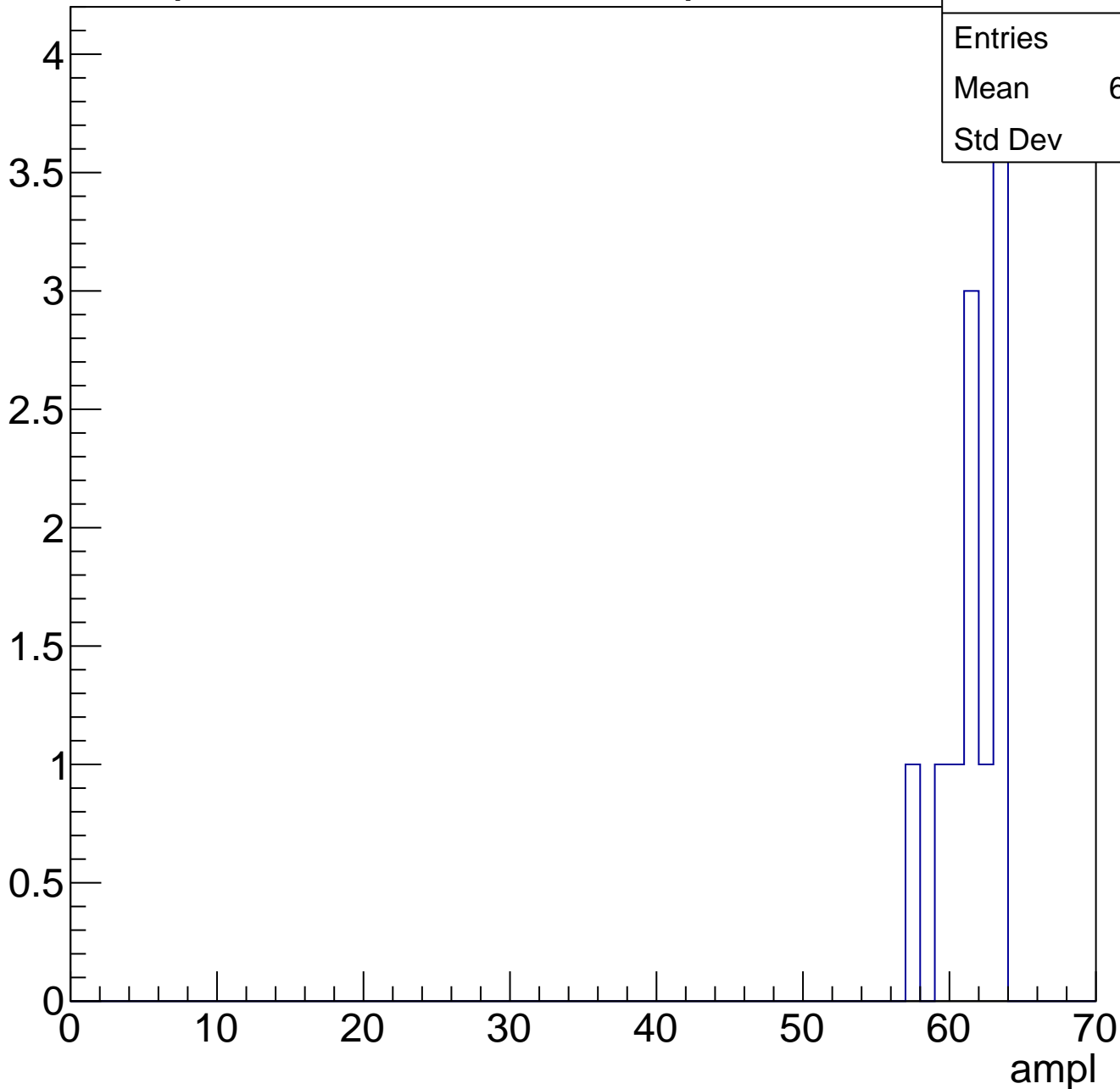
Entries	52
Mean	57.92
Std Dev	8.548



# B1L103S, U3-ch107, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U3-ch107, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	3.263
Std Dev	13.84

Entry



# B1L103S, U3-ch108, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	98
Mean	23.98
Std Dev	10.74

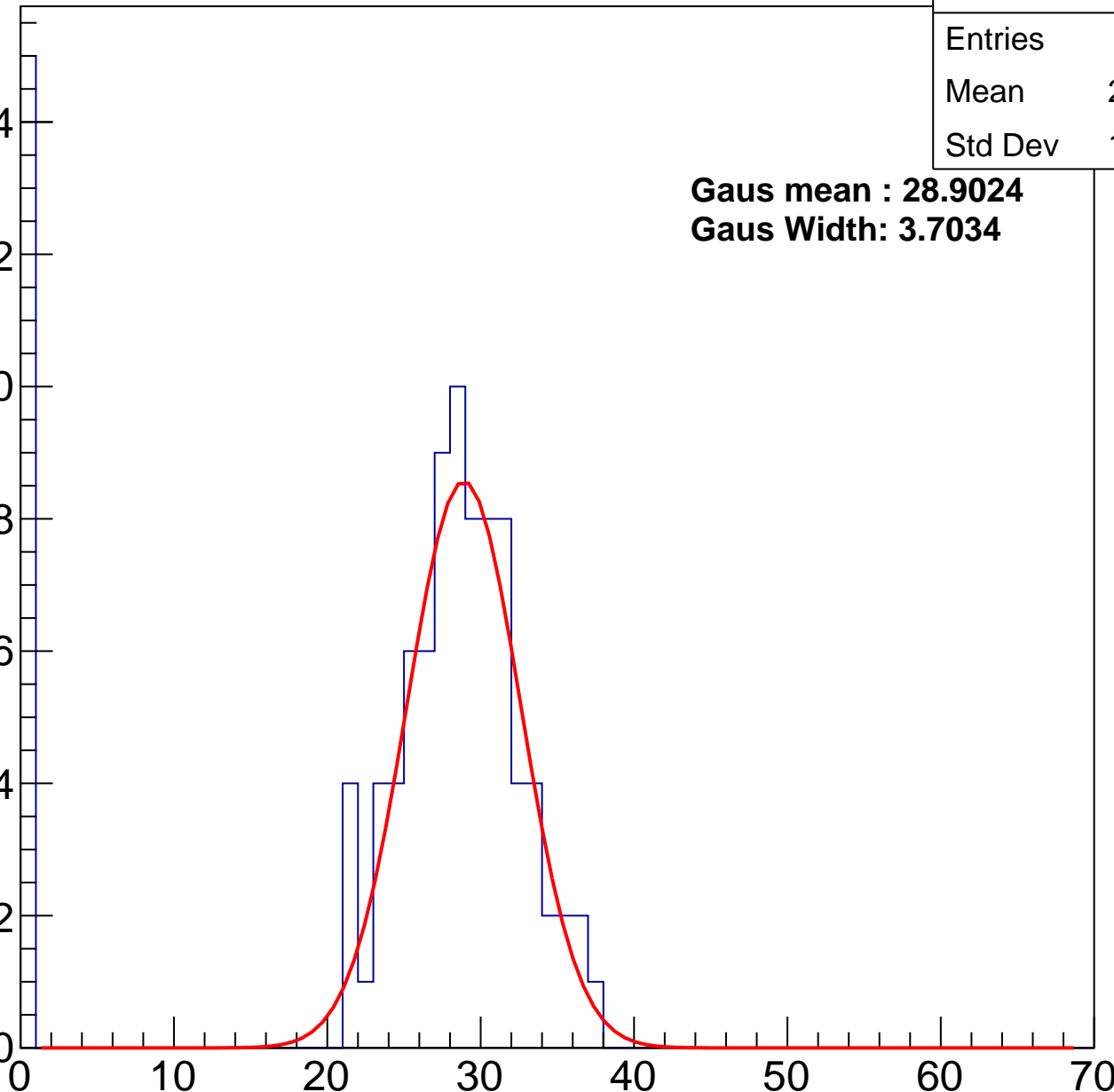
**Gaus mean : 28.9024**

**Gaus Width: 3.7034**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U3-ch108, adc1

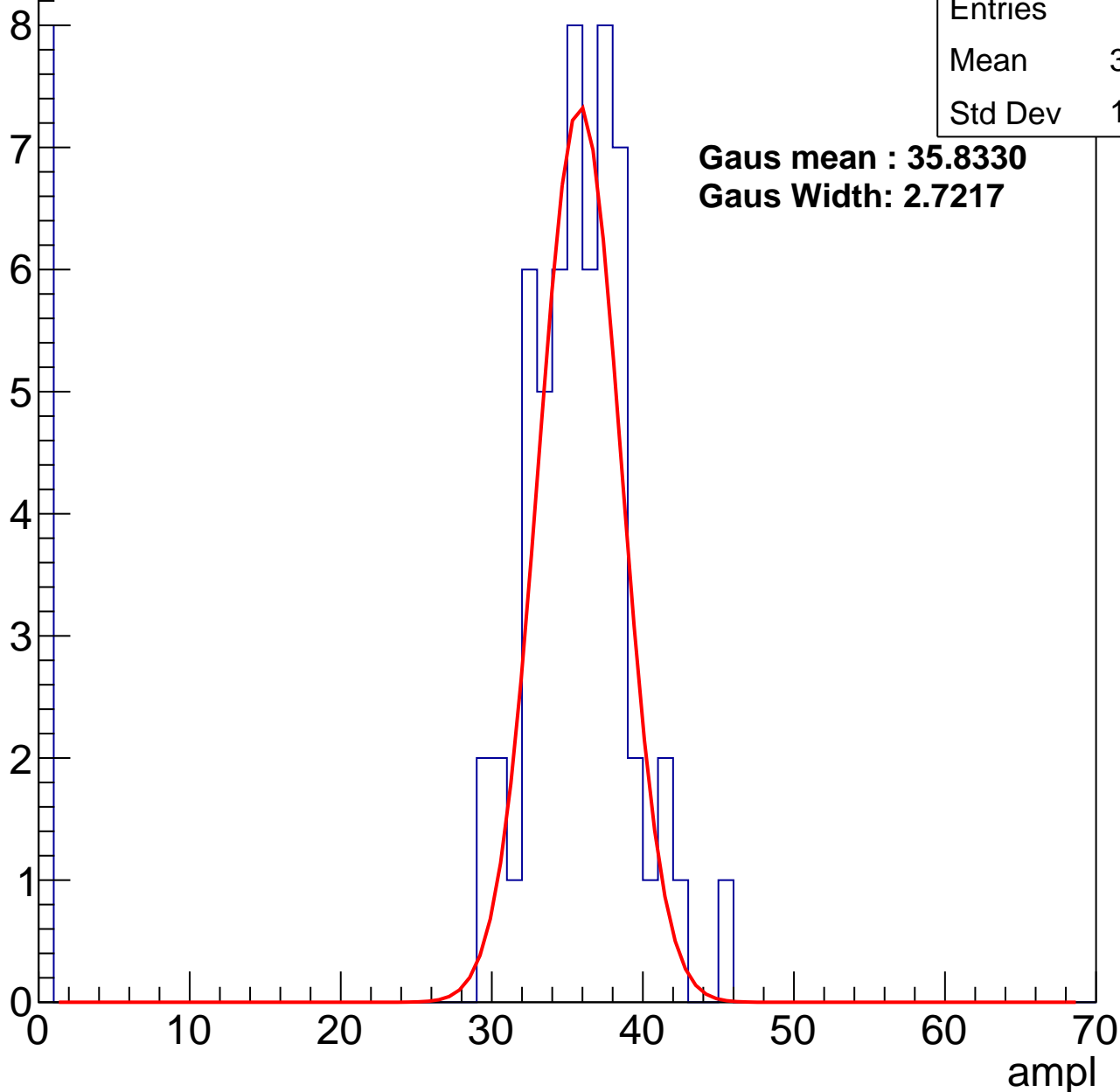
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	31.14
Std Dev	11.94

**Gaus mean : 35.8330**

**Gaus Width: 2.7217**



# B1L103S, U3-ch108, adc2

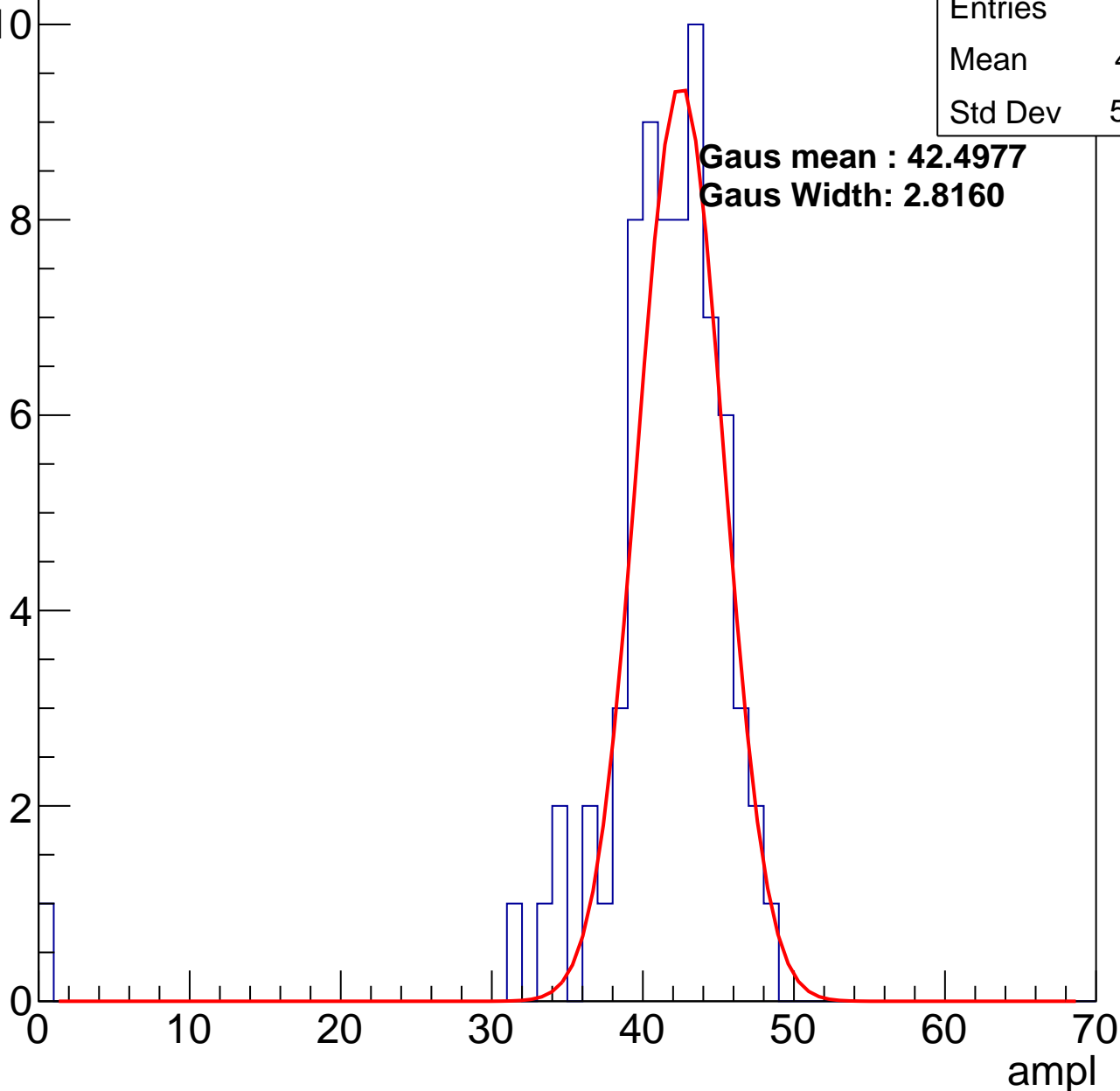
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	40.81
Std Dev	5.825

**Gaus mean : 42.4977**

**Gaus Width: 2.8160**

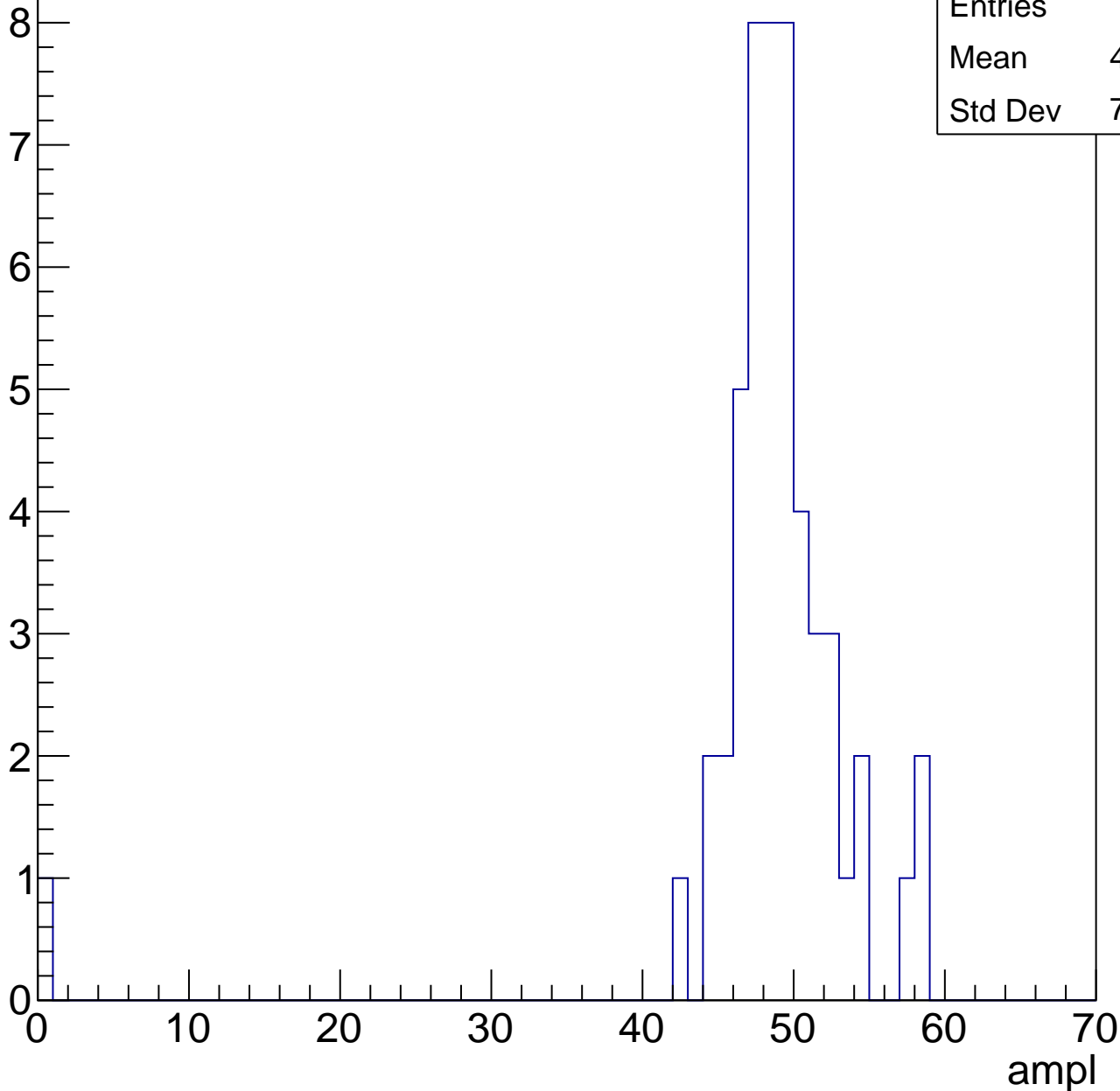


# B1L103S, U3-ch108, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	51
Mean	47.94
Std Dev	7.534

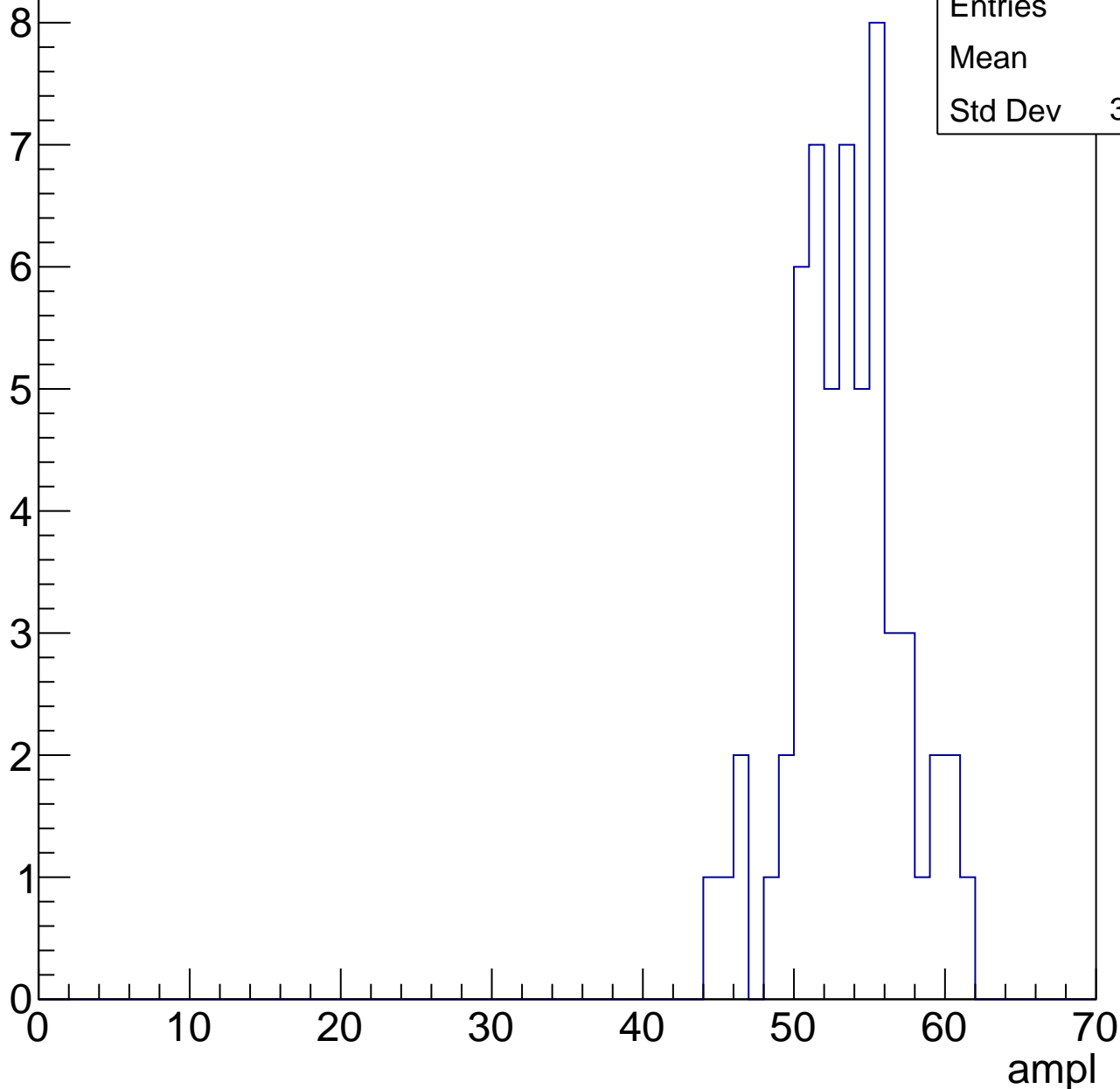


# B1L103S, U3-ch108, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	57
Mean	53
Std Dev	3.647

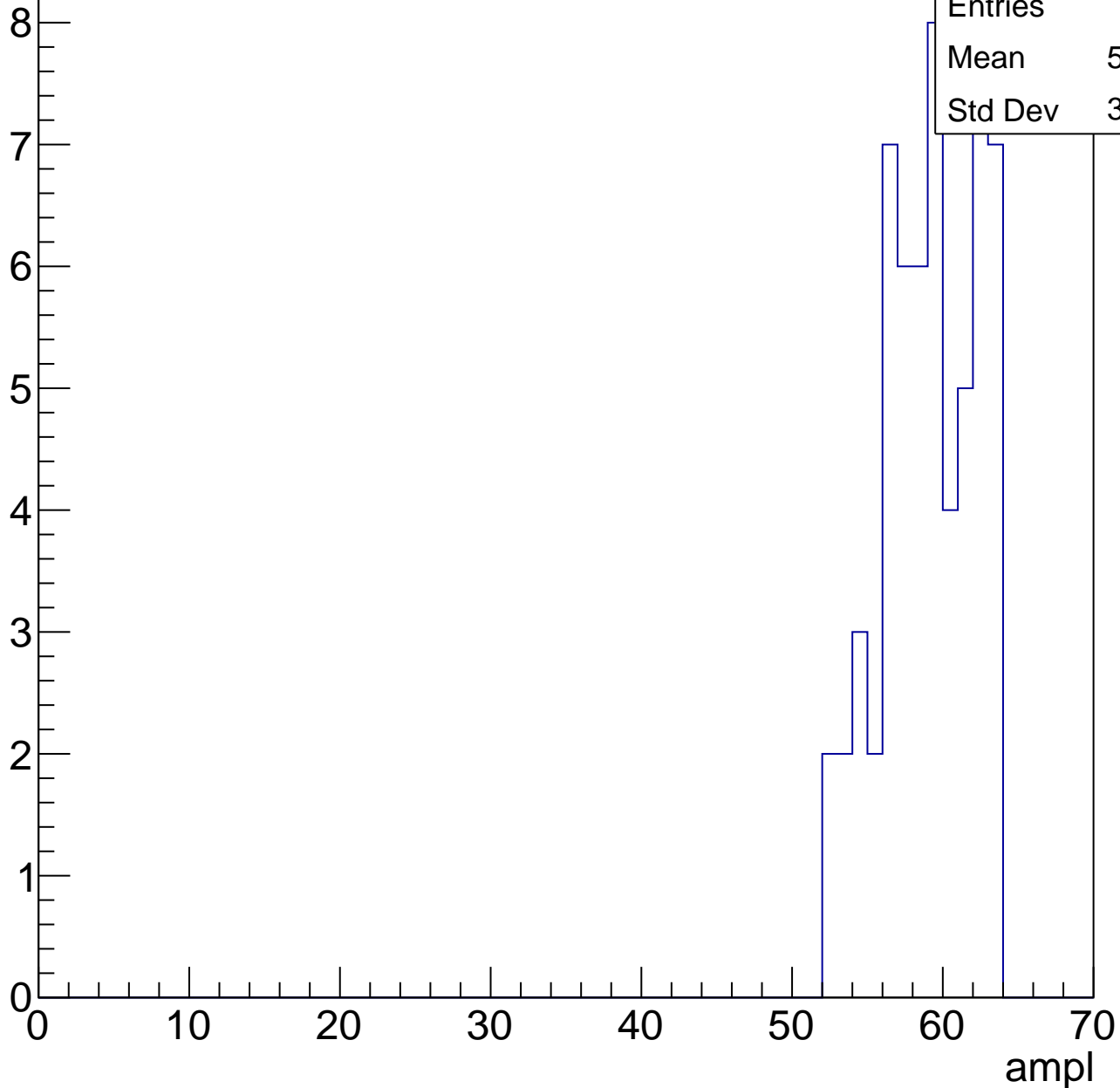


# B1L103S, U3-ch108, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

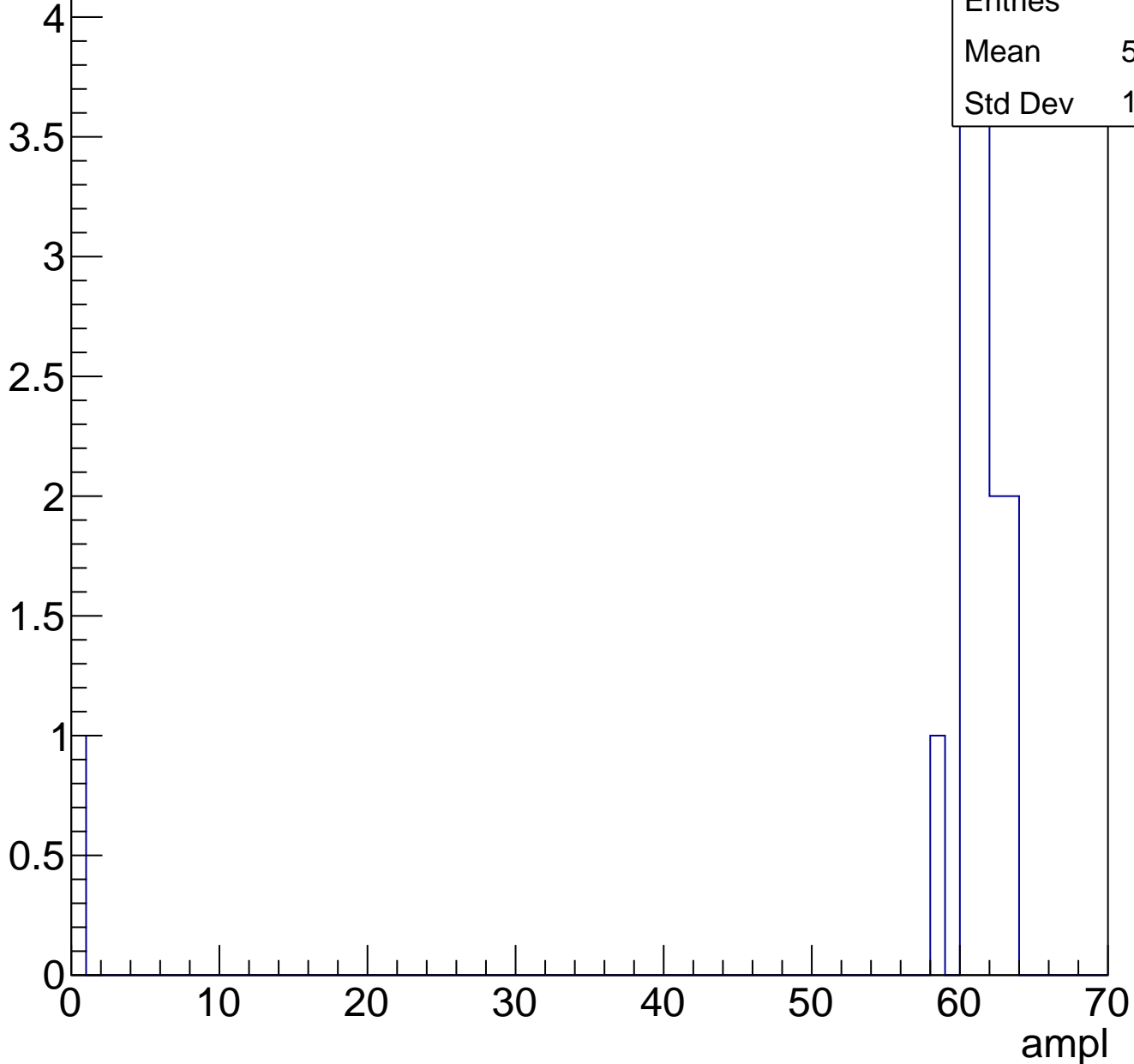
Entries	60
Mean	58.63
Std Dev	3.082



# B1L103S, U3-ch108, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U3-ch108, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73



# B1L103S, U3-ch109, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	78
Mean	24.97
Std Dev	10.18

**Gaus mean : 28.3917**

**Gaus Width: 3.4095**

Entry

10

8

6

4

2

0

0

10

20

30

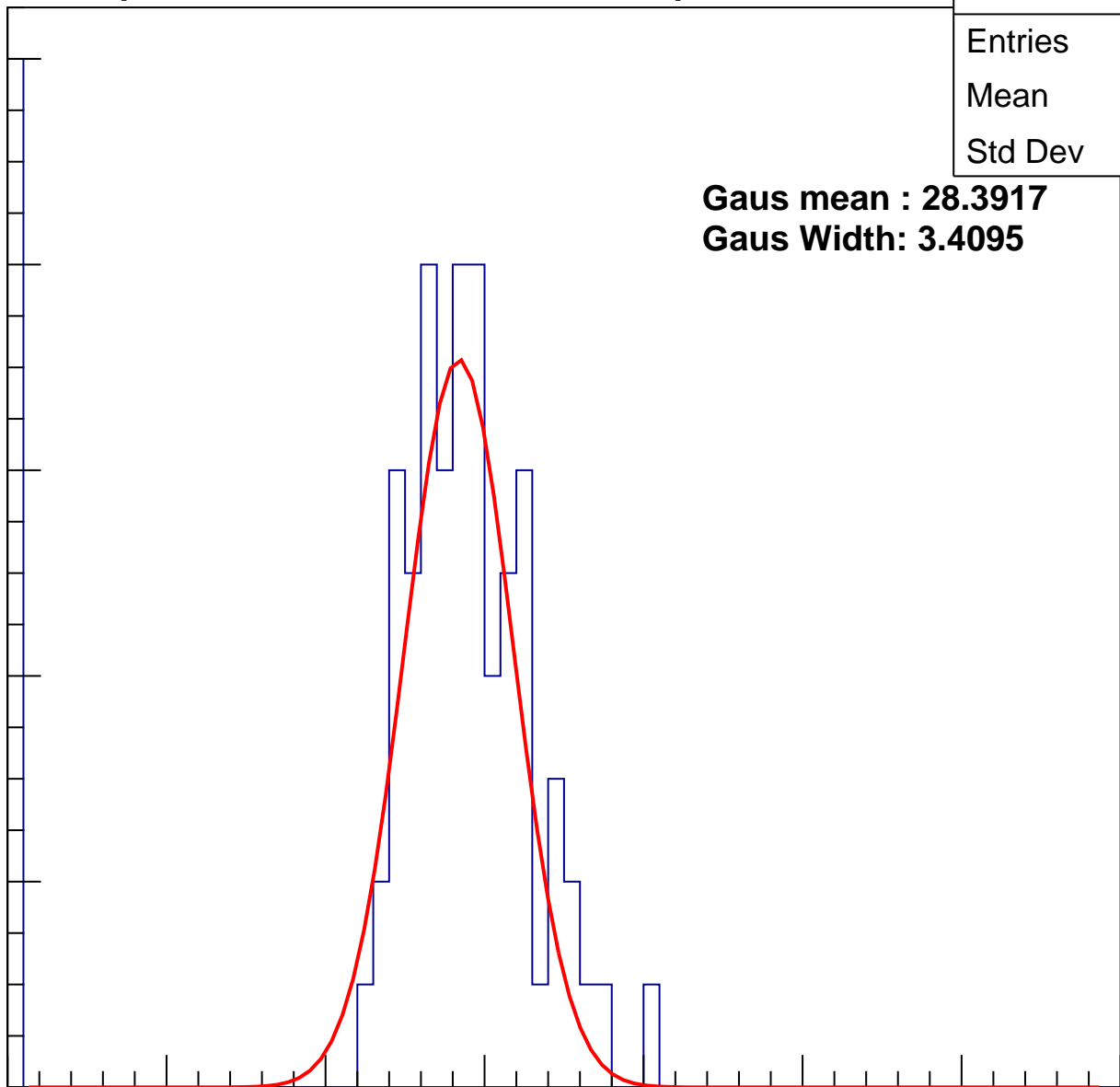
40

50

60

70

ampl



# B1L103S, U3-ch109, adc1

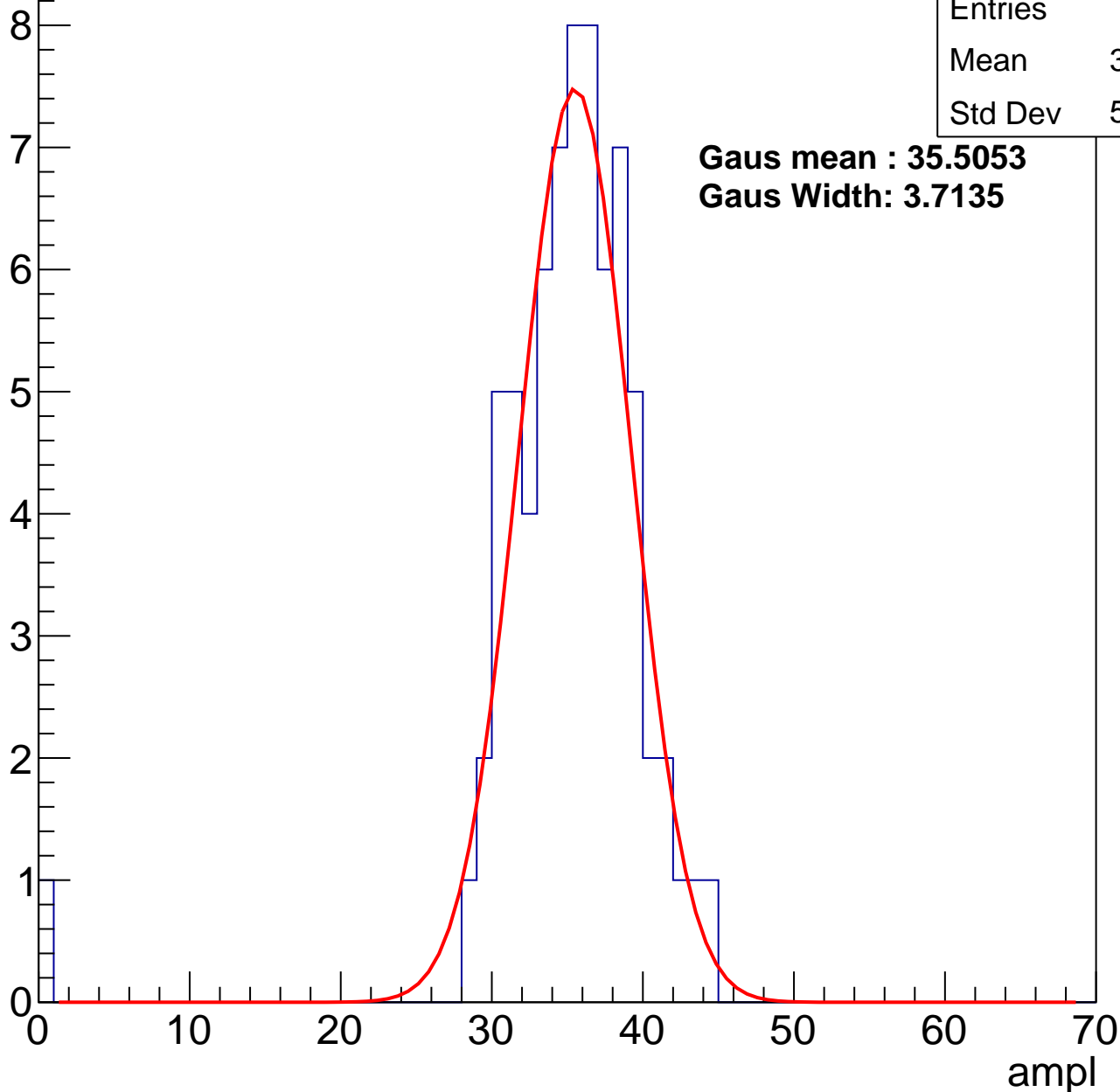
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	72
Mean	34.68
Std Dev	5.403

**Gaus mean : 35.5053**

**Gaus Width: 3.7135**



# B1L103S, U3-ch109, adc2

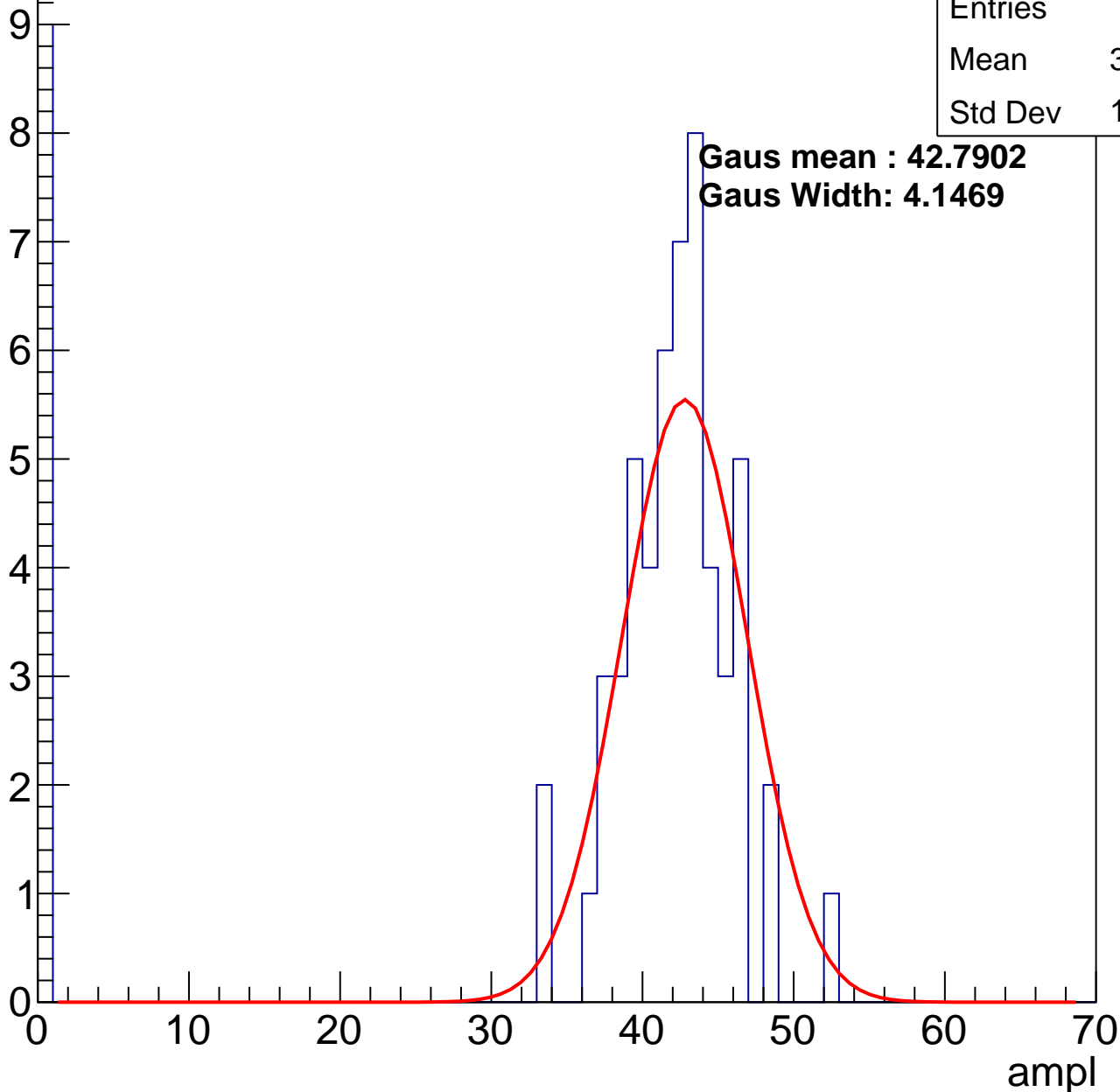
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	35.79
Std Dev	14.98

**Gaus mean : 42.7902**

**Gaus Width: 4.1469**

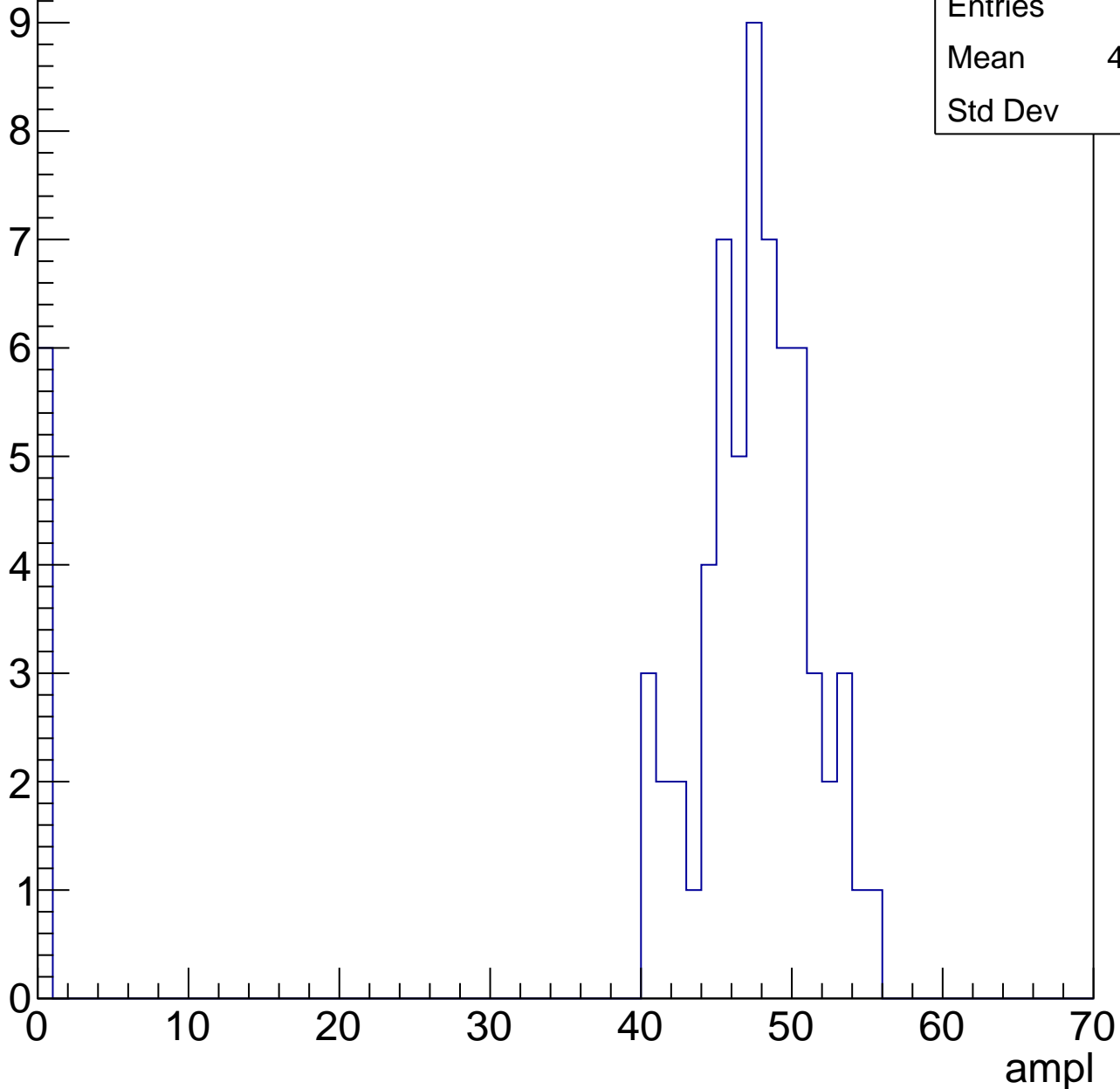


# B1L103S, U3-ch109, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

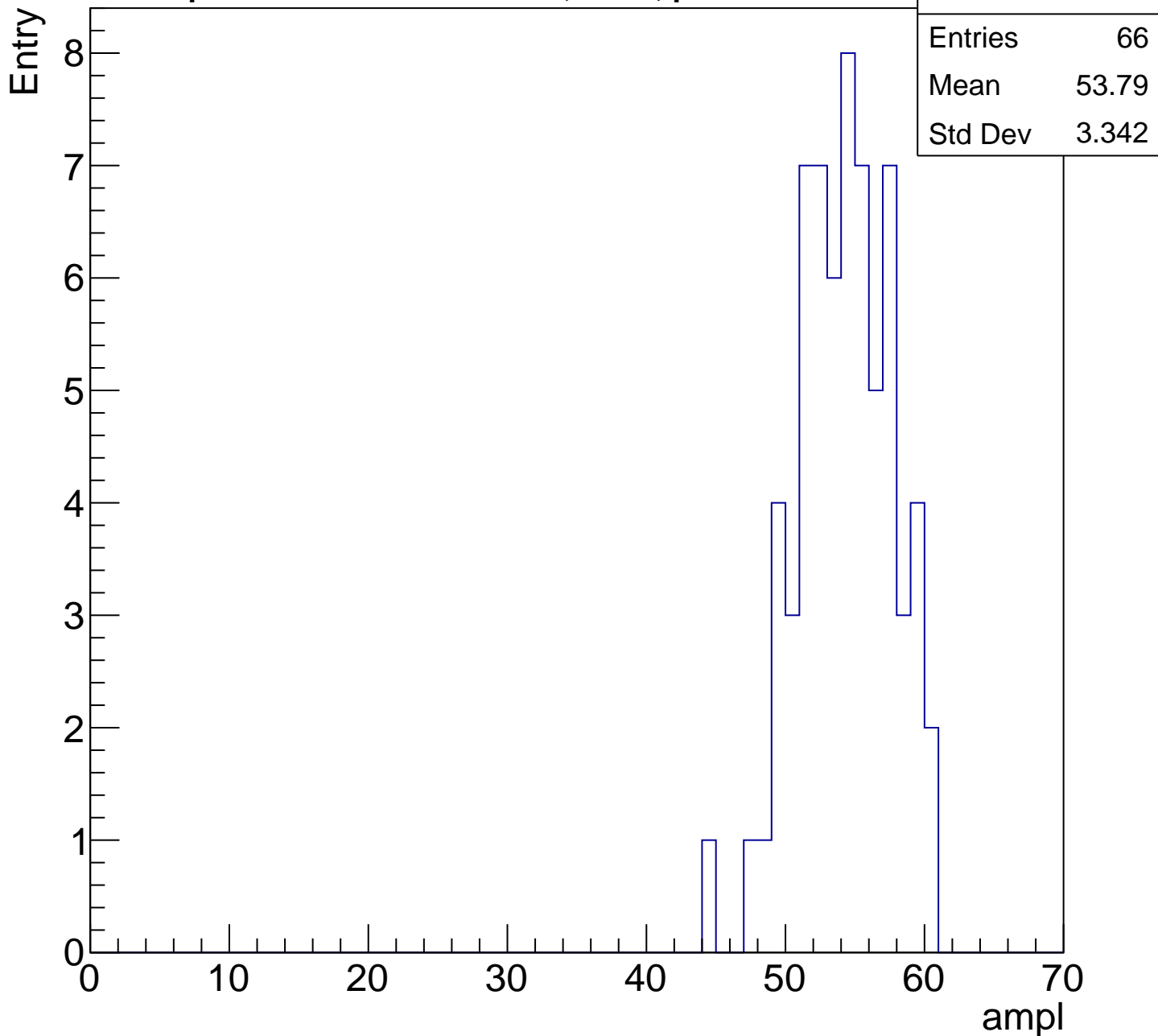
Entry

Entries	68
Mean	43.06
Std Dev	13.8



# B1L103S, U3-ch109, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

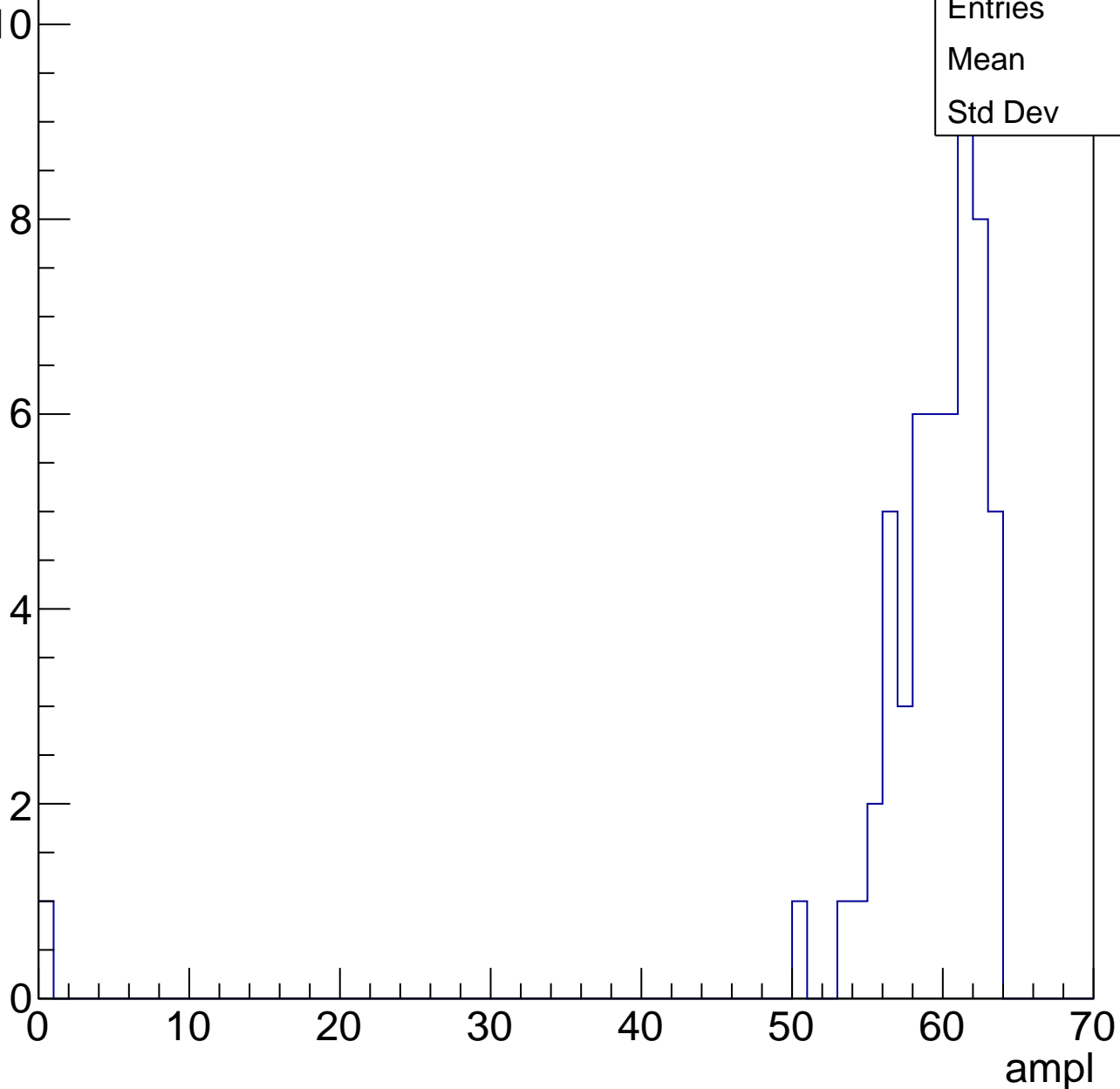


# B1L103S, U3-ch109, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

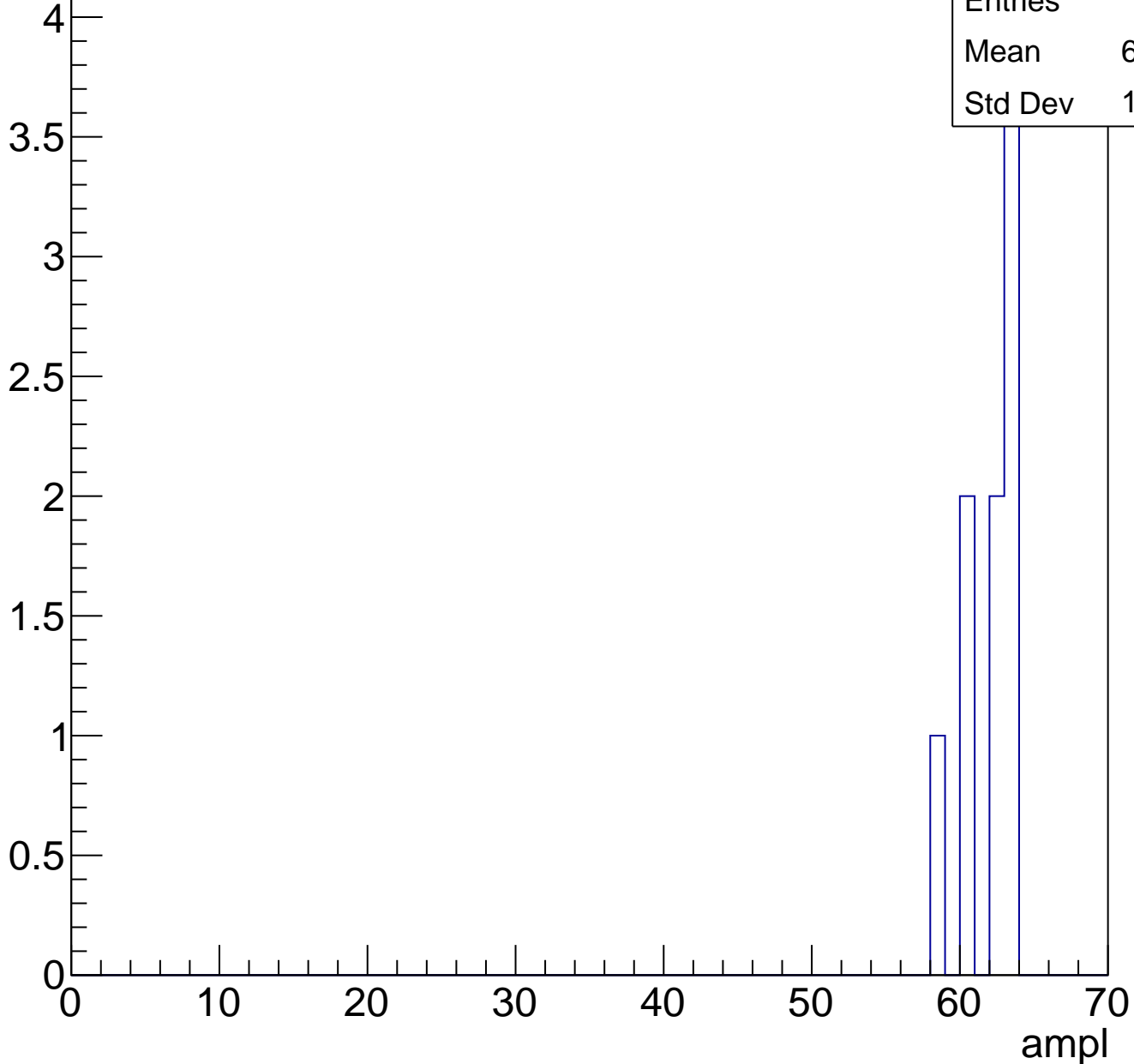
Entries	55
Mean	58.2
Std Dev	8.4



# B1L103S, U3-ch109, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



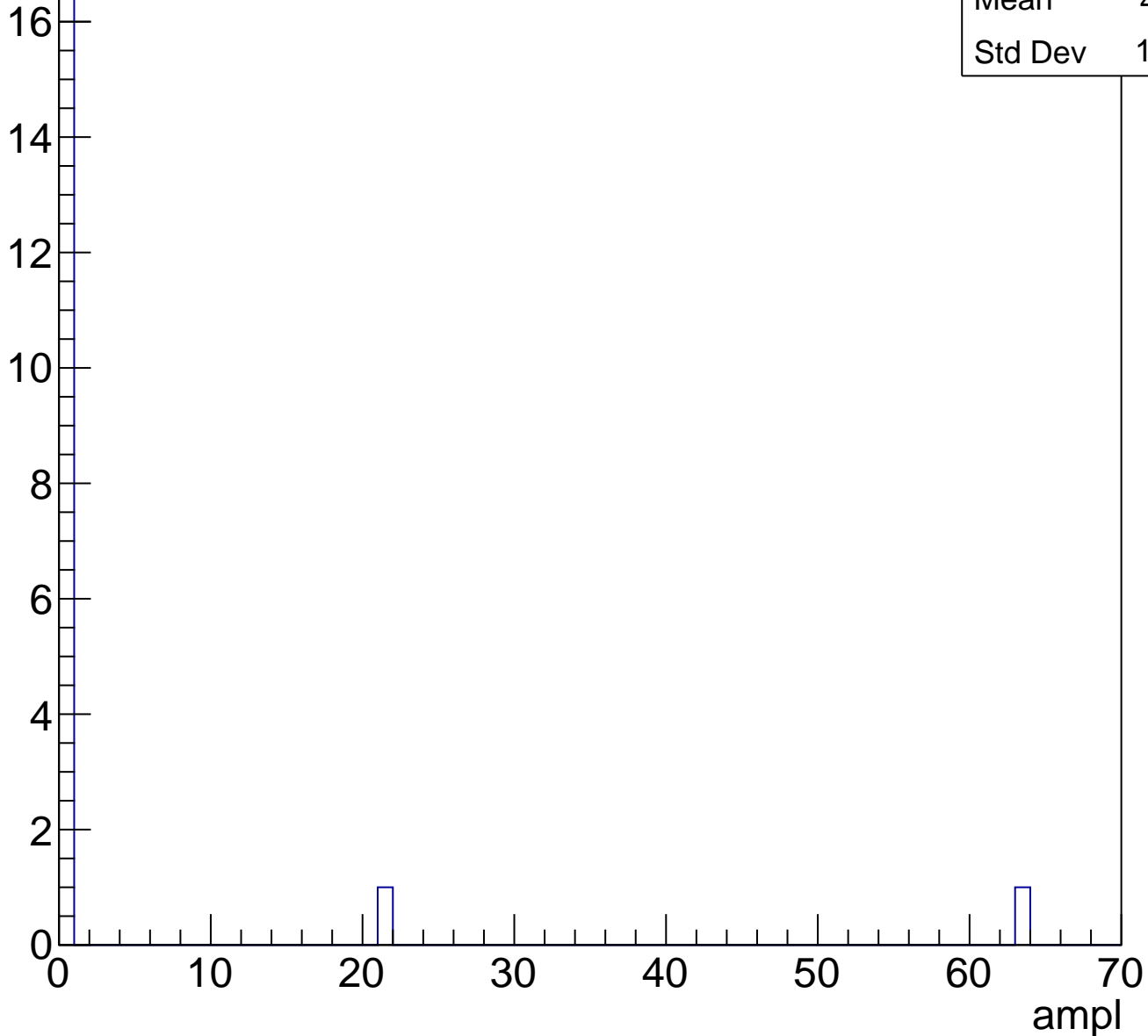


# B1L103S, U3-ch109, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	4.421
Std Dev	14.58

Entry



# B1L103S, U3-ch110, adc0

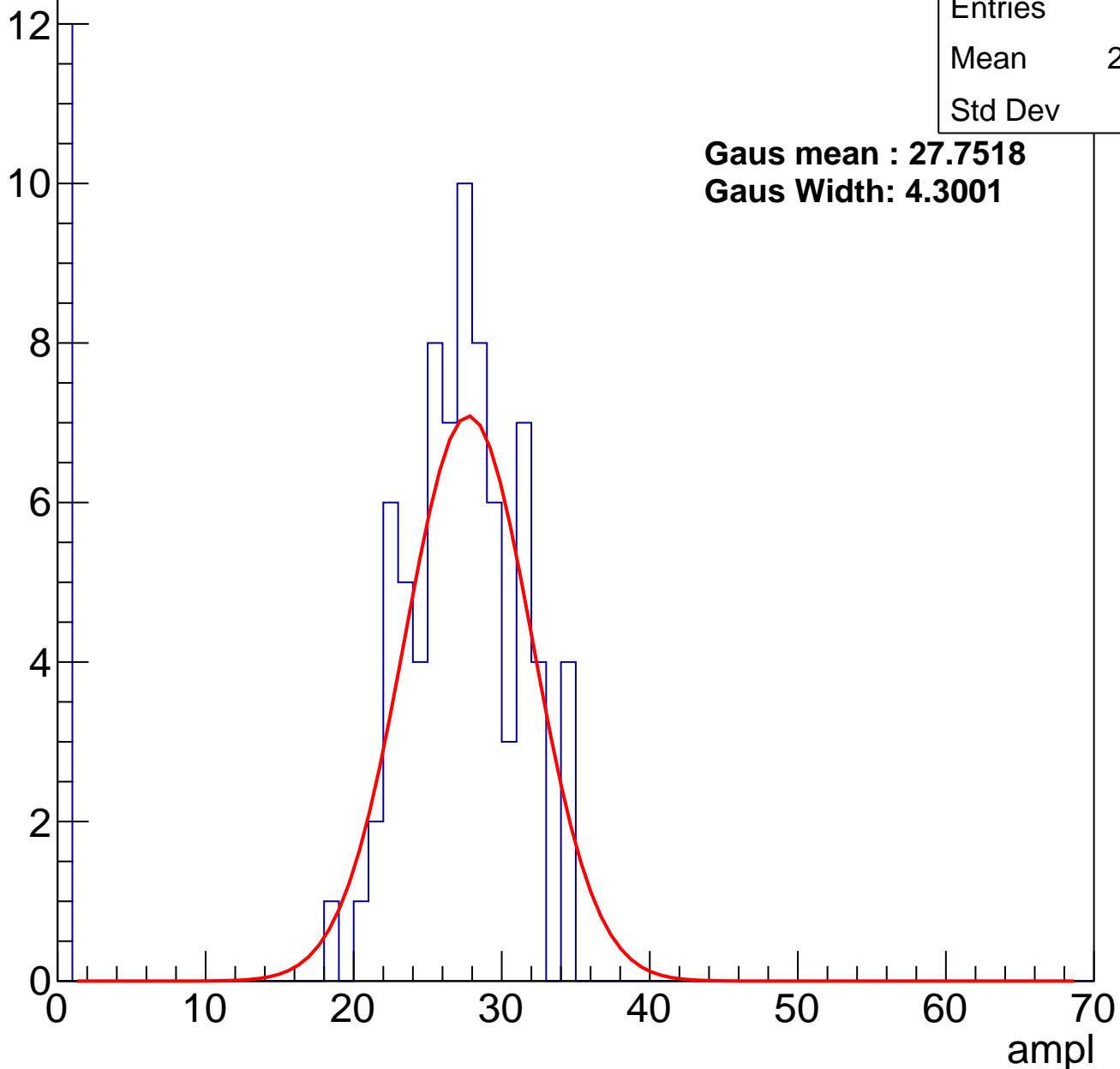
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	88
Mean	23.23
Std Dev	9.81

**Gaus mean : 27.7518**

**Gaus Width: 4.3001**

Entry



# B1L103S, U3-ch110, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	68
Mean	32.54
Std Dev	7.754

**Gaus mean : 34.3578**

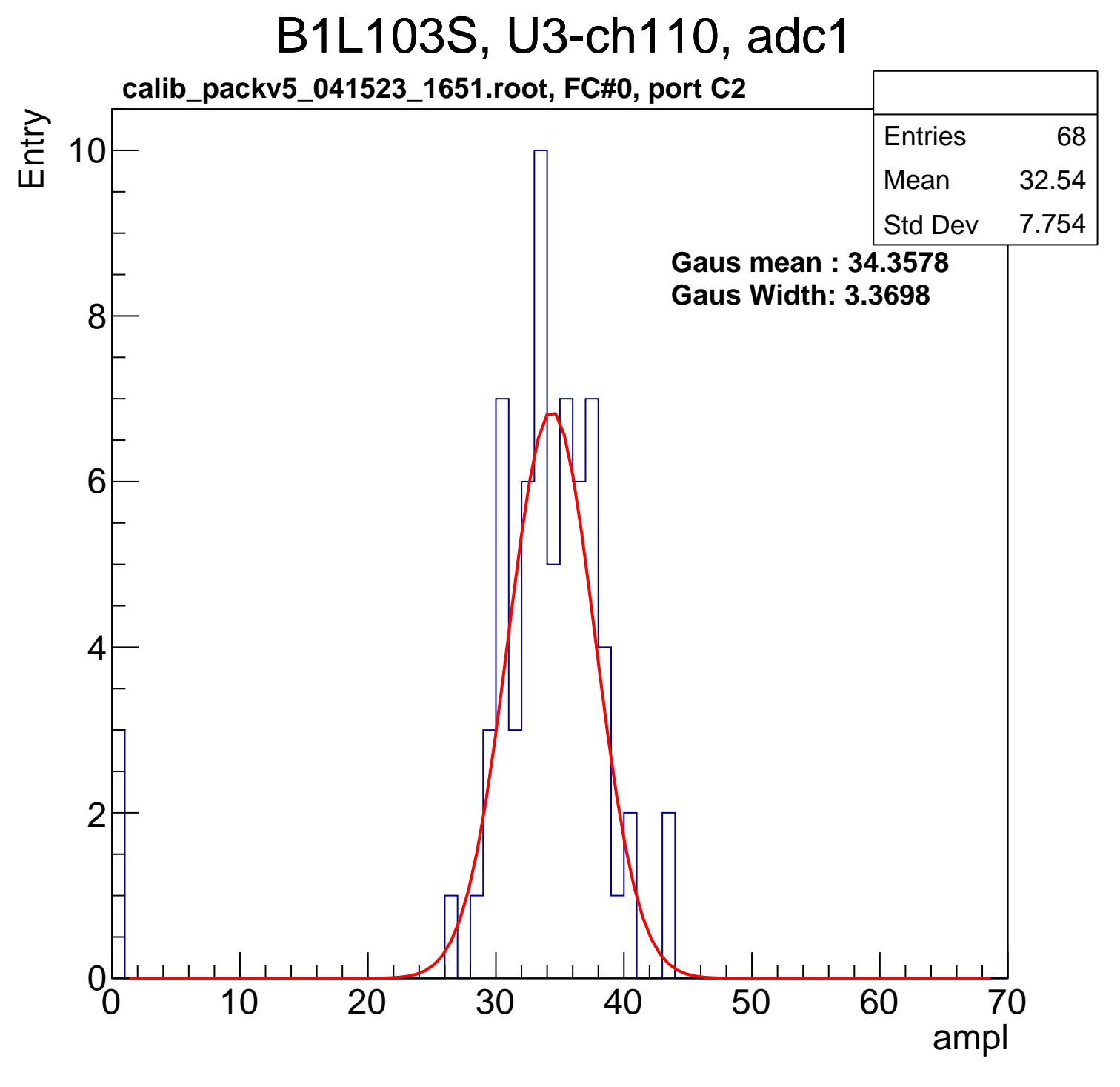
**Gaus Width: 3.3698**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch110, adc2

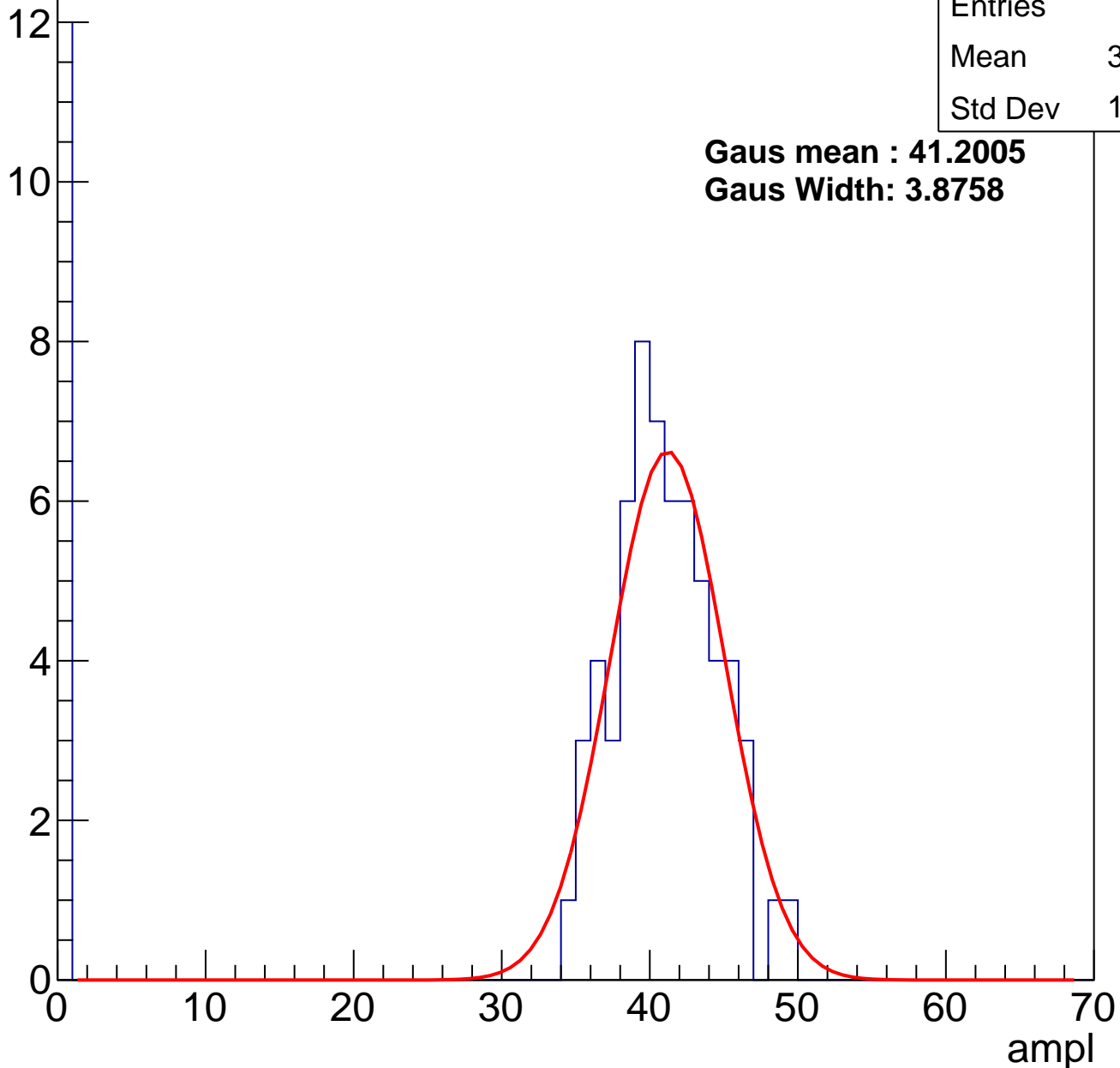
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	74
Mean	34.03
Std Dev	15.28

**Gaus mean : 41.2005**

**Gaus Width: 3.8758**

Entry

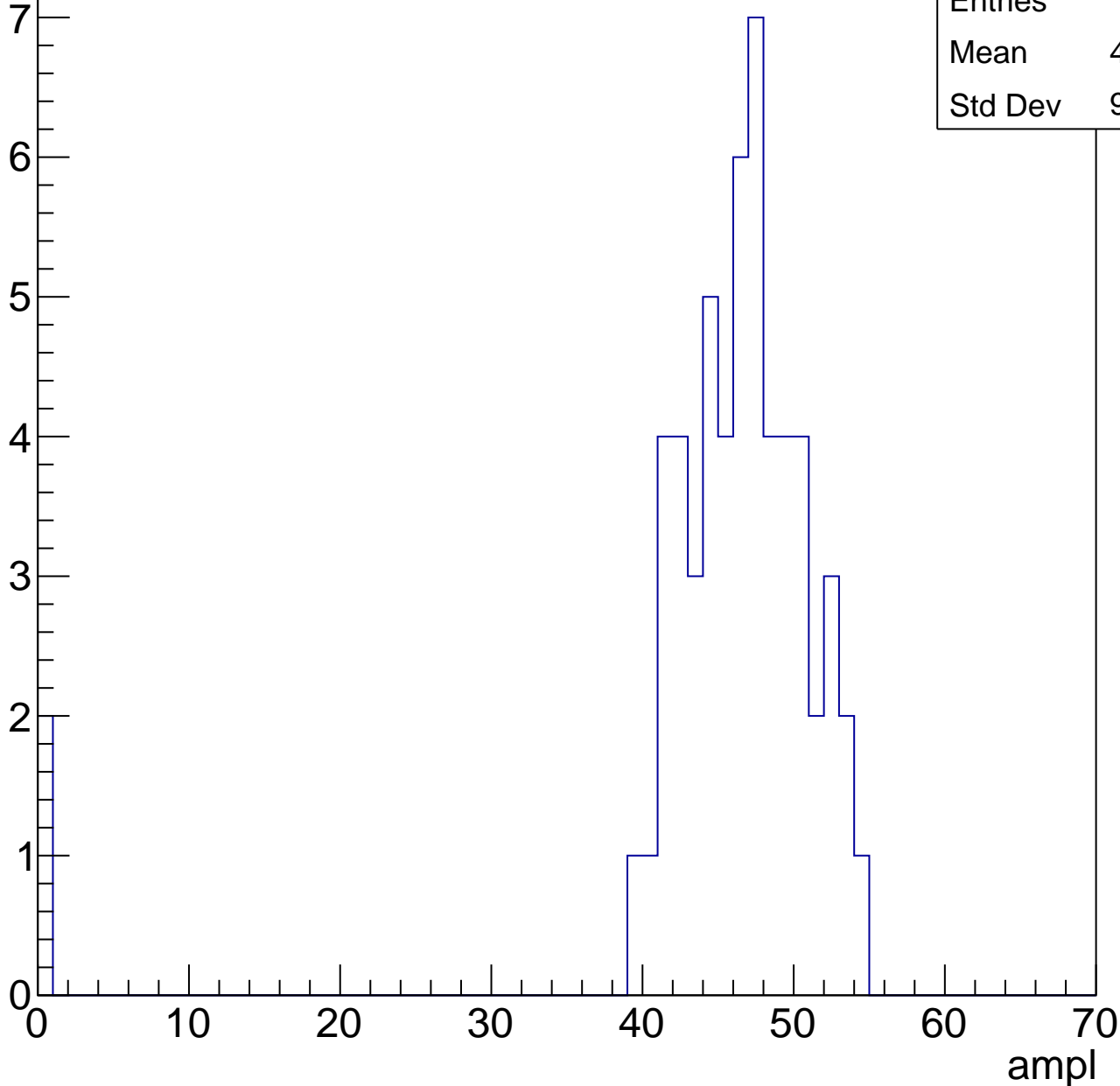


# B1L103S, U3-ch110, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	57
Mean	44.75
Std Dev	9.259

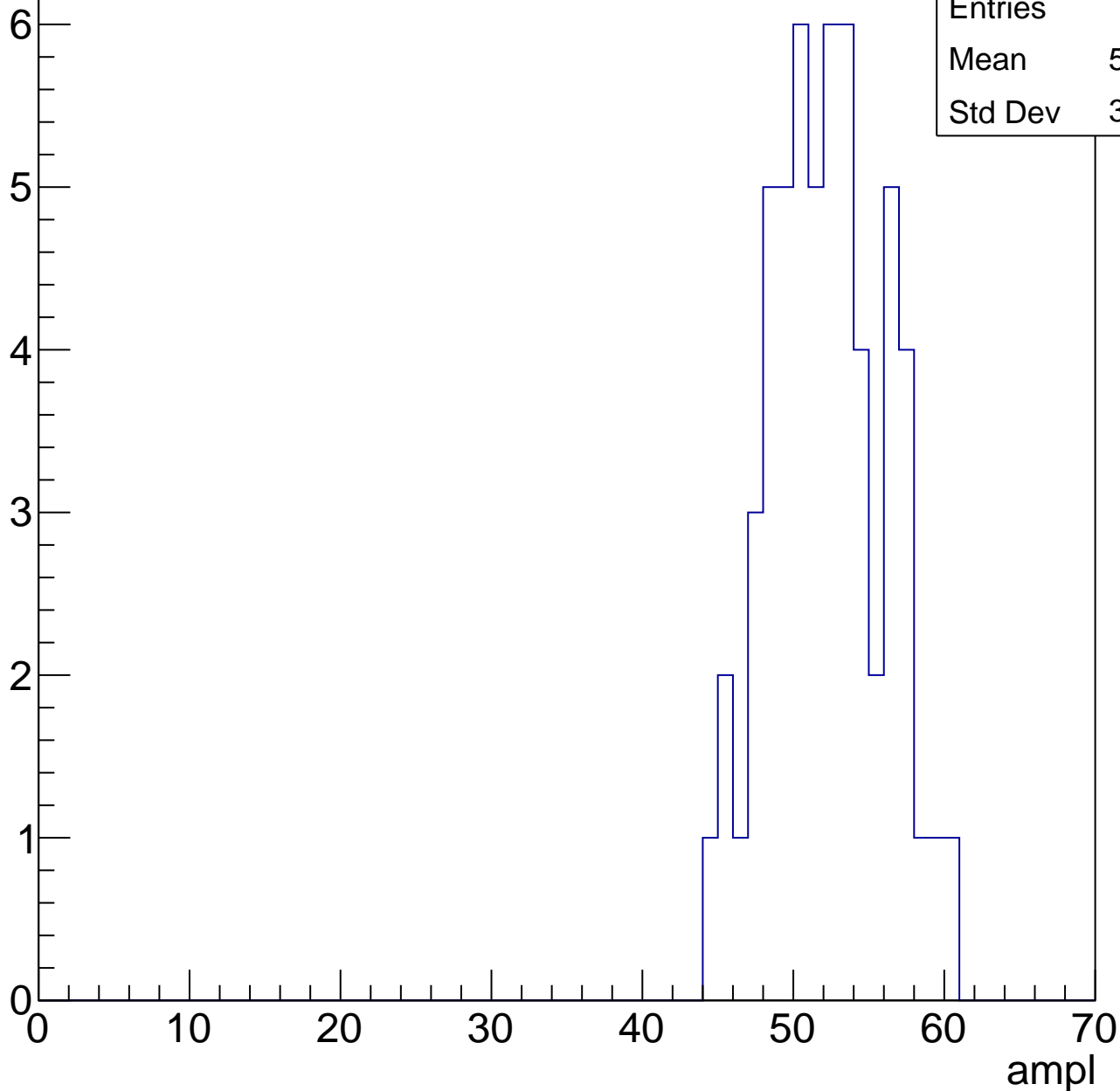


# B1L103S, U3-ch110, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	51.76
Std Dev	3.697

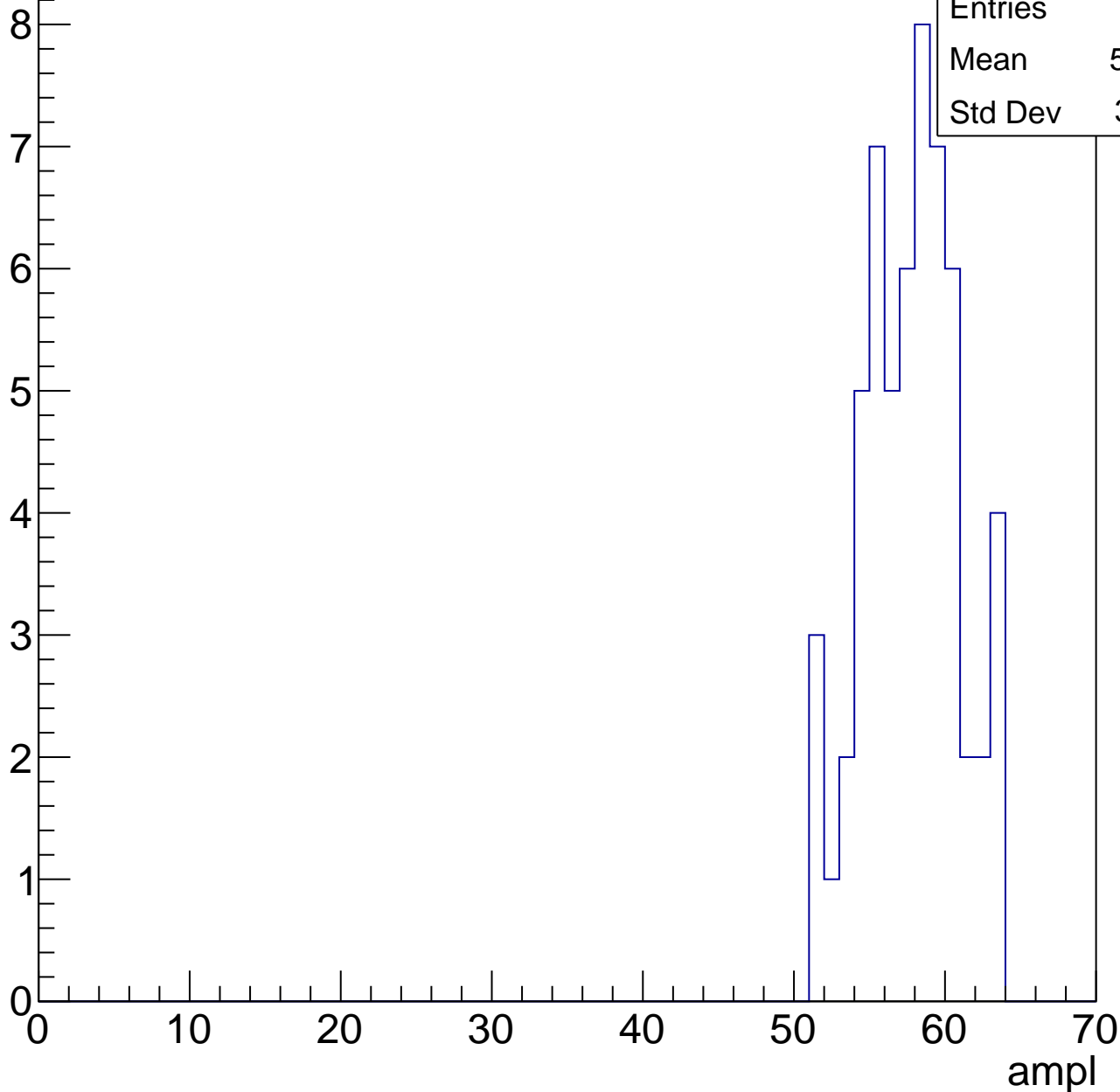


# B1L103S, U3-ch110, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	57.29
Std Dev	3.091

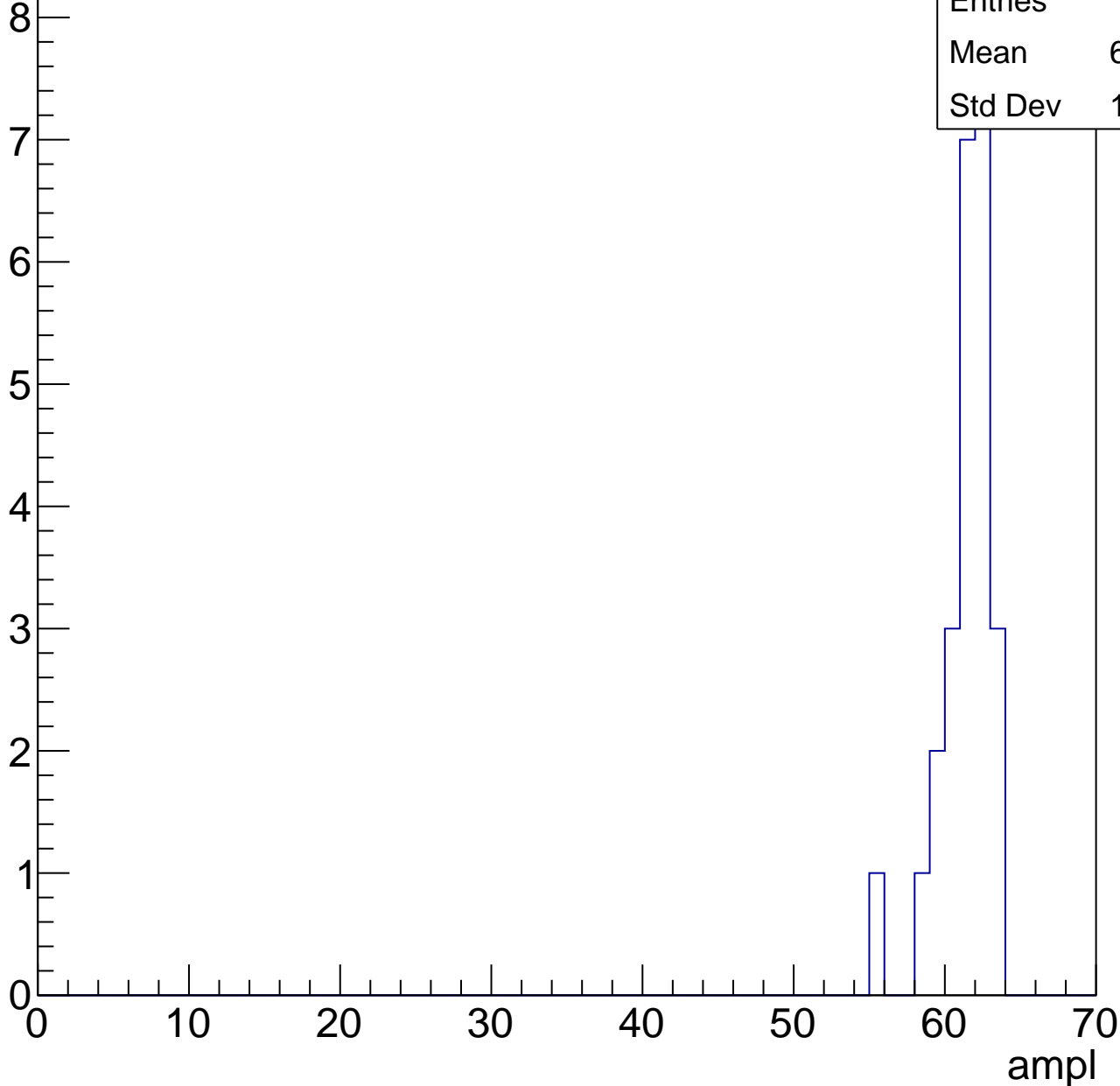


# B1L103S, U3-ch110, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	25
Mean	60.92
Std Dev	1.742

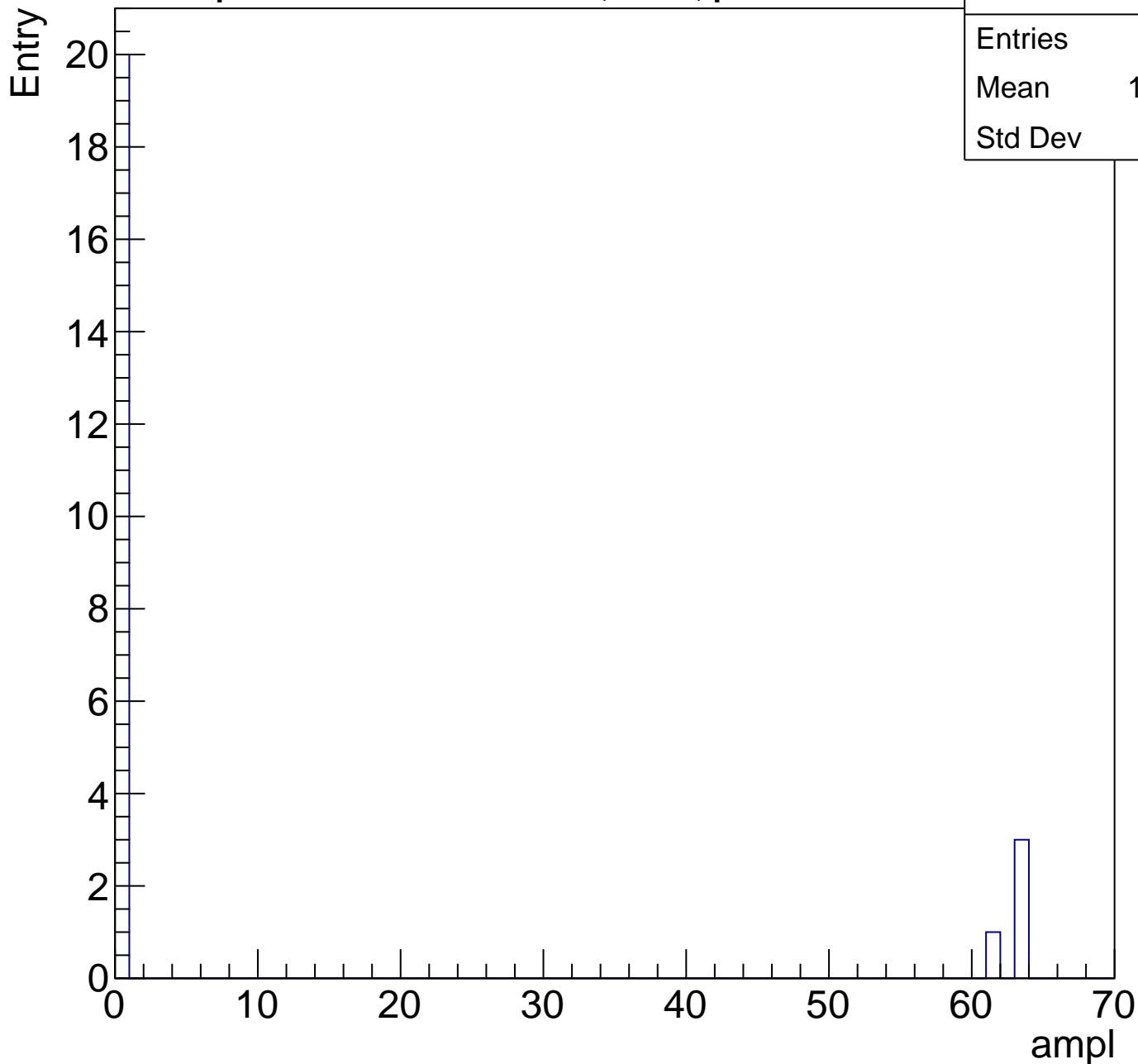




# B1L103S, U3-ch110, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	24
Mean	10.42
Std Dev	23.3



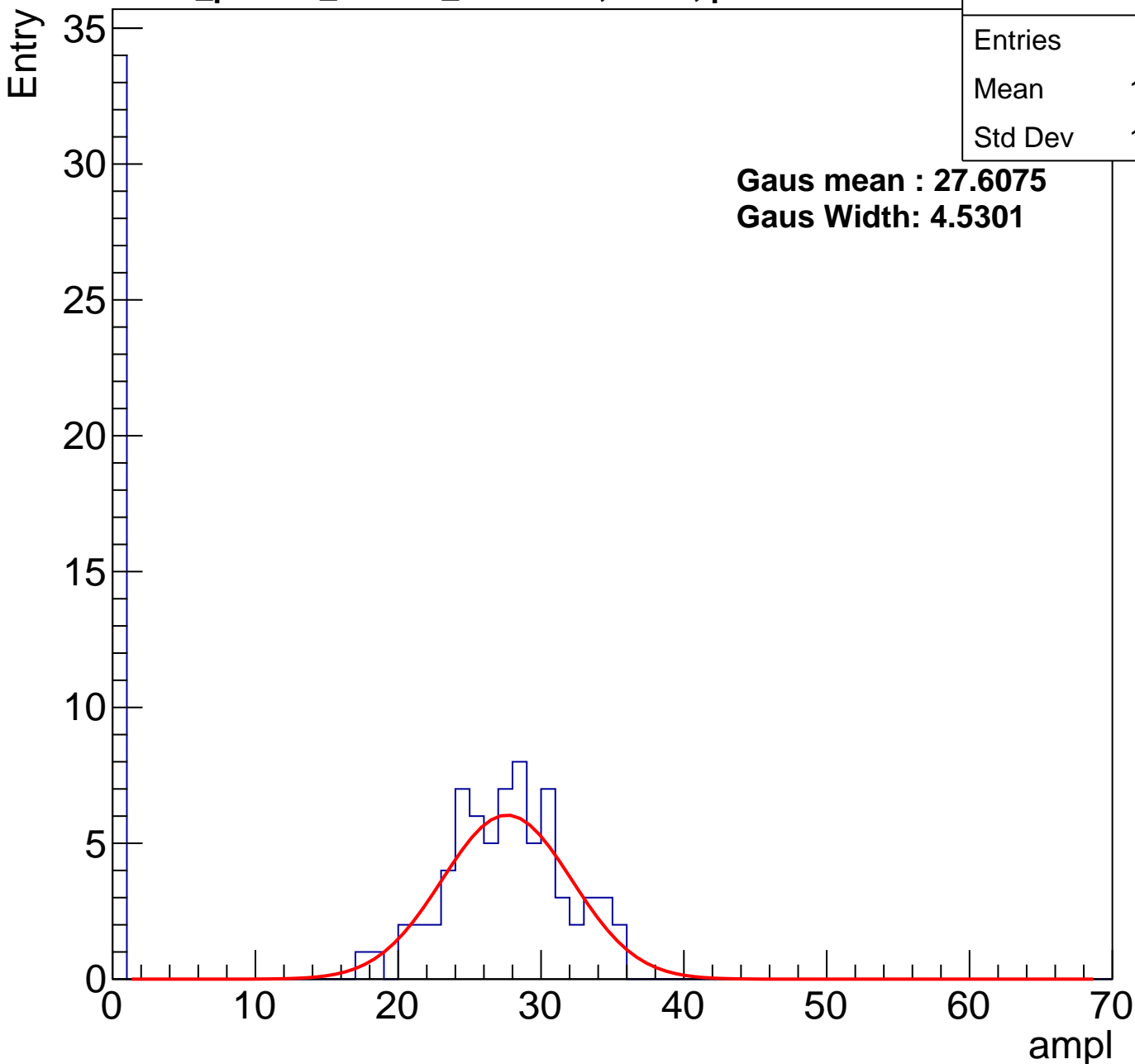
# B1L103S, U3-ch111, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	104
Mean	18.24
Std Dev	13.13

**Gaus mean : 27.6075**

**Gaus Width: 4.5301**



# B1L103S, U3-ch111, adc1

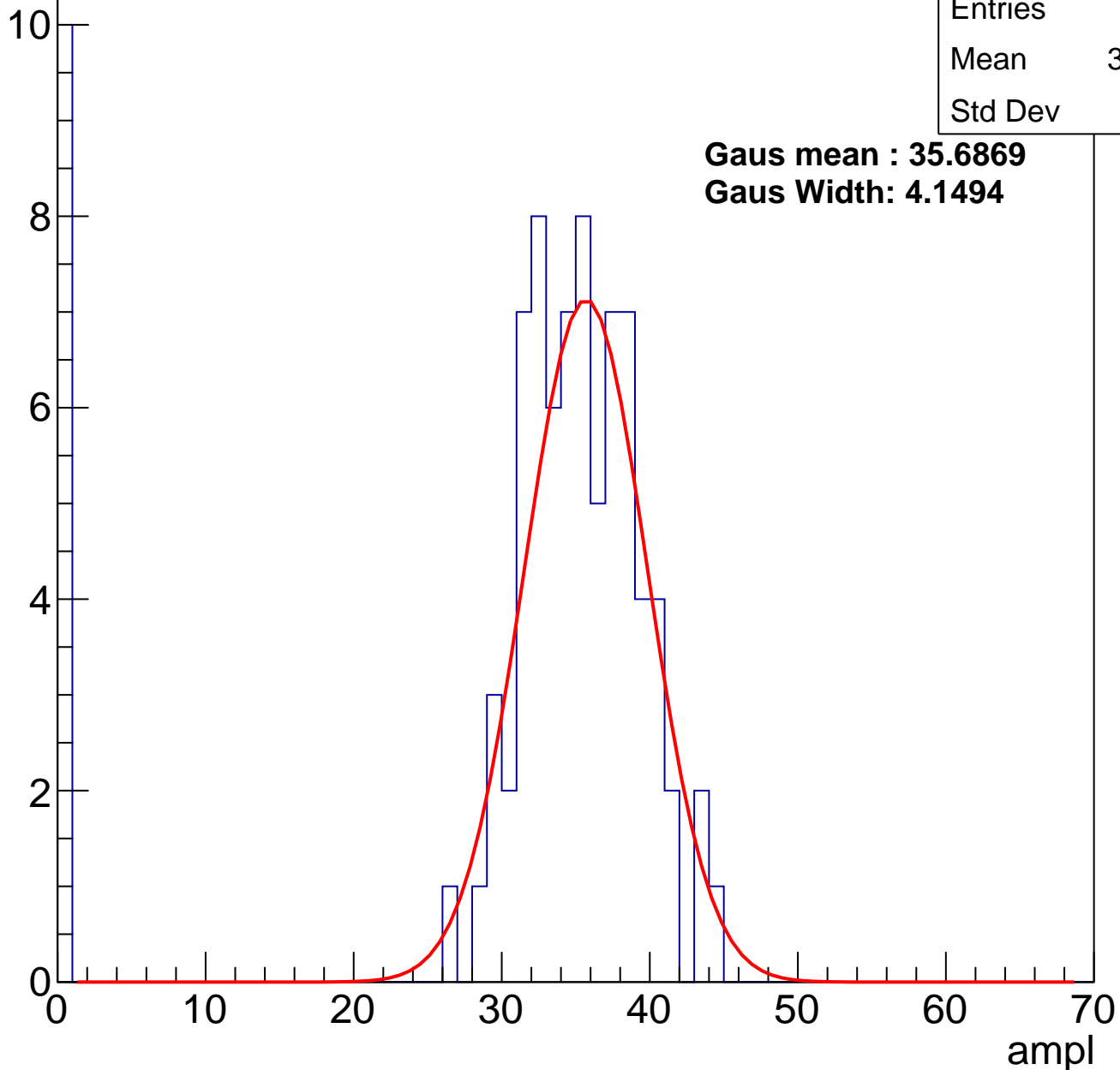
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	85
Mean	30.86
Std Dev	11.8

**Gaus mean : 35.6869**

**Gaus Width: 4.1494**

Entry



# B1L103S, U3-ch111, adc2

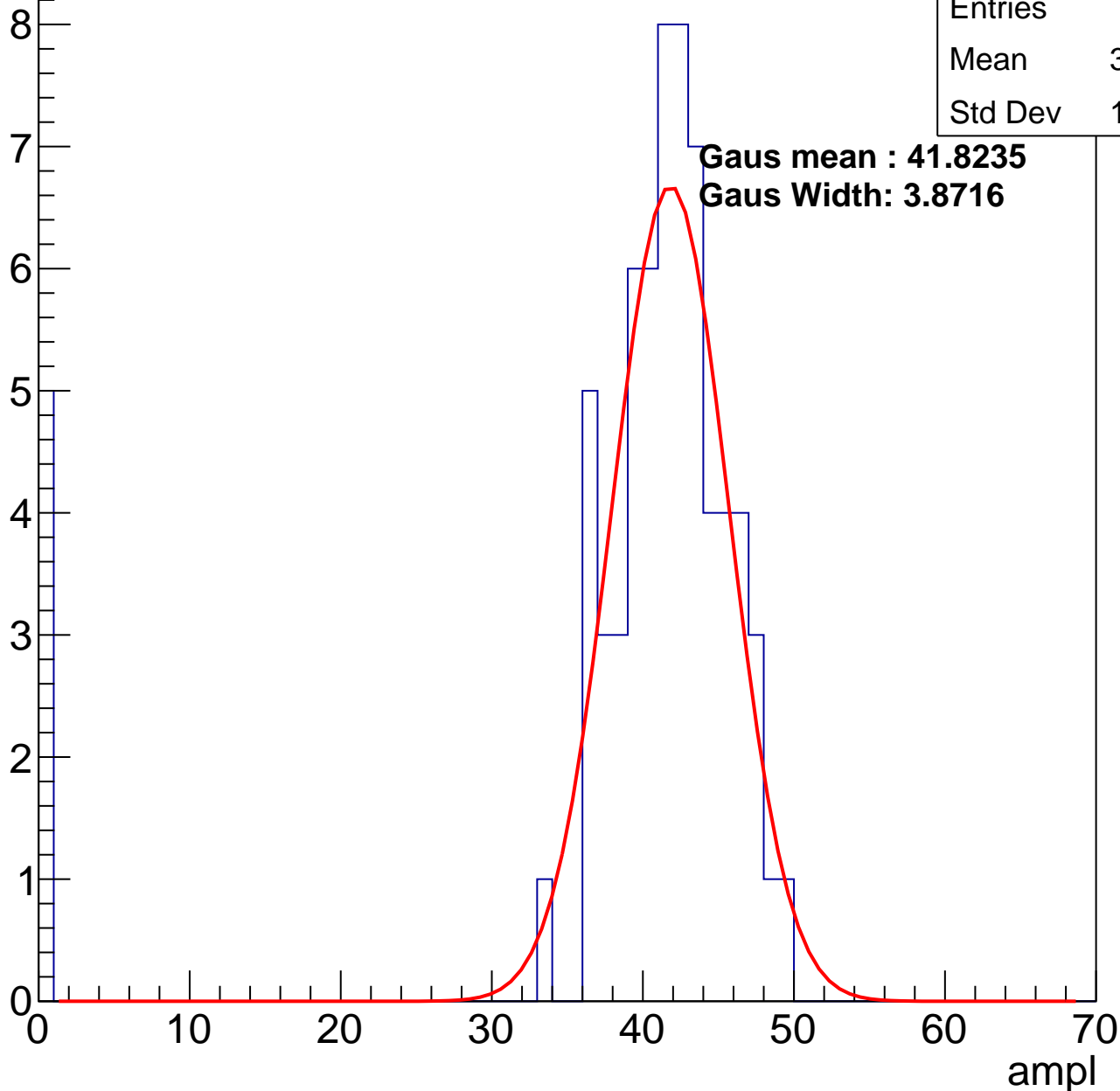
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	38.48
Std Dev	11.24

**Gaus mean : 41.8235**

**Gaus Width: 3.8716**

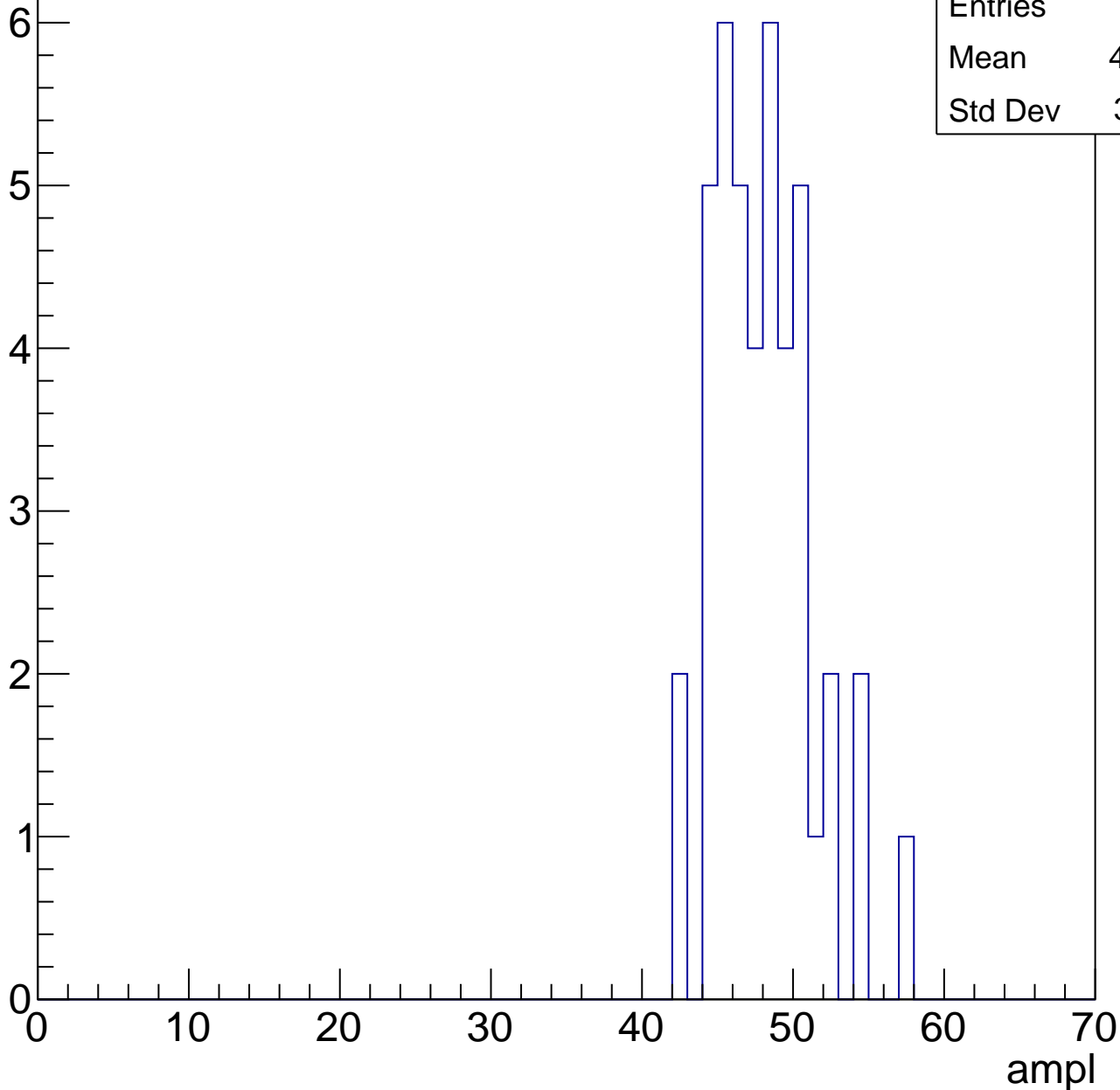


# B1L103S, U3-ch111, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	43
Mean	47.58
Std Dev	3.201



# B1L103S, U3-ch111, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

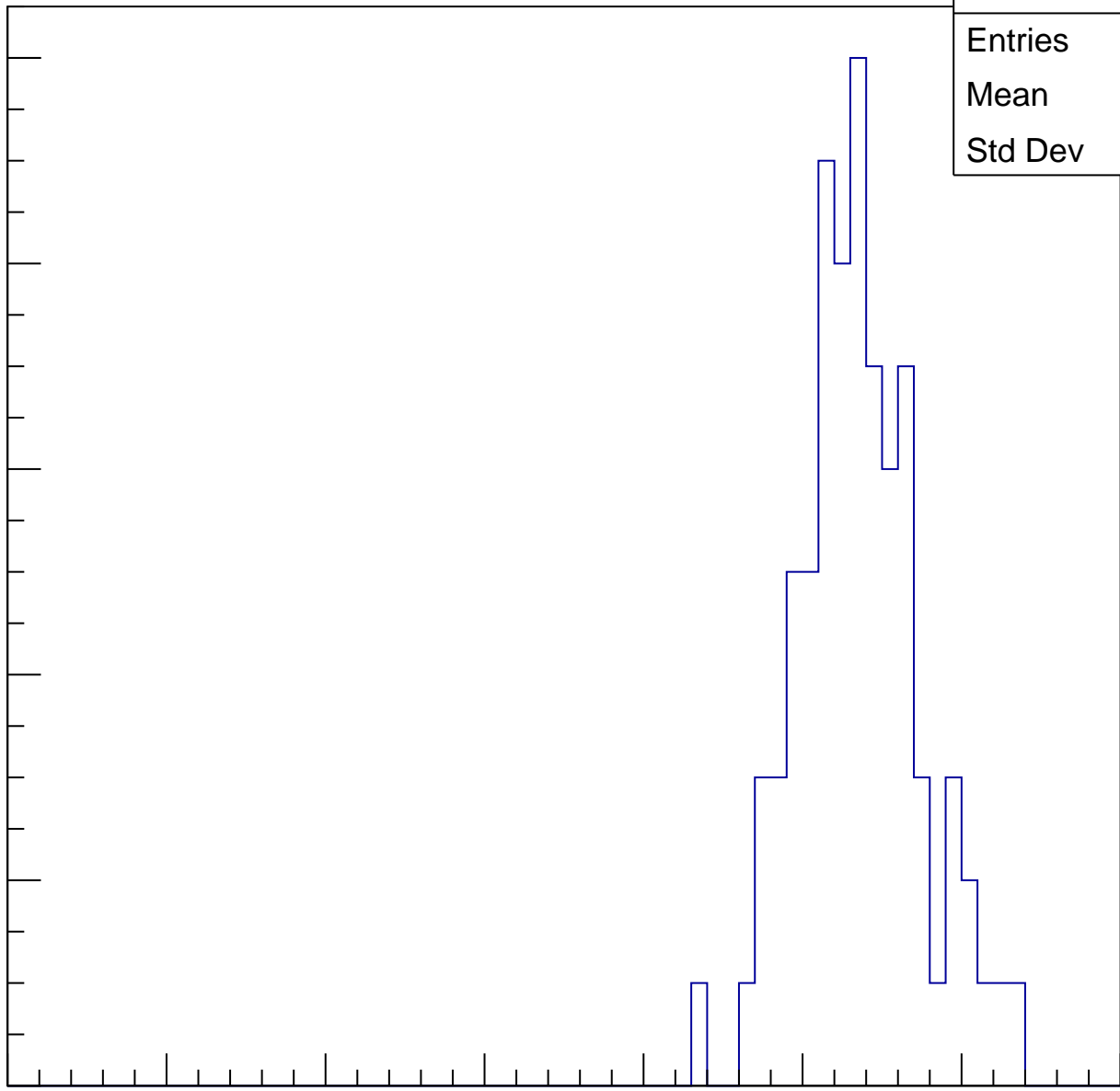
Entries	77
Mean	53.06
Std Dev	3.812

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

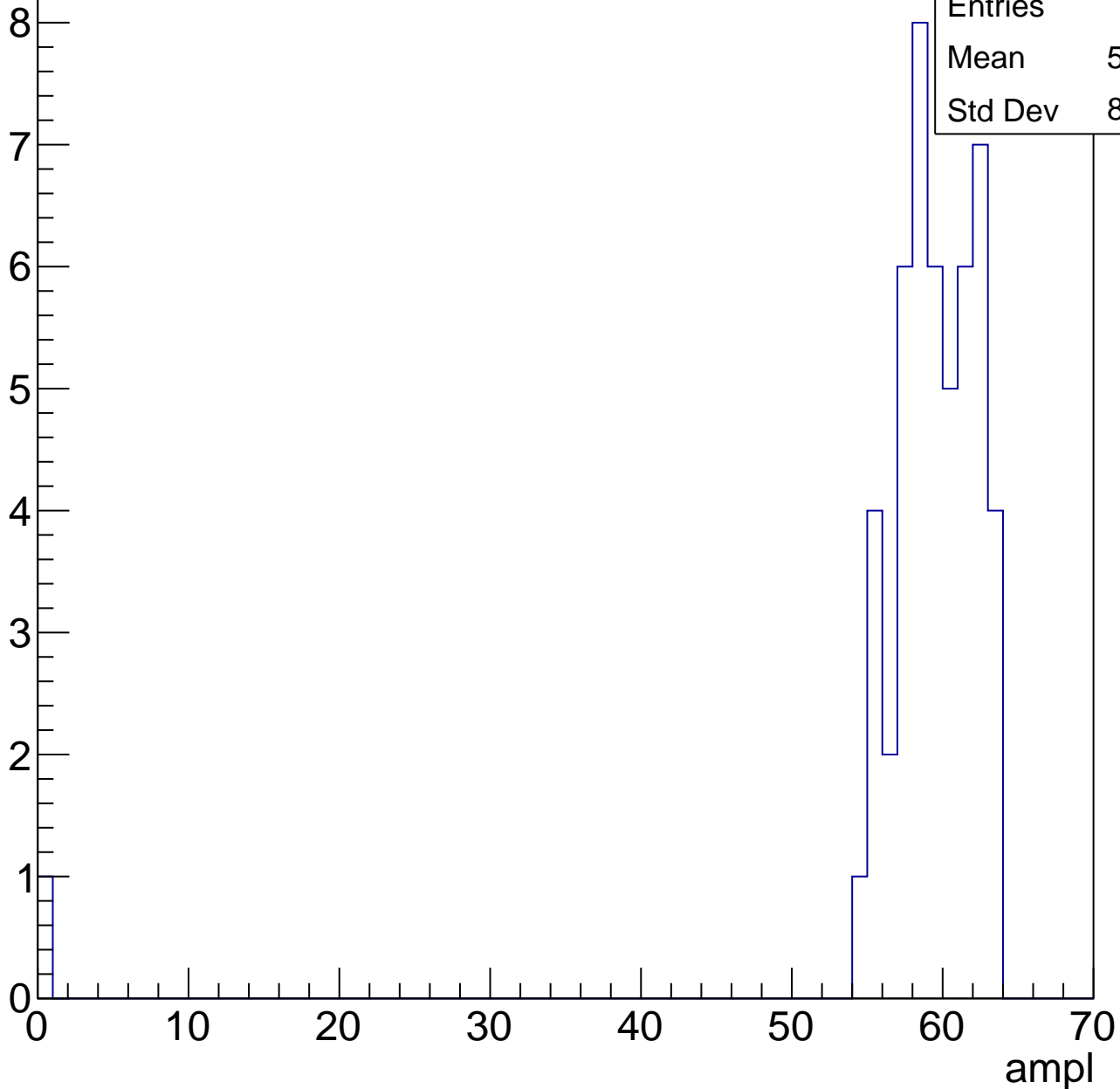


# B1L103S, U3-ch111, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

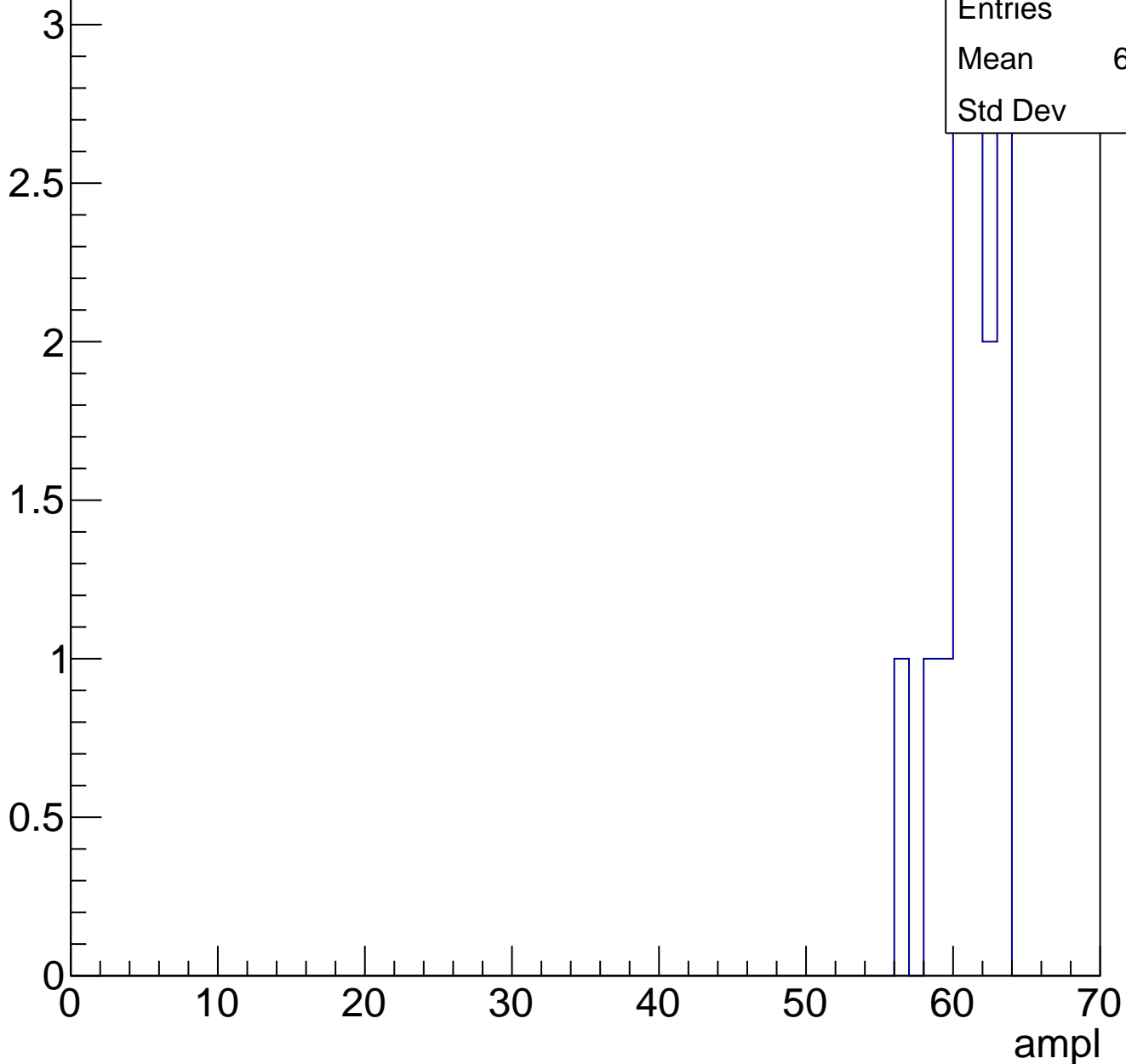
Entries	50
Mean	57.96
Std Dev	8.628



# B1L103S, U3-ch111, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U3-ch111, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	6
Std Dev	18.49

Entry



# B1L103S, U3-ch112, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	67
Mean	19.85
Std Dev	11.49

**Gaus mean : 26.0105**

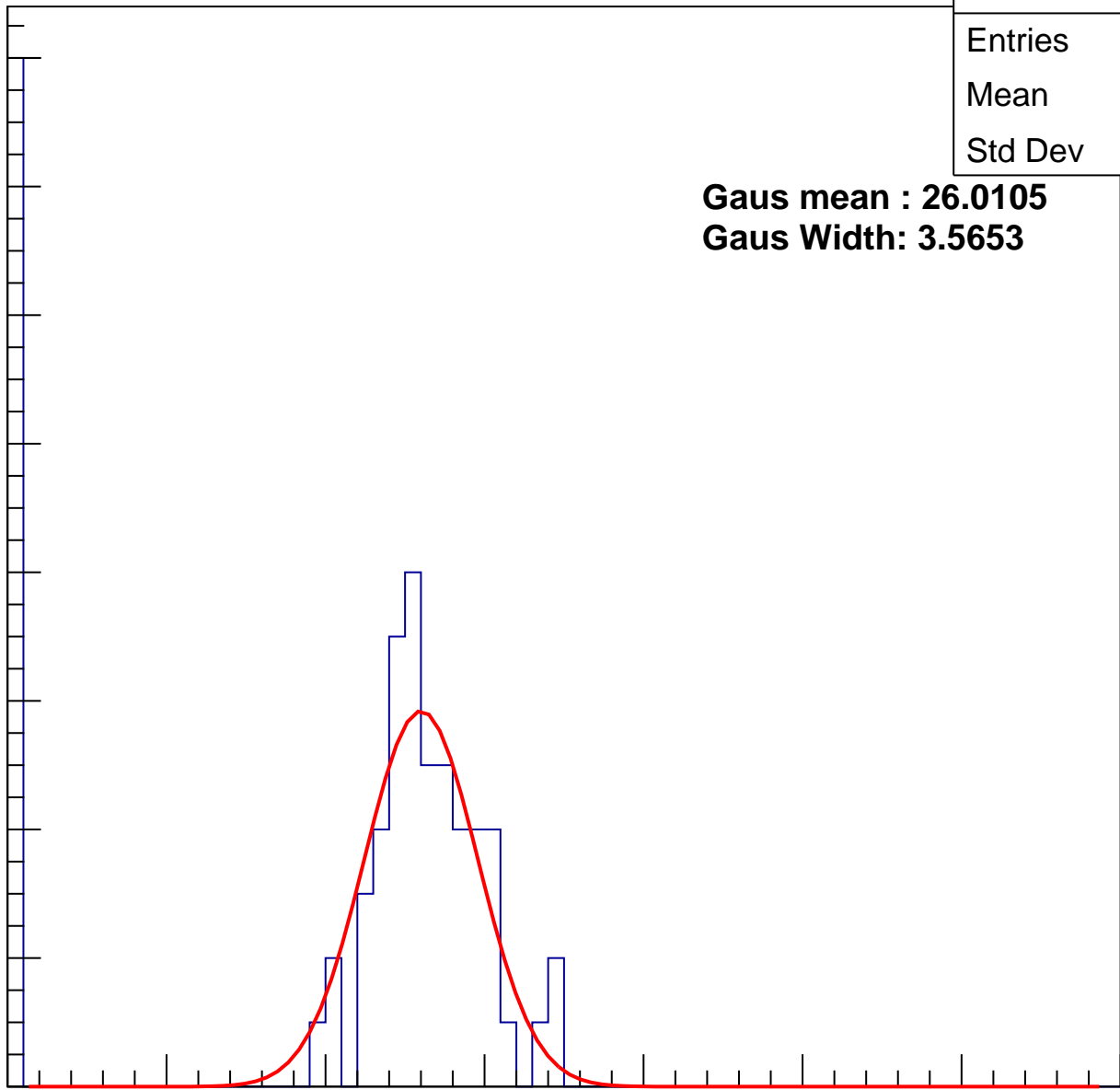
**Gaus Width: 3.5653**

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch112, adc1

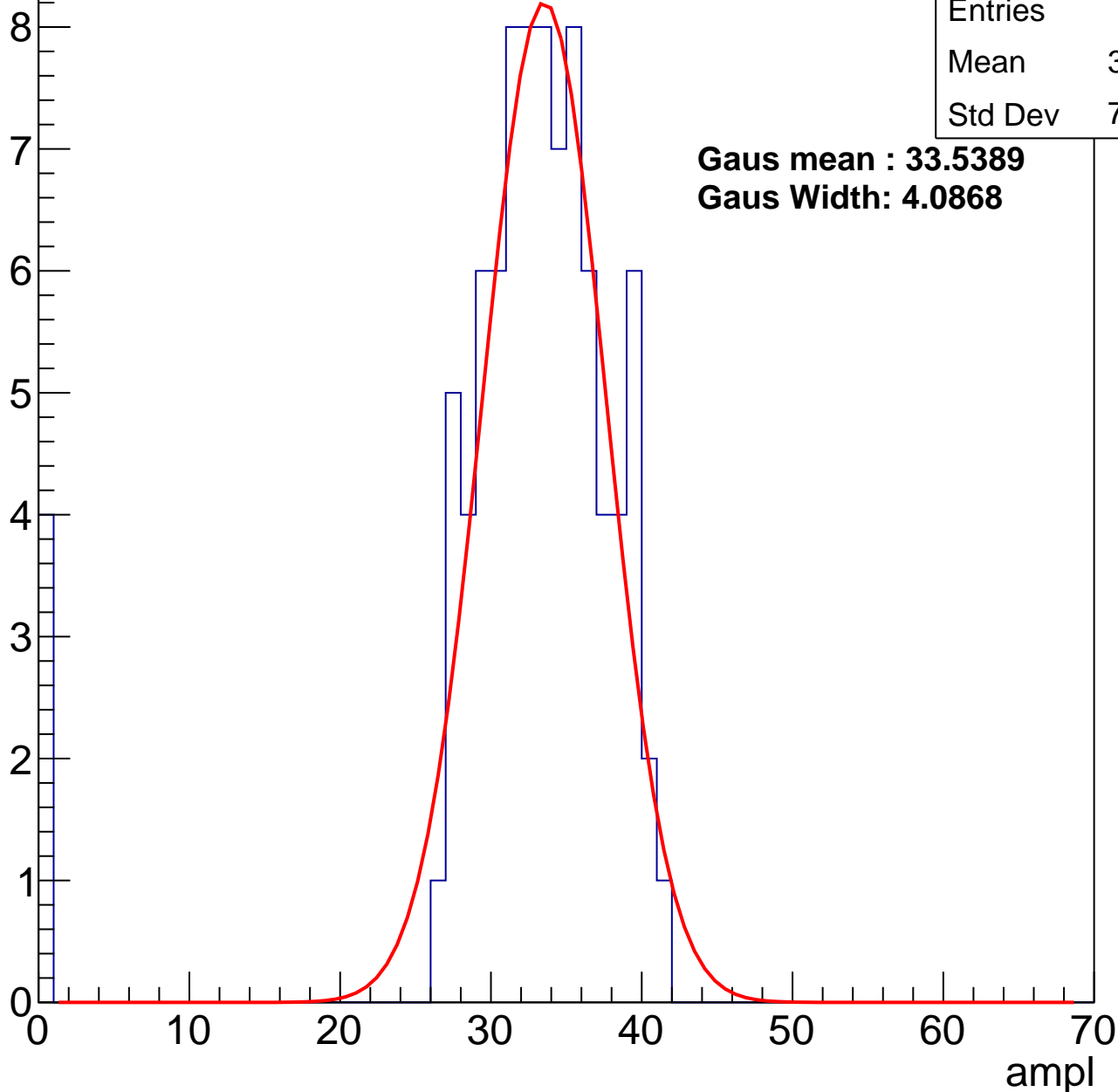
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	88
Mean	31.64
Std Dev	7.794

**Gaus mean : 33.5389**

**Gaus Width: 4.0868**



# B1L103S, U3-ch112, adc2

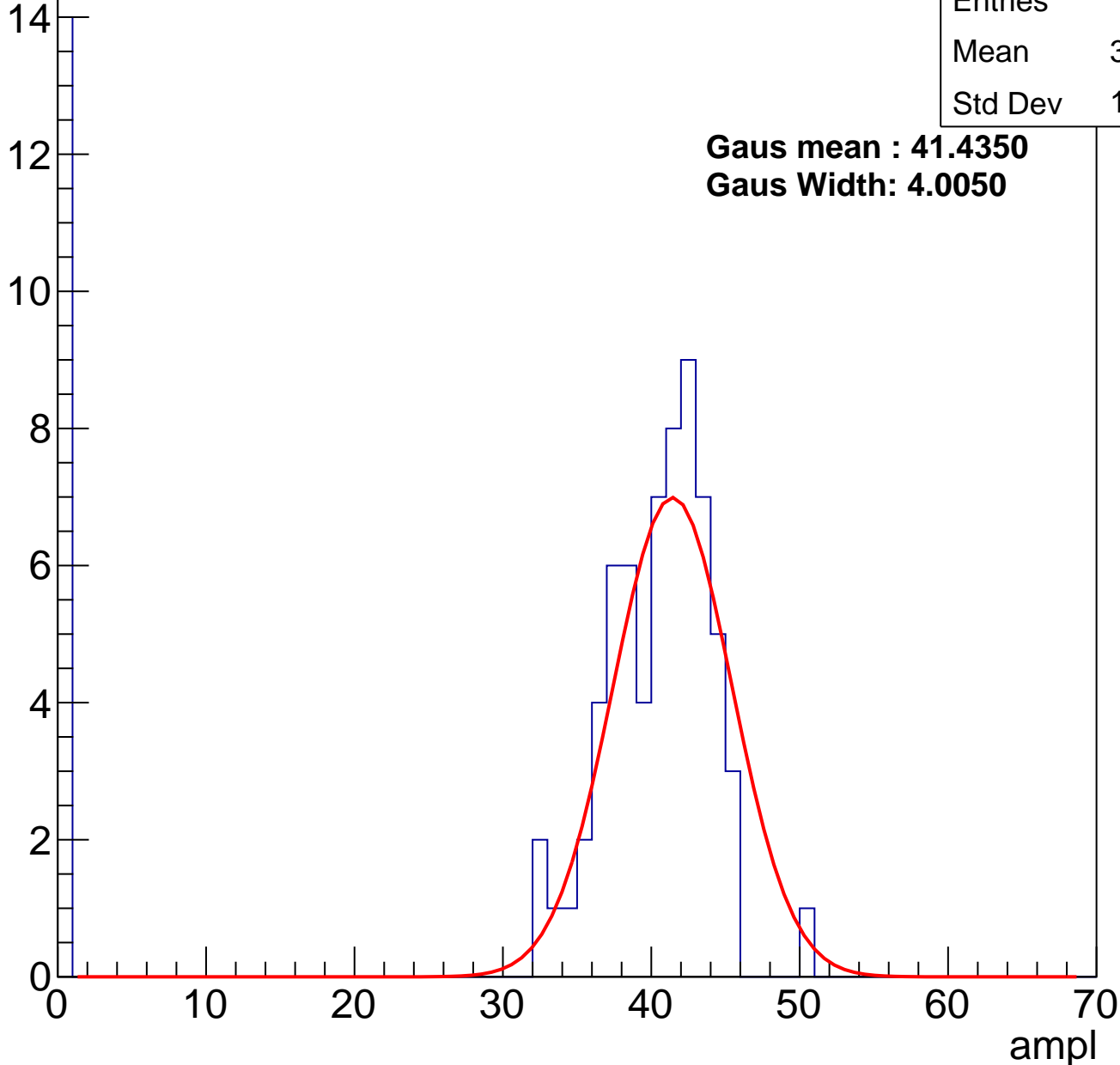
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	80
Mean	33.04
Std Dev	15.53

**Gaus mean : 41.4350**

**Gaus Width: 4.0050**

Entry

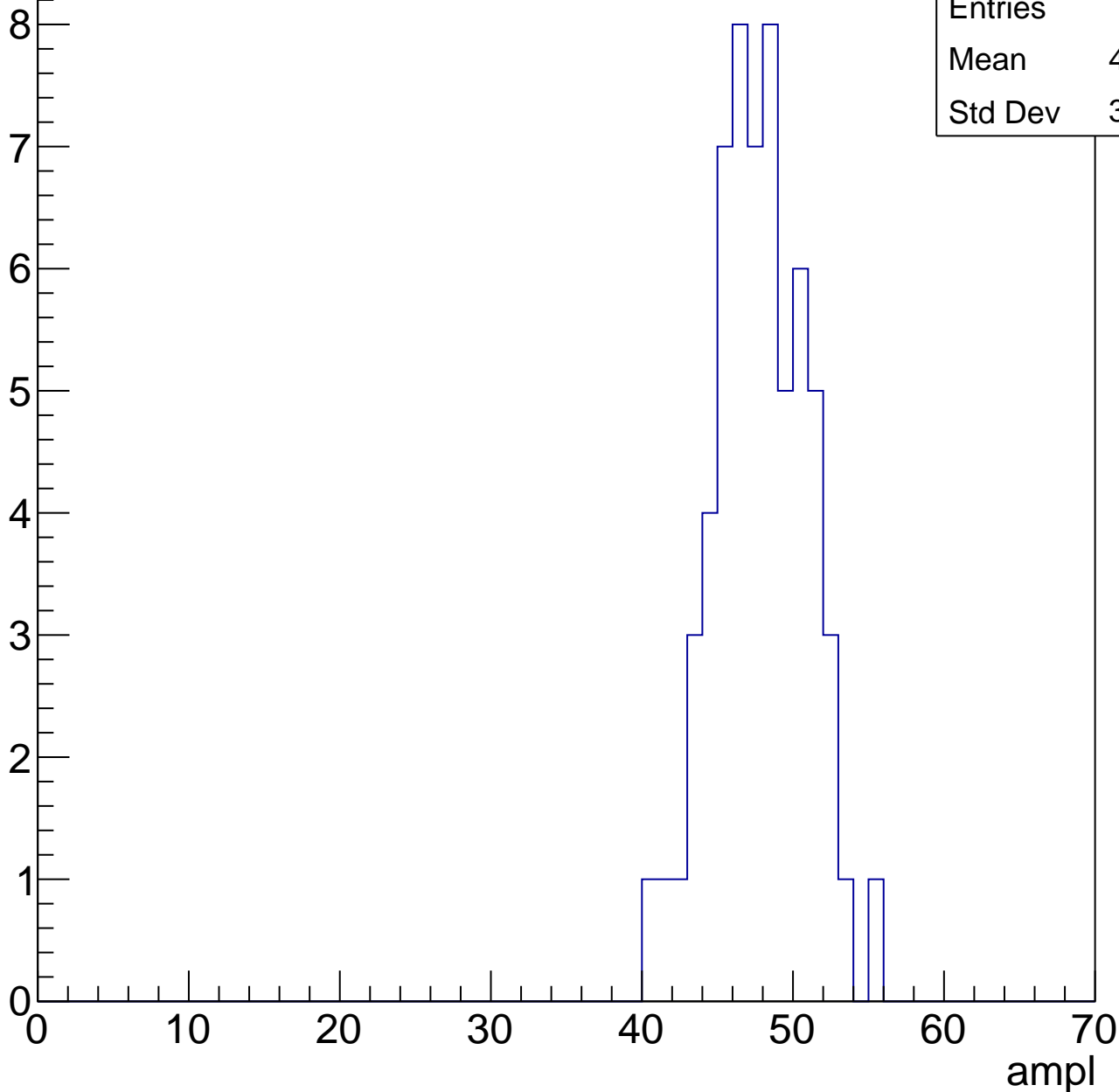


# B1L103S, U3-ch112, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	61
Mean	47.34
Std Dev	3.029

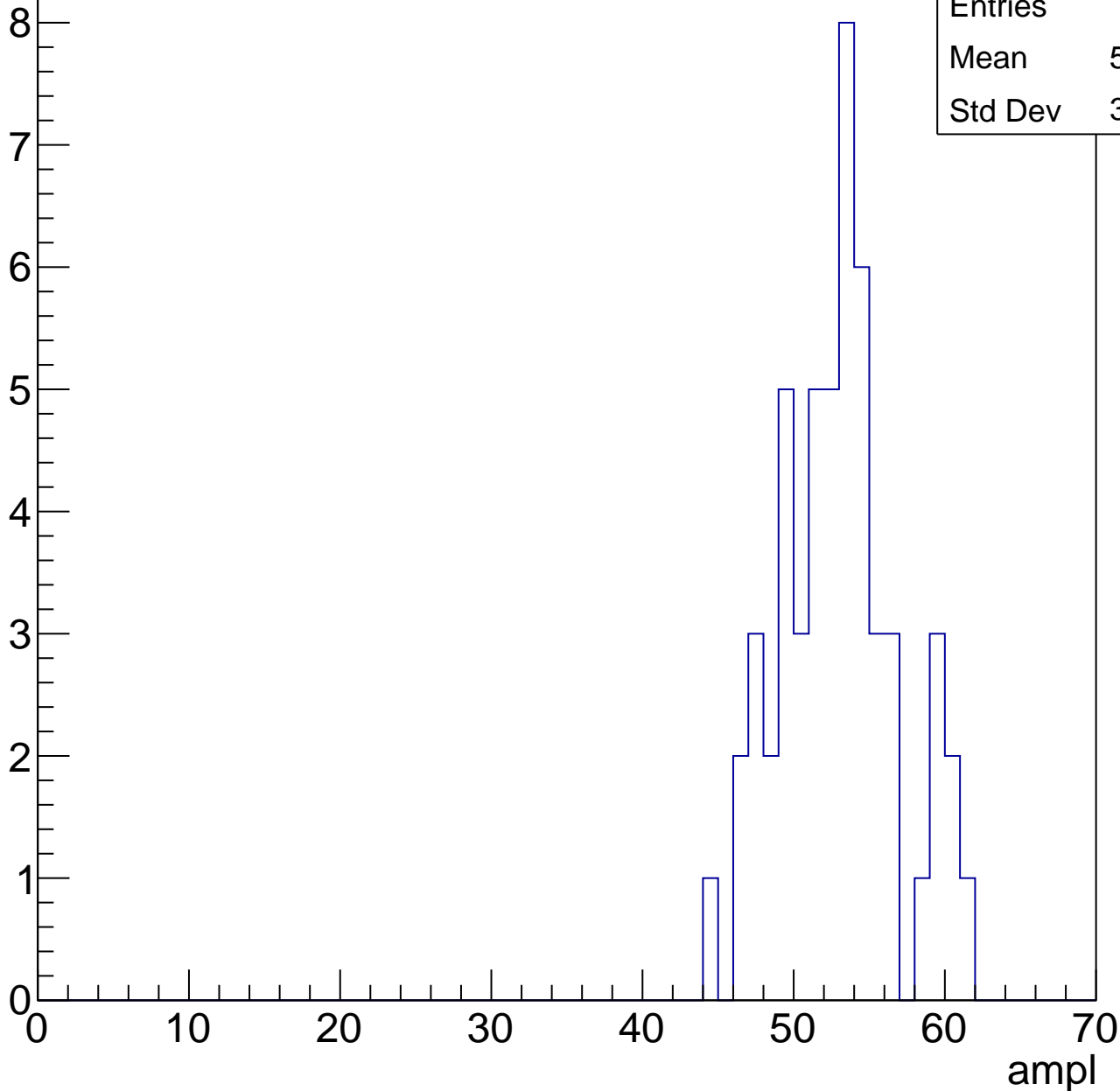


# B1L103S, U3-ch112, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	53
Mean	52.45
Std Dev	3.868

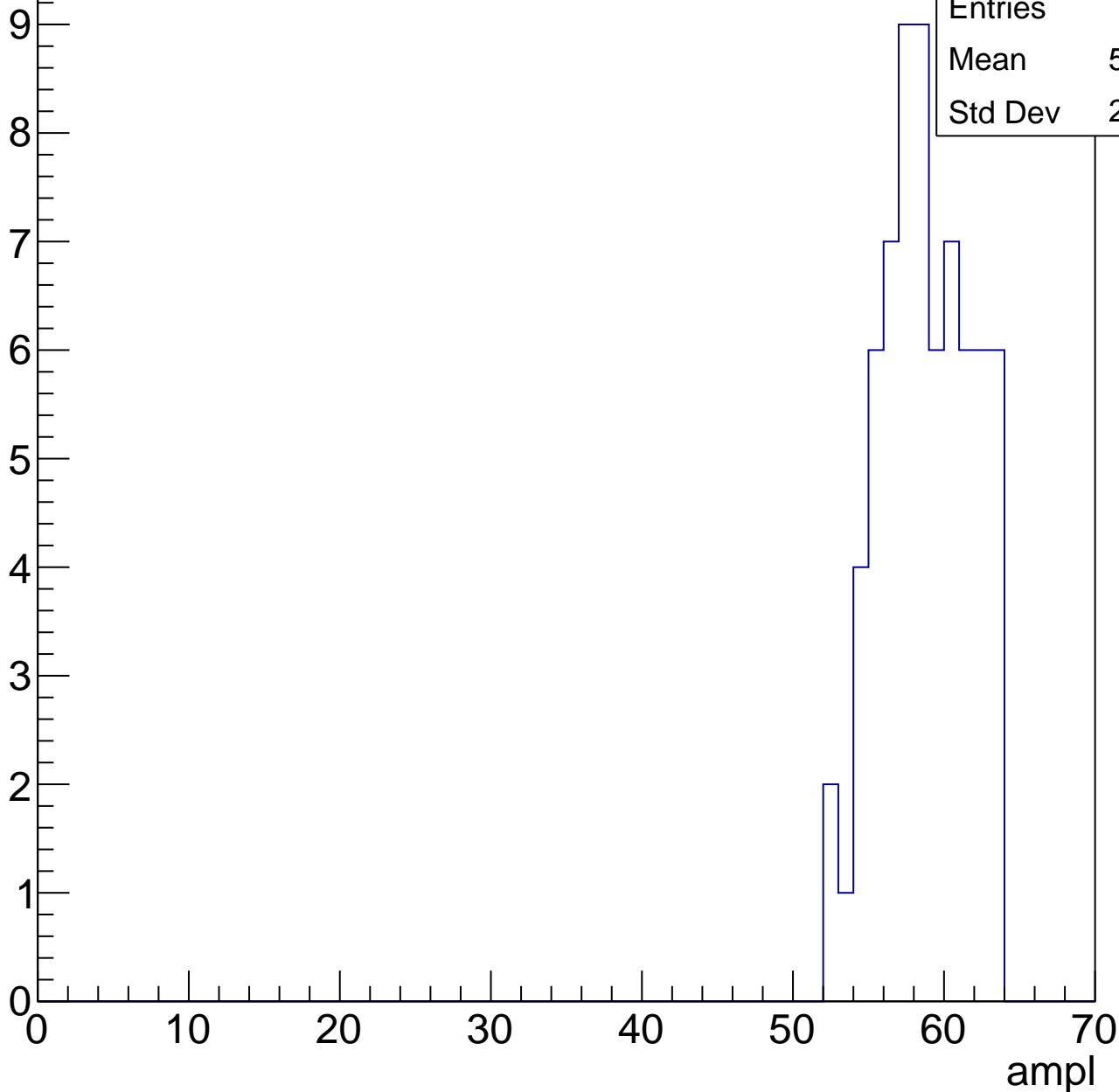


# B1L103S, U3-ch112, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

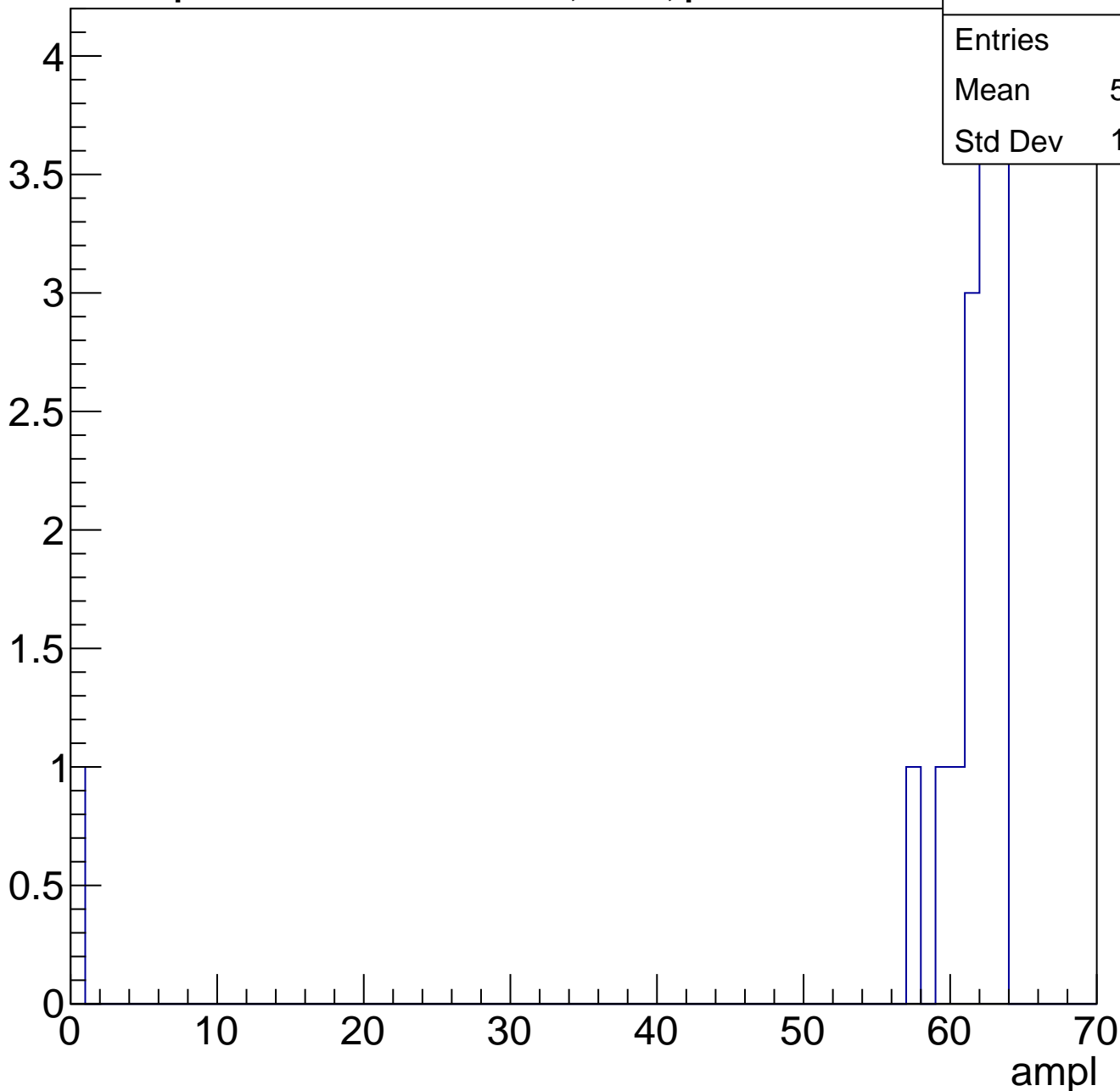
Entries	69
Mean	58.26
Std Dev	2.903



# B1L103S, U3-ch112, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U3-ch112, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U3-ch113, adc0

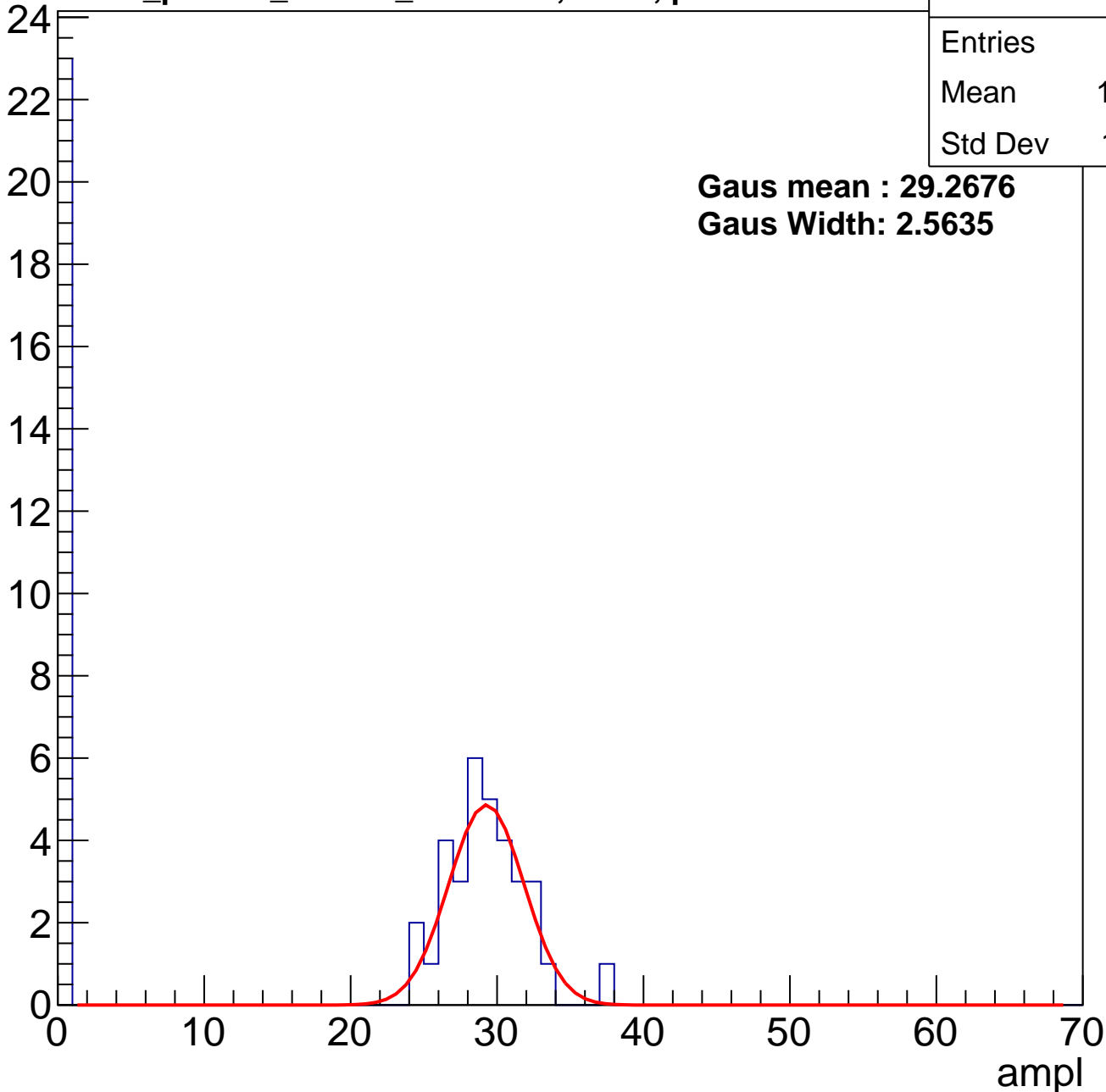
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	56
Mean	16.96
Std Dev	14.31

**Gaus mean : 29.2676**

**Gaus Width: 2.5635**

Entry



# B1L103S, U3-ch113, adc1

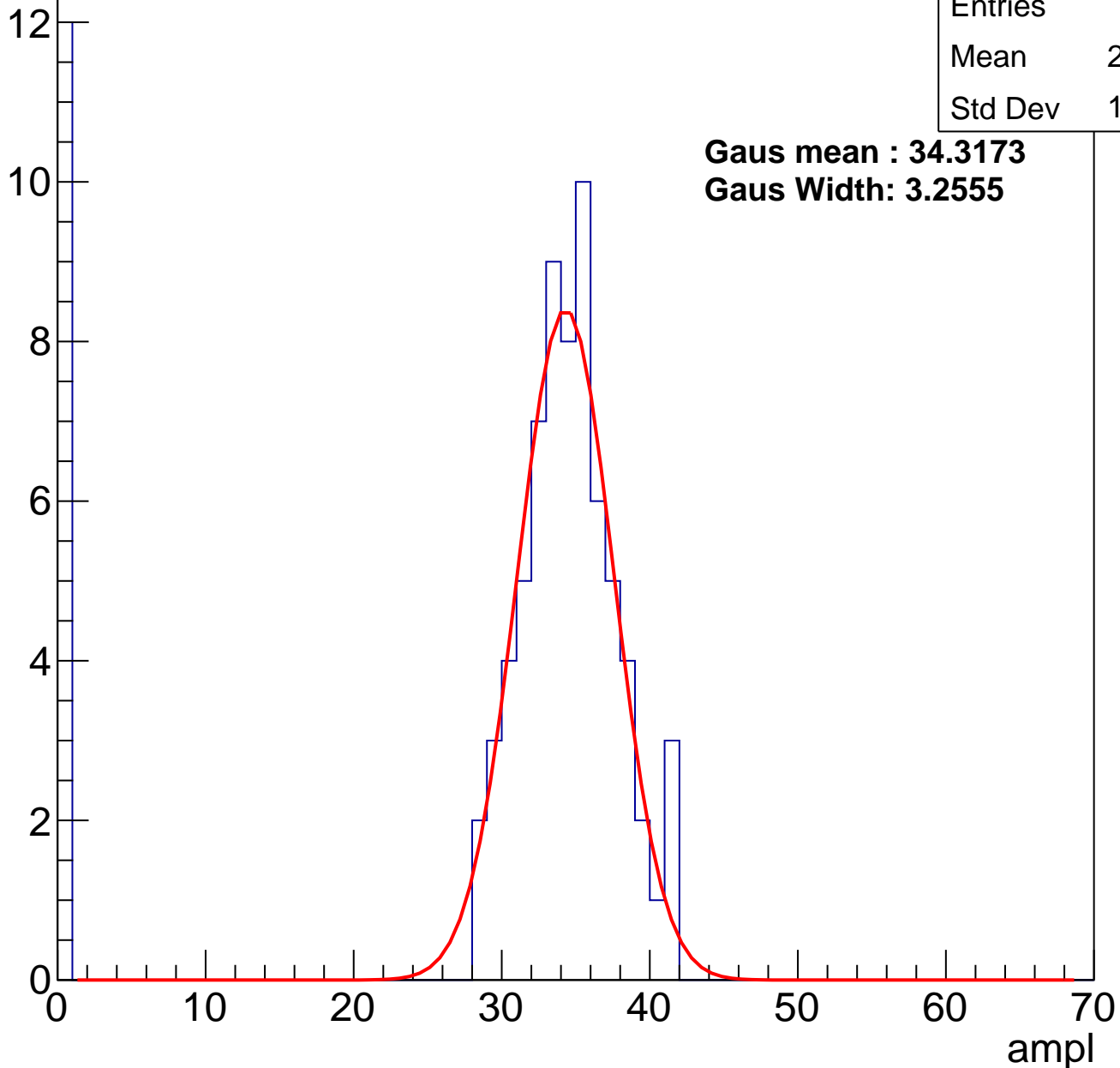
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	81
Mean	29.07
Std Dev	12.46

**Gaus mean : 34.3173**

**Gaus Width: 3.2555**

Entry



# B1L103S, U3-ch113, adc2

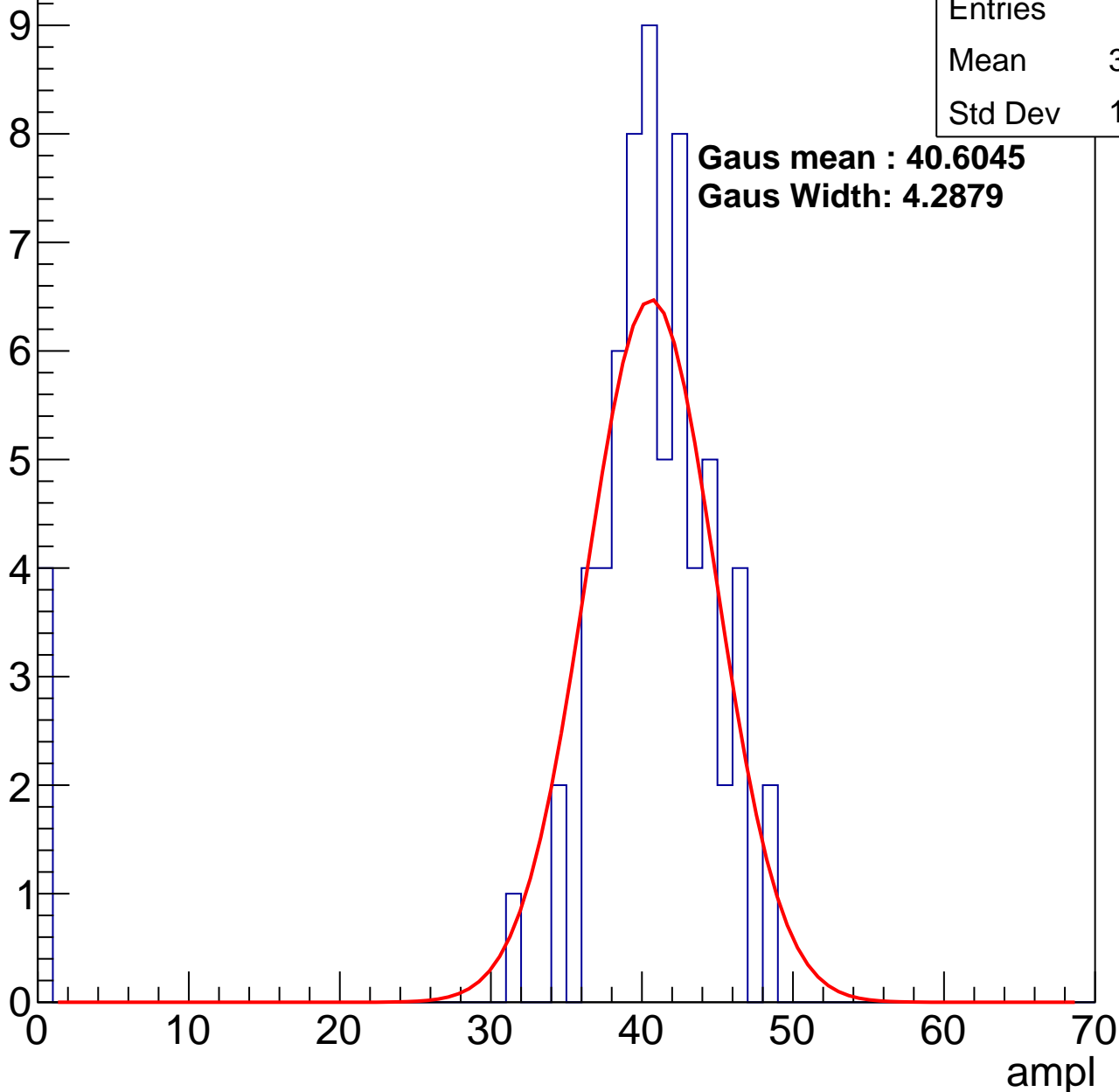
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	38.15
Std Dev	10.09

**Gaus mean : 40.6045**

**Gaus Width: 4.2879**

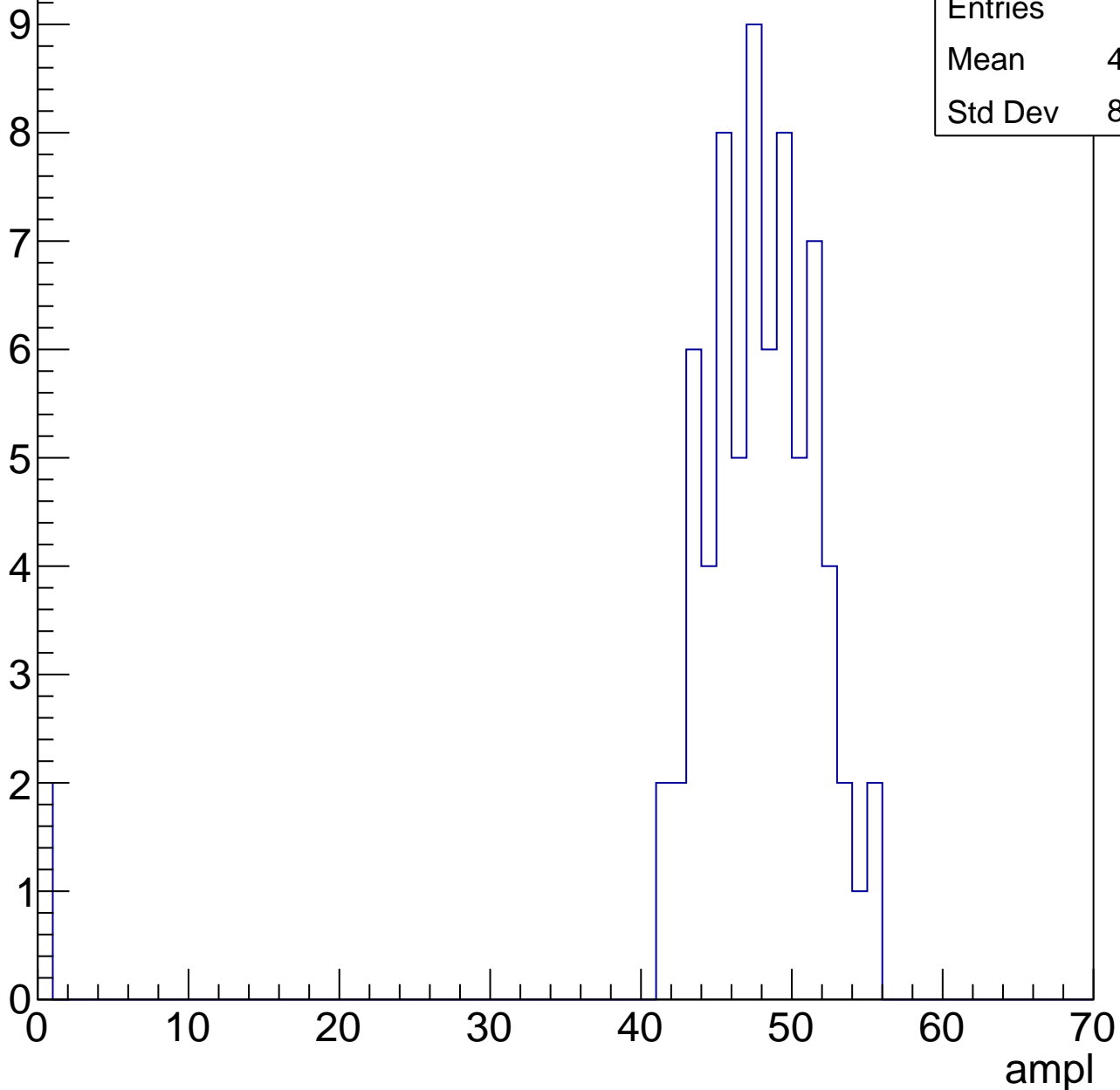


# B1L103S, U3-ch113, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	46.27
Std Dev	8.452

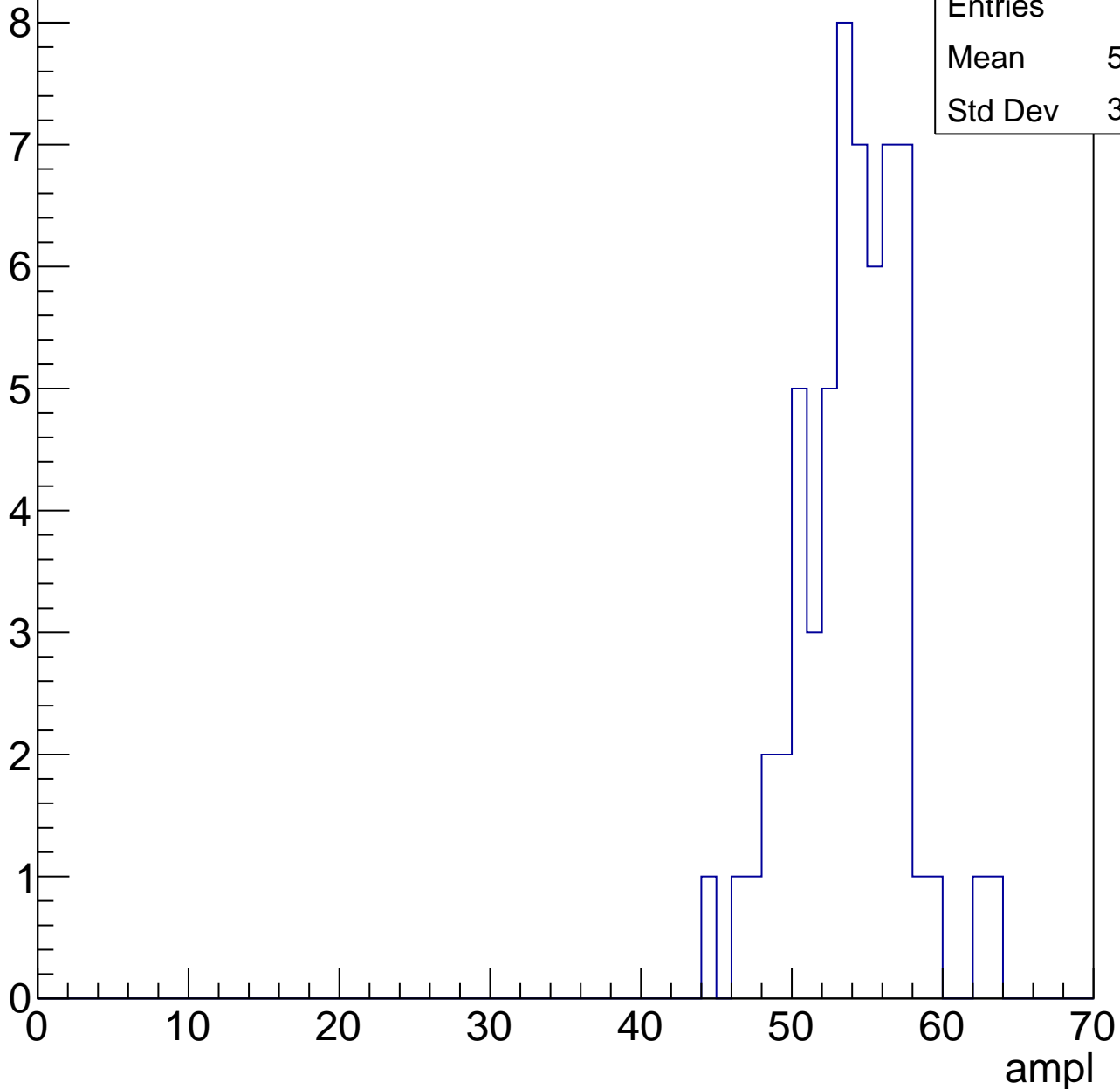


# B1L103S, U3-ch113, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	53.54
Std Dev	3.543

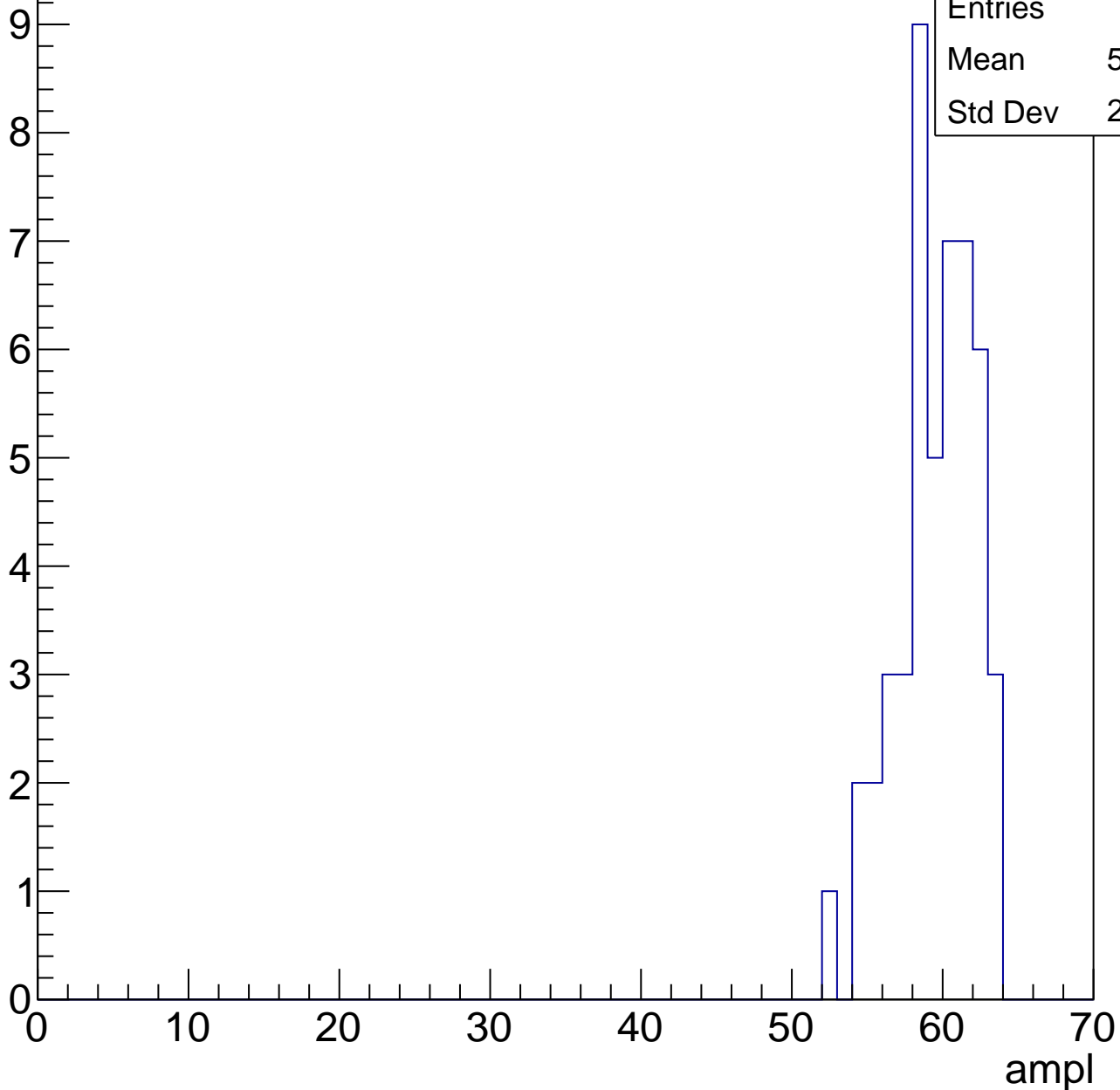


# B1L103S, U3-ch113, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	48
Mean	59.04
Std Dev	2.565

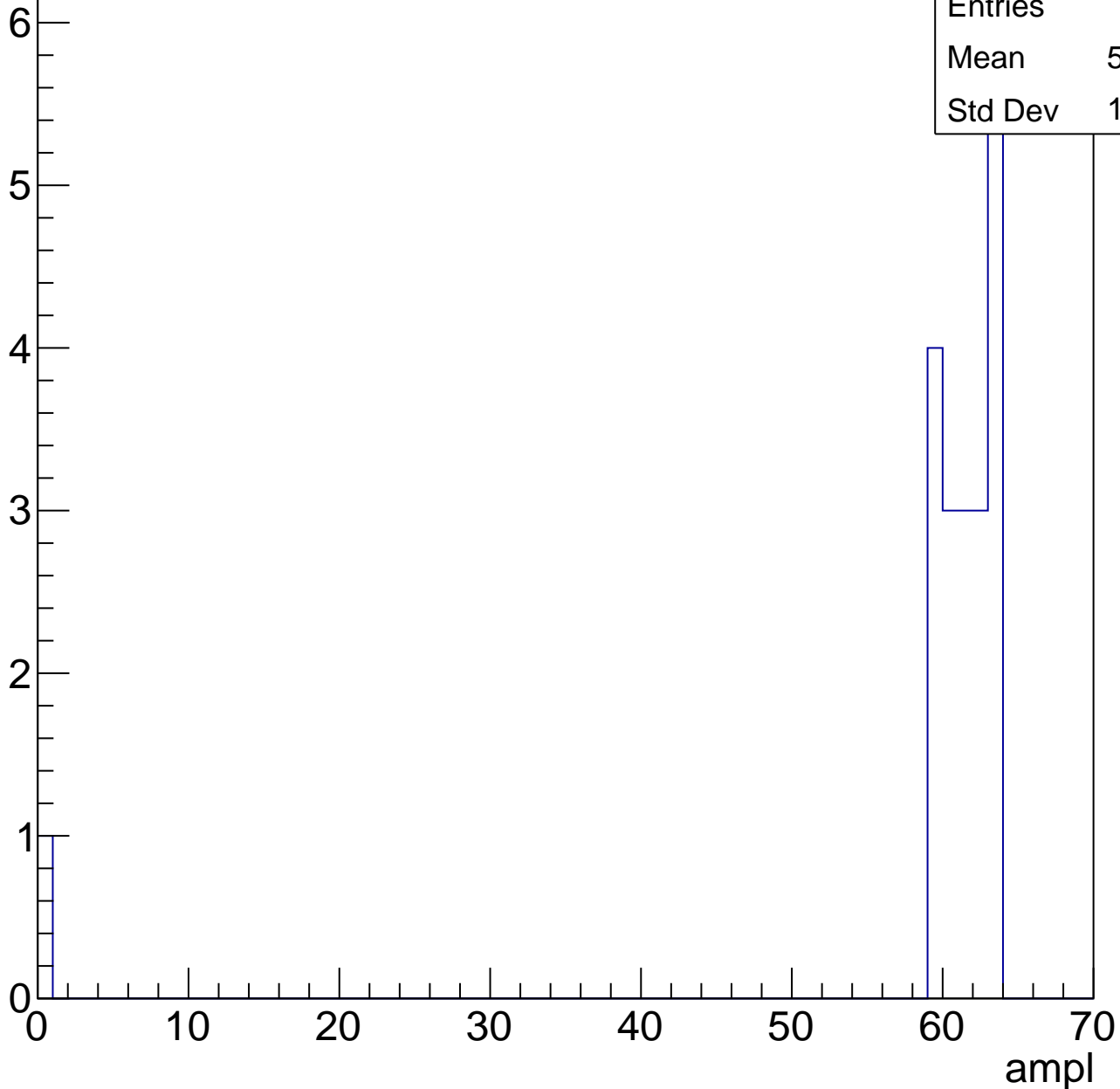


# B1L103S, U3-ch113, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	20
Mean	58.15
Std Dev	13.42





# B1L103S, U3-ch113, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U3-ch114, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	78
Mean	24.26
Std Dev	10.53

**Gaus mean : 27.8461**

**Gaus Width: 4.3303**

Entry

10

8

6

4

2

0

0

10

20

30

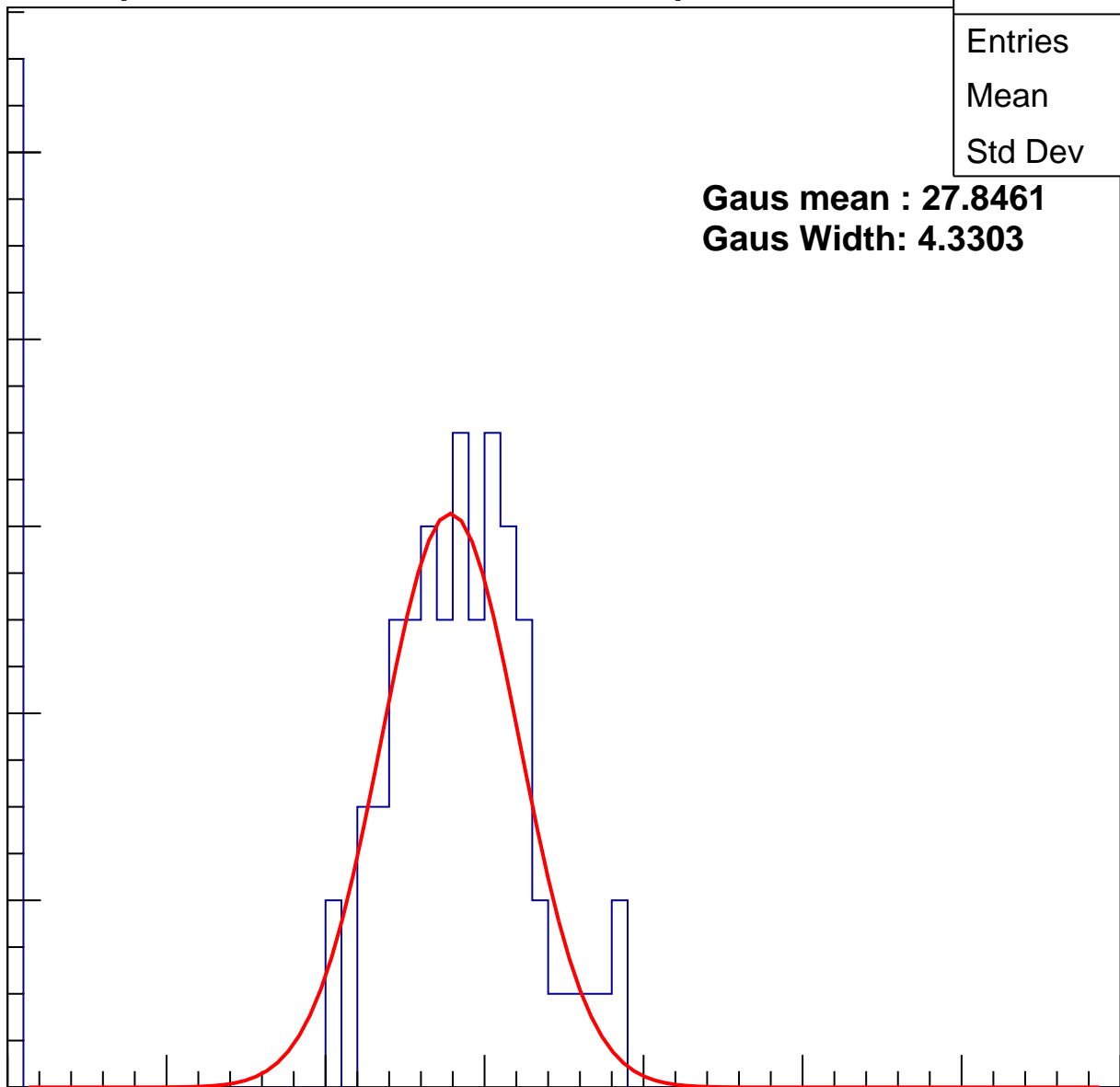
40

50

60

70

ampl



# B1L103S, U3-ch114, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	81
Mean	30.25
Std Dev	12.48

**Gaus mean : 35.2438**

**Gaus Width: 4.2269**

Entry

10

8

6

4

2

0

0

10

20

30

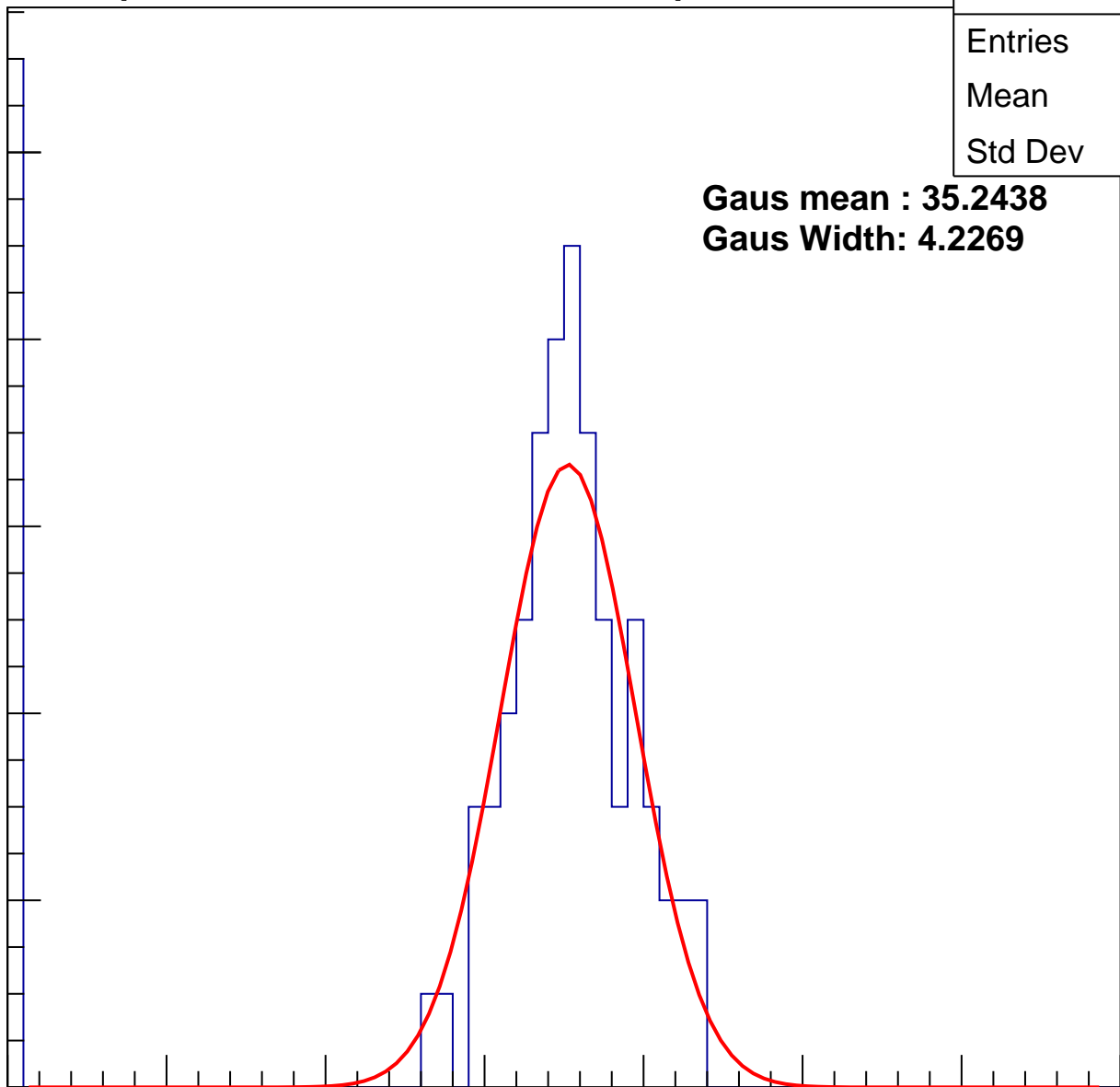
40

50

60

70

ampl



# B1L103S, U3-ch114, adc2

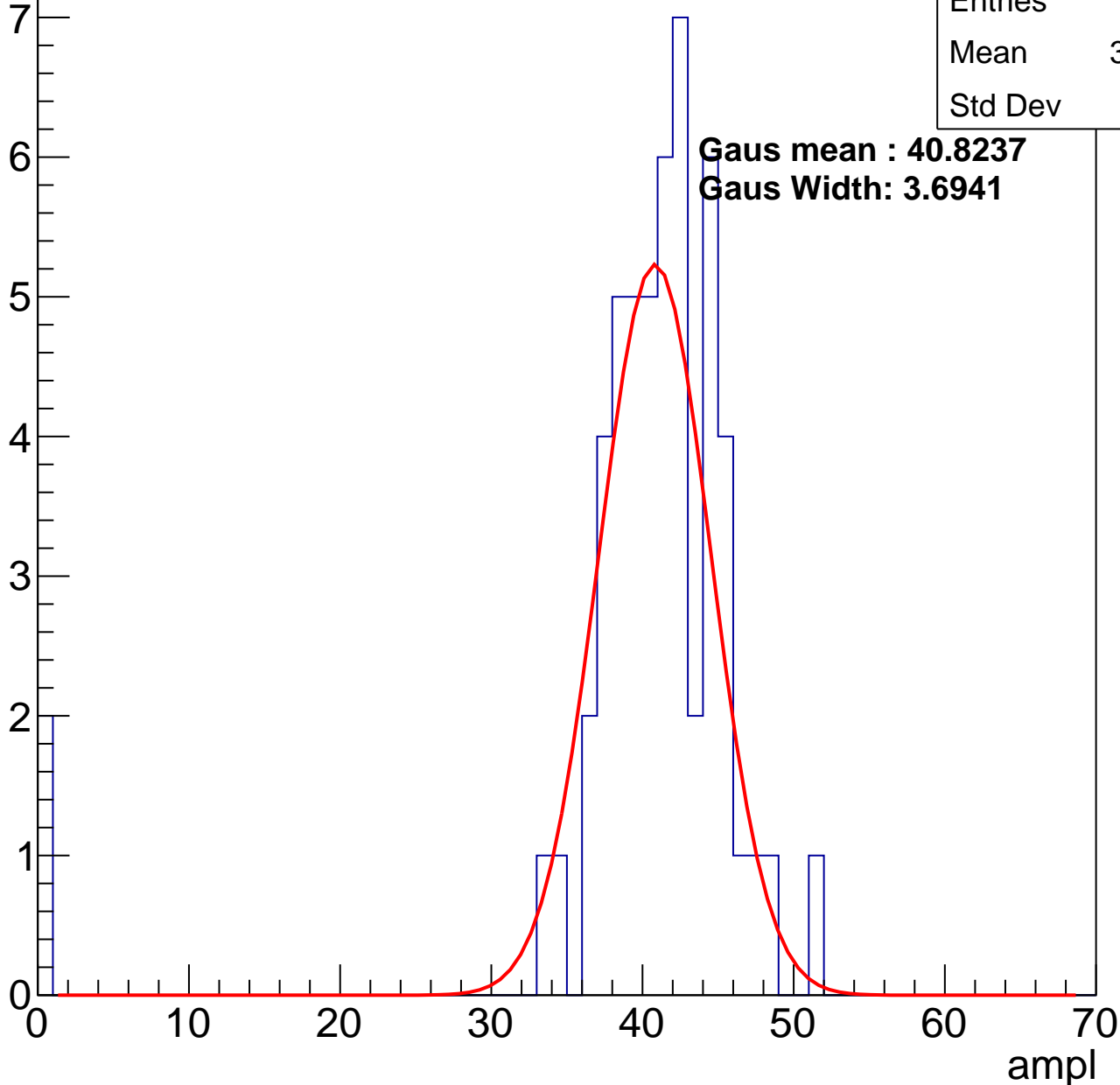
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	54
Mean	39.52
Std Dev	8.48

**Gaus mean : 40.8237**

**Gaus Width: 3.6941**

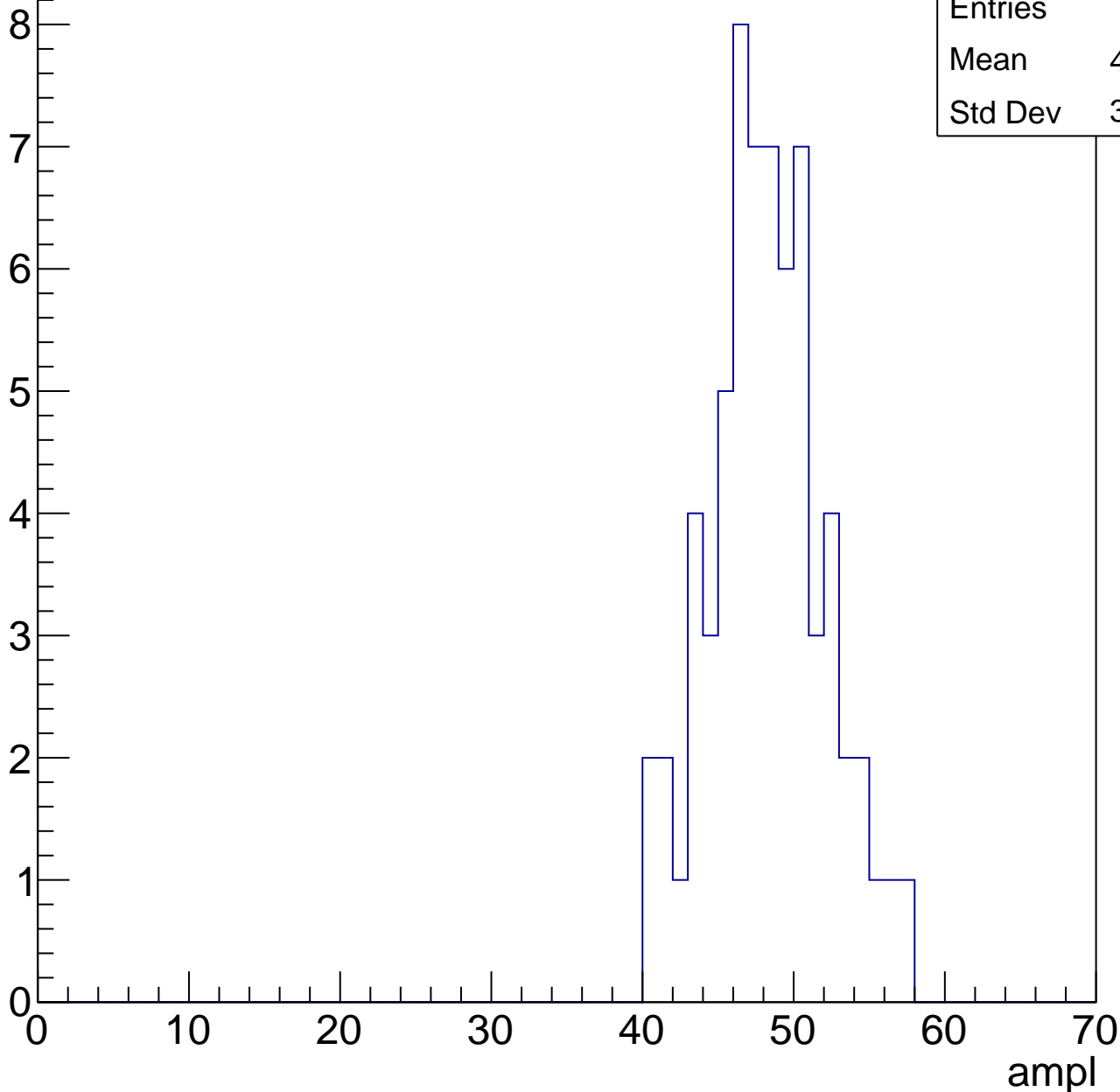


# B1L103S, U3-ch114, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	47.77
Std Dev	3.757

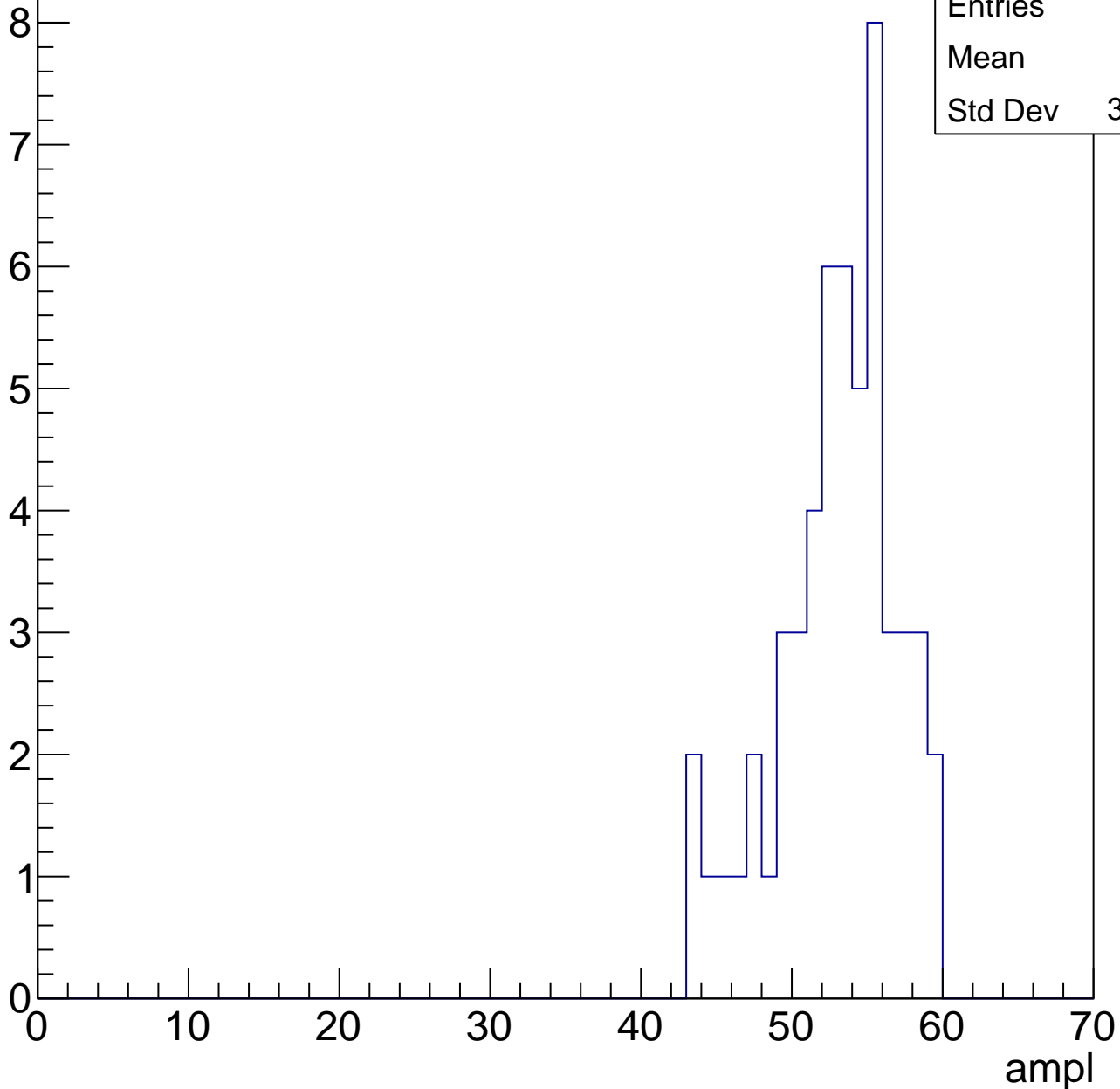


# B1L103S, U3-ch114, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	54
Mean	52.5
Std Dev	3.929

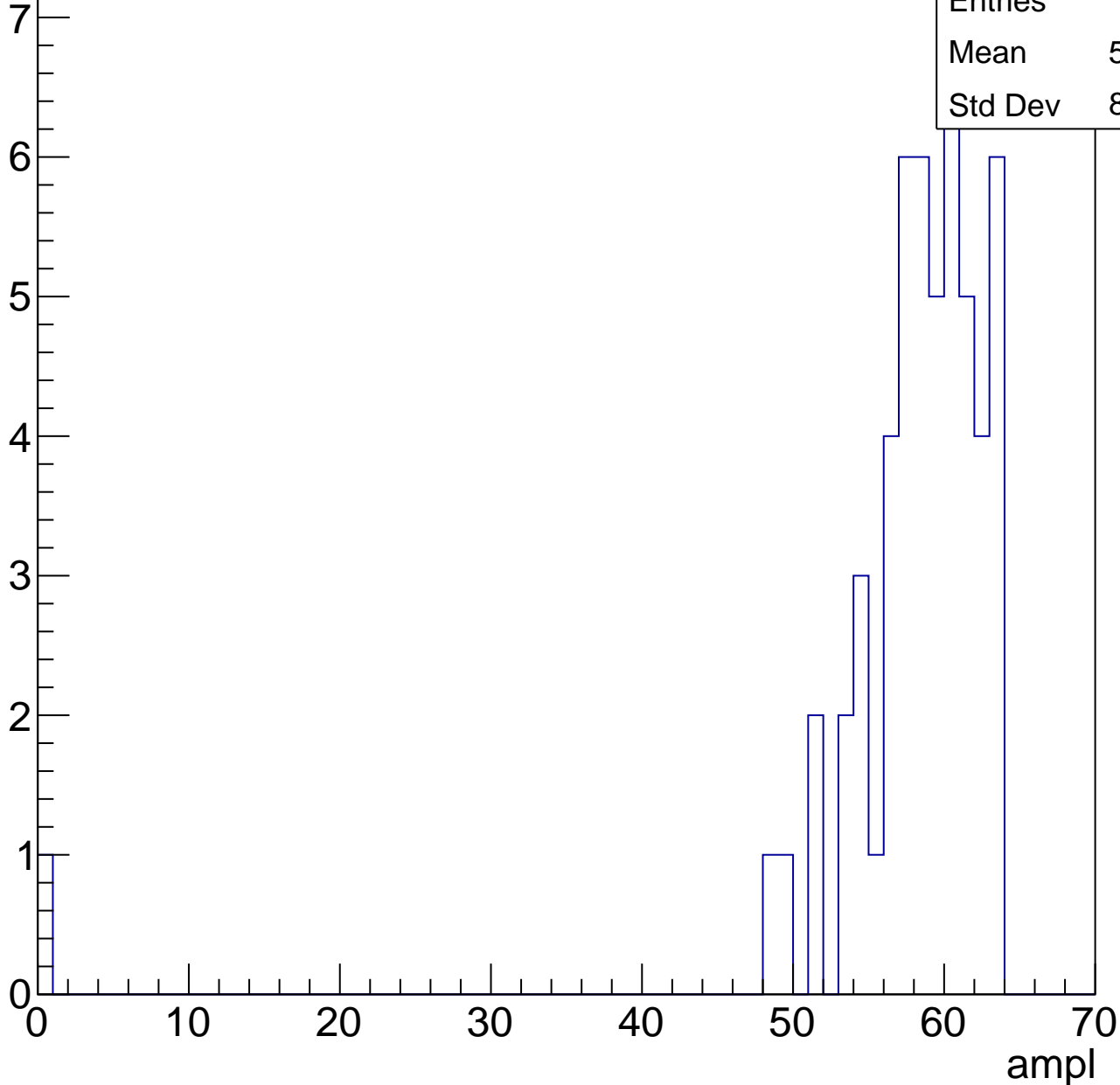


# B1L103S, U3-ch114, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	54
Mean	57.07
Std Dev	8.626

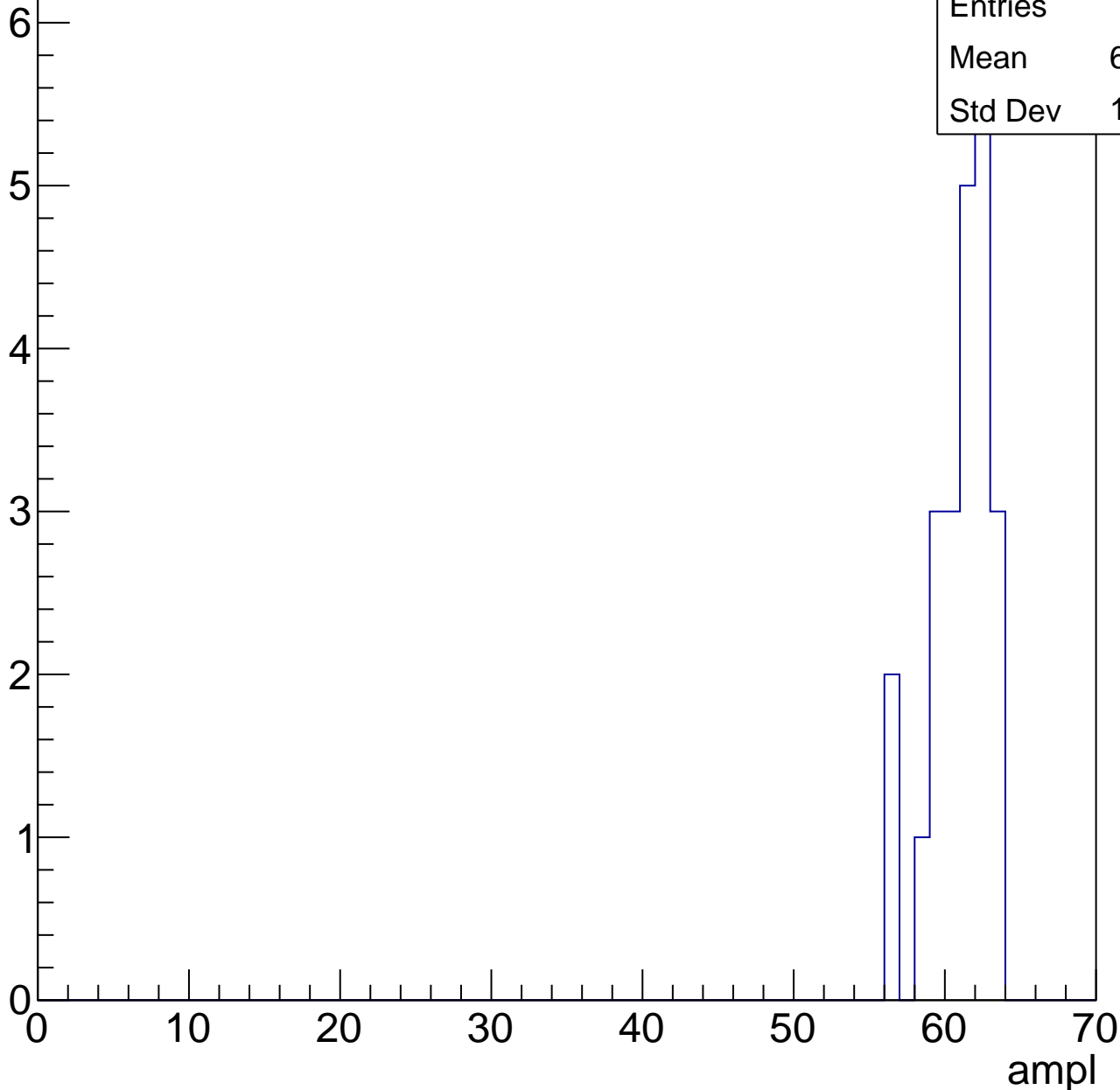


# B1L103S, U3-ch114, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	23
Mean	60.57
Std Dev	1.952





# B1L103S, U3-ch114, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry



# B1L103S, U3-ch115, adc0

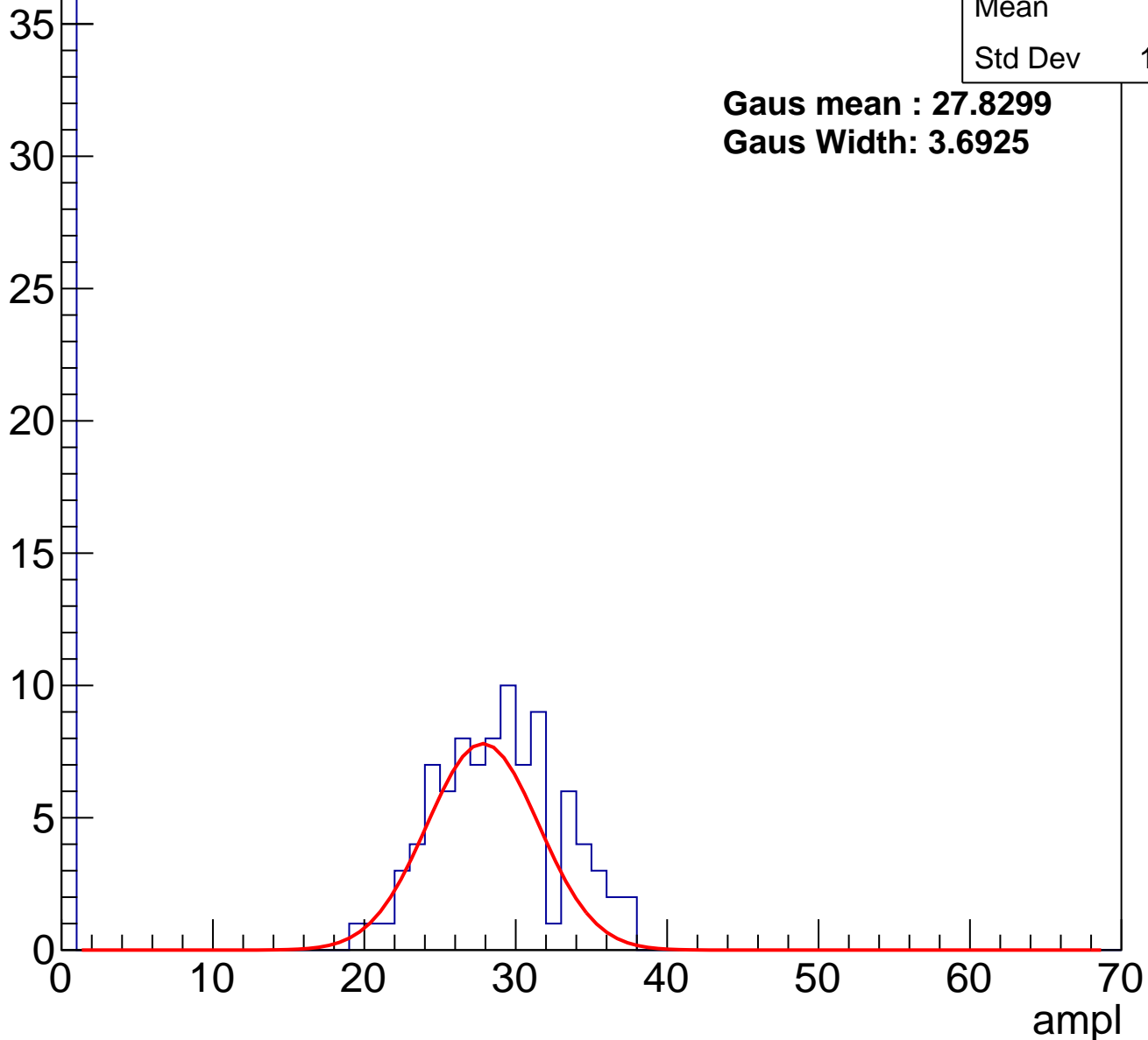
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	127
Mean	20.1
Std Dev	13.33

**Gaus mean : 27.8299**

**Gaus Width: 3.6925**

Entry



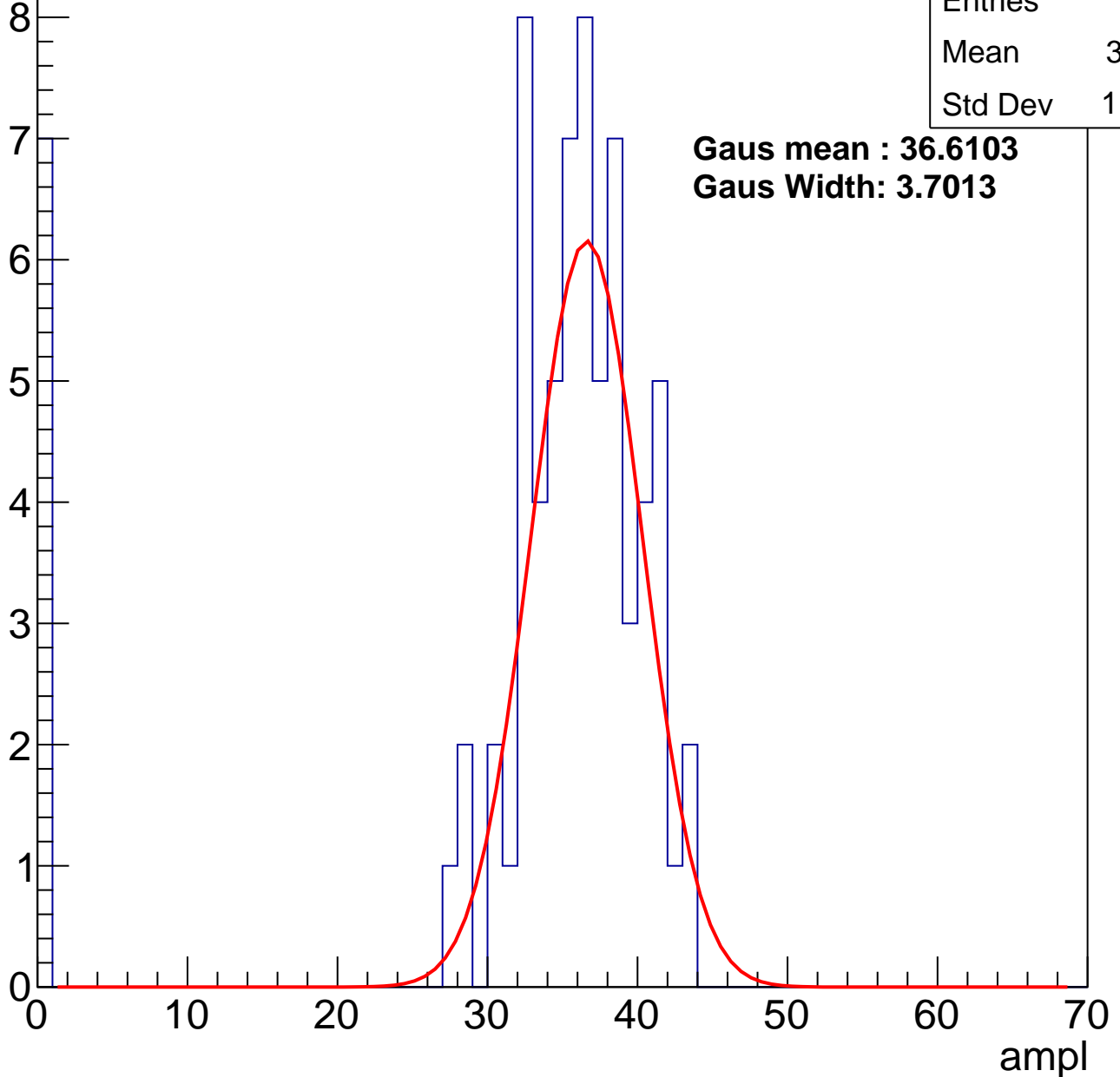
# B1L103S, U3-ch115, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	72
Mean	32.31
Std Dev	11.16

**Gaus mean : 36.6103**  
**Gaus Width: 3.7013**



# B1L103S, U3-ch115, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	74
Mean	35.8
Std Dev	15.38

**Gaus mean : 42.3795**

**Gaus Width: 4.1582**

Entry

10

8

6

4

2

0

0

10

20

30

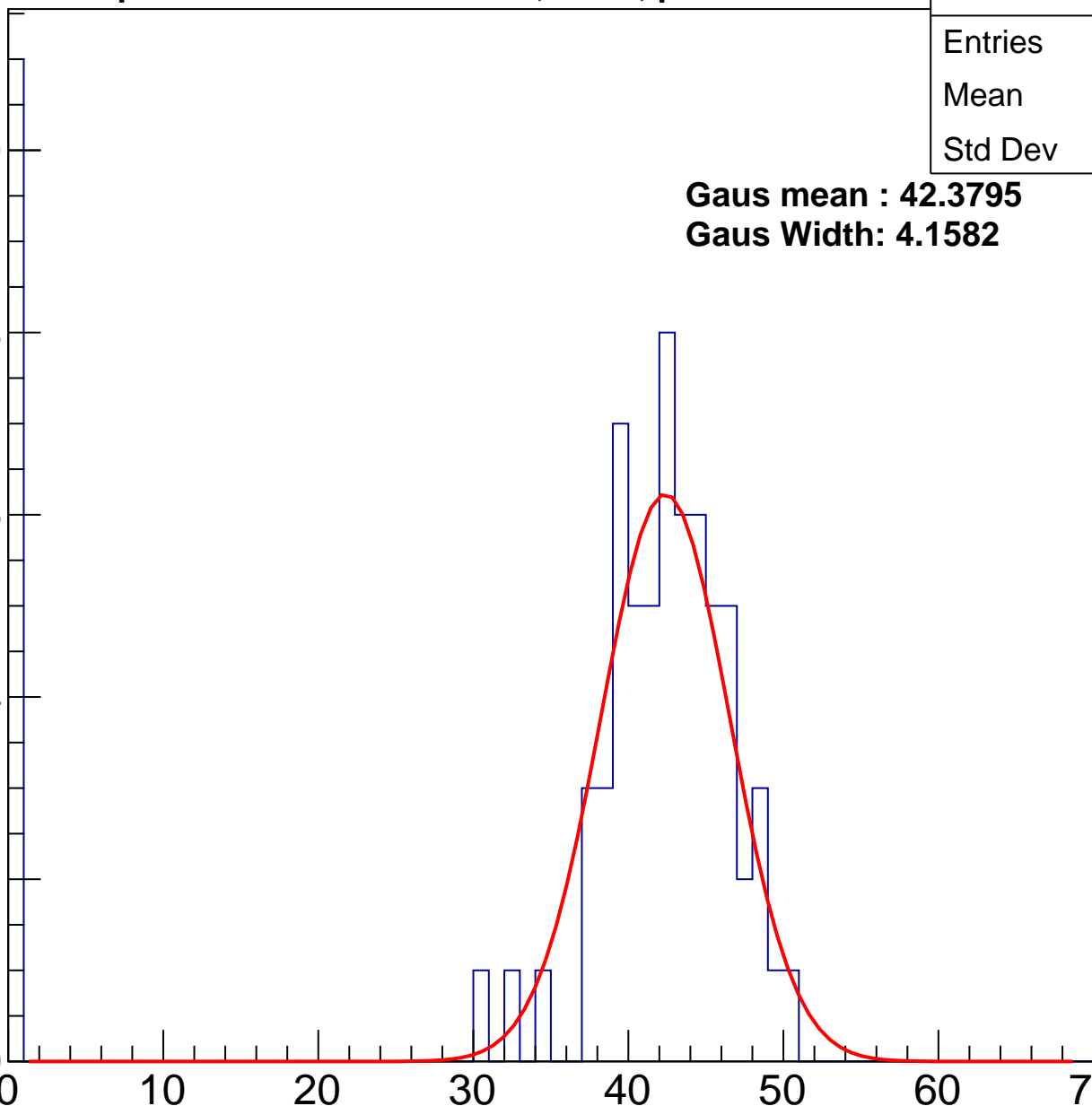
40

50

60

70

ampl

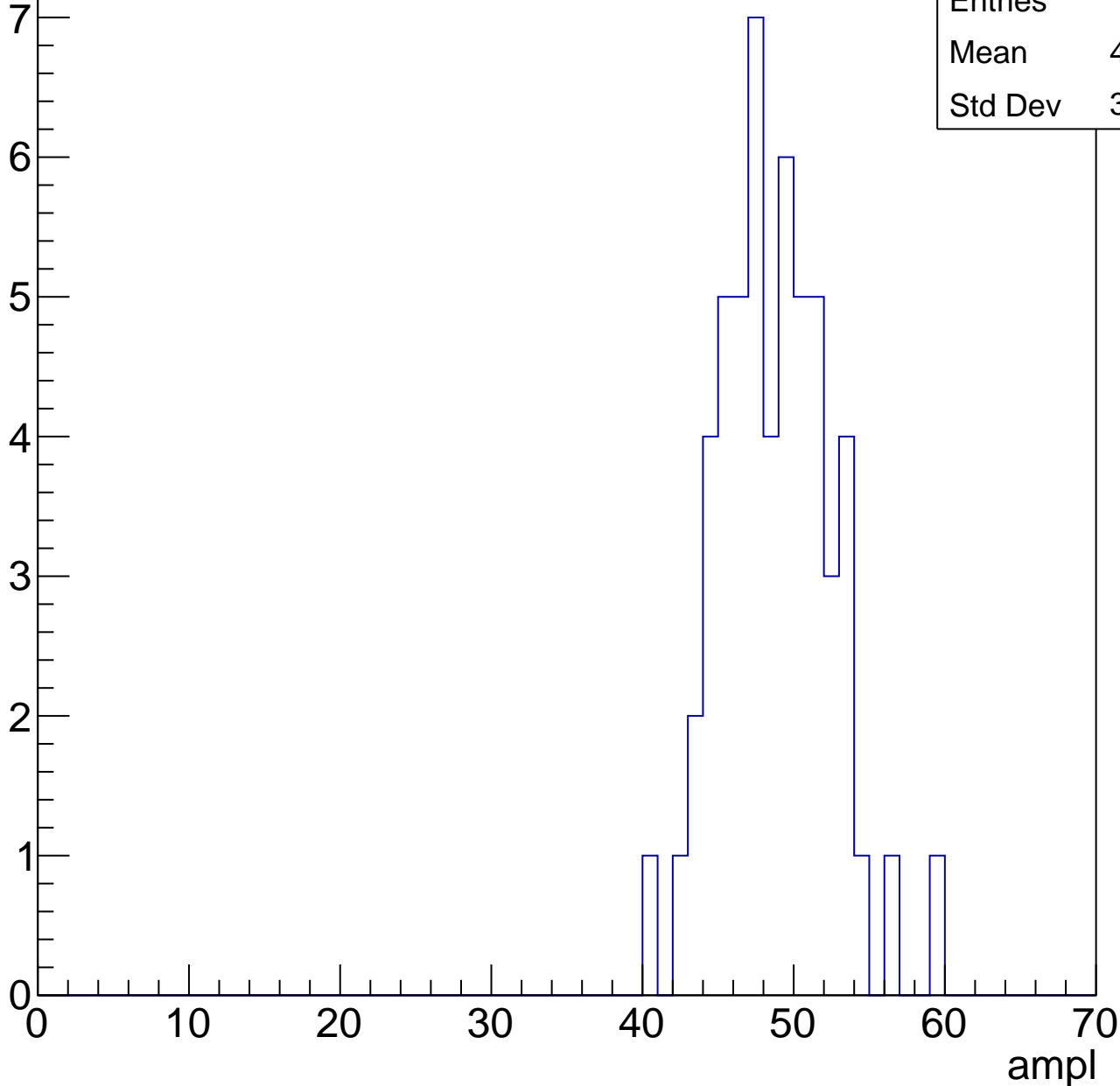


# B1L103S, U3-ch115, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

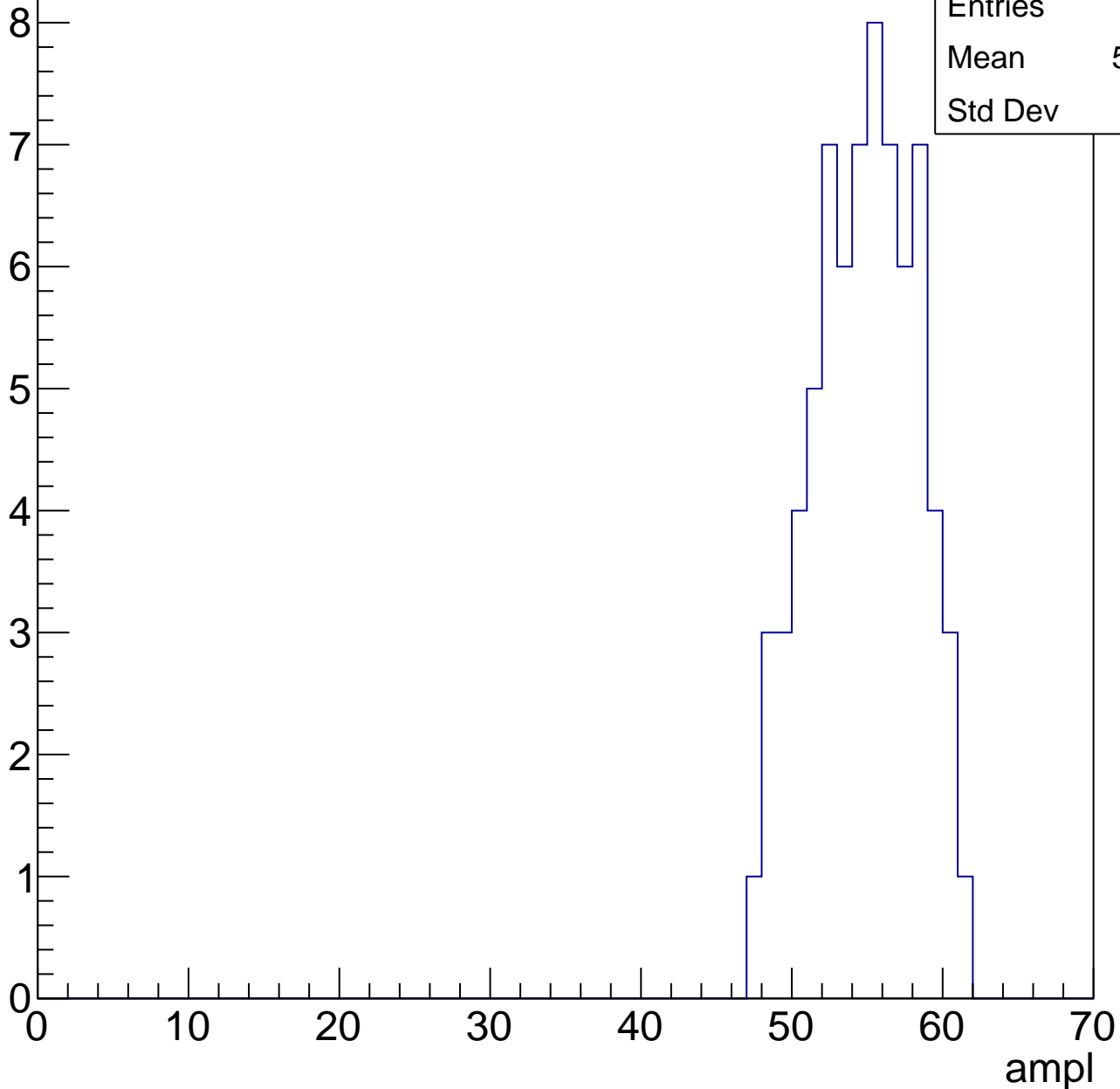
Entries	55
Mean	48.29
Std Dev	3.622



# B1L103S, U3-ch115, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



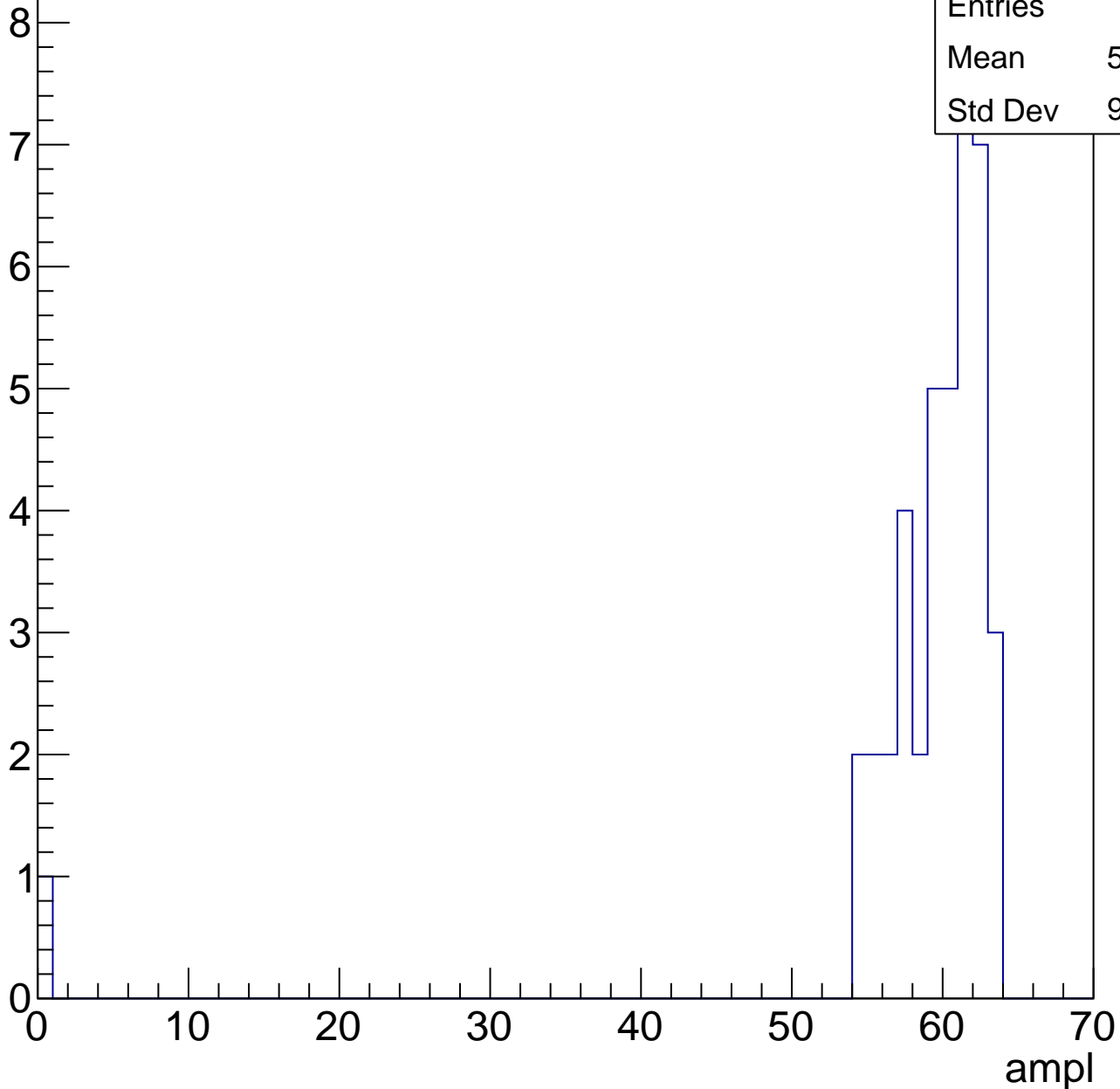
Entries	72
Mean	54.31
Std Dev	3.39

# B1L103S, U3-ch115, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	41
Mean	58.05
Std Dev	9.512

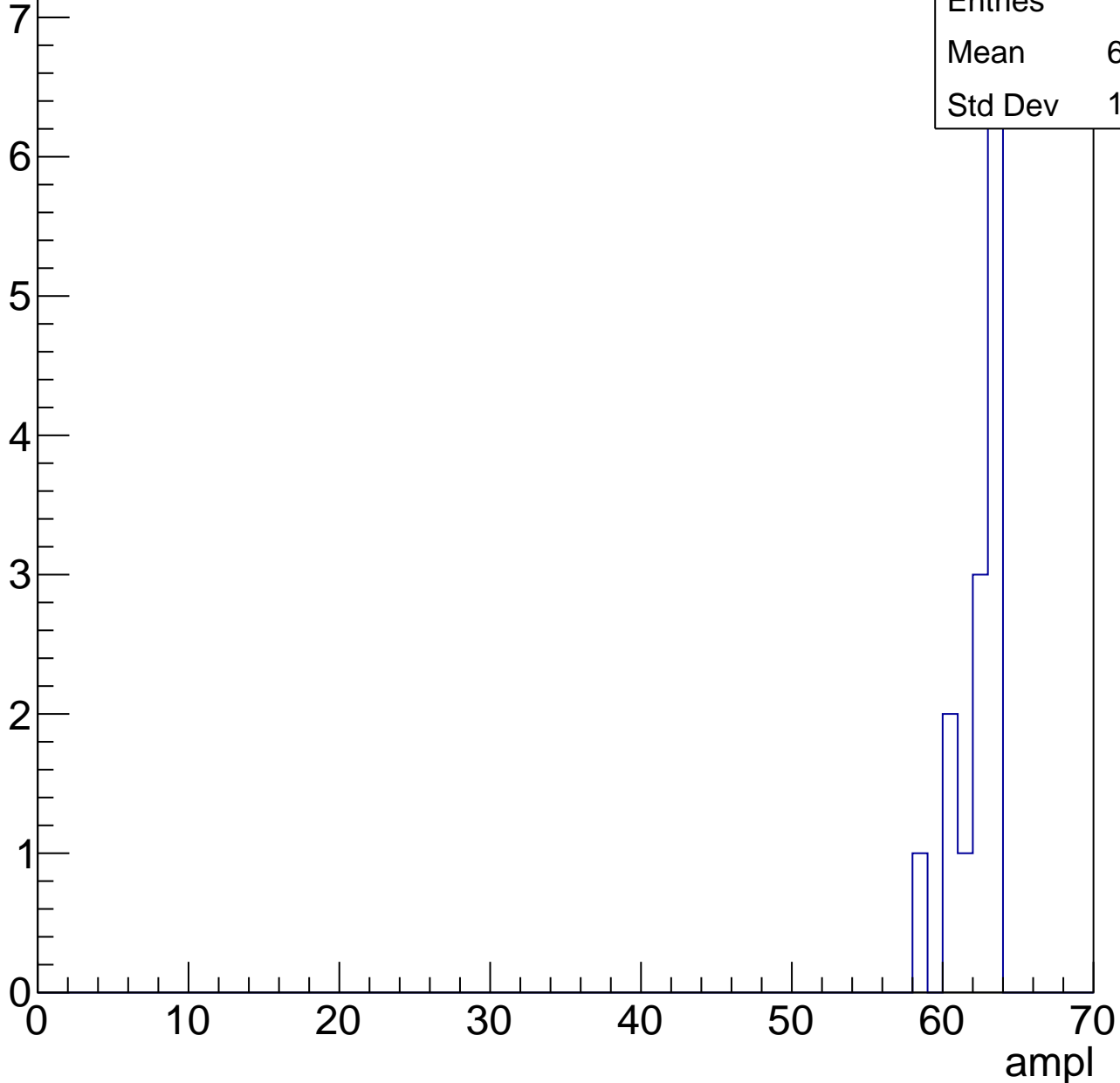


# B1L103S, U3-ch115, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	14
Mean	61.86
Std Dev	1.505





# B1L103S, U3-ch115, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	18
Mean	0
Std Dev	0

# B1L103S, U3-ch116, adc0

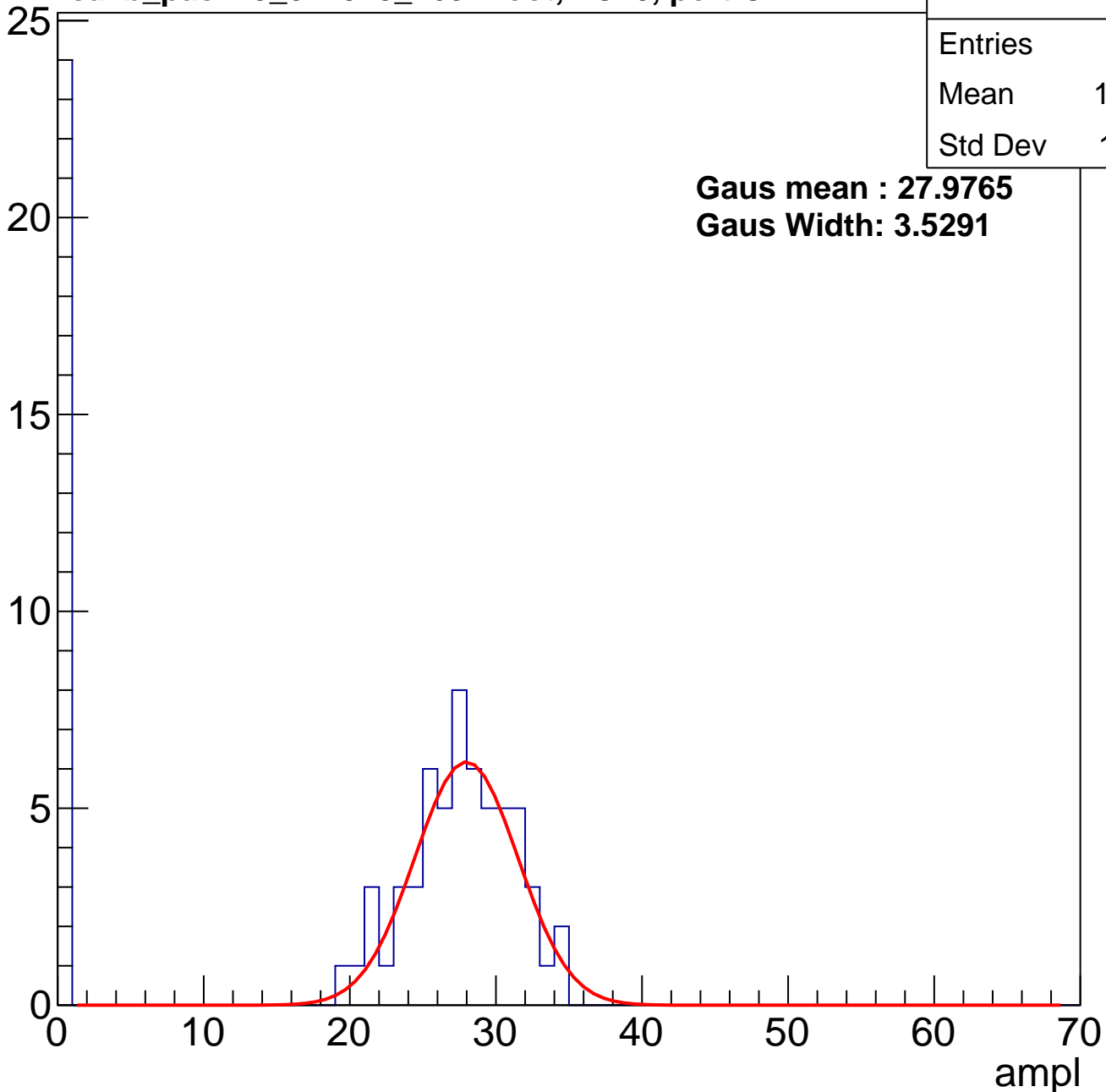
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	82
Mean	19.22
Std Dev	12.71

**Gaus mean : 27.9765**

**Gaus Width: 3.5291**

Entry



# B1L103S, U3-ch116, adc1

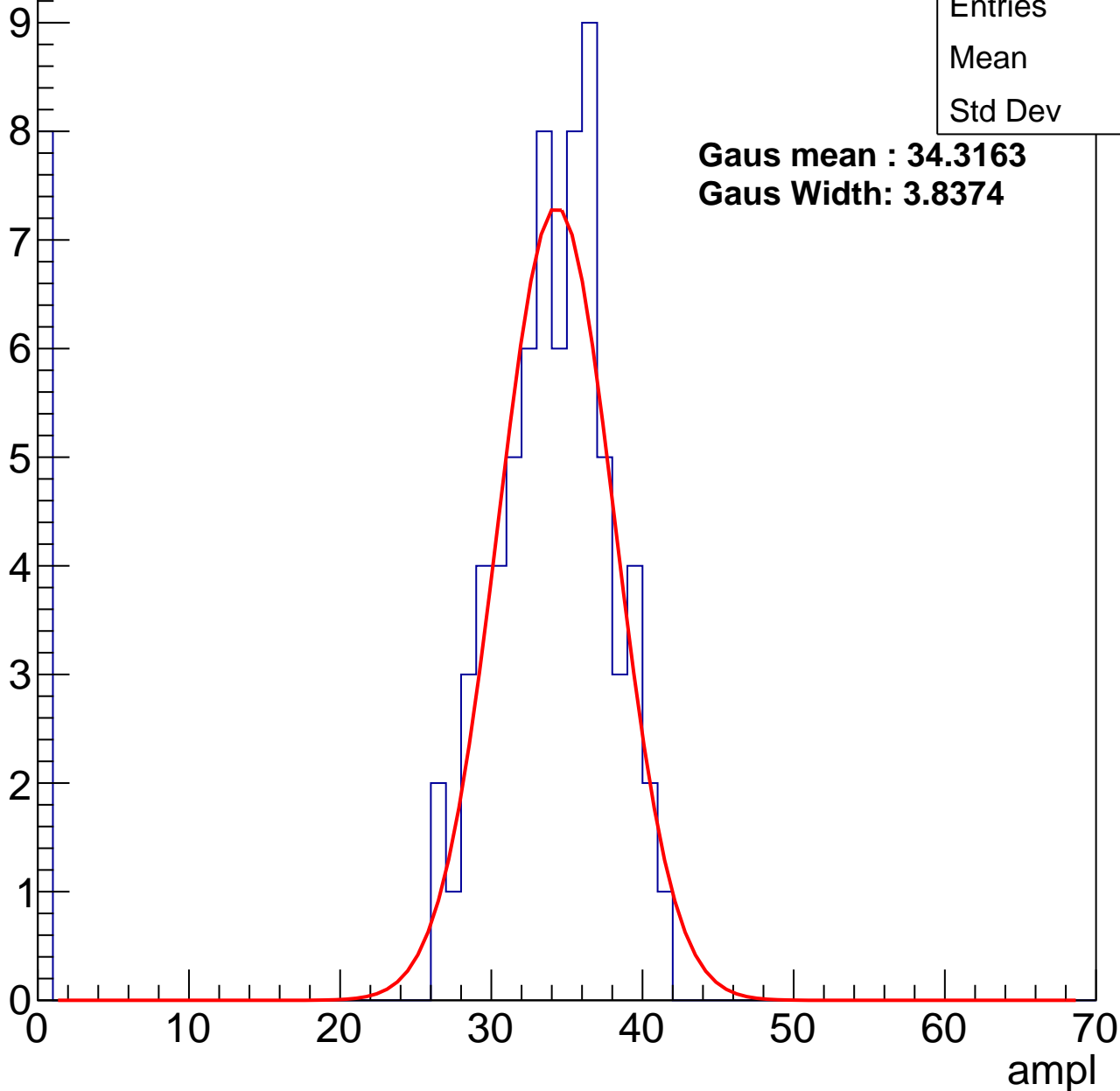
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	79
Mean	30.3
Std Dev	10.7

**Gaus mean : 34.3163**

**Gaus Width: 3.8374**



# B1L103S, U3-ch116, adc2

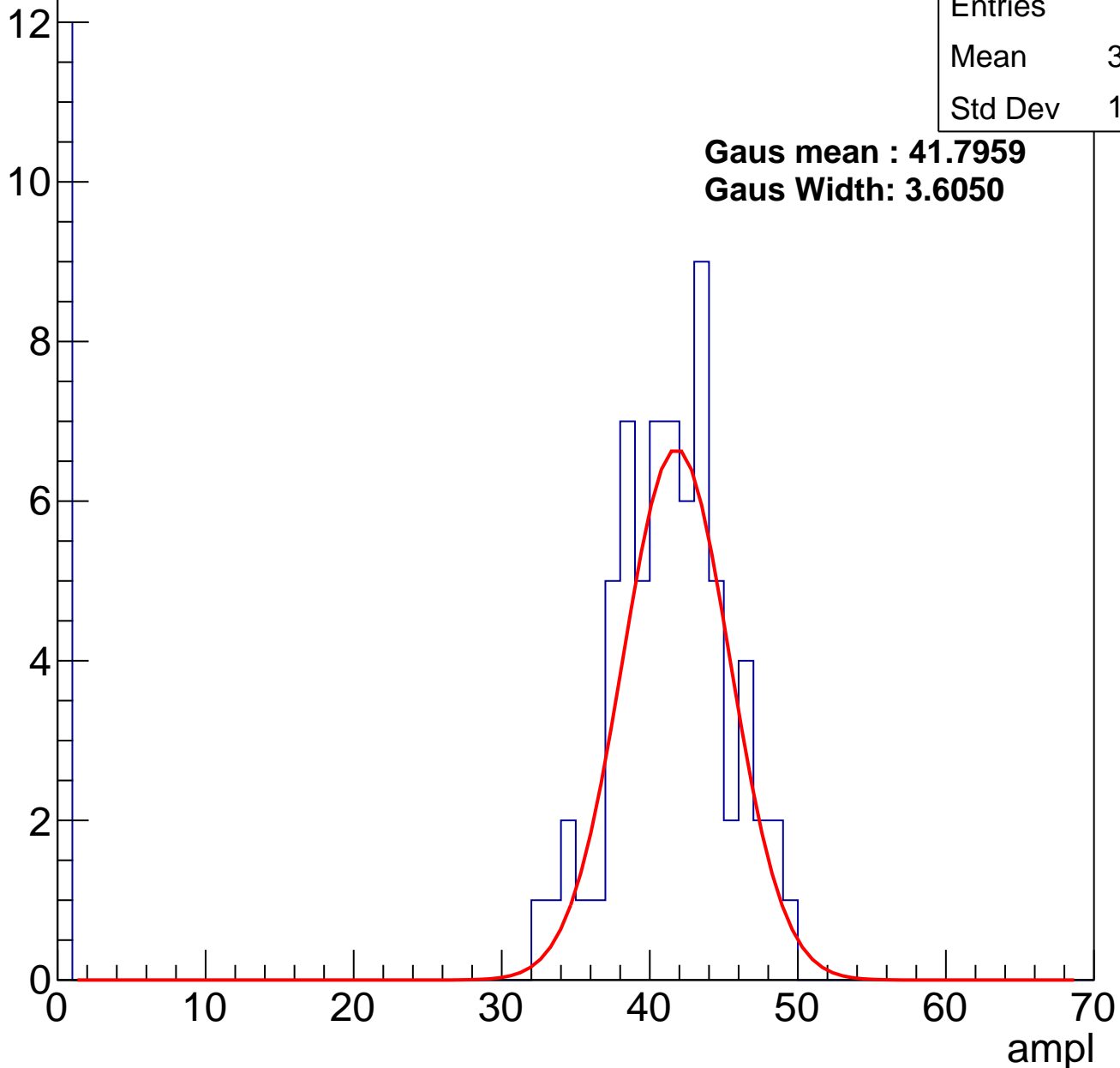
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	80
Mean	34.86
Std Dev	15.04

**Gaus mean : 41.7959**

**Gaus Width: 3.6050**

Entry

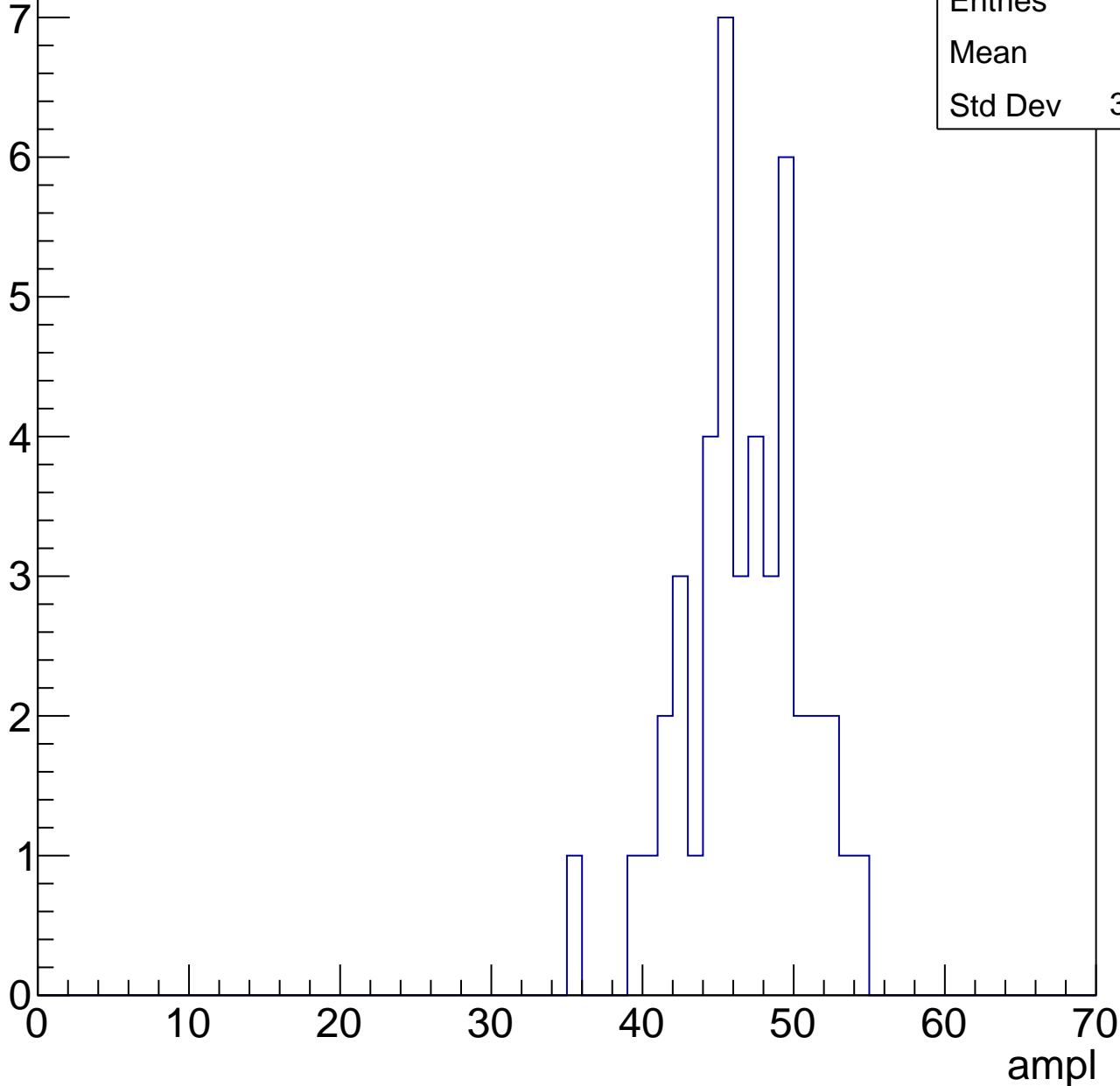


# B1L103S, U3-ch116, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

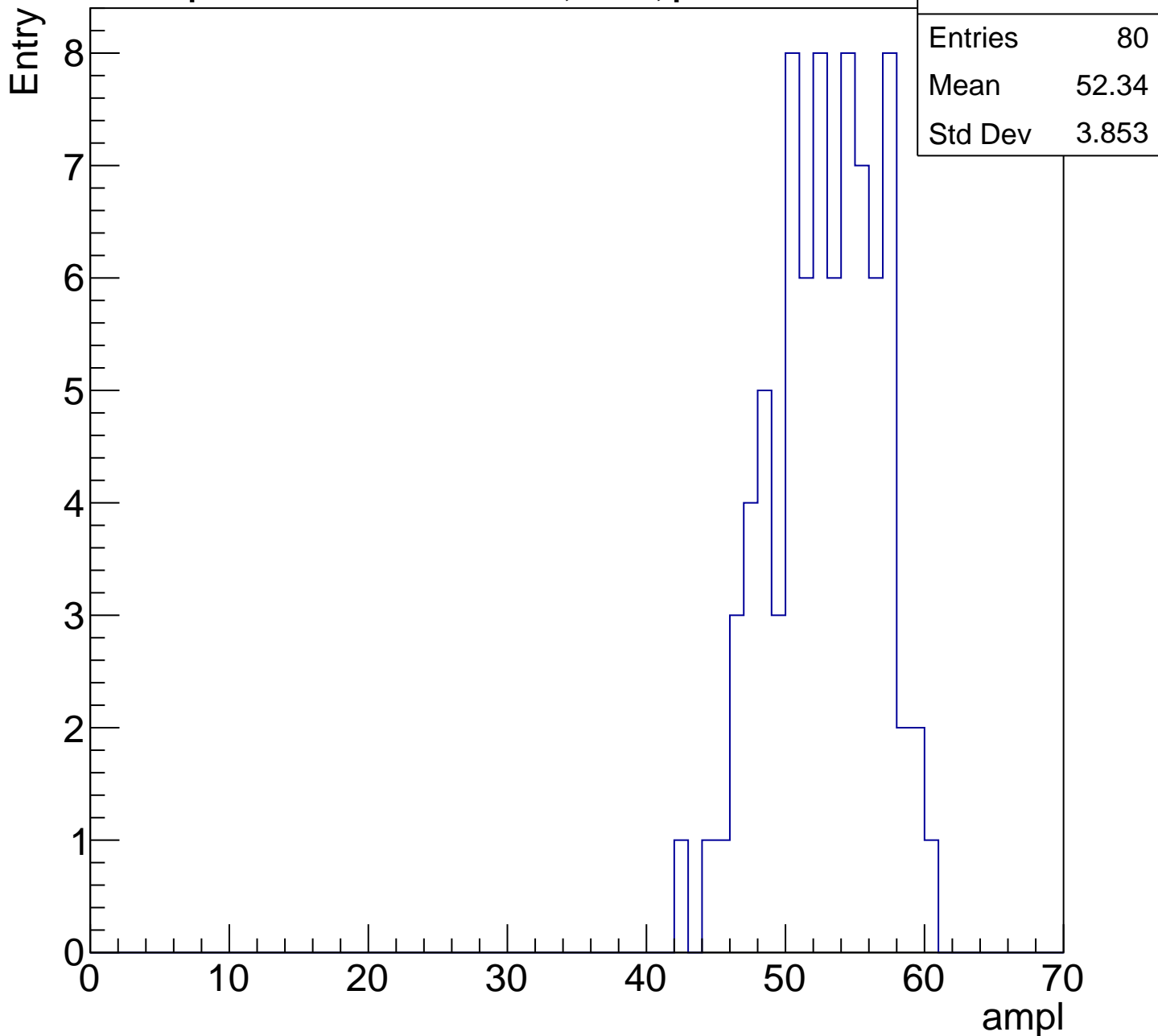
Entry

Entries	44
Mean	46.2
Std Dev	3.906



# B1L103S, U3-ch116, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

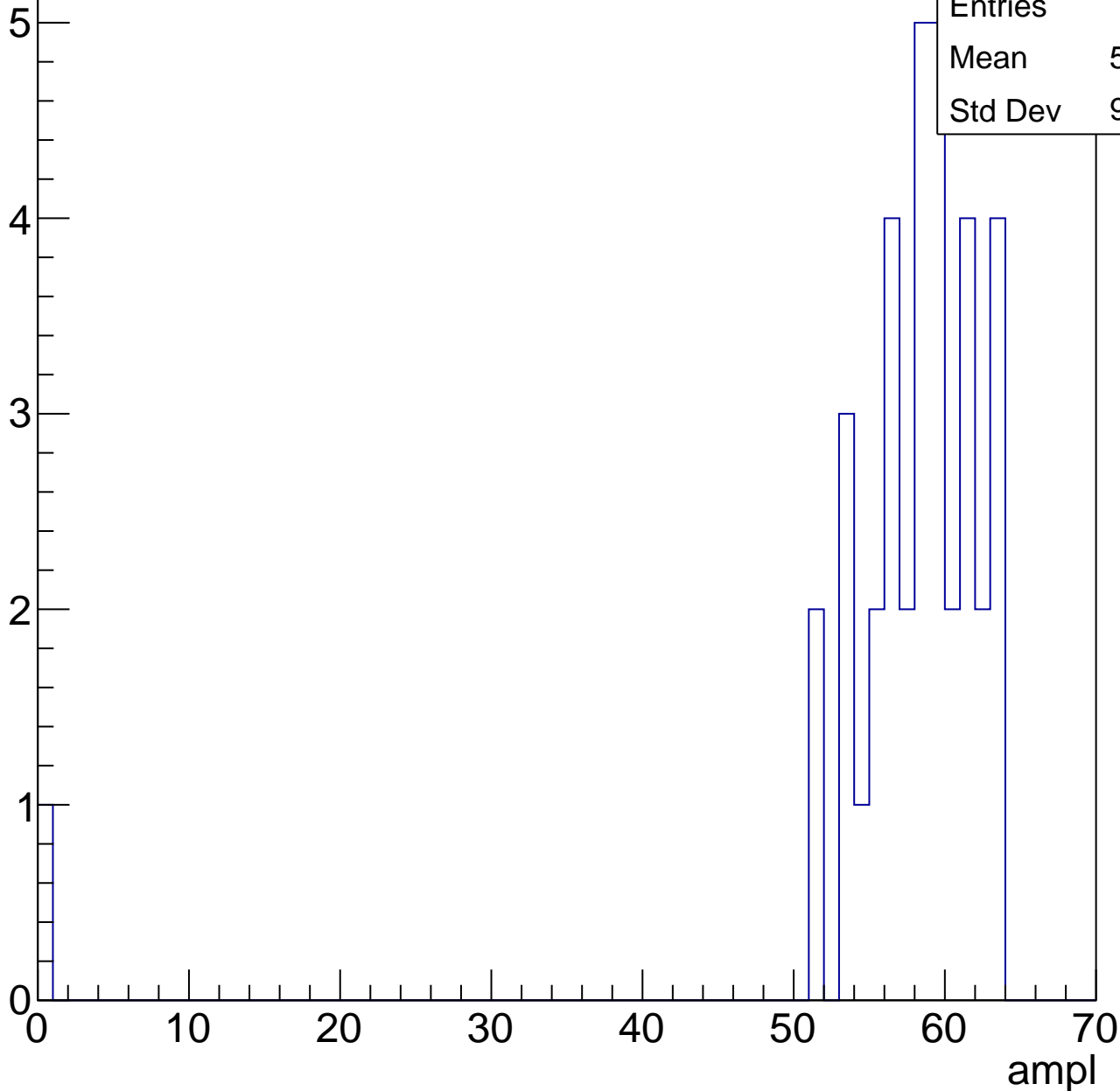


# B1L103S, U3-ch116, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	37
Mean	56.43
Std Dev	9.972

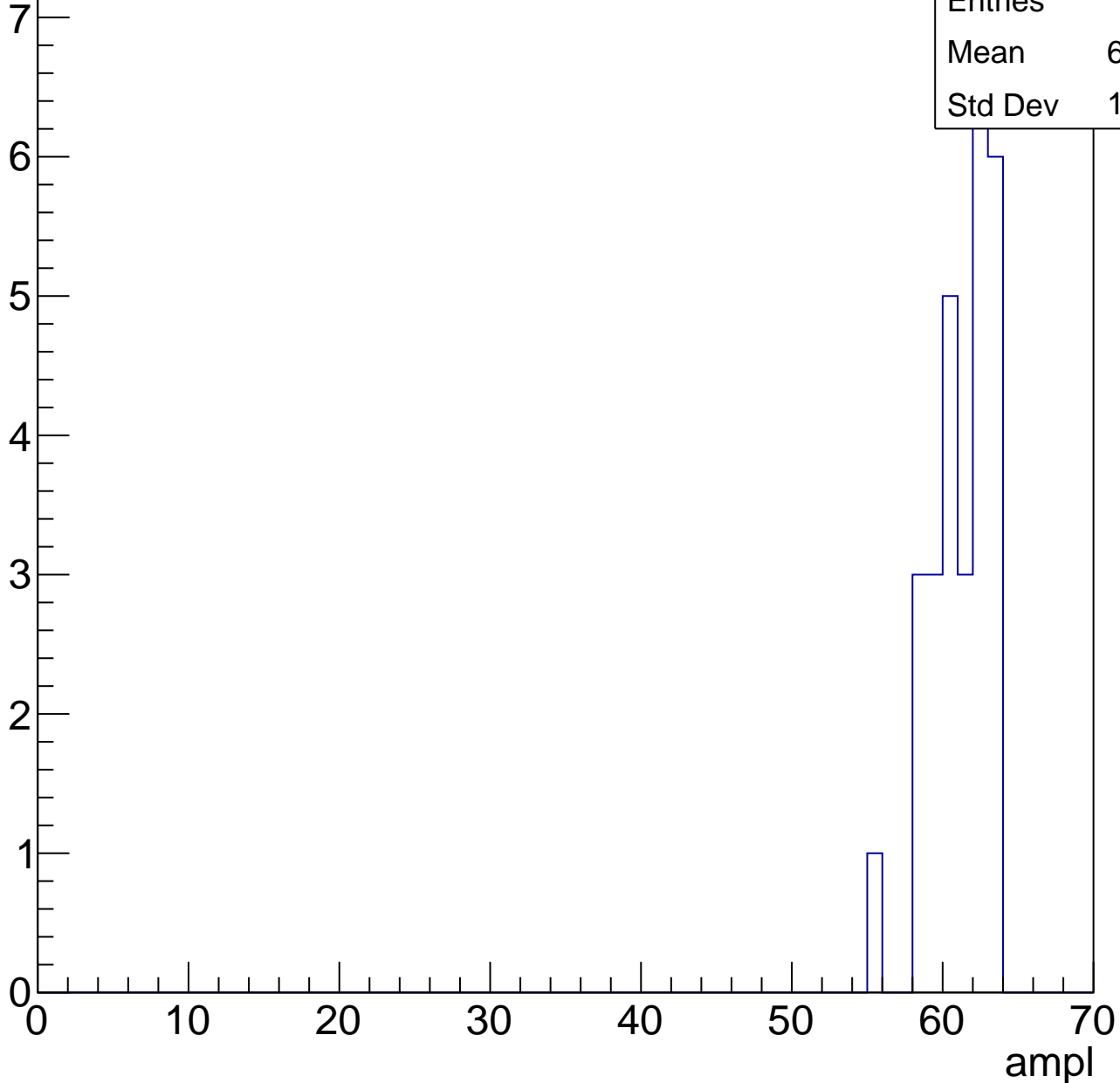


# B1L103S, U3-ch116, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	28
Mean	60.75
Std Dev	1.975



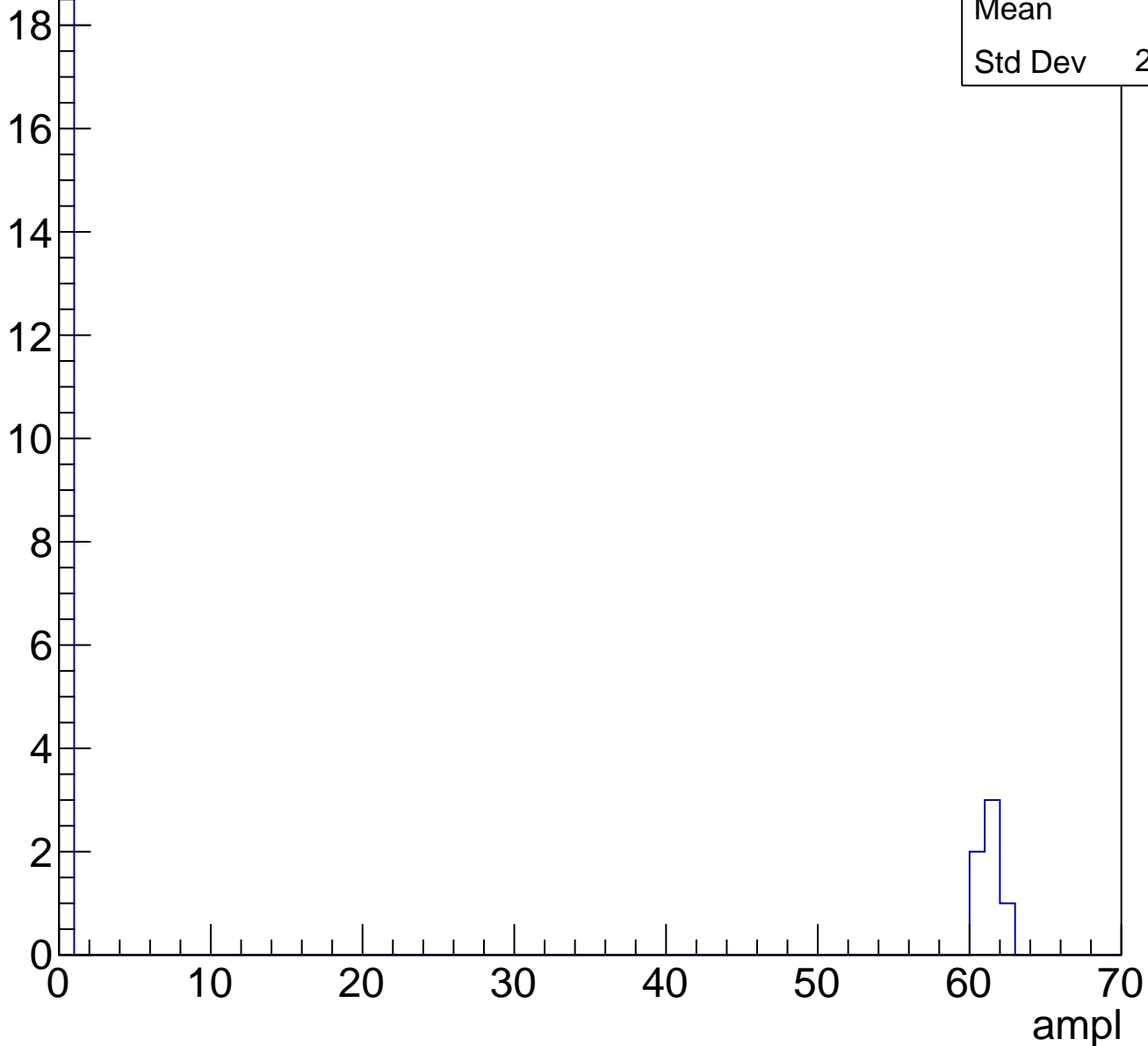


# B1L103S, U3-ch116, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	25
Mean	14.6
Std Dev	25.98

Entry



# B1L103S, U3-ch117, adc0

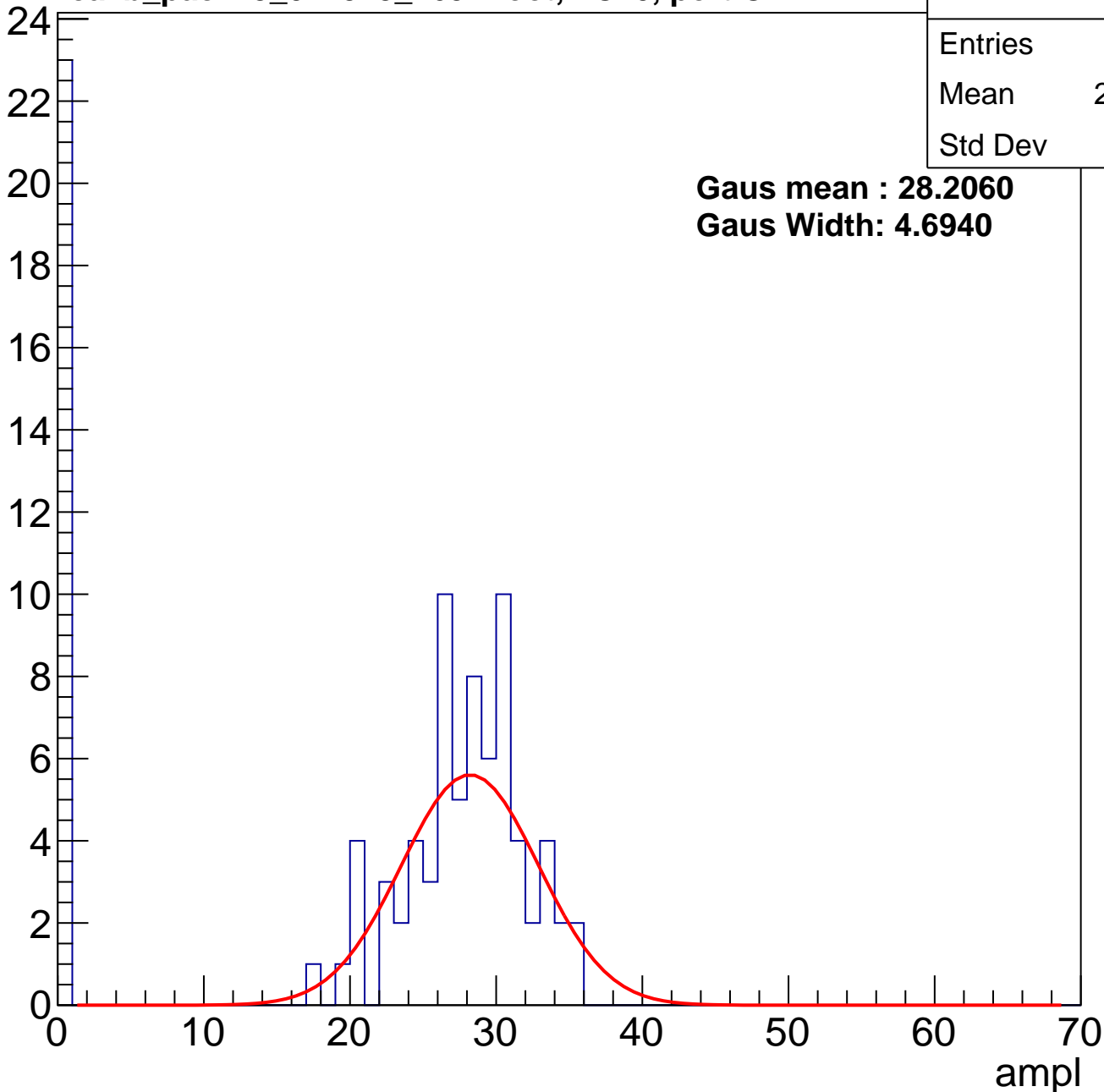
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	94
Mean	20.74
Std Dev	12.3

**Gaus mean : 28.2060**

**Gaus Width: 4.6940**

Entry



# B1L103S, U3-ch117, adc1

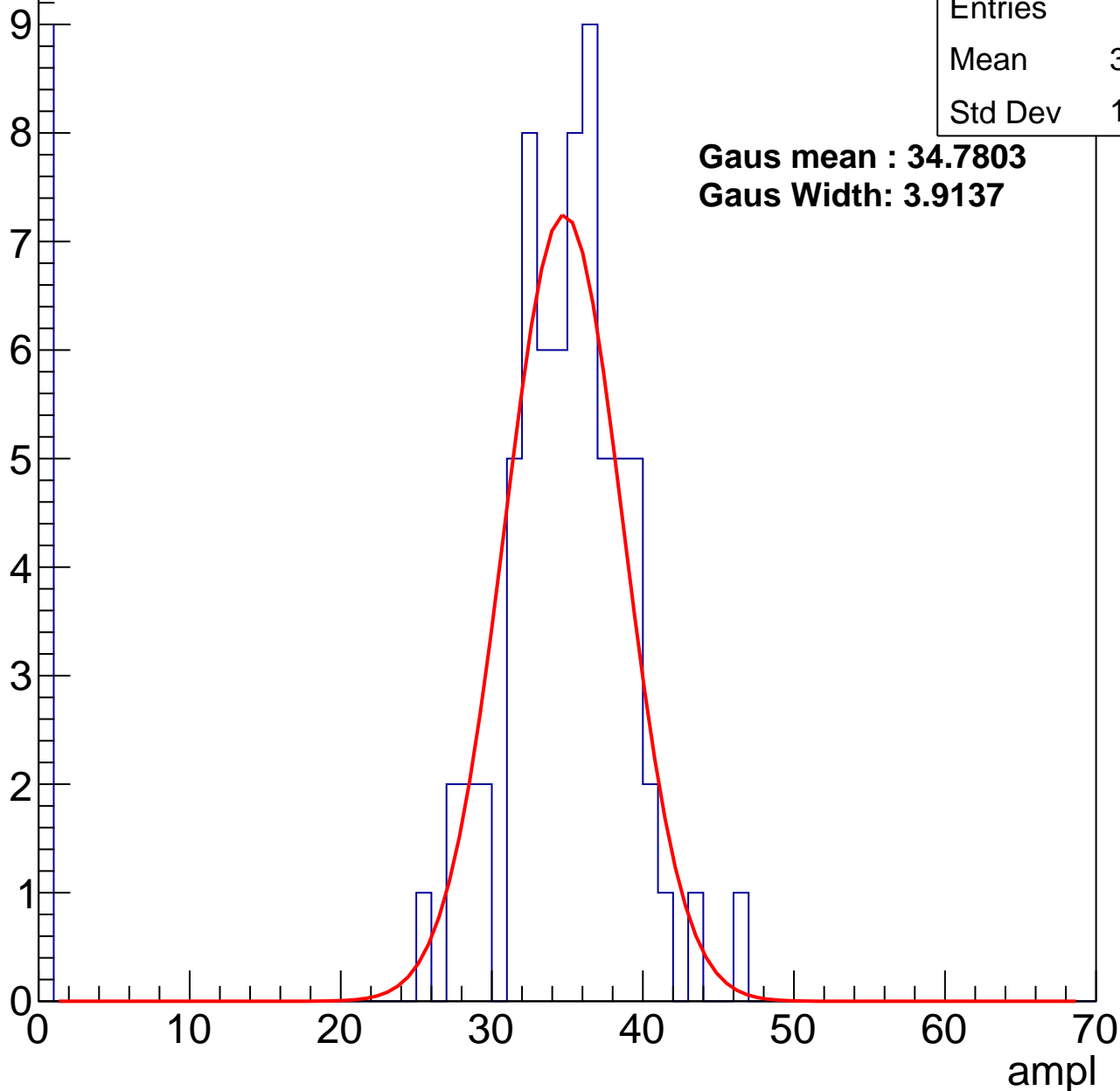
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	78
Mean	30.64
Std Dev	11.63

**Gaus mean : 34.7803**

**Gaus Width: 3.9137**



# B1L103S, U3-ch117, adc2

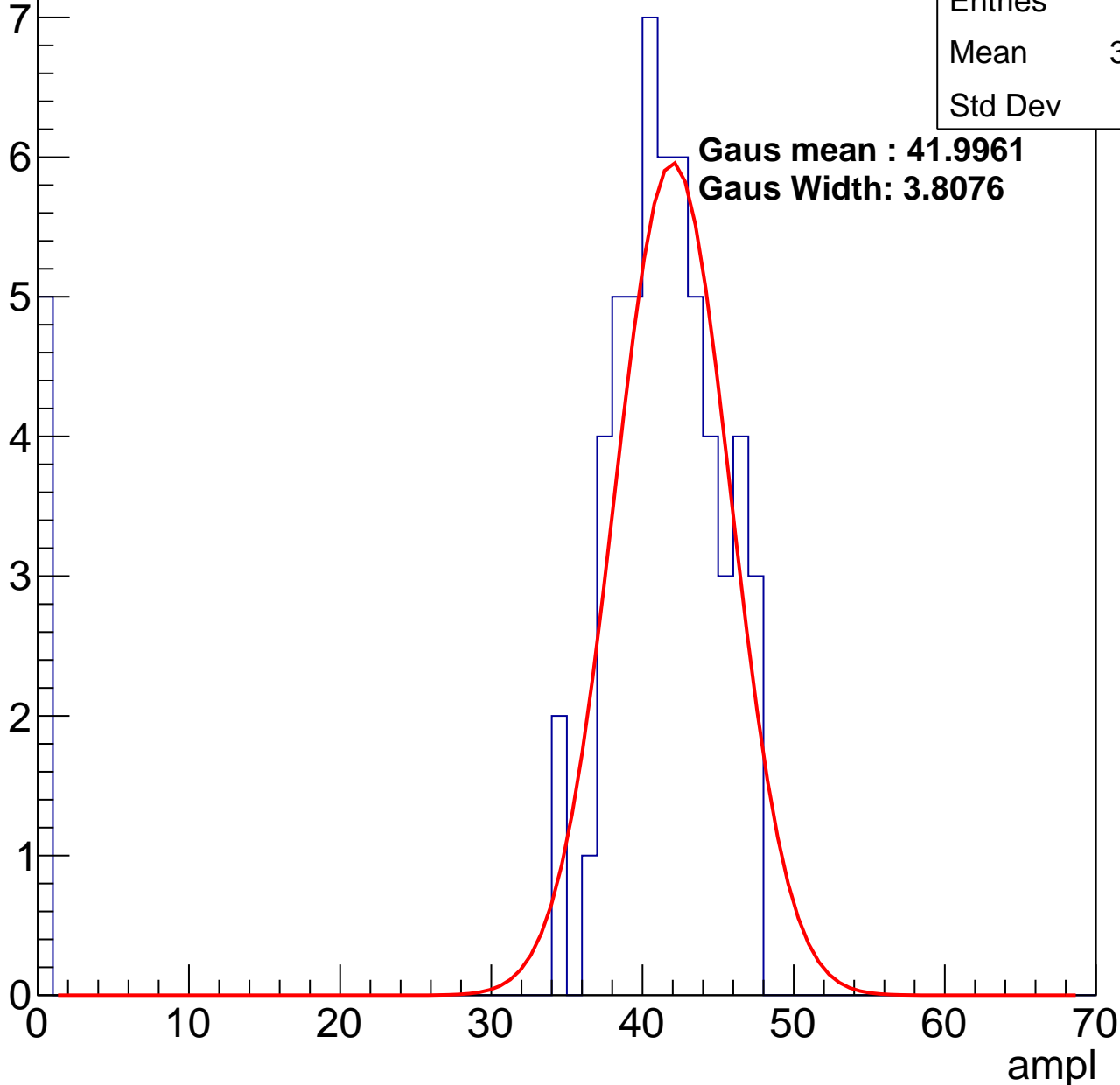
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	60
Mean	37.77
Std Dev	11.8

**Gaus mean : 41.9961**

**Gaus Width: 3.8076**

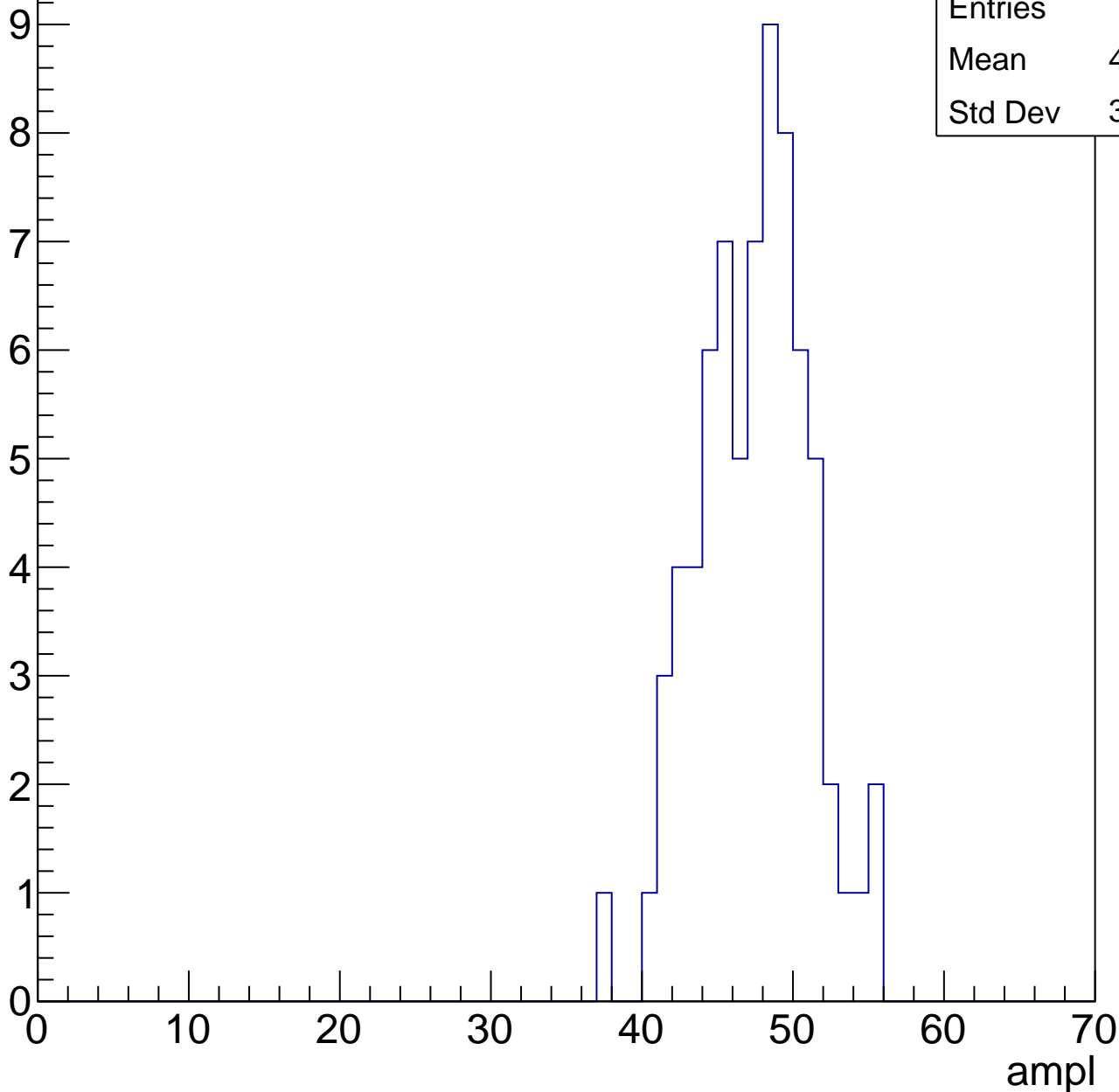


# B1L103S, U3-ch117, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	72
Mean	46.92
Std Dev	3.624

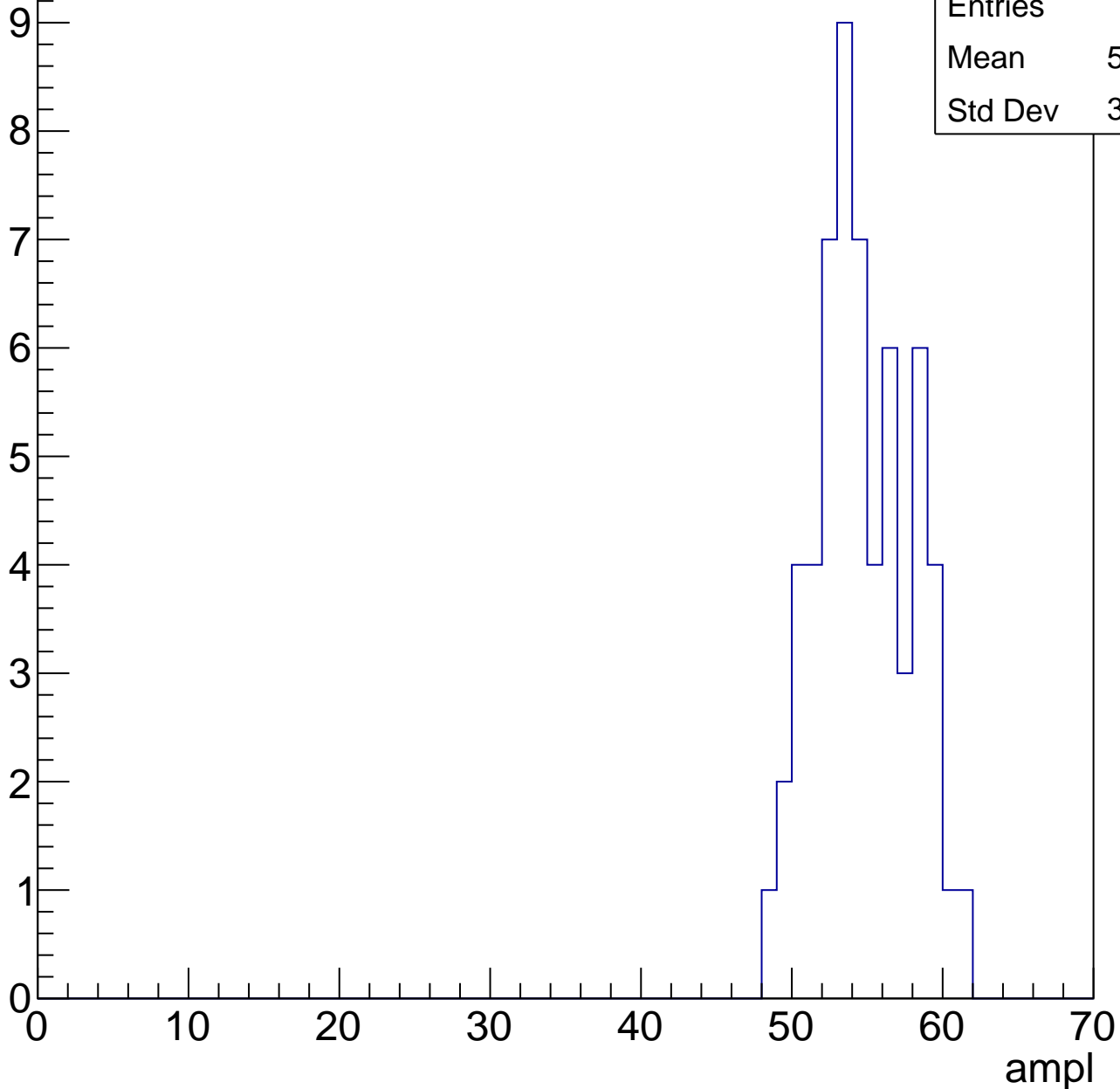


# B1L103S, U3-ch117, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	54.25
Std Dev	3.068



# B1L103S, U3-ch117, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

7

6

5

4

3

2

1

0

Entries	46
Mean	58.46
Std Dev	2.969

ampl

0

10

20

30

40

50

60

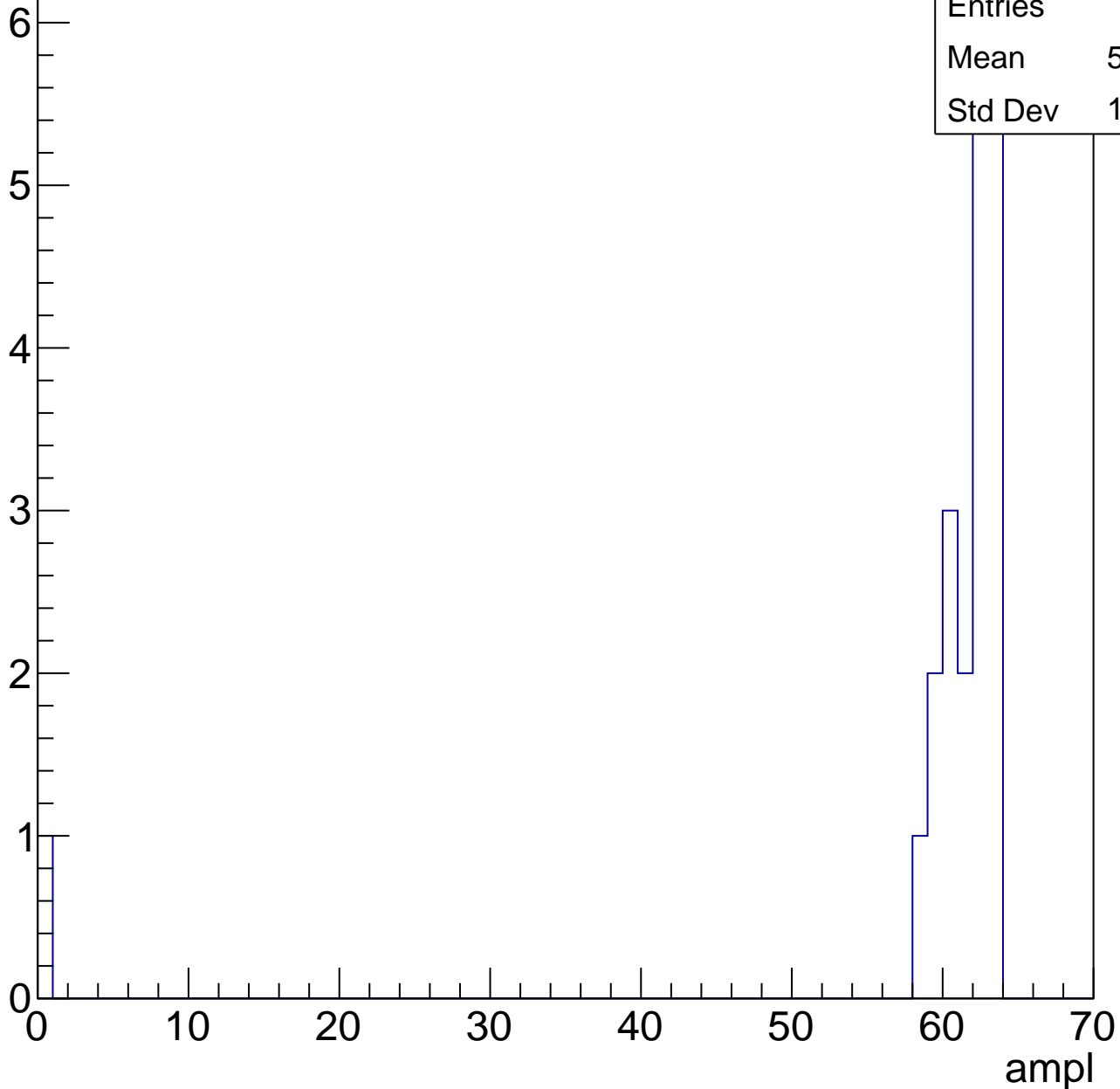
70

# B1L103S, U3-ch117, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	21
Mean	58.48
Std Dev	13.16





# B1L103S, U3-ch117, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51

Entry



# B1L103S, U3-ch118, adc0

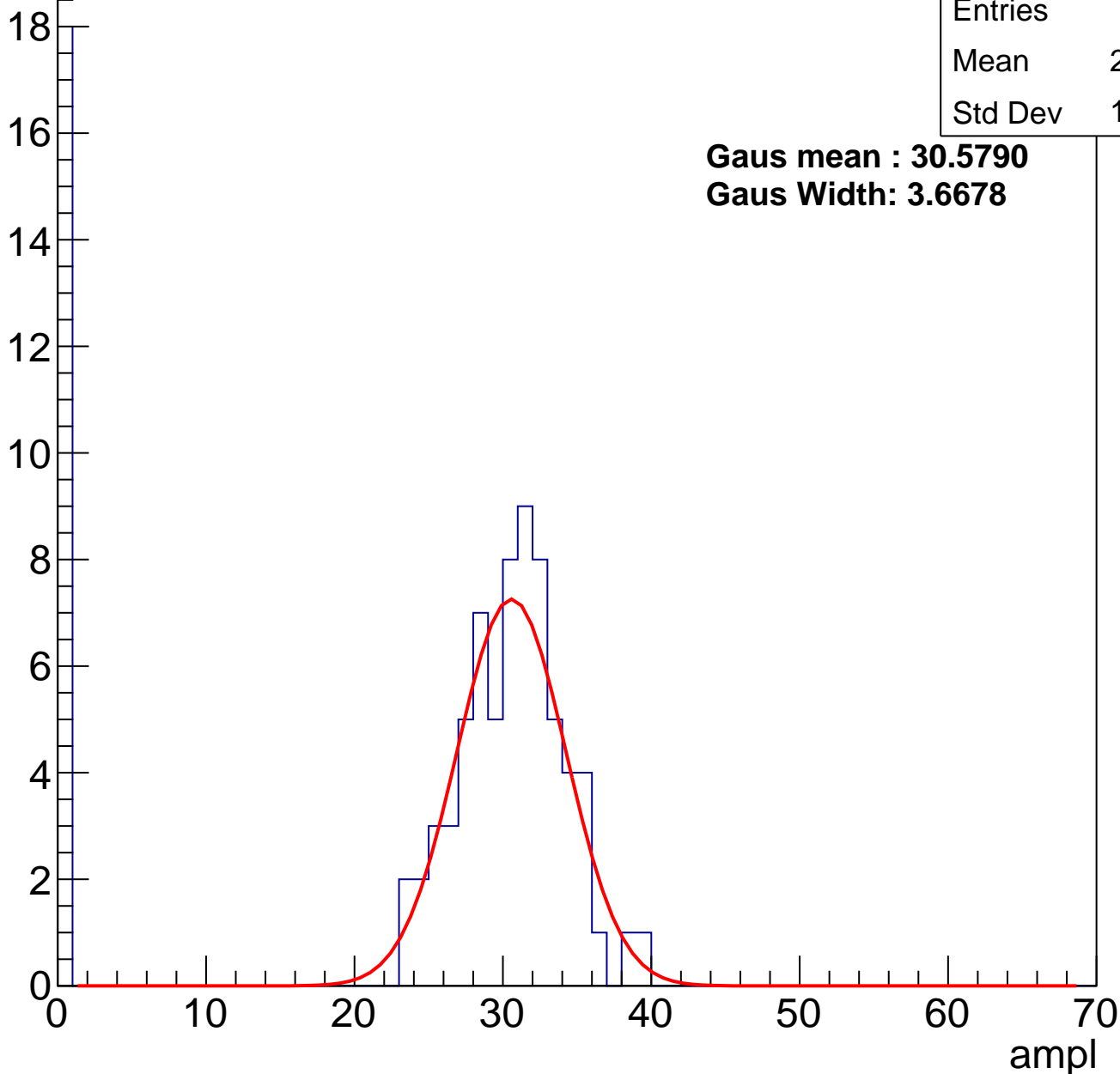
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	86
Mean	23.86
Std Dev	12.65

**Gaus mean : 30.5790**

**Gaus Width: 3.6678**

Entry



# B1L103S, U3-ch118, adc1

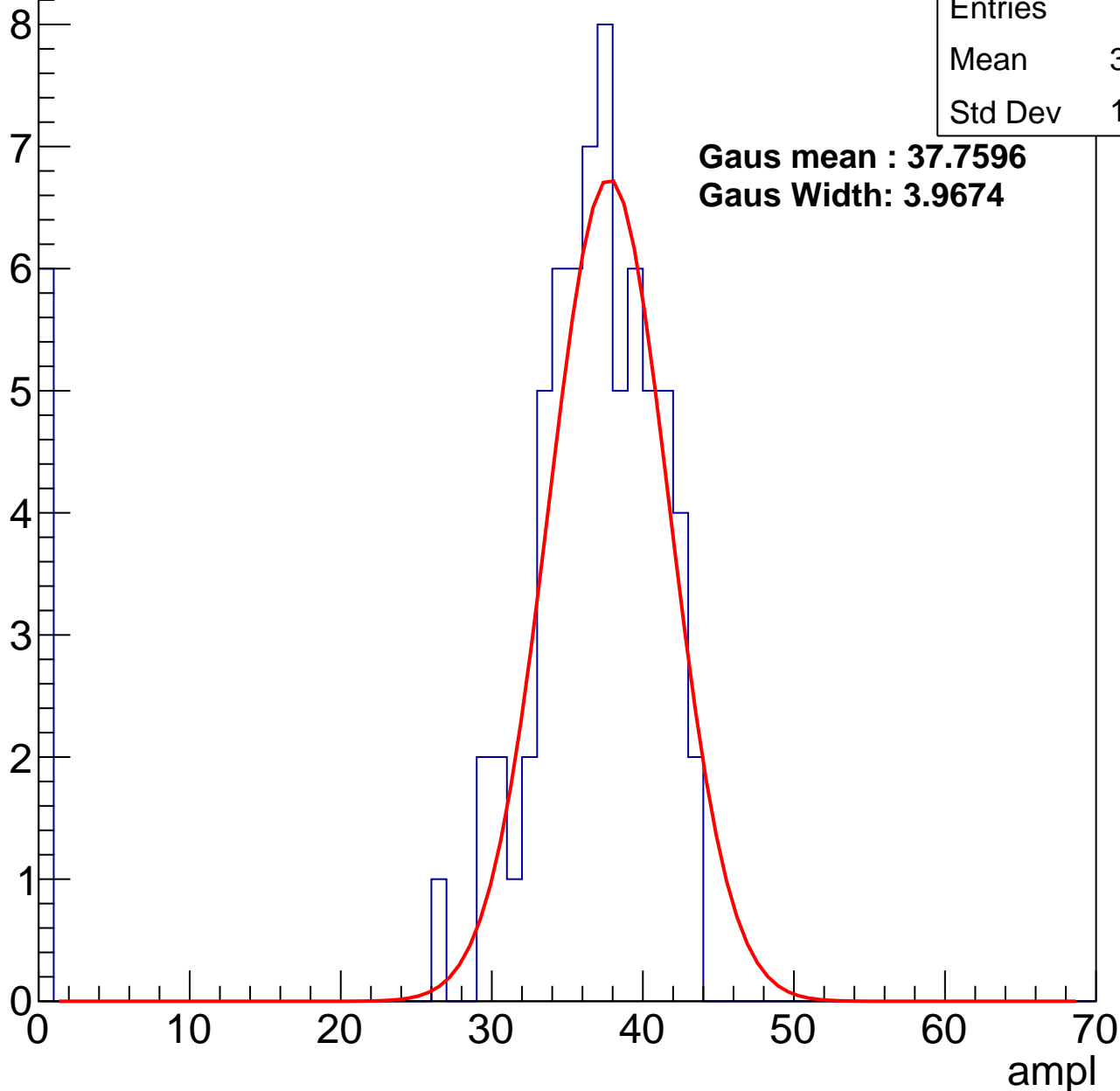
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	33.55
Std Dev	10.64

**Gaus mean : 37.7596**

**Gaus Width: 3.9674**

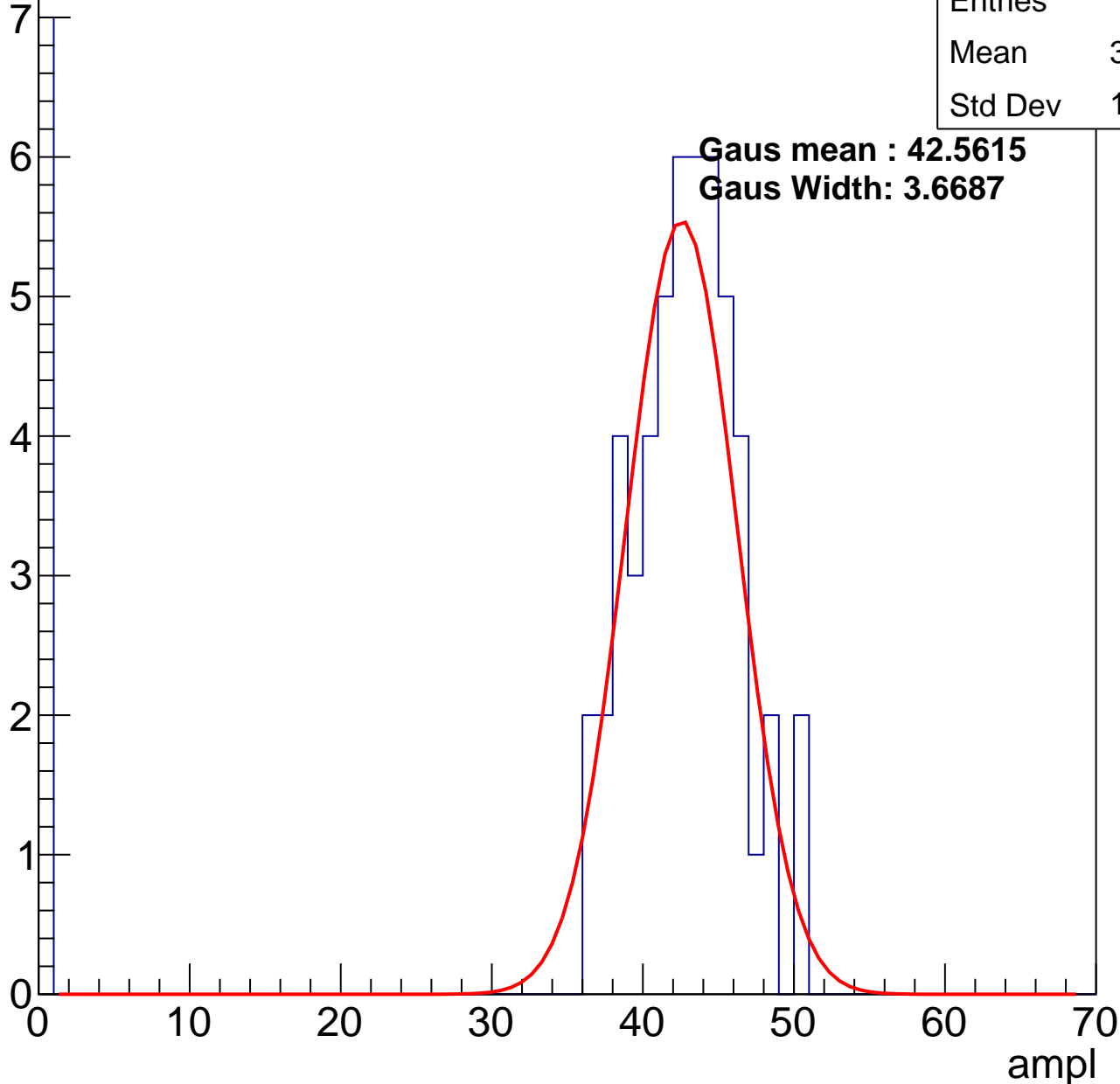


# B1L103S, U3-ch118, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	37.39
Std Dev	14.08

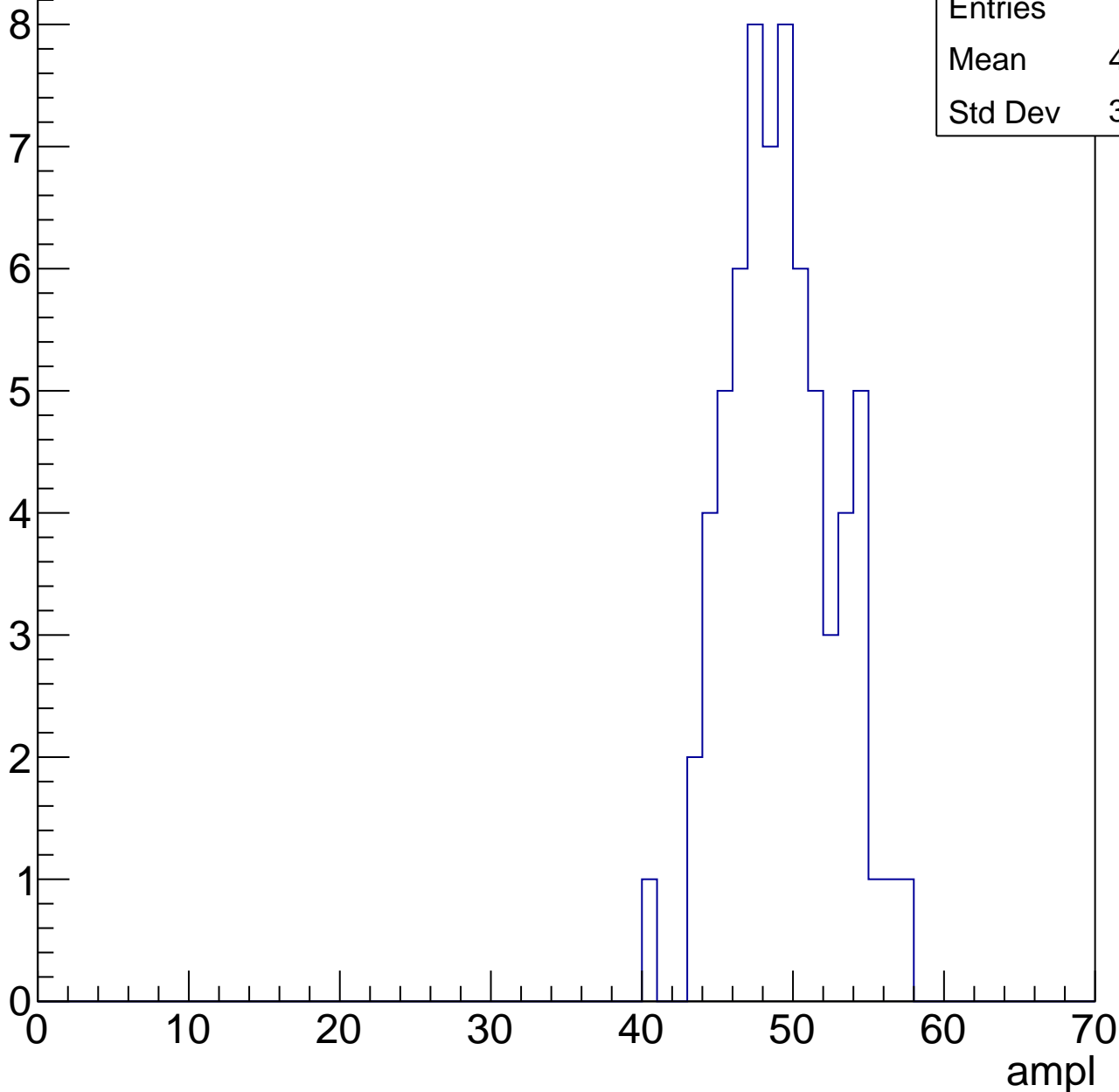


# B1L103S, U3-ch118, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

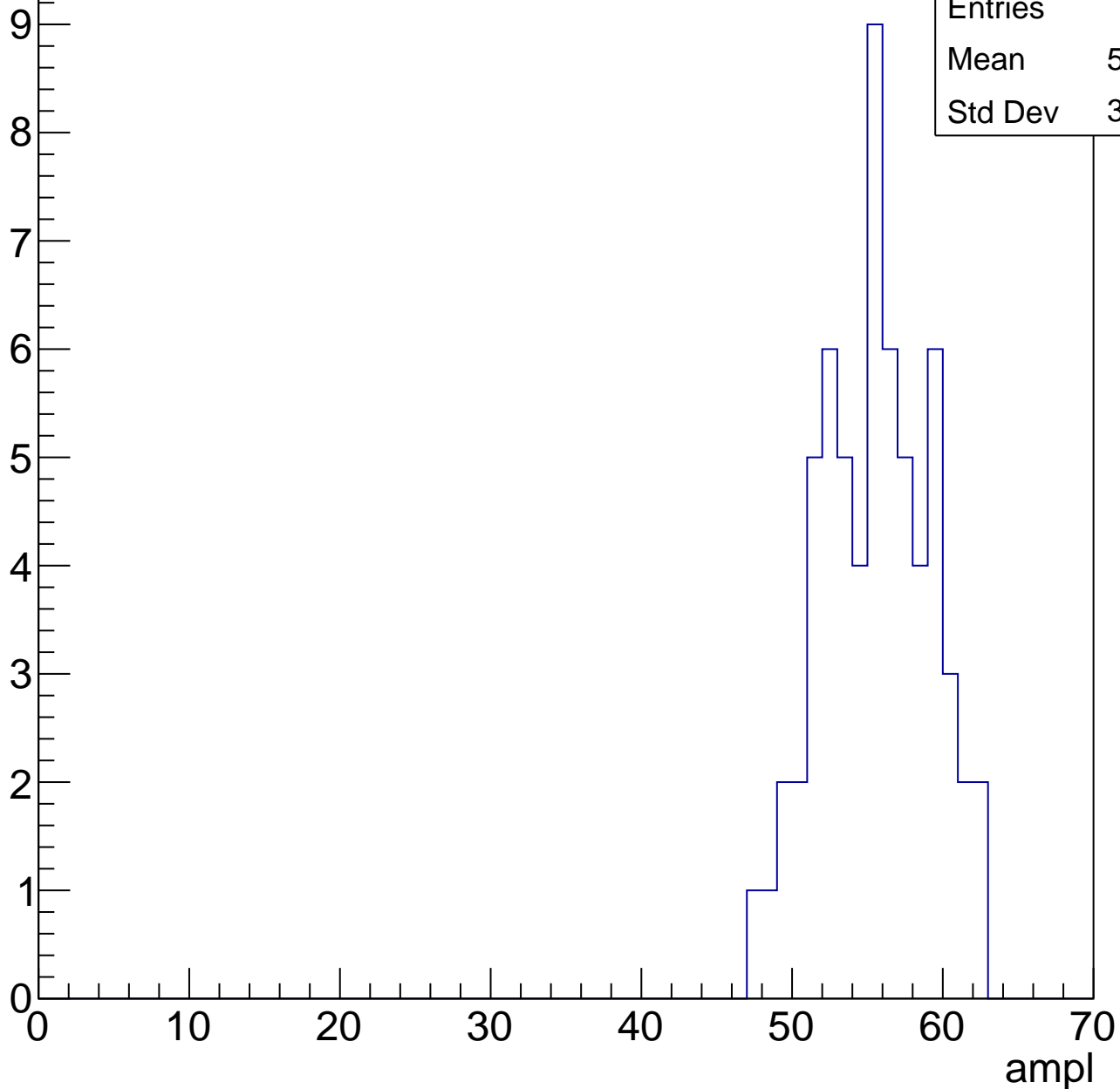
Entries	67
Mean	48.78
Std Dev	3.485



# B1L103S, U3-ch118, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

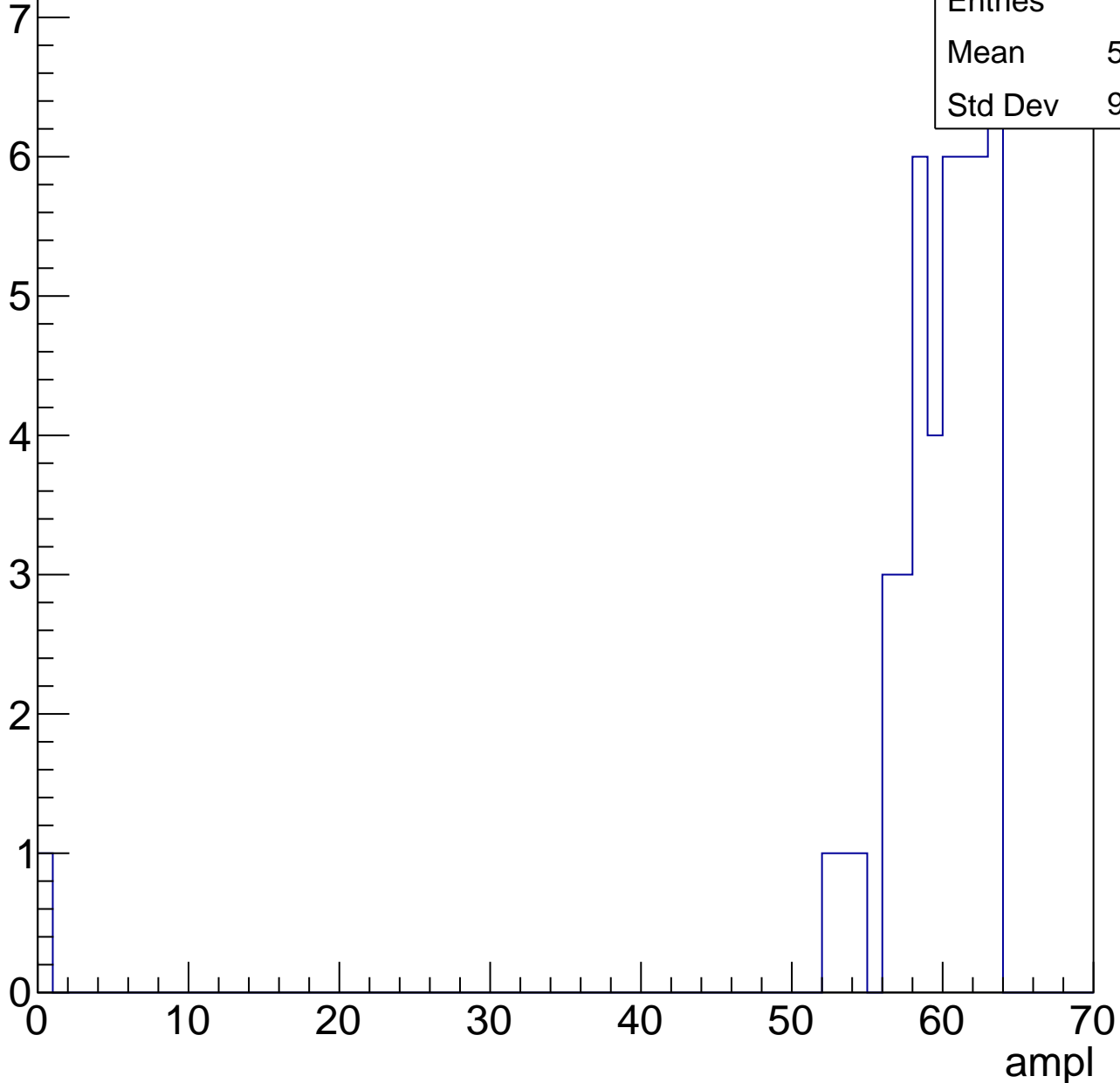


# B1L103S, U3-ch118, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

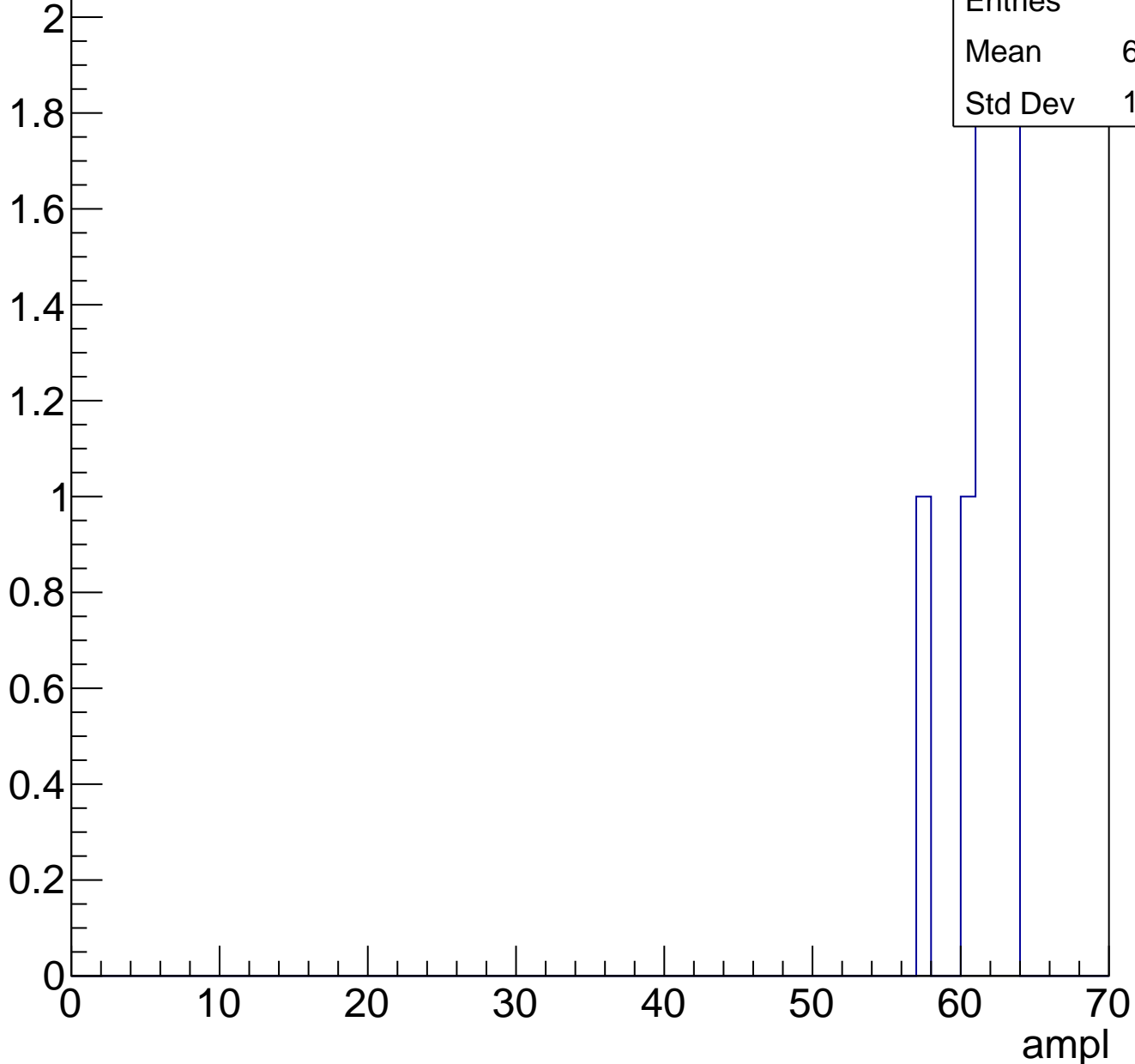
Entries	45
Mean	58.24
Std Dev	9.197



# B1L103S, U3-ch118, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	8
Mean	61.12
Std Dev	1.833

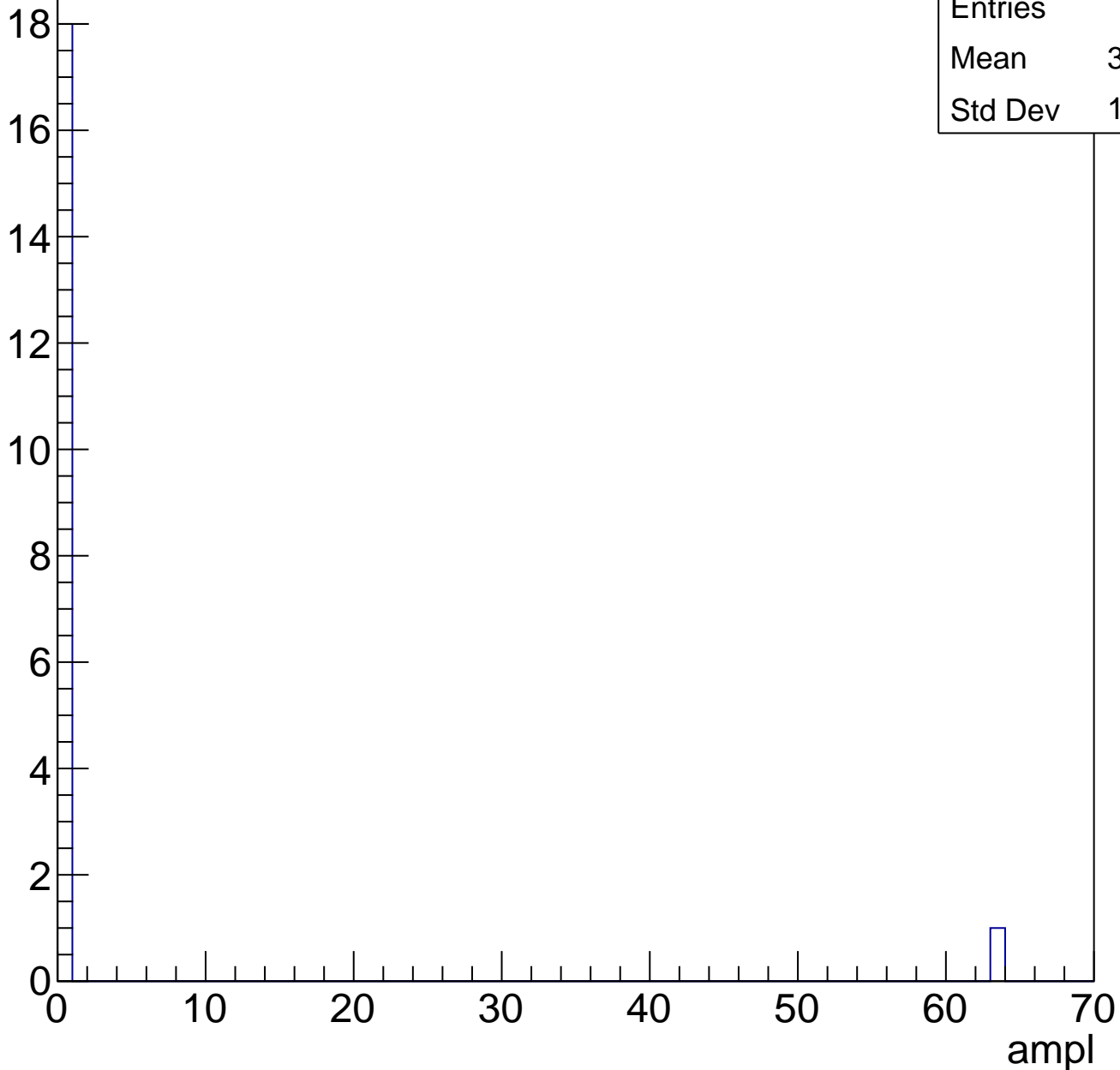


# B1L103S, U3-ch118, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	3.316
Std Dev	14.07

Entry



# B1L103S, U3-ch119, adc0

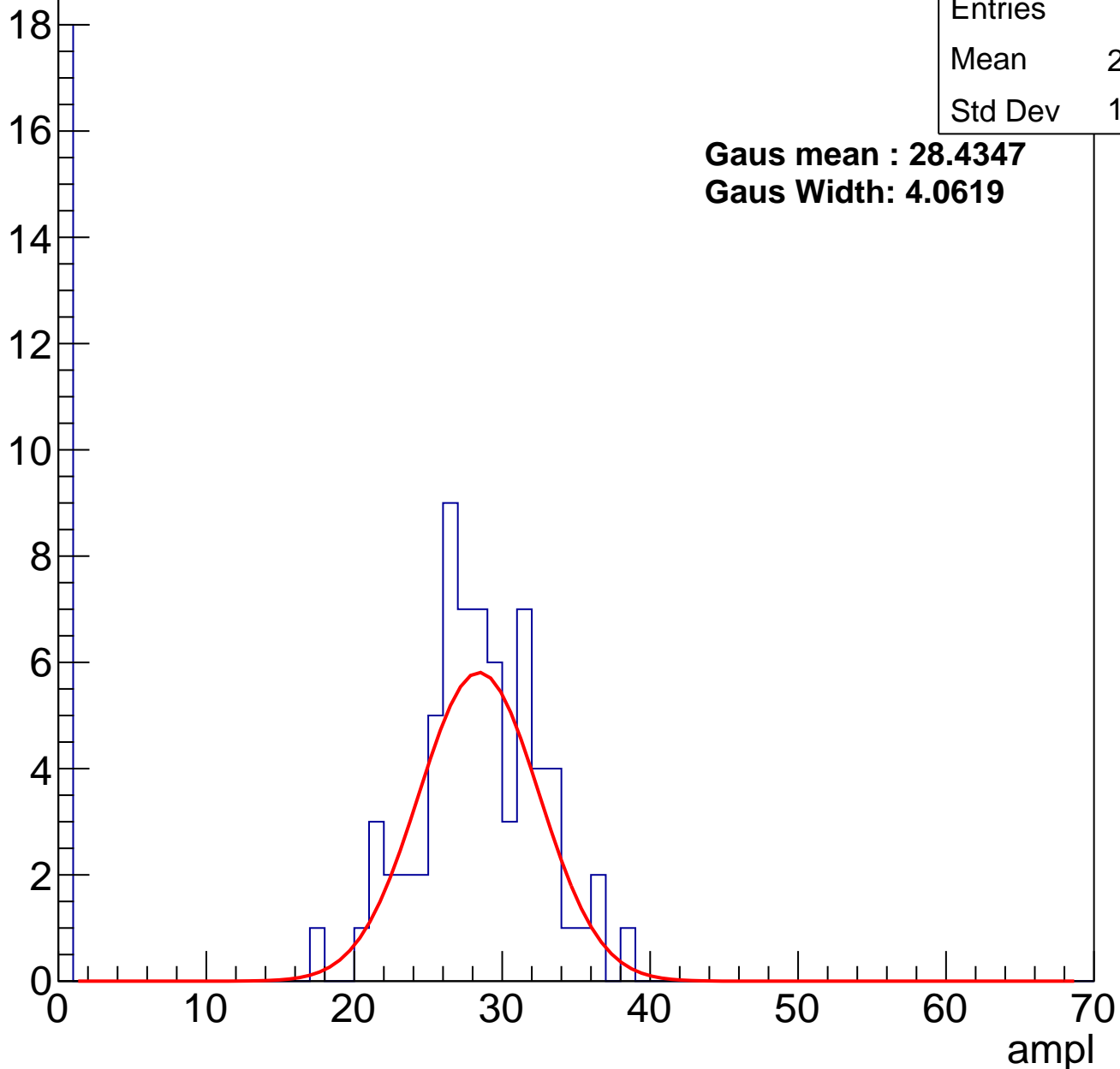
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	86
Mean	22.12
Std Dev	11.94

**Gaus mean : 28.4347**

**Gaus Width: 4.0619**

Entry



# B1L103S, U3-ch119, adc1

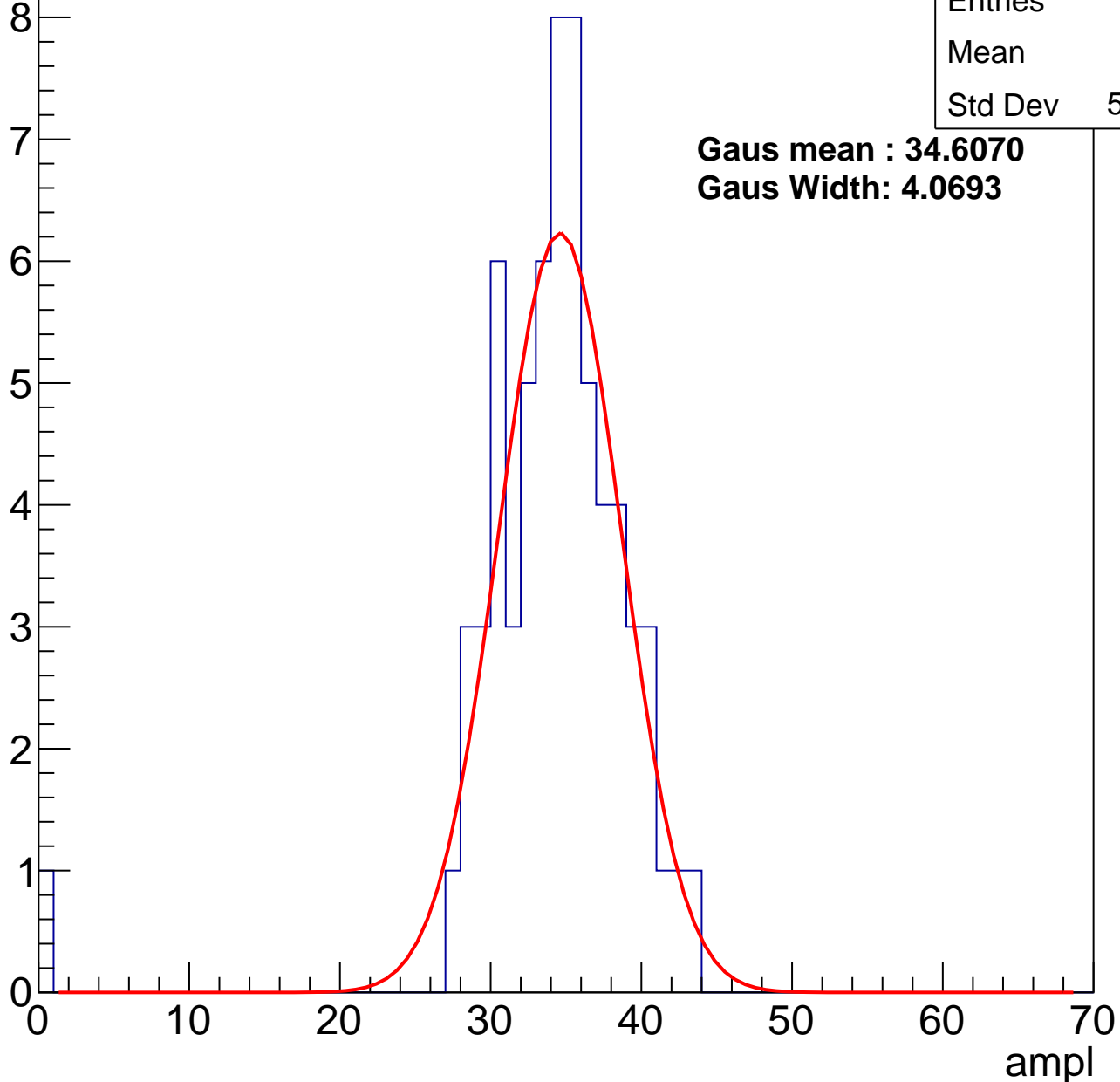
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	66
Mean	33.7
Std Dev	5.554

**Gaus mean : 34.6070**

**Gaus Width: 4.0693**



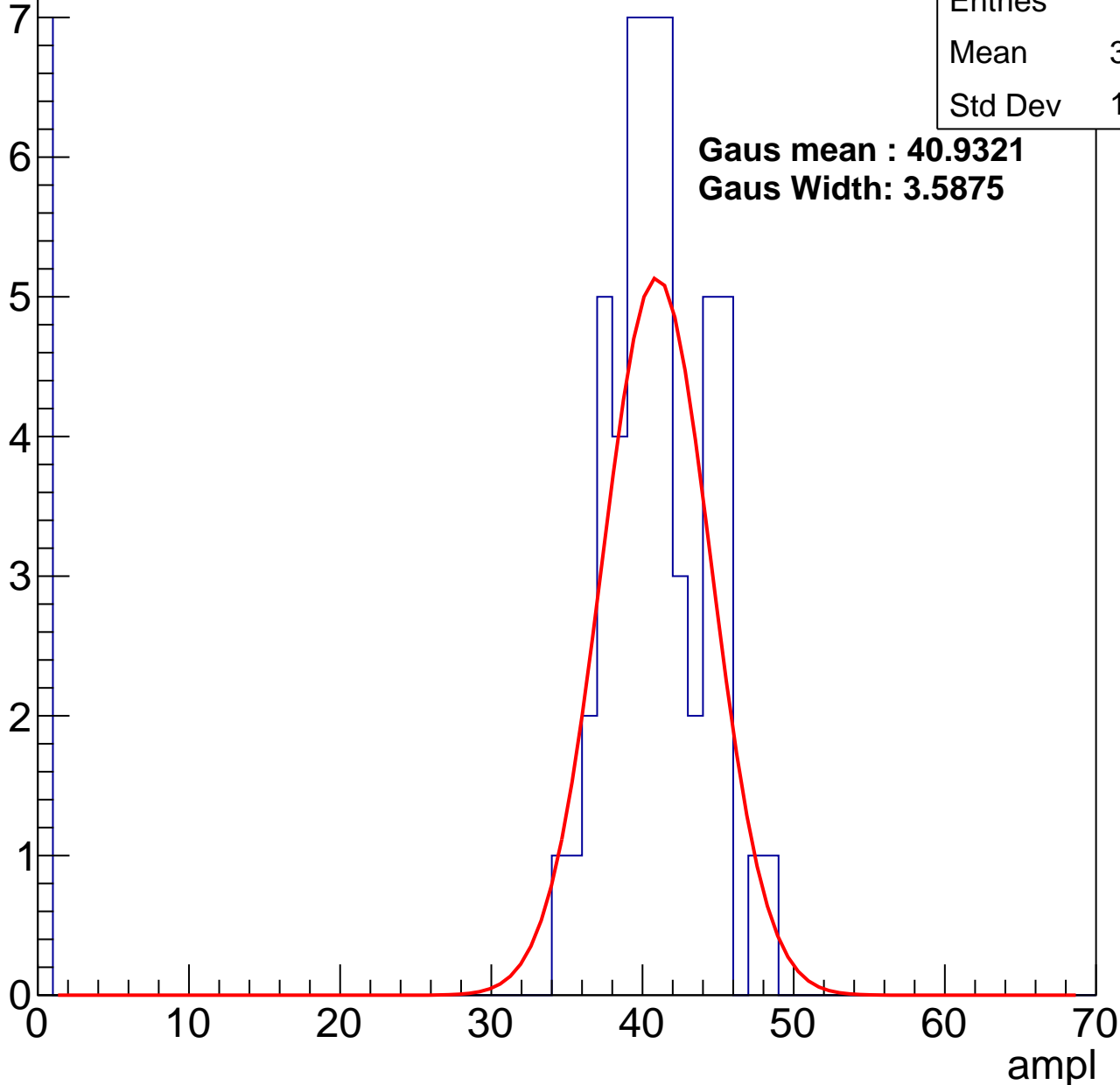
# B1L103S, U3-ch119, adc2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	58
Mean	35.69
Std Dev	13.54

**Gaus mean : 40.9321**  
**Gaus Width: 3.5875**



# B1L103S, U3-ch119, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	93
Mean	41.59
Std Dev	15.75

Entry

10

8

6

4

2

0

0

10

20

30

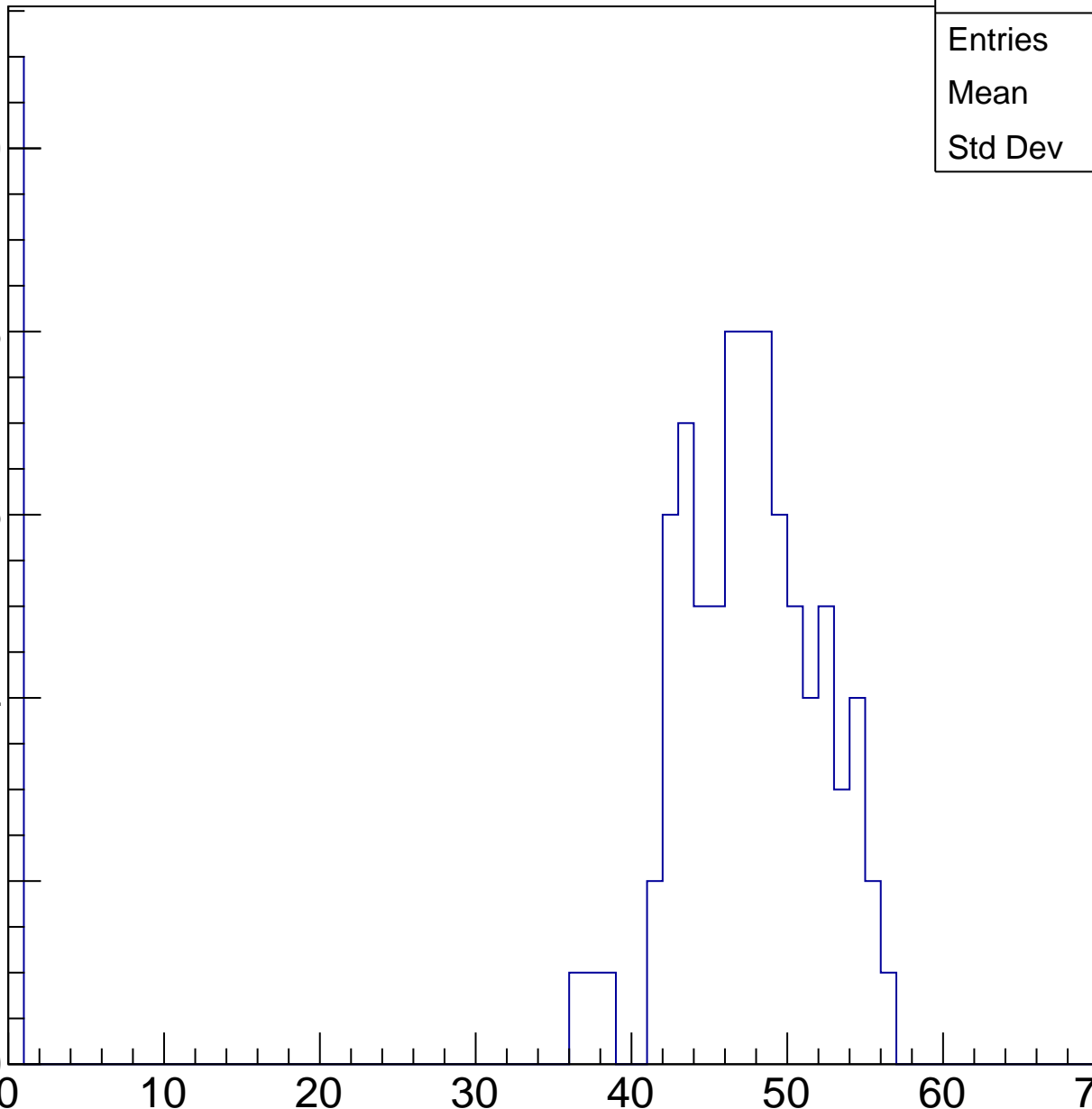
40

50

60

70

ampl



# B1L103S, U3-ch119, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

6

5

4

3

2

1

0

Entries	53
Mean	53.3
Std Dev	3.59

ampl

0

10

20

30

40

50

60

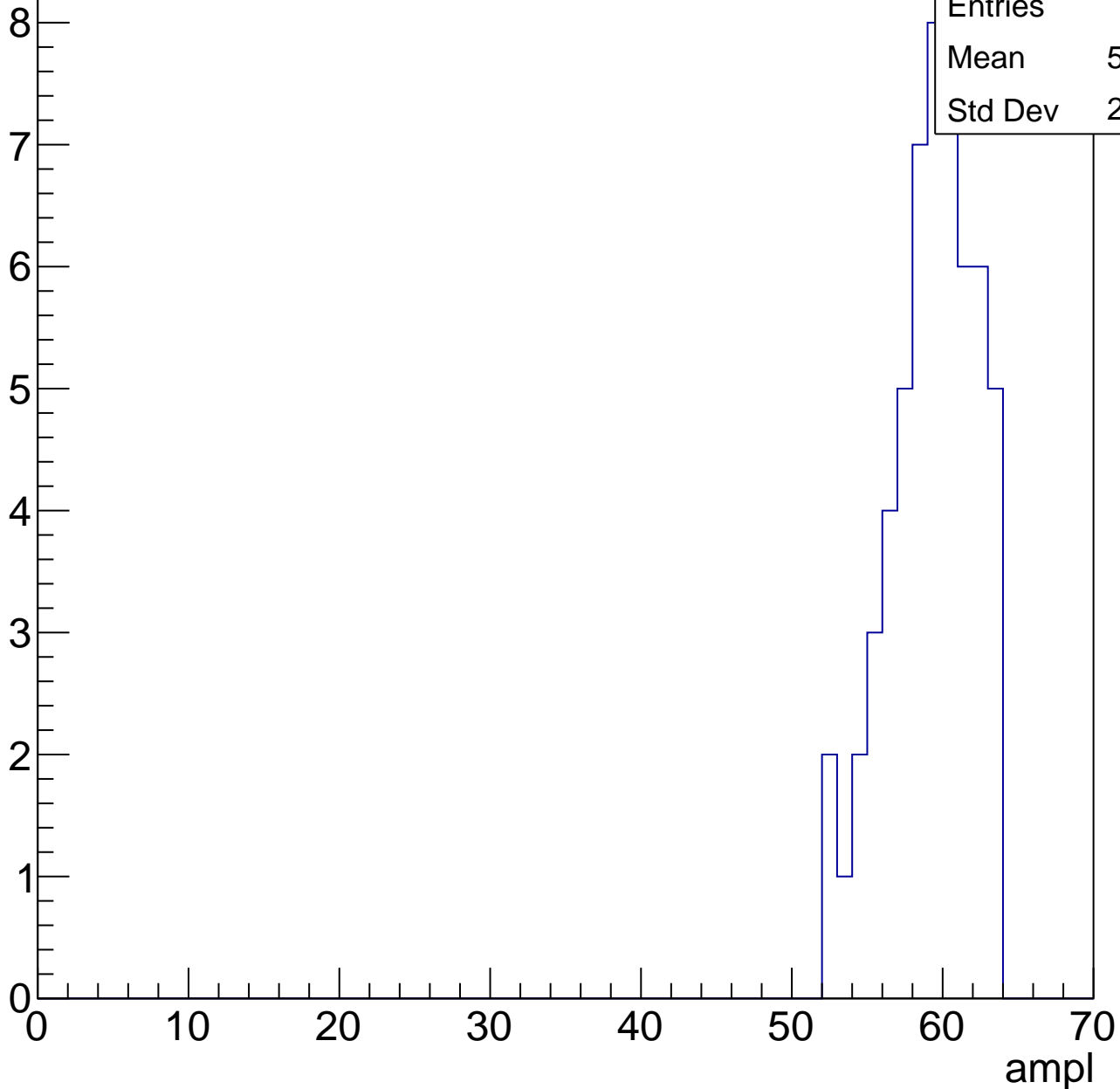
70

# B1L103S, U3-ch119, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

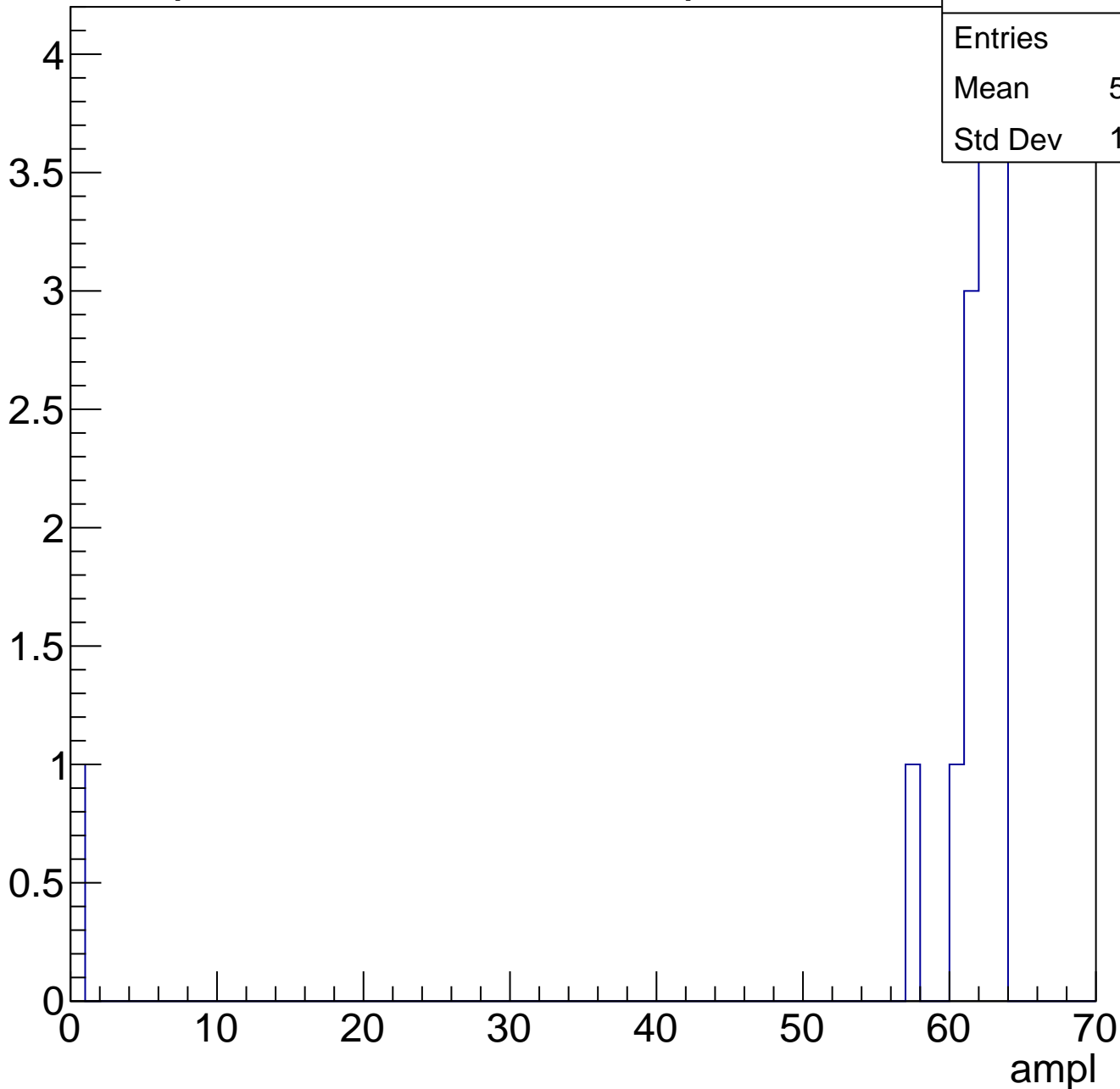
Entries	57
Mean	58.77
Std Dev	2.835



# B1L103S, U3-ch119, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U3-ch119, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry



# B1L103S, U3-ch120, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	98
Mean	24.04
Std Dev	8.15

**Gaus mean : 26.6223**

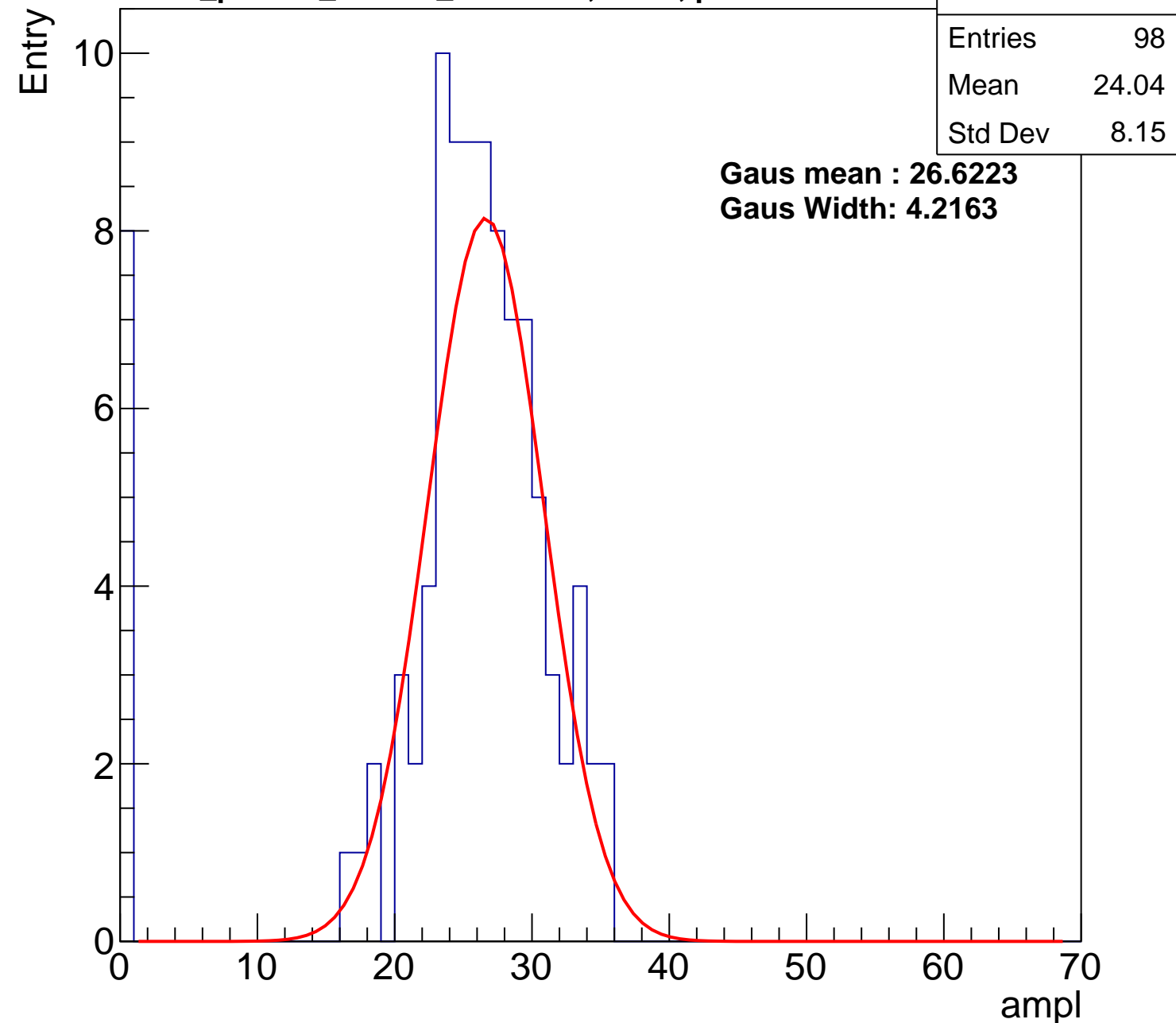
**Gaus Width: 4.2163**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch120, adc1

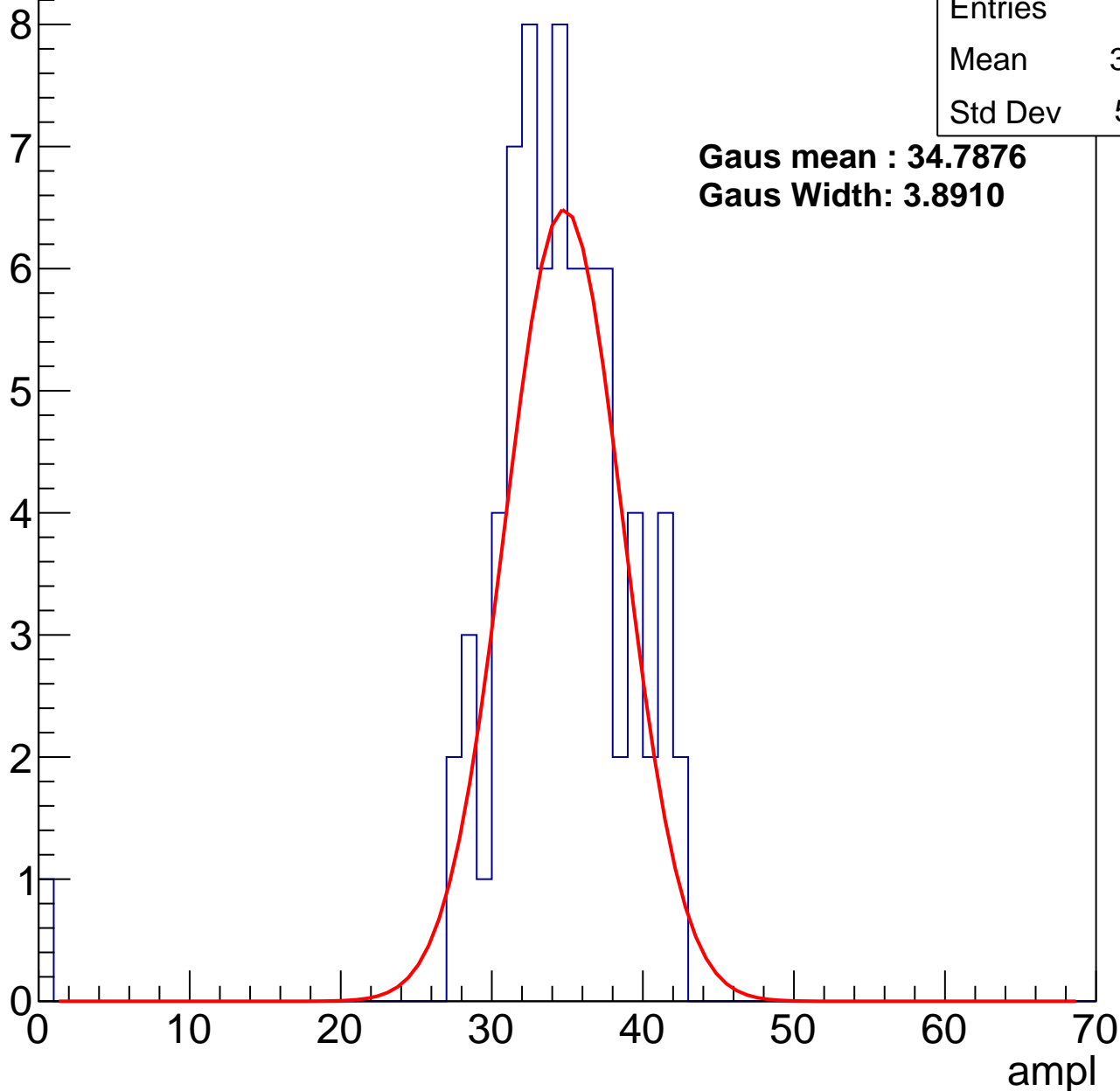
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	72
Mean	33.86
Std Dev	5.481

**Gaus mean : 34.7876**

**Gaus Width: 3.8910**



# B1L103S, U3-ch120, adc2

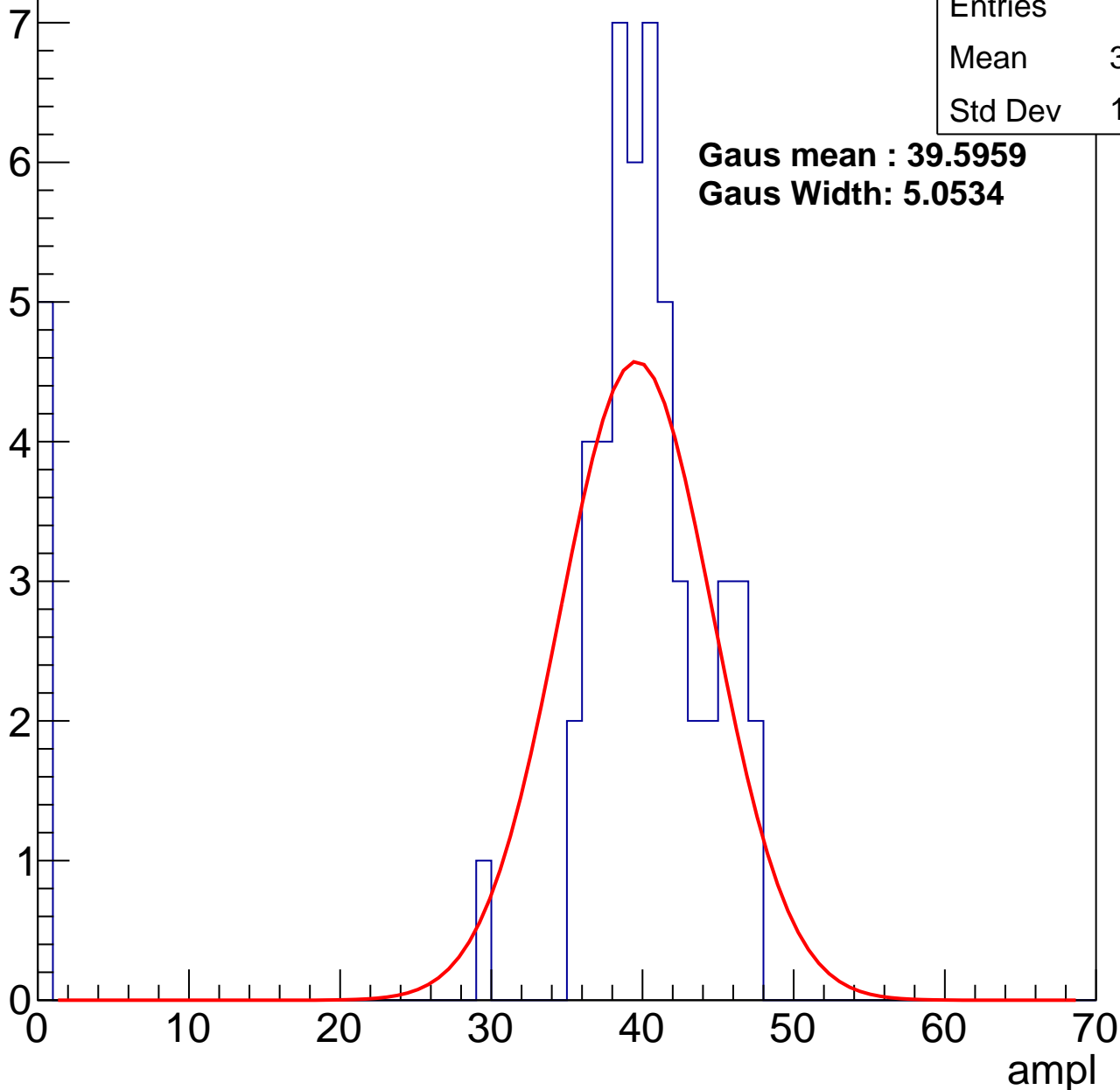
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	56
Mean	36.48
Std Dev	11.92

**Gaus mean : 39.5959**

**Gaus Width: 5.0534**

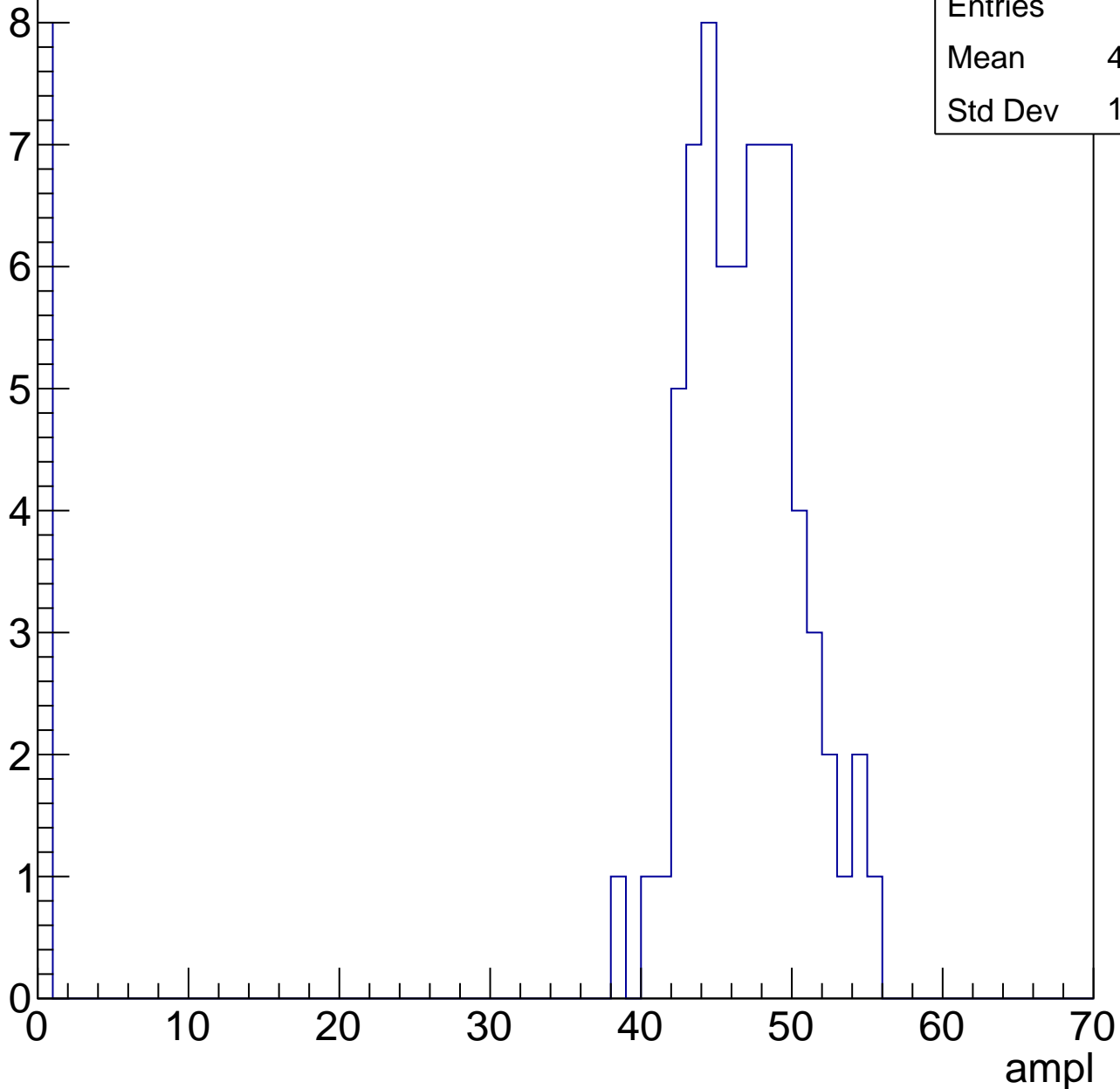


# B1L103S, U3-ch120, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	77
Mean	41.68
Std Dev	14.58

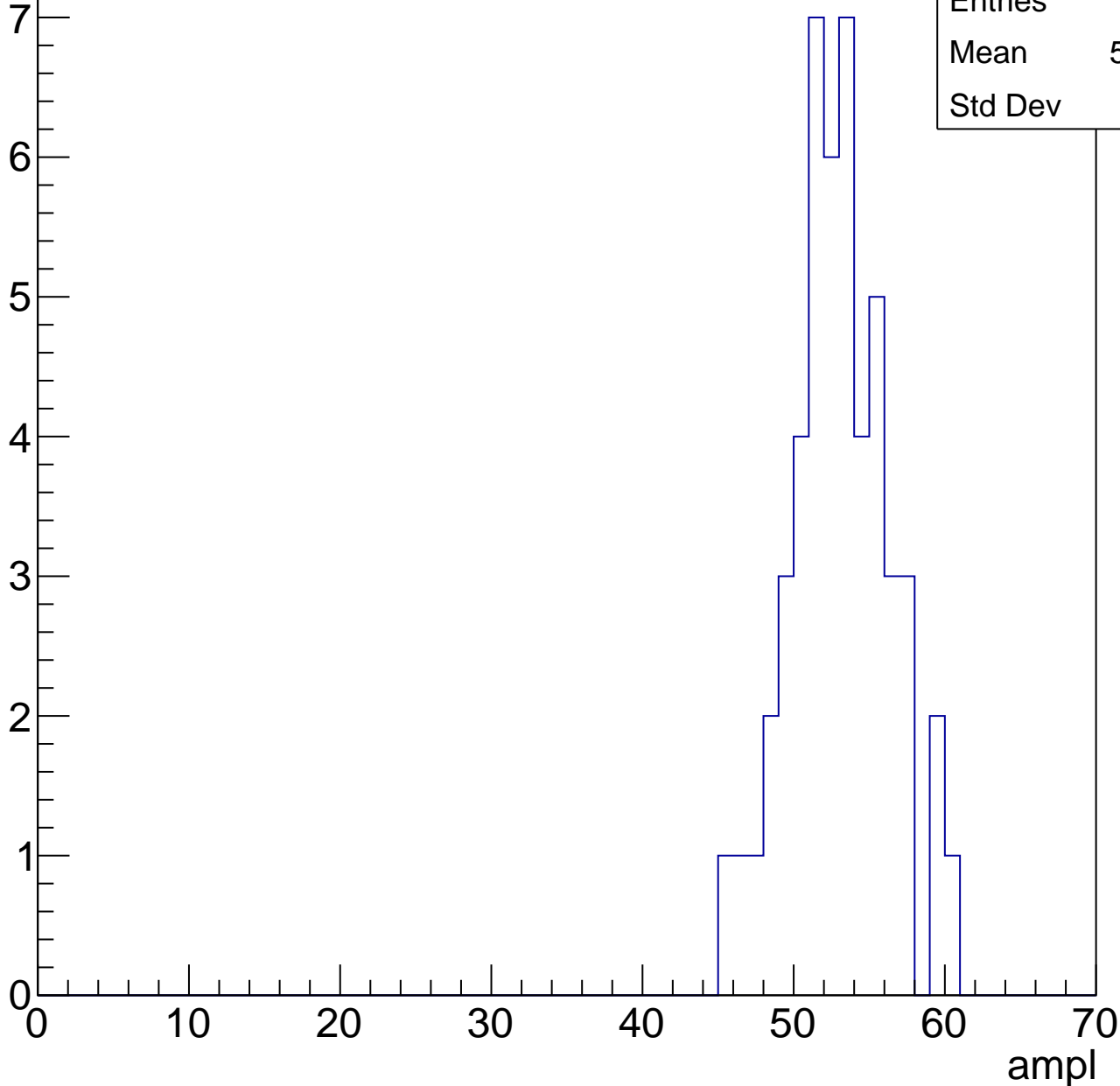


# B1L103S, U3-ch120, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	50
Mean	52.58
Std Dev	3.25

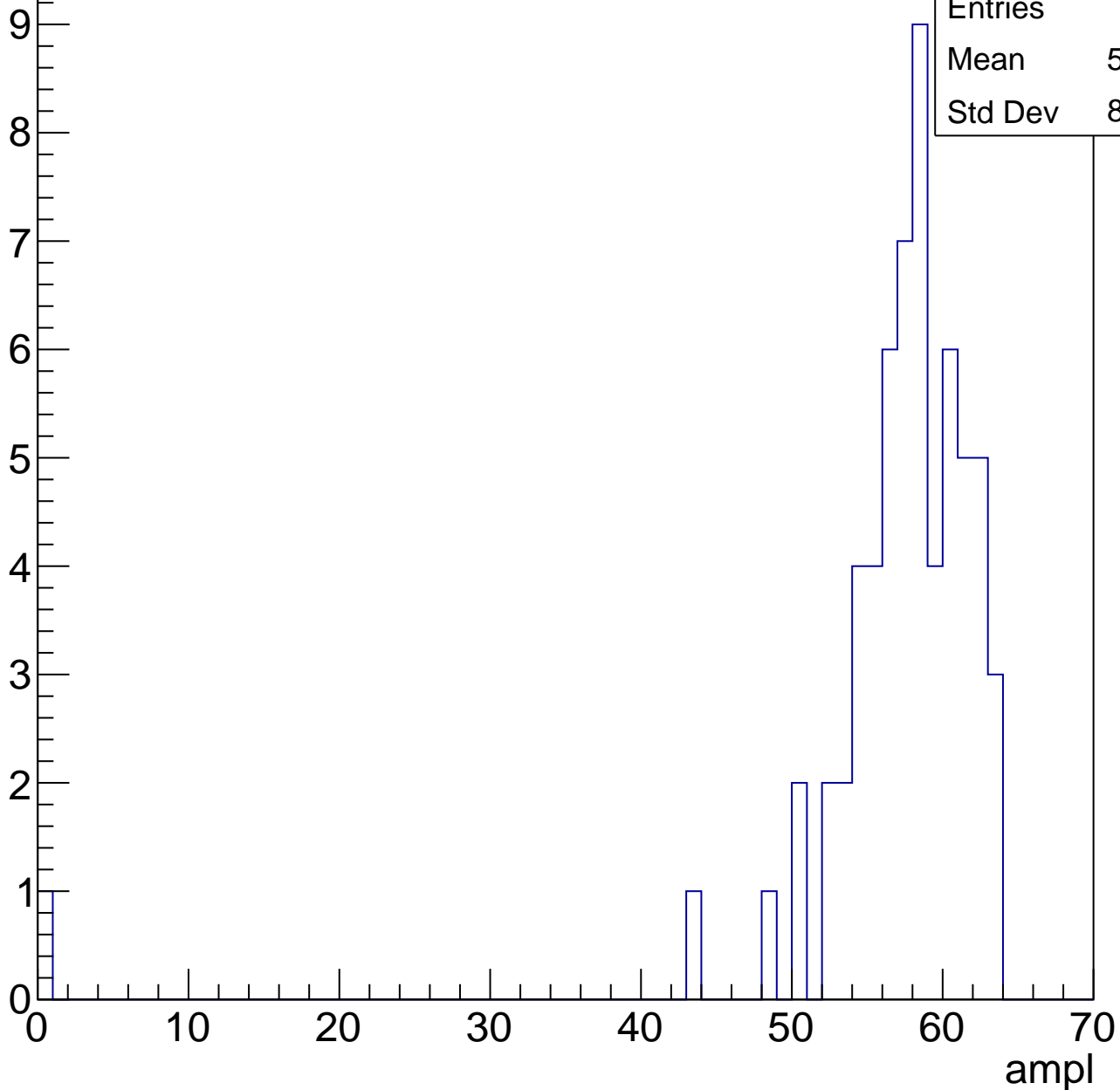


# B1L103S, U3-ch120, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	56.35
Std Dev	8.162

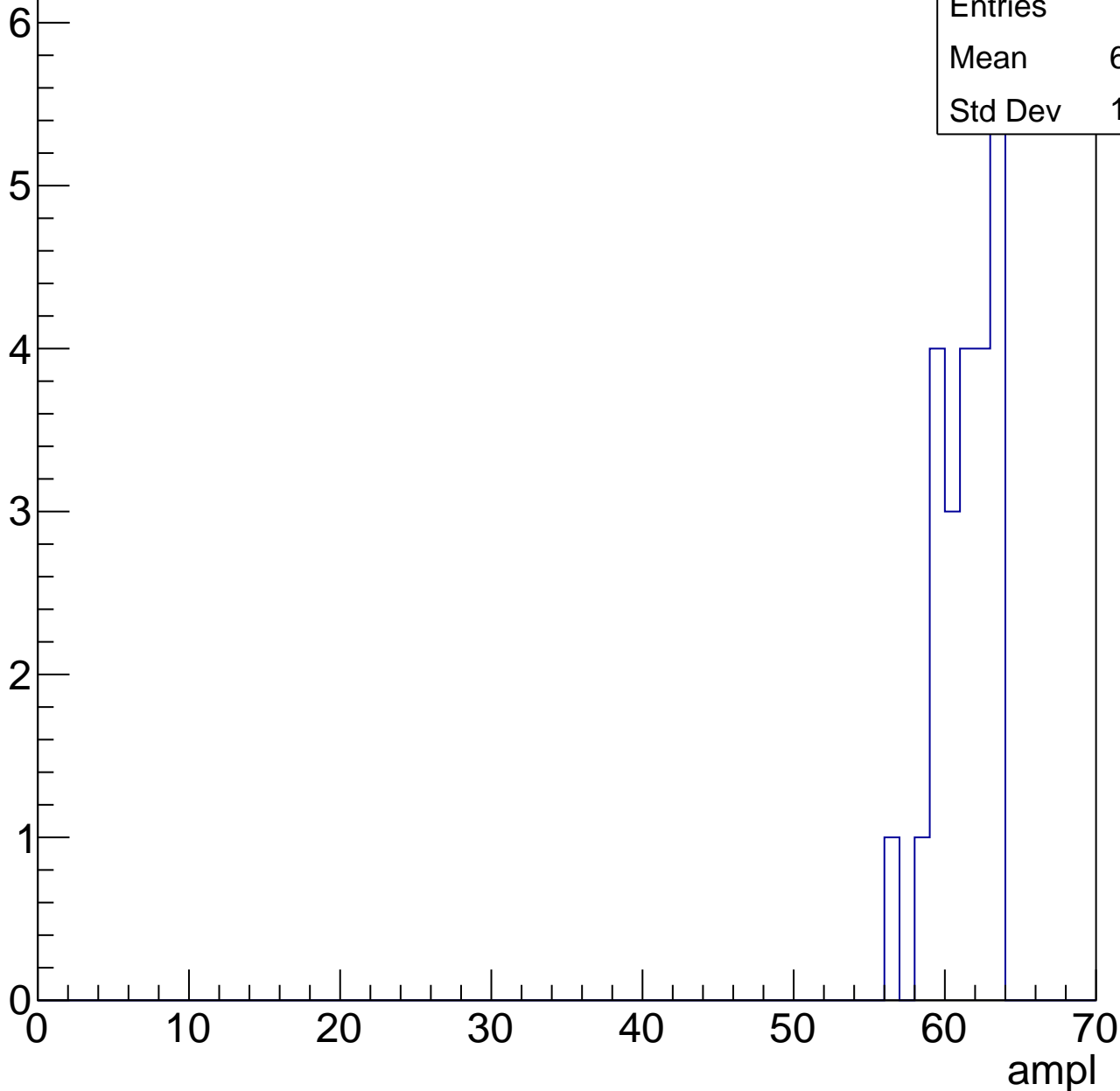


# B1L103S, U3-ch120, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	23
Mean	60.87
Std Dev	1.872



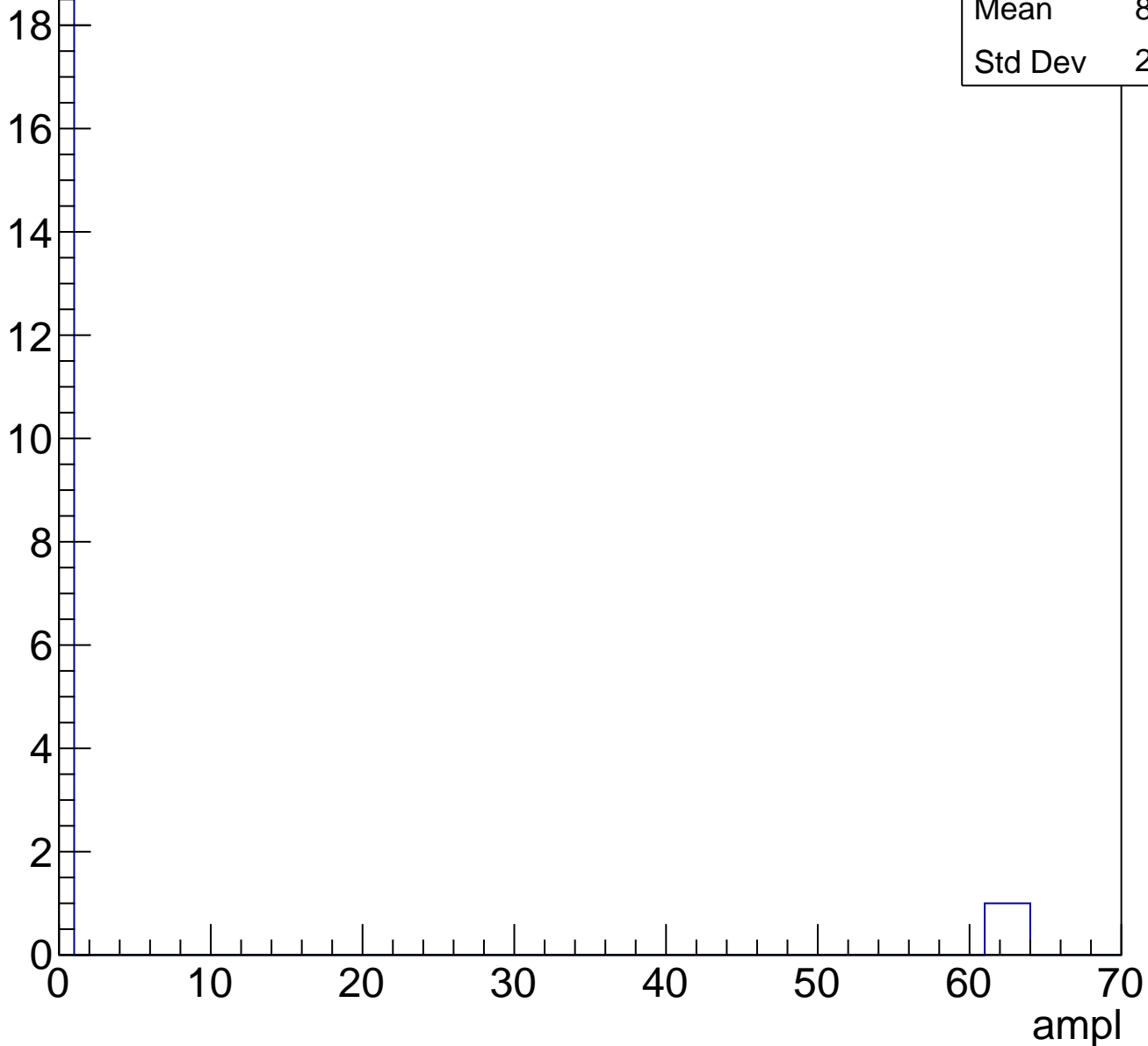


# B1L103S, U3-ch120, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	22
Mean	8.455
Std Dev	21.28

Entry



# B1L103S, U3-ch121, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	83
Mean	19.6
Std Dev	13.92

**Gaus mean : 29.7042**

**Gaus Width: 4.0997**

Entry

25

20

15

10

5

0

0

10

20

30

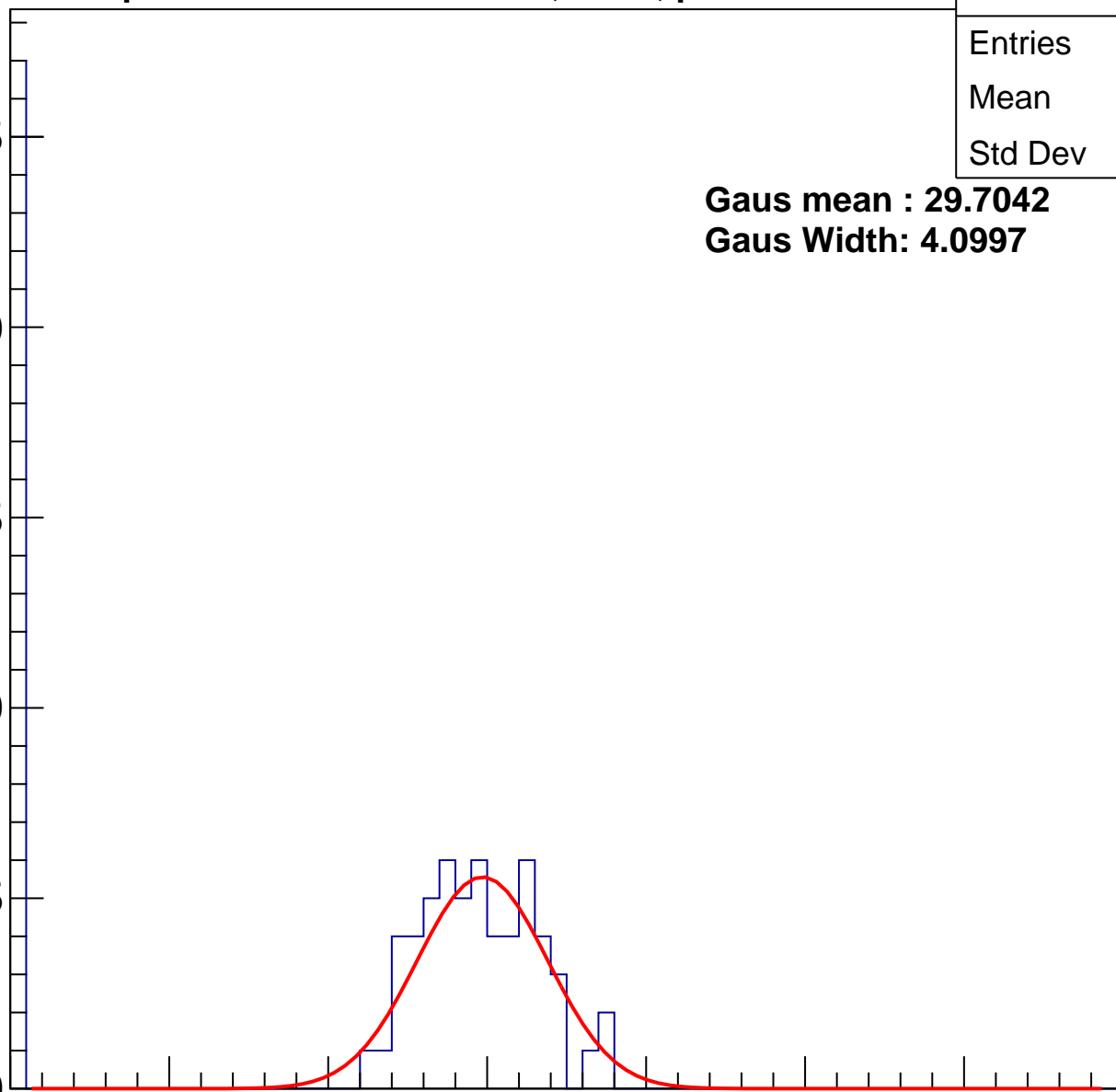
40

50

60

70

ampl



# B1L103S, U3-ch121, adc1

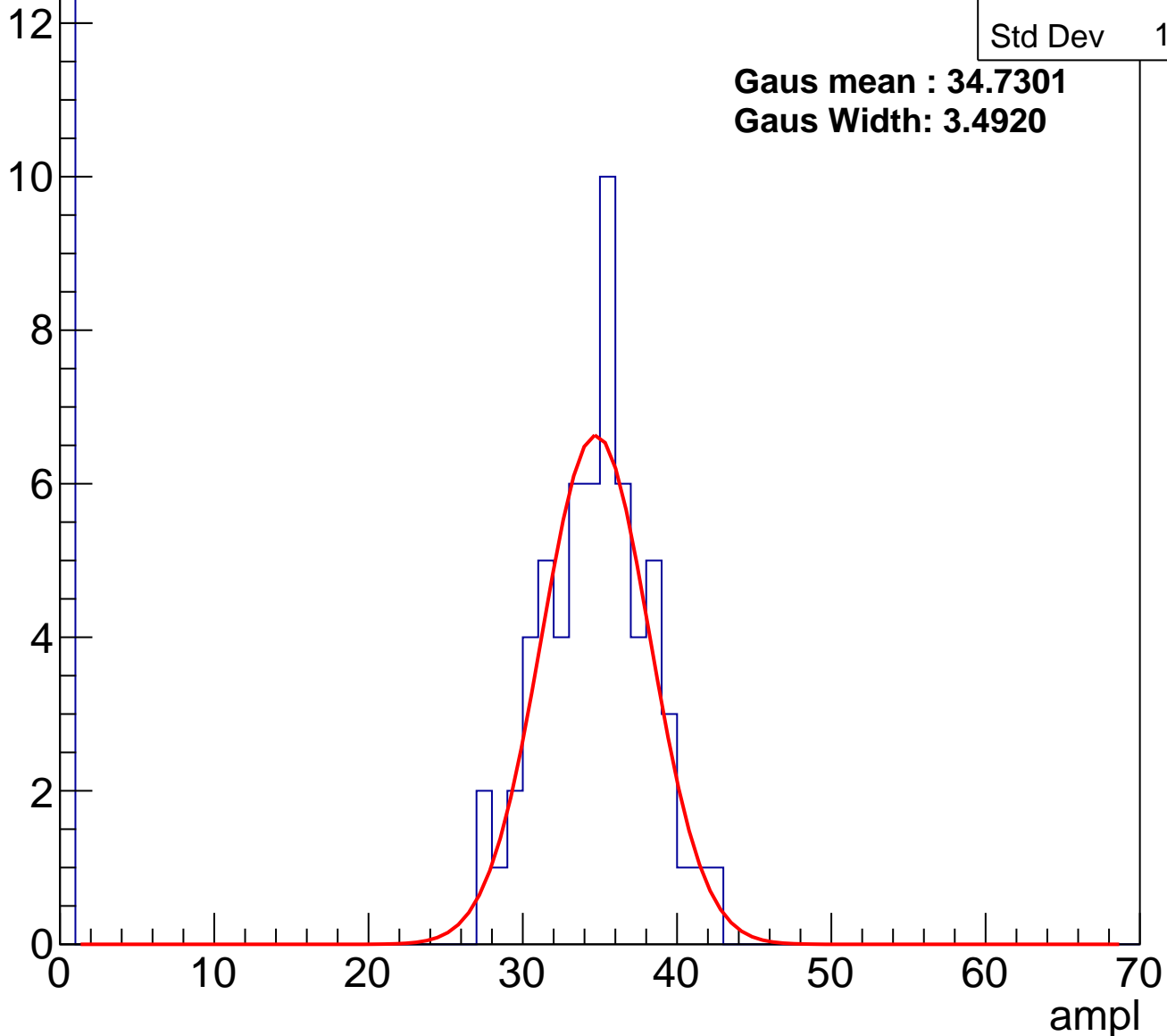
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	74
Mean	28.23
Std Dev	13.38

**Gaus mean : 34.7301**

**Gaus Width: 3.4920**



# B1L103S, U3-ch121, adc2

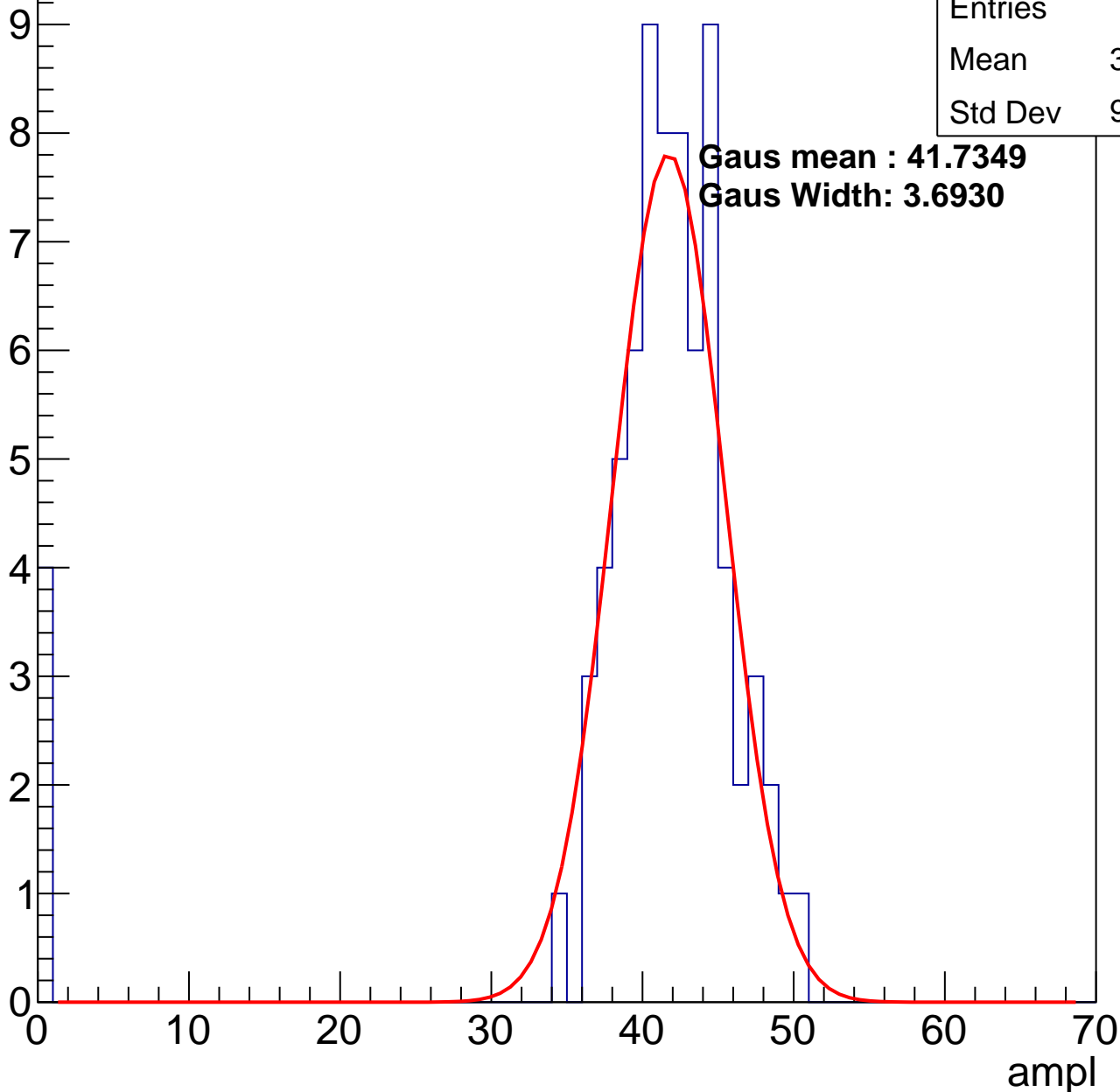
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	76
Mean	39.47
Std Dev	9.862

**Gaus mean : 41.7349**

**Gaus Width: 3.6930**

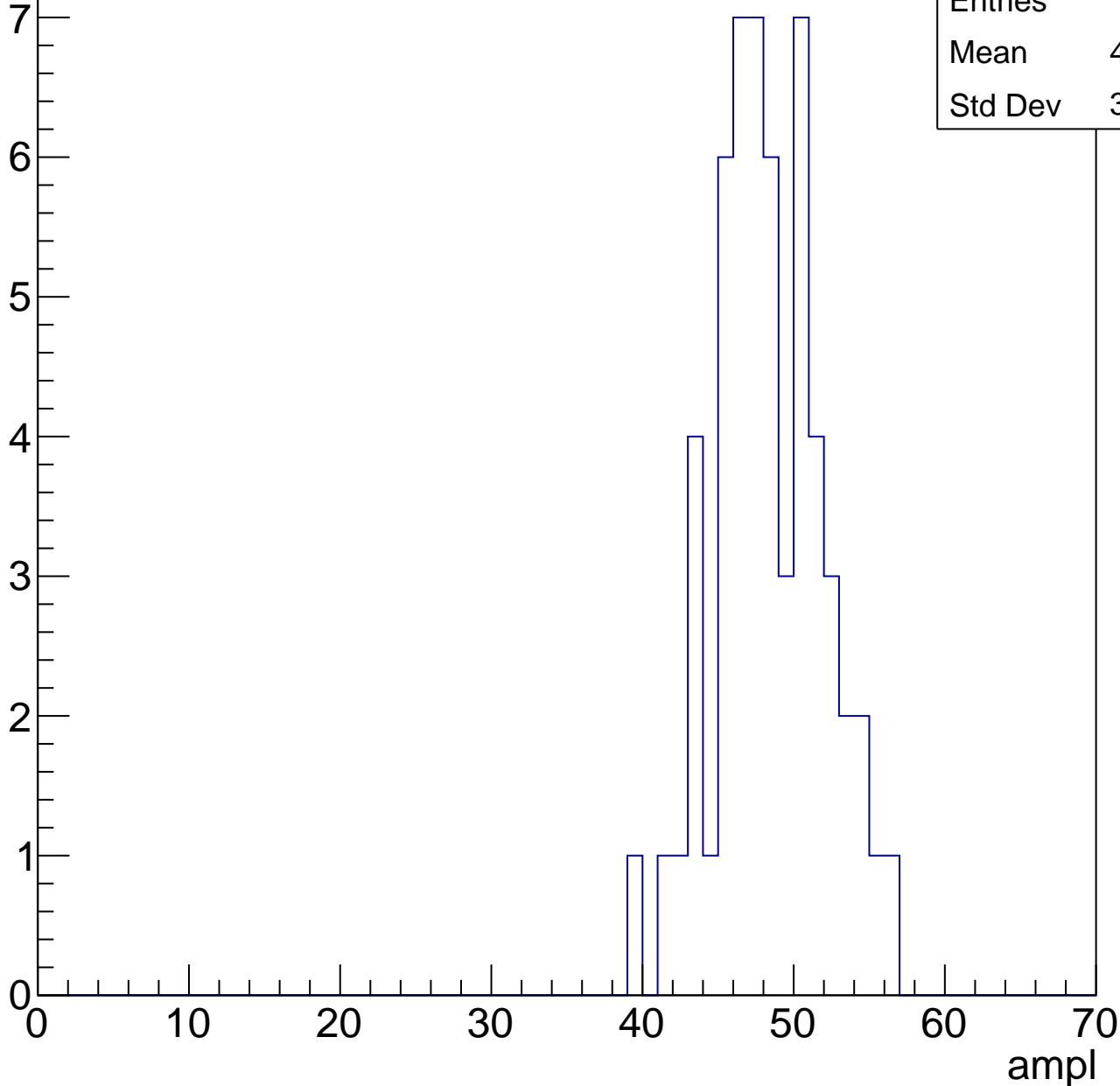


# B1L103S, U3-ch121, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	57
Mean	47.88
Std Dev	3.554

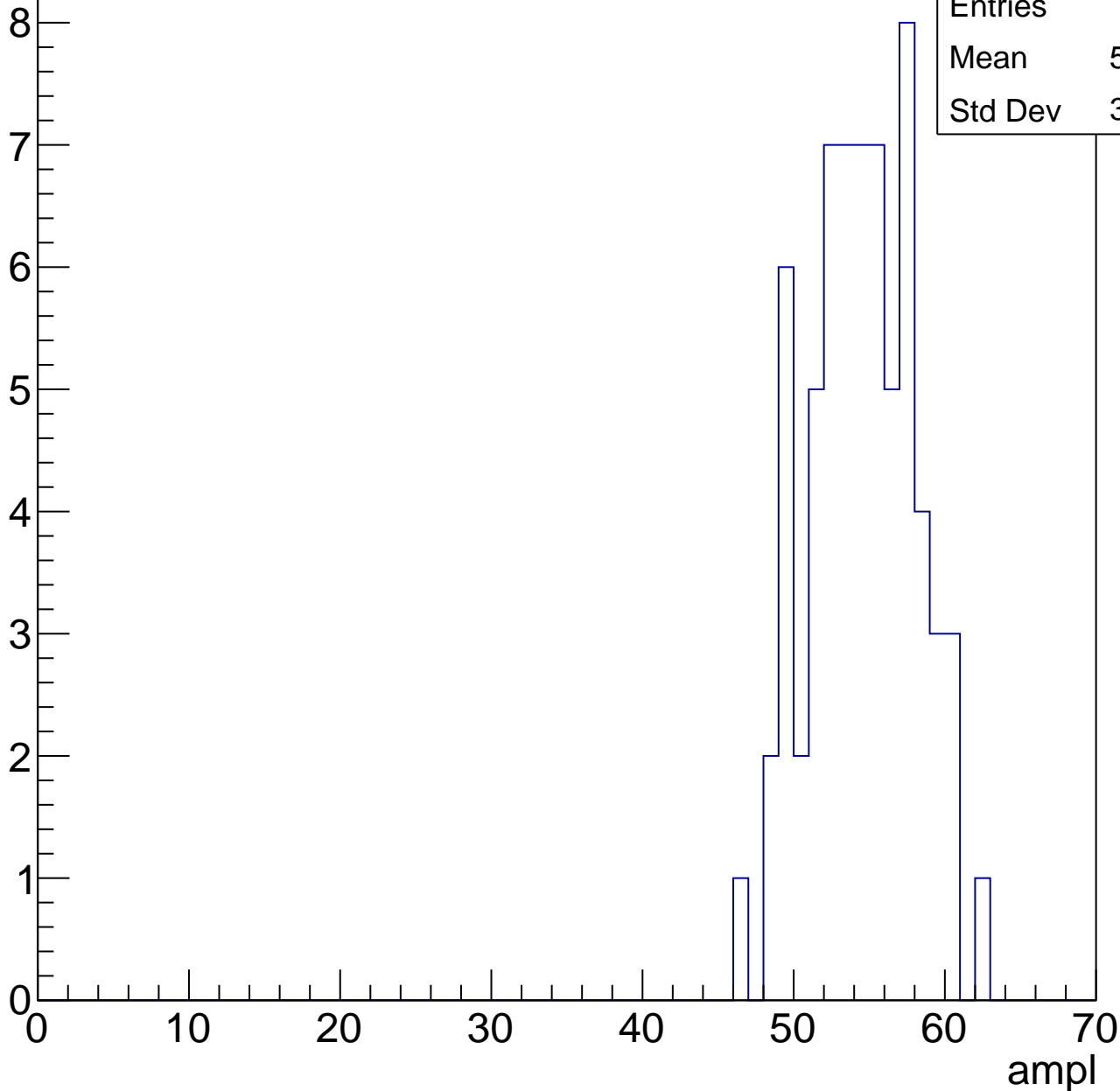


# B1L103S, U3-ch121, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	54.06
Std Dev	3.447

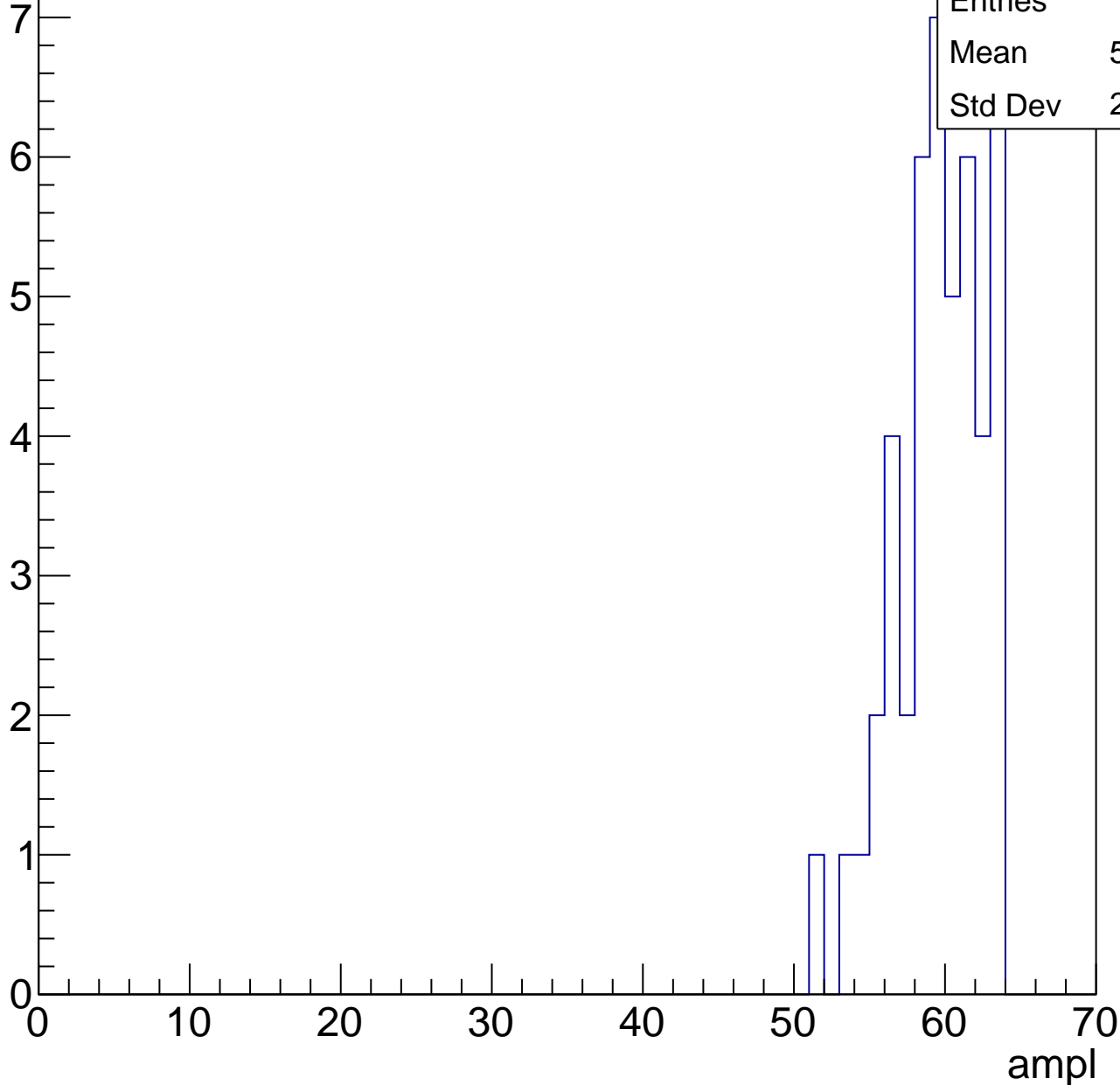


# B1L103S, U3-ch121, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	46
Mean	59.17
Std Dev	2.884

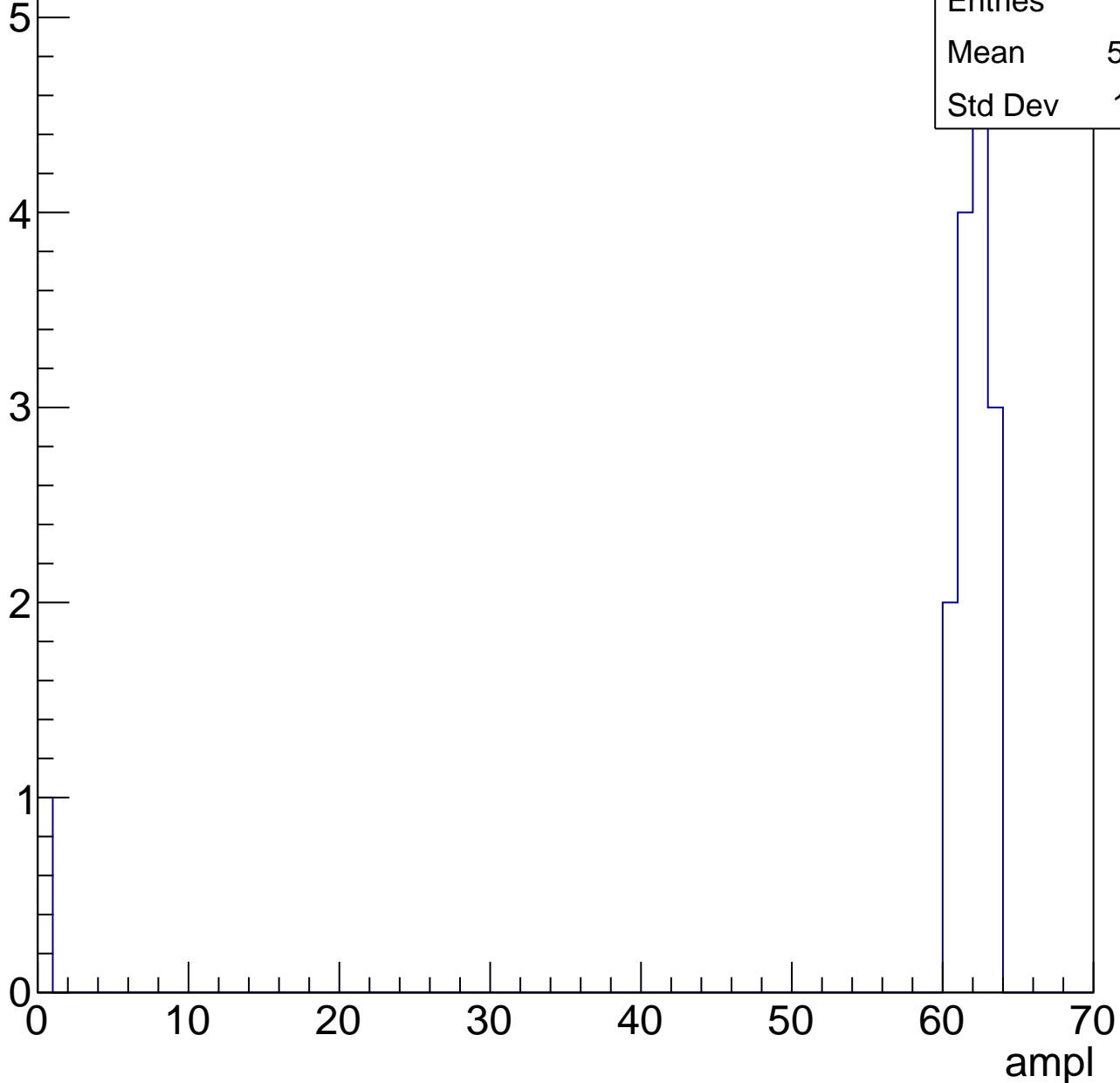


# B1L103S, U3-ch121, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	15
Mean	57.53
Std Dev	15.41



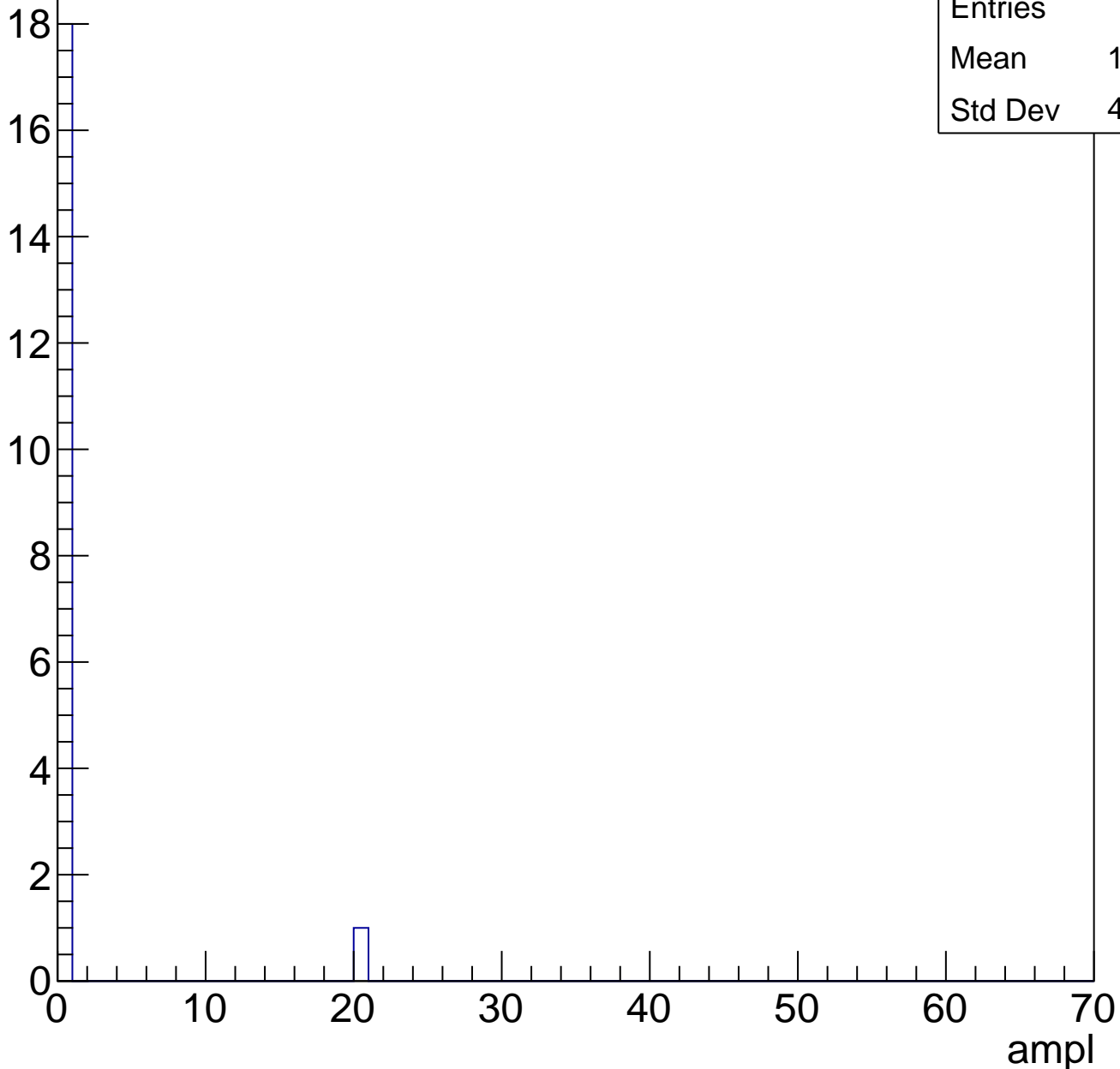


# B1L103S, U3-ch121, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	19
Mean	1.053
Std Dev	4.466

Entry



# B1L103S, U3-ch122, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	78
Mean	22.58
Std Dev	12.46

**Gaus mean : 29.1344**

**Gaus Width: 3.0005**

Entry

16

14

12

10

8

6

4

2

0

0

10

20

30

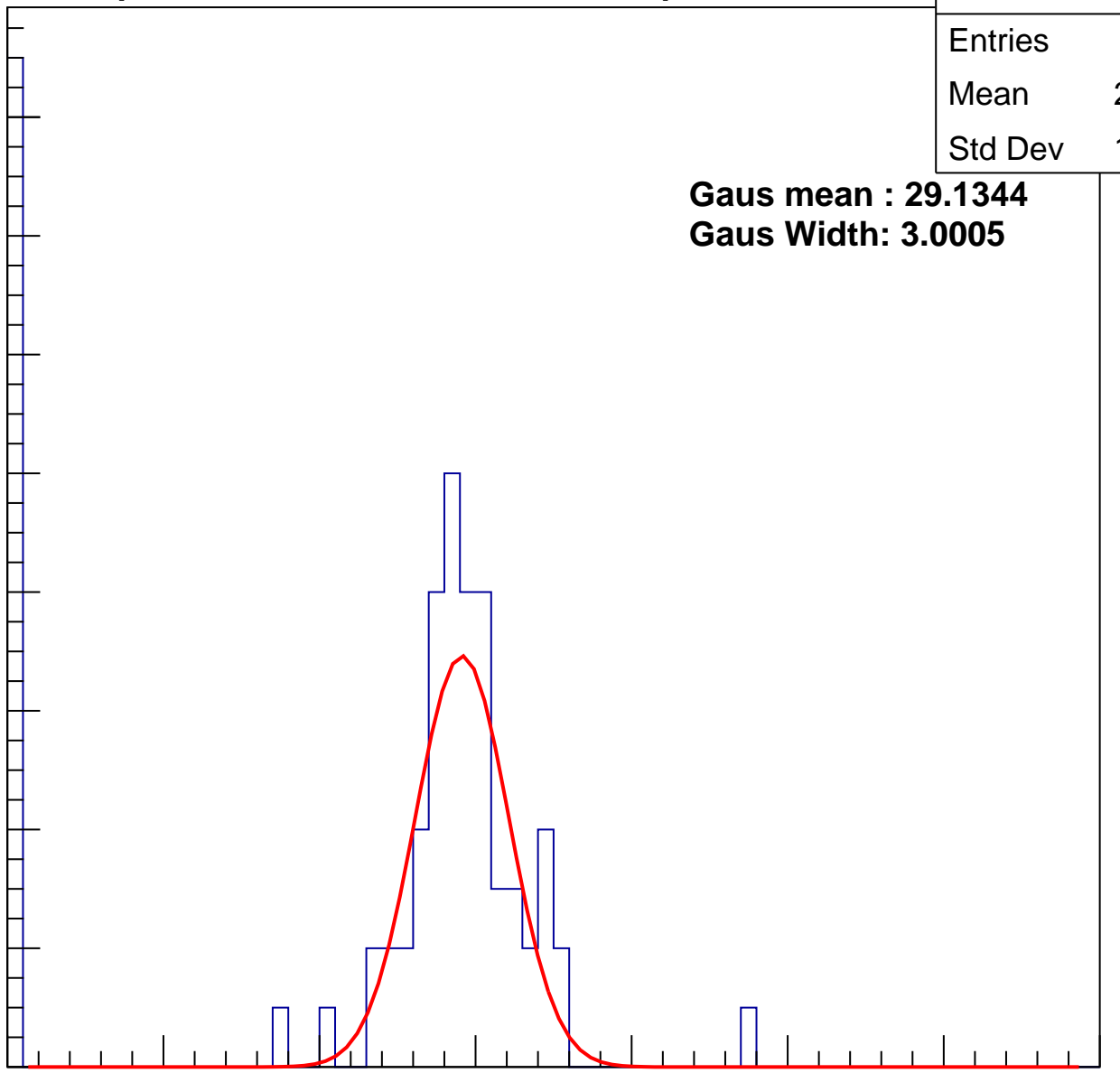
40

50

60

70

ampl



# B1L103S, U3-ch122, adc1

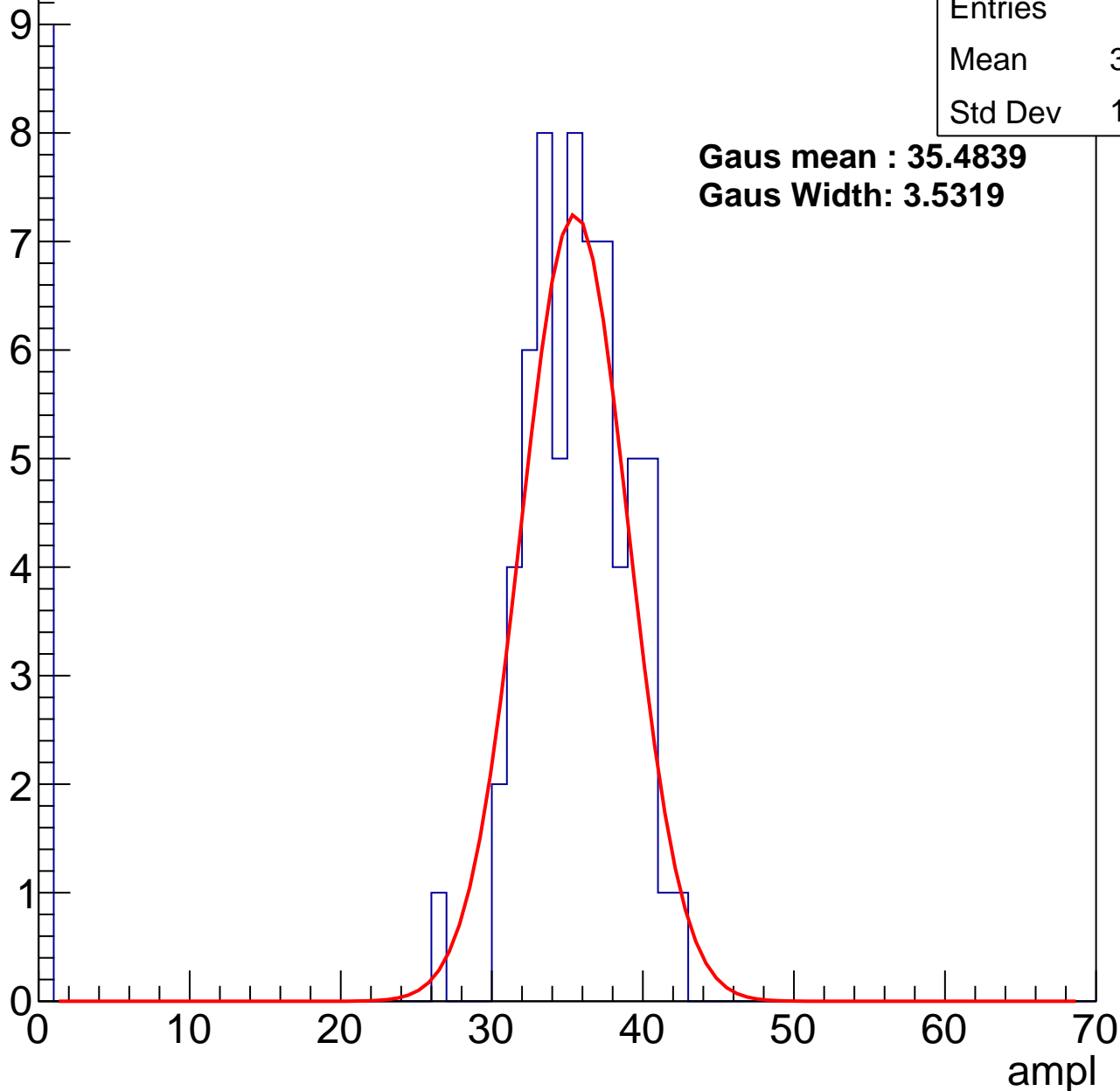
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	73
Mean	30.92
Std Dev	11.97

**Gaus mean : 35.4839**

**Gaus Width: 3.5319**



# B1L103S, U3-ch122, adc2

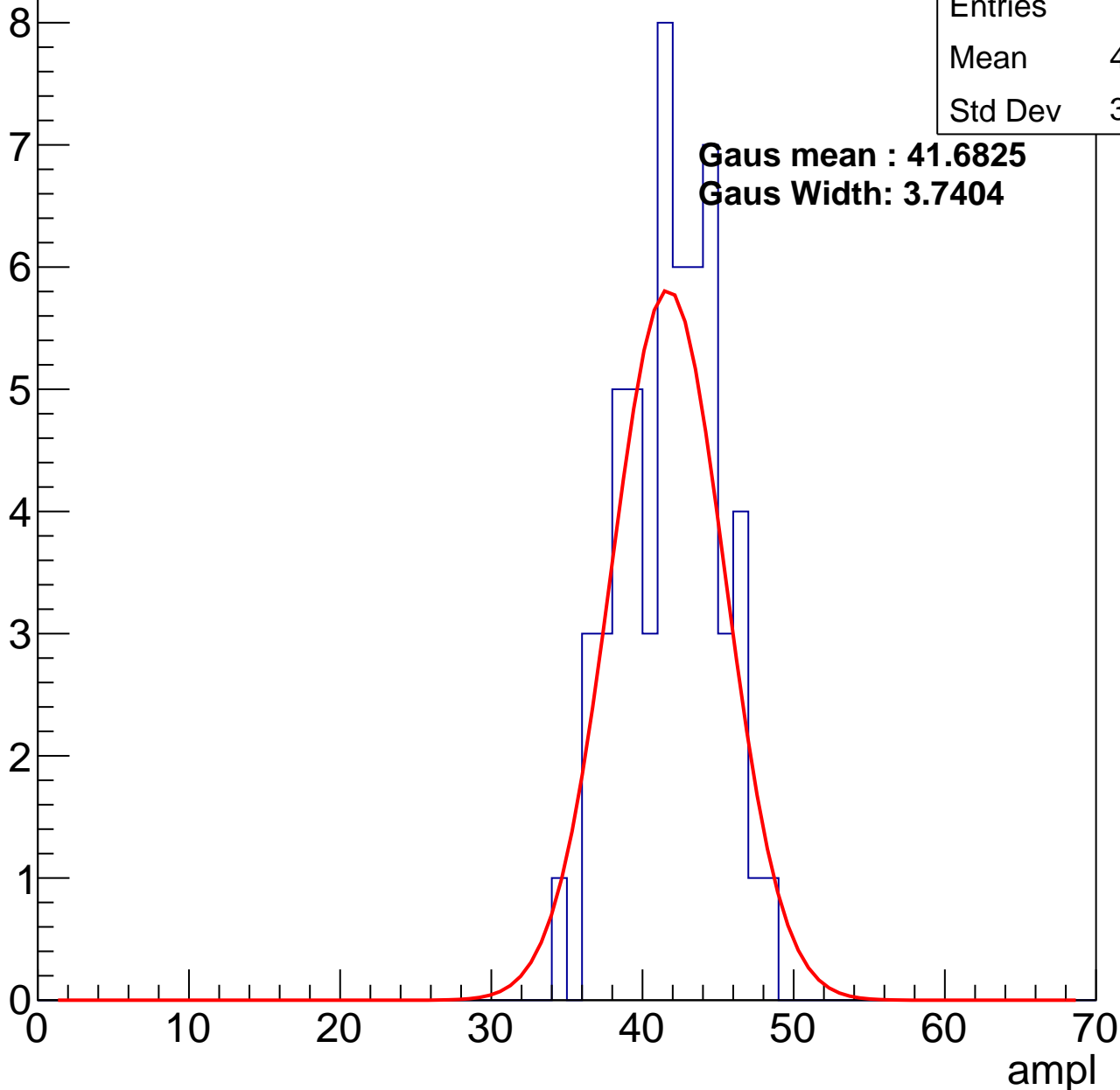
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	56
Mean	41.39
Std Dev	3.155

**Gaus mean : 41.6825**

**Gaus Width: 3.7404**

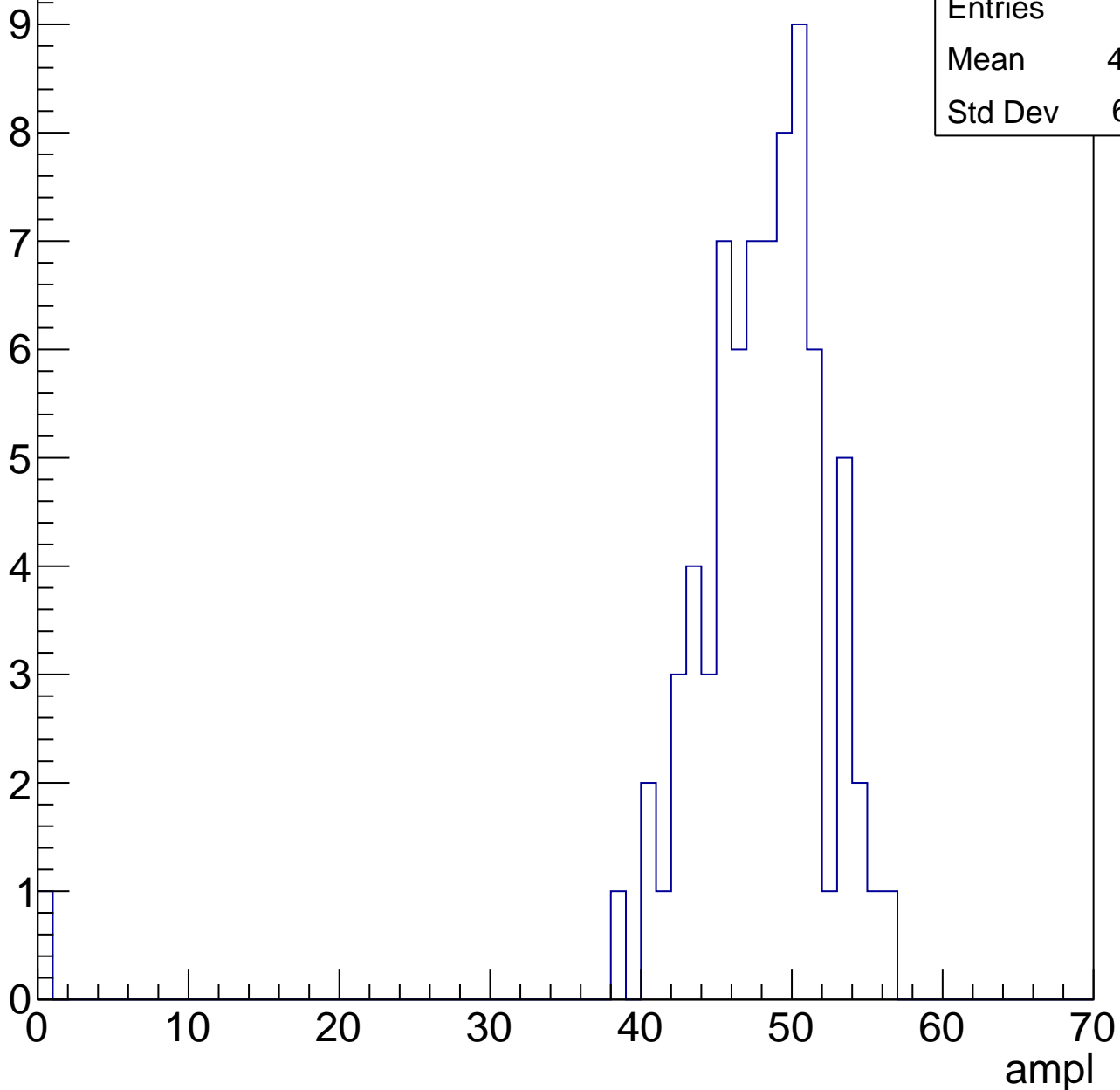


# B1L103S, U3-ch122, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	75
Mean	47.05
Std Dev	6.621

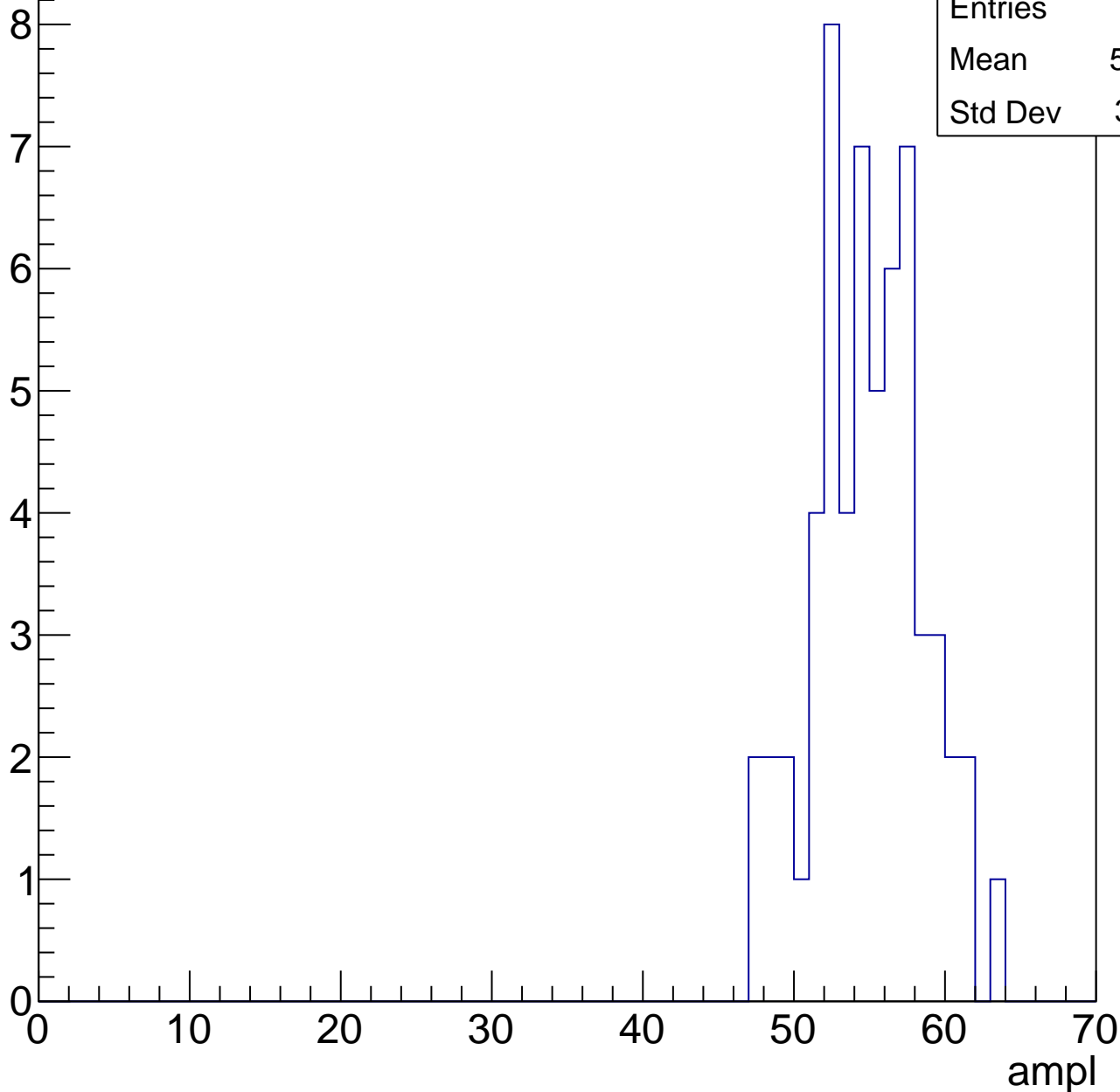


# B1L103S, U3-ch122, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	59
Mean	54.47
Std Dev	3.591



# B1L103S, U3-ch122, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

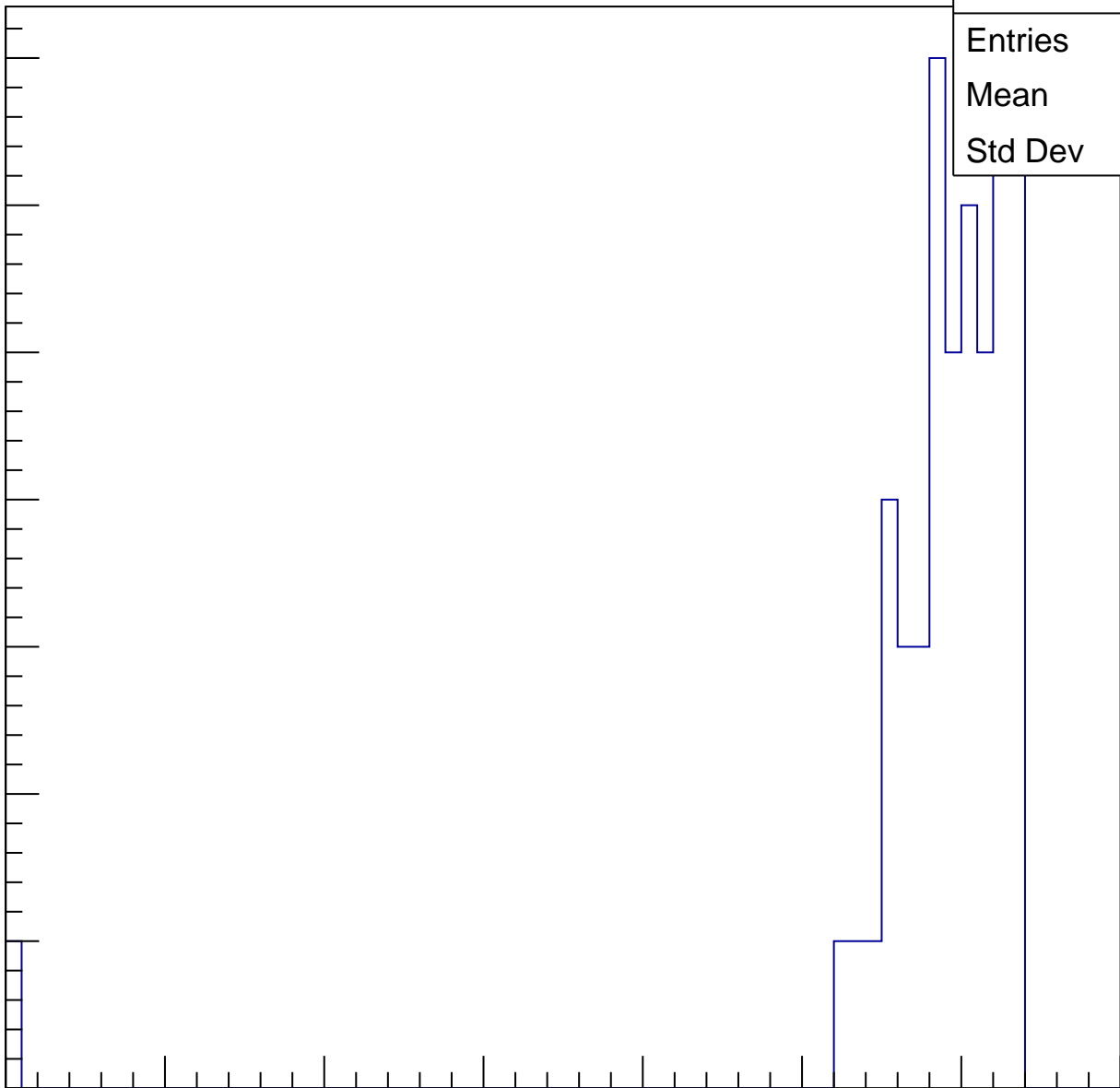
Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	58.02
Std Dev	8.692

ampl

0 10 20 30 40 50 60 70



# B1L103S, U3-ch122, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	9
Mean	61
Std Dev	1.491

ampl

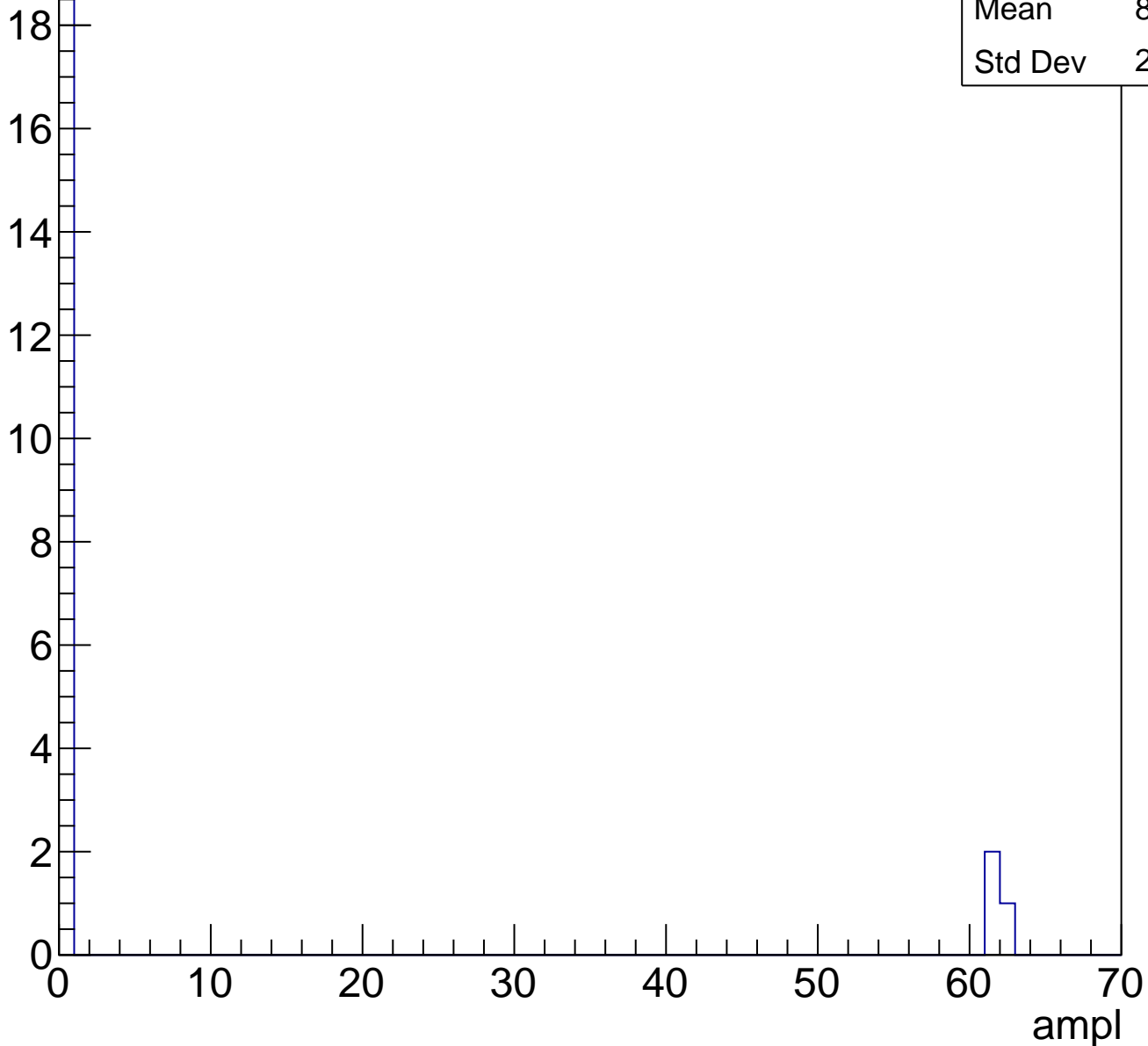


# B1L103S, U3-ch122, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	22
Mean	8.364
Std Dev	21.05

Entry



# B1L103S, U3-ch123, adc0

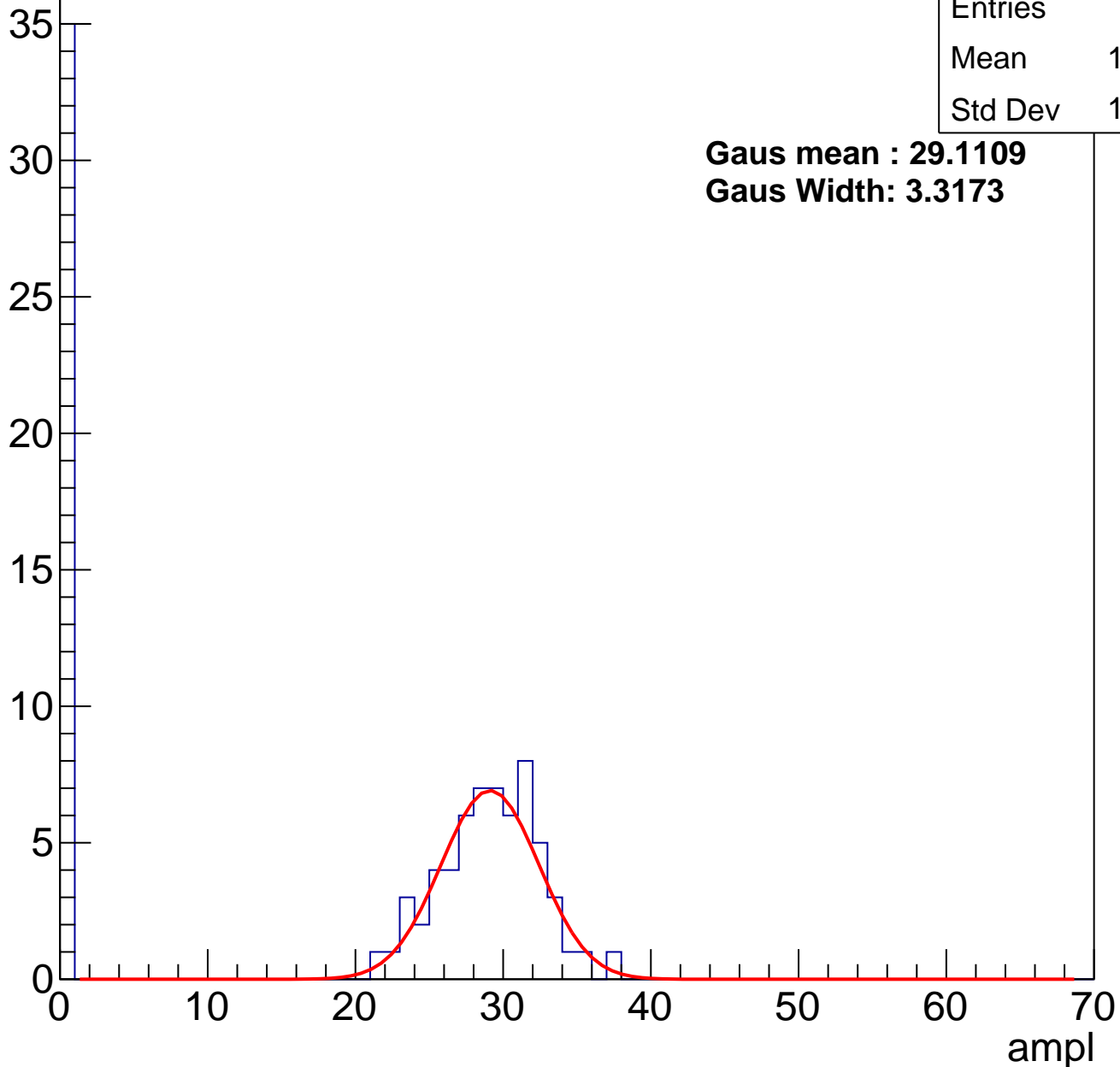
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	95
Mean	18.08
Std Dev	14.06

**Gaus mean : 29.1109**

**Gaus Width: 3.3173**

Entry



# B1L103S, U3-ch123, adc1

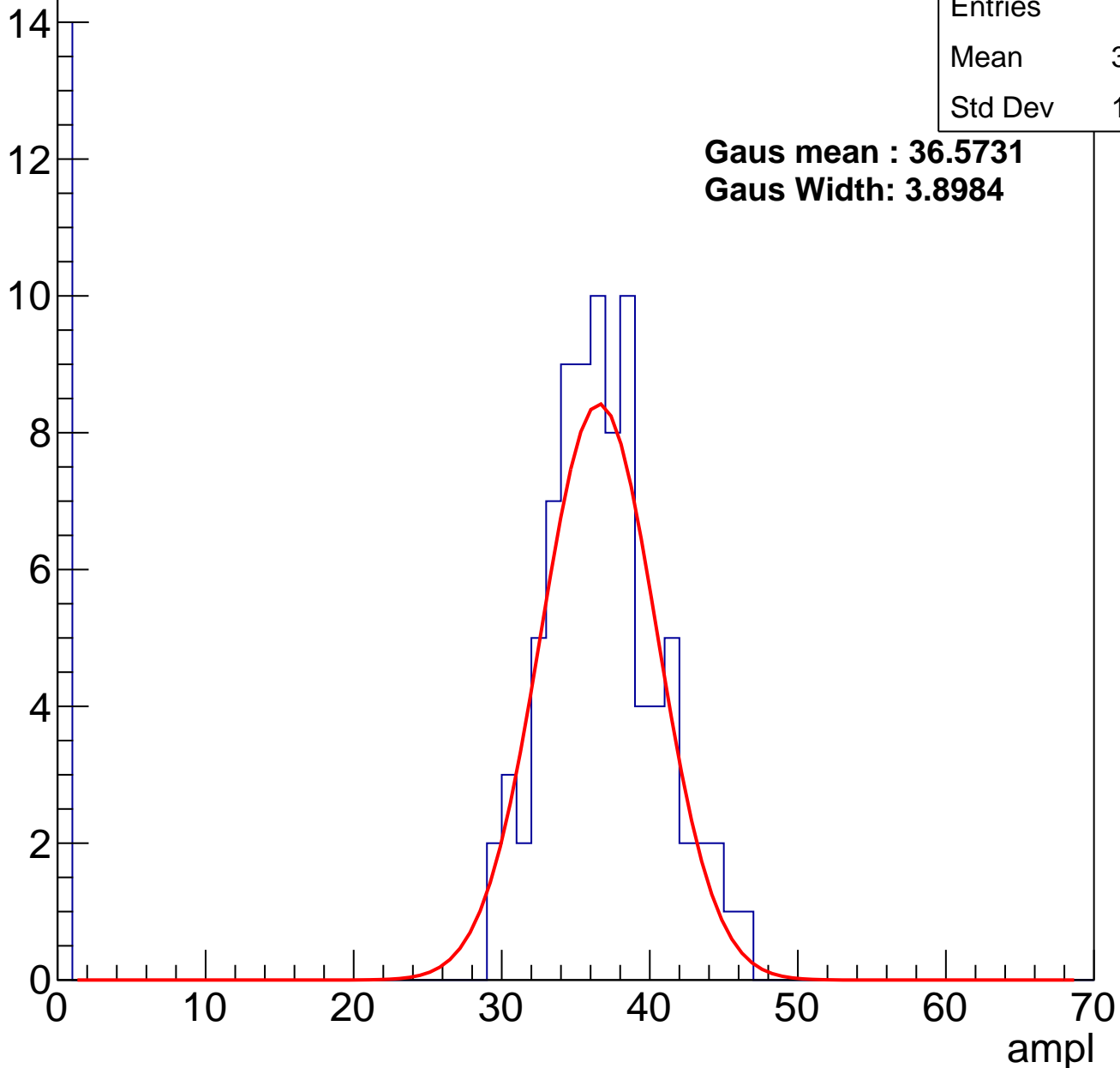
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	100
Mean	31.28
Std Dev	13.08

**Gaus mean : 36.5731**

**Gaus Width: 3.8984**

Entry



# B1L103S, U3-ch123, adc2

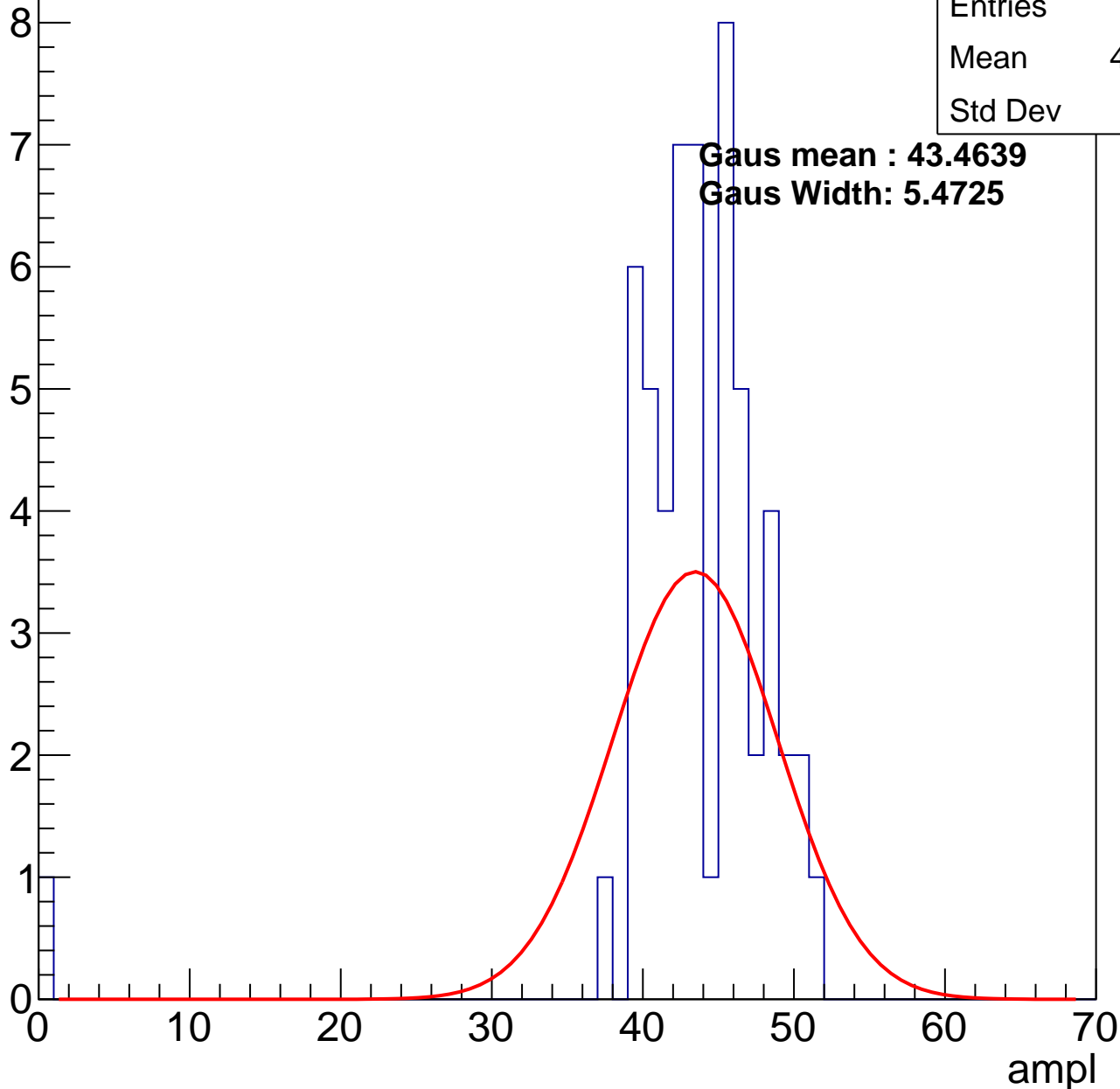
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	56
Mean	42.84
Std Dev	6.67

**Gaus mean : 43.4639**

**Gaus Width: 5.4725**

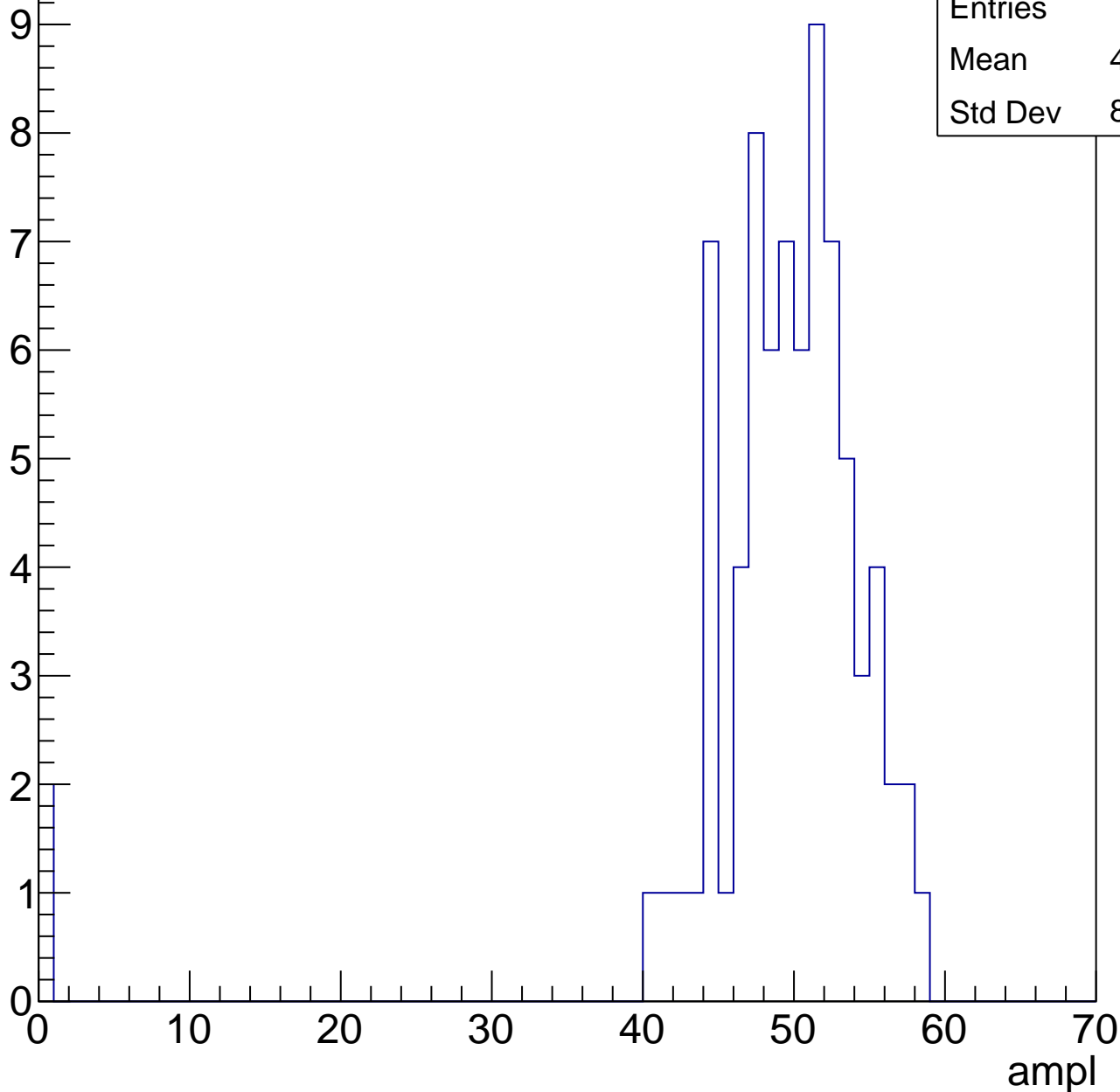


# B1L103S, U3-ch123, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	78
Mean	48.26
Std Dev	8.745

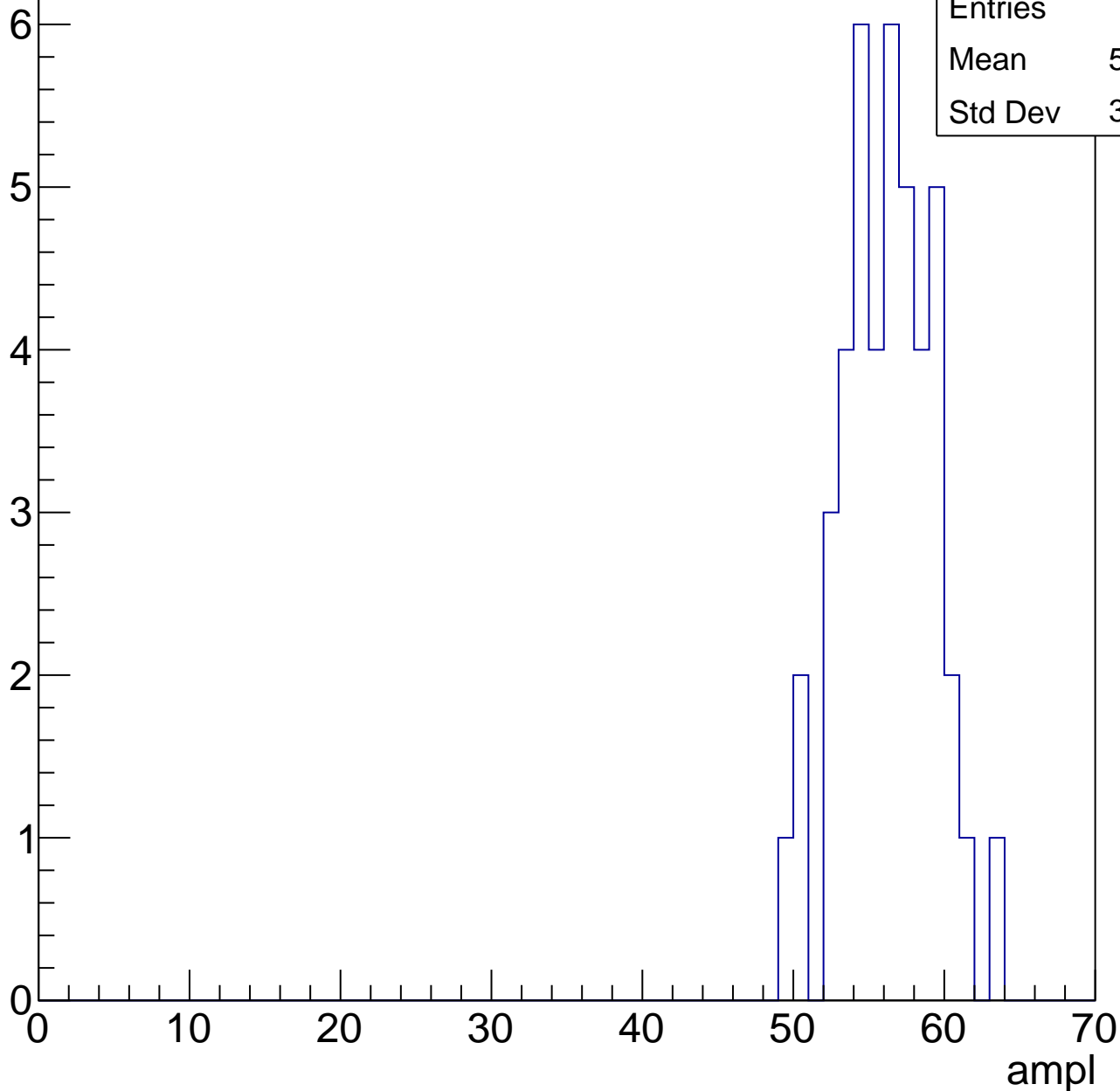


# B1L103S, U3-ch123, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	44
Mean	55.75
Std Dev	3.024



# B1L103S, U3-ch123, adc5

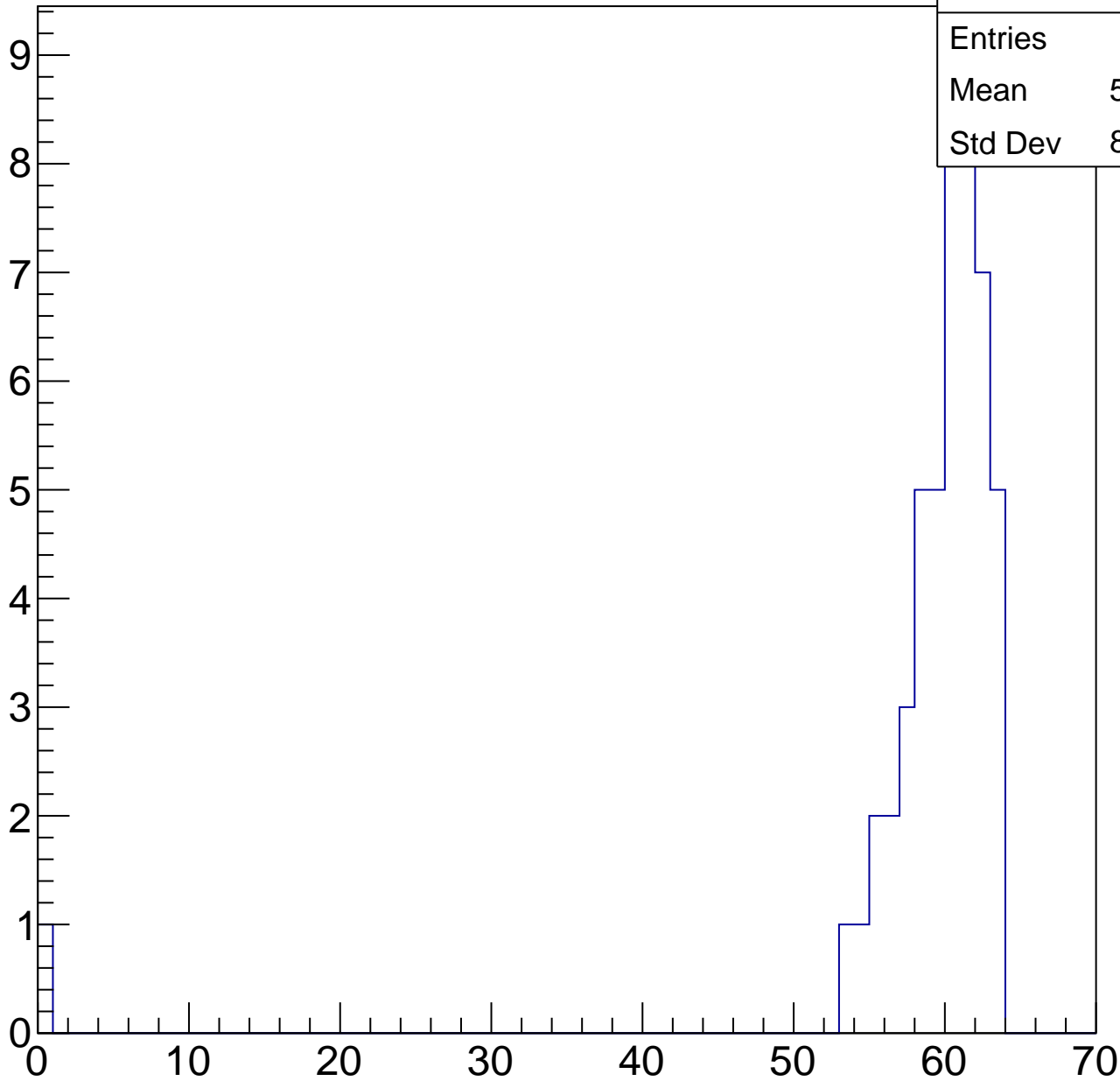
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	58.43
Std Dev	8.783

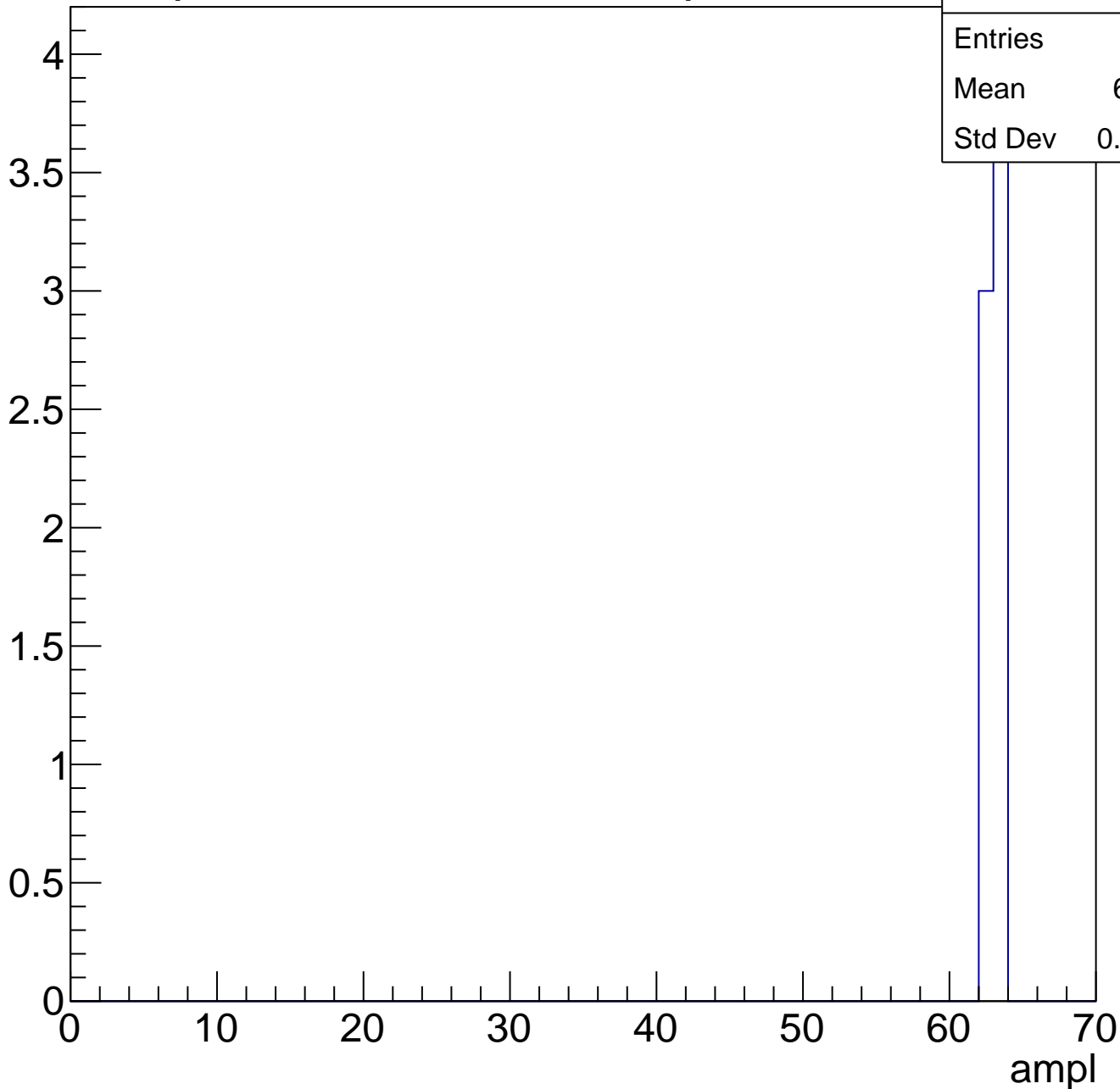
ampl



# B1L103S, U3-ch123, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry





# B1L103S, U3-ch123, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U3-ch124, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	118
Mean	20.92
Std Dev	12.67

**Gaus mean : 28.2849**

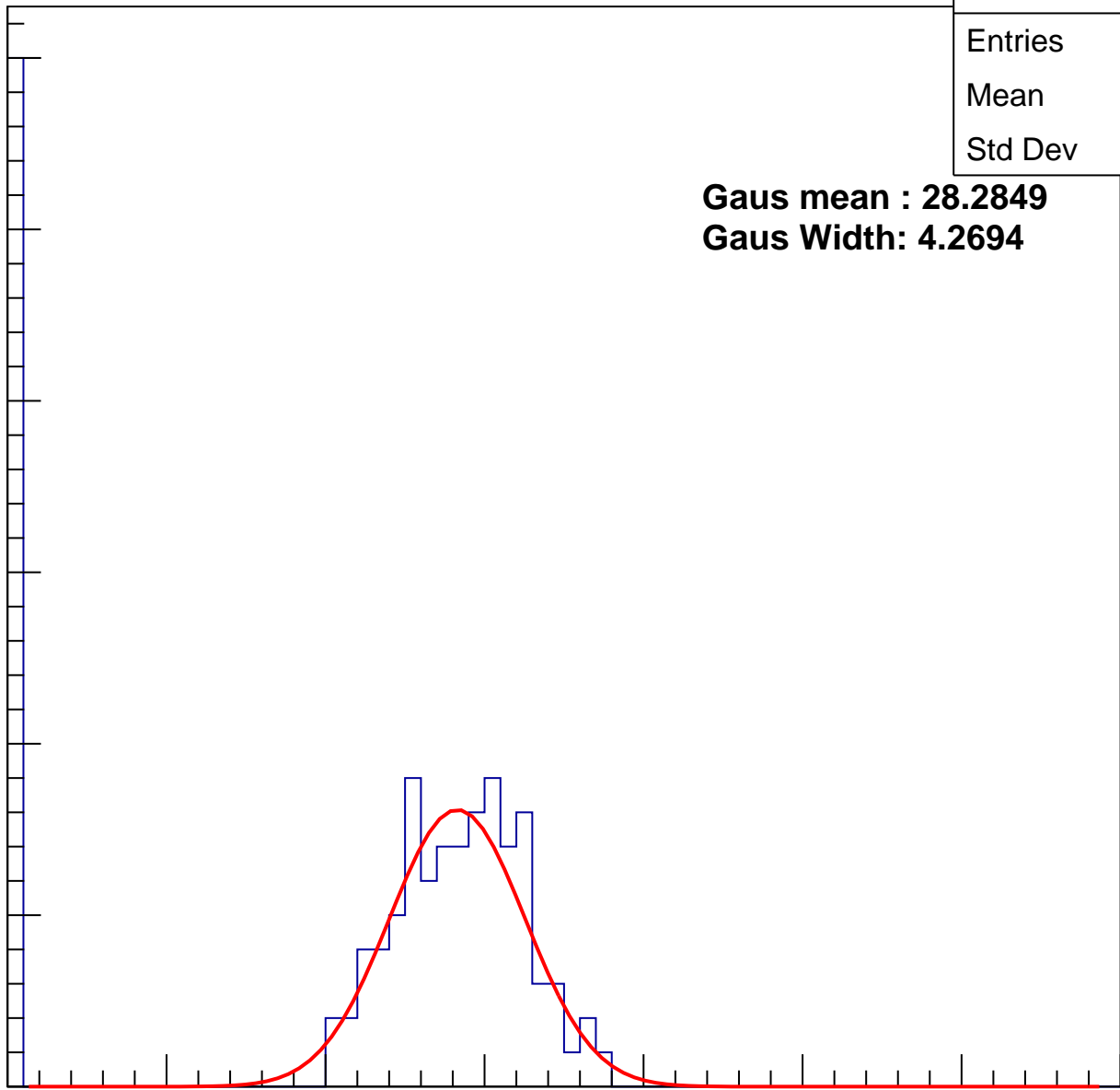
**Gaus Width: 4.2694**

Entry

30  
25  
20  
15  
10  
5  
0

ampl

0 10 20 30 40 50 60 70



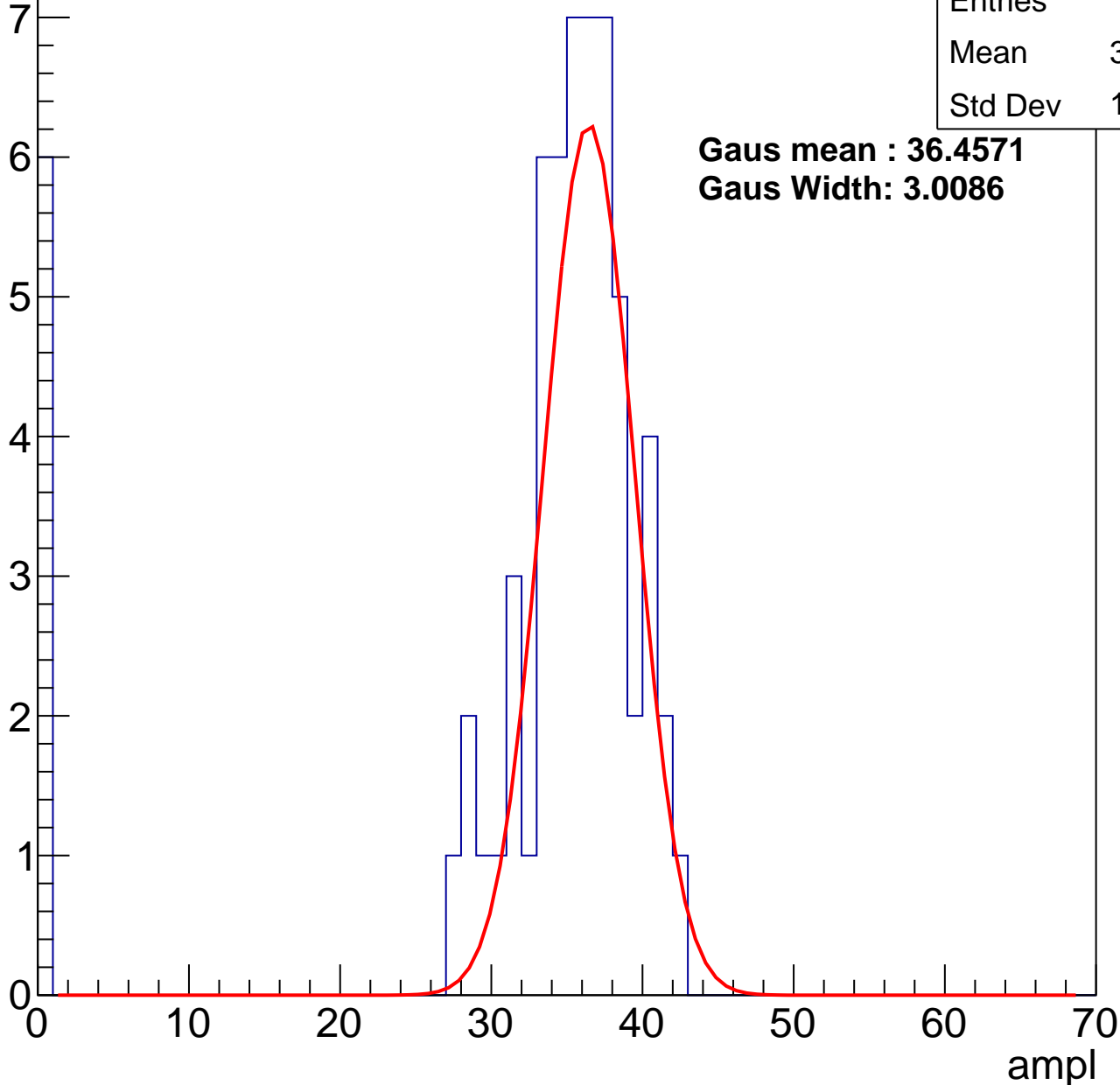
# B1L103S, U3-ch124, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	31.89
Std Dev	10.92

**Gaus mean : 36.4571**  
**Gaus Width: 3.0086**



# B1L103S, U3-ch124, adc2

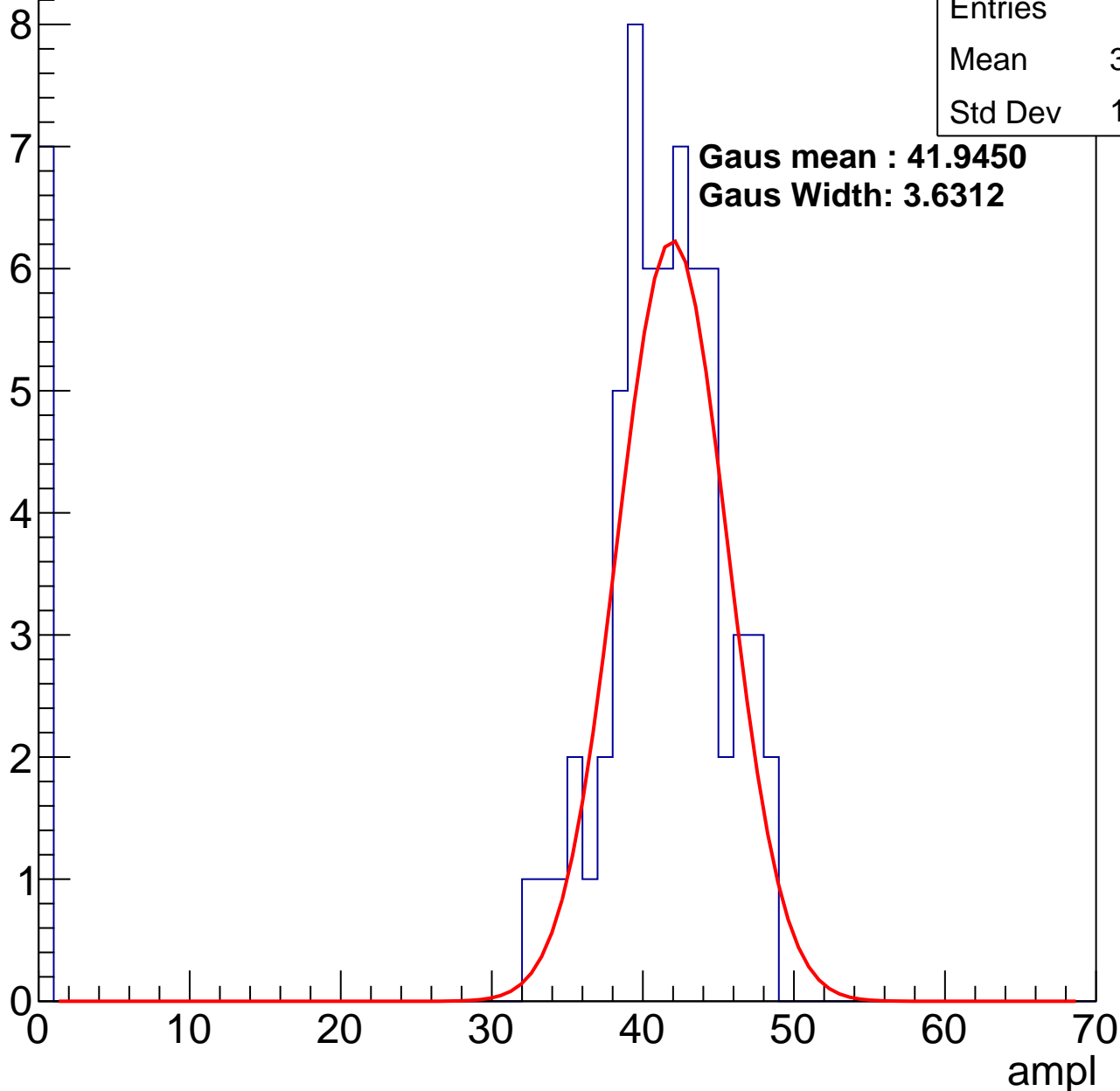
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	69
Mean	36.93
Std Dev	12.87

**Gaus mean : 41.9450**

**Gaus Width: 3.6312**

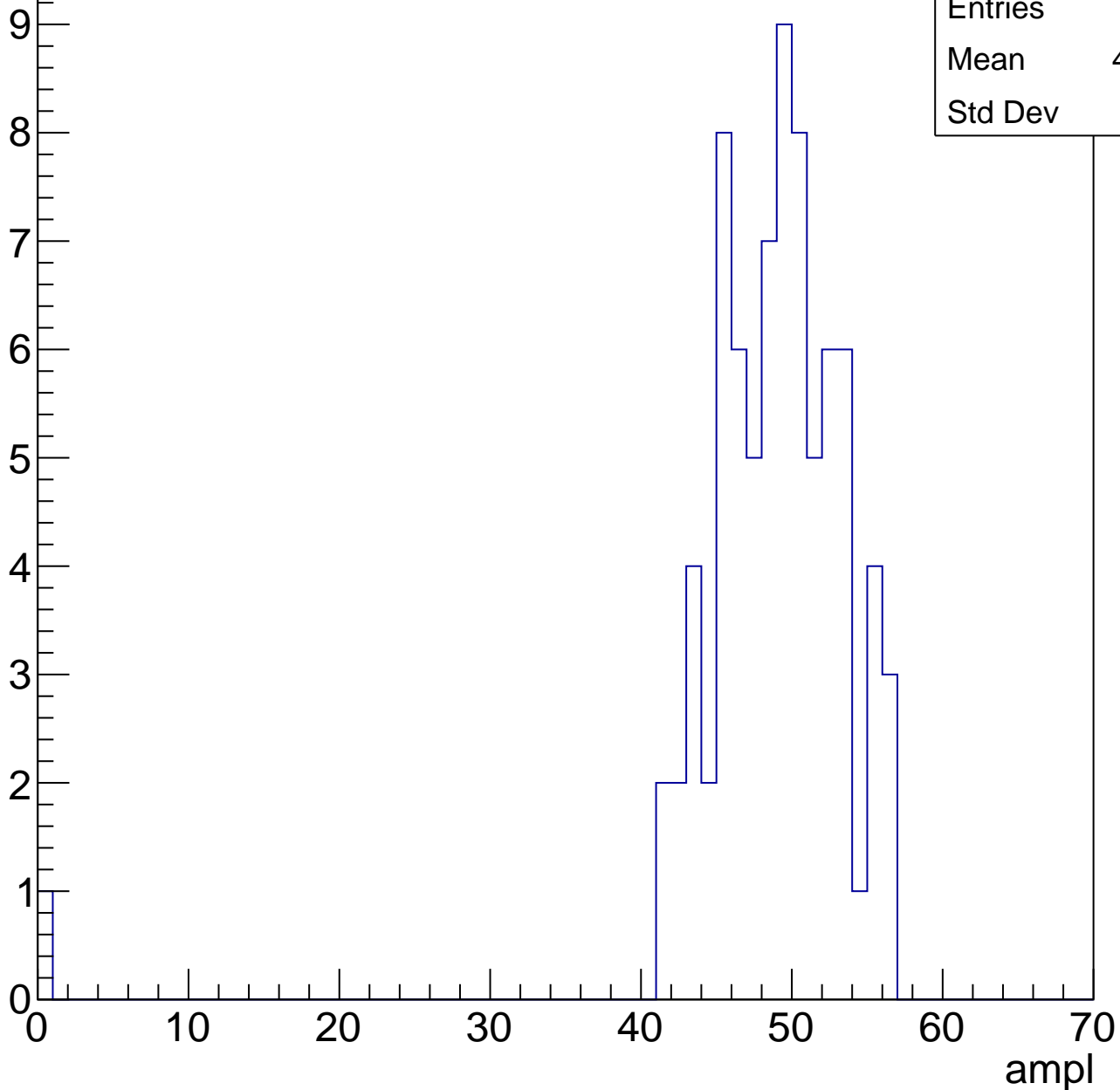


# B1L103S, U3-ch124, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	79
Mean	48.11
Std Dev	6.62

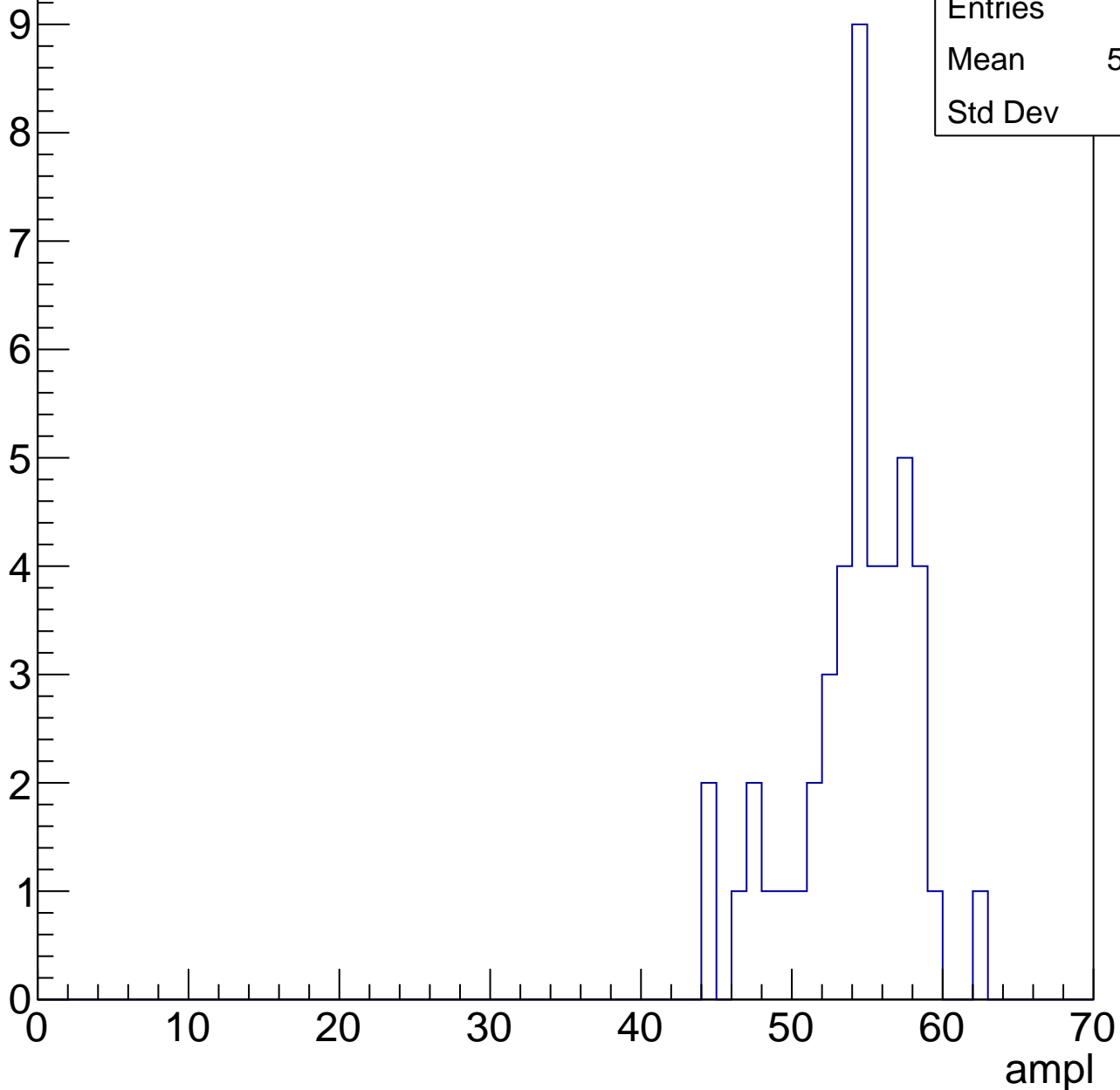


# B1L103S, U3-ch124, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	45
Mean	53.62
Std Dev	3.9

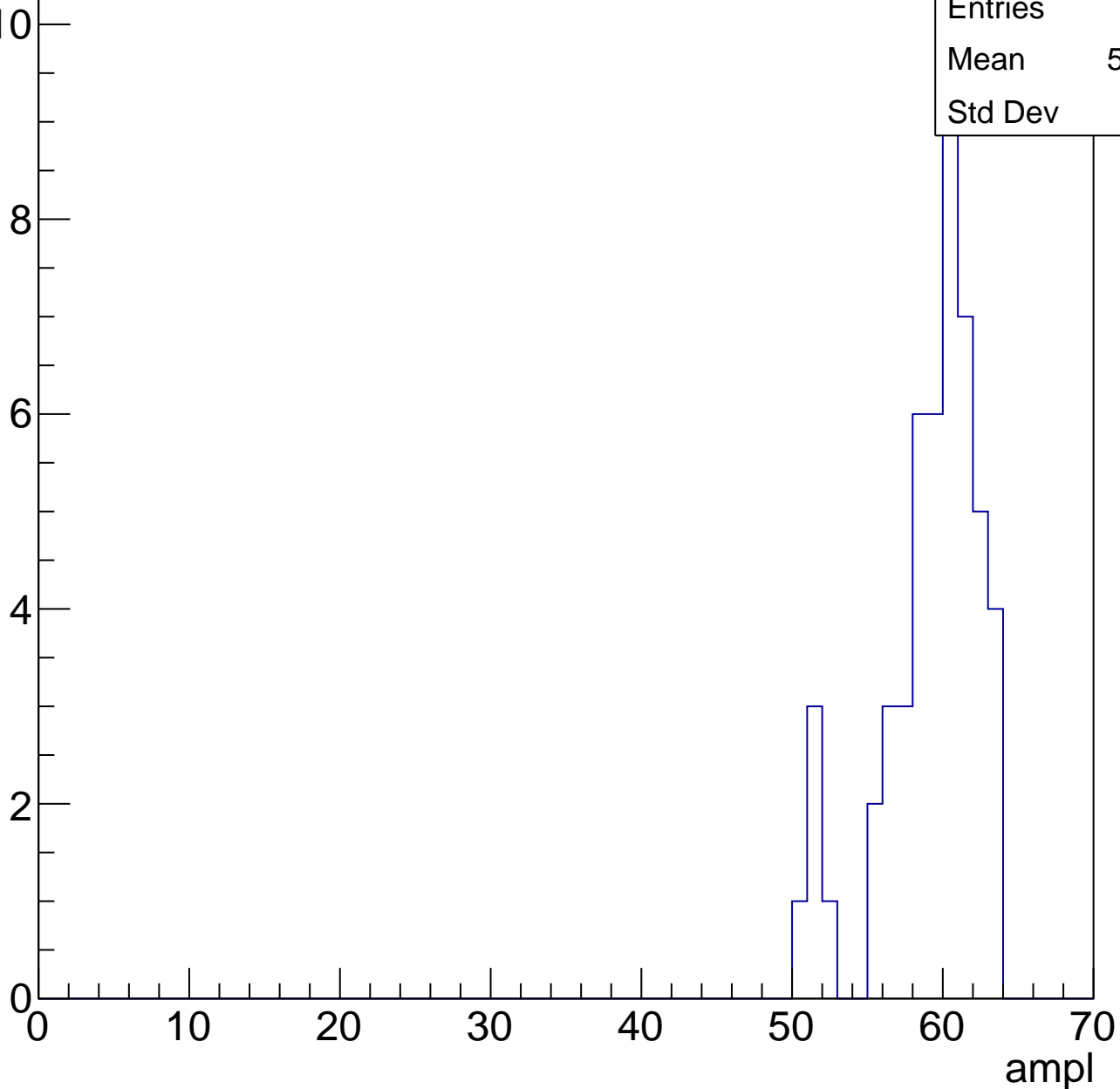


# B1L103S, U3-ch124, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	51
Mean	58.73
Std Dev	3.26

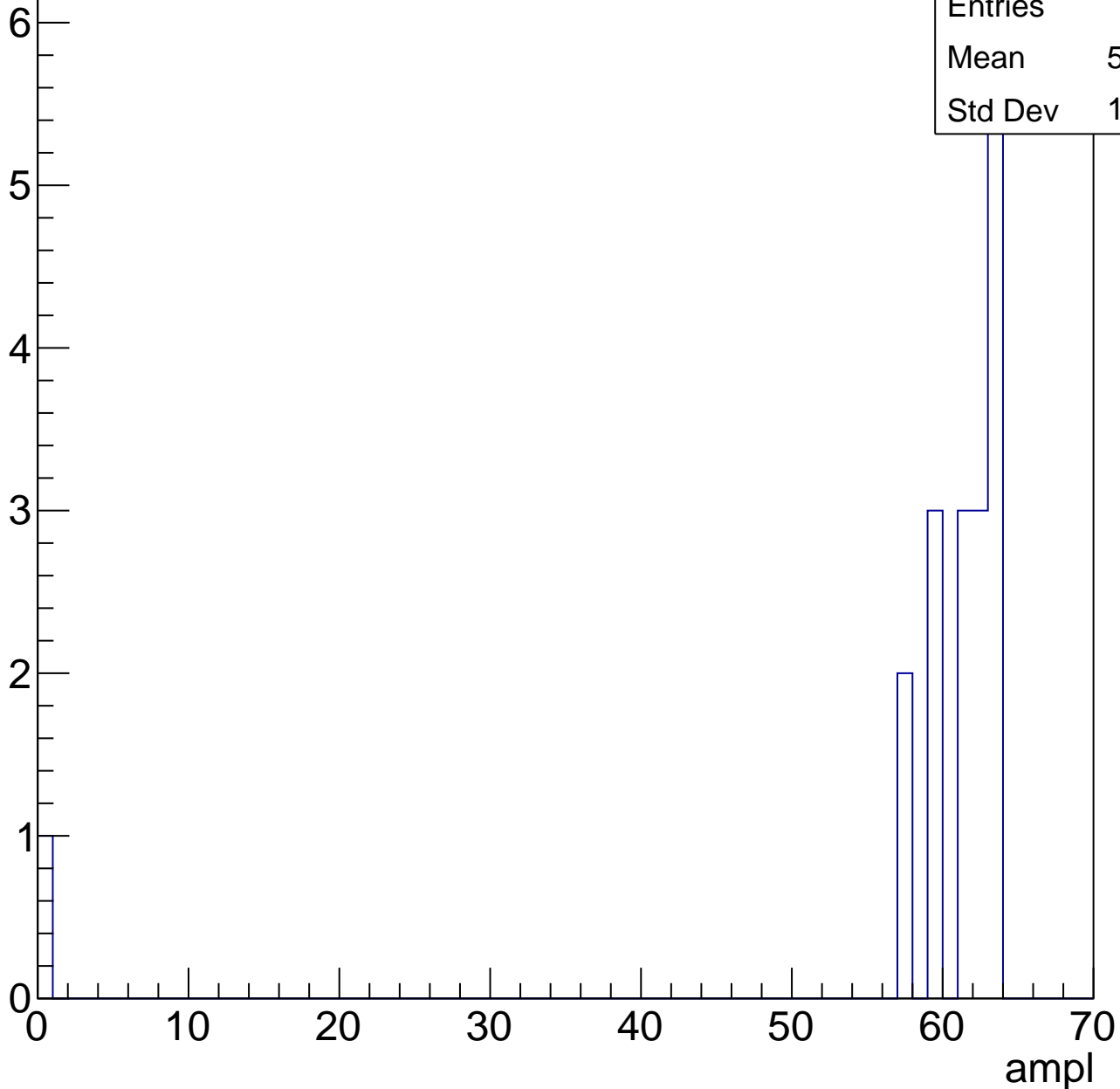


# B1L103S, U3-ch124, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	18
Mean	57.67
Std Dev	14.13





# B1L103S, U3-ch124, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51

Entry



# B1L103S, U3-ch125, adc0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	88
Mean	22.58
Std Dev	11.12

**Gaus mean : 28.7153**

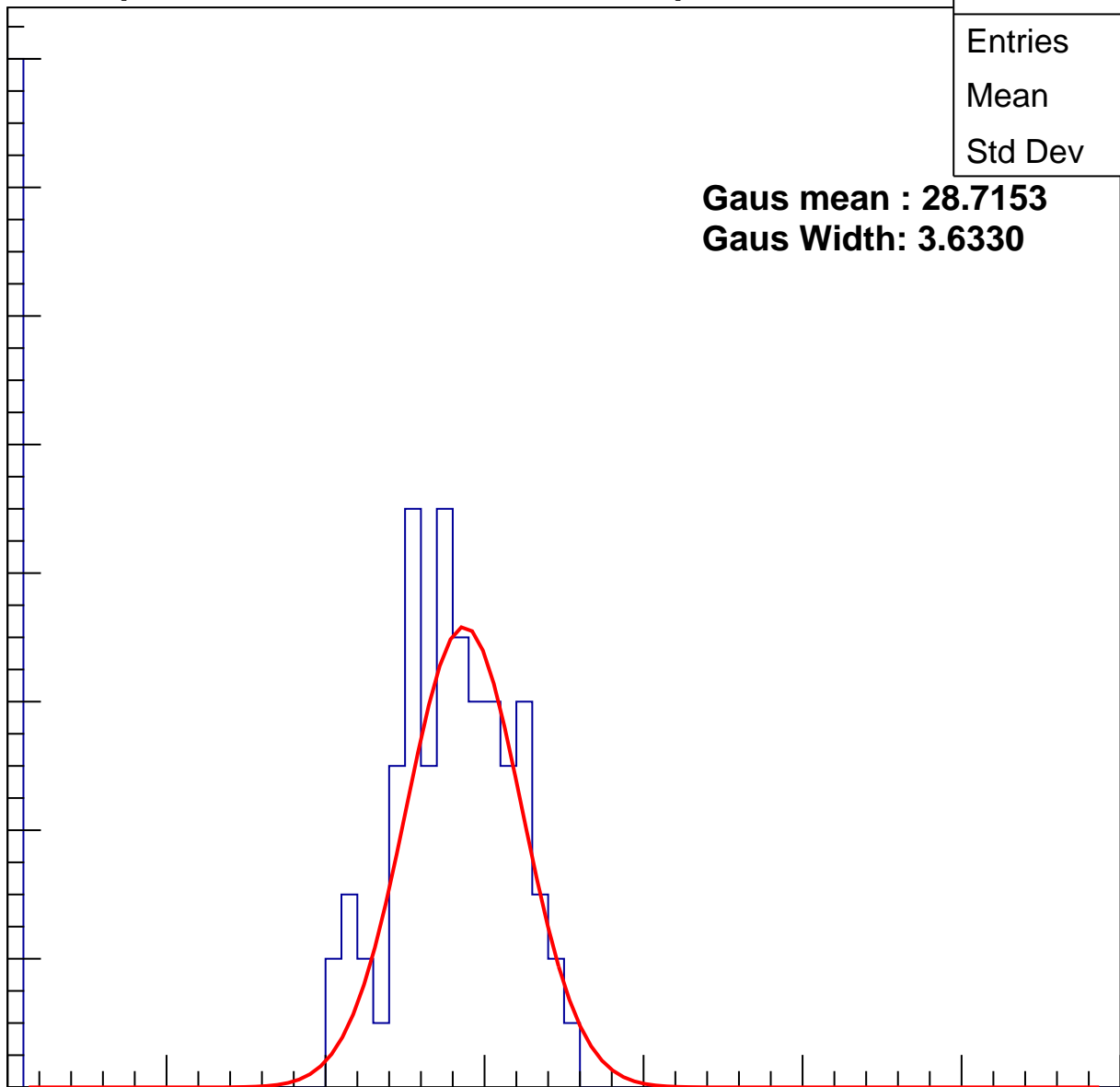
**Gaus Width: 3.6330**

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

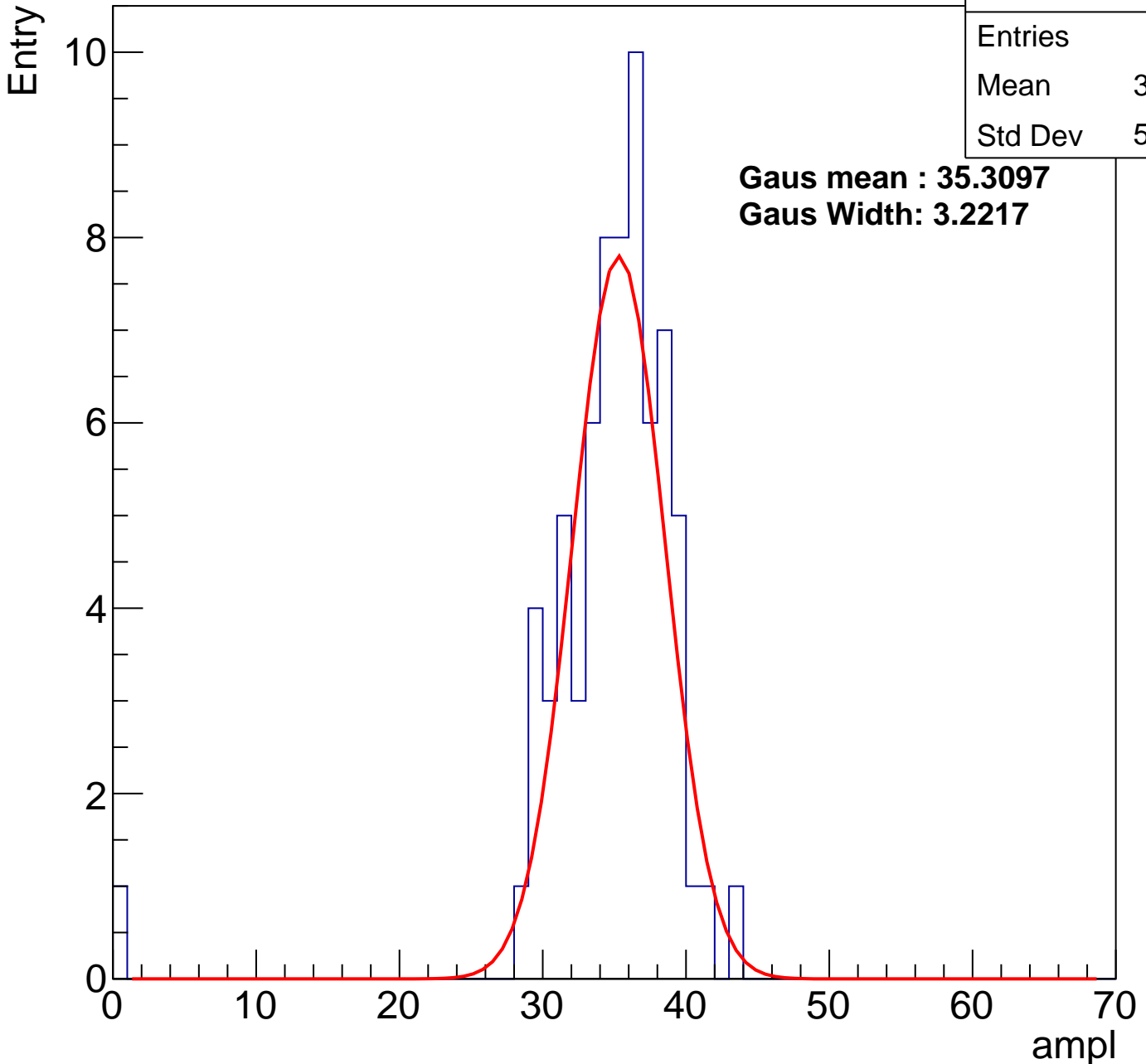


# B1L103S, U3-ch125, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	70
Mean	34.31
Std Dev	5.211

**Gaus mean : 35.3097**  
**Gaus Width: 3.2217**



# B1L103S, U3-ch125, adc2

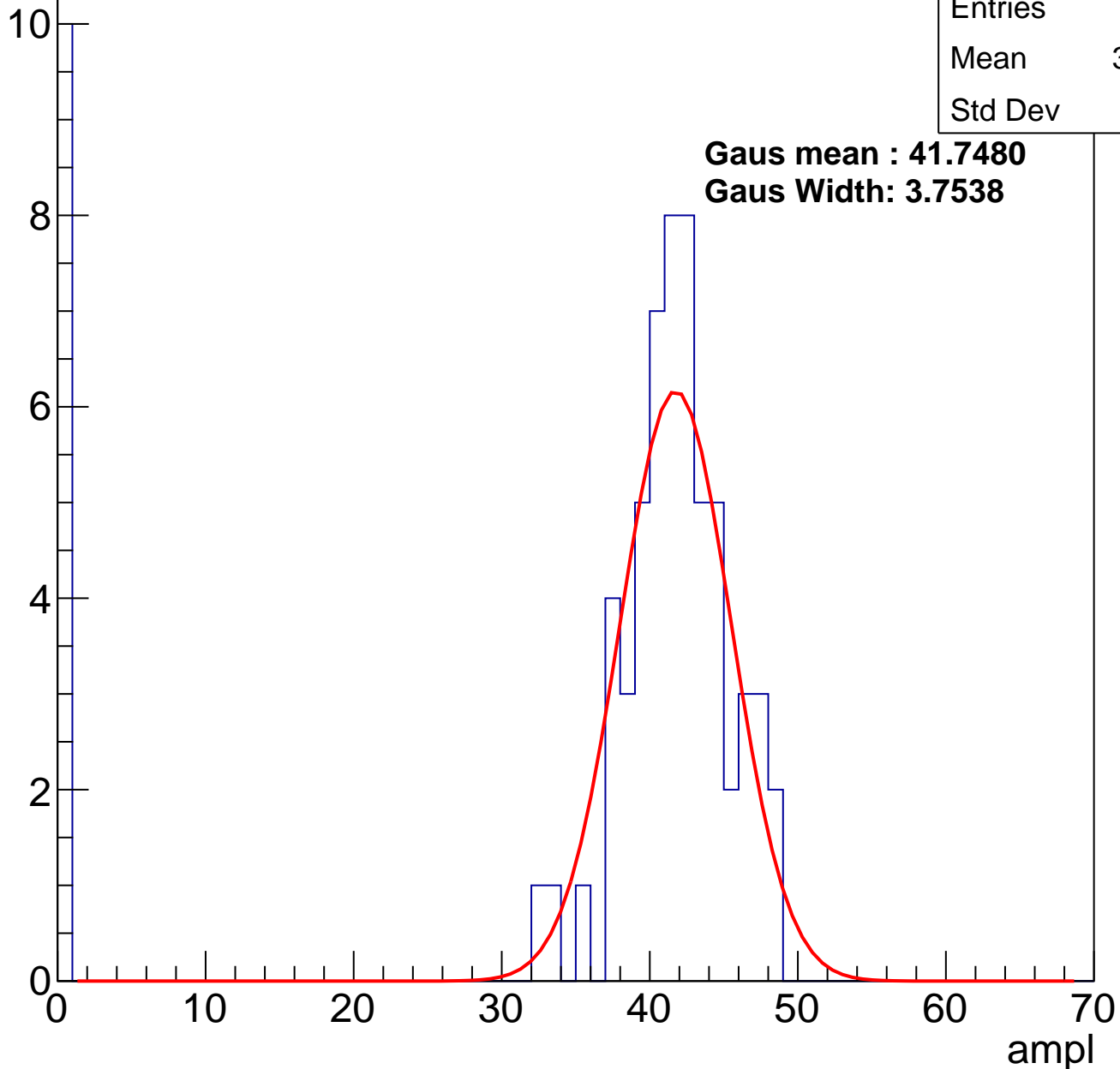
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	68
Mean	35.31
Std Dev	15

**Gaus mean : 41.7480**

**Gaus Width: 3.7538**

Entry



# B1L103S, U3-ch125, adc3

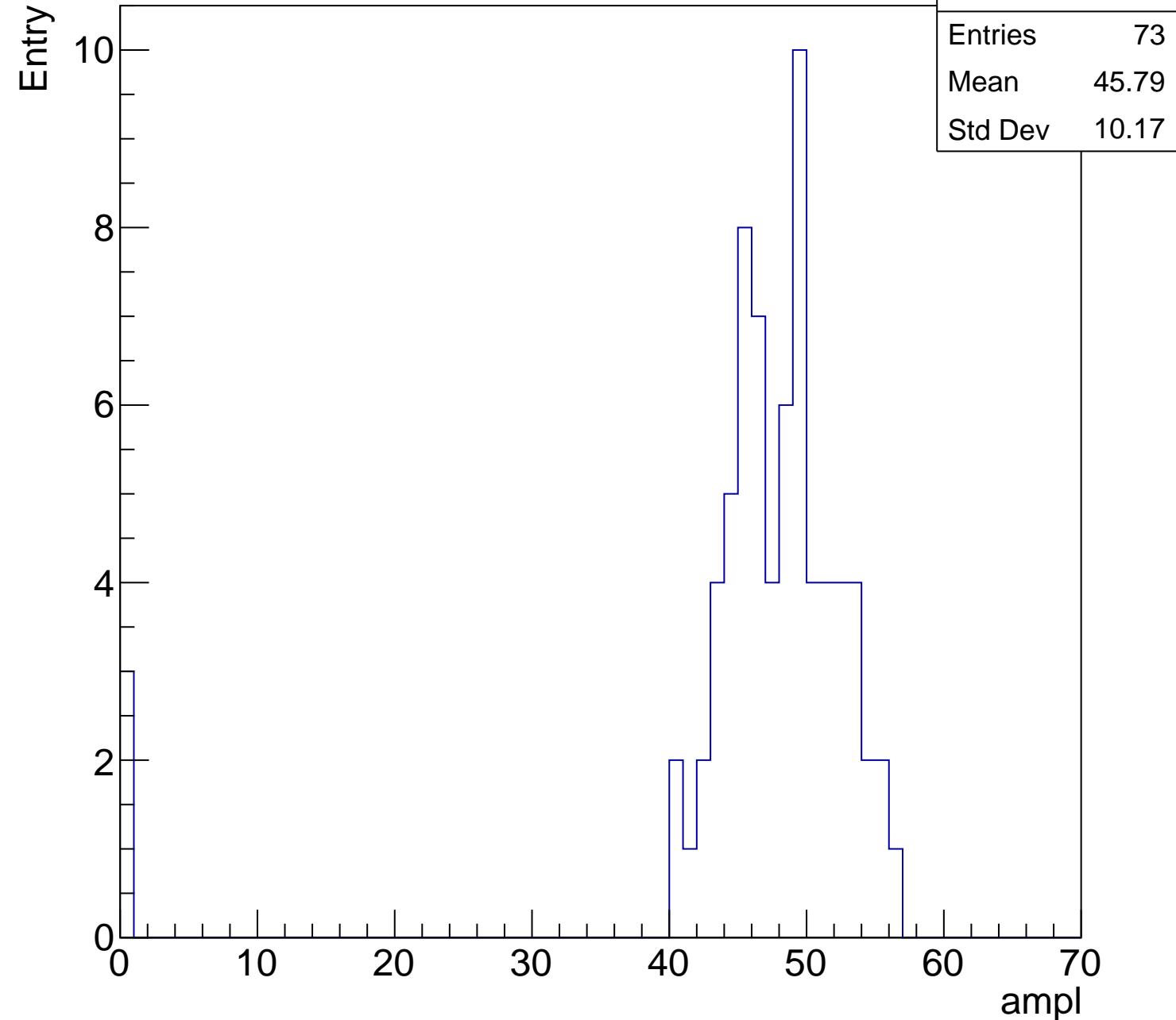
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	73
Mean	45.79
Std Dev	10.17

Entry

10  
8  
6  
4  
2  
0

ampl

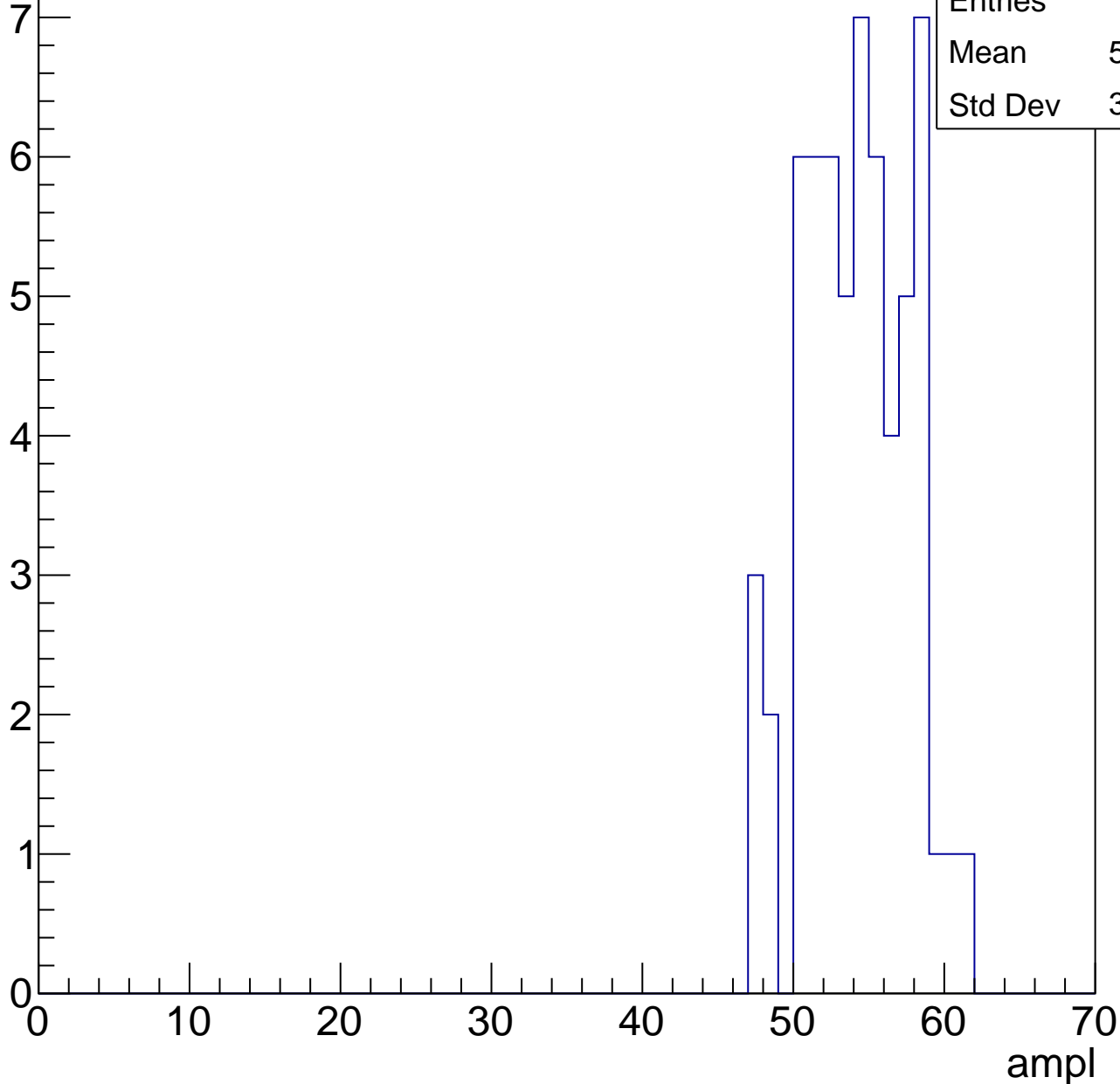


# B1L103S, U3-ch125, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

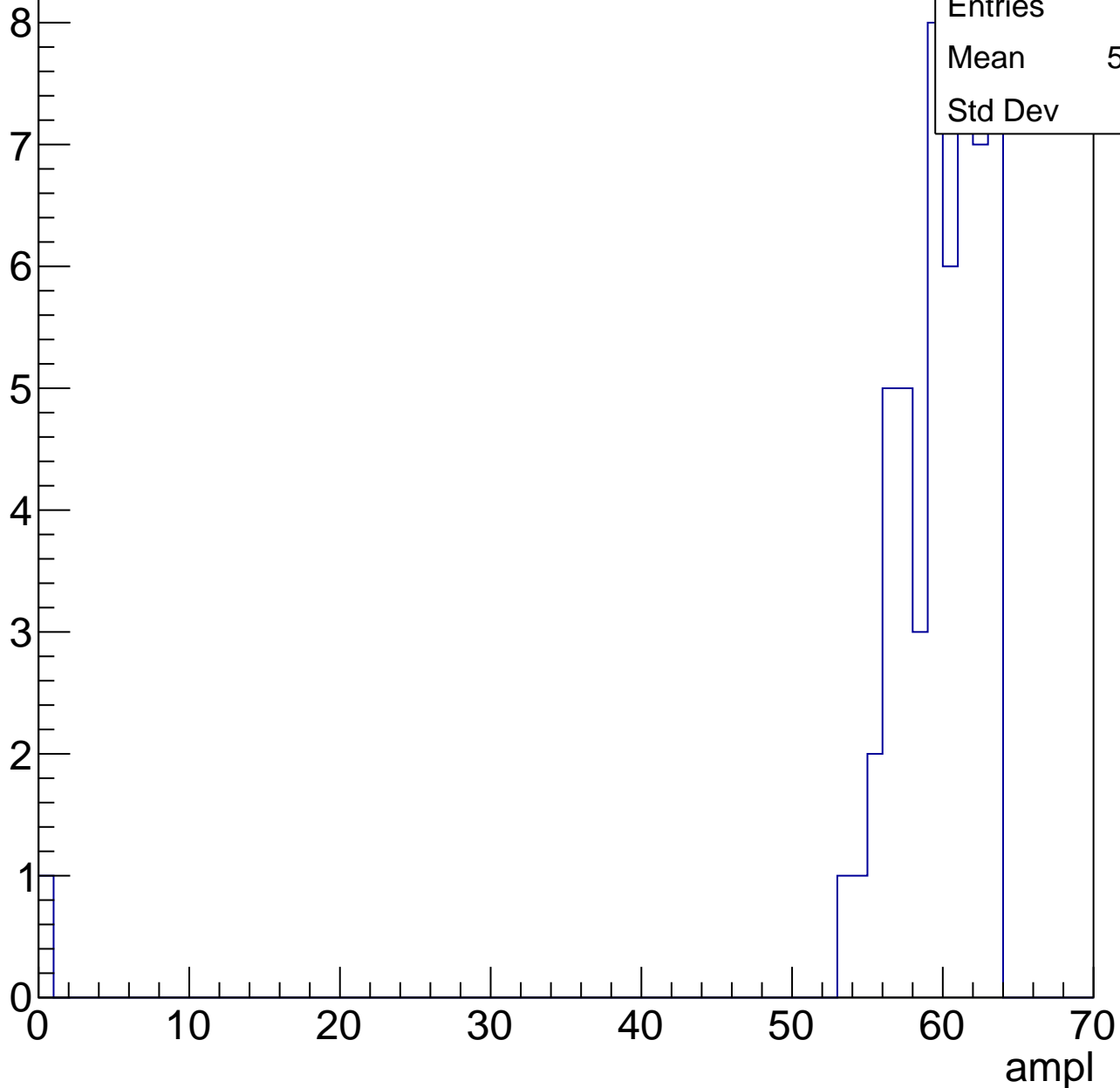
Entries	60
Mean	53.72
Std Dev	3.372



# B1L103S, U3-ch125, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

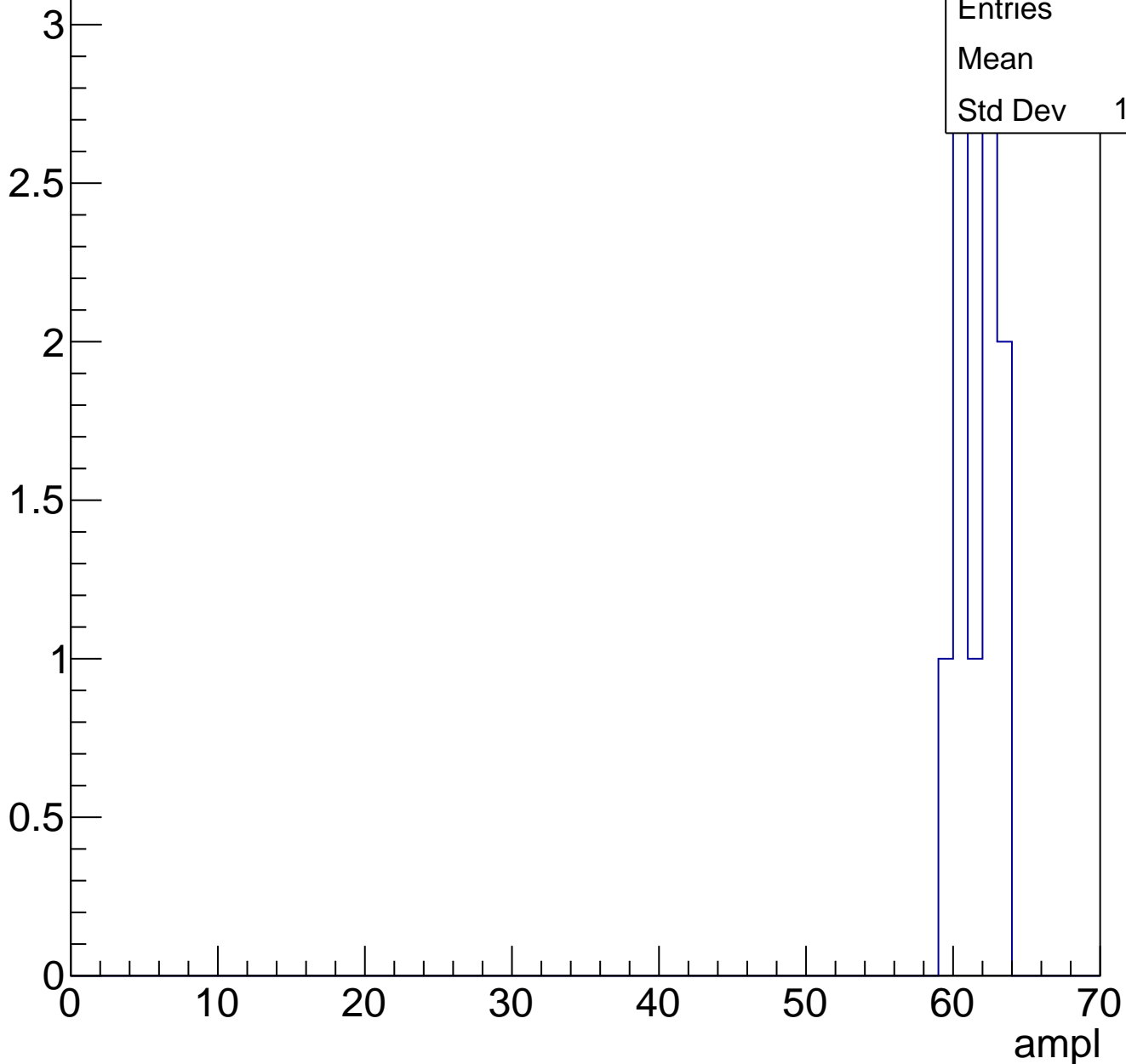
Entry



# B1L103S, U3-ch125, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	10
Mean	61.2
Std Dev	1.327



# B1L103S, U3-ch125, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

# B1L103S, U3-ch126, adc0

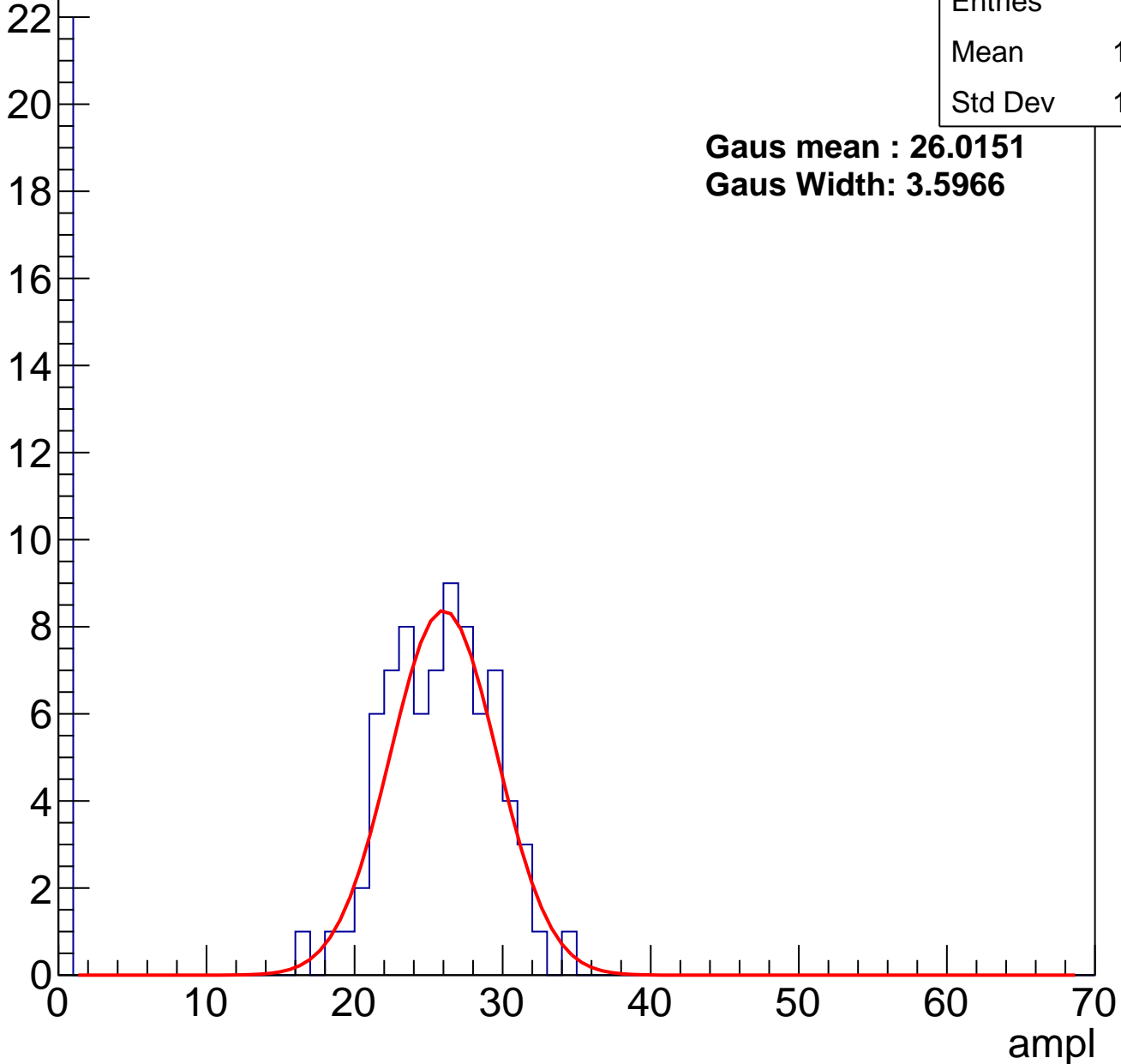
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	100
Mean	19.76
Std Dev	10.94

**Gaus mean : 26.0151**

**Gaus Width: 3.5966**

Entry



# B1L103S, U3-ch126, adc1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	79
Mean	27.42
Std Dev	12.43

**Gaus mean : 33.1890**

**Gaus Width: 2.9922**

Entry

12

10

8

6

4

2

0

0

10

20

30

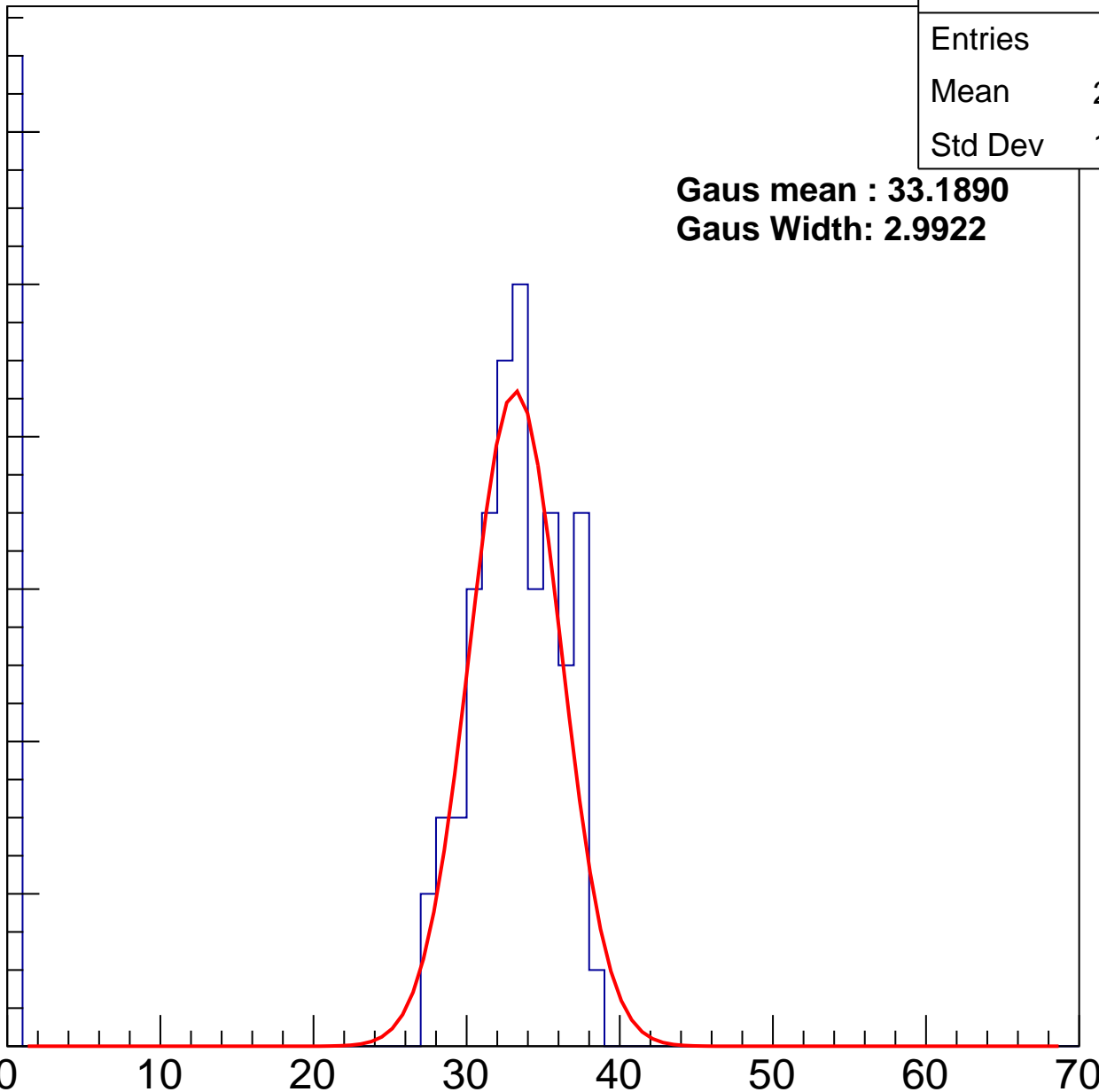
40

50

60

70

ampl



# B1L103S, U3-ch126, adc2

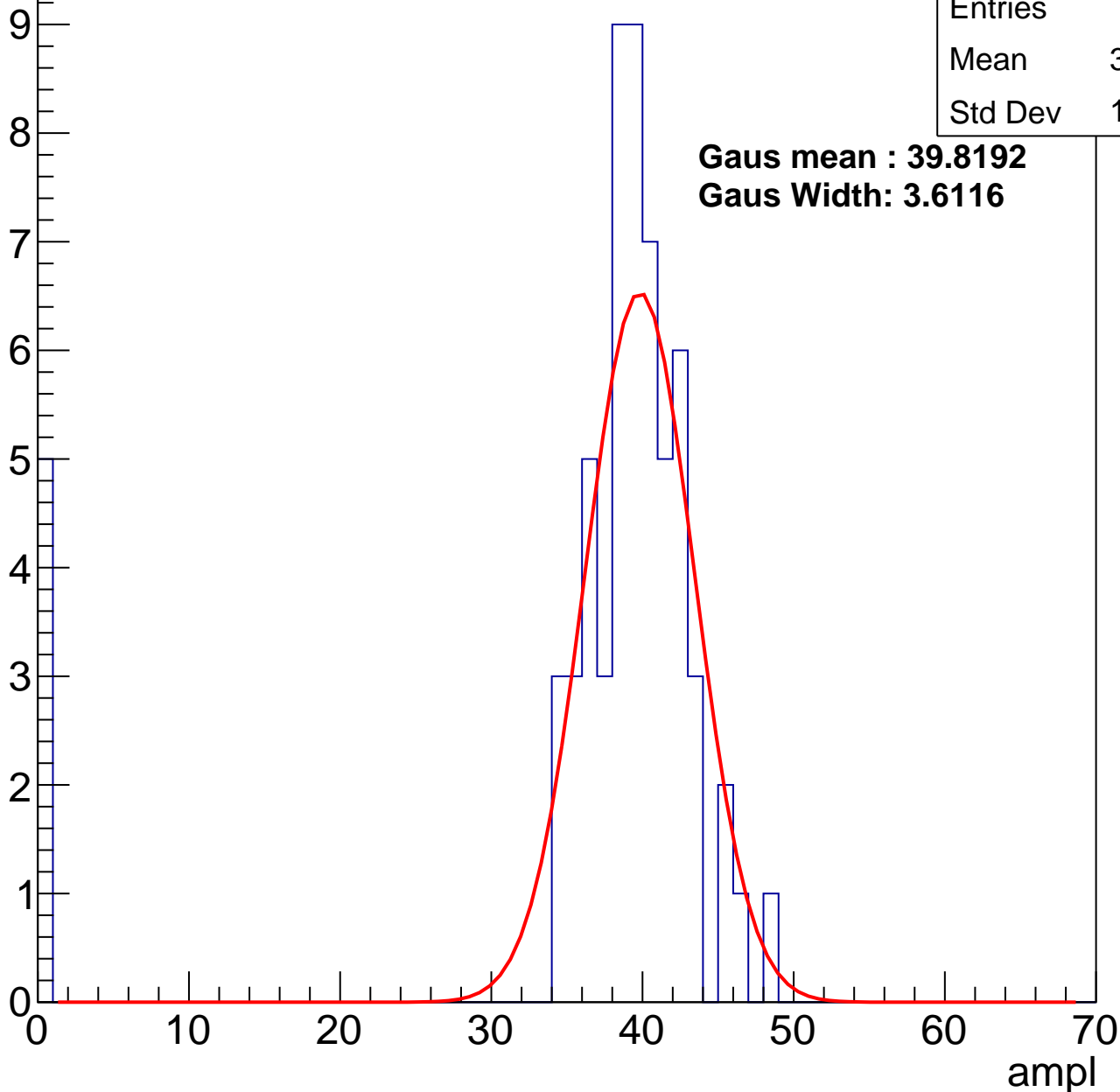
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	62
Mean	36.15
Std Dev	11.09

**Gaus mean : 39.8192**

**Gaus Width: 3.6116**

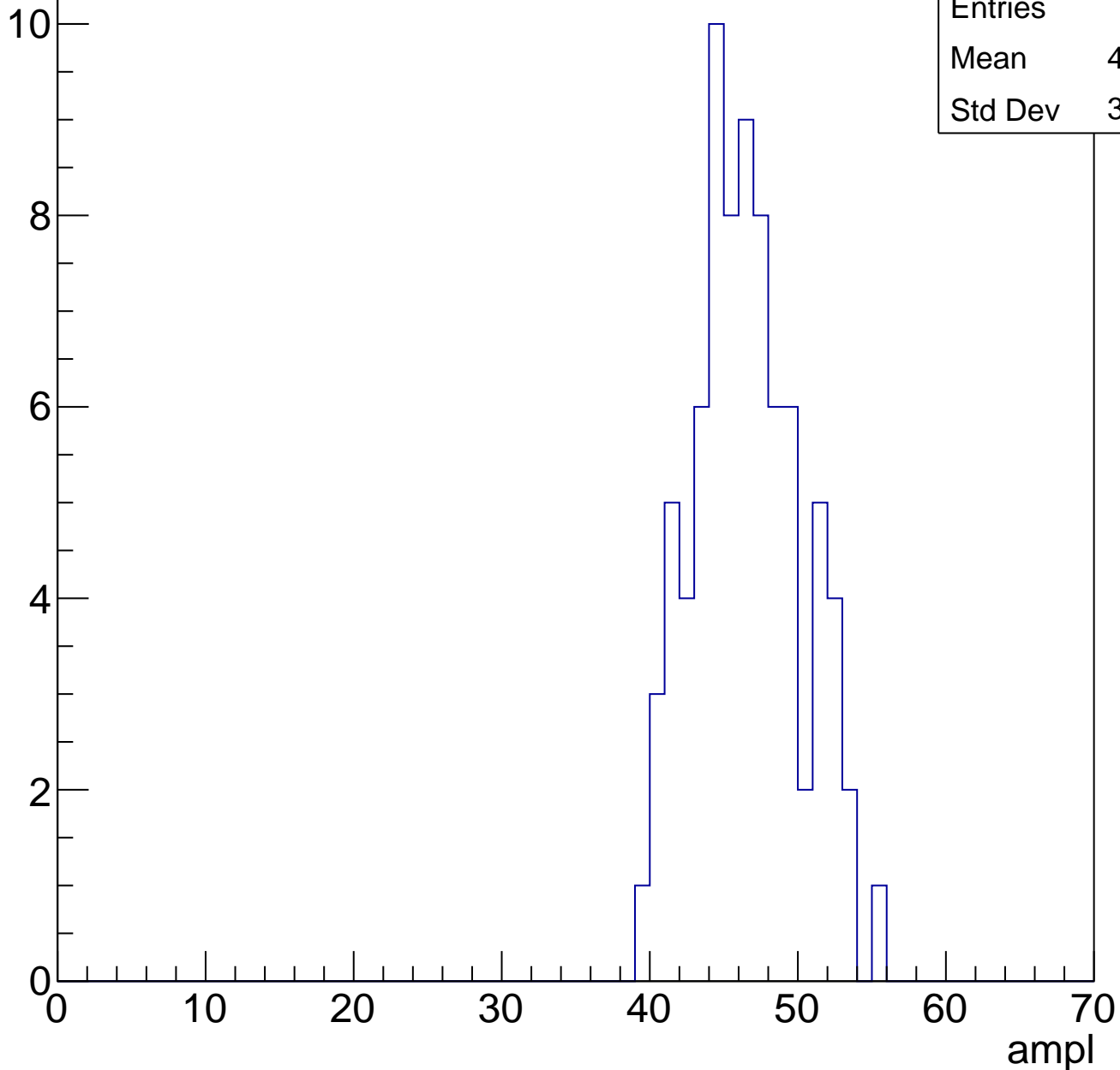


# B1L103S, U3-ch126, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	80
Mean	46.08
Std Dev	3.559

Entry

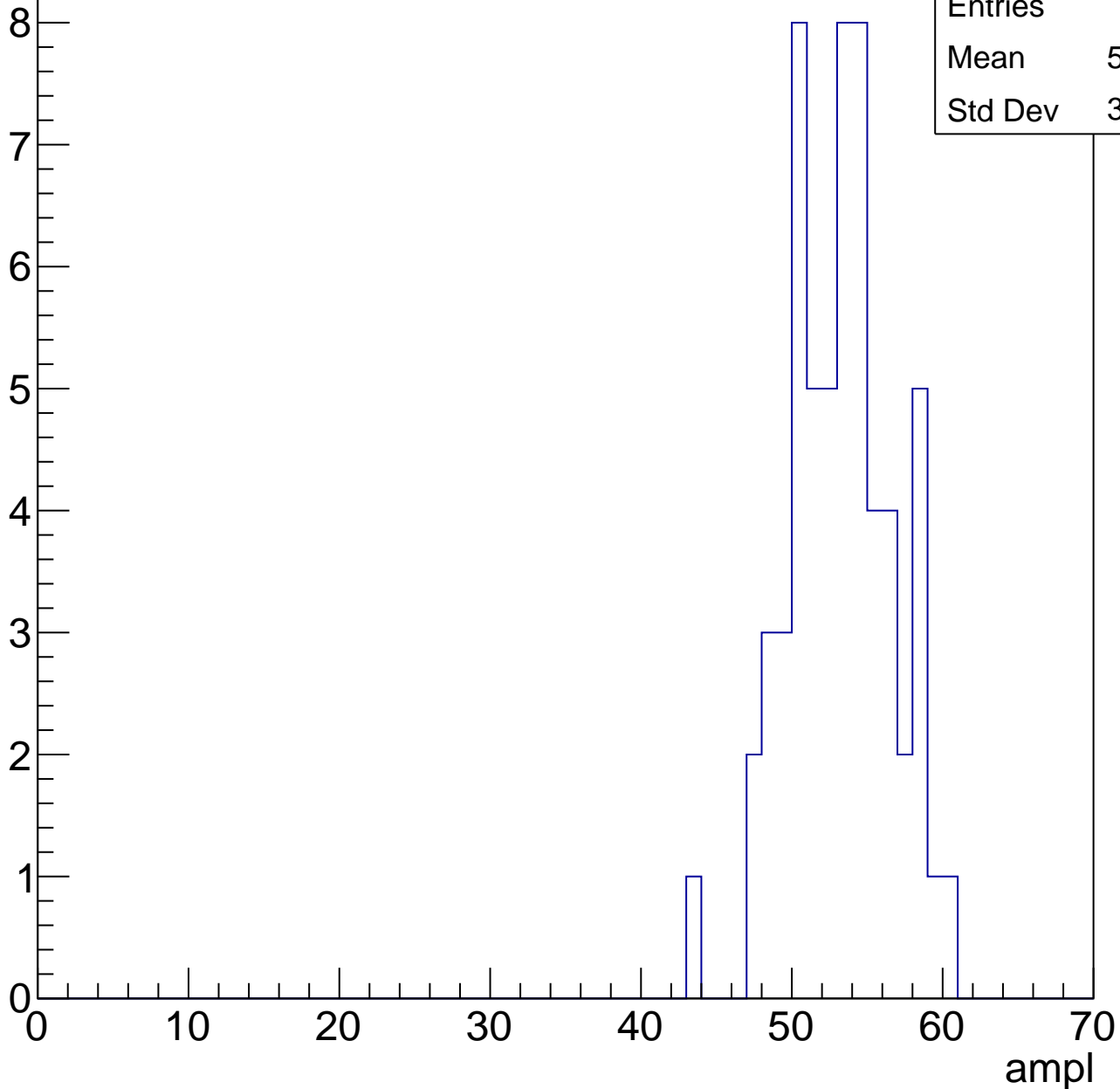


# B1L103S, U3-ch126, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

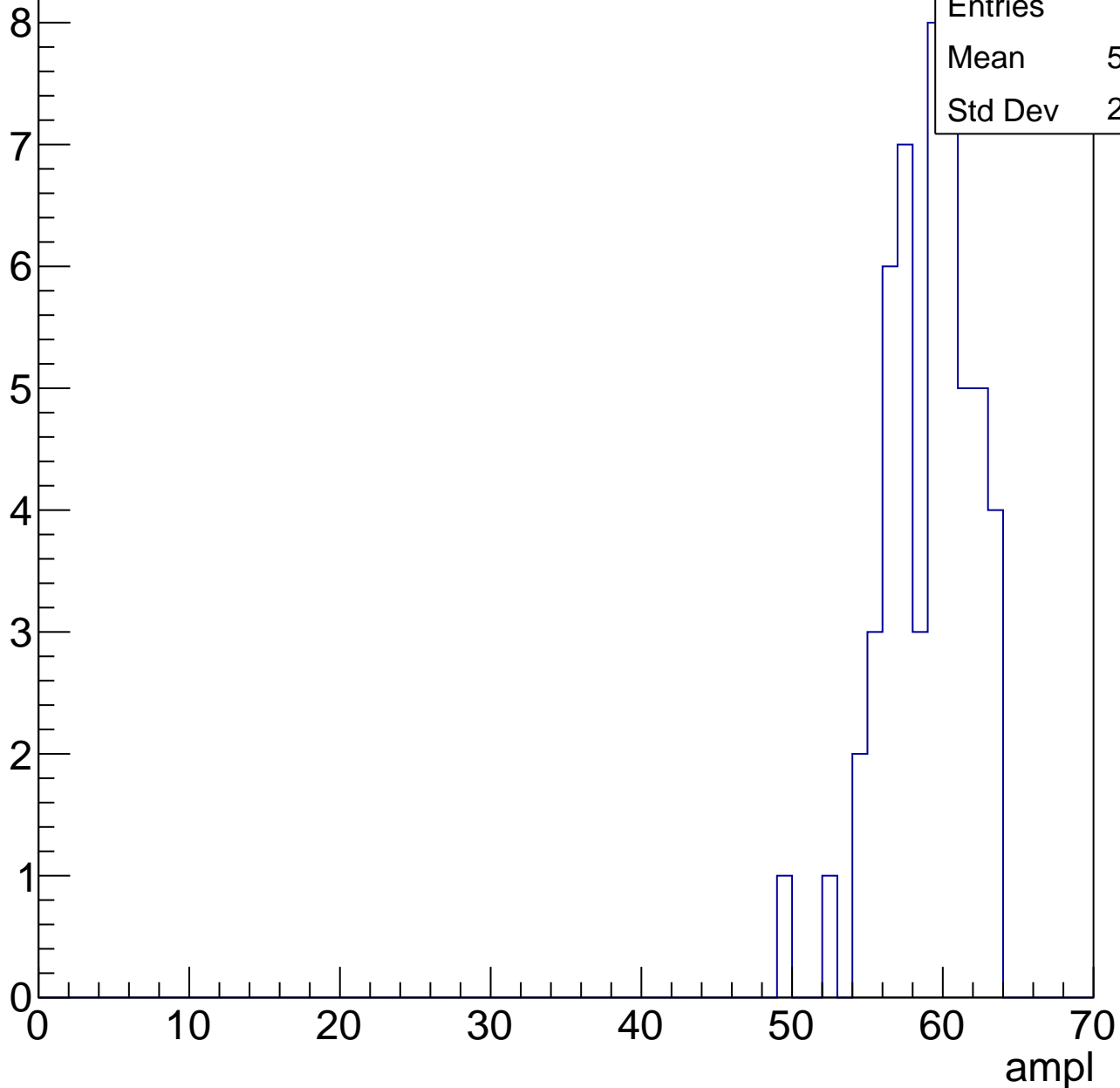
Entries	60
Mean	52.77
Std Dev	3.393



# B1L103S, U3-ch126, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

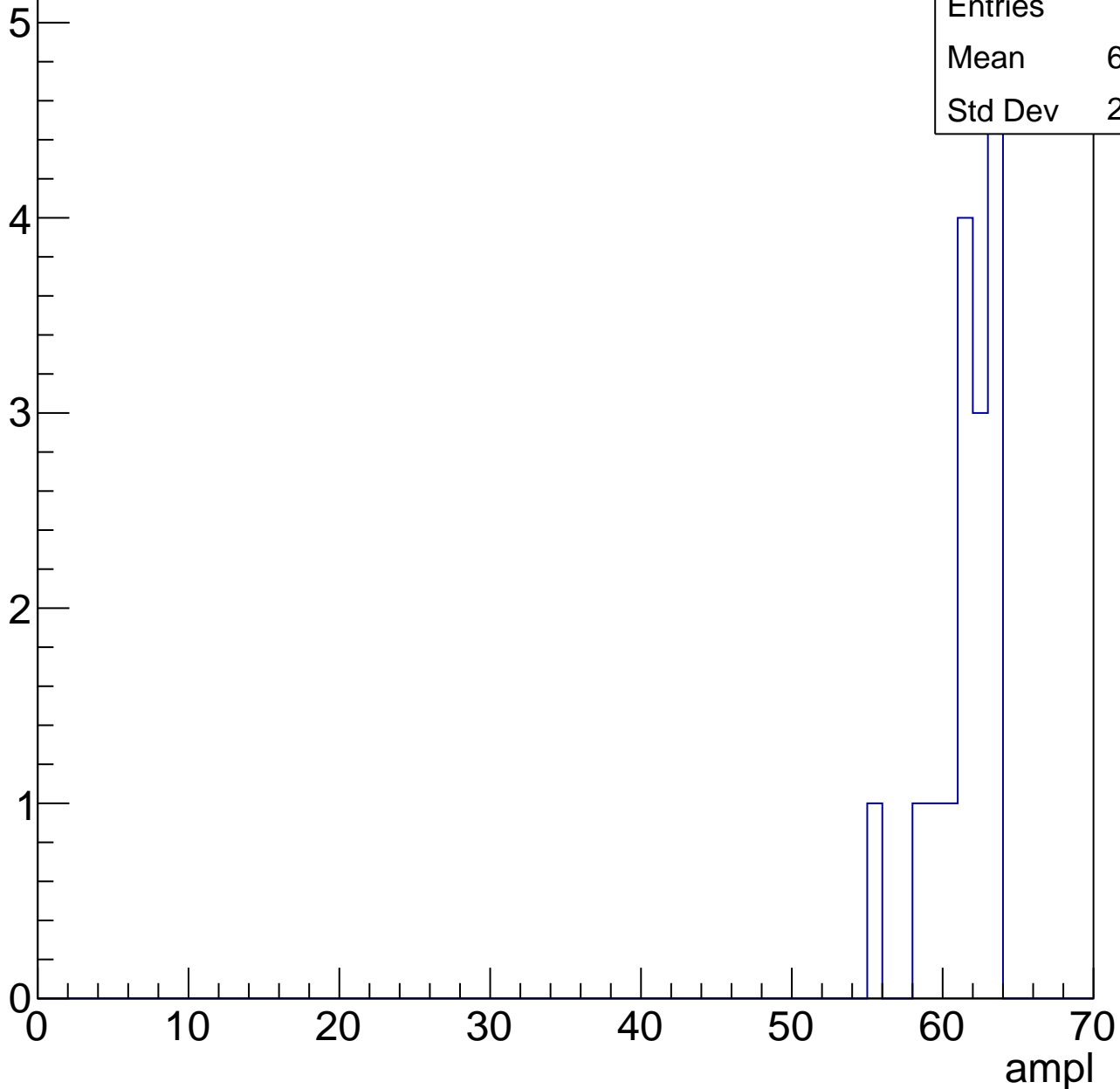


# B1L103S, U3-ch126, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	16
Mean	61.06
Std Dev	2.135







# B1L103S, U3-ch127, adc0

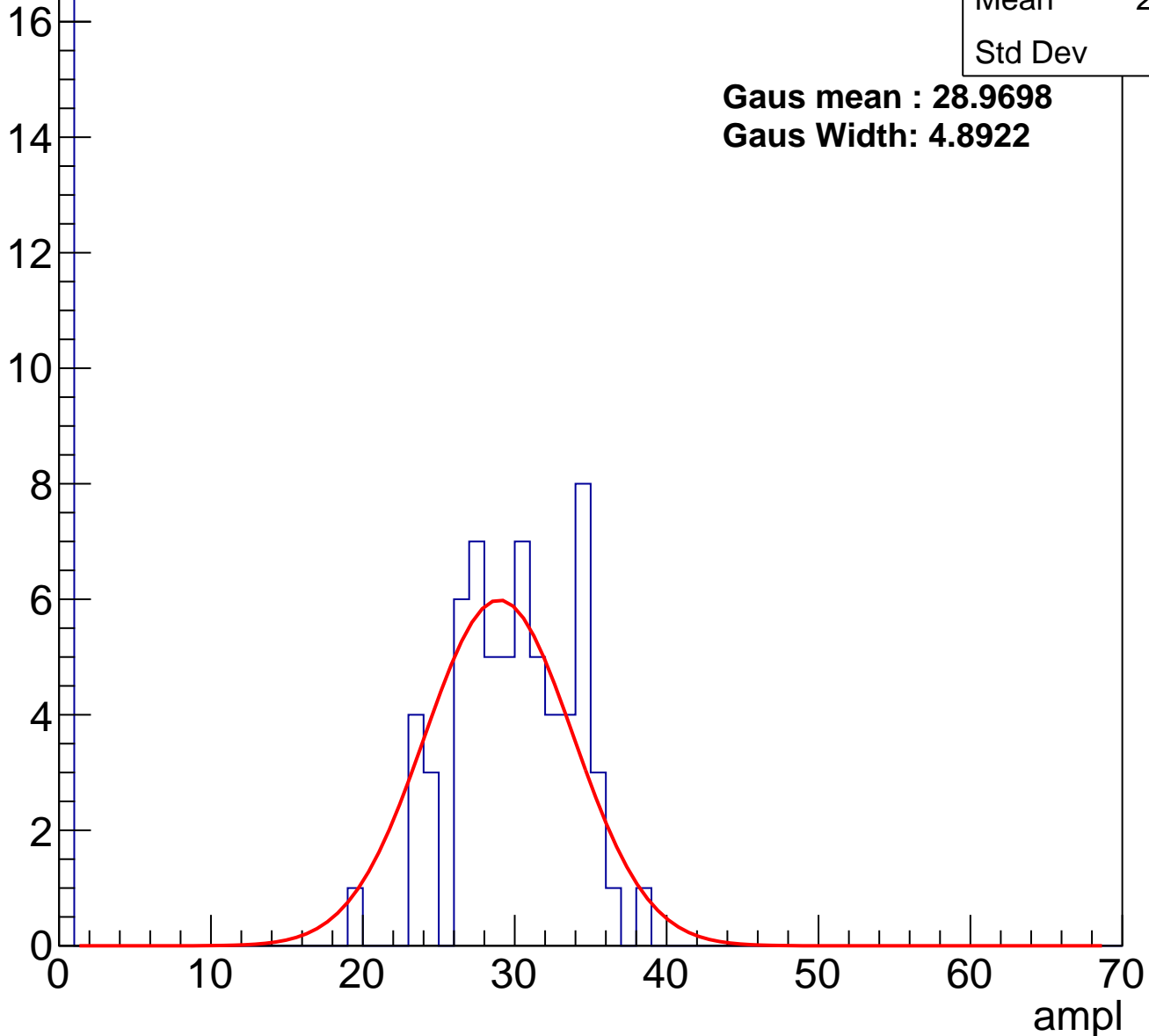
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	81
Mean	23.32
Std Dev	12.5

**Gaus mean : 28.9698**

**Gaus Width: 4.8922**

Entry



# B1L103S, U3-ch127, adc1

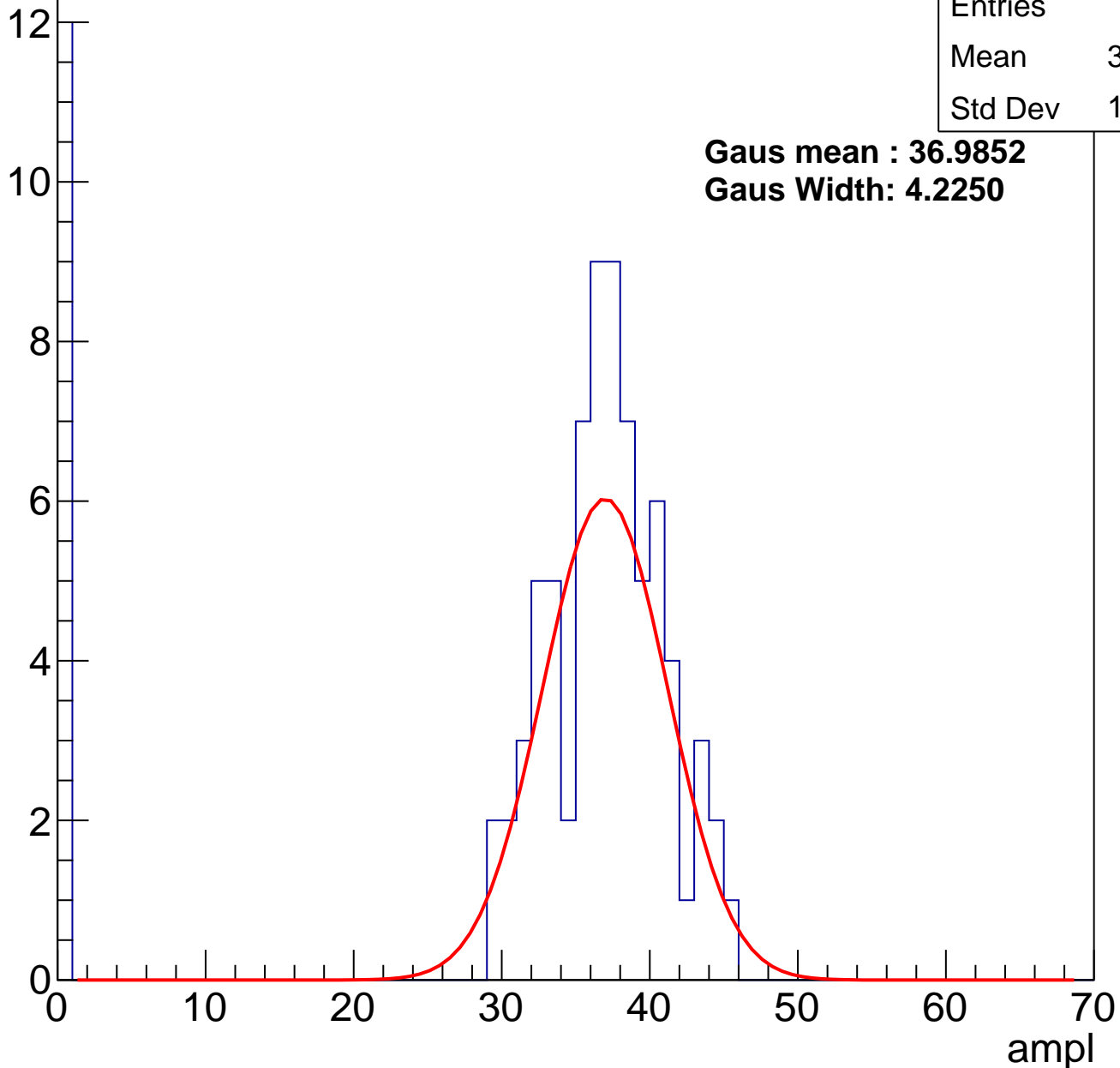
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	85
Mean	31.47
Std Dev	13.22

**Gaus mean : 36.9852**

**Gaus Width: 4.2250**

Entry



# B1L103S, U3-ch127, adc2

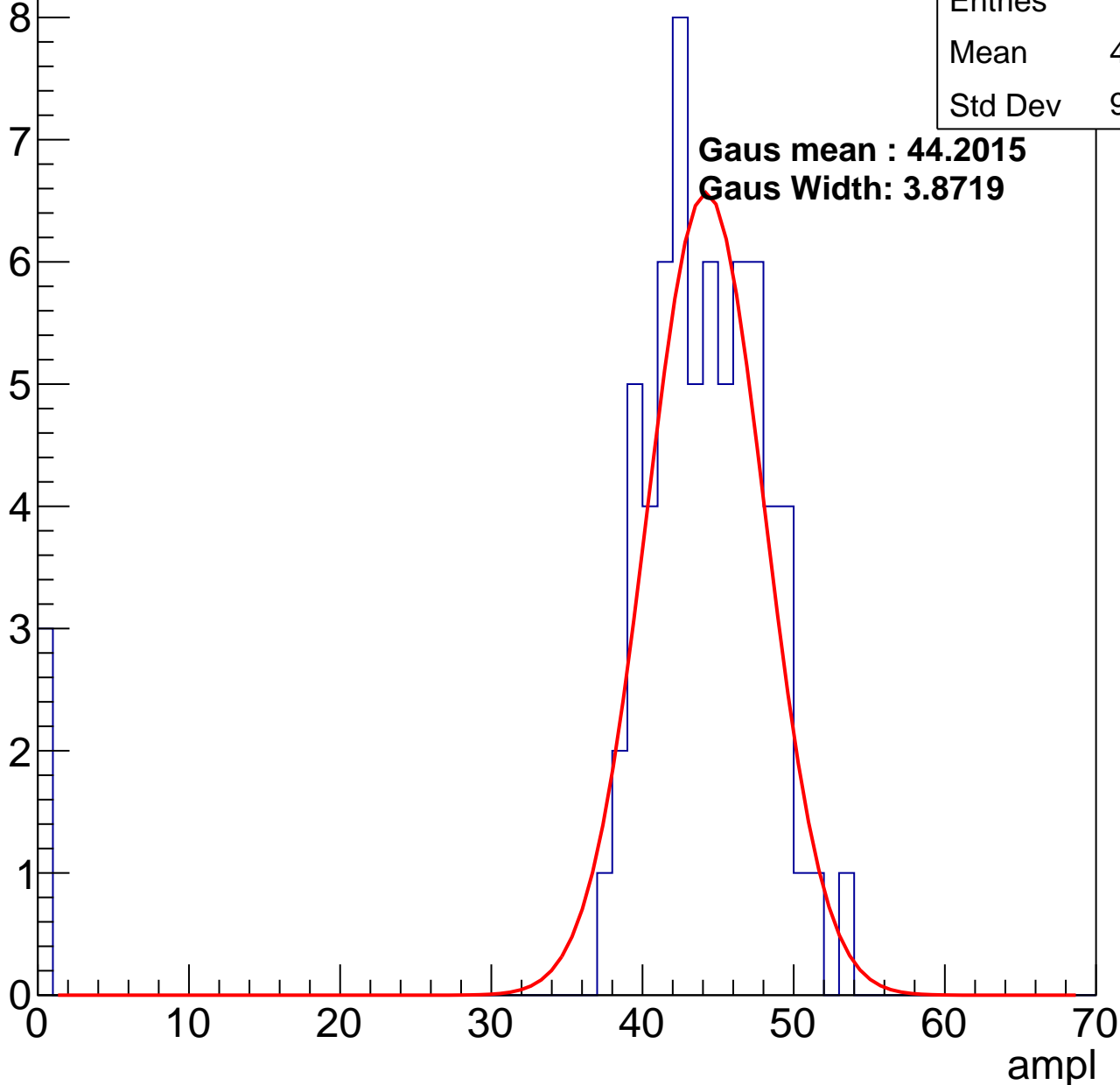
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	68
Mean	41.97
Std Dev	9.657

**Gaus mean : 44.2015**

**Gaus Width: 3.8719**

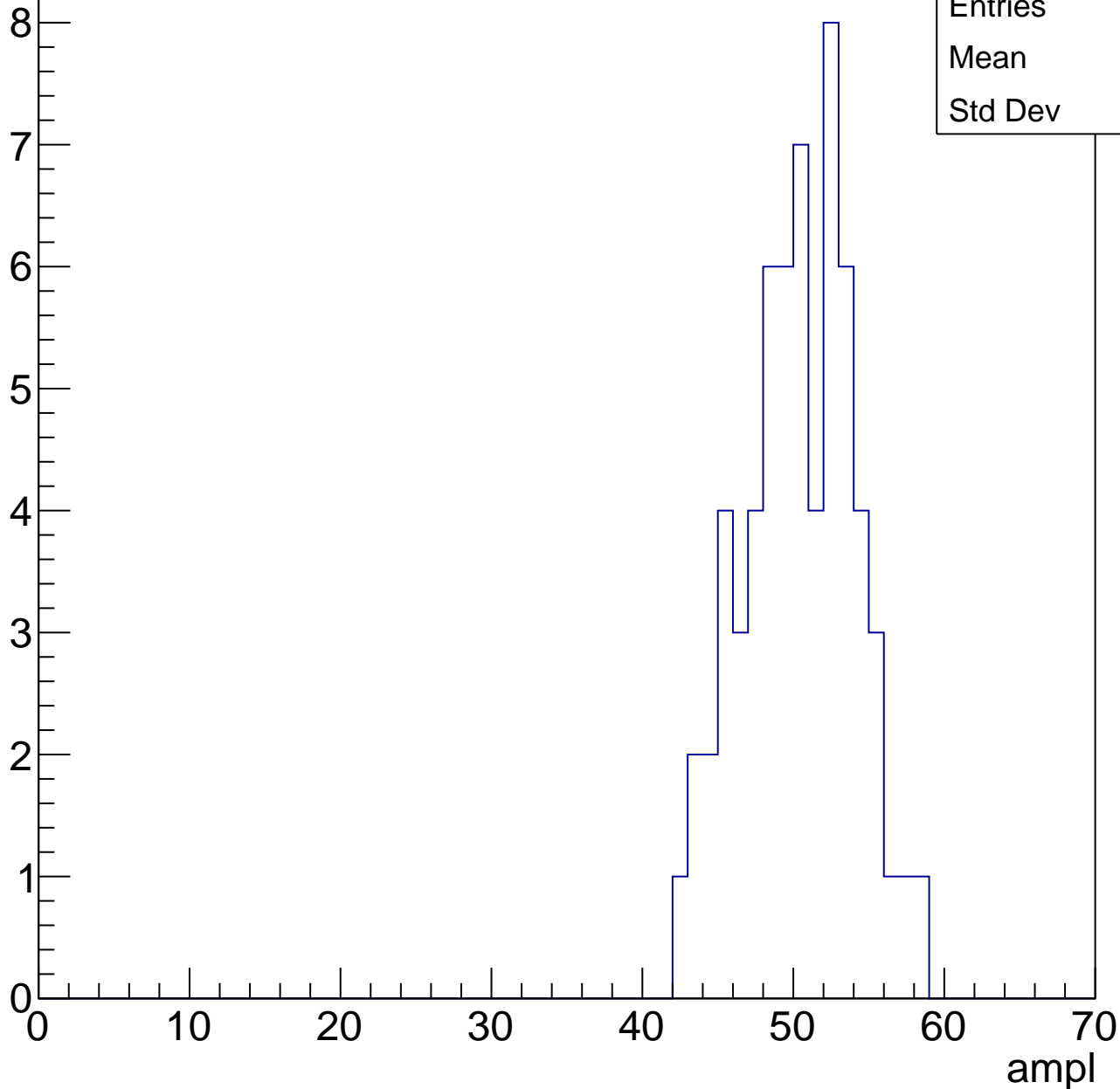


# B1L103S, U3-ch127, adc3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	49.9
Std Dev	3.62

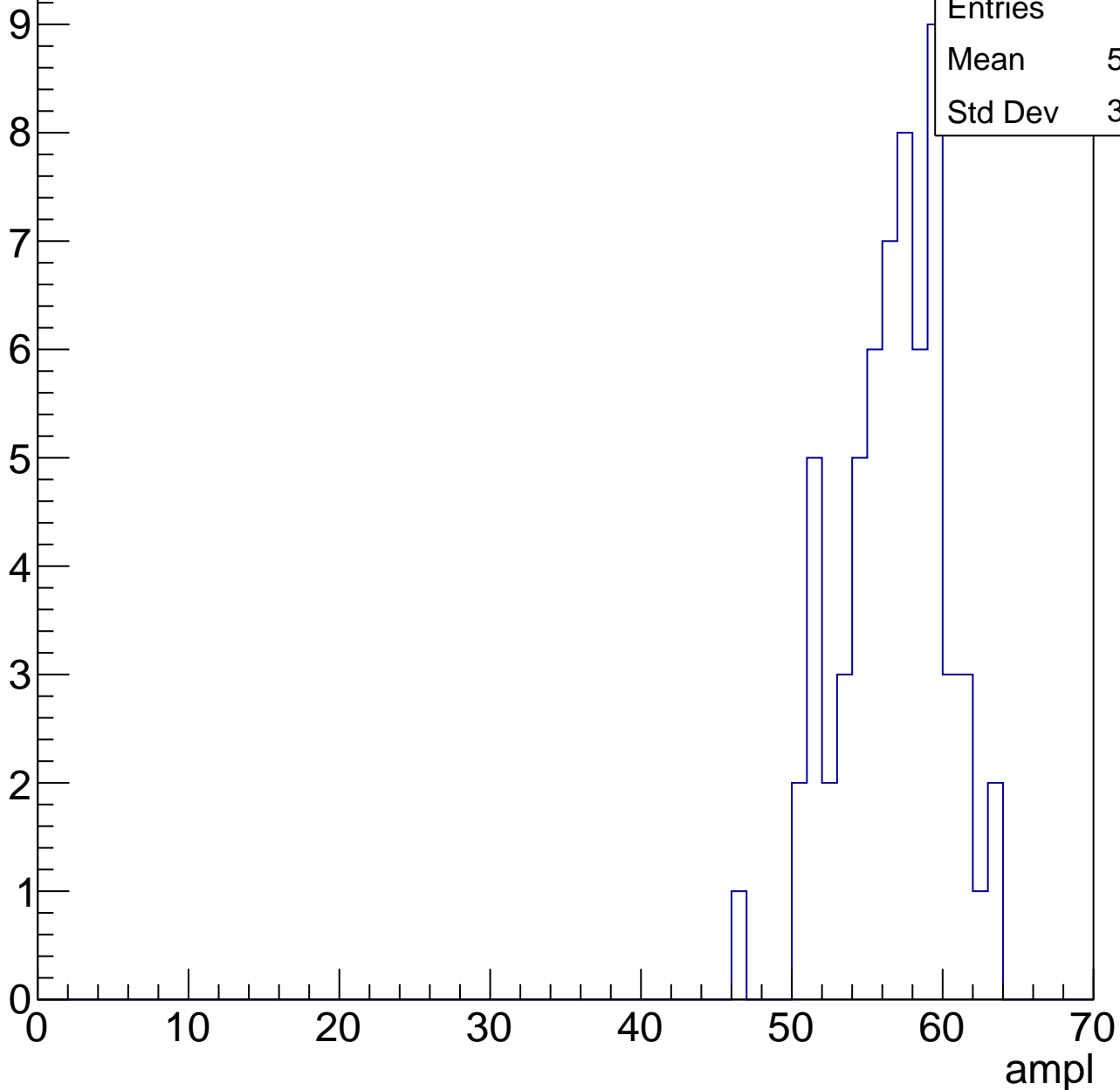


# B1L103S, U3-ch127, adc4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

Entries	63
Mean	56.22
Std Dev	3.448

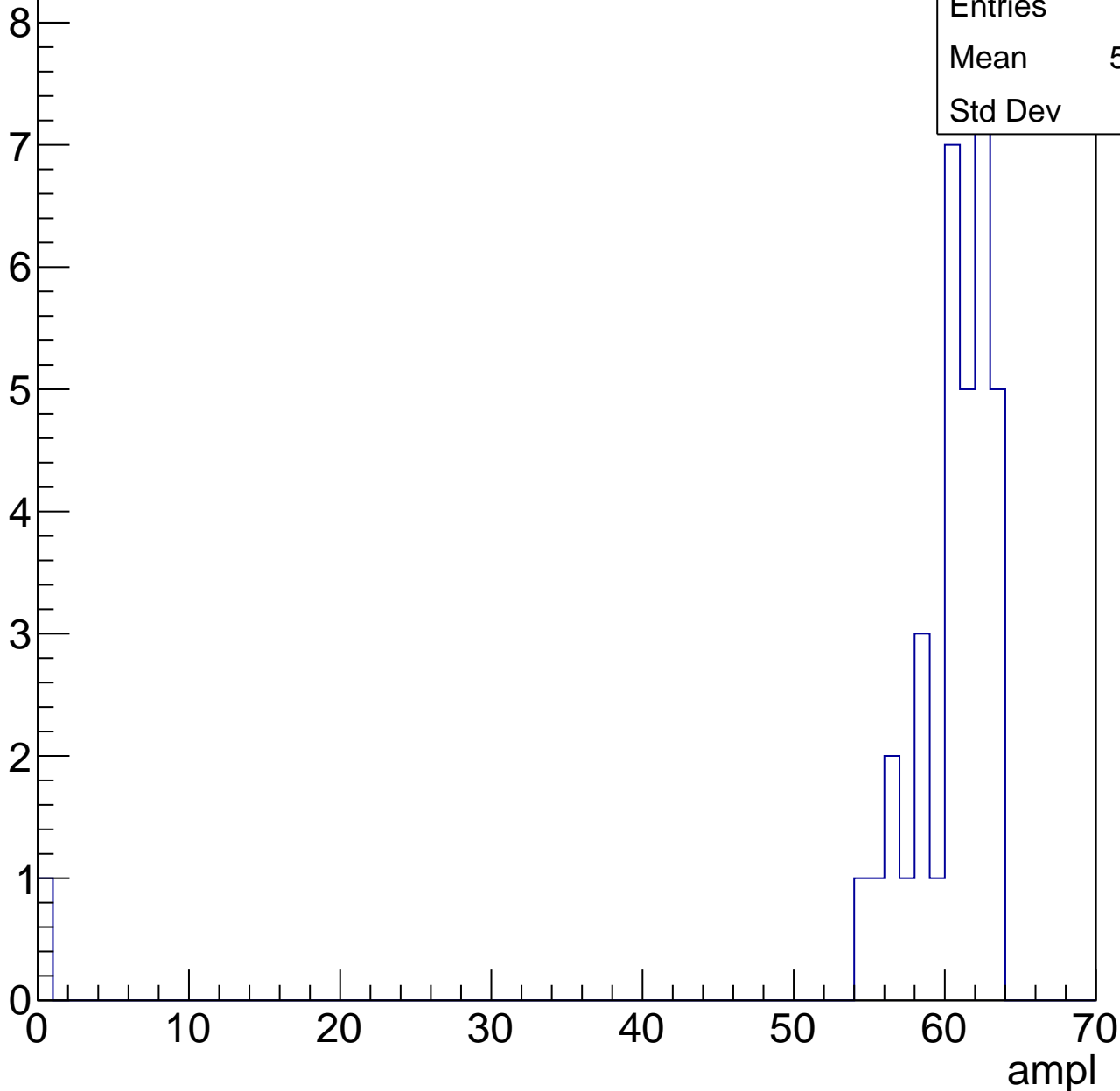


# B1L103S, U3-ch127, adc5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

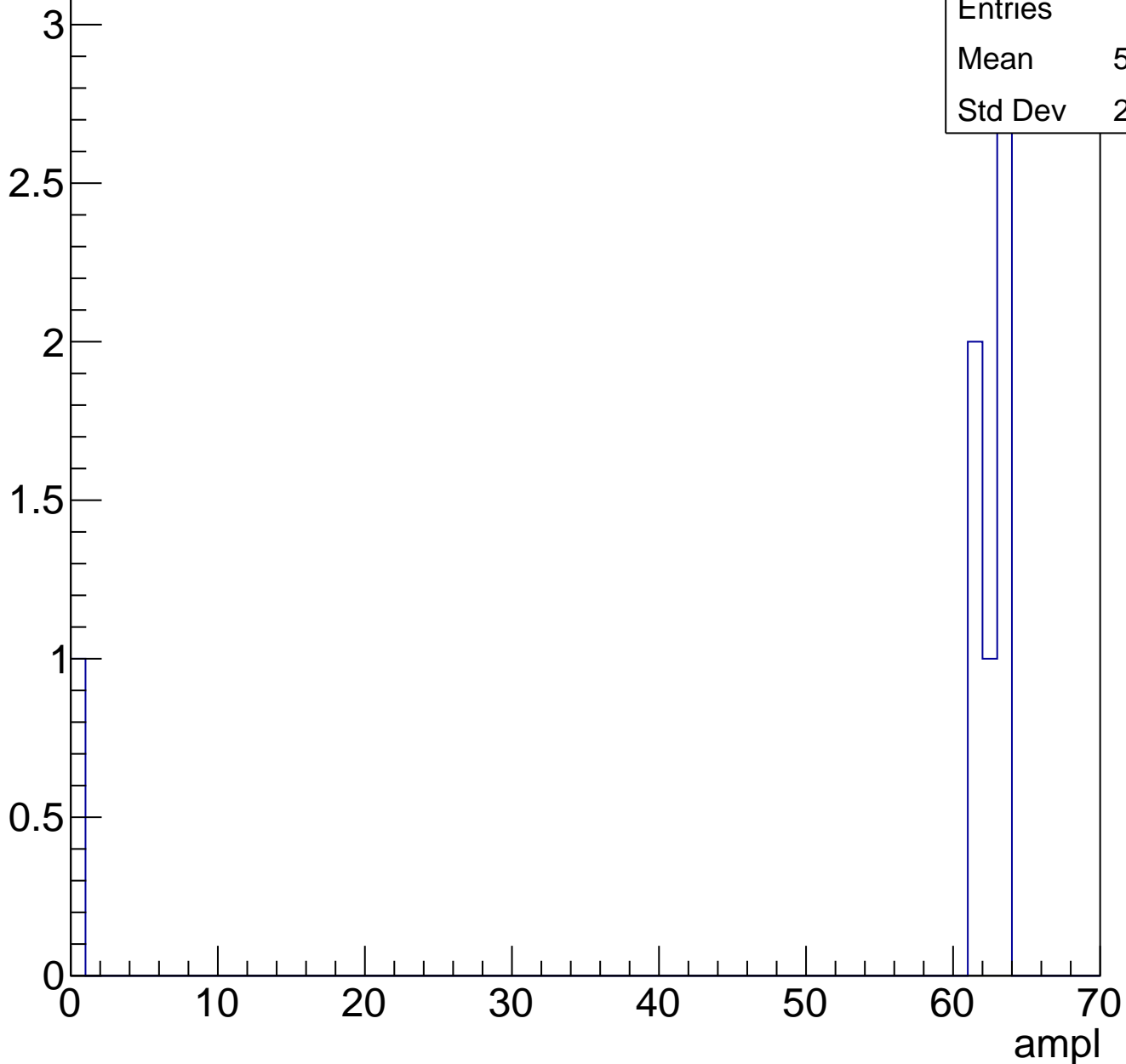
Entries	35
Mean	58.49
Std Dev	10.3



# B1L103S, U3-ch127, adc6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



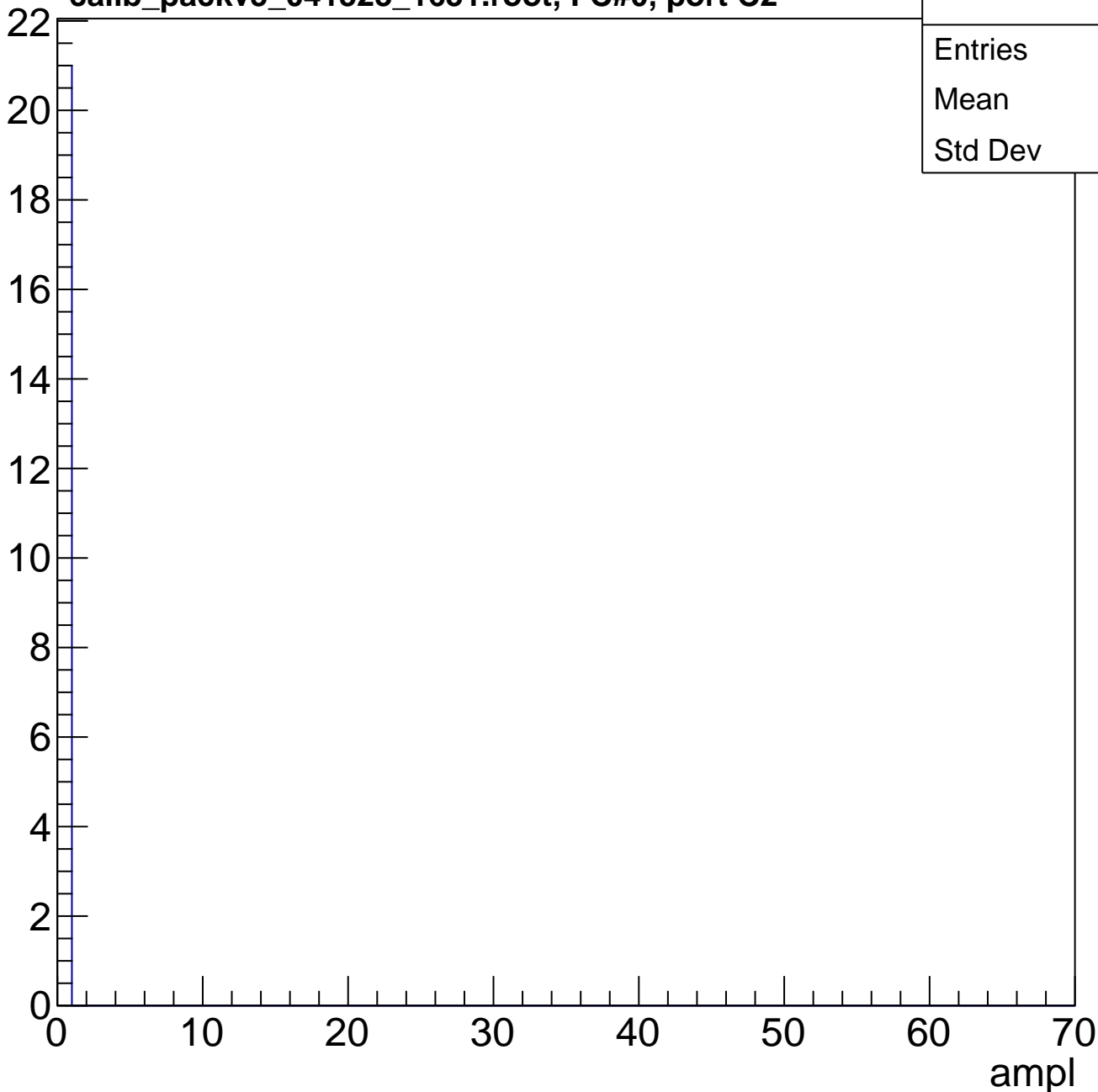
Entries	7
Mean	53.29
Std Dev	21.77



# B1L103S, U3-ch127, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry



Entries	21
Mean	0
Std Dev	0

# B1L103S, U3-ch127, adc7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	21
Mean	0
Std Dev	0

