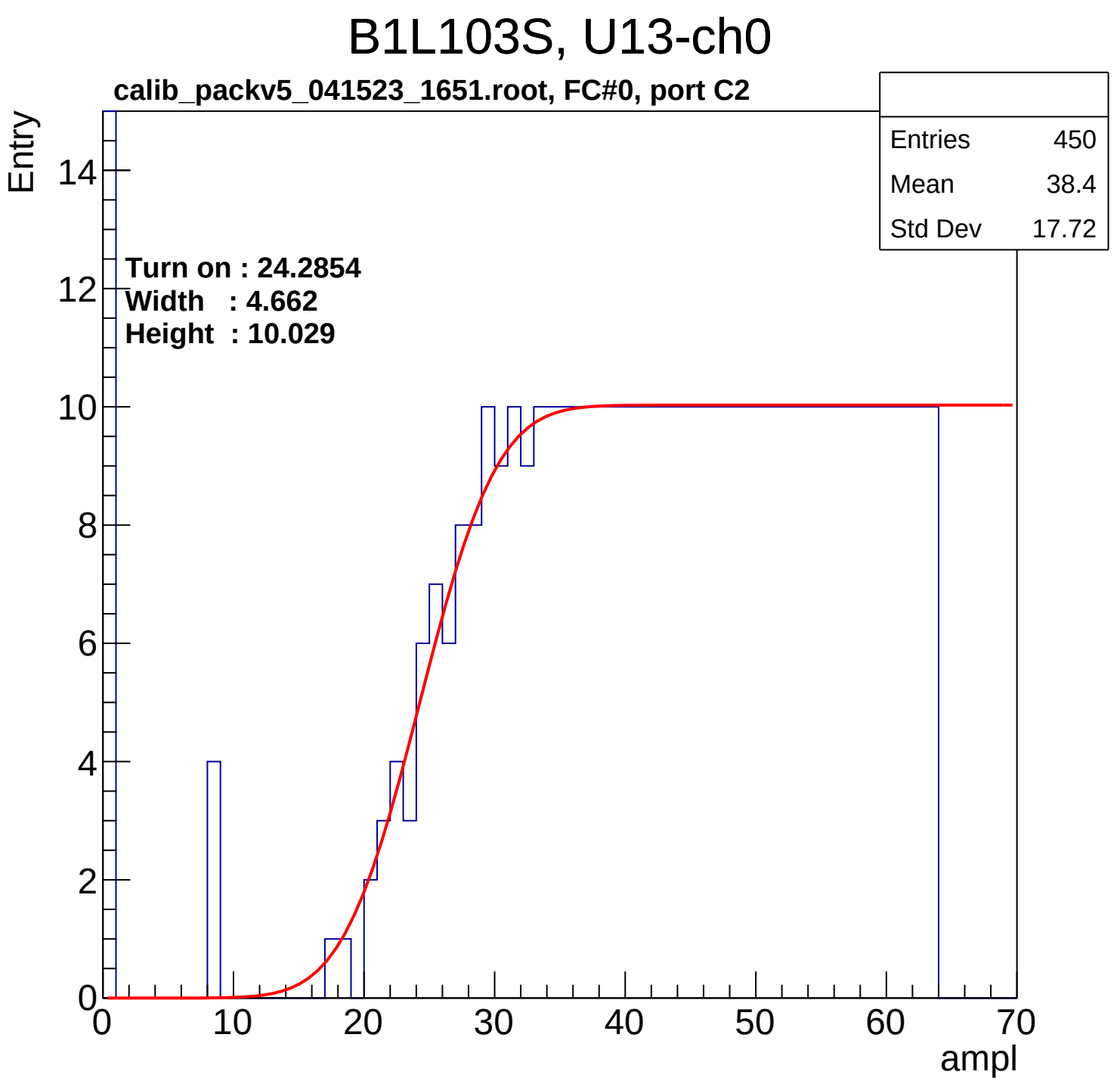
B1L103S, U13-ch0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 450
Mean 38.4
Std Dev 17.72
Turn on : 24.2854
Width : 4.662
Height : 10.029
Entry
ampl
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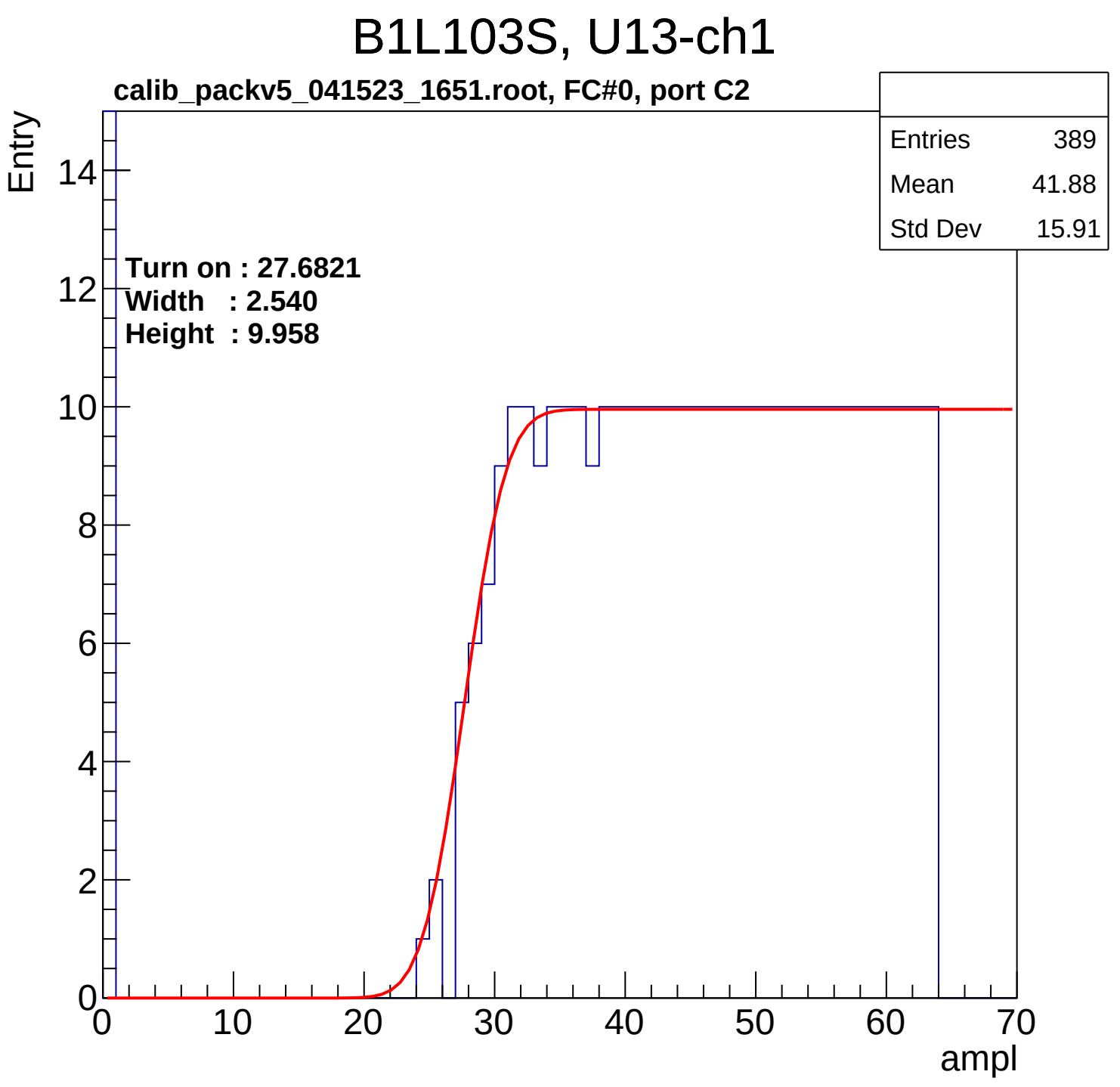
B1L103S, U13-ch1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 389
Mean 41.88
Std Dev 15.91
Turn on : 27.6821
Width : 2.540
Height : 9.958
Entry
ampl
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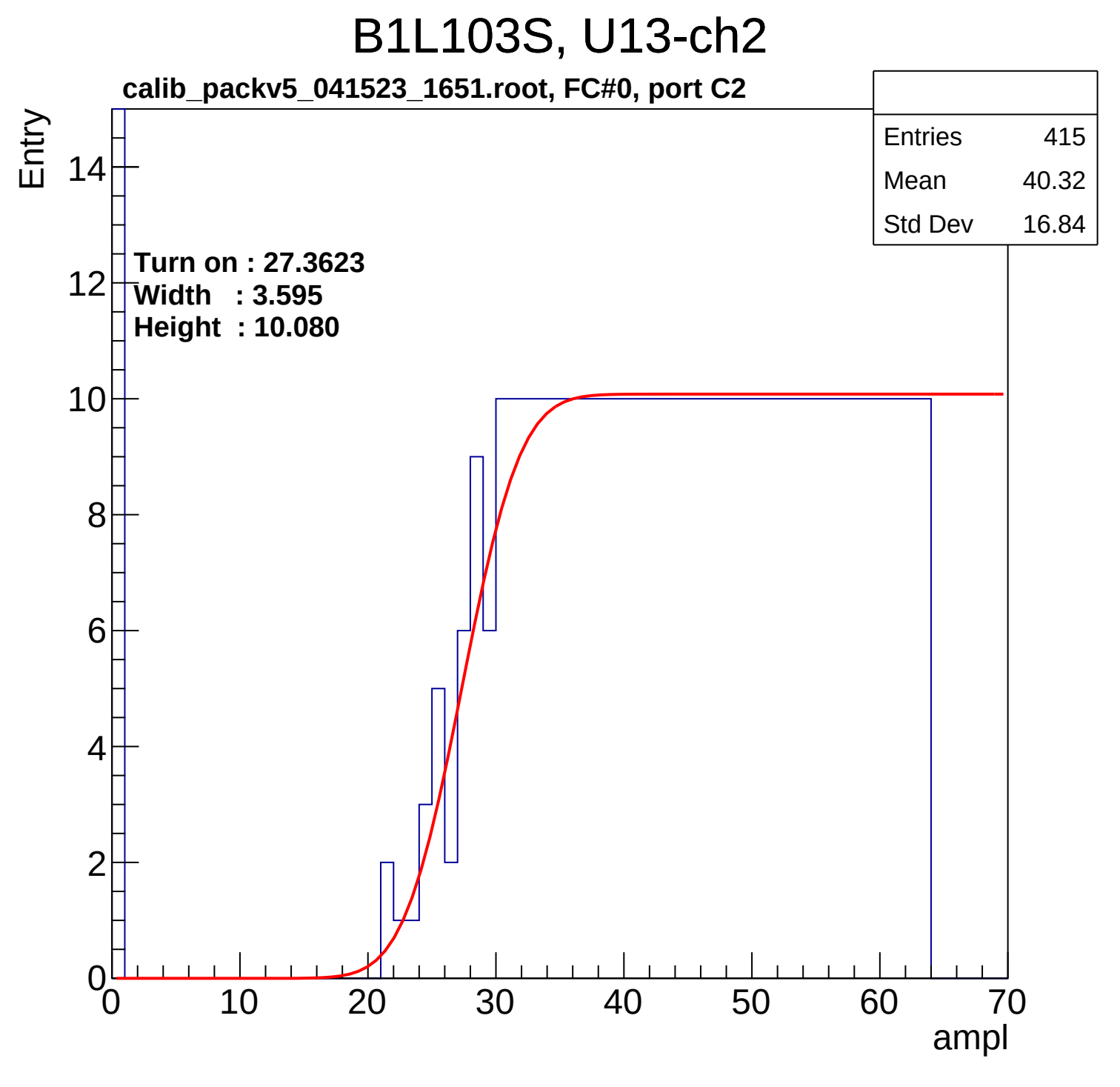
B1L103S, U13-ch2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 415
Mean 40.32
Std Dev 16.84
Turn on : 27.3623
Width : 3.595
Height : 10.080
Entry
ampl
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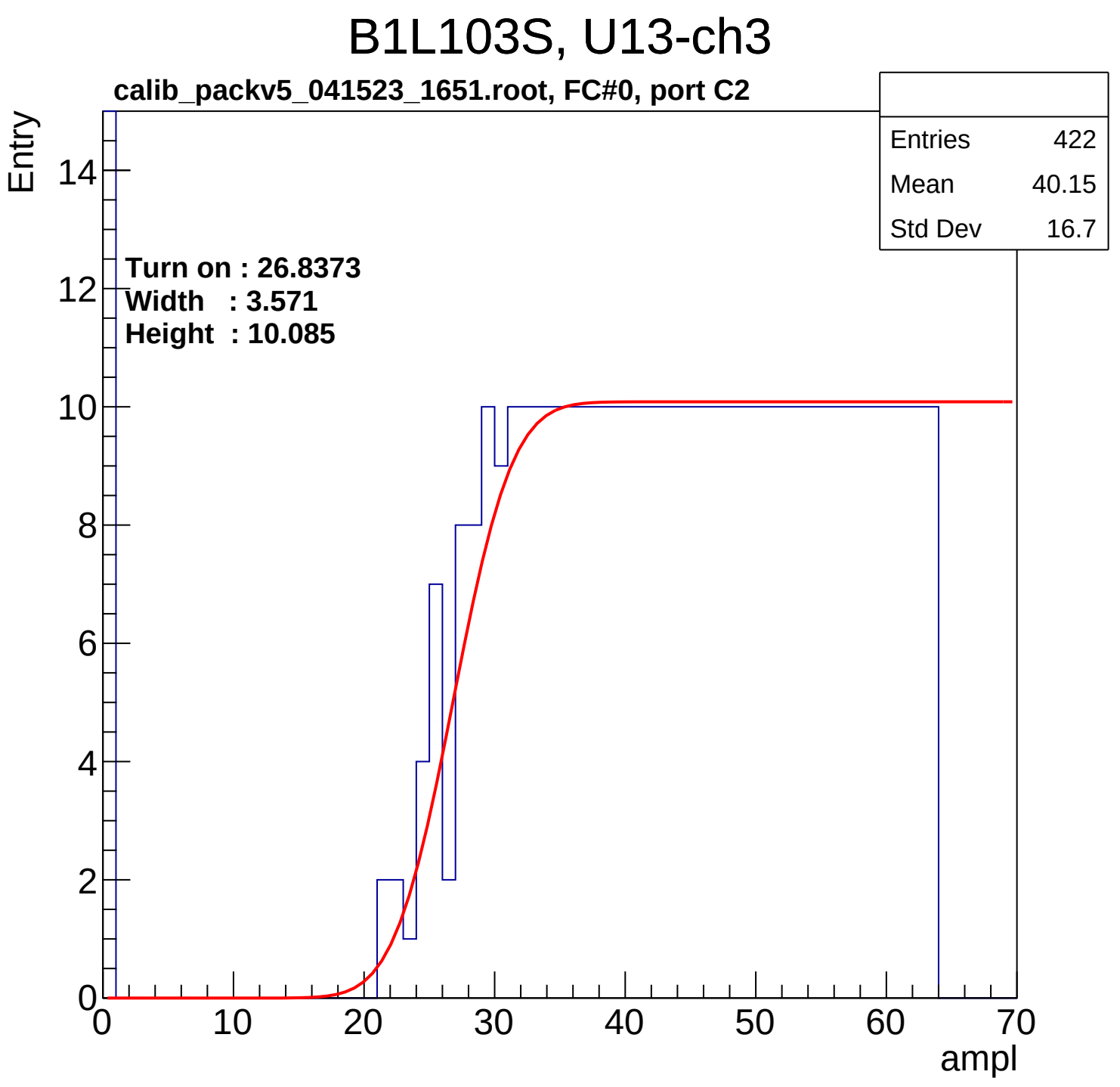
B1L103S, U13-ch3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 422
Mean 40.15
Std Dev 16.7
Turn on : 26.8373
Width : 3.571
Height : 10.085
Entry
ampl
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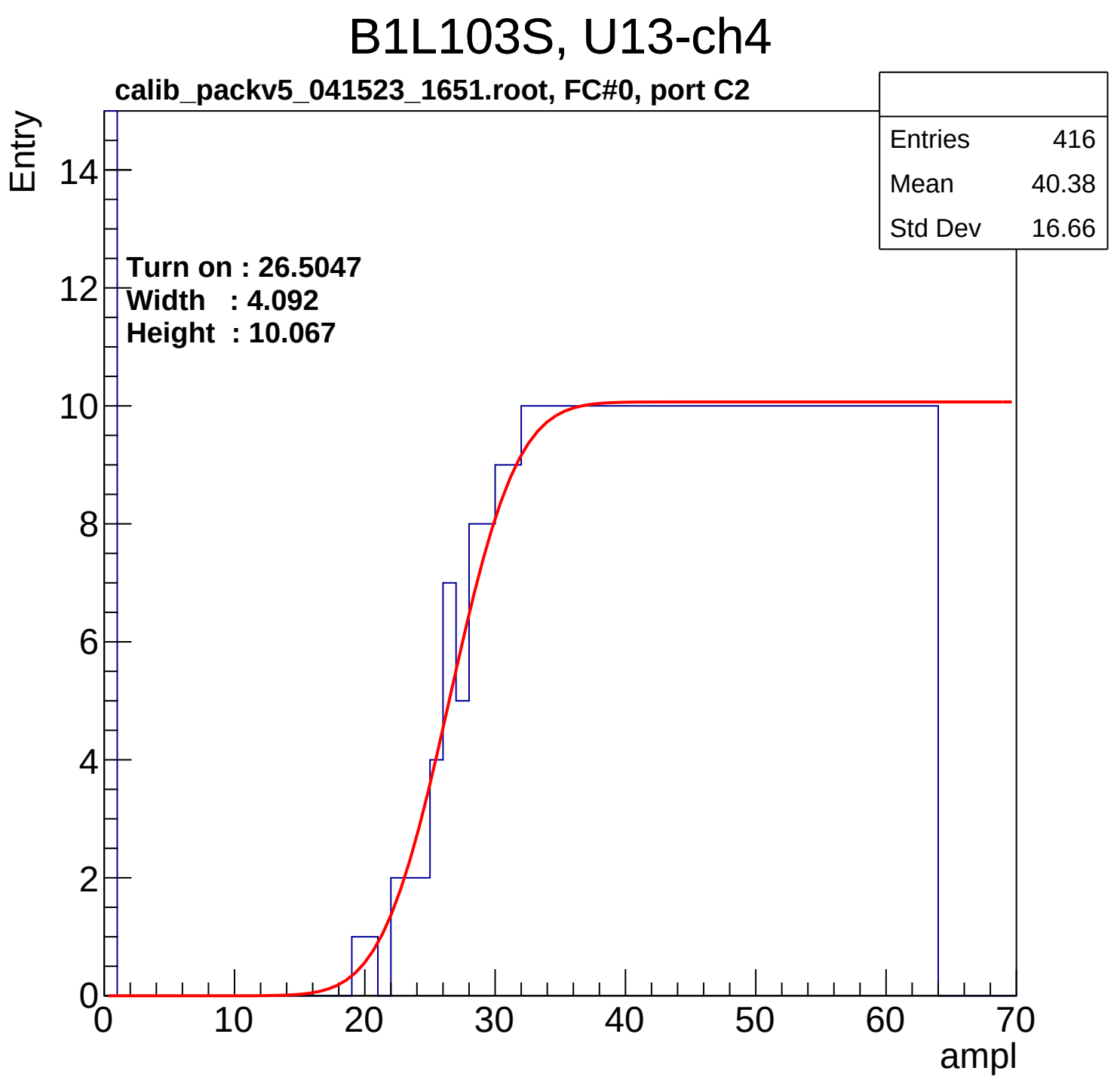
B1L103S, U13-ch4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 416
Mean 40.38
Std Dev 16.66
Turn on : 26.5047
Width : 4.092
Height : 10.067
Entry
ampl
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2
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8
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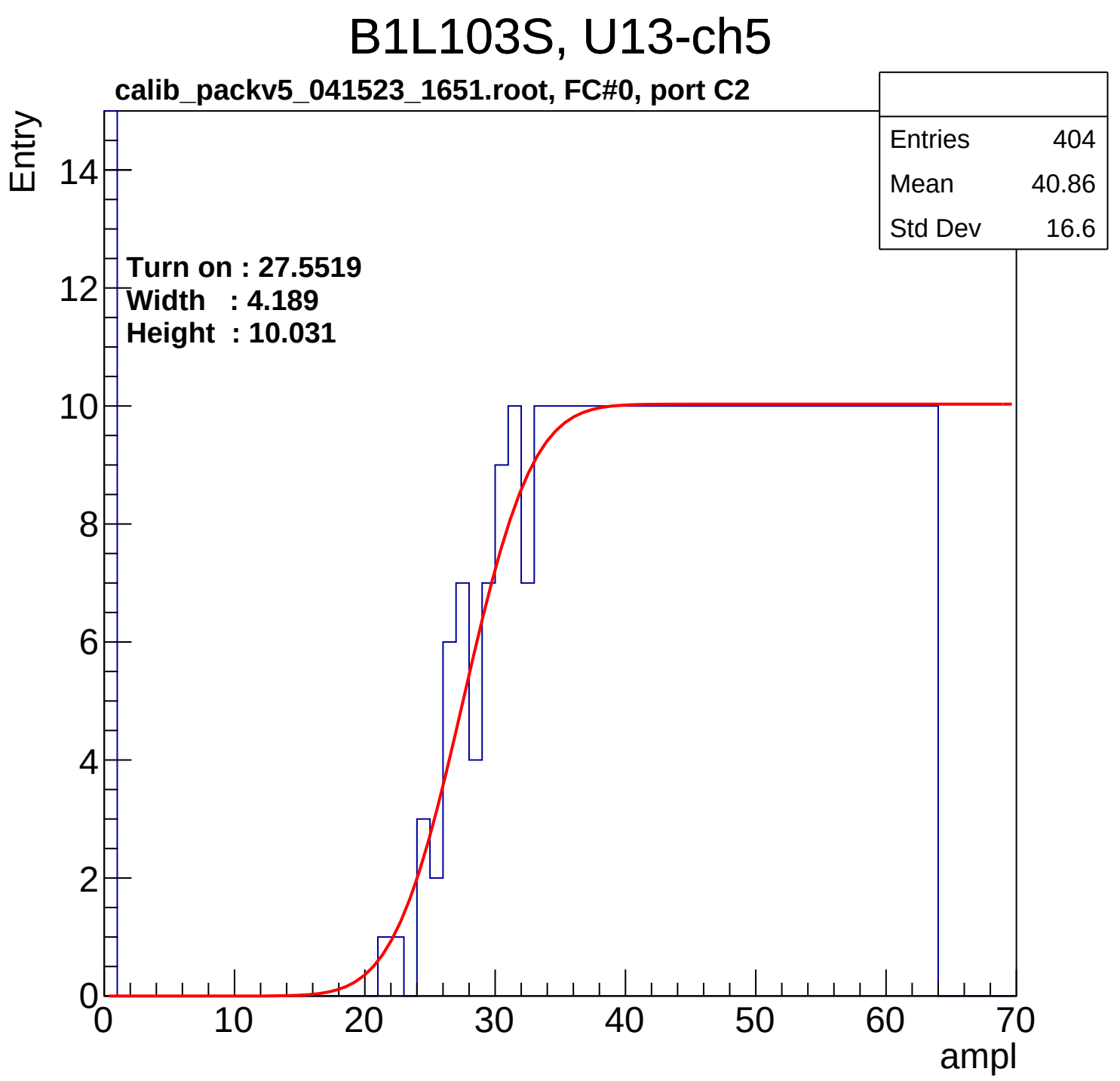
B1L103S, U13-ch5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 404
Mean 40.86
Std Dev 16.6
Turn on : 27.5519
Width : 4.189
Height : 10.031
Entry
ampl
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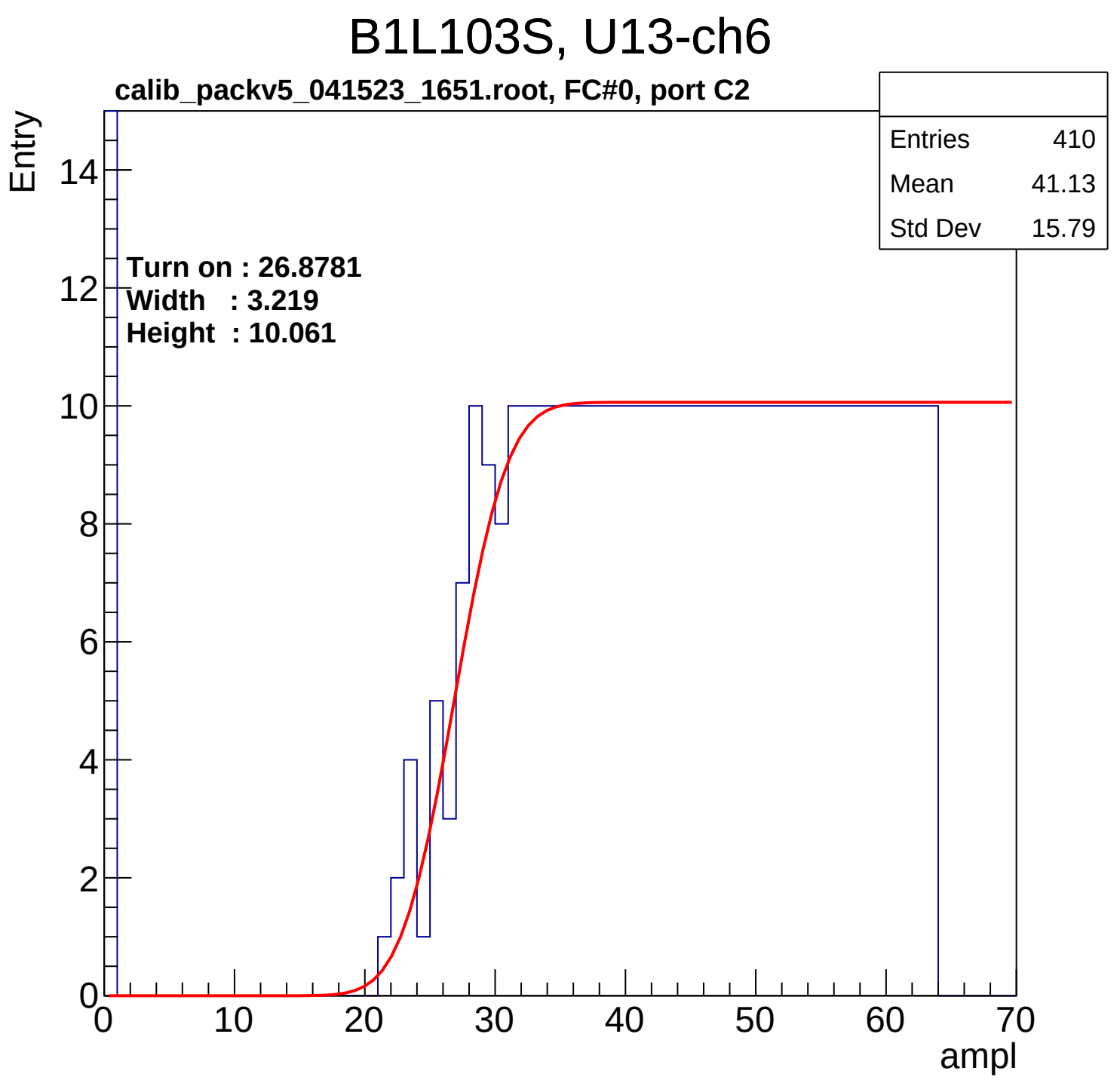
B1L103S, U13-ch6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 410
Mean 41.13
Std Dev 15.79
Turn on : 26.8781
Width : 3.219
Height : 10.061
Entry
ampl
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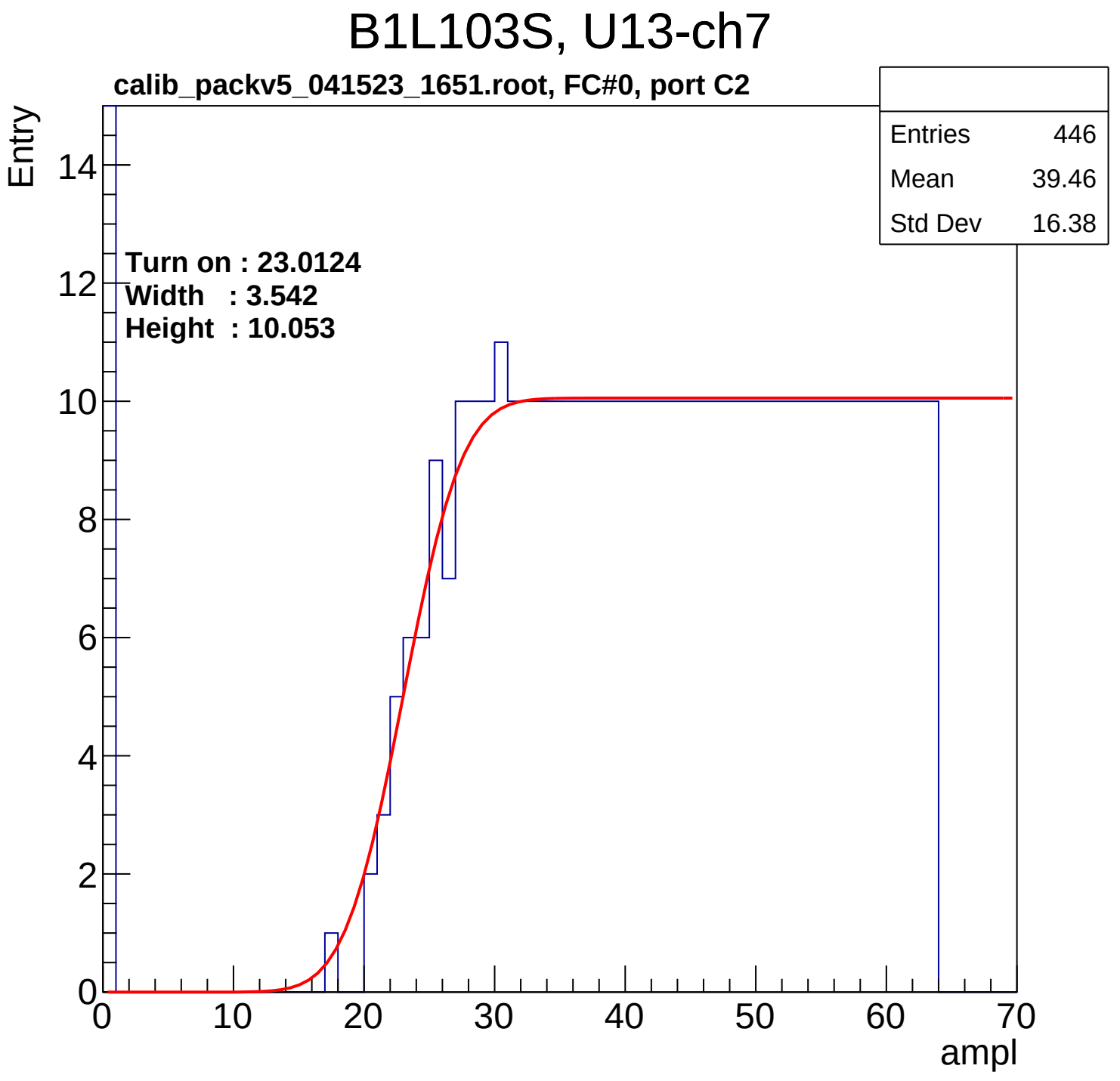
B1L103S, U13-ch7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 446
Mean 39.46
Std Dev 16.38
Turn on : 23.0124
Width : 3.542
Height : 10.053
Entry
ampl
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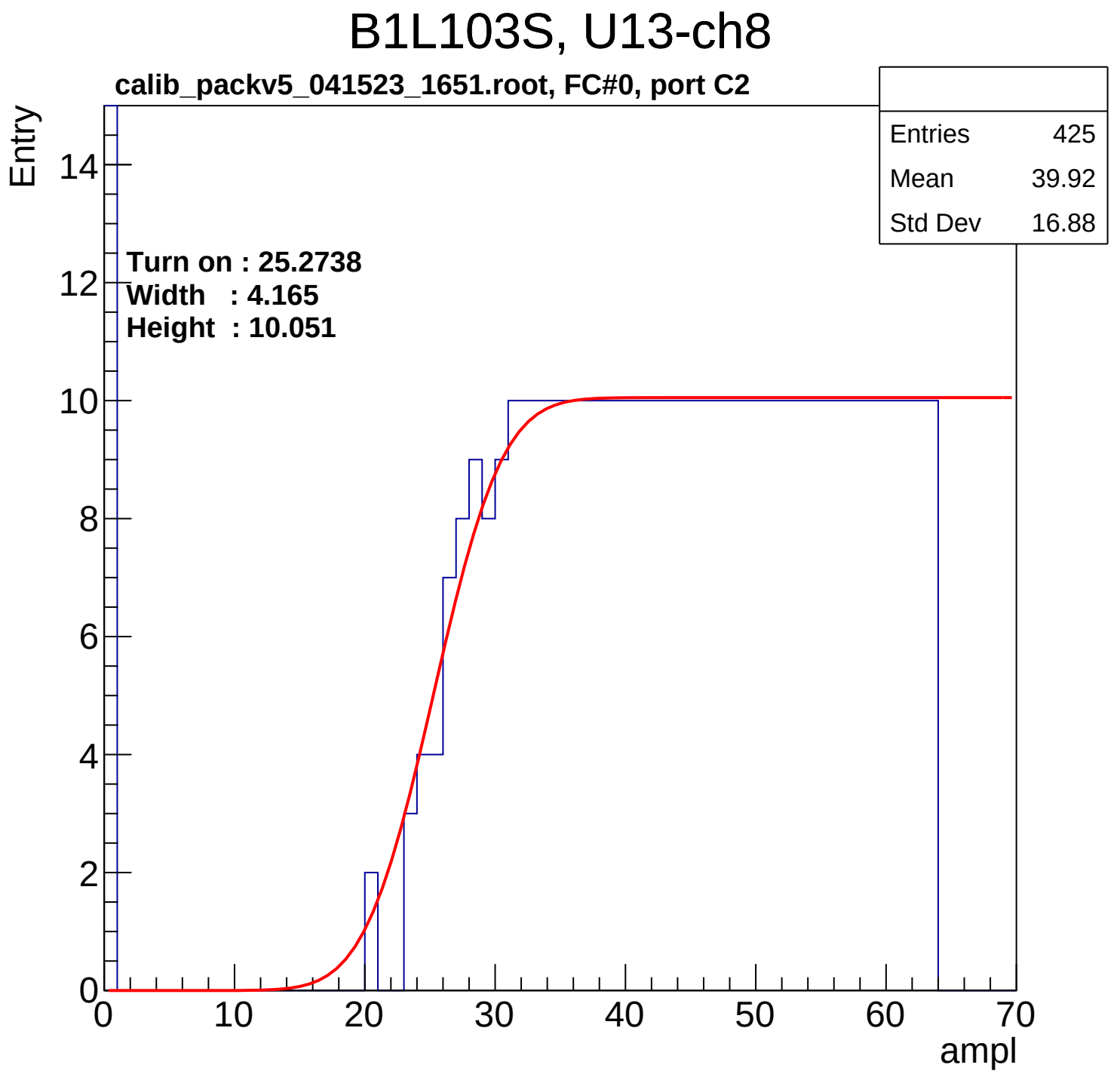
B1L103S, U13-ch8
calib_packv5_041523_1651.root, FC#0, port C2
Entries 425
Mean 39.92
Std Dev 16.88
Turn on : 25.2738
Width : 4.165
Height : 10.051
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ampl
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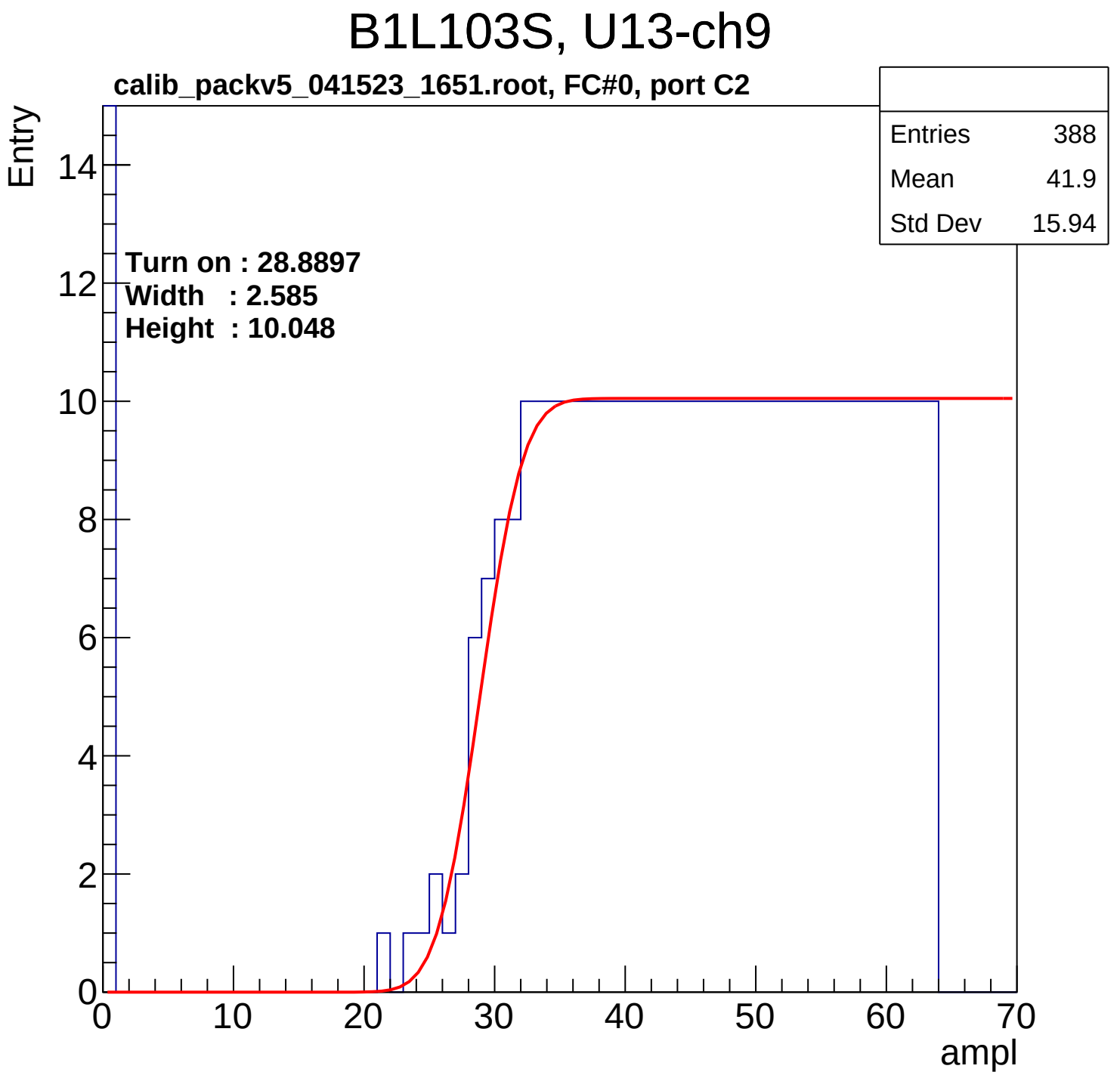
B1L103S, U13-ch9
calib_packv5_041523_1651.root, FC#0, port C2
Entries 388
Mean 41.9
Std Dev 15.94
Turn on : 28.8897
Width : 2.585
Height : 10.048
Entry
ampl
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8
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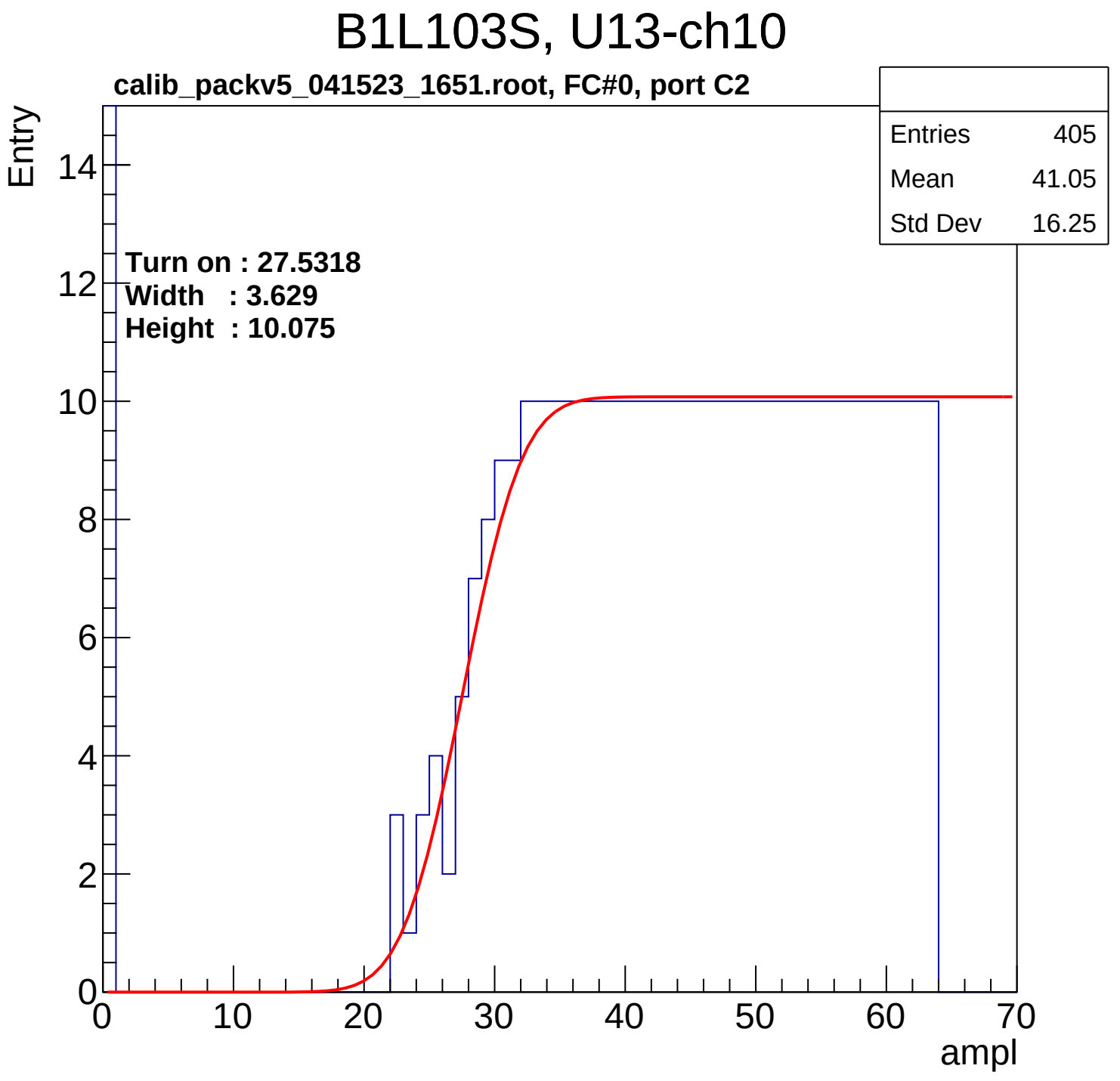
B1L103S, U13-ch10
calib_packv5_041523_1651.root, FC#0, port C2
Entries 405
Mean 41.05
Std Dev 16.25
Turn on : 27.5318
Width : 3.629
Height : 10.075
Entry
ampl
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2
4
6
8
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0
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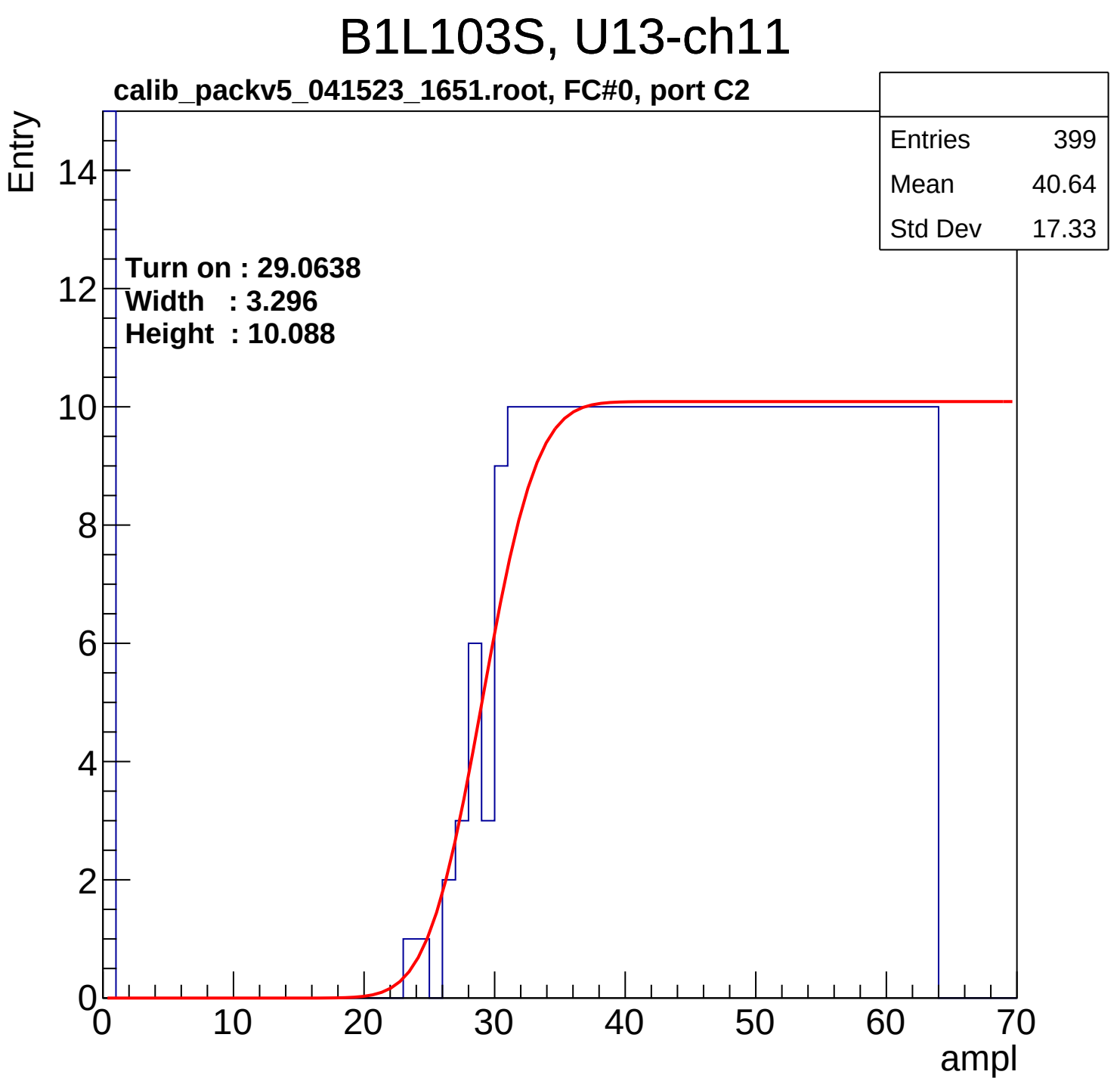
B1L103S, U13-ch11
calib_packv5_041523_1651.root, FC#0, port C2
Entries 399
Mean 40.64
Std Dev 17.33
Turn on : 29.0638
Width : 3.296
Height : 10.088
Entry
ampl
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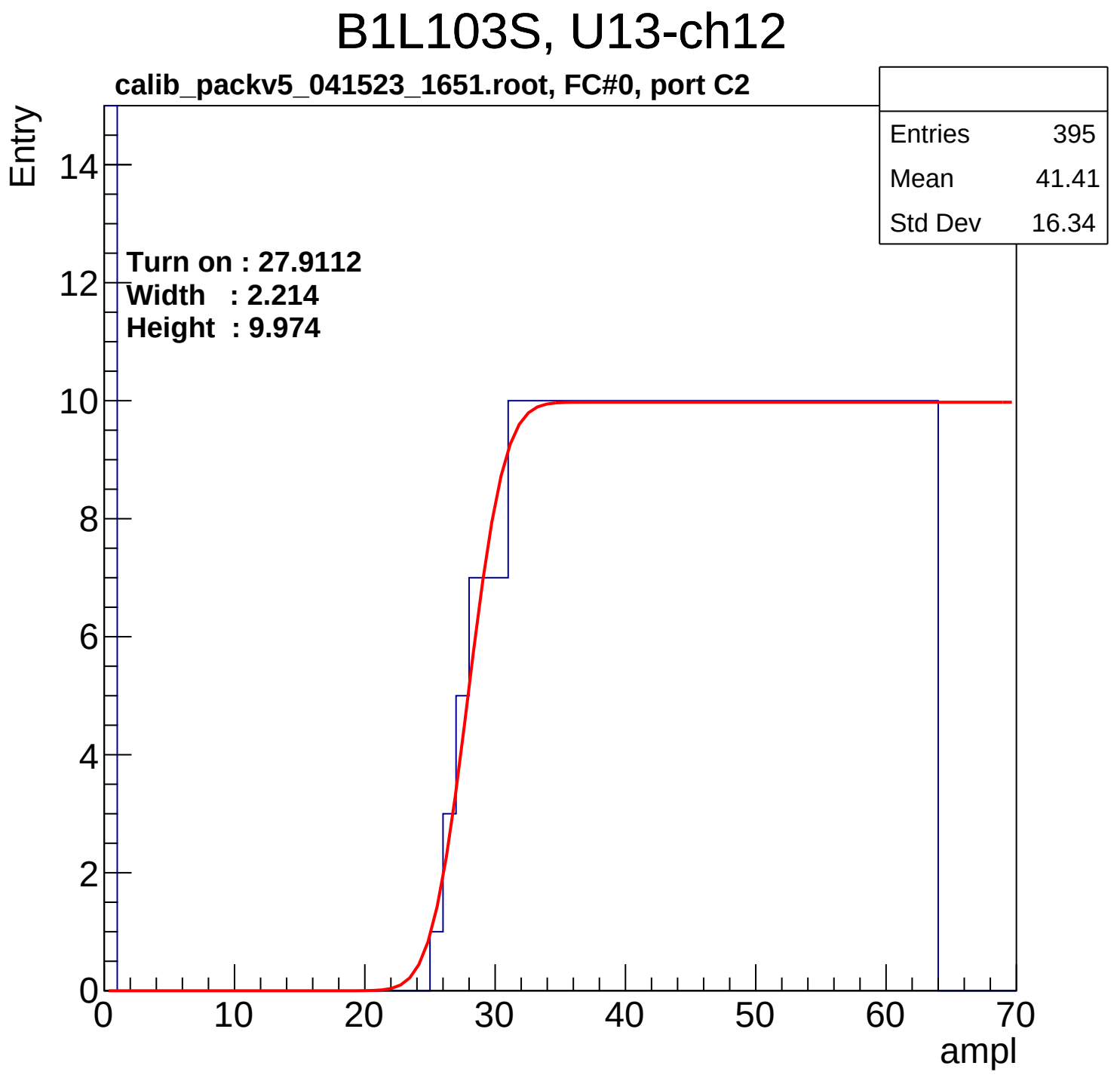
B1L103S, U13-ch12
calib_packv5_041523_1651.root, FC#0, port C2
Entries 395
Mean 41.41
Std Dev 16.34
Turn on : 27.9112
Width : 2.214
Height : 9.974
Entry
ampl
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6
8
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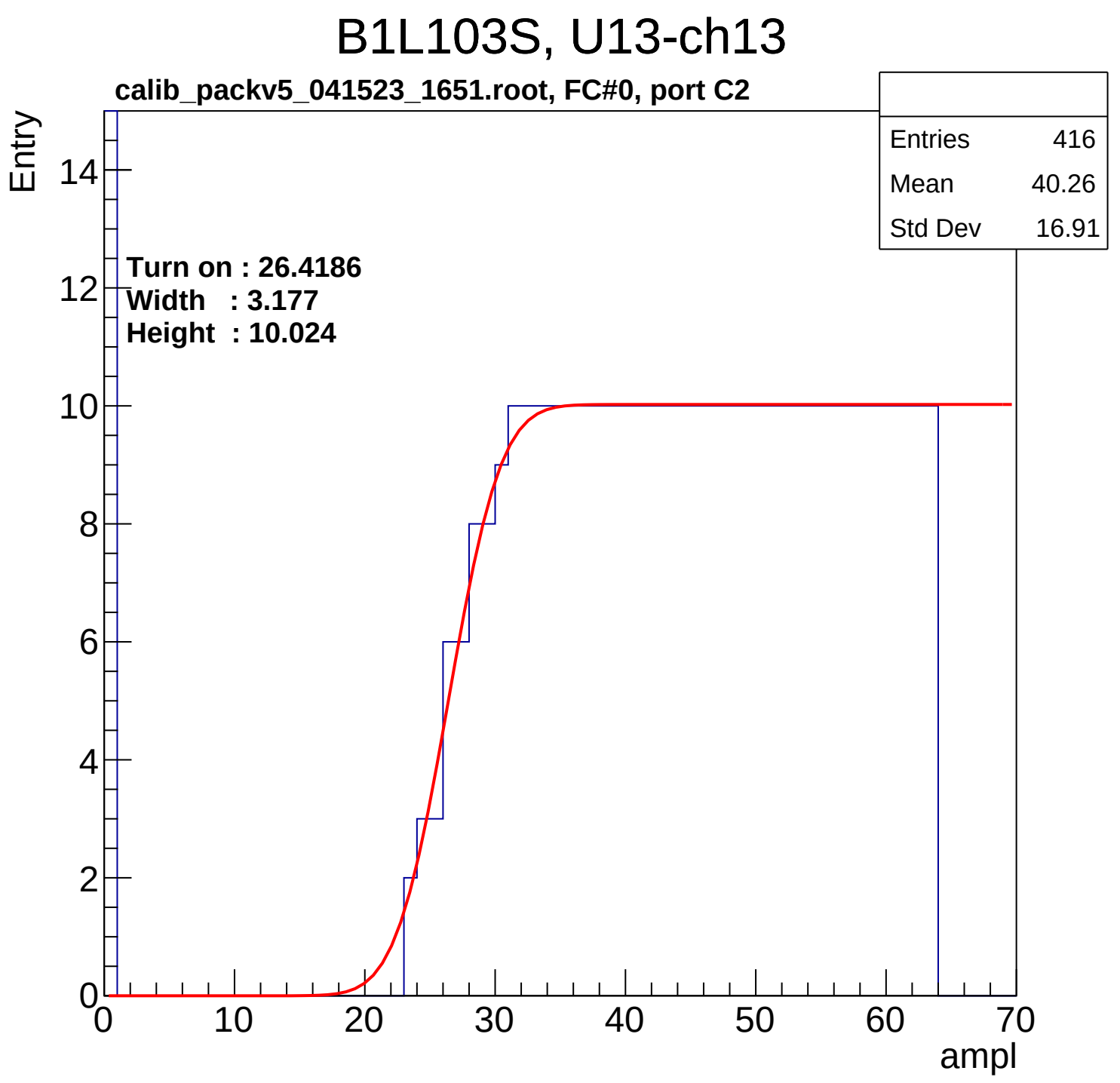
B1L103S, U13-ch13
calib_packv5_041523_1651.root, FC#0, port C2
Entries 416
Mean 40.26
Std Dev 16.91
Turn on : 26.4186
Width : 3.177
Height : 10.024
Entry
ampl
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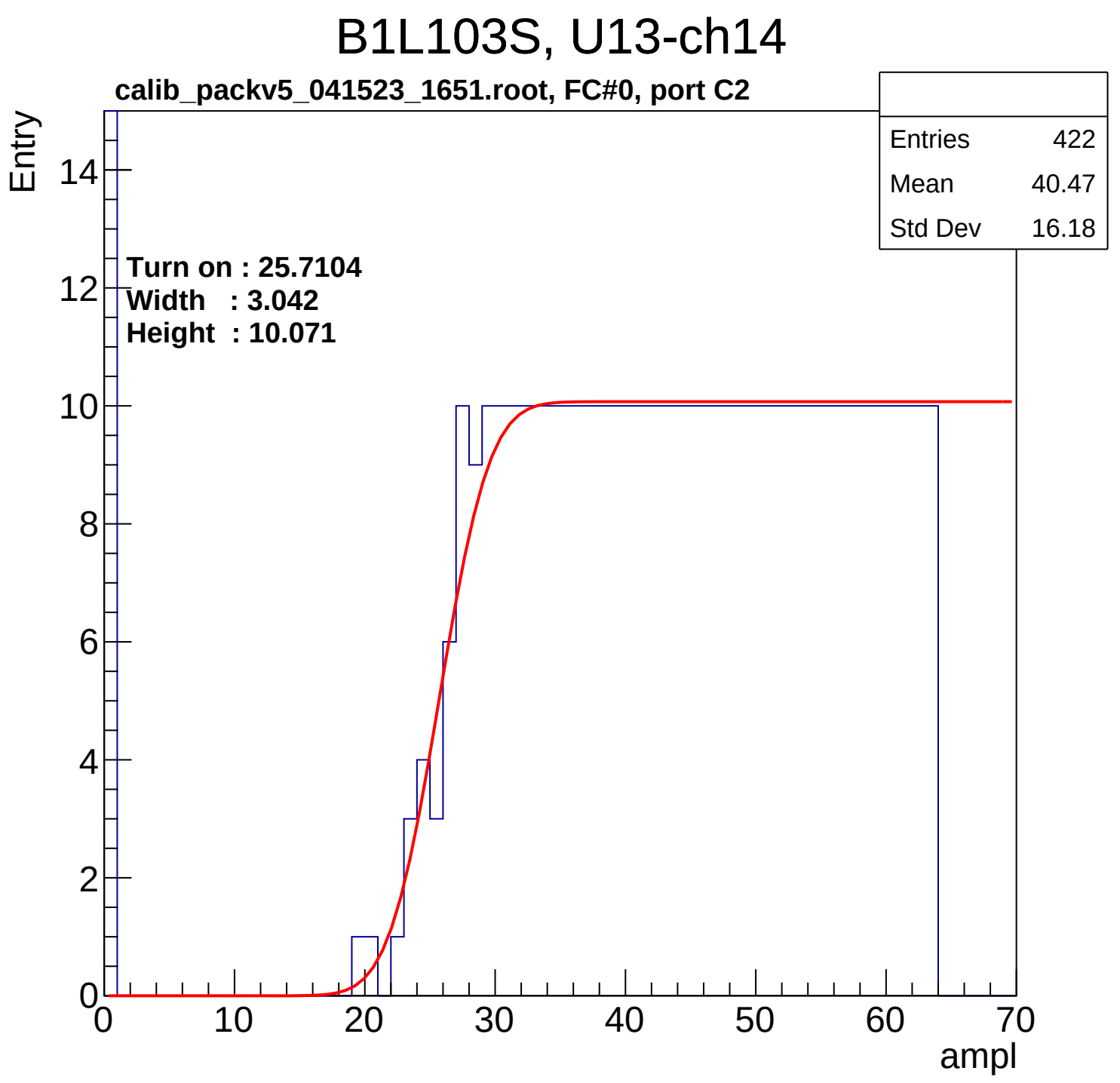
B1L103S, U13-ch14
calib_packv5_041523_1651.root, FC#0, port C2
Entries 422
Mean 40.47
Std Dev 16.18
Turn on : 25.7104
Width : 3.042
Height : 10.071
Entry
ampl
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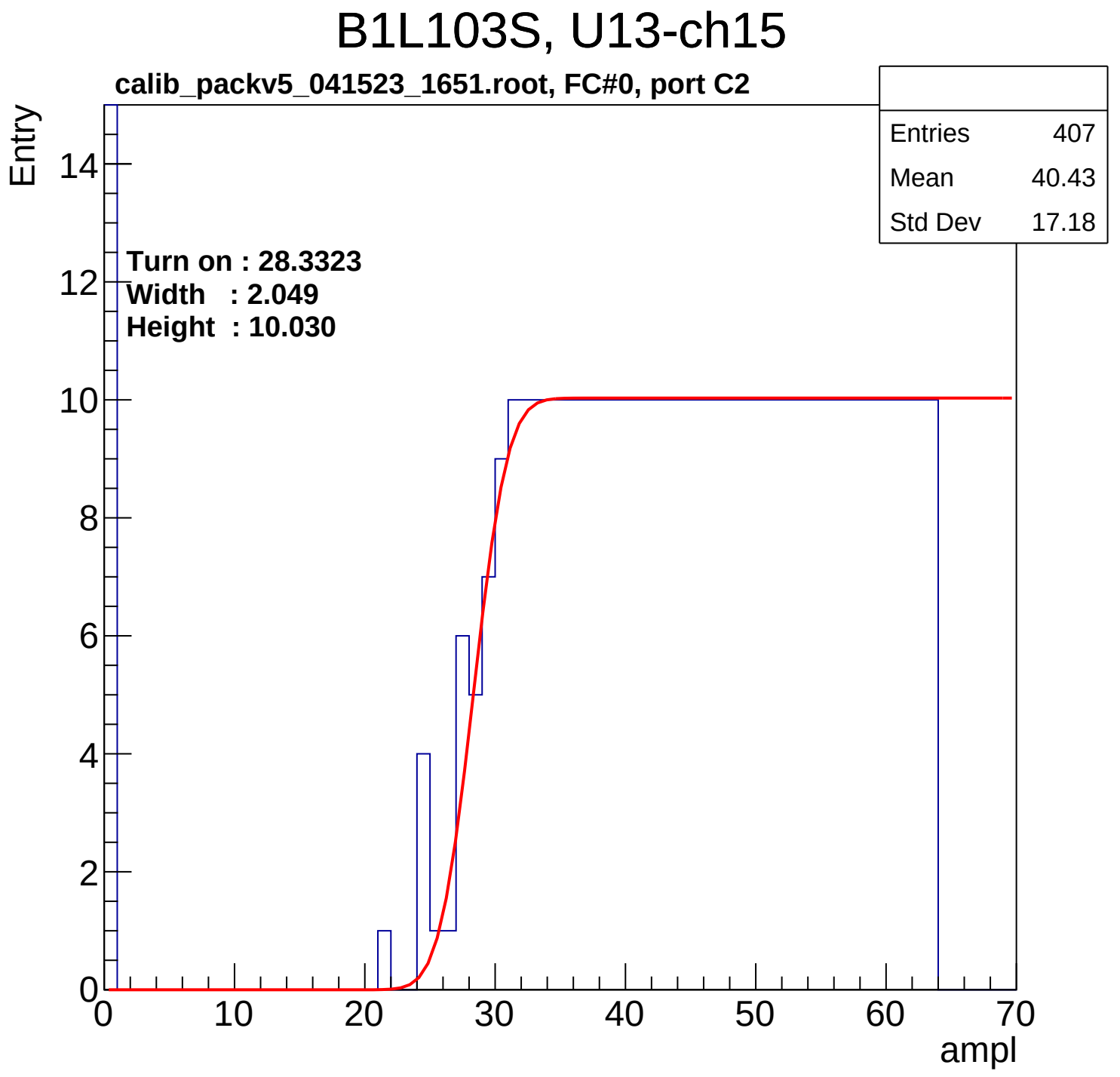
B1L103S, U13-ch15
calib_packv5_041523_1651.root, FC#0, port C2
Entries 407
Mean 40.43
Std Dev 17.18
Turn on : 28.3323
Width : 2.049
Height : 10.030
Entry
ampl
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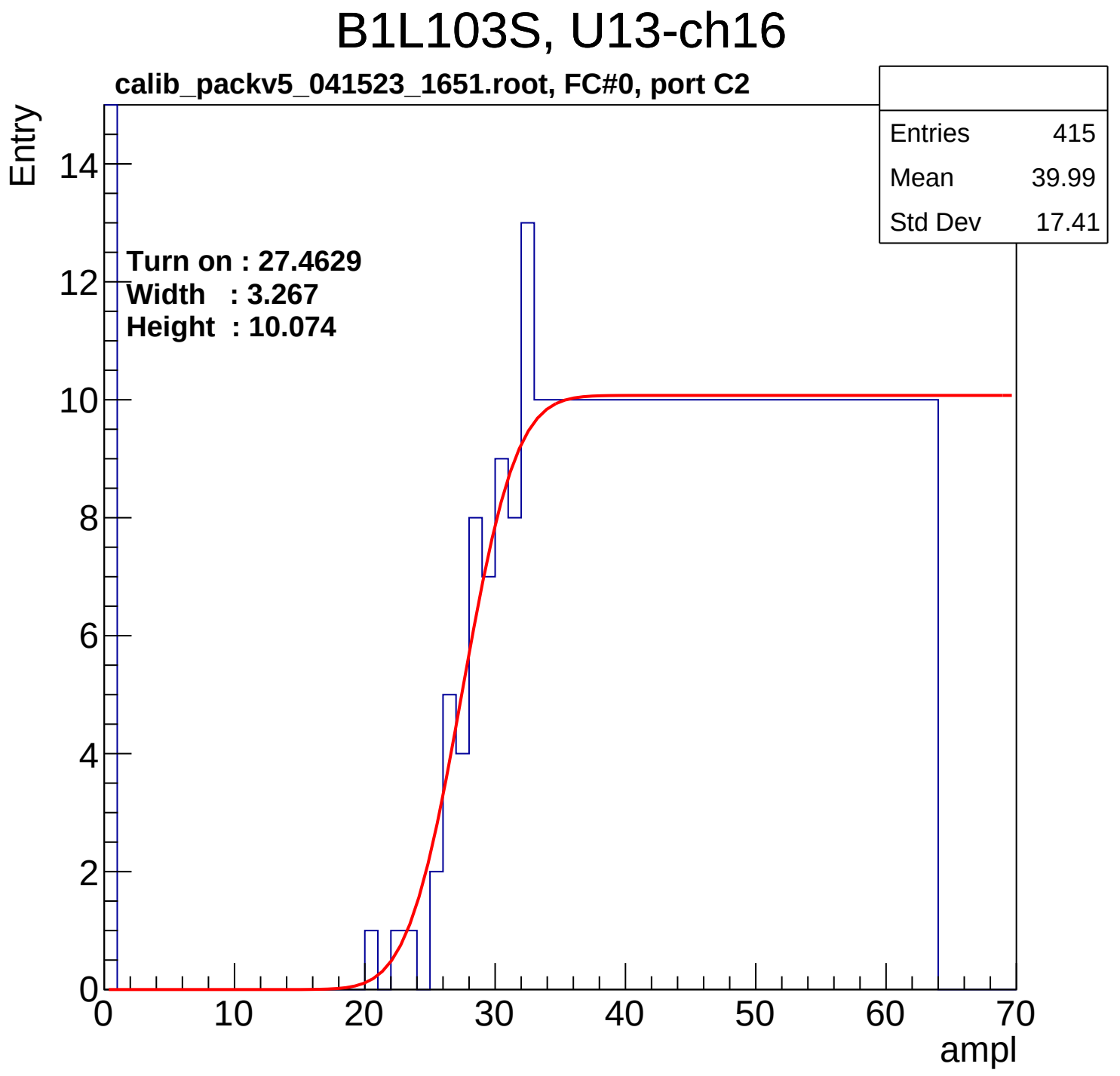
B1L103S, U13-ch16
calib_packv5_041523_1651.root, FC#0, port C2
Entries 415
Mean 39.99
Std Dev 17.41
Turn on : 27.4629
Width : 3.267
Height : 10.074
Entry
ampl
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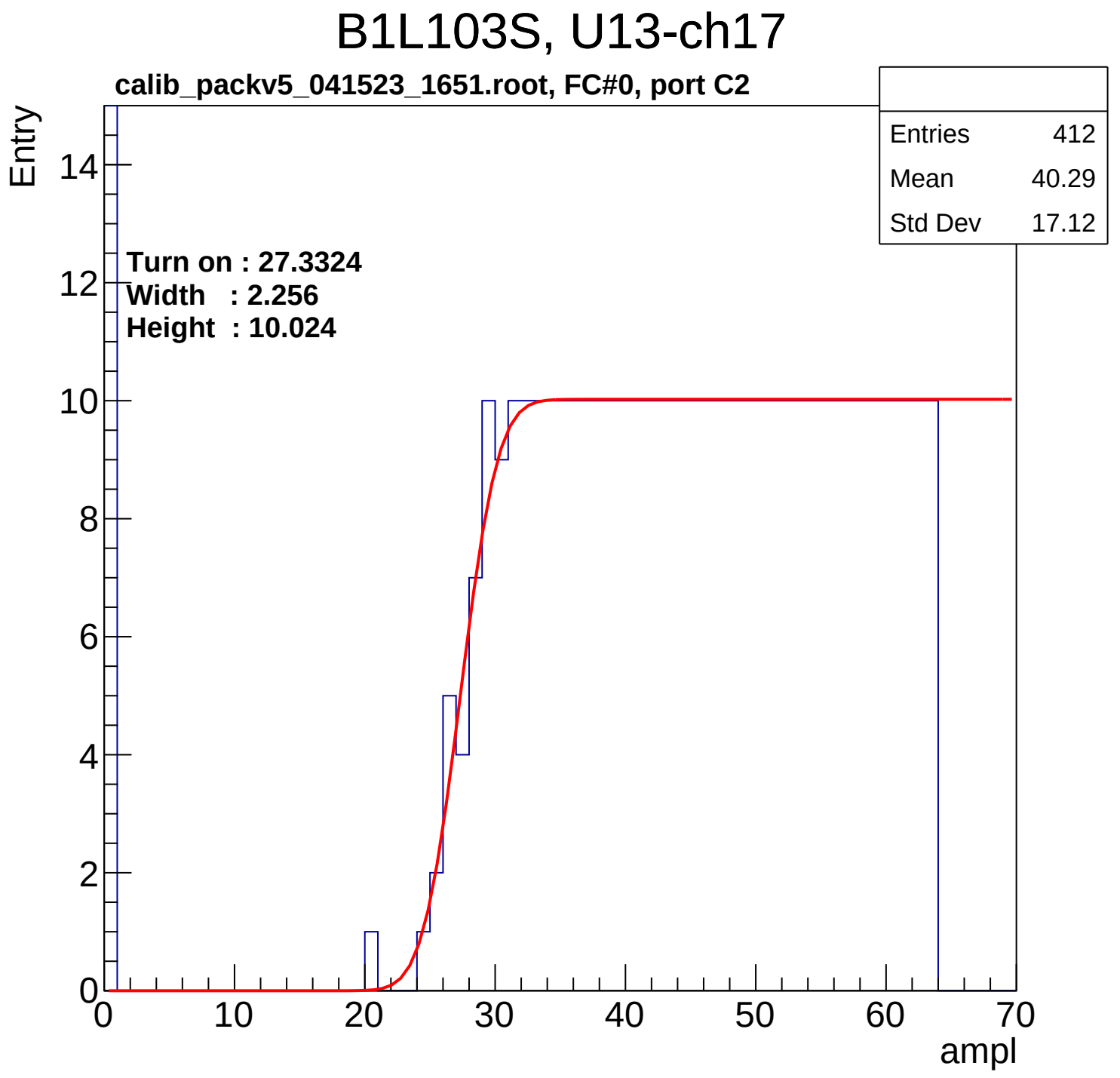
B1L103S, U13-ch17
calib_packv5_041523_1651.root, FC#0, port C2
Entries 412
Mean 40.29
Std Dev 17.12
Turn on : 27.3324
Width : 2.256
Height : 10.024
Entry
ampl
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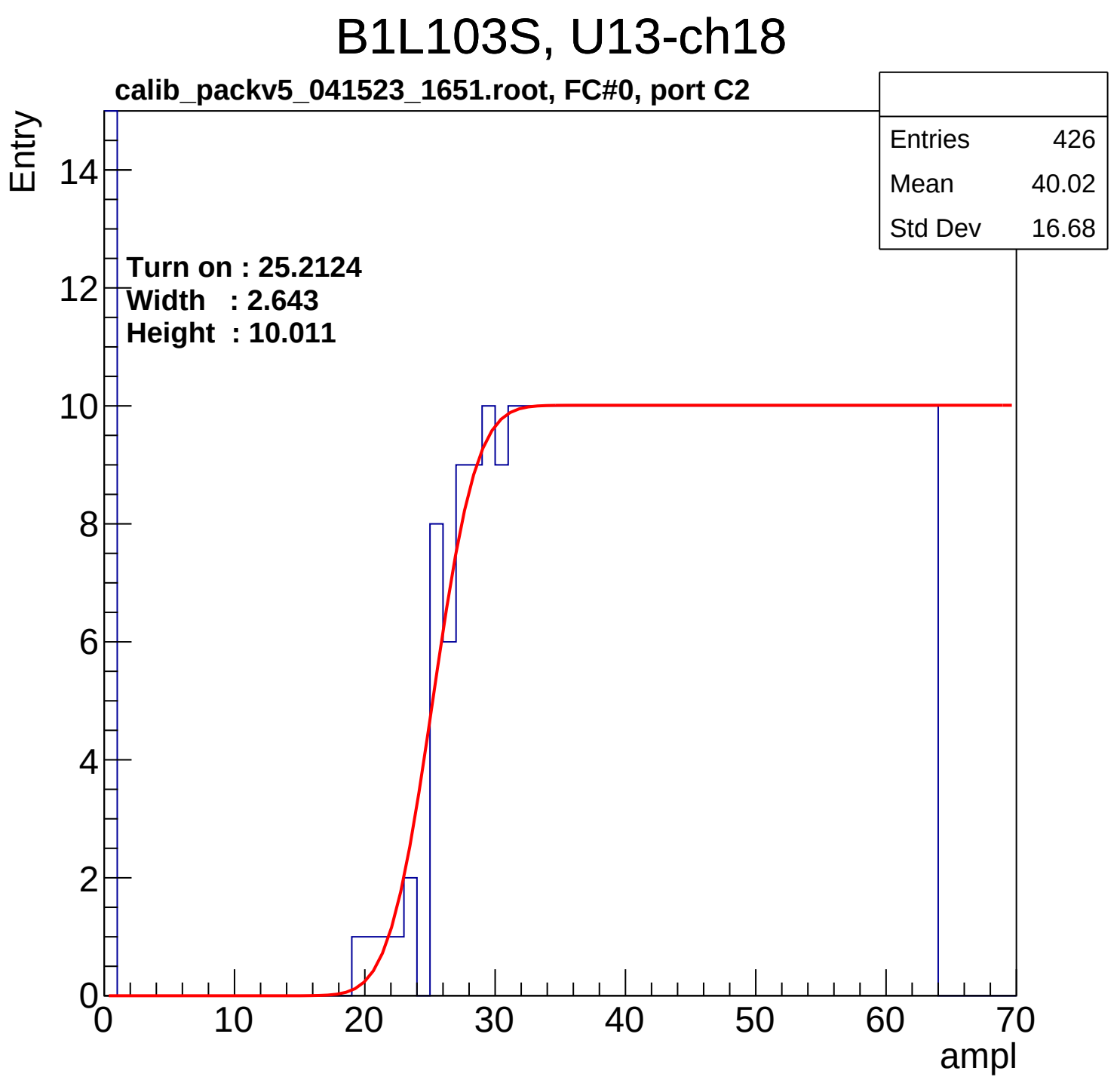
B1L103S, U13-ch18
calib_packv5_041523_1651.root, FC#0, port C2
Entries 426
Mean 40.02
Std Dev 16.68
Turn on : 25.2124
Width : 2.643
Height : 10.011
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ampl
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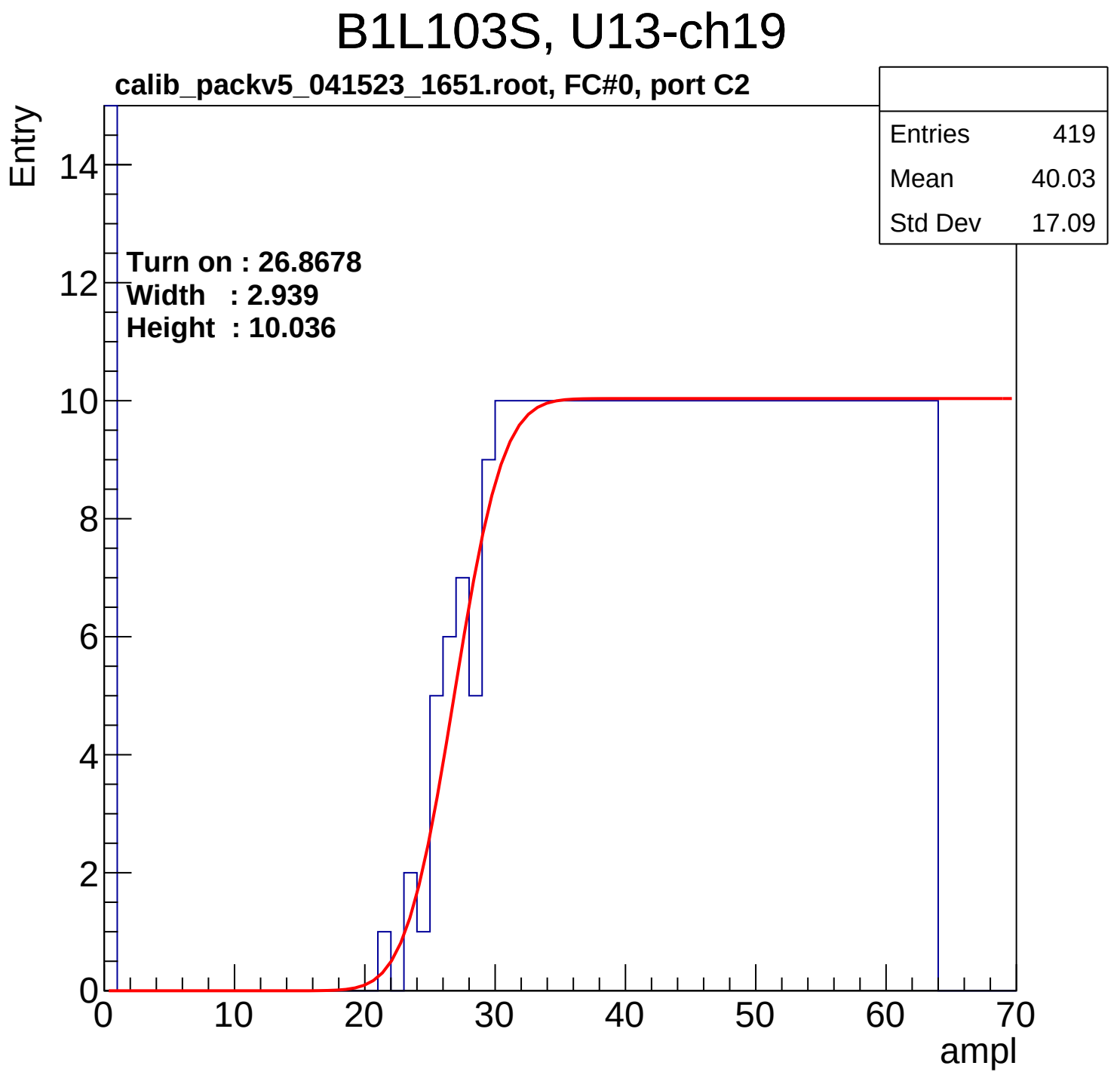
B1L103S, U13-ch19
calib_packv5_041523_1651.root, FC#0, port C2
Entries 419
Mean 40.03
Std Dev 17.09
Turn on : 26.8678
Width : 2.939
Height : 10.036
Entry
ampl
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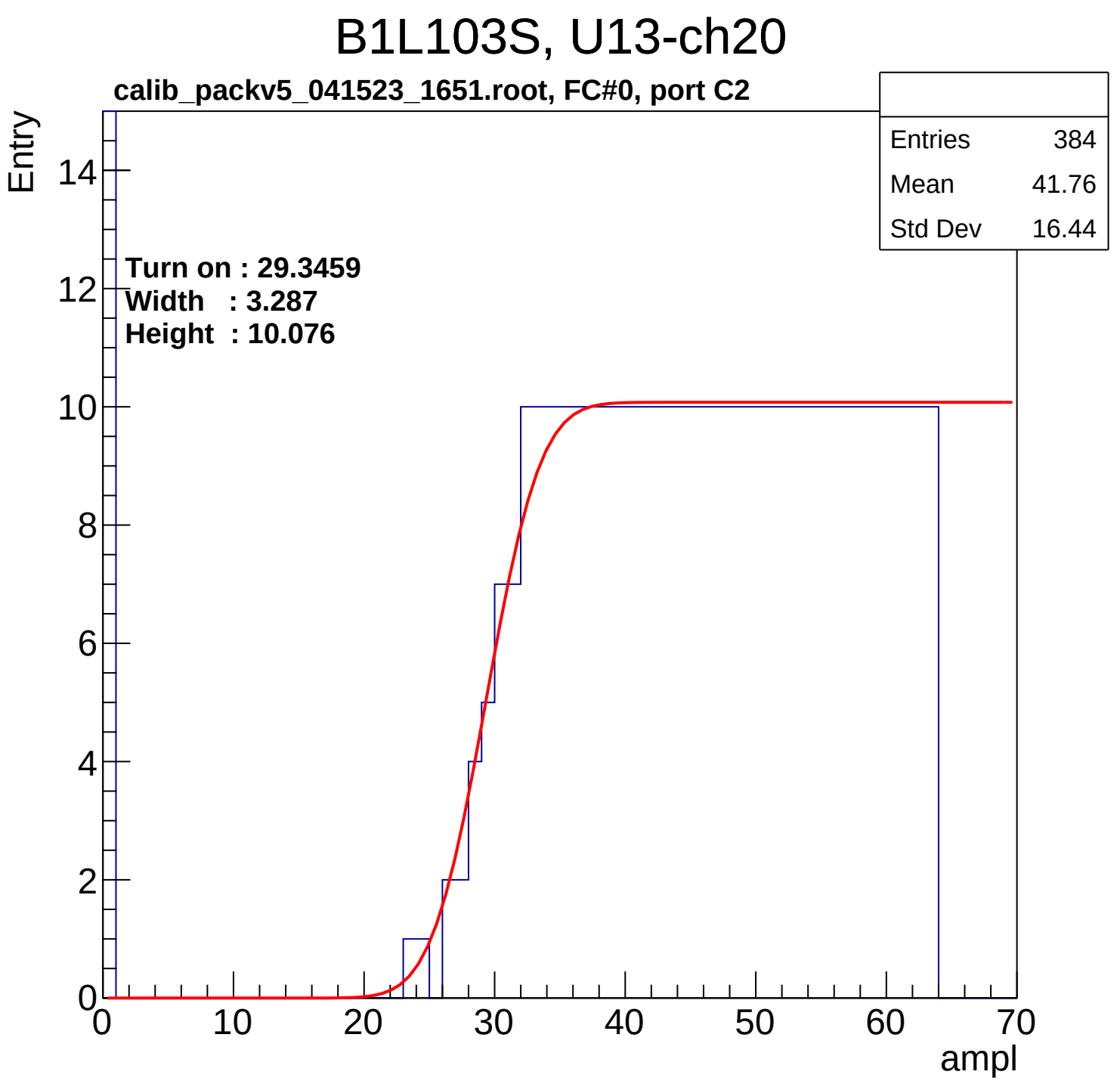
B1L103S, U13-ch20
calib_packv5_041523_1651.root, FC#0, port C2
Entries 384
Mean 41.76
Std Dev 16.44
Turn on : 29.3459
Width : 3.287
Height : 10.076
Entry
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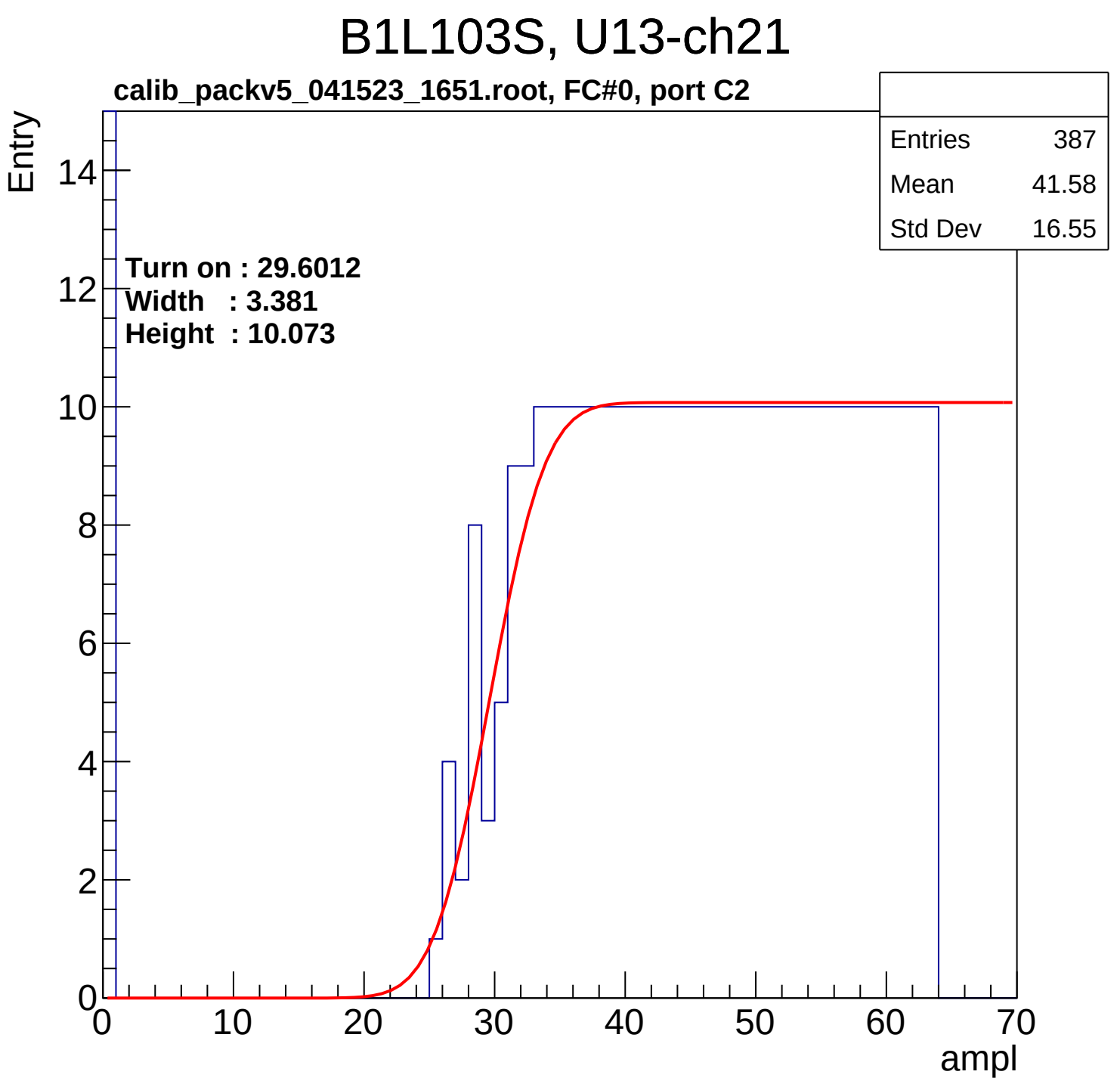
B1L103S, U13-ch21
calib_packv5_041523_1651.root, FC#0, port C2
Entries 387
Mean 41.58
Std Dev 16.55
Turn on : 29.6012
Width : 3.381
Height : 10.073
Entry
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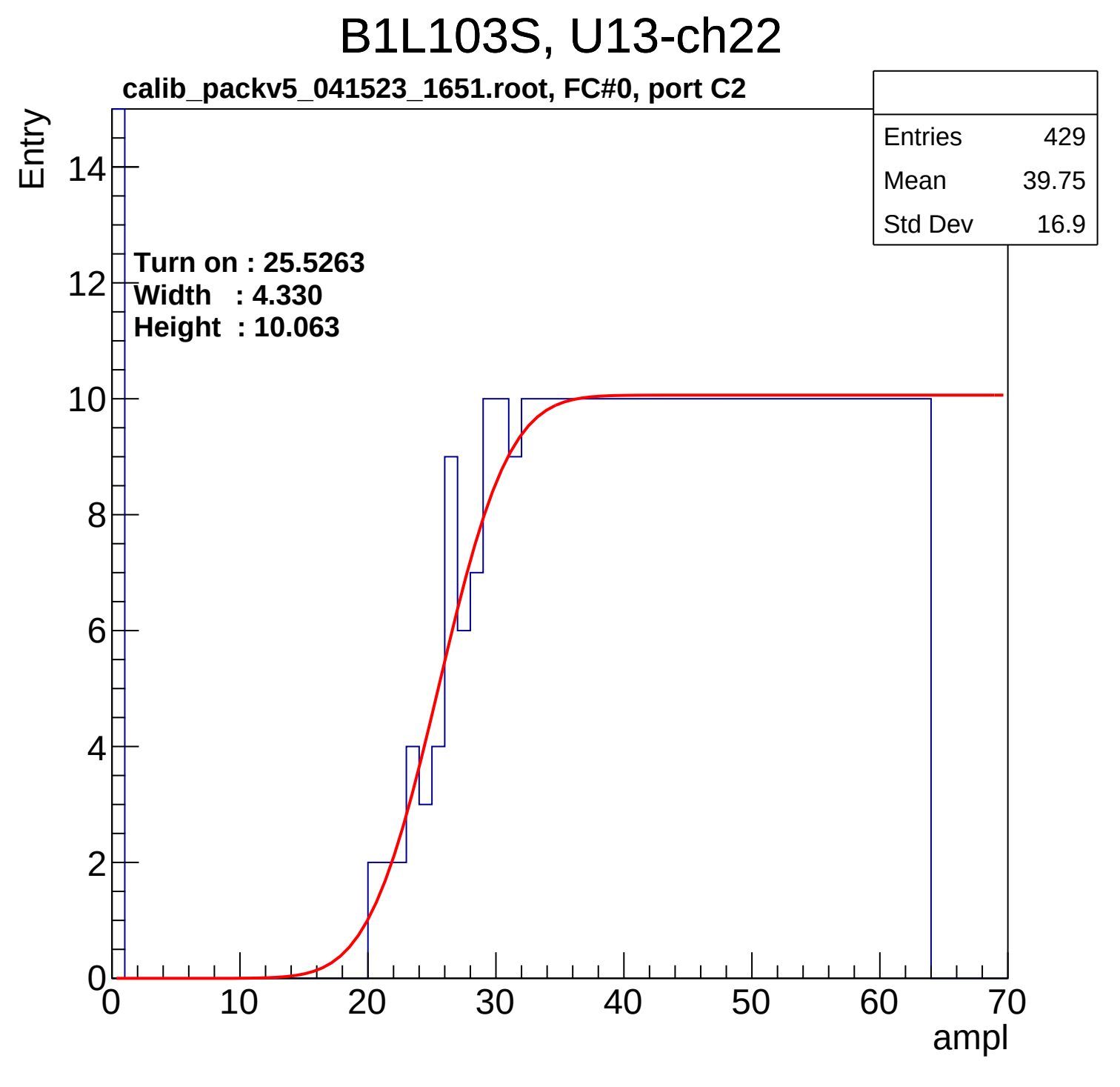
B1L103S, U13-ch22
calib_packv5_041523_1651.root, FC#0, port C2
Entries 429
Mean 39.75
Std Dev 16.9
Turn on : 25.5263
Width : 4.330
Height : 10.063
Entry
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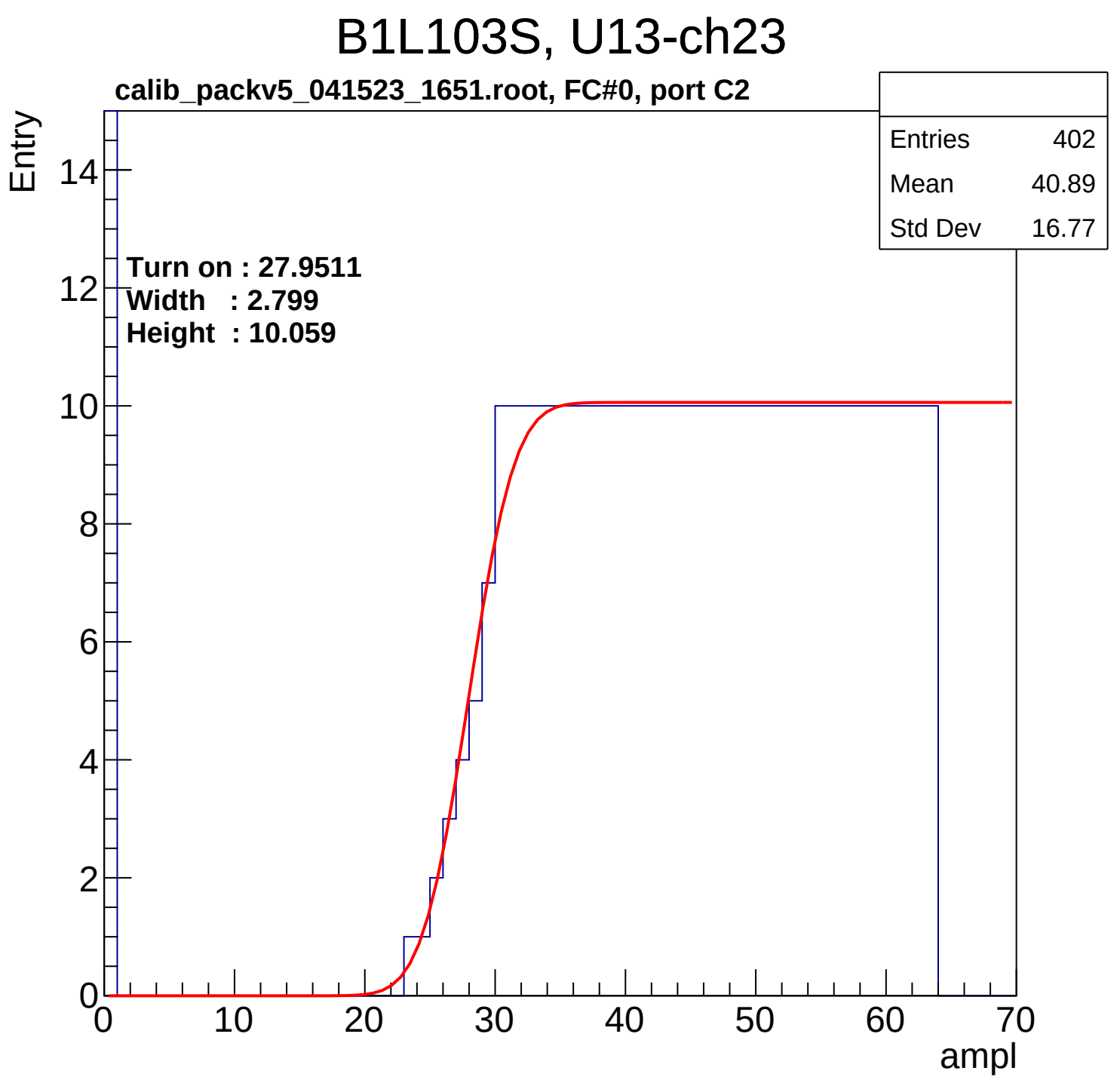
B1L103S, U13-ch23
calib_packv5_041523_1651.root, FC#0, port C2
Entries 402
Mean 40.89
Std Dev 16.77
Turn on : 27.9511
Width : 2.799
Height : 10.059
Entry
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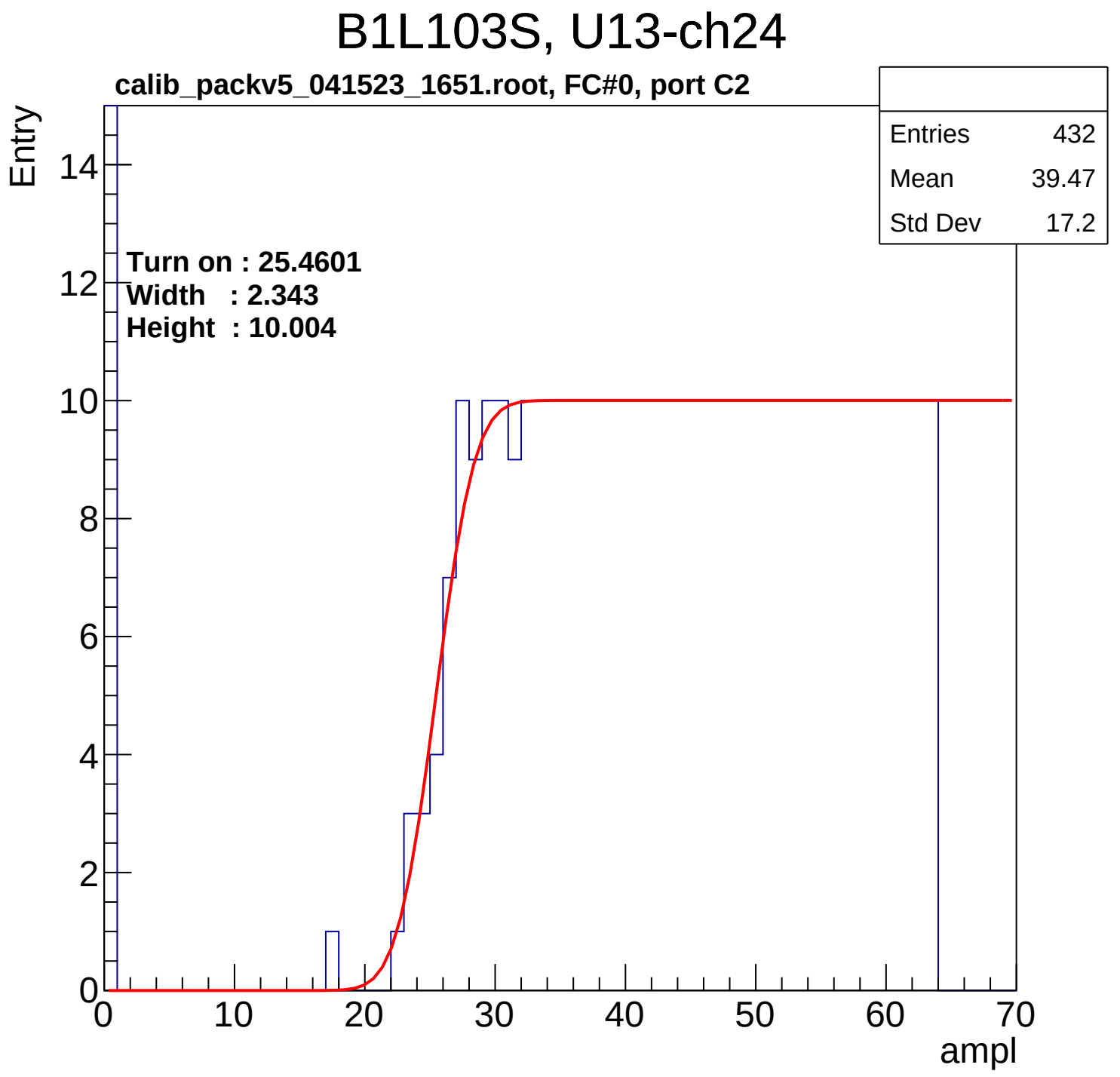
B1L103S, U13-ch24
calib_packv5_041523_1651.root, FC#0, port C2
Entries 432
Mean 39.47
Std Dev 17.2
Turn on : 25.4601
Width : 2.343
Height : 10.004
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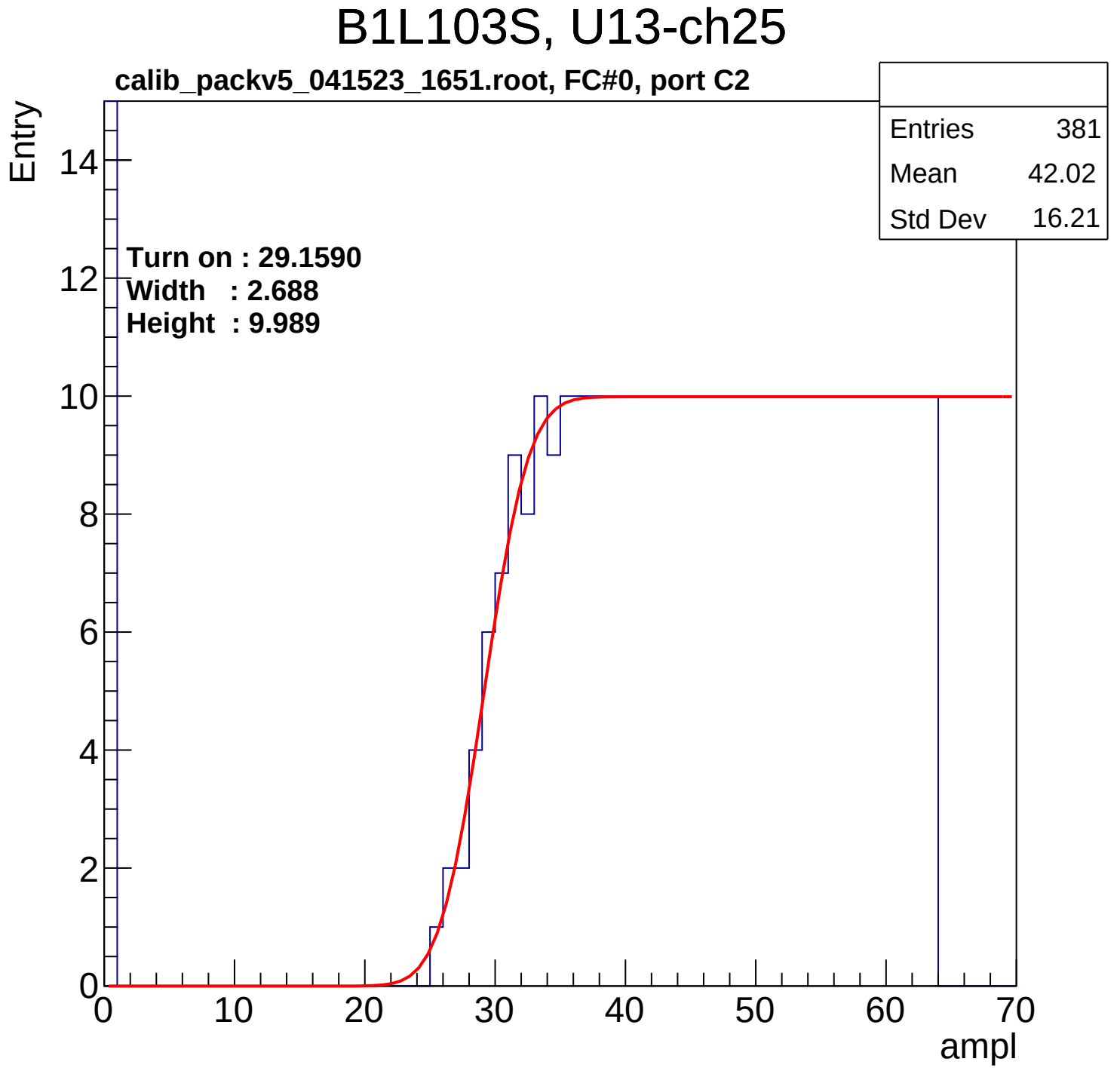
B1L103S, U13-ch25
calib_packv5_041523_1651.root, FC#0, port C2
Entries 381
Mean 42.02
Std Dev 16.21
Turn on : 29.1590
Width : 2.688
Height : 9.989
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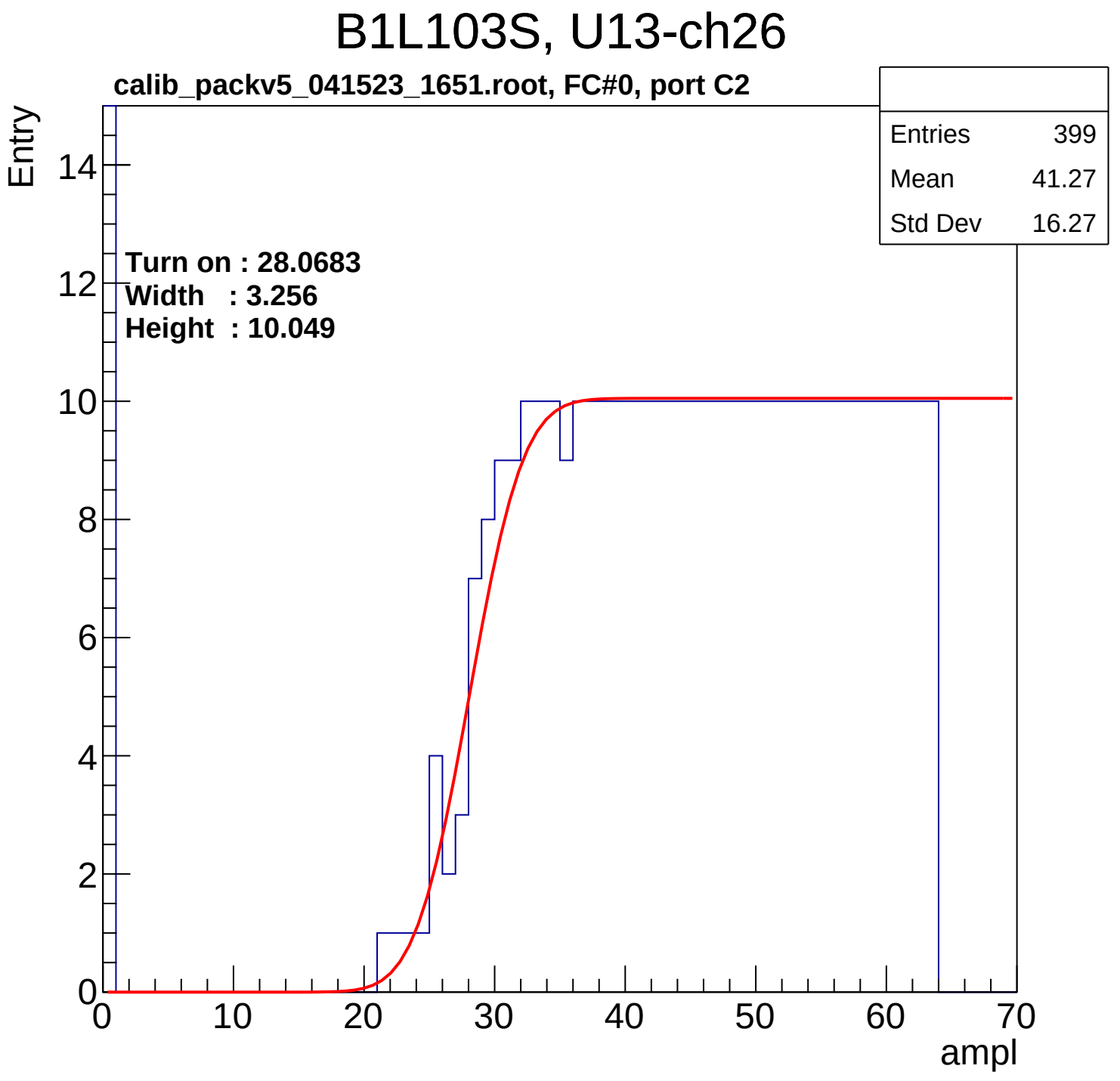
B1L103S, U13-ch26
calib_packv5_041523_1651.root, FC#0, port C2
Entries 399
Mean 41.27
Std Dev 16.27
Turn on : 28.0683
Width : 3.256
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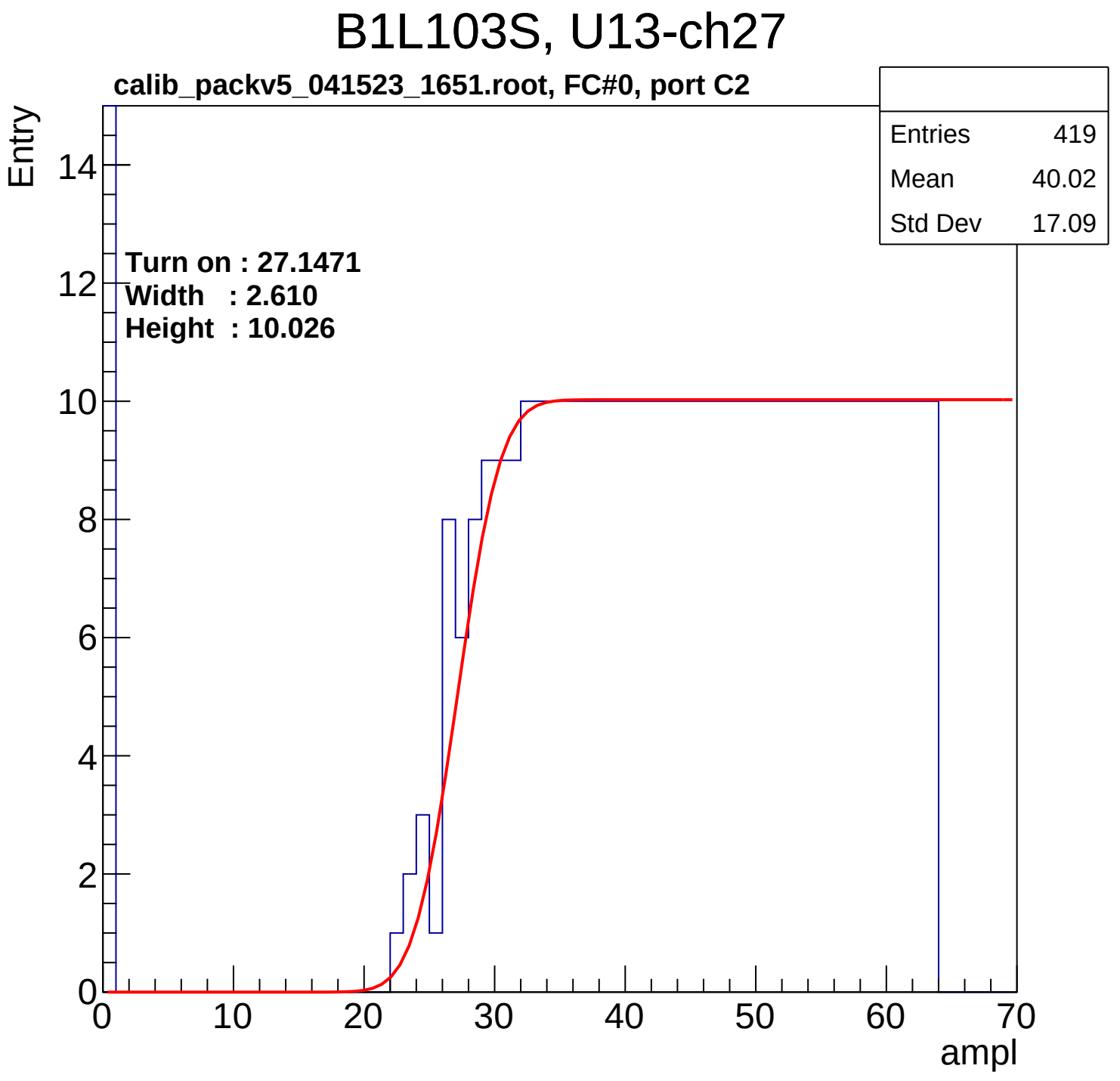
B1L103S, U13-ch27
calib_packv5_041523_1651.root, FC#0, port C2
Entries 419
Mean 40.02
Std Dev 17.09
Turn on : 27.1471
Width : 2.610
Height : 10.026
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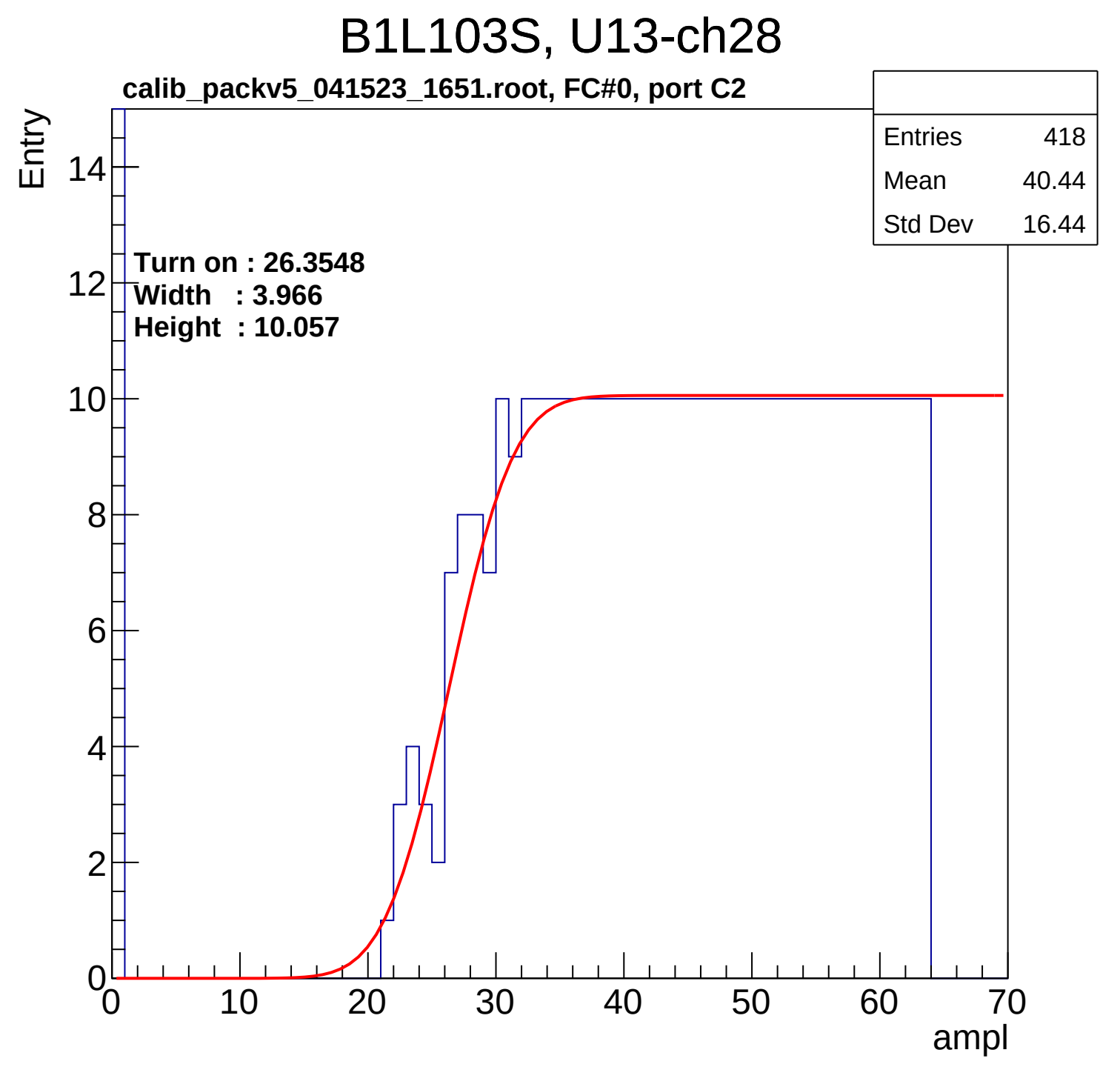
B1L103S, U13-ch28
calib_packv5_041523_1651.root, FC#0, port C2
Entries 418
Mean 40.44
Std Dev 16.44
Turn on : 26.3548
Width : 3.966
Height : 10.057
Entry
ampl
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4
6
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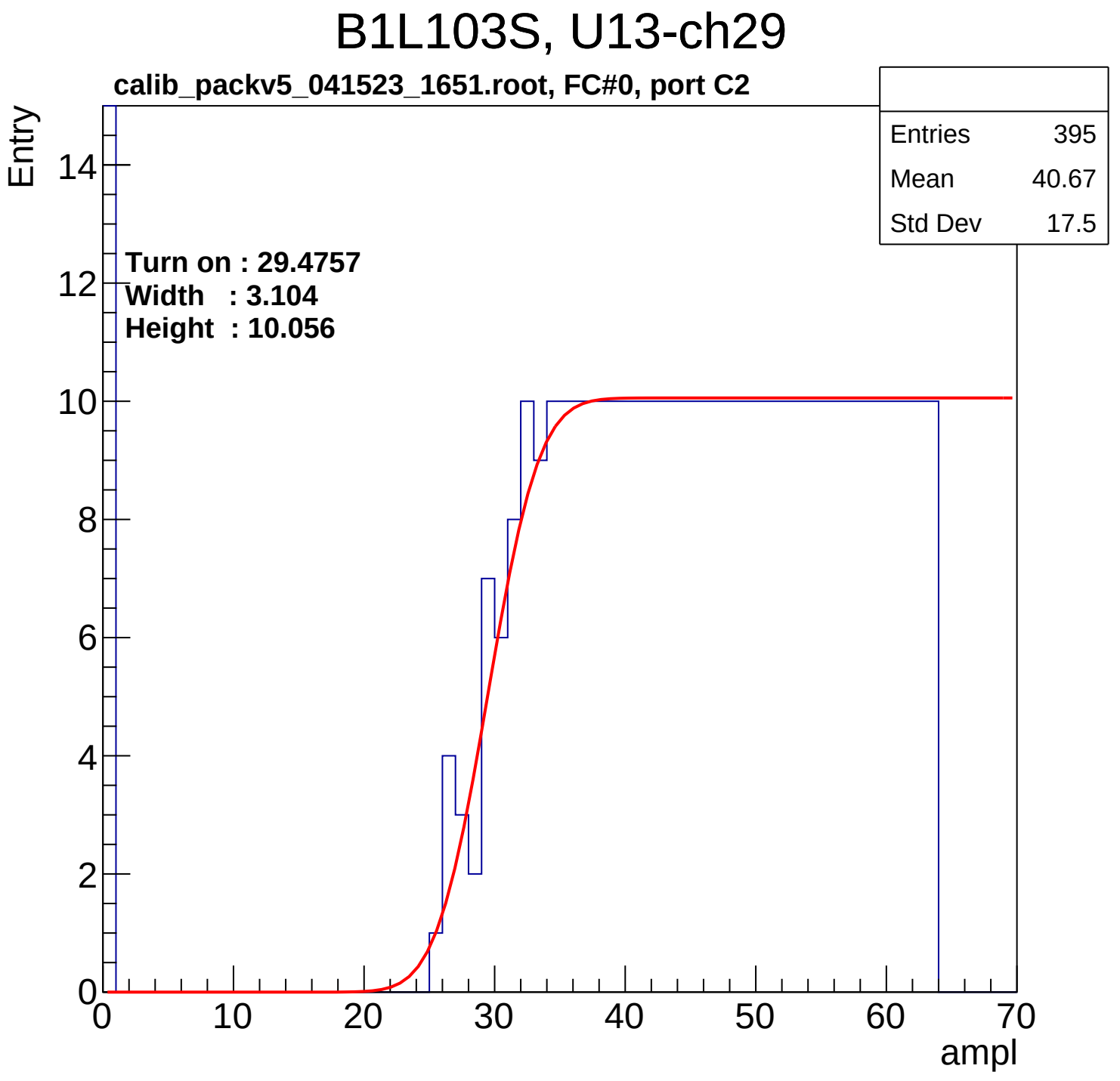
B1L103S, U13-ch29
calib_packv5_041523_1651.root, FC#0, port C2
Entries 395
Mean 40.67
Std Dev 17.5
Turn on : 29.4757
Width : 3.104
Height : 10.056
Entry
ampl
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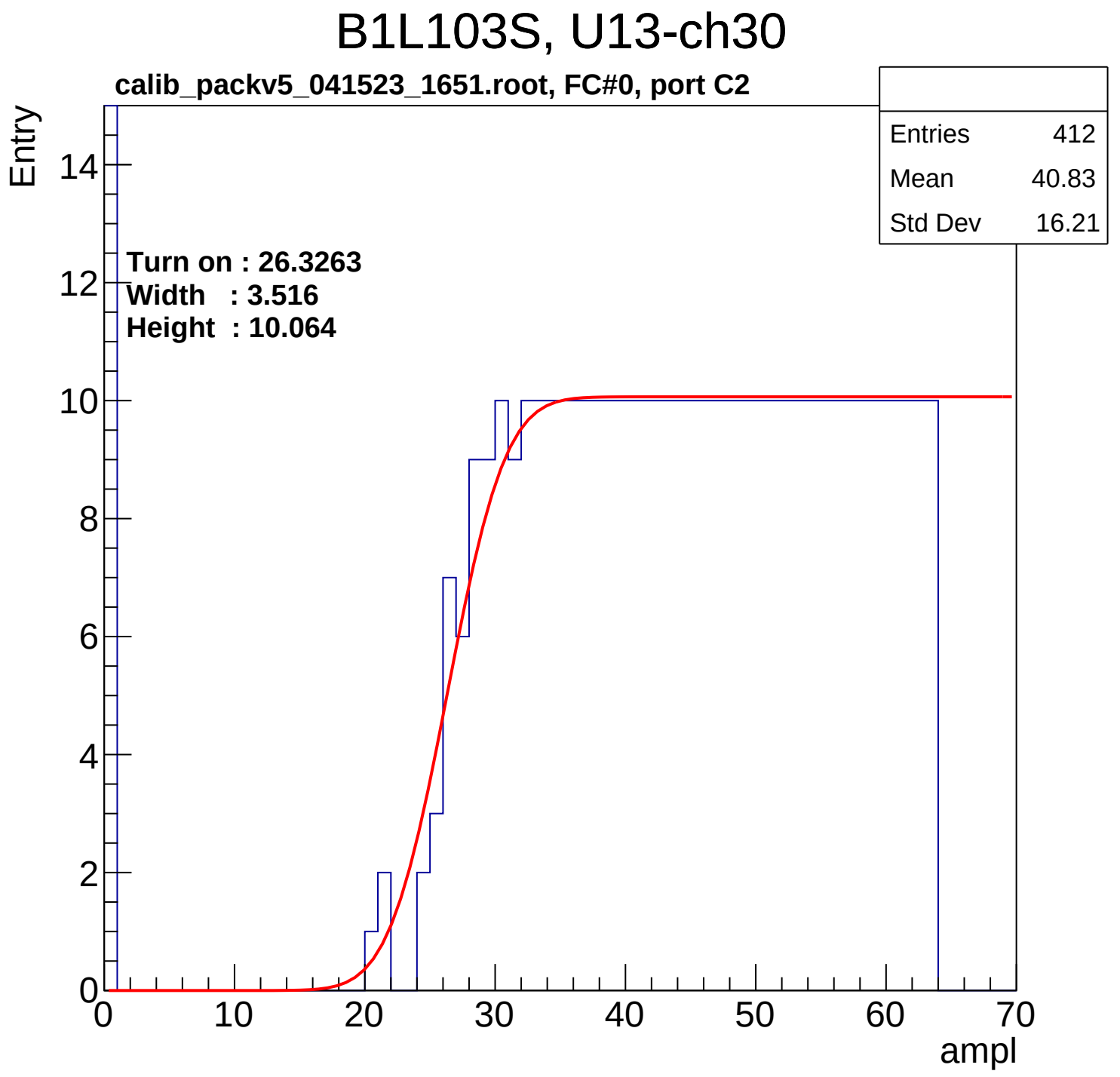
B1L103S, U13-ch30
calib_packv5_041523_1651.root, FC#0, port C2
Entries 412
Mean 40.83
Std Dev 16.21
Turn on : 26.3263
Width : 3.516
Height : 10.064
Entry
ampl
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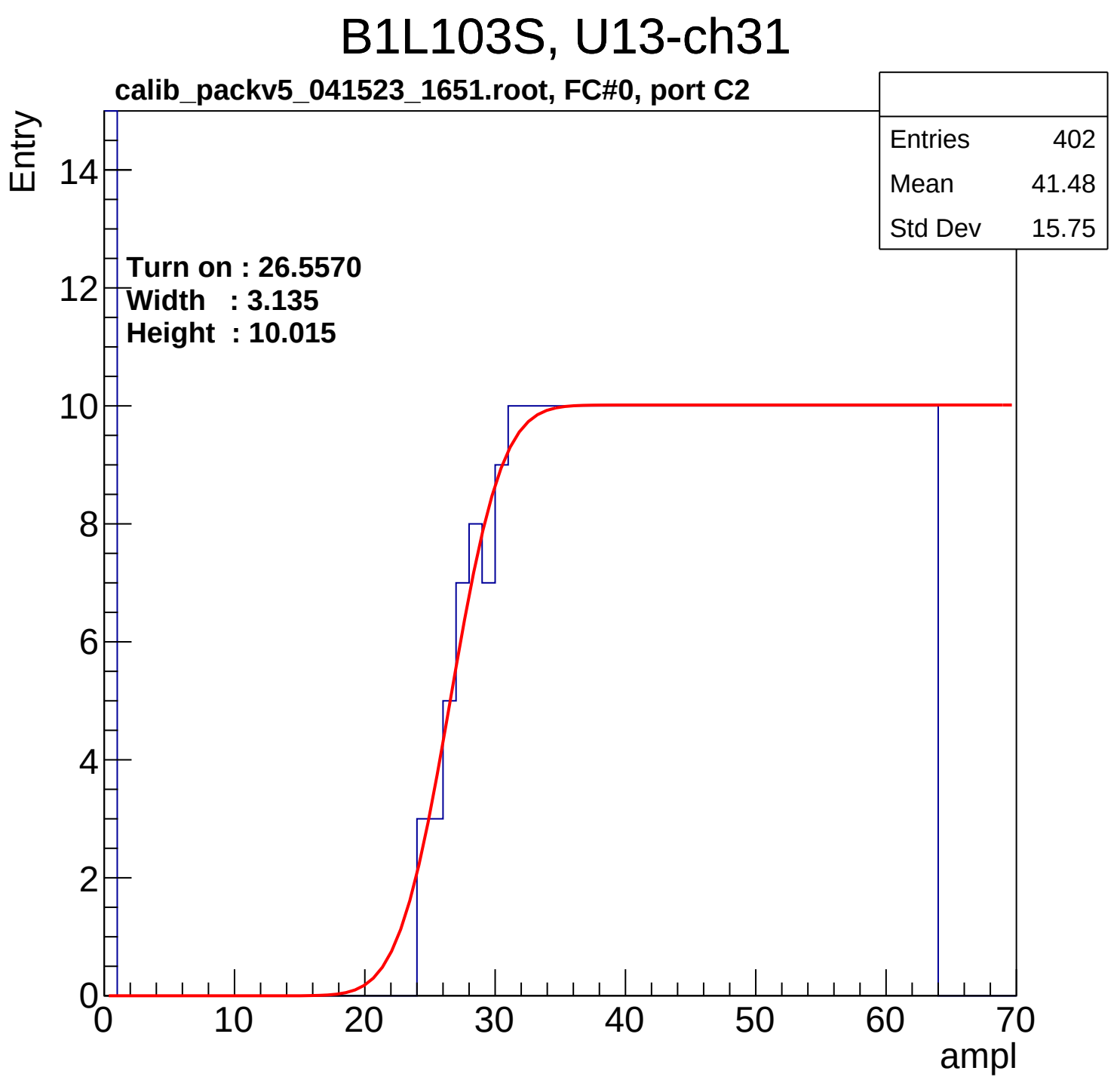
B1L103S, U13-ch31
calib_packv5_041523_1651.root, FC#0, port C2
Entries 402
Mean 41.48
Std Dev 15.75
Turn on : 26.5570
Width : 3.135
Height : 10.015
Entry
ampl
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2
4
6
8
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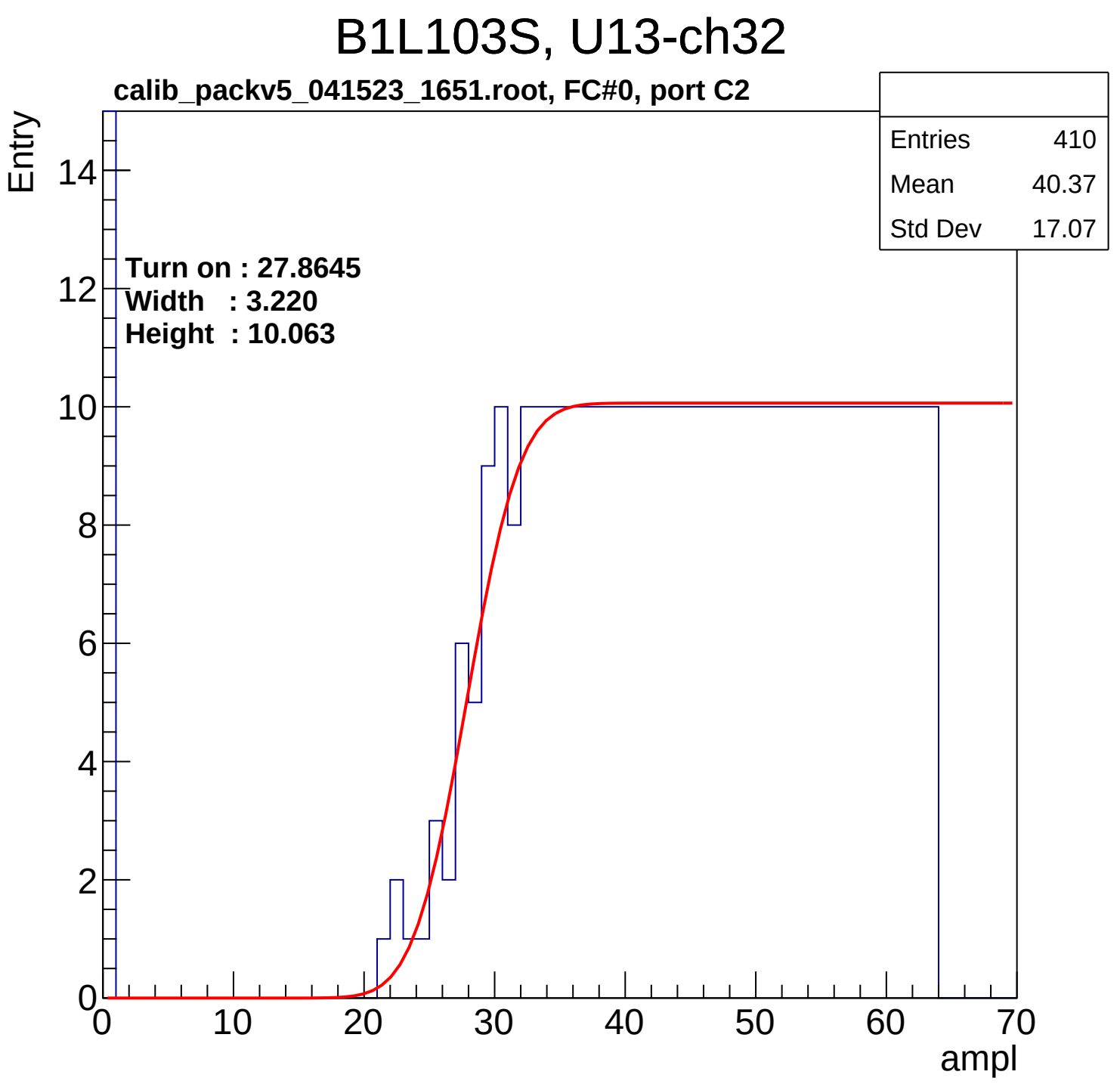
B1L103S, U13-ch32
calib_packv5_041523_1651.root, FC#0, port C2
Entries 410
Mean 40.37
Std Dev 17.07
Turn on : 27.8645
Width : 3.220
Height : 10.063
Entry
ampl
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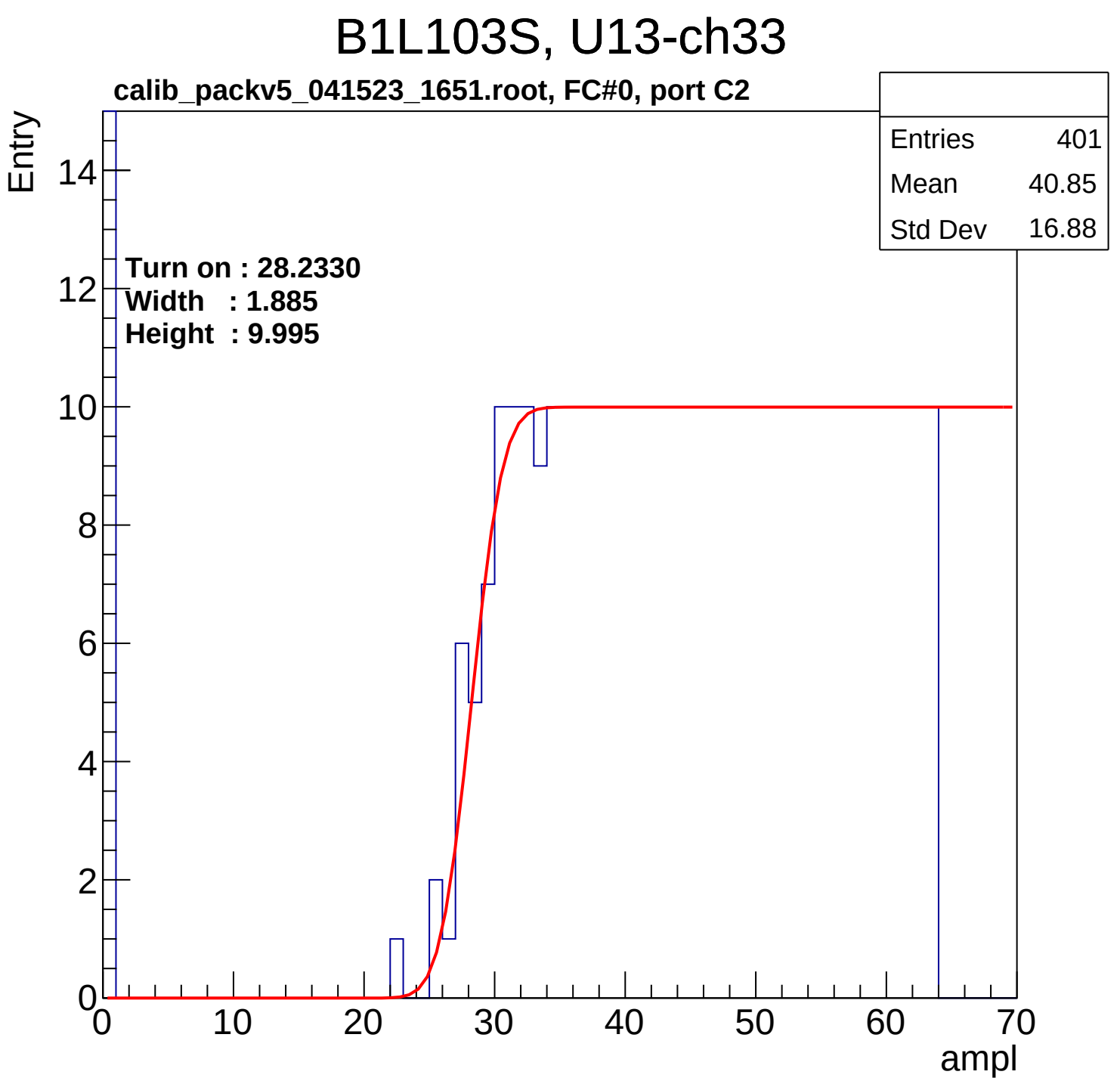
B1L103S, U13-ch33
calib_packv5_041523_1651.root, FC#0, port C2
Entries 401
Mean 40.85
Std Dev 16.88
Turn on : 28.2330
Width : 1.885
Height : 9.995
Entry
ampl
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2
4
6
8
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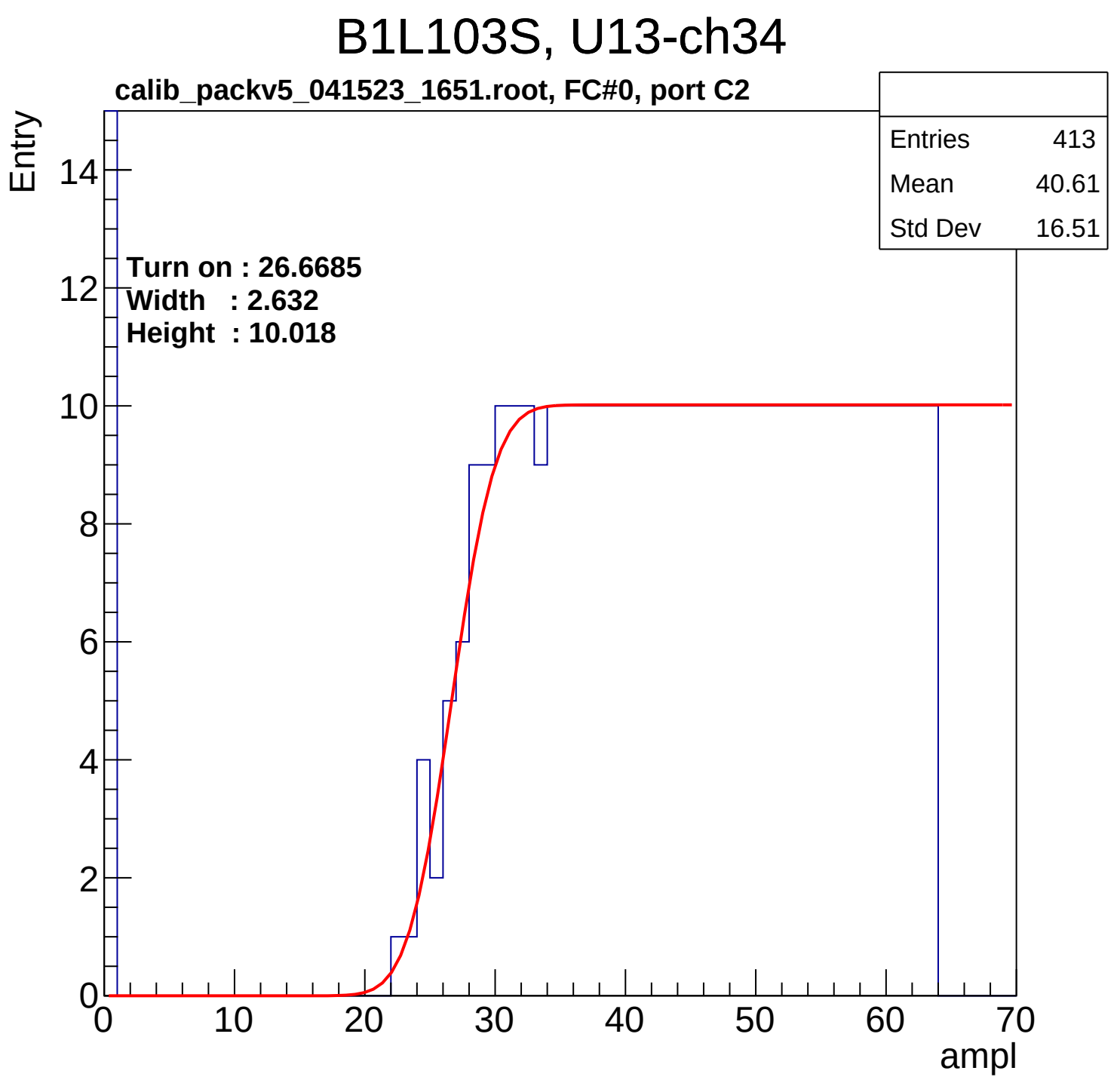
B1L103S, U13-ch34
calib_packv5_041523_1651.root, FC#0, port C2
Entries 413
Mean 40.61
Std Dev 16.51
Turn on : 26.6685
Width : 2.632
Height : 10.018
Entry
ampl
0
2
4
6
8
10
12
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0
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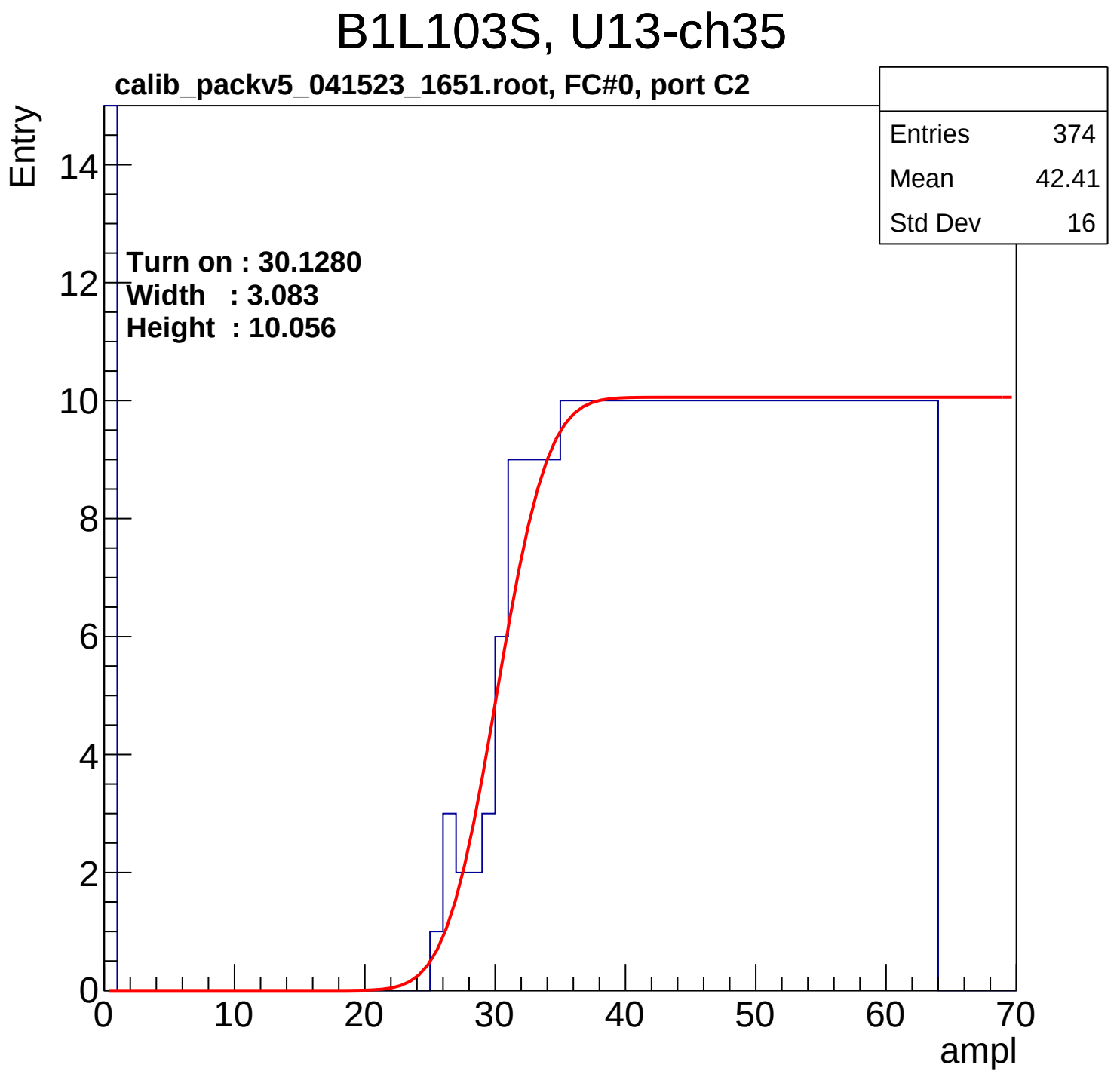
B1L103S, U13-ch35
calib_packv5_041523_1651.root, FC#0, port C2
Entries 374
Mean 42.41
Std Dev 16
Turn on : 30.1280
Width : 3.083
Height : 10.056
Entry
ampl
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2
4
6
8
10
12
14
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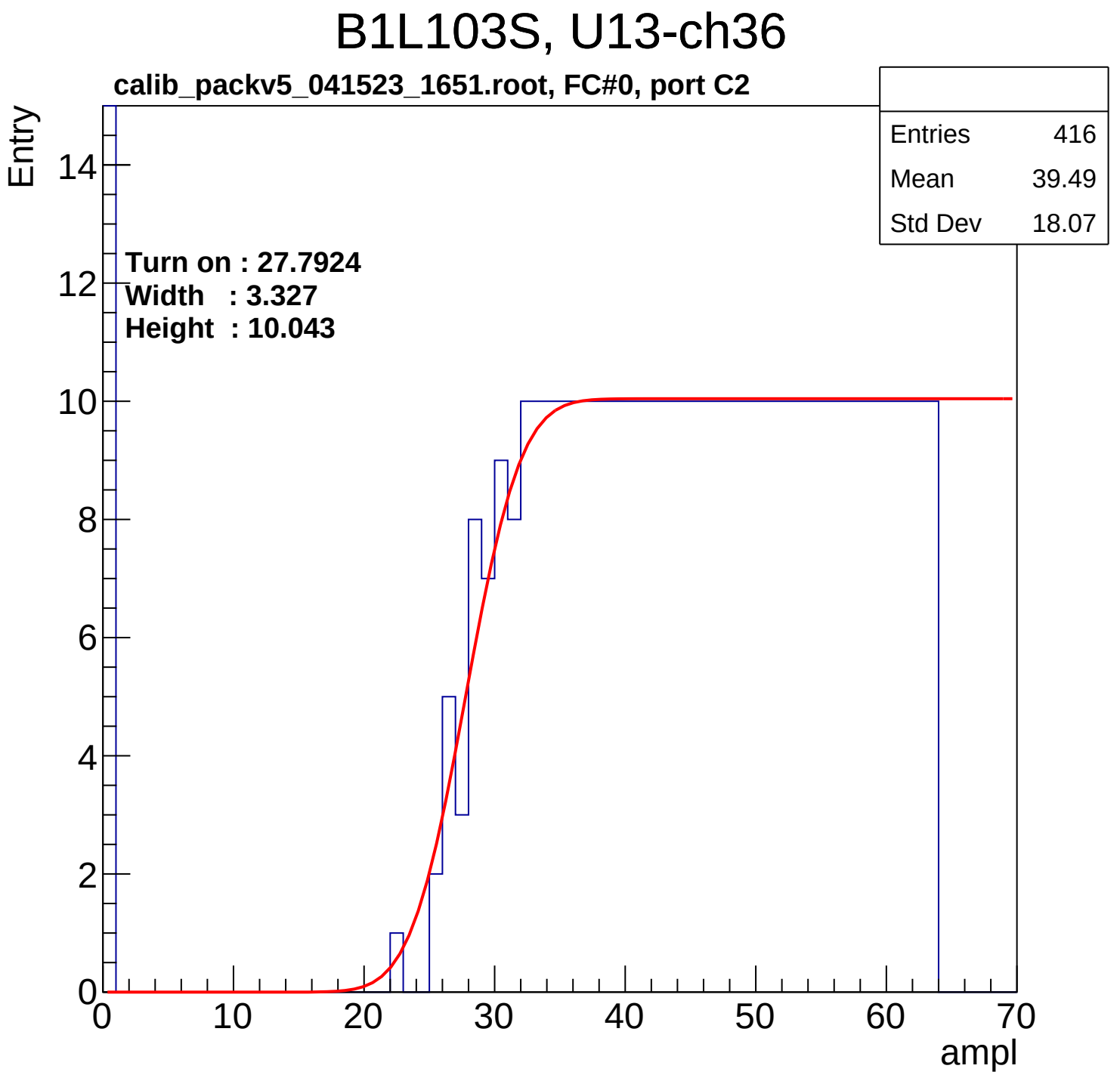
B1L103S, U13-ch36
calib_packv5_041523_1651.root, FC#0, port C2
Entries 416
Mean 39.49
Std Dev 18.07
Turn on : 27.7924
Width : 3.327
Height : 10.043
Entry
ampl
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2
4
6
8
10
12
14
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40
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60
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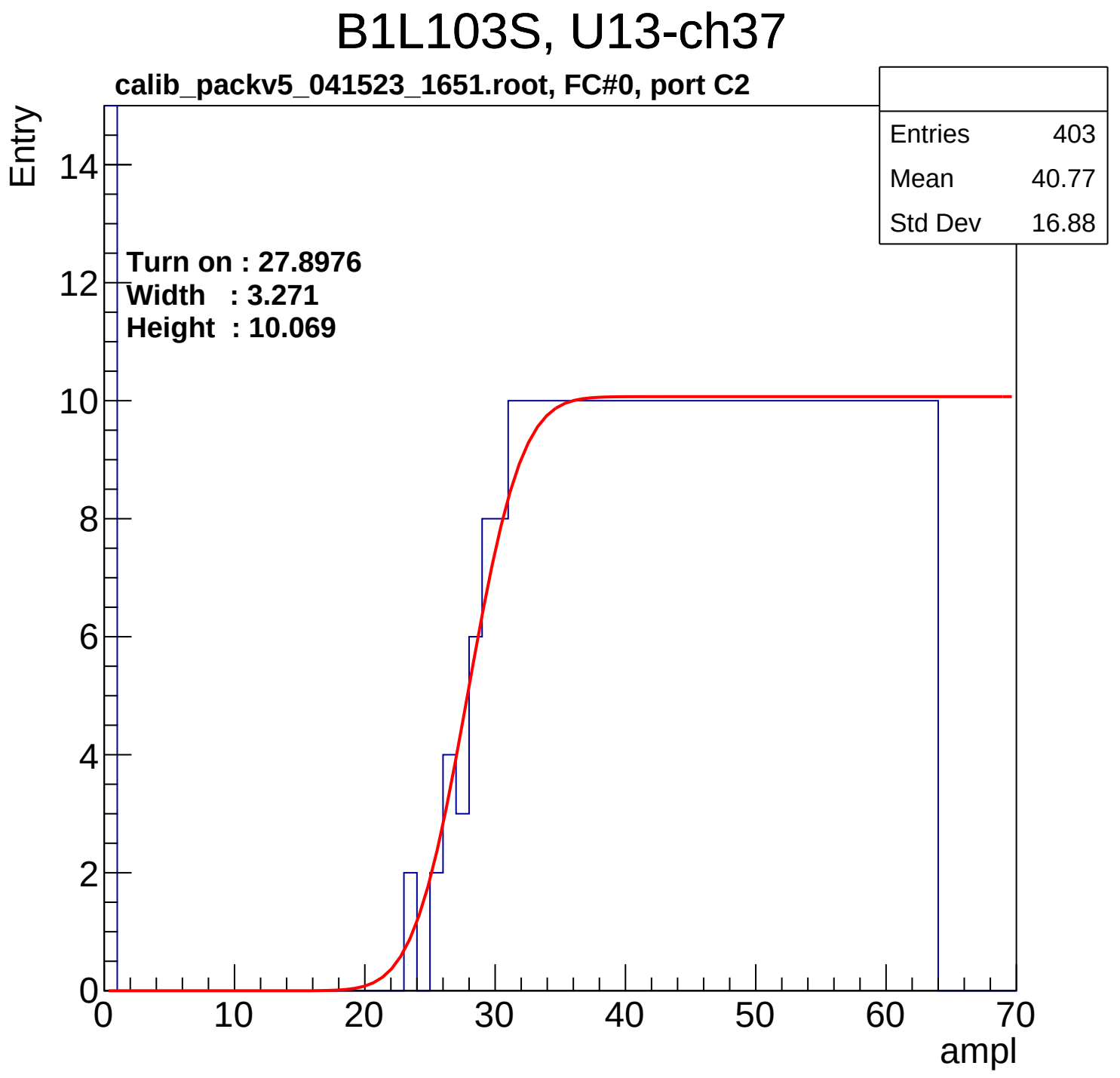
B1L103S, U13-ch37
calib_packv5_041523_1651.root, FC#0, port C2
Entries 403
Mean 40.77
Std Dev 16.88
Turn on : 27.8976
Width : 3.271
Height : 10.069
Entry
ampl
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6
8
10
12
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0
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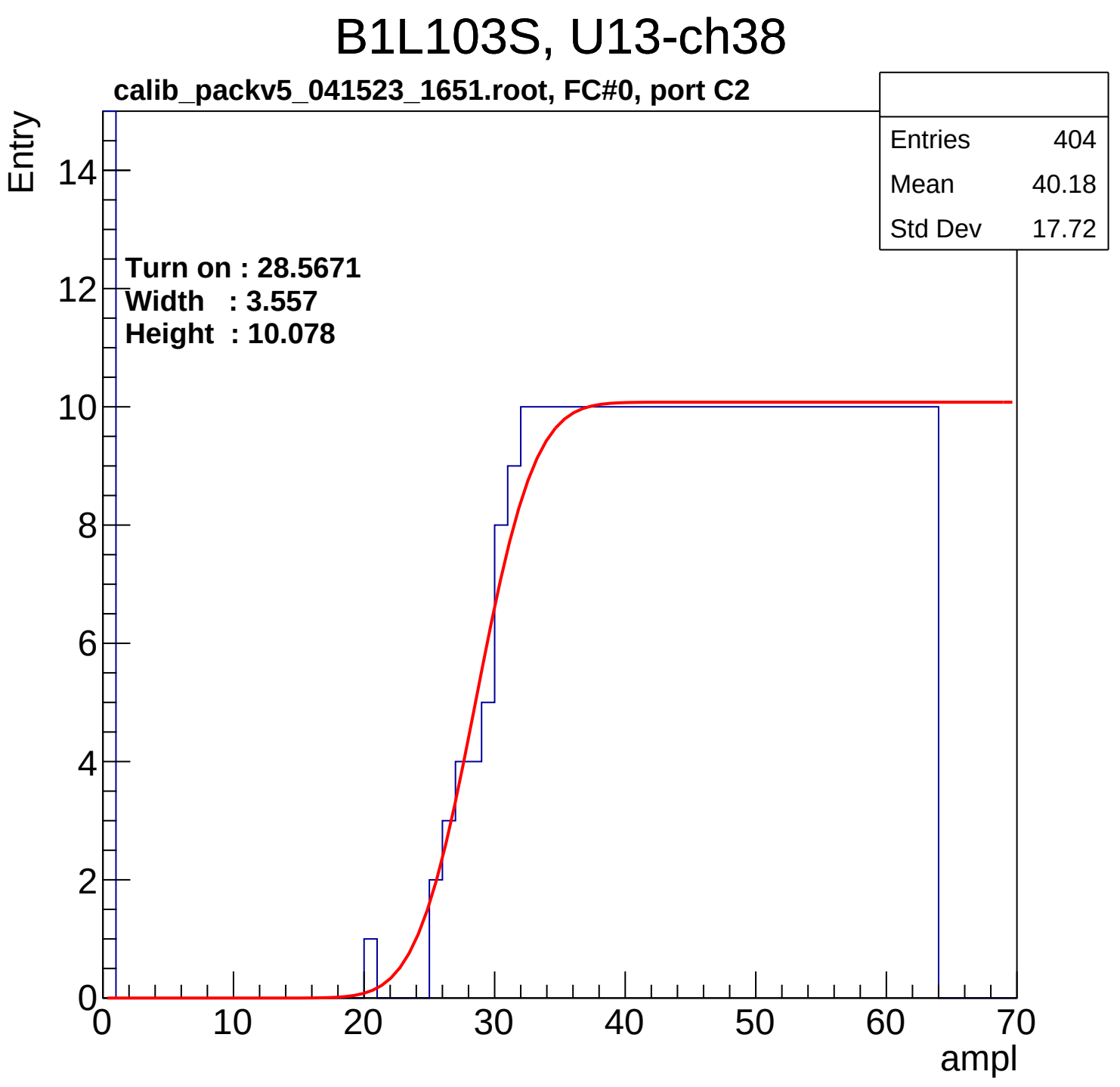
B1L103S, U13-ch38
calib_packv5_041523_1651.root, FC#0, port C2
Entries 404
Mean 40.18
Std Dev 17.72
Turn on : 28.5671
Width : 3.557
Height : 10.078
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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40
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60
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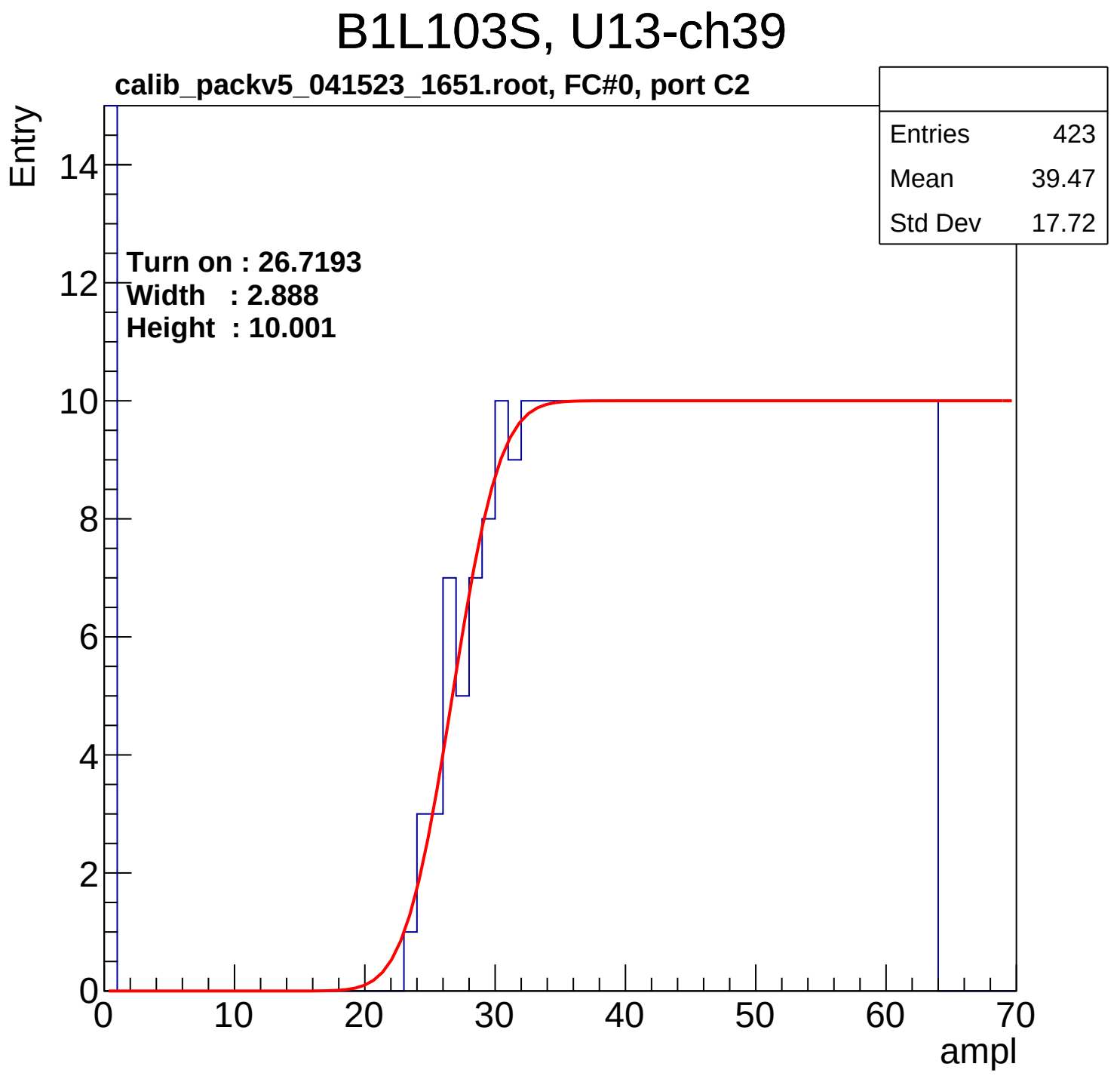
B1L103S, U13-ch39
calib_packv5_041523_1651.root, FC#0, port C2
Entries 423
Mean 39.47
Std Dev 17.72
Turn on : 26.7193
Width : 2.888
Height : 10.001
Entry
ampl
0
2
4
6
8
10
12
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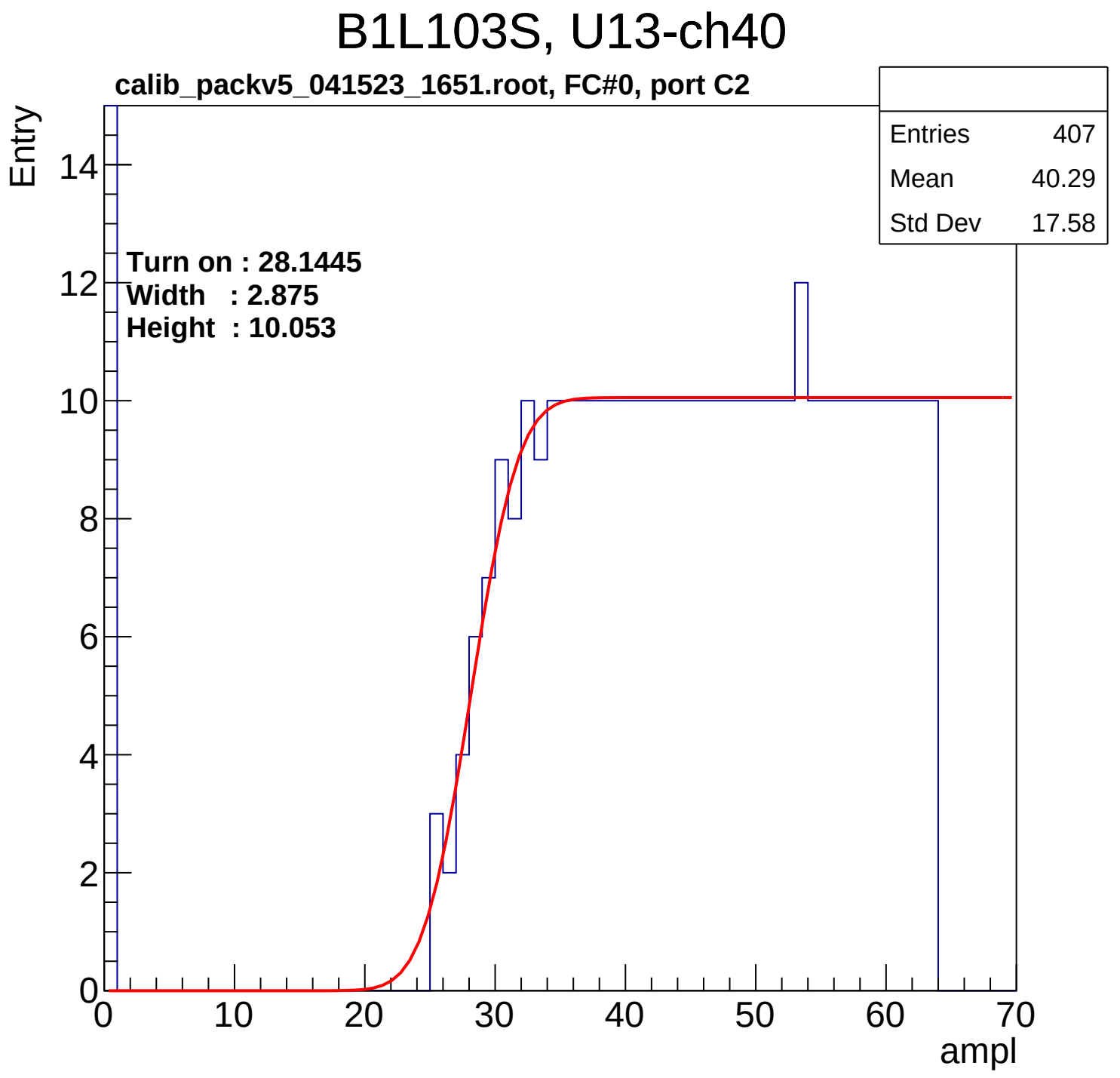
B1L103S, U13-ch40
calib_packv5_041523_1651.root, FC#0, port C2
Entries 407
Mean 40.29
Std Dev 17.58
Turn on : 28.1445
Width : 2.875
Height : 10.053
Entry
ampl
0
2
4
6
8
10
12
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0
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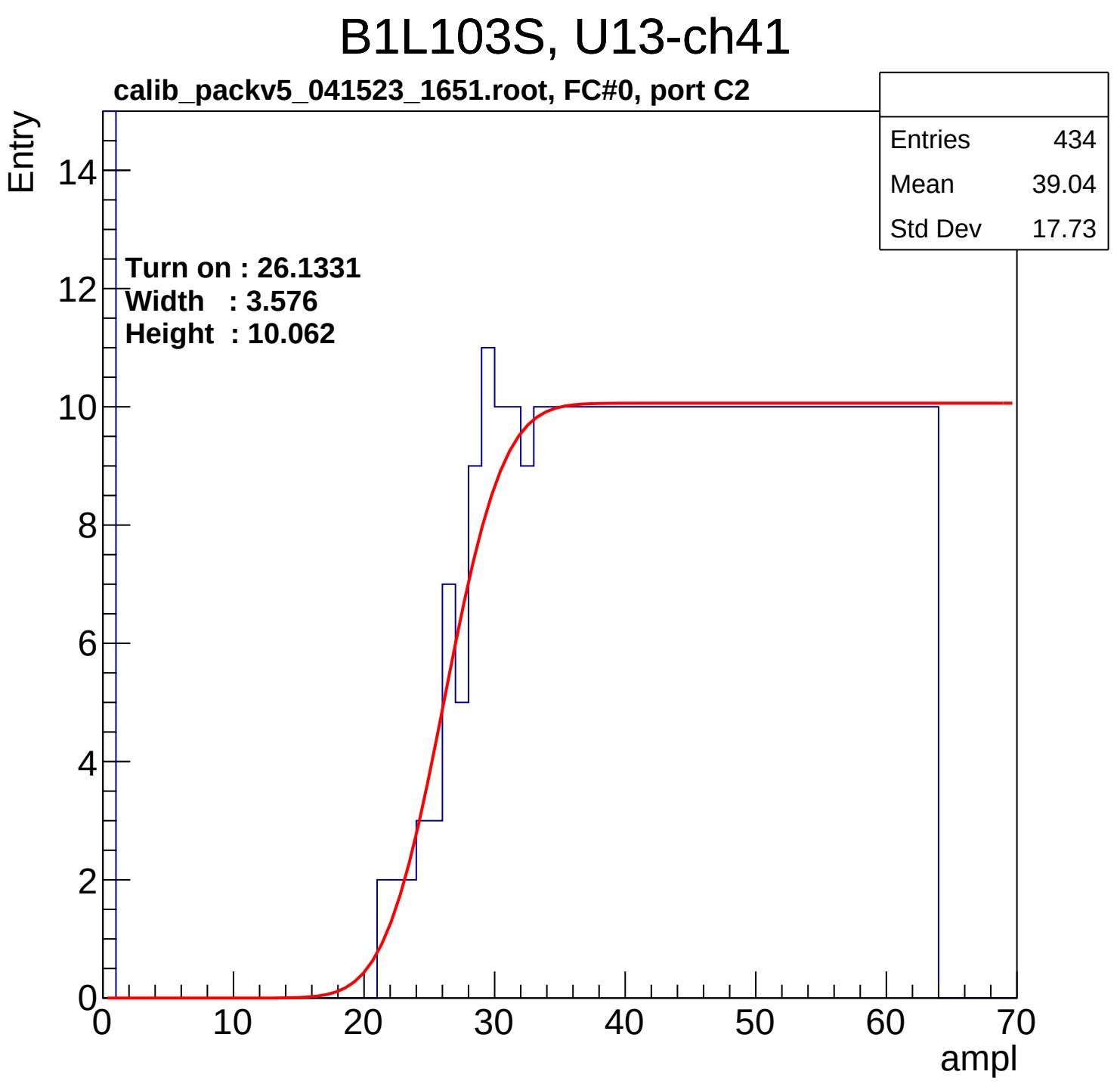
B1L103S, U13-ch41
calib_packv5_041523_1651.root, FC#0, port C2
Entries 434
Mean 39.04
Std Dev 17.73
Turn on : 26.1331
Width : 3.576
Height : 10.062
Entry
ampl
0
2
4
6
8
10
12
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0
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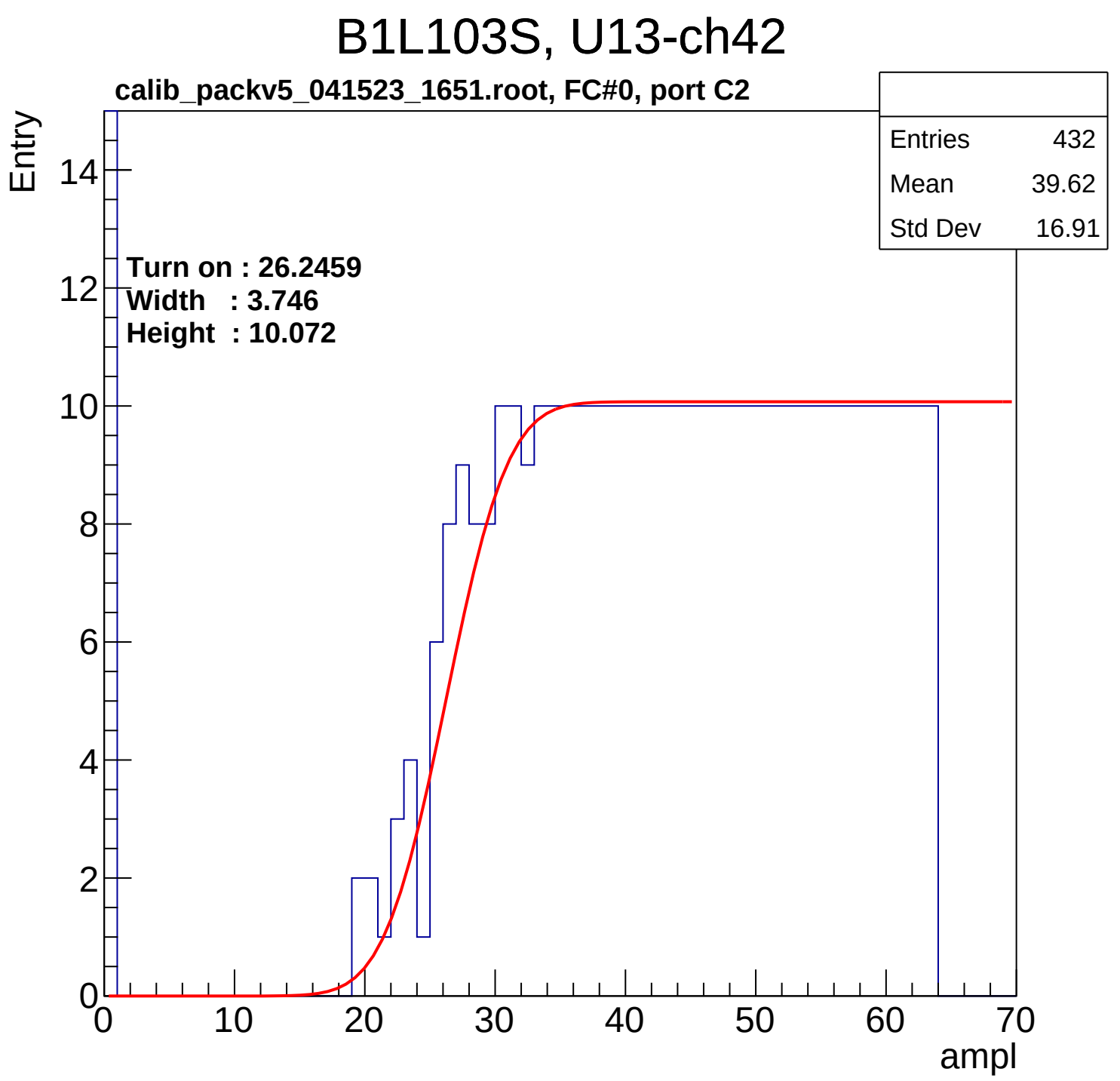
B1L103S, U13-ch42
calib_packv5_041523_1651.root, FC#0, port C2
Entries 432
Mean 39.62
Std Dev 16.91
Turn on : 26.2459
Width : 3.746
Height : 10.072
Entry
ampl
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4
6
8
10
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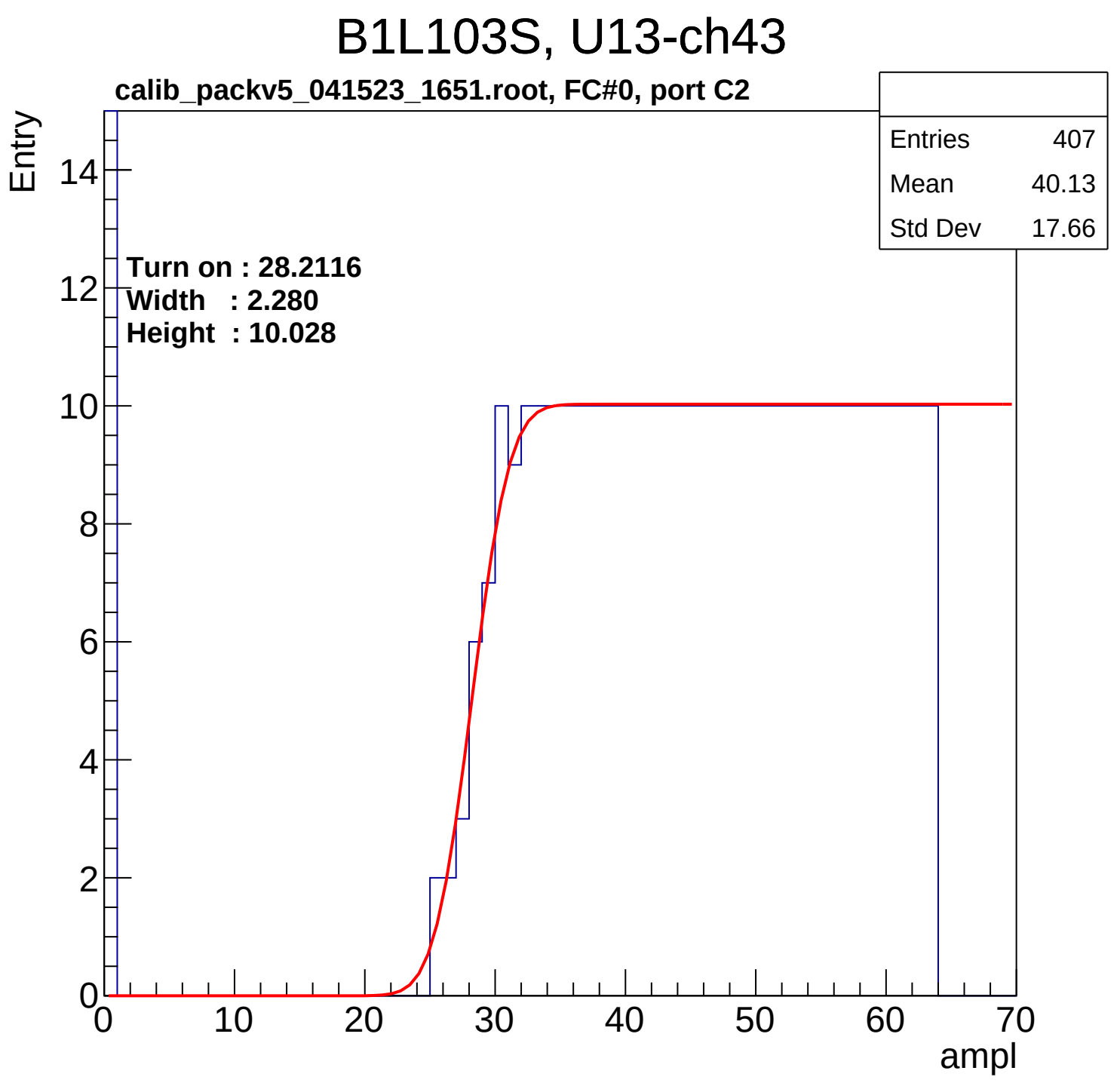
B1L103S, U13-ch43
calib_packv5_041523_1651.root, FC#0, port C2
Entries 407
Mean 40.13
Std Dev 17.66
Turn on : 28.2116
Width : 2.280
Height : 10.028
Entry
ampl
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6
8
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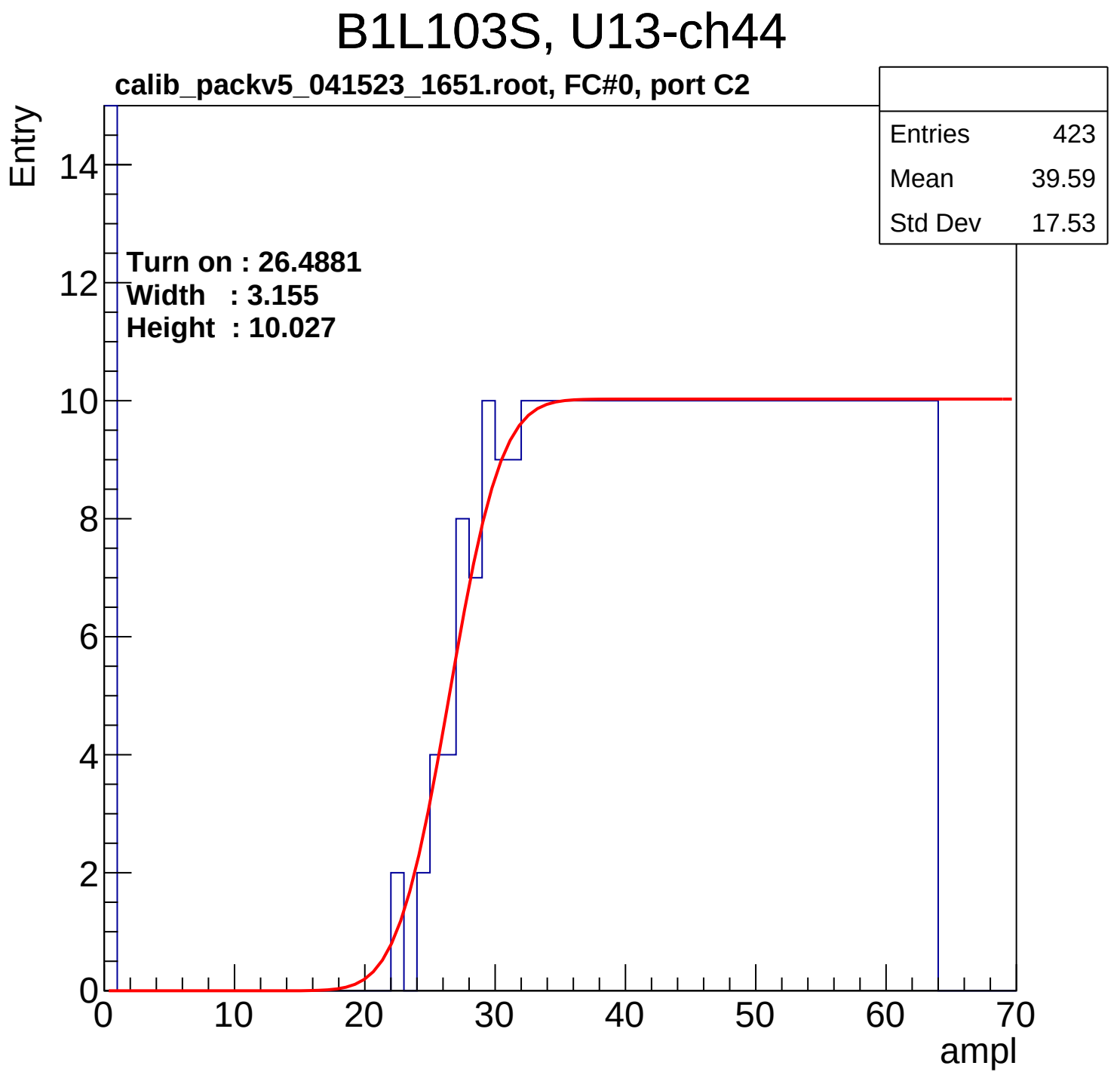
B1L103S, U13-ch44
calib_packv5_041523_1651.root, FC#0, port C2
Entries 423
Mean 39.59
Std Dev 17.53
Turn on : 26.4881
Width : 3.155
Height : 10.027
Entry
ampl
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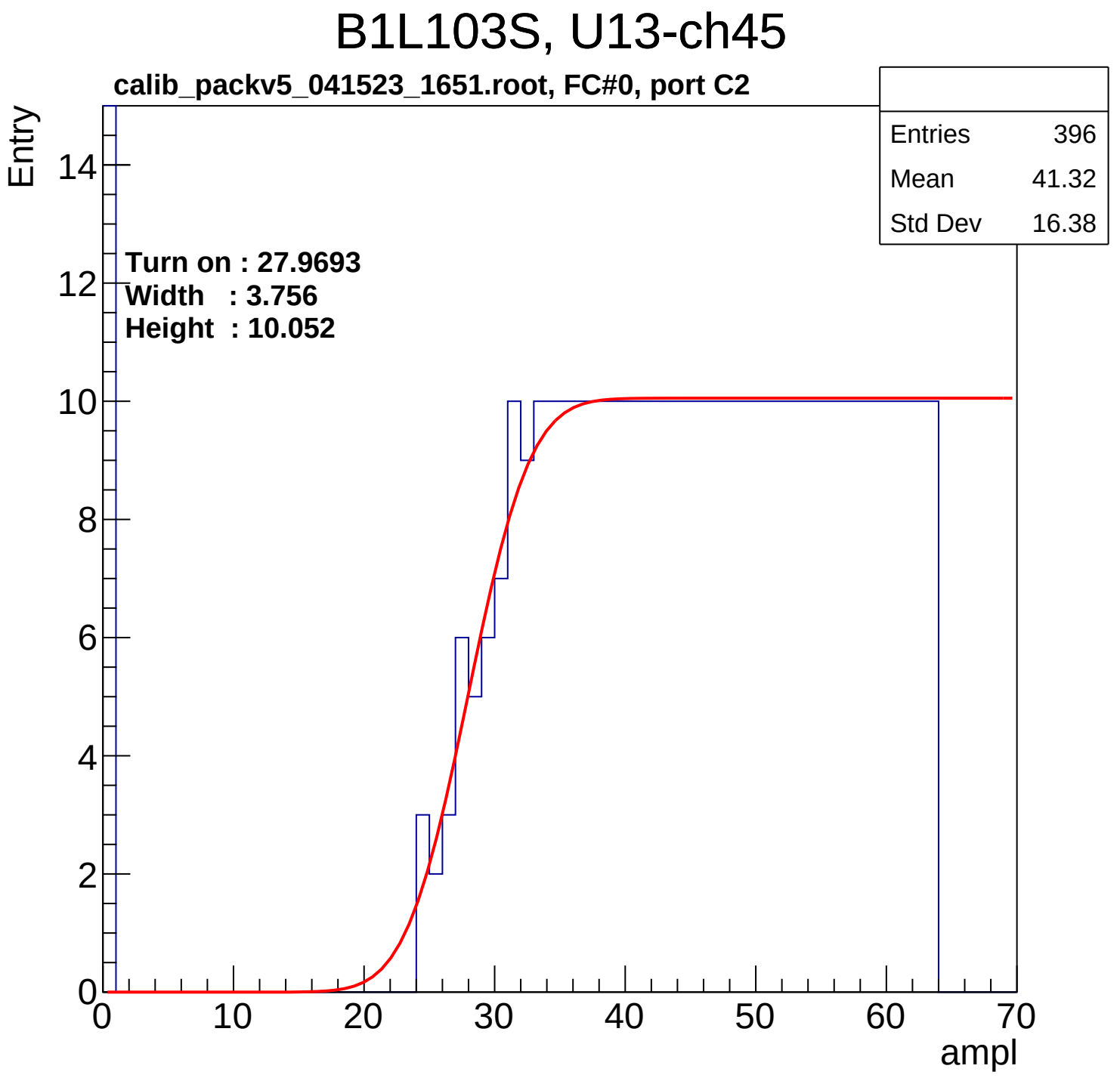
B1L103S, U13-ch45
calib_packv5_041523_1651.root, FC#0, port C2
Entries 396
Mean 41.32
Std Dev 16.38
Turn on : 27.9693
Width : 3.756
Height : 10.052
Entry
ampl
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8
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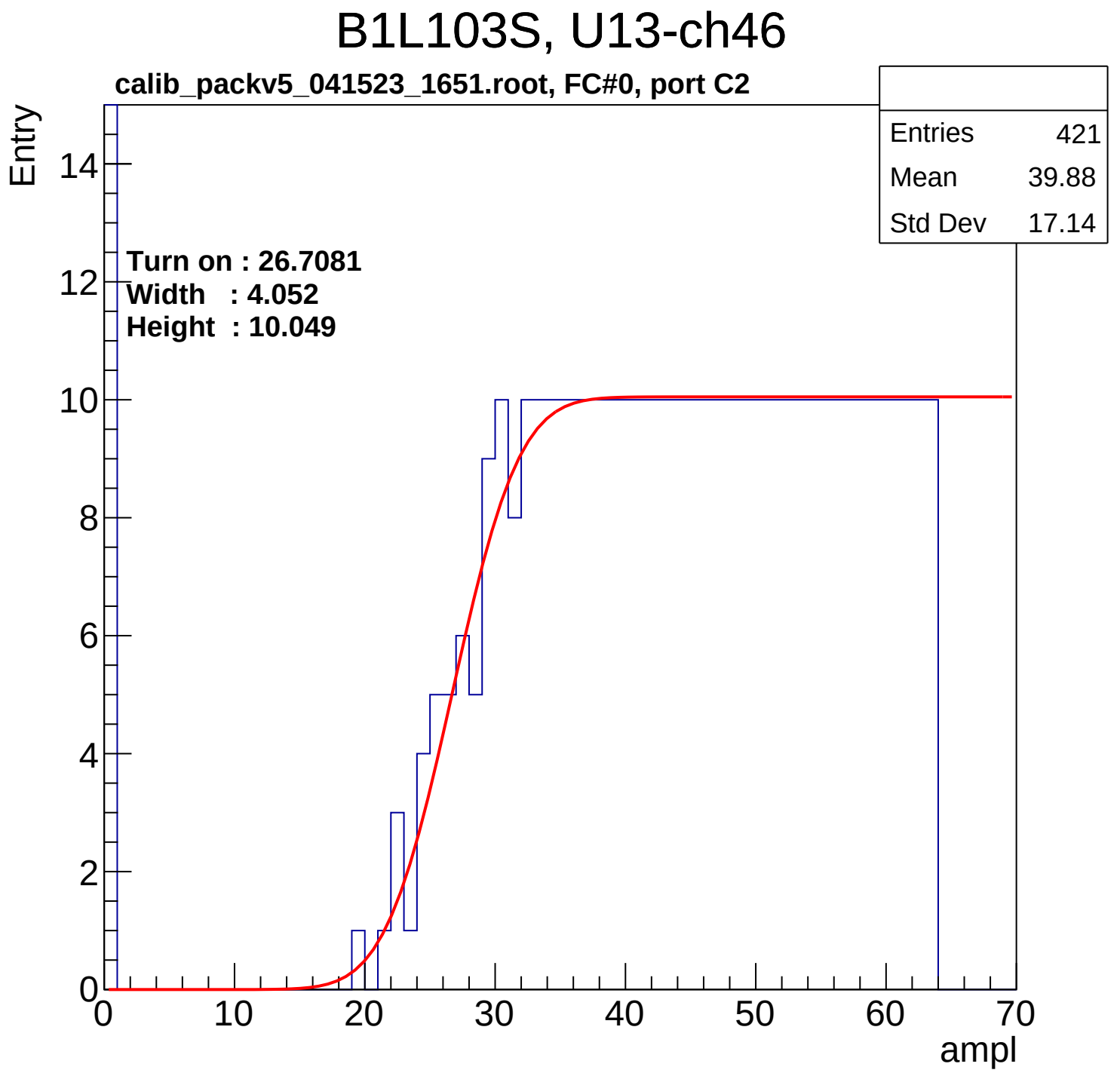
B1L103S, U13-ch46
calib_packv5_041523_1651.root, FC#0, port C2
Entries 421
Mean 39.88
Std Dev 17.14
Turn on : 26.7081
Width : 4.052
Height : 10.049
Entry
ampl
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2
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6
8
10
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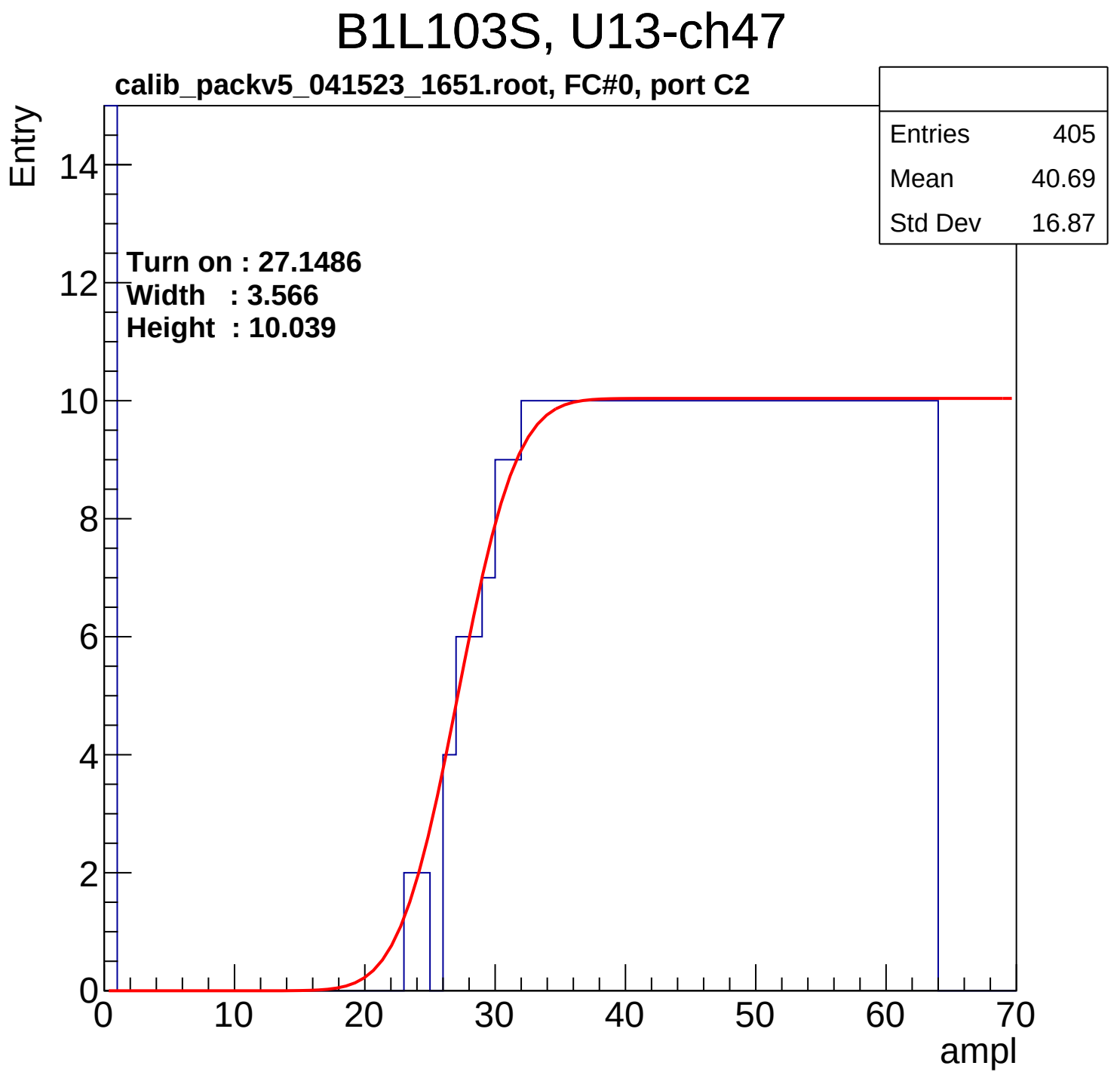
B1L103S, U13-ch47
calib_packv5_041523_1651.root, FC#0, port C2
Entries 405
Mean 40.69
Std Dev 16.87
Turn on : 27.1486
Width : 3.566
Height : 10.039
Entry
ampl
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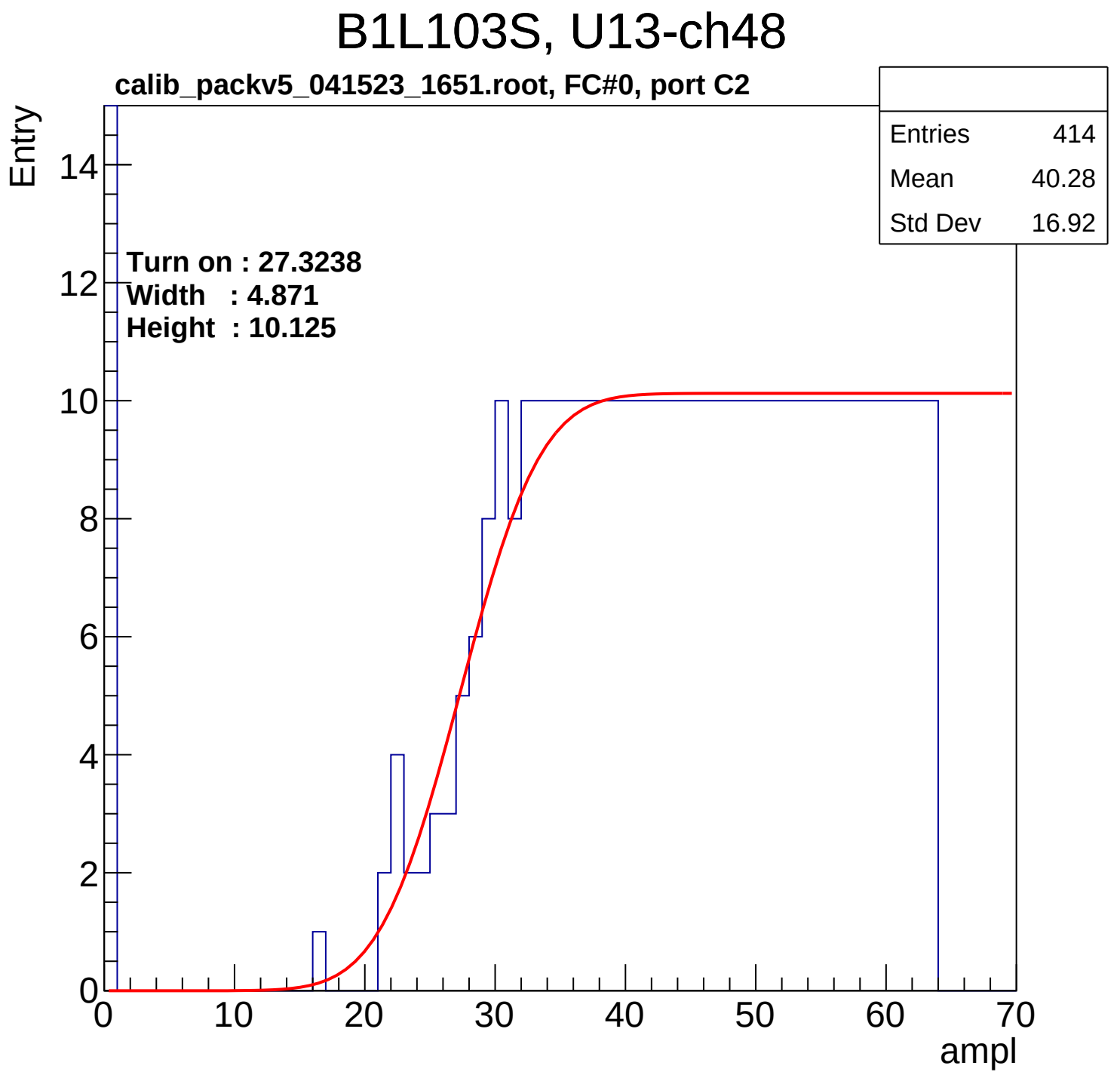
B1L103S, U13-ch48
calib_packv5_041523_1651.root, FC#0, port C2
Entries 414
Mean 40.28
Std Dev 16.92
Turn on : 27.3238
Width : 4.871
Height : 10.125
Entry
ampl
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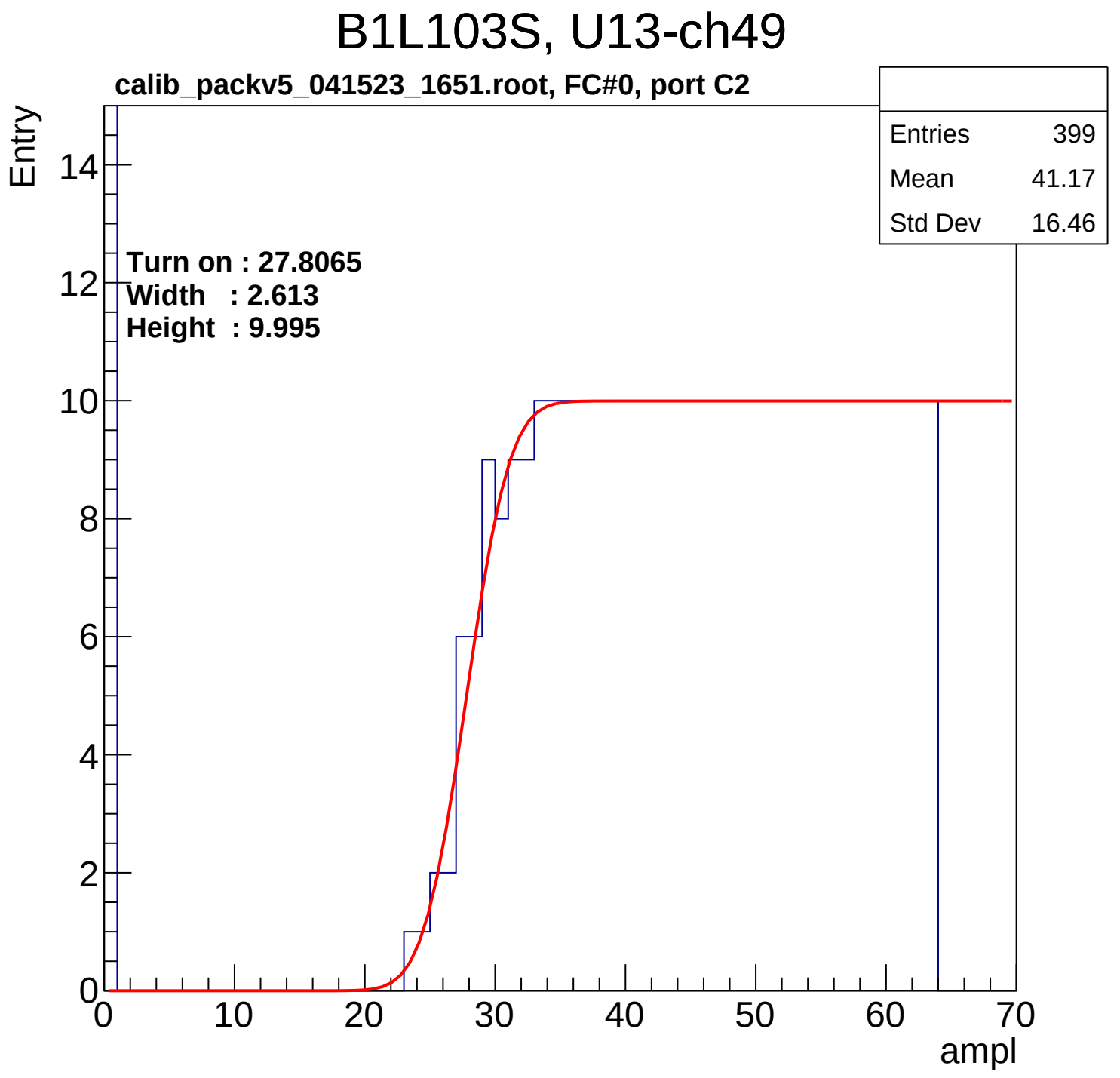
B1L103S, U13-ch49
calib_packv5_041523_1651.root, FC#0, port C2
Entries 399
Mean 41.17
Std Dev 16.46
Turn on : 27.8065
Width : 2.613
Height : 9.995
Entry
ampl
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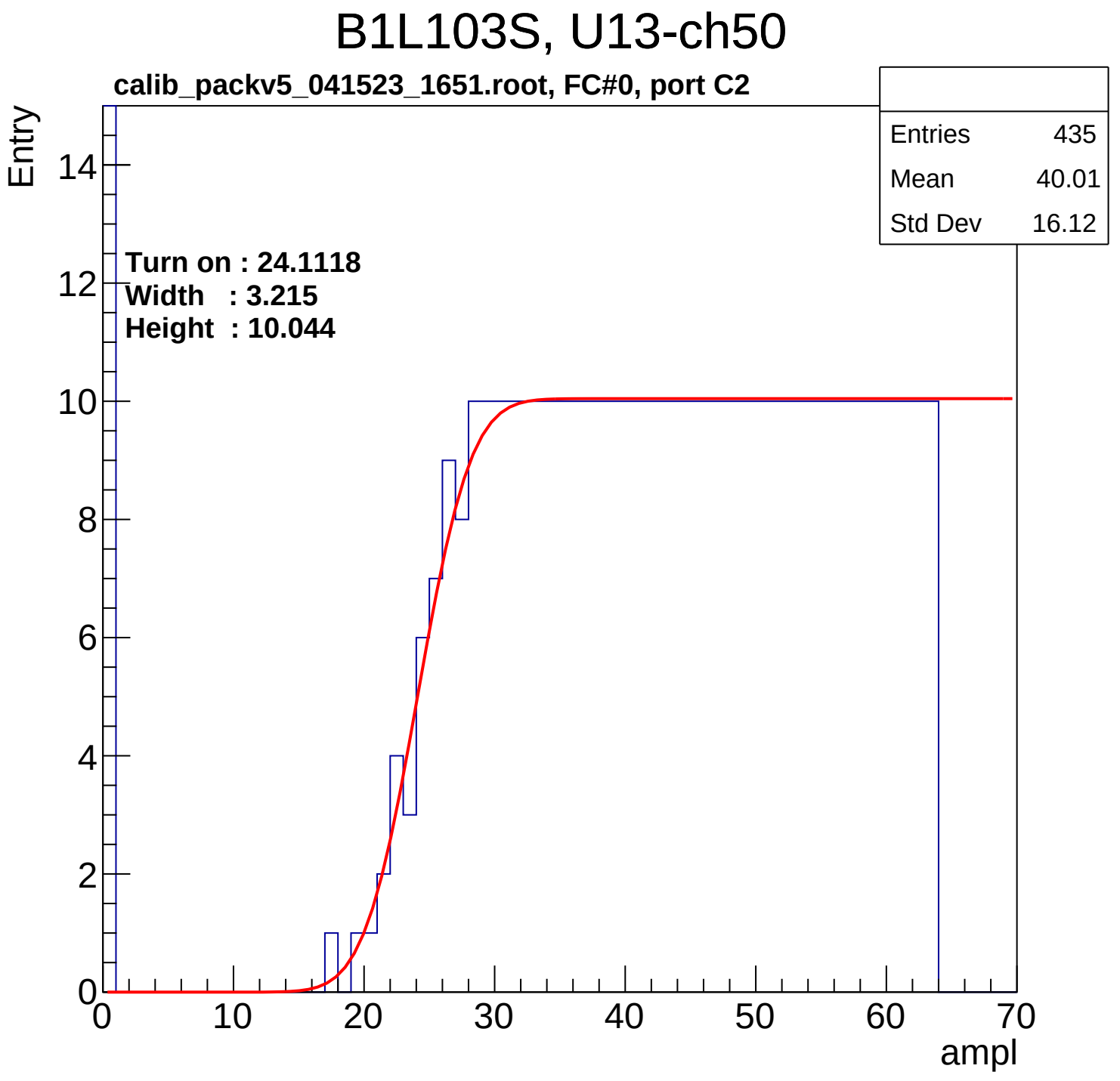
B1L103S, U13-ch50
calib_packv5_041523_1651.root, FC#0, port C2
Entries 435
Mean 40.01
Std Dev 16.12
Turn on : 24.1118
Width : 3.215
Height : 10.044
Entry
ampl
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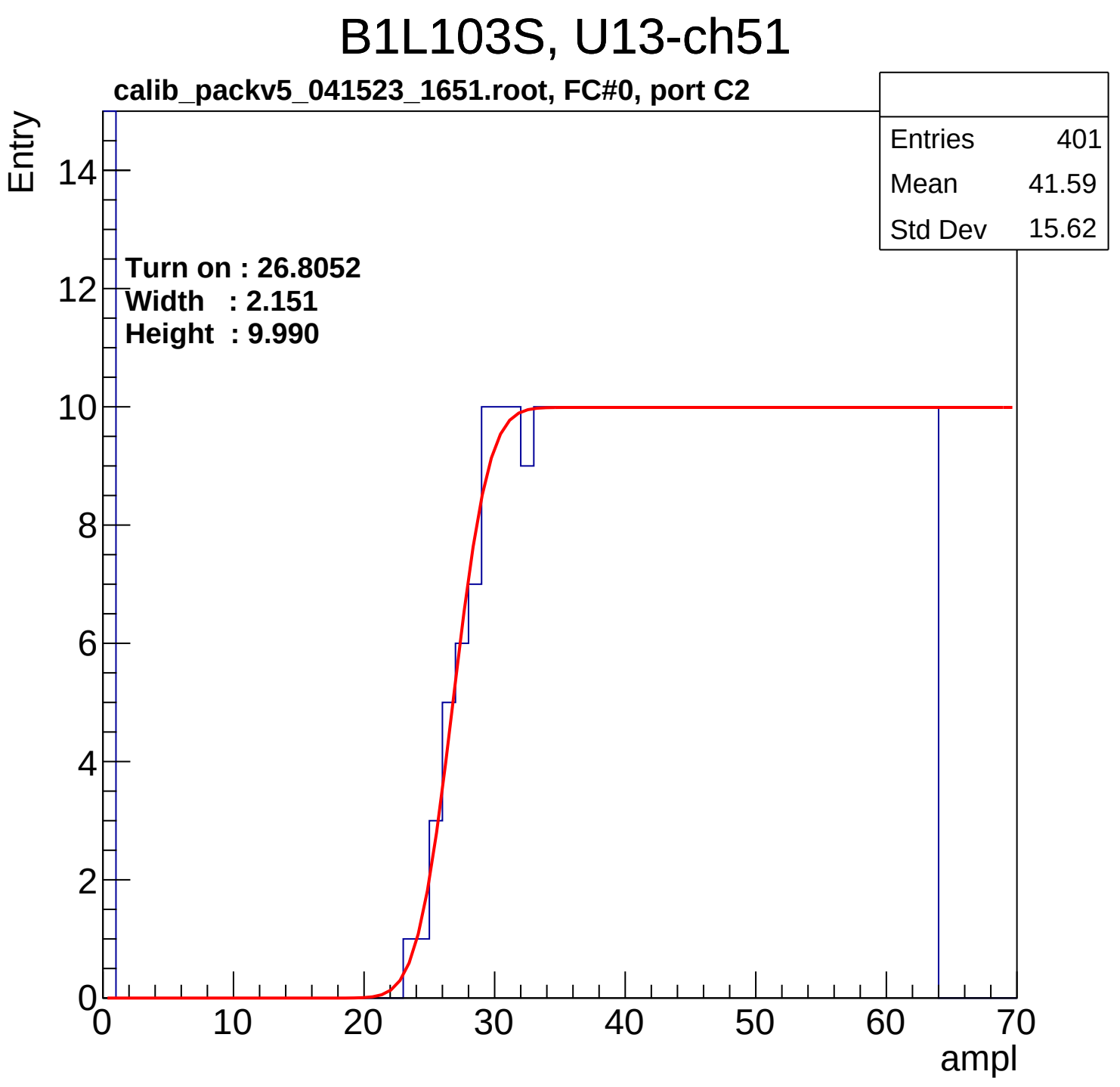
B1L103S, U13-ch51
calib_packv5_041523_1651.root, FC#0, port C2
Entries 401
Mean 41.59
Std Dev 15.62
Turn on : 26.8052
Width : 2.151
Height : 9.990
Entry
ampl
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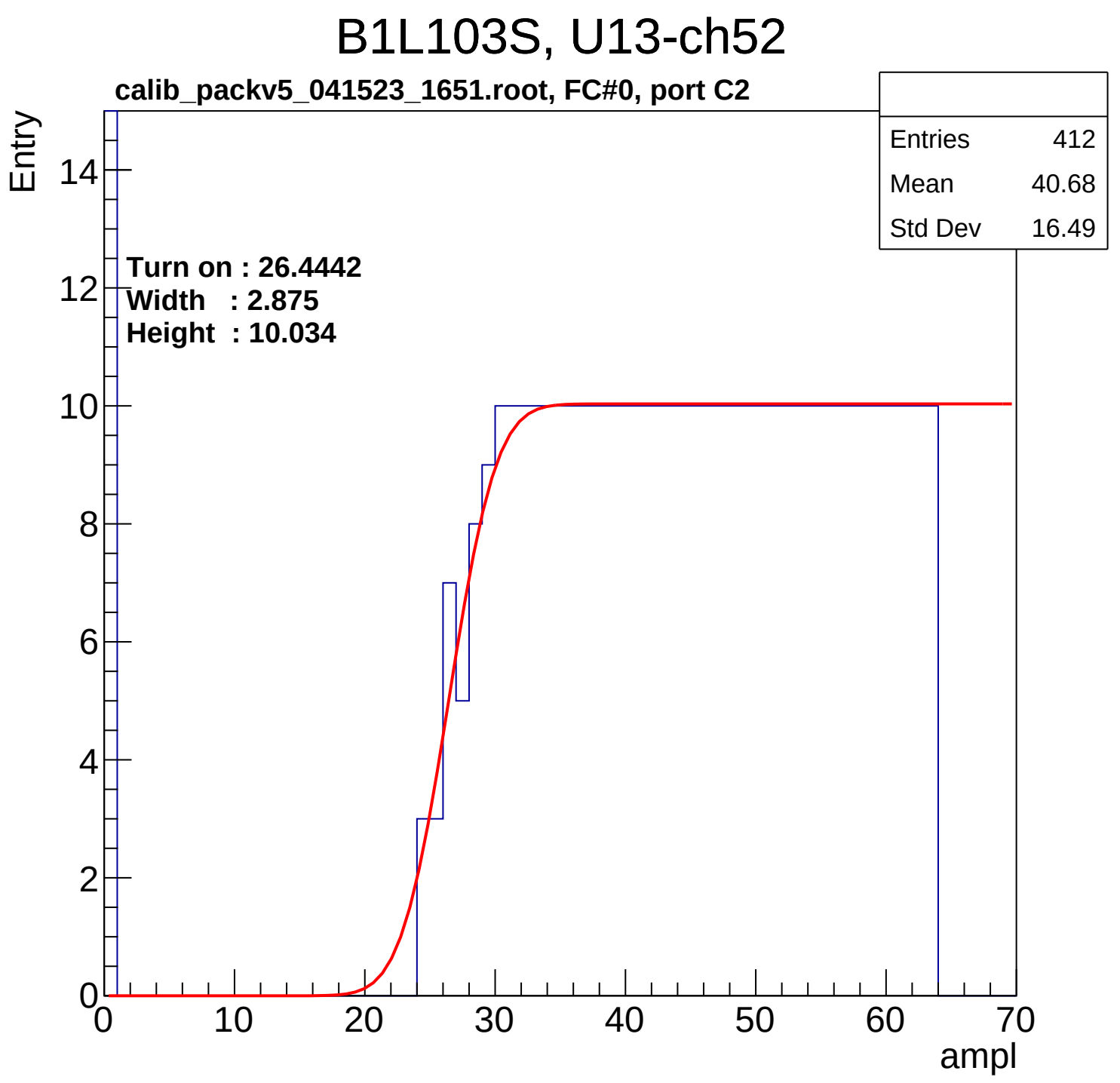
B1L103S, U13-ch52
calib_packv5_041523_1651.root, FC#0, port C2
Entries 412
Mean 40.68
Std Dev 16.49
Turn on : 26.4442
Width : 2.875
Height : 10.034
Entry
ampl
0
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8
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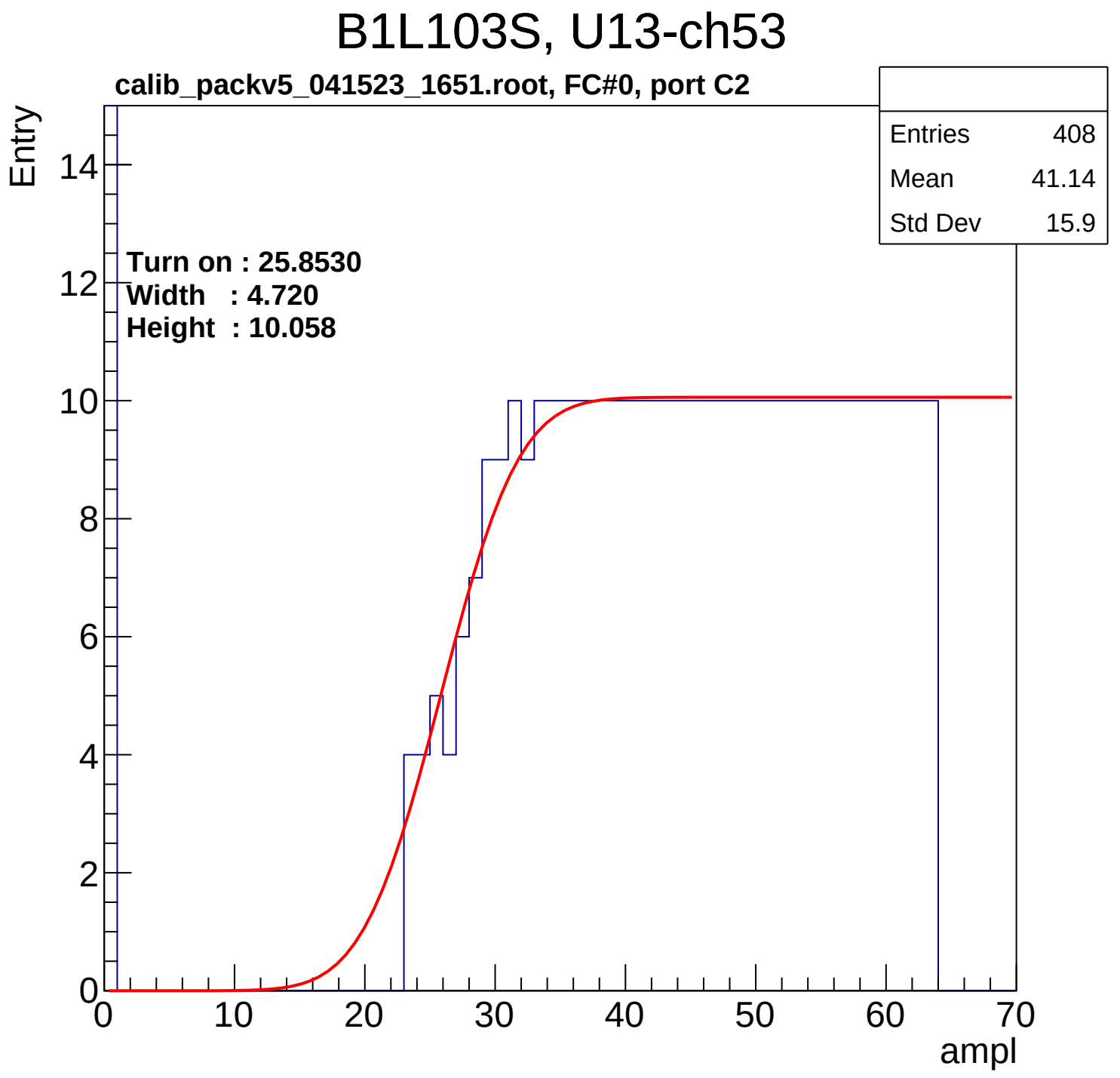
B1L103S, U13-ch53
calib_packv5_041523_1651.root, FC#0, port C2
Entries 408
Mean 41.14
Std Dev 15.9
Turn on : 25.8530
Width : 4.720
Height : 10.058
Entry
ampl
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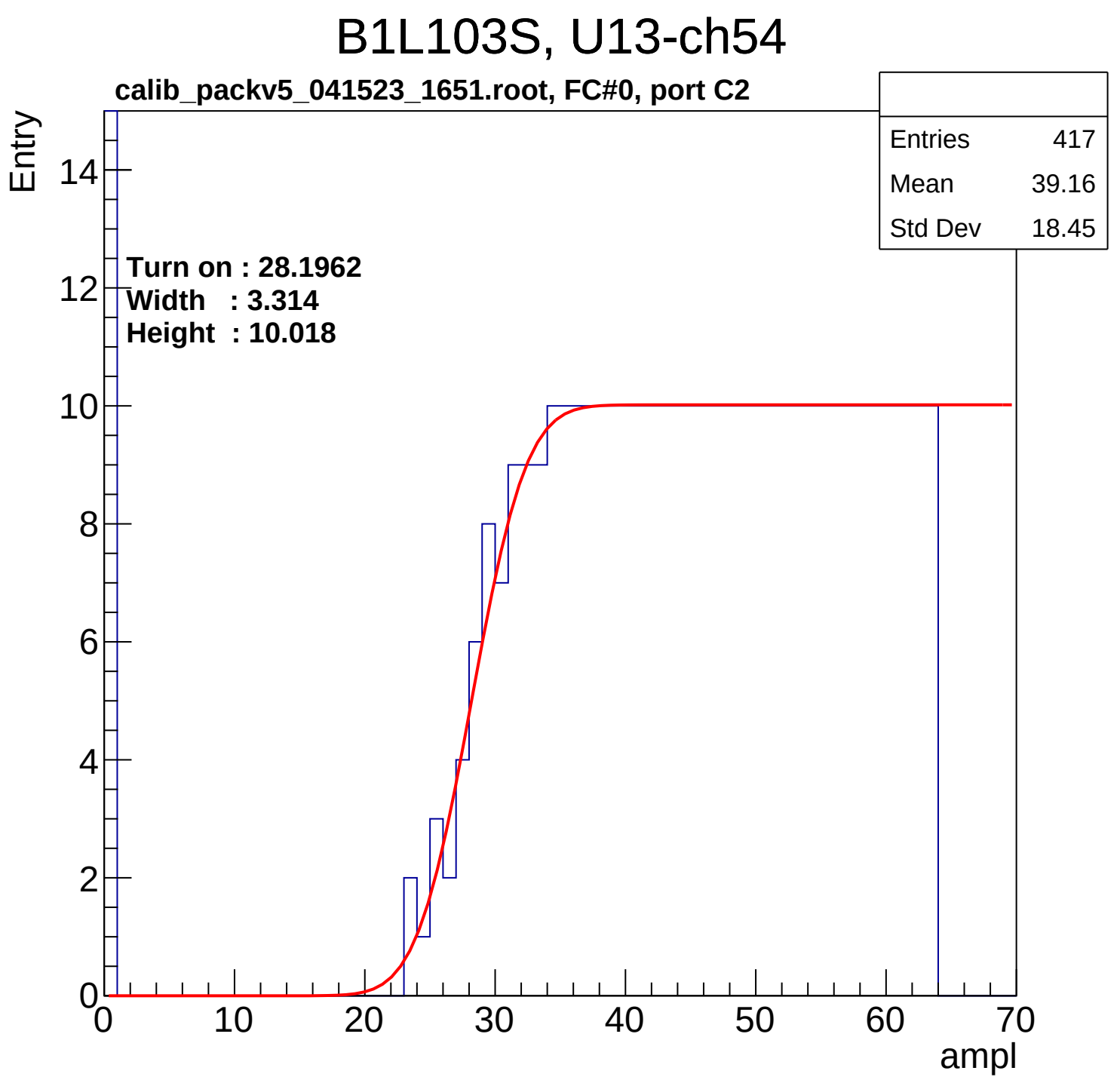
B1L103S, U13-ch54
calib_packv5_041523_1651.root, FC#0, port C2
Entries 417
Mean 39.16
Std Dev 18.45
Turn on : 28.1962
Width : 3.314
Height : 10.018
Entry
ampl
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6
8
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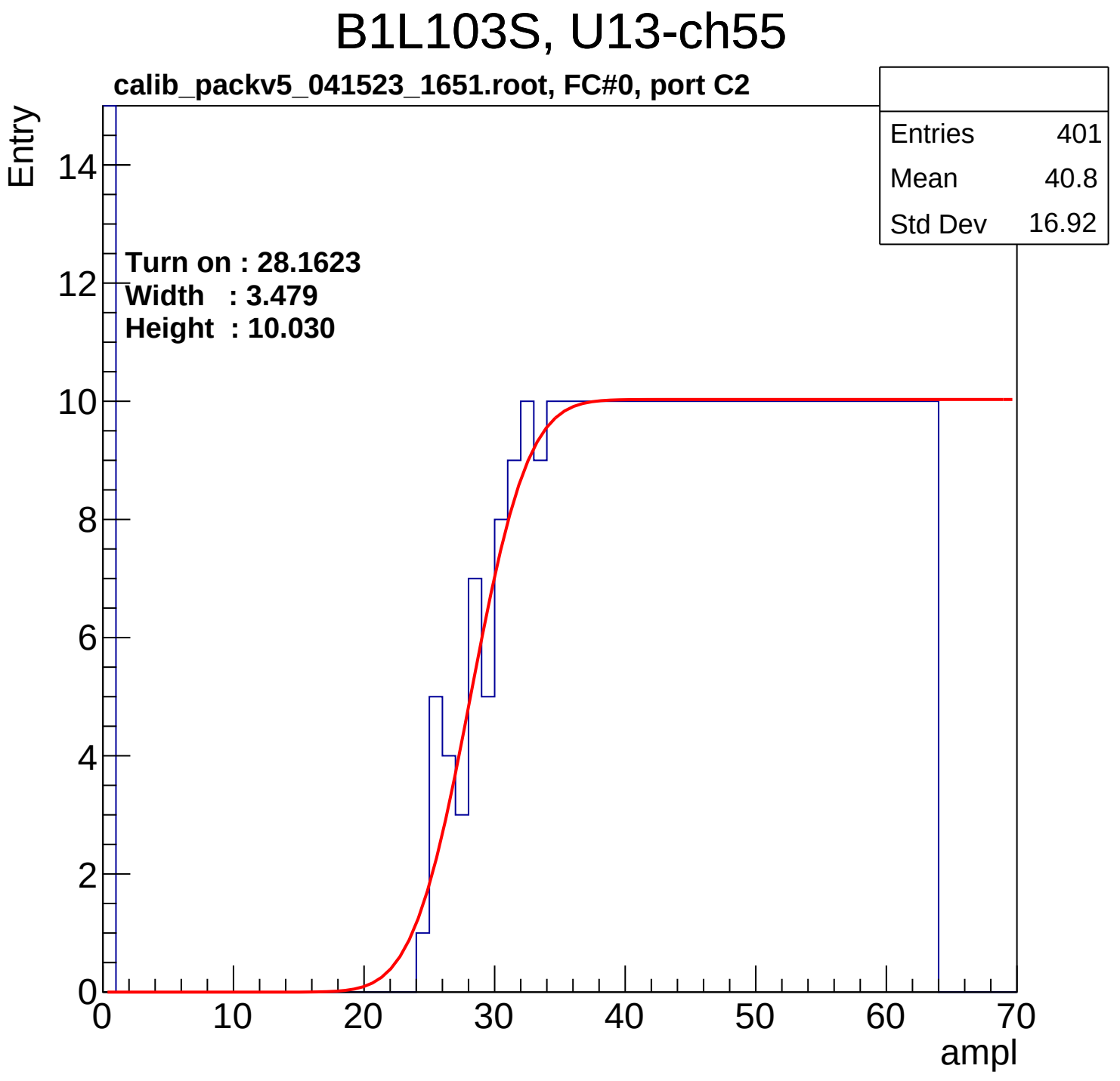
B1L103S, U13-ch55
calib_packv5_041523_1651.root, FC#0, port C2
Entries 401
Mean 40.8
Std Dev 16.92
Turn on : 28.1623
Width : 3.479
Height : 10.030
Entry
ampl
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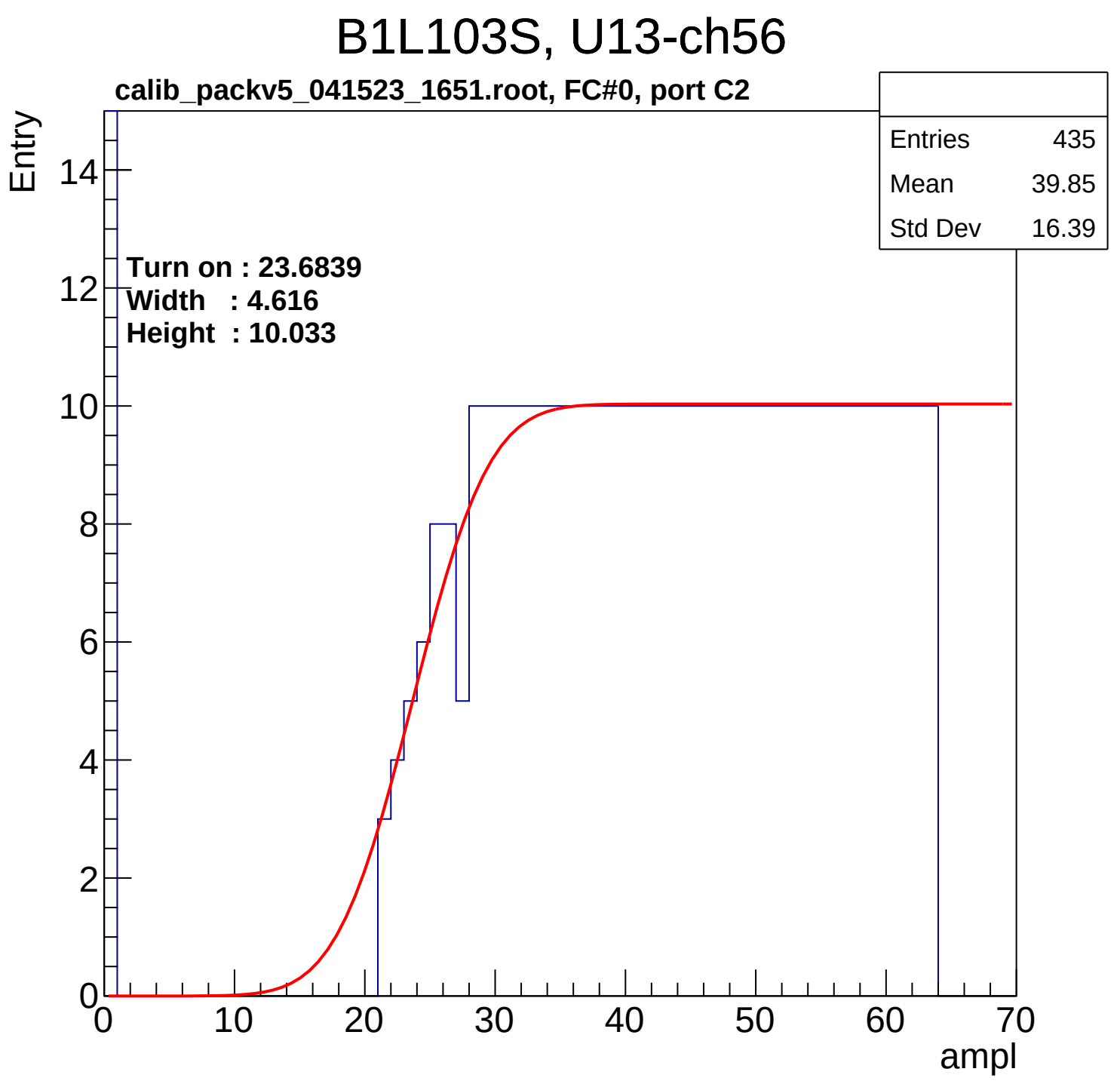
B1L103S, U13-ch56
calib_packv5_041523_1651.root, FC#0, port C2
Entries 435
Mean 39.85
Std Dev 16.39
Turn on : 23.6839
Width : 4.616
Height : 10.033
Entry
ampl
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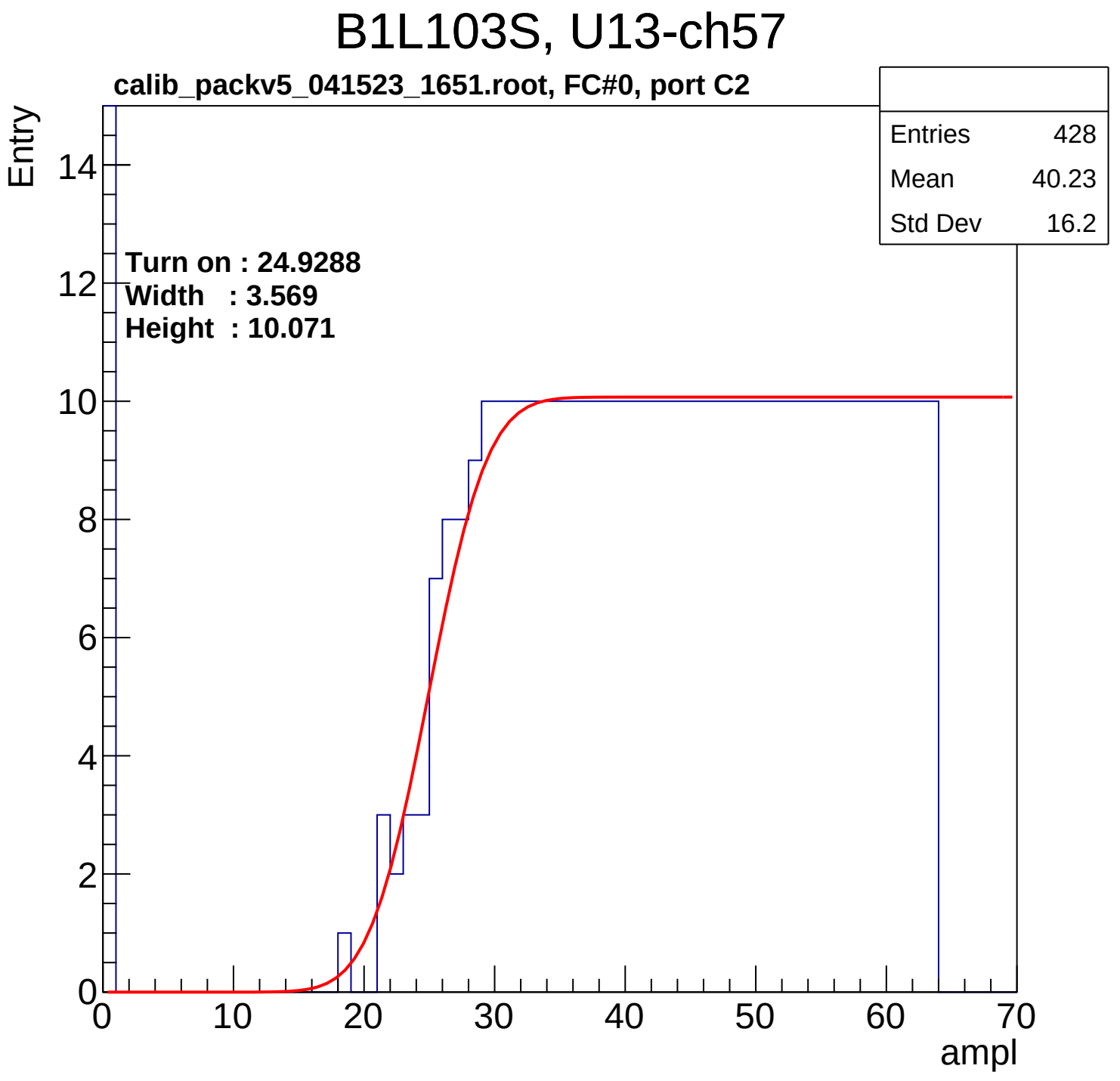
B1L103S, U13-ch57
calib_packv5_041523_1651.root, FC#0, port C2
Entries 428
Mean 40.23
Std Dev 16.2
Turn on : 24.9288
Width : 3.569
Height : 10.071
Entry
ampl
0
2
4
6
8
10
12
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10
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50
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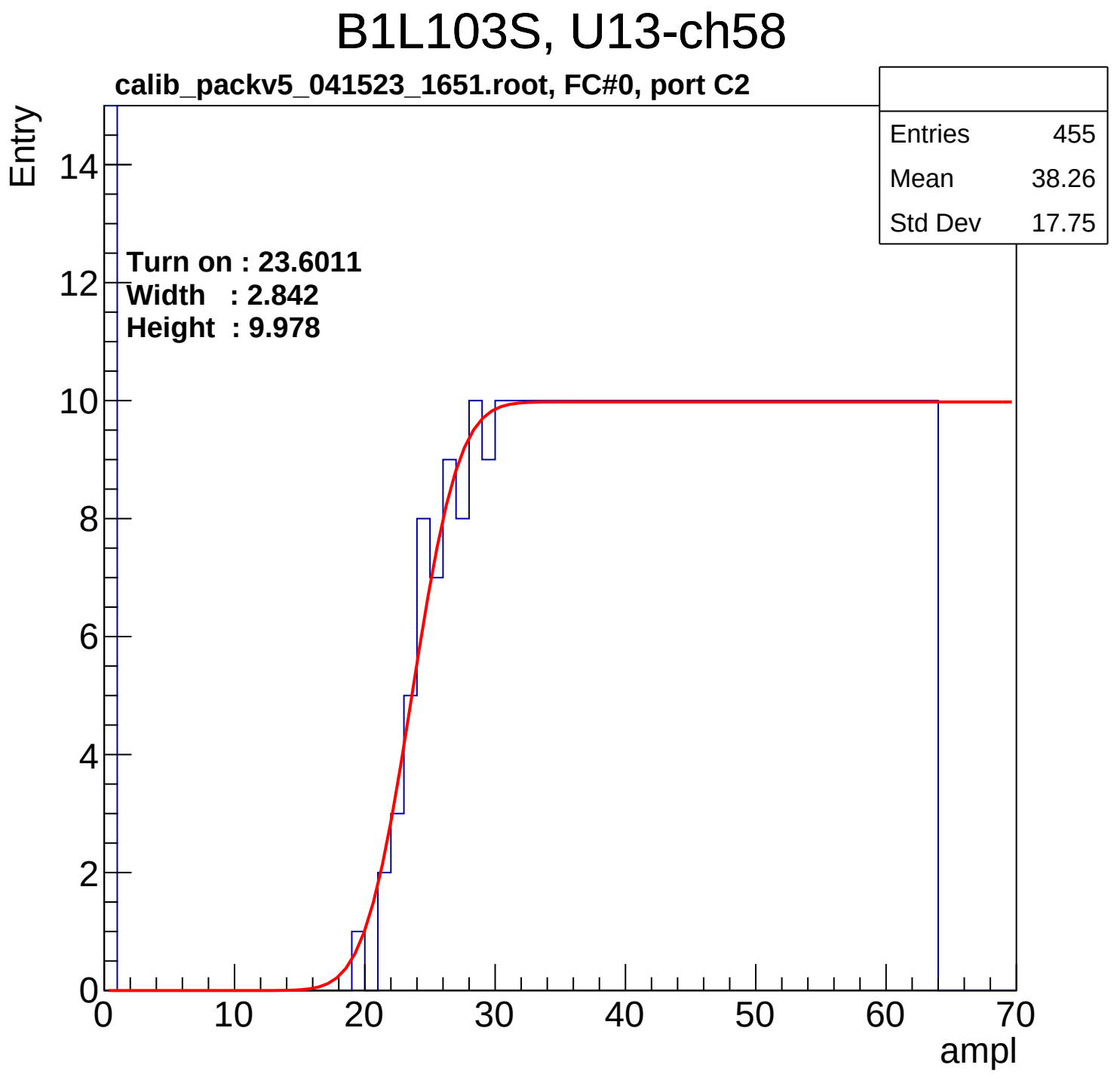
B1L103S, U13-ch58
calib_packv5_041523_1651.root, FC#0, port C2
Entries 455
Mean 38.26
Std Dev 17.75
Turn on : 23.6011
Width : 2.842
Height : 9.978
Entry
ampl
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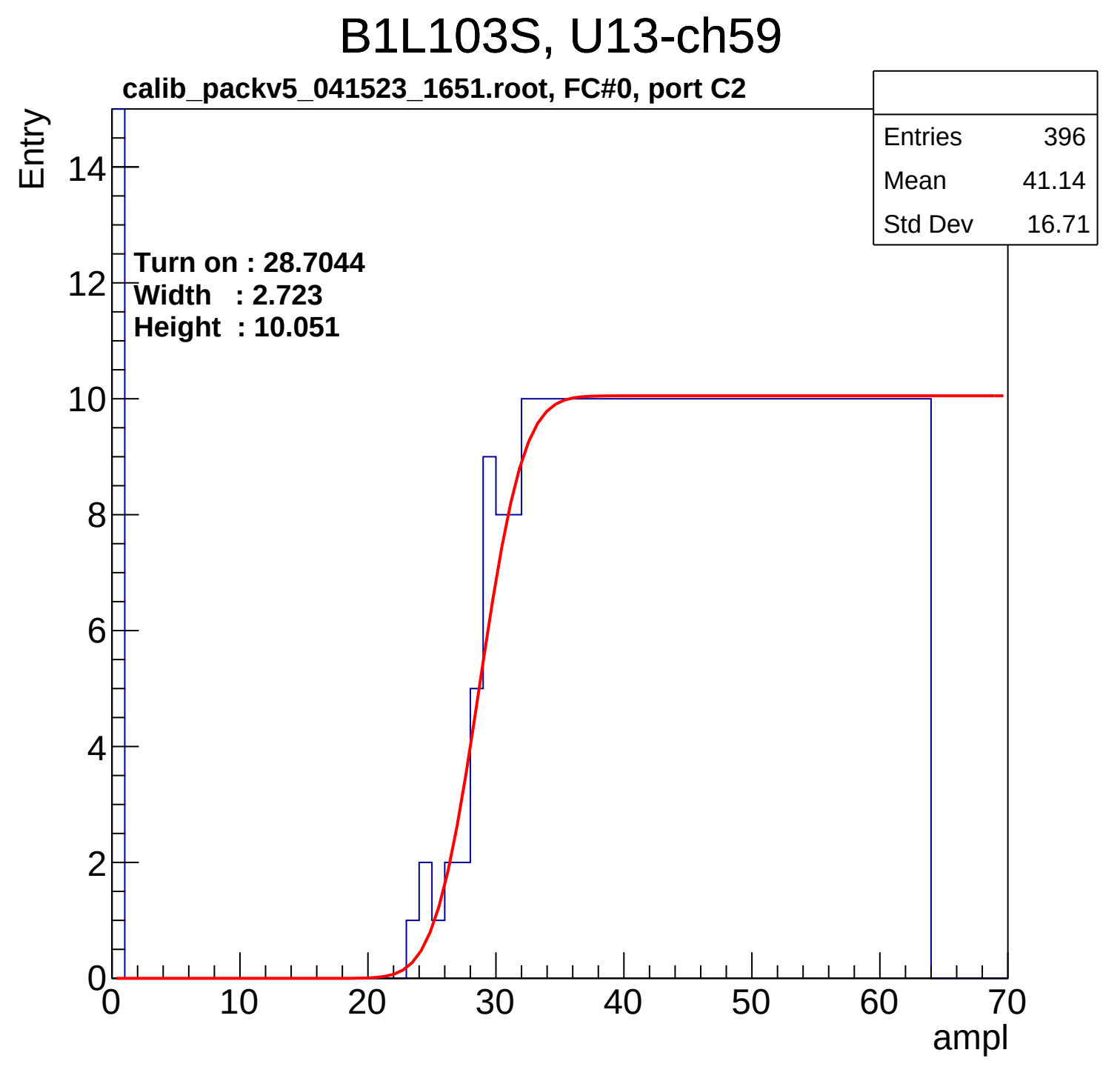
B1L103S, U13-ch59
calib_packv5_041523_1651.root, FC#0, port C2
Entries 396
Mean 41.14
Std Dev 16.71
Turn on : 28.7044
Width : 2.723
Height : 10.051
Entry
ampl
0
2
4
6
8
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0
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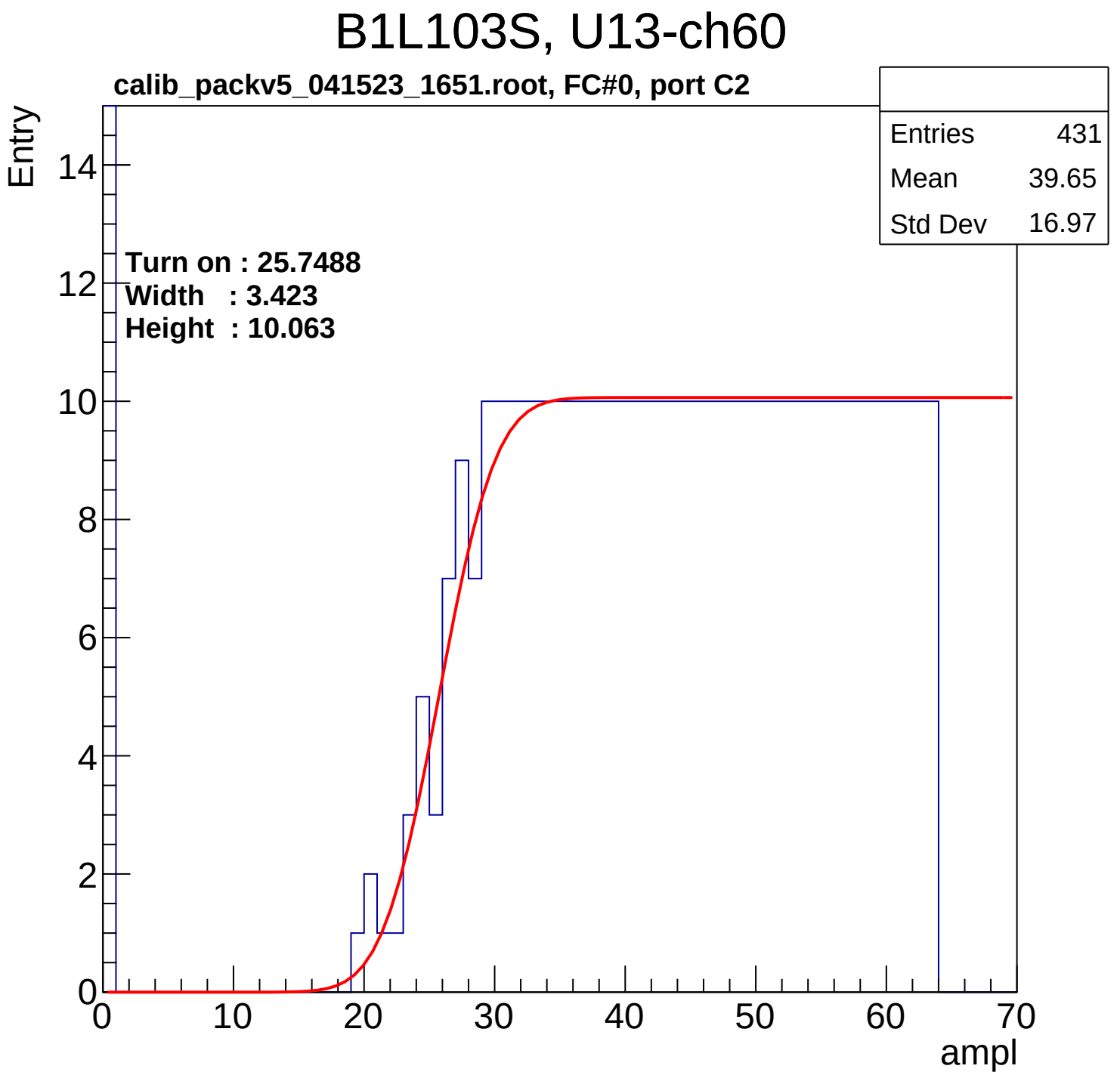
B1L103S, U13-ch60
calib_packv5_041523_1651.root, FC#0, port C2
Entries 431
Mean 39.65
Std Dev 16.97
Turn on : 25.7488
Width : 3.423
Height : 10.063
Entry
ampl
0
2
4
6
8
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12
14
0
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60
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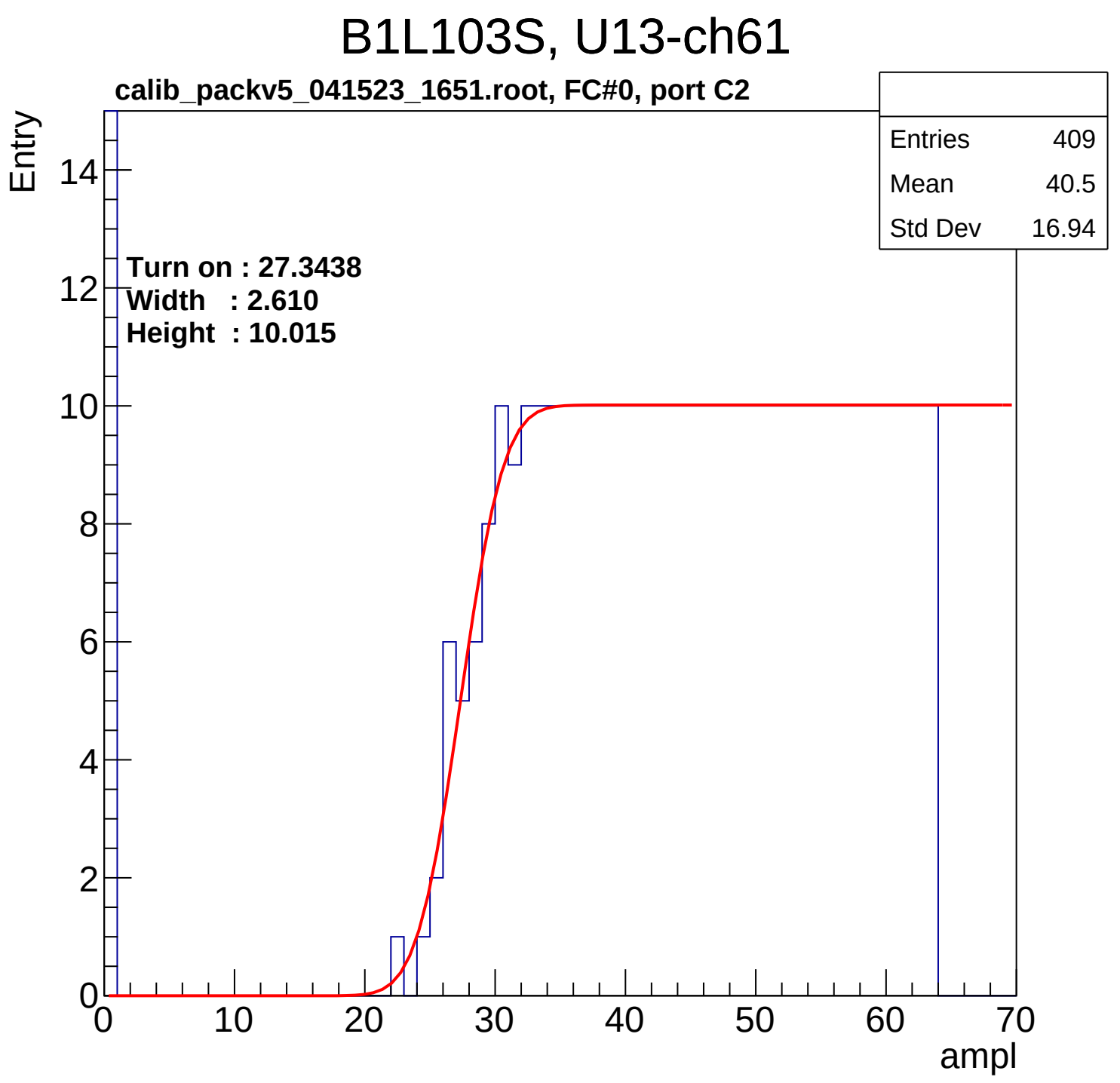
B1L103S, U13-ch61
calib_packv5_041523_1651.root, FC#0, port C2
Entries 409
Mean 40.5
Std Dev 16.94
Turn on : 27.3438
Width : 2.610
Height : 10.015
Entry
ampl
0
2
4
6
8
10
12
14
0
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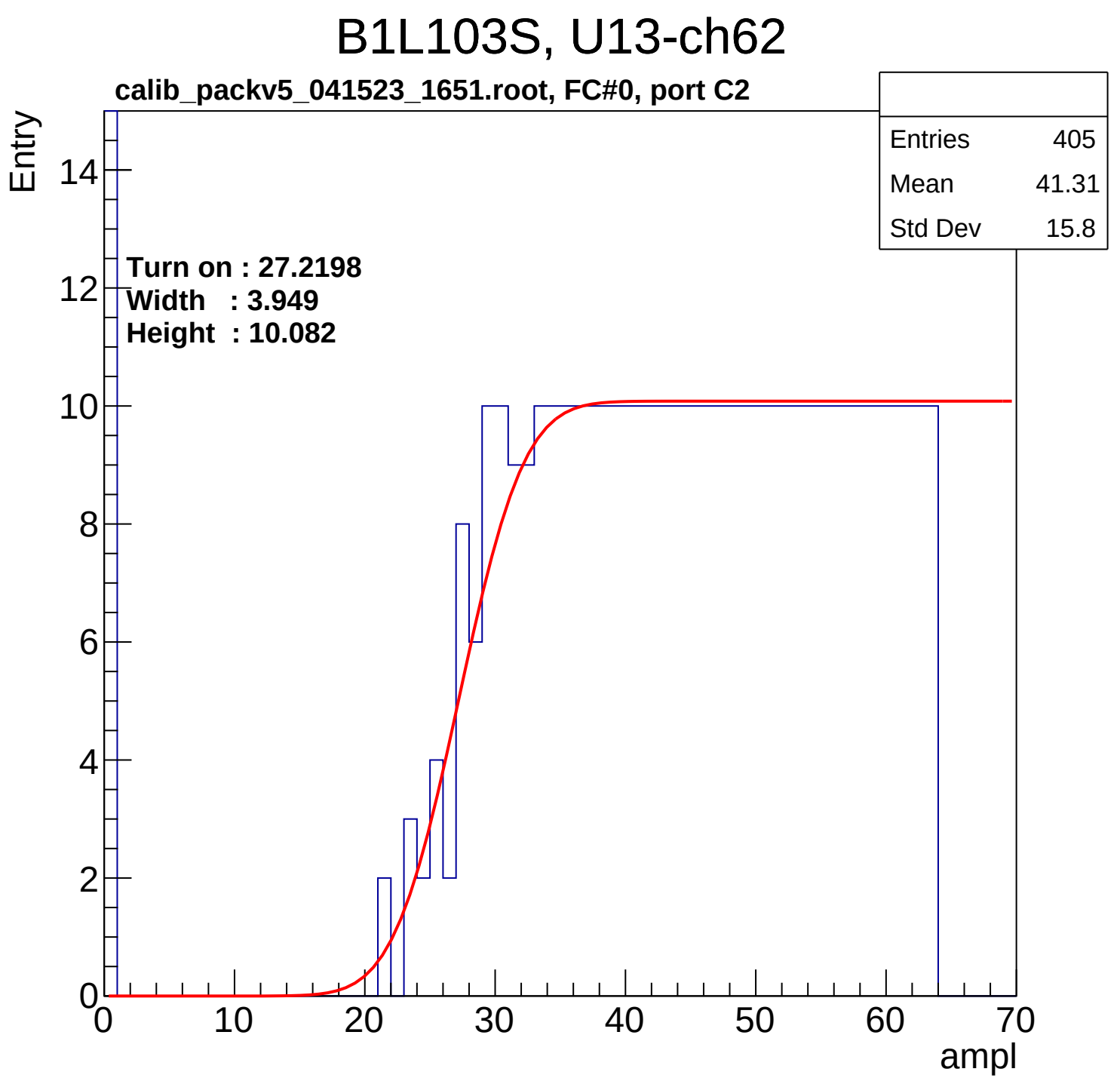
B1L103S, U13-ch62
calib_packv5_041523_1651.root, FC#0, port C2
Entries 405
Mean 41.31
Std Dev 15.8
Turn on : 27.2198
Width : 3.949
Height : 10.082
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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60
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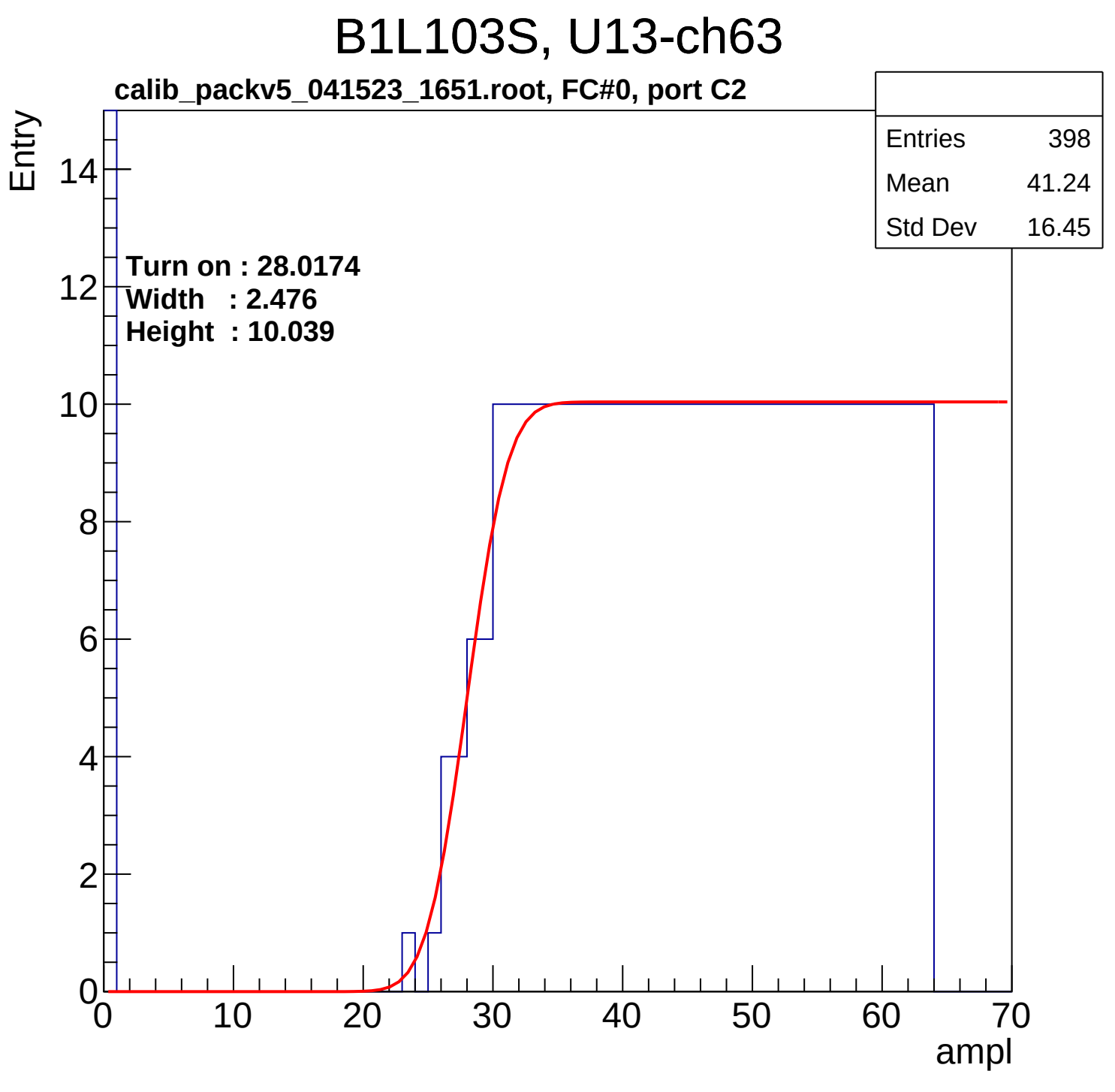
B1L103S, U13-ch63
calib_packv5_041523_1651.root, FC#0, port C2
Entries 398
Mean 41.24
Std Dev 16.45
Turn on : 28.0174
Width : 2.476
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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60
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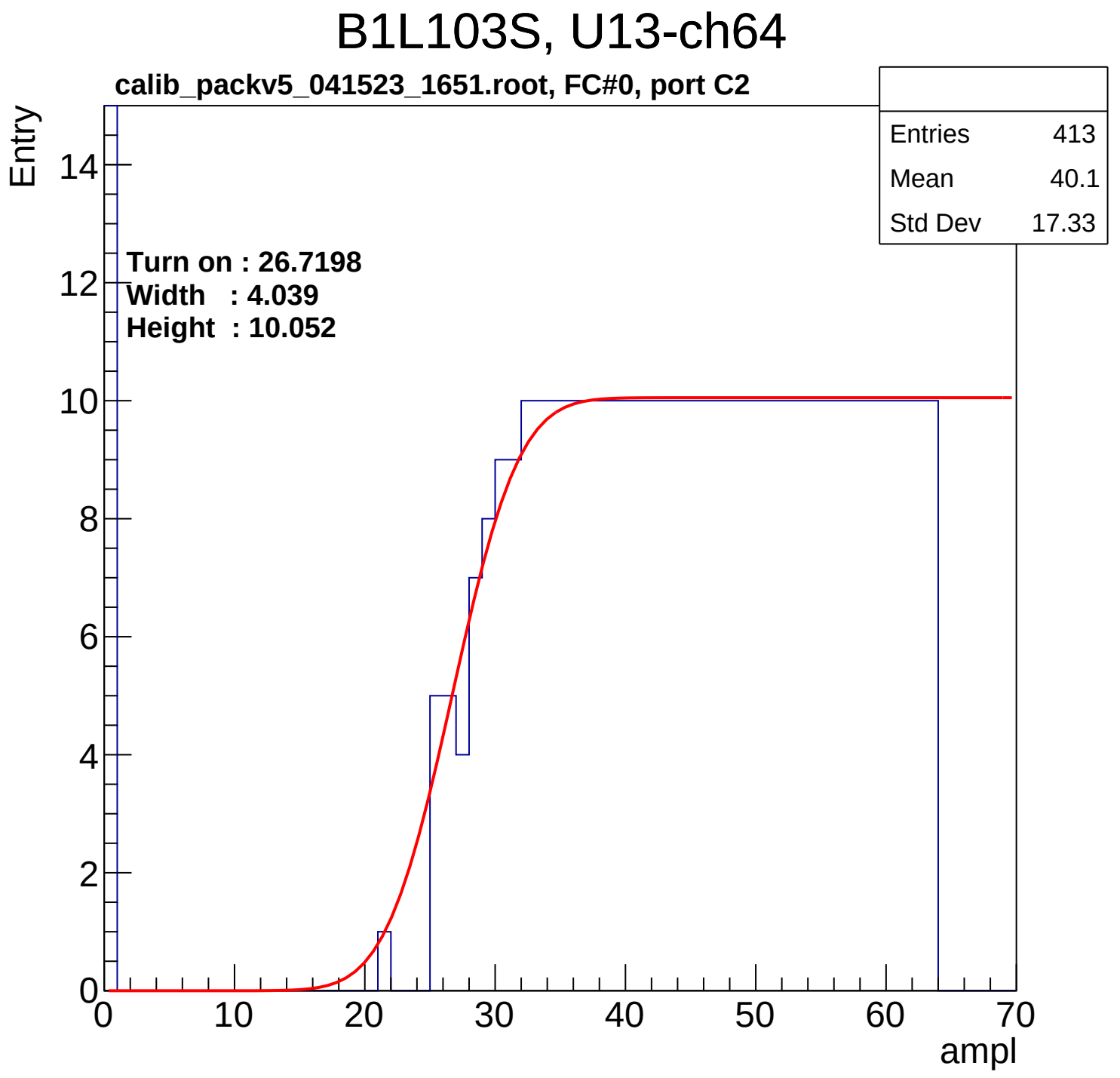
B1L103S, U13-ch64
calib_packv5_041523_1651.root, FC#0, port C2
Entries 413
Mean 40.1
Std Dev 17.33
Turn on : 26.7198
Width : 4.039
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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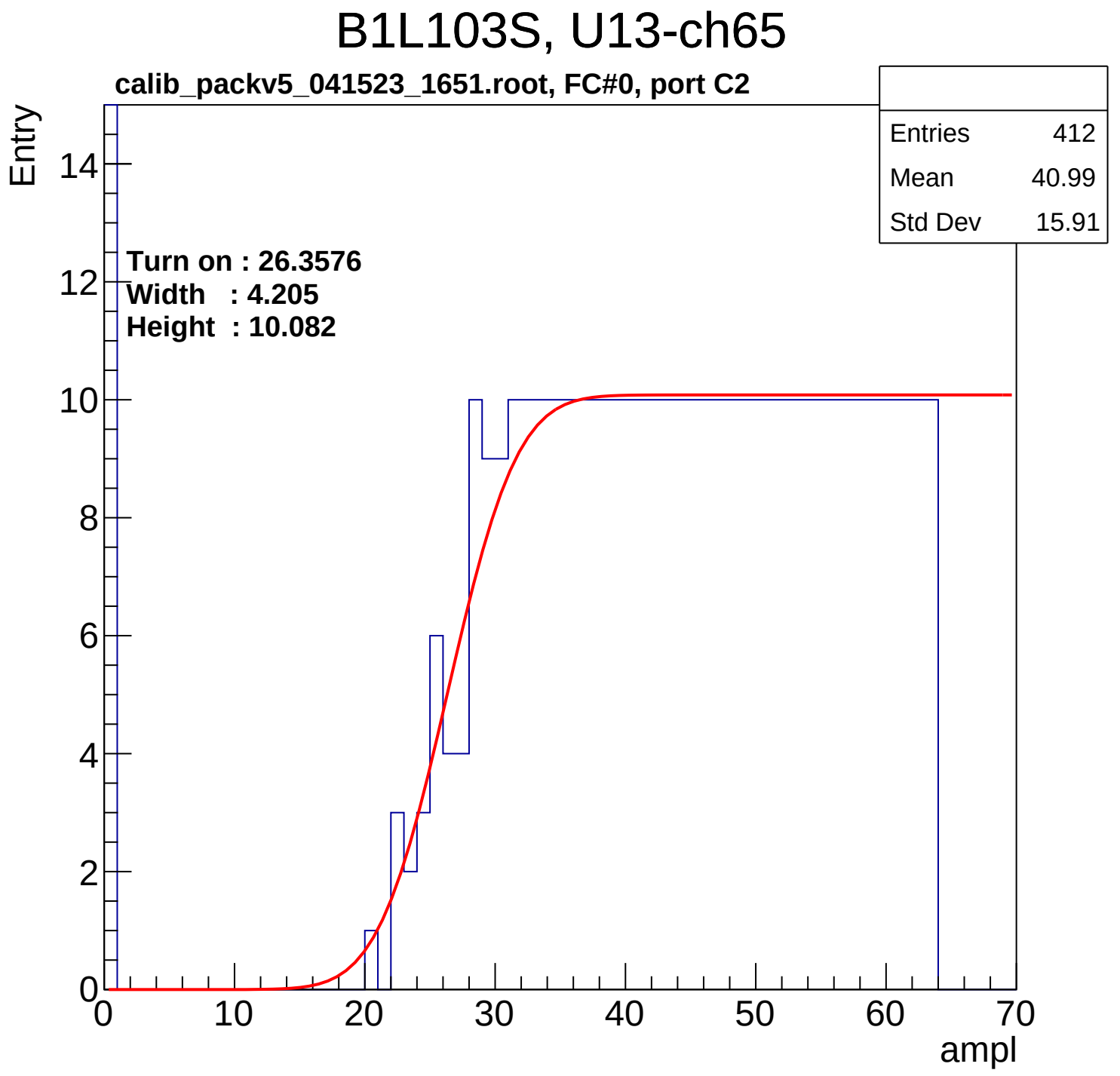
B1L103S, U13-ch65
calib_packv5_041523_1651.root, FC#0, port C2
Entries 412
Mean 40.99
Std Dev 15.91
Turn on : 26.3576
Width : 4.205
Height : 10.082
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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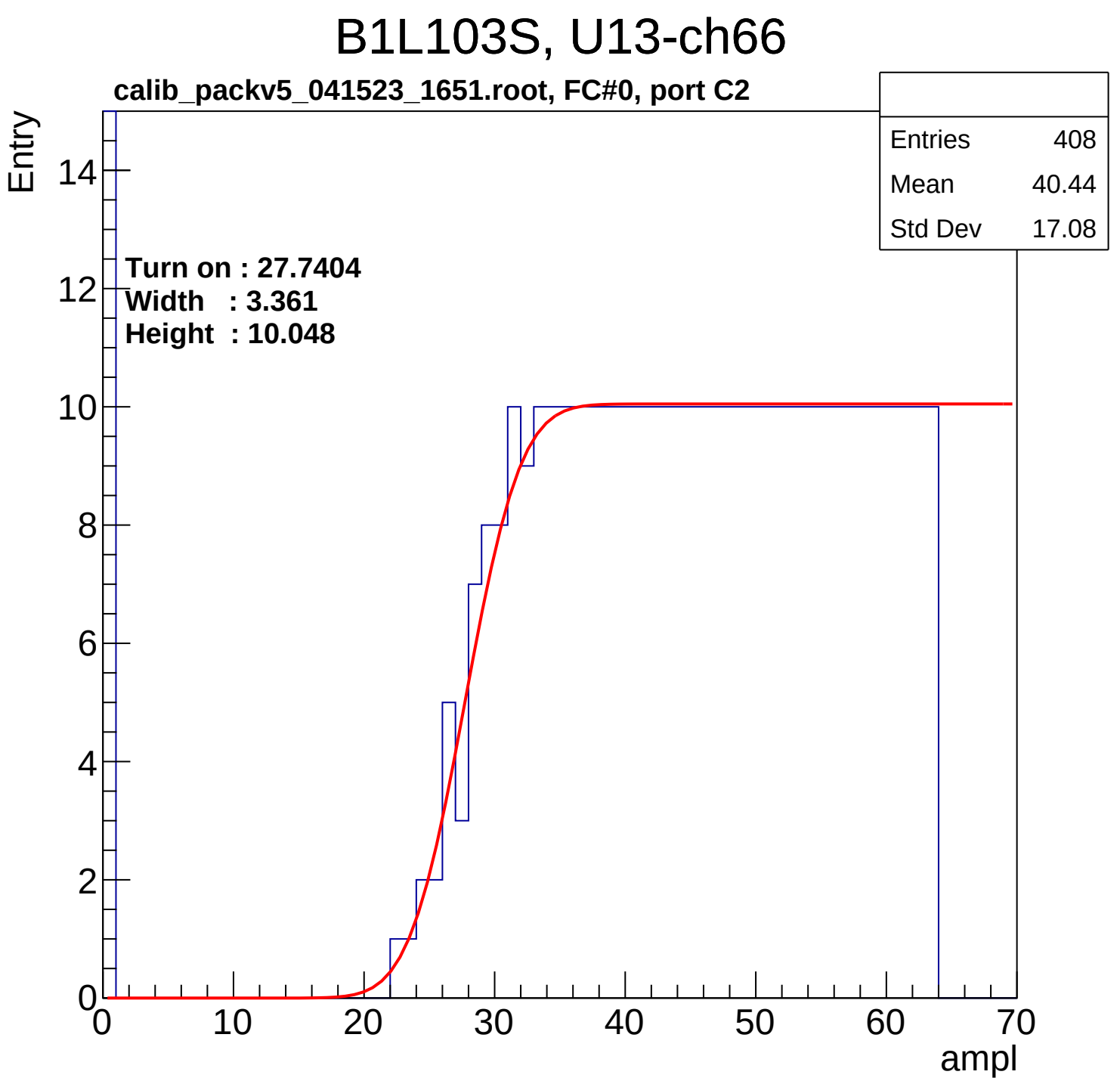
B1L103S, U13-ch66
calib_packv5_041523_1651.root, FC#0, port C2
Entries 408
Mean 40.44
Std Dev 17.08
Turn on : 27.7404
Width : 3.361
Height : 10.048
Entry
ampl
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2
4
6
8
10
12
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0
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20
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60
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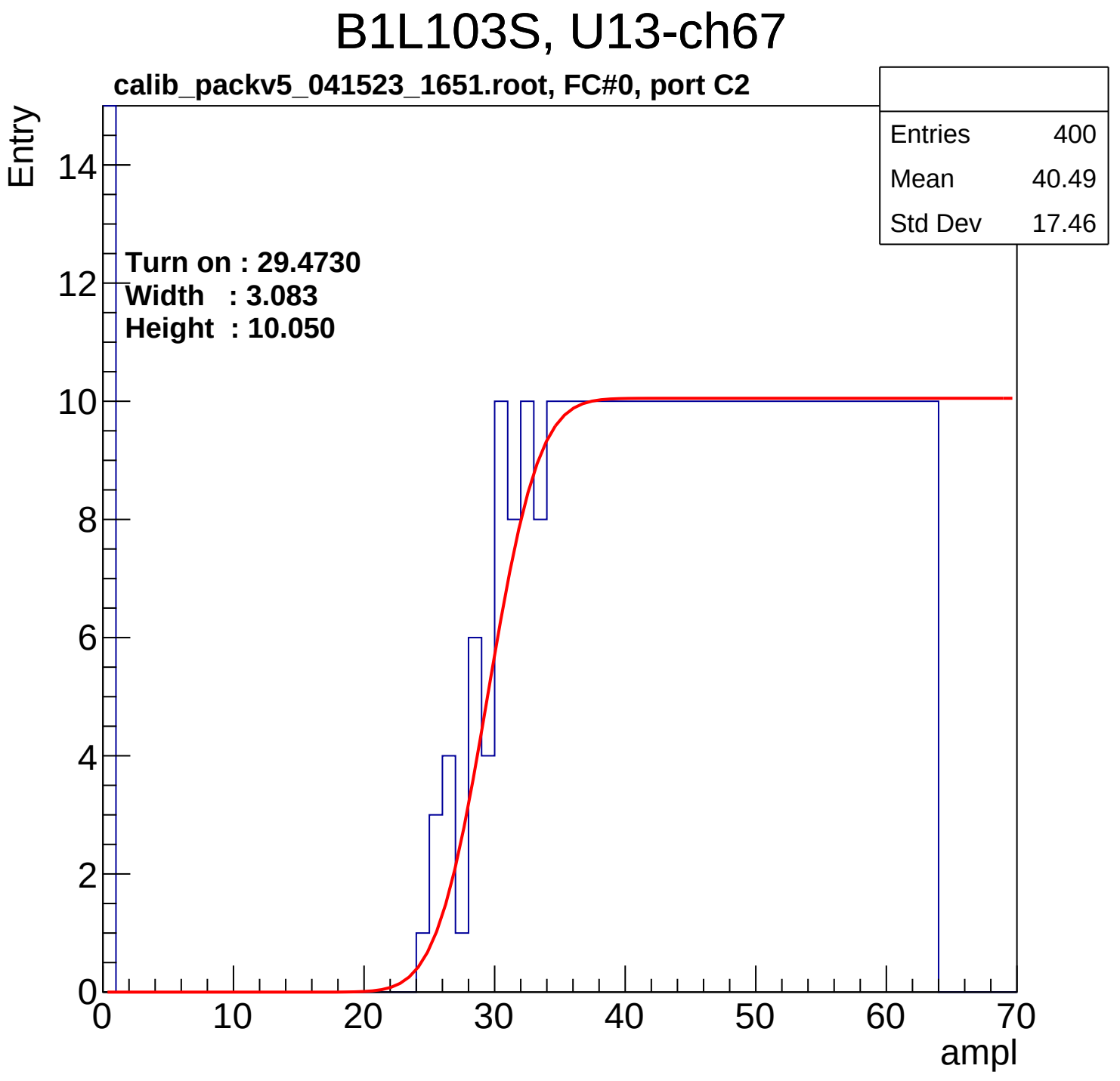
B1L103S, U13-ch67
calib_packv5_041523_1651.root, FC#0, port C2
Entries 400
Mean 40.49
Std Dev 17.46
Turn on : 29.4730
Width : 3.083
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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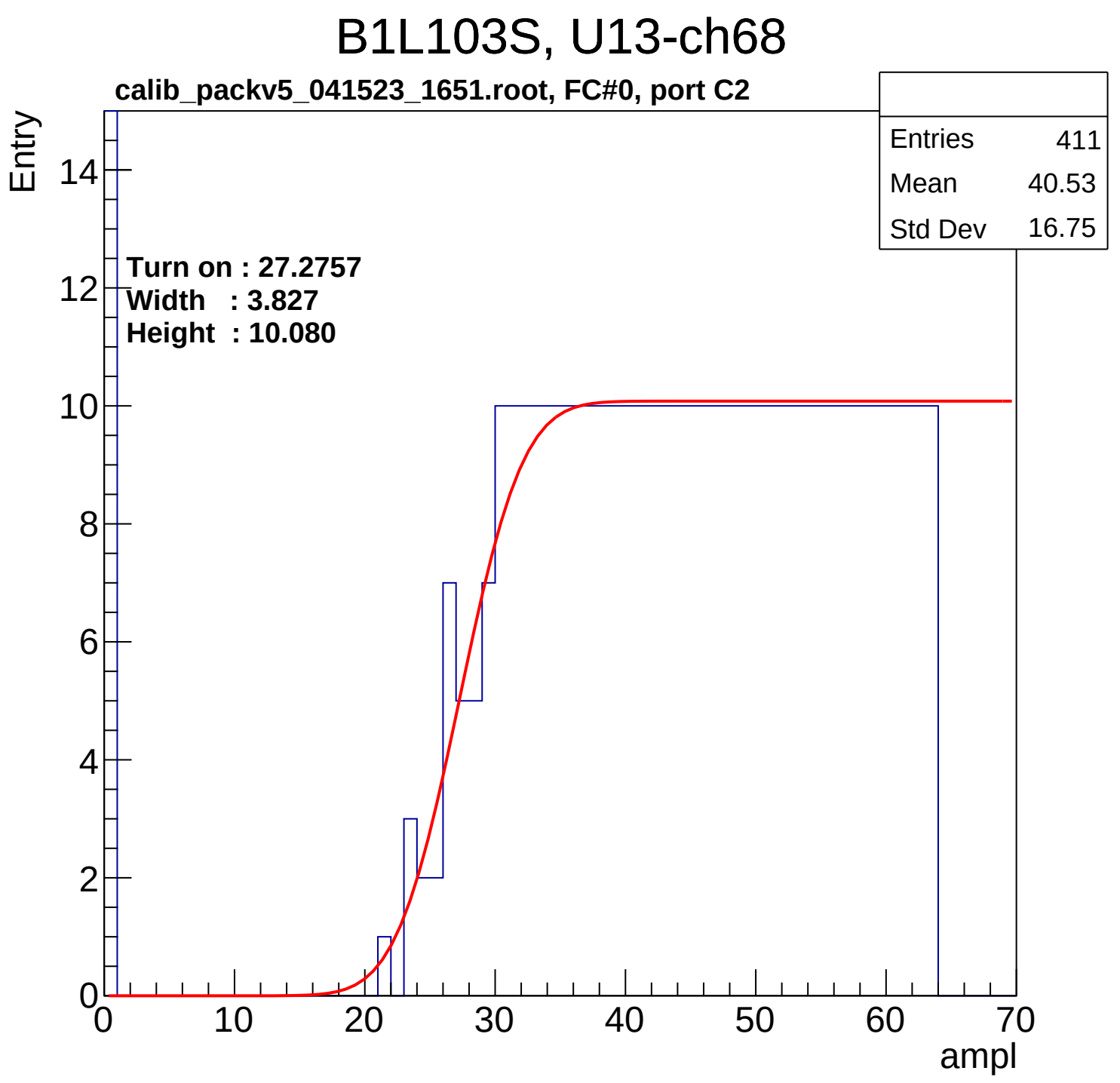
B1L103S, U13-ch68
calib_packv5_041523_1651.root, FC#0, port C2
Entries 411
Mean 40.53
Std Dev 16.75
Turn on : 27.2757
Width : 3.827
Height : 10.080
Entry
ampl
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4
6
8
10
12
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0
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40
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60
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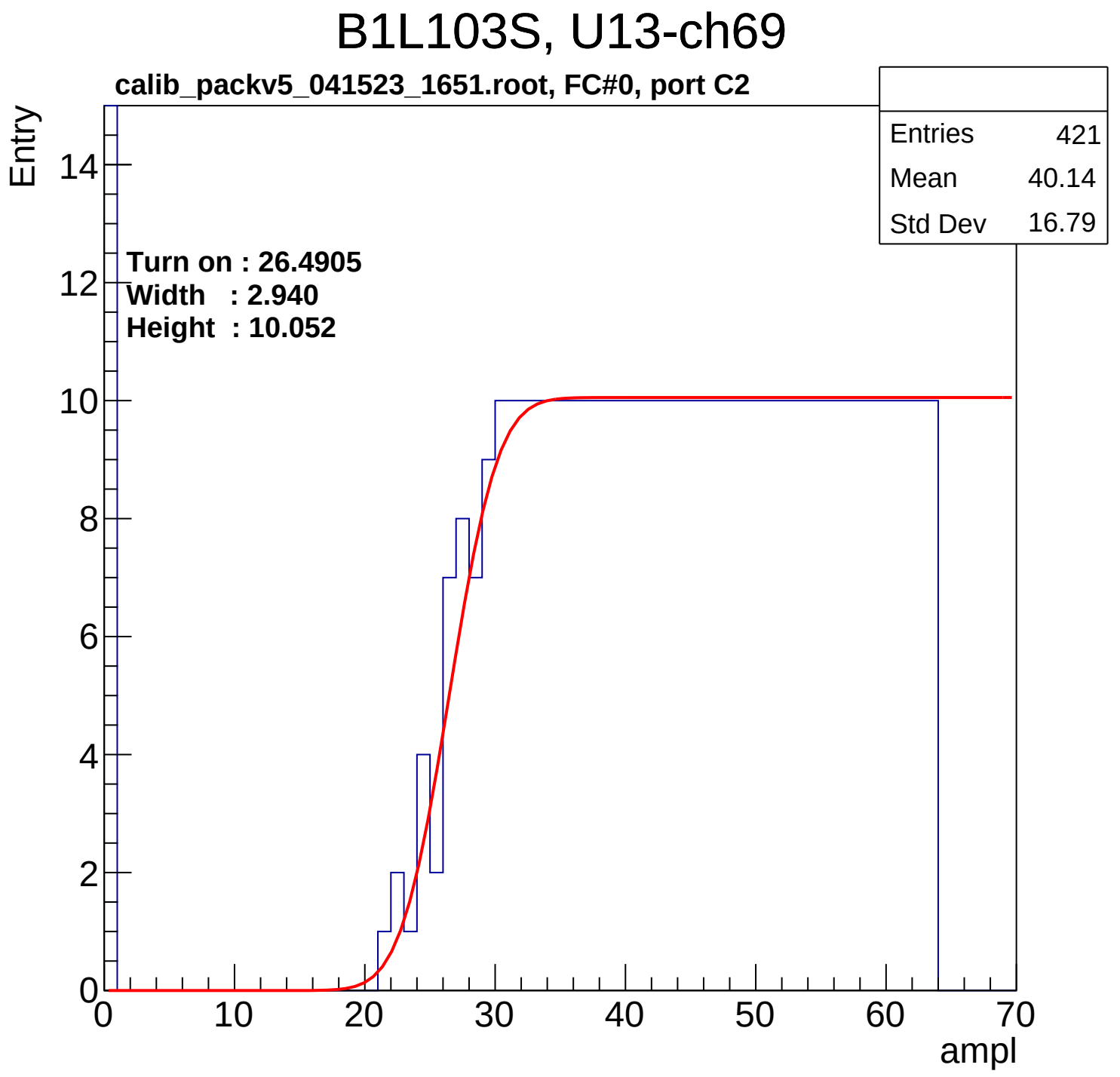
B1L103S, U13-ch69
calib_packv5_041523_1651.root, FC#0, port C2
Entries 421
Mean 40.14
Std Dev 16.79
Turn on : 26.4905
Width : 2.940
Height : 10.052
Entry
ampl
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2
4
6
8
10
12
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0
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20
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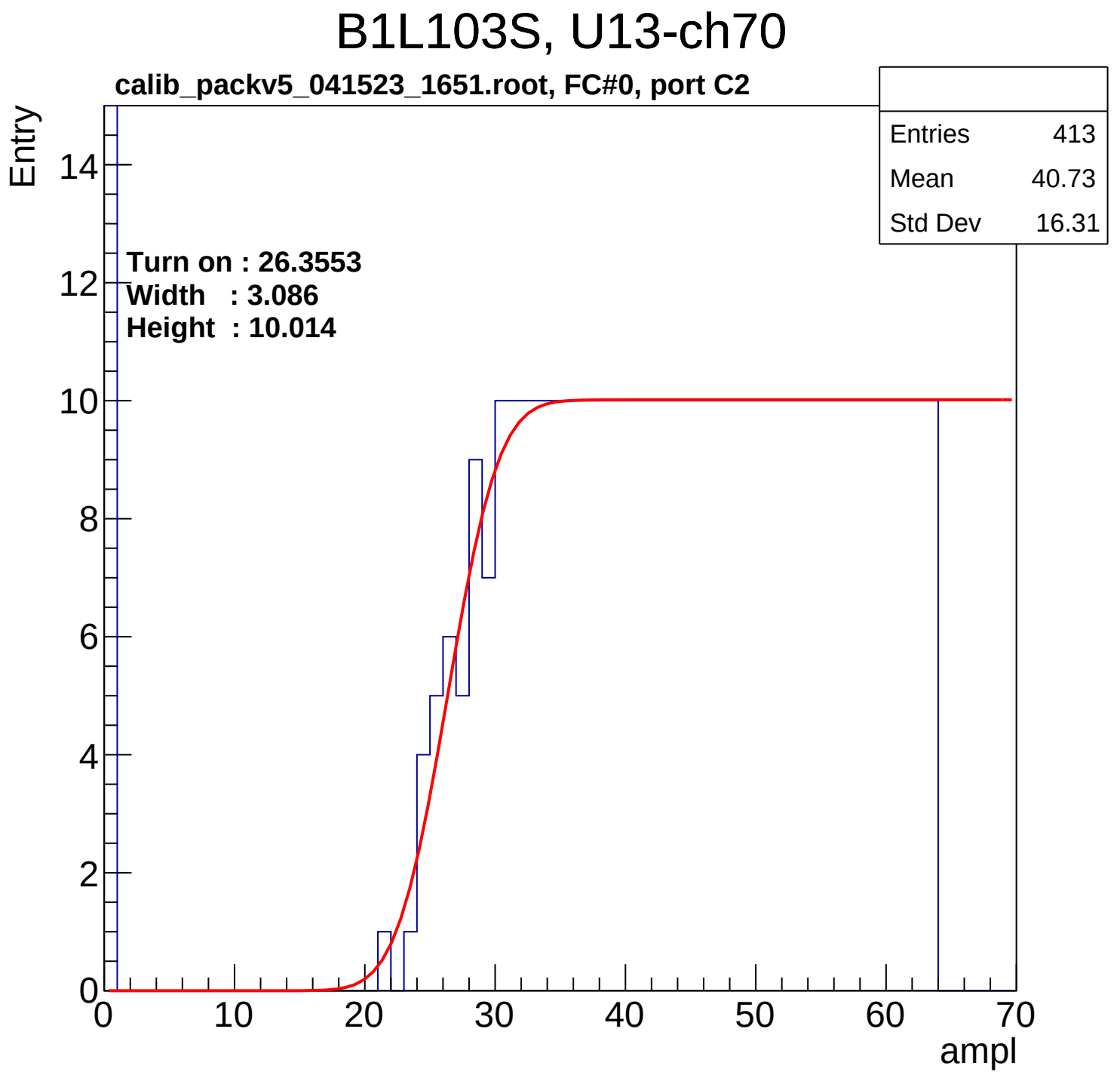
B1L103S, U13-ch70
calib_packv5_041523_1651.root, FC#0, port C2
Entries 413
Mean 40.73
Std Dev 16.31
Turn on : 26.3553
Width : 3.086
Height : 10.014
Entry
ampl
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6
8
10
12
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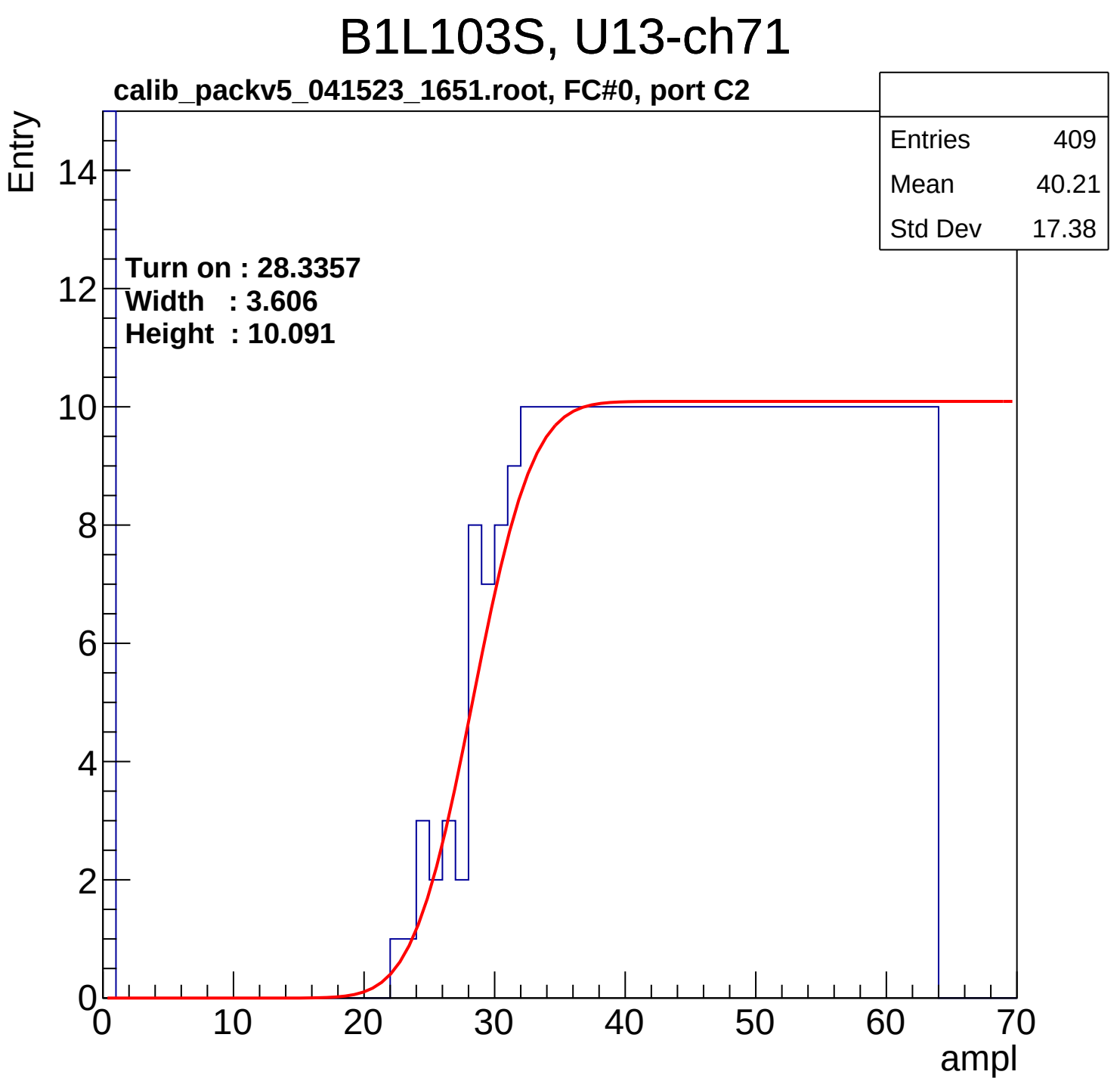
B1L103S, U13-ch71
calib_packv5_041523_1651.root, FC#0, port C2
Entries 409
Mean 40.21
Std Dev 17.38
Turn on : 28.3357
Width : 3.606
Height : 10.091
Entry
ampl
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4
6
8
10
12
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20
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60
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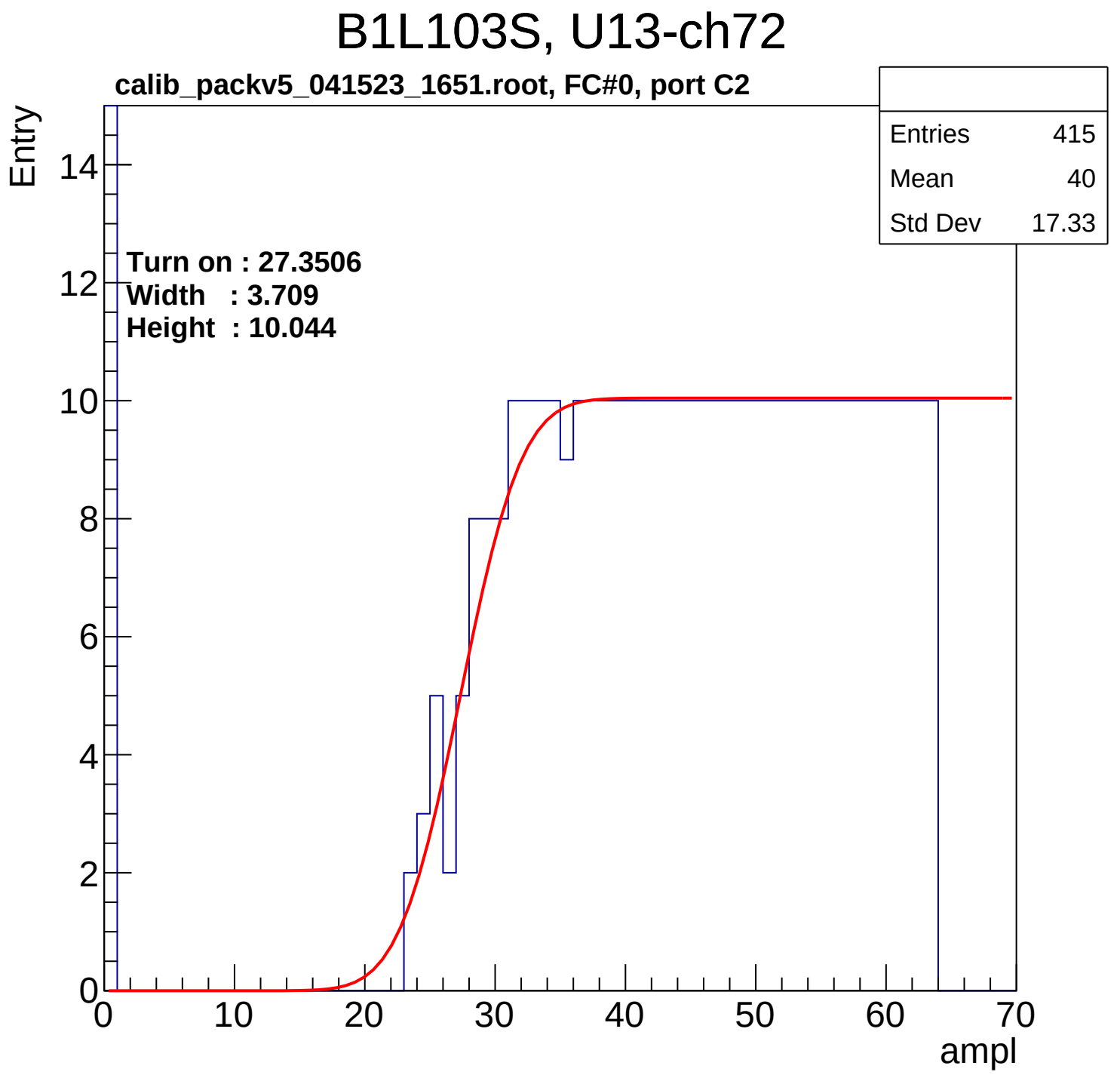
B1L103S, U13-ch72
calib_packv5_041523_1651.root, FC#0, port C2
Entries 415
Mean 40
Std Dev 17.33
Turn on : 27.3506
Width : 3.709
Height : 10.044
Entry
ampl
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6
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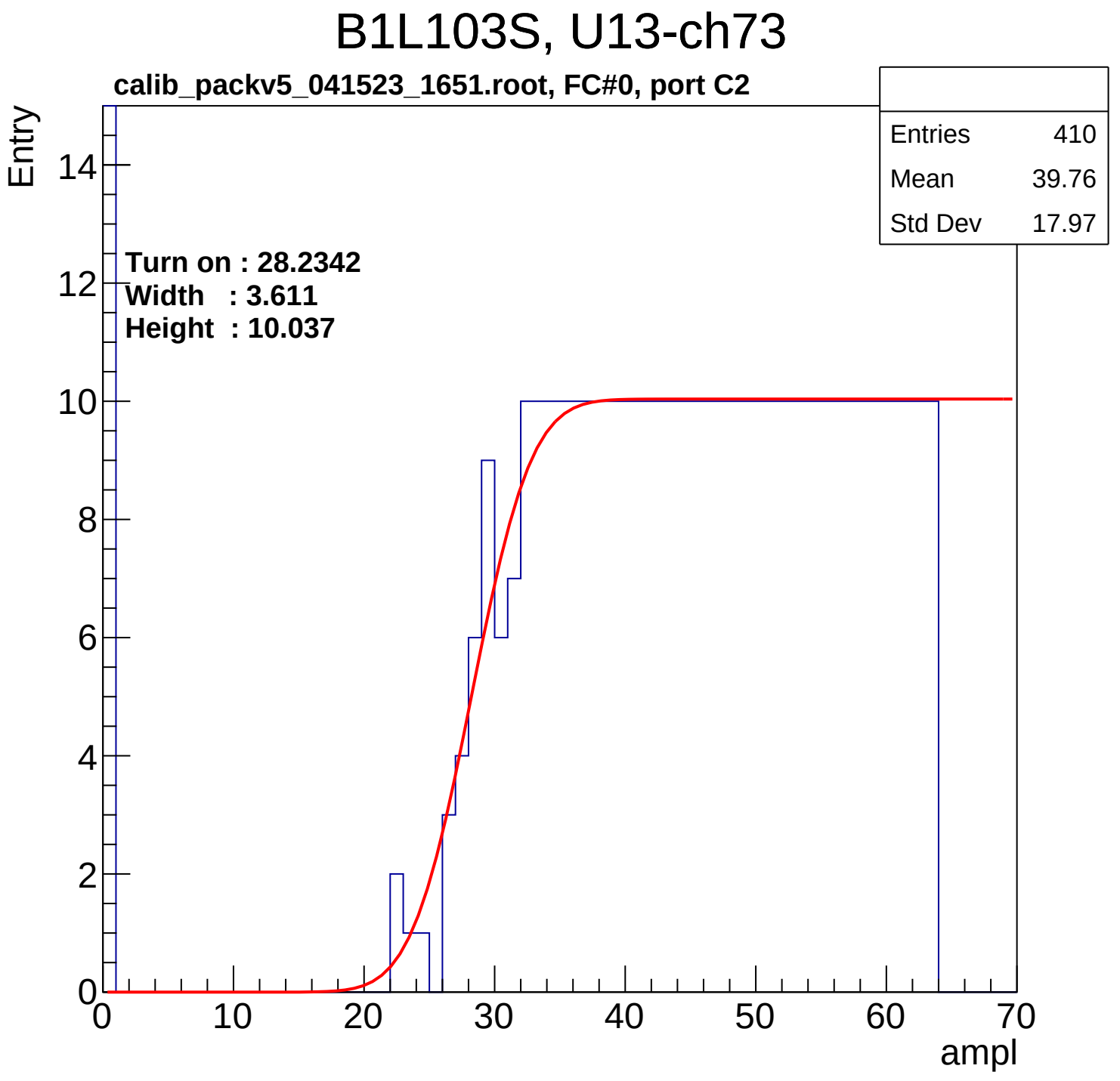
B1L103S, U13-ch73
calib_packv5_041523_1651.root, FC#0, port C2
Entries 410
Mean 39.76
Std Dev 17.97
Turn on : 28.2342
Width : 3.611
Height : 10.037
Entry
ampl
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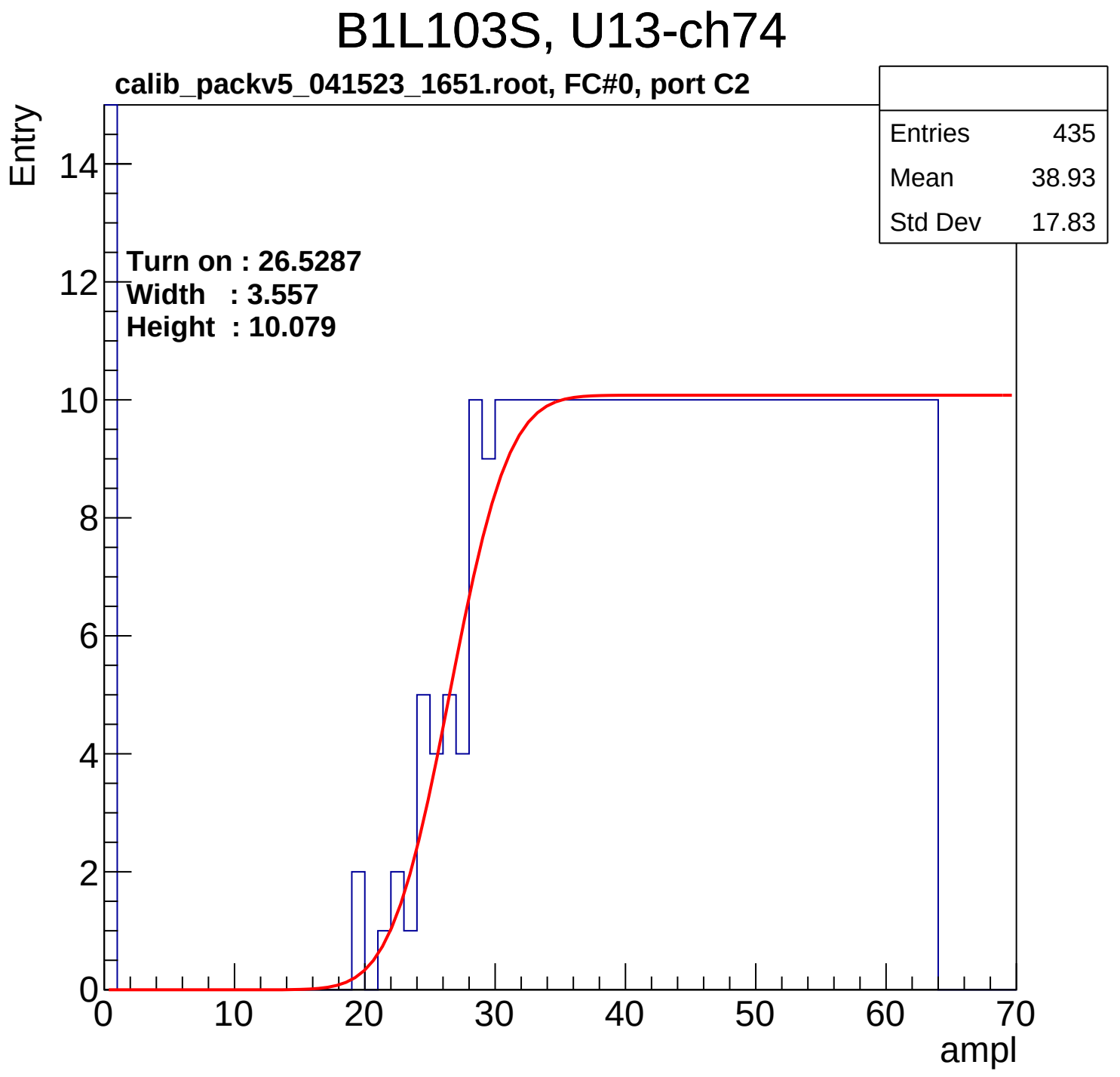
B1L103S, U13-ch74
calib_packv5_041523_1651.root, FC#0, port C2
Entries 435
Mean 38.93
Std Dev 17.83
Turn on : 26.5287
Width : 3.557
Height : 10.079
Entry
ampl
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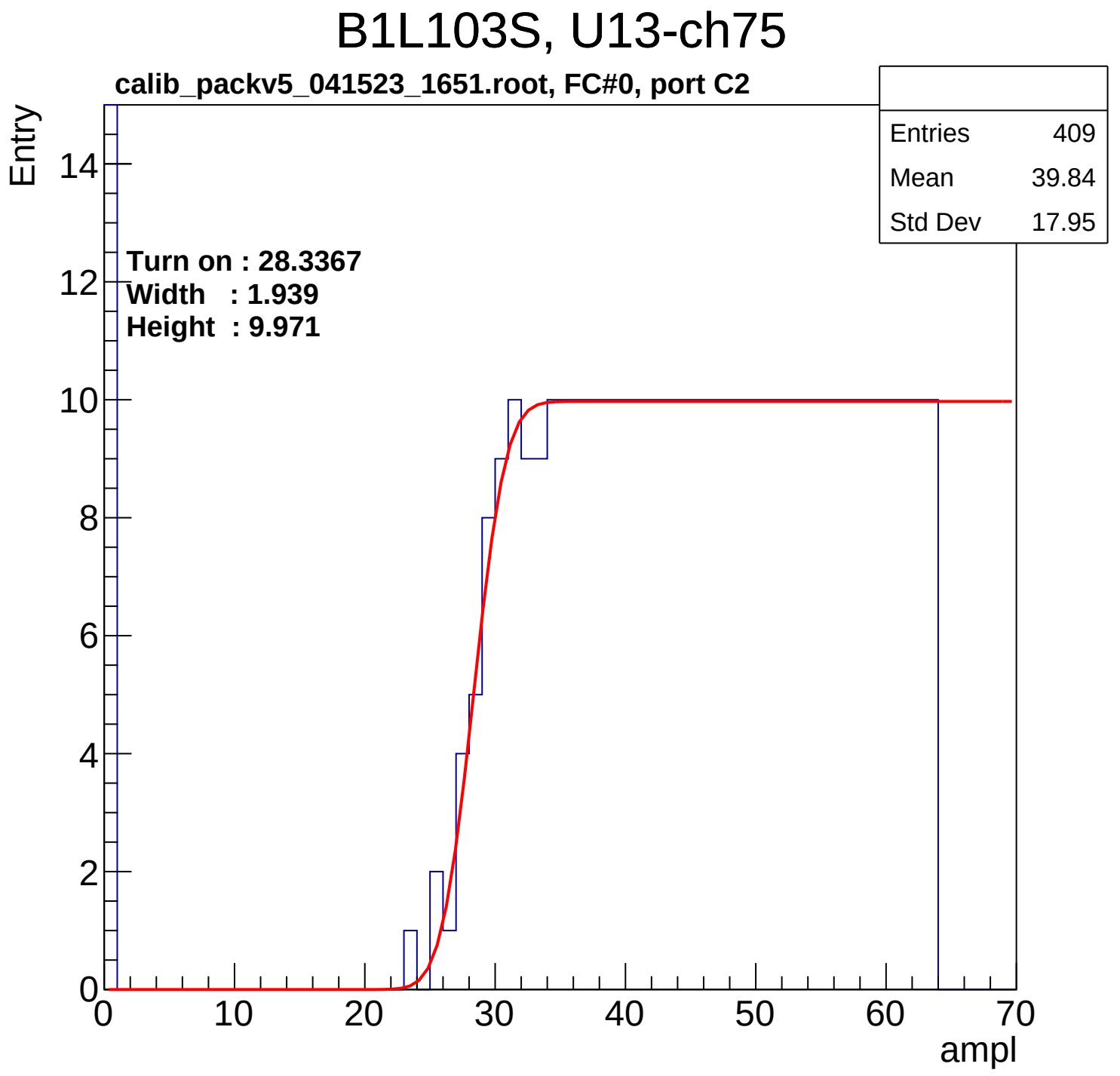
B1L103S, U13-ch75
calib_packv5_041523_1651.root, FC#0, port C2
Entries 409
Mean 39.84
Std Dev 17.95
Turn on : 28.3367
Width : 1.939
Height : 9.971
Entry
ampl
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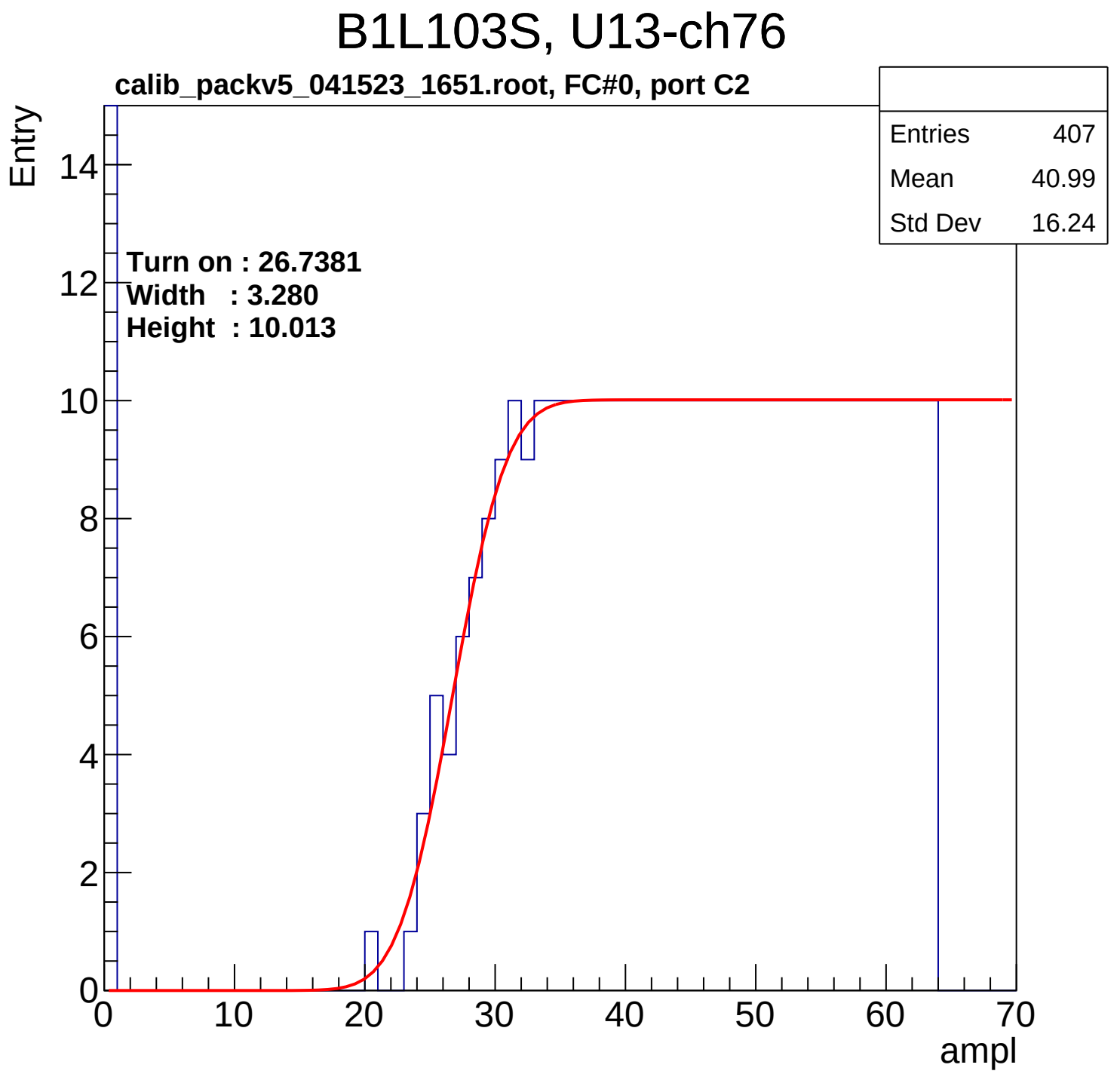
B1L103S, U13-ch76
calib_packv5_041523_1651.root, FC#0, port C2
Entries 407
Mean 40.99
Std Dev 16.24
Turn on : 26.7381
Width : 3.280
Height : 10.013
Entry
ampl
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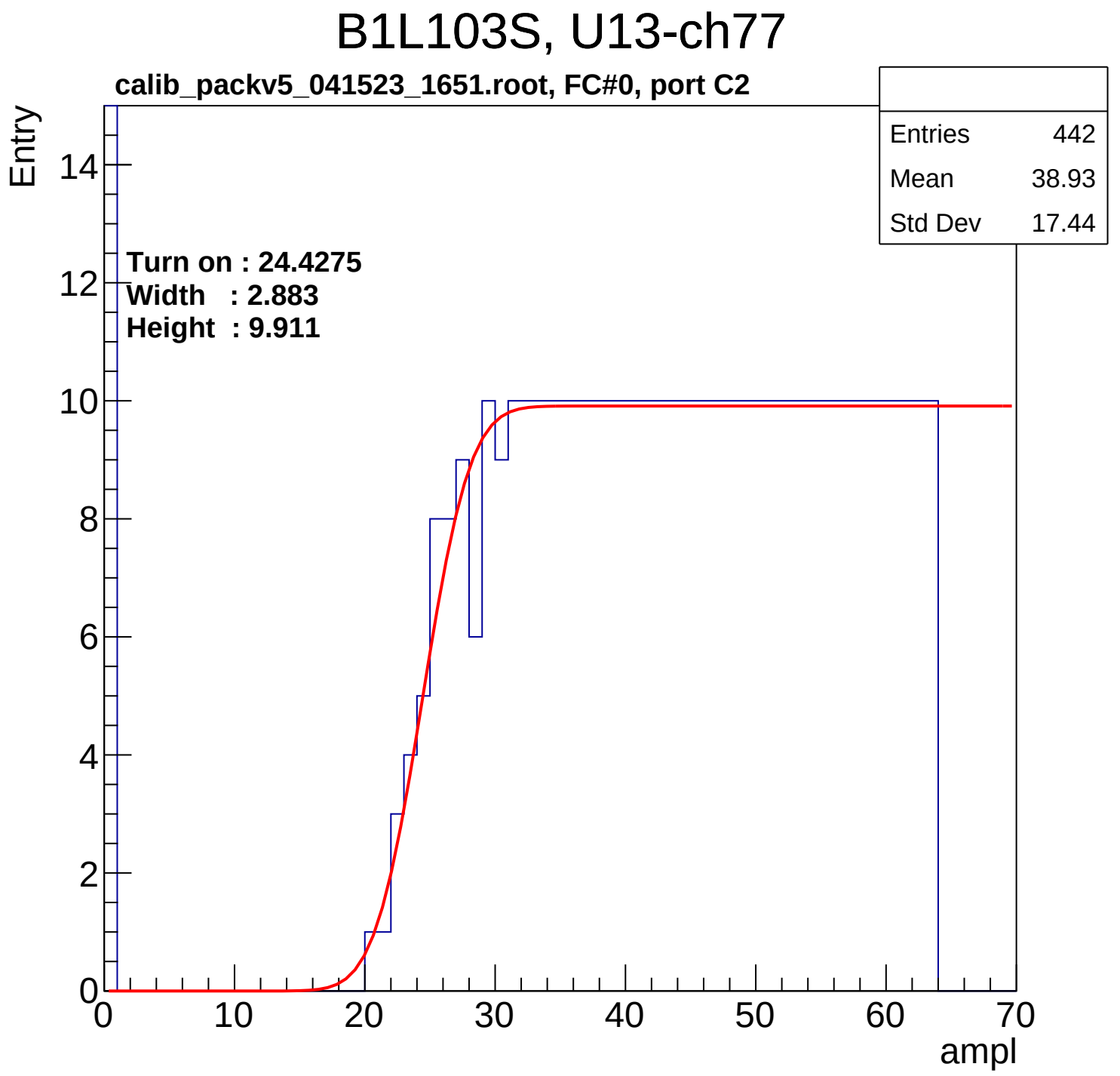
B1L103S, U13-ch77
calib_packv5_041523_1651.root, FC#0, port C2
Entries 442
Mean 38.93
Std Dev 17.44
Turn on : 24.4275
Width : 2.883
Height : 9.911
Entry
ampl
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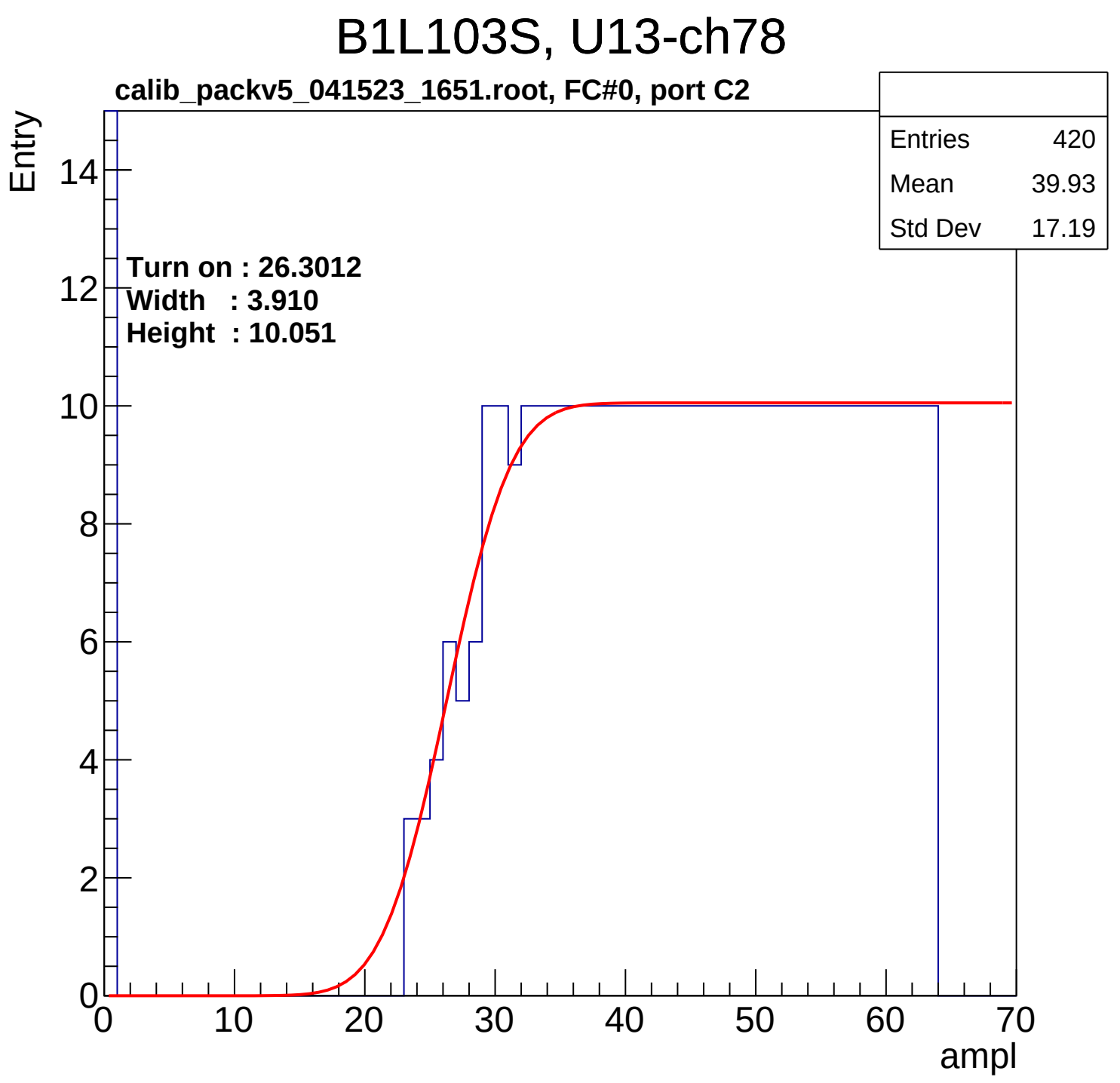
B1L103S, U13-ch78
calib_packv5_041523_1651.root, FC#0, port C2
Entries 420
Mean 39.93
Std Dev 17.19
Turn on : 26.3012
Width : 3.910
Height : 10.051
Entry
ampl
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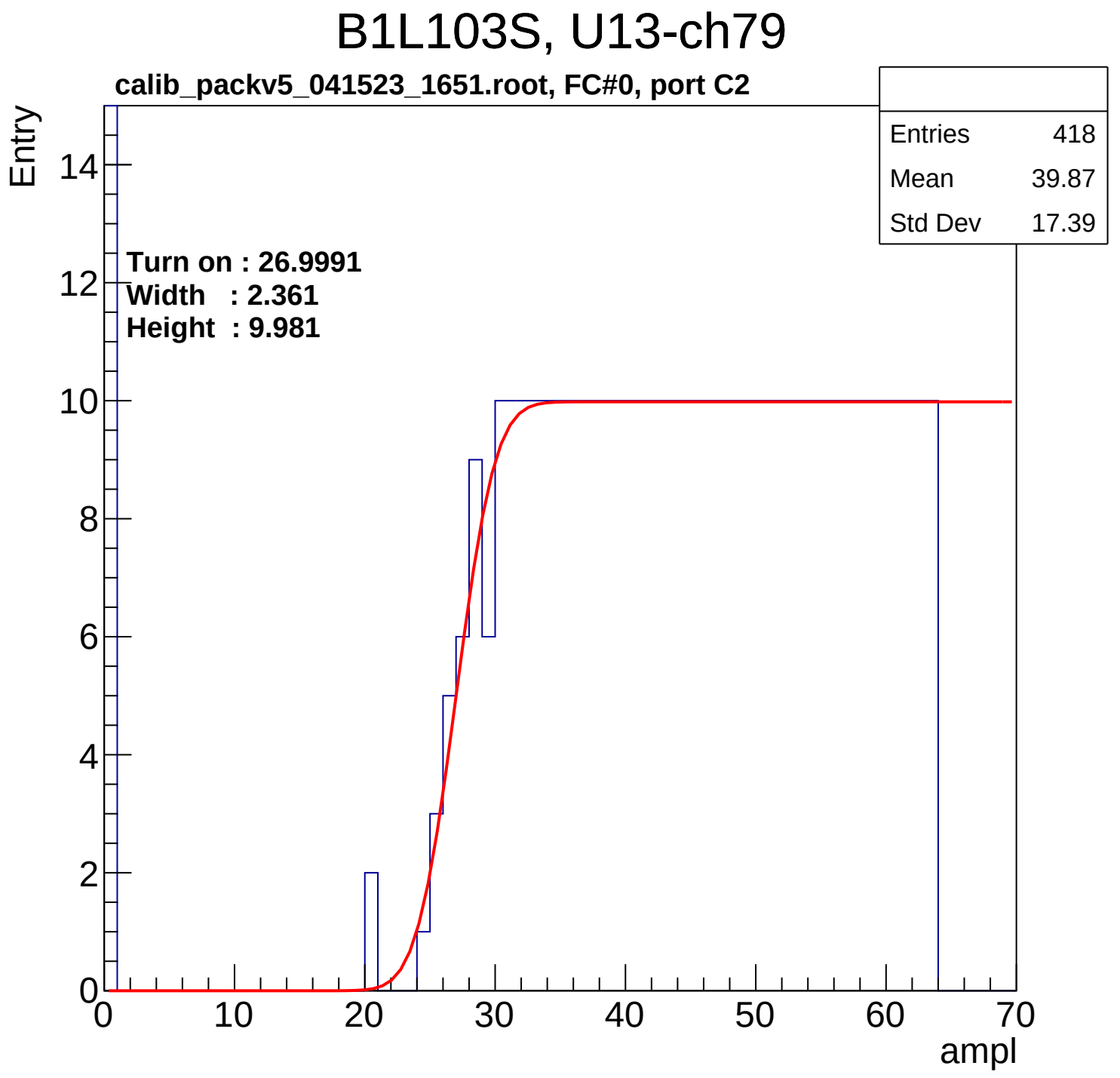
B1L103S, U13-ch79
calib_packv5_041523_1651.root, FC#0, port C2
Entries 418
Mean 39.87
Std Dev 17.39
Turn on : 26.9991
Width : 2.361
Height : 9.981
Entry
ampl
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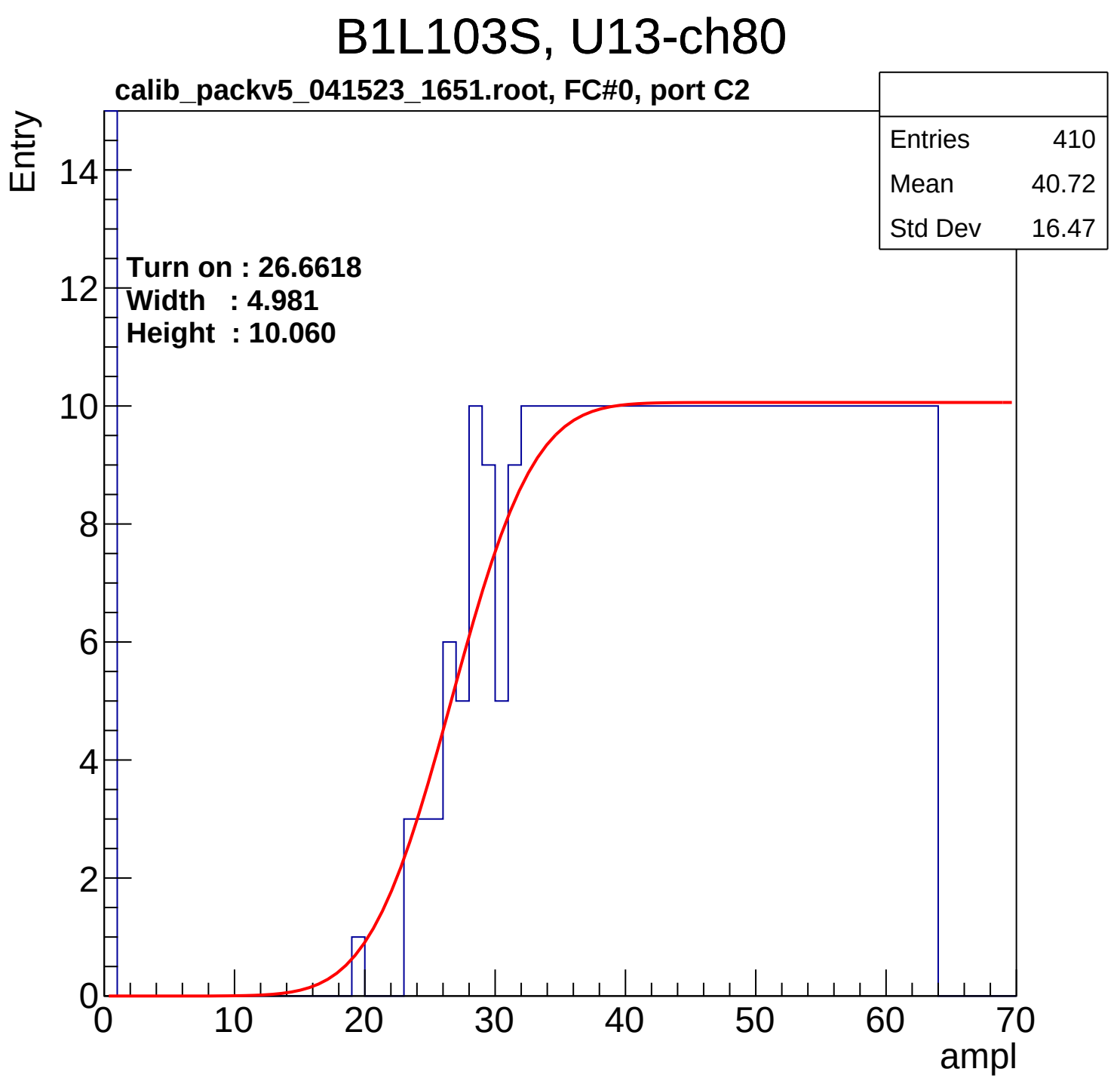
B1L103S, U13-ch80
calib_packv5_041523_1651.root, FC#0, port C2
Entries 410
Mean 40.72
Std Dev 16.47
Turn on : 26.6618
Width : 4.981
Height : 10.060
Entry
ampl
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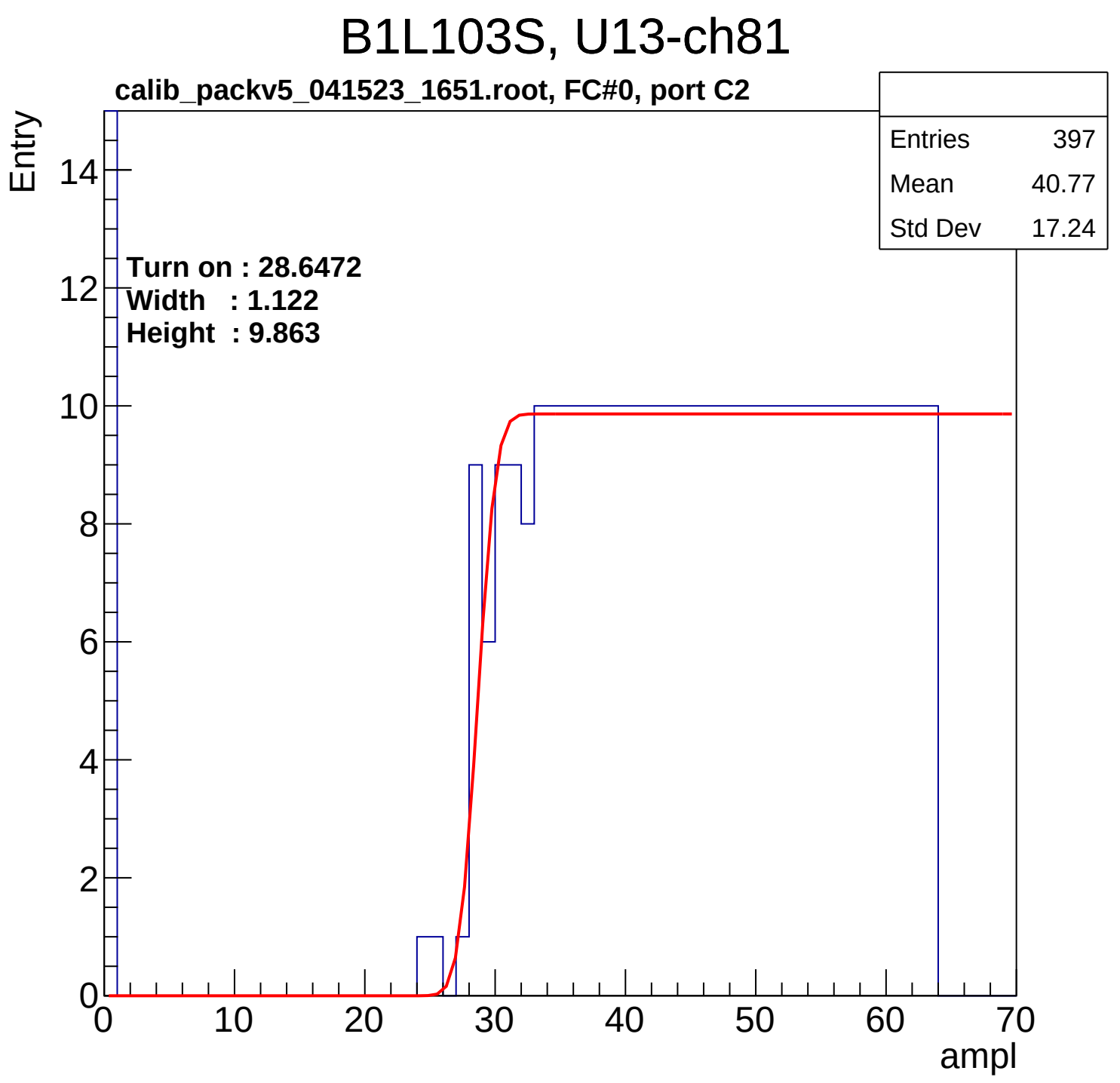
B1L103S, U13-ch81
calib_packv5_041523_1651.root, FC#0, port C2
Entries 397
Mean 40.77
Std Dev 17.24
Turn on : 28.6472
Width : 1.122
Height : 9.863
Entry
ampl
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6
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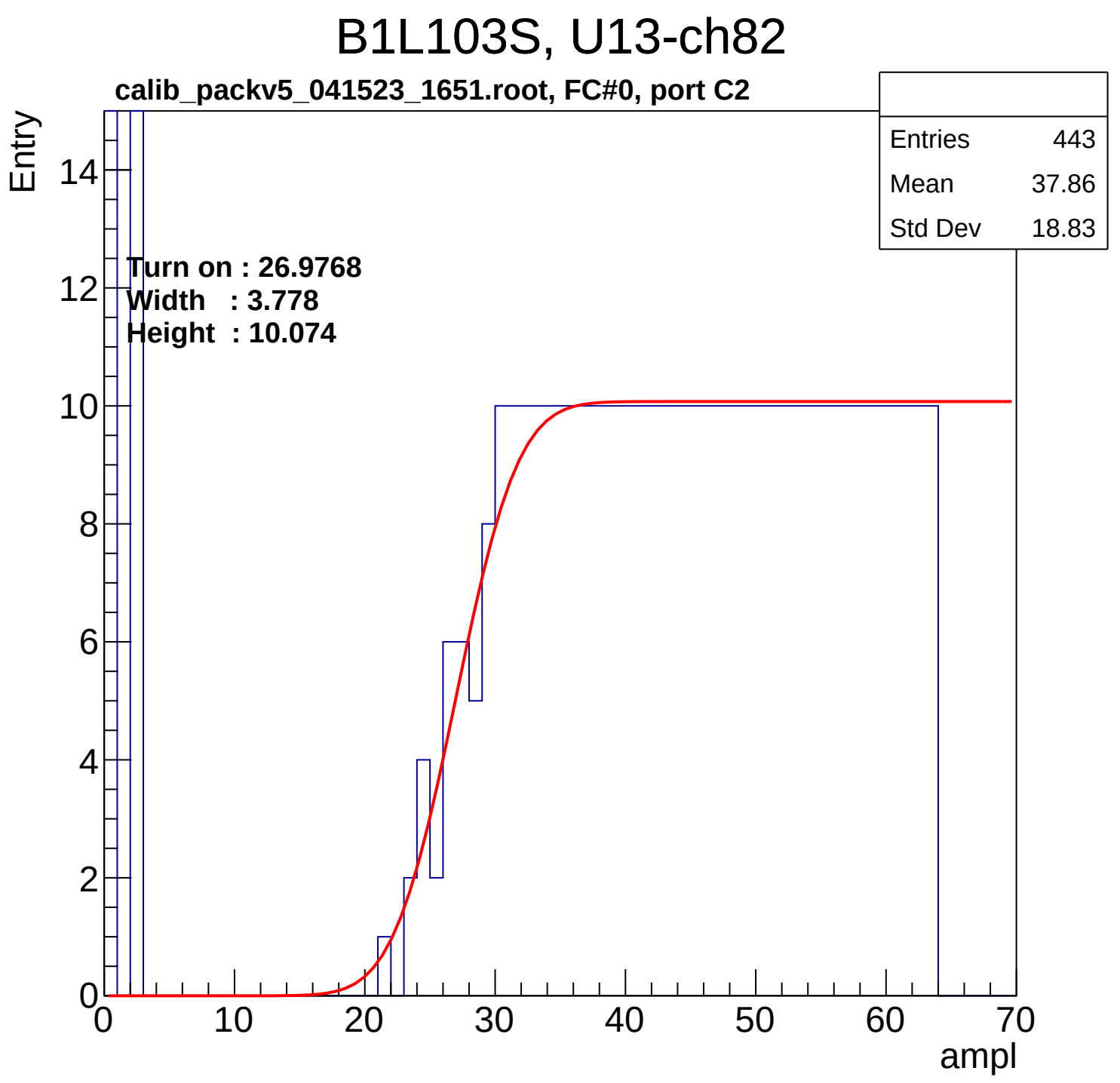
B1L103S, U13-ch82
calib_packv5_041523_1651.root, FC#0, port C2
Entries 443
Mean 37.86
Std Dev 18.83
Turn on : 26.9768
Width : 3.778
Height : 10.074
Entry
ampl
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6
8
10
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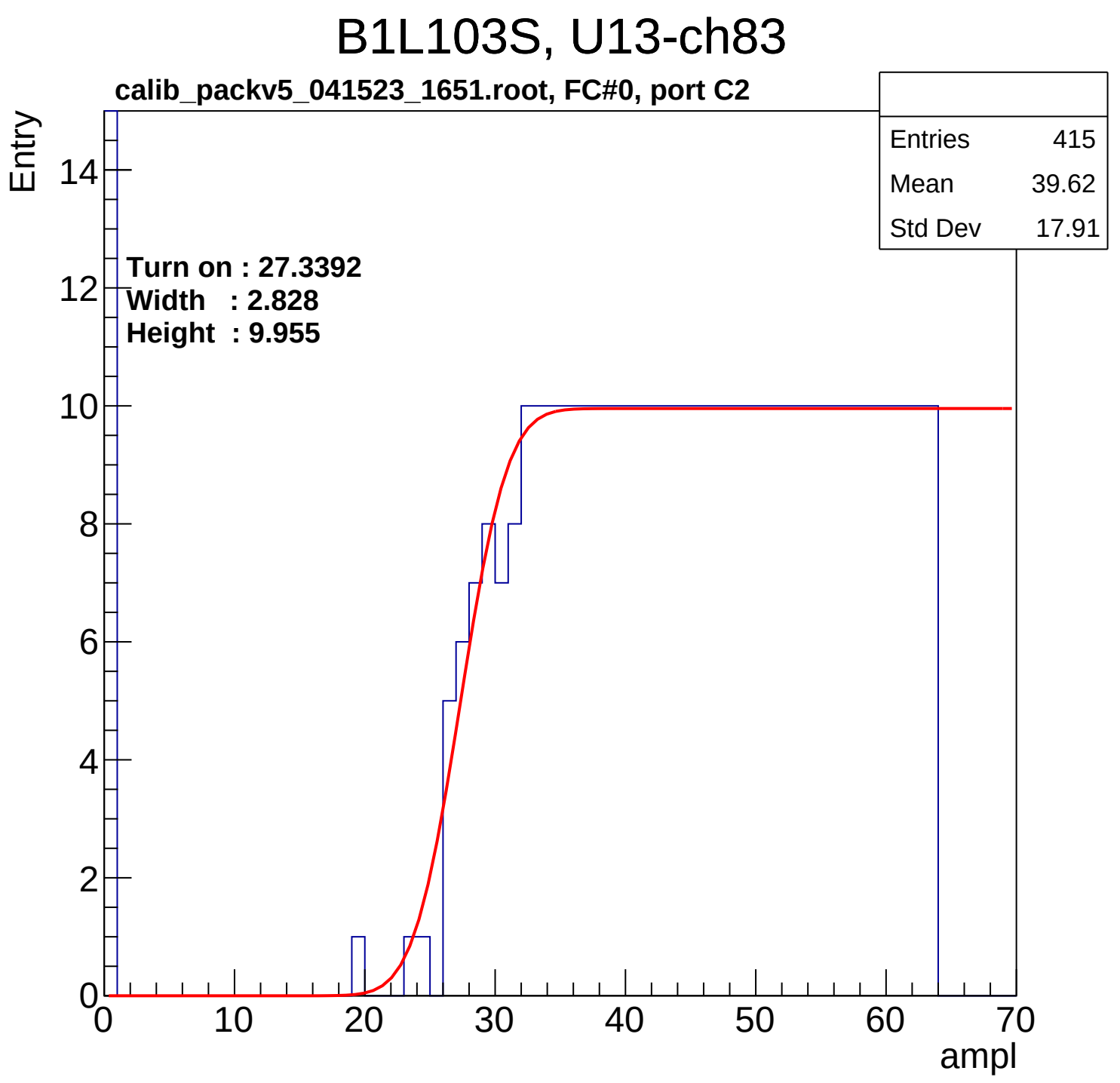
B1L103S, U13-ch83
calib_packv5_041523_1651.root, FC#0, port C2
Entries 415
Mean 39.62
Std Dev 17.91
Turn on : 27.3392
Width : 2.828
Height : 9.955
Entry
ampl
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6
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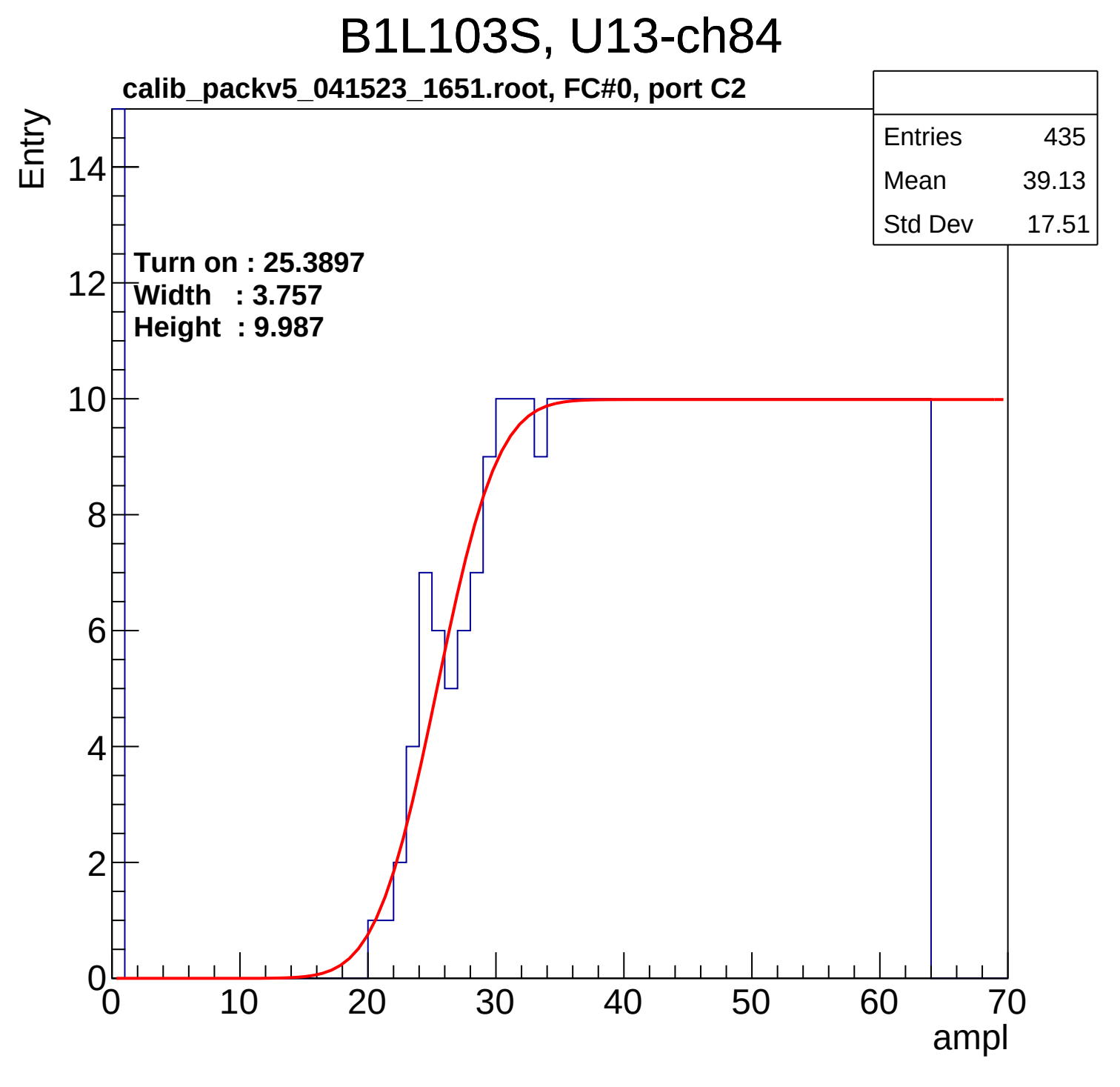
B1L103S, U13-ch84
calib_packv5_041523_1651.root, FC#0, port C2
Entries 435
Mean 39.13
Std Dev 17.51
Turn on : 25.3897
Width : 3.757
Height : 9.987
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ampl
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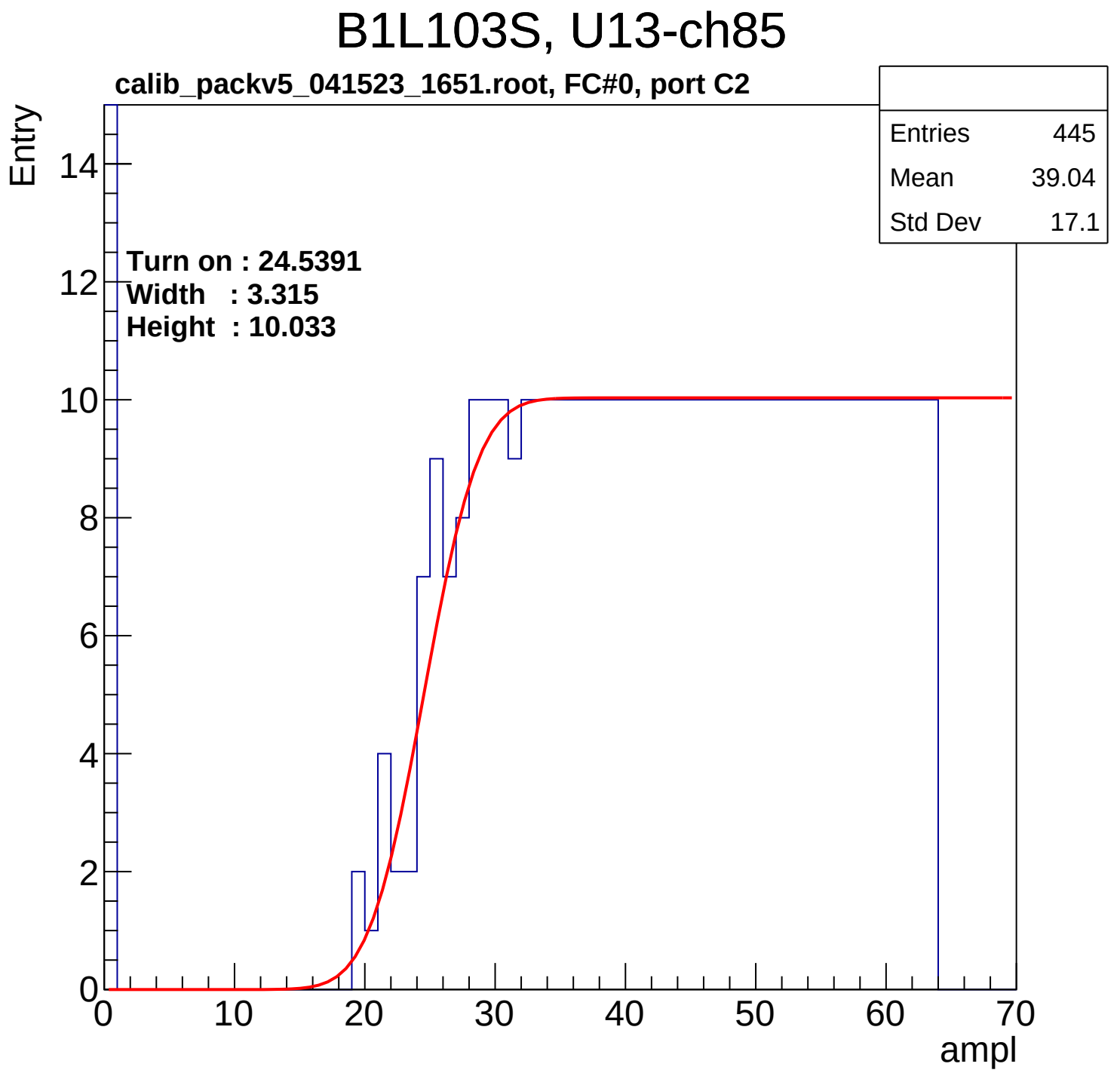
B1L103S, U13-ch85
calib_packv5_041523_1651.root, FC#0, port C2
Entries 445
Mean 39.04
Std Dev 17.1
Turn on : 24.5391
Width : 3.315
Height : 10.033
Entry
ampl
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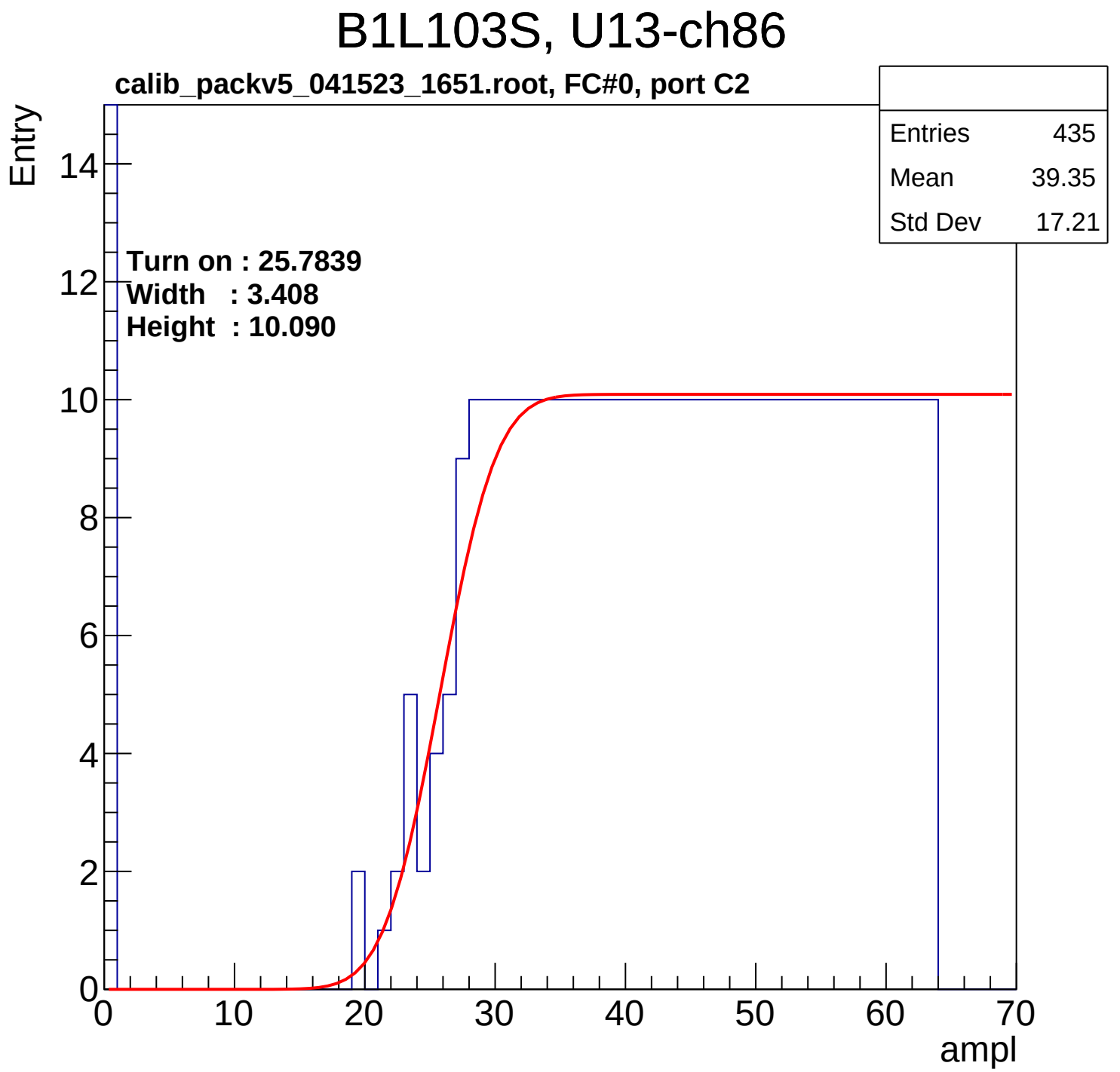
B1L103S, U13-ch86
calib_packv5_041523_1651.root, FC#0, port C2
Entries 435
Mean 39.35
Std Dev 17.21
Turn on : 25.7839
Width : 3.408
Height : 10.090
Entry
ampl
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4
6
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20
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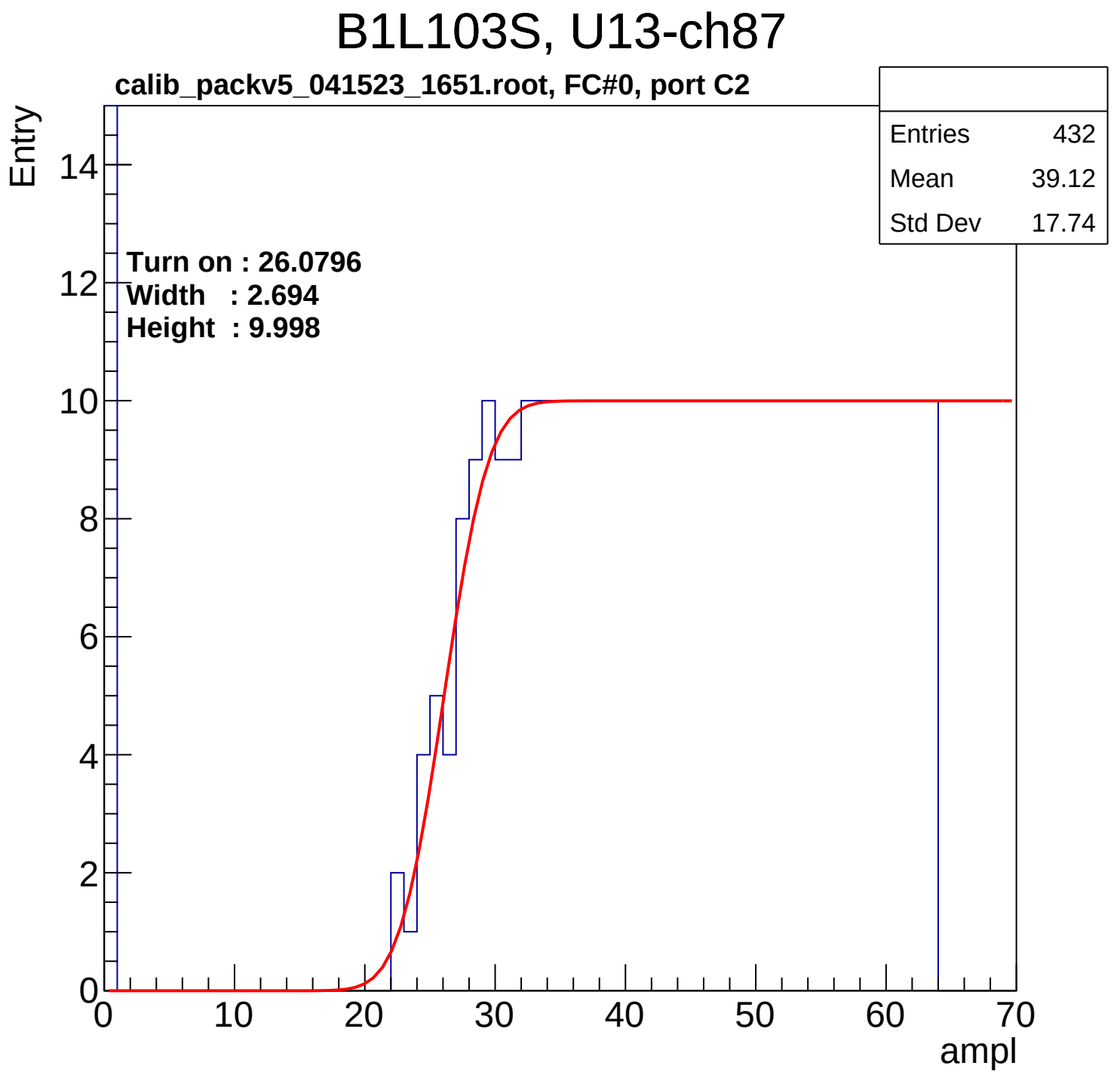
B1L103S, U13-ch87
calib_packv5_041523_1651.root, FC#0, port C2
Entries 432
Mean 39.12
Std Dev 17.74
Turn on : 26.0796
Width : 2.694
Height : 9.998
Entry
ampl
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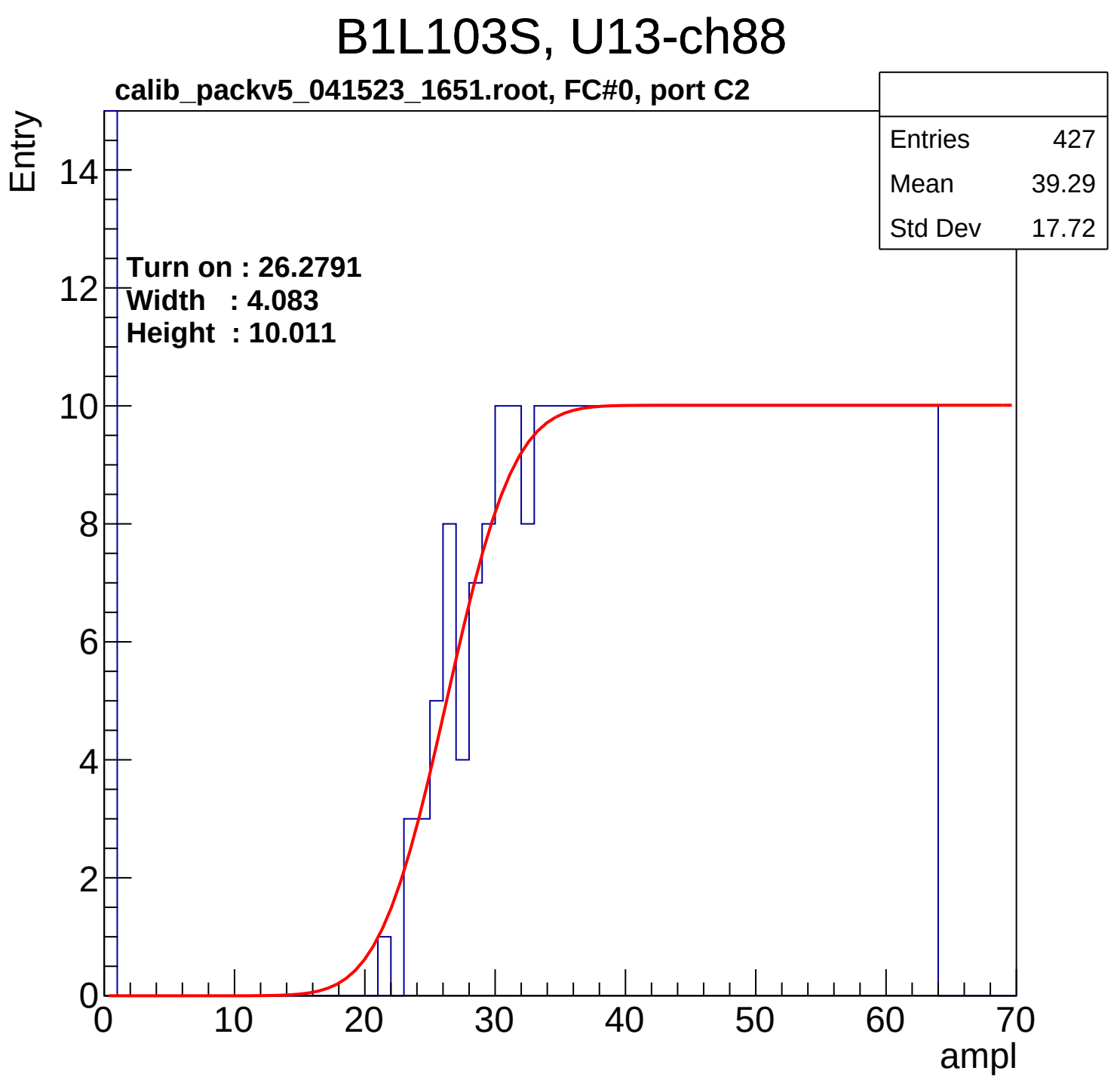
B1L103S, U13-ch88
calib_packv5_041523_1651.root, FC#0, port C2
Entries 427
Mean 39.29
Std Dev 17.72
Turn on : 26.2791
Width : 4.083
Height : 10.011
Entry
ampl
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4
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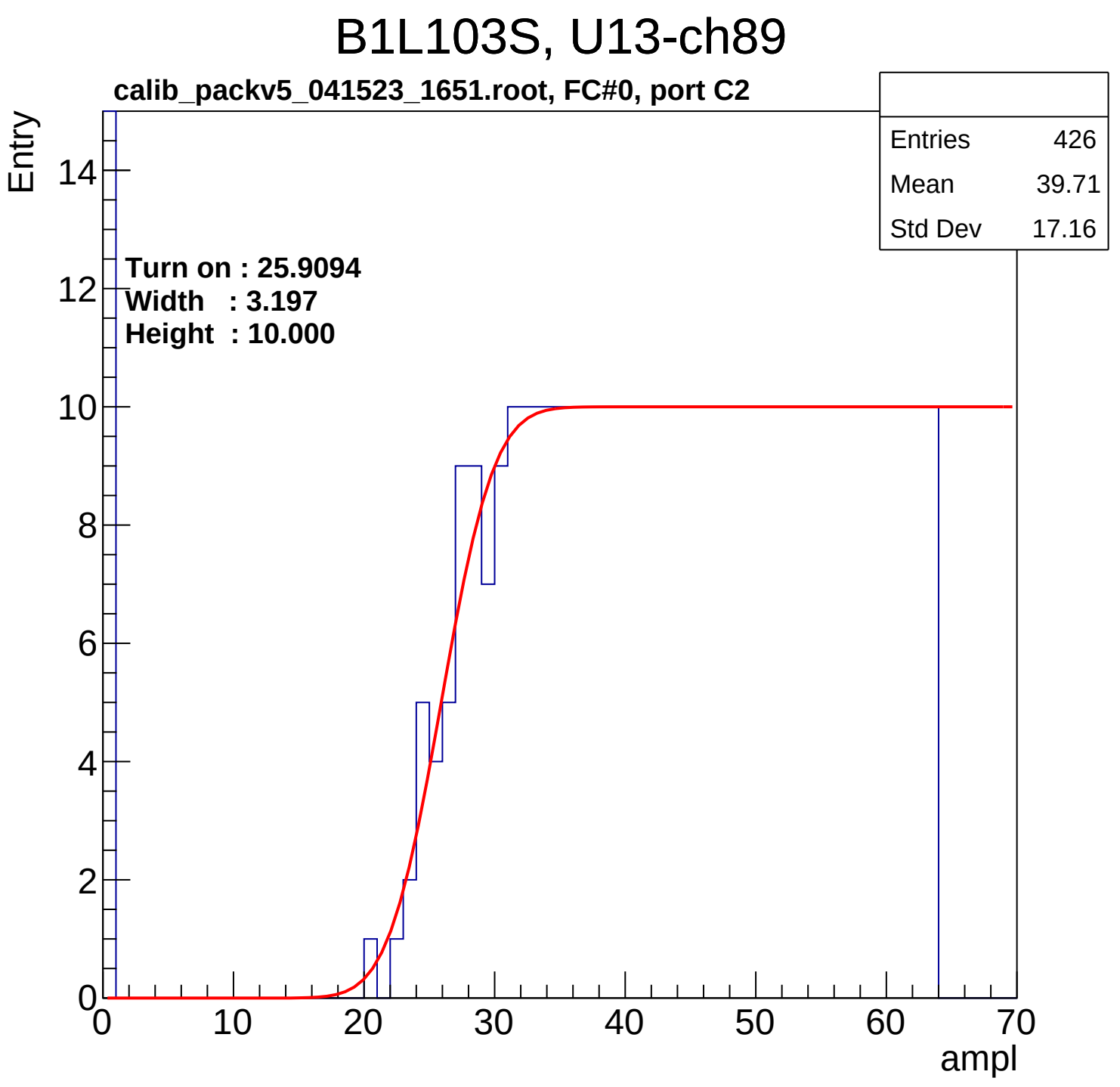
B1L103S, U13-ch89
calib_packv5_041523_1651.root, FC#0, port C2
Entries 426
Mean 39.71
Std Dev 17.16
Turn on : 25.9094
Width : 3.197
Height : 10.000
Entry
ampl
0
2
4
6
8
10
12
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0
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40
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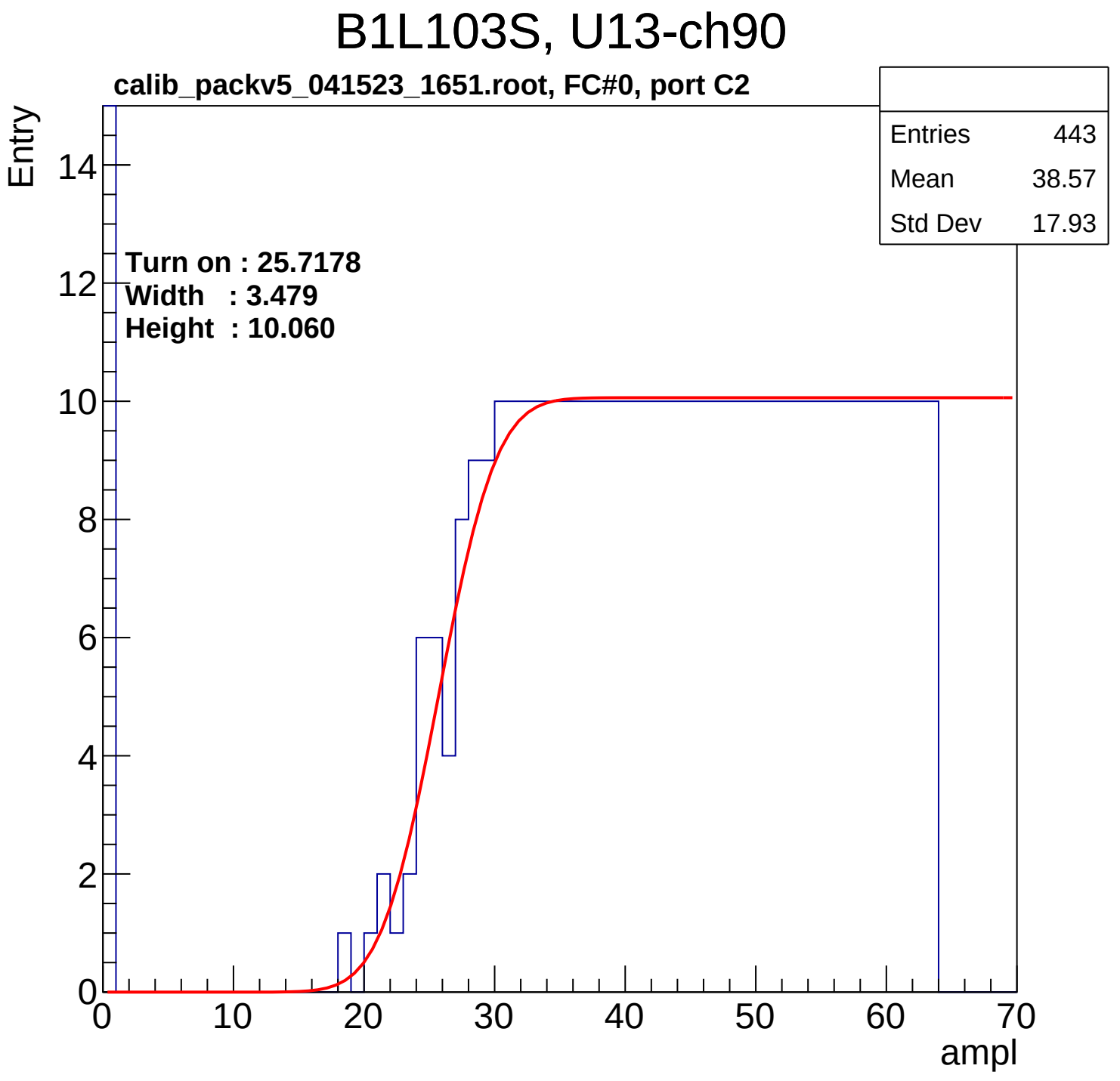
B1L103S, U13-ch90
calib_packv5_041523_1651.root, FC#0, port C2
Entries 443
Mean 38.57
Std Dev 17.93
Turn on : 25.7178
Width : 3.479
Height : 10.060
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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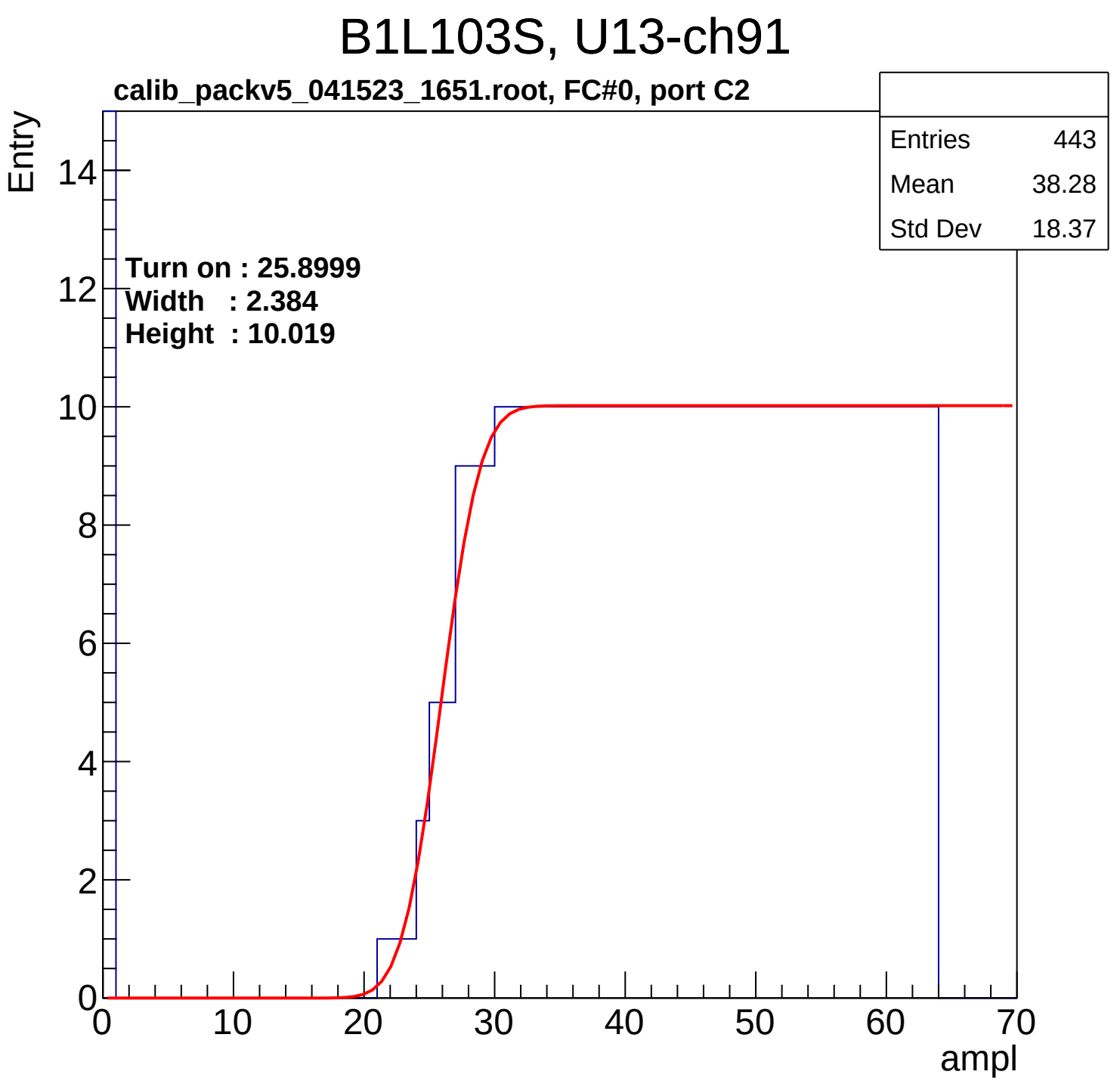
B1L103S, U13-ch91
calib_packv5_041523_1651.root, FC#0, port C2
Entries 443
Mean 38.28
Std Dev 18.37
Turn on : 25.8999
Width : 2.384
Height : 10.019
Entry
ampl
0
2
4
6
8
10
12
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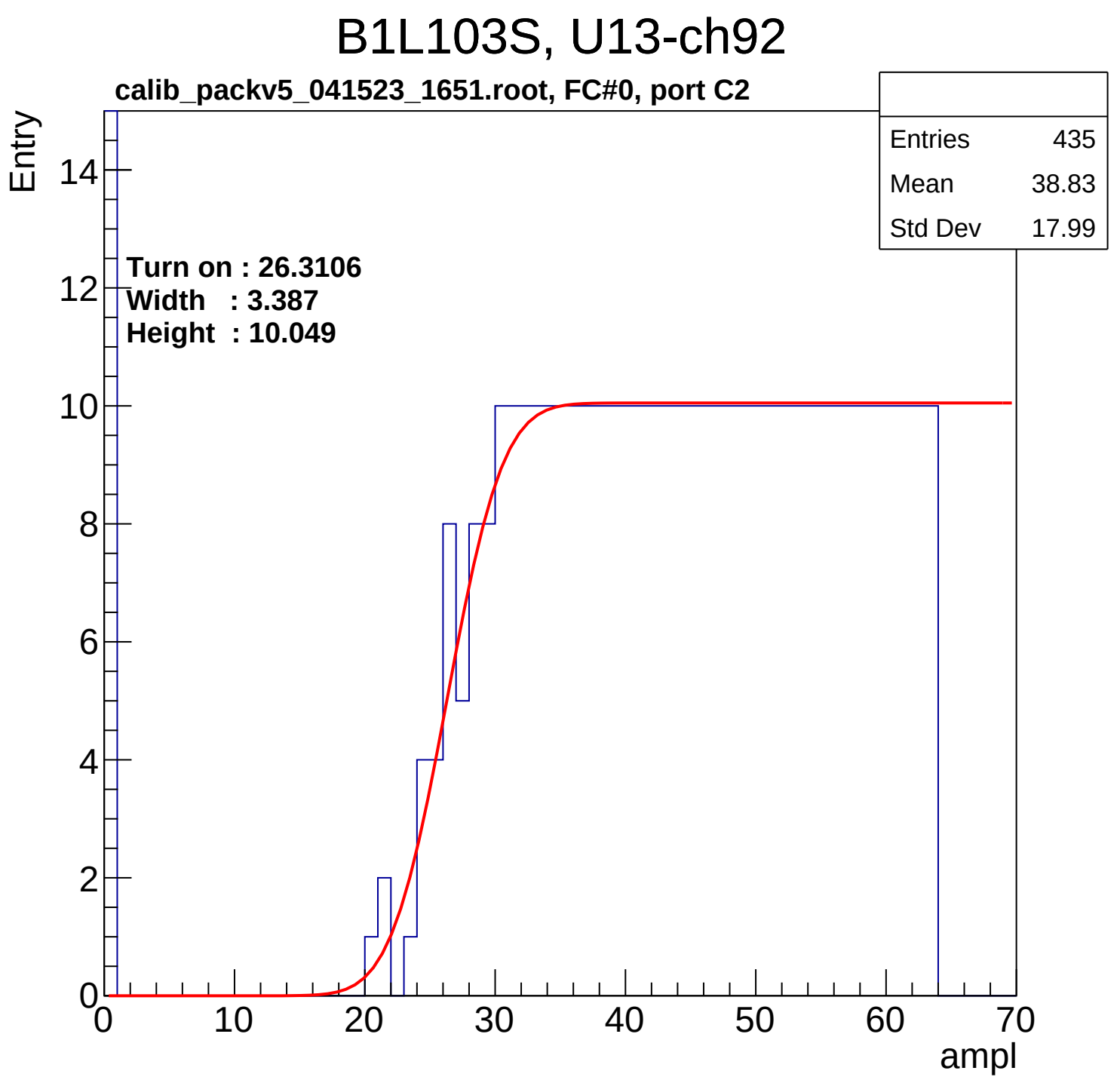
B1L103S, U13-ch92
calib_packv5_041523_1651.root, FC#0, port C2
Entries 435
Mean 38.83
Std Dev 17.99
Turn on : 26.3106
Width : 3.387
Height : 10.049
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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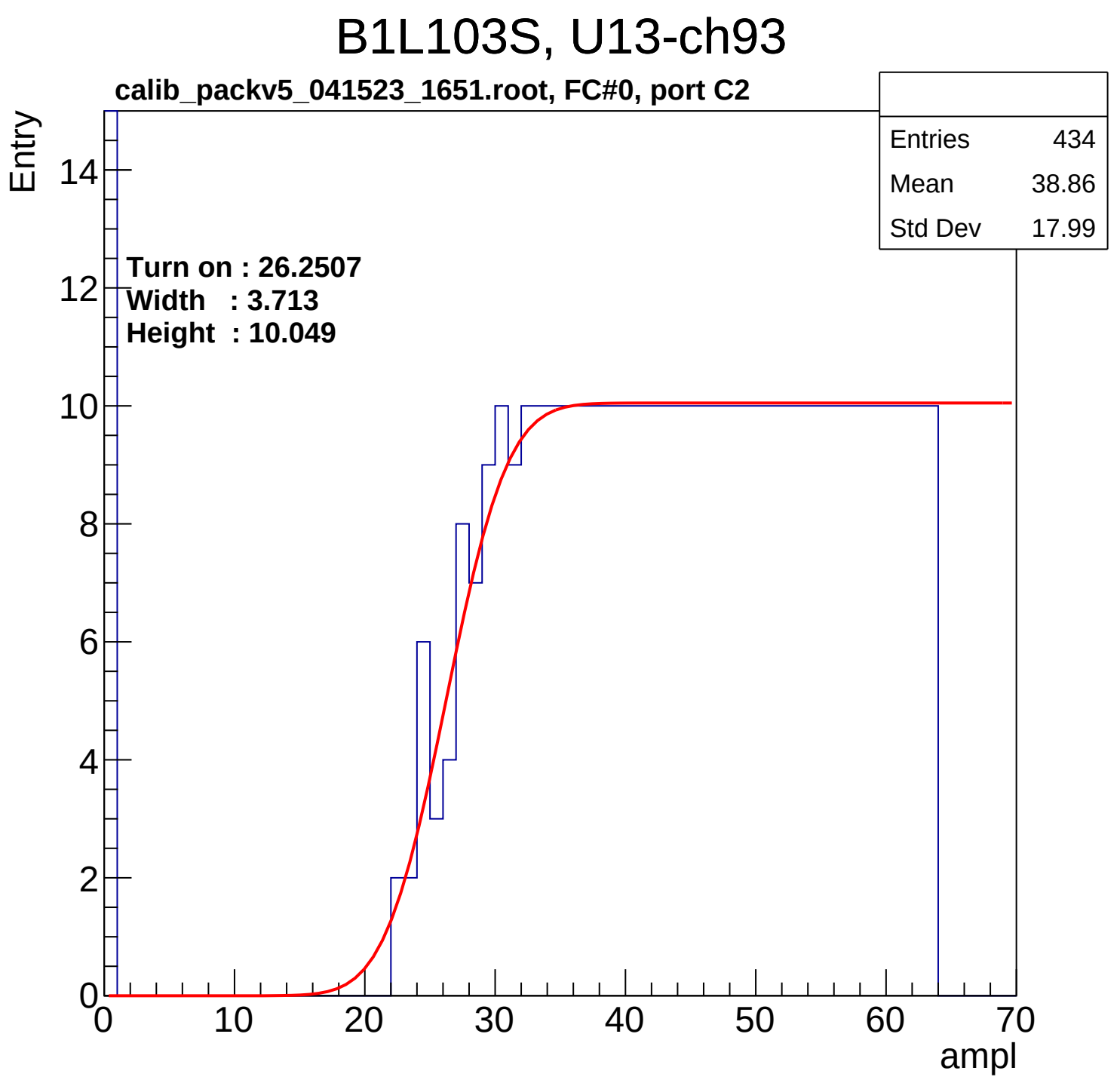
B1L103S, U13-ch93
calib_packv5_041523_1651.root, FC#0, port C2
Entries 434
Mean 38.86
Std Dev 17.99
Turn on : 26.2507
Width : 3.713
Height : 10.049
Entry
ampl
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6
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10
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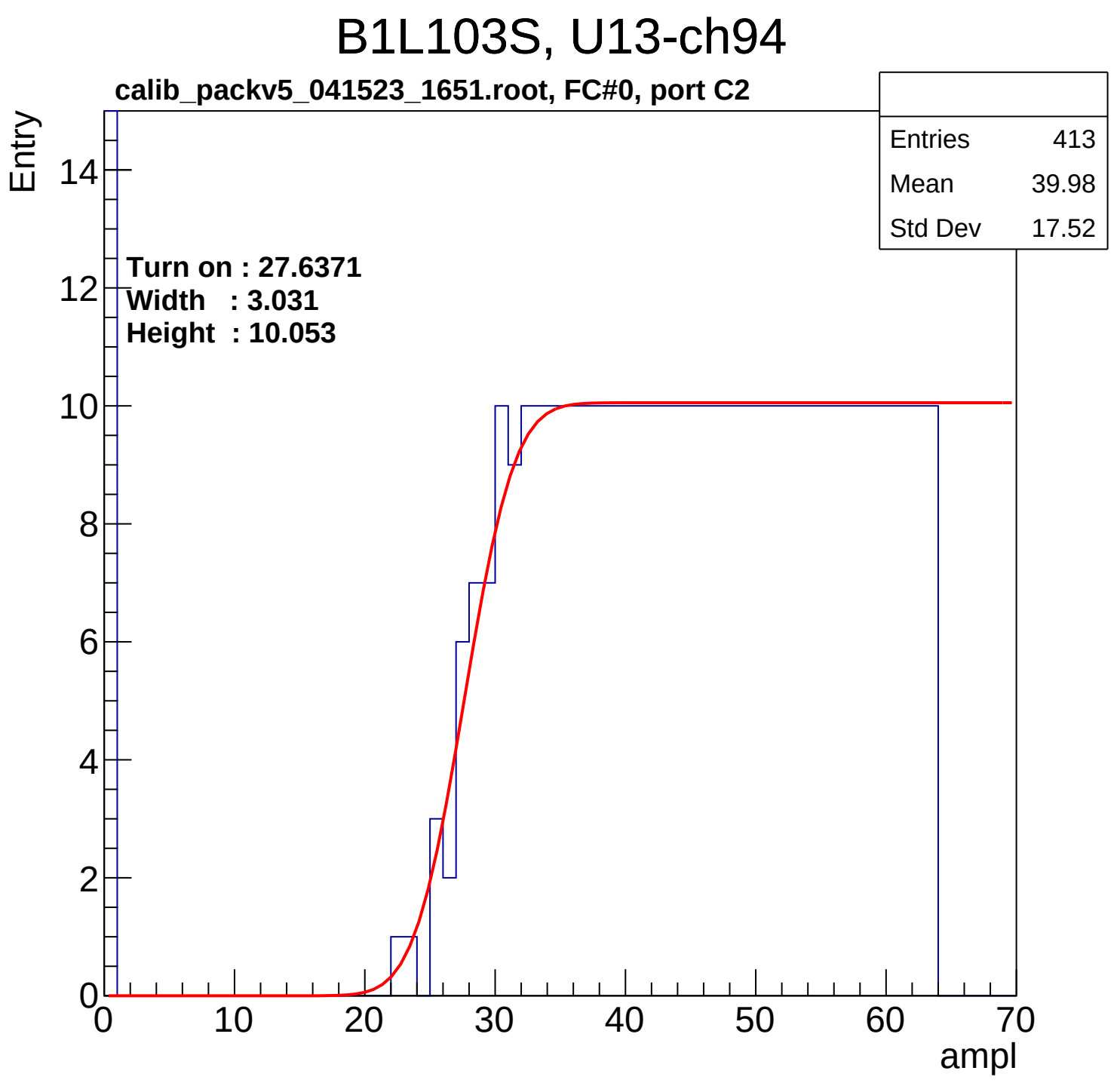
B1L103S, U13-ch94
calib_packv5_041523_1651.root, FC#0, port C2
Entries 413
Mean 39.98
Std Dev 17.52
Turn on : 27.6371
Width : 3.031
Height : 10.053
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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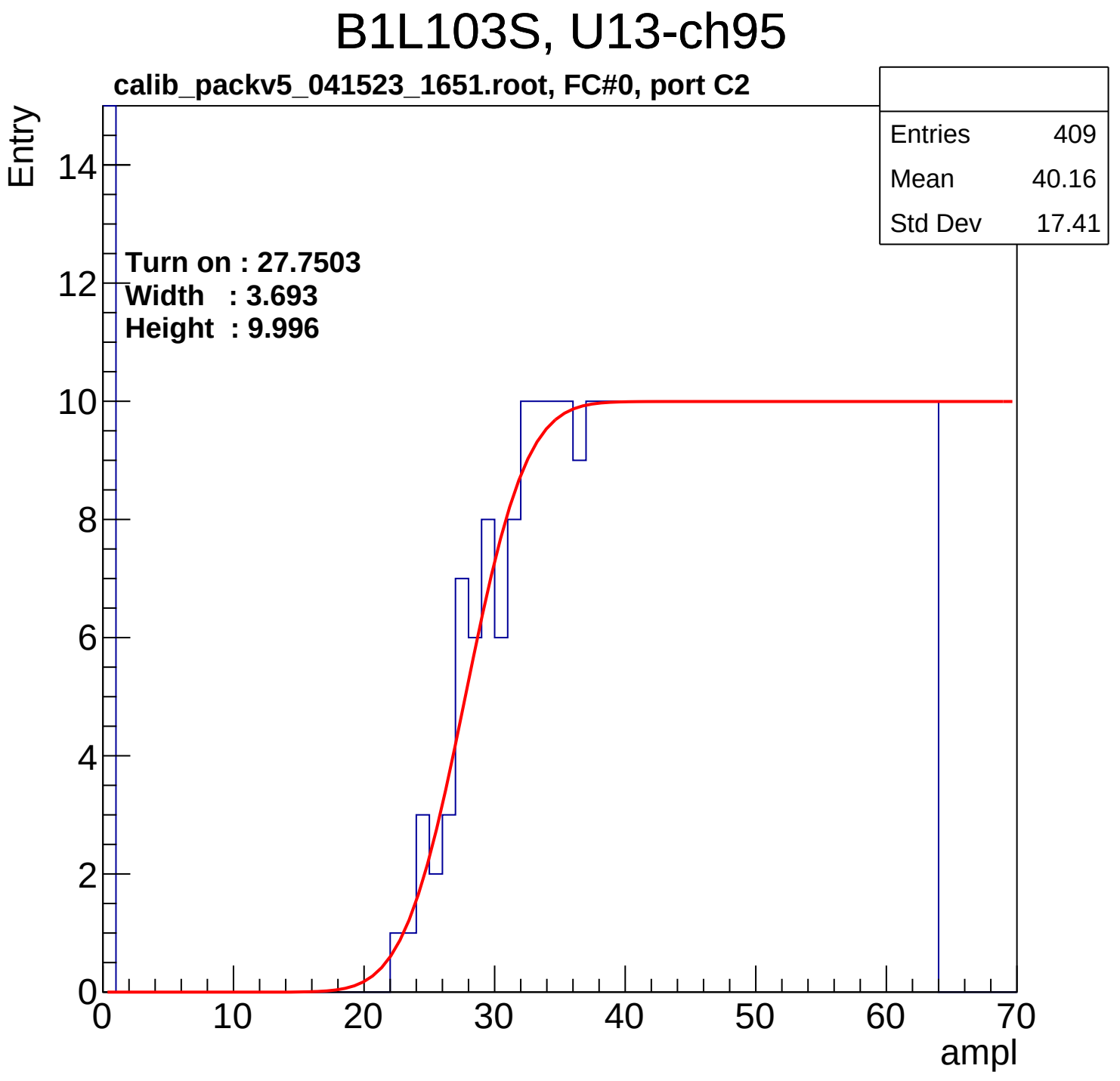
B1L103S, U13-ch95
calib_packv5_041523_1651.root, FC#0, port C2
Entries 409
Mean 40.16
Std Dev 17.41
Turn on : 27.7503
Width : 3.693
Height : 9.996
Entry
ampl
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2
4
6
8
10
12
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0
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20
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60
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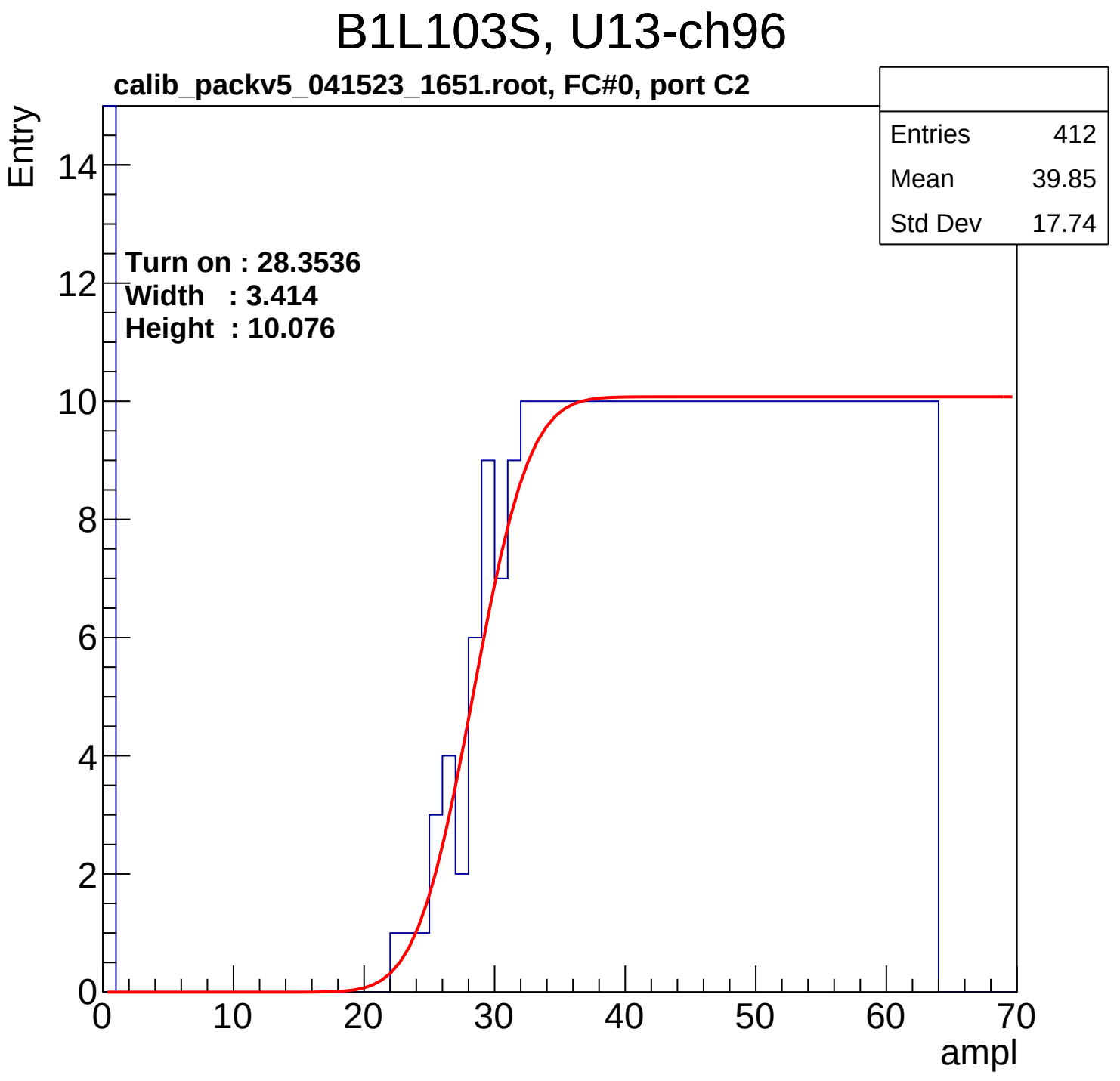
B1L103S, U13-ch96
calib_packv5_041523_1651.root, FC#0, port C2
Entries 412
Mean 39.85
Std Dev 17.74
Turn on : 28.3536
Width : 3.414
Height : 10.076
Entry
ampl
0
2
4
6
8
10
12
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60
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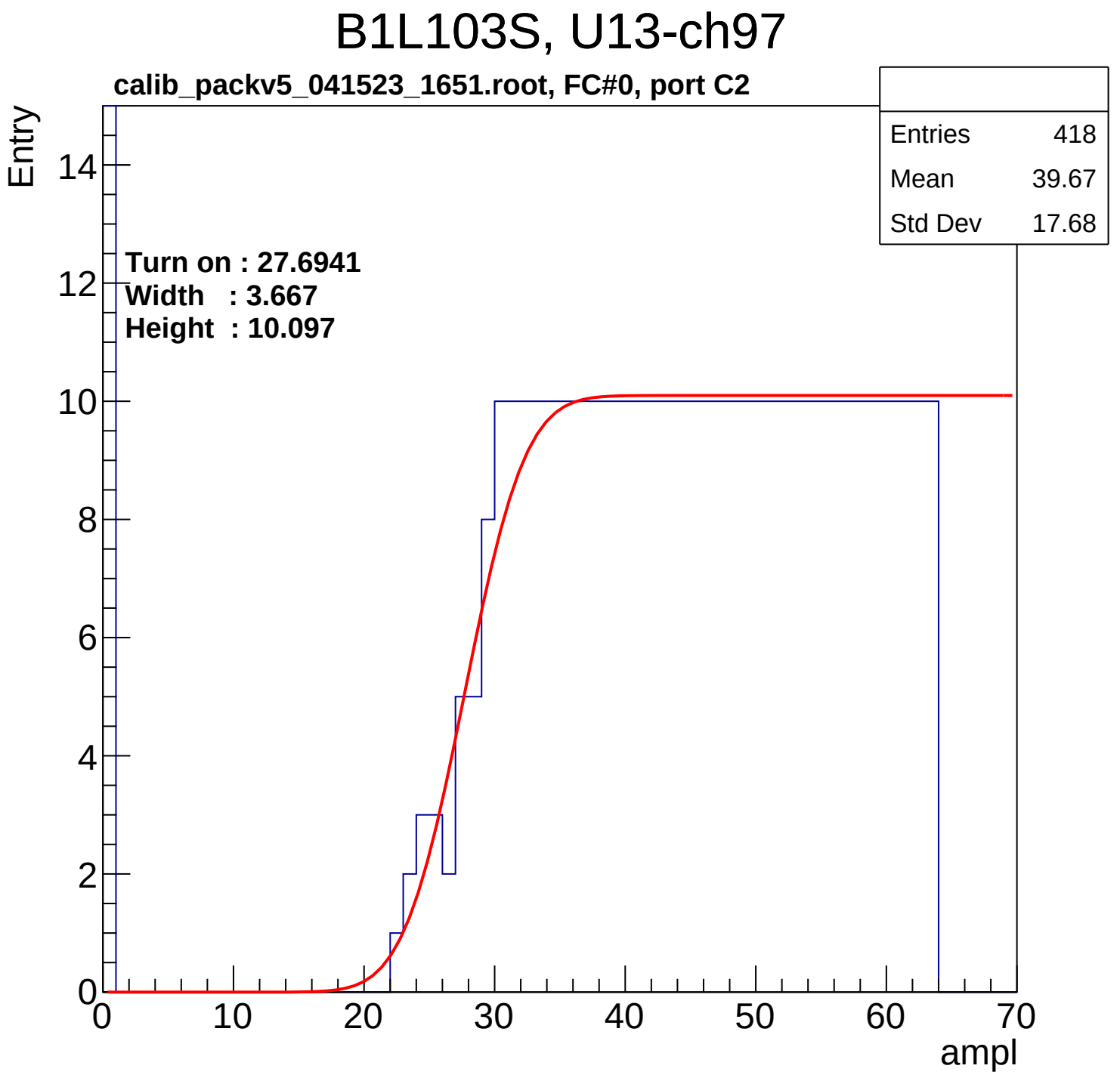
B1L103S, U13-ch97
calib_packv5_041523_1651.root, FC#0, port C2
Entries 418
Mean 39.67
Std Dev 17.68
Turn on : 27.6941
Width : 3.667
Height : 10.097
Entry
ampl
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2
4
6
8
10
12
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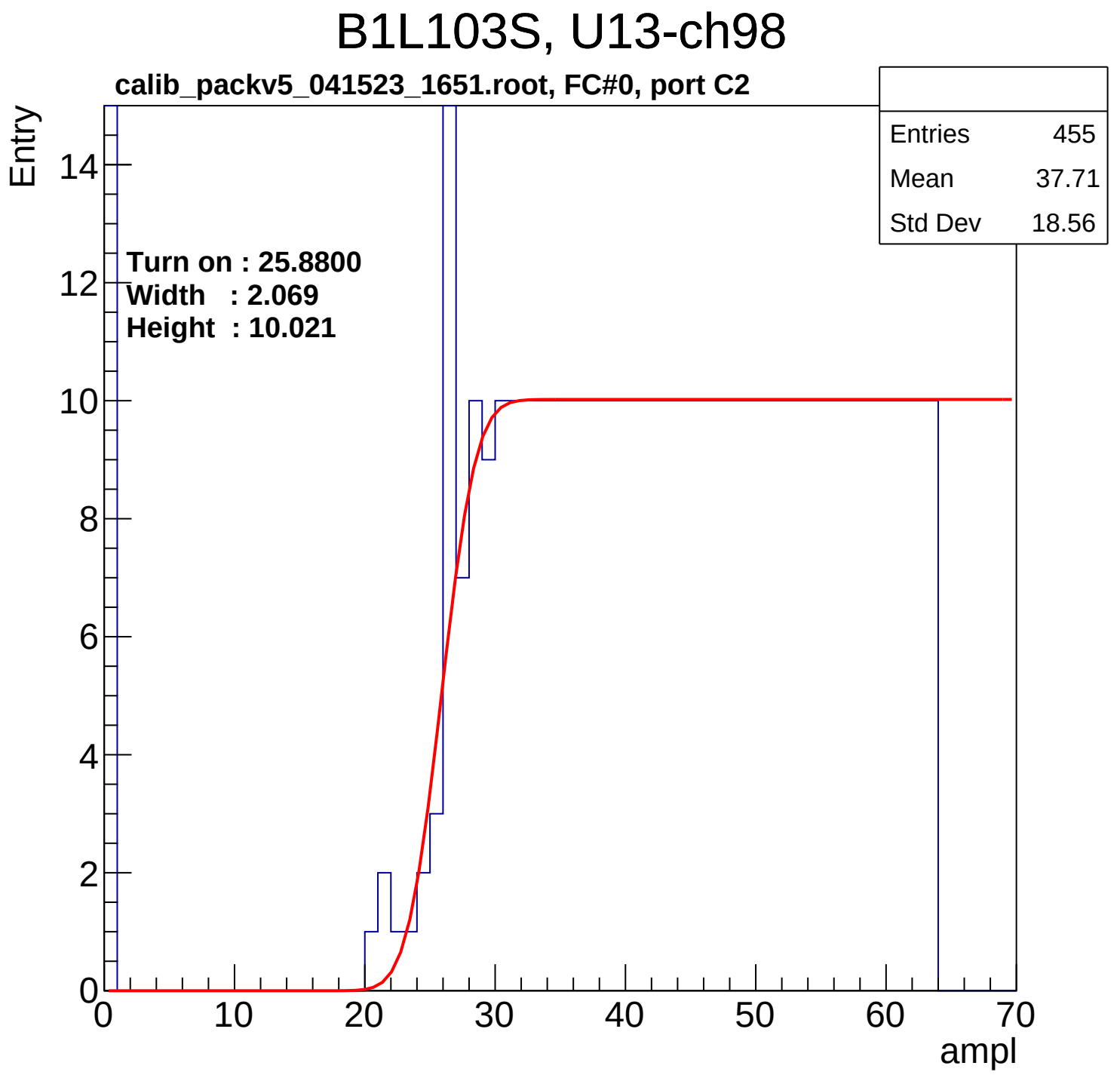
B1L103S, U13-ch98
calib_packv5_041523_1651.root, FC#0, port C2
Entries 455
Mean 37.71
Std Dev 18.56
Turn on : 25.8800
Width : 2.069
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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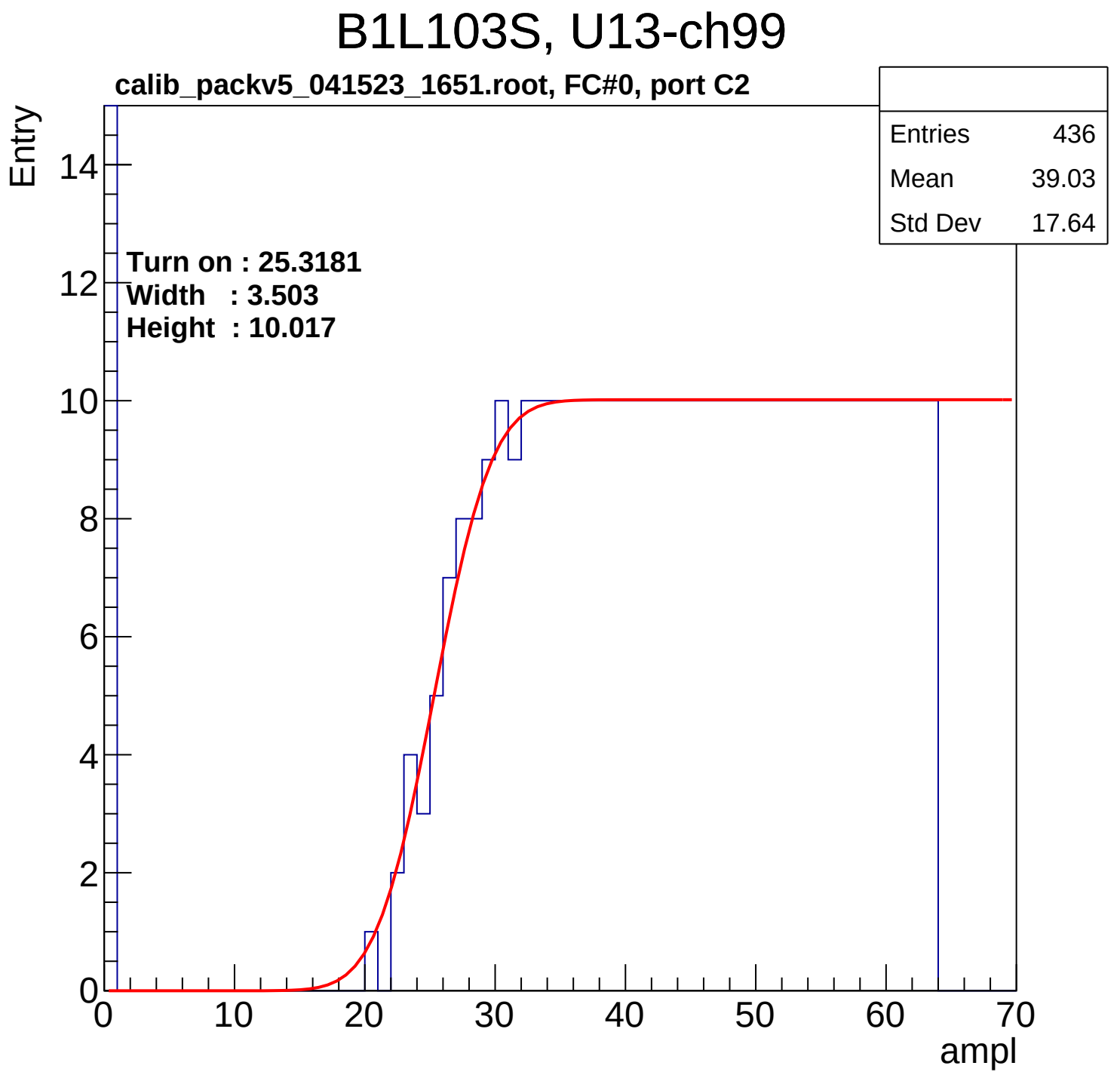
B1L103S, U13-ch99
calib_packv5_041523_1651.root, FC#0, port C2
Entries 436
Mean 39.03
Std Dev 17.64
Turn on : 25.3181
Width : 3.503
Height : 10.017
Entry
ampl
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2
4
6
8
10
12
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0
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60
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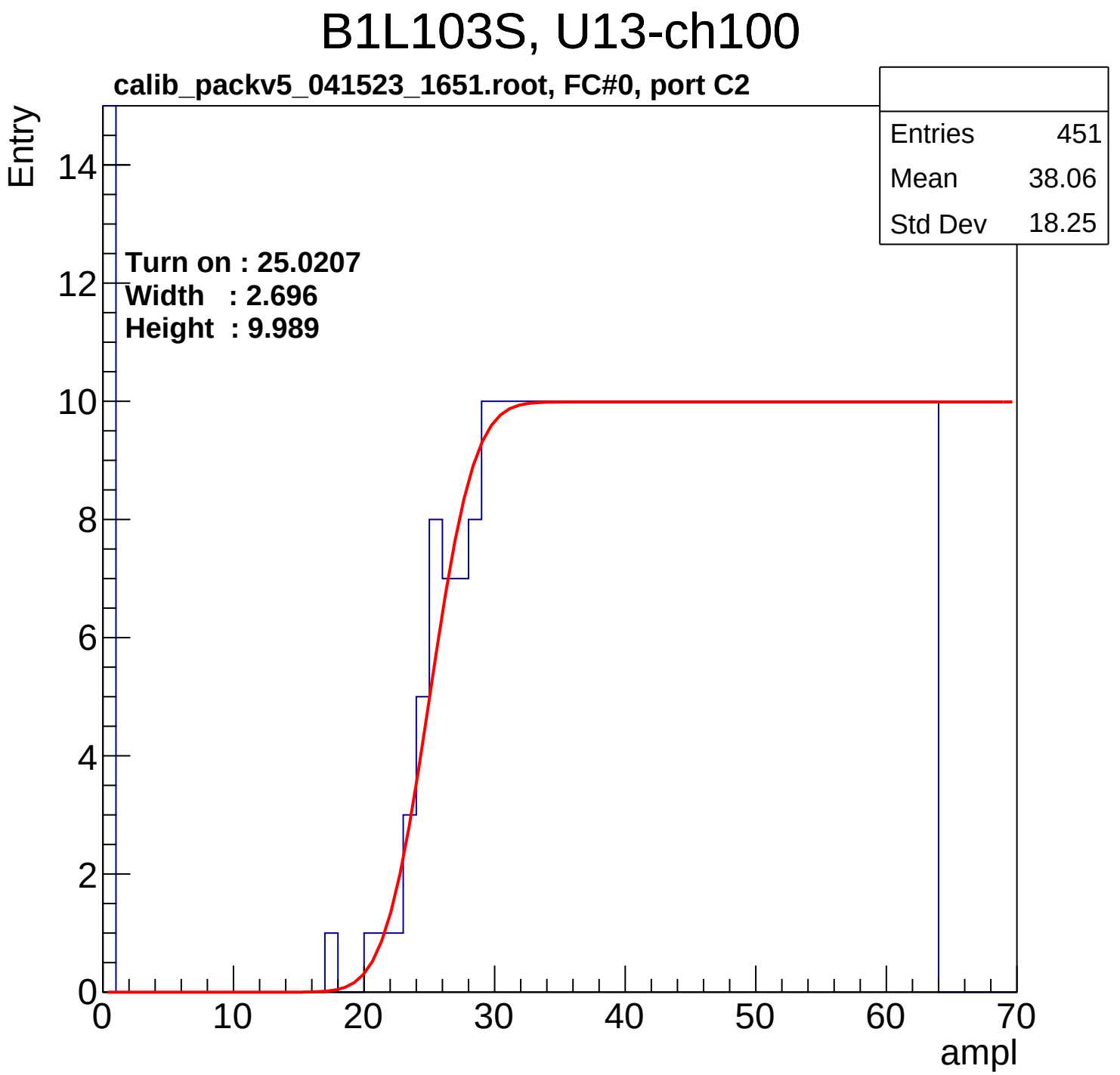
B1L103S, U13-ch100
calib_packv5_041523_1651.root, FC#0, port C2
Entries 451
Mean 38.06
Std Dev 18.25
Turn on : 25.0207
Width : 2.696
Height : 9.989
Entry
ampl
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6
8
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20
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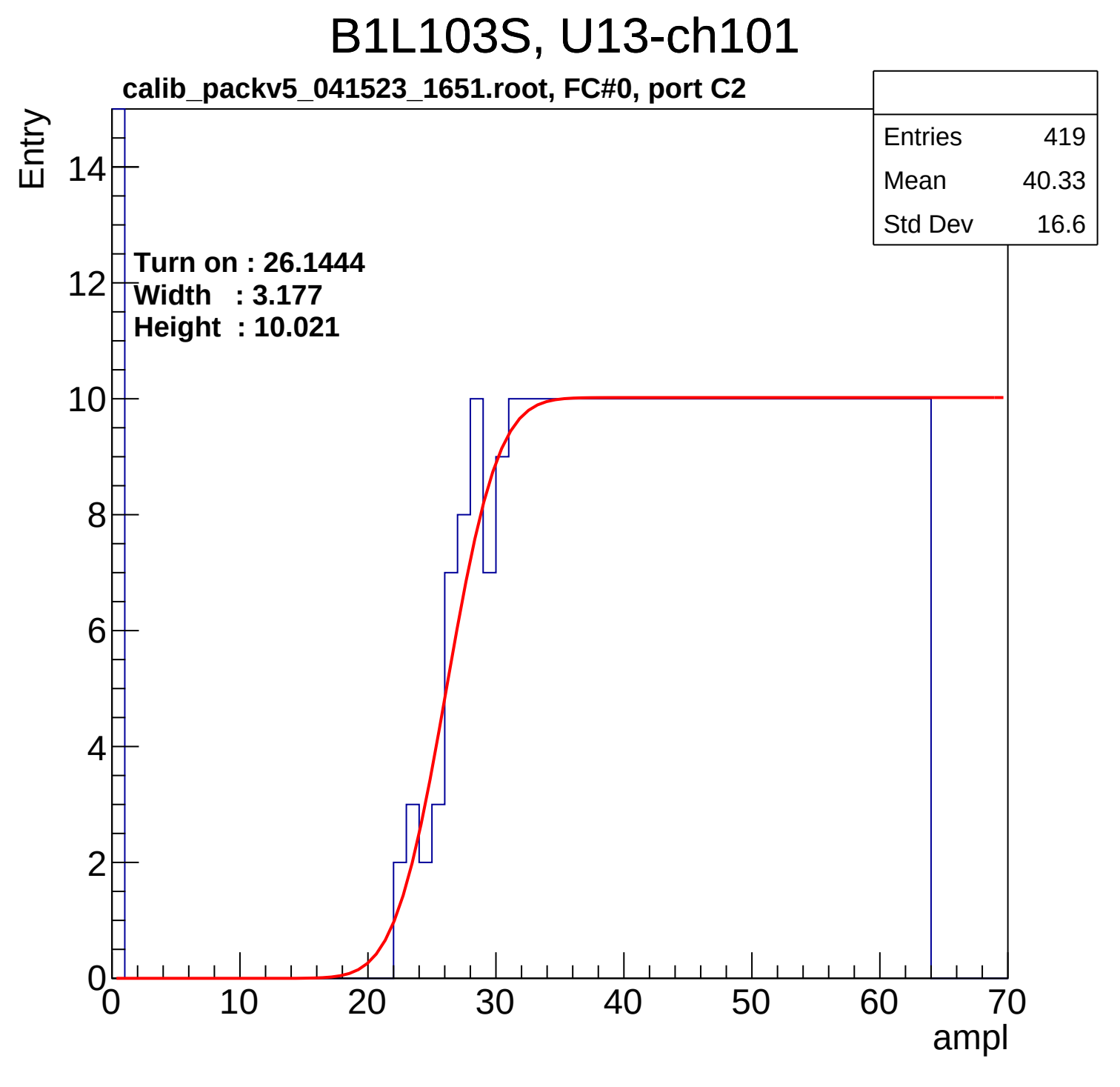
B1L103S, U13-ch101
calib_packv5_041523_1651.root, FC#0, port C2
Entries 419
Mean 40.33
Std Dev 16.6
Turn on : 26.1444
Width : 3.177
Height : 10.021
Entry
ampl
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8
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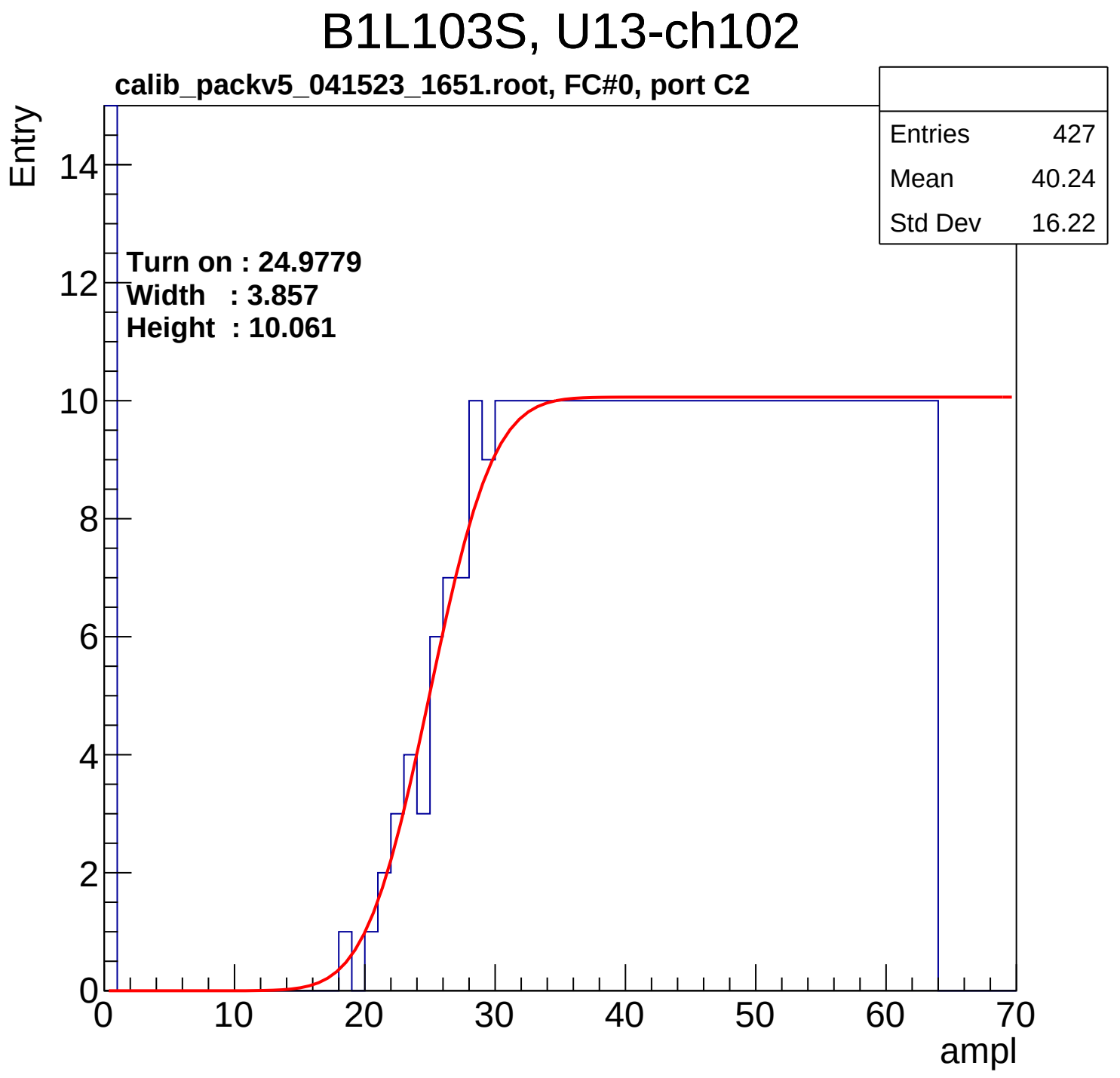
B1L103S, U13-ch102
calib_packv5_041523_1651.root, FC#0, port C2
Entries 427
Mean 40.24
Std Dev 16.22
Turn on : 24.9779
Width : 3.857
Height : 10.061
Entry
ampl
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4
6
8
10
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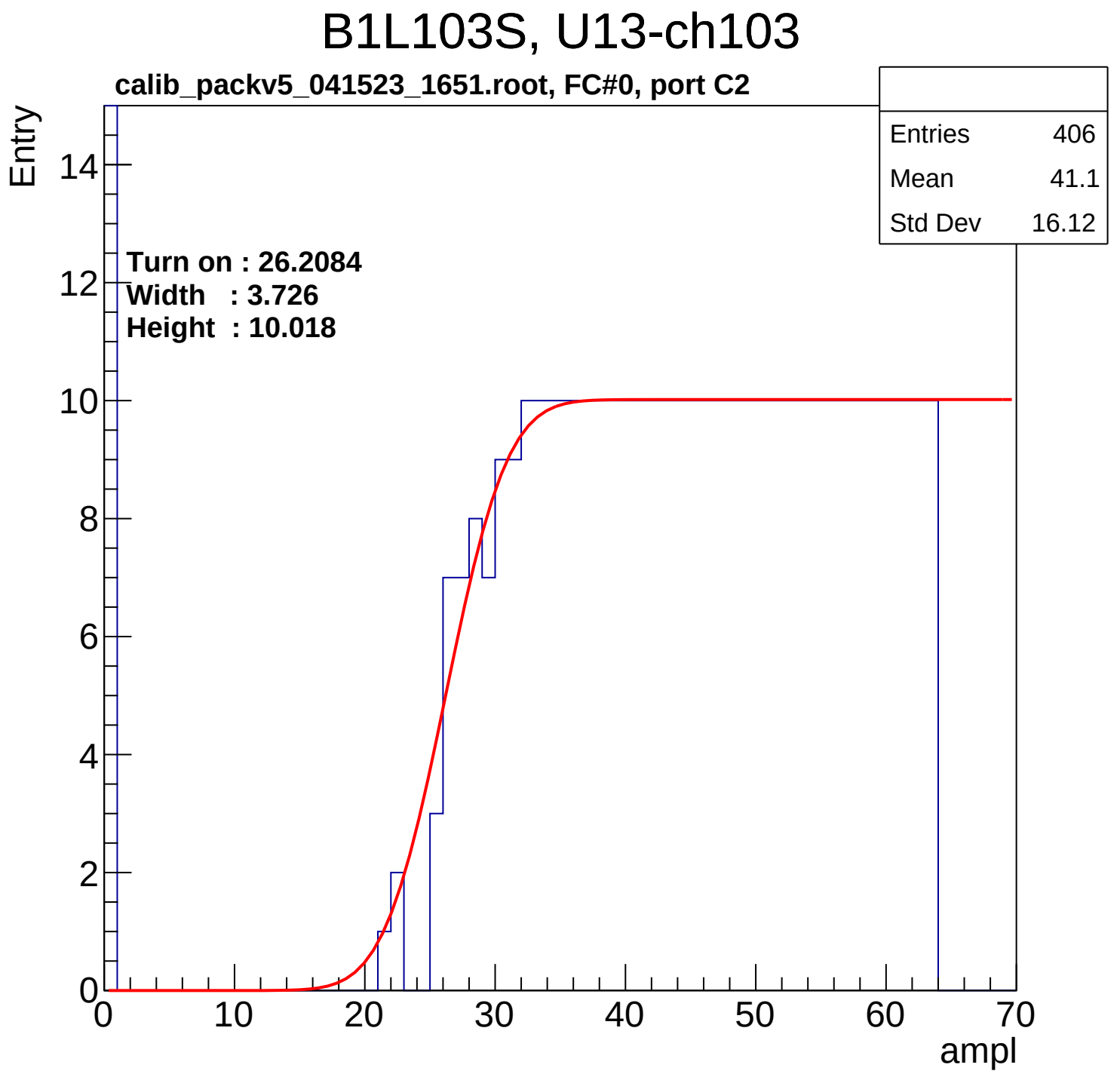
B1L103S, U13-ch103
calib_packv5_041523_1651.root, FC#0, port C2
Entries 406
Mean 41.1
Std Dev 16.12
Turn on : 26.2084
Width : 3.726
Height : 10.018
Entry
ampl
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2
4
6
8
10
12
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0
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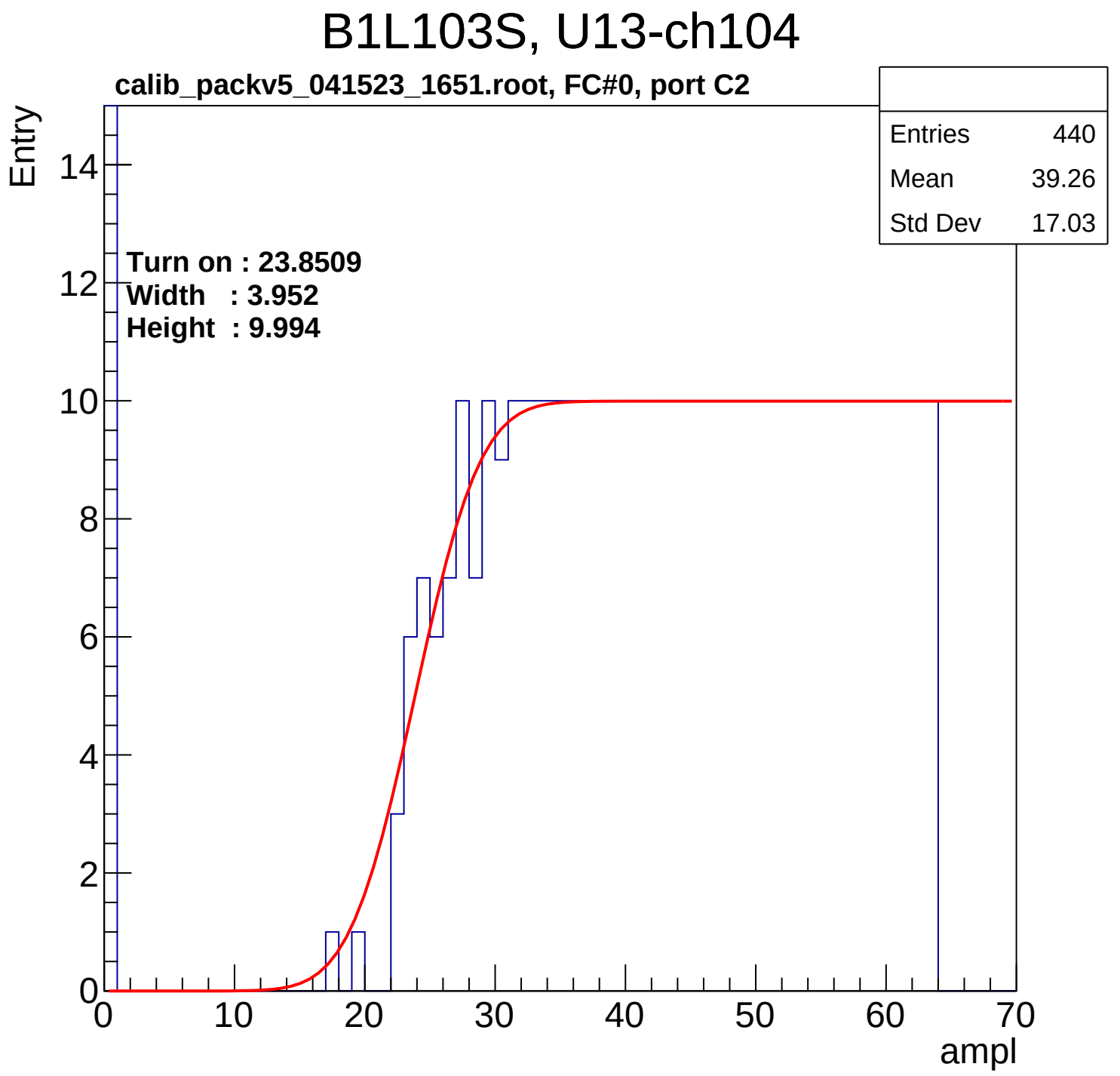
B1L103S, U13-ch104
calib_packv5_041523_1651.root, FC#0, port C2
Entries 440
Mean 39.26
Std Dev 17.03
Turn on : 23.8509
Width : 3.952
Height : 9.994
Entry
ampl
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2
4
6
8
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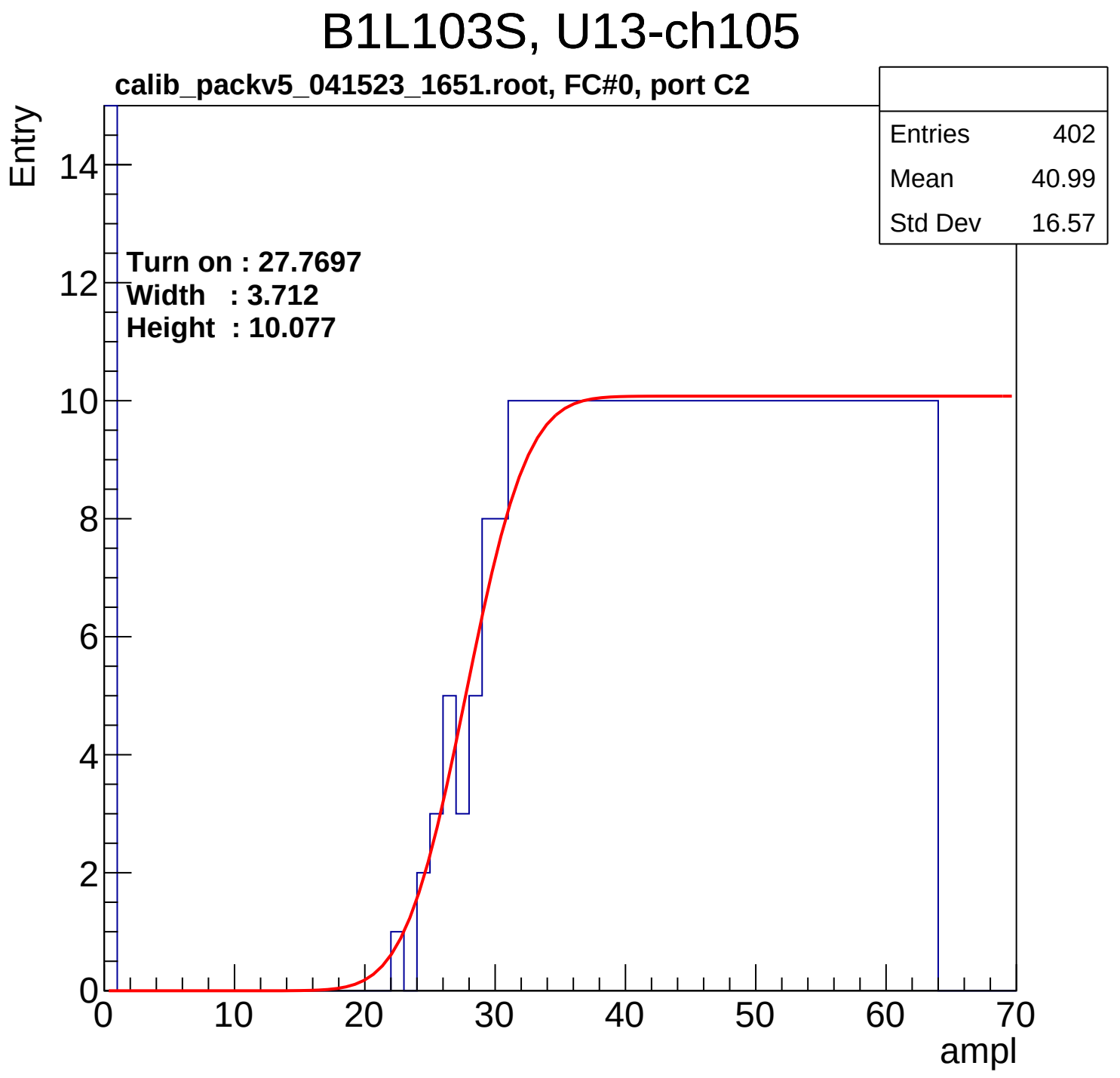
B1L103S, U13-ch105
calib_packv5_041523_1651.root, FC#0, port C2
Entries 402
Mean 40.99
Std Dev 16.57
Turn on : 27.7697
Width : 3.712
Height : 10.077
Entry
ampl
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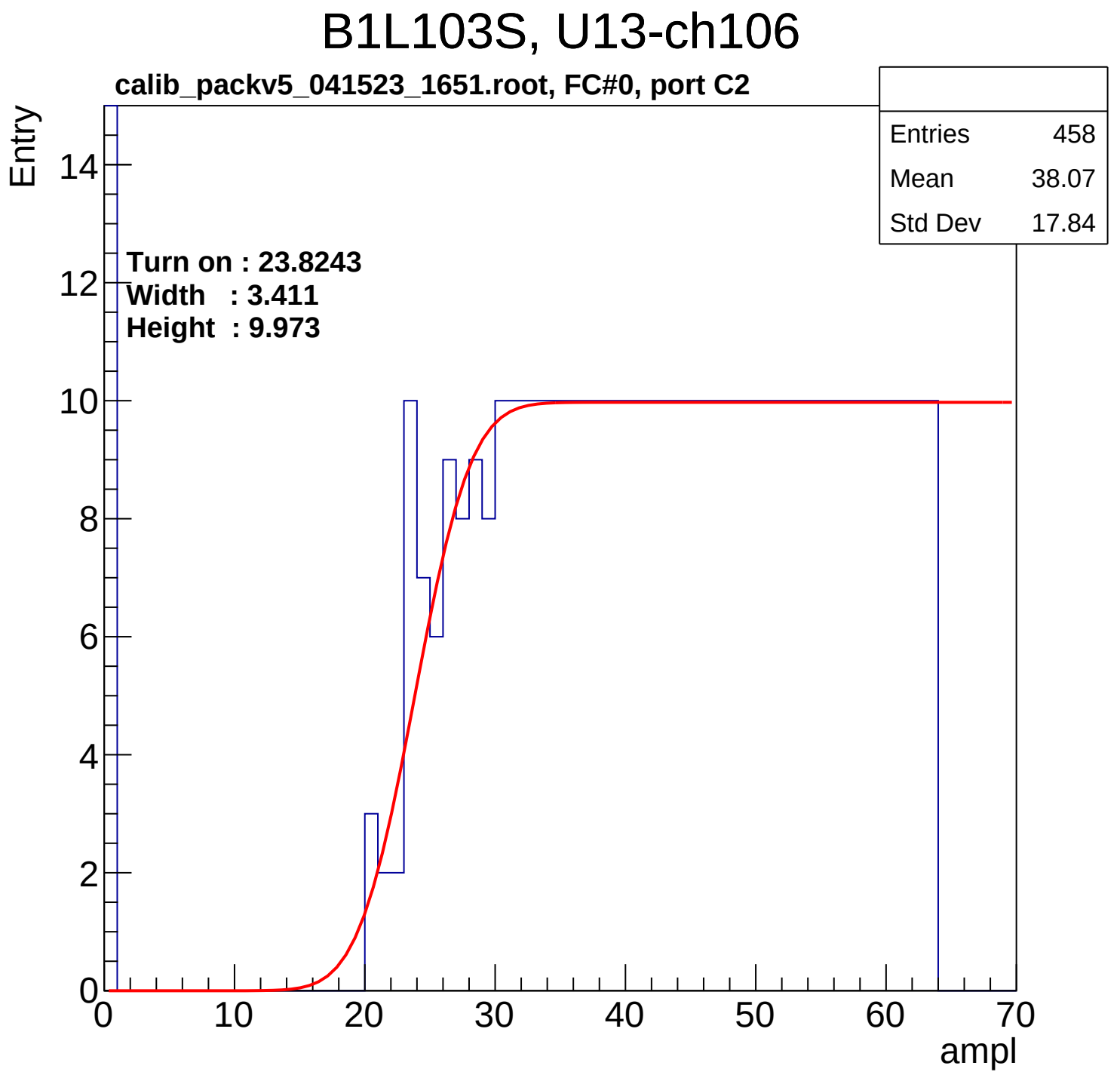
B1L103S, U13-ch106
calib_packv5_041523_1651.root, FC#0, port C2
Entries 458
Mean 38.07
Std Dev 17.84
Turn on : 23.8243
Width : 3.411
Height : 9.973
Entry
ampl
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8
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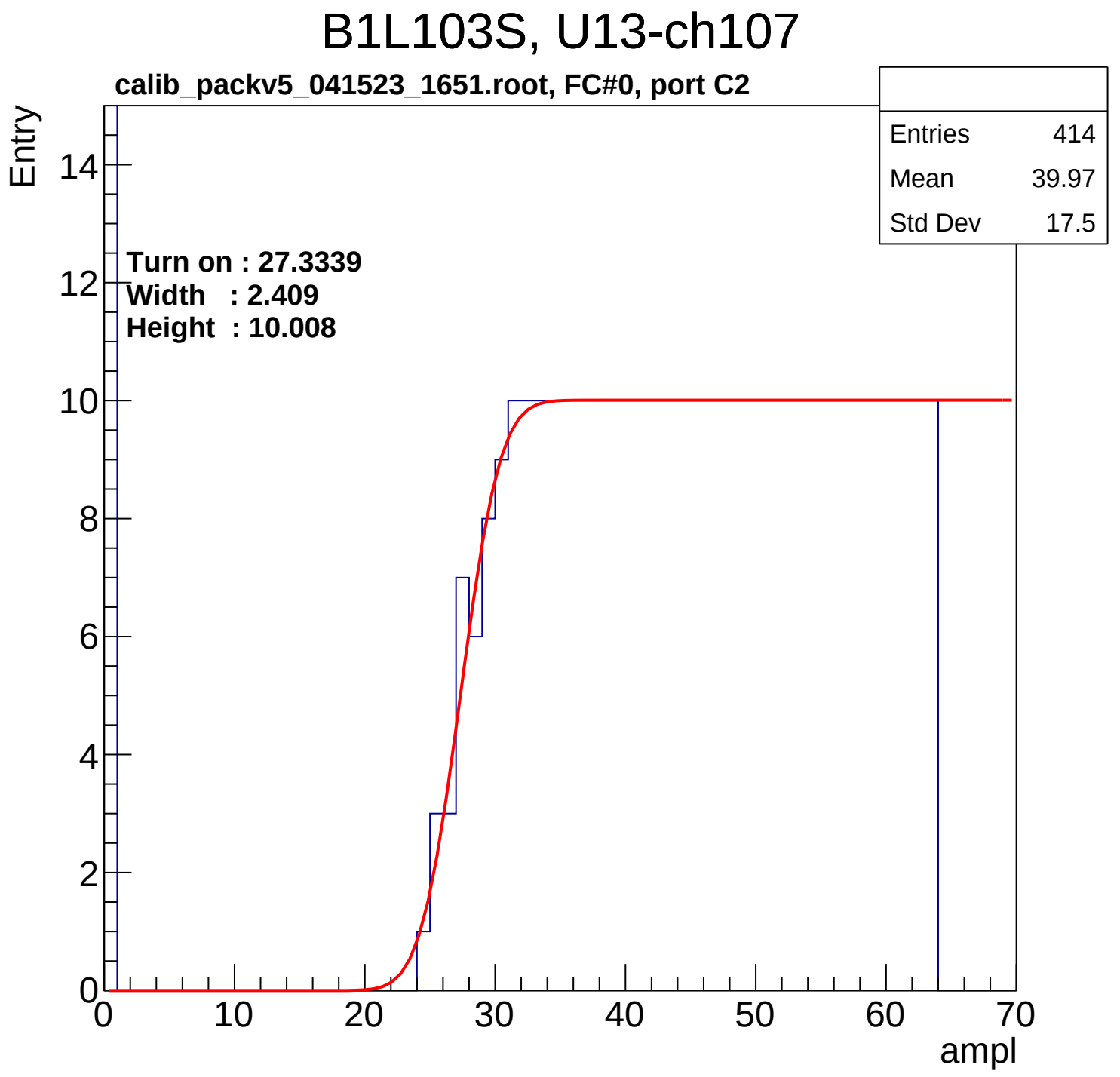
B1L103S, U13-ch107
calib_packv5_041523_1651.root, FC#0, port C2
Entries 414
Mean 39.97
Std Dev 17.5
Turn on : 27.3339
Width : 2.409
Height : 10.008
Entry
ampl
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6
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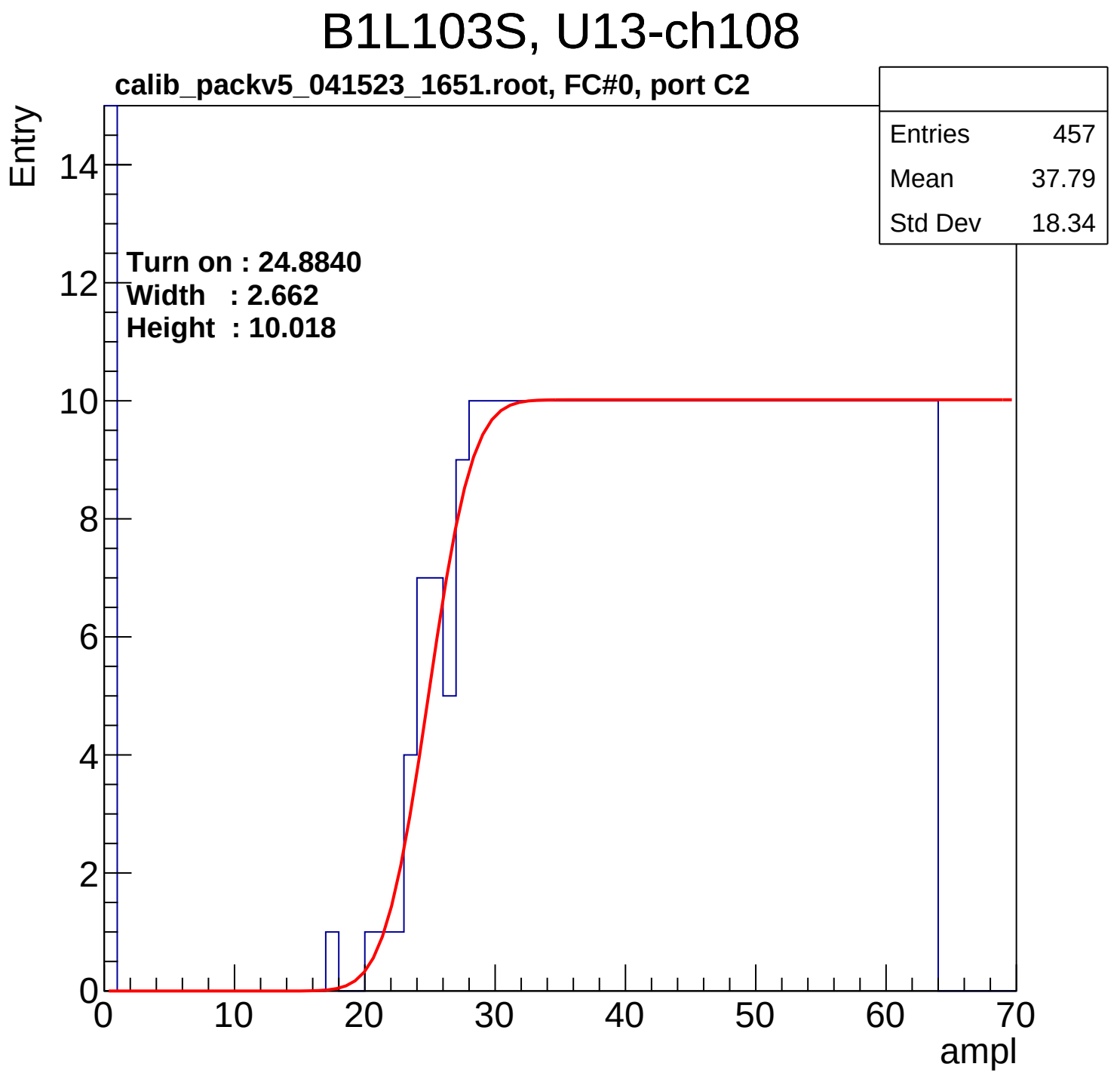
B1L103S, U13-ch108
calib_packv5_041523_1651.root, FC#0, port C2
Entries 457
Mean 37.79
Std Dev 18.34
Turn on : 24.8840
Width : 2.662
Height : 10.018
Entry
ampl
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6
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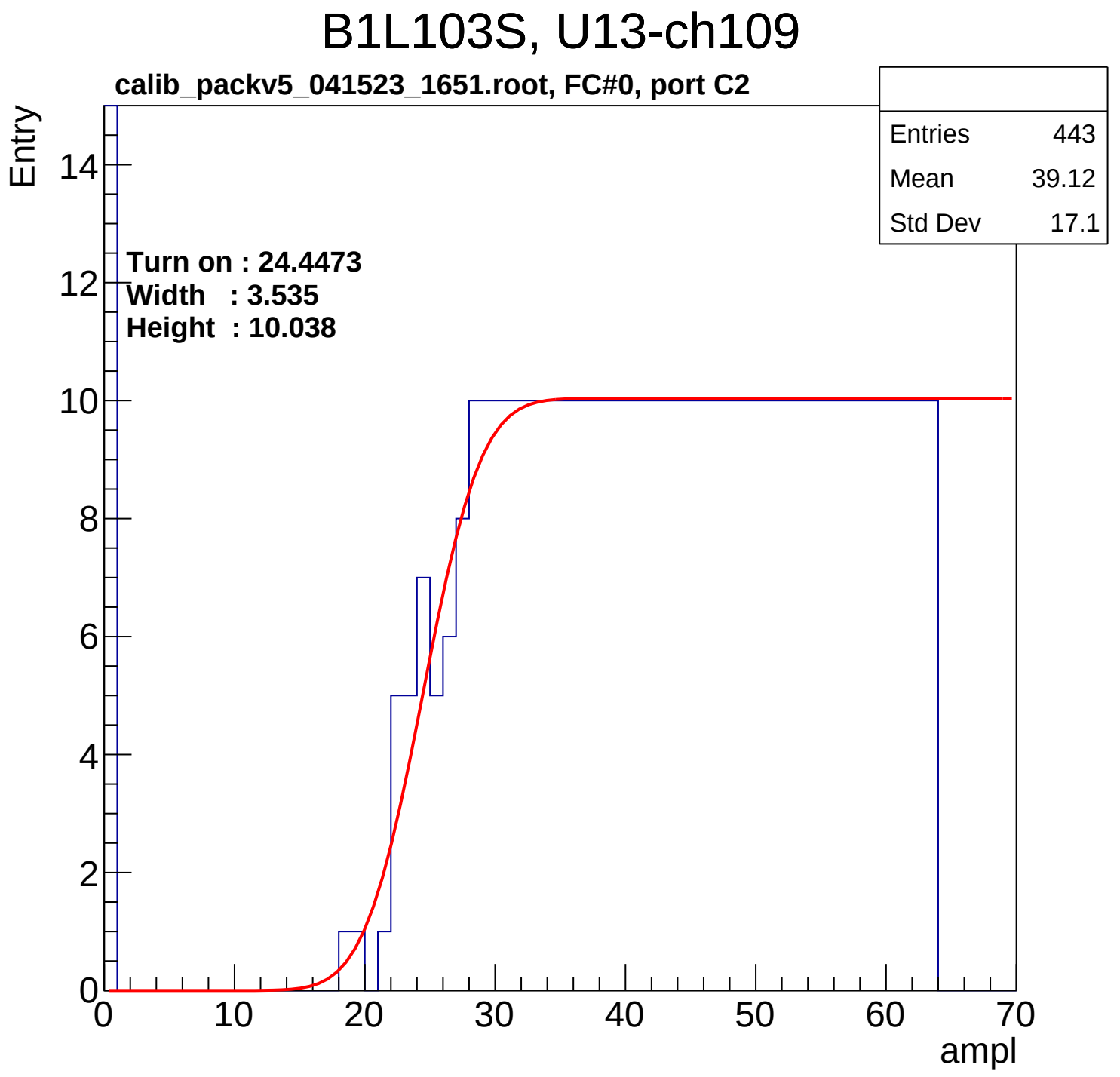
B1L103S, U13-ch109
calib_packv5_041523_1651.root, FC#0, port C2
Entries 443
Mean 39.12
Std Dev 17.1
Turn on : 24.4473
Width : 3.535
Height : 10.038
Entry
ampl
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6
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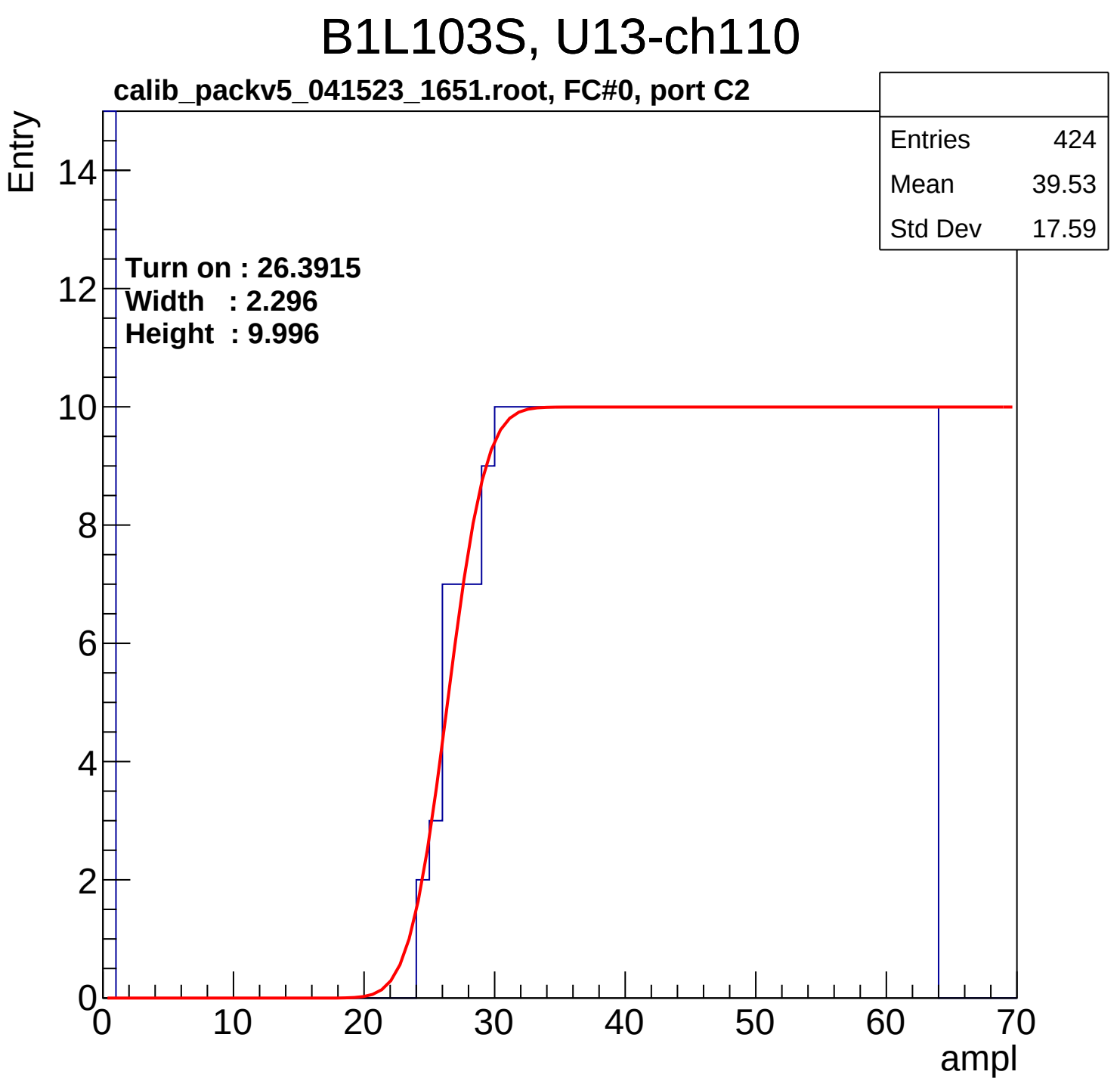
B1L103S, U13-ch110
calib_packv5_041523_1651.root, FC#0, port C2
Entries 424
Mean 39.53
Std Dev 17.59
Turn on : 26.3915
Width : 2.296
Height : 9.996
Entry
ampl
0
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4
6
8
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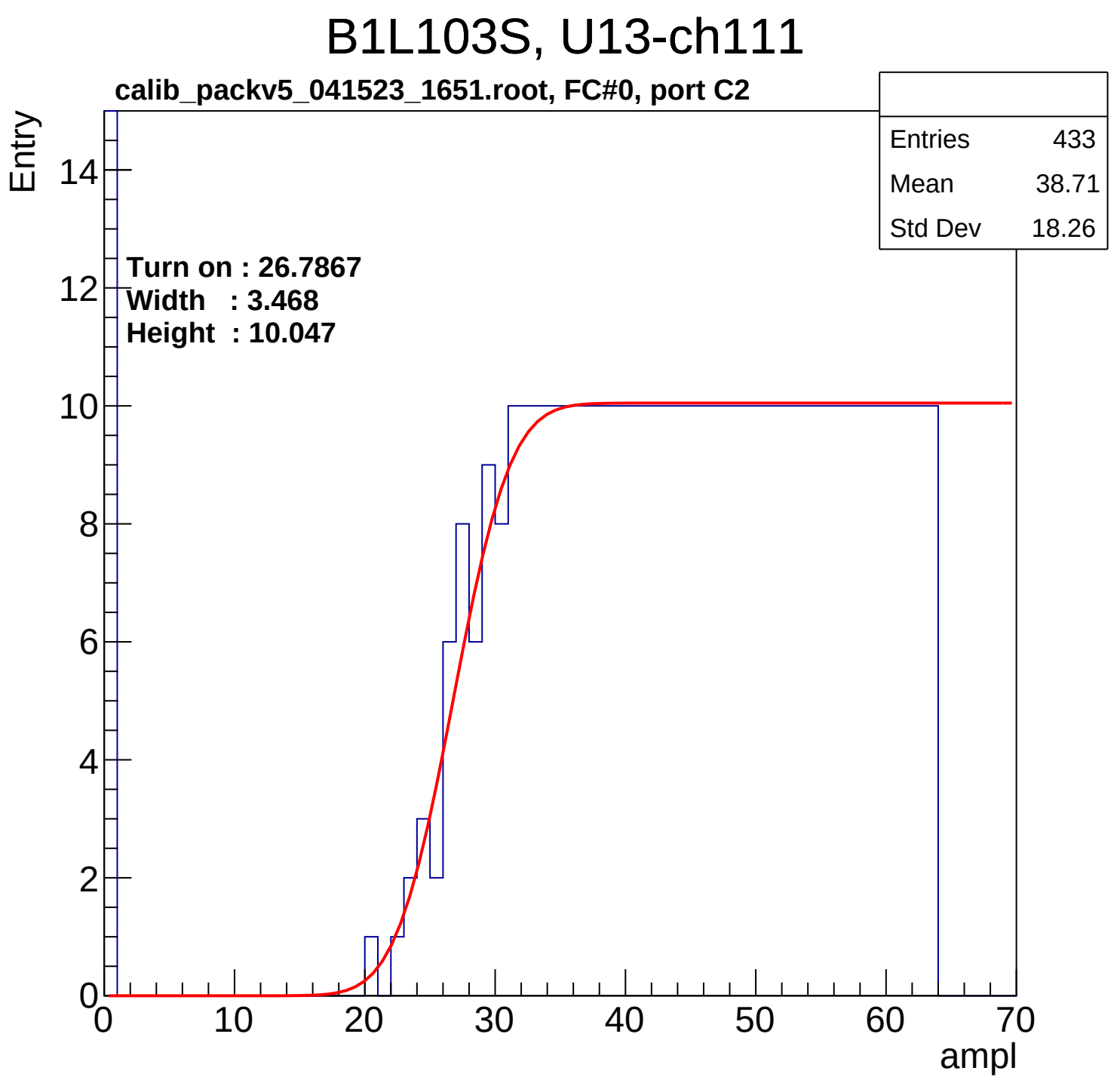
B1L103S, U13-ch111
calib_packv5_041523_1651.root, FC#0, port C2
Entries 433
Mean 38.71
Std Dev 18.26
Turn on : 26.7867
Width : 3.468
Height : 10.047
Entry
ampl
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8
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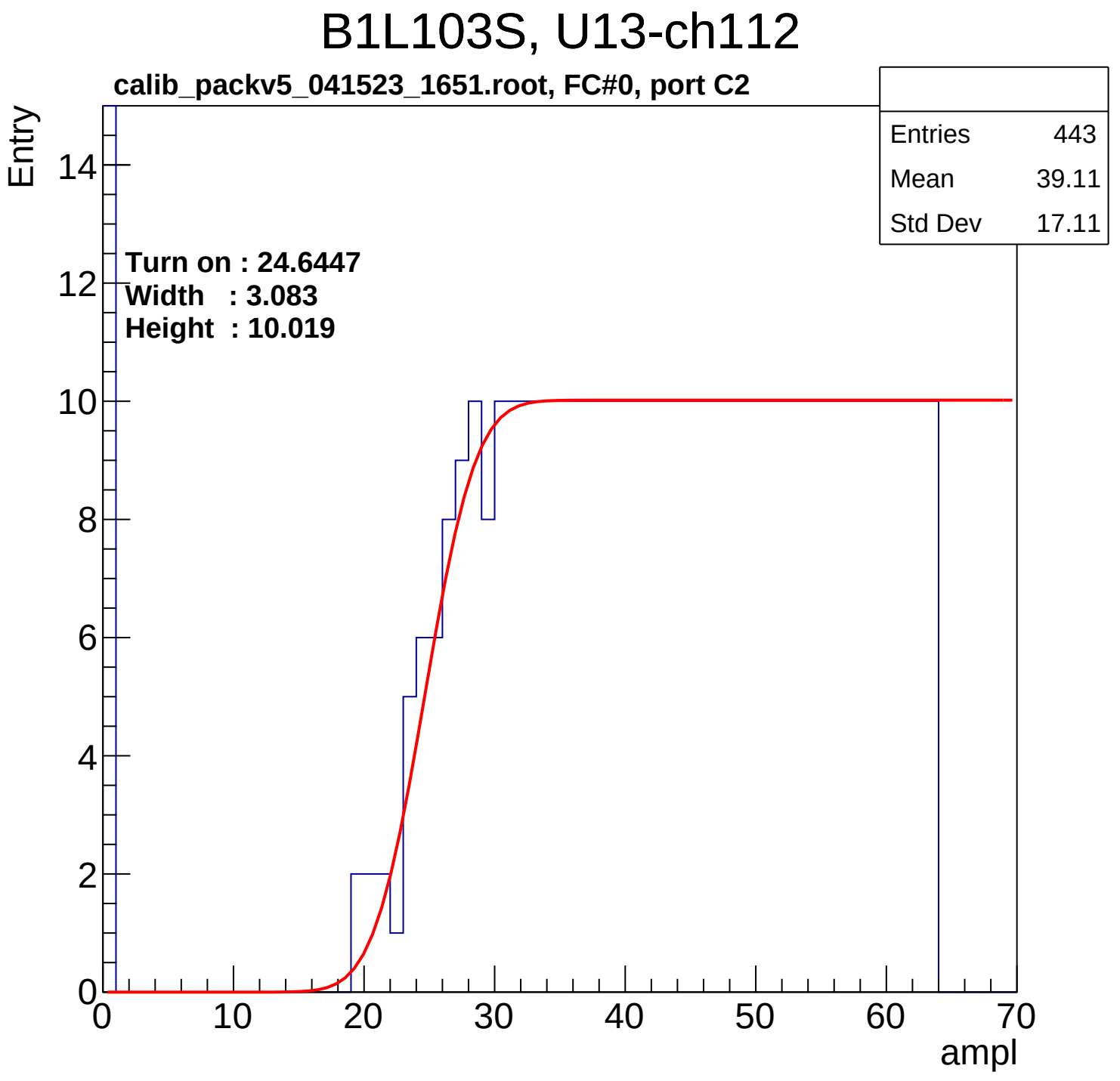
B1L103S, U13-ch112
calib_packv5_041523_1651.root, FC#0, port C2
Entries 443
Mean 39.11
Std Dev 17.11
Turn on : 24.6447
Width : 3.083
Height : 10.019
Entry
ampl
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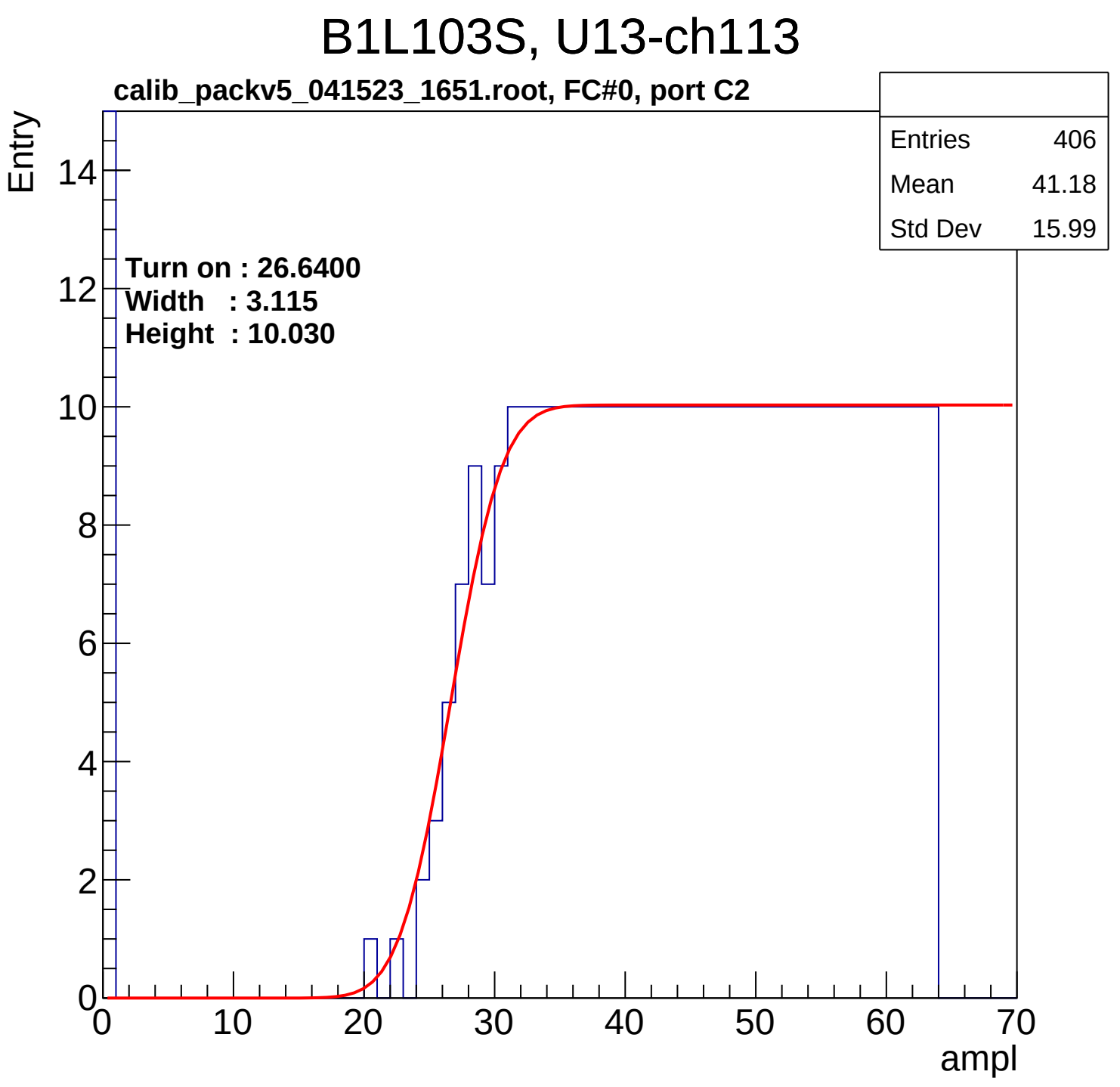
B1L103S, U13-ch113
calib_packv5_041523_1651.root, FC#0, port C2
Entries 406
Mean 41.18
Std Dev 15.99
Turn on : 26.6400
Width : 3.115
Height : 10.030
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ampl
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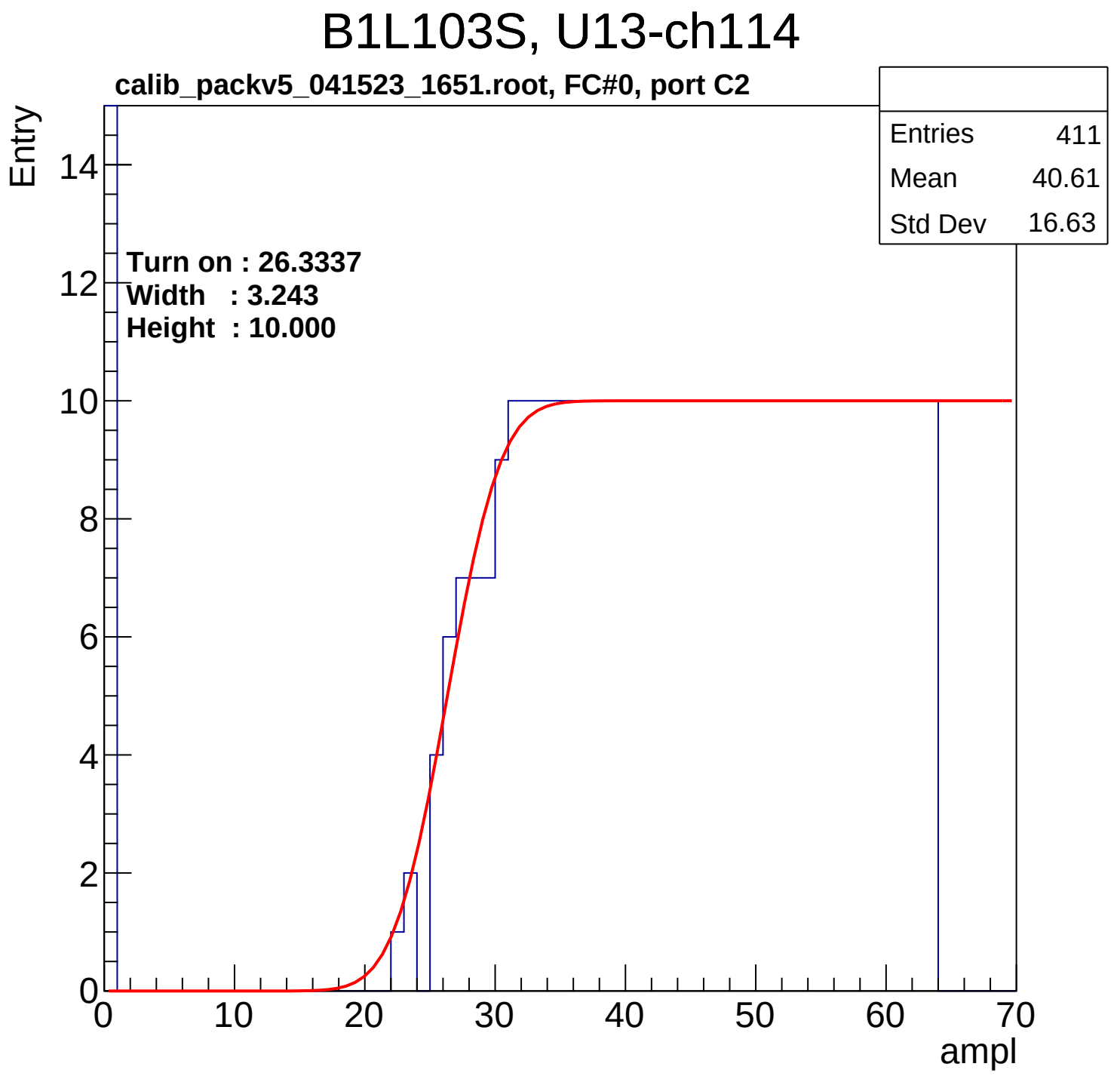
B1L103S, U13-ch114
calib_packv5_041523_1651.root, FC#0, port C2
Entries 411
Mean 40.61
Std Dev 16.63
Turn on : 26.3337
Width : 3.243
Height : 10.000
Entry
ampl
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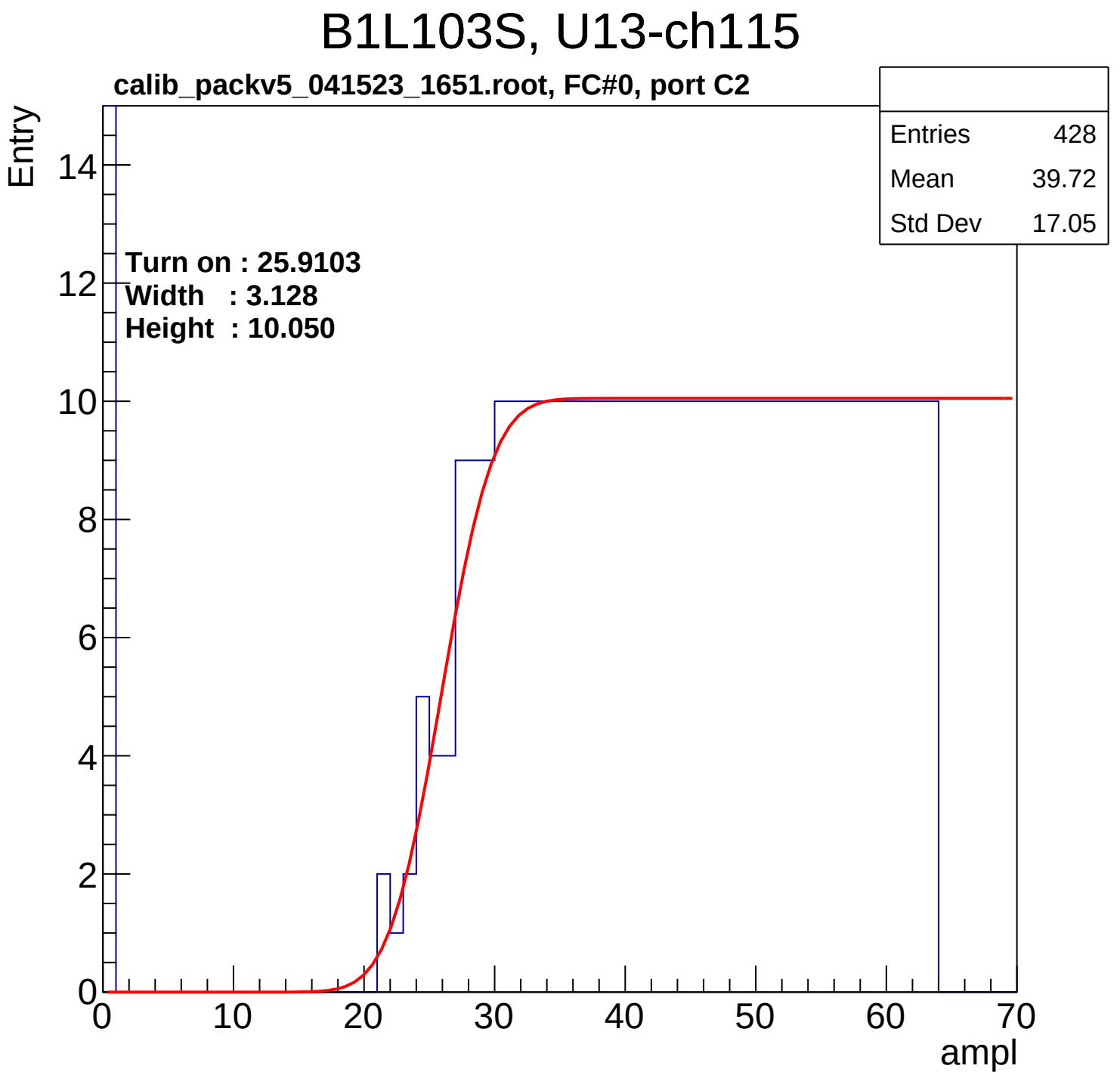
B1L103S, U13-ch115
calib_packv5_041523_1651.root, FC#0, port C2
Entries 428
Mean 39.72
Std Dev 17.05
Turn on : 25.9103
Width : 3.128
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
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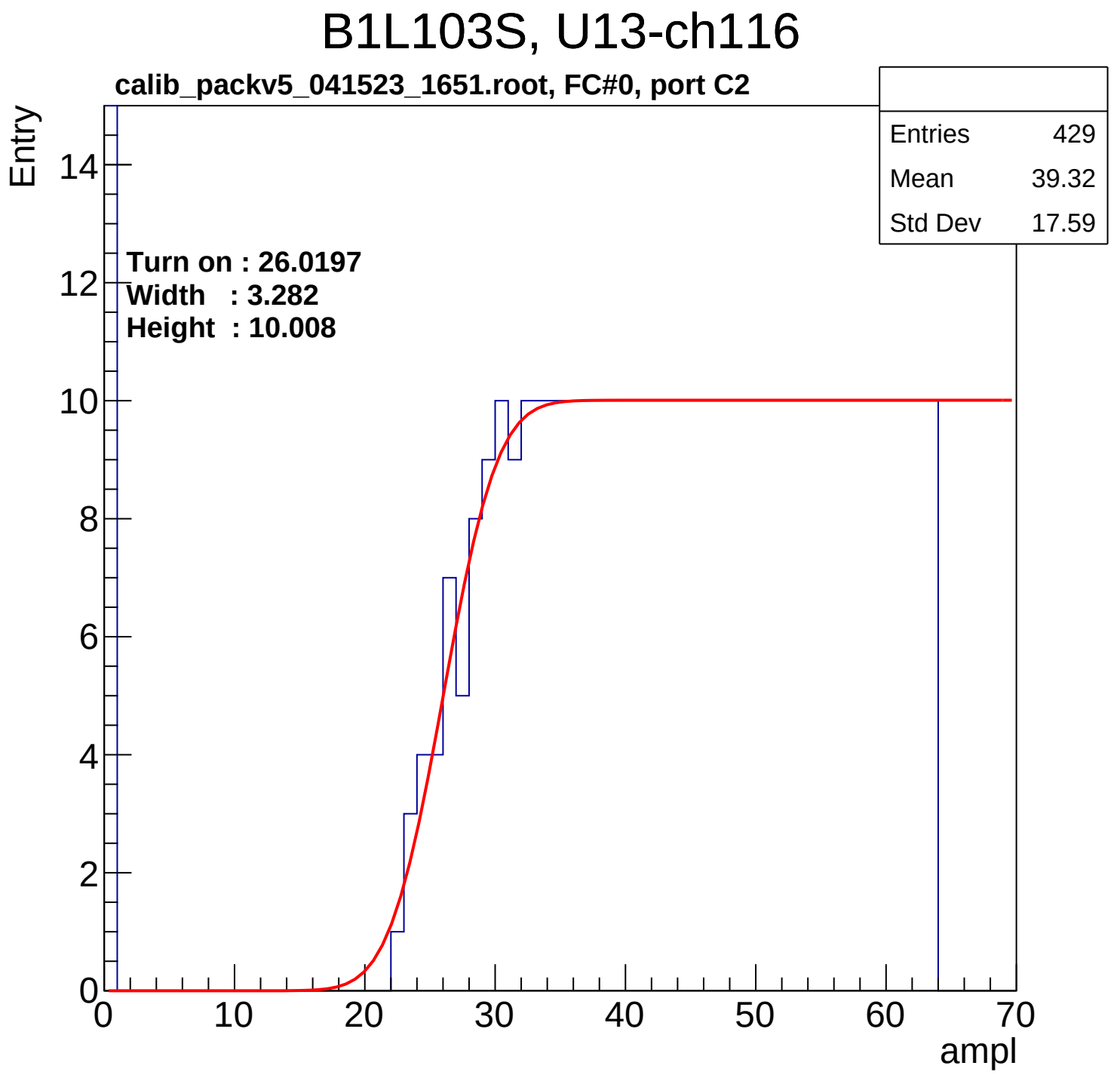
B1L103S, U13-ch116
calib_packv5_041523_1651.root, FC#0, port C2
Entries 429
Mean 39.32
Std Dev 17.59
Turn on : 26.0197
Width : 3.282
Height : 10.008
Entry
ampl
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2
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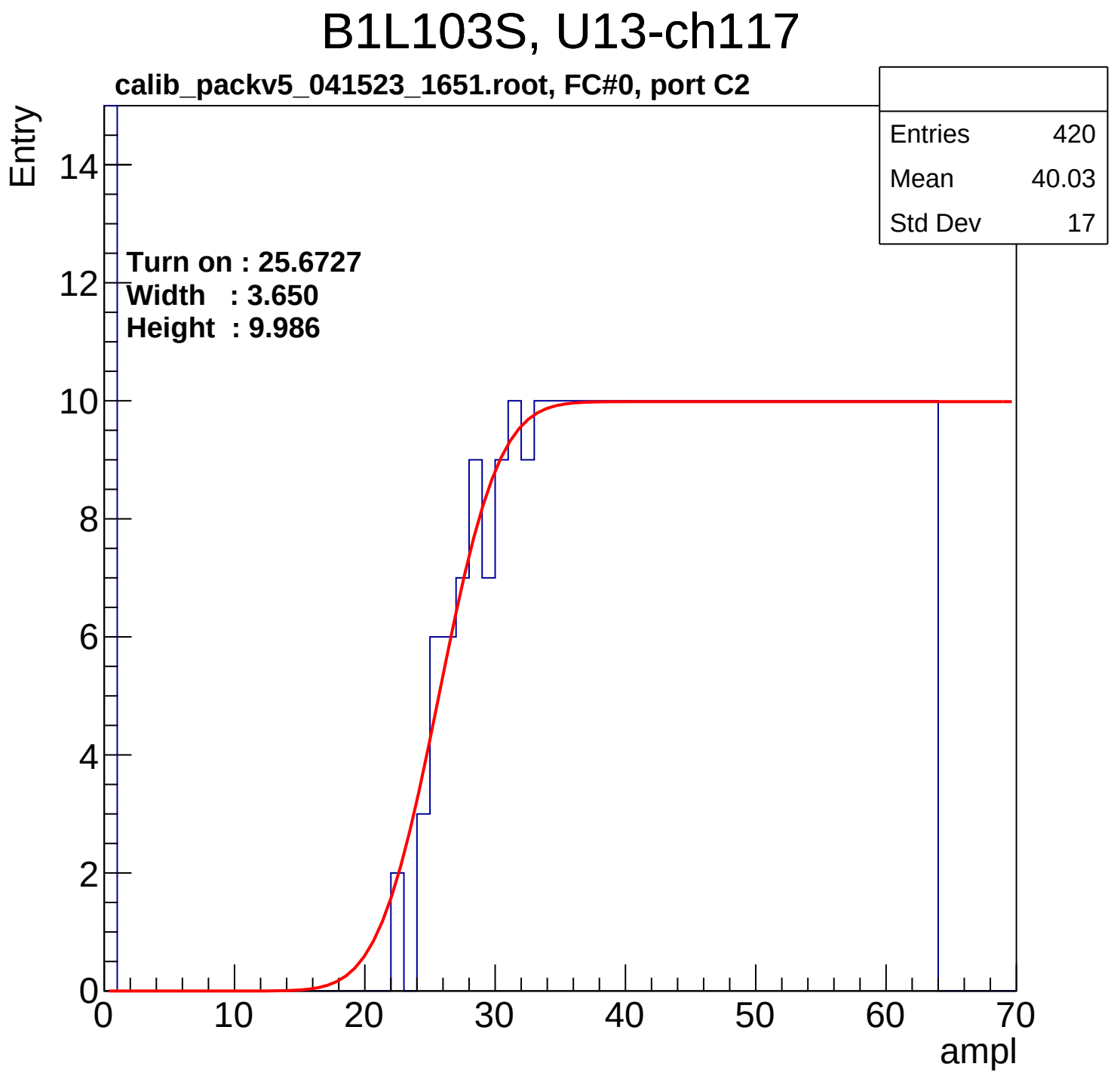
B1L103S, U13-ch117
calib_packv5_041523_1651.root, FC#0, port C2
Entries 420
Mean 40.03
Std Dev 17
Turn on : 25.6727
Width : 3.650
Height : 9.986
Entry
ampl
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2
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6
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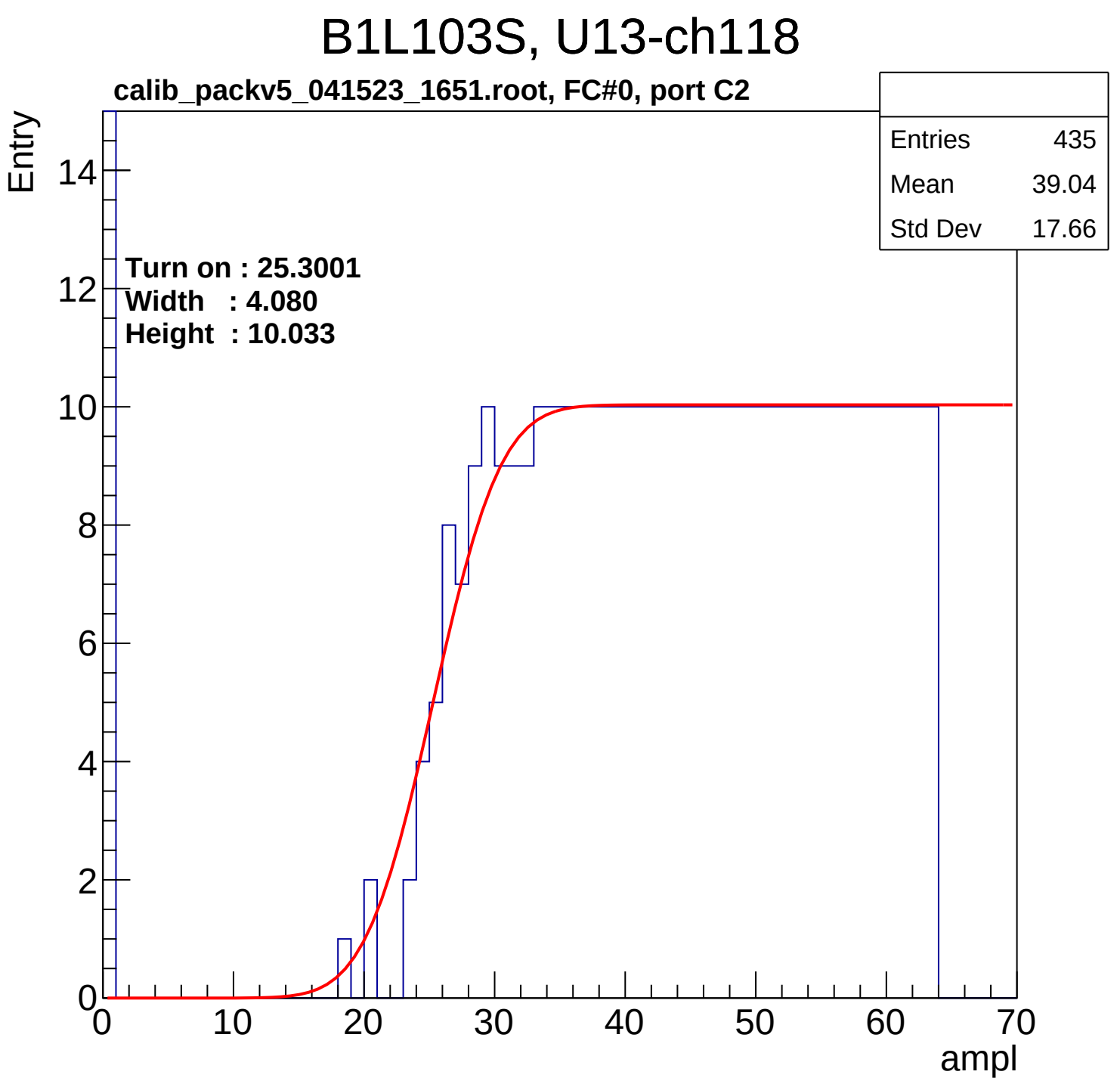
B1L103S, U13-ch118
calib_packv5_041523_1651.root, FC#0, port C2
Entries 435
Mean 39.04
Std Dev 17.66
Turn on : 25.3001
Width : 4.080
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
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0
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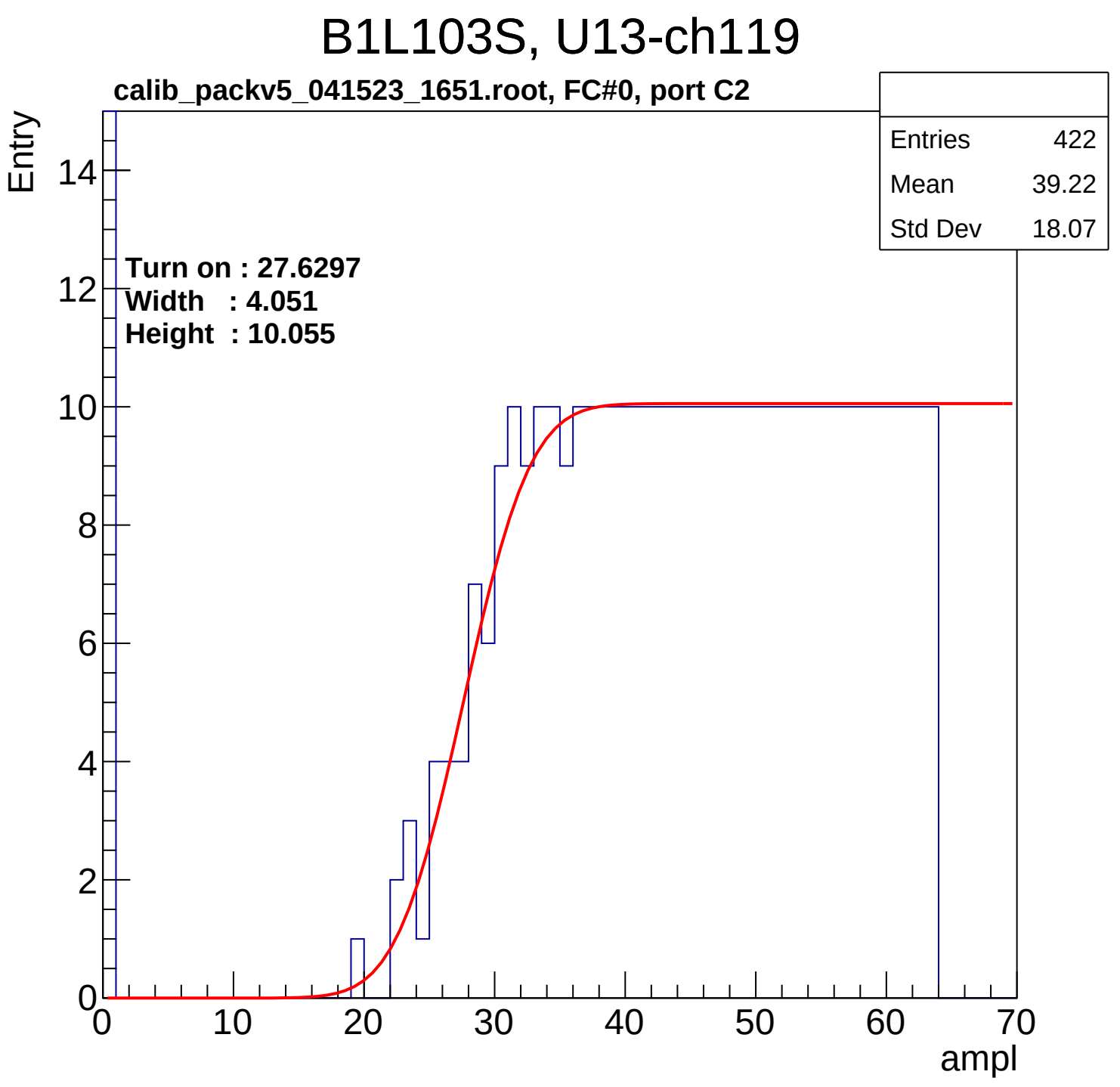
B1L103S, U13-ch119
calib_packv5_041523_1651.root, FC#0, port C2
Entries 422
Mean 39.22
Std Dev 18.07
Turn on : 27.6297
Width : 4.051
Height : 10.055
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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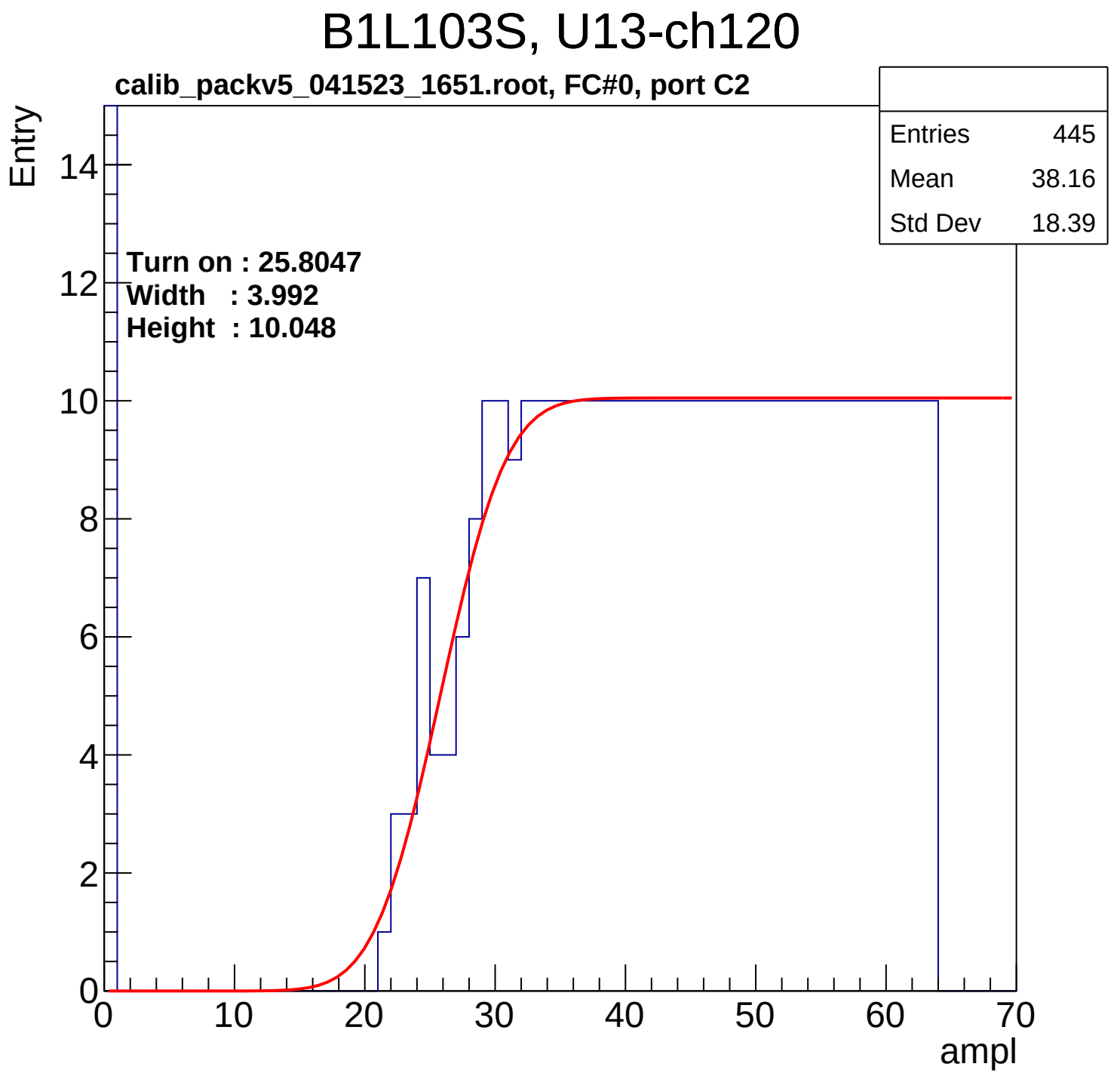
B1L103S, U13-ch120
calib_packv5_041523_1651.root, FC#0, port C2
Entries 445
Mean 38.16
Std Dev 18.39
Turn on : 25.8047
Width : 3.992
Height : 10.048
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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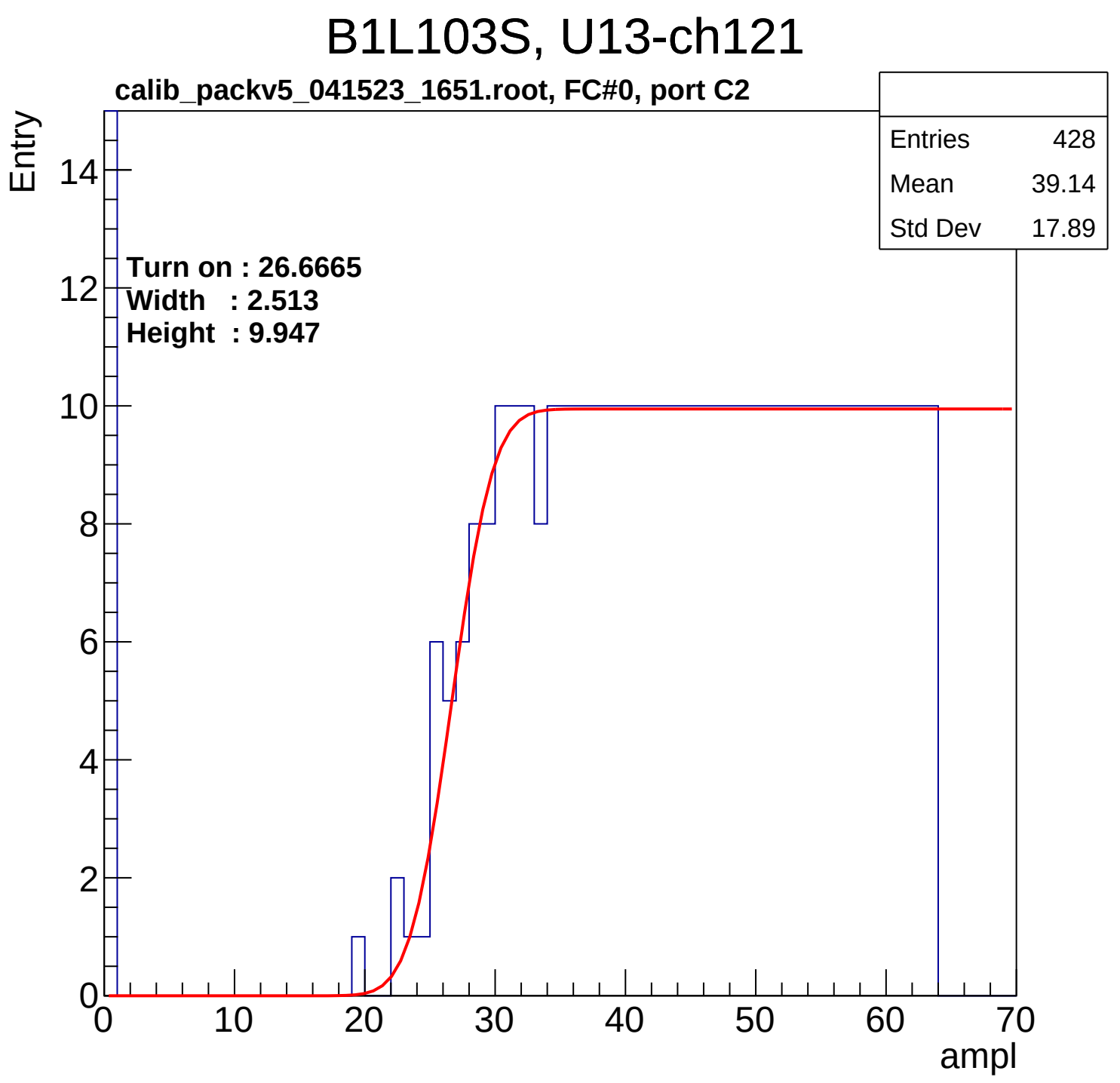
B1L103S, U13-ch121
calib_packv5_041523_1651.root, FC#0, port C2
Entries 428
Mean 39.14
Std Dev 17.89
Turn on : 26.6665
Width : 2.513
Height : 9.947
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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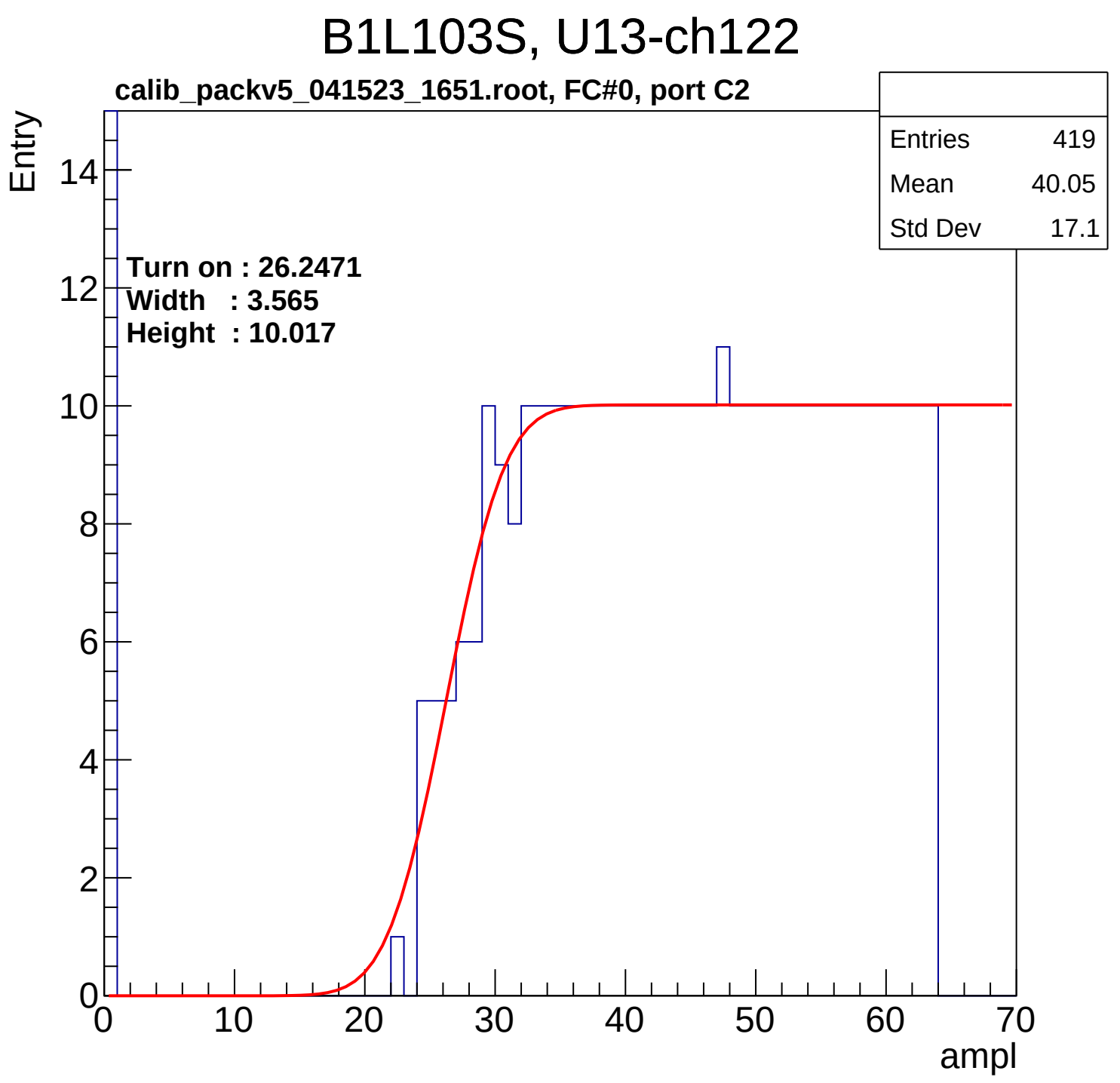
B1L103S, U13-ch122
calib_packv5_041523_1651.root, FC#0, port C2
Entries 419
Mean 40.05
Std Dev 17.1
Turn on : 26.2471
Width : 3.565
Height : 10.017
Entry
ampl
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2
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6
8
10
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10
20
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60
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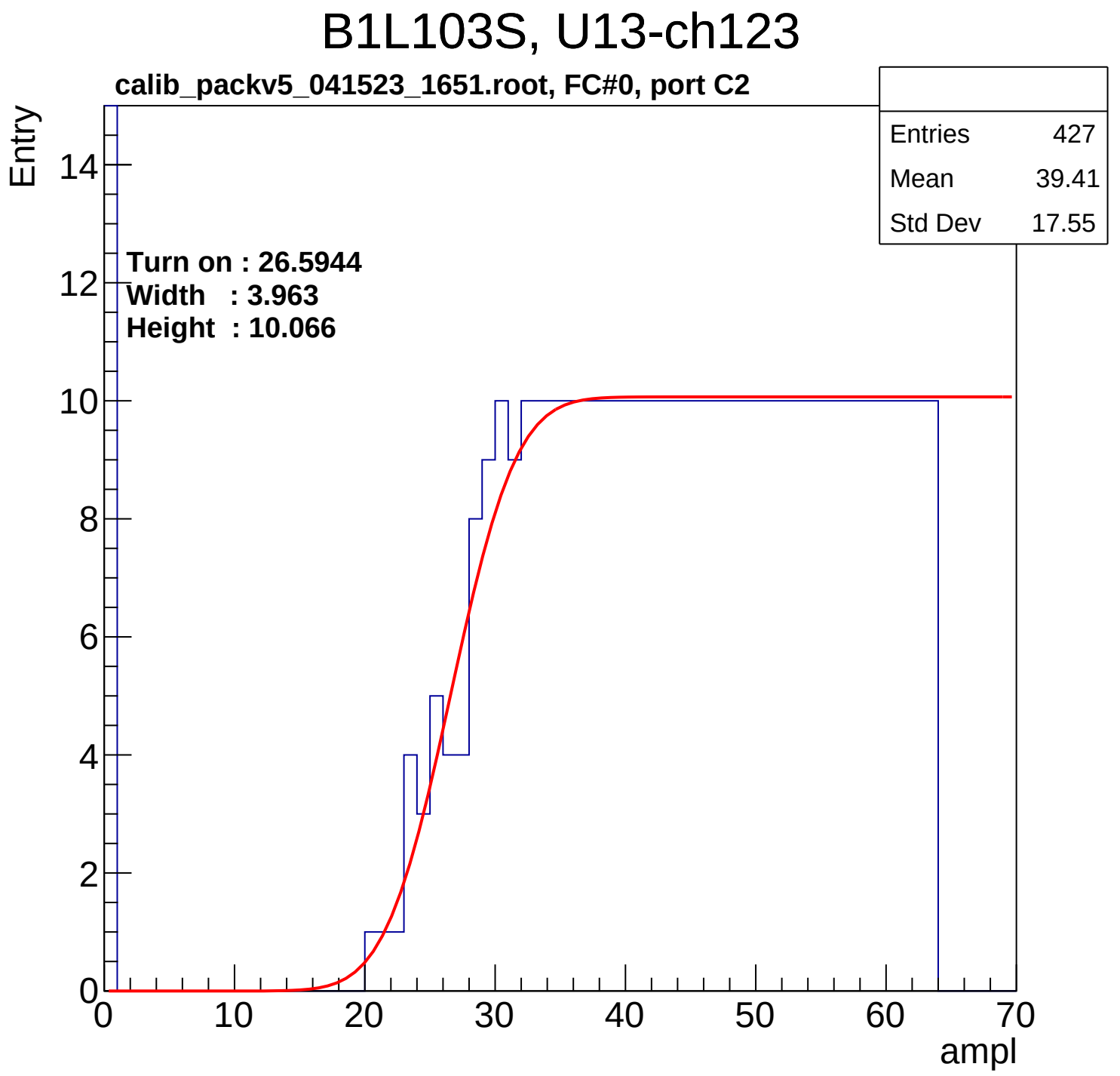
B1L103S, U13-ch123
calib_packv5_041523_1651.root, FC#0, port C2
Entries 427
Mean 39.41
Std Dev 17.55
Turn on : 26.5944
Width : 3.963
Height : 10.066
Entry
ampl
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4
6
8
10
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14
0
10
20
30
40
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60
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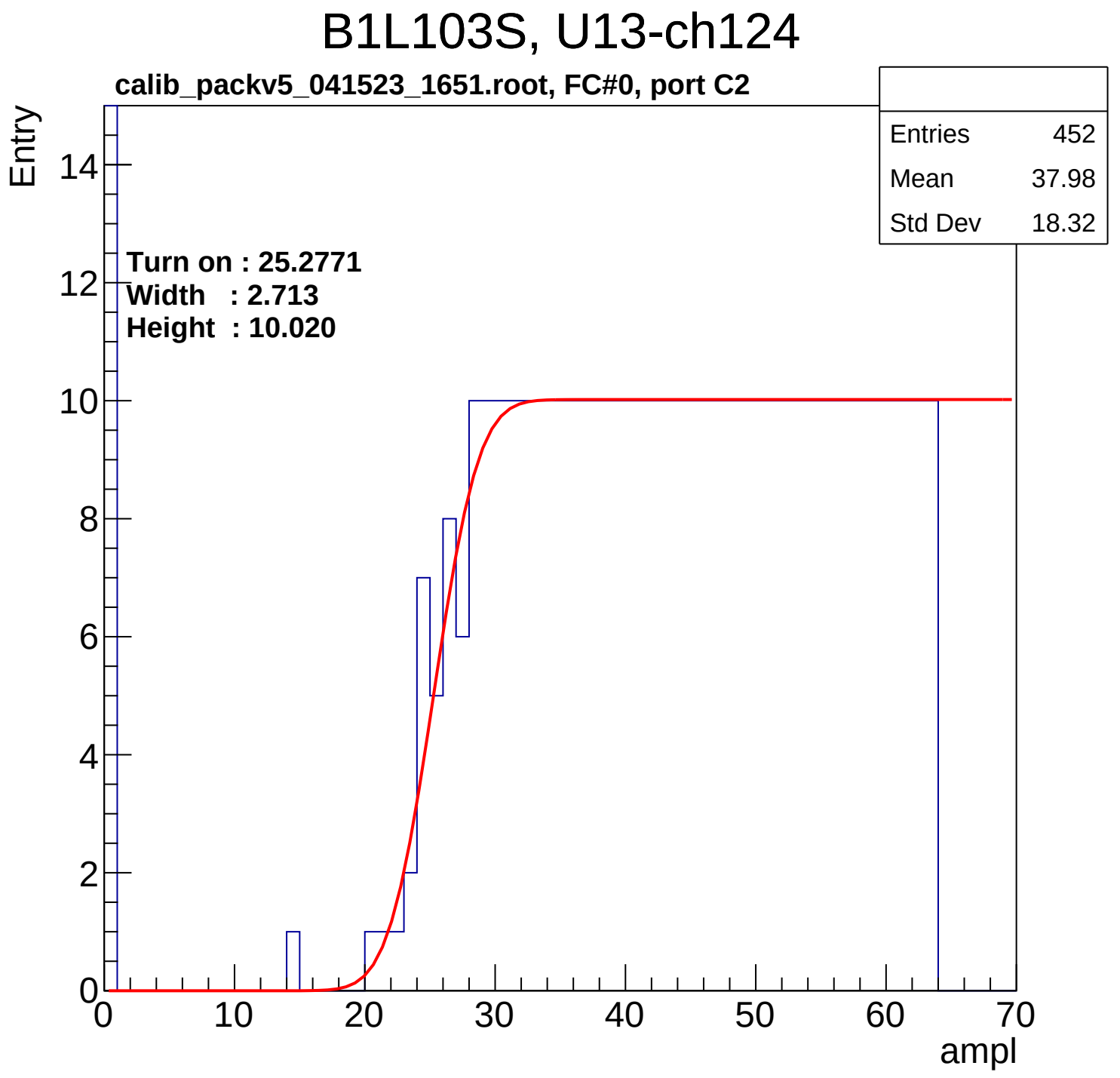
B1L103S, U13-ch124
calib_packv5_041523_1651.root, FC#0, port C2
Entries 452
Mean 37.98
Std Dev 18.32
Turn on : 25.2771
Width : 2.713
Height : 10.020
Entry
ampl
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6
8
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14
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10
20
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40
50
60
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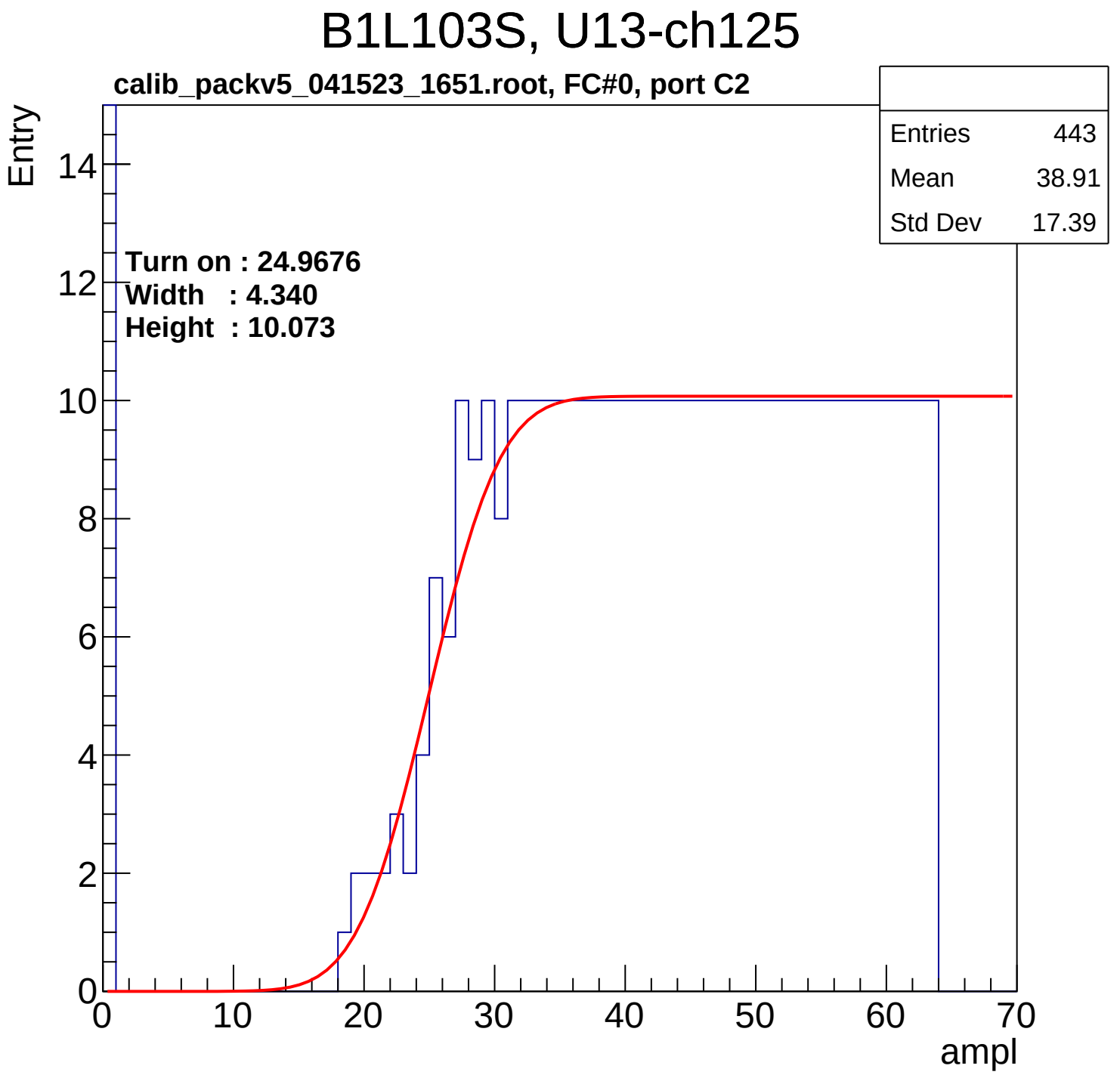
B1L103S, U13-ch125
calib_packv5_041523_1651.root, FC#0, port C2
Entries 443
Mean 38.91
Std Dev 17.39
Turn on : 24.9676
Width : 4.340
Height : 10.073
Entry
ampl
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2
4
6
8
10
12
14
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10
20
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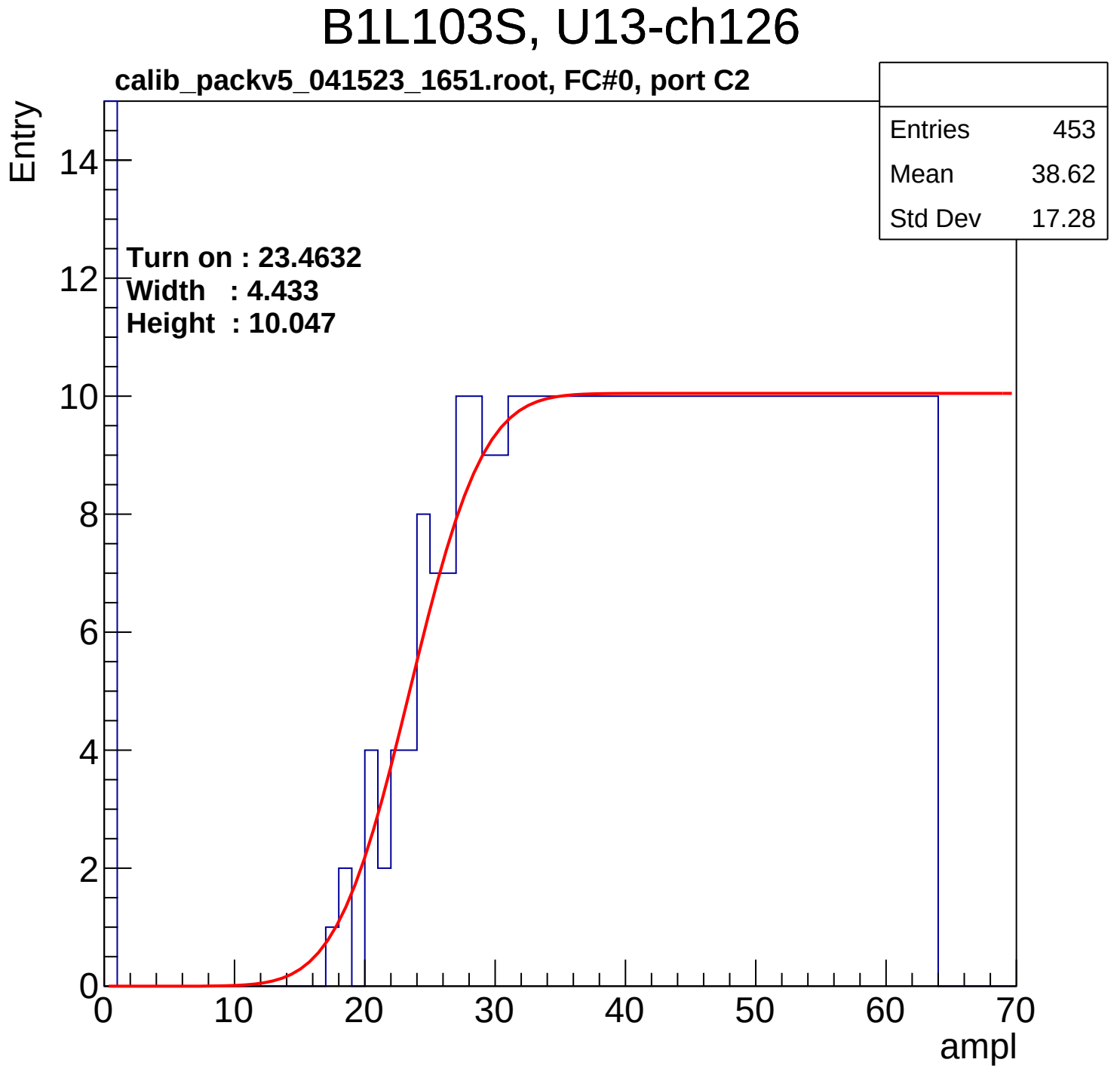
40
50
60
70


B1L103S, U13-ch126
calib_packv5_041523_1651.root, FC#0, port C2
Entries 453
Mean 38.62
Std Dev 17.28
Turn on : 23.4632
Width : 4.433
Height : 10.047
Entry
ampl
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4
6
8
10
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0
10
20
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40
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60
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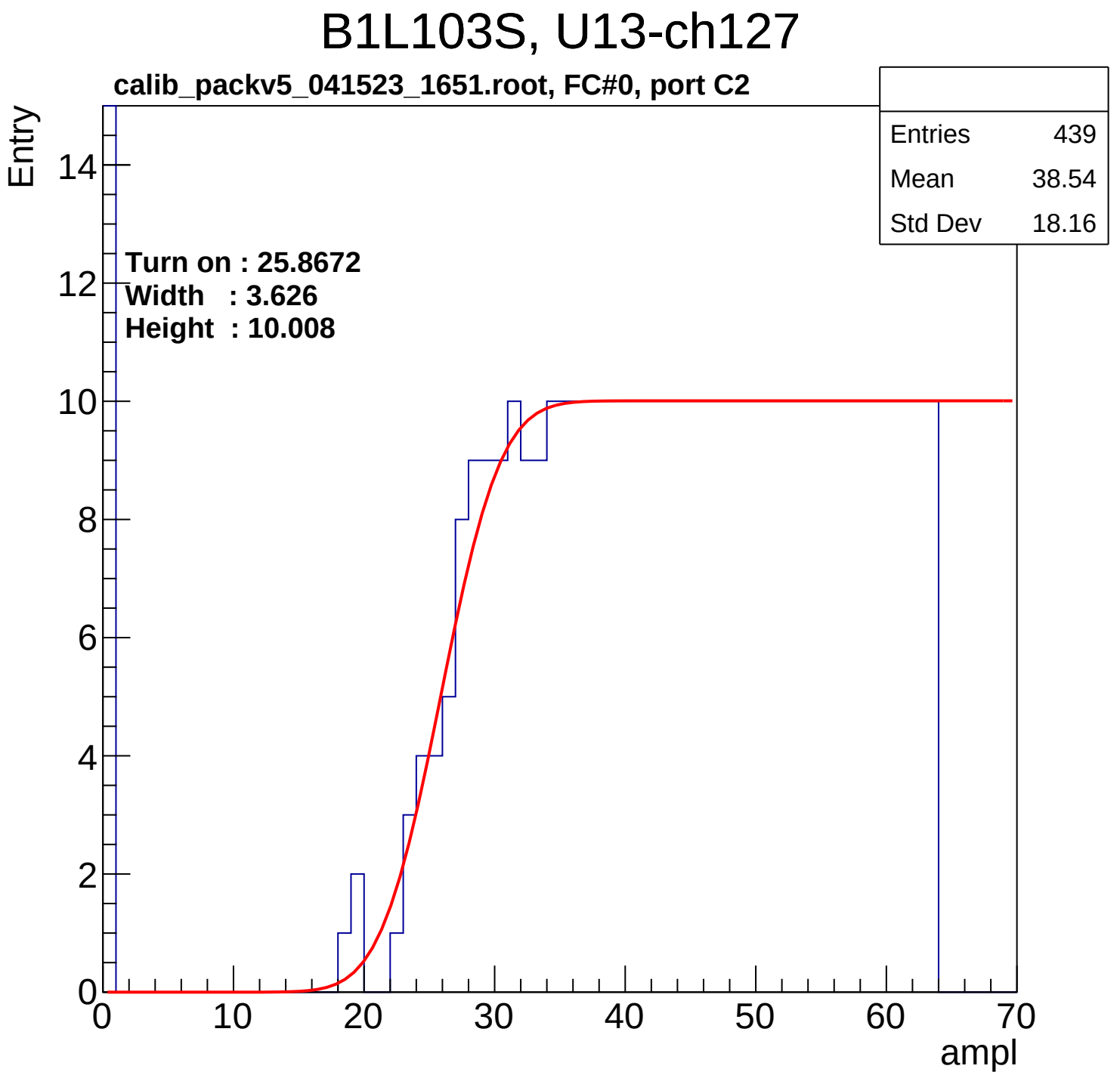
B1L103S, U13-ch127
calib_packv5_041523_1651.root, FC#0, port C2
Entries 439
Mean 38.54
Std Dev 18.16
Turn on : 25.8672
Width : 3.626
Height : 10.008
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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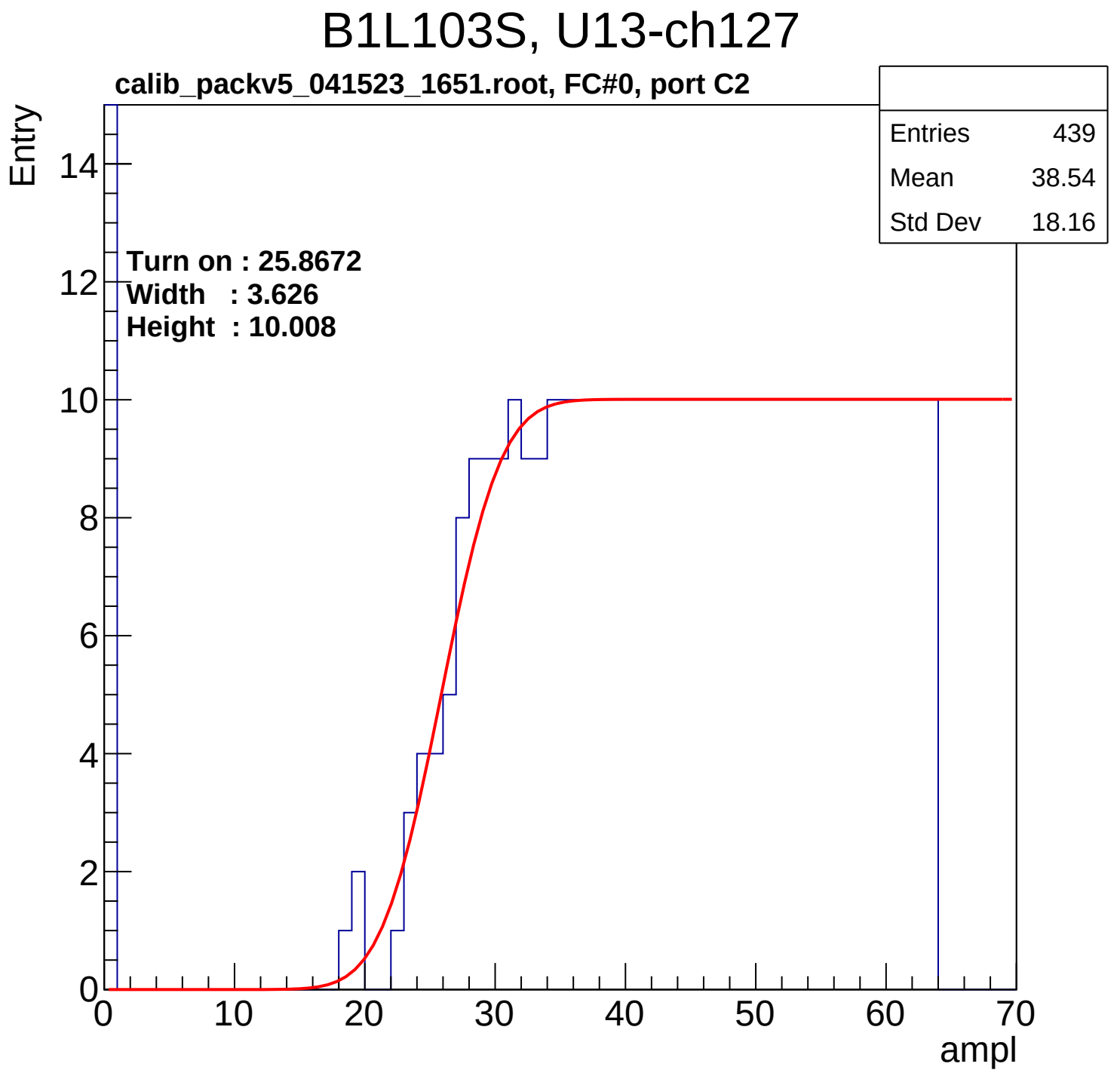
B1L103S, U13-ch127
calib_packv5_041523_1651.root, FC#0, port C2
Entries 439
Mean 38.54
Std Dev 18.16
Turn on : 25.8672
Width : 3.626
Height : 10.008
Entry
ampl
0
2
4
6
8
10
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14
0
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20
30
40
50
60
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