

B1L003S, U1-ch0

calib_packv5_042523_0143.root, FC#13, port D2

Entries	374
Mean	44.51
Std Dev	11.53

Turn on : 27.4891

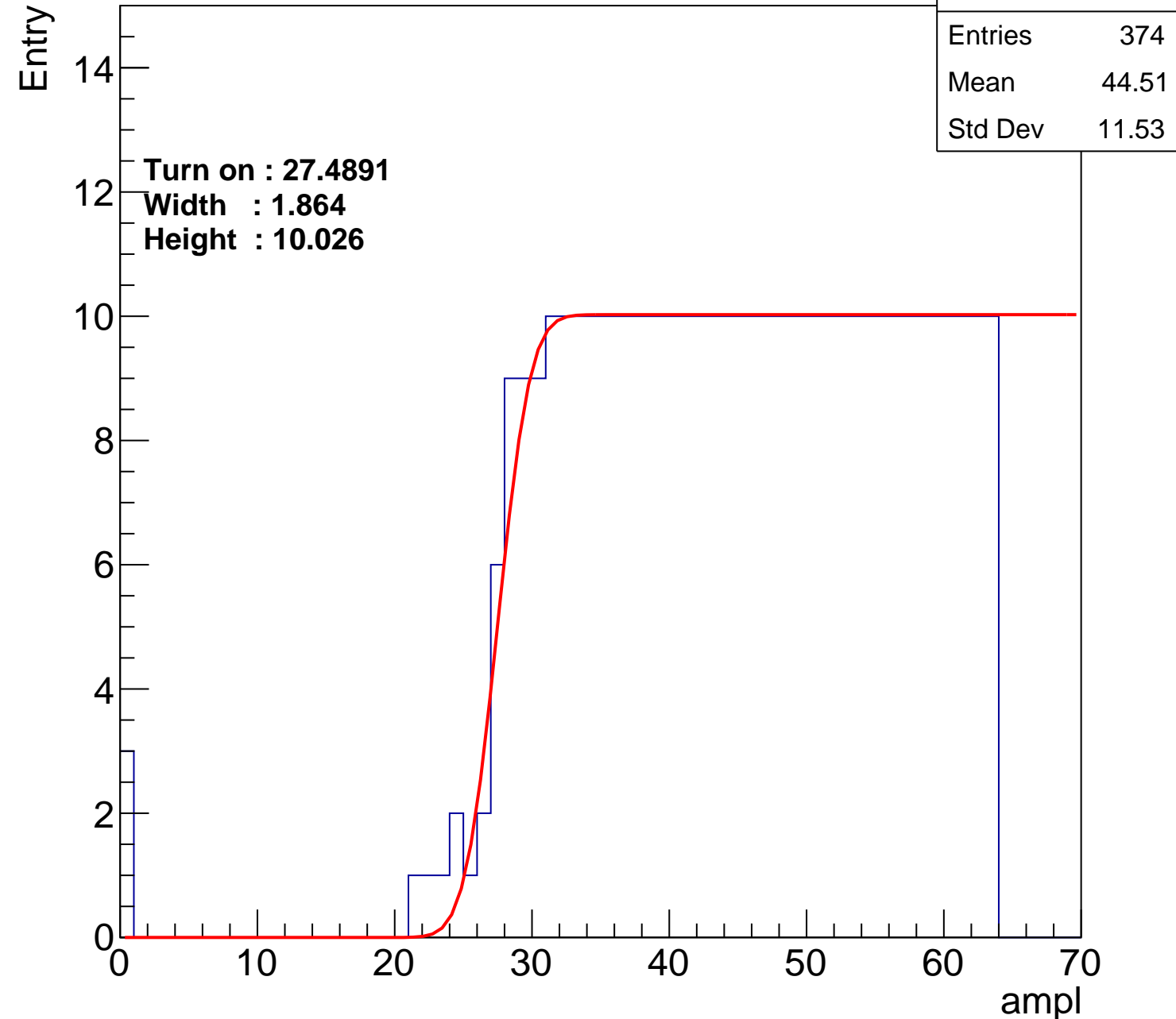
Width : 1.864

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch1

calib_packv5_042523_0143.root, FC#13, port D2

Entries	372
Mean	44.56
Std Dev	11.55

Turn on : 27.4591

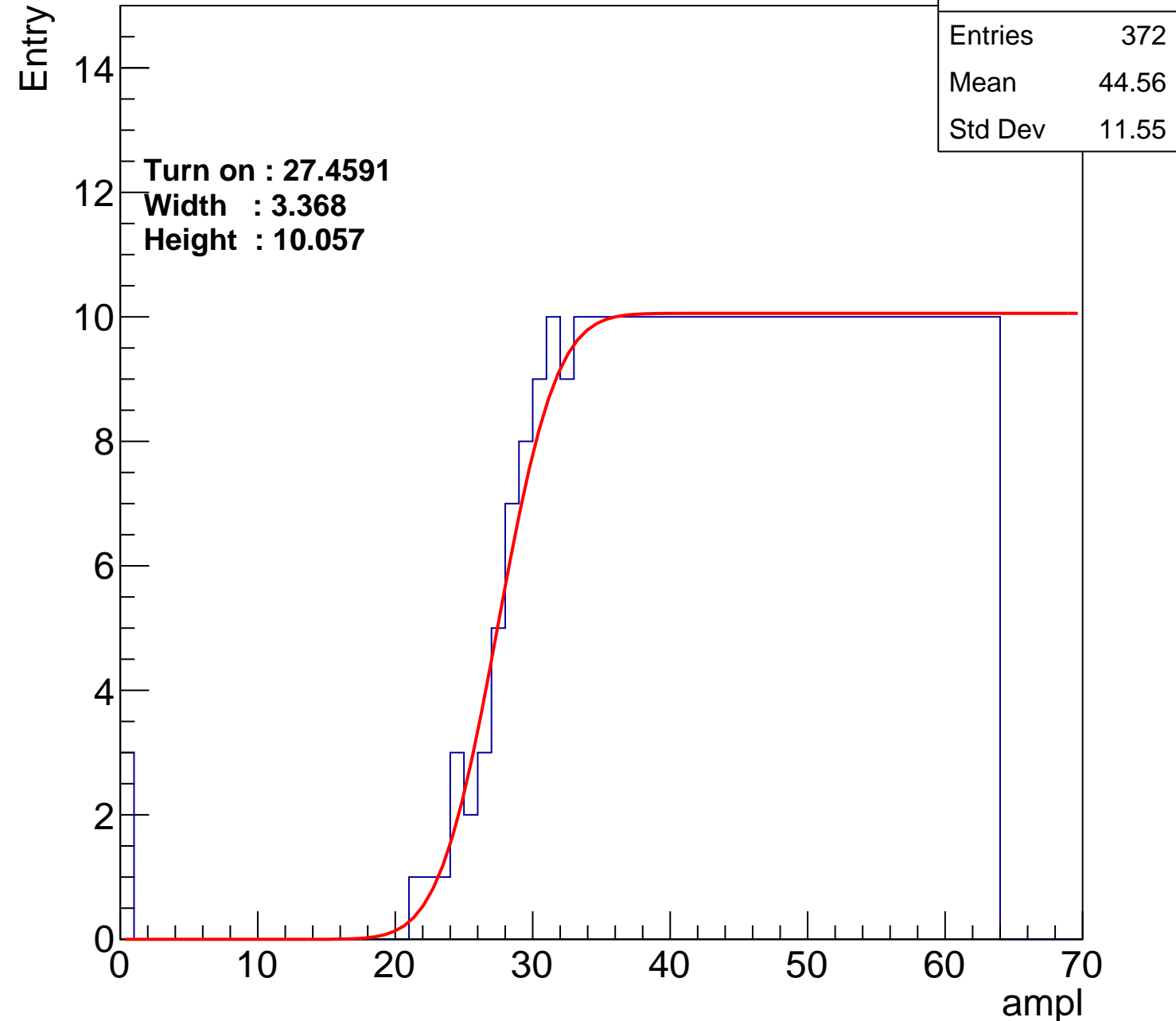
Width : 3.368

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch2

calib_packv5_042523_0143.root, FC#13, port D2

Entries	389
Mean	43.82
Std Dev	11.74

Turn on : 25.6547

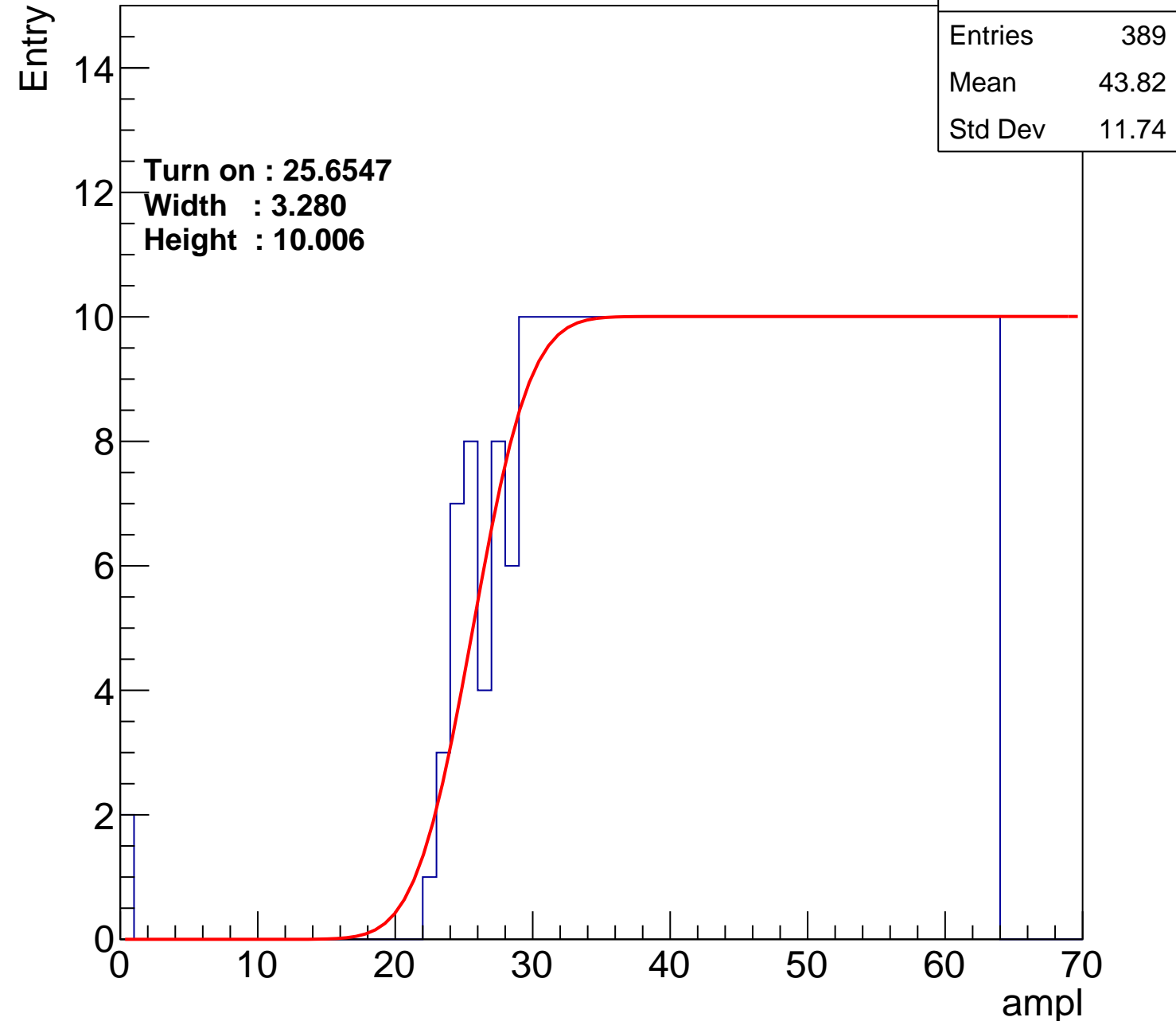
Width : 3.280

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch3

calib_packv5_042523_0143.root, FC#13, port D2

Entries	352
Mean	45.39
Std Dev	11.49

Turn on : 29.9031

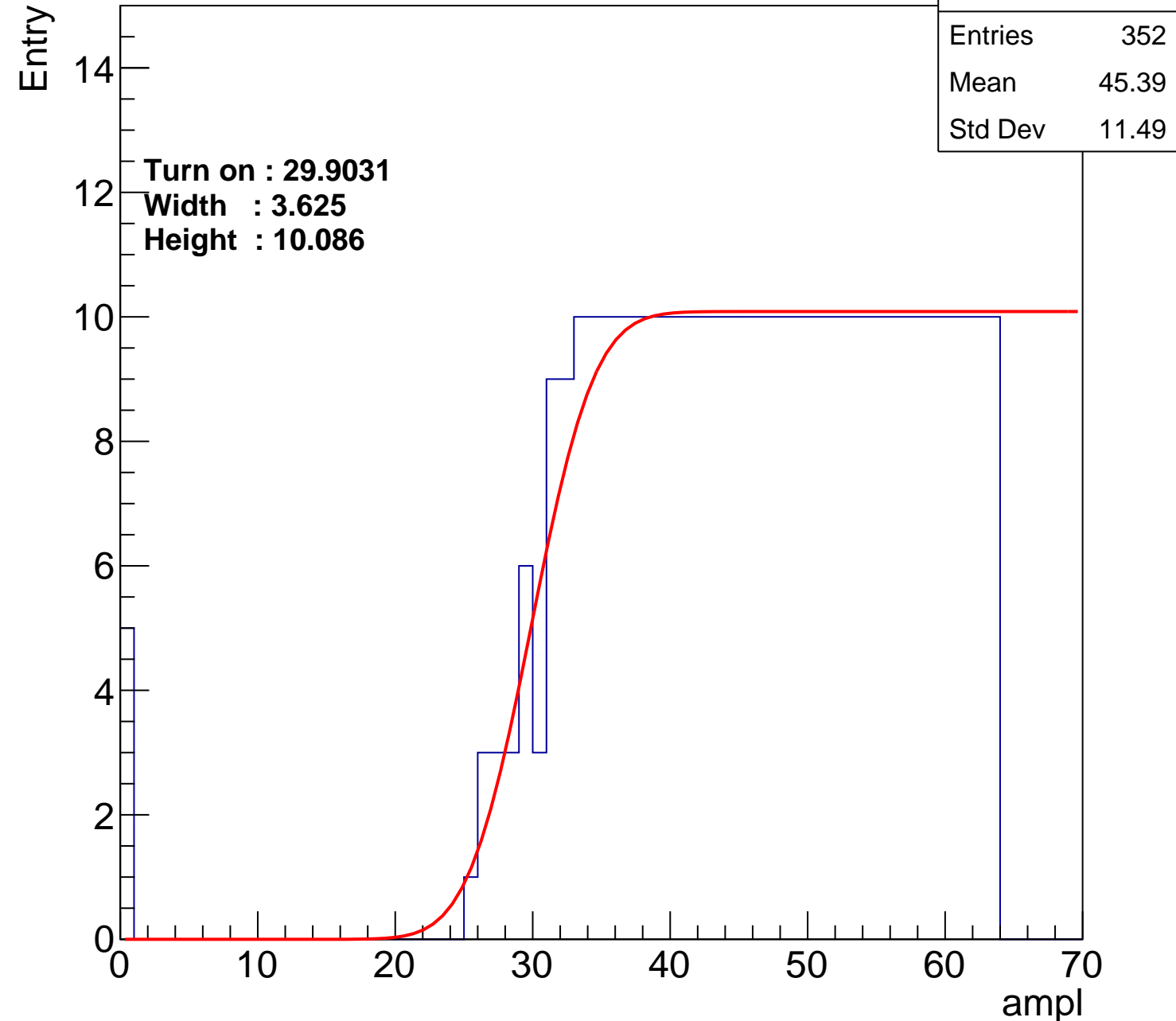
Width : 3.625

Height : 10.086

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch4

calib_packv5_042523_0143.root, FC#13, port D2

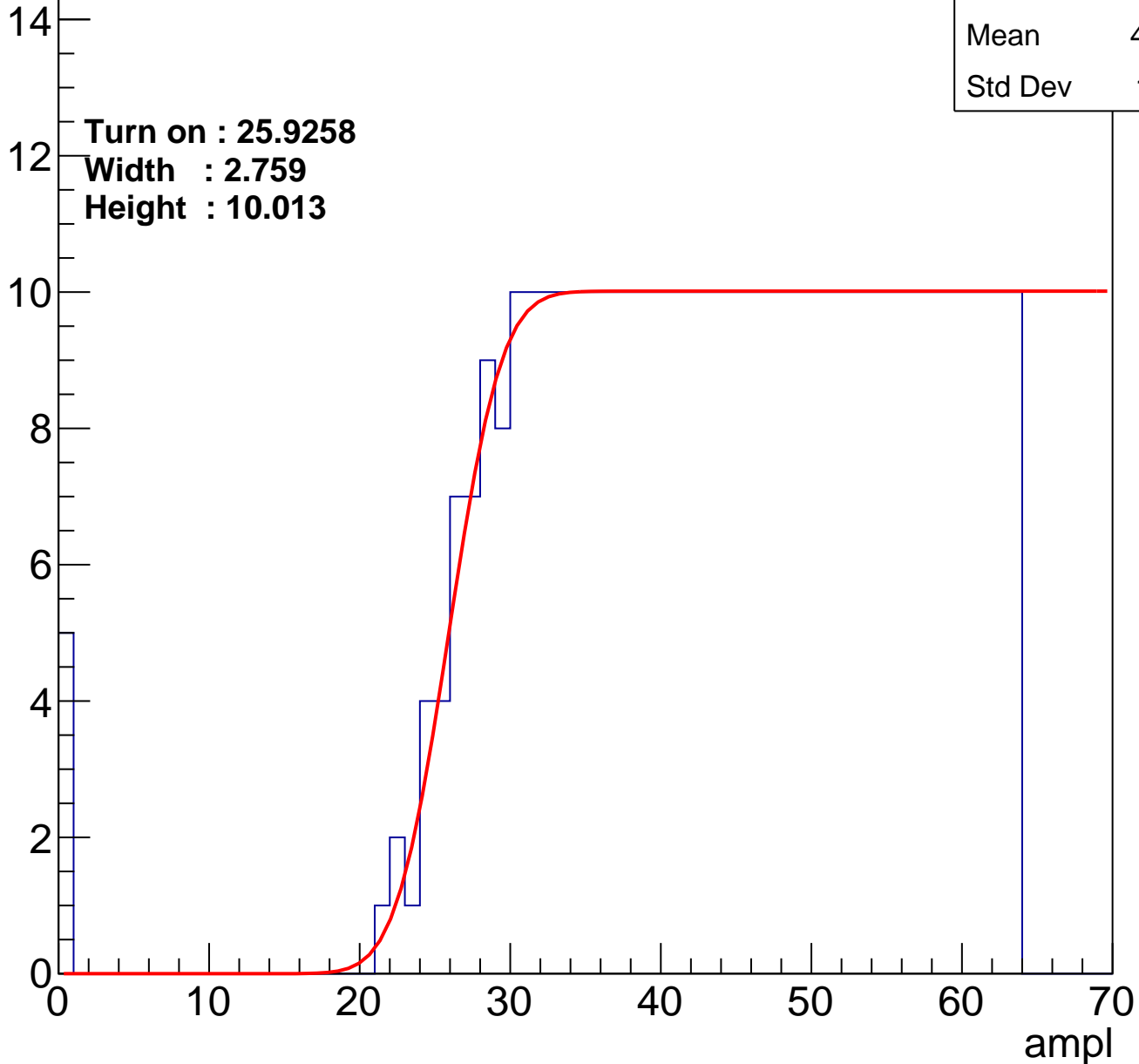
Entries	388
Mean	43.68
Std Dev	12.21

Turn on : 25.9258

Width : 2.759

Height : 10.013

Entry



B1L003S, U1-ch5

calib_packv5_042523_0143.root, FC#13, port D2

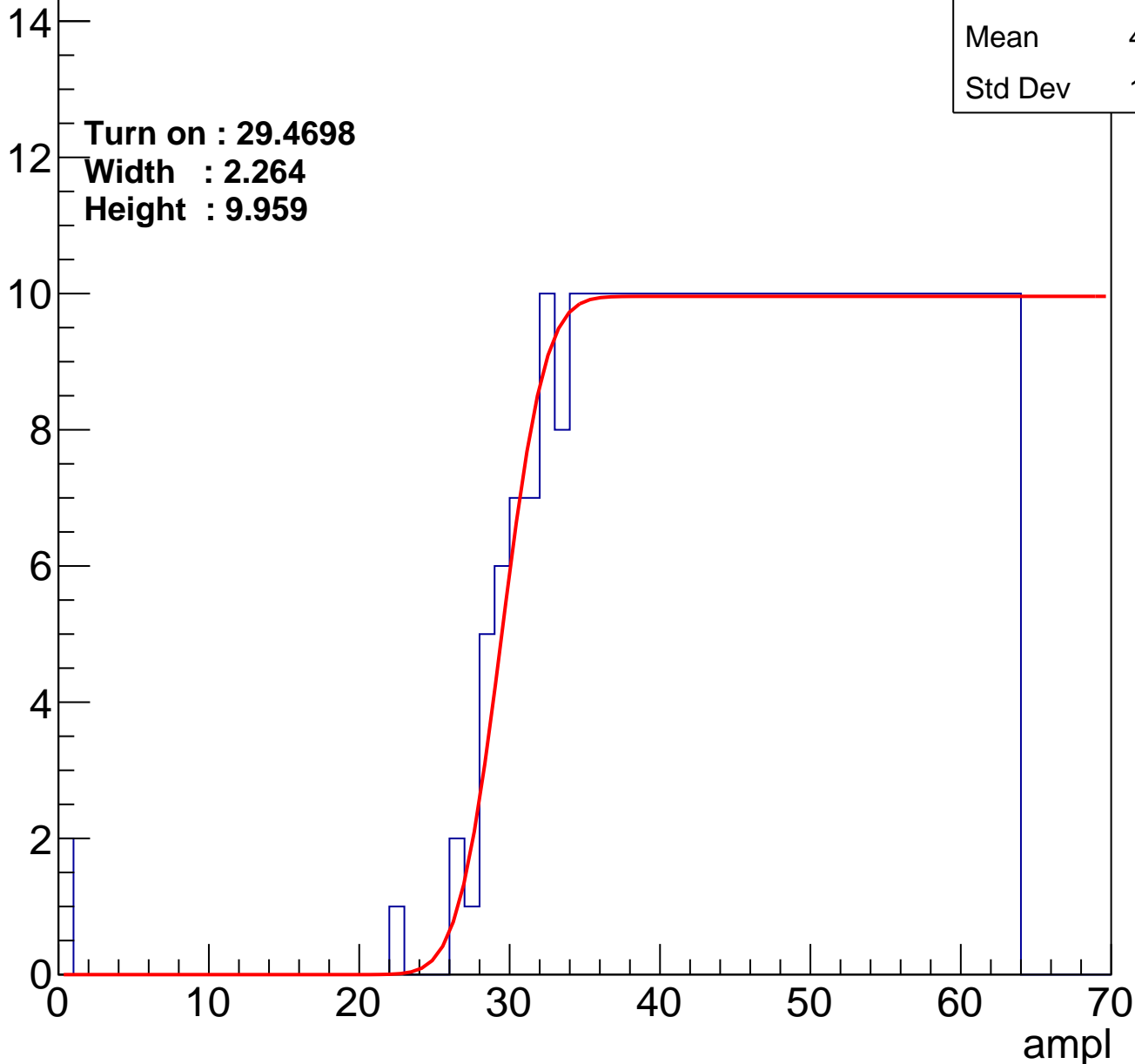
Entry

Entries	349
Mean	45.78
Std Dev	10.75

Turn on : 29.4698

Width : 2.264

Height : 9.959



B1L003S, U1-ch6

calib_packv5_042523_0143.root, FC#13, port D2

Entries	359
Mean	45.31
Std Dev	10.97

Turn on : 28.6698

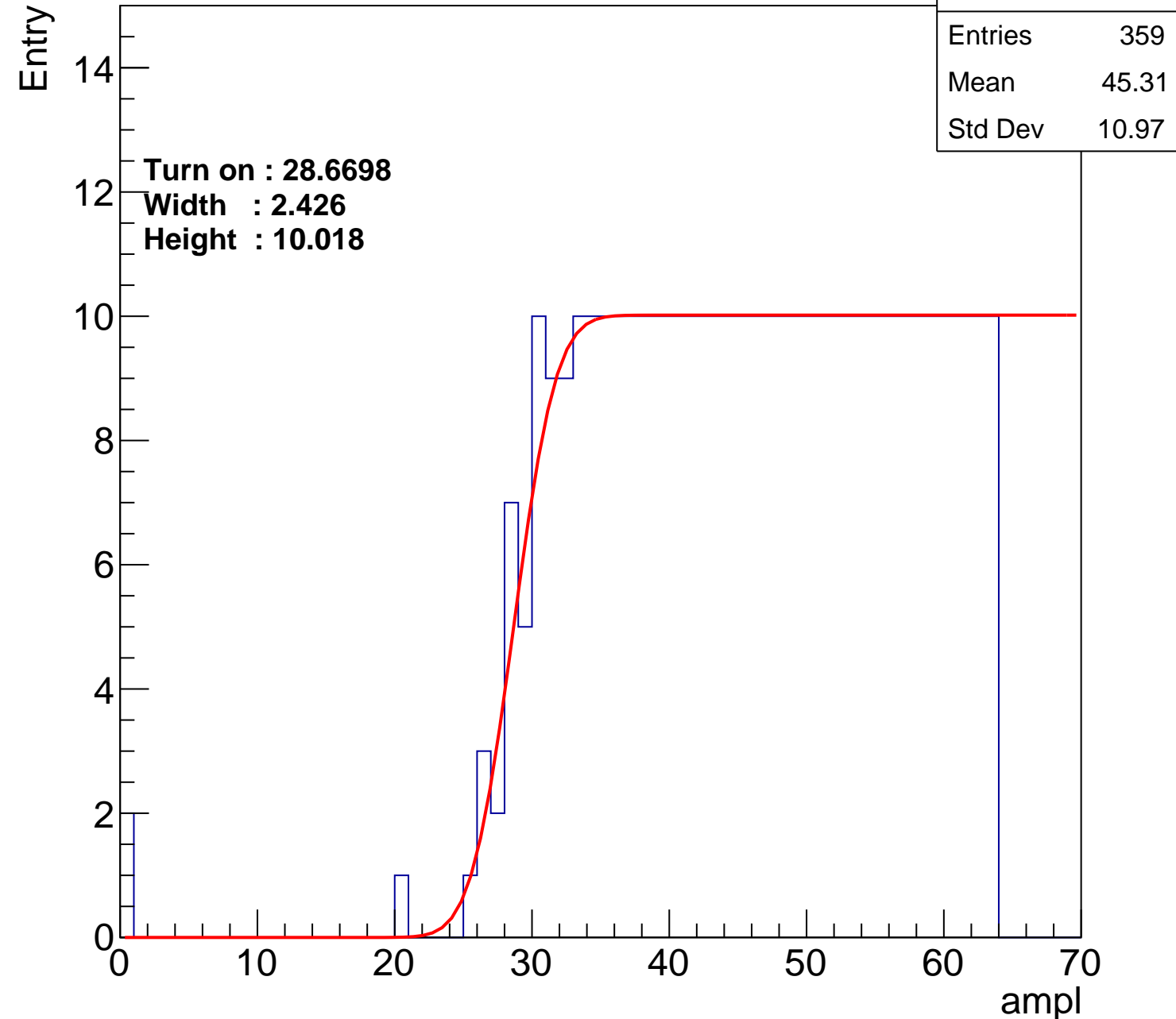
Width : 2.426

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch7

calib_packv5_042523_0143.root, FC#13, port D2

Entries	375
Mean	44.53
Std Dev	11.36

Turn on : 26.7458

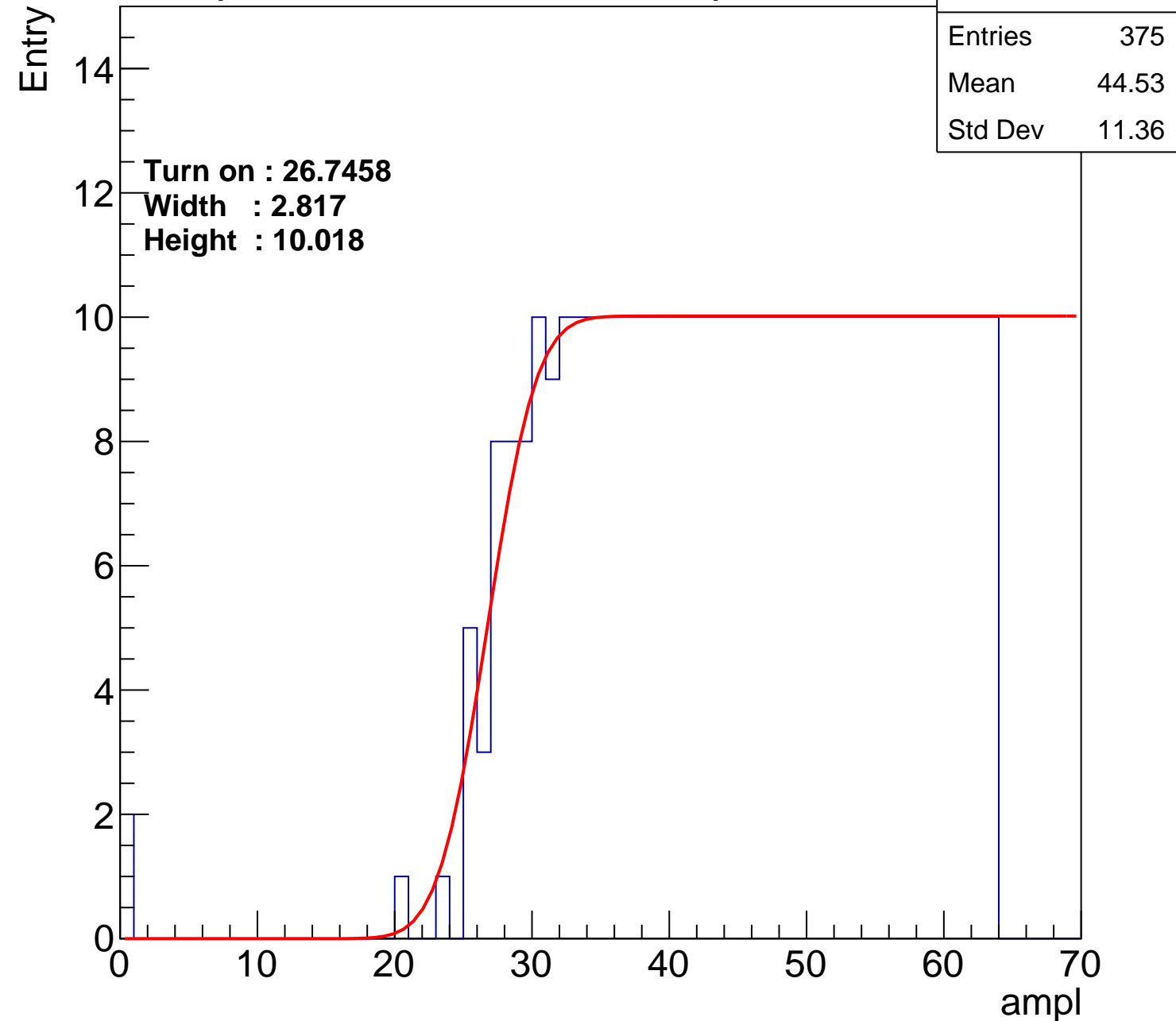
Width : 2.817

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch8

calib_packv5_042523_0143.root, FC#13, port D2

Entries	389
Mean	43.8
Std Dev	11.78

Turn on : 25.4312

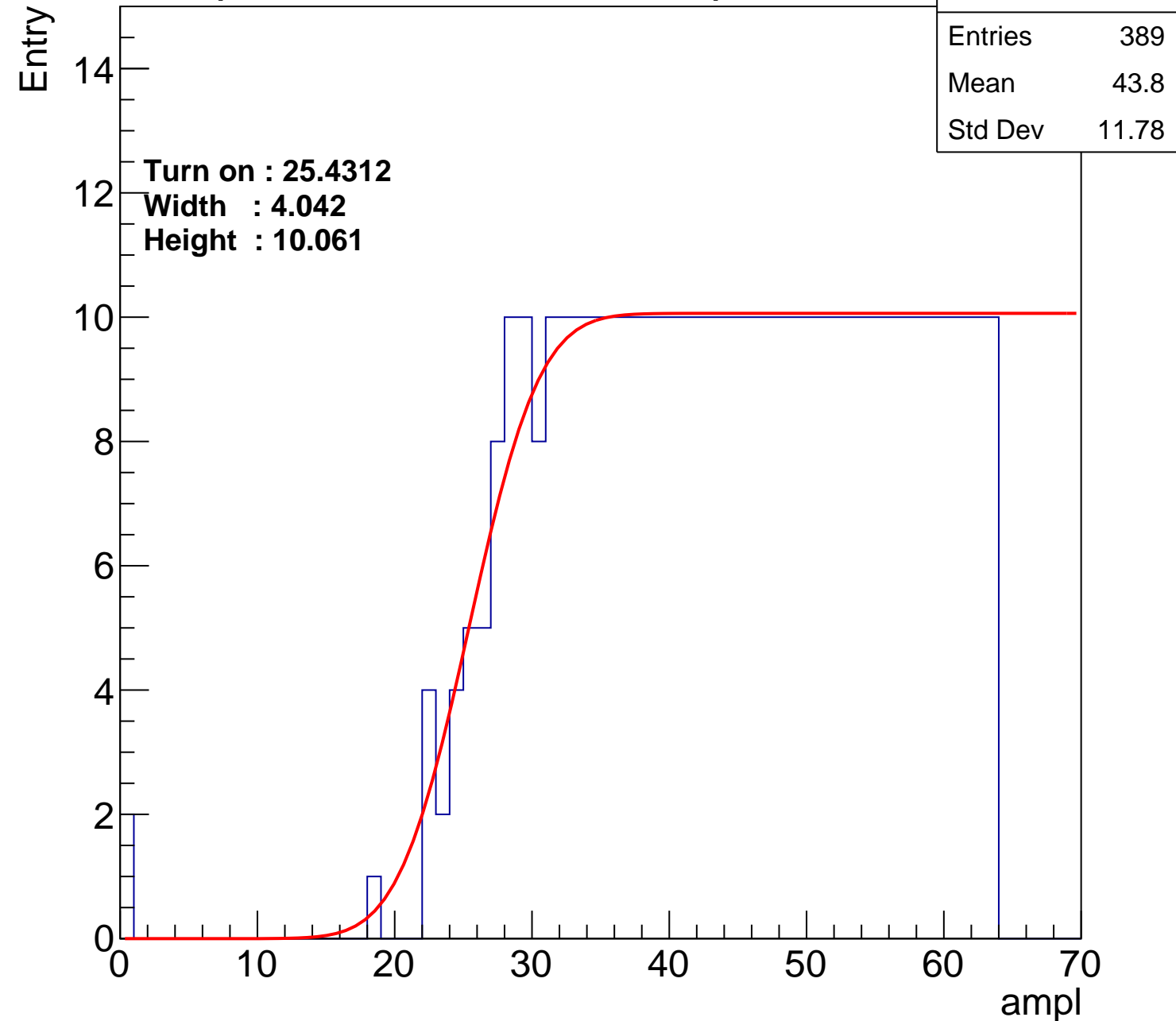
Width : 4.042

Height : 10.061

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch9

calib_packv5_042523_0143.root, FC#13, port D2

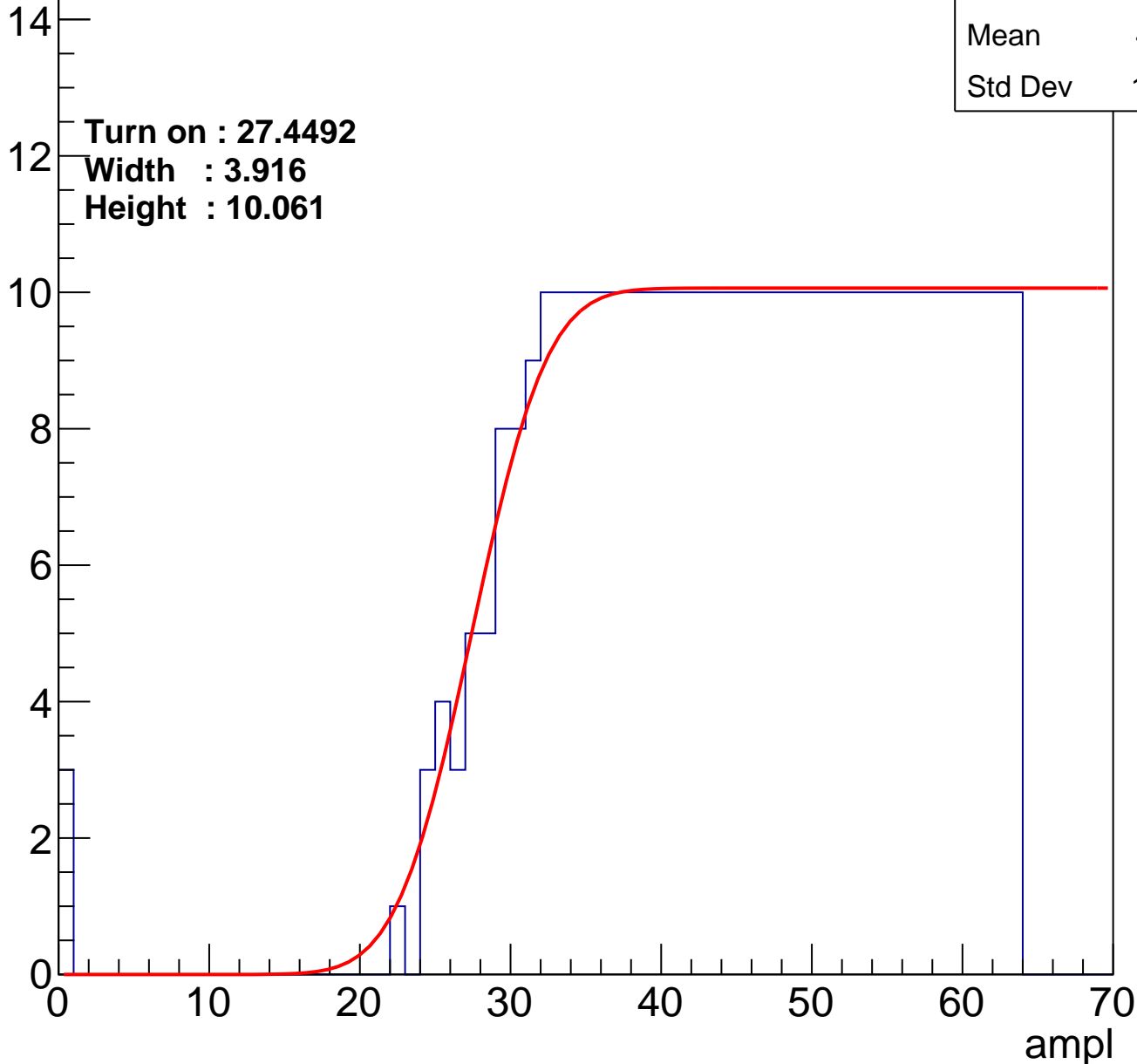
Entries	369
Mean	44.71
Std Dev	11.47

Turn on : 27.4492

Width : 3.916

Height : 10.061

Entry



B1L003S, U1-ch10

calib_packv5_042523_0143.root, FC#13, port D2

Entries	384
Mean	43.99
Std Dev	11.87

Turn on : 26.3874

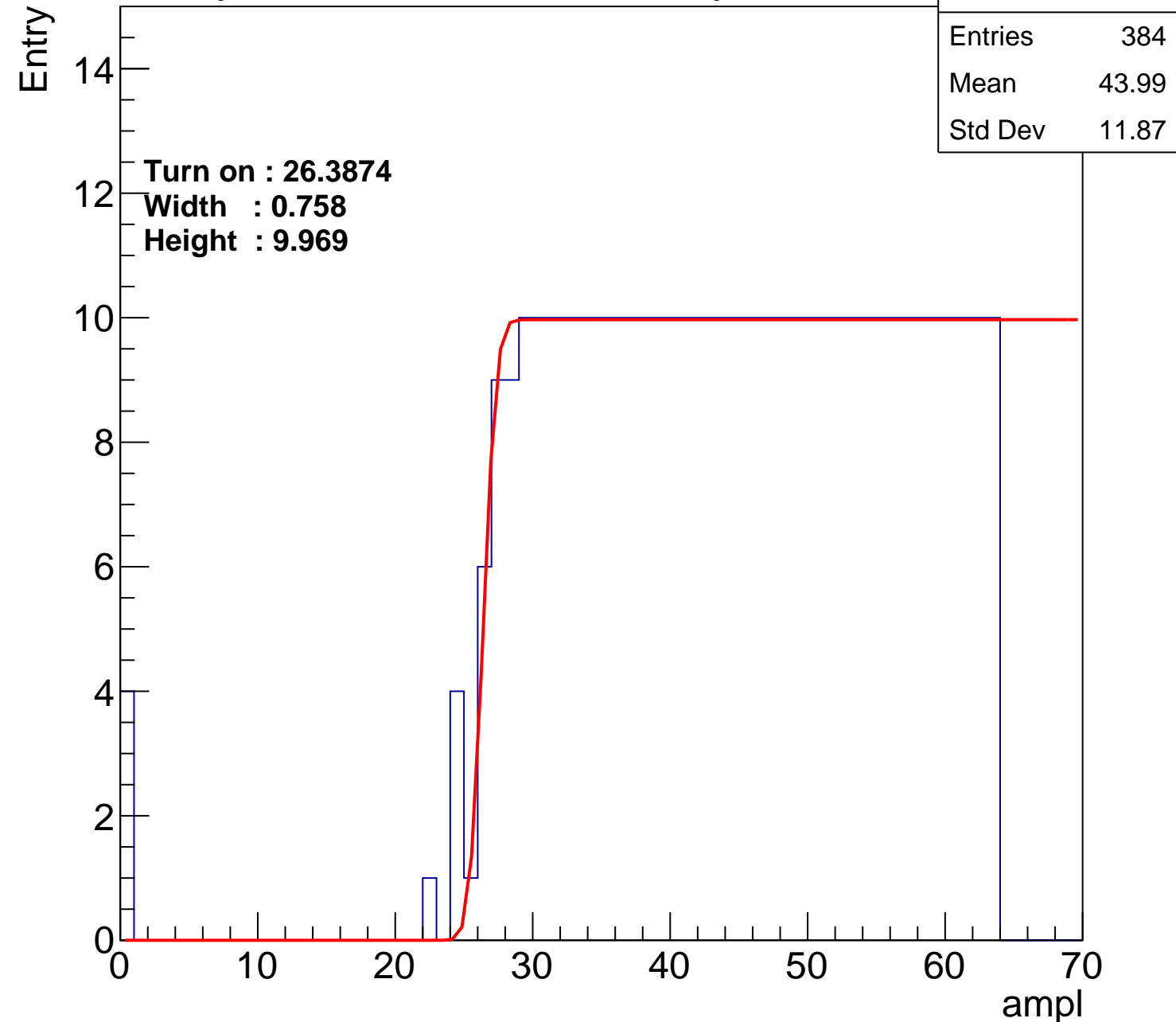
Width : 0.758

Height : 9.969

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch11

calib_packv5_042523_0143.root, FC#13, port D2

Entries	365
Mean	45.01
Std Dev	11.11

Turn on : 28.2426

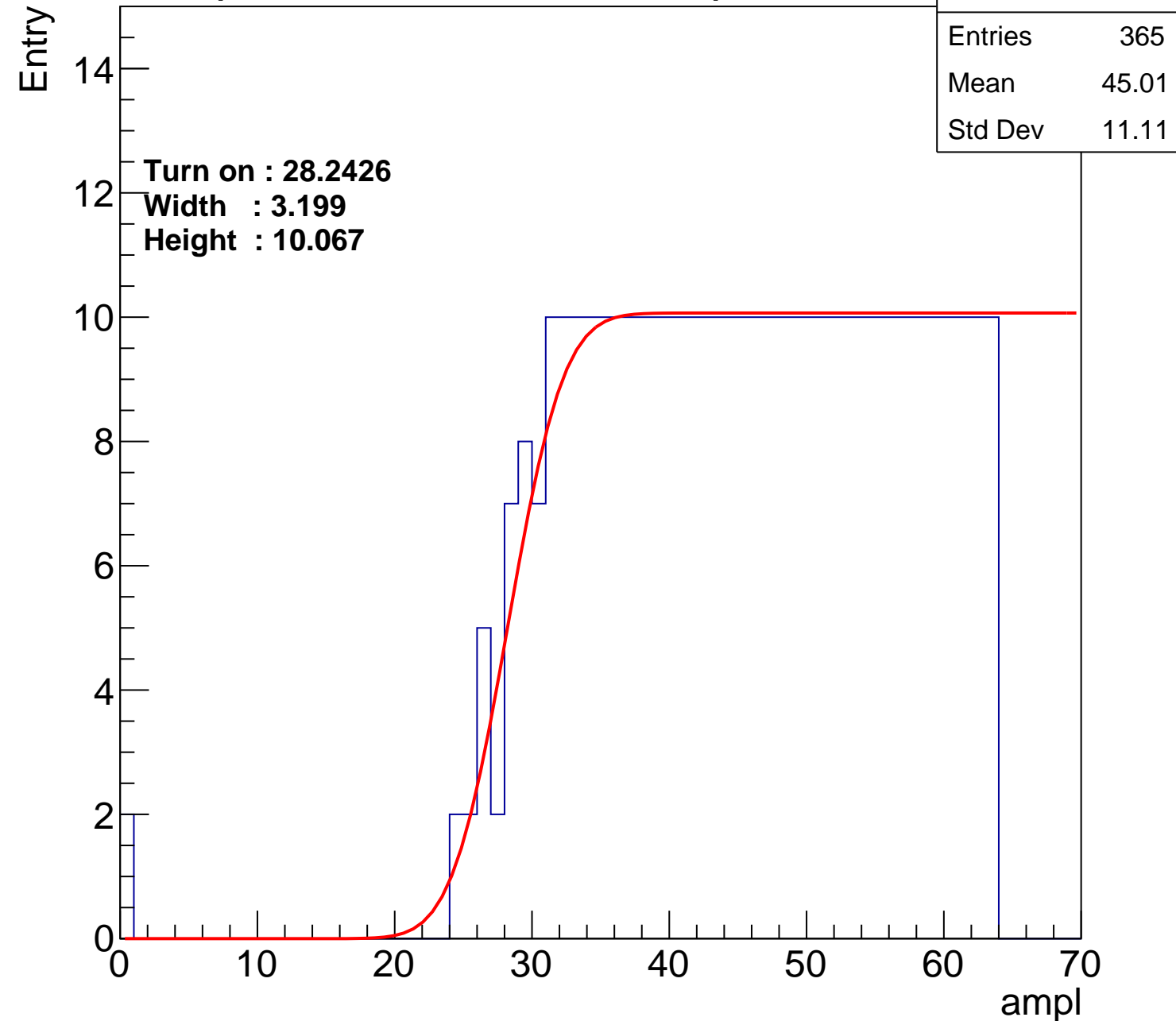
Width : 3.199

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch12

calib_packv5_042523_0143.root, FC#13, port D2

Entries	384
Mean	43.97
Std Dev	11.84

Turn on : 26.0566

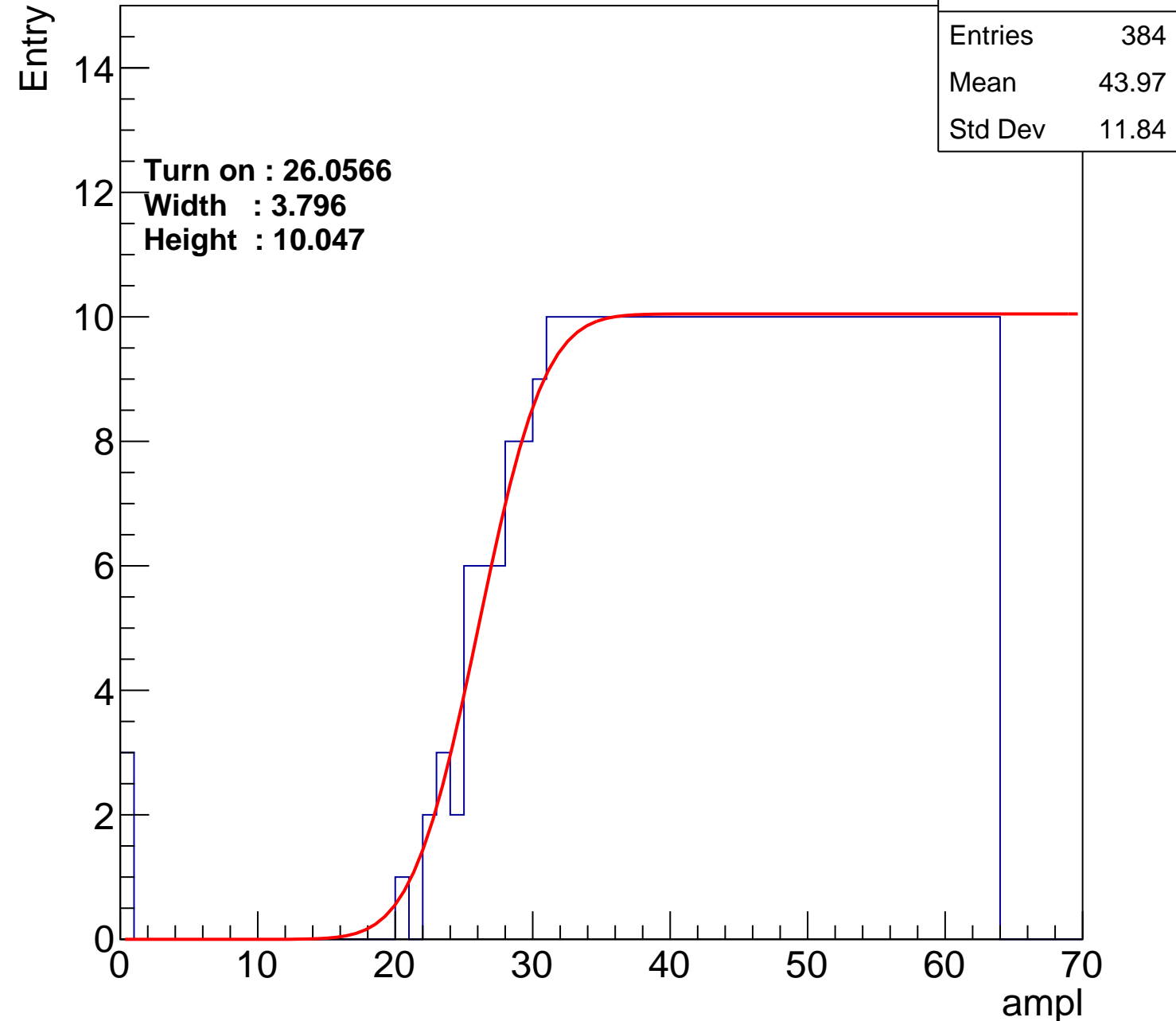
Width : 3.796

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch13

calib_packv5_042523_0143.root, FC#13, port D2

Entries	362
Mean	45.09
Std Dev	11.15

Turn on : 27.7515

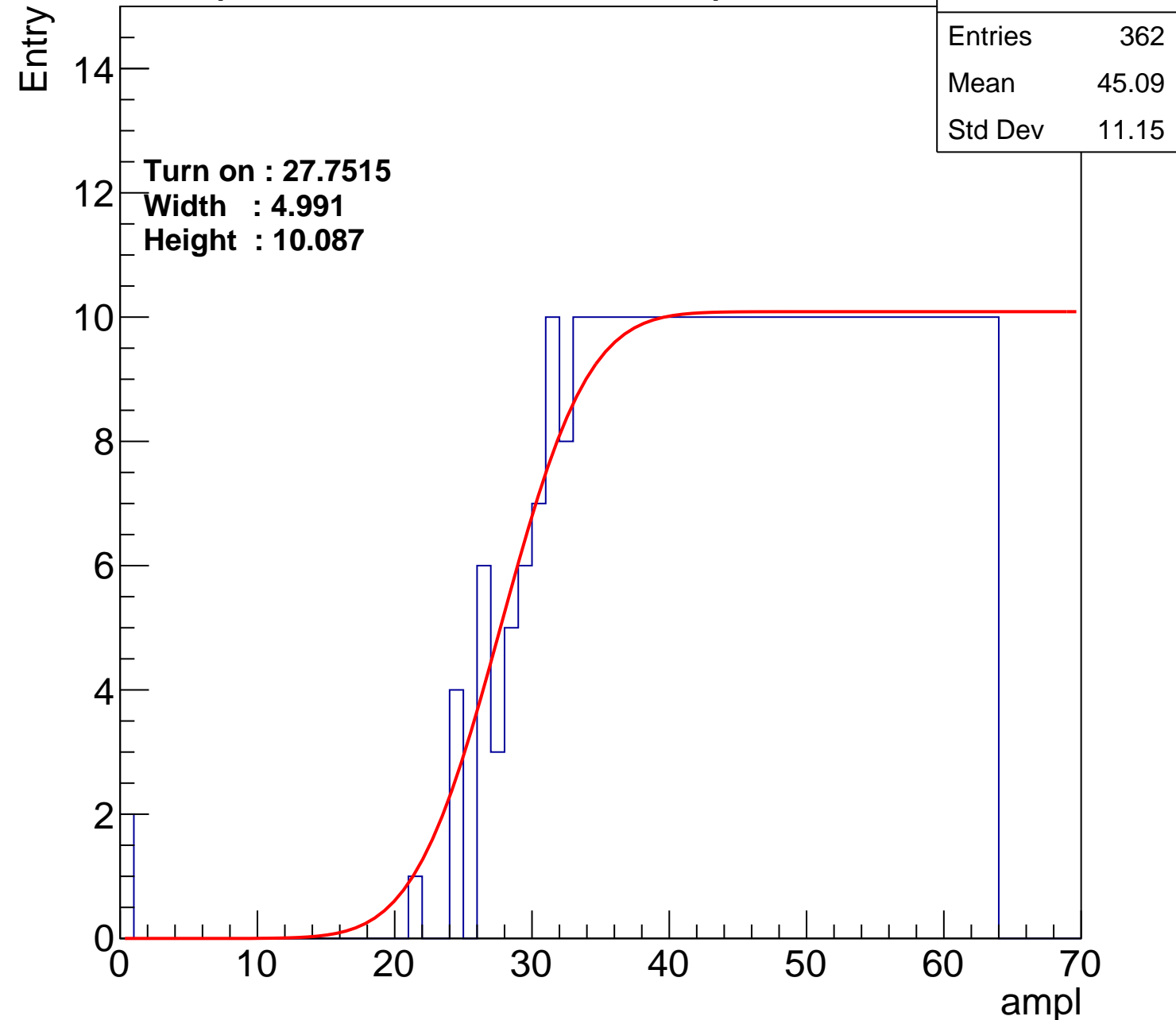
Width : 4.991

Height : 10.087

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch14

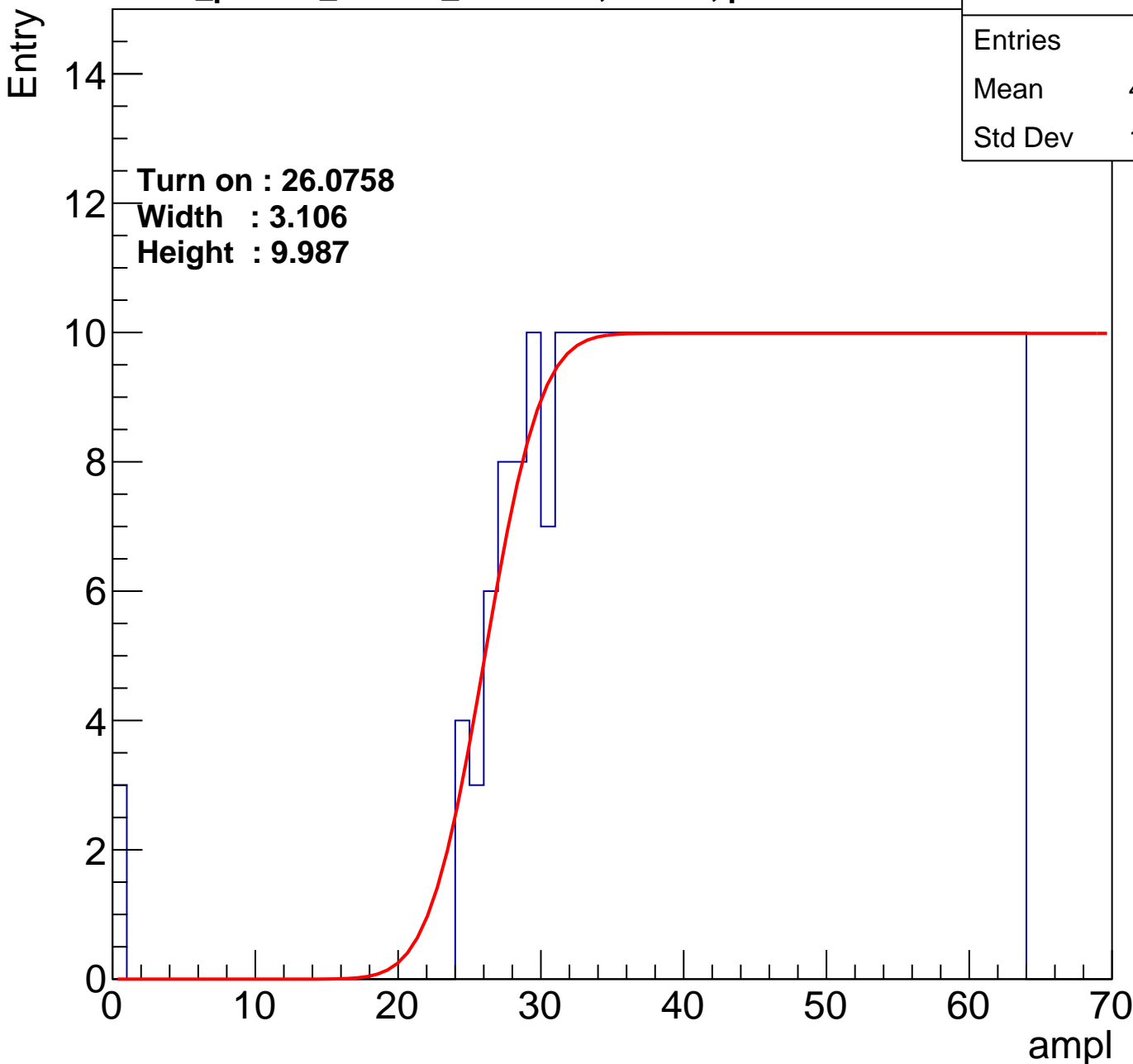
calib_packv5_042523_0143.root, FC#13, port D2

Entries	379
Mean	44.27
Std Dev	11.63

Turn on : 26.0758

Width : 3.106

Height : 9.987



B1L003S, U1-ch15

calib_packv5_042523_0143.root, FC#13, port D2

Entries	373
Mean	44.39
Std Dev	11.92

Turn on : 27.2794

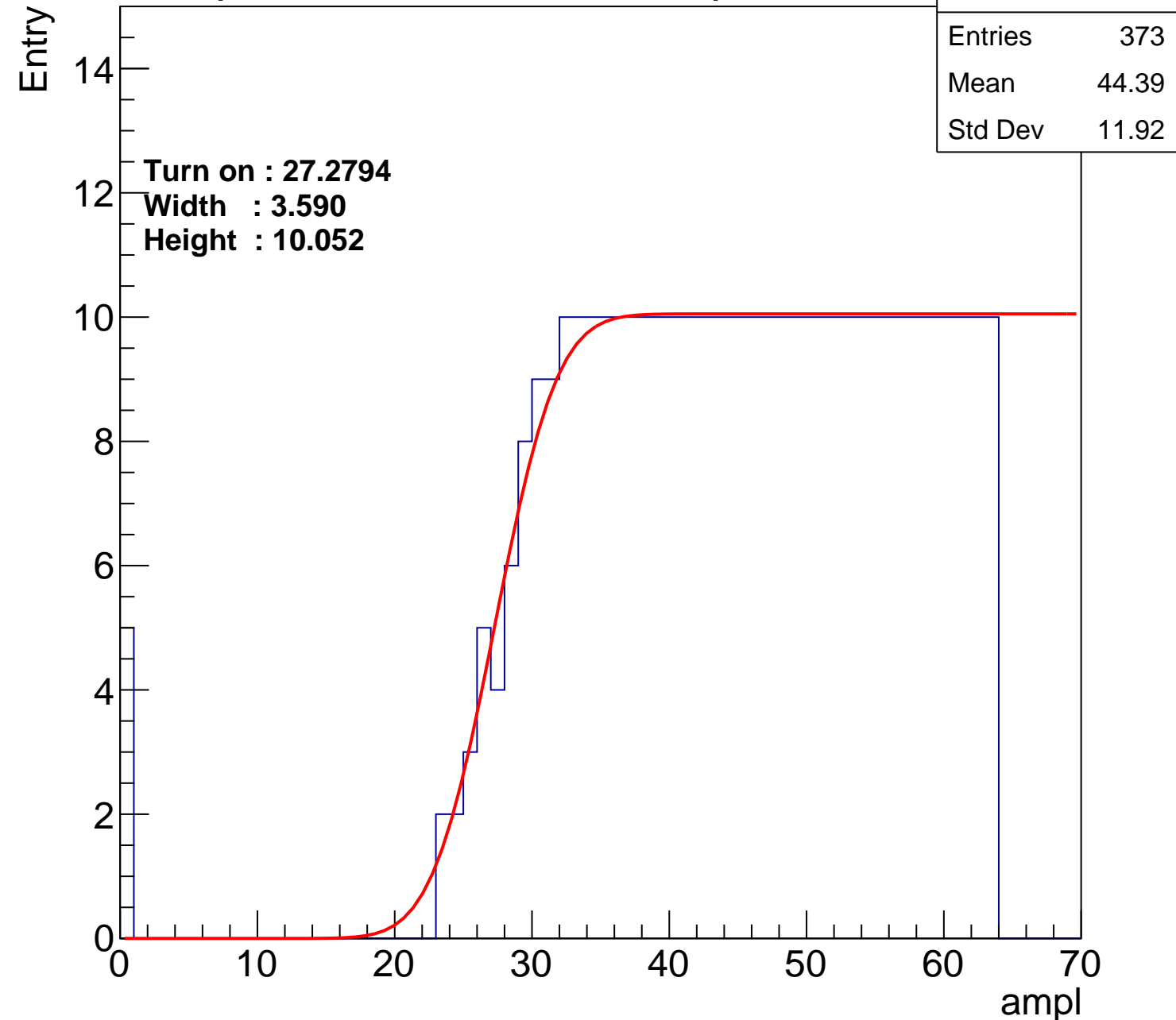
Width : 3.590

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch16

calib_packv5_042523_0143.root, FC#13, port D2

Entries	380
Mean	44.27
Std Dev	11.5

Turn on : 26.2963

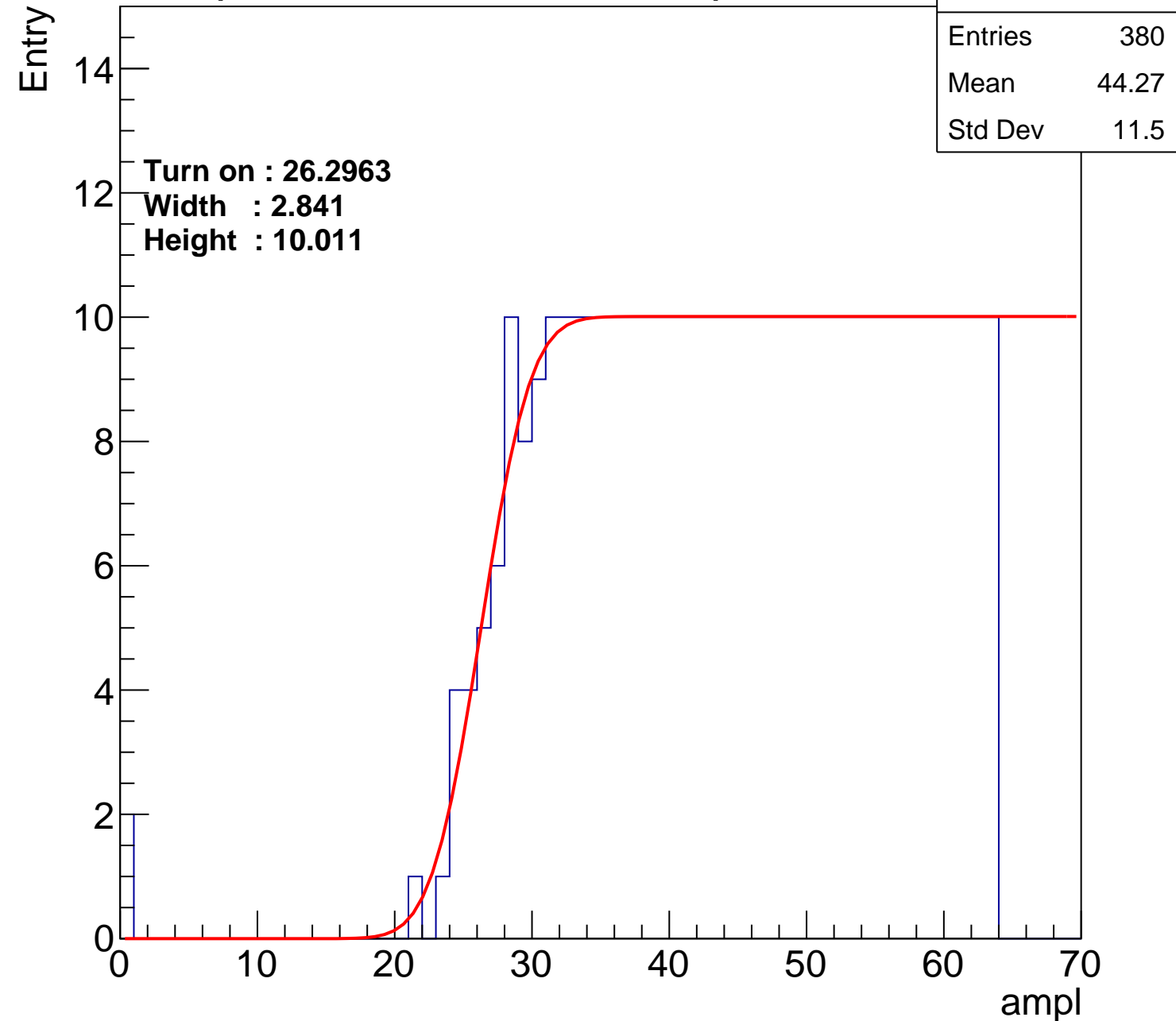
Width : 2.841

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch17

calib_packv5_042523_0143.root, FC#13, port D2

Entries	375
Mean	44.6
Std Dev	11.16

Turn on : 26.5839

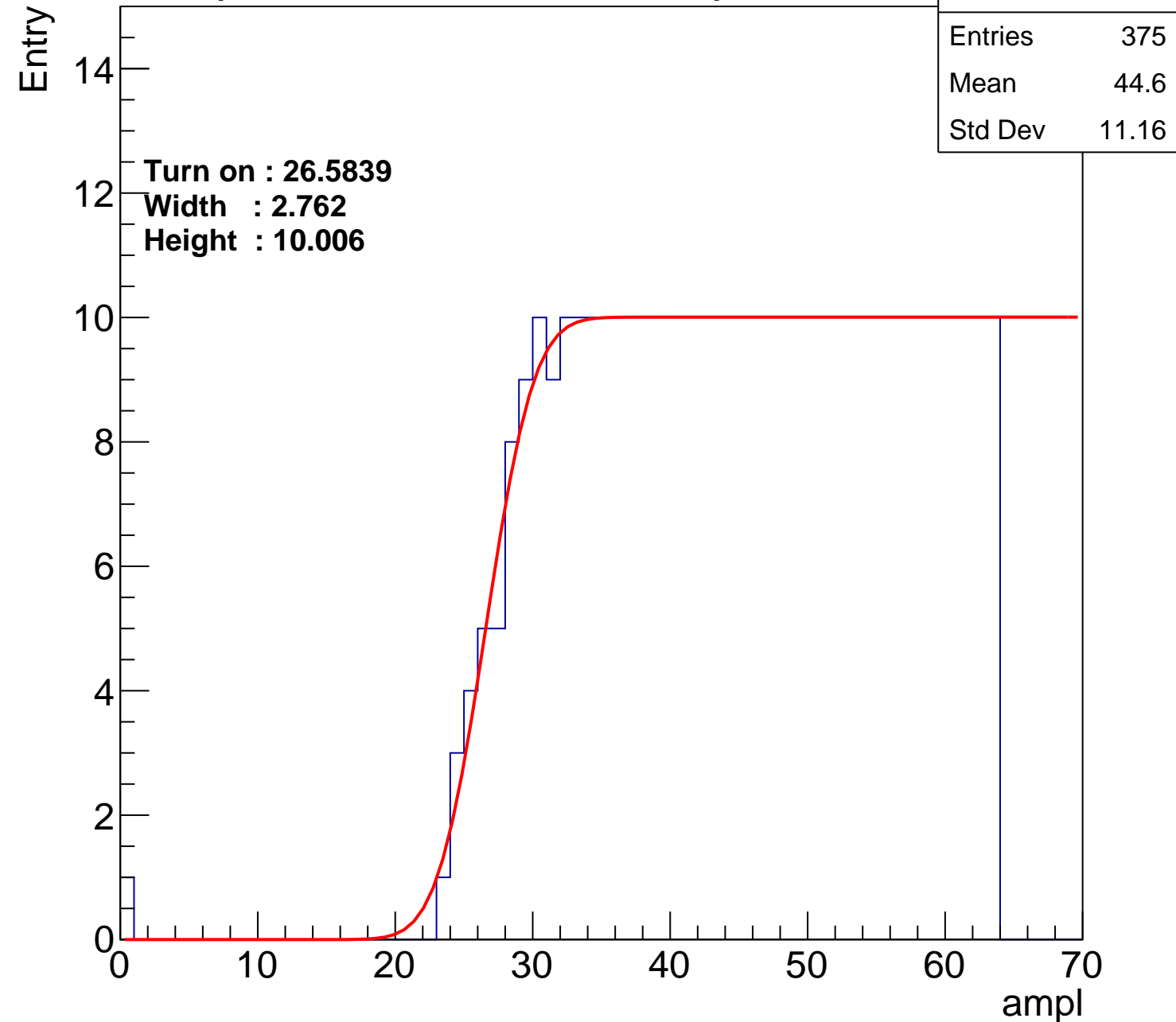
Width : 2.762

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch18

calib_packv5_042523_0143.root, FC#13, port D2

Entries	372
Mean	44.66
Std Dev	11.3

Turn on : 27.3186

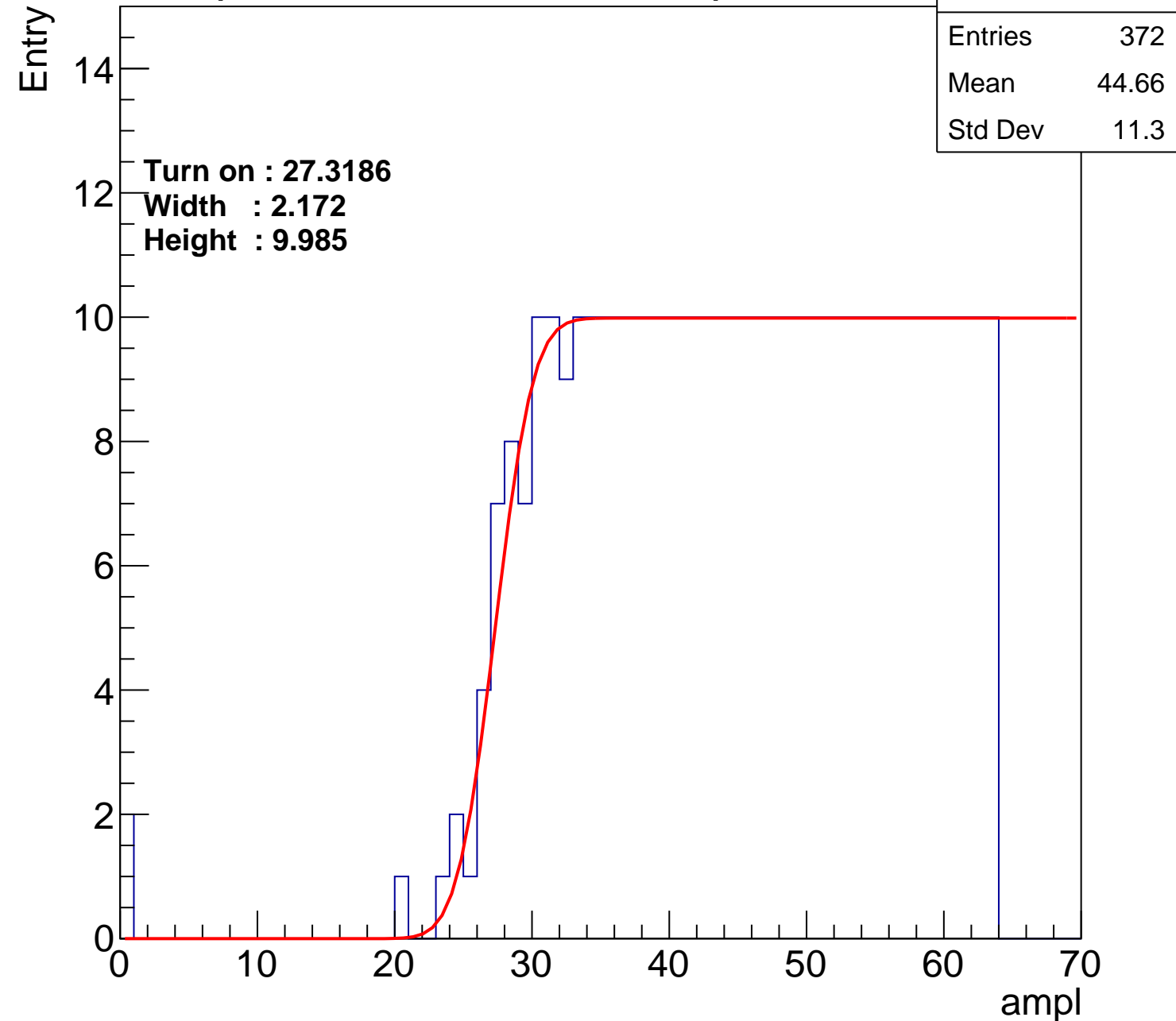
Width : 2.172

Height : 9.985

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch19

calib_packv5_042523_0143.root, FC#13, port D2

Entries	384
Mean	44.09
Std Dev	11.58

Turn on : 25.7905

Width : 3.635

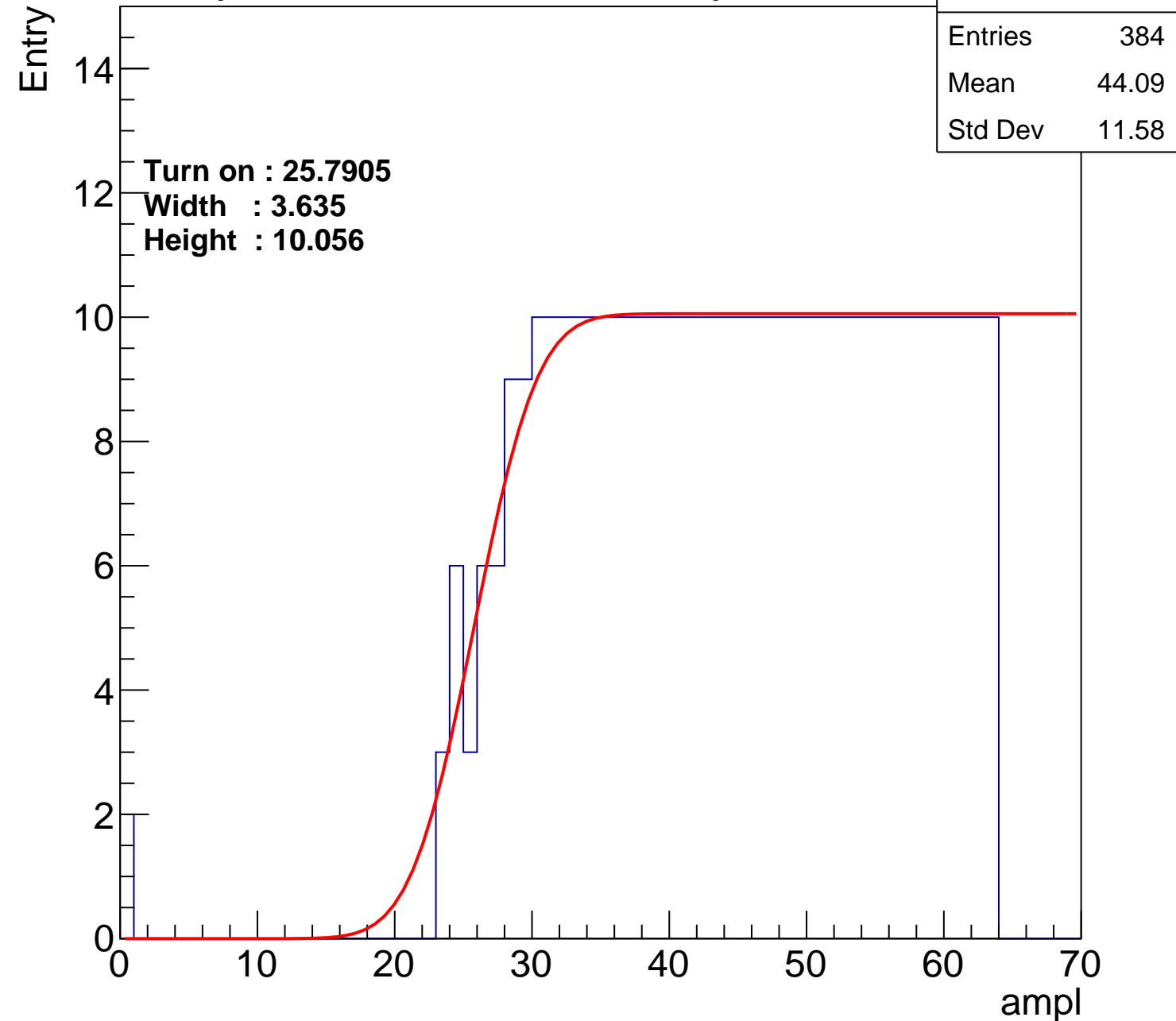
Height : 10.056

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L003S, U1-ch20

calib_packv5_042523_0143.root, FC#13, port D2

Entries	378
Mean	44.37
Std Dev	11.45

Turn on : 26.7306

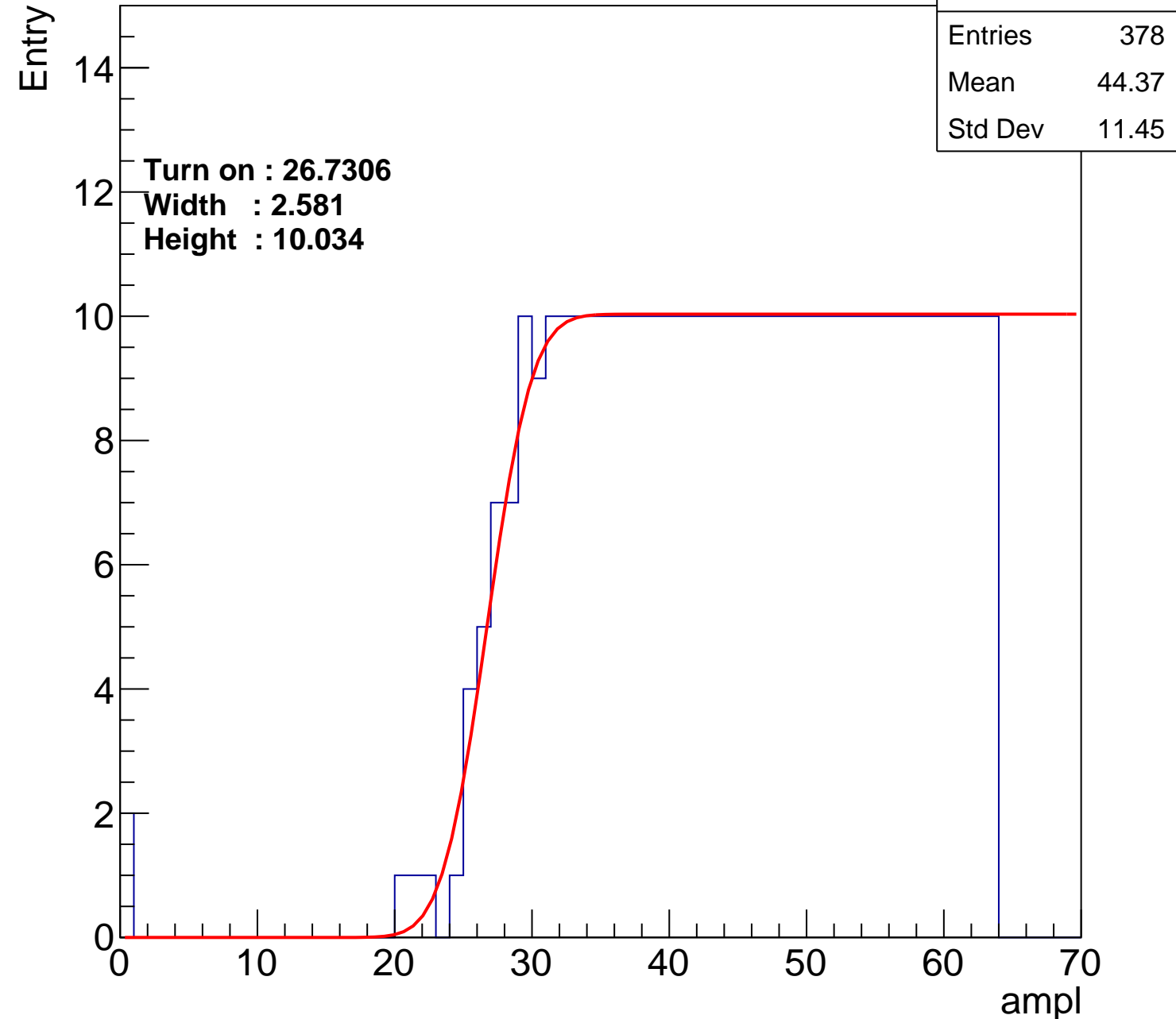
Width : 2.581

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch21

calib_packv5_042523_0143.root, FC#13, port D2

Entries	384
Mean	44.03
Std Dev	11.75

Turn on : 26.1042

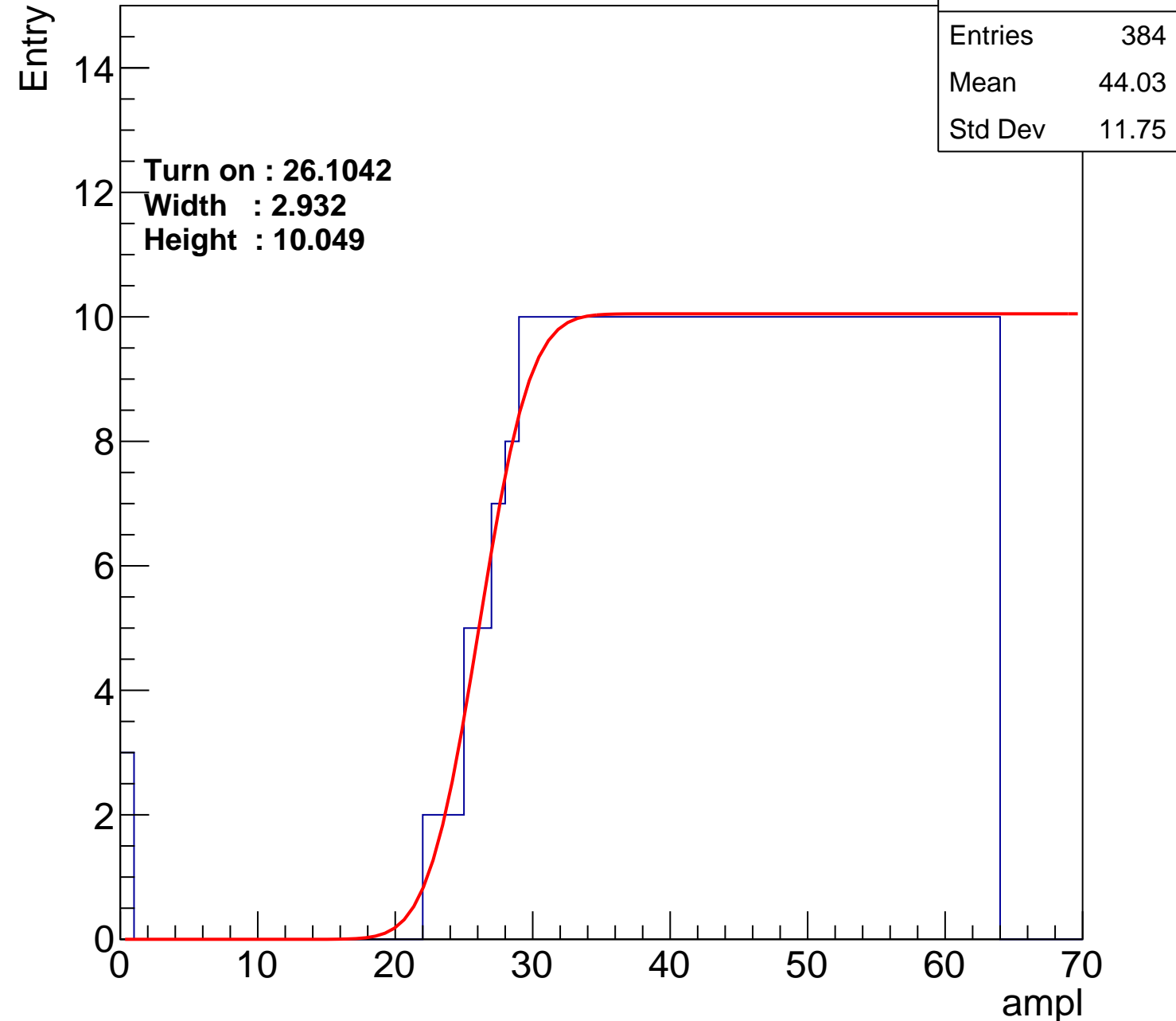
Width : 2.932

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch22

calib_packv5_042523_0143.root, FC#13, port D2

Entries	370
Mean	44.86
Std Dev	11

Turn on : 27.2411

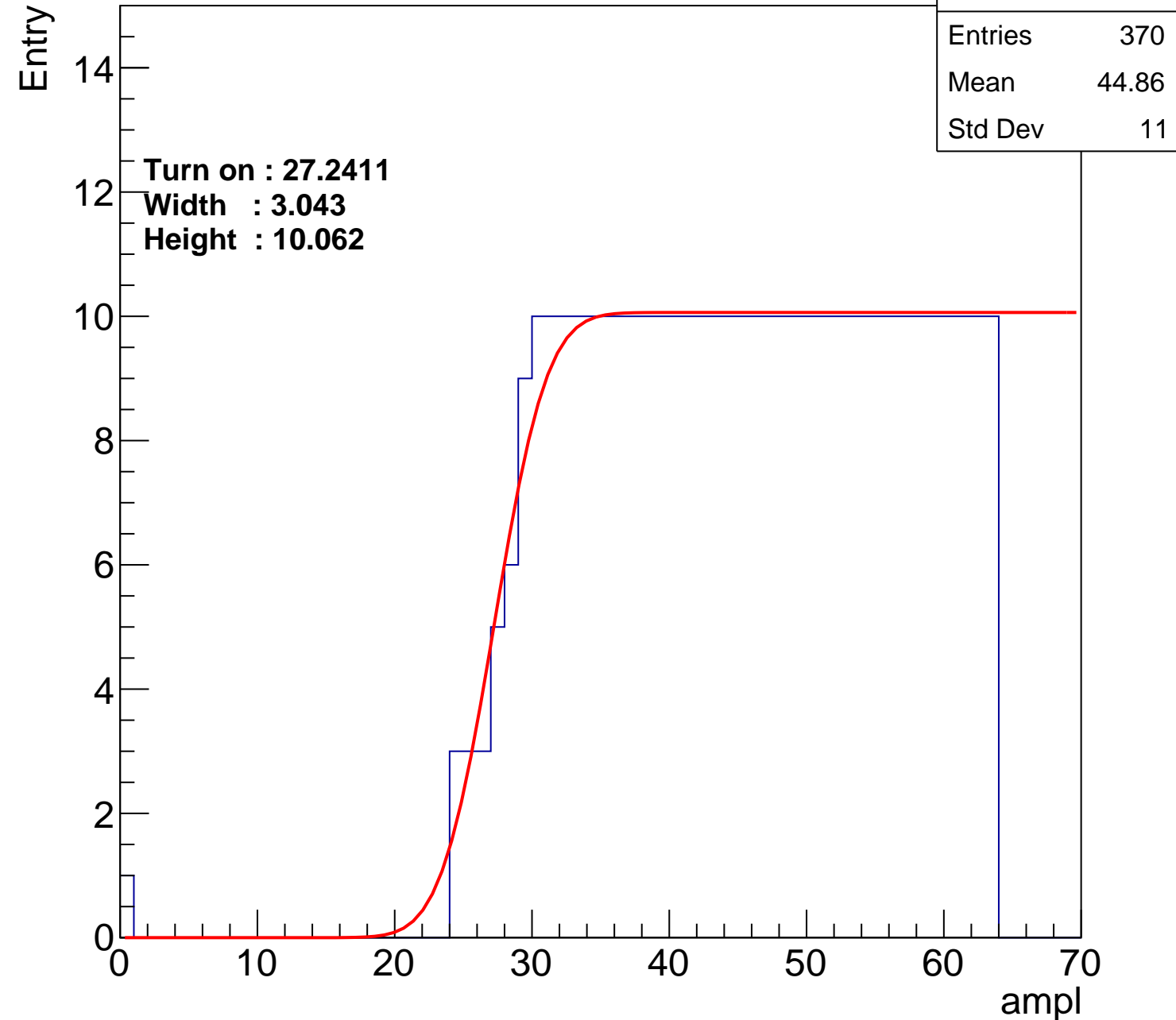
Width : 3.043

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch23

calib_packv5_042523_0143.root, FC#13, port D2

Entries	360
Mean	44.89
Std Dev	11.92

Turn on : 29.1133

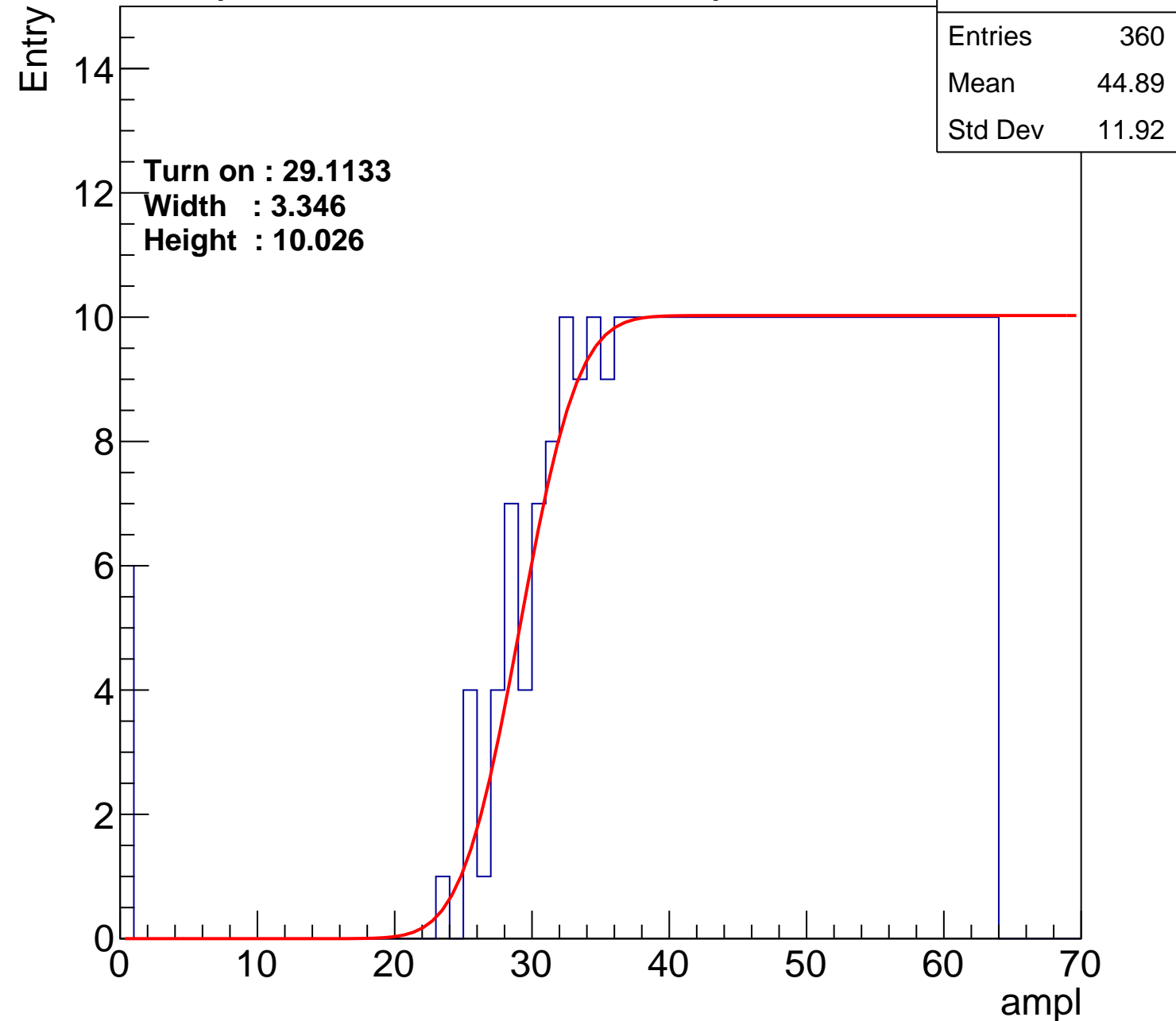
Width : 3.346

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch24

calib_packv5_042523_0143.root, FC#13, port D2

Entries	394
Mean	43.59
Std Dev	11.85

Turn on : 24.7524

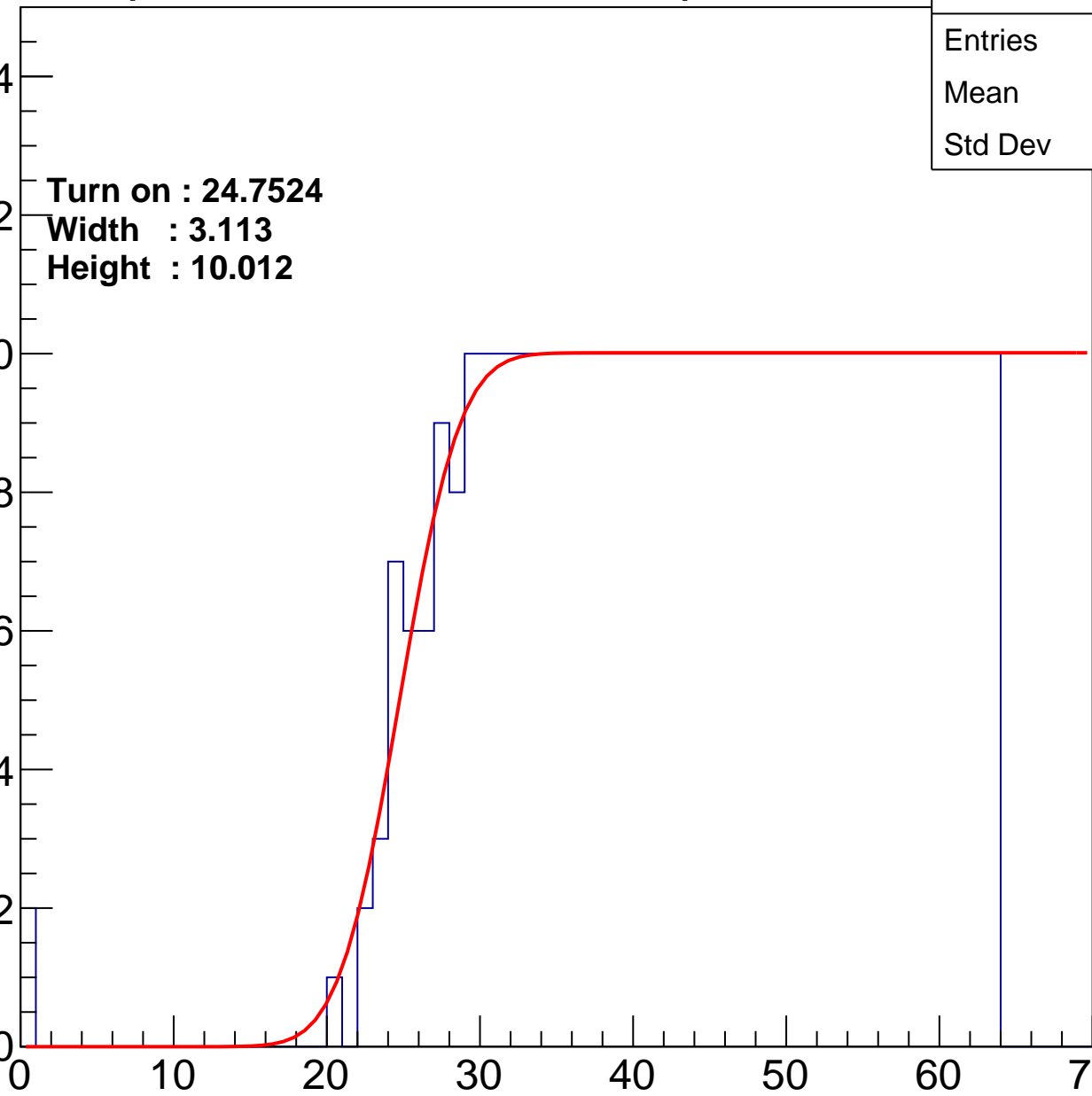
Width : 3.113

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch25

calib_packv5_042523_0143.root, FC#13, port D2

Entries	376
Mean	44.13
Std Dev	12.29

Turn on : 27.1320

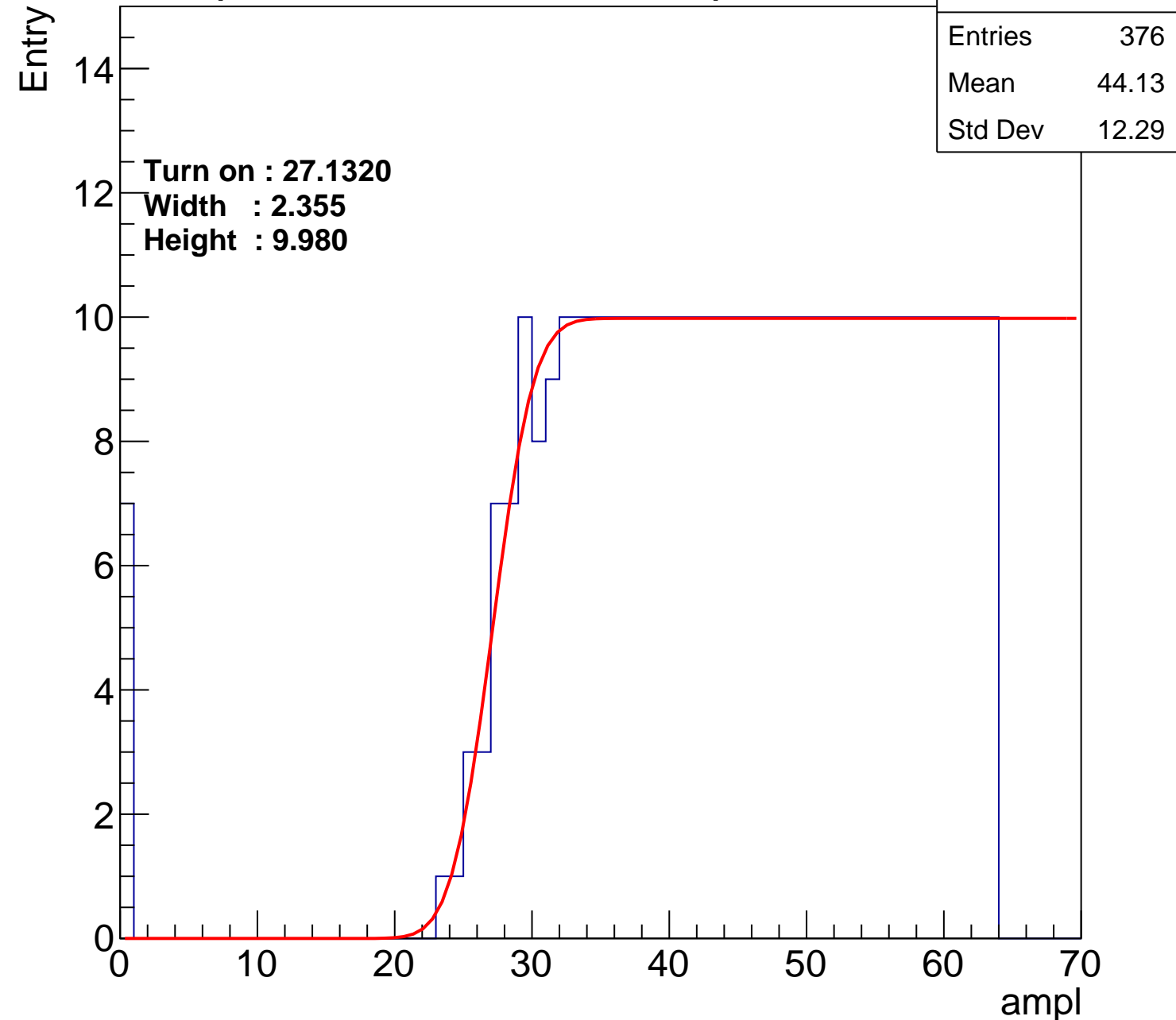
Width : 2.355

Height : 9.980

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch26

calib_packv5_042523_0143.root, FC#13, port D2

Entries	396
Mean	43.38
Std Dev	12.2

Turn on : 25.3160

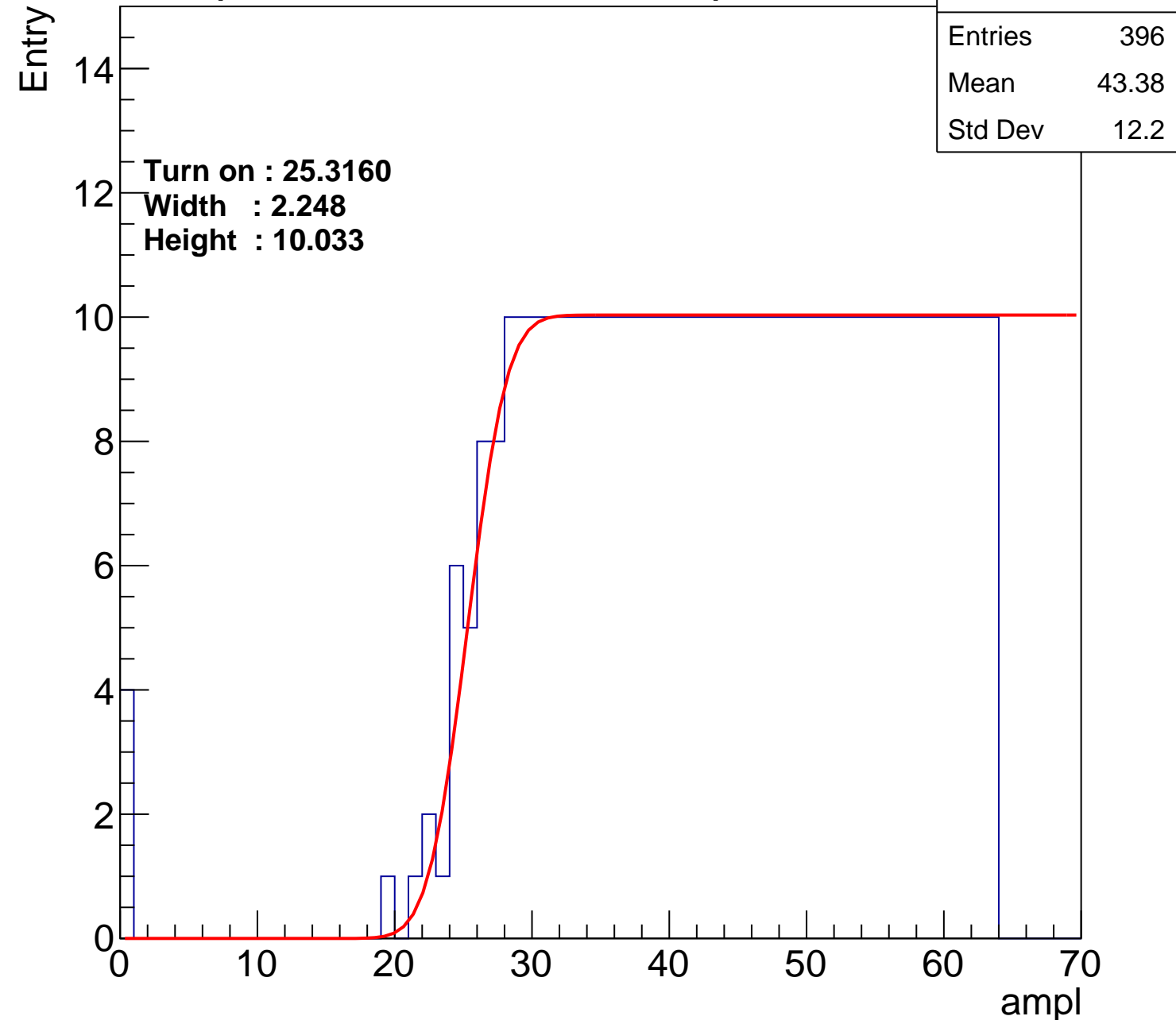
Width : 2.248

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch27

calib_packv5_042523_0143.root, FC#13, port D2

Entries	368
Mean	44.66
Std Dev	11.76

Turn on : 27.6865

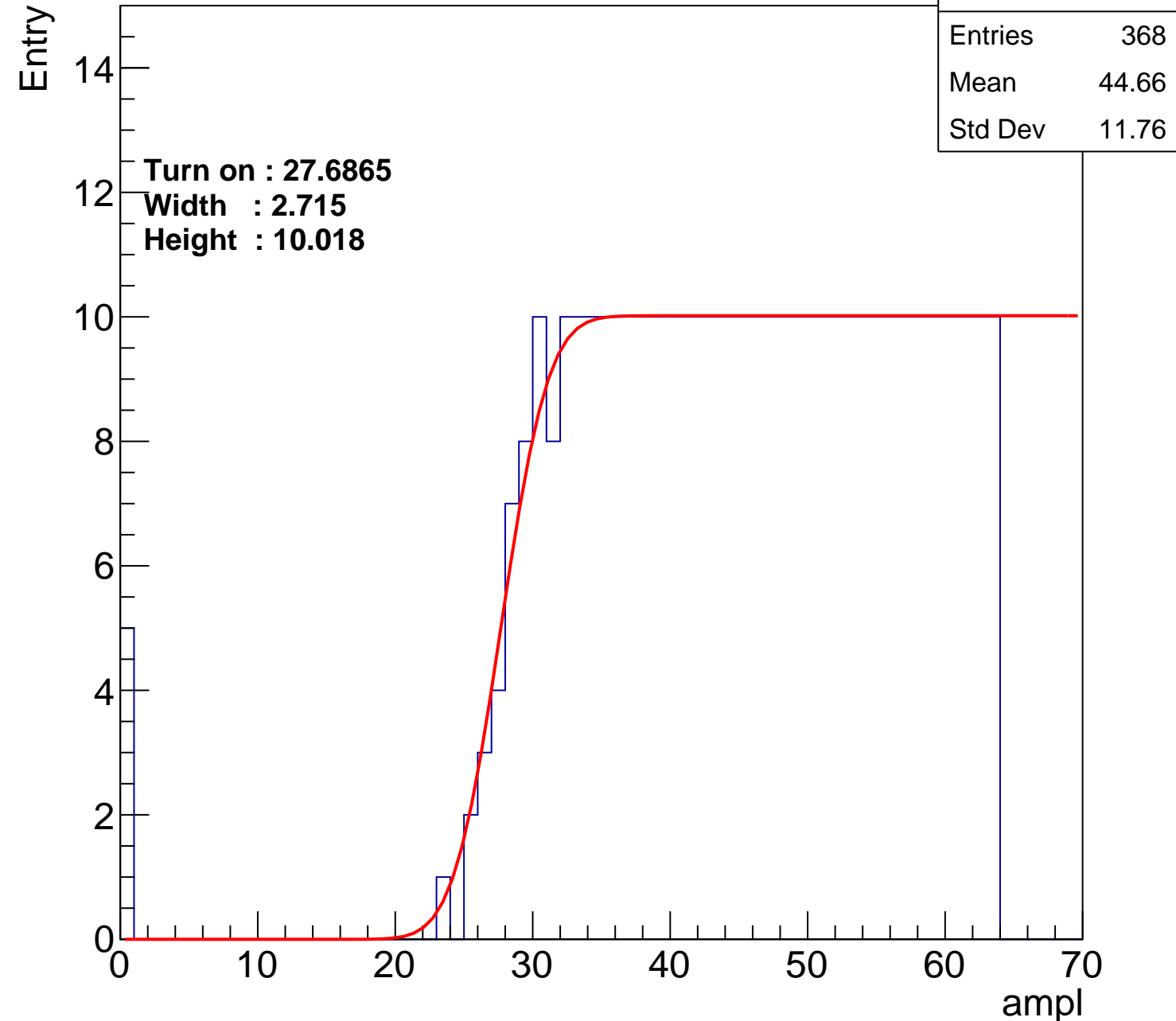
Width : 2.715

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch28

calib_packv5_042523_0143.root, FC#13, port D2

Entries	372
Mean	44.53
Std Dev	11.67

Turn on : 27.2336

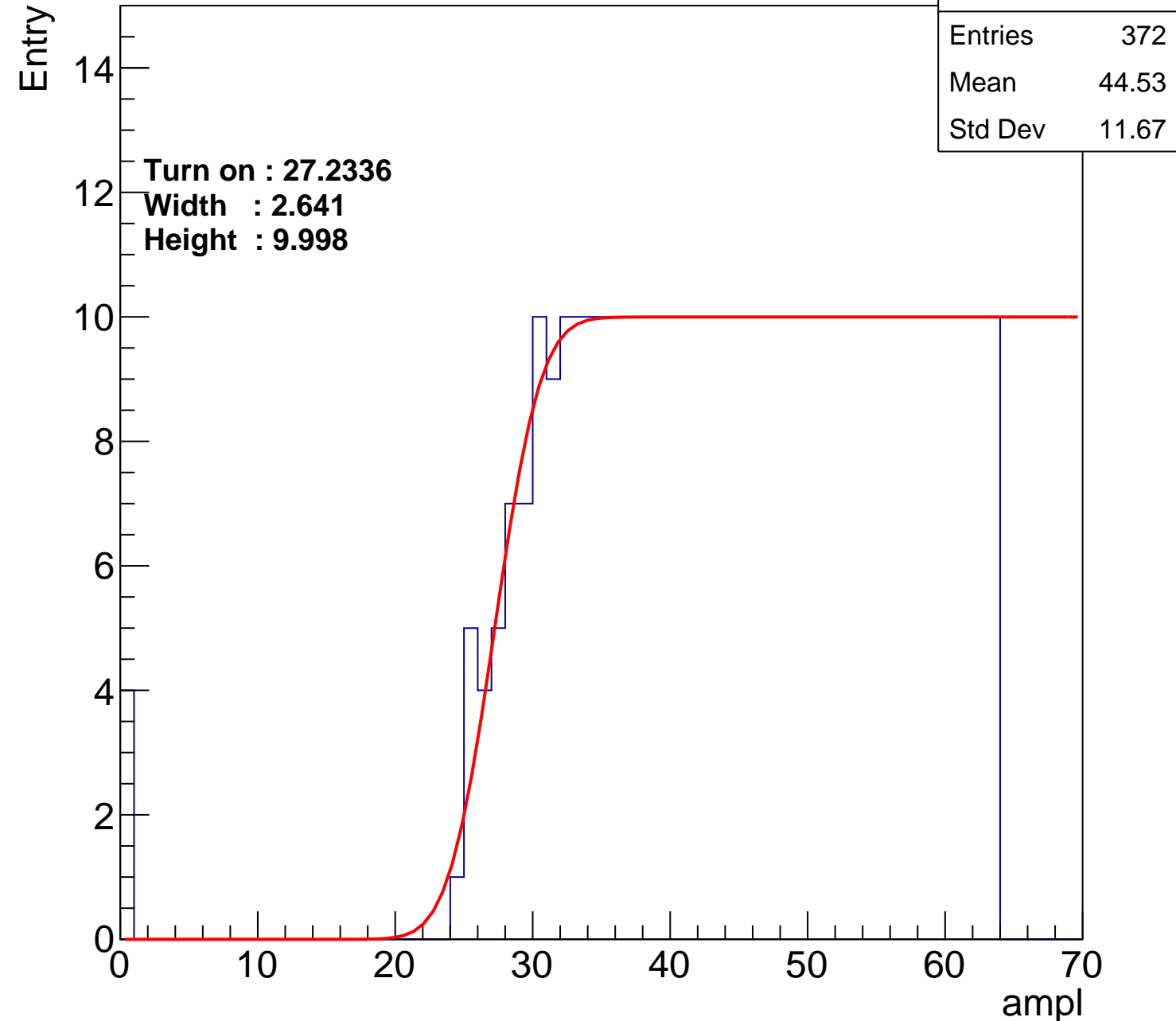
Width : 2.641

Height : 9.998

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch29

calib_packv5_042523_0143.root, FC#13, port D2

Entries	365
Mean	44.96
Std Dev	11.21

Turn on : 28.8315

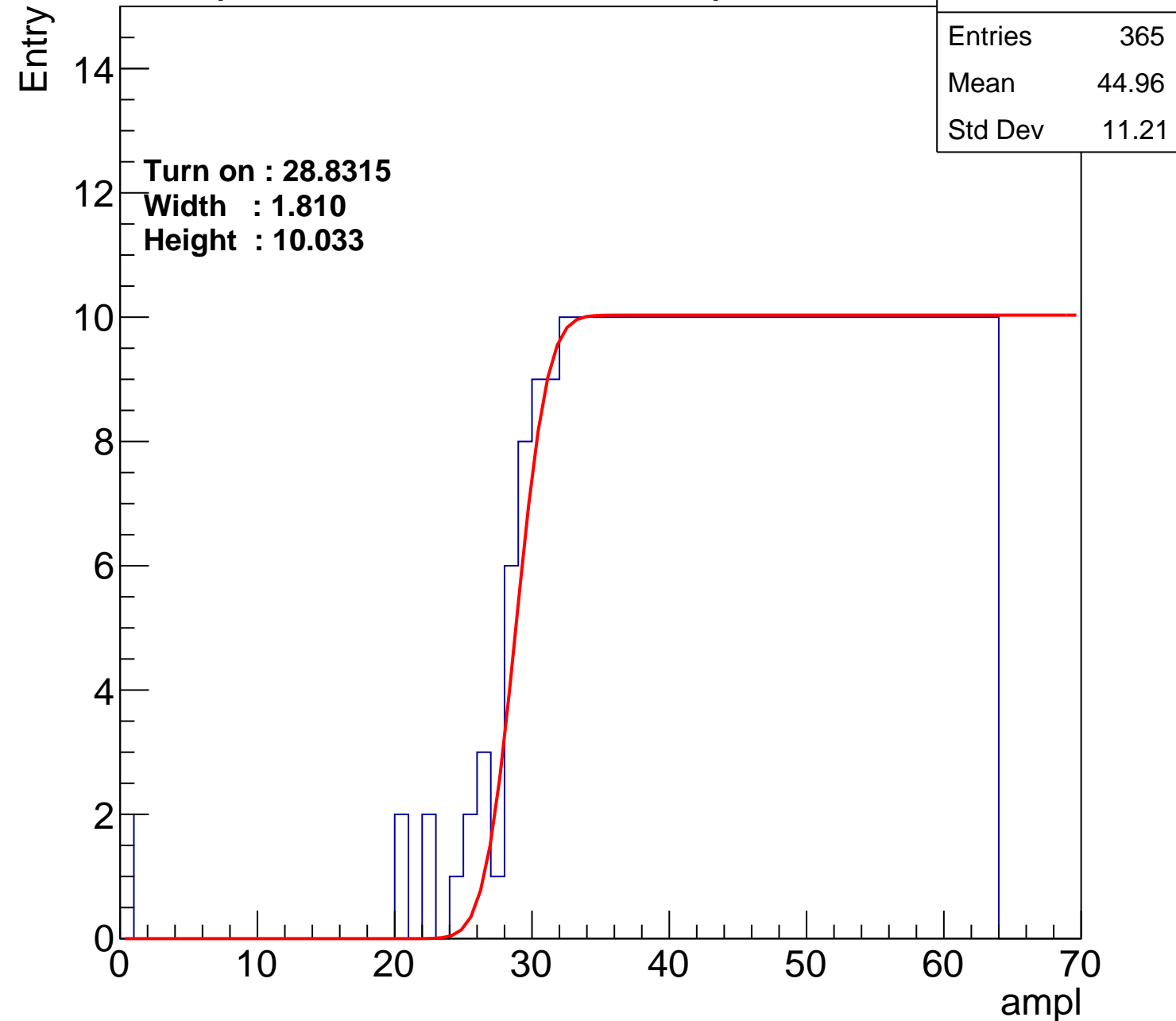
Width : 1.810

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch30

calib_packv5_042523_0143.root, FC#13, port D2

Entries	377
Mean	44.22
Std Dev	11.96

Turn on : 26.6967

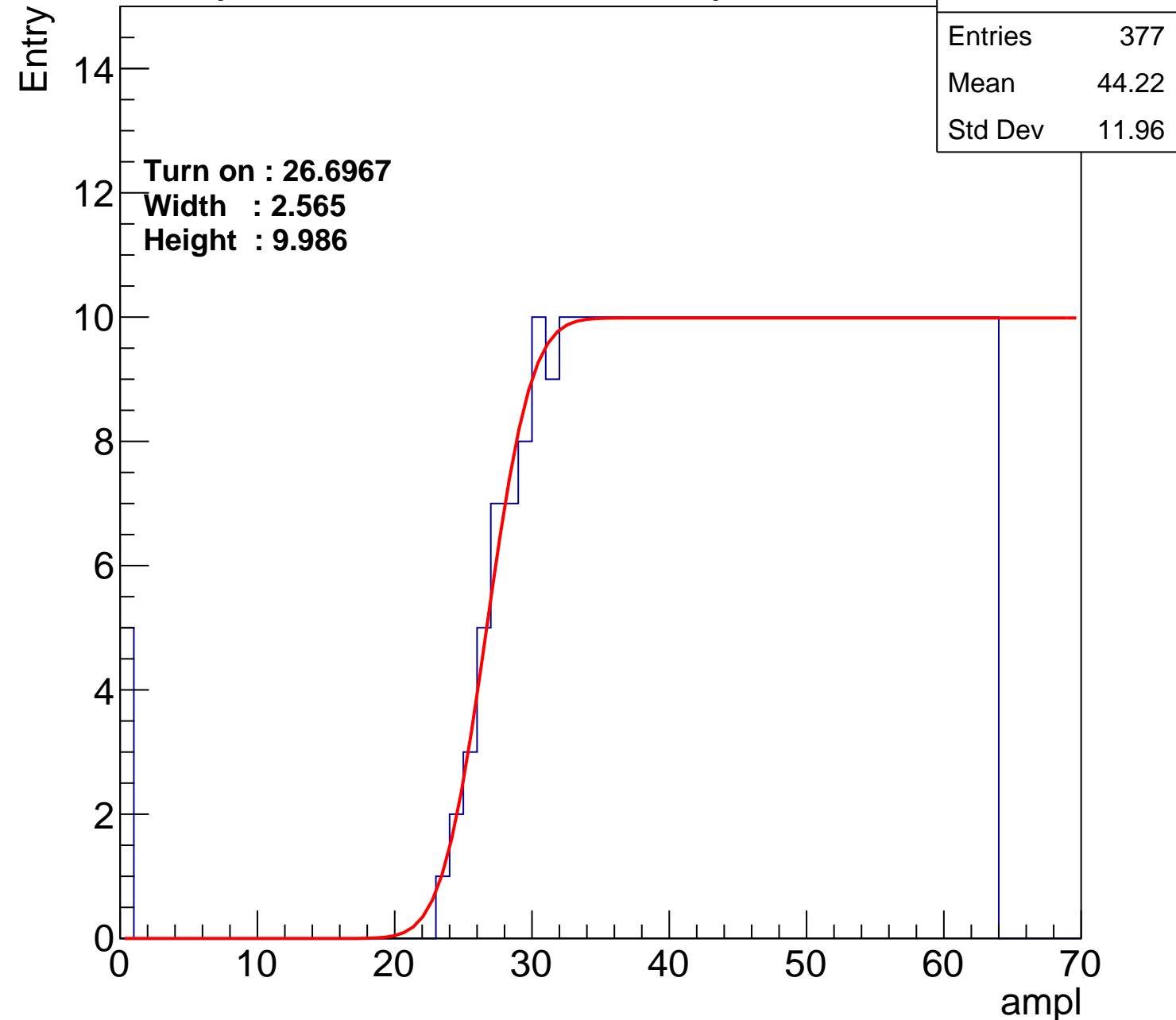
Width : 2.565

Height : 9.986

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch31

calib_packv5_042523_0143.root, FC#13, port D2

Entries	371
Mean	44.57
Std Dev	11.67

Turn on : 27.5021

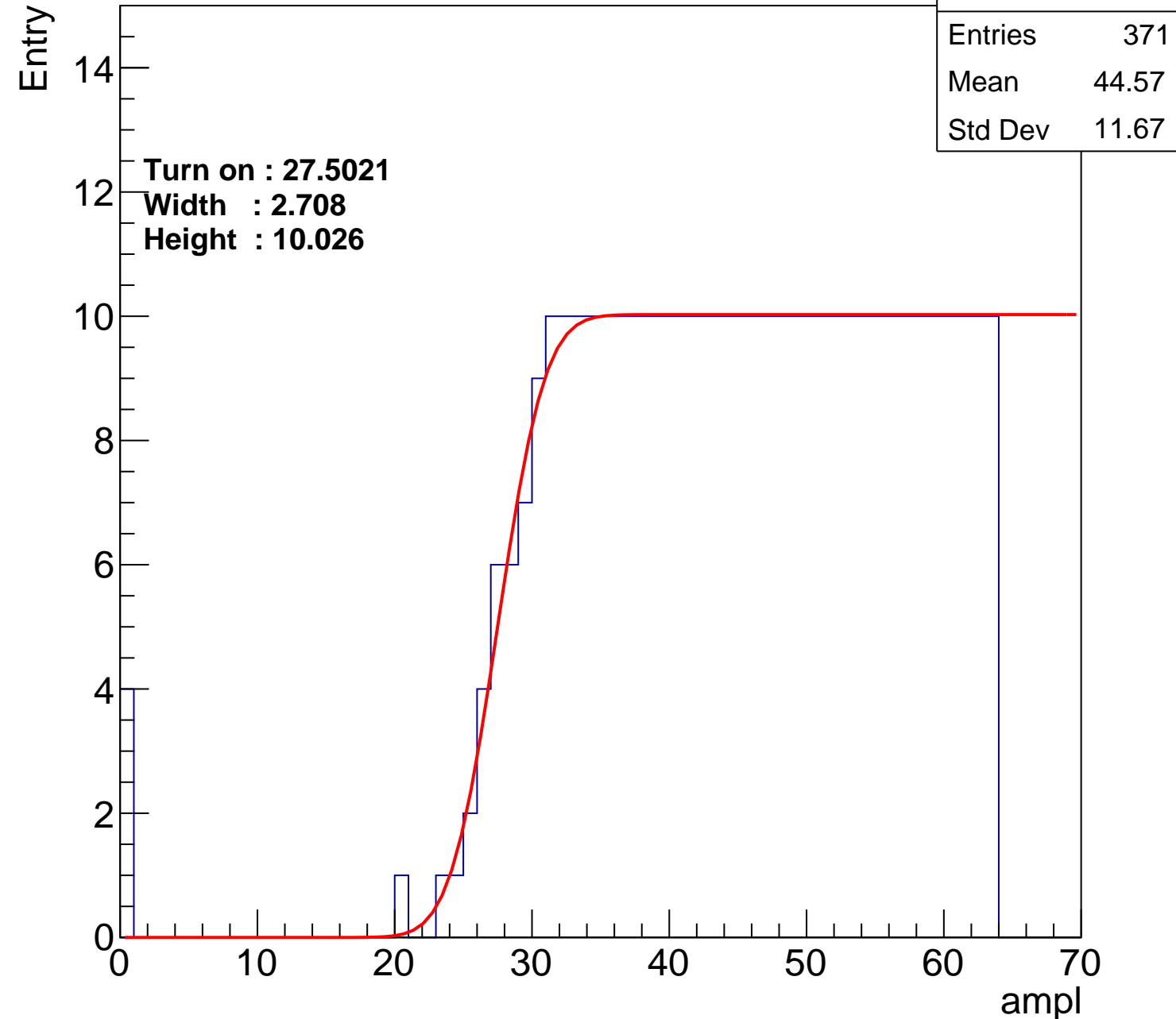
Width : 2.708

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch32

calib_packv5_042523_0143.root, FC#13, port D2

Entries	381
Mean	44.27
Std Dev	11.37

Turn on : 26.1478

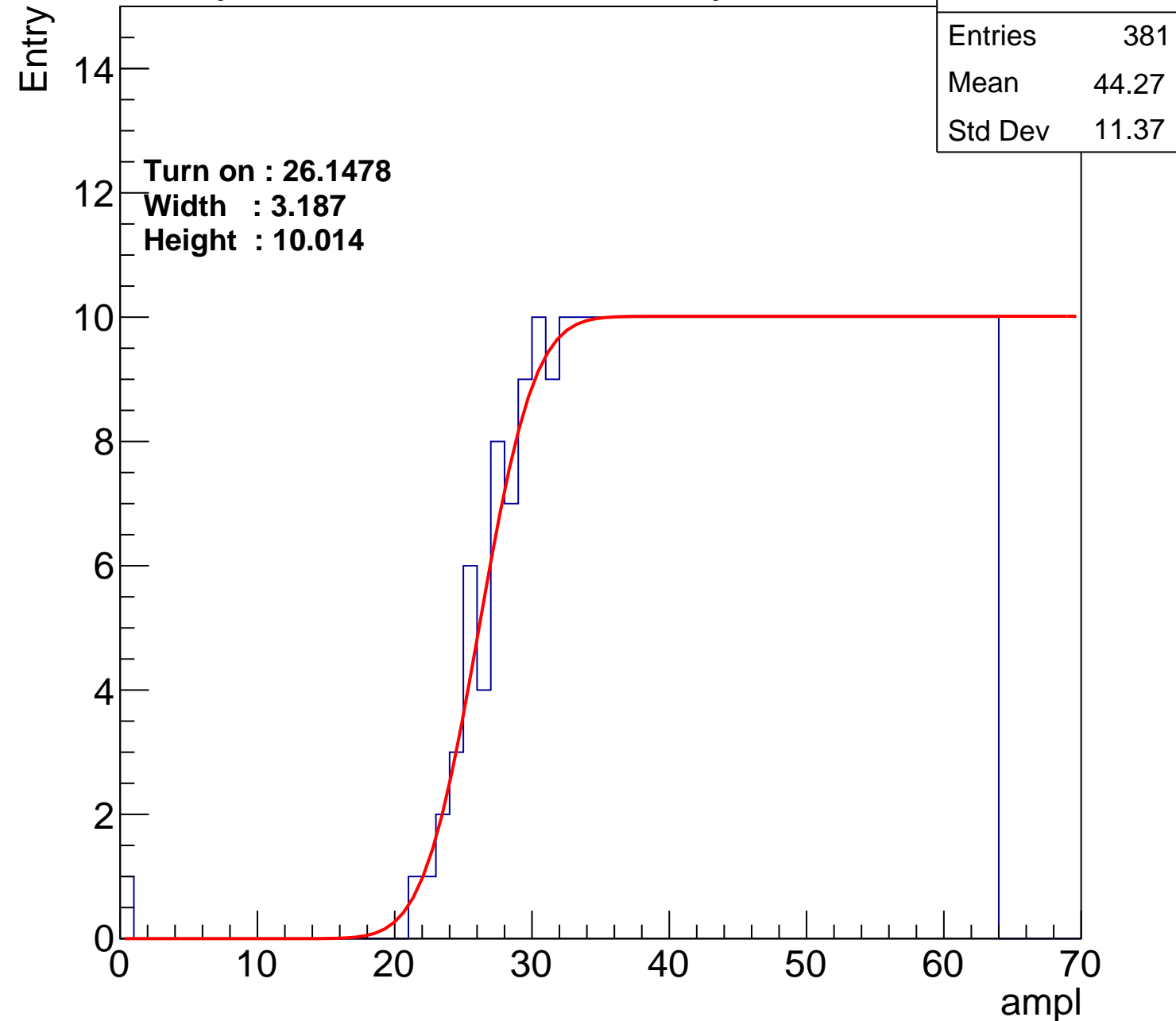
Width : 3.187

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch33

calib_packv5_042523_0143.root, FC#13, port D2

Entries	373
Mean	44.72
Std Dev	11.06

Turn on : 26.8538

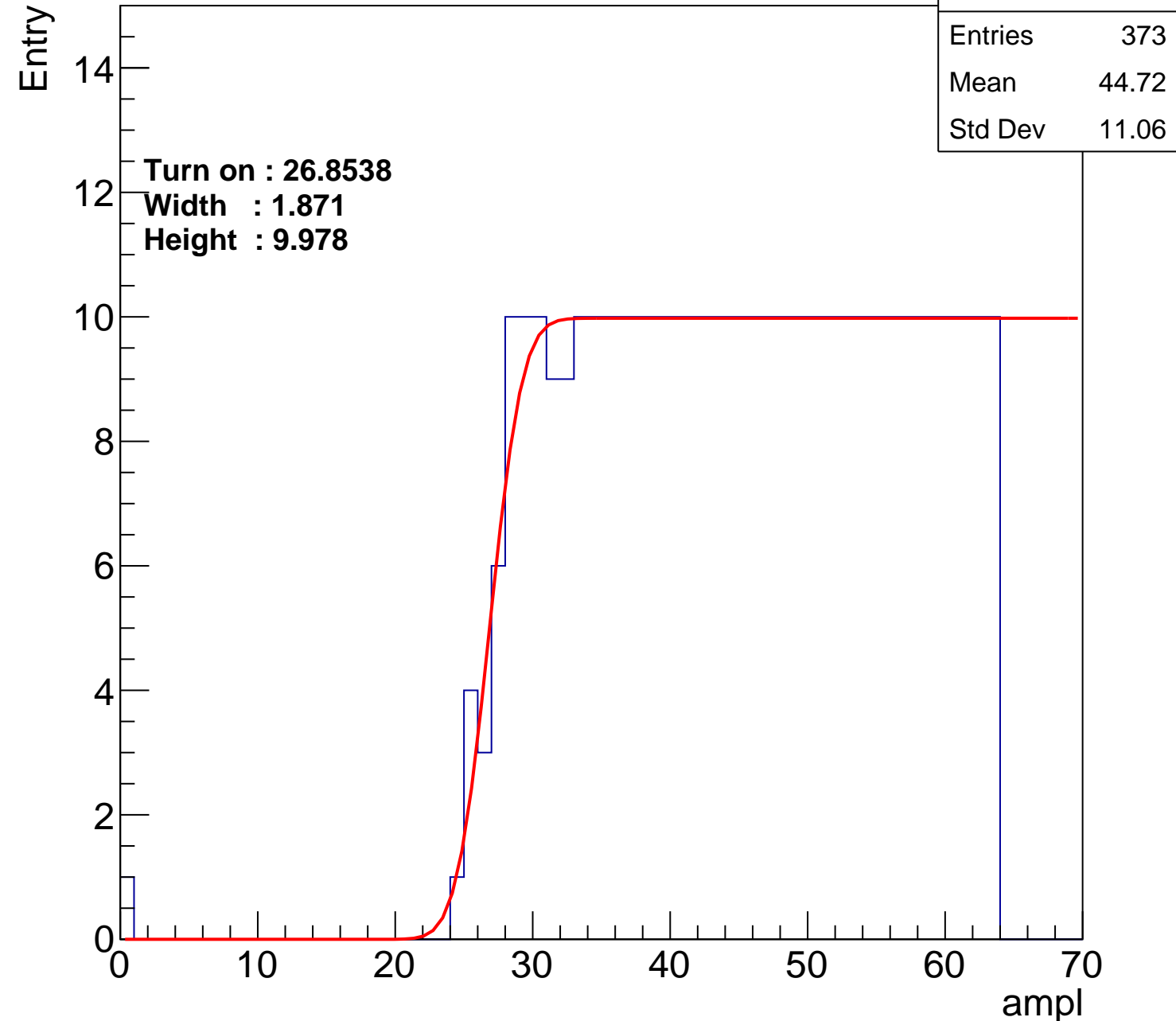
Width : 1.871

Height : 9.978

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch34

calib_packv5_042523_0143.root, FC#13, port D2

Entries	368
Mean	44.64
Std Dev	11.72

Turn on : 28.0759

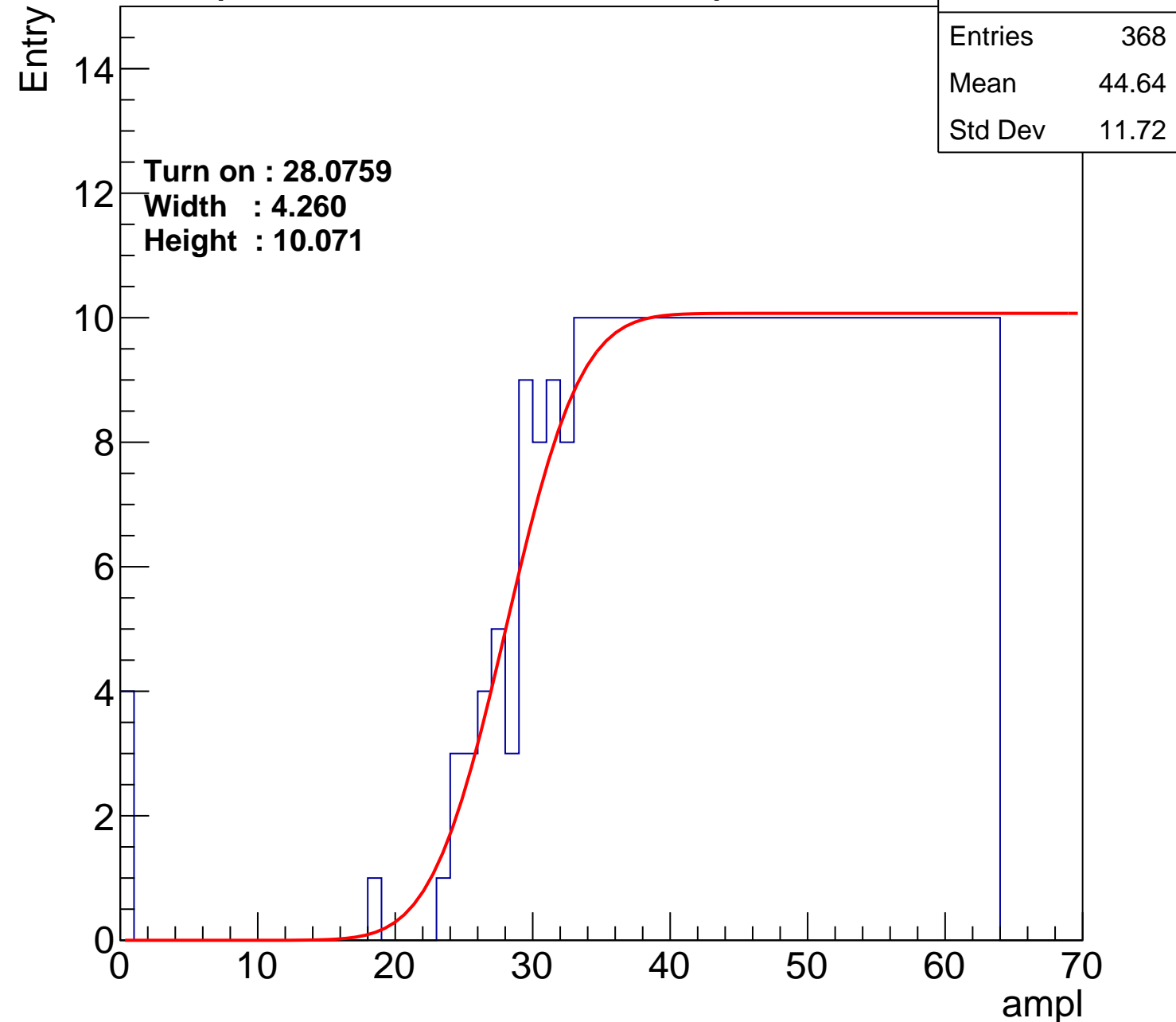
Width : 4.260

Height : 10.071

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch35

calib_packv5_042523_0143.root, FC#13, port D2

Entries	375
Mean	44.45
Std Dev	11.57

Turn on : 27.1416

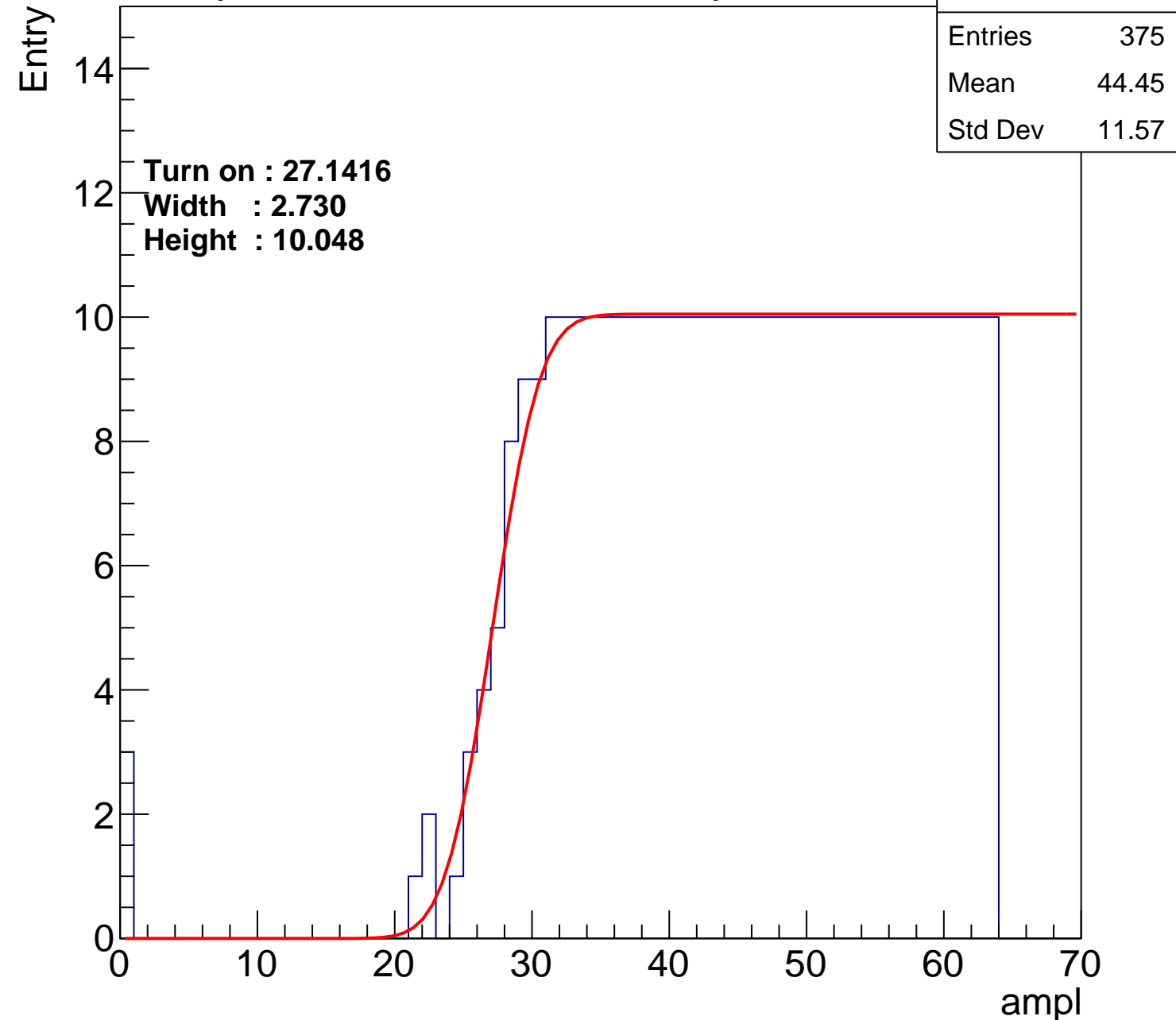
Width : 2.730

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch36

calib_packv5_042523_0143.root, FC#13, port D2

Entries	378
Mean	44.37
Std Dev	11.45

Turn on : 26.4010

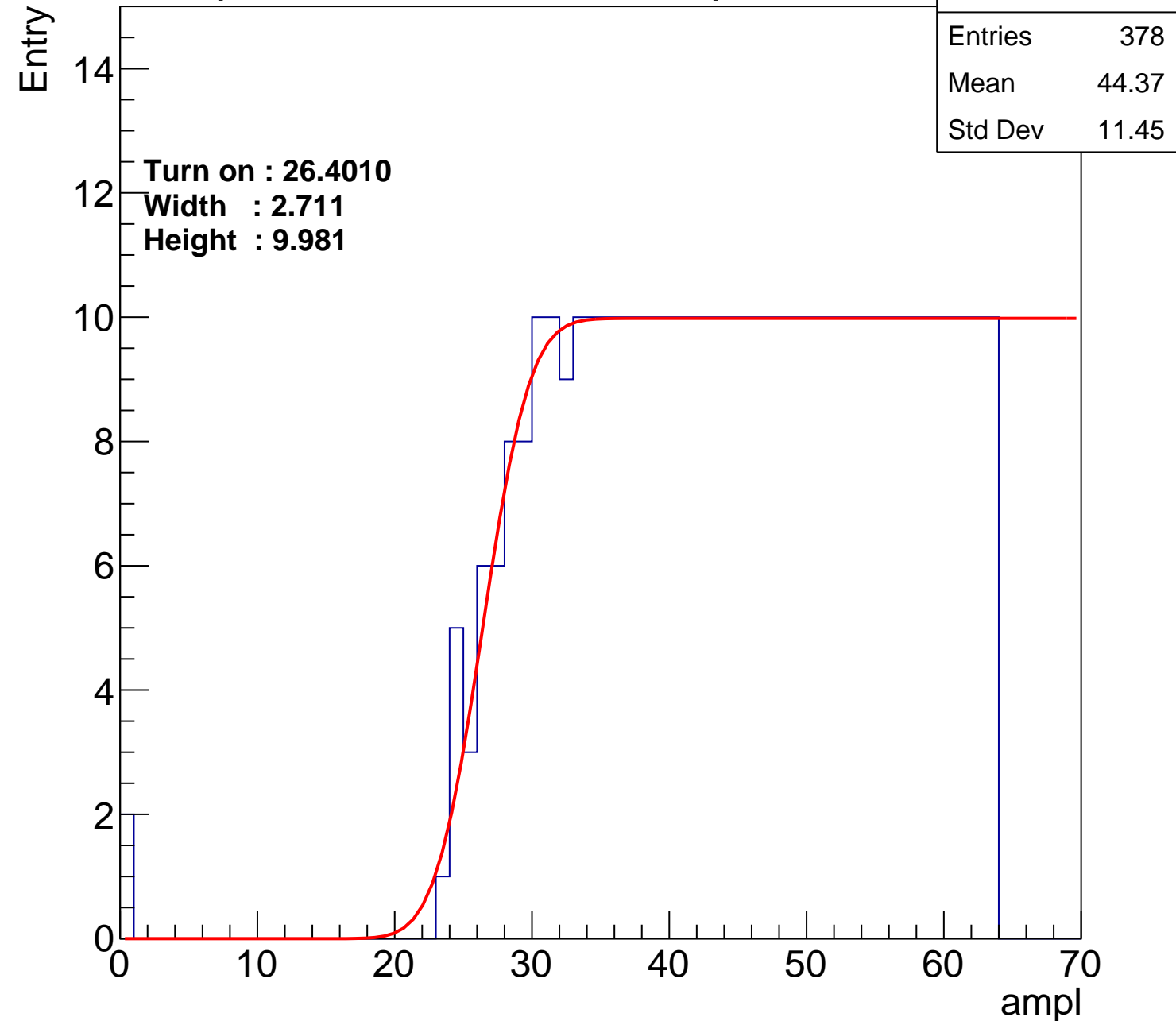
Width : 2.711

Height : 9.981

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch37

calib_packv5_042523_0143.root, FC#13, port D2

Entries	354
Mean	45.51
Std Dev	10.9

Turn on : 28.7514

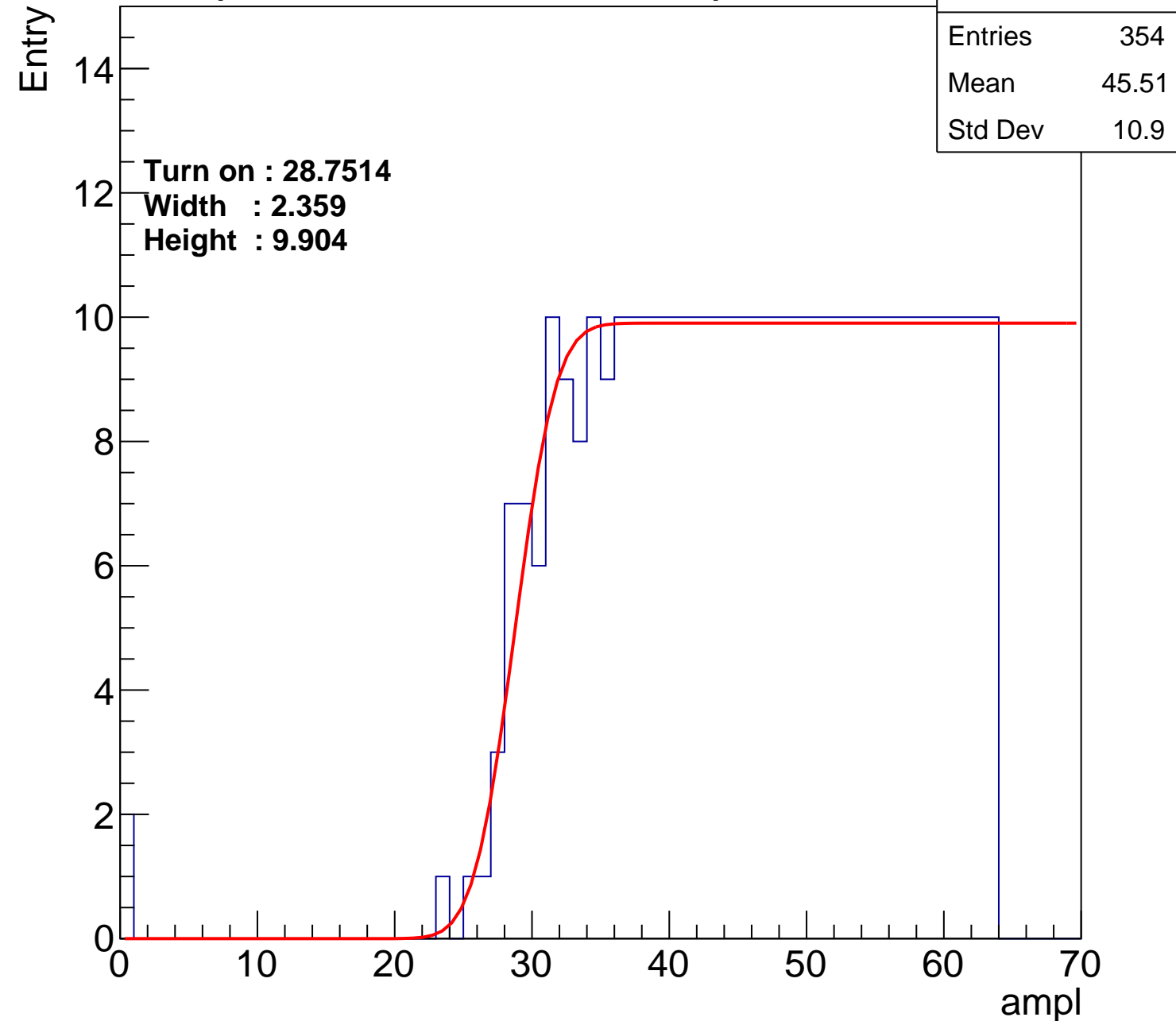
Width : 2.359

Height : 9.904

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch38

calib_packv5_042523_0143.root, FC#13, port D2

Entries	388
Mean	43.87
Std Dev	11.72

Turn on : 25.3291

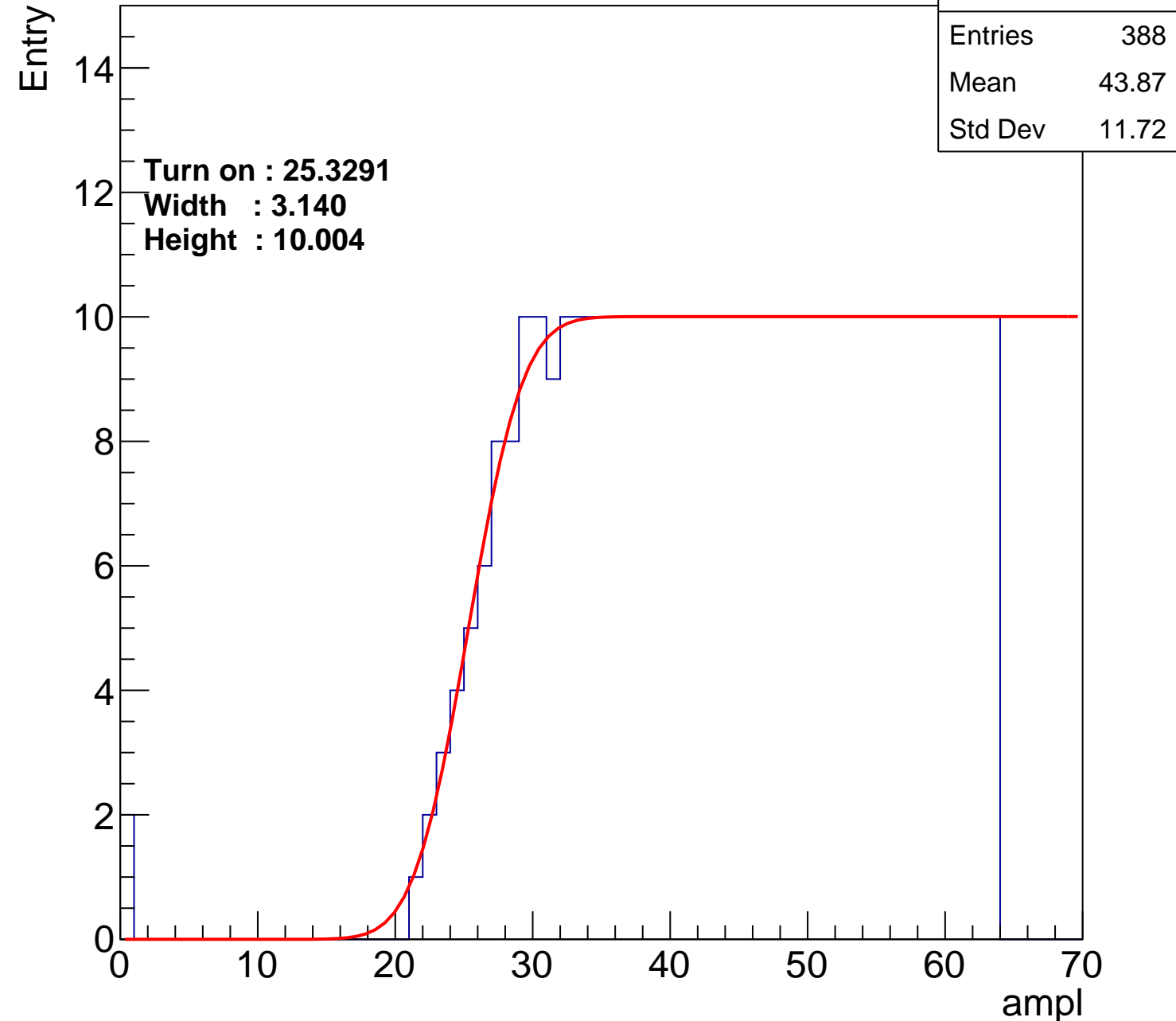
Width : 3.140

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch39

calib_packv5_042523_0143.root, FC#13, port D2

Entries	364
Mean	44.97
Std Dev	11.32

Turn on : 28.0345

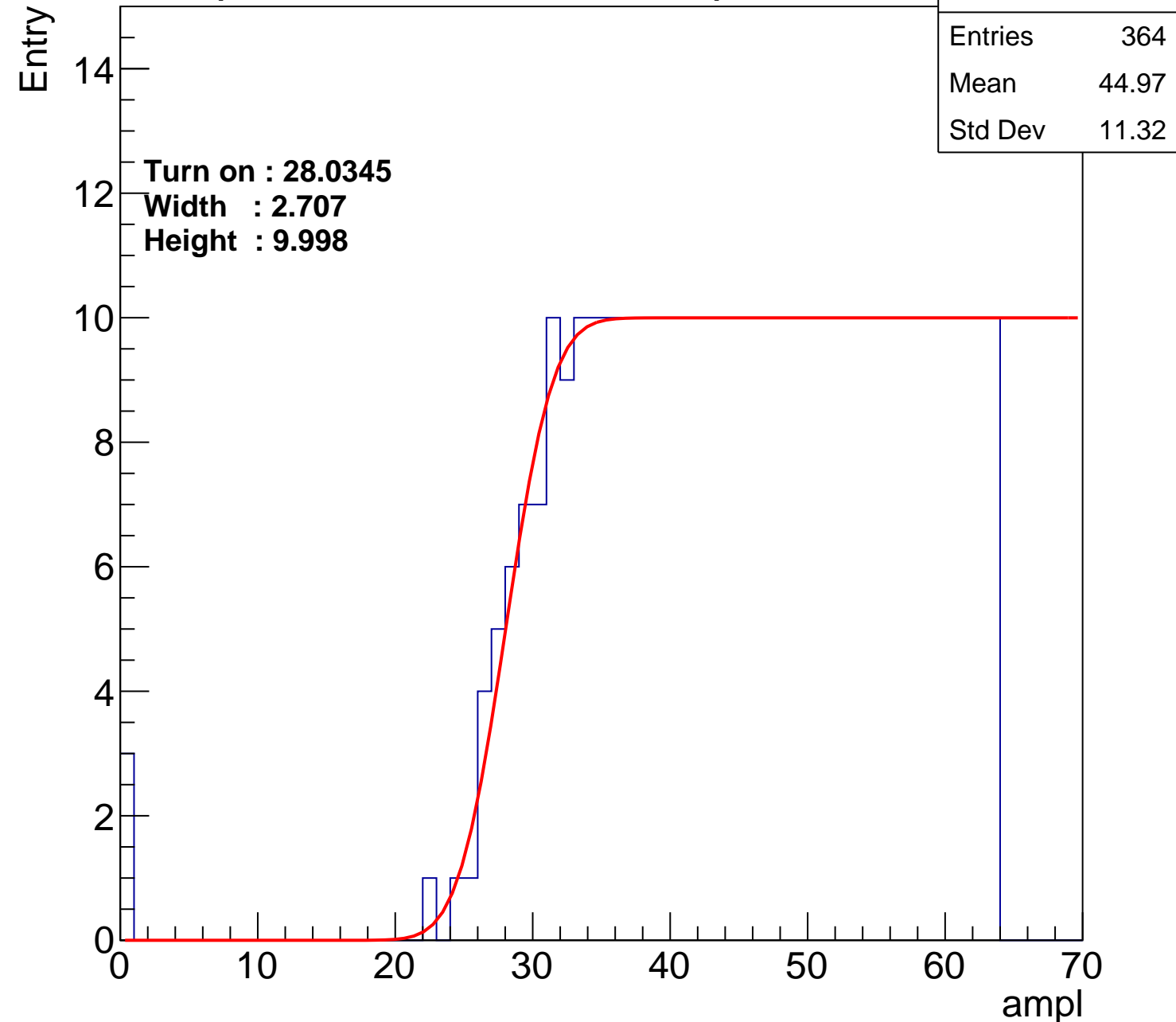
Width : 2.707

Height : 9.998

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch40

calib_packv5_042523_0143.root, FC#13, port D2

Entries	382
Mean	43.96
Std Dev	12.1

Turn on : 26.2987

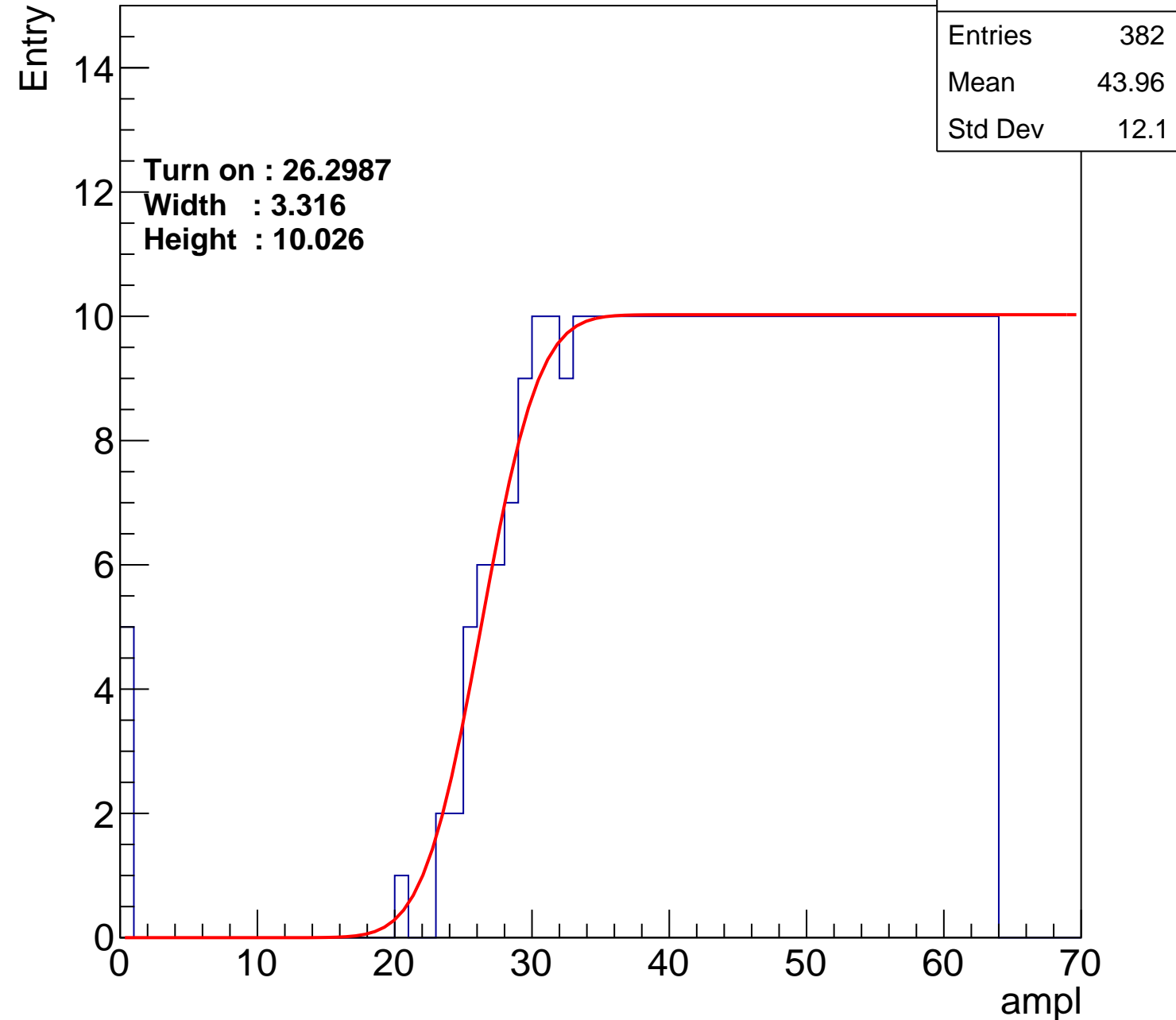
Width : 3.316

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch41

calib_packv5_042523_0143.root, FC#13, port D2

Entries	370
Mean	44.74
Std Dev	11.29

Turn on : 27.3899

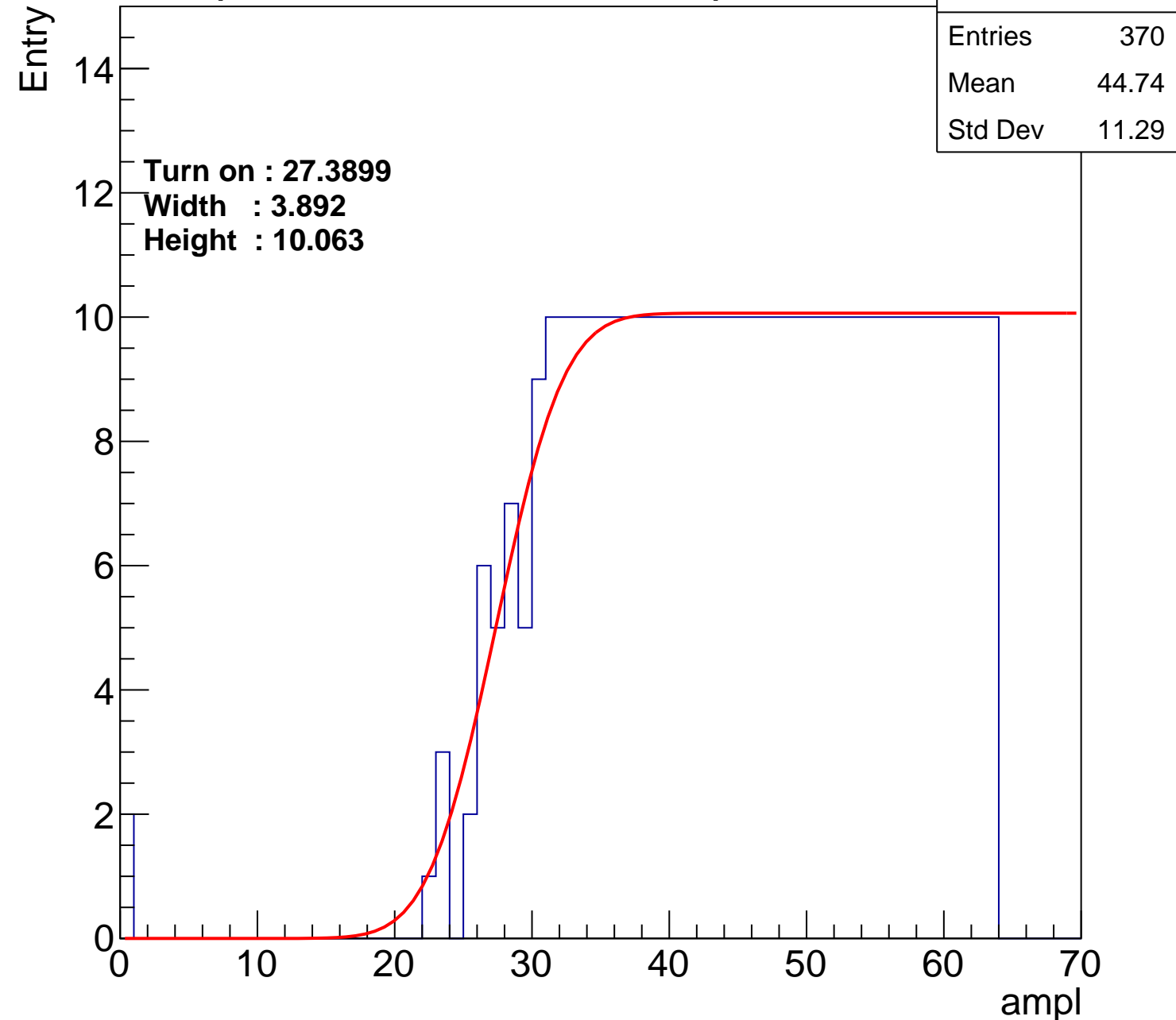
Width : 3.892

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch42

calib_packv5_042523_0143.root, FC#13, port D2

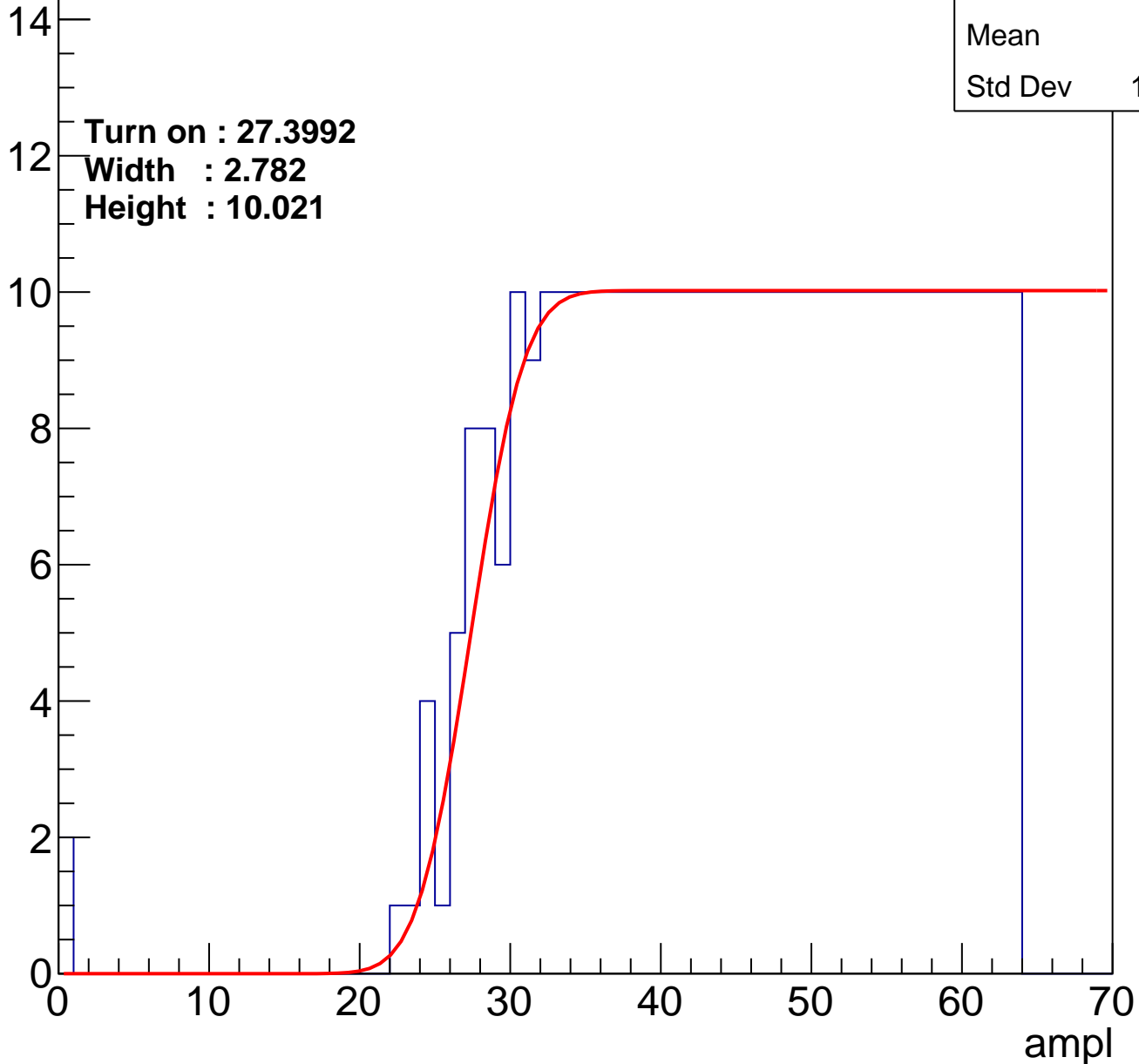
Entries	375
Mean	44.5
Std Dev	11.39

Turn on : 27.3992

Width : 2.782

Height : 10.021

Entry



B1L003S, U1-ch43

calib_packv5_042523_0143.root, FC#13, port D2

Entries	394
Mean	43.25
Std Dev	12.69

Turn on : 25.6970

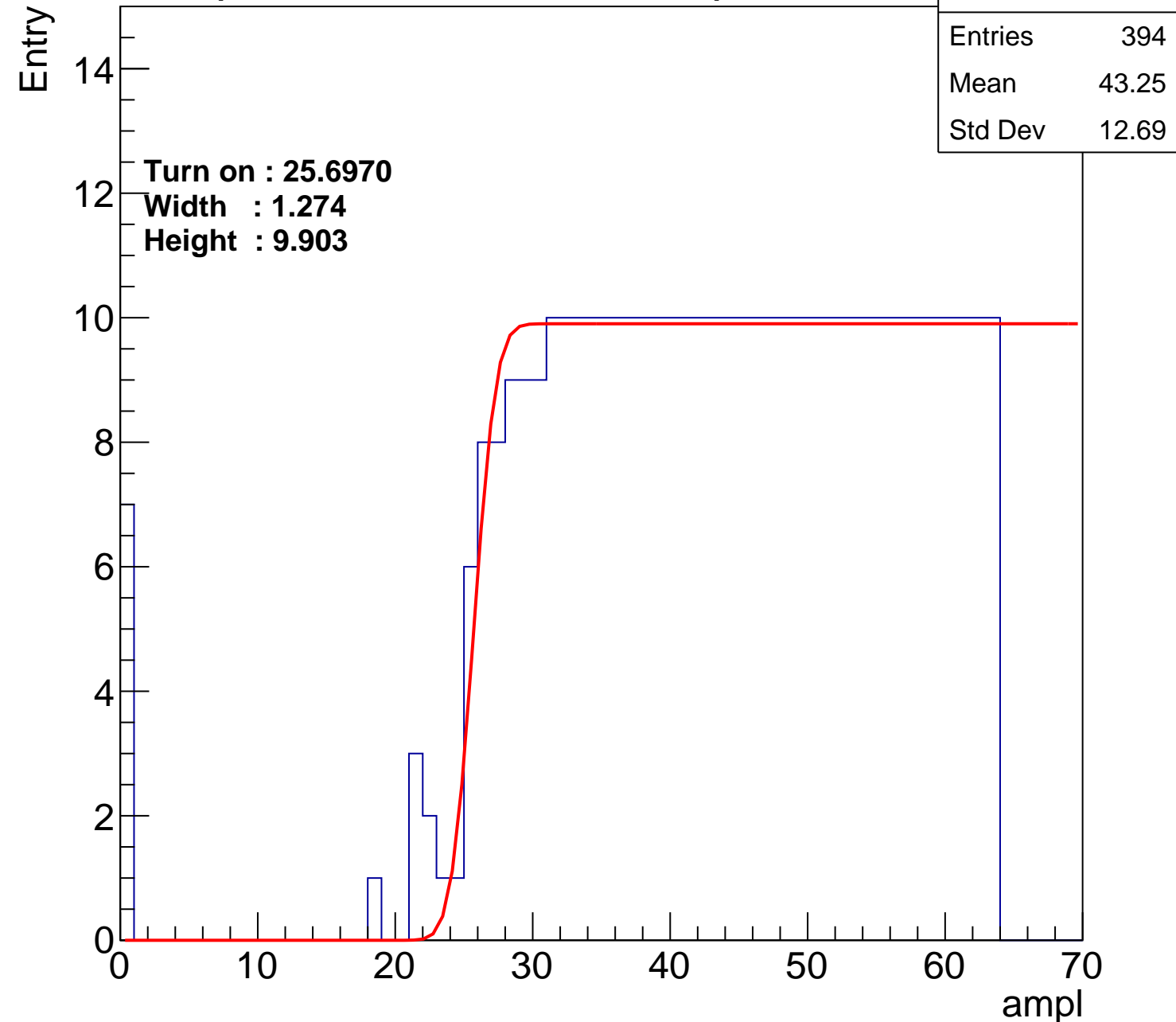
Width : 1.274

Height : 9.903

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch44

calib_packv5_042523_0143.root, FC#13, port D2

Entries	367
Mean	44.73
Std Dev	11.63

Turn on : 28.1110

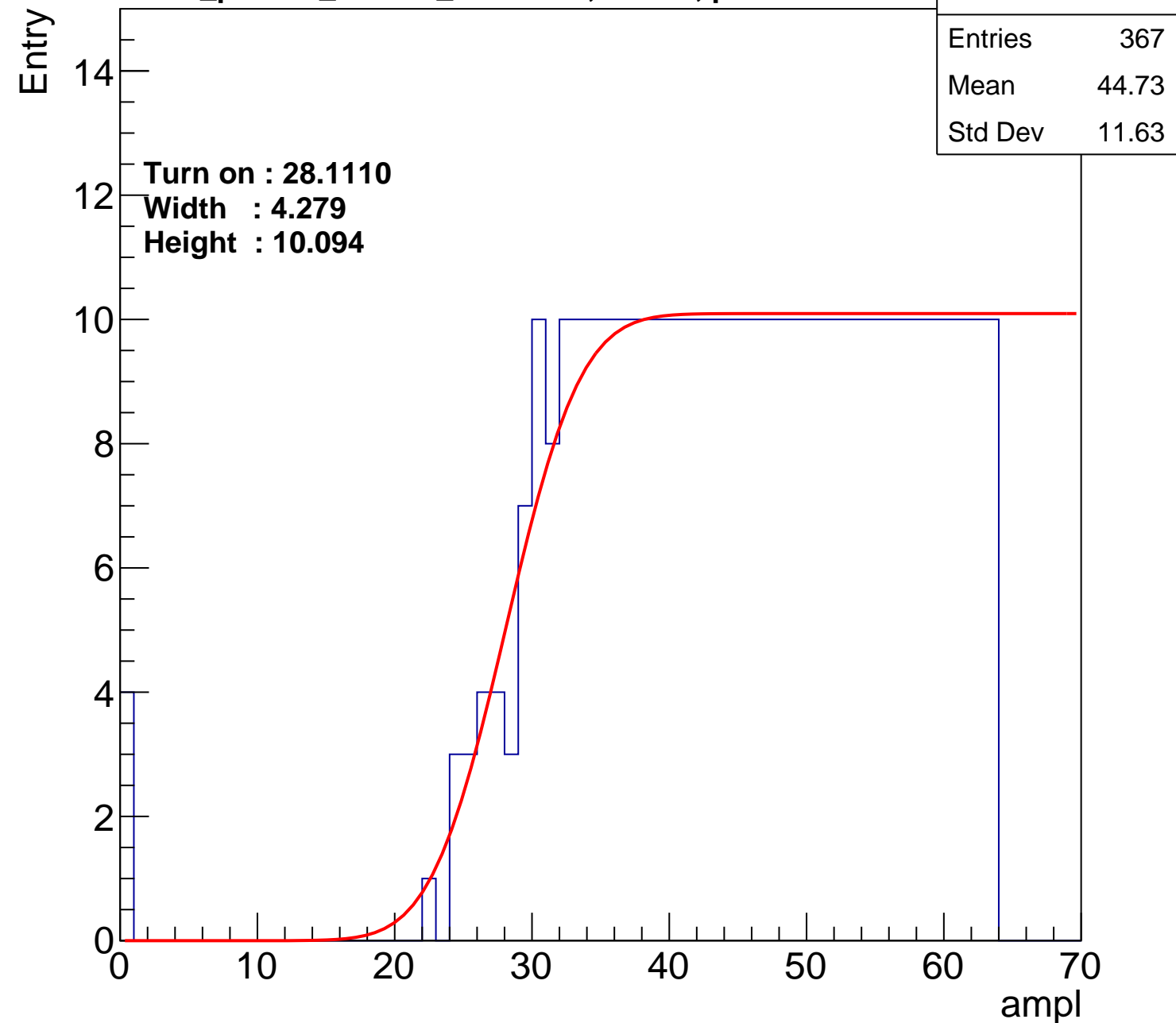
Width : 4.279

Height : 10.094

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch45

calib_packv5_042523_0143.root, FC#13, port D2

Entries	365
Mean	44.87
Std Dev	11.52

Turn on : 27.8782

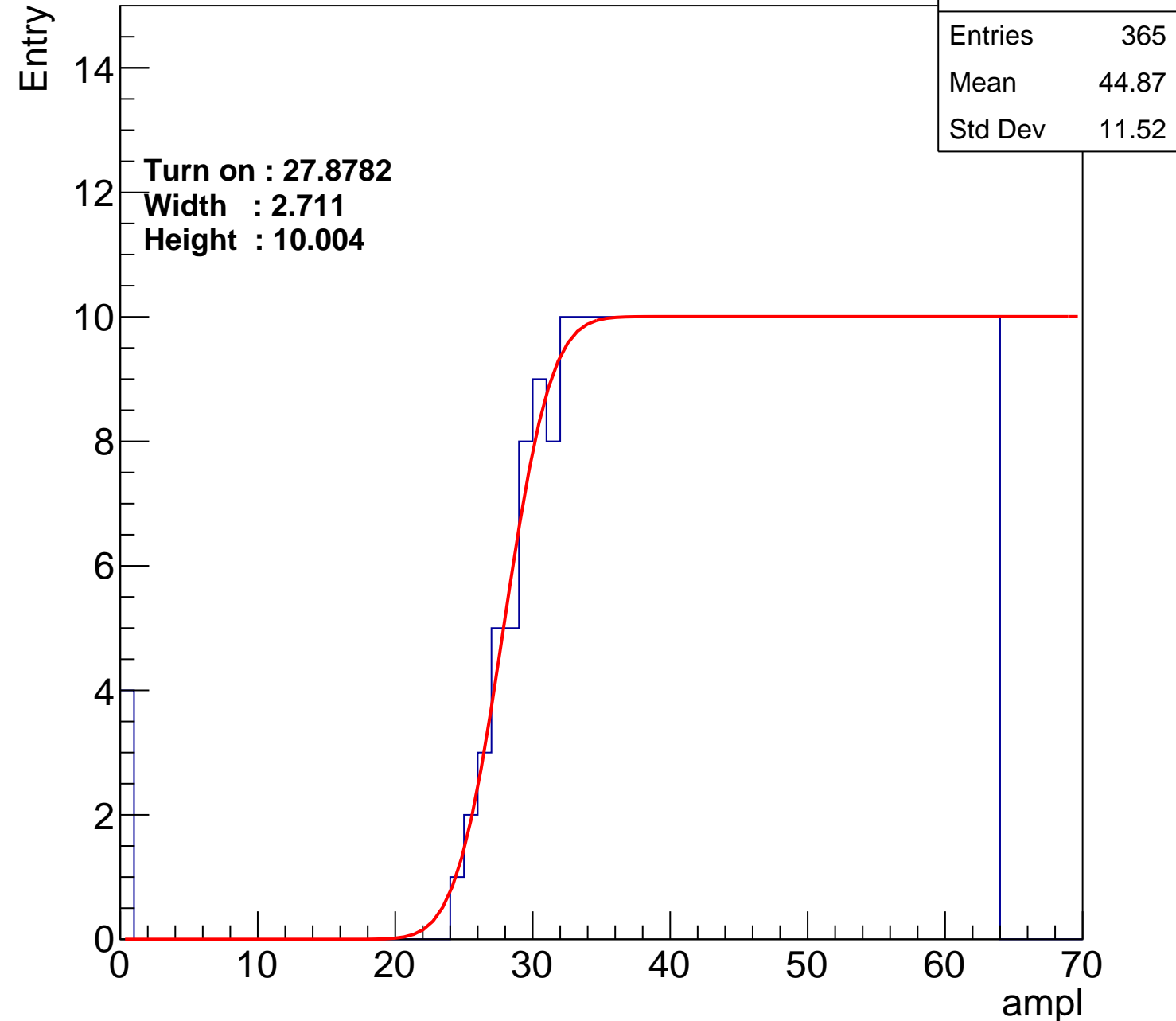
Width : 2.711

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch46

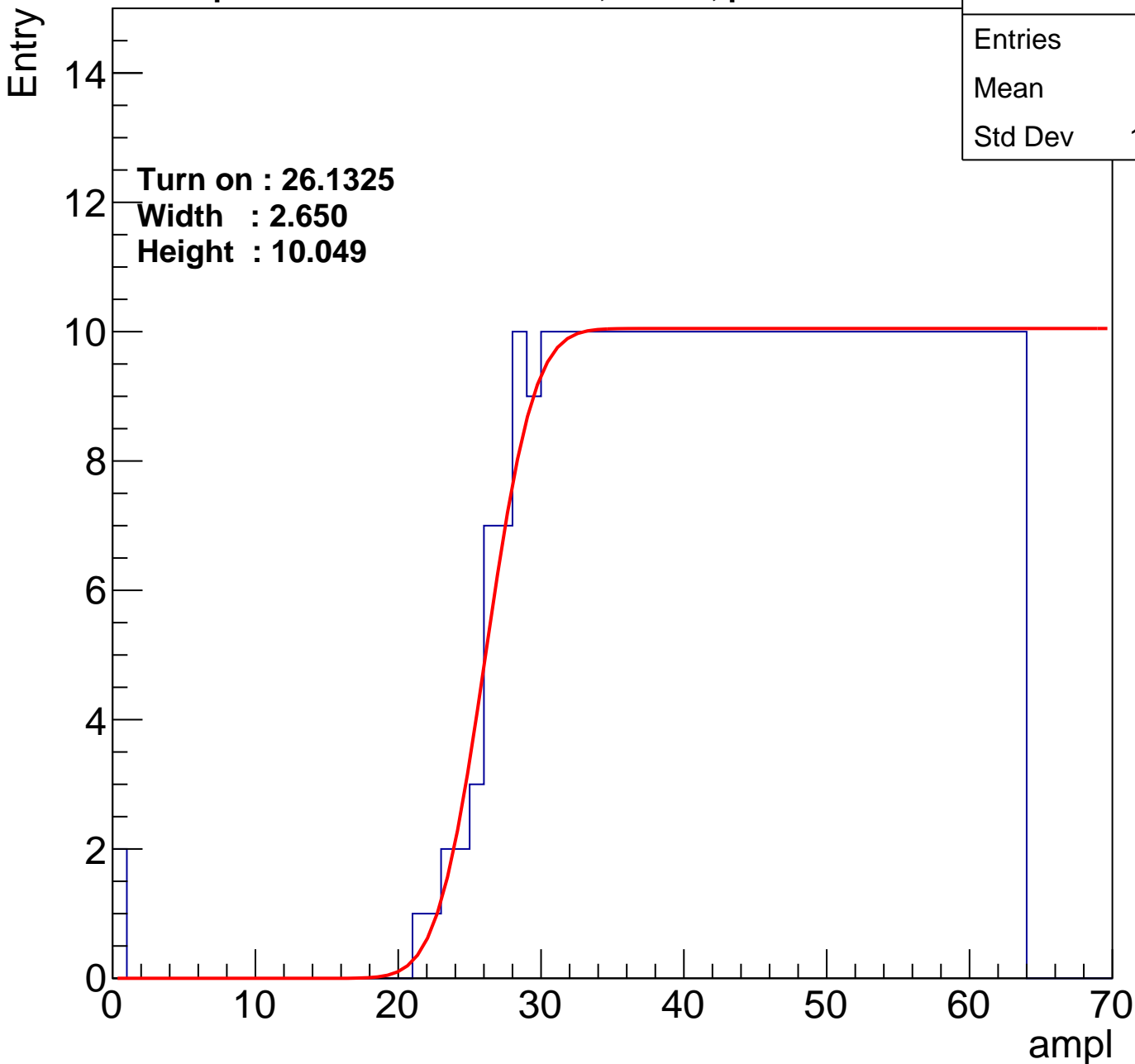
calib_packv5_042523_0143.root, FC#13, port D2

Entries	384
Mean	44.1
Std Dev	11.57

Turn on : 26.1325

Width : 2.650

Height : 10.049



B1L003S, U1-ch47

calib_packv5_042523_0143.root, FC#13, port D2

Entries	376
Mean	44.44
Std Dev	11.45

Turn on : 26.5699

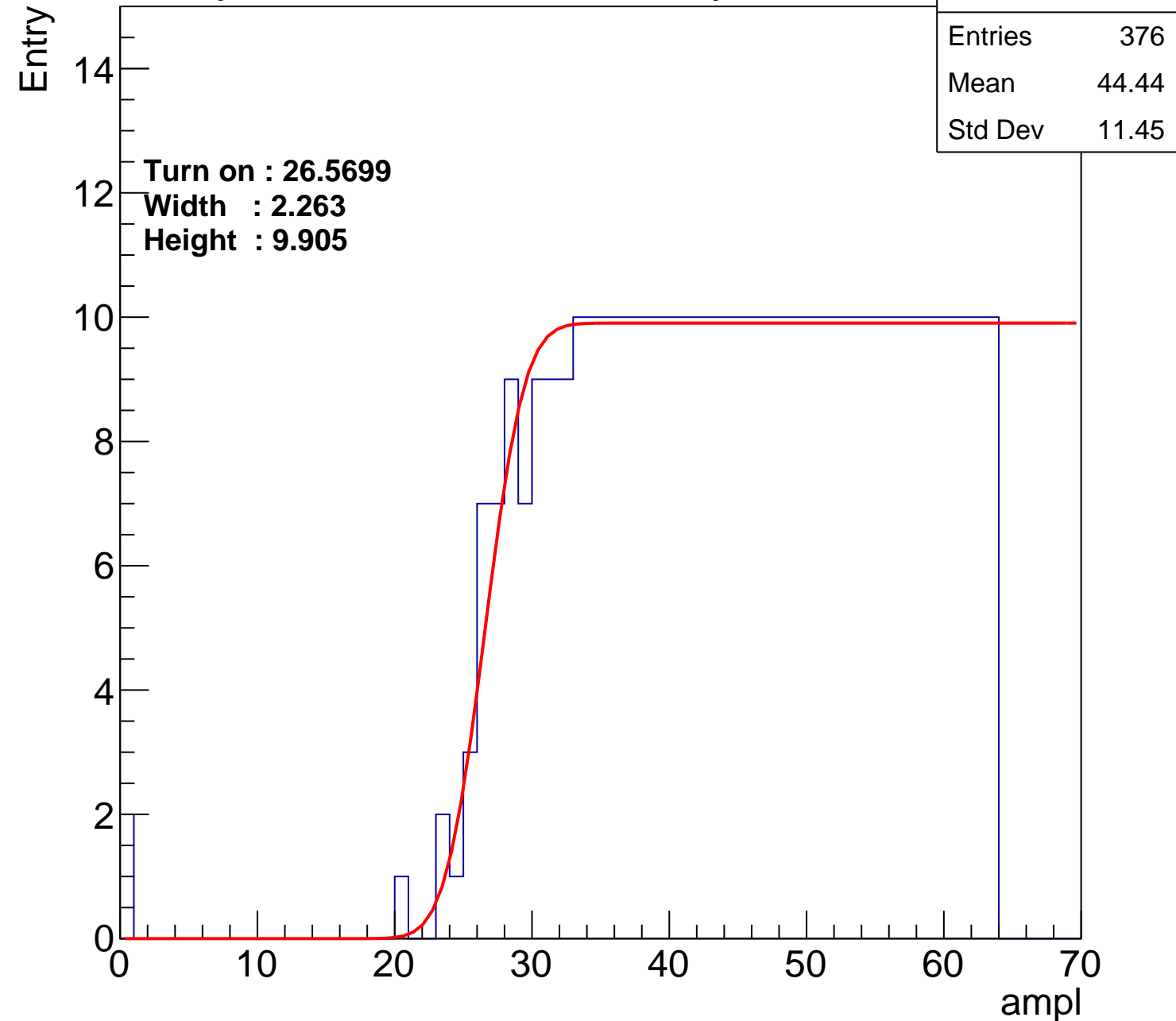
Width : 2.263

Height : 9.905

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch48

calib_packv5_042523_0143.root, FC#13, port D2

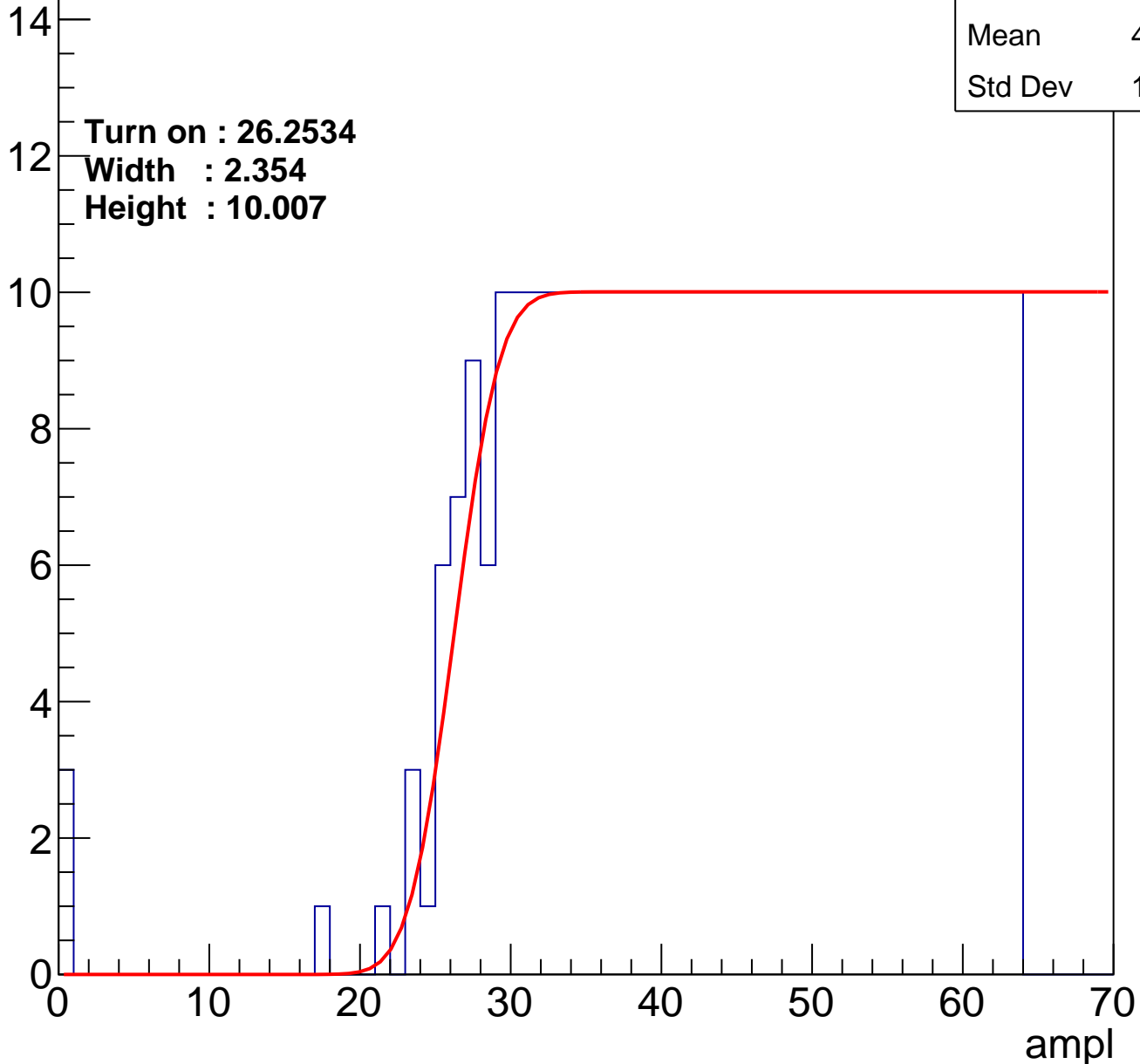
Entries	387
Mean	43.86
Std Dev	11.86

Turn on : 26.2534

Width : 2.354

Height : 10.007

Entry



B1L003S, U1-ch49

calib_packv5_042523_0143.root, FC#13, port D2

Entries	386
Mean	43.89
Std Dev	11.86

Turn on : 26.1667

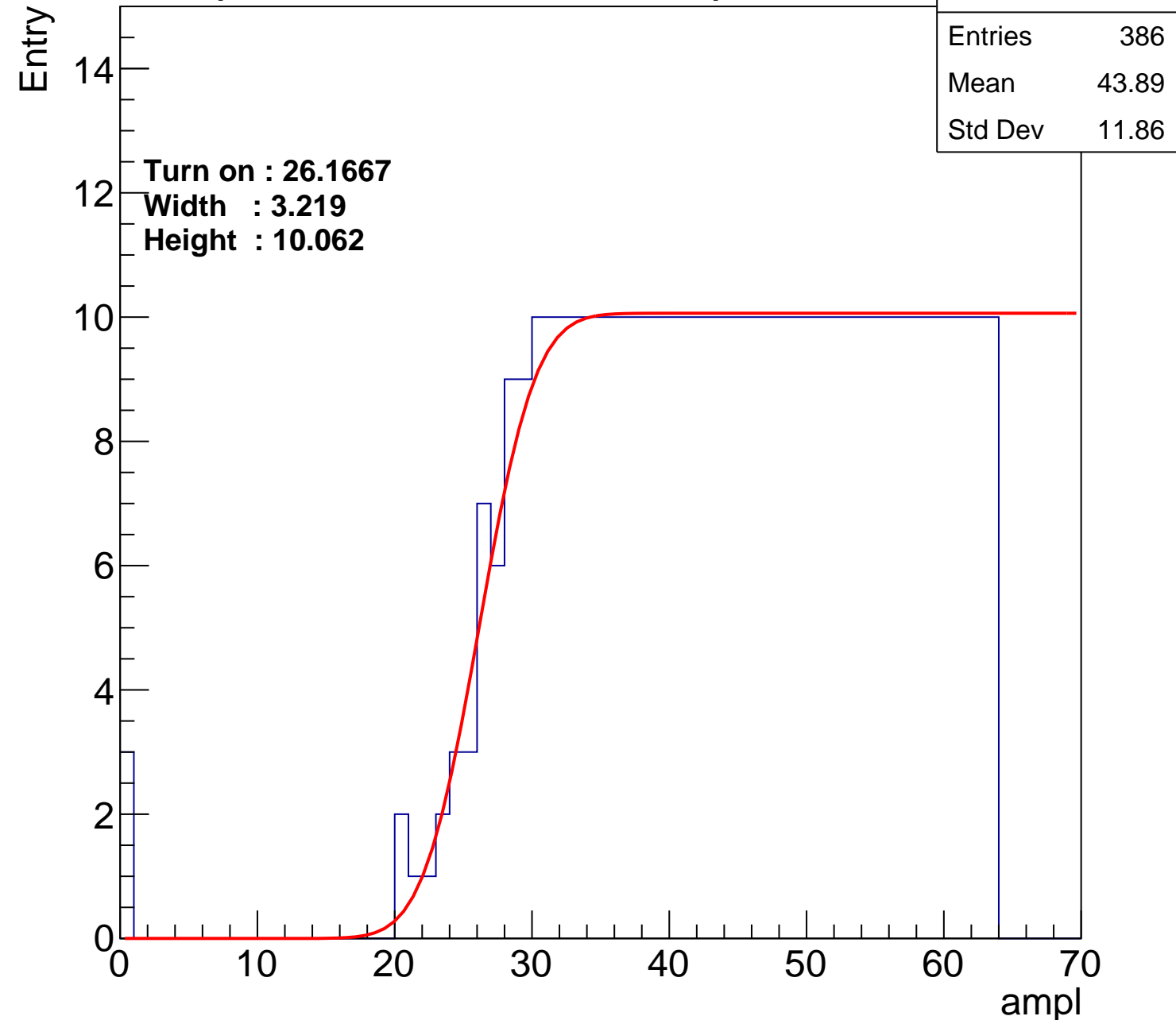
Width : 3.219

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch50

calib_packv5_042523_0143.root, FC#13, port D2

Entries	369
Mean	44.84
Std Dev	11.17

Turn on : 27.4735

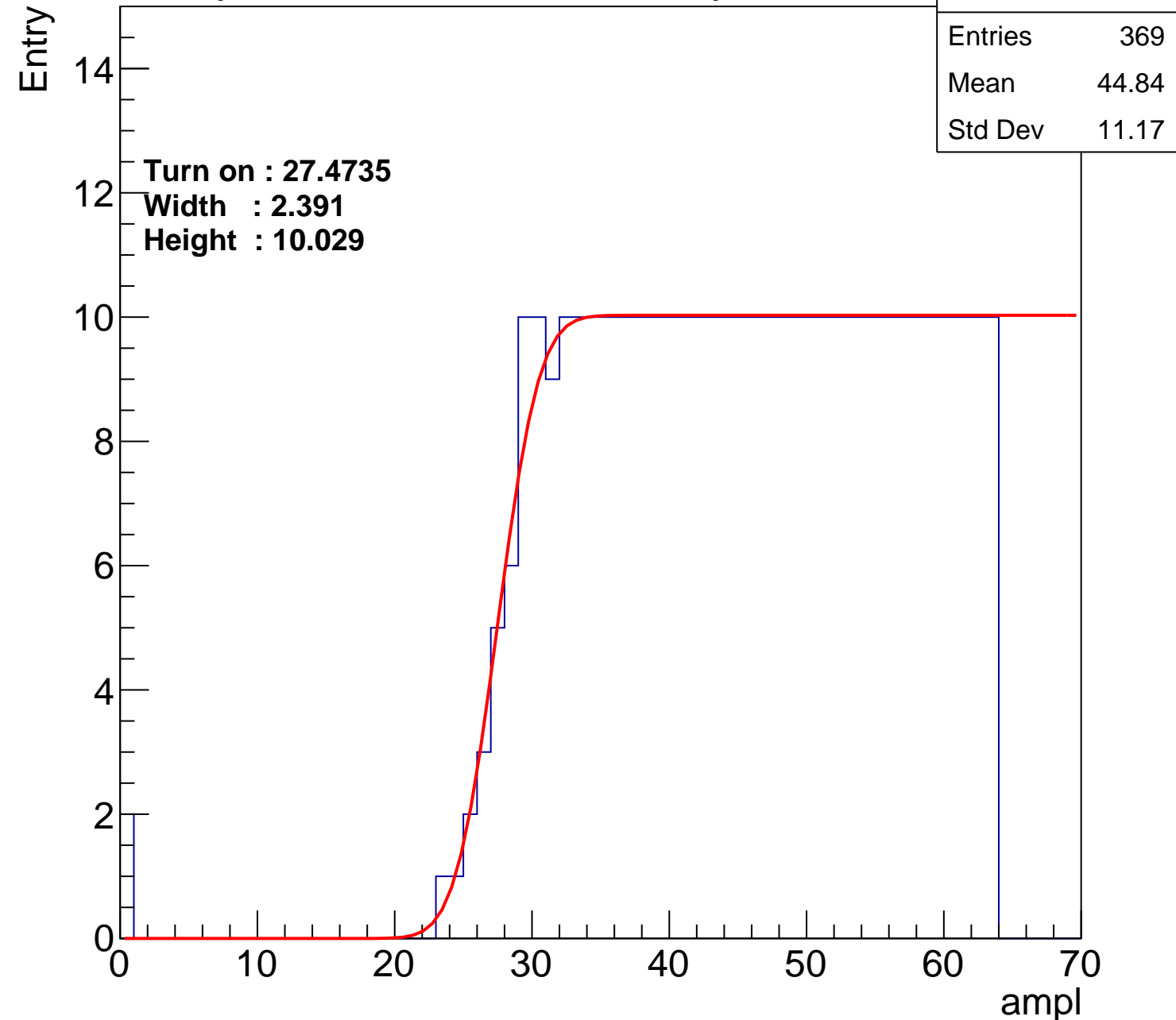
Width : 2.391

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch51

calib_packv5_042523_0143.root, FC#13, port D2

Entries	364
Mean	45.15
Std Dev	10.85

Turn on : 27.5639

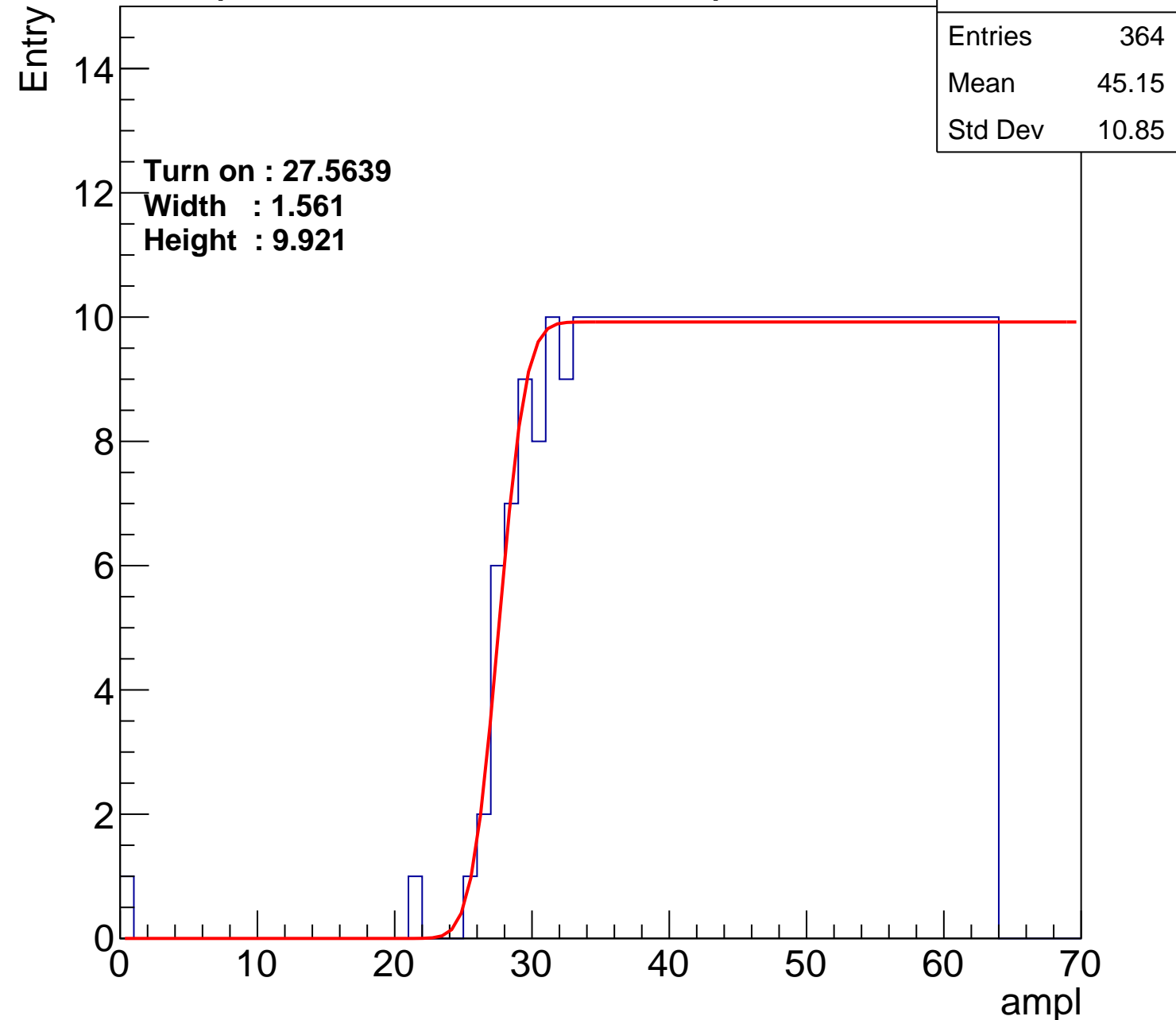
Width : 1.561

Height : 9.921

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch52

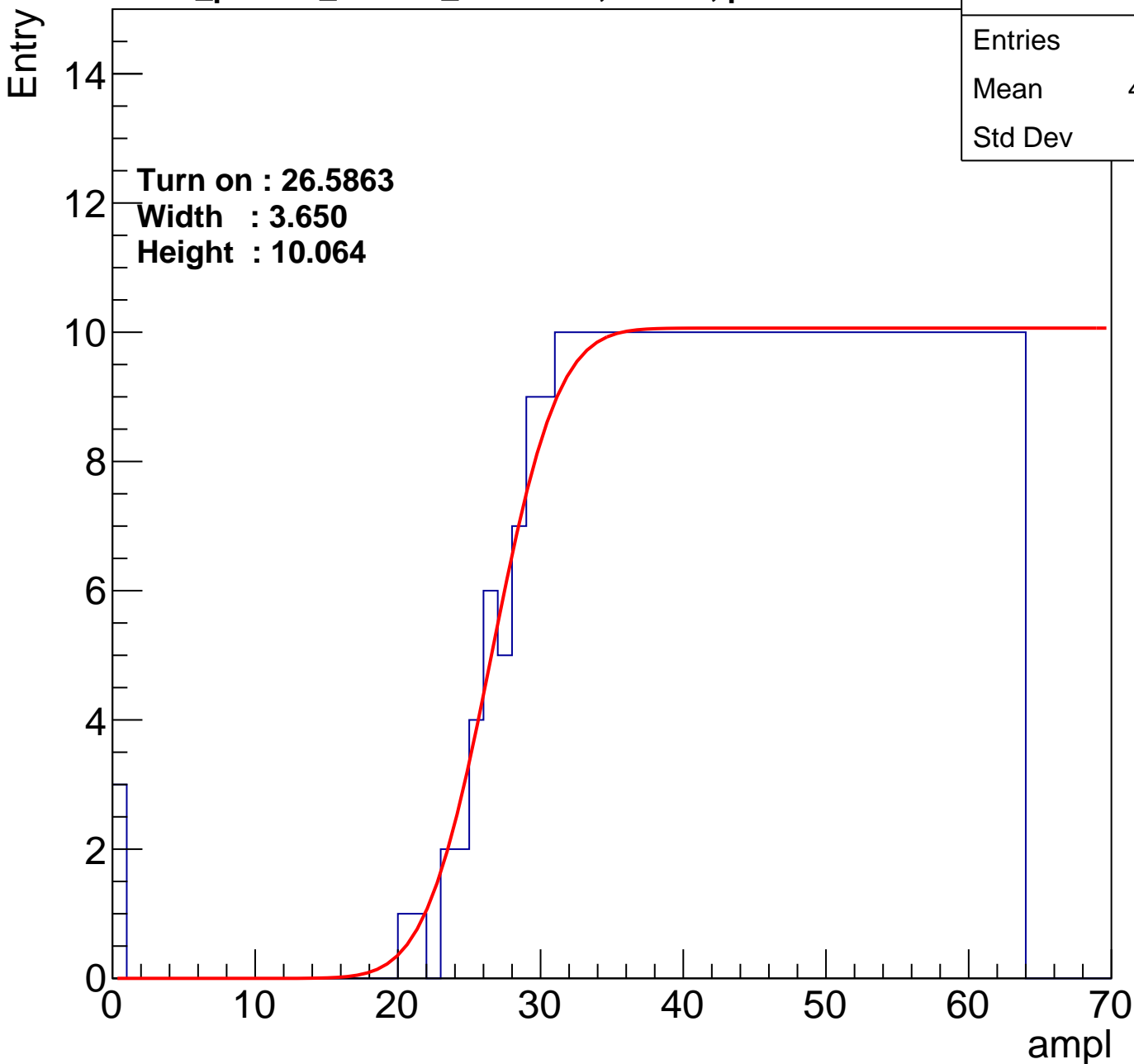
calib_packv5_042523_0143.root, FC#13, port D2

Entries	379
Mean	44.23
Std Dev	11.7

Turn on : 26.5863

Width : 3.650

Height : 10.064



B1L003S, U1-ch53

calib_packv5_042523_0143.root, FC#13, port D2

Entries	361
Mean	45.07
Std Dev	11.42

Turn on : 28.5278

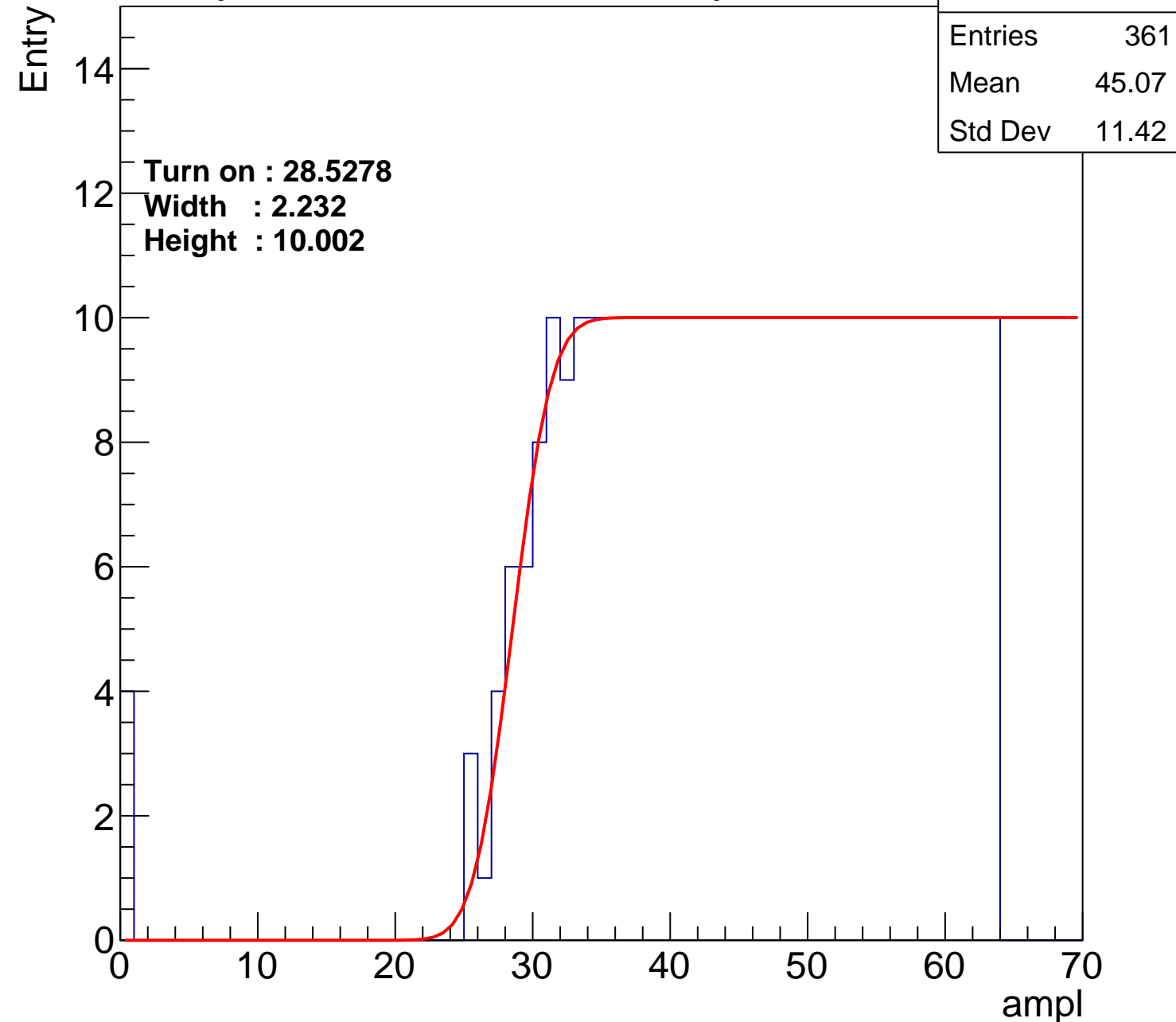
Width : 2.232

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch54

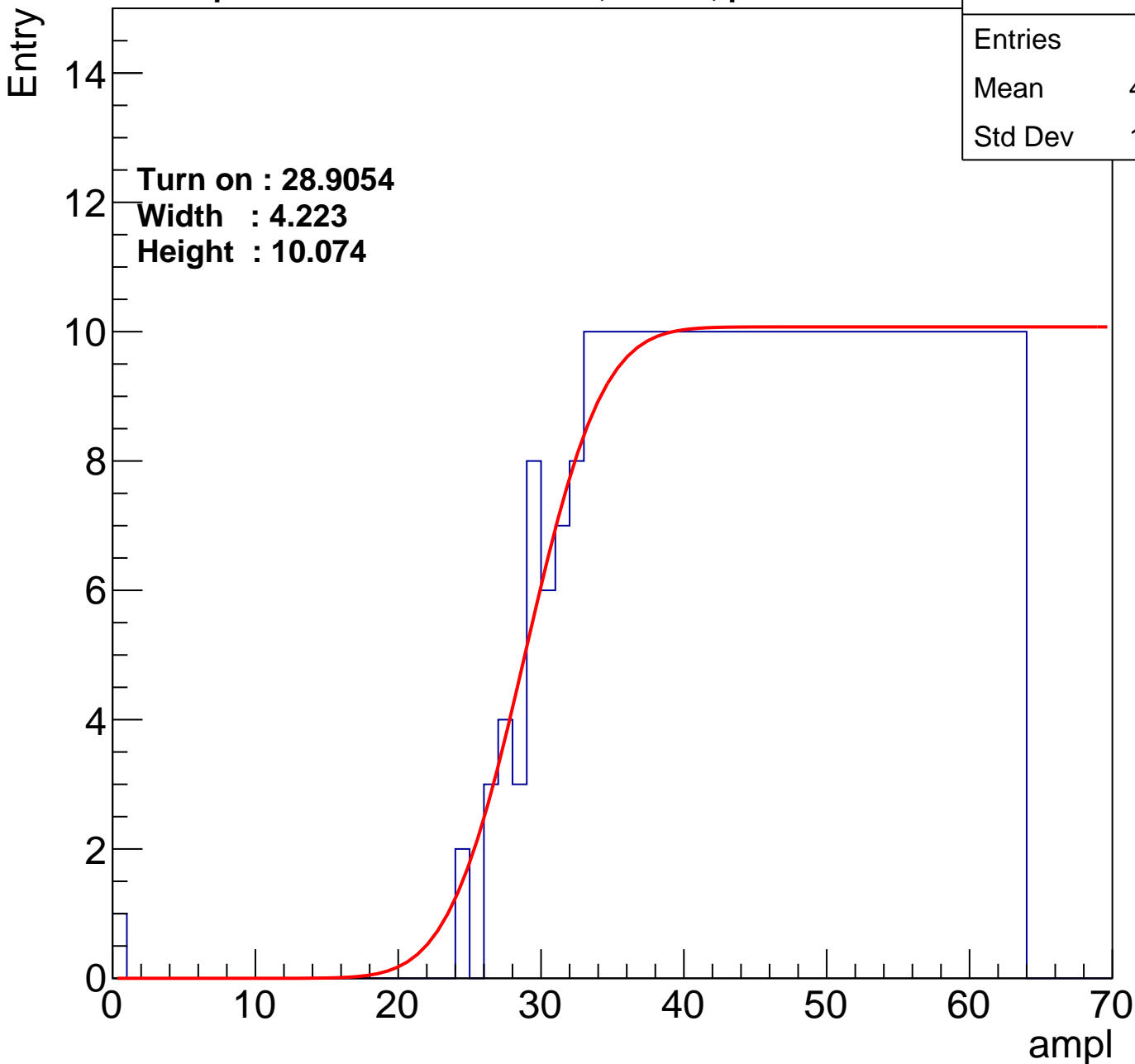
calib_packv5_042523_0143.root, FC#13, port D2

Entries	352
Mean	45.69
Std Dev	10.62

Turn on : 28.9054

Width : 4.223

Height : 10.074



B1L003S, U1-ch55

calib_packv5_042523_0143.root, FC#13, port D2

Entries	378
Mean	44.37
Std Dev	11.37

Turn on : 26.1854

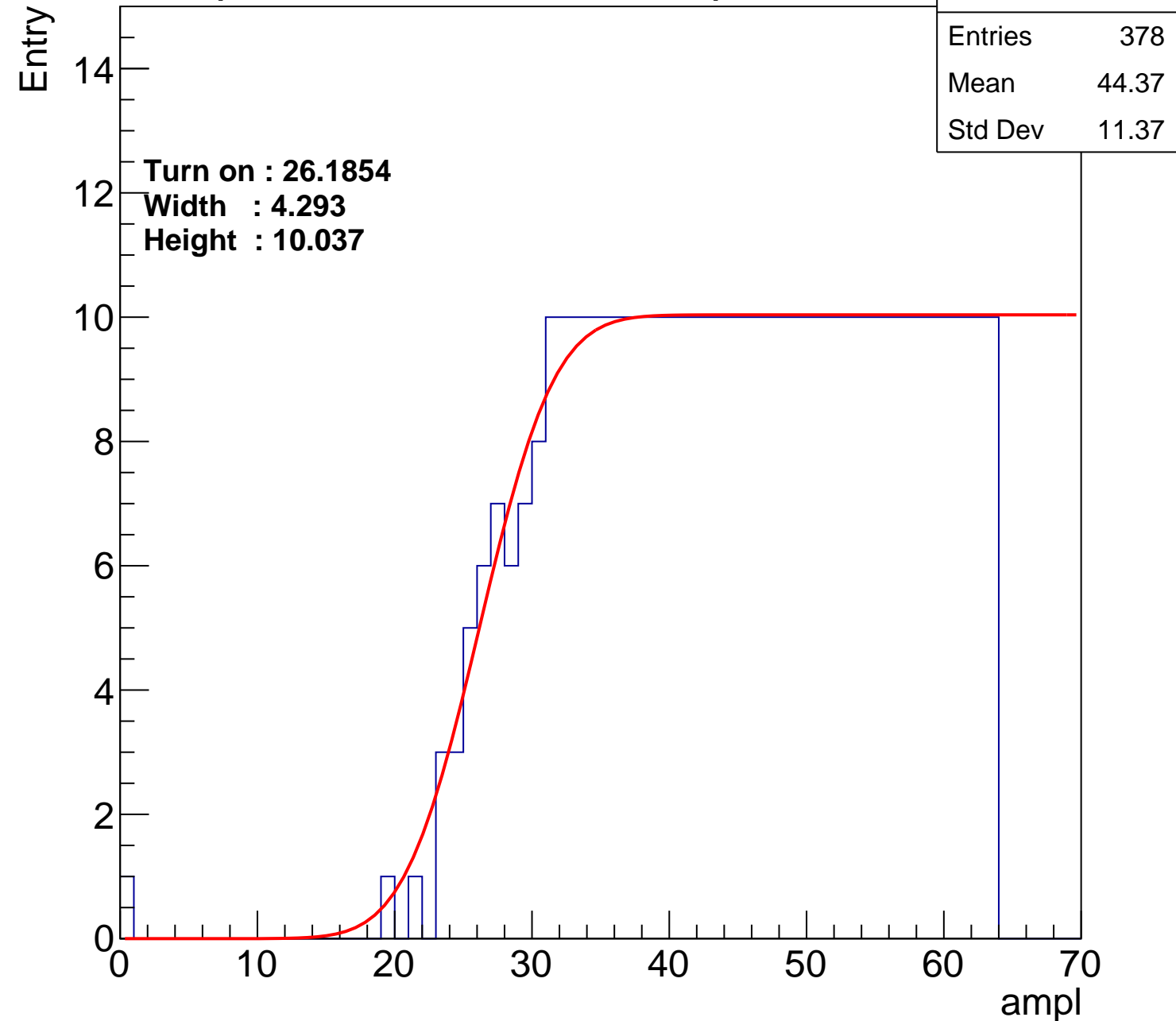
Width : 4.293

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch56

calib_packv5_042523_0143.root, FC#13, port D2

Entries	371
Mean	44.77
Std Dev	11.09

Turn on : 27.4623

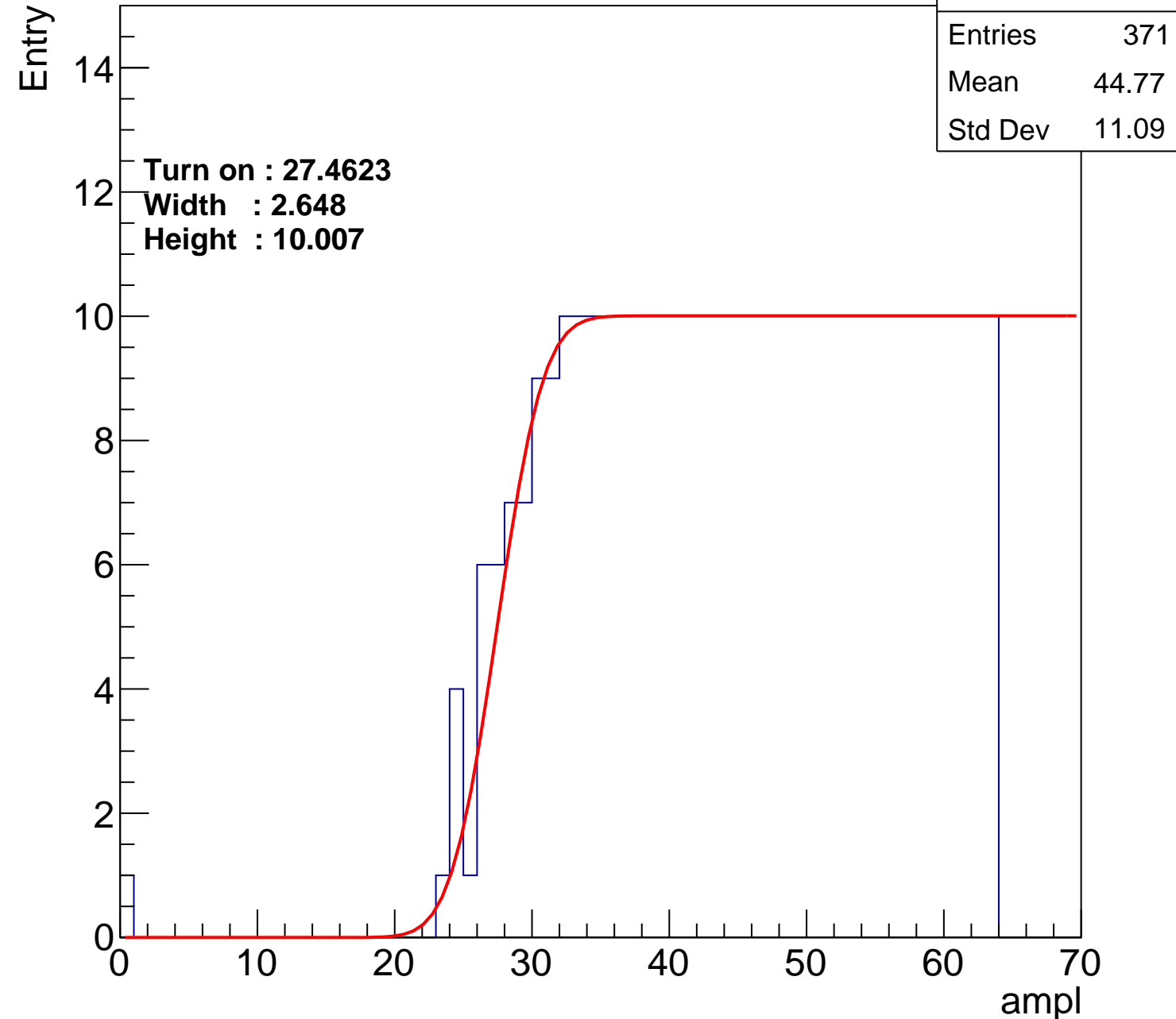
Width : 2.648

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch57

calib_packv5_042523_0143.root, FC#13, port D2

Entries	378
Mean	44.14
Std Dev	12.03

Turn on : 27.0395

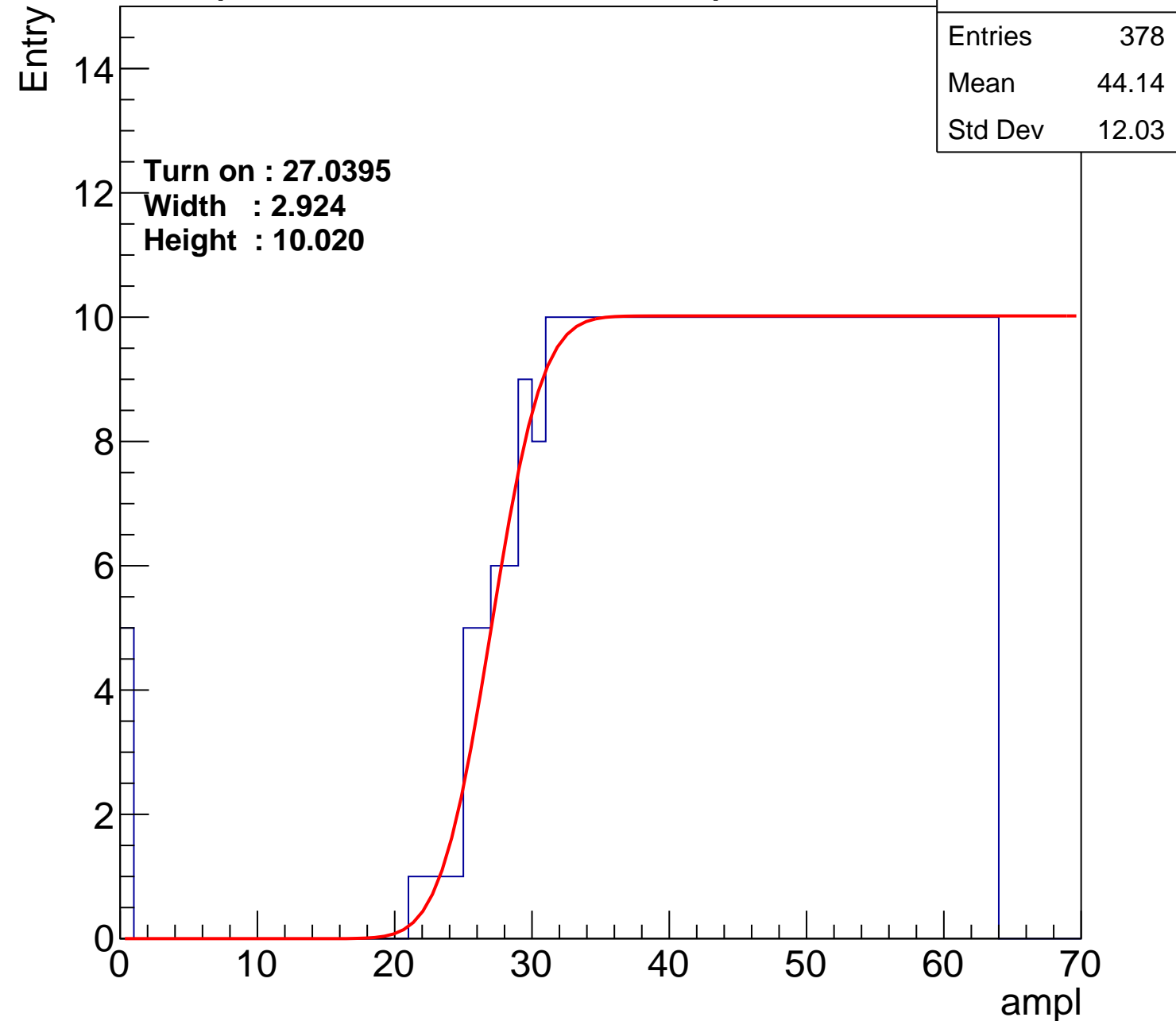
Width : 2.924

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch58

calib_packv5_042523_0143.root, FC#13, port D2

Entries	391
Mean	43.76
Std Dev	11.66

Turn on : 25.7183

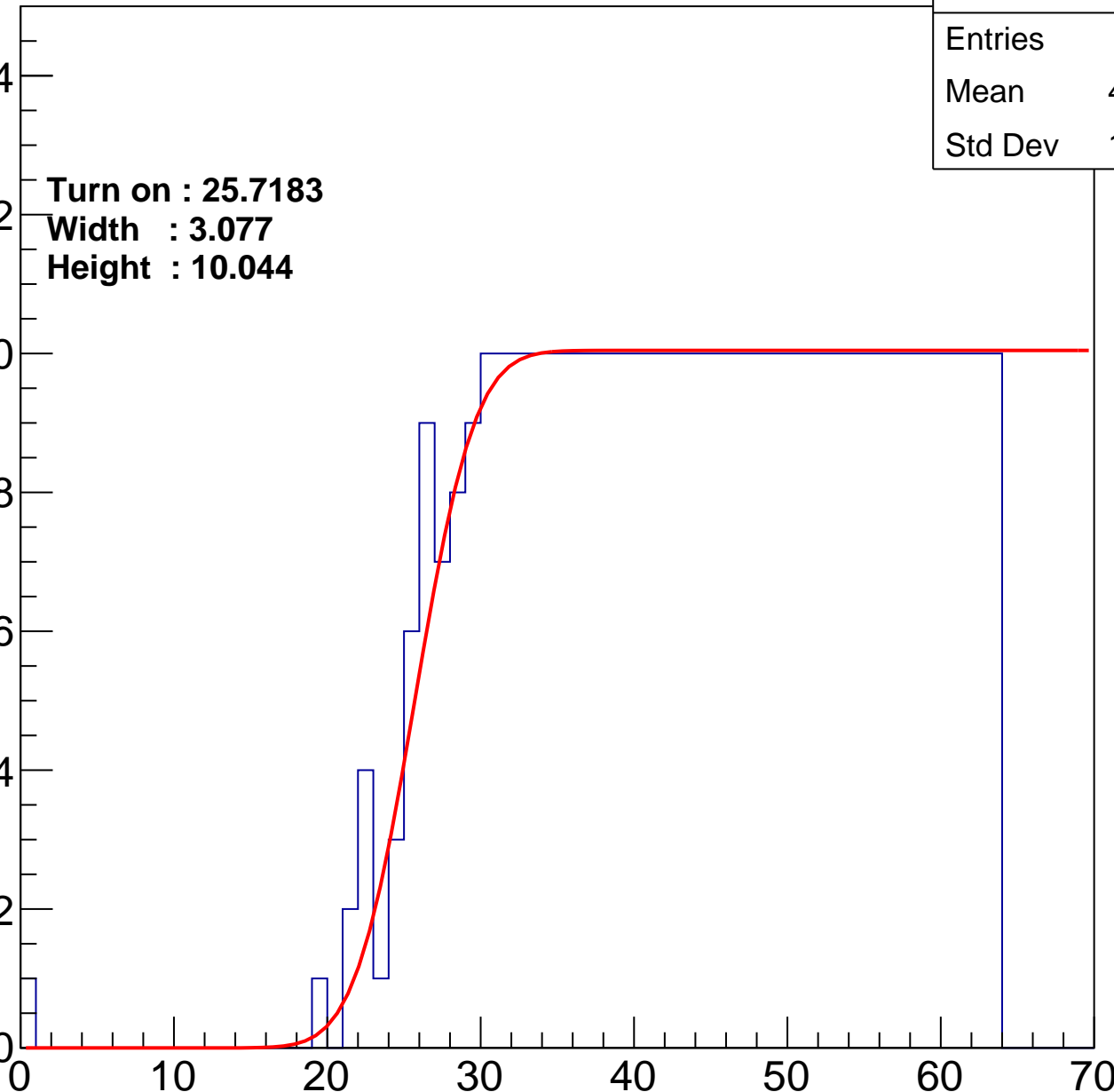
Width : 3.077

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch59

calib_packv5_042523_0143.root, FC#13, port D2

Entries	373
Mean	44.45
Std Dev	11.74

Turn on : 27.4652

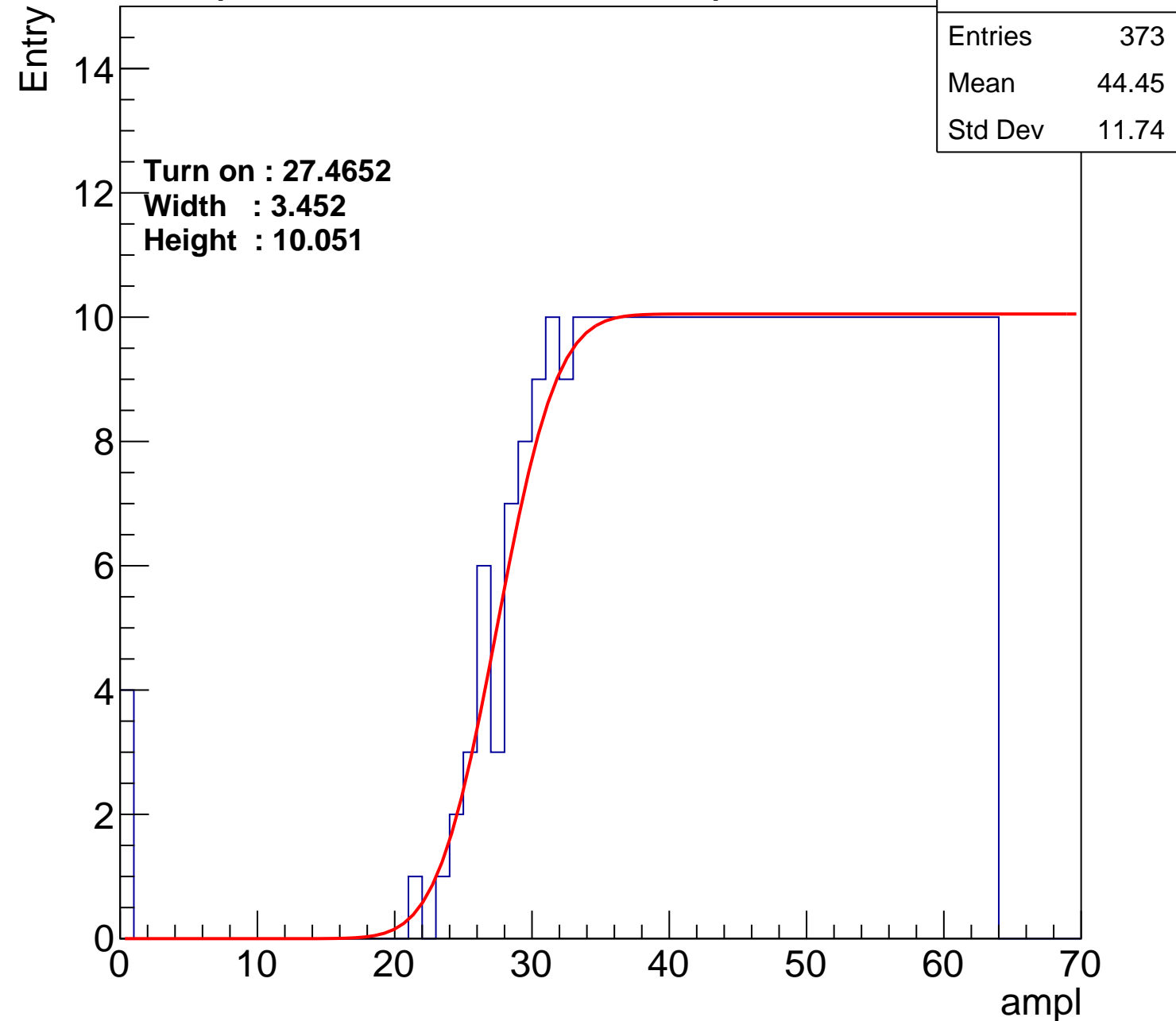
Width : 3.452

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch60

calib_packv5_042523_0143.root, FC#13, port D2

Entries	383
Mean	44.09
Std Dev	11.7

Turn on : 25.6667

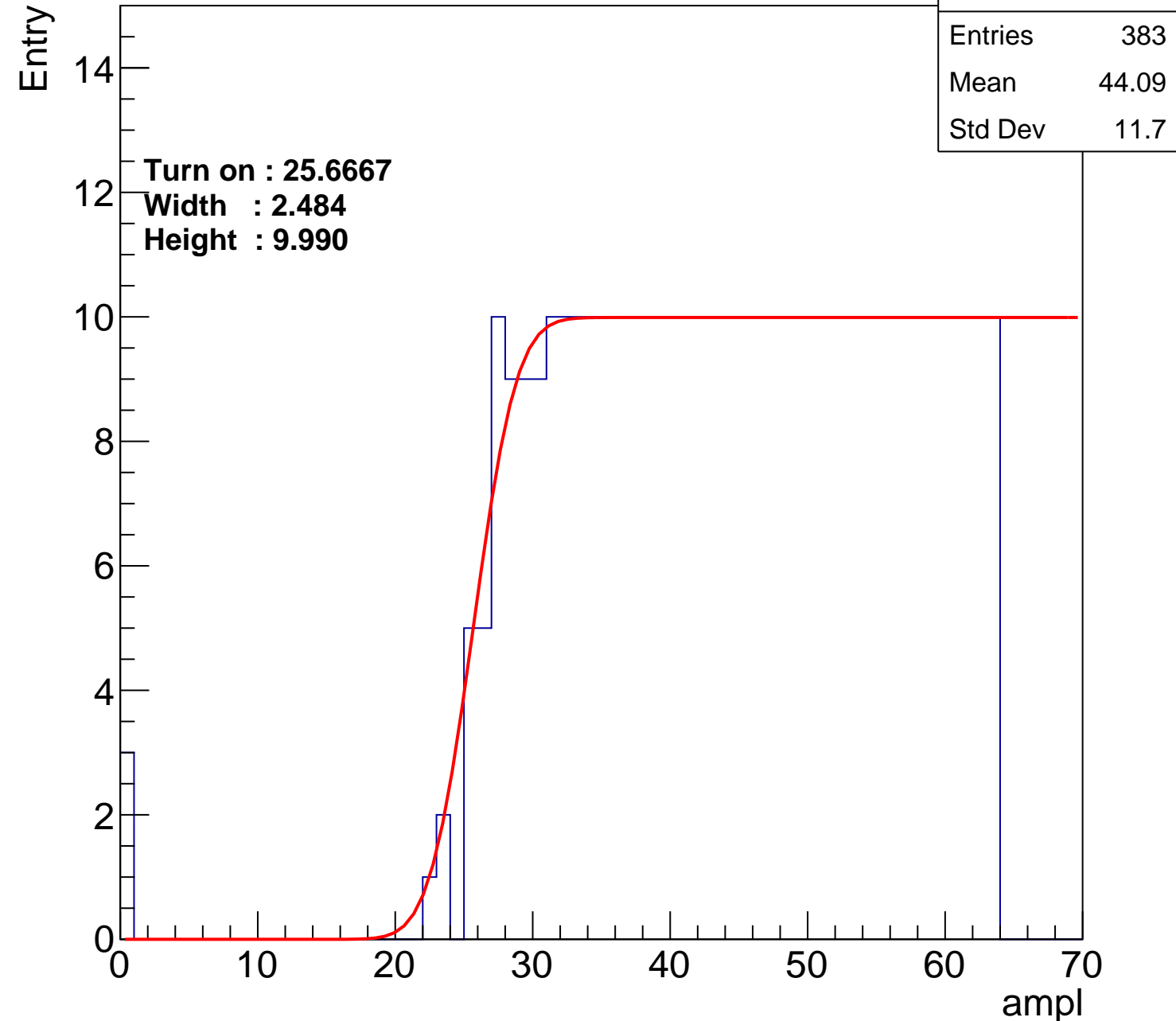
Width : 2.484

Height : 9.990

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch61

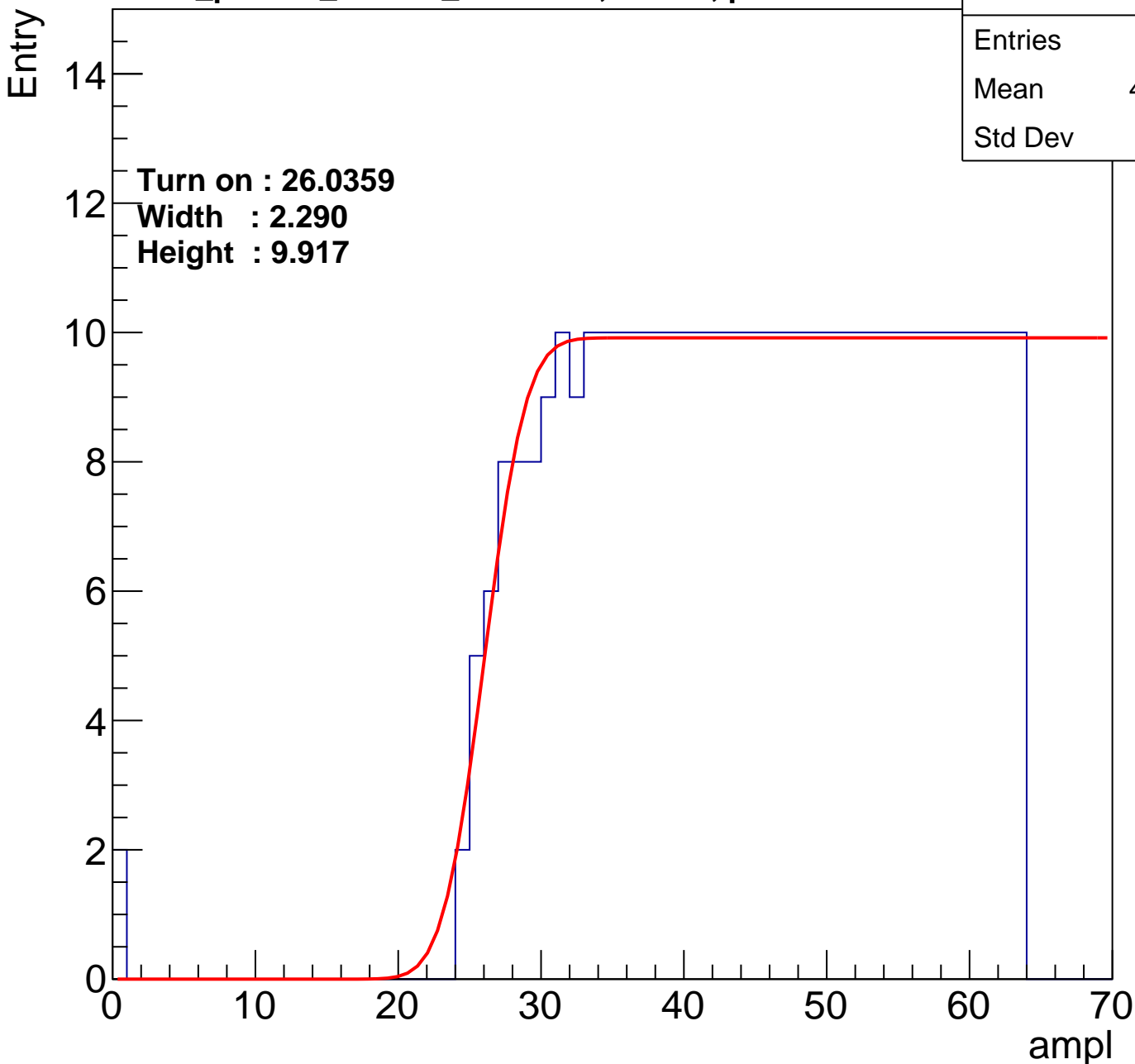
calib_packv5_042523_0143.root, FC#13, port D2

Entries	377
Mean	44.43
Std Dev	11.4

Turn on : 26.0359

Width : 2.290

Height : 9.917



B1L003S, U1-ch62

calib_packv5_042523_0143.root, FC#13, port D2

Entries	359
Mean	45.13
Std Dev	11.42

Turn on : 28.6522

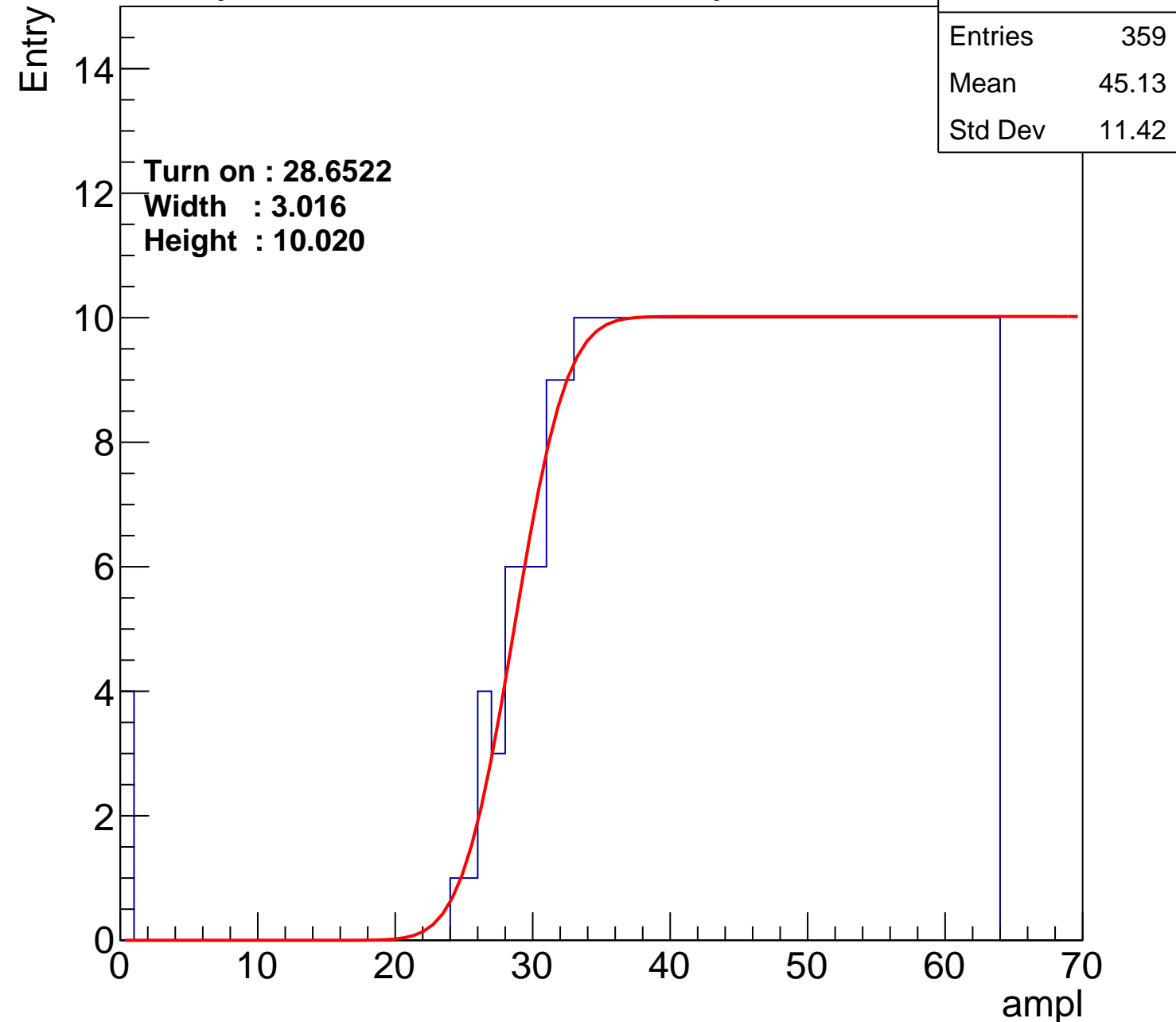
Width : 3.016

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch63

calib_packv5_042523_0143.root, FC#13, port D2

Entries	369
Mean	44.75
Std Dev	11.4

Turn on : 27.6188

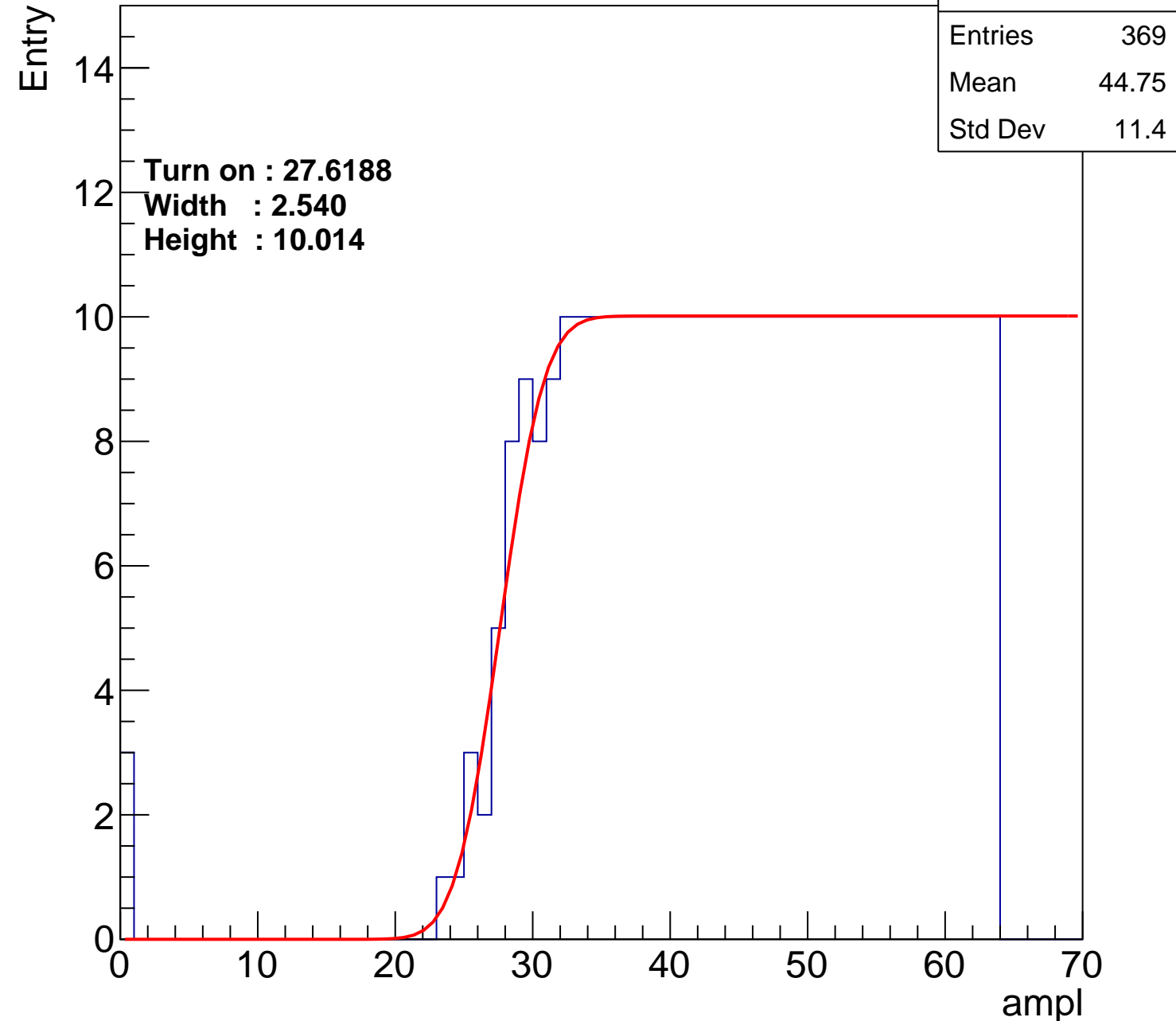
Width : 2.540

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch64

calib_packv5_042523_0143.root, FC#13, port D2

Entries	363
Mean	45.15
Std Dev	11.01

Turn on : 28.1610

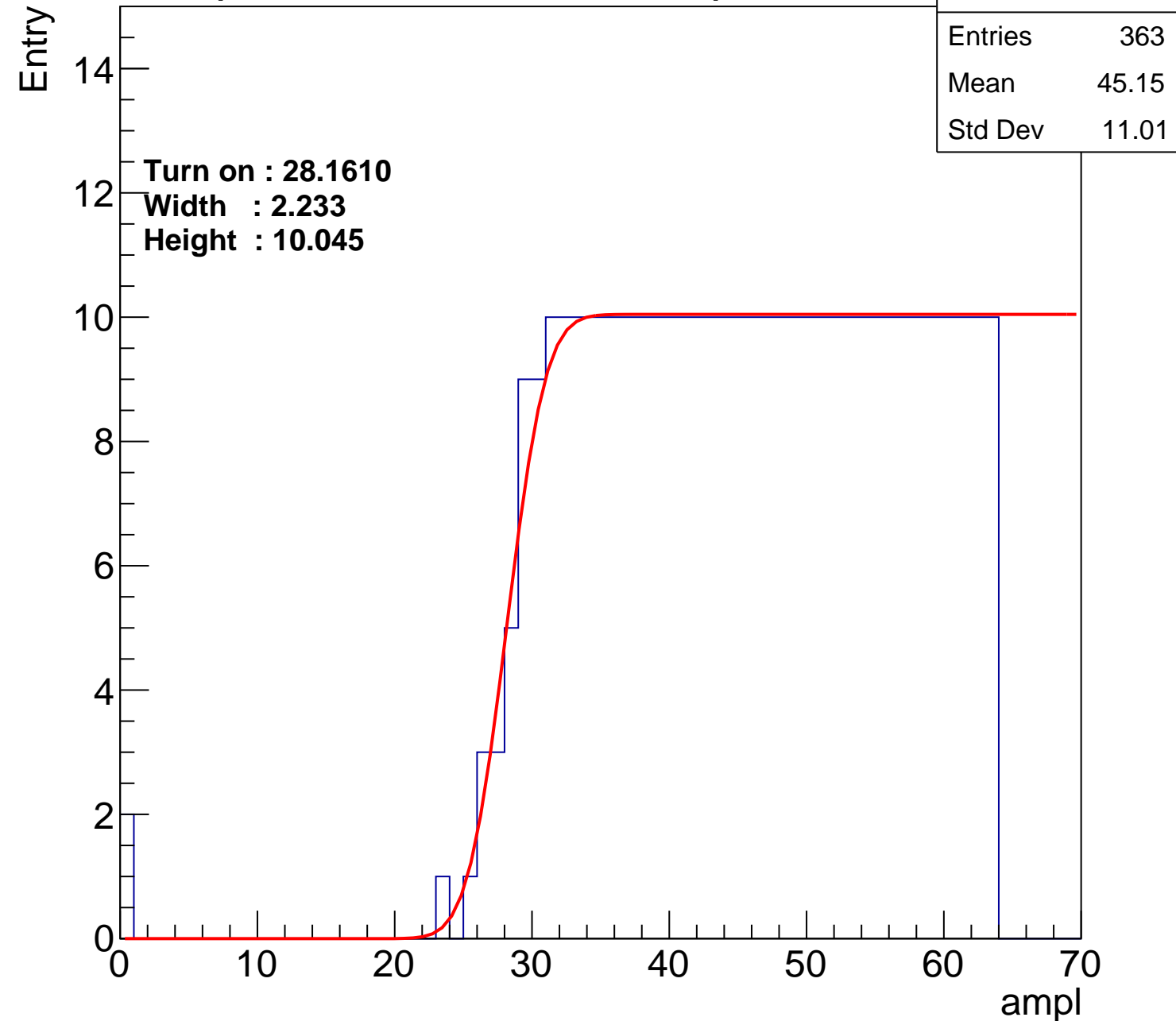
Width : 2.233

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch65

calib_packv5_042523_0143.root, FC#13, port D2

Entries	389
Mean	43.84
Std Dev	11.65

Turn on : 25.6367

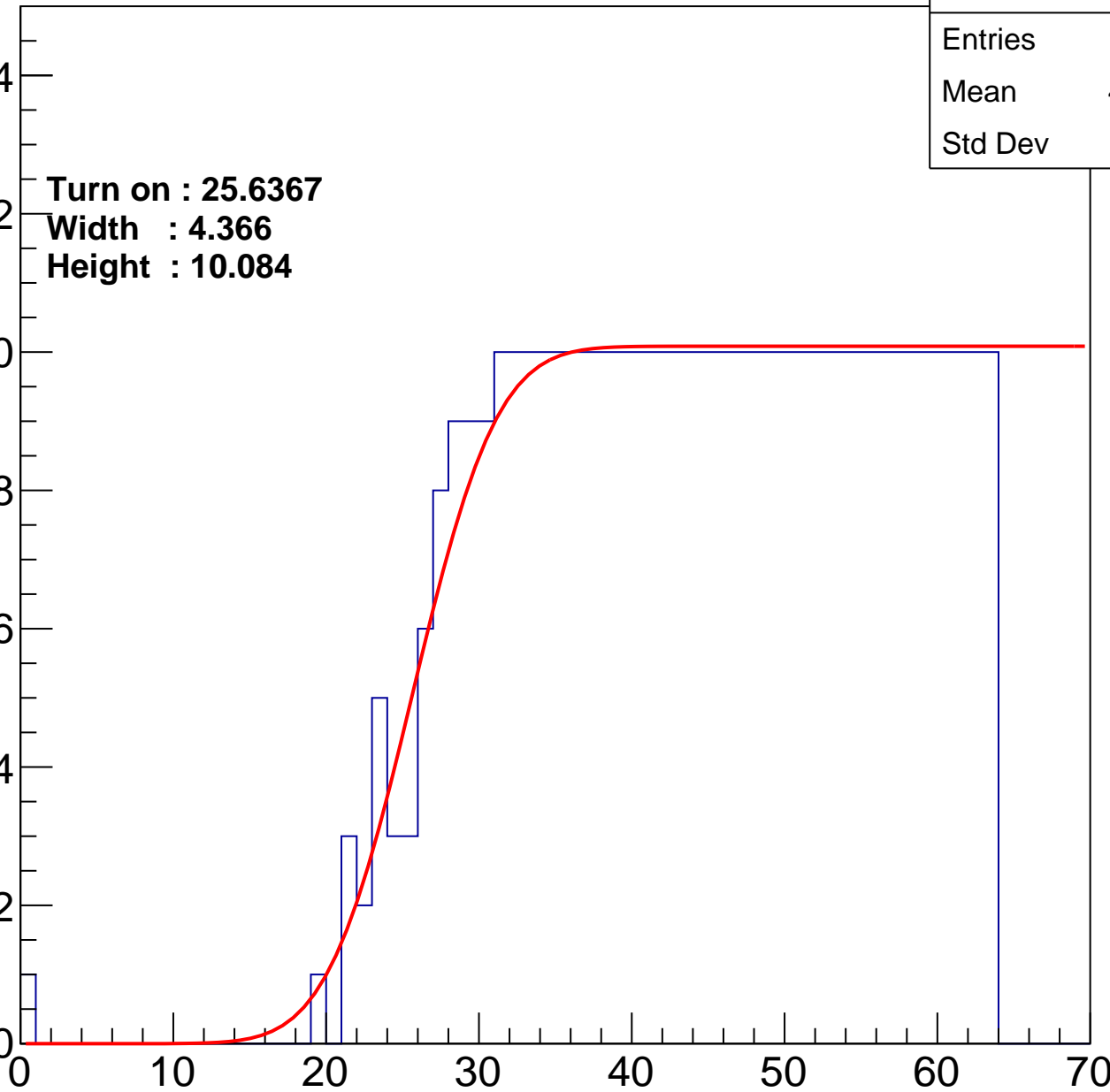
Width : 4.366

Height : 10.084

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch66

calib_packv5_042523_0143.root, FC#13, port D2

Entries	388
Mean	43.85
Std Dev	11.75

Turn on : 25.6090

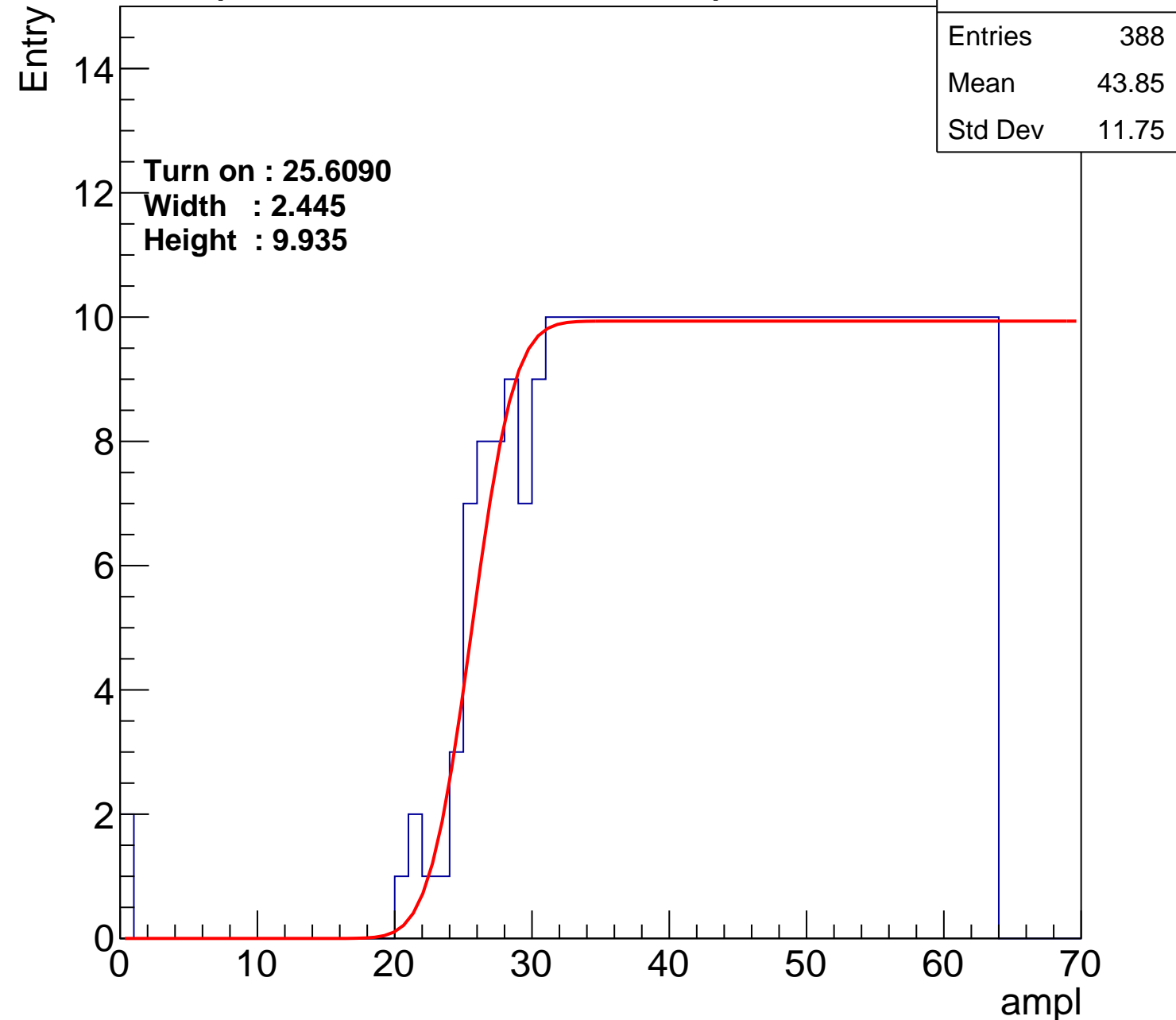
Width : 2.445

Height : 9.935

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch67

calib_packv5_042523_0143.root, FC#13, port D2

Entries	374
Mean	44.39
Std Dev	11.78

Turn on : 26.7633

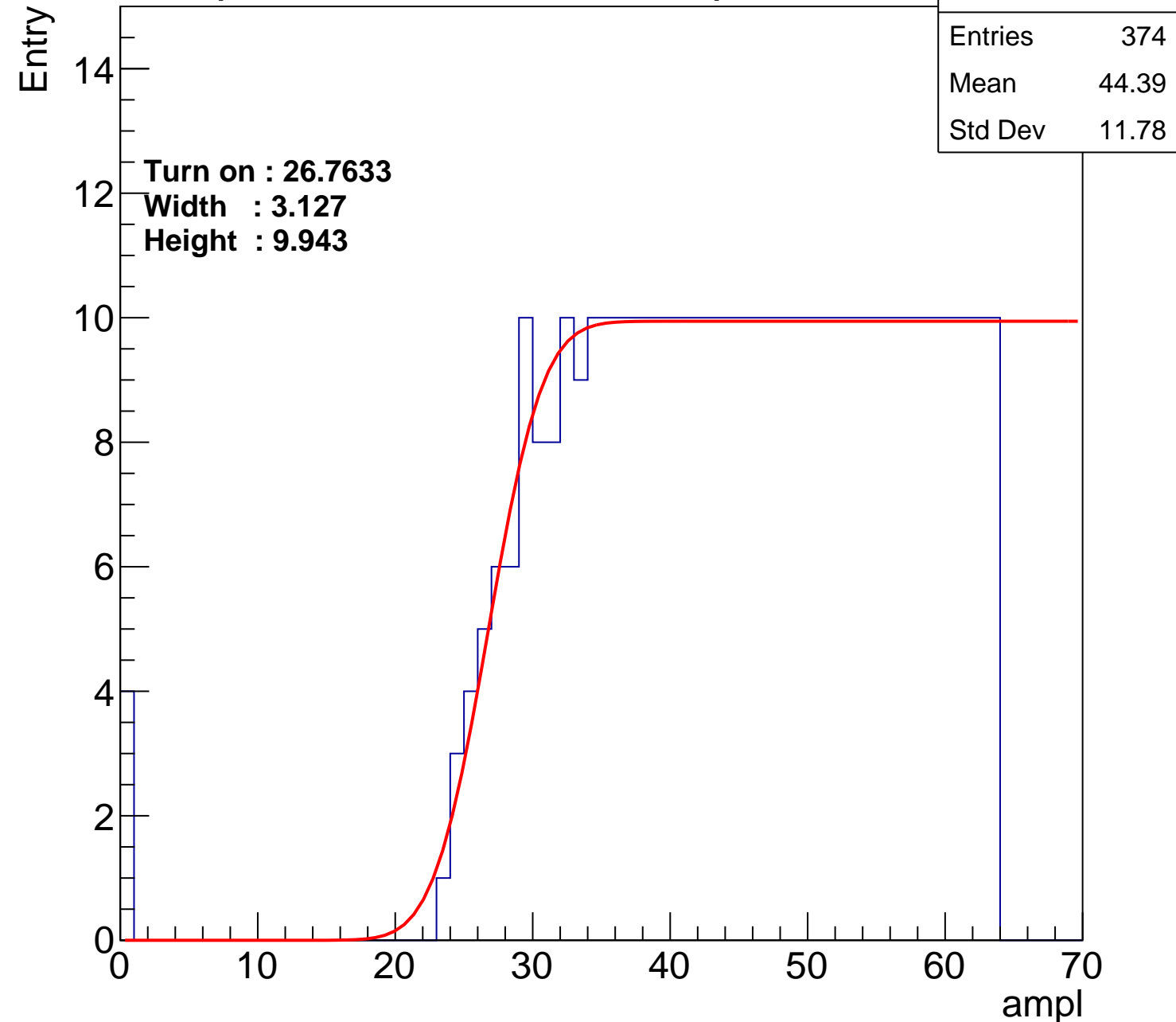
Width : 3.127

Height : 9.943

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch68

calib_packv5_042523_0143.root, FC#13, port D2

Entries	384
Mean	44.05
Std Dev	11.65

Turn on : 25.7946

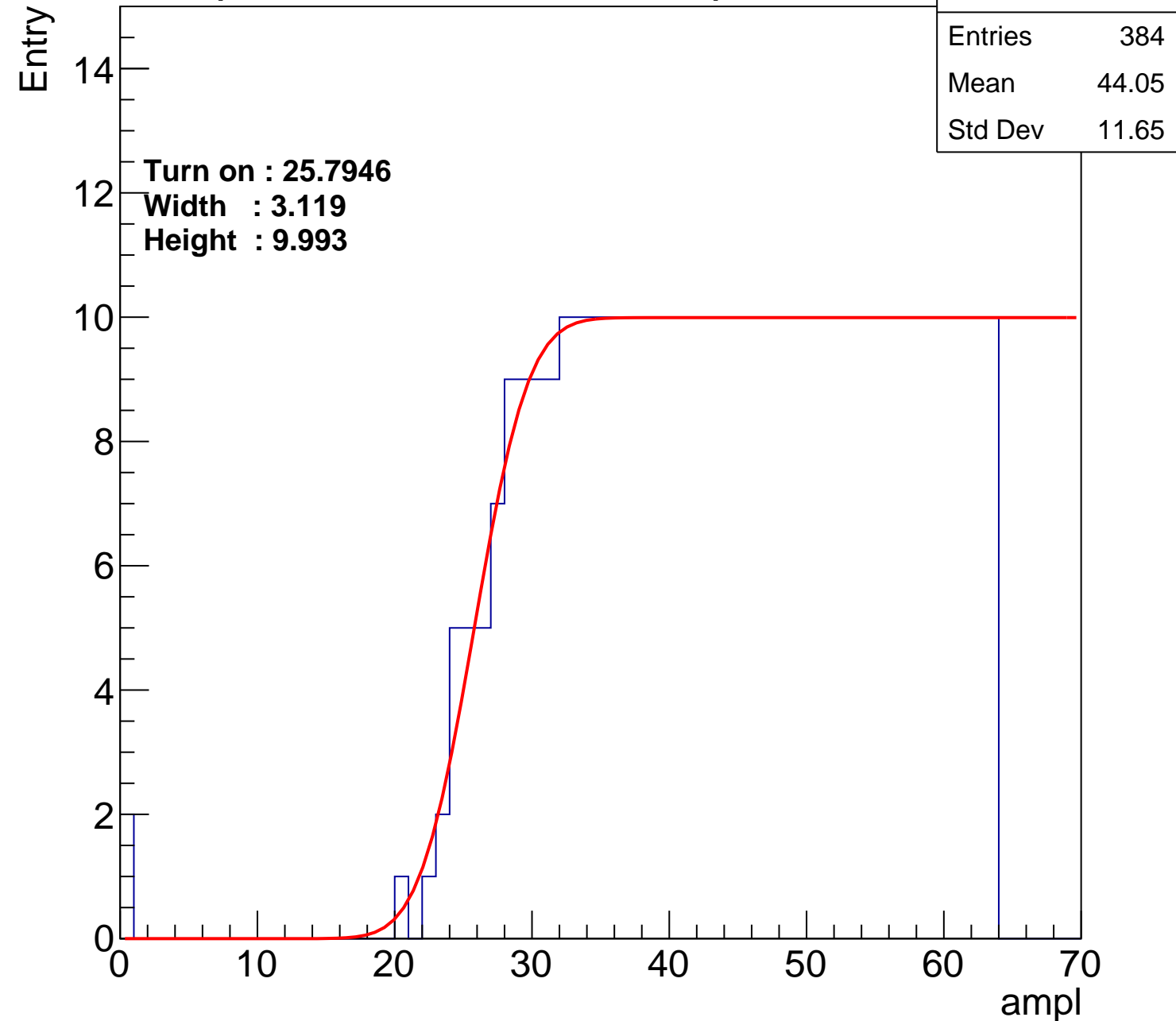
Width : 3.119

Height : 9.993

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch69

calib_packv5_042523_0143.root, FC#13, port D2

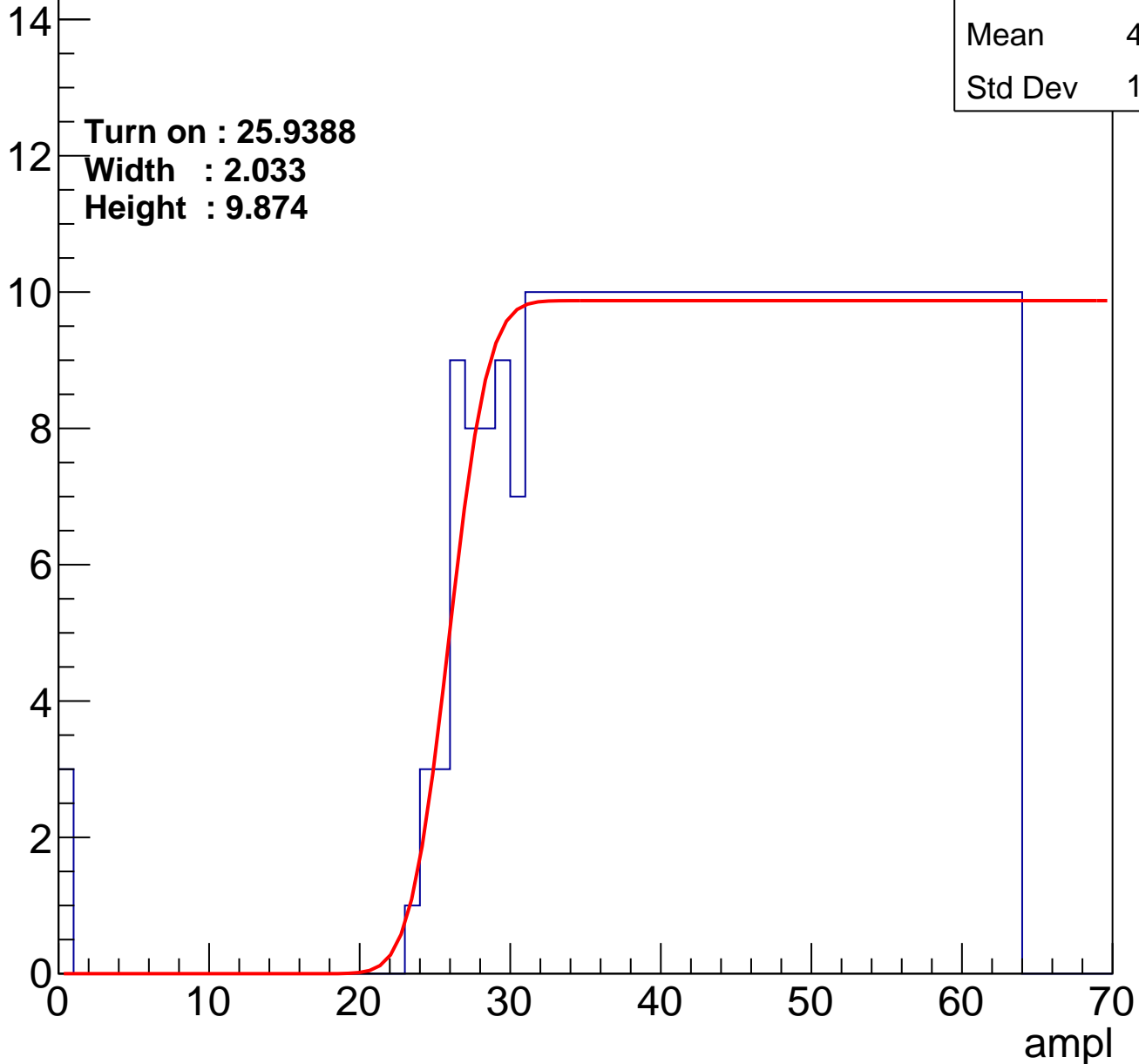
Entries	381
Mean	44.16
Std Dev	11.69

Turn on : 25.9388

Width : 2.033

Height : 9.874

Entry



B1L003S, U1-ch70

calib_packv5_042523_0143.root, FC#13, port D2

Entries	369
Mean	44.81
Std Dev	11.23

Turn on : 27.4426

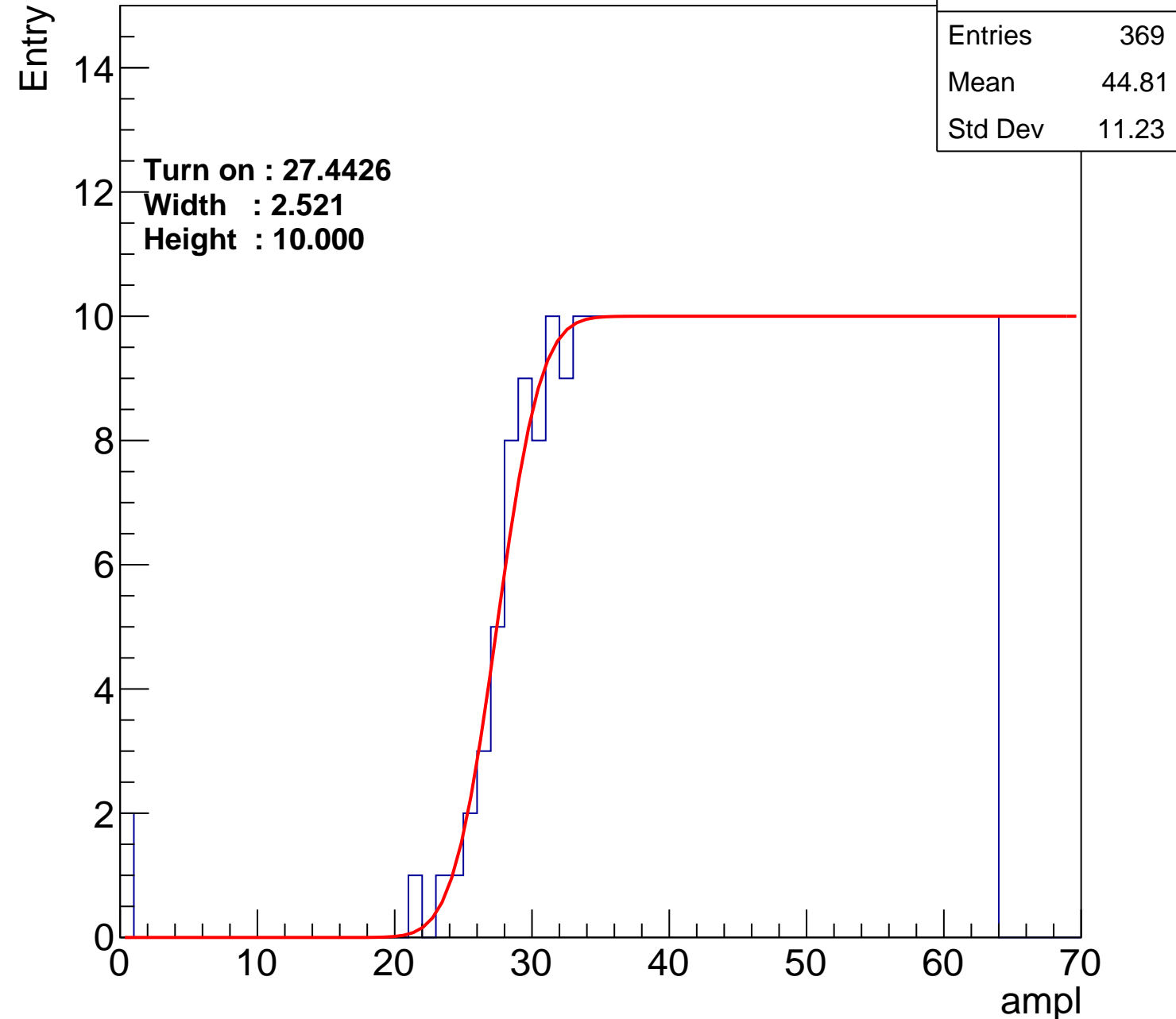
Width : 2.521

Height : 10.000

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch71

calib_packv5_042523_0143.root, FC#13, port D2

Entries	373
Mean	44.55
Std Dev	11.5

Turn on : 27.2443

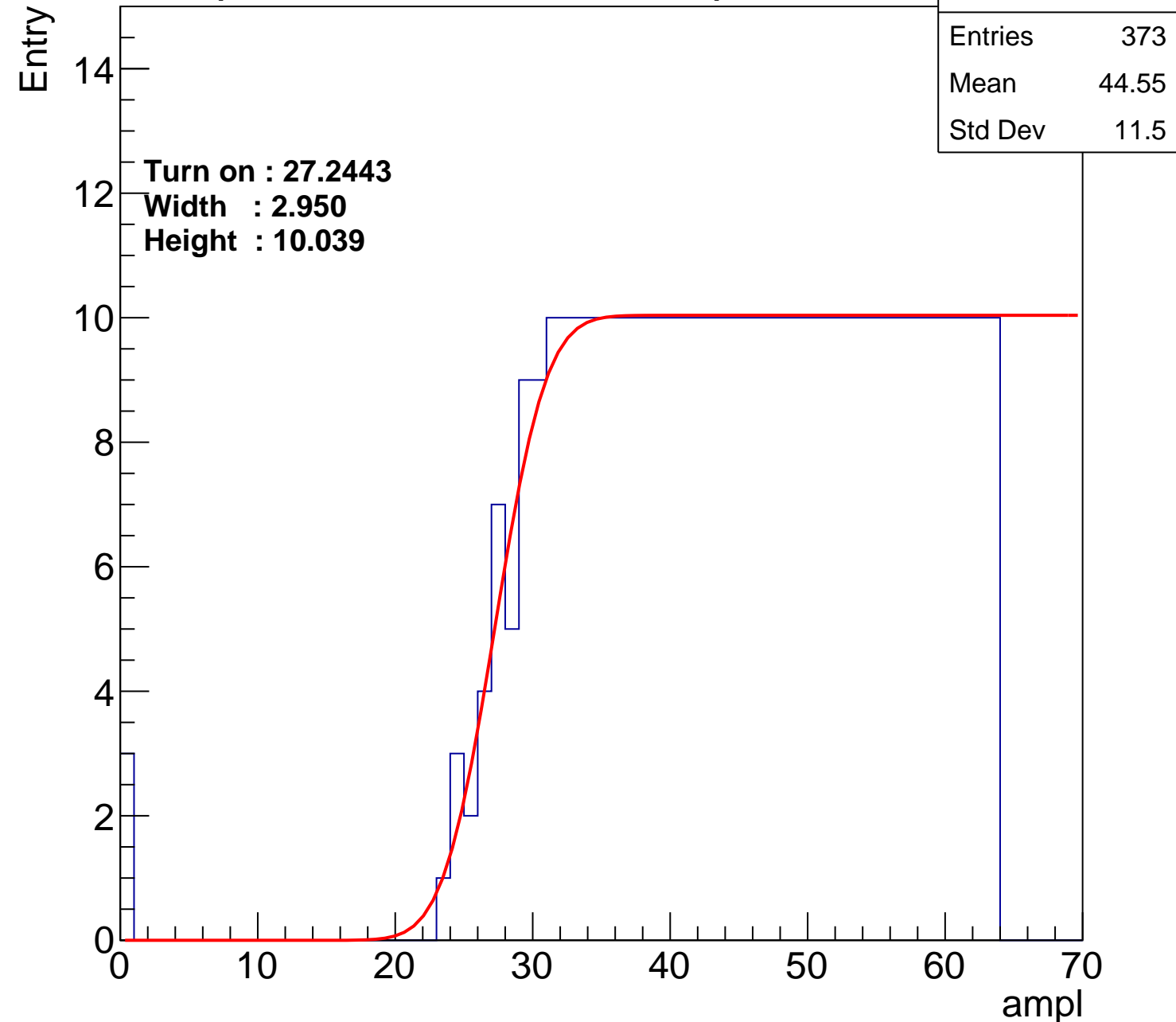
Width : 2.950

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch72

calib_packv5_042523_0143.root, FC#13, port D2

Entries	392
Mean	43.53
Std Dev	12.18

Turn on : 25.9315

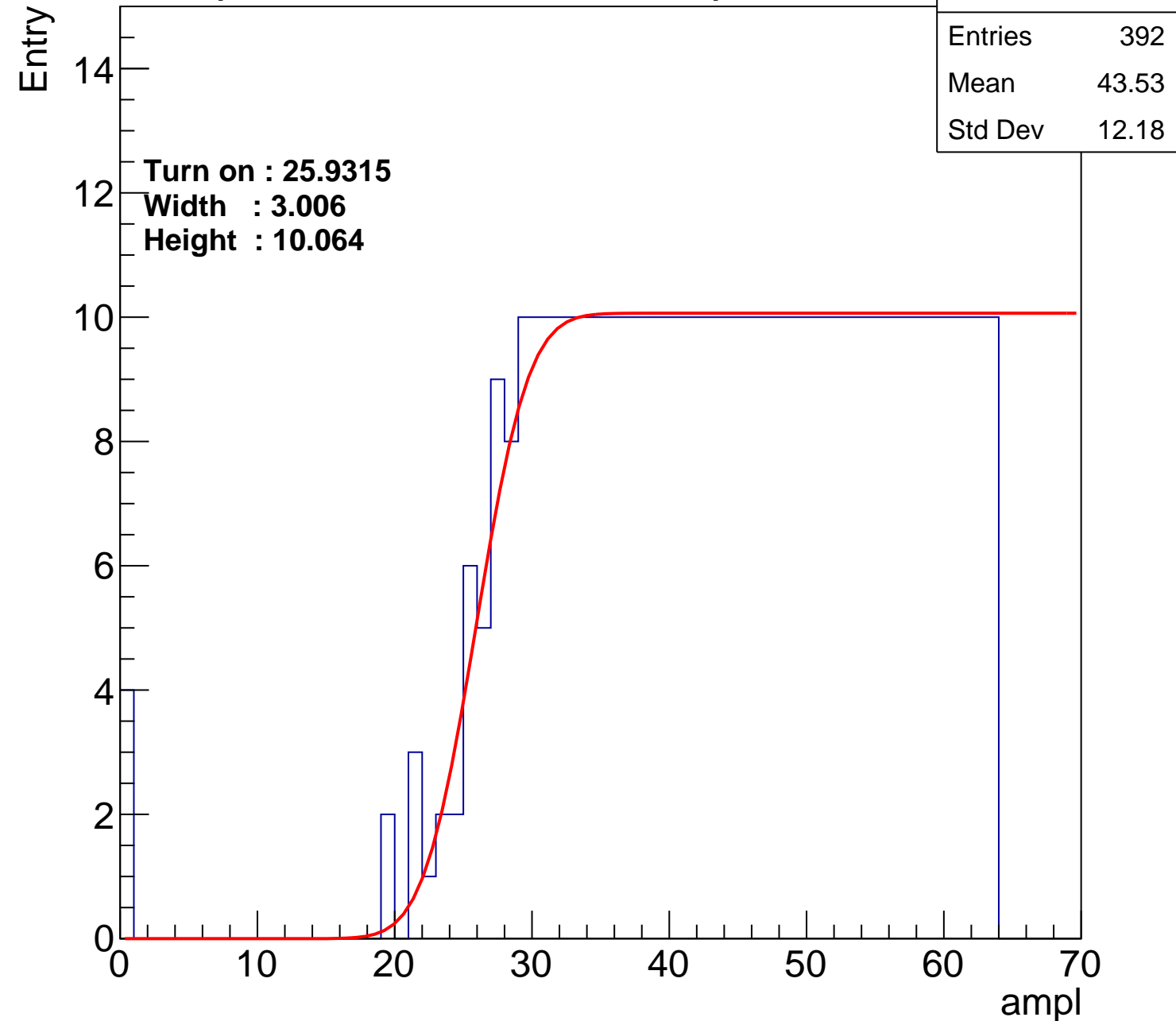
Width : 3.006

Height : 10.064

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch73

calib_packv5_042523_0143.root, FC#13, port D2

Entries	356
Mean	45.47
Std Dev	10.86

Turn on : 28.8945

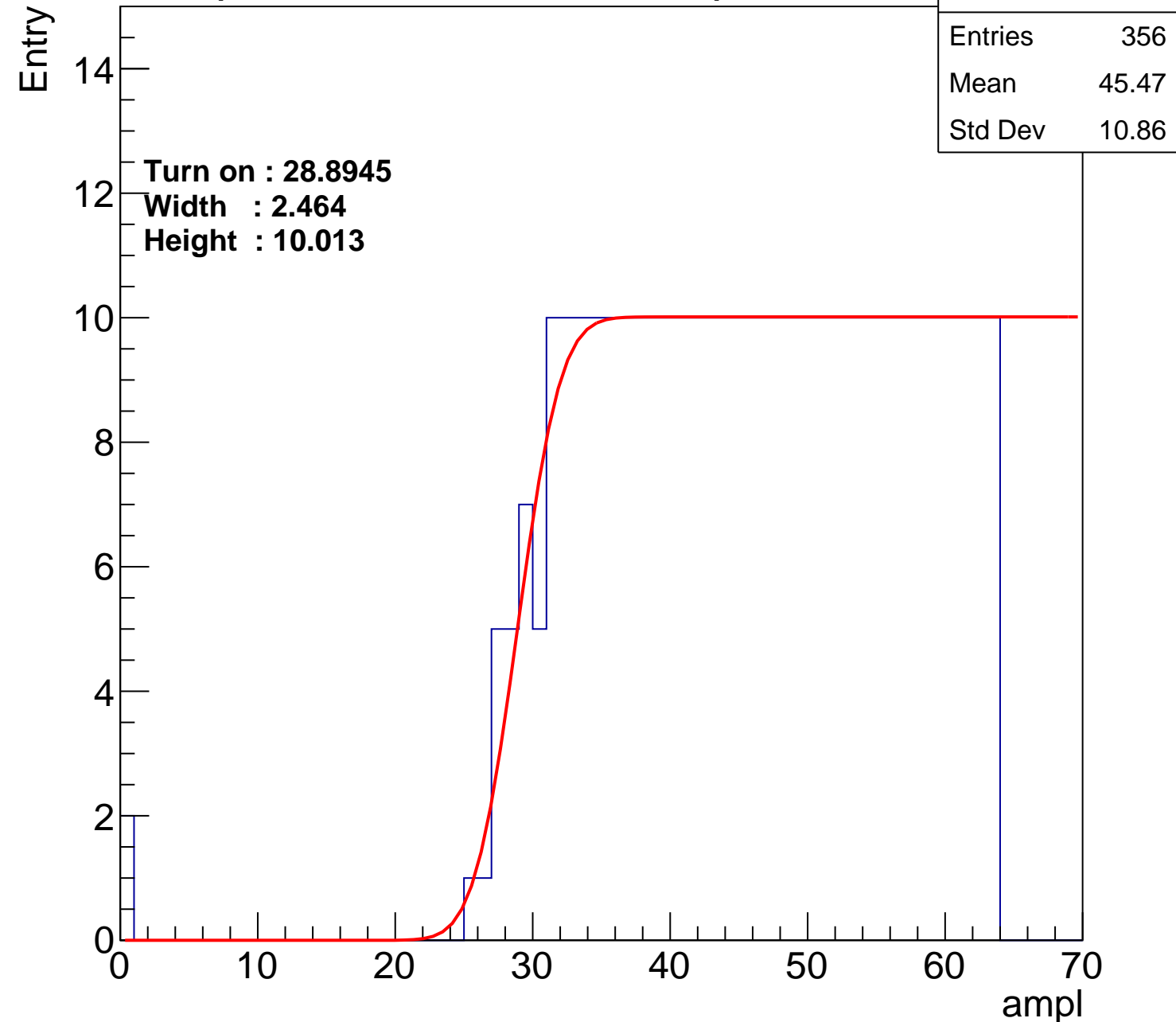
Width : 2.464

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch74

calib_packv5_042523_0143.root, FC#13, port D2

Entries	362
Mean	45.23
Std Dev	10.84

Turn on : 27.9594

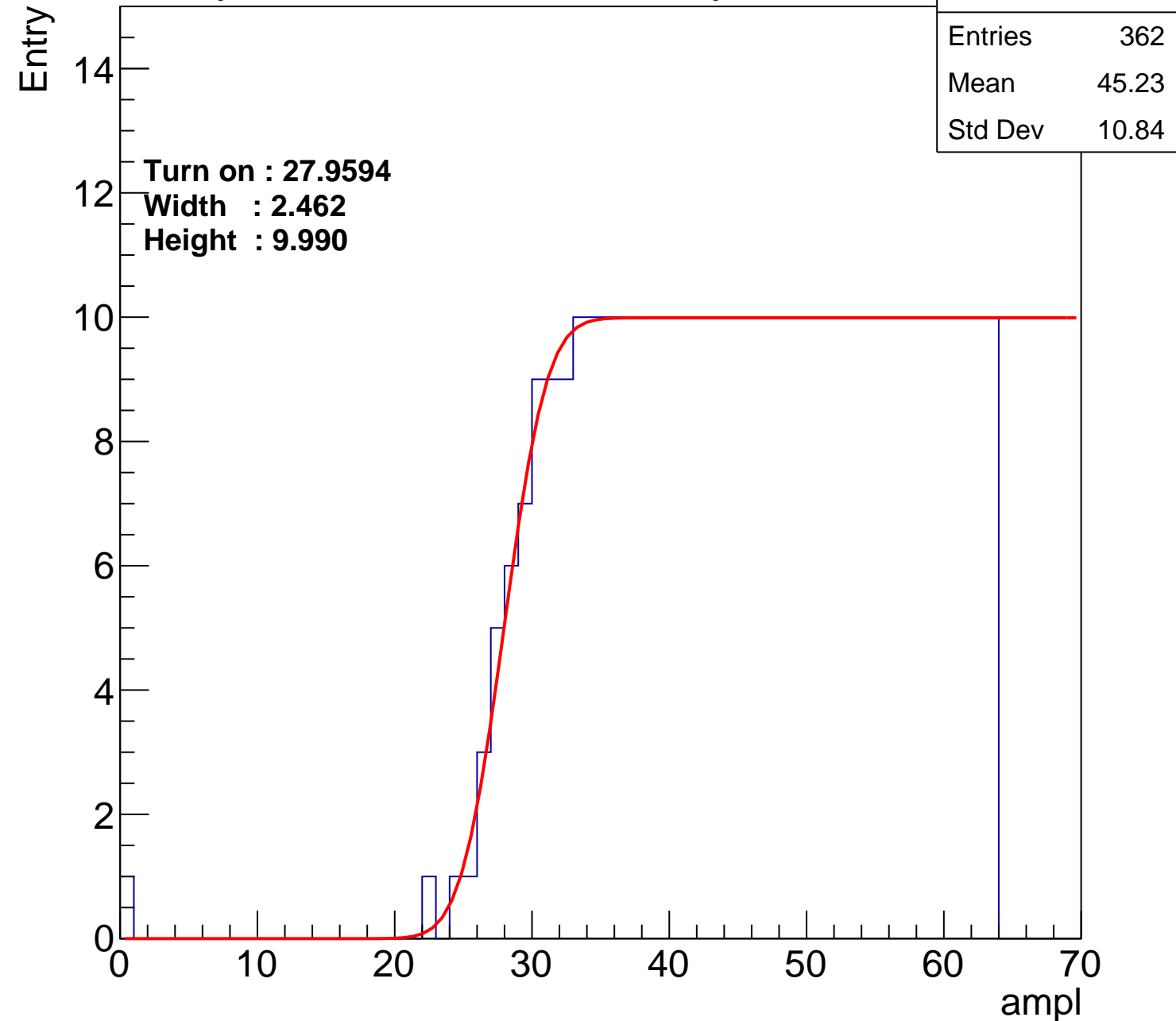
Width : 2.462

Height : 9.990

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch75

calib_packv5_042523_0143.root, FC#13, port D2

Entries	387
Mean	43.85
Std Dev	11.87

Turn on : 25.6912

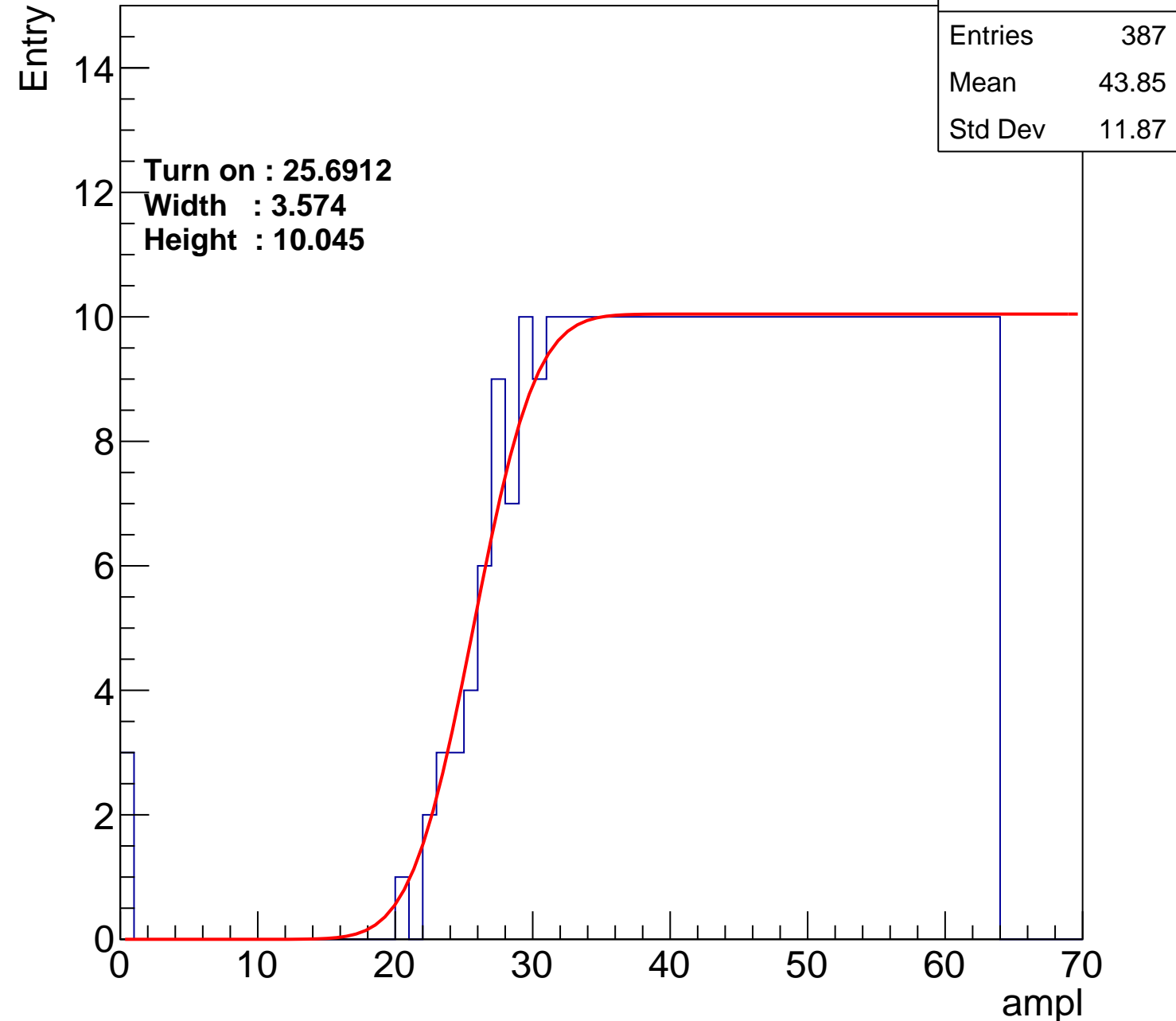
Width : 3.574

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch76

calib_packv5_042523_0143.root, FC#13, port D2

Entries	378
Mean	44.29
Std Dev	11.65

Turn on : 26.4184

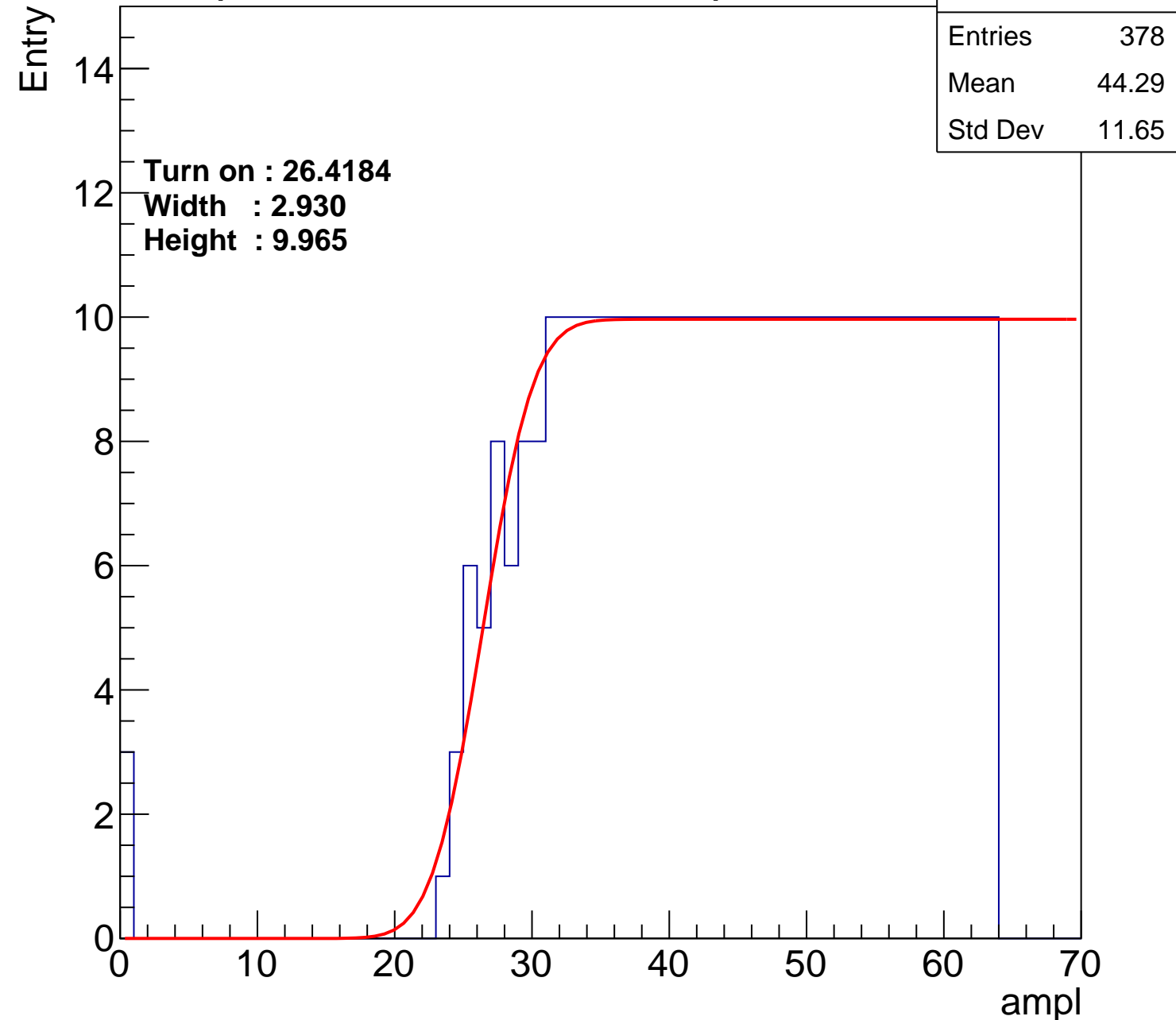
Width : 2.930

Height : 9.965

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch77

calib_packv5_042523_0143.root, FC#13, port D2

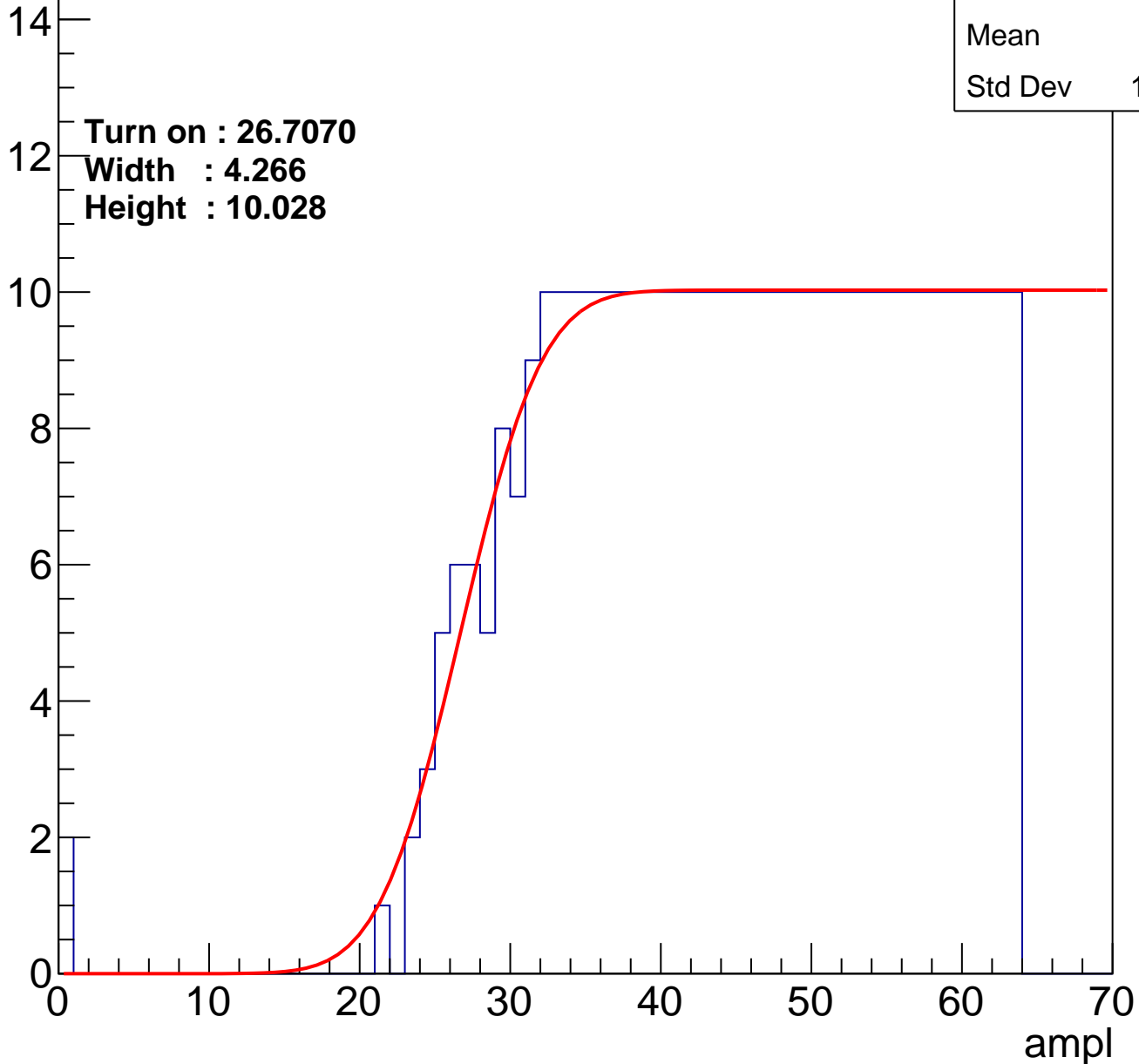
Entries	374
Mean	44.5
Std Dev	11.45

Turn on : 26.7070

Width : 4.266

Height : 10.028

Entry



B1L003S, U1-ch78

calib_packv5_042523_0143.root, FC#13, port D2

Entries	367
Mean	44.89
Std Dev	11.21

Turn on : 27.6567

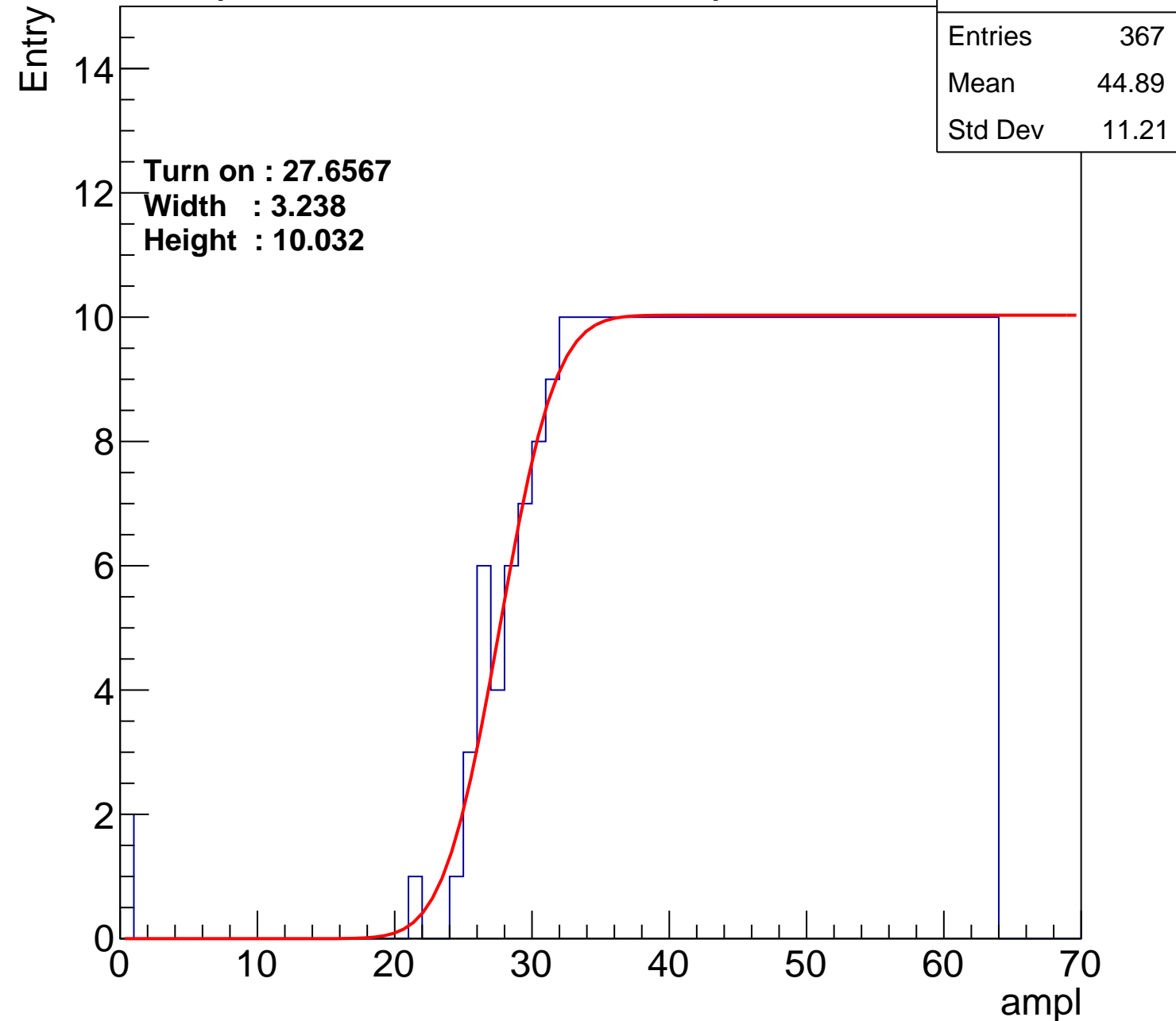
Width : 3.238

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch79

calib_packv5_042523_0143.root, FC#13, port D2

Entries	372
Mean	44.69
Std Dev	11.25

Turn on : 27.0389

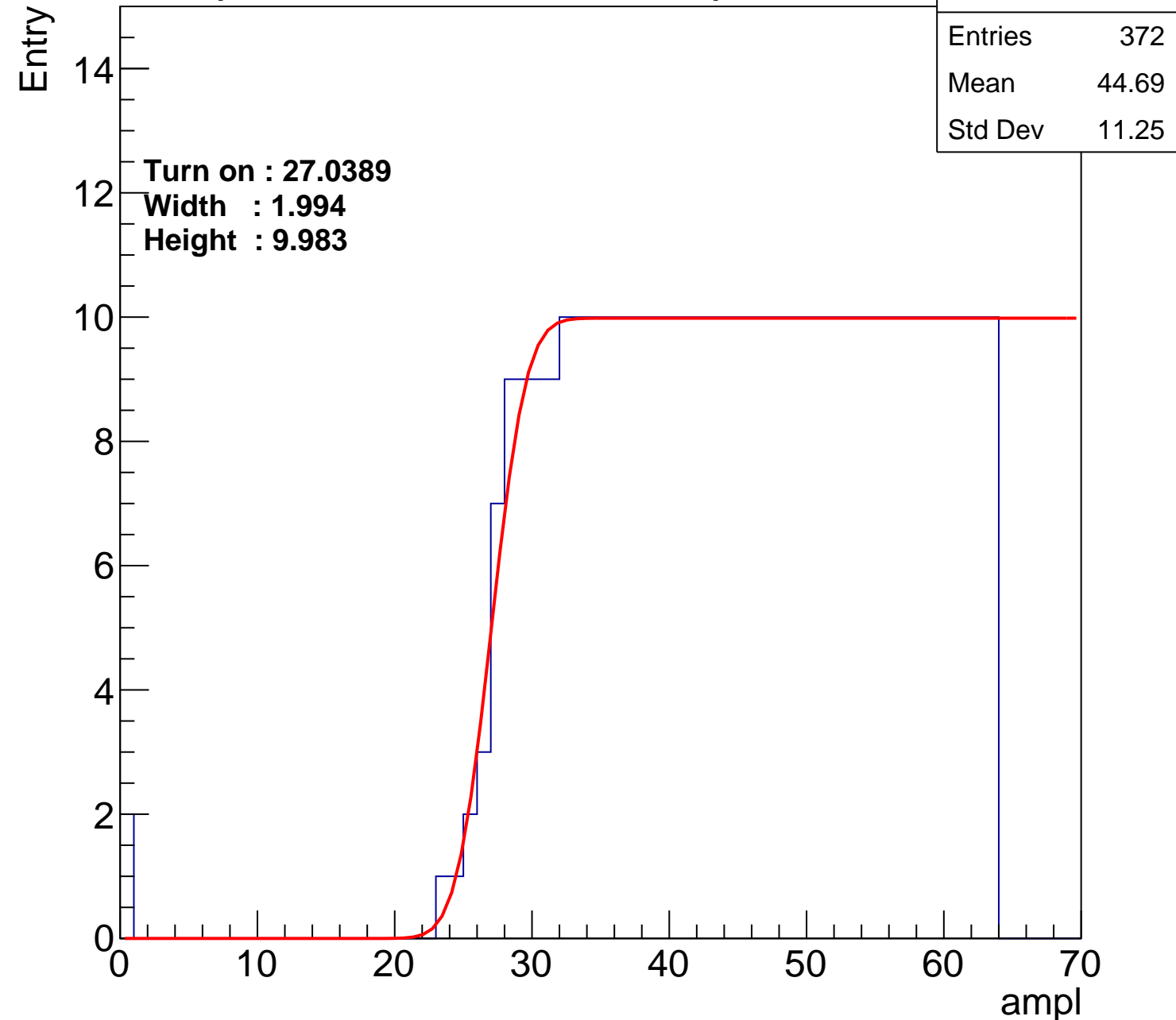
Width : 1.994

Height : 9.983

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch80

calib_packv5_042523_0143.root, FC#13, port D2

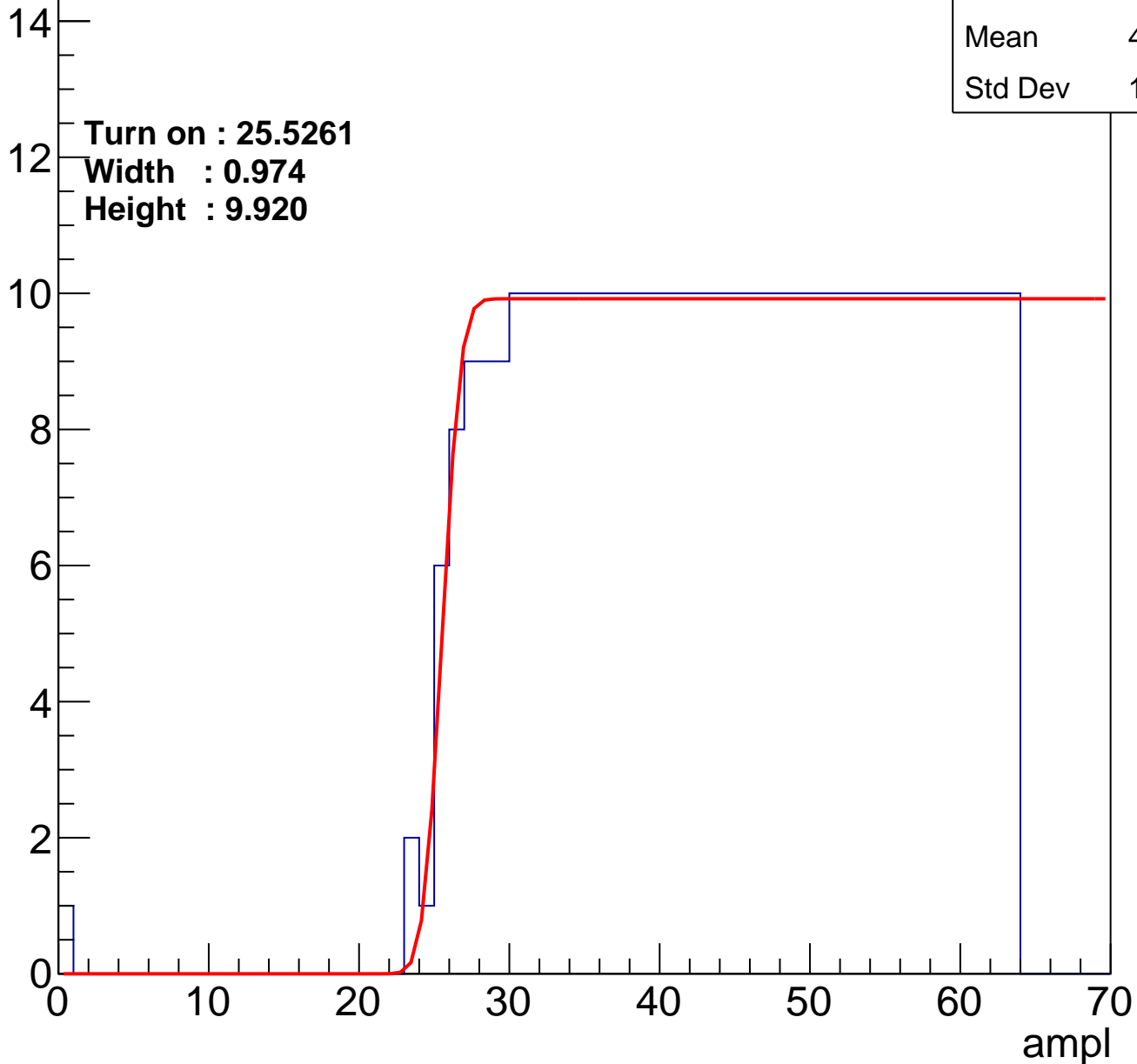
Entries	385
Mean	44.14
Std Dev	11.37

Turn on : 25.5261

Width : 0.974

Height : 9.920

Entry



B1L003S, U1-ch81

calib_packv5_042523_0143.root, FC#13, port D2

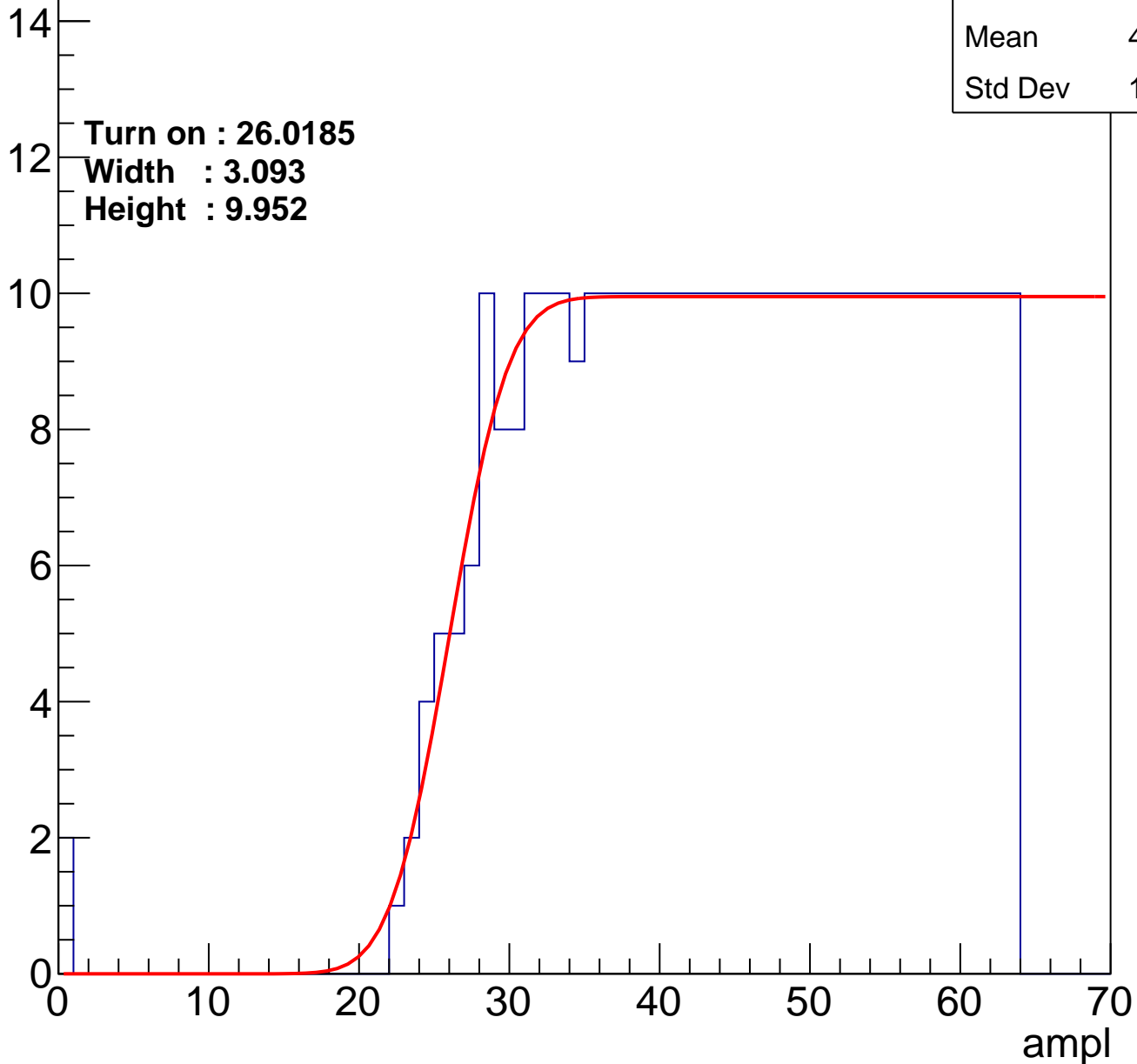
Entries	380
Mean	44.23
Std Dev	11.55

Turn on : 26.0185

Width : 3.093

Height : 9.952

Entry



B1L003S, U1-ch82

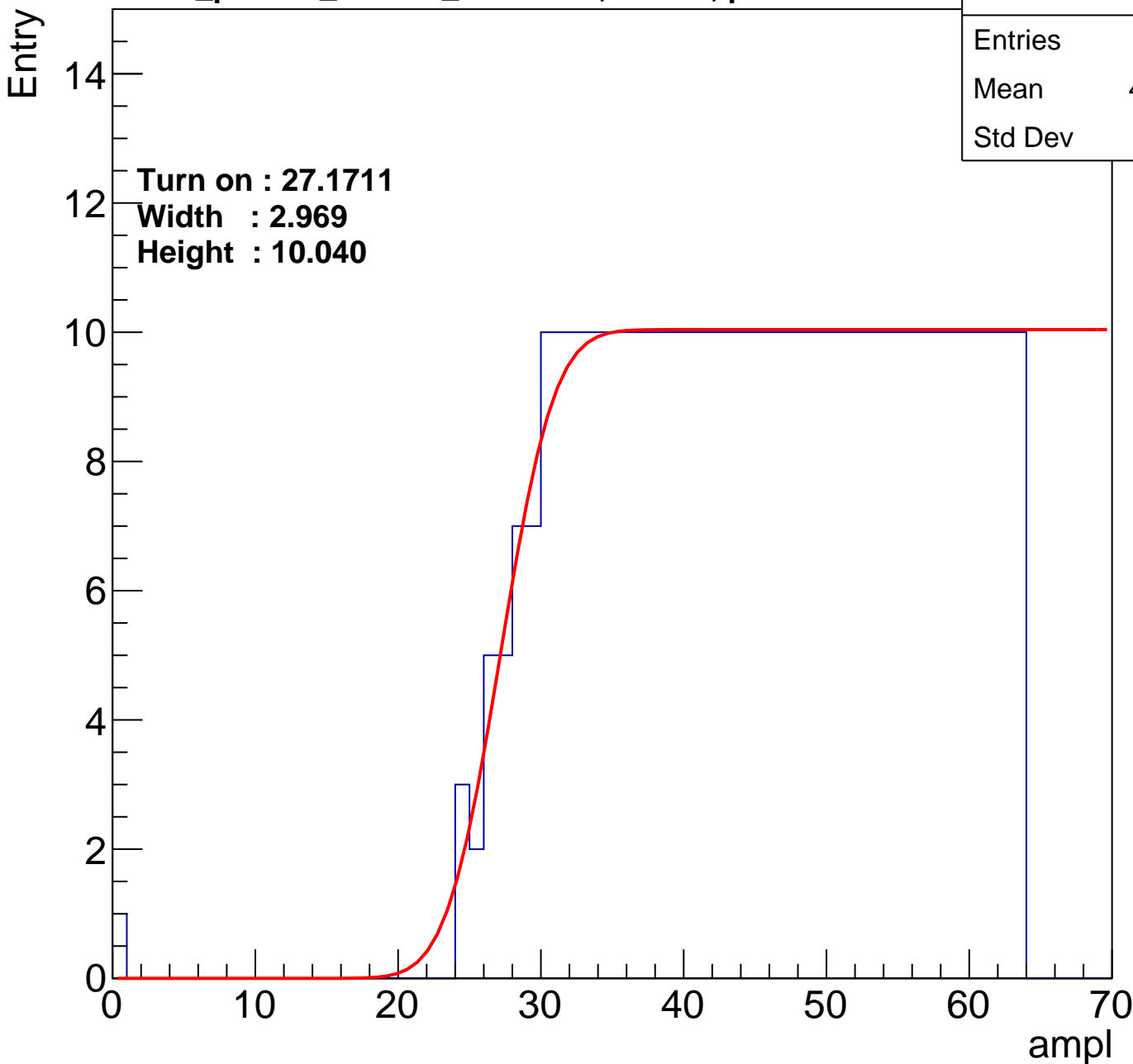
calib_packv5_042523_0143.root, FC#13, port D2

Turn on : 27.1711

Width : 2.969

Height : 10.040

Entries	370
Mean	44.85
Std Dev	11.01



B1L003S, U1-ch83

calib_packv5_042523_0143.root, FC#13, port D2

Entries	395
Mean	43.38
Std Dev	12.32

Turn on : 25.2264

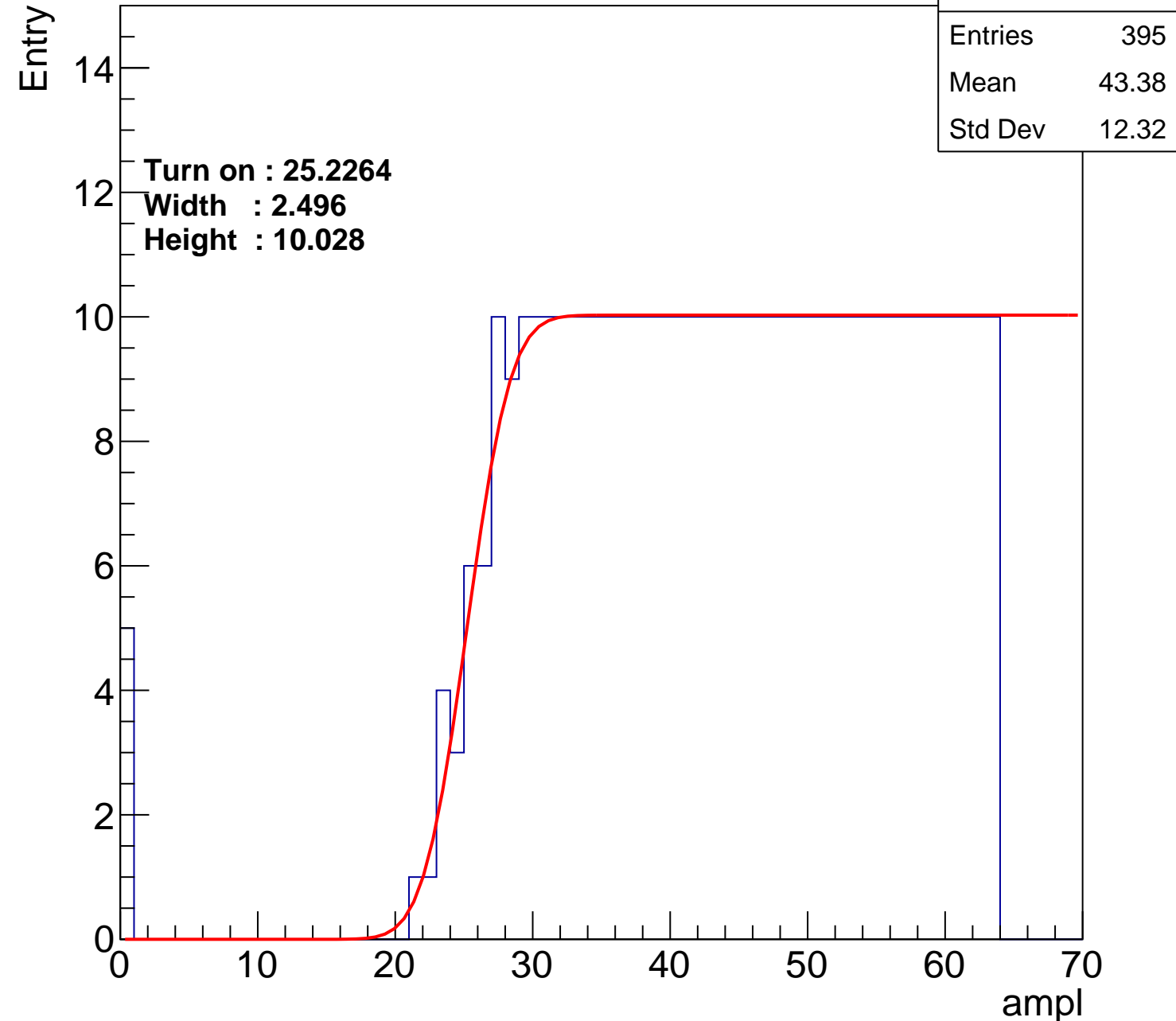
Width : 2.496

Height : 10.028

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch84

calib_packv5_042523_0143.root, FC#13, port D2

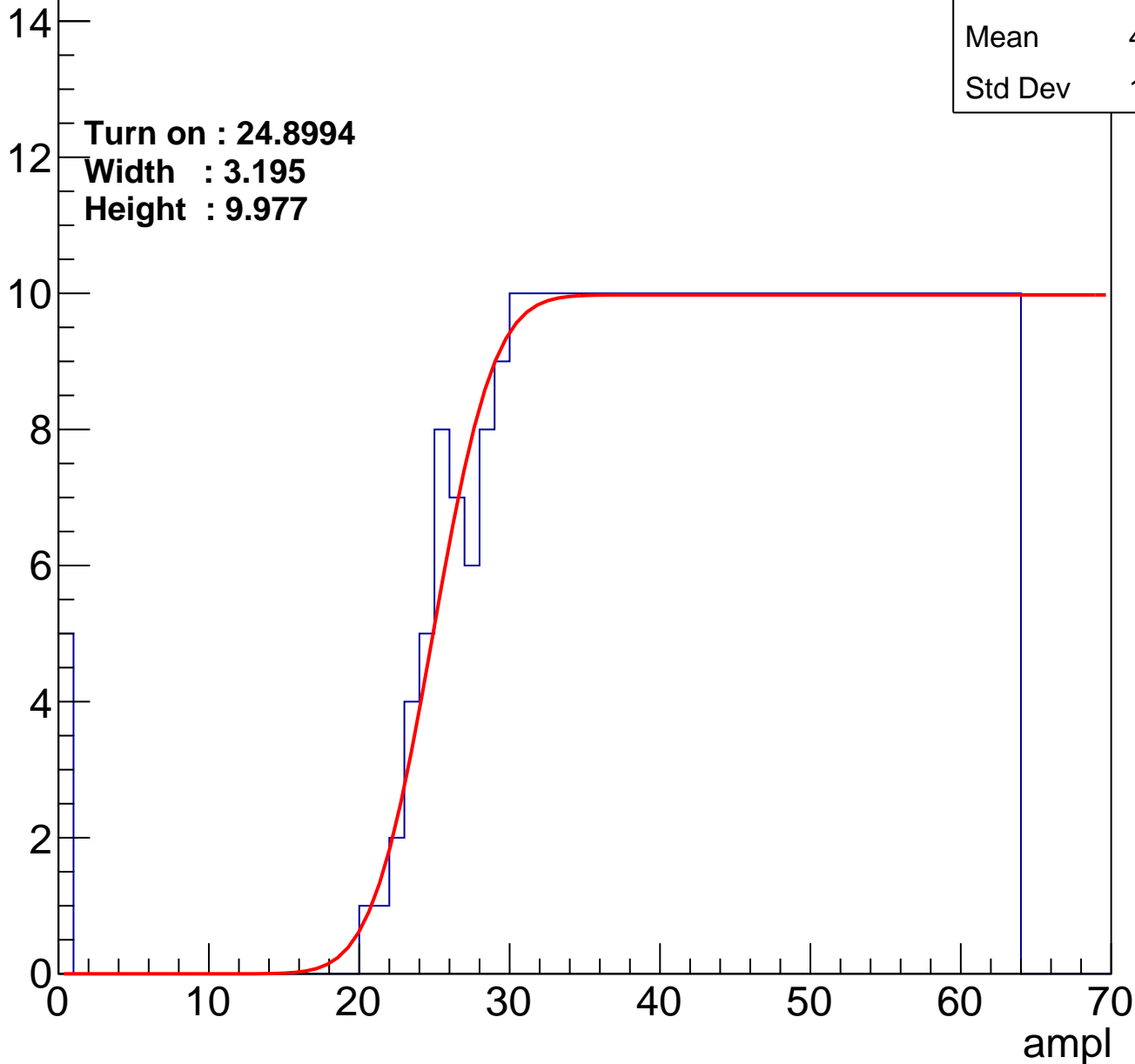
Entry

Entries	396
Mean	43.27
Std Dev	12.42

Turn on : 24.8994

Width : 3.195

Height : 9.977



B1L003S, U1-ch85

calib_packv5_042523_0143.root, FC#13, port D2

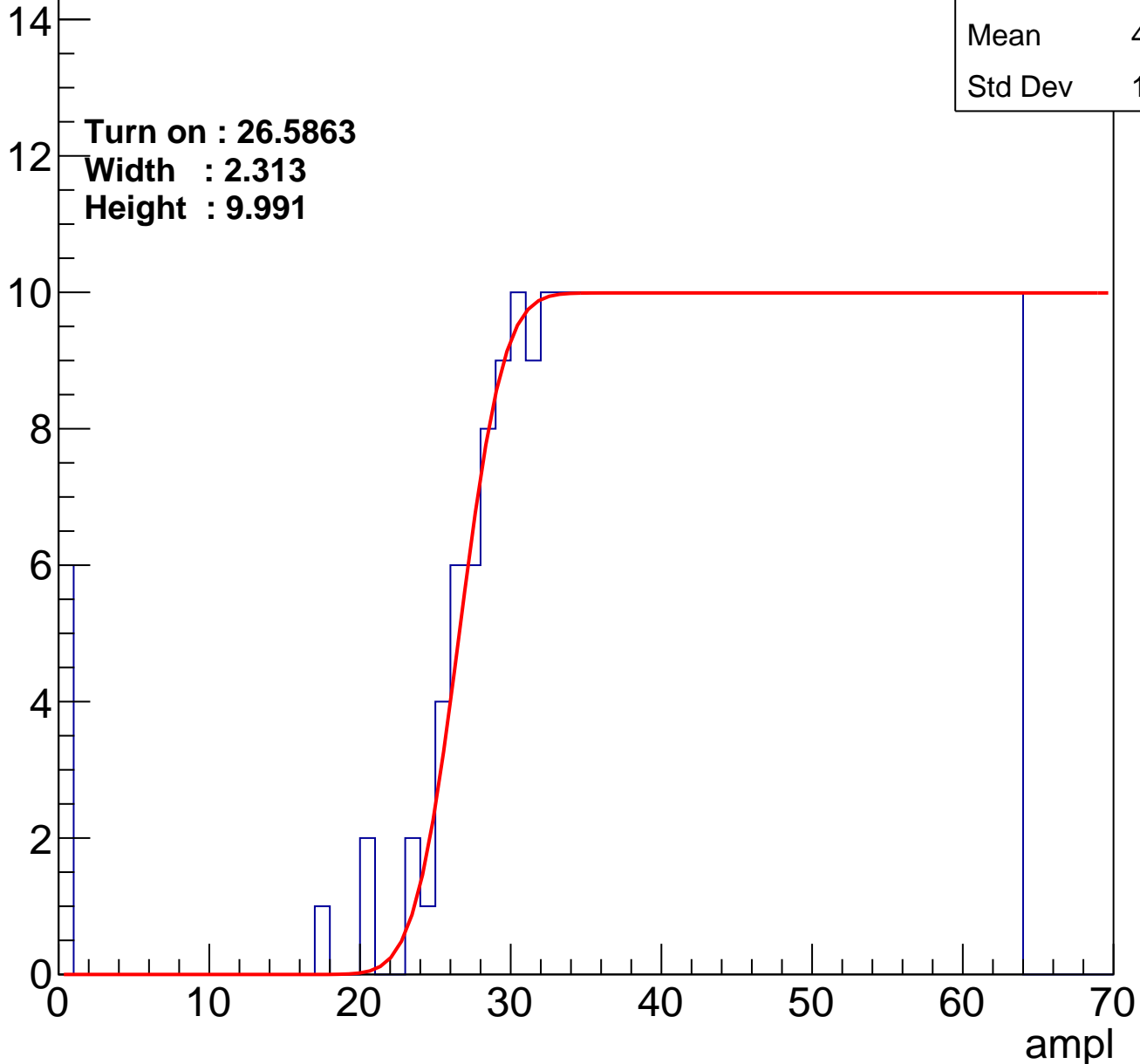
Entries	384
Mean	43.77
Std Dev	12.36

Turn on : 26.5863

Width : 2.313

Height : 9.991

Entry



B1L003S, U1-ch86

calib_packv5_042523_0143.root, FC#13, port D2

Entries	371
Mean	44.45
Std Dev	11.92

Turn on : 27.7260

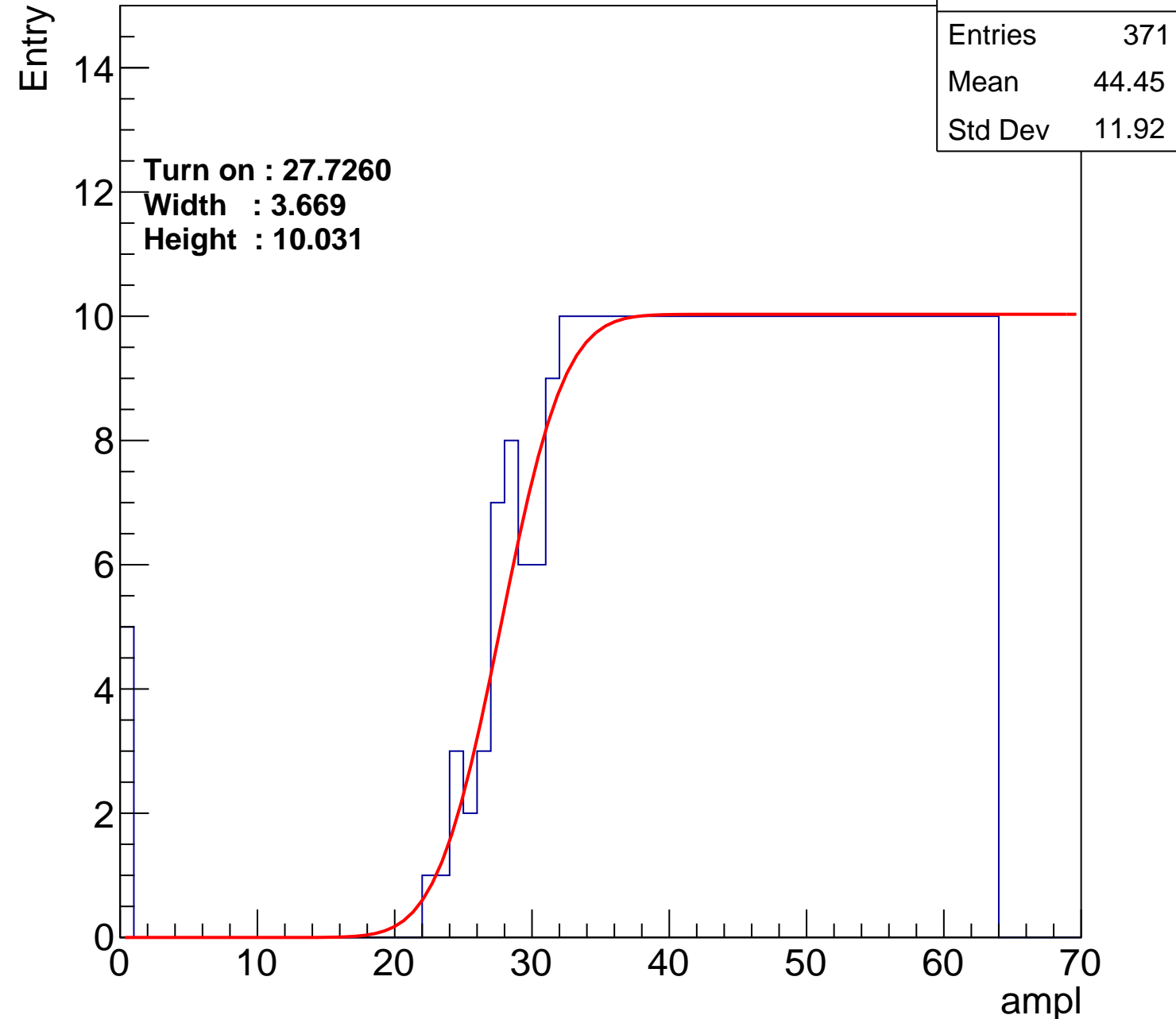
Width : 3.669

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch87

calib_packv5_042523_0143.root, FC#13, port D2

Entries	381
Mean	44.31
Std Dev	11.39

Turn on : 26.5228

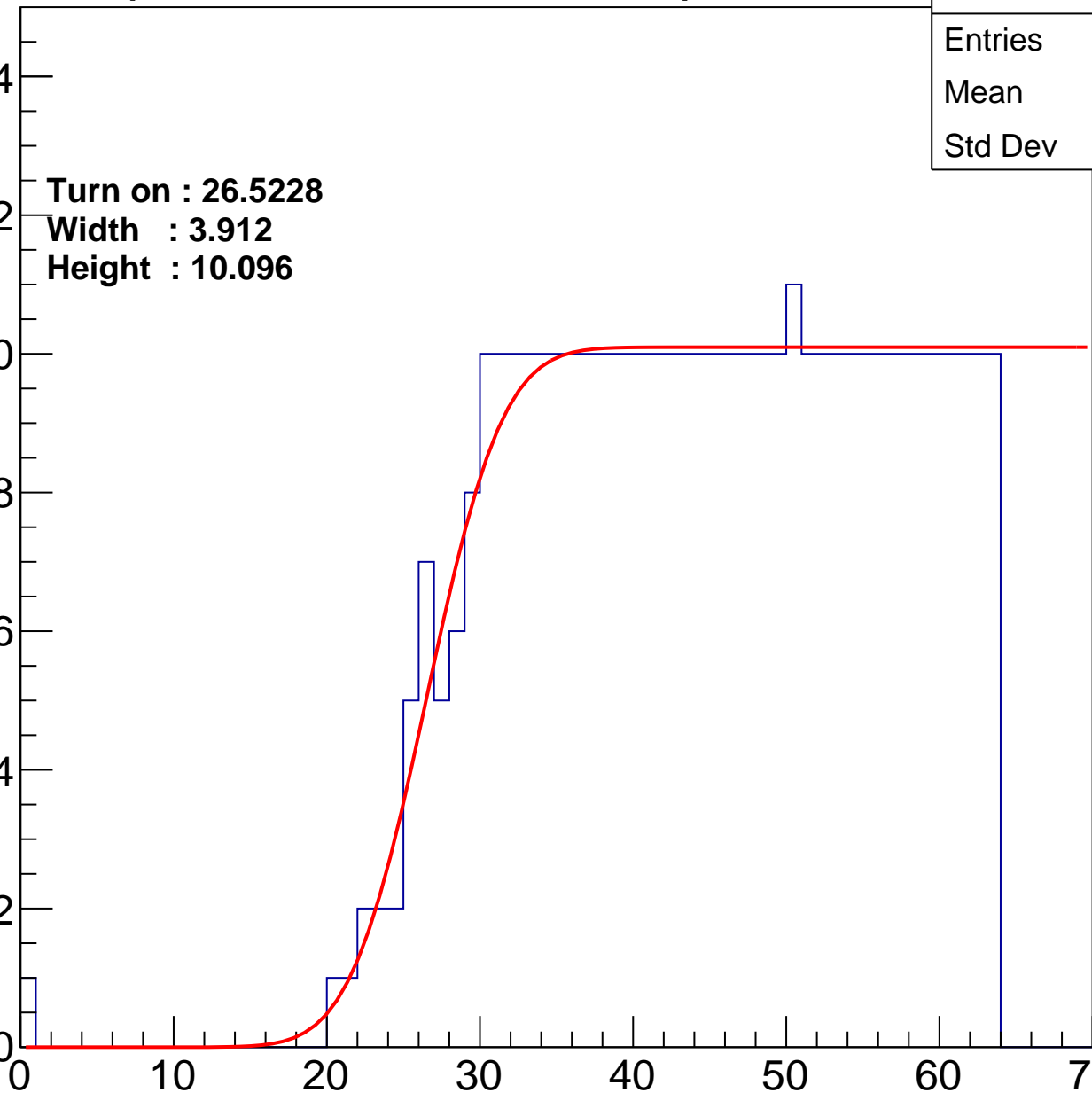
Width : 3.912

Height : 10.096

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch88

calib_packv5_042523_0143.root, FC#13, port D2

Entries	364
Mean	45.08
Std Dev	10.96

Turn on : 28.0265

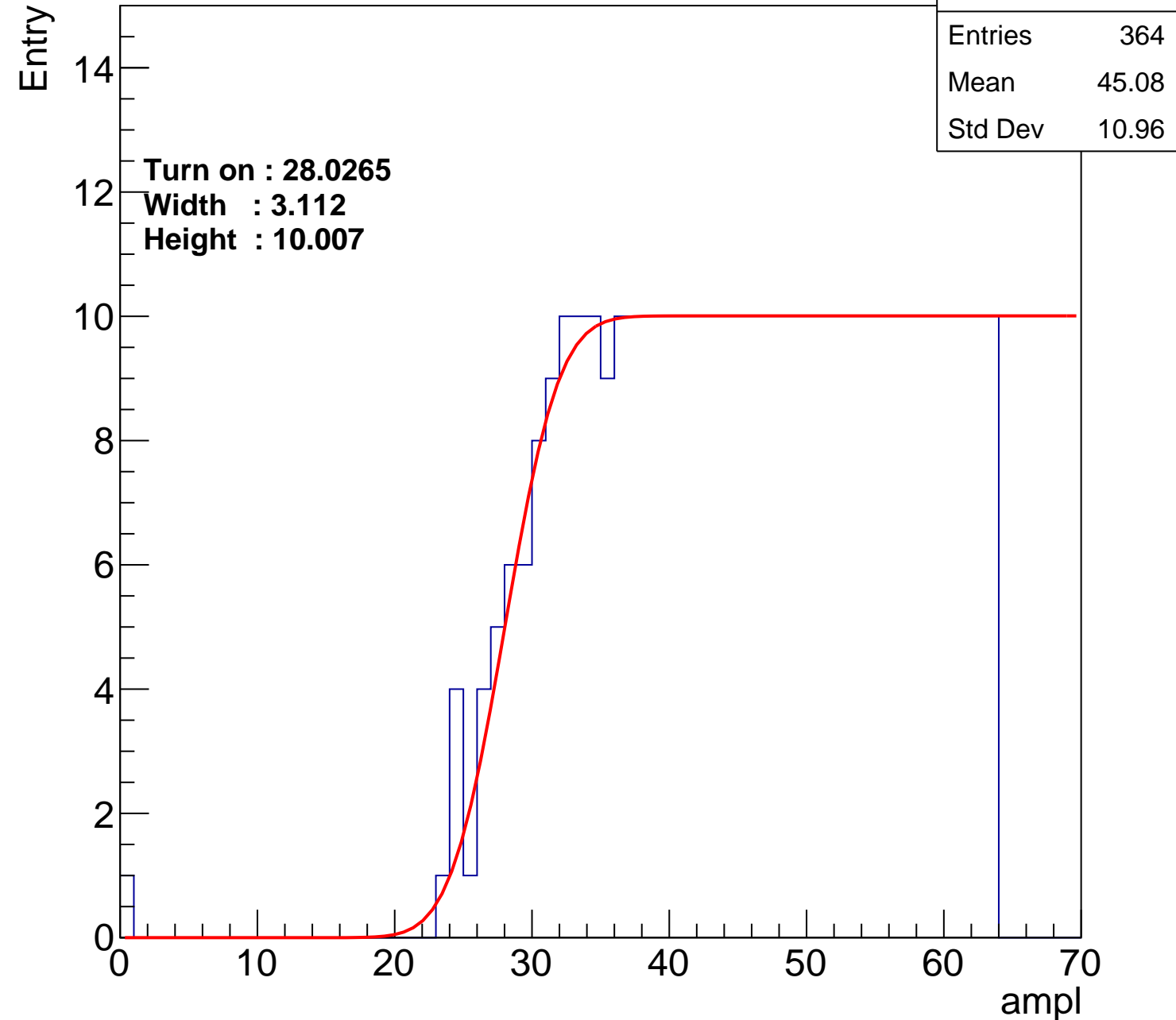
Width : 3.112

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch89

calib_packv5_042523_0143.root, FC#13, port D2

Entries	377
Mean	44.45
Std Dev	11.29

Turn on : 26.4113

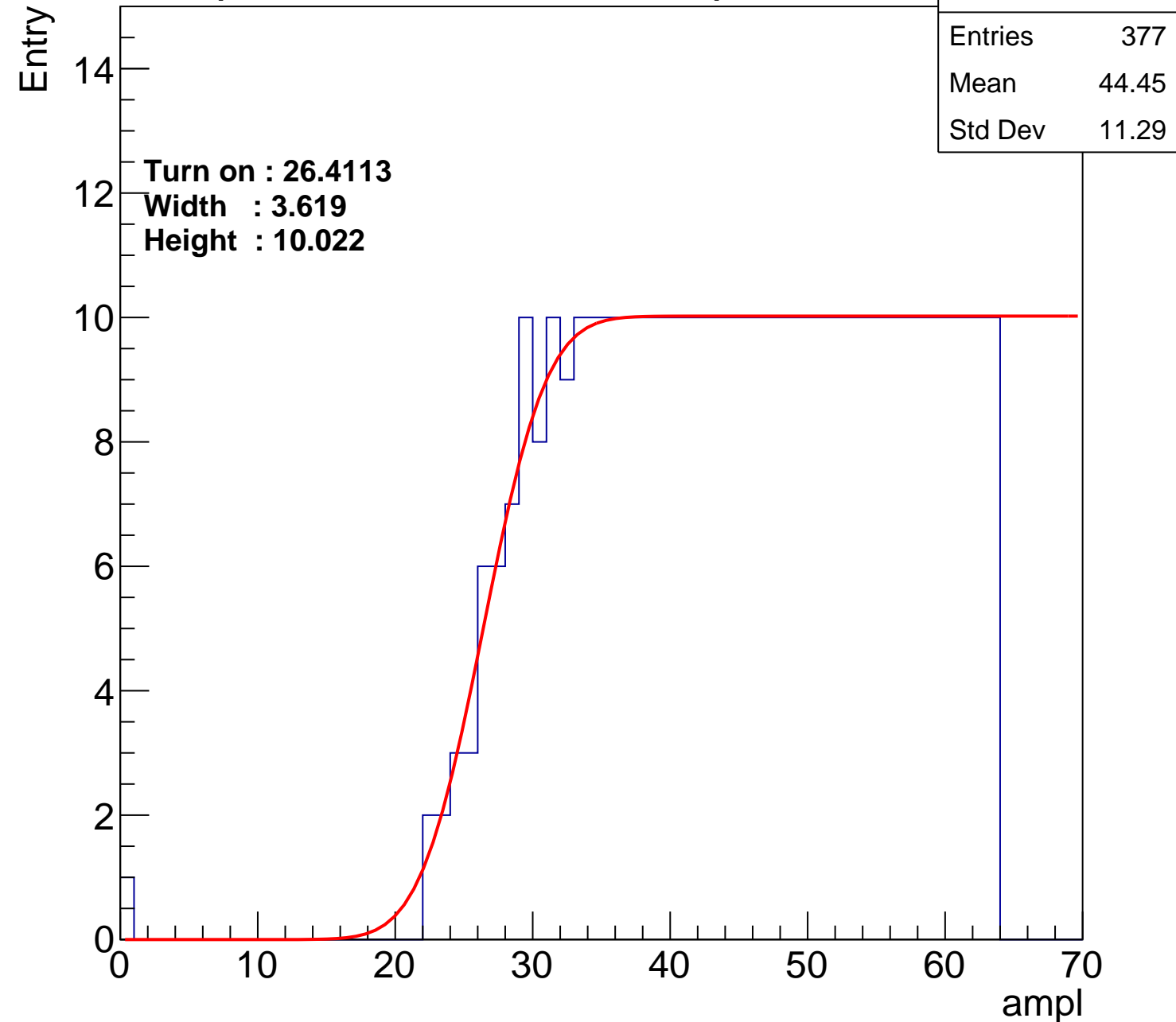
Width : 3.619

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch90

calib_packv5_042523_0143.root, FC#13, port D2

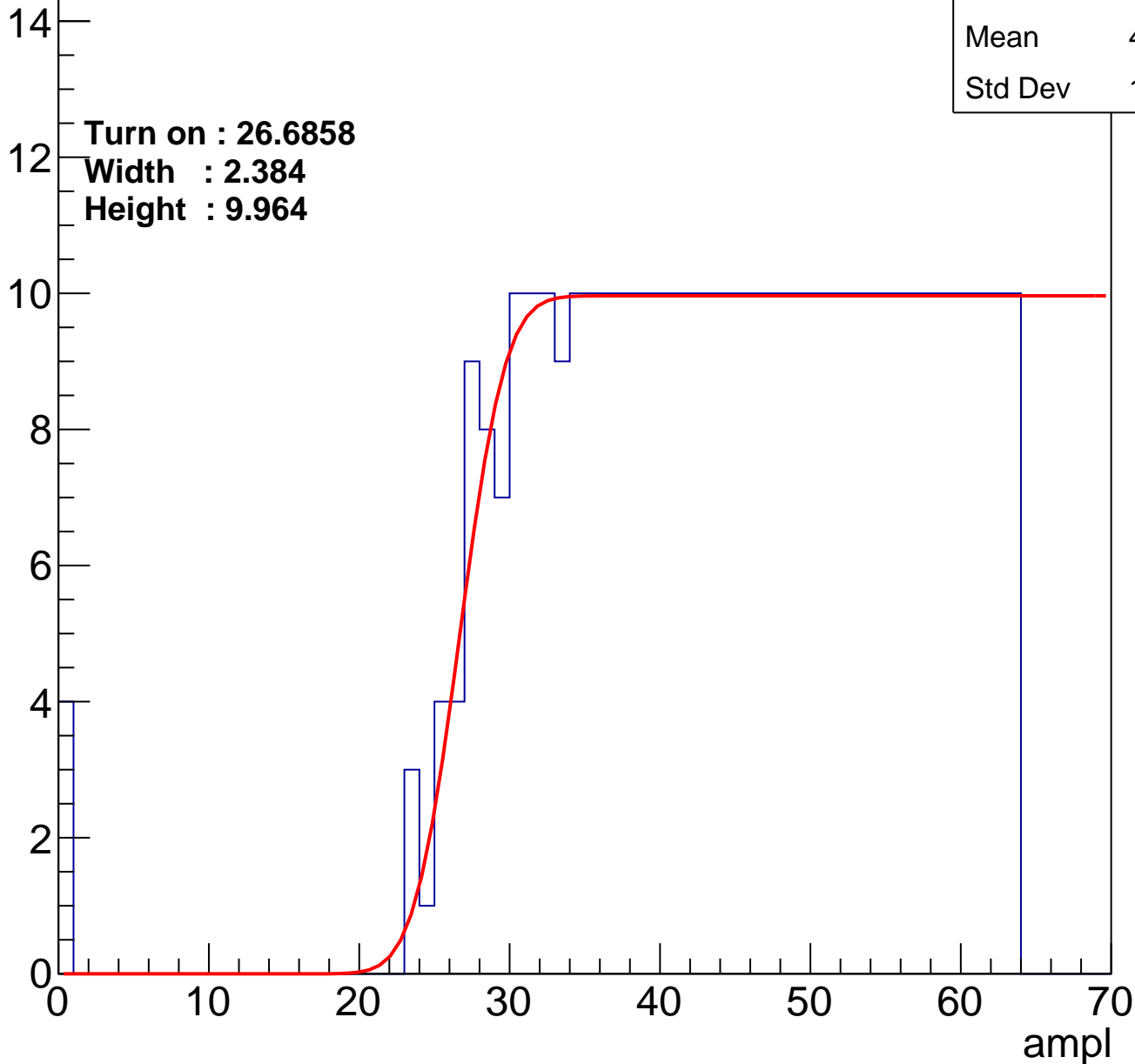
Entry

Entries	379
Mean	44.18
Std Dev	11.84

Turn on : 26.6858

Width : 2.384

Height : 9.964



B1L003S, U1-ch91

calib_packv5_042523_0143.root, FC#13, port D2

Entries	358
Mean	45.3
Std Dev	11.02

Turn on : 28.6602

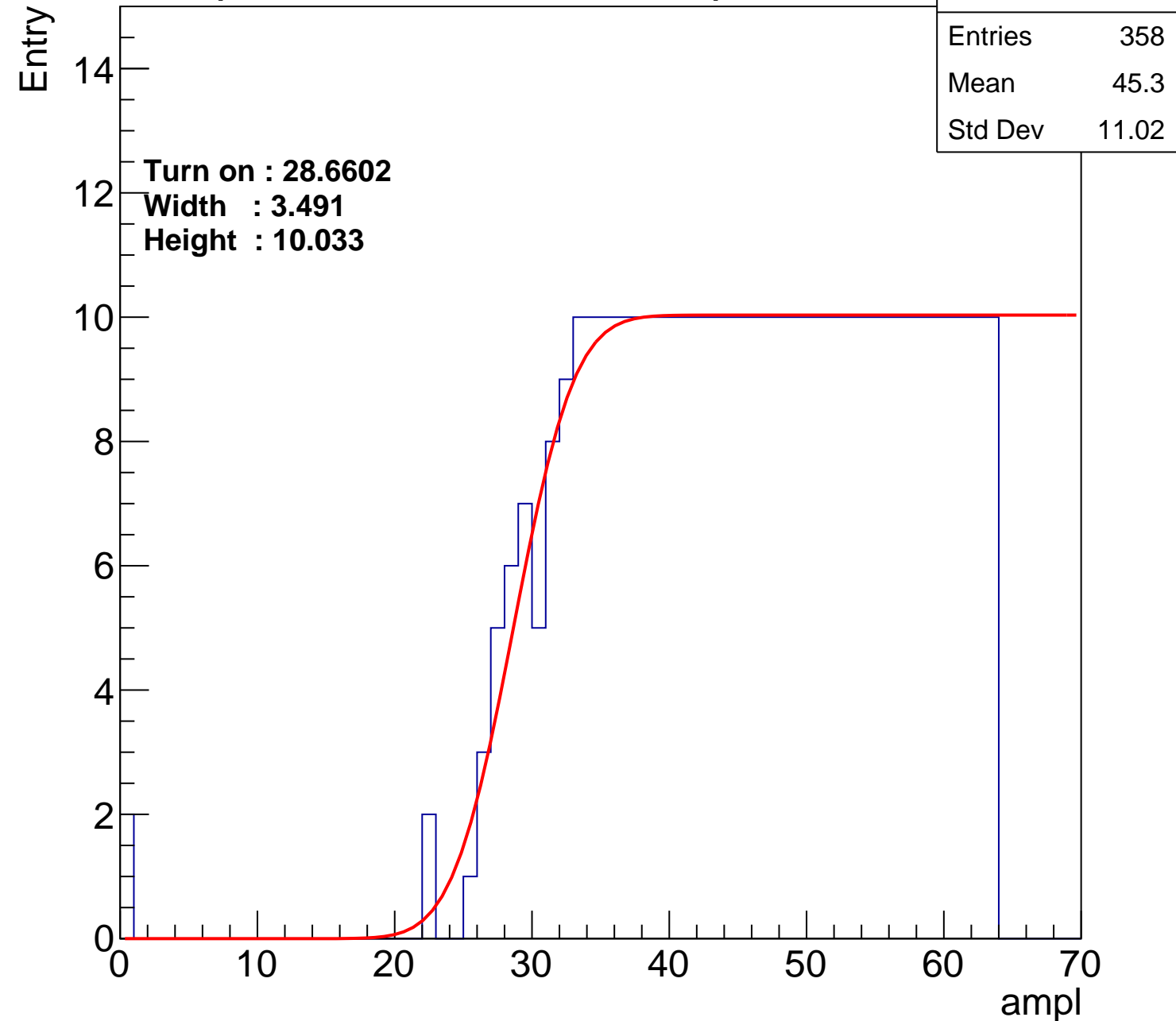
Width : 3.491

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch92

calib_packv5_042523_0143.root, FC#13, port D2

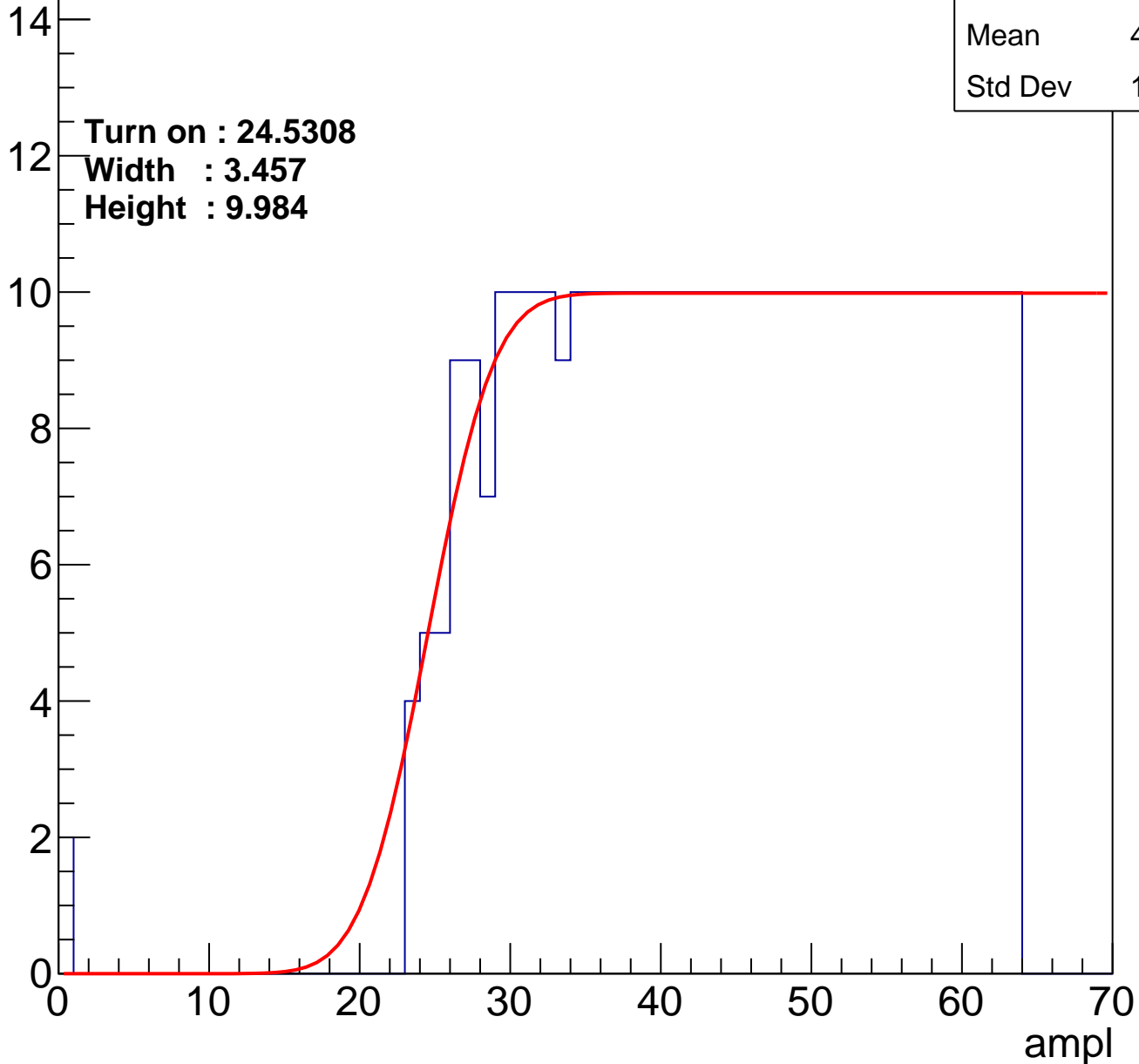
Entries	390
Mean	43.79
Std Dev	11.74

Turn on : 24.5308

Width : 3.457

Height : 9.984

Entry



B1L003S, U1-ch93

calib_packv5_042523_0143.root, FC#13, port D2

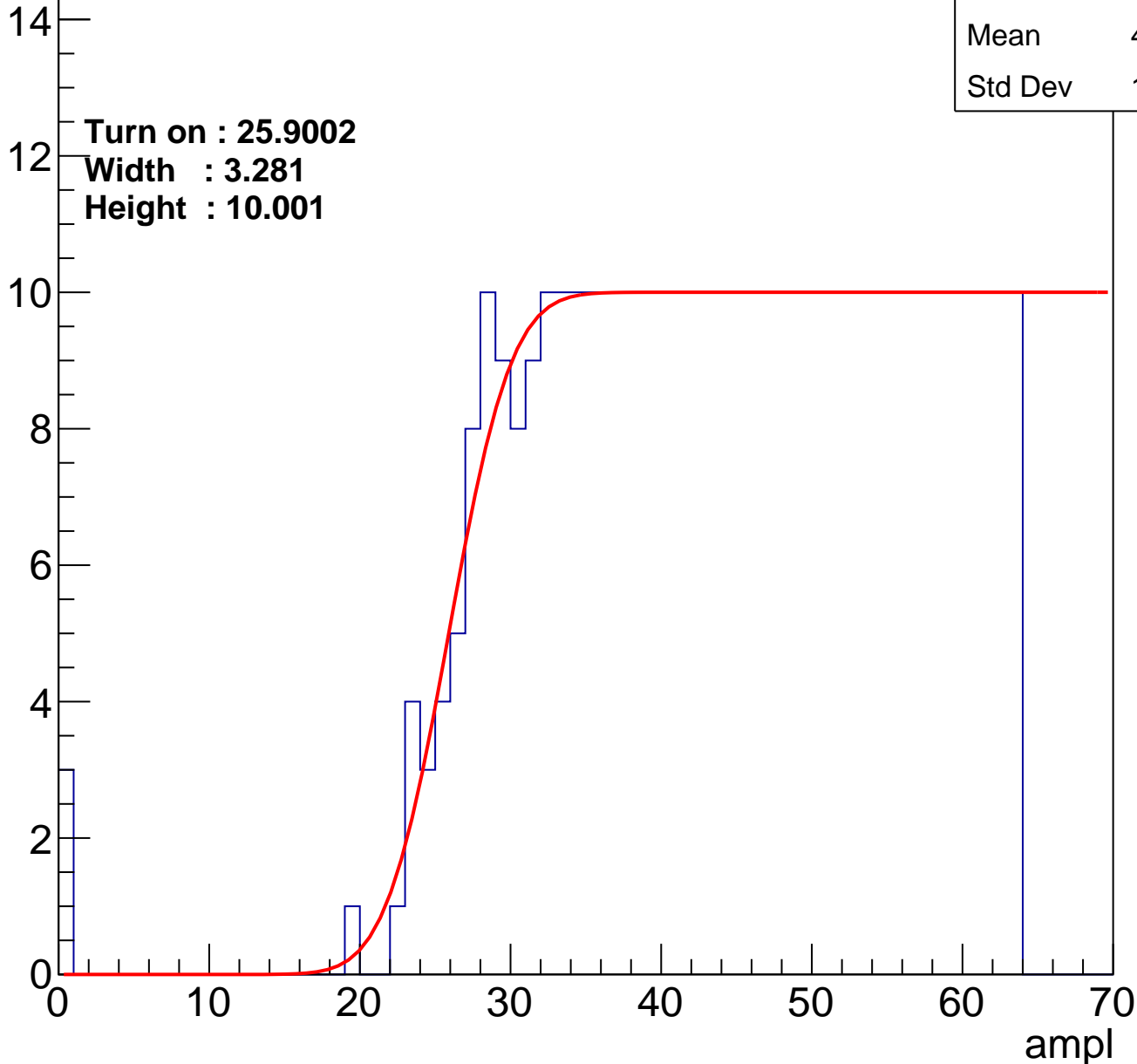
Entries	385
Mean	43.92
Std Dev	11.86

Turn on : 25.9002

Width : 3.281

Height : 10.001

Entry



B1L003S, U1-ch94

calib_packv5_042523_0143.root, FC#13, port D2

Entries	375
Mean	44.47
Std Dev	11.52

Turn on : 26.9687

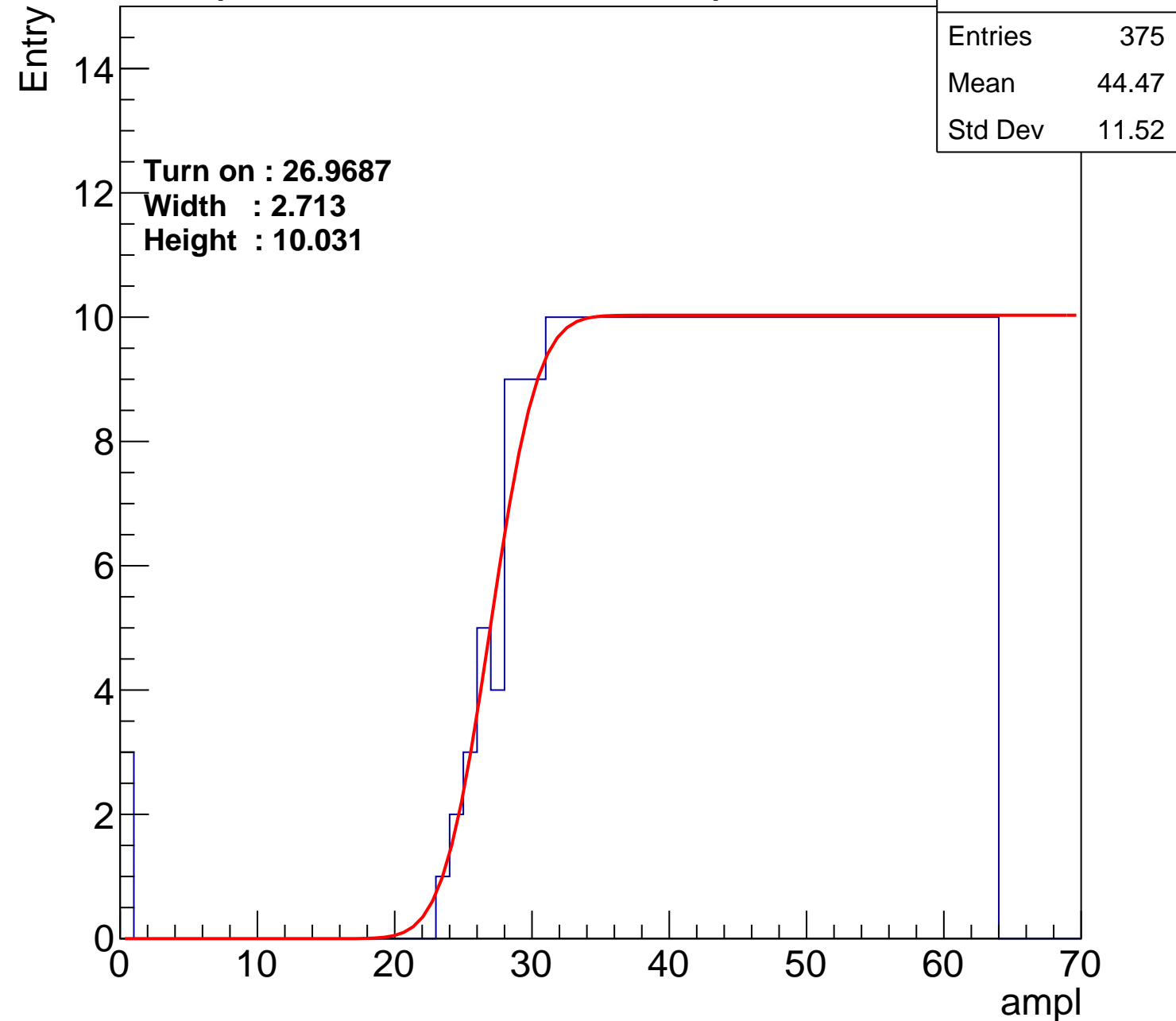
Width : 2.713

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch95

calib_packv5_042523_0143.root, FC#13, port D2

Entries	365
Mean	44.88
Std Dev	11.4

Turn on : 28.1953

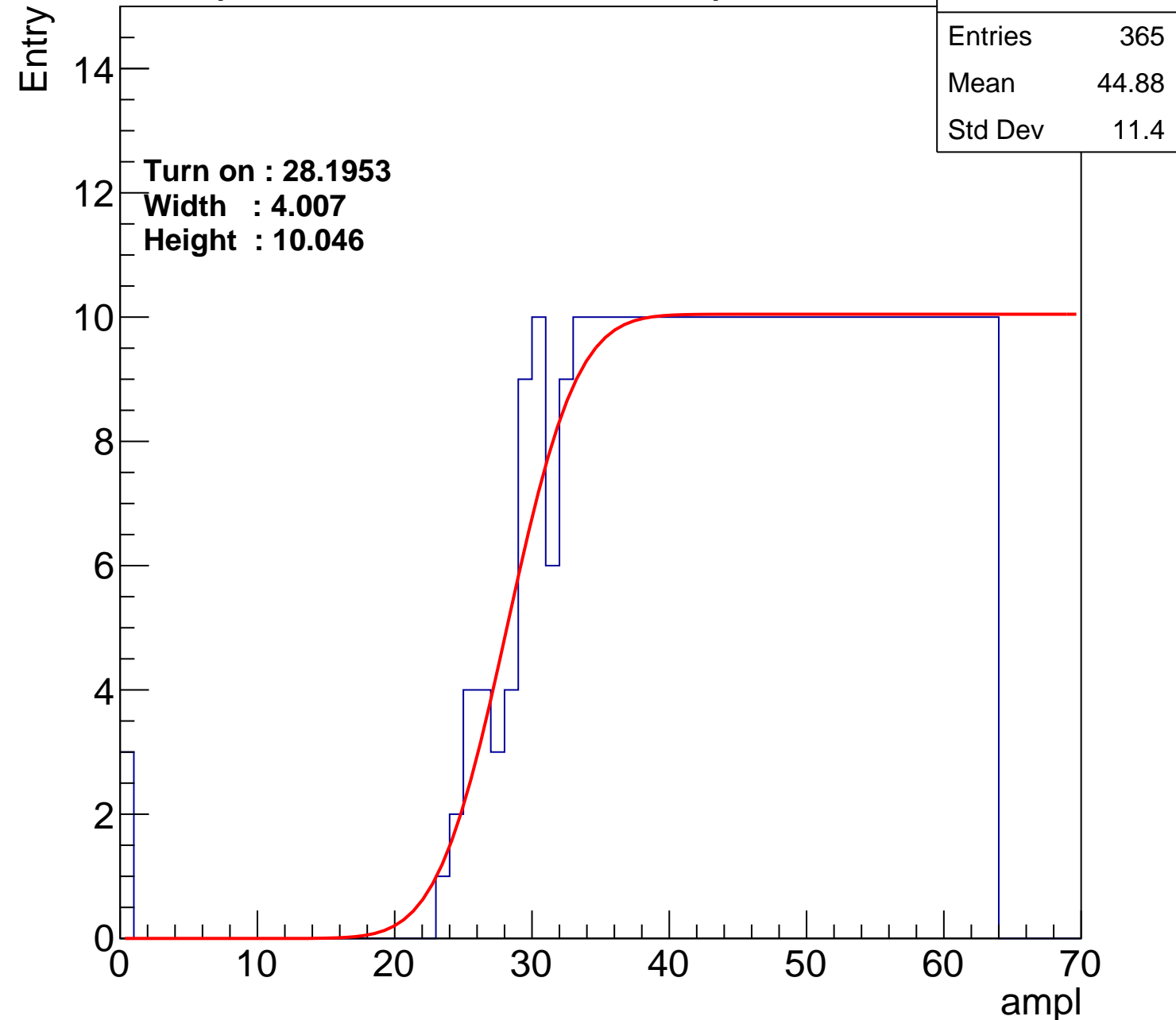
Width : 4.007

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch96

calib_packv5_042523_0143.root, FC#13, port D2

Entries	369
Mean	44.83
Std Dev	11.19

Turn on : 27.6957

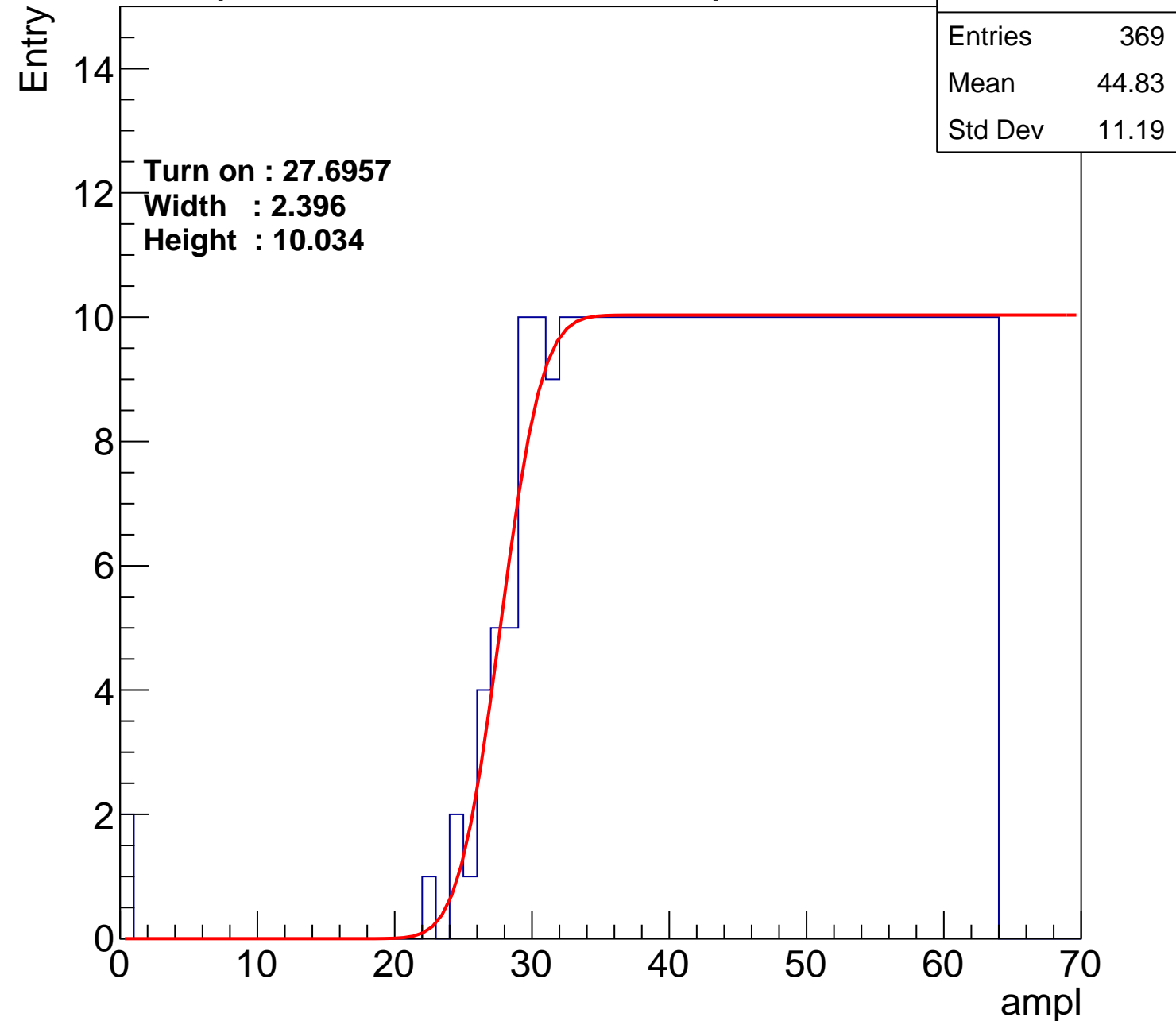
Width : 2.396

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch97

calib_packv5_042523_0143.root, FC#13, port D2

Entries	373
Mean	44.68
Std Dev	11.13

Turn on : 27.3308

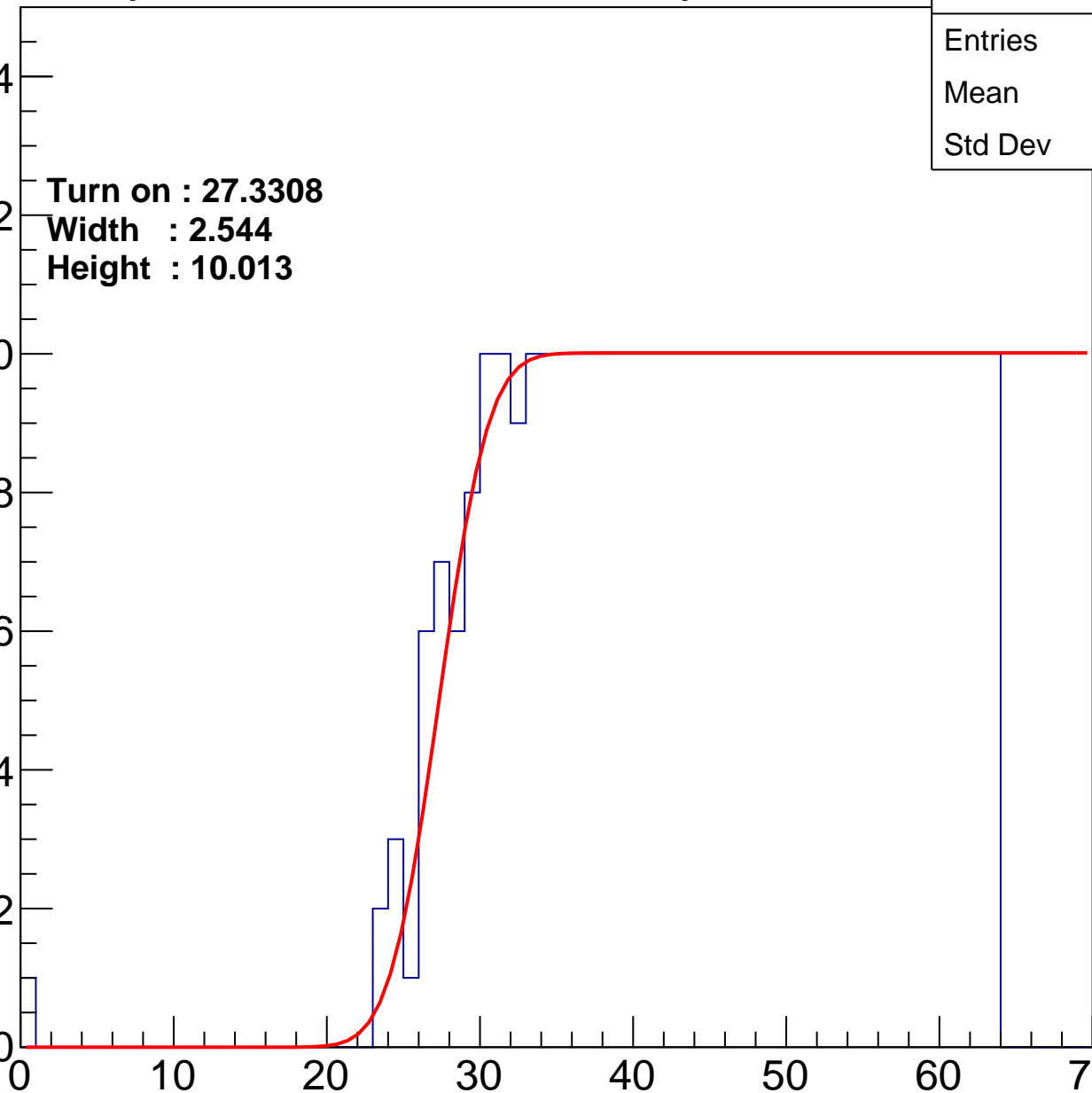
Width : 2.544

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch98

calib_packv5_042523_0143.root, FC#13, port D2

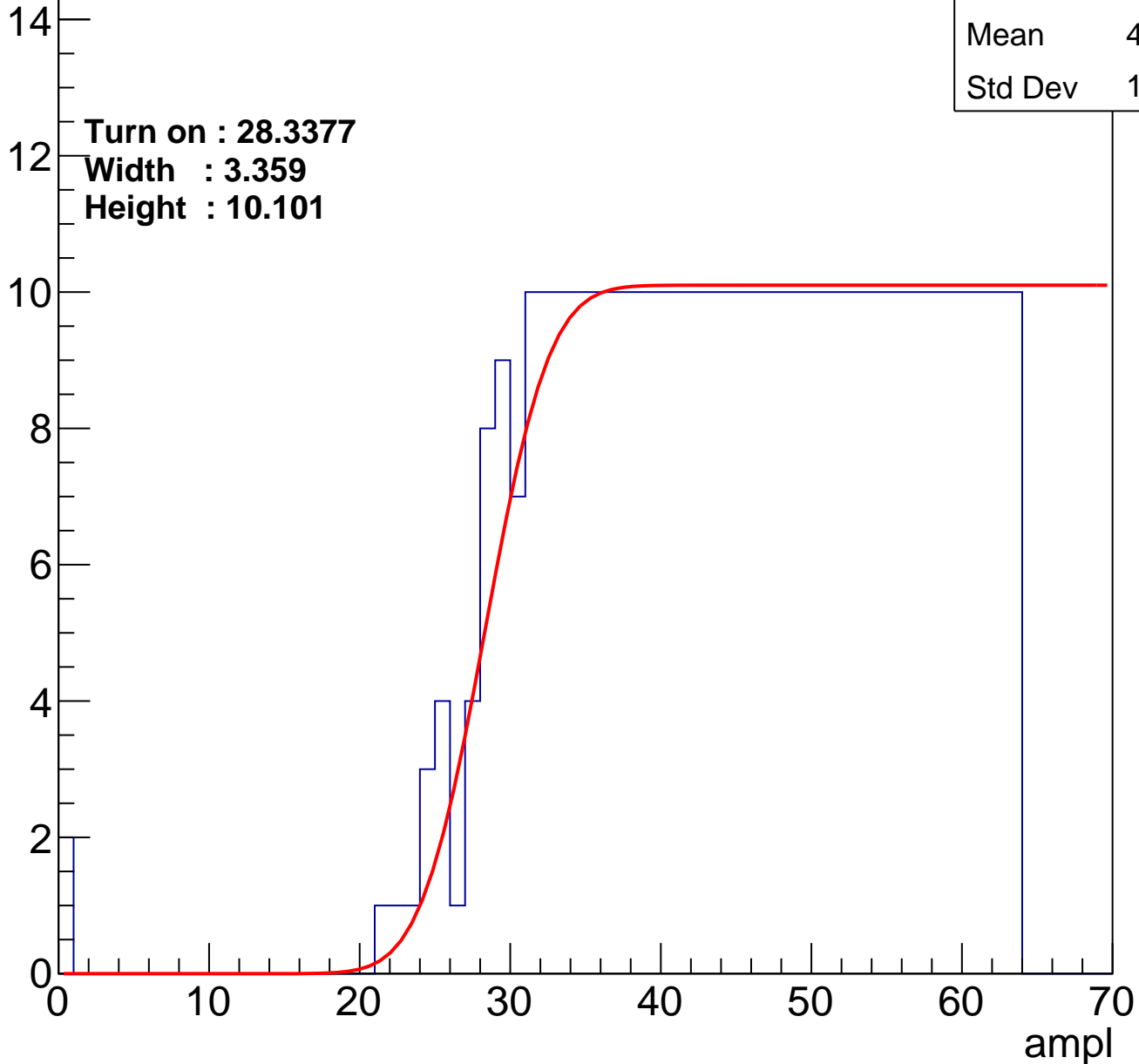
Entries	371
Mean	44.68
Std Dev	11.33

Turn on : 28.3377

Width : 3.359

Height : 10.101

Entry



B1L003S, U1-ch99

calib_packv5_042523_0143.root, FC#13, port D2

Entries	385
Mean	43.85
Std Dev	12.06

Turn on : 25.9055

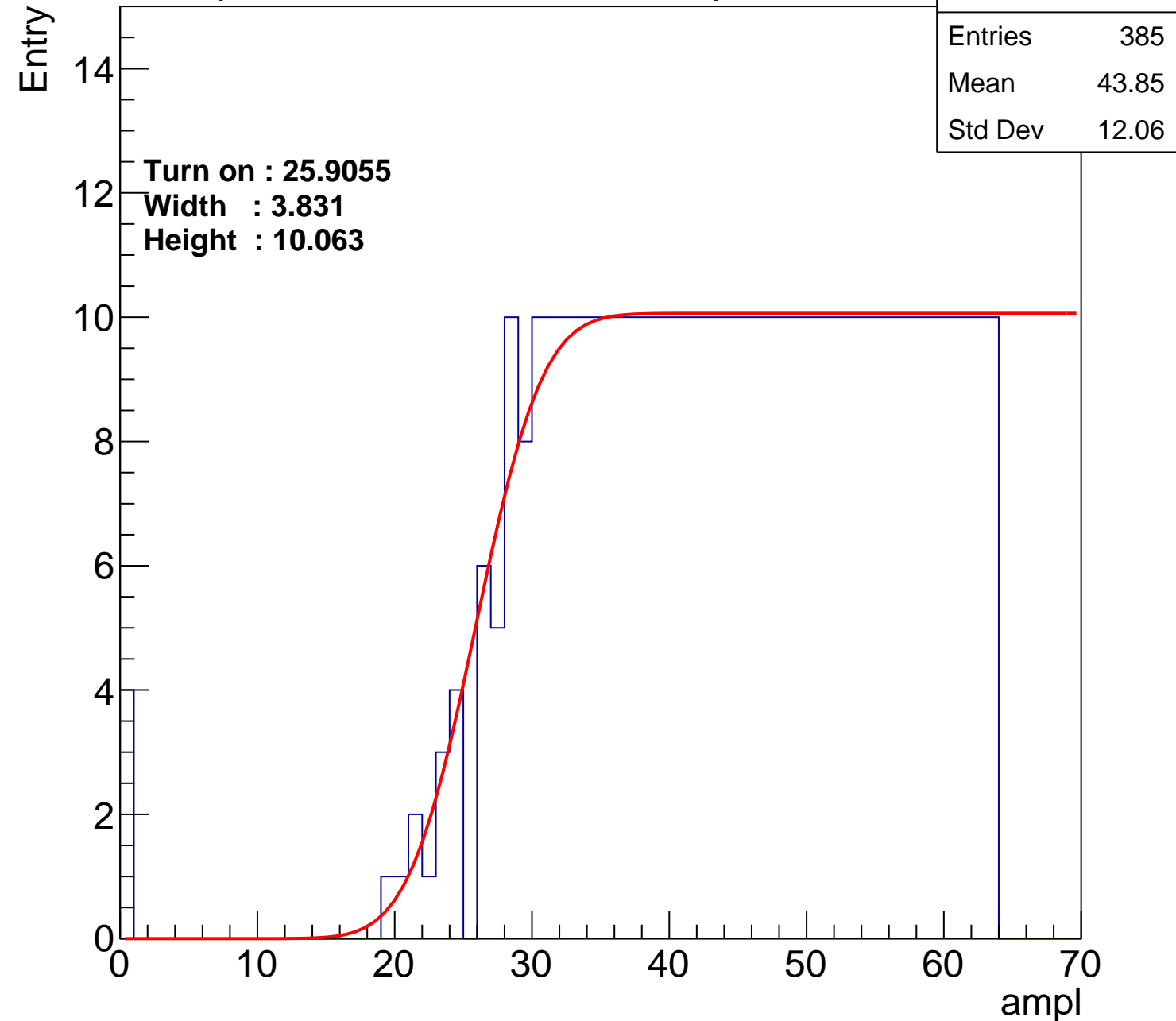
Width : 3.831

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch100

calib_packv5_042523_0143.root, FC#13, port D2

Entries	386
Mean	43.88
Std Dev	11.94

Turn on : 25.6081

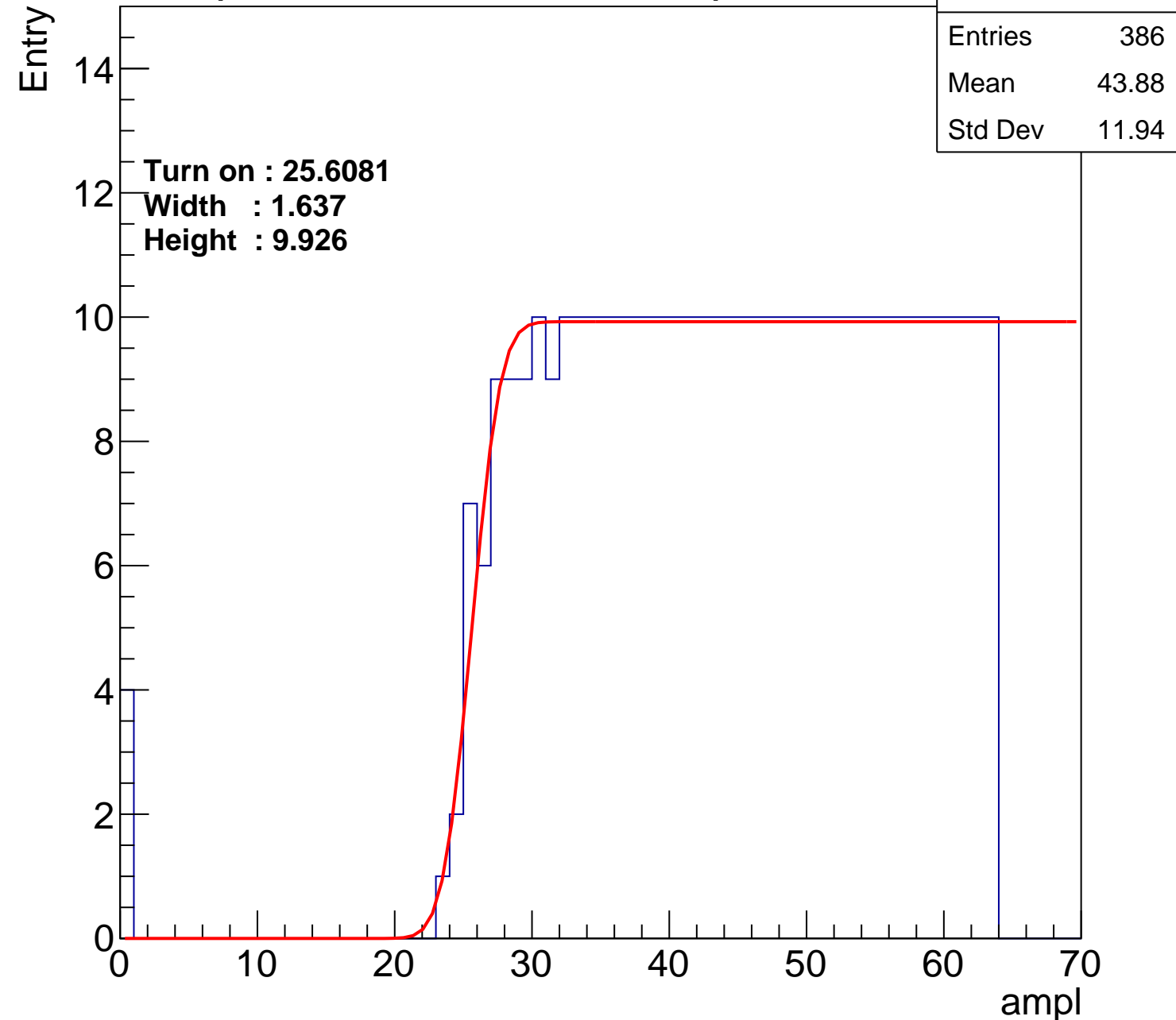
Width : 1.637

Height : 9.926

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch101

calib_packv5_042523_0143.root, FC#13, port D2

Entries	370
Mean	44.63
Std Dev	11.62

Turn on : 27.5621

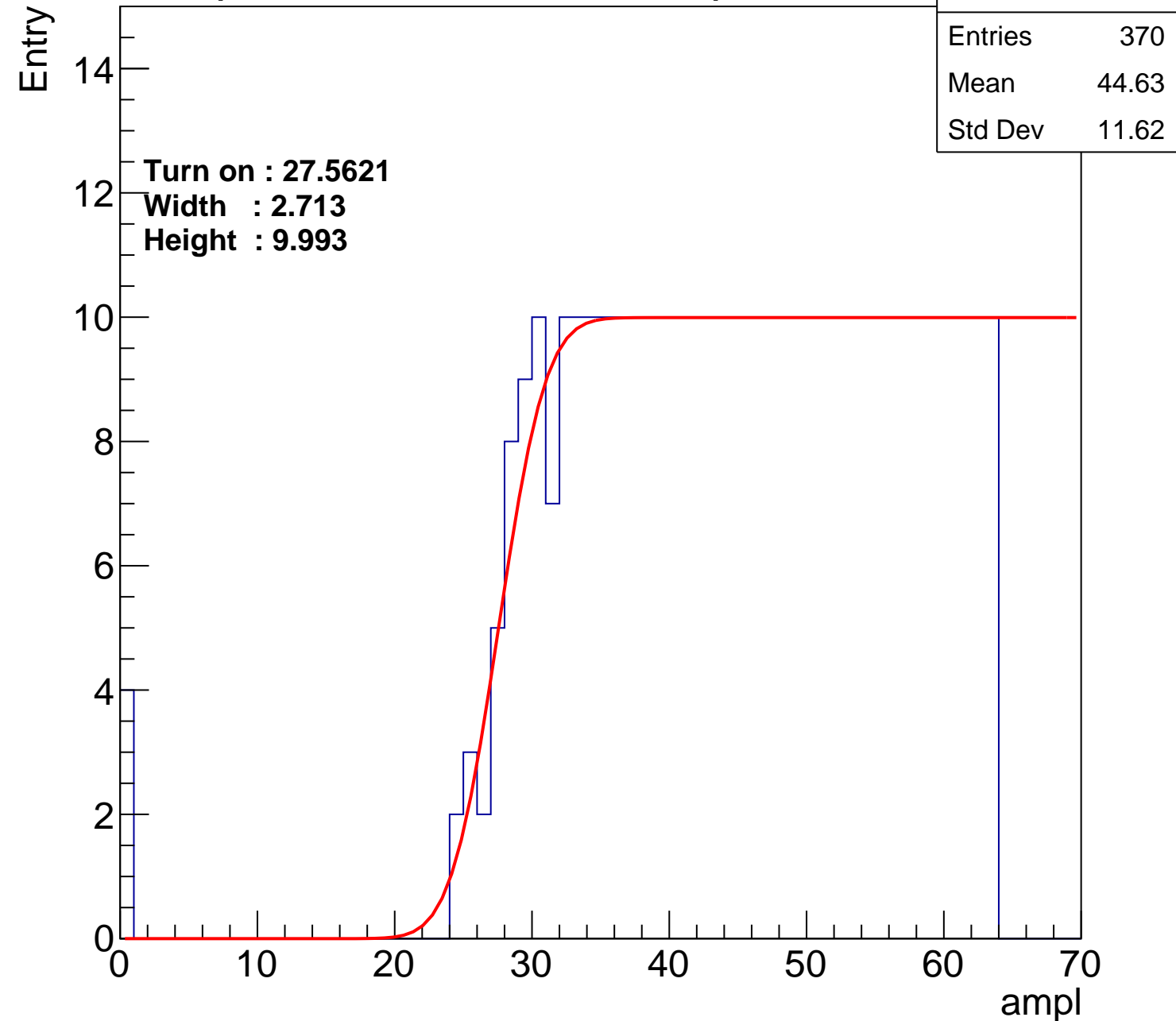
Width : 2.713

Height : 9.993

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch102

calib_packv5_042523_0143.root, FC#13, port D2

Entries	377
Mean	44.37
Std Dev	11.5

Turn on : 26.5946

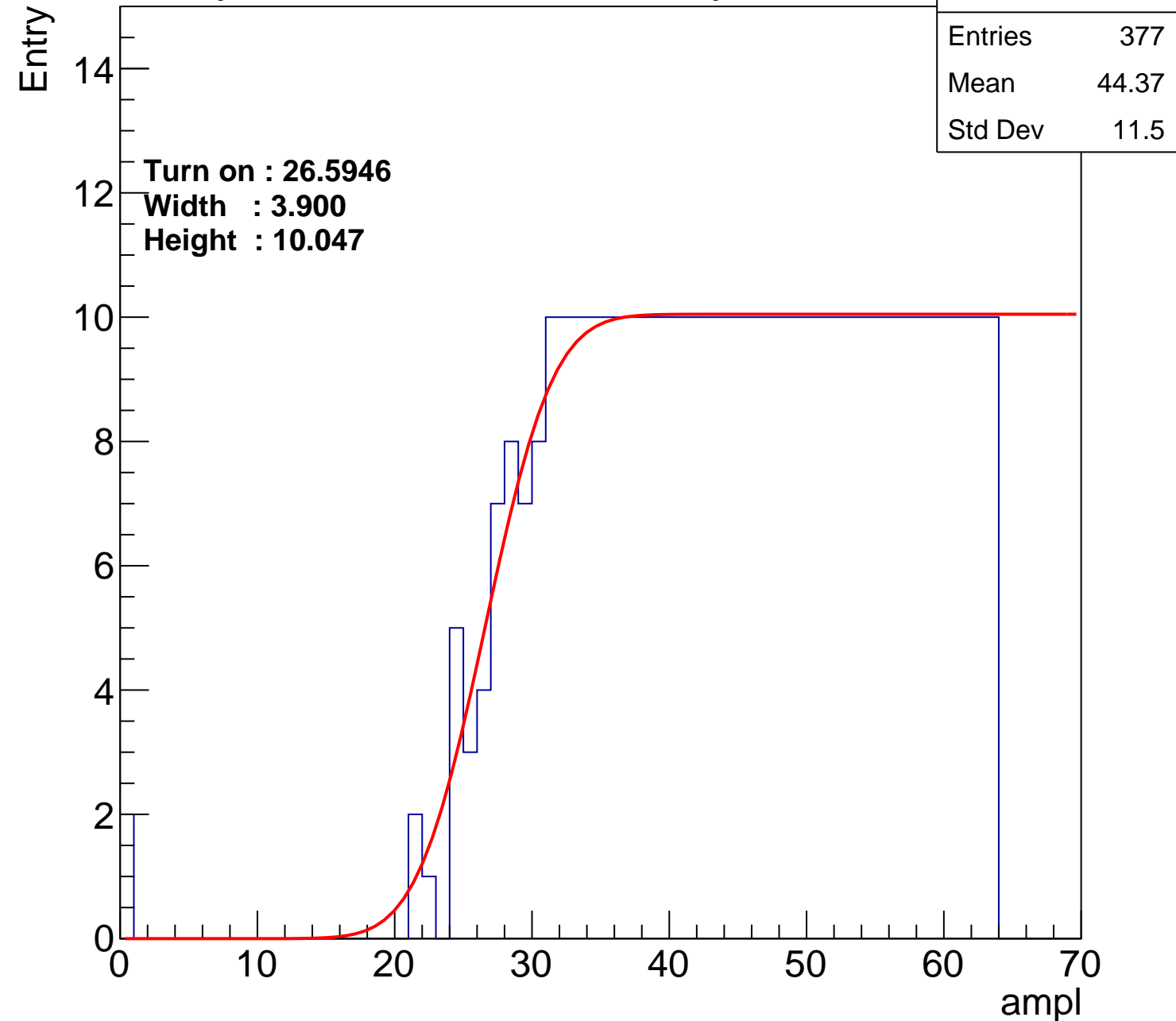
Width : 3.900

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch103

calib_packv5_042523_0143.root, FC#13, port D2

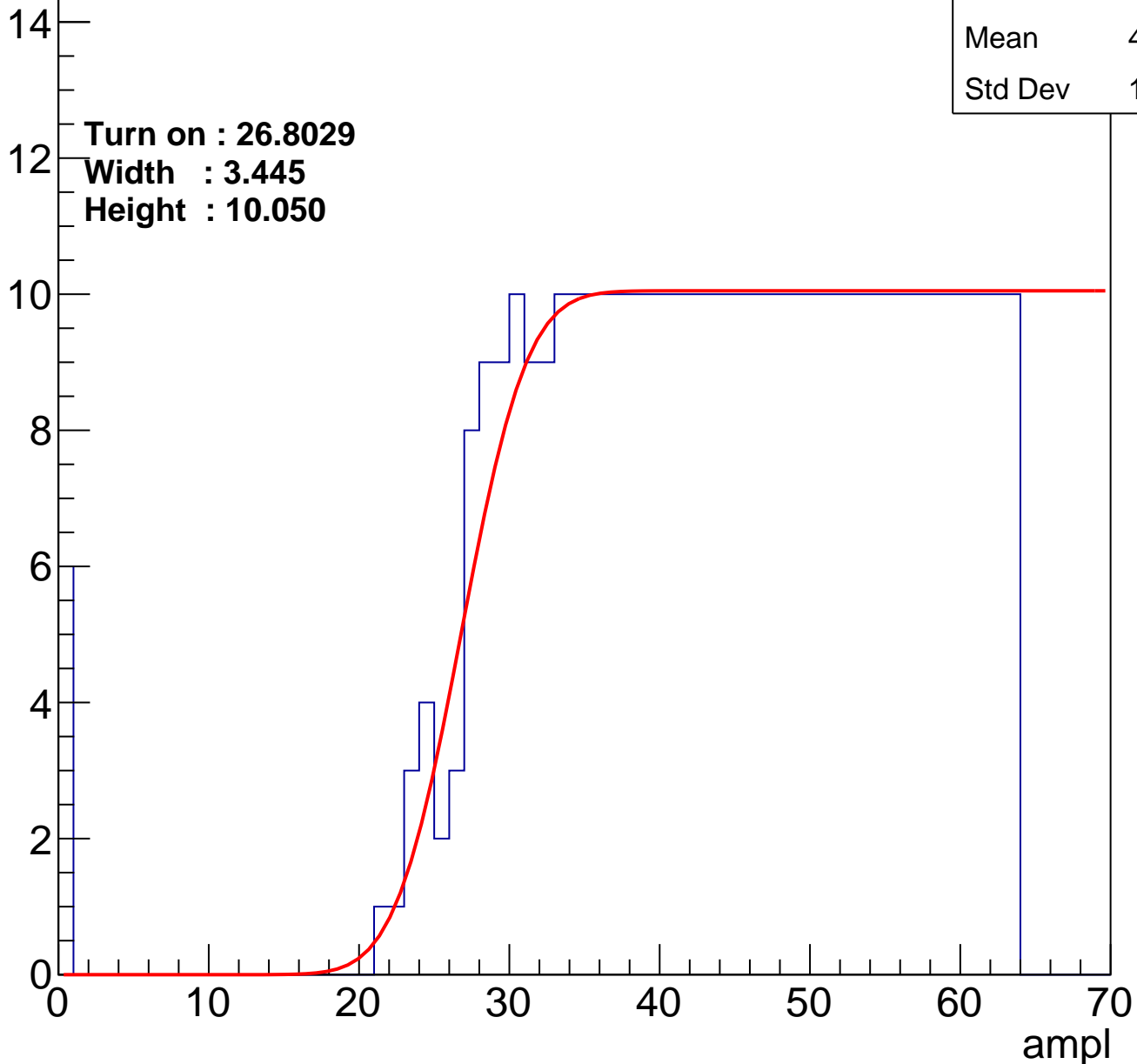
Entries	384
Mean	43.78
Std Dev	12.33

Turn on : 26.8029

Width : 3.445

Height : 10.050

Entry



B1L003S, U1-ch104

calib_packv5_042523_0143.root, FC#13, port D2

Entries	378
Mean	44.23
Std Dev	11.83

Turn on : 26.9797

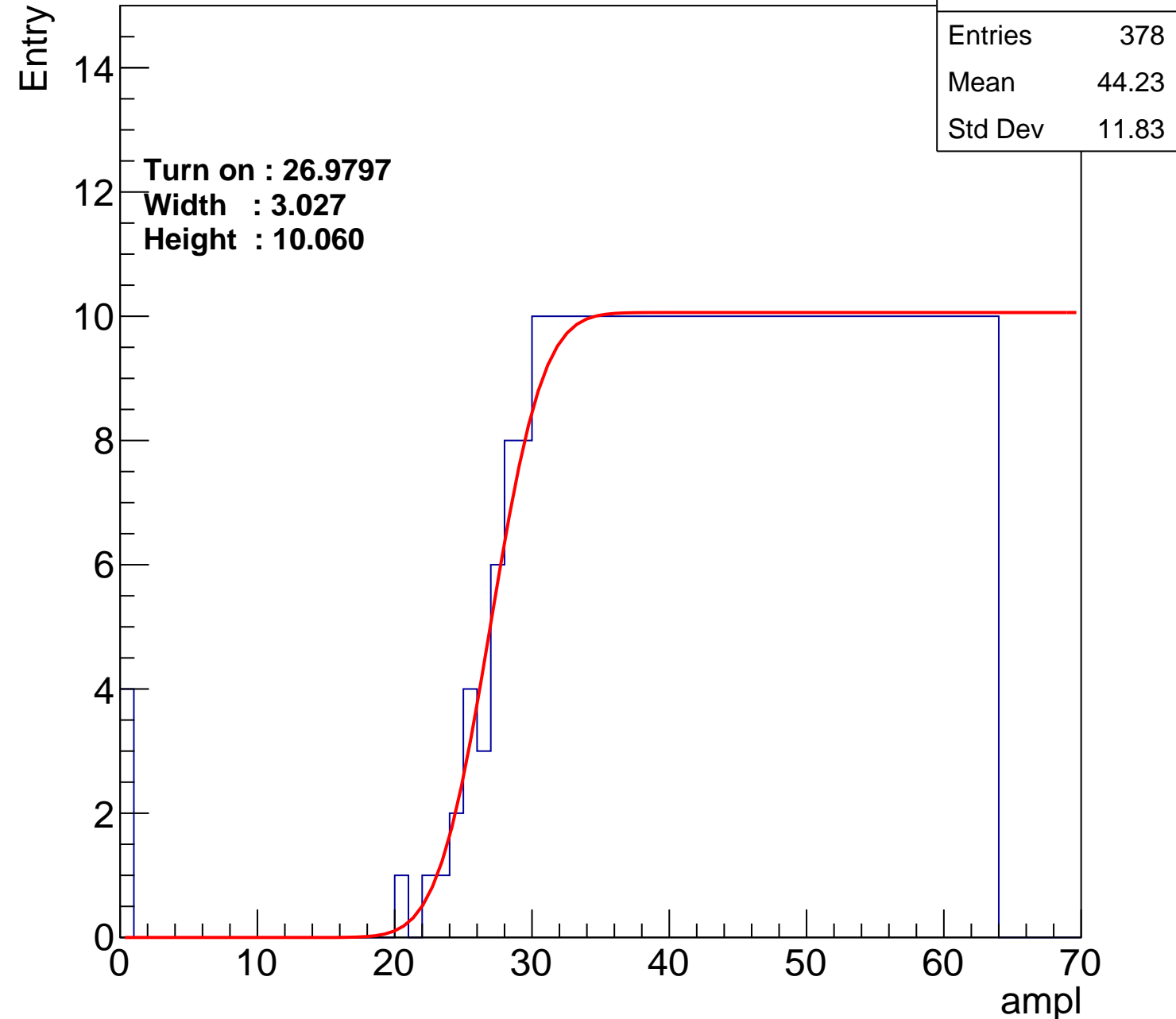
Width : 3.027

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch105

calib_packv5_042523_0143.root, FC#13, port D2

Entries	358
Mean	45.21
Std Dev	11.36

Turn on : 29.0361

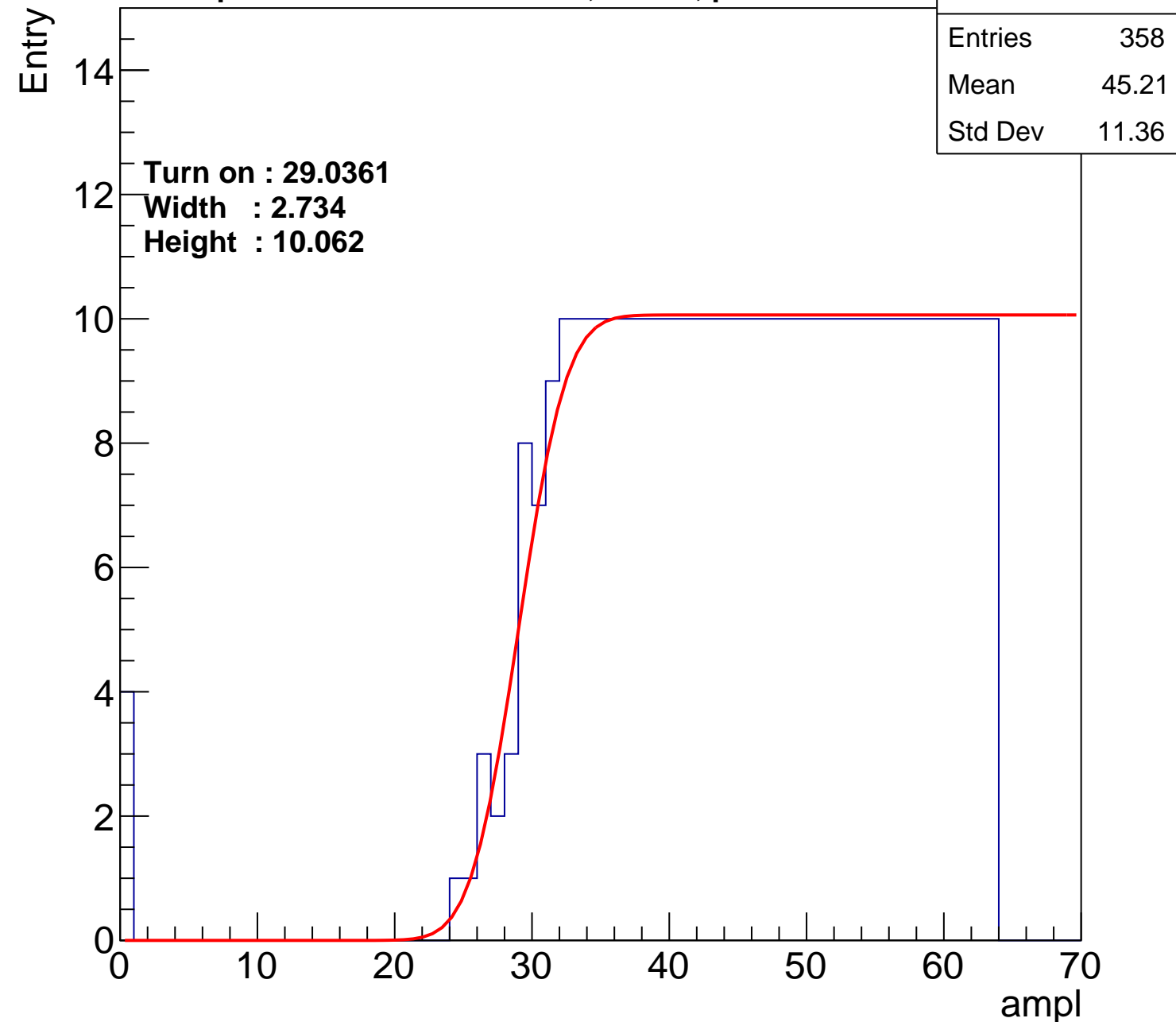
Width : 2.734

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch106

calib_packv5_042523_0143.root, FC#13, port D2

Entries	380
Mean	44.14
Std Dev	11.85

Turn on : 26.3179

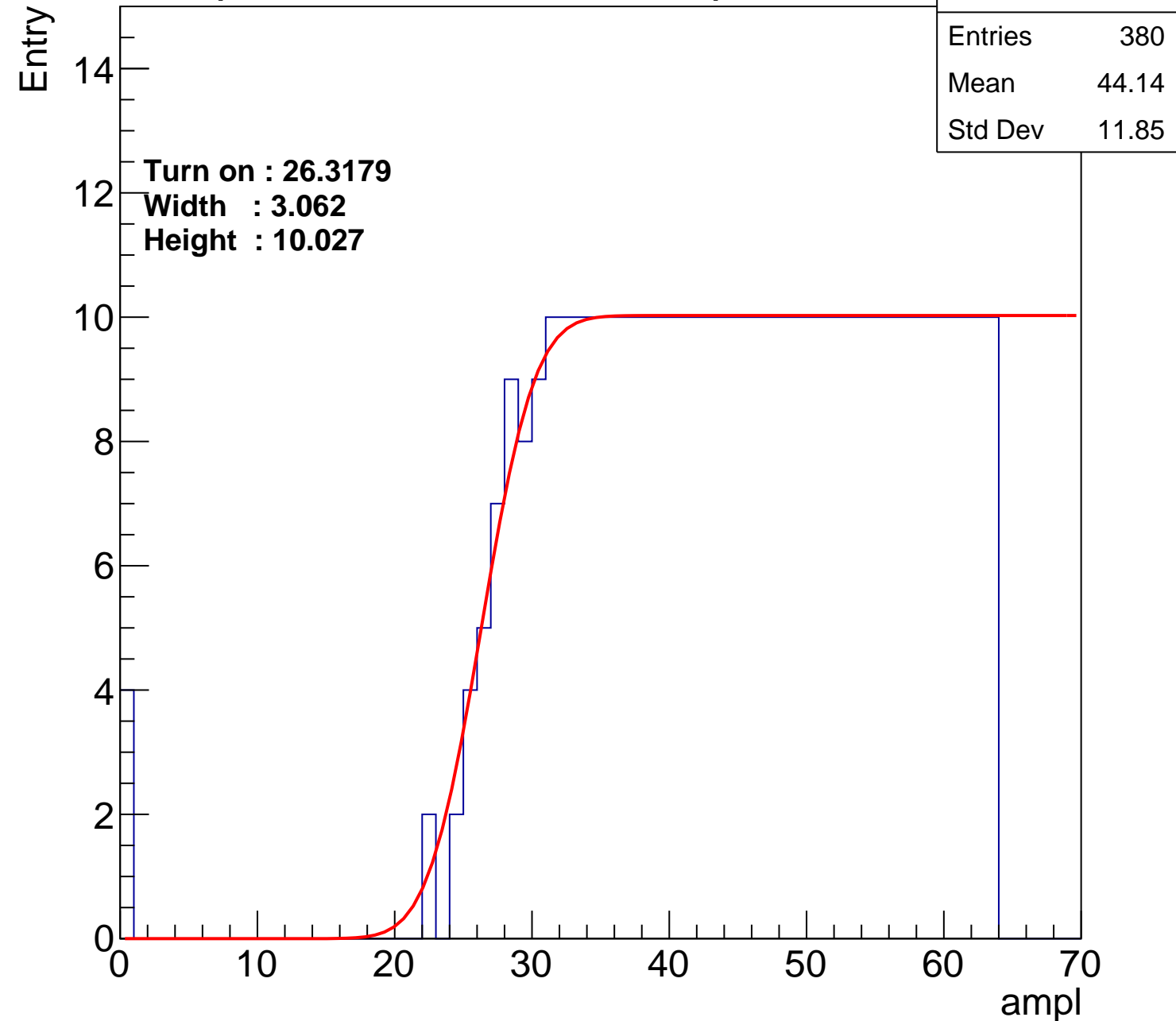
Width : 3.062

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch107

calib_packv5_042523_0143.root, FC#13, port D2

Entries	359
Mean	45.11
Std Dev	11.47

Turn on : 28.9840

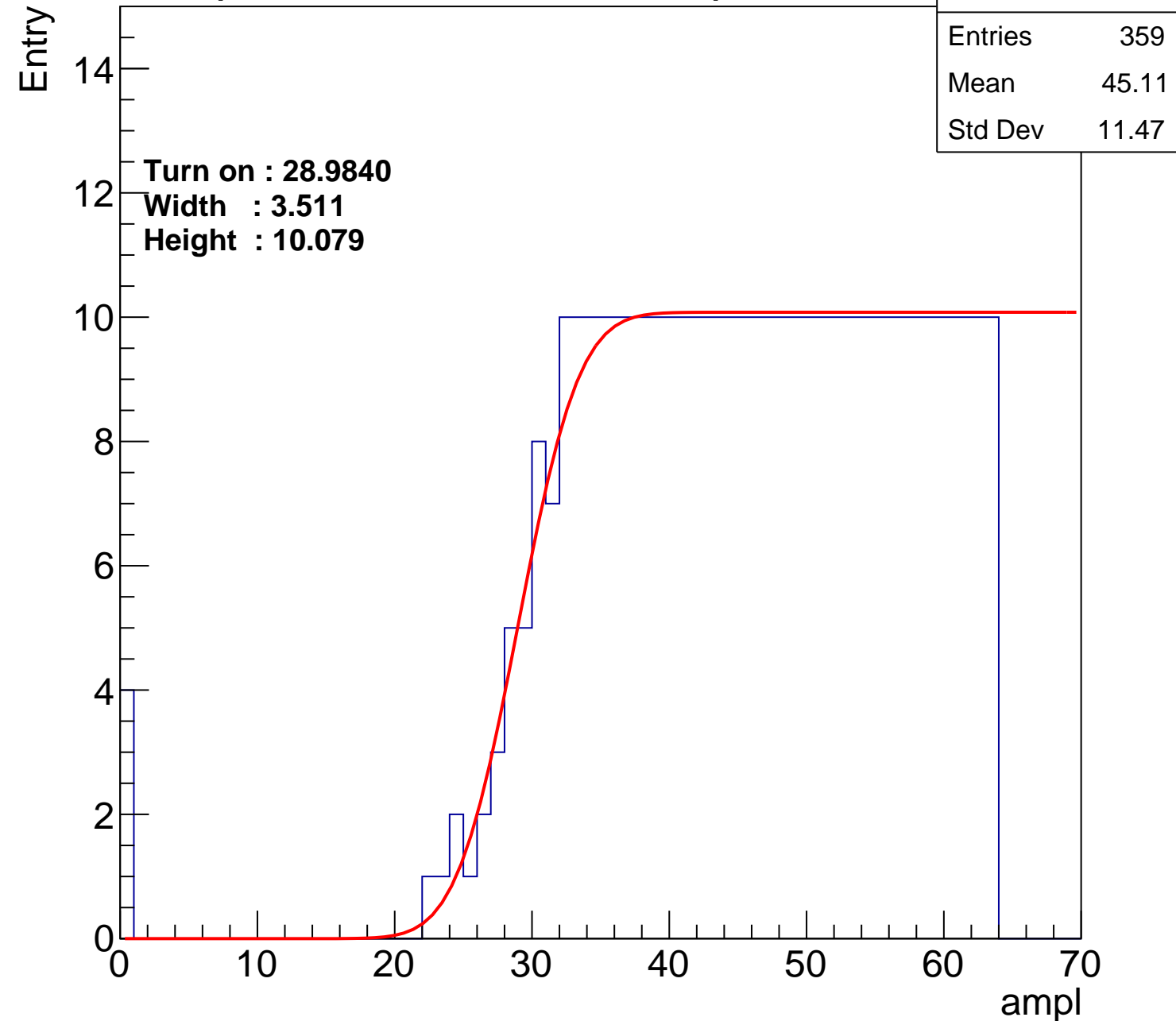
Width : 3.511

Height : 10.079

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch108

calib_packv5_042523_0143.root, FC#13, port D2

Entries	383
Mean	43.93
Std Dev	12.09

Turn on : 26.3424

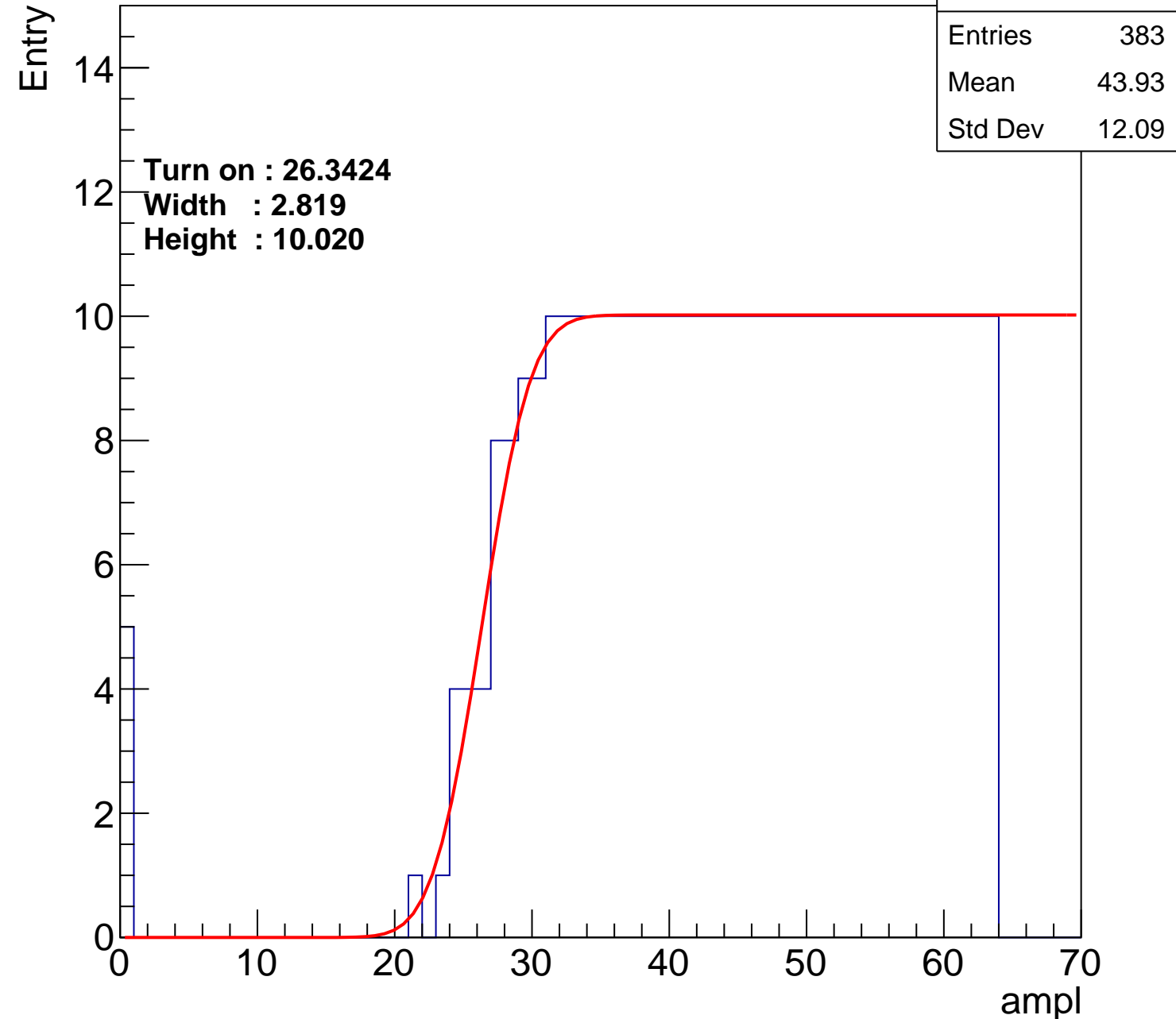
Width : 2.819

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch109

calib_packv5_042523_0143.root, FC#13, port D2

Entries	381
Mean	44.29
Std Dev	11.33

Turn on : 26.0414

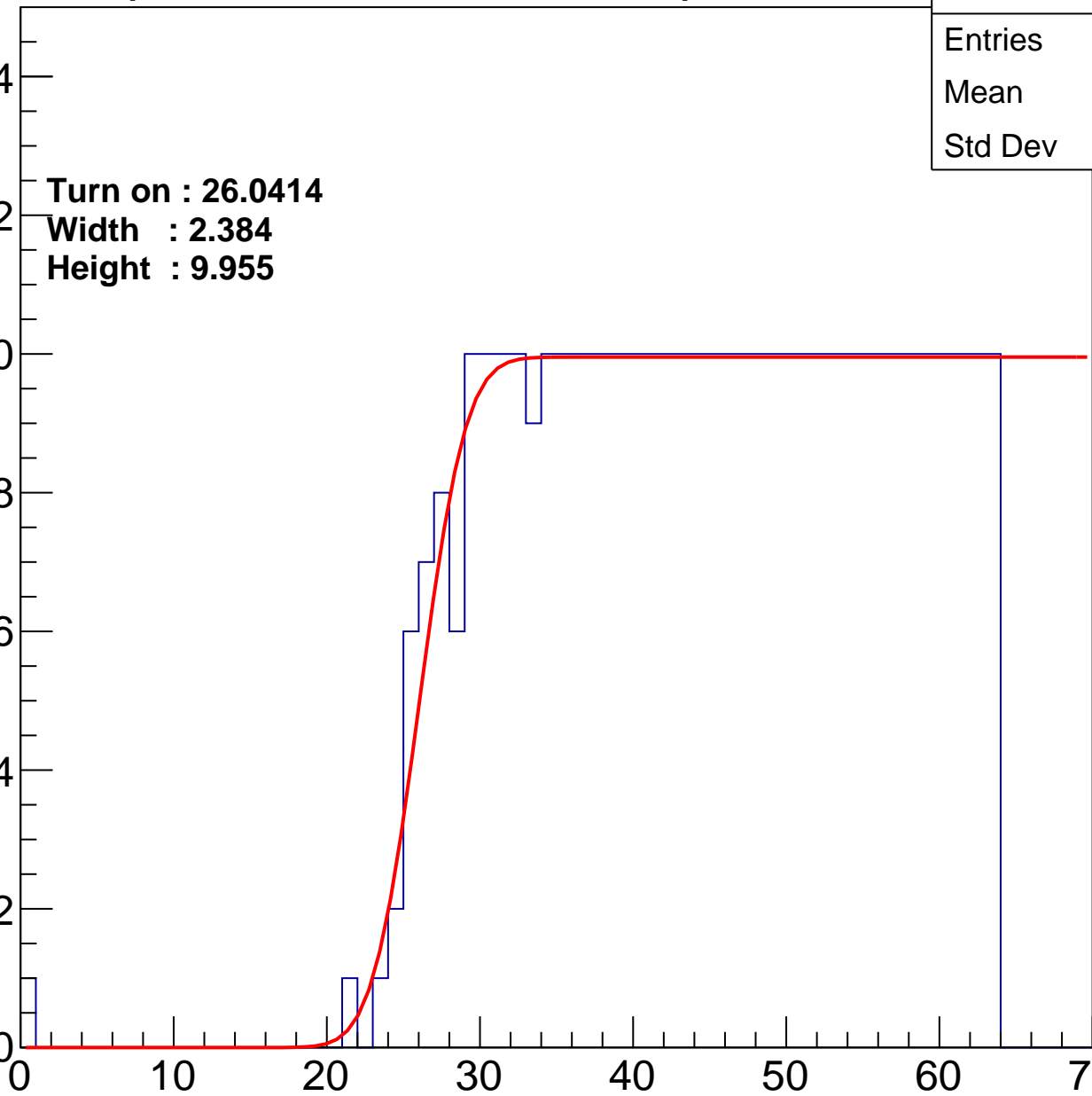
Width : 2.384

Height : 9.955

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch110

calib_packv5_042523_0143.root, FC#13, port D2

Entries	378
Mean	44.15
Std Dev	11.94

Turn on : 26.5522

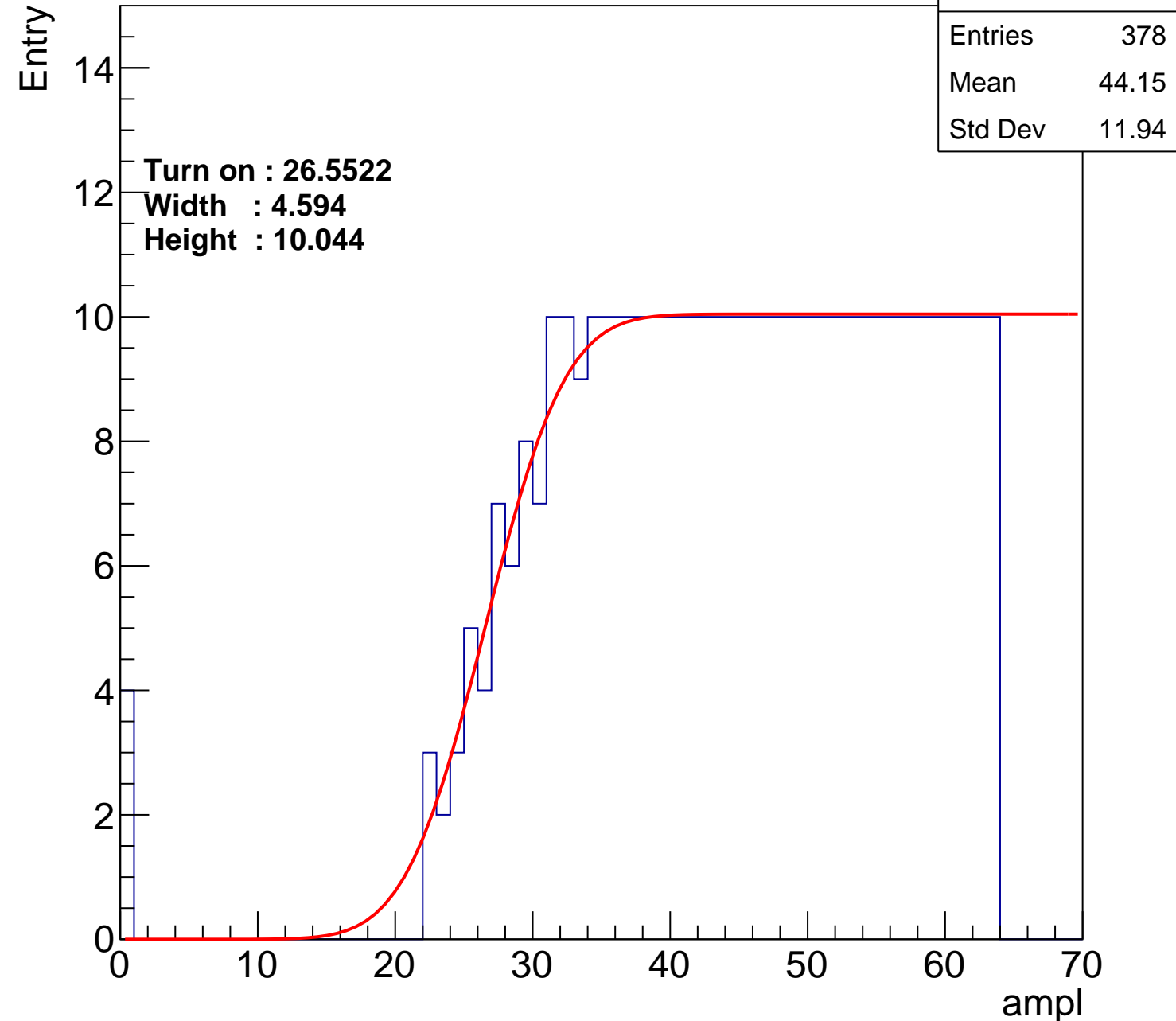
Width : 4.594

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch111

calib_packv5_042523_0143.root, FC#13, port D2

Entries	360
Mean	45.09
Std Dev	11.44

Turn on : 28.5503

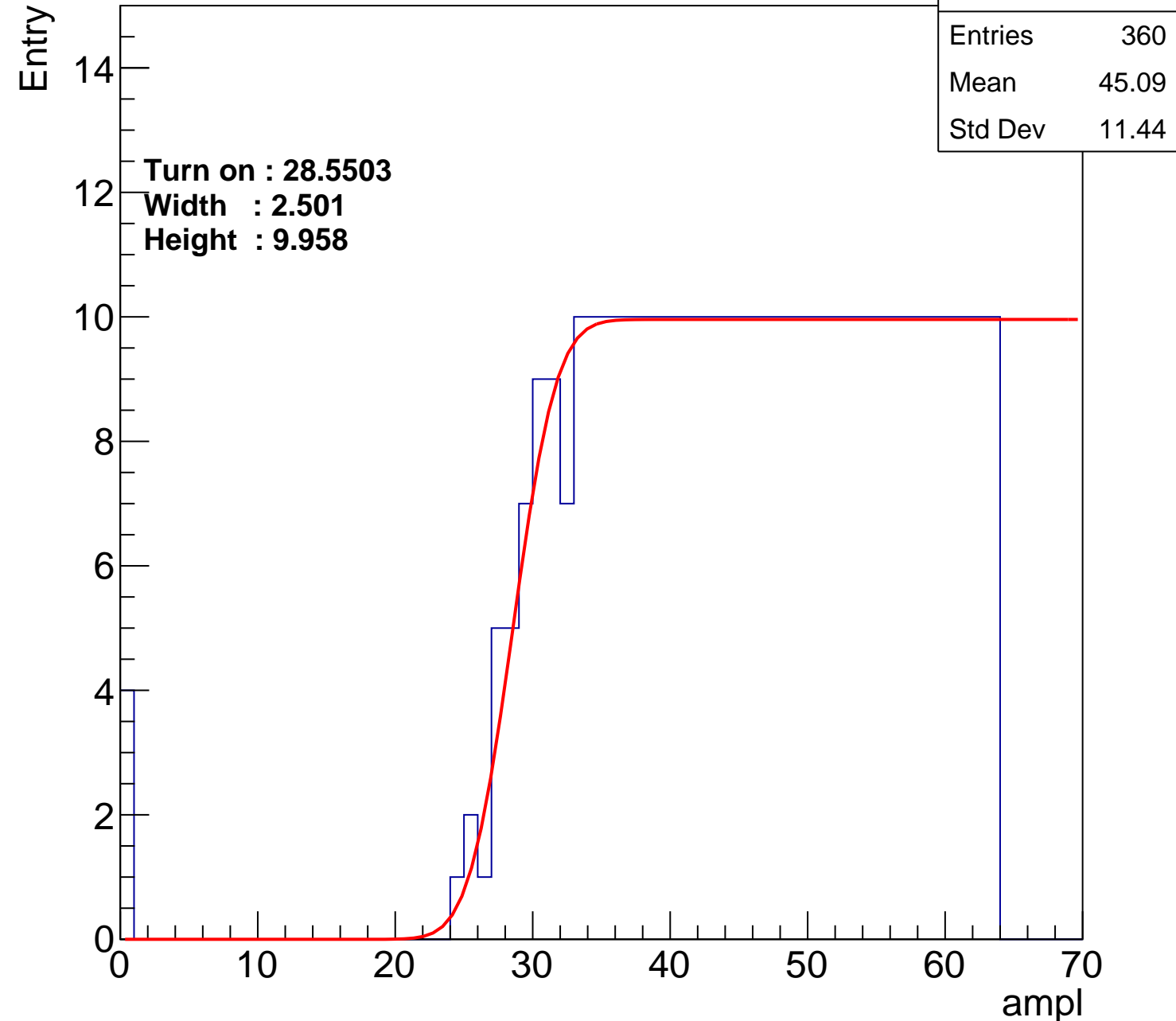
Width : 2.501

Height : 9.958

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch112

calib_packv5_042523_0143.root, FC#13, port D2

Entries	377
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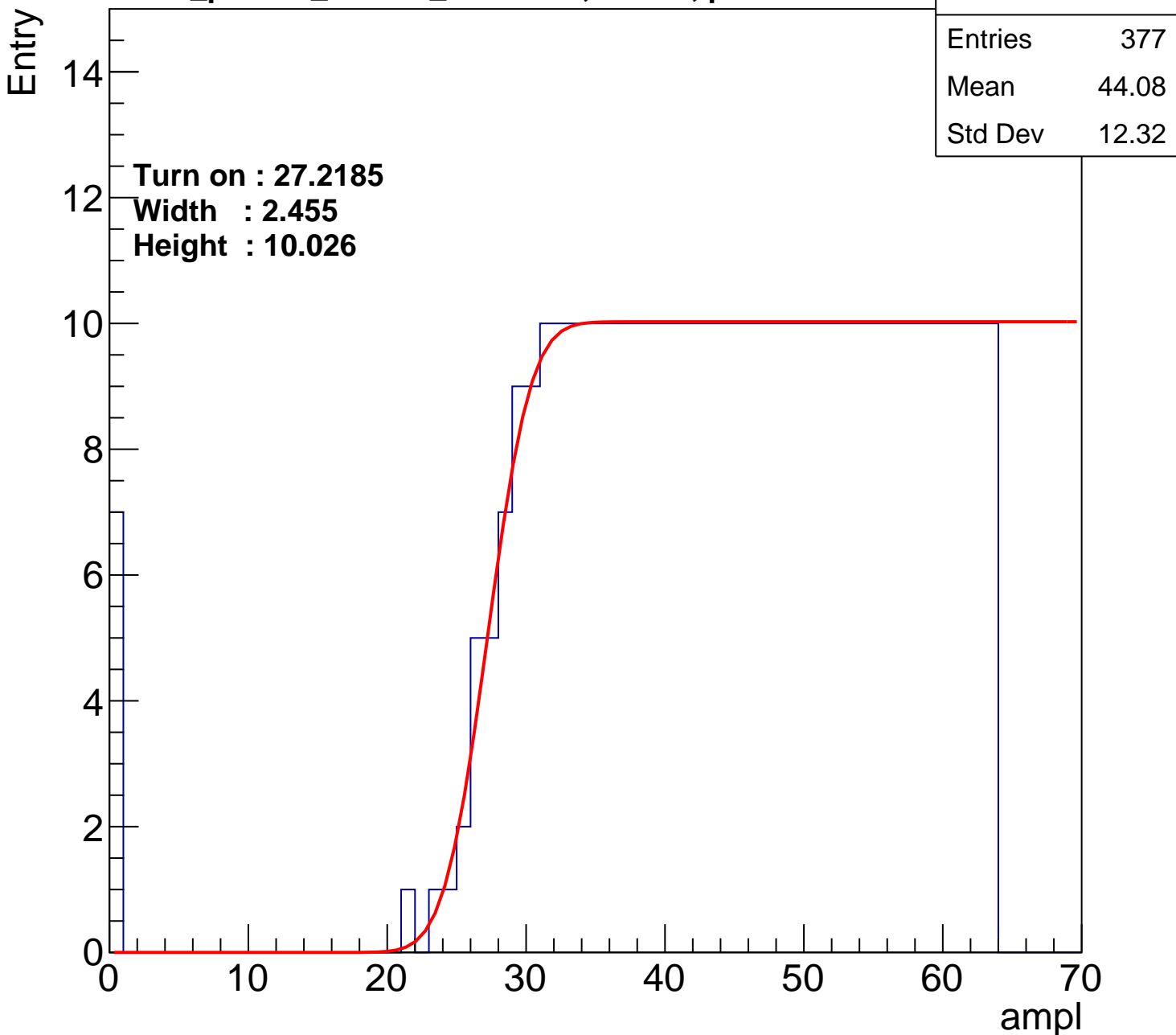
Mean	44.08
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Std Dev	12.32
---------	-------

Turn on : 27.2185

Width : 2.455

Height : 10.026



B1L003S, U1-ch113

calib_packv5_042523_0143.root, FC#13, port D2

Entries	368
Mean	44.86
Std Dev	11.19

Turn on : 27.6929

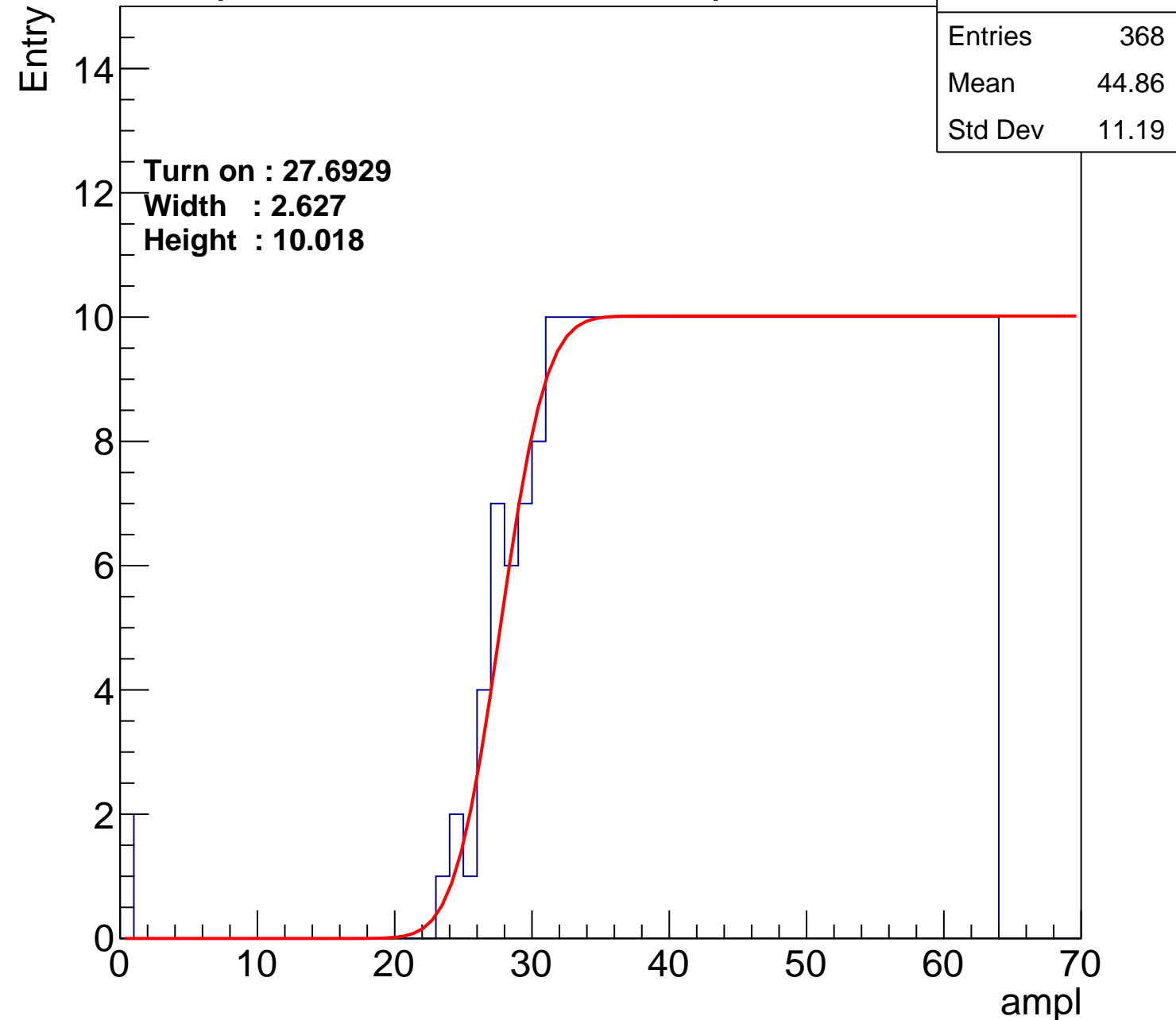
Width : 2.627

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch114

calib_packv5_042523_0143.root, FC#13, port D2

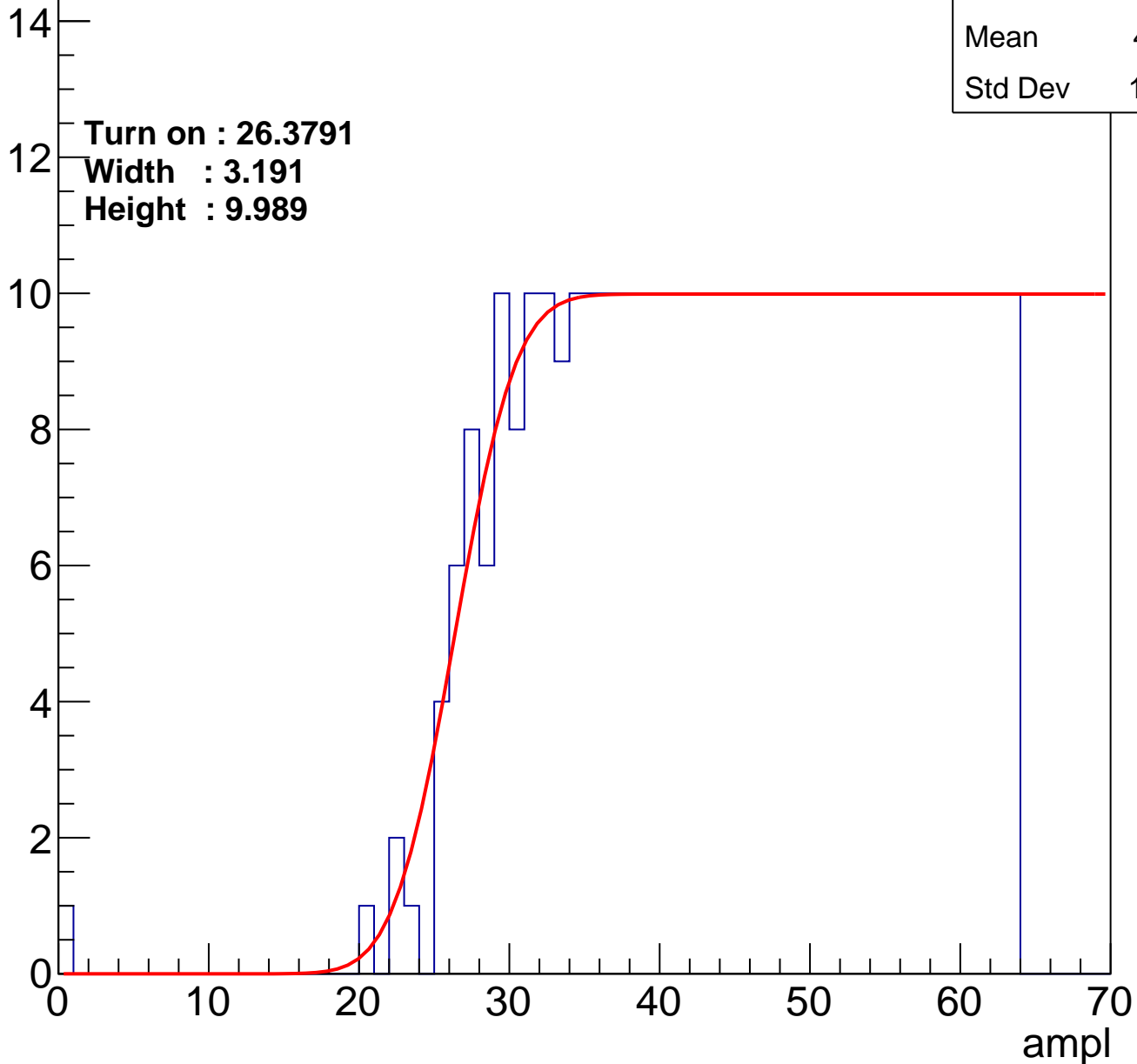
Entries	376
Mean	44.51
Std Dev	11.26

Turn on : 26.3791

Width : 3.191

Height : 9.989

Entry



B1L003S, U1-ch115

calib_packv5_042523_0143.root, FC#13, port D2

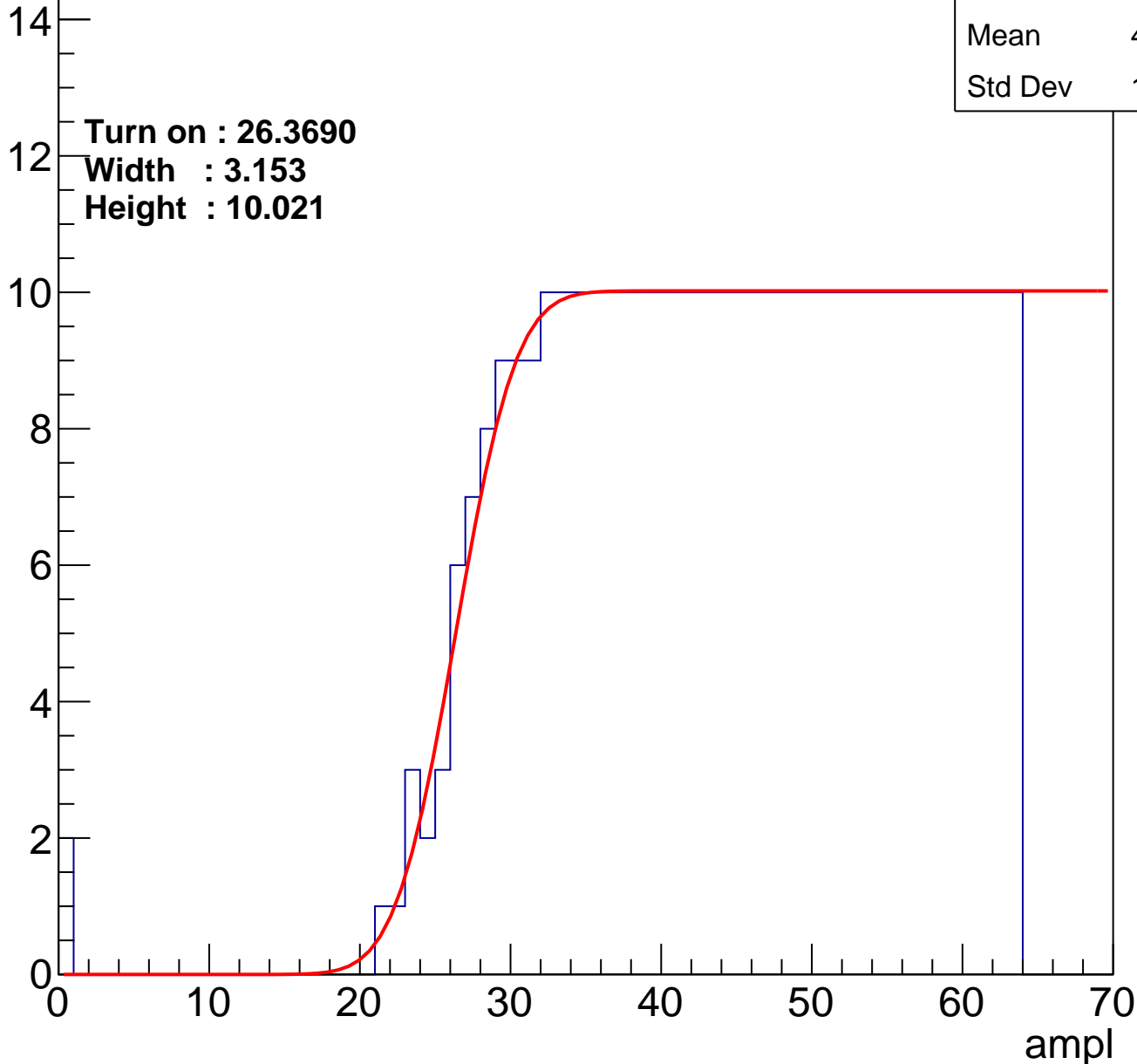
Entries	380
Mean	44.25
Std Dev	11.54

Turn on : 26.3690

Width : 3.153

Height : 10.021

Entry



B1L003S, U1-ch116

calib_packv5_042523_0143.root, FC#13, port D2

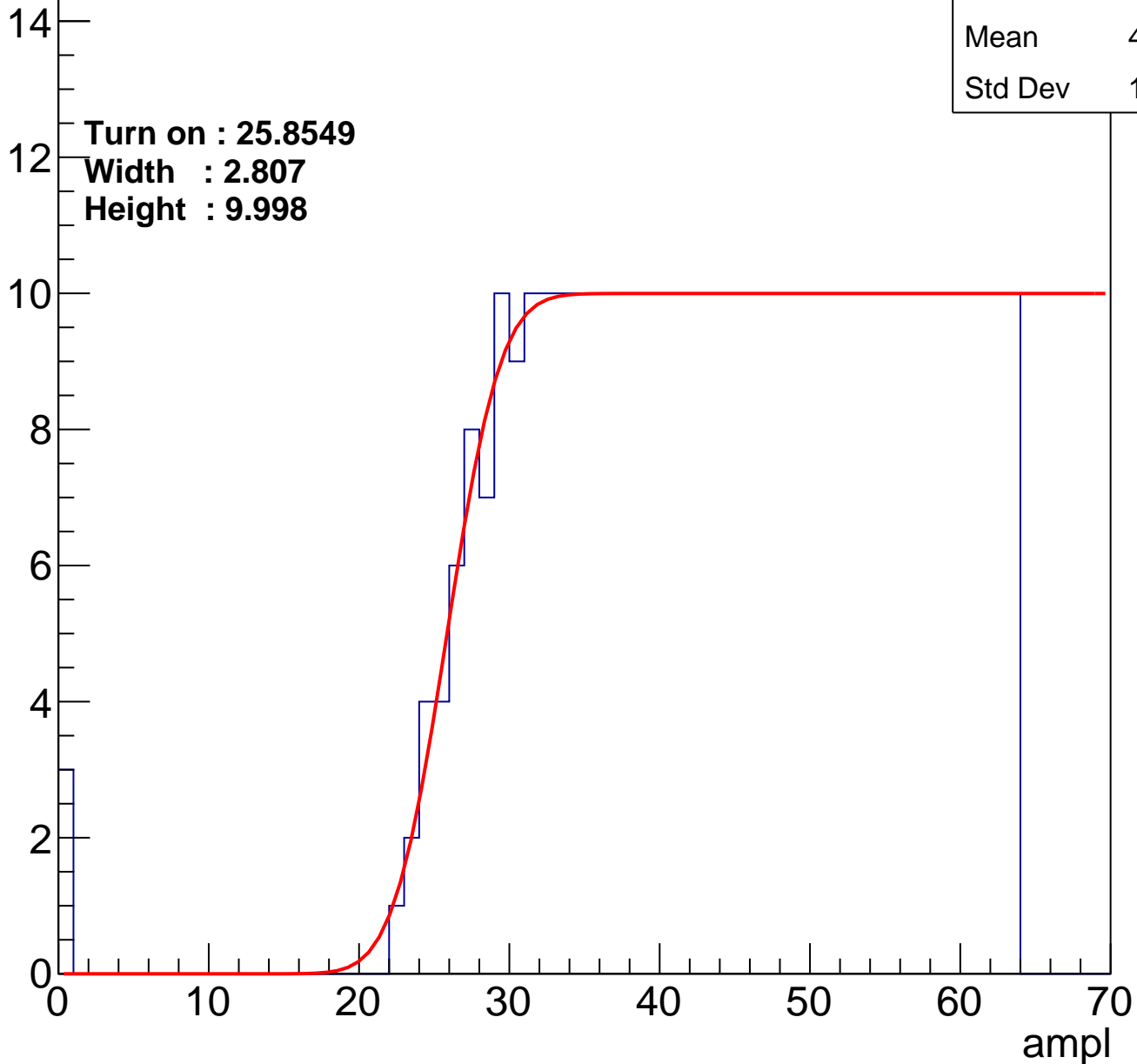
Entries	384
Mean	44.02
Std Dev	11.77

Turn on : 25.8549

Width : 2.807

Height : 9.998

Entry



B1L003S, U1-ch117

calib_packv5_042523_0143.root, FC#13, port D2

Entries	383
Mean	43.97
Std Dev	11.97

Turn on : 26.5600

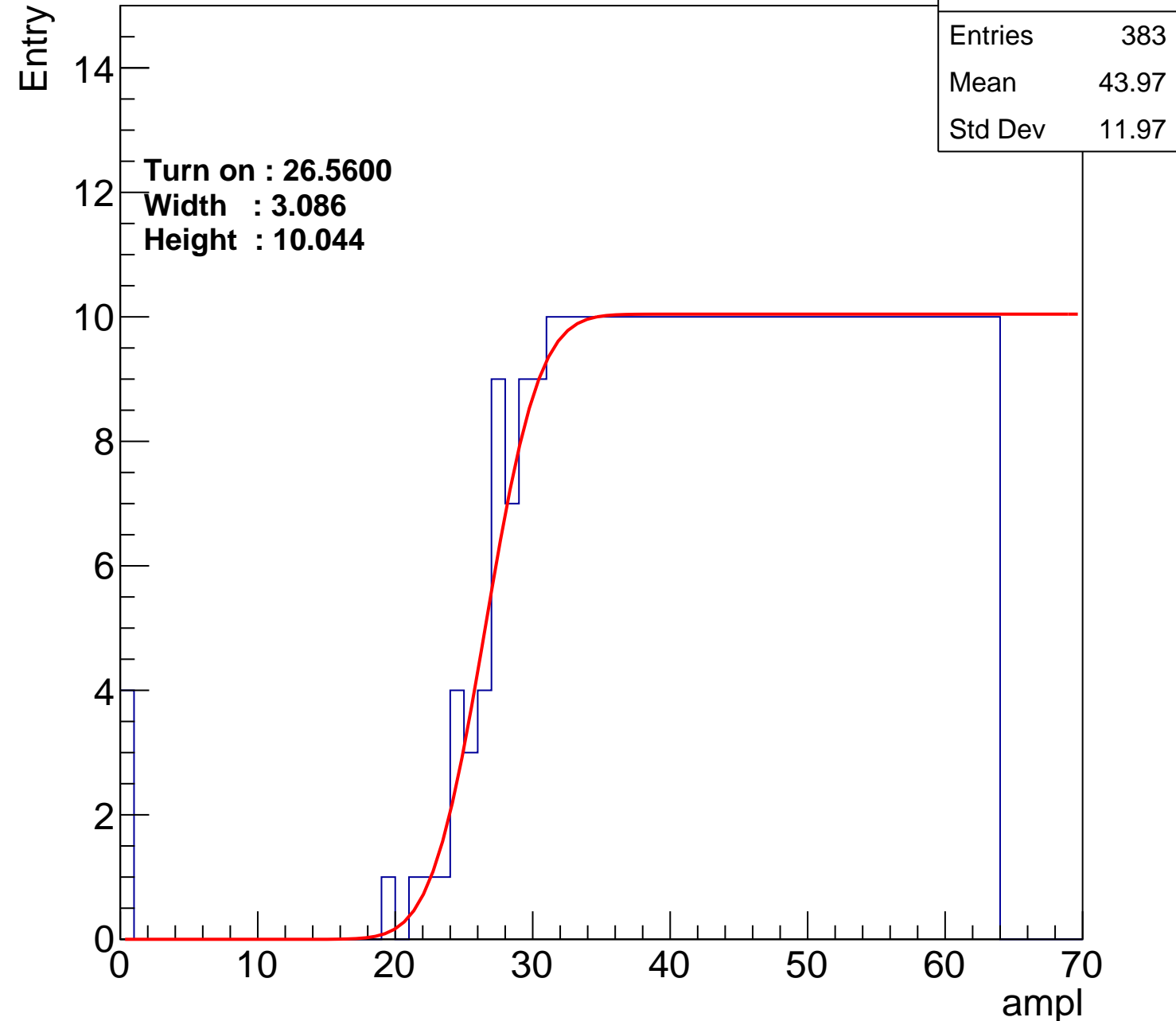
Width : 3.086

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch118

calib_packv5_042523_0143.root, FC#13, port D2

Entries	396
Mean	43.36
Std Dev	12.24

Turn on : 25.4839

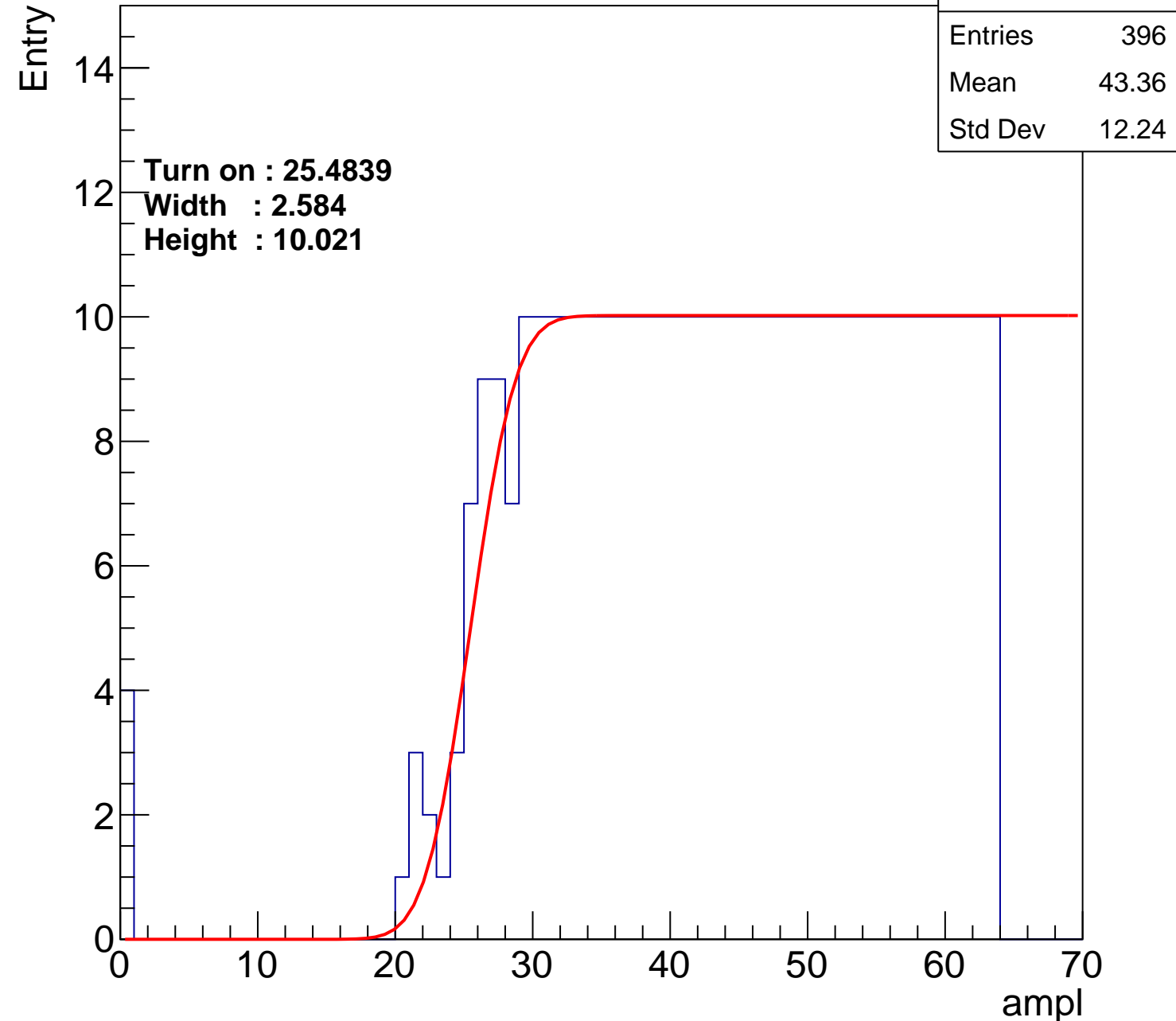
Width : 2.584

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



calib_packv5_042523_0143.root, FC#13, port D2

calib_packv5_042523_0143.root, FC#13, port D2

Turn on : 25.4339
Width : 2.679
Height : 9.971



B1L003S, U1-ch120

calib_packv5_042523_0143.root, FC#13, port D2

Entries	370
Mean	44.81
Std Dev	11.09

Turn on : 27.3050

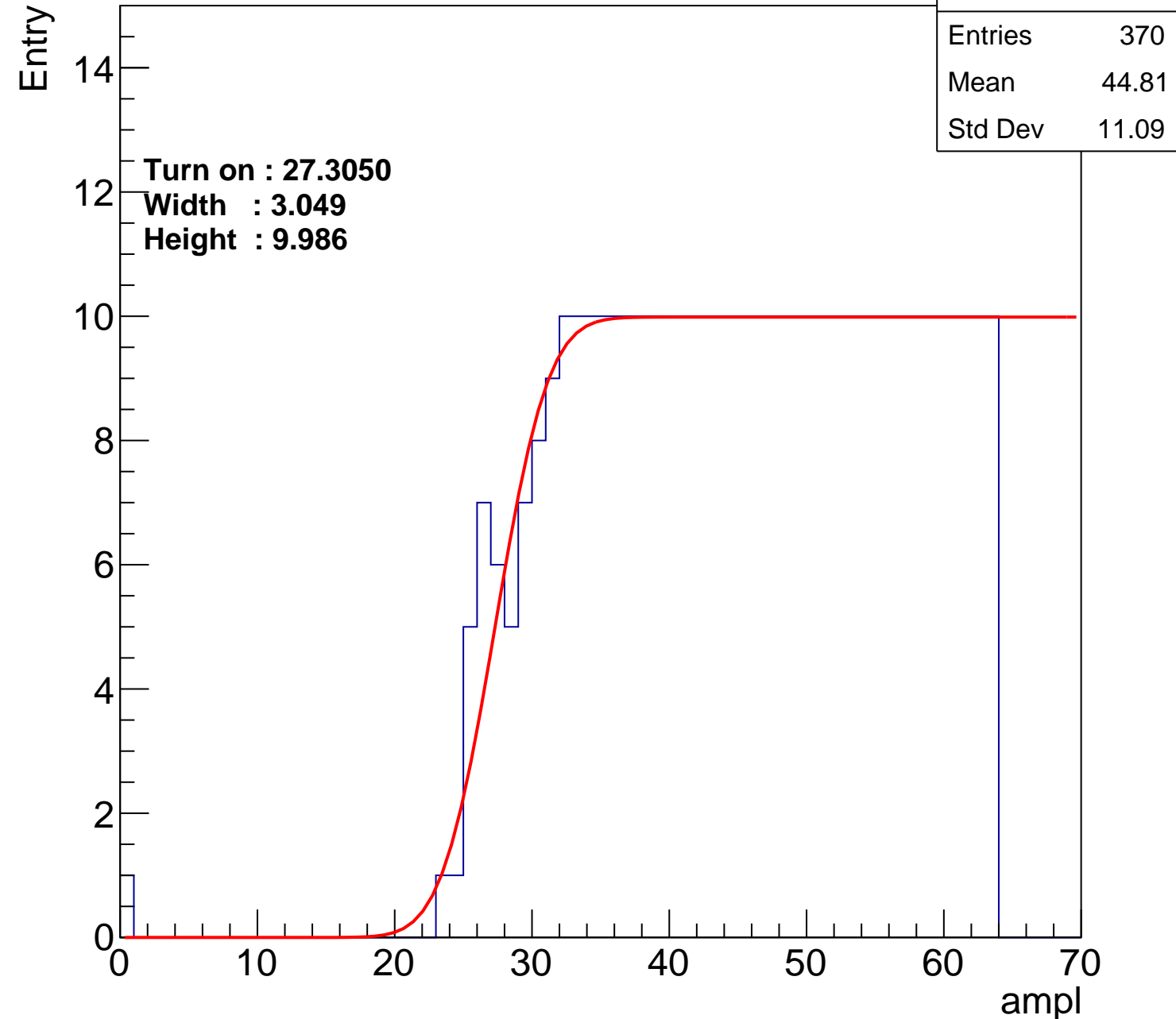
Width : 3.049

Height : 9.986

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch121

calib_packv5_042523_0143.root, FC#13, port D2

Entries	386
Mean	43.82
Std Dev	12.05

Turn on : 26.3596

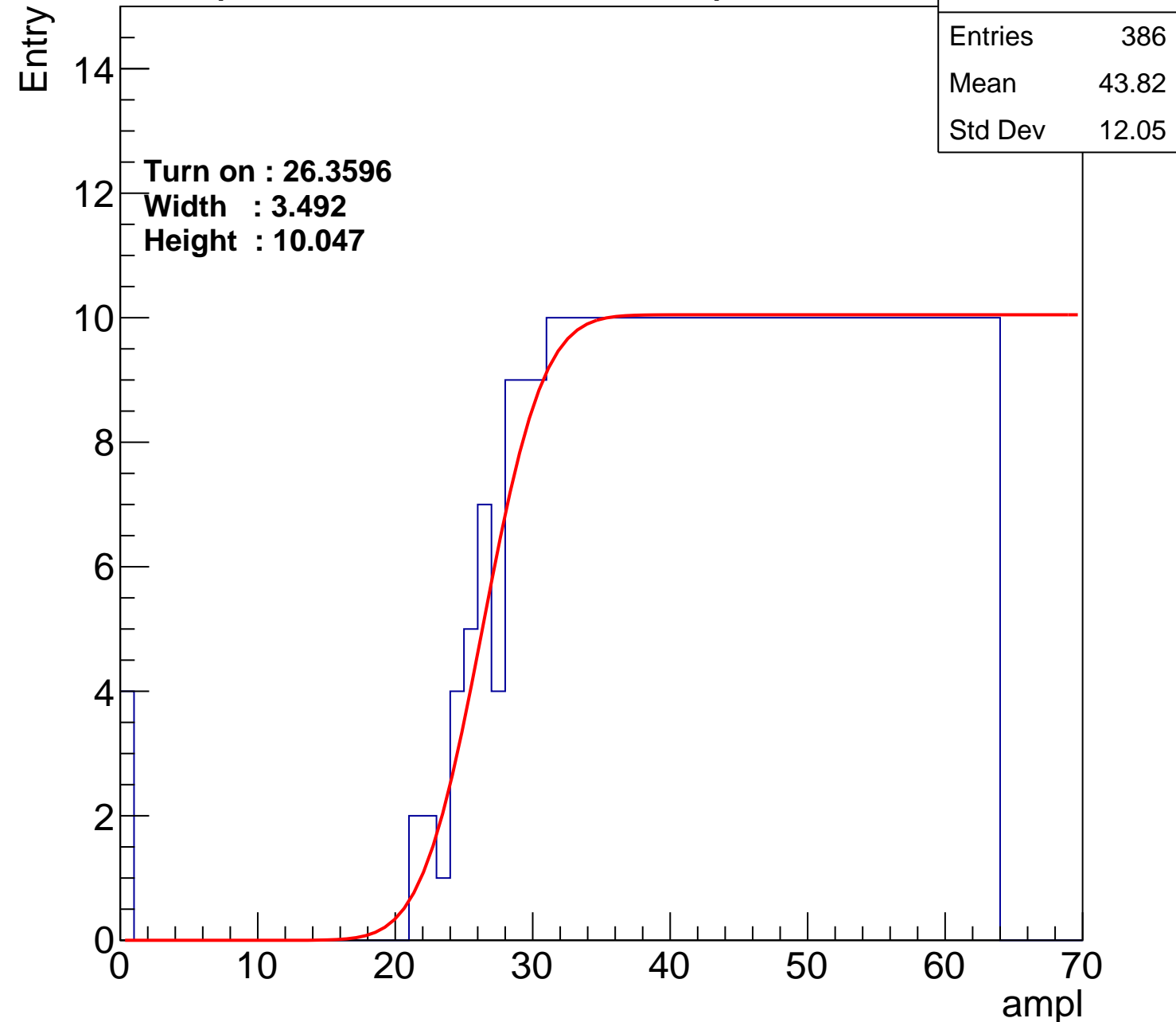
Width : 3.492

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch122

calib_packv5_042523_0143.root, FC#13, port D2

Entries	375
Mean	44.47
Std Dev	11.45

Turn on : 27.6269

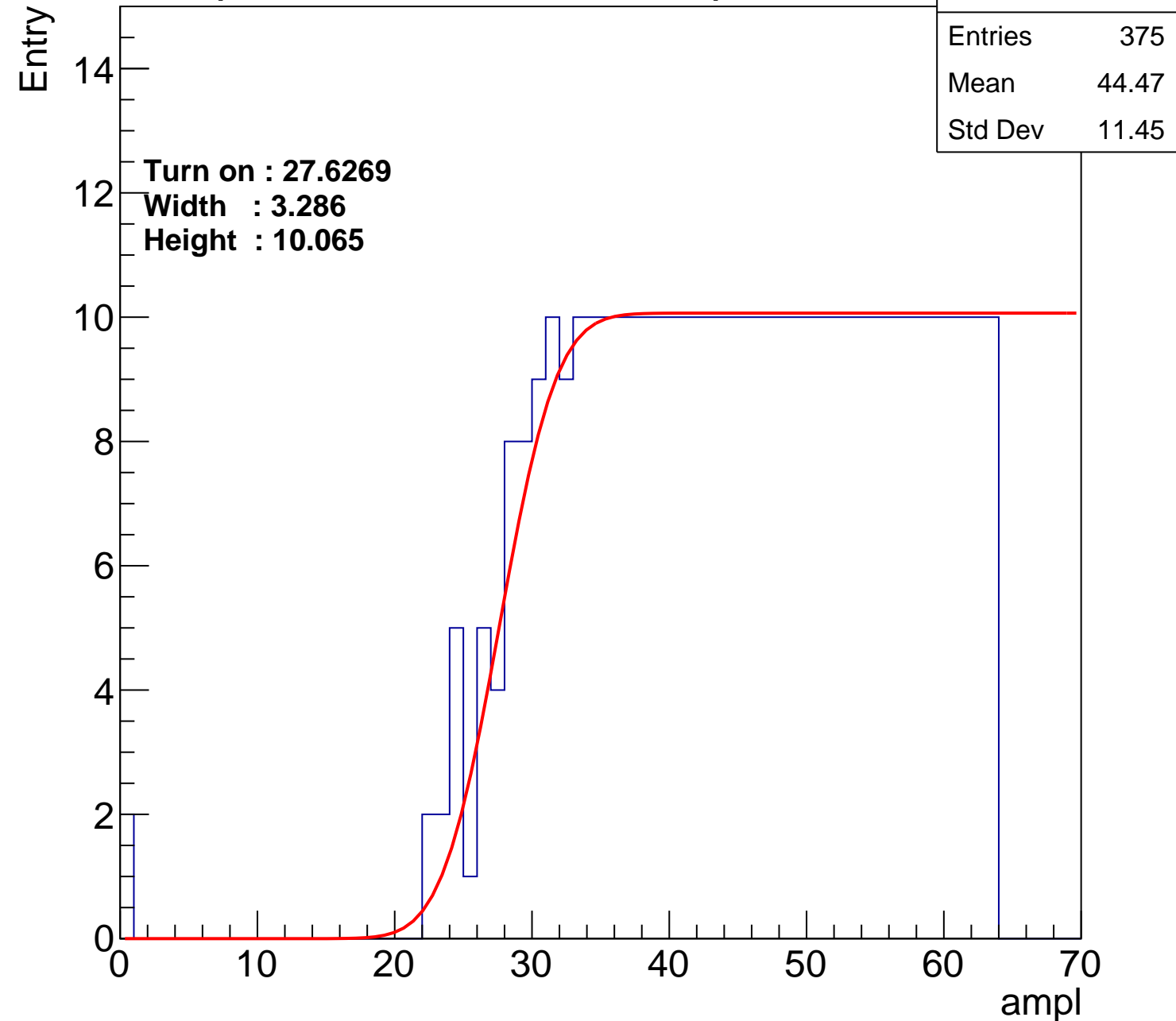
Width : 3.286

Height : 10.065

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch123

calib_packv5_042523_0143.root, FC#13, port D2

Entries	378
Mean	44.14
Std Dev	12.03

Turn on : 26.5998

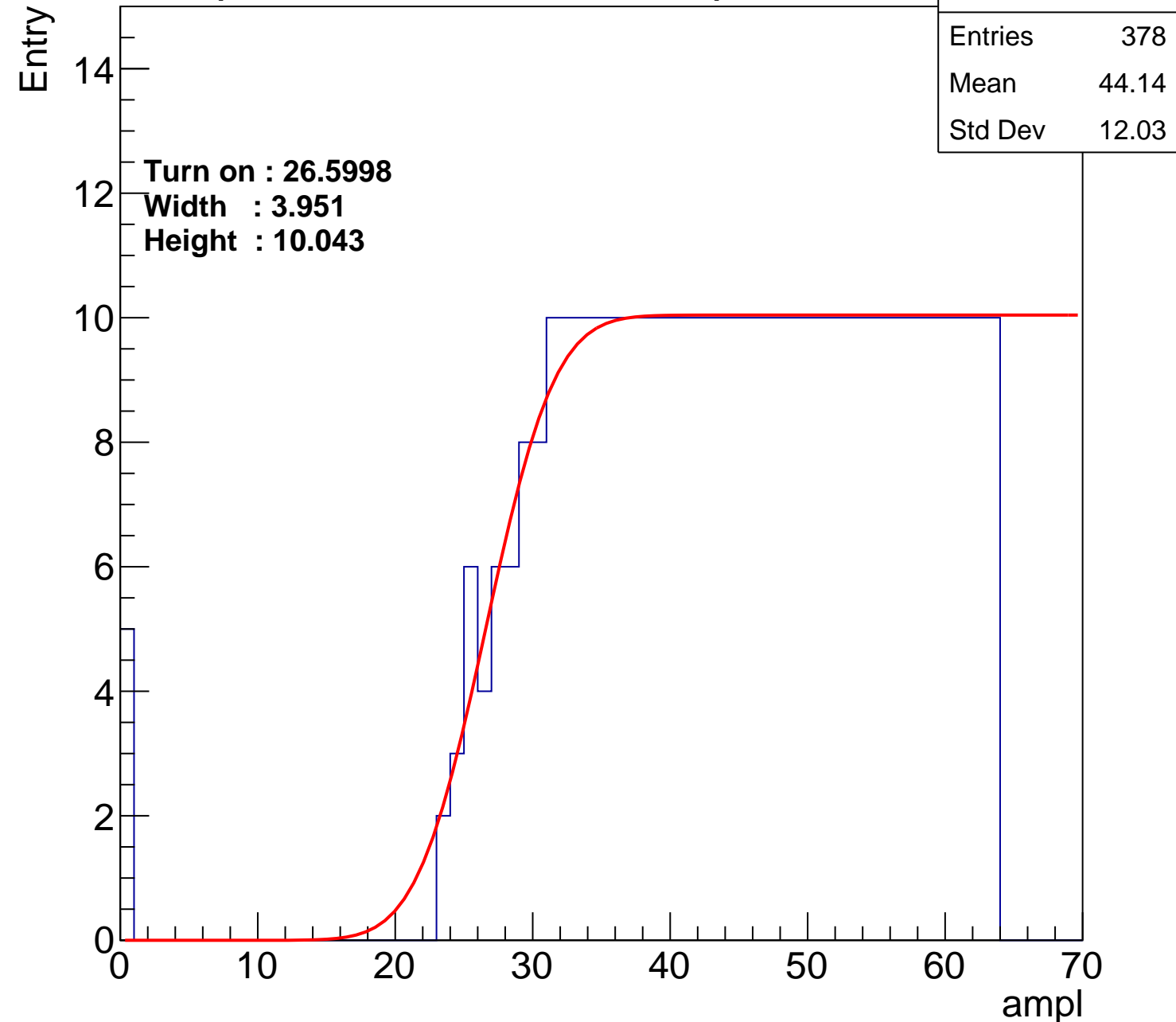
Width : 3.951

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch124

calib_packv5_042523_0143.root, FC#13, port D2

Entries	374
Mean	44.49
Std Dev	11.55

Turn on : 26.9241

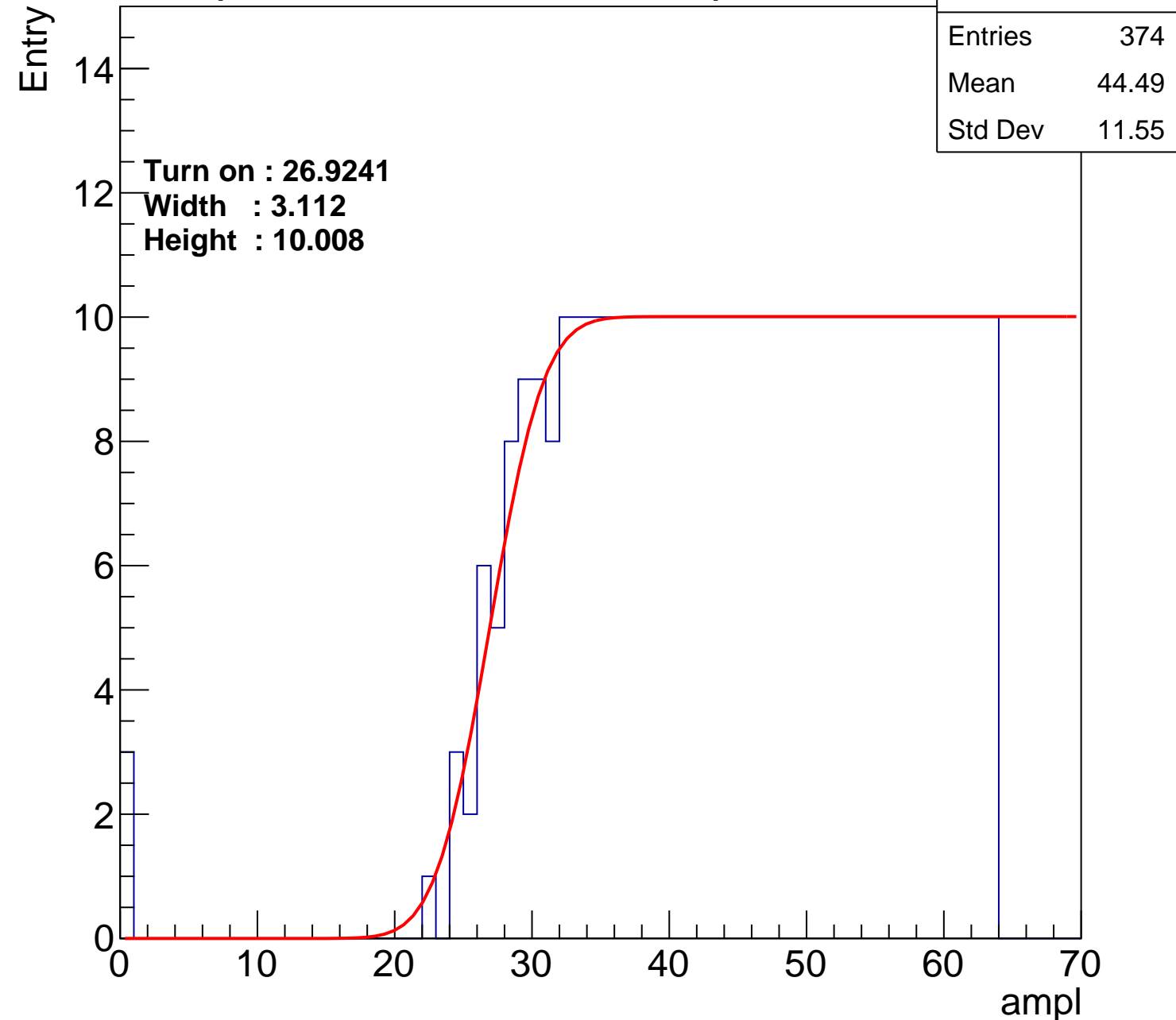
Width : 3.112

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch125

calib_packv5_042523_0143.root, FC#13, port D2

Entries	385
Mean	43.84
Std Dev	12.13

Turn on : 25.9973

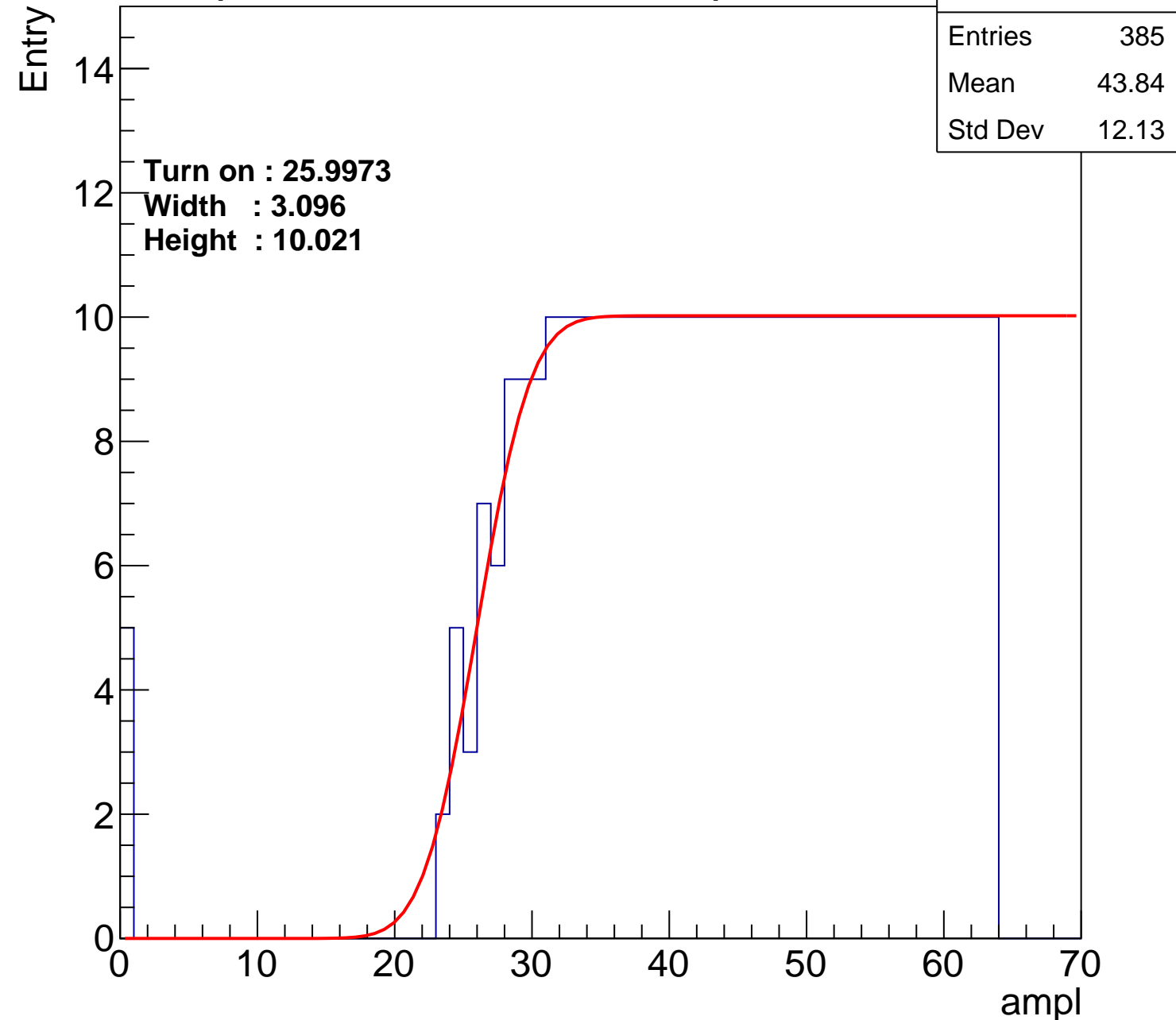
Width : 3.096

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch126

calib_packv5_042523_0143.root, FC#13, port D2

Entries	368
Mean	44.71
Std Dev	11.6

Turn on : 27.6203

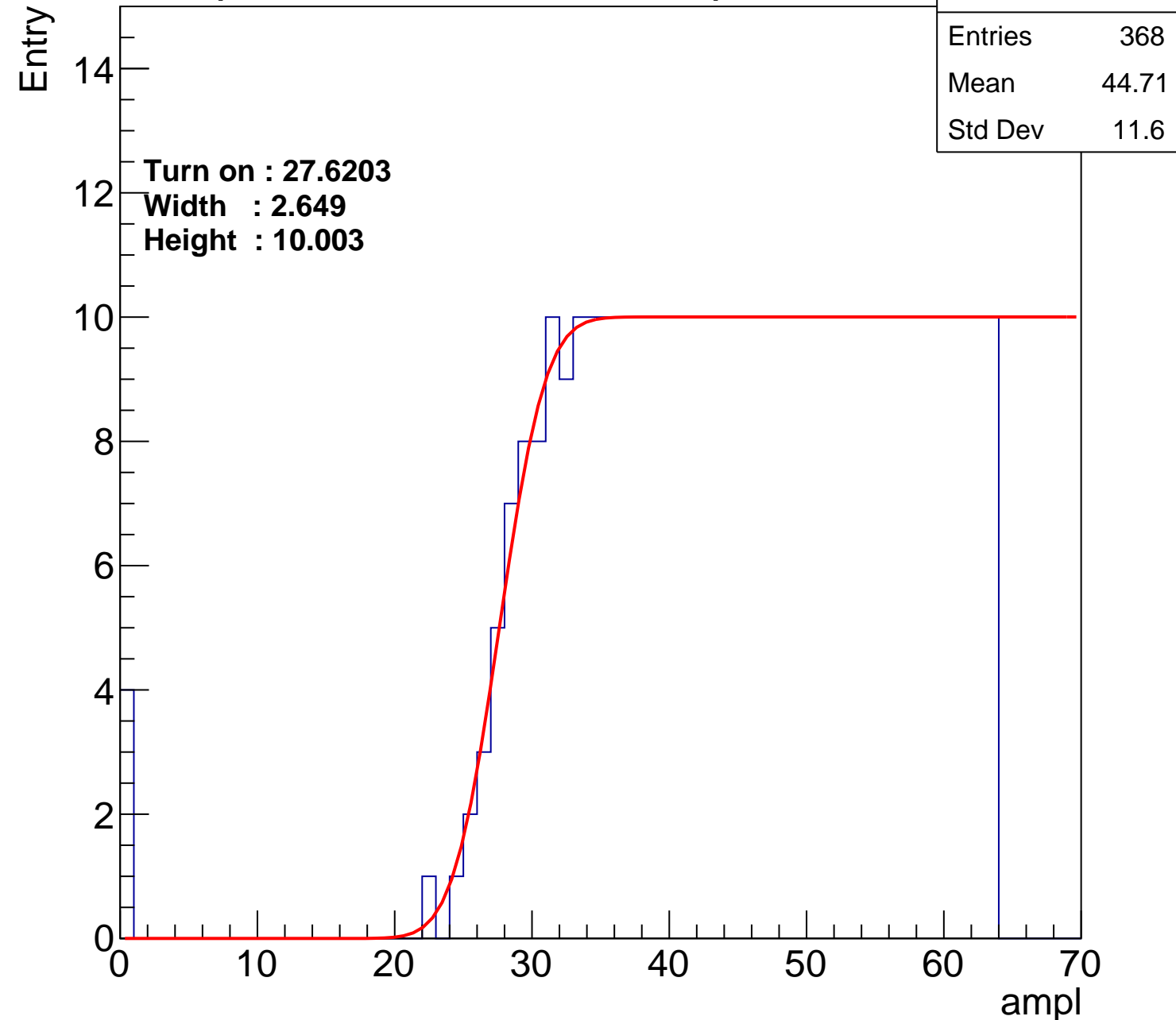
Width : 2.649

Height : 10.003

Entry

14
12
10
8
6
4
2
0

ampl



B1L003S, U1-ch127

calib_packv5_042523_0143.root, FC#13, port D2

Entries	370
Mean	44.73
Std Dev	11.3

Turn on : 26.8836

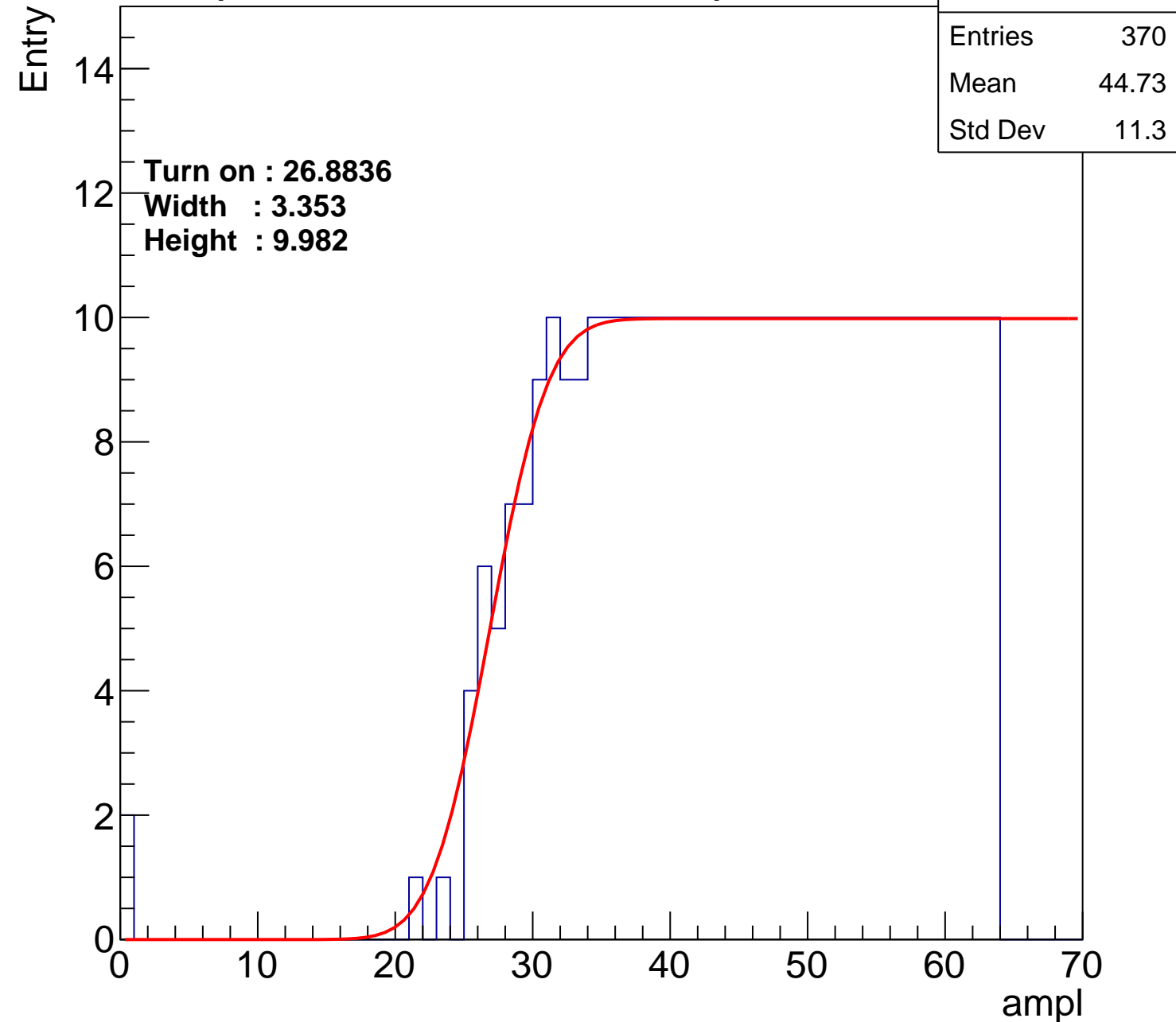
Width : 3.353

Height : 9.982

Entry

14
12
10
8
6
4
2
0

ampl



calib_packv5_042523_0143.root, FC#13, port D2

Entries	370
Mean	44.73
Std Dev	11.3

Height : 9.982

