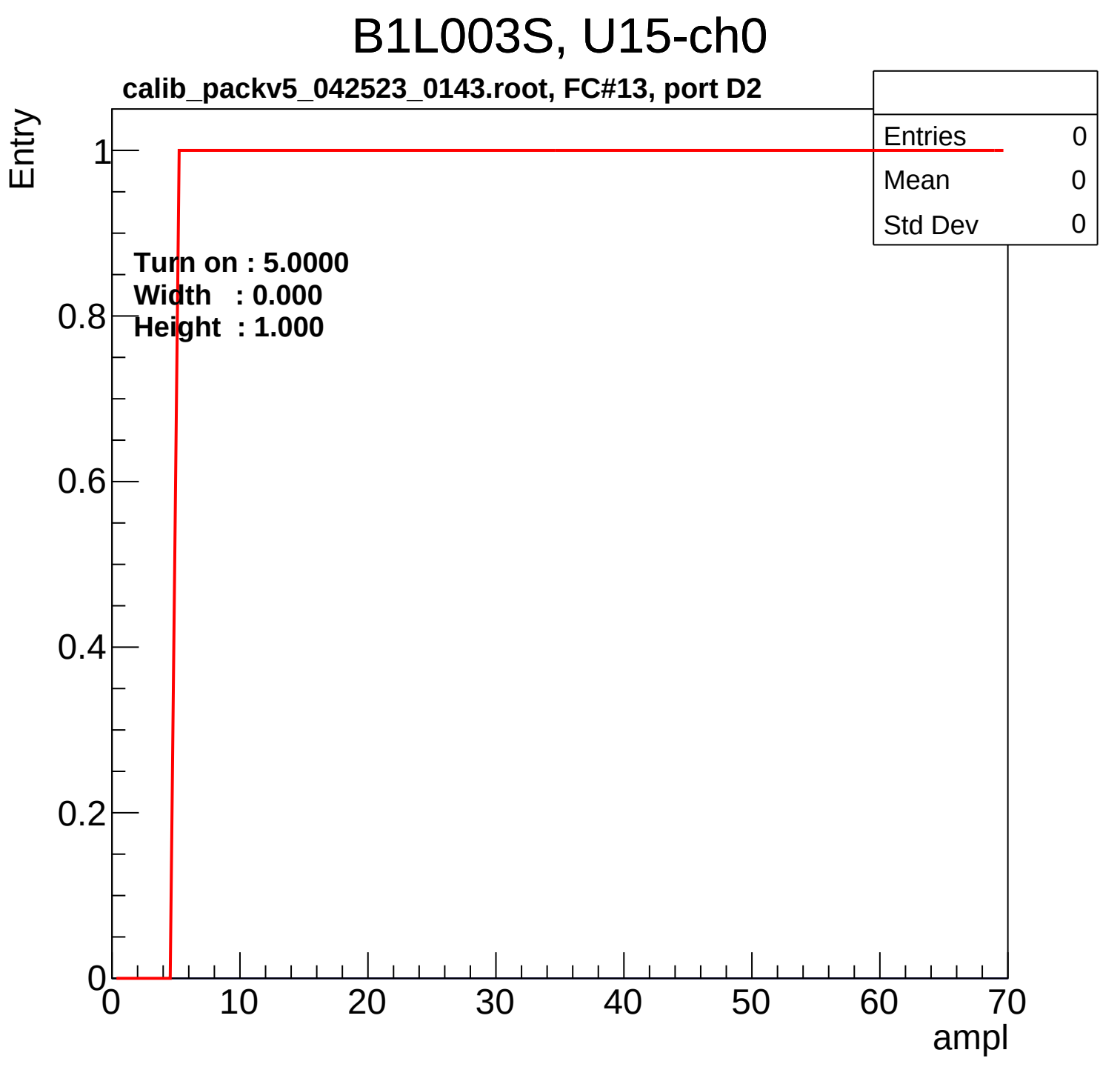
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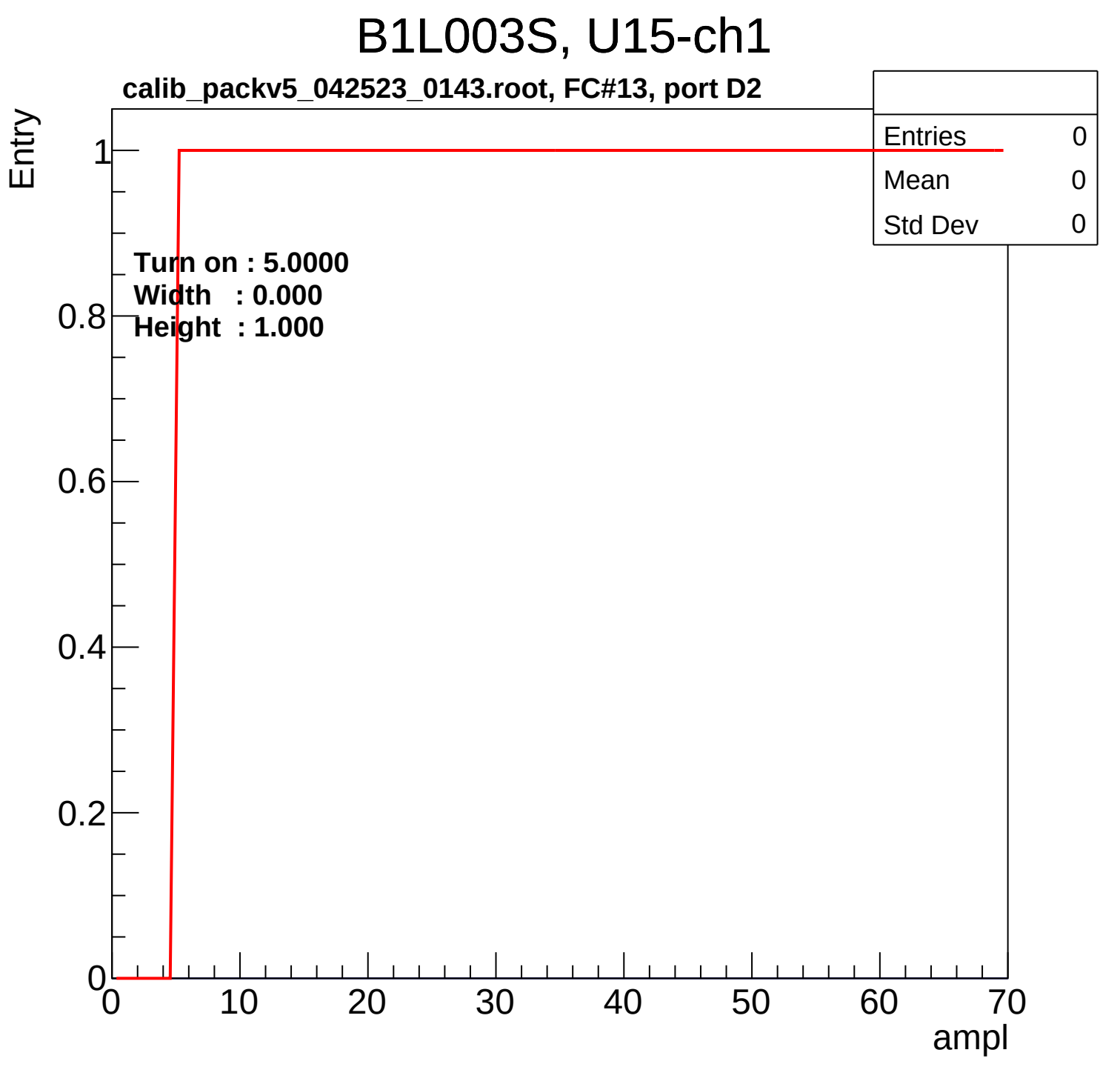
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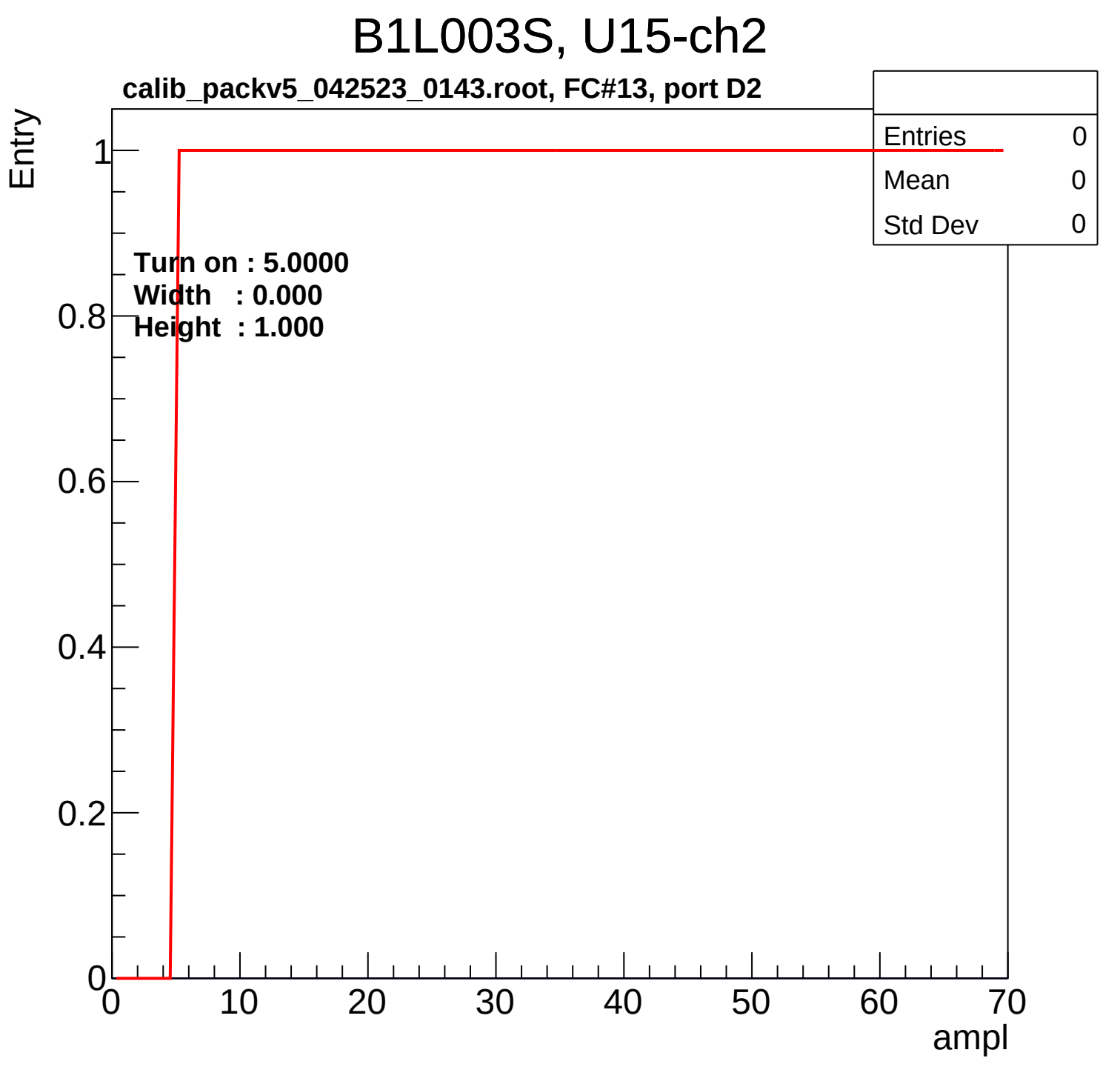
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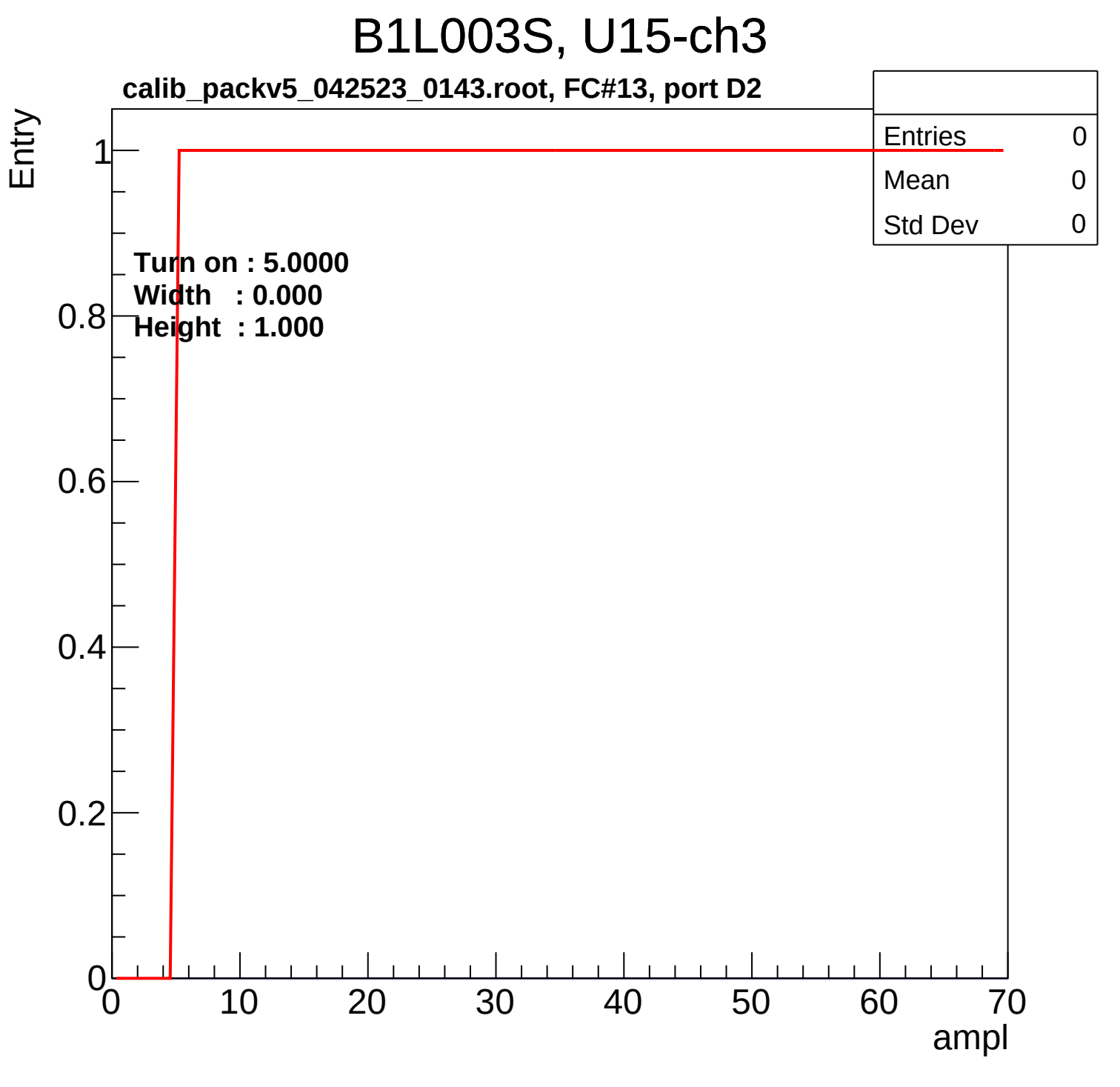
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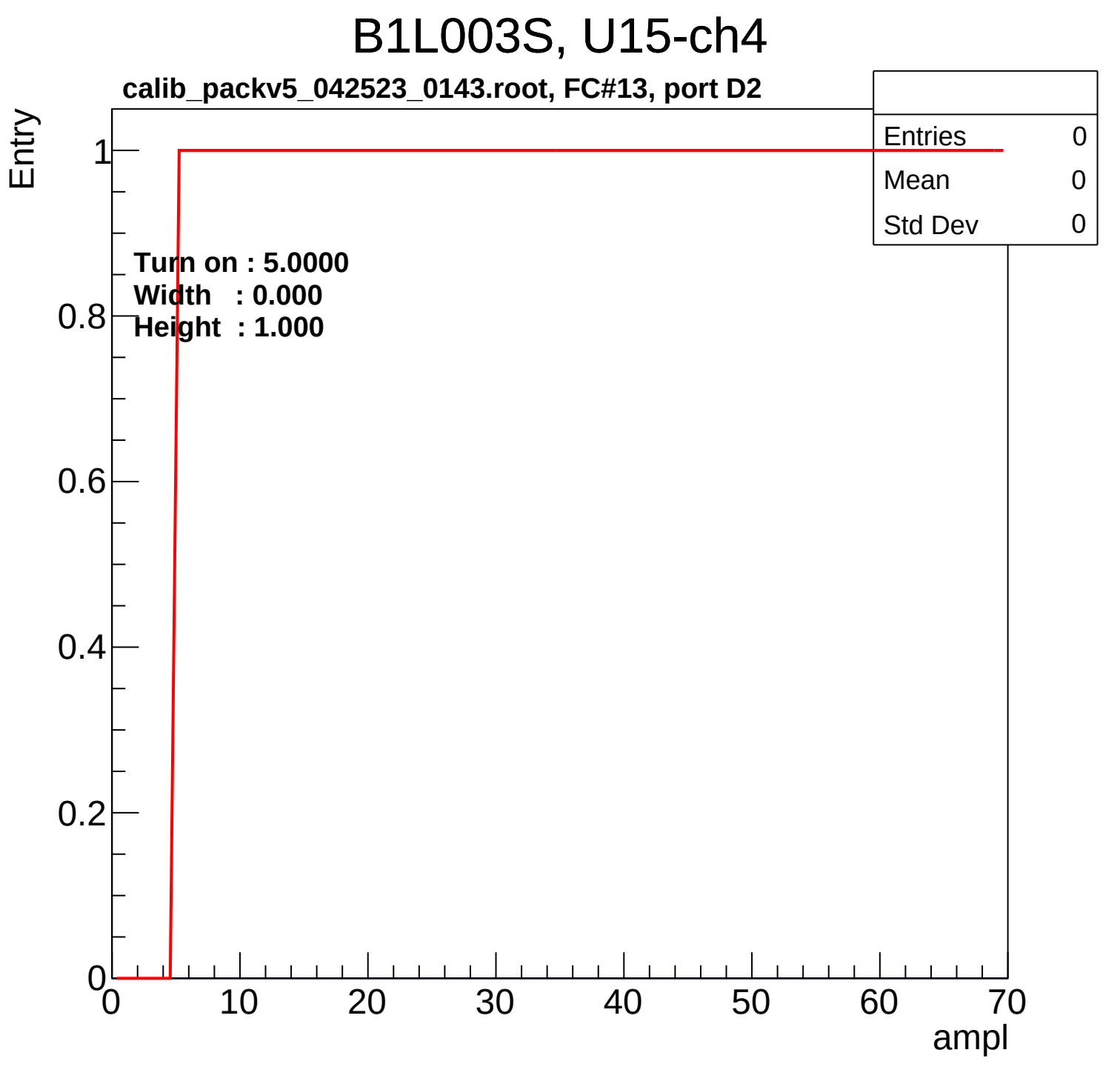
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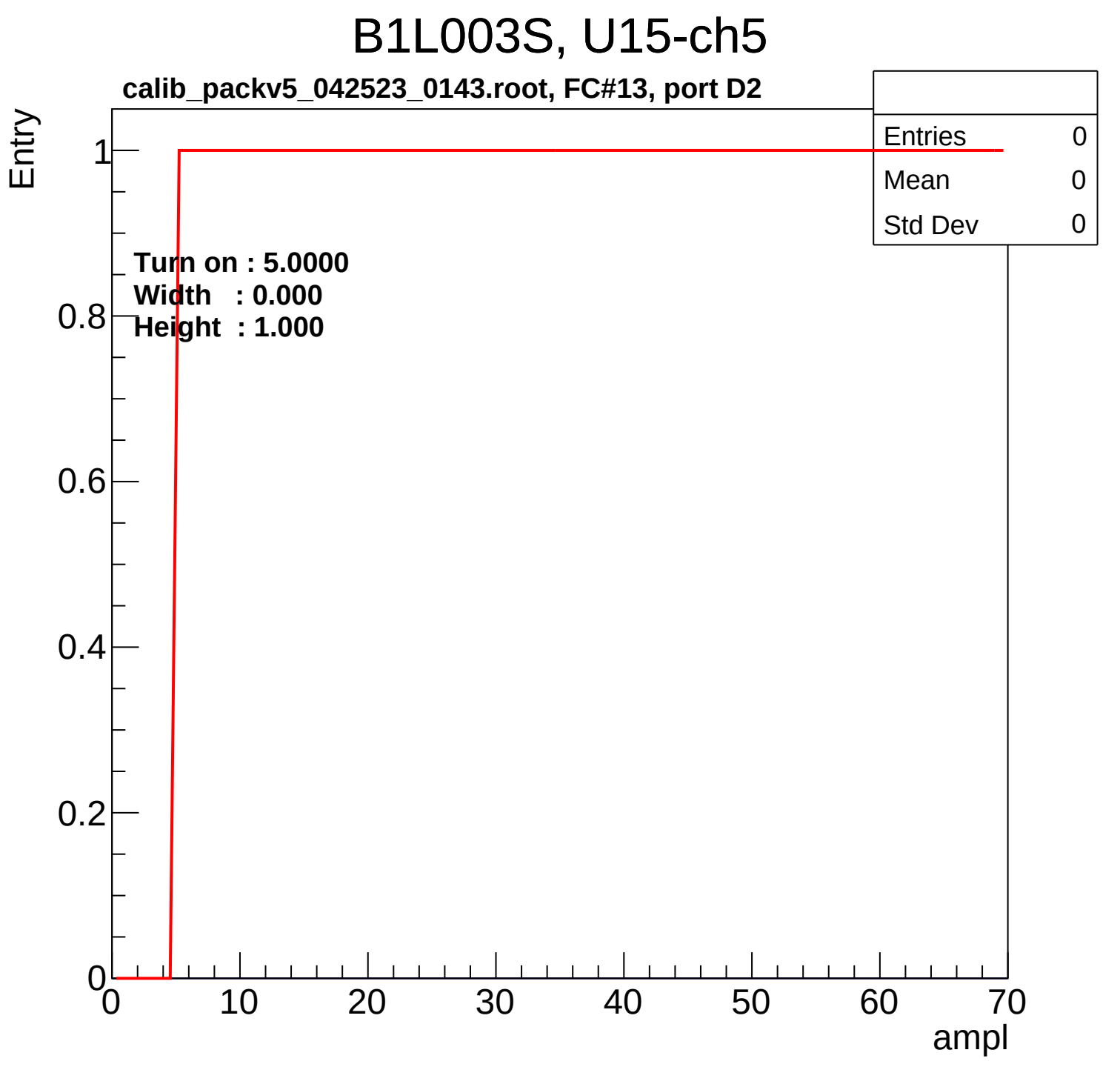
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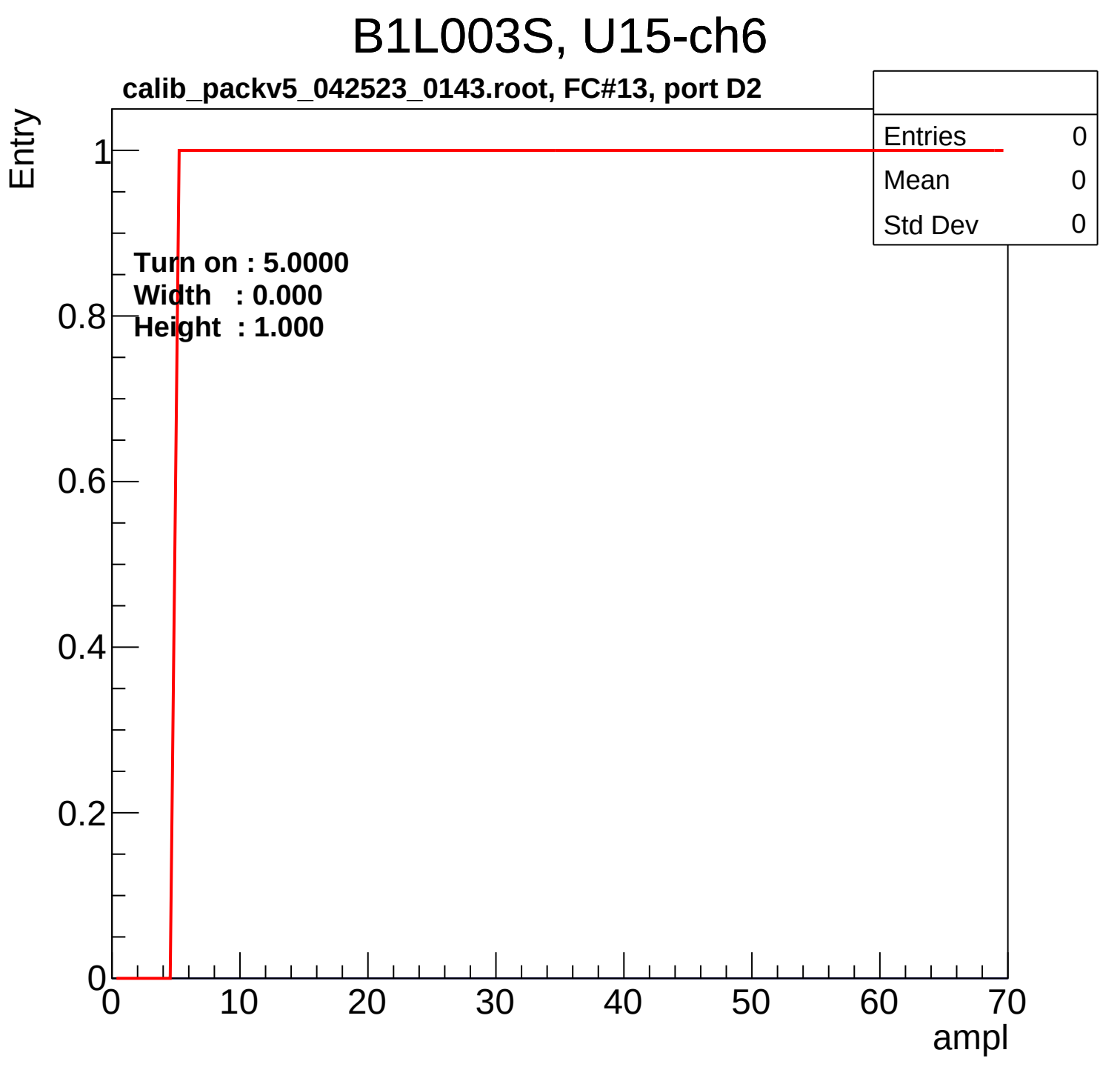
B1L003S, U15-ch6
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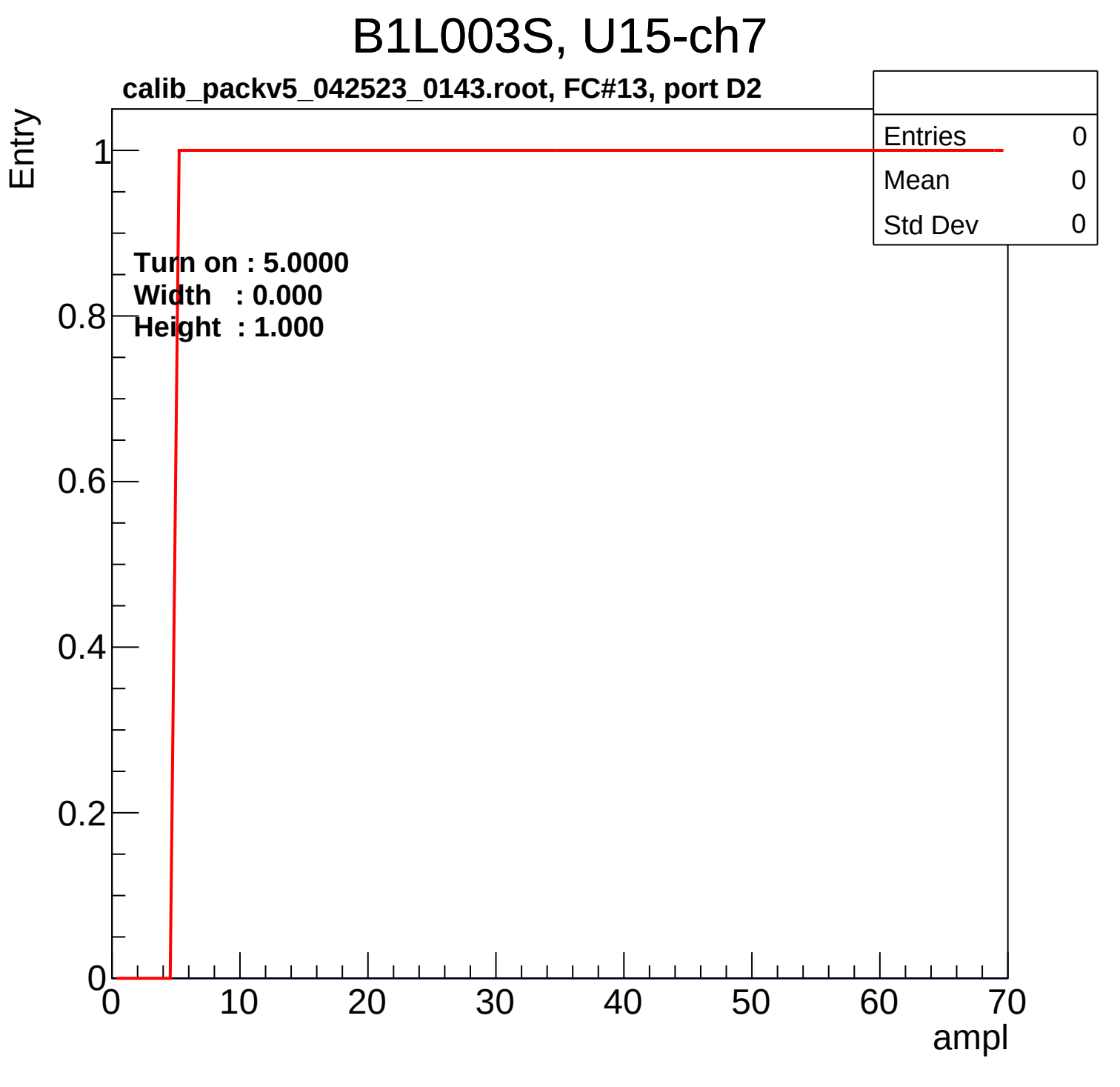
B1L003S, U15-ch7
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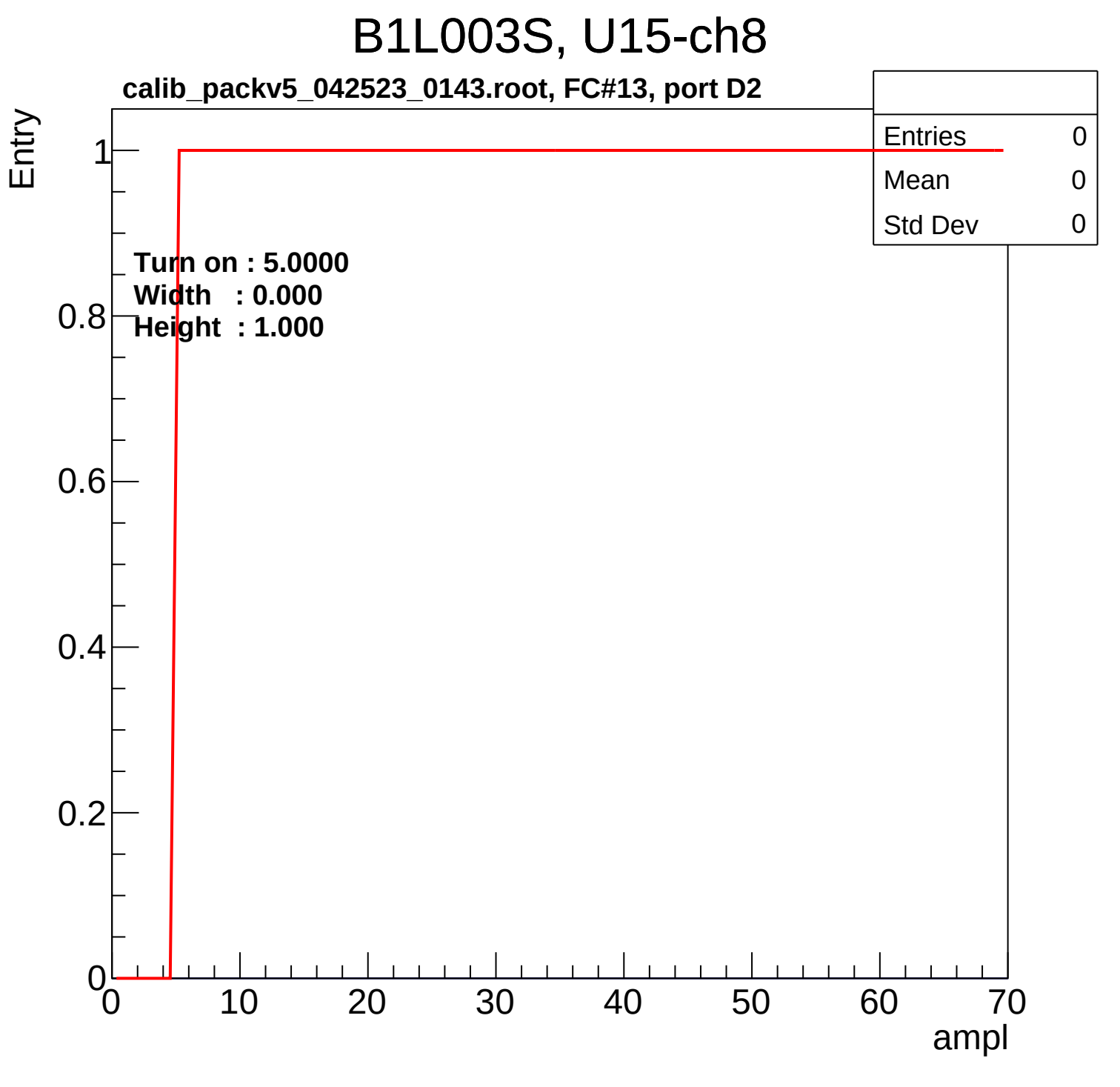
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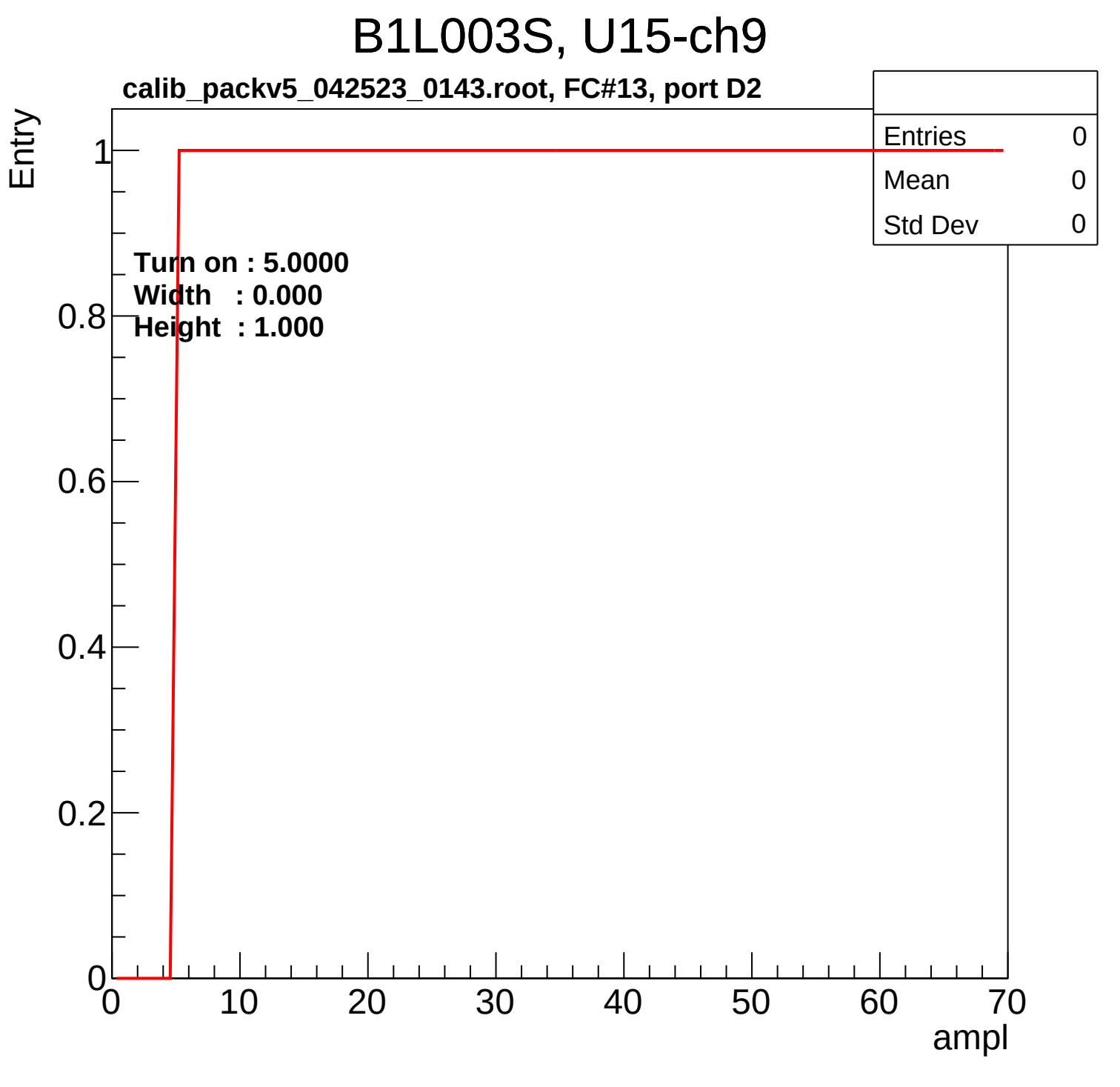
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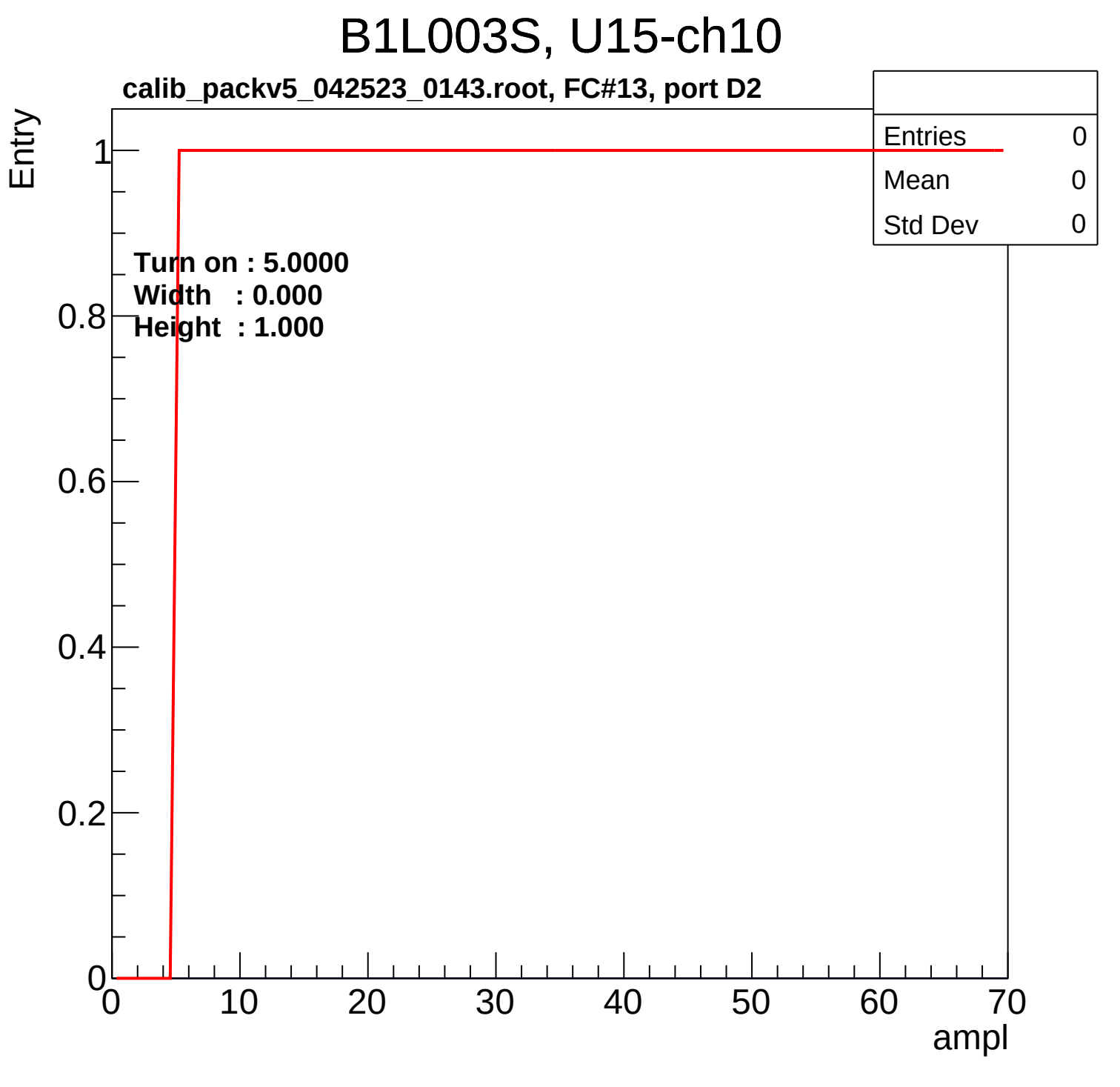
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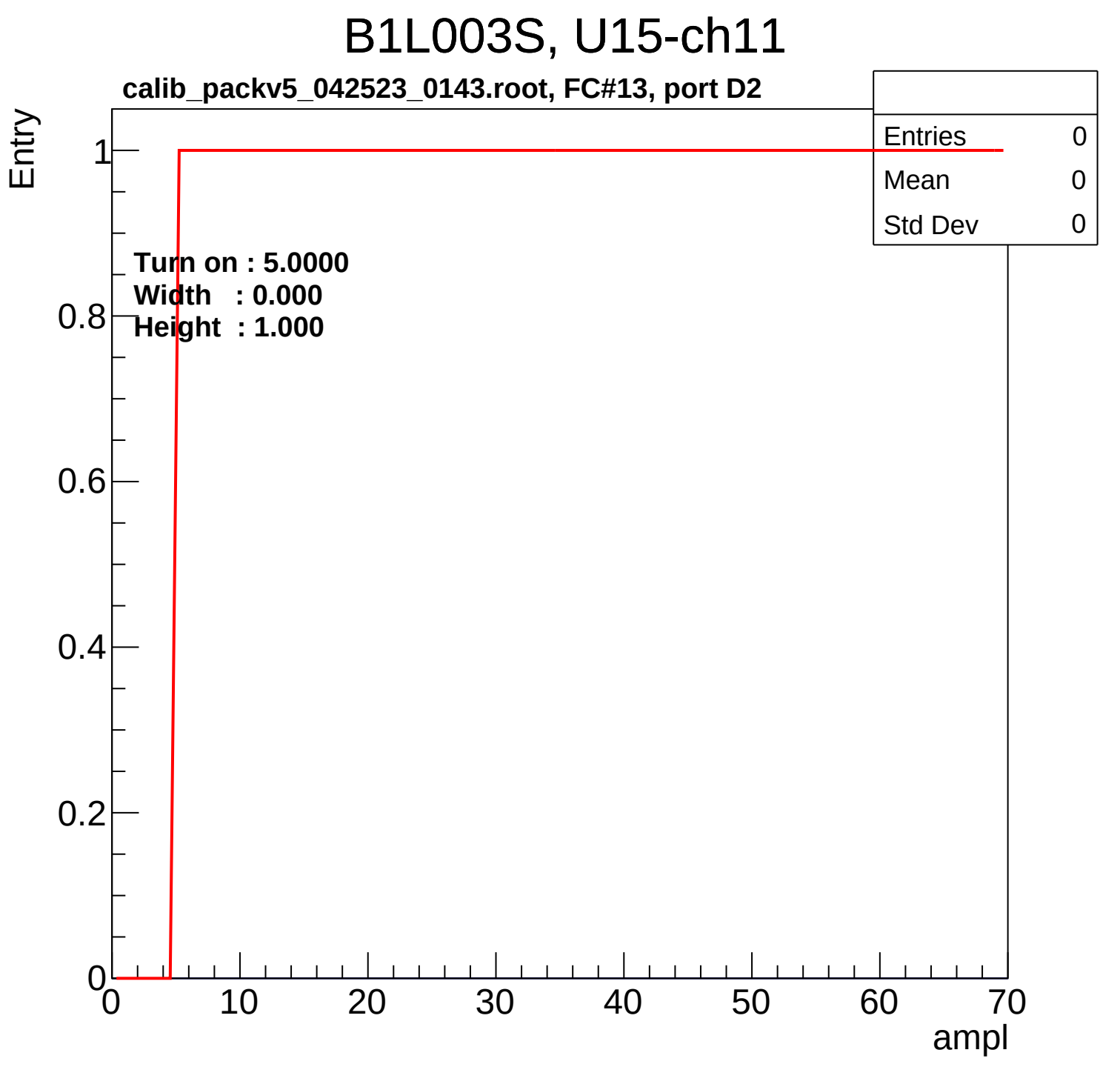
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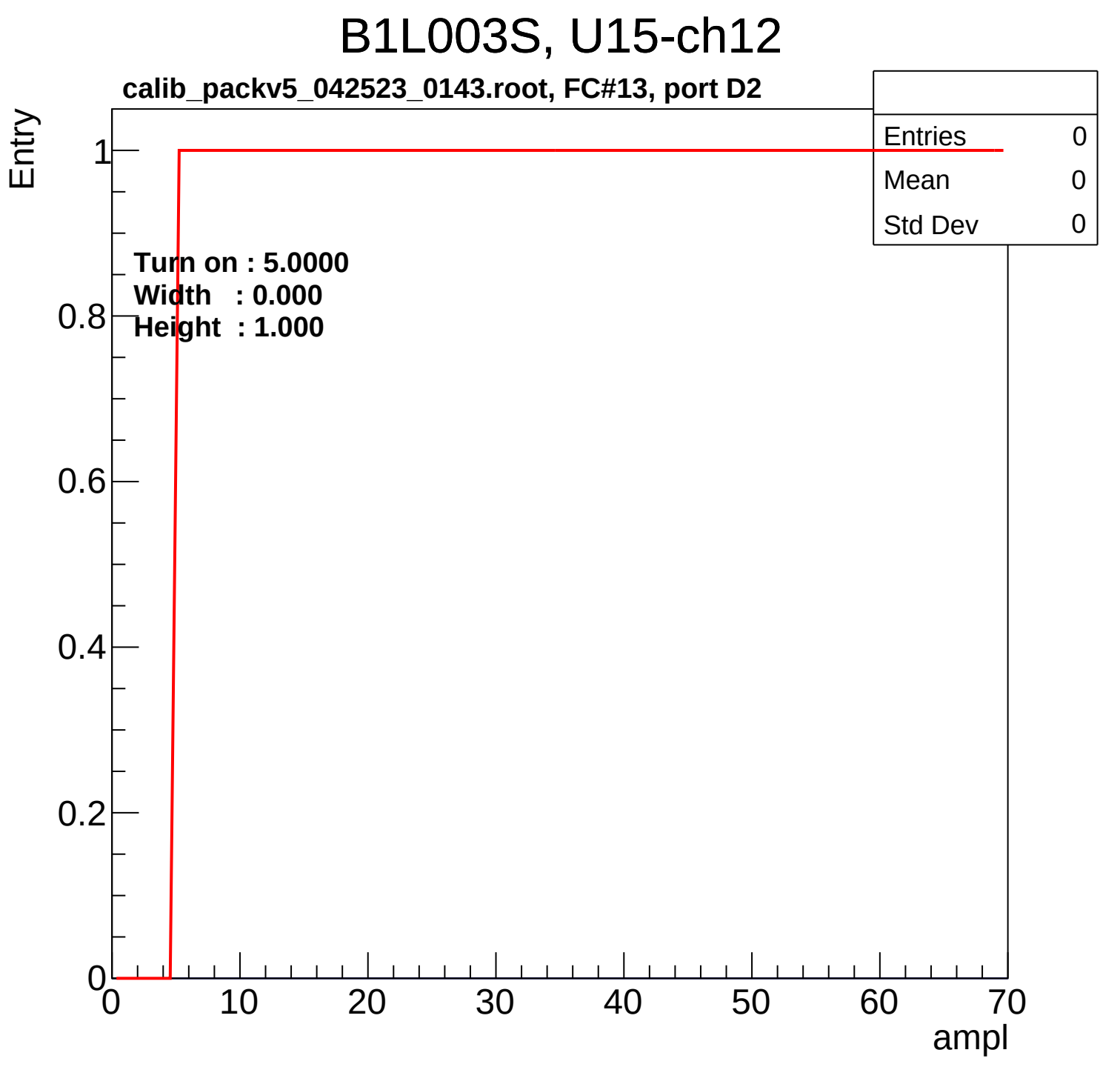
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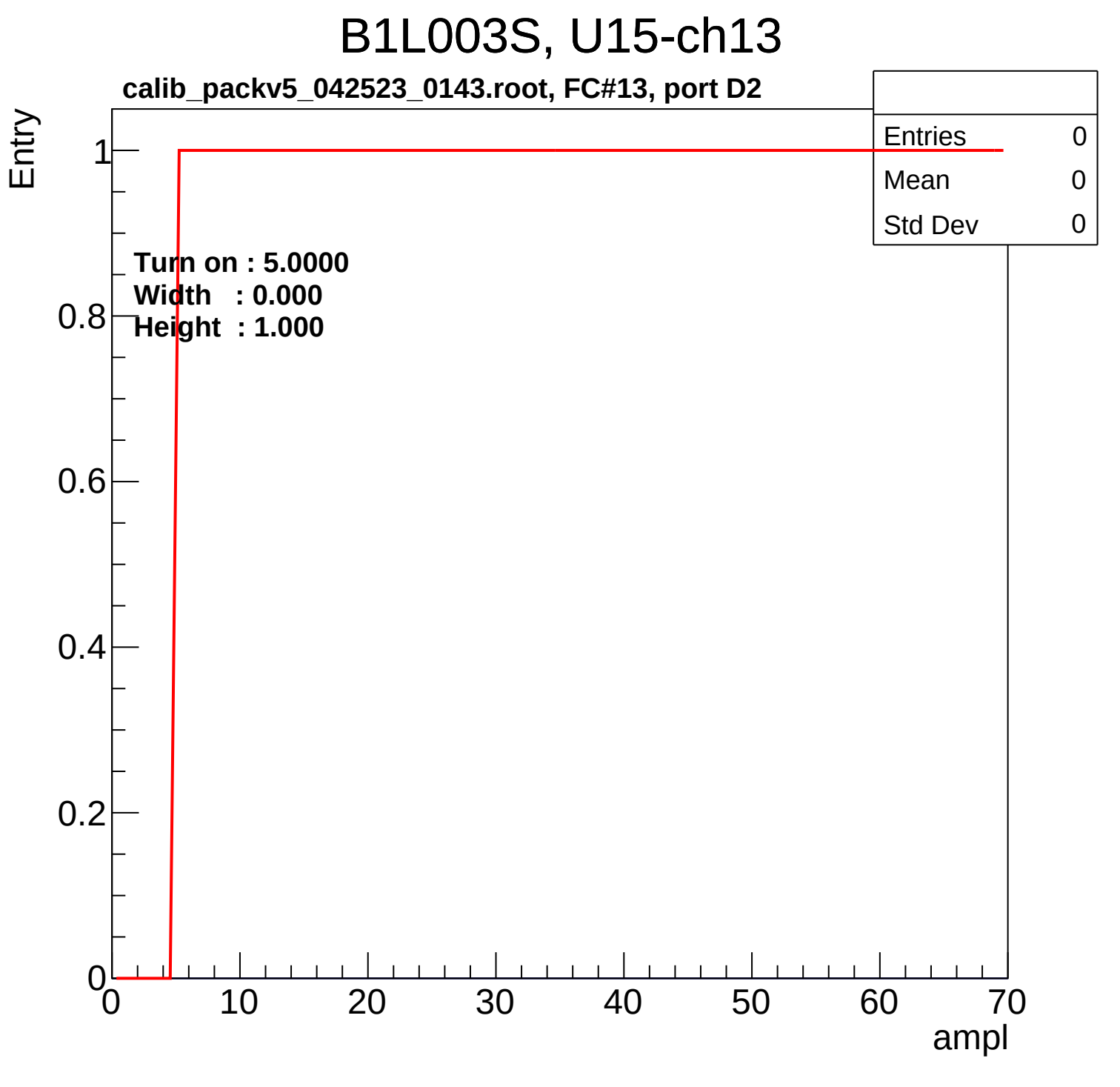
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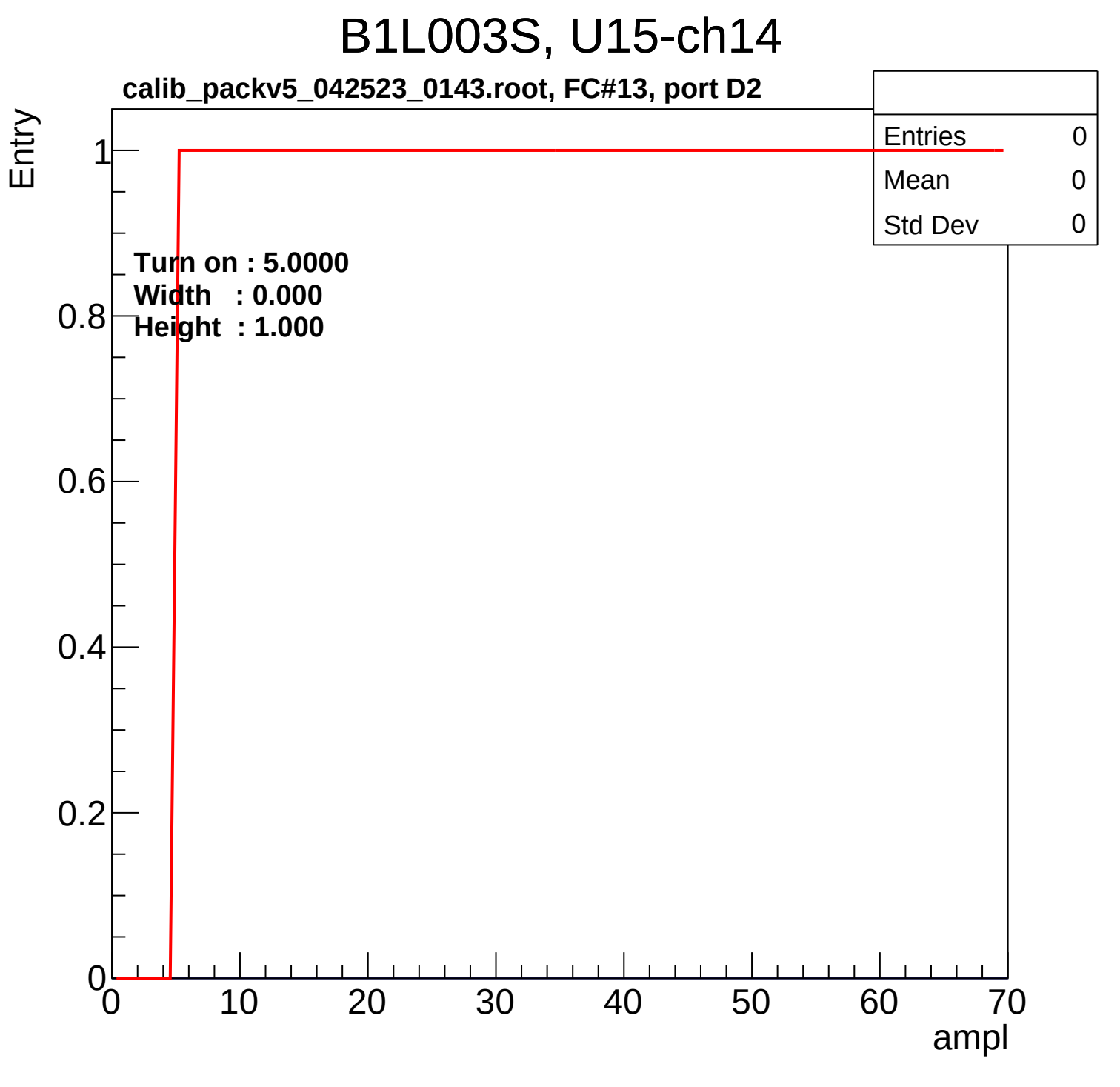
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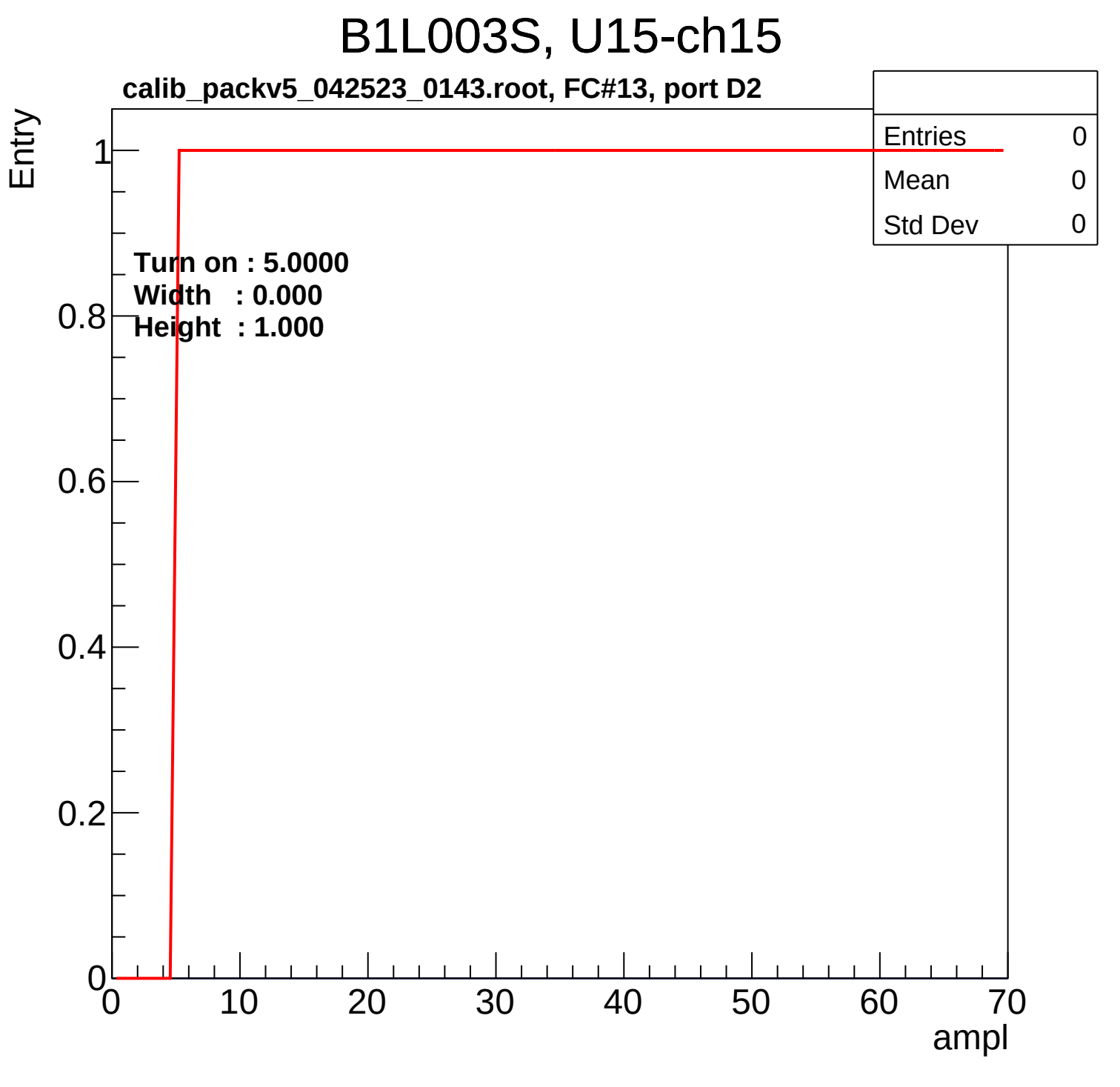
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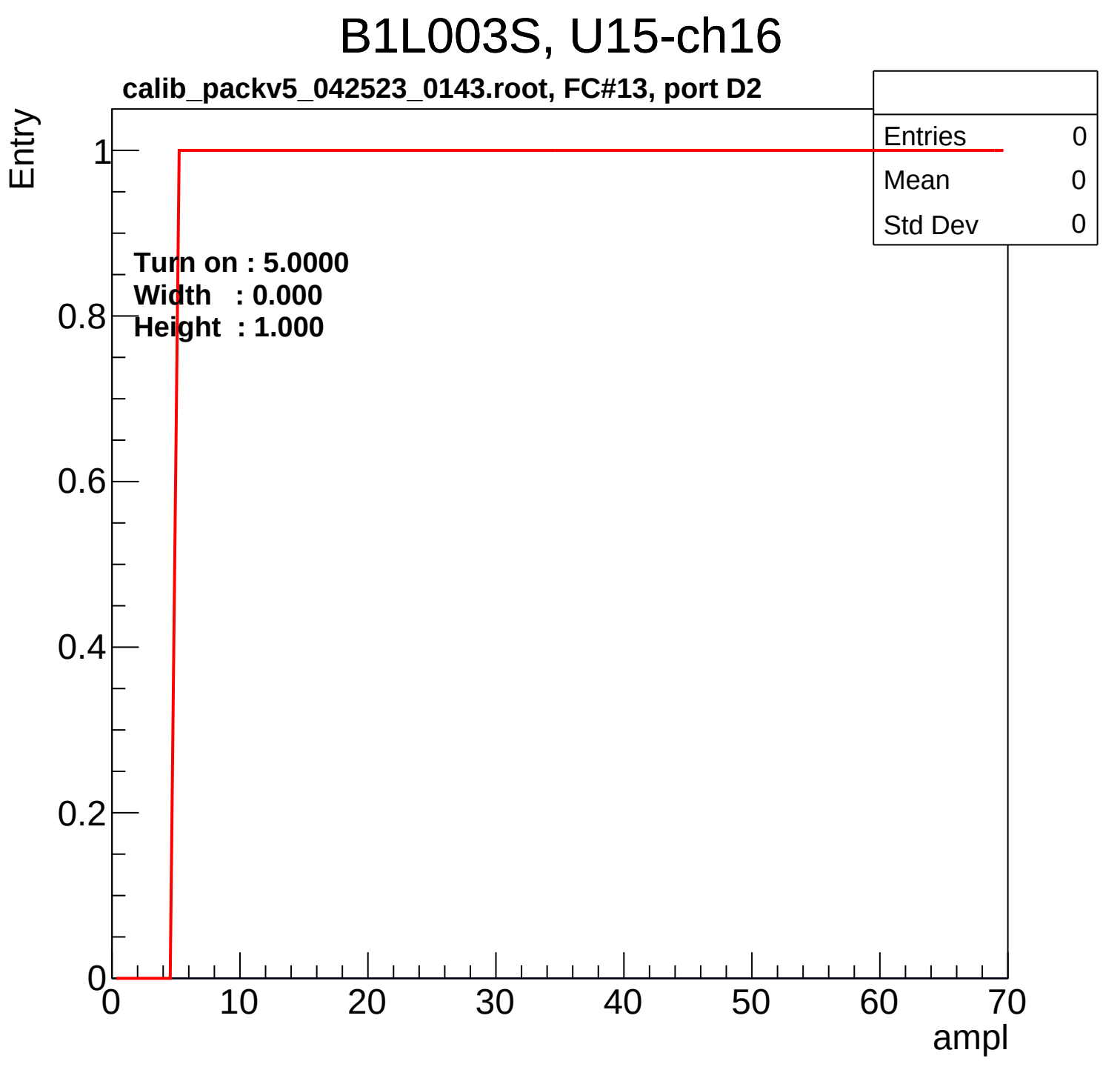
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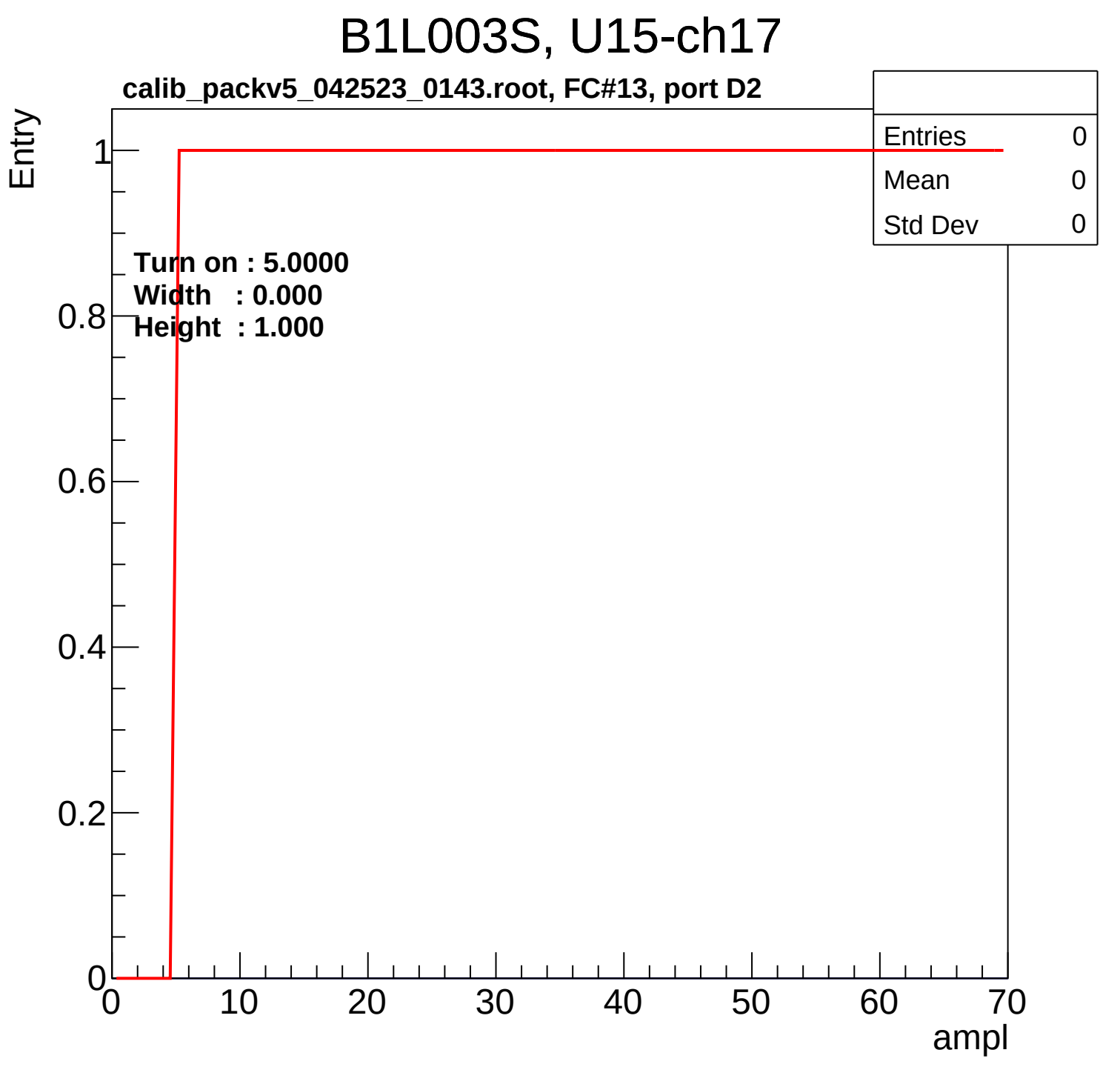
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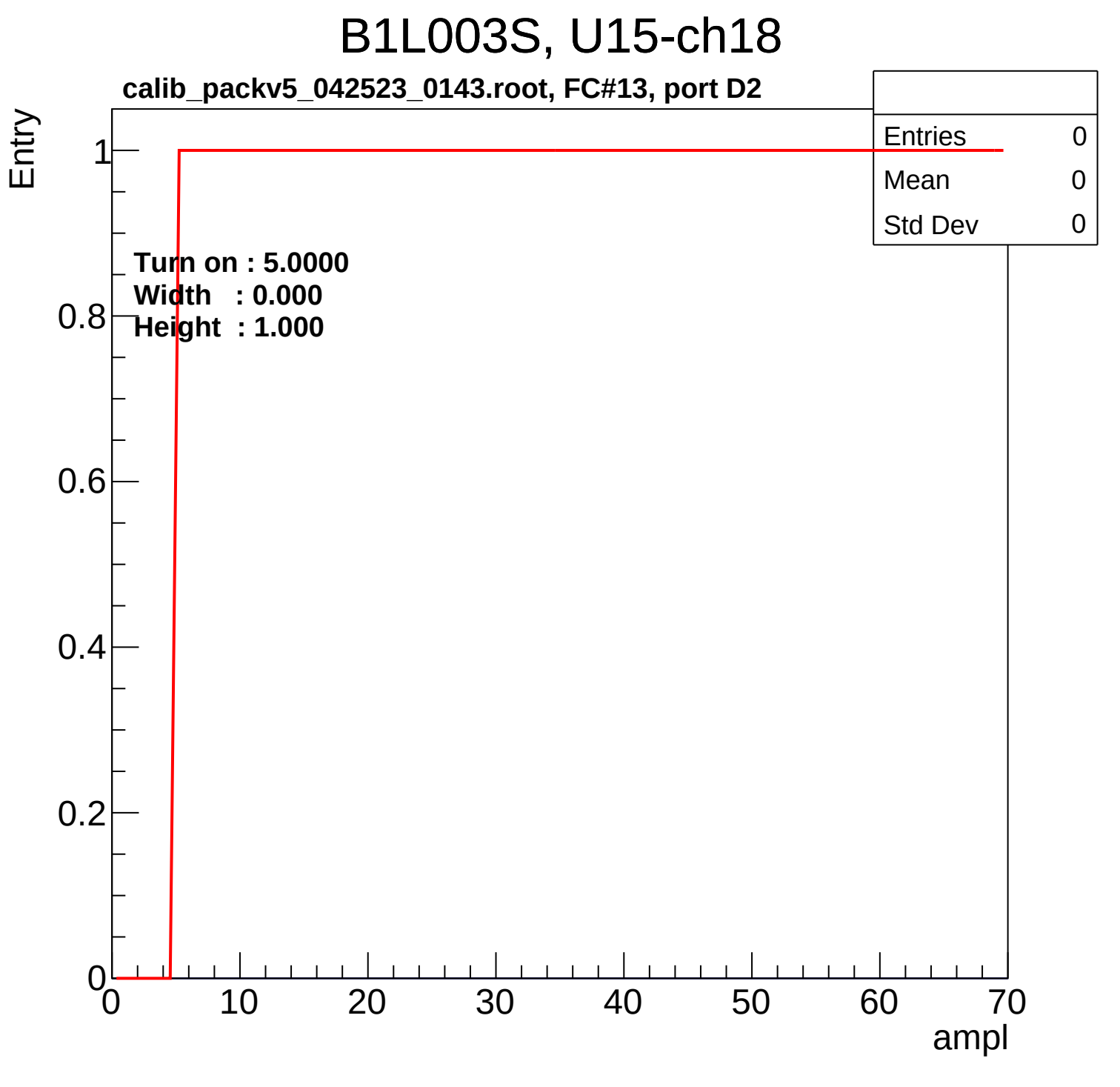
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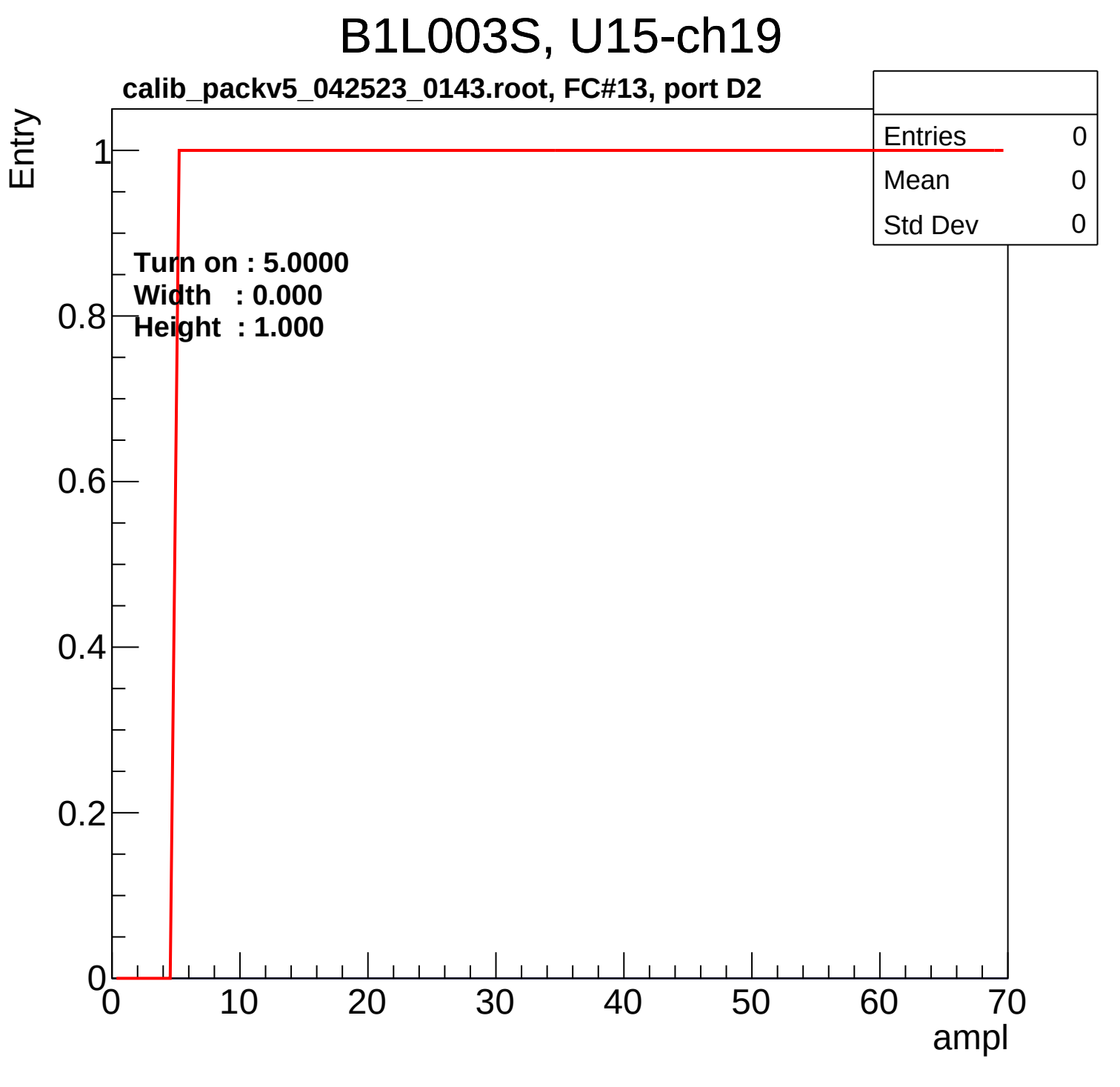
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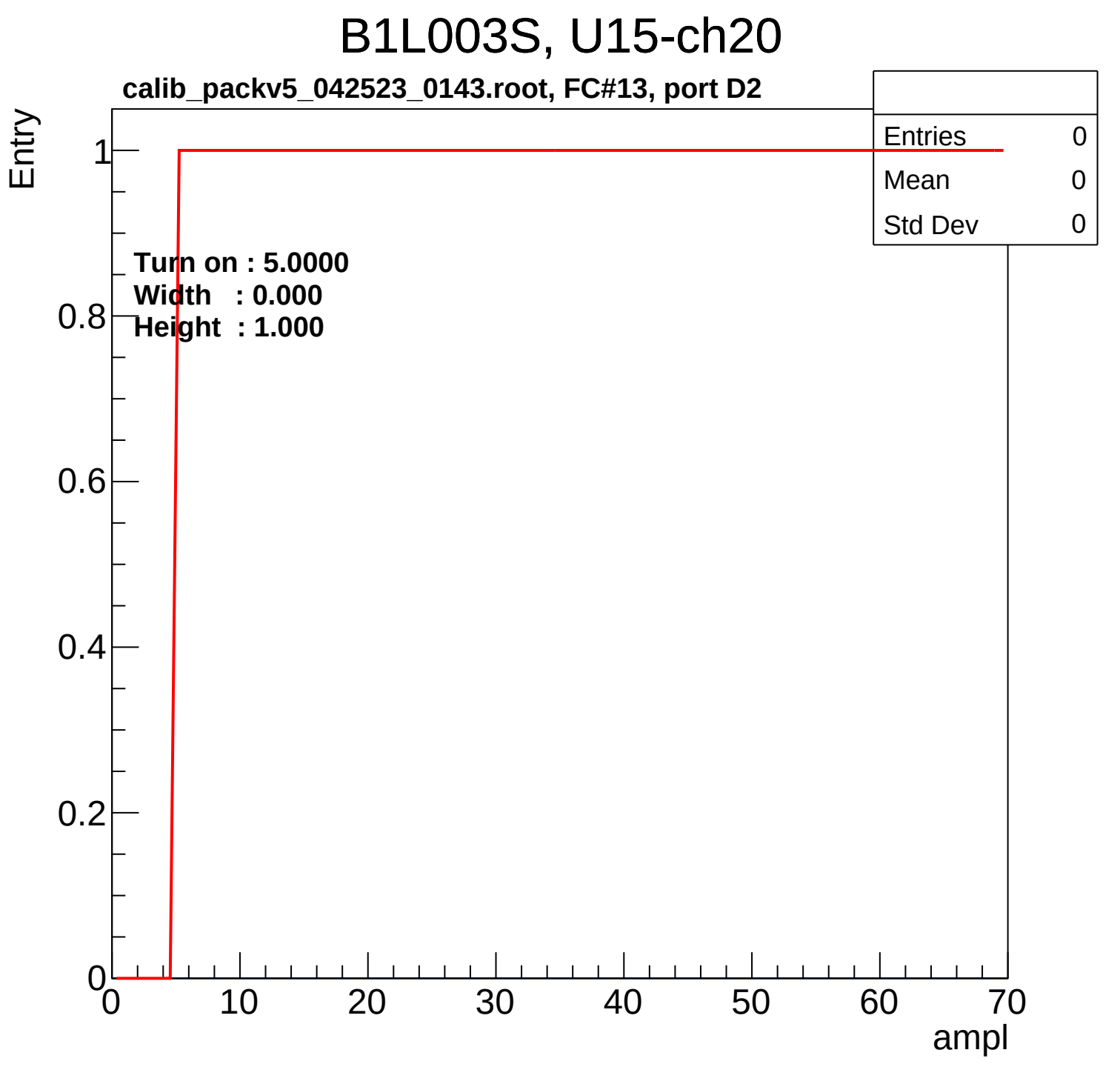
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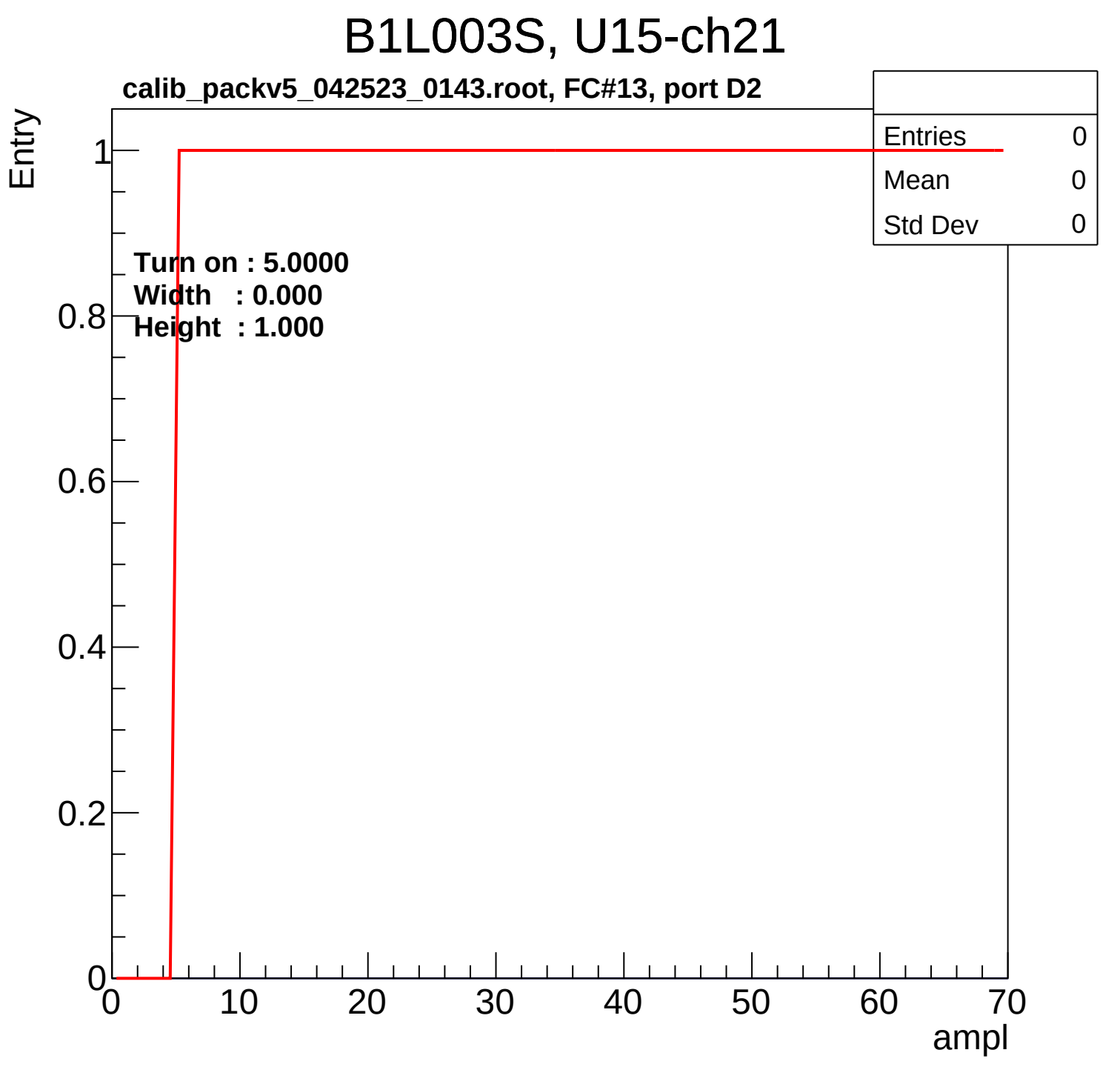
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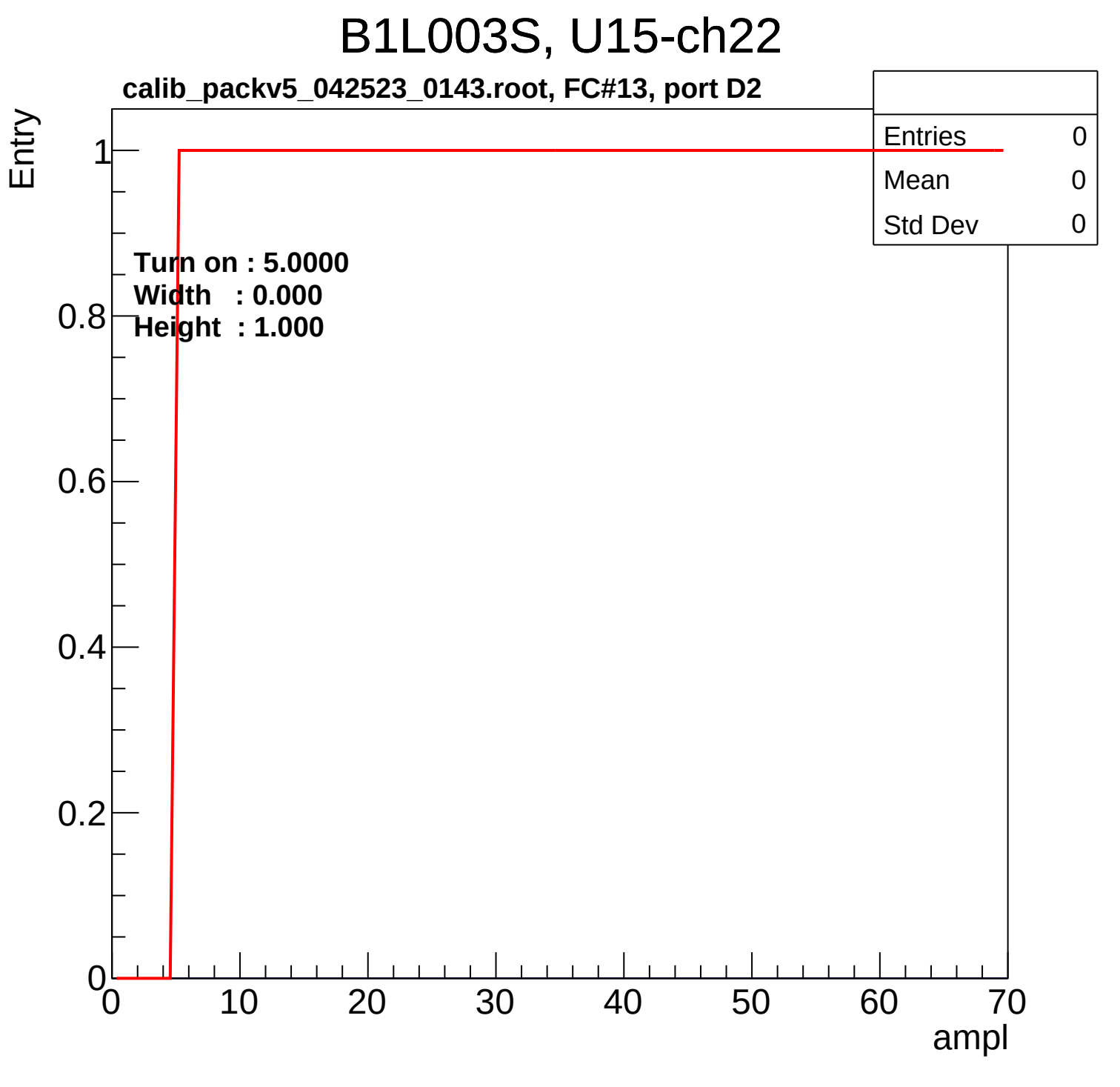
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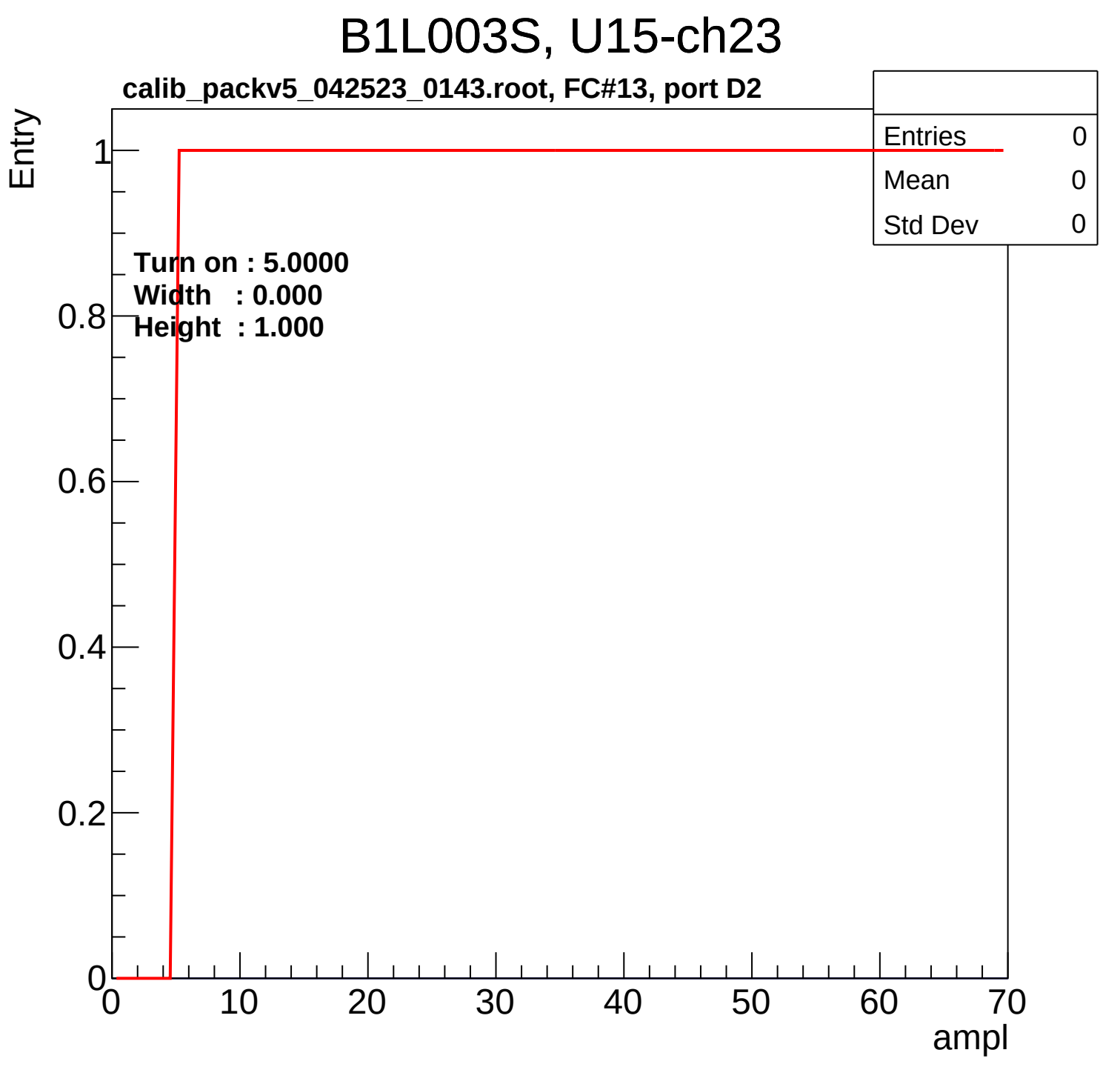
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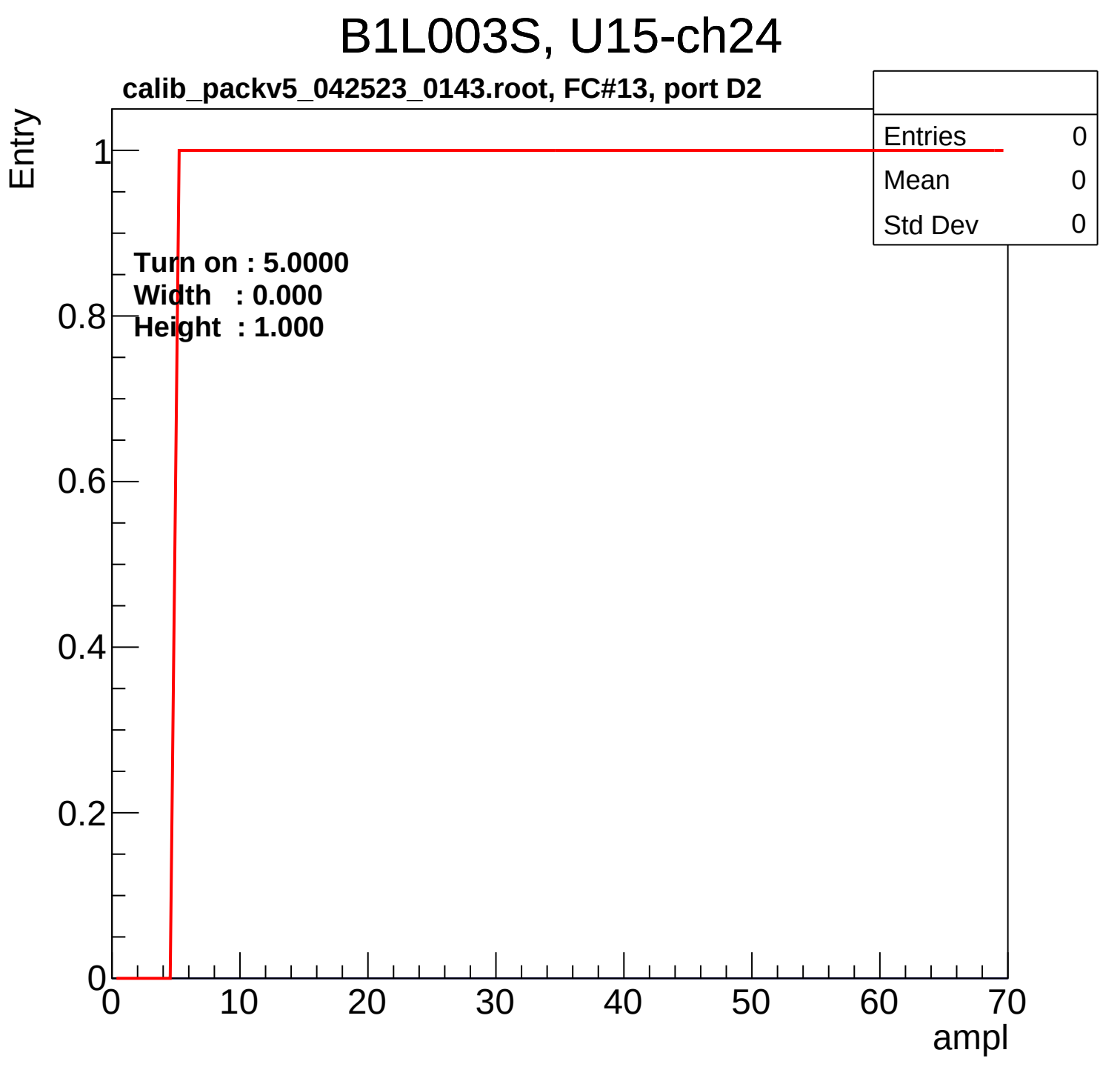
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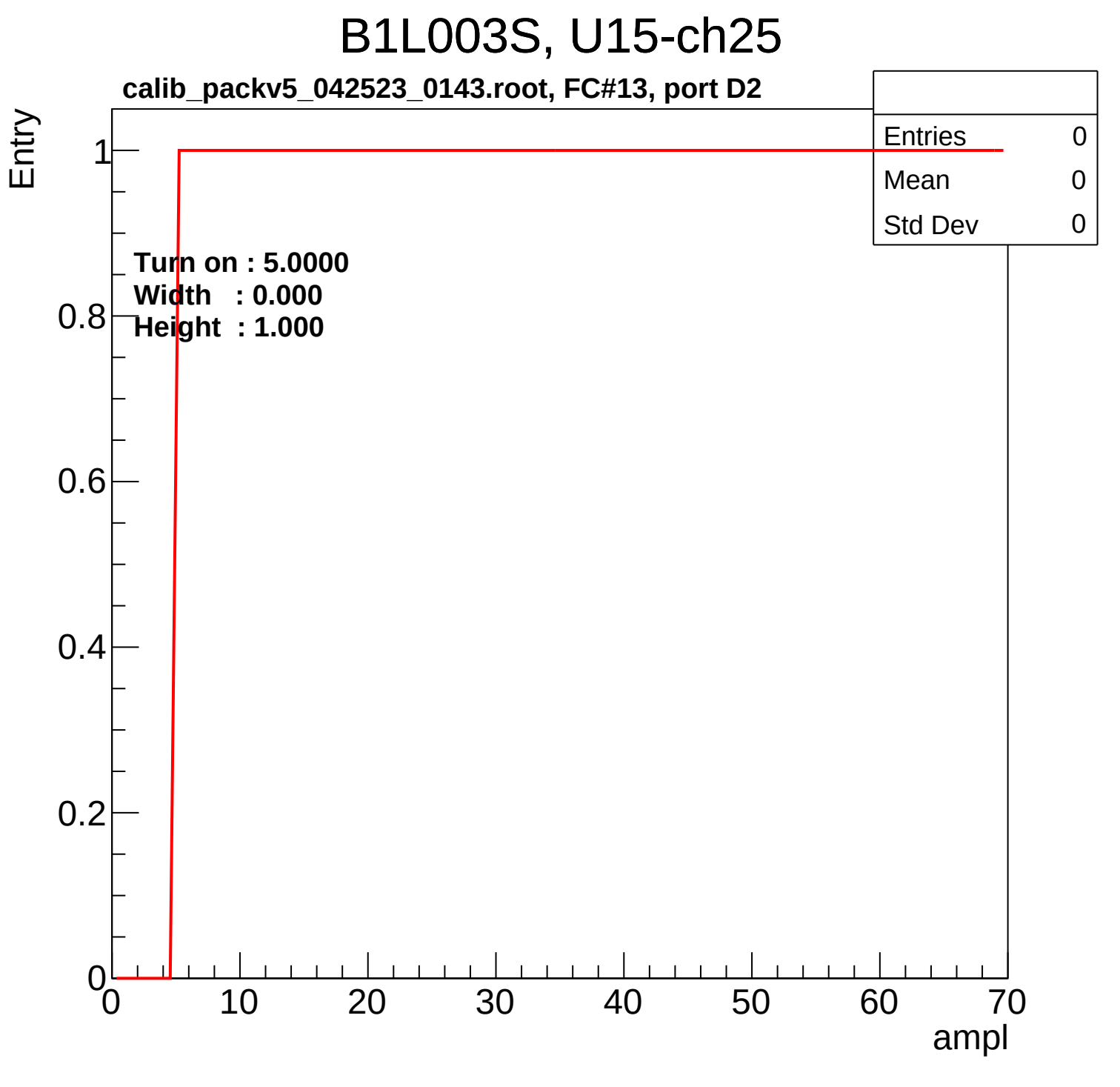
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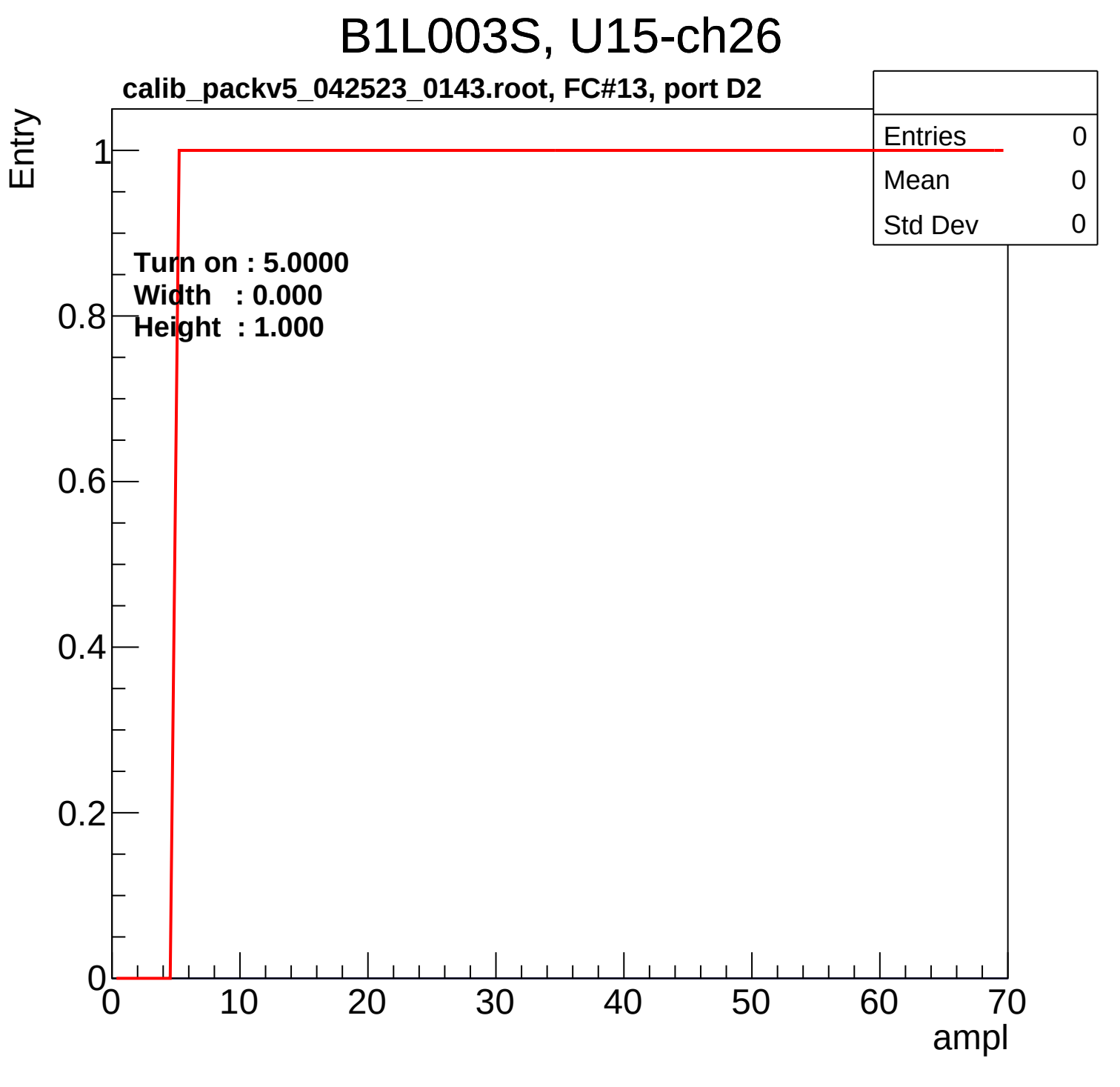
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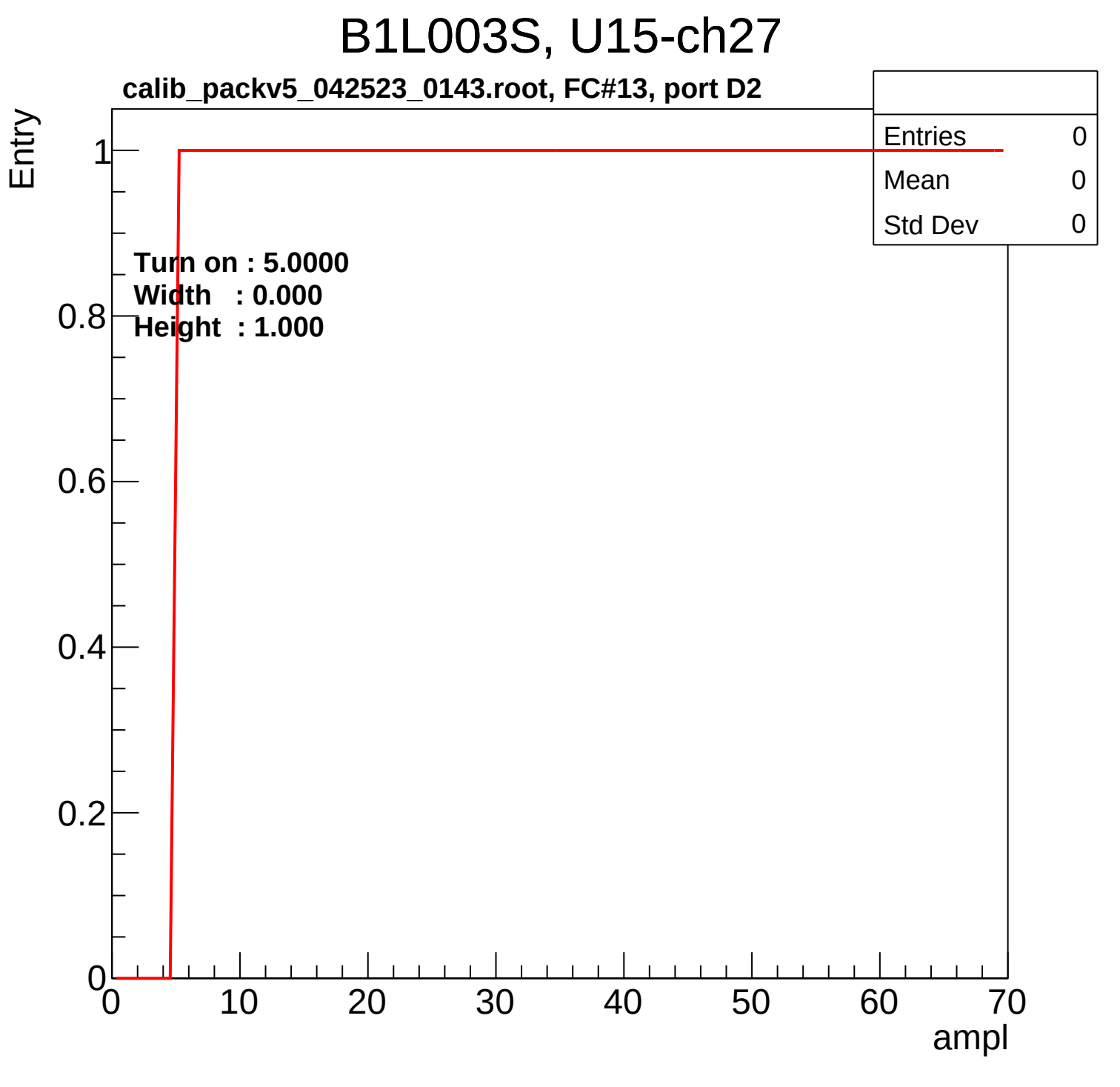
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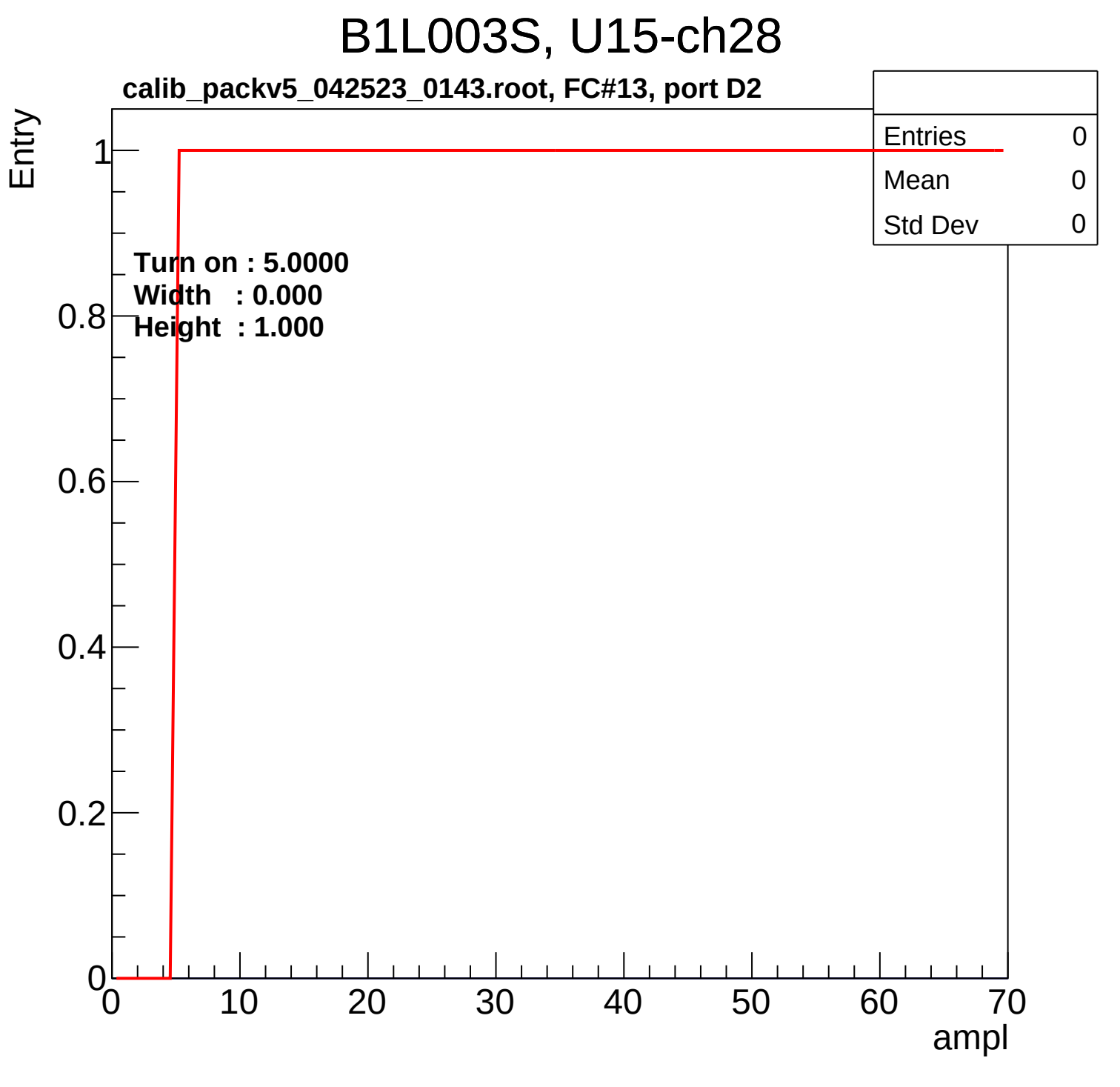
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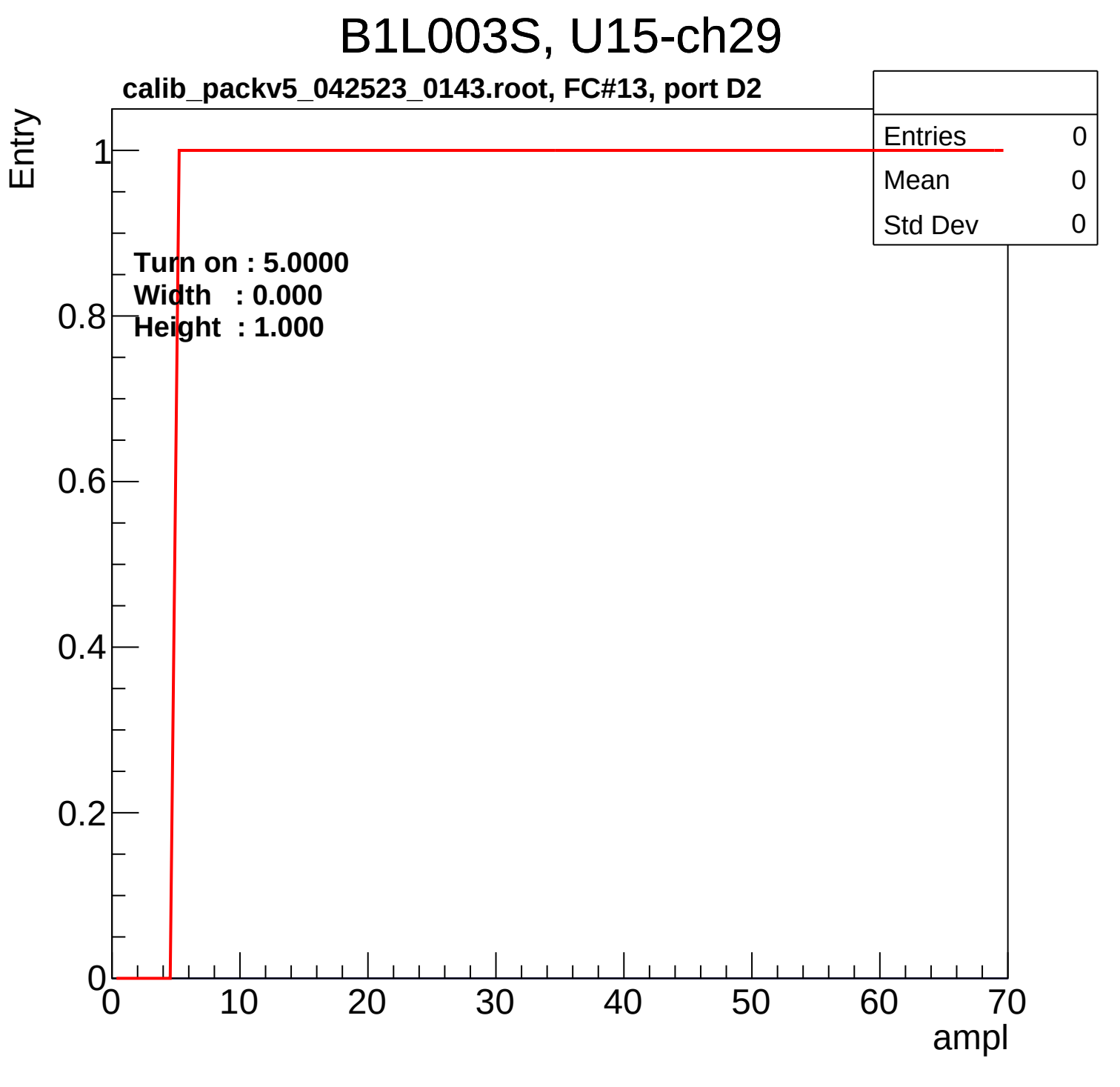
B1L003S, U15-ch29
calib_packv5_042523_0143.root, FC#13, port D2
Entries 0
Mean 0
Std Dev 0
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Height : 1.000
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0.6
0.4
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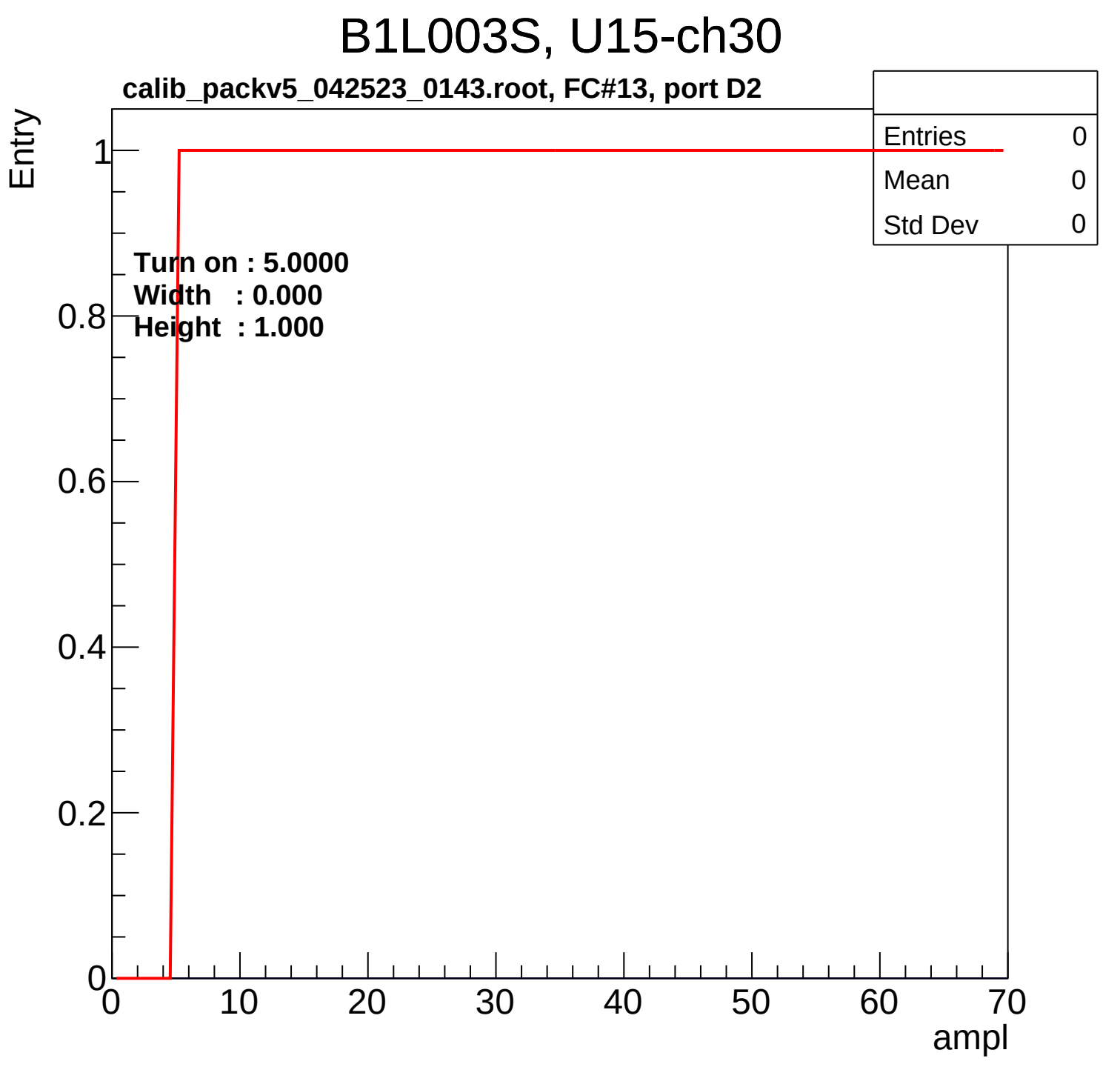
ampl


B1L003S, U15-ch30
calib_packv5_042523_0143.root, FC#13, port D2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
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Height : 1.000
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0.6
0.4
0.2
0
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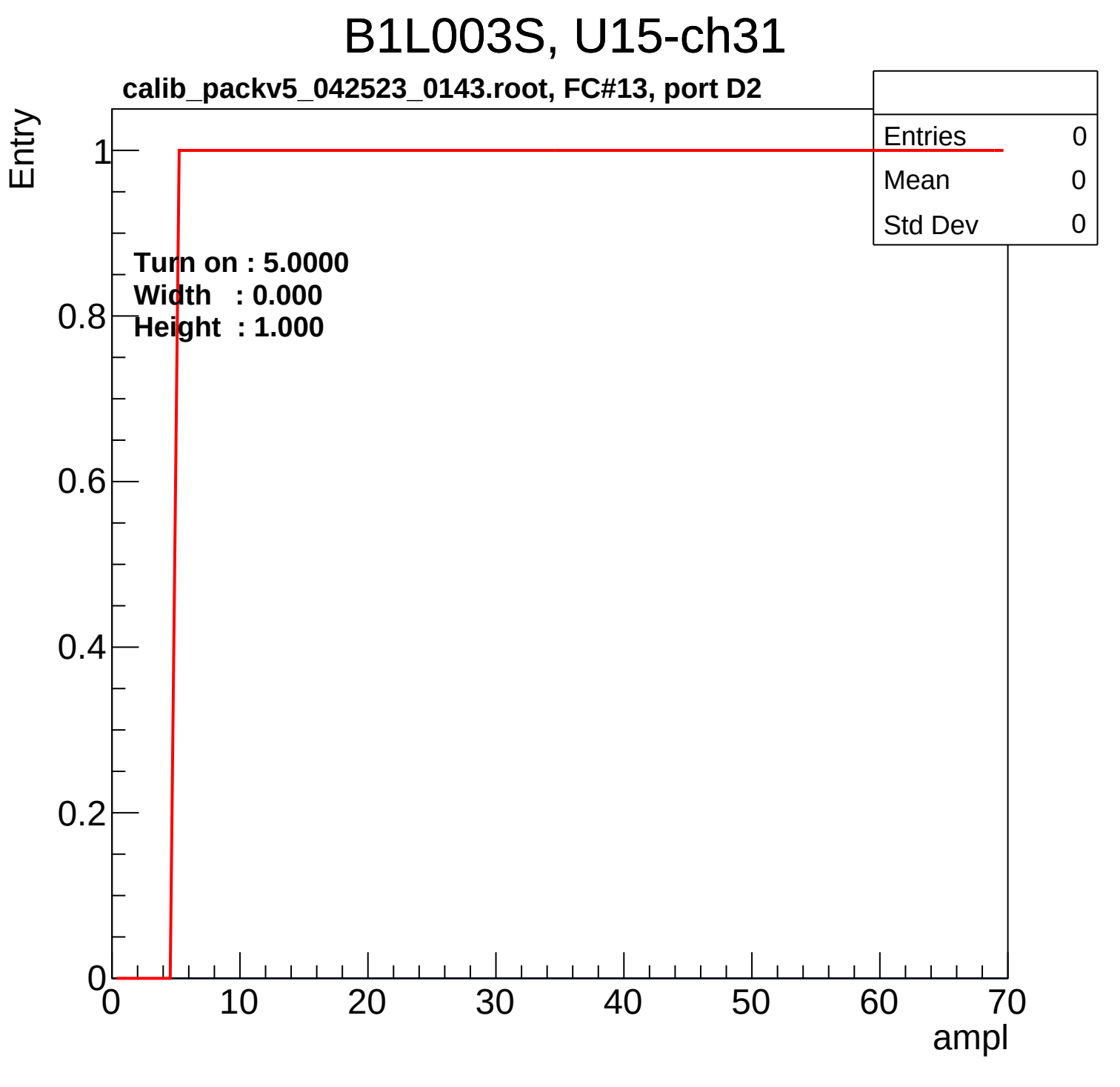
70
ampl


B1L003S, U15-ch31
calib_packv5_042523_0143.root, FC#13, port D2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
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0.8
0.6
0.4
0.2
0
0
10
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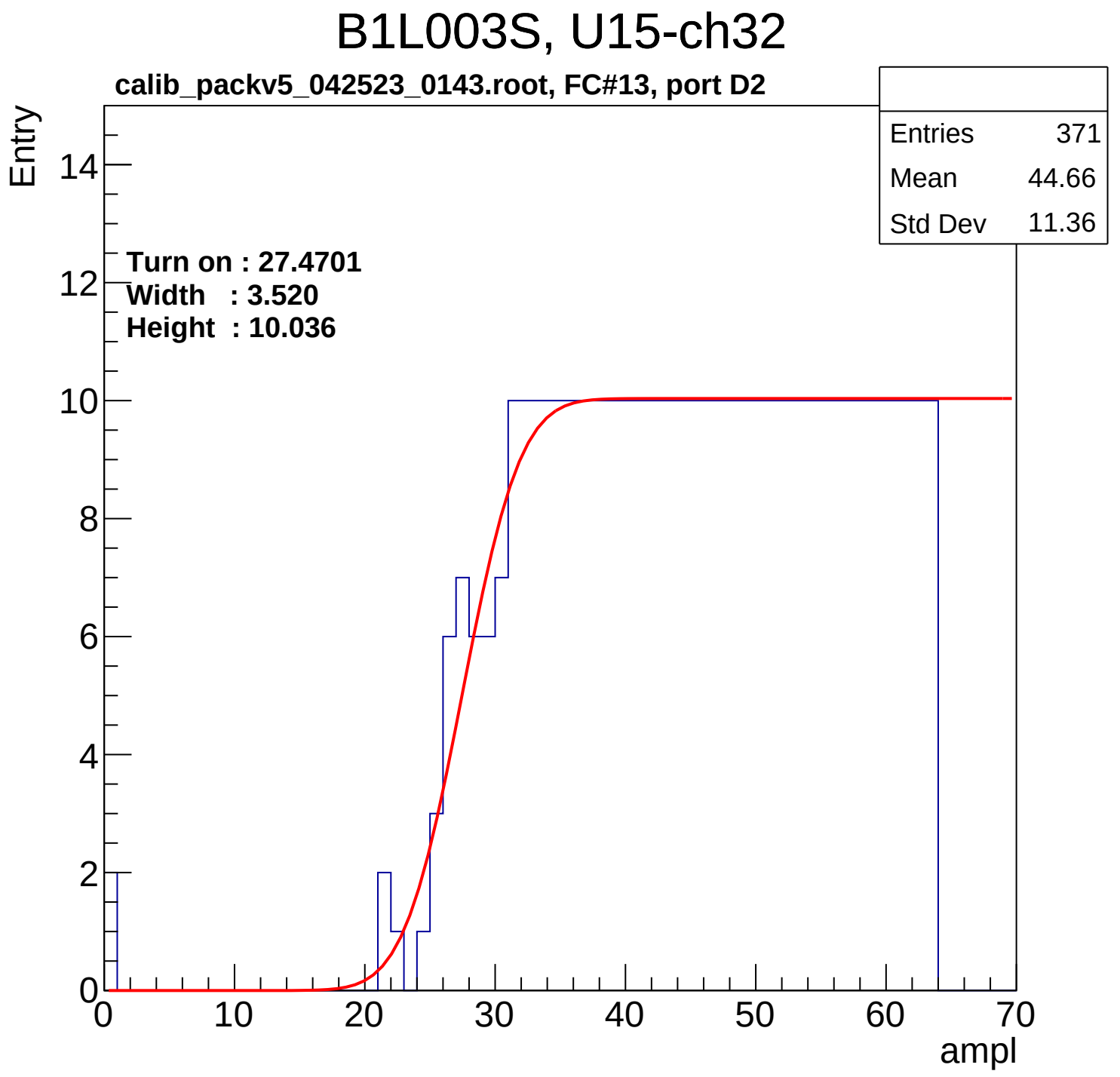
70
ampl


B1L003S, U15-ch32
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.66
Std Dev 11.36
Turn on : 27.4701
Width : 3.520
Height : 10.036
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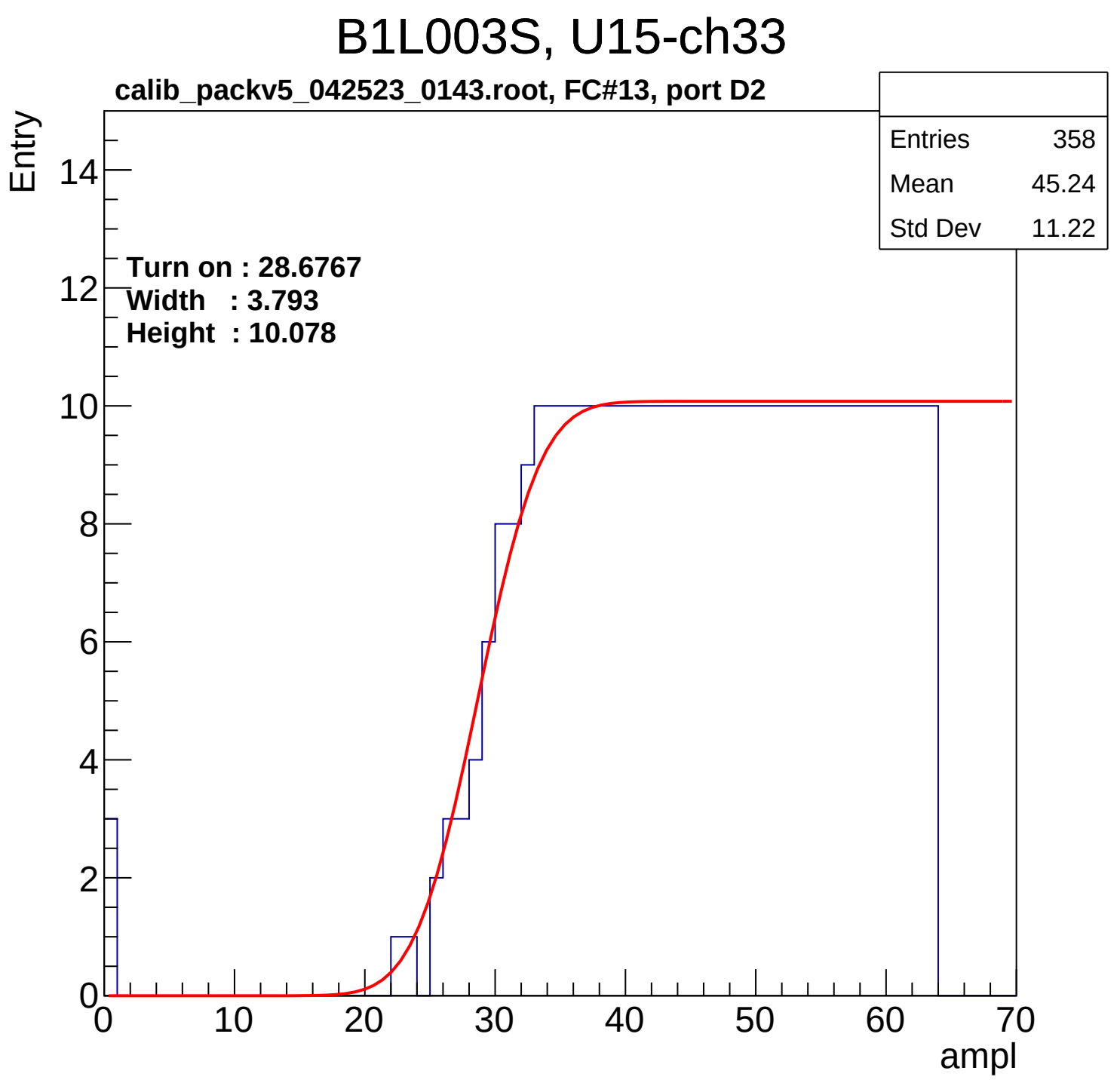
B1L003S, U15-ch33
calib_packv5_042523_0143.root, FC#13, port D2
Entries 358
Mean 45.24
Std Dev 11.22
Turn on : 28.6767
Width : 3.793
Height : 10.078
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ampl
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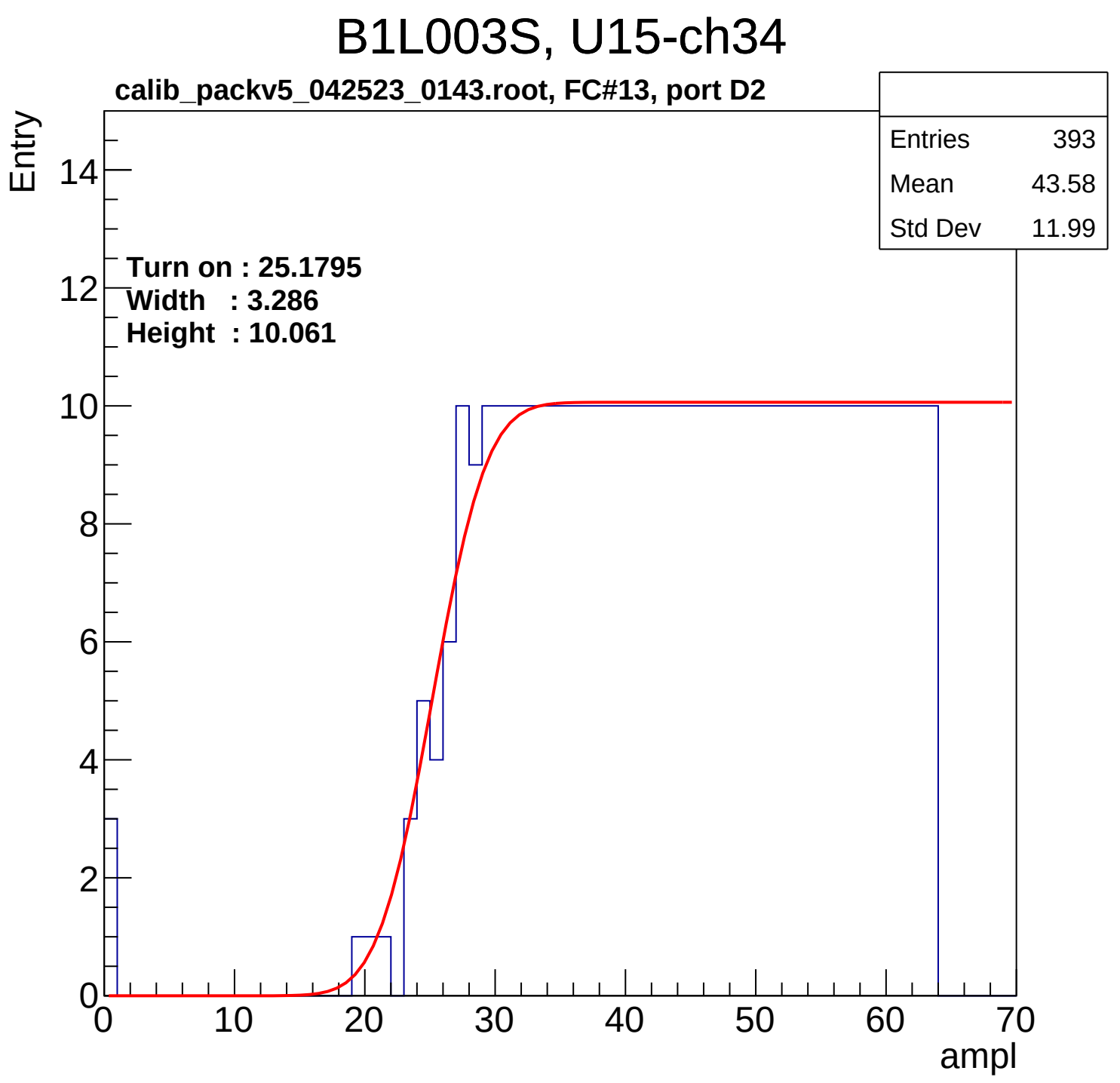
B1L003S, U15-ch34
calib_packv5_042523_0143.root, FC#13, port D2
Entries 393
Mean 43.58
Std Dev 11.99
Turn on : 25.1795
Width : 3.286
Height : 10.061
Entry
ampl
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2
4
6
8
10
12
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60
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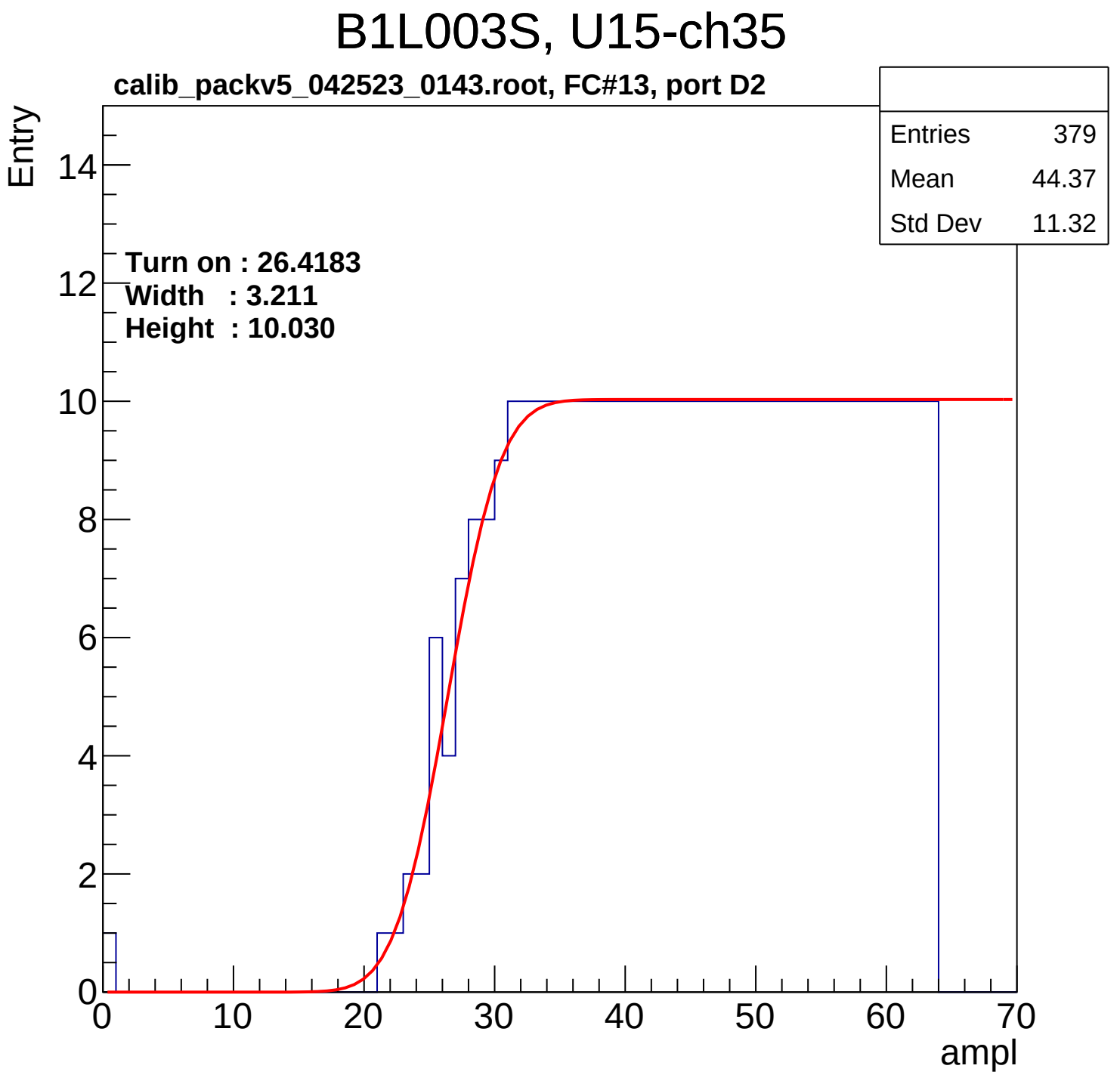
B1L003S, U15-ch35
calib_packv5_042523_0143.root, FC#13, port D2
Entries 379
Mean 44.37
Std Dev 11.32
Turn on : 26.4183
Width : 3.211
Height : 10.030
Entry
ampl
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6
8
10
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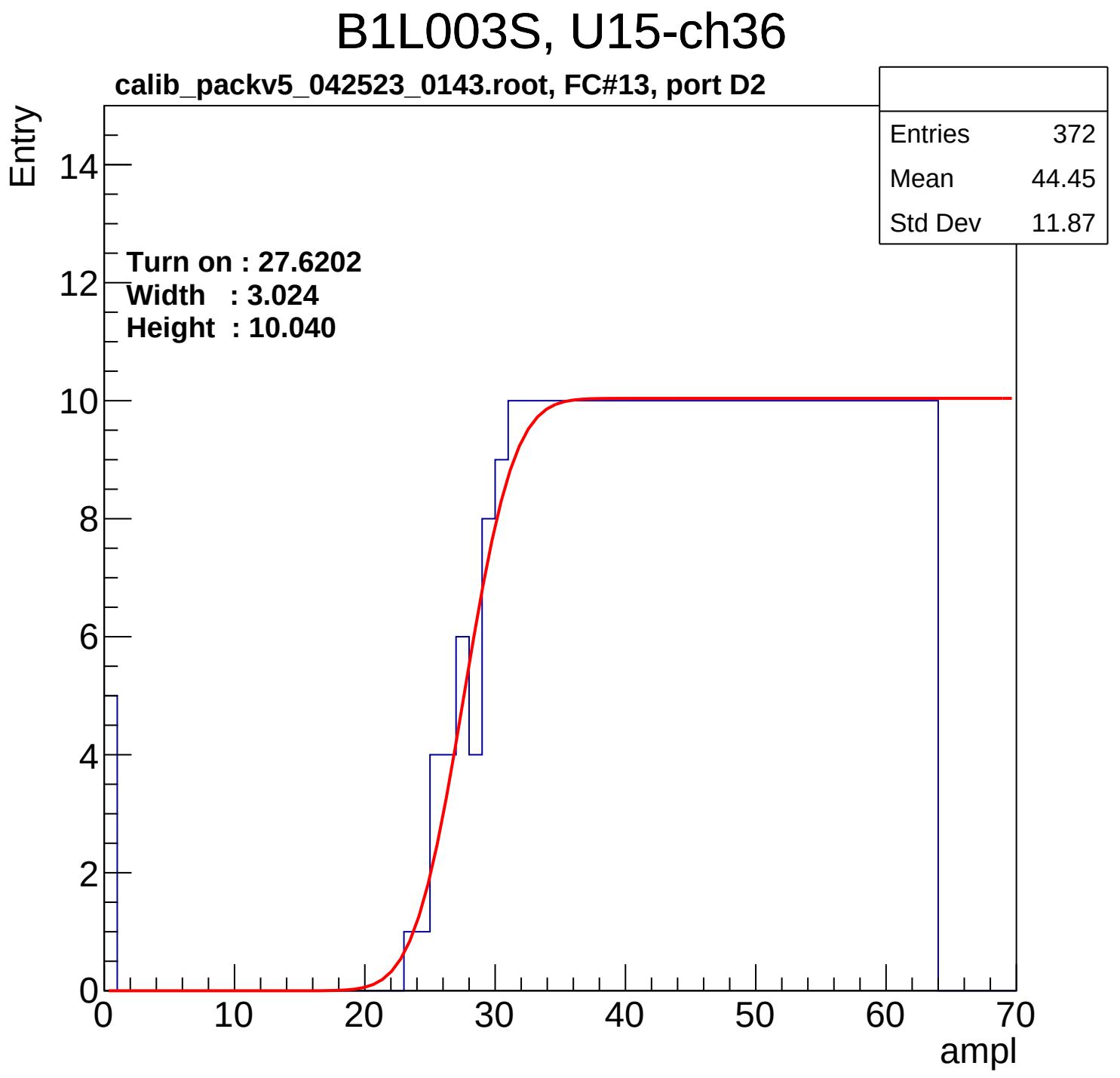
B1L003S, U15-ch36
calib_packv5_042523_0143.root, FC#13, port D2
Entries 372
Mean 44.45
Std Dev 11.87
Turn on : 27.6202
Width : 3.024
Height : 10.040
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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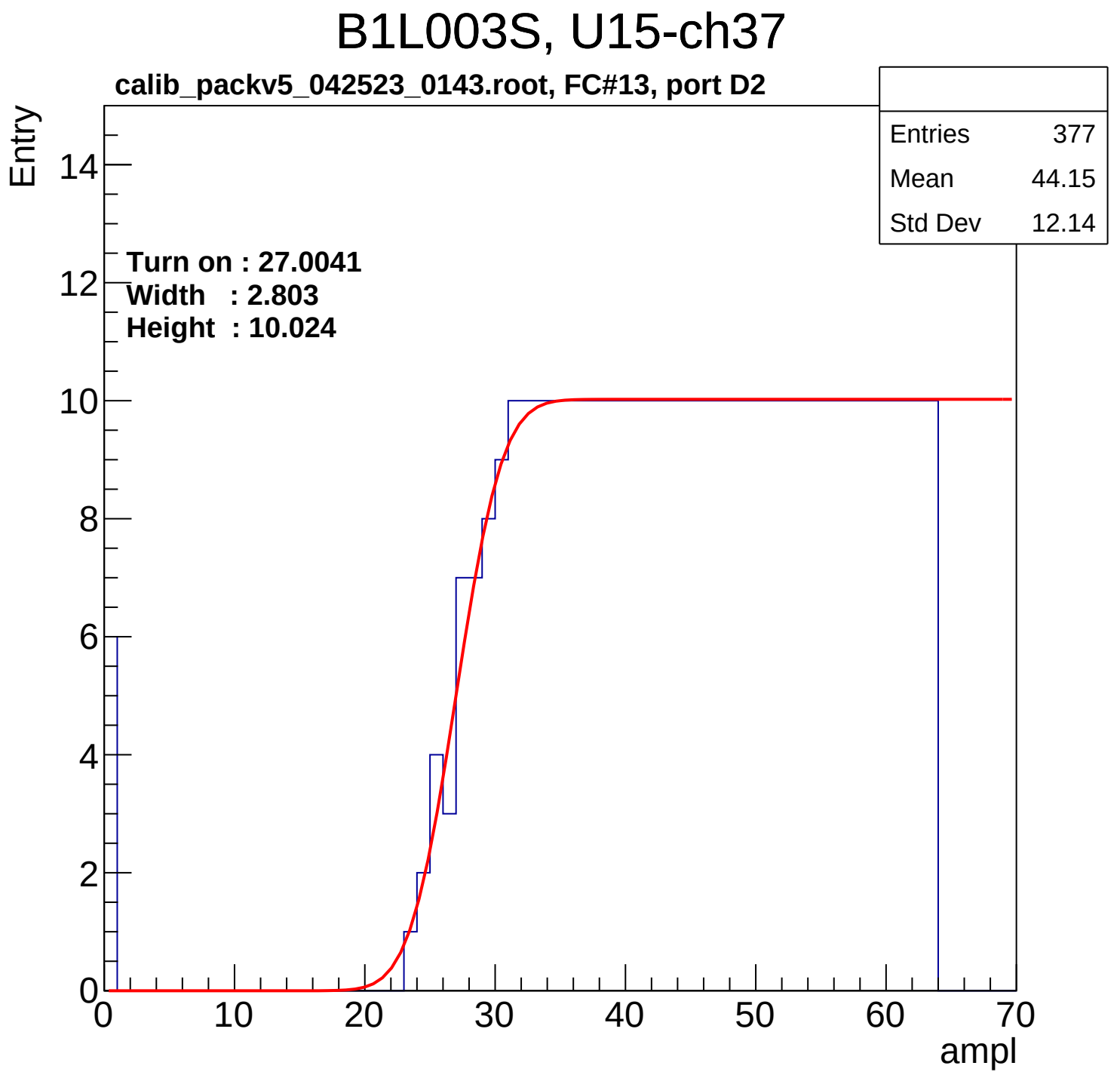
B1L003S, U15-ch37
calib_packv5_042523_0143.root, FC#13, port D2
Entries 377
Mean 44.15
Std Dev 12.14
Turn on : 27.0041
Width : 2.803
Height : 10.024
Entry
ampl
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2
4
6
8
10
12
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0
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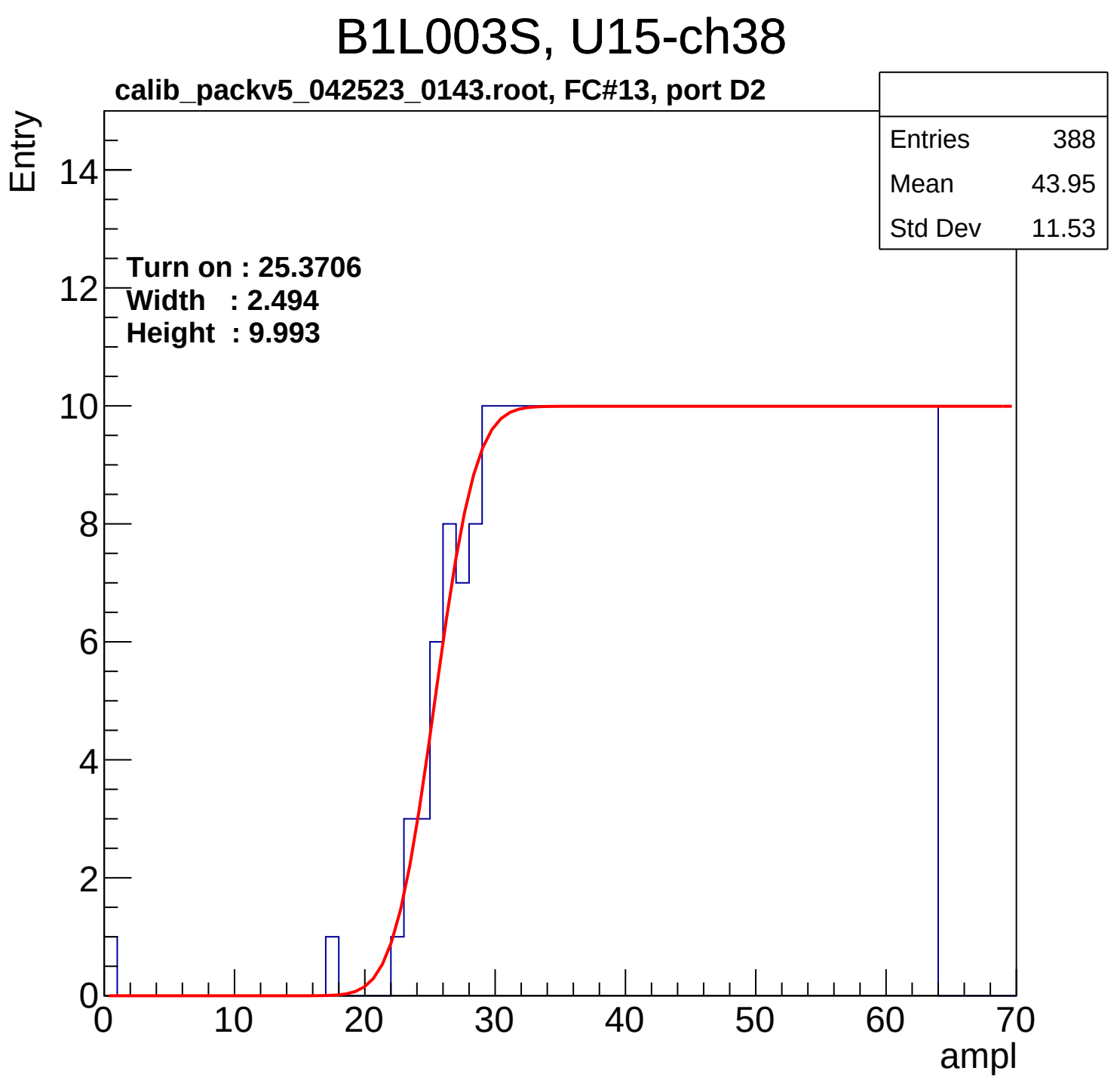
B1L003S, U15-ch38
calib_packv5_042523_0143.root, FC#13, port D2
Entries 388
Mean 43.95
Std Dev 11.53
Turn on : 25.3706
Width : 2.494
Height : 9.993
Entry
ampl
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2
4
6
8
10
12
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0
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20
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60
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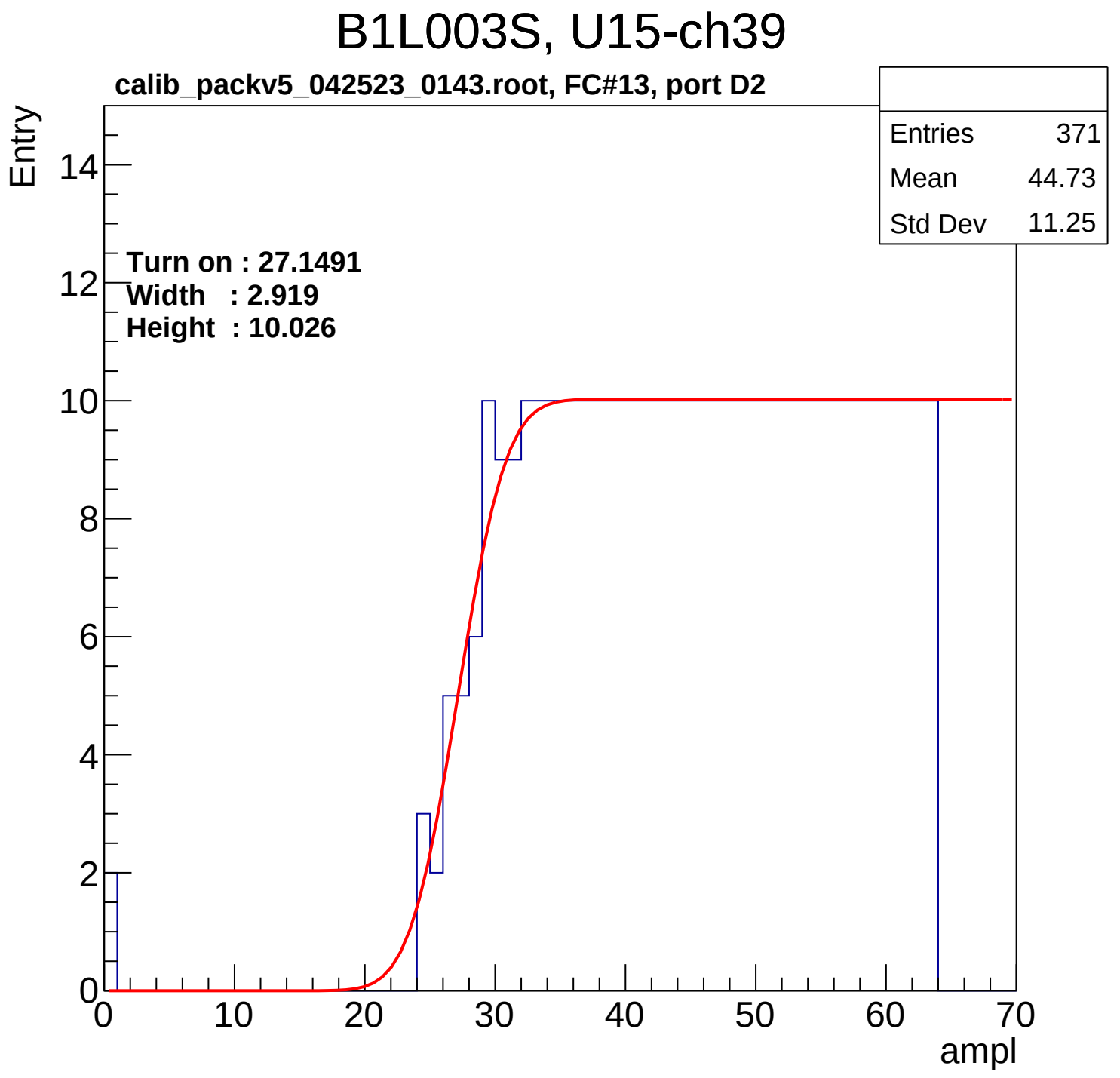
B1L003S, U15-ch39
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.73
Std Dev 11.25
Turn on : 27.1491
Width : 2.919
Height : 10.026
Entry
ampl
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2
4
6
8
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12
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0
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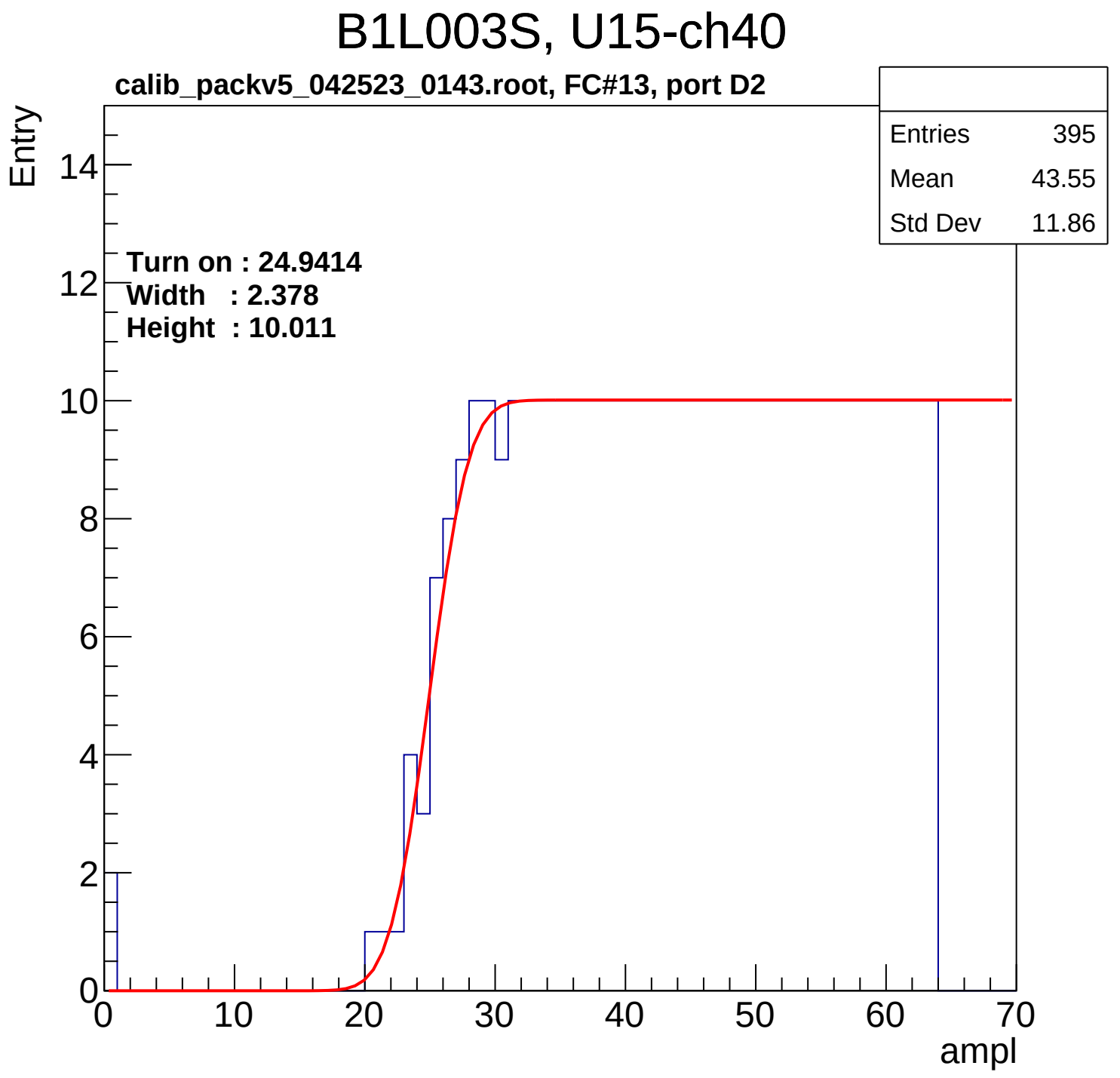
B1L003S, U15-ch40
calib_packv5_042523_0143.root, FC#13, port D2
Entries 395
Mean 43.55
Std Dev 11.86
Turn on : 24.9414
Width : 2.378
Height : 10.011
Entry
ampl
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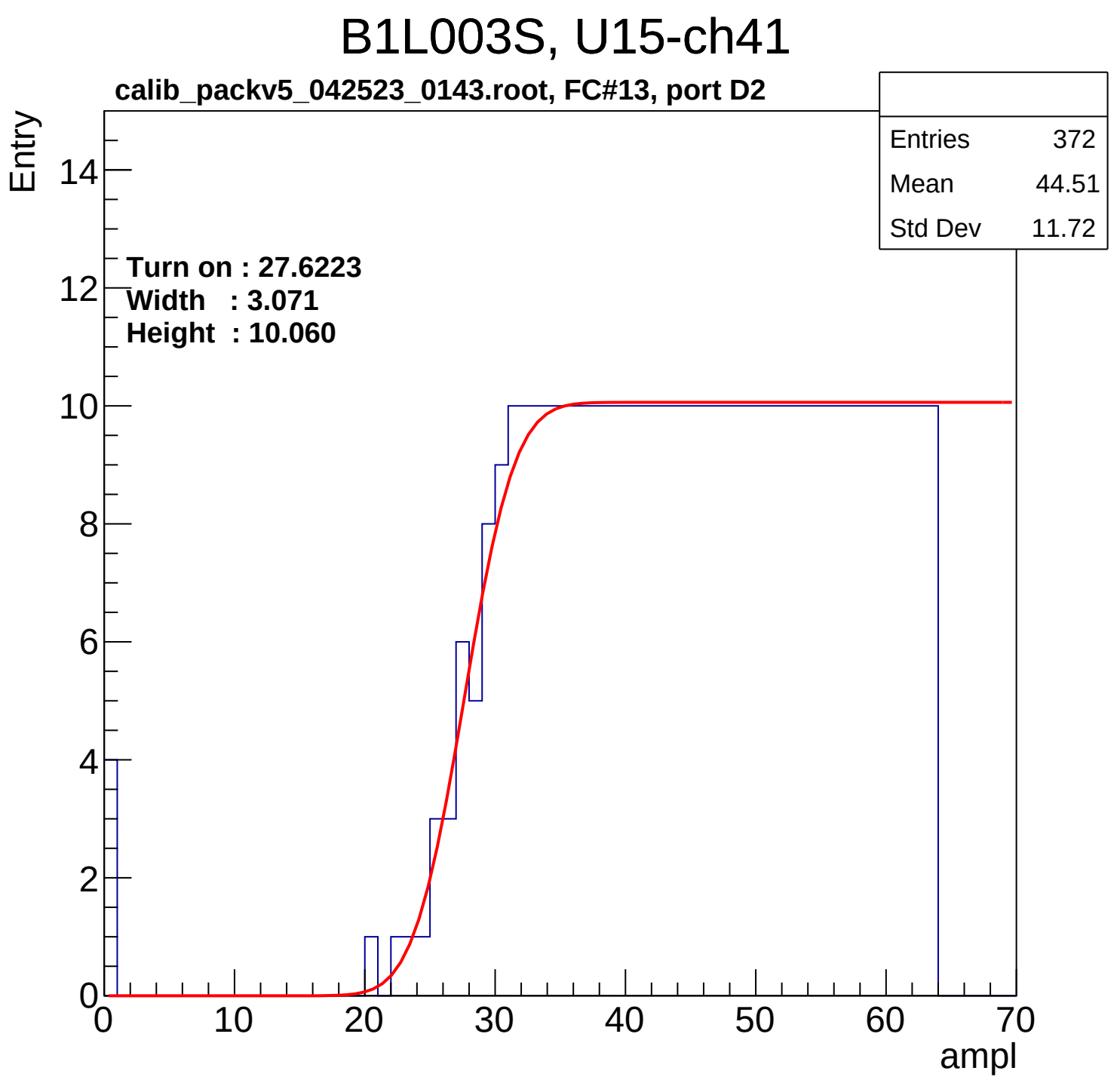
B1L003S, U15-ch41
calib_packv5_042523_0143.root, FC#13, port D2
Entries 372
Mean 44.51
Std Dev 11.72
Turn on : 27.6223
Width : 3.071
Height : 10.060
Entry
ampl
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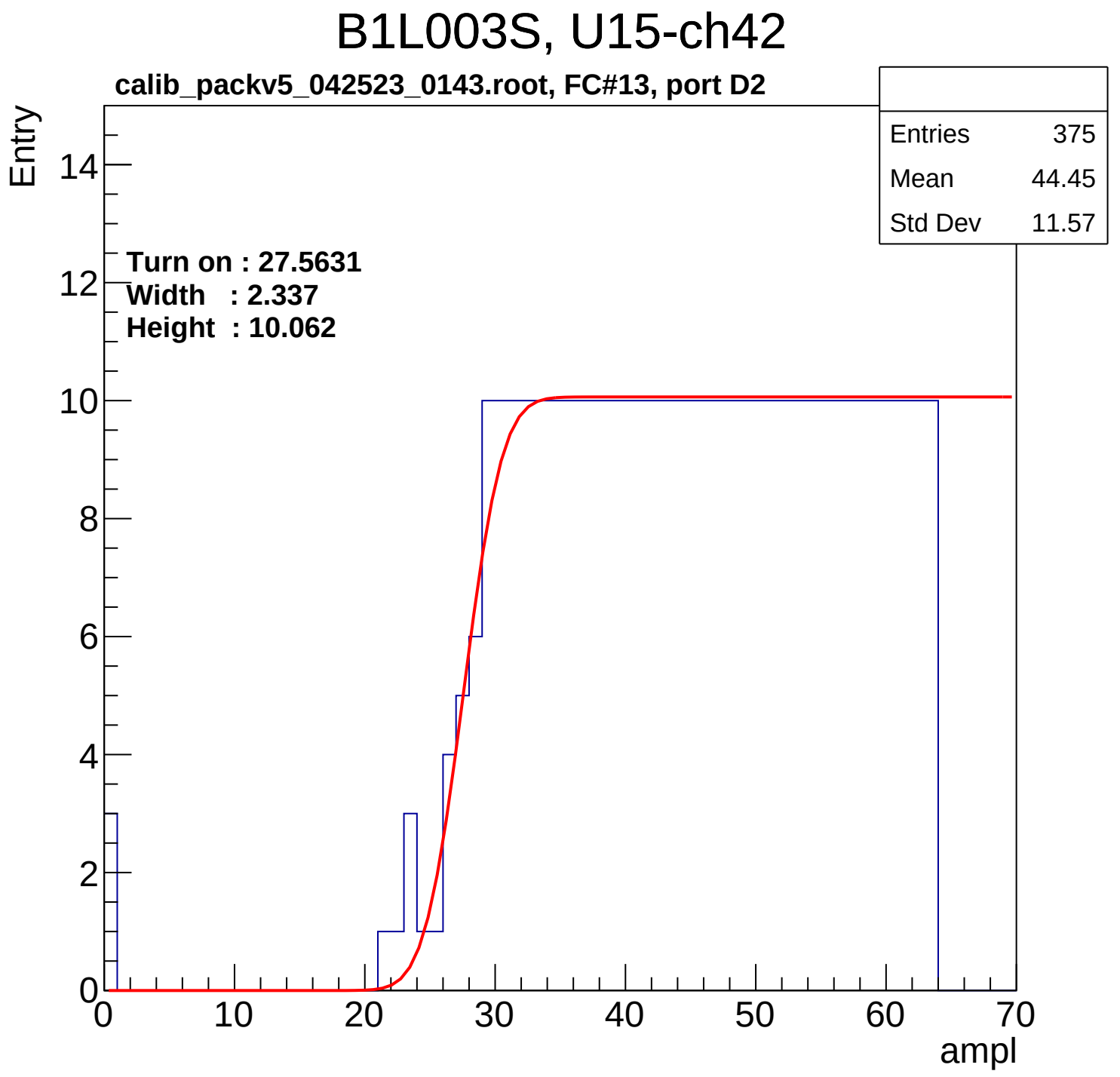
B1L003S, U15-ch42
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.45
Std Dev 11.57
Turn on : 27.5631
Width : 2.337
Height : 10.062
Entry
ampl
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6
8
10
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0
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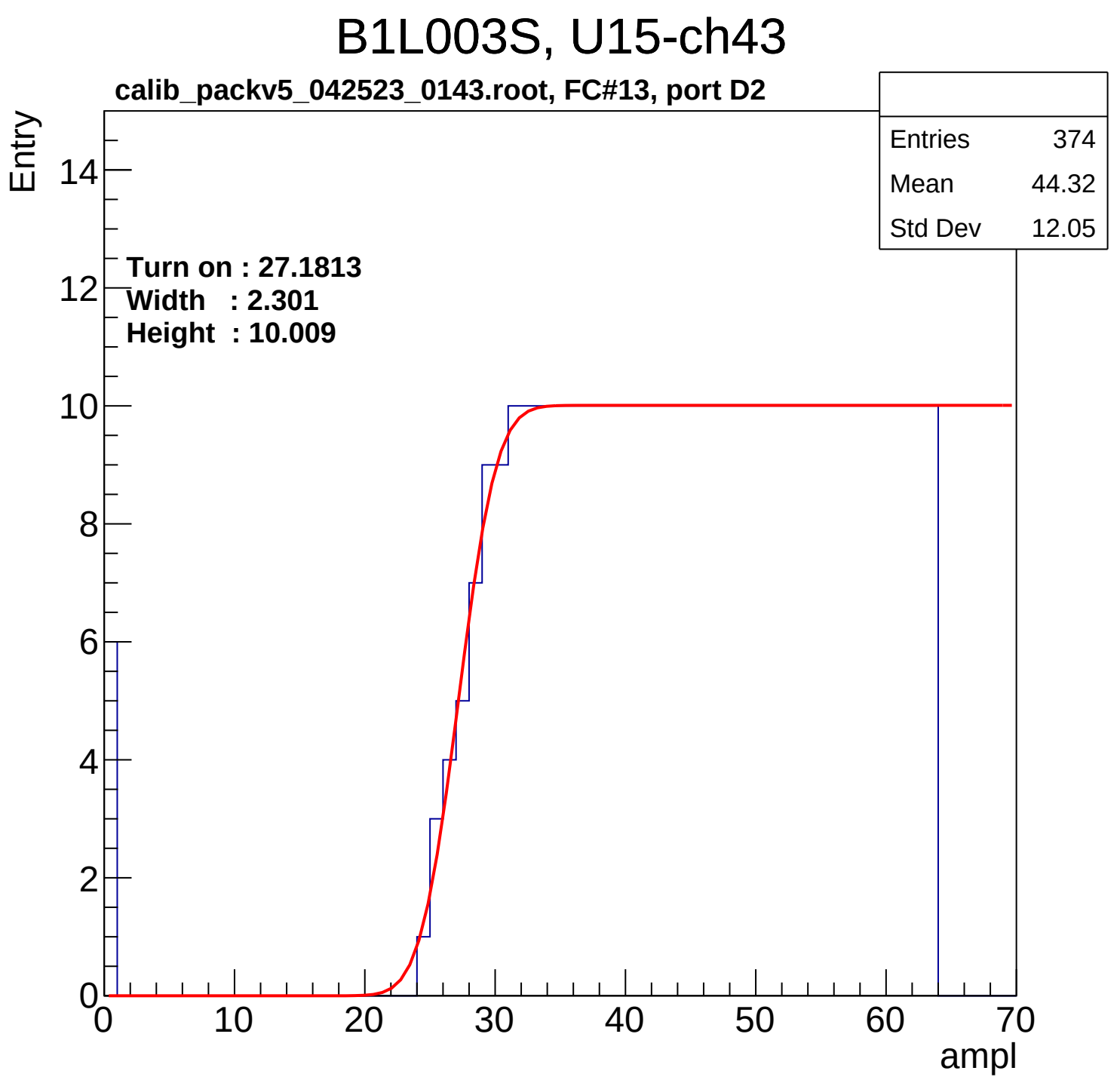
B1L003S, U15-ch43
calib_packv5_042523_0143.root, FC#13, port D2
Entries 374
Mean 44.32
Std Dev 12.05
Turn on : 27.1813
Width : 2.301
Height : 10.009
Entry
ampl
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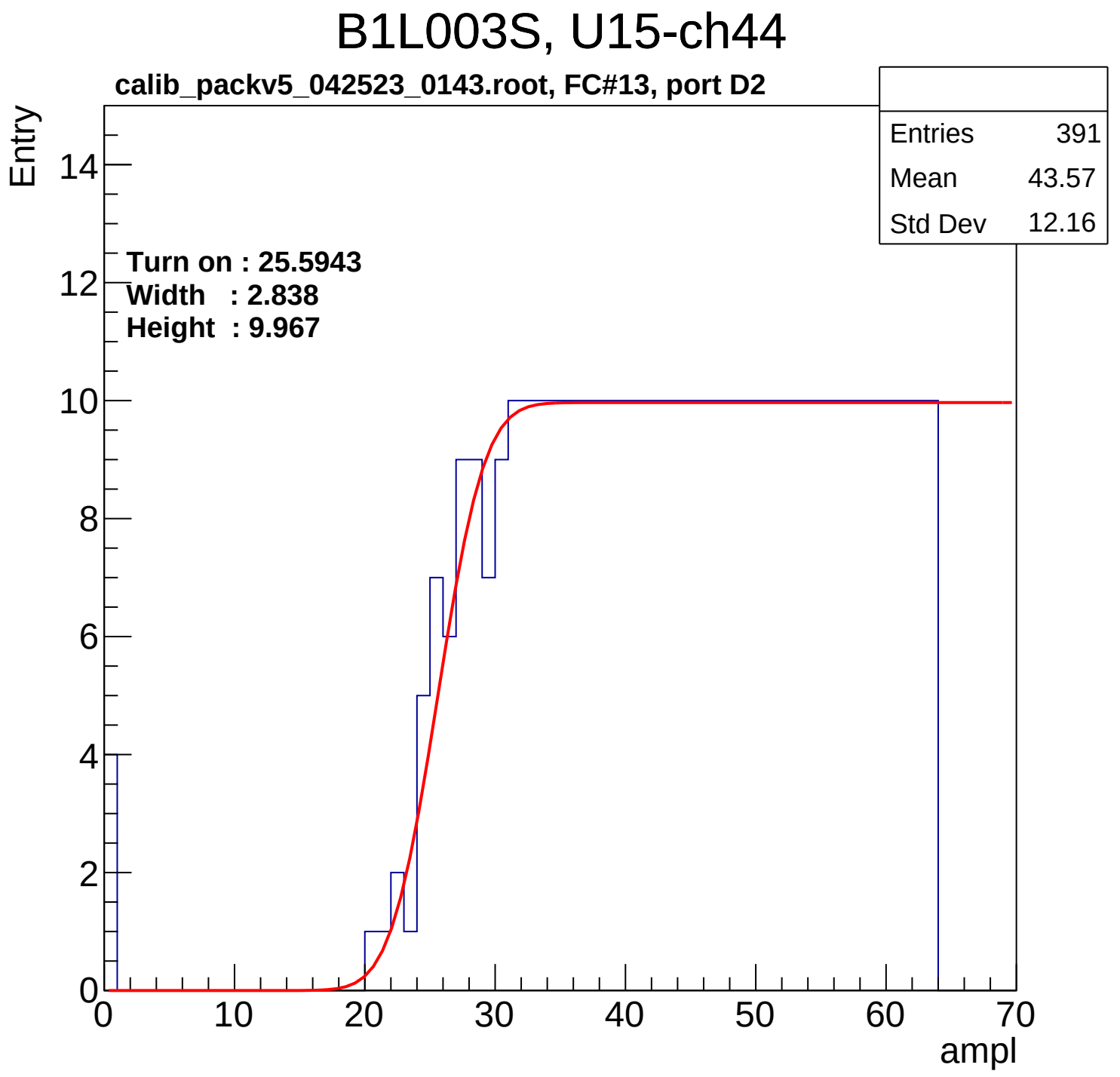
B1L003S, U15-ch44
calib_packv5_042523_0143.root, FC#13, port D2
Entries 391
Mean 43.57
Std Dev 12.16
Turn on : 25.5943
Width : 2.838
Height : 9.967
Entry
ampl
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6
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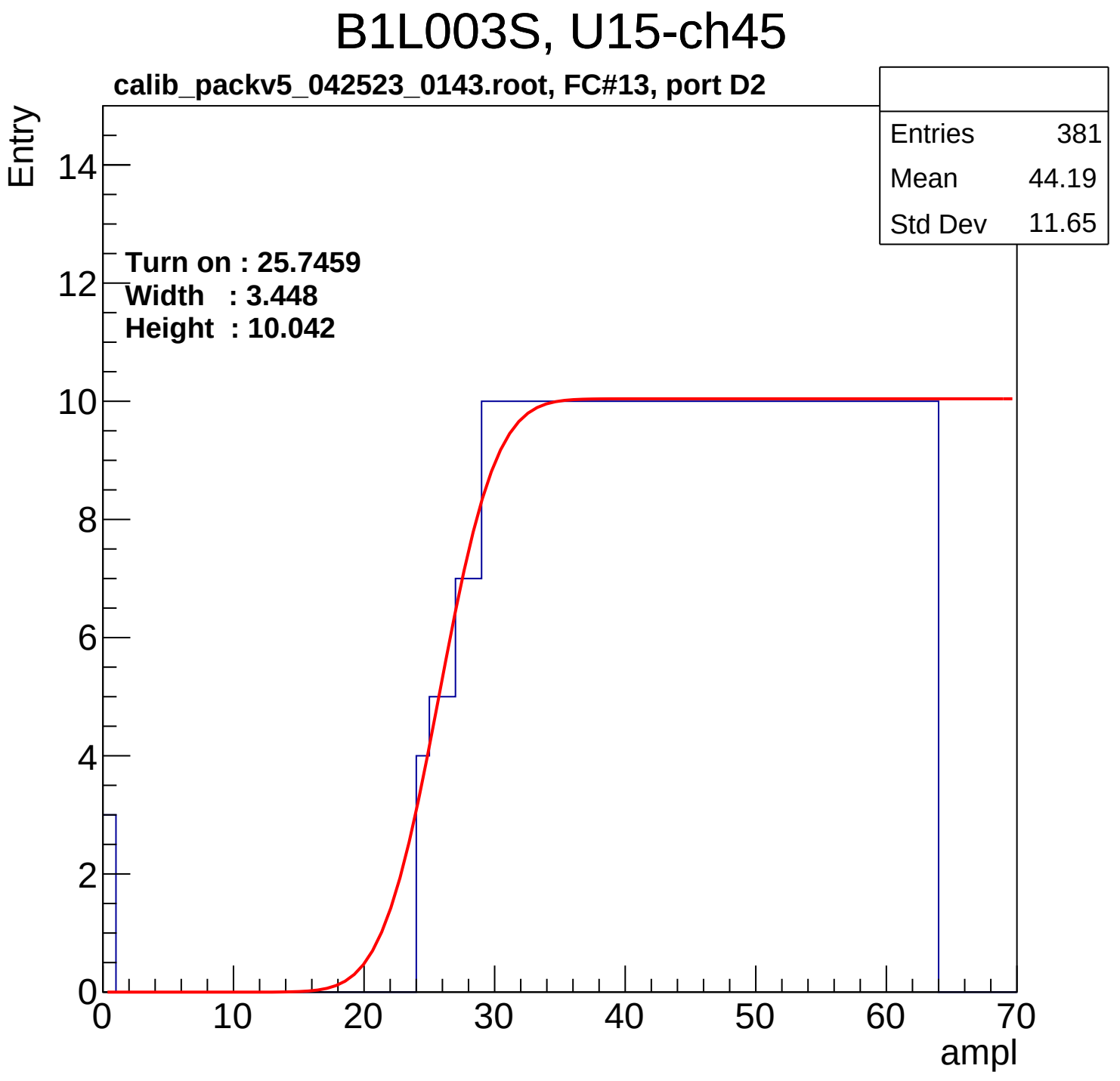
B1L003S, U15-ch45
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 44.19
Std Dev 11.65
Turn on : 25.7459
Width : 3.448
Height : 10.042
Entry
ampl
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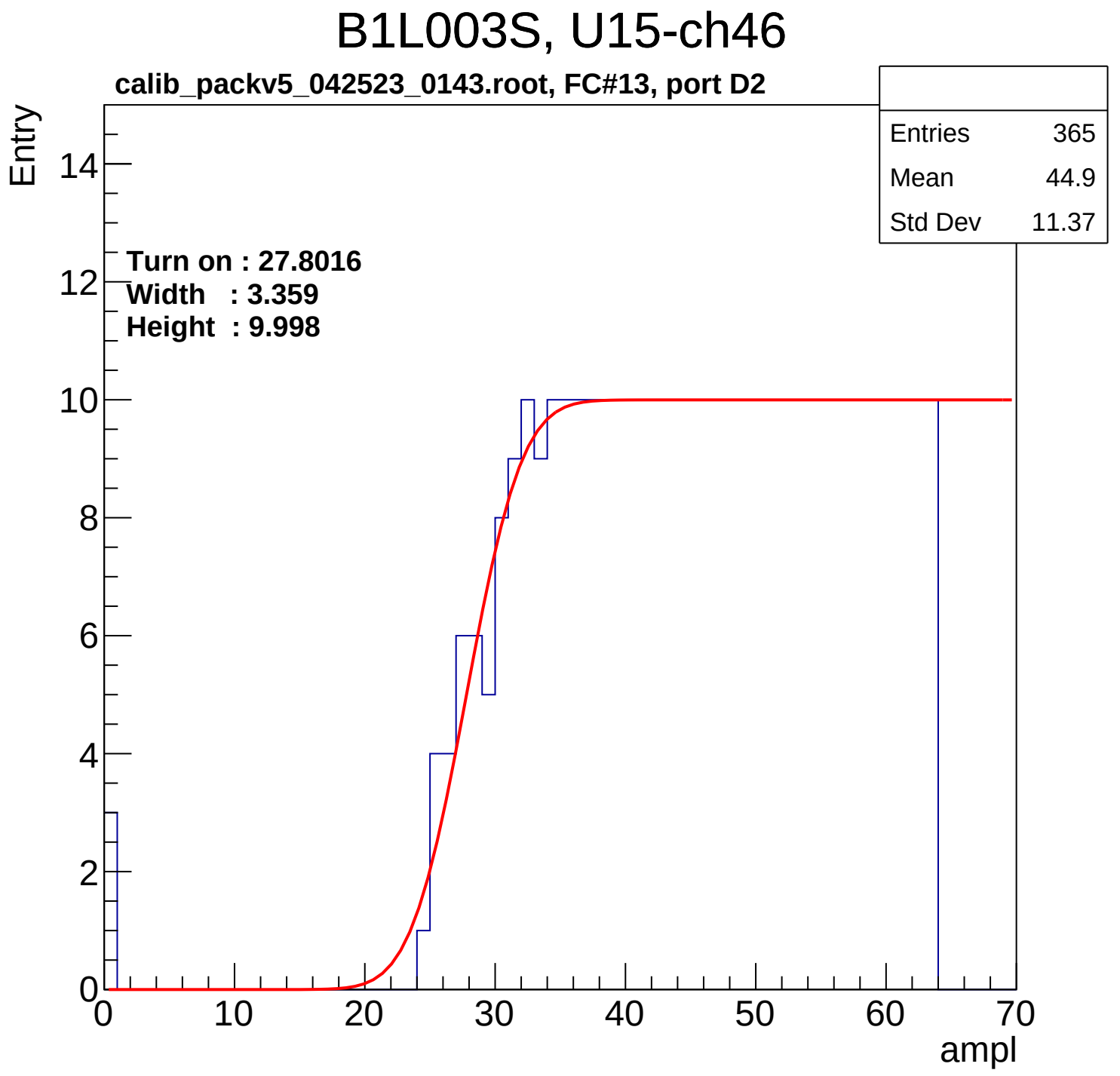
B1L003S, U15-ch46
calib_packv5_042523_0143.root, FC#13, port D2
Entries 365
Mean 44.9
Std Dev 11.37
Turn on : 27.8016
Width : 3.359
Height : 9.998
Entry
ampl
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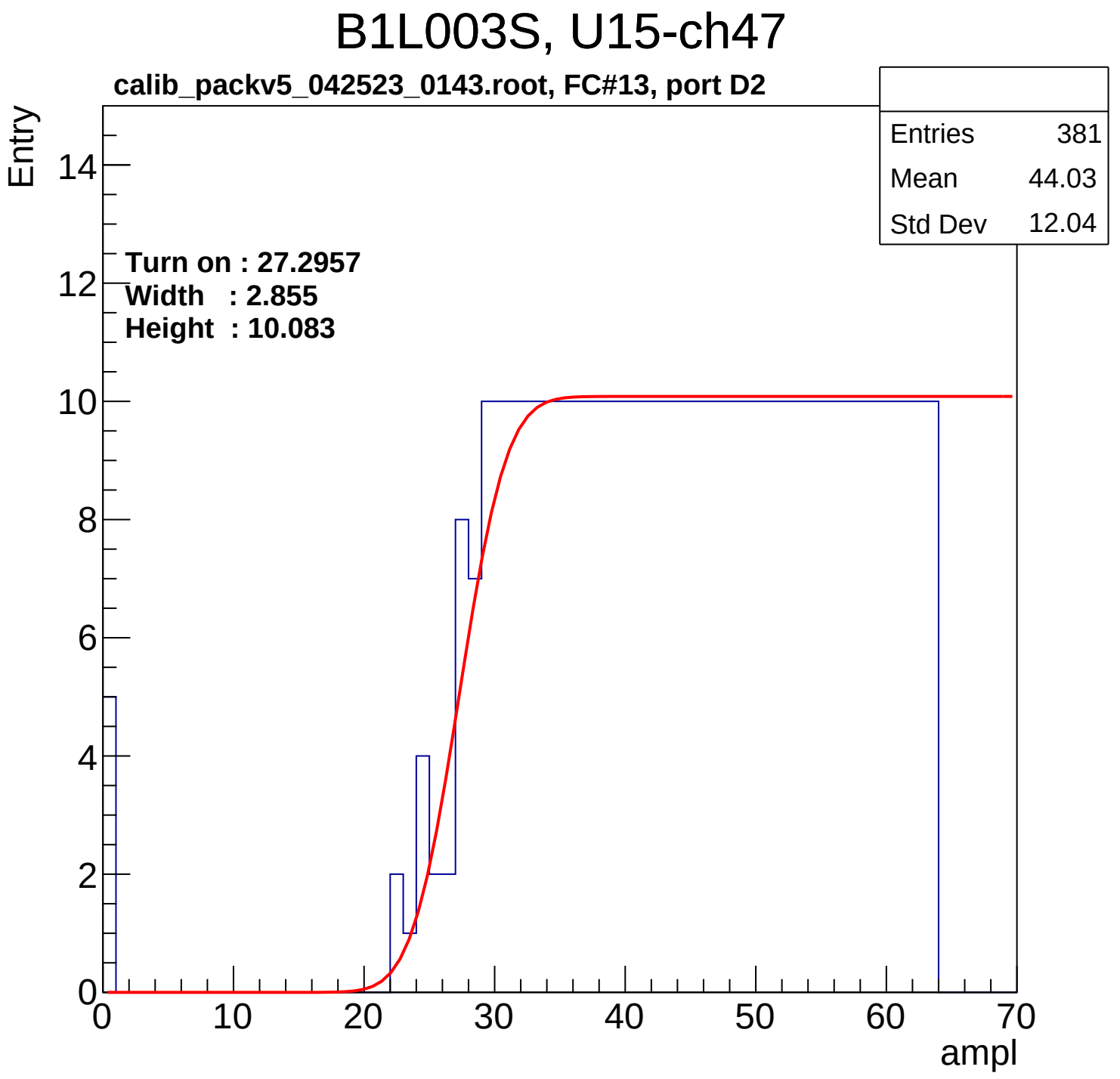
B1L003S, U15-ch47
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 44.03
Std Dev 12.04
Turn on : 27.2957
Width : 2.855
Height : 10.083
Entry
ampl
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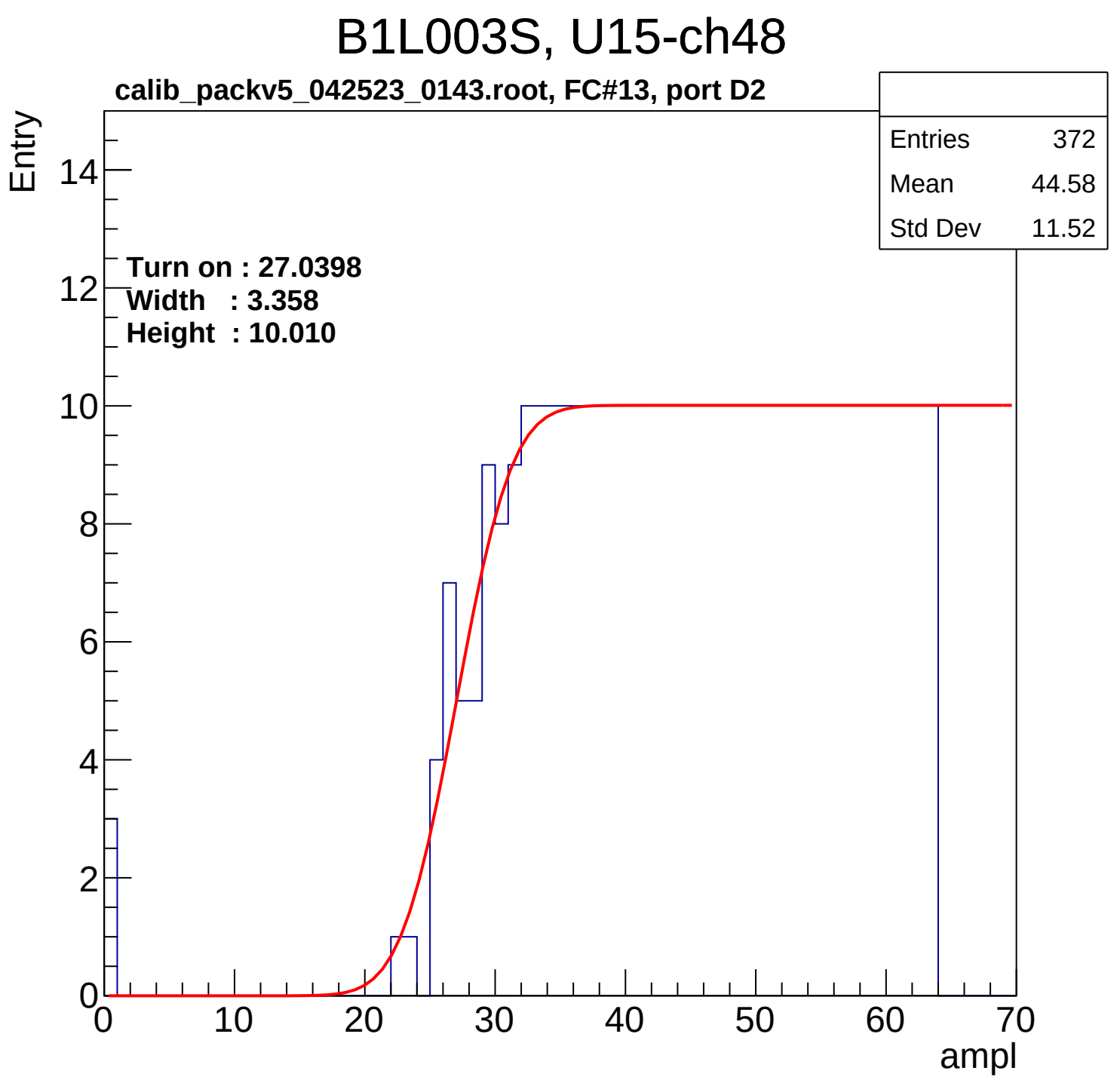
B1L003S, U15-ch48
calib_packv5_042523_0143.root, FC#13, port D2
Entries 372
Mean 44.58
Std Dev 11.52
Turn on : 27.0398
Width : 3.358
Height : 10.010
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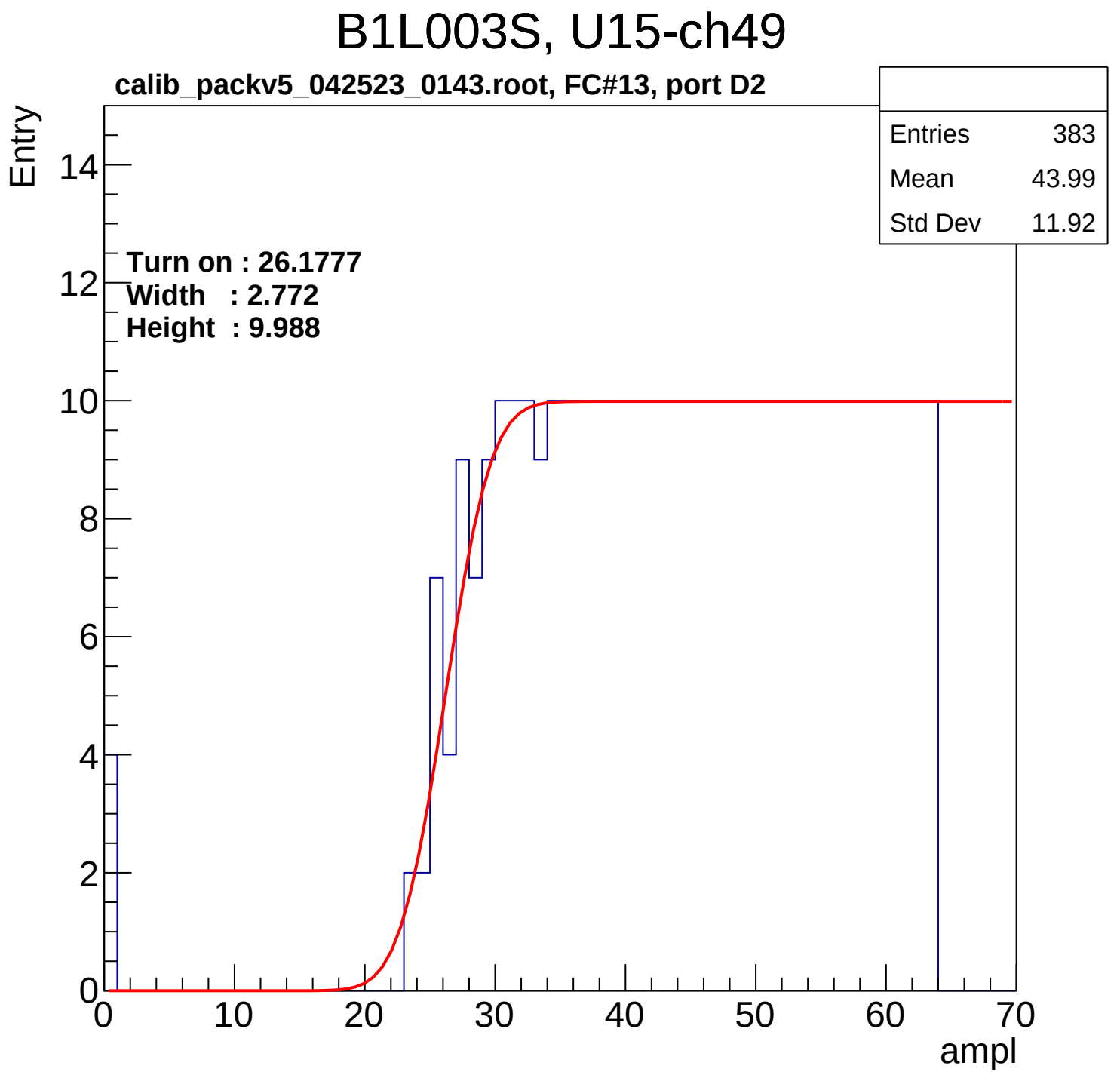
B1L003S, U15-ch49
calib_packv5_042523_0143.root, FC#13, port D2
Entries 383
Mean 43.99
Std Dev 11.92
Turn on : 26.1777
Width : 2.772
Height : 9.988
Entry
ampl
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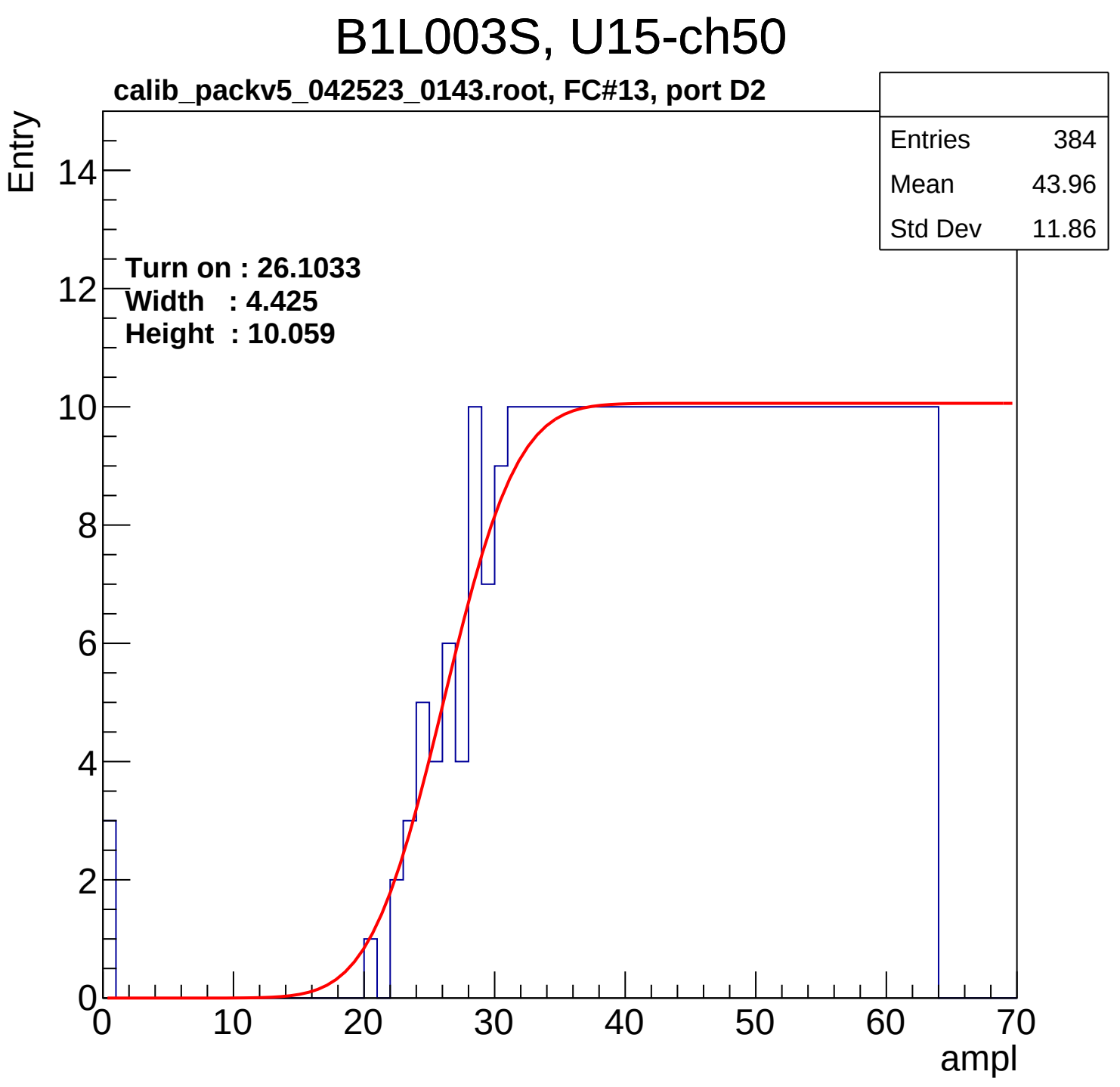
B1L003S, U15-ch50
calib_packv5_042523_0143.root, FC#13, port D2
Entries 384
Mean 43.96
Std Dev 11.86
Turn on : 26.1033
Width : 4.425
Height : 10.059
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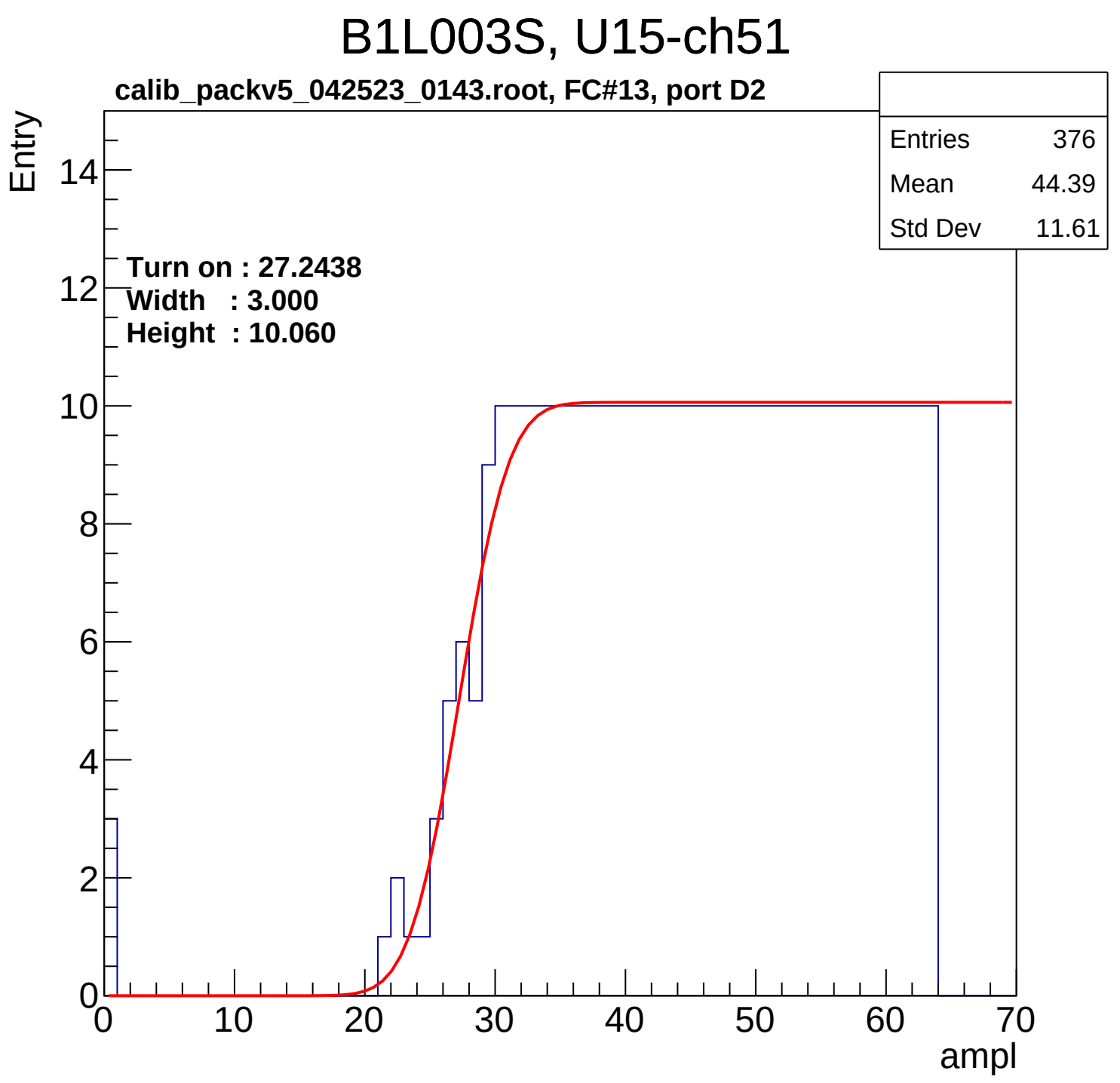
B1L003S, U15-ch51
calib_packv5_042523_0143.root, FC#13, port D2
Entries 376
Mean 44.39
Std Dev 11.61
Turn on : 27.2438
Width : 3.000
Height : 10.060
Entry
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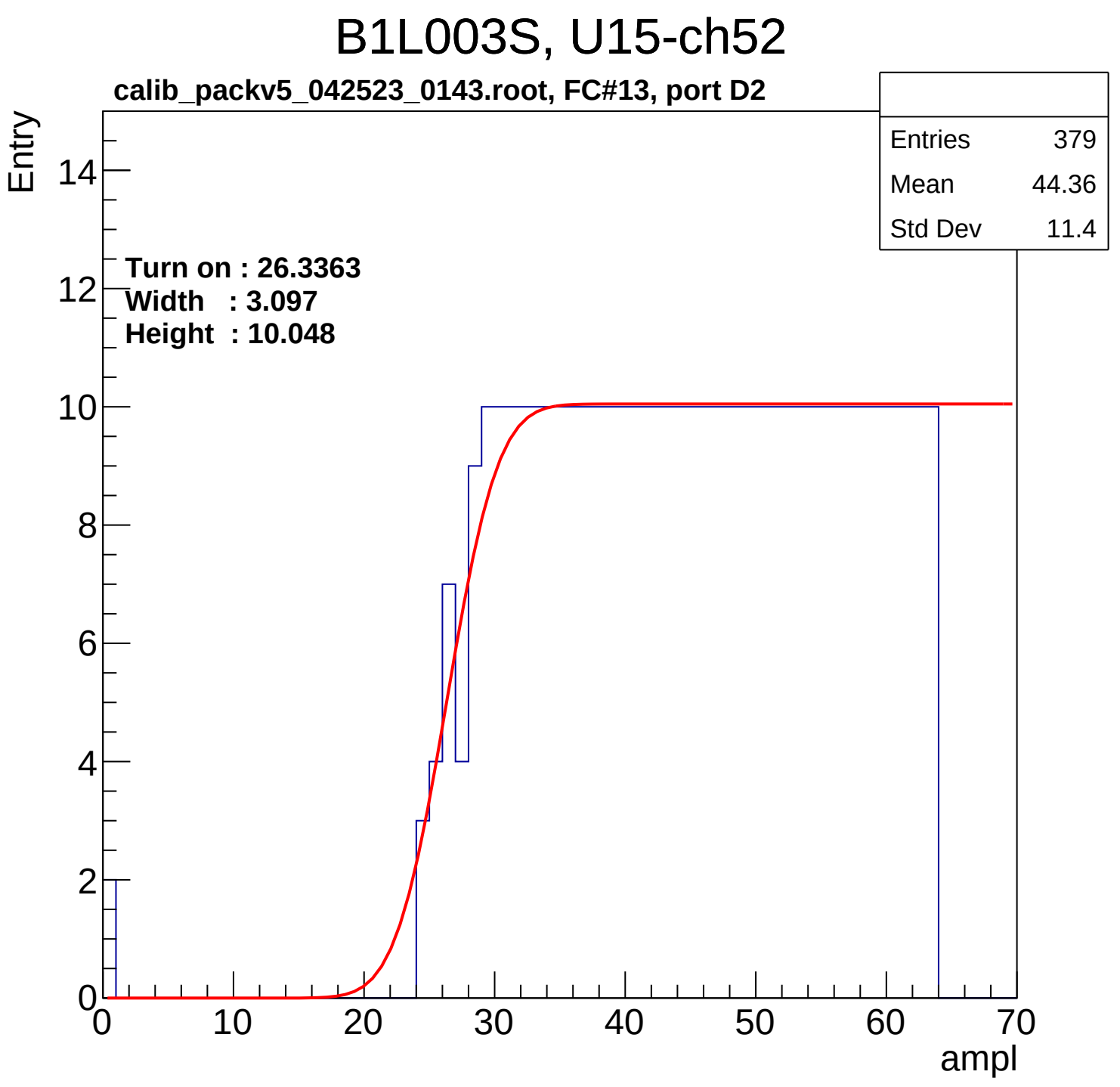
B1L003S, U15-ch52
calib_packv5_042523_0143.root, FC#13, port D2
Entries 379
Mean 44.36
Std Dev 11.4
Turn on : 26.3363
Width : 3.097
Height : 10.048
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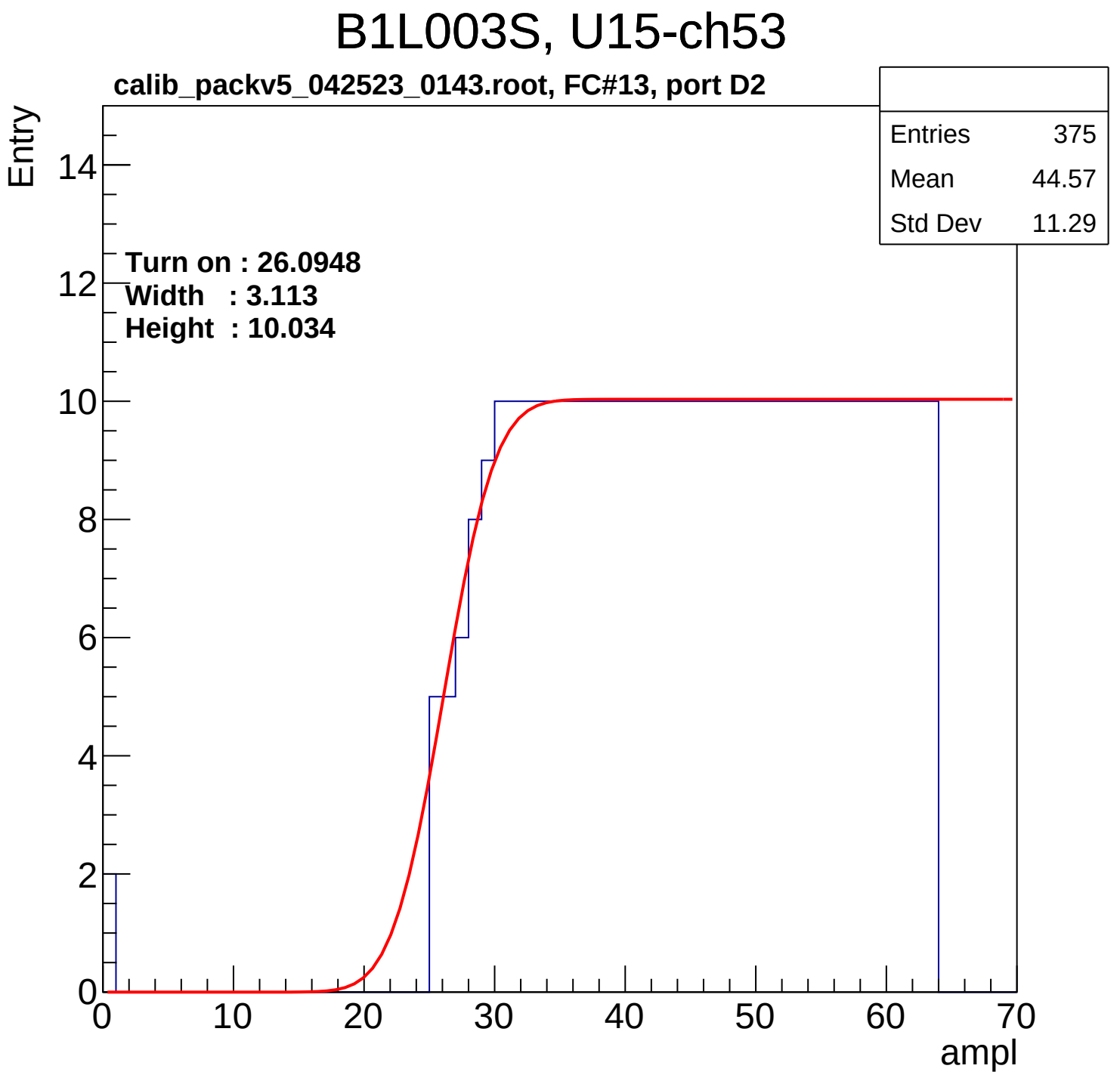
B1L003S, U15-ch53
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.57
Std Dev 11.29
Turn on : 26.0948
Width : 3.113
Height : 10.034
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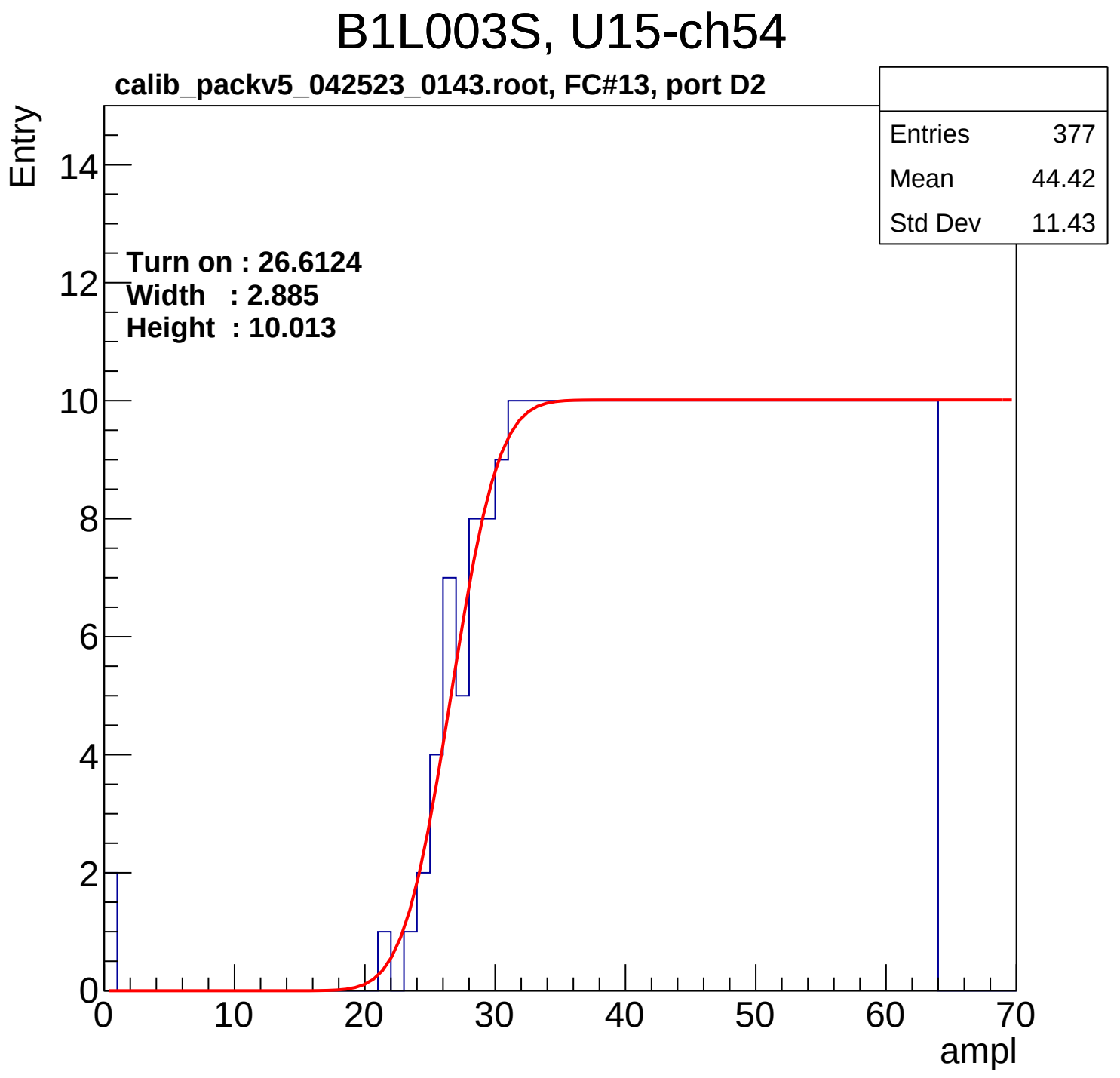
B1L003S, U15-ch54
calib_packv5_042523_0143.root, FC#13, port D2
Entries 377
Mean 44.42
Std Dev 11.43
Turn on : 26.6124
Width : 2.885
Height : 10.013
Entry
ampl
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6
8
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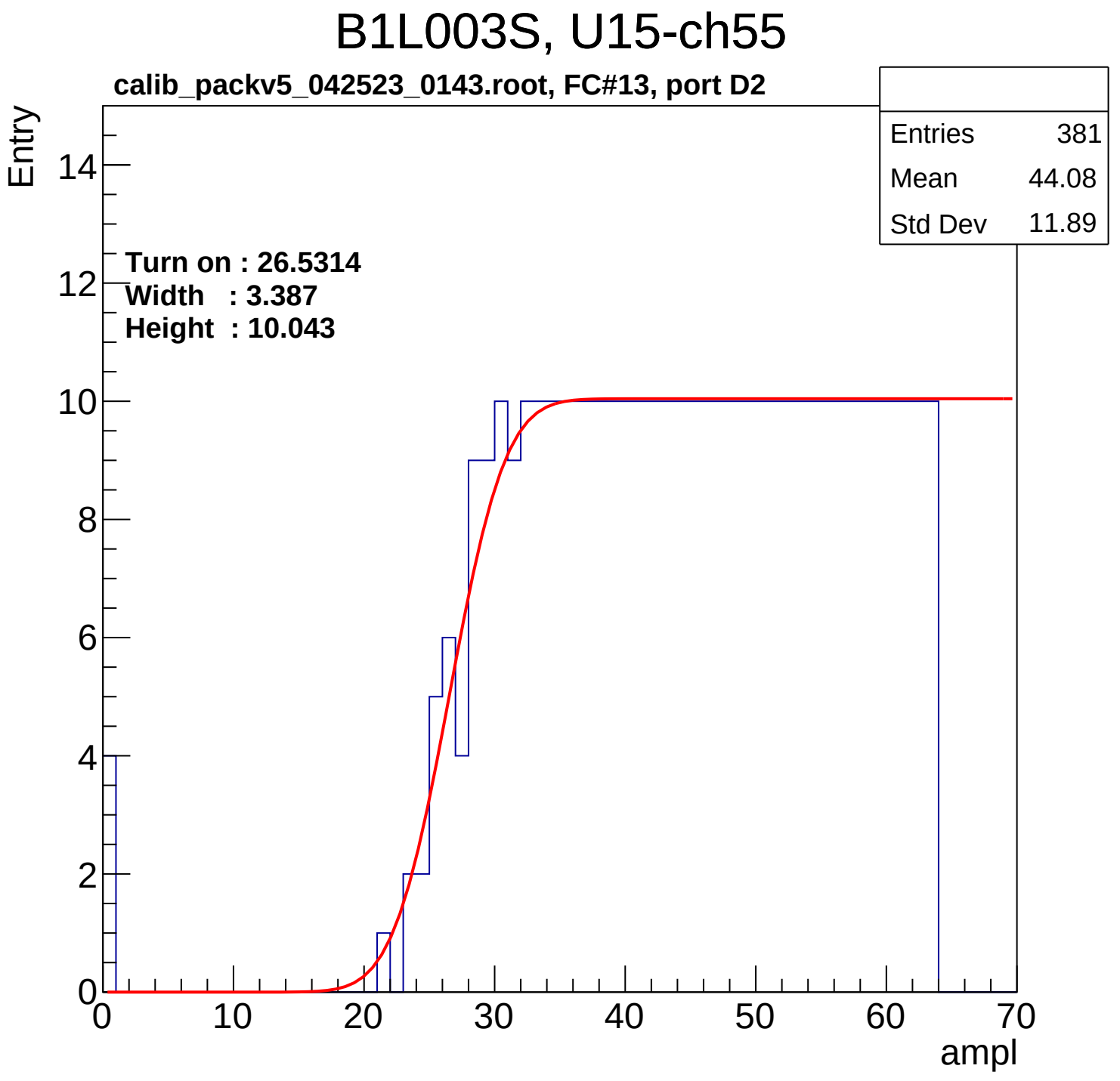
B1L003S, U15-ch55
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 44.08
Std Dev 11.89
Turn on : 26.5314
Width : 3.387
Height : 10.043
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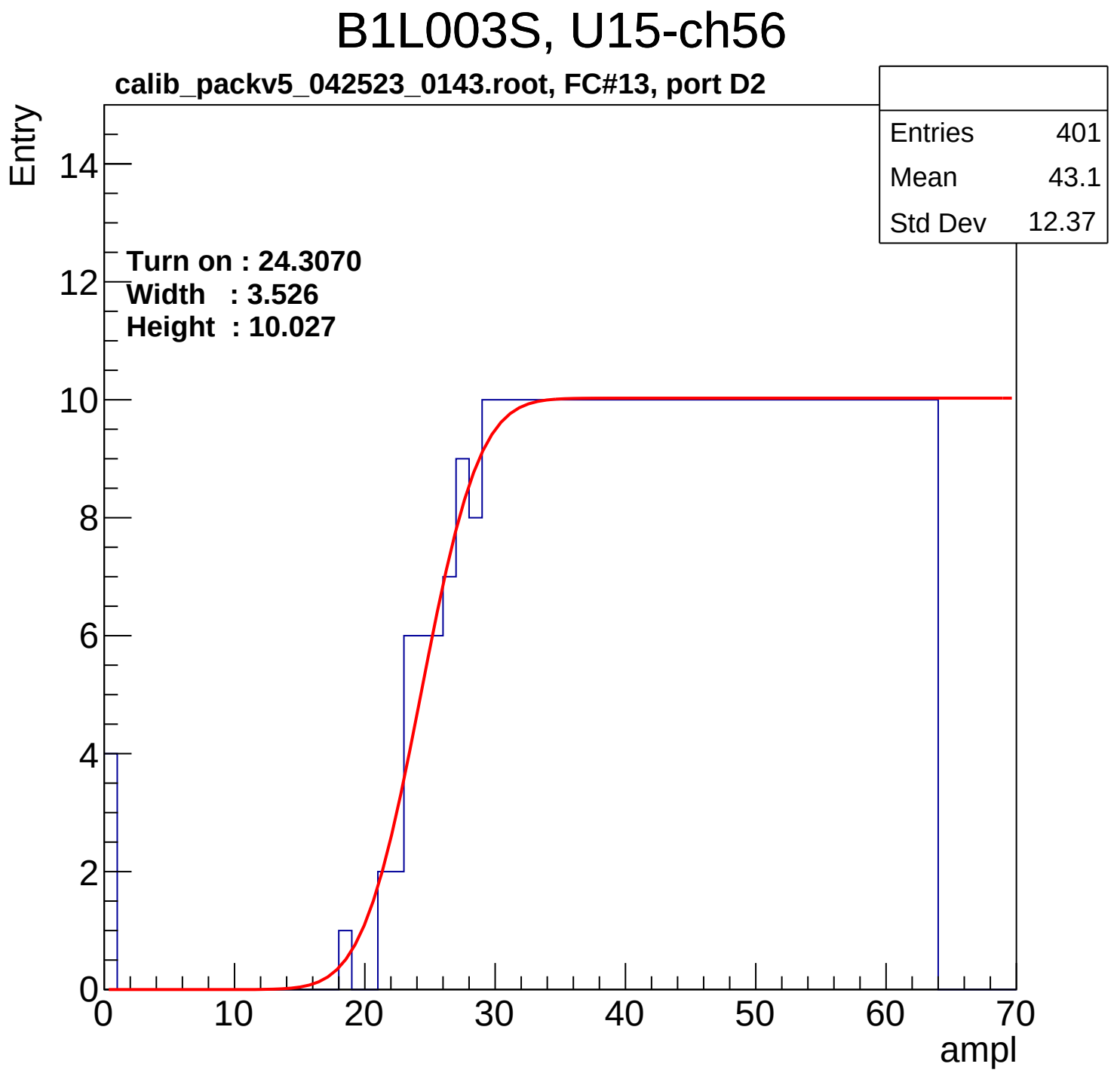
B1L003S, U15-ch56
calib_packv5_042523_0143.root, FC#13, port D2
Entries 401
Mean 43.1
Std Dev 12.37
Turn on : 24.3070
Width : 3.526
Height : 10.027
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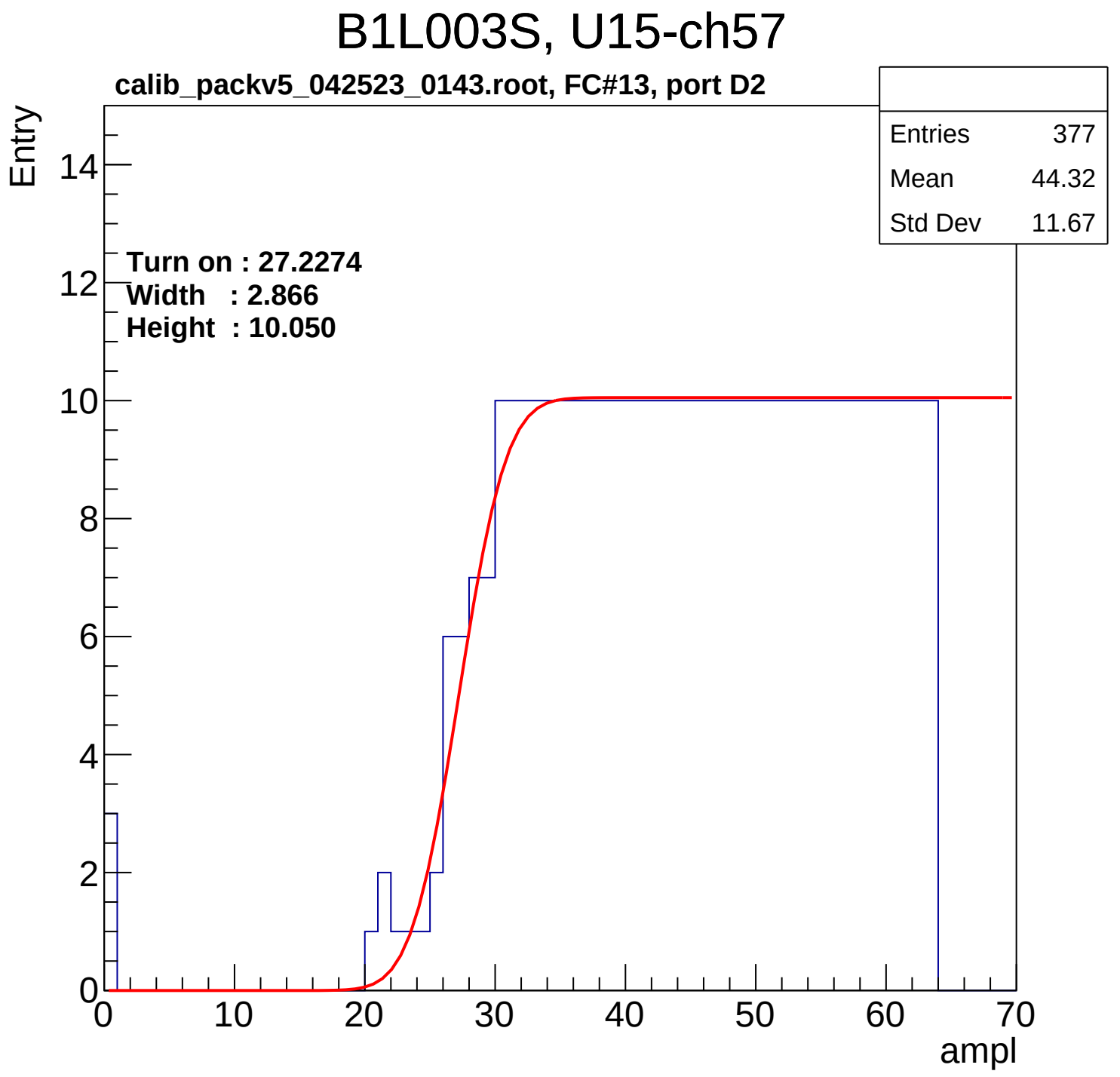
B1L003S, U15-ch57
calib_packv5_042523_0143.root, FC#13, port D2
Entries 377
Mean 44.32
Std Dev 11.67
Turn on : 27.2274
Width : 2.866
Height : 10.050
Entry
ampl
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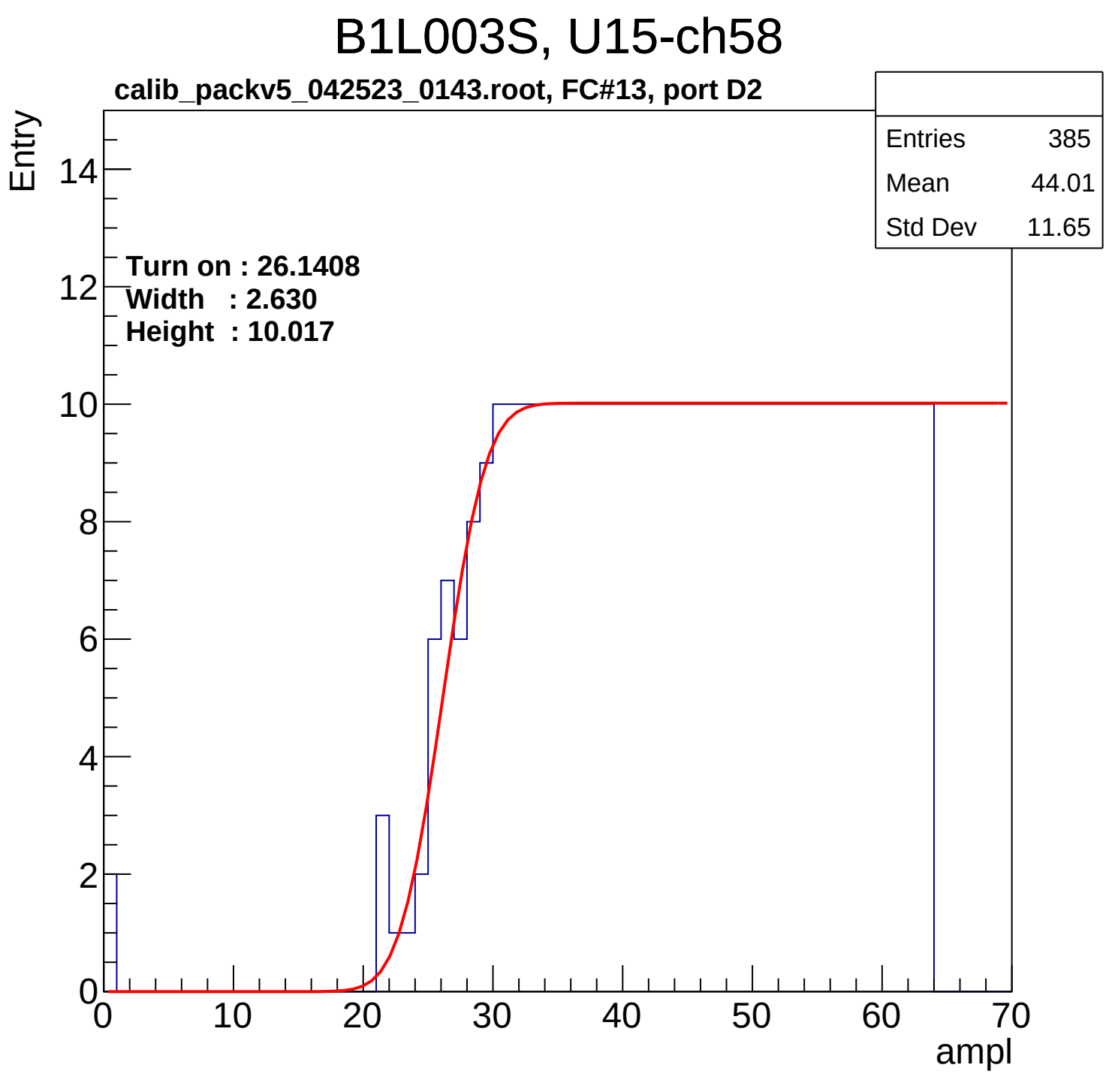
B1L003S, U15-ch58
calib_packv5_042523_0143.root, FC#13, port D2
Entries 385
Mean 44.01
Std Dev 11.65
Turn on : 26.1408
Width : 2.630
Height : 10.017
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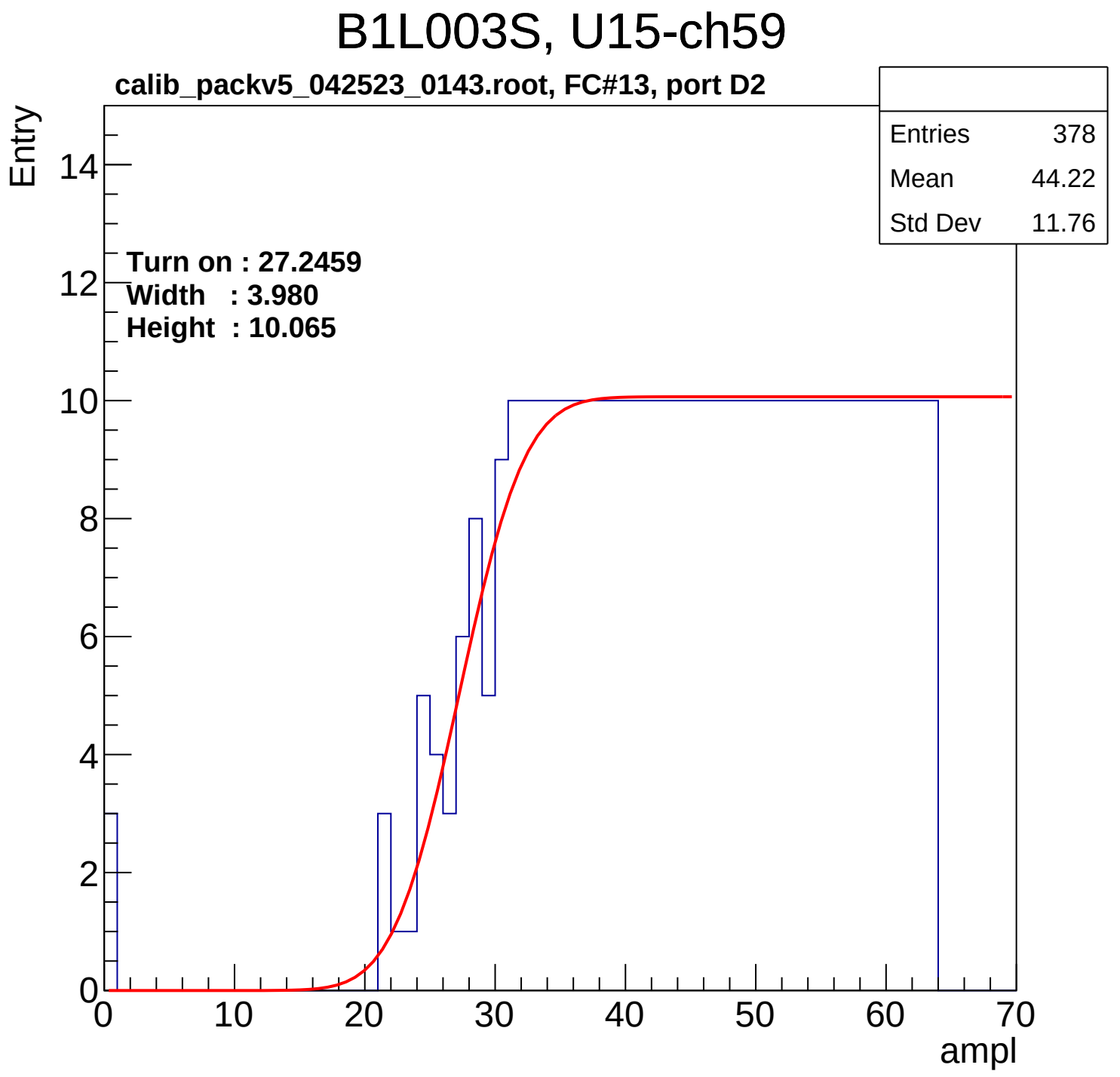
B1L003S, U15-ch59
calib_packv5_042523_0143.root, FC#13, port D2
Entries 378
Mean 44.22
Std Dev 11.76
Turn on : 27.2459
Width : 3.980
Height : 10.065
Entry
ampl
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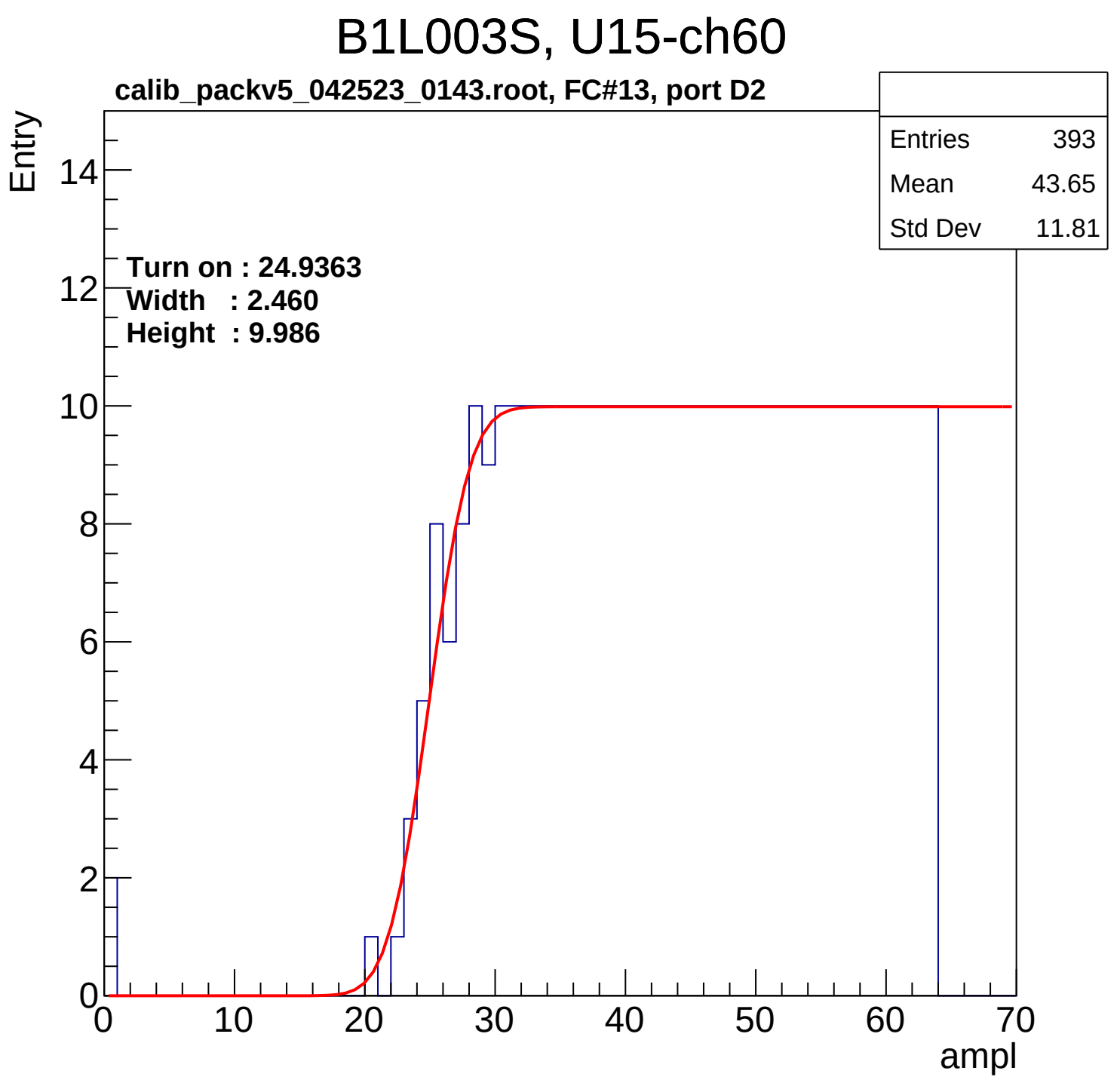
B1L003S, U15-ch60
calib_packv5_042523_0143.root, FC#13, port D2
Entries 393
Mean 43.65
Std Dev 11.81
Turn on : 24.9363
Width : 2.460
Height : 9.986
Entry
ampl
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2
4
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8
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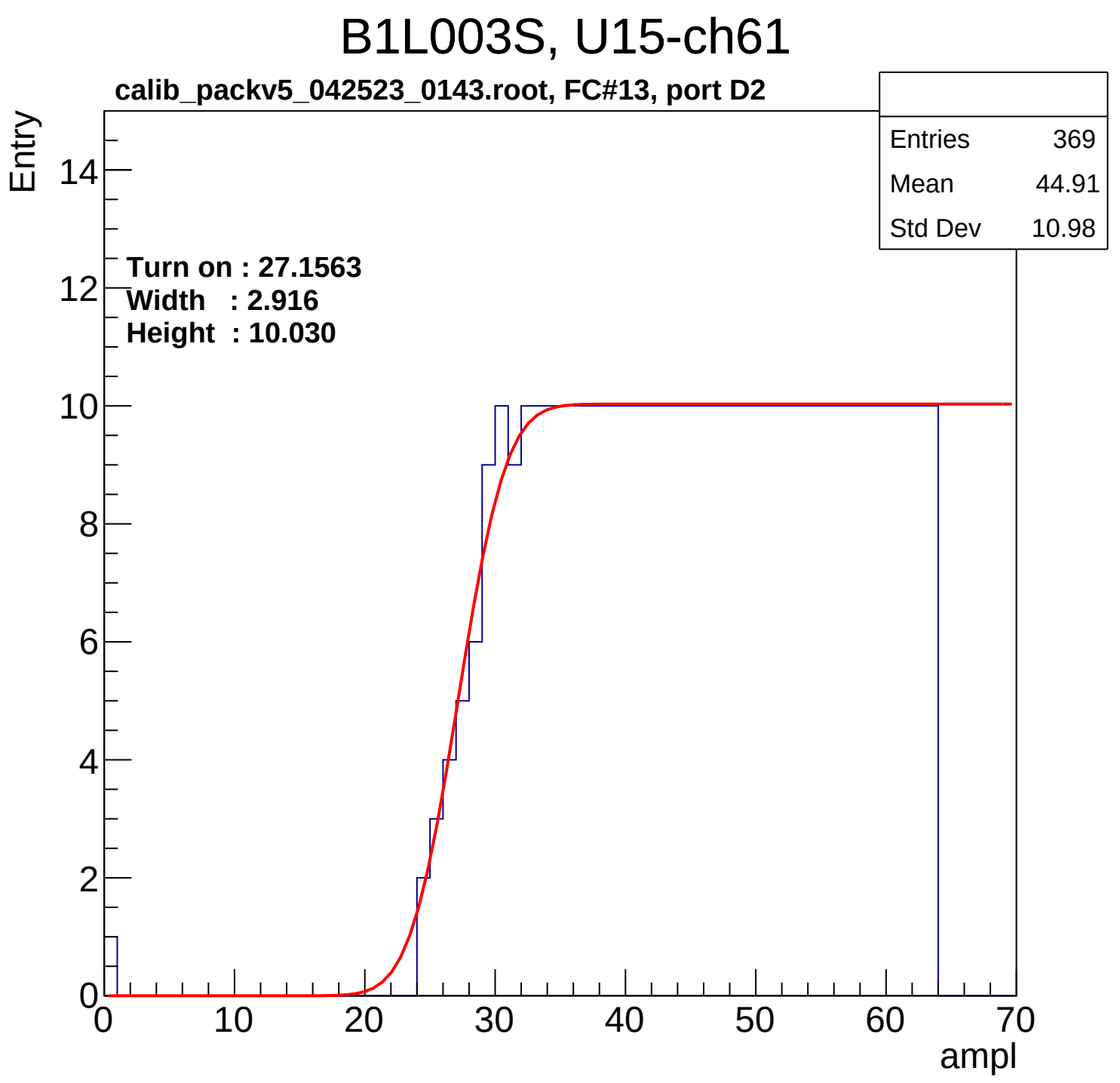
B1L003S, U15-ch61
calib_packv5_042523_0143.root, FC#13, port D2
Entries 369
Mean 44.91
Std Dev 10.98
Turn on : 27.1563
Width : 2.916
Height : 10.030
Entry
ampl
0
2
4
6
8
10
12
14
0
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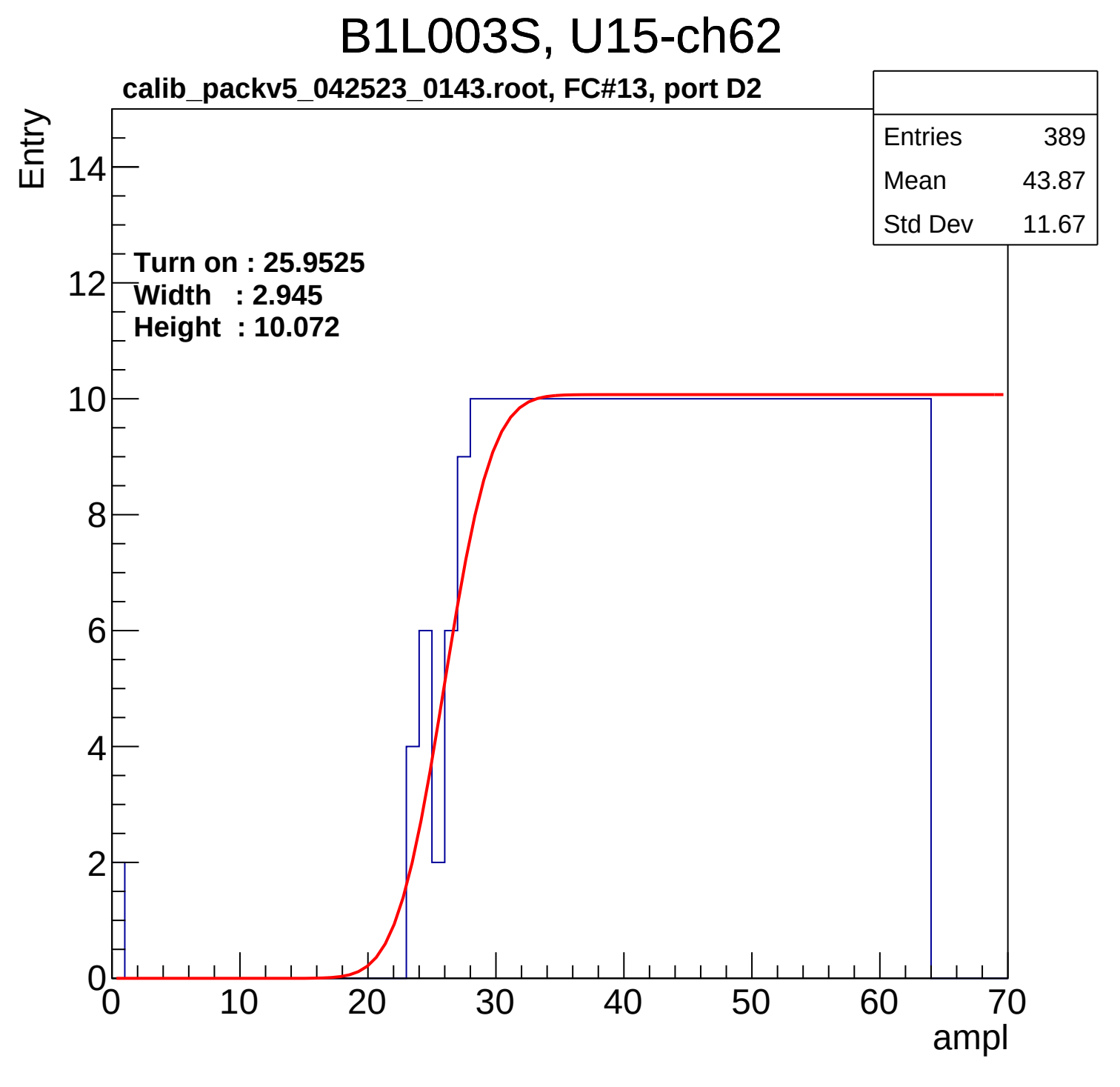
B1L003S, U15-ch62
calib_packv5_042523_0143.root, FC#13, port D2
Entries 389
Mean 43.87
Std Dev 11.67
Turn on : 25.9525
Width : 2.945
Height : 10.072
Entry
ampl
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2
4
6
8
10
12
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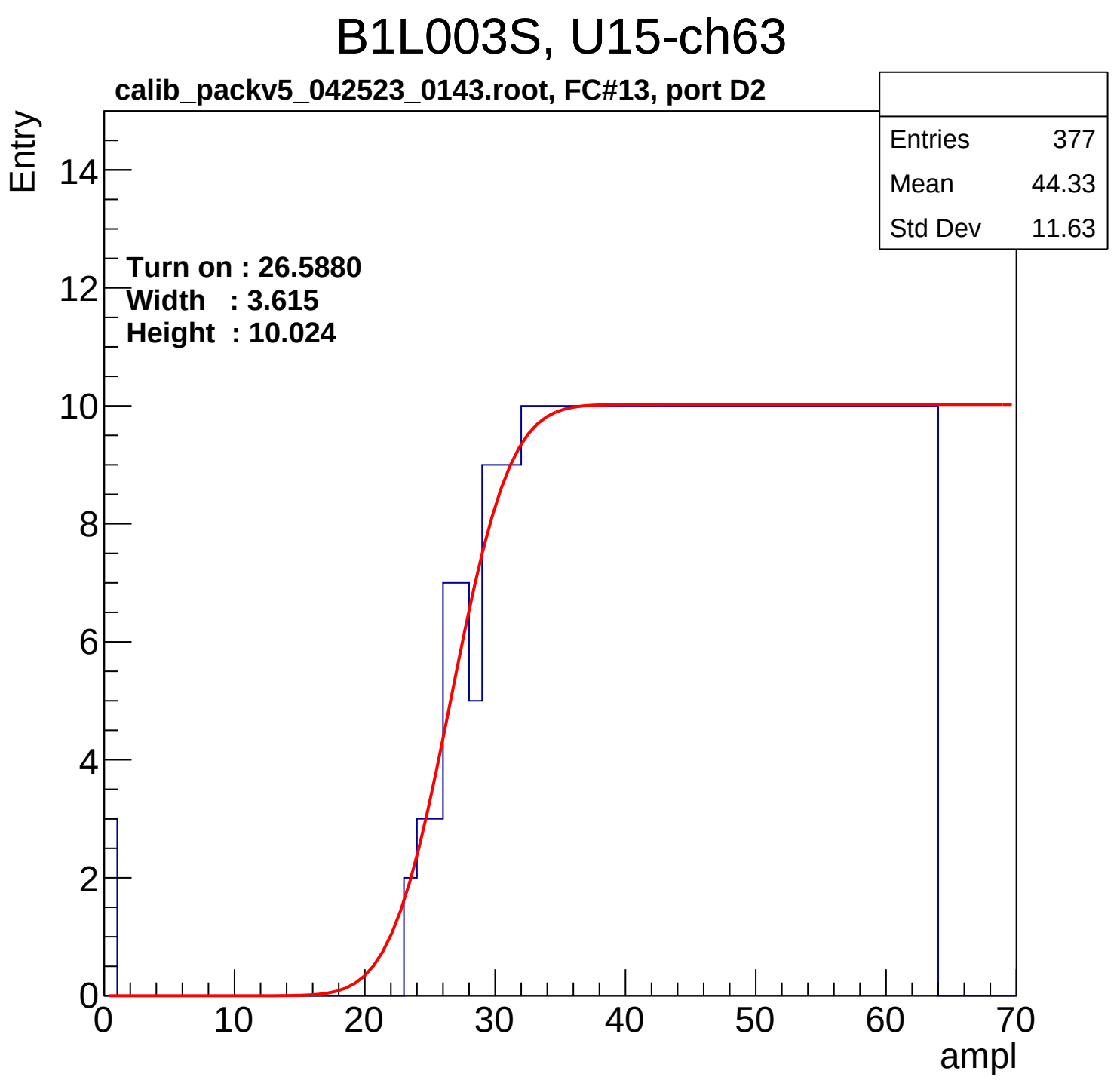
B1L003S, U15-ch63
calib_packv5_042523_0143.root, FC#13, port D2
Entries 377
Mean 44.33
Std Dev 11.63
Turn on : 26.5880
Width : 3.615
Height : 10.024
Entry
ampl
0
2
4
6
8
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12
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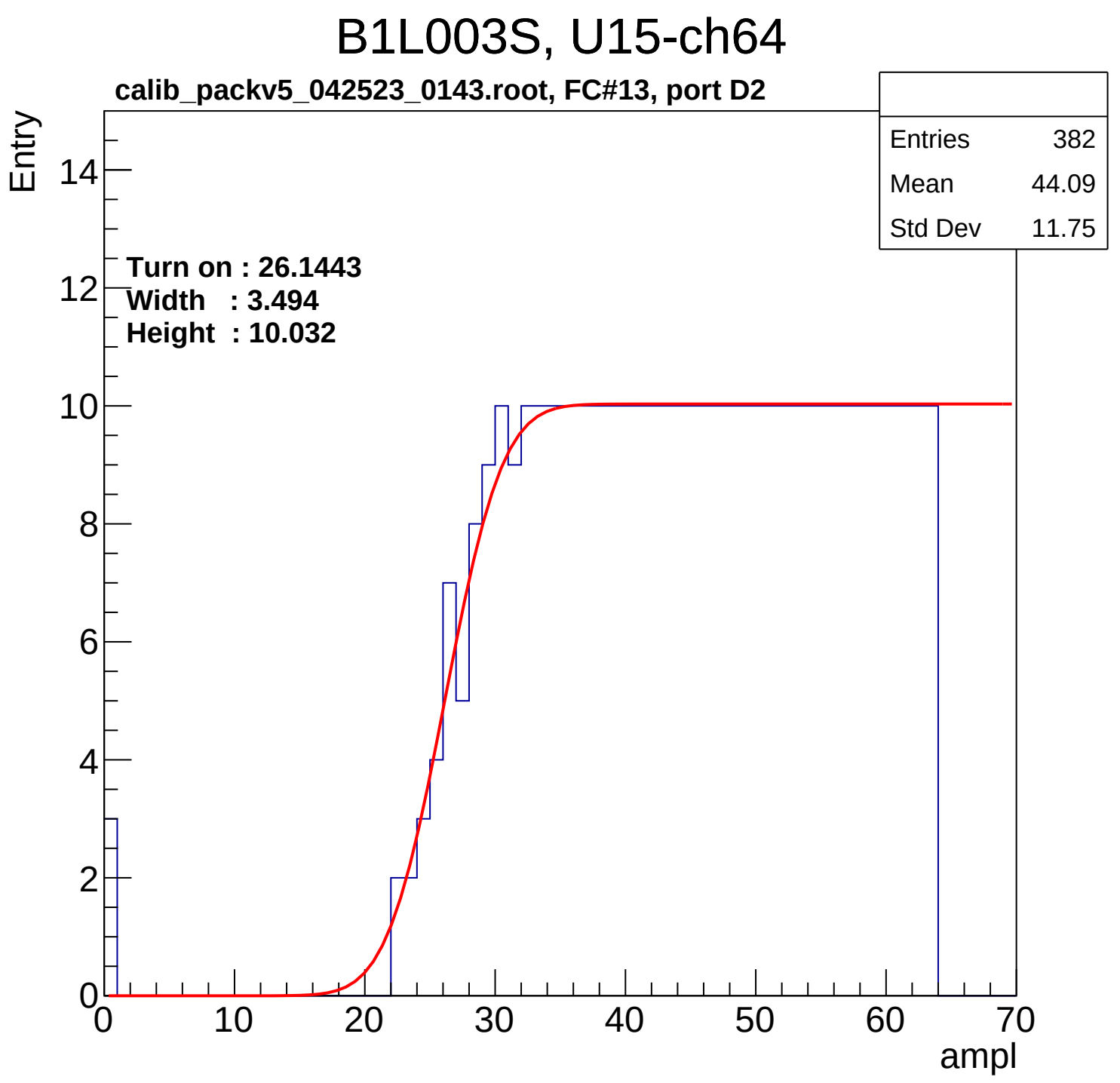
B1L003S, U15-ch64
calib_packv5_042523_0143.root, FC#13, port D2
Entries 382
Mean 44.09
Std Dev 11.75
Turn on : 26.1443
Width : 3.494
Height : 10.032
Entry
ampl
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6
8
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12
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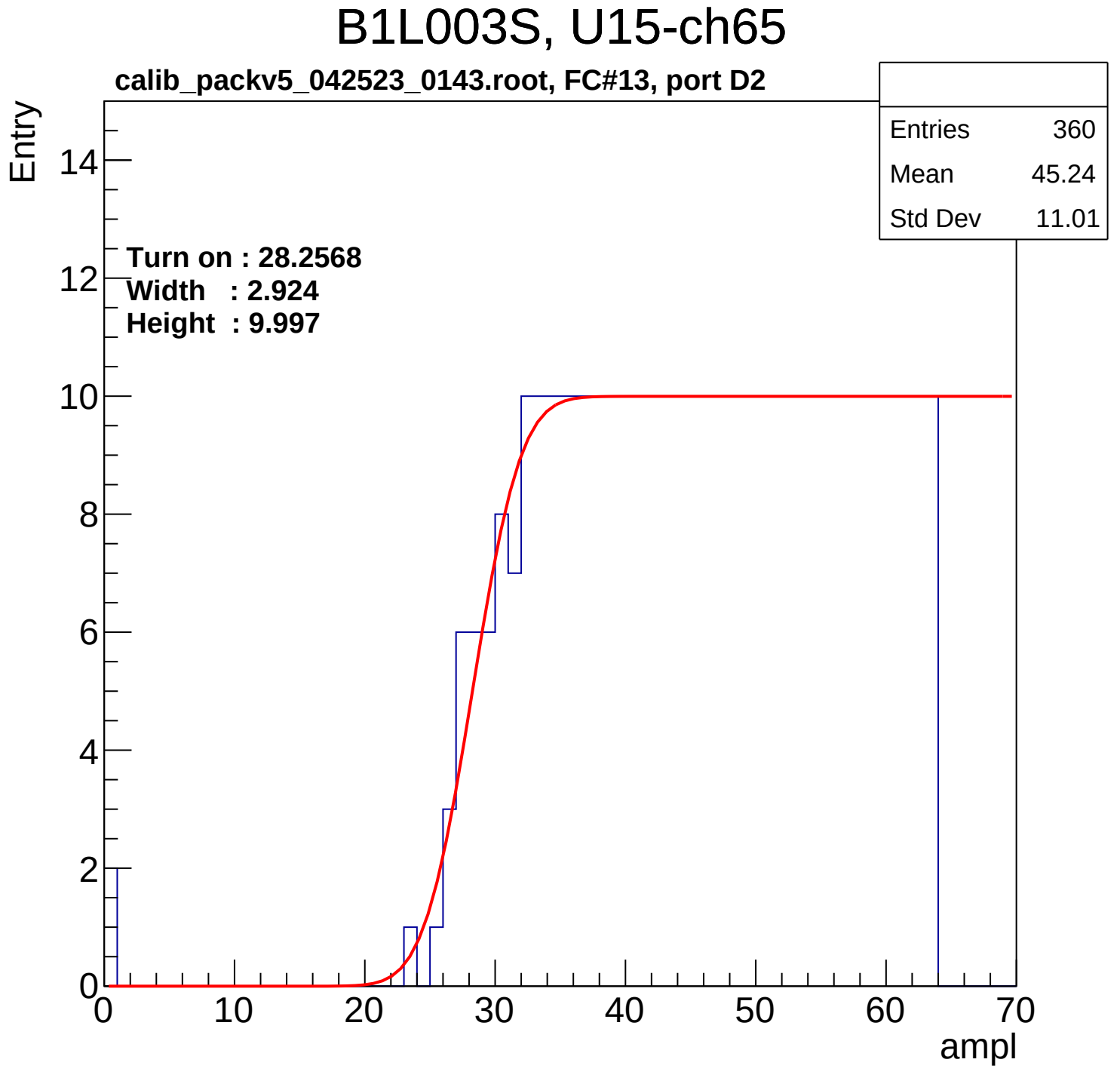
B1L003S, U15-ch65
calib_packv5_042523_0143.root, FC#13, port D2
Entries 360
Mean 45.24
Std Dev 11.01
Turn on : 28.2568
Width : 2.924
Height : 9.997
Entry
ampl
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2
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6
8
10
12
14
0
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20
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40
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60
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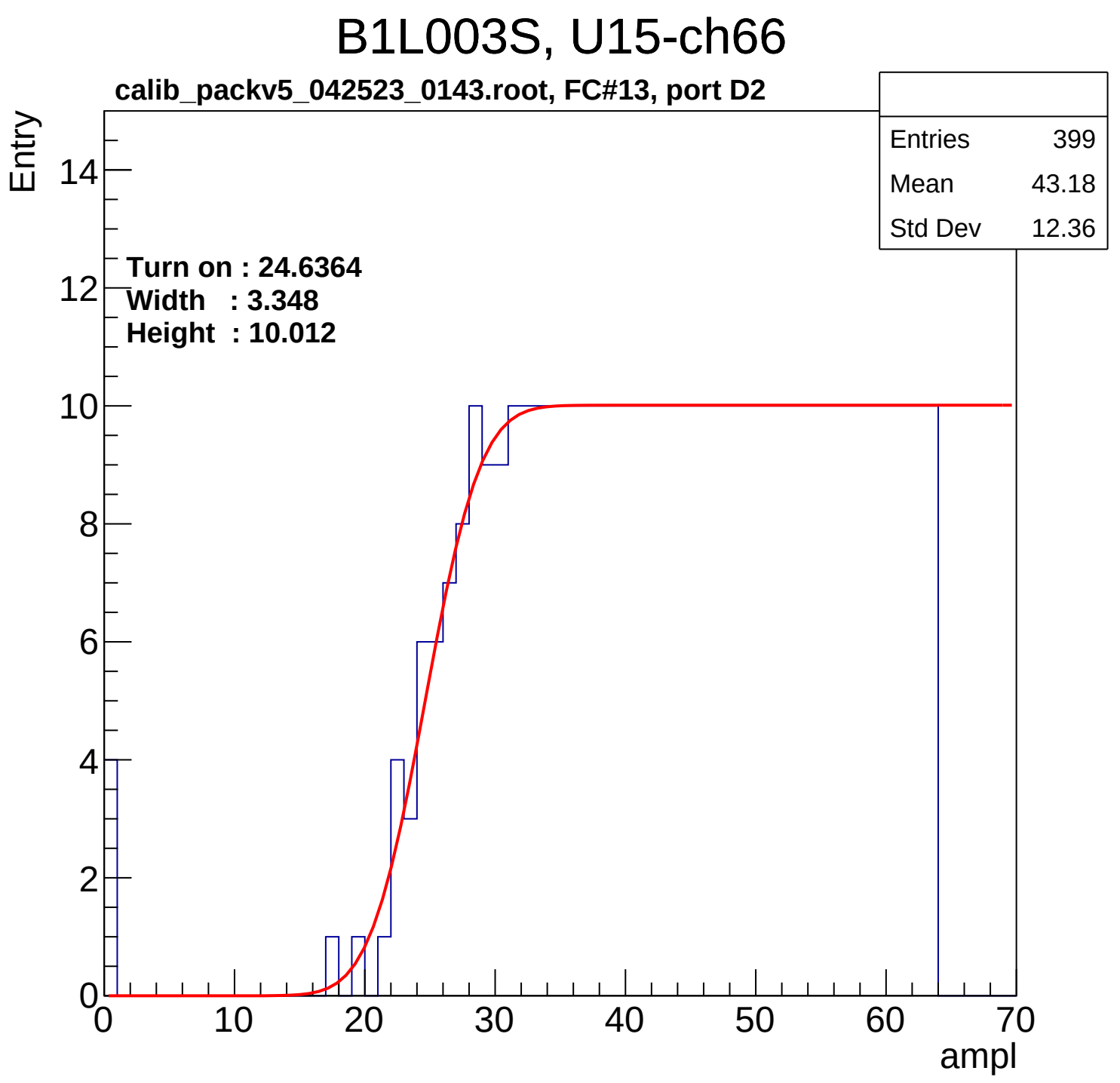
B1L003S, U15-ch66
calib_packv5_042523_0143.root, FC#13, port D2
Entries 399
Mean 43.18
Std Dev 12.36
Turn on : 24.6364
Width : 3.348
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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60
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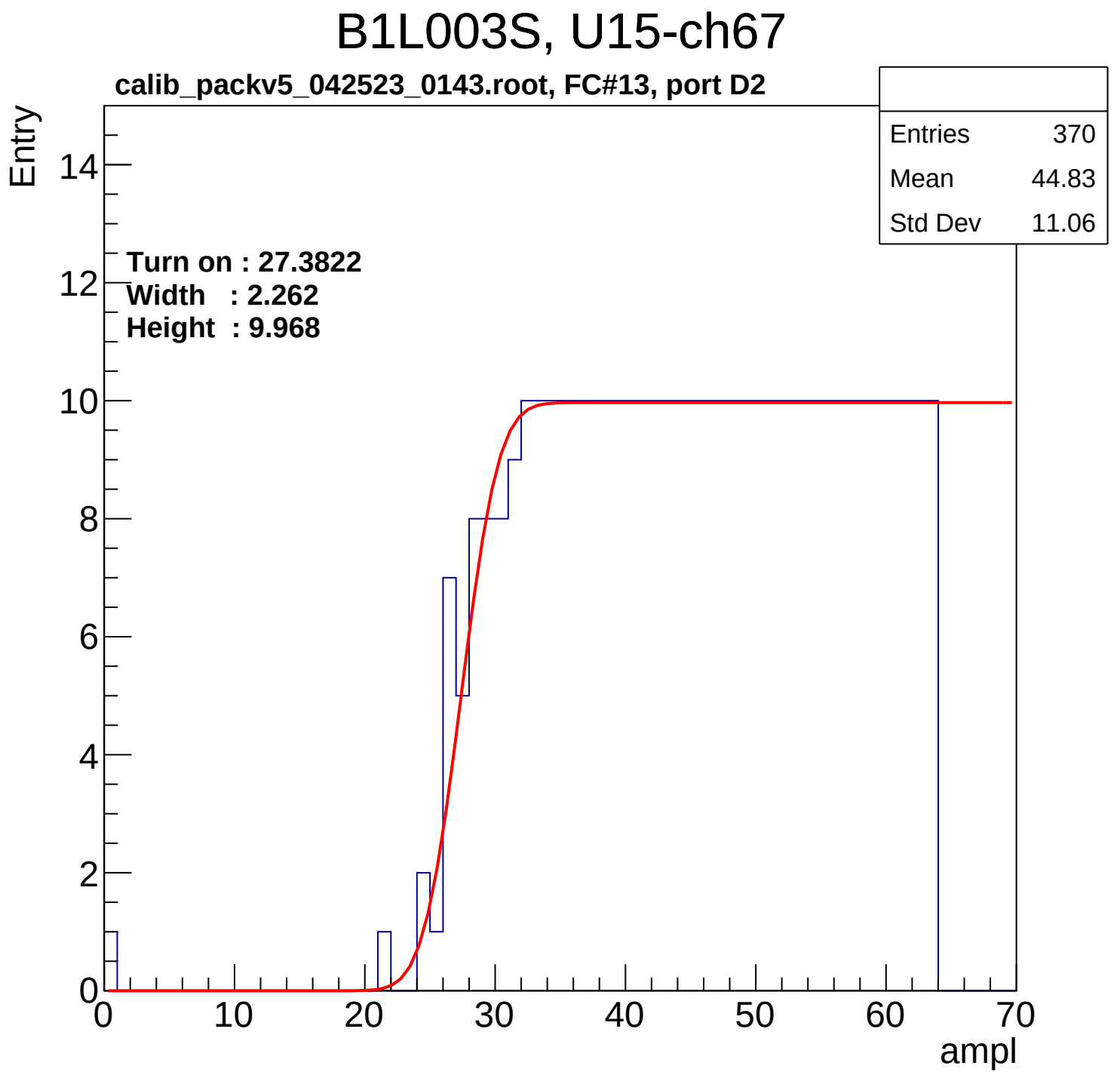
B1L003S, U15-ch67
calib_packv5_042523_0143.root, FC#13, port D2
Entries 370
Mean 44.83
Std Dev 11.06
Turn on : 27.3822
Width : 2.262
Height : 9.968
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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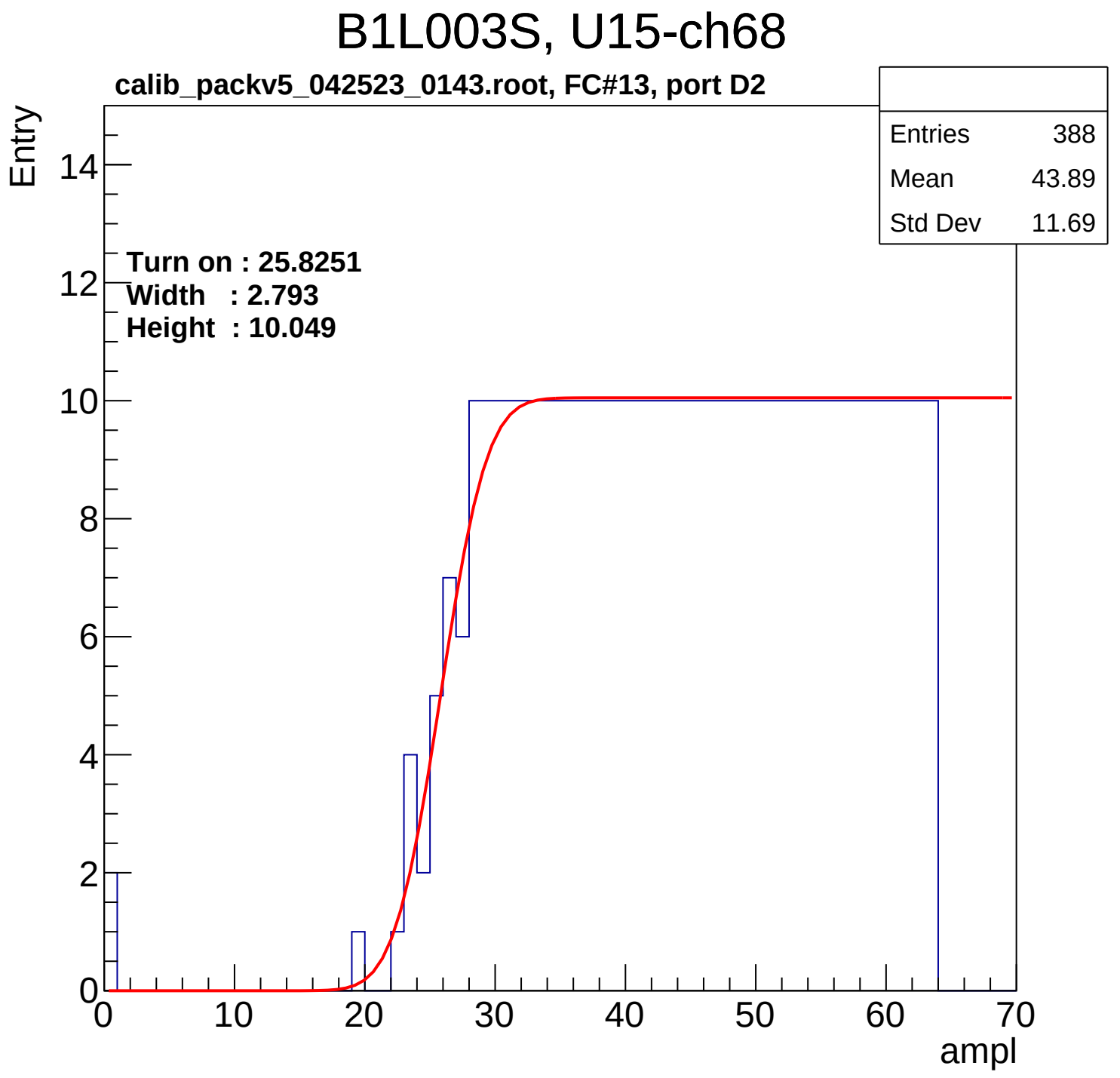
B1L003S, U15-ch68
calib_packv5_042523_0143.root, FC#13, port D2
Entries 388
Mean 43.89
Std Dev 11.69
Turn on : 25.8251
Width : 2.793
Height : 10.049
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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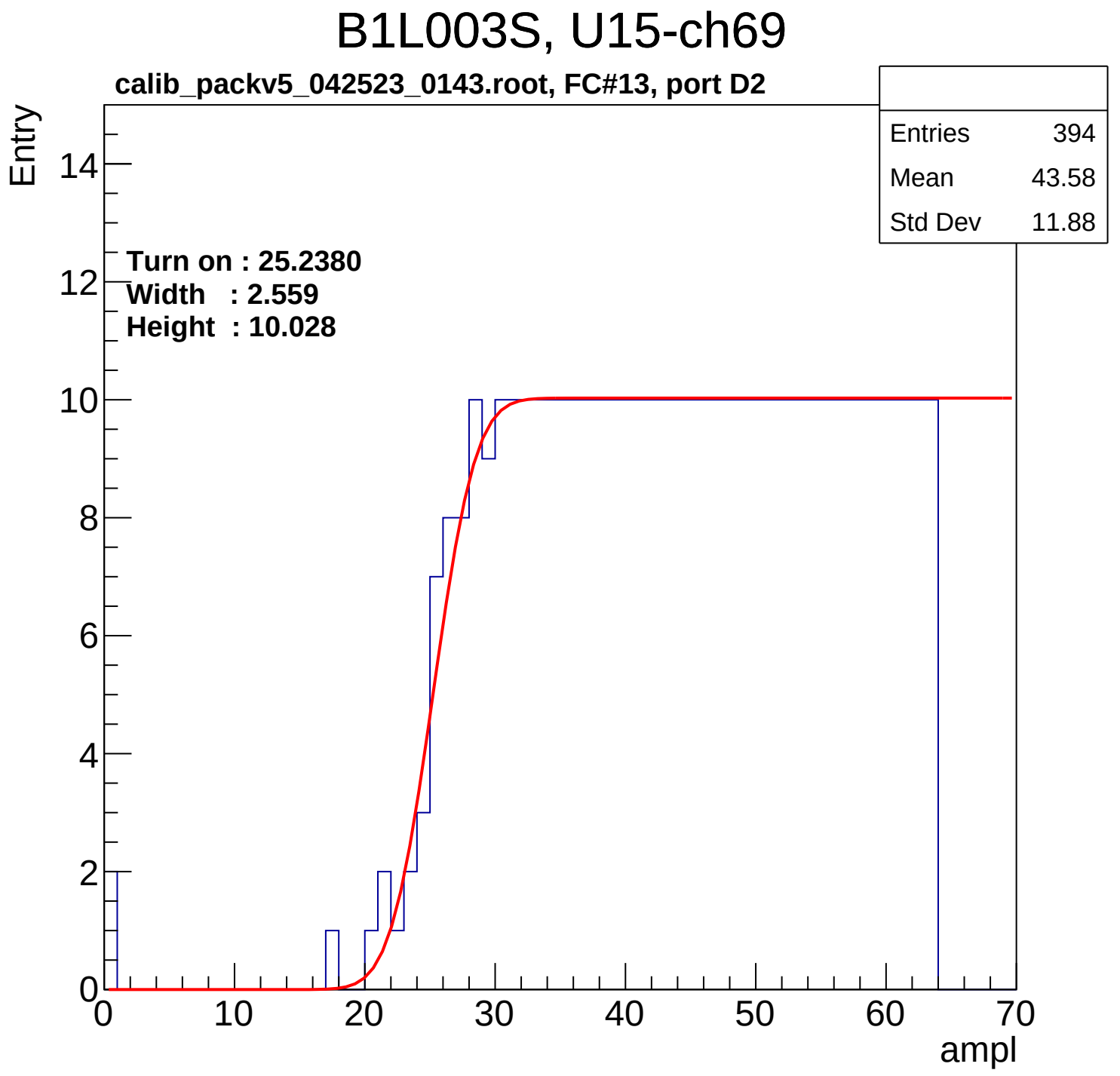
B1L003S, U15-ch69
calib_packv5_042523_0143.root, FC#13, port D2
Entries 394
Mean 43.58
Std Dev 11.88
Turn on : 25.2380
Width : 2.559
Height : 10.028
Entry
ampl
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6
8
10
12
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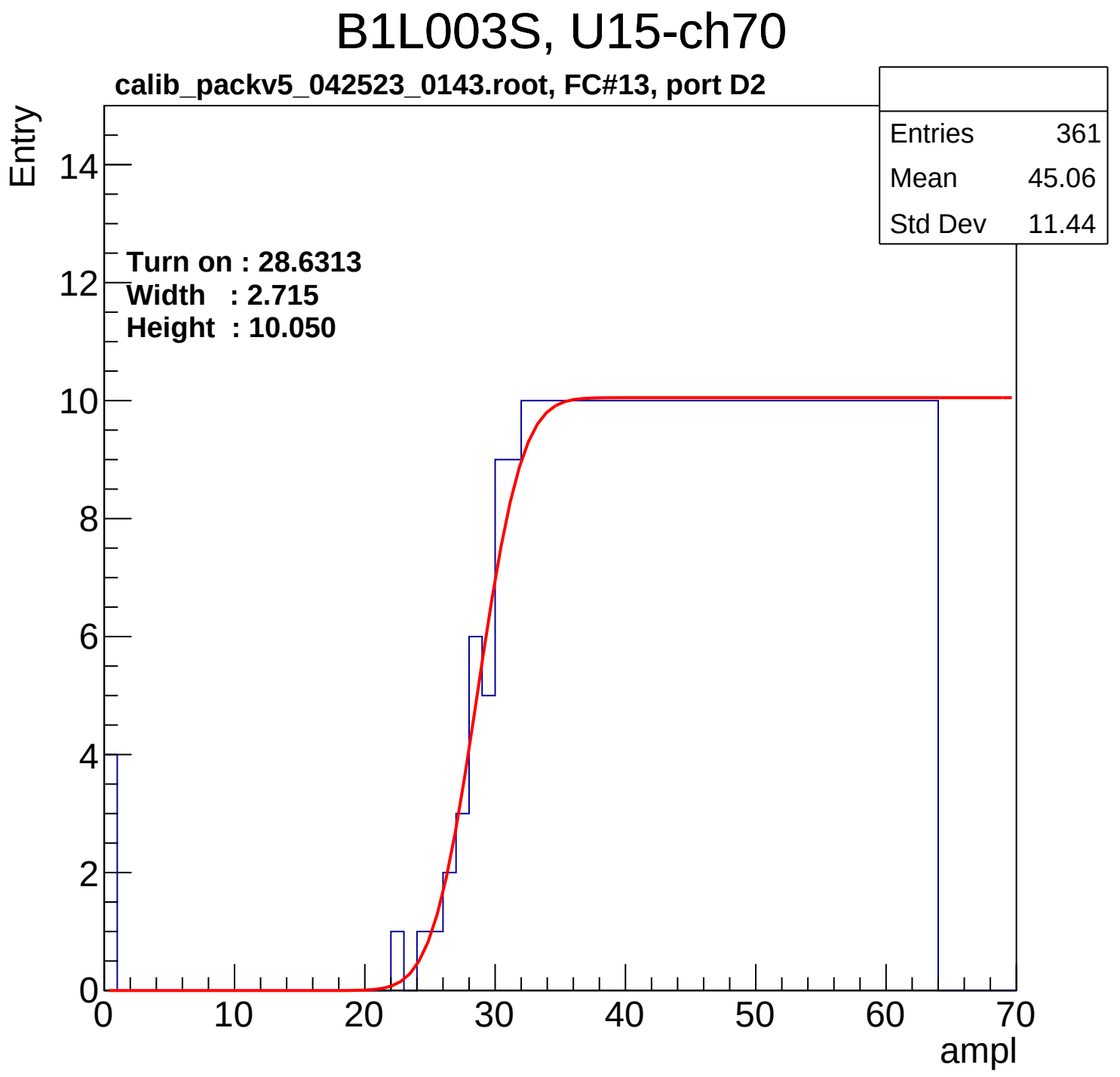
B1L003S, U15-ch70
calib_packv5_042523_0143.root, FC#13, port D2
Entries 361
Mean 45.06
Std Dev 11.44
Turn on : 28.6313
Width : 2.715
Height : 10.050
Entry
ampl
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8
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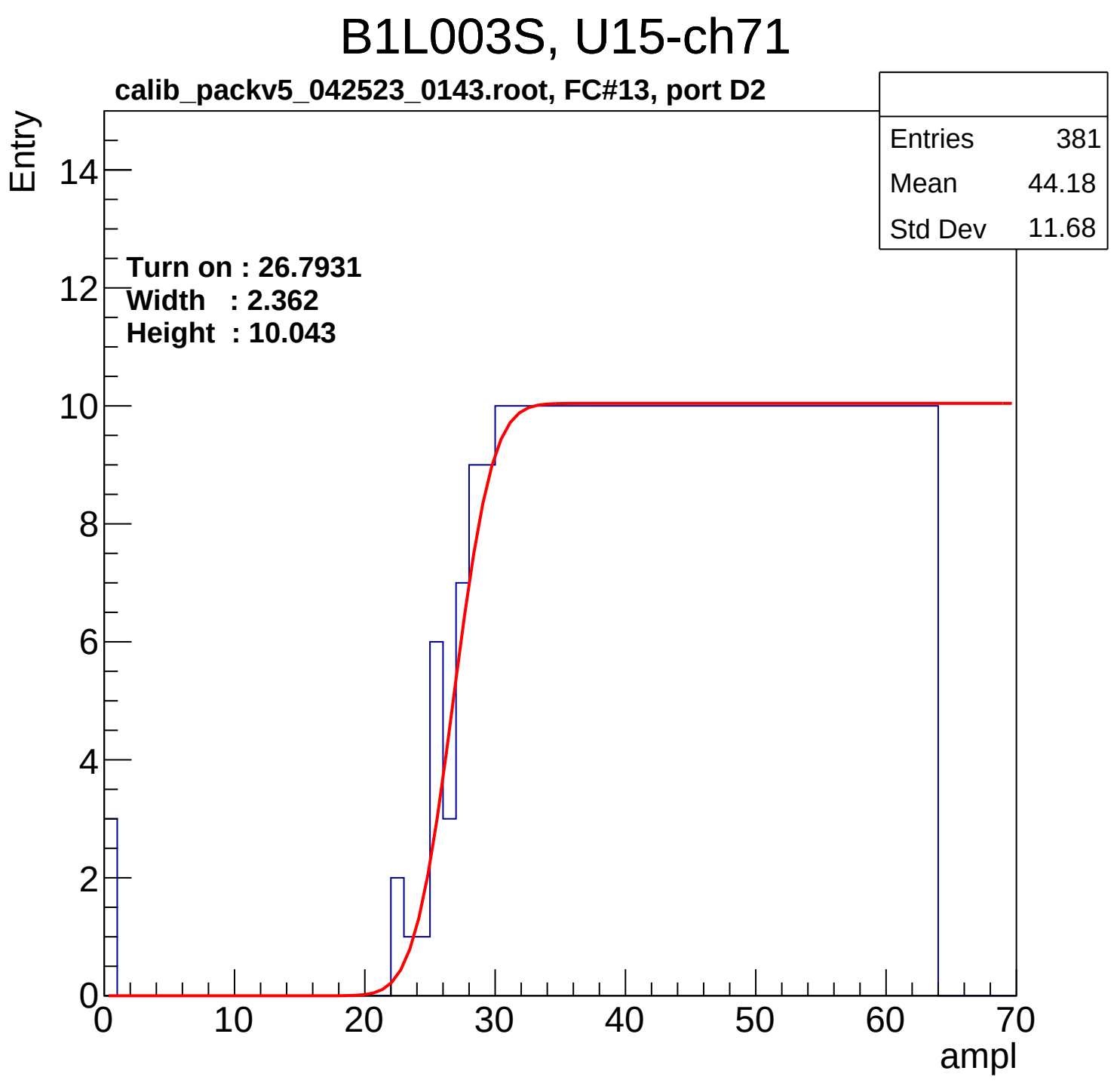
B1L003S, U15-ch71
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 44.18
Std Dev 11.68
Turn on : 26.7931
Width : 2.362
Height : 10.043
Entry
ampl
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4
6
8
10
12
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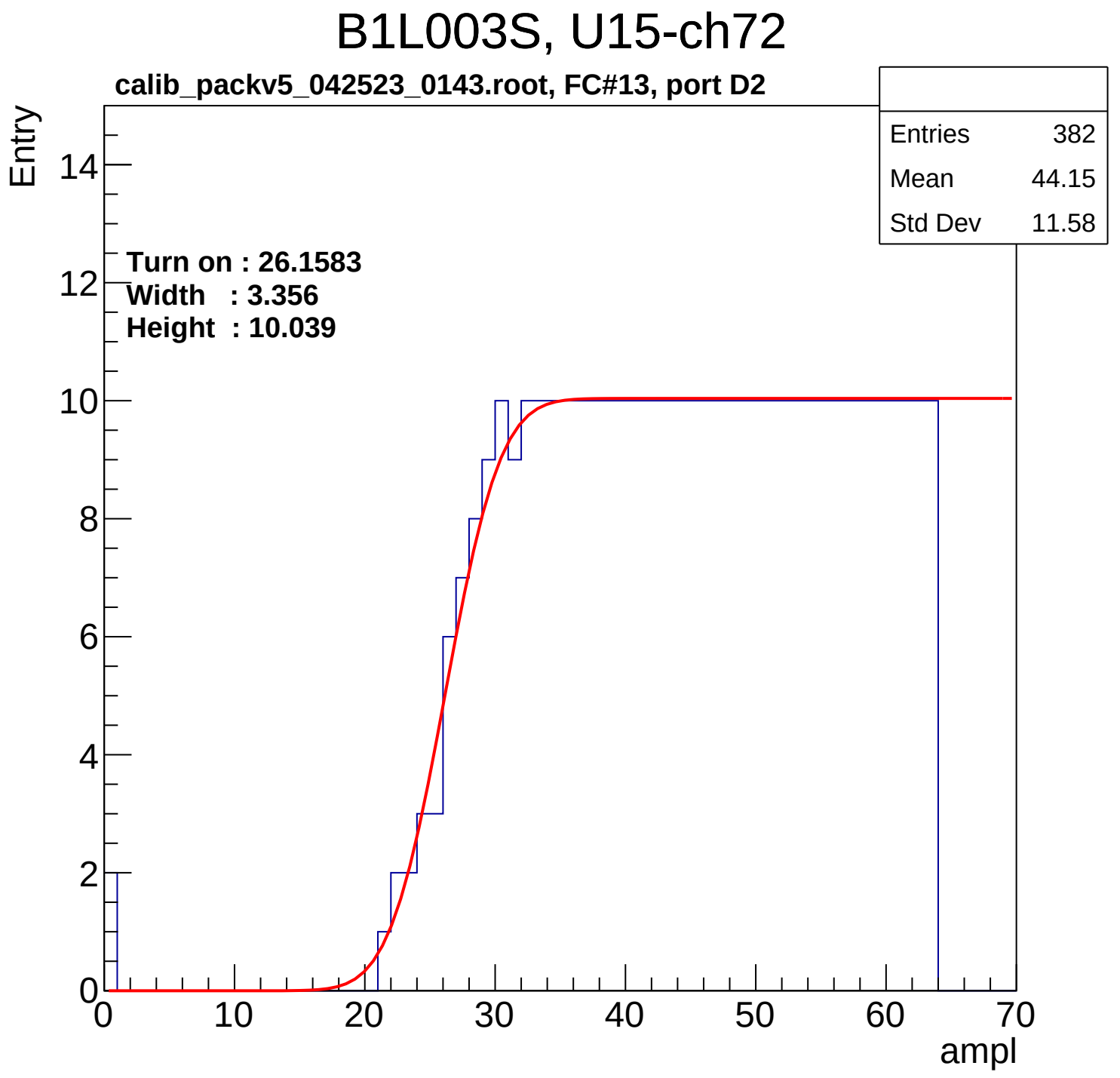
B1L003S, U15-ch72
calib_packv5_042523_0143.root, FC#13, port D2
Entries 382
Mean 44.15
Std Dev 11.58
Turn on : 26.1583
Width : 3.356
Height : 10.039
Entry
ampl
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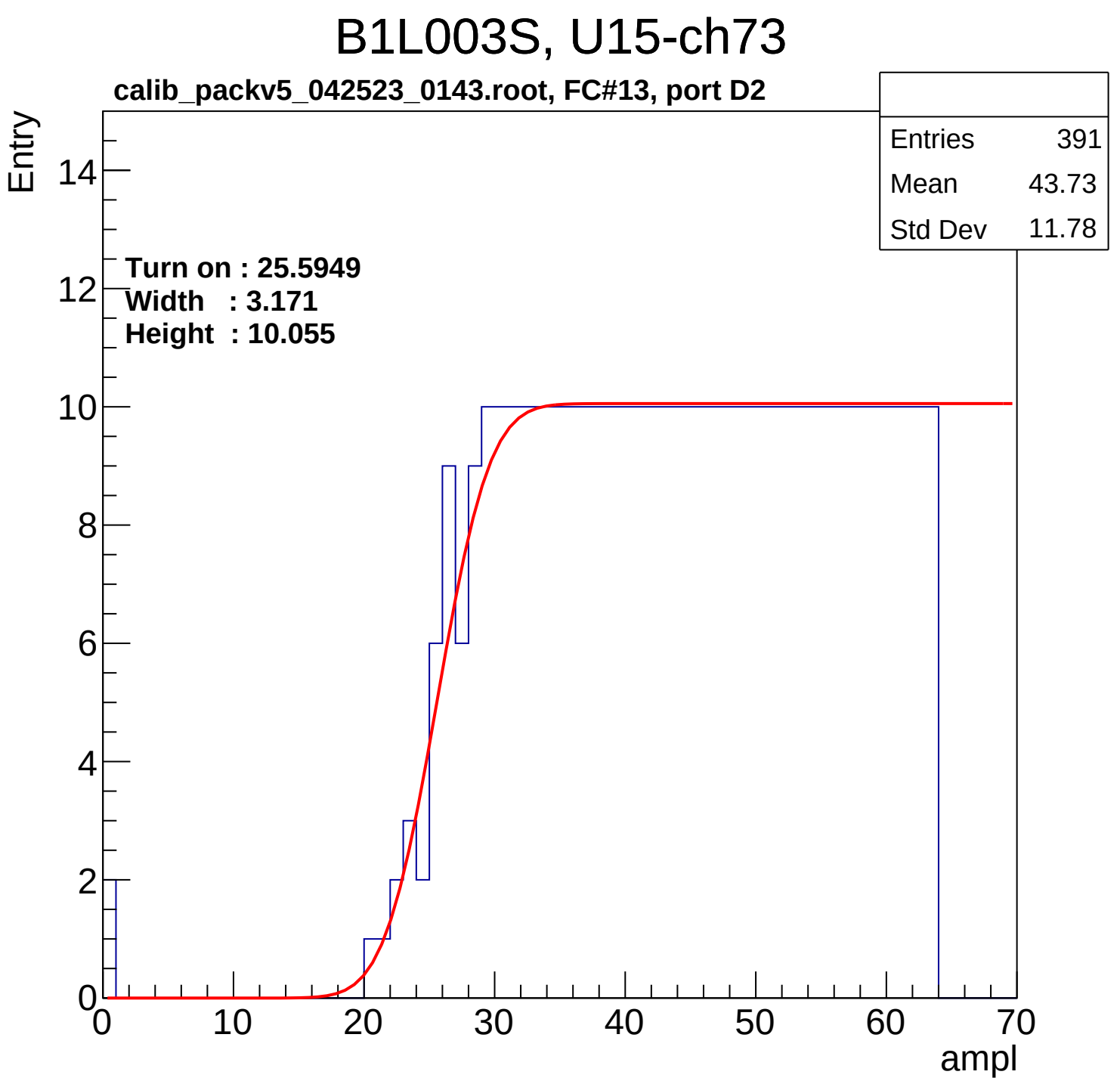
B1L003S, U15-ch73
calib_packv5_042523_0143.root, FC#13, port D2
Entries 391
Mean 43.73
Std Dev 11.78
Turn on : 25.5949
Width : 3.171
Height : 10.055
Entry
ampl
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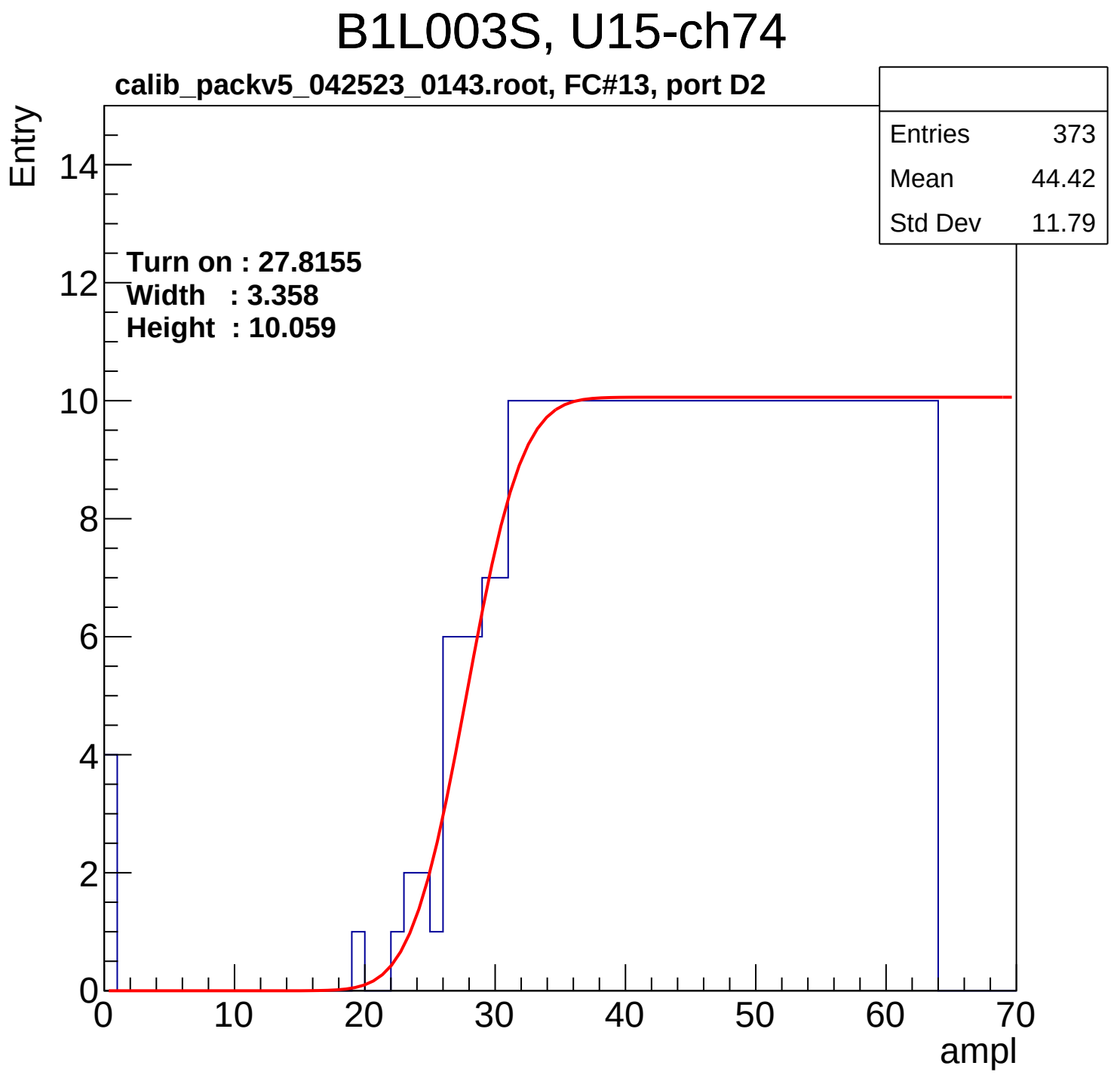
B1L003S, U15-ch74
calib_packv5_042523_0143.root, FC#13, port D2
Entries 373
Mean 44.42
Std Dev 11.79
Turn on : 27.8155
Width : 3.358
Height : 10.059
Entry
ampl
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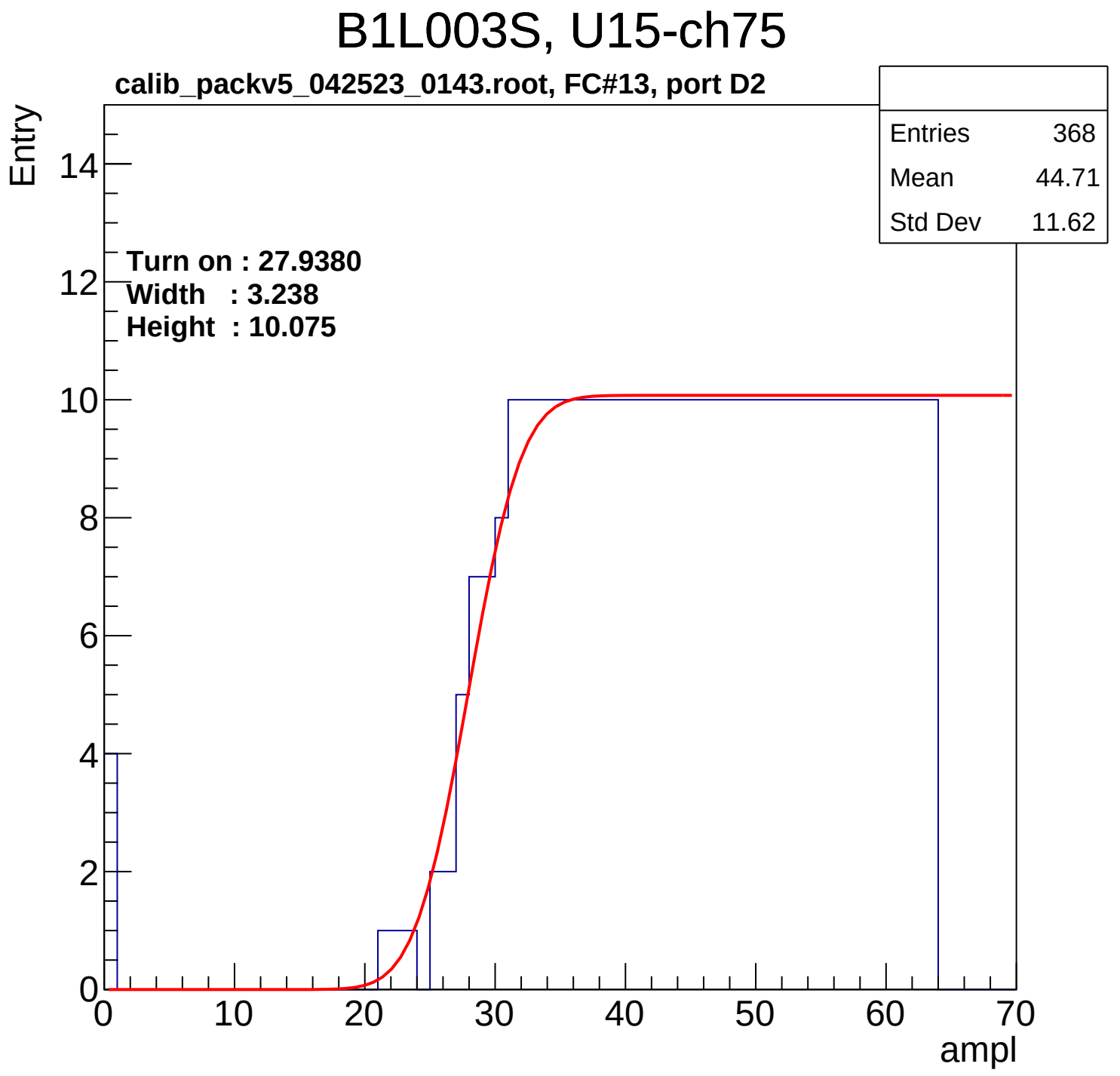
B1L003S, U15-ch75
calib_packv5_042523_0143.root, FC#13, port D2
Entries 368
Mean 44.71
Std Dev 11.62
Turn on : 27.9380
Width : 3.238
Height : 10.075
Entry
ampl
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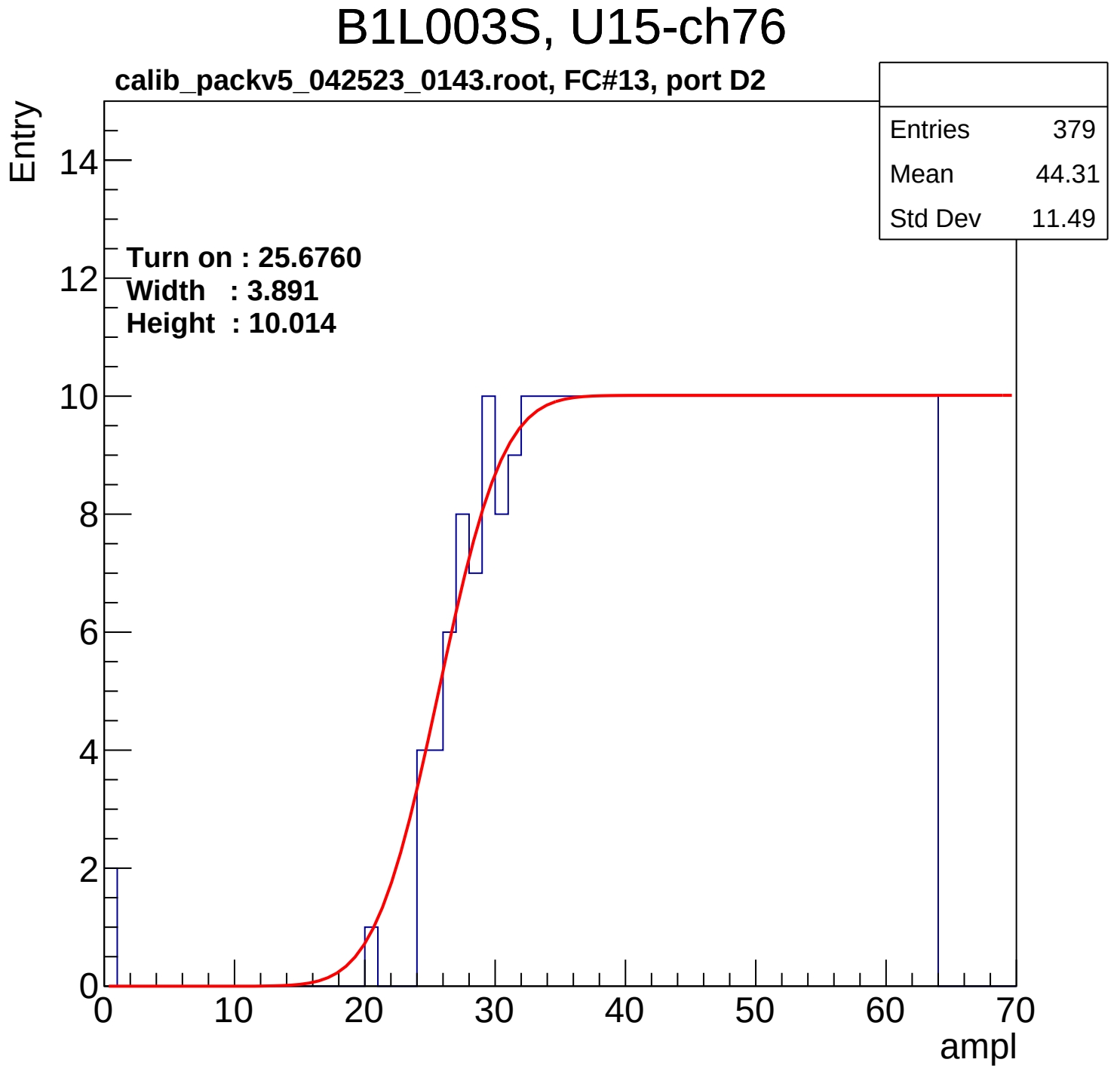
B1L003S, U15-ch76
calib_packv5_042523_0143.root, FC#13, port D2
Entries 379
Mean 44.31
Std Dev 11.49
Turn on : 25.6760
Width : 3.891
Height : 10.014
Entry
ampl
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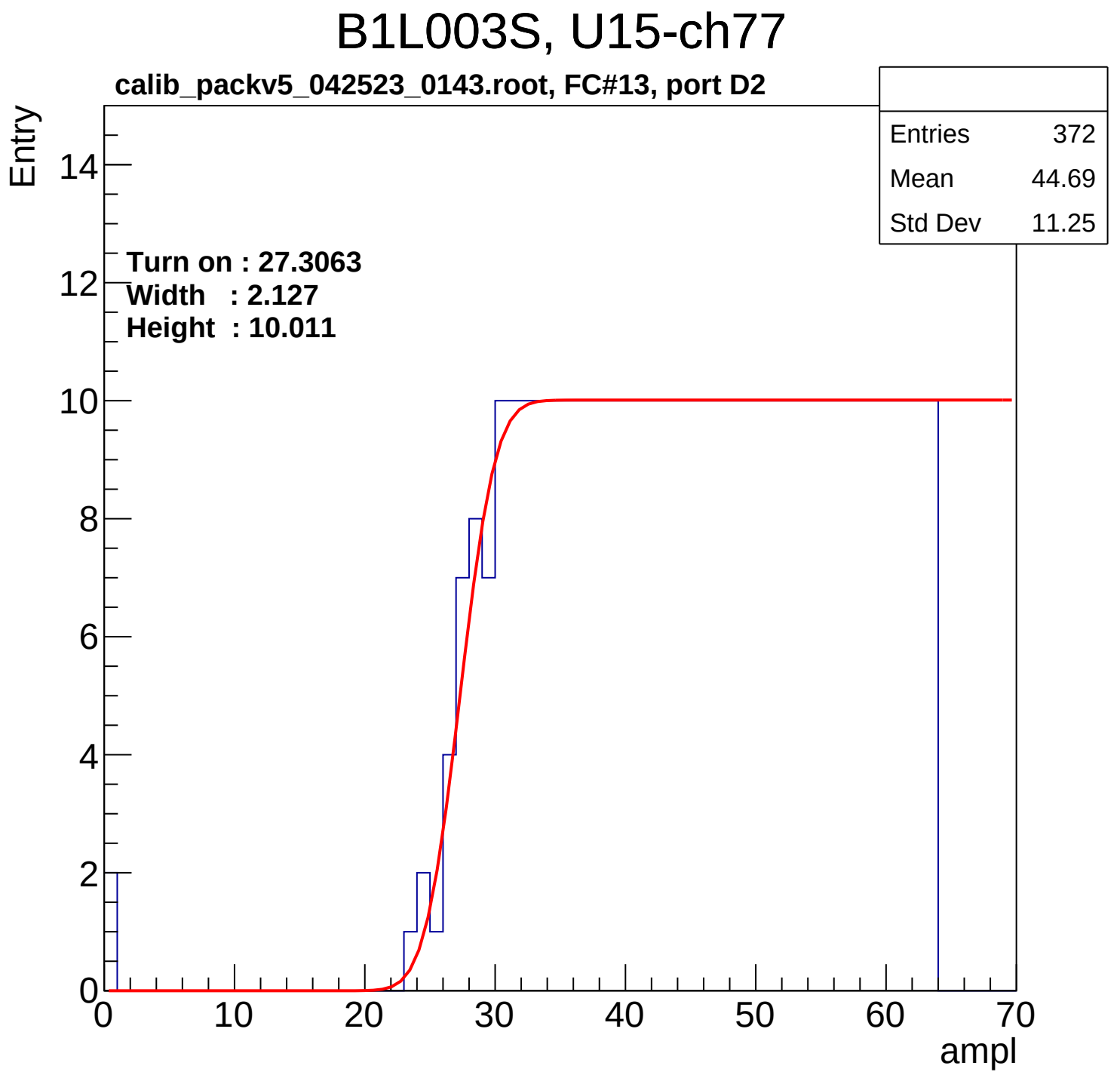
B1L003S, U15-ch77
calib_packv5_042523_0143.root, FC#13, port D2
Entries 372
Mean 44.69
Std Dev 11.25
Turn on : 27.3063
Width : 2.127
Height : 10.011
Entry
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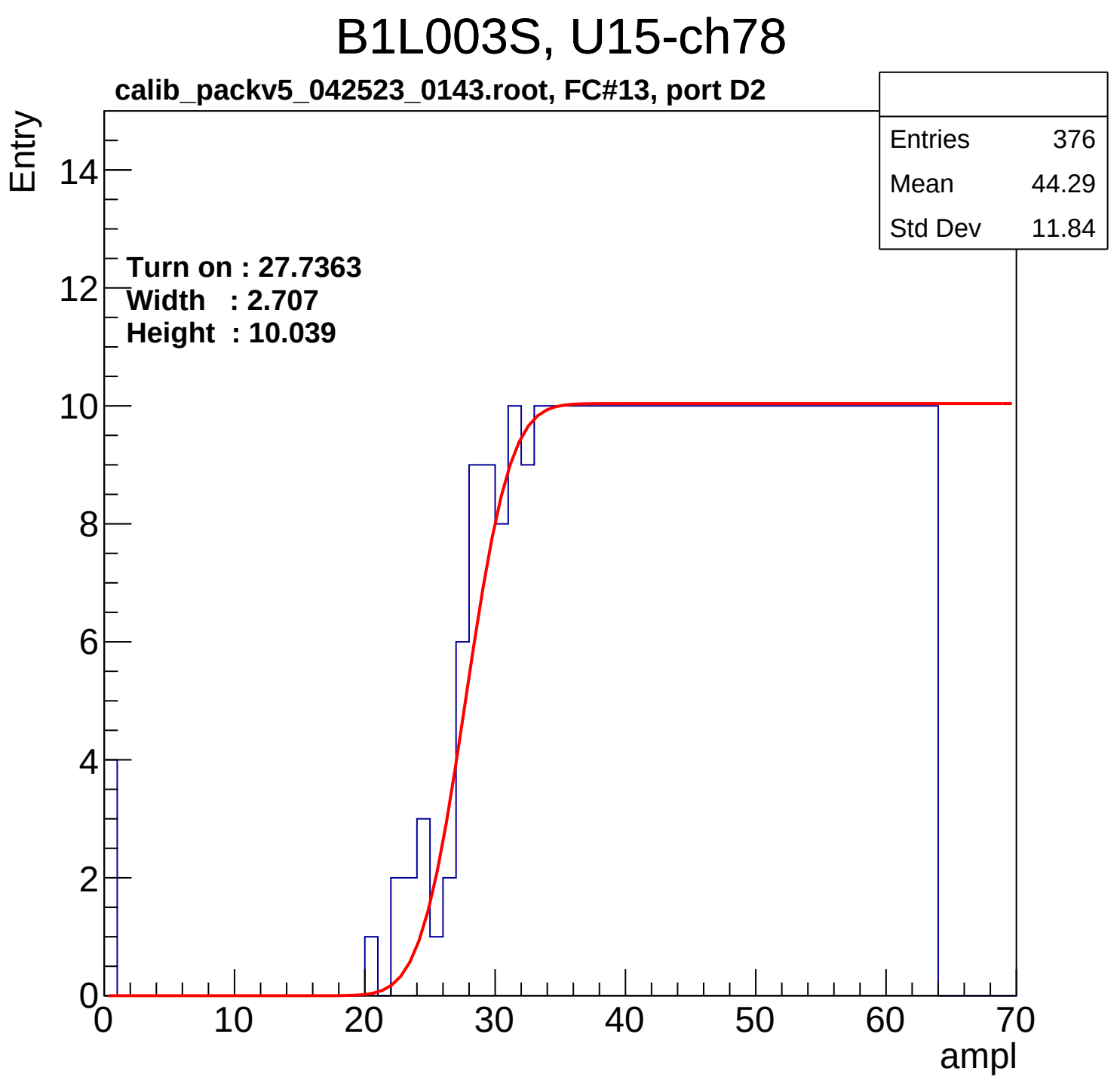
B1L003S, U15-ch78
calib_packv5_042523_0143.root, FC#13, port D2
Entries 376
Mean 44.29
Std Dev 11.84
Turn on : 27.7363
Width : 2.707
Height : 10.039
Entry
ampl
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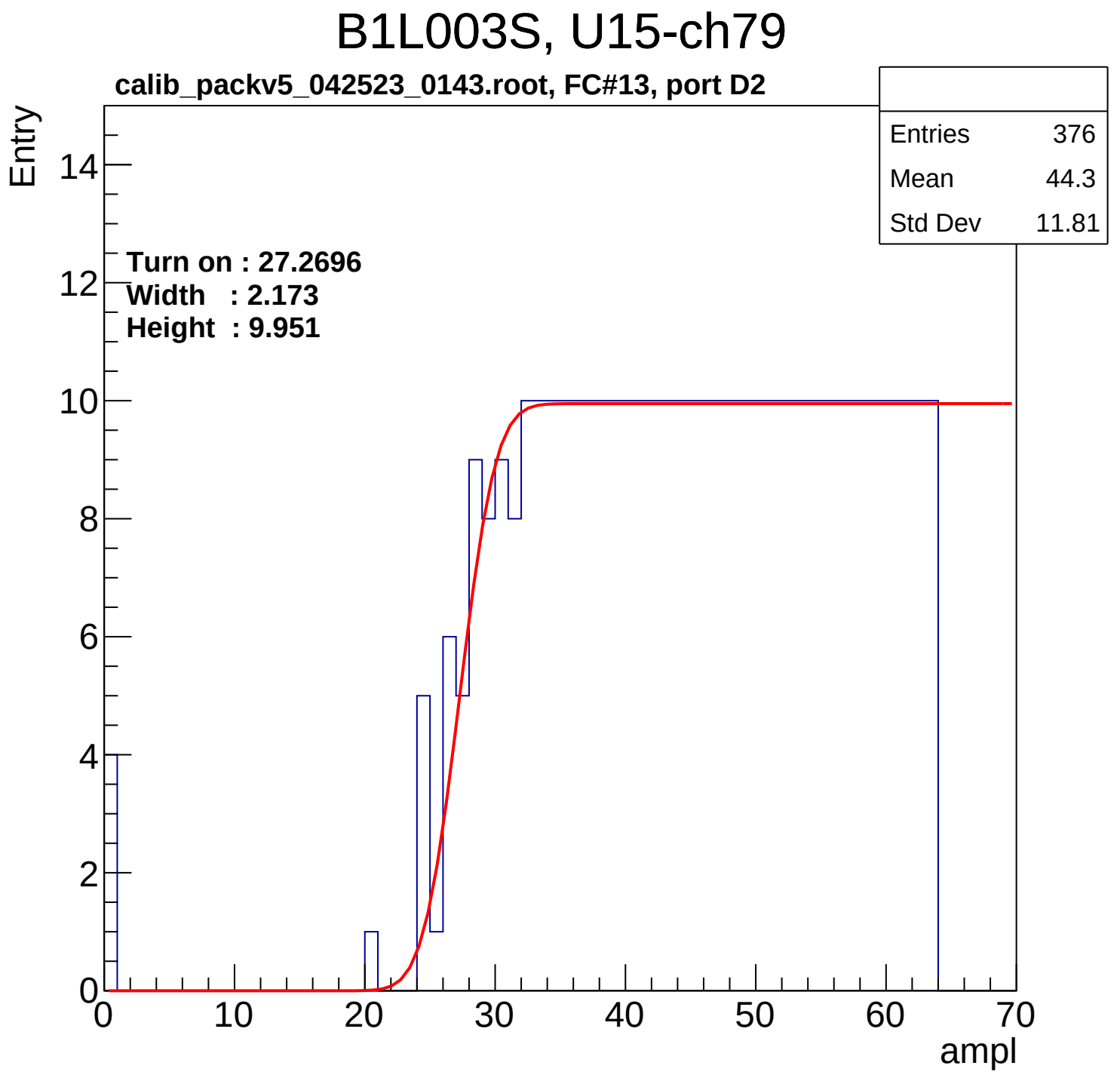
B1L003S, U15-ch79
calib_packv5_042523_0143.root, FC#13, port D2
Entries 376
Mean 44.3
Std Dev 11.81
Turn on : 27.2696
Width : 2.173
Height : 9.951
Entry
ampl
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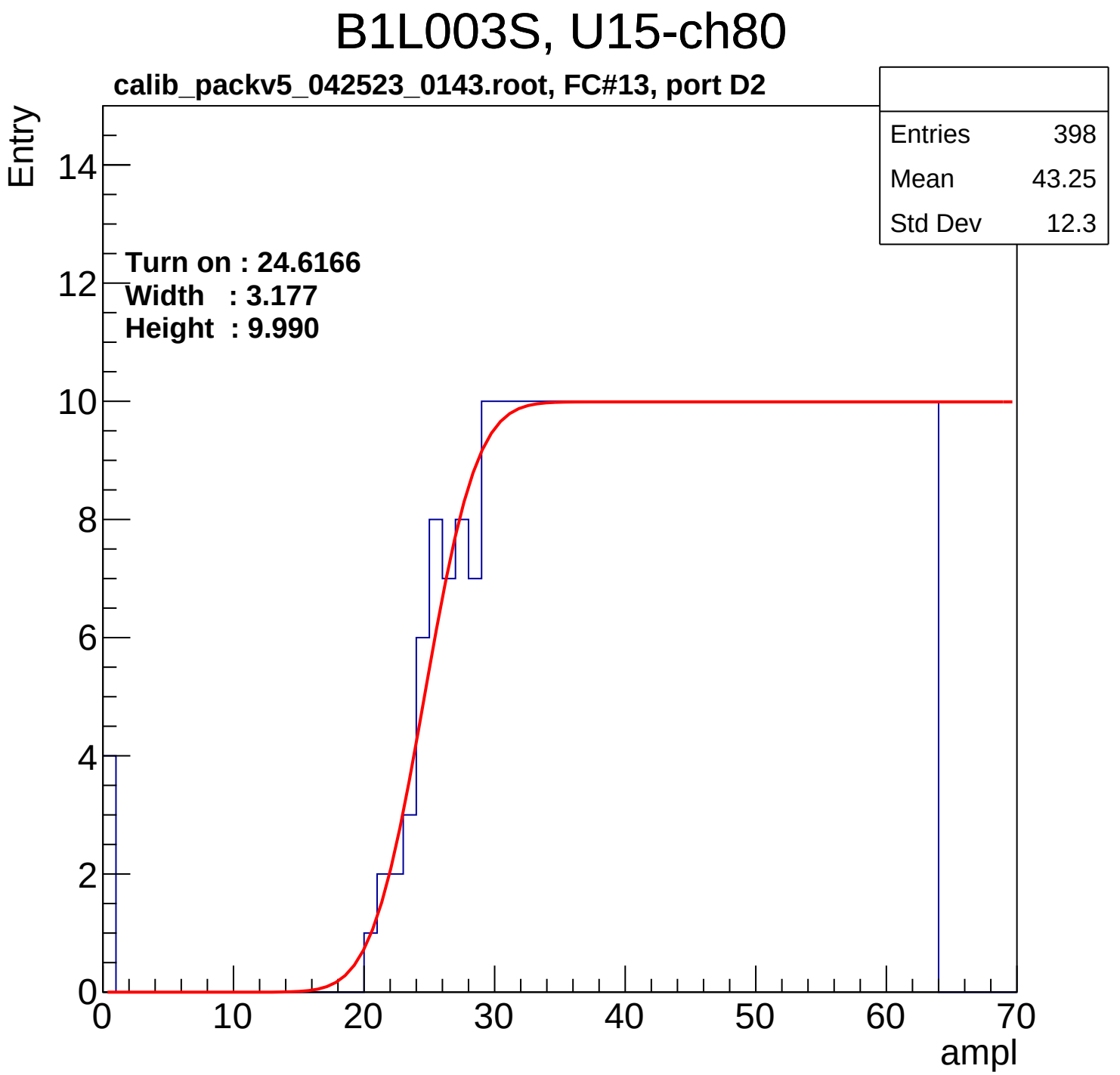
B1L003S, U15-ch80
calib_packv5_042523_0143.root, FC#13, port D2
Entries 398
Mean 43.25
Std Dev 12.3
Turn on : 24.6166
Width : 3.177
Height : 9.990
Entry
ampl
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6
8
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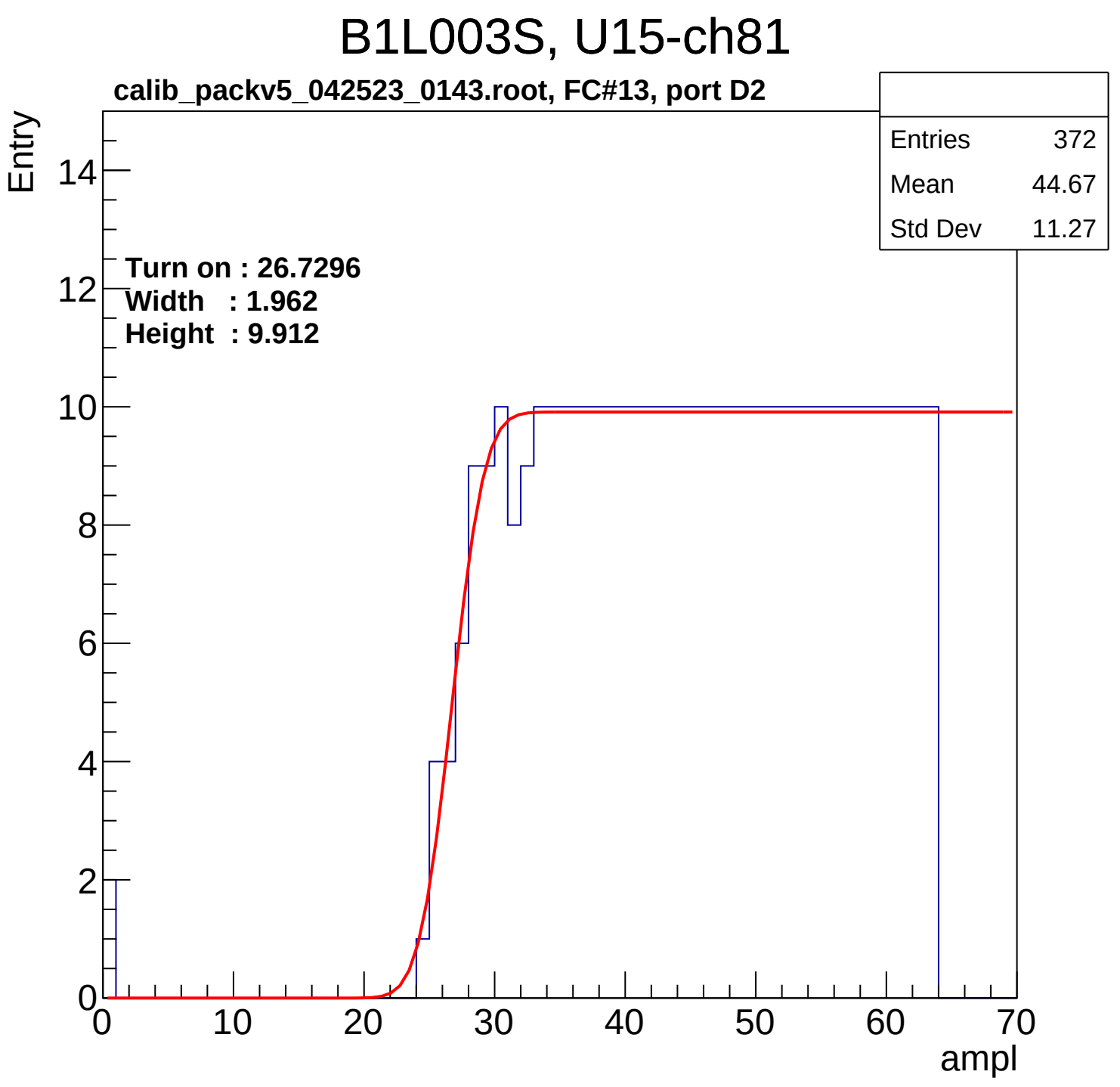
B1L003S, U15-ch81
calib_packv5_042523_0143.root, FC#13, port D2
Entries 372
Mean 44.67
Std Dev 11.27
Turn on : 26.7296
Width : 1.962
Height : 9.912
Entry
ampl
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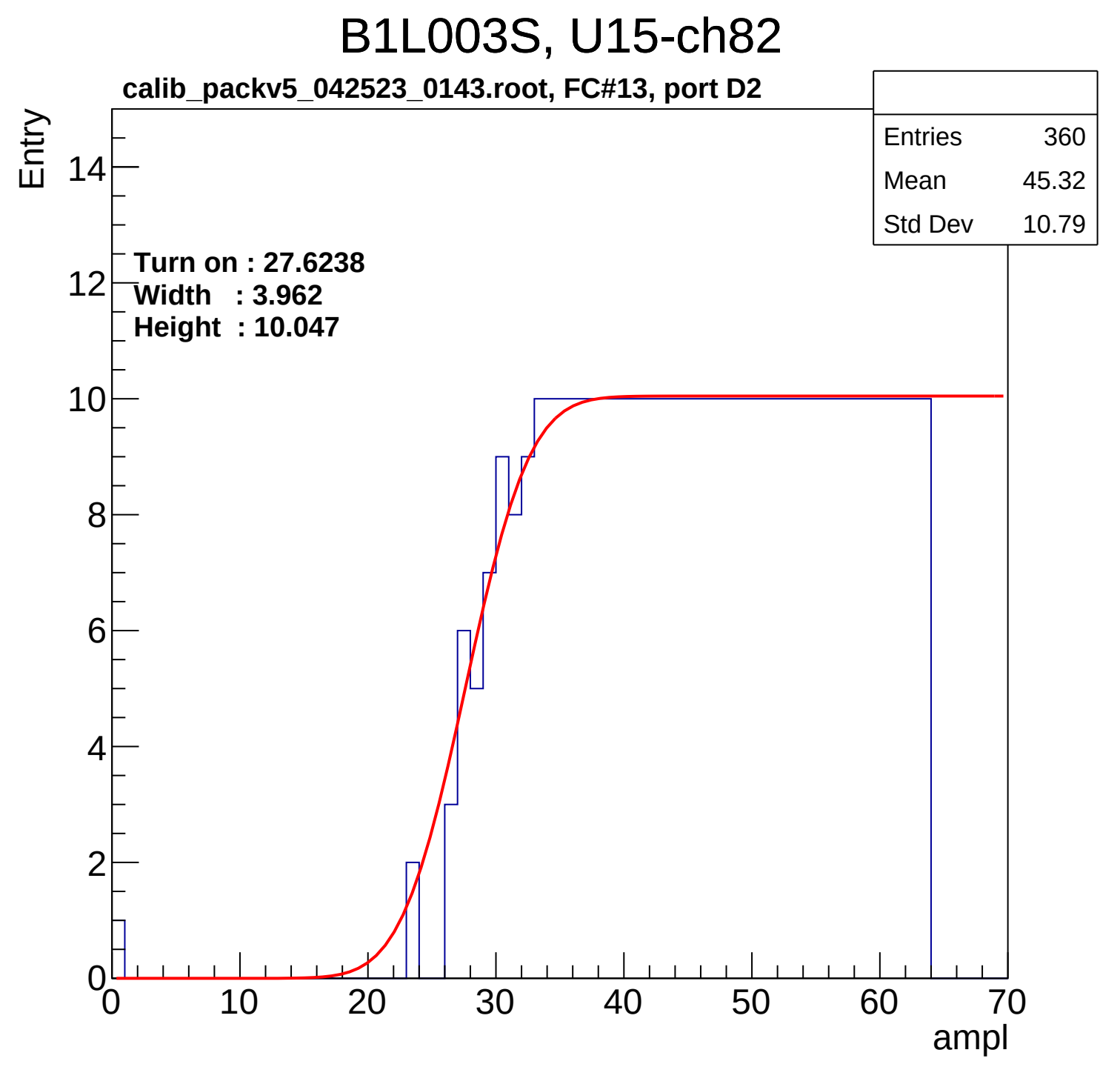
B1L003S, U15-ch82
calib_packv5_042523_0143.root, FC#13, port D2
Entries 360
Mean 45.32
Std Dev 10.79
Turn on : 27.6238
Width : 3.962
Height : 10.047
Entry
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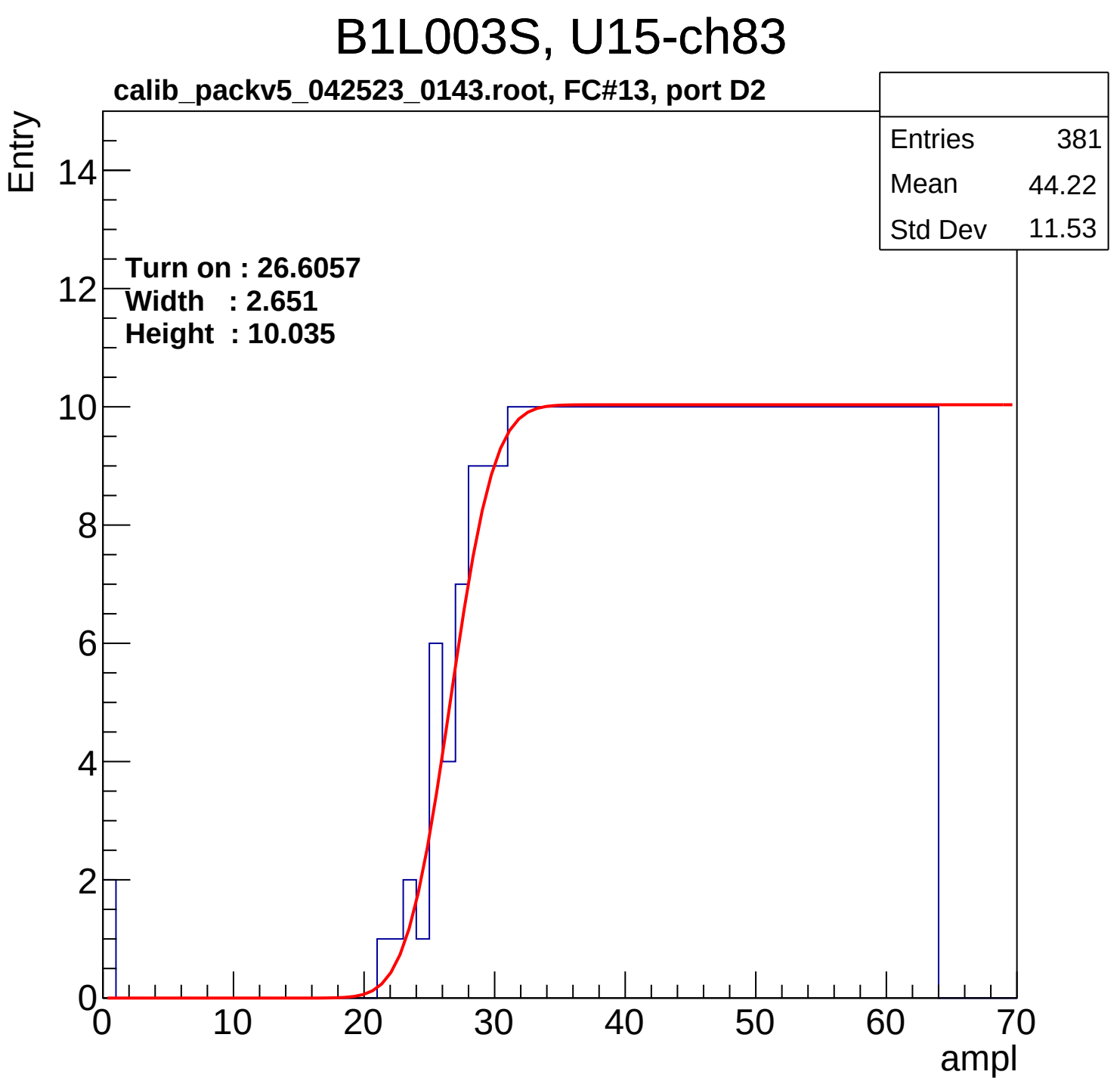
B1L003S, U15-ch83
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 44.22
Std Dev 11.53
Turn on : 26.6057
Width : 2.651
Height : 10.035
Entry
ampl
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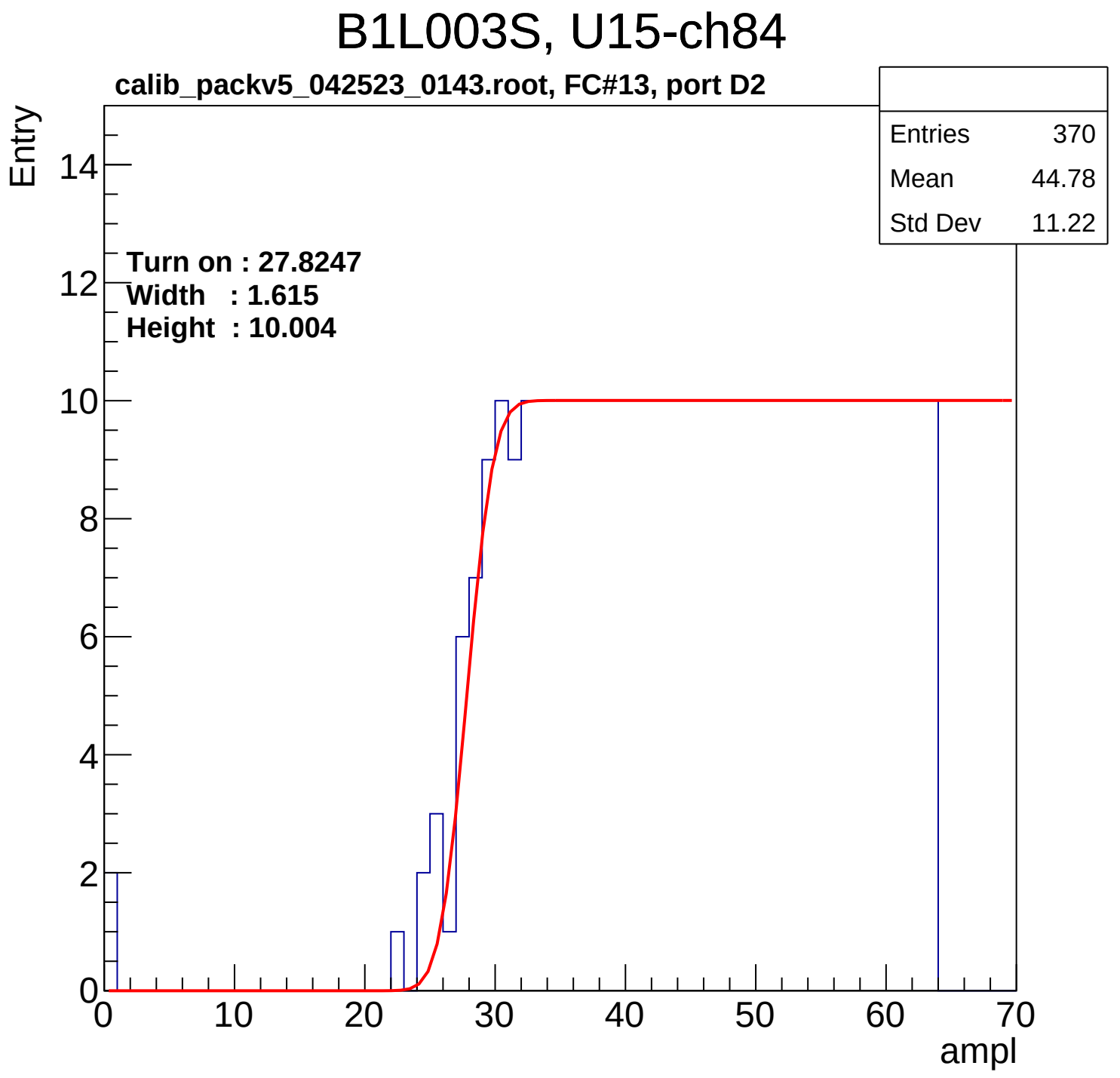
B1L003S, U15-ch84
calib_packv5_042523_0143.root, FC#13, port D2
Entries 370
Mean 44.78
Std Dev 11.22
Turn on : 27.8247
Width : 1.615
Height : 10.004
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ampl
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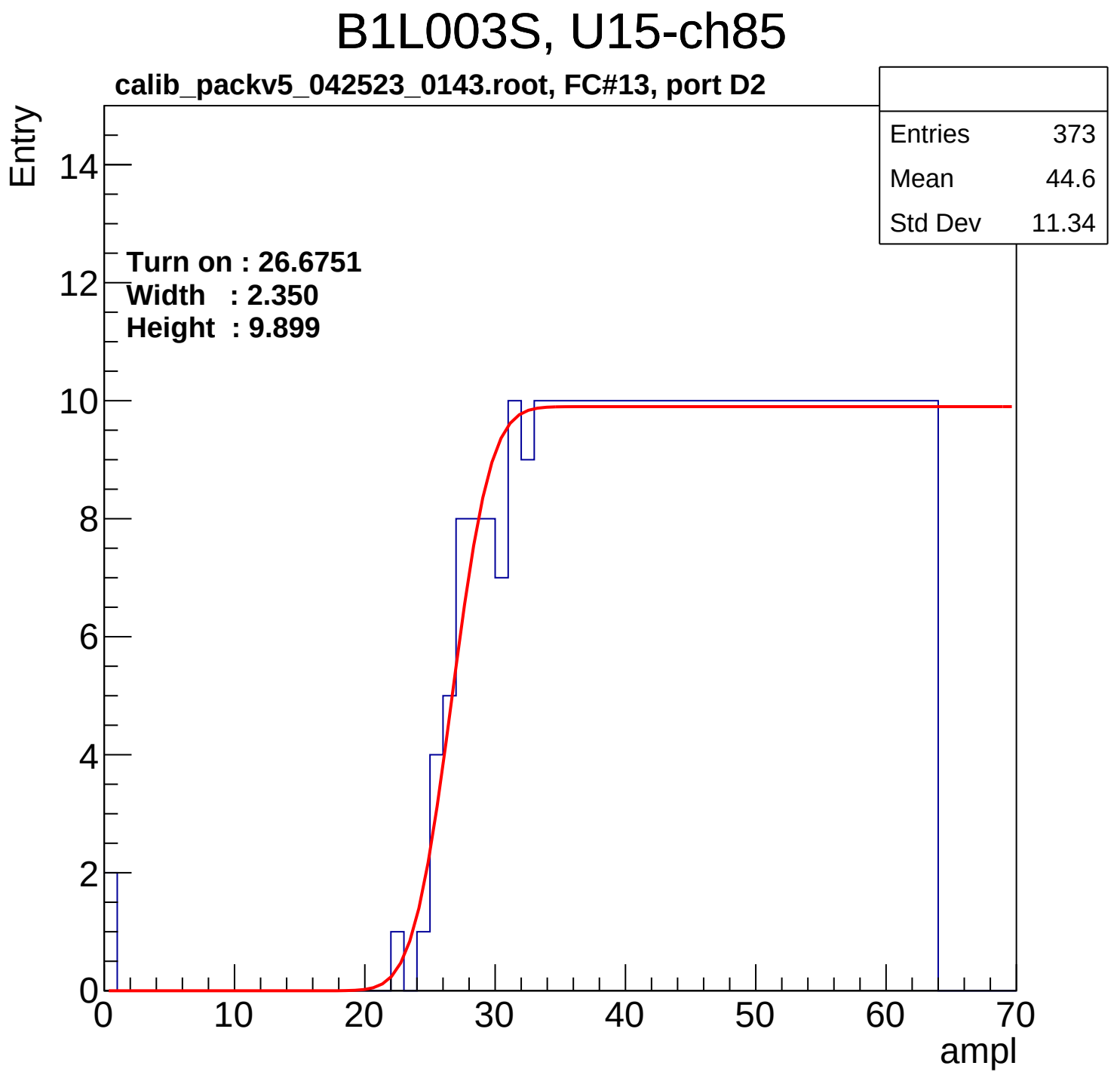
B1L003S, U15-ch85
calib_packv5_042523_0143.root, FC#13, port D2
Entries 373
Mean 44.6
Std Dev 11.34
Turn on : 26.6751
Width : 2.350
Height : 9.899
Entry
ampl
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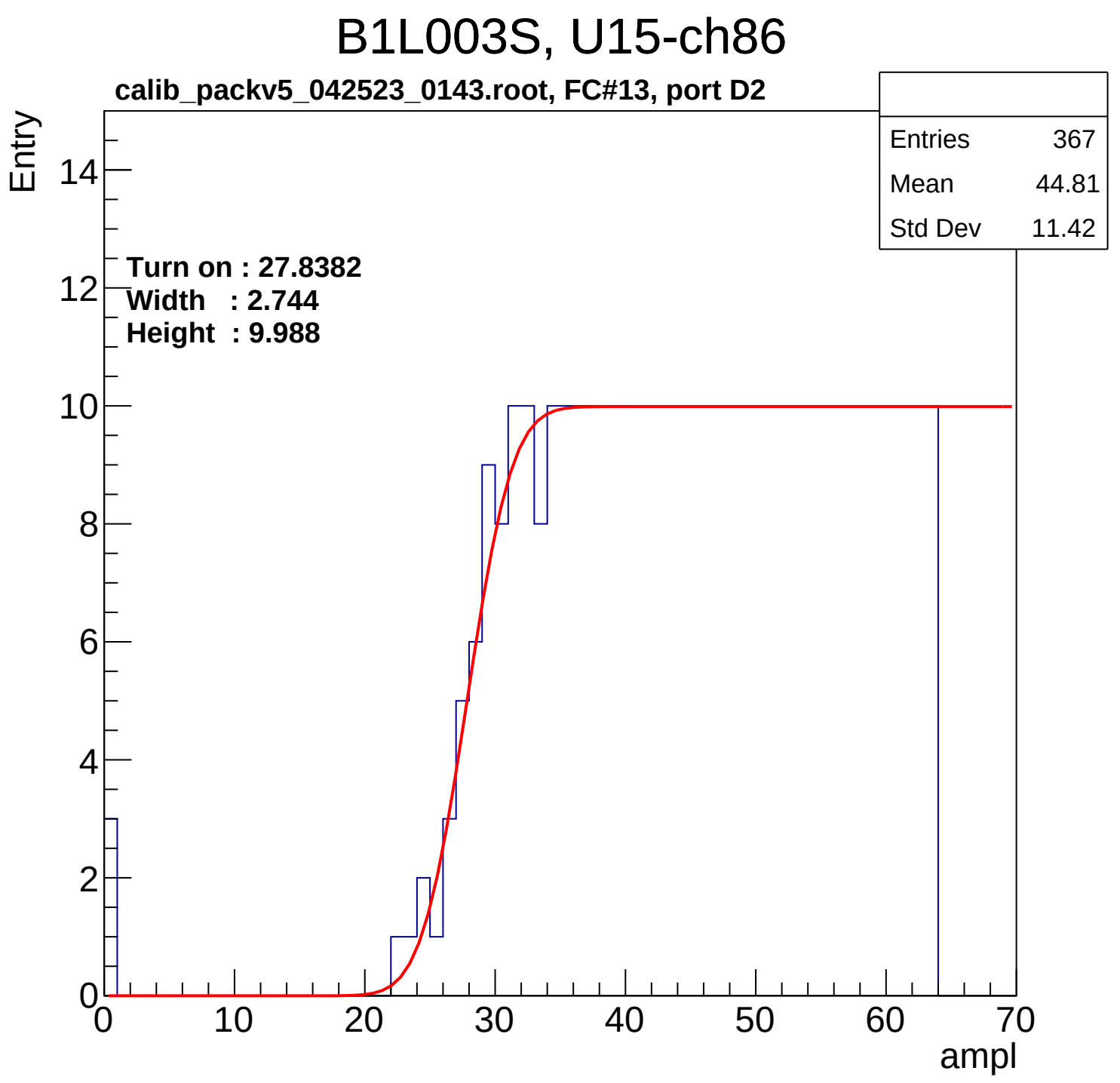
B1L003S, U15-ch86
calib_packv5_042523_0143.root, FC#13, port D2
Entries 367
Mean 44.81
Std Dev 11.42
Turn on : 27.8382
Width : 2.744
Height : 9.988
Entry
ampl
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4
6
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12
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10
20
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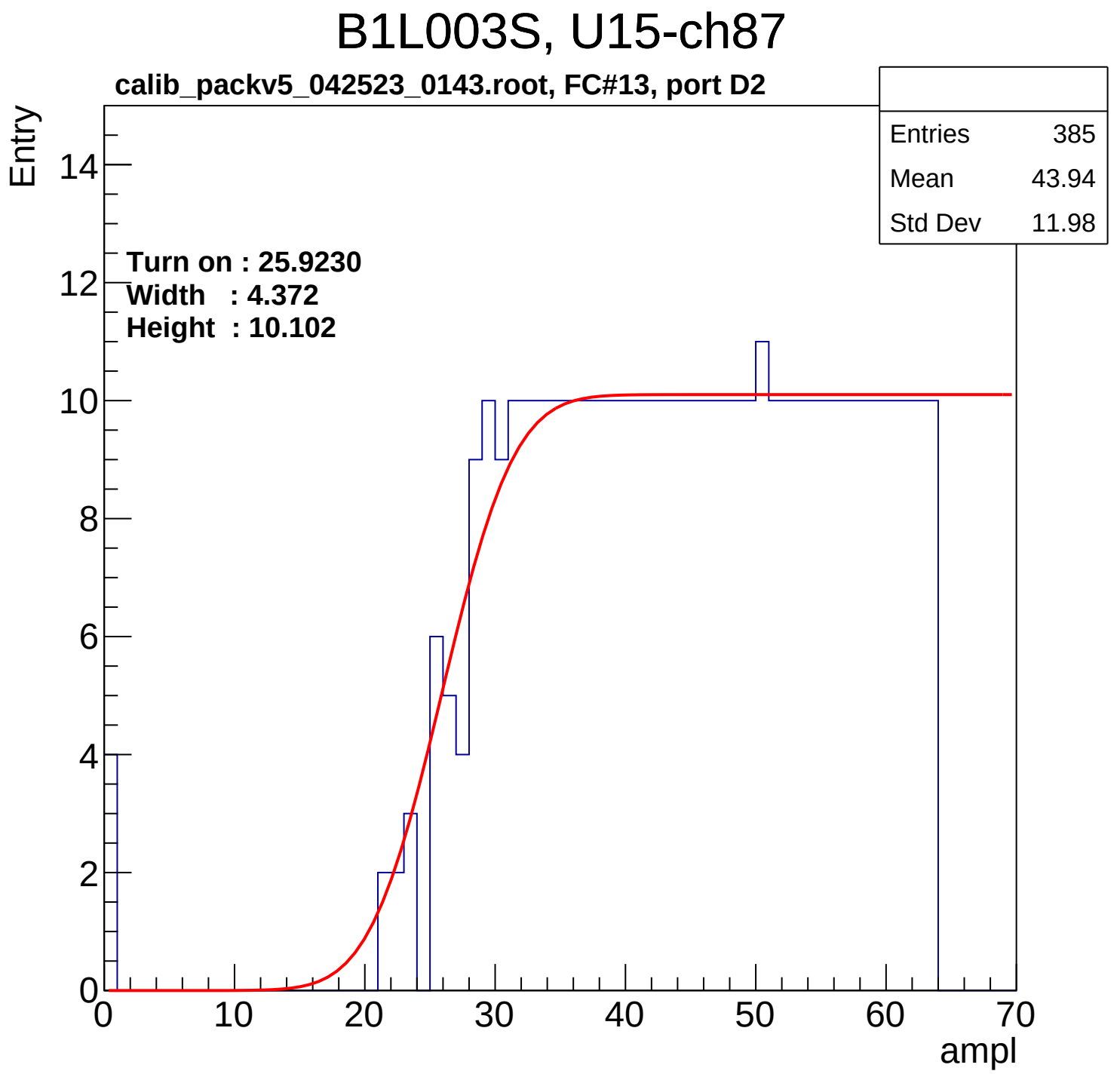
B1L003S, U15-ch87
calib_packv5_042523_0143.root, FC#13, port D2
Entries 385
Mean 43.94
Std Dev 11.98
Turn on : 25.9230
Width : 4.372
Height : 10.102
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ampl
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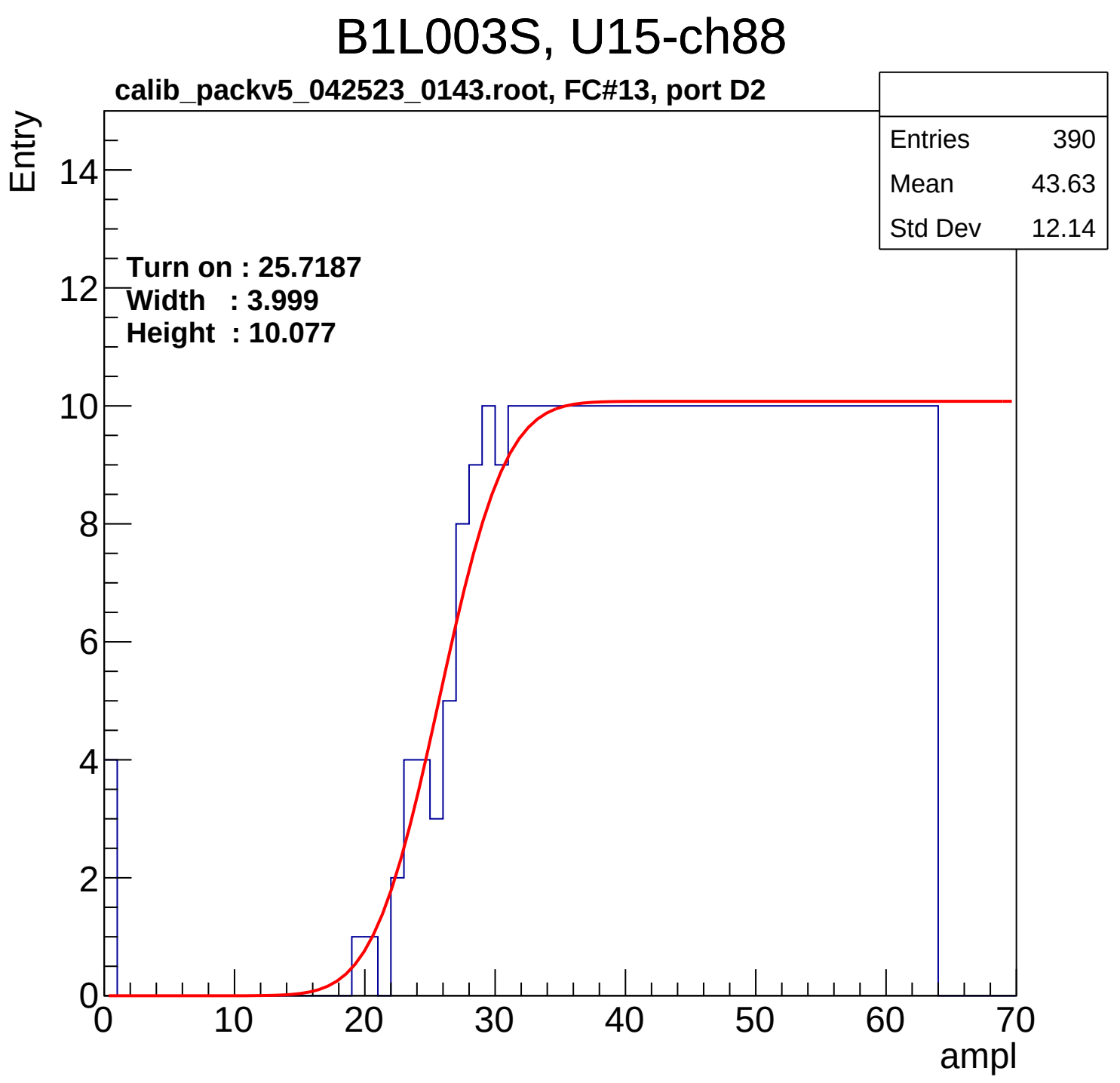
B1L003S, U15-ch88
calib_packv5_042523_0143.root, FC#13, port D2
Entries 390
Mean 43.63
Std Dev 12.14
Turn on : 25.7187
Width : 3.999
Height : 10.077
Entry
ampl
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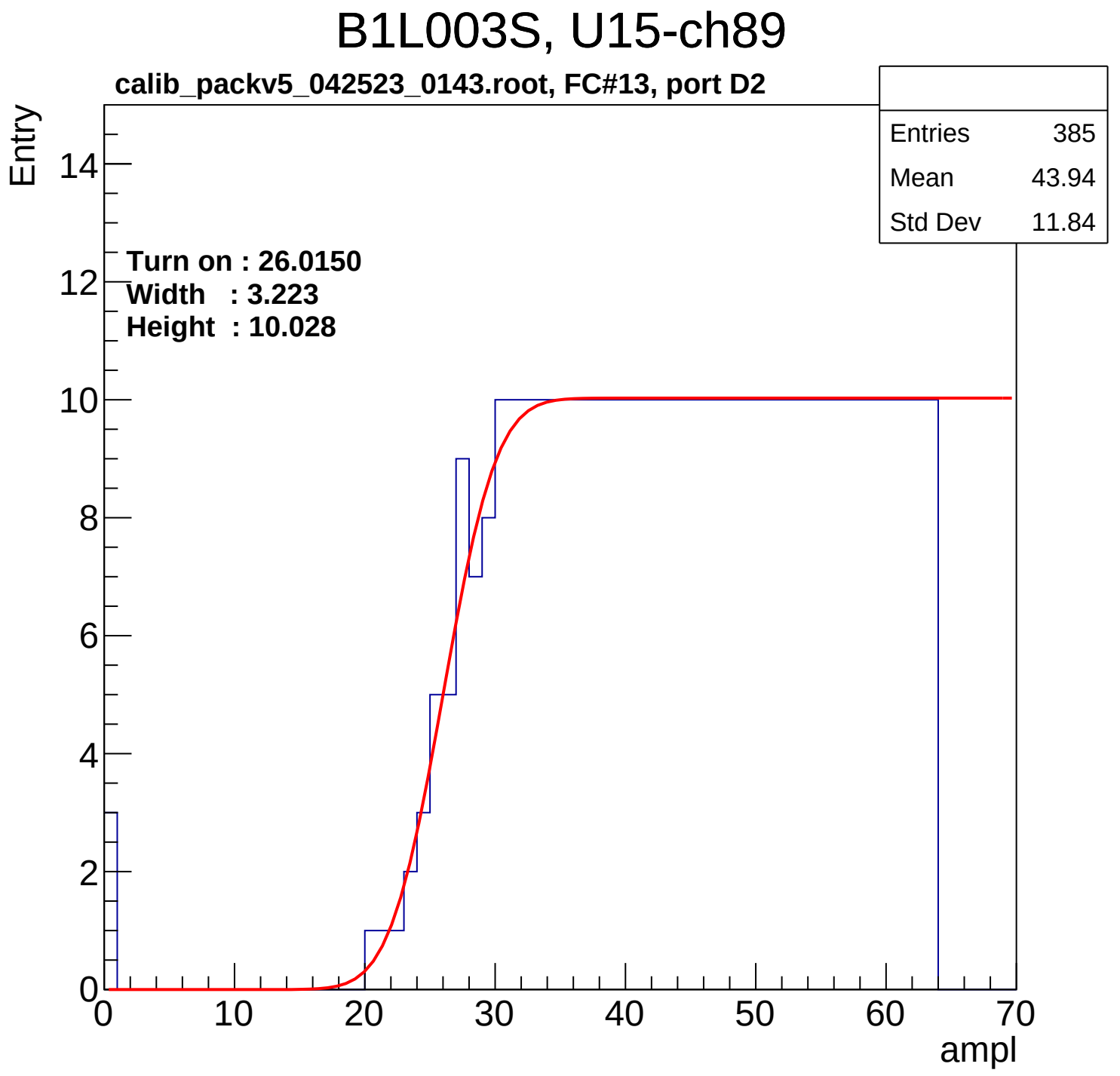
B1L003S, U15-ch89
calib_packv5_042523_0143.root, FC#13, port D2
Entries 385
Mean 43.94
Std Dev 11.84
Turn on : 26.0150
Width : 3.223
Height : 10.028
Entry
ampl
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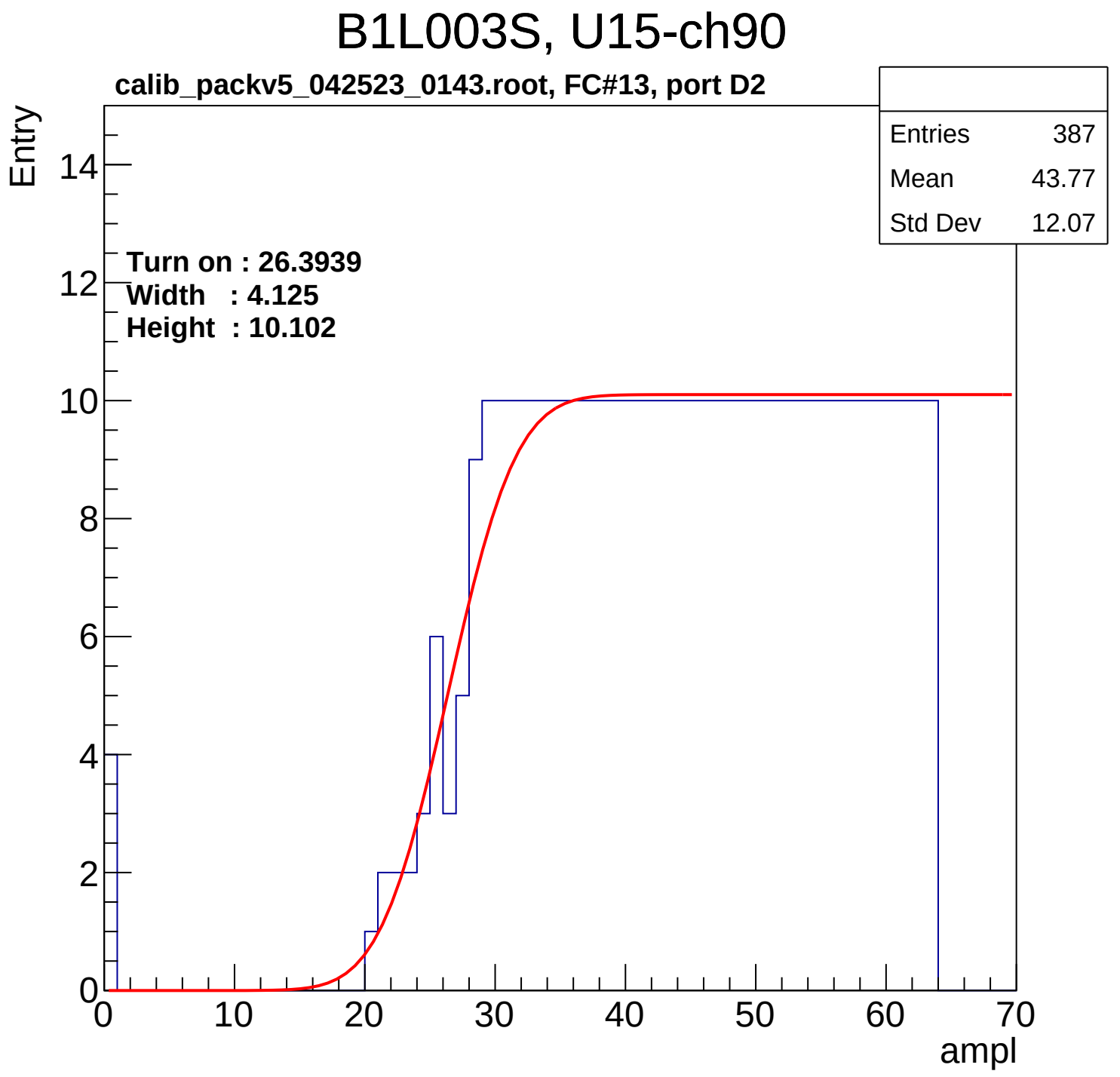
B1L003S, U15-ch90
calib_packv5_042523_0143.root, FC#13, port D2
Entries 387
Mean 43.77
Std Dev 12.07
Turn on : 26.3939
Width : 4.125
Height : 10.102
Entry
ampl
0
2
4
6
8
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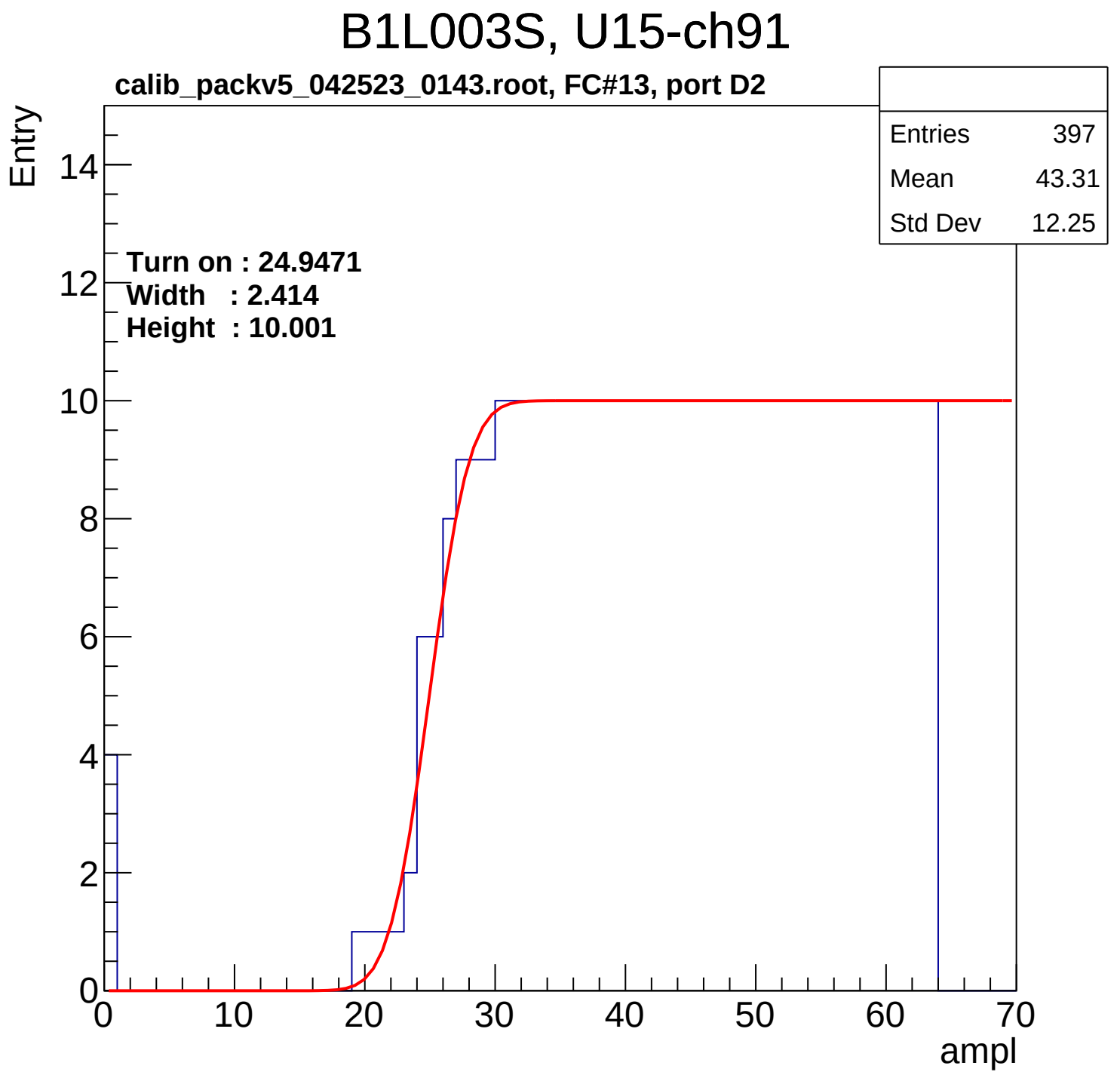
B1L003S, U15-ch91
calib_packv5_042523_0143.root, FC#13, port D2
Entries 397
Mean 43.31
Std Dev 12.25
Turn on : 24.9471
Width : 2.414
Height : 10.001
Entry
ampl
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6
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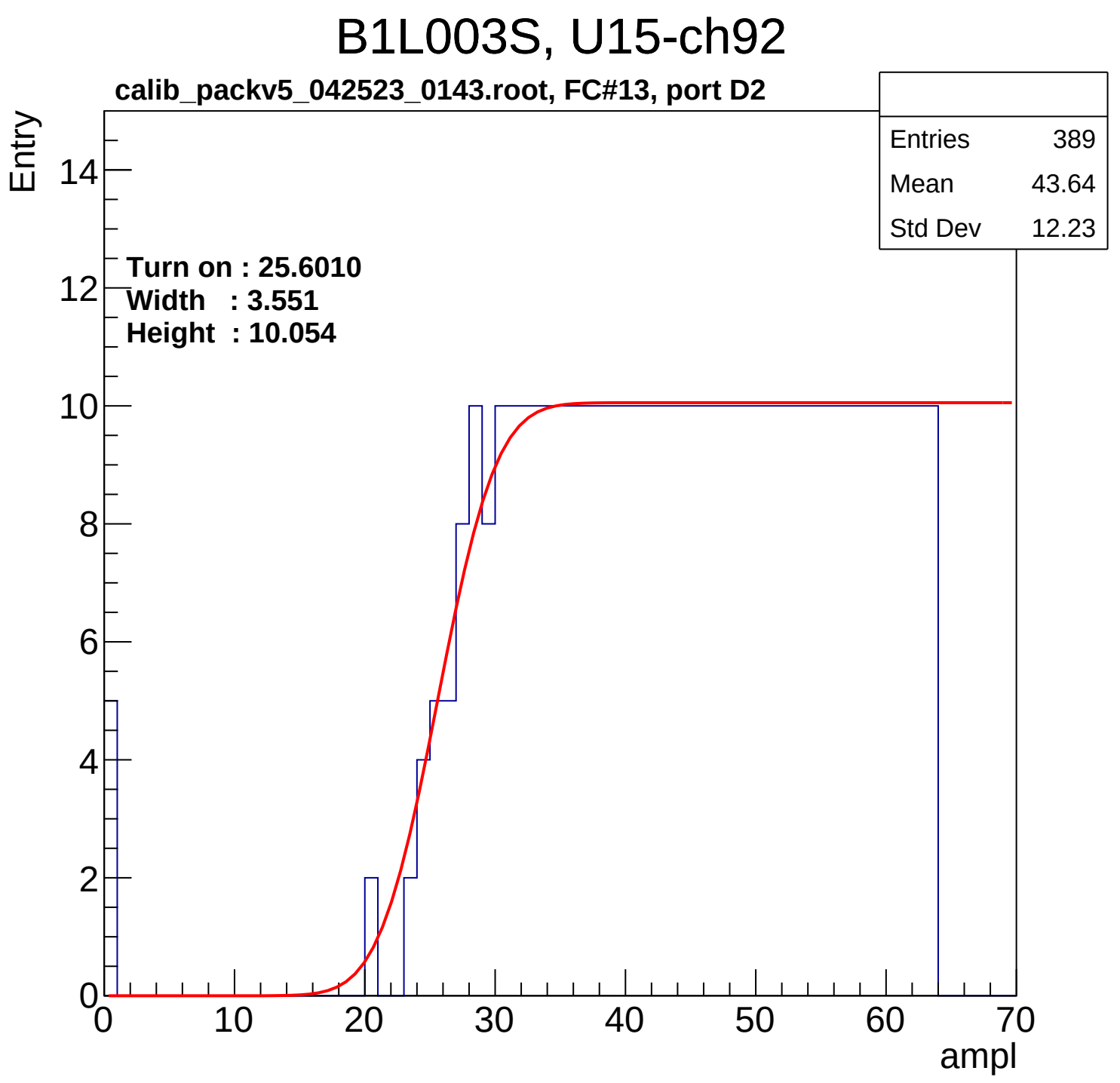
B1L003S, U15-ch92
calib_packv5_042523_0143.root, FC#13, port D2
Entries 389
Mean 43.64
Std Dev 12.23
Turn on : 25.6010
Width : 3.551
Height : 10.054
Entry
ampl
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6
8
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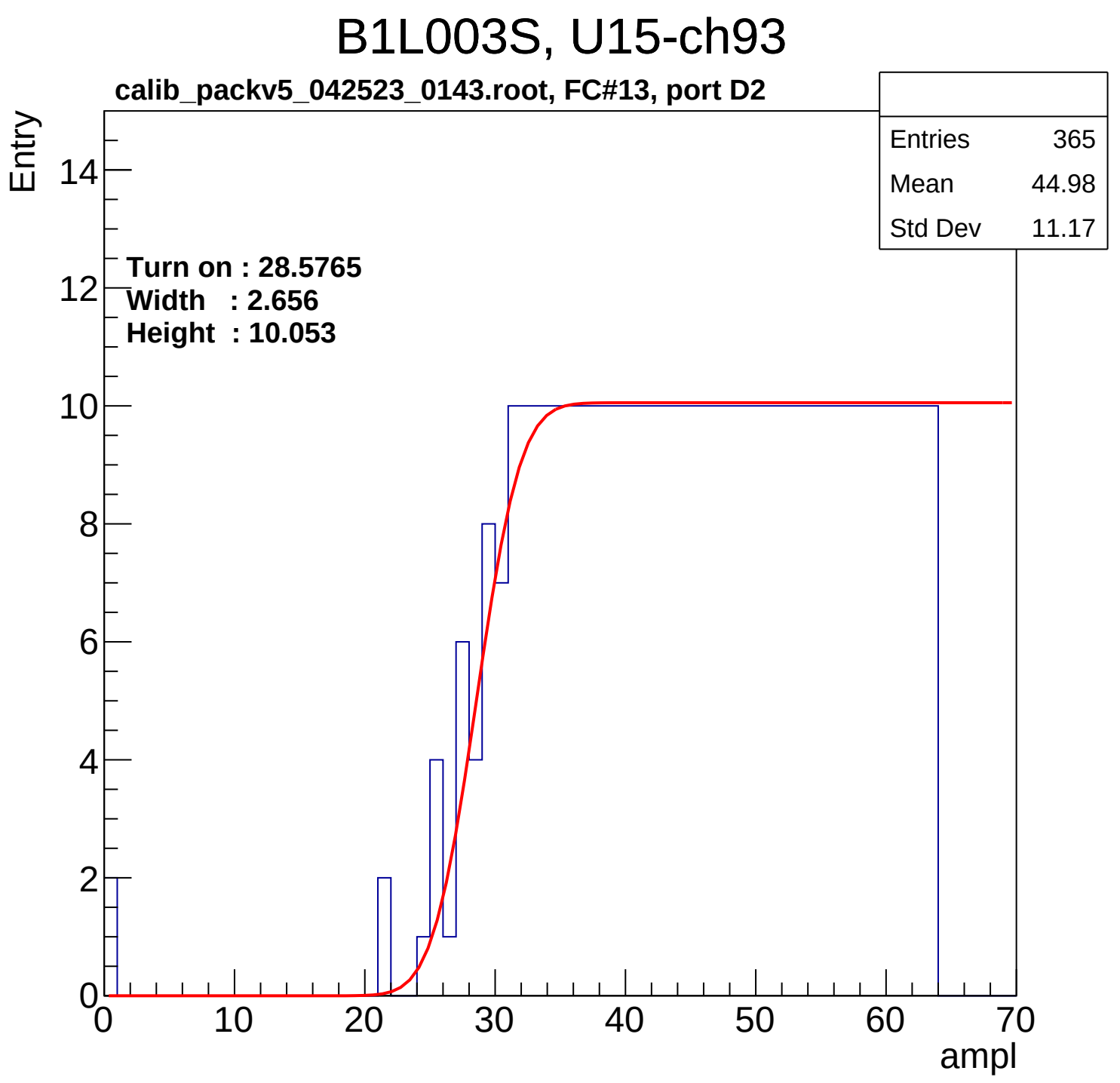
B1L003S, U15-ch93
calib_packv5_042523_0143.root, FC#13, port D2
Entries 365
Mean 44.98
Std Dev 11.17
Turn on : 28.5765
Width : 2.656
Height : 10.053
Entry
ampl
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6
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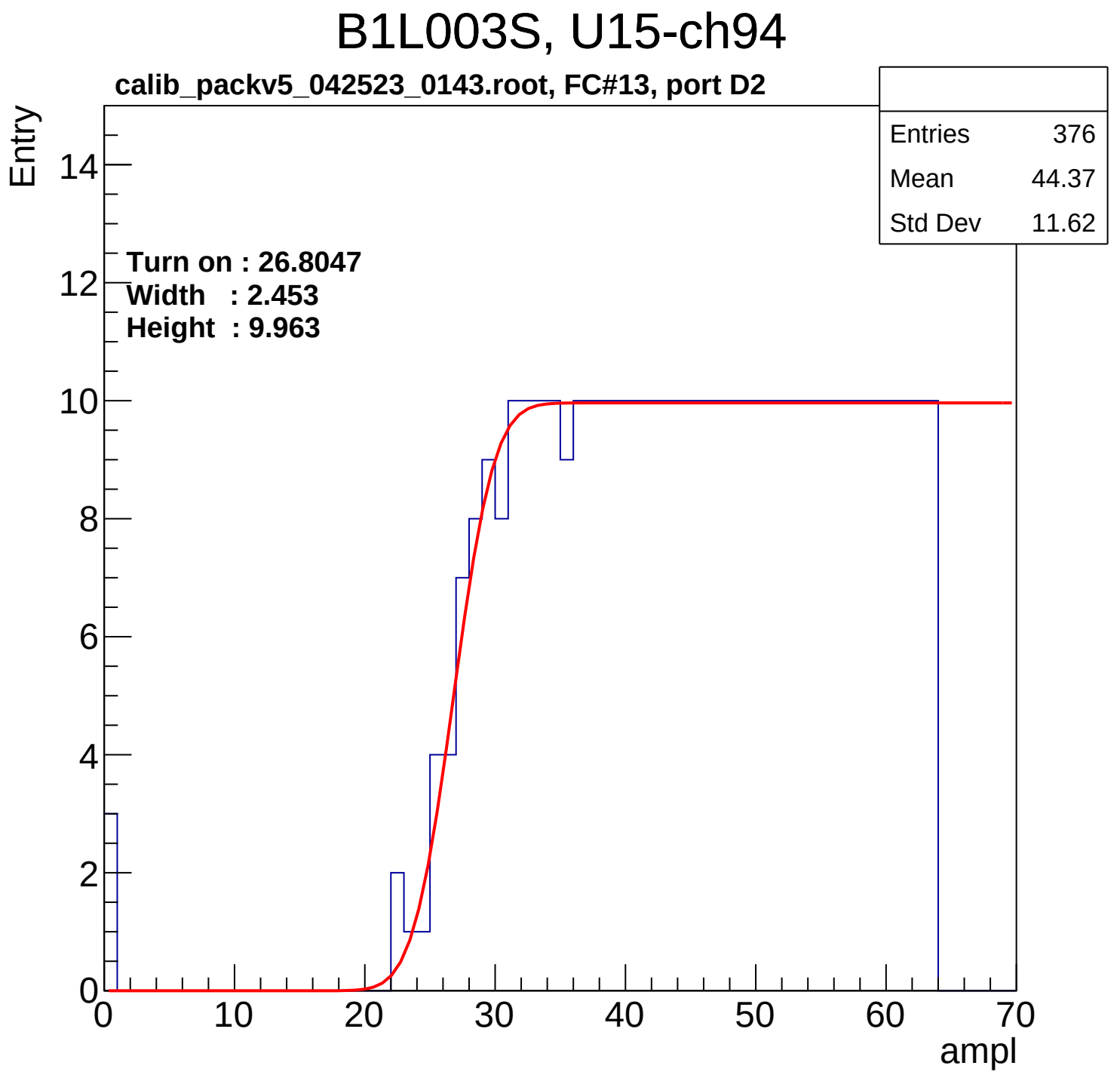
B1L003S, U15-ch94
calib_packv5_042523_0143.root, FC#13, port D2
Entries 376
Mean 44.37
Std Dev 11.62
Turn on : 26.8047
Width : 2.453
Height : 9.963
Entry
ampl
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2
4
6
8
10
12
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0
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60
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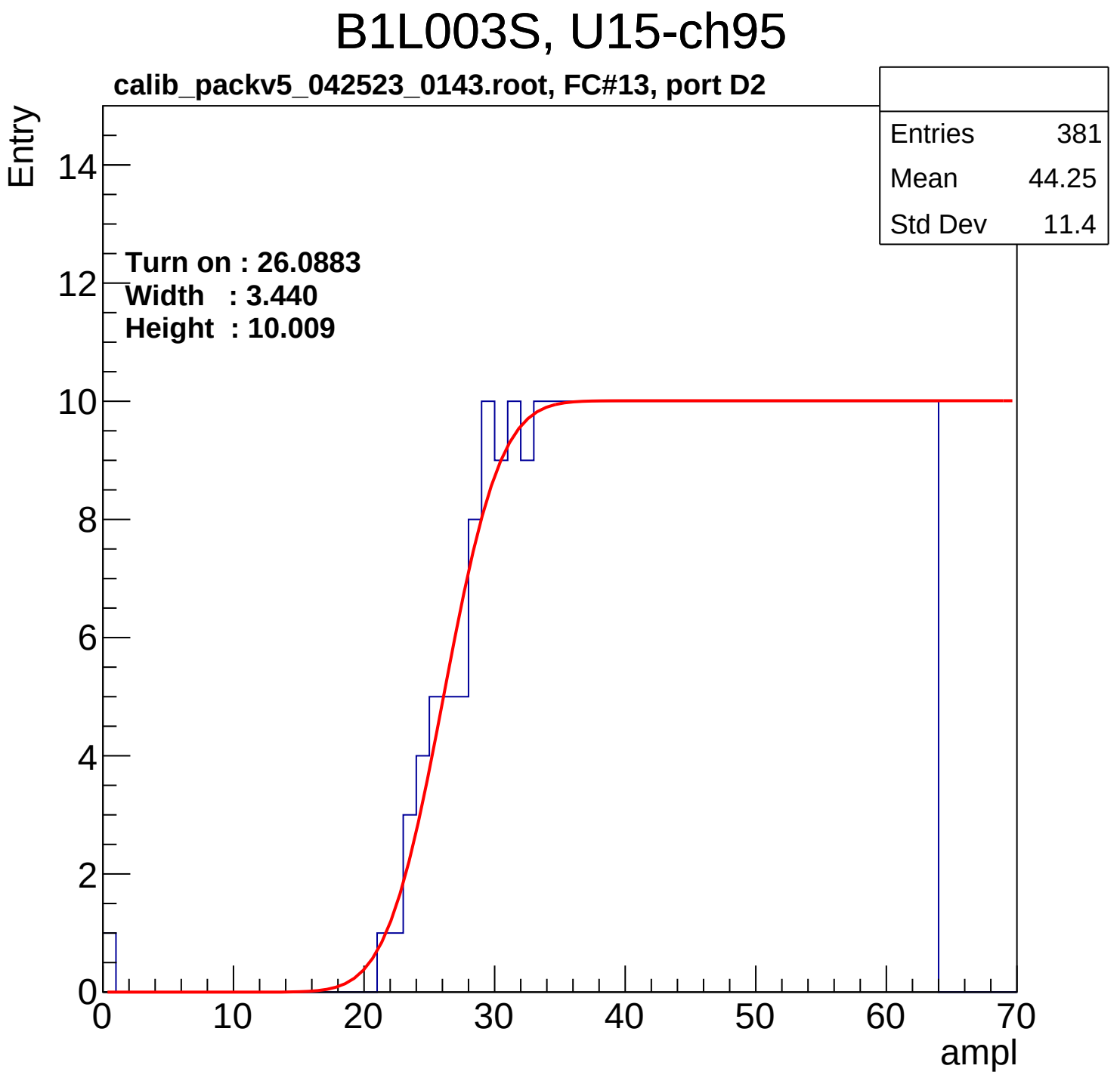
B1L003S, U15-ch95
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 44.25
Std Dev 11.4
Turn on : 26.0883
Width : 3.440
Height : 10.009
Entry
ampl
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6
8
10
12
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0
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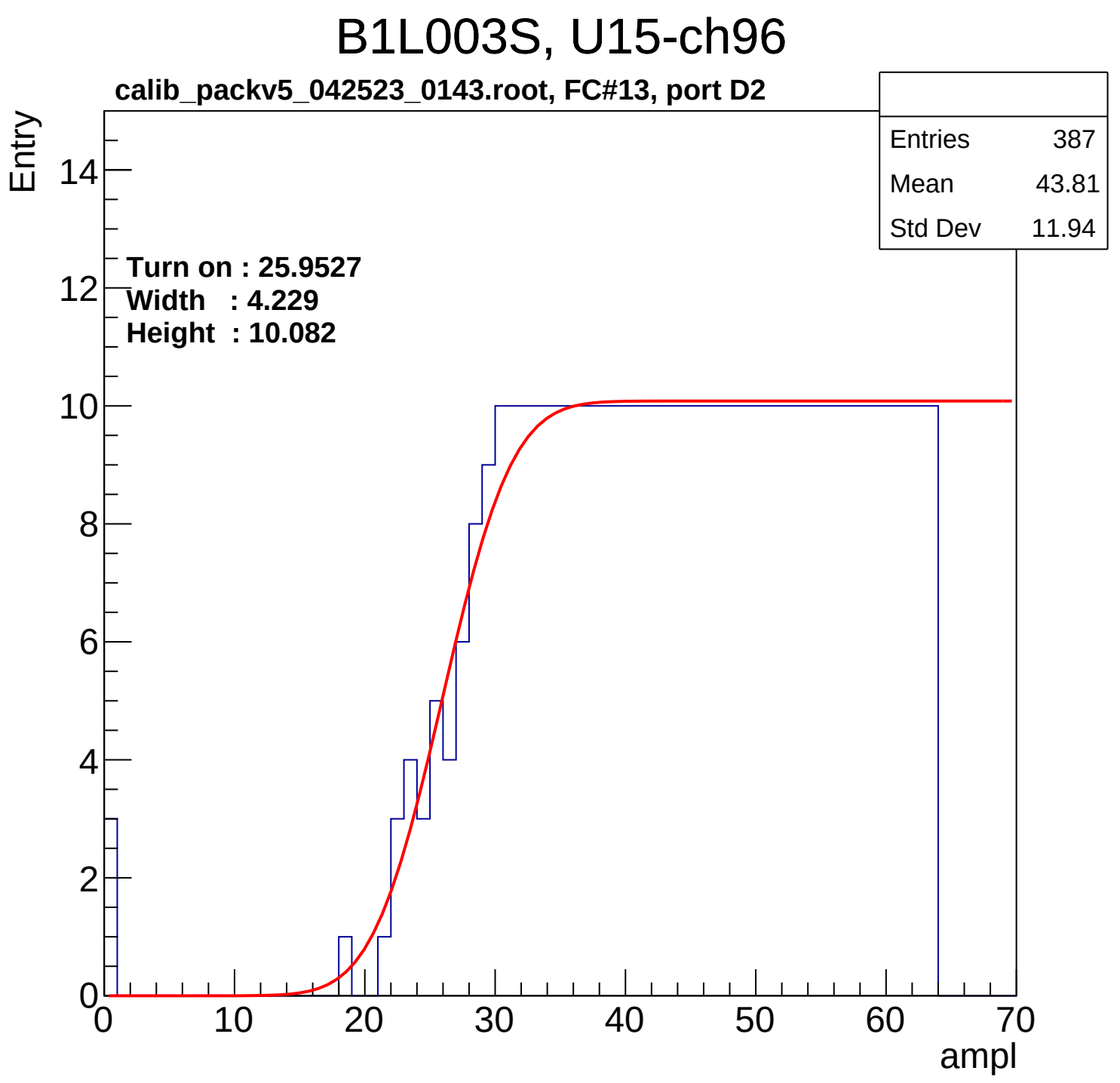
B1L003S, U15-ch96
calib_packv5_042523_0143.root, FC#13, port D2
Entries 387
Mean 43.81
Std Dev 11.94
Turn on : 25.9527
Width : 4.229
Height : 10.082
Entry
ampl
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6
8
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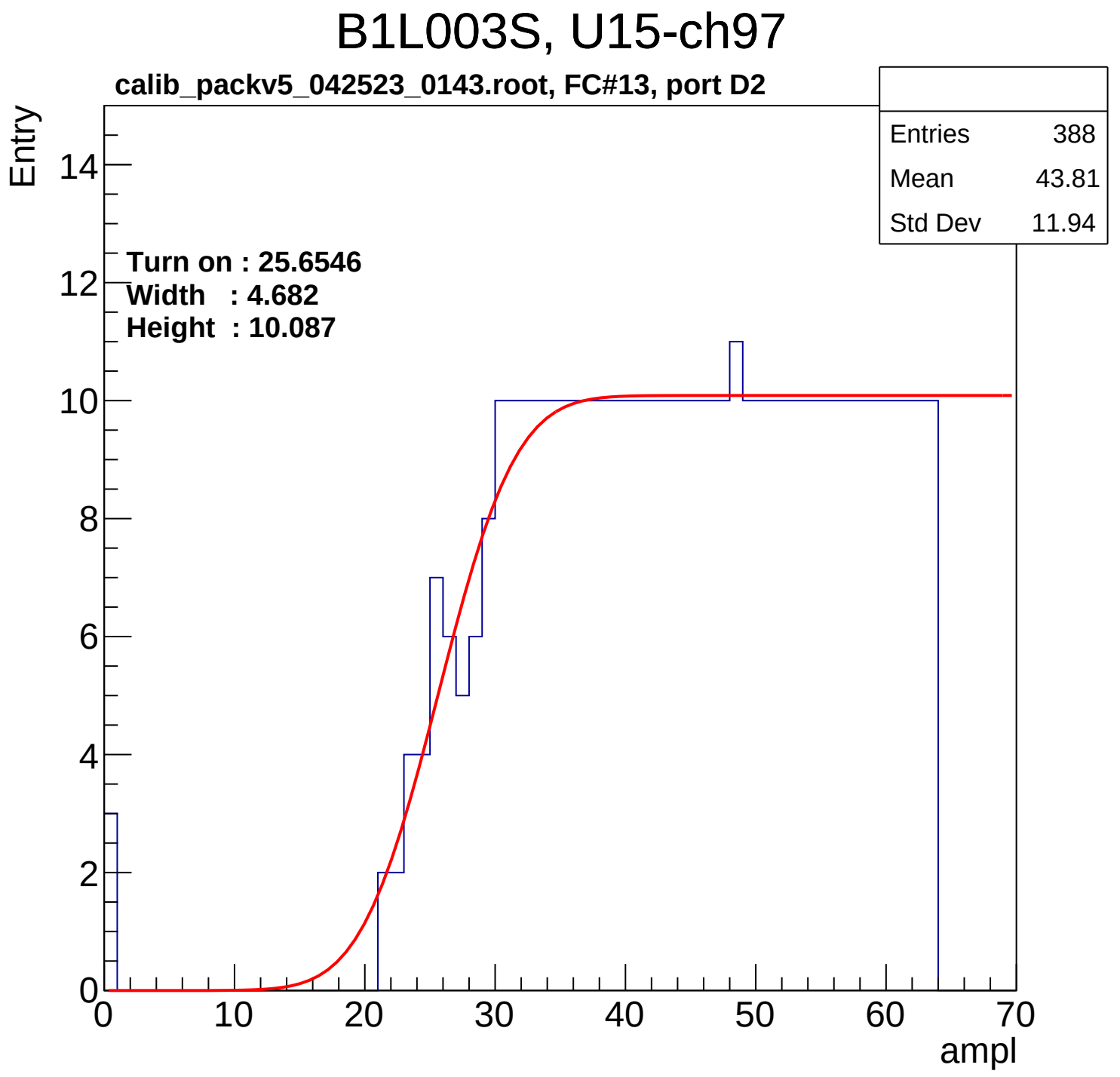
B1L003S, U15-ch97
calib_packv5_042523_0143.root, FC#13, port D2
Entries 388
Mean 43.81
Std Dev 11.94
Turn on : 25.6546
Width : 4.682
Height : 10.087
Entry
ampl
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6
8
10
12
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0
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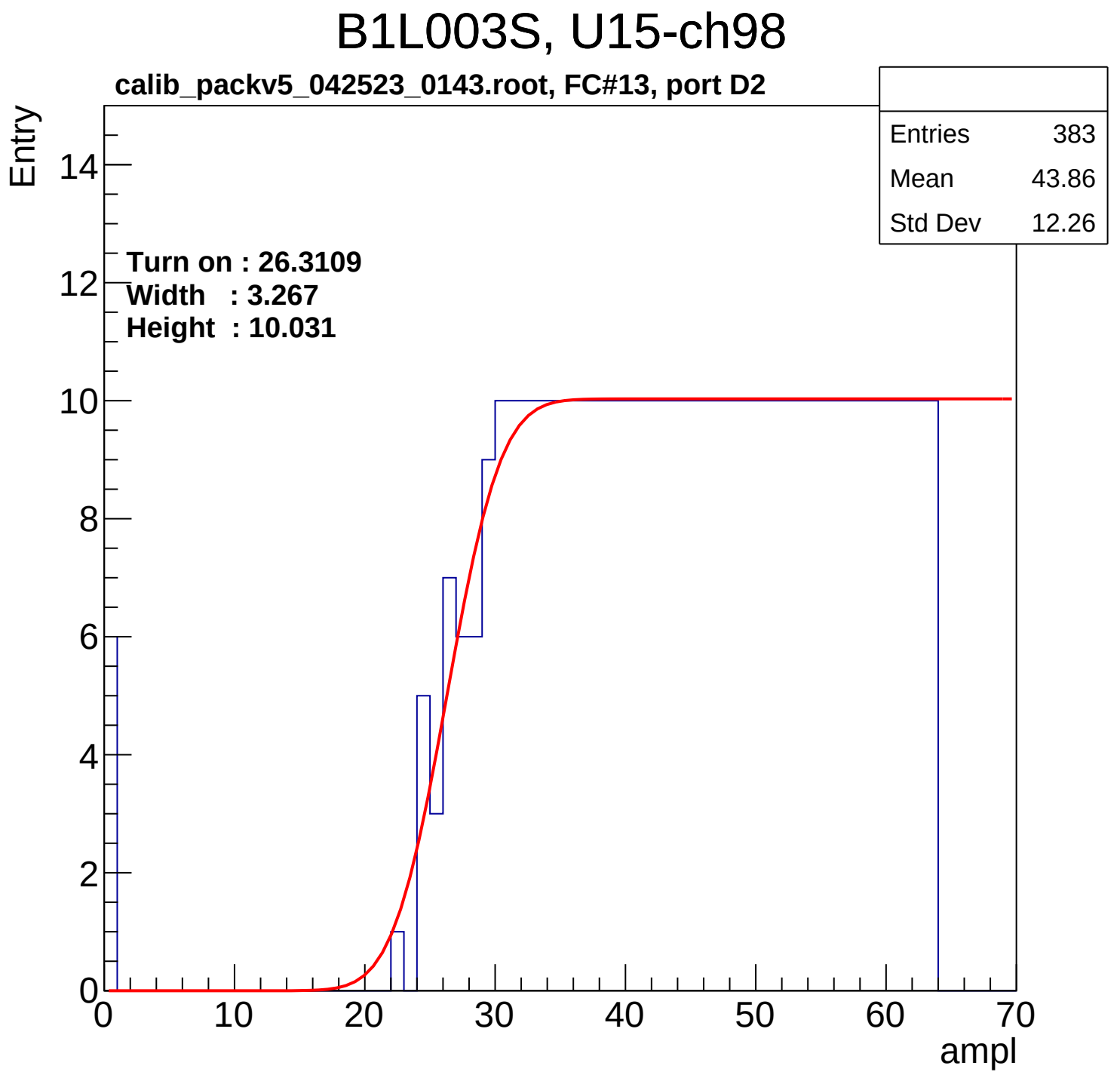
B1L003S, U15-ch98
calib_packv5_042523_0143.root, FC#13, port D2
Entries 383
Mean 43.86
Std Dev 12.26
Turn on : 26.3109
Width : 3.267
Height : 10.031
Entry
ampl
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2
4
6
8
10
12
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0
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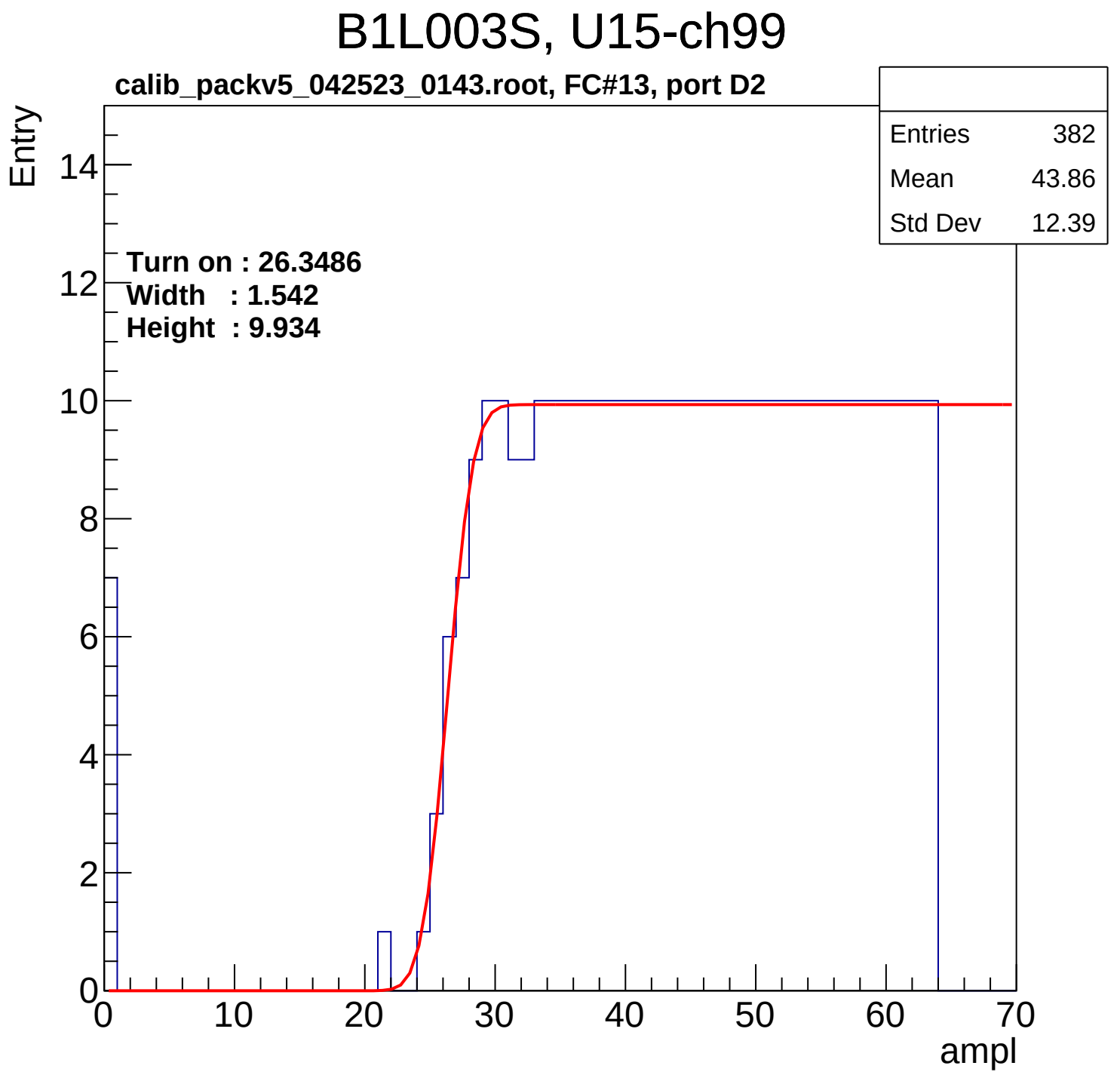
B1L003S, U15-ch99
calib_packv5_042523_0143.root, FC#13, port D2
Entries 382
Mean 43.86
Std Dev 12.39
Turn on : 26.3486
Width : 1.542
Height : 9.934
Entry
ampl
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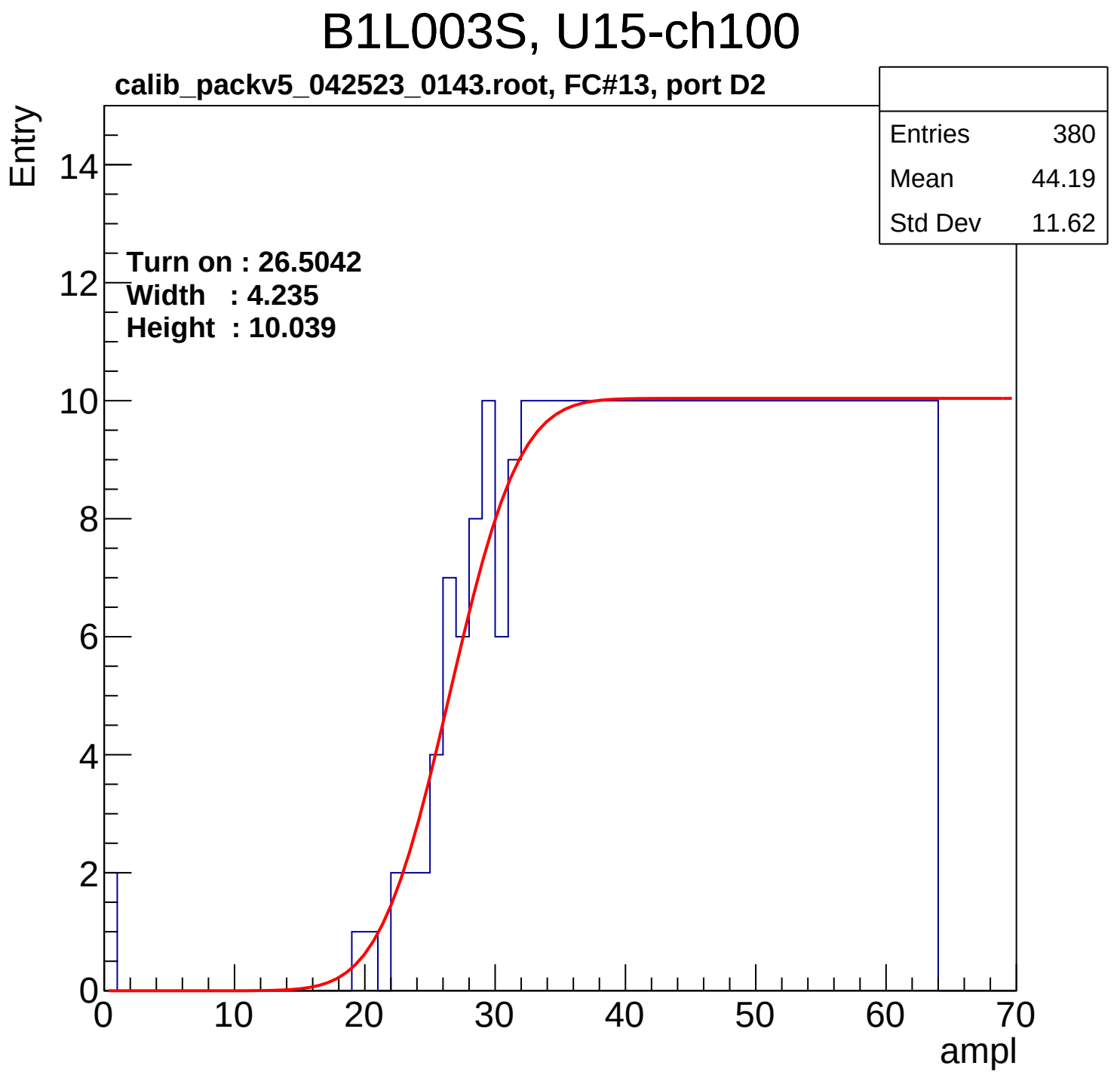
B1L003S, U15-ch100
calib_packv5_042523_0143.root, FC#13, port D2
Entries 380
Mean 44.19
Std Dev 11.62
Turn on : 26.5042
Width : 4.235
Height : 10.039
Entry
ampl
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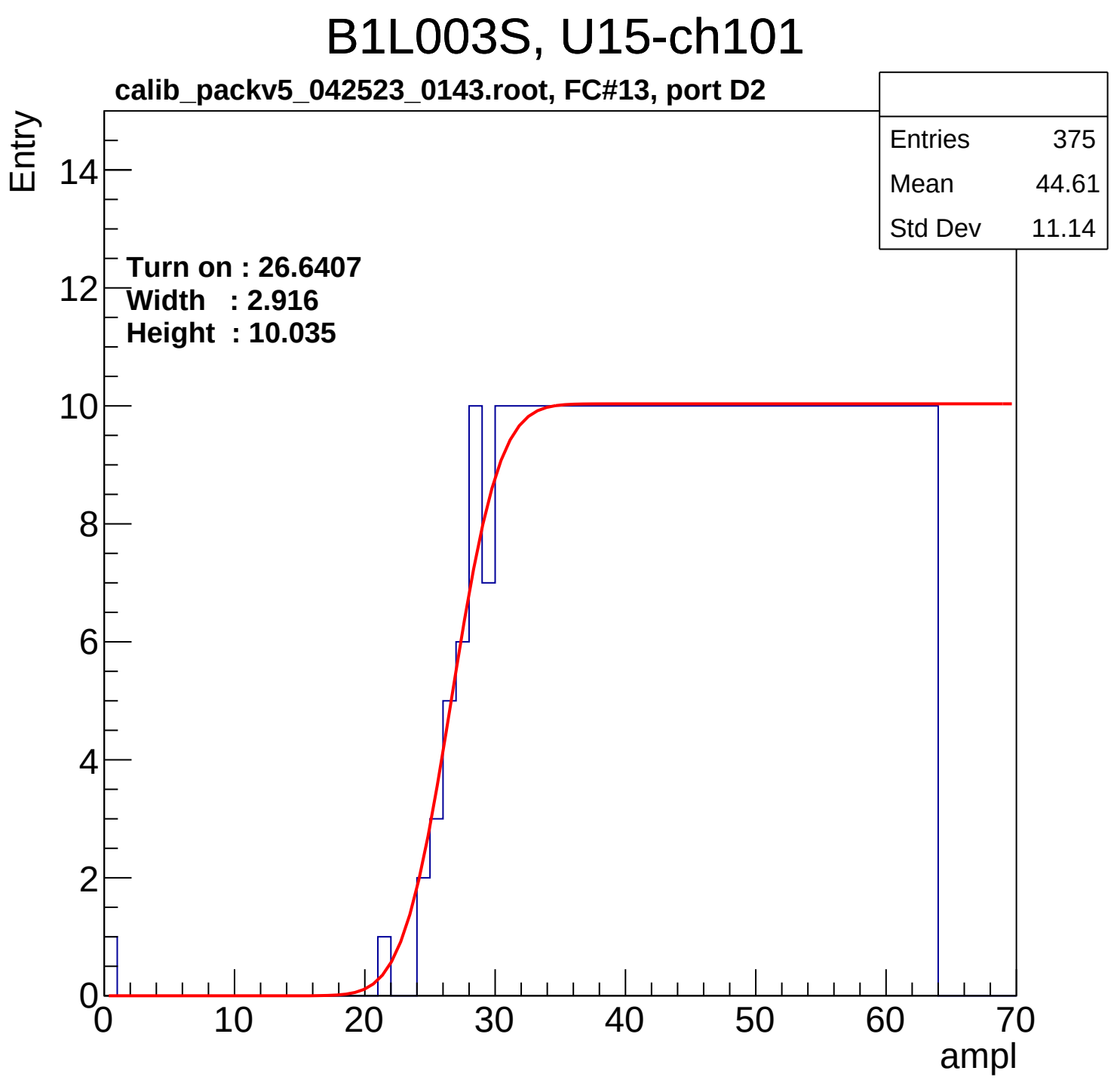
B1L003S, U15-ch101
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.61
Std Dev 11.14
Turn on : 26.6407
Width : 2.916
Height : 10.035
Entry
ampl
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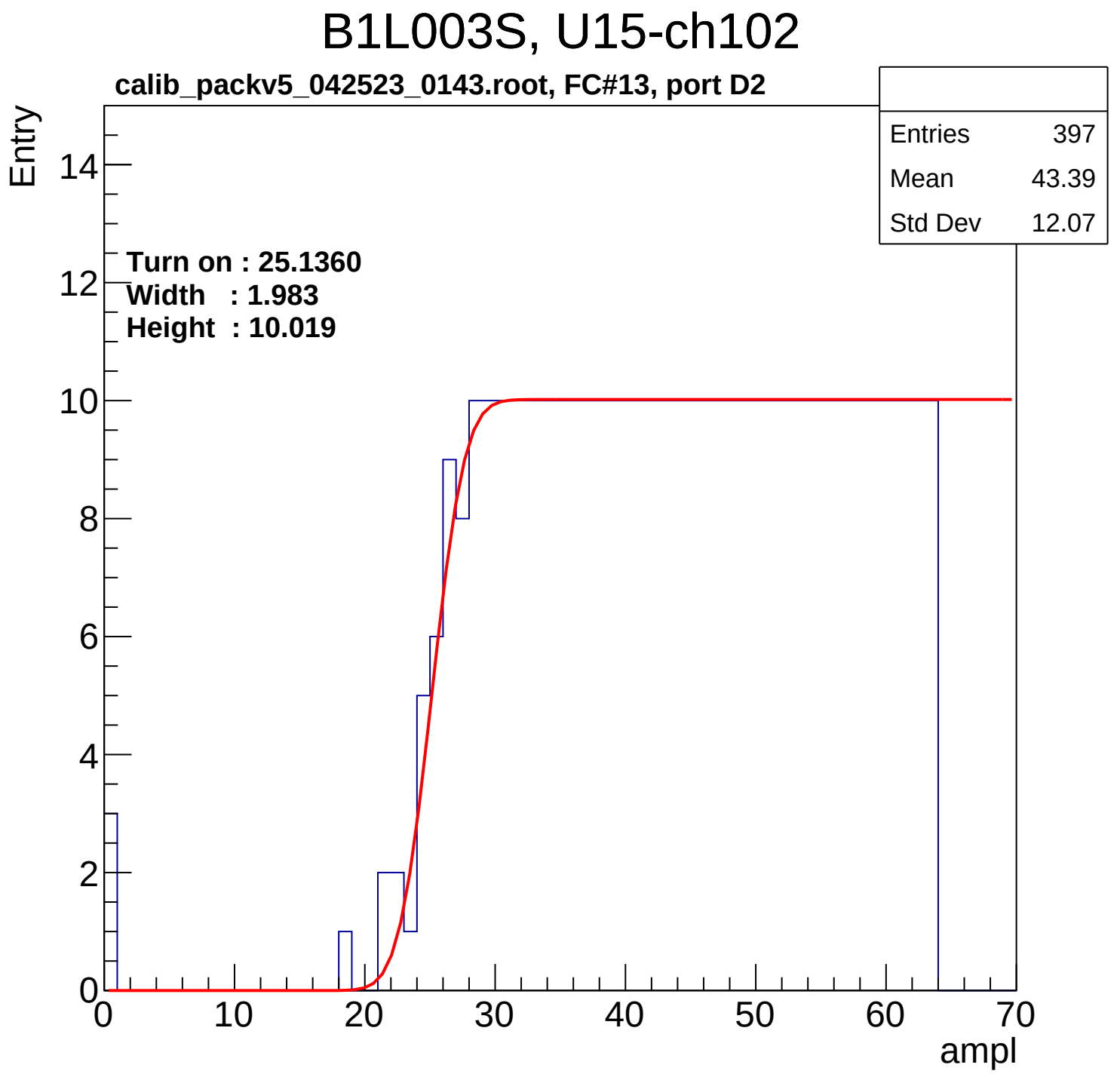
B1L003S, U15-ch102
calib_packv5_042523_0143.root, FC#13, port D2
Entries 397
Mean 43.39
Std Dev 12.07
Turn on : 25.1360
Width : 1.983
Height : 10.019
Entry
ampl
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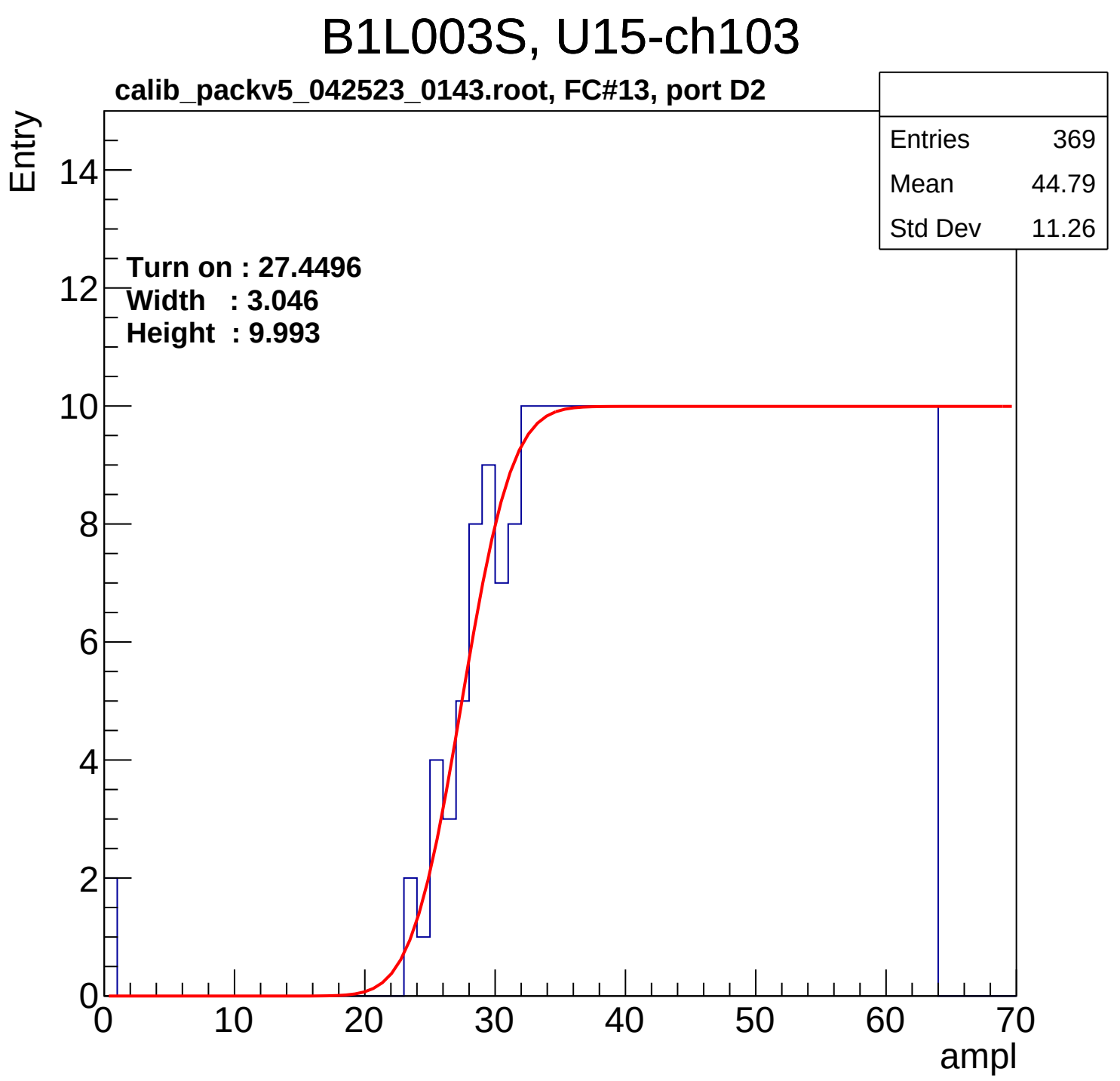
B1L003S, U15-ch103
calib_packv5_042523_0143.root, FC#13, port D2
Entries 369
Mean 44.79
Std Dev 11.26
Turn on : 27.4496
Width : 3.046
Height : 9.993
Entry
ampl
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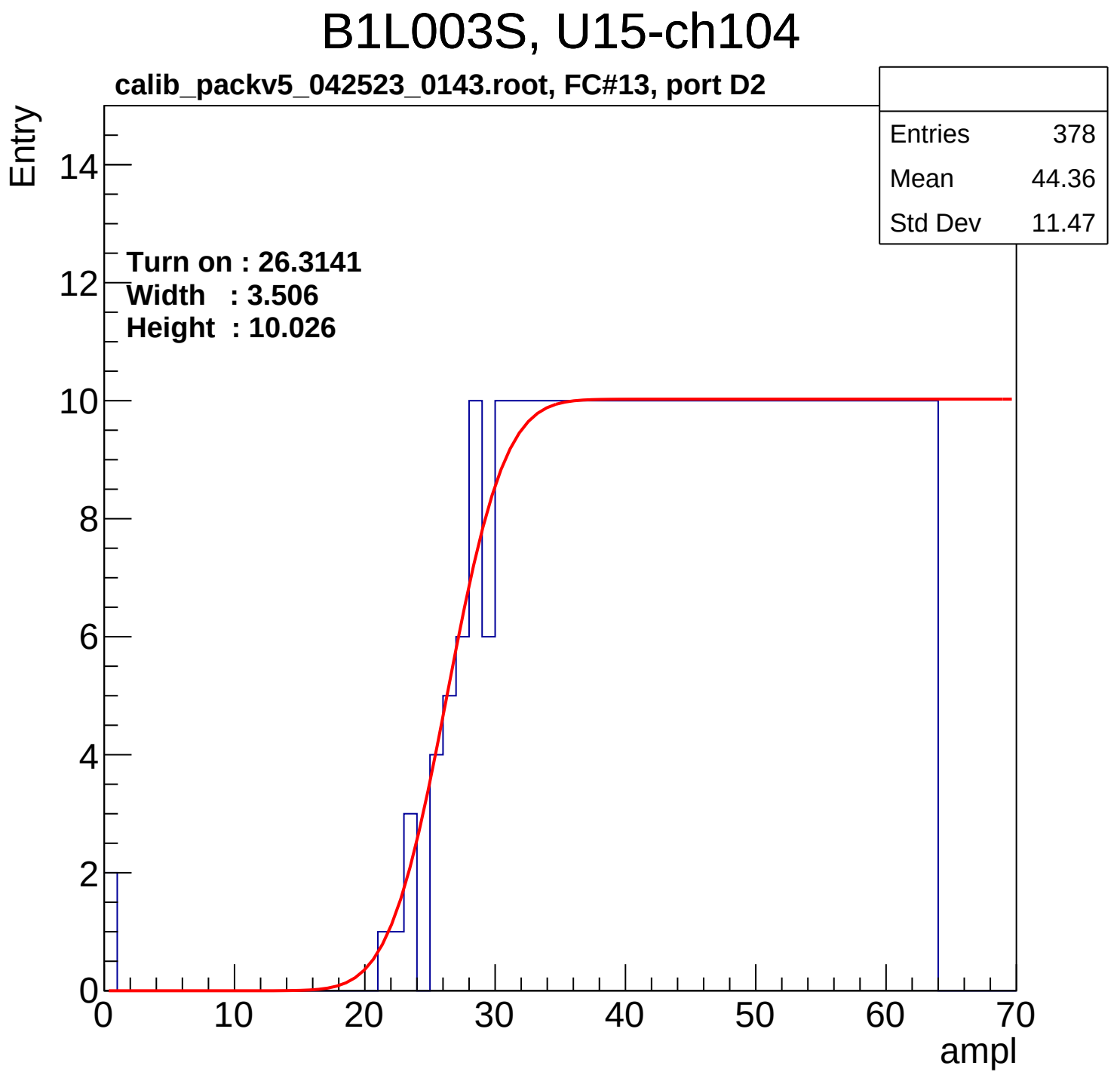
B1L003S, U15-ch104
calib_packv5_042523_0143.root, FC#13, port D2
Entries 378
Mean 44.36
Std Dev 11.47
Turn on : 26.3141
Width : 3.506
Height : 10.026
Entry
ampl
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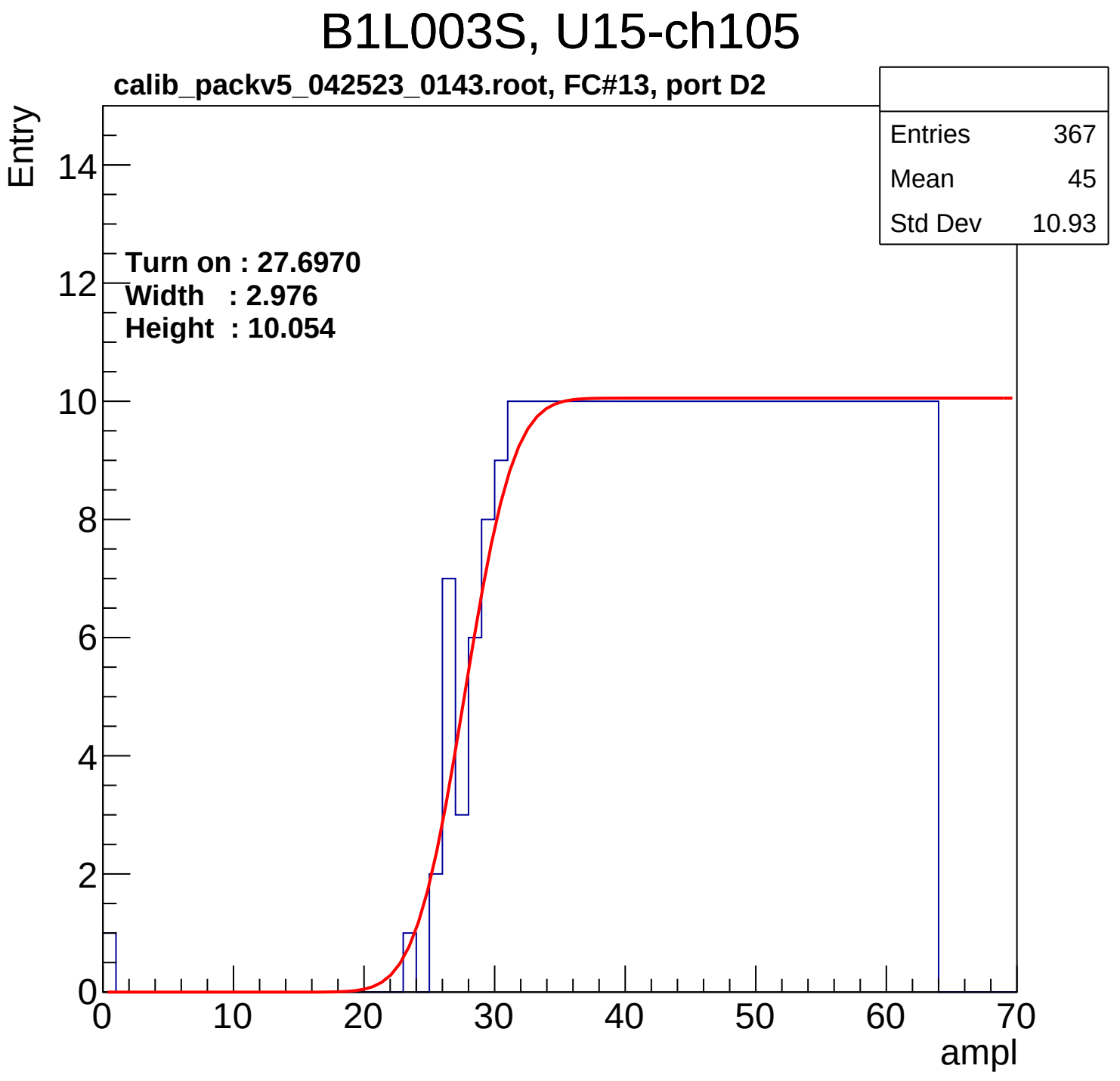
B1L003S, U15-ch105
calib_packv5_042523_0143.root, FC#13, port D2
Entries 367
Mean 45
Std Dev 10.93
Turn on : 27.6970
Width : 2.976
Height : 10.054
Entry
ampl
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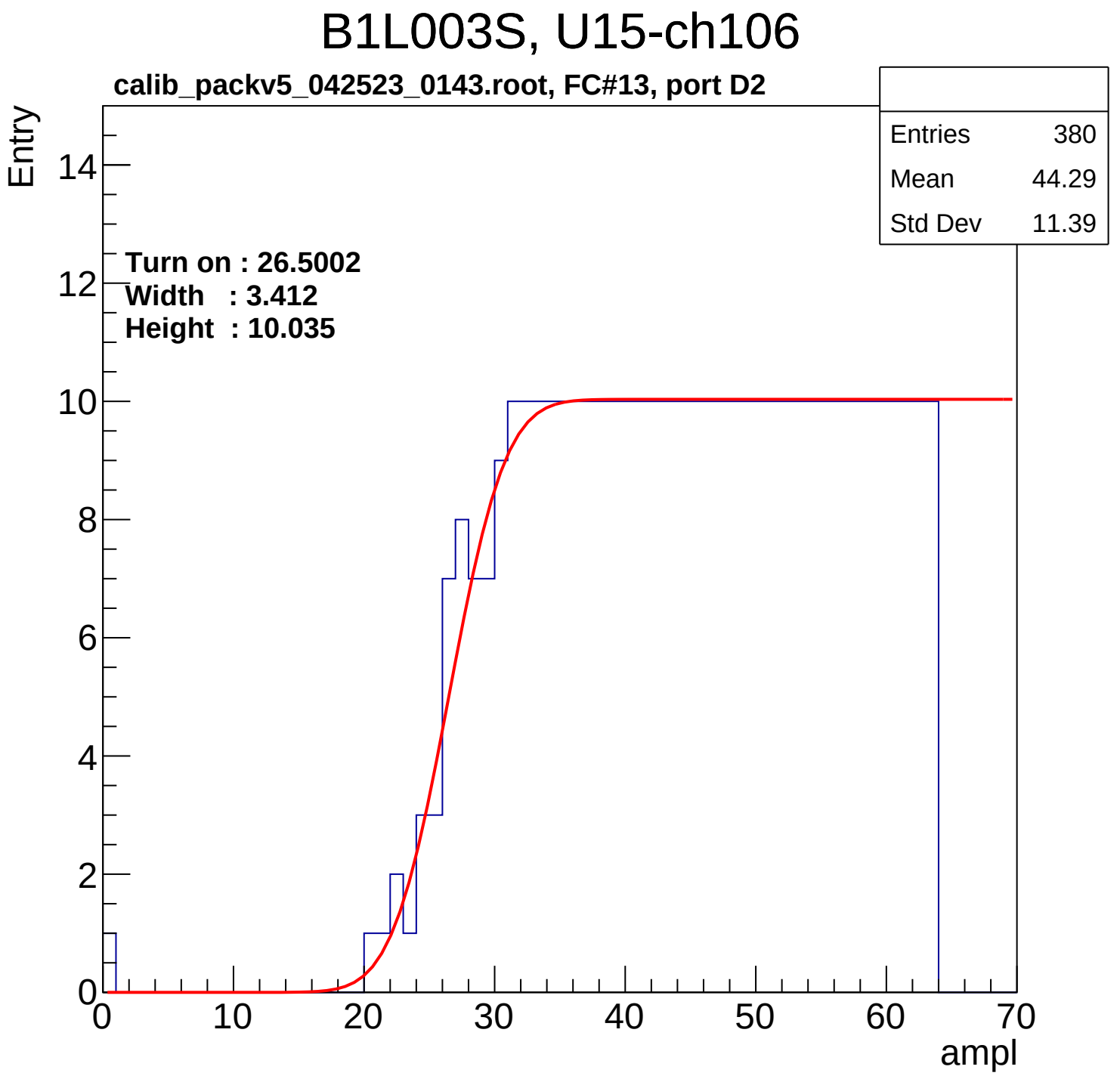
B1L003S, U15-ch106
calib_packv5_042523_0143.root, FC#13, port D2
Entries 380
Mean 44.29
Std Dev 11.39
Turn on : 26.5002
Width : 3.412
Height : 10.035
Entry
ampl
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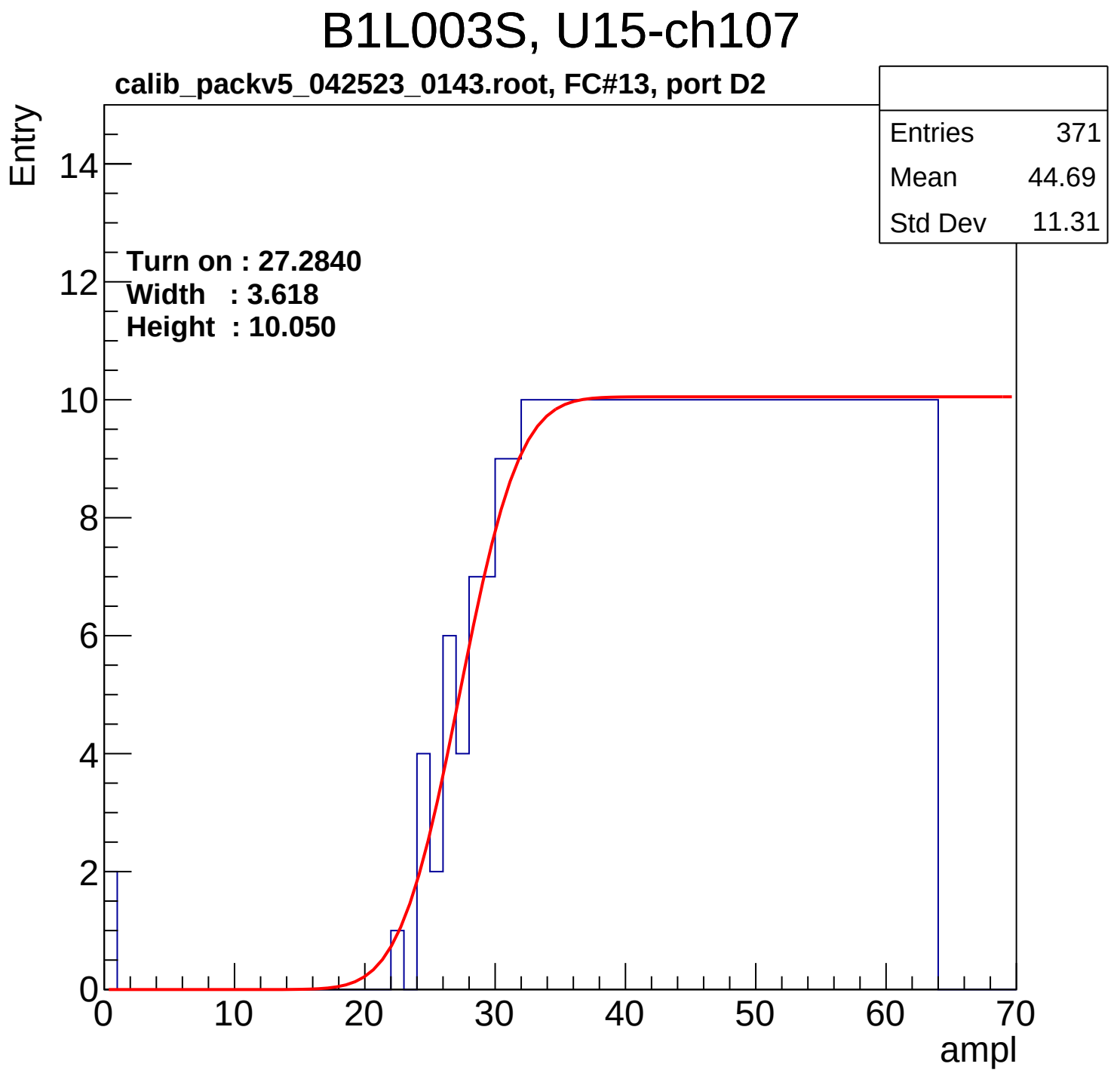
B1L003S, U15-ch107
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.69
Std Dev 11.31
Turn on : 27.2840
Width : 3.618
Height : 10.050
Entry
ampl
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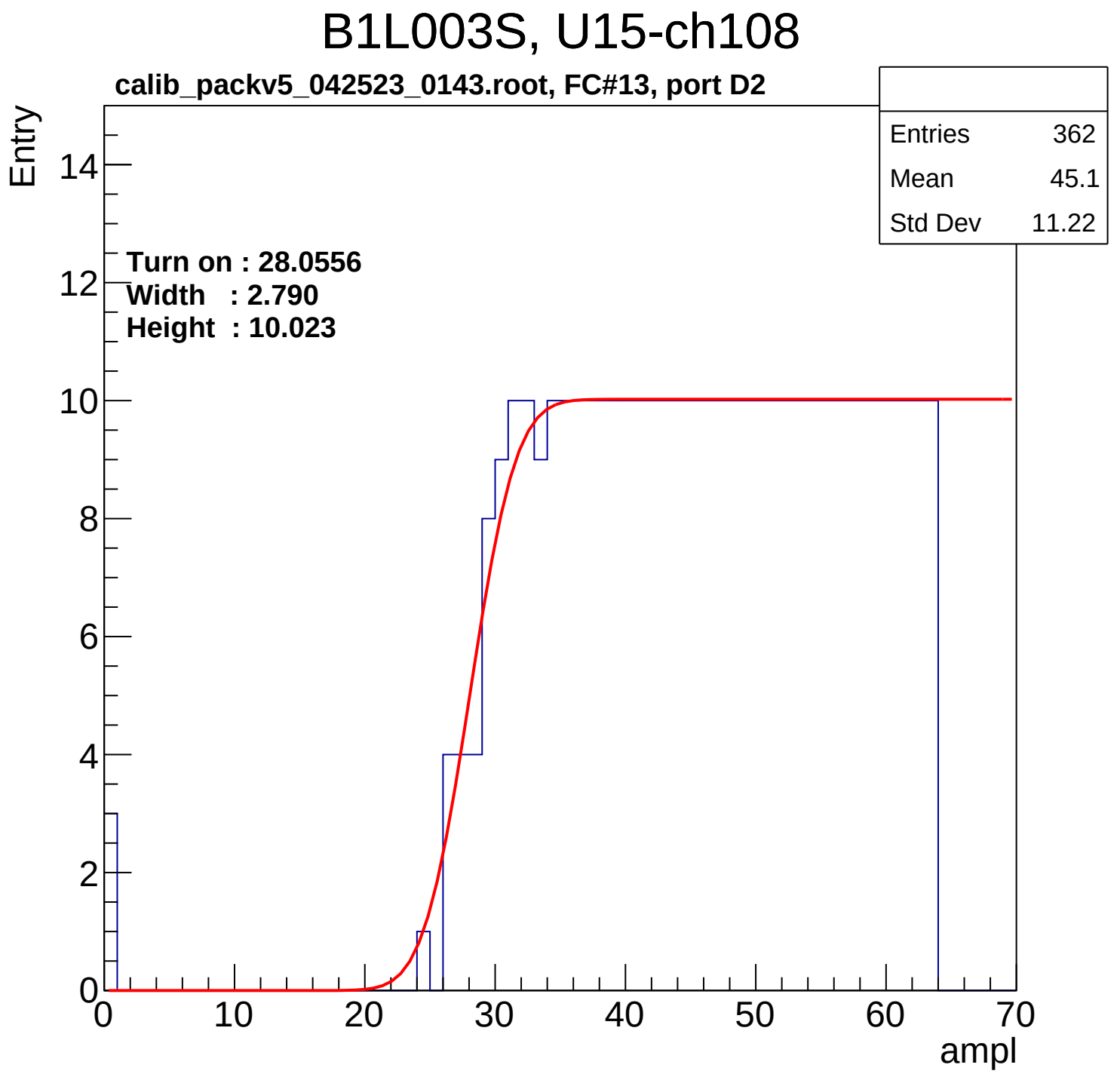
B1L003S, U15-ch108
calib_packv5_042523_0143.root, FC#13, port D2
Entries 362
Mean 45.1
Std Dev 11.22
Turn on : 28.0556
Width : 2.790
Height : 10.023
Entry
ampl
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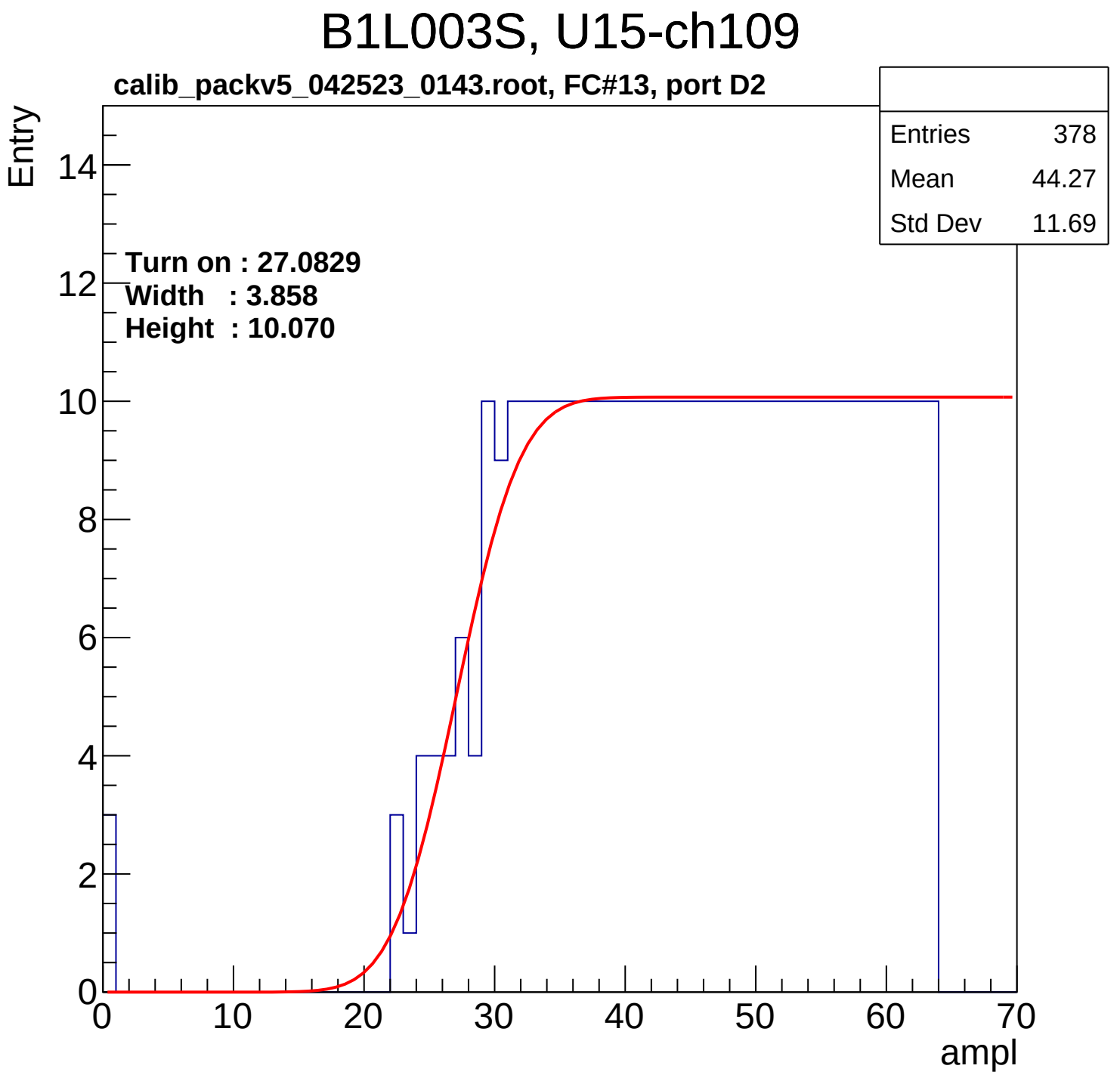
B1L003S, U15-ch109
calib_packv5_042523_0143.root, FC#13, port D2
Entries 378
Mean 44.27
Std Dev 11.69
Turn on : 27.0829
Width : 3.858
Height : 10.070
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ampl
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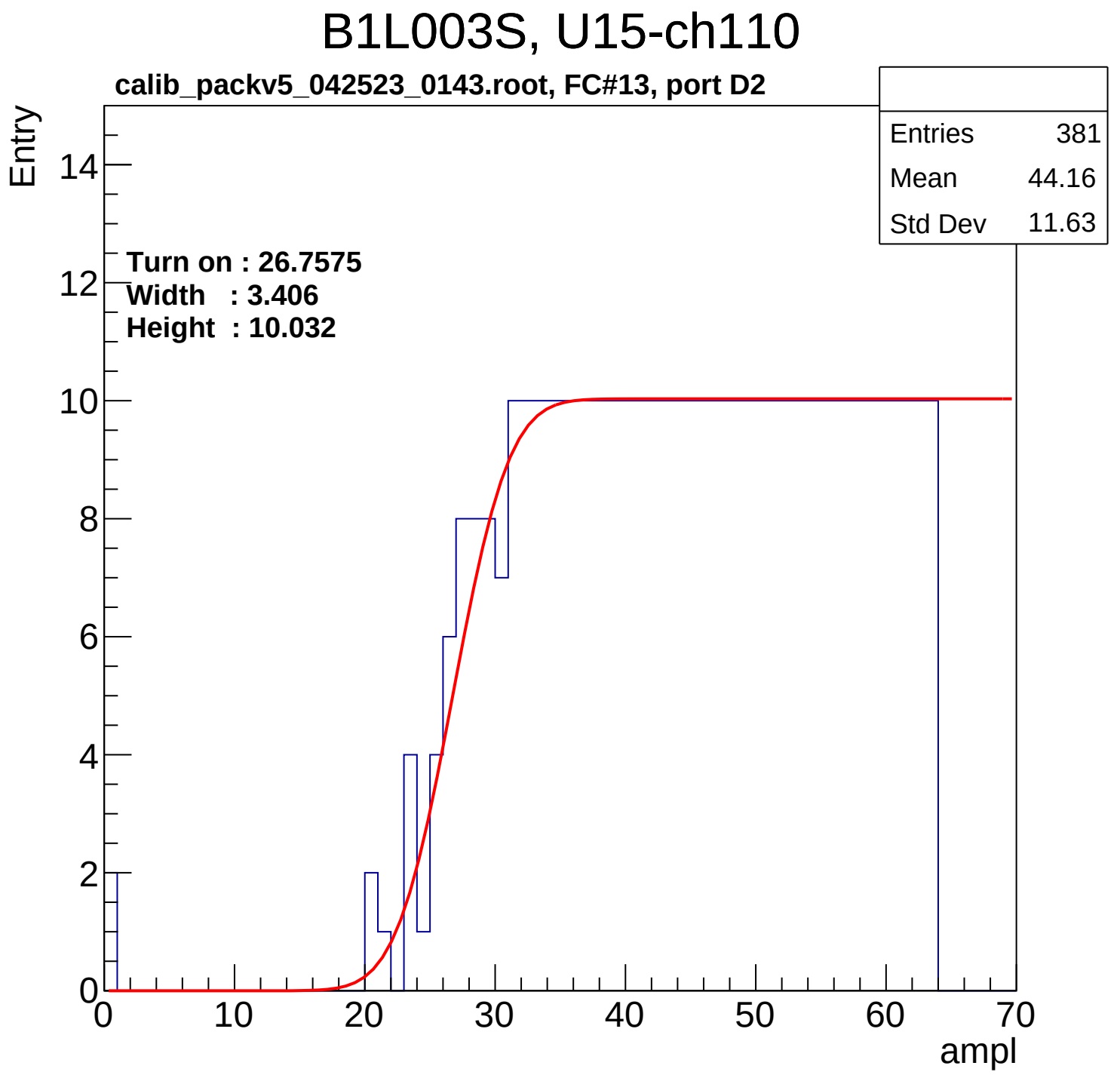
B1L003S, U15-ch110
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 44.16
Std Dev 11.63
Turn on : 26.7575
Width : 3.406
Height : 10.032
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ampl
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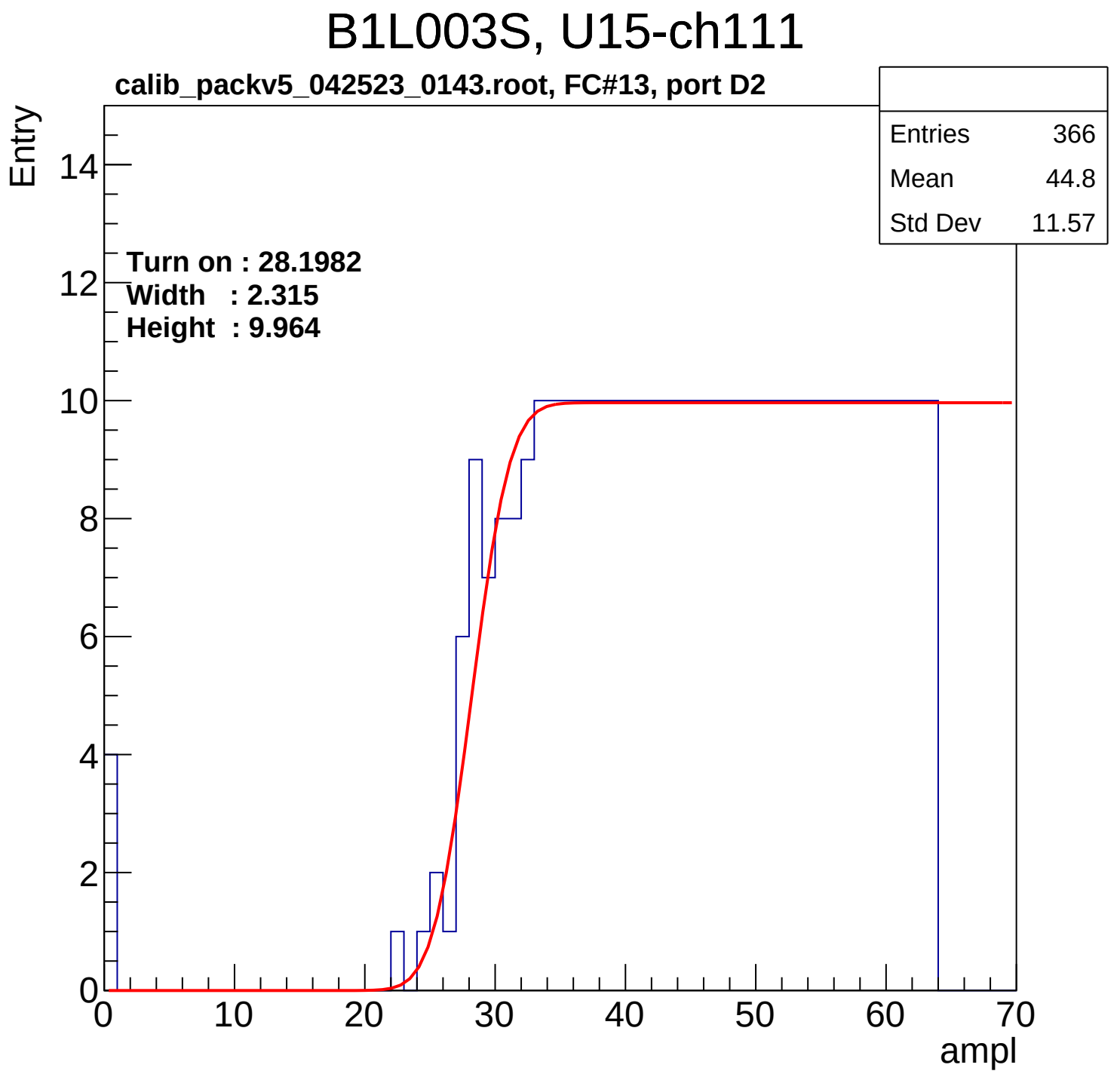
B1L003S, U15-ch111
calib_packv5_042523_0143.root, FC#13, port D2
Entries 366
Mean 44.8
Std Dev 11.57
Turn on : 28.1982
Width : 2.315
Height : 9.964
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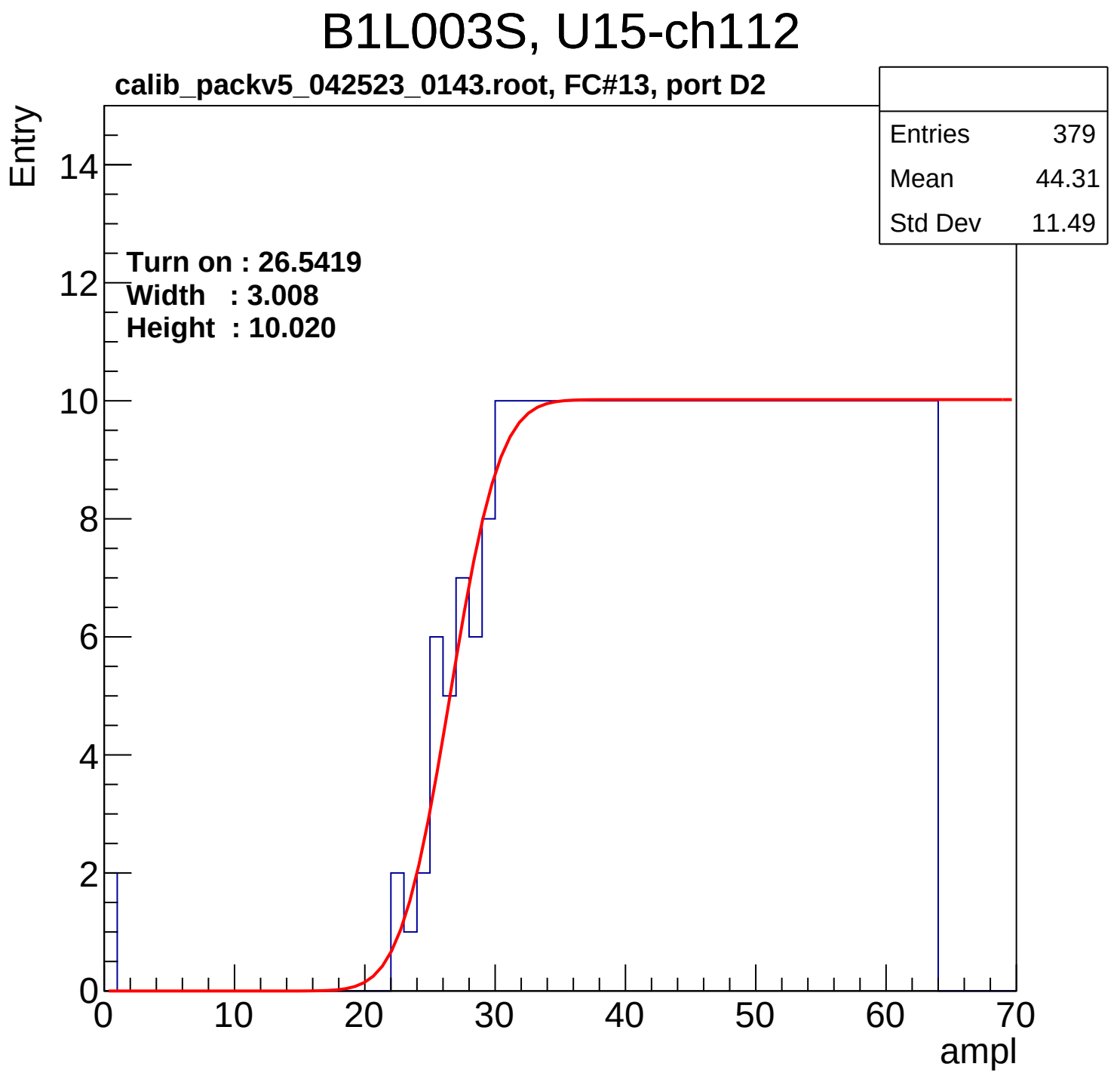
B1L003S, U15-ch112
calib_packv5_042523_0143.root, FC#13, port D2
Entries 379
Mean 44.31
Std Dev 11.49
Turn on : 26.5419
Width : 3.008
Height : 10.020
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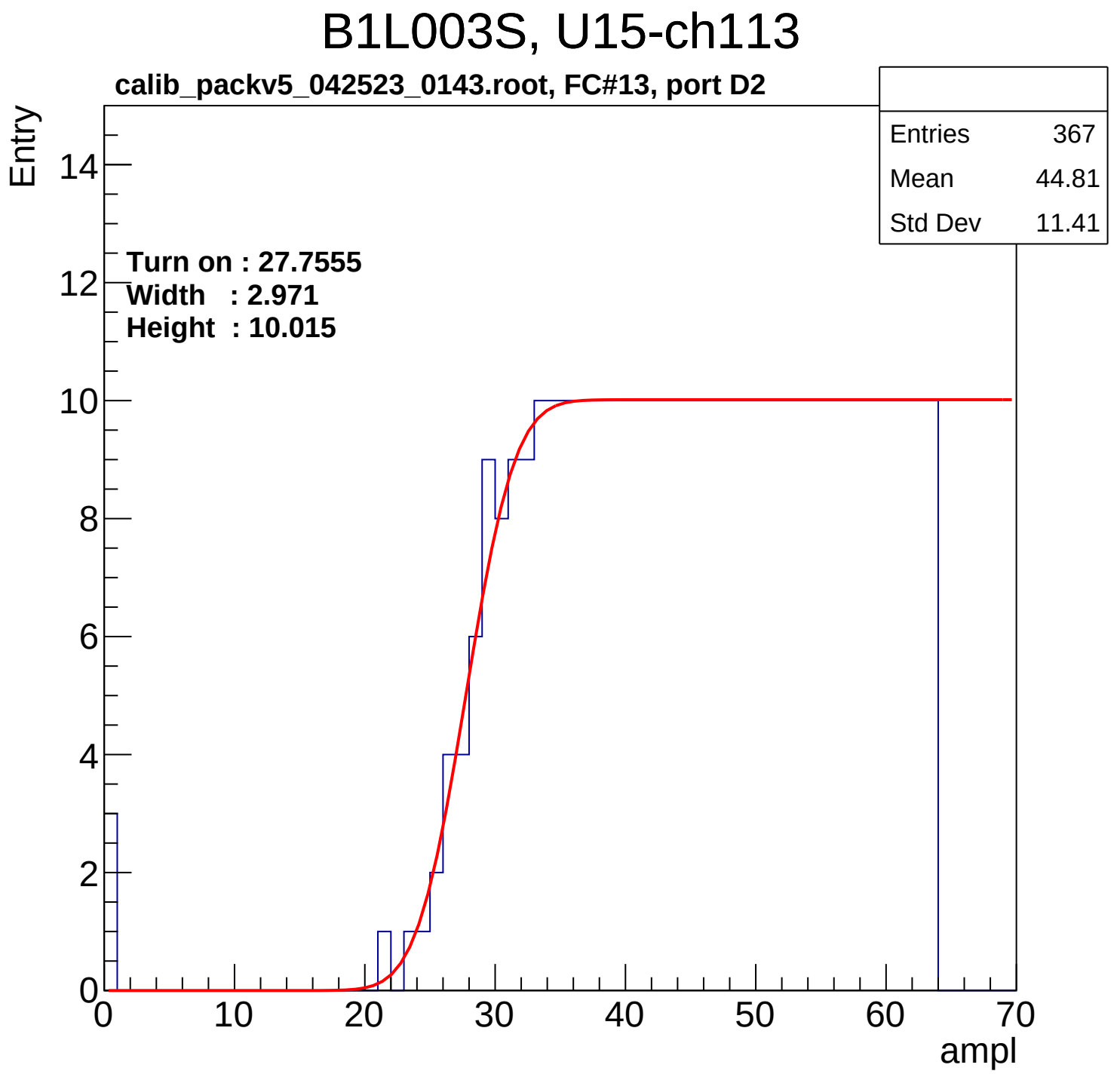
B1L003S, U15-ch113
calib_packv5_042523_0143.root, FC#13, port D2
Entries 367
Mean 44.81
Std Dev 11.41
Turn on : 27.7555
Width : 2.971
Height : 10.015
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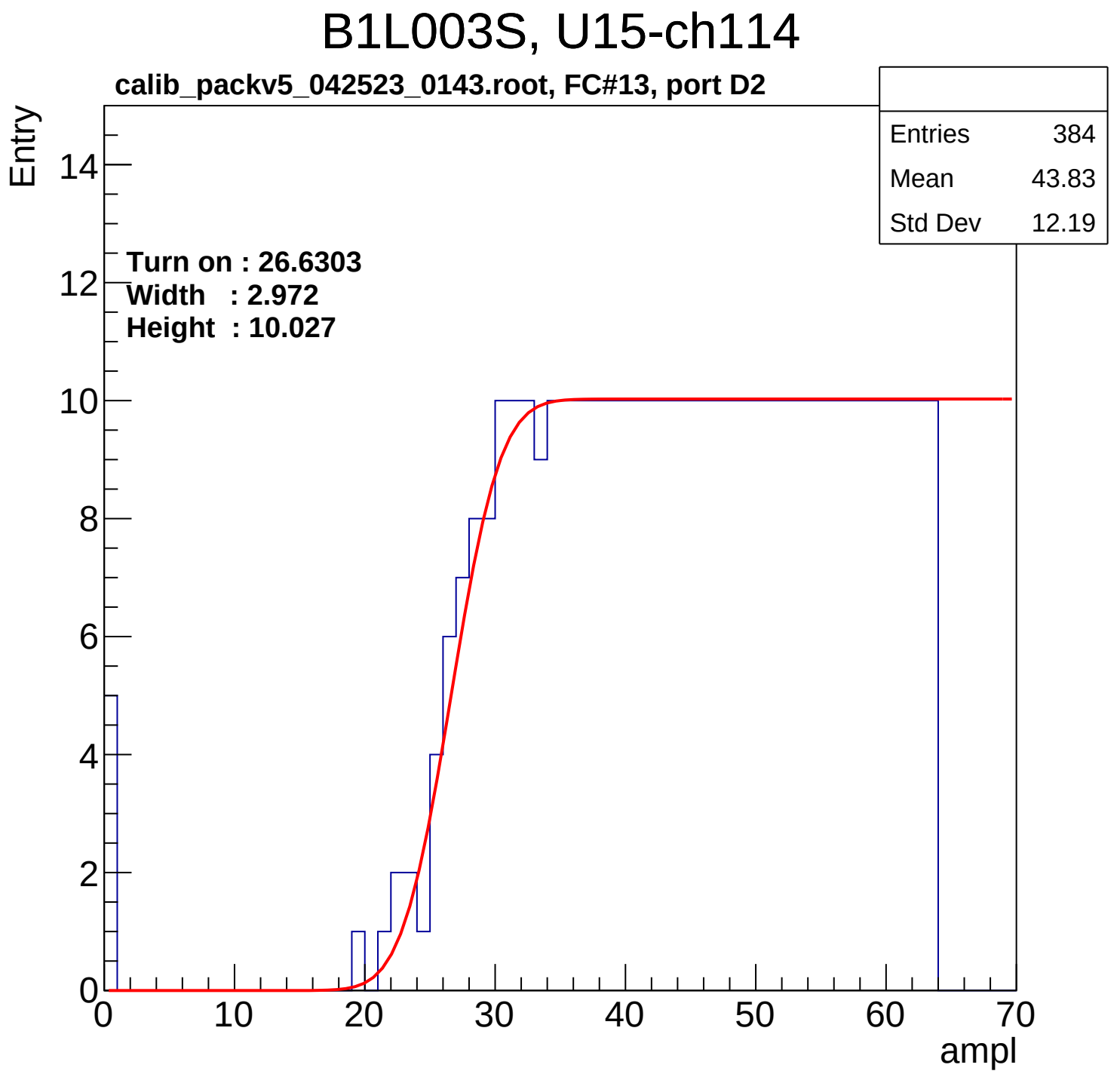
B1L003S, U15-ch114
calib_packv5_042523_0143.root, FC#13, port D2
Entries 384
Mean 43.83
Std Dev 12.19
Turn on : 26.6303
Width : 2.972
Height : 10.027
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ampl
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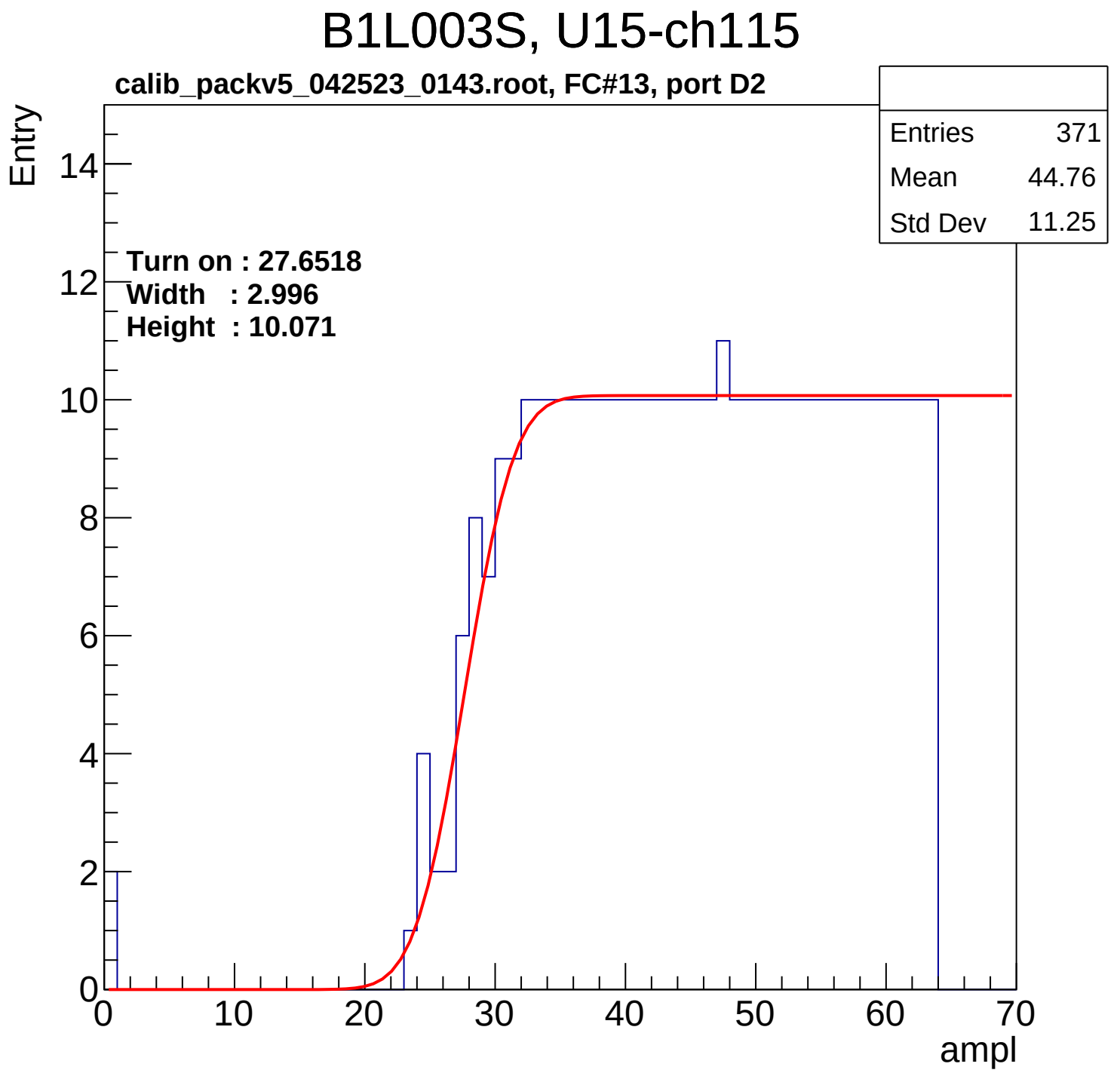
B1L003S, U15-ch115
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.76
Std Dev 11.25
Turn on : 27.6518
Width : 2.996
Height : 10.071
Entry
ampl
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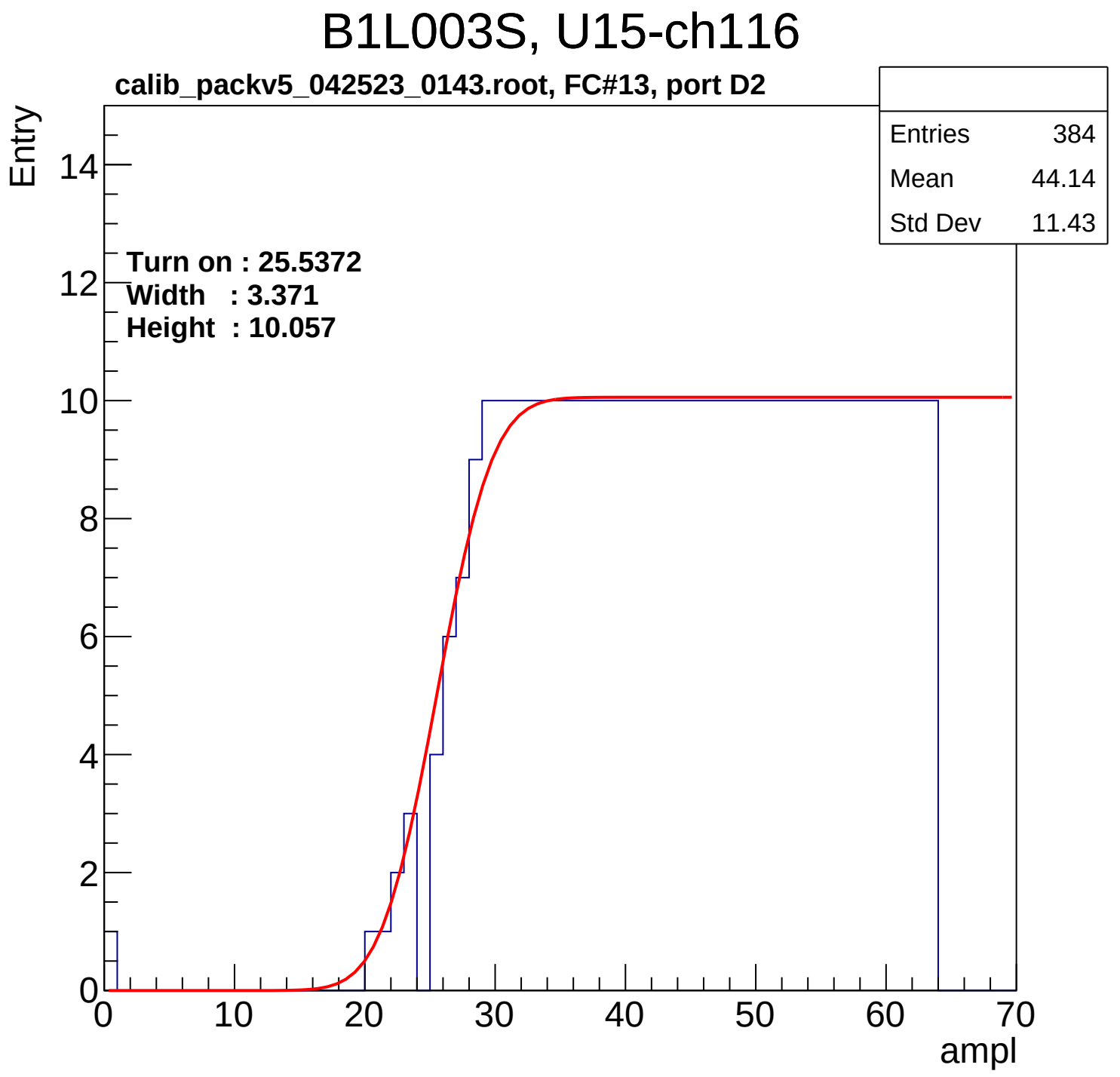
B1L003S, U15-ch116
calib_packv5_042523_0143.root, FC#13, port D2
Entries 384
Mean 44.14
Std Dev 11.43
Turn on : 25.5372
Width : 3.371
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
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0
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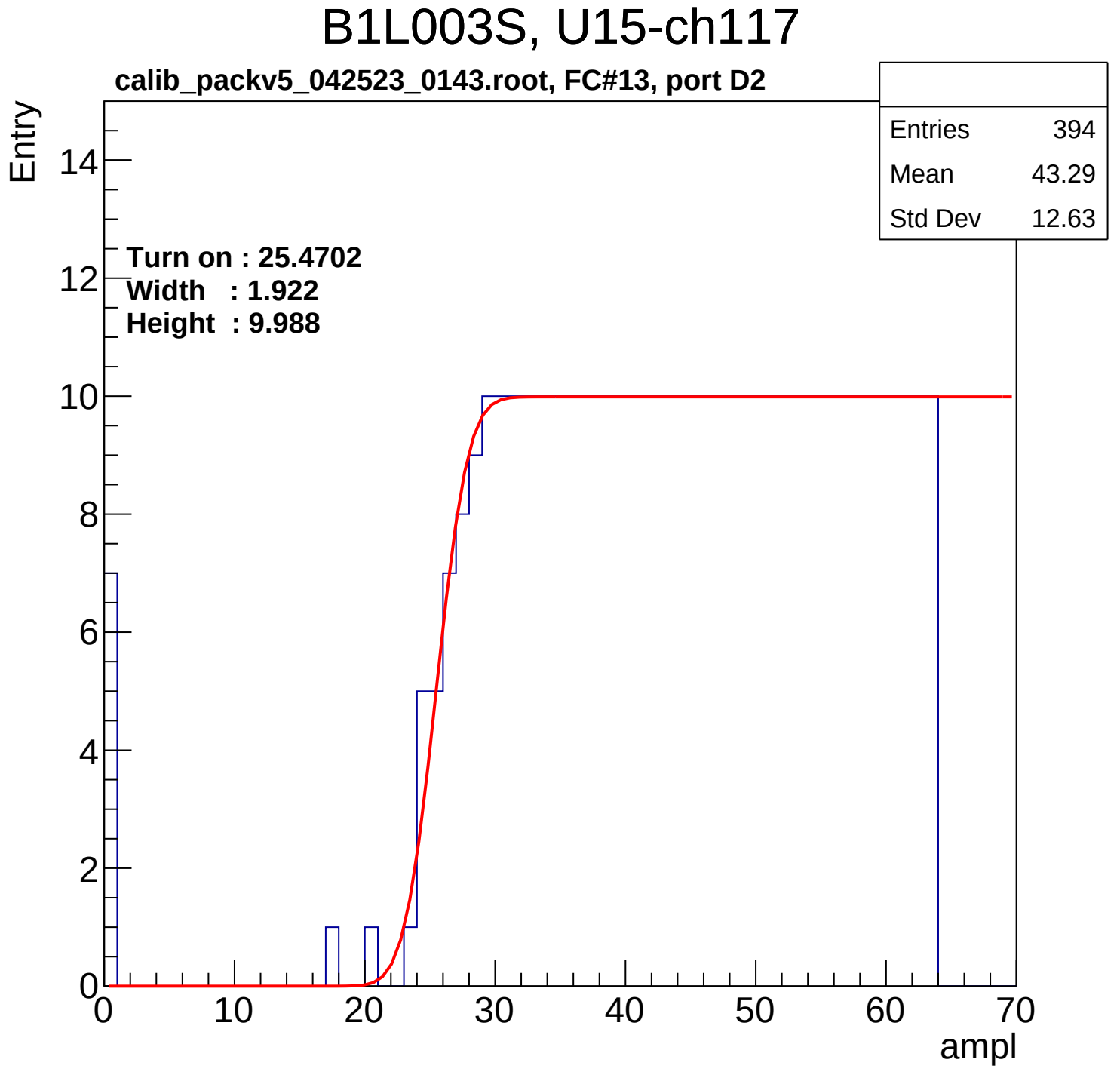
B1L003S, U15-ch117
calib_packv5_042523_0143.root, FC#13, port D2
Entries 394
Mean 43.29
Std Dev 12.63
Turn on : 25.4702
Width : 1.922
Height : 9.988
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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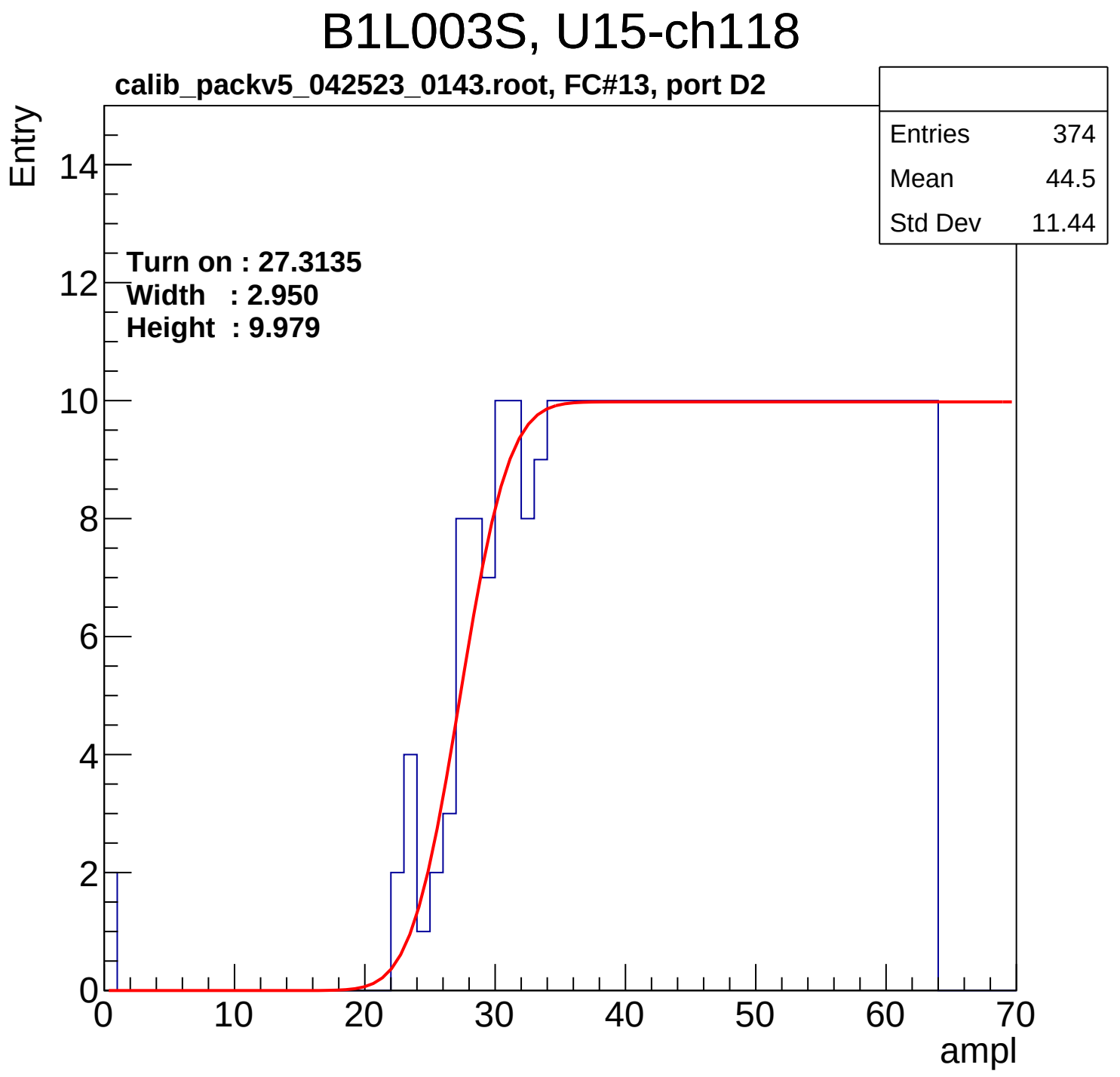
B1L003S, U15-ch118
calib_packv5_042523_0143.root, FC#13, port D2
Entries 374
Mean 44.5
Std Dev 11.44
Turn on : 27.3135
Width : 2.950
Height : 9.979
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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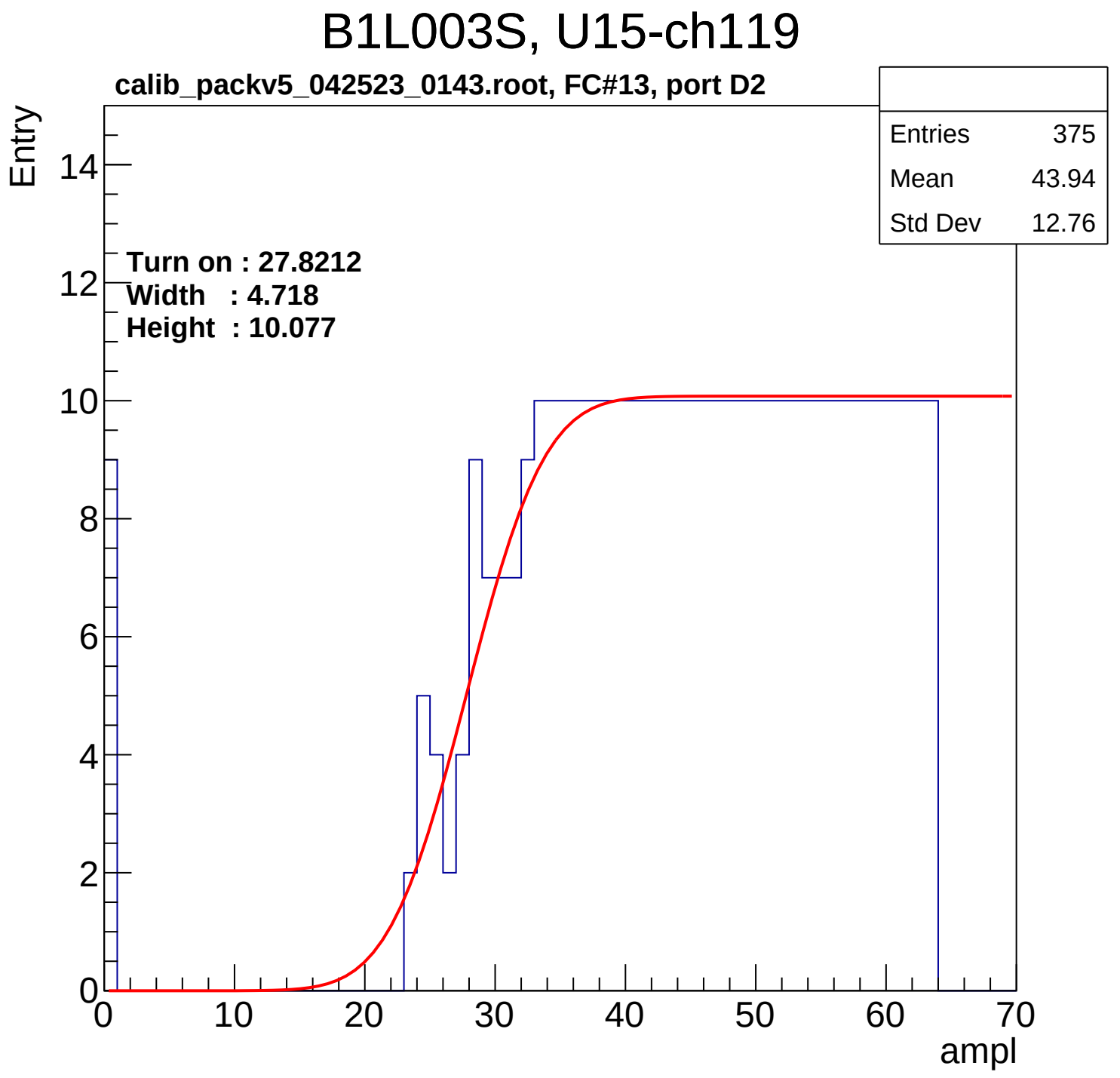
B1L003S, U15-ch119
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 43.94
Std Dev 12.76
Turn on : 27.8212
Width : 4.718
Height : 10.077
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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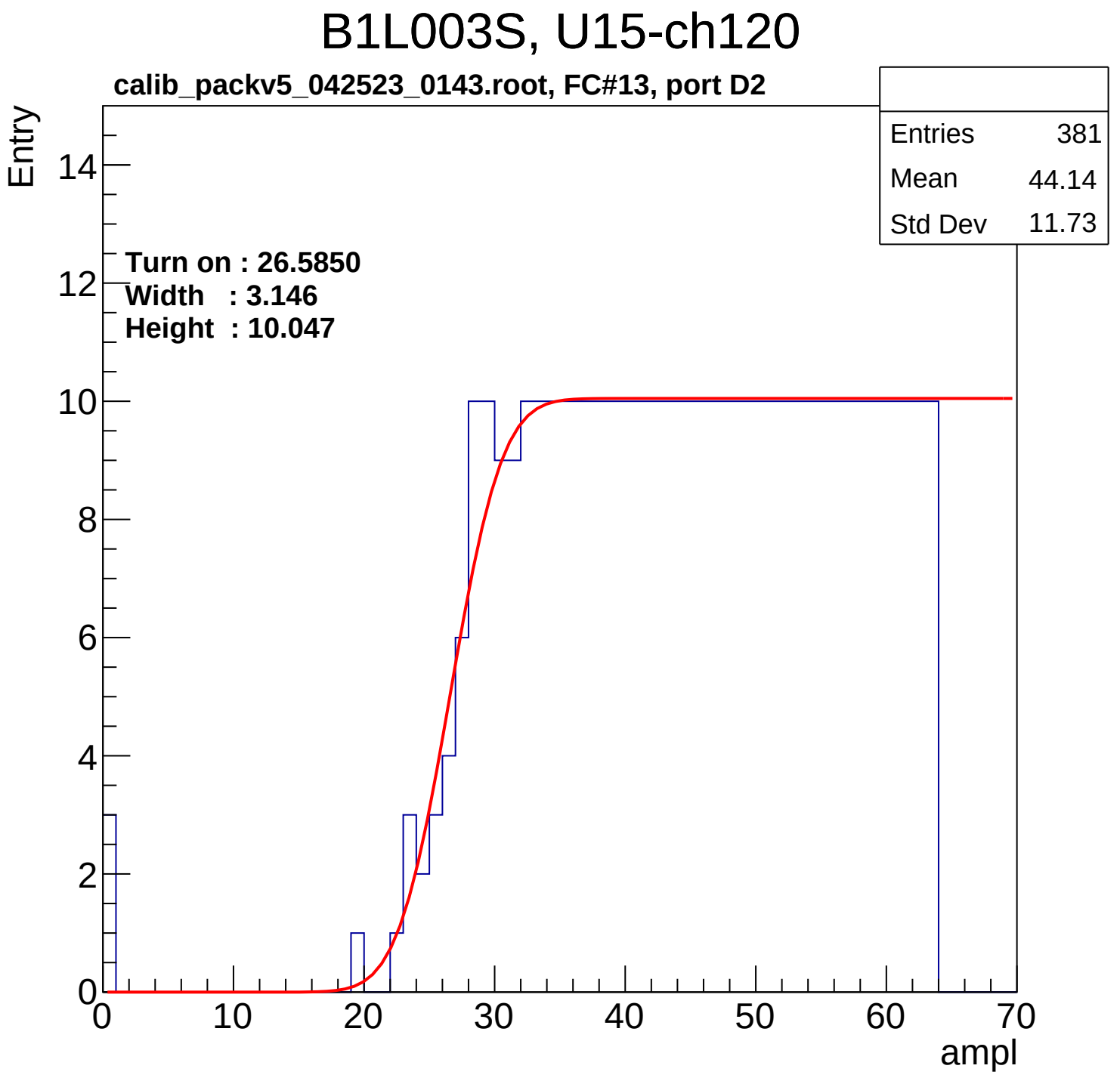
B1L003S, U15-ch120
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 44.14
Std Dev 11.73
Turn on : 26.5850
Width : 3.146
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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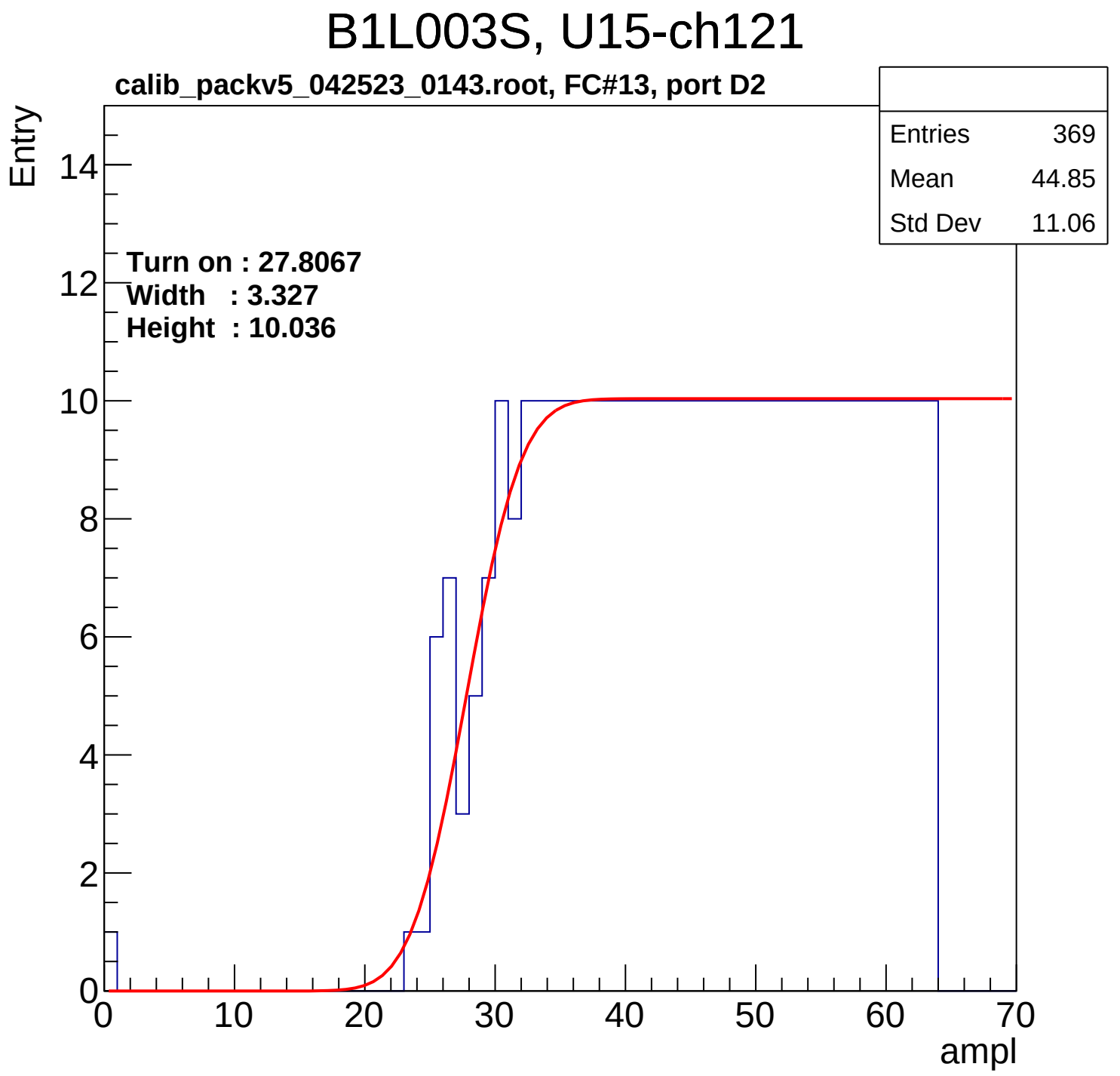
B1L003S, U15-ch121
calib_packv5_042523_0143.root, FC#13, port D2
Entries 369
Mean 44.85
Std Dev 11.06
Turn on : 27.8067
Width : 3.327
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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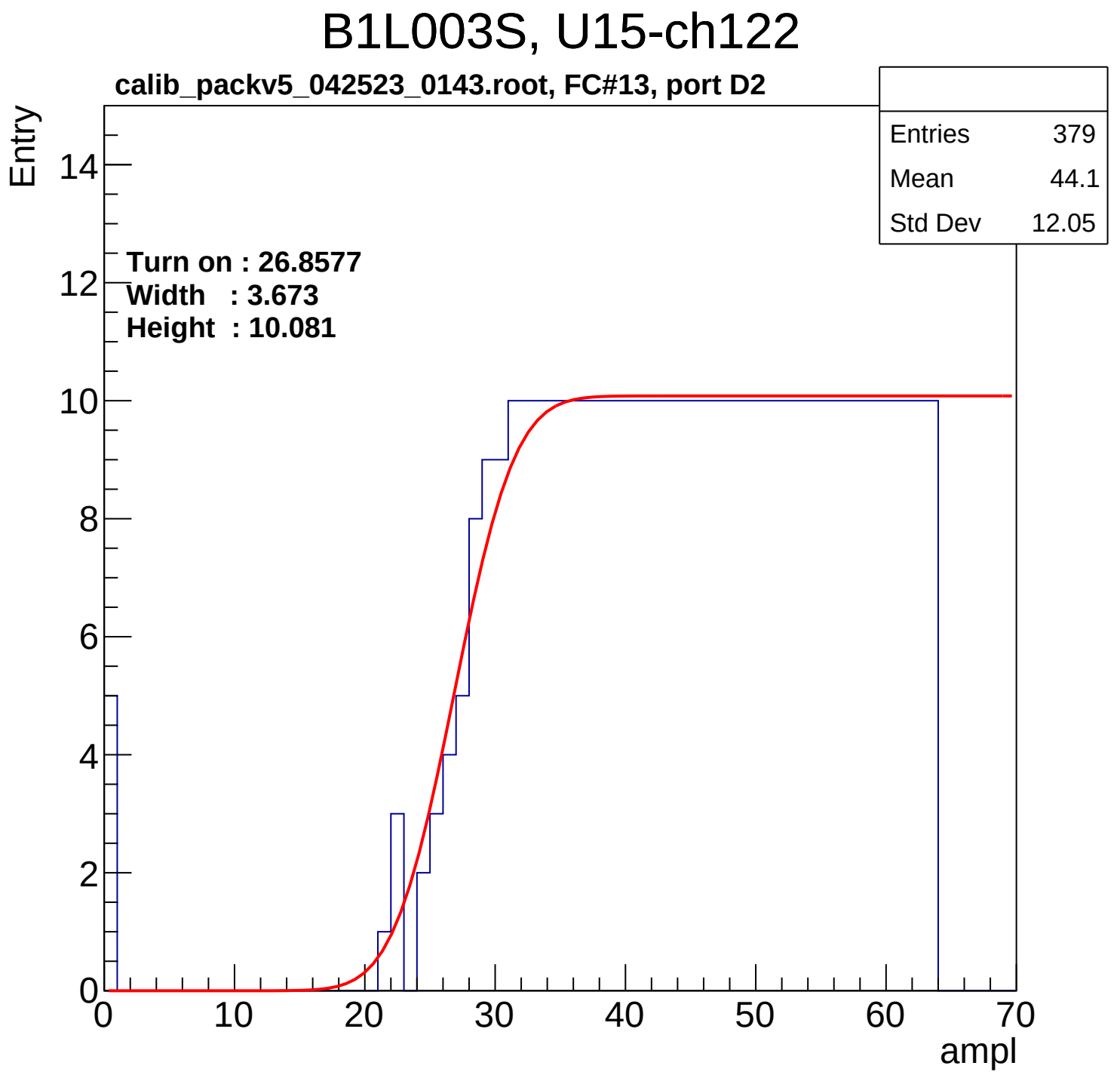
B1L003S, U15-ch122
calib_packv5_042523_0143.root, FC#13, port D2
Entries 379
Mean 44.1
Std Dev 12.05
Turn on : 26.8577
Width : 3.673
Height : 10.081
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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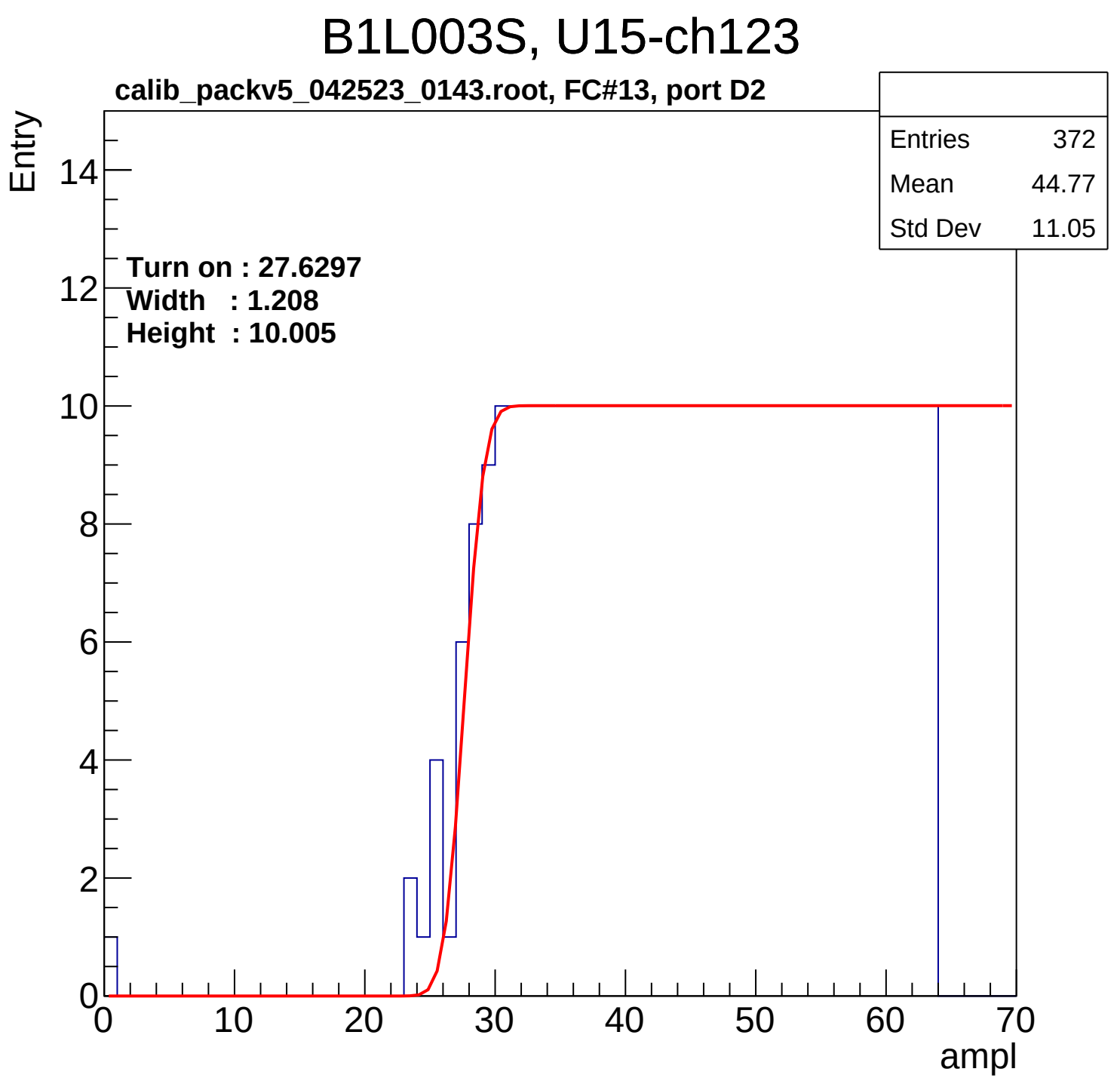
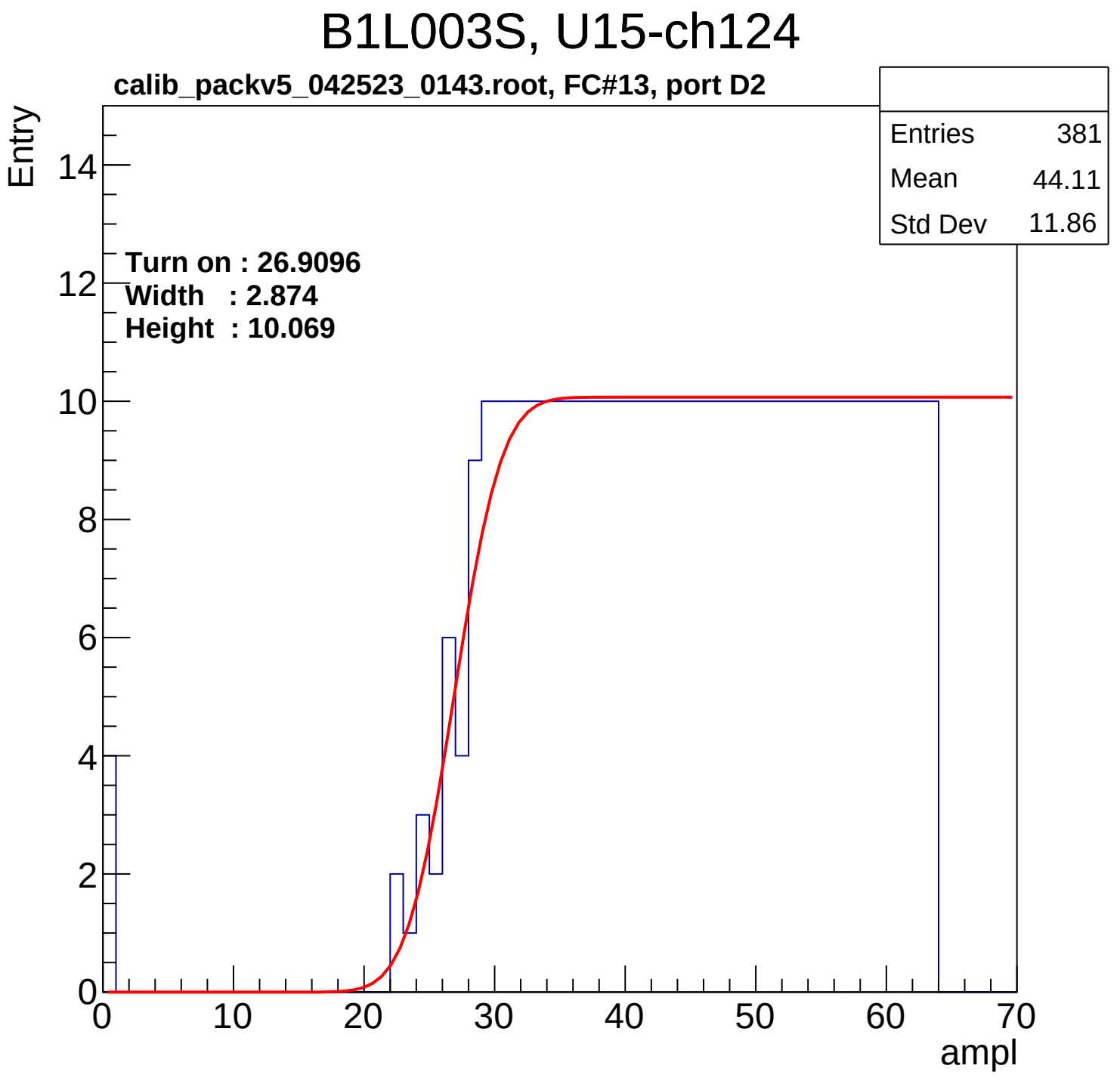
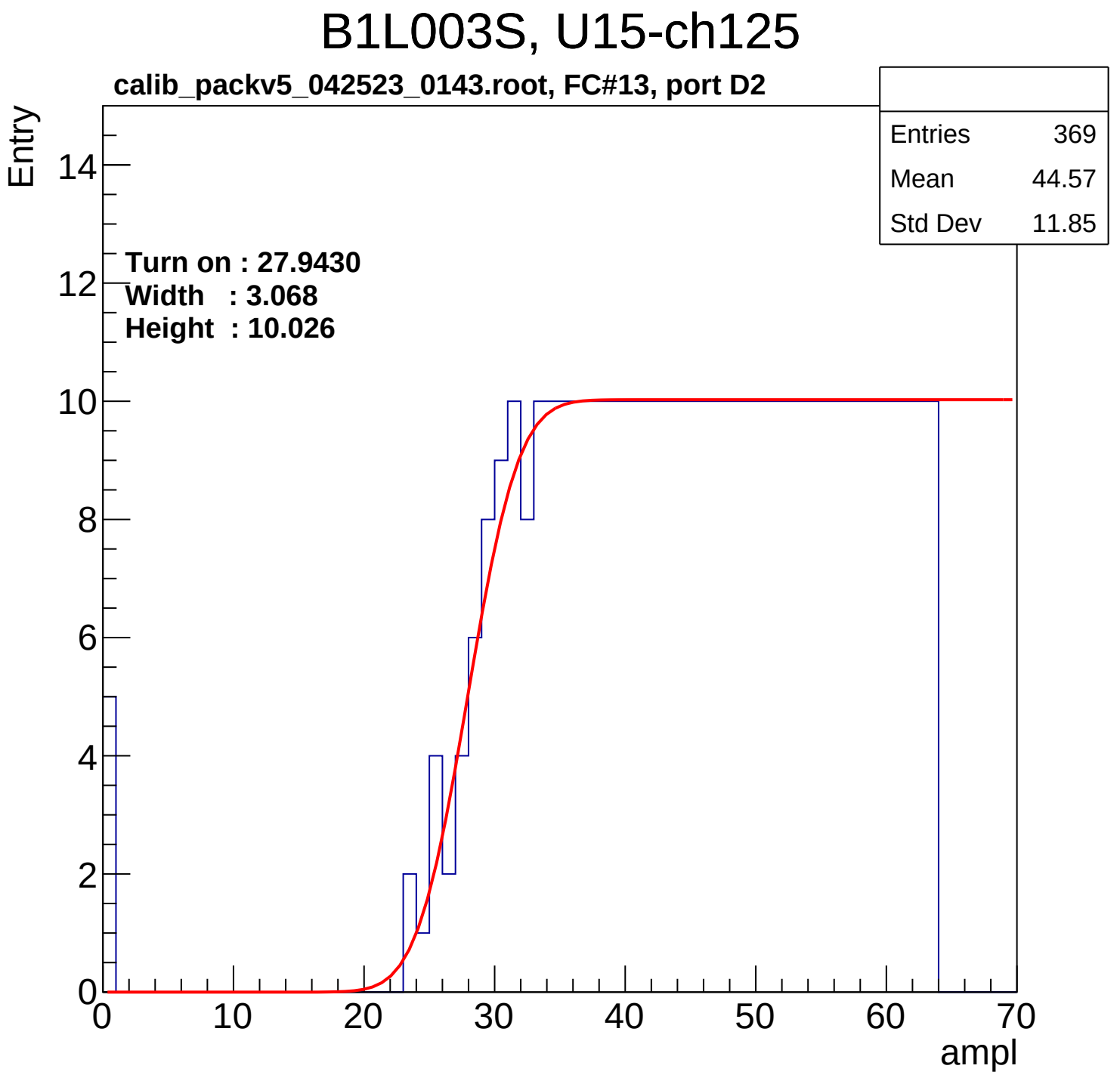
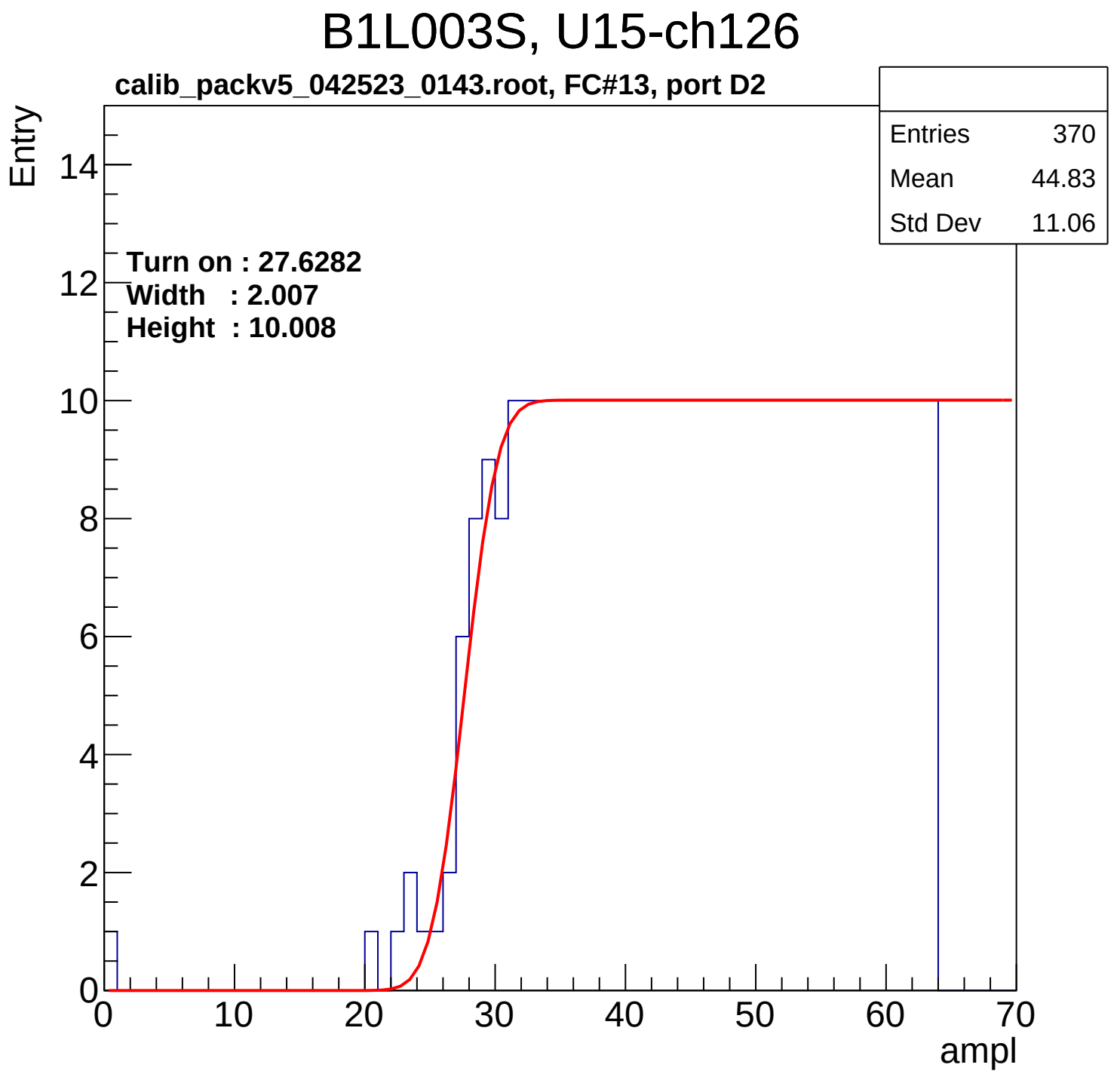

B1L003S, U15-ch123
calib_packv5_042523_0143.root, FC#13, port D2
Entries 372
Mean 44.77
Std Dev 11.05
Turn on : 27.6297
Width : 1.208
Height : 10.005
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U15-ch124
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 44.11
Std Dev 11.86
Turn on : 26.9096
Width : 2.874
Height : 10.069
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U15-ch125
calib_packv5_042523_0143.root, FC#13, port D2
Entries 369
Mean 44.57
Std Dev 11.85
Turn on : 27.9430
Width : 3.068
Height : 10.026
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U15-ch126
calib_packv5_042523_0143.root, FC#13, port D2
Entries 370
Mean 44.83
Std Dev 11.06
Turn on : 27.6282
Width : 2.007
Height : 10.008
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
50
60
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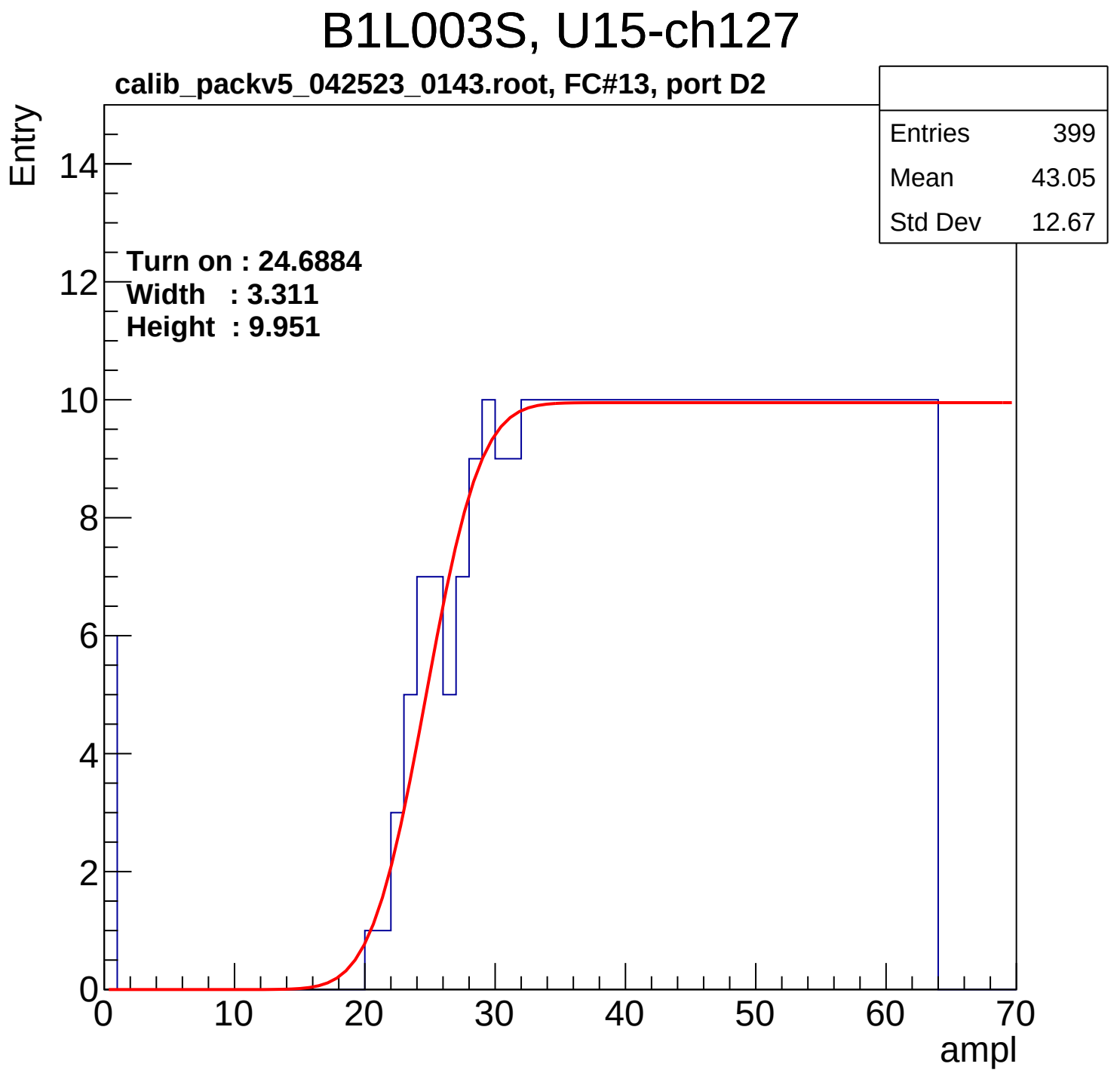
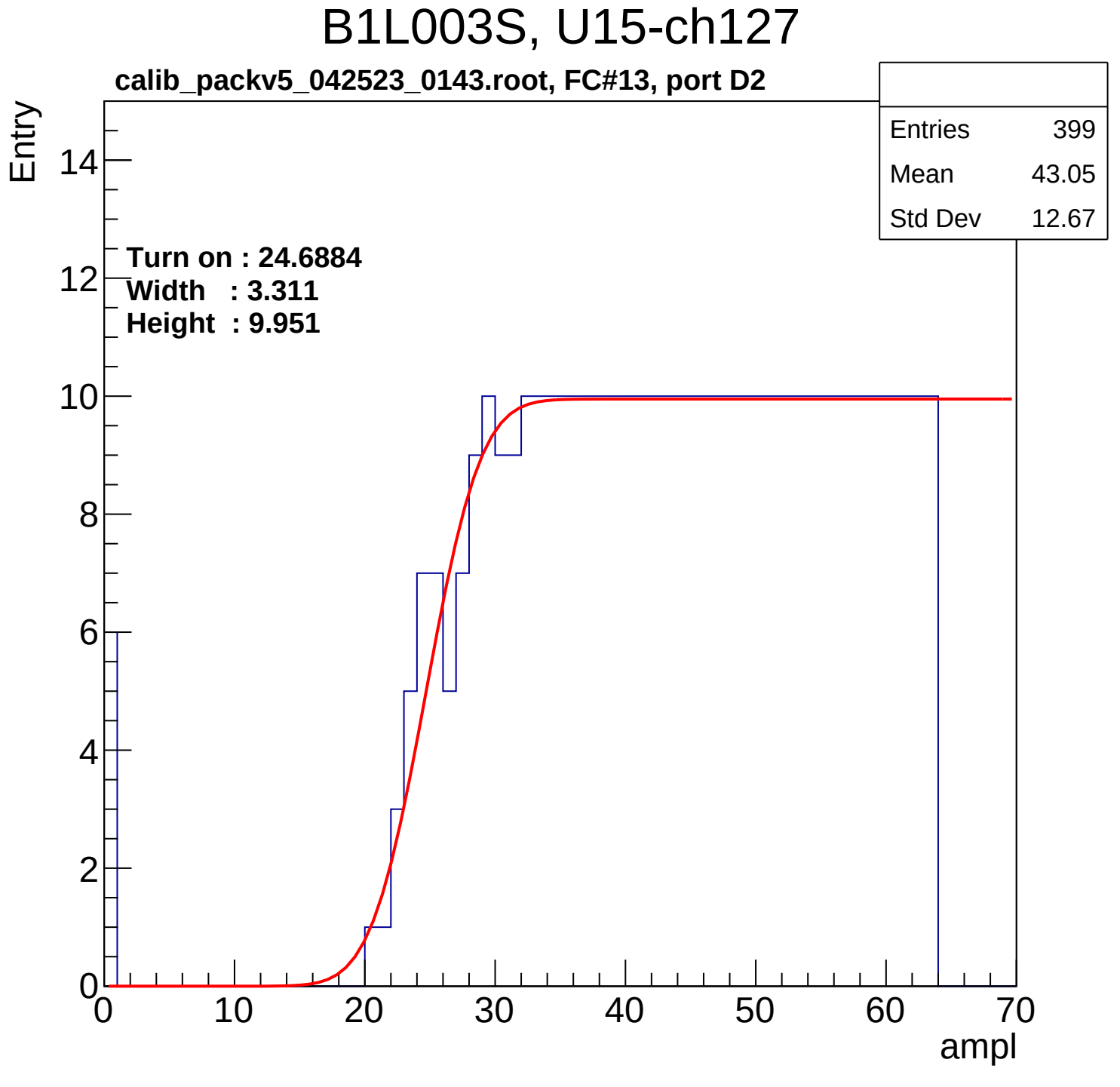

B1L003S, U15-ch127
calib_packv5_042523_0143.root, FC#13, port D2
Entries 399
Mean 43.05
Std Dev 12.67
Turn on : 24.6884
Width : 3.311
Height : 9.951
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U15-ch127
calib_packv5_042523_0143.root, FC#13, port D2
Entries 399
Mean 43.05
Std Dev 12.67
Turn on : 24.6884
Width : 3.311
Height : 9.951
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70