

B1L103S, U3-ch0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	456
Mean	38.09
Std Dev	17.89

Turn on : 24.6808

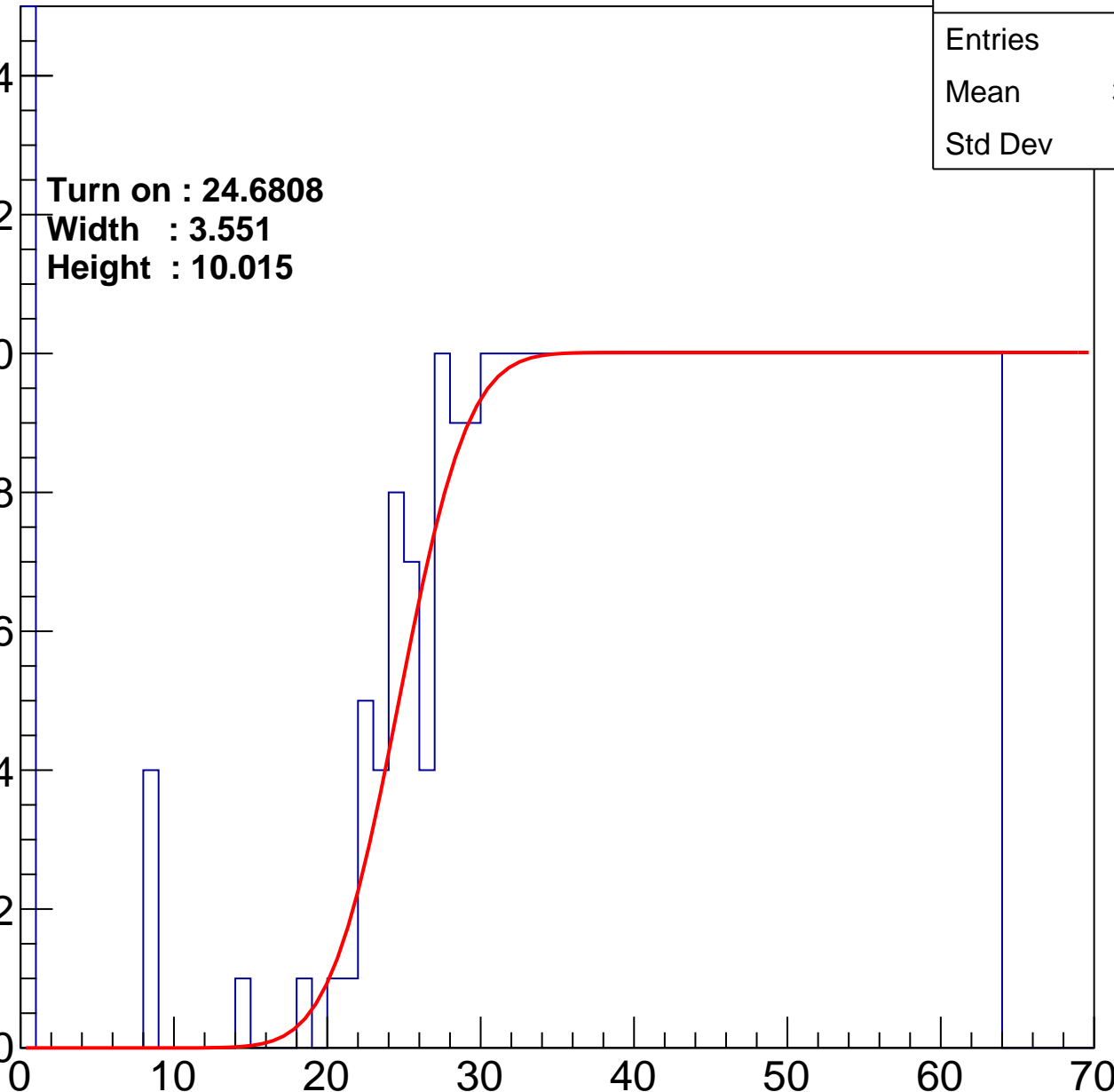
Width : 3.551

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	445
Mean	38.51
Std Dev	17.91

Turn on : 25.0261

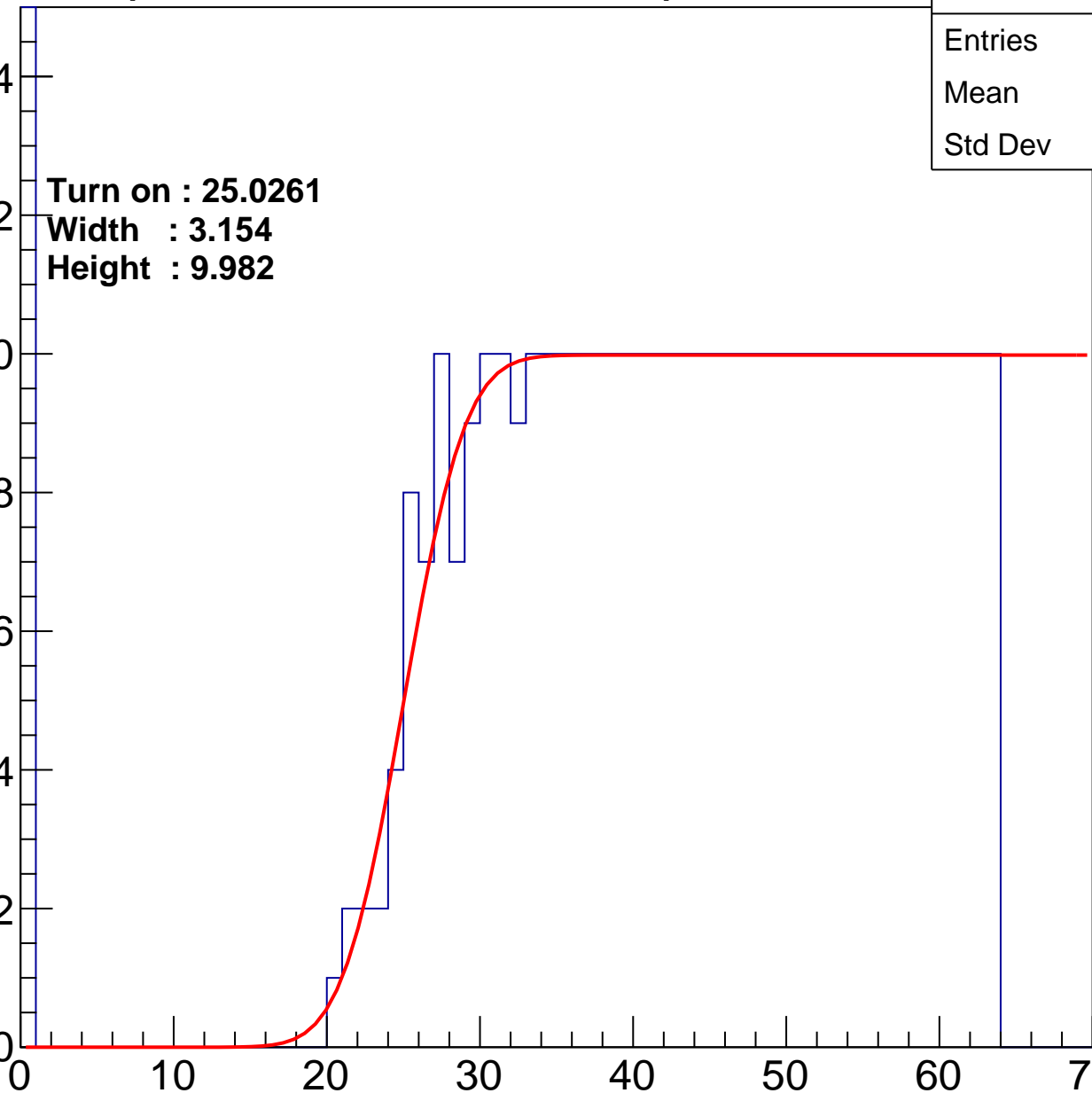
Width : 3.154

Height : 9.982

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	40.06
Std Dev	17.1

Turn on : 27.0085

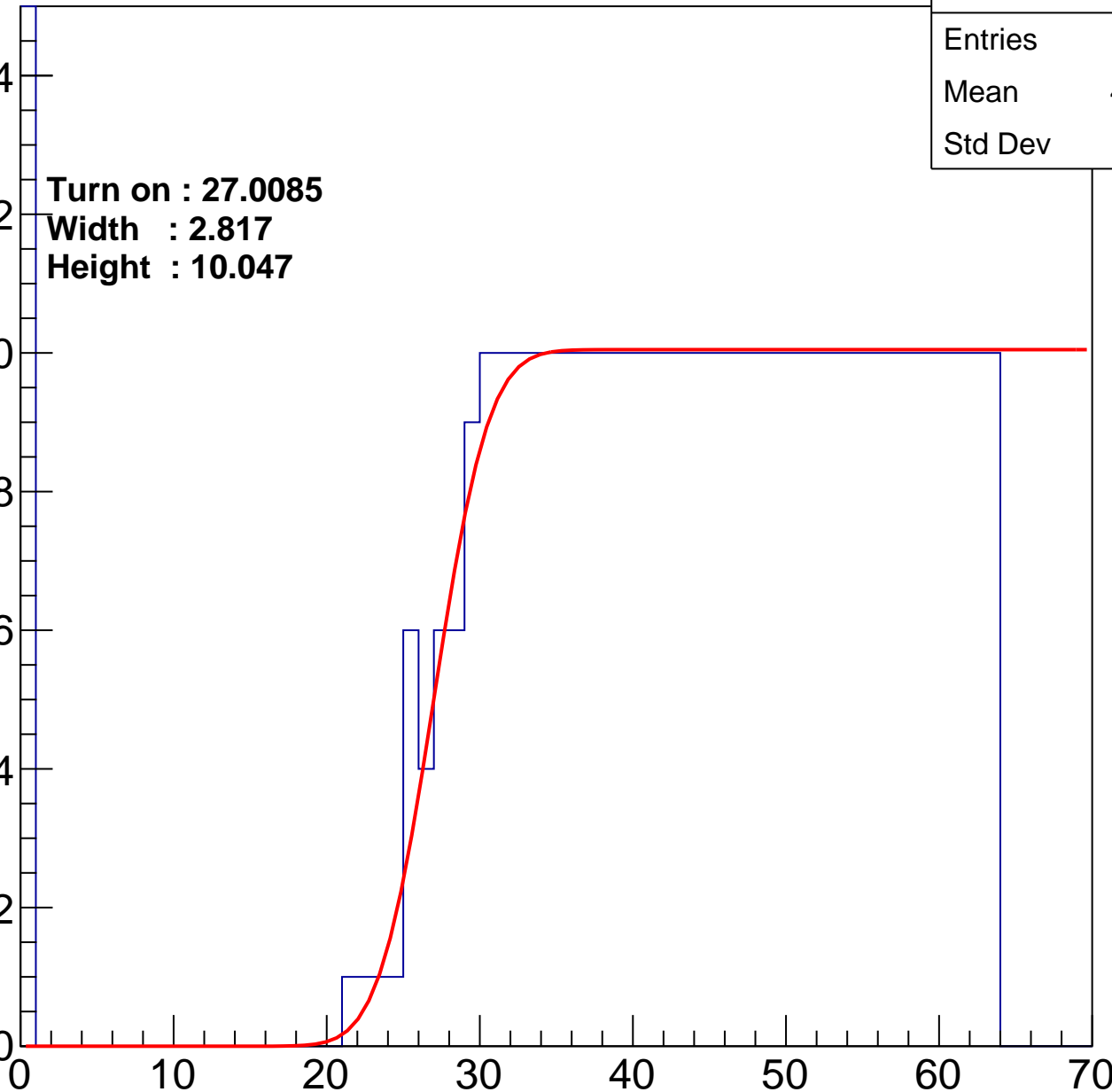
Width : 2.817

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch3

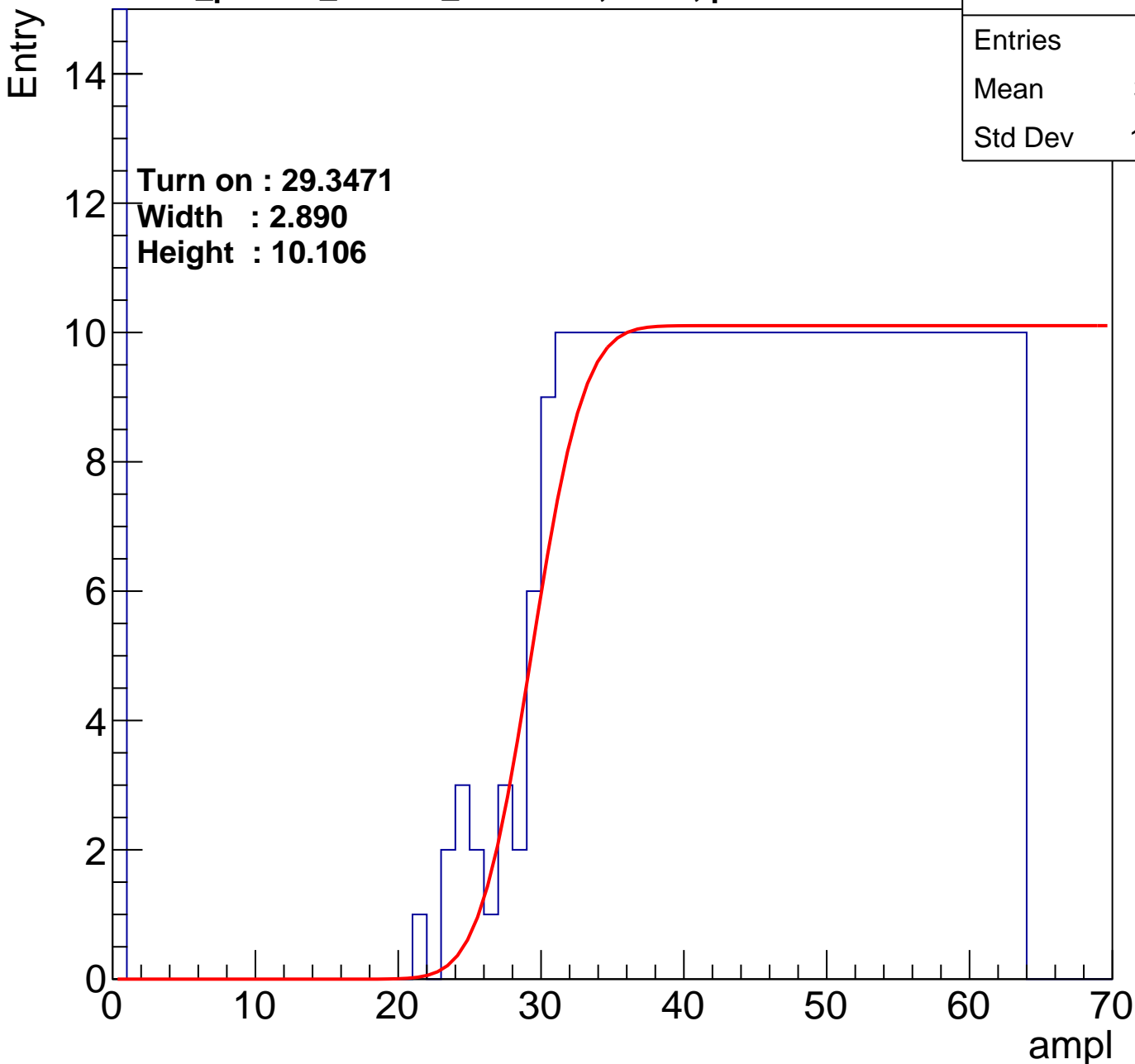
calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	39.01
Std Dev	18.62

Turn on : 29.3471

Width : 2.890

Height : 10.106



B1L103S, U3-ch4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	39.4
Std Dev	17.12

Turn on : 24.9038

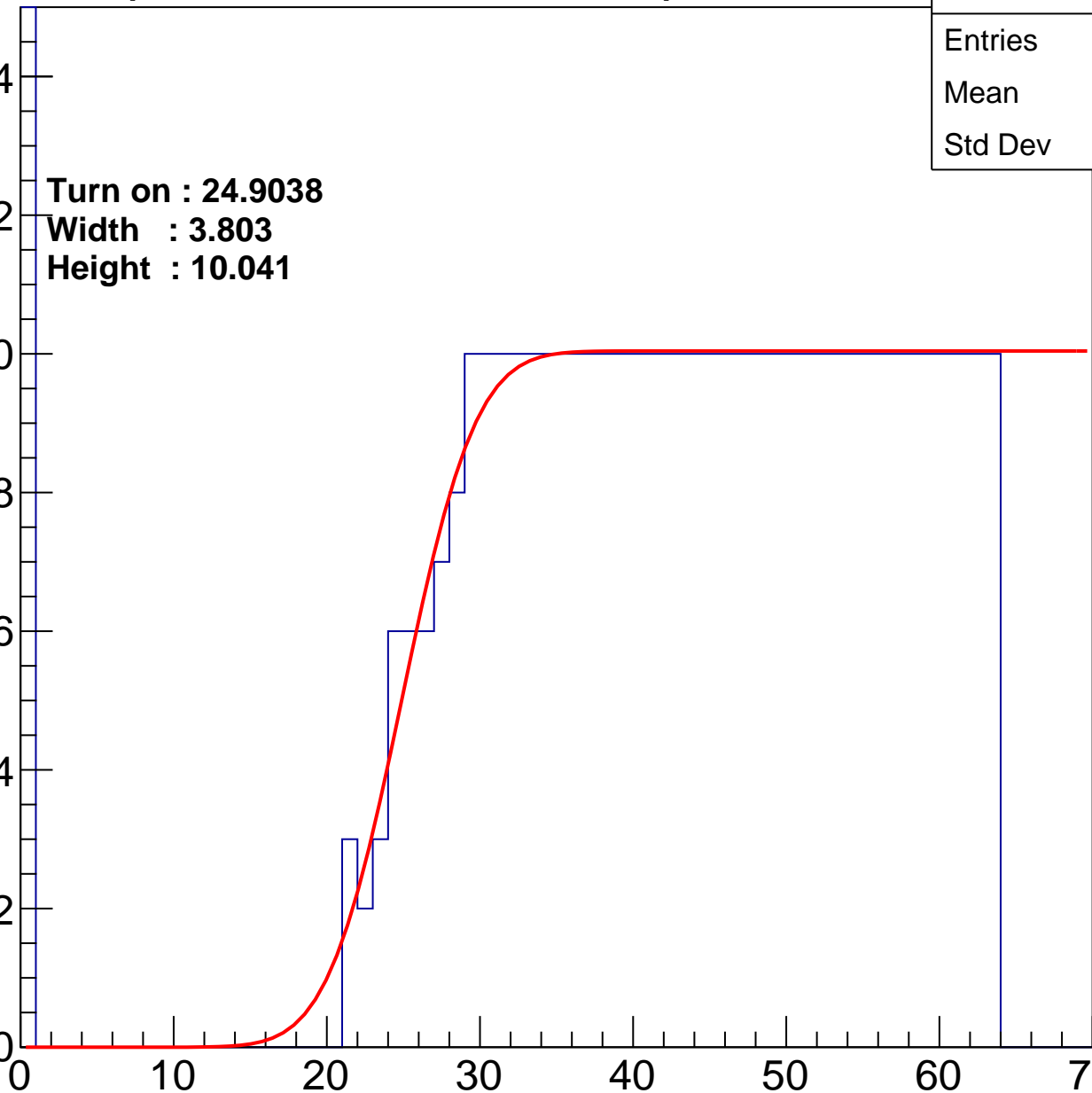
Width : 3.803

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch5

calib_packv5_041523_1651.root, FC#0, port C2

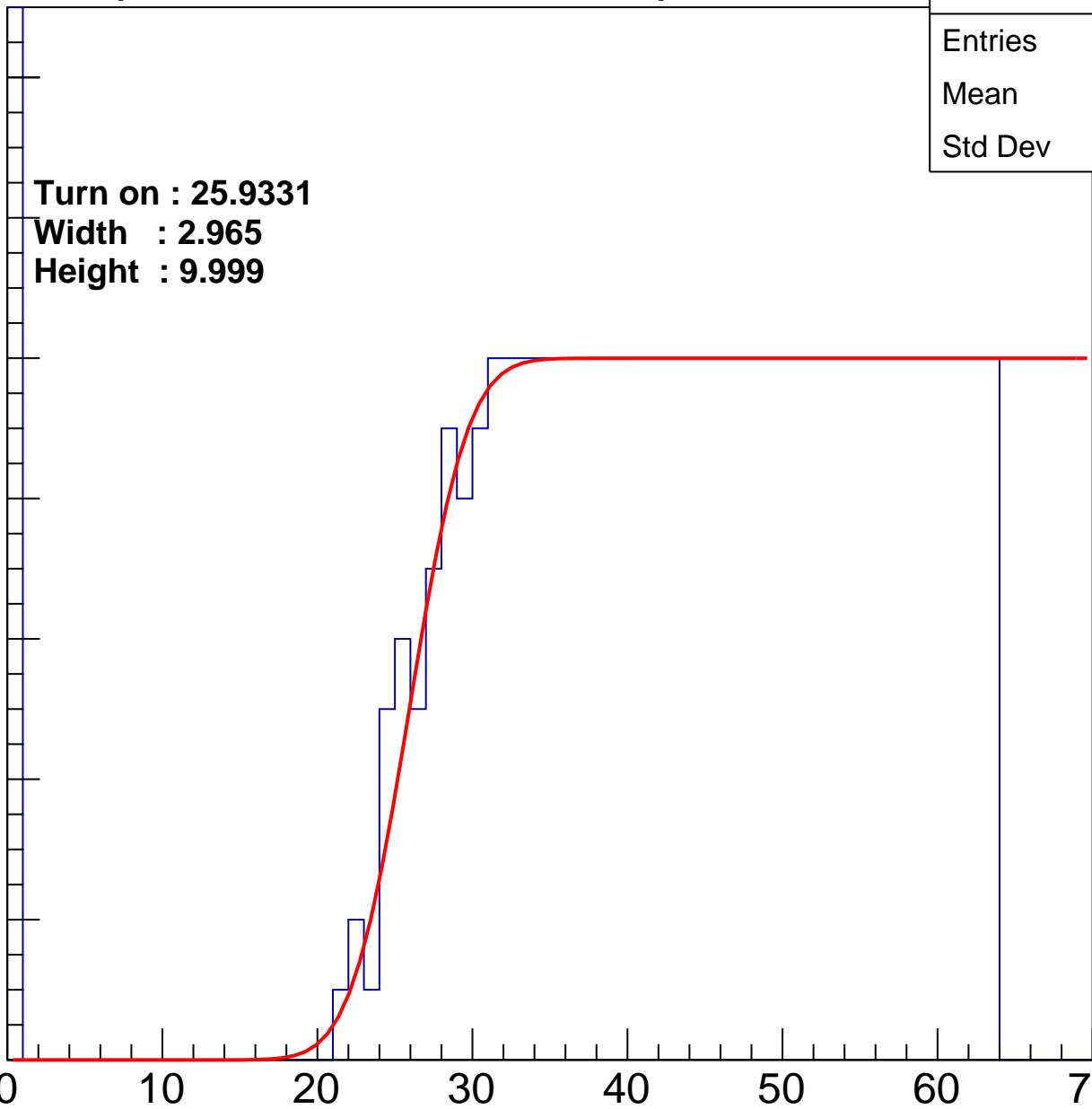
Entry

14
12
10
8
6
4
2
0

Turn on : 25.9331
Width : 2.965
Height : 9.999

Entries	437
Mean	38.77
Std Dev	17.97

ampl



B1L103S, U3-ch6

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	39.25
Std Dev	17.52

Turn on : 26.5521

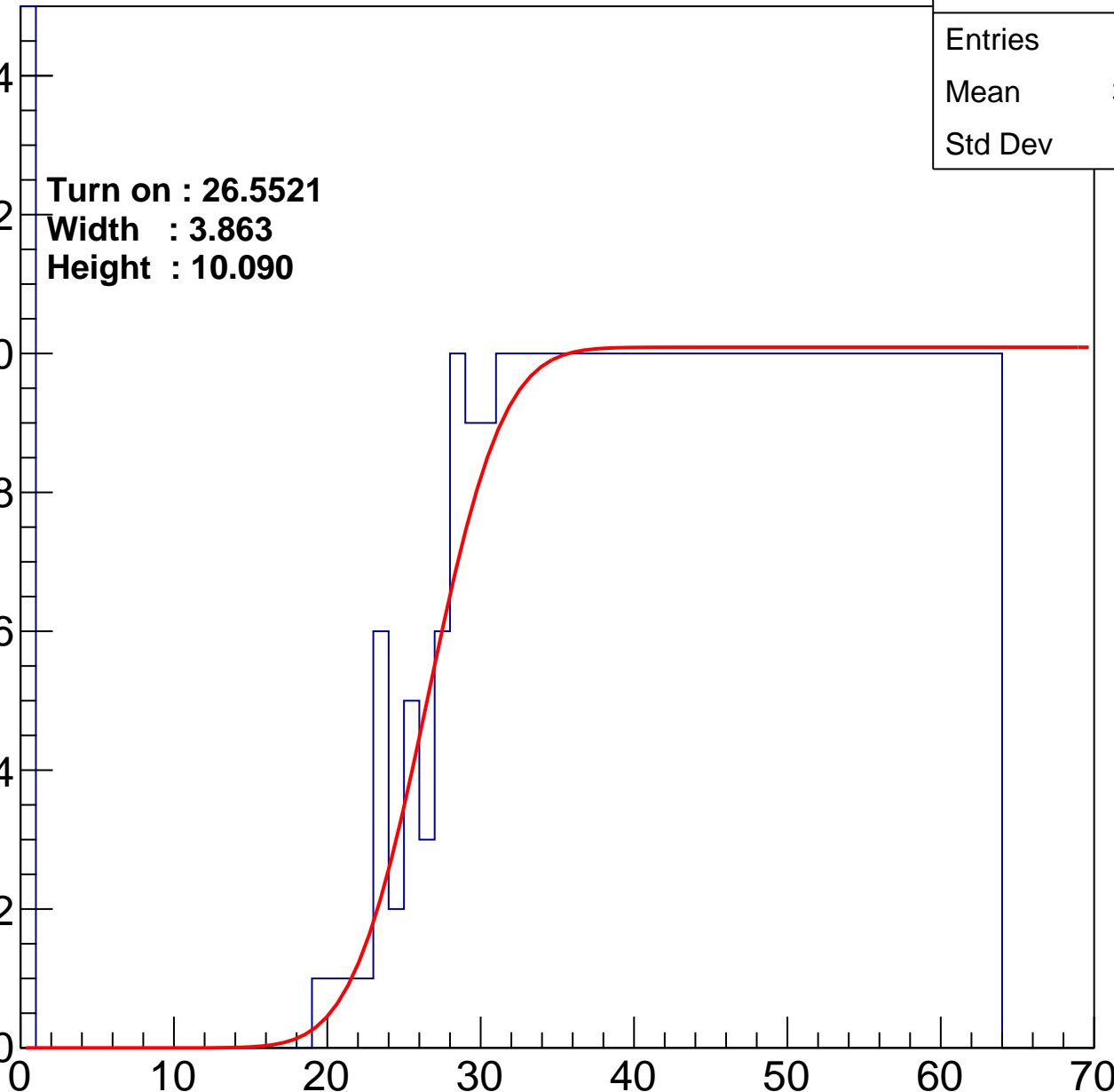
Width : 3.863

Height : 10.090

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	422
Mean	39.68
Std Dev	17.46

Turn on : 26.7003

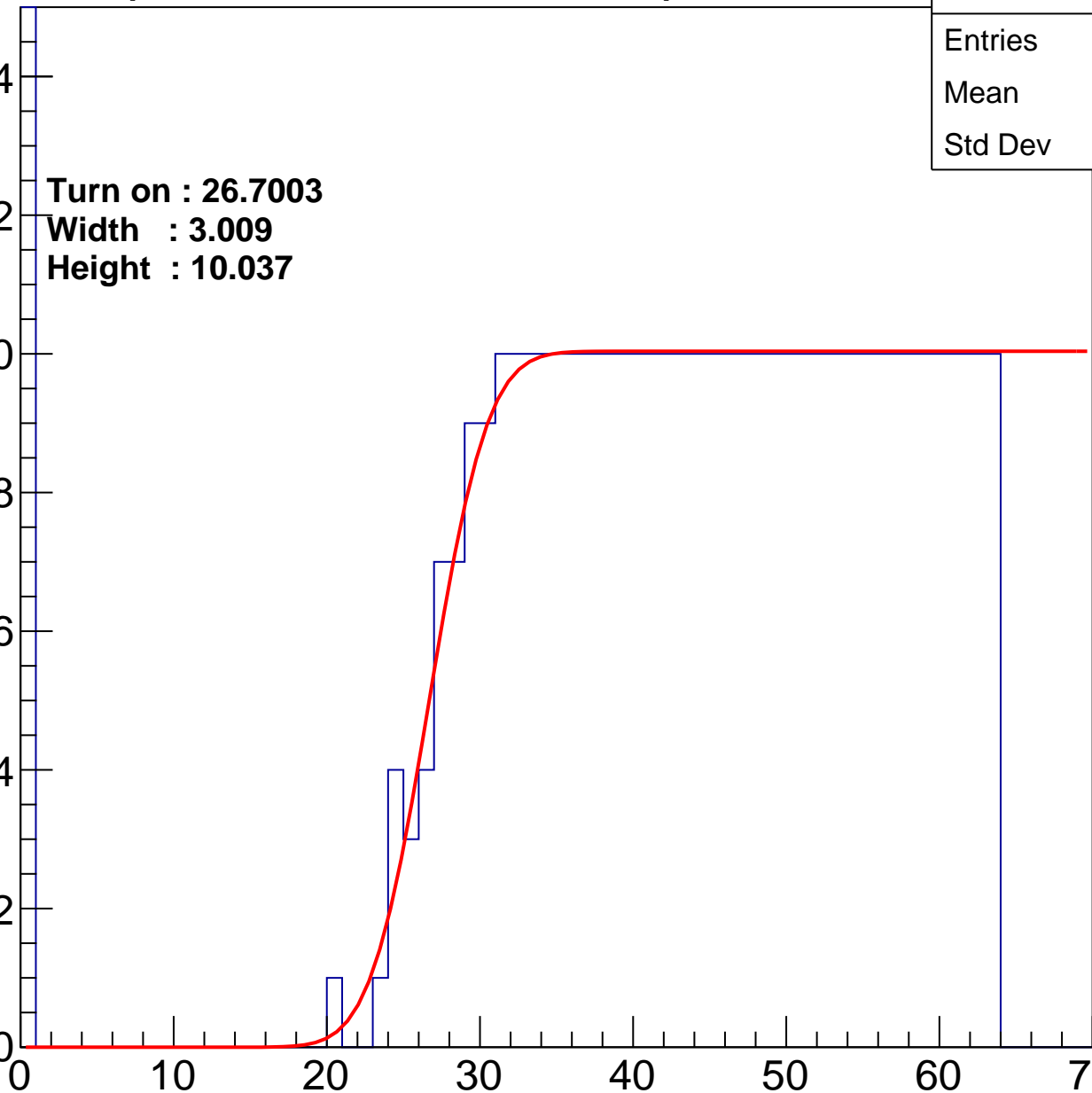
Width : 3.009

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch8

calib_packv5_041523_1651.root, FC#0, port C2

Entries	457
Mean	37.95
Std Dev	18.11

Turn on : 24.2019

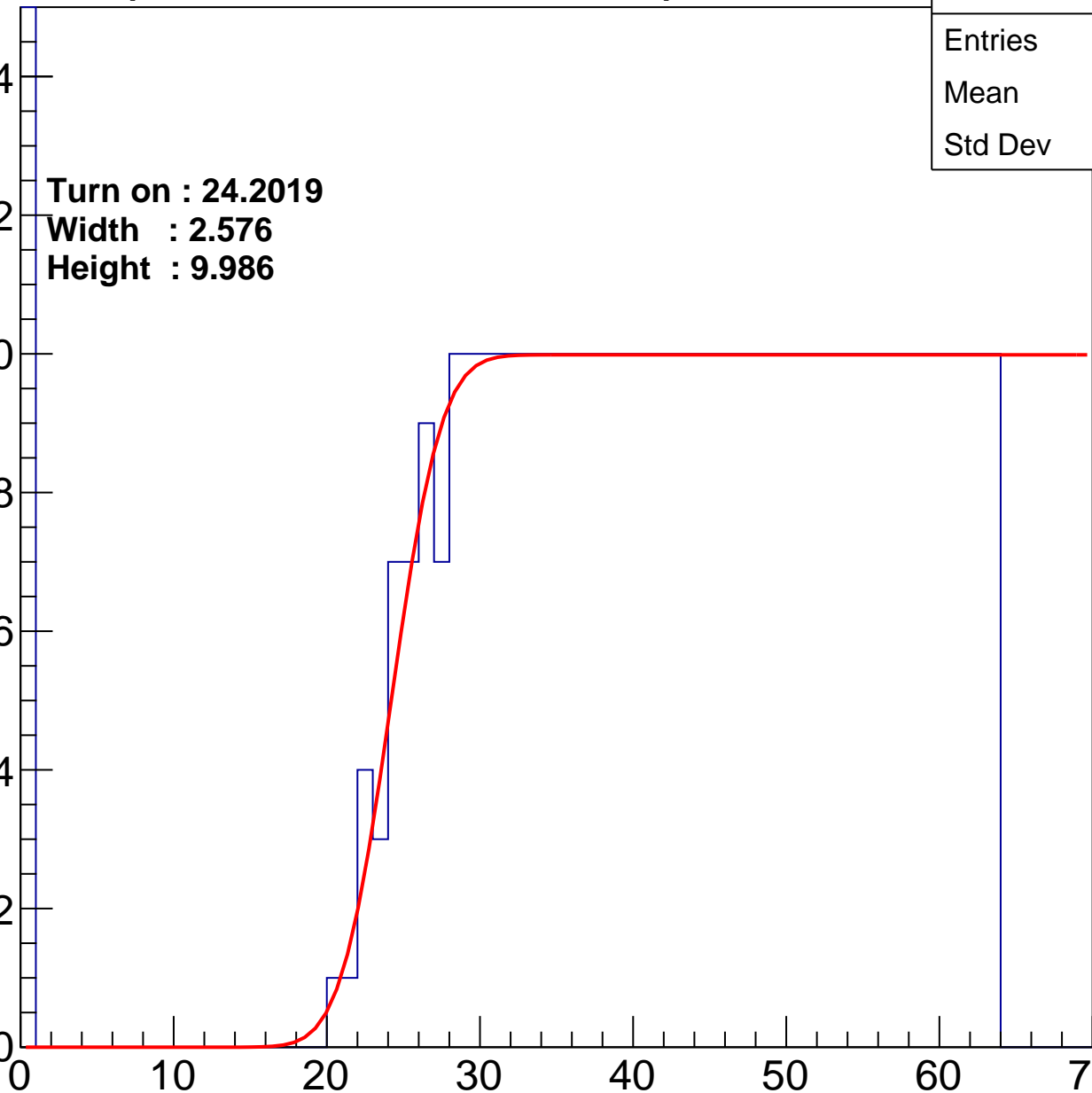
Width : 2.576

Height : 9.986

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch9

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	39.75
Std Dev	17.21

Turn on : 26.6668

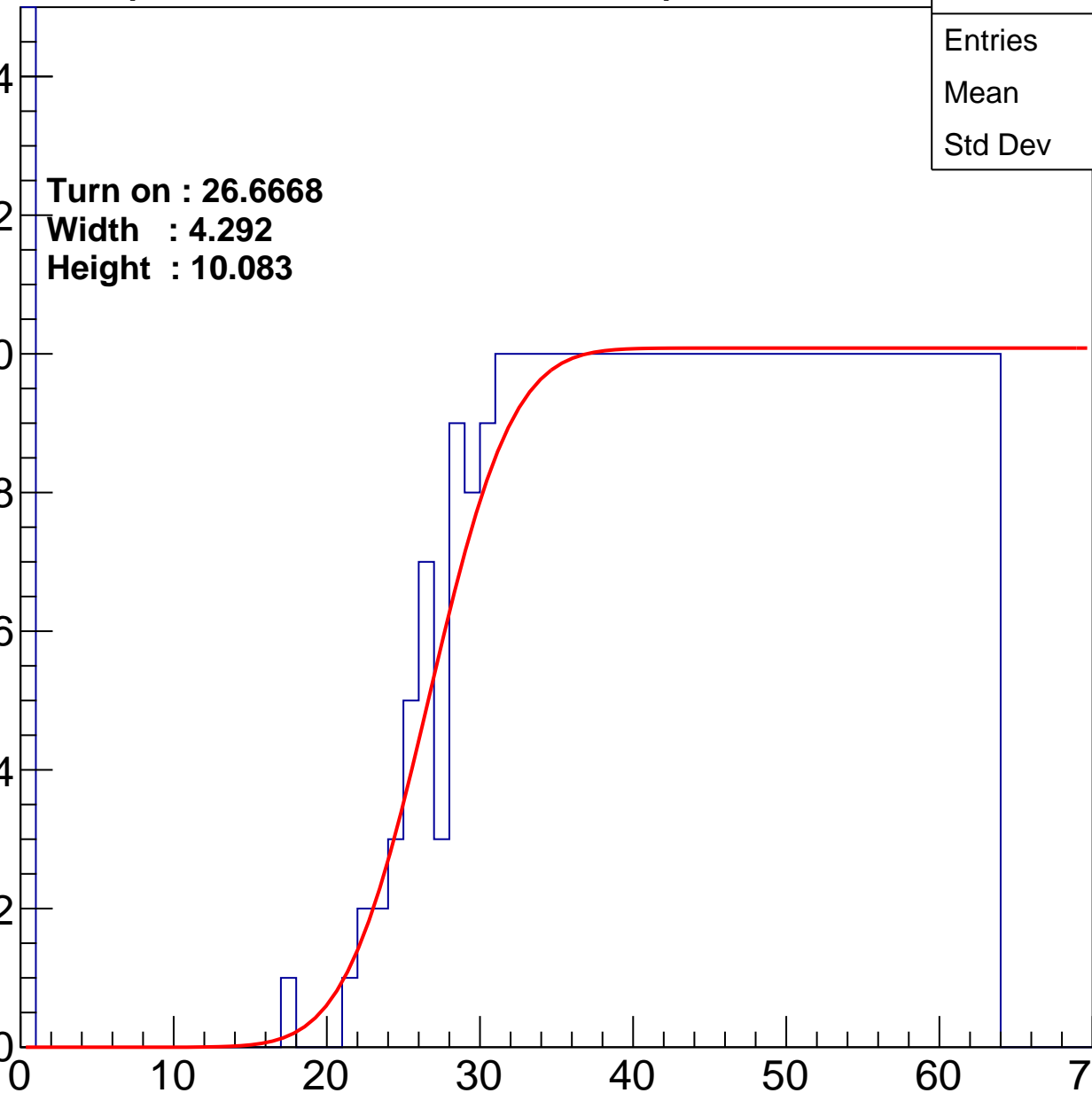
Width : 4.292

Height : 10.083

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch10

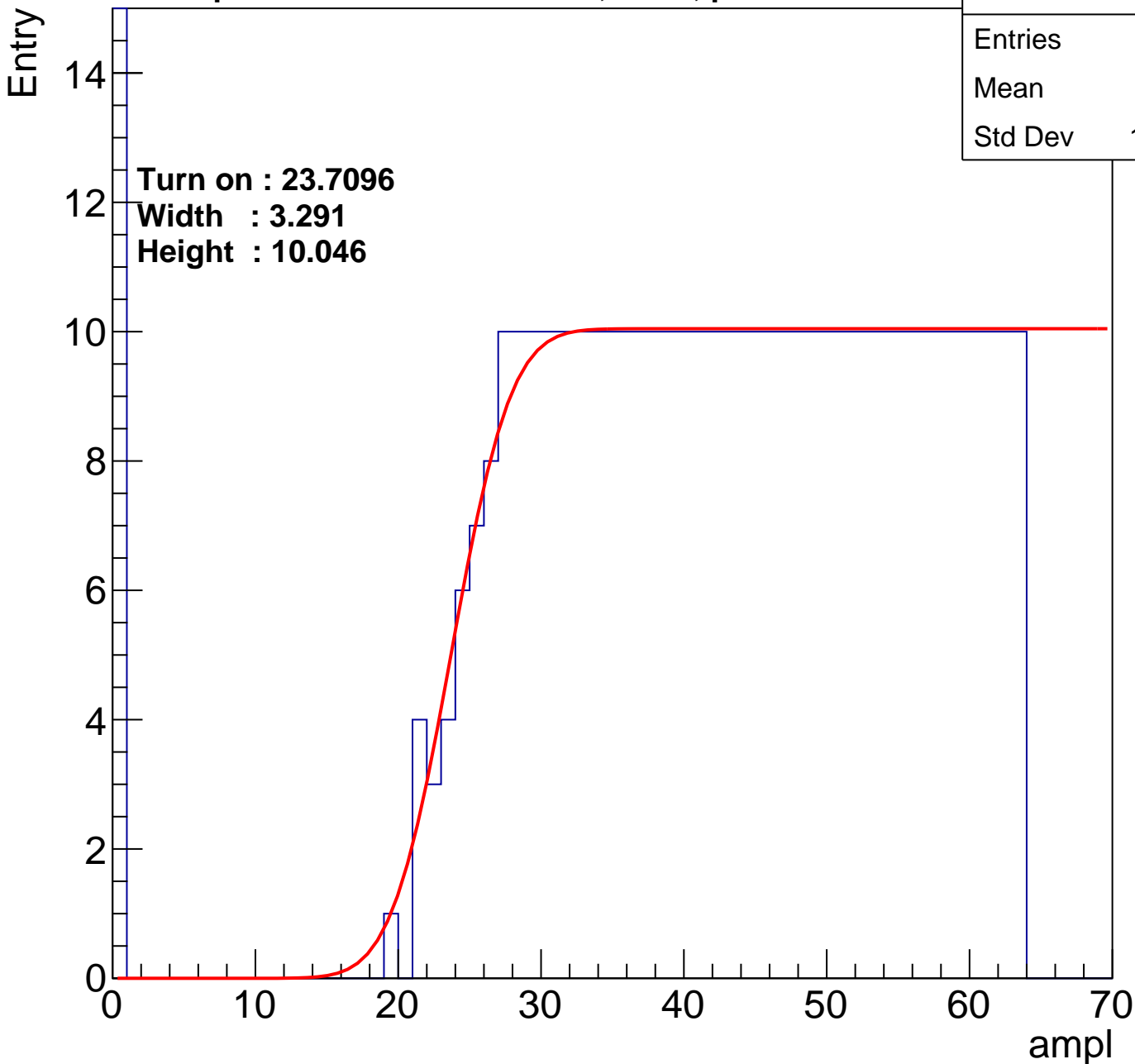
calib_packv5_041523_1651.root, FC#0, port C2

Entries	465
Mean	37.5
Std Dev	18.34

Turn on : 23.7096

Width : 3.291

Height : 10.046



B1L103S, U3-ch11

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	39.48
Std Dev	18.07

Turn on : 28.3472

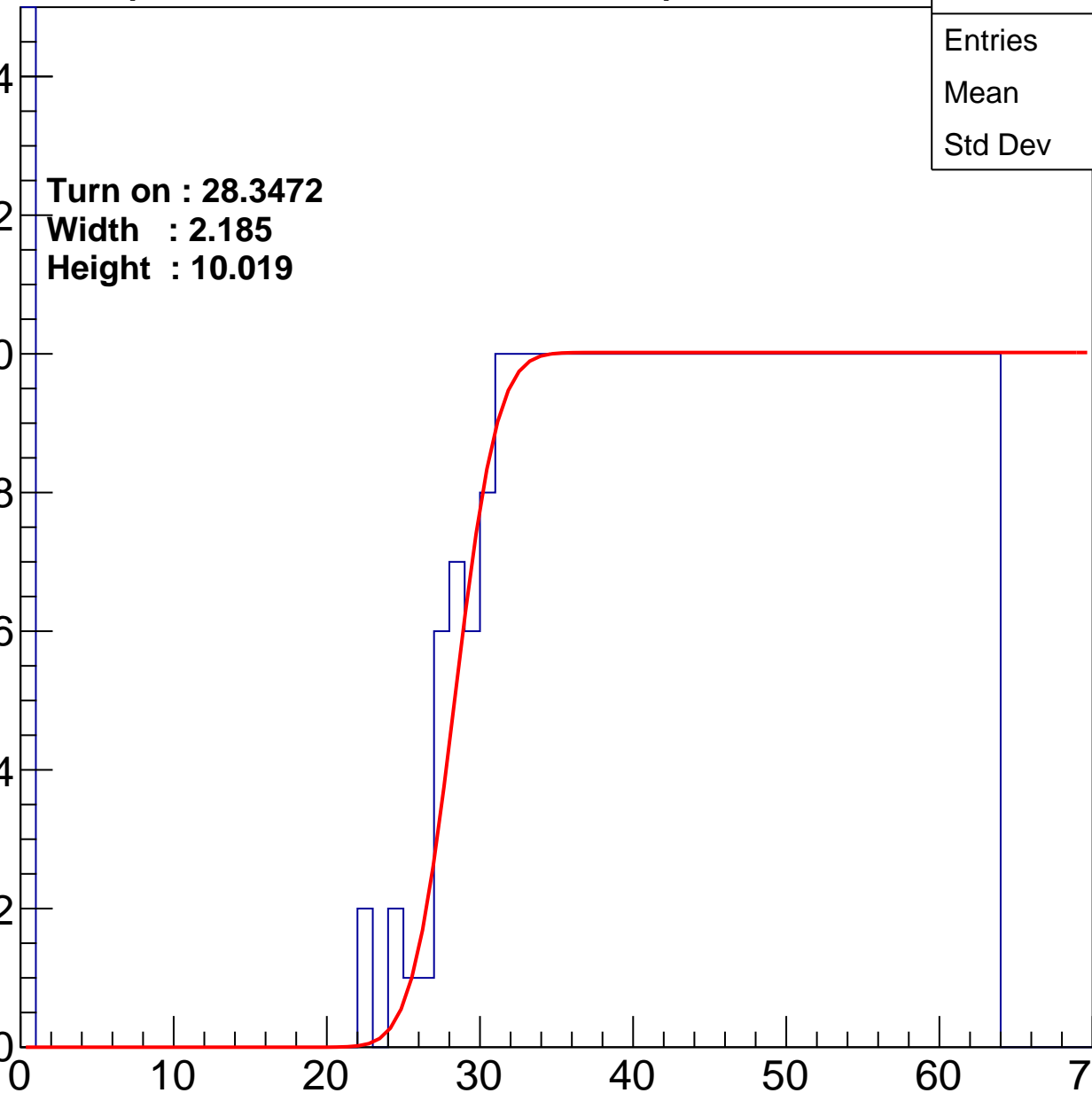
Width : 2.185

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch12

calib_packv5_041523_1651.root, FC#0, port C2

Entries	451
Mean	38.53
Std Dev	17.56

Turn on : 24.2861

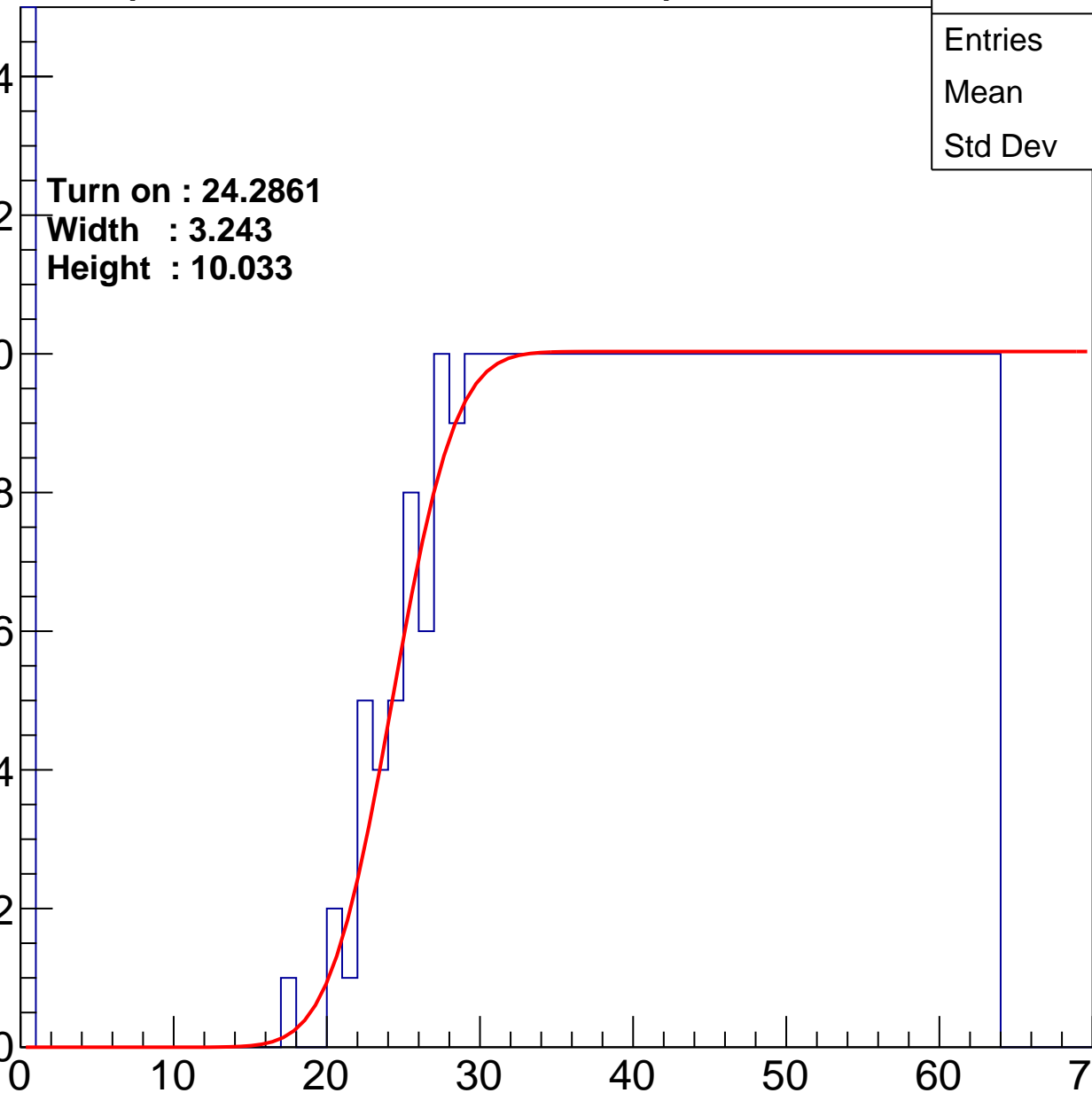
Width : 3.243

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch13

calib_packv5_041523_1651.root, FC#0, port C2

Entries	411
Mean	40.16
Std Dev	17.34

Turn on : 27.8024

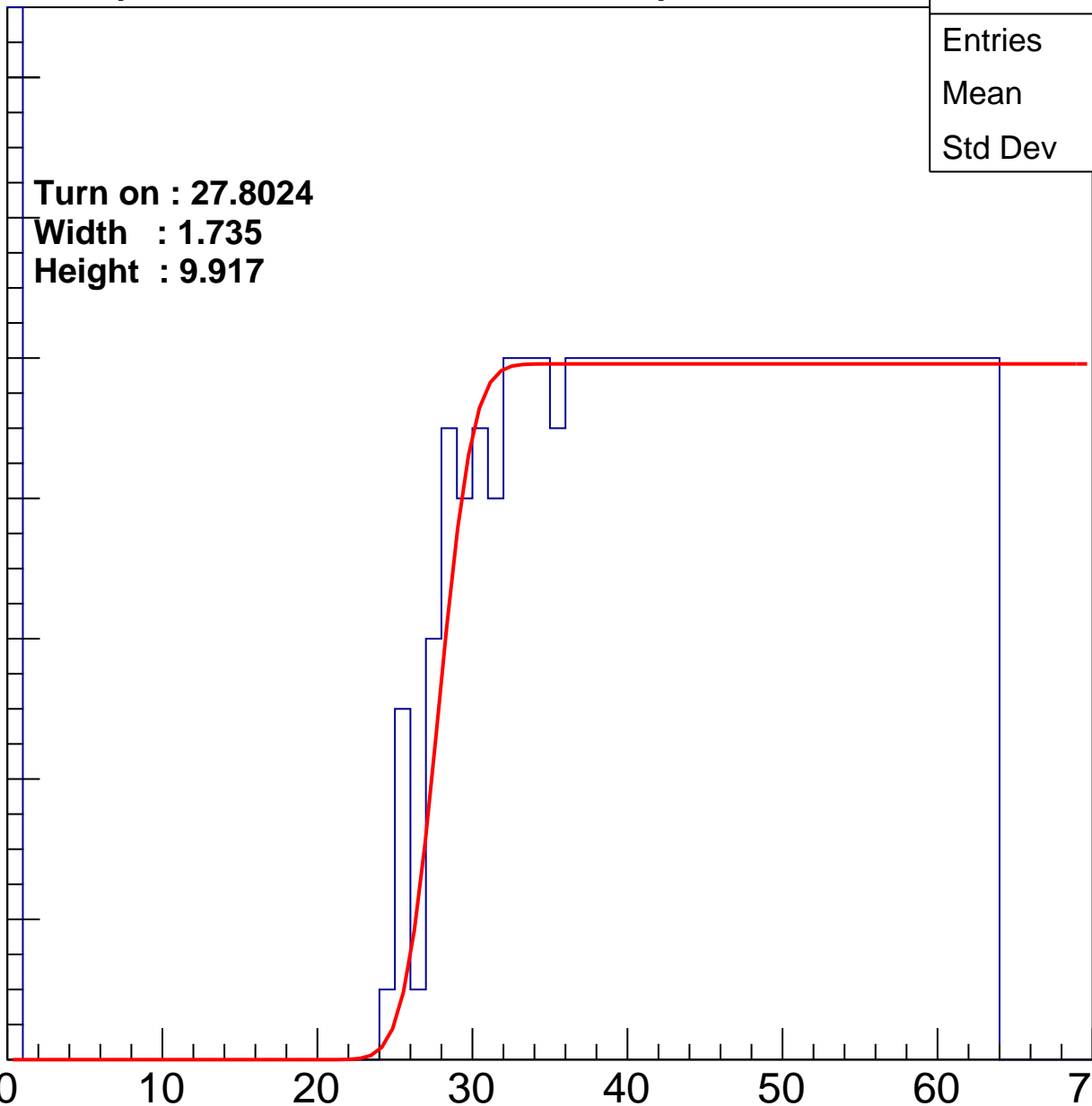
Width : 1.735

Height : 9.917

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch14

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	39.67
Std Dev	17.57

Turn on : 27.1244

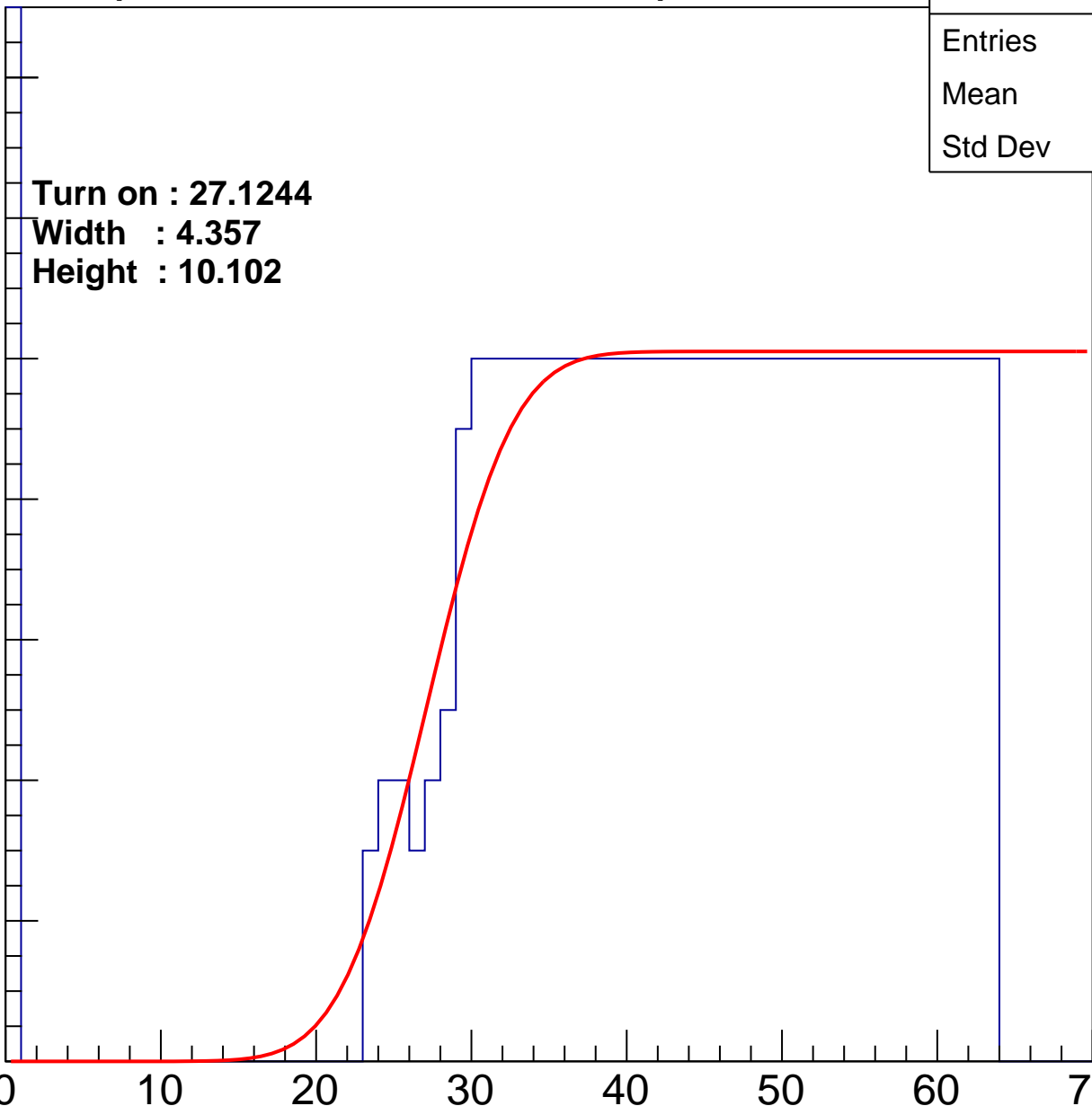
Width : 4.357

Height : 10.102

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch15

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	40.34
Std Dev	16.79

Turn on : 26.9459

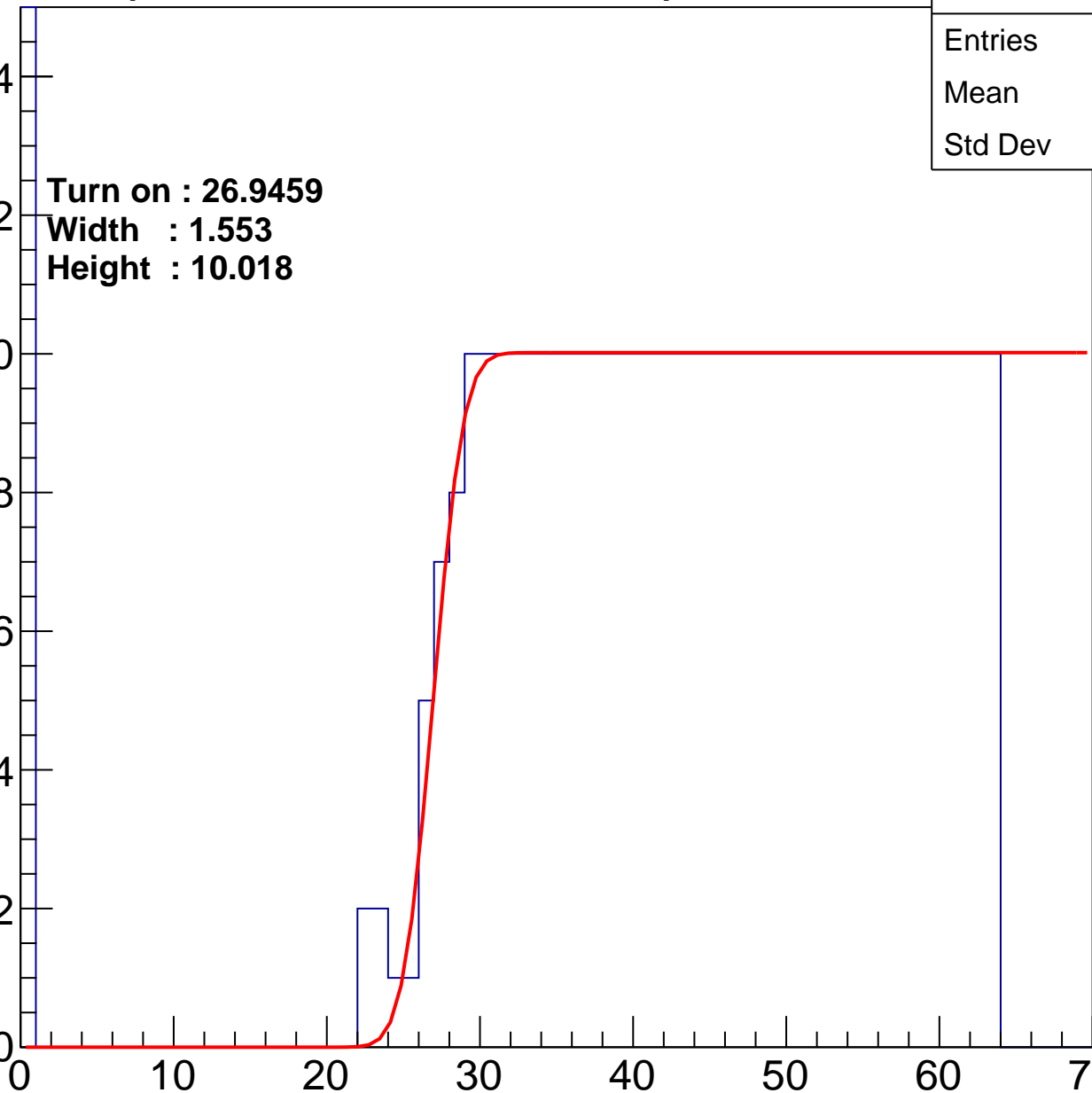
Width : 1.553

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch16

calib_packv5_041523_1651.root, FC#0, port C2

Entries	427
Mean	40.02
Std Dev	16.65

Turn on : 25.6812

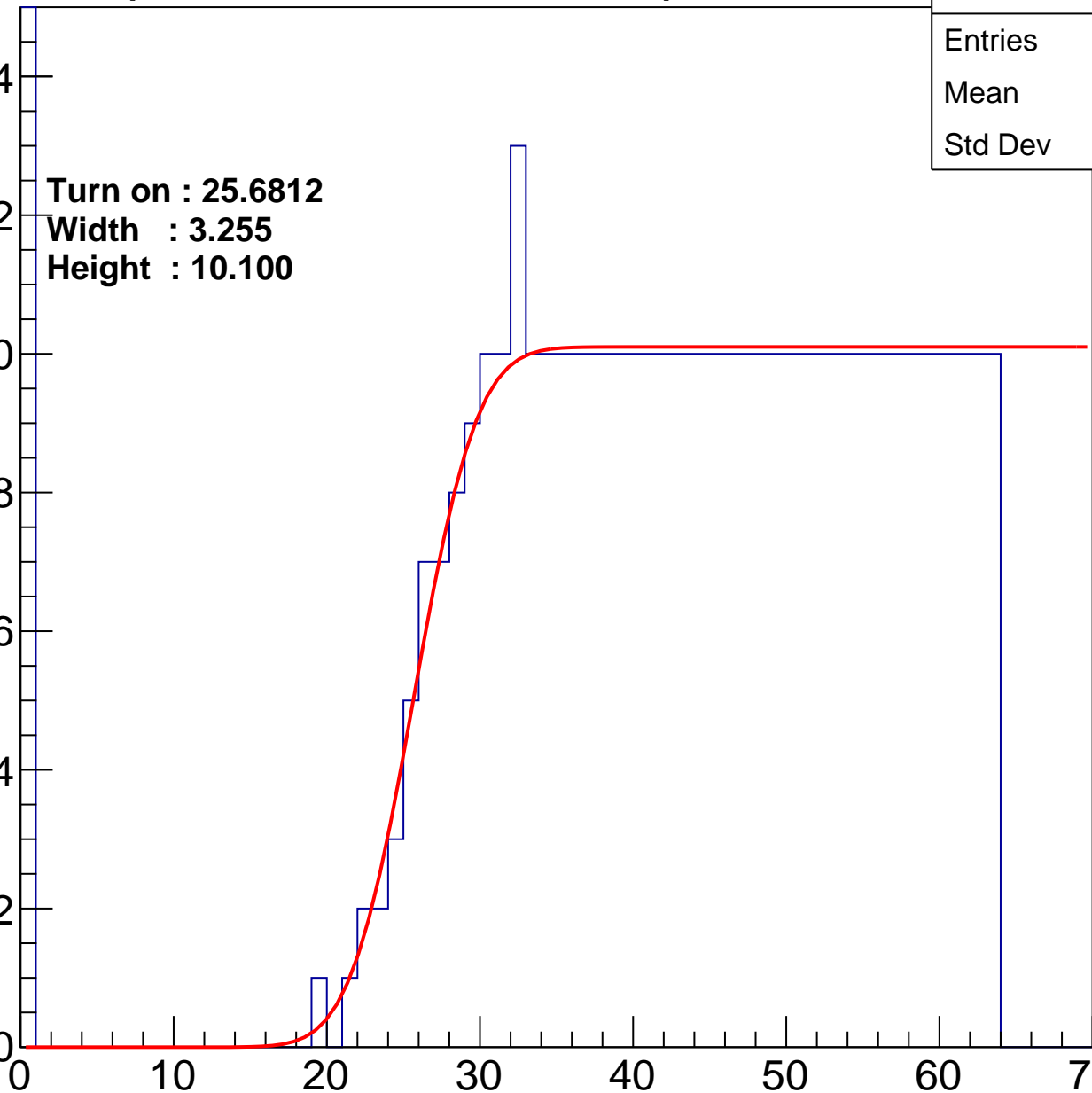
Width : 3.255

Height : 10.100

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch17

calib_packv5_041523_1651.root, FC#0, port C2

Entries	421
Mean	40.01
Std Dev	16.99

Turn on : 26.2534

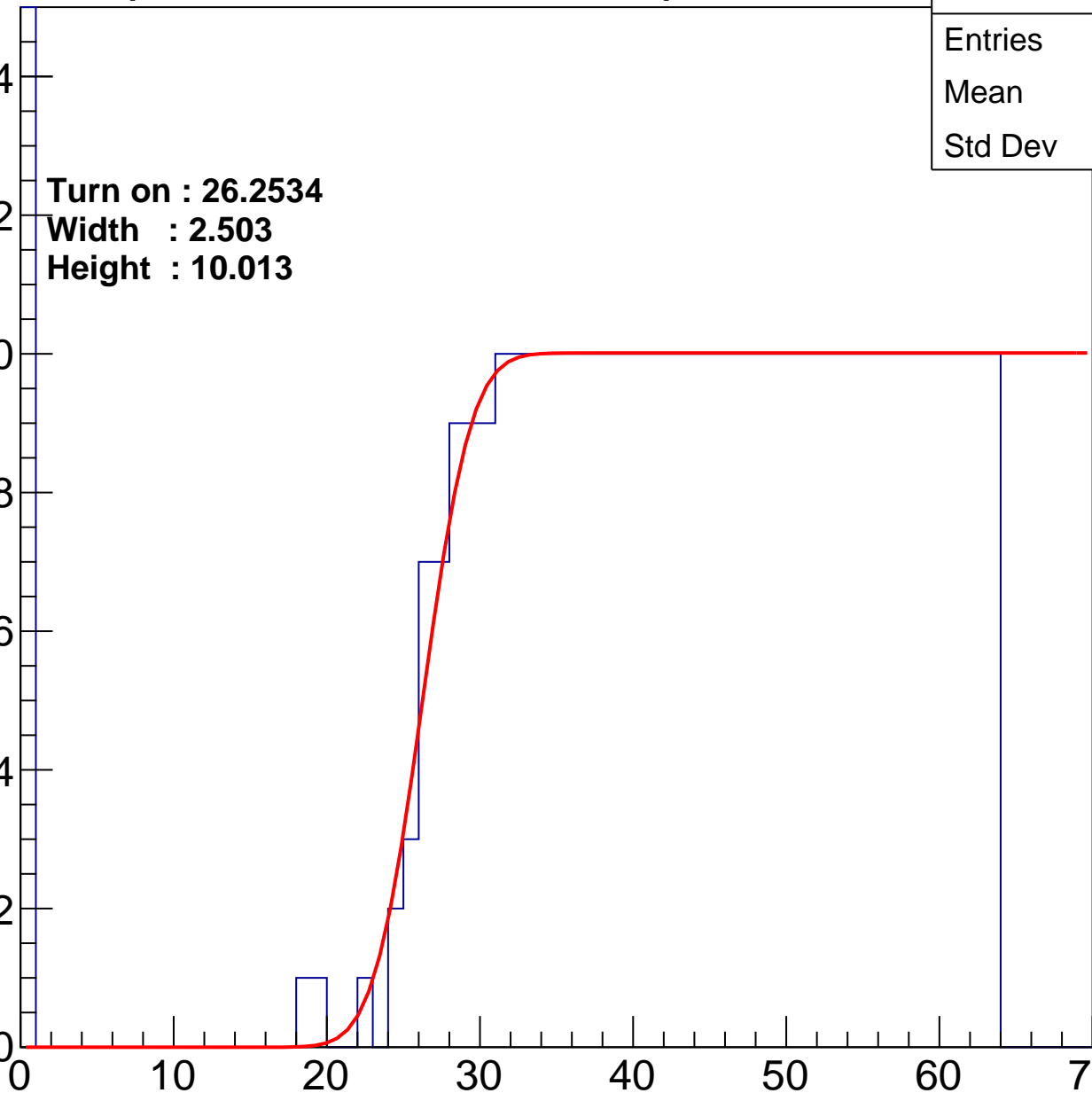
Width : 2.503

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch18

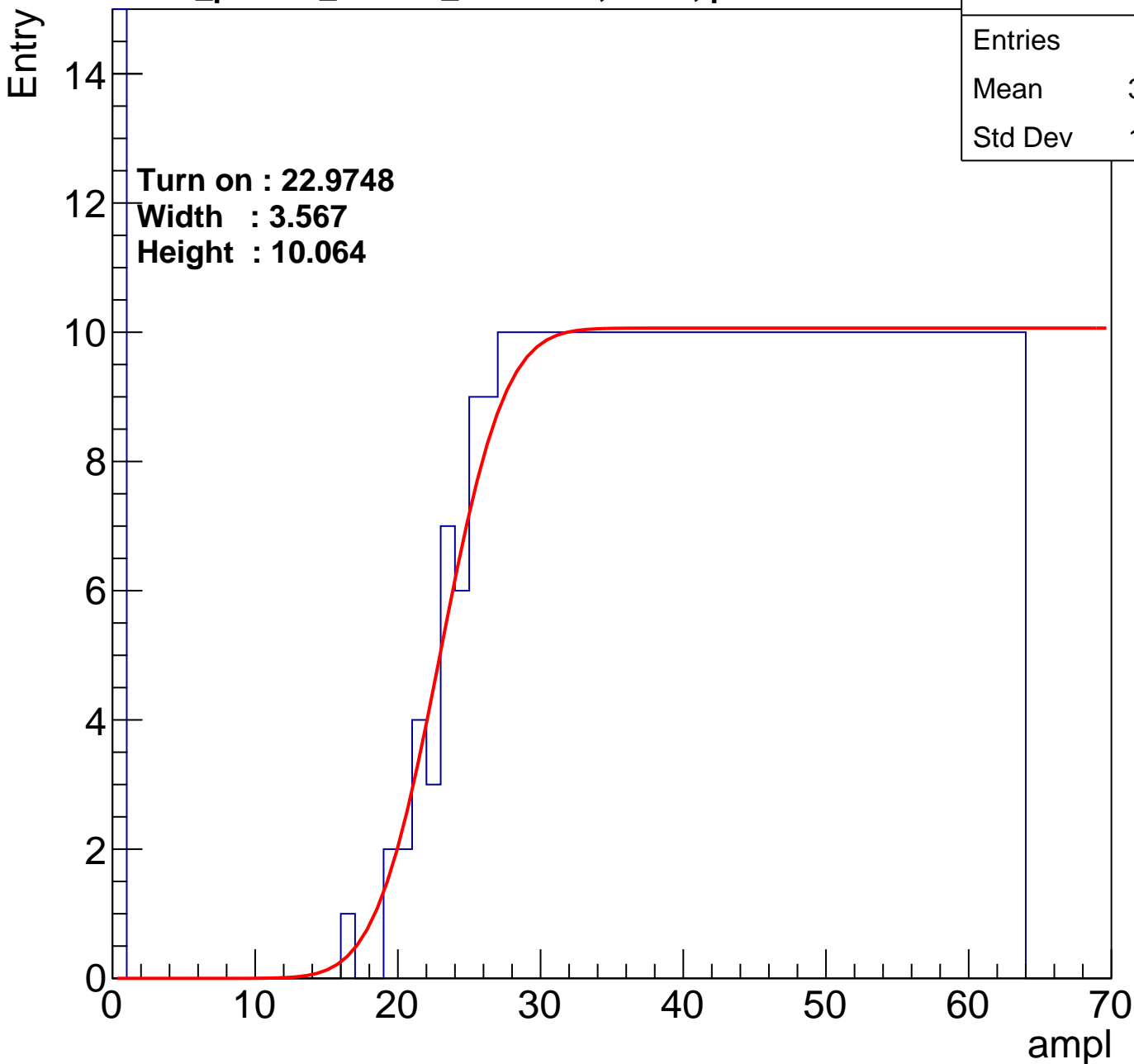
calib_packv5_041523_1651.root, FC#0, port C2

Entries	475
Mean	37.17
Std Dev	18.29

Turn on : 22.9748

Width : 3.567

Height : 10.064



B1L103S, U3-ch19

calib_packv5_041523_1651.root, FC#0, port C2

Entries	413
Mean	40.57
Std Dev	16.6

Turn on : 26.6755

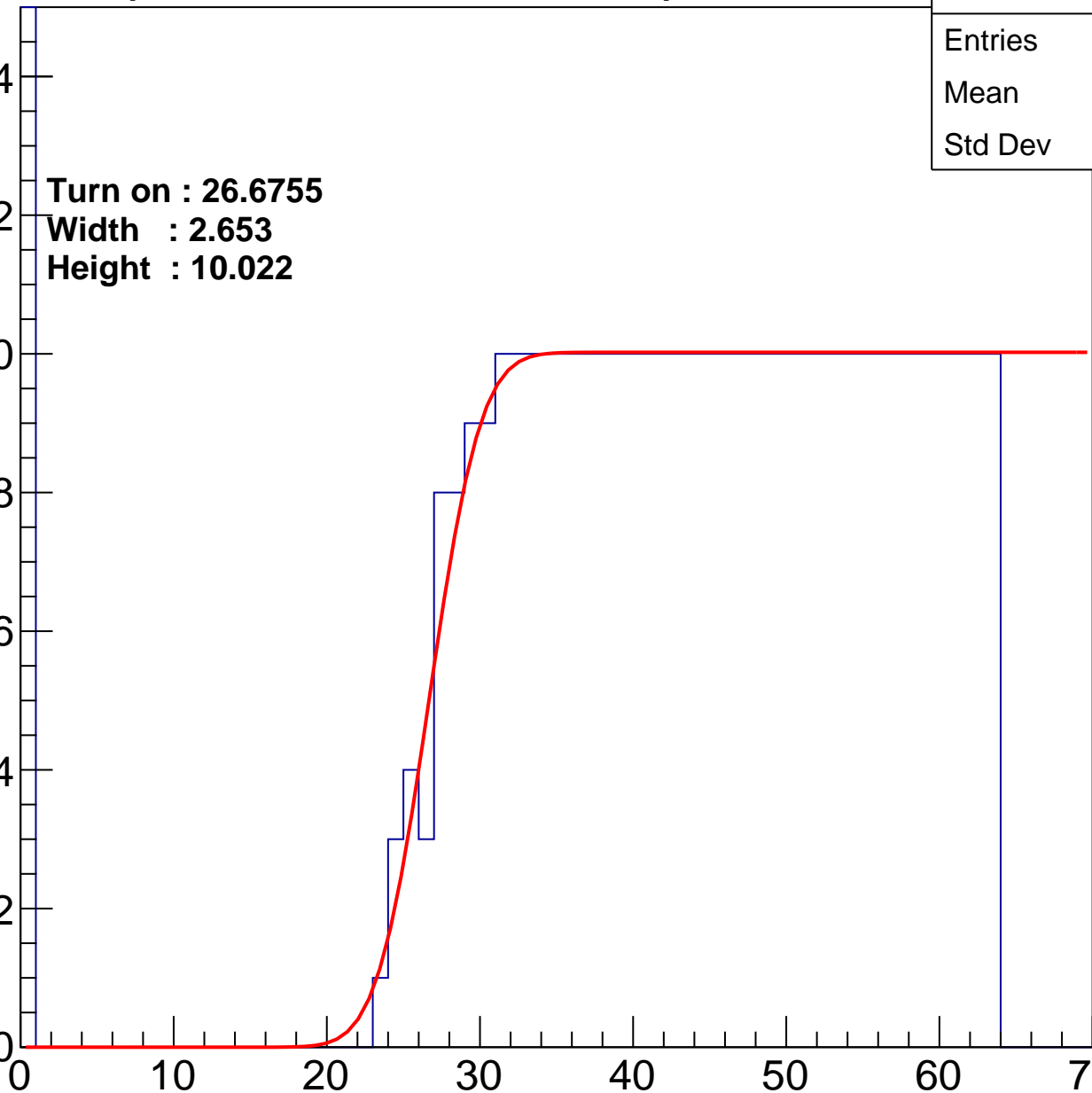
Width : 2.653

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch20

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	39.73
Std Dev	17.33

Turn on : 25.5587

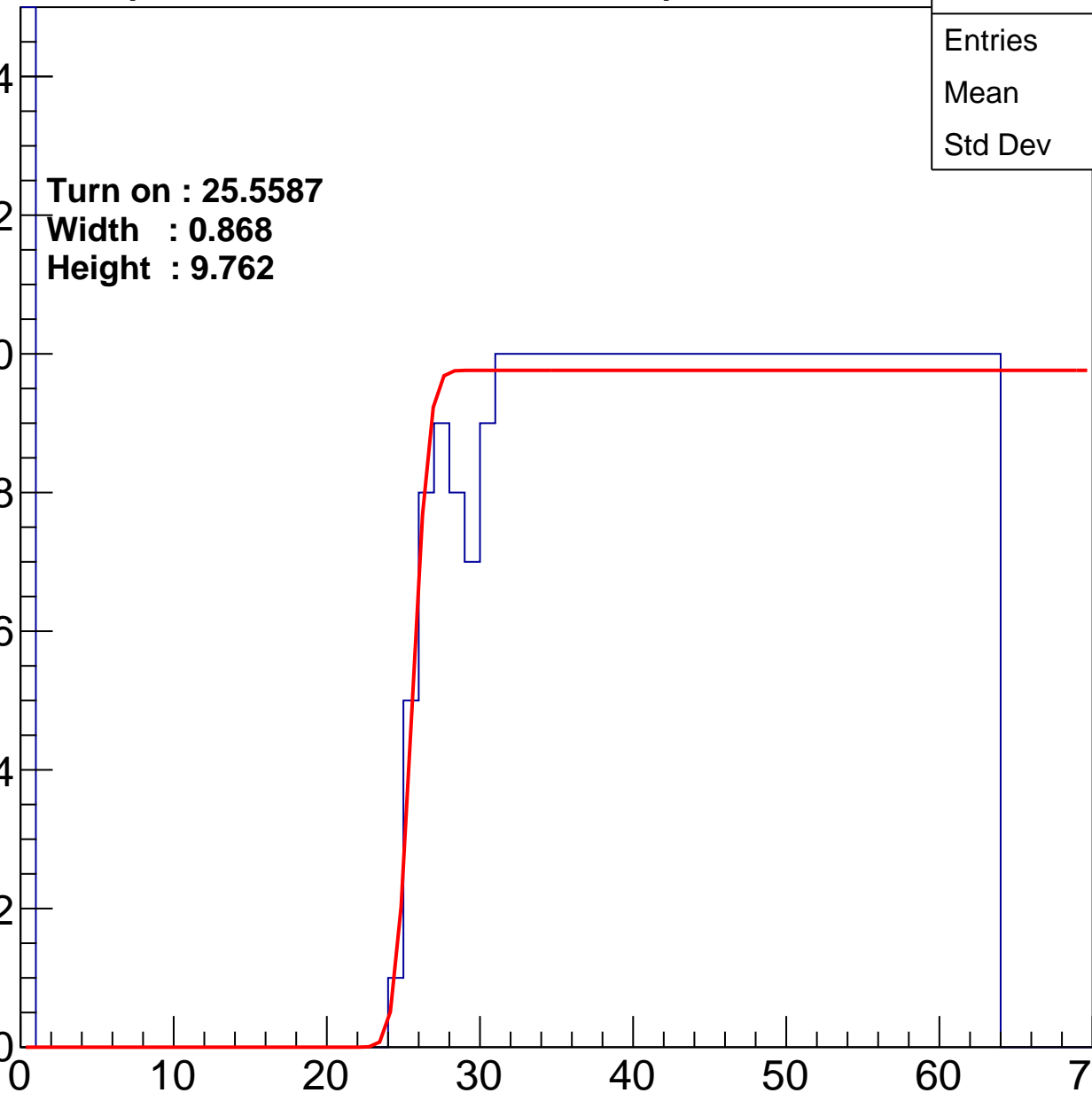
Width : 0.868

Height : 9.762

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch21

calib_packv5_041523_1651.root, FC#0, port C2

Entries	413
Mean	40.03
Std Dev	17.43

Turn on : 27.5300

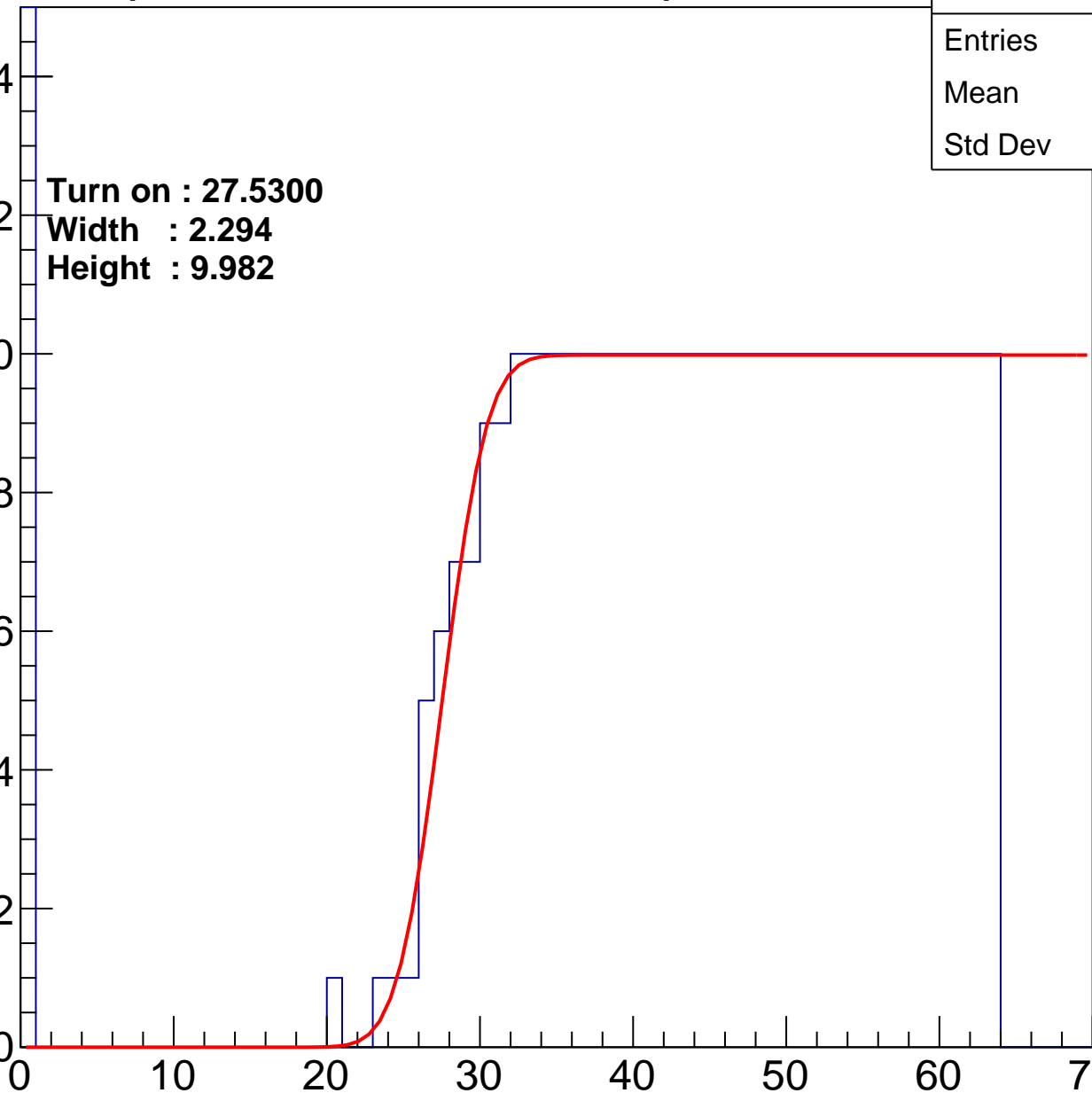
Width : 2.294

Height : 9.982

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch22

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	39.32
Std Dev	16.8

Turn on : 24.3431

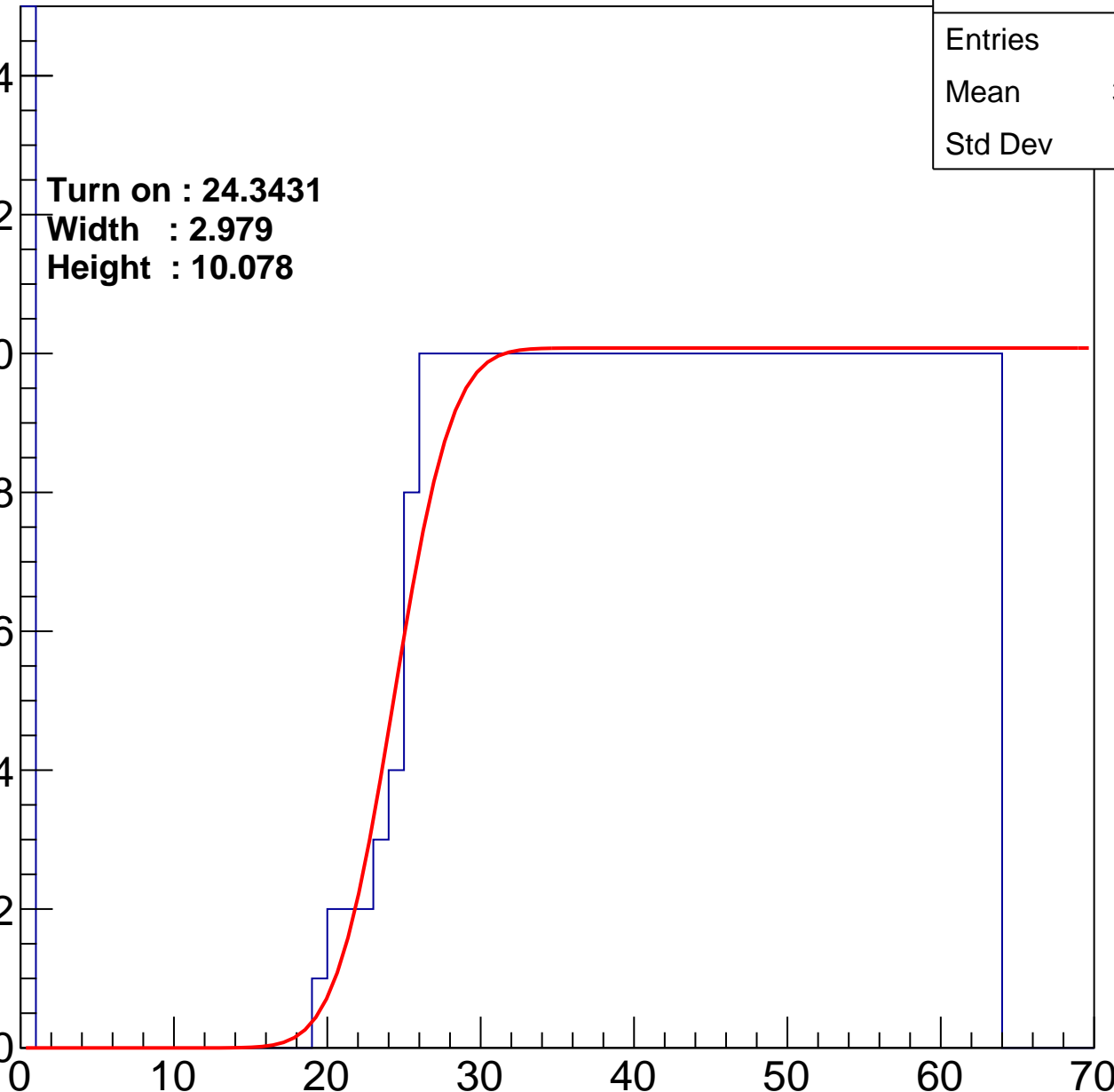
Width : 2.979

Height : 10.078

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch23

calib_packv5_041523_1651.root, FC#0, port C2

Entries	413
Mean	40.15
Std Dev	17.23

Turn on : 27.1400

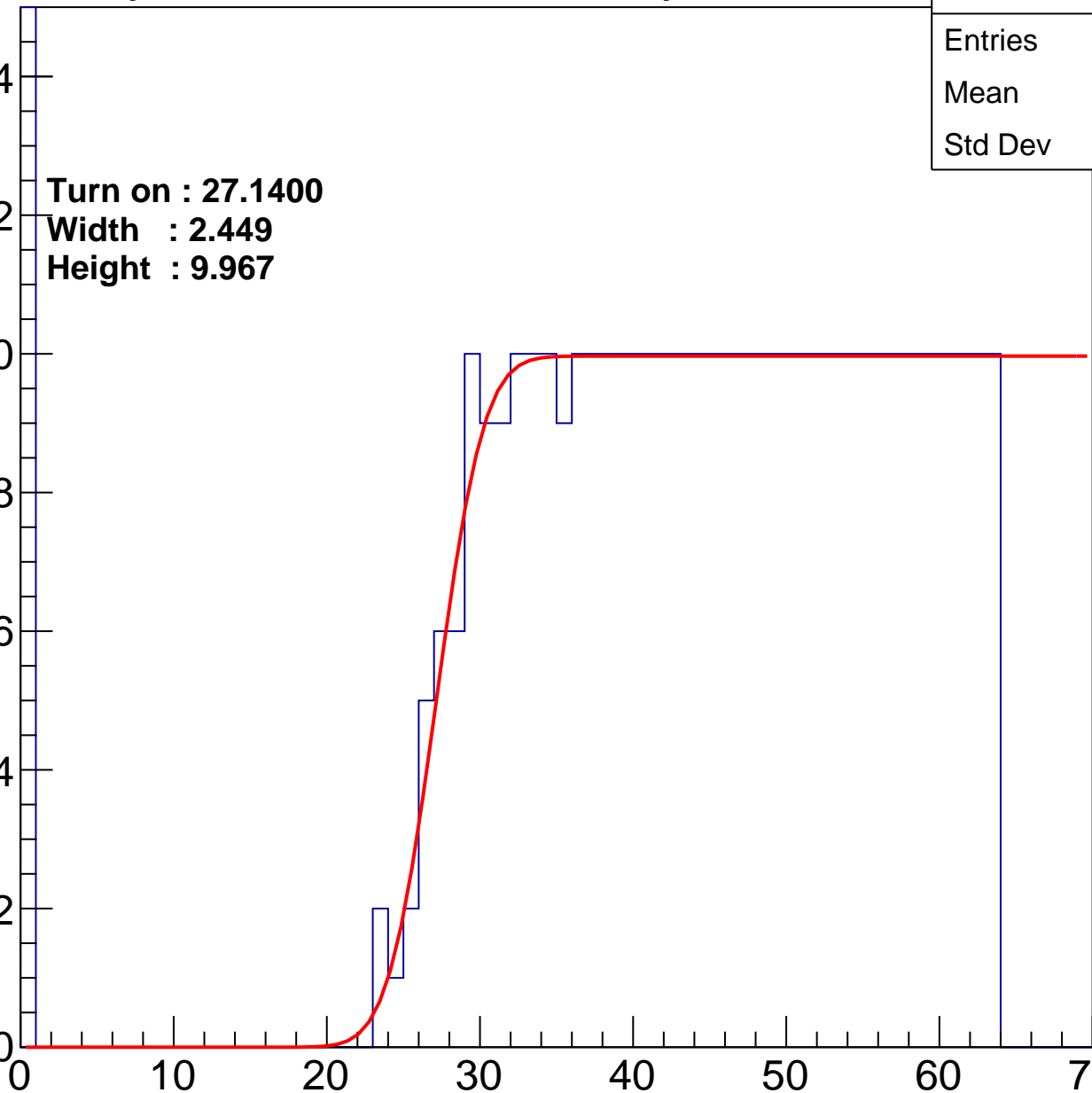
Width : 2.449

Height : 9.967

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch24

calib_packv5_041523_1651.root, FC#0, port C2

Entries	453
Mean	38.22
Std Dev	17.92

Turn on : 24.2235

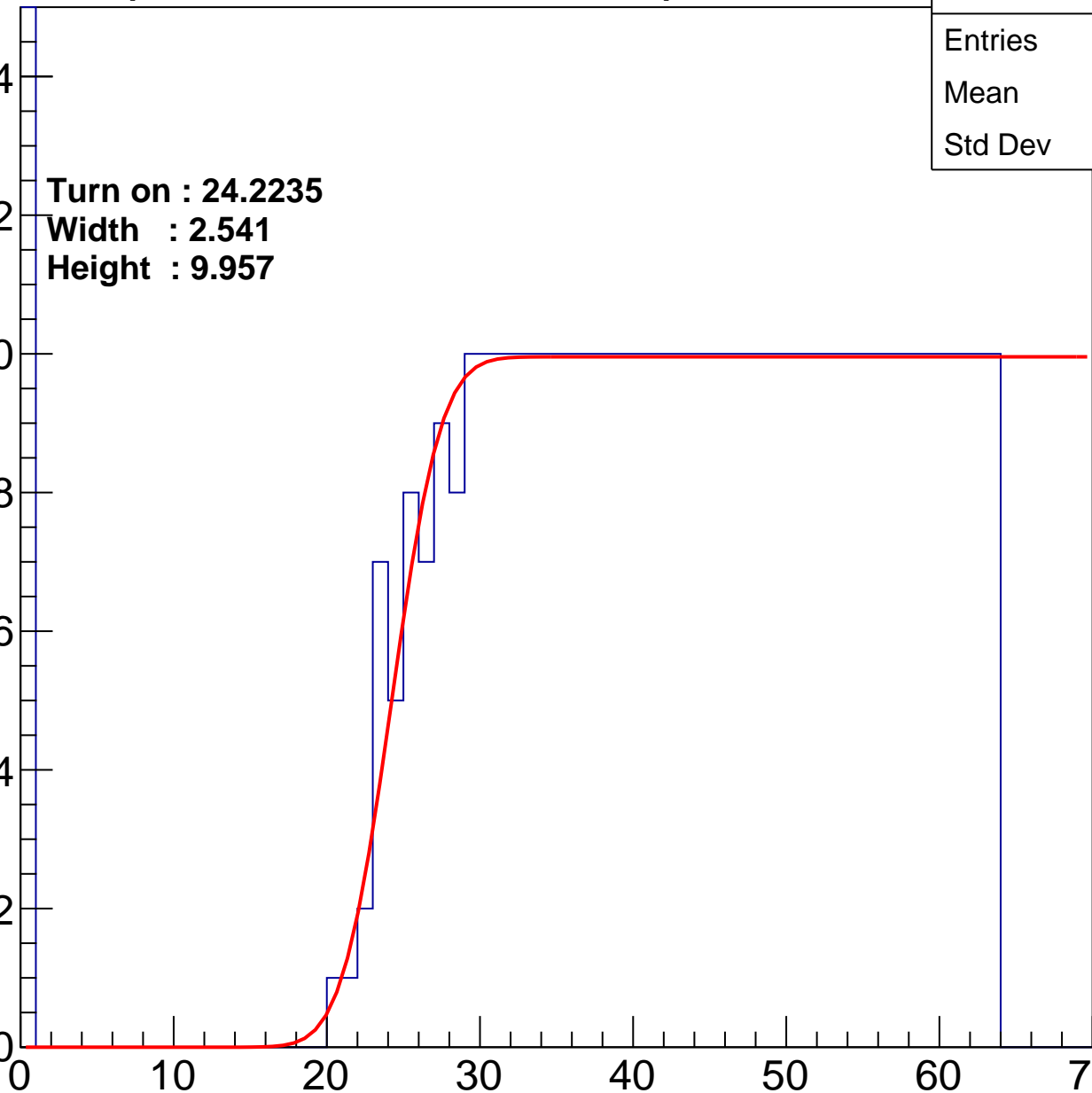
Width : 2.541

Height : 9.957

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch25

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	38.96
Std Dev	17.59

Turn on : 25.4805

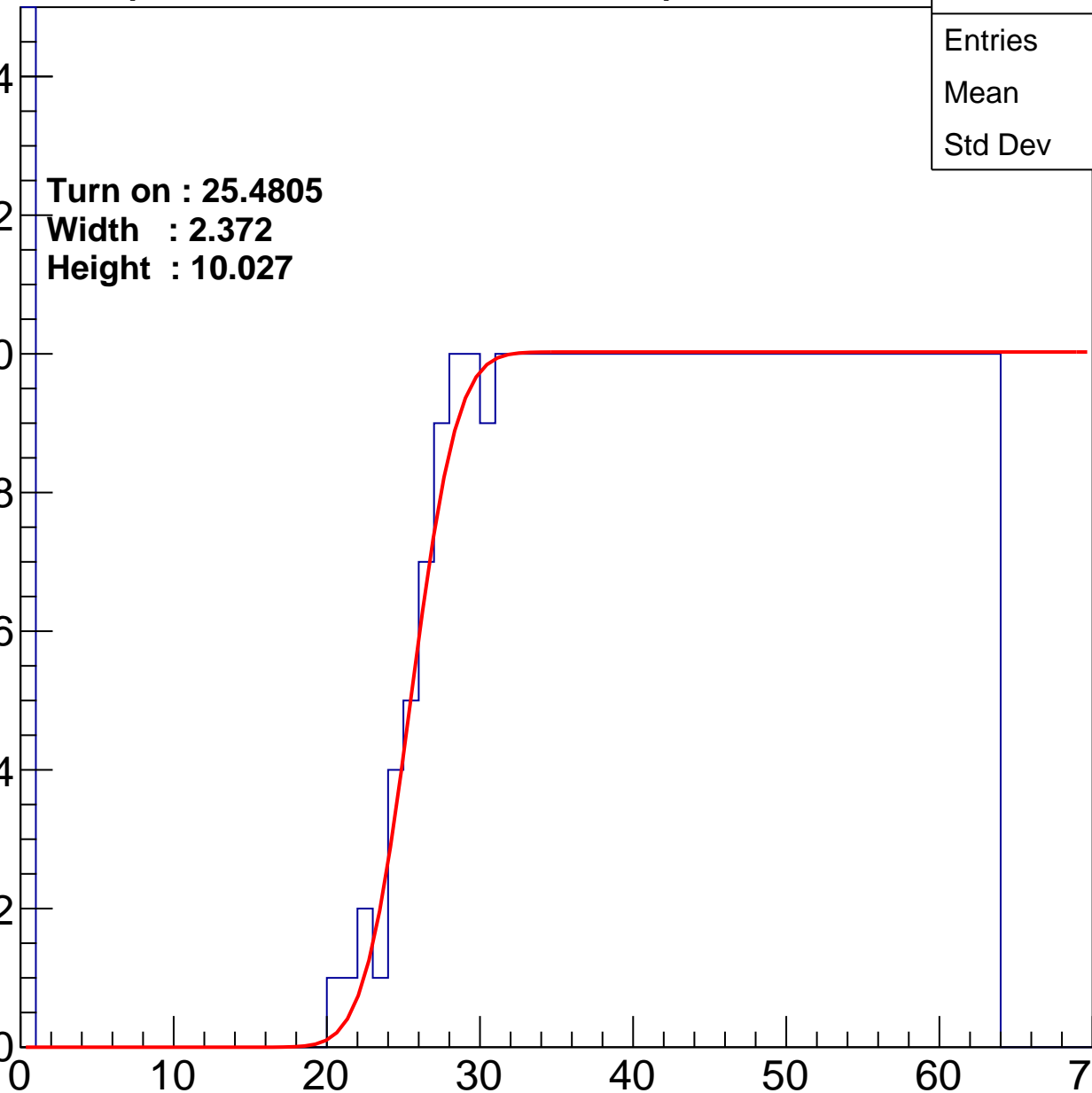
Width : 2.372

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch26

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	39.05
Std Dev	17.65

Turn on : 25.3122

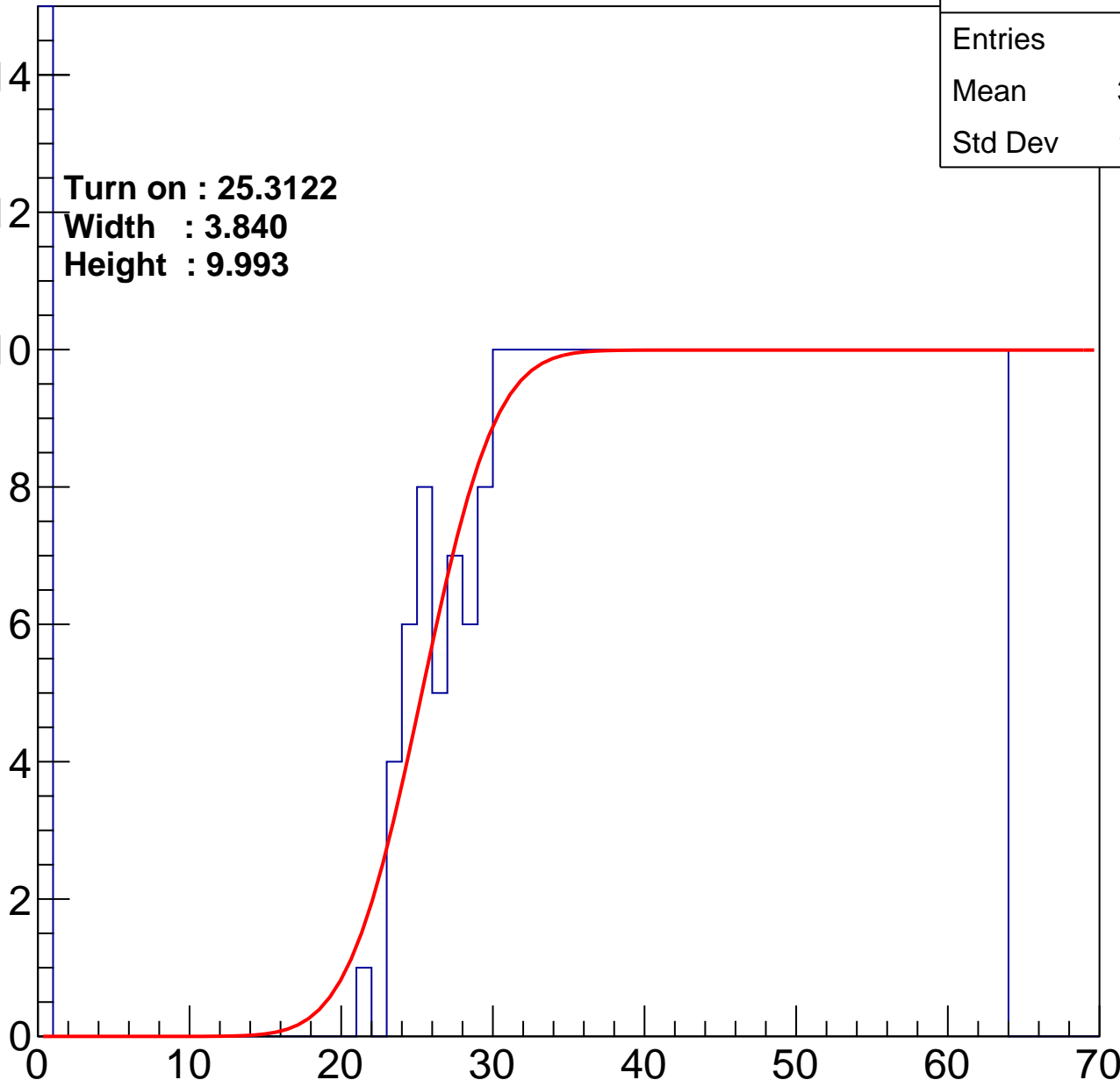
Width : 3.840

Height : 9.993

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch27

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	39.2
Std Dev	17.35

Turn on : 24.5235

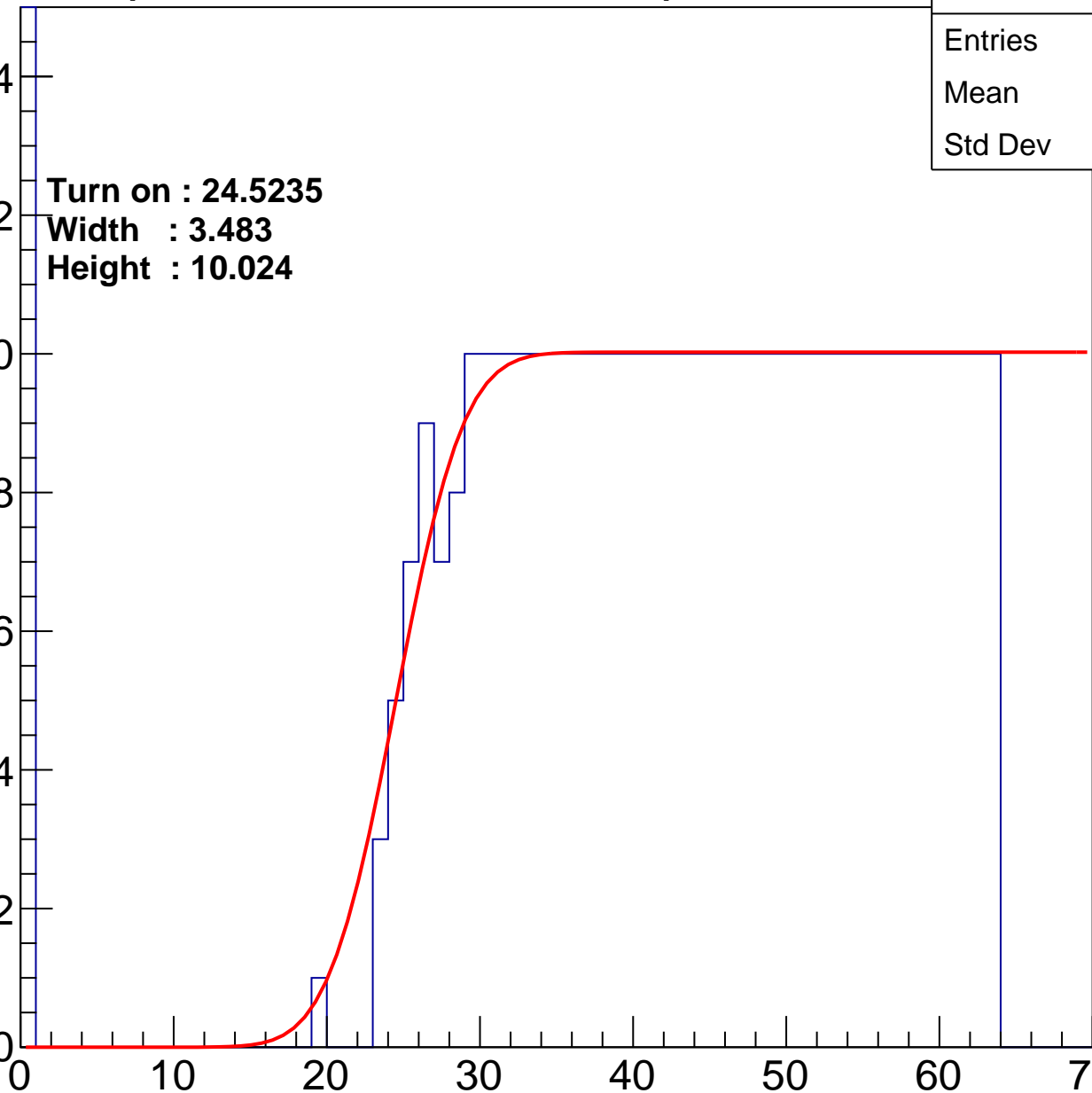
Width : 3.483

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch28

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	40.1
Std Dev	17.07

Turn on : 26.7031

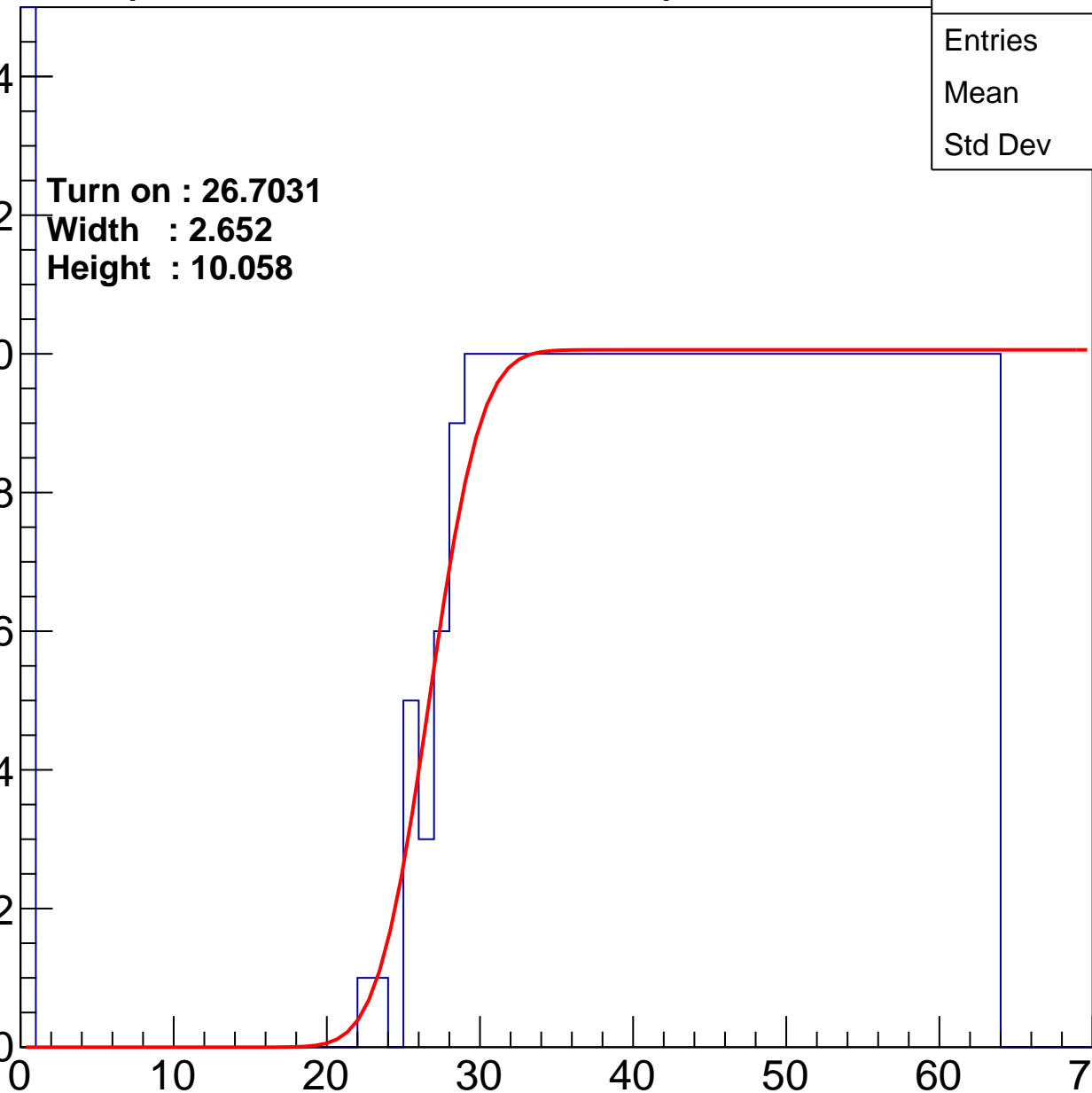
Width : 2.652

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch29

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	38.23
Std Dev	18.68

Turn on : 26.6405

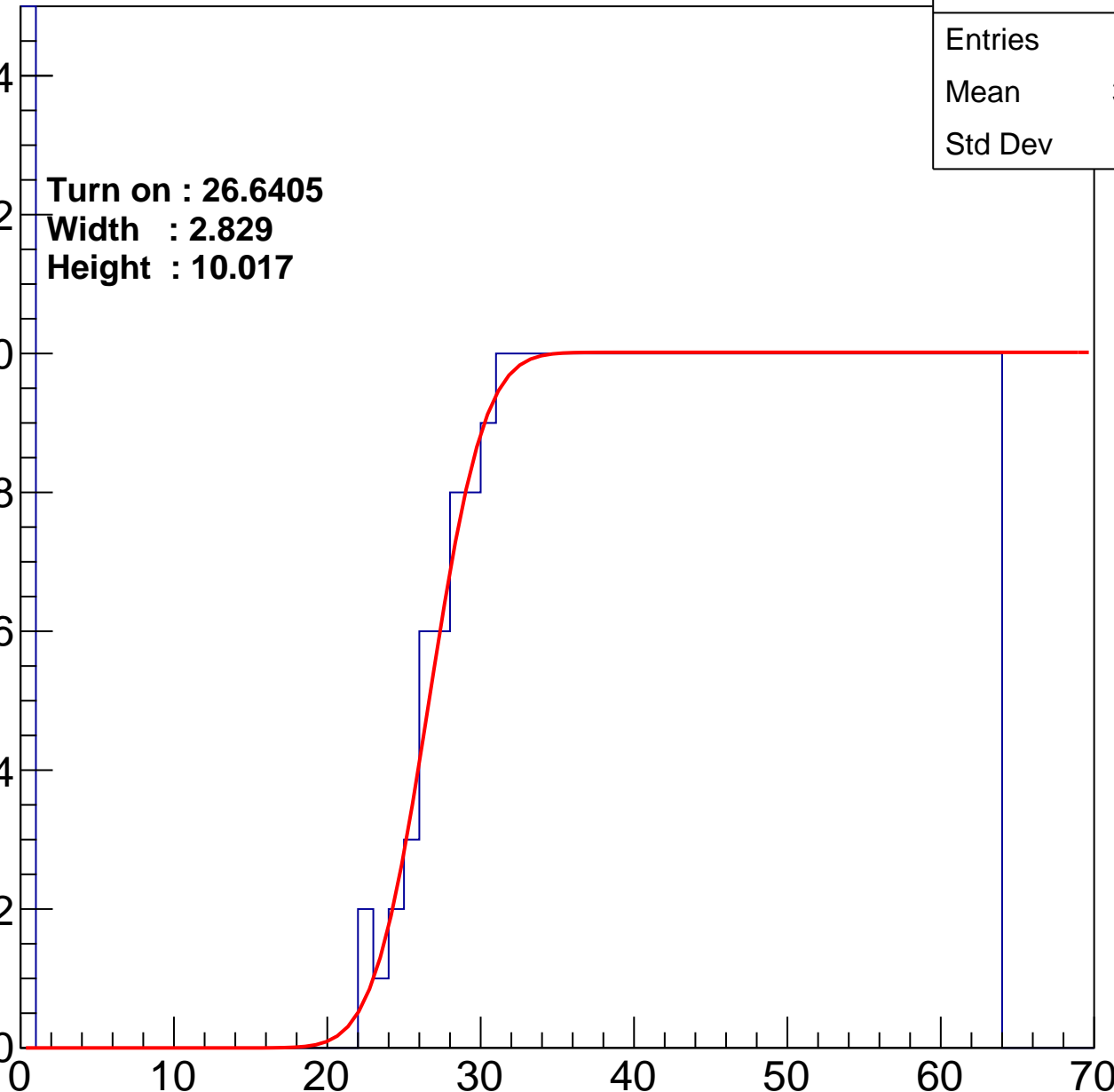
Width : 2.829

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch30

calib_packv5_041523_1651.root, FC#0, port C2

Entries	457
Mean	37.61
Std Dev	18.56

Turn on : 24.5748

Width : 2.307

Height : 9.917

Entry

14

12

10

8

6

4

2

0

0

10

20

30

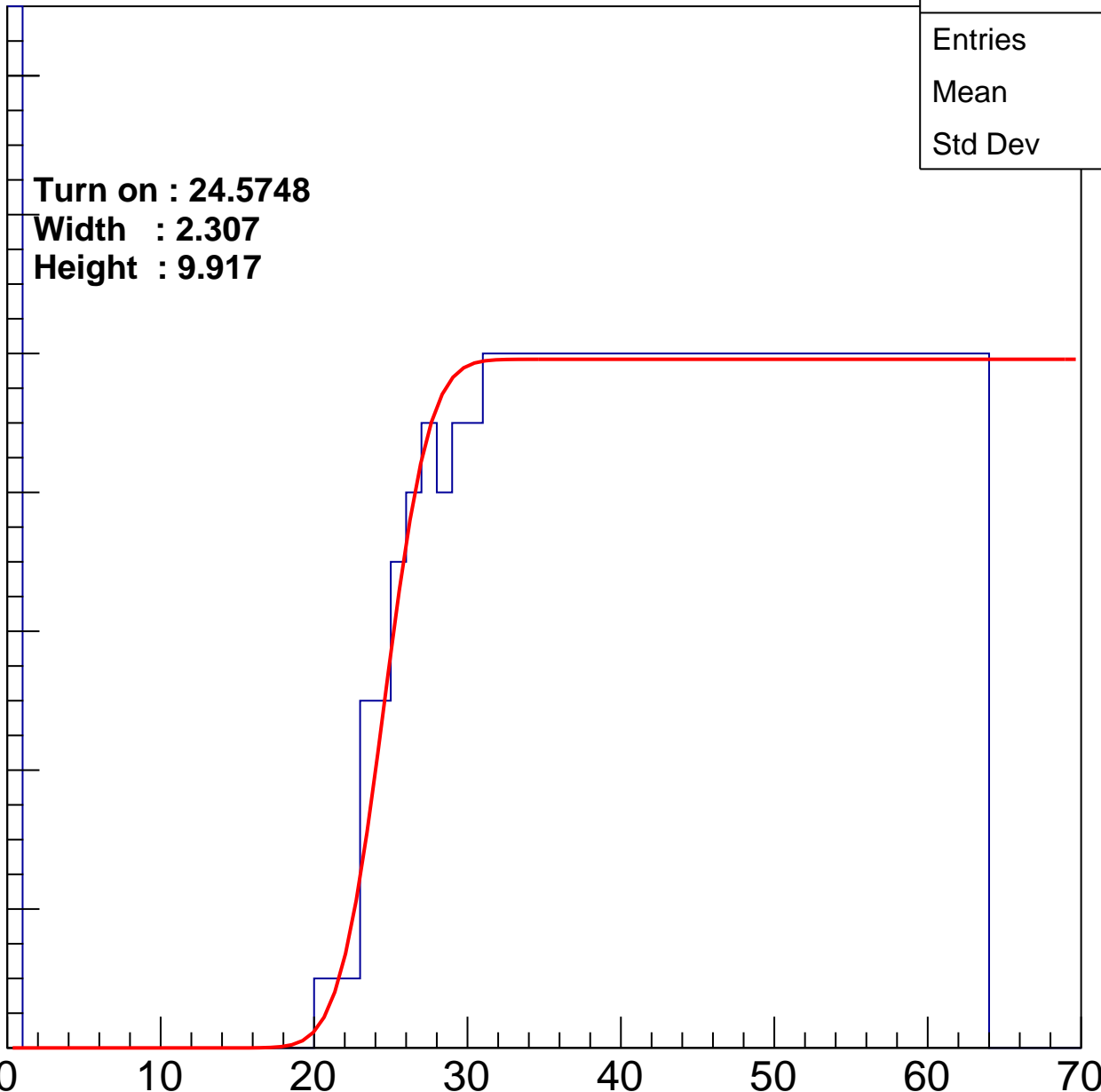
40

50

60

70

ampl



B1L103S, U3-ch31

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	38.43
Std Dev	18.22

Turn on : 26.0678

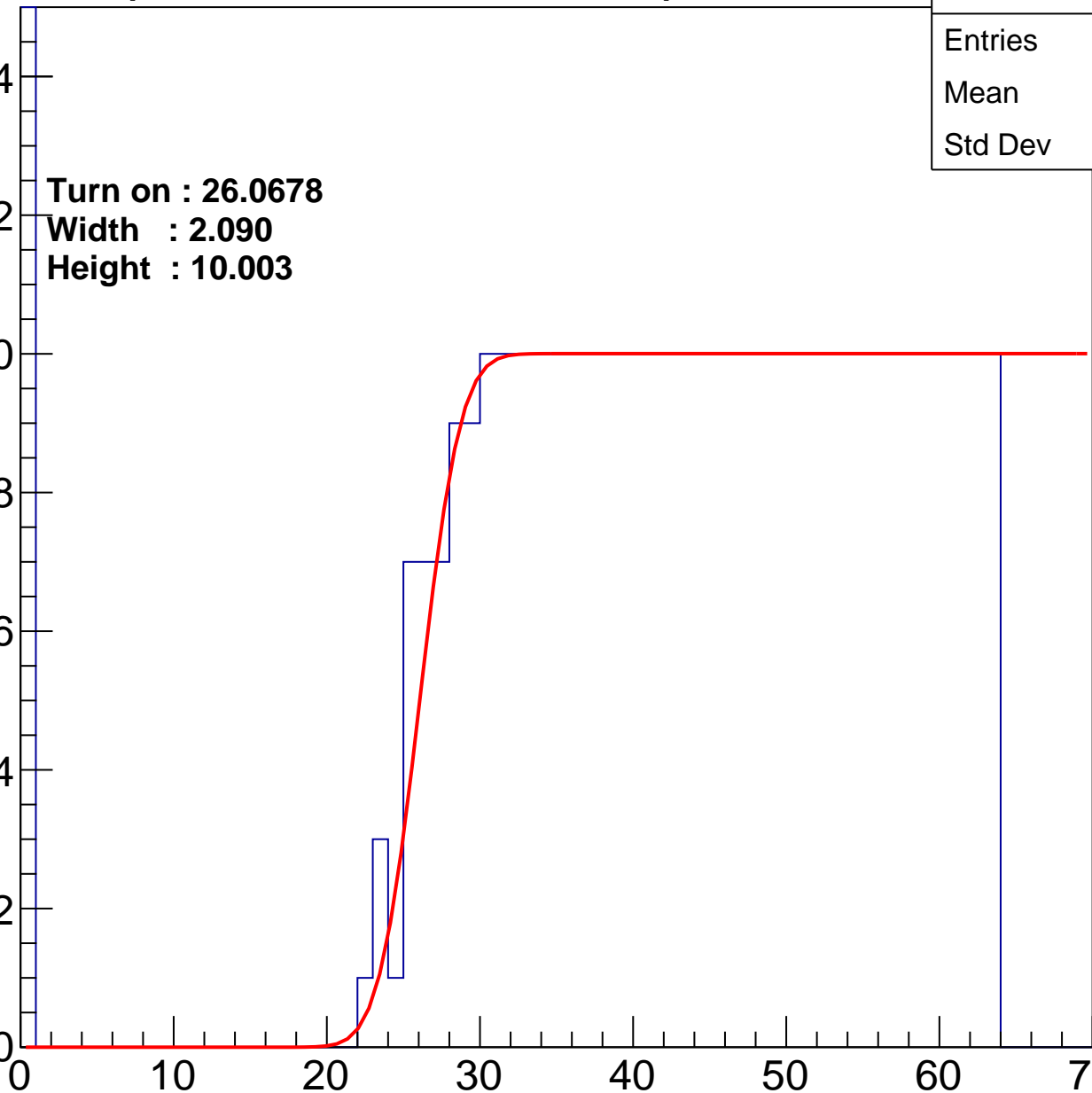
Width : 2.090

Height : 10.003

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch32

calib_packv5_041523_1651.root, FC#0, port C2

Entries	478
Mean	36.79
Std Dev	18.66

Turn on : 22.9440

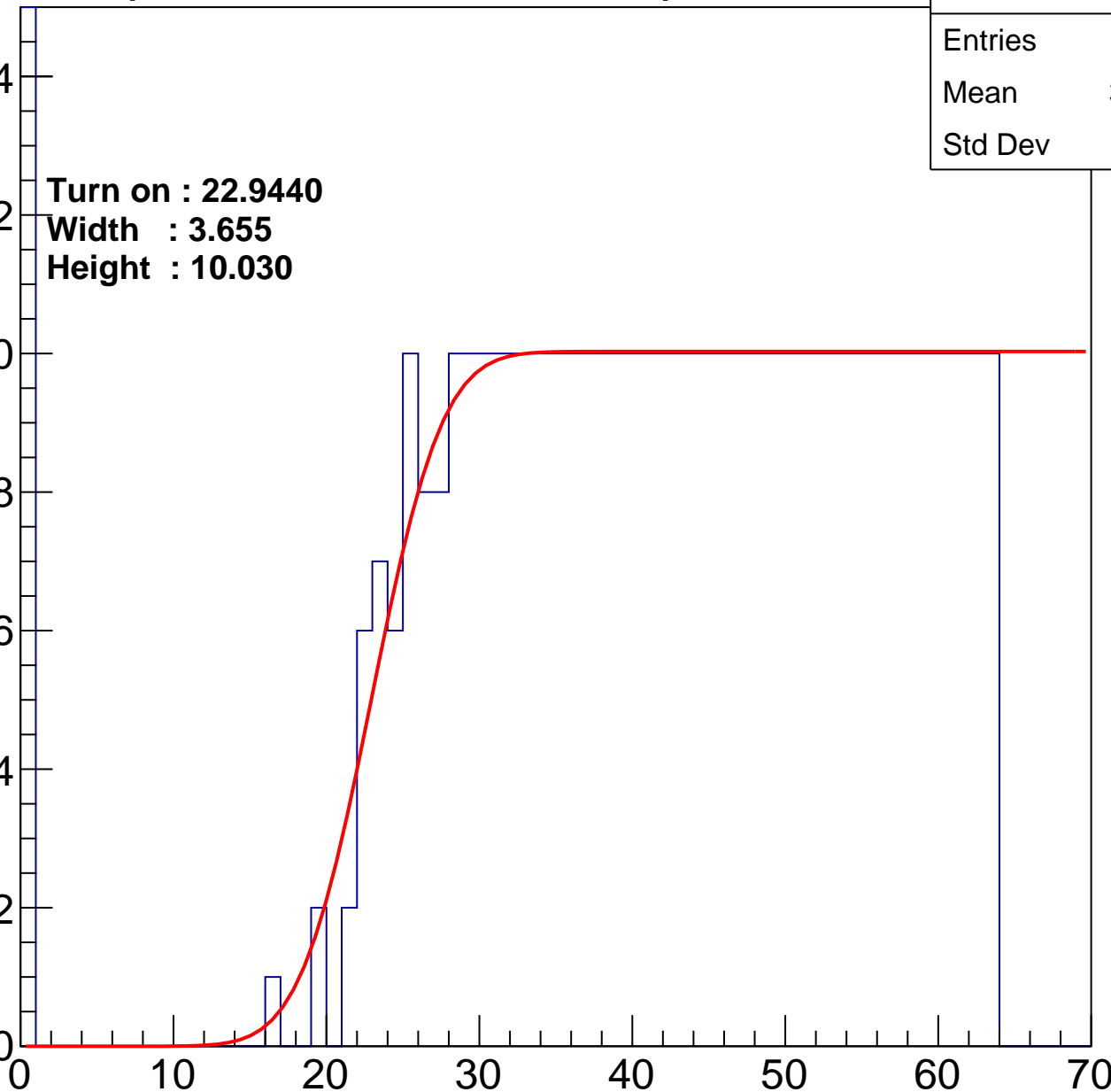
Width : 3.655

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch33

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	38.37
Std Dev	18.64

Turn on : 27.2664

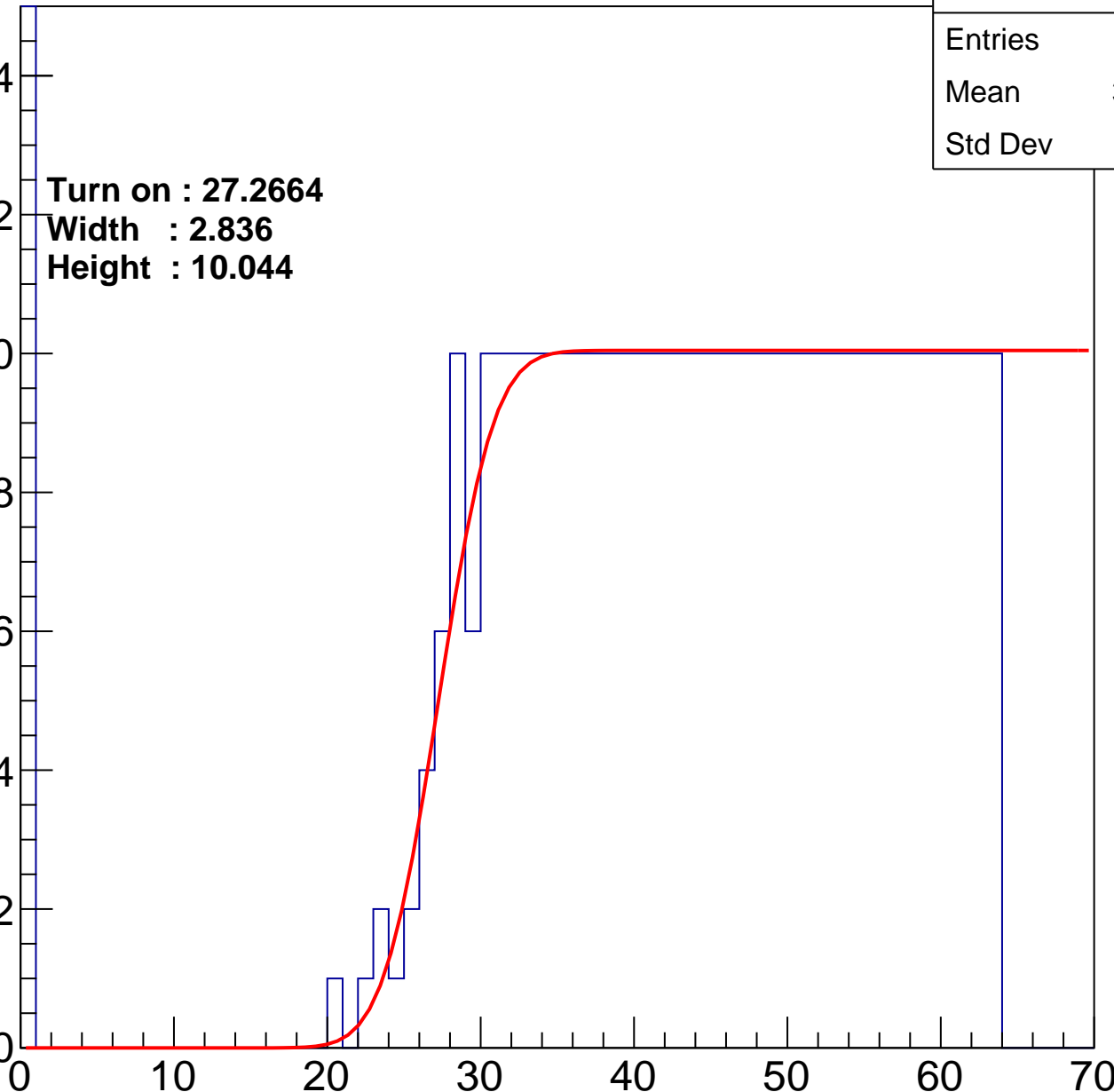
Width : 2.836

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch34

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	38.64
Std Dev	18.18

Turn on : 26.1657

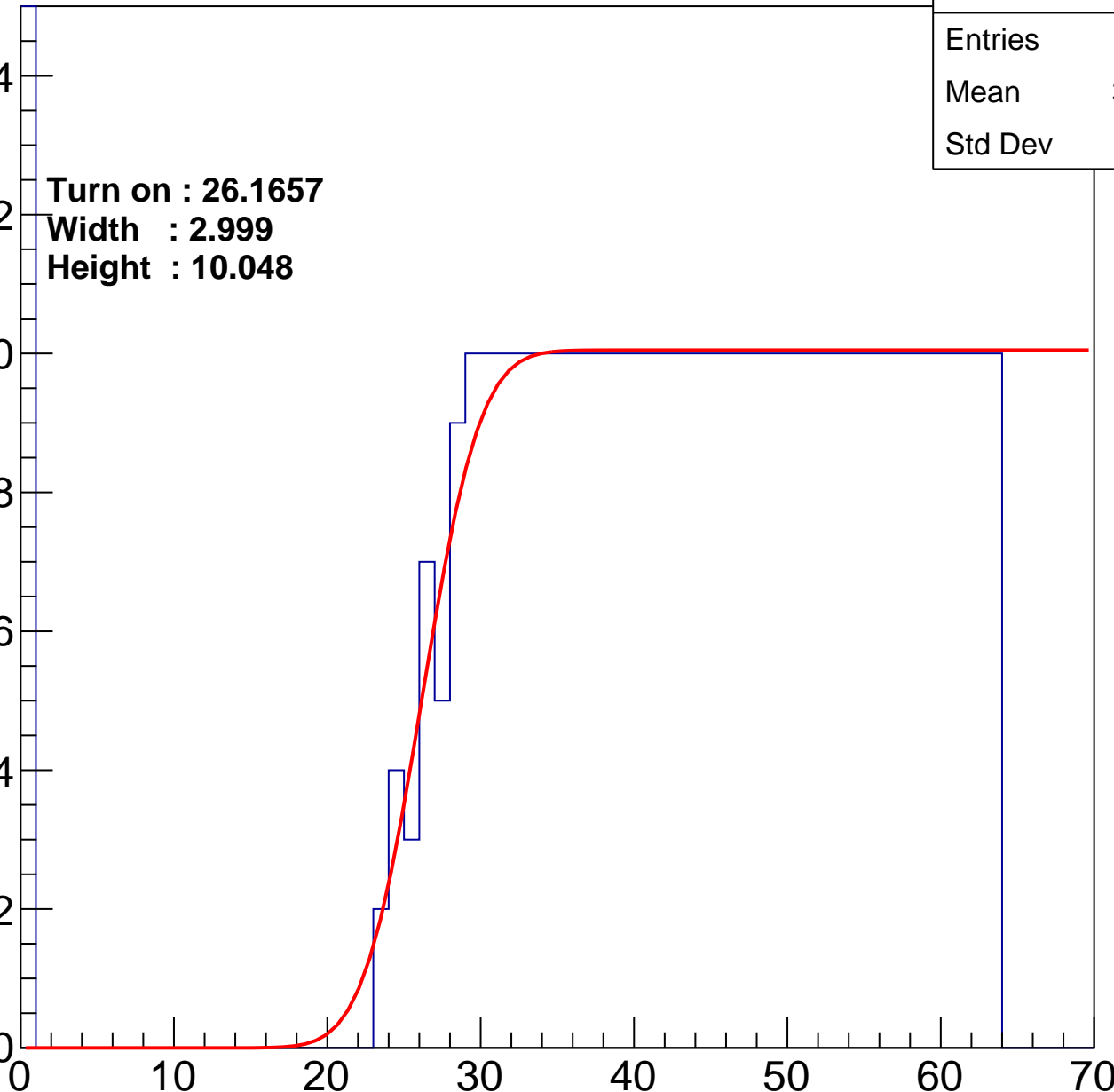
Width : 2.999

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch35

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	38.51
Std Dev	18.22

Turn on : 26.7773

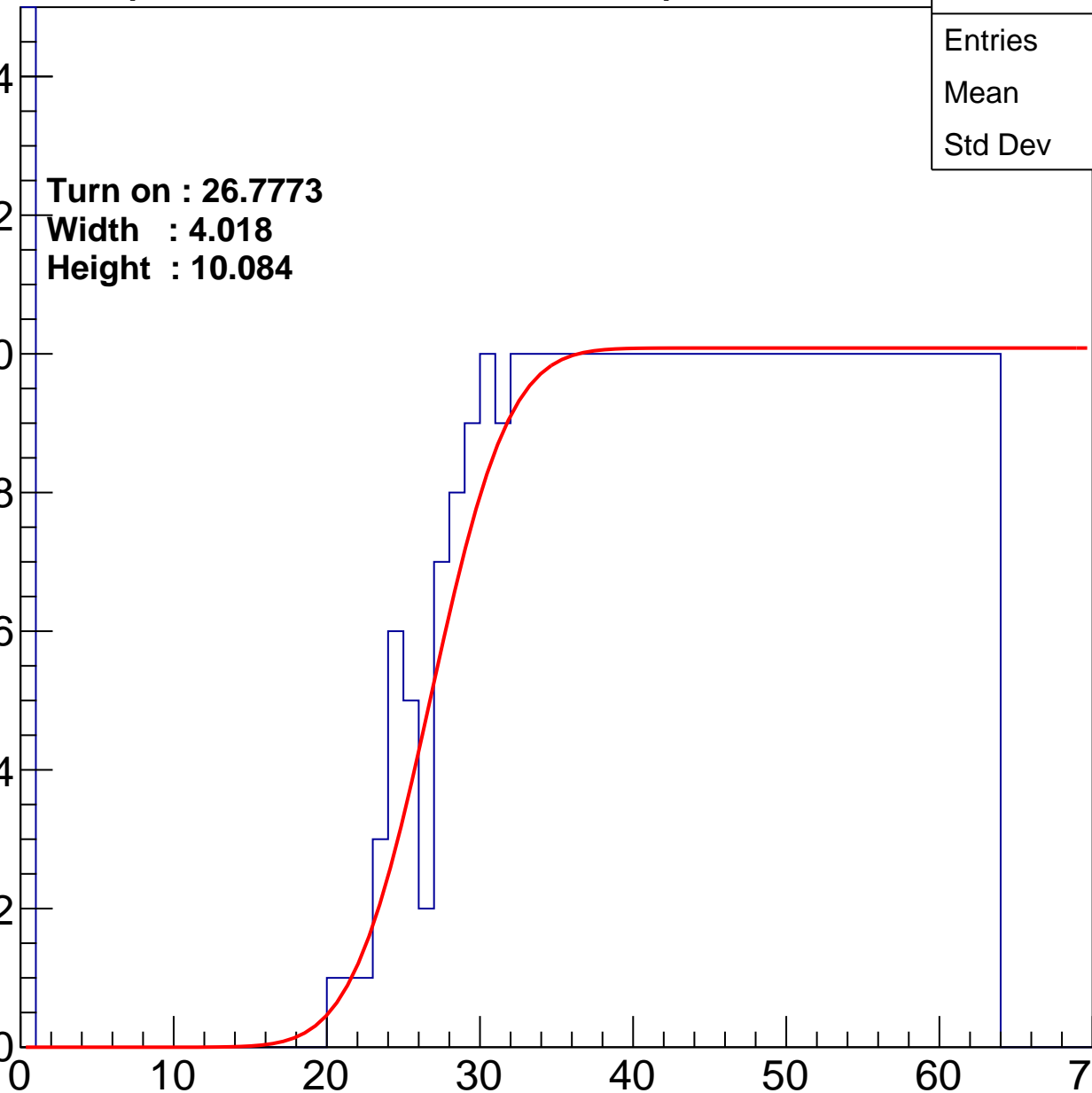
Width : 4.018

Height : 10.084

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch36

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	39.14
Std Dev	17.15

Turn on : 24.2436

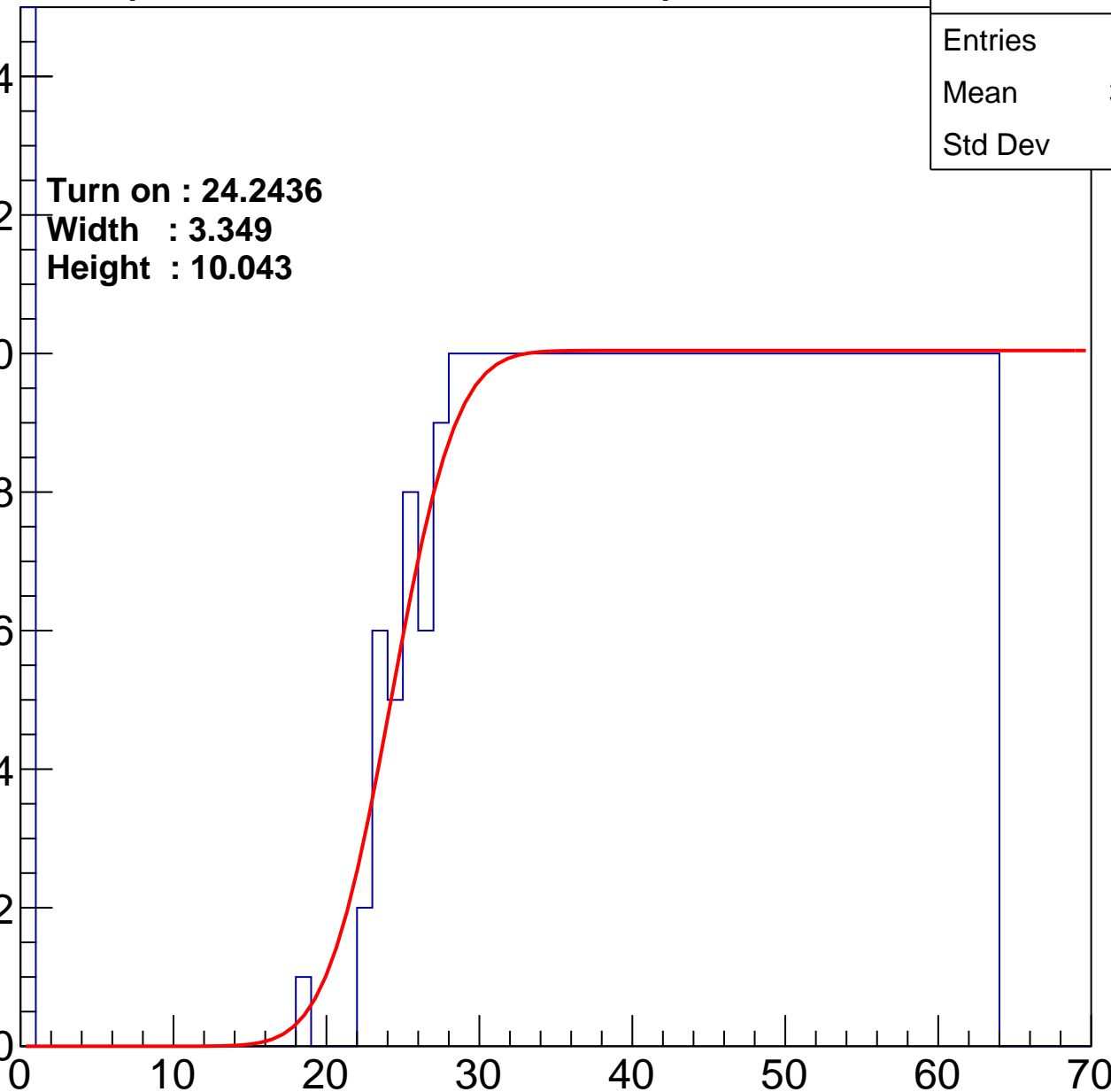
Width : 3.349

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch37

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	39.75
Std Dev	16.86

Turn on : 25.0889

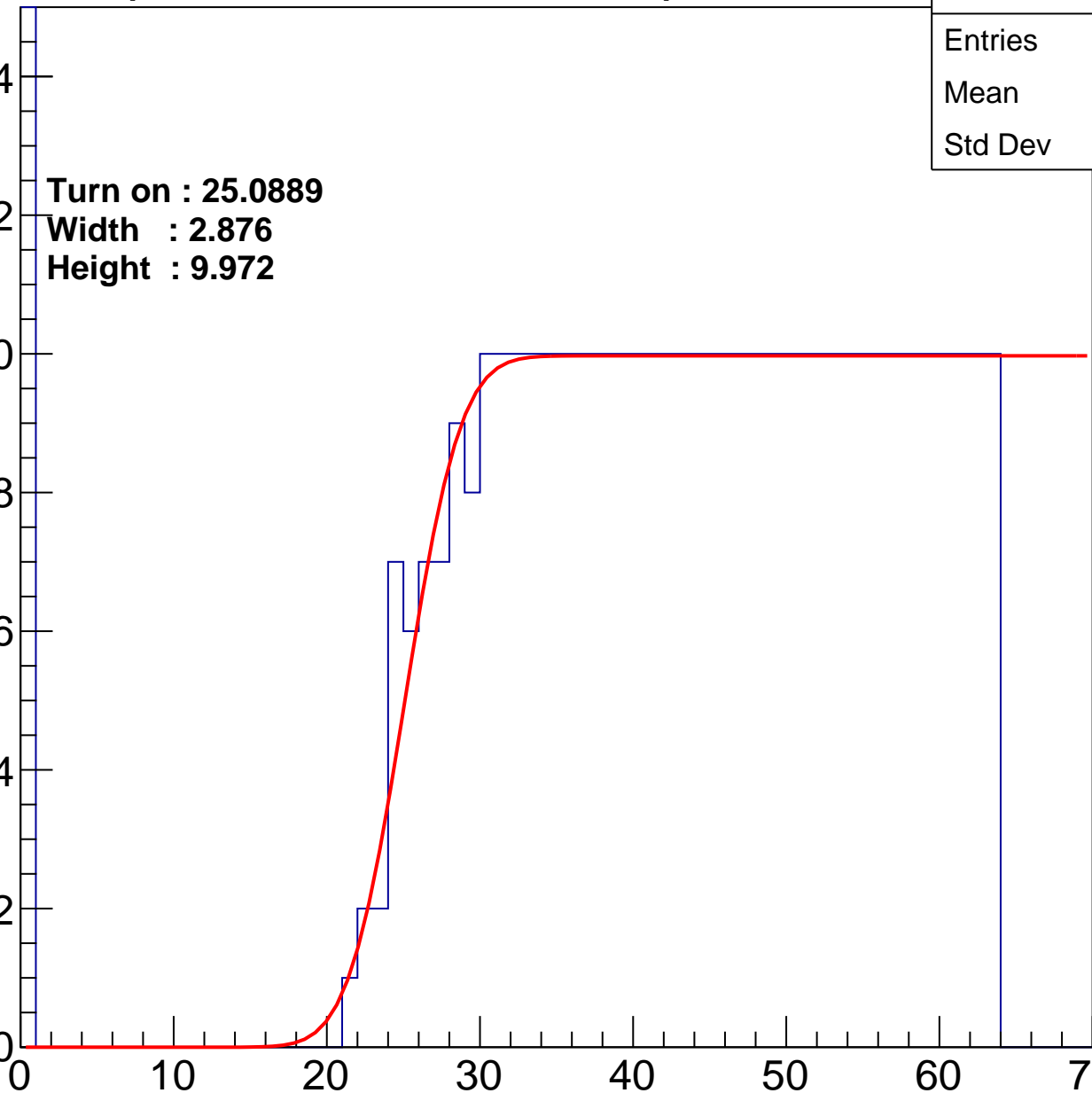
Width : 2.876

Height : 9.972

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch38

calib_packv5_041523_1651.root, FC#0, port C2

Entries	454
Mean	37.61
Std Dev	18.73

Turn on : 25.2583

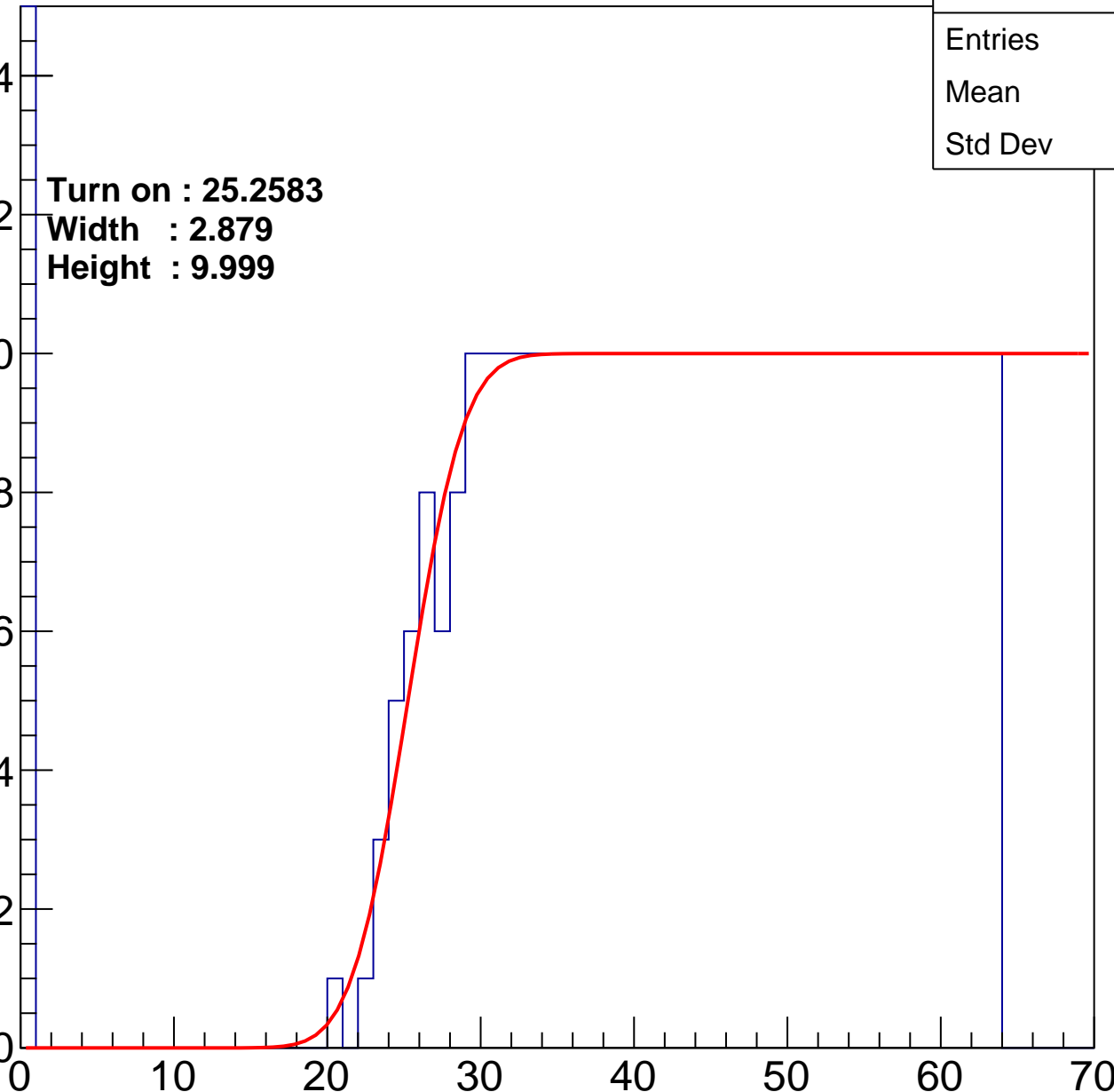
Width : 2.879

Height : 9.999

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch39

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	40.06
Std Dev	16.71

Turn on : 25.2010

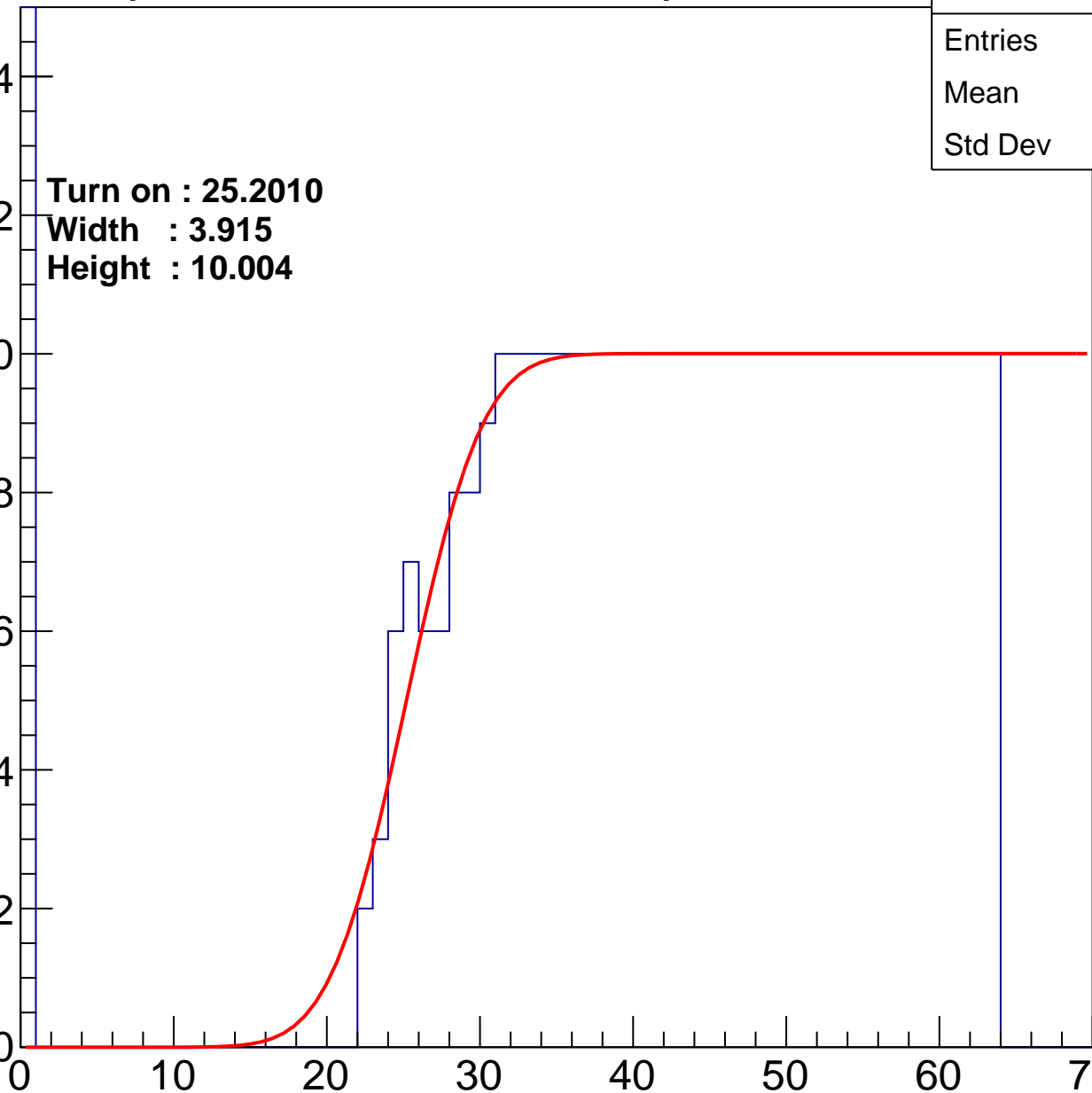
Width : 3.915

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch40

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	38.95
Std Dev	18.07

Turn on : 26.7911

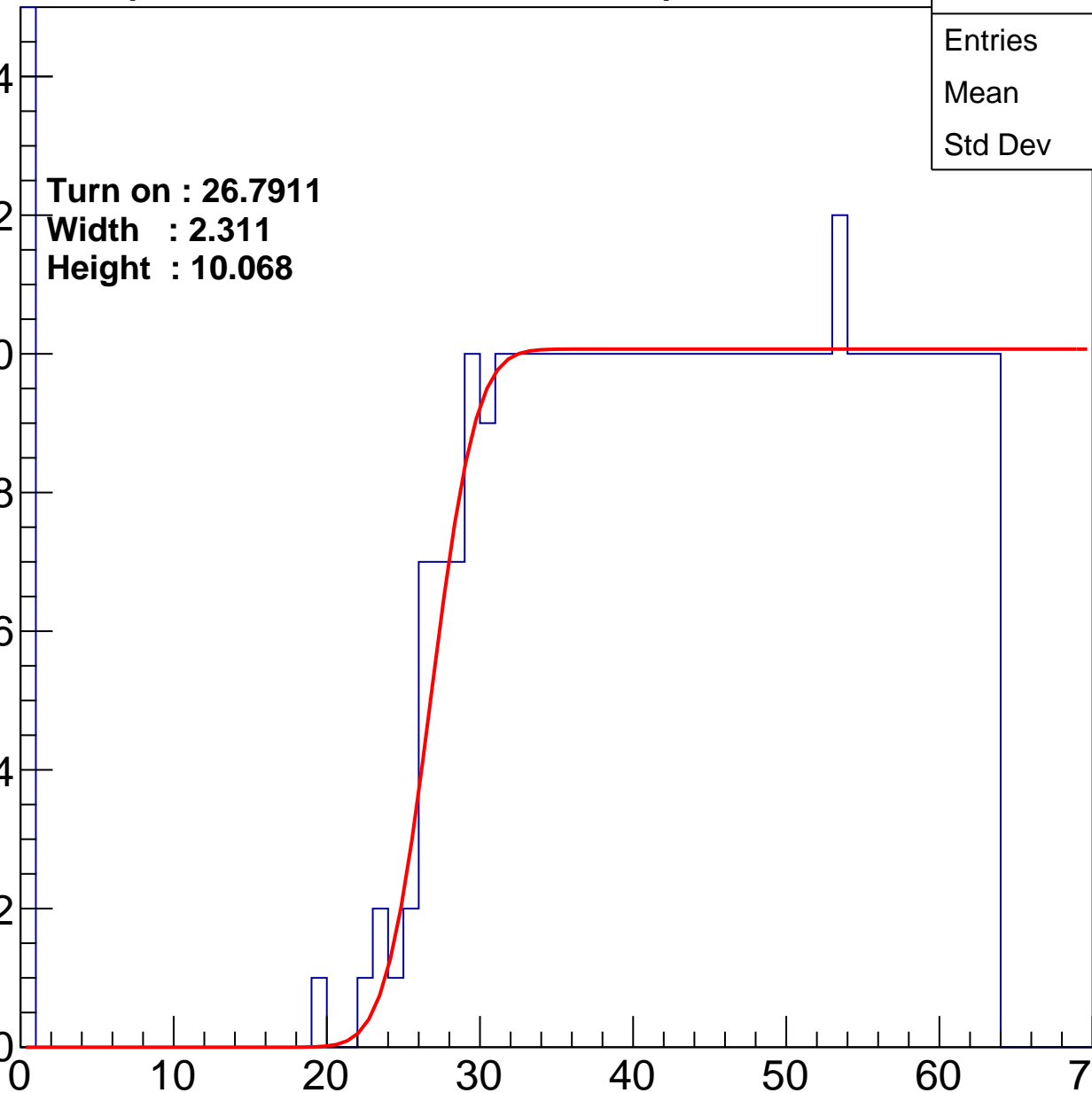
Width : 2.311

Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch41

calib_packv5_041523_1651.root, FC#0, port C2

Entries	406
Mean	40.51
Std Dev	17.14

Turn on : 27.8940

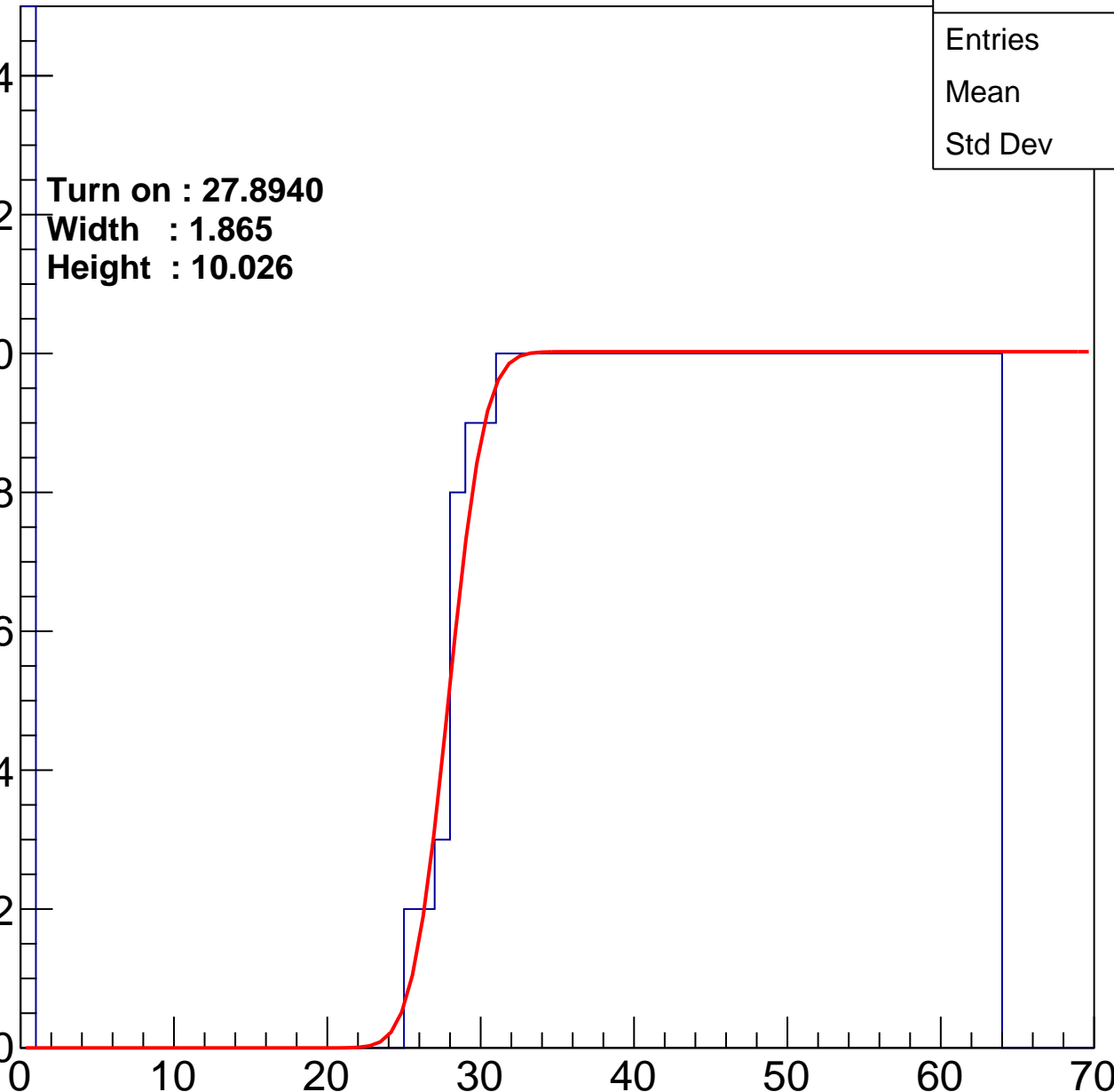
Width : 1.865

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch42

calib_packv5_041523_1651.root, FC#0, port C2

Entries	414
Mean	40.57
Std Dev	16.46

Turn on : 25.7811

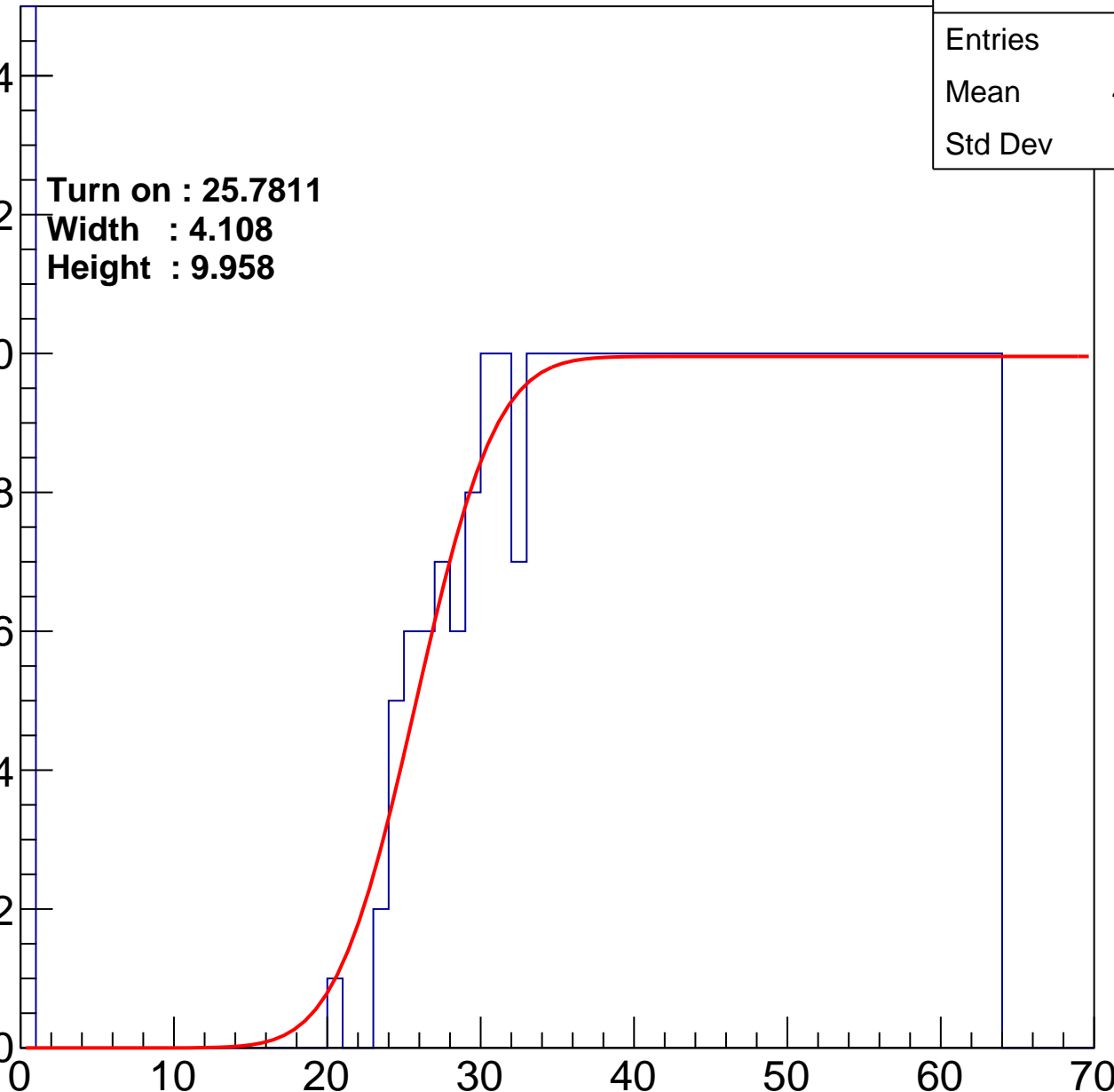
Width : 4.108

Height : 9.958

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch43

calib_packv5_041523_1651.root, FC#0, port C2

Entries	450
Mean	38.3
Std Dev	17.92

Turn on : 24.5061

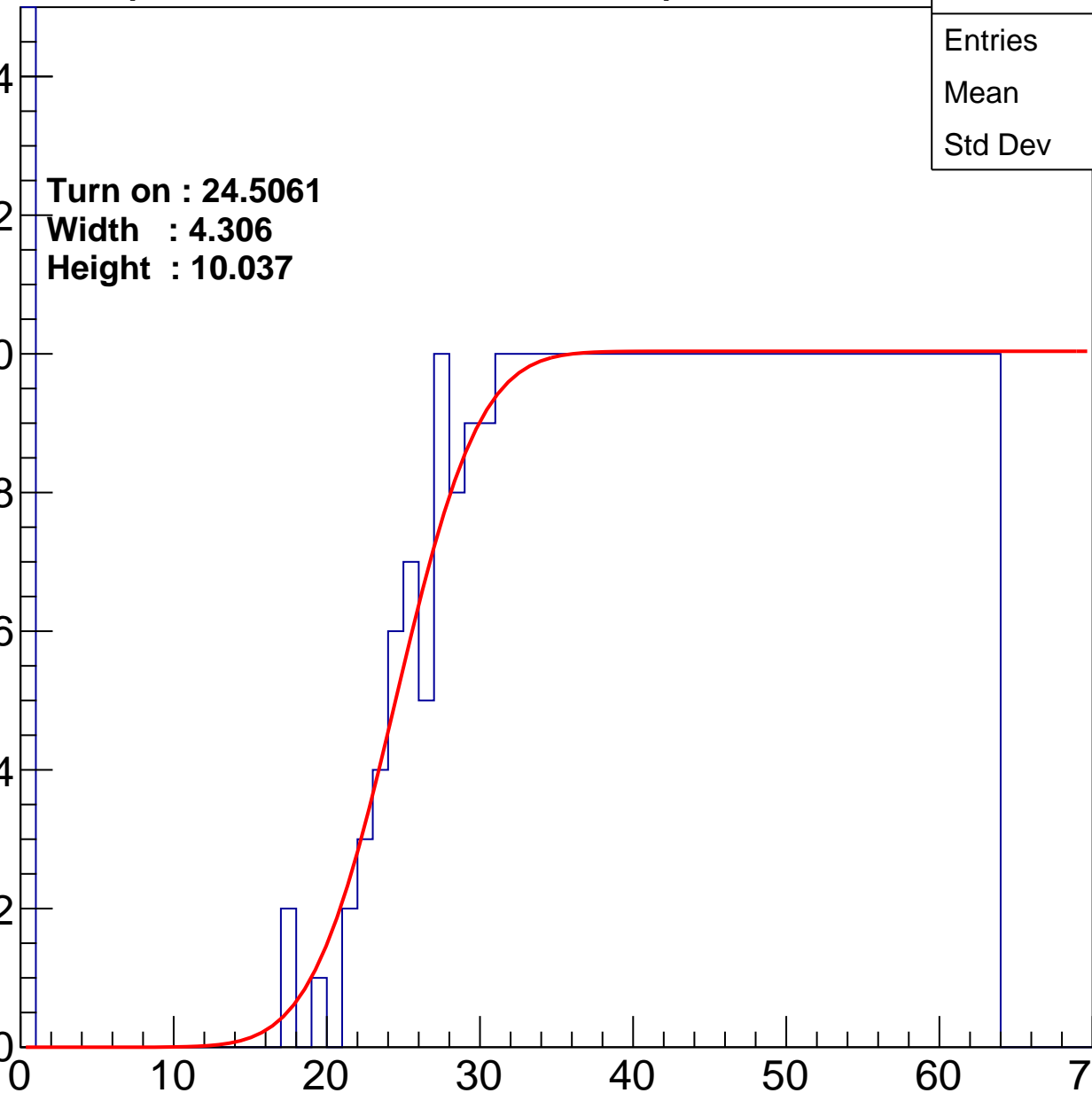
Width : 4.306

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch44

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	39.06
Std Dev	17.9

Turn on : 26.5064

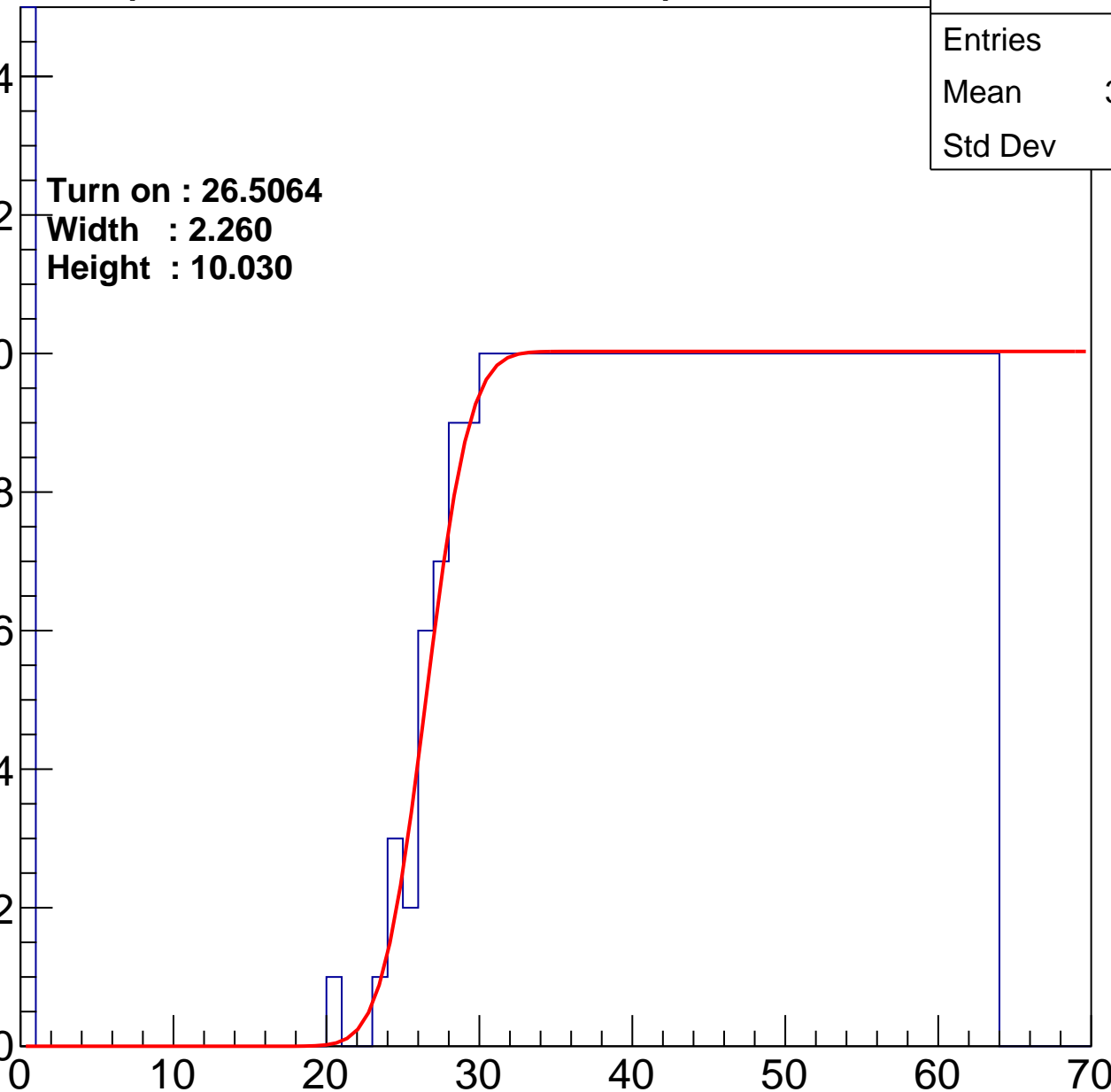
Width : 2.260

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch45

calib_packv5_041523_1651.root, FC#0, port C2

Entries	446
Mean	38.31
Std Dev	18.14

Turn on : 25.5733

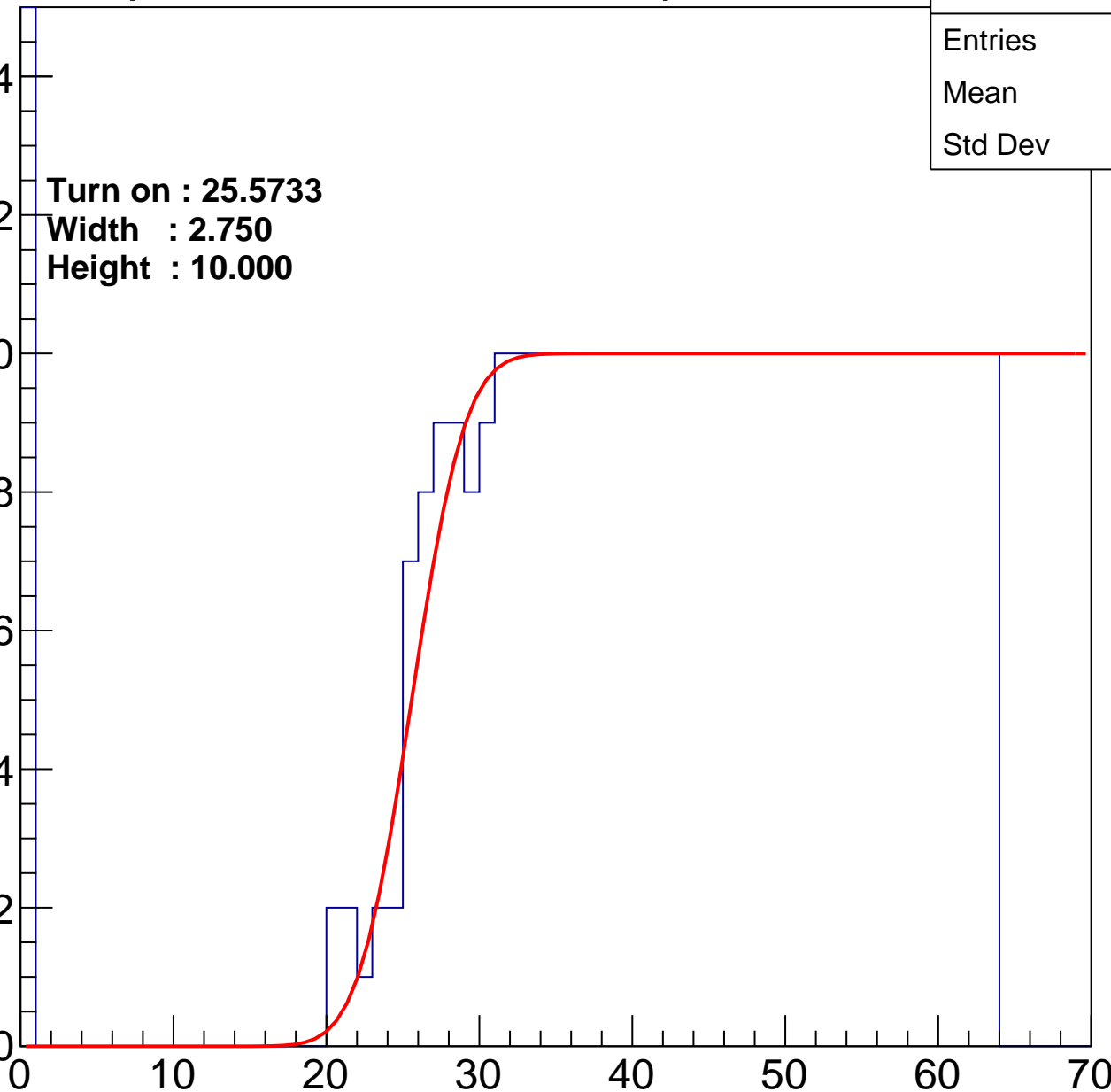
Width : 2.750

Height : 10.000

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch46

calib_packv5_041523_1651.root, FC#0, port C2

Entries	445
Mean	37.78
Std Dev	18.92

Turn on : 25.9944

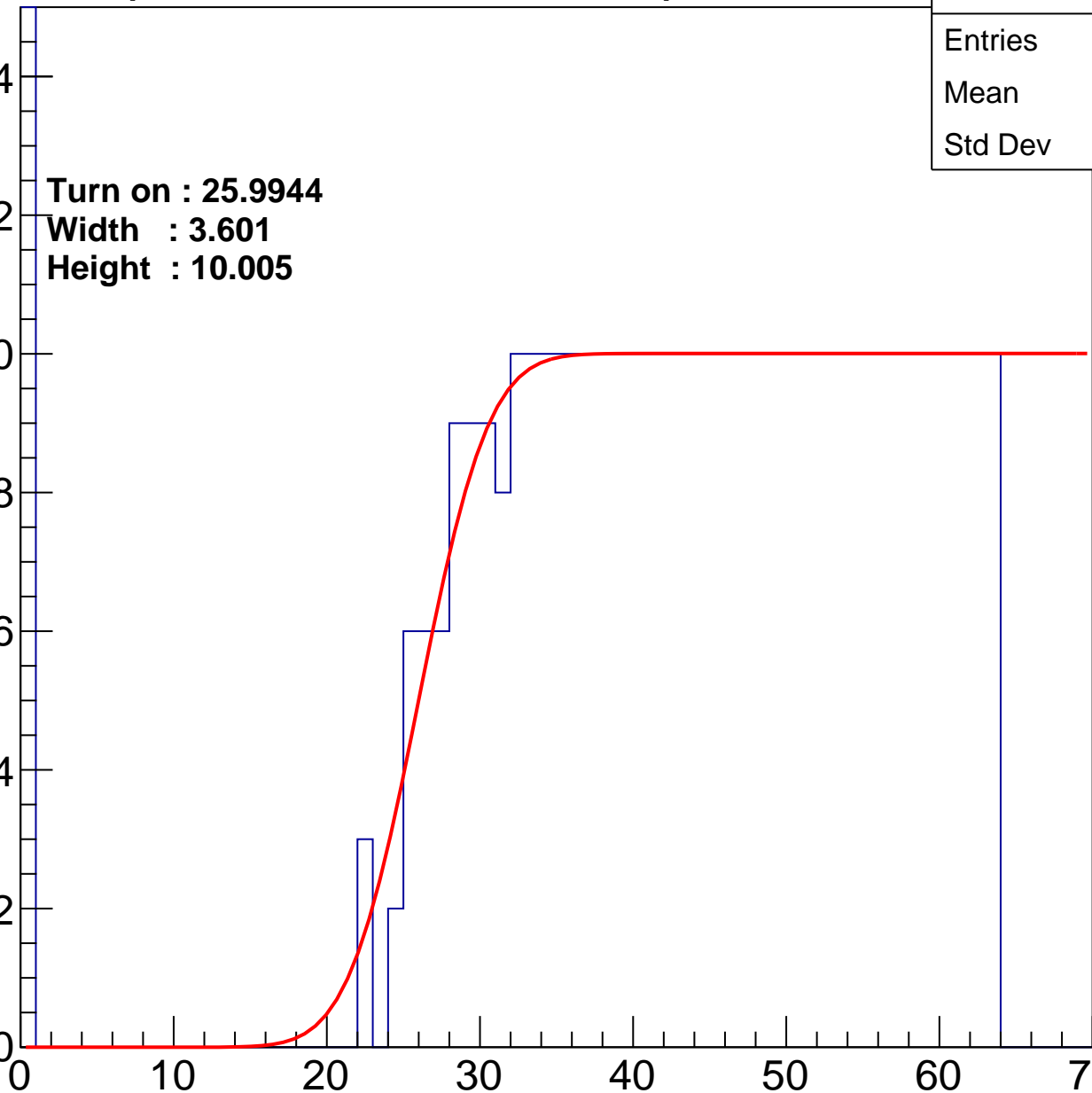
Width : 3.601

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch47

calib_packv5_041523_1651.root, FC#0, port C2

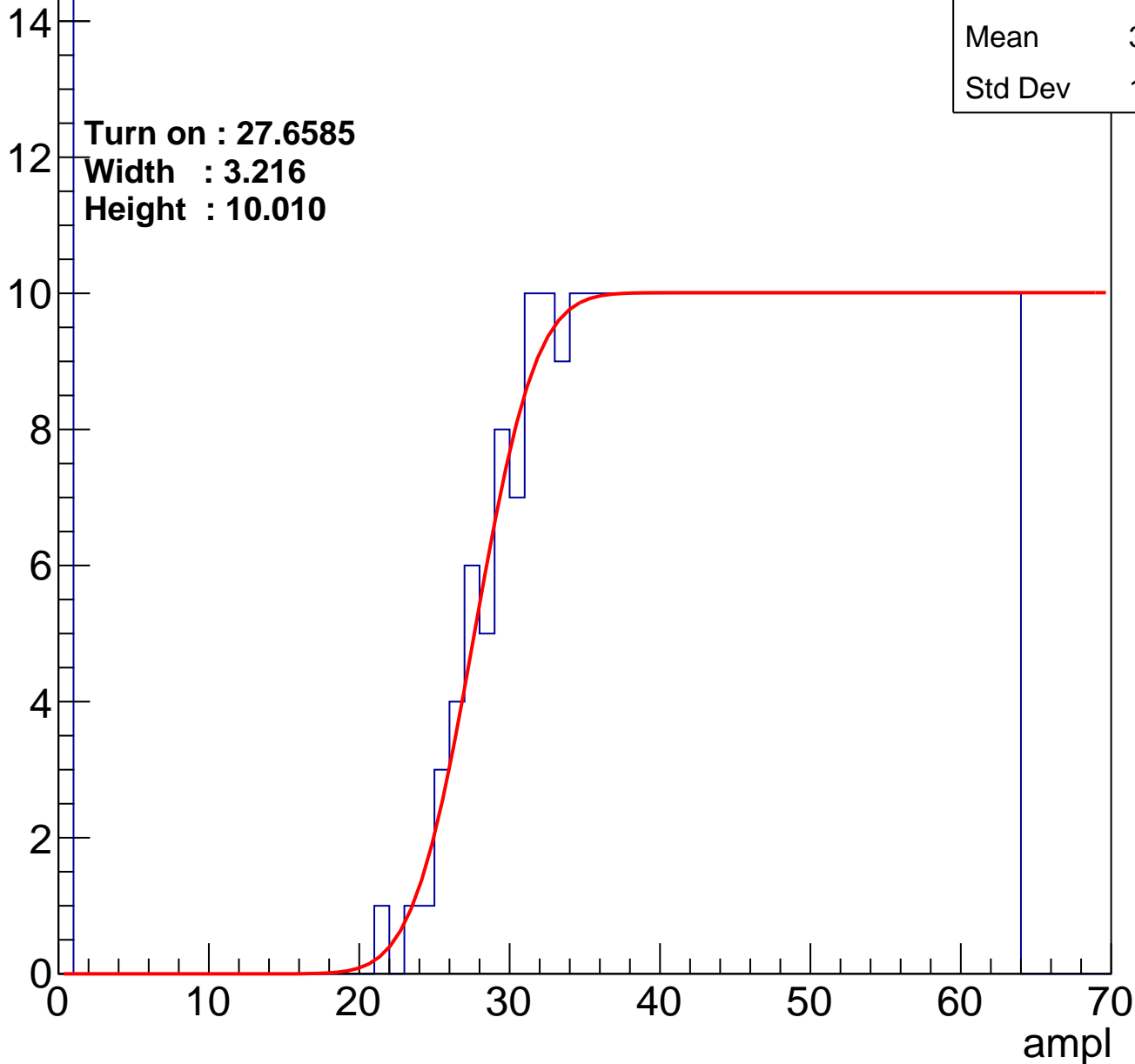
Entry

Entries	415
Mean	39.68
Std Dev	17.82

Turn on : 27.6585

Width : 3.216

Height : 10.010



B1L103S, U3-ch48

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	38.33
Std Dev	18.27

Turn on : 25.8810

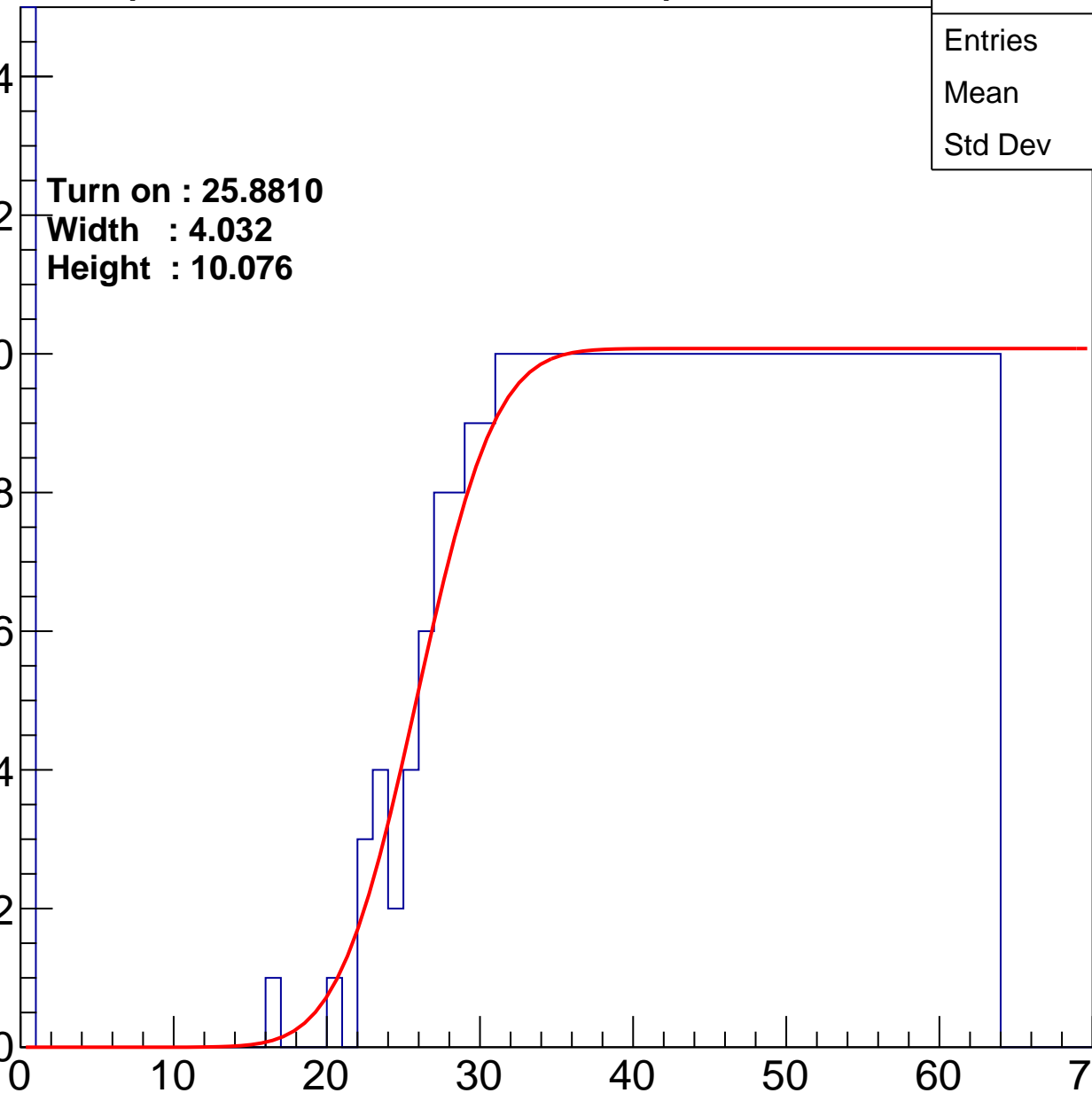
Width : 4.032

Height : 10.076

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch49

calib_packv5_041523_1651.root, FC#0, port C2

Entries	427
Mean	39.43
Std Dev	17.53

Turn on : 26.1902

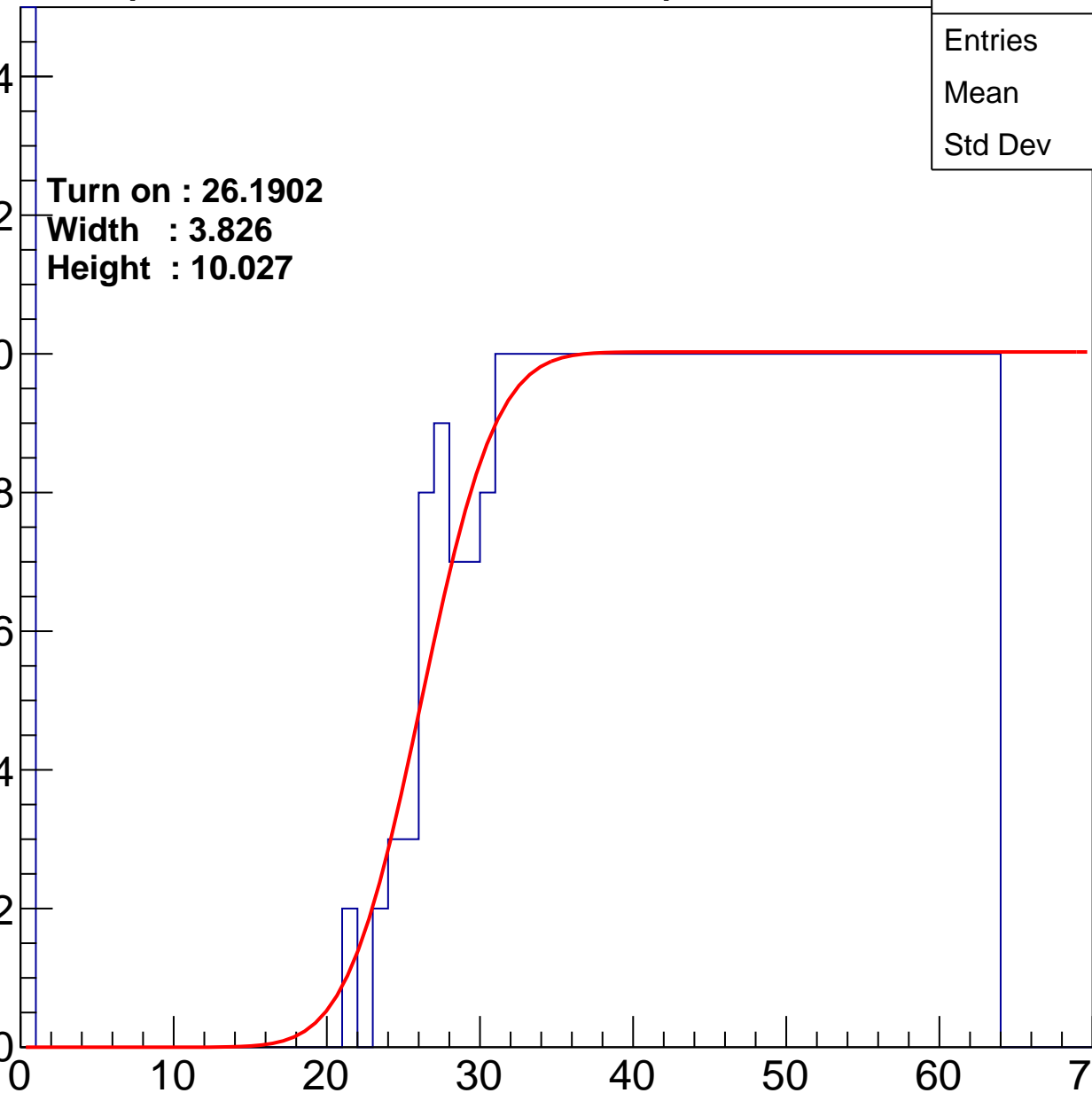
Width : 3.826

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch50

calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	39.48
Std Dev	17.12

Turn on : 25.4217

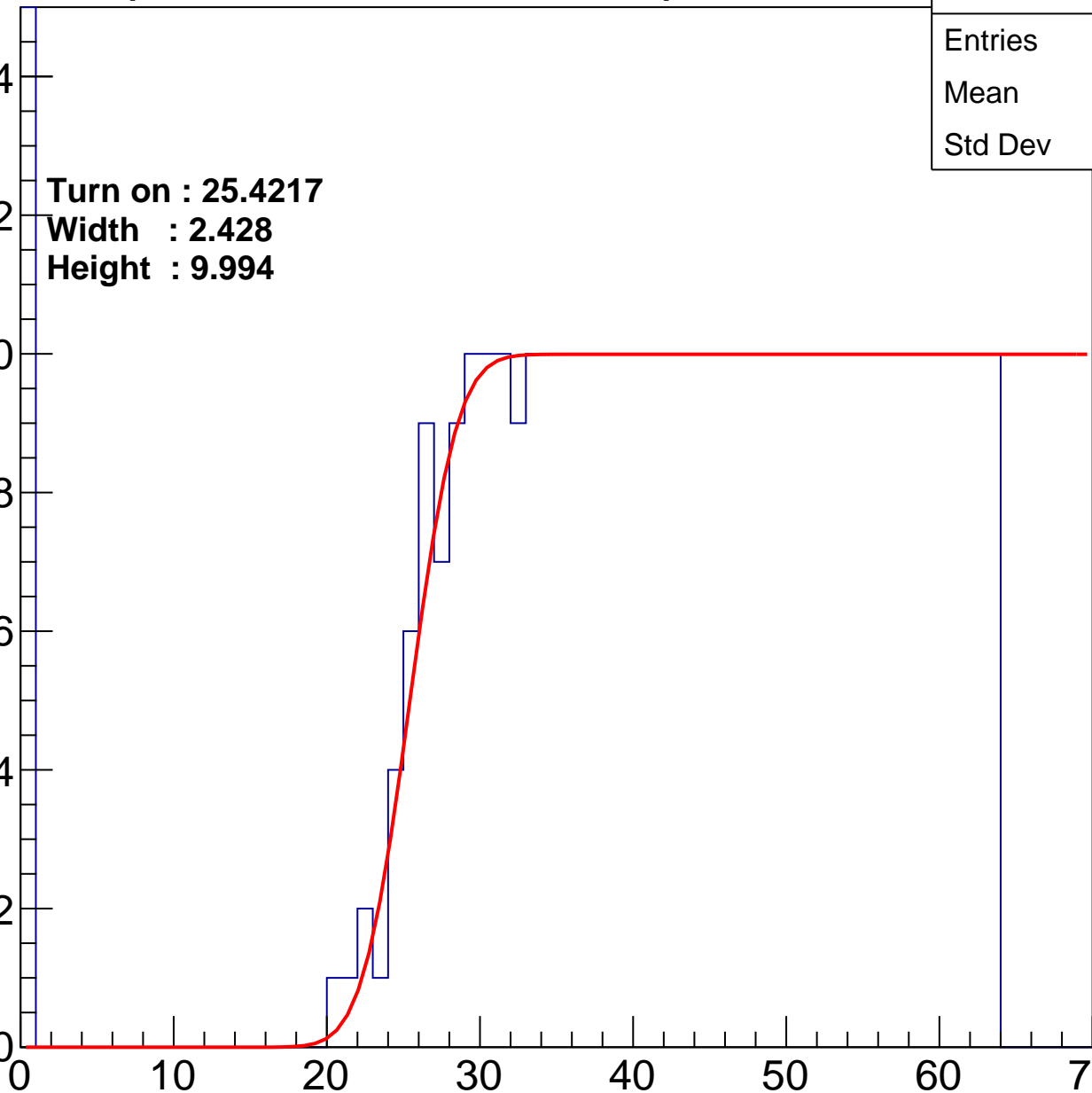
Width : 2.428

Height : 9.994

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch51

calib_packv5_041523_1651.root, FC#0, port C2

Entries	409
Mean	41.12
Std Dev	15.88

Turn on : 26.1688

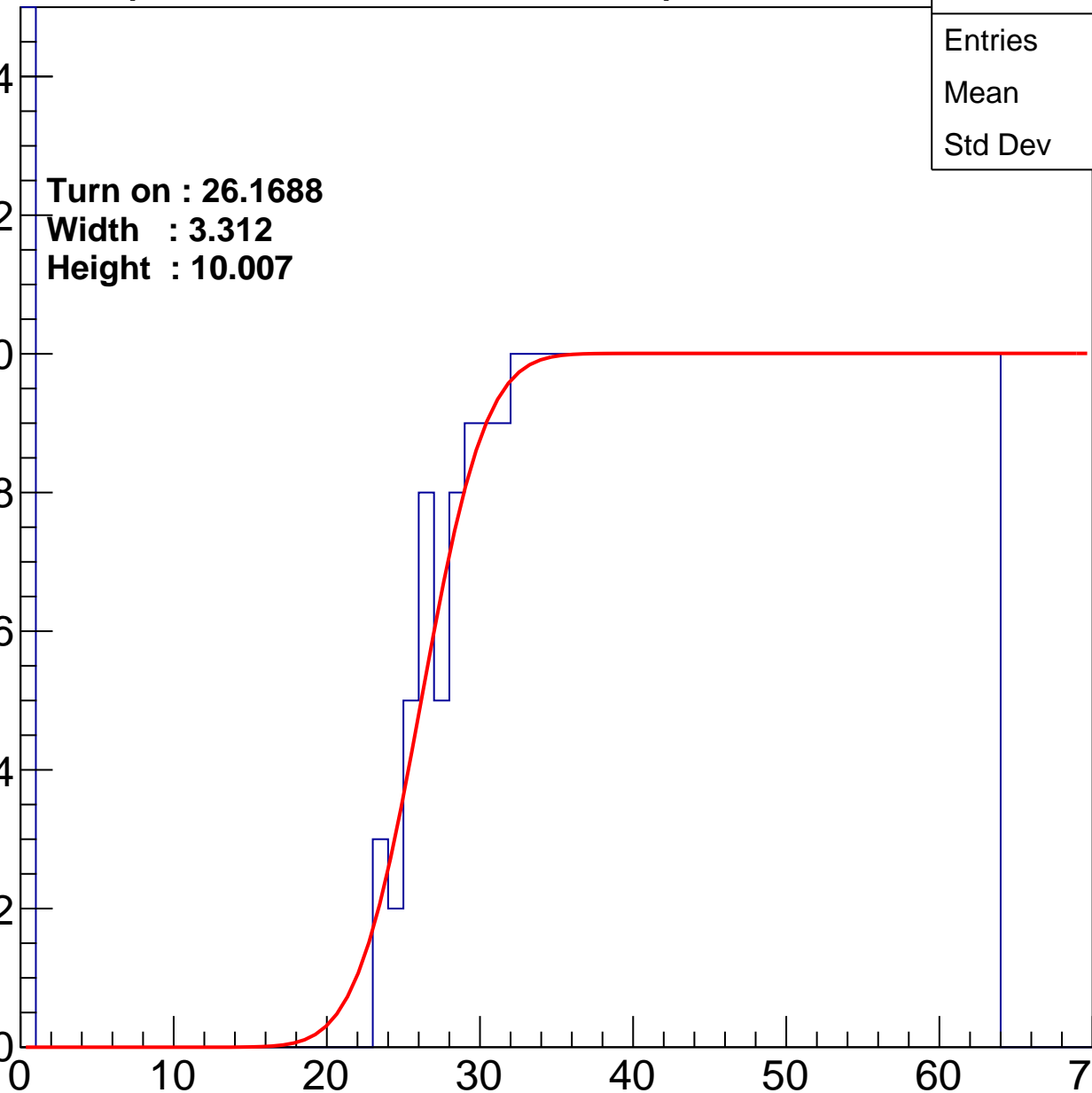
Width : 3.312

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch52

calib_packv5_041523_1651.root, FC#0, port C2

Entries	449
Mean	38.39
Std Dev	17.88

Turn on : 25.0447

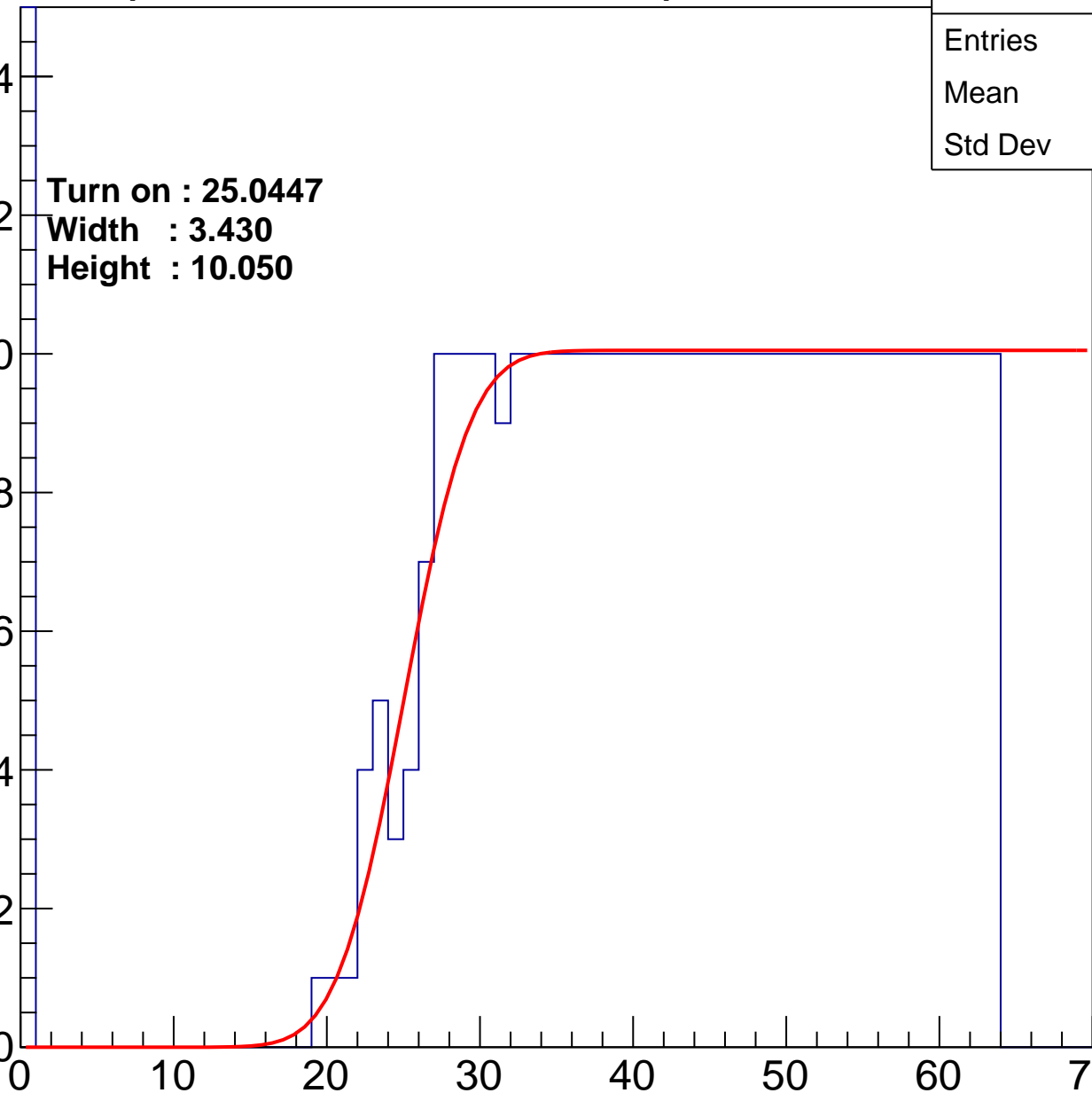
Width : 3.430

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch53

calib_packv5_041523_1651.root, FC#0, port C2

Entries	449
Mean	37.4
Std Dev	19.23

Turn on : 26.5104

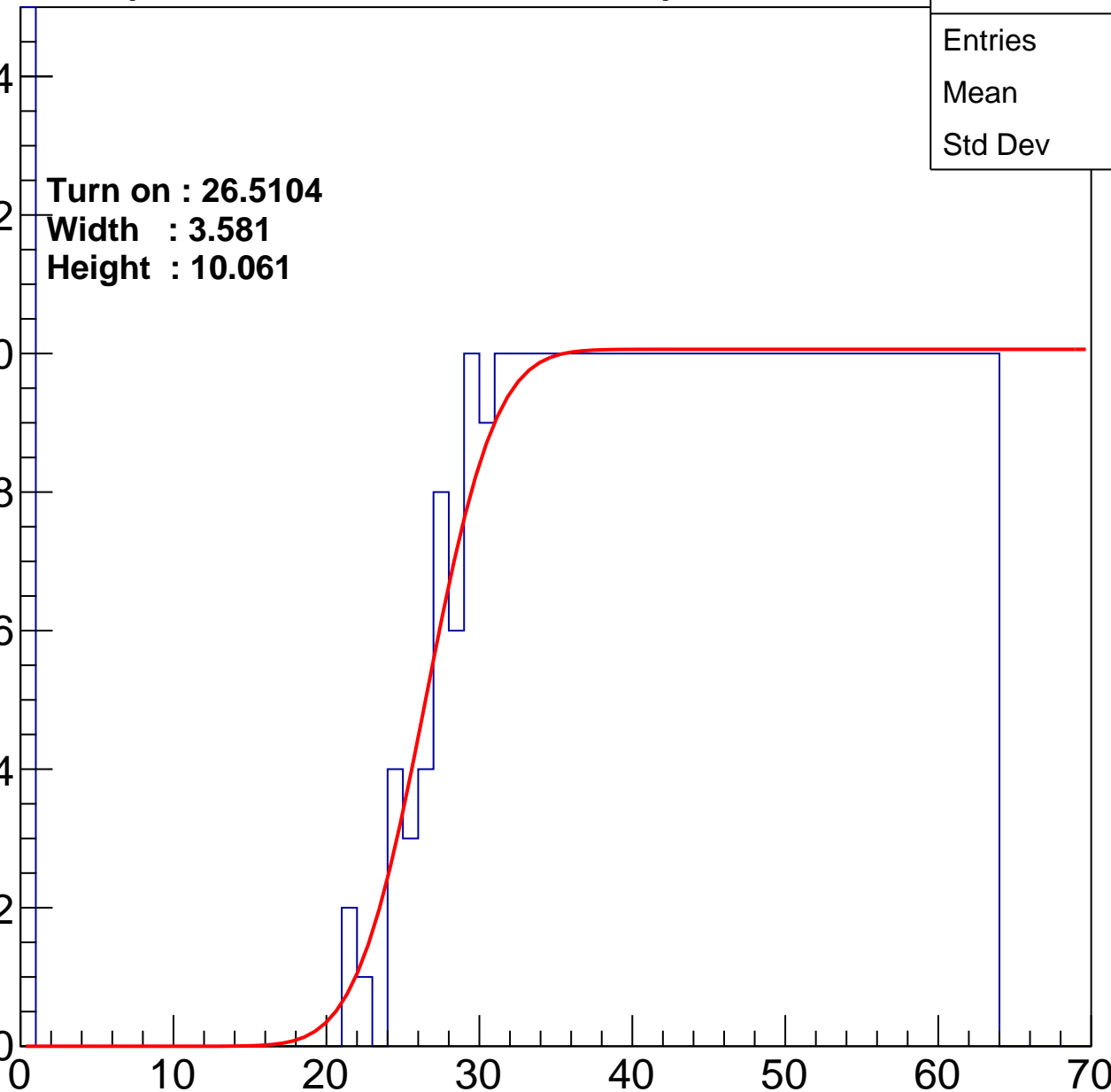
Width : 3.581

Height : 10.061

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch54

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	38.27
Std Dev	18.51

Turn on : 26.6007

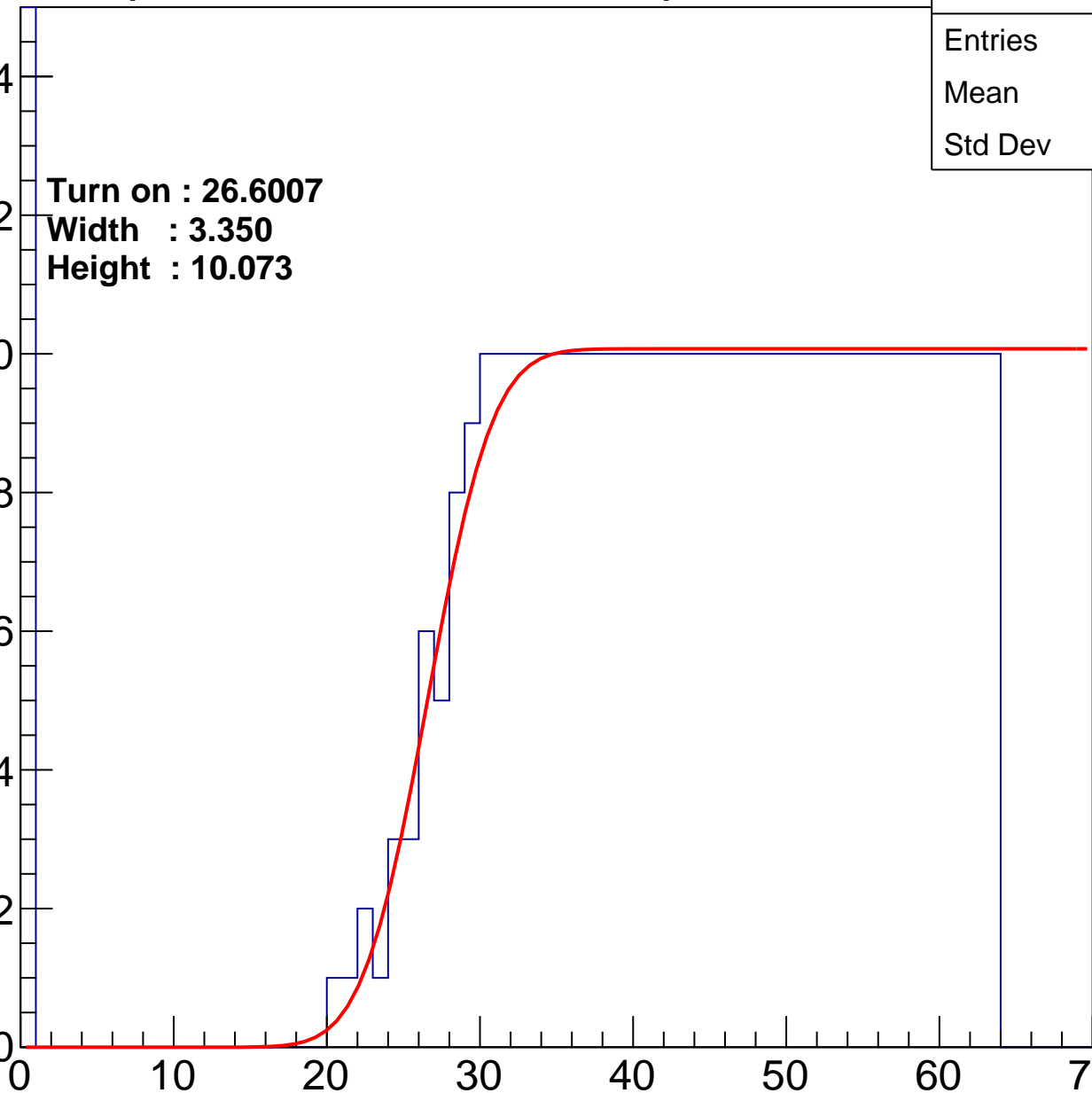
Width : 3.350

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch55

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	38.92
Std Dev	18.01

Turn on : 26.5576

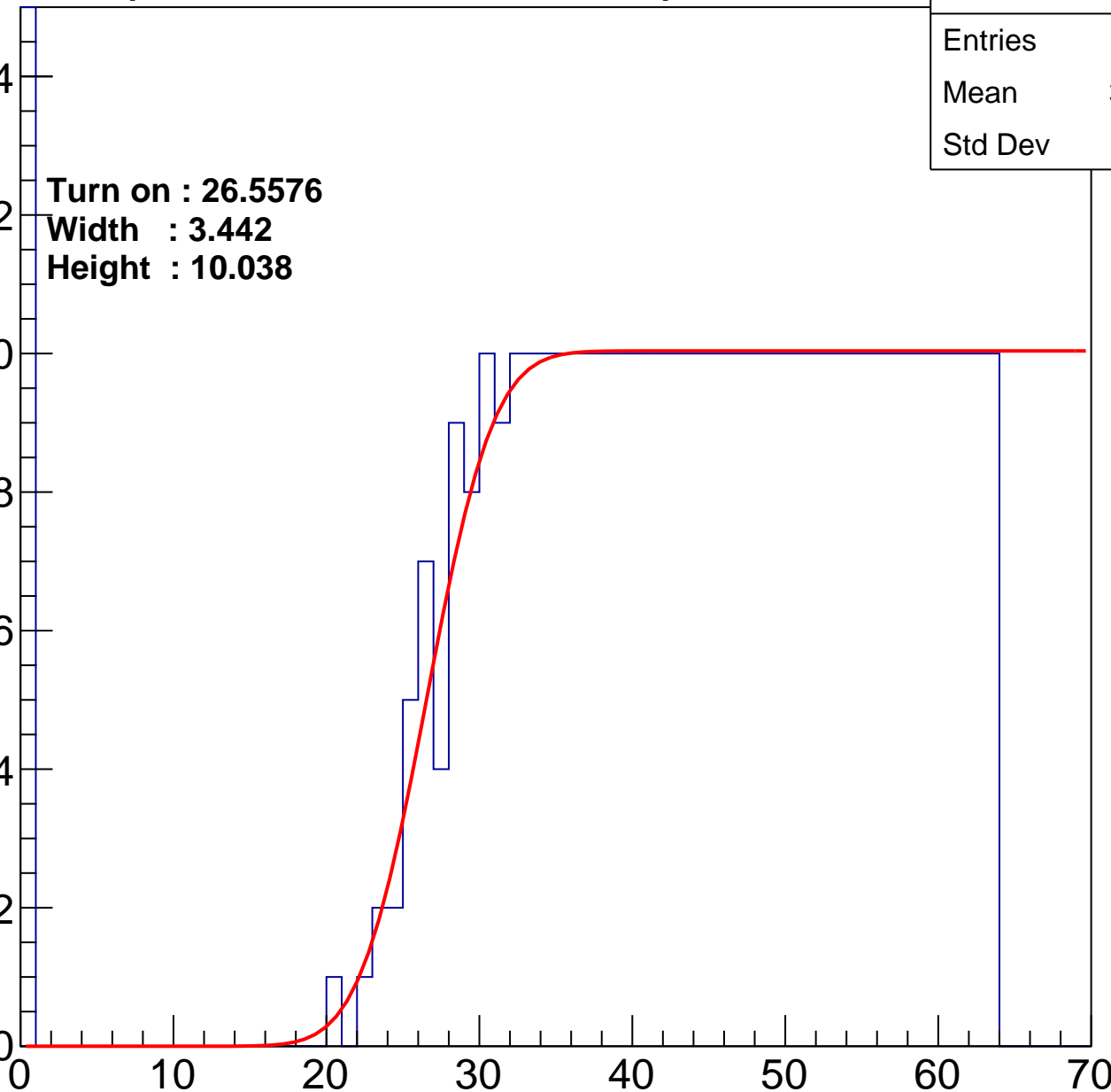
Width : 3.442

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch56

calib_packv5_041523_1651.root, FC#0, port C2

Entries	452
Mean	38.36
Std Dev	17.77

Turn on : 24.5808

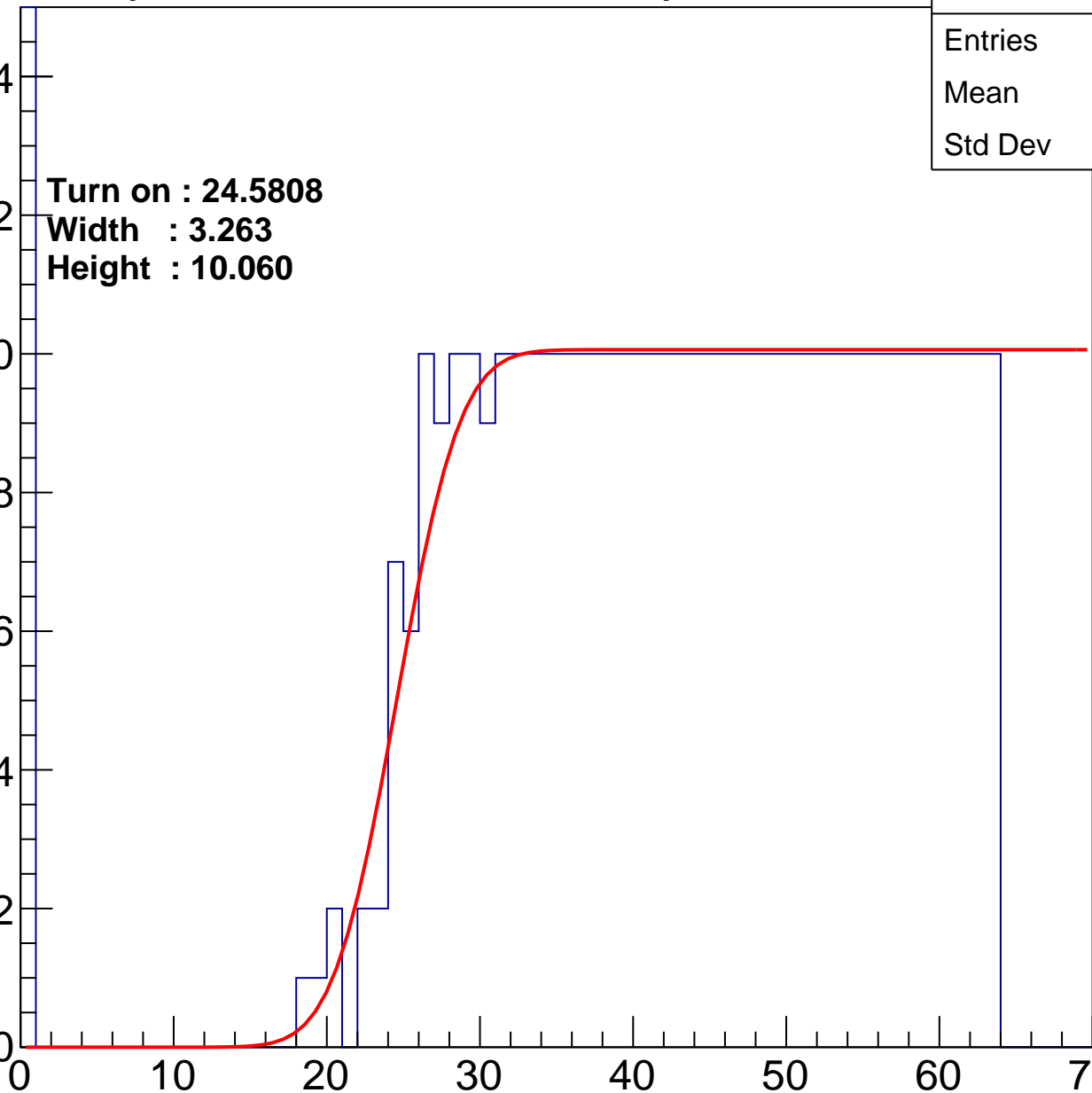
Width : 3.263

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch57

calib_packv5_041523_1651.root, FC#0, port C2

Entries	441
Mean	38.57
Std Dev	18.03

Turn on : 25.5785

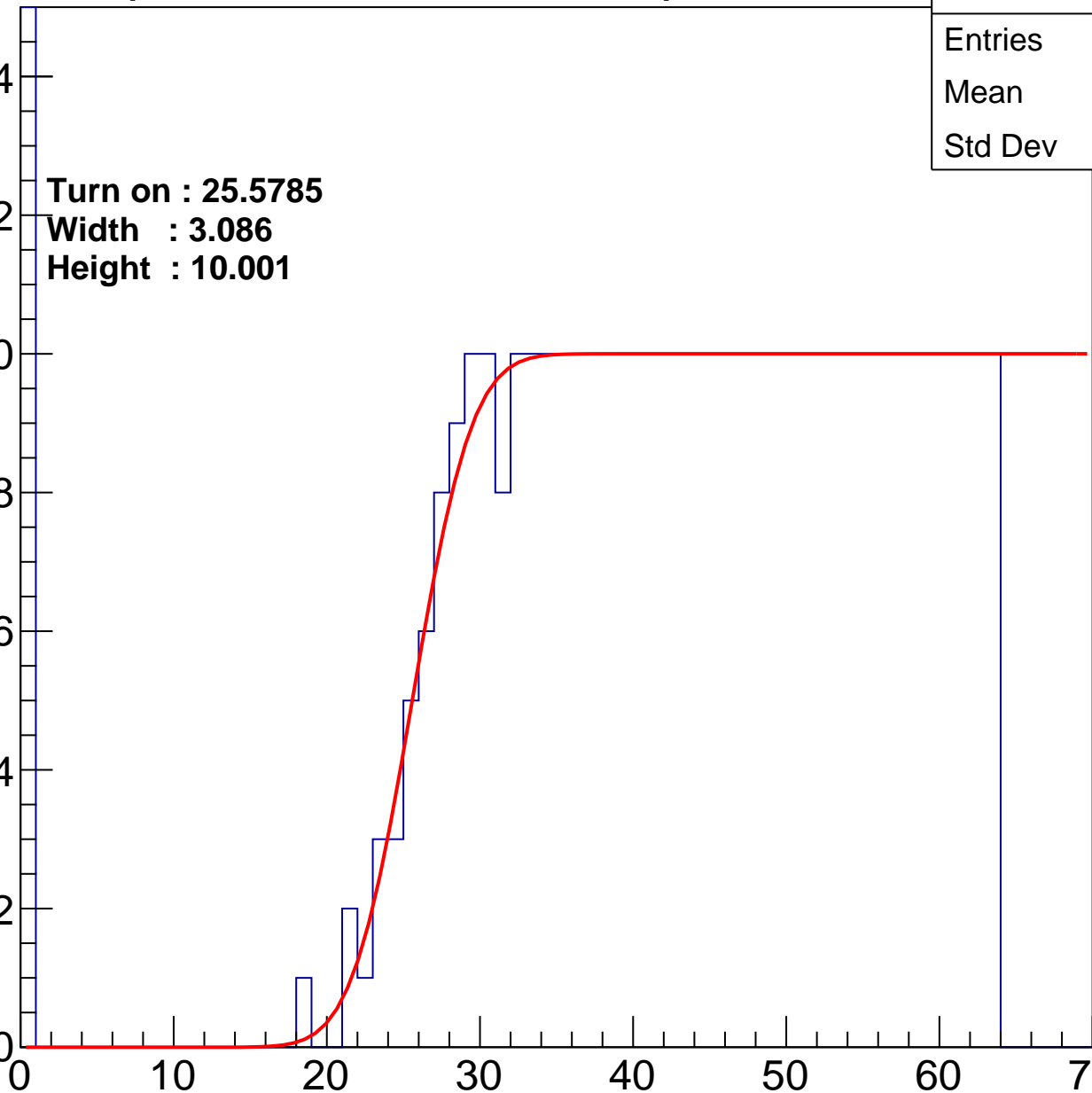
Width : 3.086

Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch58

calib_packv5_041523_1651.root, FC#0, port C2

Entries	444
Mean	39.17
Std Dev	16.98

Turn on : 23.9142

Width : 3.463

Height : 10.018

Entry

14

12

10

8

6

4

2

0

0

10

20

30

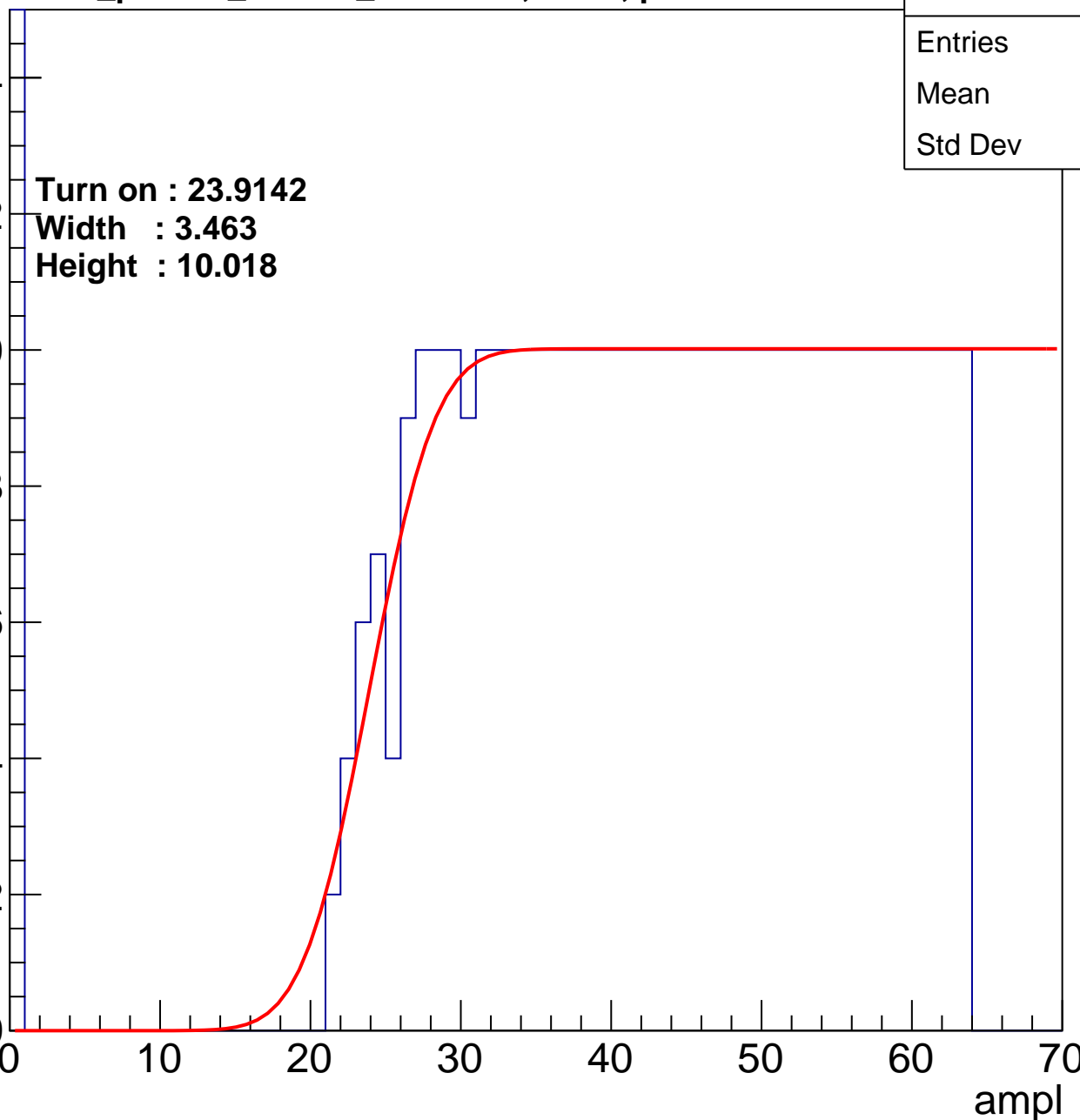
40

50

60

70

ampl



B1L103S, U3-ch59

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.23
Std Dev	17.78

Turn on : 26.3711

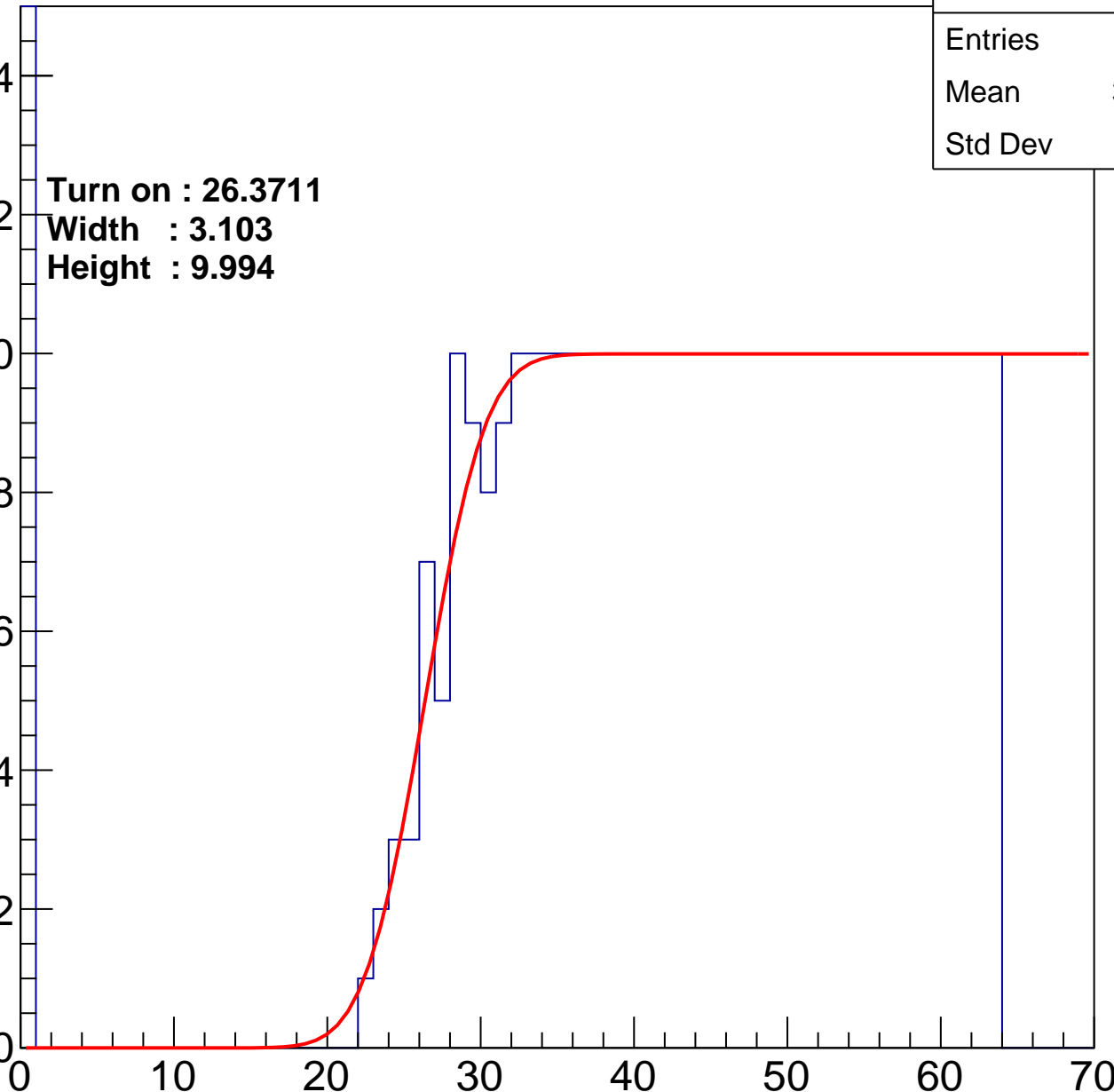
Width : 3.103

Height : 9.994

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch60

calib_packv5_041523_1651.root, FC#0, port C2

Entries	447
Mean	38.85
Std Dev	17.31

Turn on : 23.2915

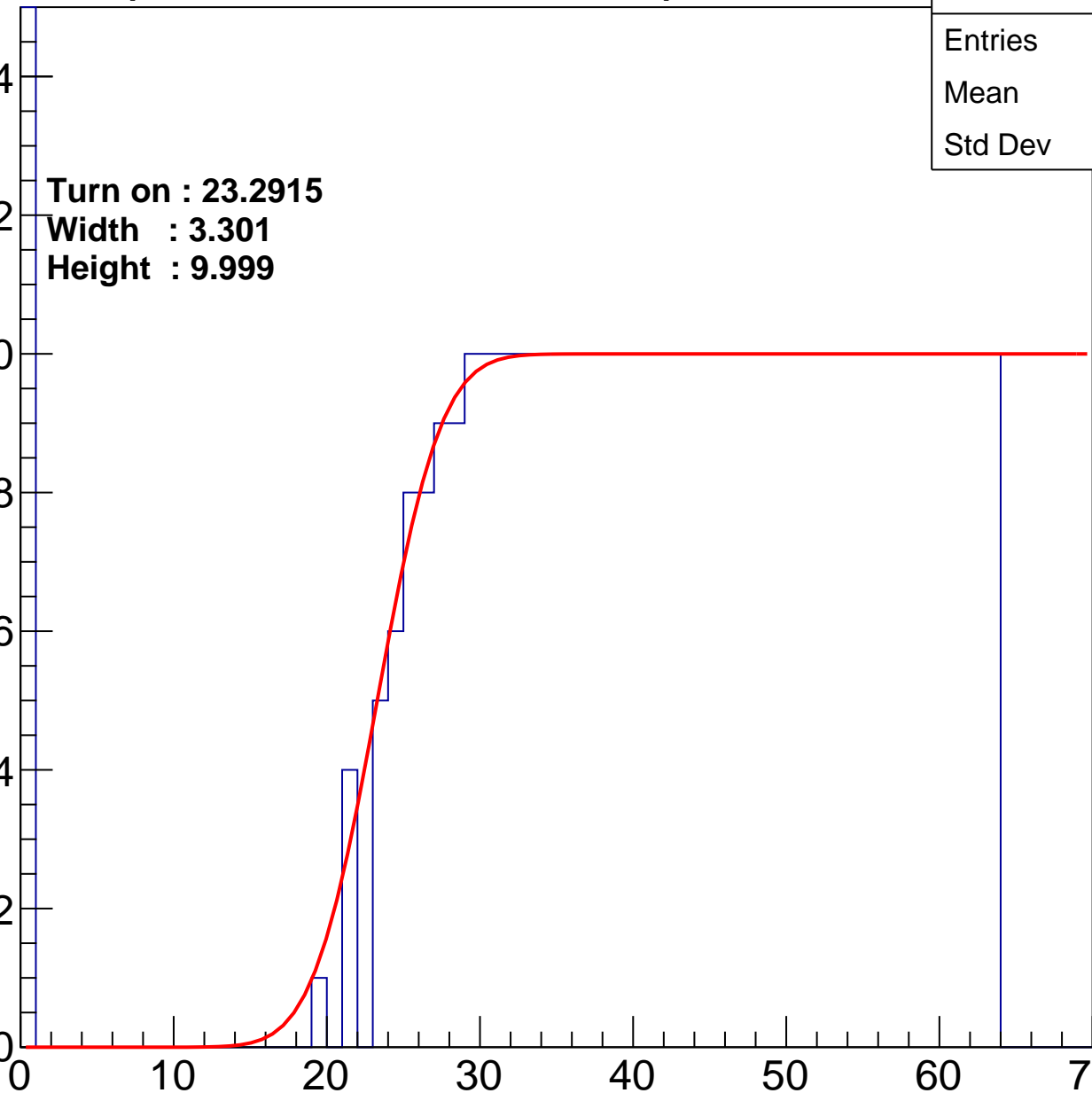
Width : 3.301

Height : 9.999

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch61

calib_packv5_041523_1651.root, FC#0, port C2

Entries	468
Mean	36.13
Std Dev	19.93

Turn on : 26.0379

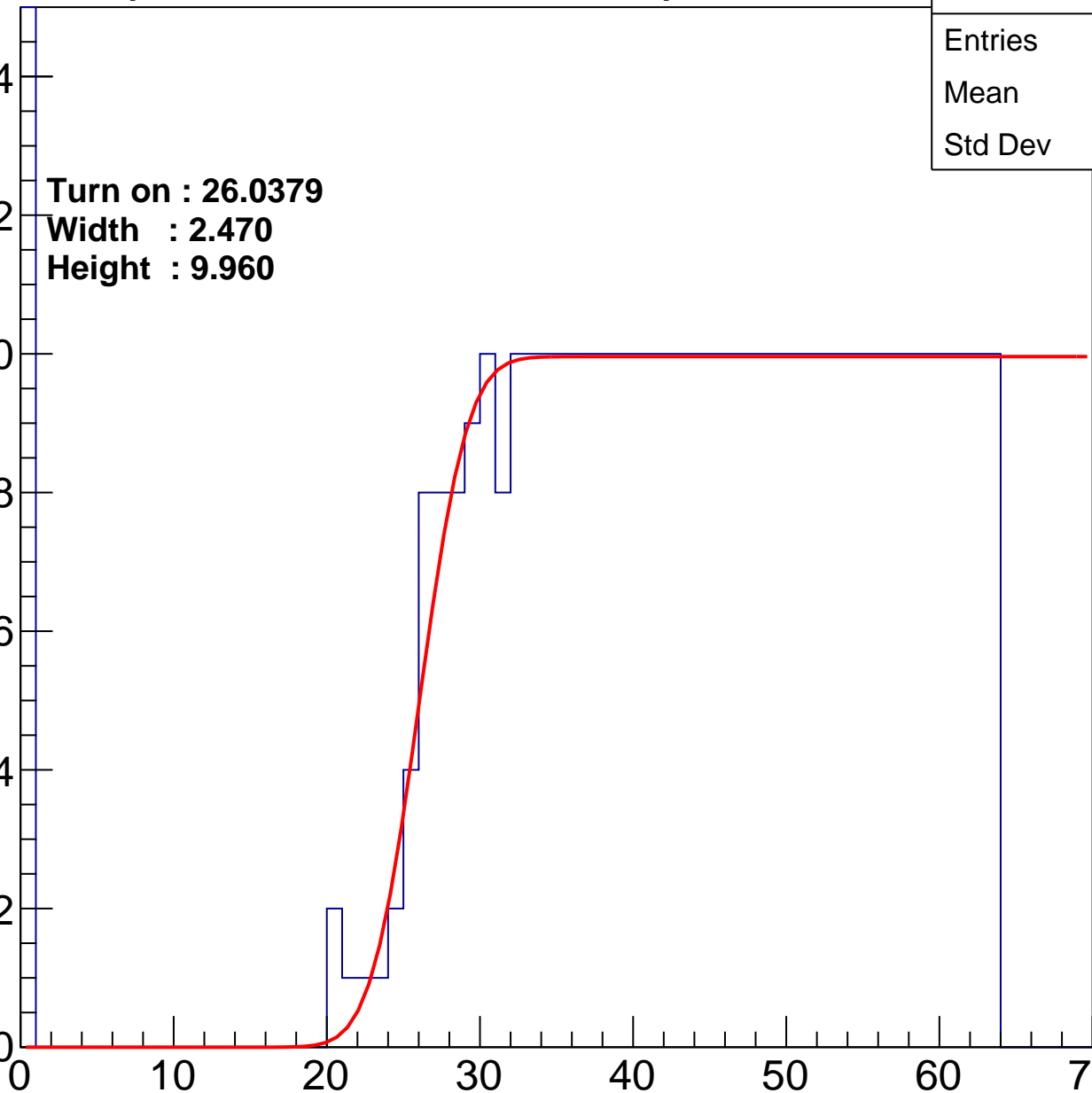
Width : 2.470

Height : 9.960

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch62

calib_packv5_041523_1651.root, FC#0, port C2

Entries	474
Mean	37.11
Std Dev	18.43

Turn on : 23.5602

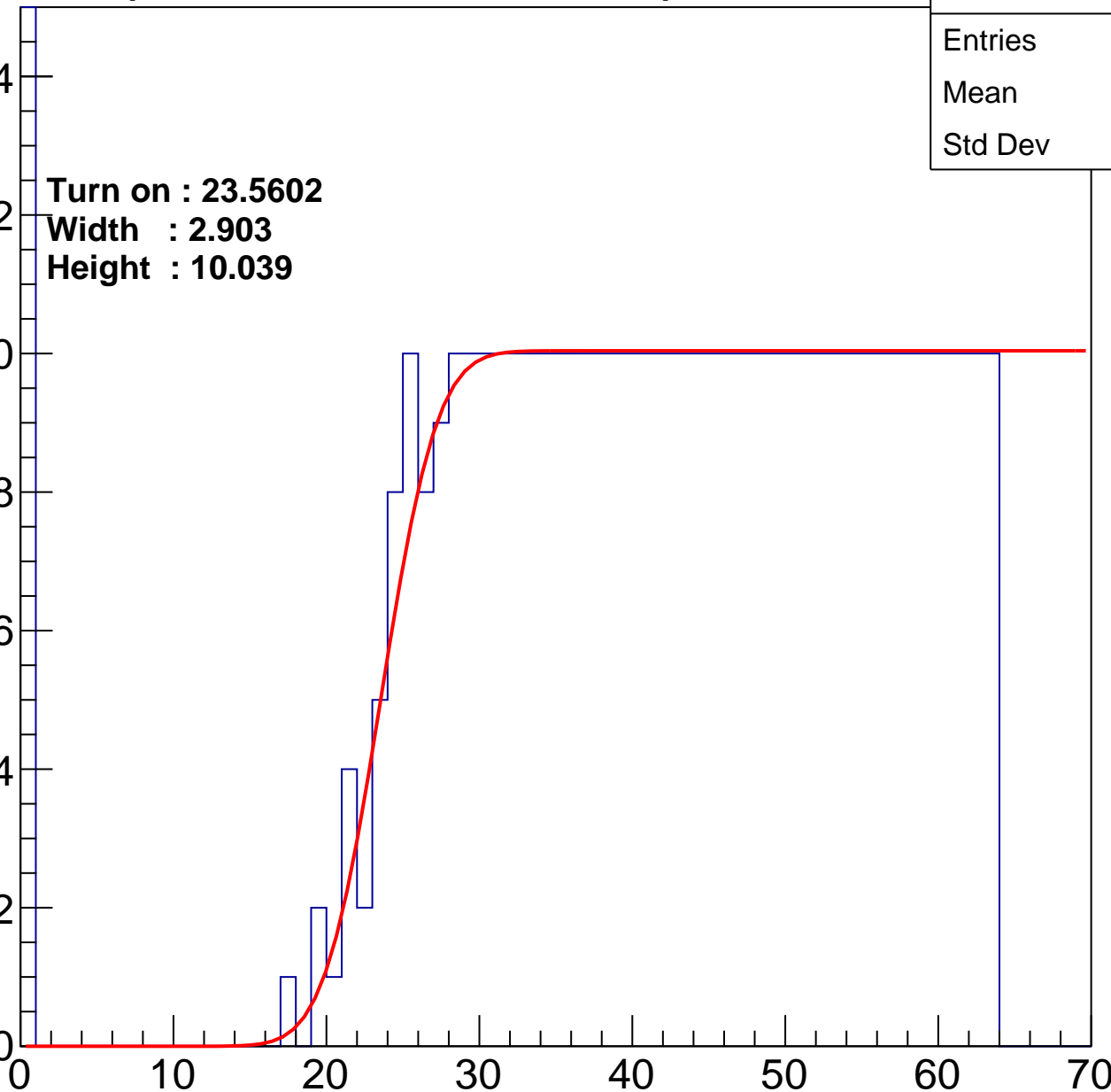
Width : 2.903

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch63

calib_packv5_041523_1651.root, FC#0, port C2

Entries	451
Mean	38.48
Std Dev	17.63

Turn on : 23.8905

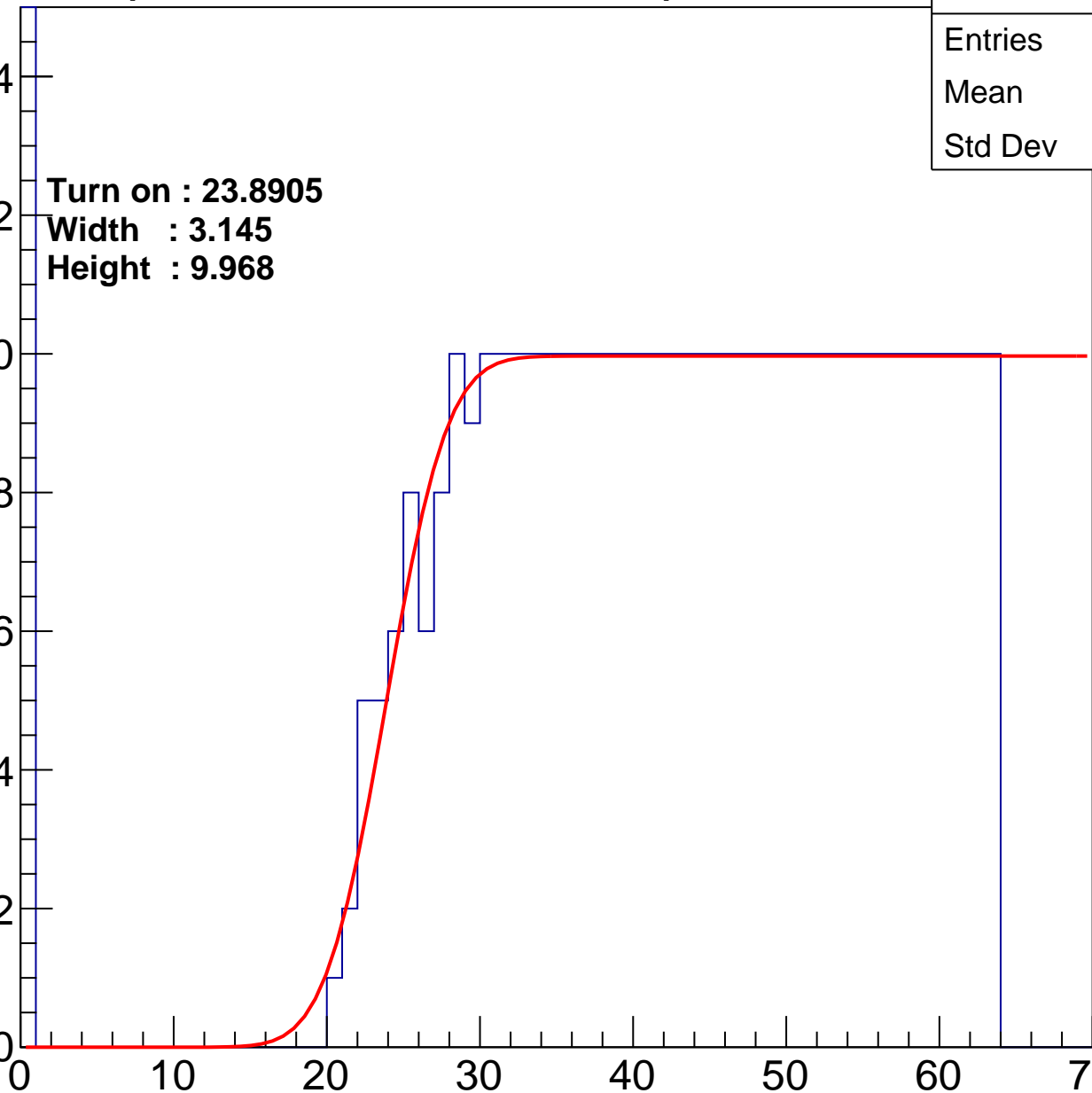
Width : 3.145

Height : 9.968

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch64

calib_packv5_041523_1651.root, FC#0, port C2

Entries	449
Mean	38.4
Std Dev	17.87

Turn on : 24.6174

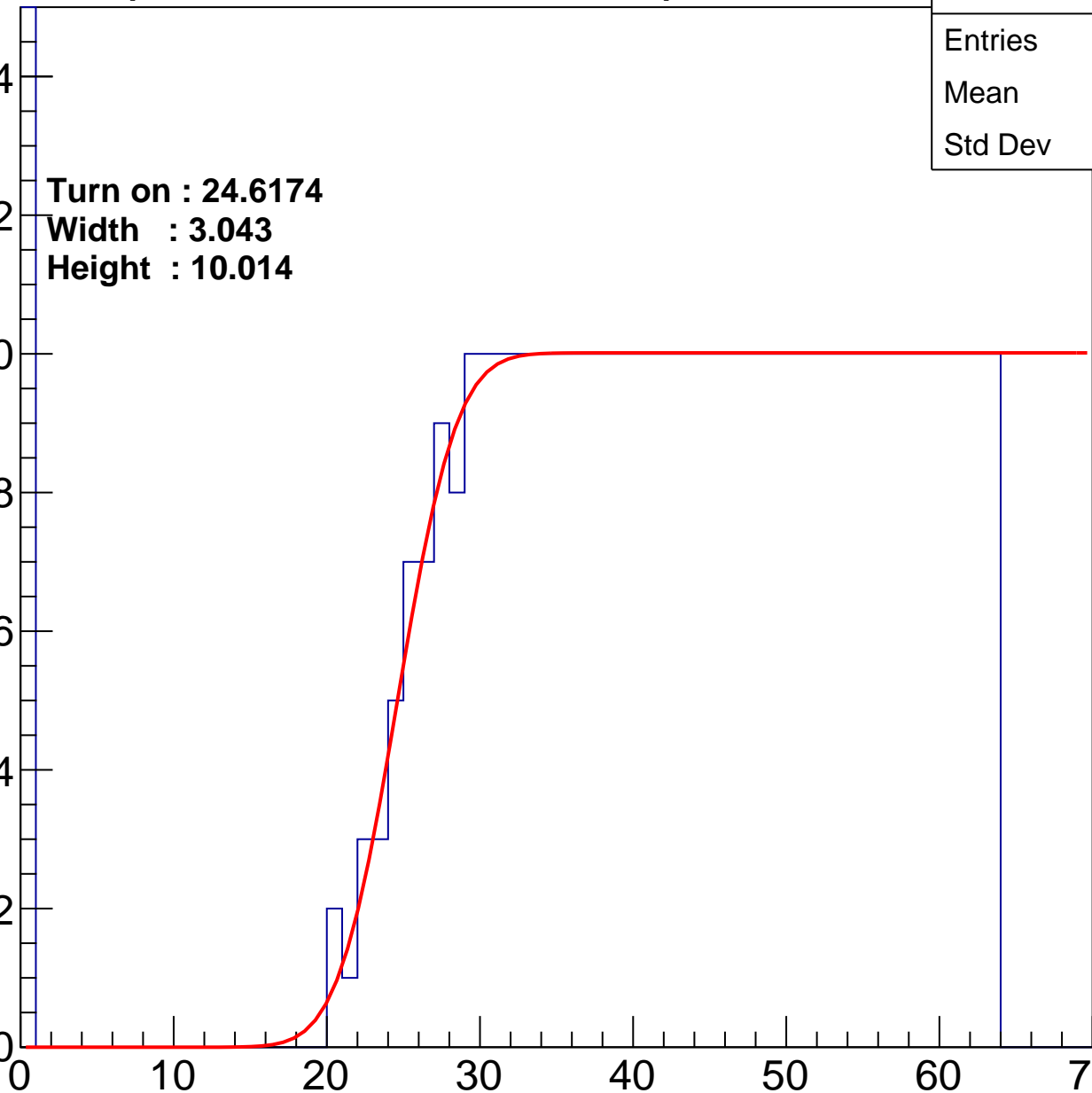
Width : 3.043

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch65

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	37.7
Std Dev	19.12

Turn on : 27.1160

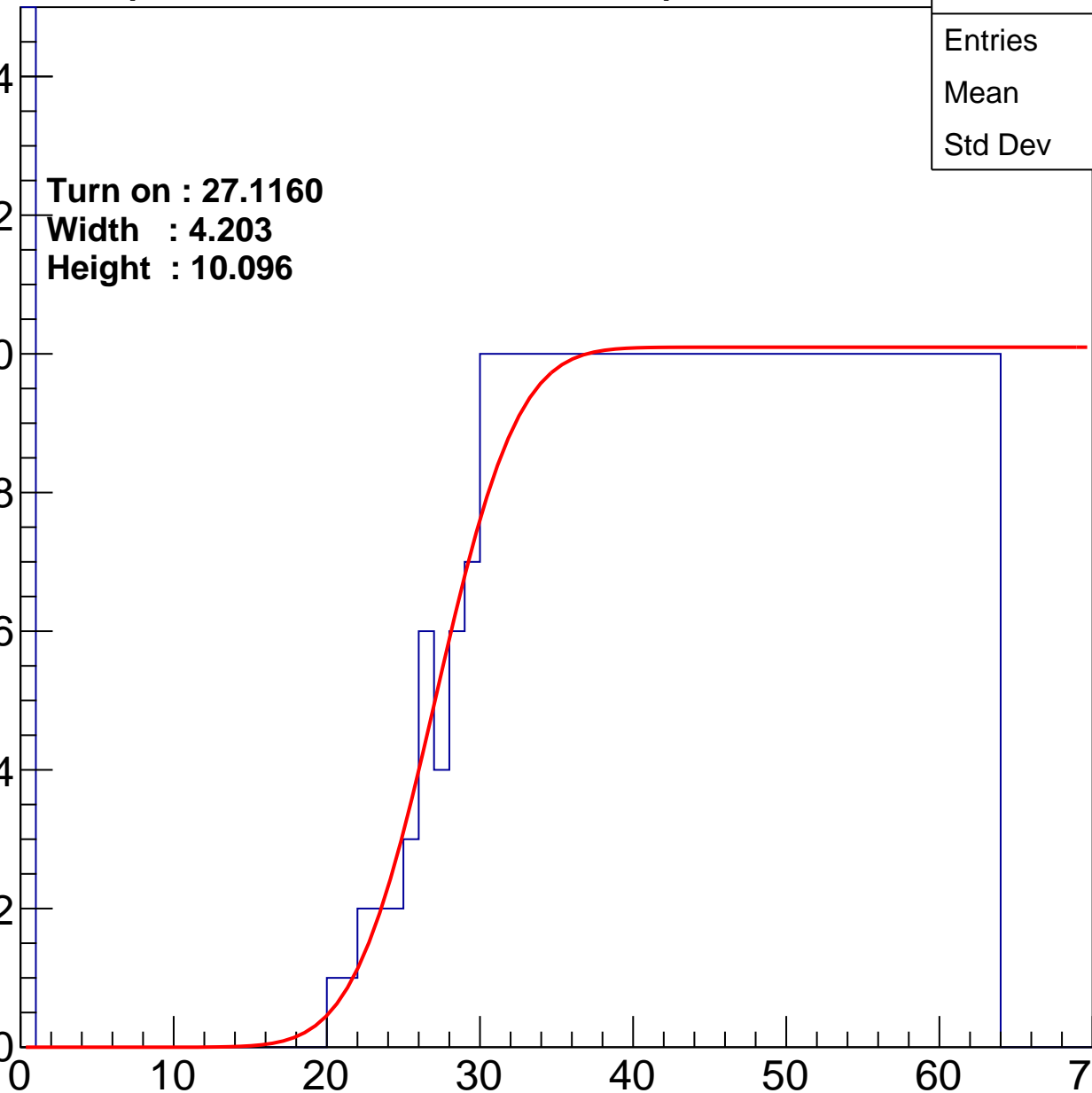
Width : 4.203

Height : 10.096

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch66

calib_packv5_041523_1651.root, FC#0, port C2

Entries	444
Mean	38.49
Std Dev	17.99

Turn on : 24.7349

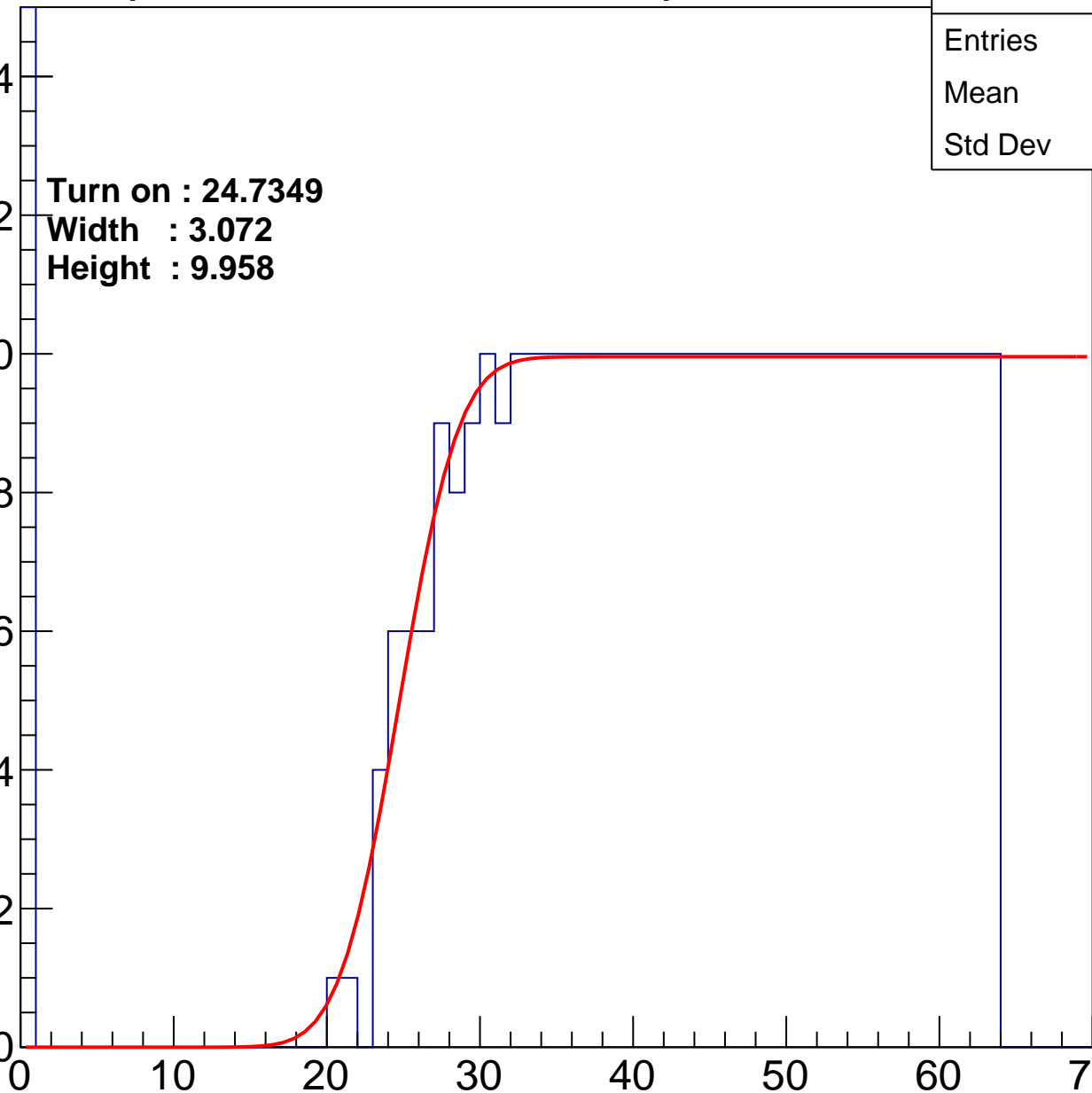
Width : 3.072

Height : 9.958

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch67

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	39.87
Std Dev	17.05

Turn on : 25.7617

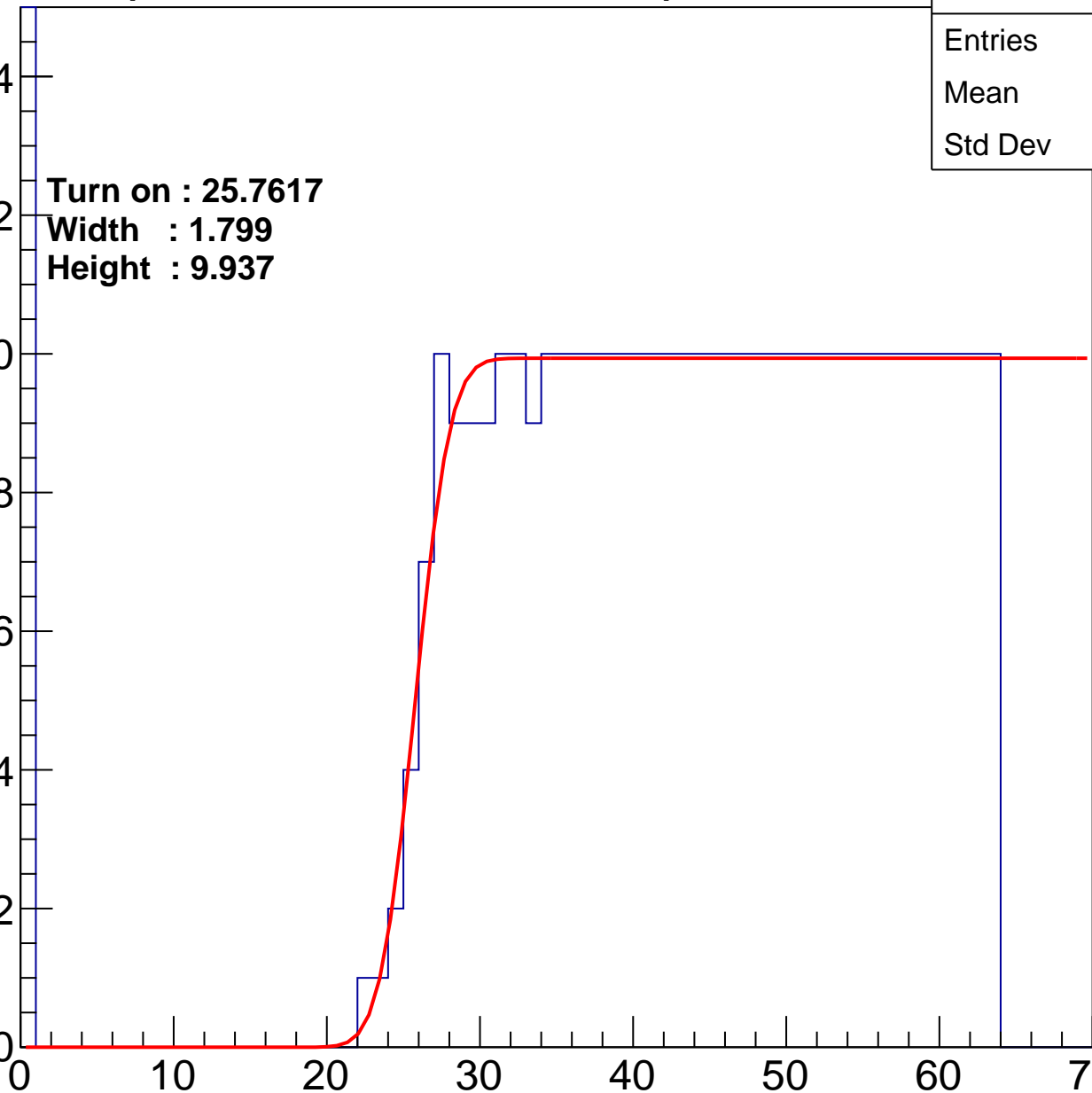
Width : 1.799

Height : 9.937

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch68

calib_packv5_041523_1651.root, FC#0, port C2

Entries	465
Mean	37.51
Std Dev	18.3

Turn on : 23.5419

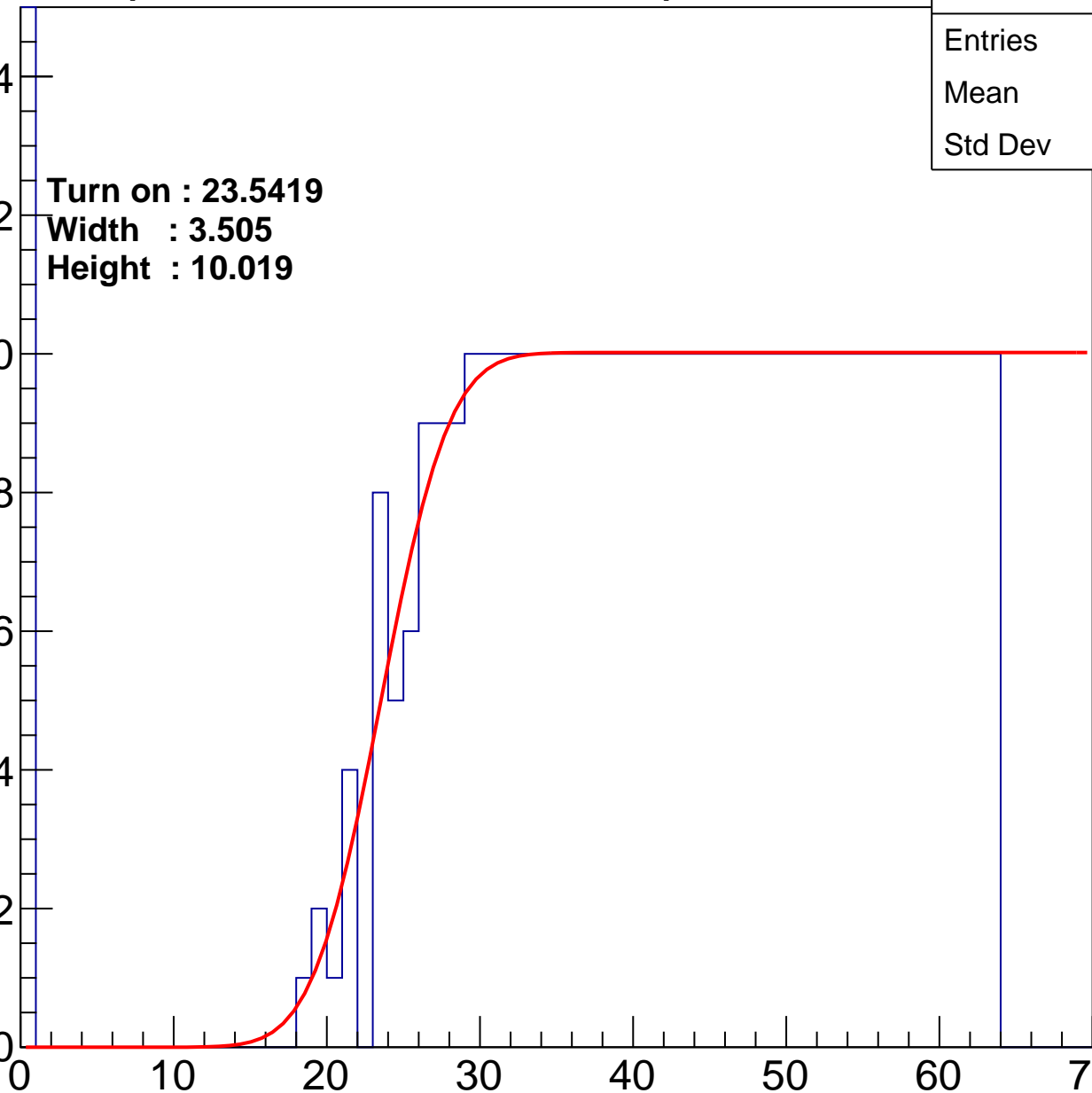
Width : 3.505

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch69

calib_packv5_041523_1651.root, FC#0, port C2

Entries	453
Mean	37.06
Std Dev	19.47

Turn on : 26.6744

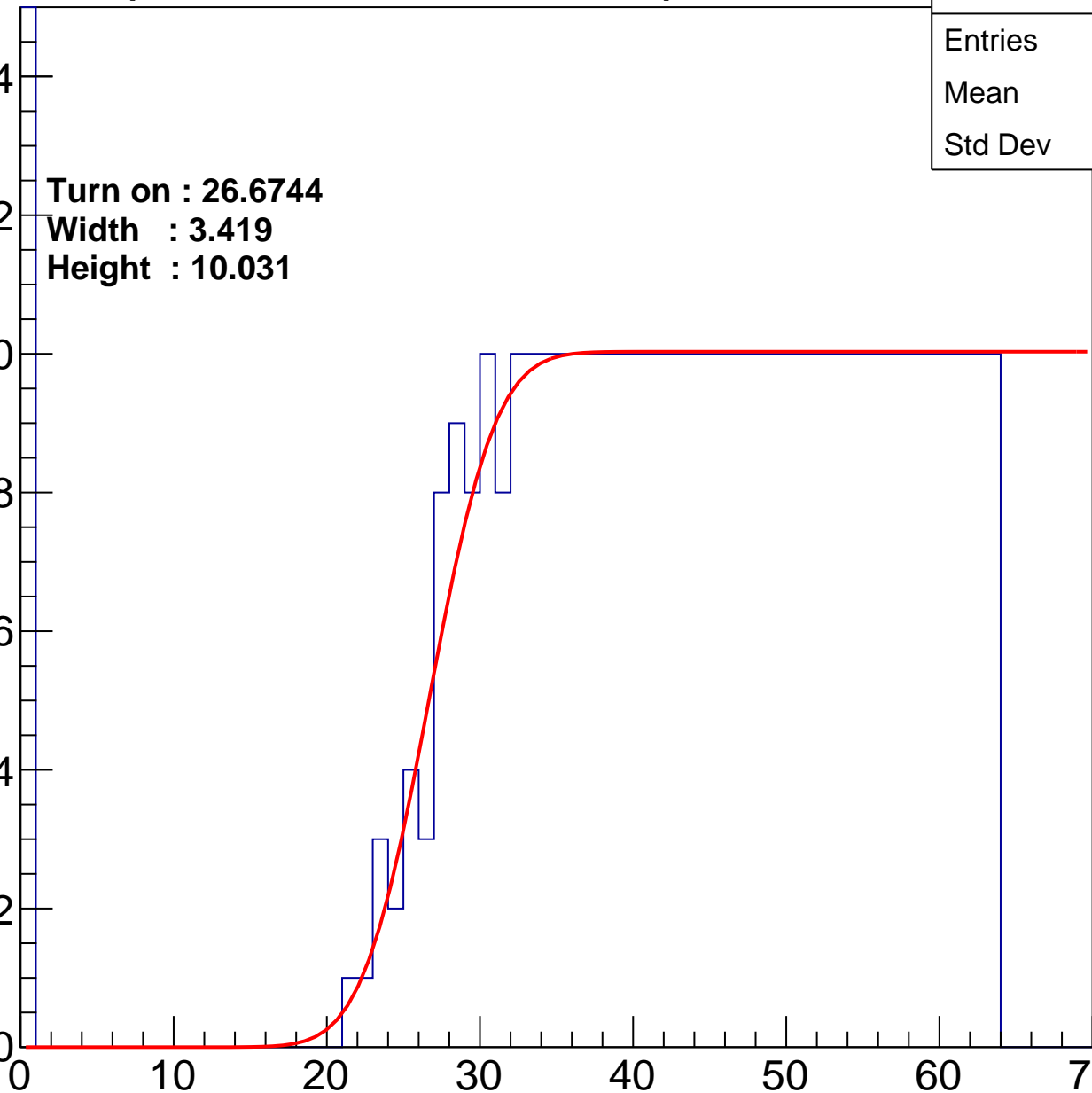
Width : 3.419

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch70

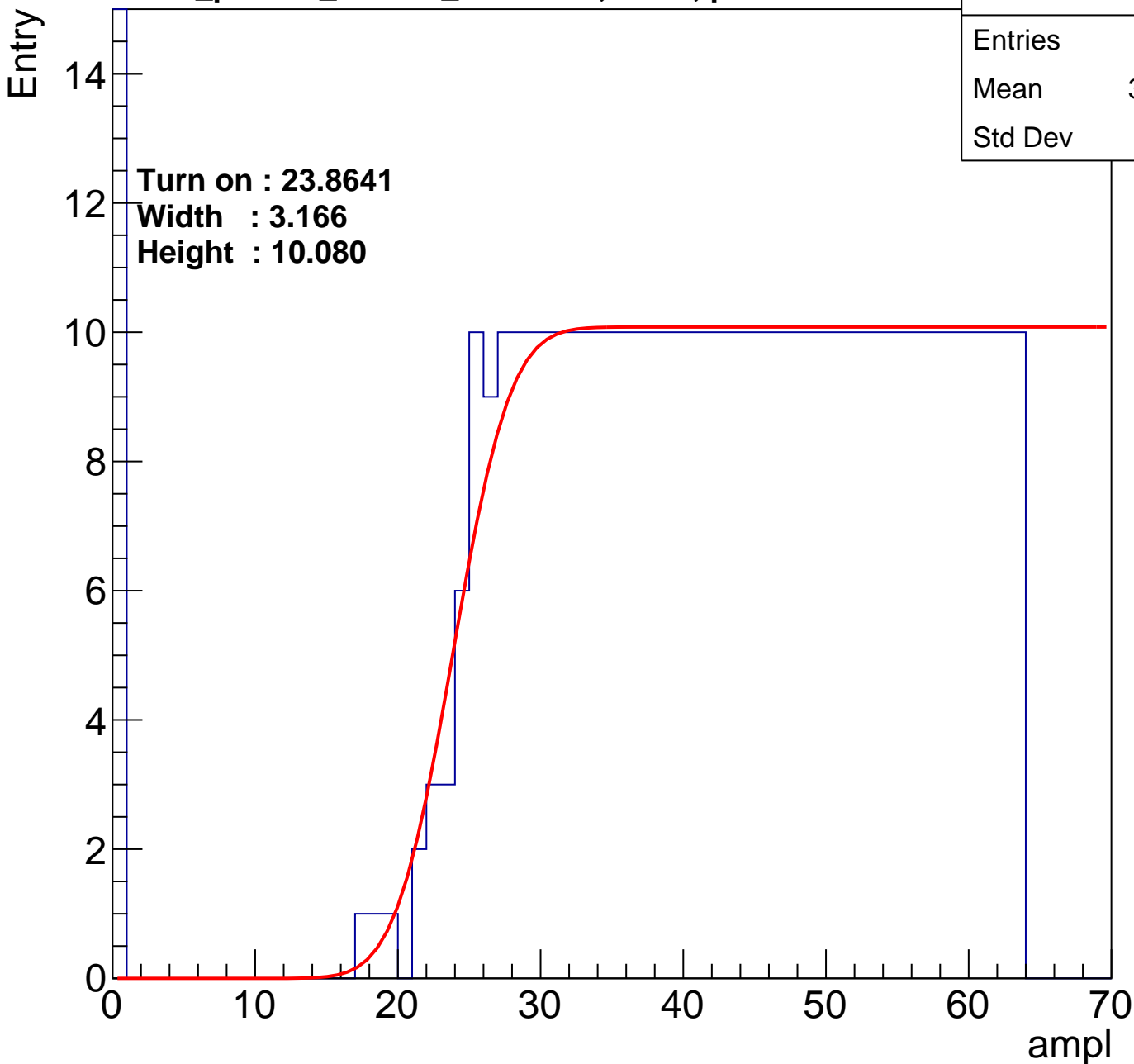
calib_packv5_041523_1651.root, FC#0, port C2

Entries	452
Mean	38.74
Std Dev	17.21

Turn on : 23.8641

Width : 3.166

Height : 10.080



B1L103S, U3-ch71

calib_packv5_041523_1651.root, FC#0, port C2

Entries	410
Mean	40.64
Std Dev	16.64

Turn on : 27.1683

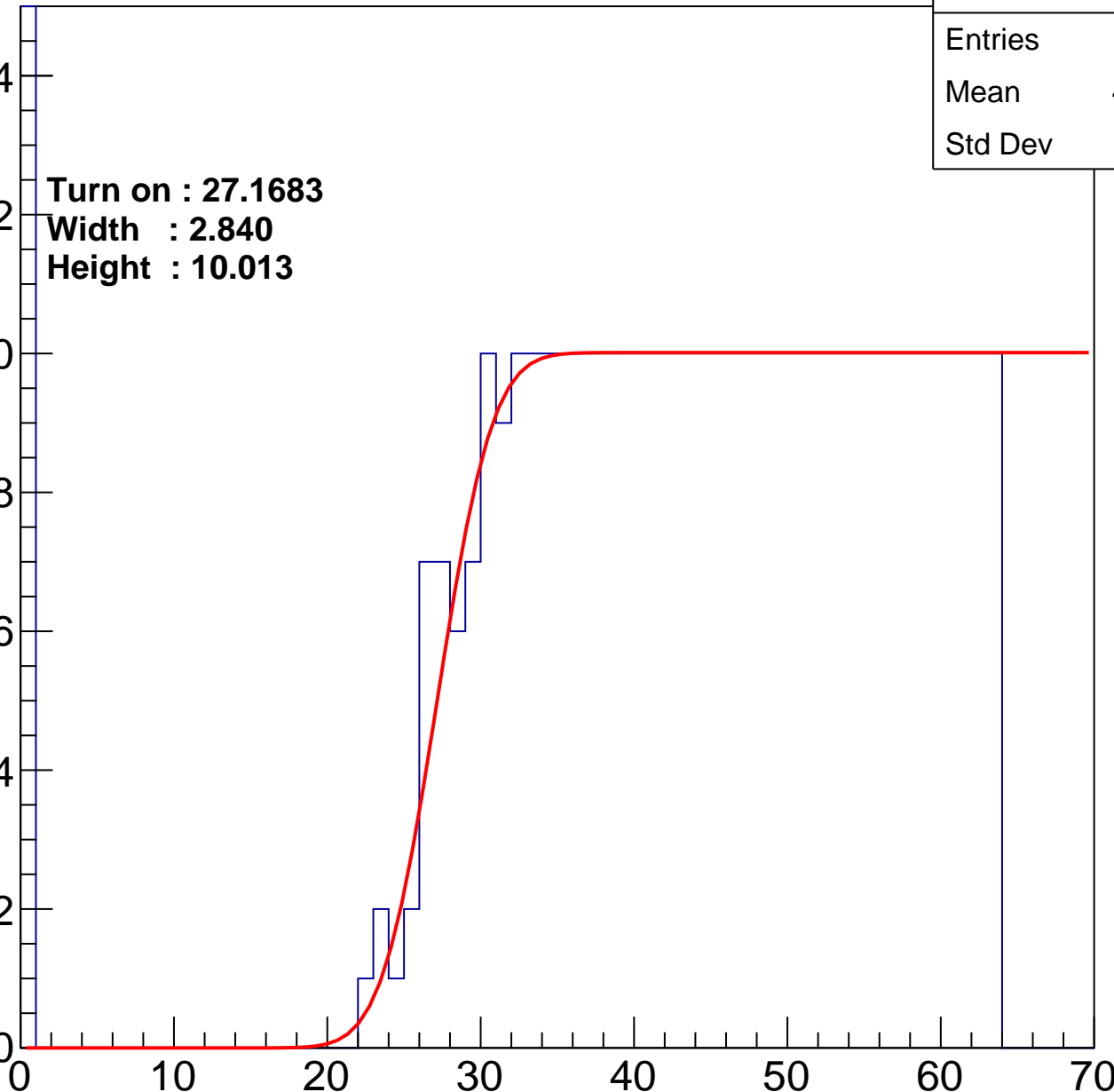
Width : 2.840

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch72

calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	38.64
Std Dev	18.35

Turn on : 26.4434

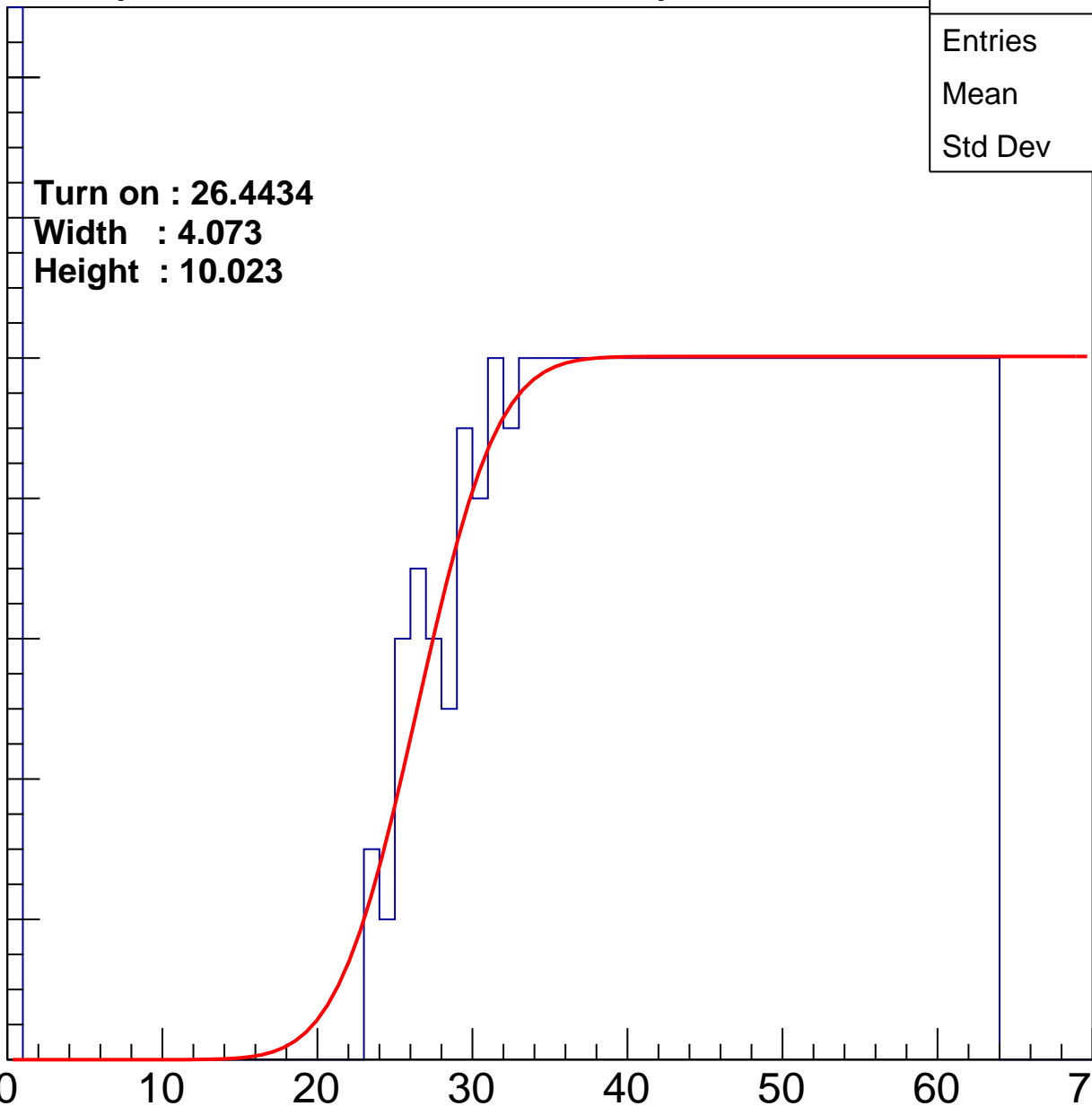
Width : 4.073

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch73

calib_packv5_041523_1651.root, FC#0, port C2

Entries	415
Mean	40.36
Std Dev	16.81

Turn on : 26.6237

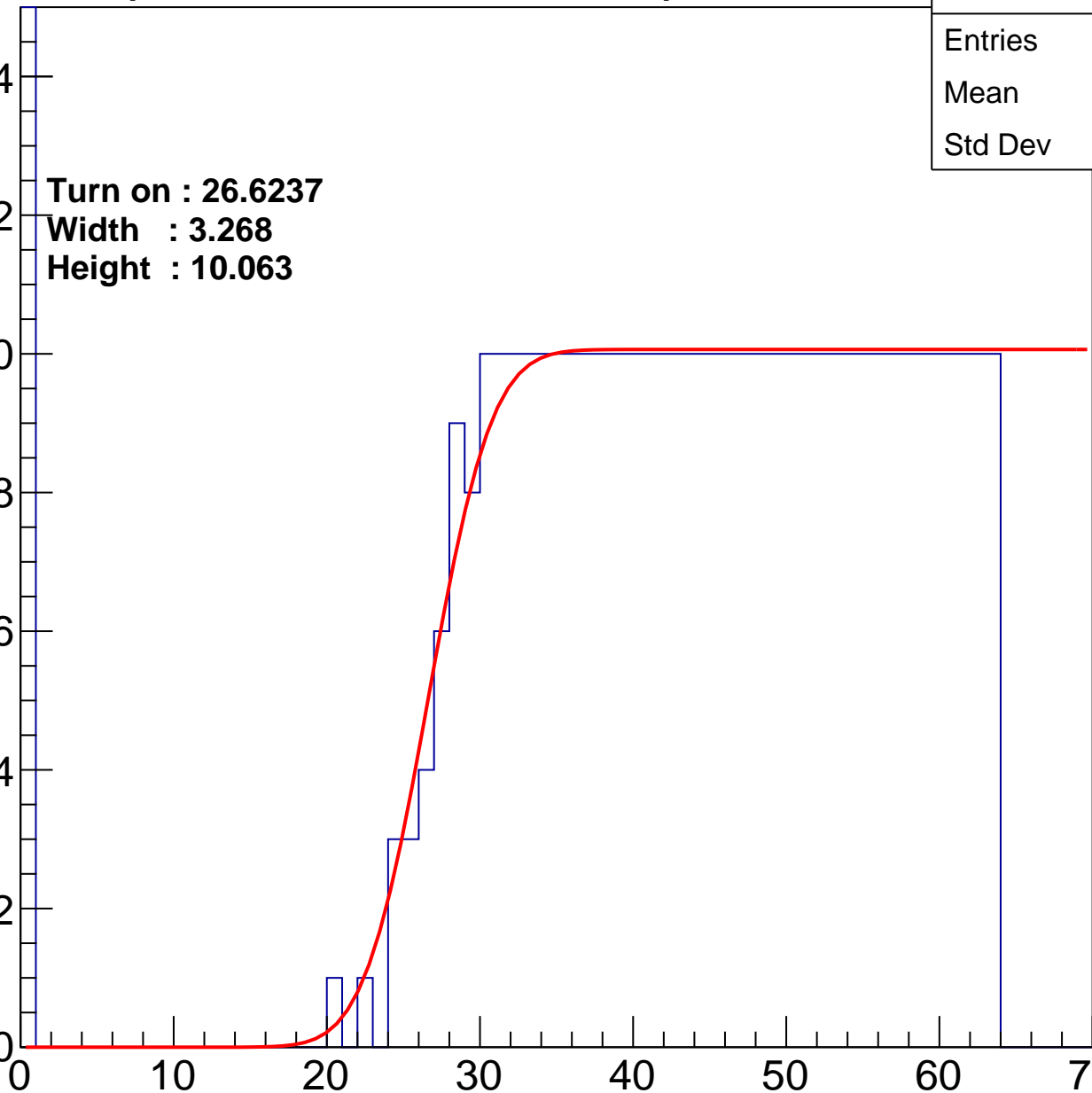
Width : 3.268

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch74

calib_packv5_041523_1651.root, FC#0, port C2

Entries	427
Mean	39.65
Std Dev	17.18

Turn on : 26.1020

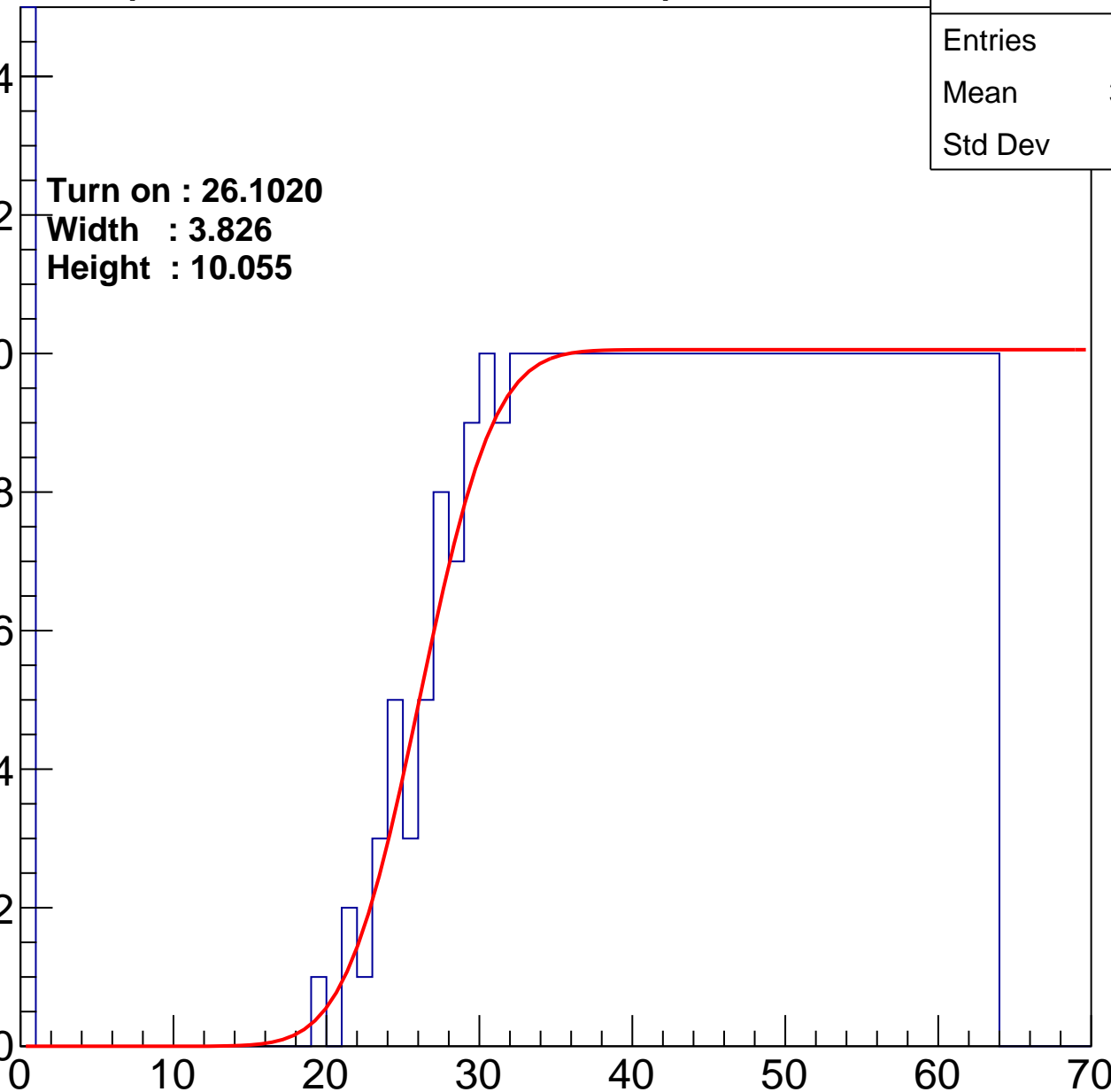
Width : 3.826

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch75

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	39.36
Std Dev	16.9

Turn on : 24.1778

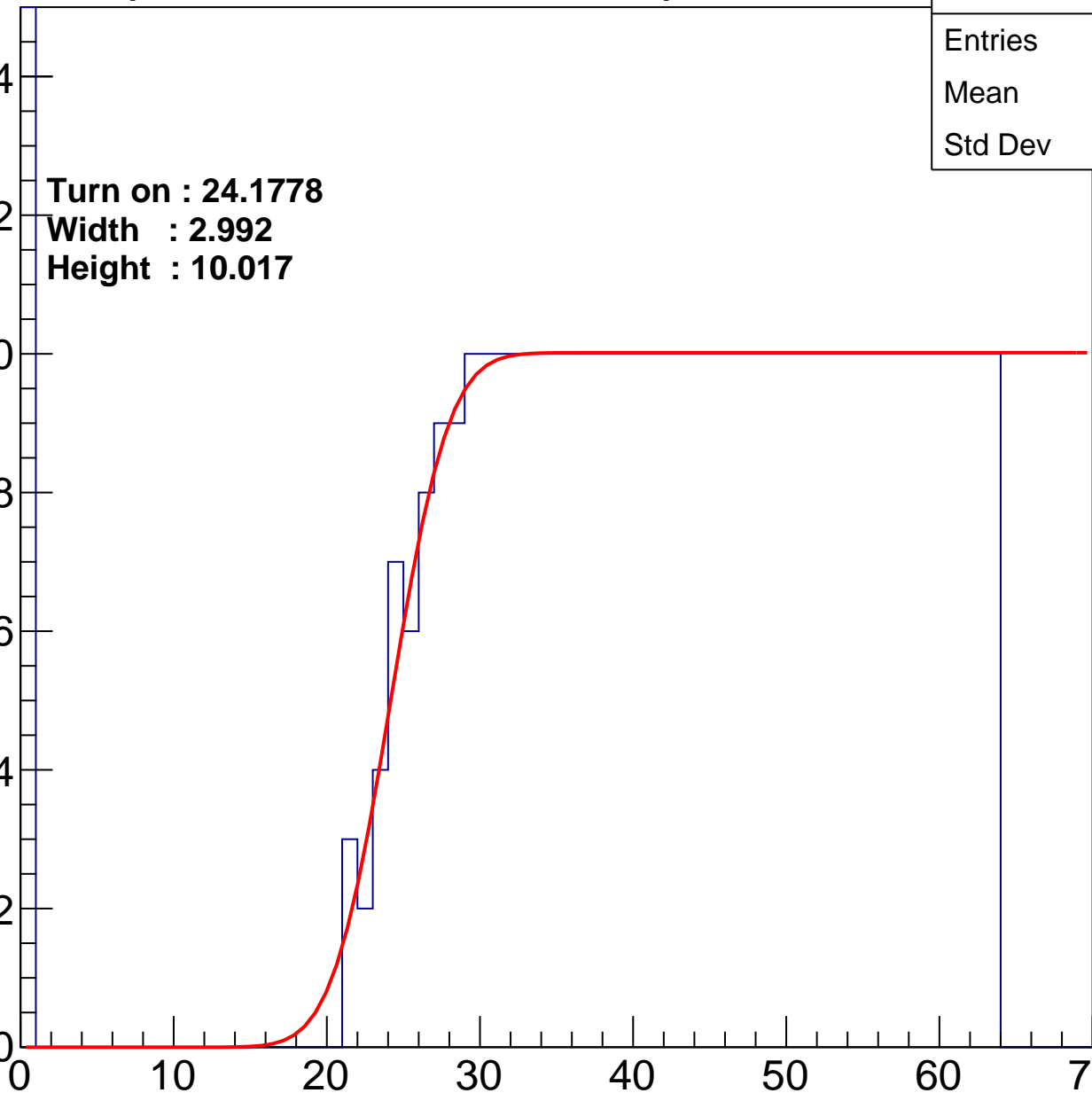
Width : 2.992

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch76

calib_packv5_041523_1651.root, FC#0, port C2

Entries	445
Mean	39.08
Std Dev	17.06

Turn on : 23.8575

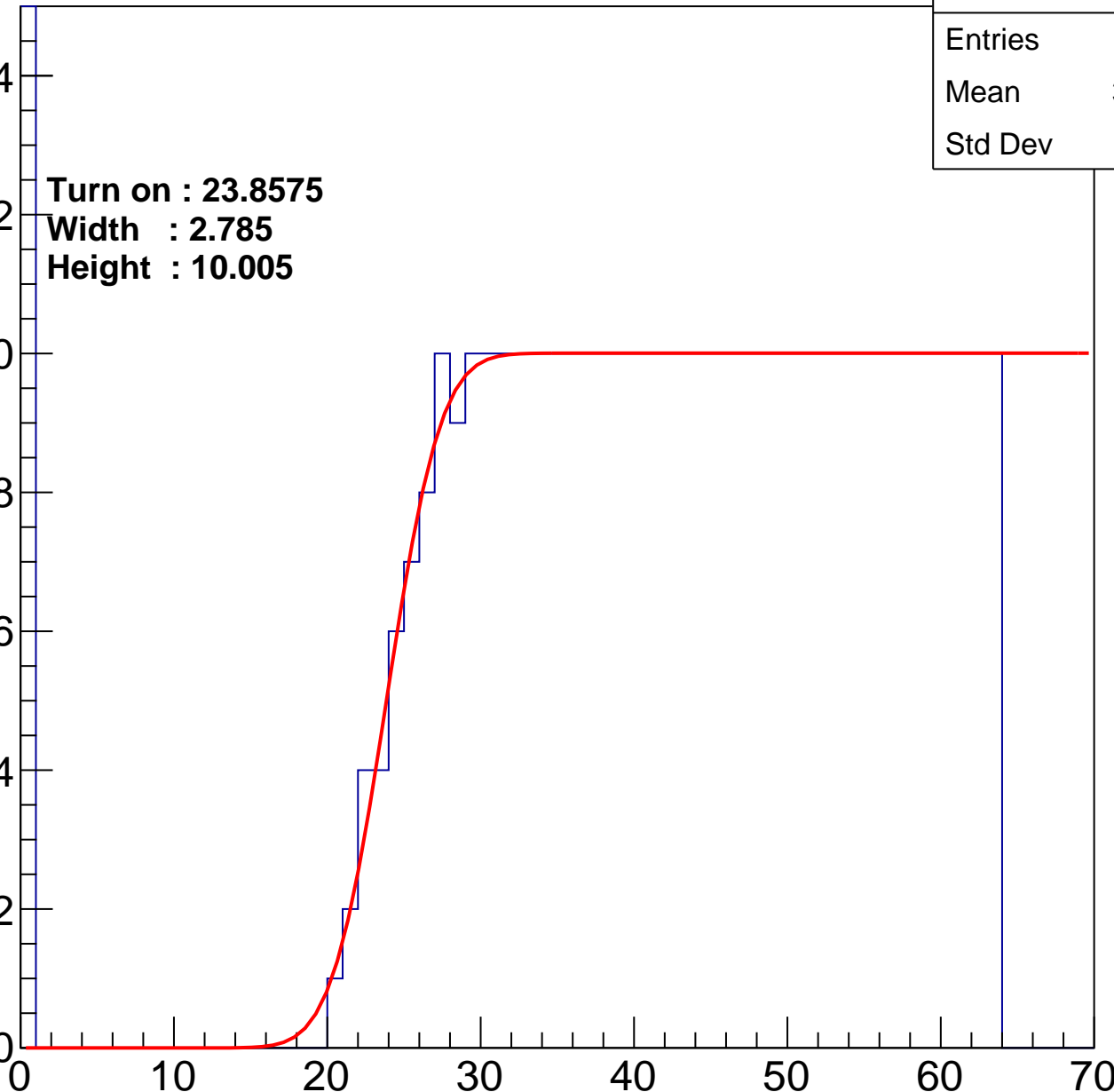
Width : 2.785

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch77

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	39.2
Std Dev	17.27

Turn on : 24.7195

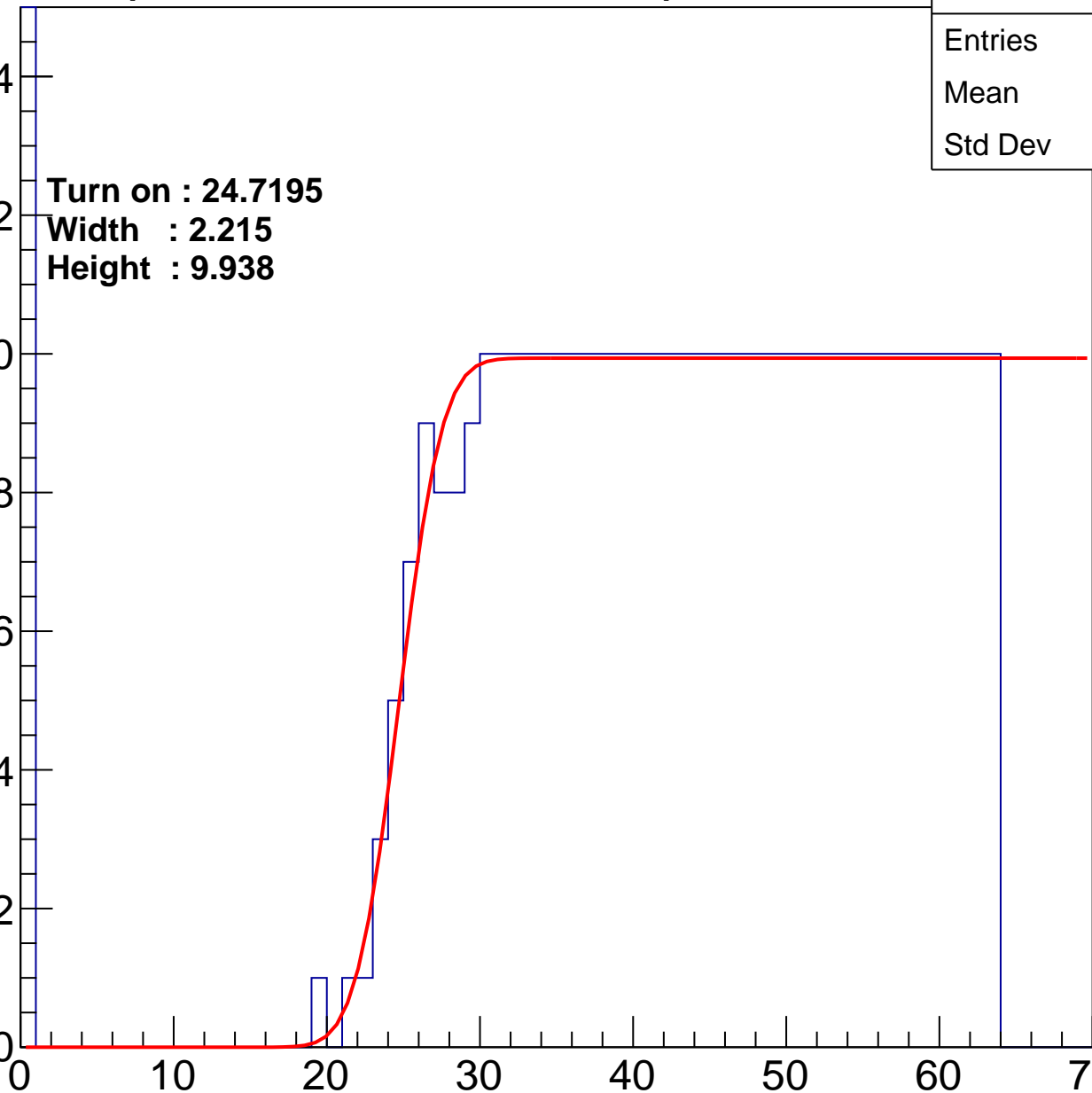
Width : 2.215

Height : 9.938

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch78

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	39.16
Std Dev	17.41

Turn on : 26.0063

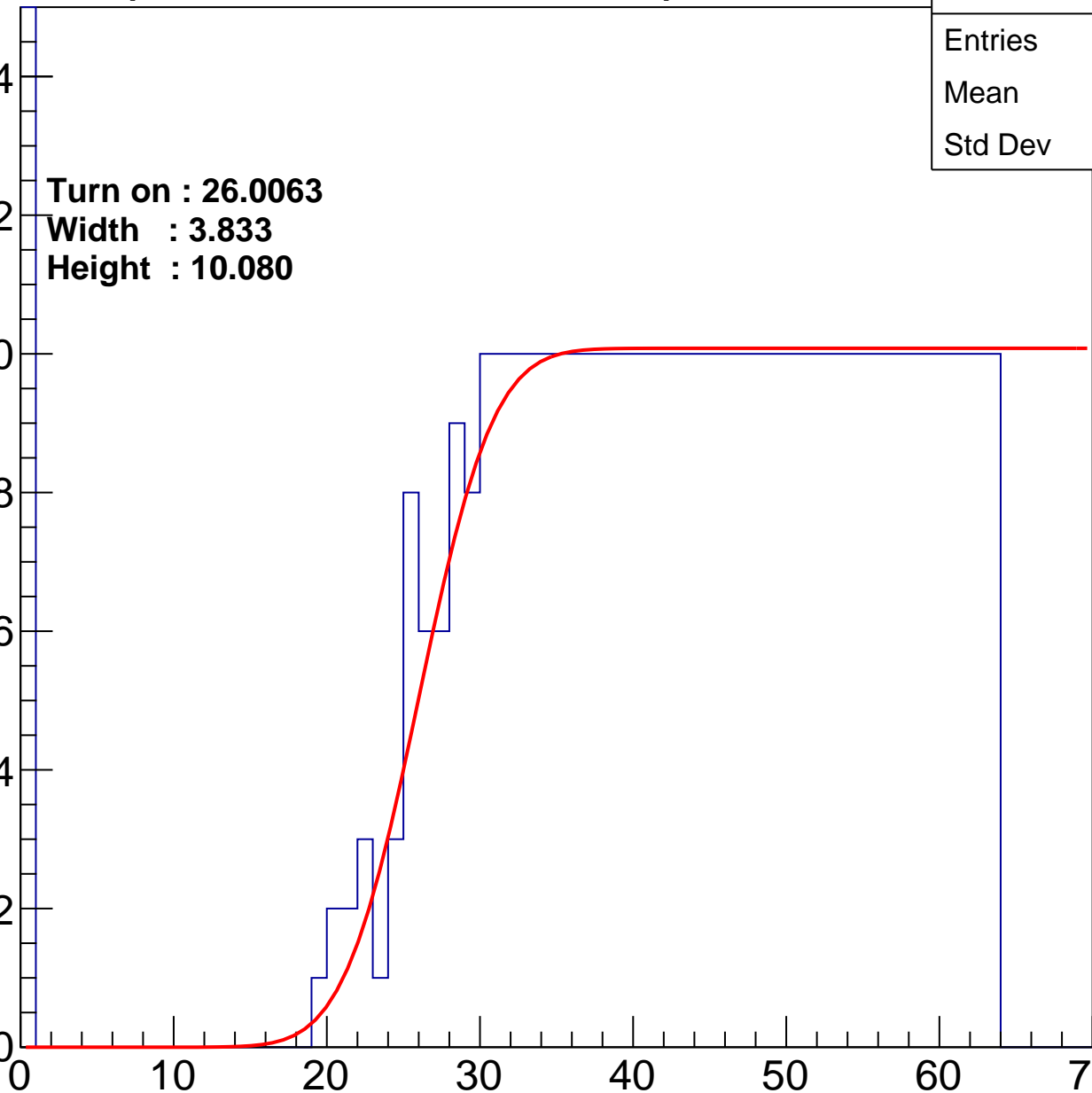
Width : 3.833

Height : 10.080

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch79

calib_packv5_041523_1651.root, FC#0, port C2

Entries	464
Mean	37.98
Std Dev	17.7

Turn on : 22.9675

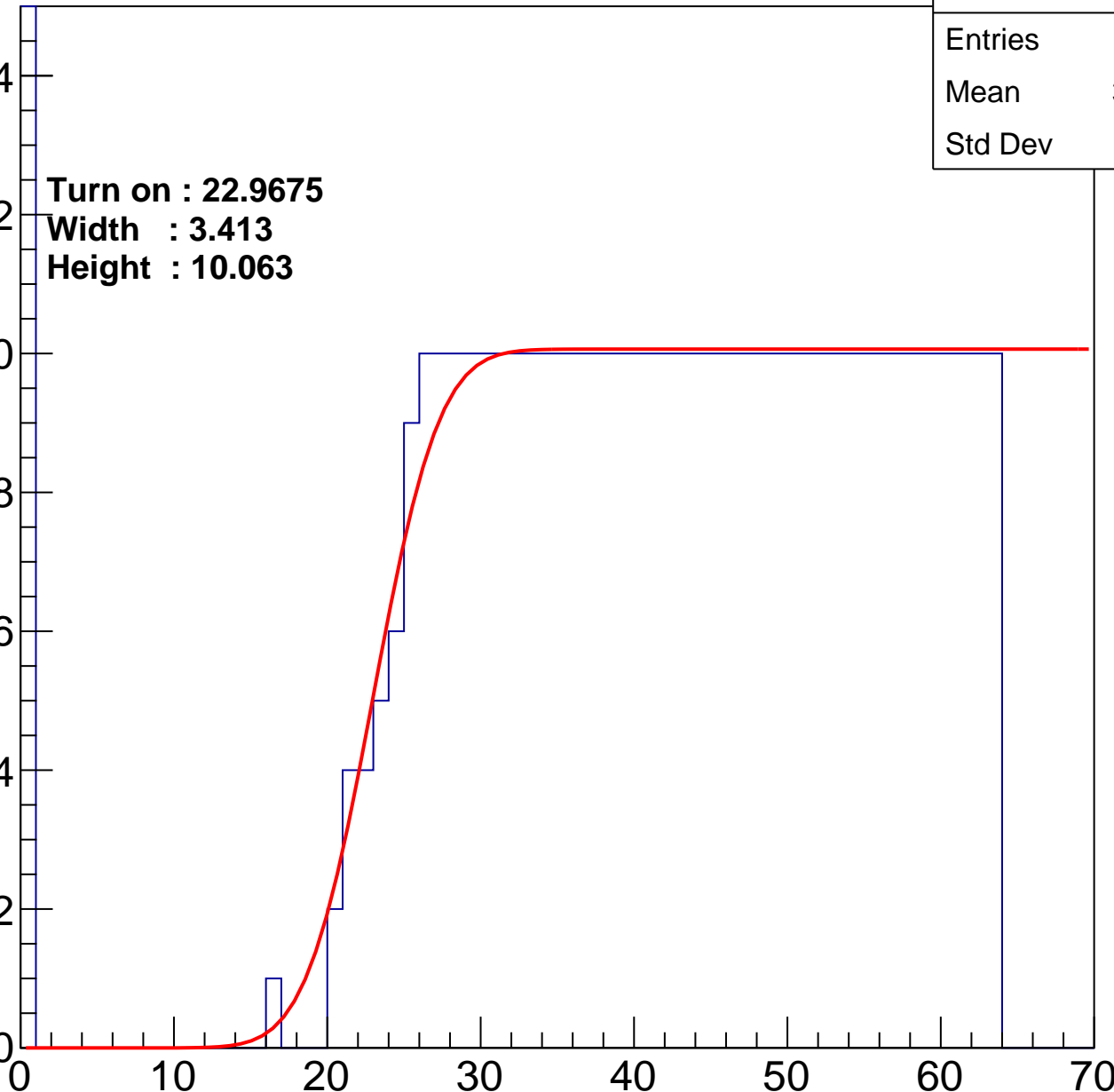
Width : 3.413

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch80

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	39.83
Std Dev	16.49

Turn on : 24.4458

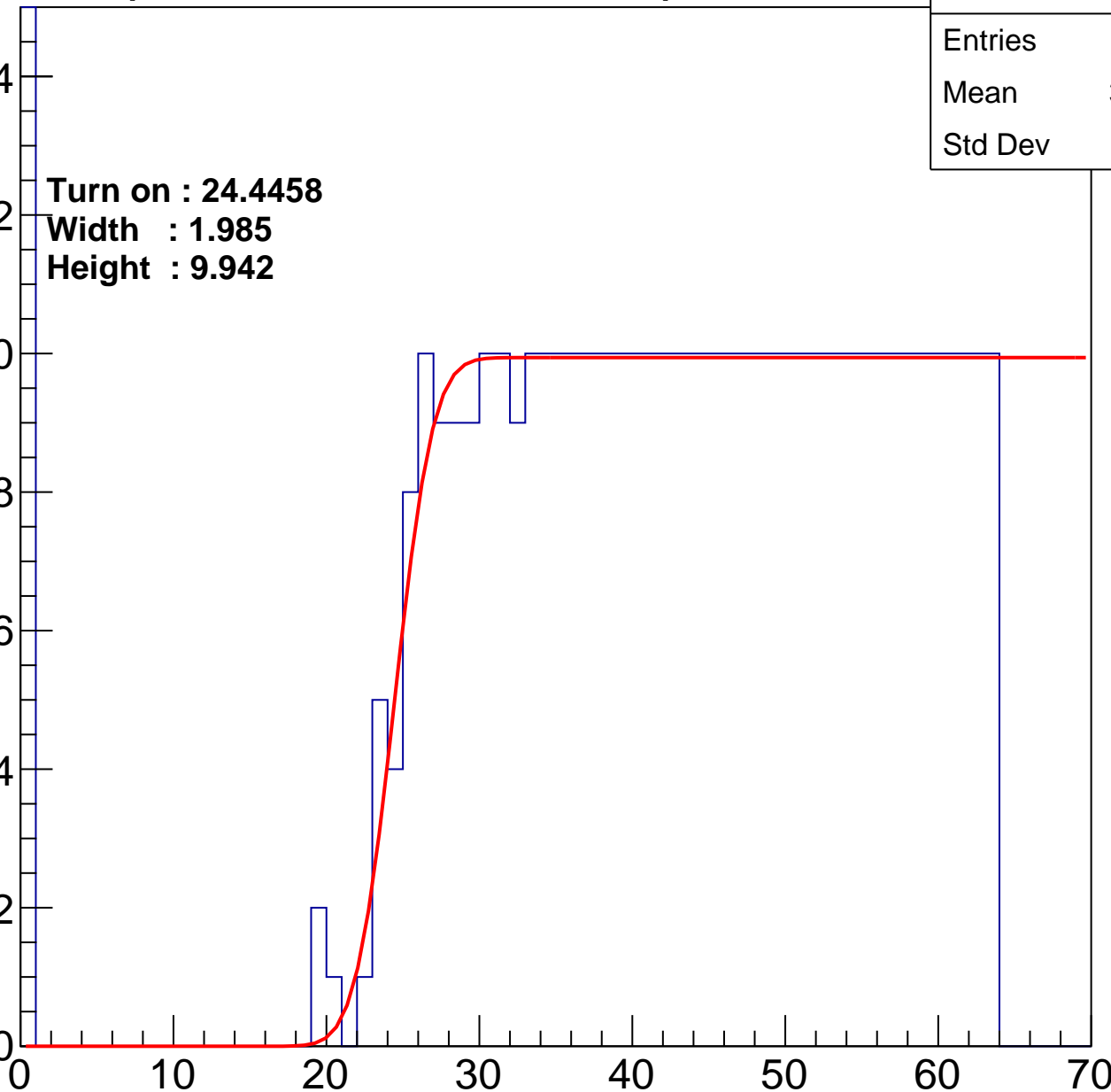
Width : 1.985

Height : 9.942

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch81

calib_packv5_041523_1651.root, FC#0, port C2

Entries	447
Mean	38.08
Std Dev	18.44

Turn on : 25.9698

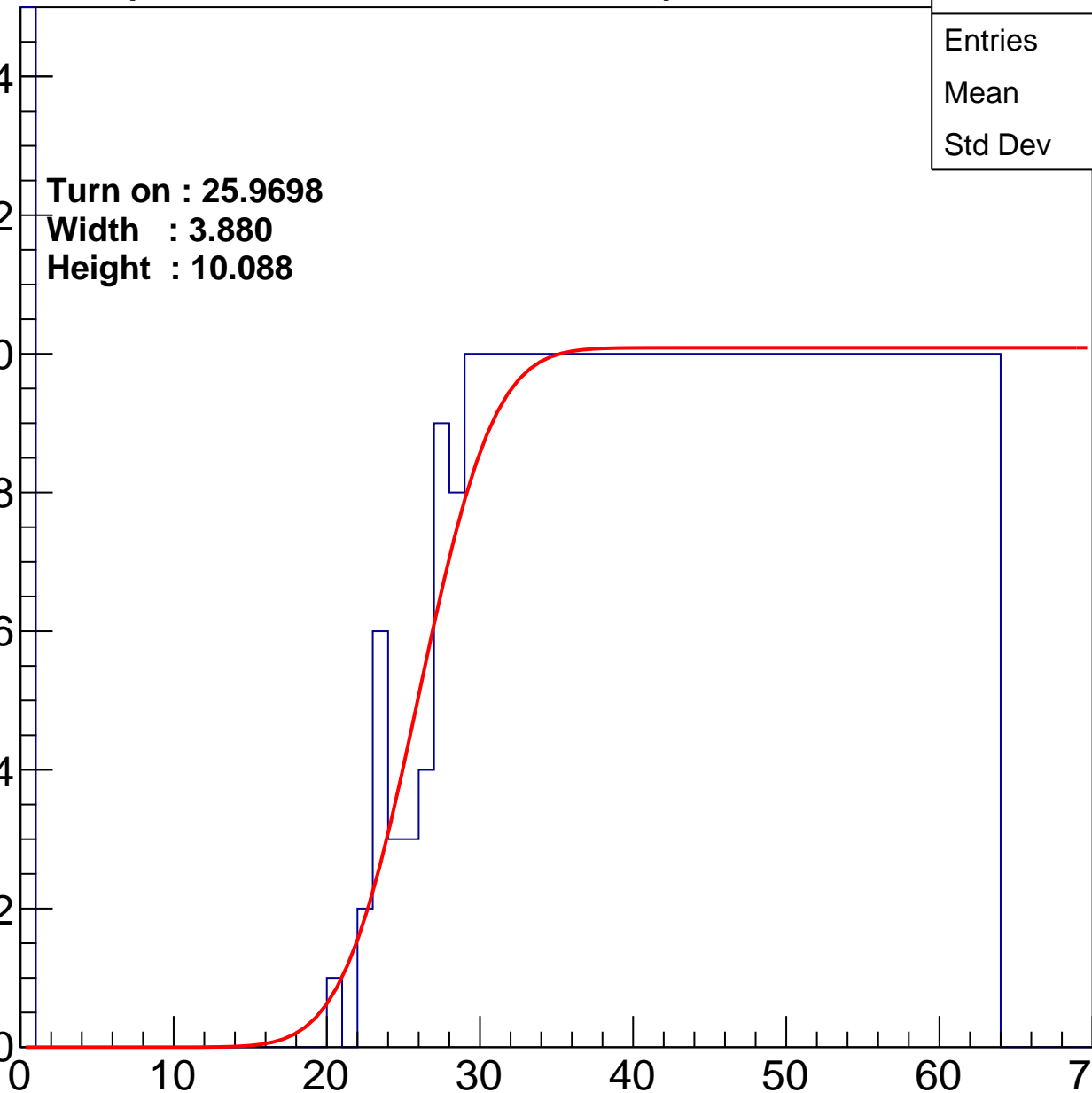
Width : 3.880

Height : 10.088

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch82

calib_packv5_041523_1651.root, FC#0, port C2

Entries	577
Mean	30.78
Std Dev	21.5

Turn on : 23.3584

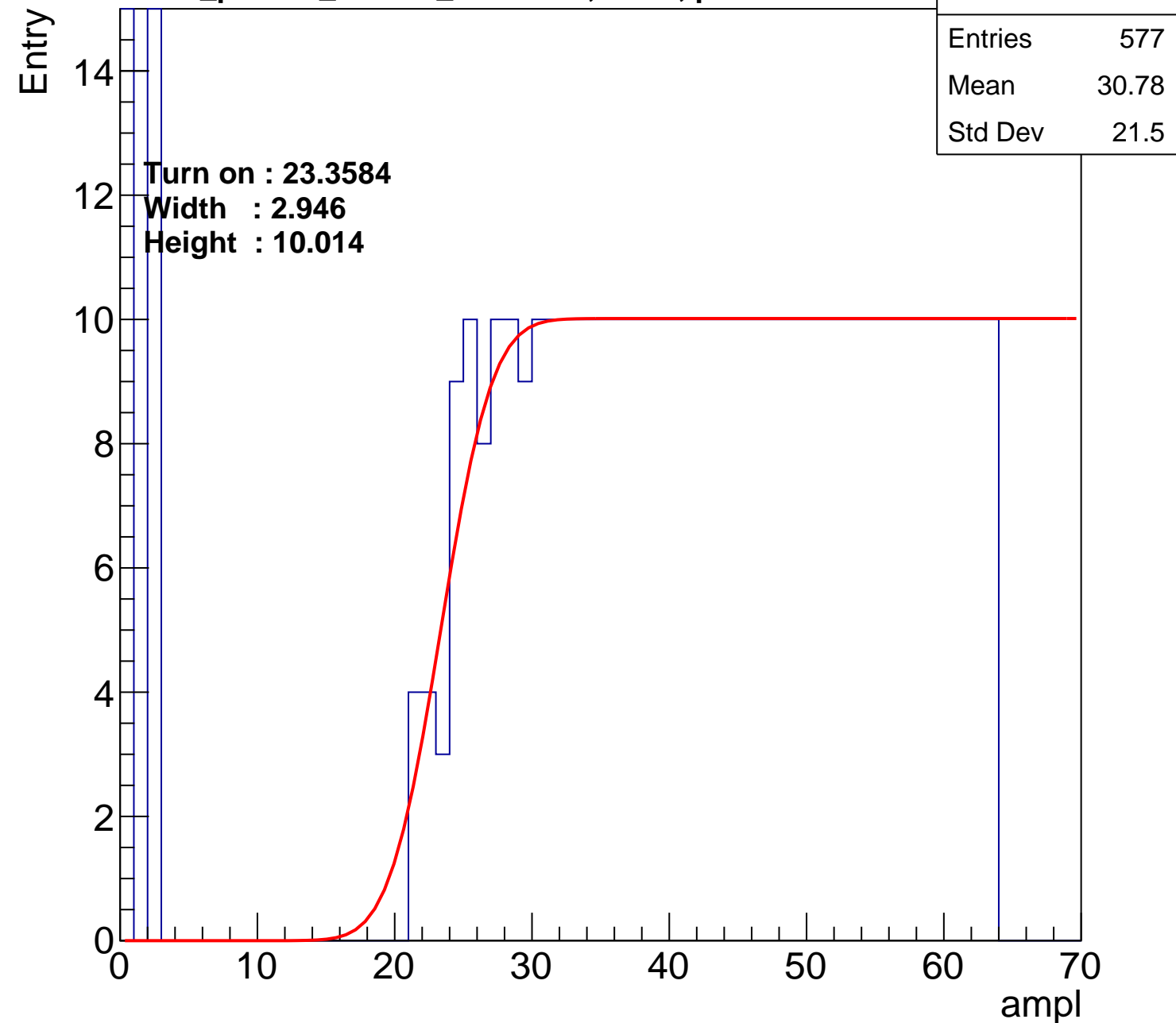
Width : 2.946

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch83

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	38.81
Std Dev	17.97

Turn on : 26.2775

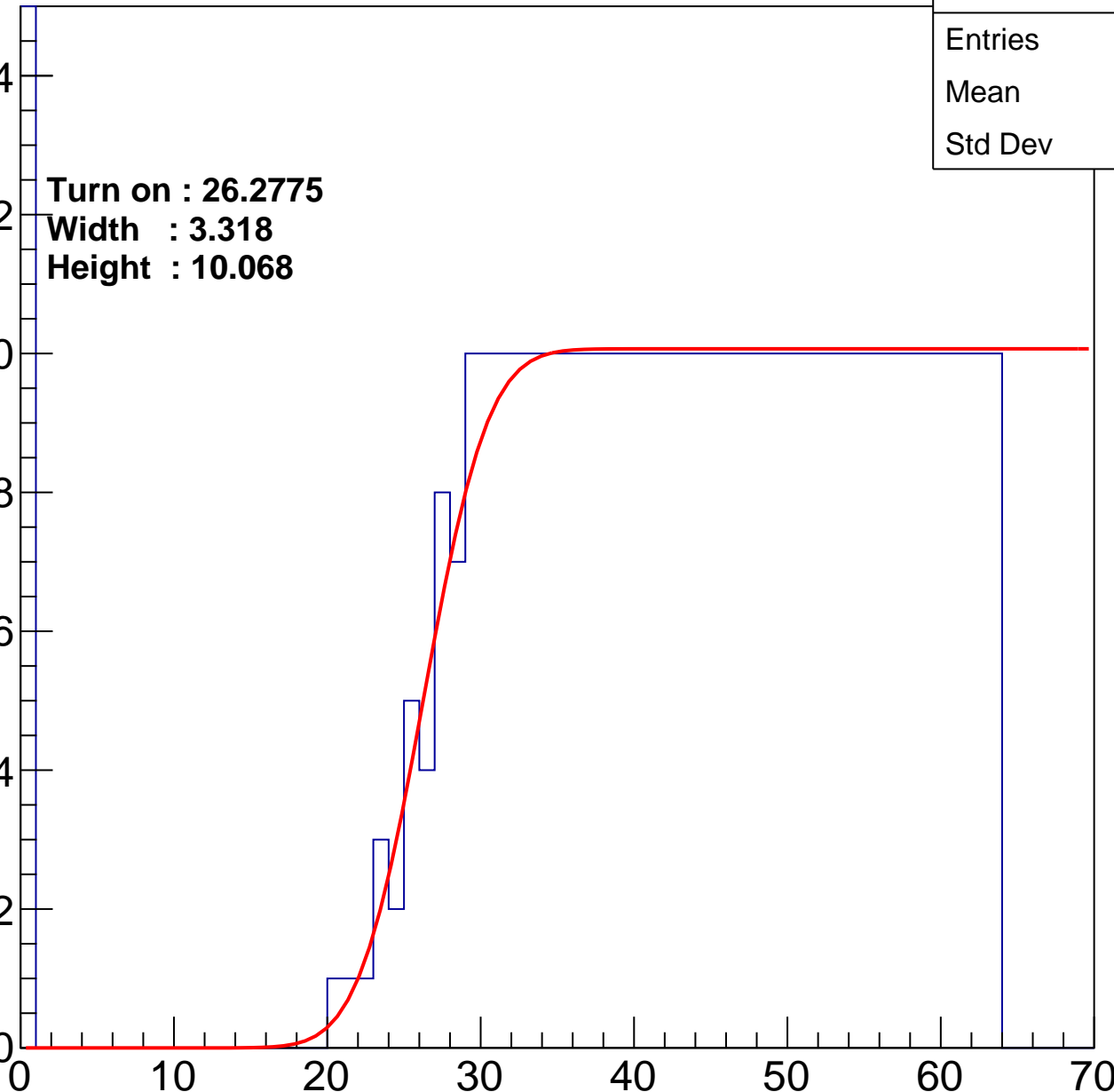
Width : 3.318

Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch84

calib_packv5_041523_1651.root, FC#0, port C2

Entries	462
Mean	37.81
Std Dev	18.06

Turn on : 23.4254

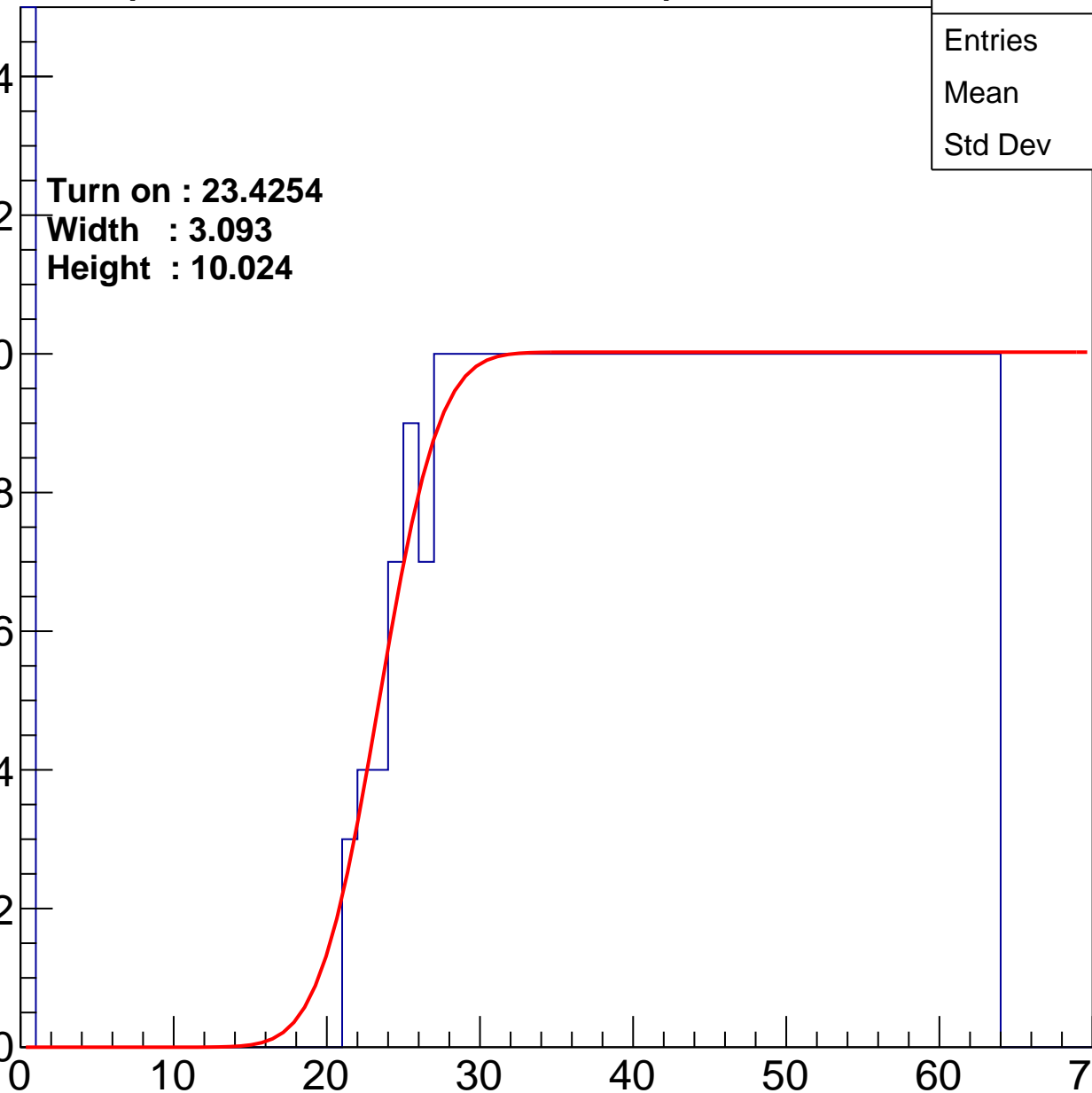
Width : 3.093

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch85

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	39.58
Std Dev	17.54

Turn on : 26.7912

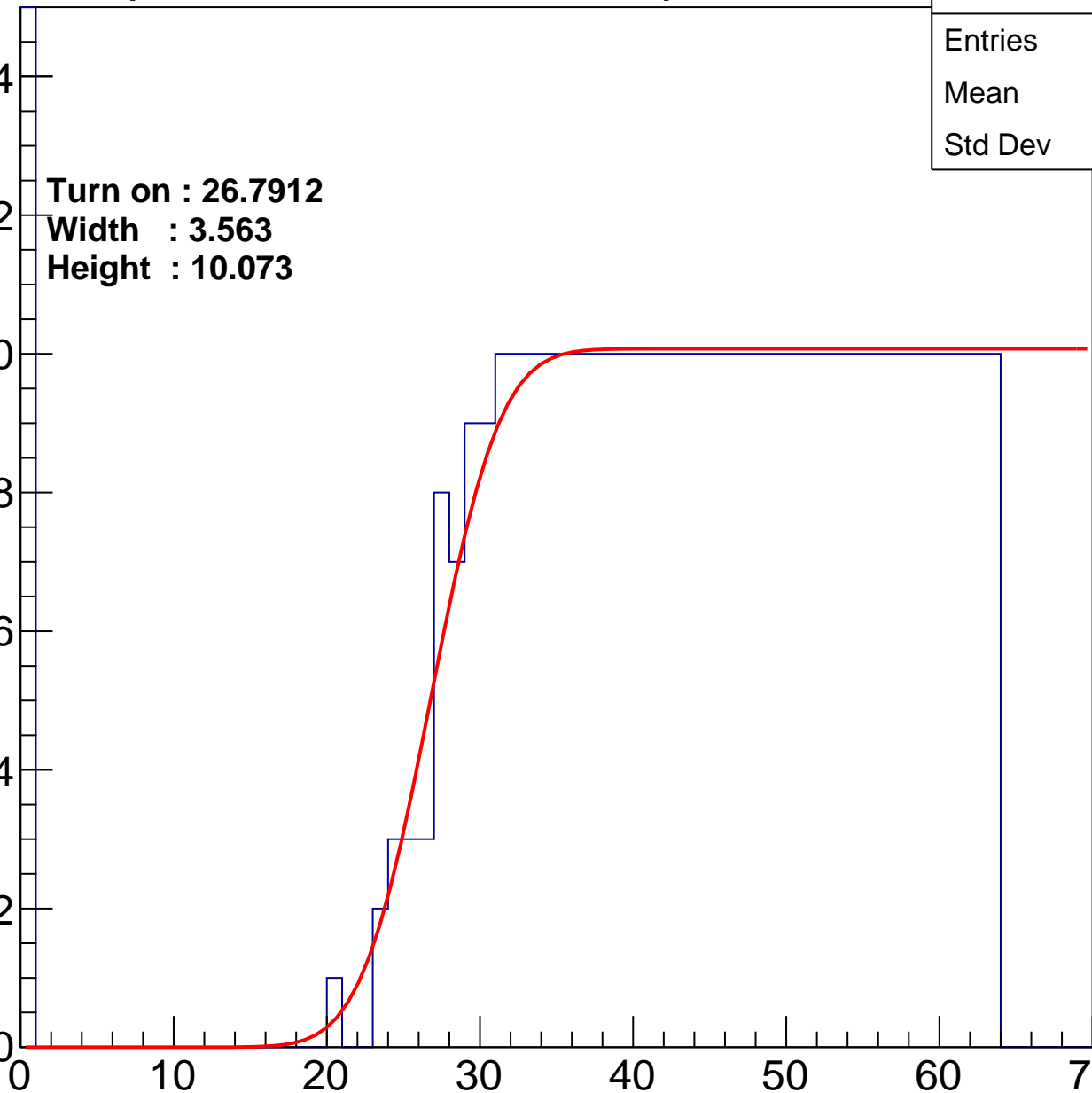
Width : 3.563

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch86

calib_packv5_041523_1651.root, FC#0, port C2

Entries	441
Mean	38.56
Std Dev	18.08

Turn on : 25.9348

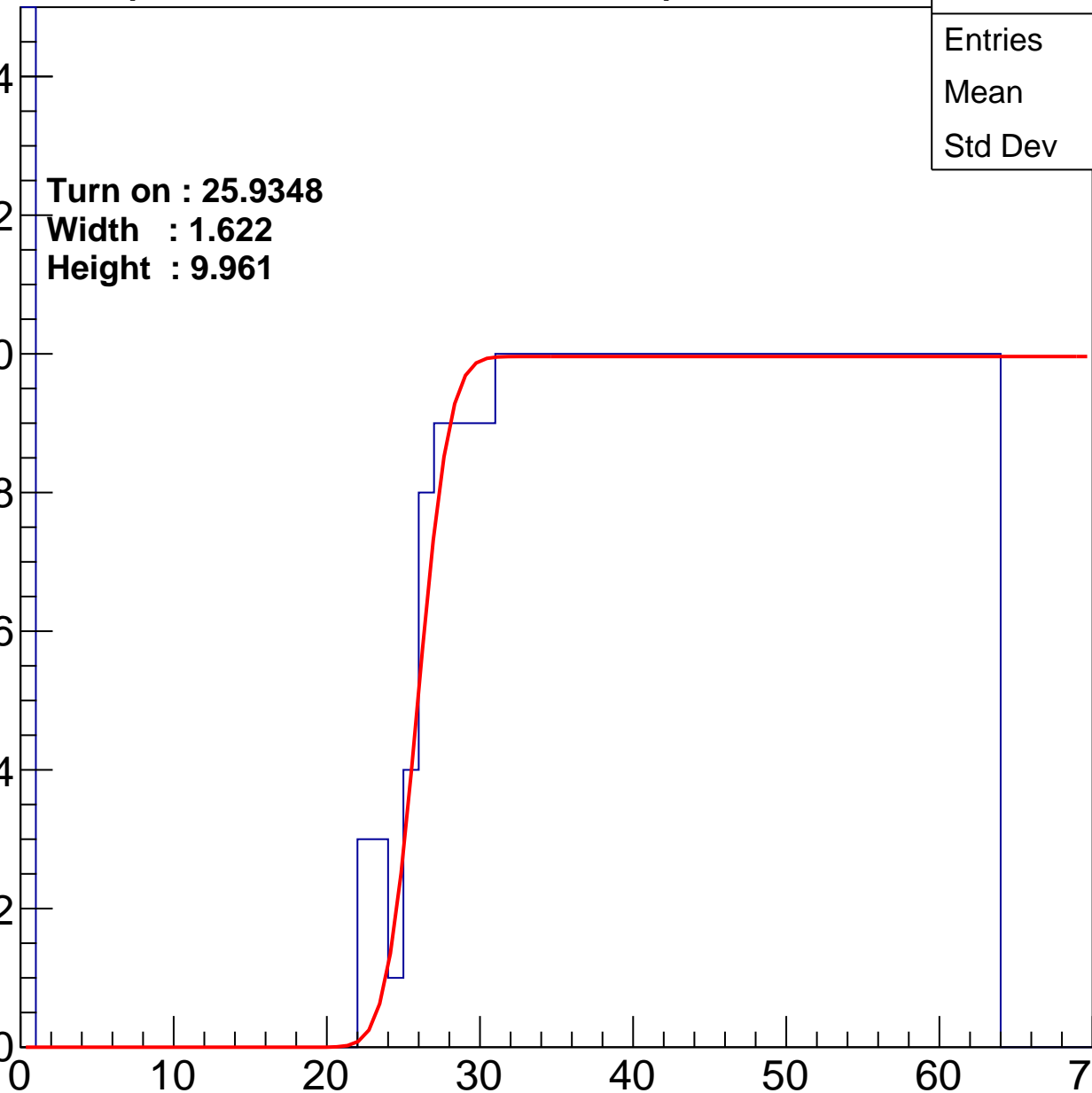
Width : 1.622

Height : 9.961

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch87

calib_packv5_041523_1651.root, FC#0, port C2

Entries	451
Mean	38.17
Std Dev	18.1

Turn on : 24.9188

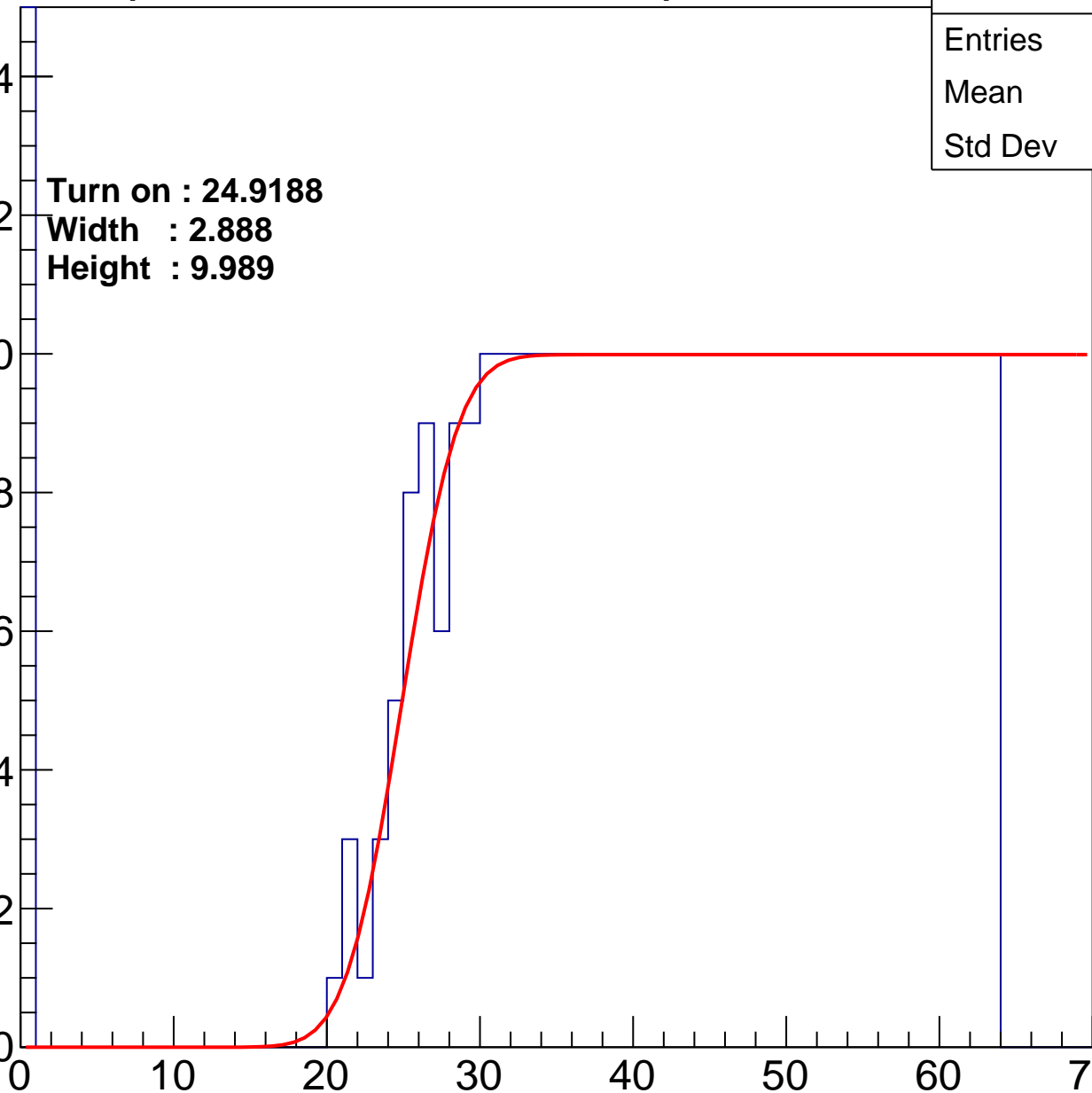
Width : 2.888

Height : 9.989

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch88

calib_packv5_041523_1651.root, FC#0, port C2

Entries	451
Mean	38.31
Std Dev	17.88

Turn on : 24.5845

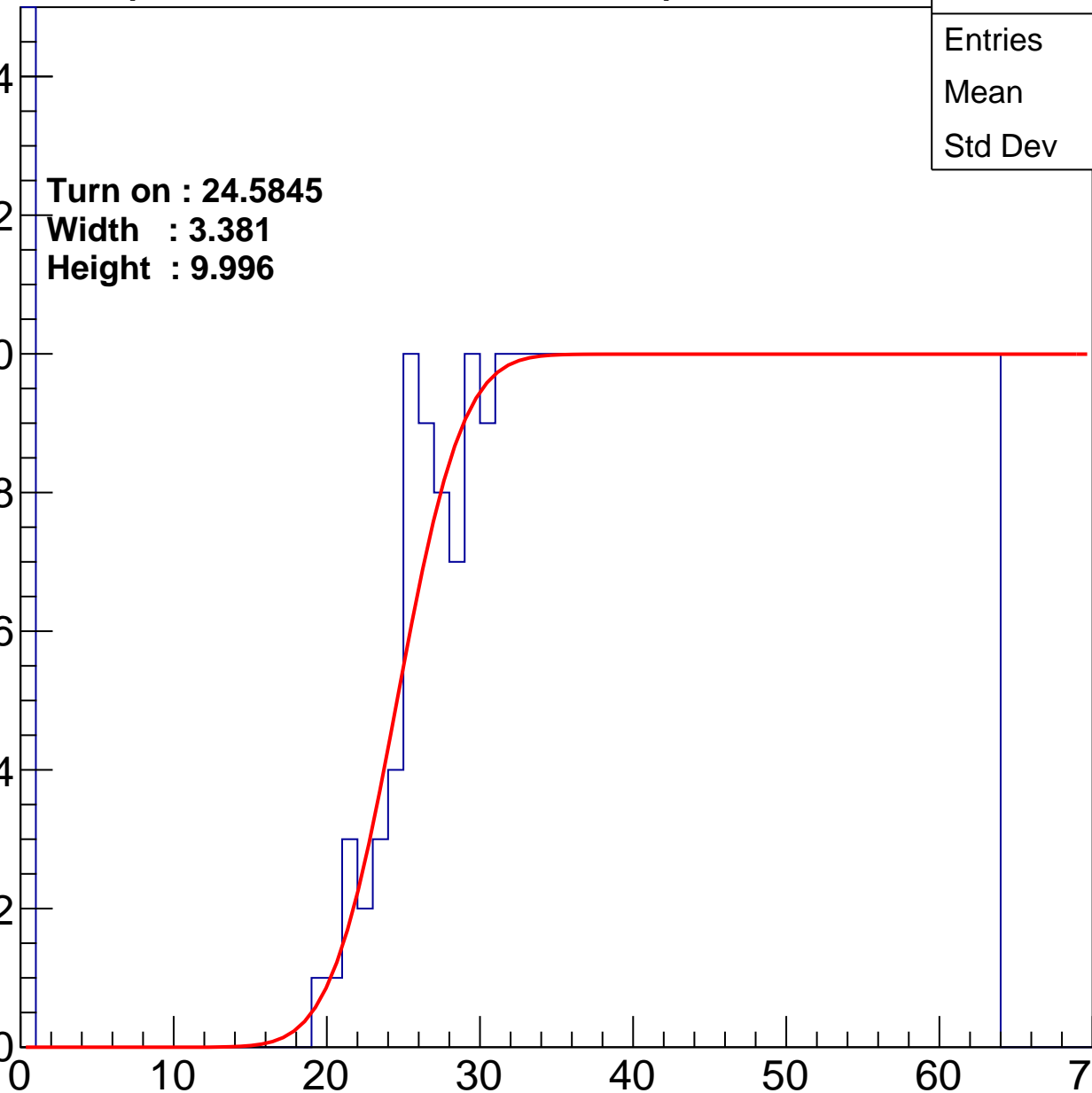
Width : 3.381

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch89

calib_packv5_041523_1651.root, FC#0, port C2

Entries	448
Mean	38.44
Std Dev	17.87

Turn on : 24.6077

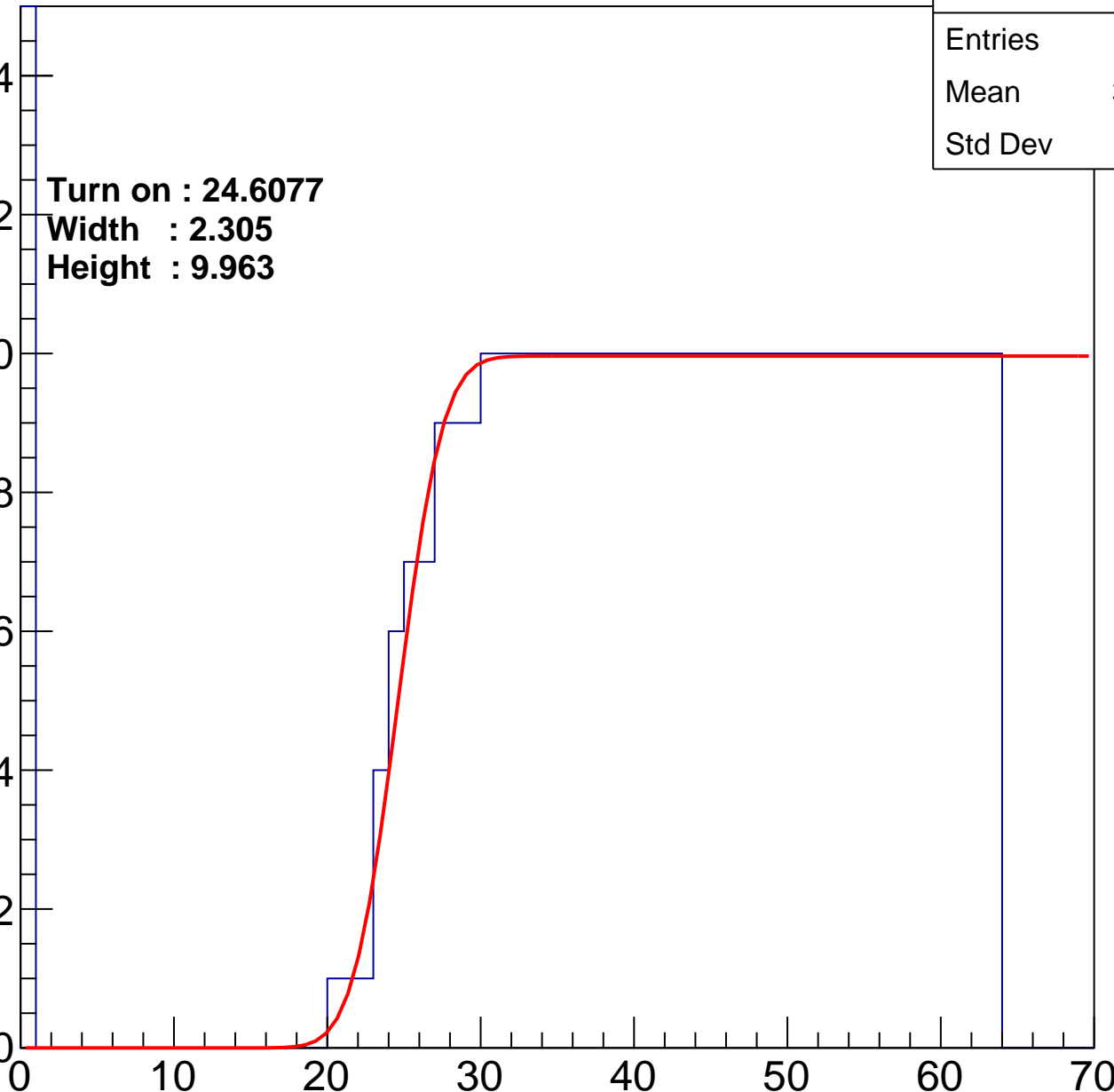
Width : 2.305

Height : 9.963

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch90

calib_packv5_041523_1651.root, FC#0, port C2

Entries	455
Mean	38.01
Std Dev	18.09

Turn on : 24.2679

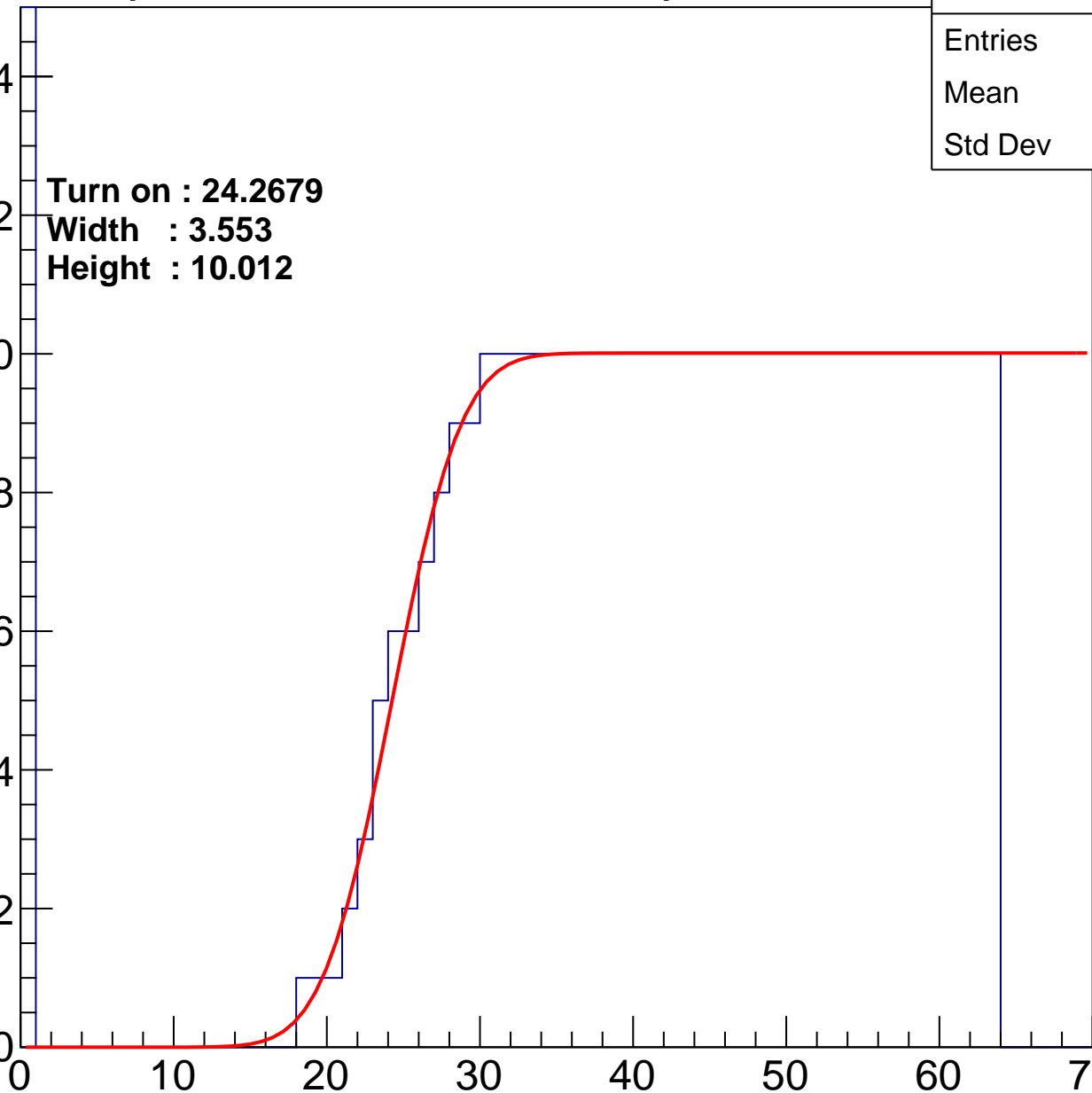
Width : 3.553

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch91

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	38.6
Std Dev	18.24

Turn on : 26.0570

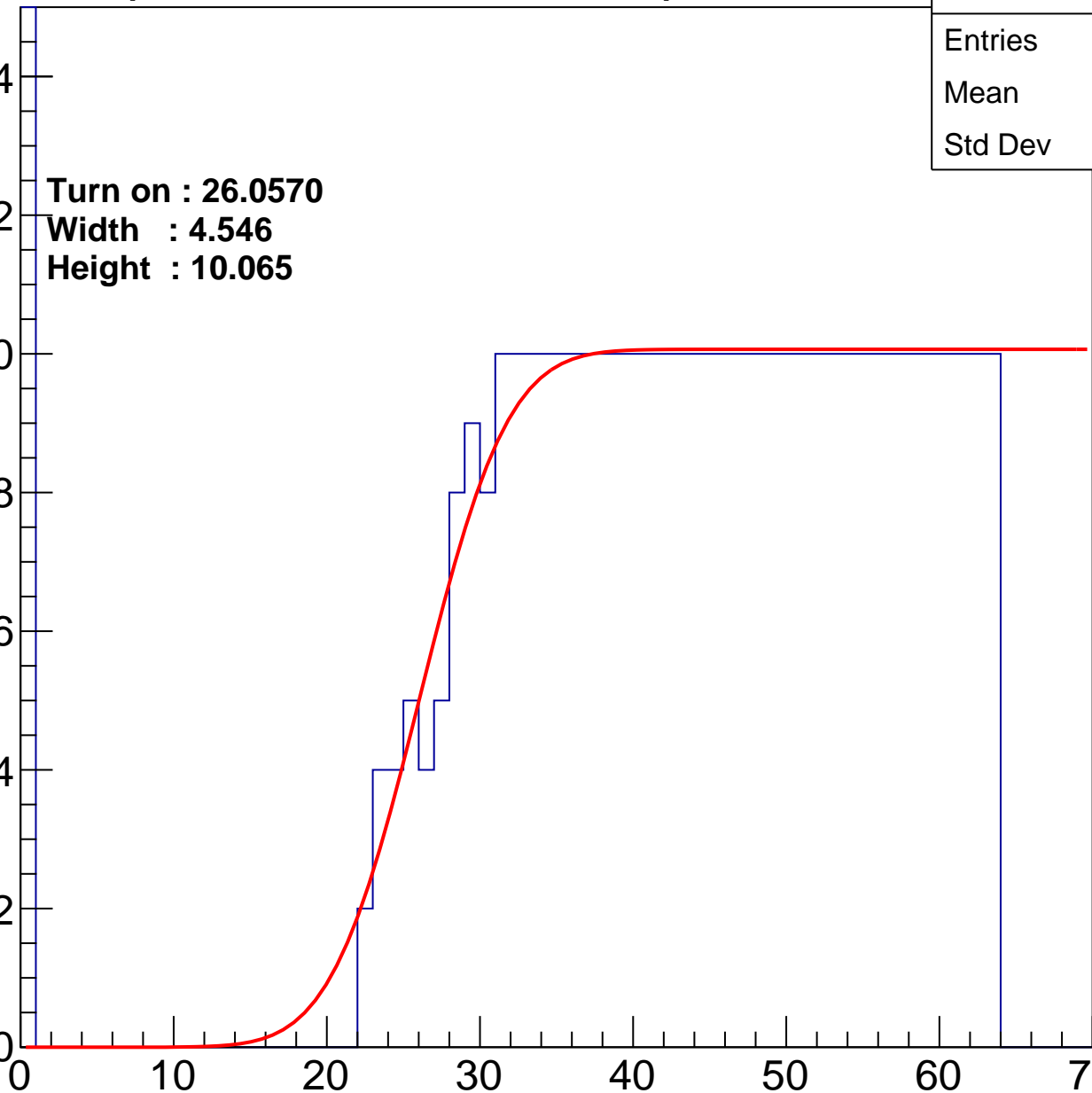
Width : 4.546

Height : 10.065

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch92

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	38.89
Std Dev	17.52

Turn on : 25.2854

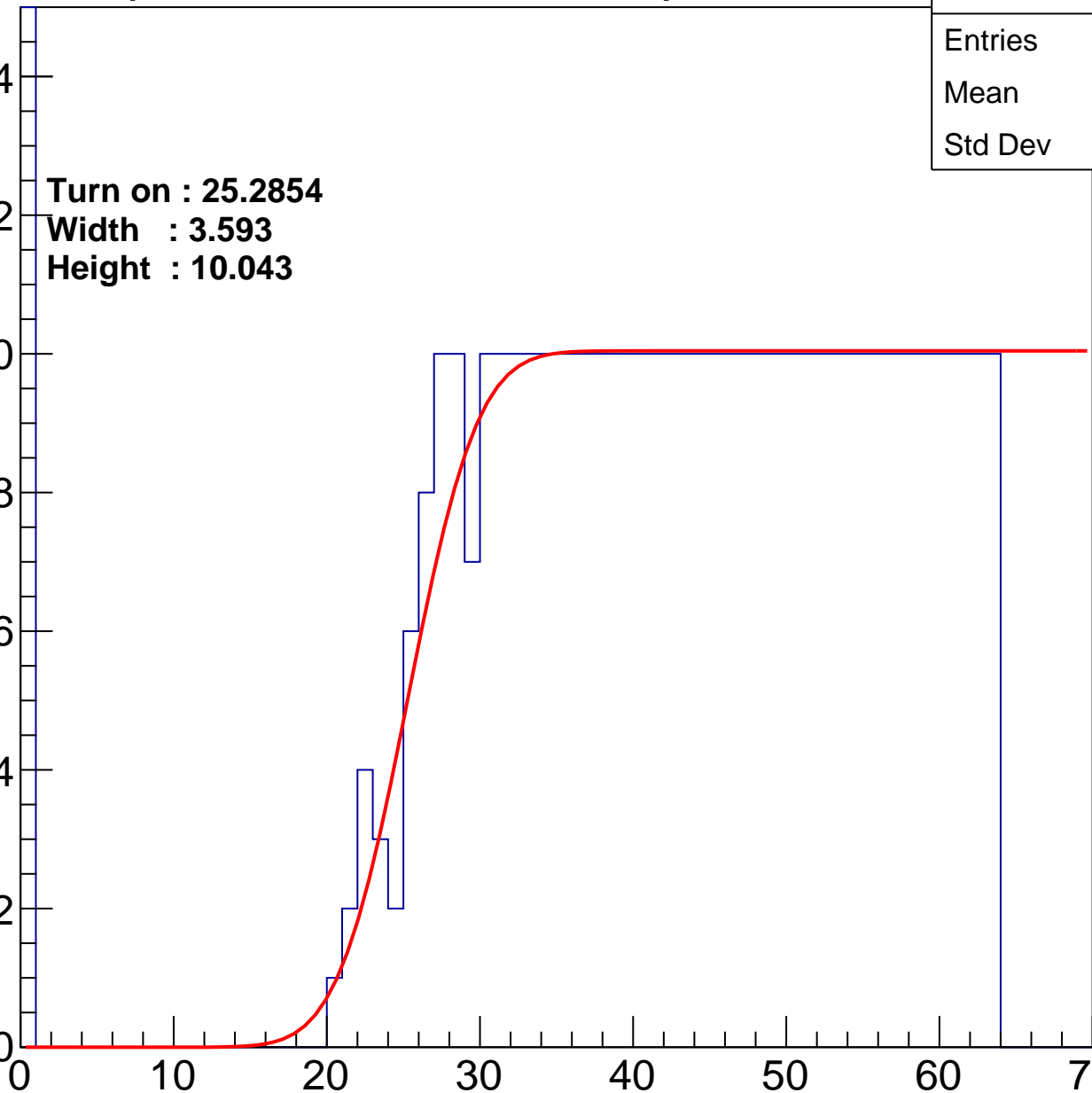
Width : 3.593

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch93

calib_packv5_041523_1651.root, FC#0, port C2

Entries	445
Mean	38.03
Std Dev	18.6

Turn on : 26.0513

Width : 2.597

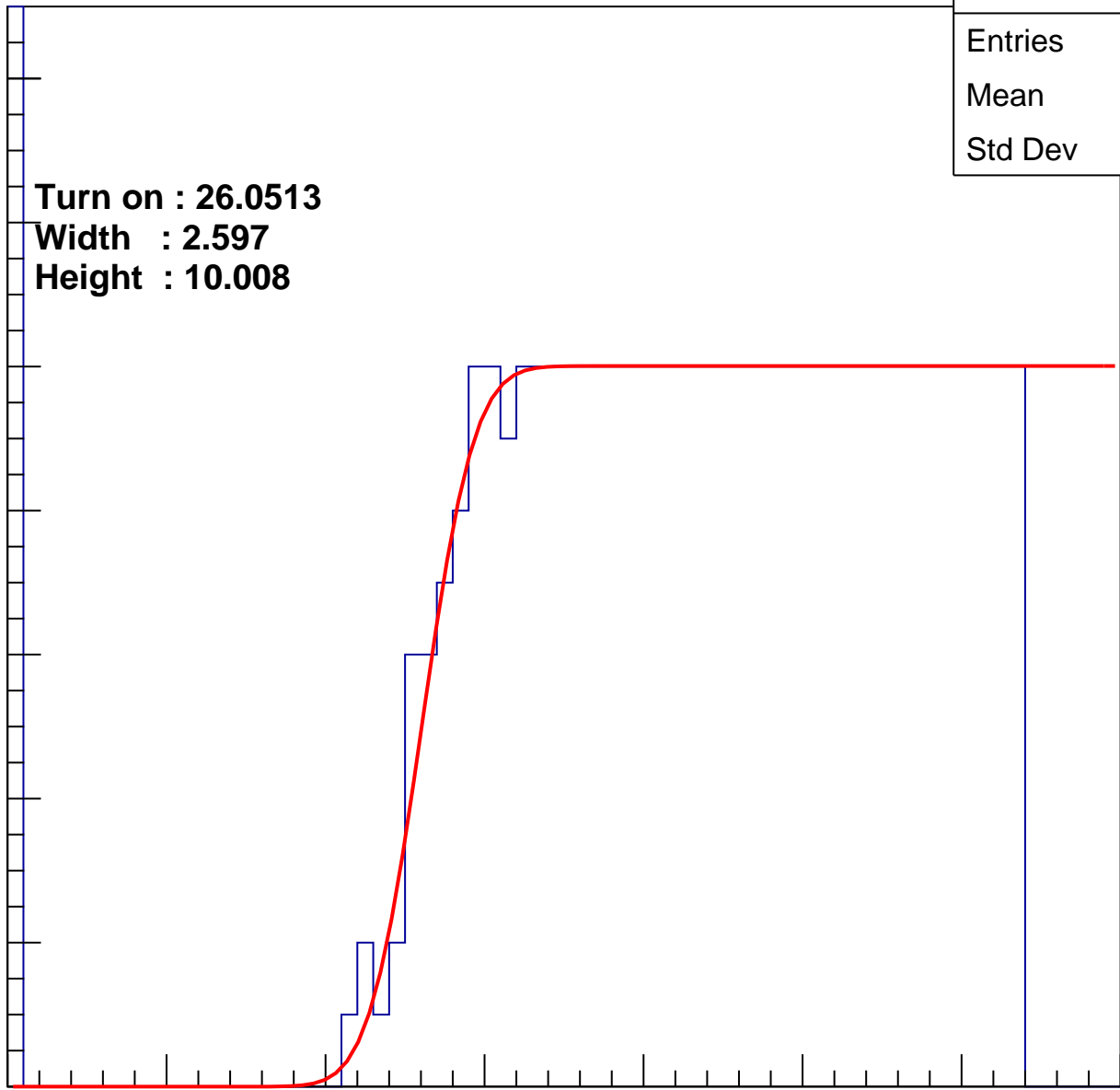
Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U3-ch94

calib_packv5_041523_1651.root, FC#0, port C2

Entries	417
Mean	39.61
Std Dev	17.81

Turn on : 27.7072

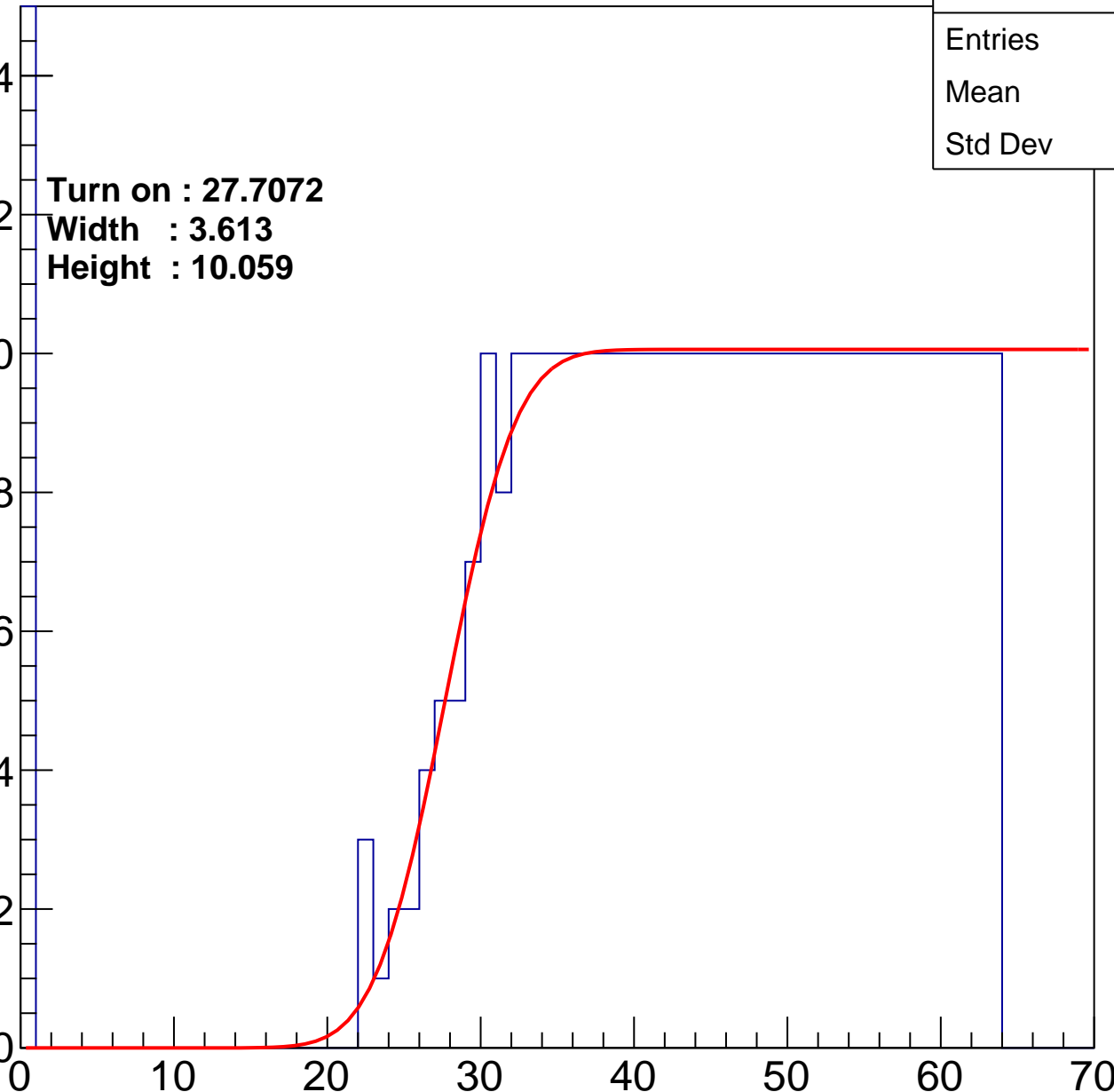
Width : 3.613

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch95

calib_packv5_041523_1651.root, FC#0, port C2

Entries	462
Mean	37.5
Std Dev	18.5

Turn on : 24.2479

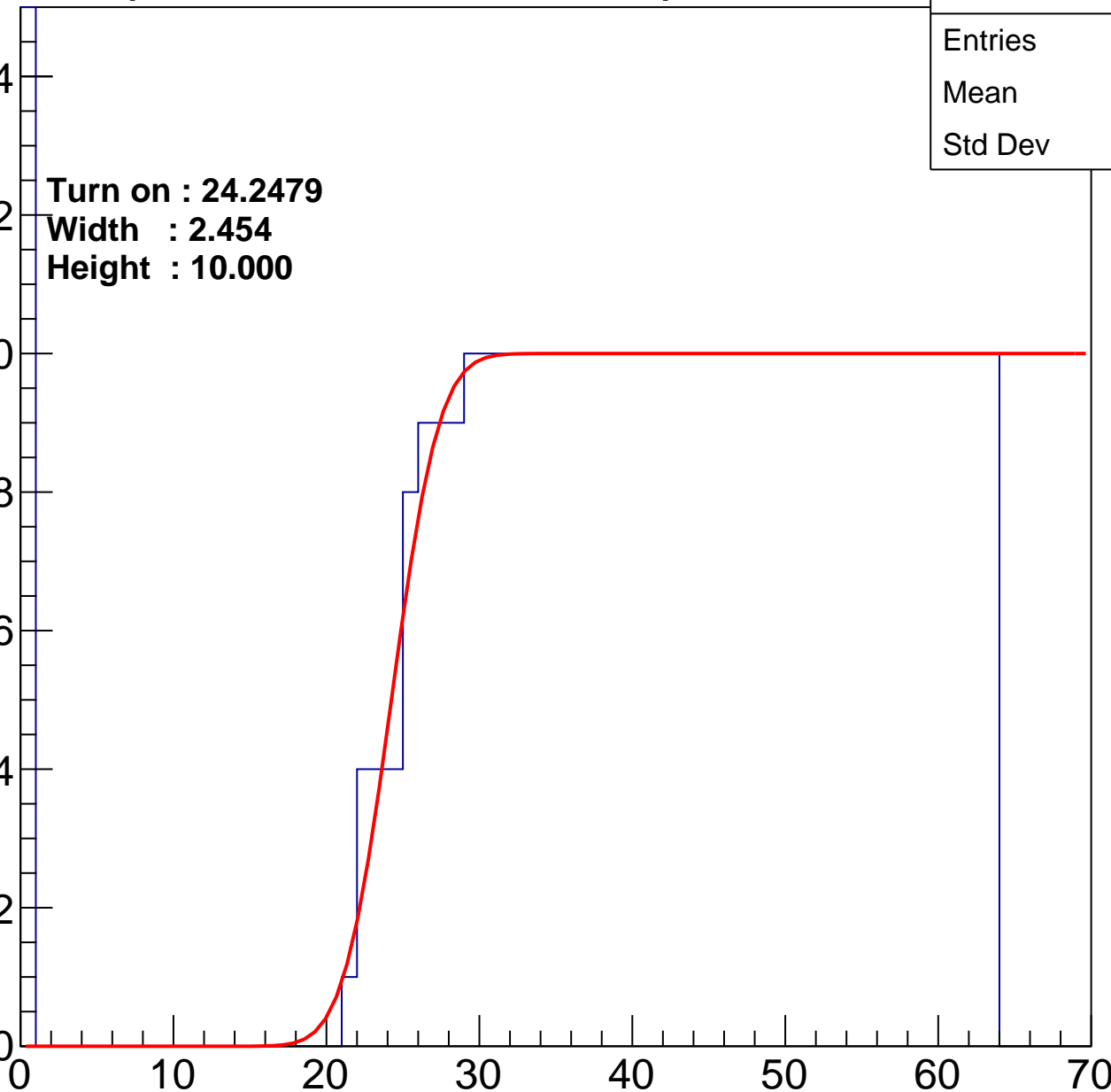
Width : 2.454

Height : 10.000

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch96

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	39.02
Std Dev	17.29

Turn on : 24.2216

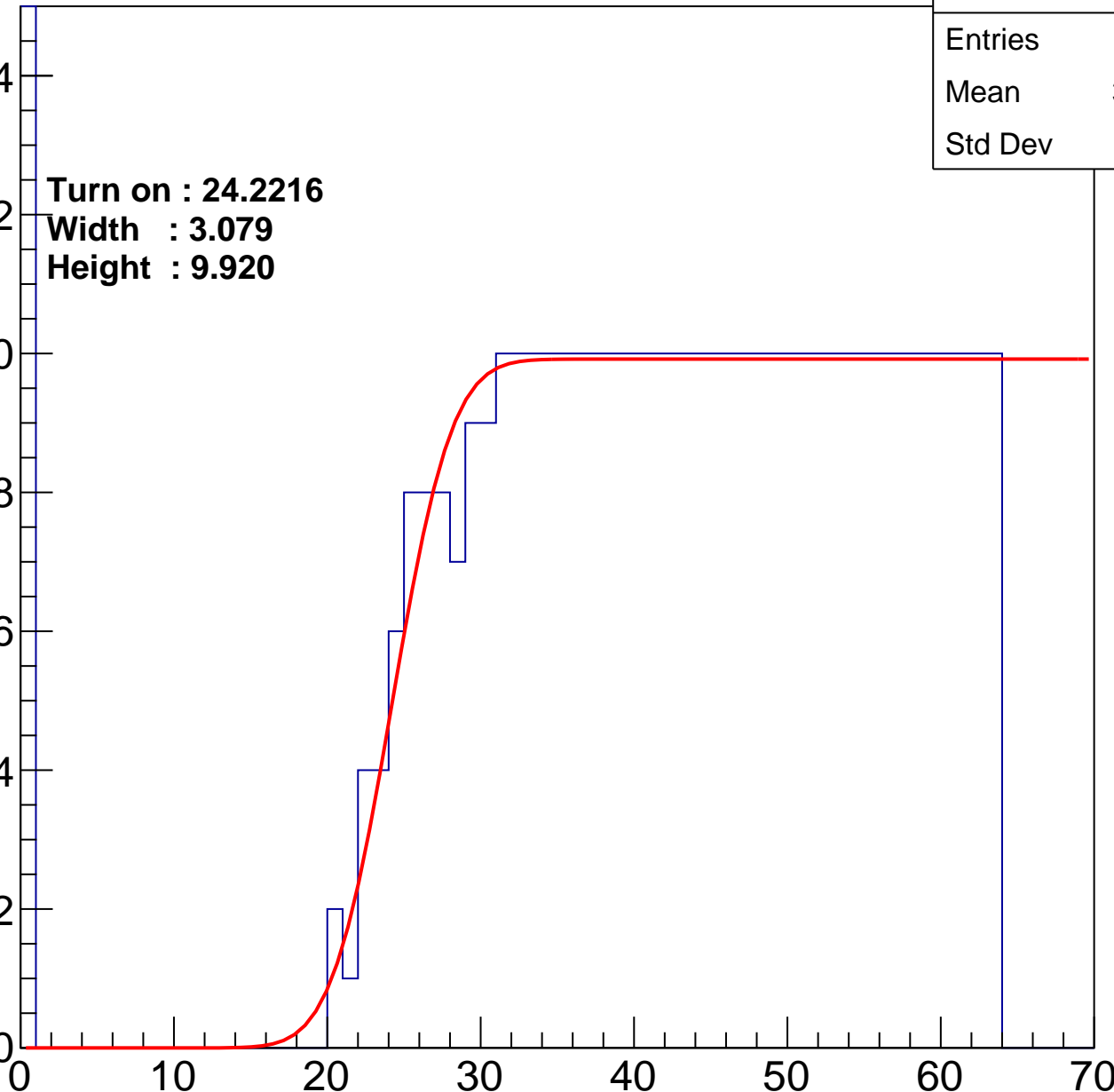
Width : 3.079

Height : 9.920

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch97

calib_packv5_041523_1651.root, FC#0, port C2

Entries	425
Mean	39.4
Std Dev	17.71

Turn on : 27.4821

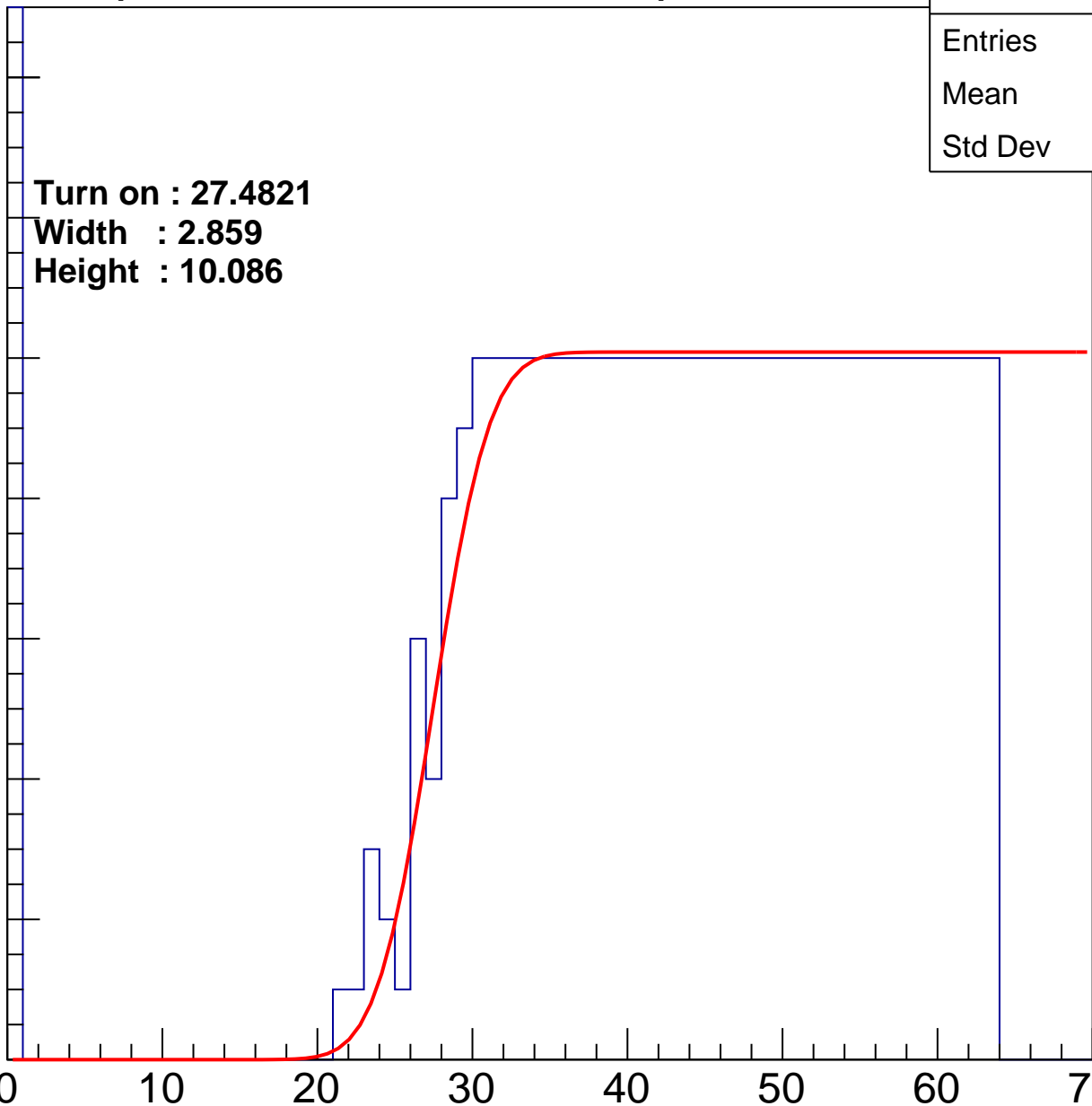
Width : 2.859

Height : 10.086

Entry

14
12
10
8
6
4
2
0

ampl

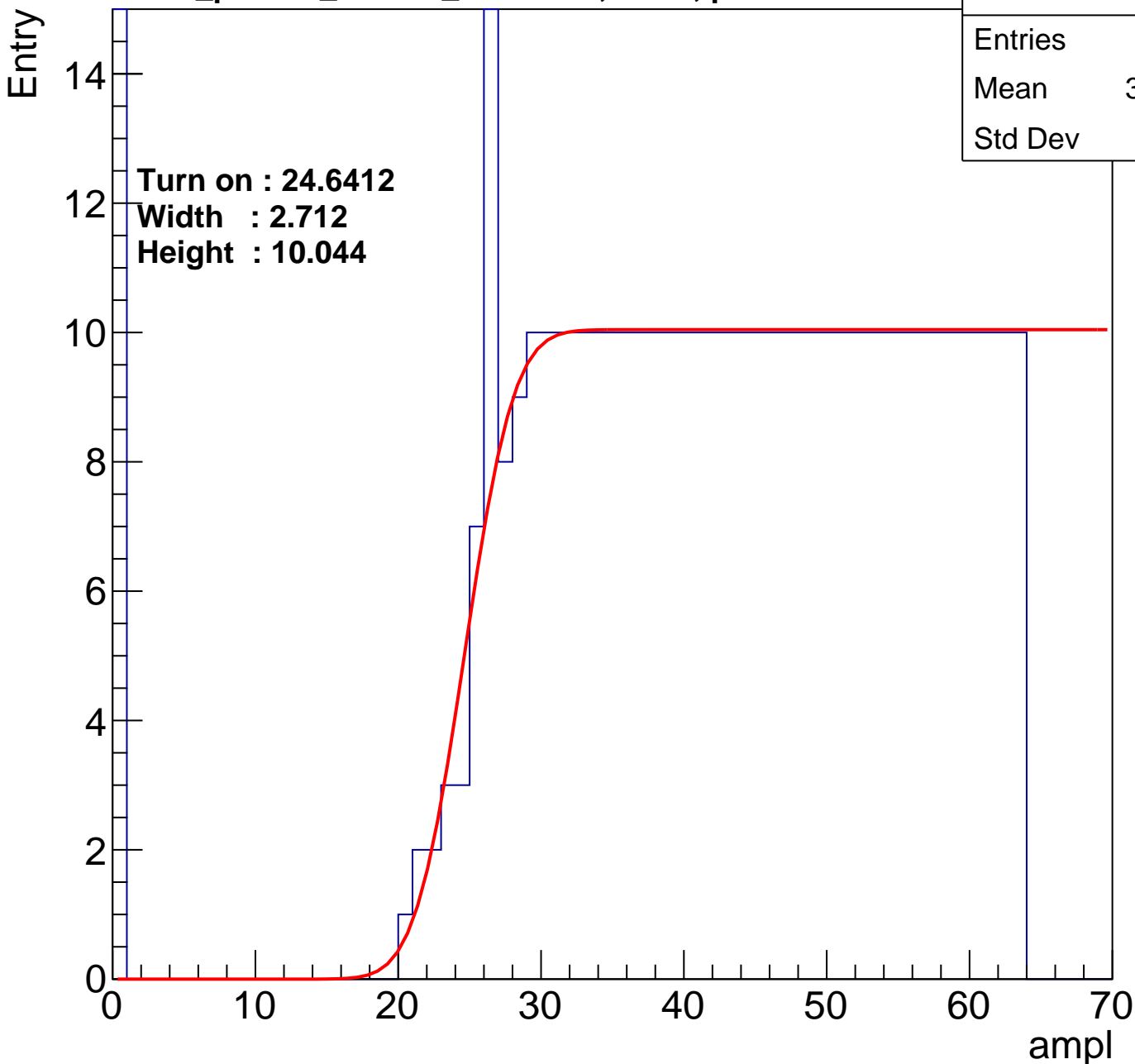


B1L103S, U3-ch98

calib_packv5_041523_1651.root, FC#0, port C2

Entries	451
Mean	38.59
Std Dev	17.5

Turn on : 24.6412
Width : 2.712
Height : 10.044



B1L103S, U3-ch99

calib_packv5_041523_1651.root, FC#0, port C2

Entries	452
Mean	37
Std Dev	19.61

Turn on : 27.0335

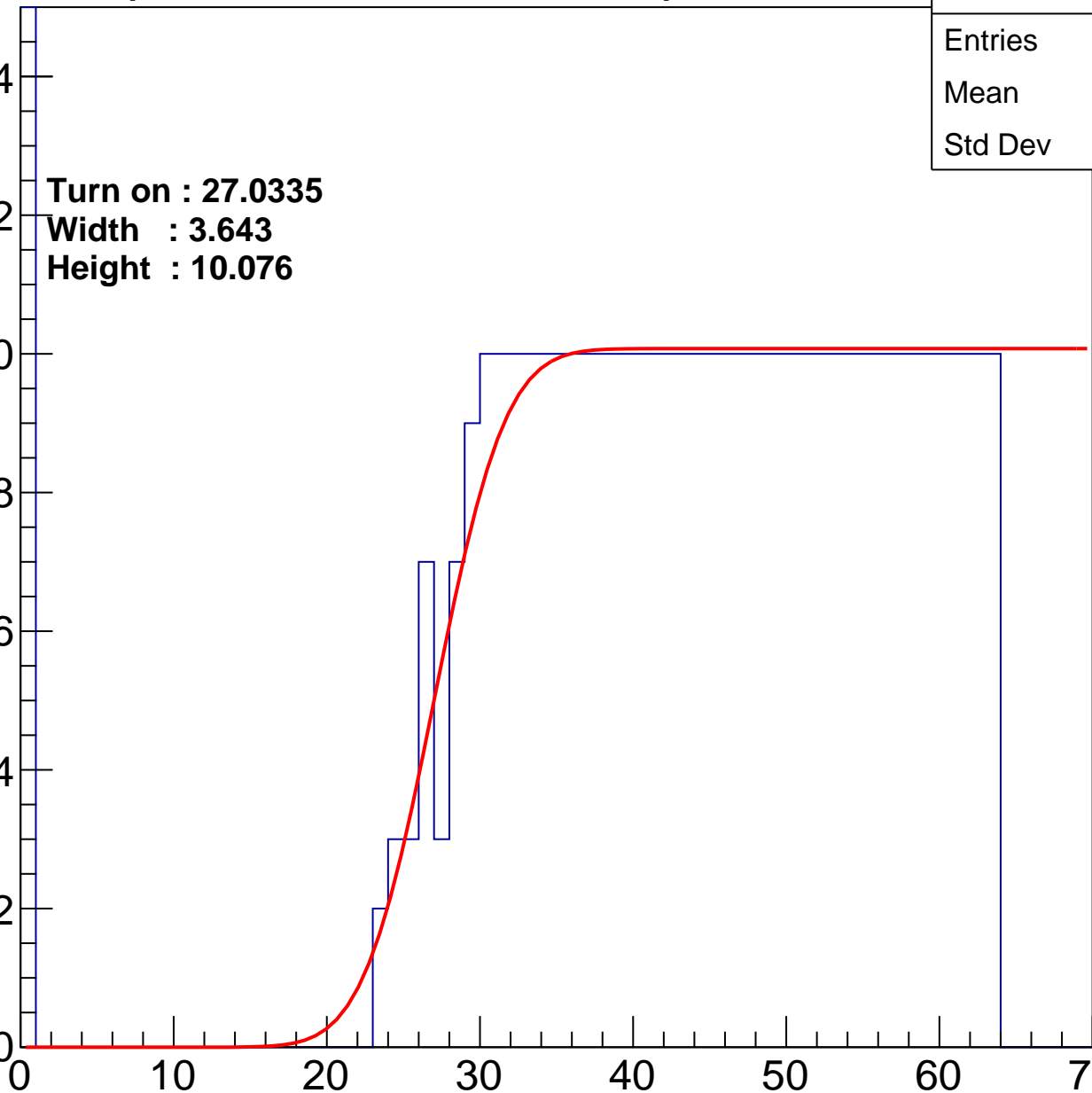
Width : 3.643

Height : 10.076

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch100

calib_packv5_041523_1651.root, FC#0, port C2

Entries	455
Mean	38.11
Std Dev	17.98

Turn on : 24.6006

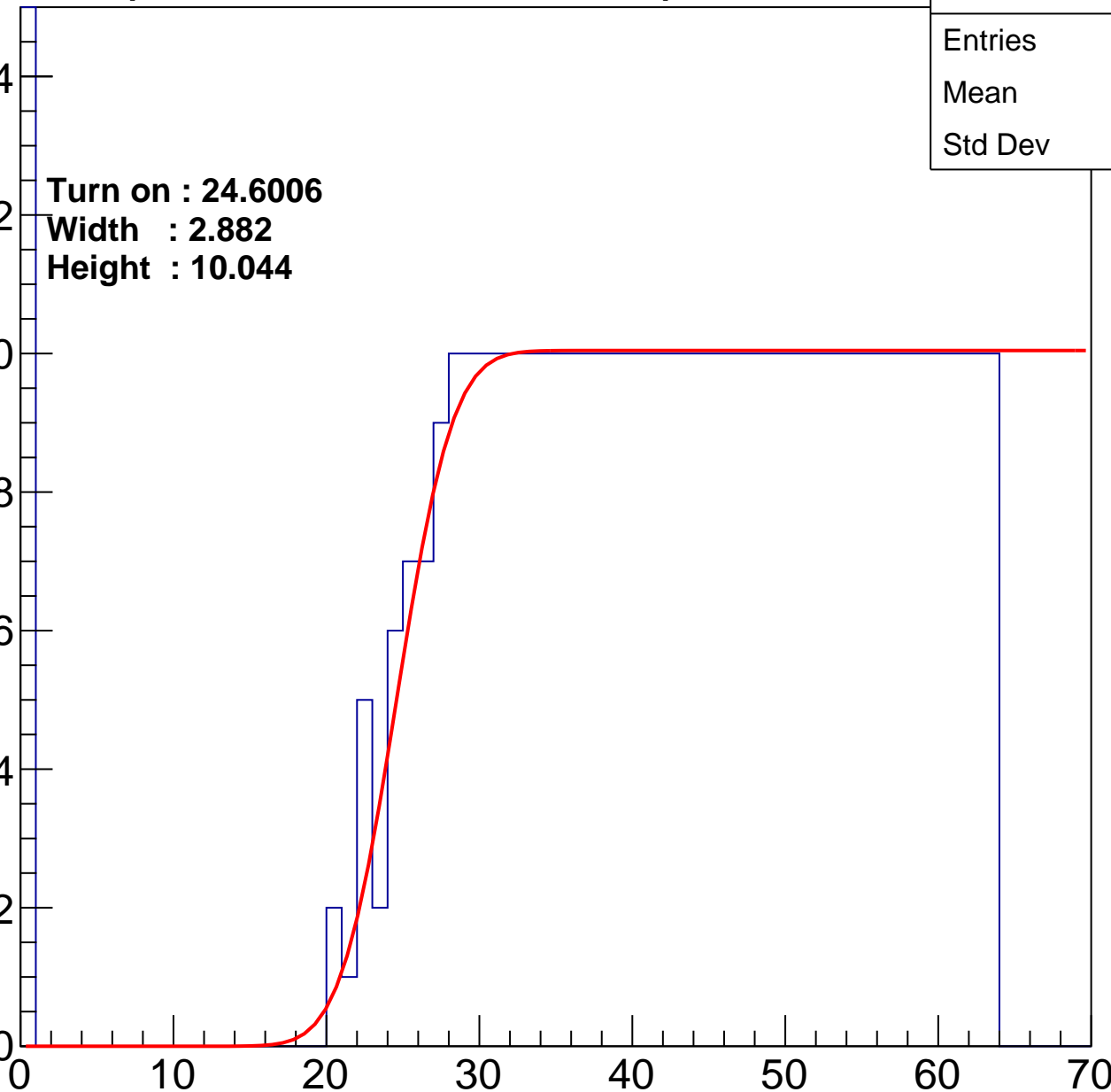
Width : 2.882

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch101

calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	38.94
Std Dev	17.92

Turn on : 26.4115

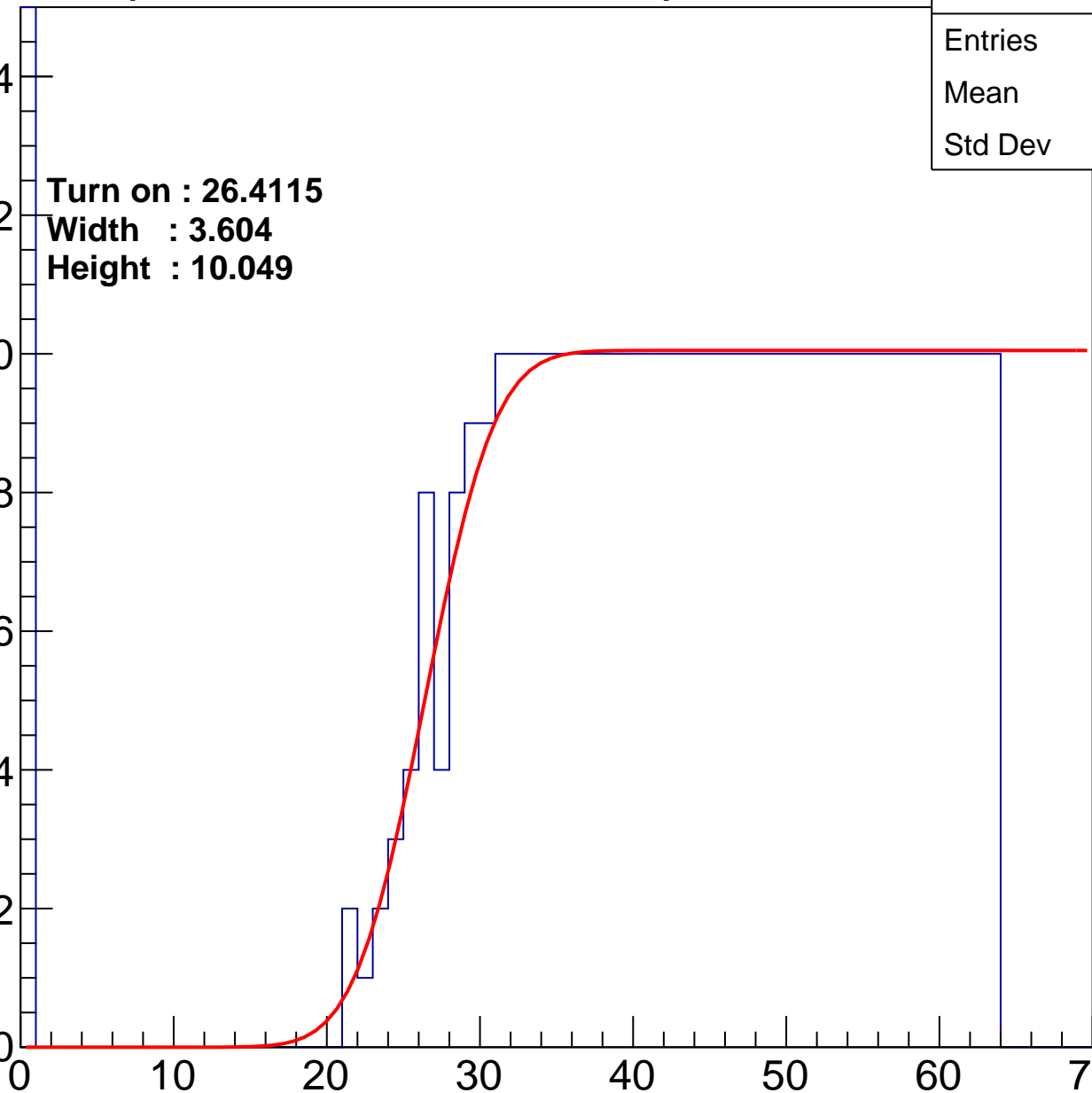
Width : 3.604

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch102

calib_packv5_041523_1651.root, FC#0, port C2

Entries	475
Mean	37.18
Std Dev	18.28

Turn on : 22.5454

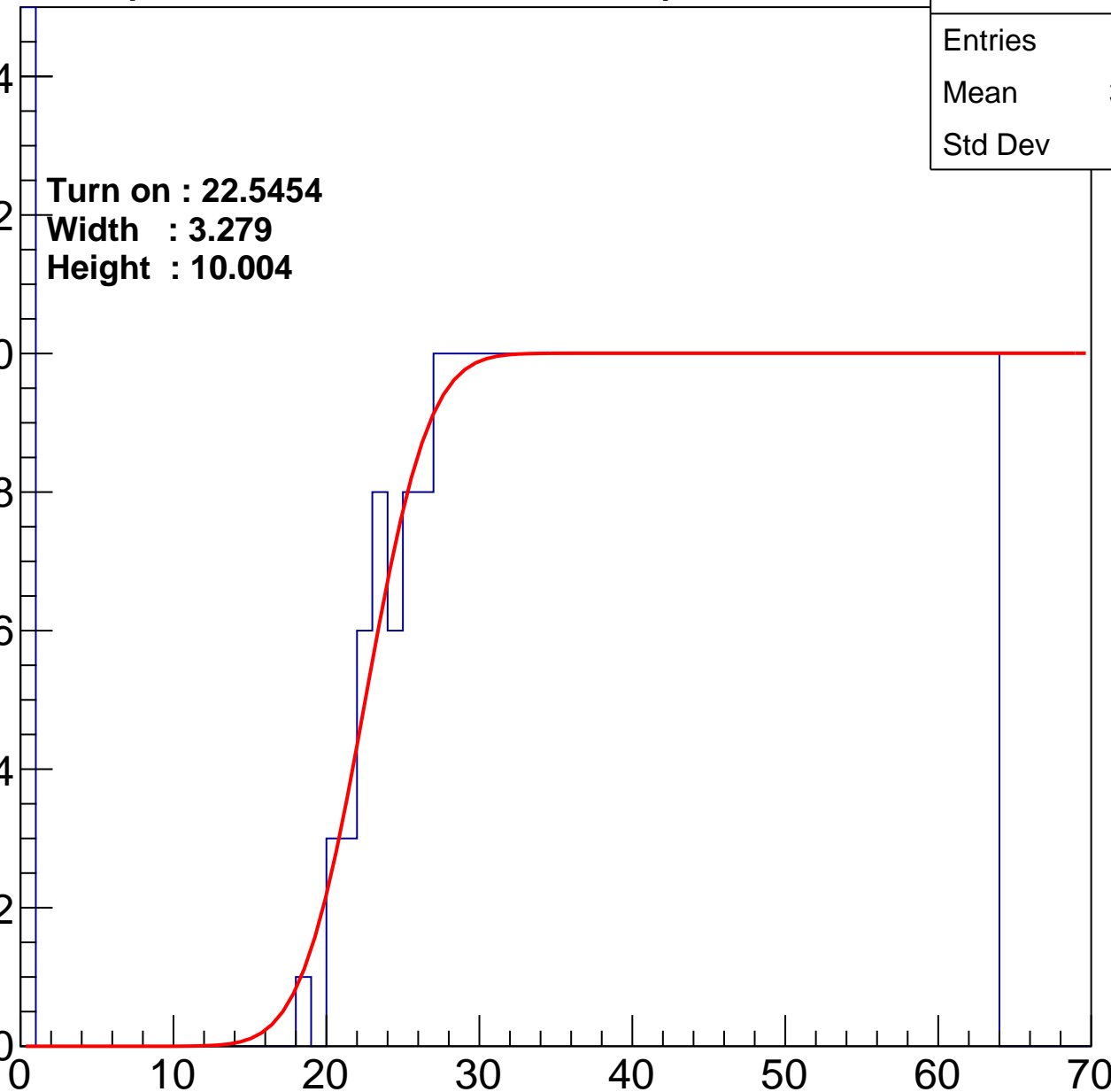
Width : 3.279

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch103

calib_packv5_041523_1651.root, FC#0, port C2

Entries	462
Mean	36.92
Std Dev	19.23

Turn on : 25.6755

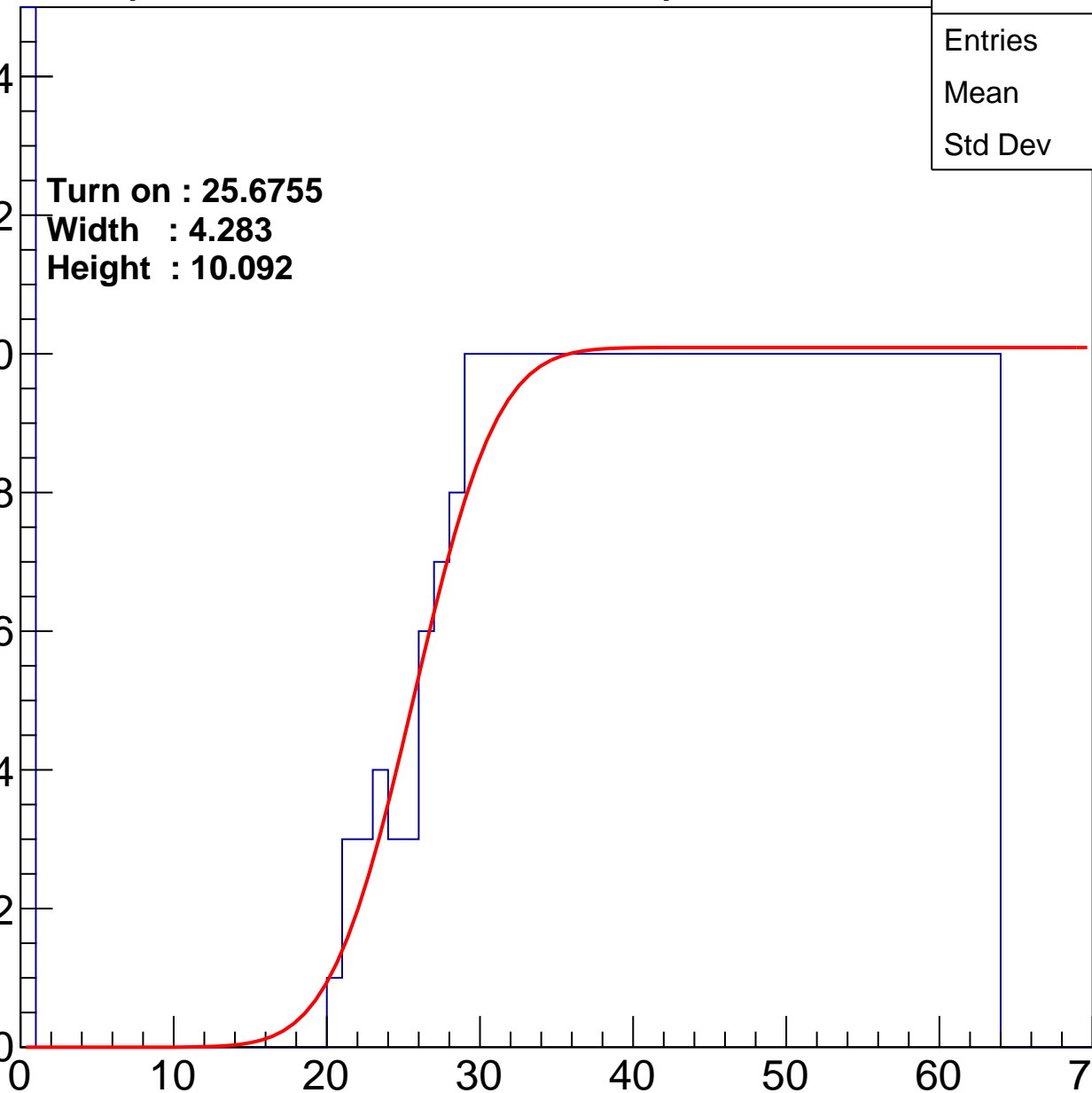
Width : 4.283

Height : 10.092

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch104

calib_packv5_041523_1651.root, FC#0, port C2

Entries	452
Mean	38.3
Std Dev	17.82

Turn on : 24.5335

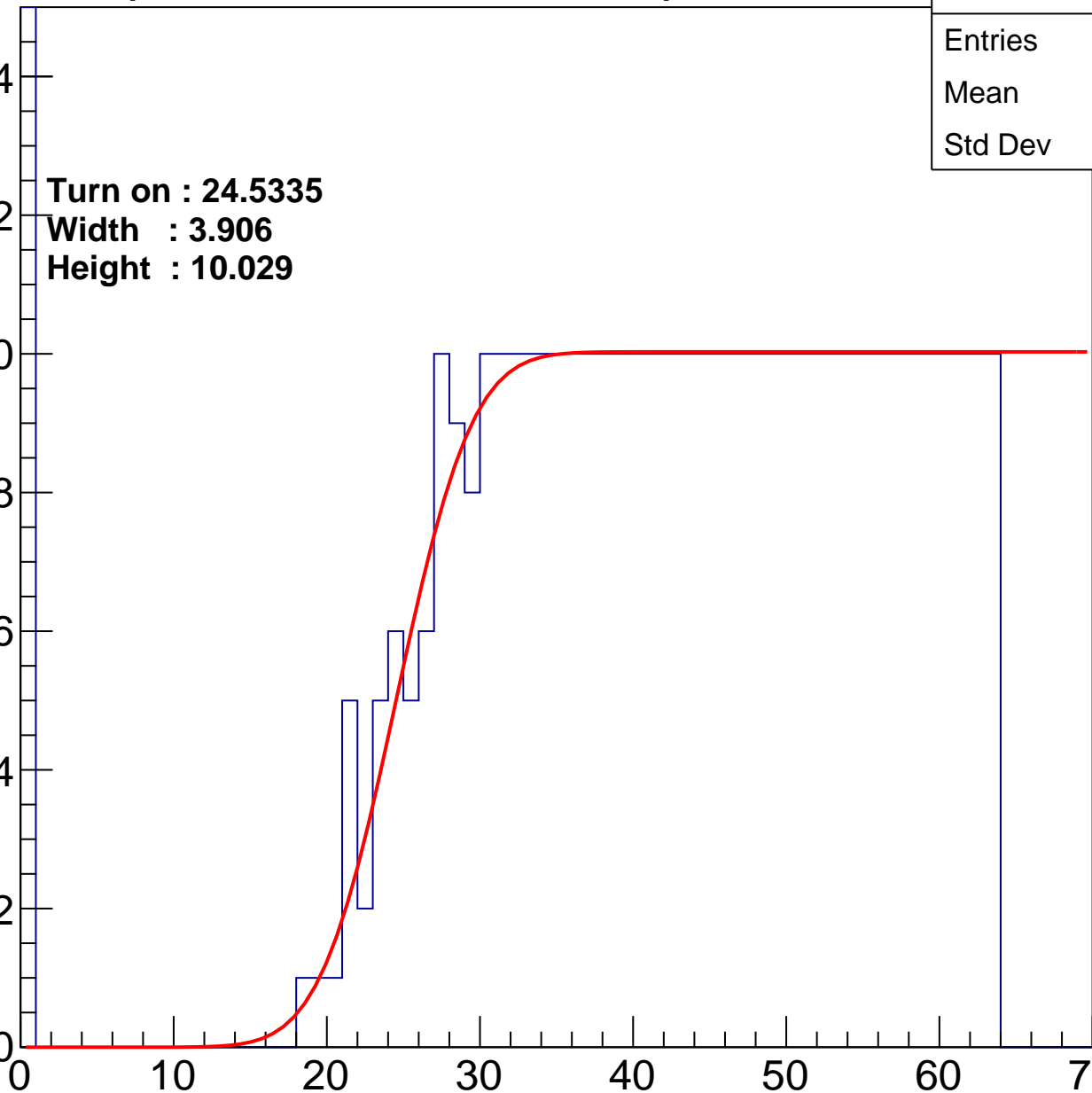
Width : 3.906

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch105

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	38.6
Std Dev	18.34

Turn on : 26.2003

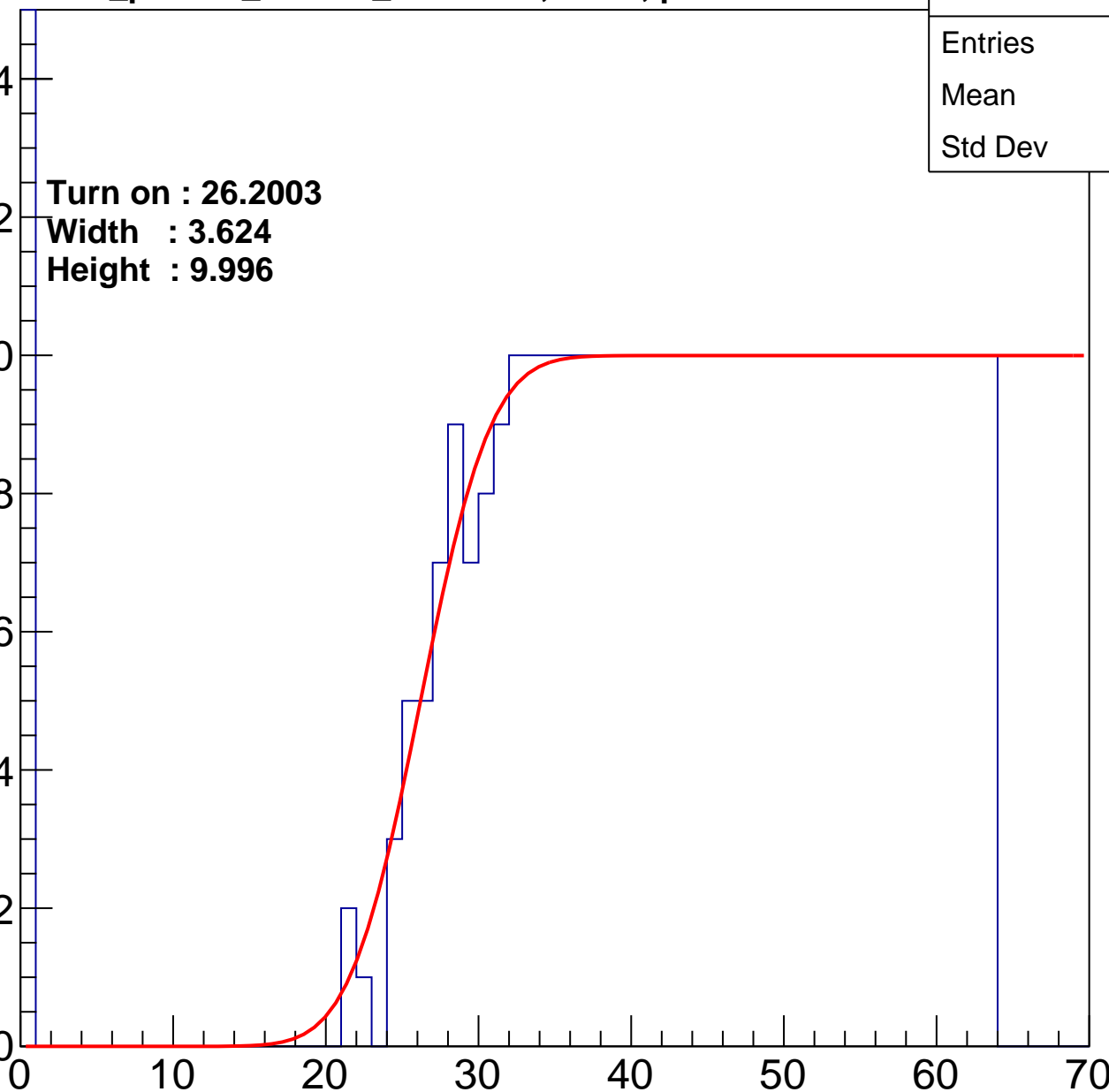
Width : 3.624

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch106

calib_packv5_041523_1651.root, FC#0, port C2

Entries	455
Mean	38.39
Std Dev	17.5

Turn on : 23.7760

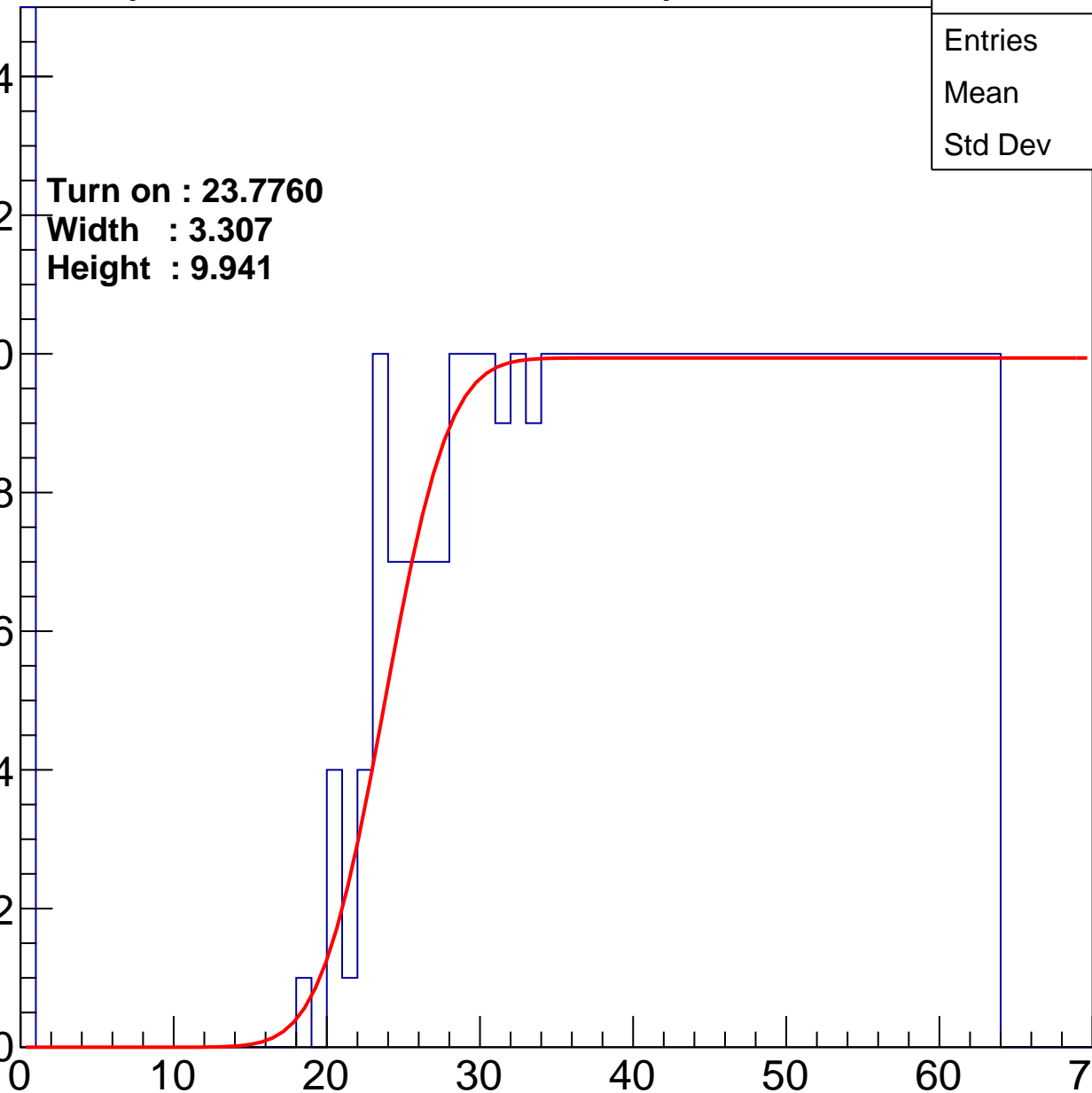
Width : 3.307

Height : 9.941

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch107

calib_packv5_041523_1651.root, FC#0, port C2

Entries	425
Mean	39.54
Std Dev	17.47

Turn on : 26.8095

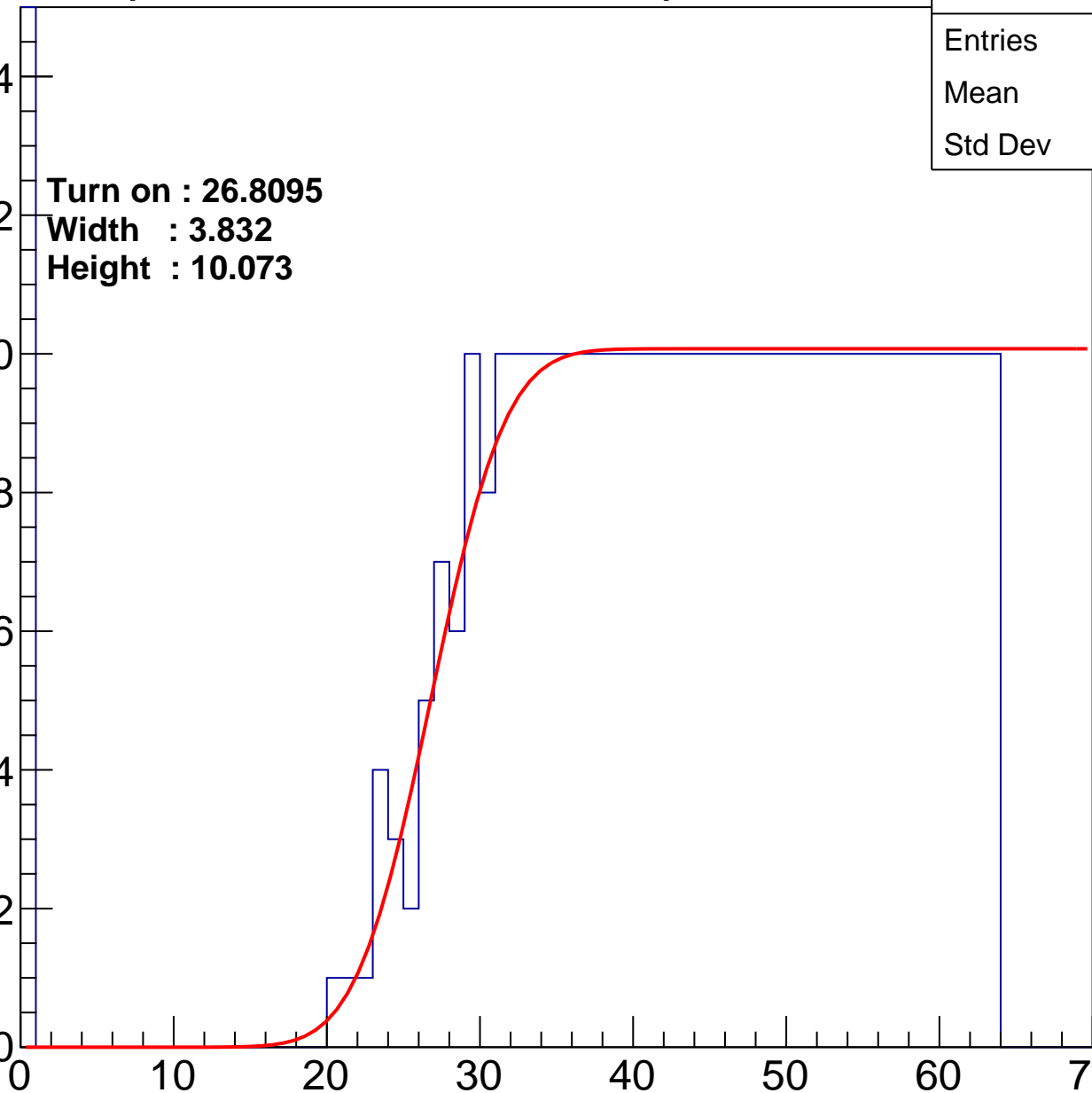
Width : 3.832

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch108

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	39.23
Std Dev	17.17

Turn on : 25.0302

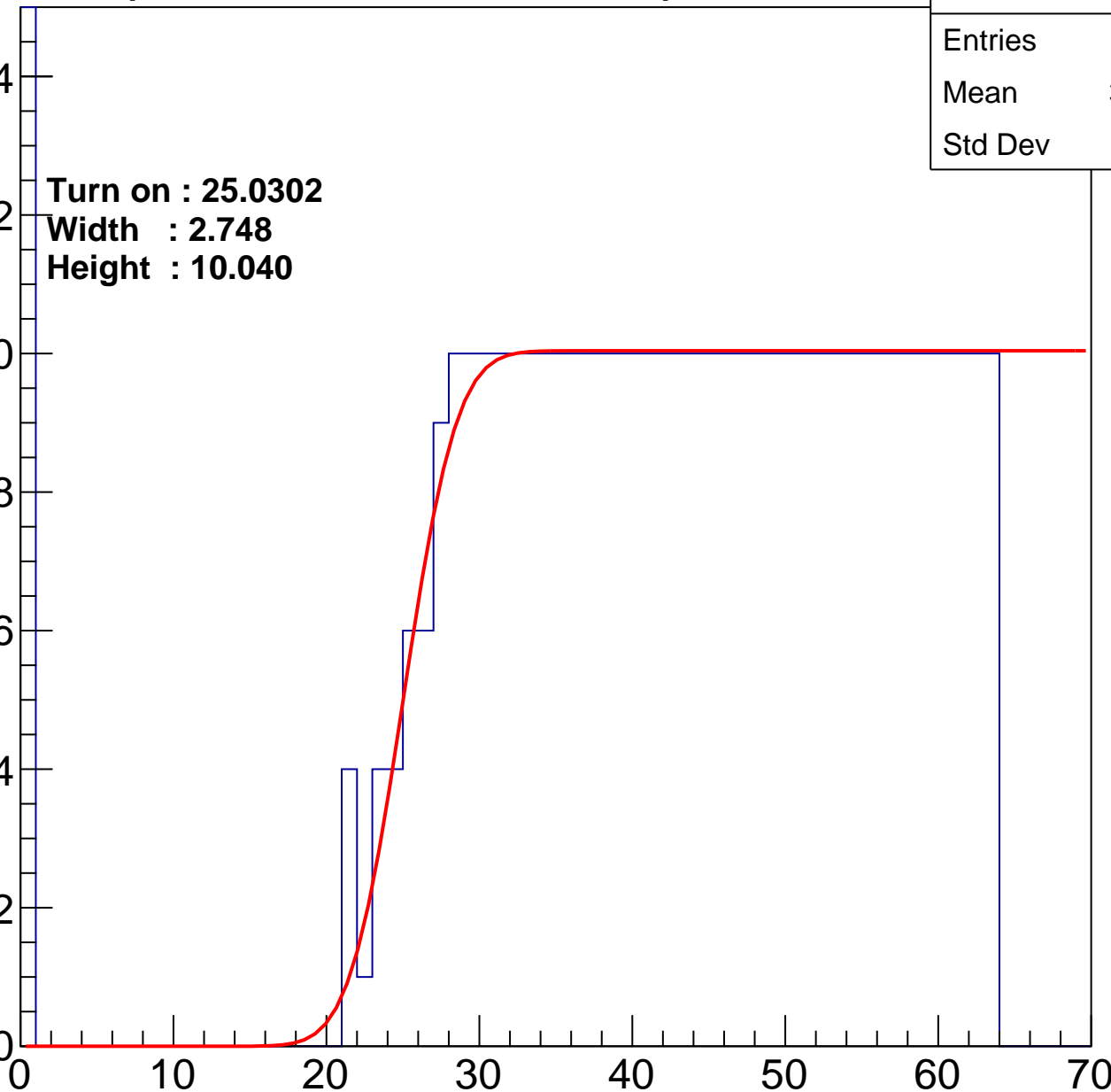
Width : 2.748

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch109

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	39.57
Std Dev	17.14

Turn on : 25.3641

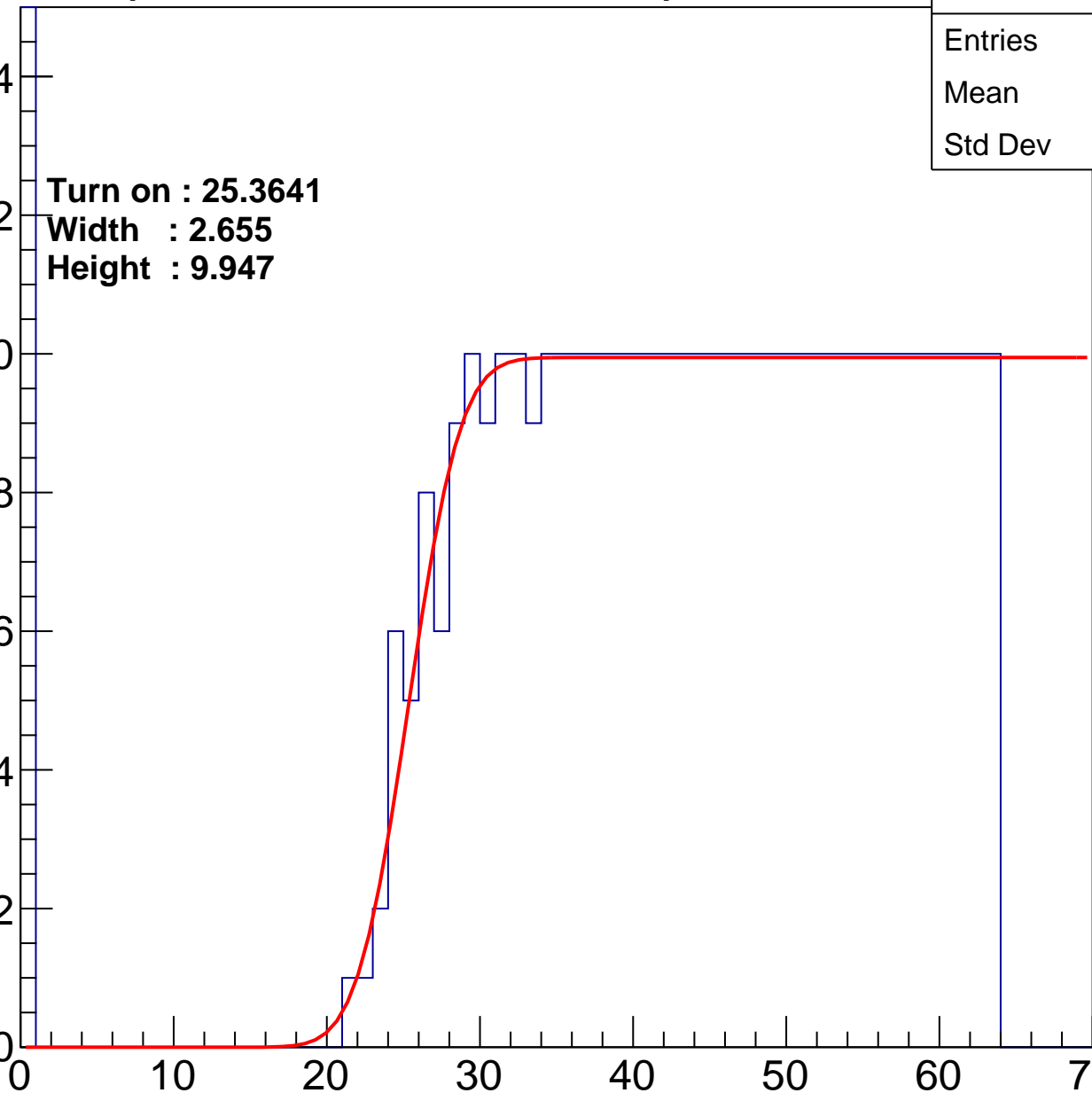
Width : 2.655

Height : 9.947

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch110

calib_packv5_041523_1651.root, FC#0, port C2

Entries	452
Mean	38.55
Std Dev	17.47

Turn on : 23.8987

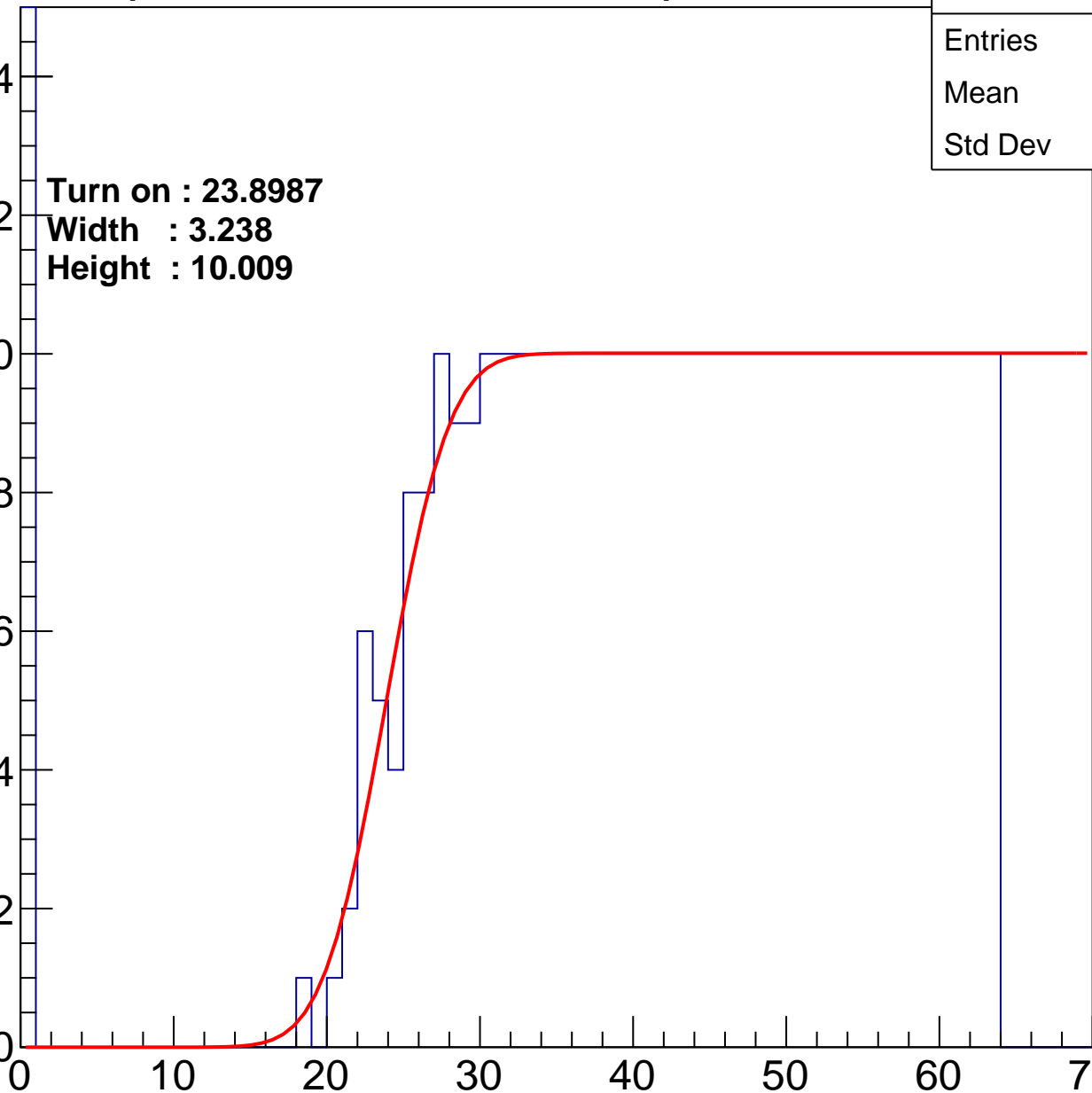
Width : 3.238

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch111

calib_packv5_041523_1651.root, FC#0, port C2

Entries	463
Mean	37.11
Std Dev	18.91

Turn on : 24.7761

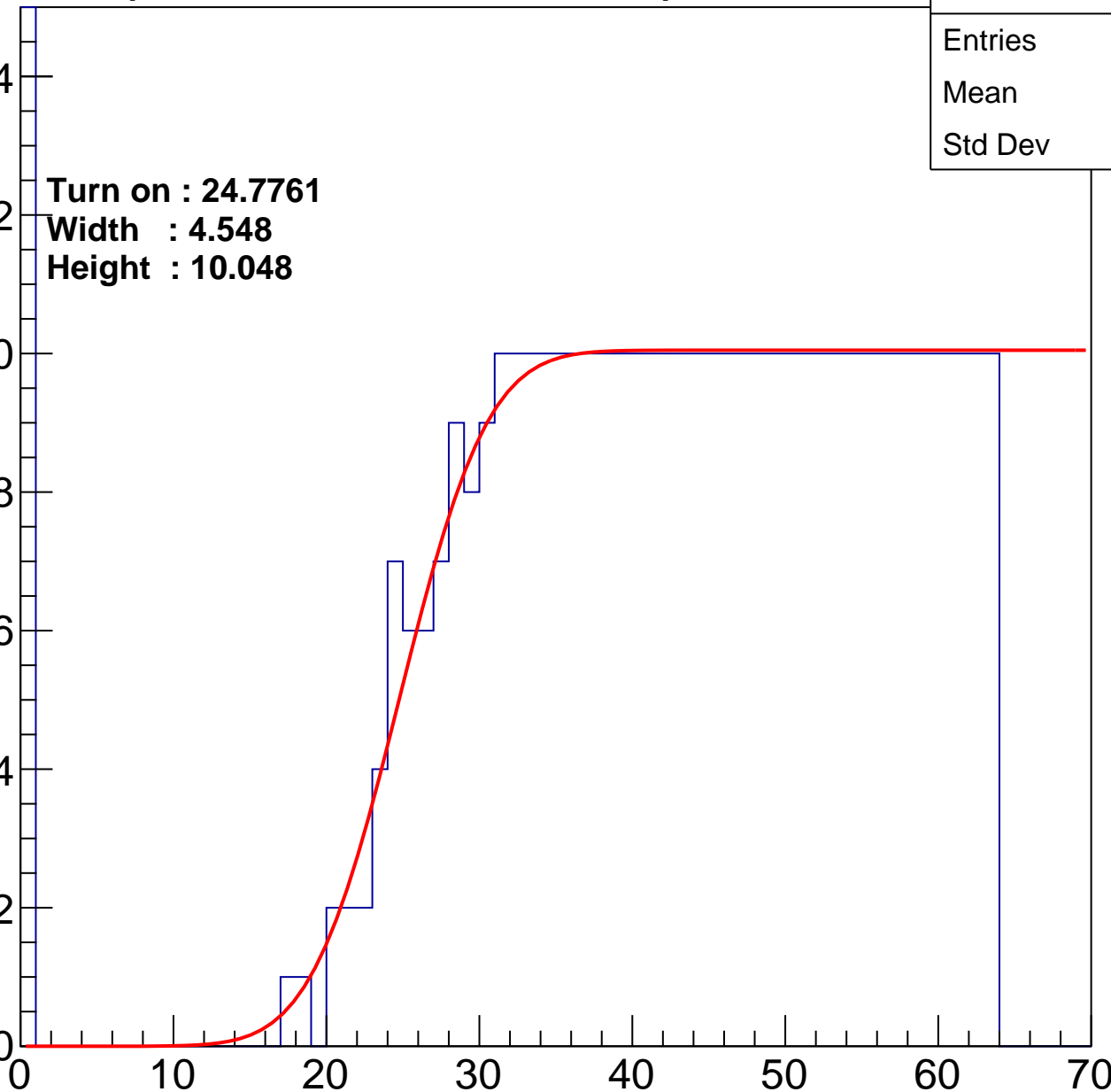
Width : 4.548

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch112

calib_packv5_041523_1651.root, FC#0, port C2

Entries	452
Mean	38.28
Std Dev	17.87

Turn on : 23.9315

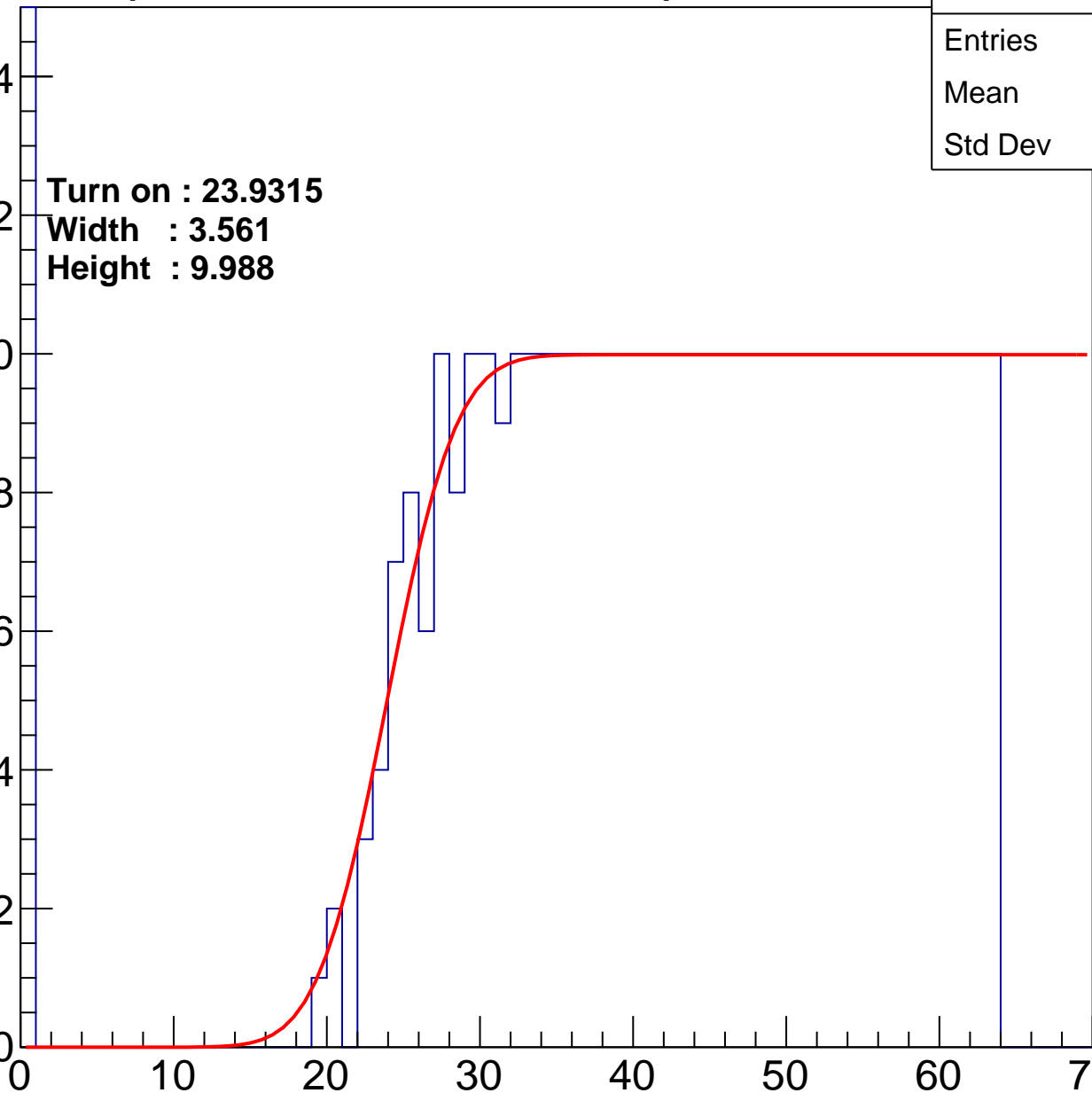
Width : 3.561

Height : 9.988

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch113

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	38.76
Std Dev	18.68

Turn on : 27.9493

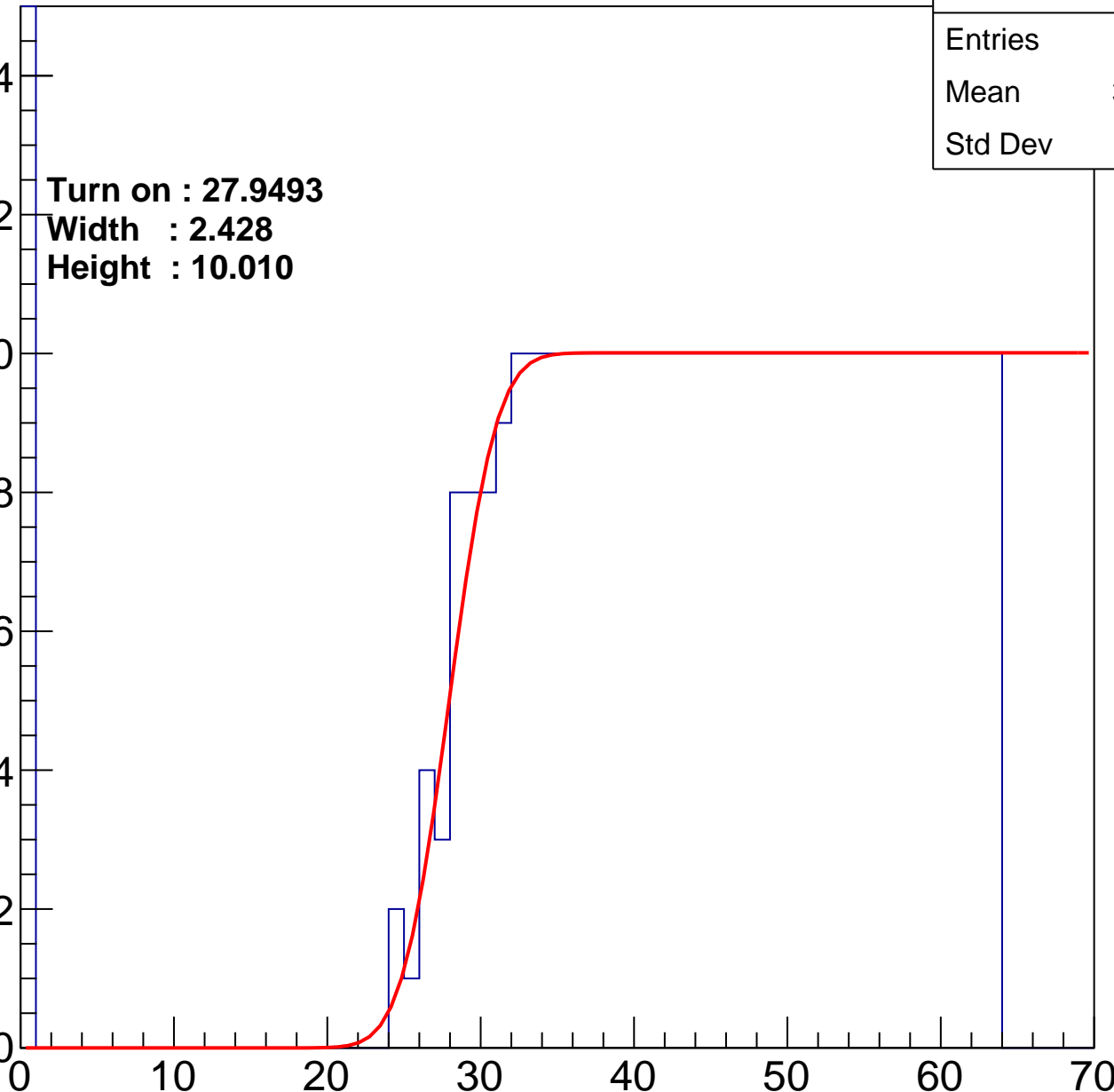
Width : 2.428

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch114

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	39.54
Std Dev	17.17

Turn on : 25.1667

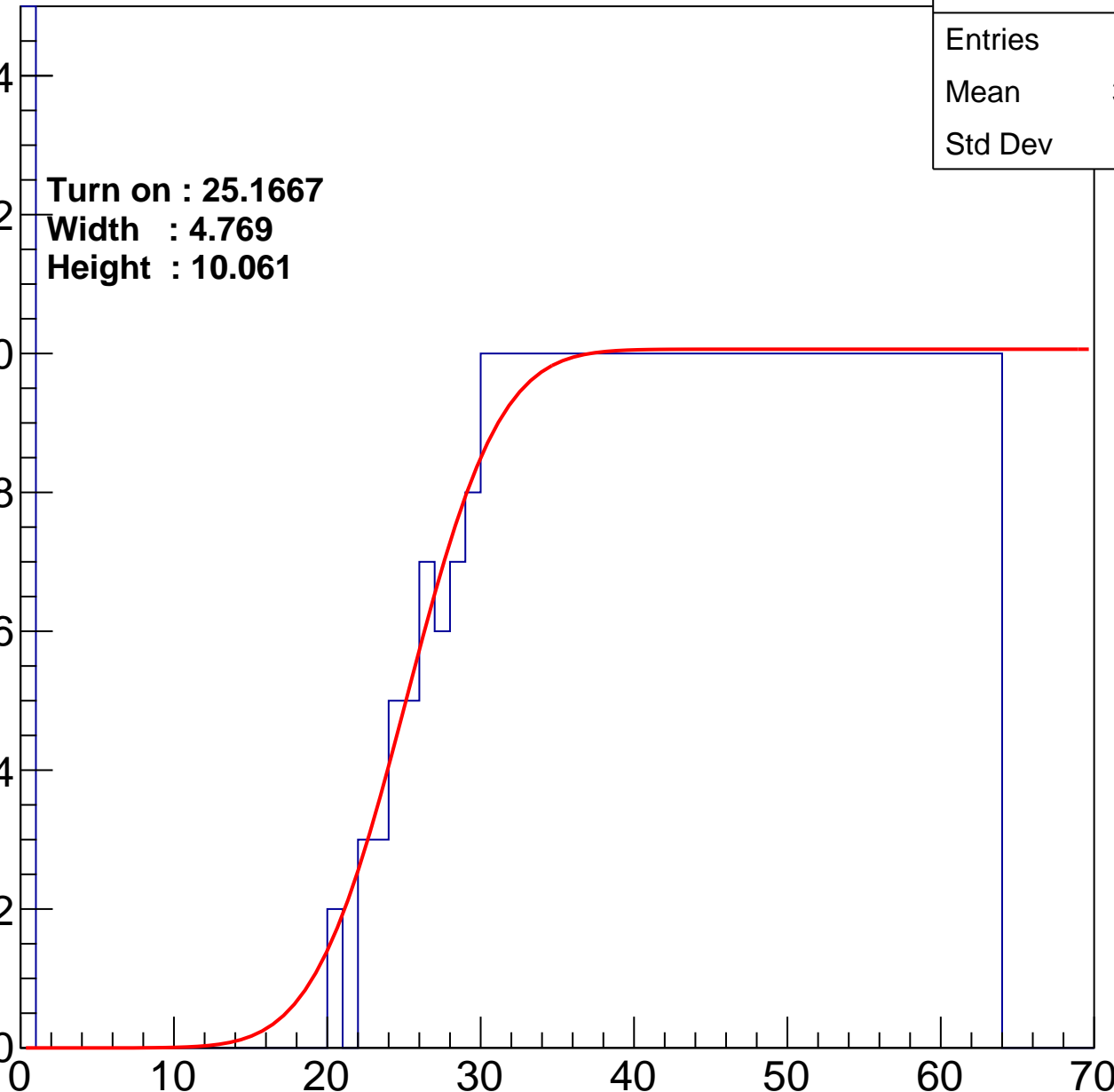
Width : 4.769

Height : 10.061

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch115

calib_packv5_041523_1651.root, FC#0, port C2

Entries	473
Mean	36.66
Std Dev	19.08

Turn on : 24.2497

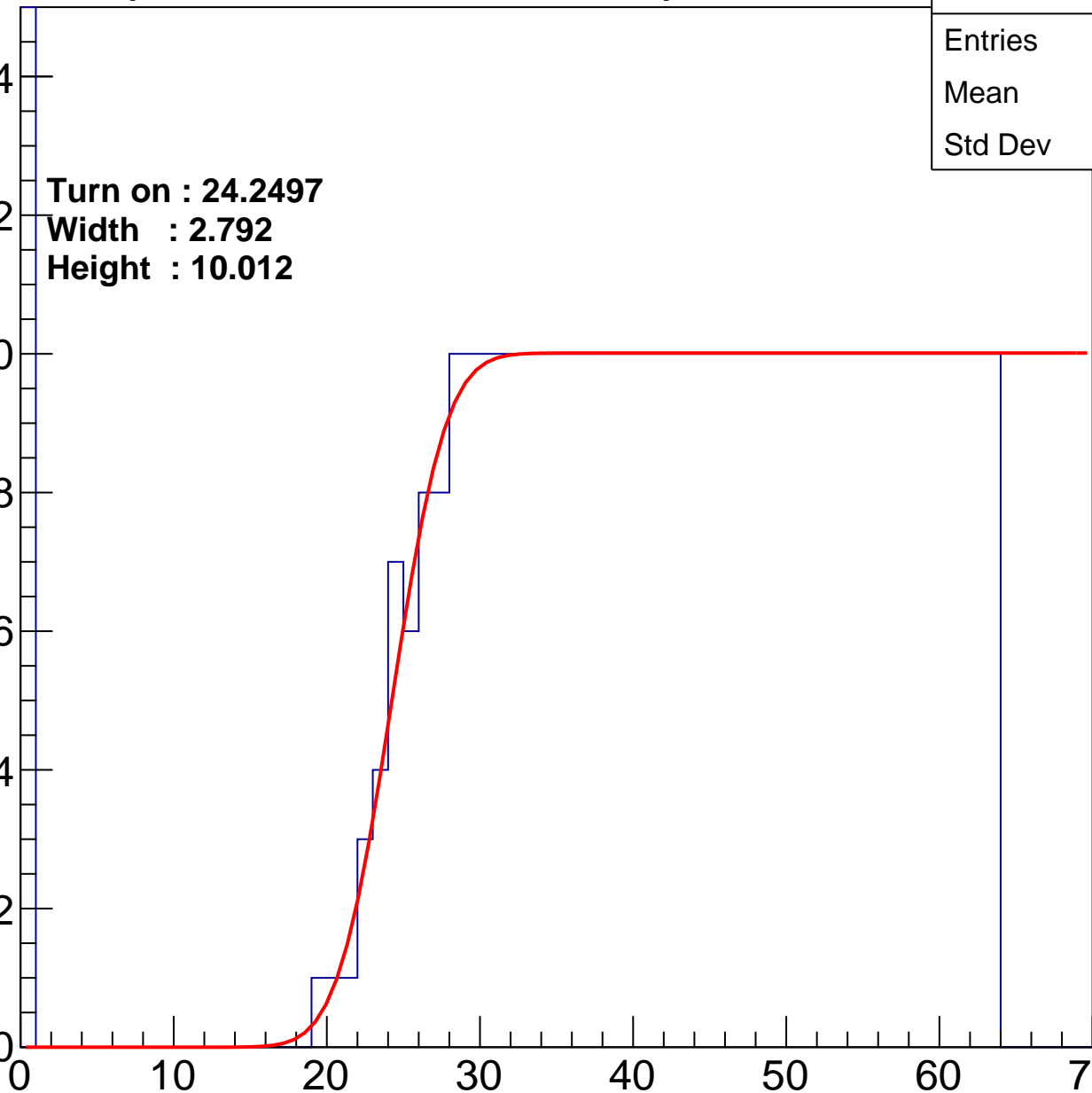
Width : 2.792

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch116

calib_packv5_041523_1651.root, FC#0, port C2

Entries	455
Mean	37.65
Std Dev	18.6

Turn on : 25.3315

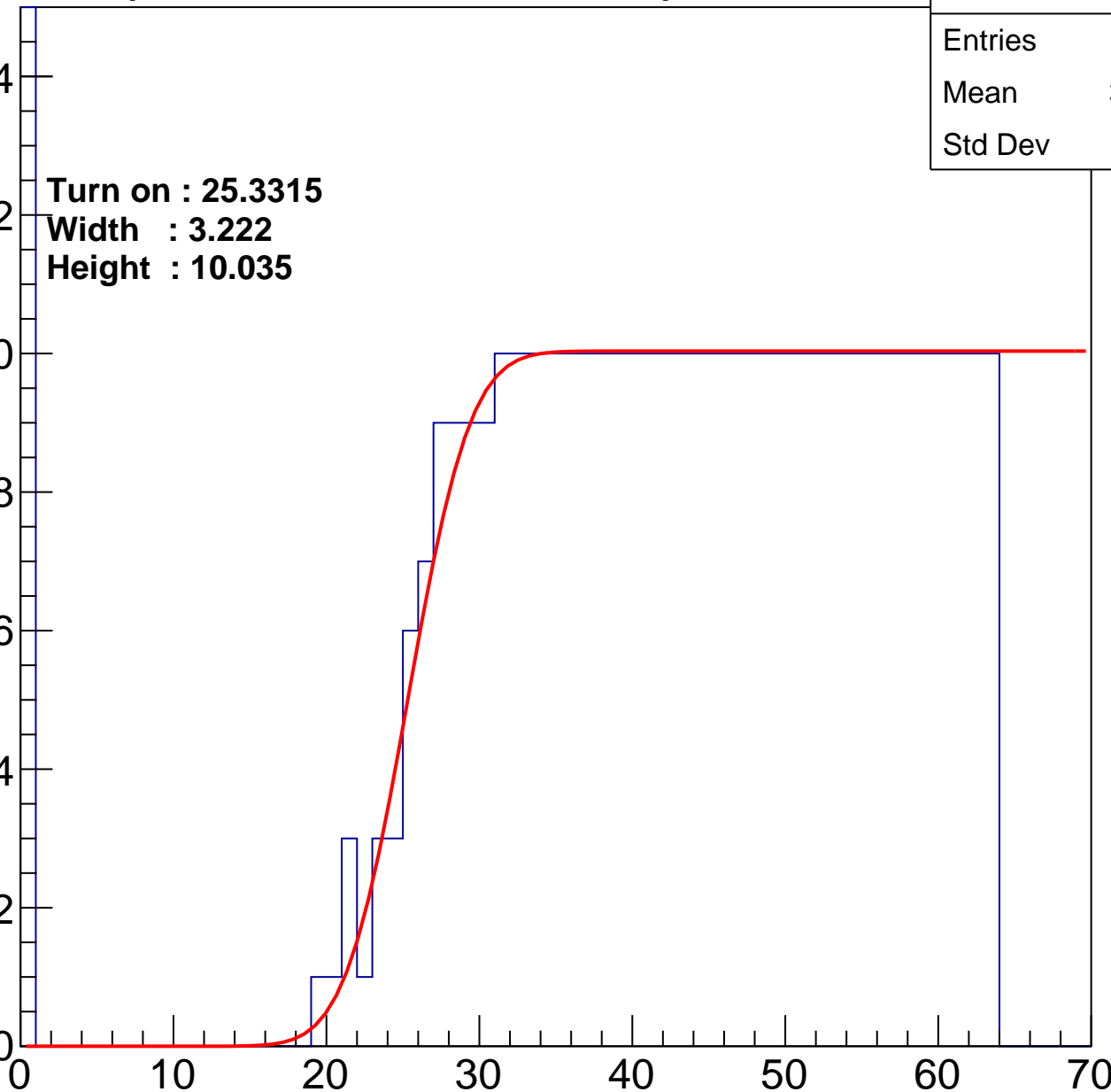
Width : 3.222

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch117

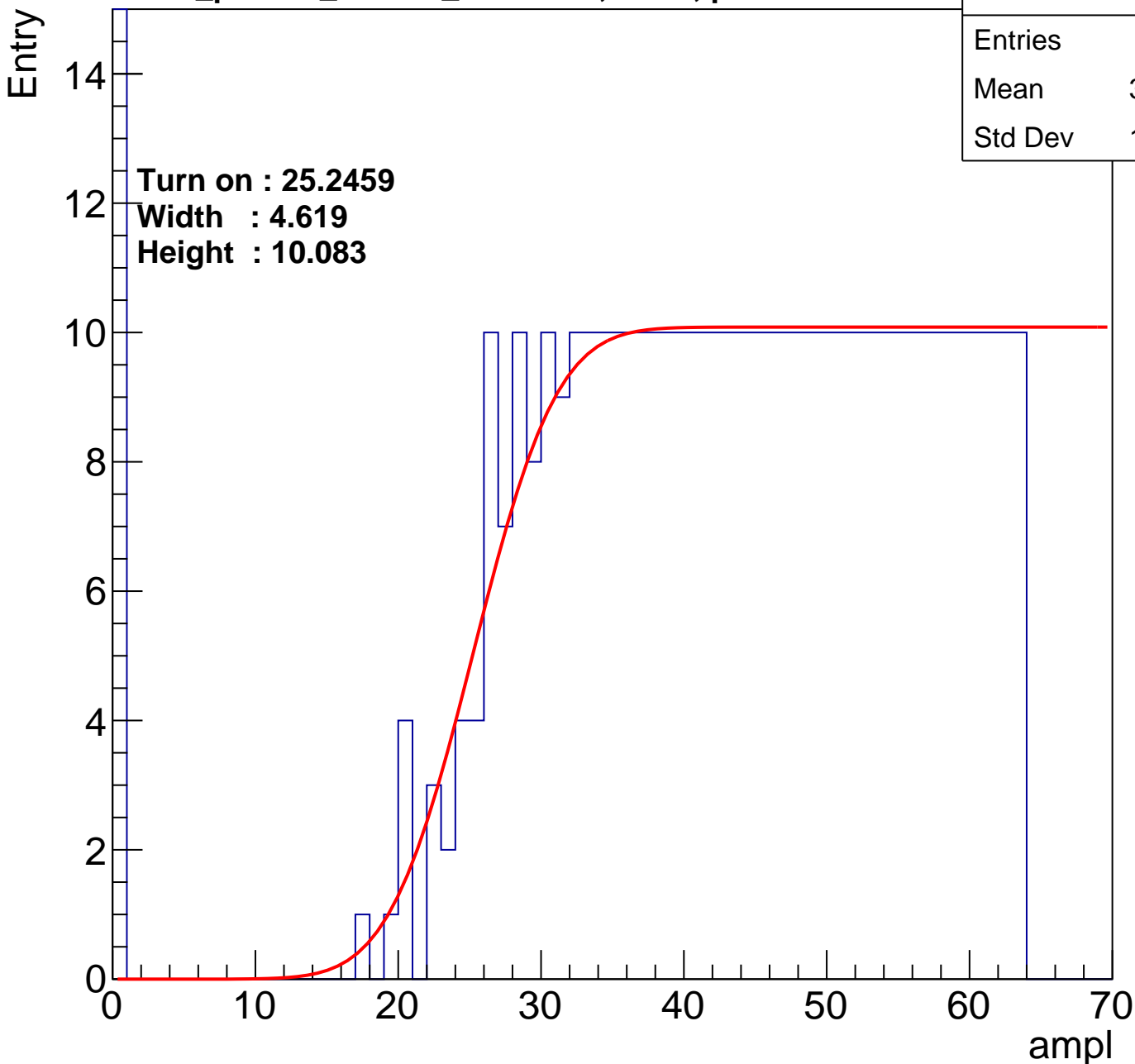
calib_packv5_041523_1651.root, FC#0, port C2

Entries	450
Mean	38.14
Std Dev	18.15

Turn on : 25.2459

Width : 4.619

Height : 10.083



B1L103S, U3-ch118

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	39.56
Std Dev	17.75

Turn on : 27.1043

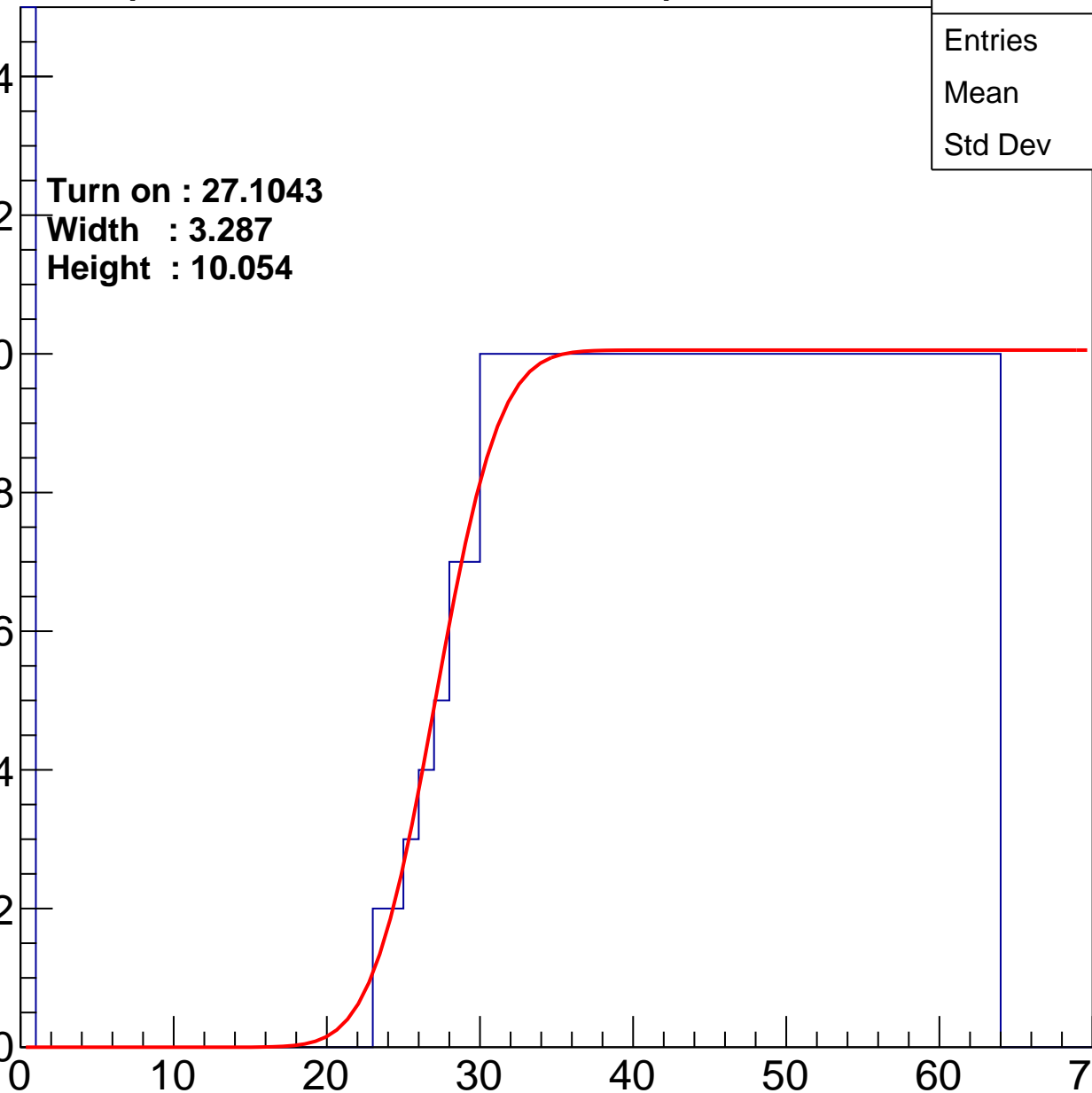
Width : 3.287

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch119

calib_packv5_041523_1651.root, FC#0, port C2

Entries	447
Mean	38.26
Std Dev	18.15

Turn on : 25.6329

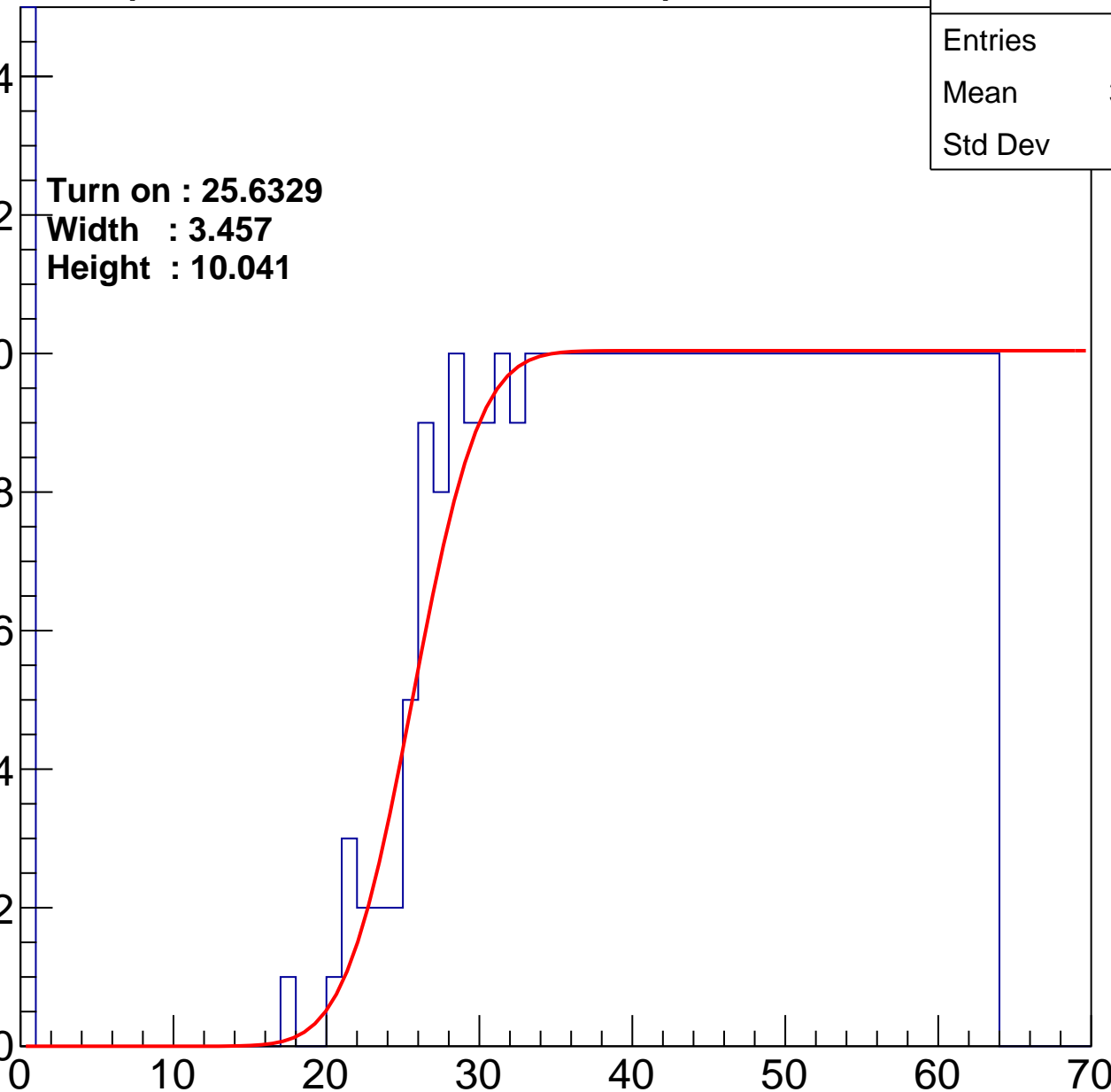
Width : 3.457

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch120

calib_packv5_041523_1651.root, FC#0, port C2

Entries	460
Mean	38.6
Std Dev	16.93

Turn on : 22.5502

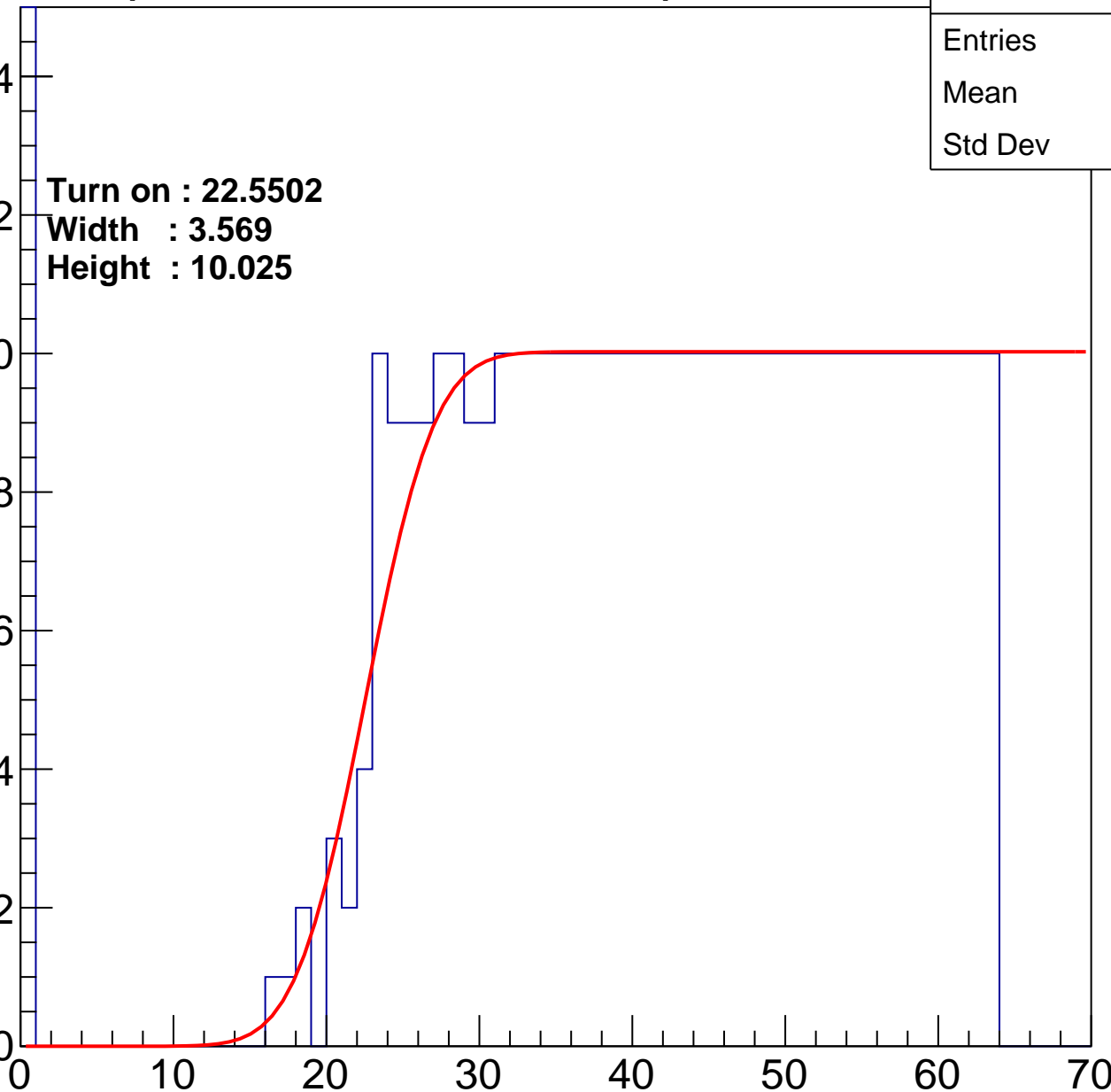
Width : 3.569

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch121

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	38.19
Std Dev	18.71

Turn on : 26.6209

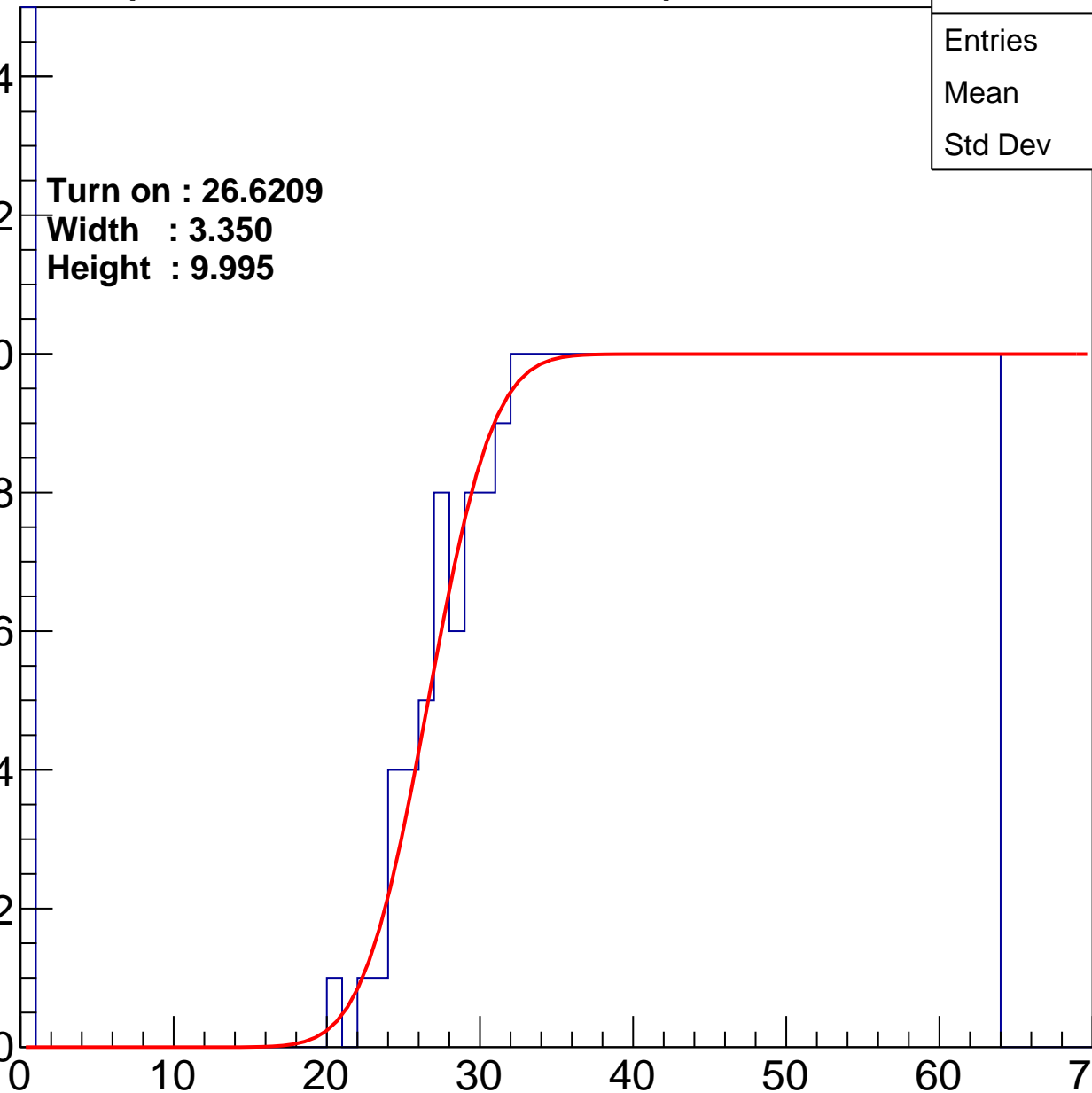
Width : 3.350

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch122

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	39.65
Std Dev	17.48

Turn on : 26.7425

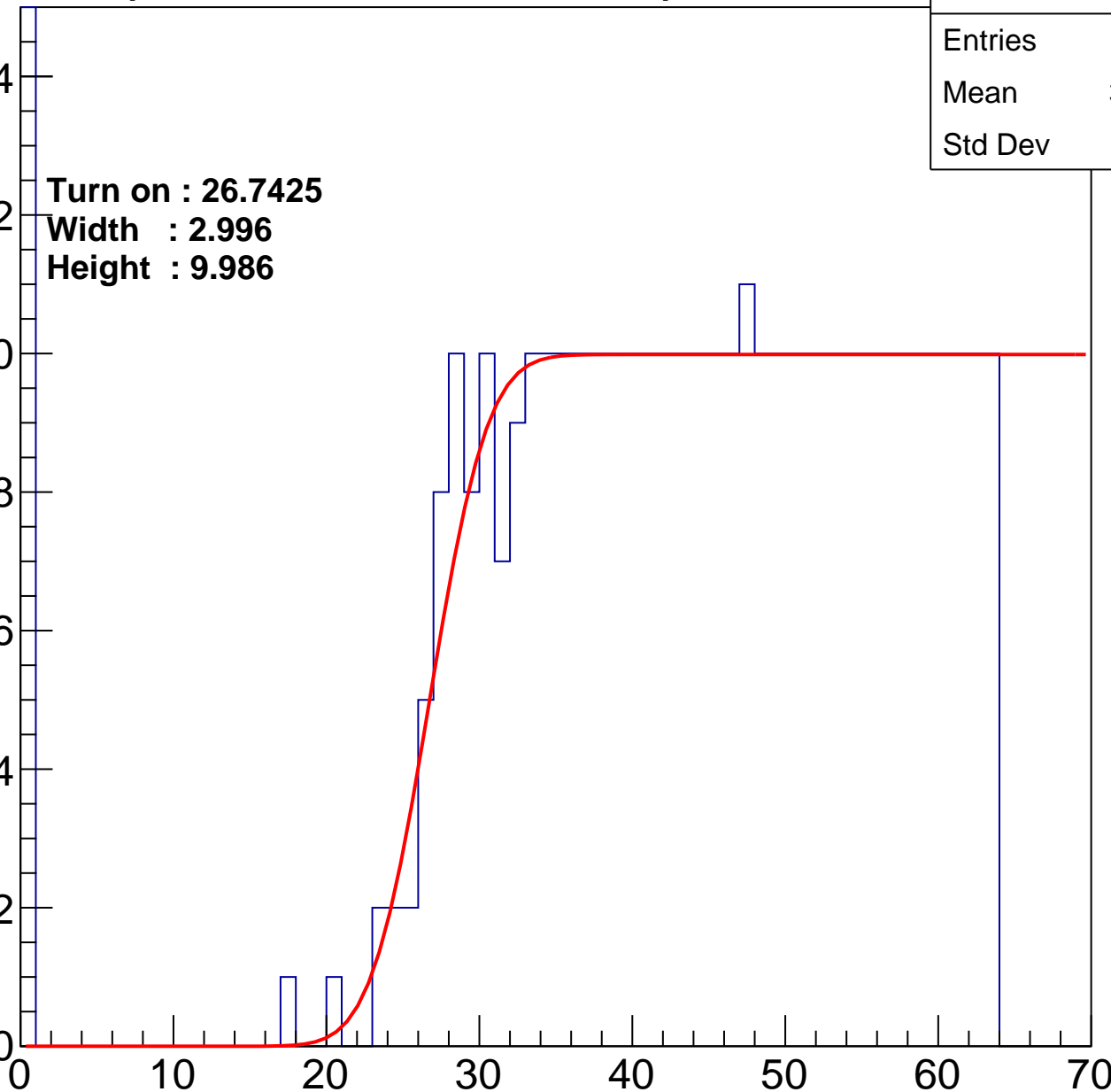
Width : 2.996

Height : 9.986

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch123

calib_packv5_041523_1651.root, FC#0, port C2

Entries	448
Mean	37.42
Std Dev	19.25

Turn on : 26.6581

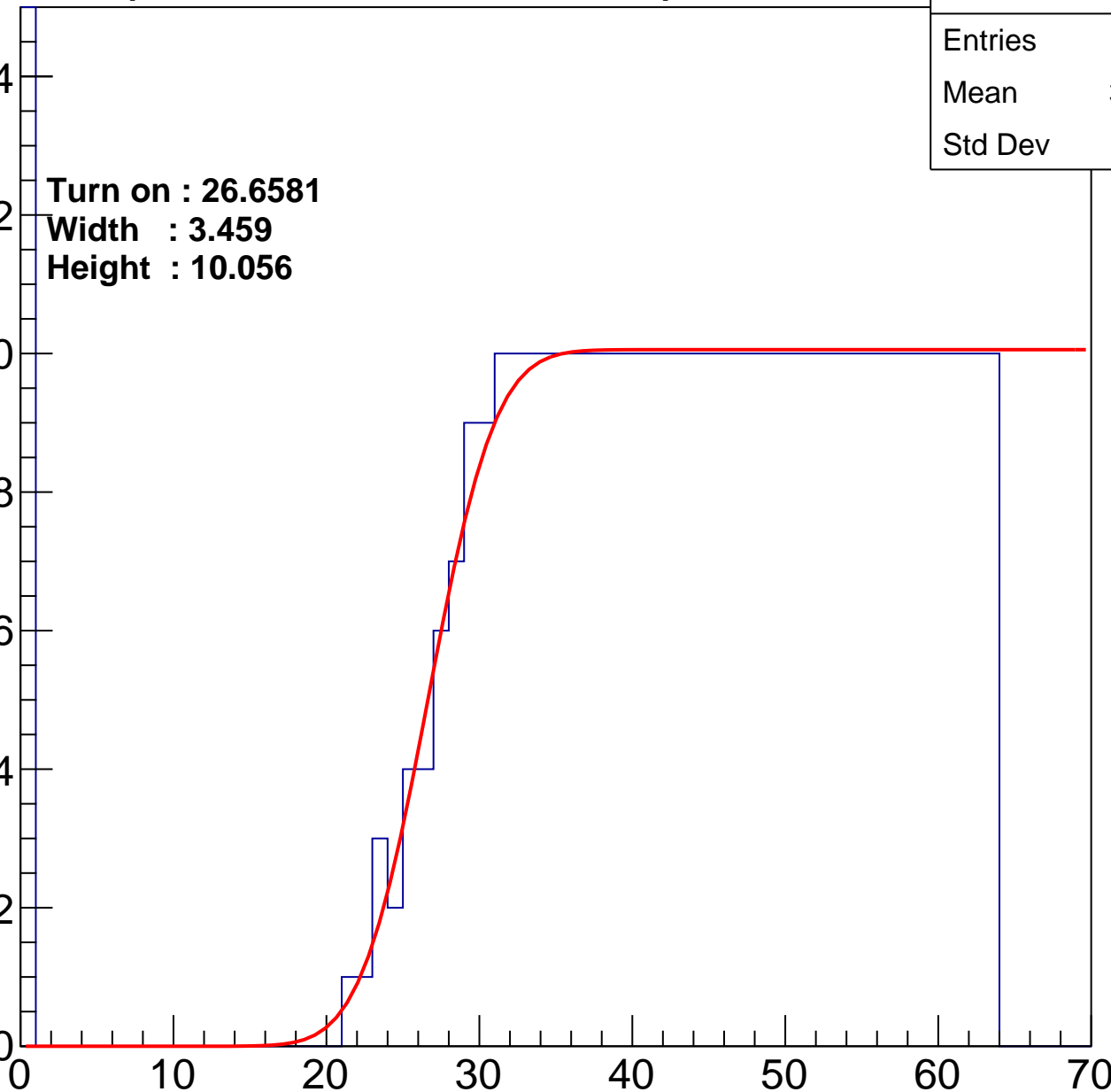
Width : 3.459

Height : 10.056

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch124

calib_packv5_041523_1651.root, FC#0, port C2

Entries	462
Mean	37.45
Std Dev	18.53

Turn on : 24.1428

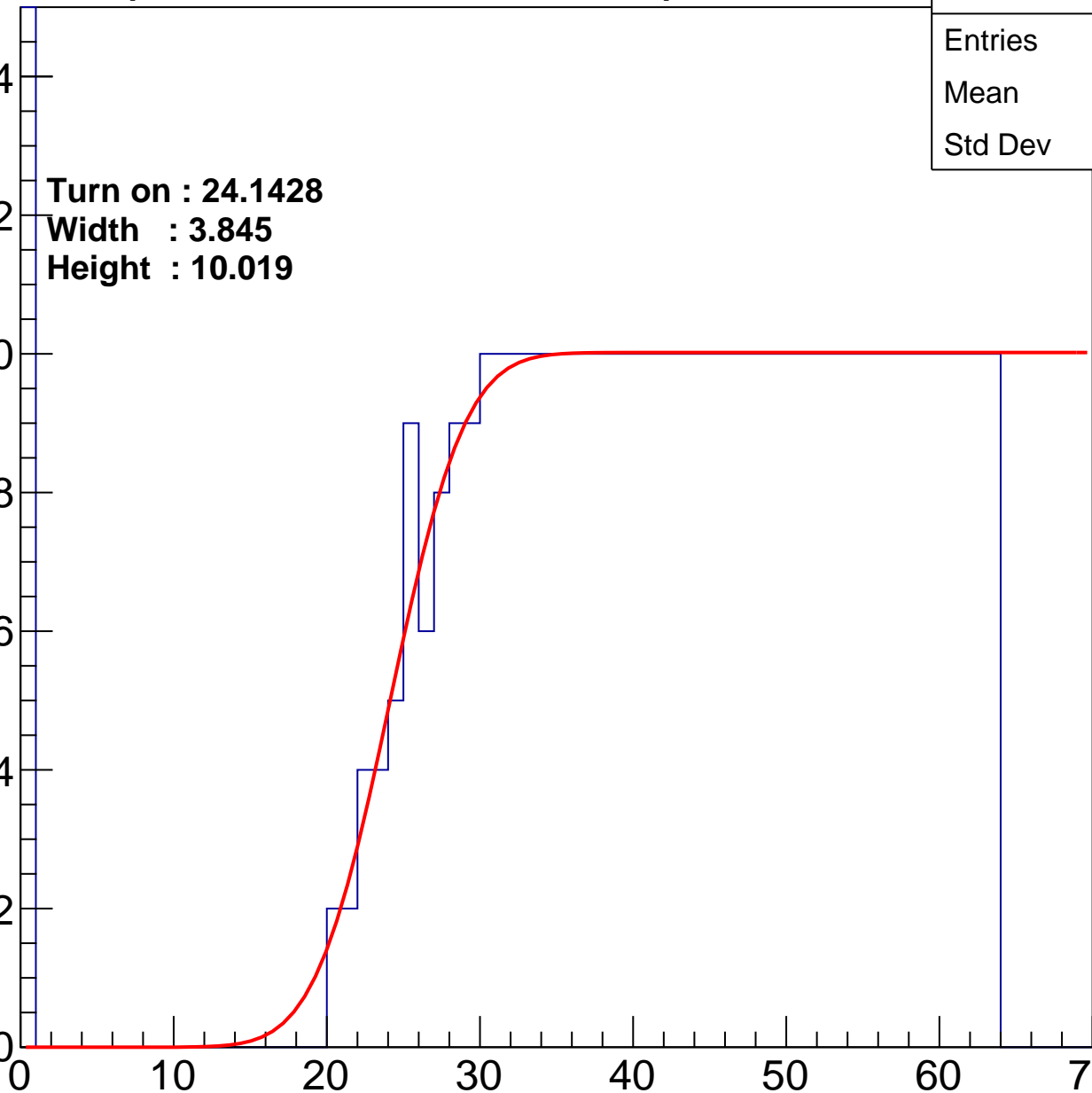
Width : 3.845

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch125

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	38.79
Std Dev	17.61

Turn on : 25.5912

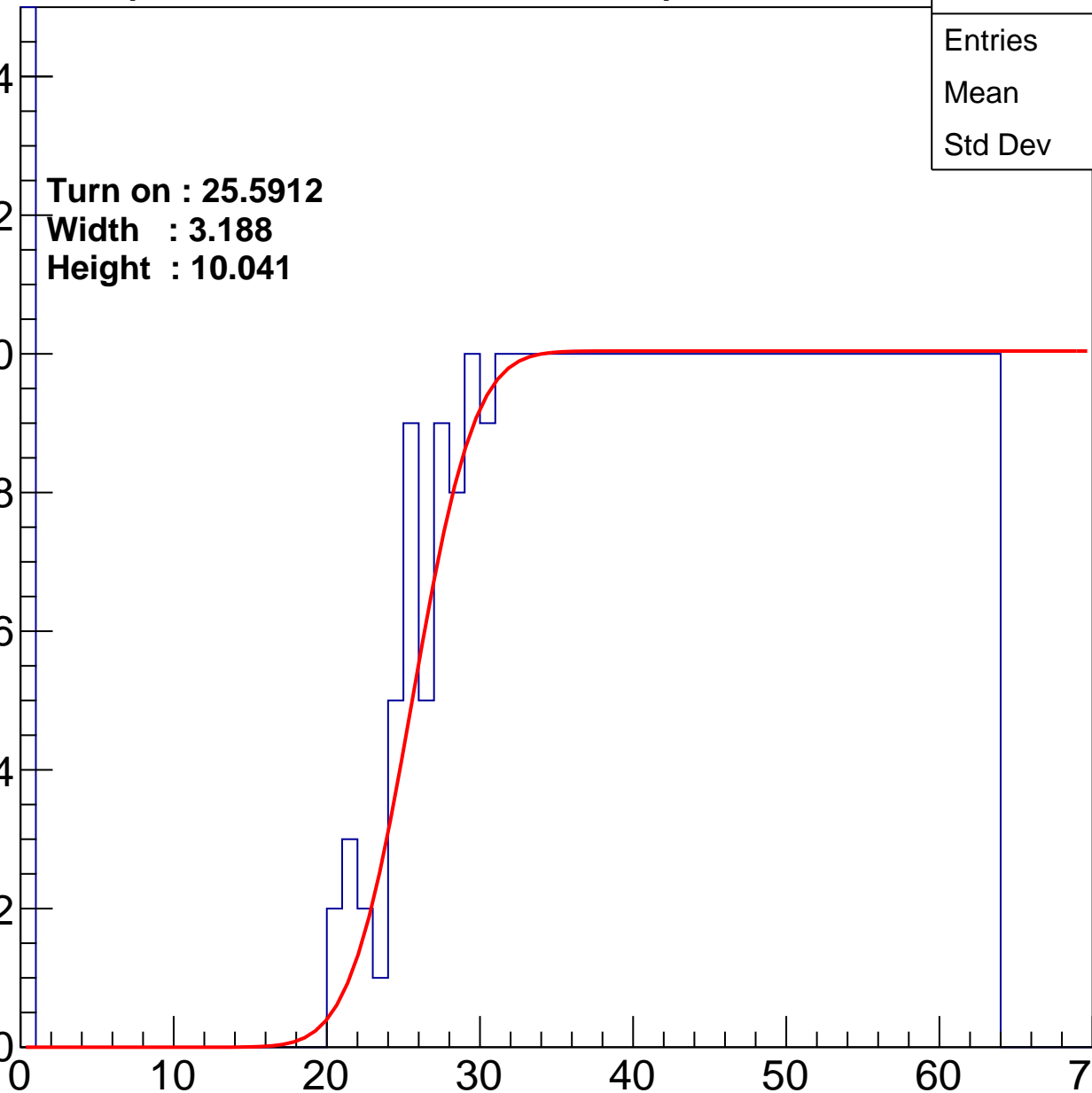
Width : 3.188

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch126

calib_packv5_041523_1651.root, FC#0, port C2

Entries	477
Mean	37.17
Std Dev	18.17

Turn on : 22.4393

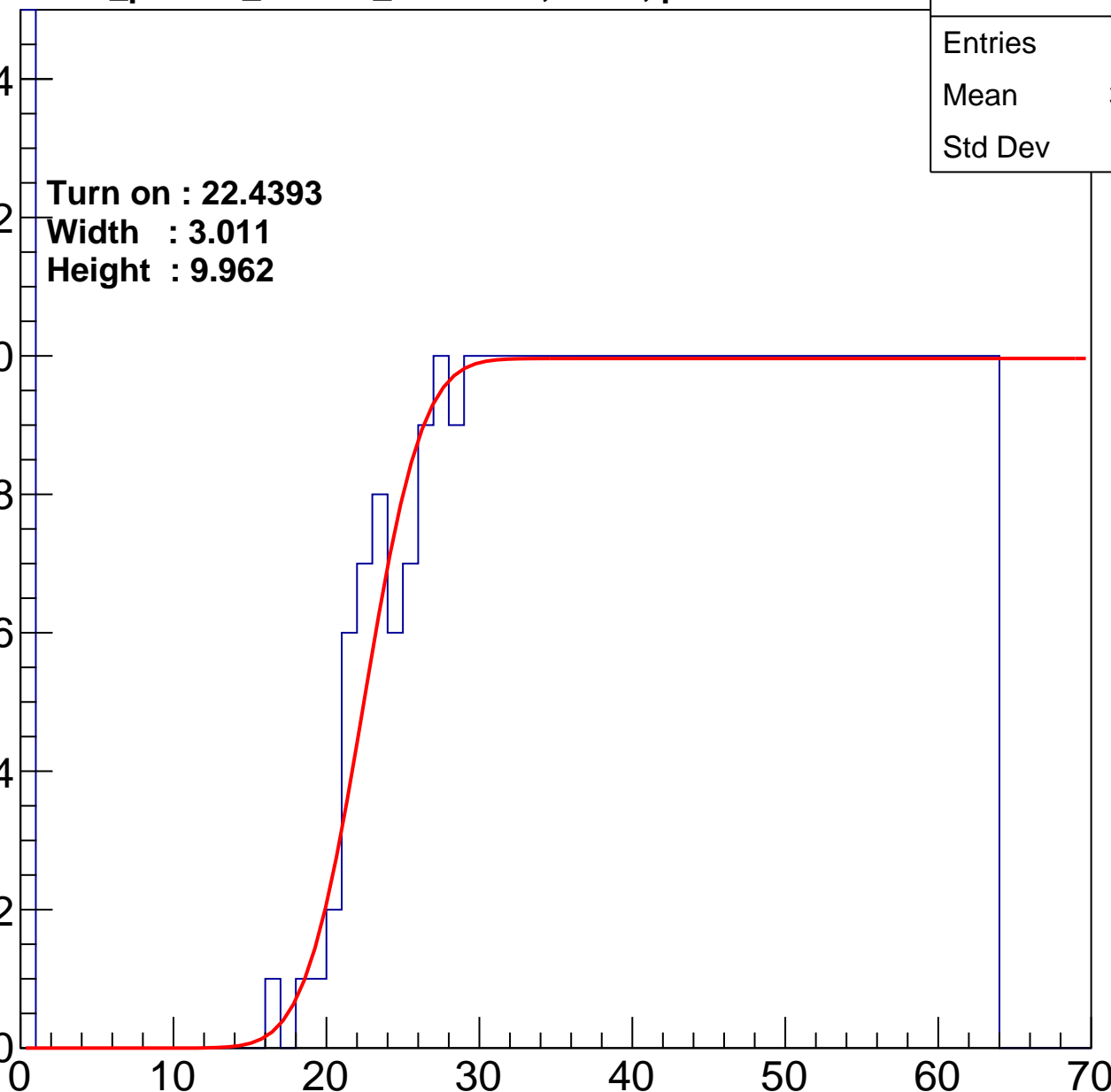
Width : 3.011

Height : 9.962

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch127

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	39.06
Std Dev	18.23

Turn on : 26.2645

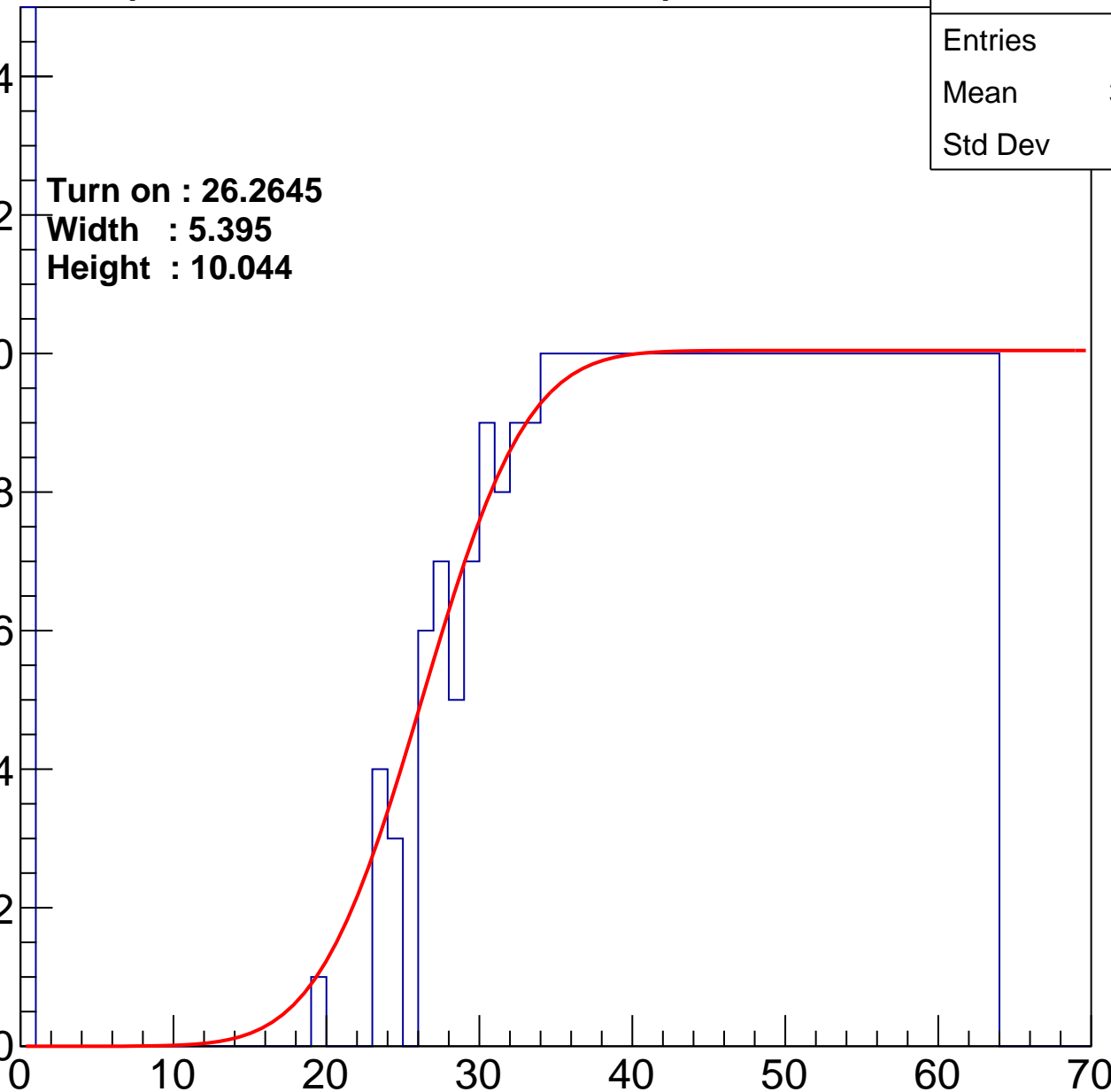
Width : 5.395

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U3-ch127

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	39.06
Std Dev	18.23

Turn on : 26.2645

Width : 5.395

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl

