



# B1L101S, U26-ch0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	375
Mean	44.59
Std Dev	11.17

Turn on : 26.9788

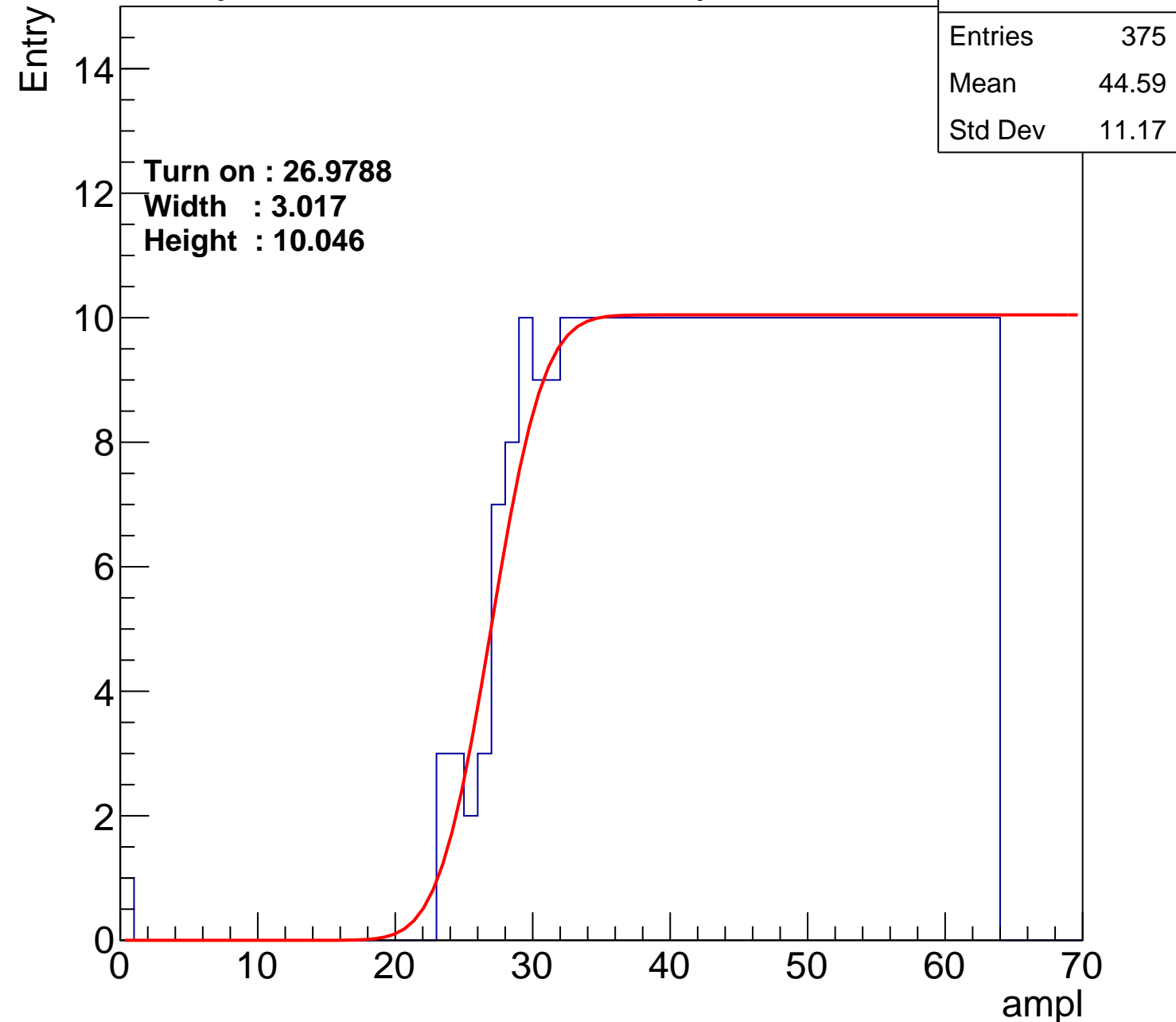
Width : 3.017

Height : 10.046

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	355
Mean	45.53
Std Dev	10.71

Turn on : 29.1591

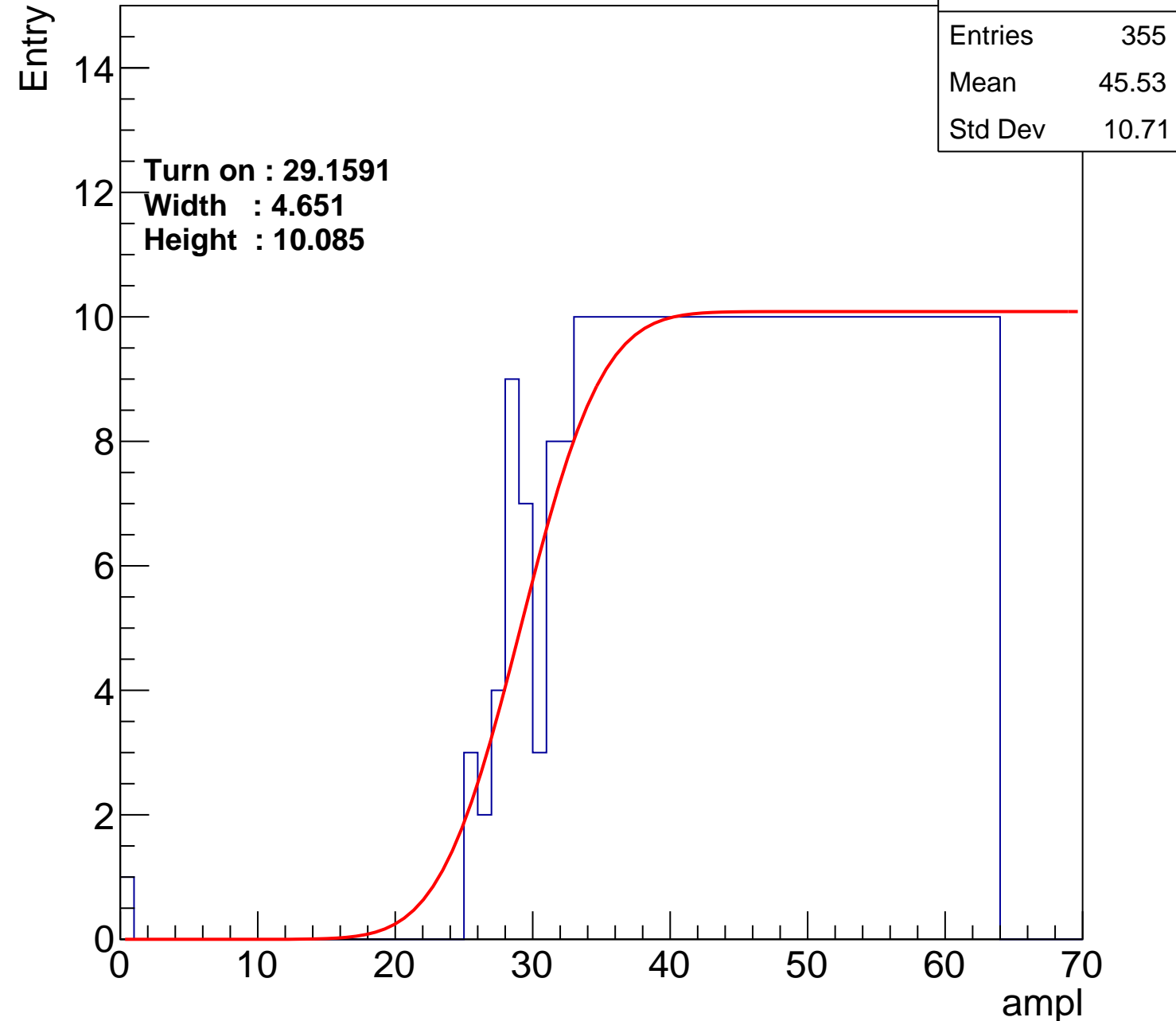
Width : 4.651

Height : 10.085

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	372
Mean	44.66
Std Dev	11.3

Turn on : 26.2064

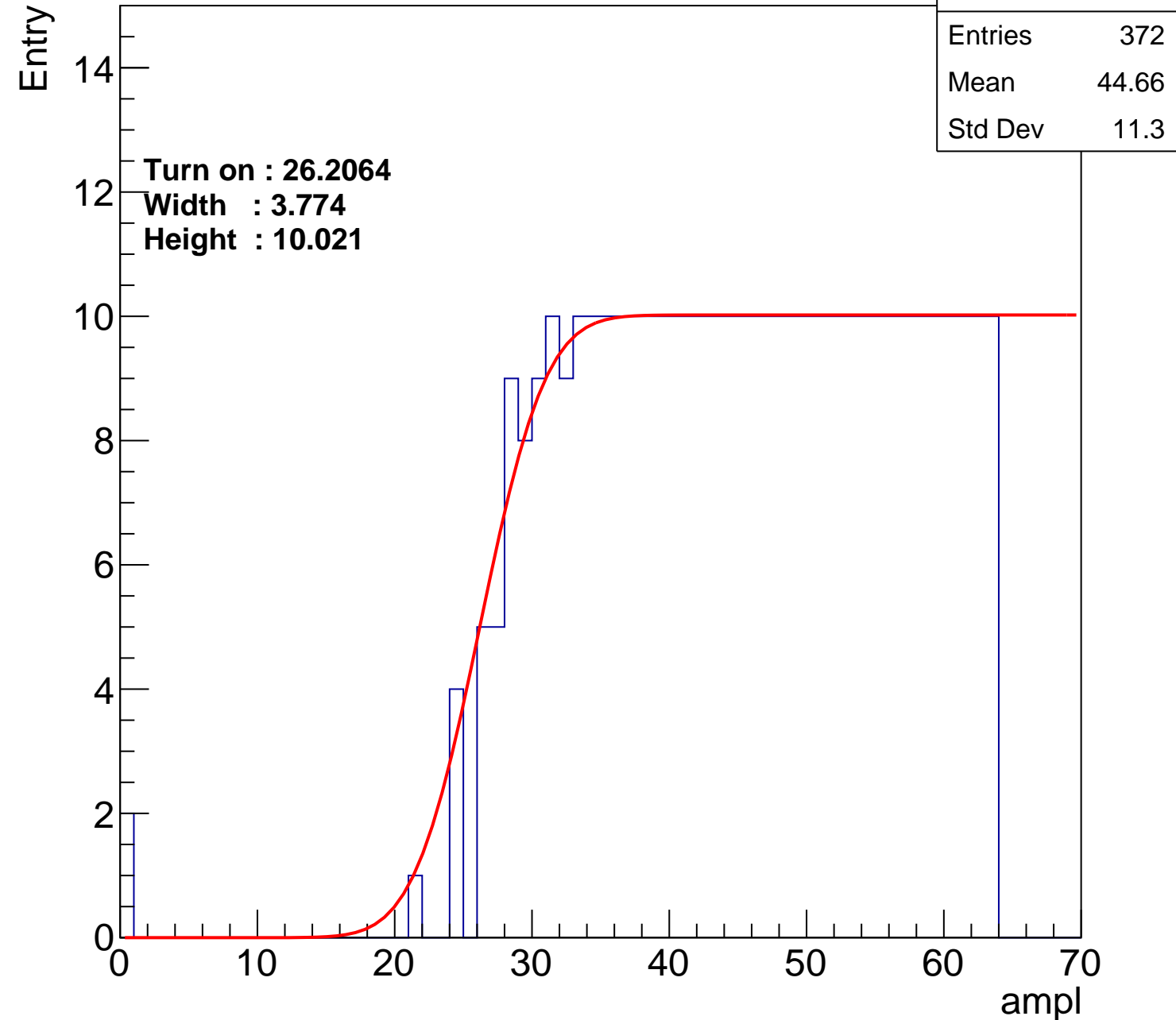
Width : 3.774

Height : 10.021

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	344
Mean	45.93
Std Dev	10.89

Turn on : 30.3007

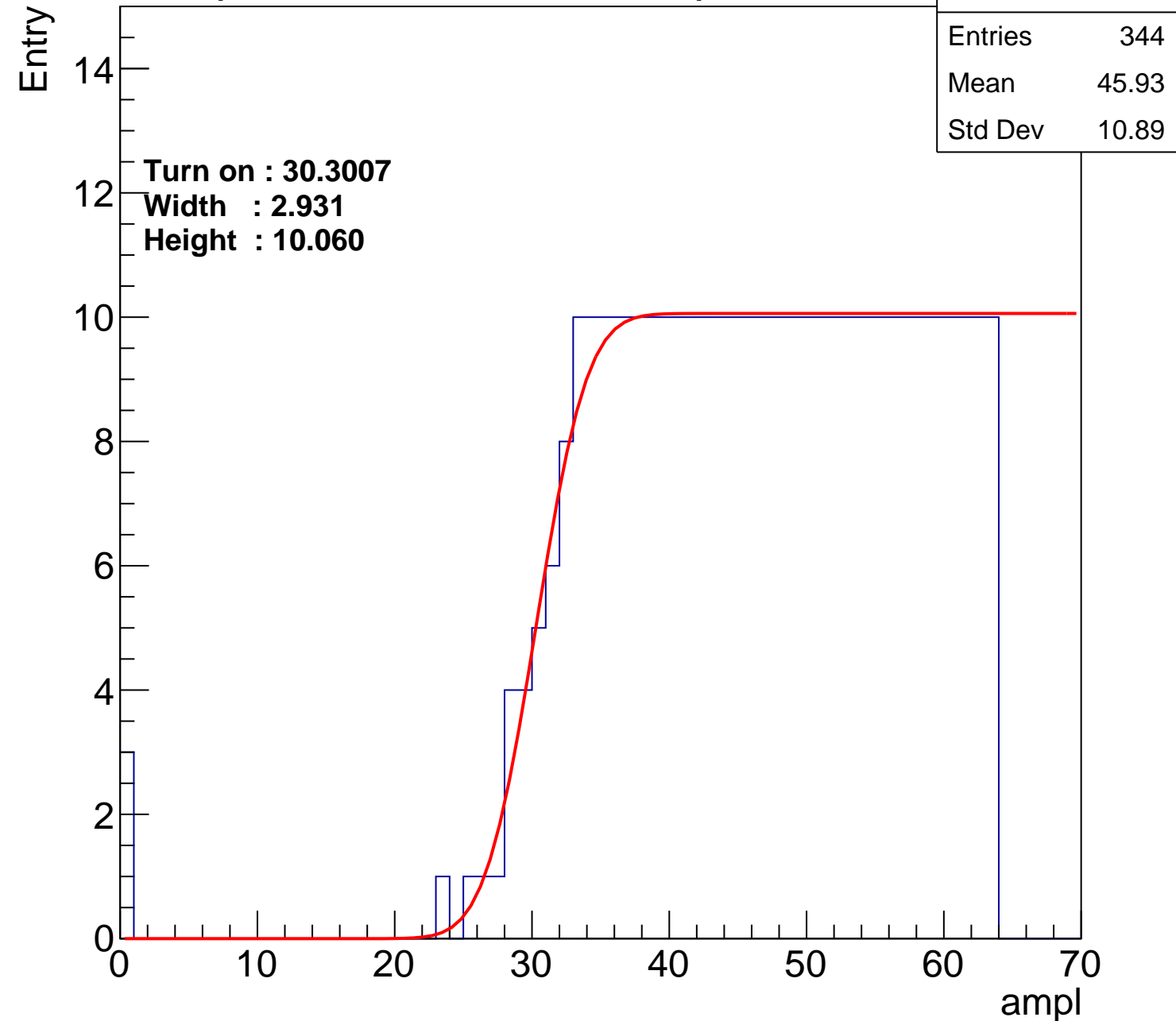
Width : 2.931

Height : 10.060

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	371
Mean	44.6
Std Dev	11.54

Turn on : 27.5271

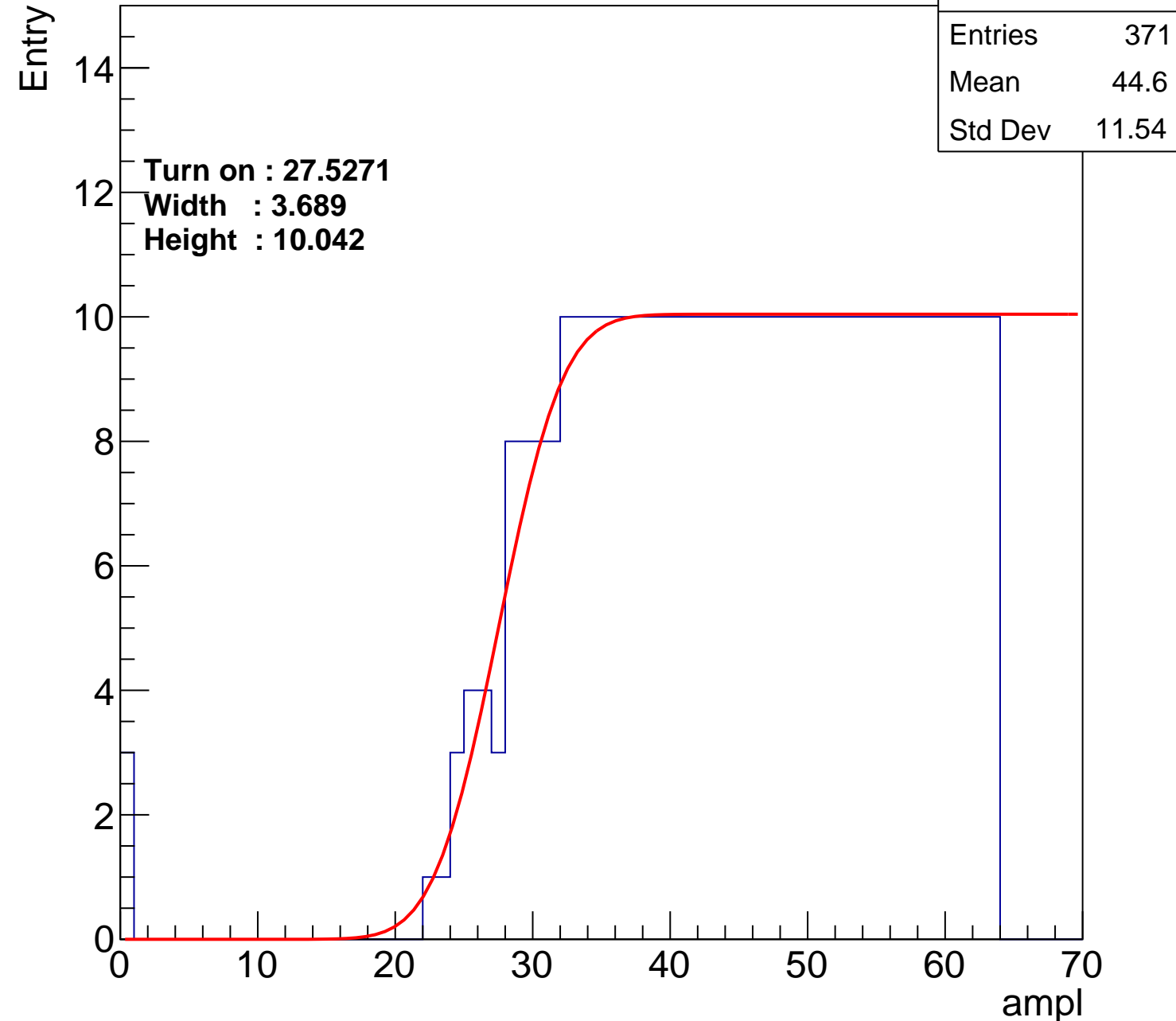
Width : 3.689

Height : 10.042

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch5

calib\_packv5\_042523\_0143.root, FC#0, port D2

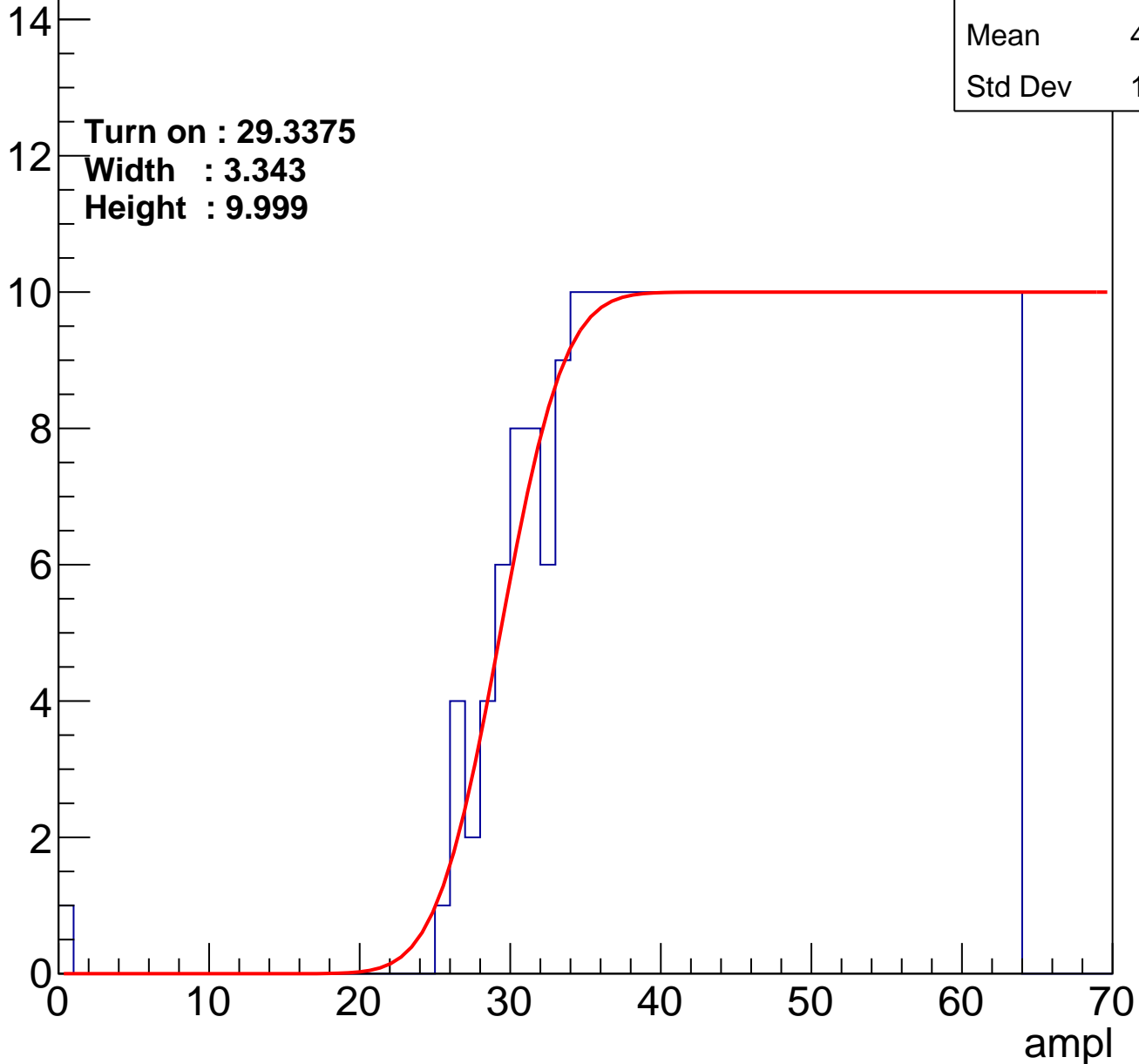
Entries	349
Mean	45.83
Std Dev	10.54

Turn on : 29.3375

Width : 3.343

Height : 9.999

Entry



# B1L101S, U26-ch6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	348
Mean	45.95
Std Dev	10.41

Turn on : 28.3768

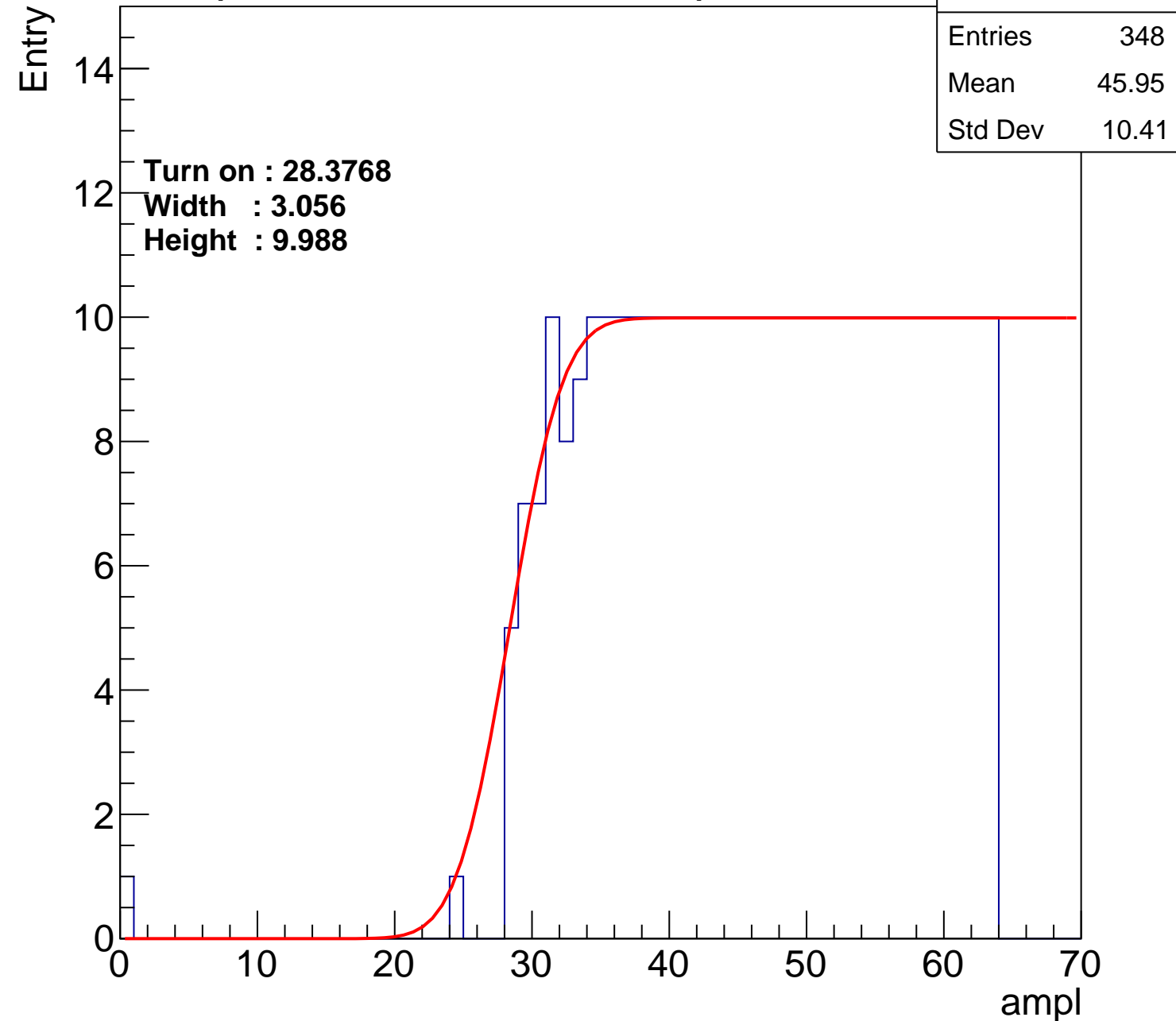
Width : 3.056

Height : 9.988

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U26-ch7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	360
Mean	45.23
Std Dev	11.05

Turn on : 28.6926

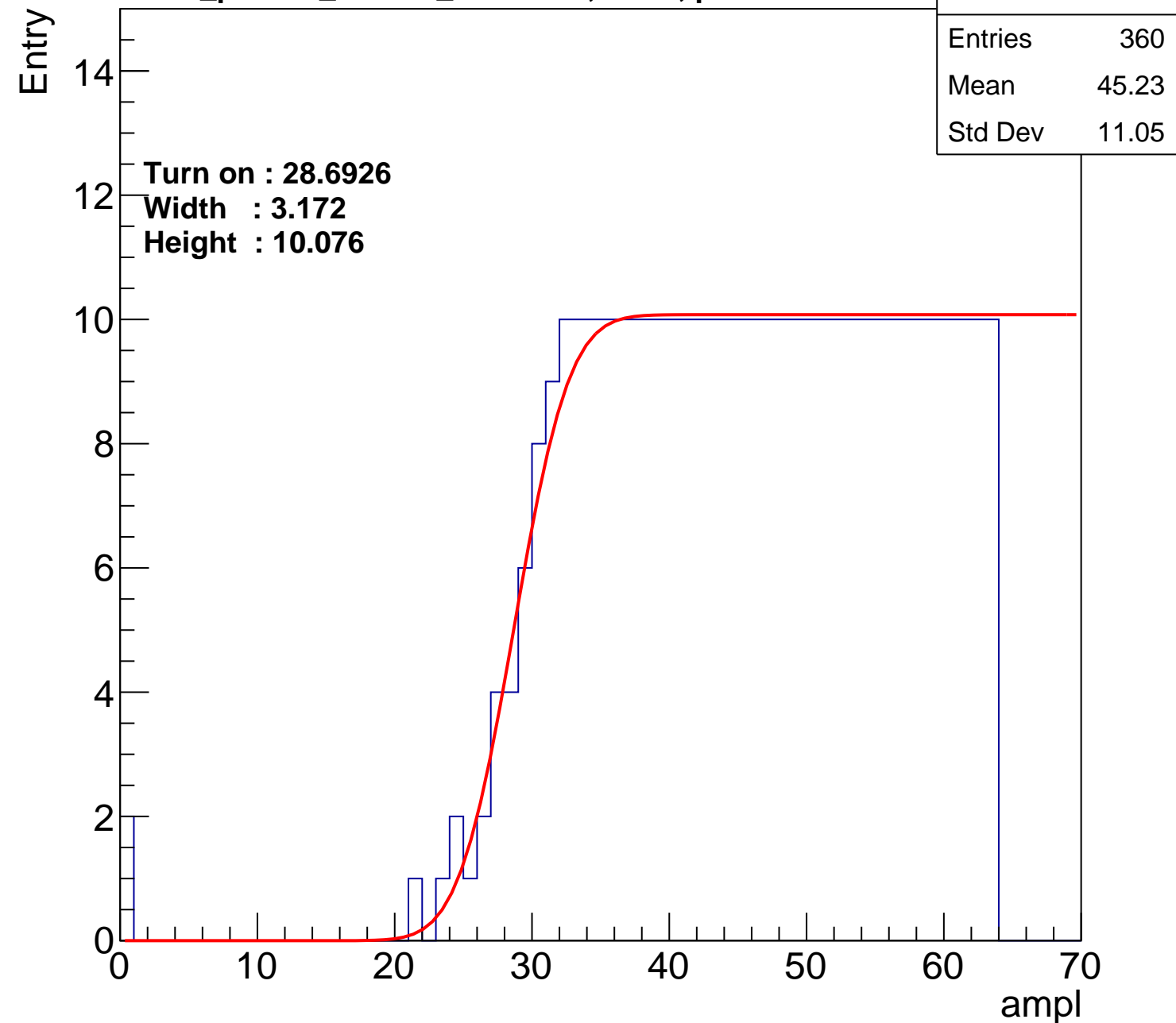
Width : 3.172

Height : 10.076

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch8

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	355
Mean	45.41
Std Dev	11.11

Turn on : 28.5678

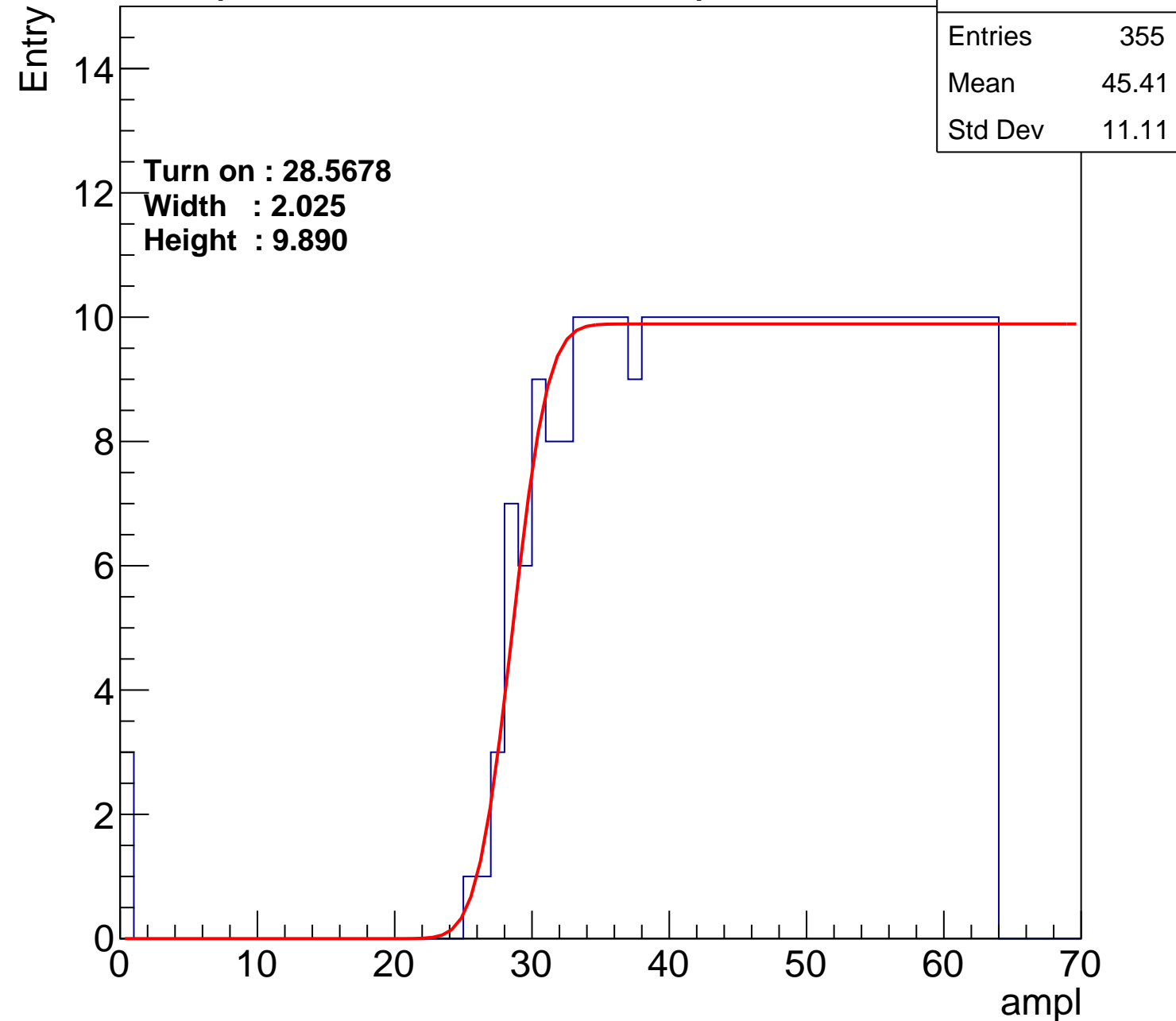
Width : 2.025

Height : 9.890

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch9

calib\_packv5\_042523\_0143.root, FC#0, port D2

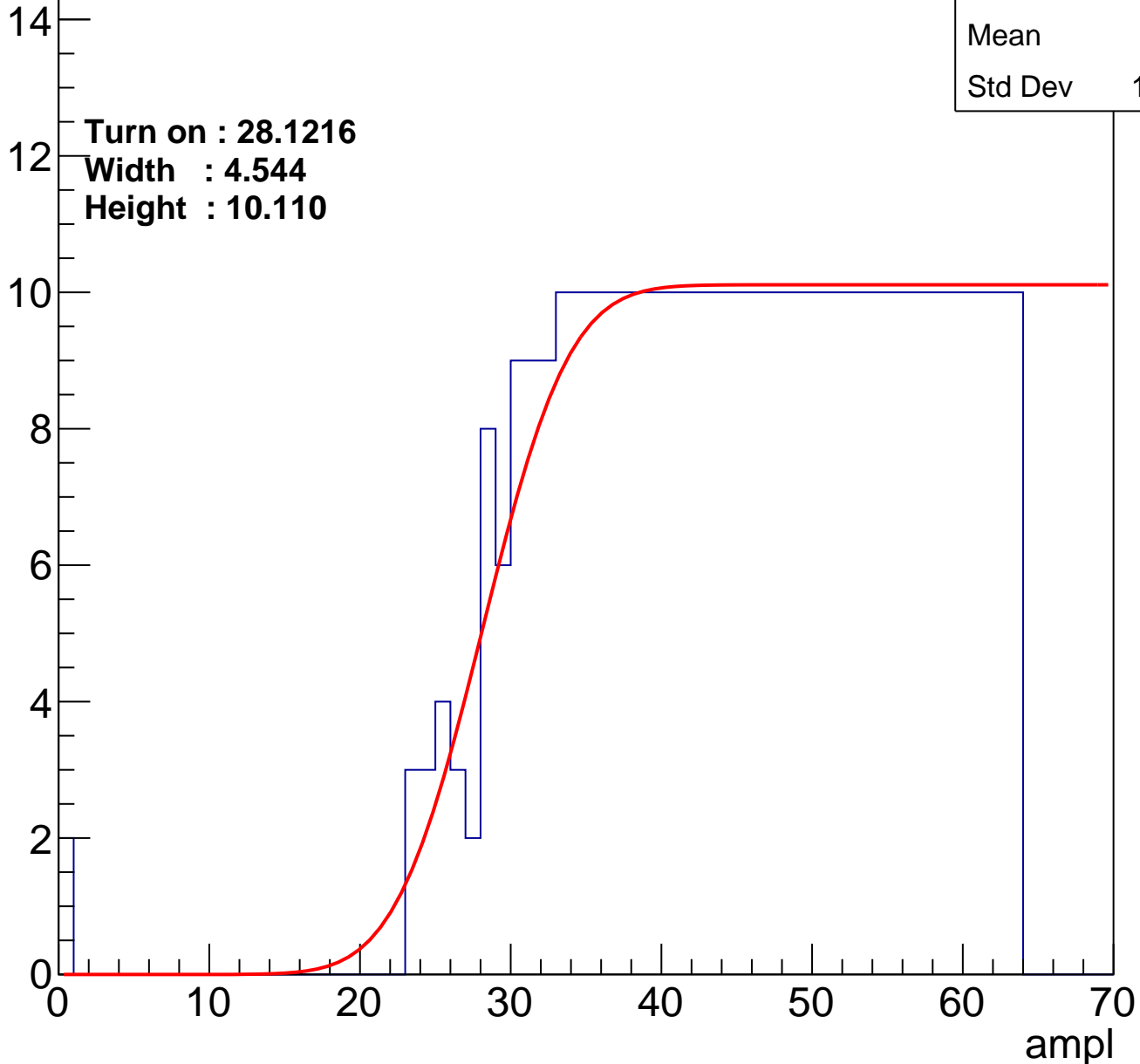
Entries	368
Mean	44.8
Std Dev	11.29

**Turn on : 28.1216**

**Width : 4.544**

**Height : 10.110**

Entry



# B1L101S, U26-ch10

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	355
Mean	45.45
Std Dev	10.94

Turn on : 29.0622

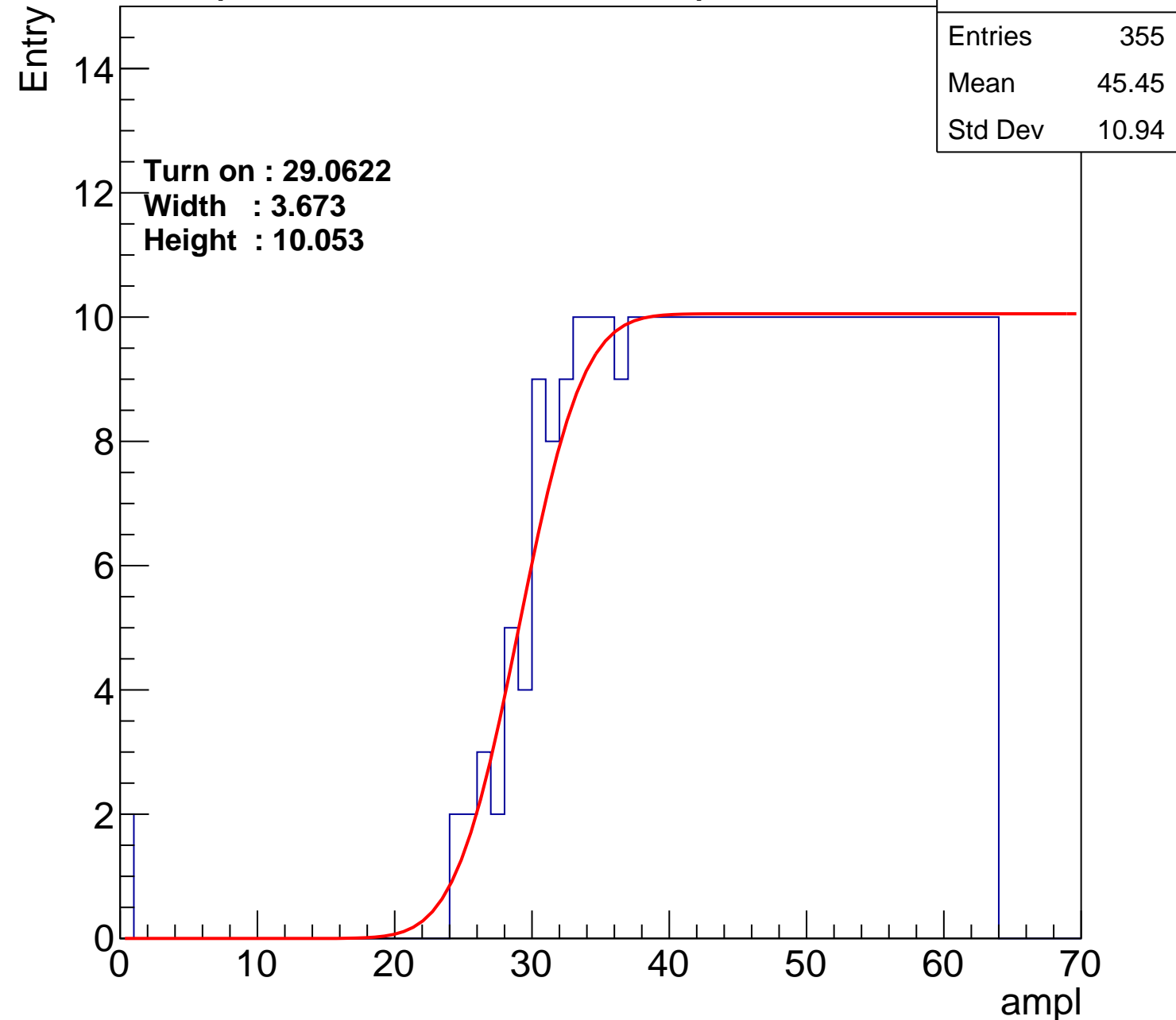
Width : 3.673

Height : 10.053

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch11

calib\_packv5\_042523\_0143.root, FC#0, port D2

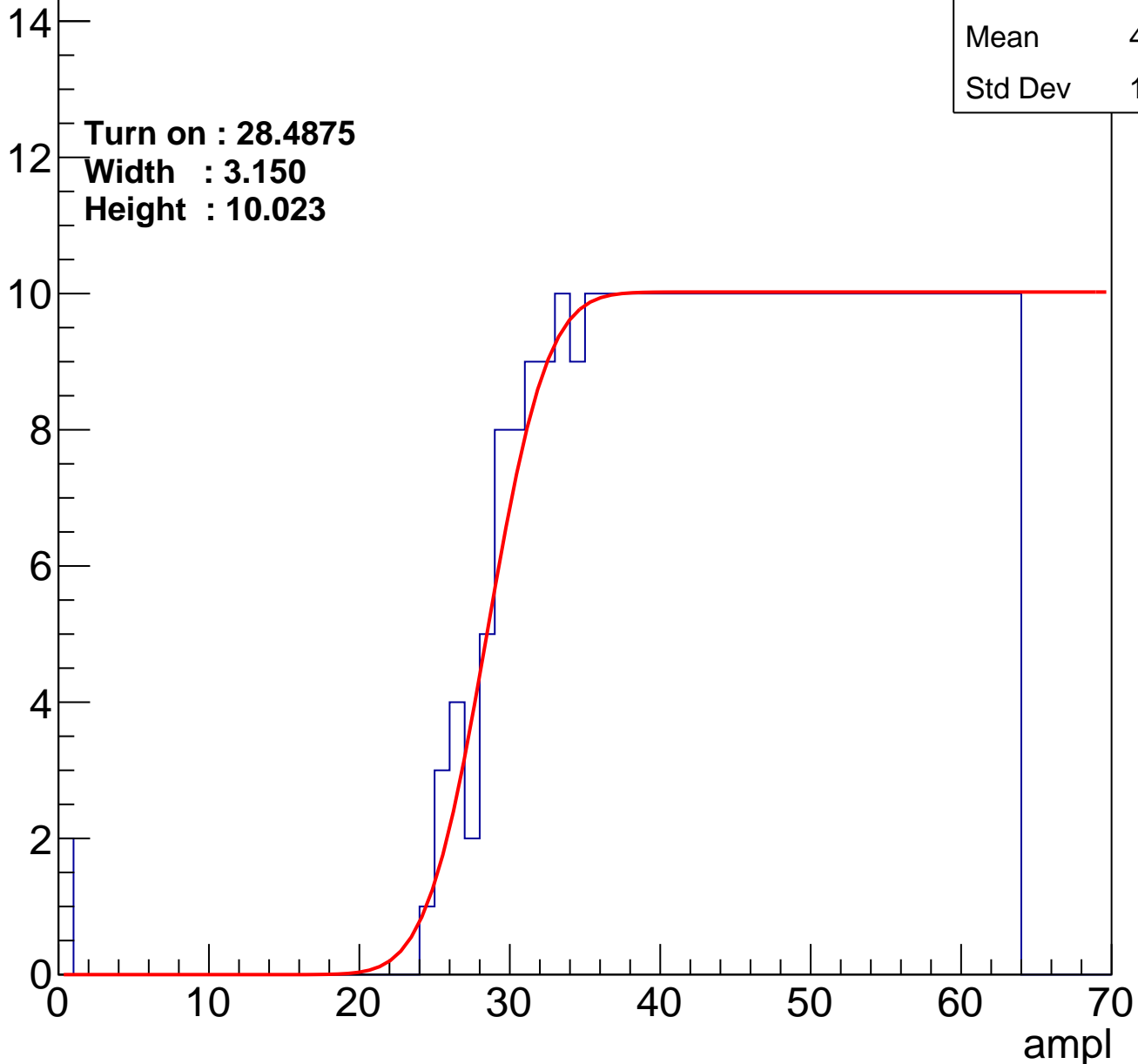
Entries	360
Mean	45.23
Std Dev	11.03

Turn on : 28.4875

Width : 3.150

Height : 10.023

Entry



# B1L101S, U26-ch12

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	373
Mean	44.68
Std Dev	11.13

Turn on : 27.0905

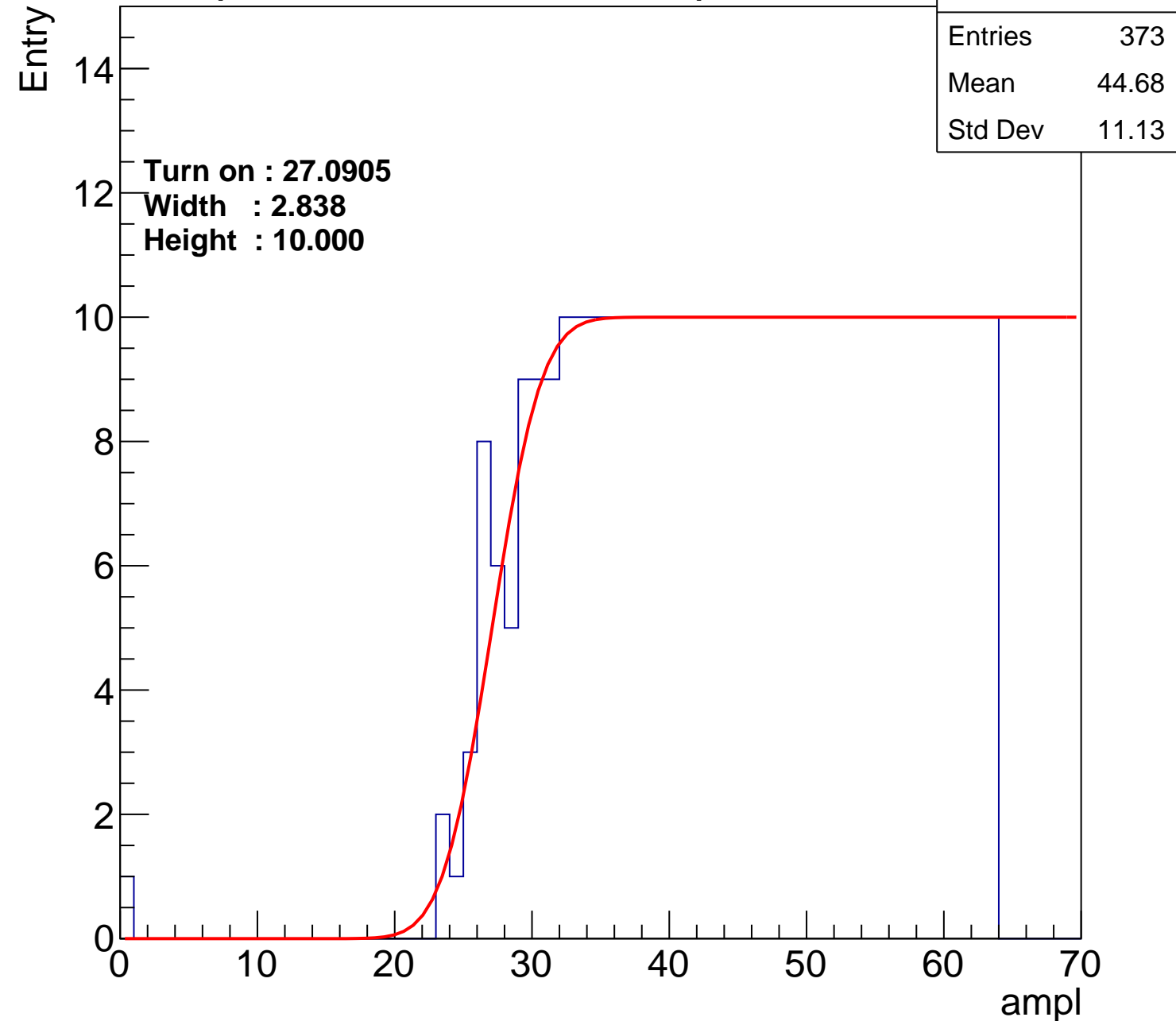
Width : 2.838

Height : 10.000

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch13

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	354
Mean	45.65
Std Dev	10.58

**Turn on : 29.2308**

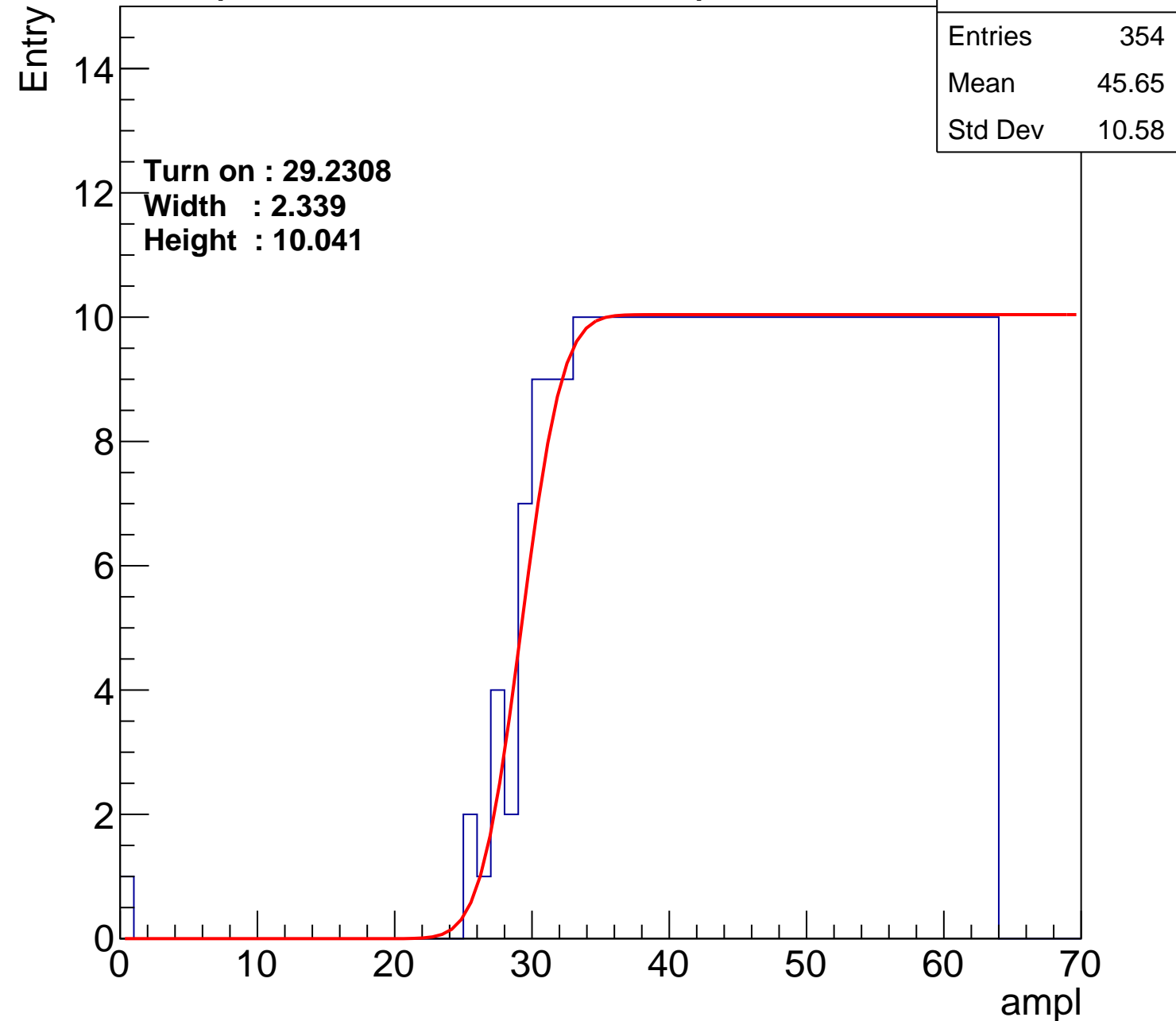
**Width : 2.339**

**Height : 10.041**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch14

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	360
Mean	45.04
Std Dev	11.51

Turn on : 28.5674

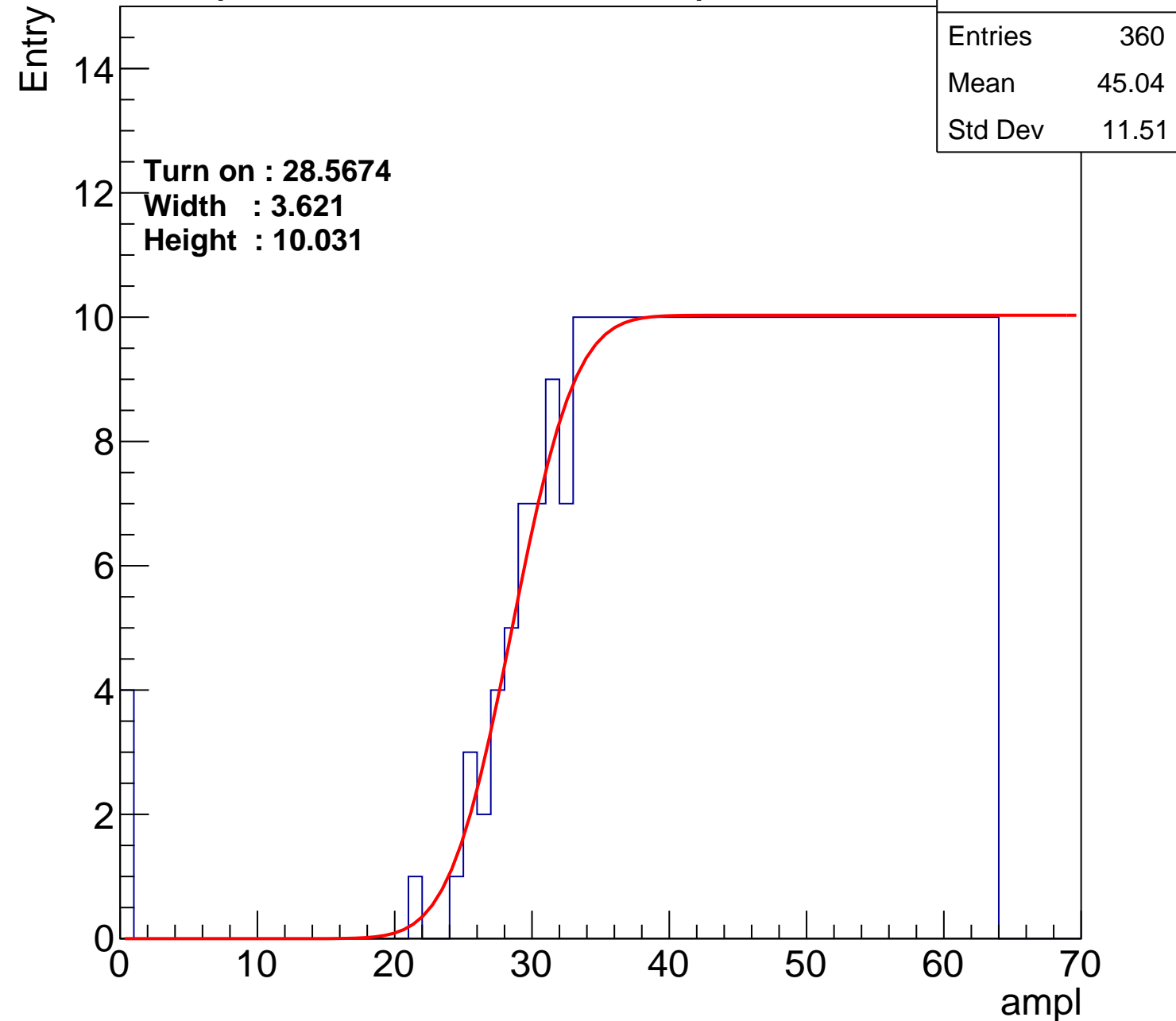
Width : 3.621

Height : 10.031

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U26-ch15

calib\_packv5\_042523\_0143.root, FC#0, port D2

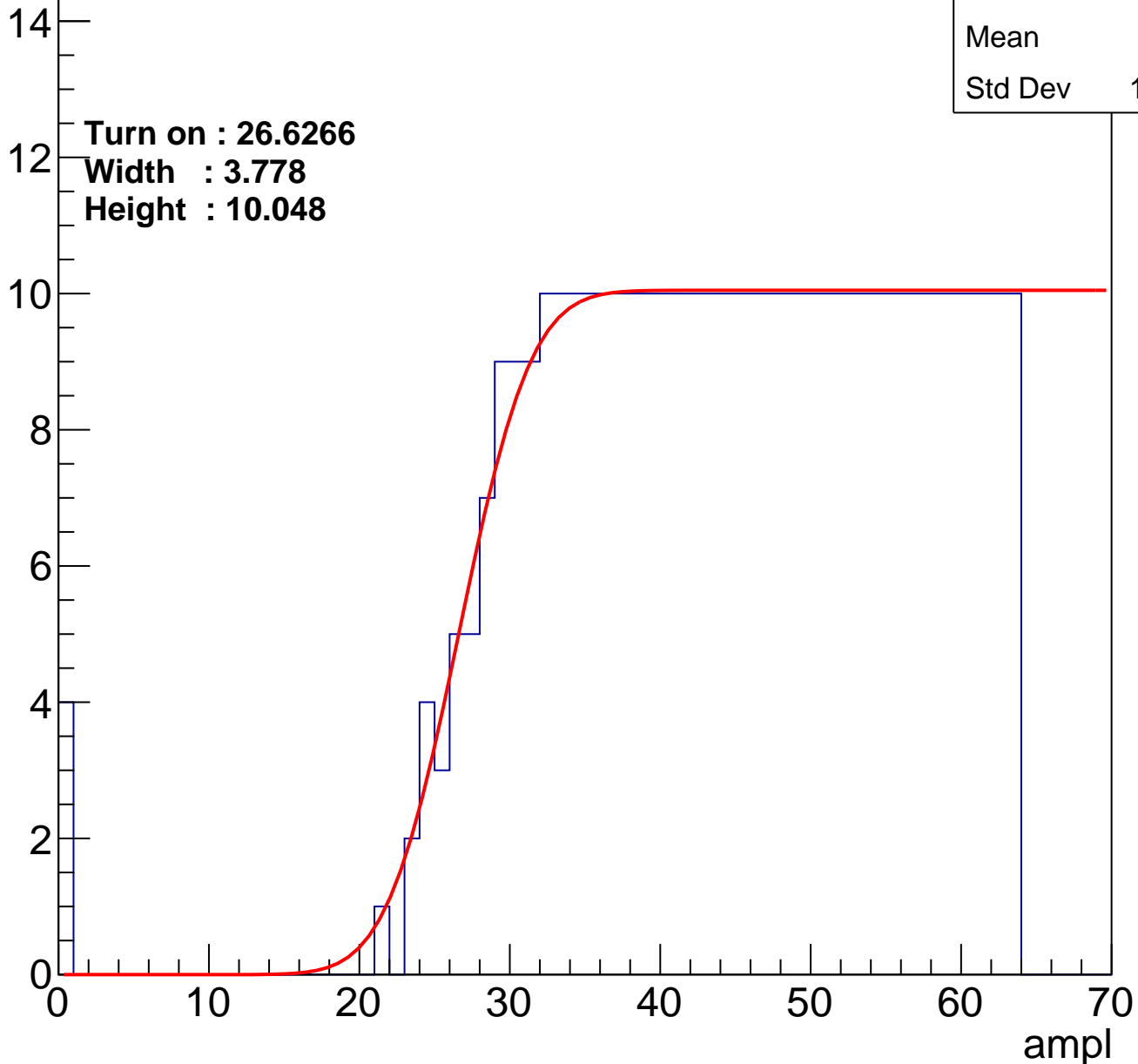
Entries	378
Mean	44.2
Std Dev	11.86

Turn on : 26.6266

Width : 3.778

Height : 10.048

Entry



# B1L101S, U26-ch16

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	348
Mean	45.82
Std Dev	10.73

**Turn on : 29.5306**

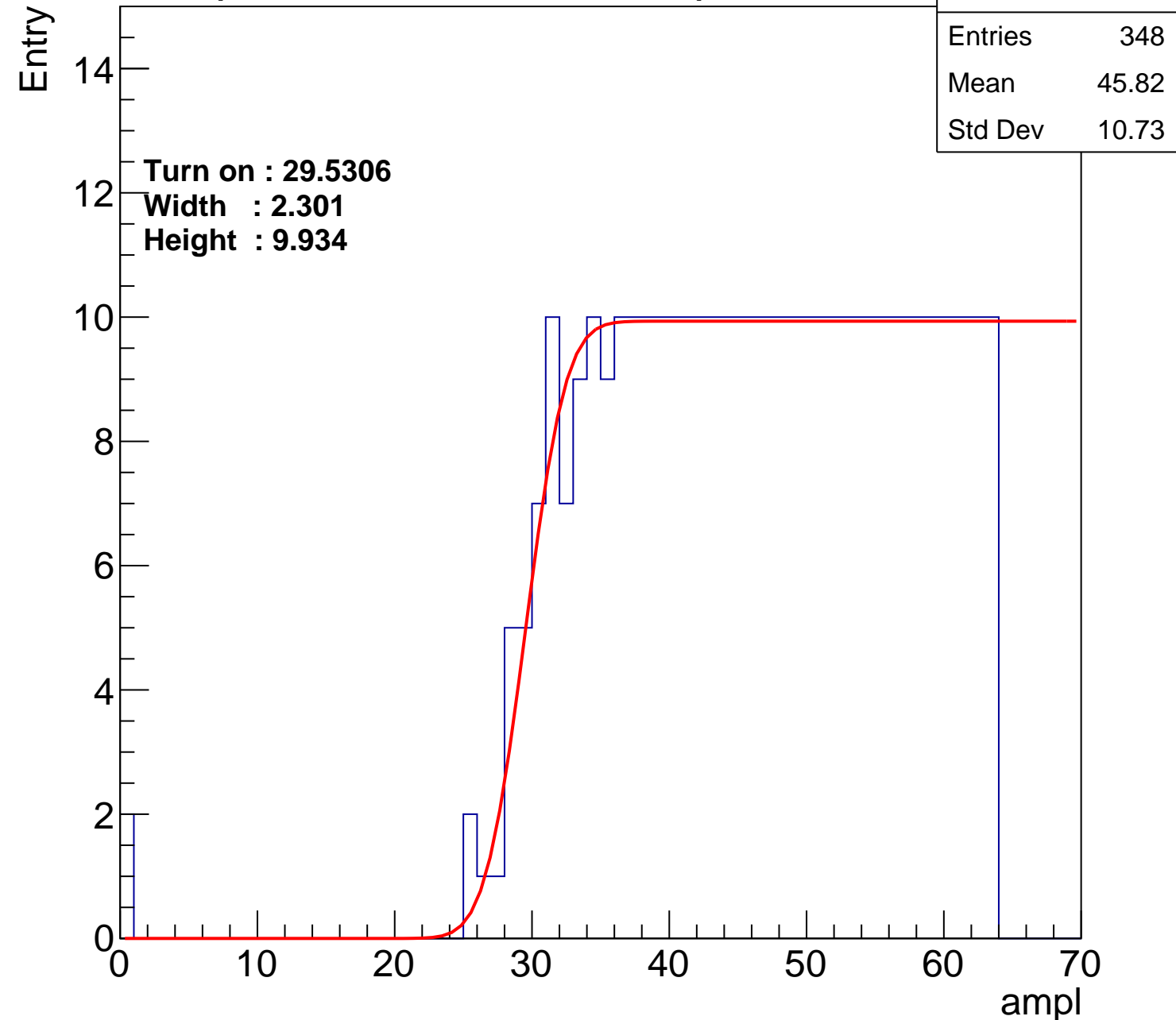
**Width : 2.301**

**Height : 9.934**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch17

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	373
Mean	44.73
Std Dev	11.06

Turn on : 27.0435

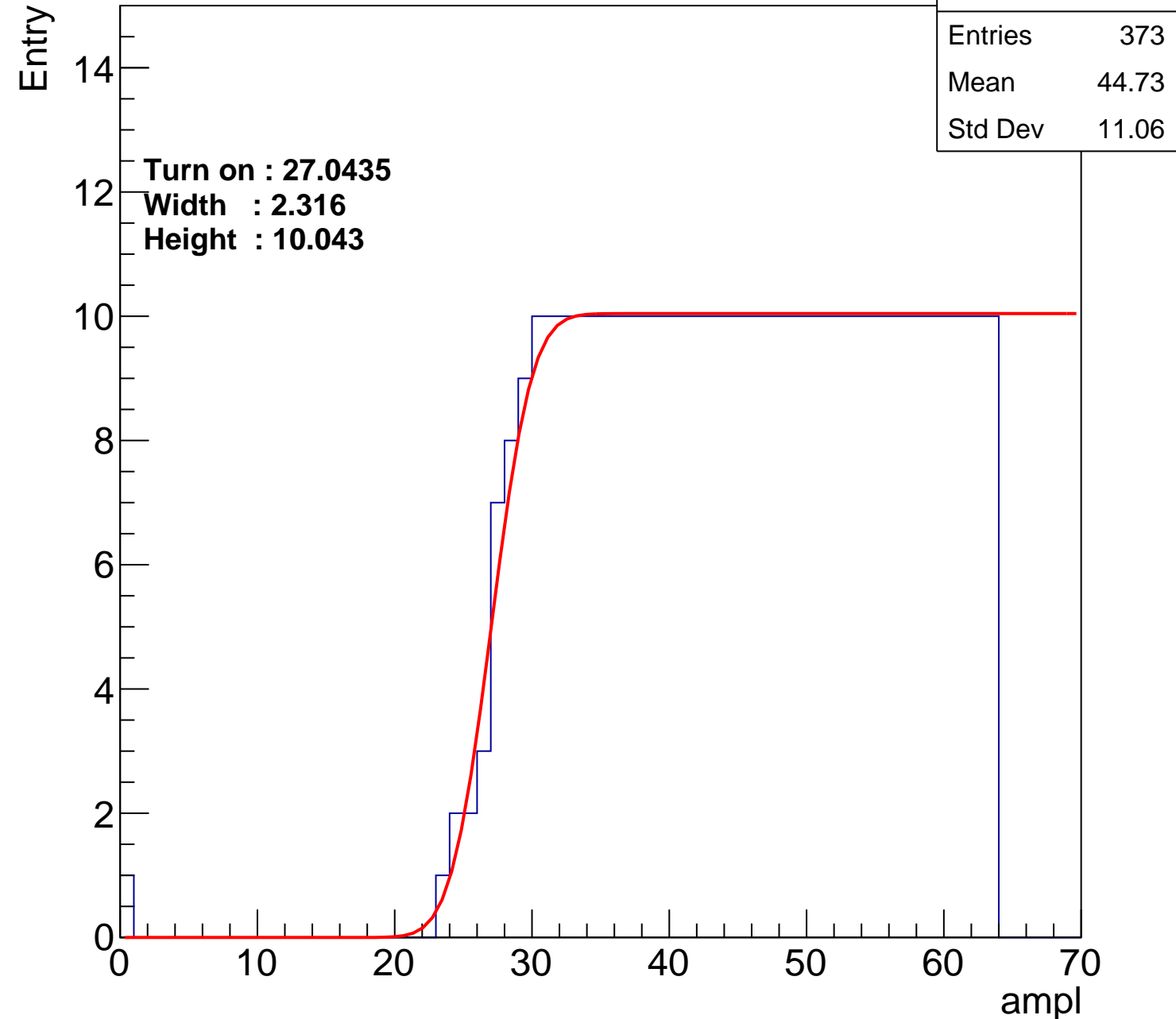
Width : 2.316

Height : 10.043

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch18

calib\_packv5\_042523\_0143.root, FC#0, port D2

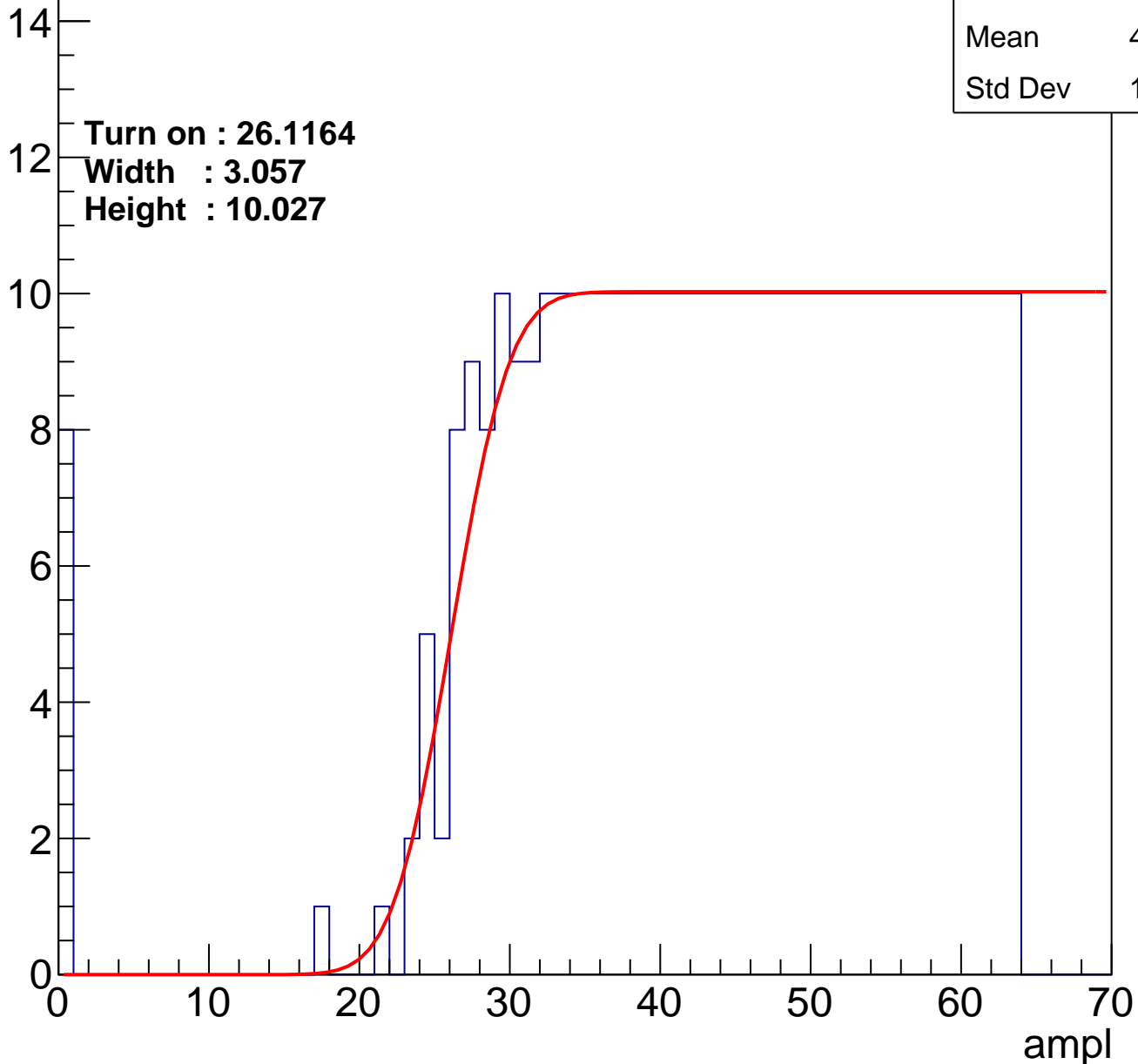
Entries	392
Mean	43.29
Std Dev	12.79

Turn on : 26.1164

Width : 3.057

Height : 10.027

Entry



# B1L101S, U26-ch19

calib\_packv5\_042523\_0143.root, FC#0, port D2

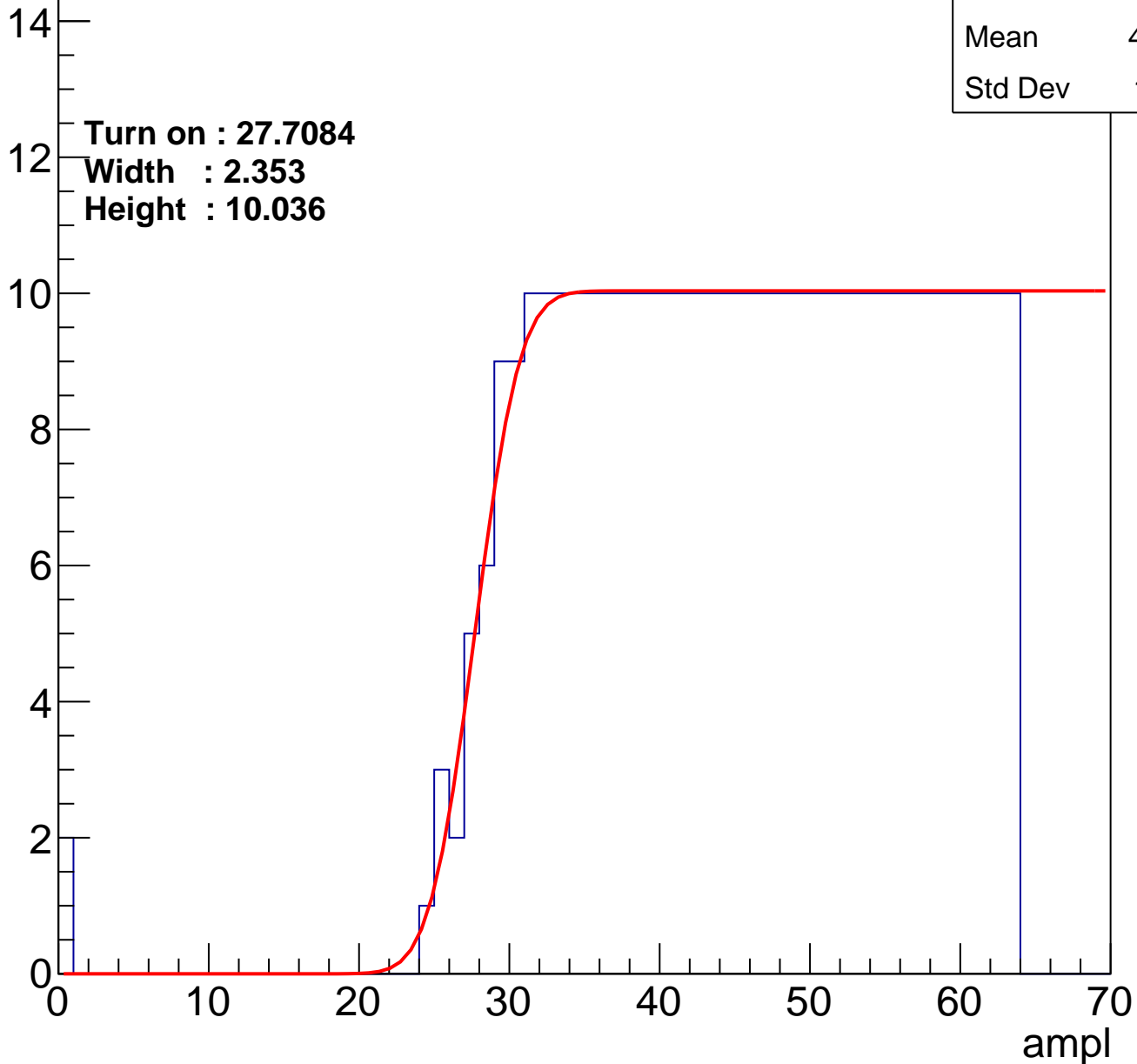
Entries	367
Mean	44.95
Std Dev	11.11

Turn on : 27.7084

Width : 2.353

Height : 10.036

Entry



# B1L101S, U26-ch20

calib\_packv5\_042523\_0143.root, FC#0, port D2

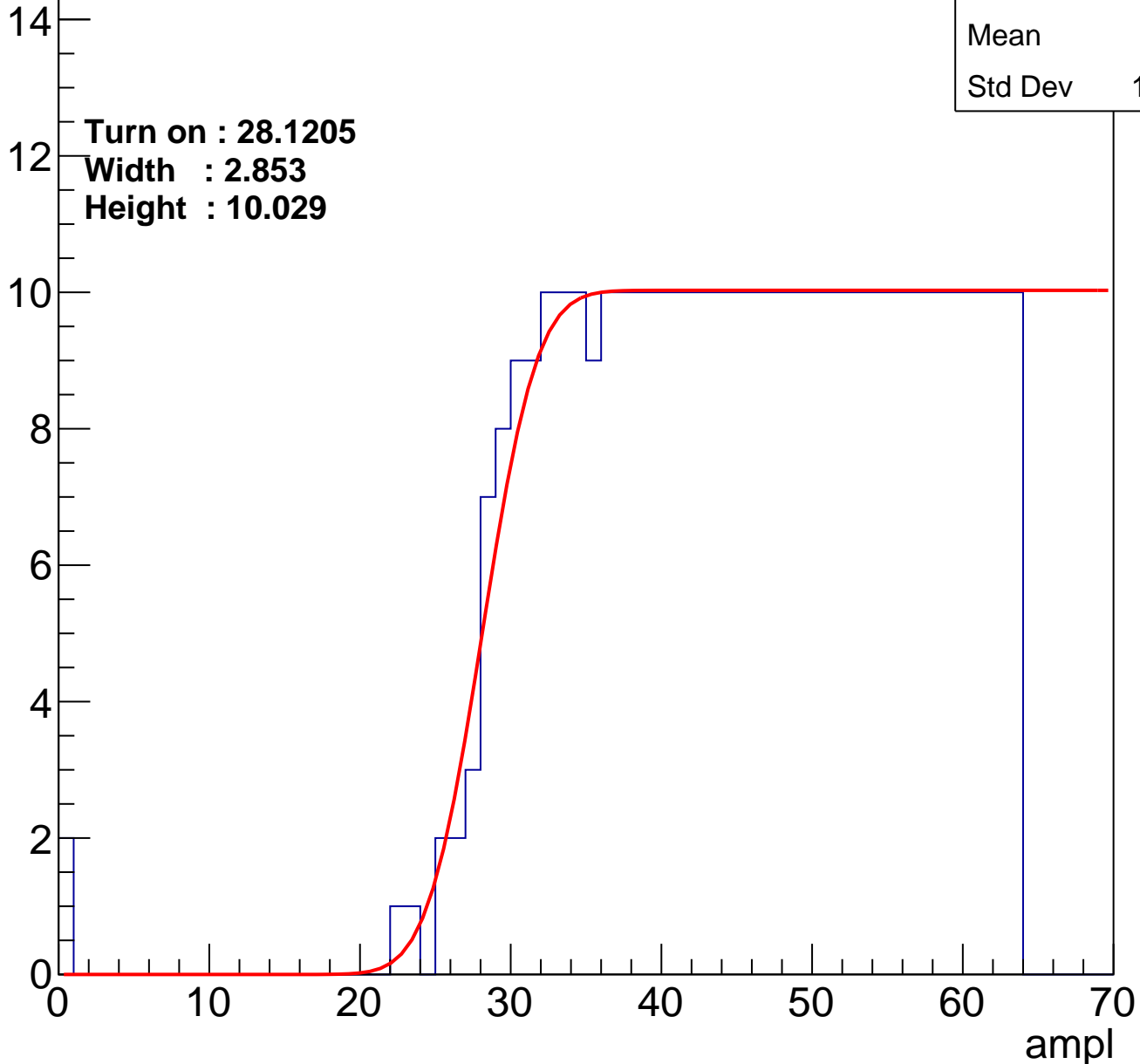
Entries	363
Mean	45.1
Std Dev	11.08

**Turn on : 28.1205**

**Width : 2.853**

**Height : 10.029**

Entry



# B1L101S, U26-ch21

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	387
Mean	43.92
Std Dev	11.69

Turn on : 25.4723

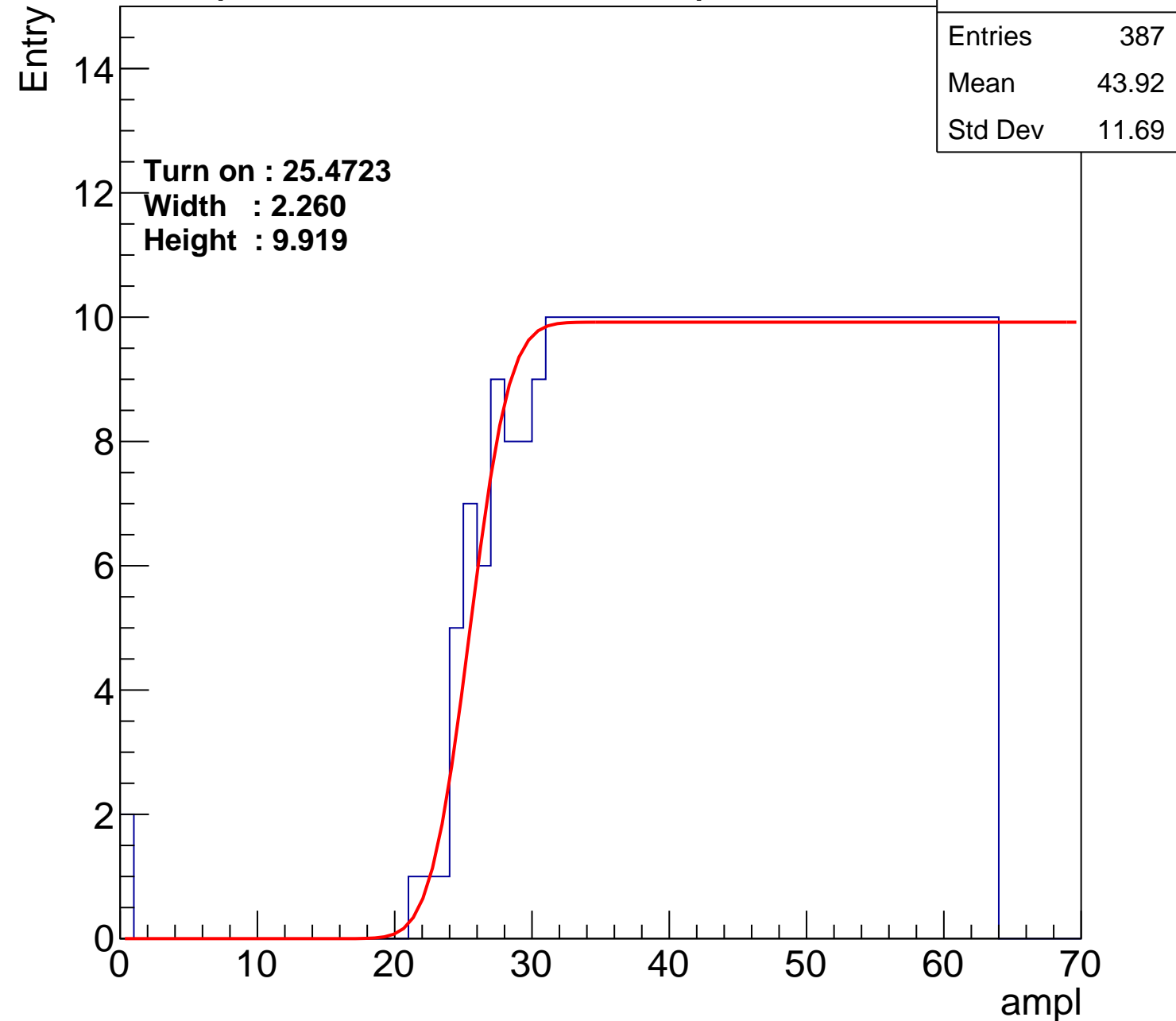
Width : 2.260

Height : 9.919

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch22

calib\_packv5\_042523\_0143.root, FC#0, port D2

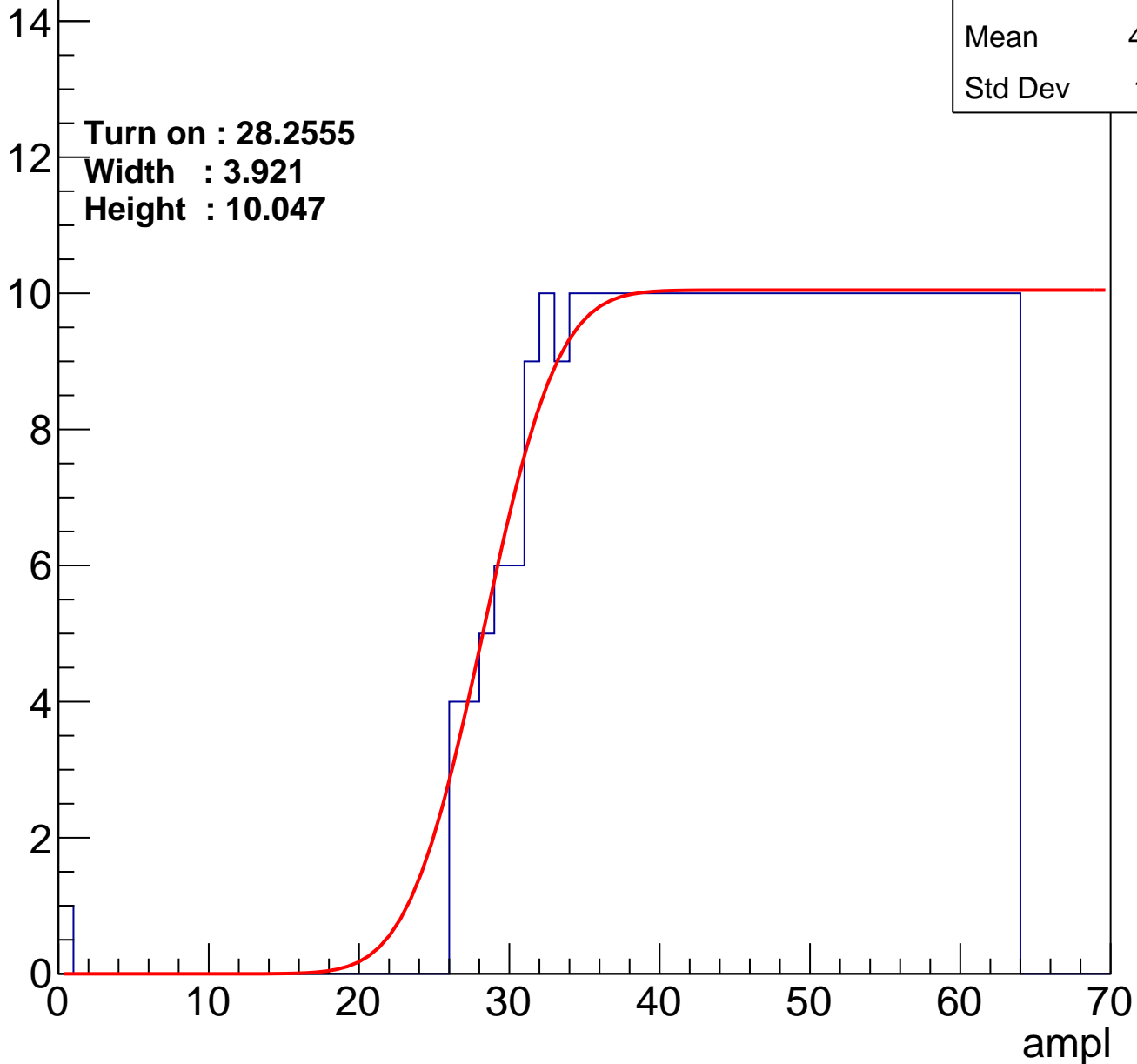
Entries	354
Mean	45.63
Std Dev	10.61

Turn on : 28.2555

Width : 3.921

Height : 10.047

Entry





# B1L101S, U26-ch23

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	375
Mean	44.42
Std Dev	11.6

Turn on : 27.1560

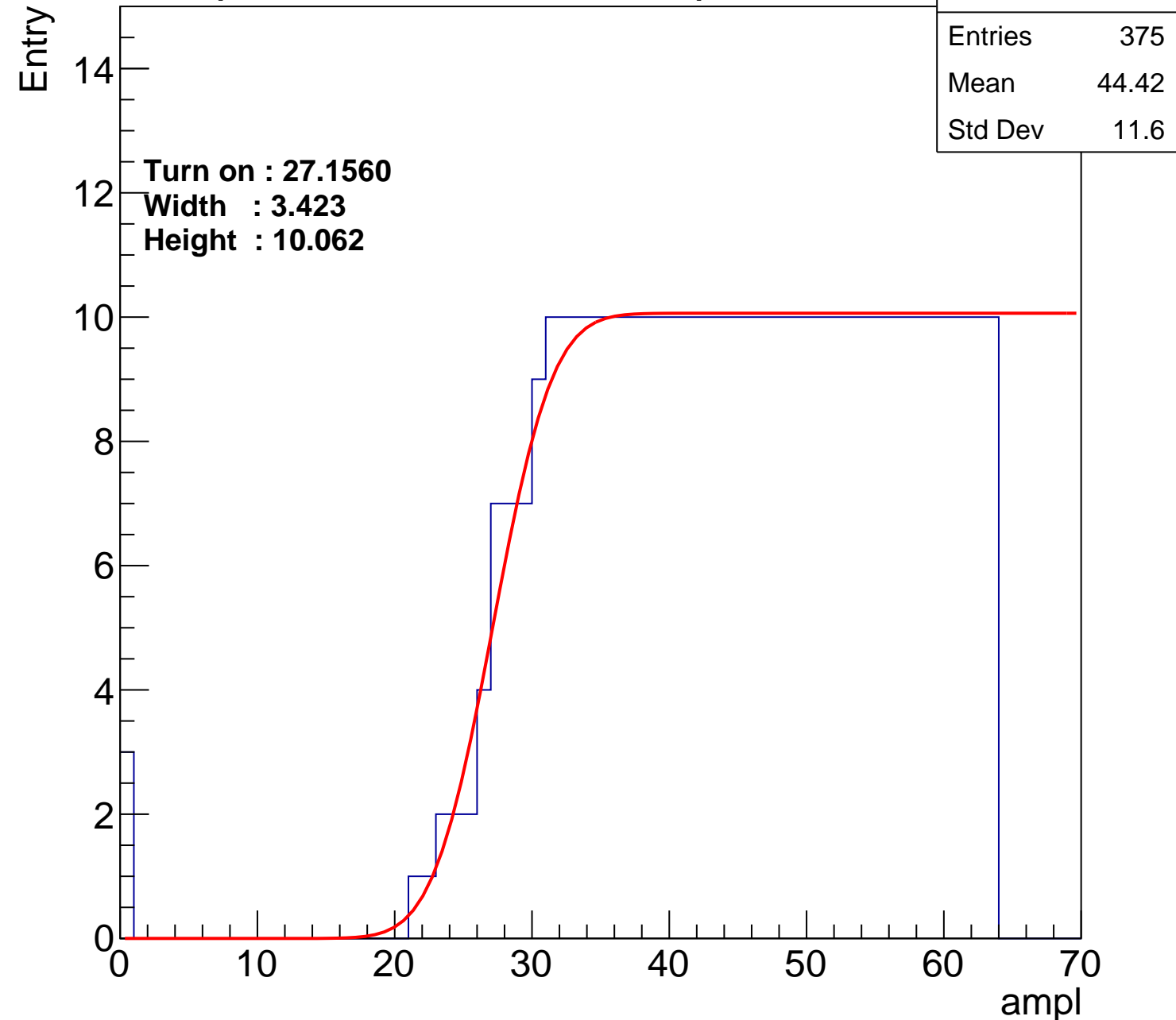
Width : 3.423

Height : 10.062

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch24

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	369
Mean	44.75
Std Dev	11.4

Turn on : 27.2527

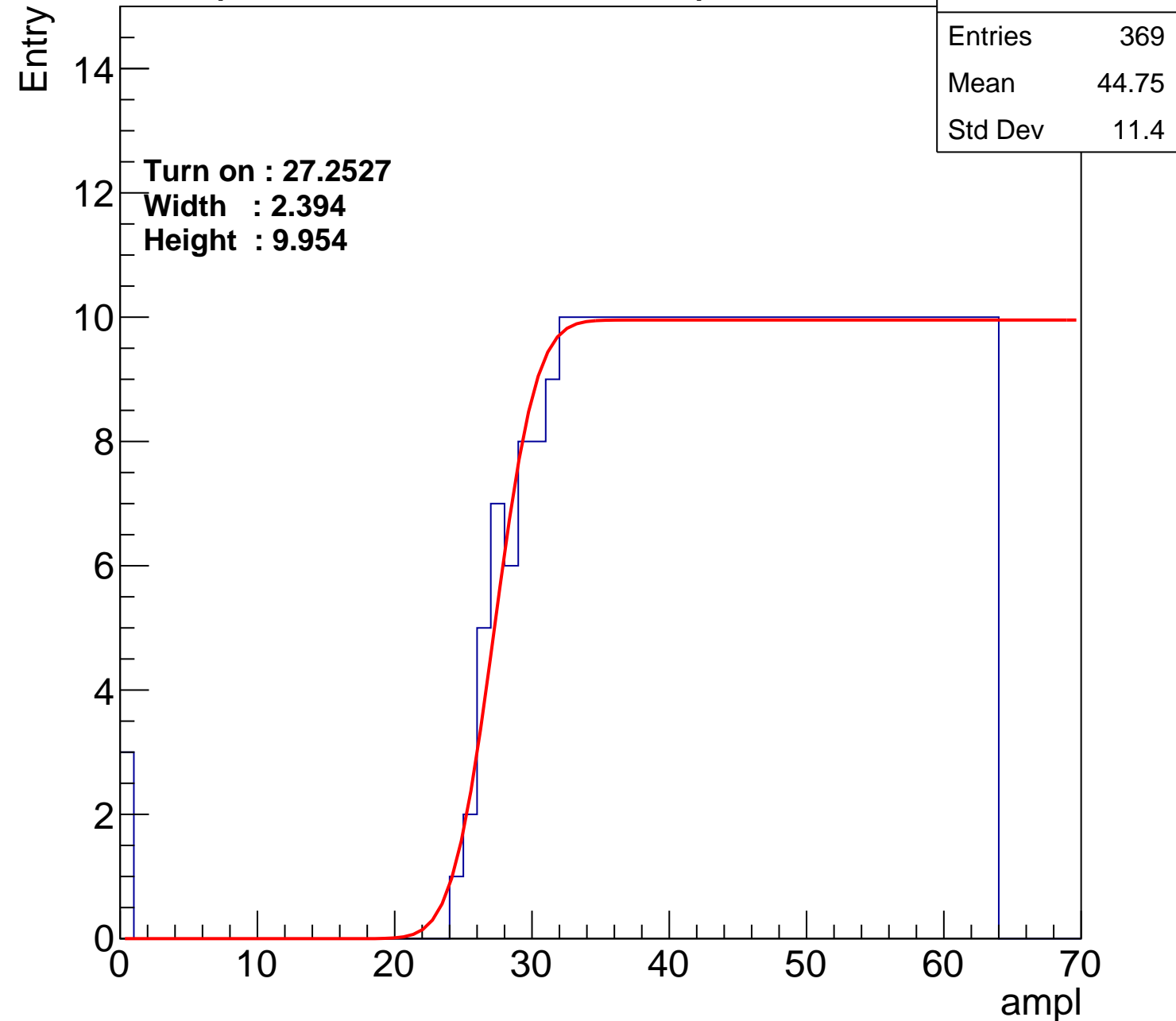
Width : 2.394

Height : 9.954

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch25

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	350
Mean	45.82
Std Dev	10.51

Turn on : 28.9929

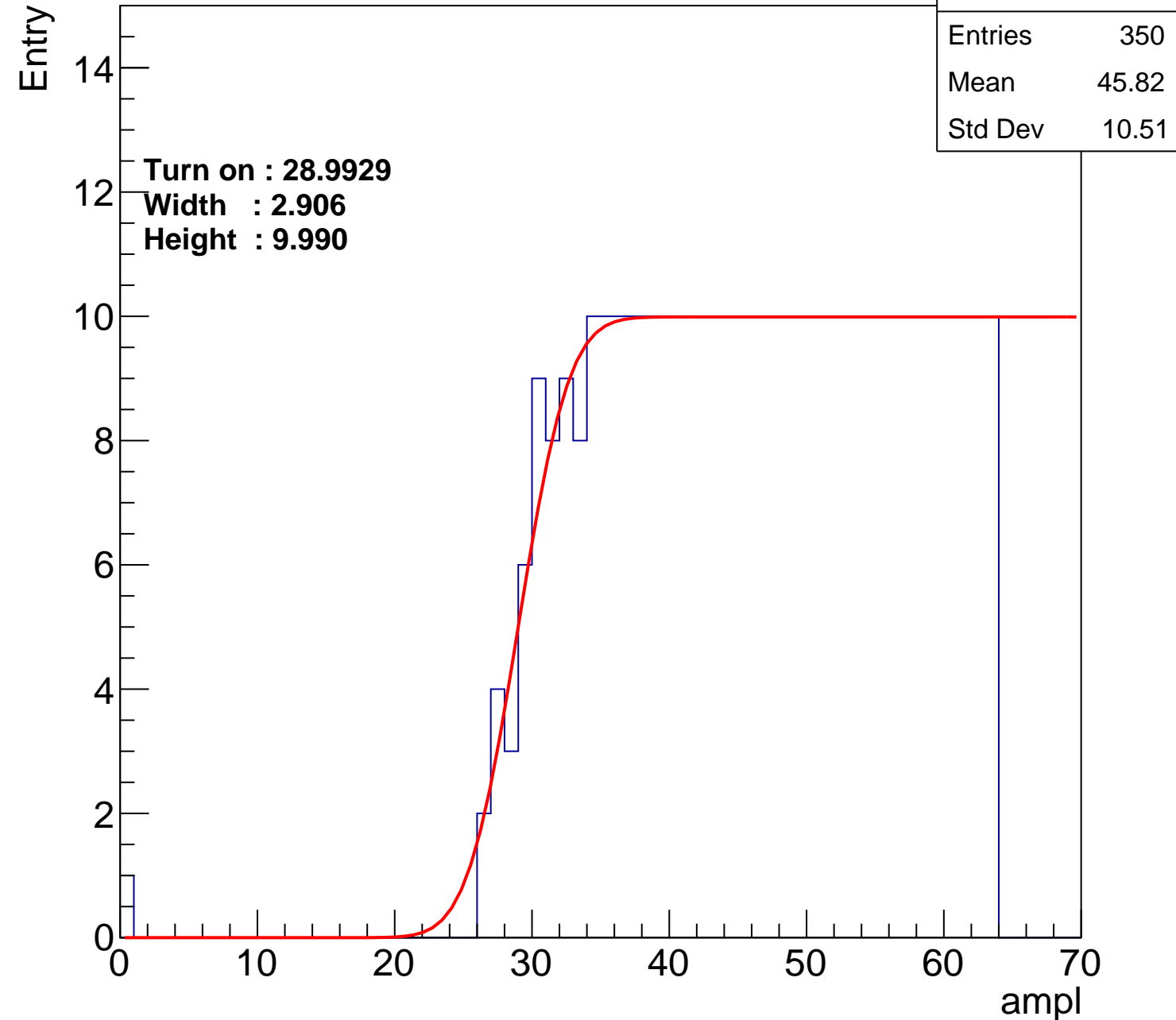
Width : 2.906

Height : 9.990

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch26

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	386
Mean	43.83
Std Dev	12.03

Turn on : 26.5702

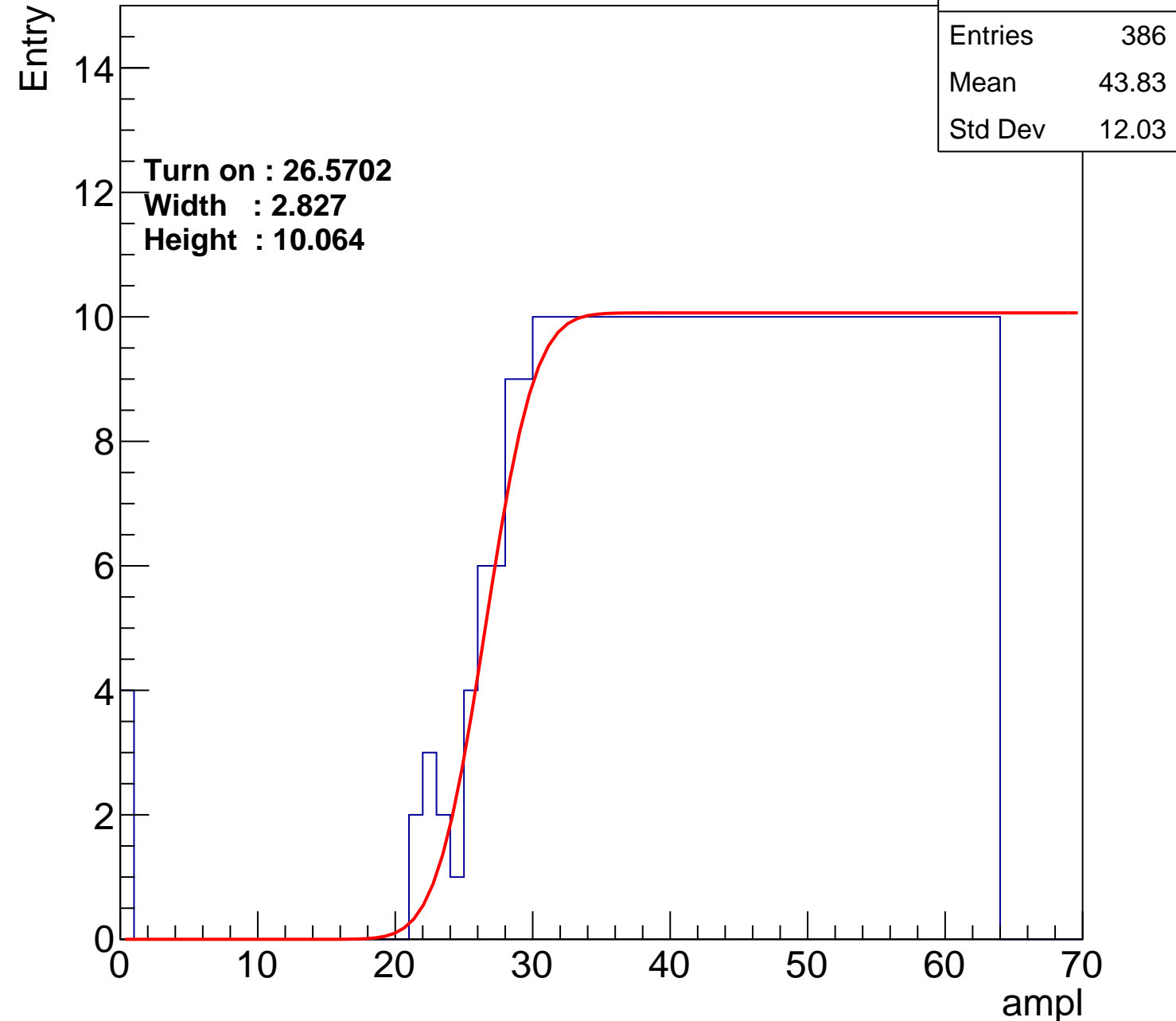
Width : 2.827

Height : 10.064

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch27

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	349
Mean	45.83
Std Dev	10.56

Turn on : 29.4875

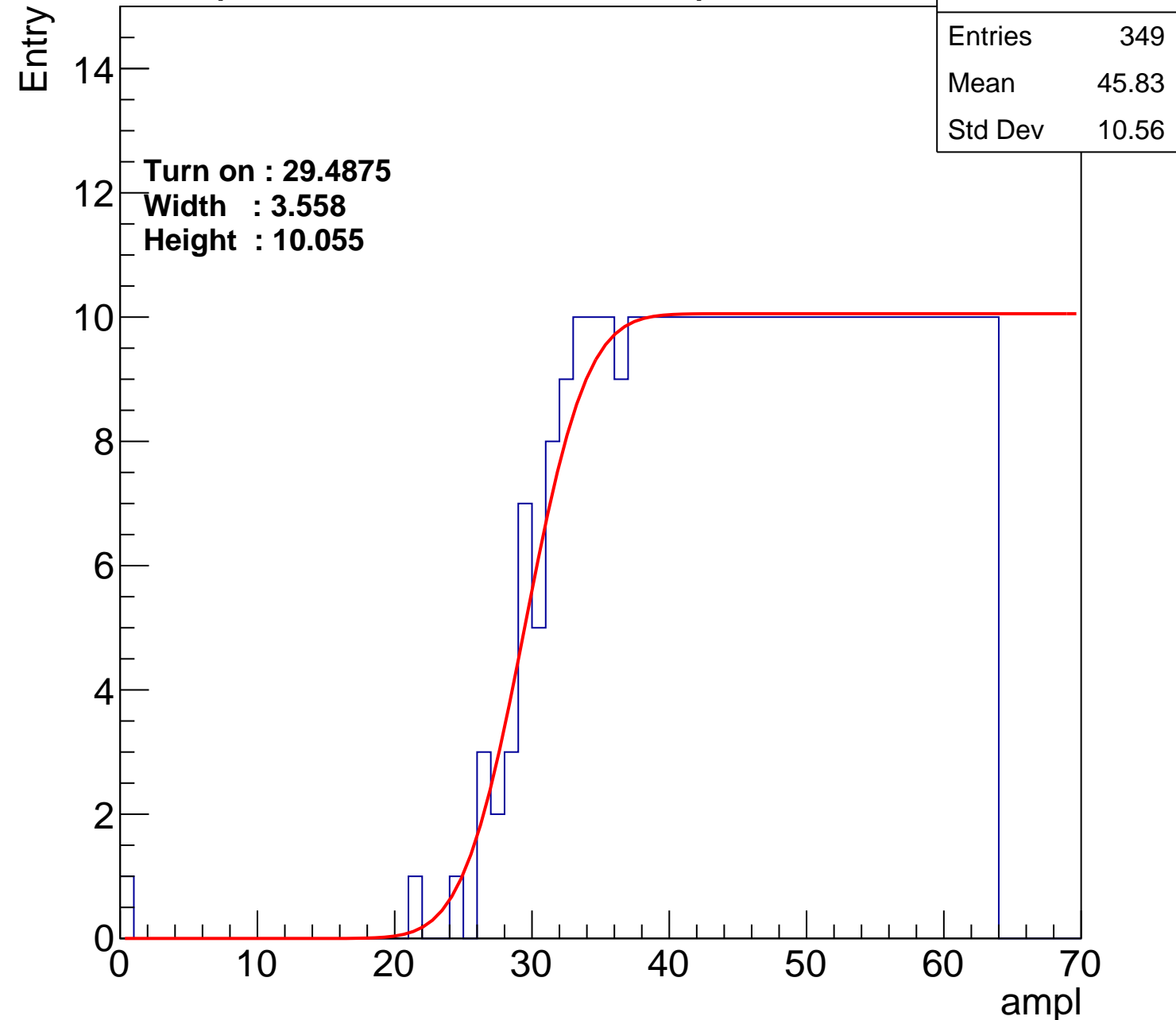
Width : 3.558

Height : 10.055

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch28

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	373
Mean	44.48
Std Dev	11.7

Turn on : 27.3941

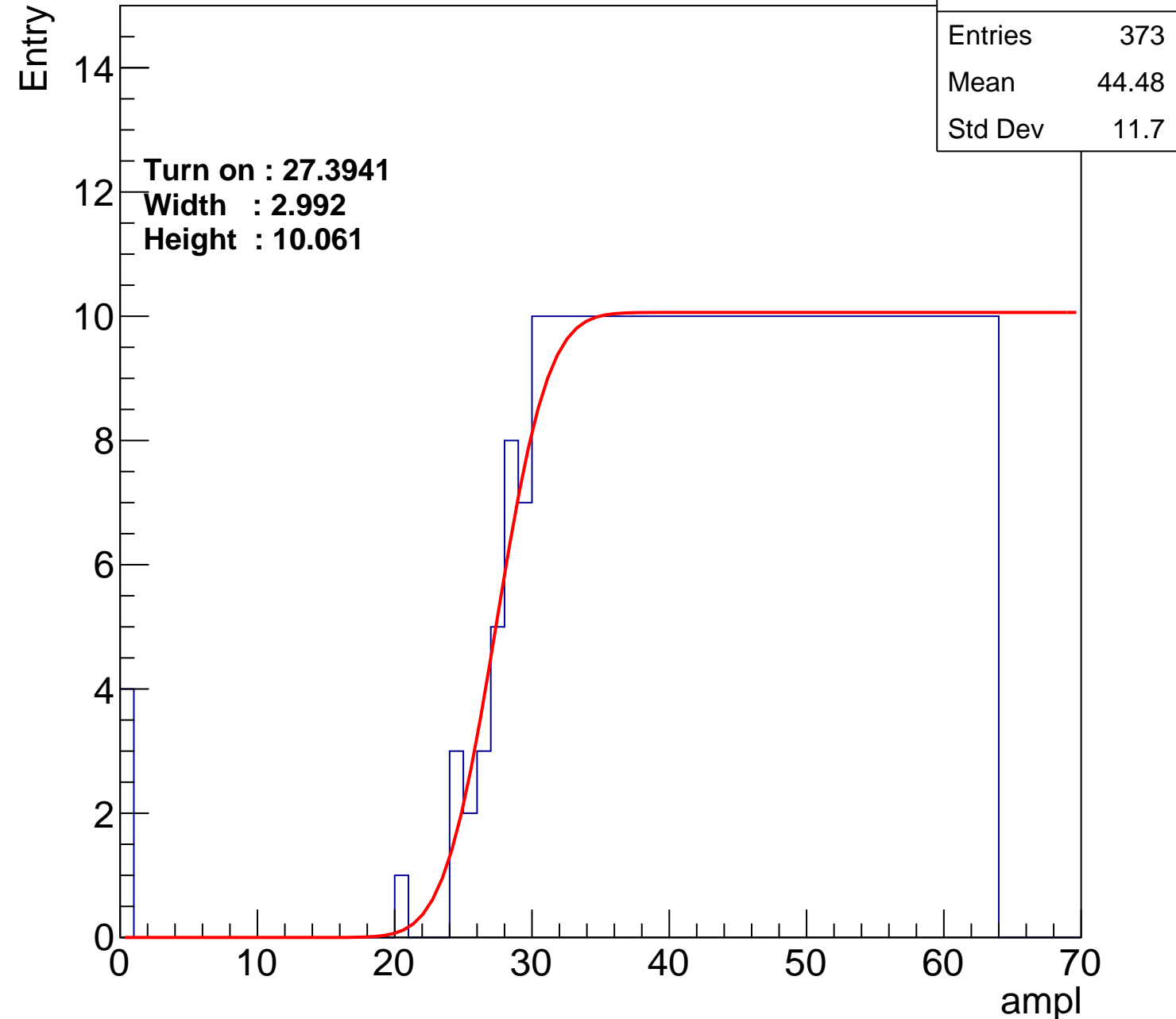
Width : 2.992

Height : 10.061

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



**calib\_packv5\_042523\_0143.root, FC#0, port D2**

Entries	368
Mean	44.8
Std Dev	11.3

Mean	44.8
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Std Dev	11.3
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**Width : 3.676**

**Height : 10.009**



# B1L101S, U26-ch30

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	390
Mean	43.67
Std Dev	11.99

Turn on : 25.4287

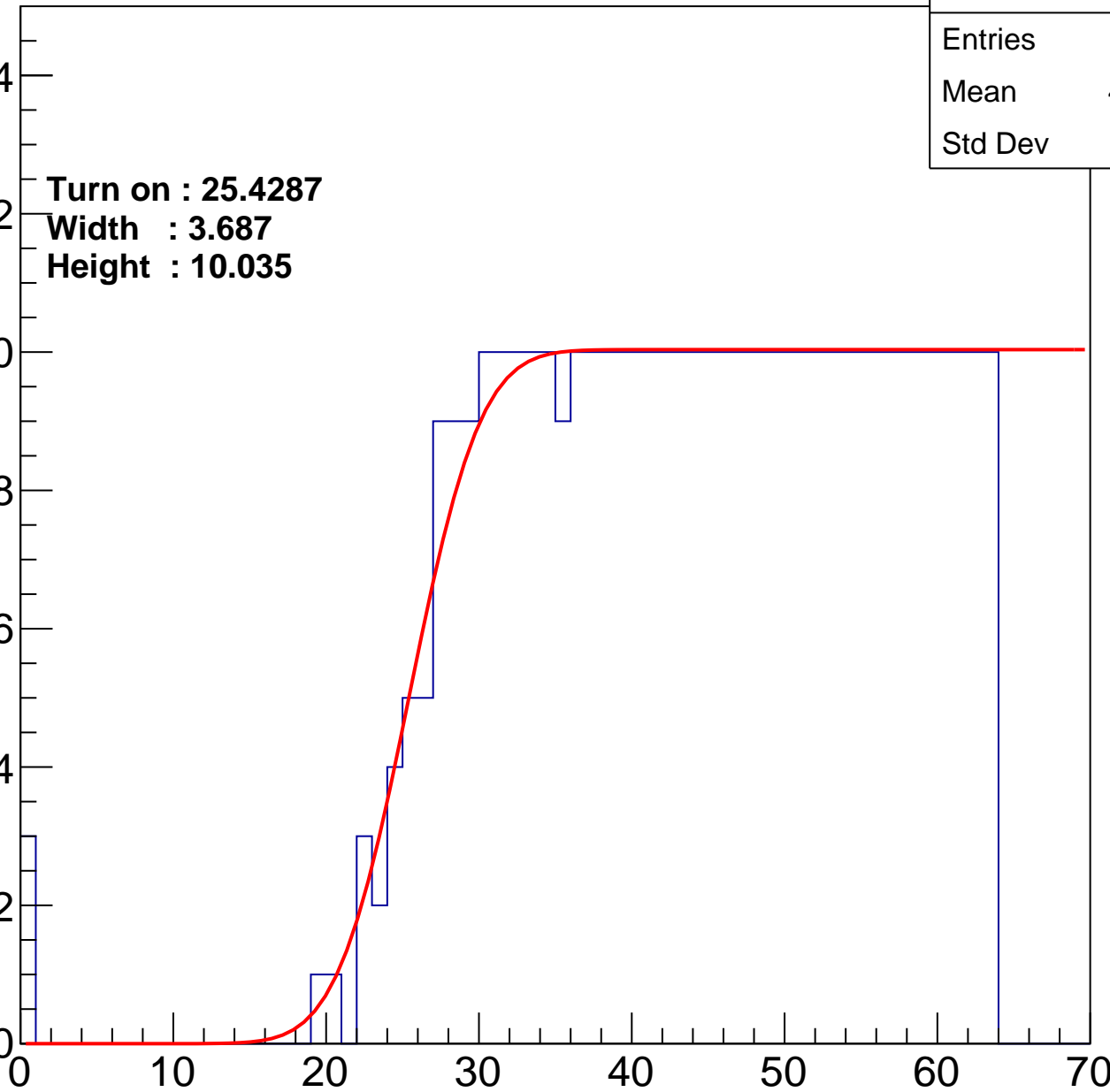
Width : 3.687

Height : 10.035

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U26-ch31

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	363
Mean	45.04
Std Dev	11.26

Turn on : 28.0281

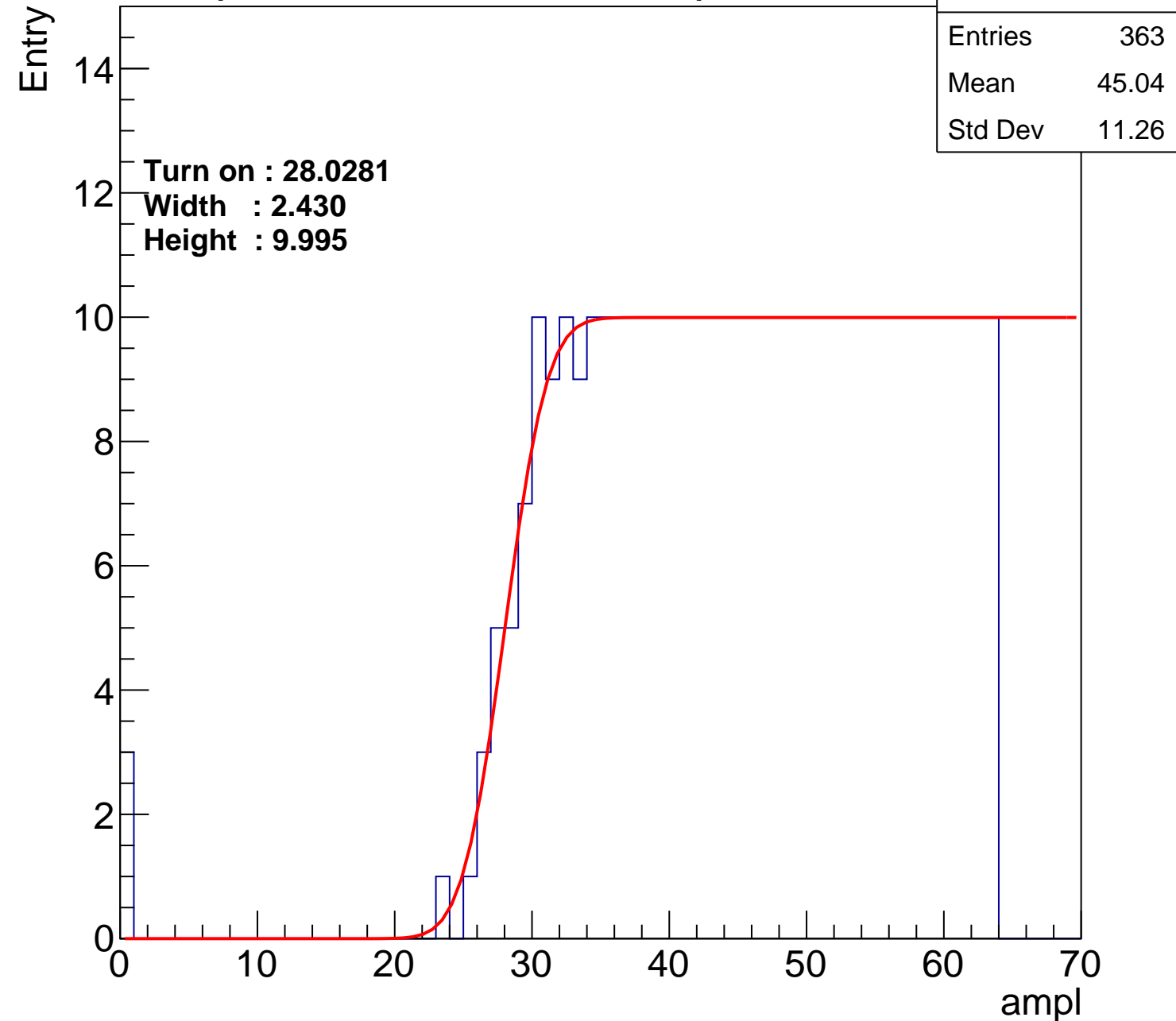
Width : 2.430

Height : 9.995

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch32

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	369
Mean	44.66
Std Dev	11.56

Turn on : 27.7583

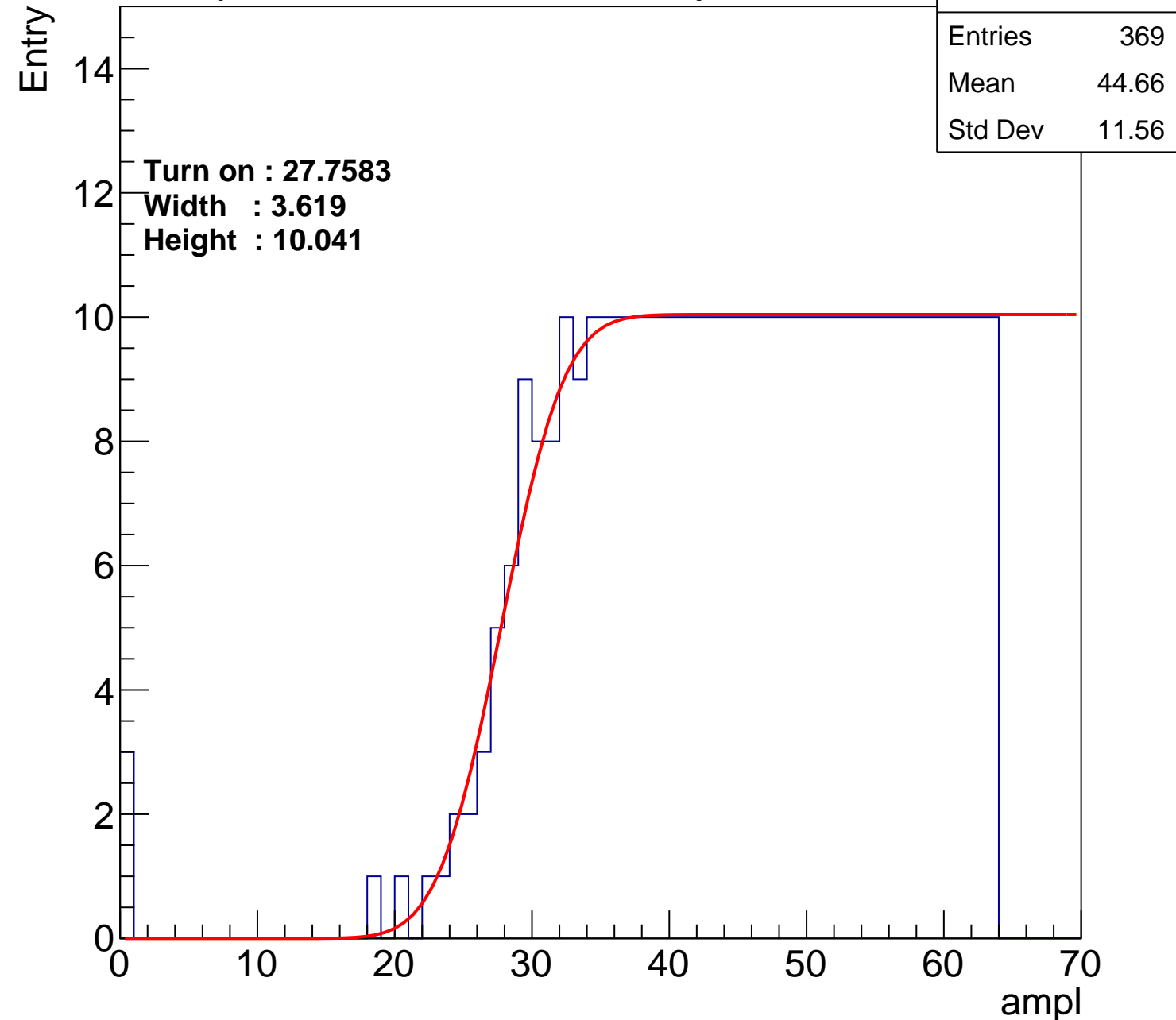
Width : 3.619

Height : 10.041

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch33

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	369
Mean	44.8
Std Dev	11.23

Turn on : 27.8534

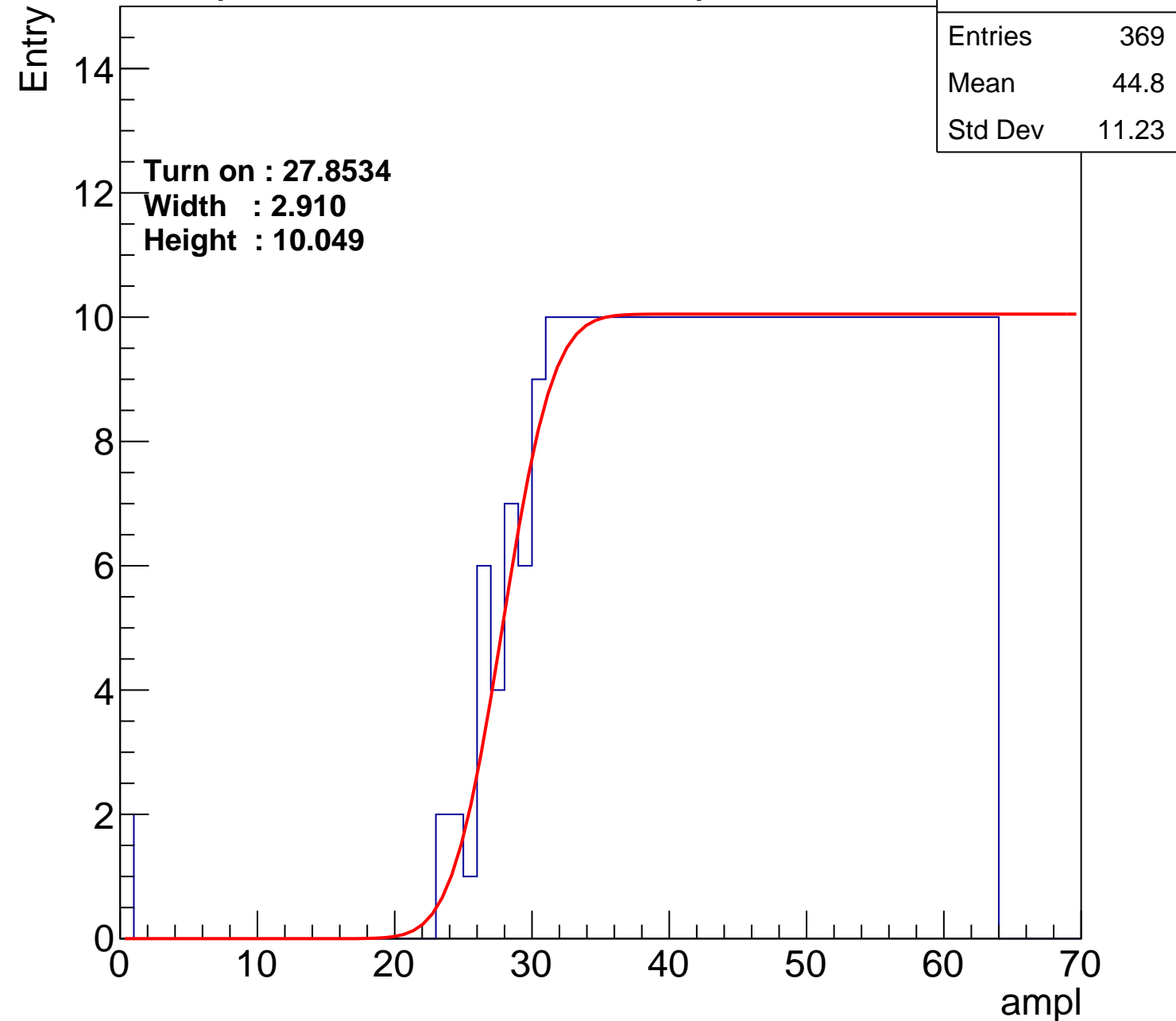
Width : 2.910

Height : 10.049

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch34

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	392
Mean	43.64
Std Dev	11.94

Turn on : 25.2842

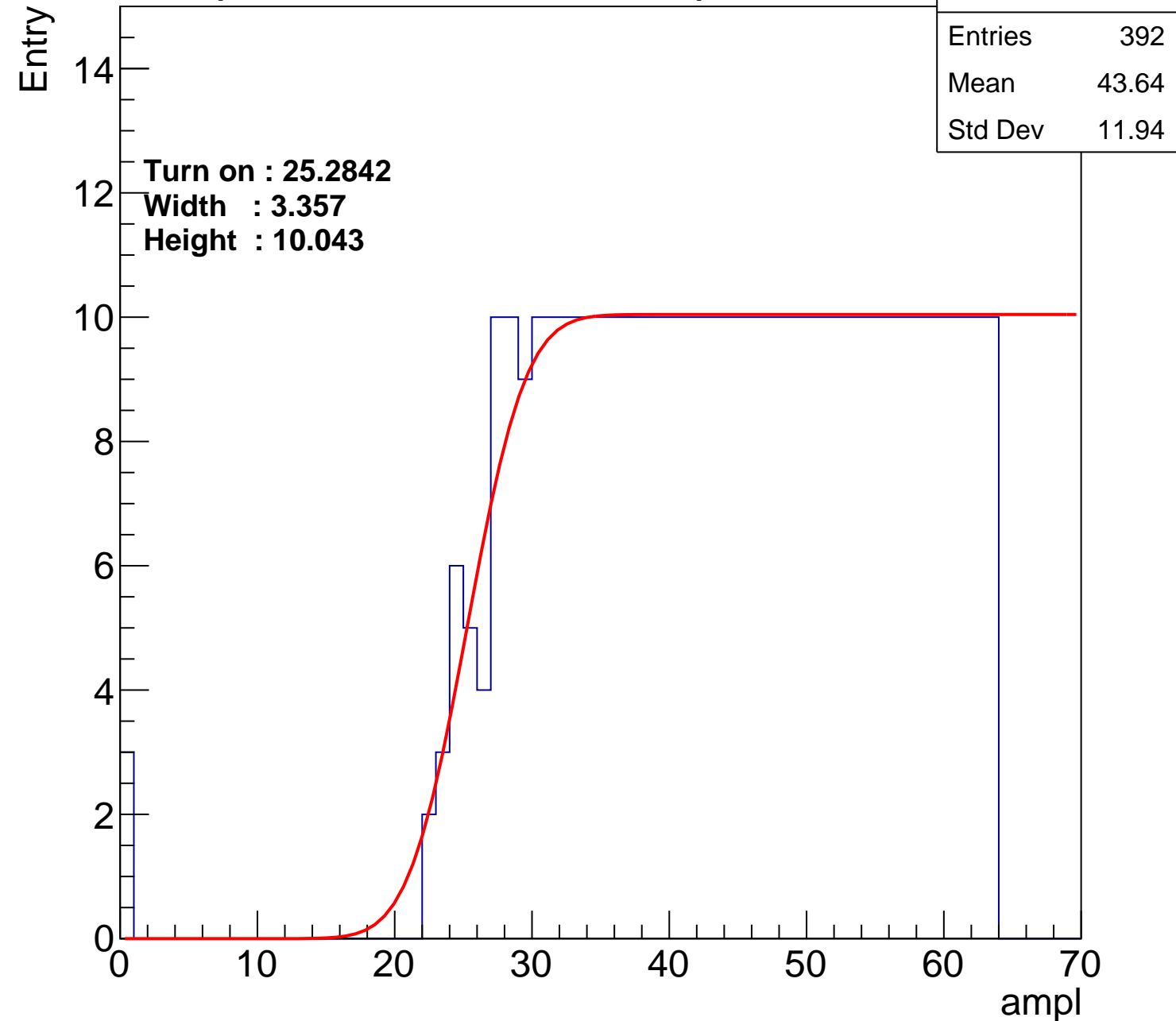
Width : 3.357

Height : 10.043

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch35

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	387
Mean	43.84
Std Dev	11.88

Turn on : 25.5297

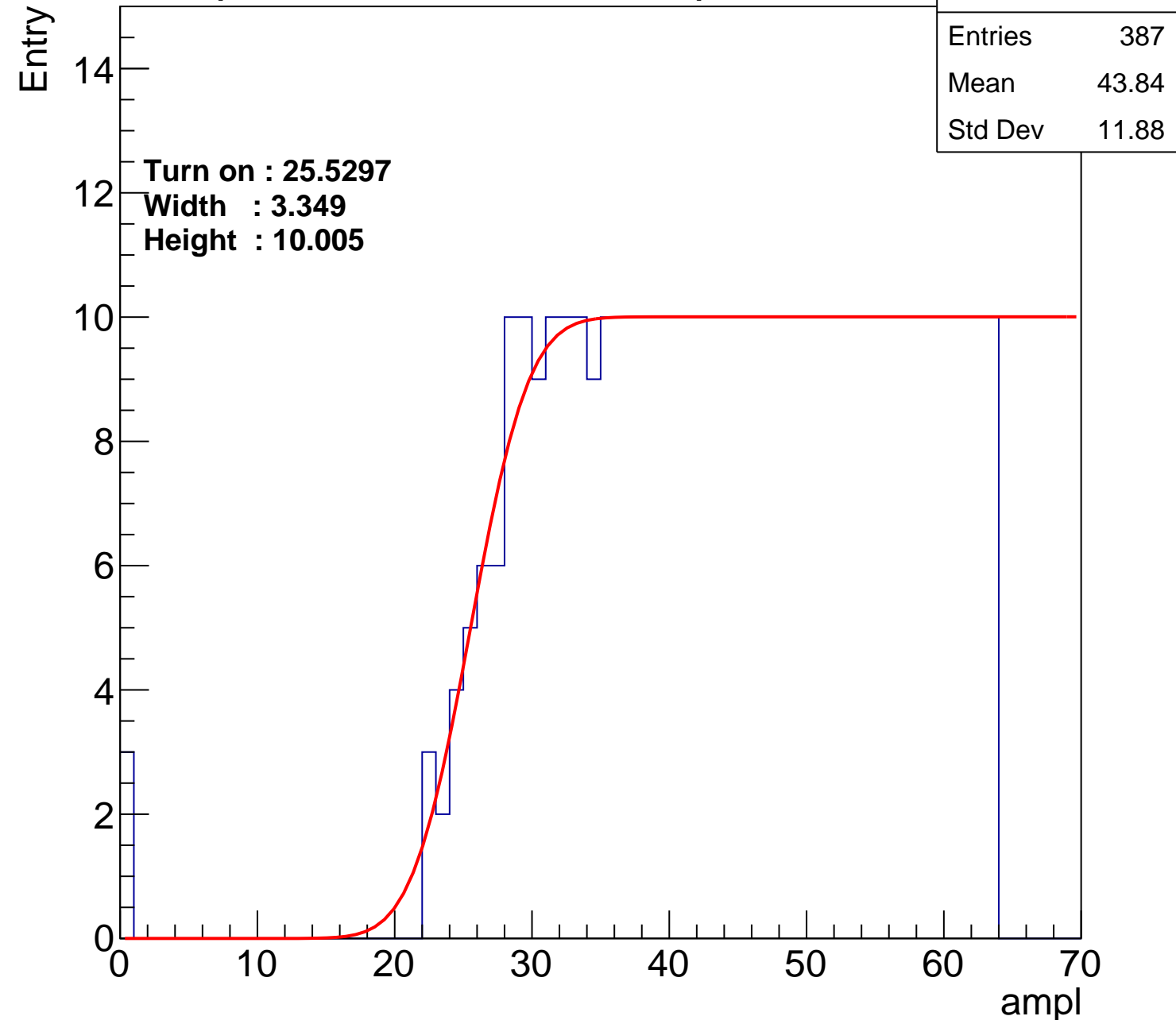
Width : 3.349

Height : 10.005

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch36

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	381
Mean	44.12
Std Dev	11.75

**Turn on : 26.7516**

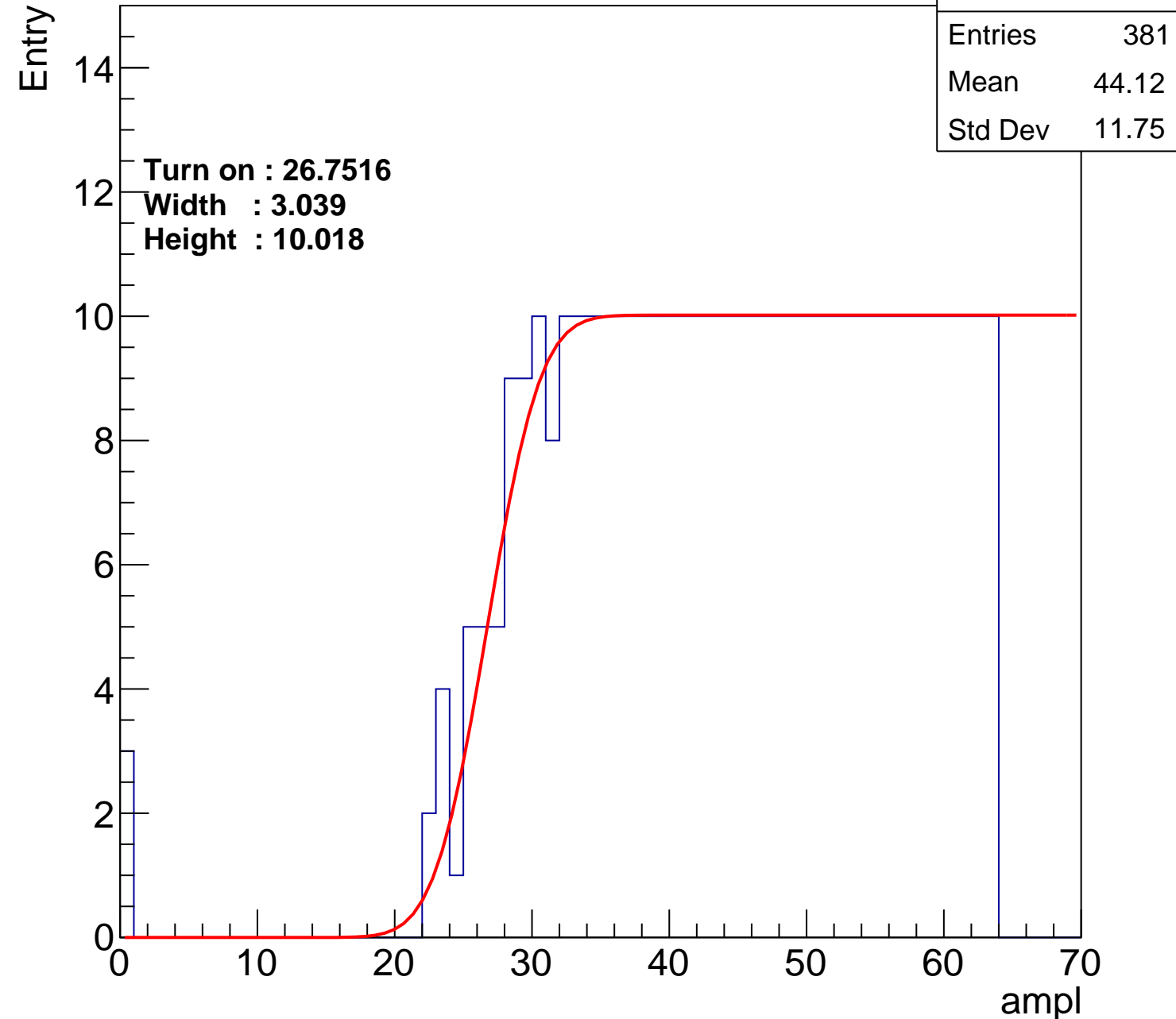
**Width : 3.039**

**Height : 10.018**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch37

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	341
Mean	46.08
Std Dev	10.8

Turn on : 30.3690

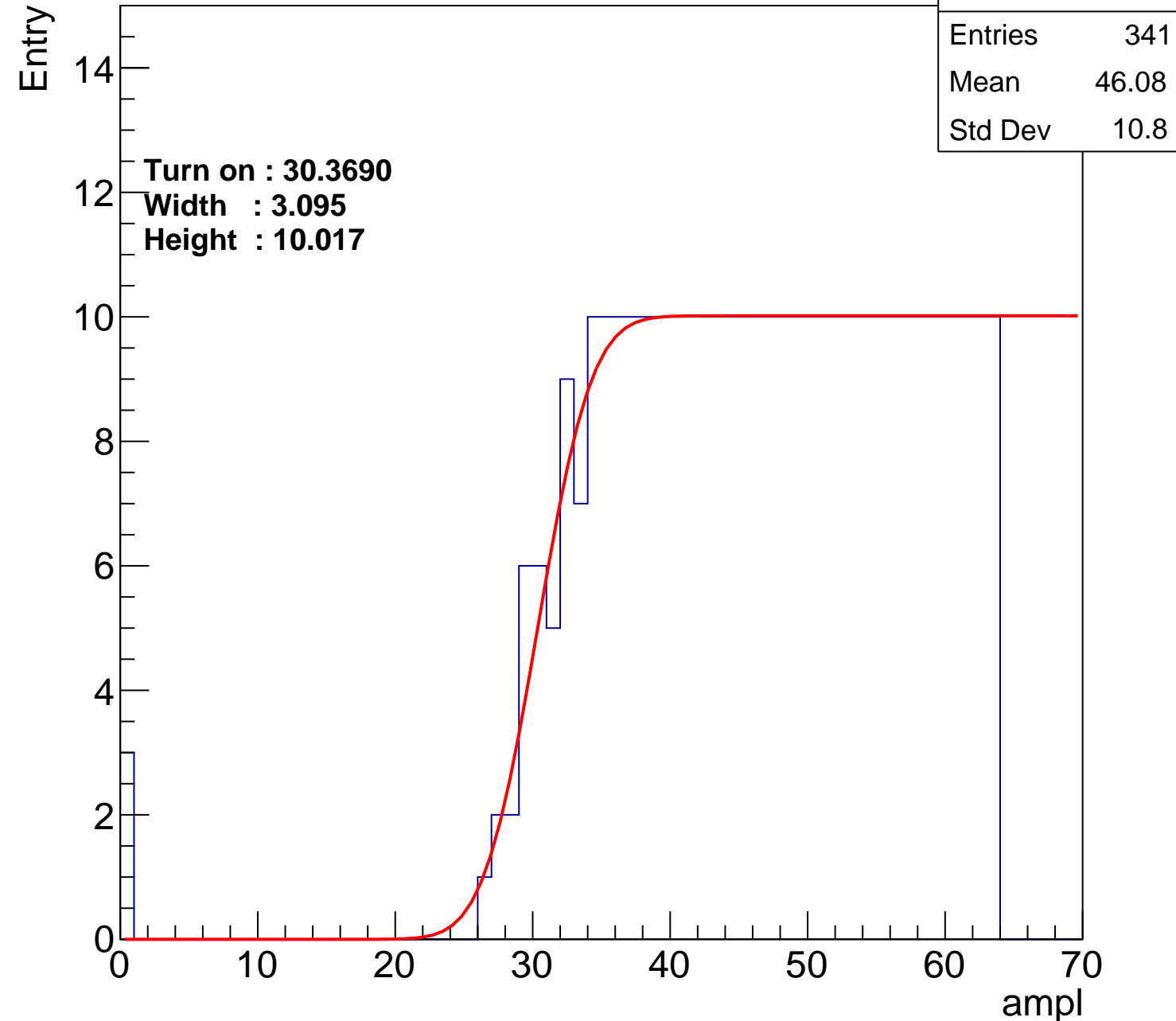
Width : 3.095

Height : 10.017

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch38

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	371
Mean	44.62
Std Dev	11.5

Turn on : 27.0019

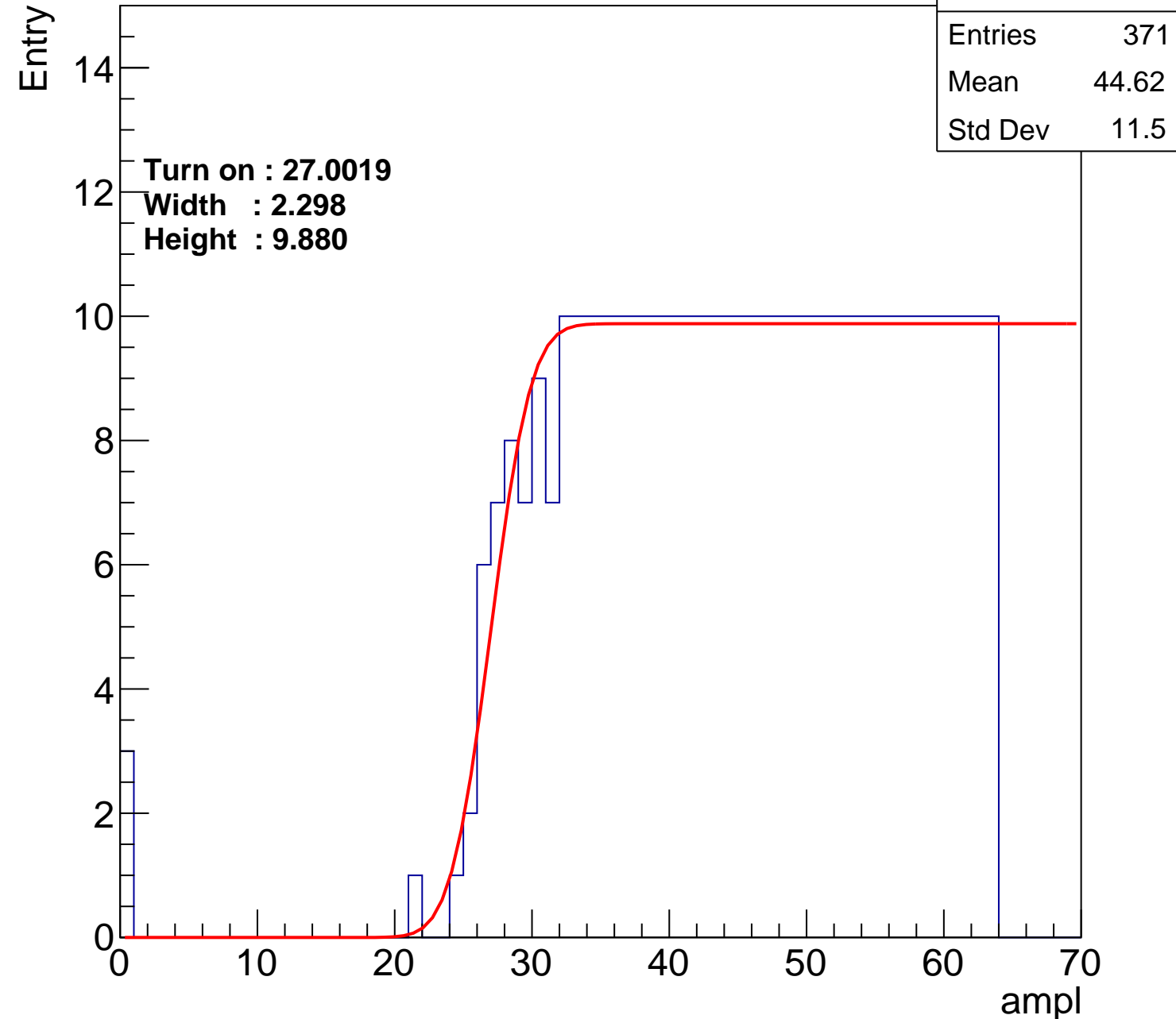
Width : 2.298

Height : 9.880

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U26-ch39

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	366
Mean	45.01
Std Dev	10.98

Turn on : 27.8996

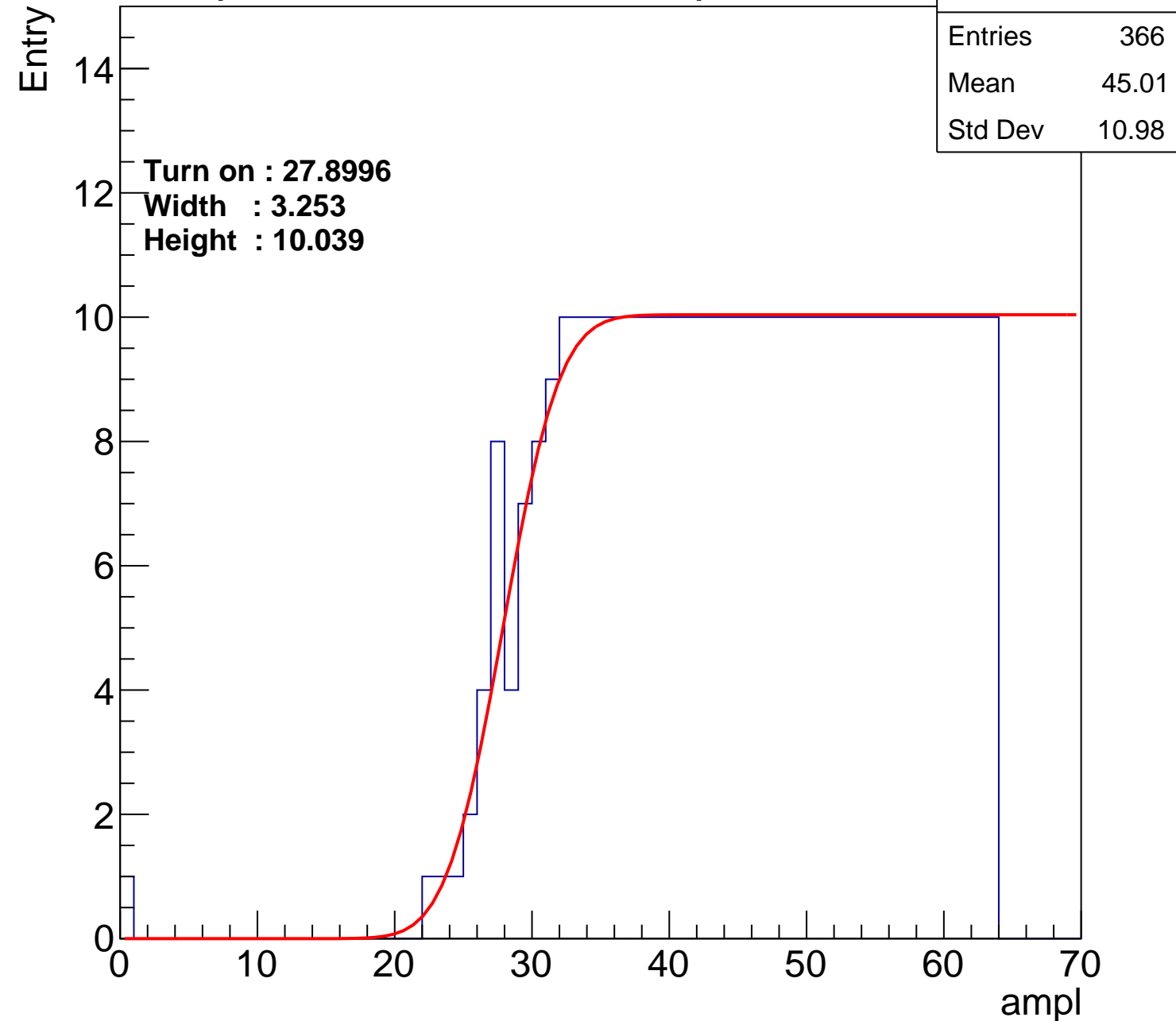
Width : 3.253

Height : 10.039

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch40

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	363
Mean	44.74
Std Dev	12.06

Turn on : 28.6444

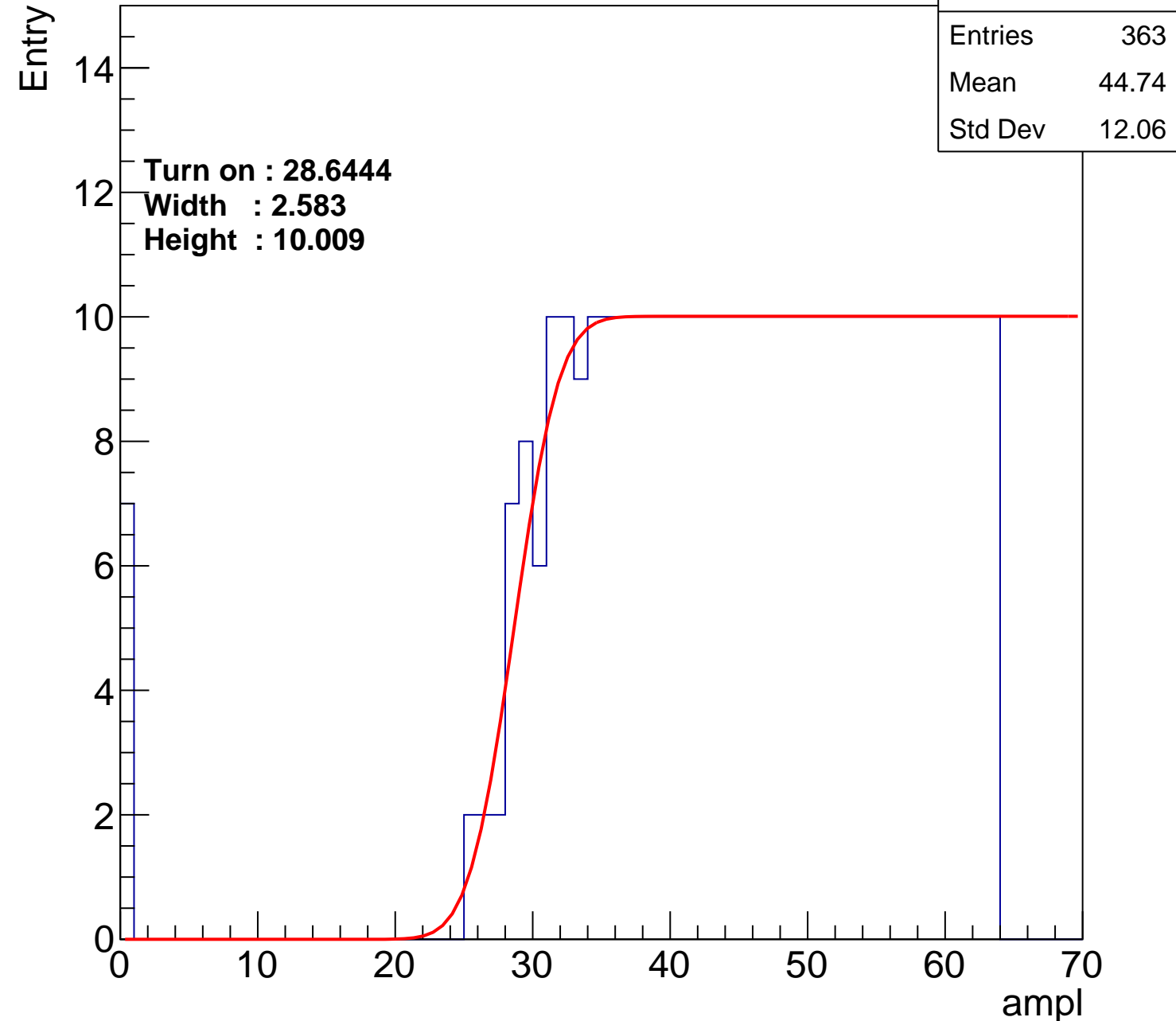
Width : 2.583

Height : 10.009

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch41

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	372
Mean	44.66
Std Dev	11.3

**Turn on : 26.8832**

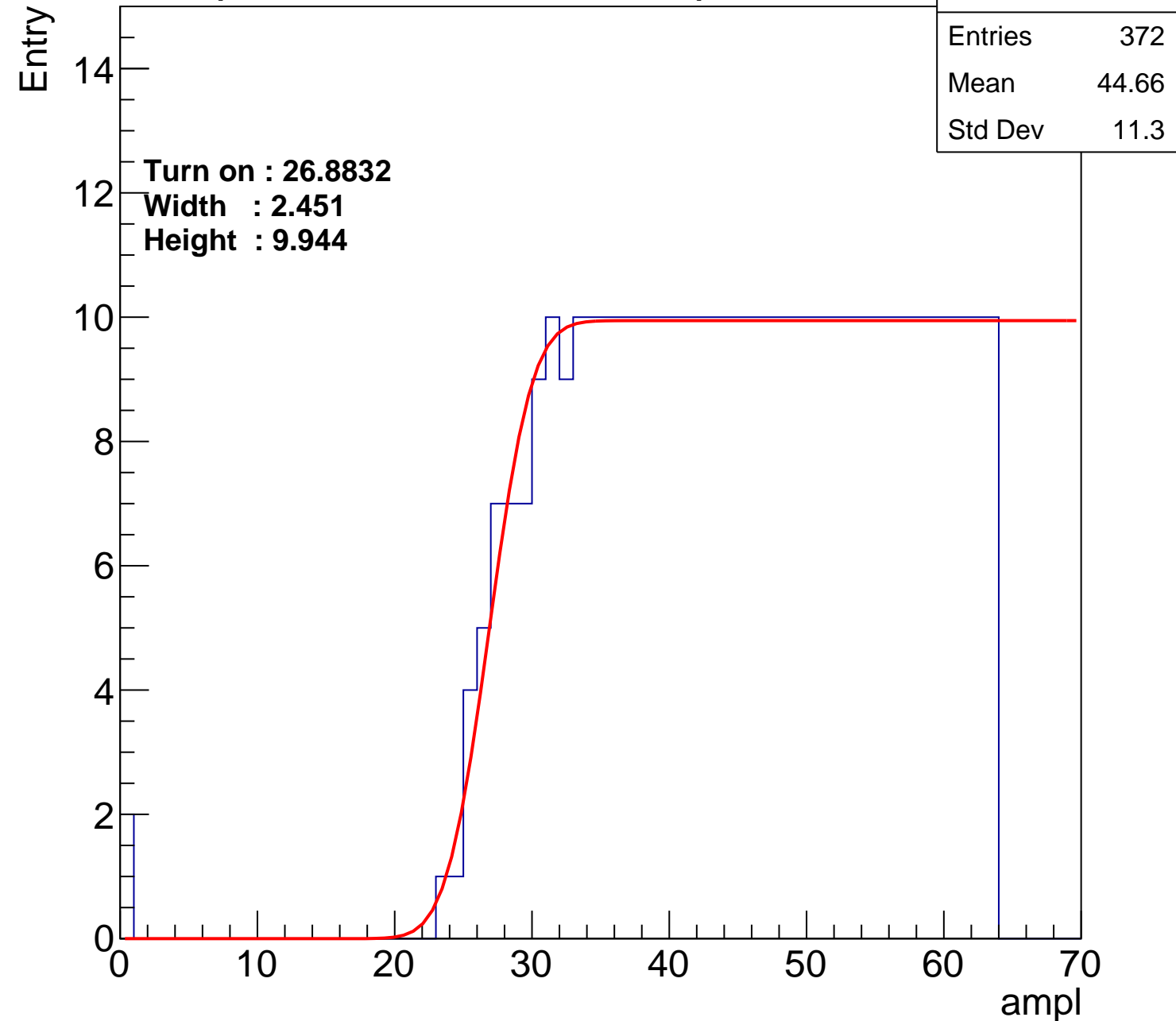
**Width : 2.451**

**Height : 9.944**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch42

calib\_packv5\_042523\_0143.root, FC#0, port D2

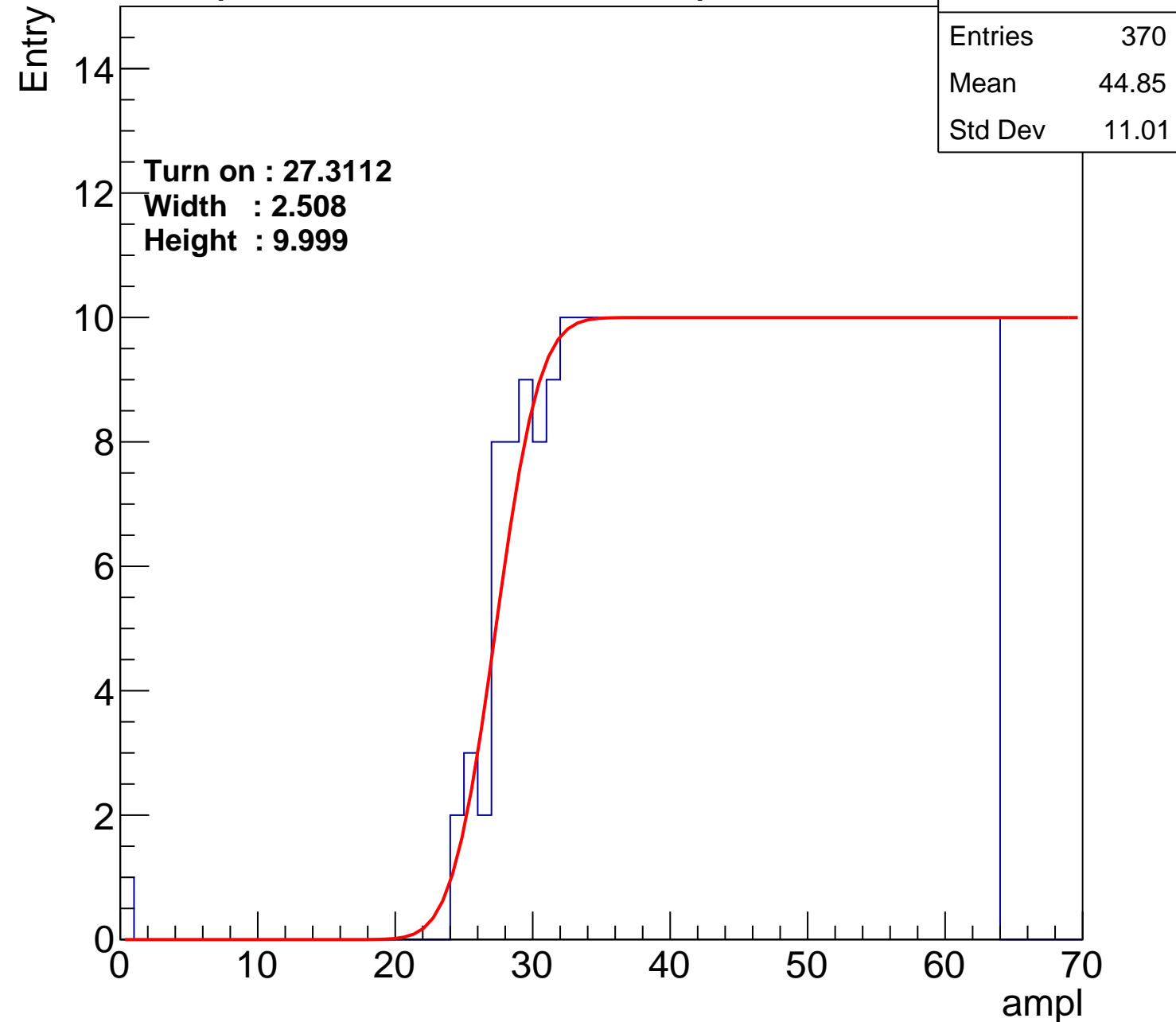
Entry

14  
12  
10  
8  
6  
4  
2  
0

Turn on : 27.3112  
Width : 2.508  
Height : 9.999

Entries	370
Mean	44.85
Std Dev	11.01

ampl



# B1L101S, U26-ch43

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	375
Mean	44.47
Std Dev	11.45

Turn on : 26.9952

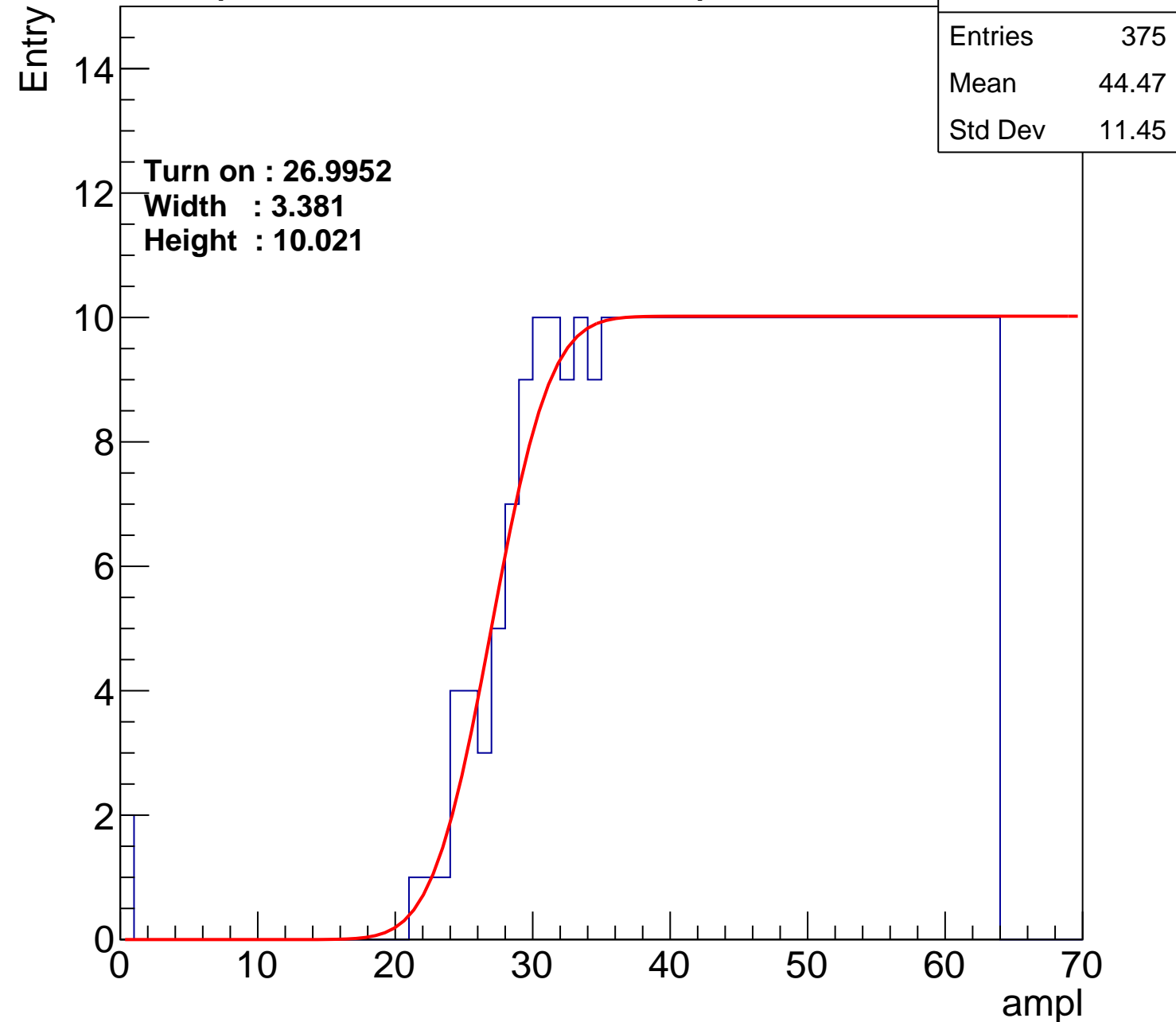
Width : 3.381

Height : 10.021

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch44

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	369
Mean	44.62
Std Dev	11.7

Turn on : 27.7309

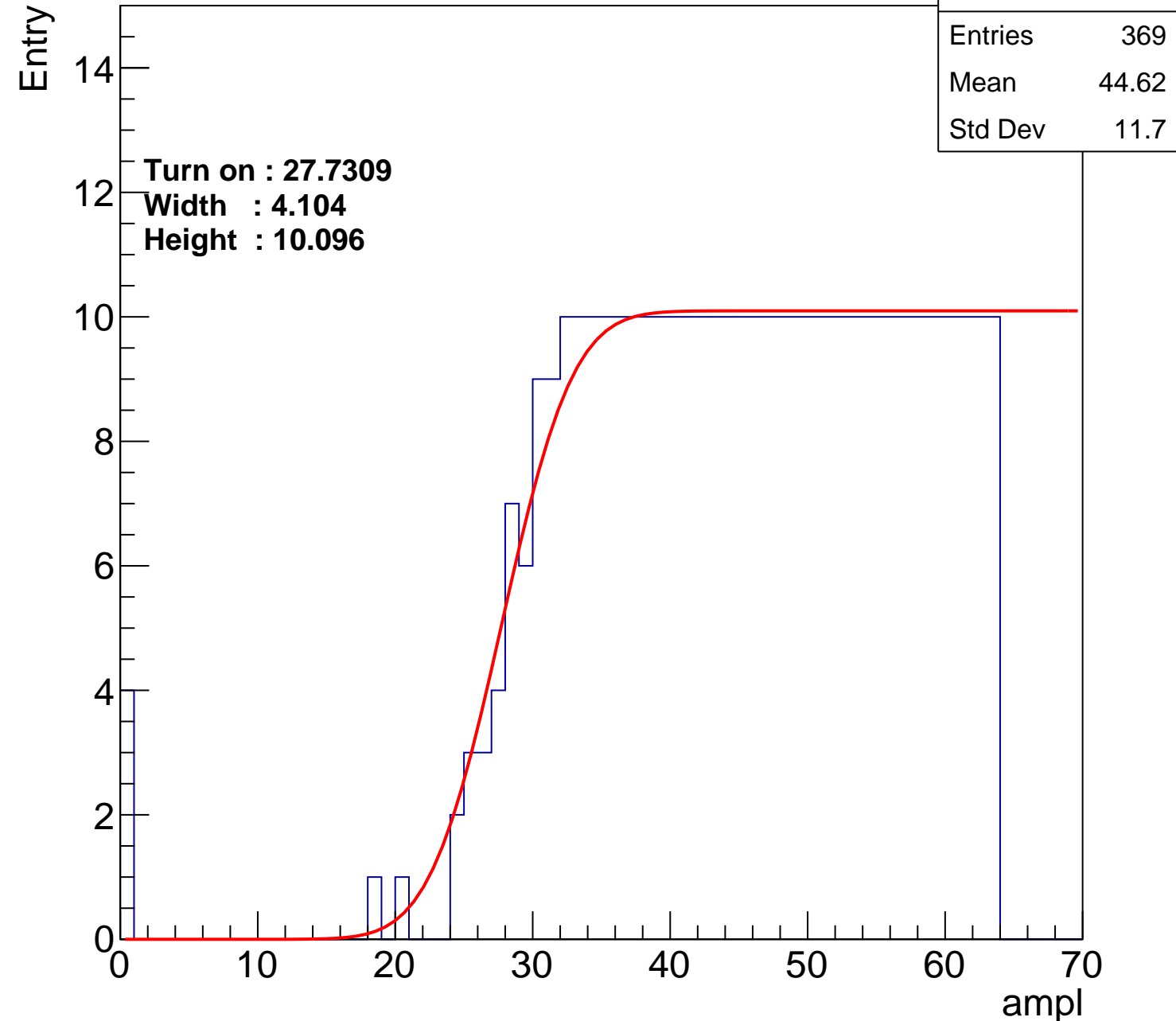
Width : 4.104

Height : 10.096

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch45

calib\_packv5\_042523\_0143.root, FC#0, port D2

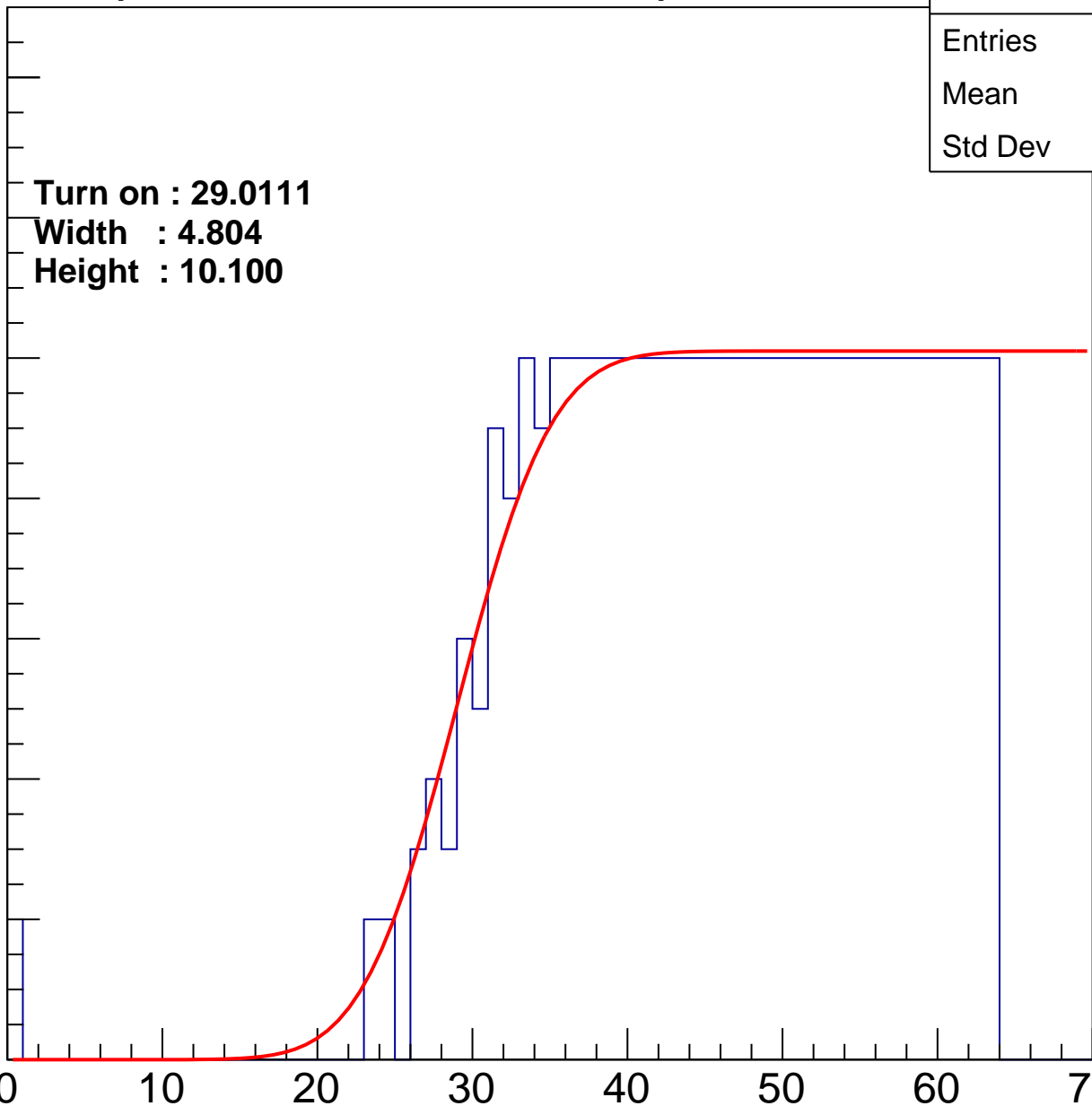
Entry

14  
12  
10  
8  
6  
4  
2  
0

Turn on : 29.0111  
Width : 4.804  
Height : 10.100

Entries	353
Mean	45.52
Std Dev	10.95

ampl



# B1L101S, U26-ch46

calib\_packv5\_042523\_0143.root, FC#0, port D2

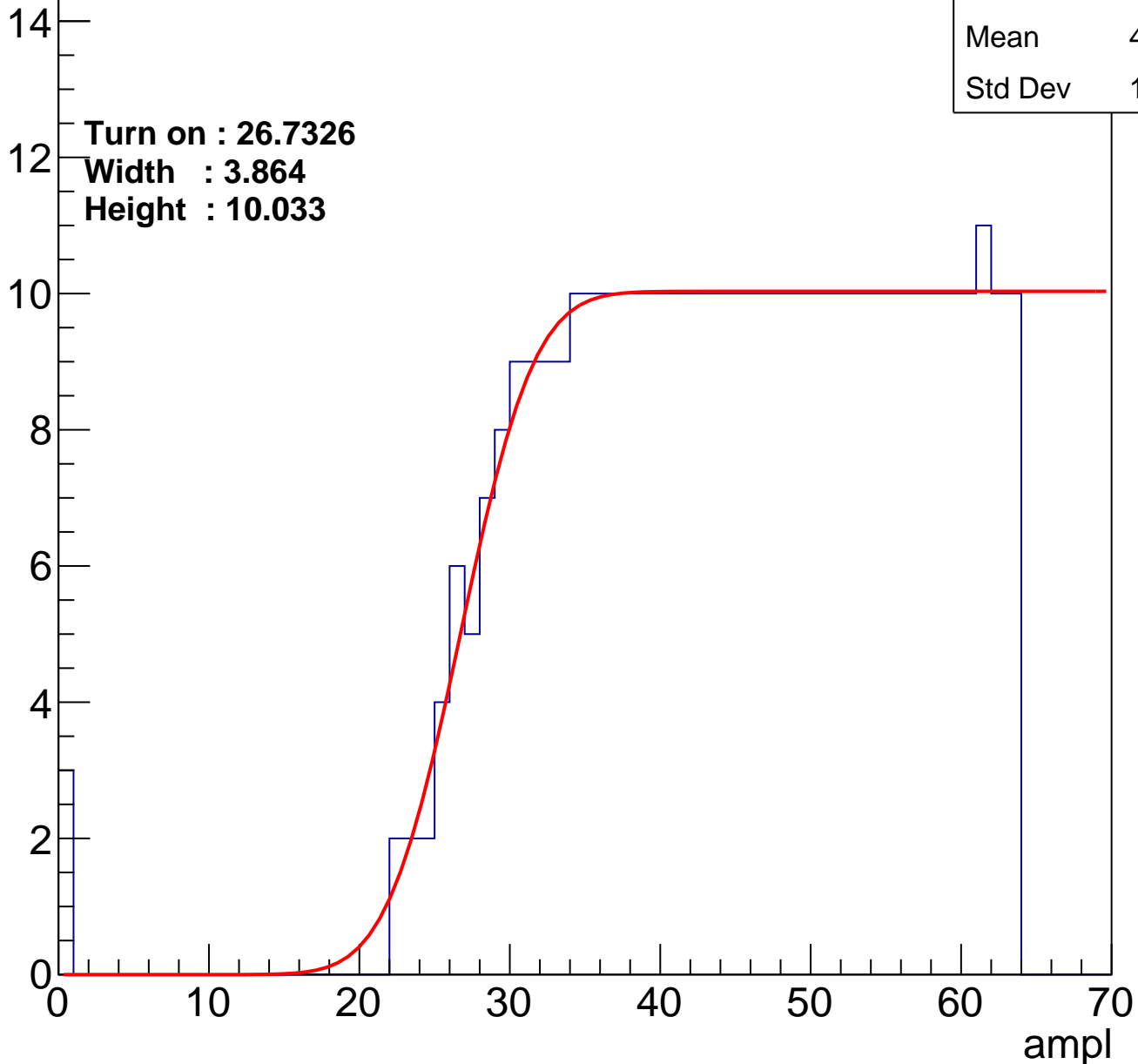
Entries	376
Mean	44.42
Std Dev	11.68

**Turn on : 26.7326**

**Width : 3.864**

**Height : 10.033**

Entry





# B1L101S, U26-ch47

calib\_packv5\_042523\_0143.root, FC#0, port D2

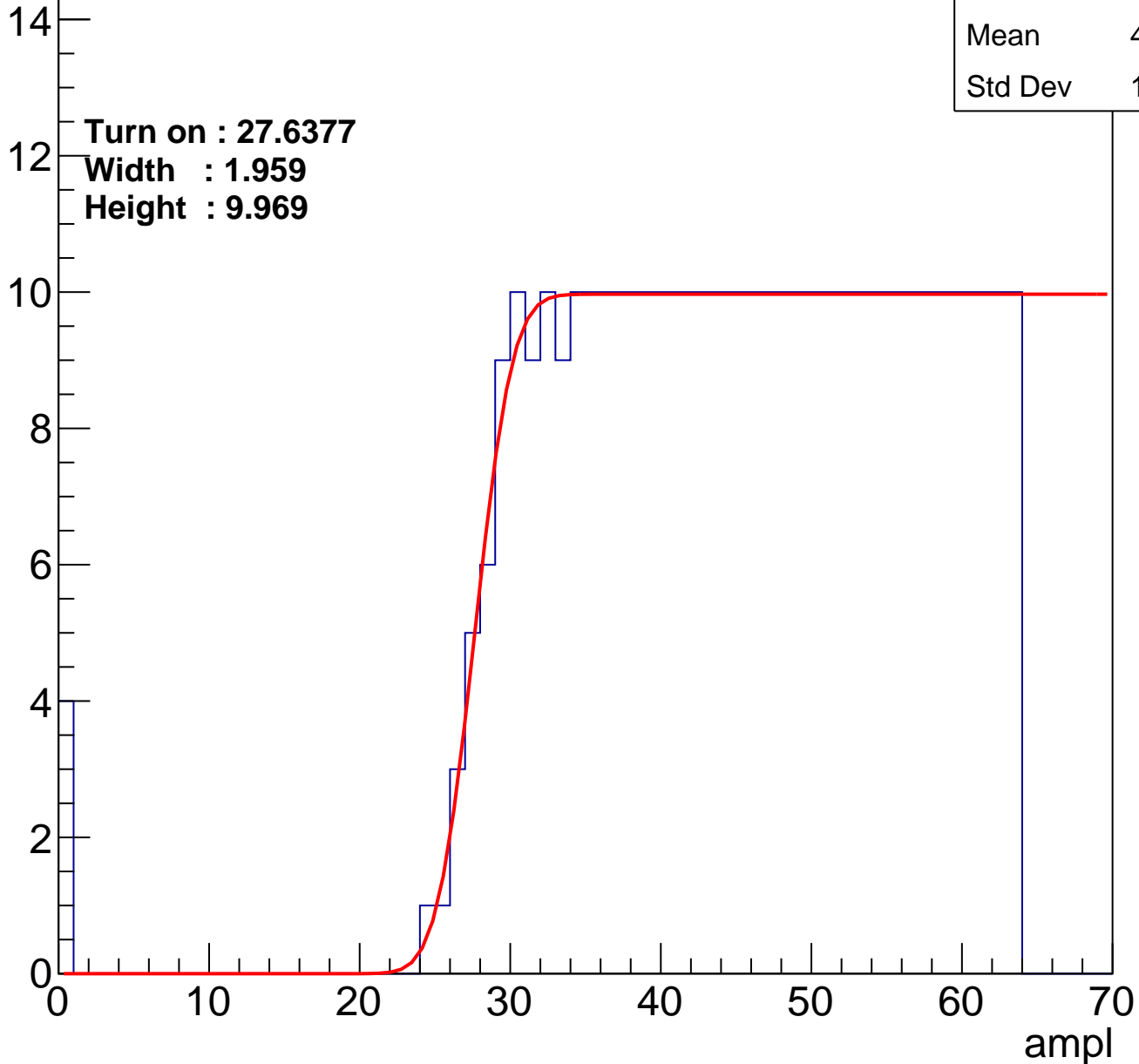
Entries	367
Mean	44.79
Std Dev	11.53

Turn on : 27.6377

Width : 1.959

Height : 9.969

Entry



# B1L101S, U26-ch48

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	370
Mean	44.81
Std Dev	11.09

**Turn on : 26.7728**

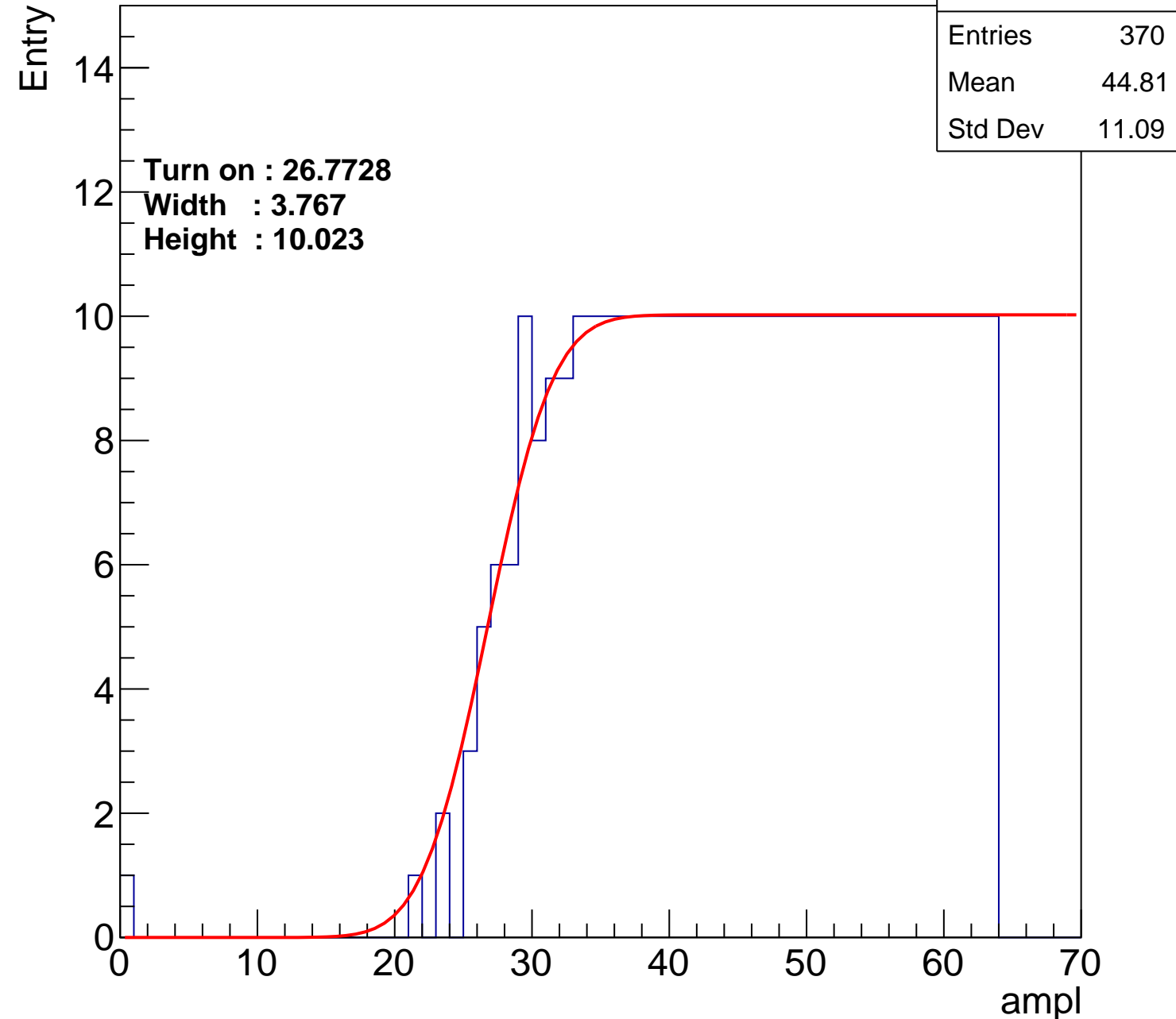
**Width : 3.767**

**Height : 10.023**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch49

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	373
Mean	44.68
Std Dev	11.14

Turn on : 26.7434

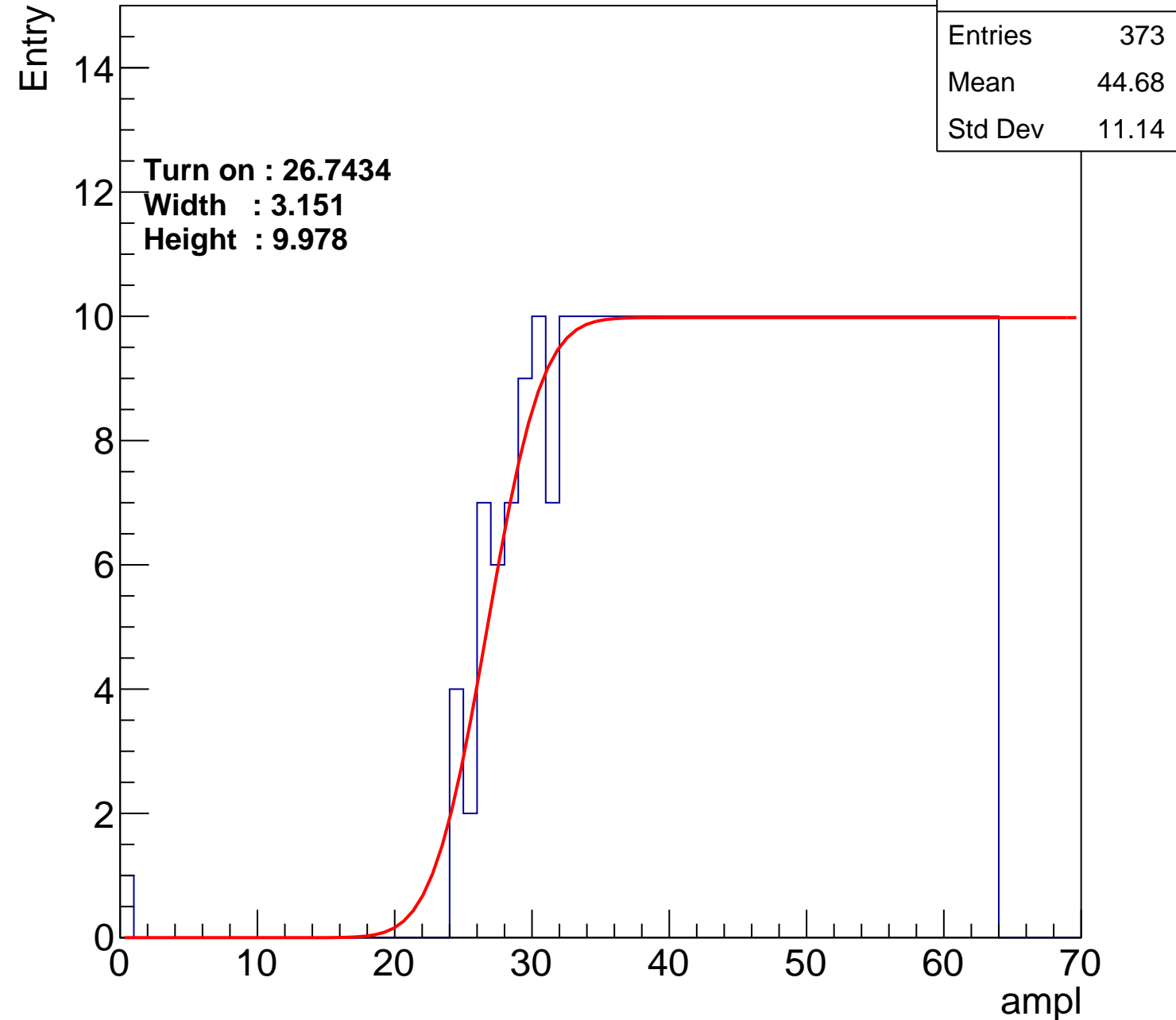
Width : 3.151

Height : 9.978

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch50

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	367
Mean	44.82
Std Dev	11.4

Turn on : 28.0052

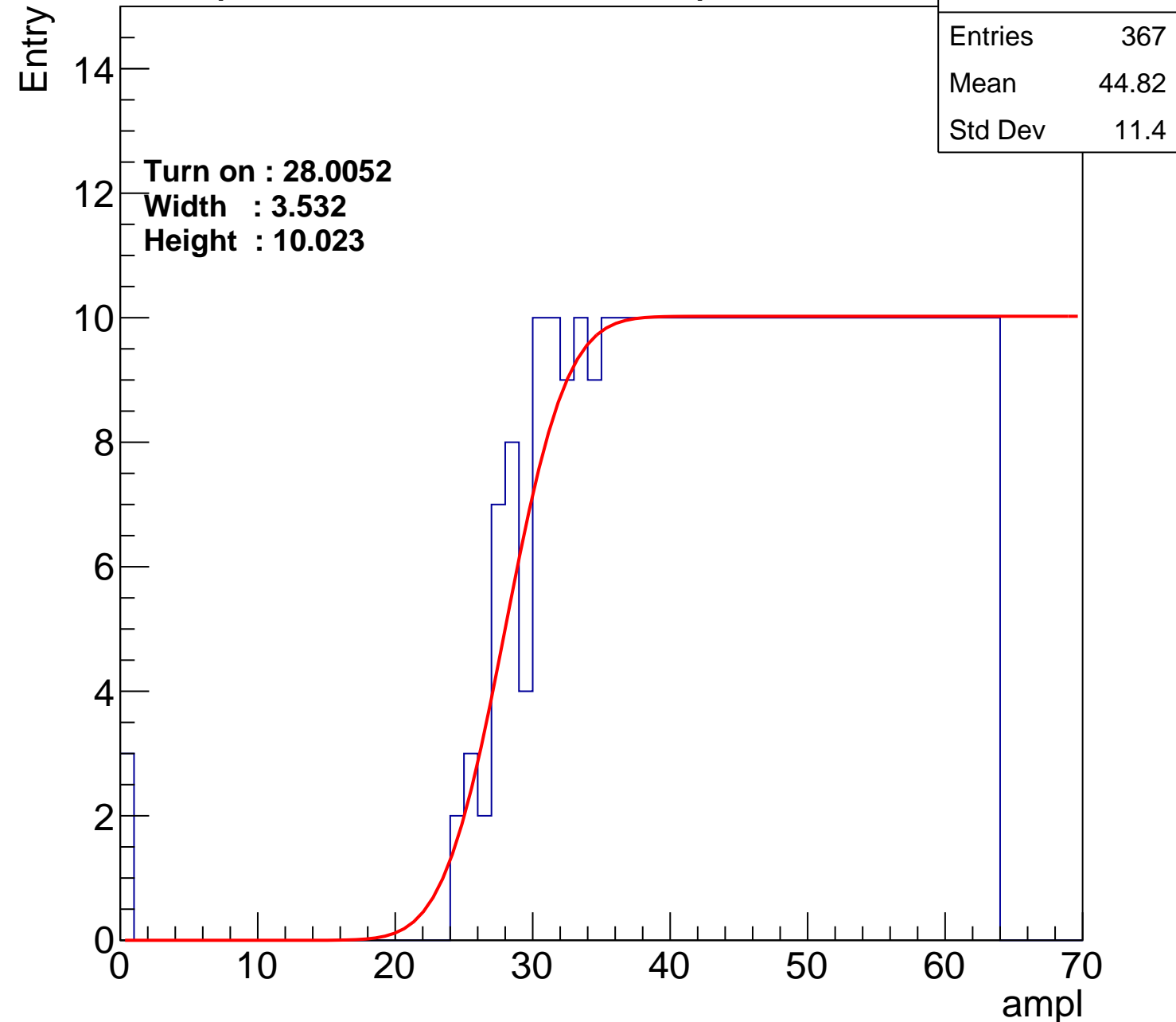
Width : 3.532

Height : 10.023

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch51

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	350
Mean	45.8
Std Dev	10.54

Turn on : 29.1820

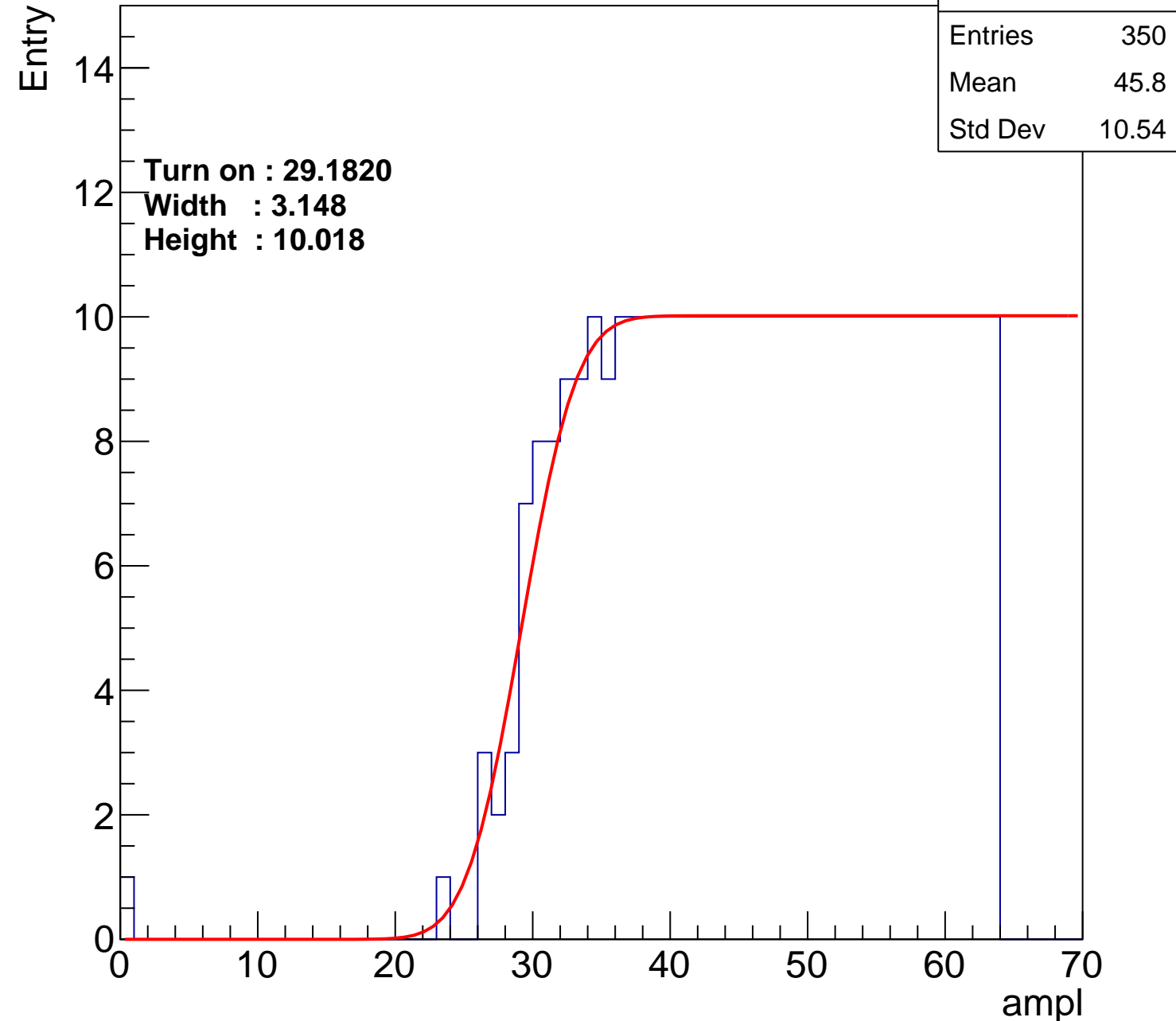
Width : 3.148

Height : 10.018

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch52

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	375
Mean	44.62
Std Dev	11.13

Turn on : 26.3329

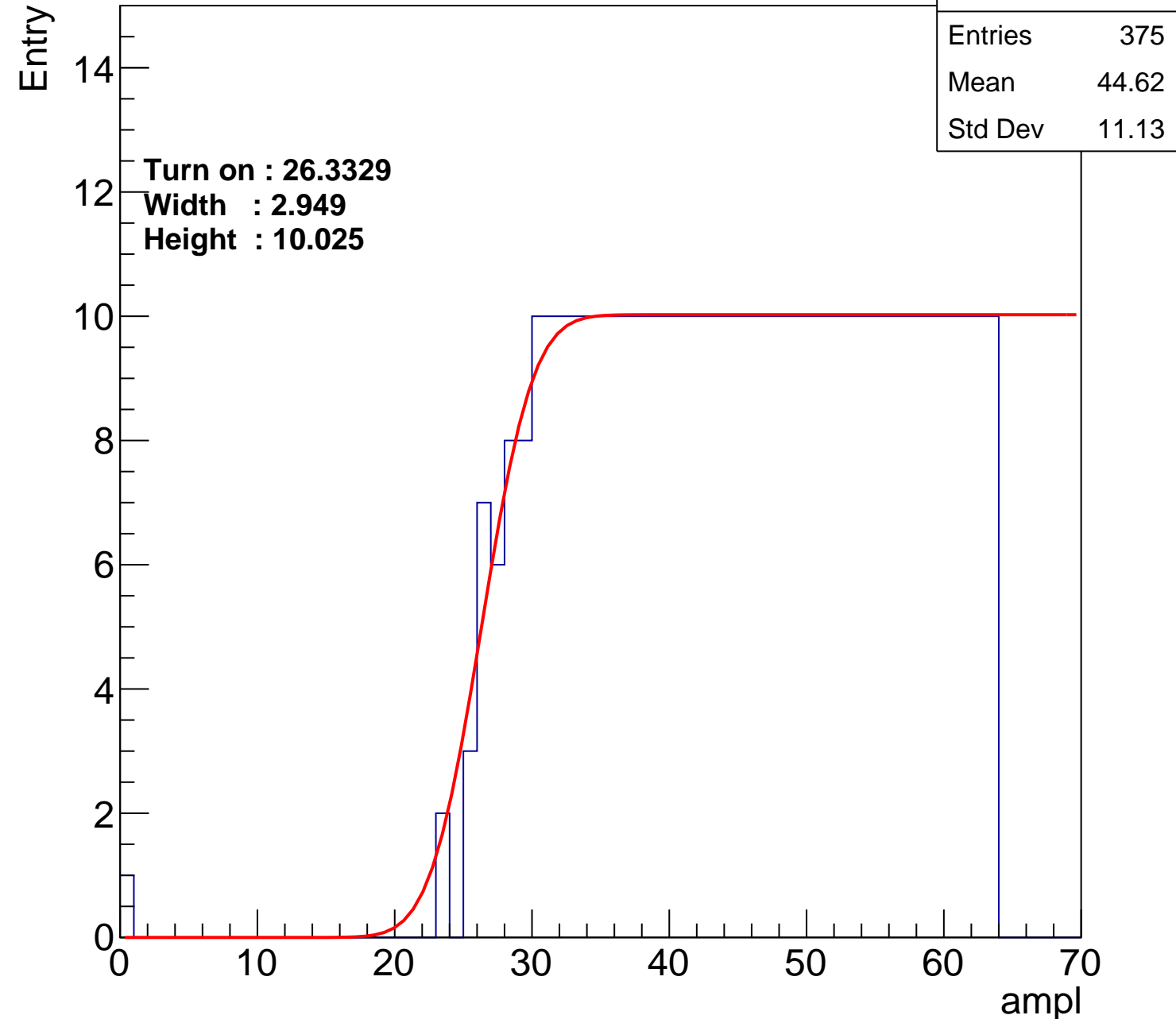
Width : 2.949

Height : 10.025

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch53

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	368
Mean	44.95
Std Dev	10.96

Turn on : 27.4139

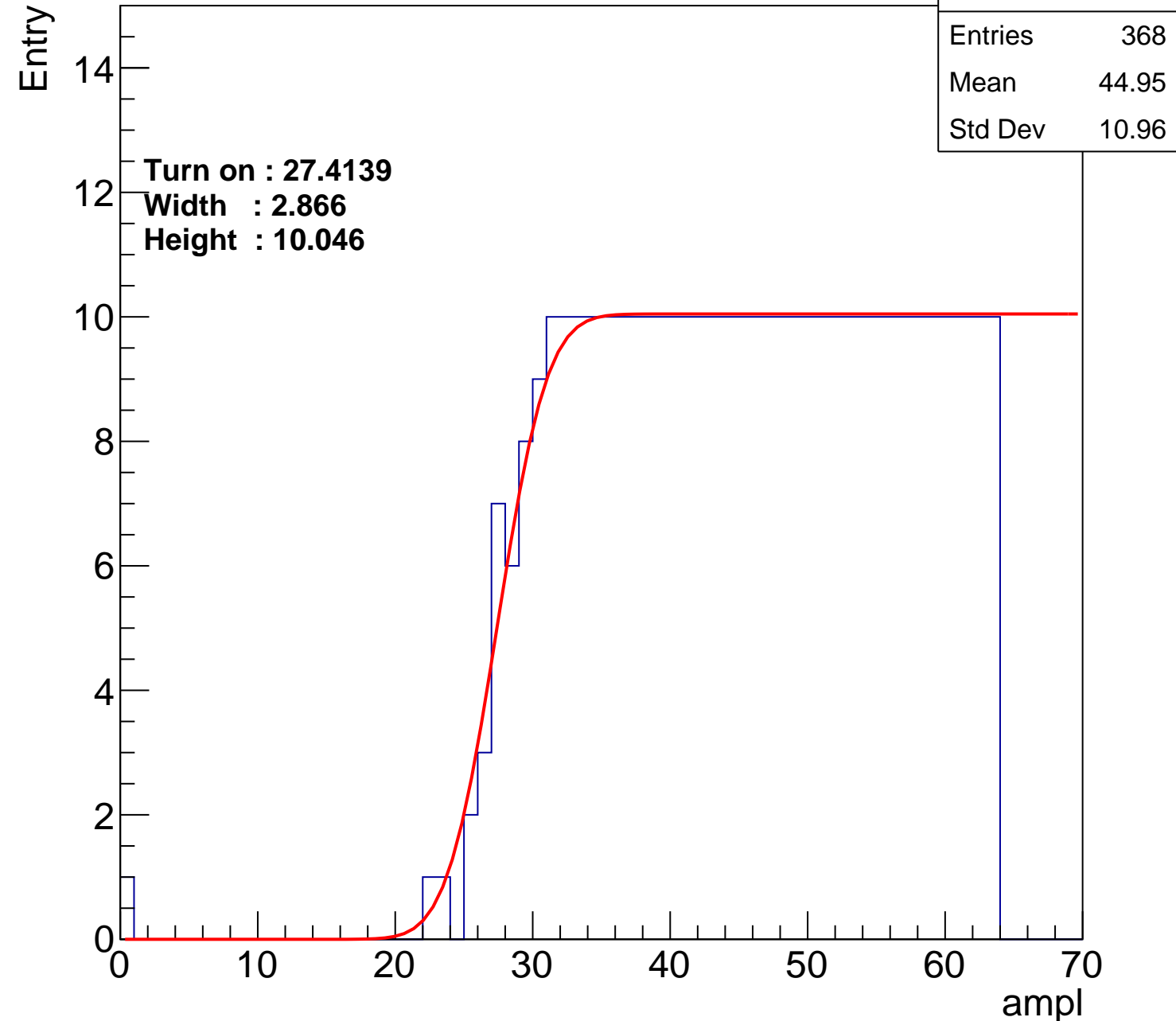
Width : 2.866

Height : 10.046

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch54

calib\_packv5\_042523\_0143.root, FC#0, port D2

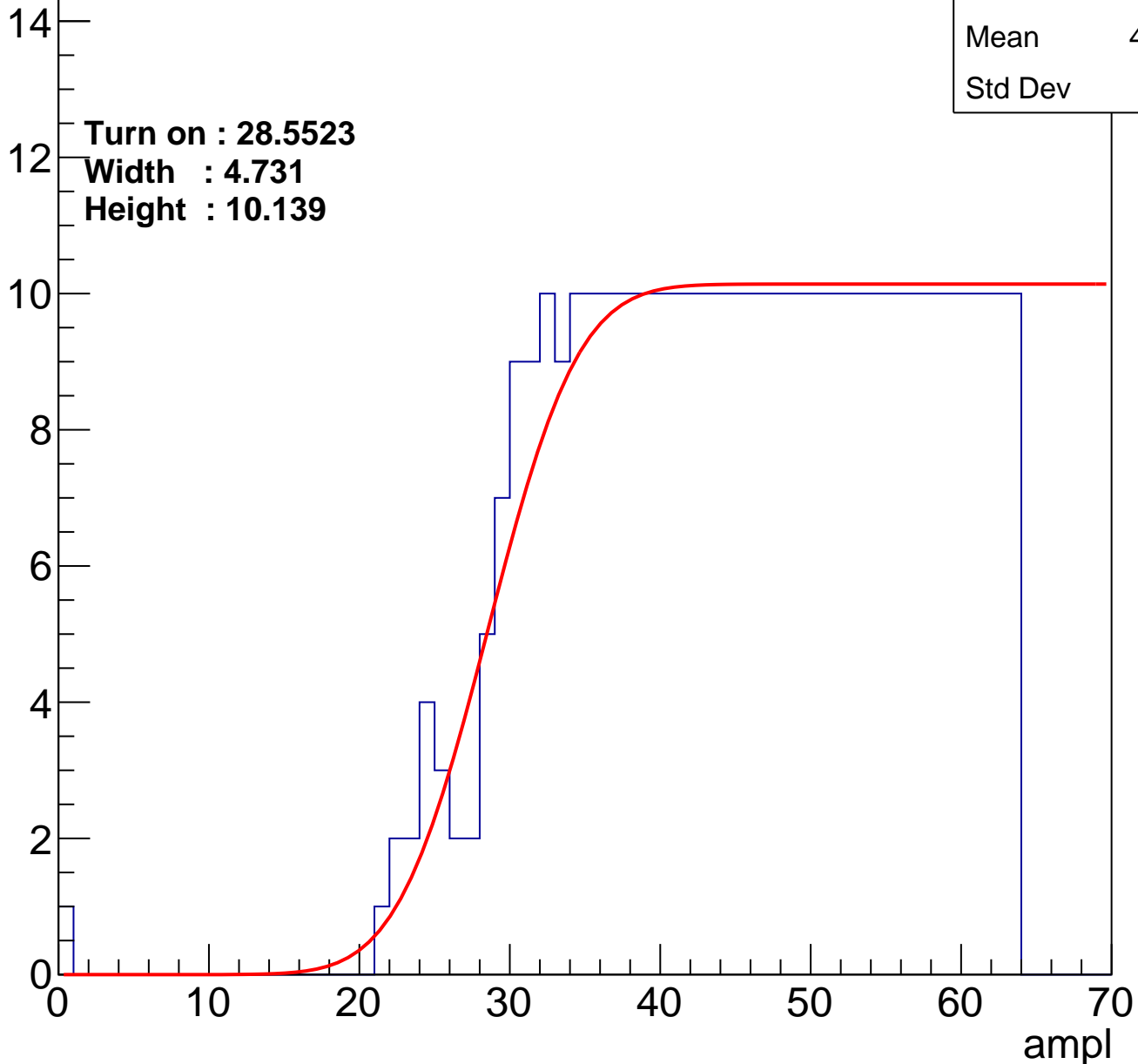
Entries	366
Mean	44.94
Std Dev	11.1

Turn on : 28.5523

Width : 4.731

Height : 10.139

Entry





# B1L101S, U26-ch55

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	353
Mean	45.58
Std Dev	10.85

**Turn on : 29.3269**

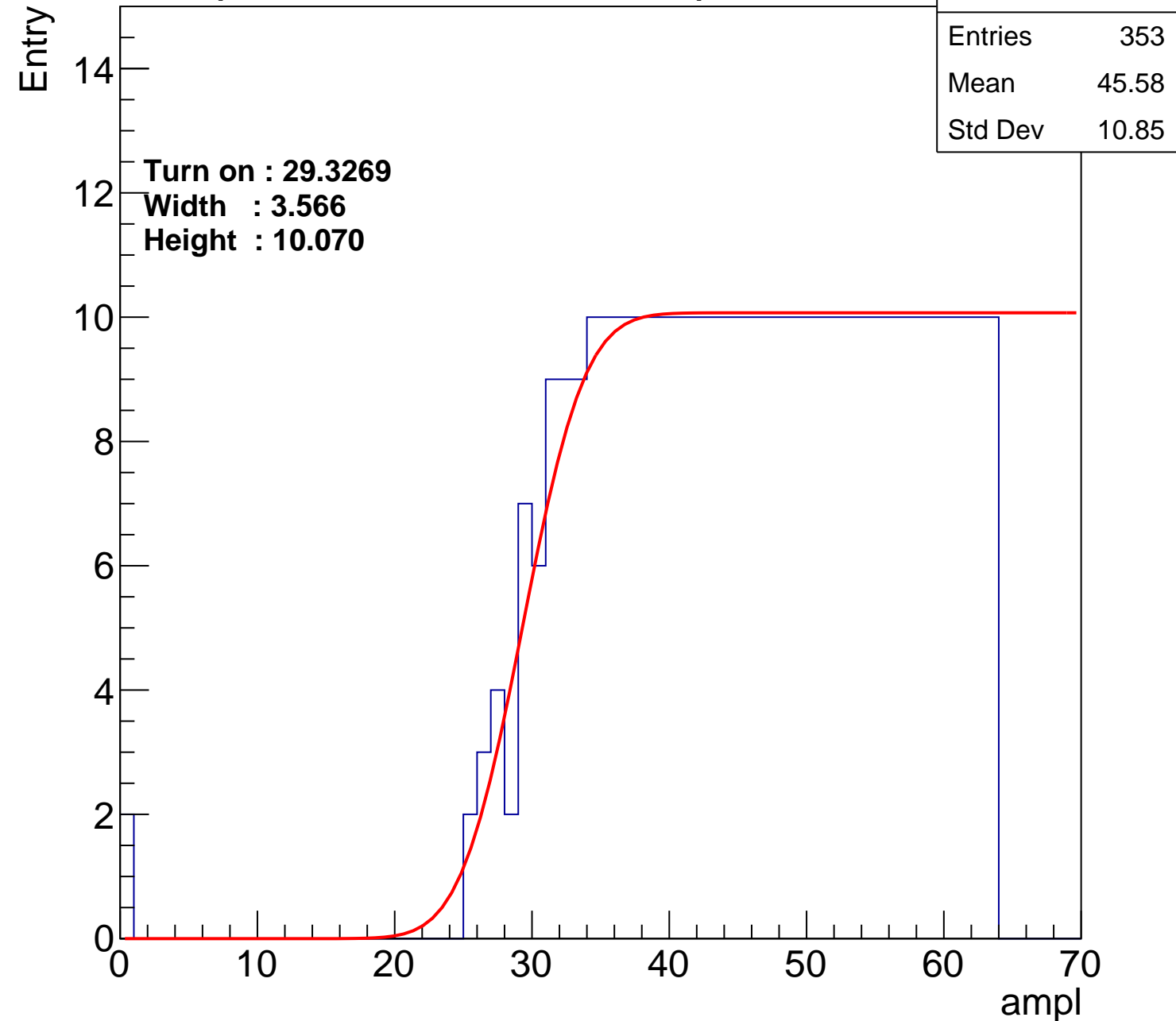
**Width : 3.566**

**Height : 10.070**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch56

calib\_packv5\_042523\_0143.root, FC#0, port D2

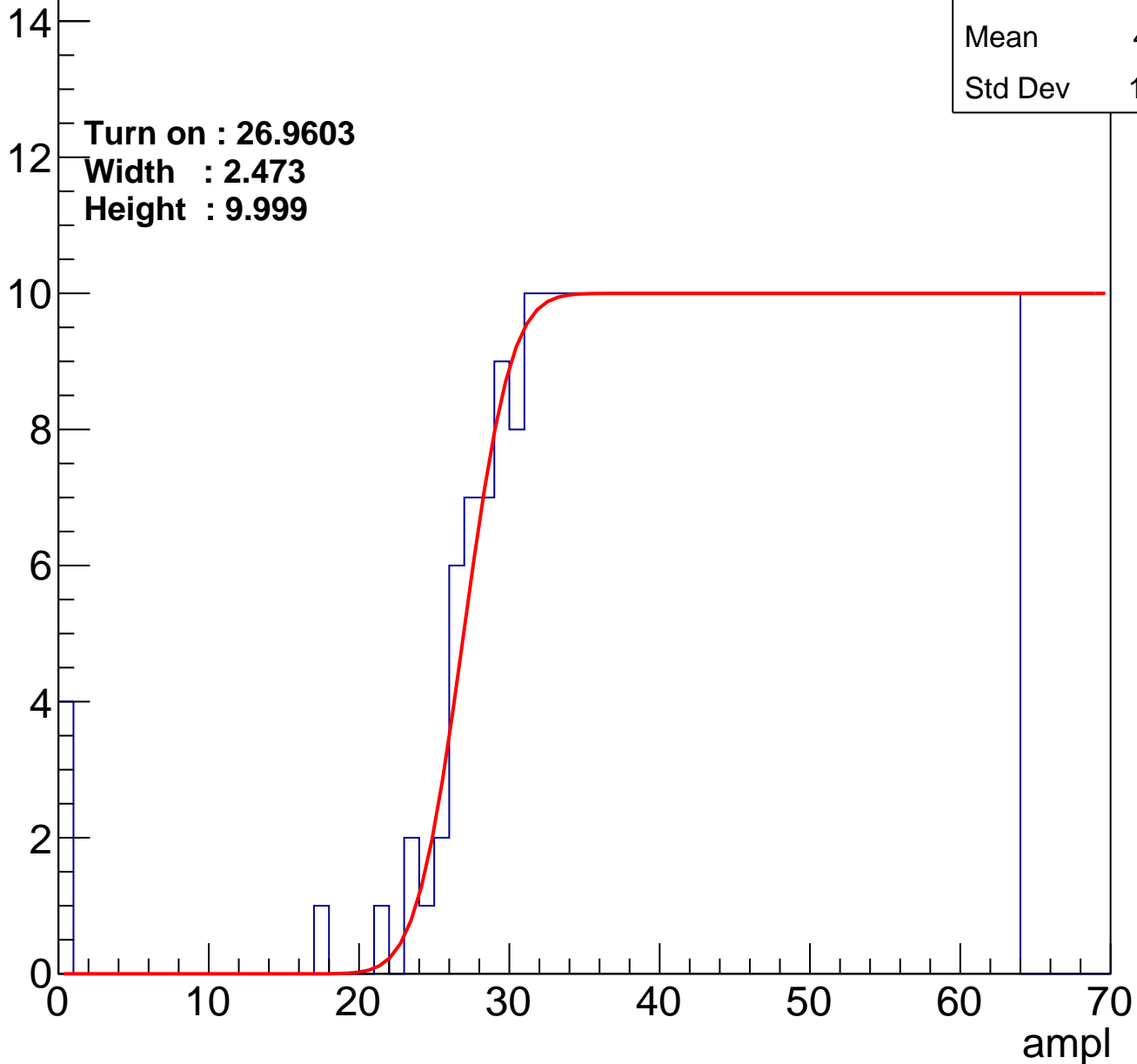
Entries	378
Mean	44.21
Std Dev	11.87

**Turn on : 26.9603**

**Width : 2.473**

**Height : 9.999**

Entry



# B1L101S, U26-ch57

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	361
Mean	45.07
Std Dev	11.33

Turn on : 28.1231

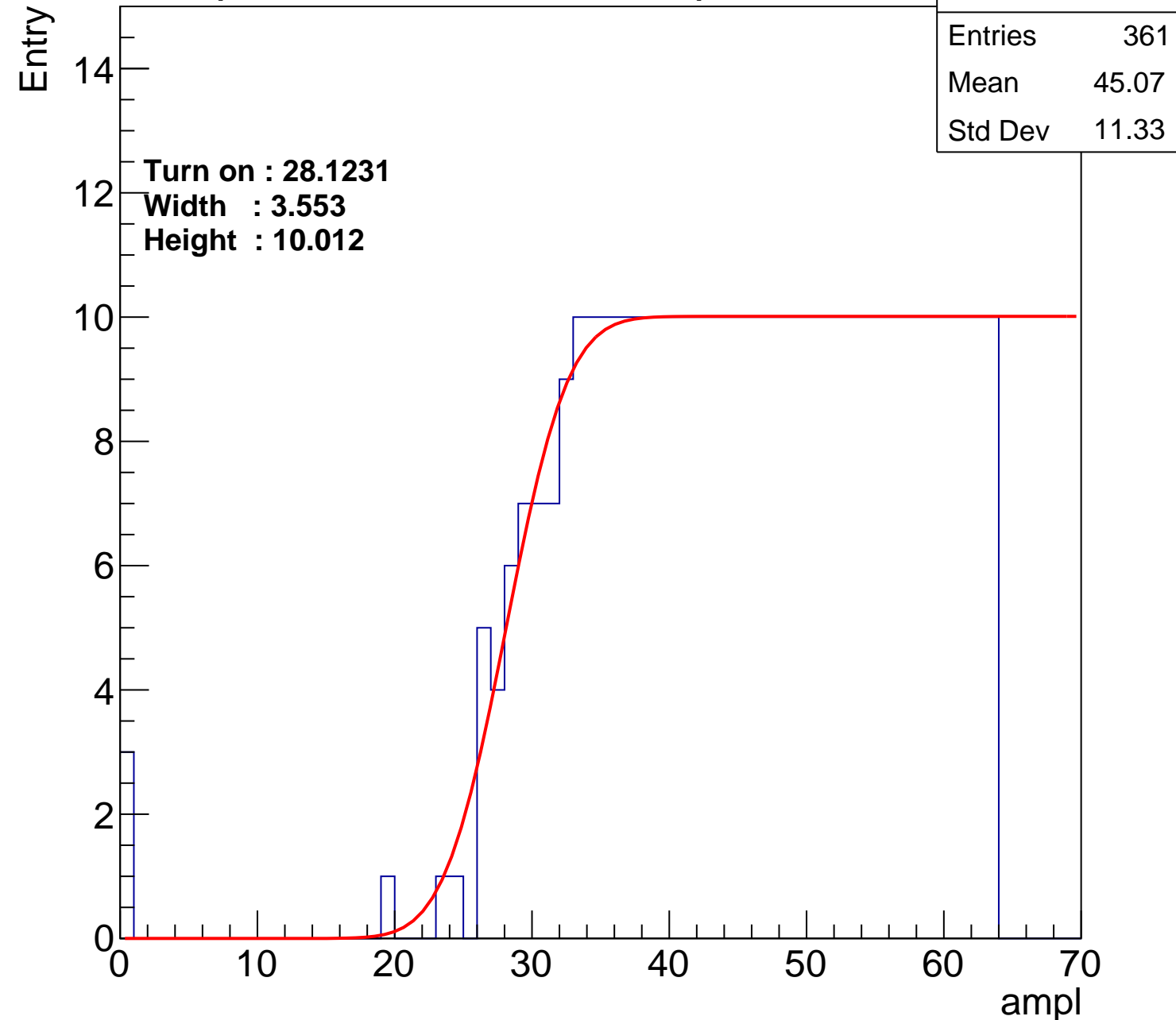
Width : 3.553

Height : 10.012

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch58

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	349
Mean	45.78
Std Dev	10.75

**Turn on : 29.4160**

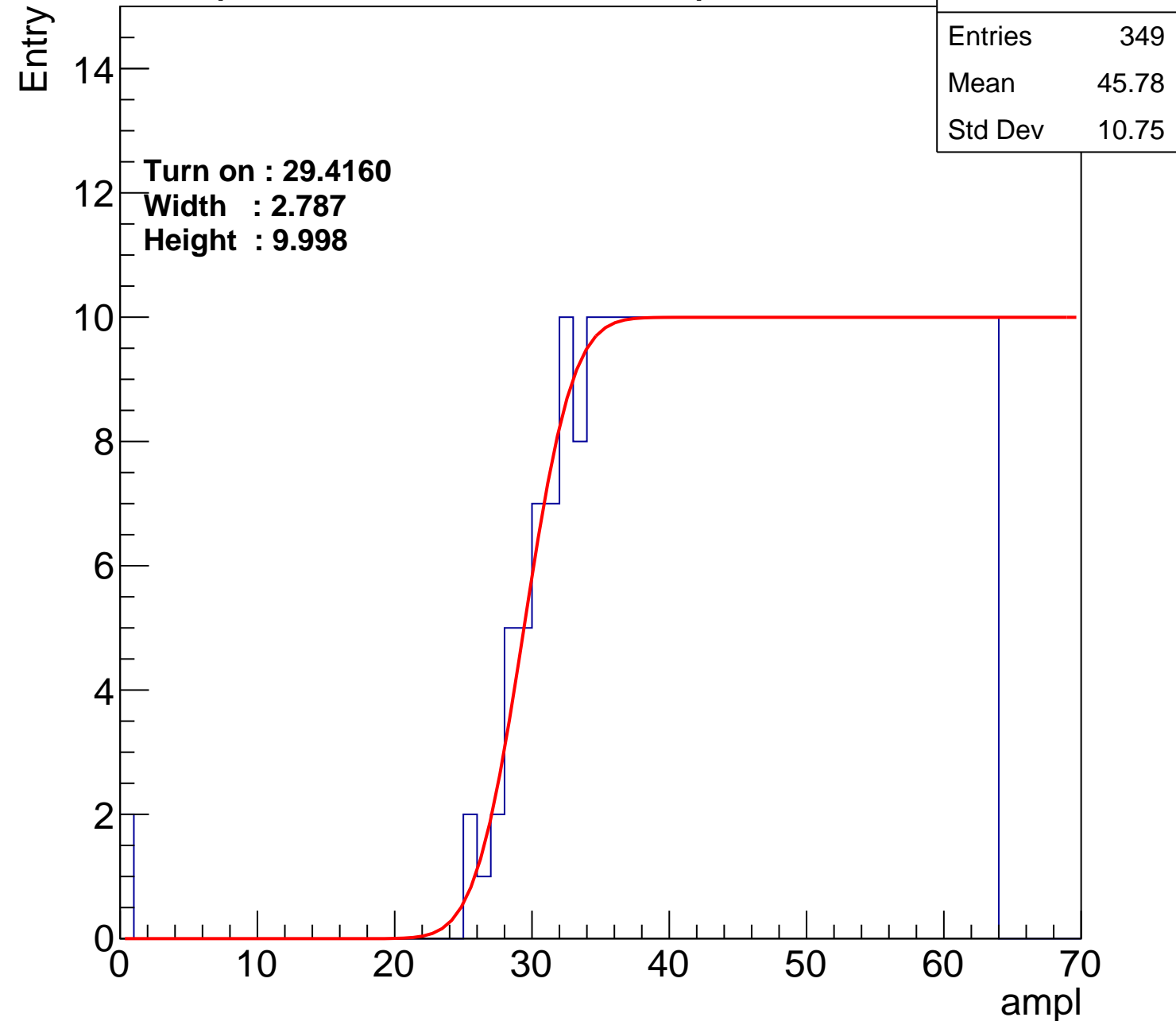
**Width : 2.787**

**Height : 9.998**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch59

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	371
Mean	44.6
Std Dev	11.61

Turn on : 27.2224

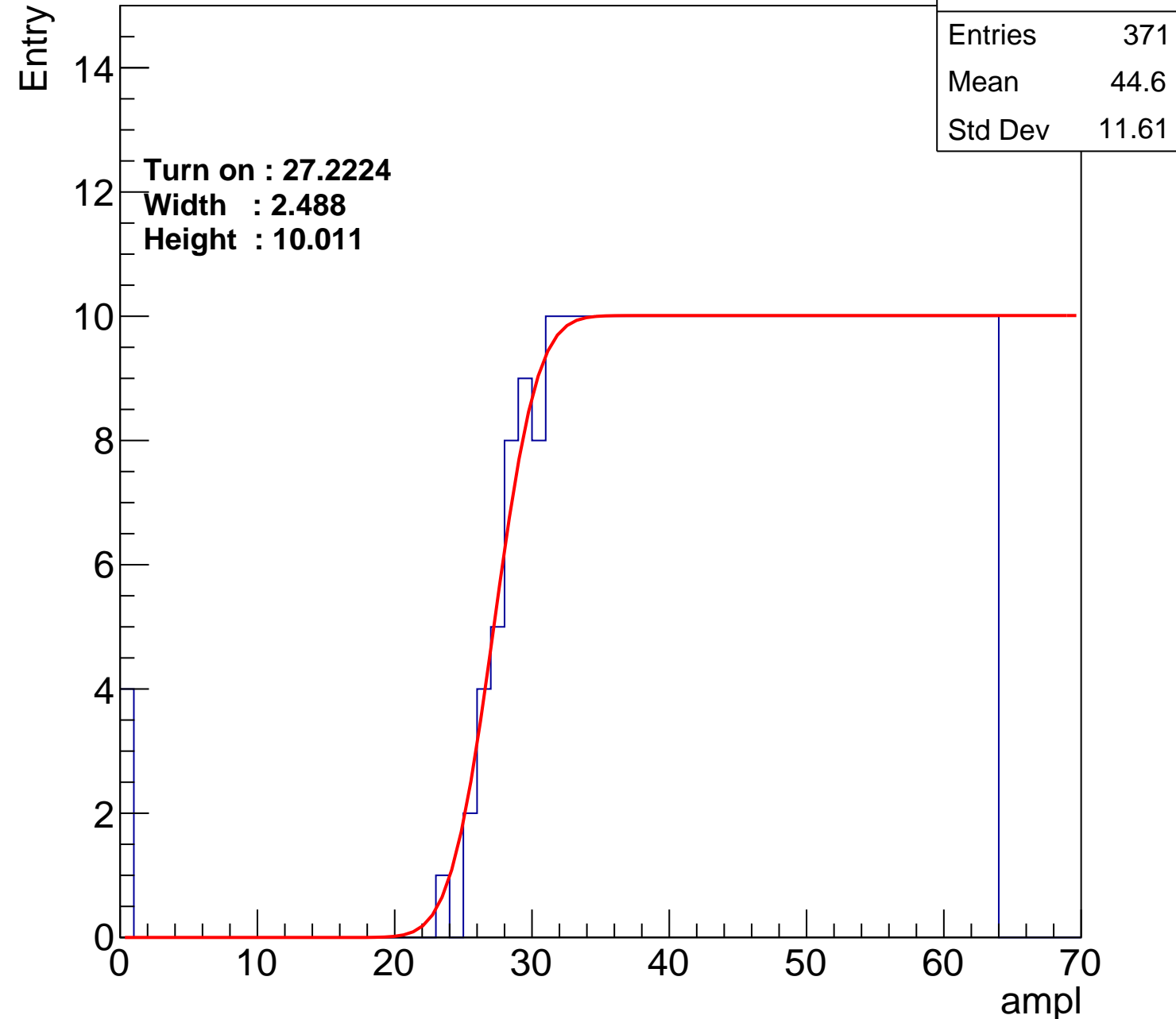
Width : 2.488

Height : 10.011

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch60

calib\_packv5\_042523\_0143.root, FC#0, port D2

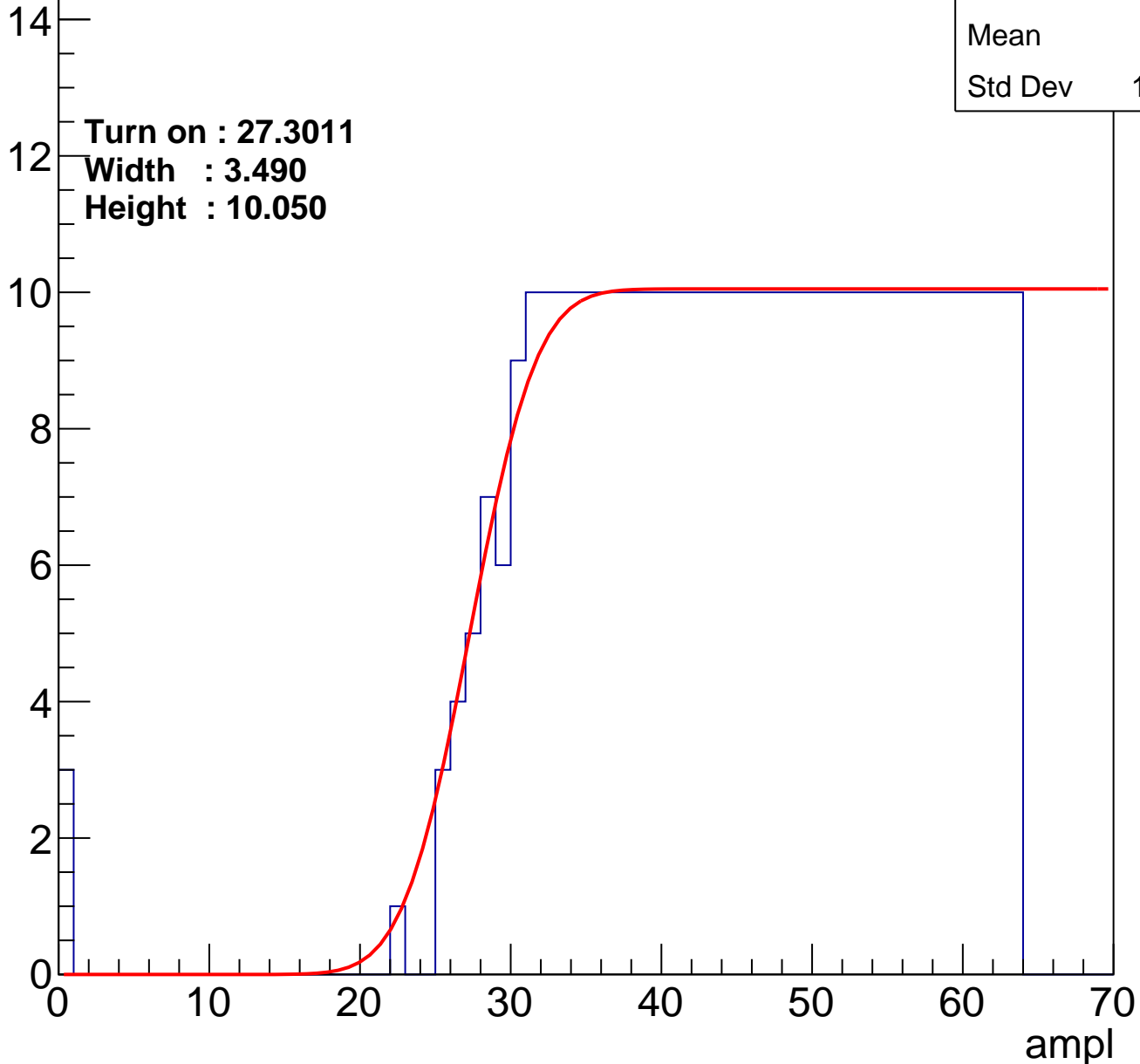
Entries	368
Mean	44.8
Std Dev	11.38

Turn on : 27.3011

Width : 3.490

Height : 10.050

Entry



# B1L101S, U26-ch61

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	363
Mean	45.01
Std Dev	11.32

**Turn on : 28.9795**

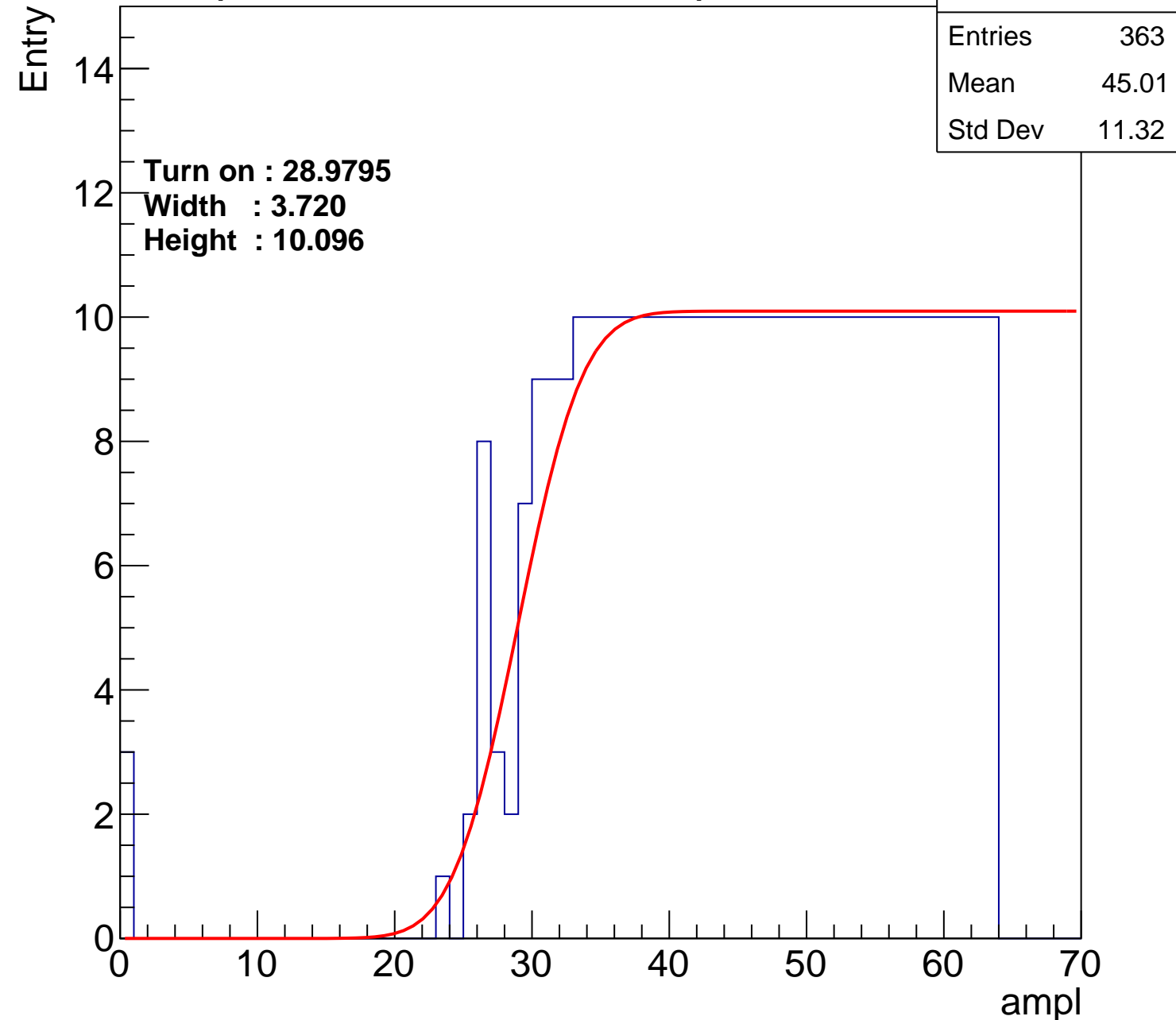
**Width : 3.720**

**Height : 10.096**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch62

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	378
Mean	44.43
Std Dev	11.27

Turn on : 27.0990

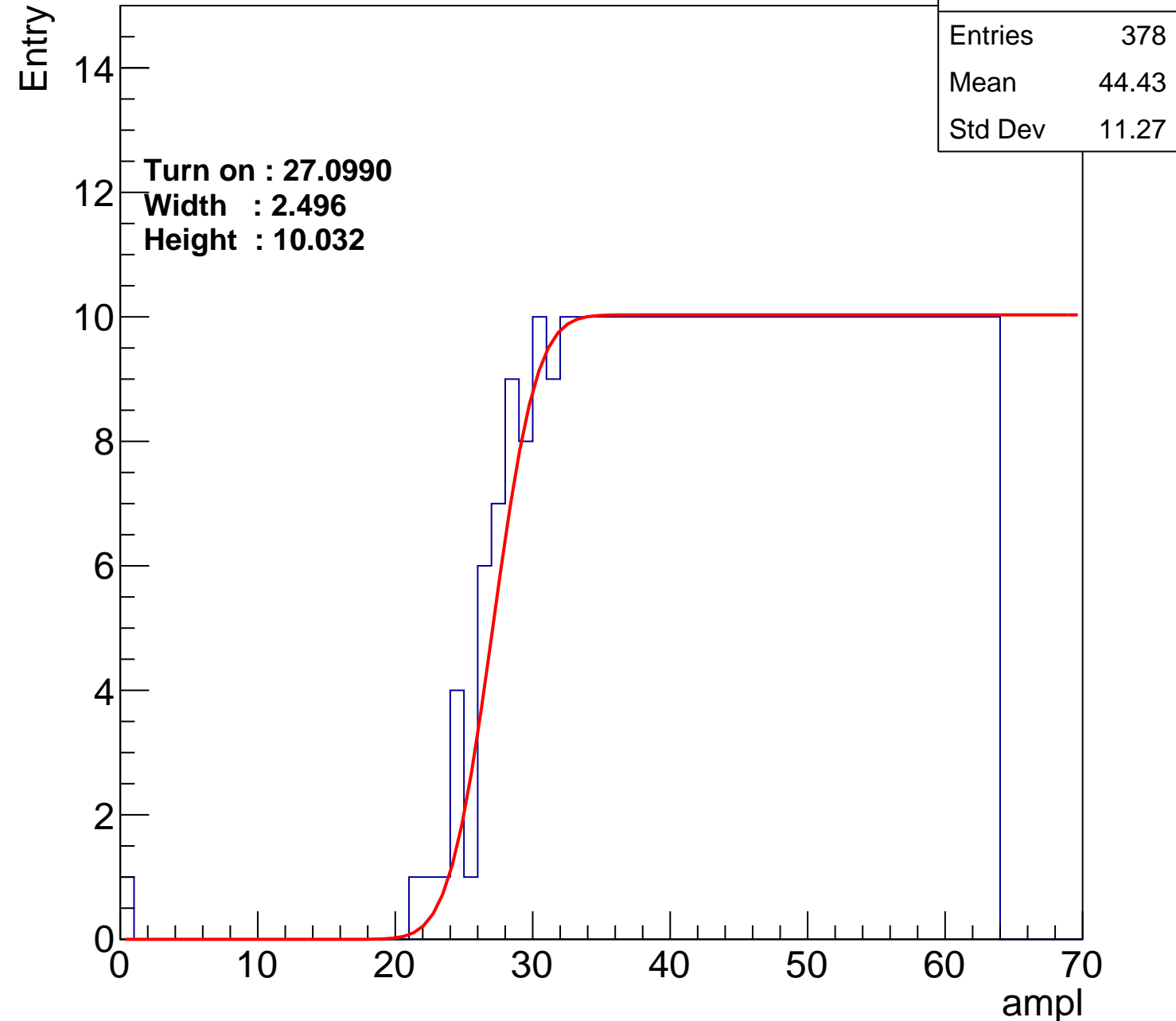
Width : 2.496

Height : 10.032

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U26-ch63

calib\_packv5\_042523\_0143.root, FC#0, port D2

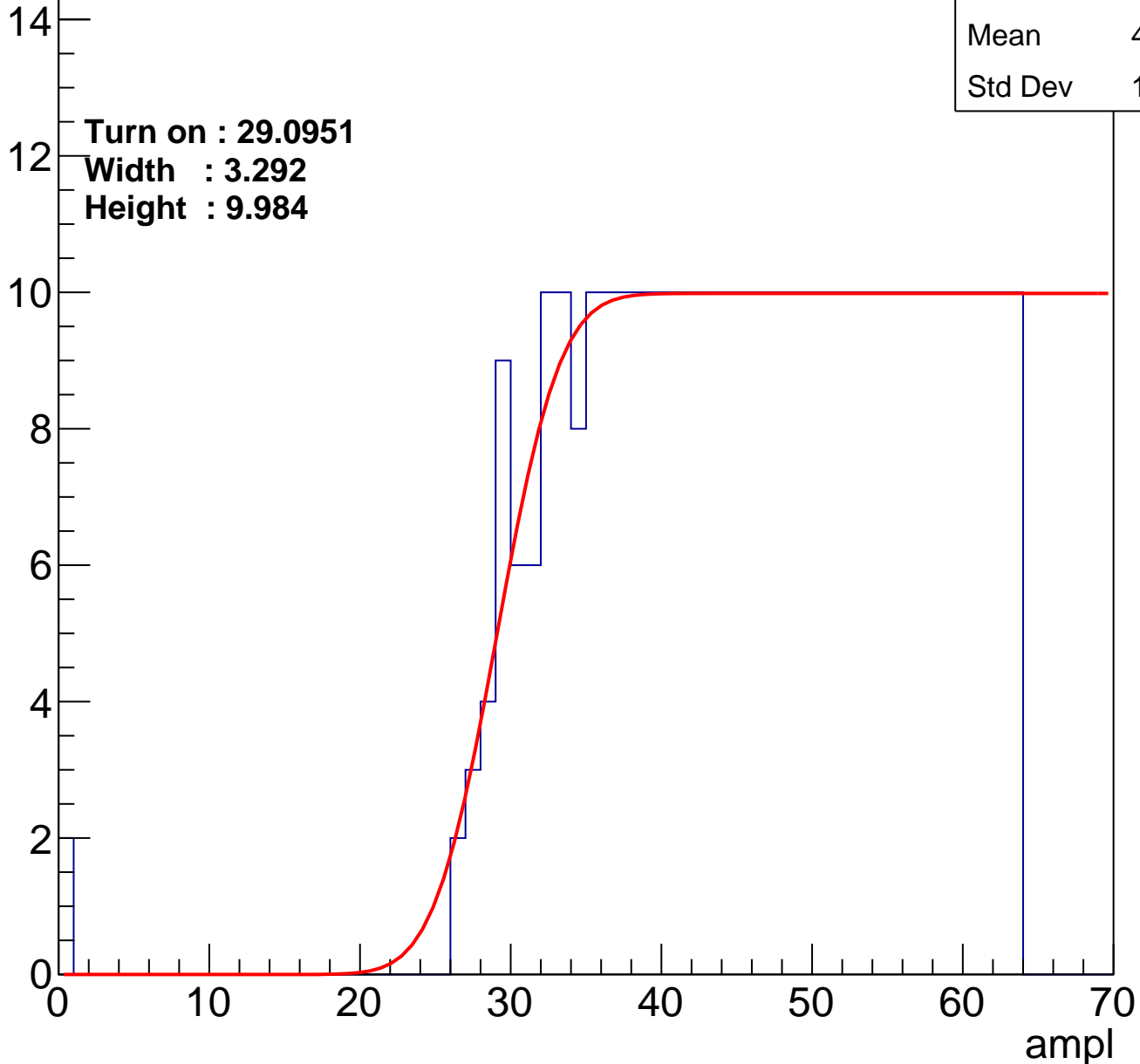
Entries	350
Mean	45.73
Std Dev	10.77

Turn on : 29.0951

Width : 3.292

Height : 9.984

Entry



# B1L101S, U26-ch64

calib\_packv5\_042523\_0143.root, FC#0, port D2

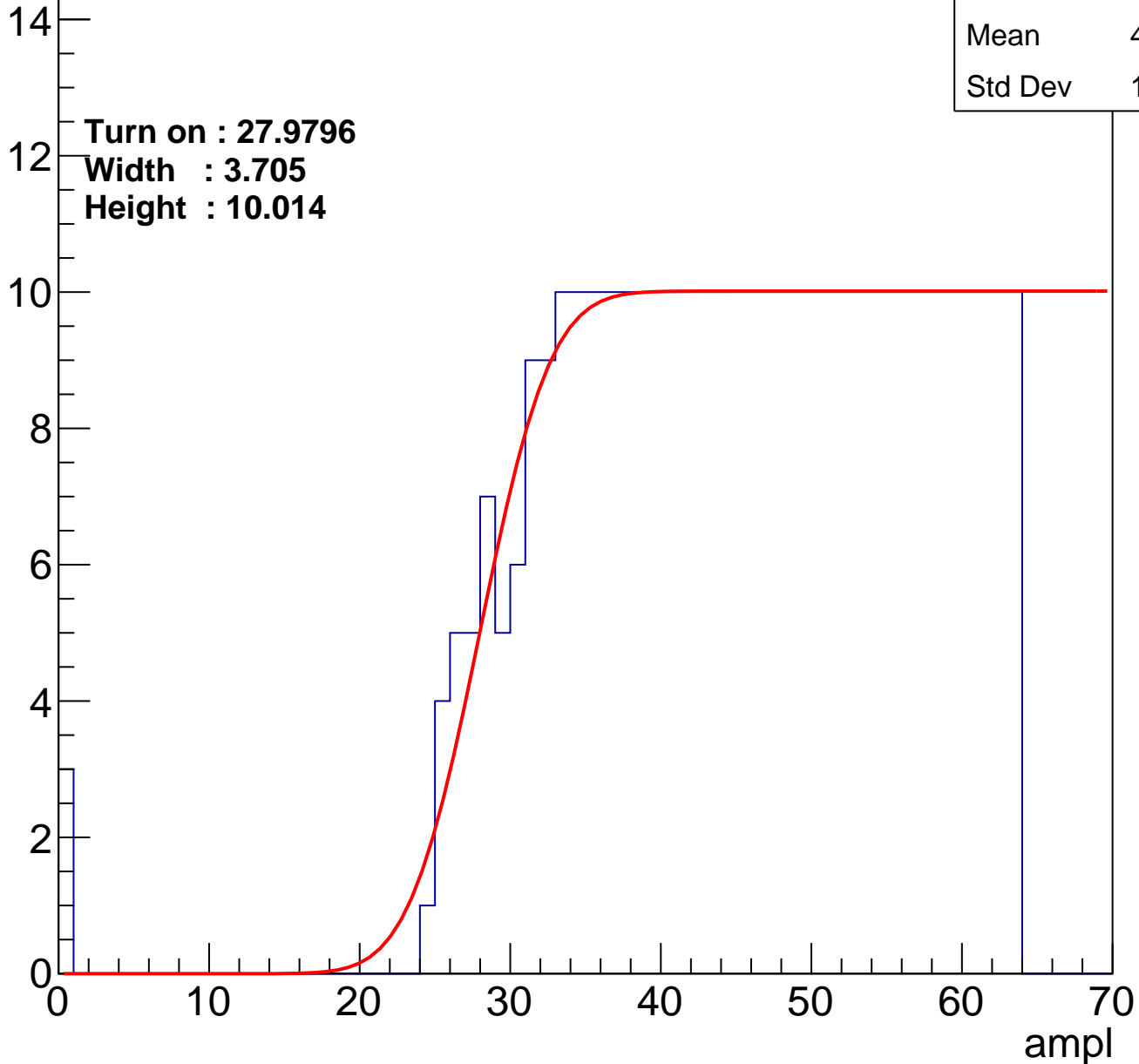
Entries	364
Mean	44.94
Std Dev	11.37

Turn on : 27.9796

Width : 3.705

Height : 10.014

Entry



# B1L101S, U26-ch65

calib\_packv5\_042523\_0143.root, FC#0, port D2

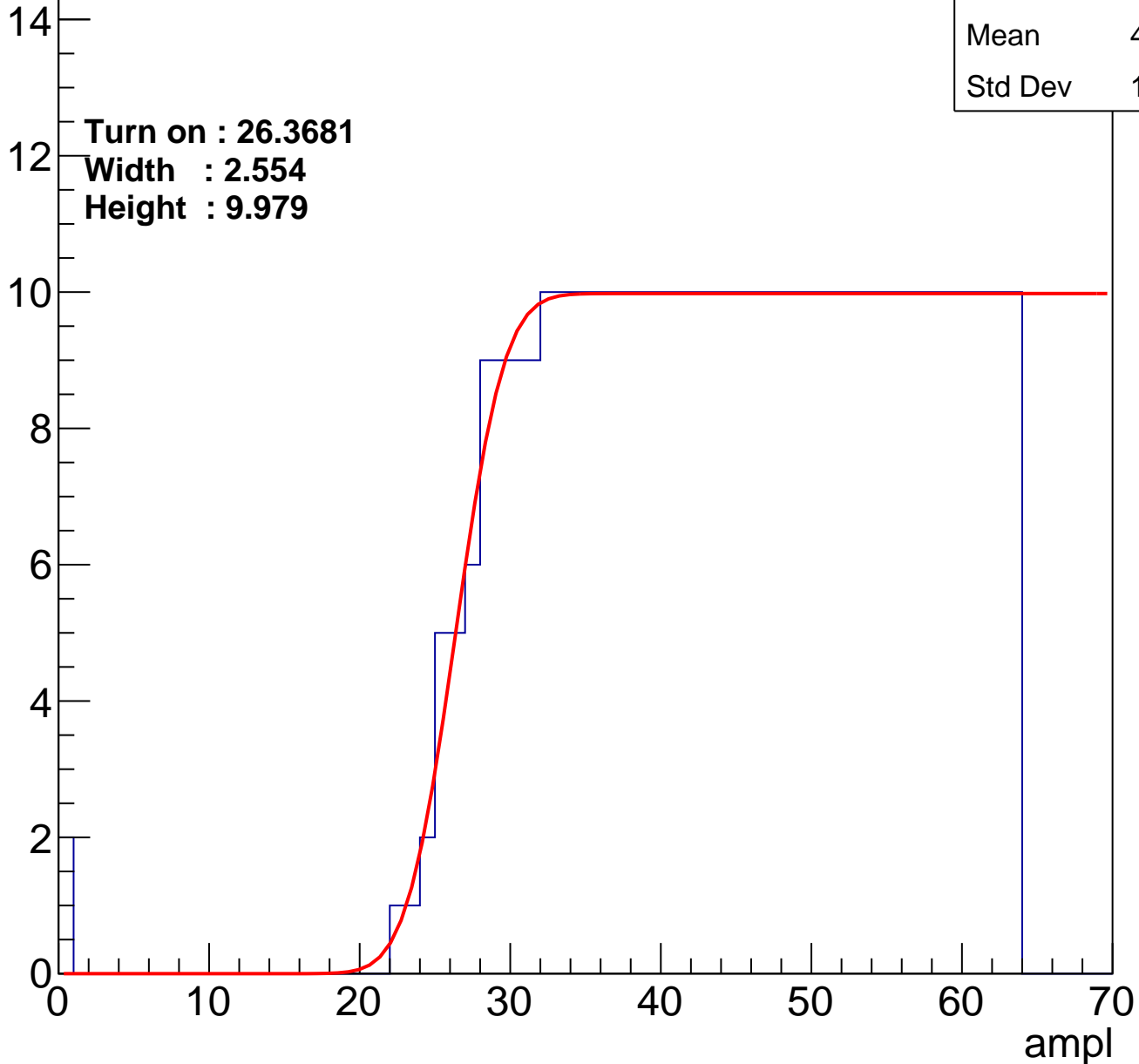
Entries	378
Mean	44.37
Std Dev	11.45

Turn on : 26.3681

Width : 2.554

Height : 9.979

Entry



# B1L101S, U26-ch66

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	370
Mean	44.7
Std Dev	11.35

Turn on : 28.3209

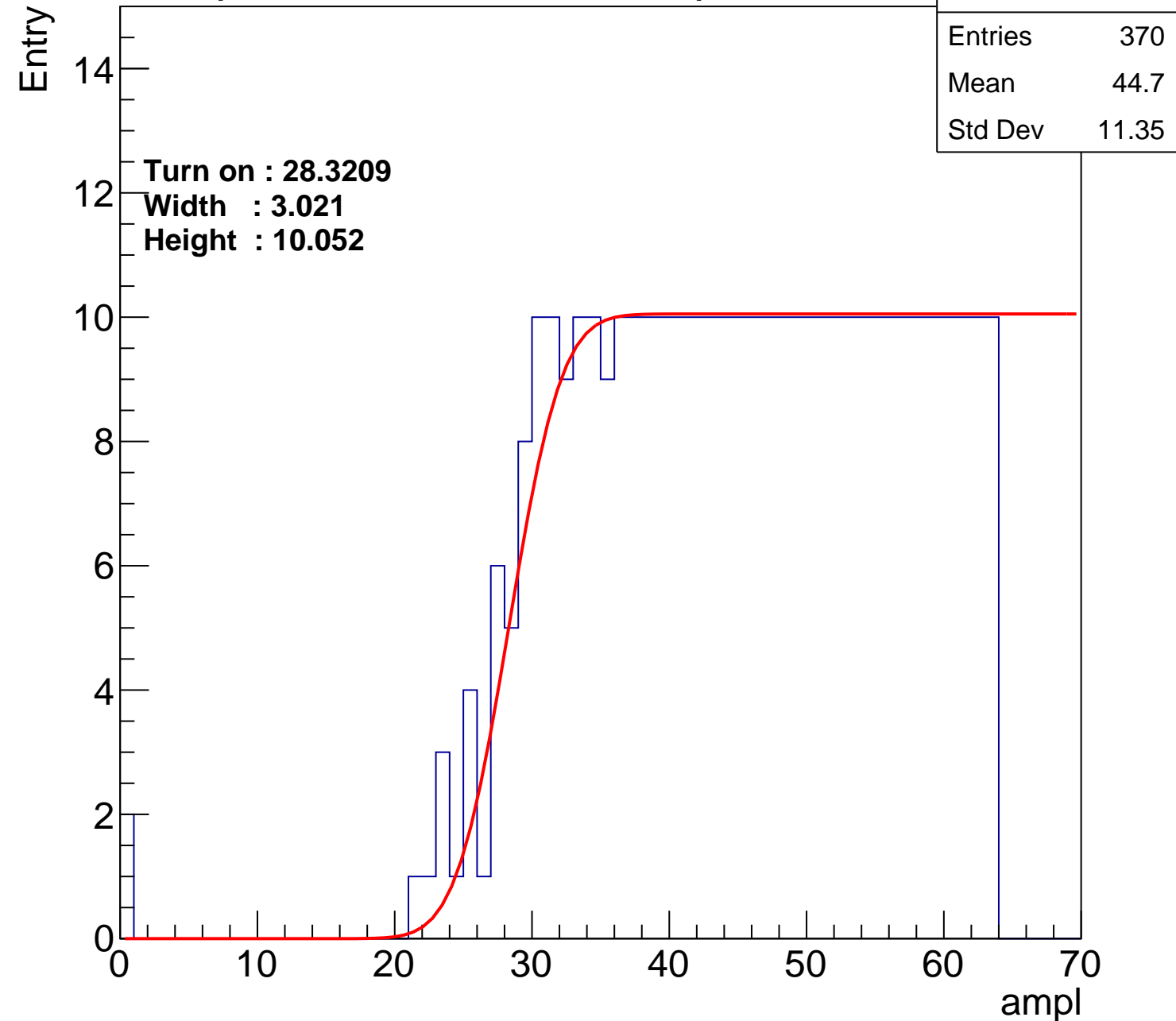
Width : 3.021

Height : 10.052

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch67

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	355
Mean	45.37
Std Dev	11.27

Turn on : 28.9989

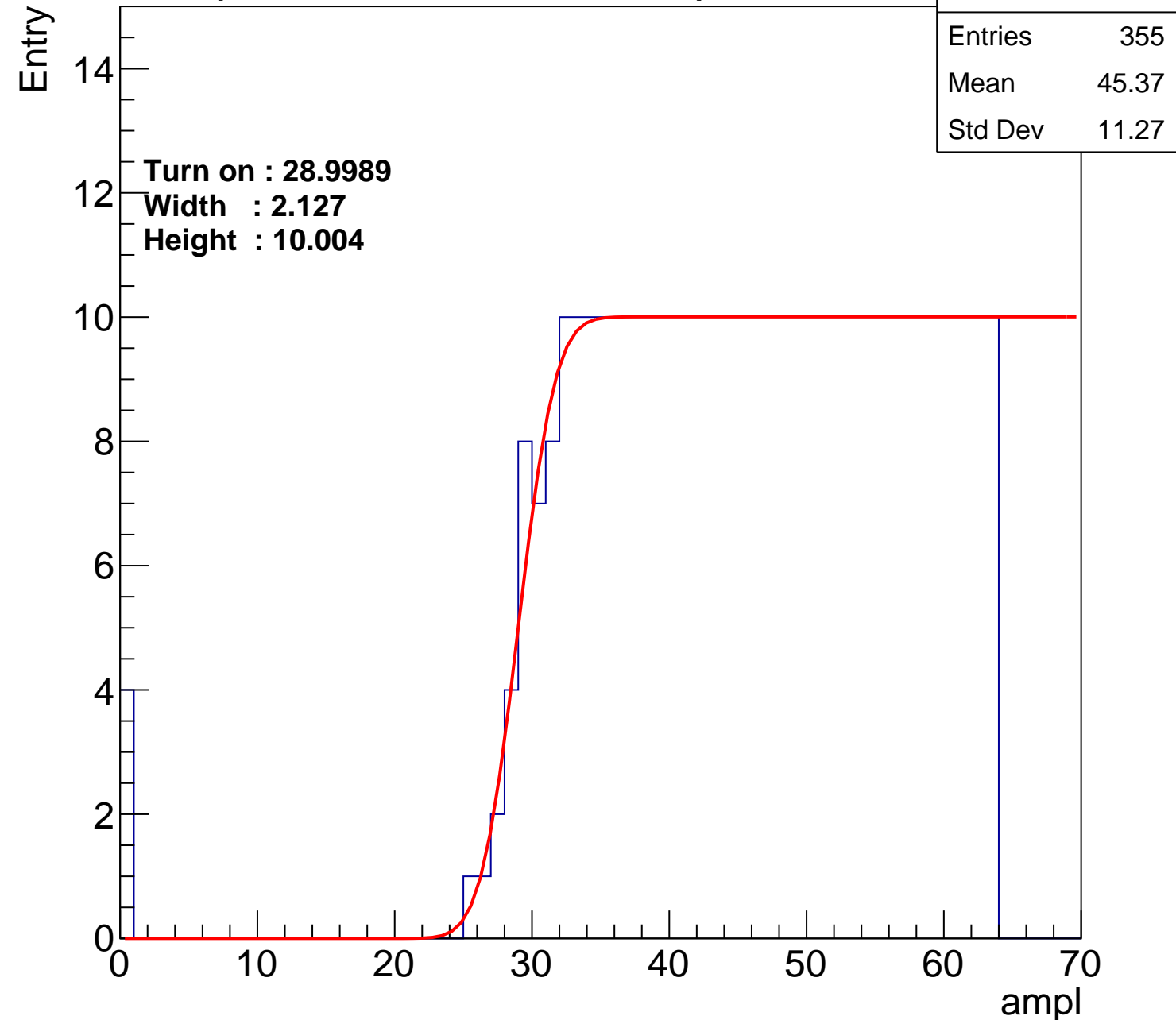
Width : 2.127

Height : 10.004

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch68

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	382
Mean	44.05
Std Dev	11.9

Turn on : 26.6761

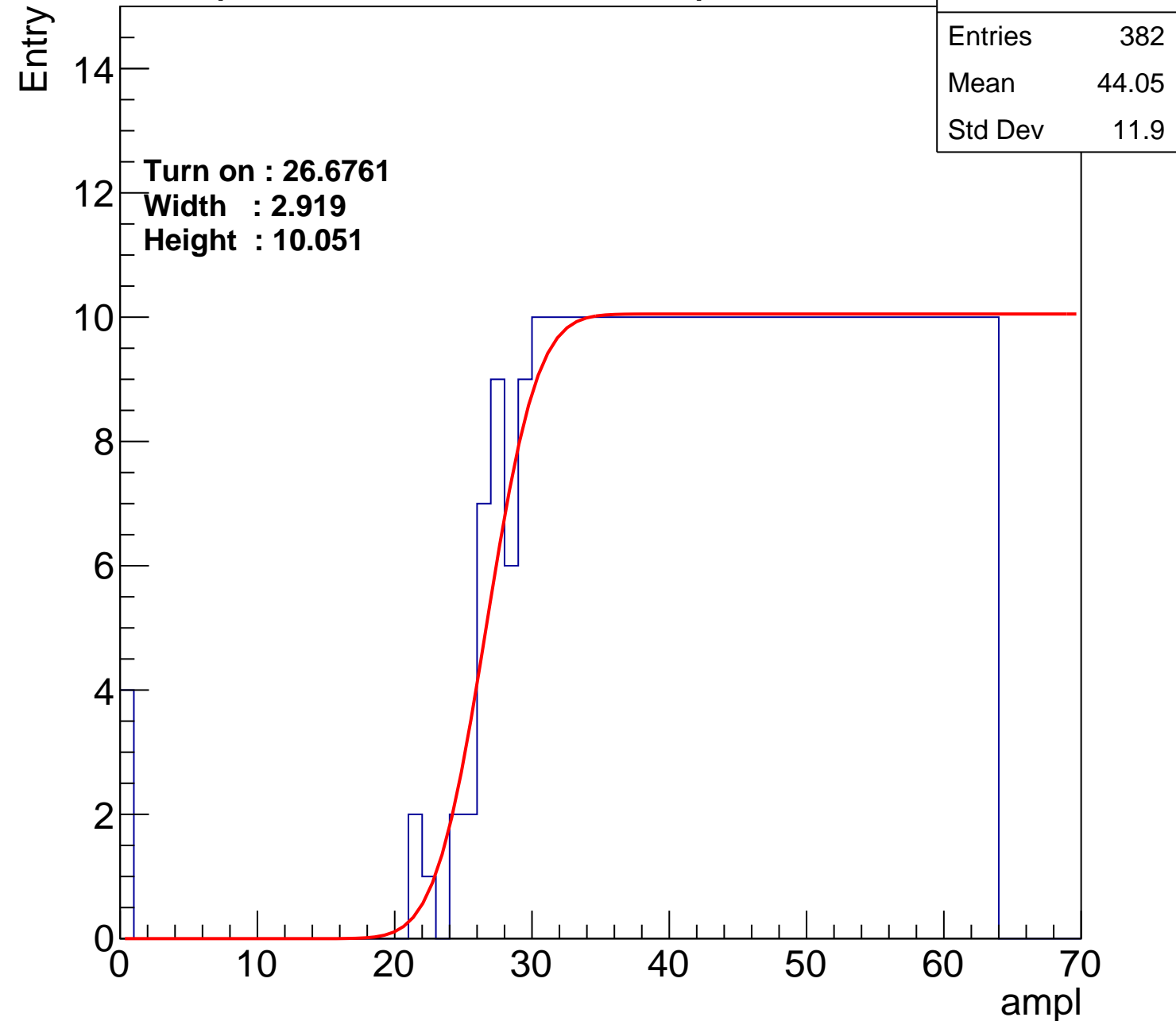
Width : 2.919

Height : 10.051

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch69

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	364
Mean	44.86
Std Dev	11.58

Turn on : 28.7789

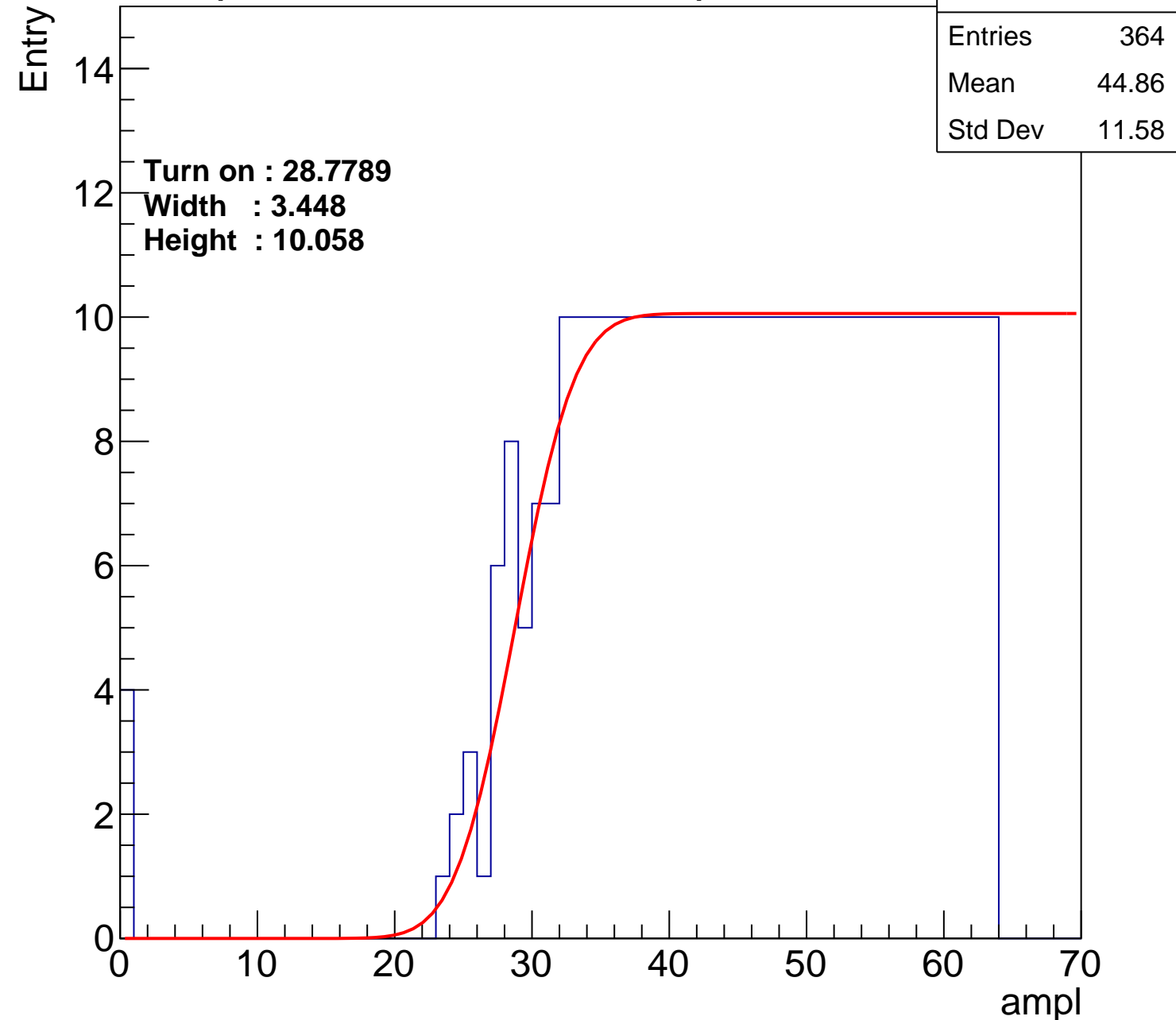
Width : 3.448

Height : 10.058

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch70

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	376
Mean	44.41
Std Dev	11.57

Turn on : 27.2088

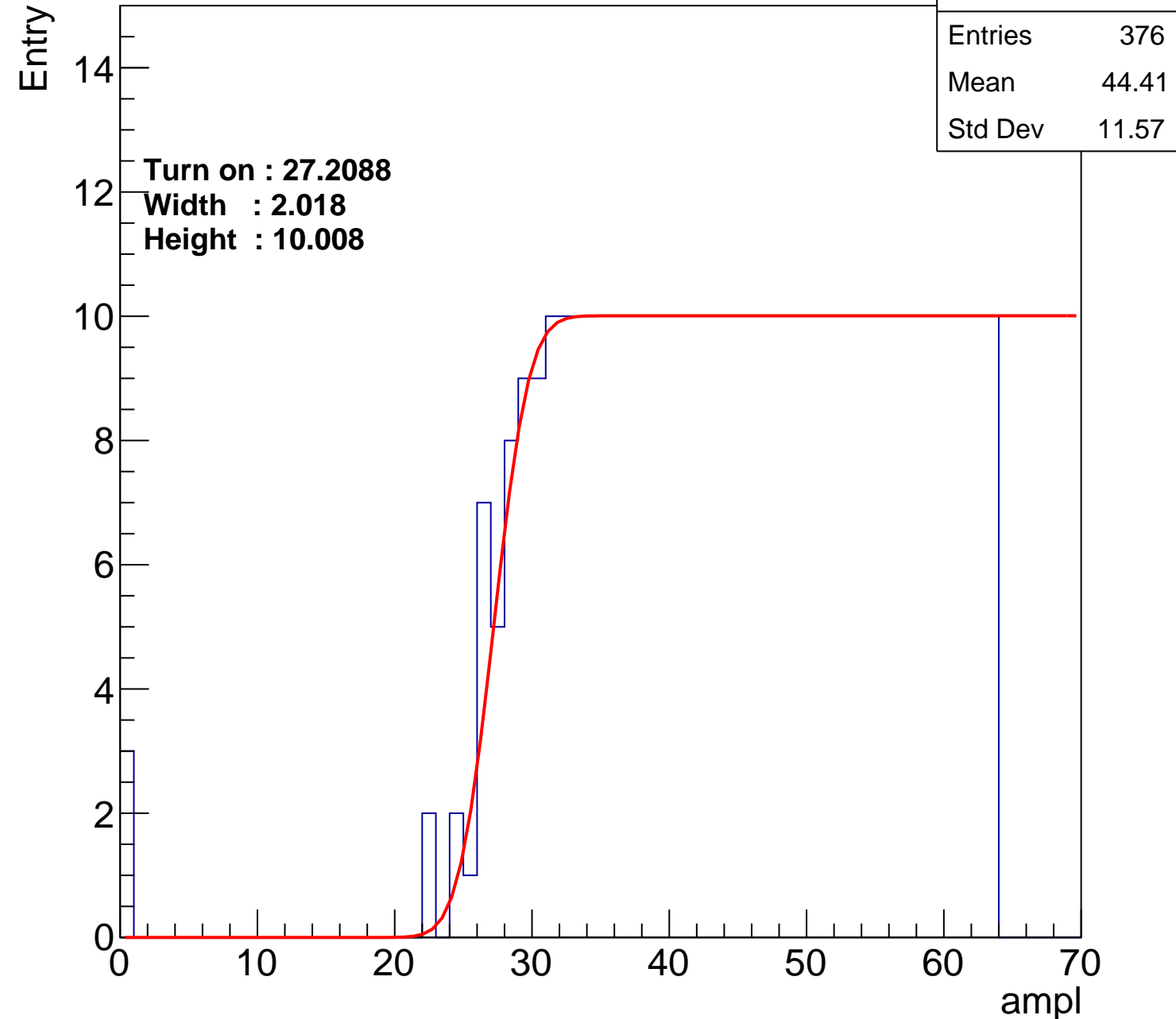
Width : 2.018

Height : 10.008

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U26-ch71

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	349
Mean	45.83
Std Dev	10.56

Turn on : 29.4933

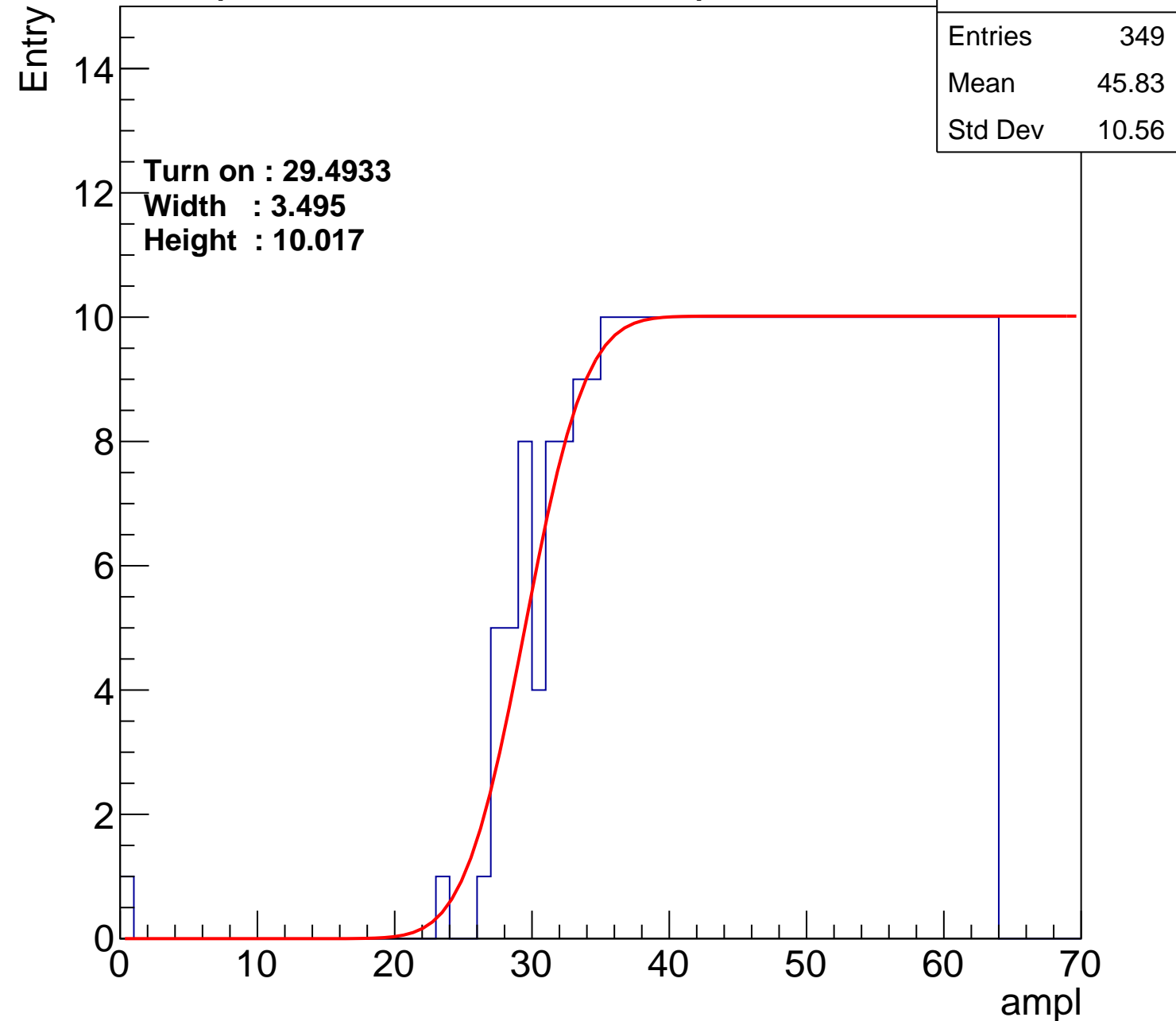
Width : 3.495

Height : 10.017

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch72

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	385
Mean	43.96
Std Dev	11.8

Turn on : 26.4625

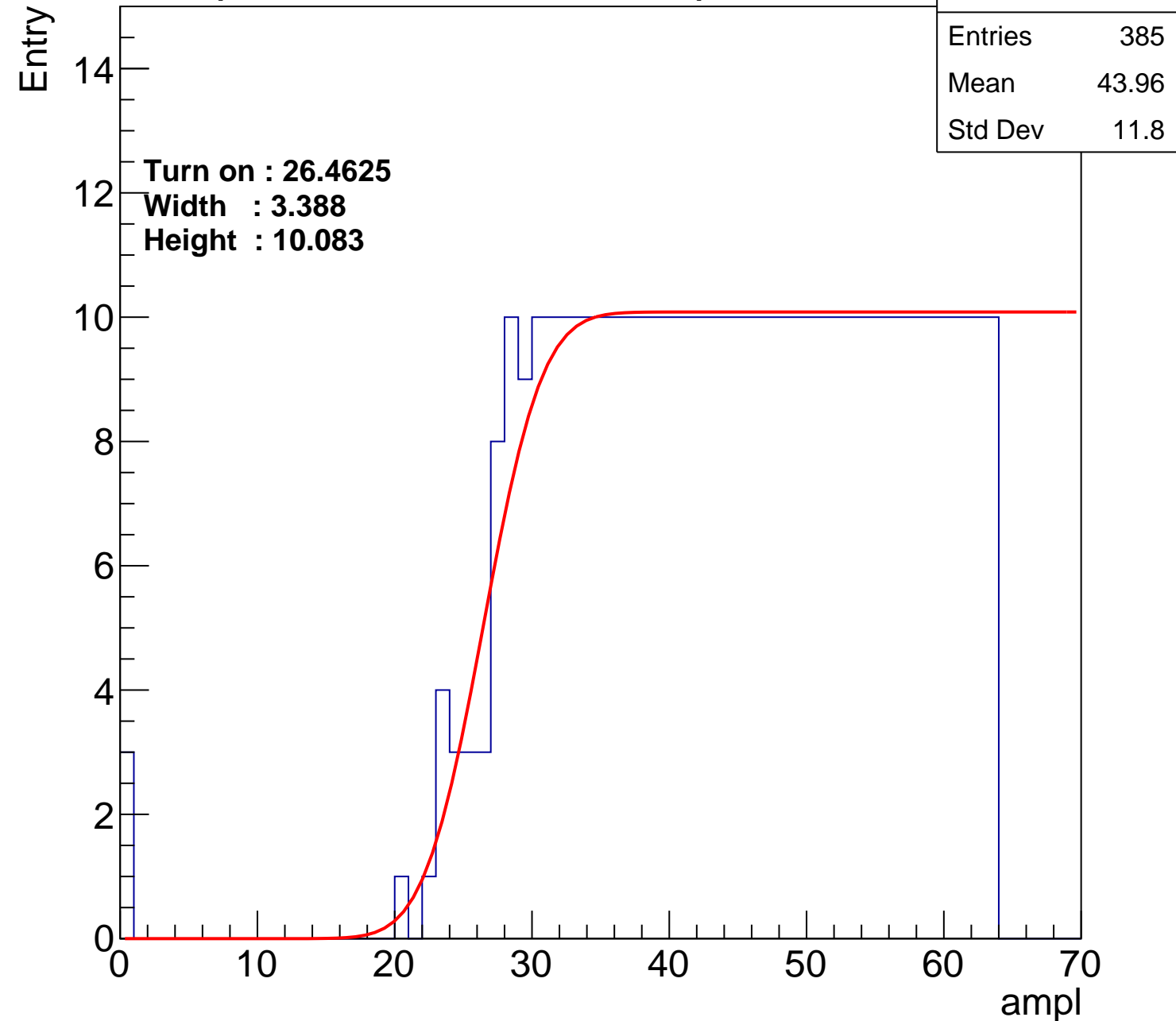
Width : 3.388

Height : 10.083

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch73

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	353
Mean	45.45
Std Dev	11.16

Turn on : 29.8821

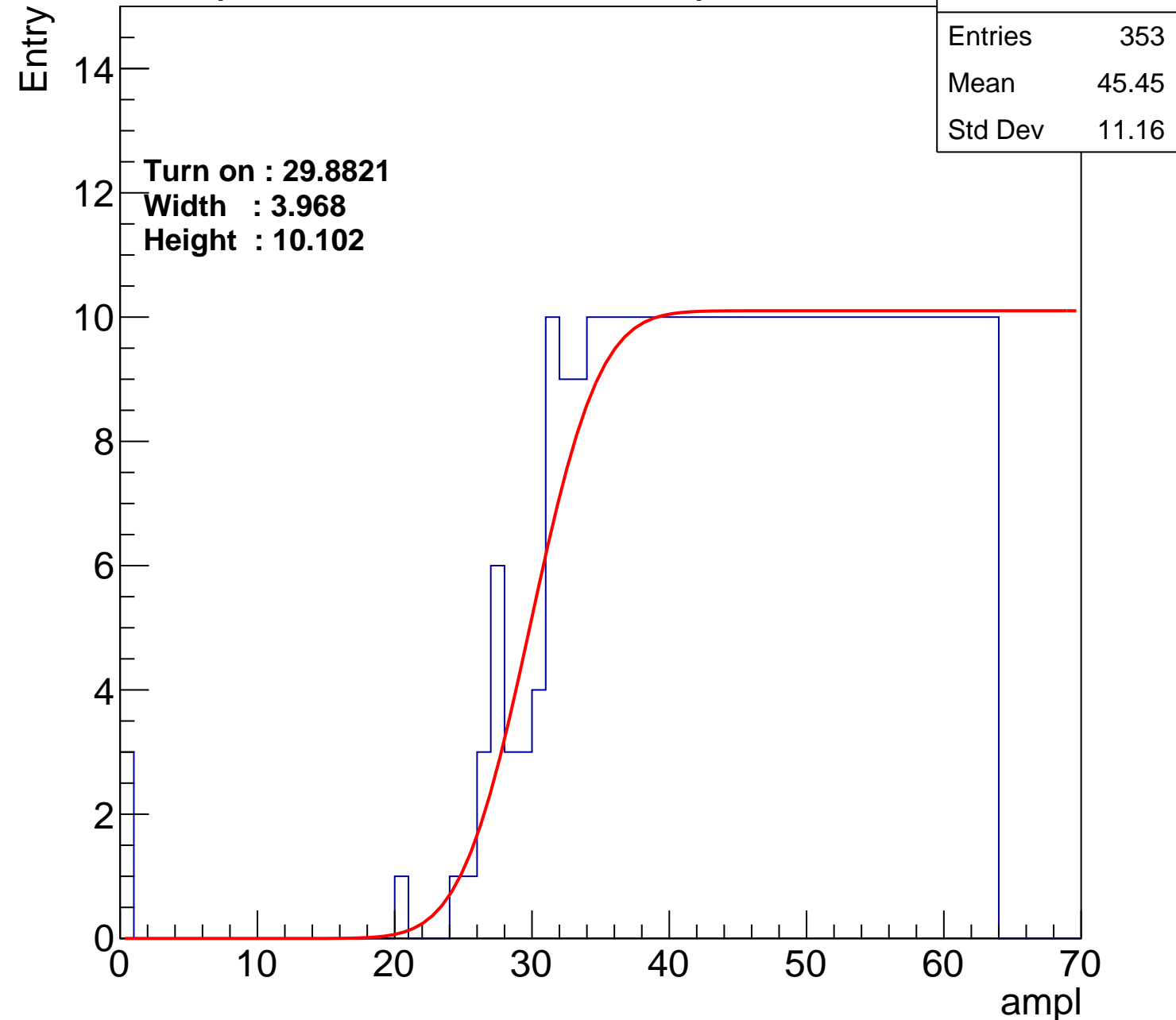
Width : 3.968

Height : 10.102

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch74

calib\_packv5\_042523\_0143.root, FC#0, port D2

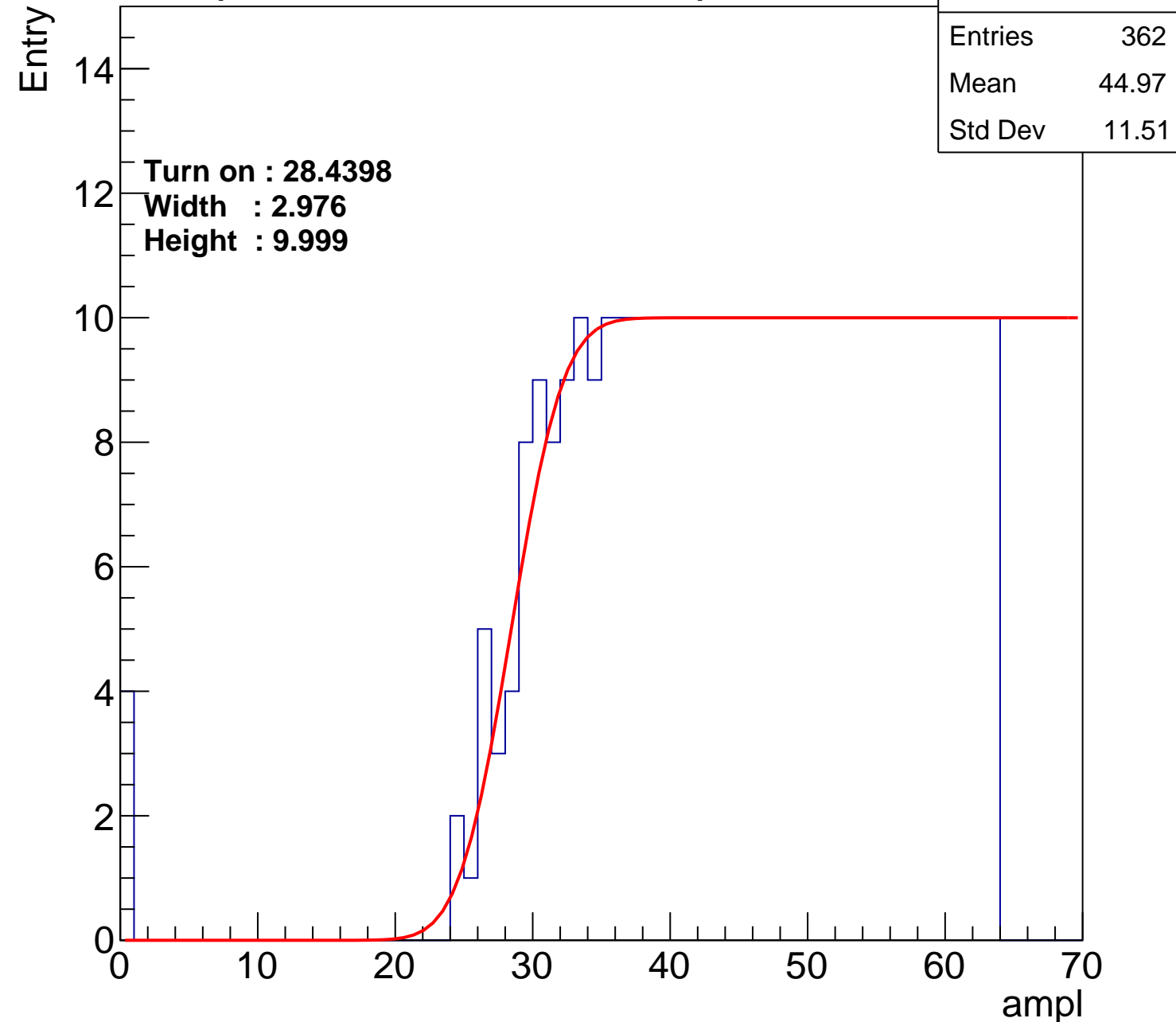
Entry

14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 28.4398**  
**Width : 2.976**  
**Height : 9.999**

Entries	362
Mean	44.97
Std Dev	11.51

ampl



# B1L101S, U26-ch75

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	368
Mean	44.82
Std Dev	11.26

Turn on : 27.7226

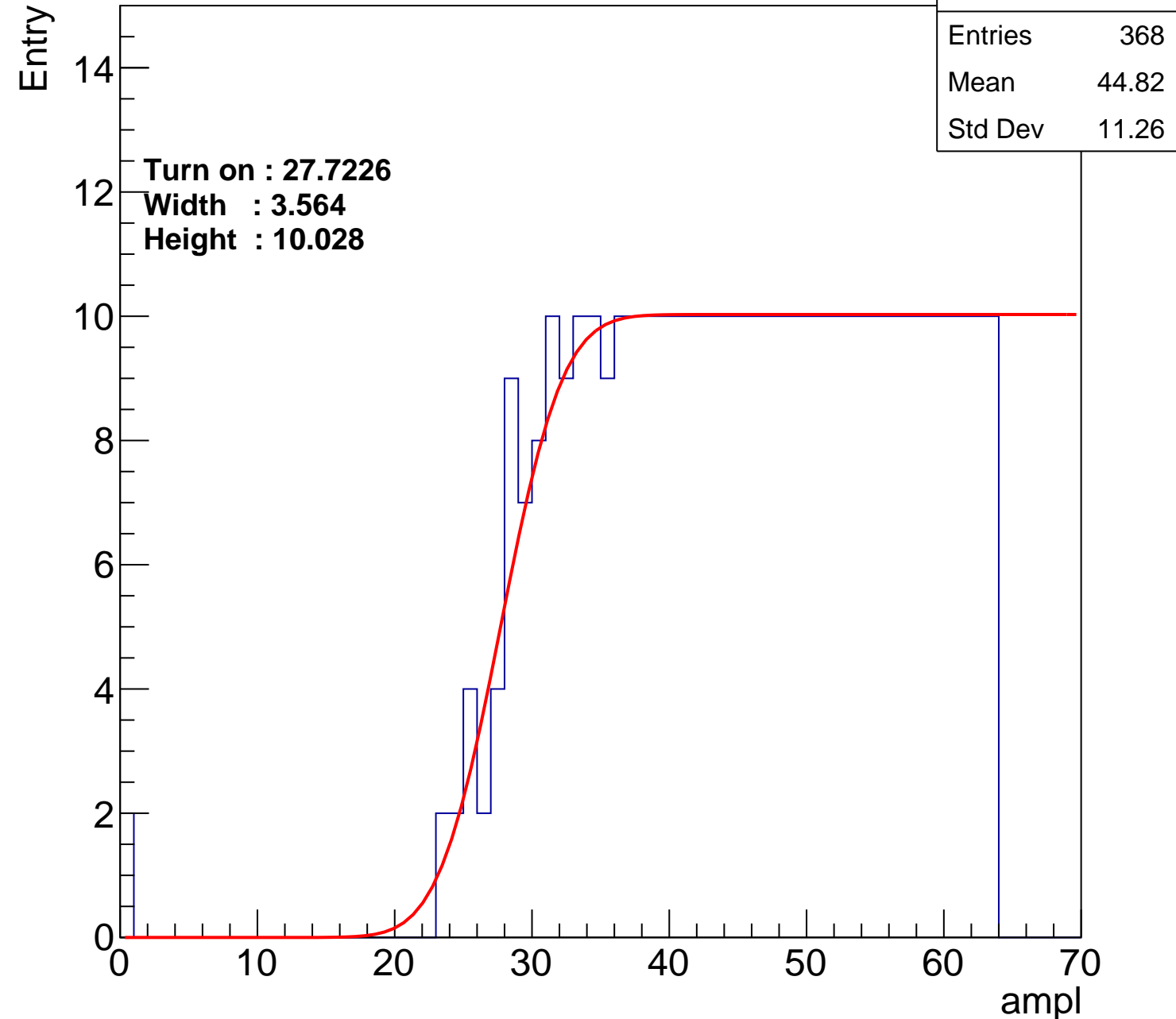
Width : 3.564

Height : 10.028

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch76

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	373
Mean	44.44
Std Dev	11.68

Turn on : 27.2621

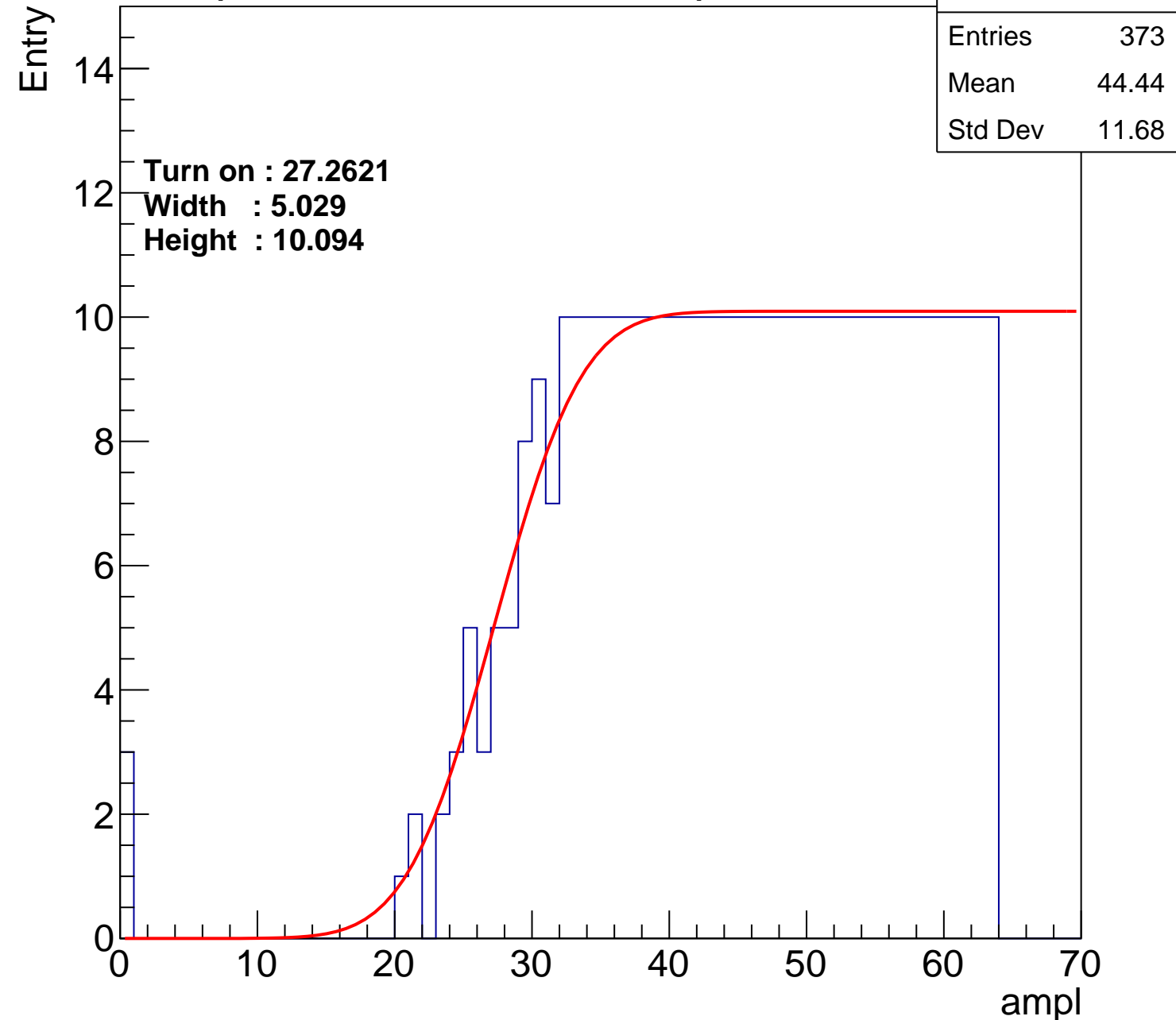
Width : 5.029

Height : 10.094

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch77

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	353
Mean	45.4
Std Dev	11.34

Turn on : 29.6393

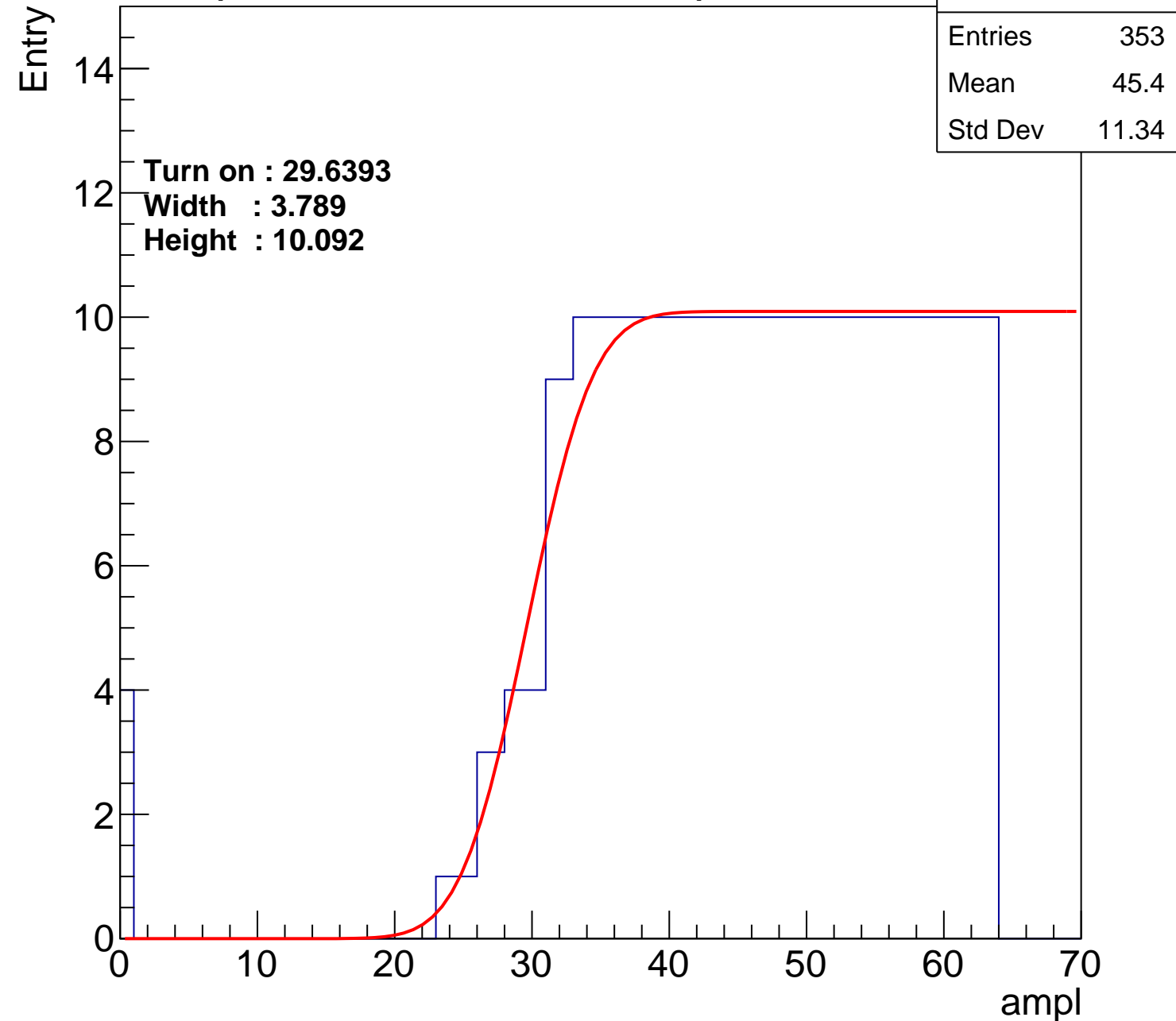
Width : 3.789

Height : 10.092

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch78

calib\_packv5\_042523\_0143.root, FC#0, port D2

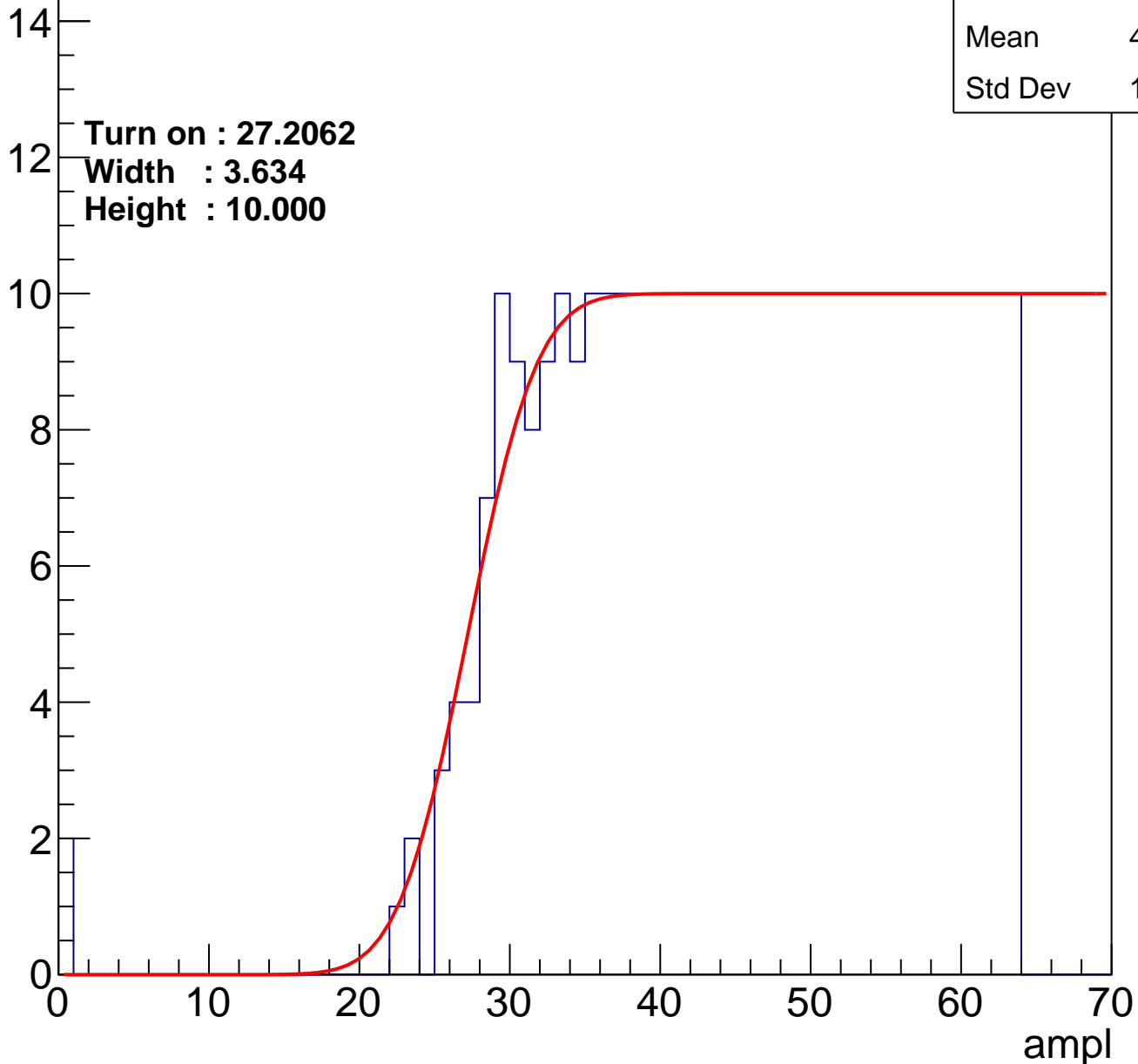
Entries	368
Mean	44.82
Std Dev	11.26

Turn on : 27.2062

Width : 3.634

Height : 10.000

Entry





# B1L101S, U26-ch79

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	333
Mean	46.5
Std Dev	10.59

**Turn on : 30.9934**

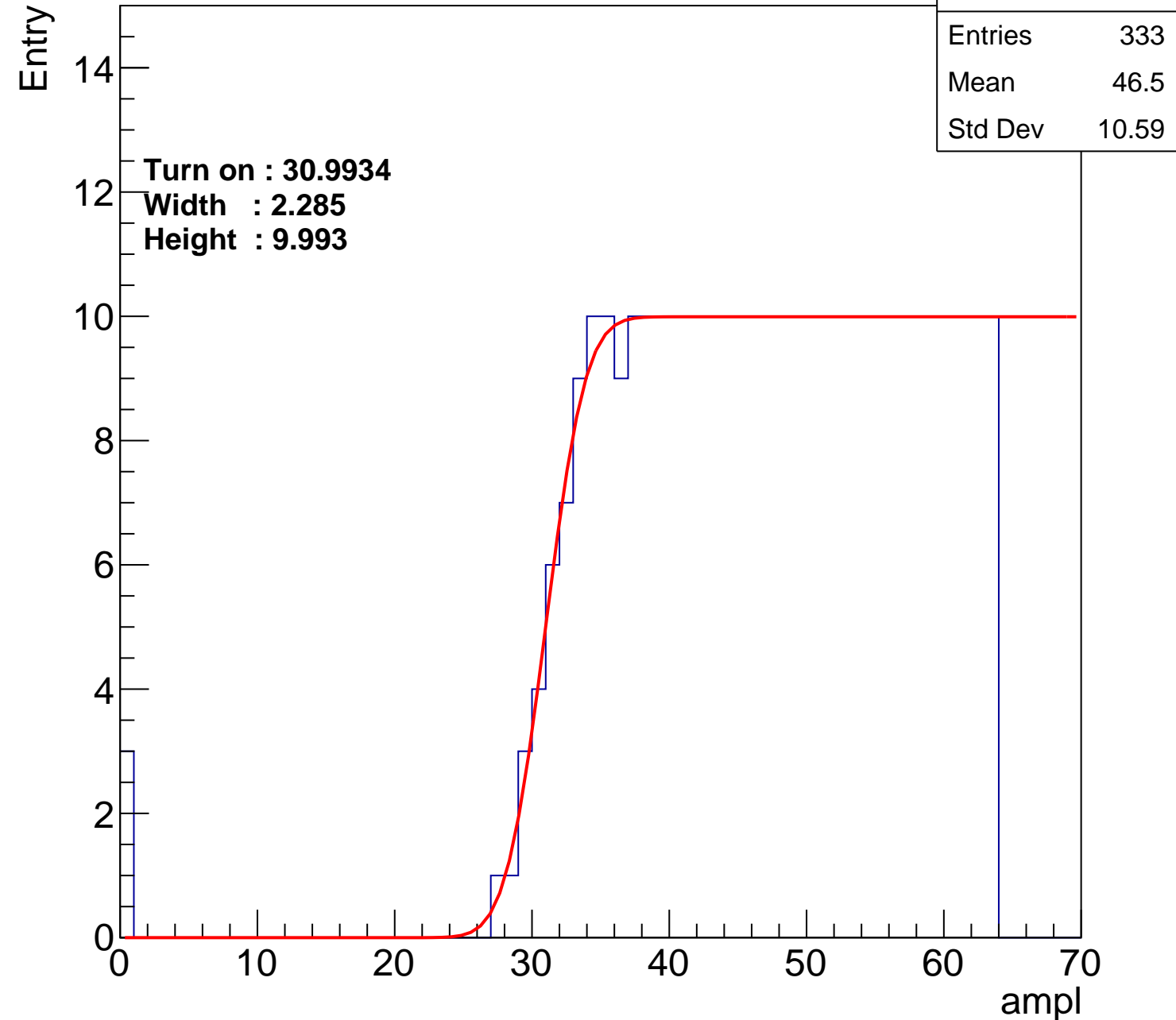
**Width : 2.285**

**Height : 9.993**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch80

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	371
Mean	44.69
Std Dev	11.3

Turn on : 27.2043

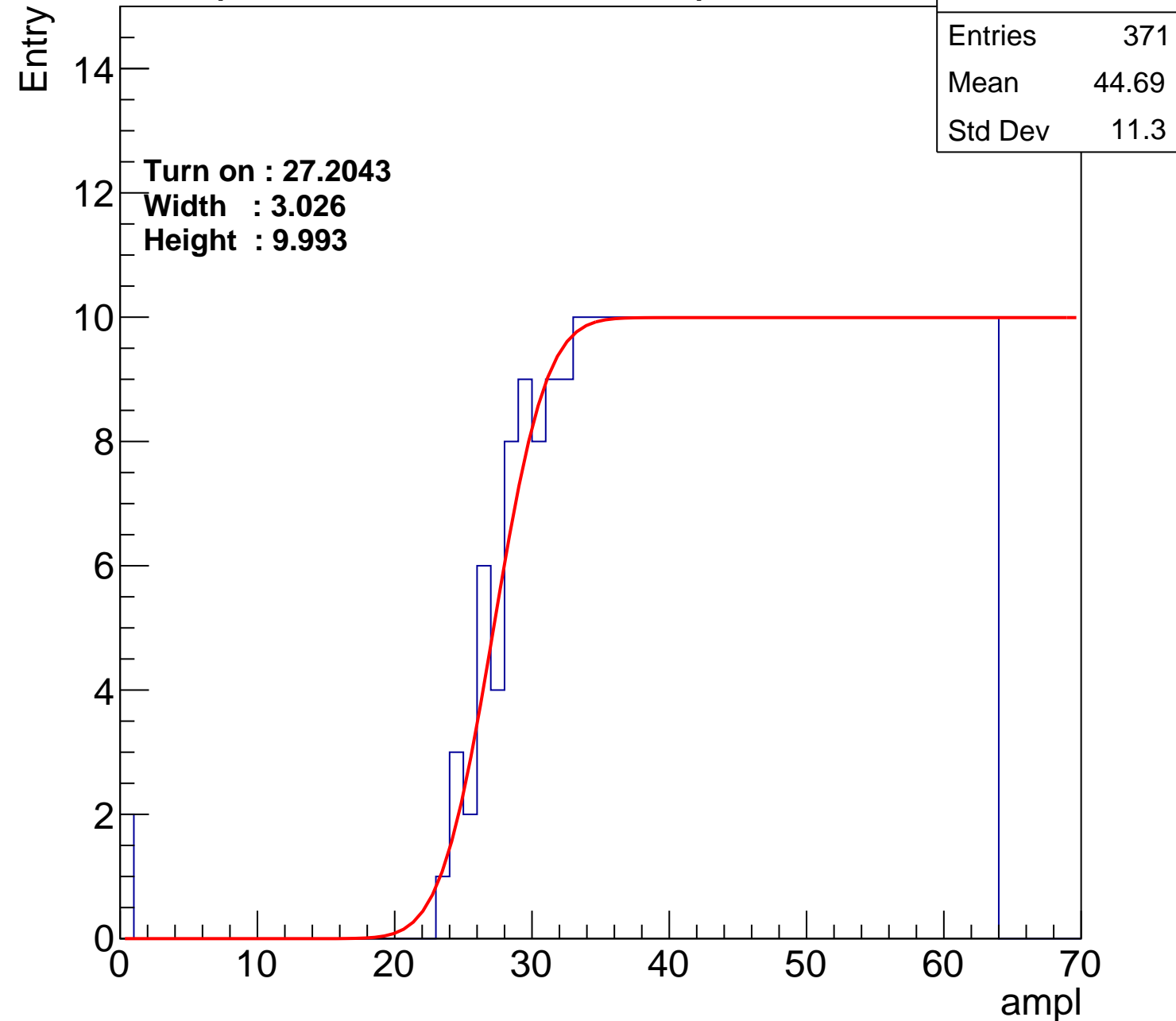
Width : 3.026

Height : 9.993

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch81

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	353
Mean	45.57
Std Dev	10.87

**Turn on : 29.0070**

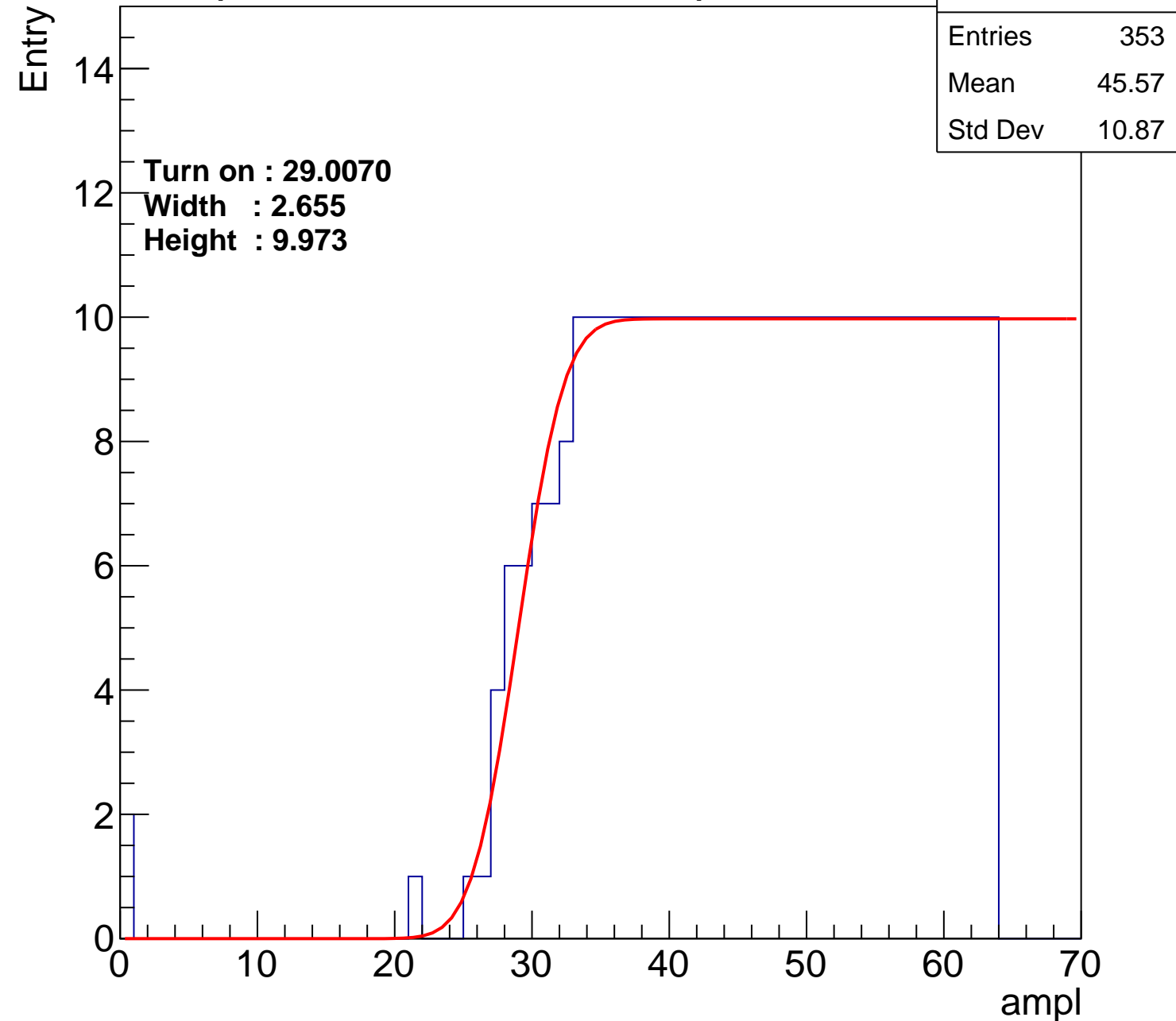
**Width : 2.655**

**Height : 9.973**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch82

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	366
Mean	44.73
Std Dev	11.75

Turn on : 27.9030

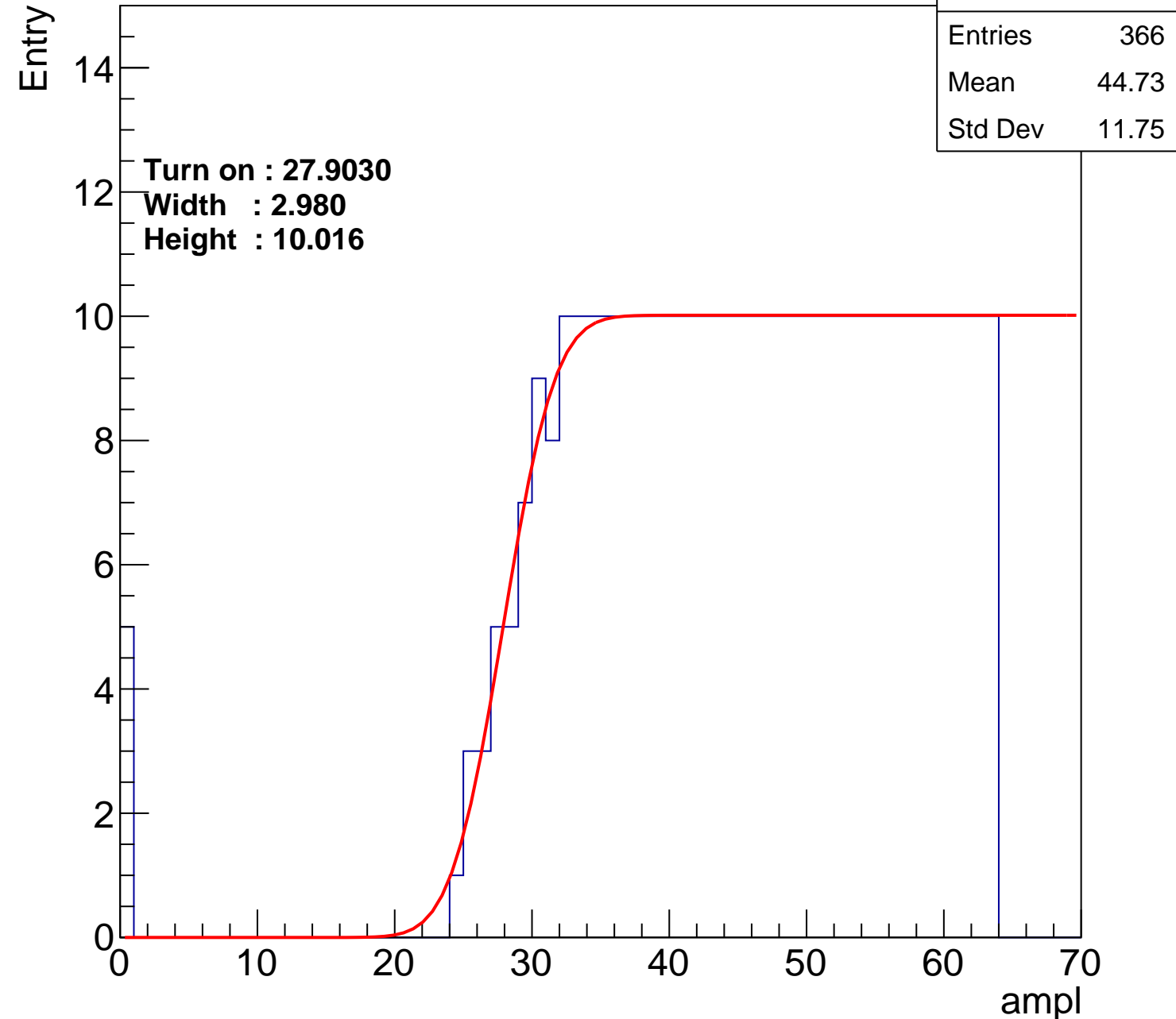
Width : 2.980

Height : 10.016

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch83

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	370
Mean	44.63
Std Dev	11.62

Turn on : 27.5618

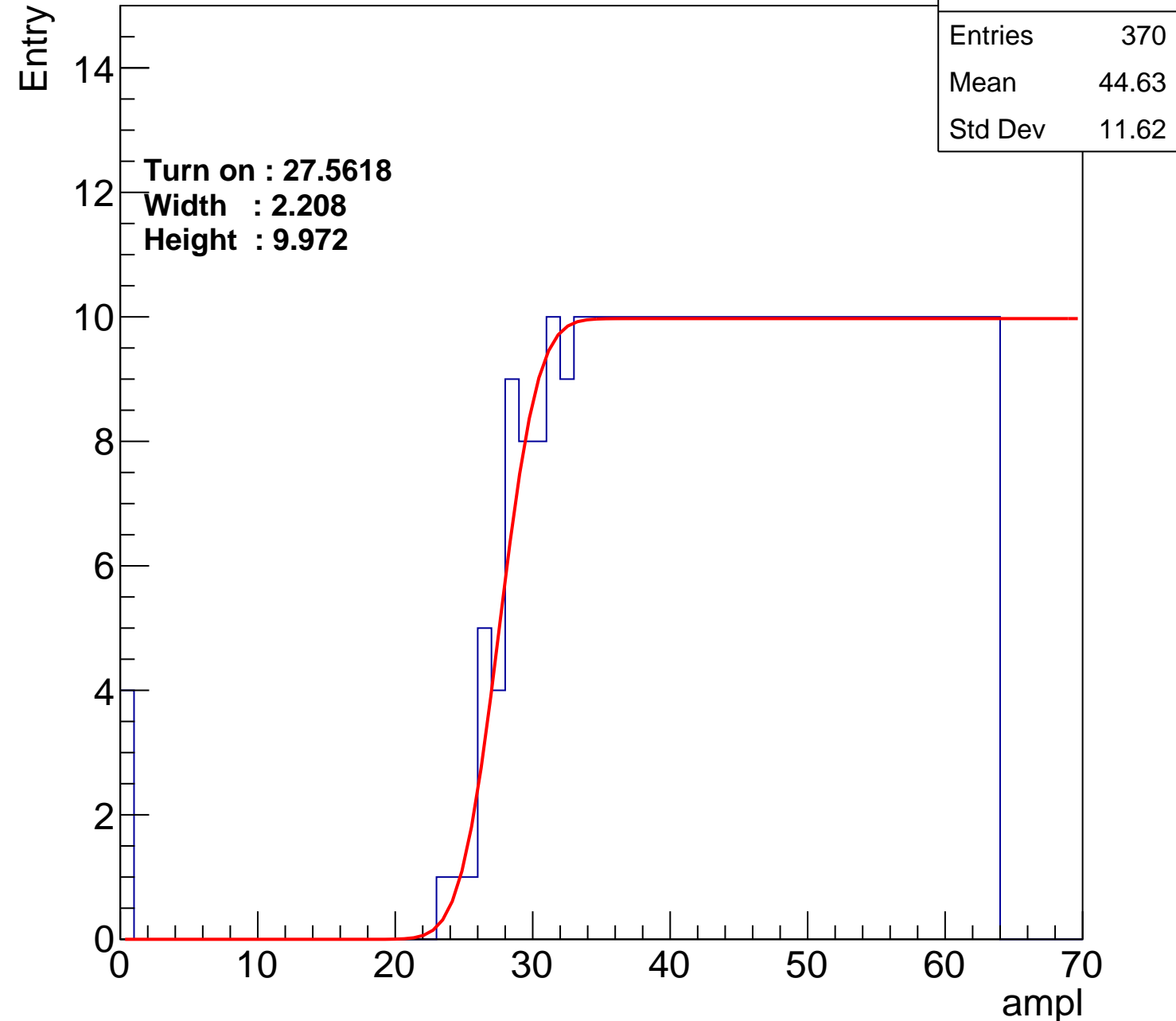
Width : 2.208

Height : 9.972

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch84

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	361
Mean	45.01
Std Dev	11.51

Turn on : 28.4181

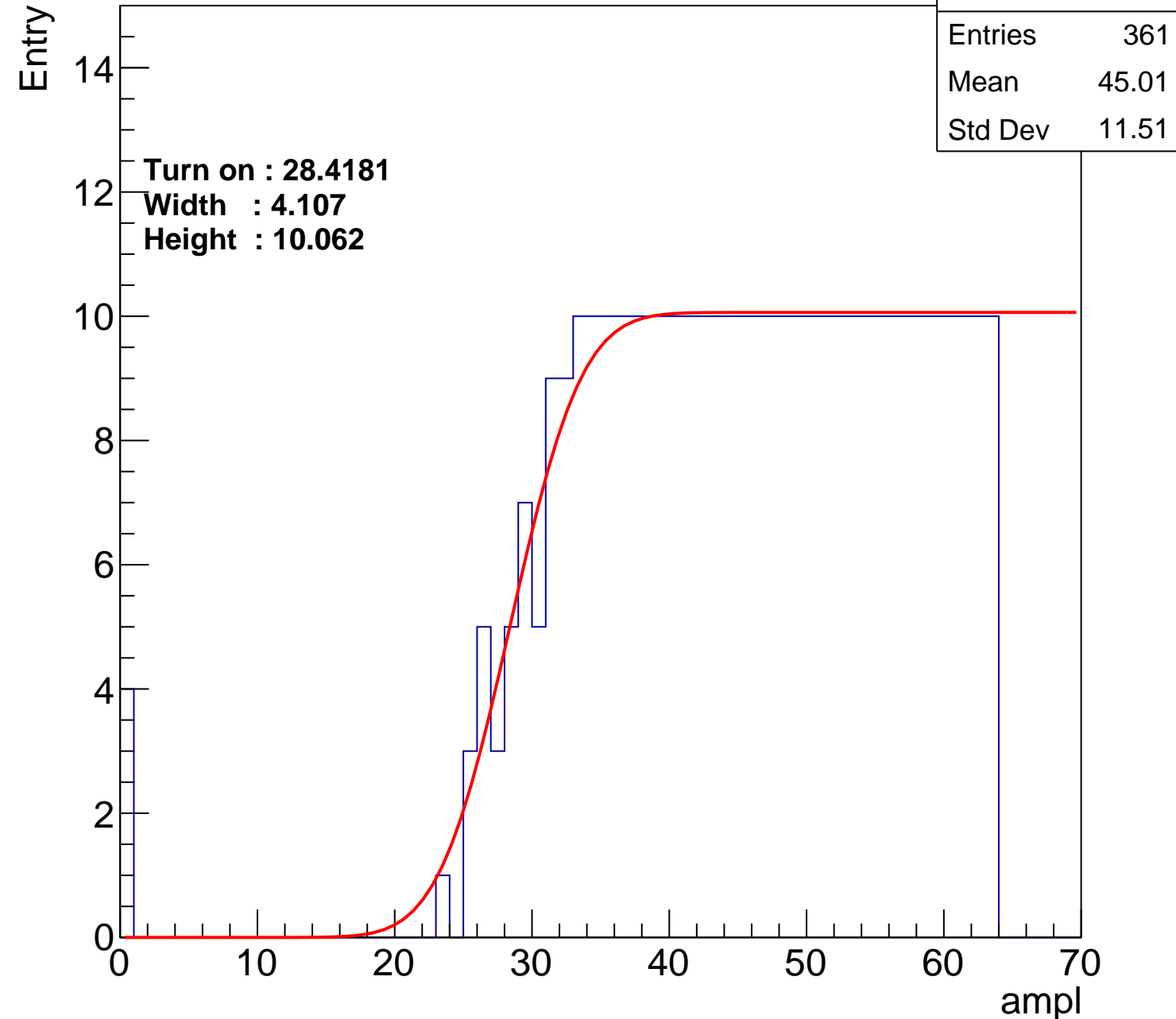
Width : 4.107

Height : 10.062

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch85

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	358
Mean	45.04
Std Dev	11.79

Turn on : 28.5321

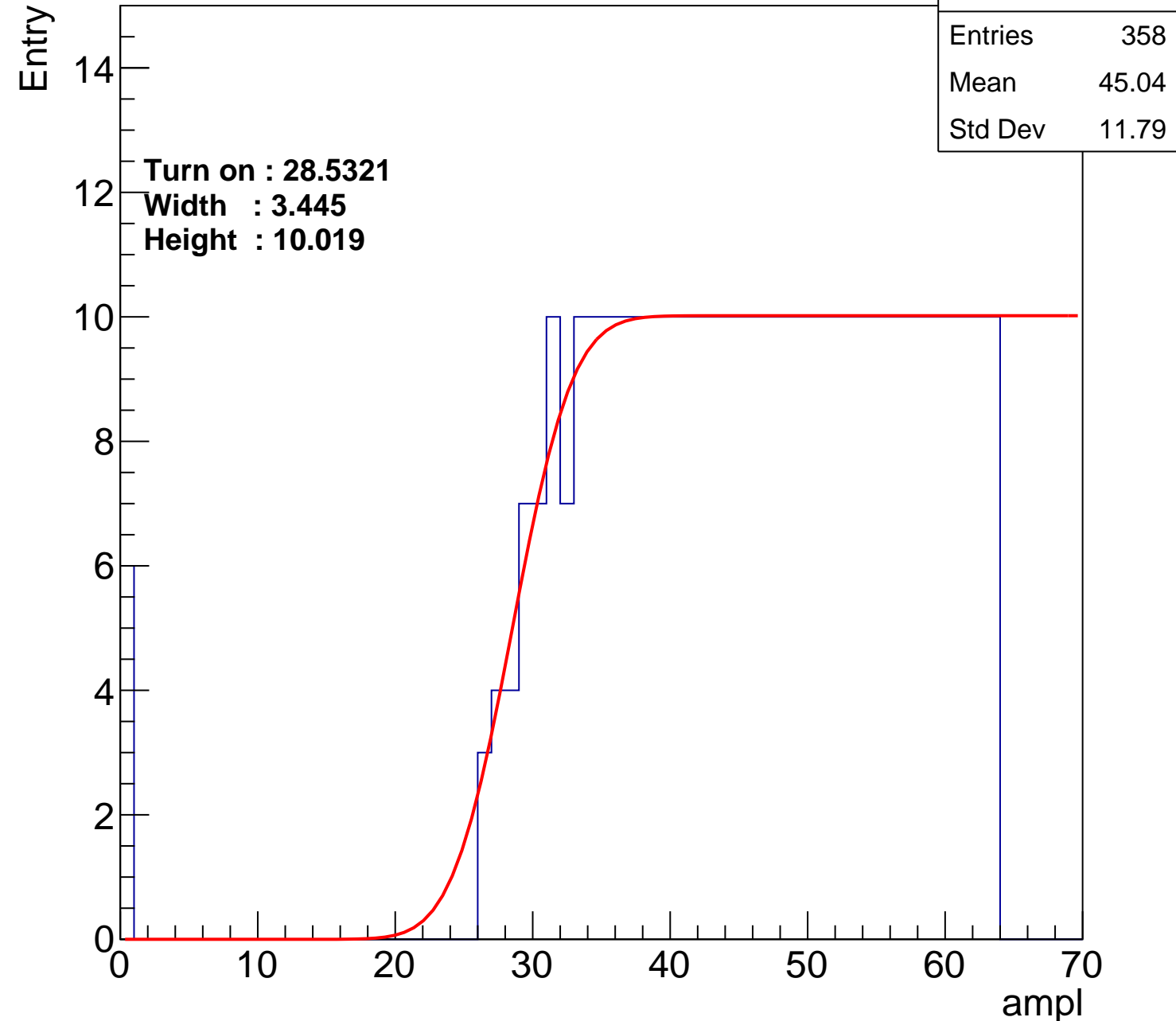
Width : 3.445

Height : 10.019

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch86

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	383
Mean	44.15
Std Dev	11.54

Turn on : 25.9689

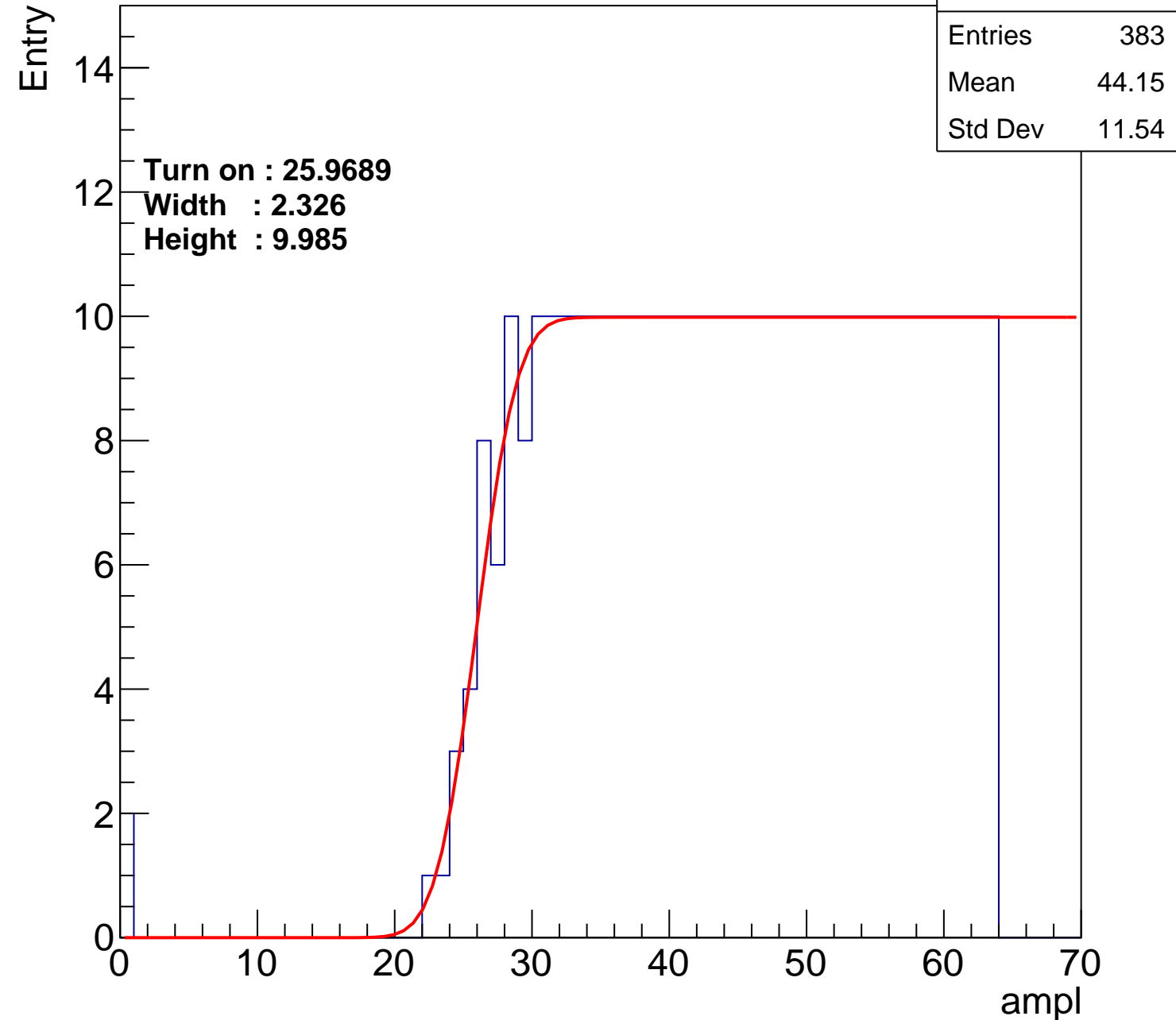
Width : 2.326

Height : 9.985

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U26-ch87

calib\_packv5\_042523\_0143.root, FC#0, port D2

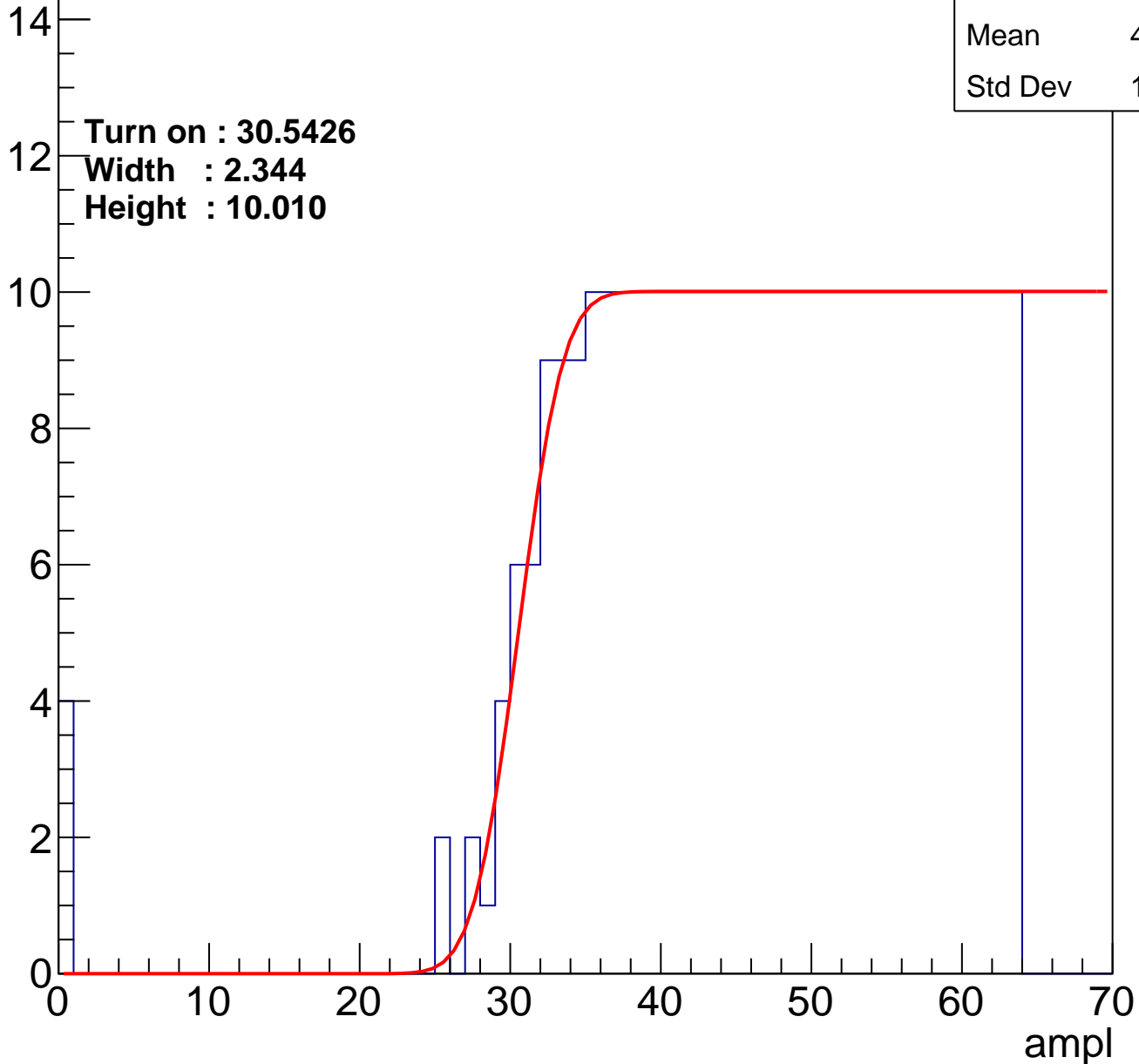
Entries	342
Mean	45.95
Std Dev	11.07

Turn on : 30.5426

Width : 2.344

Height : 10.010

Entry



# B1L101S, U26-ch88

calib\_packv5\_042523\_0143.root, FC#0, port D2

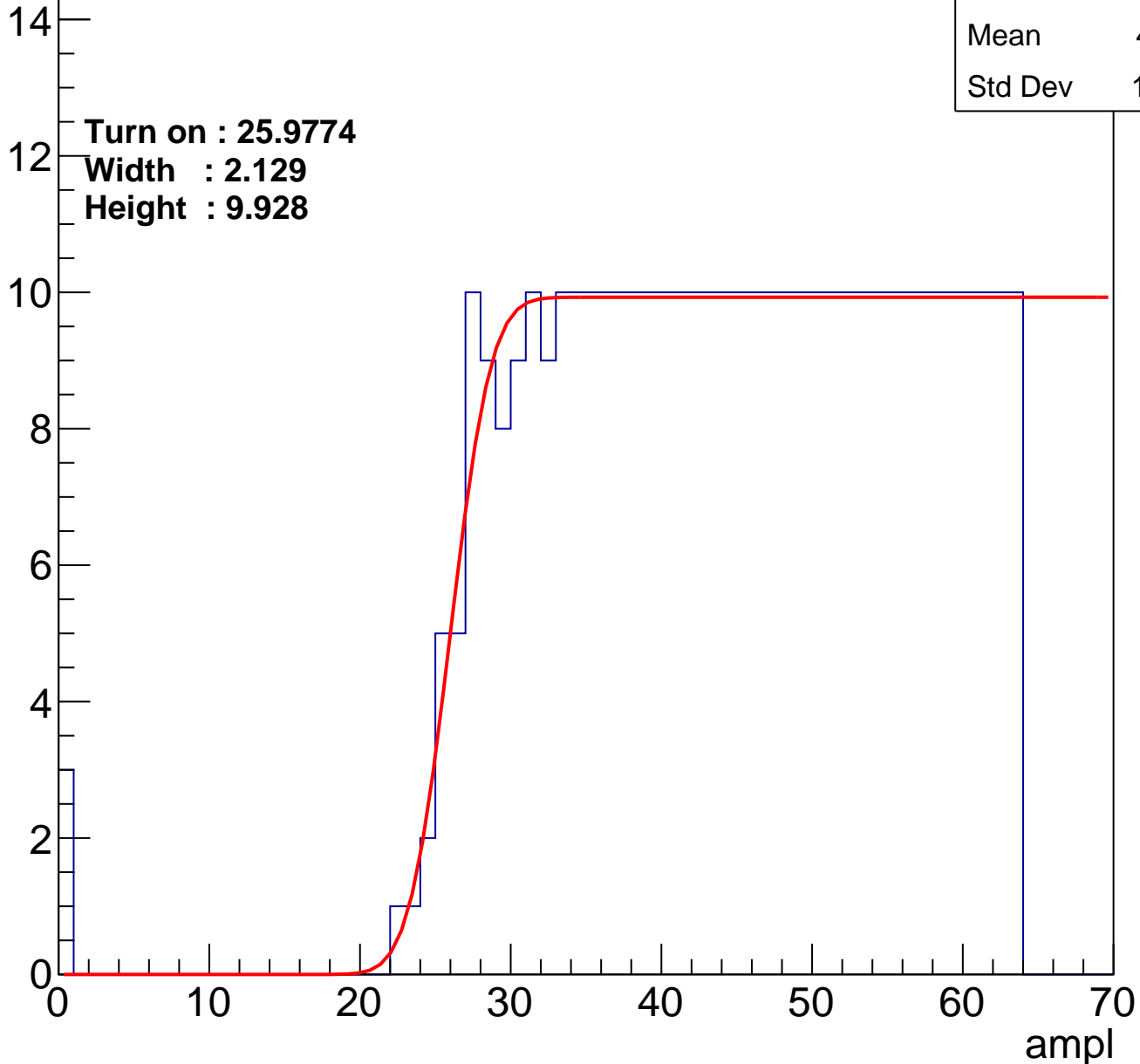
Entries	382
Mean	44.11
Std Dev	11.72

**Turn on : 25.9774**

**Width : 2.129**

**Height : 9.928**

Entry



# B1L101S, U26-ch89

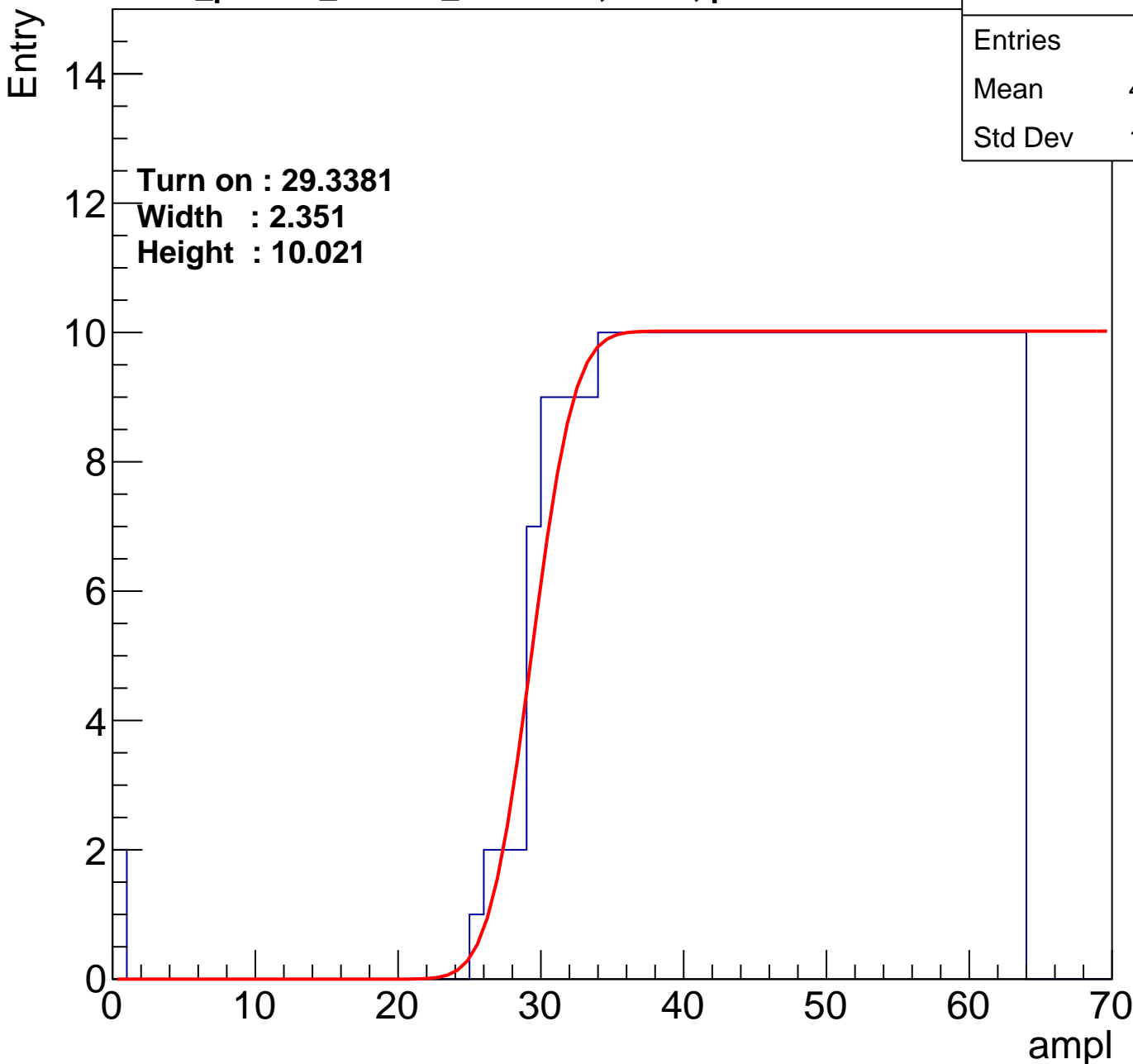
**calib\_packv5\_042523\_0143.root, FC#0, port D2**

Entries	352
Mean	45.66
Std Dev	10.76

**Turn on : 29.3381**

**Width : 2.351**

**Height : 10.021**



# B1L101S, U26-ch90

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	383
Mean	44.13
Std Dev	11.51

Turn on : 26.0830

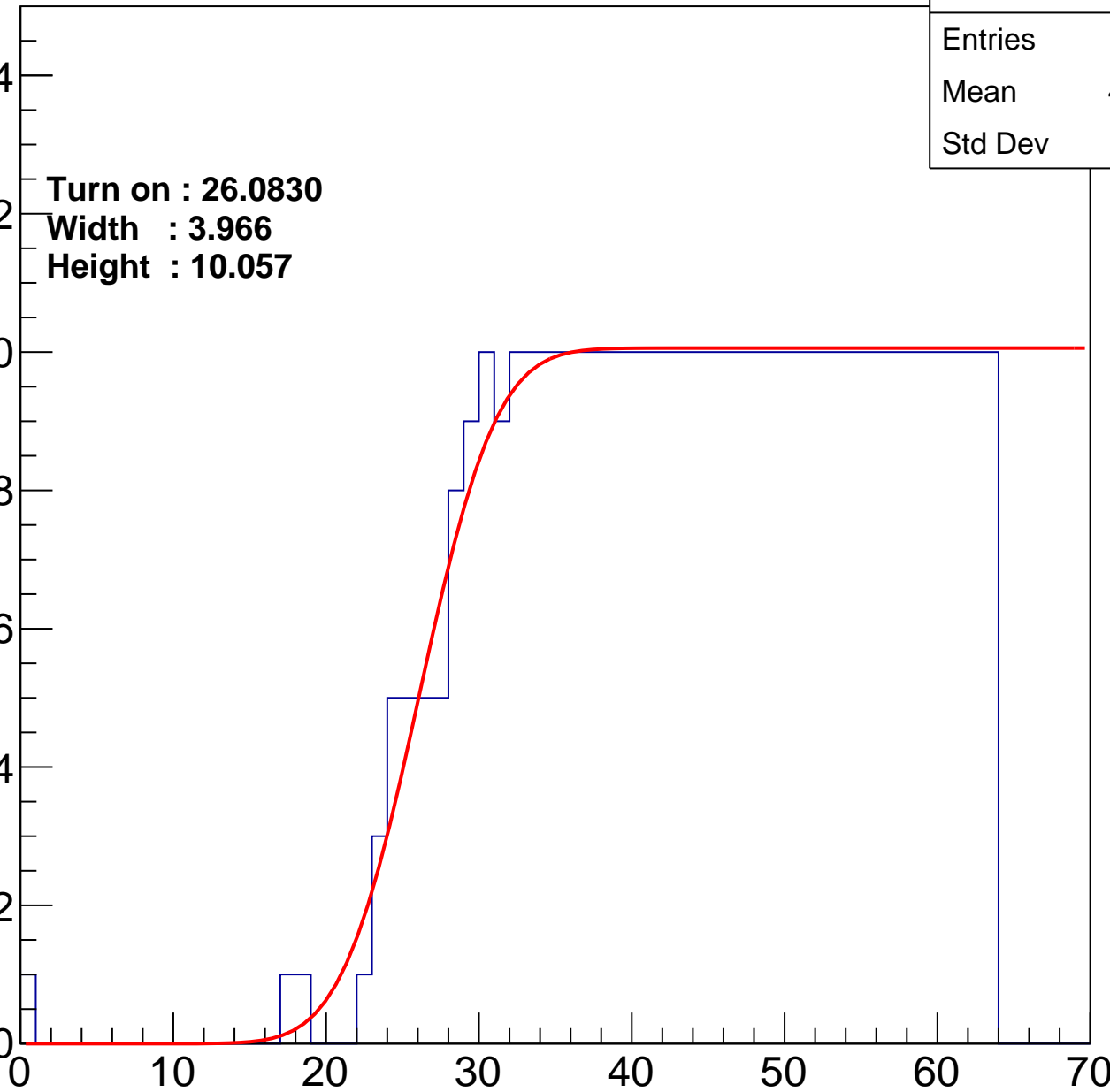
Width : 3.966

Height : 10.057

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch91

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	345
Mean	45.68
Std Dev	11.42

Turn on : 30.4709

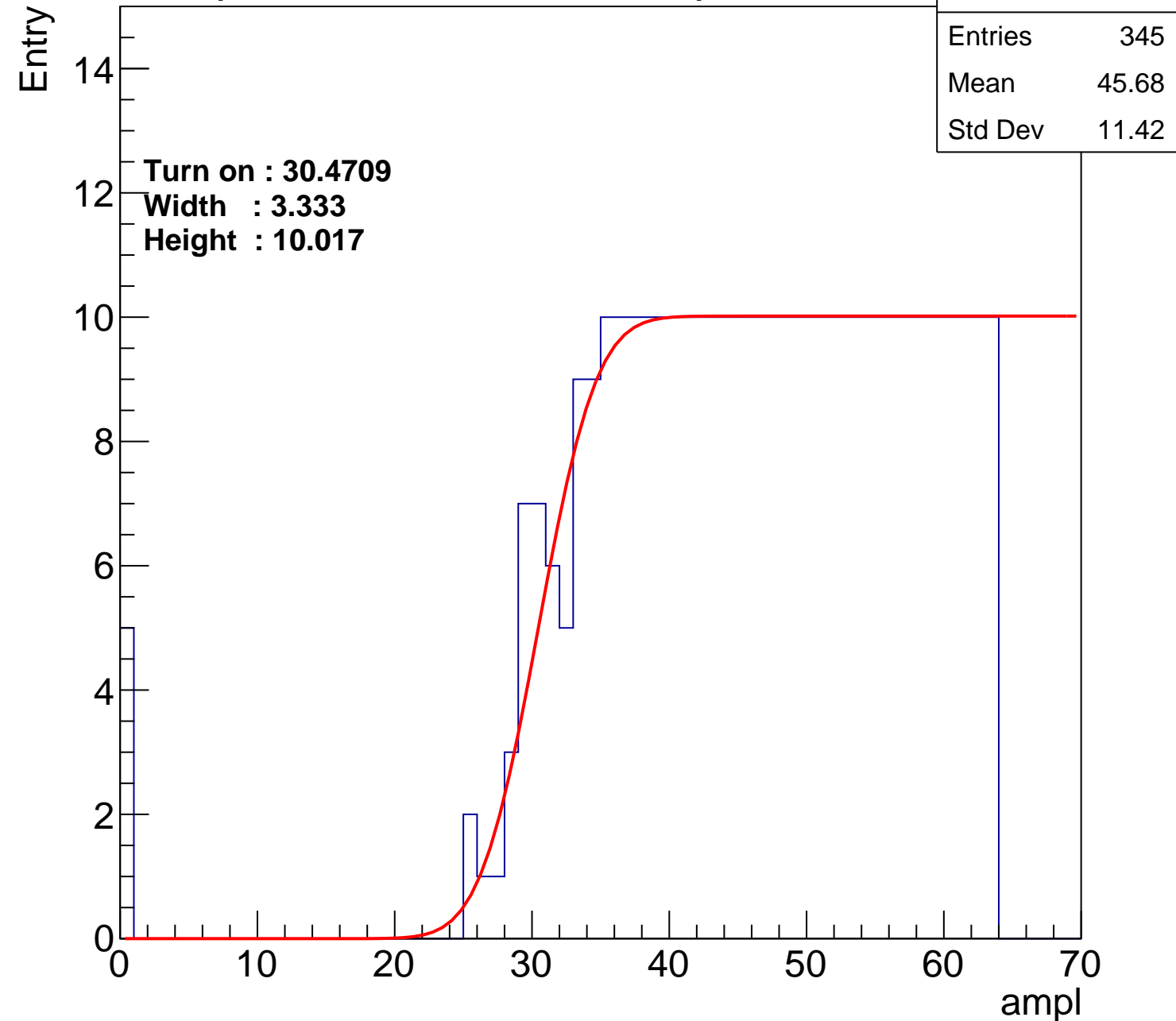
Width : 3.333

Height : 10.017

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch92

calib\_packv5\_042523\_0143.root, FC#0, port D2

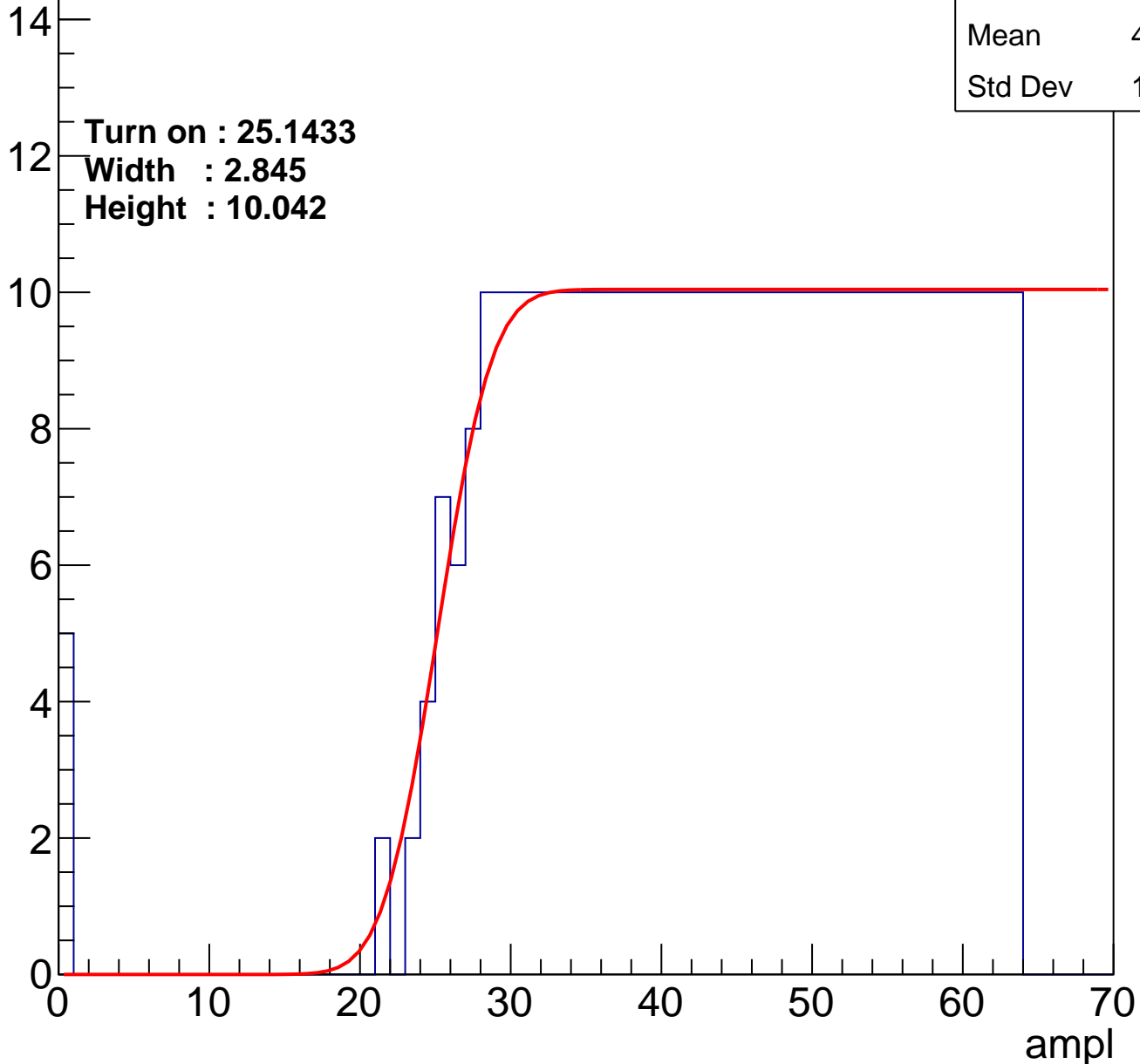
Entries	394
Mean	43.43
Std Dev	12.29

Turn on : 25.1433

Width : 2.845

Height : 10.042

Entry



# B1L101S, U26-ch93

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	366
Mean	44.97
Std Dev	11.12

Turn on : 27.6054

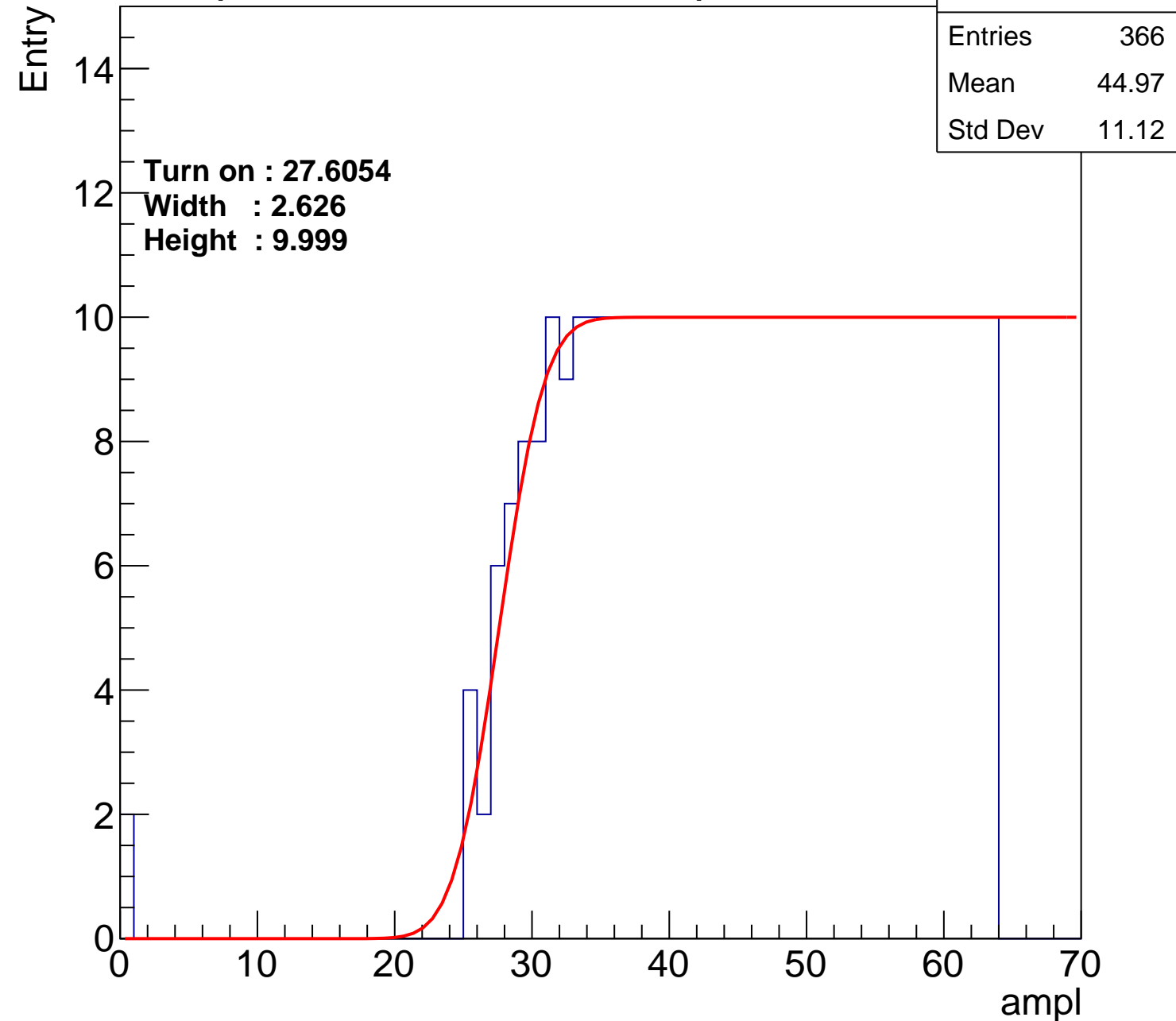
Width : 2.626

Height : 9.999

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch94

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	385
Mean	43.98
Std Dev	11.63

Turn on : 25.9200

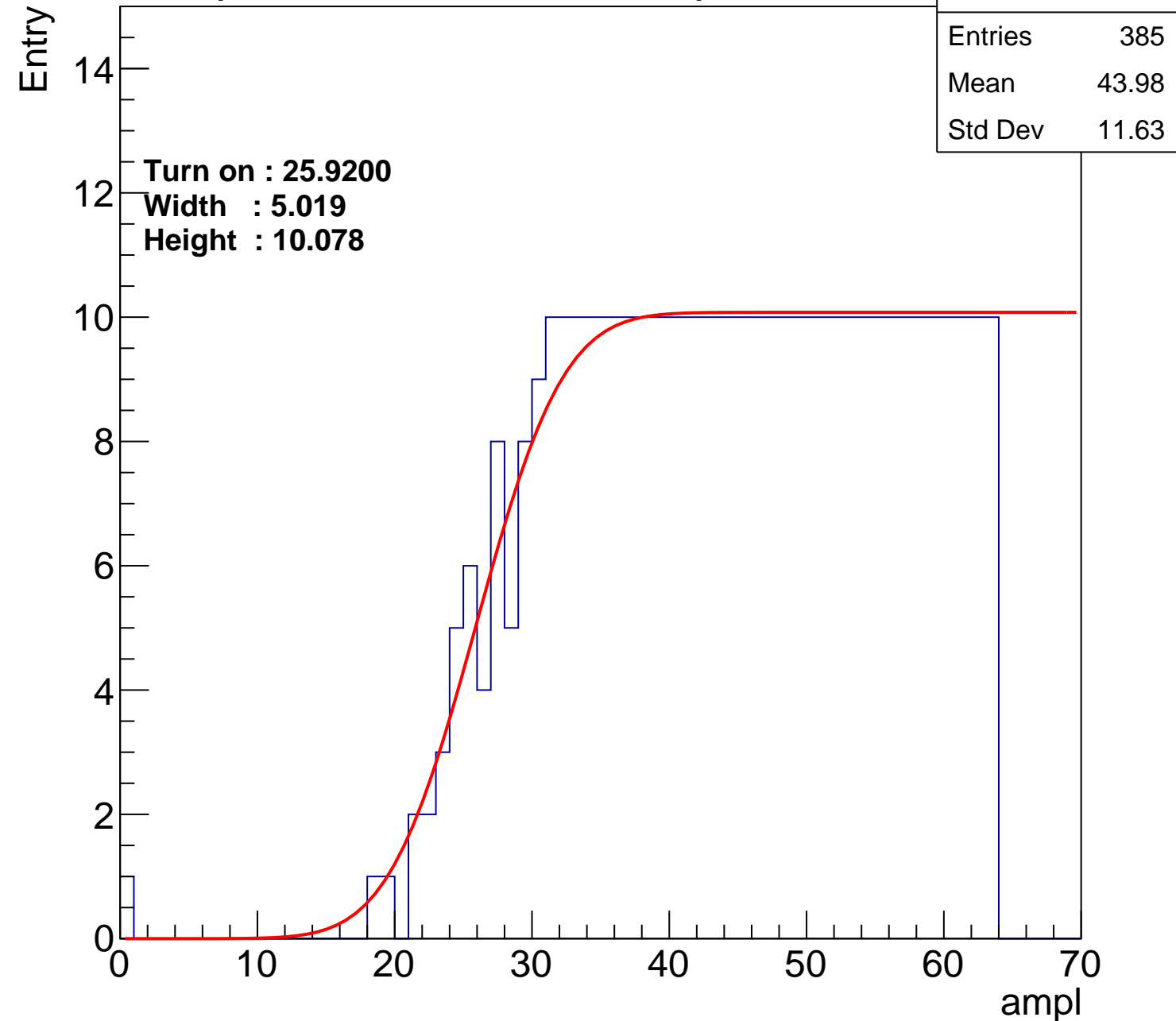
Width : 5.019

Height : 10.078

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U26-ch95

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	363
Mean	45.2
Std Dev	10.83

Turn on : 27.7344

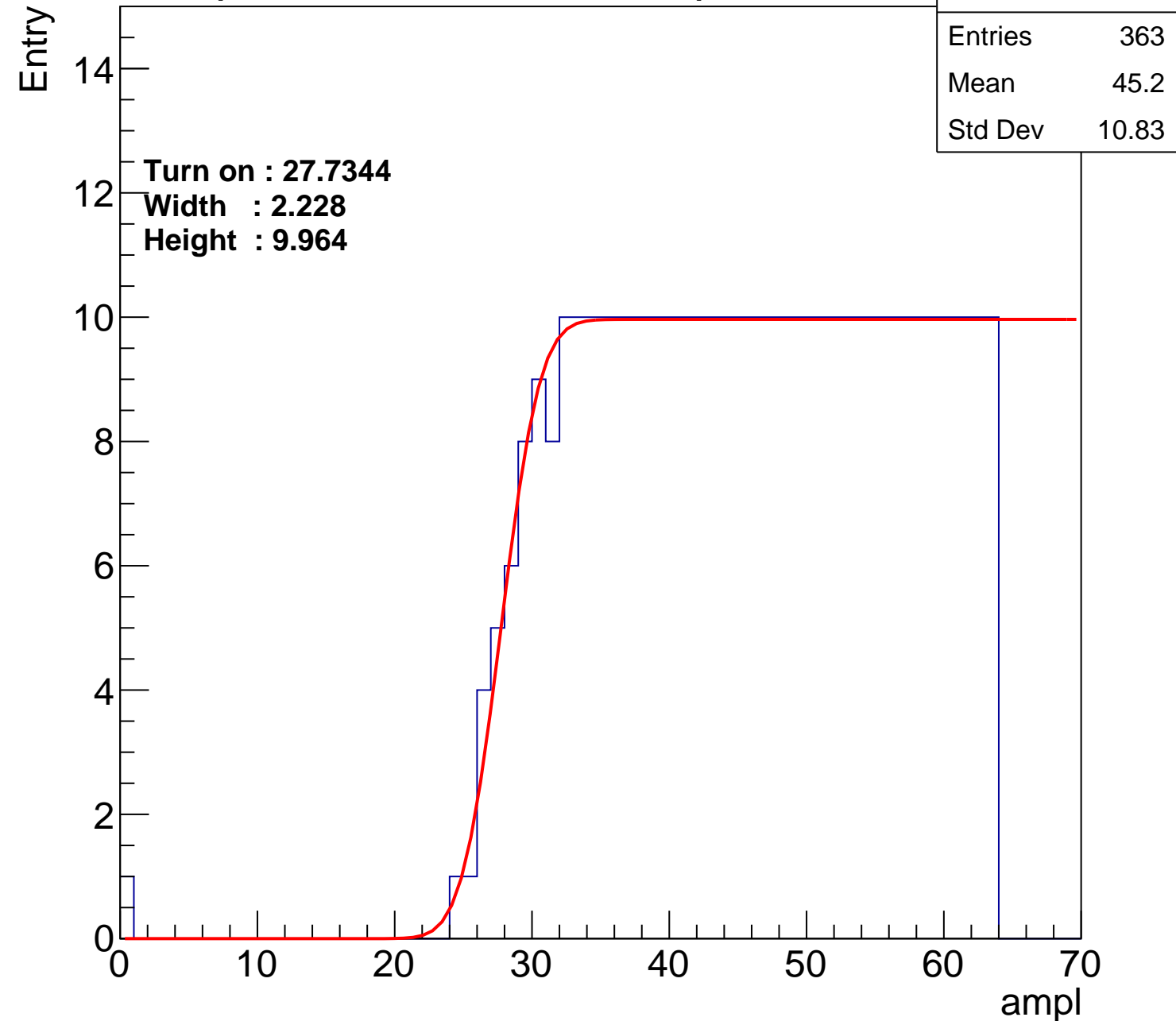
Width : 2.228

Height : 9.964

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch96

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	365
Mean	45.09
Std Dev	10.9

Turn on : 27.7250

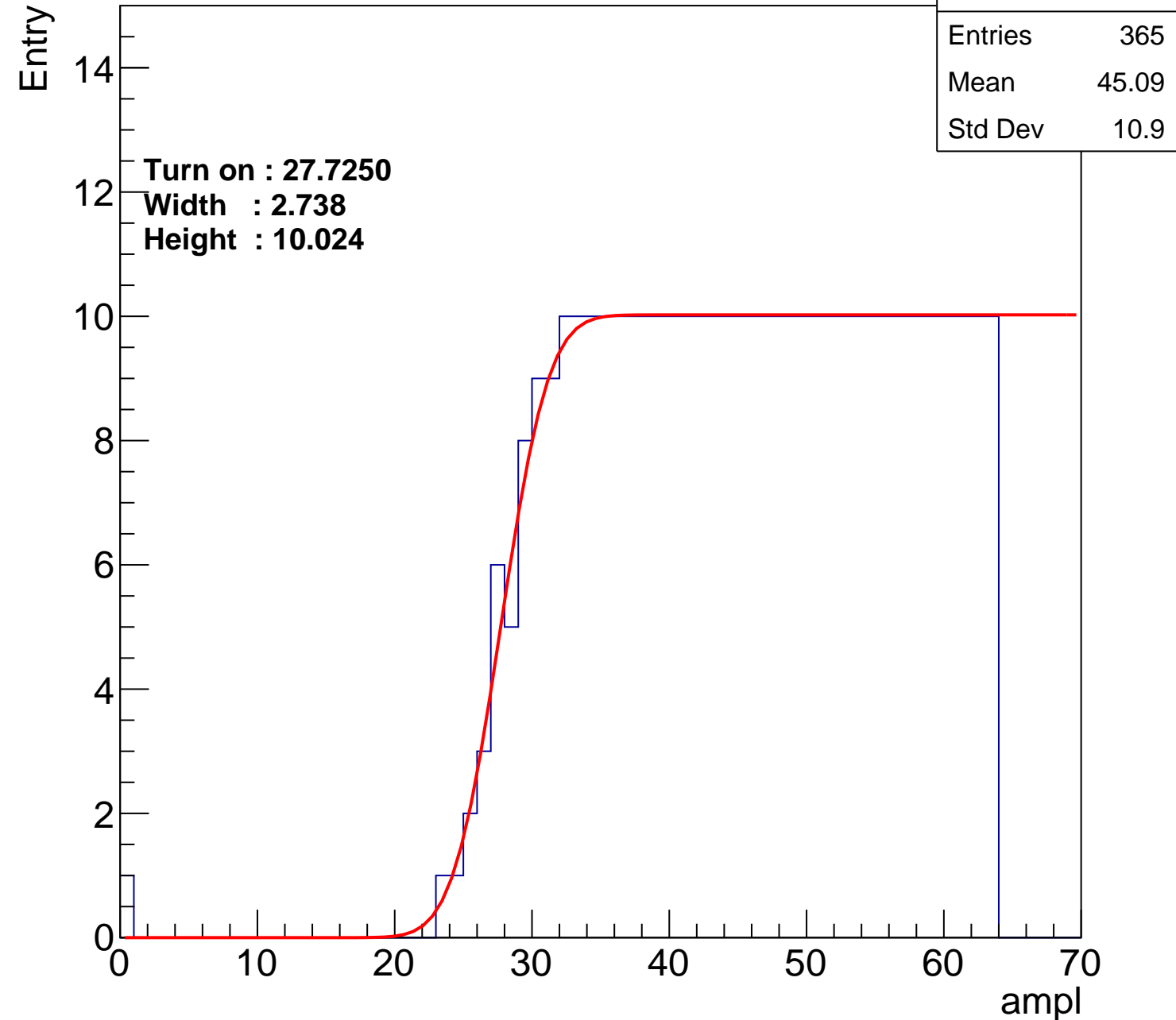
Width : 2.738

Height : 10.024

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch97

calib\_packv5\_042523\_0143.root, FC#0, port D2

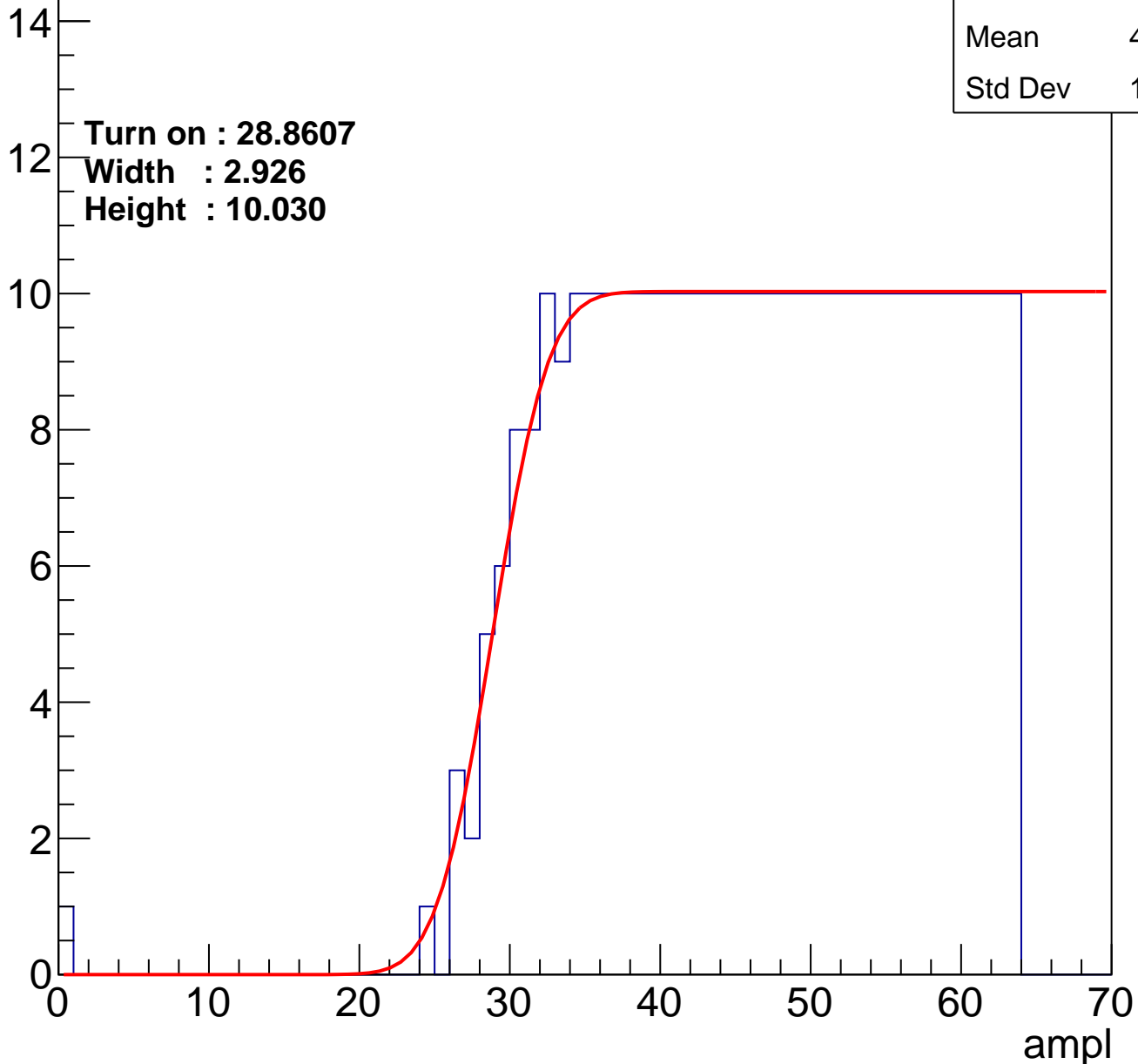
Entries	353
Mean	45.68
Std Dev	10.58

Turn on : 28.8607

Width : 2.926

Height : 10.030

Entry



# B1L101S, U26-ch98

calib\_packv5\_042523\_0143.root, FC#0, port D2

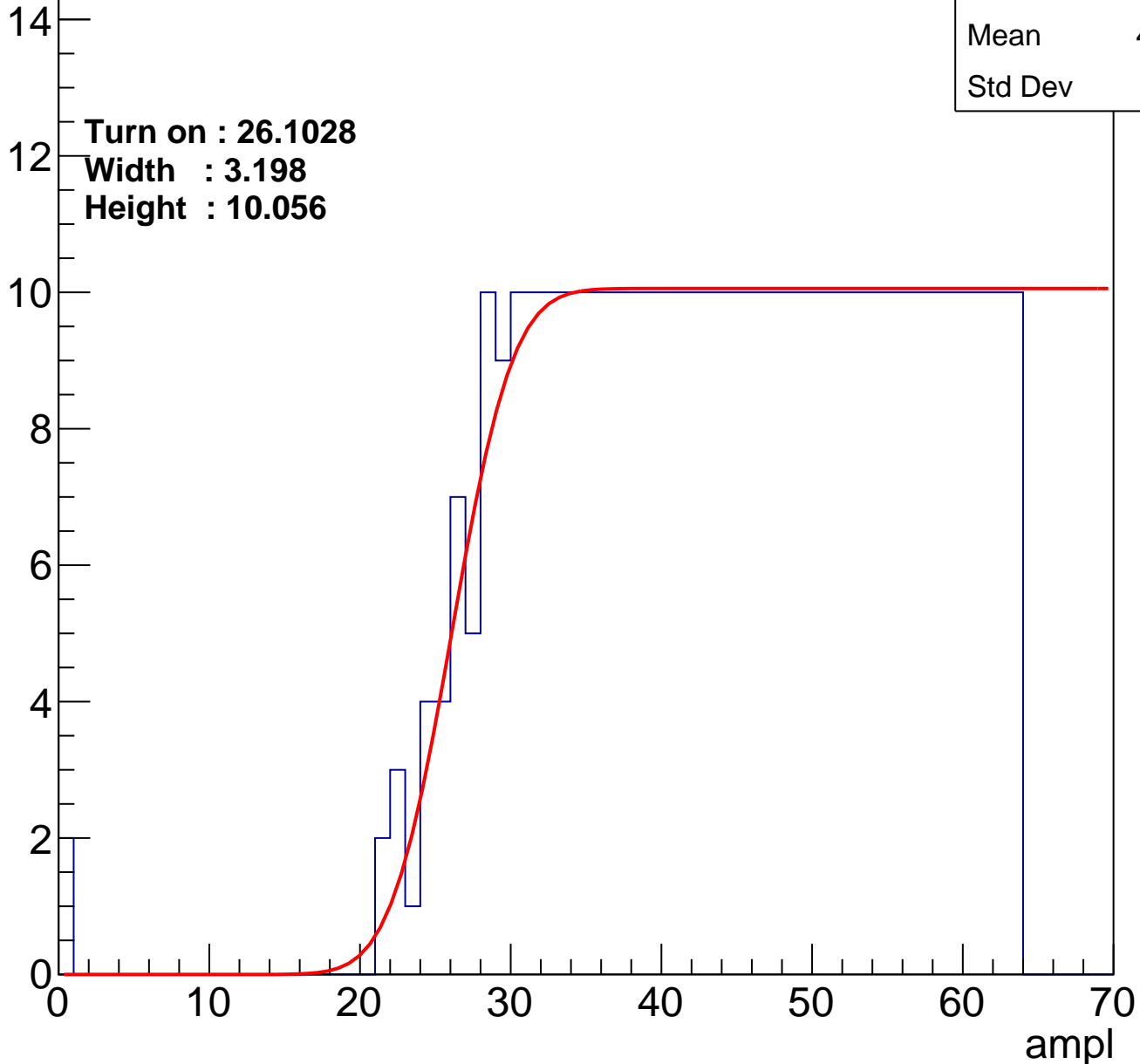
Entries	387
Mean	43.91
Std Dev	11.7

Turn on : 26.1028

Width : 3.198

Height : 10.056

Entry



# B1L101S, U26-ch99

calib\_packv5\_042523\_0143.root, FC#0, port D2

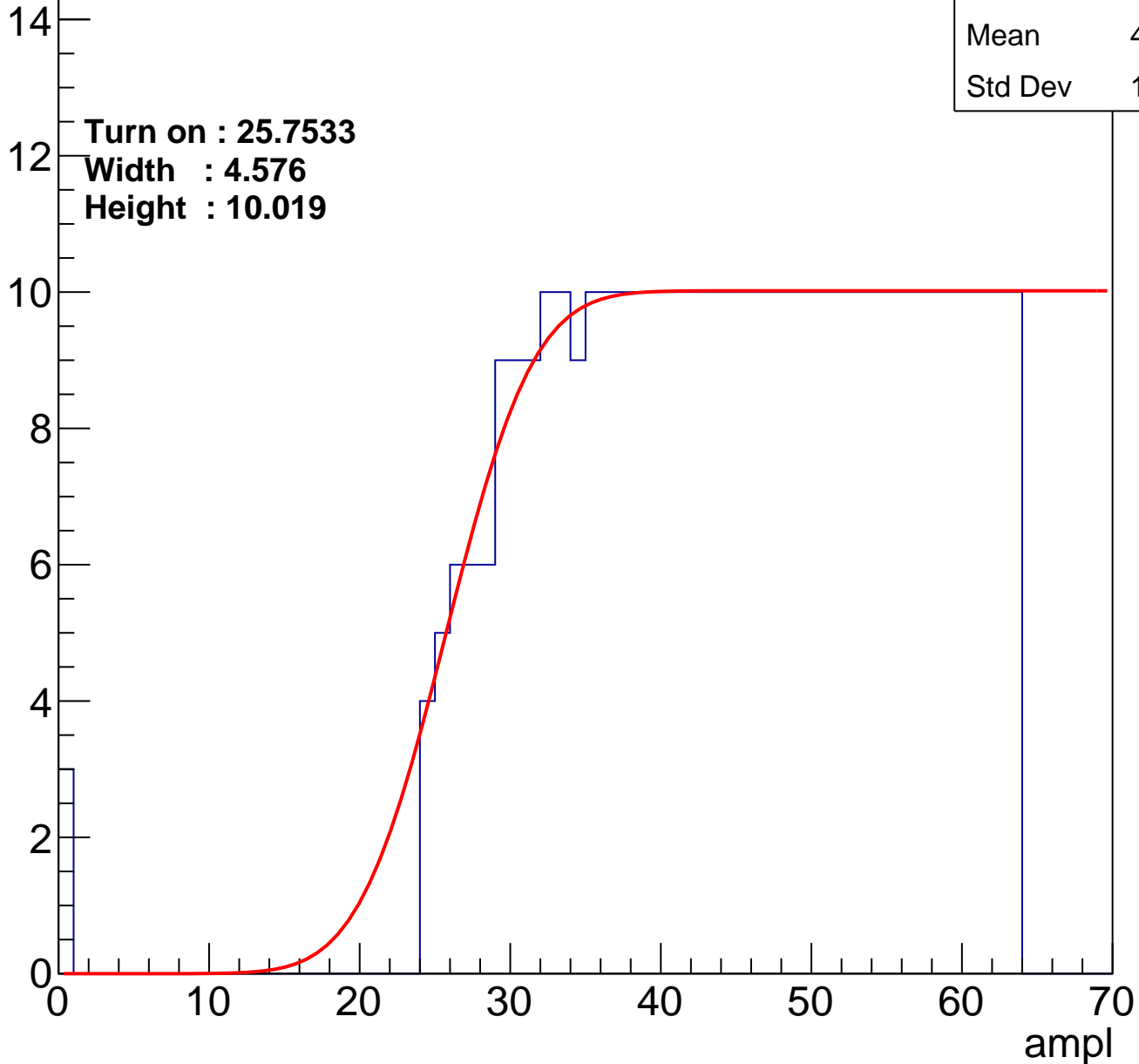
Entries	376
Mean	44.37
Std Dev	11.62

Turn on : 25.7533

Width : 4.576

Height : 10.019

Entry



# B1L101S, U26-ch100

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	374
Mean	44.47
Std Dev	11.57

**Turn on : 27.0075**

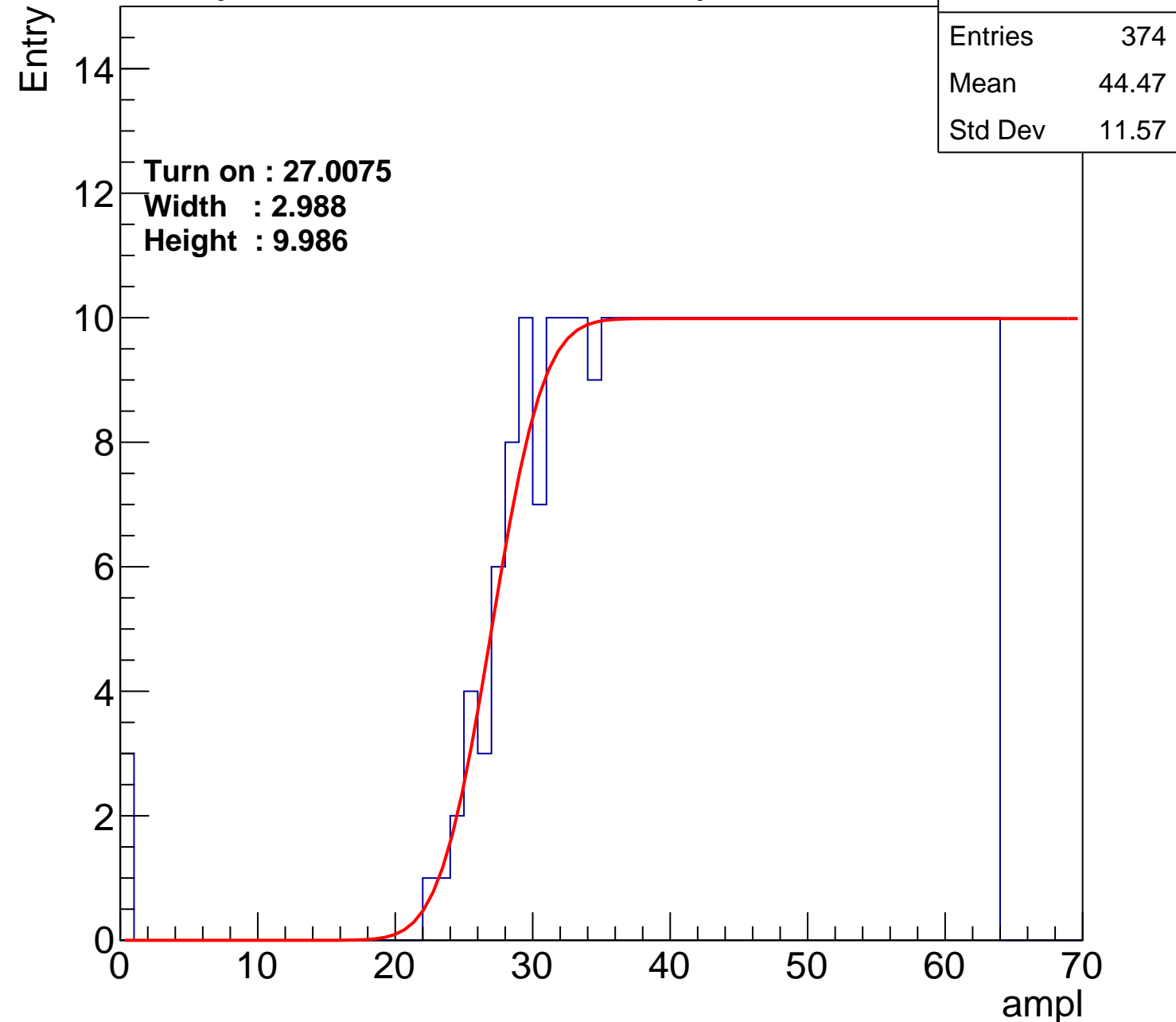
**Width : 2.988**

**Height : 9.986**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch101

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	355
Mean	45.49
Std Dev	10.9

**Turn on : 29.2261**

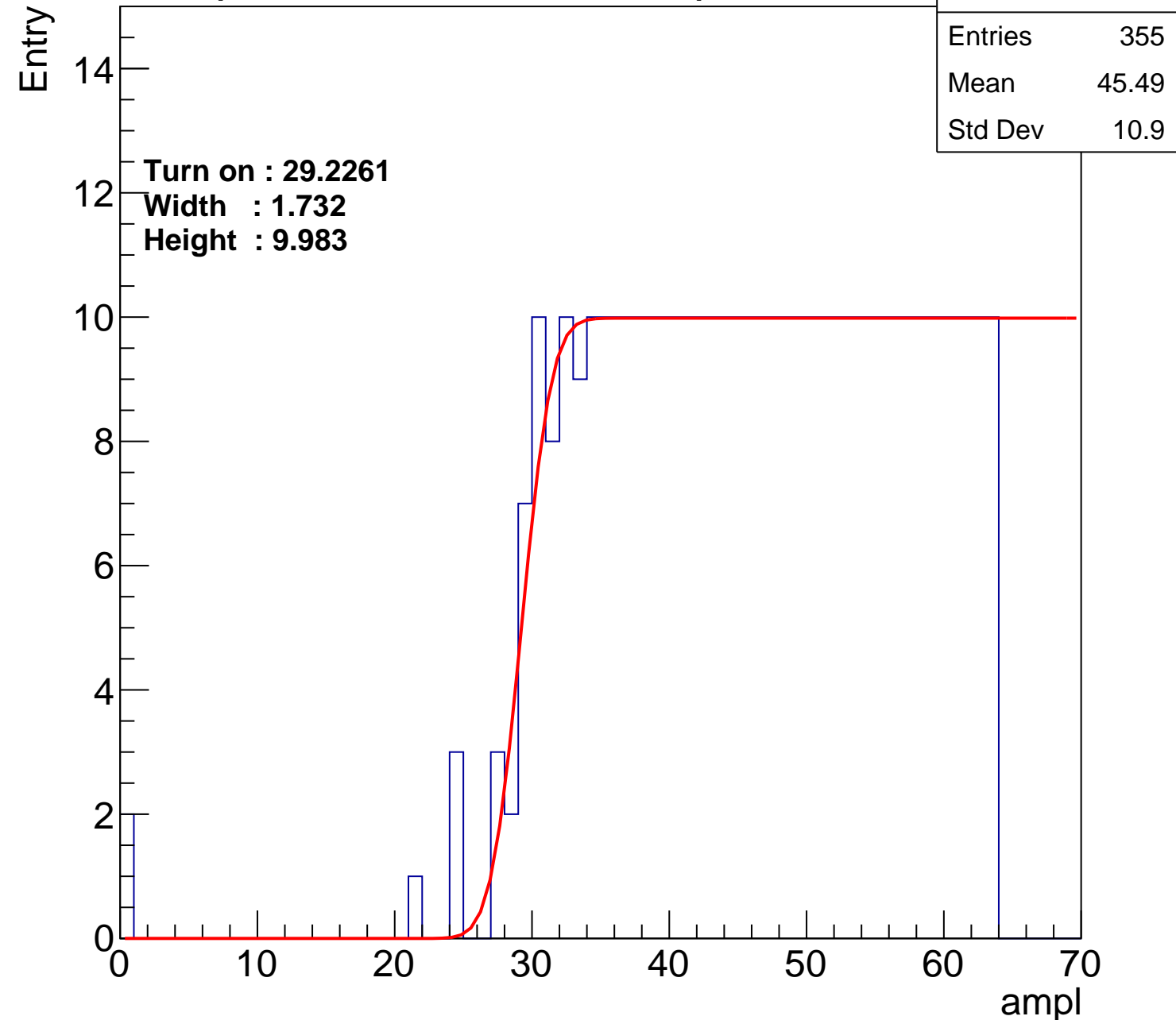
**Width : 1.732**

**Height : 9.983**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch102

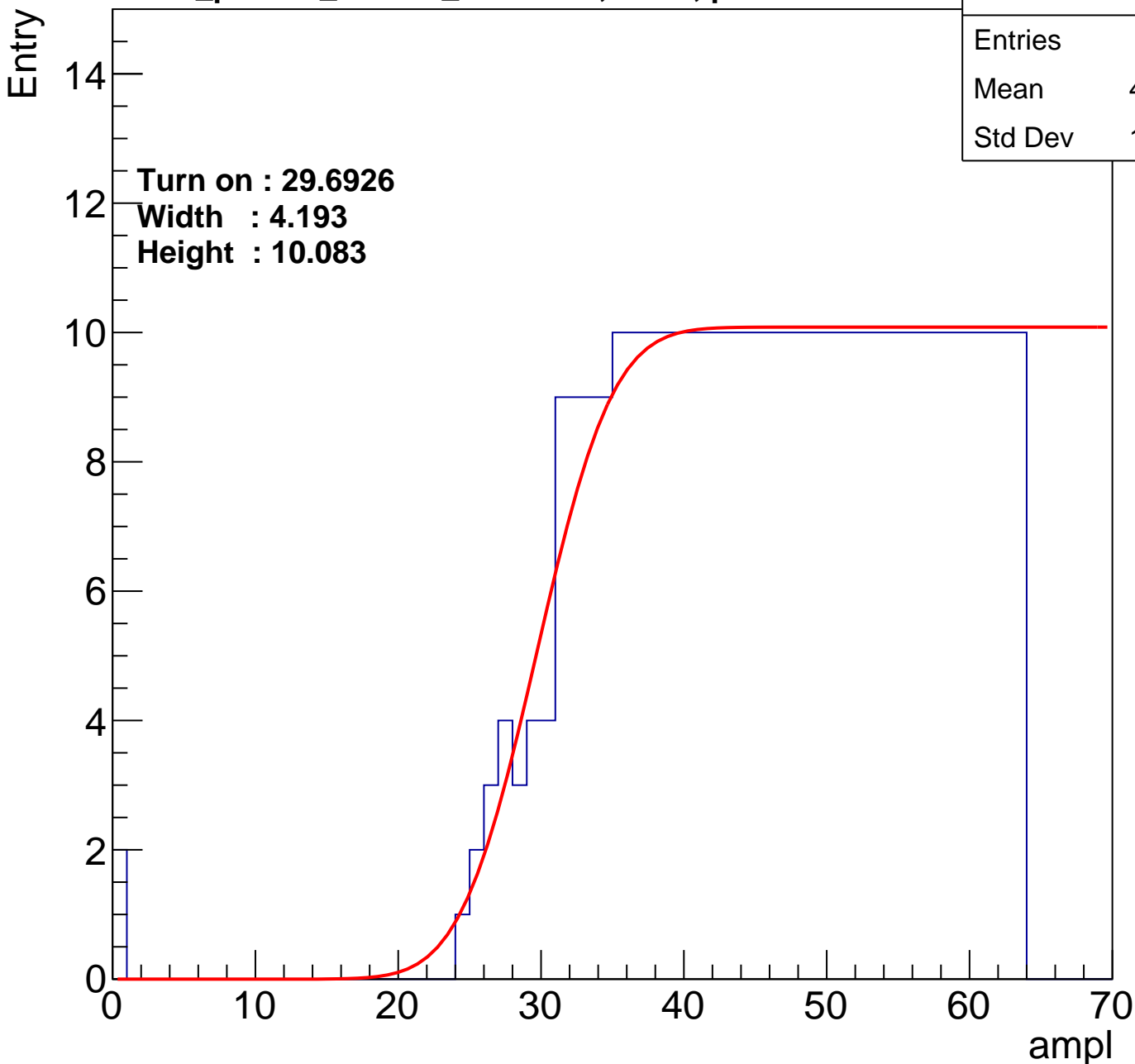
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	349
Mean	45.73
Std Dev	10.82

Turn on : 29.6926

Width : 4.193

Height : 10.083





# B1L101S, U26-ch103

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	373
Mean	44.38
Std Dev	11.87

Turn on : 27.8720

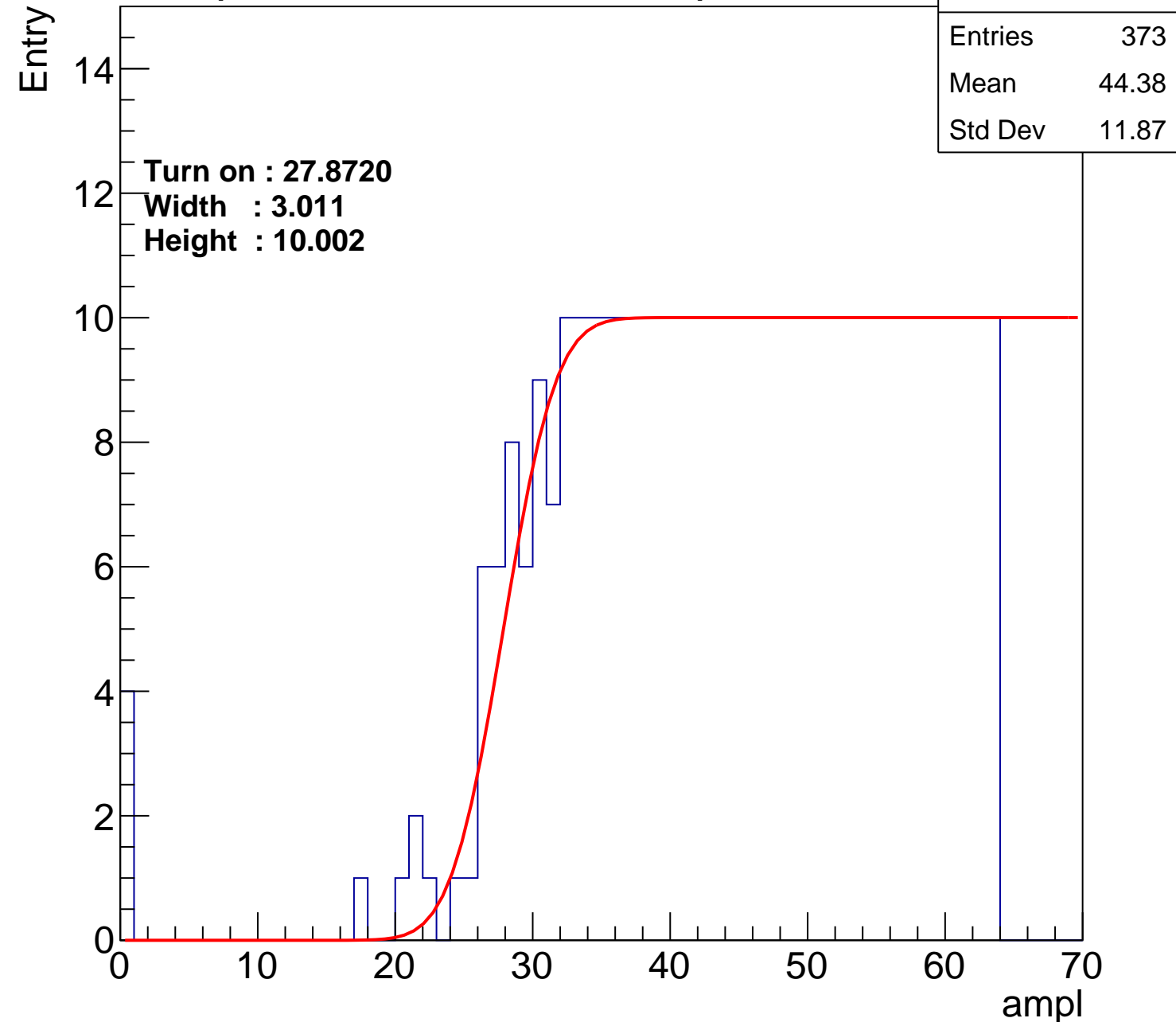
Width : 3.011

Height : 10.002

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch104

calib\_packv5\_042523\_0143.root, FC#0, port D2

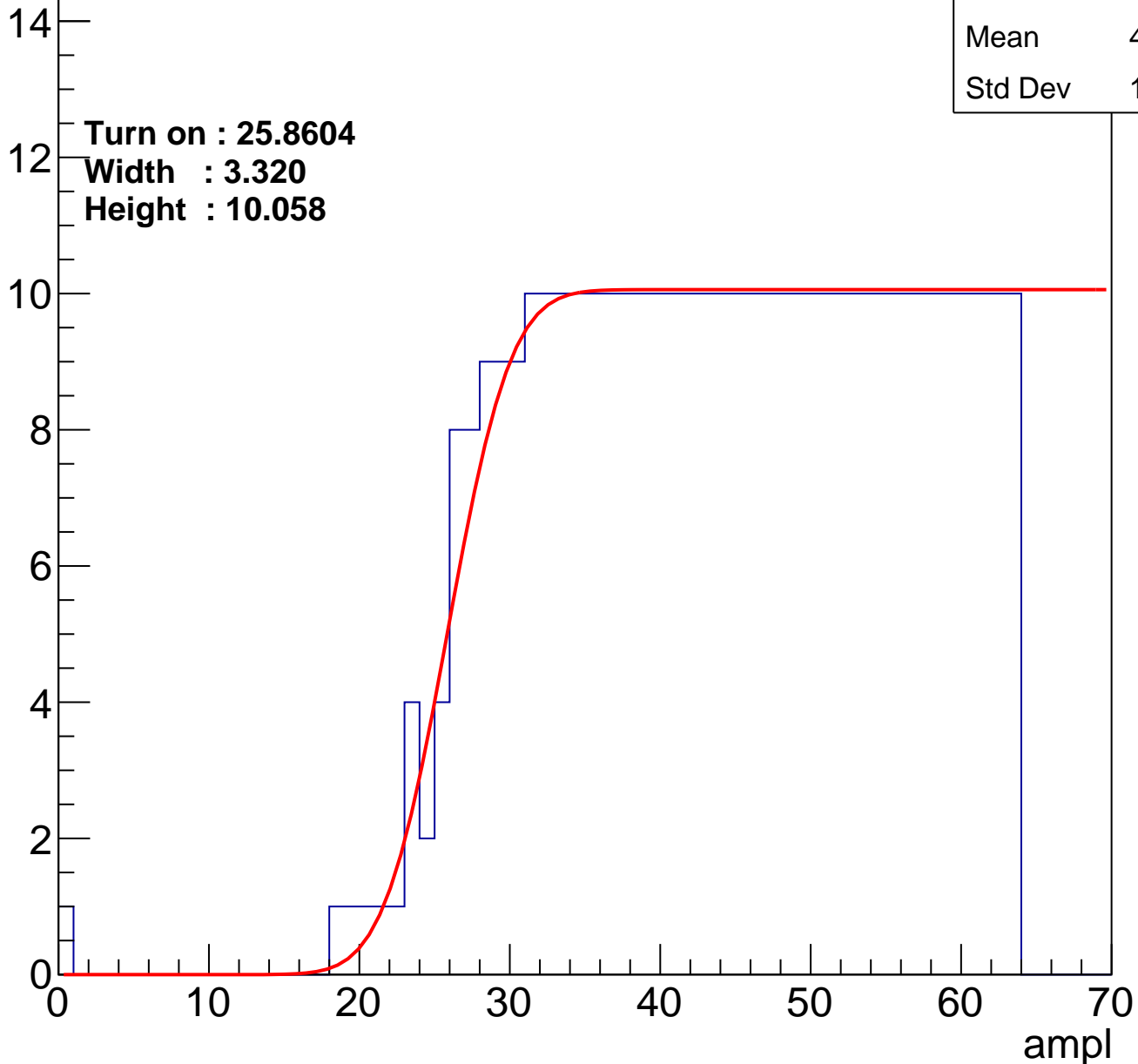
Entries	389
Mean	43.85
Std Dev	11.64

Turn on : 25.8604

Width : 3.320

Height : 10.058

Entry



# B1L101S, U26-ch105

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	360
Mean	45.24
Std Dev	11.02

**Turn on : 28.5632**

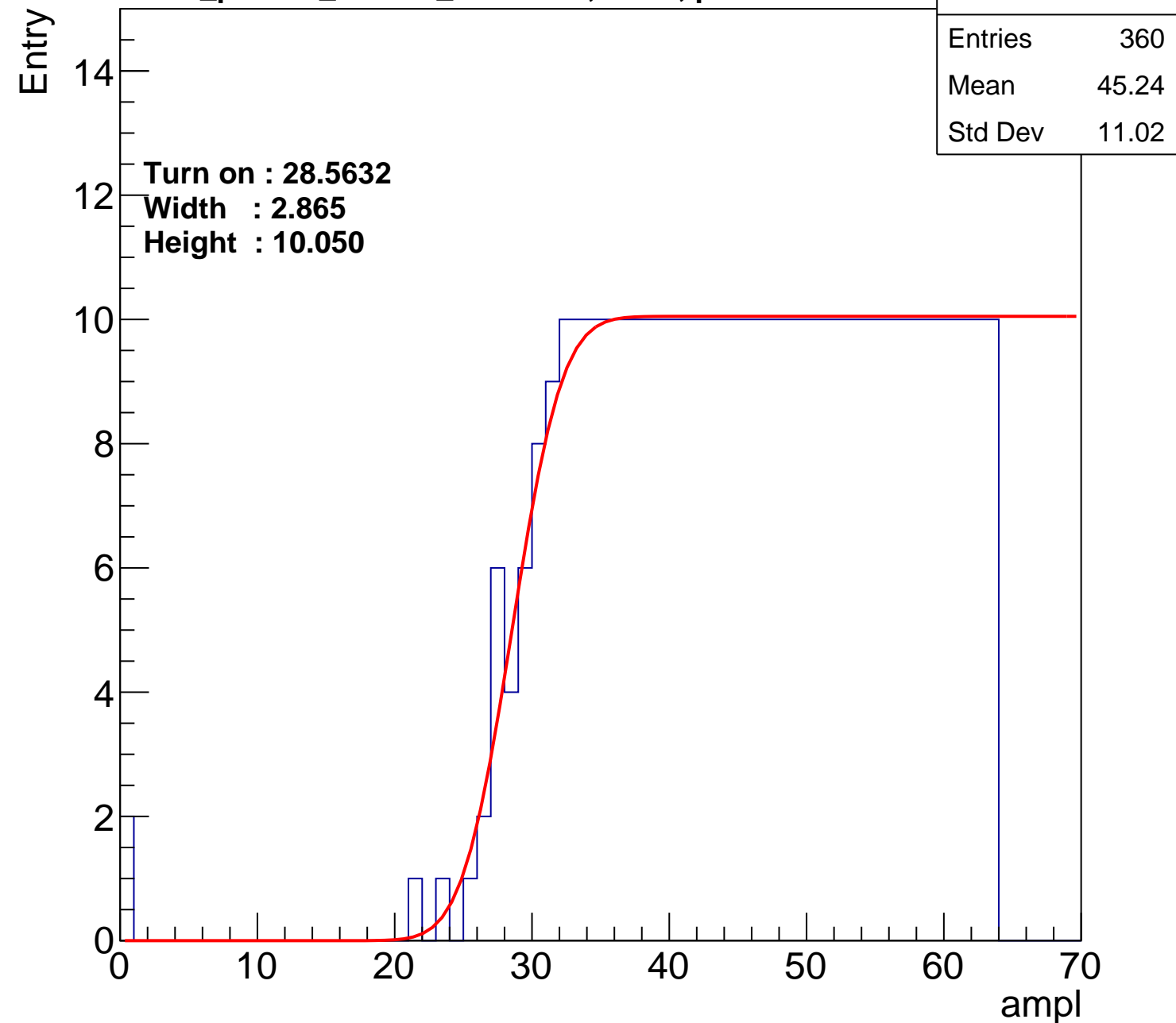
**Width : 2.865**

**Height : 10.050**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch106

calib\_packv5\_042523\_0143.root, FC#0, port D2

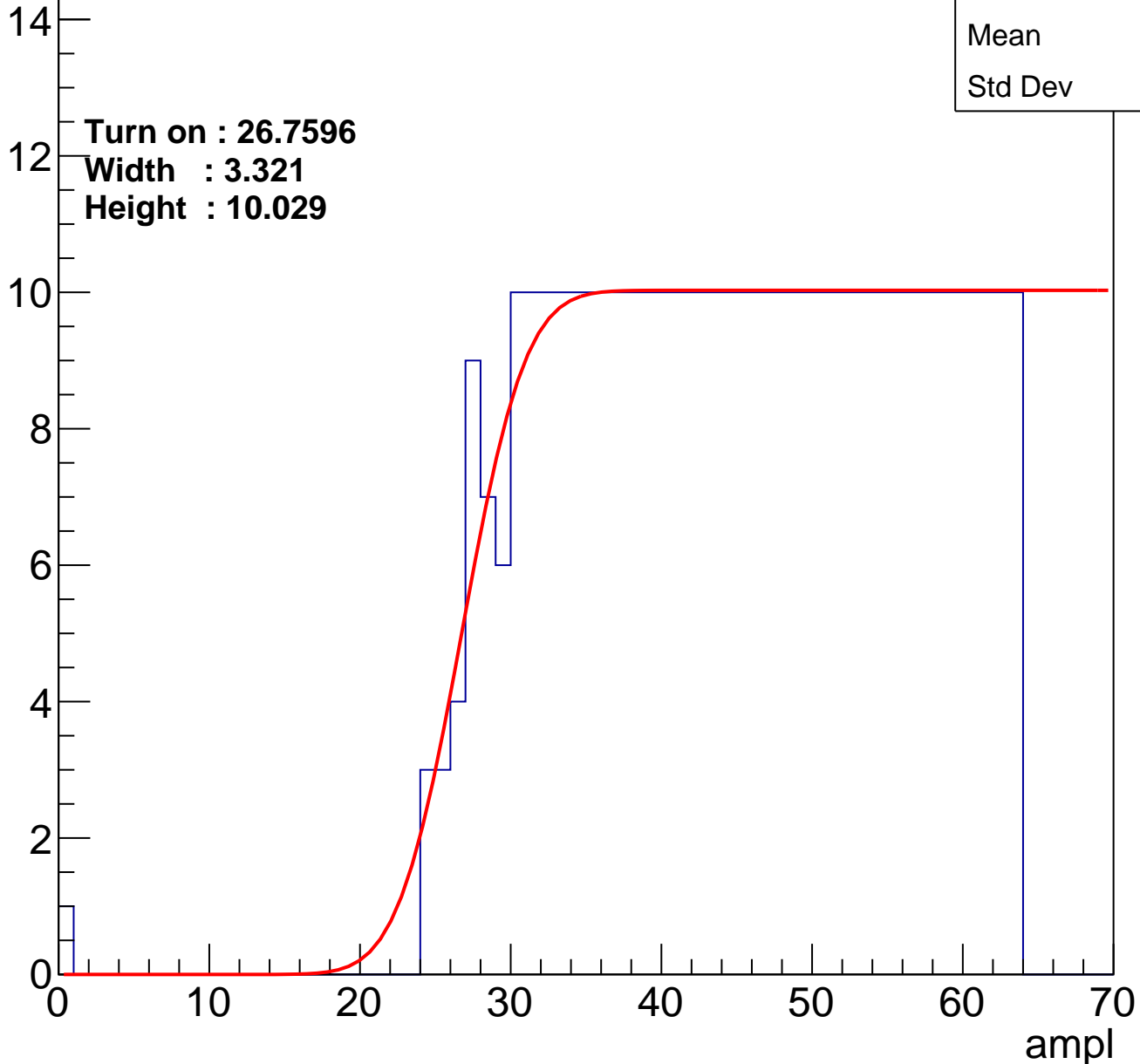
Entries	373
Mean	44.7
Std Dev	11.1

Turn on : 26.7596

Width : 3.321

Height : 10.029

Entry



# B1L101S, U26-ch107

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	361
Mean	45.04
Std Dev	11.47

**Turn on : 28.5573**

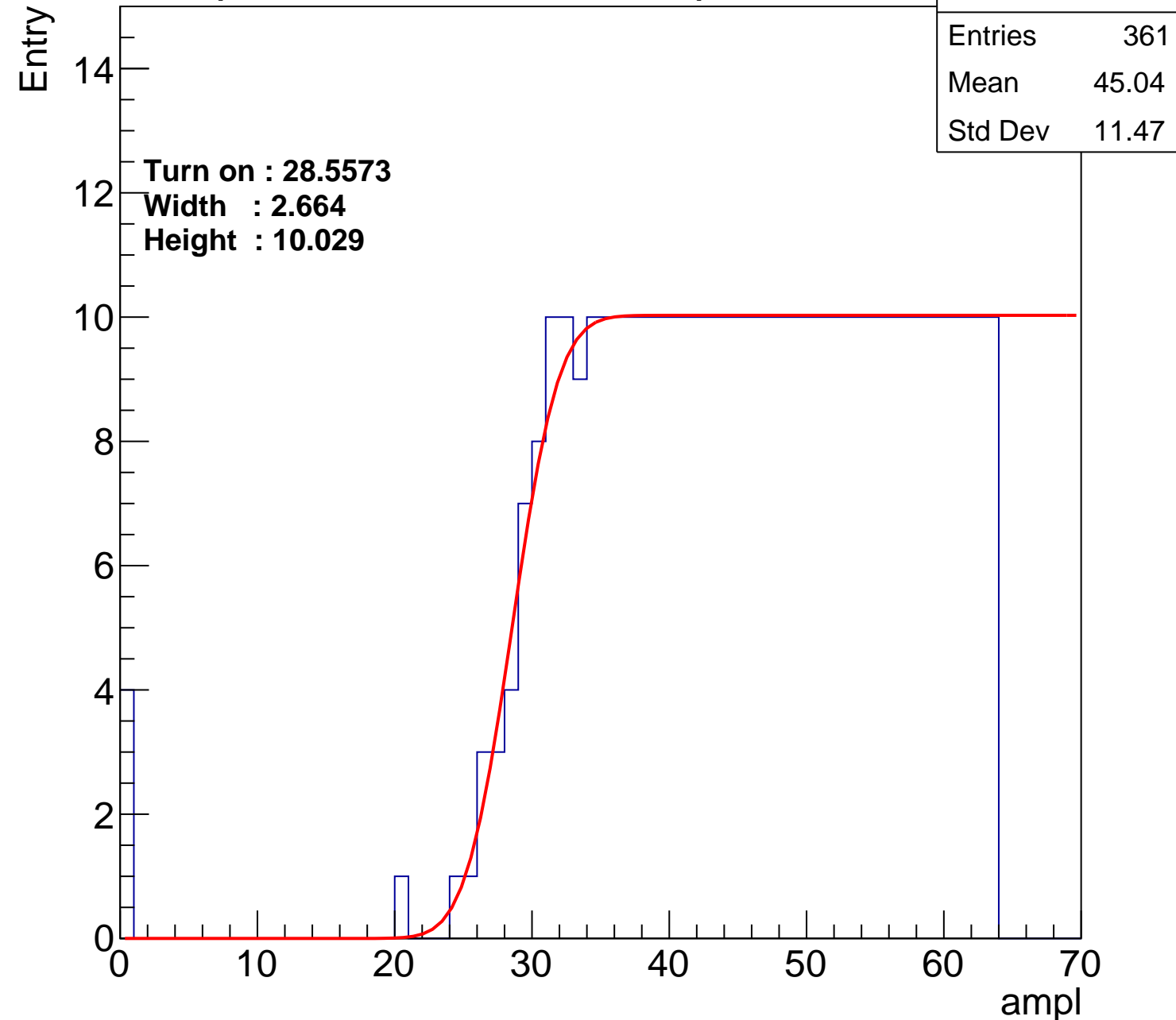
**Width : 2.664**

**Height : 10.029**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch108

calib\_packv5\_042523\_0143.root, FC#0, port D2

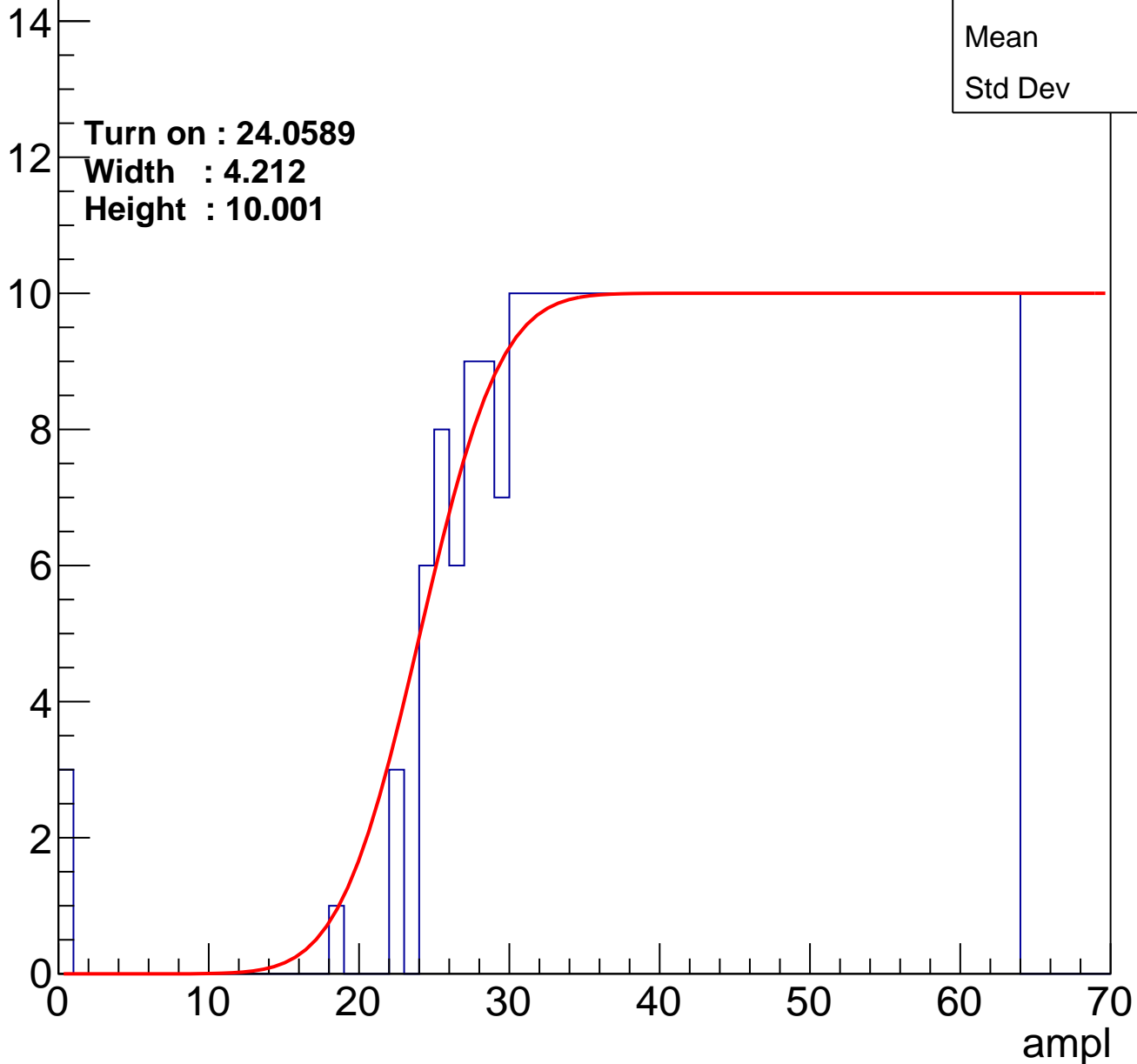
Entries	392
Mean	43.6
Std Dev	12

Turn on : 24.0589

Width : 4.212

Height : 10.001

Entry



# B1L101S, U26-ch109

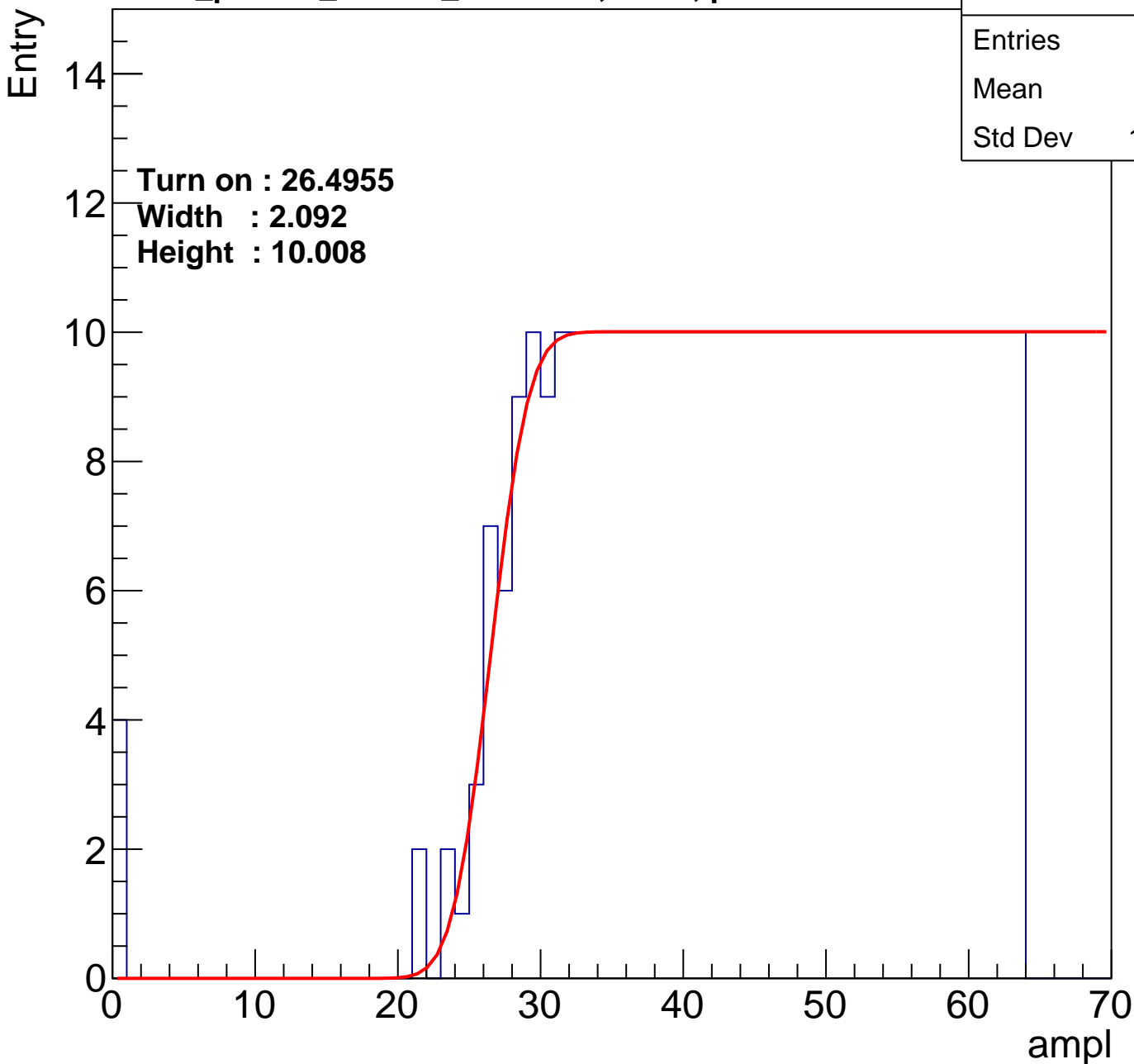
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	383
Mean	44
Std Dev	11.92

Turn on : 26.4955

Width : 2.092

Height : 10.008



# B1L101S, U26-ch110

calib\_packv5\_042523\_0143.root, FC#0, port D2

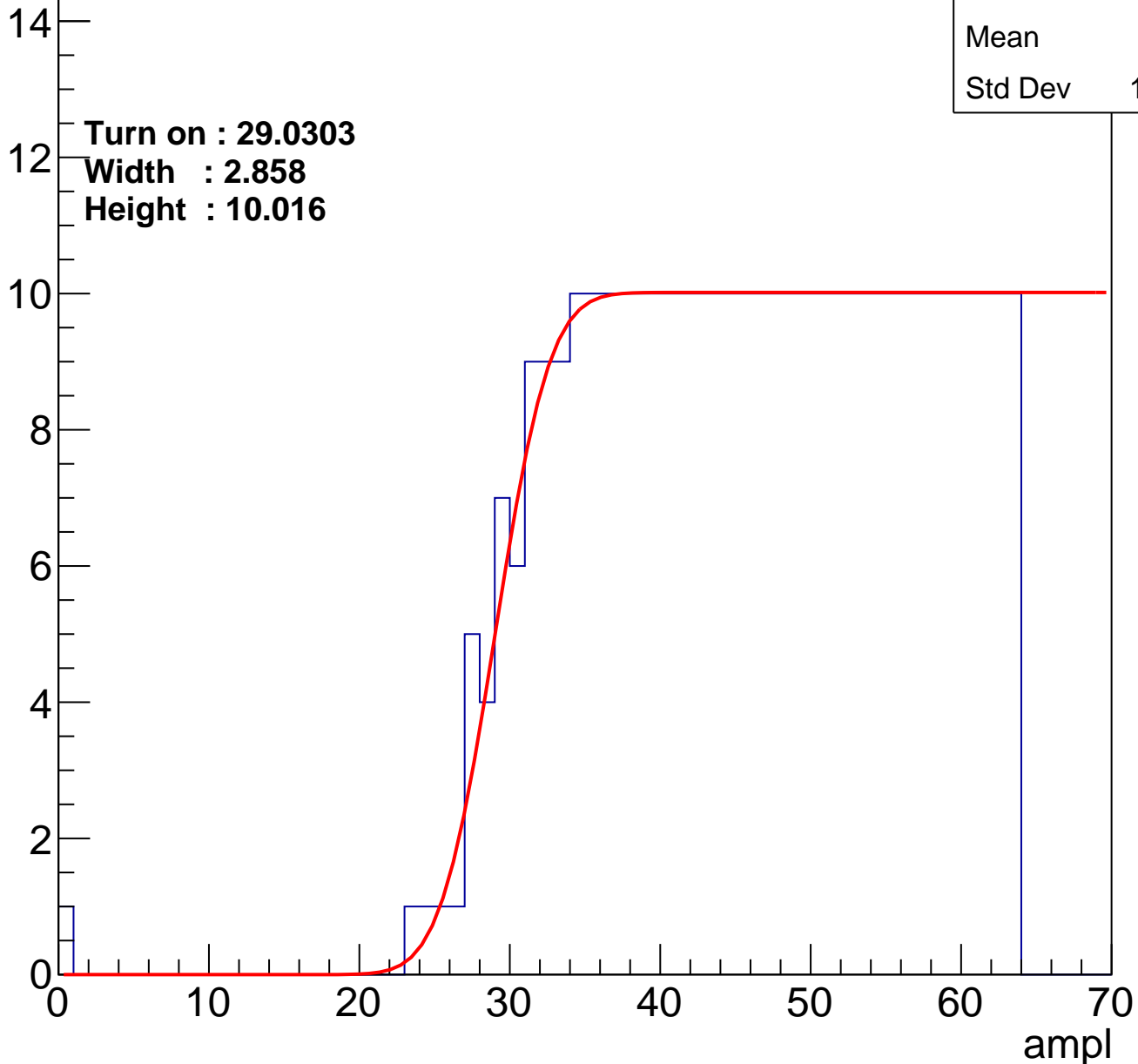
Entries	354
Mean	45.6
Std Dev	10.66

Turn on : 29.0303

Width : 2.858

Height : 10.016

Entry





# B1L101S, U26-ch111

calib\_packv5\_042523\_0143.root, FC#0, port D2

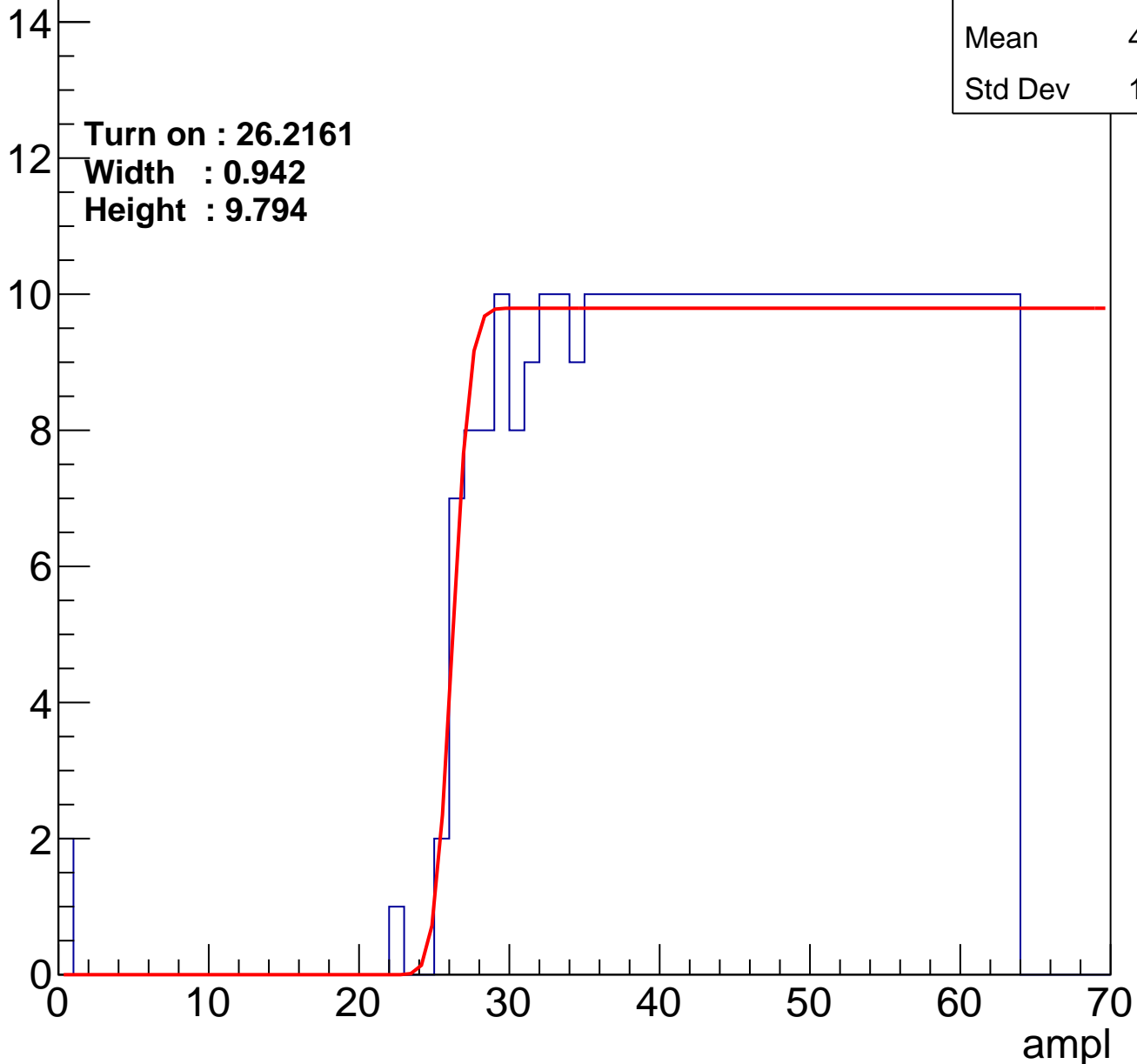
Entry

Entries	374
Mean	44.57
Std Dev	11.33

Turn on : 26.2161

Width : 0.942

Height : 9.794



# B1L101S, U26-ch112

calib\_packv5\_042523\_0143.root, FC#0, port D2

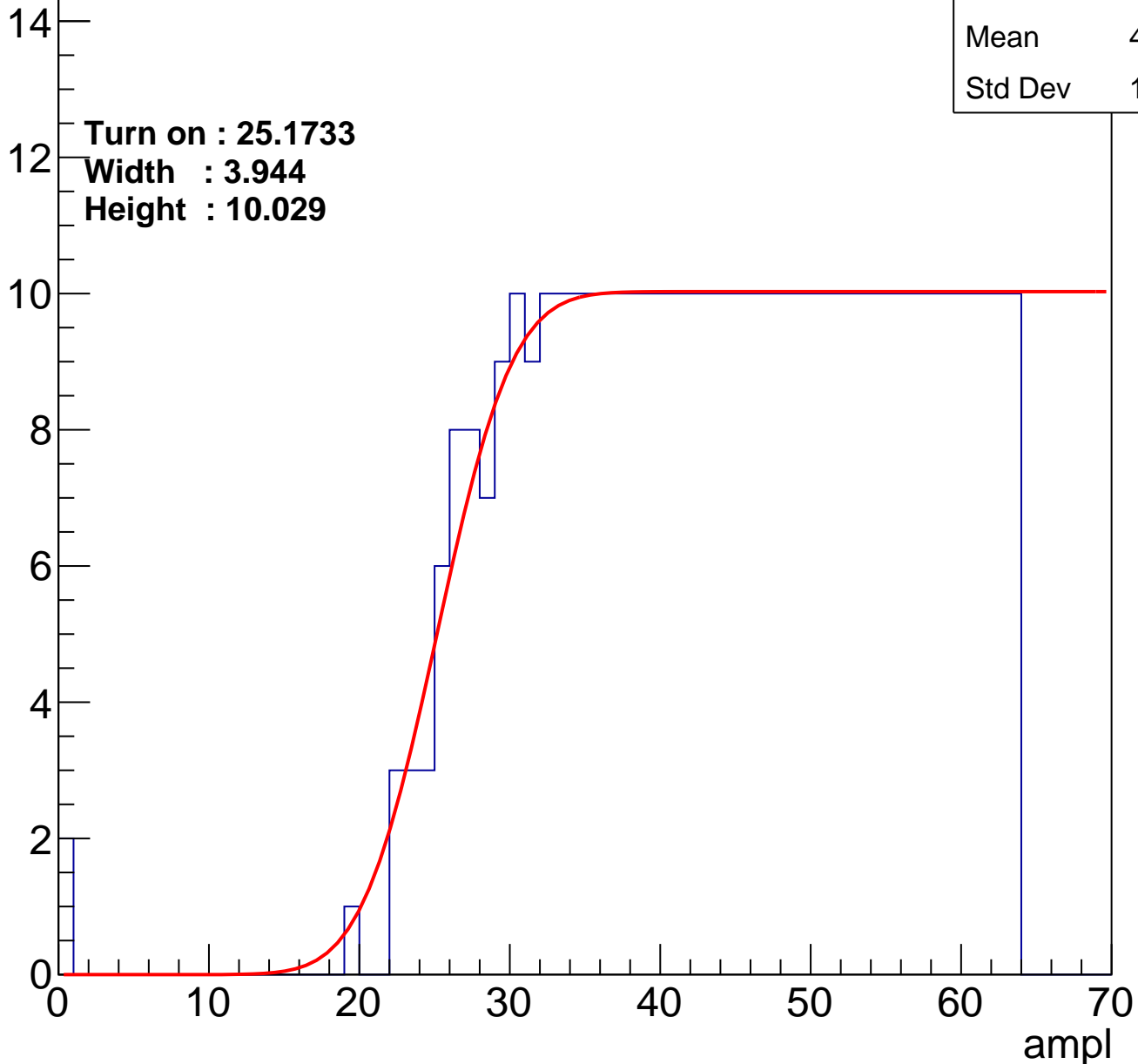
Entries	389
Mean	43.79
Std Dev	11.78

Turn on : 25.1733

Width : 3.944

Height : 10.029

Entry



# B1L101S, U26-ch113

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	372
Mean	44.56
Std Dev	11.55

Turn on : 27.5548

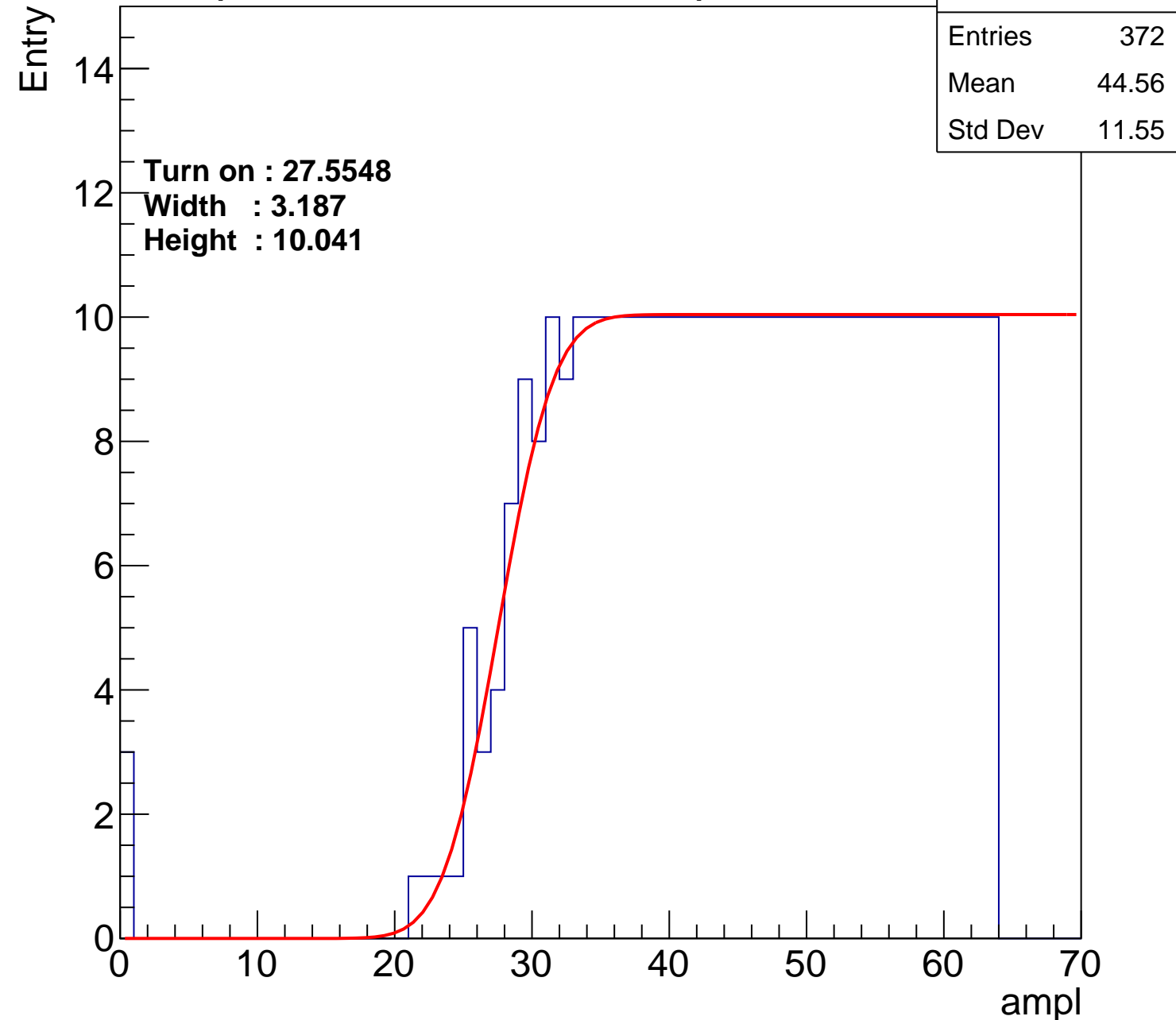
Width : 3.187

Height : 10.041

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch114

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	366
Mean	44.88
Std Dev	11.28

Turn on : 28.3416

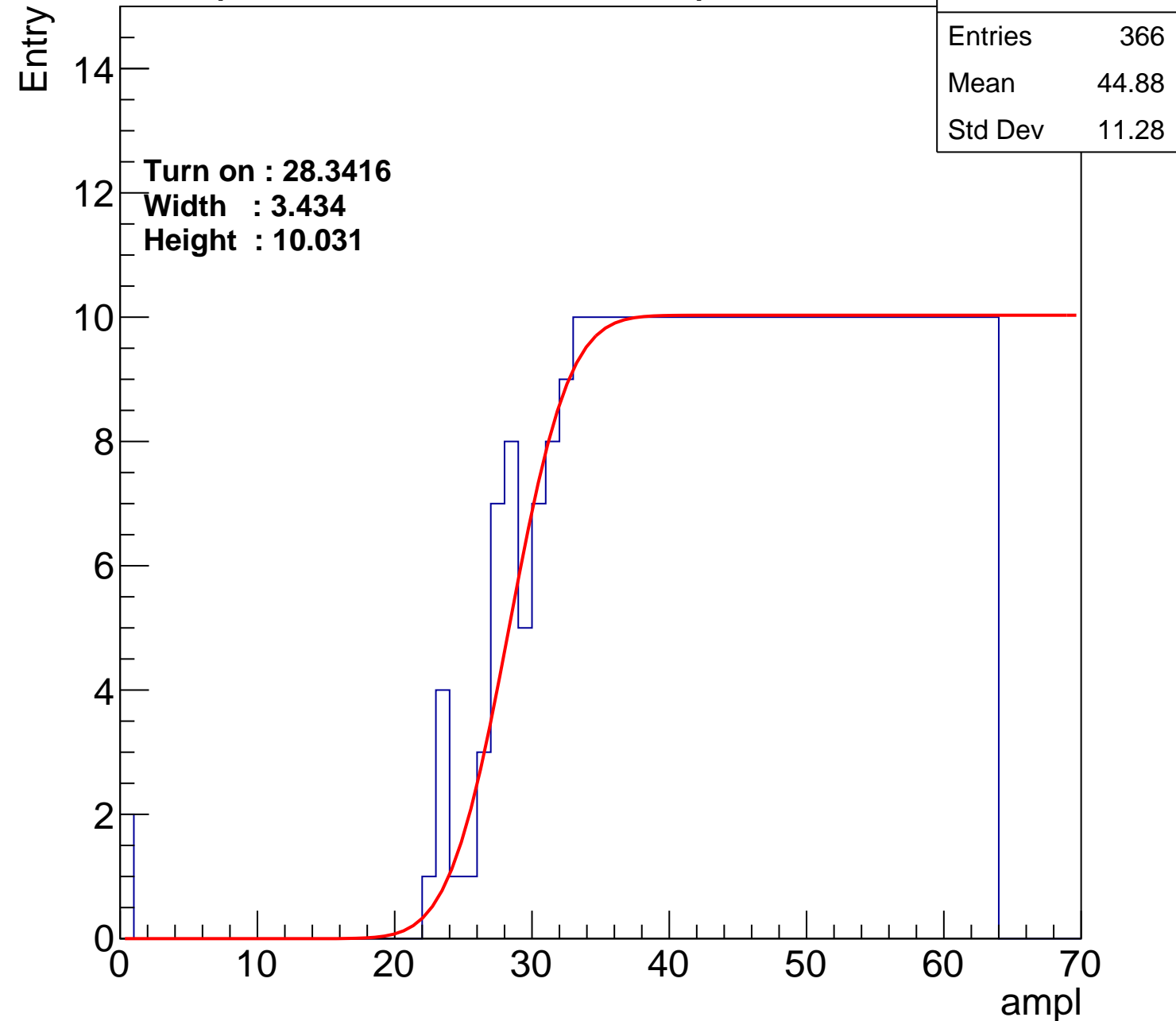
Width : 3.434

Height : 10.031

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch115

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	363
Mean	45
Std Dev	11.42

Turn on : 28.0220

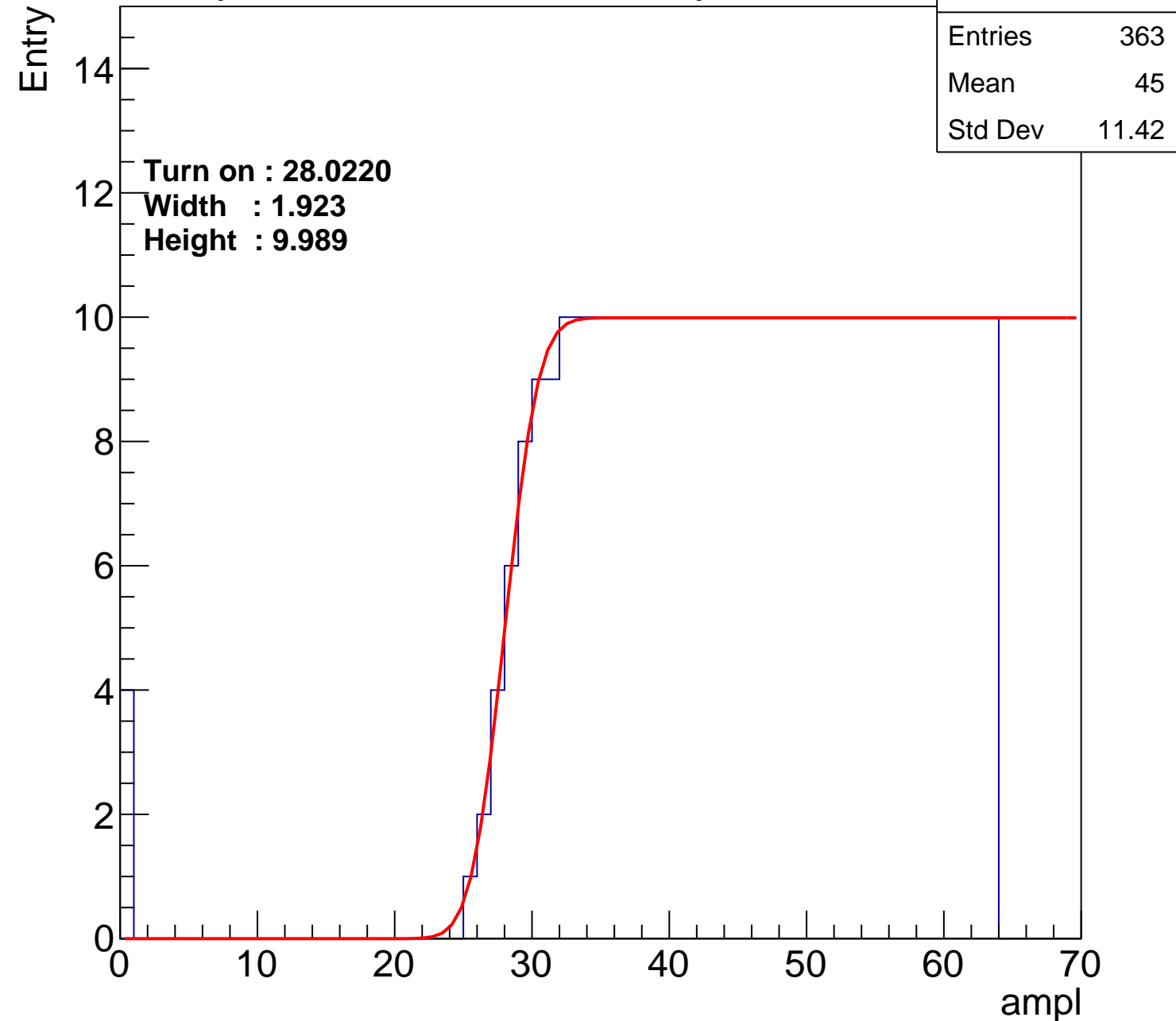
Width : 1.923

Height : 9.989

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch116

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	362
Mean	45.11
Std Dev	11.21

**Turn on : 27.9673**

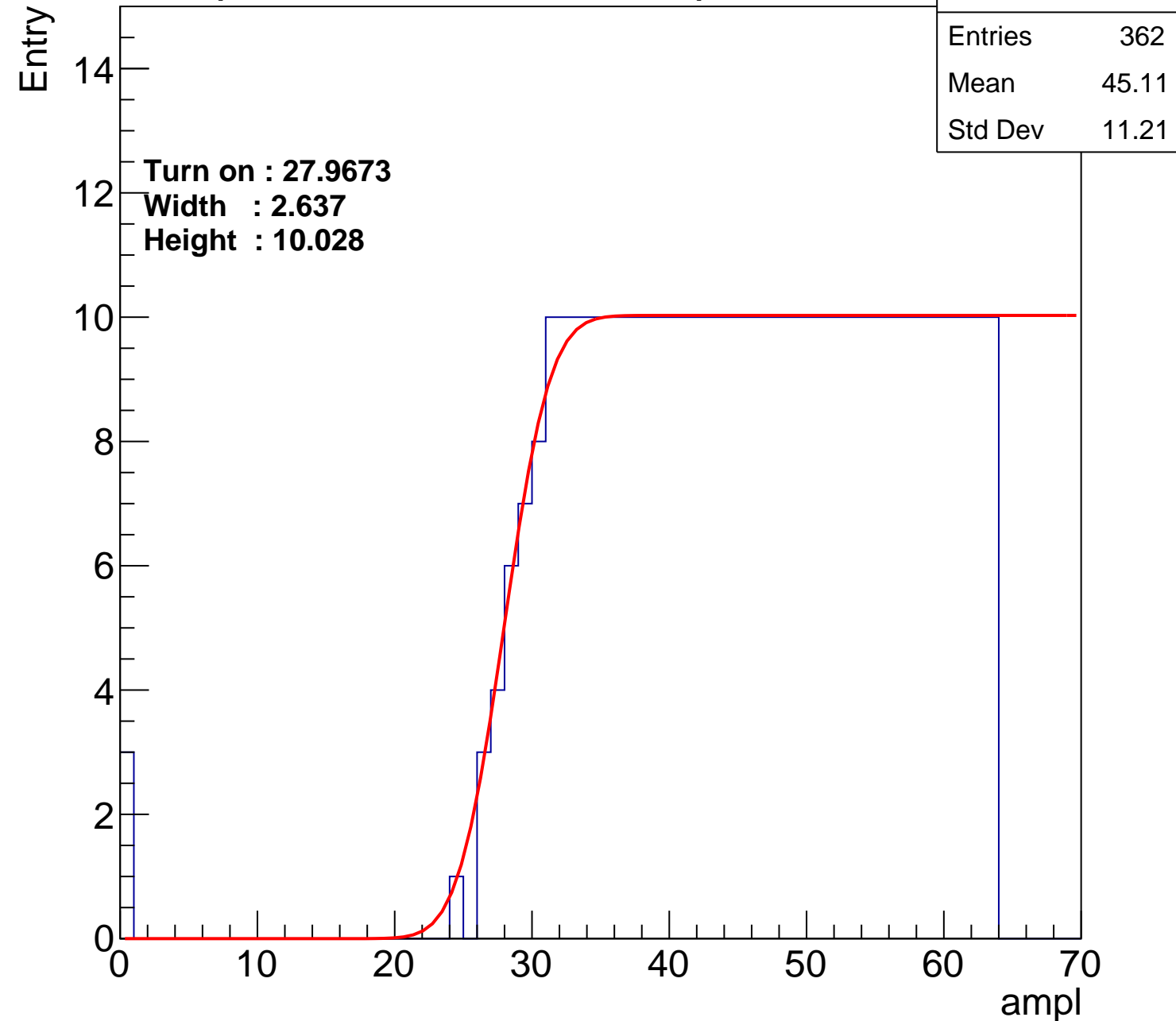
**Width : 2.637**

**Height : 10.028**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch117

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	381
Mean	44.11
Std Dev	11.76

Turn on : 26.5348

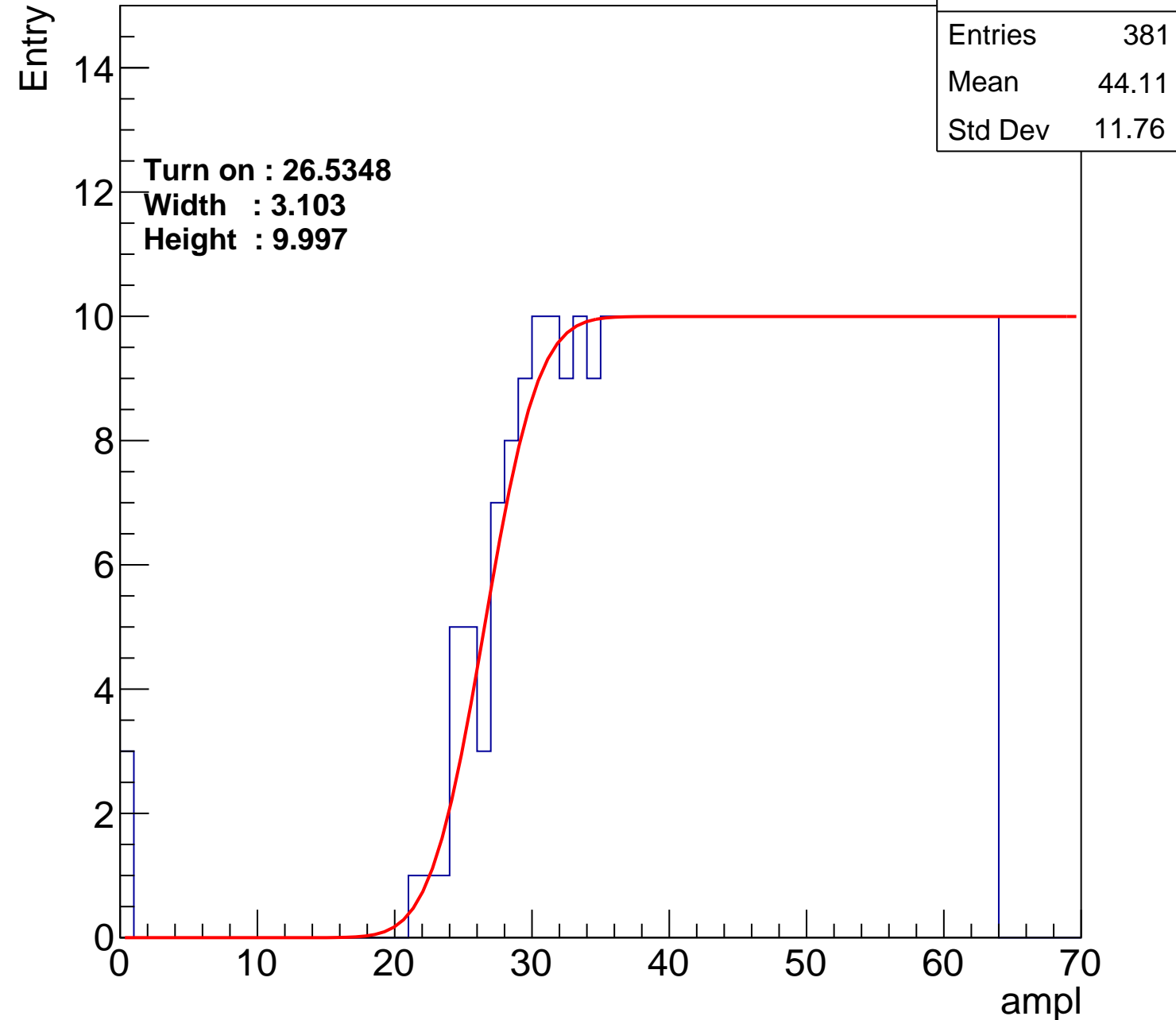
Width : 3.103

Height : 9.997

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch118

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	354
Mean	45.53
Std Dev	10.88

**Turn on : 29.7447**

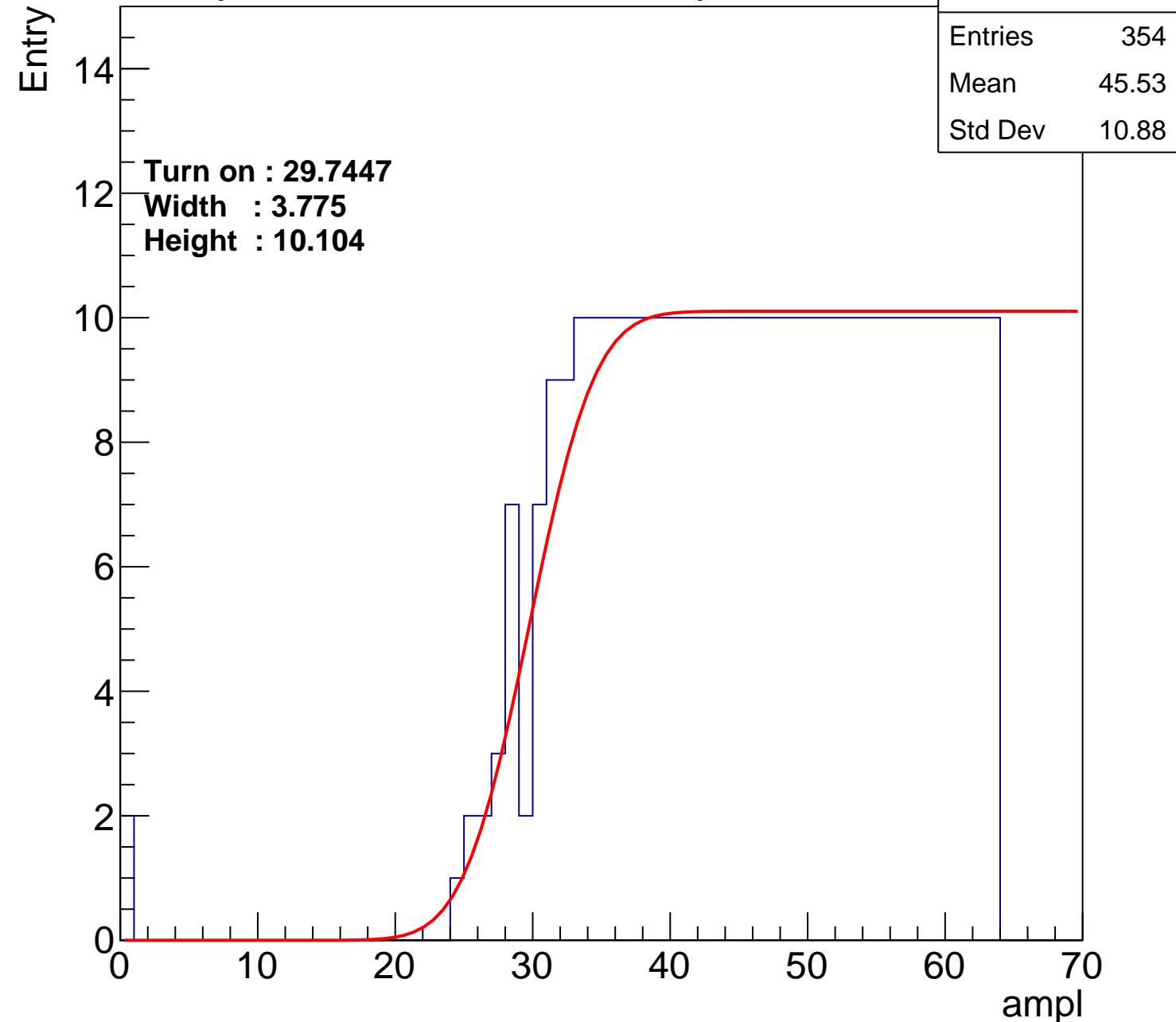
**Width : 3.775**

**Height : 10.104**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U26-ch119

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	366
Mean	44.92
Std Dev	11.22

Turn on : 28.3072

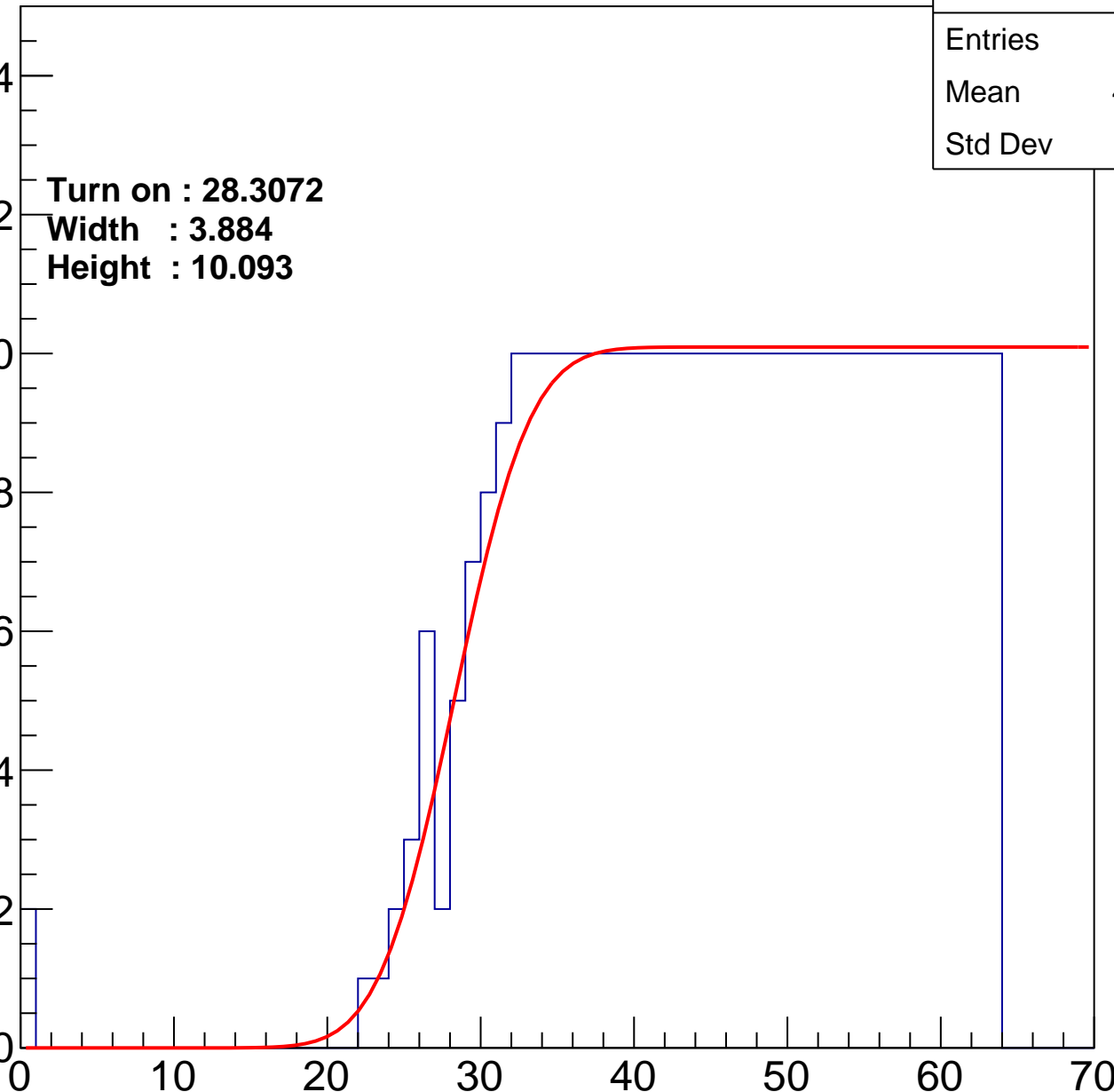
Width : 3.884

Height : 10.093

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch120

calib\_packv5\_042523\_0143.root, FC#0, port D2

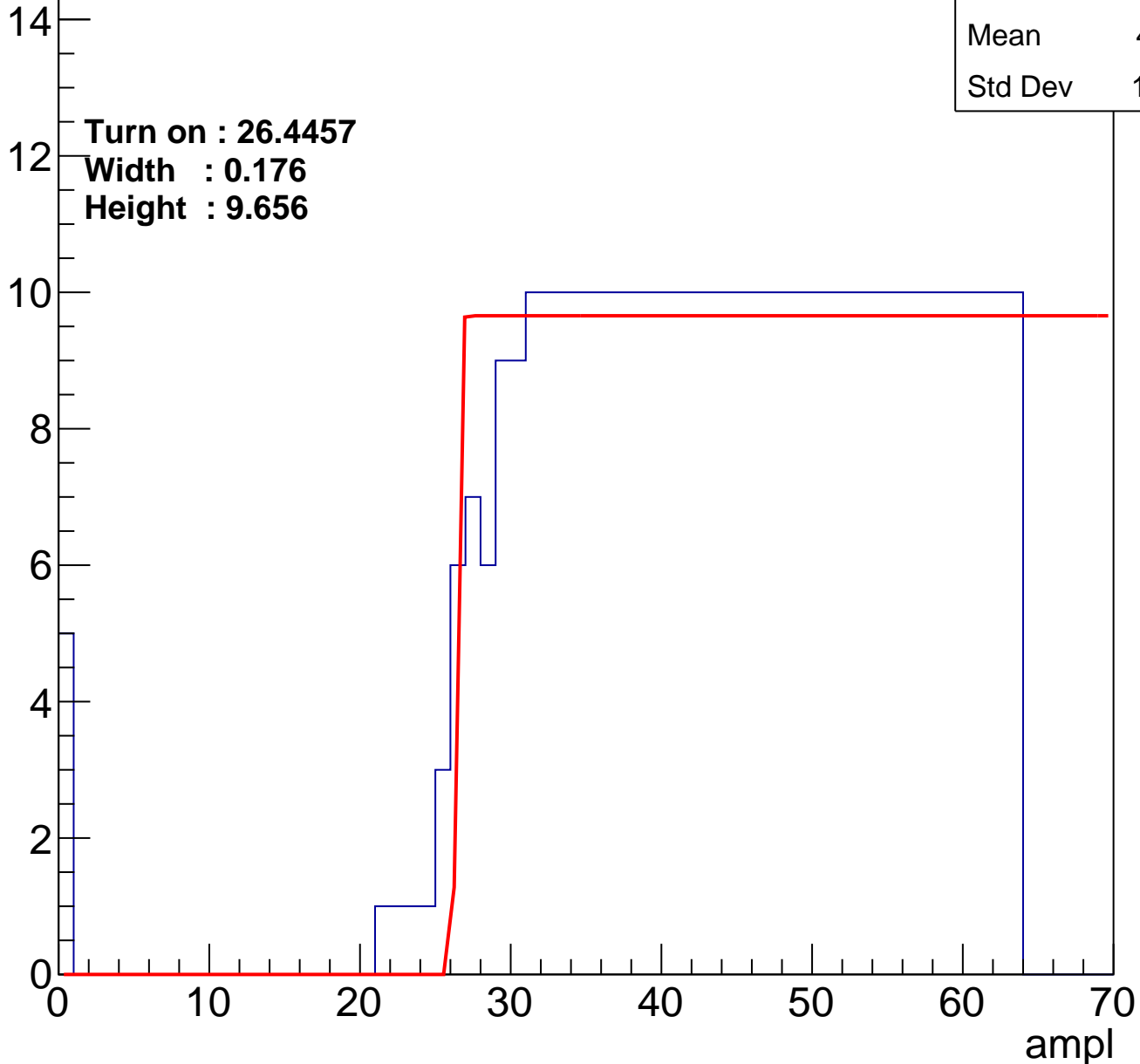
Entries	379
Mean	44.11
Std Dev	12.02

Turn on : 26.4457

Width : 0.176

Height : 9.656

Entry



# B1L101S, U26-ch121

calib\_packv5\_042523\_0143.root, FC#0, port D2

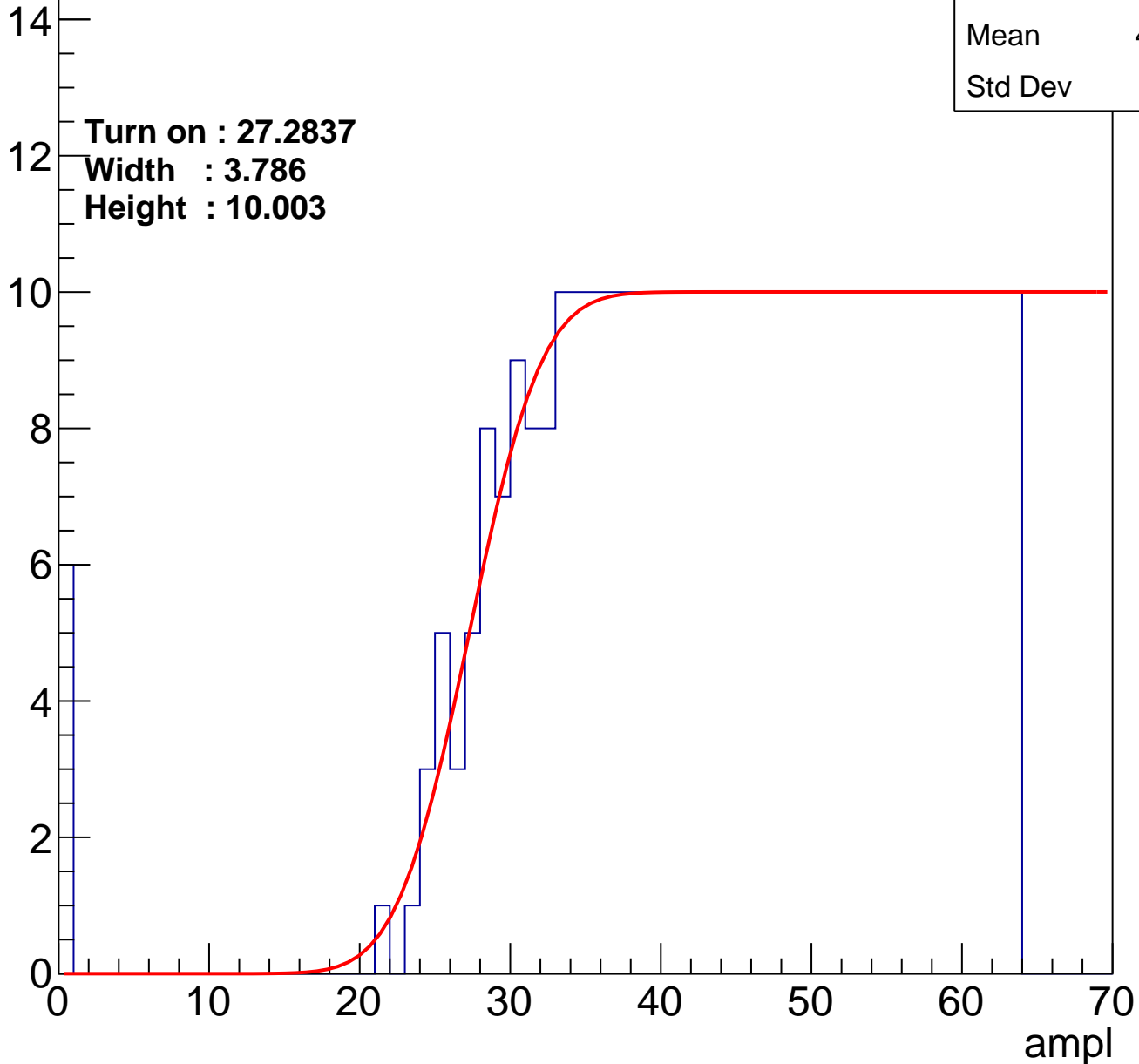
Entries	374
Mean	44.21
Std Dev	12.2

Turn on : 27.2837

Width : 3.786

Height : 10.003

Entry



# B1L101S, U26-ch122

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	374
Mean	44.49
Std Dev	11.47

Turn on : 27.0088

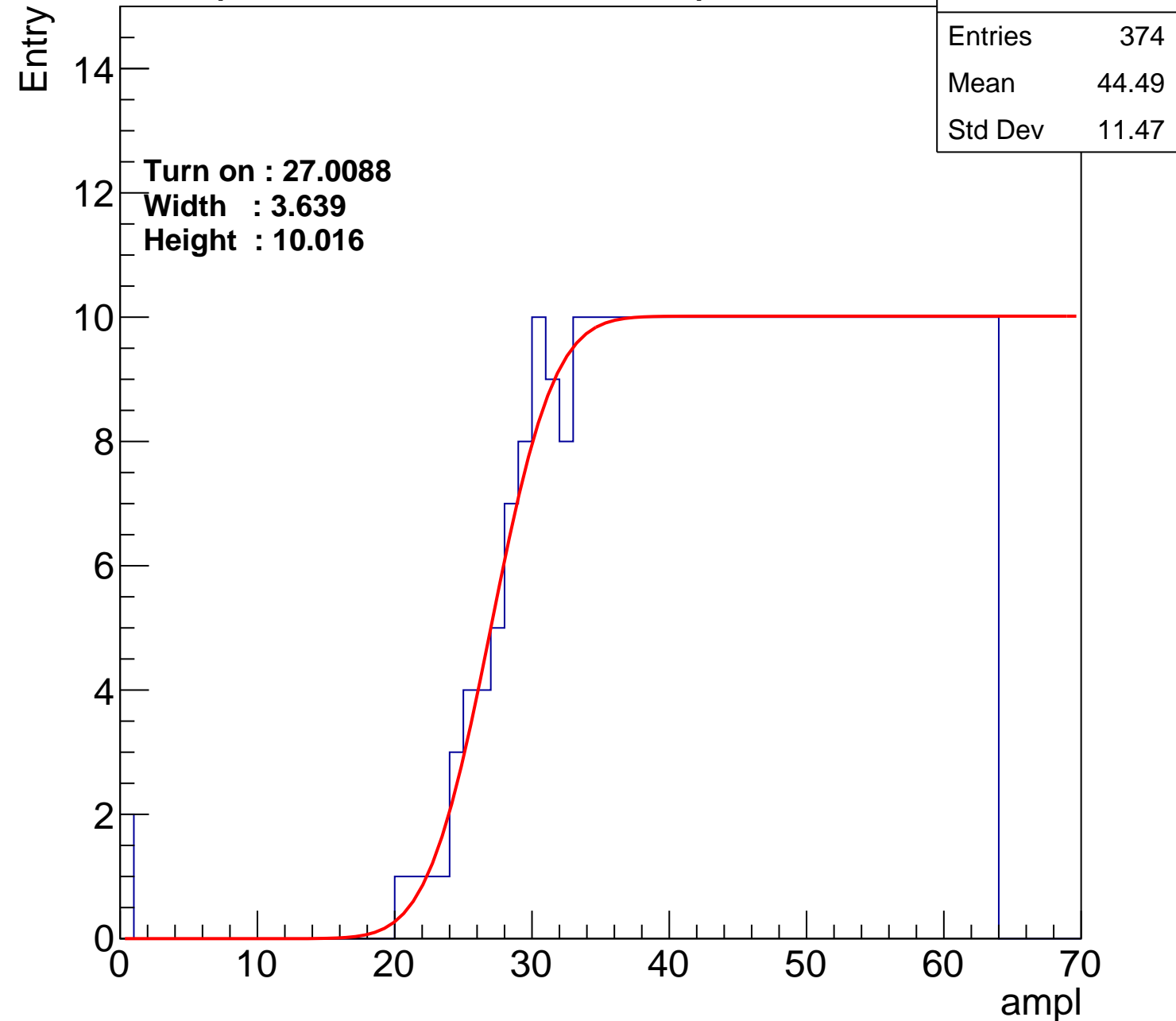
Width : 3.639

Height : 10.016

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch123

calib\_packv5\_042523\_0143.root, FC#0, port D2

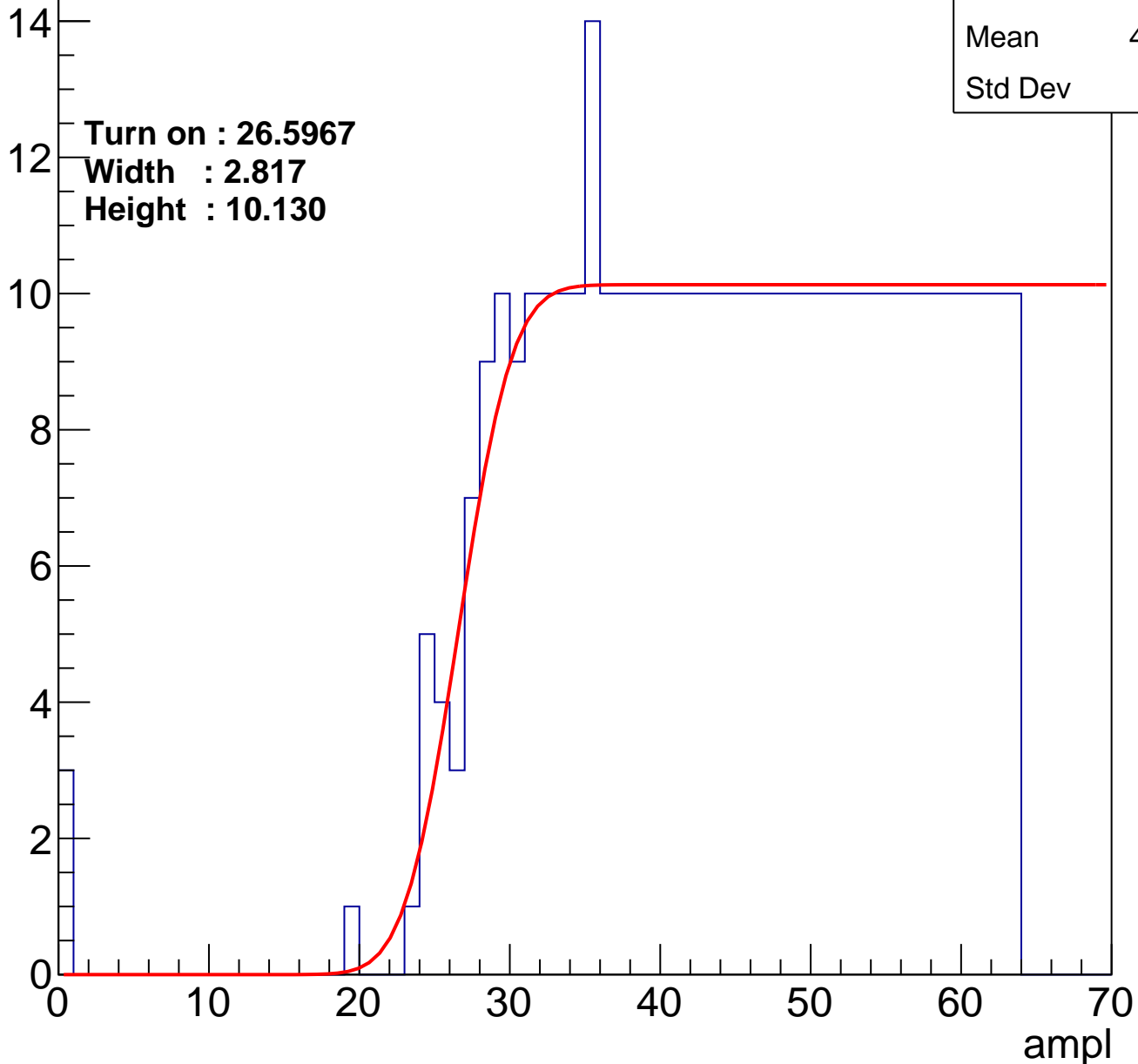
Entries	386
Mean	44.02
Std Dev	11.7

Turn on : 26.5967

Width : 2.817

Height : 10.130

Entry



# B1L101S, U26-ch124

calib\_packv5\_042523\_0143.root, FC#0, port D2

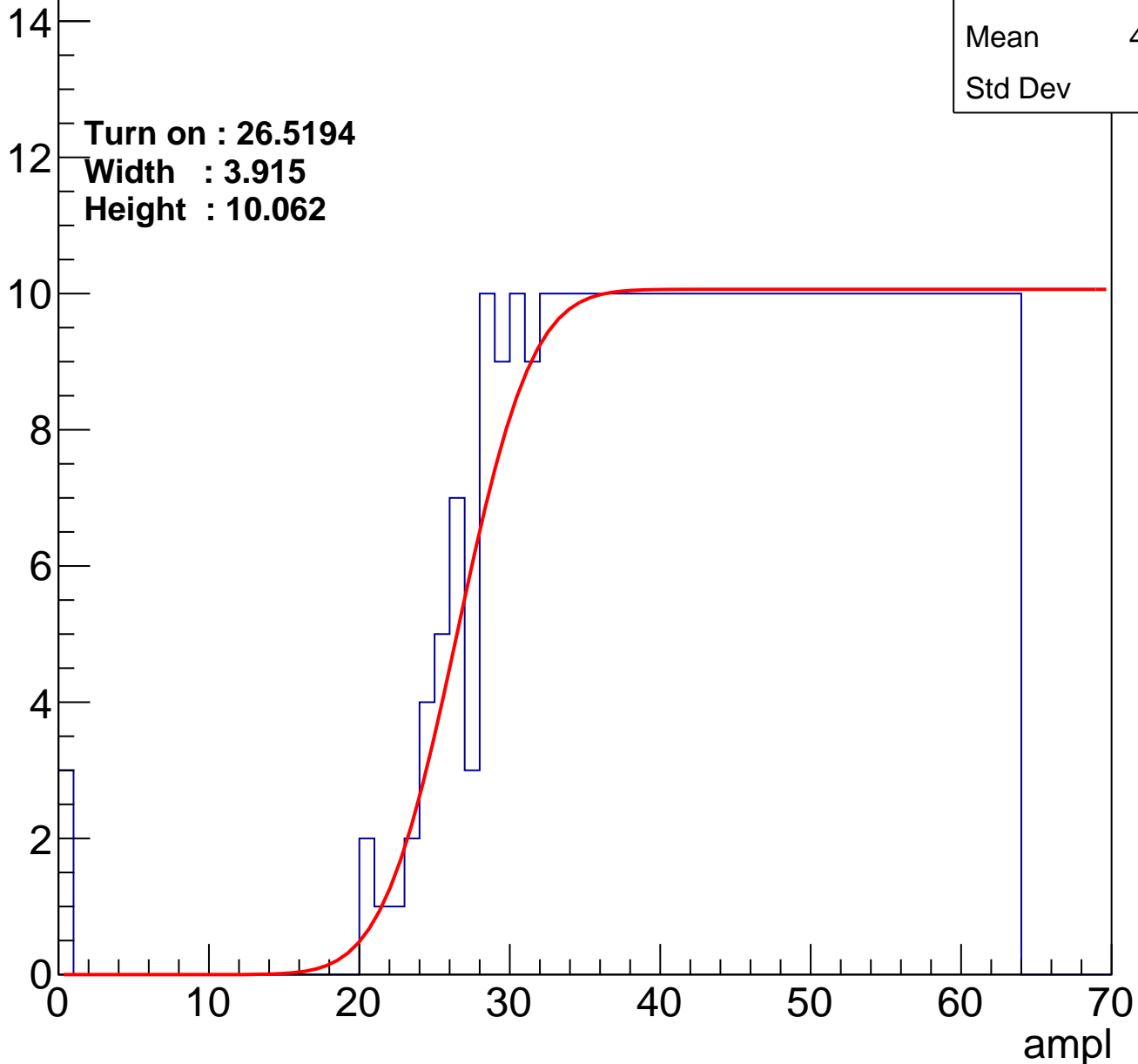
Entries	386
Mean	43.87
Std Dev	11.9

Turn on : 26.5194

Width : 3.915

Height : 10.062

Entry



# B1L101S, U26-ch125

calib\_packv5\_042523\_0143.root, FC#0, port D2

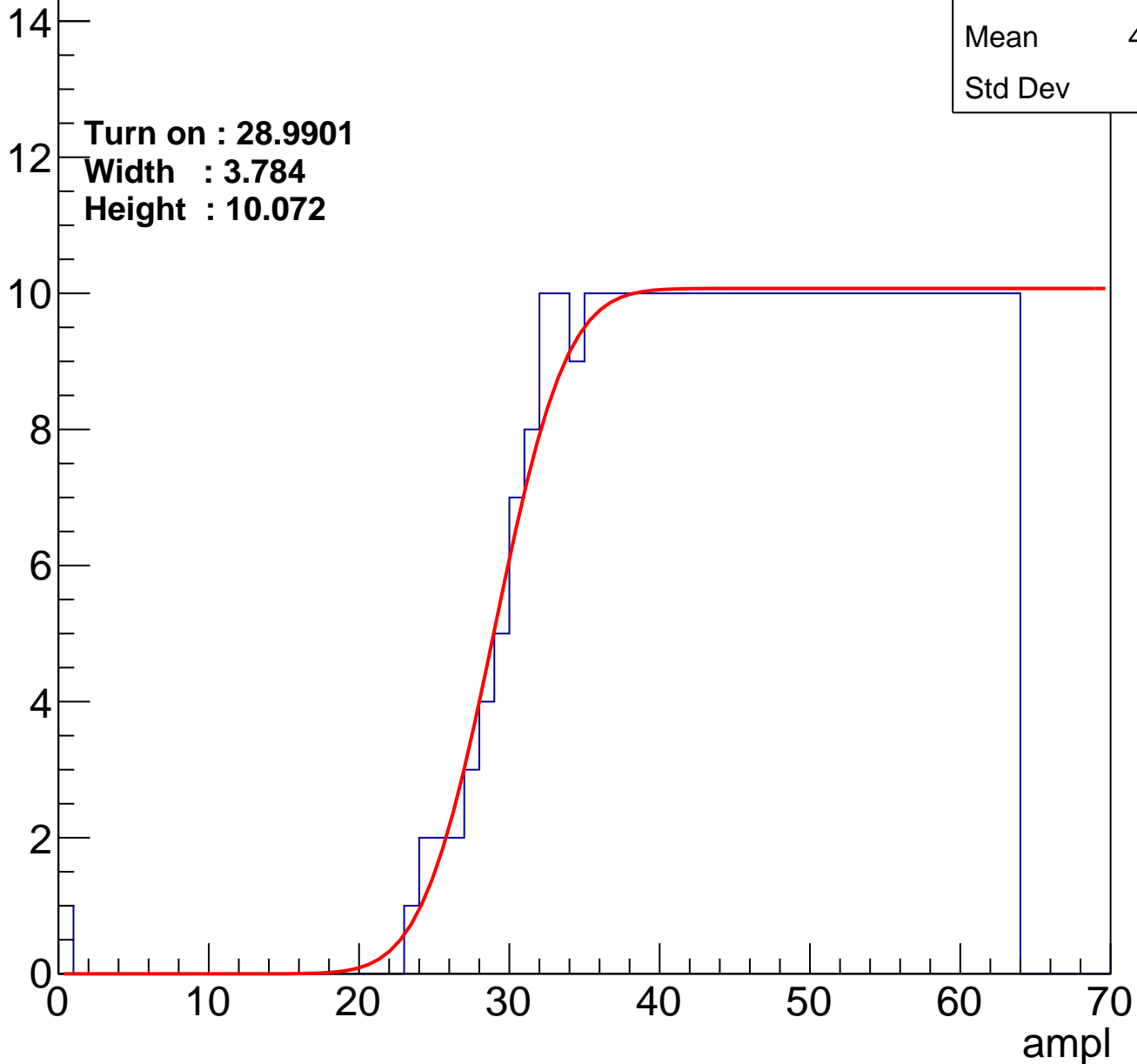
Entries	354
Mean	45.58
Std Dev	10.7

Turn on : 28.9901

Width : 3.784

Height : 10.072

Entry



# B1L101S, U26-ch126

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	378
Mean	44.24
Std Dev	11.74

Turn on : 26.9682

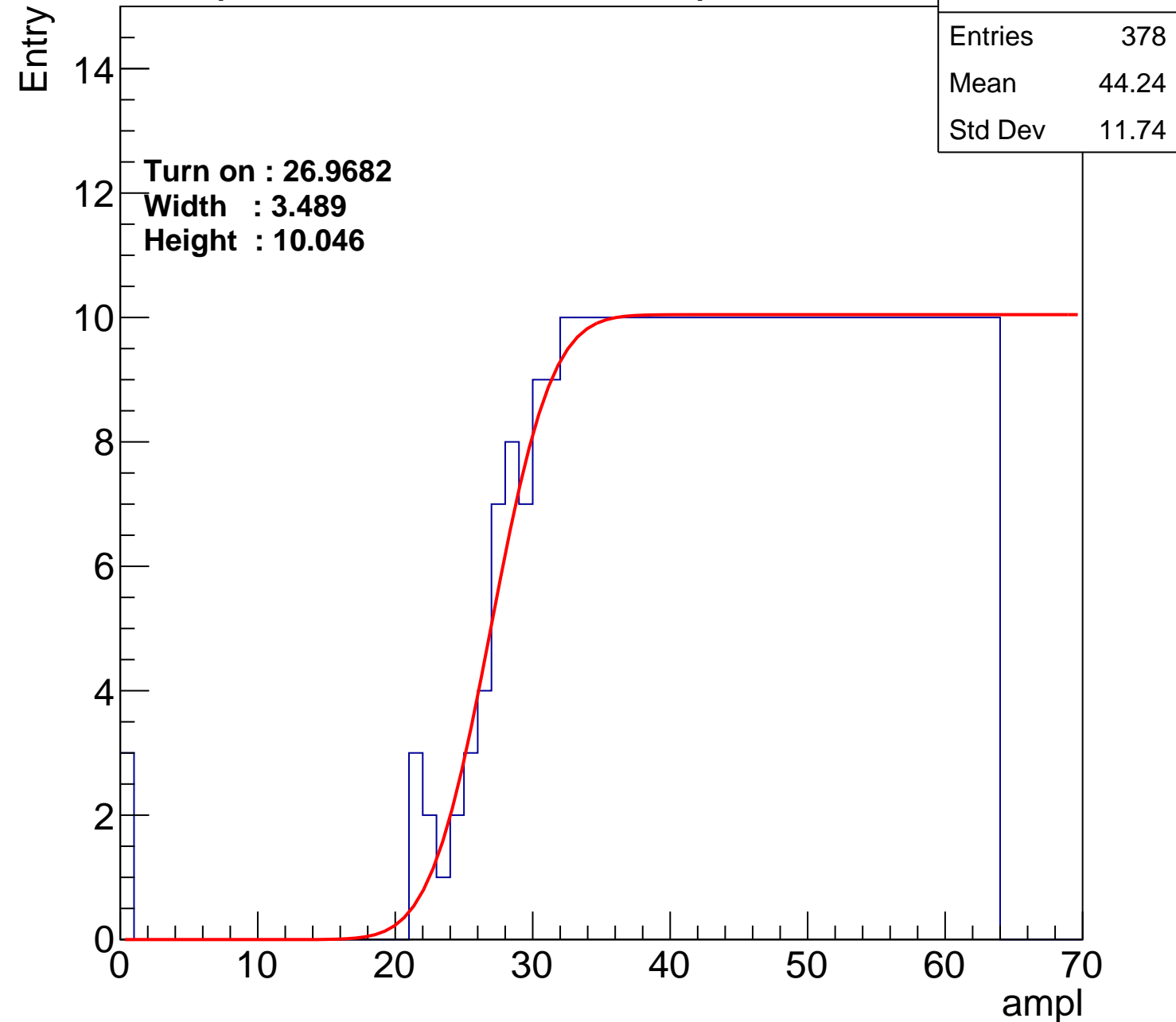
Width : 3.489

Height : 10.046

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L101S, U26-ch127

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	348
Mean	45.61
Std Dev	11.37

Turn on : 29.3067

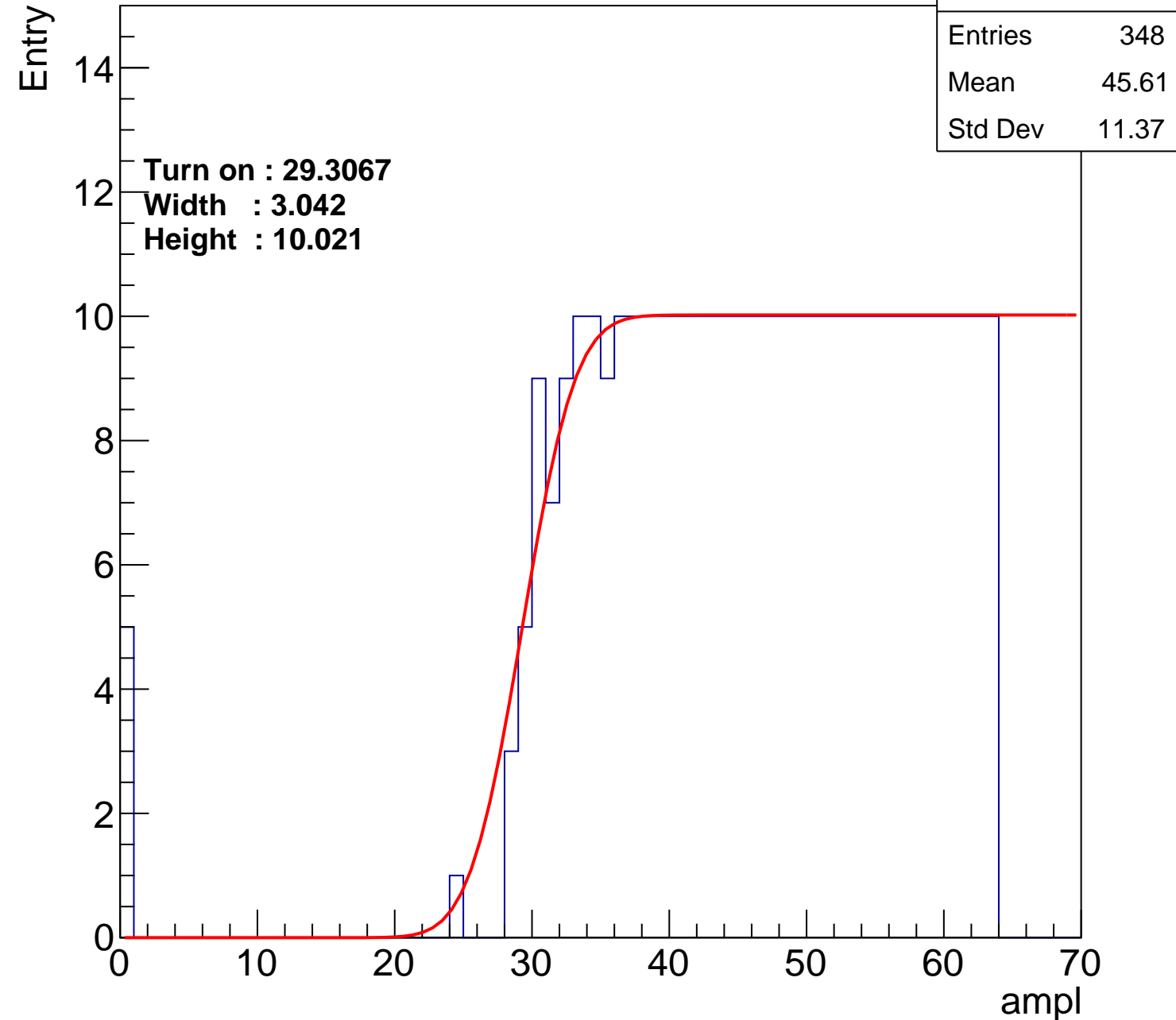
Width : 3.042

Height : 10.021

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L101S, U26-ch127

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	348
Mean	45.61
Std Dev	11.37

Turn on : 29.3067

Width : 3.042

Height : 10.021

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

