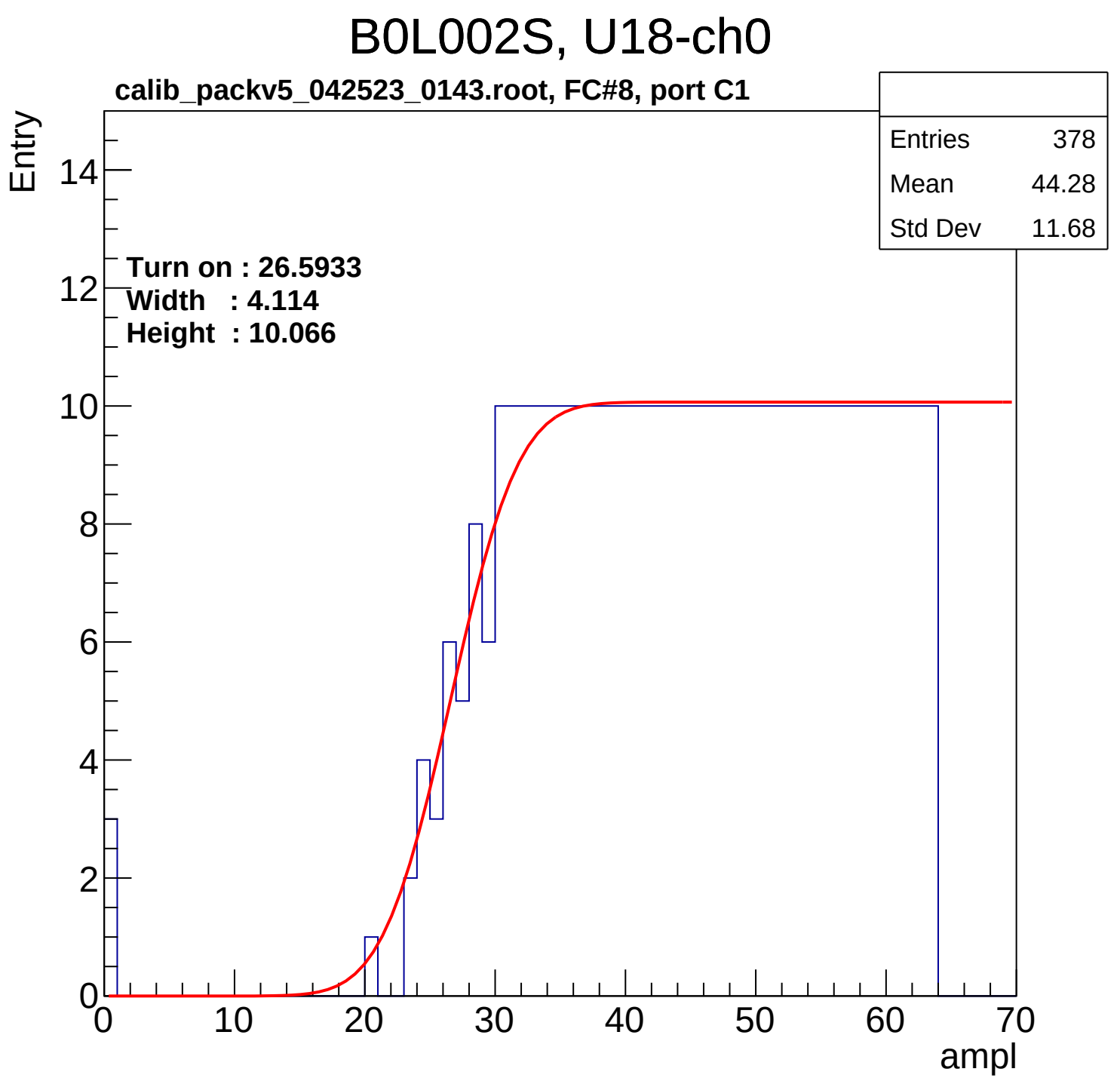
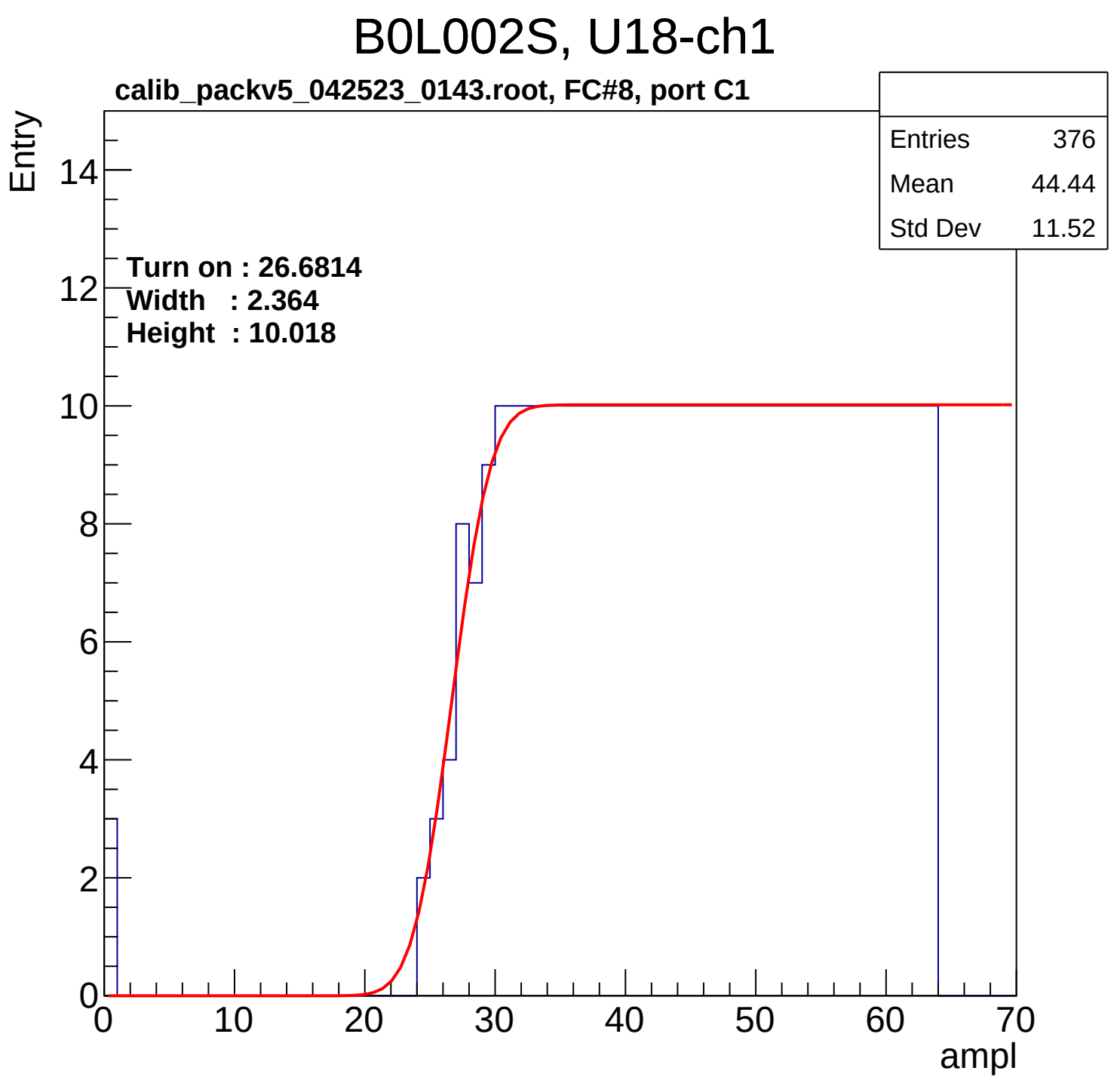
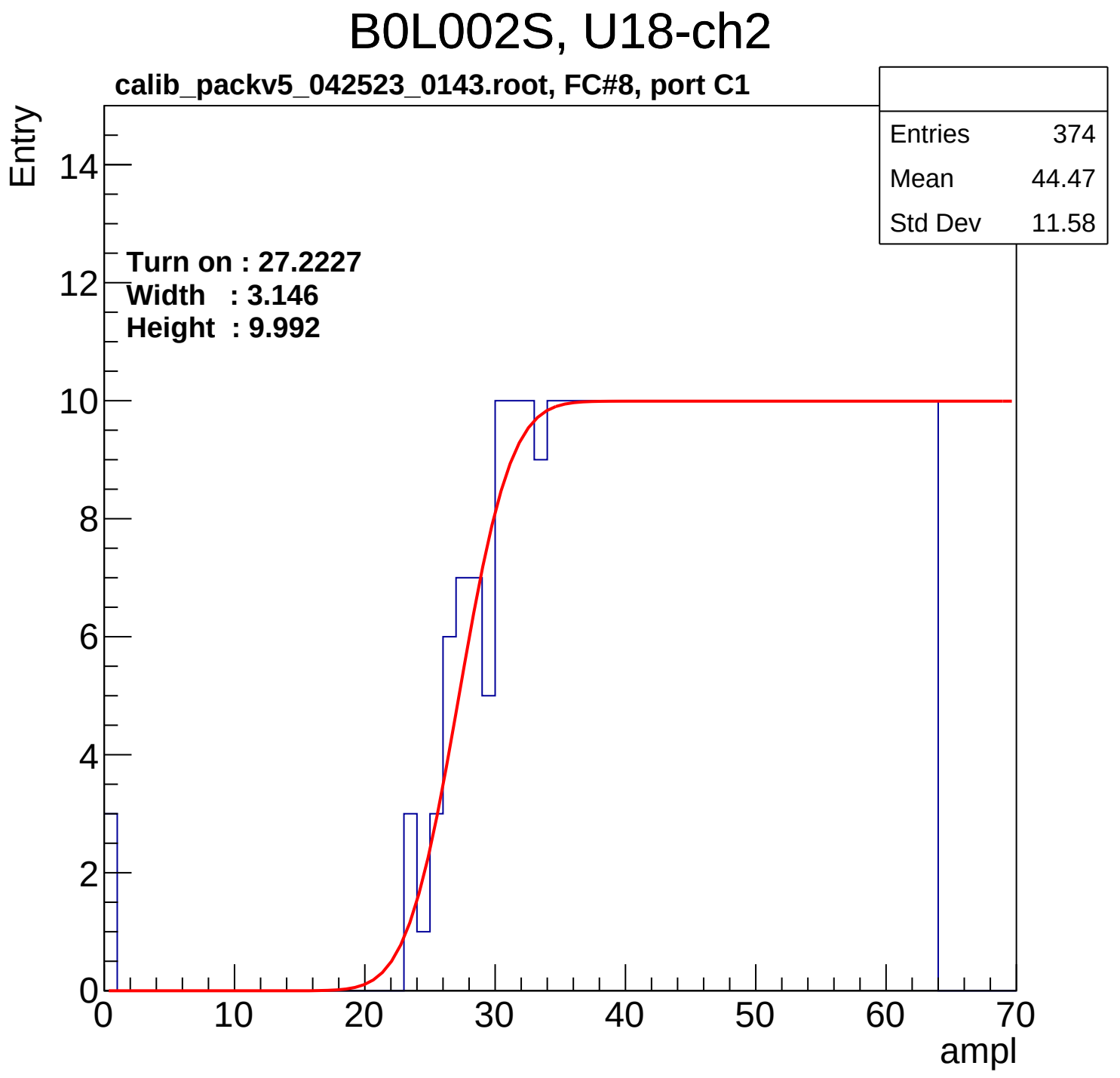
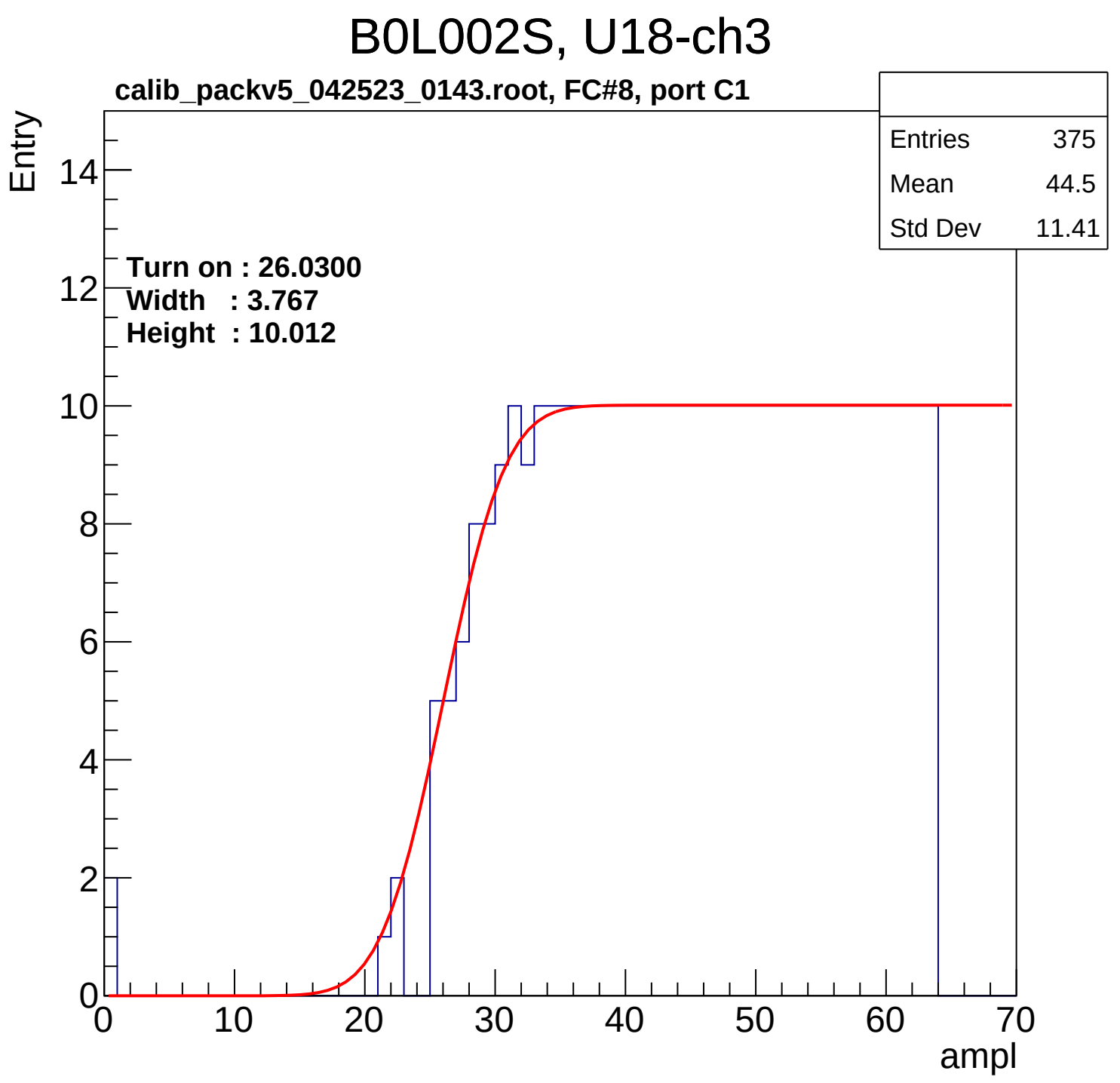
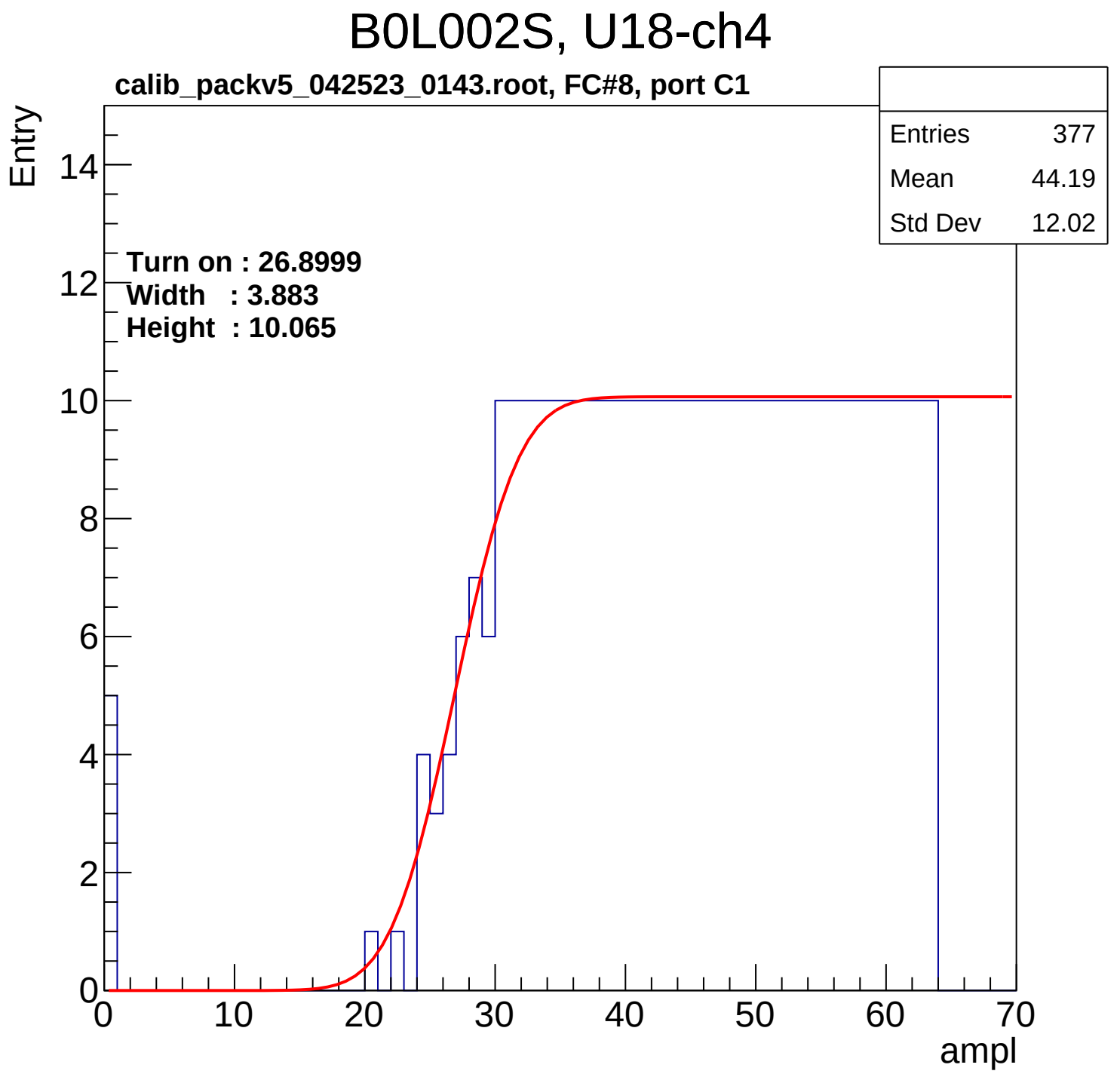
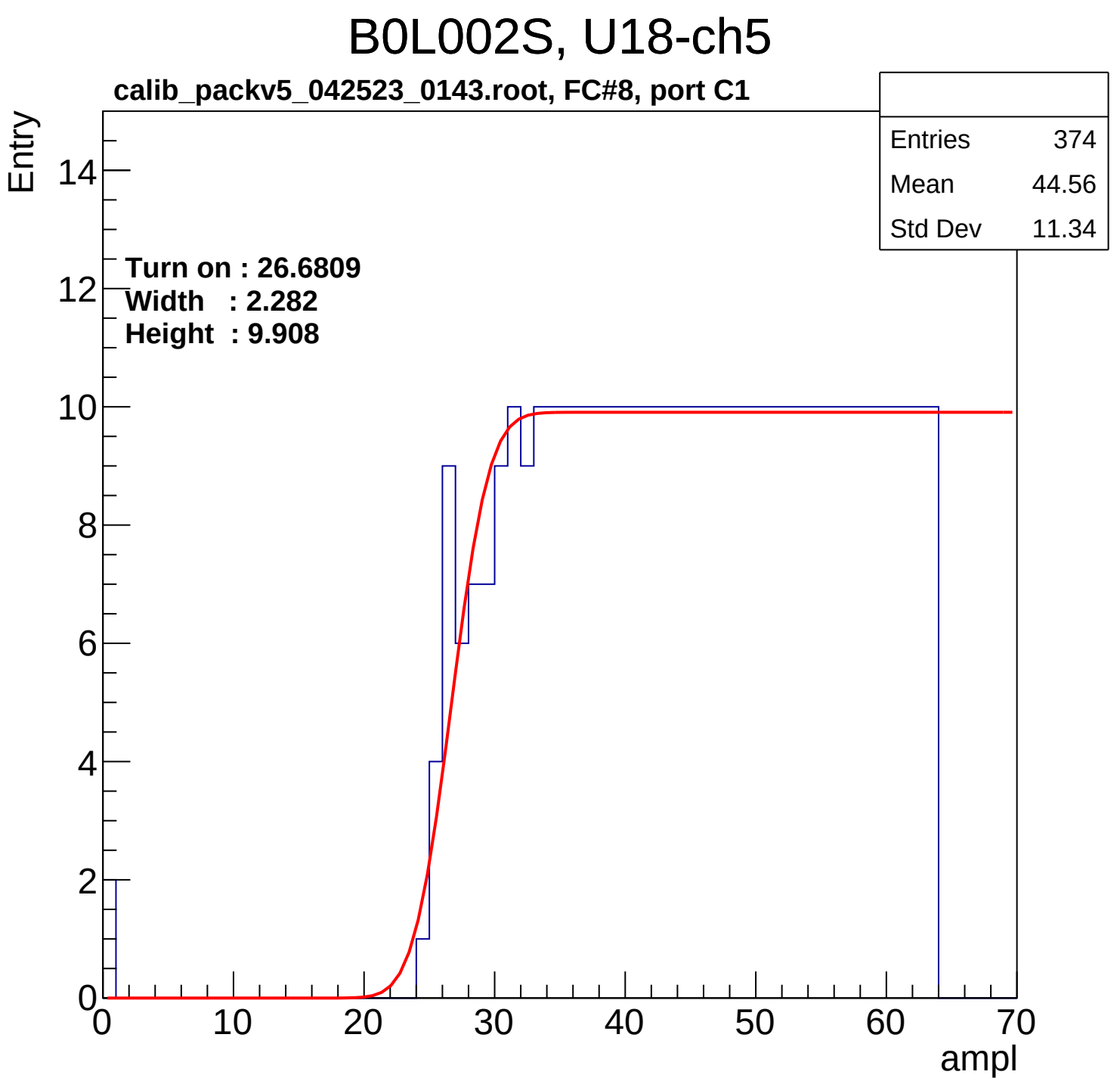

B0L002S, U18-ch0
calib_packv5_042523_0143.root, FC#8, port C1
Entries 378
Mean 44.28
Std Dev 11.68
Turn on : 26.5933
Width : 4.114
Height : 10.066
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

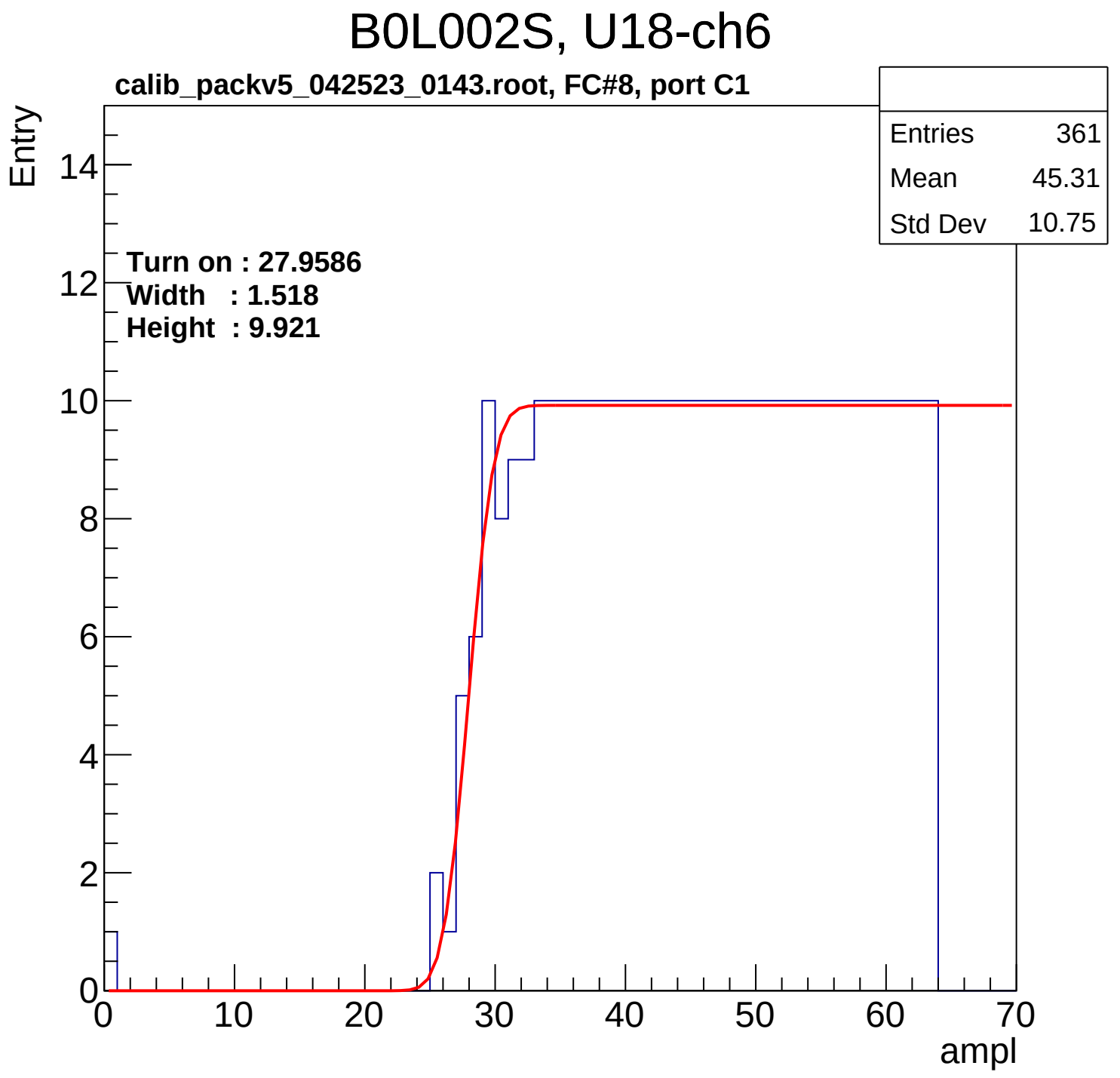

B0L002S, U18-ch1
calib_packv5_042523_0143.root, FC#8, port C1
Entries 376
Mean 44.44
Std Dev 11.52
Turn on : 26.6814
Width : 2.364
Height : 10.018
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

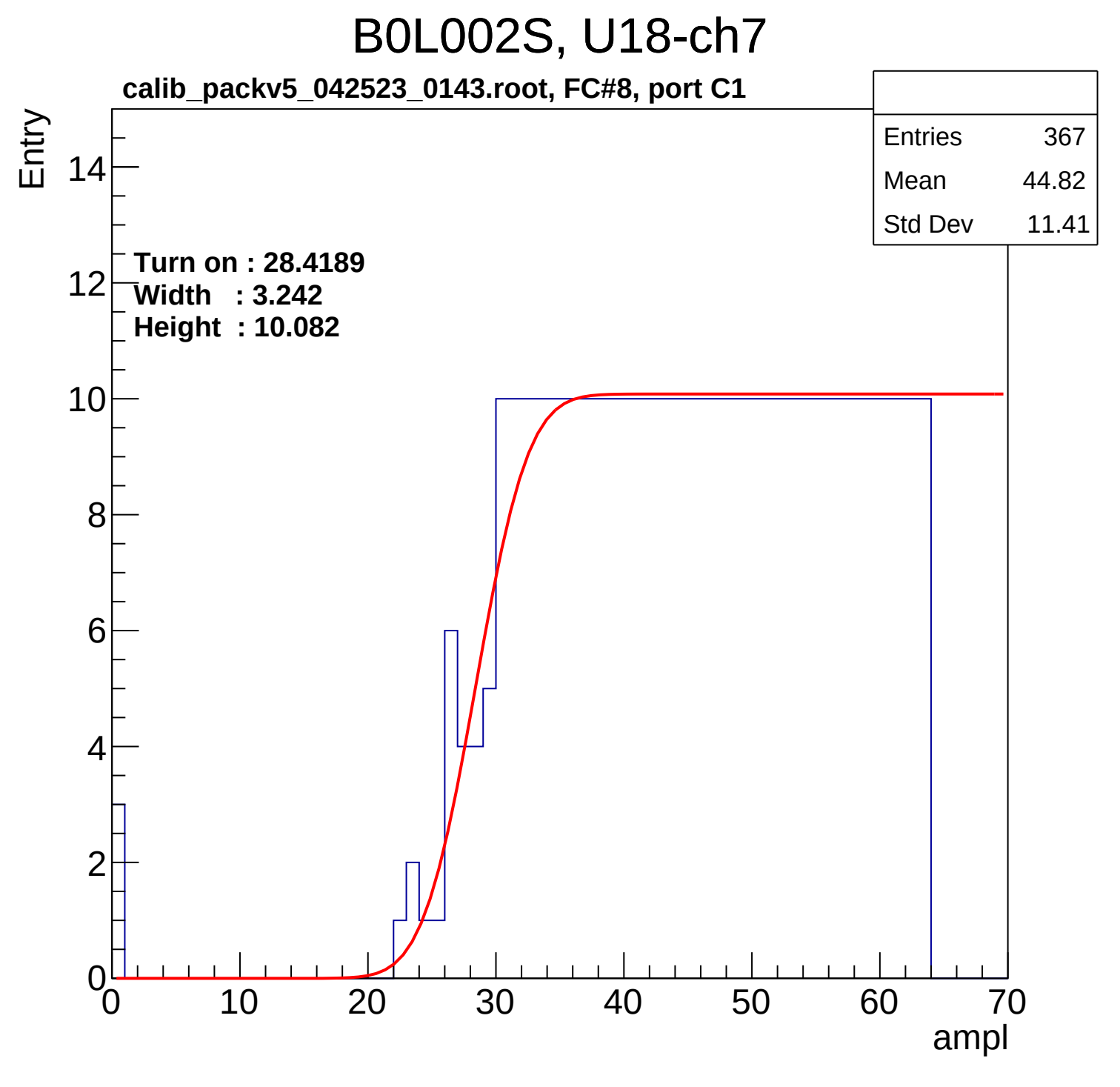

B0L002S, U18-ch2
calib_packv5_042523_0143.root, FC#8, port C1
Entries 374
Mean 44.47
Std Dev 11.58
Turn on : 27.2227
Width : 3.146
Height : 9.992
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

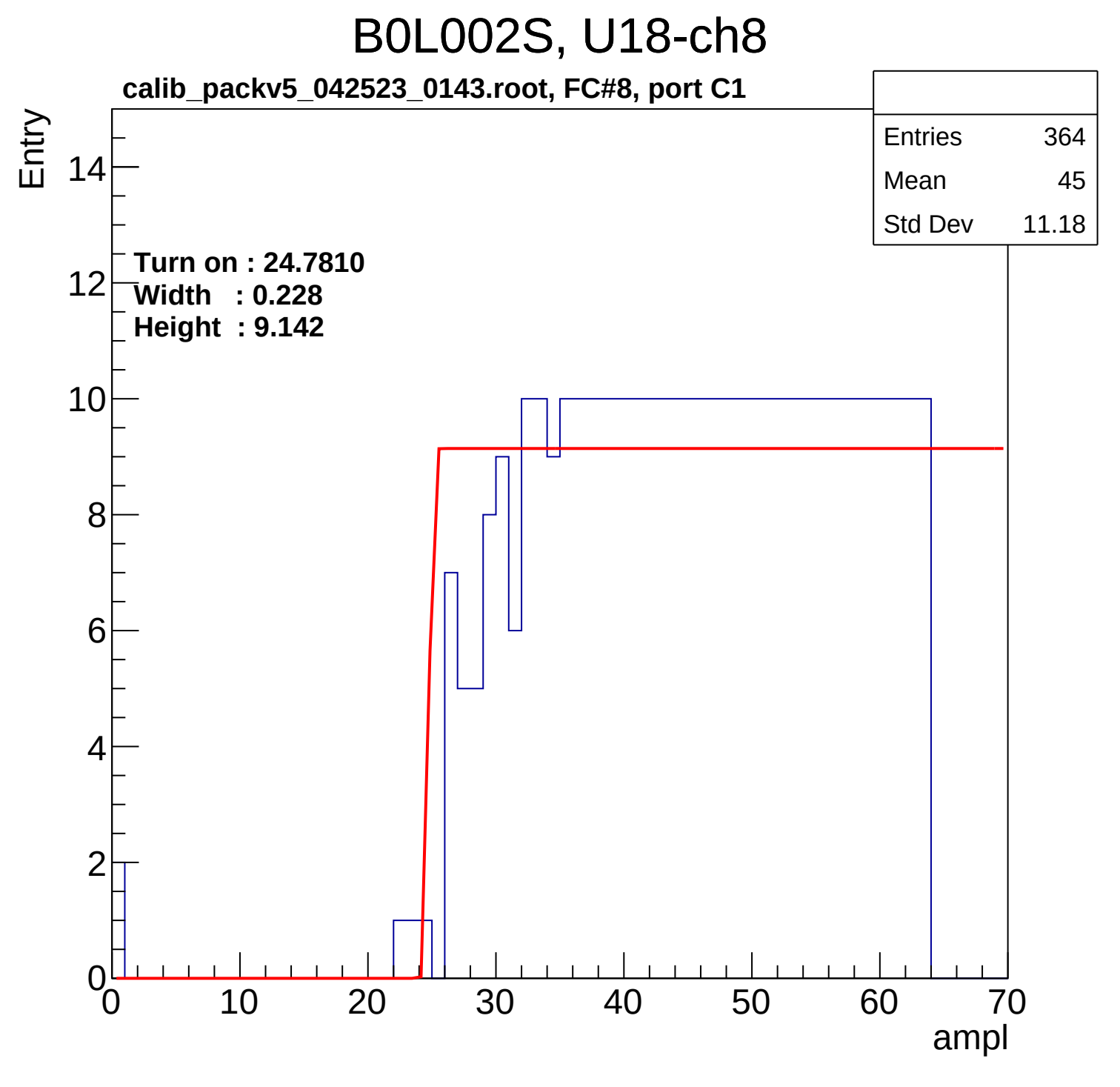

B0L002S, U18-ch3
calib_packv5_042523_0143.root, FC#8, port C1
Entries 375
Mean 44.5
Std Dev 11.41
Turn on : 26.0300
Width : 3.767
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

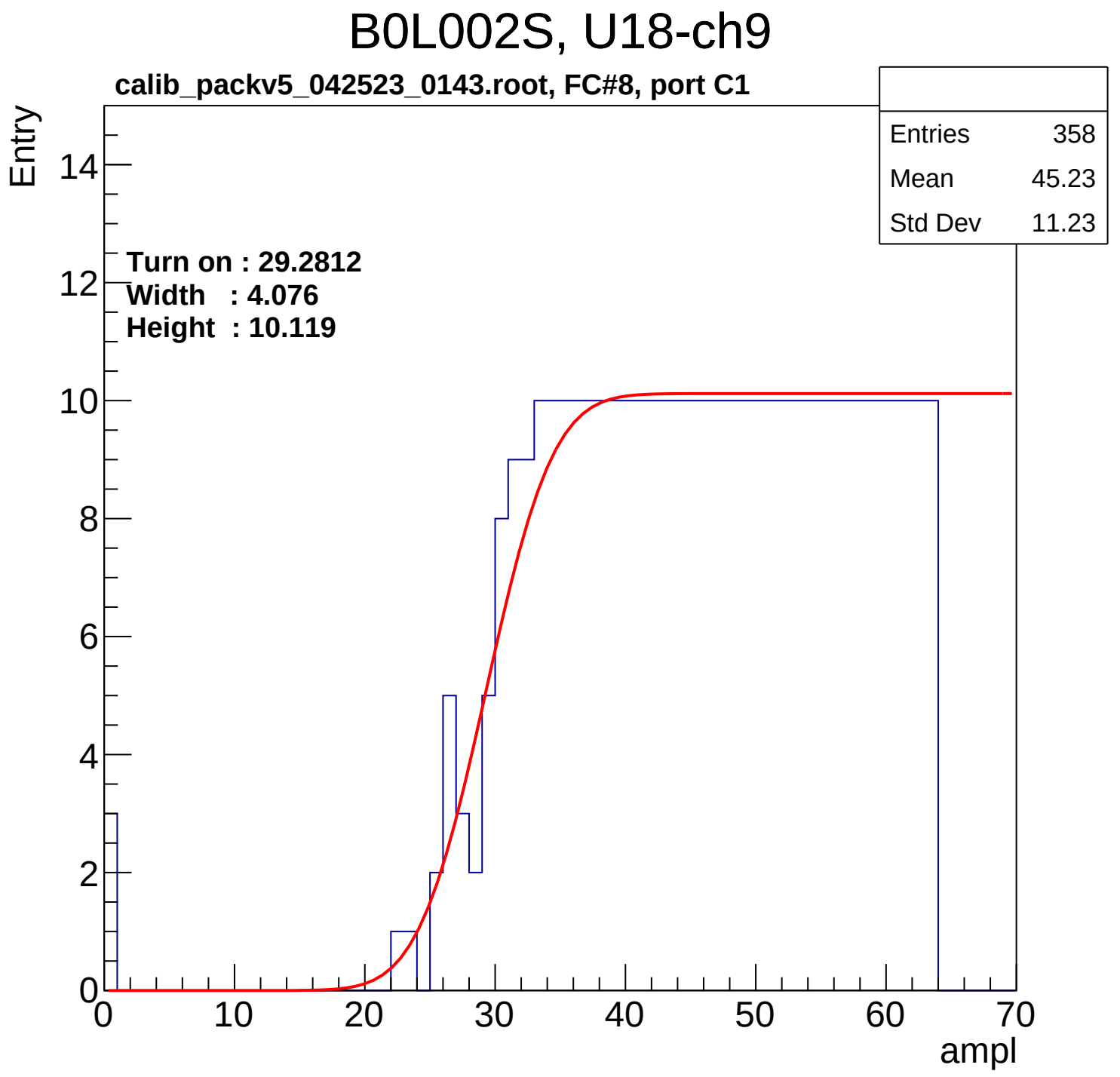

B0L002S, U18-ch4
calib_packv5_042523_0143.root, FC#8, port C1
Entries 377
Mean 44.19
Std Dev 12.02
Turn on : 26.8999
Width : 3.883
Height : 10.065
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

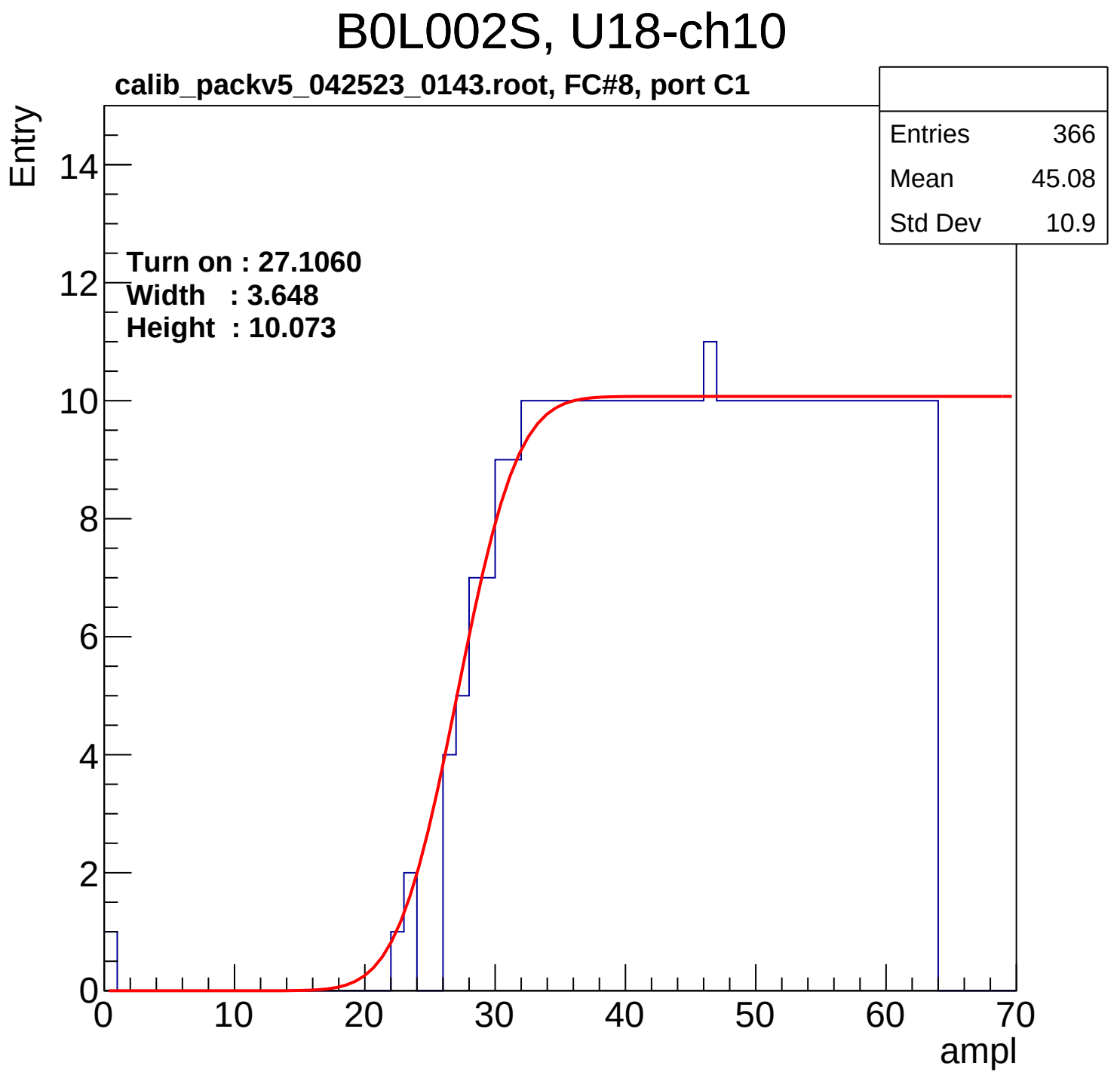

B0L002S, U18-ch5
calib_packv5_042523_0143.root, FC#8, port C1
Entries 374
Mean 44.56
Std Dev 11.34
Turn on : 26.6809
Width : 2.282
Height : 9.908
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

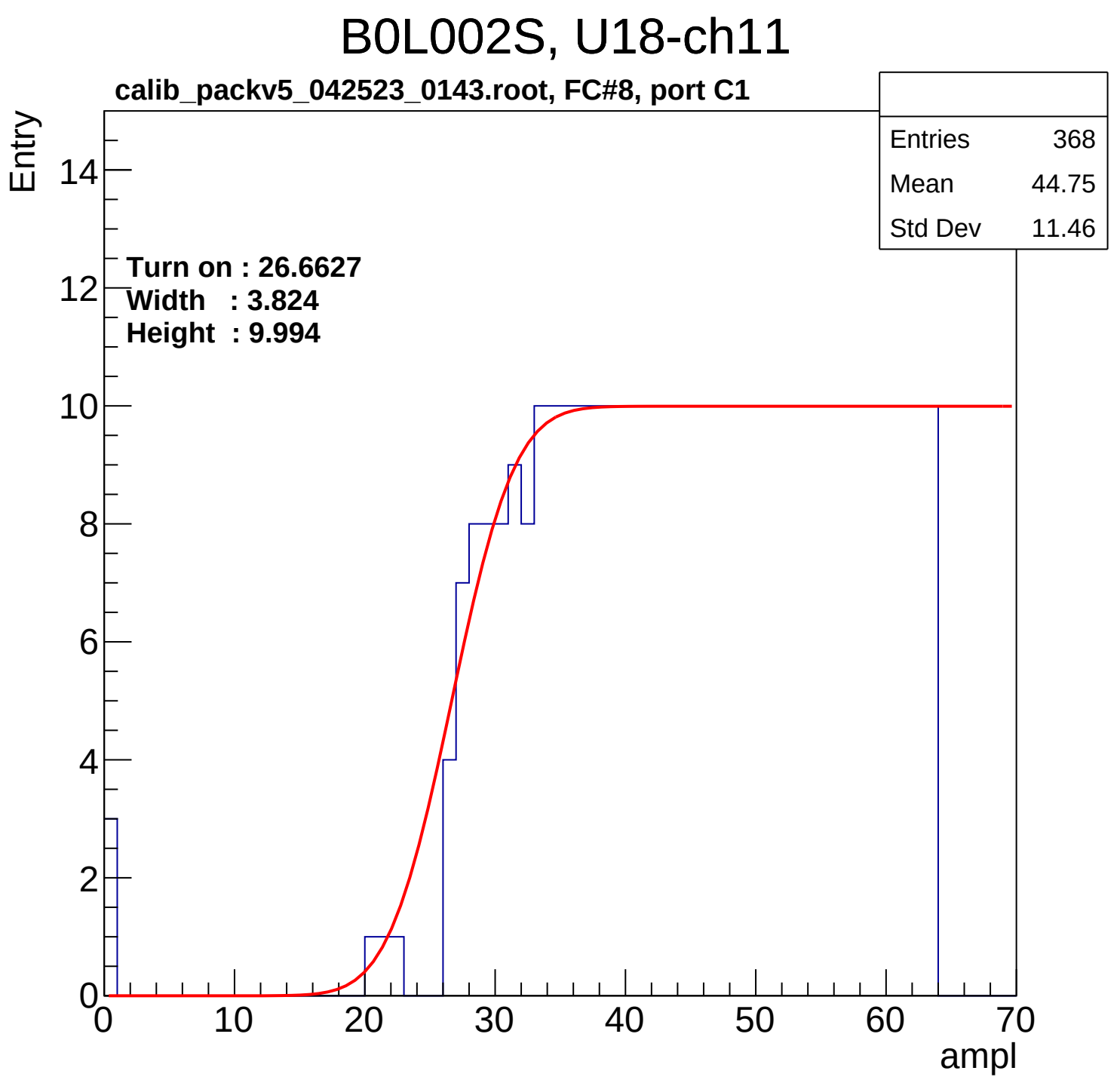

B0L002S, U18-ch6
calib_packv5_042523_0143.root, FC#8, port C1
Entries 361
Mean 45.31
Std Dev 10.75
Turn on : 27.9586
Width : 1.518
Height : 9.921
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

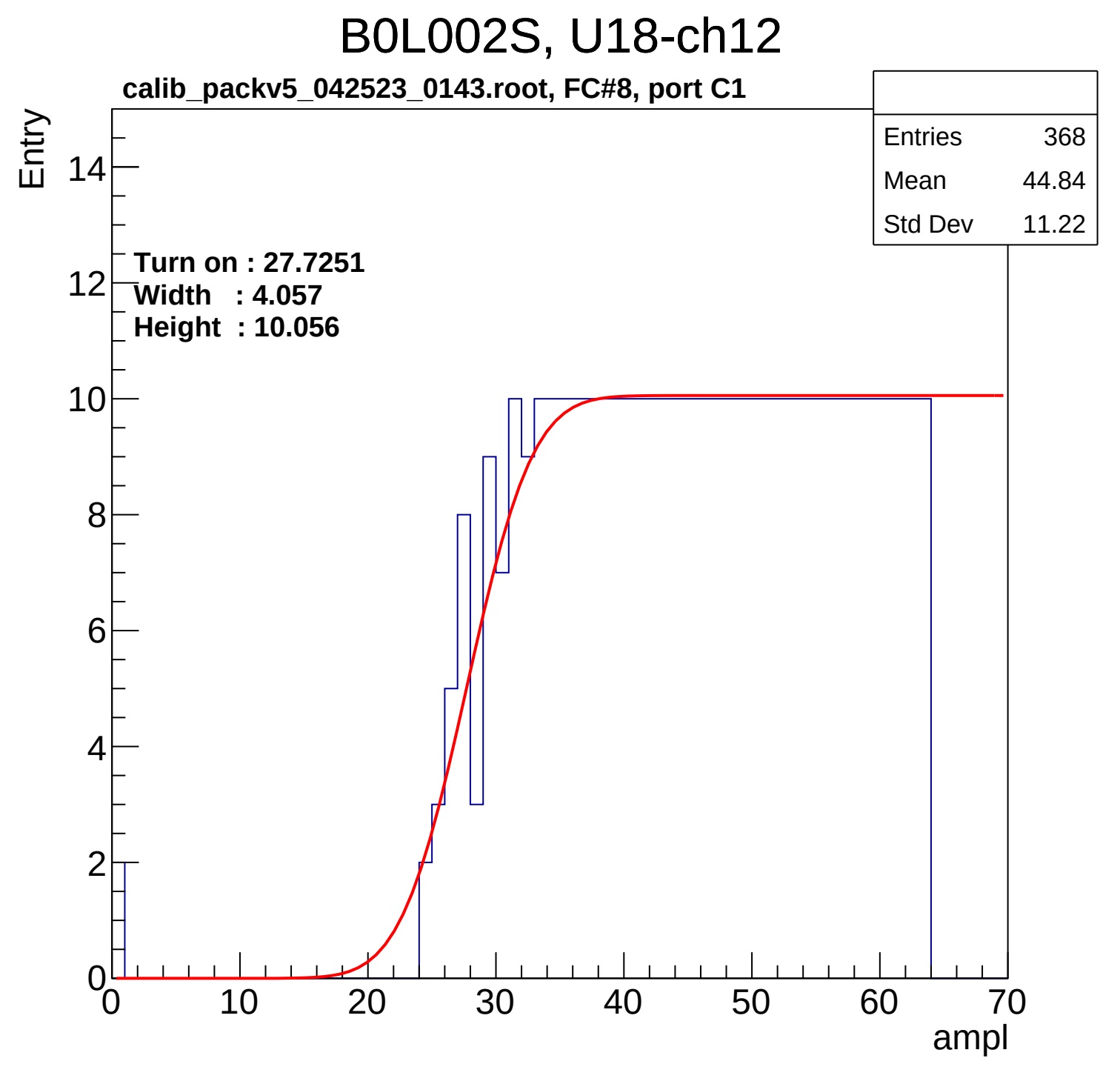

B0L002S, U18-ch7
calib_packv5_042523_0143.root, FC#8, port C1
Entries 367
Mean 44.82
Std Dev 11.41
Turn on : 28.4189
Width : 3.242
Height : 10.082
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

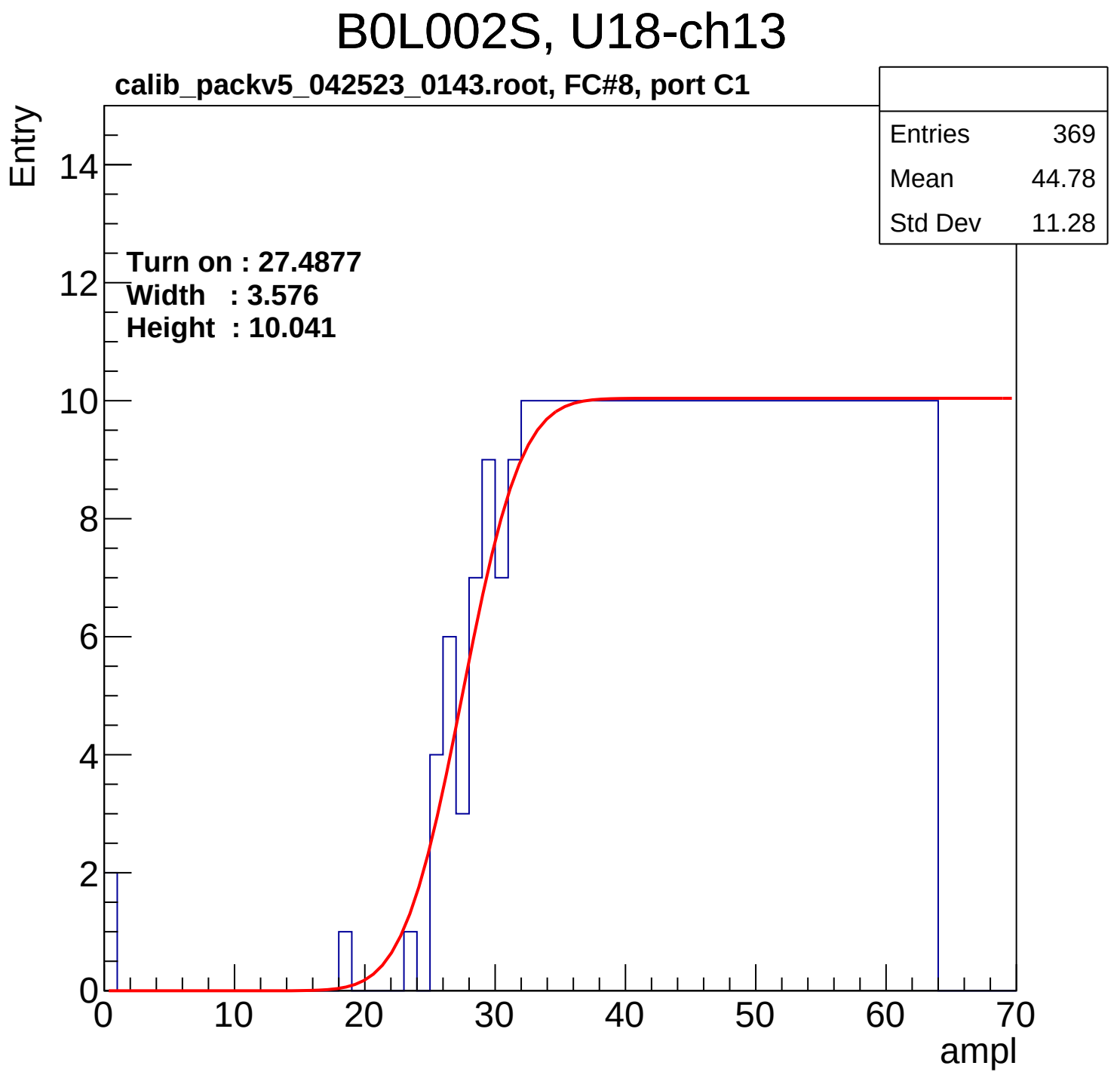

B0L002S, U18-ch8
calib_packv5_042523_0143.root, FC#8, port C1
Entries 364
Mean 45
Std Dev 11.18
Turn on : 24.7810
Width : 0.228
Height : 9.142
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

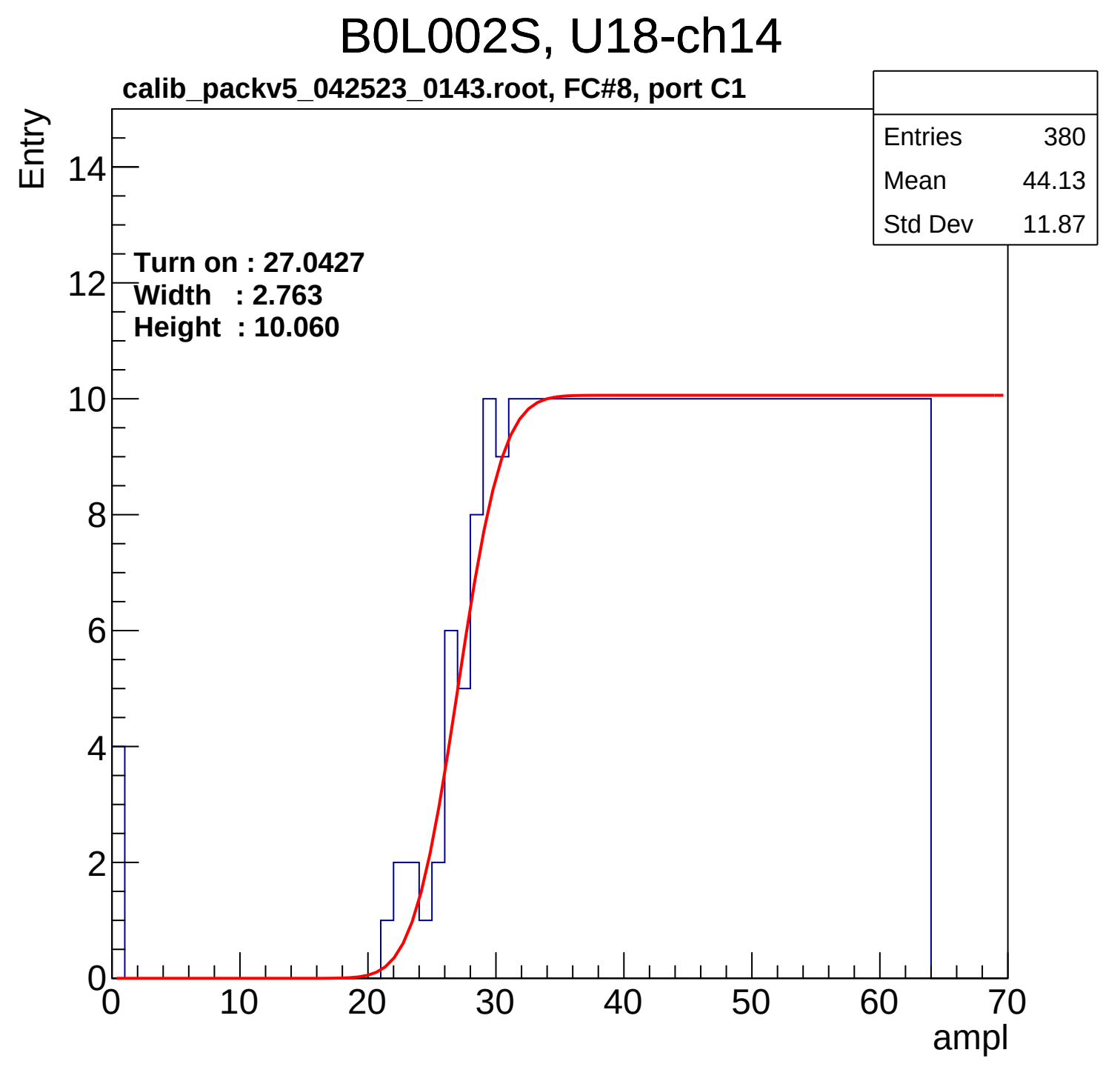

B0L002S, U18-ch9
calib_packv5_042523_0143.root, FC#8, port C1
Entries 358
Mean 45.23
Std Dev 11.23
Turn on : 29.2812
Width : 4.076
Height : 10.119
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

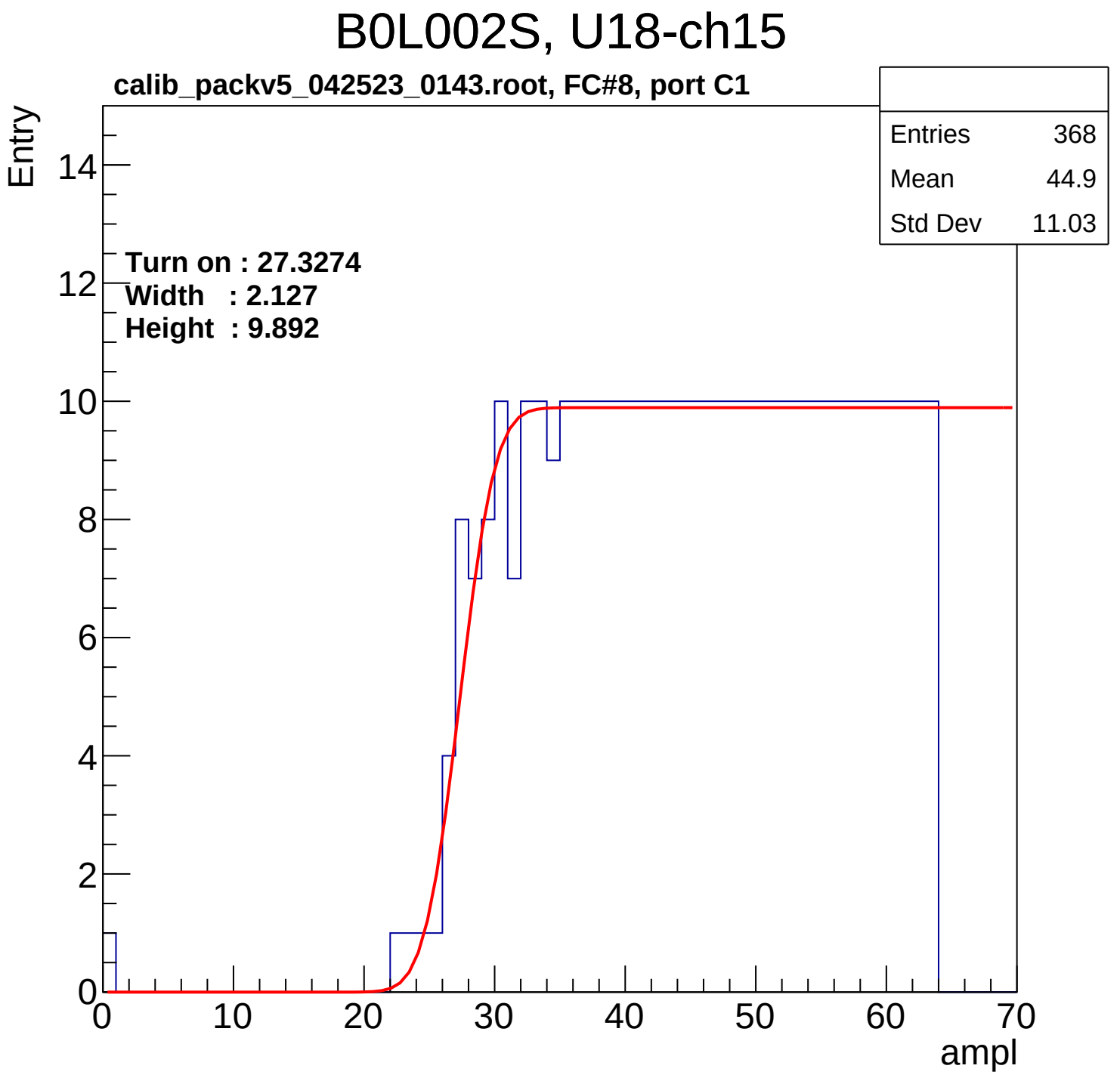

B0L002S, U18-ch10
calib_packv5_042523_0143.root, FC#8, port C1
Entries 366
Mean 45.08
Std Dev 10.9
Turn on : 27.1060
Width : 3.648
Height : 10.073
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

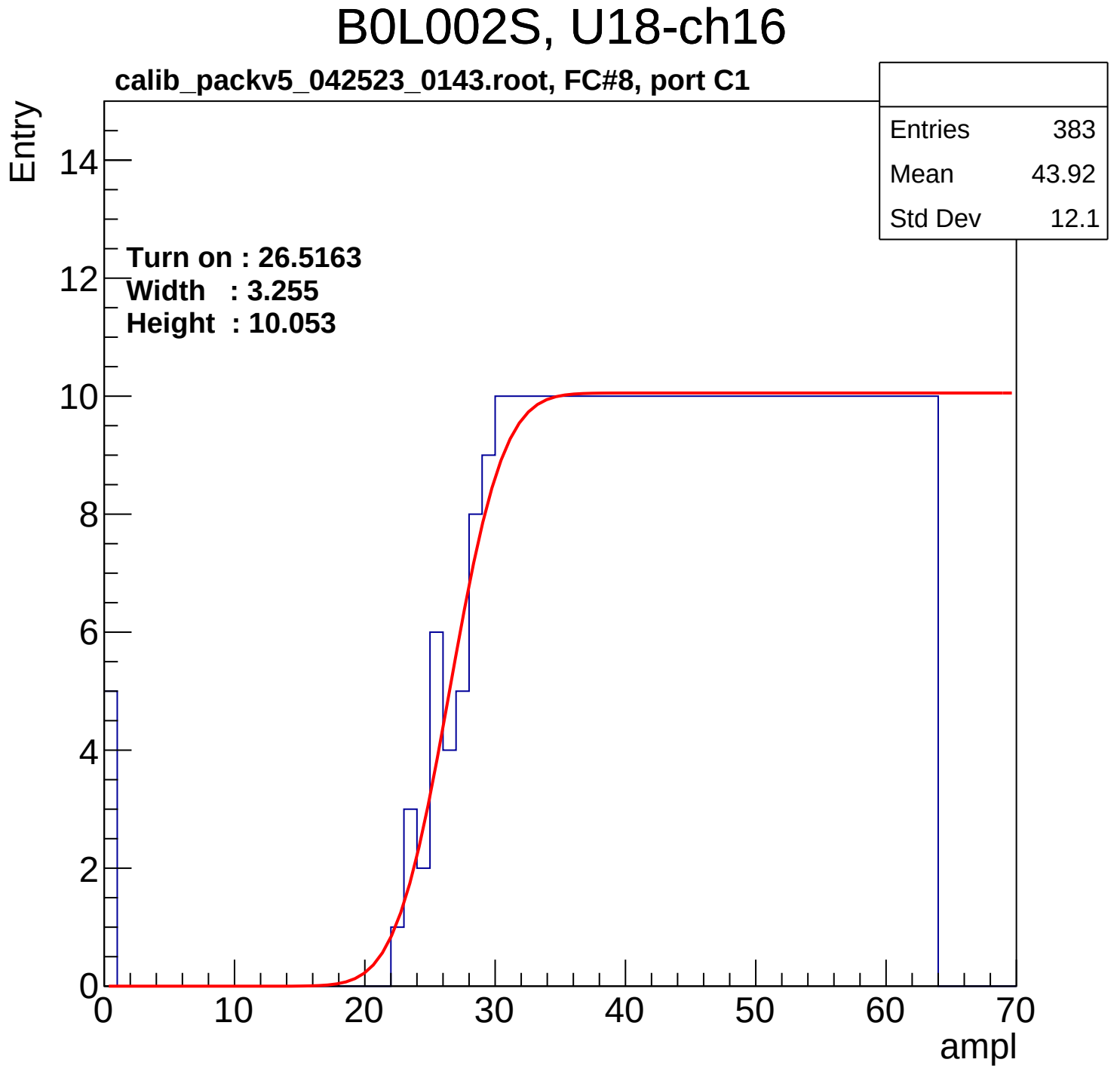

B0L002S, U18-ch11
calib_packv5_042523_0143.root, FC#8, port C1
Entries 368
Mean 44.75
Std Dev 11.46
Turn on : 26.6627
Width : 3.824
Height : 9.994
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

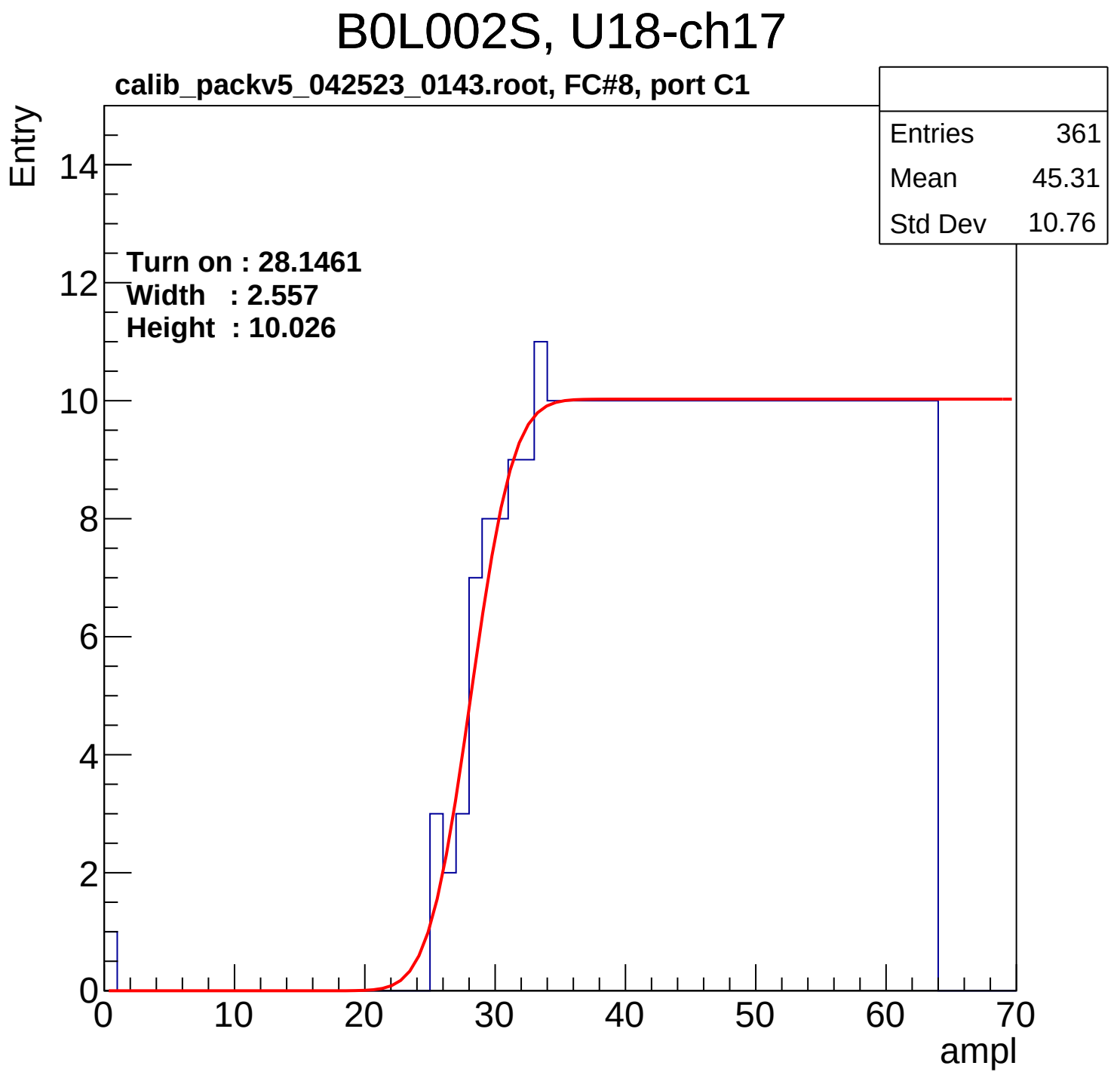

B0L002S, U18-ch12
calib_packv5_042523_0143.root, FC#8, port C1
Entries 368
Mean 44.84
Std Dev 11.22
Turn on : 27.7251
Width : 4.057
Height : 10.056
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

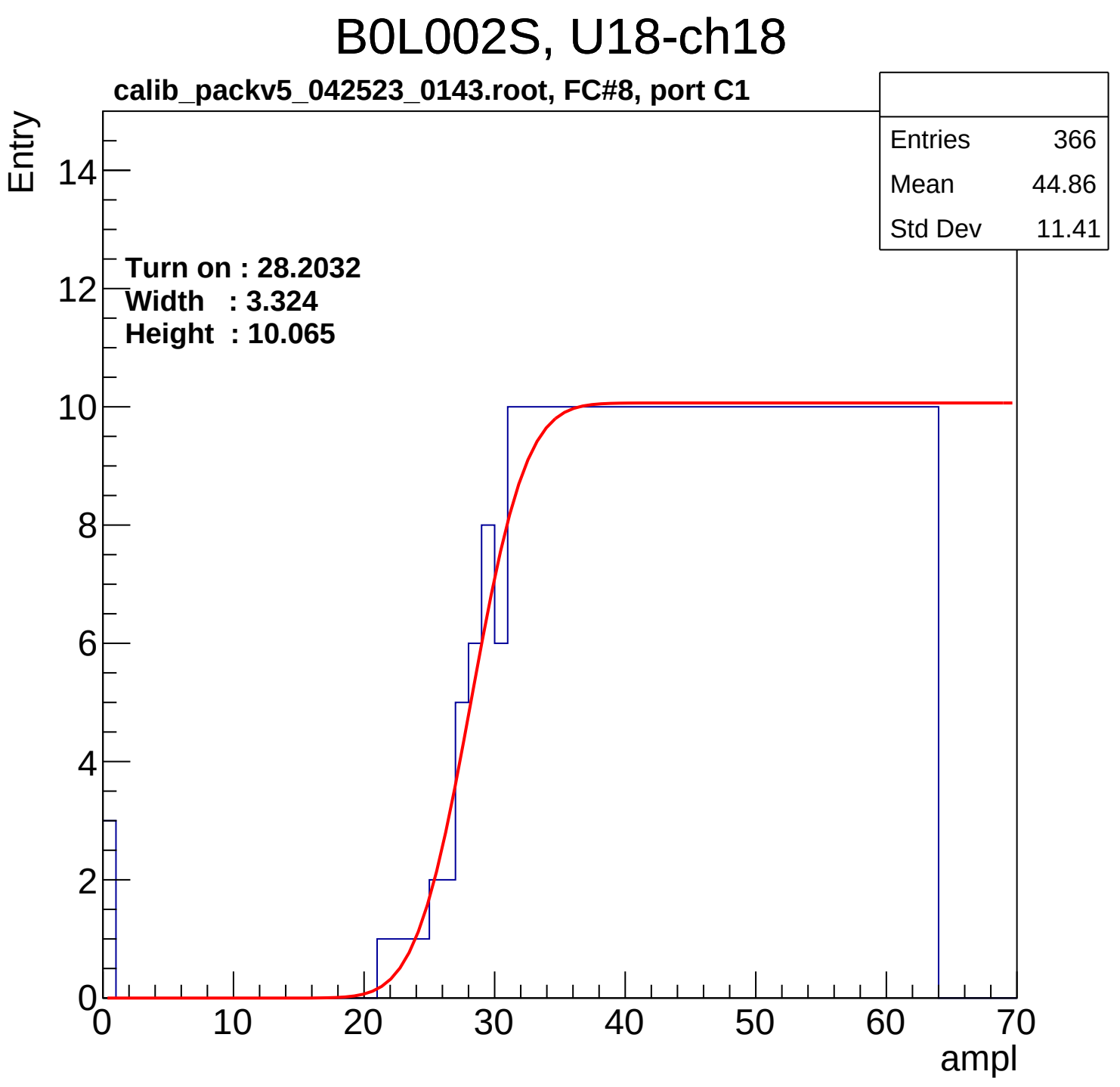

B0L002S, U18-ch13
calib_packv5_042523_0143.root, FC#8, port C1
Entries 369
Mean 44.78
Std Dev 11.28
Turn on : 27.4877
Width : 3.576
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

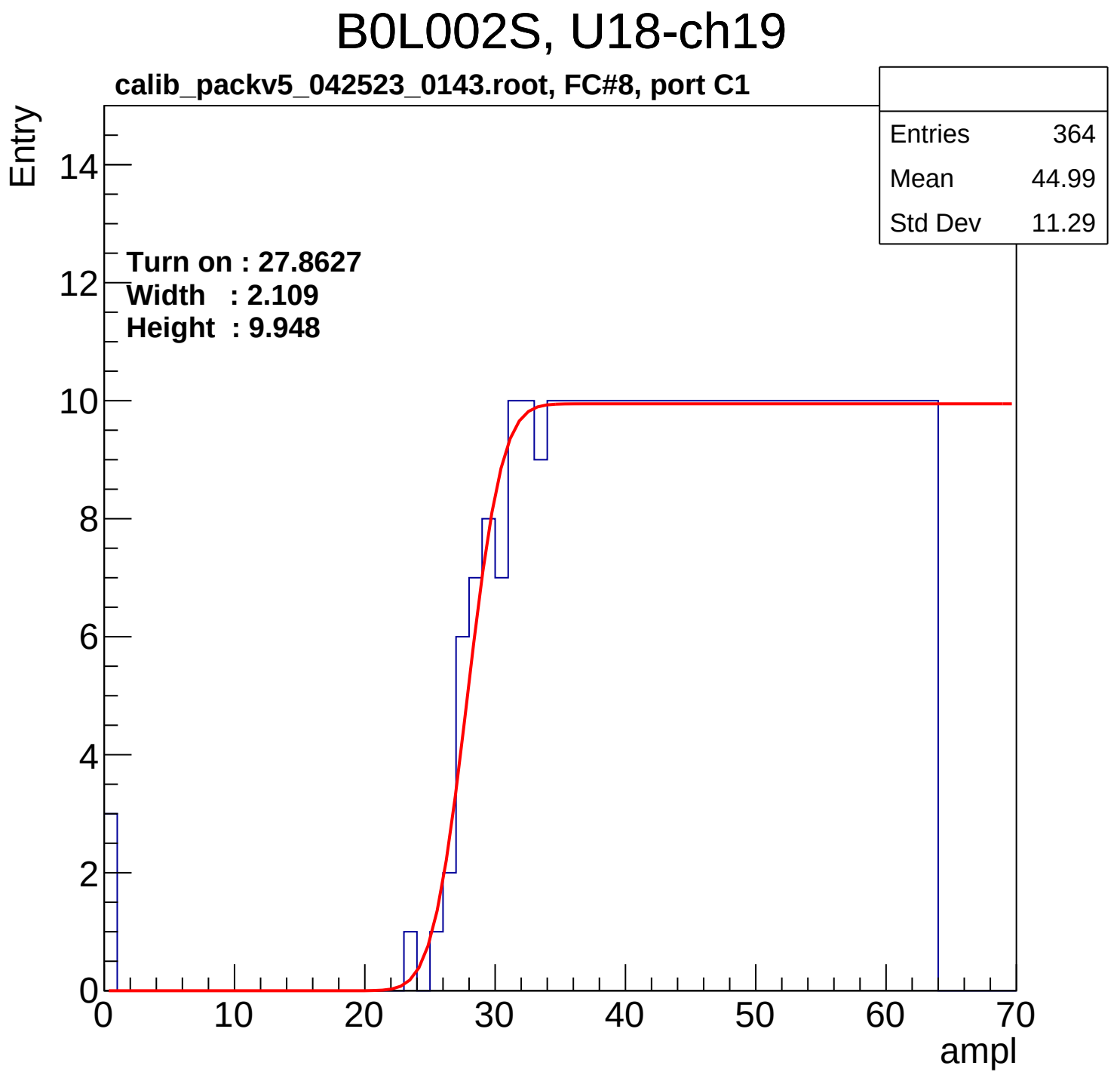

B0L002S, U18-ch14
calib_packv5_042523_0143.root, FC#8, port C1
Entries 380
Mean 44.13
Std Dev 11.87
Turn on : 27.0427
Width : 2.763
Height : 10.060
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

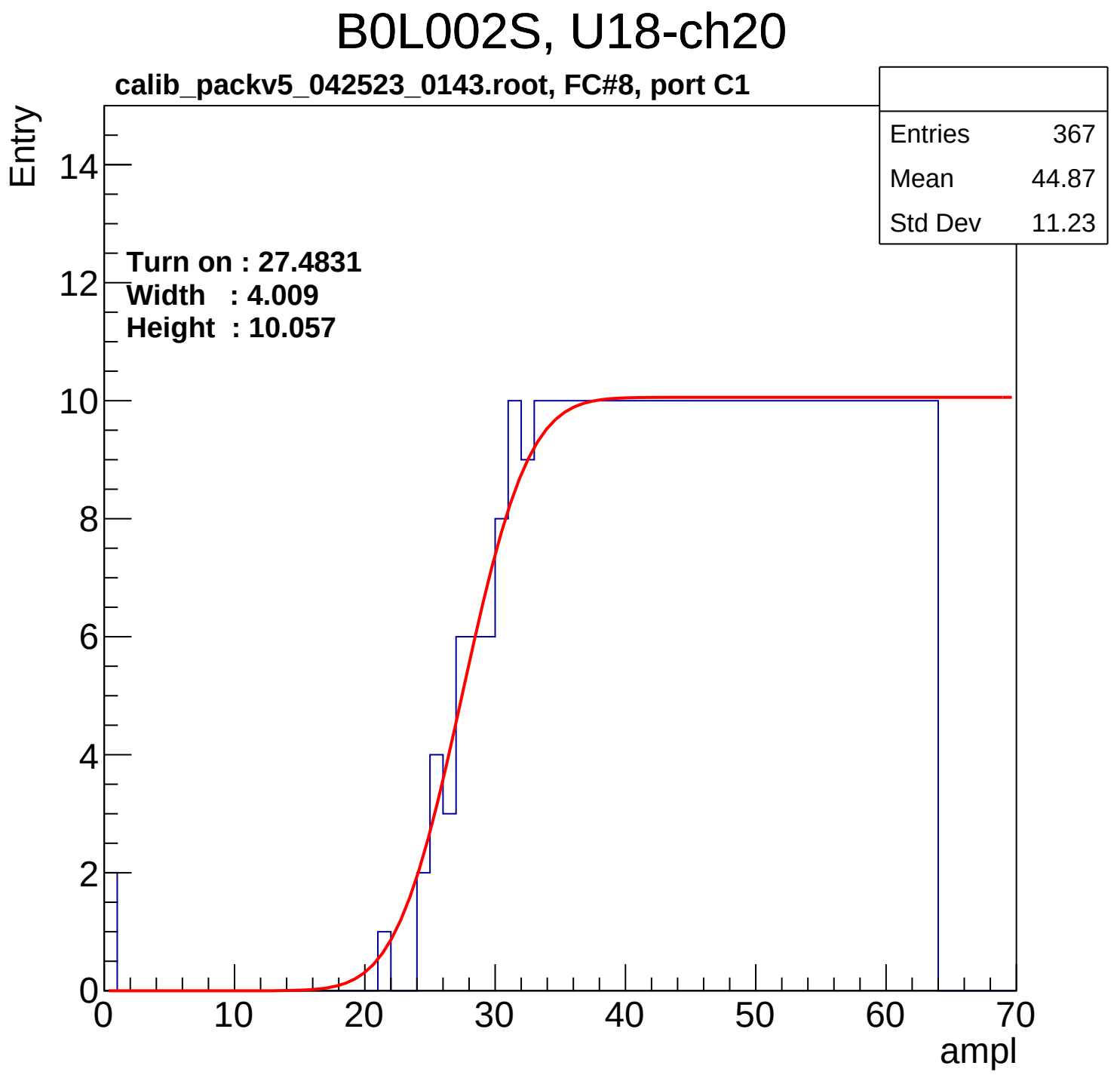

B0L002S, U18-ch15
calib_packv5_042523_0143.root, FC#8, port C1
Entries 368
Mean 44.9
Std Dev 11.03
Turn on : 27.3274
Width : 2.127
Height : 9.892
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

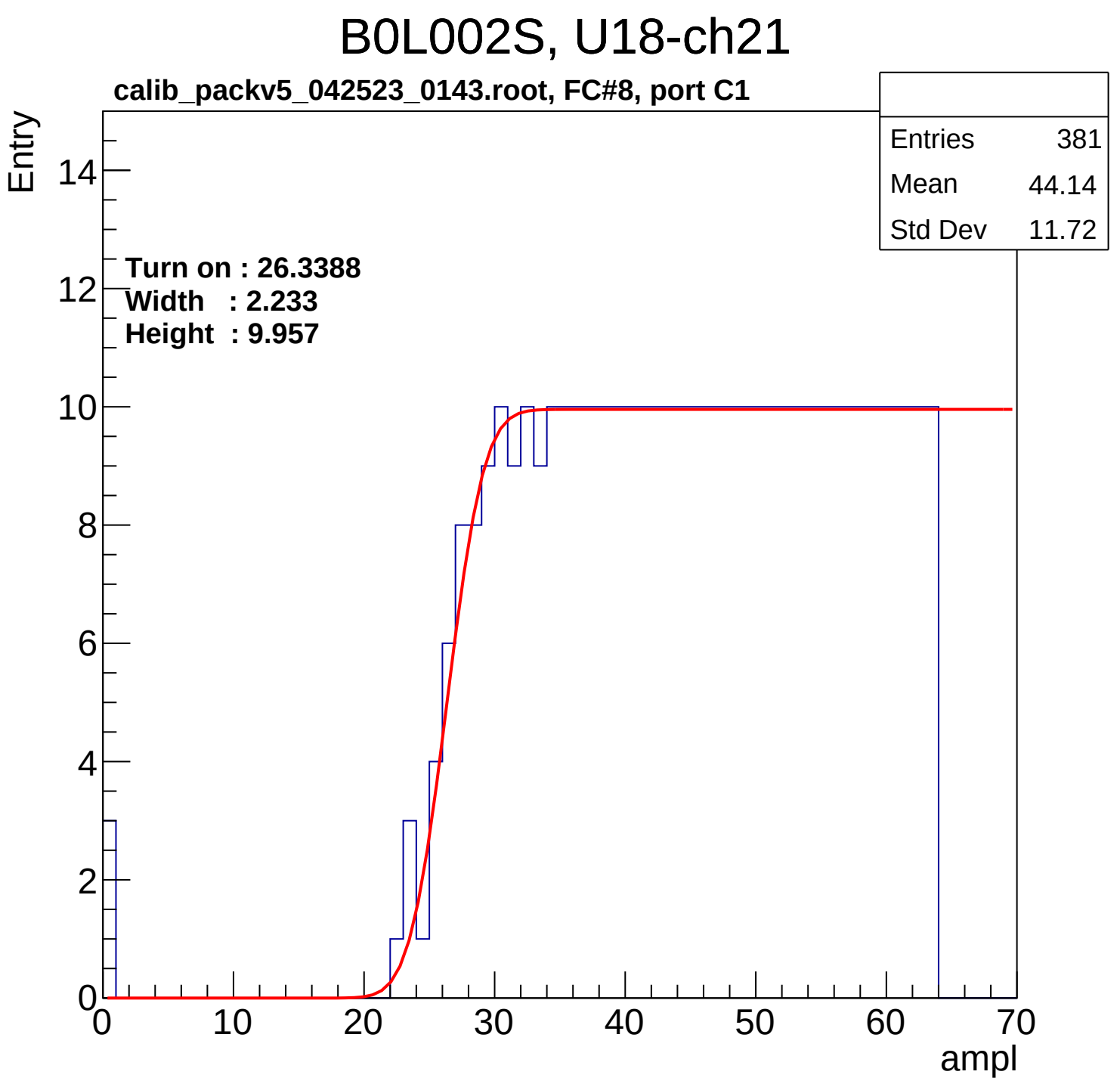

B0L002S, U18-ch16
calib_packv5_042523_0143.root, FC#8, port C1
Entries 383
Mean 43.92
Std Dev 12.1
Turn on : 26.5163
Width : 3.255
Height : 10.053
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

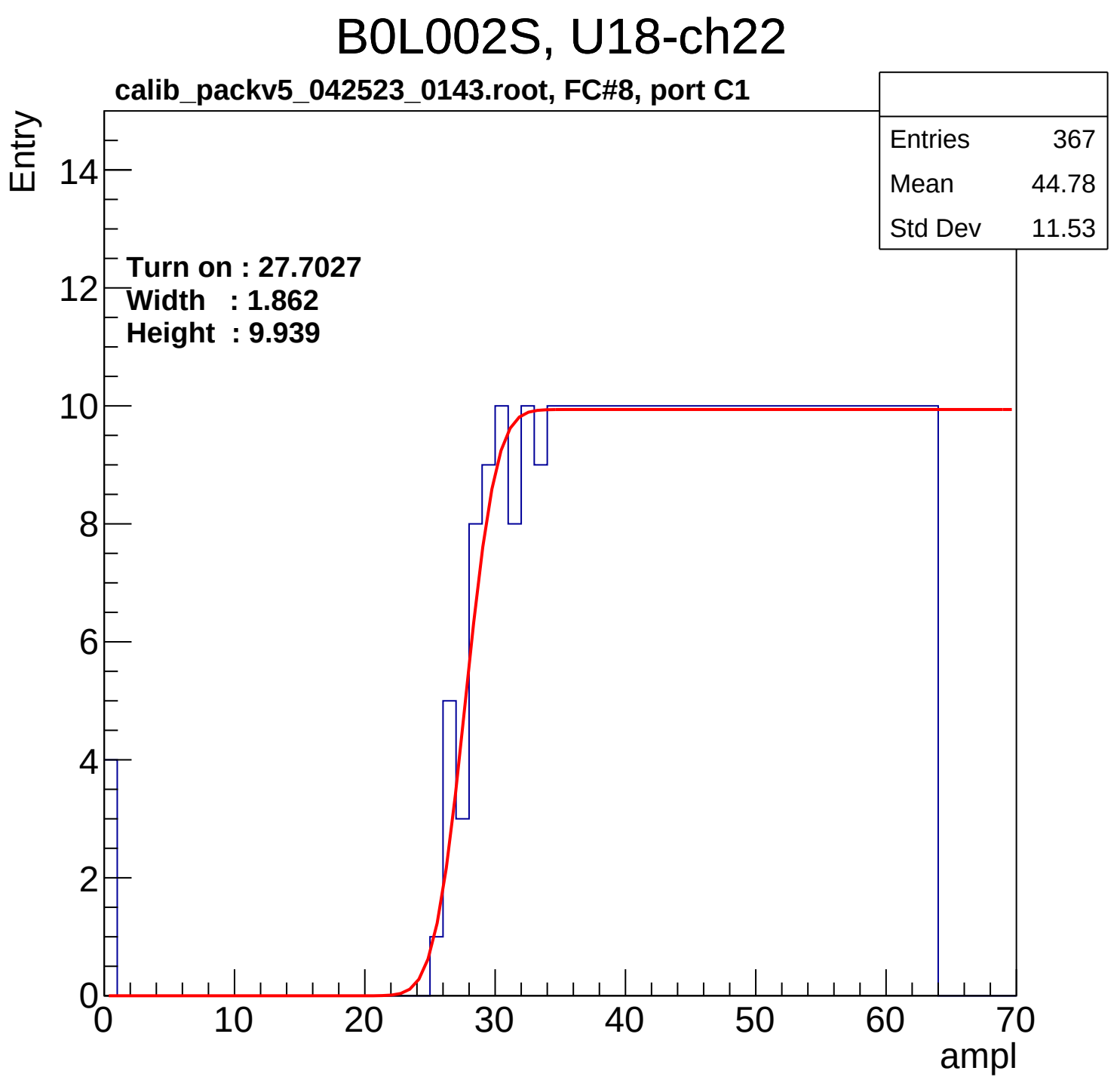

B0L002S, U18-ch17
calib_packv5_042523_0143.root, FC#8, port C1
Entries 361
Mean 45.31
Std Dev 10.76
Turn on : 28.1461
Width : 2.557
Height : 10.026
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

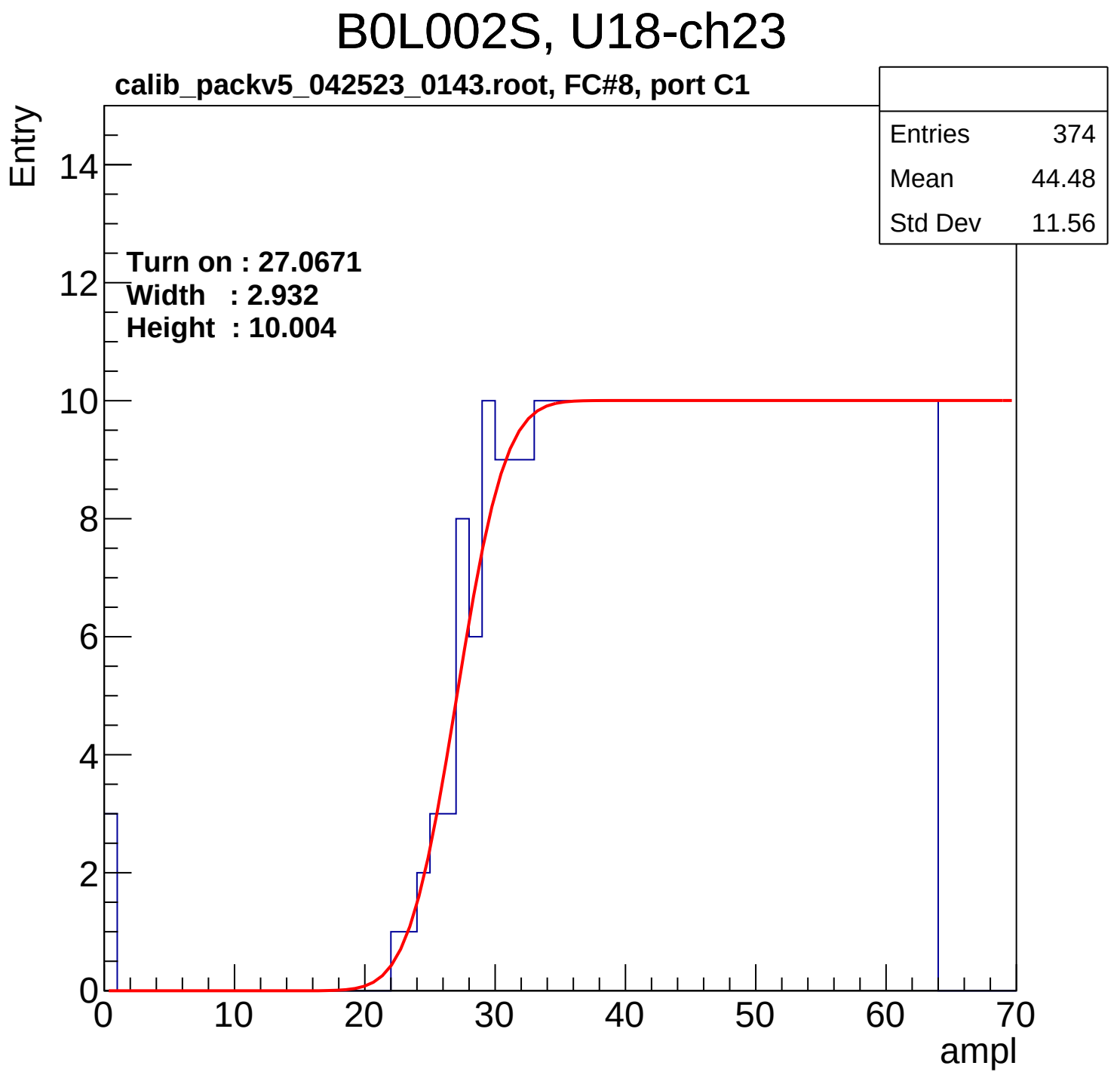

B0L002S, U18-ch18
calib_packv5_042523_0143.root, FC#8, port C1
Entries 366
Mean 44.86
Std Dev 11.41
Turn on : 28.2032
Width : 3.324
Height : 10.065
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

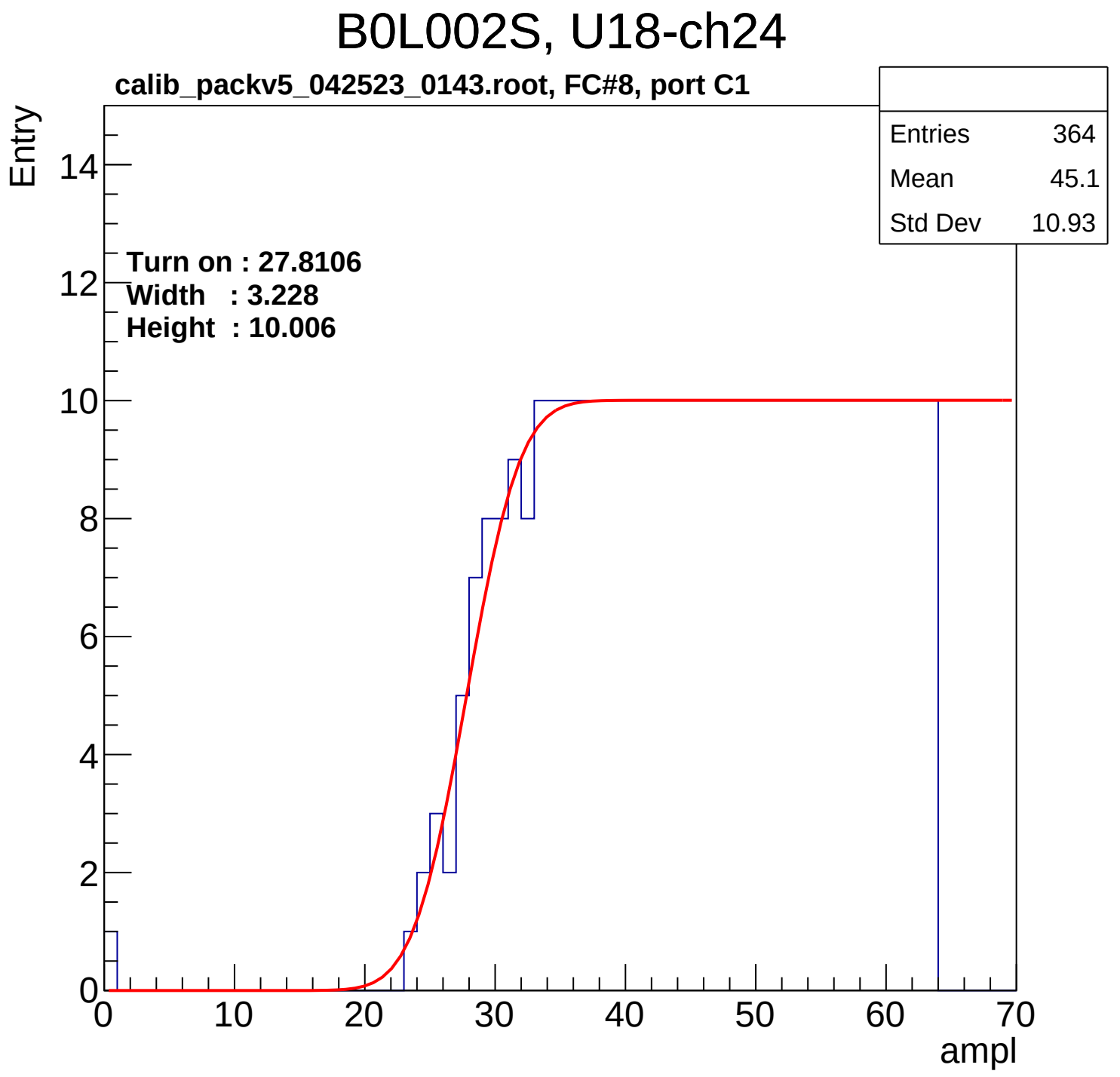

B0L002S, U18-ch19
calib_packv5_042523_0143.root, FC#8, port C1
Entries 364
Mean 44.99
Std Dev 11.29
Turn on : 27.8627
Width : 2.109
Height : 9.948
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

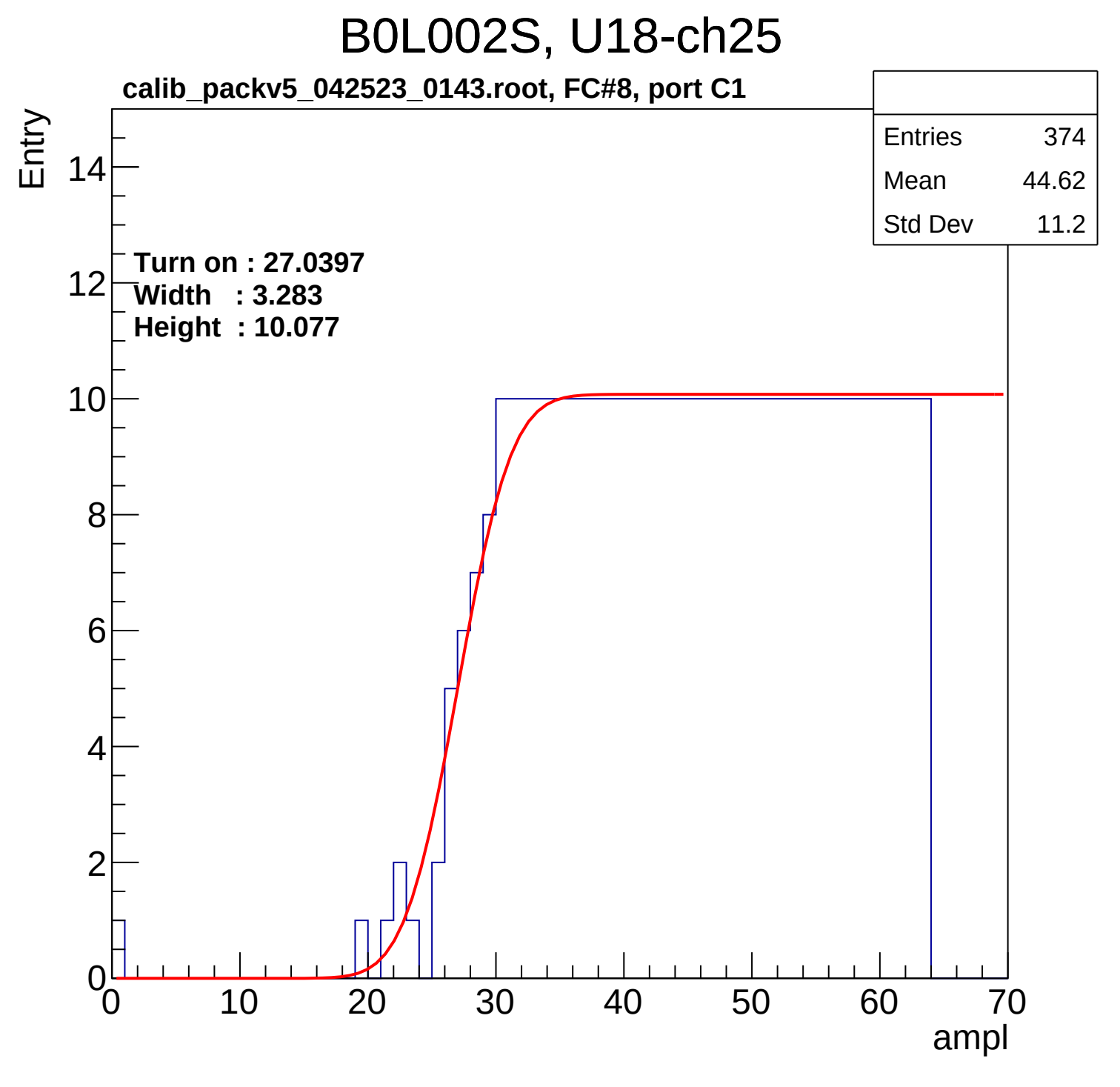

B0L002S, U18-ch20
calib_packv5_042523_0143.root, FC#8, port C1
Entries 367
Mean 44.87
Std Dev 11.23
Turn on : 27.4831
Width : 4.009
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

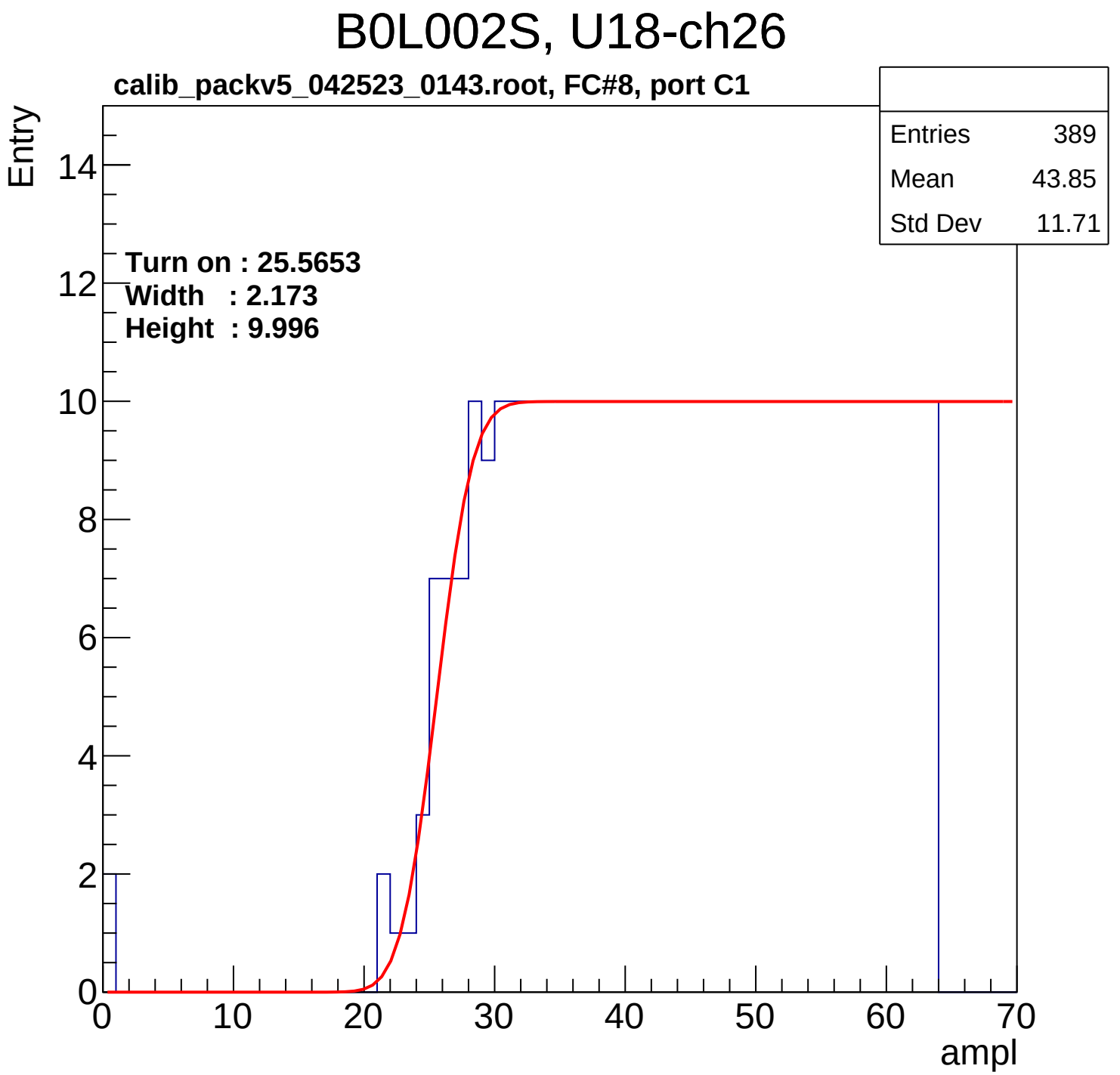

B0L002S, U18-ch21
calib_packv5_042523_0143.root, FC#8, port C1
Entries 381
Mean 44.14
Std Dev 11.72
Turn on : 26.3388
Width : 2.233
Height : 9.957
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

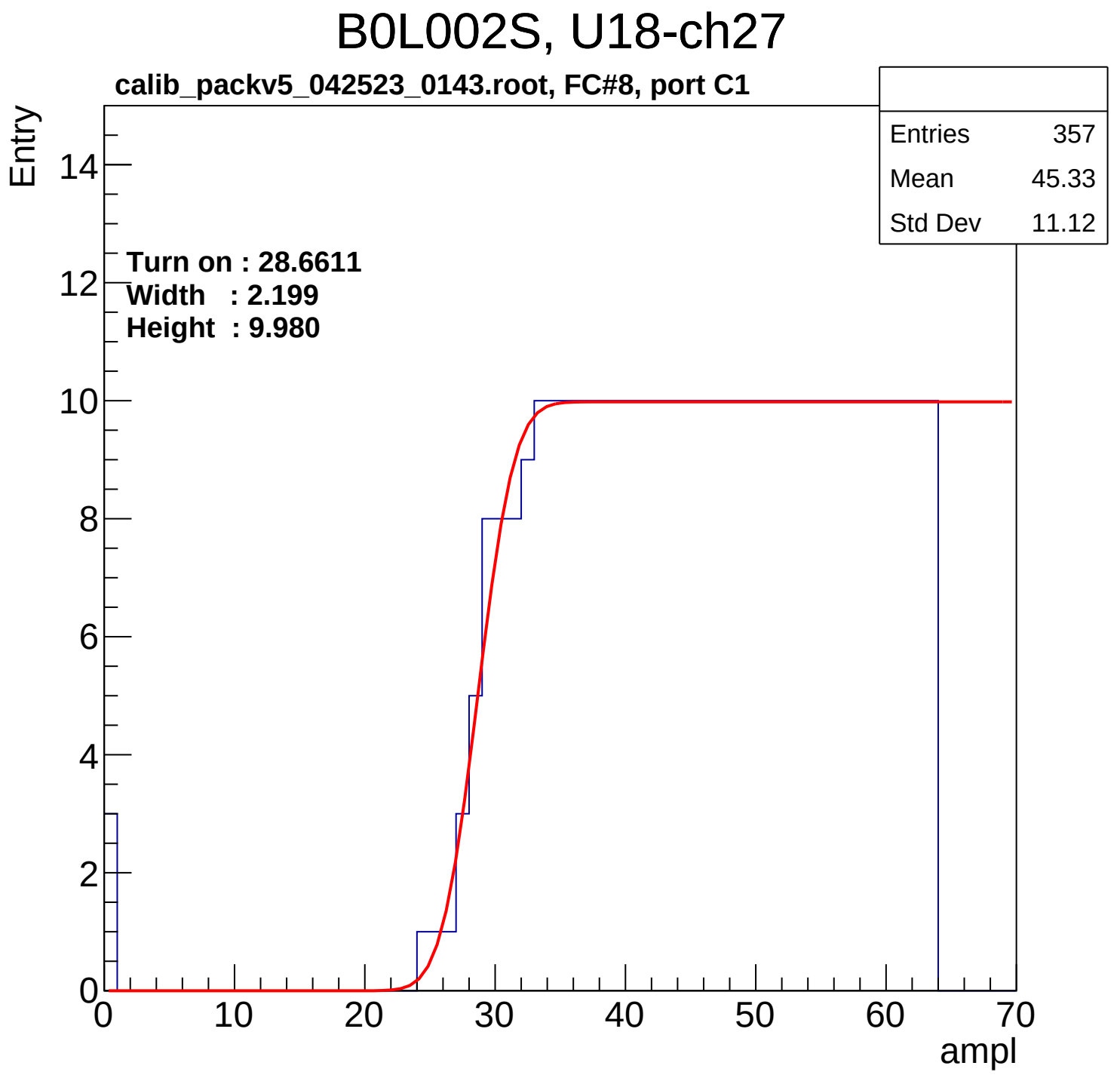

B0L002S, U18-ch22
calib_packv5_042523_0143.root, FC#8, port C1
Entries 367
Mean 44.78
Std Dev 11.53
Turn on : 27.7027
Width : 1.862
Height : 9.939
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

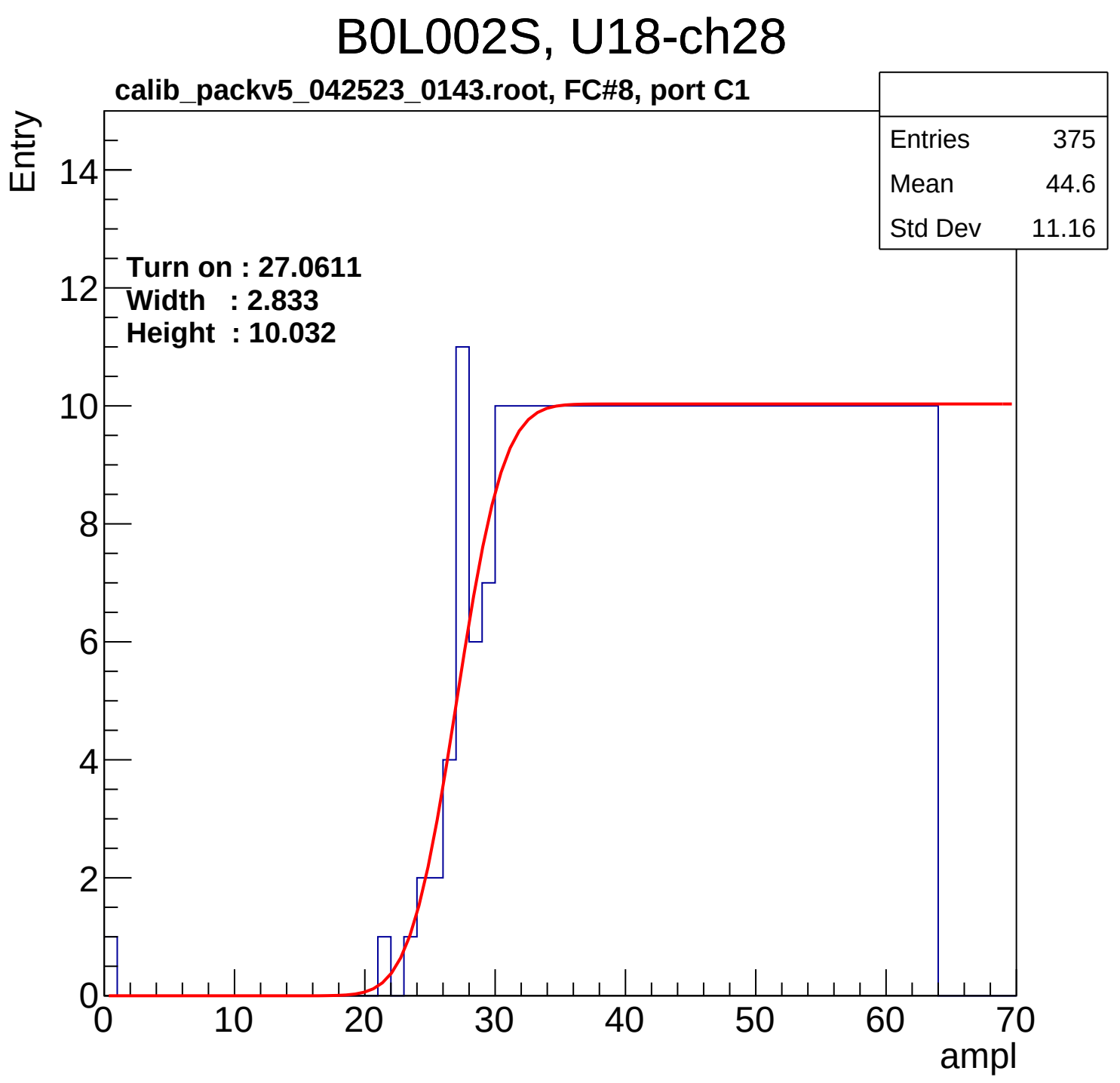

B0L002S, U18-ch23
calib_packv5_042523_0143.root, FC#8, port C1
Entries 374
Mean 44.48
Std Dev 11.56
Turn on : 27.0671
Width : 2.932
Height : 10.004
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

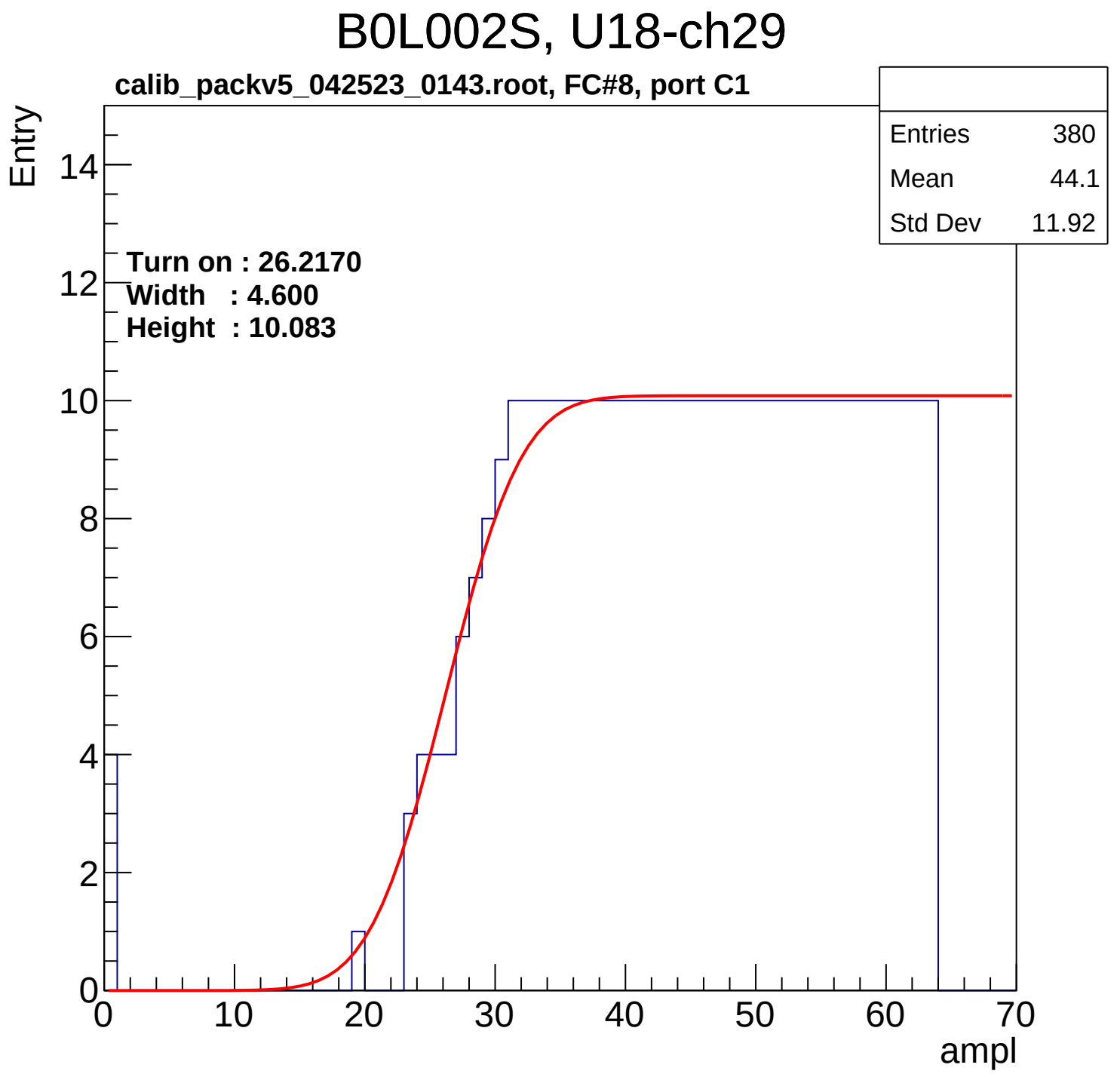

B0L002S, U18-ch24
calib_packv5_042523_0143.root, FC#8, port C1
Entries 364
Mean 45.1
Std Dev 10.93
Turn on : 27.8106
Width : 3.228
Height : 10.006
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

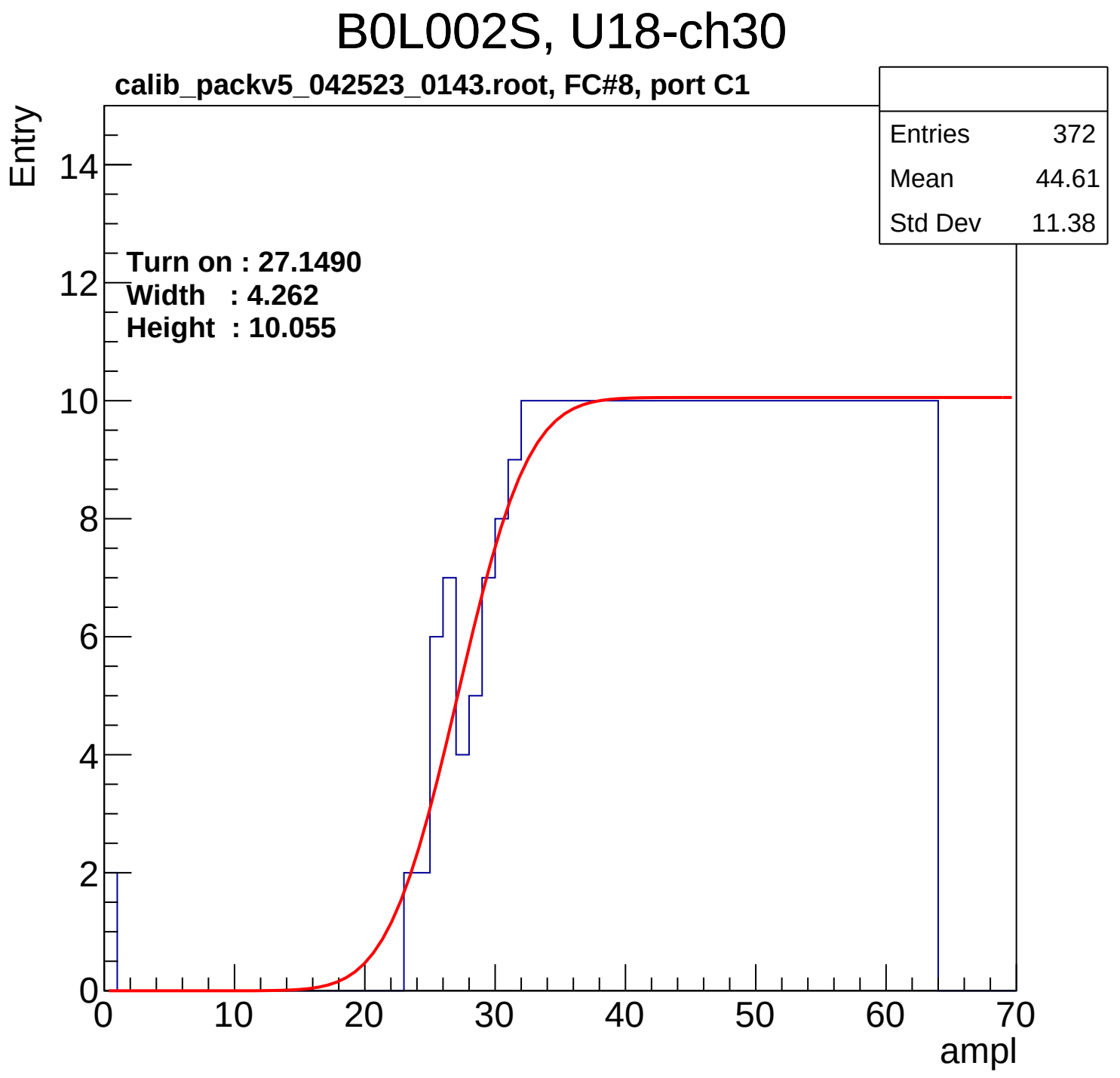

B0L002S, U18-ch25
calib_packv5_042523_0143.root, FC#8, port C1
Entries 374
Mean 44.62
Std Dev 11.2
Turn on : 27.0397
Width : 3.283
Height : 10.077
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

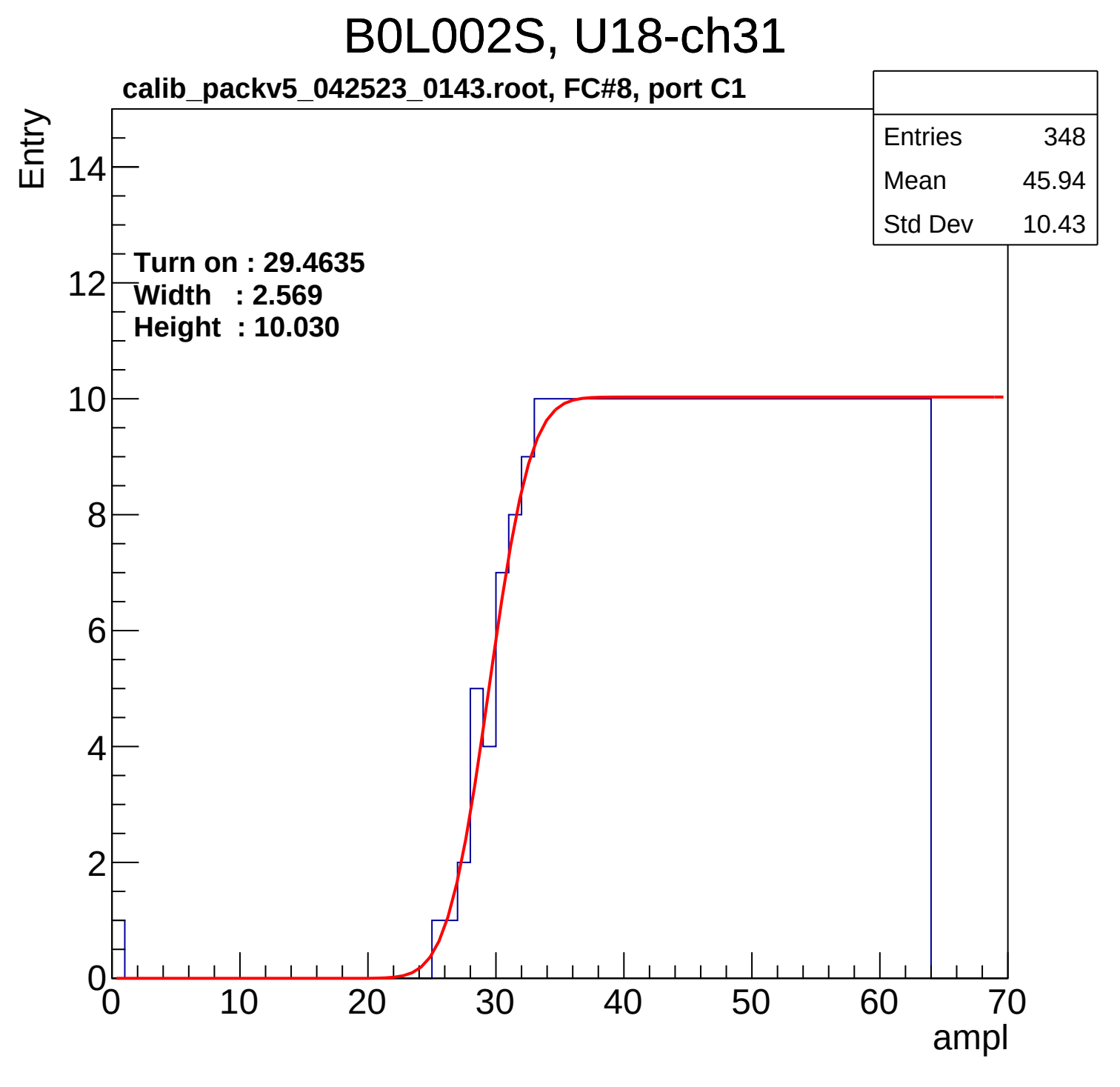

B0L002S, U18-ch26
calib_packv5_042523_0143.root, FC#8, port C1
Entries 389
Mean 43.85
Std Dev 11.71
Turn on : 25.5653
Width : 2.173
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

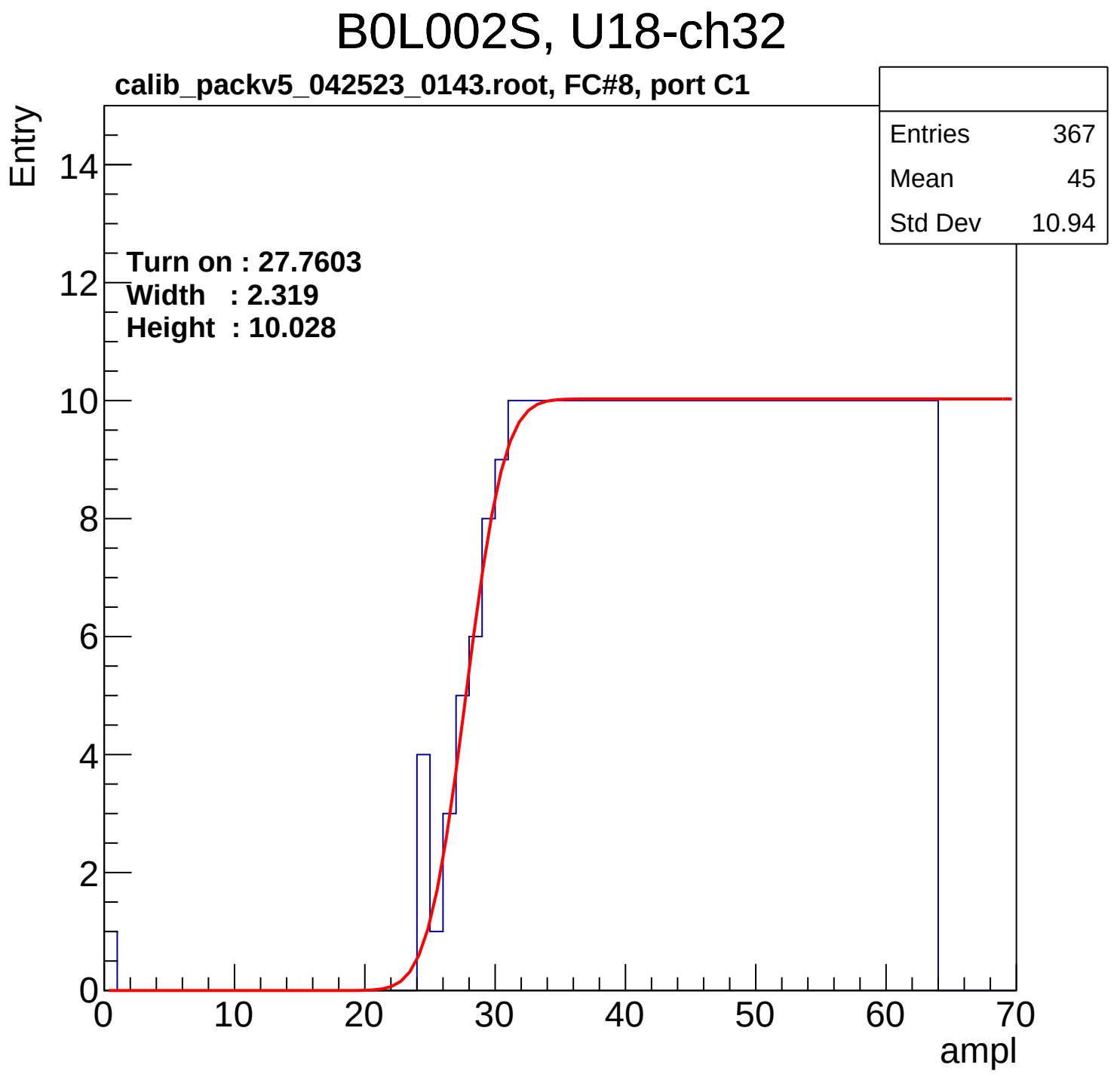

B0L002S, U18-ch27
calib_packv5_042523_0143.root, FC#8, port C1
Entries 357
Mean 45.33
Std Dev 11.12
Turn on : 28.6611
Width : 2.199
Height : 9.980
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

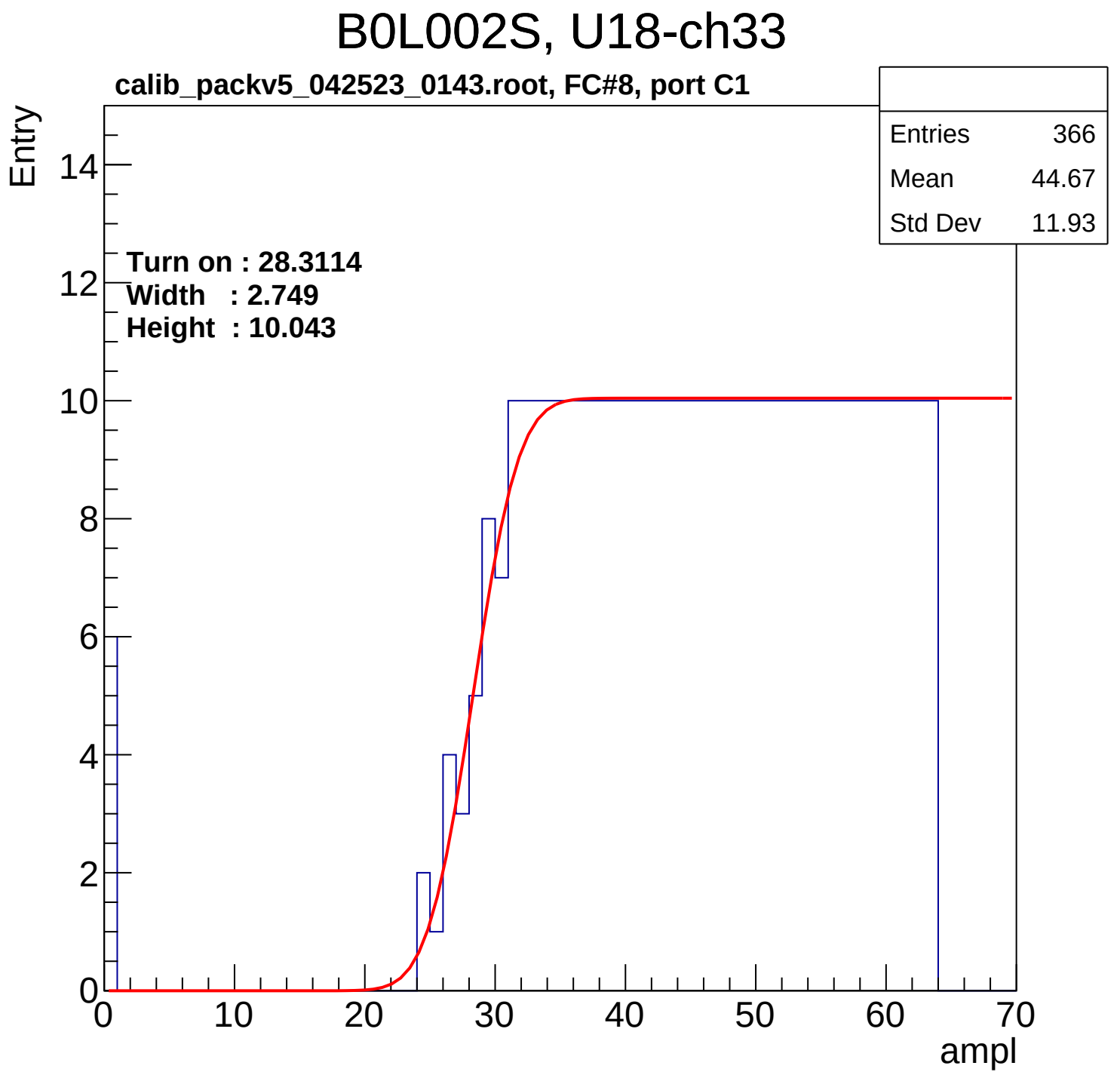

B0L002S, U18-ch28
calib_packv5_042523_0143.root, FC#8, port C1
Entries 375
Mean 44.6
Std Dev 11.16
Turn on : 27.0611
Width : 2.833
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

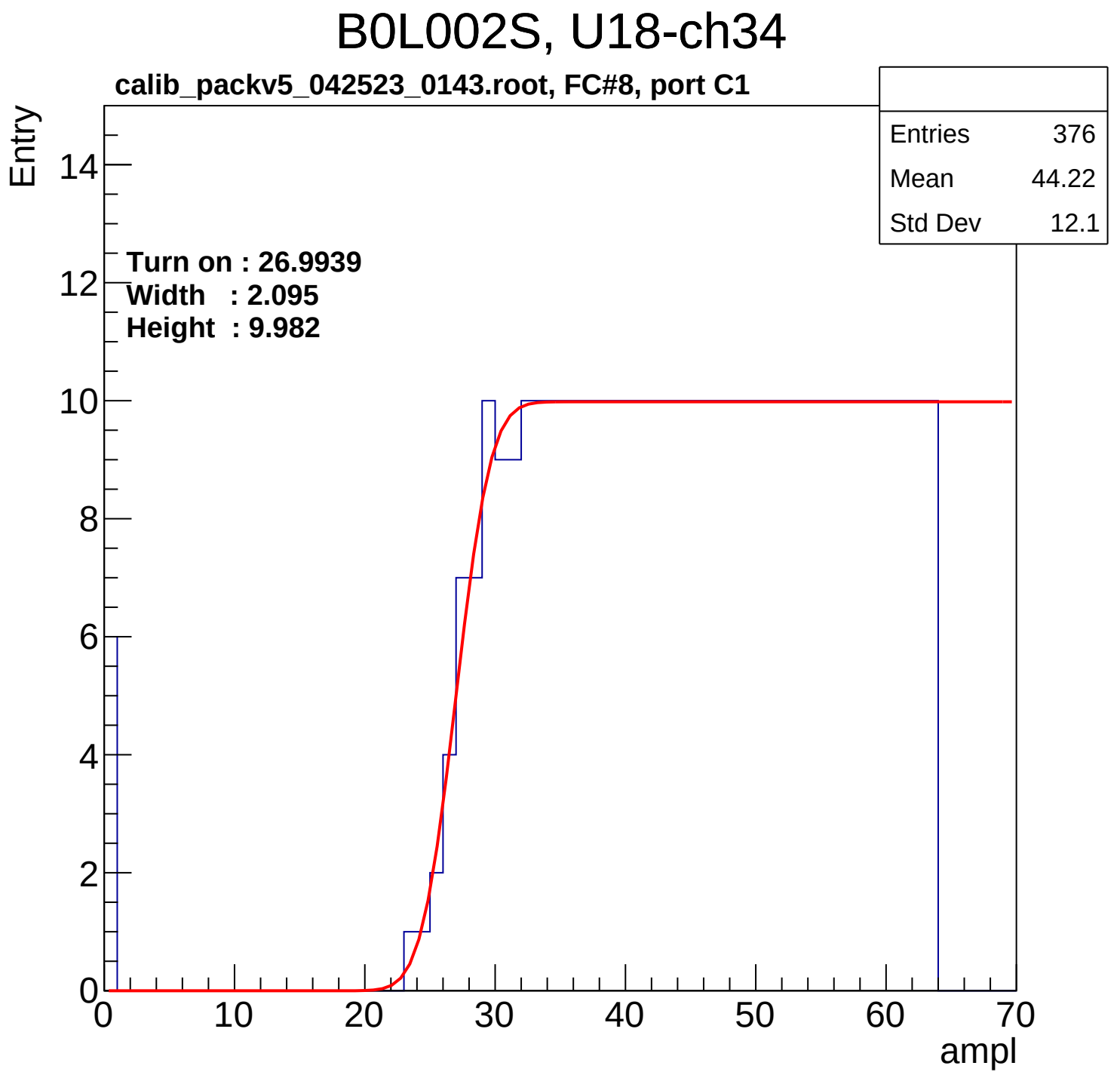

B0L002S, U18-ch29
calib_packv5_042523_0143.root, FC#8, port C1
Entries 380
Mean 44.1
Std Dev 11.92
Turn on : 26.2170
Width : 4.600
Height : 10.083
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

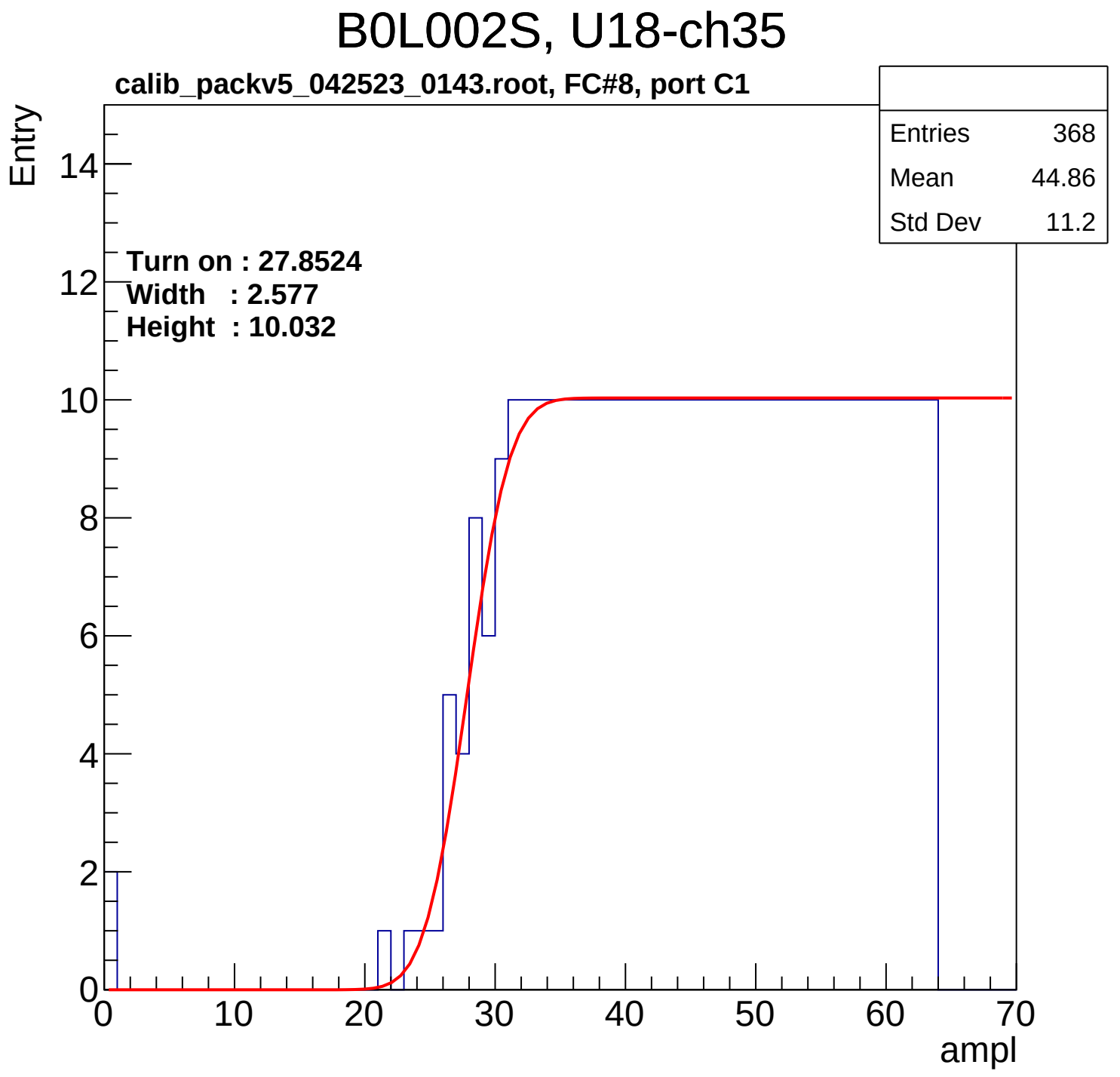

B0L002S, U18-ch30
calib_packv5_042523_0143.root, FC#8, port C1
Entries 372
Mean 44.61
Std Dev 11.38
Turn on : 27.1490
Width : 4.262
Height : 10.055
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

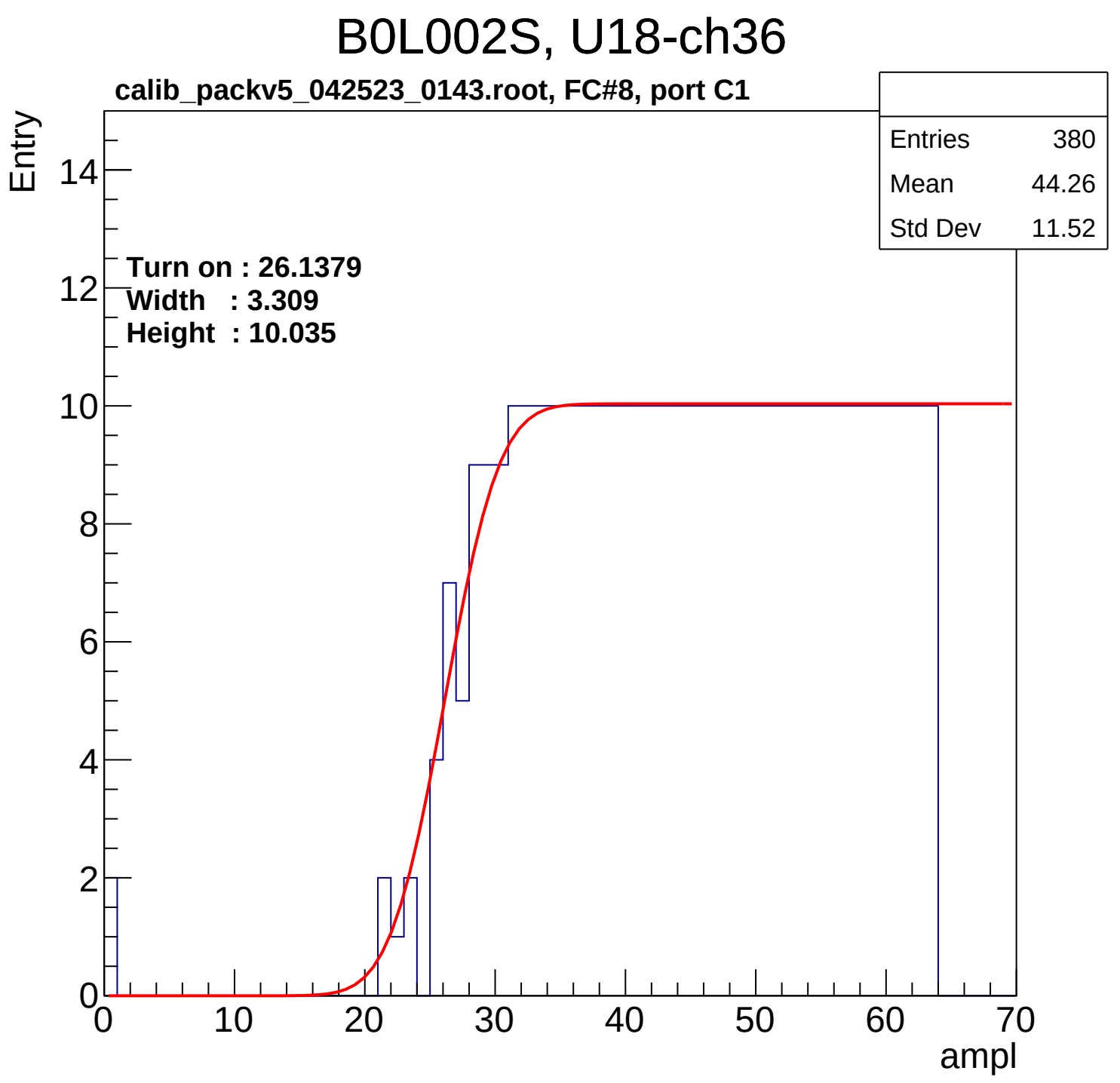

B0L002S, U18-ch31
calib_packv5_042523_0143.root, FC#8, port C1
Entries 348
Mean 45.94
Std Dev 10.43
Turn on : 29.4635
Width : 2.569
Height : 10.030
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

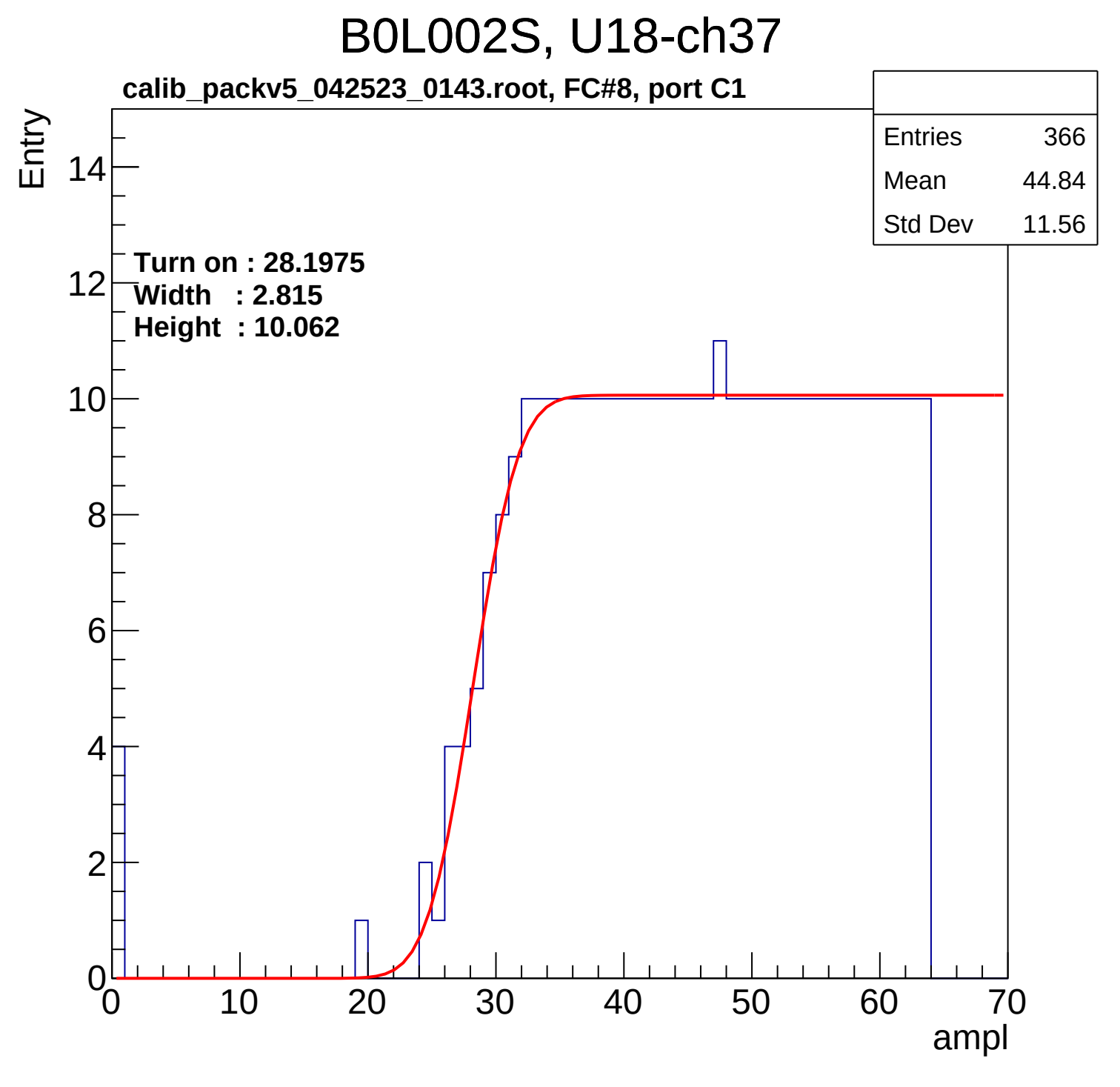

B0L002S, U18-ch32
calib_packv5_042523_0143.root, FC#8, port C1
Entries 367
Mean 45
Std Dev 10.94
Turn on : 27.7603
Width : 2.319
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

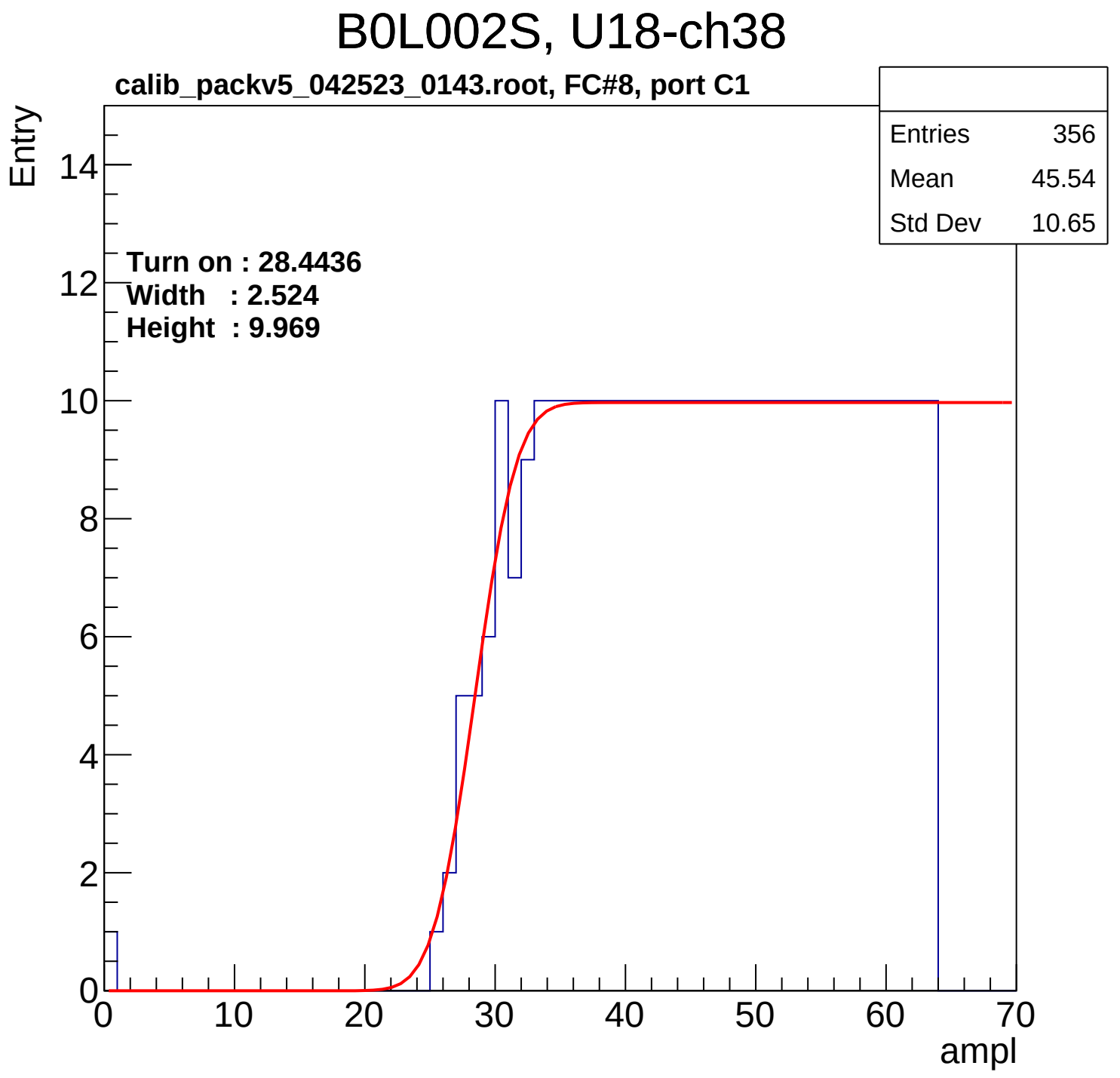

B0L002S, U18-ch33
calib_packv5_042523_0143.root, FC#8, port C1
Entries 366
Mean 44.67
Std Dev 11.93
Turn on : 28.3114
Width : 2.749
Height : 10.043
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

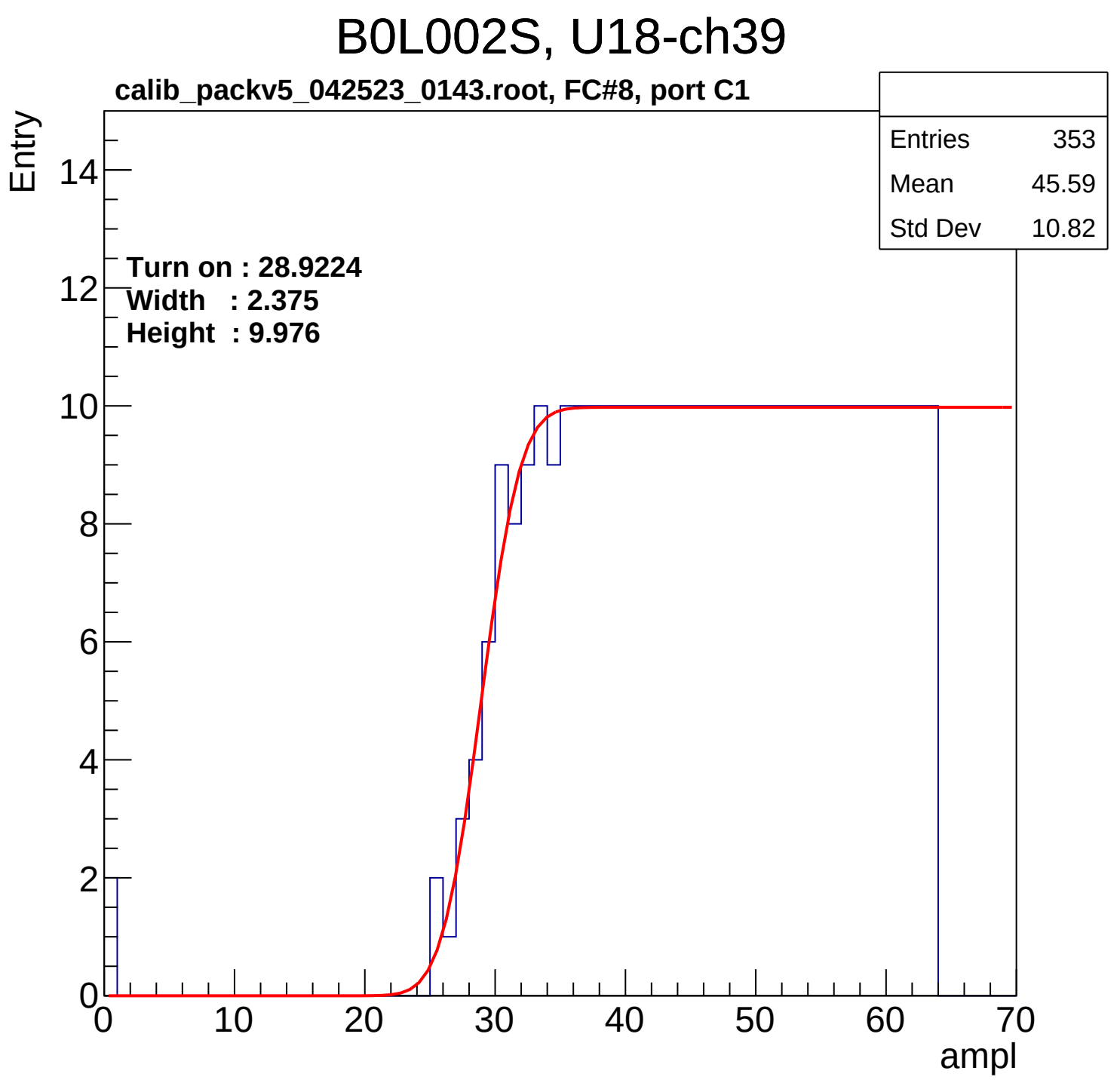

B0L002S, U18-ch34
calib_packv5_042523_0143.root, FC#8, port C1
Entries 376
Mean 44.22
Std Dev 12.1
Turn on : 26.9939
Width : 2.095
Height : 9.982
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

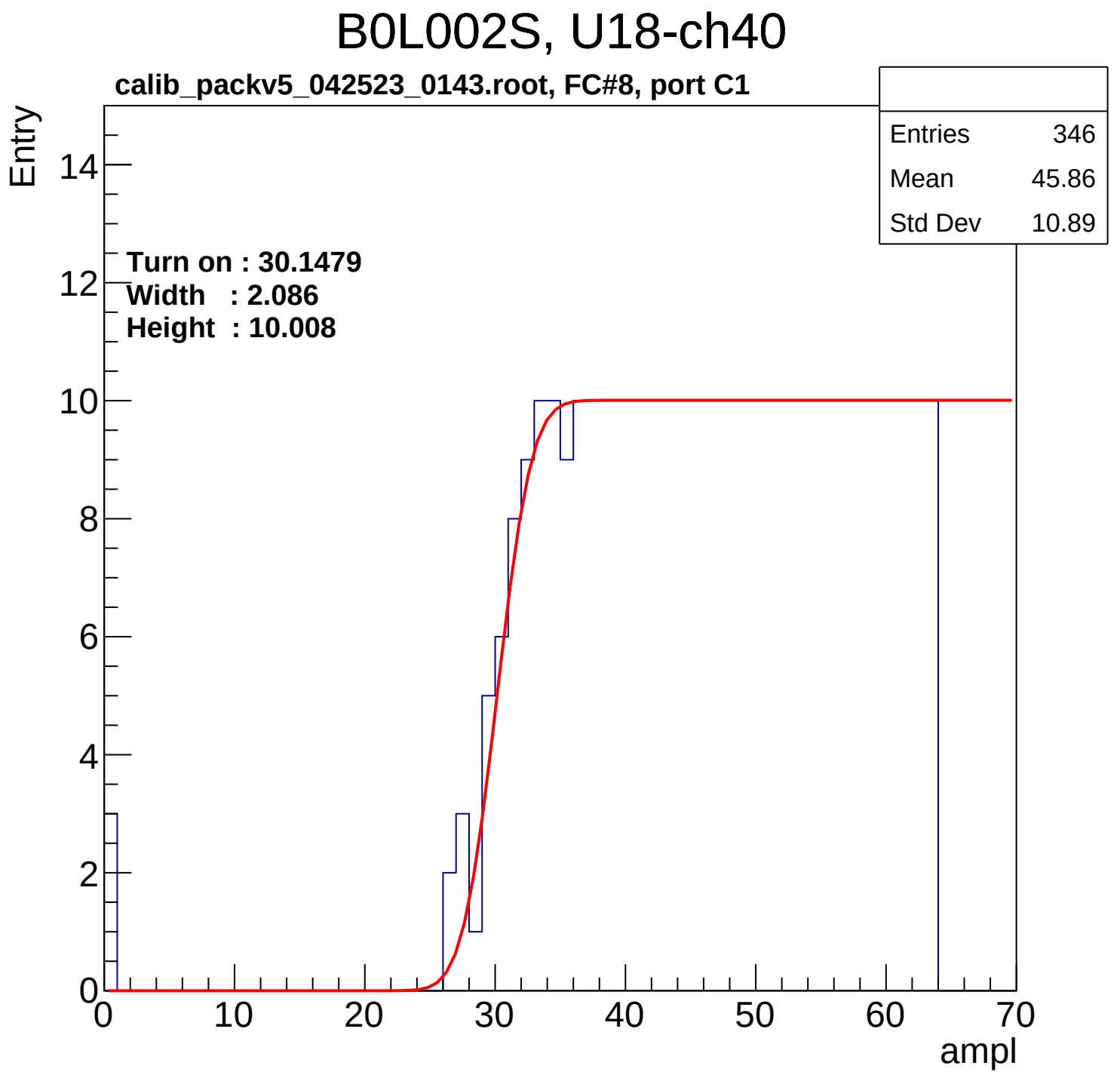

B0L002S, U18-ch35
calib_packv5_042523_0143.root, FC#8, port C1
Entries 368
Mean 44.86
Std Dev 11.2
Turn on : 27.8524
Width : 2.577
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

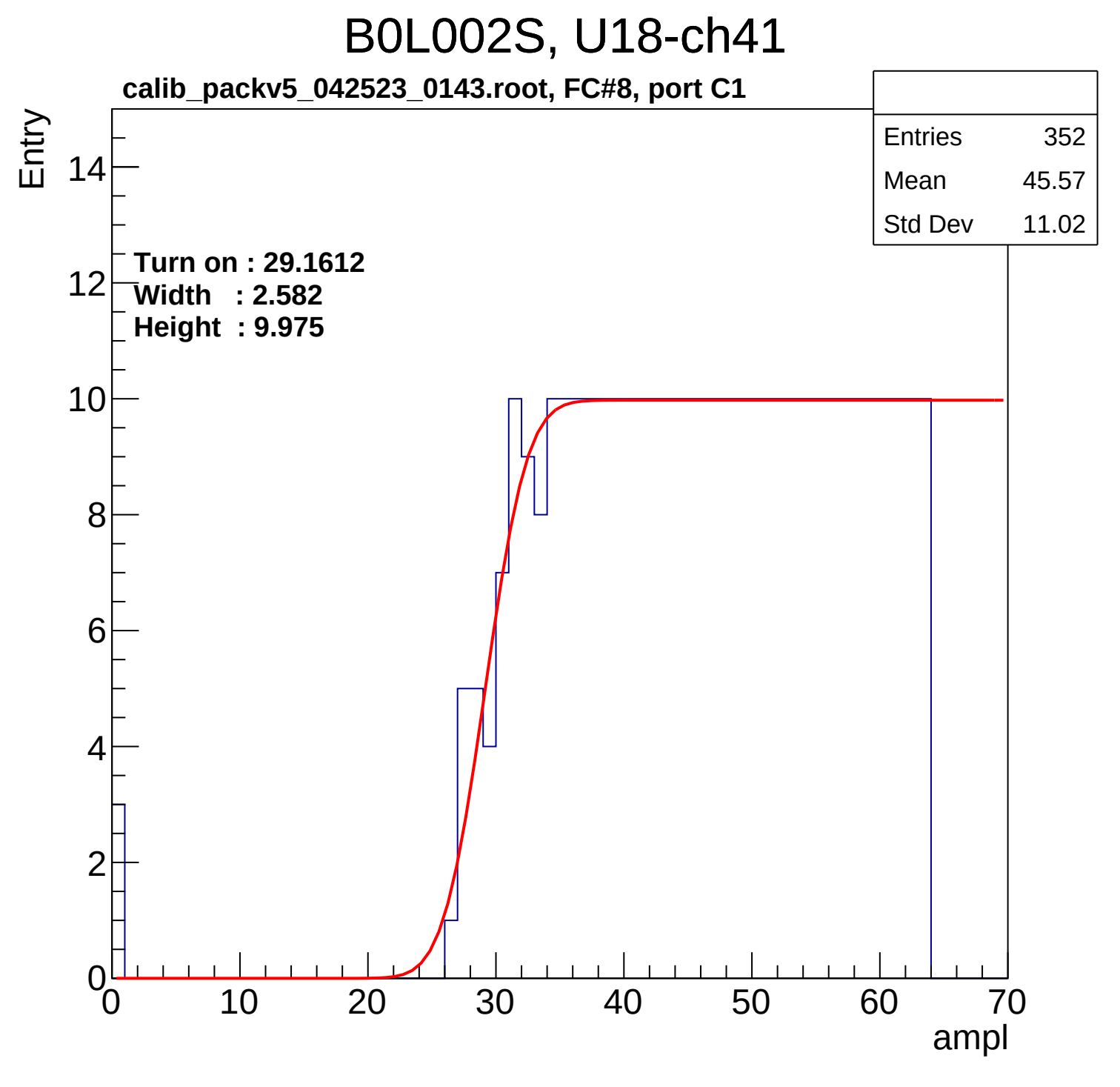

B0L002S, U18-ch36
calib_packv5_042523_0143.root, FC#8, port C1
Entries 380
Mean 44.26
Std Dev 11.52
Turn on : 26.1379
Width : 3.309
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

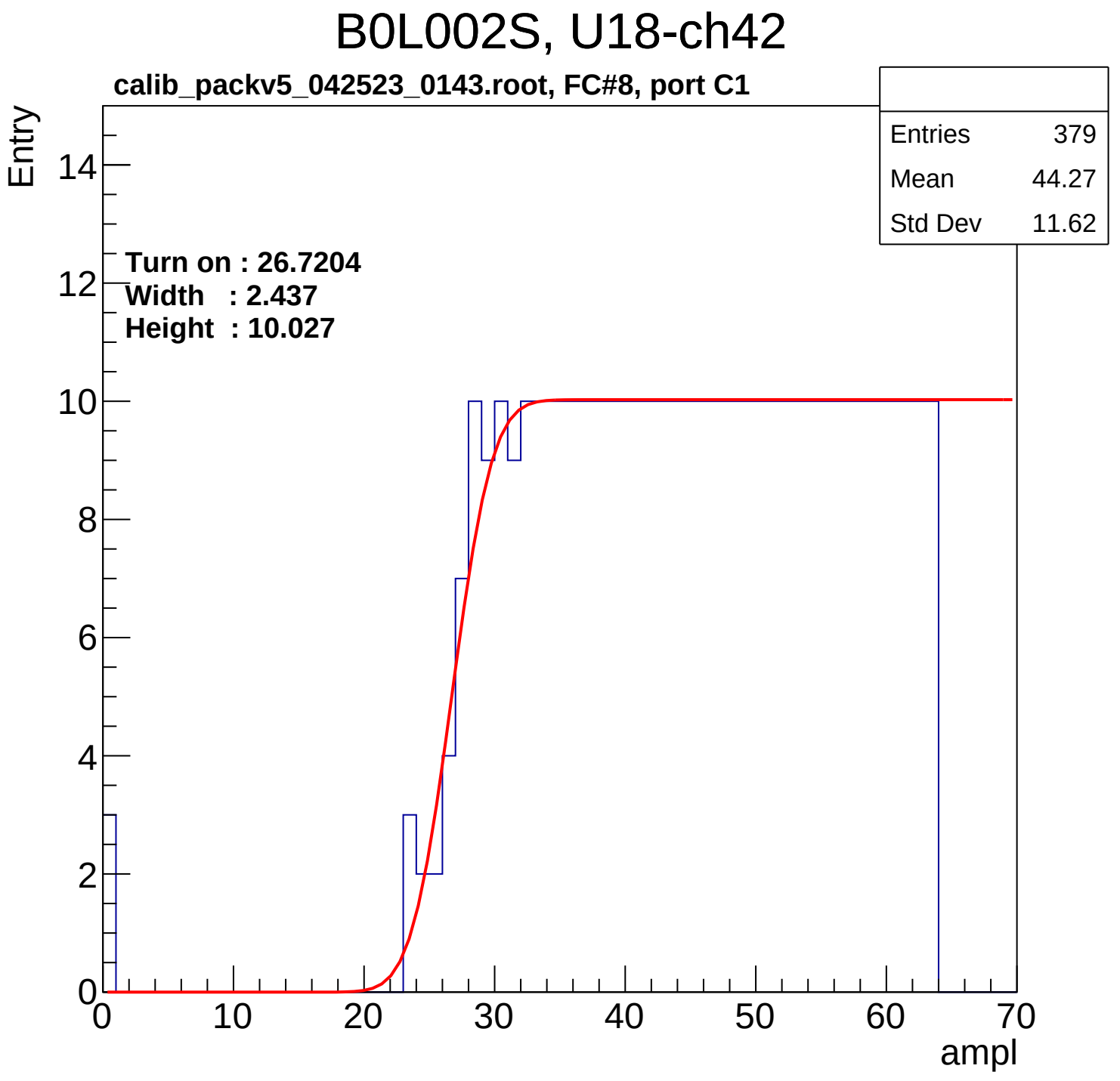

B0L002S, U18-ch37
calib_packv5_042523_0143.root, FC#8, port C1
Entries 366
Mean 44.84
Std Dev 11.56
Turn on : 28.1975
Width : 2.815
Height : 10.062
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

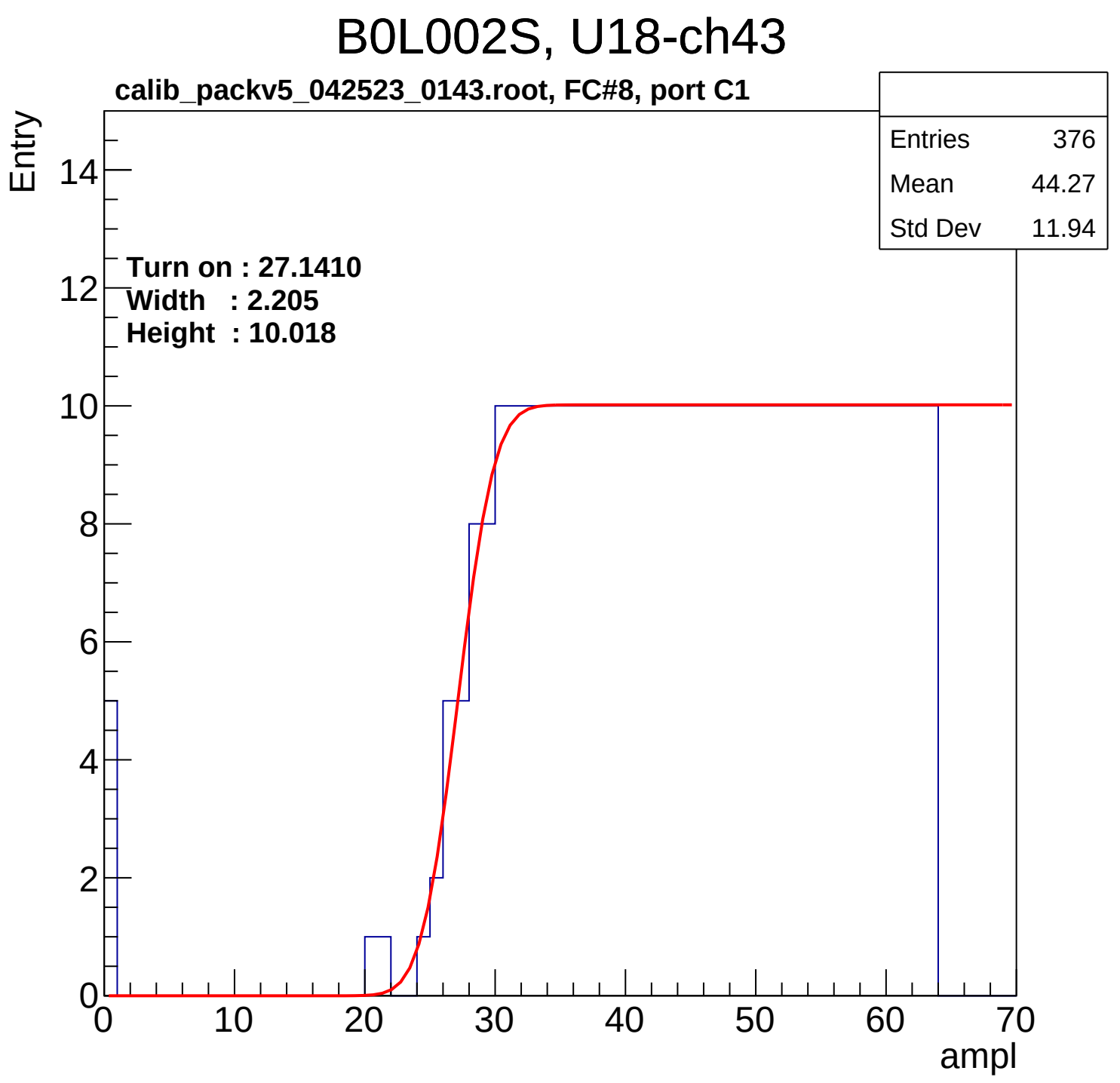

B0L002S, U18-ch38
calib_packv5_042523_0143.root, FC#8, port C1
Entries 356
Mean 45.54
Std Dev 10.65
Turn on : 28.4436
Width : 2.524
Height : 9.969
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

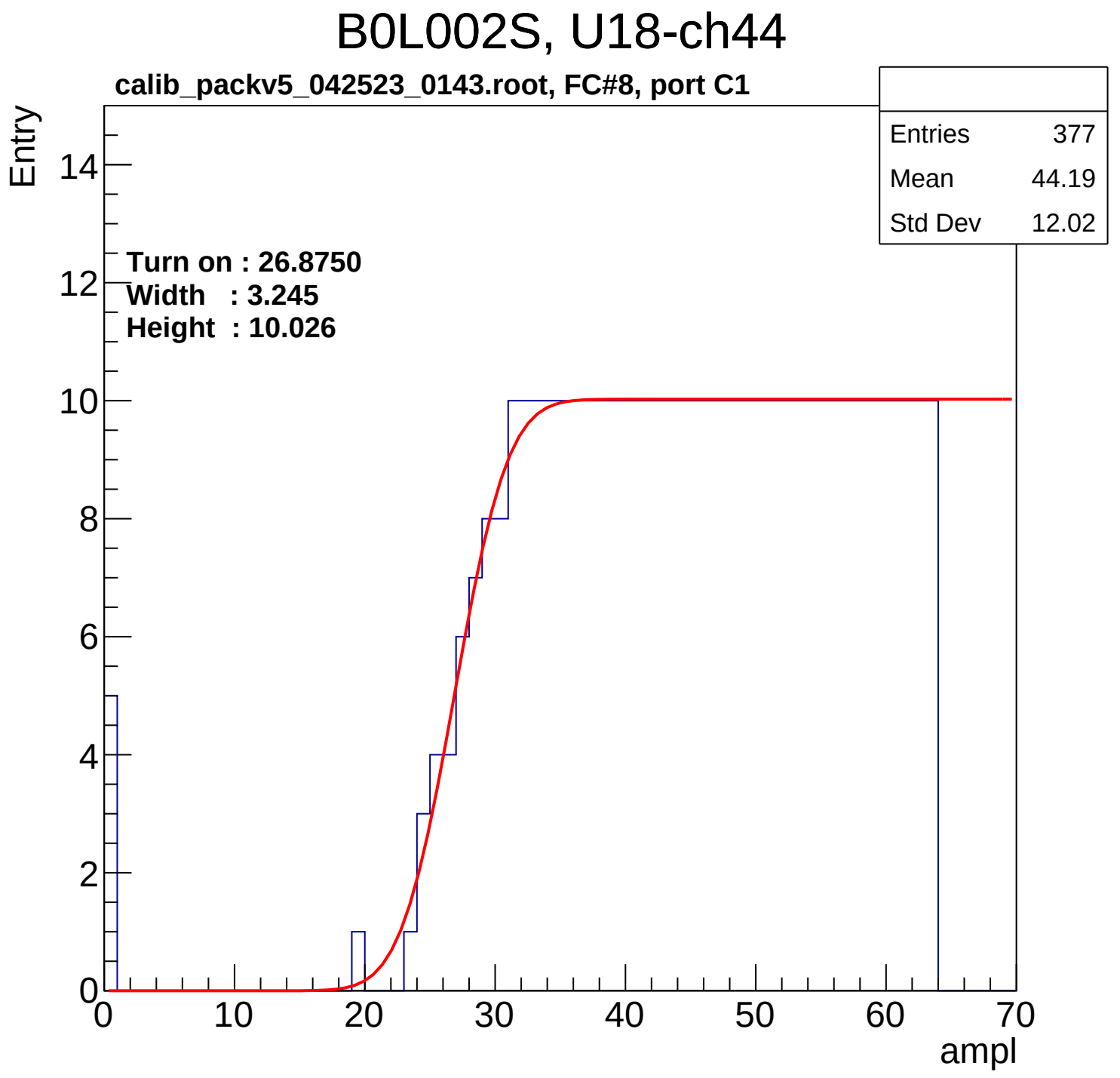

B0L002S, U18-ch39
calib_packv5_042523_0143.root, FC#8, port C1
Entries 353
Mean 45.59
Std Dev 10.82
Turn on : 28.9224
Width : 2.375
Height : 9.976
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

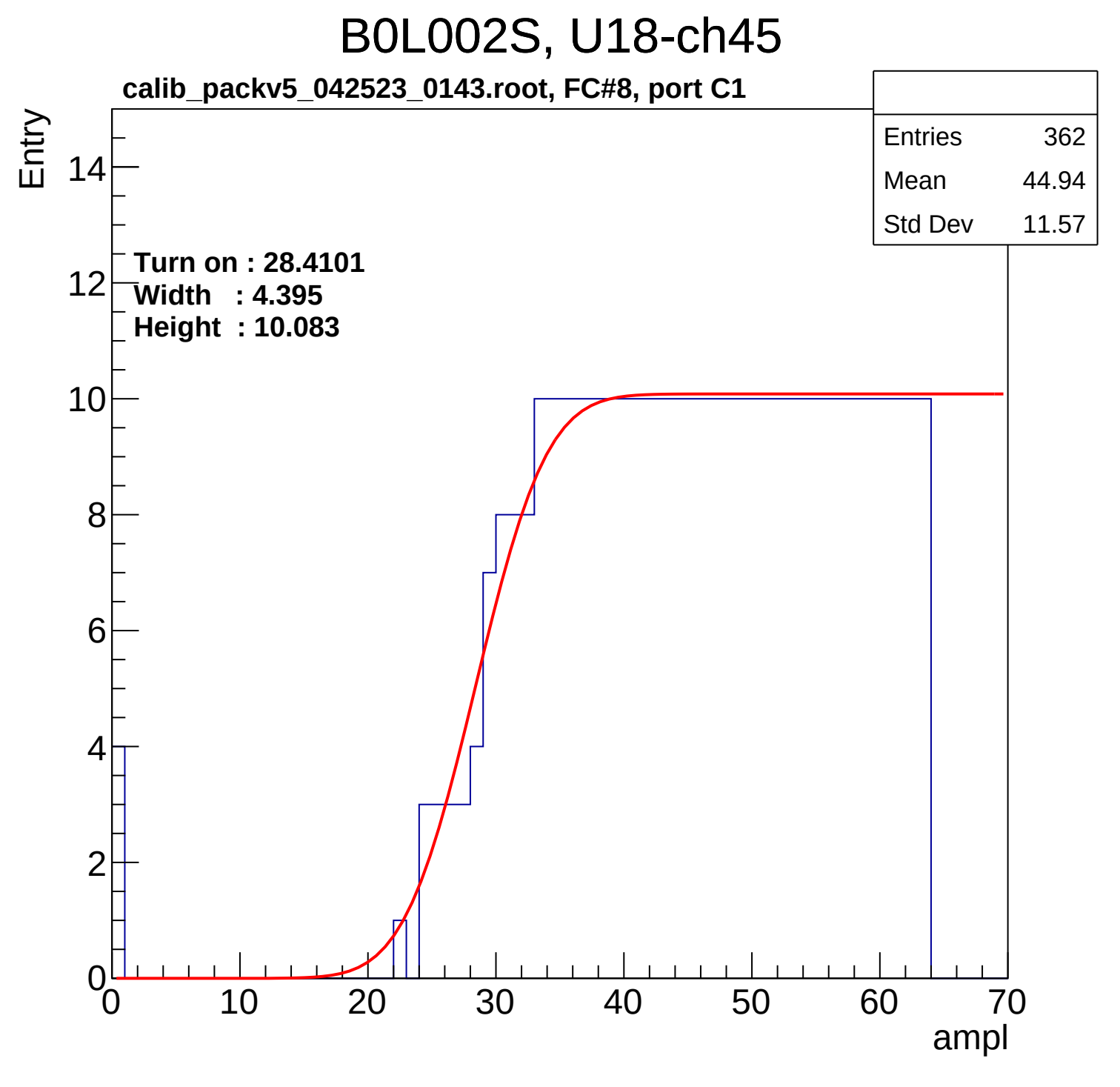

B0L002S, U18-ch40
calib_packv5_042523_0143.root, FC#8, port C1
Entries 346
Mean 45.86
Std Dev 10.89
Turn on : 30.1479
Width : 2.086
Height : 10.008
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

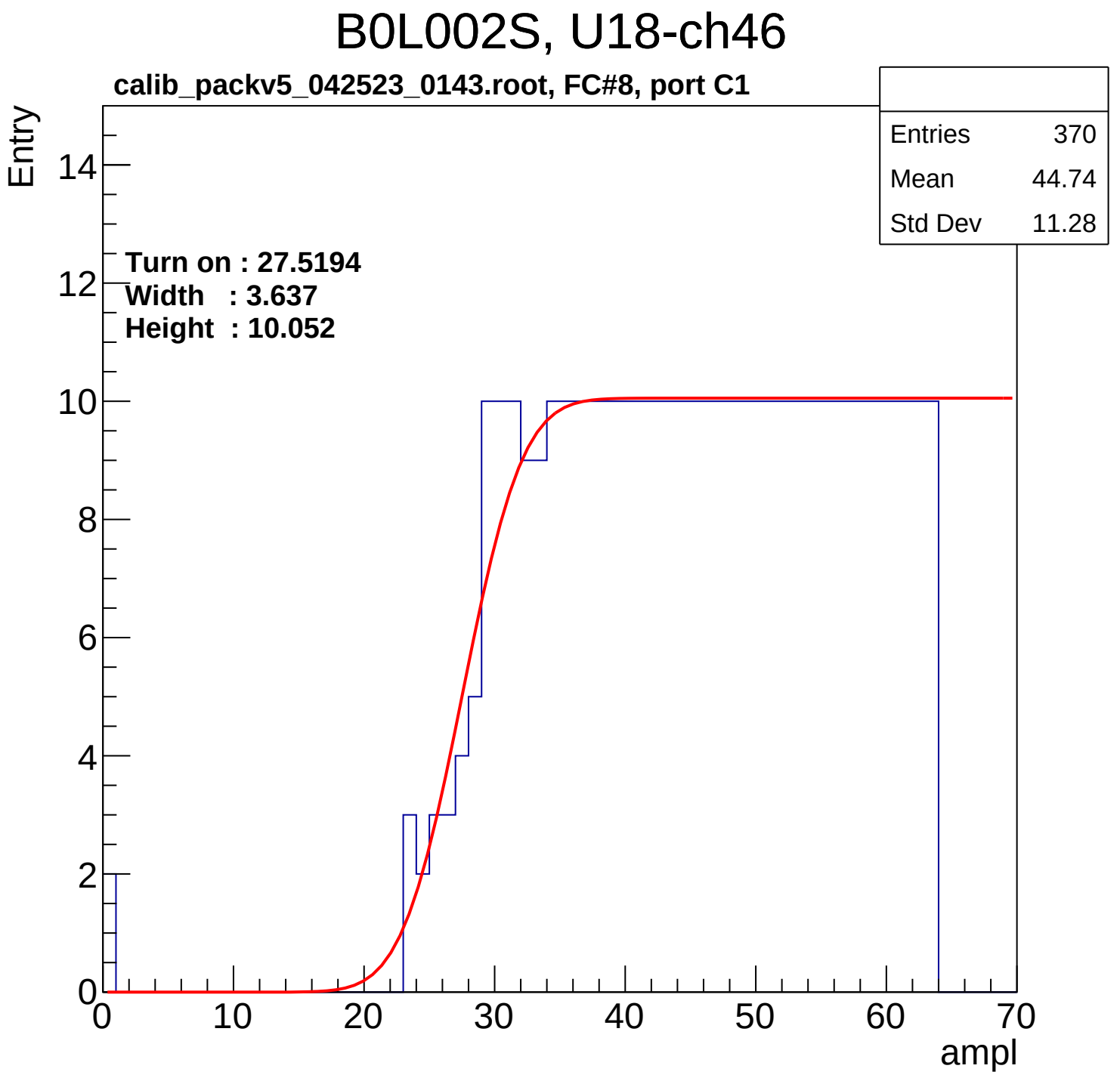

B0L002S, U18-ch41
calib_packv5_042523_0143.root, FC#8, port C1
Entries 352
Mean 45.57
Std Dev 11.02
Turn on : 29.1612
Width : 2.582
Height : 9.975
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

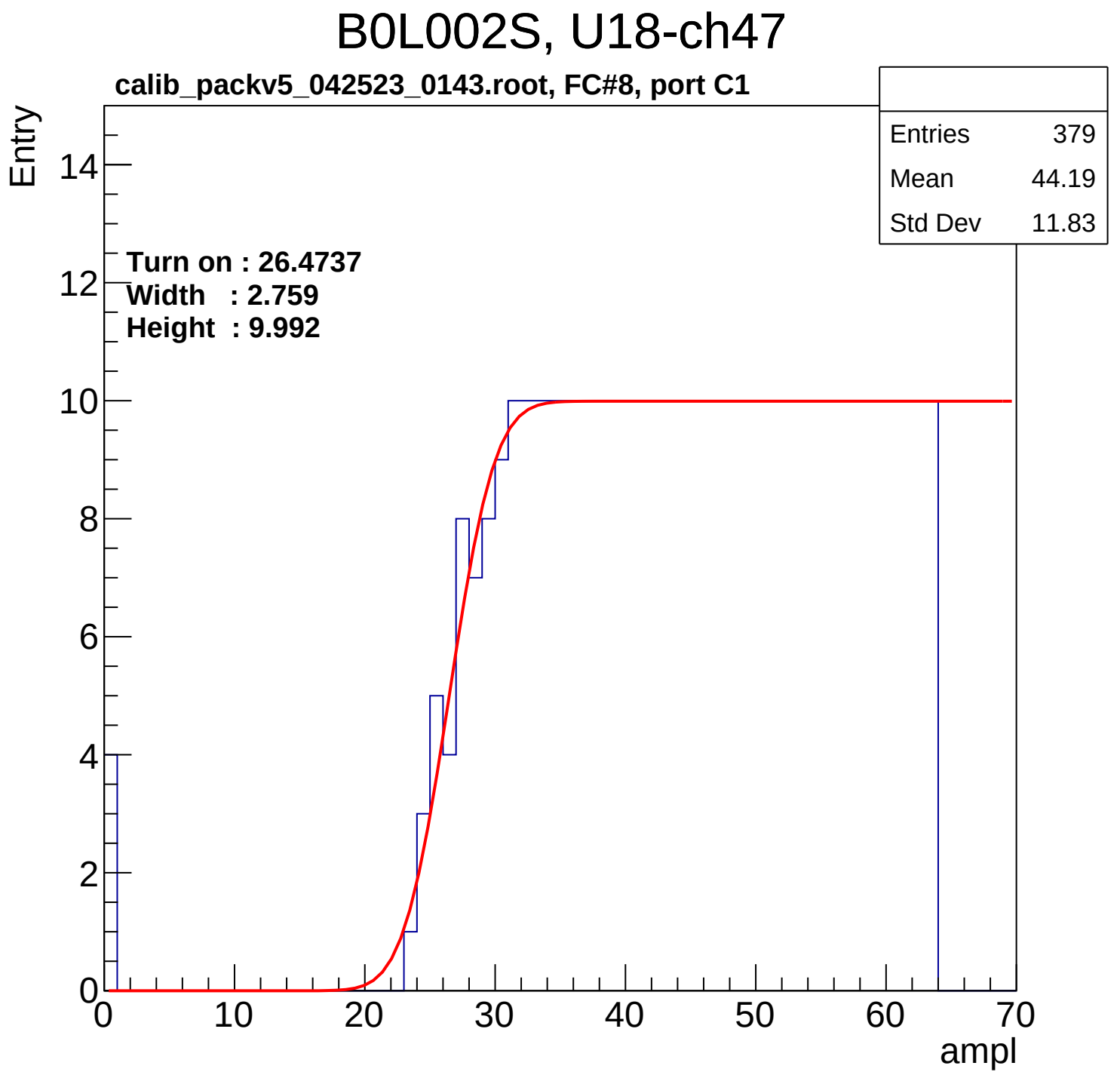

B0L002S, U18-ch42
calib_packv5_042523_0143.root, FC#8, port C1
Entries 379
Mean 44.27
Std Dev 11.62
Turn on : 26.7204
Width : 2.437
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

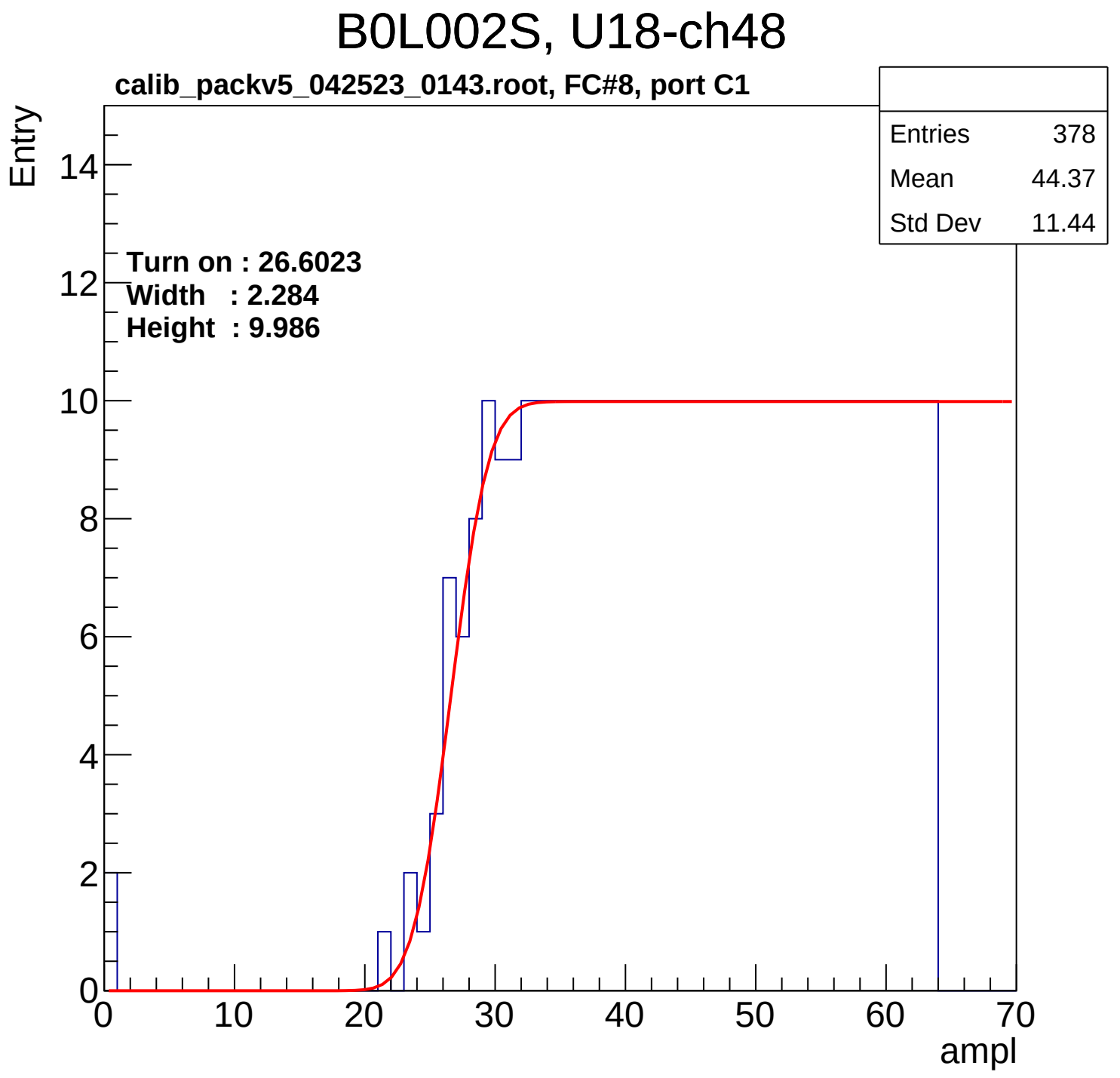

B0L002S, U18-ch43
calib_packv5_042523_0143.root, FC#8, port C1
Entries 376
Mean 44.27
Std Dev 11.94
Turn on : 27.1410
Width : 2.205
Height : 10.018
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

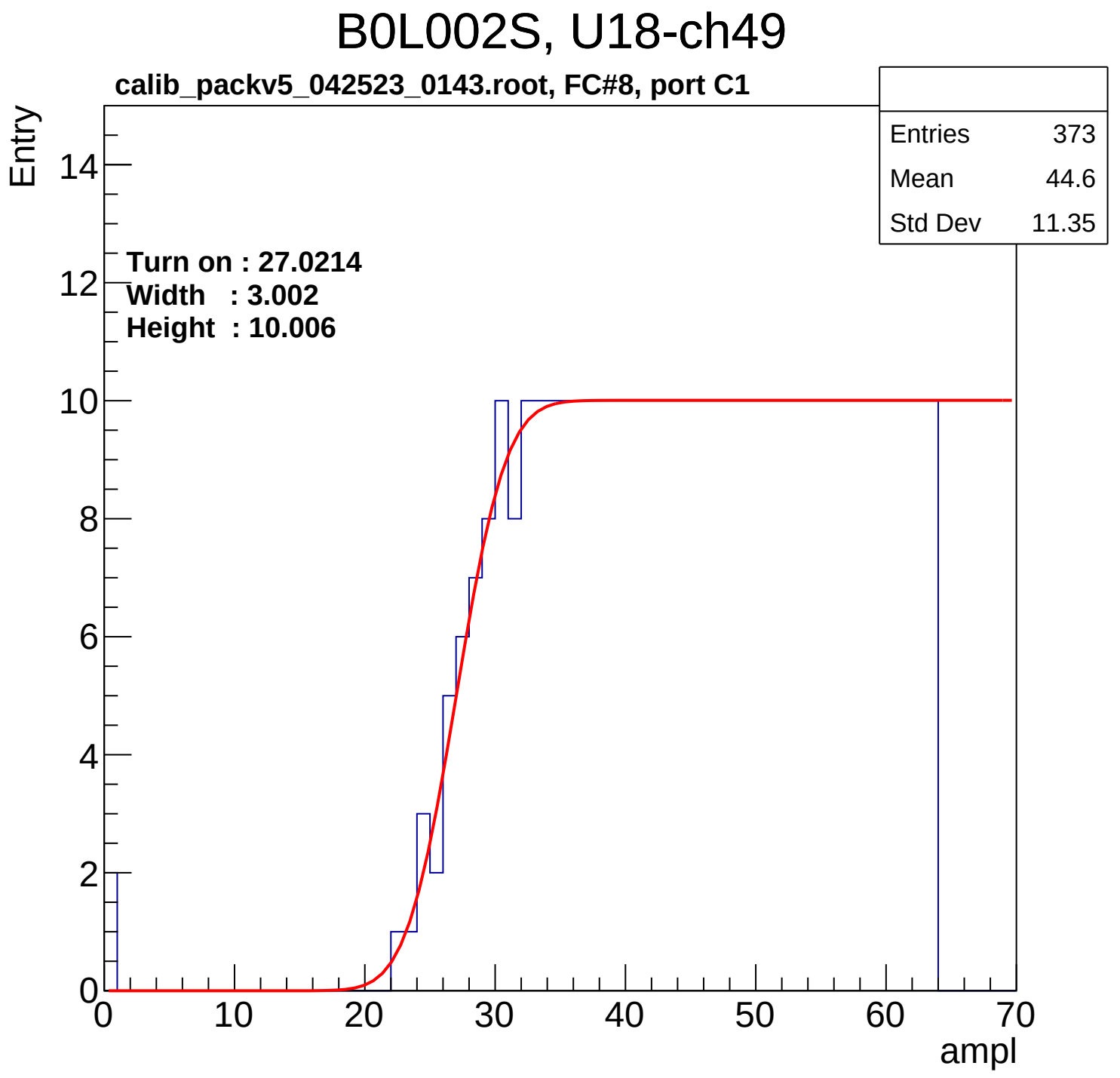

B0L002S, U18-ch44
calib_packv5_042523_0143.root, FC#8, port C1
Entries 377
Mean 44.19
Std Dev 12.02
Turn on : 26.8750
Width : 3.245
Height : 10.026
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

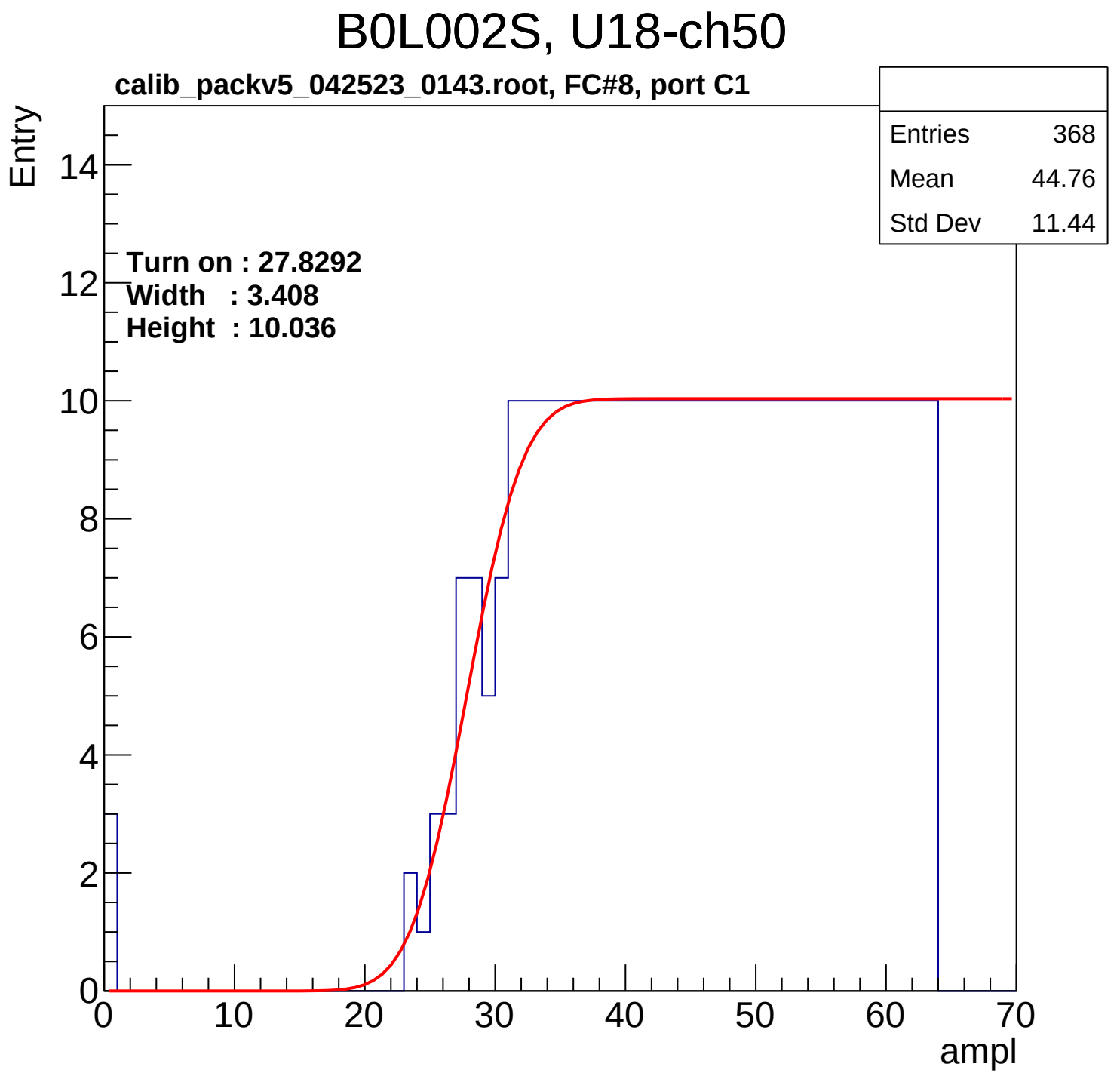

B0L002S, U18-ch45
calib_packv5_042523_0143.root, FC#8, port C1
Entries 362
Mean 44.94
Std Dev 11.57
Turn on : 28.4101
Width : 4.395
Height : 10.083
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

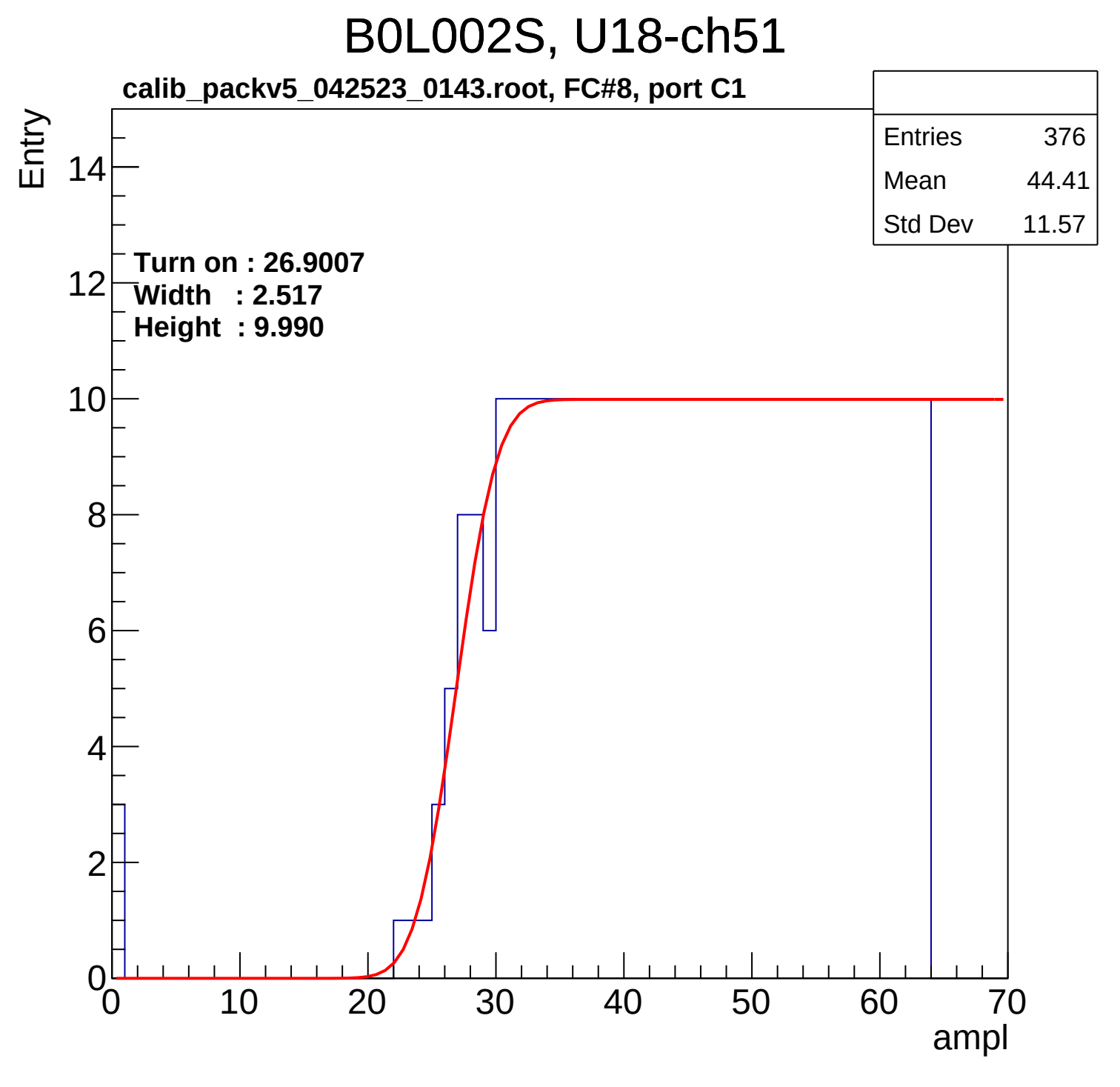

B0L002S, U18-ch46
calib_packv5_042523_0143.root, FC#8, port C1
Entries 370
Mean 44.74
Std Dev 11.28
Turn on : 27.5194
Width : 3.637
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

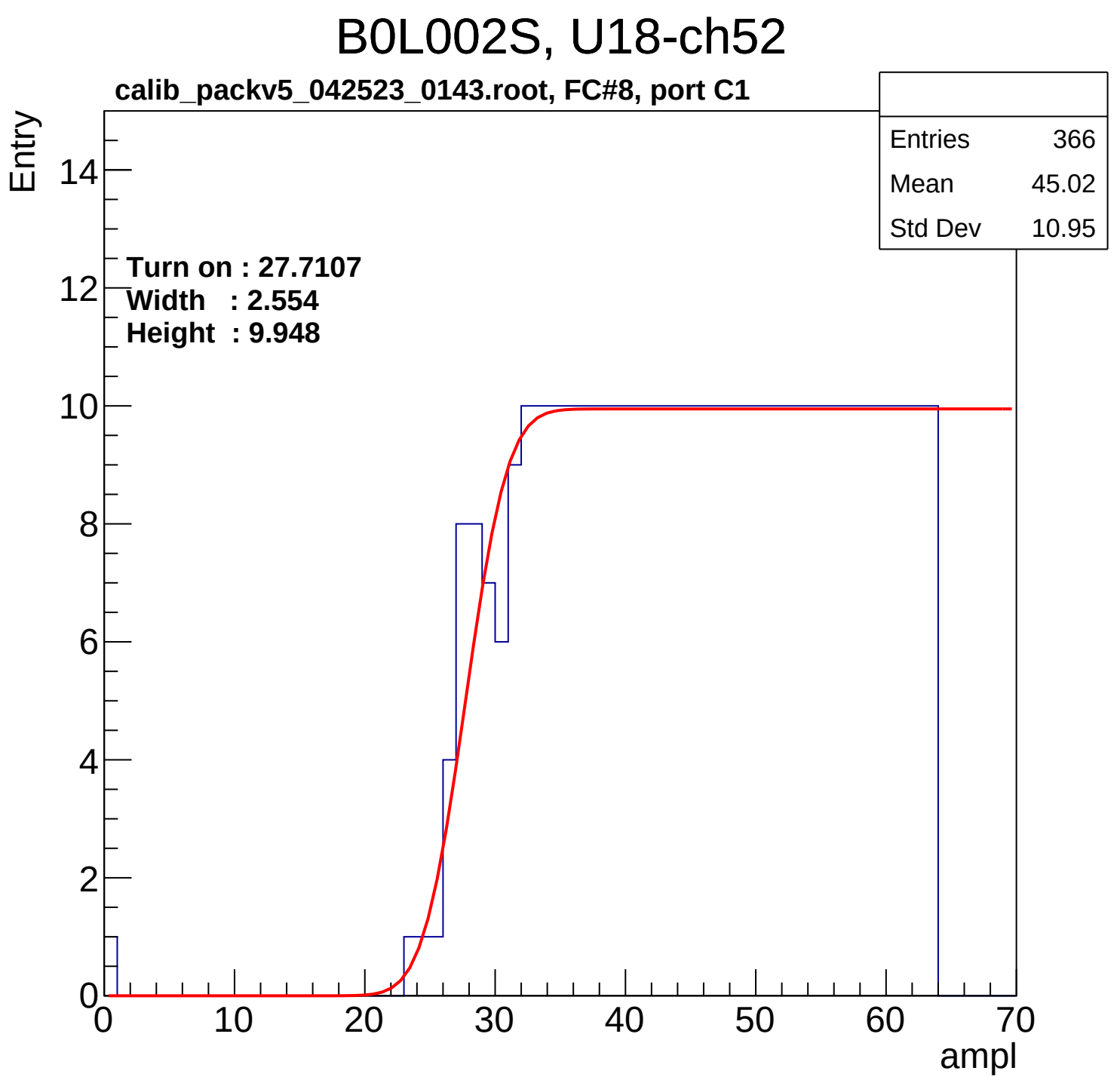

B0L002S, U18-ch47
calib_packv5_042523_0143.root, FC#8, port C1
Entries 379
Mean 44.19
Std Dev 11.83
Turn on : 26.4737
Width : 2.759
Height : 9.992
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

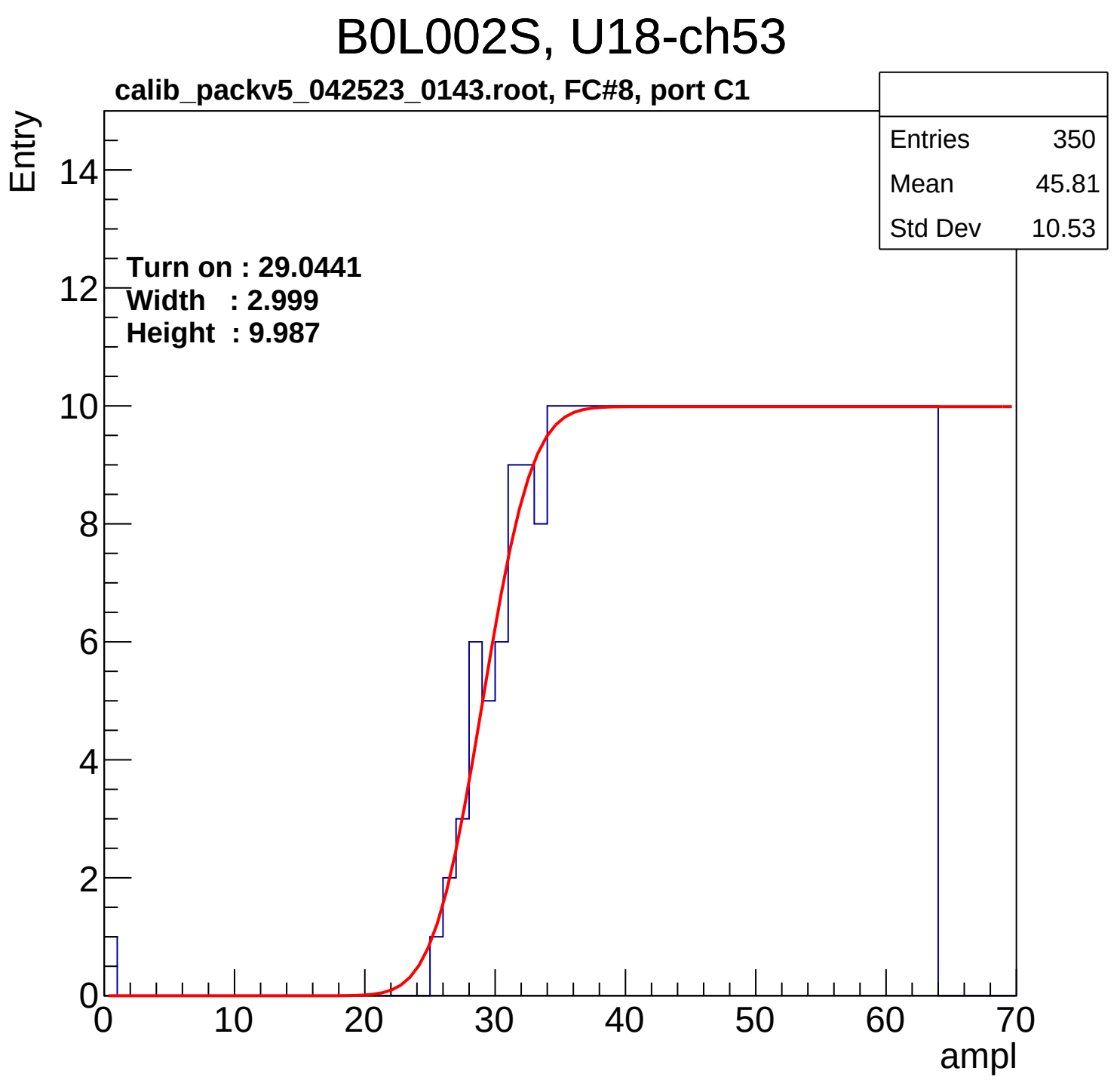

B0L002S, U18-ch48
calib_packv5_042523_0143.root, FC#8, port C1
Entries 378
Mean 44.37
Std Dev 11.44
Turn on : 26.6023
Width : 2.284
Height : 9.986
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

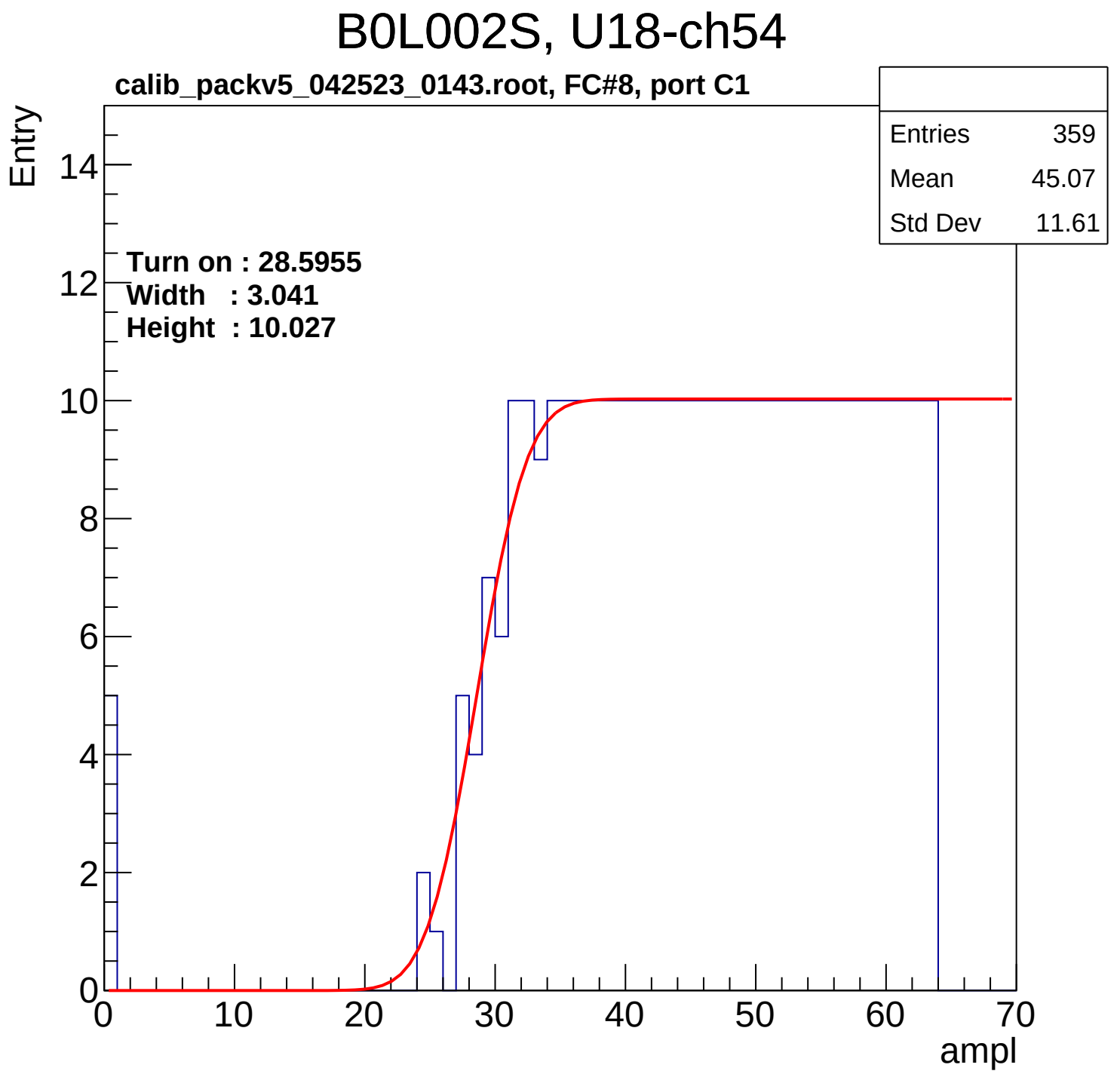

B0L002S, U18-ch49
calib_packv5_042523_0143.root, FC#8, port C1
Entries 373
Mean 44.6
Std Dev 11.35
Turn on : 27.0214
Width : 3.002
Height : 10.006
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

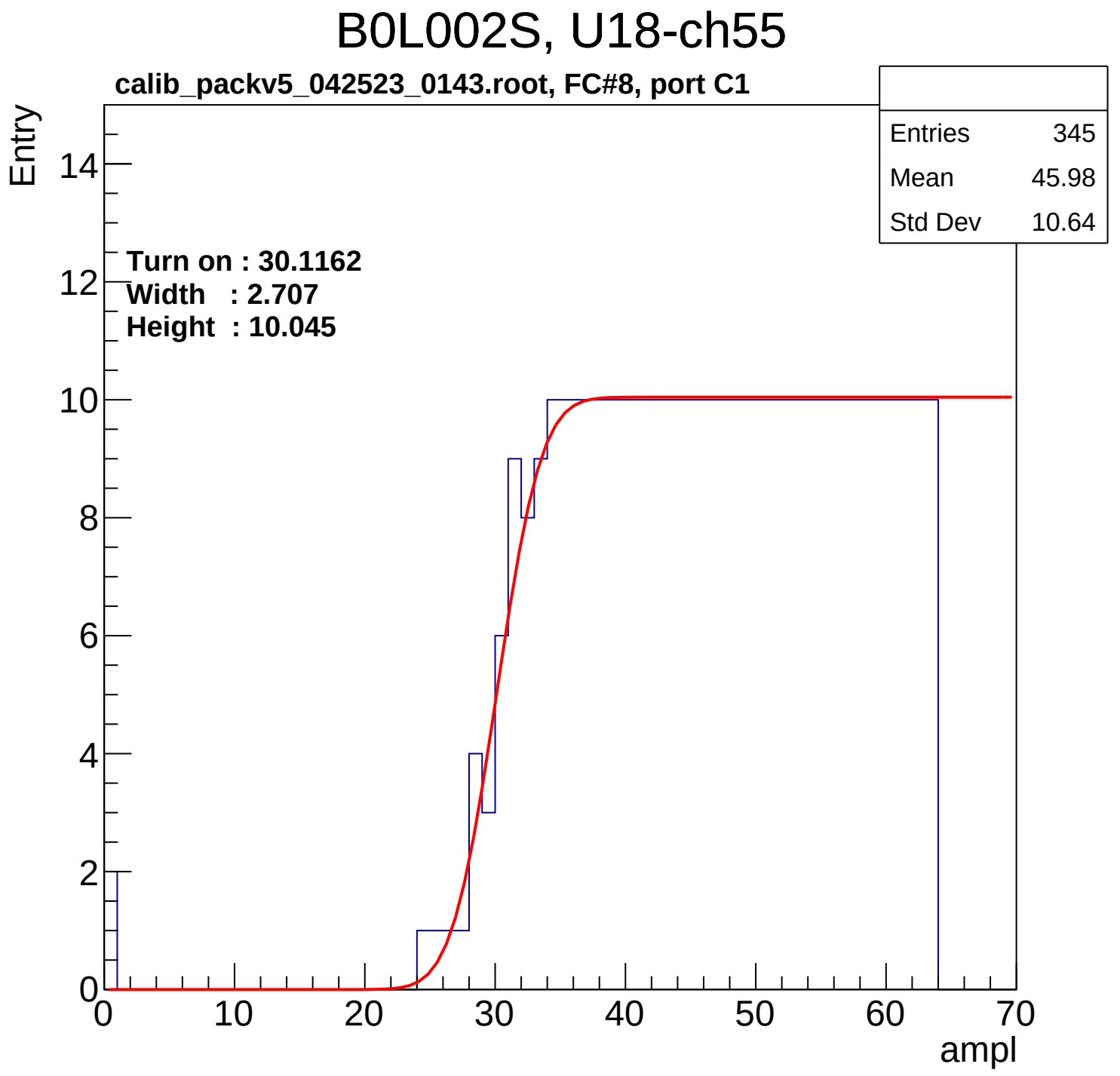

B0L002S, U18-ch50
calib_packv5_042523_0143.root, FC#8, port C1
Entries 368
Mean 44.76
Std Dev 11.44
Turn on : 27.8292
Width : 3.408
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

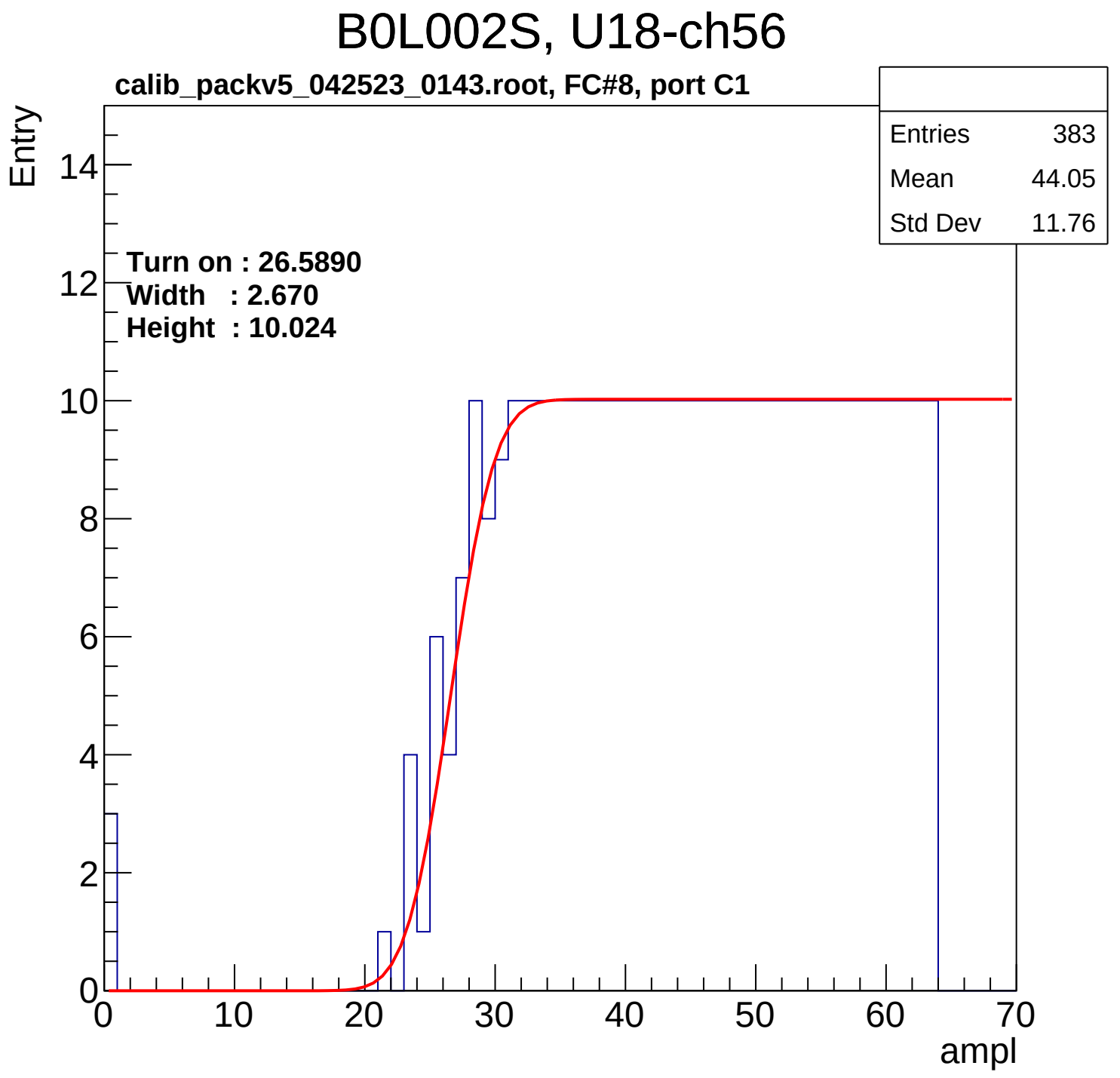

B0L002S, U18-ch51
calib_packv5_042523_0143.root, FC#8, port C1
Entries 376
Mean 44.41
Std Dev 11.57
Turn on : 26.9007
Width : 2.517
Height : 9.990
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

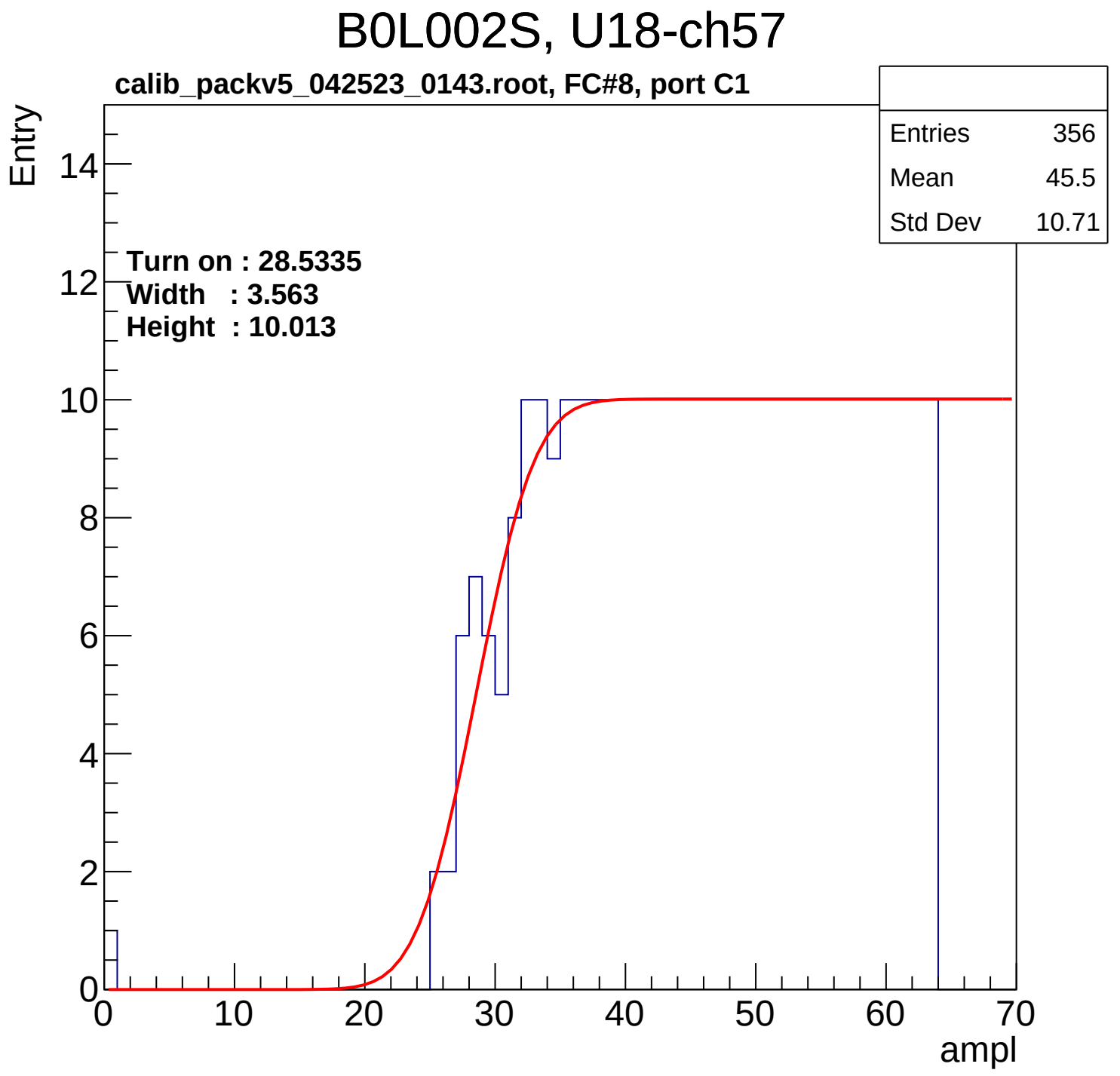

B0L002S, U18-ch52
calib_packv5_042523_0143.root, FC#8, port C1
Entries 366
Mean 45.02
Std Dev 10.95
Turn on : 27.7107
Width : 2.554
Height : 9.948
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

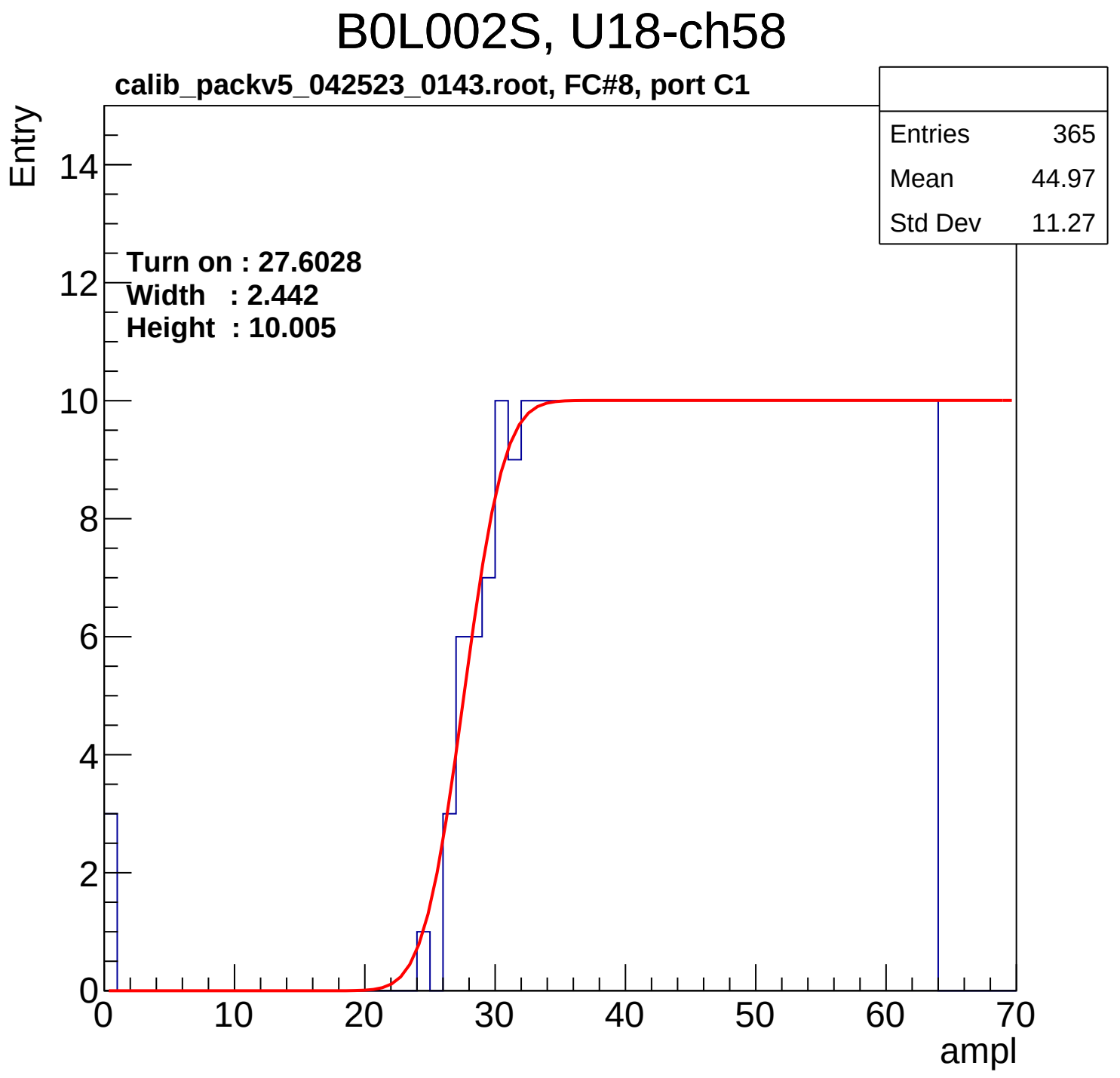

B0L002S, U18-ch53
calib_packv5_042523_0143.root, FC#8, port C1
Entries 350
Mean 45.81
Std Dev 10.53
Turn on : 29.0441
Width : 2.999
Height : 9.987
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

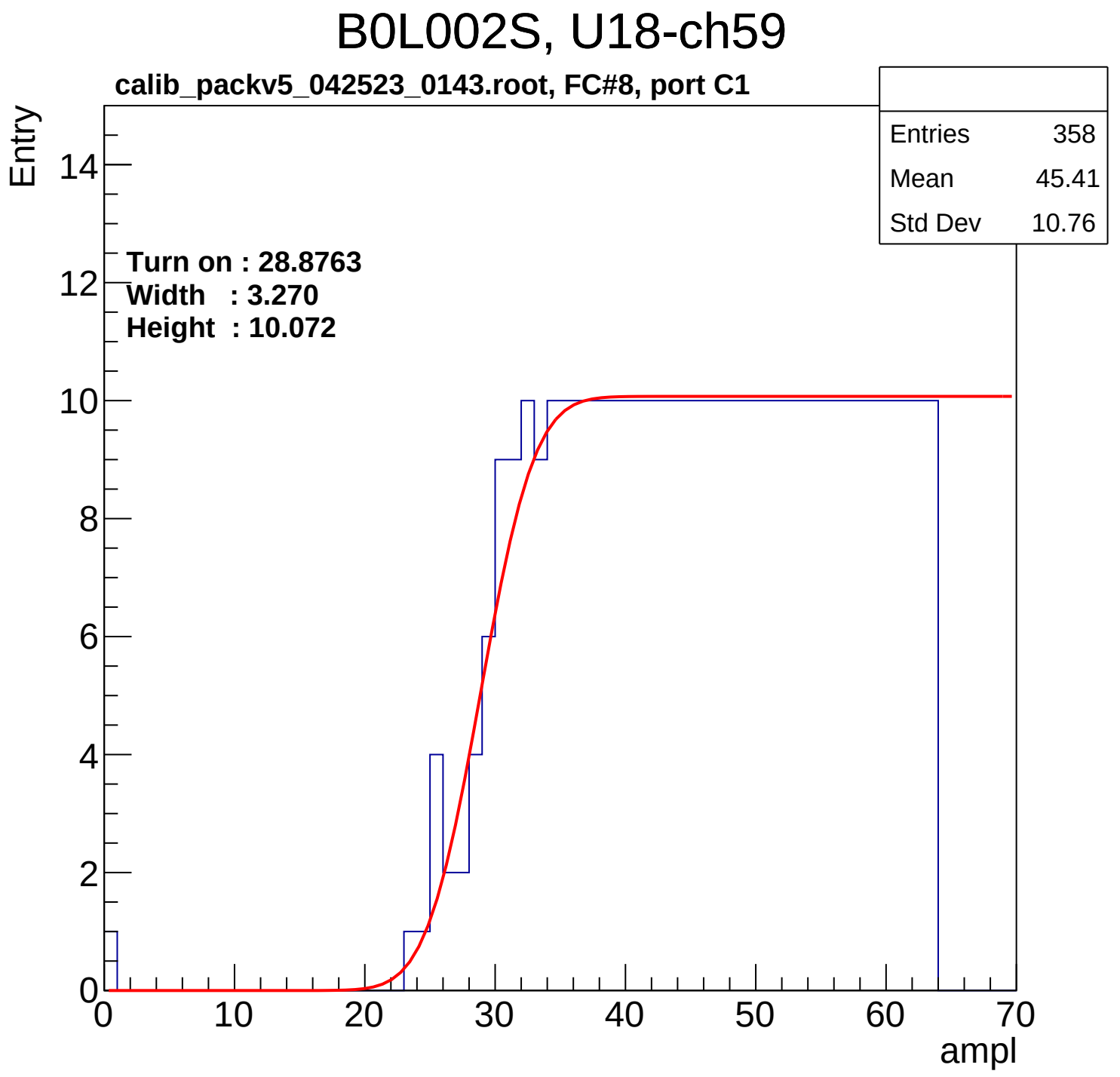

B0L002S, U18-ch54
calib_packv5_042523_0143.root, FC#8, port C1
Entries 359
Mean 45.07
Std Dev 11.61
Turn on : 28.5955
Width : 3.041
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

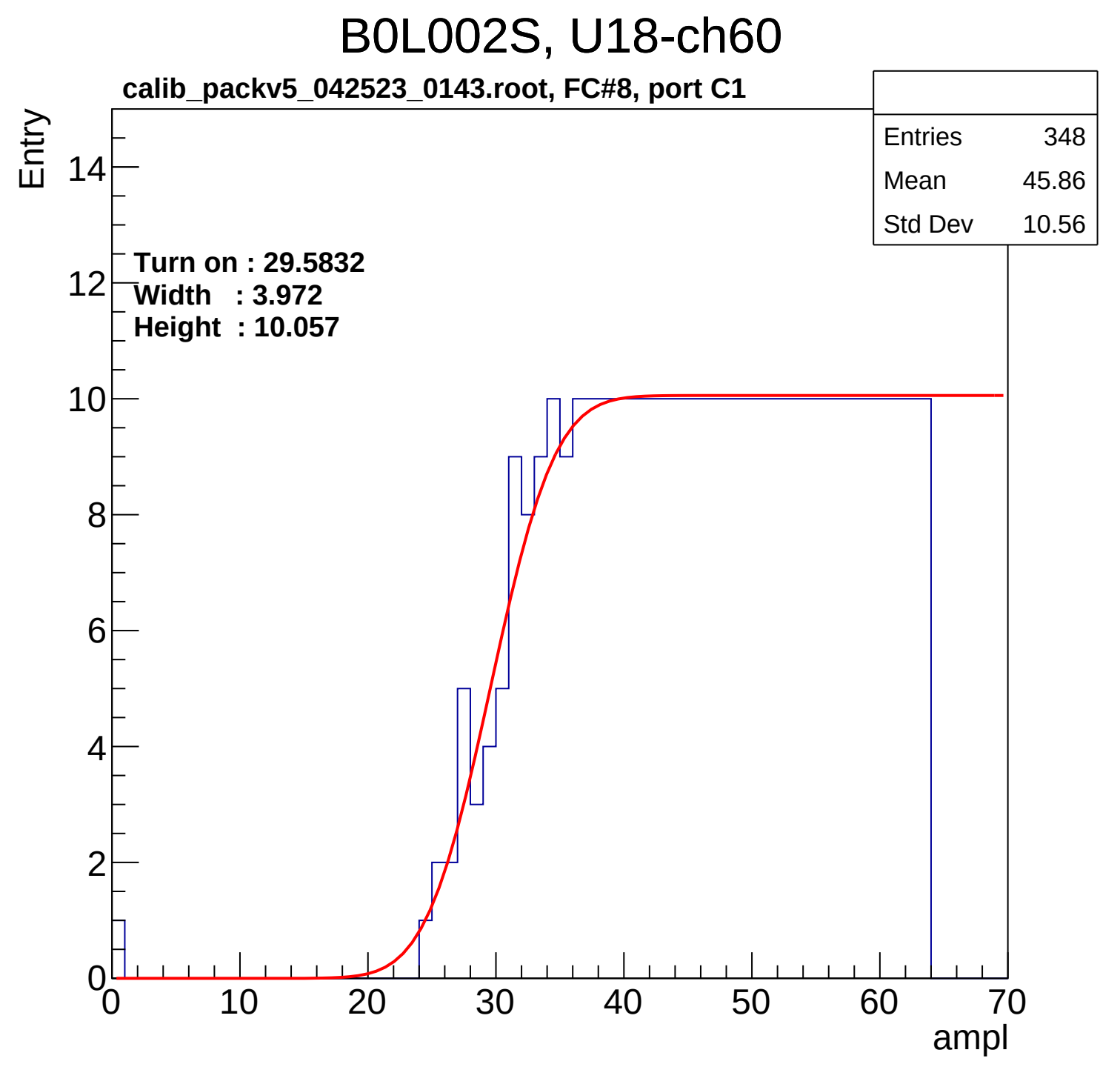

B0L002S, U18-ch55
calib_packv5_042523_0143.root, FC#8, port C1
Entries 345
Mean 45.98
Std Dev 10.64
Turn on : 30.1162
Width : 2.707
Height : 10.045
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

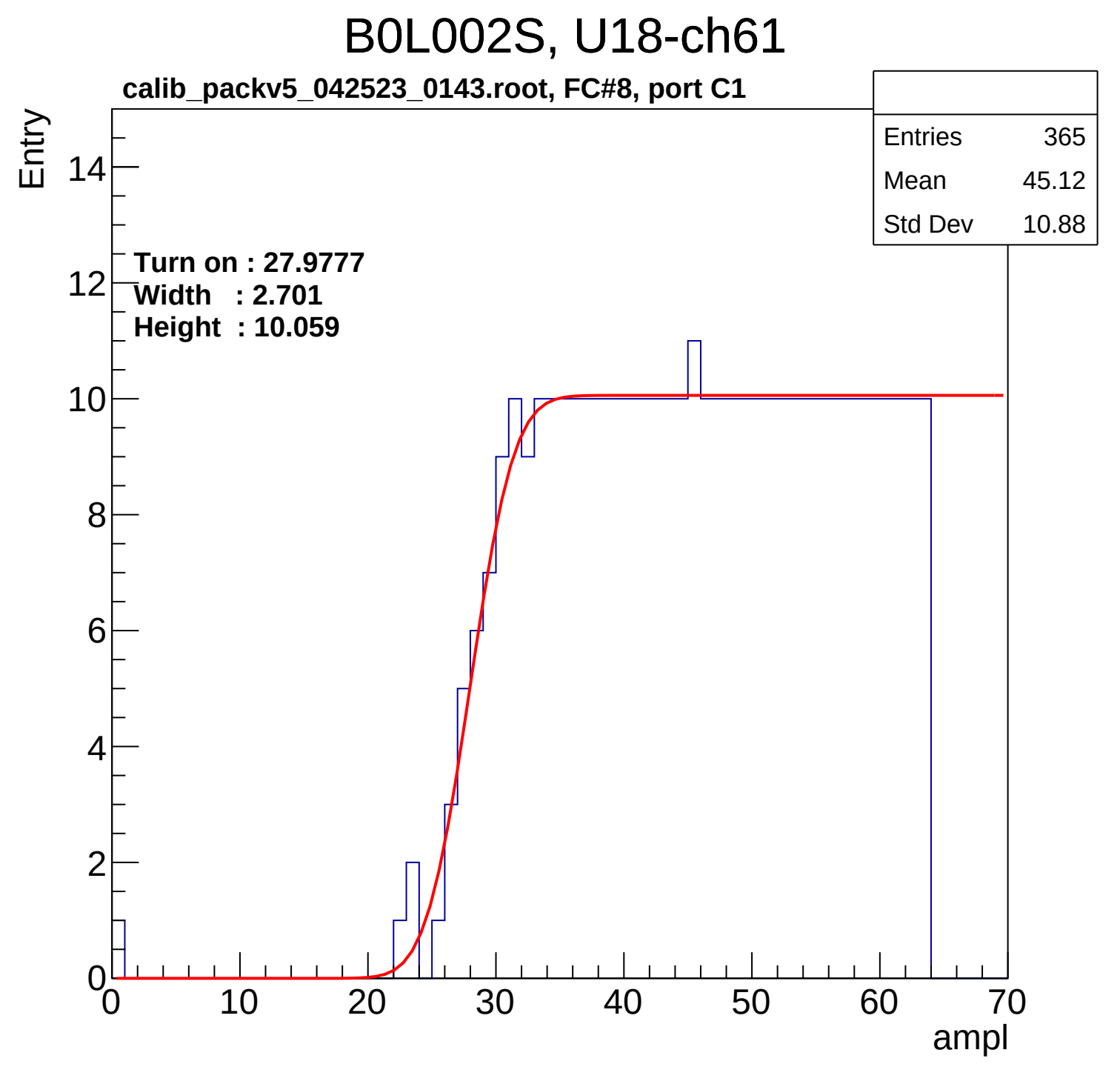

B0L002S, U18-ch56
calib_packv5_042523_0143.root, FC#8, port C1
Entries 383
Mean 44.05
Std Dev 11.76
Turn on : 26.5890
Width : 2.670
Height : 10.024
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

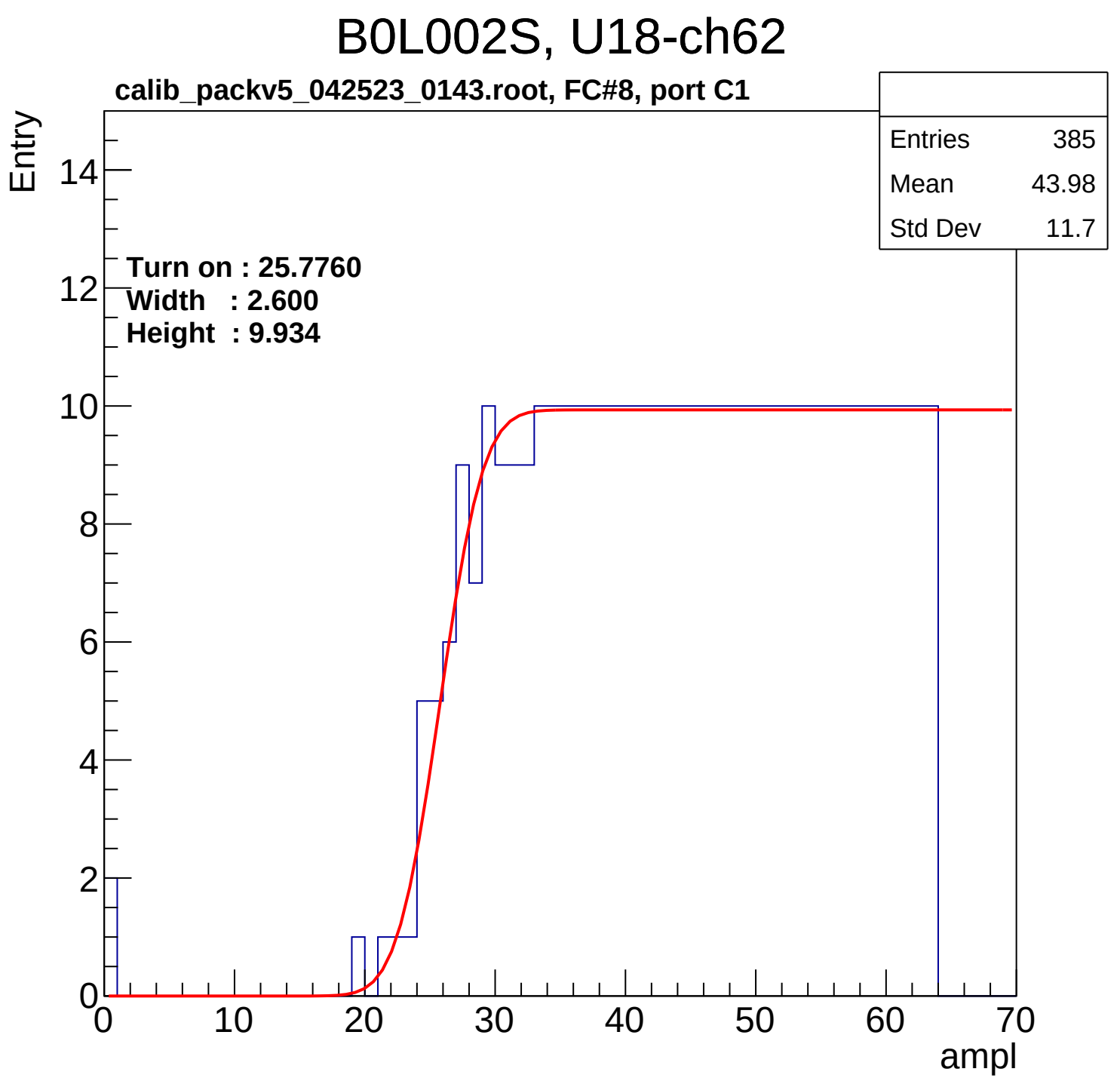

B0L002S, U18-ch57
calib_packv5_042523_0143.root, FC#8, port C1
Entries 356
Mean 45.5
Std Dev 10.71
Turn on : 28.5335
Width : 3.563
Height : 10.013
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

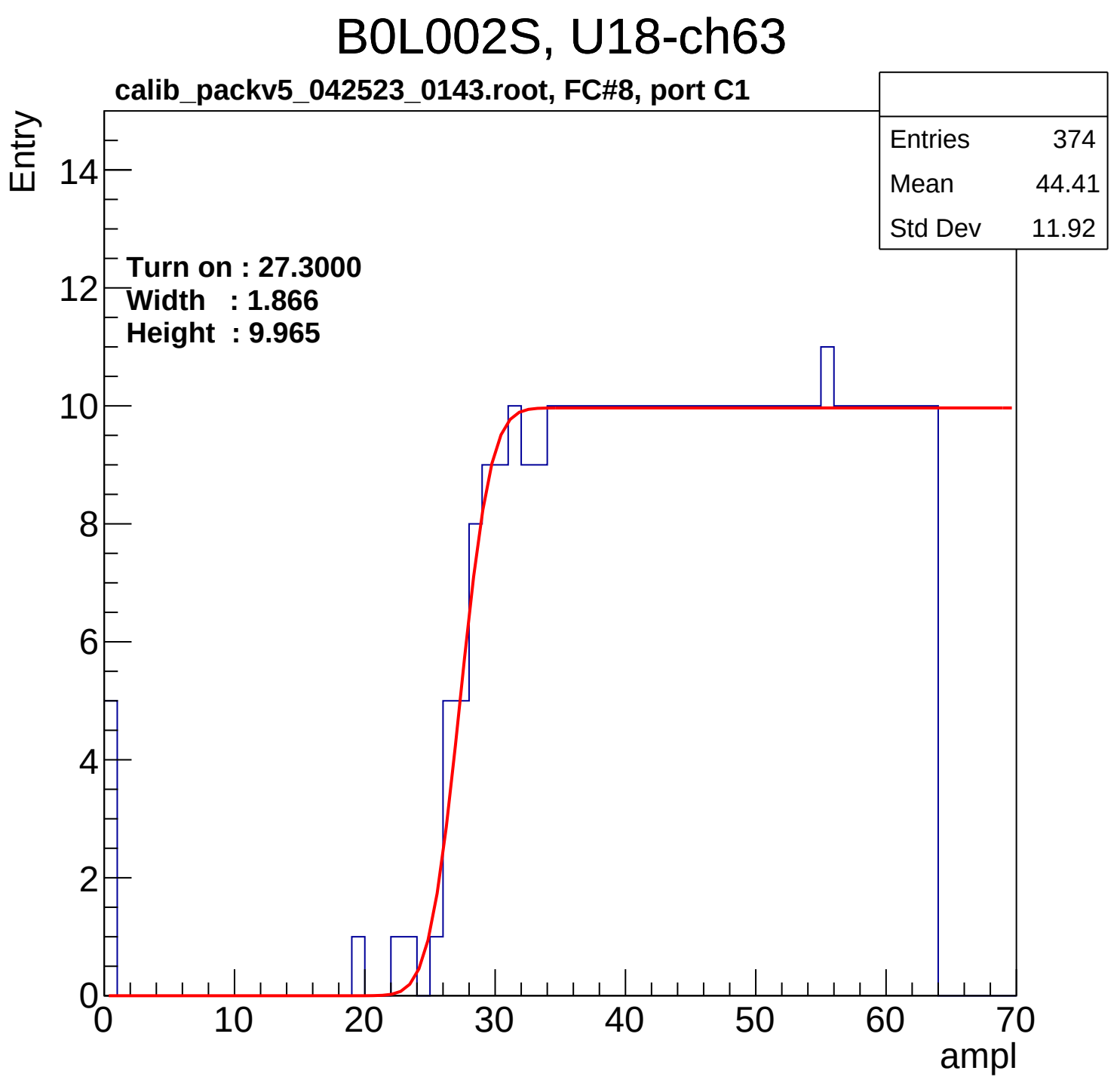

B0L002S, U18-ch58
calib_packv5_042523_0143.root, FC#8, port C1
Entries 365
Mean 44.97
Std Dev 11.27
Turn on : 27.6028
Width : 2.442
Height : 10.005
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

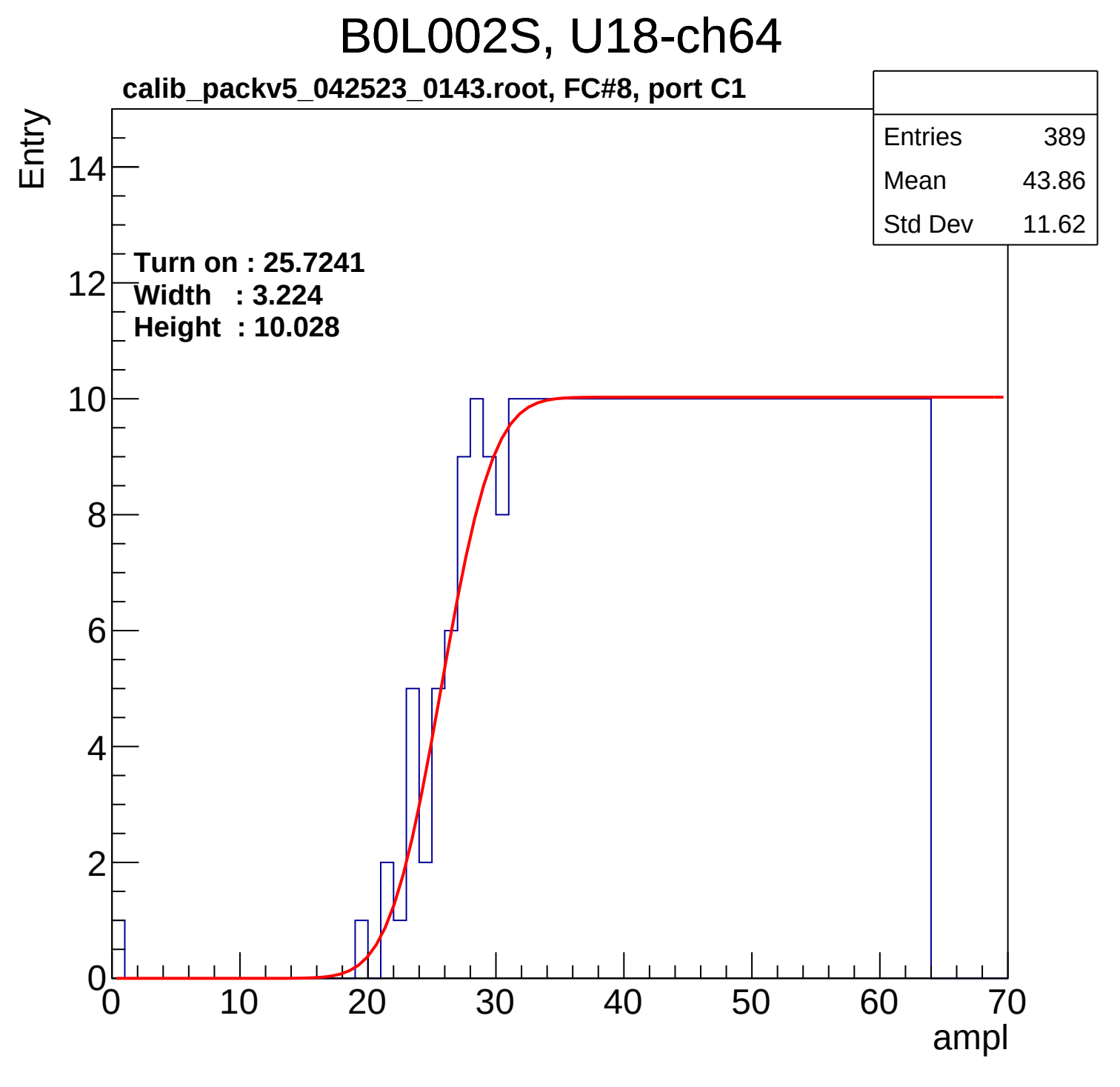

B0L002S, U18-ch59
calib_packv5_042523_0143.root, FC#8, port C1
Entries 358
Mean 45.41
Std Dev 10.76
Turn on : 28.8763
Width : 3.270
Height : 10.072
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

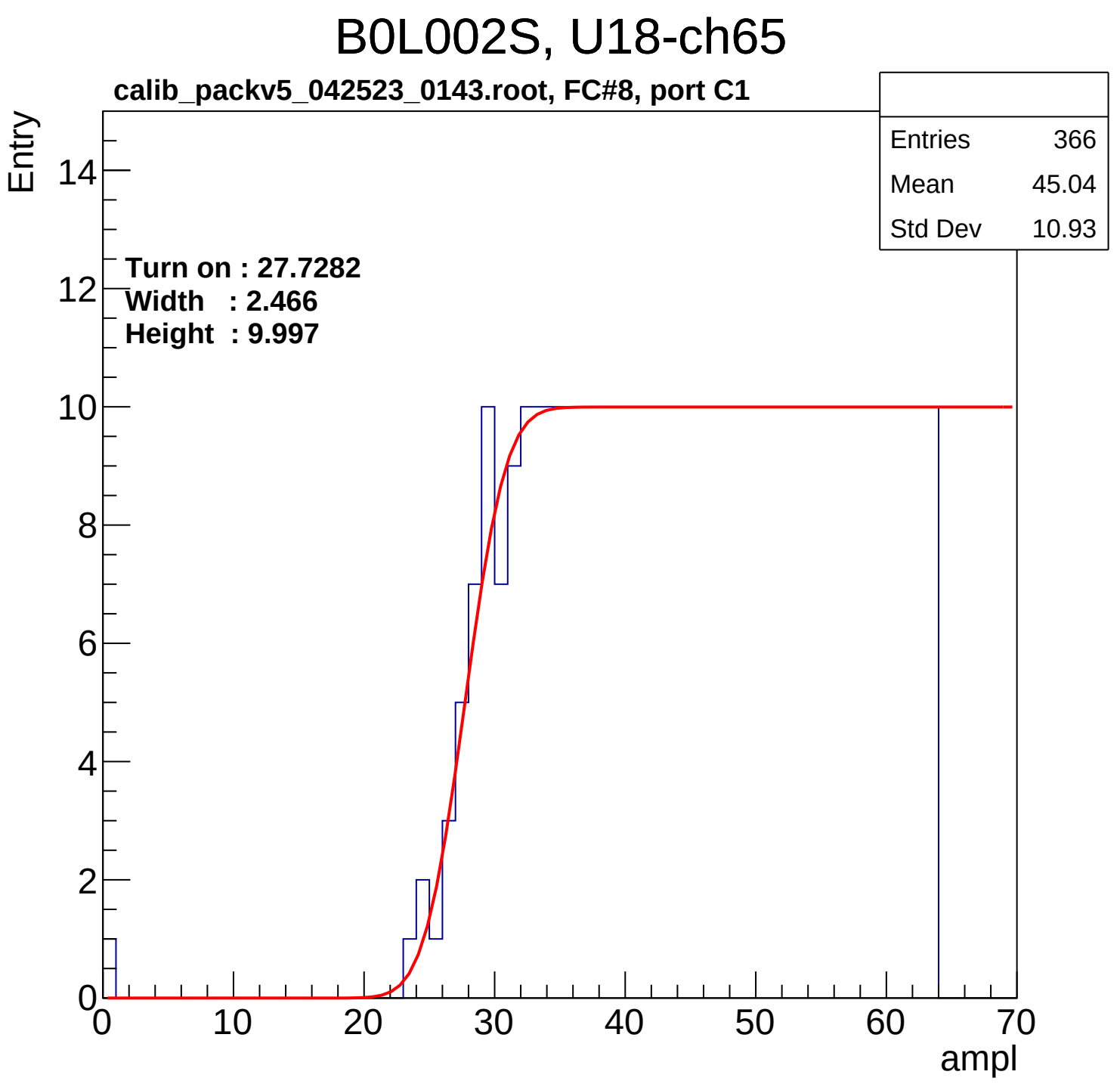

B0L002S, U18-ch60
calib_packv5_042523_0143.root, FC#8, port C1
Entries 348
Mean 45.86
Std Dev 10.56
Turn on : 29.5832
Width : 3.972
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

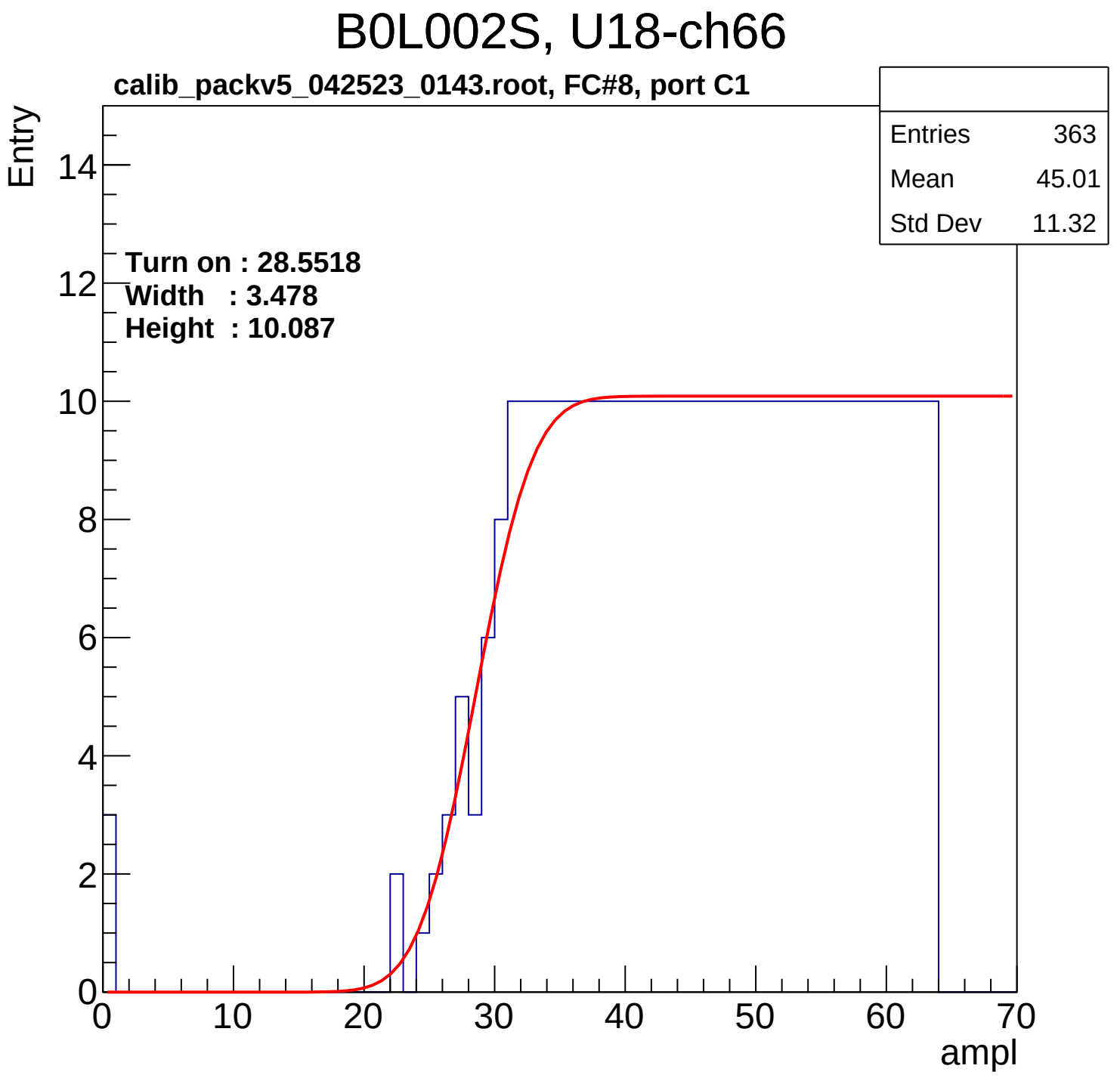

B0L002S, U18-ch61
calib_packv5_042523_0143.root, FC#8, port C1
Entries 365
Mean 45.12
Std Dev 10.88
Turn on : 27.9777
Width : 2.701
Height : 10.059
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

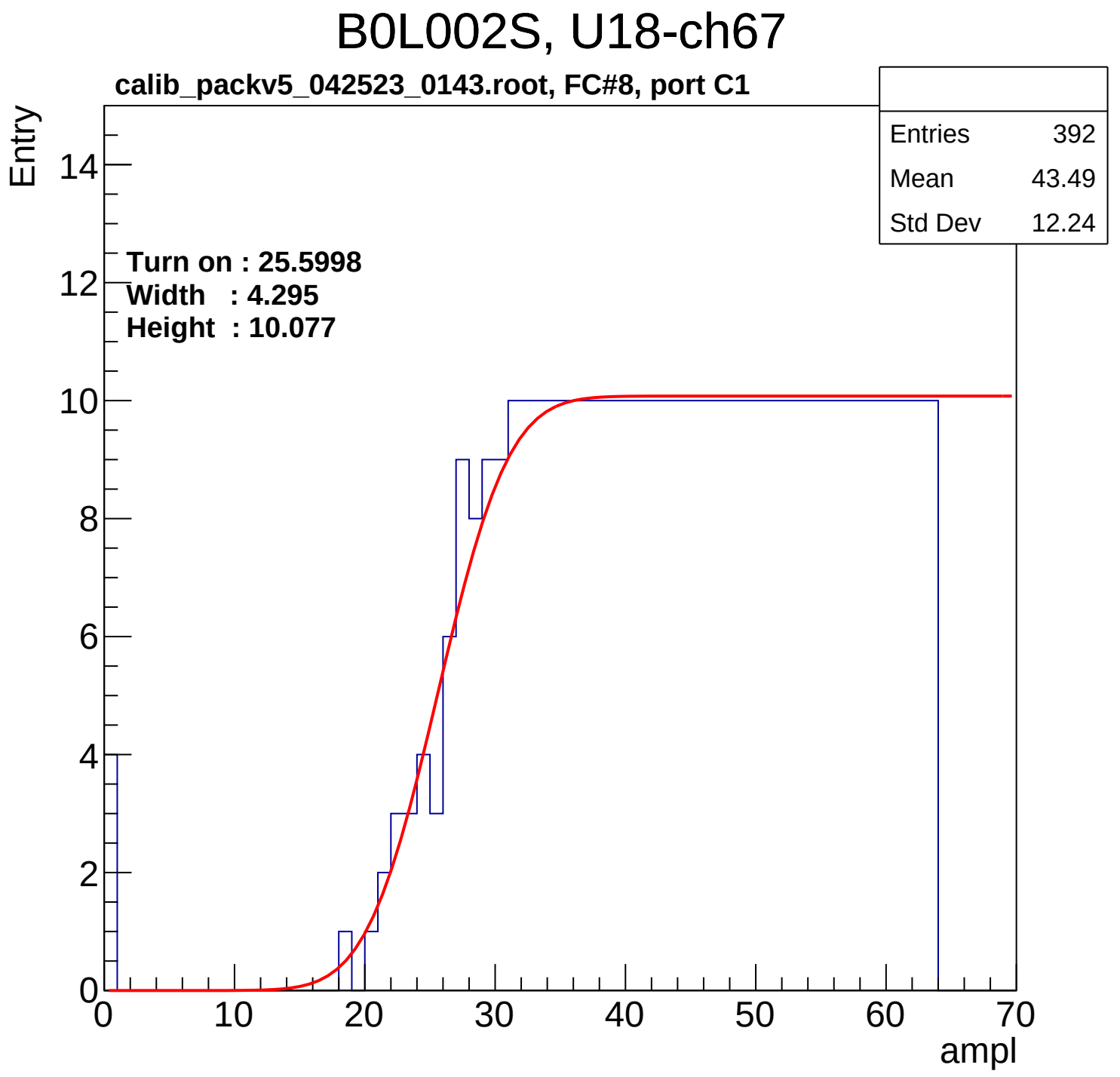

B0L002S, U18-ch62
calib_packv5_042523_0143.root, FC#8, port C1
Entries 385
Mean 43.98
Std Dev 11.7
Turn on : 25.7760
Width : 2.600
Height : 9.934
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

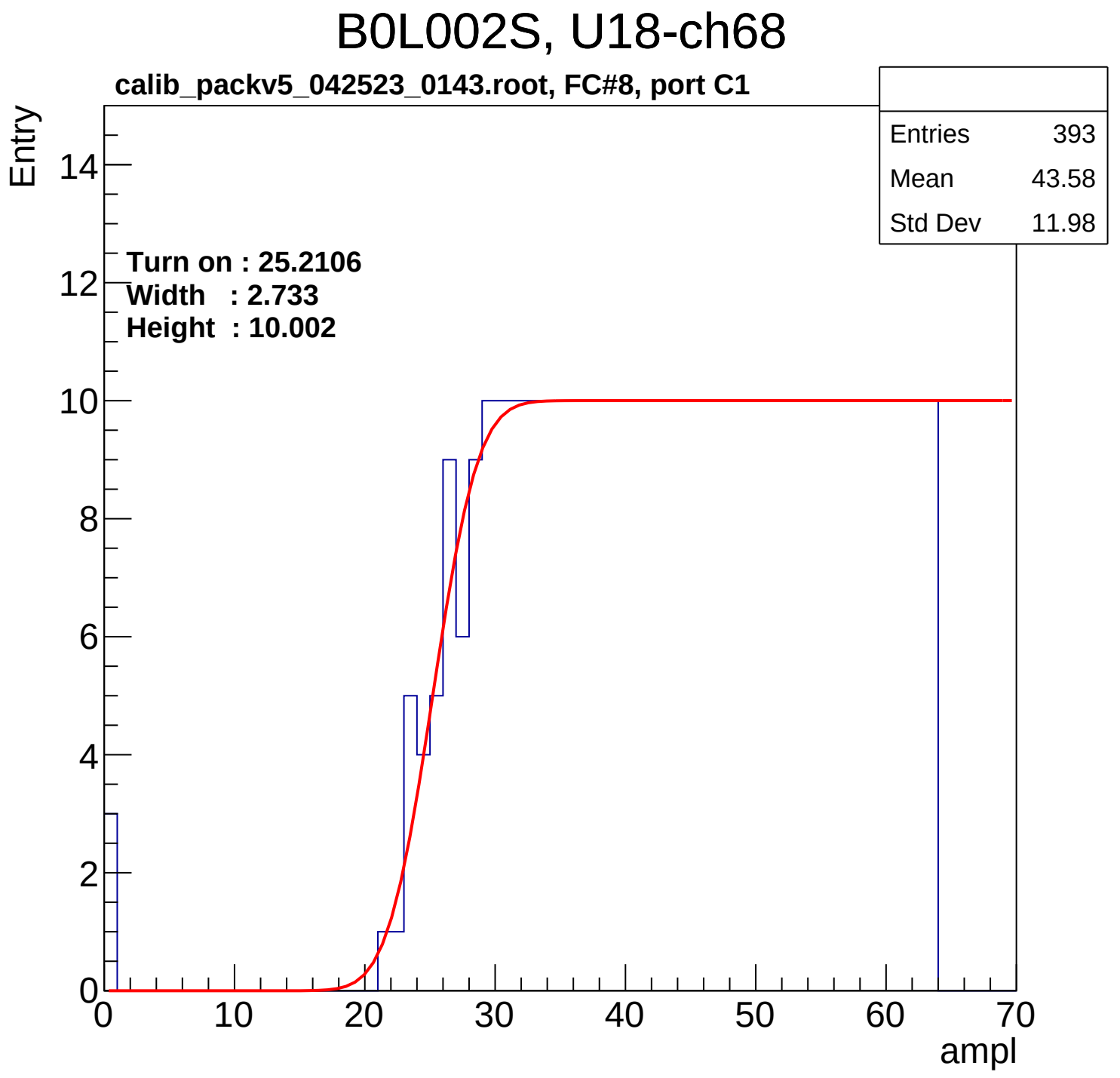

B0L002S, U18-ch63
calib_packv5_042523_0143.root, FC#8, port C1
Entries 374
Mean 44.41
Std Dev 11.92
Turn on : 27.3000
Width : 1.866
Height : 9.965
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

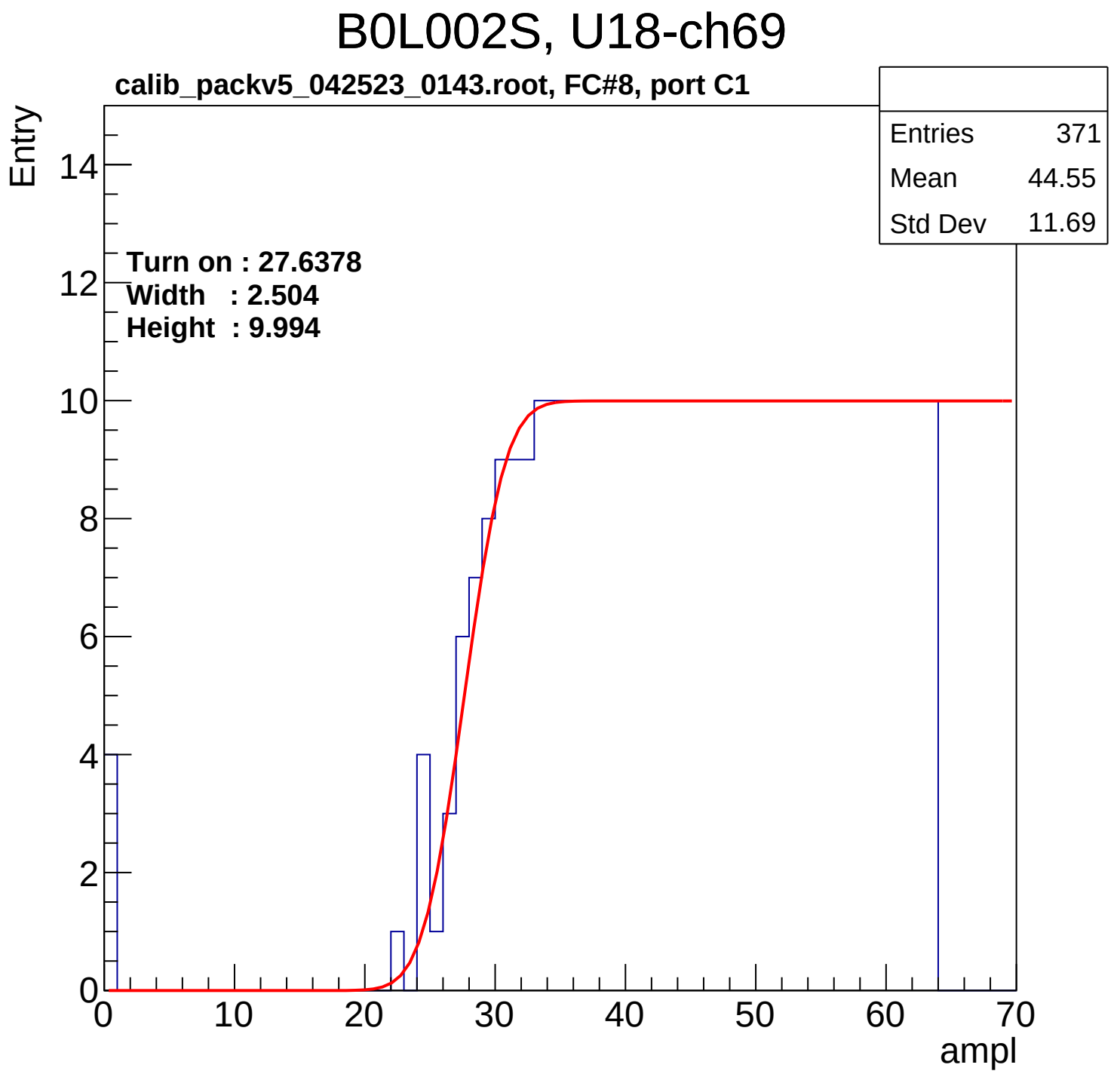

B0L002S, U18-ch64
calib_packv5_042523_0143.root, FC#8, port C1
Entries 389
Mean 43.86
Std Dev 11.62
Turn on : 25.7241
Width : 3.224
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

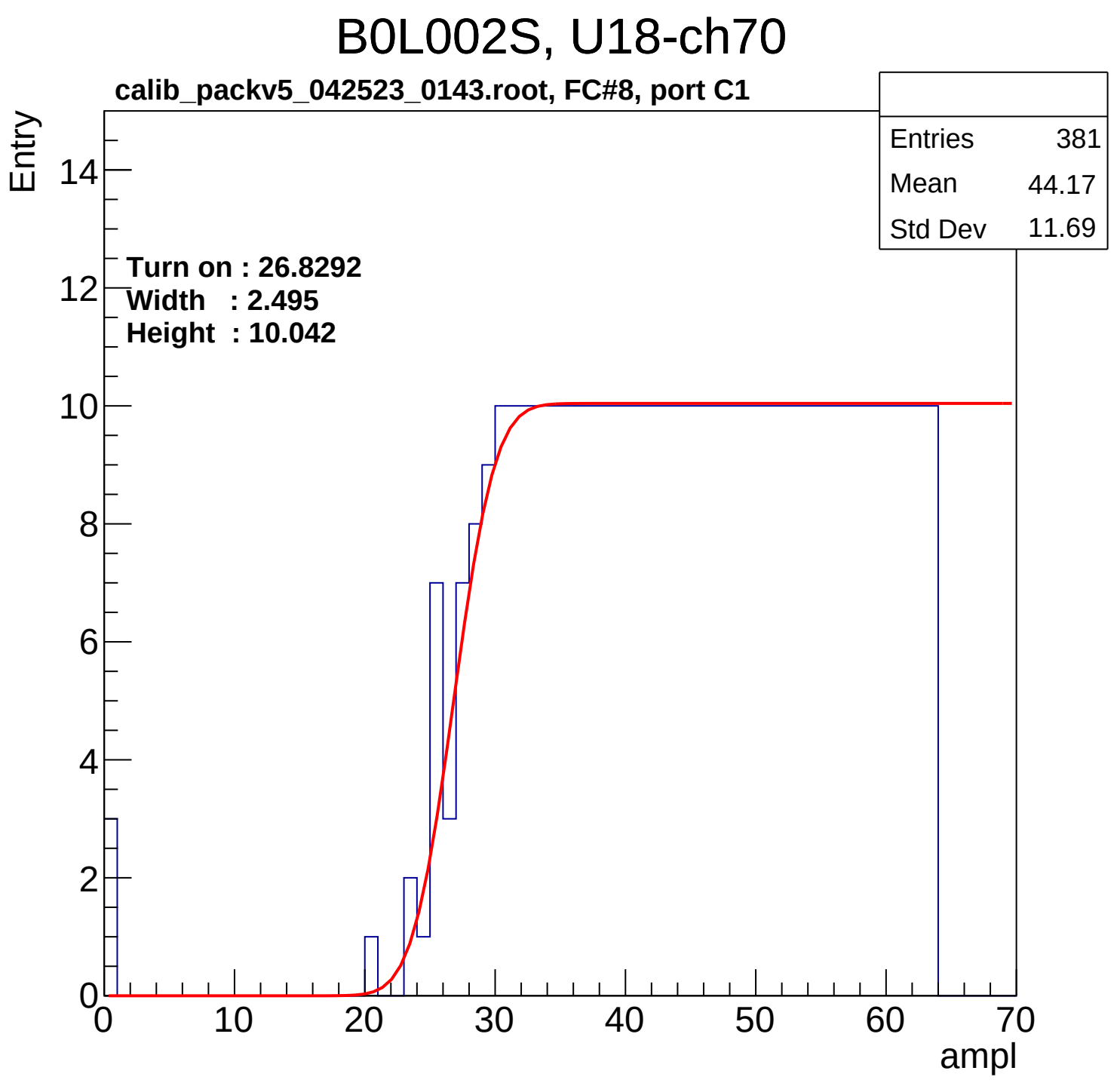

B0L002S, U18-ch65
calib_packv5_042523_0143.root, FC#8, port C1
Entries 366
Mean 45.04
Std Dev 10.93
Turn on : 27.7282
Width : 2.466
Height : 9.997
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

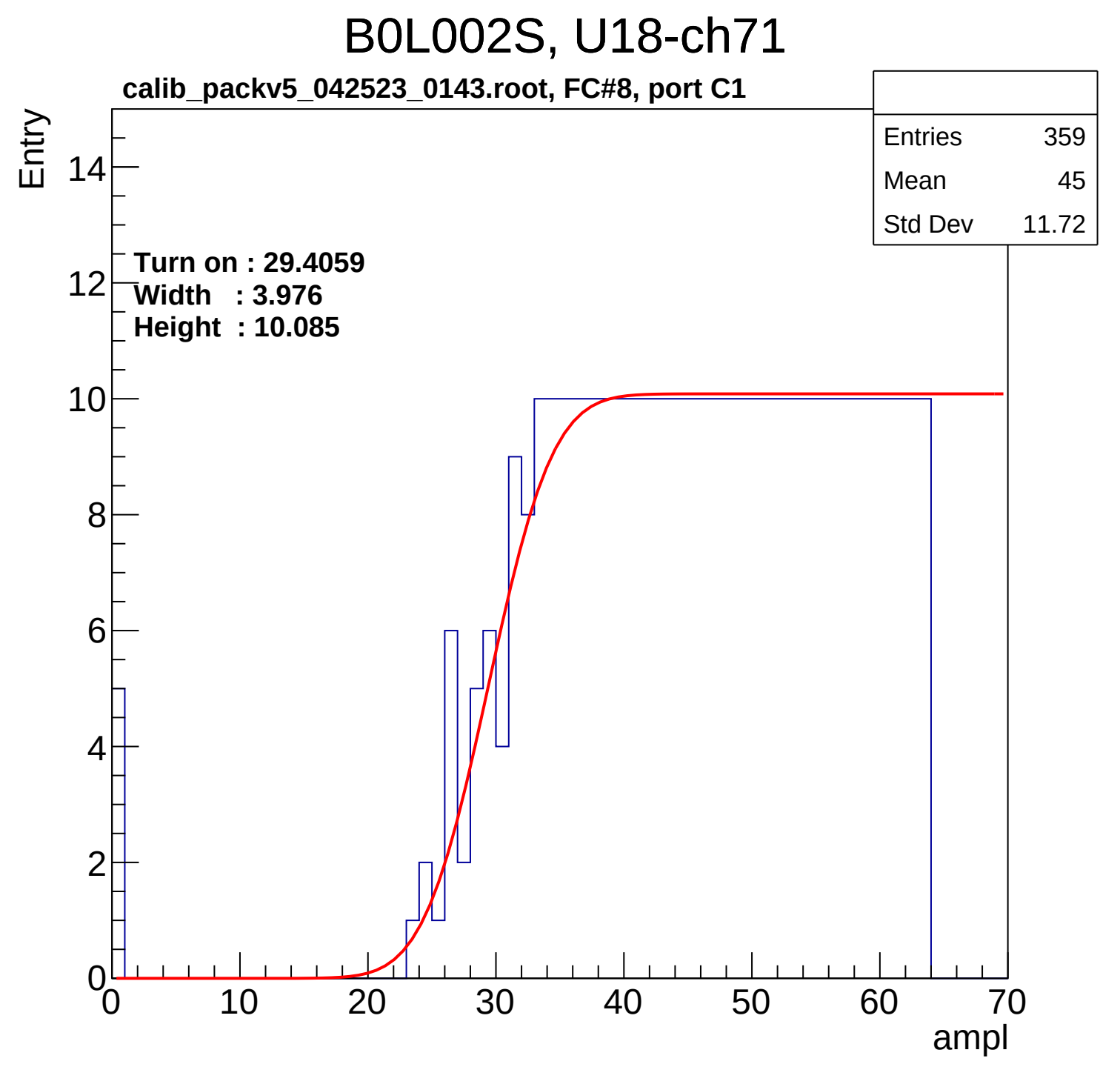

B0L002S, U18-ch66
calib_packv5_042523_0143.root, FC#8, port C1
Entries 363
Mean 45.01
Std Dev 11.32
Turn on : 28.5518
Width : 3.478
Height : 10.087
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

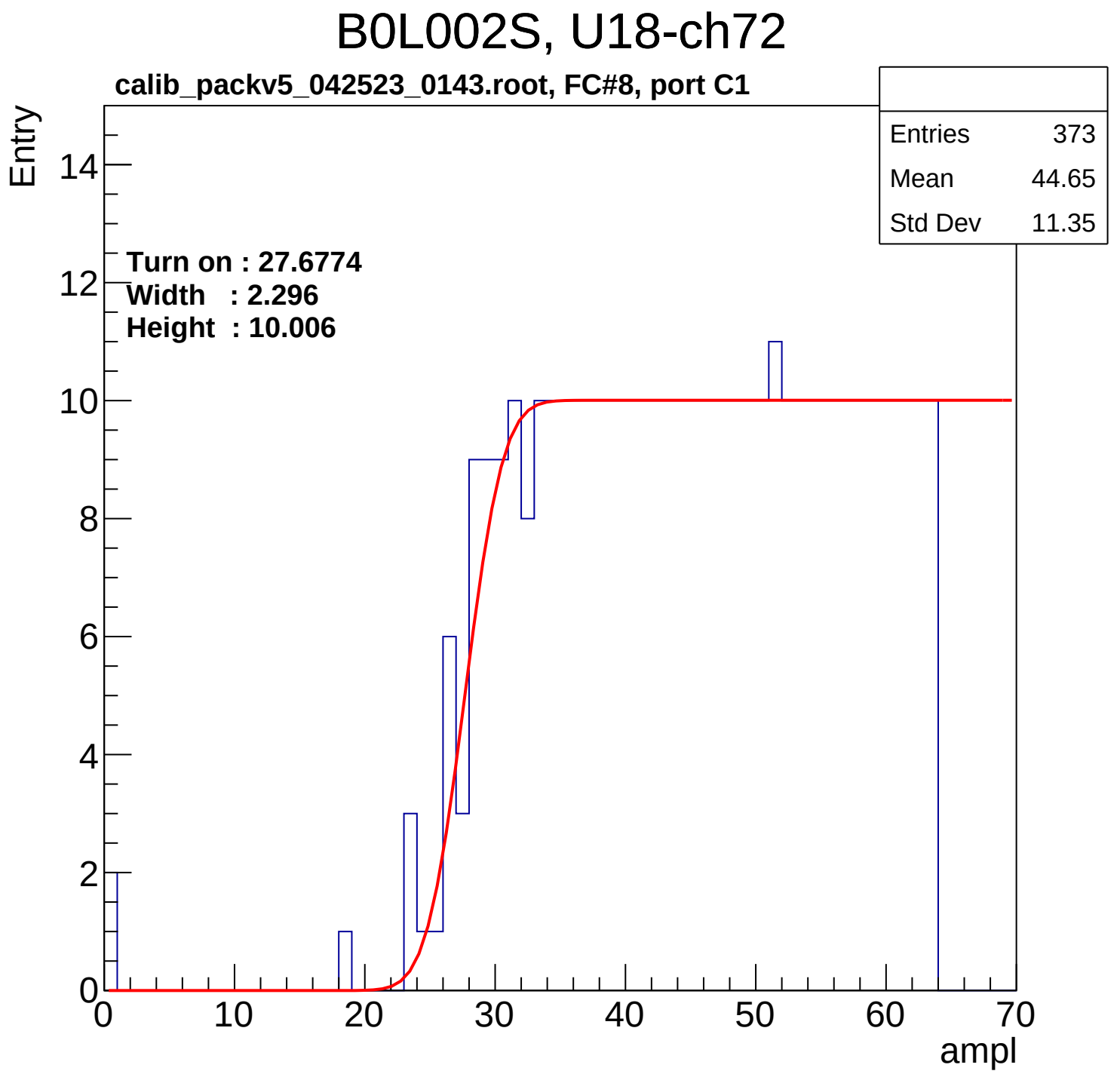

B0L002S, U18-ch67
calib_packv5_042523_0143.root, FC#8, port C1
Entries 392
Mean 43.49
Std Dev 12.24
Turn on : 25.5998
Width : 4.295
Height : 10.077
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

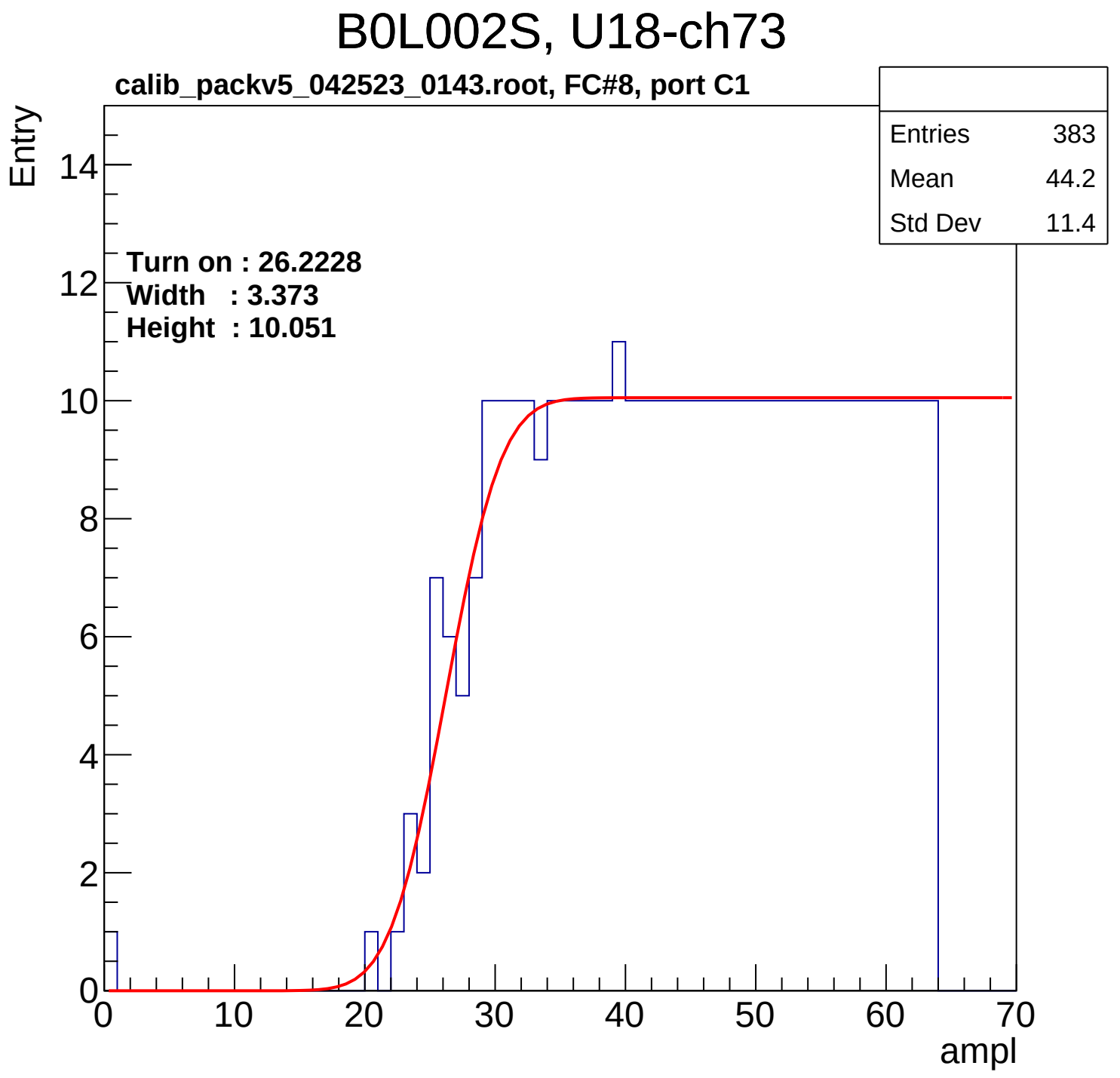

B0L002S, U18-ch68
calib_packv5_042523_0143.root, FC#8, port C1
Entries 393
Mean 43.58
Std Dev 11.98
Turn on : 25.2106
Width : 2.733
Height : 10.002
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

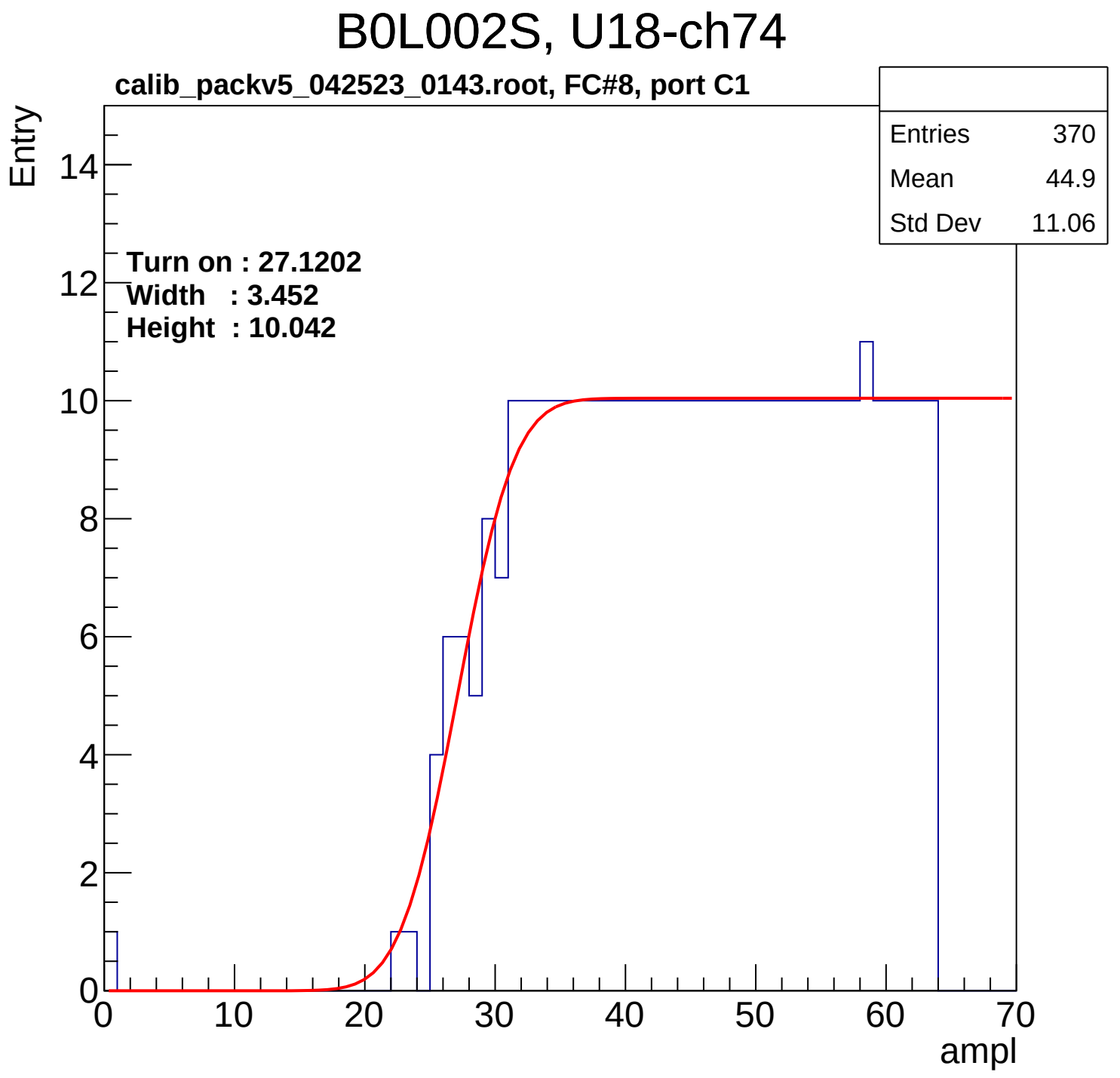

B0L002S, U18-ch69
calib_packv5_042523_0143.root, FC#8, port C1
Entries 371
Mean 44.55
Std Dev 11.69
Turn on : 27.6378
Width : 2.504
Height : 9.994
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

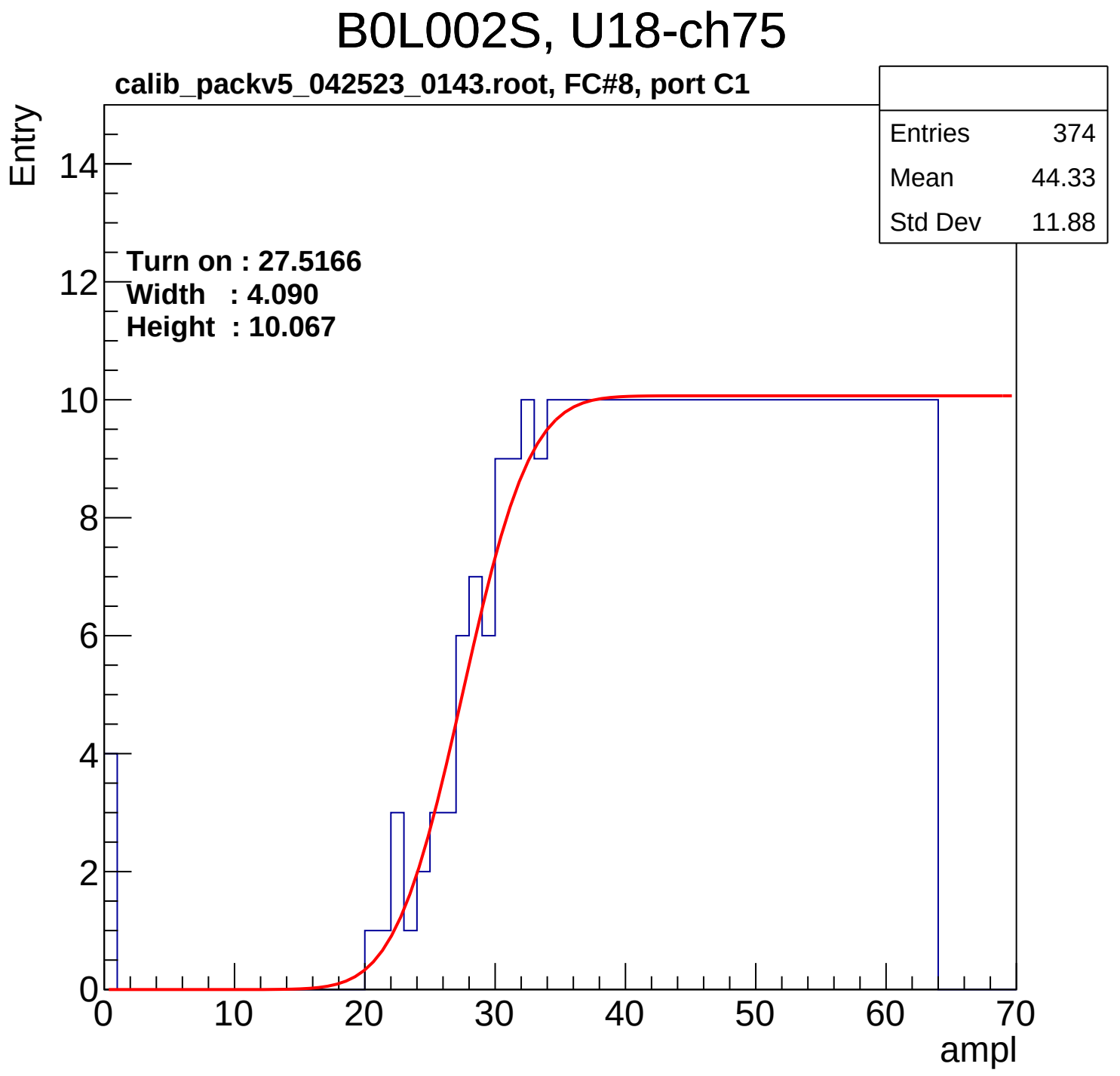

B0L002S, U18-ch70
calib_packv5_042523_0143.root, FC#8, port C1
Entries 381
Mean 44.17
Std Dev 11.69
Turn on : 26.8292
Width : 2.495
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

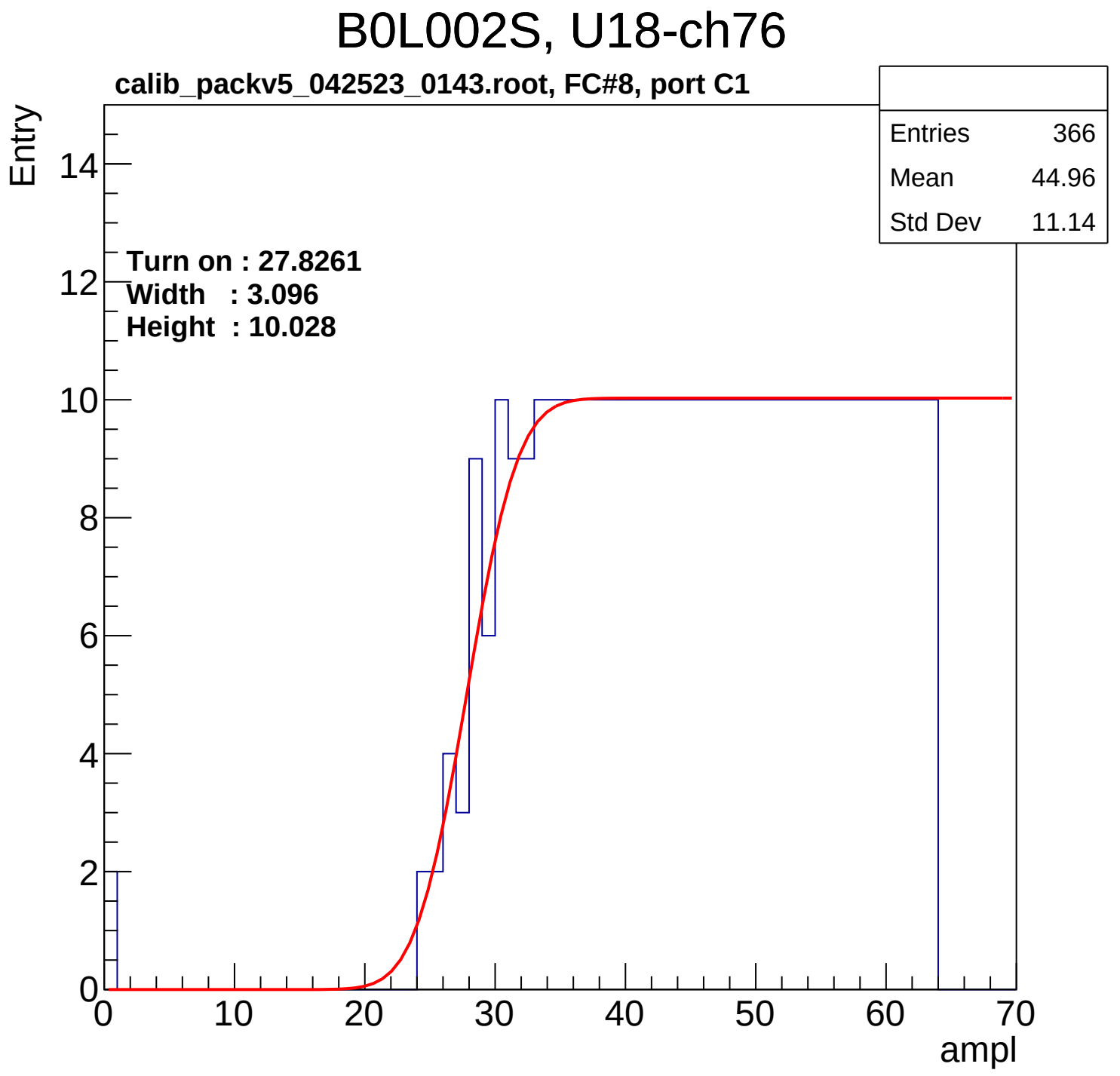

B0L002S, U18-ch71
calib_packv5_042523_0143.root, FC#8, port C1
Entries 359
Mean 45
Std Dev 11.72
Turn on : 29.4059
Width : 3.976
Height : 10.085
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

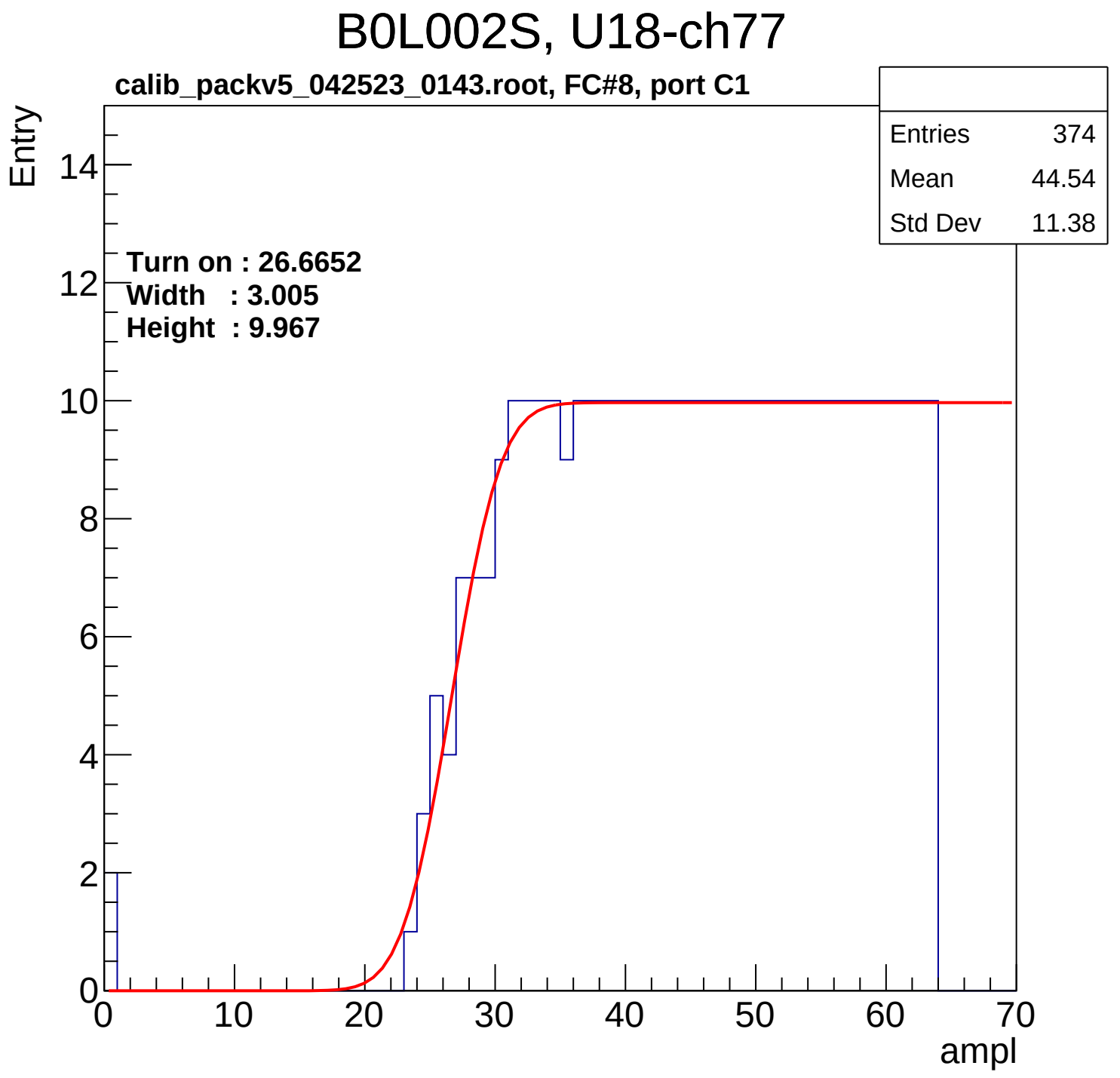

B0L002S, U18-ch72
calib_packv5_042523_0143.root, FC#8, port C1
Entries 373
Mean 44.65
Std Dev 11.35
Turn on : 27.6774
Width : 2.296
Height : 10.006
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

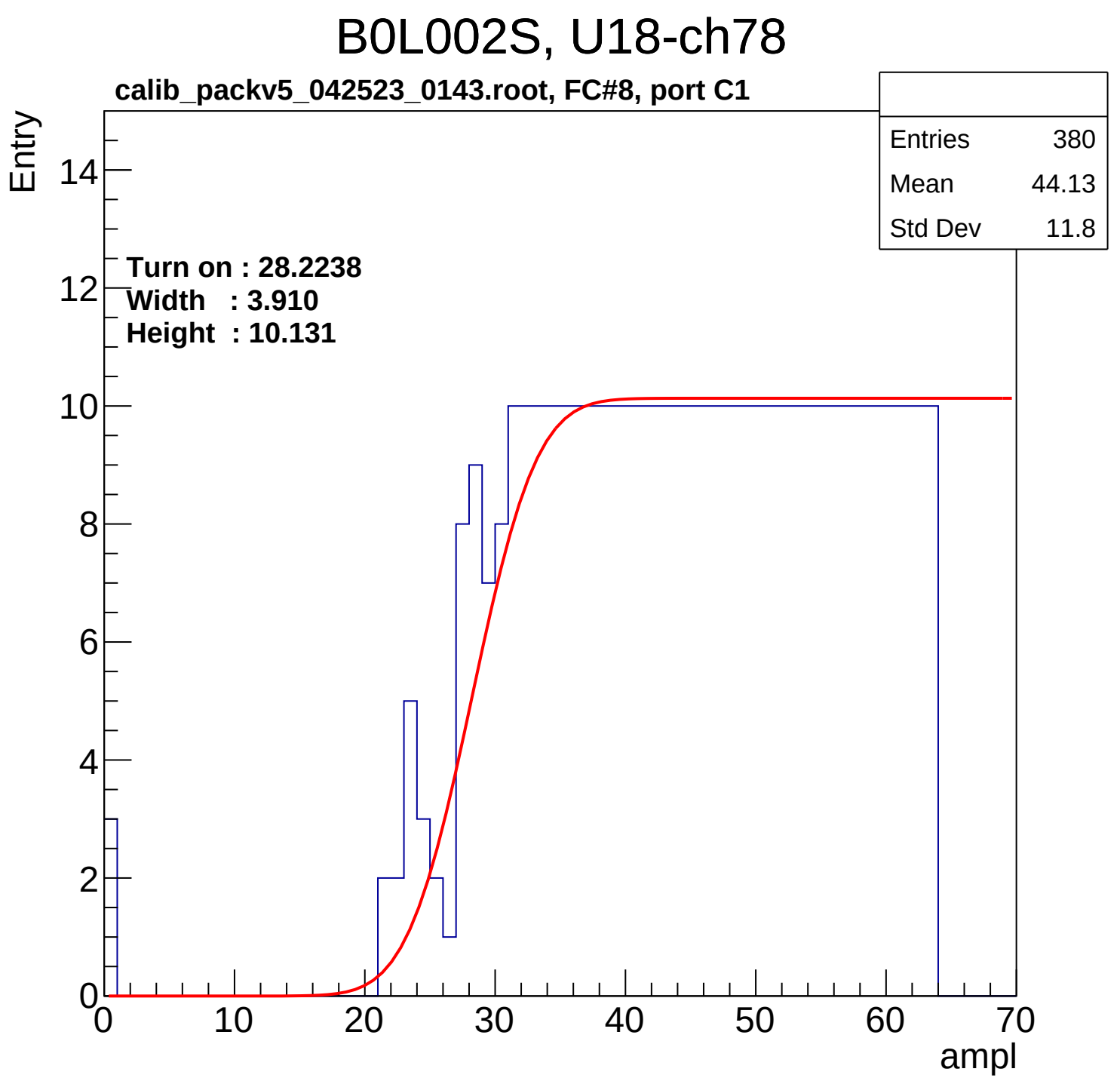

B0L002S, U18-ch73
calib_packv5_042523_0143.root, FC#8, port C1
Entries 383
Mean 44.2
Std Dev 11.4
Turn on : 26.2228
Width : 3.373
Height : 10.051
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

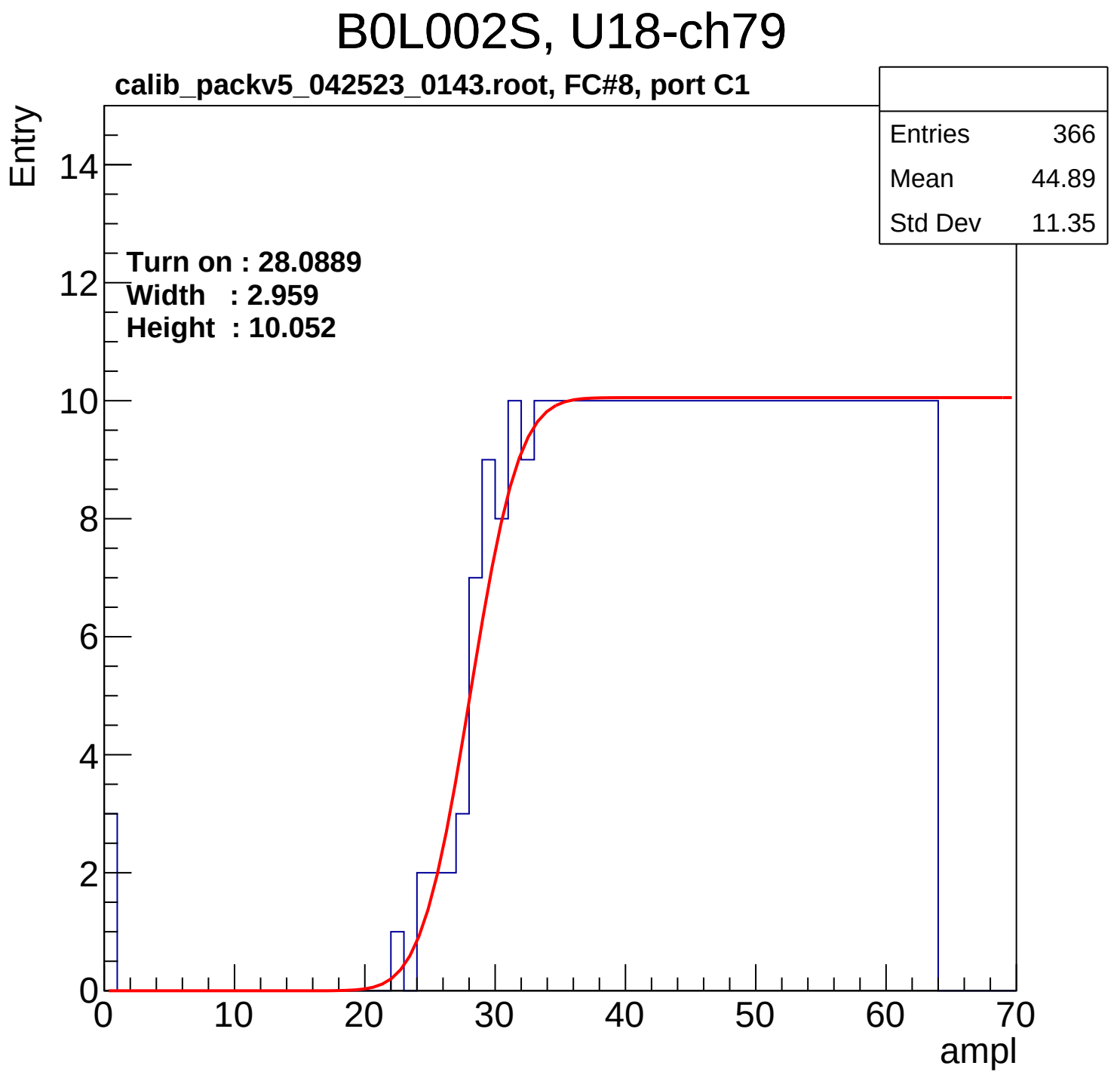

B0L002S, U18-ch74
calib_packv5_042523_0143.root, FC#8, port C1
Entries 370
Mean 44.9
Std Dev 11.06
Turn on : 27.1202
Width : 3.452
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

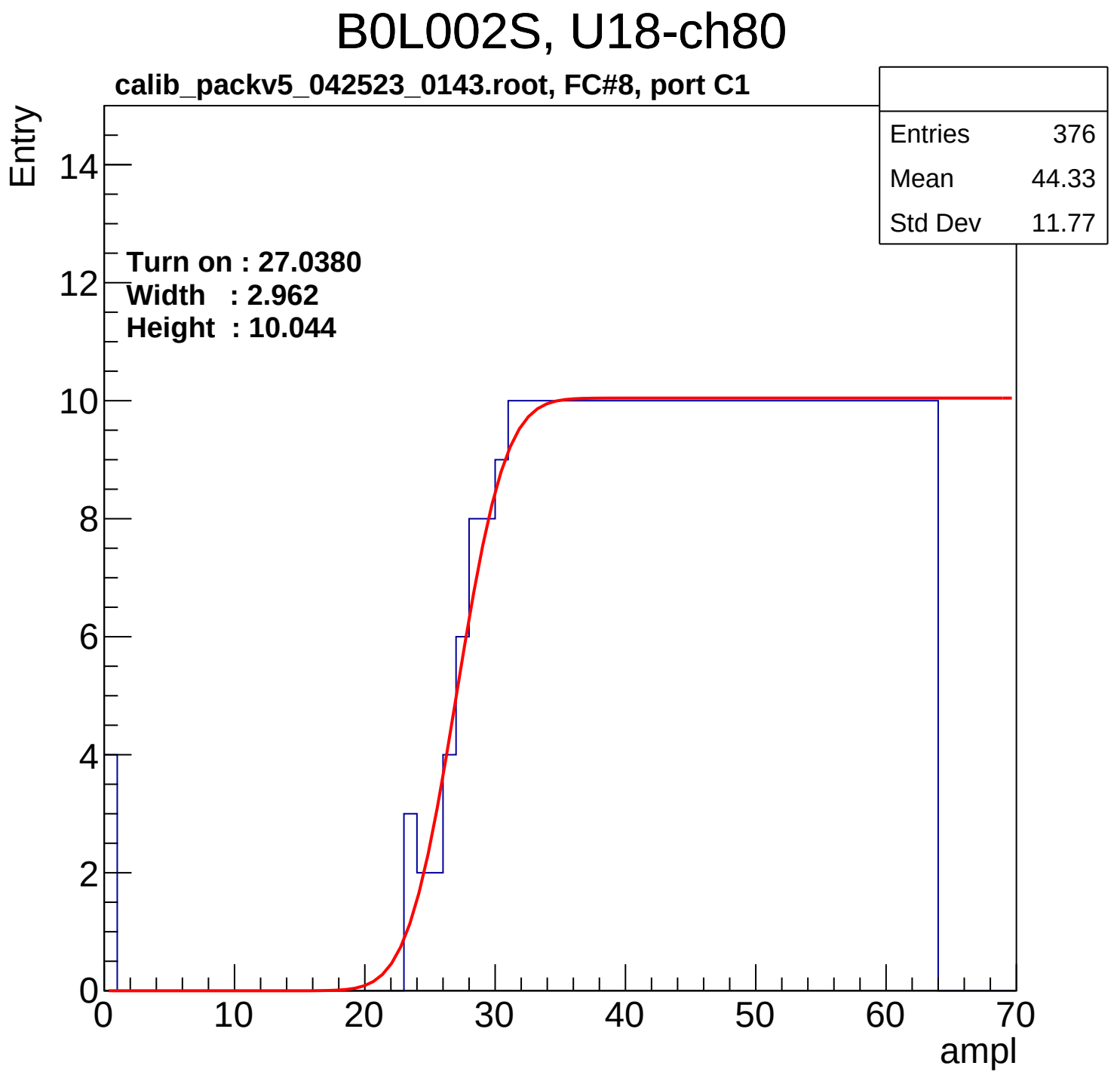

B0L002S, U18-ch75
calib_packv5_042523_0143.root, FC#8, port C1
Entries 374
Mean 44.33
Std Dev 11.88
Turn on : 27.5166
Width : 4.090
Height : 10.067
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

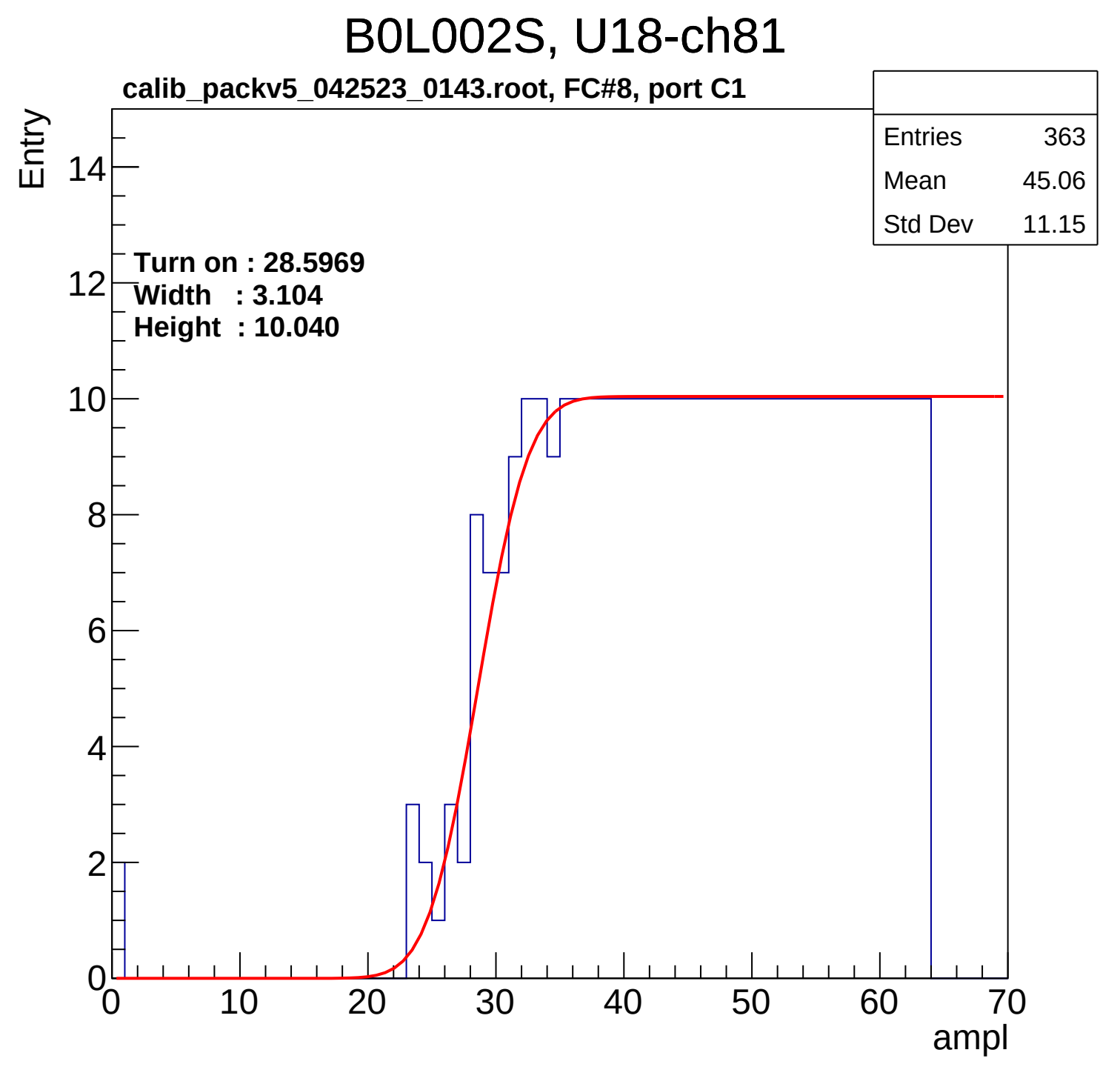

B0L002S, U18-ch76
calib_packv5_042523_0143.root, FC#8, port C1
Entries 366
Mean 44.96
Std Dev 11.14
Turn on : 27.8261
Width : 3.096
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

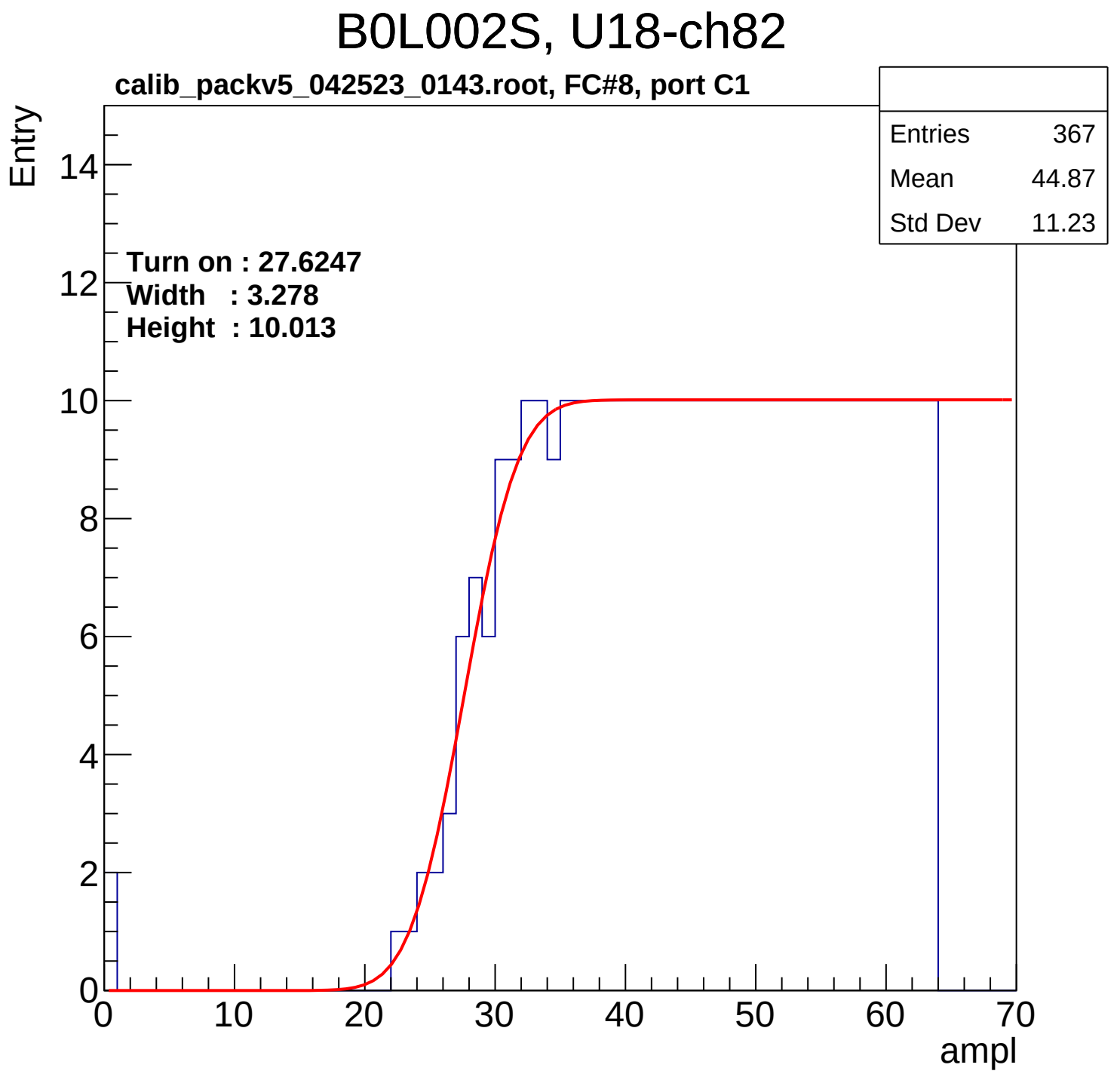

B0L002S, U18-ch77
calib_packv5_042523_0143.root, FC#8, port C1
Entries 374
Mean 44.54
Std Dev 11.38
Turn on : 26.6652
Width : 3.005
Height : 9.967
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

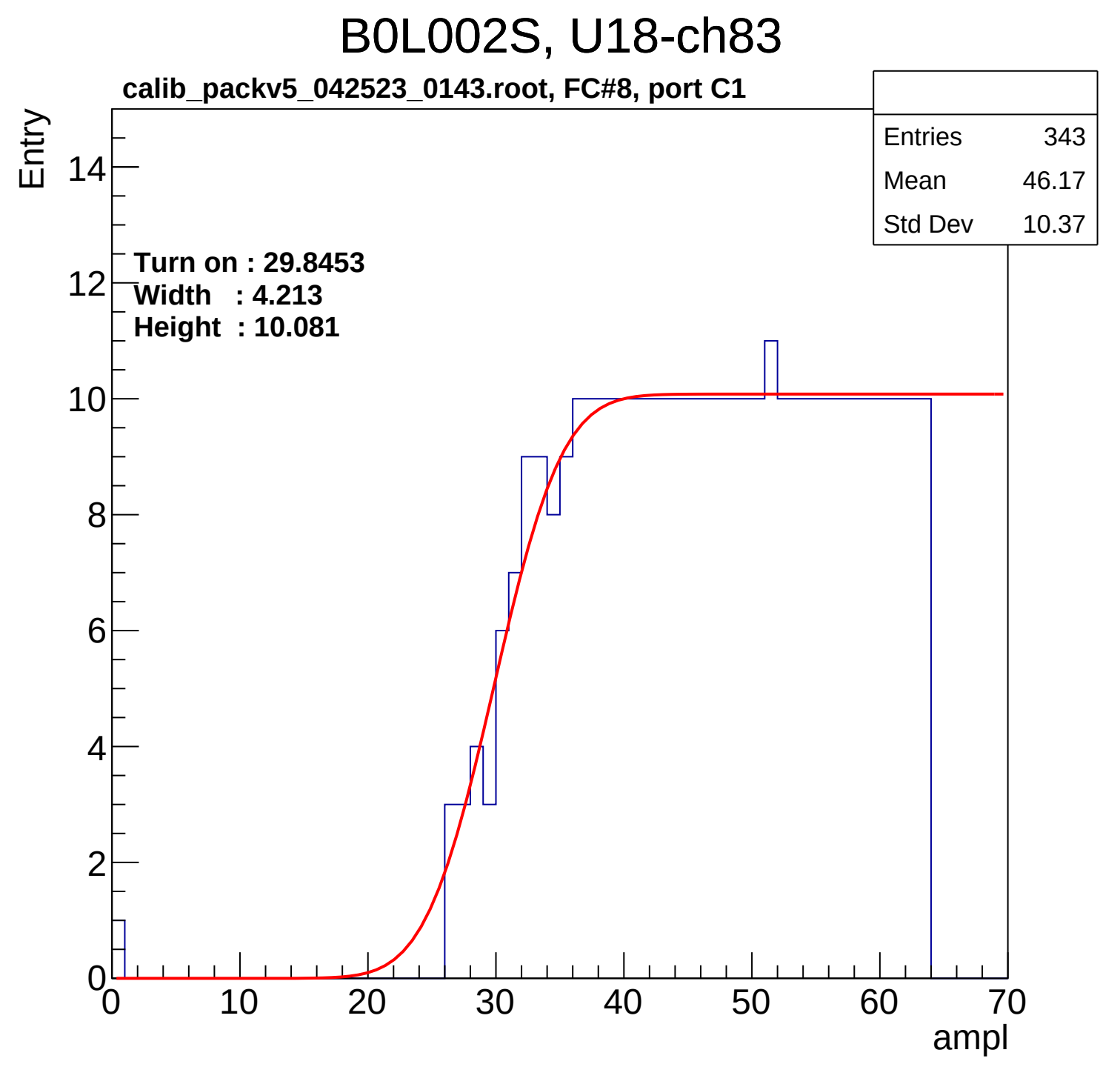

B0L002S, U18-ch78
calib_packv5_042523_0143.root, FC#8, port C1
Entries 380
Mean 44.13
Std Dev 11.8
Turn on : 28.2238
Width : 3.910
Height : 10.131
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

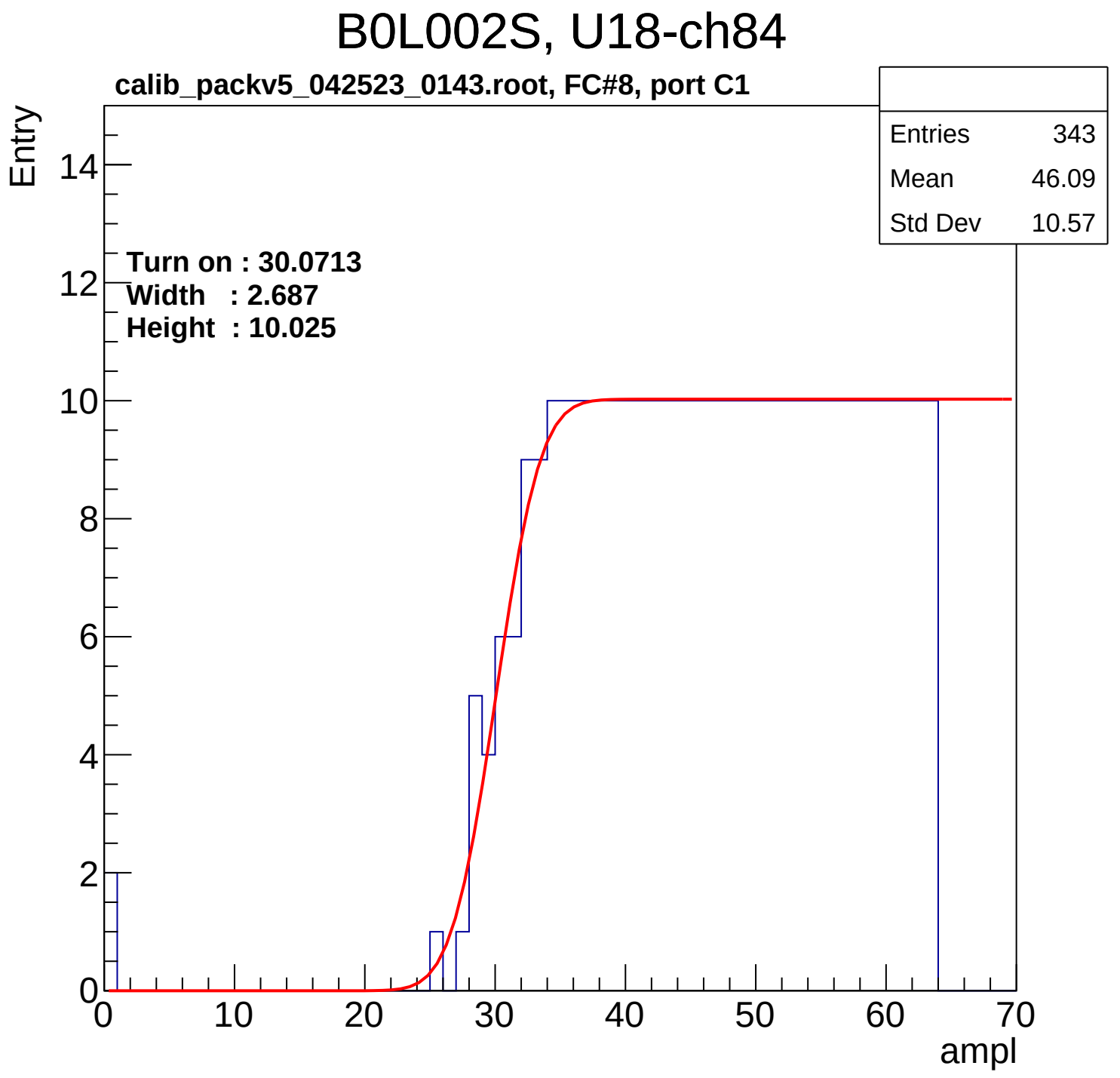

B0L002S, U18-ch79
calib_packv5_042523_0143.root, FC#8, port C1
Entries 366
Mean 44.89
Std Dev 11.35
Turn on : 28.0889
Width : 2.959
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

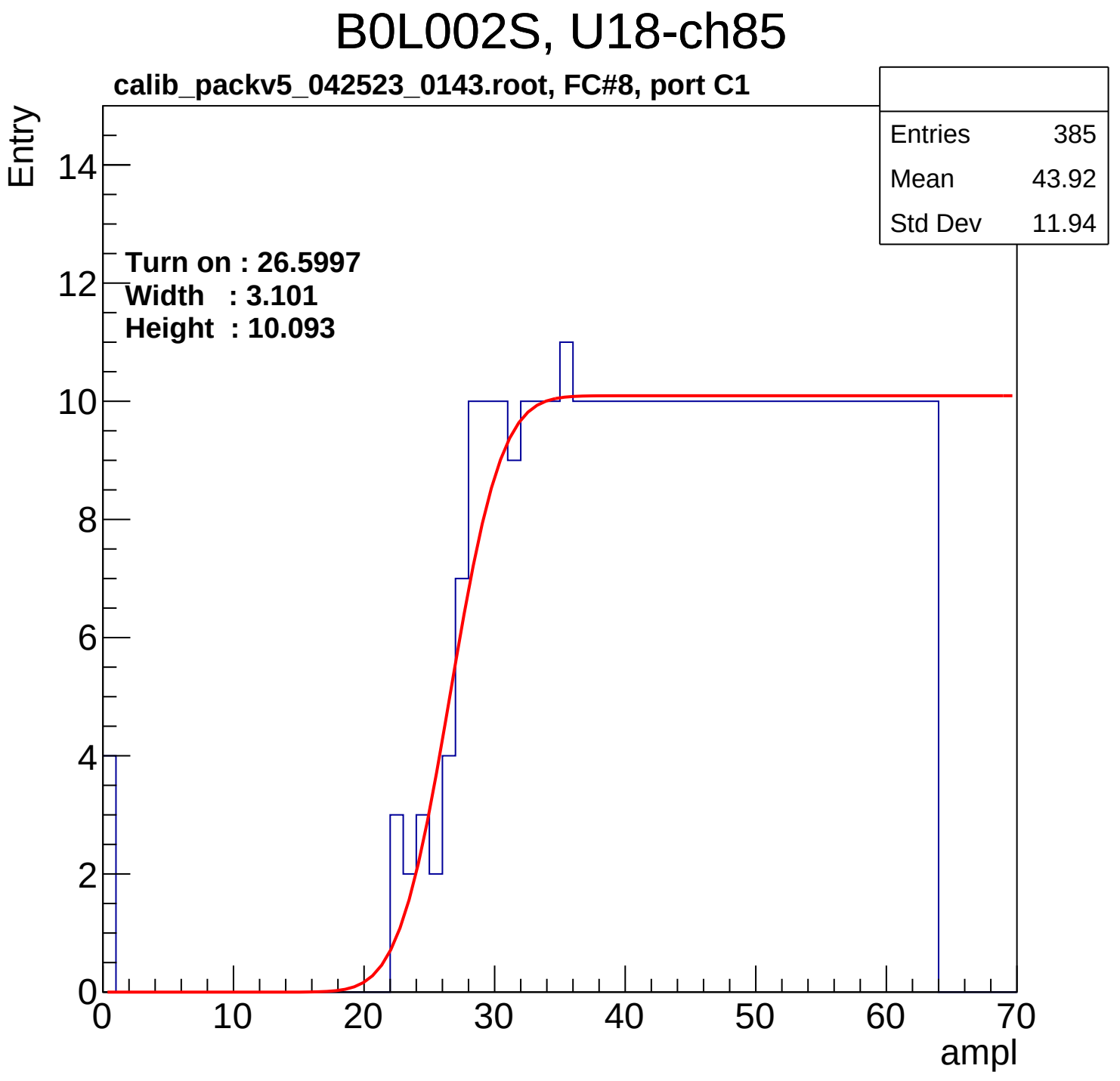

B0L002S, U18-ch80
calib_packv5_042523_0143.root, FC#8, port C1
Entries 376
Mean 44.33
Std Dev 11.77
Turn on : 27.0380
Width : 2.962
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

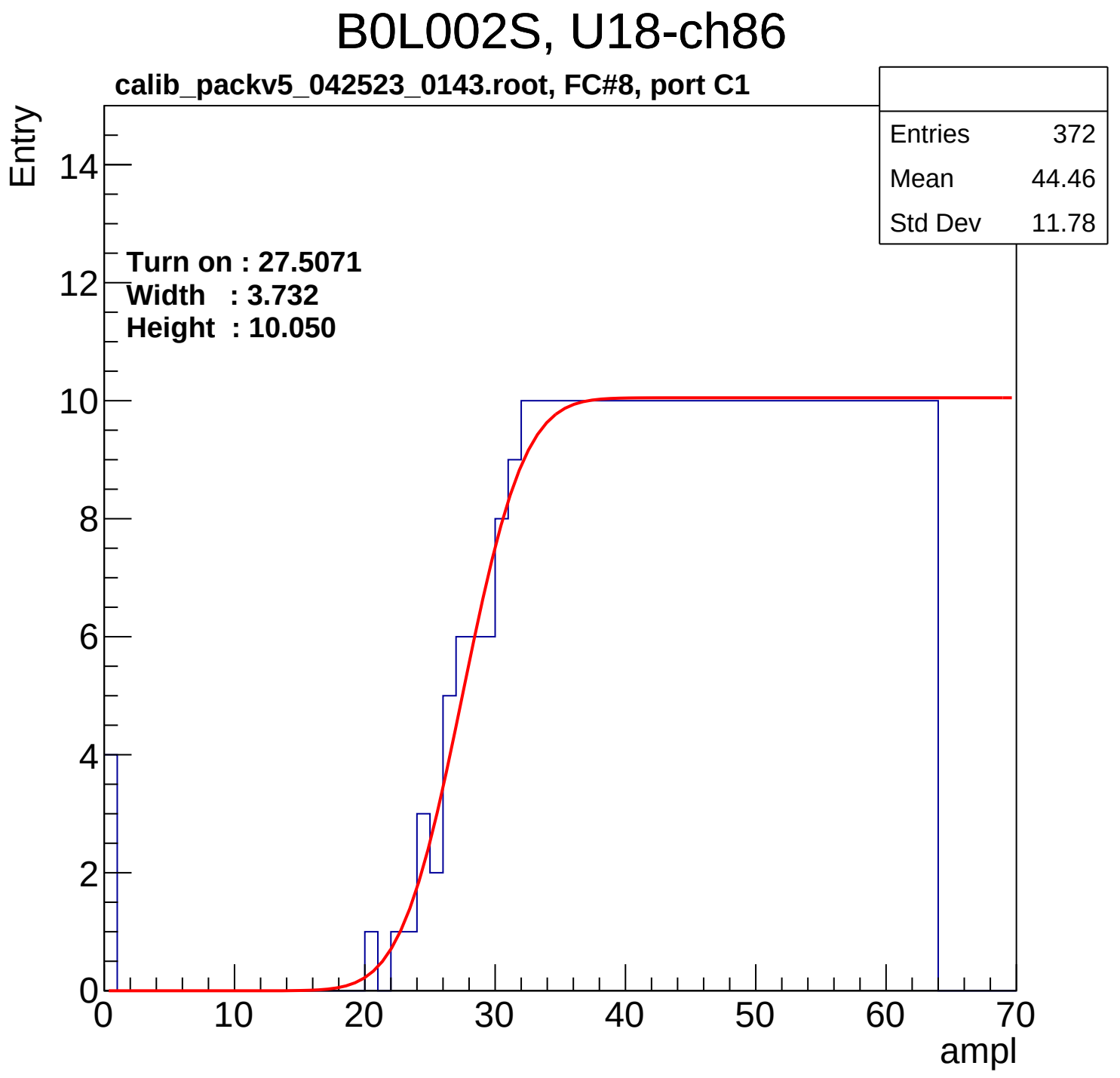

B0L002S, U18-ch81
calib_packv5_042523_0143.root, FC#8, port C1
Entries 363
Mean 45.06
Std Dev 11.15
Turn on : 28.5969
Width : 3.104
Height : 10.040
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

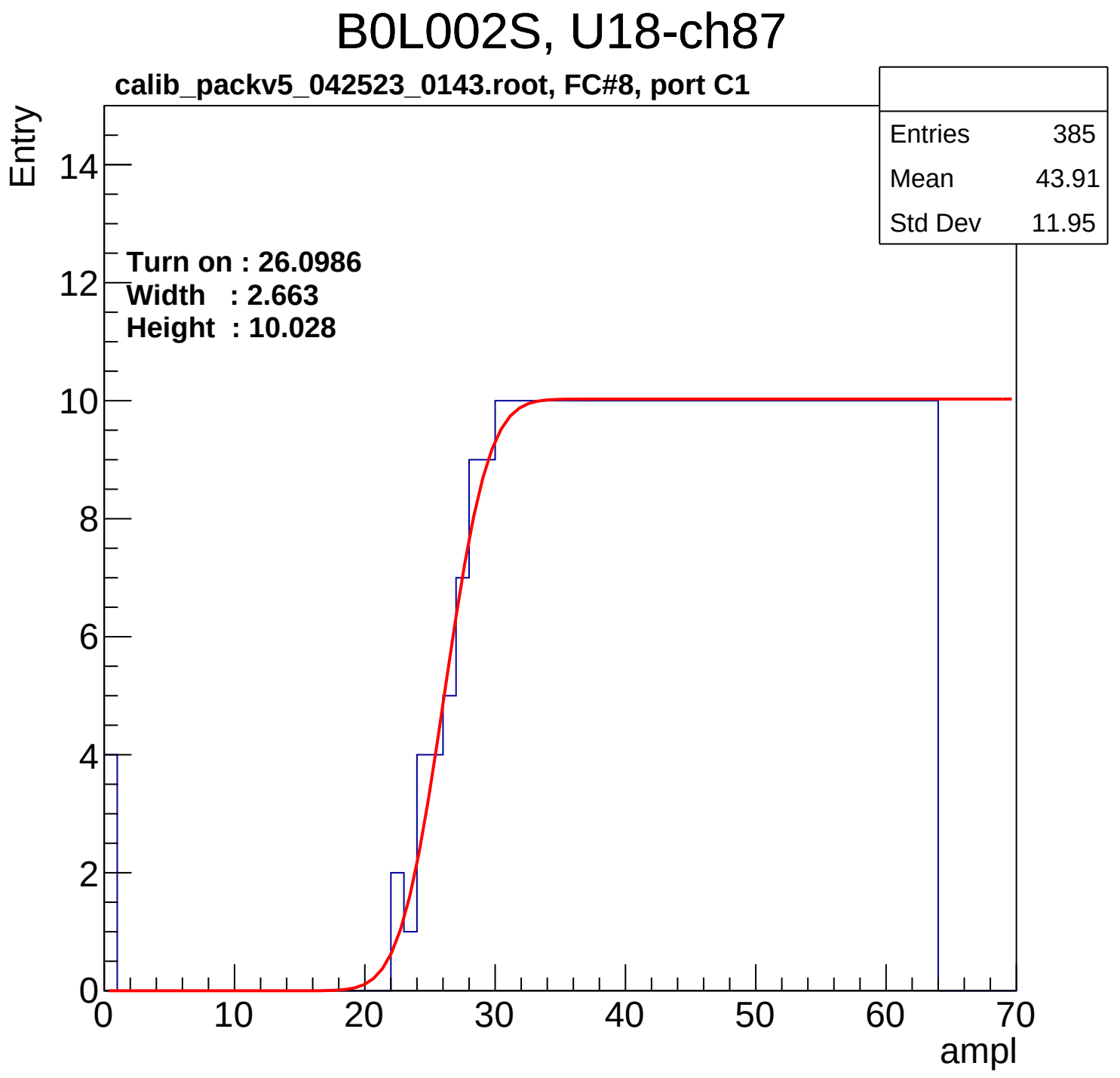

B0L002S, U18-ch82
calib_packv5_042523_0143.root, FC#8, port C1
Entries 367
Mean 44.87
Std Dev 11.23
Turn on : 27.6247
Width : 3.278
Height : 10.013
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

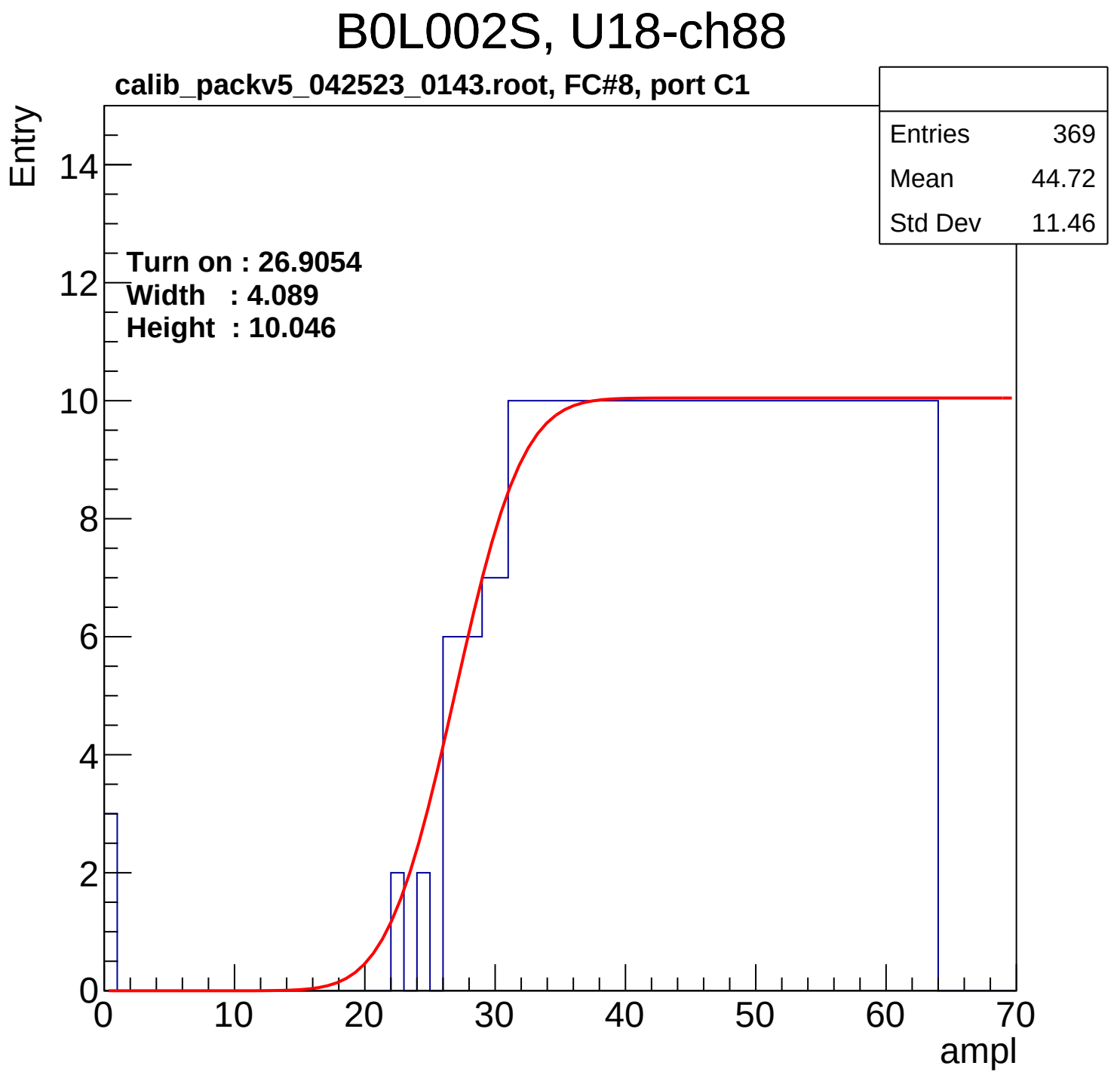

B0L002S, U18-ch83
calib_packv5_042523_0143.root, FC#8, port C1
Entries 343
Mean 46.17
Std Dev 10.37
Turn on : 29.8453
Width : 4.213
Height : 10.081
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

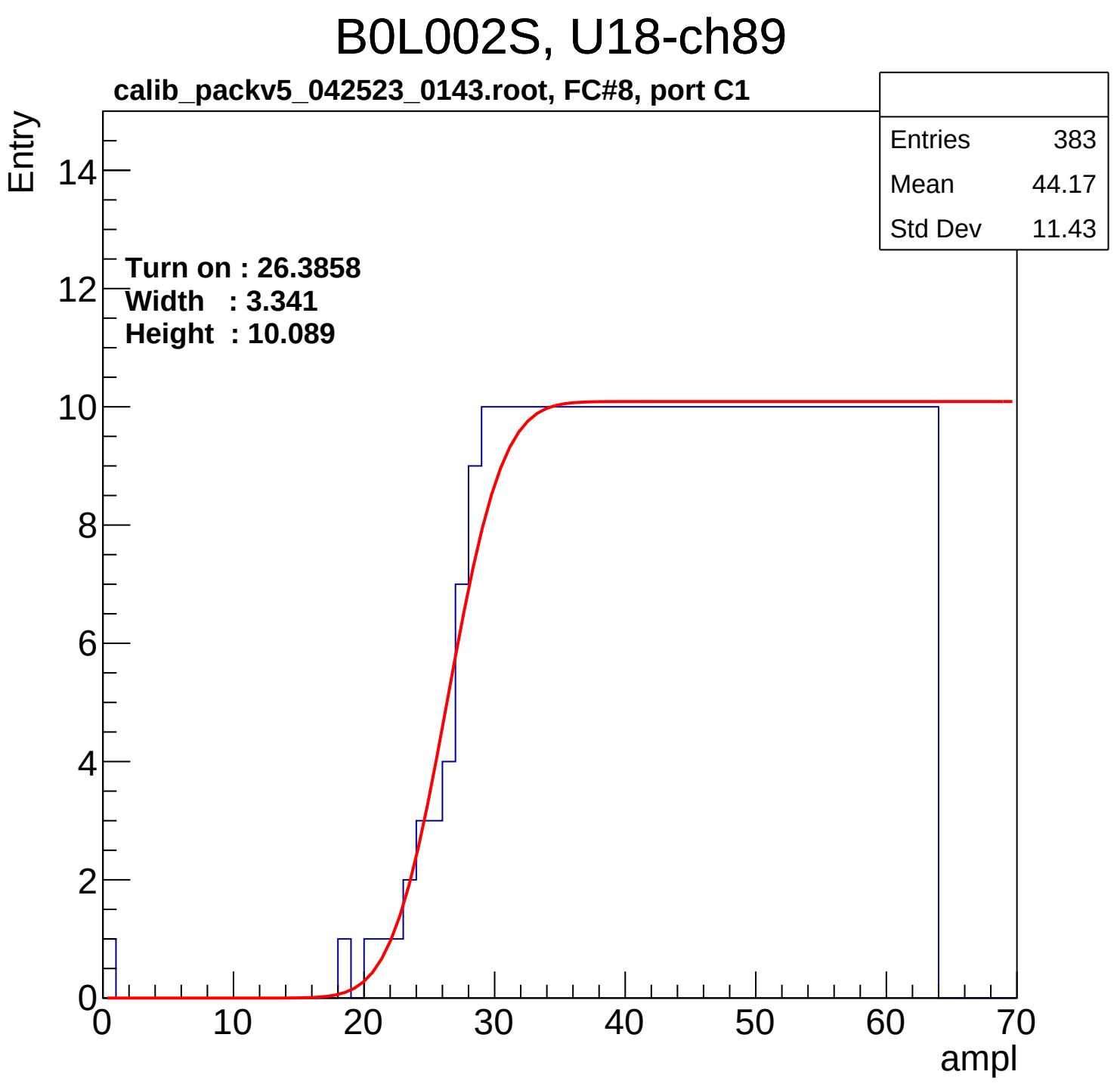

B0L002S, U18-ch84
calib_packv5_042523_0143.root, FC#8, port C1
Entries 343
Mean 46.09
Std Dev 10.57
Turn on : 30.0713
Width : 2.687
Height : 10.025
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

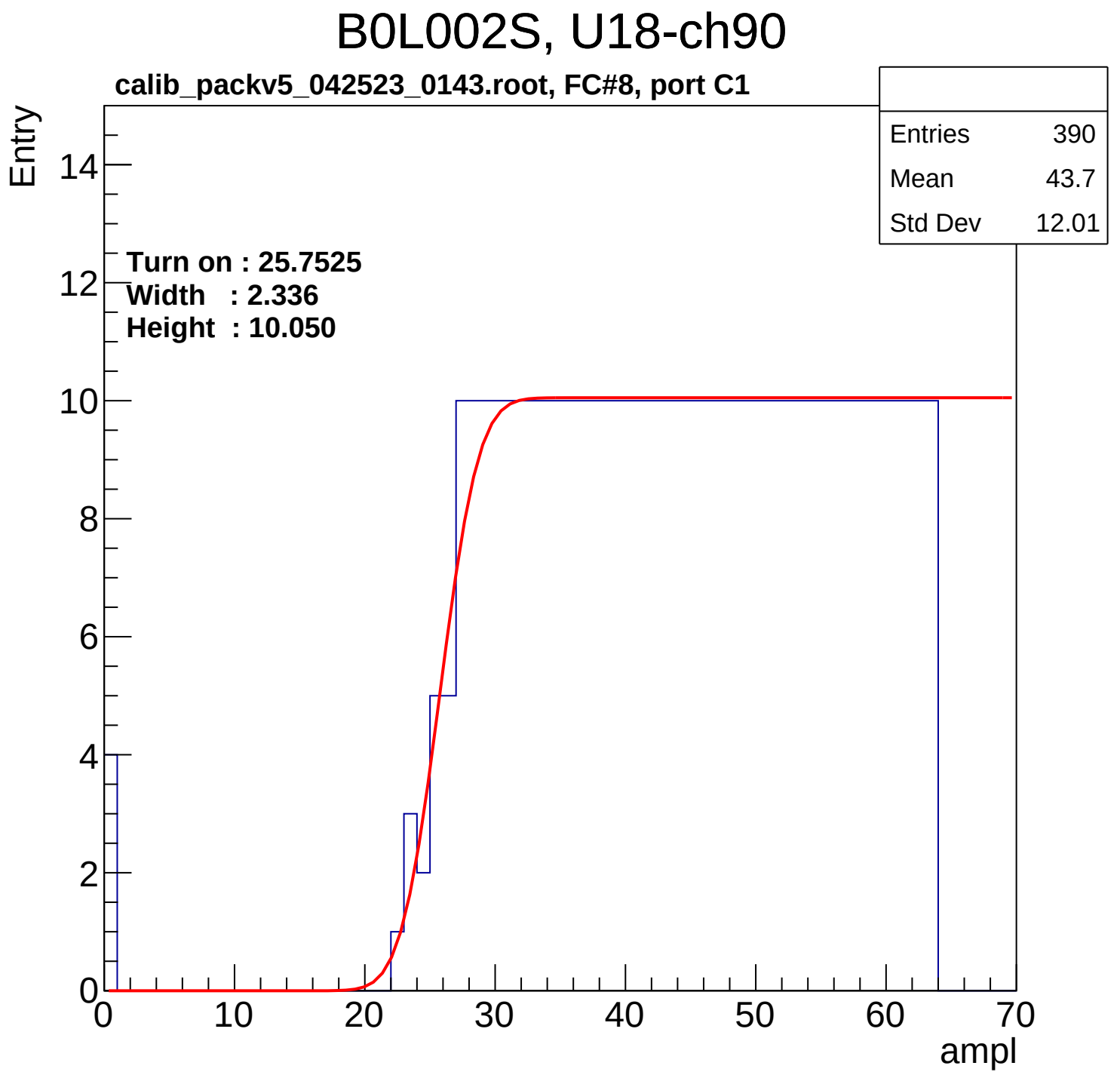

B0L002S, U18-ch85
calib_packv5_042523_0143.root, FC#8, port C1
Entries 385
Mean 43.92
Std Dev 11.94
Turn on : 26.5997
Width : 3.101
Height : 10.093
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

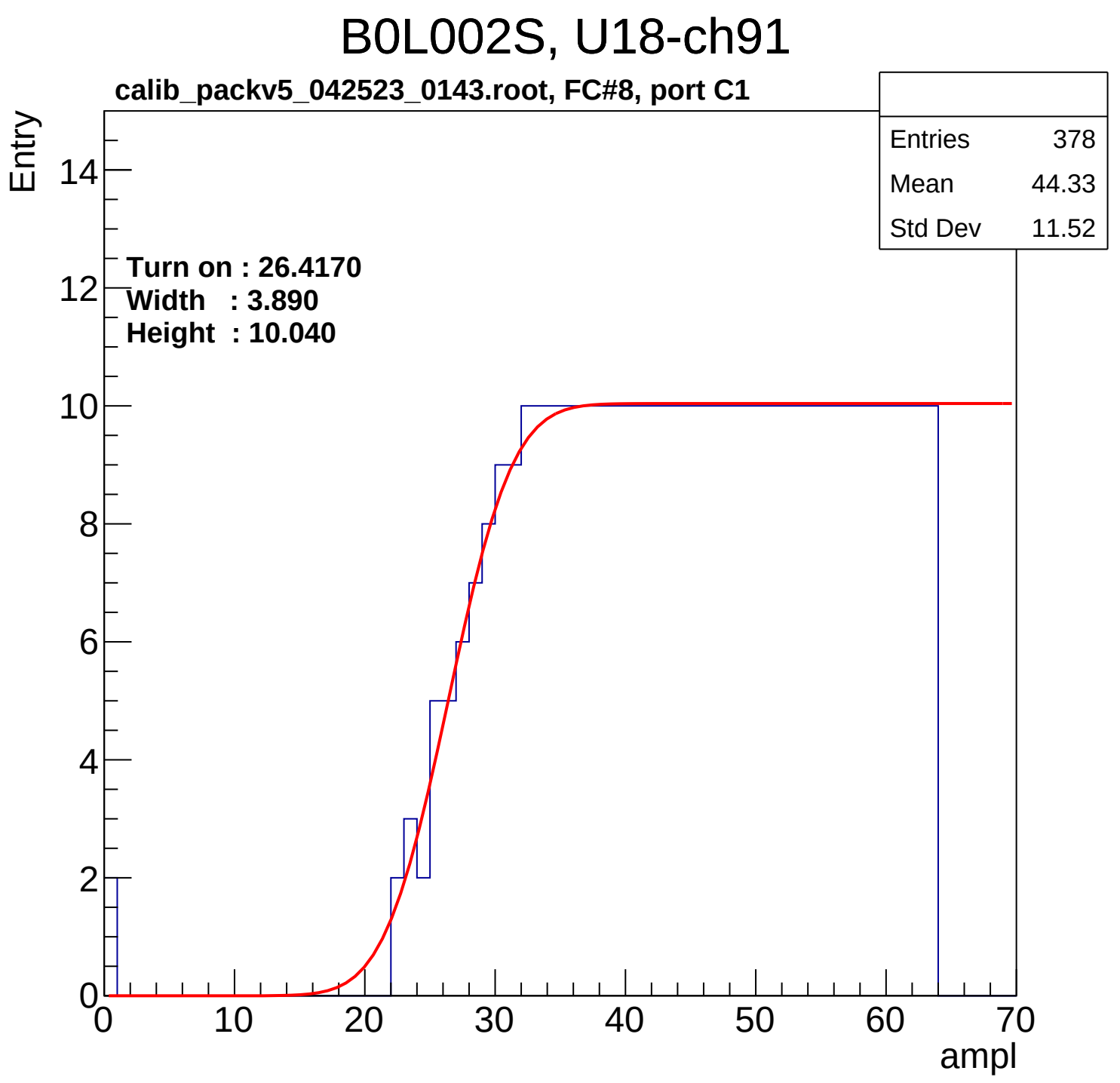

B0L002S, U18-ch86
calib_packv5_042523_0143.root, FC#8, port C1
Entries 372
Mean 44.46
Std Dev 11.78
Turn on : 27.5071
Width : 3.732
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

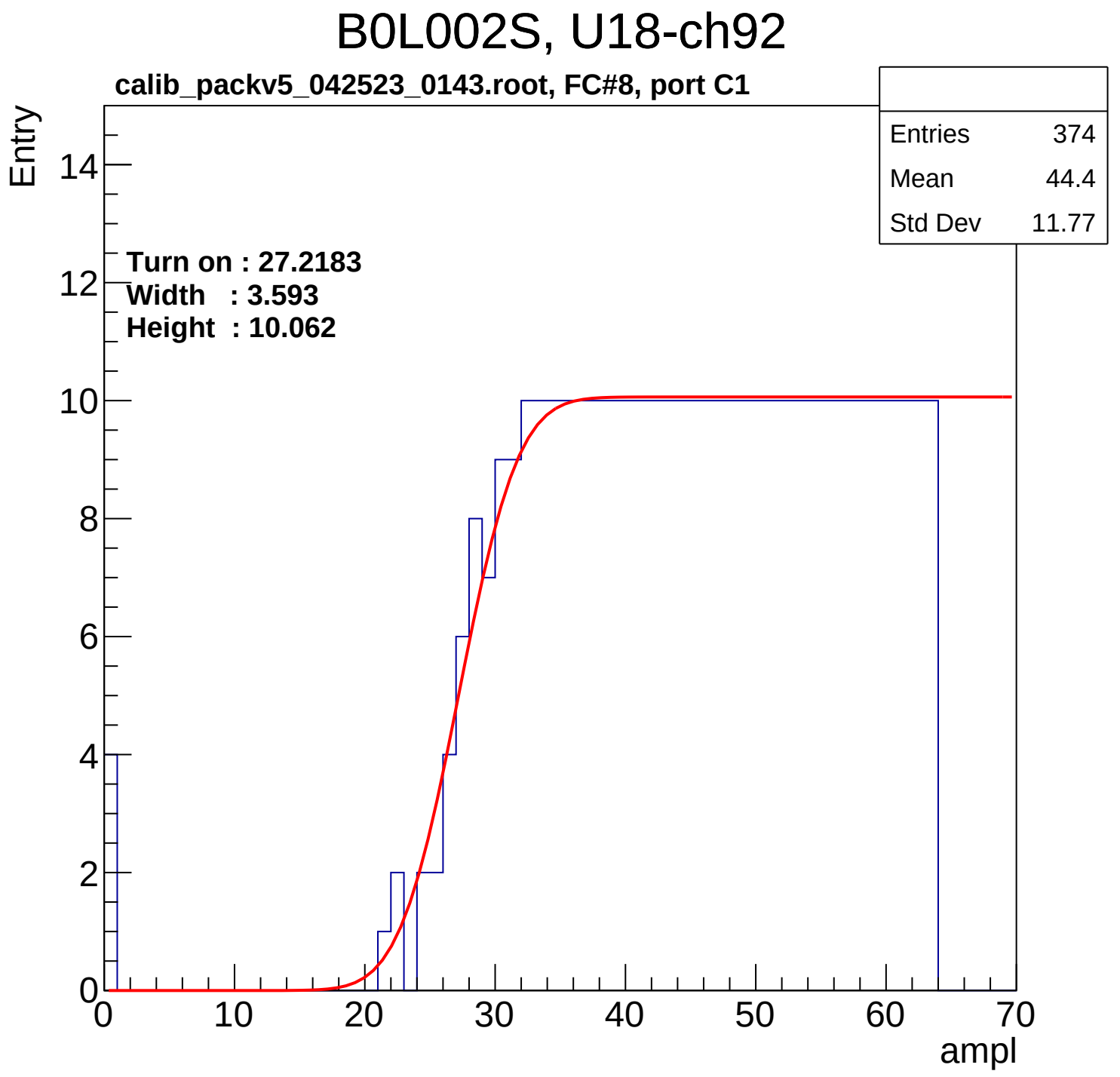

B0L002S, U18-ch87
calib_packv5_042523_0143.root, FC#8, port C1
Entries 385
Mean 43.91
Std Dev 11.95
Turn on : 26.0986
Width : 2.663
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

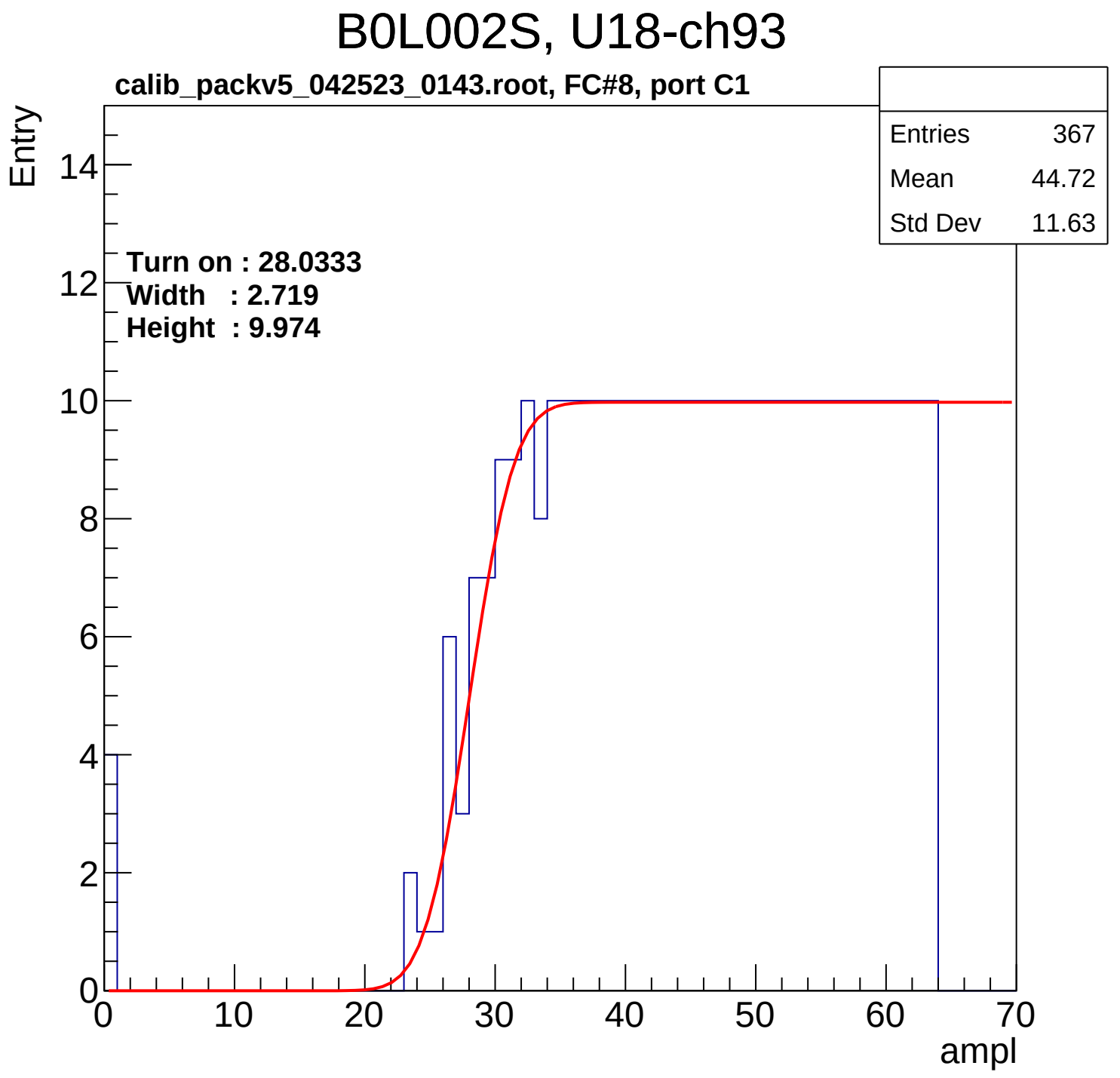

B0L002S, U18-ch88
calib_packv5_042523_0143.root, FC#8, port C1
Entries 369
Mean 44.72
Std Dev 11.46
Turn on : 26.9054
Width : 4.089
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

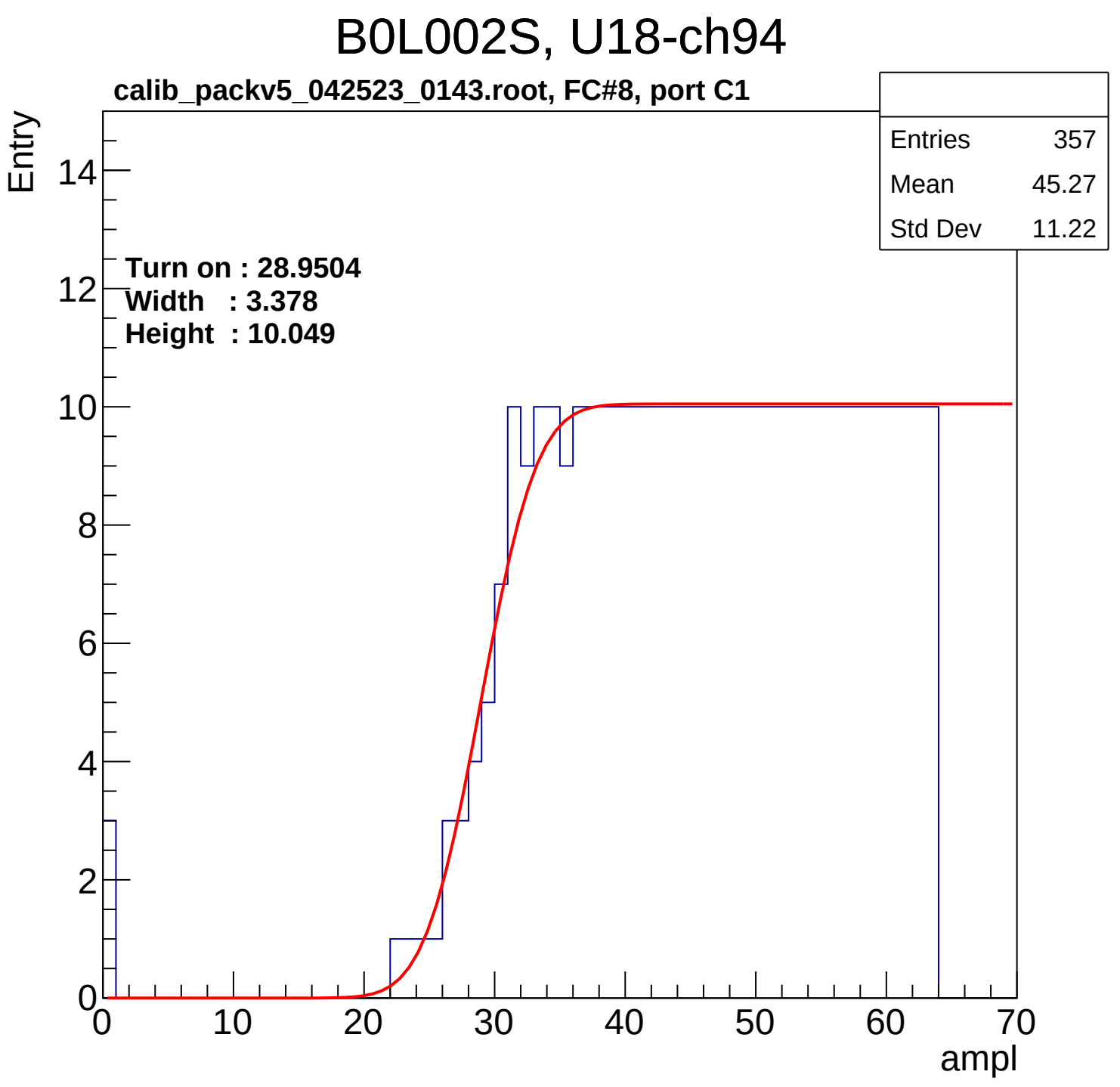

B0L002S, U18-ch89
calib_packv5_042523_0143.root, FC#8, port C1
Entries 383
Mean 44.17
Std Dev 11.43
Turn on : 26.3858
Width : 3.341
Height : 10.089
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

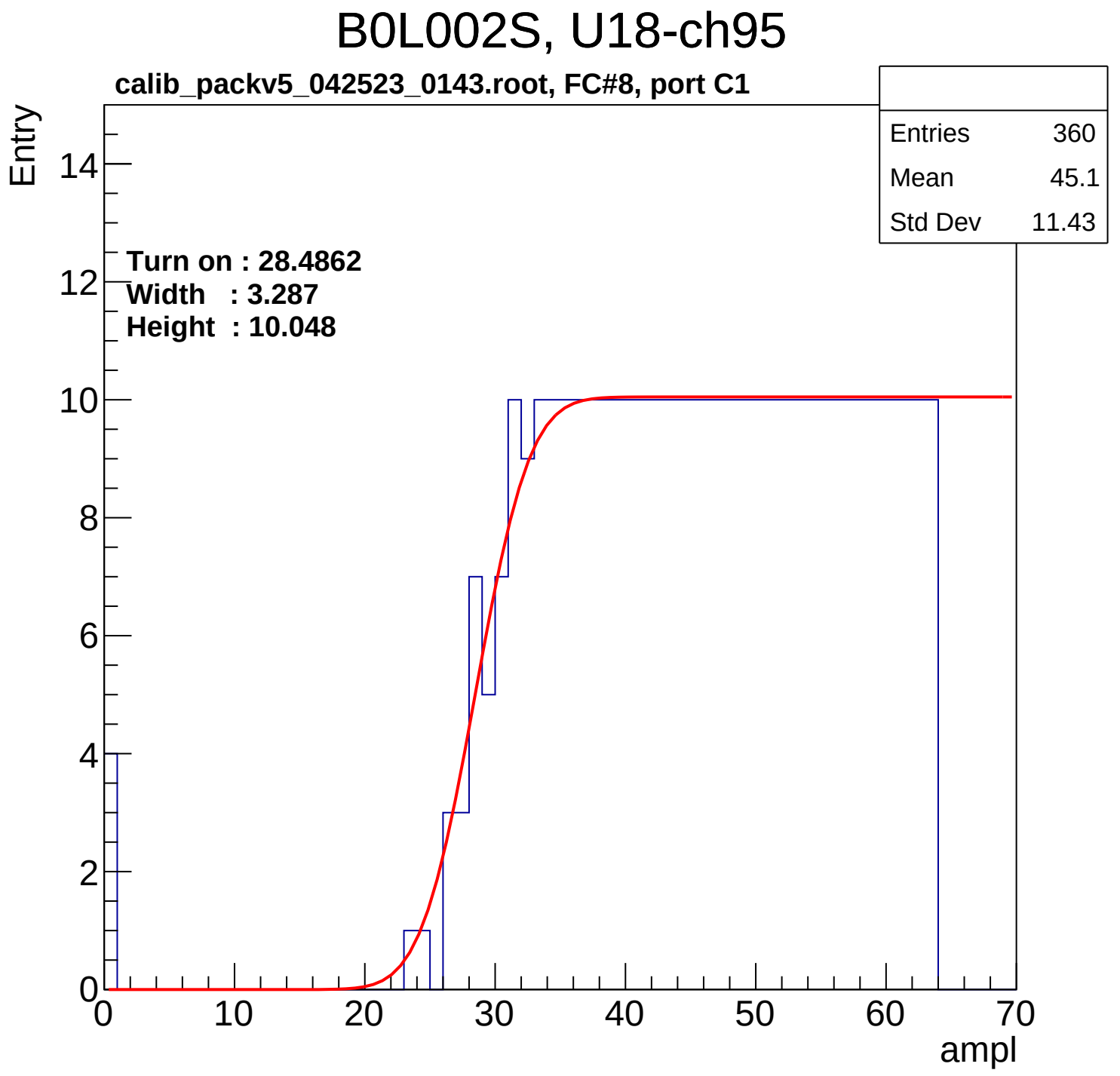

B0L002S, U18-ch90
calib_packv5_042523_0143.root, FC#8, port C1
Entries 390
Mean 43.7
Std Dev 12.01
Turn on : 25.7525
Width : 2.336
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

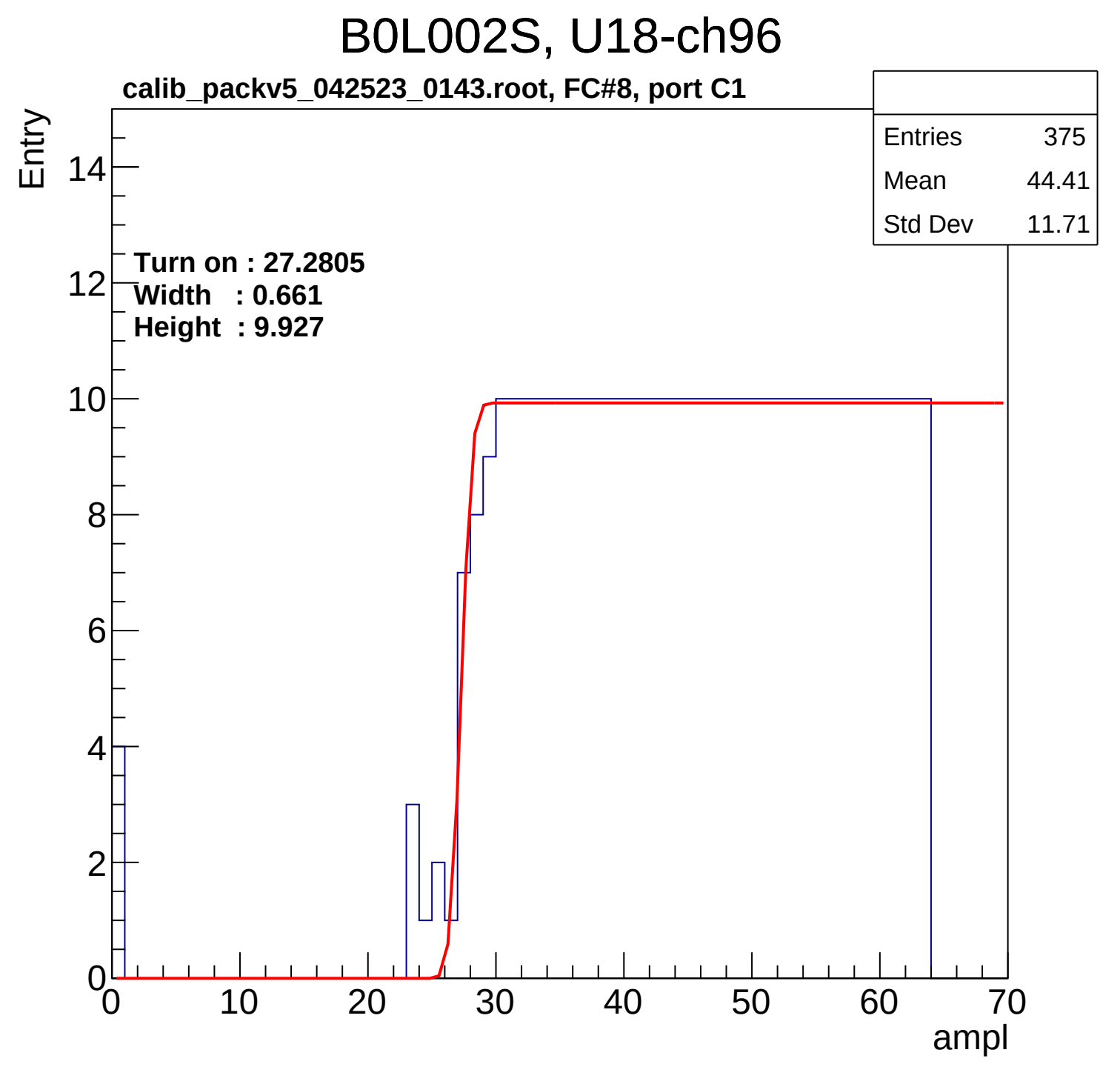

B0L002S, U18-ch91
calib_packv5_042523_0143.root, FC#8, port C1
Entries 378
Mean 44.33
Std Dev 11.52
Turn on : 26.4170
Width : 3.890
Height : 10.040
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

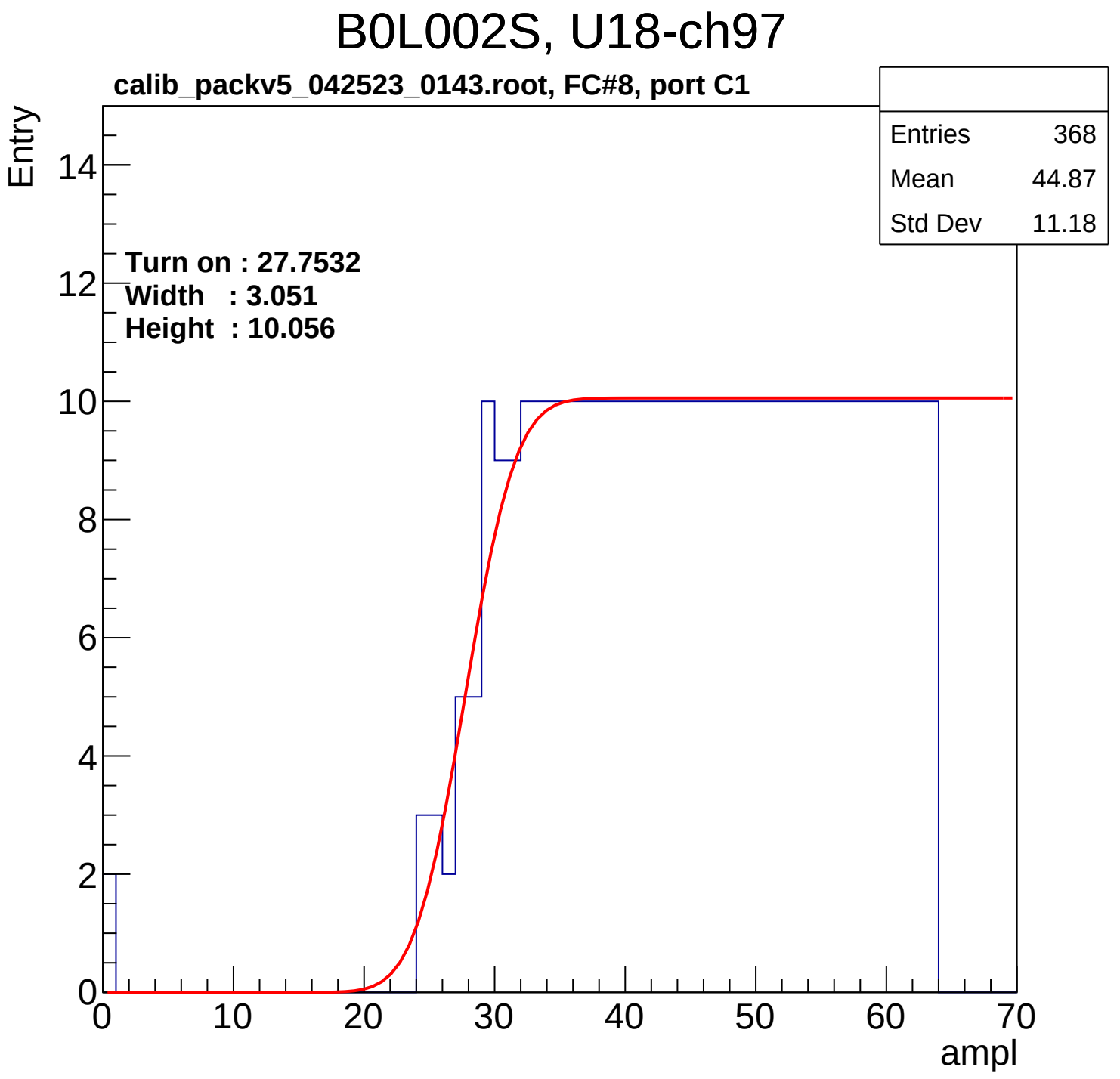

B0L002S, U18-ch92
calib_packv5_042523_0143.root, FC#8, port C1
Entries 374
Mean 44.4
Std Dev 11.77
Turn on : 27.2183
Width : 3.593
Height : 10.062
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

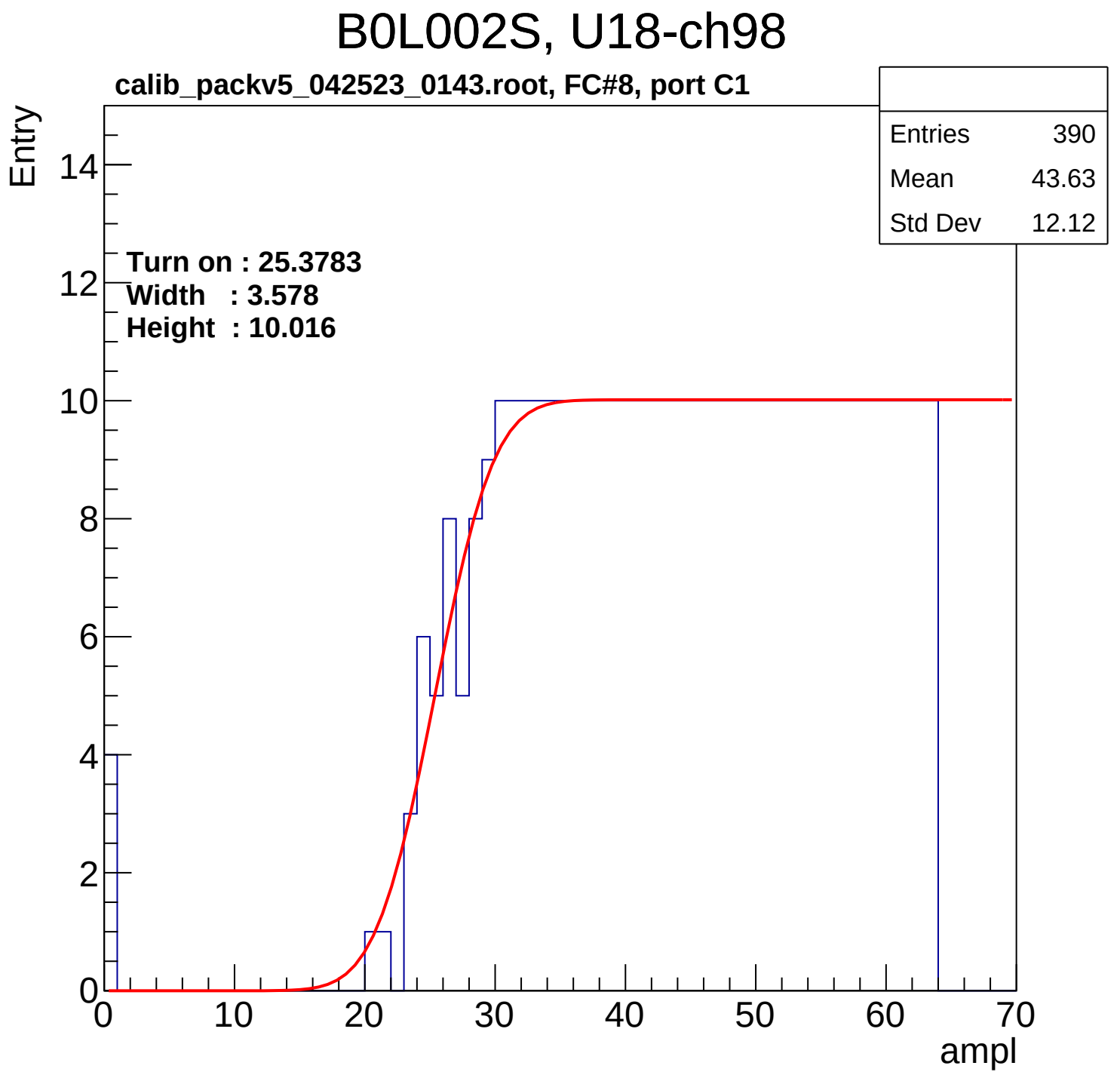

B0L002S, U18-ch93
calib_packv5_042523_0143.root, FC#8, port C1
Entries 367
Mean 44.72
Std Dev 11.63
Turn on : 28.0333
Width : 2.719
Height : 9.974
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

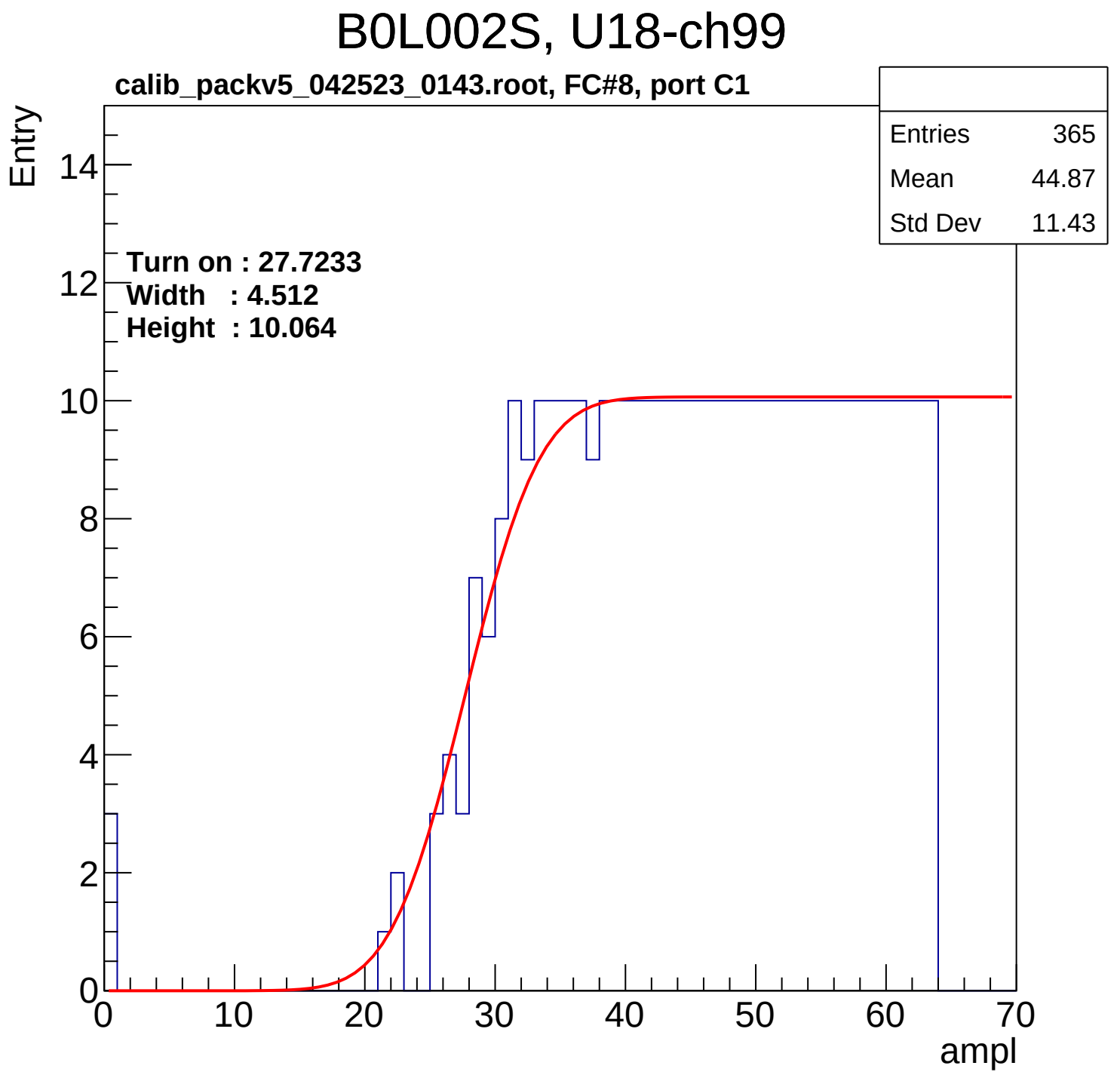

B0L002S, U18-ch94
calib_packv5_042523_0143.root, FC#8, port C1
Entries 357
Mean 45.27
Std Dev 11.22
Turn on : 28.9504
Width : 3.378
Height : 10.049
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

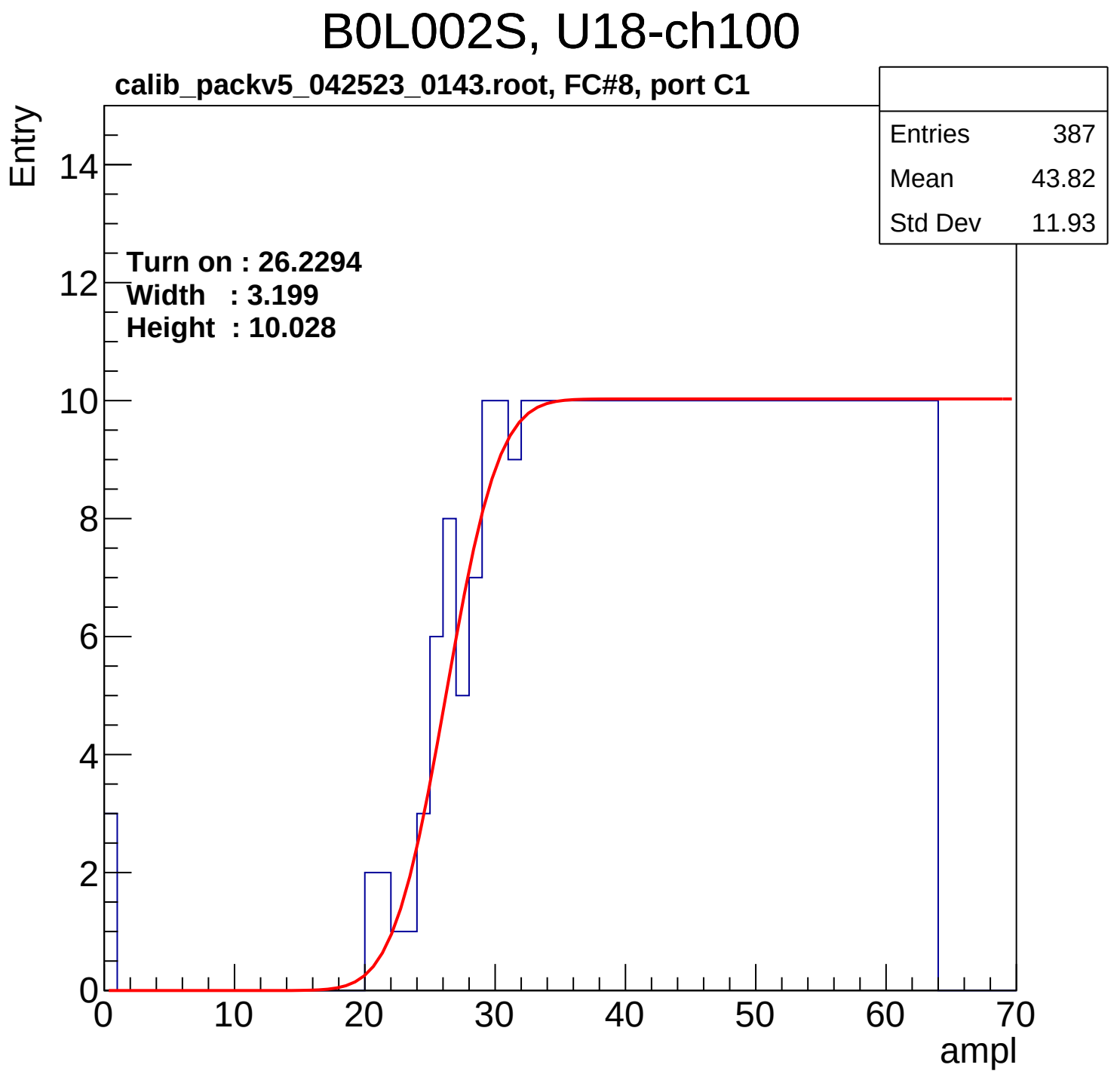

B0L002S, U18-ch95
calib_packv5_042523_0143.root, FC#8, port C1
Entries 360
Mean 45.1
Std Dev 11.43
Turn on : 28.4862
Width : 3.287
Height : 10.048
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

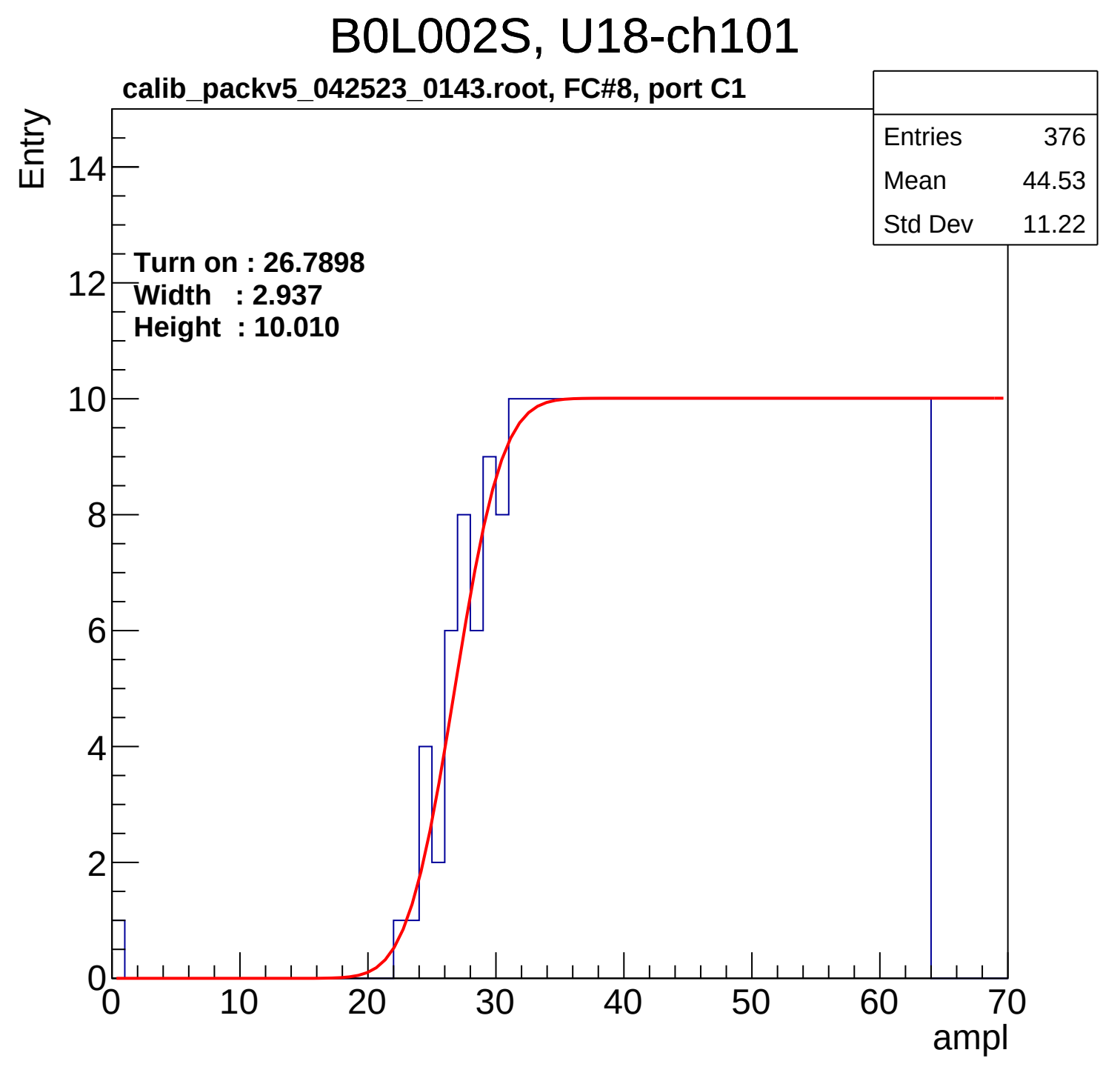

B0L002S, U18-ch96
calib_packv5_042523_0143.root, FC#8, port C1
Entries 375
Mean 44.41
Std Dev 11.71
Turn on : 27.2805
Width : 0.661
Height : 9.927
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

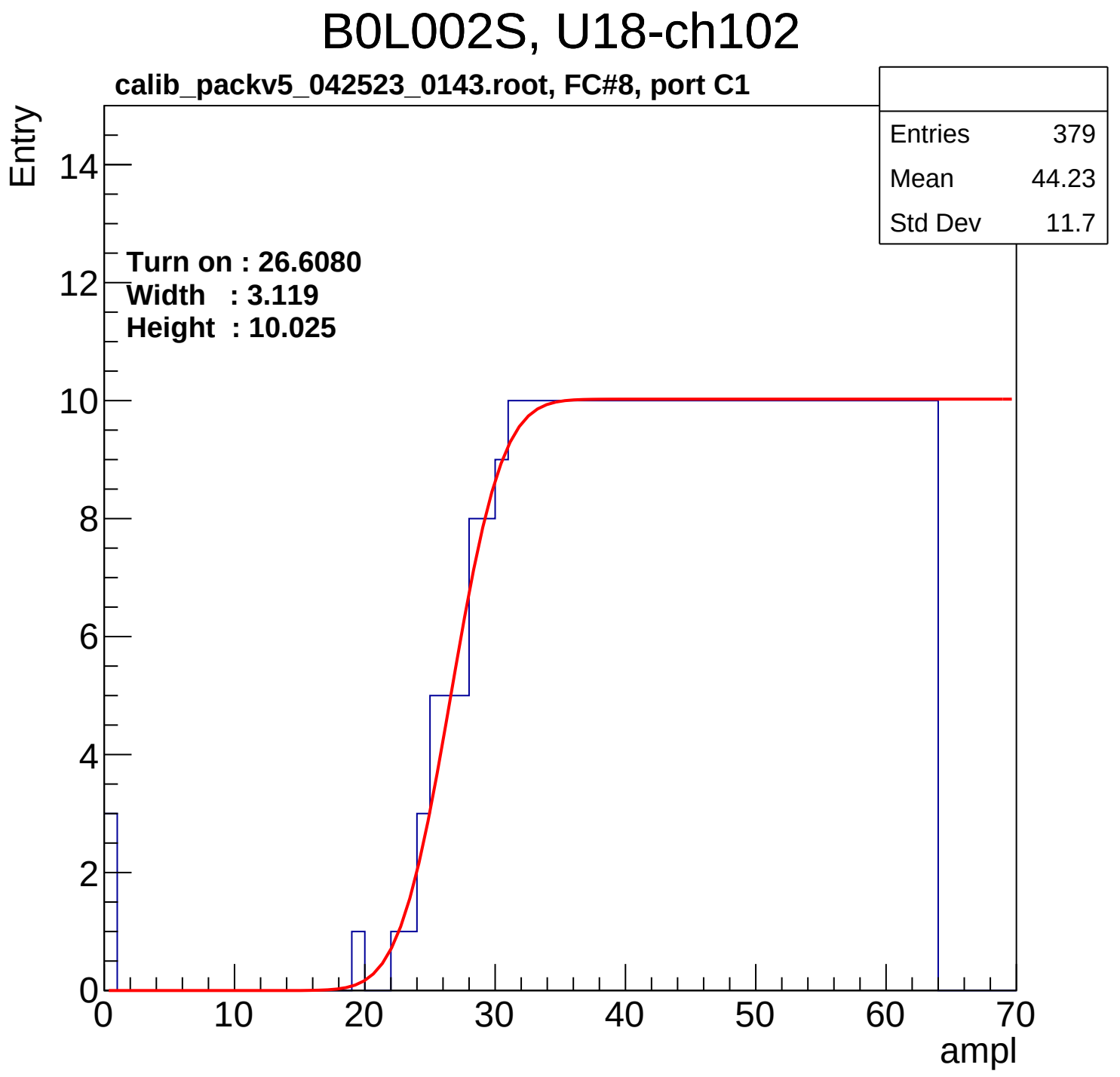

B0L002S, U18-ch97
calib_packv5_042523_0143.root, FC#8, port C1
Entries 368
Mean 44.87
Std Dev 11.18
Turn on : 27.7532
Width : 3.051
Height : 10.056
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

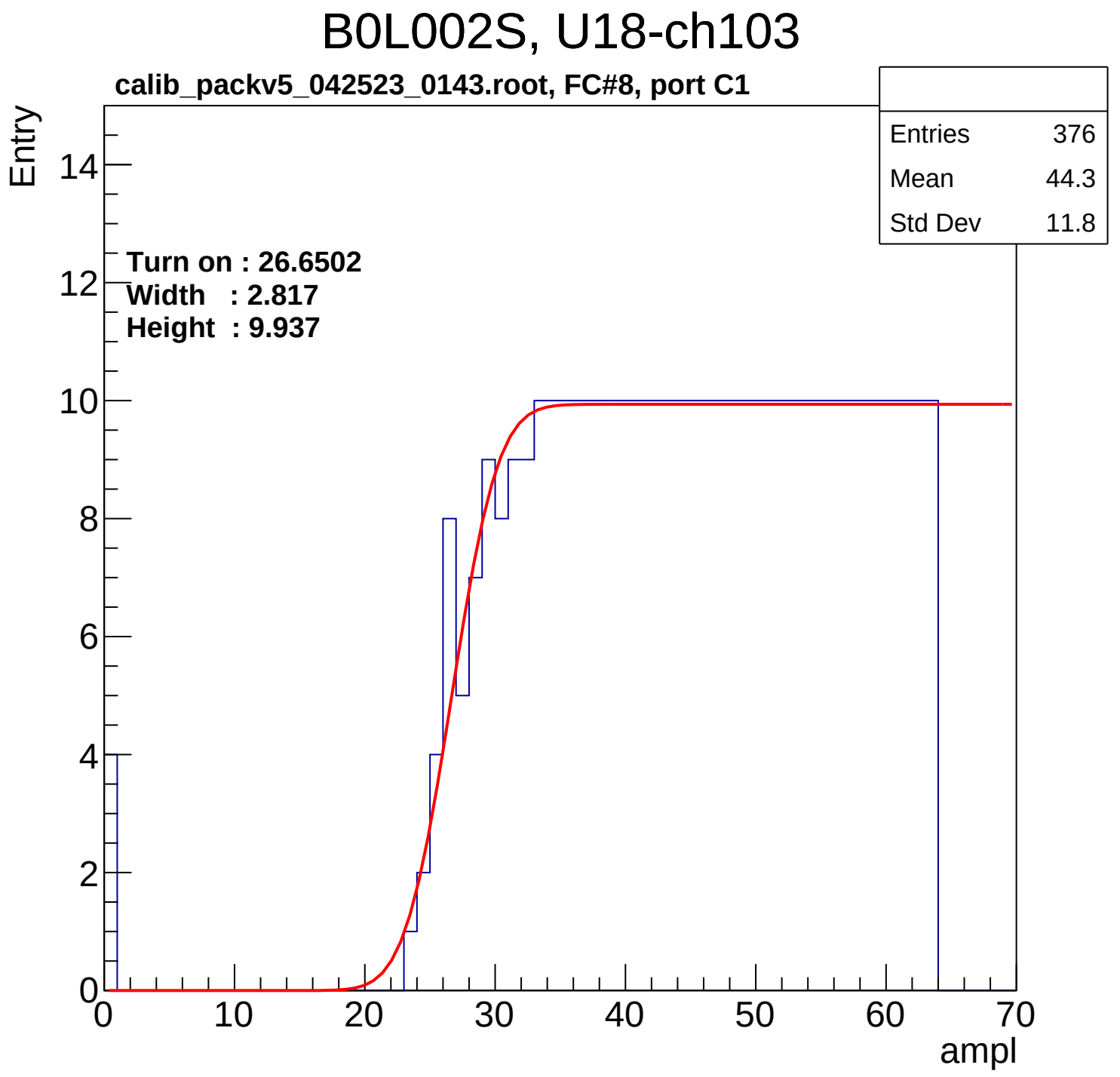

B0L002S, U18-ch98
calib_packv5_042523_0143.root, FC#8, port C1
Entries 390
Mean 43.63
Std Dev 12.12
Turn on : 25.3783
Width : 3.578
Height : 10.016
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

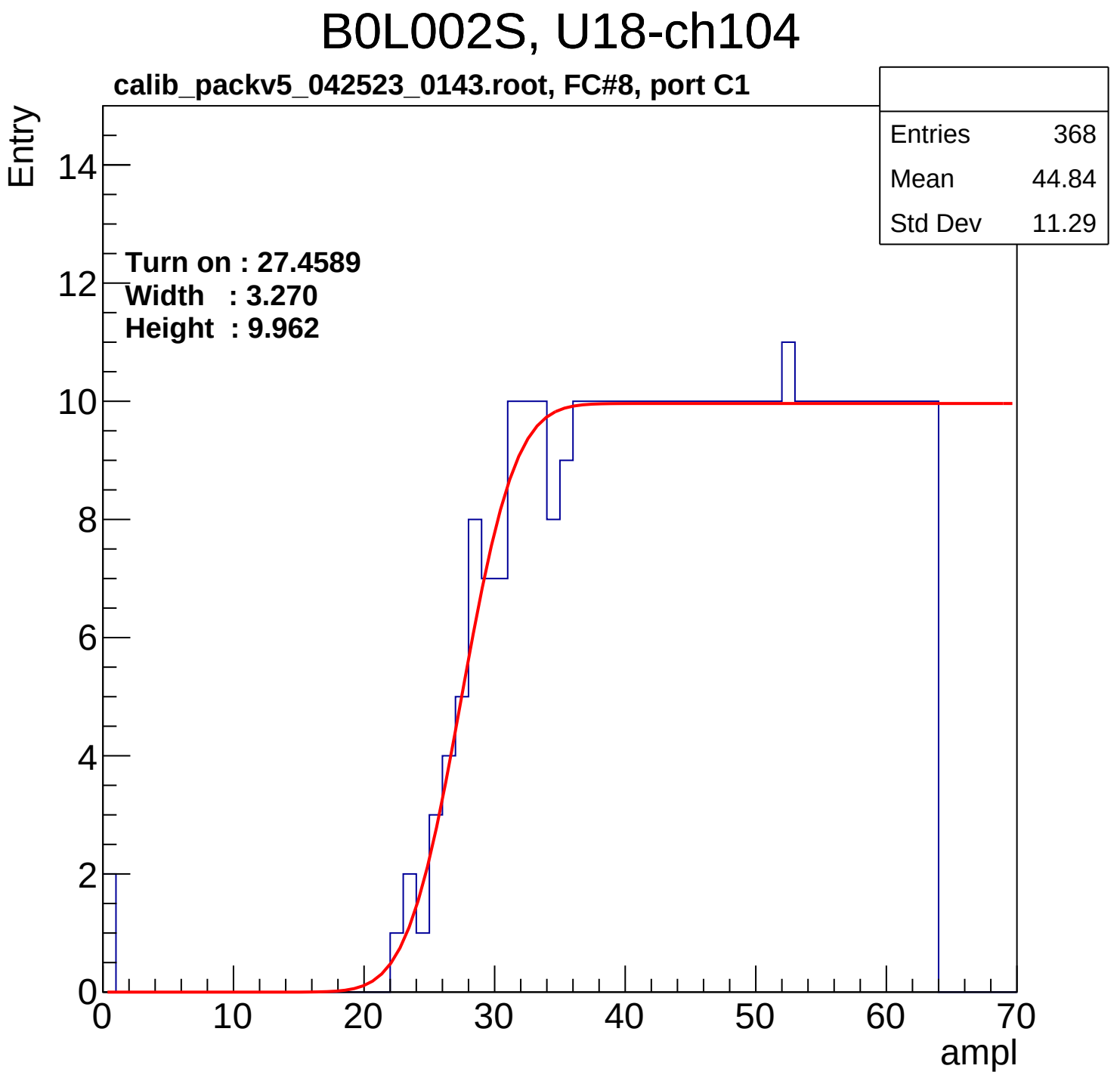

B0L002S, U18-ch99
calib_packv5_042523_0143.root, FC#8, port C1
Entries 365
Mean 44.87
Std Dev 11.43
Turn on : 27.7233
Width : 4.512
Height : 10.064
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

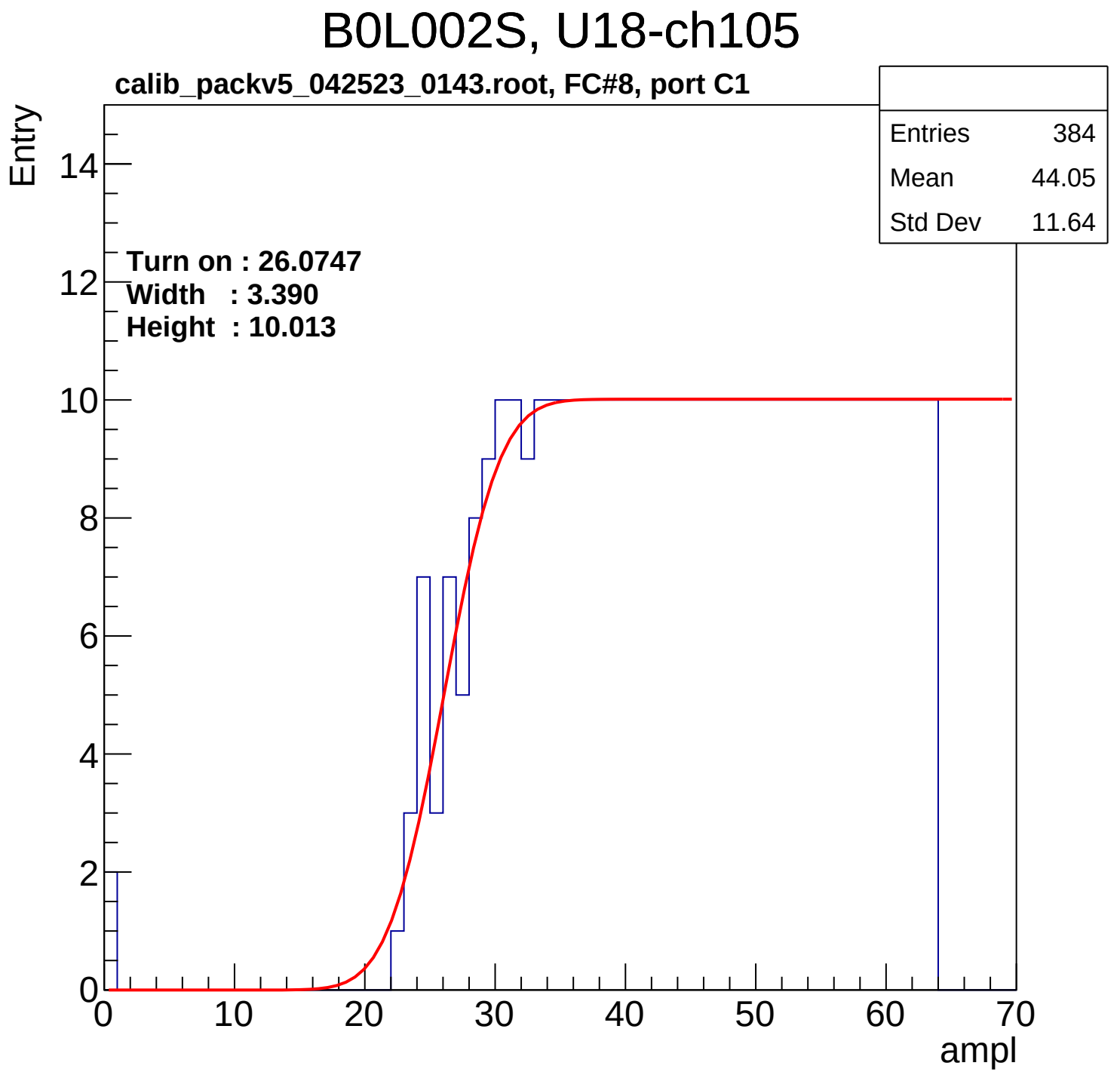

B0L002S, U18-ch100
calib_packv5_042523_0143.root, FC#8, port C1
Entries 387
Mean 43.82
Std Dev 11.93
Turn on : 26.2294
Width : 3.199
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

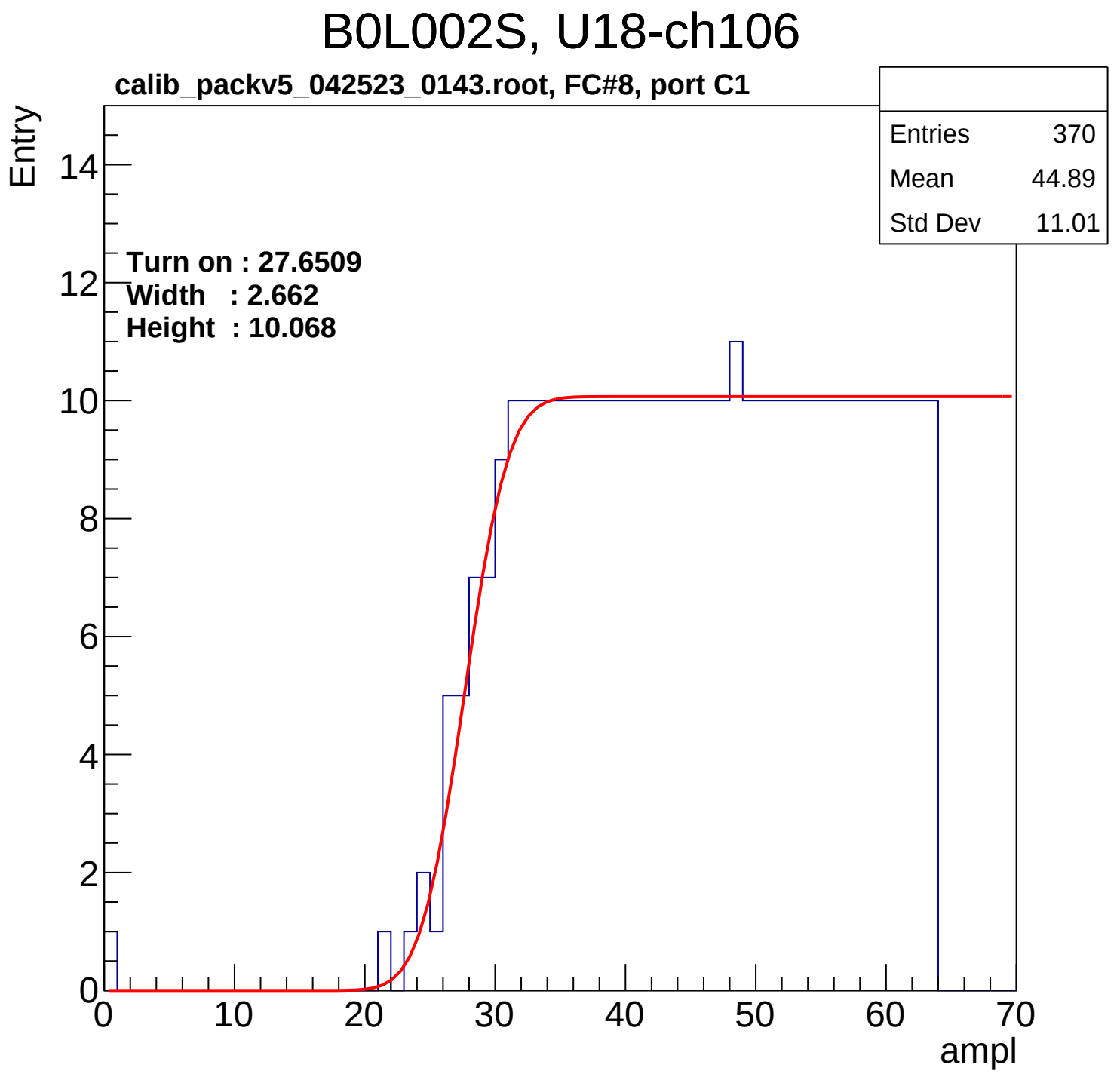

B0L002S, U18-ch101
calib_packv5_042523_0143.root, FC#8, port C1
Entries 376
Mean 44.53
Std Dev 11.22
Turn on : 26.7898
Width : 2.937
Height : 10.010
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

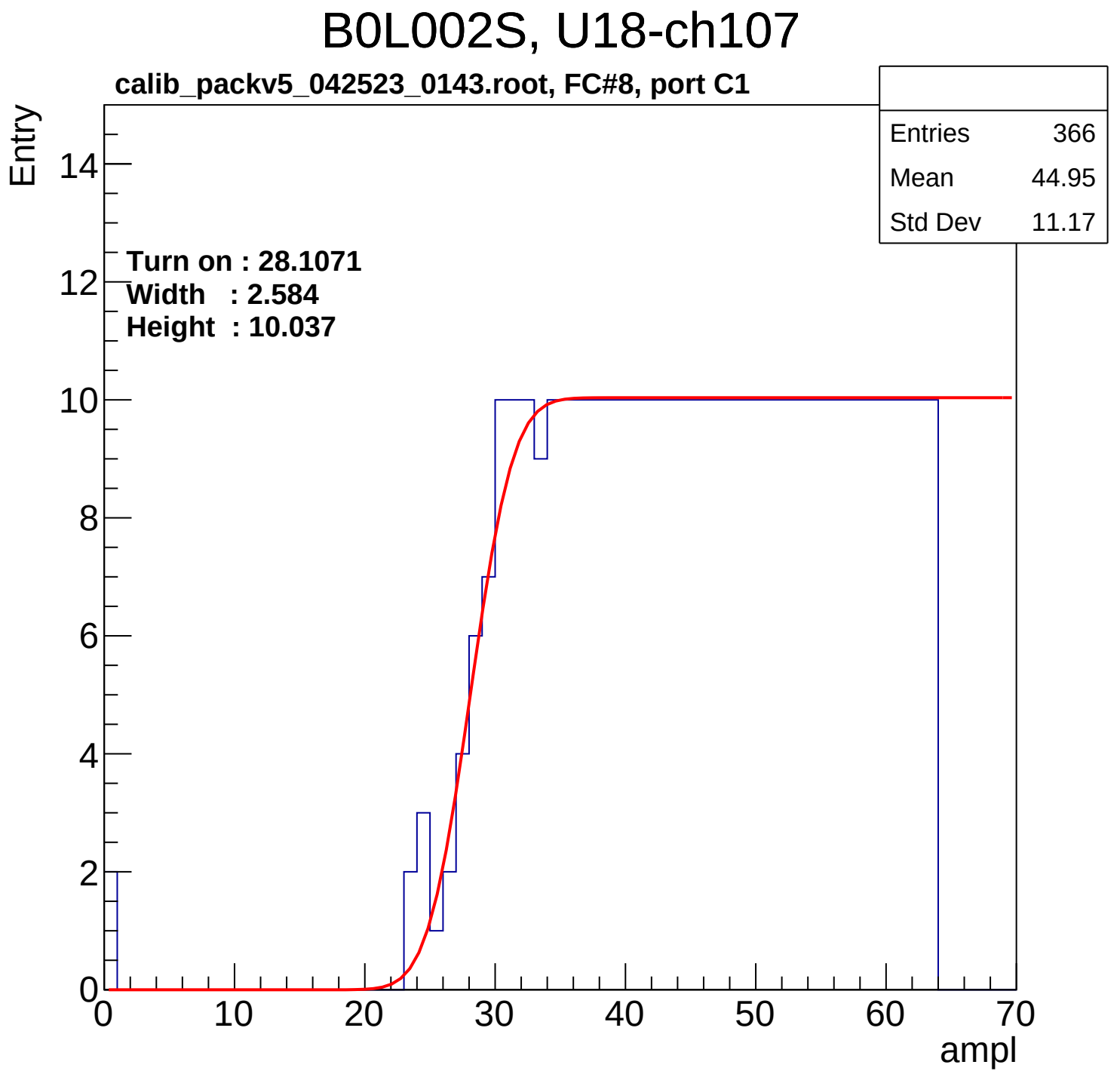

B0L002S, U18-ch102
calib_packv5_042523_0143.root, FC#8, port C1
Entries 379
Mean 44.23
Std Dev 11.7
Turn on : 26.6080
Width : 3.119
Height : 10.025
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

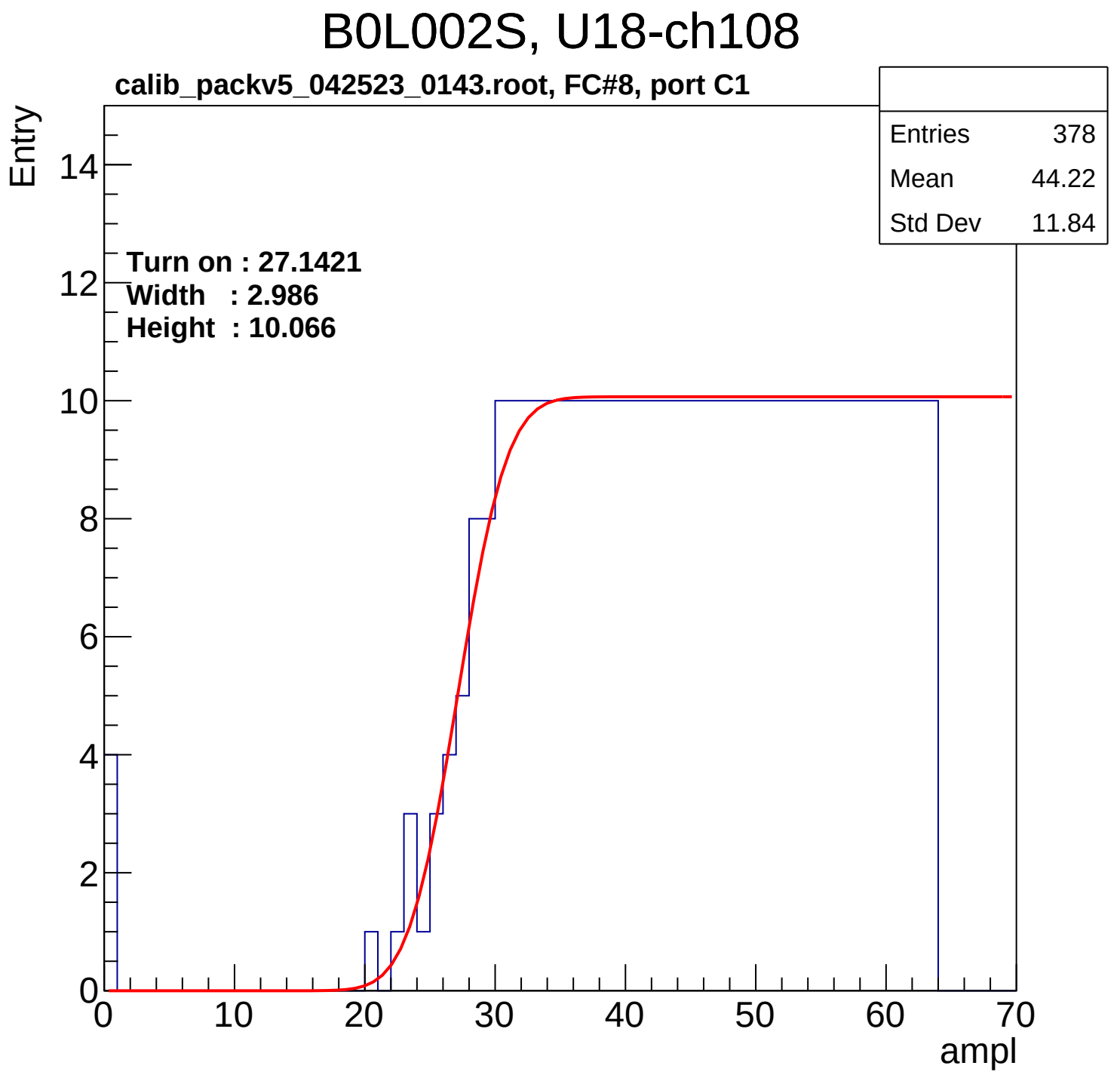

B0L002S, U18-ch103
calib_packv5_042523_0143.root, FC#8, port C1
Entries 376
Mean 44.3
Std Dev 11.8
Turn on : 26.6502
Width : 2.817
Height : 9.937
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

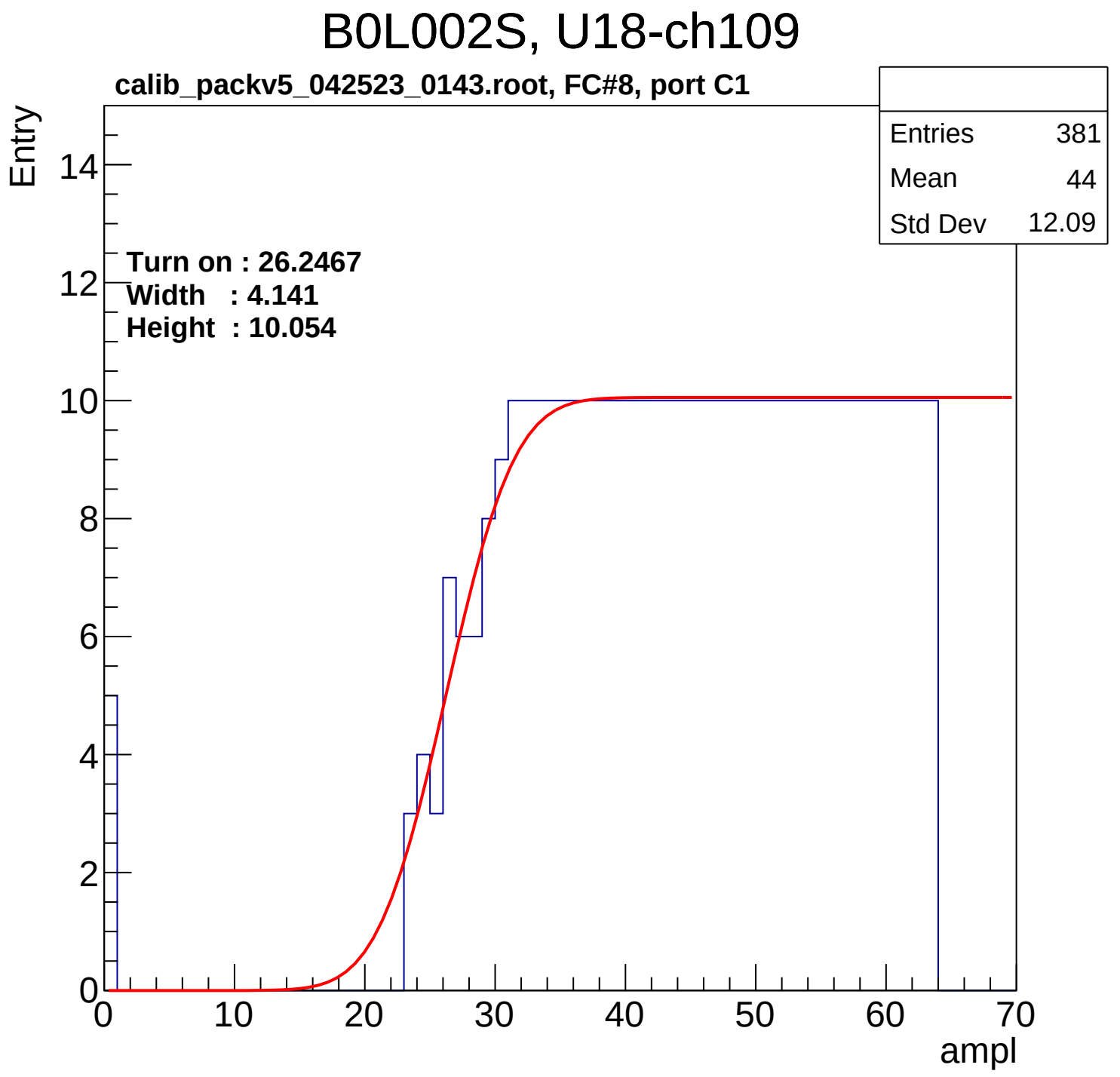

B0L002S, U18-ch104
calib_packv5_042523_0143.root, FC#8, port C1
Entries 368
Mean 44.84
Std Dev 11.29
Turn on : 27.4589
Width : 3.270
Height : 9.962
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

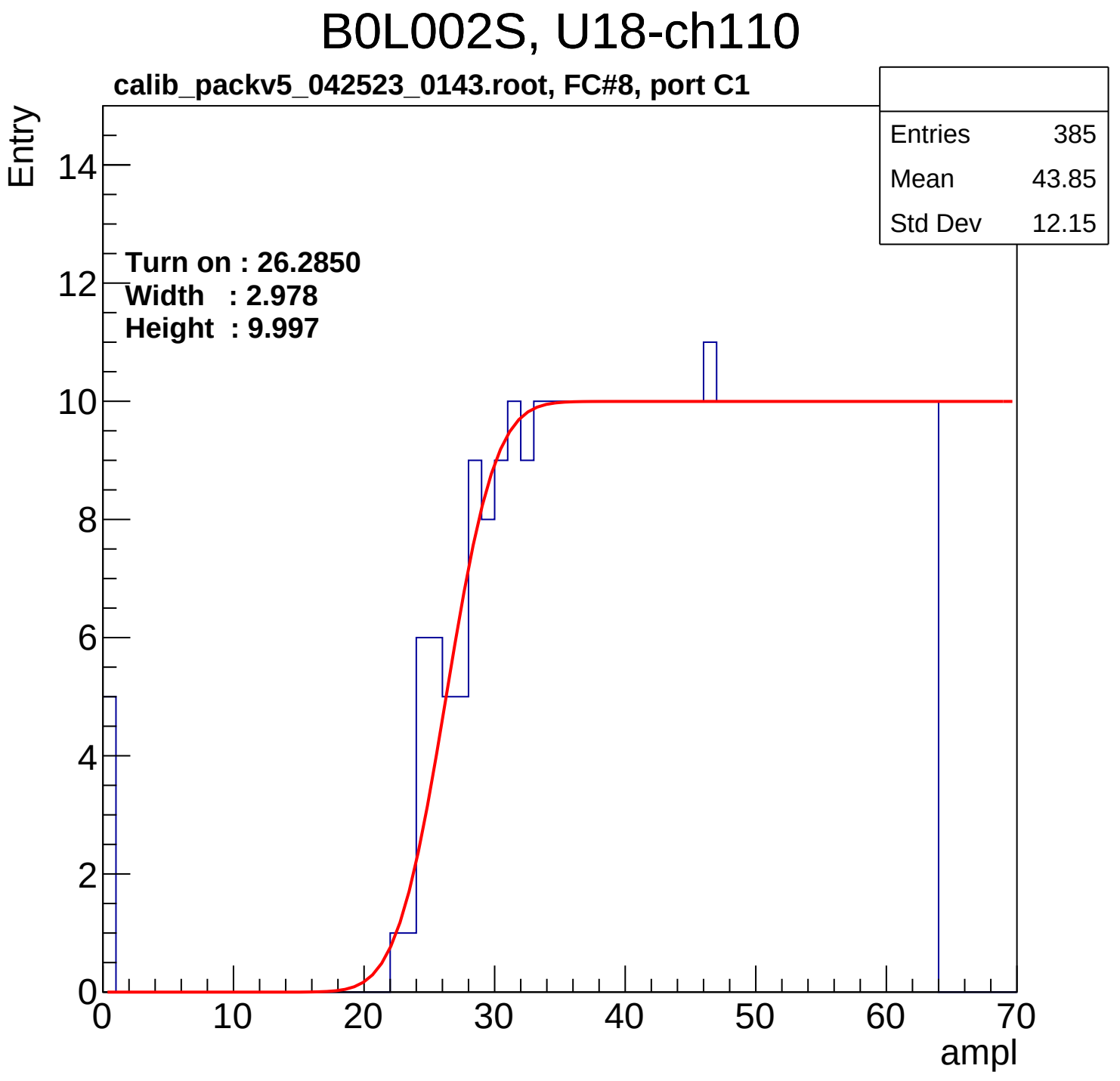

B0L002S, U18-ch105
calib_packv5_042523_0143.root, FC#8, port C1
Entries 384
Mean 44.05
Std Dev 11.64
Turn on : 26.0747
Width : 3.390
Height : 10.013
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

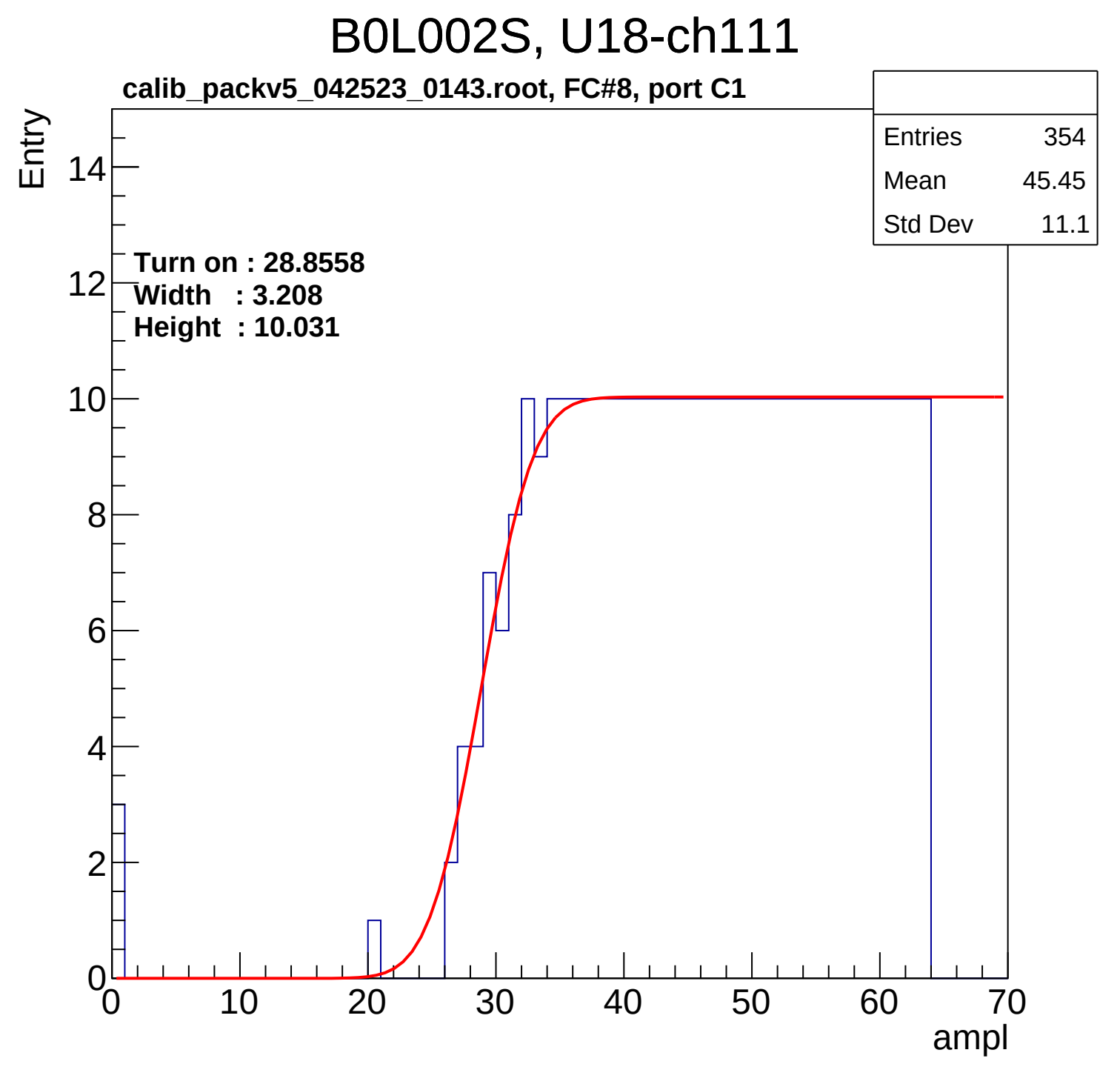

B0L002S, U18-ch106
calib_packv5_042523_0143.root, FC#8, port C1
Entries 370
Mean 44.89
Std Dev 11.01
Turn on : 27.6509
Width : 2.662
Height : 10.068
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

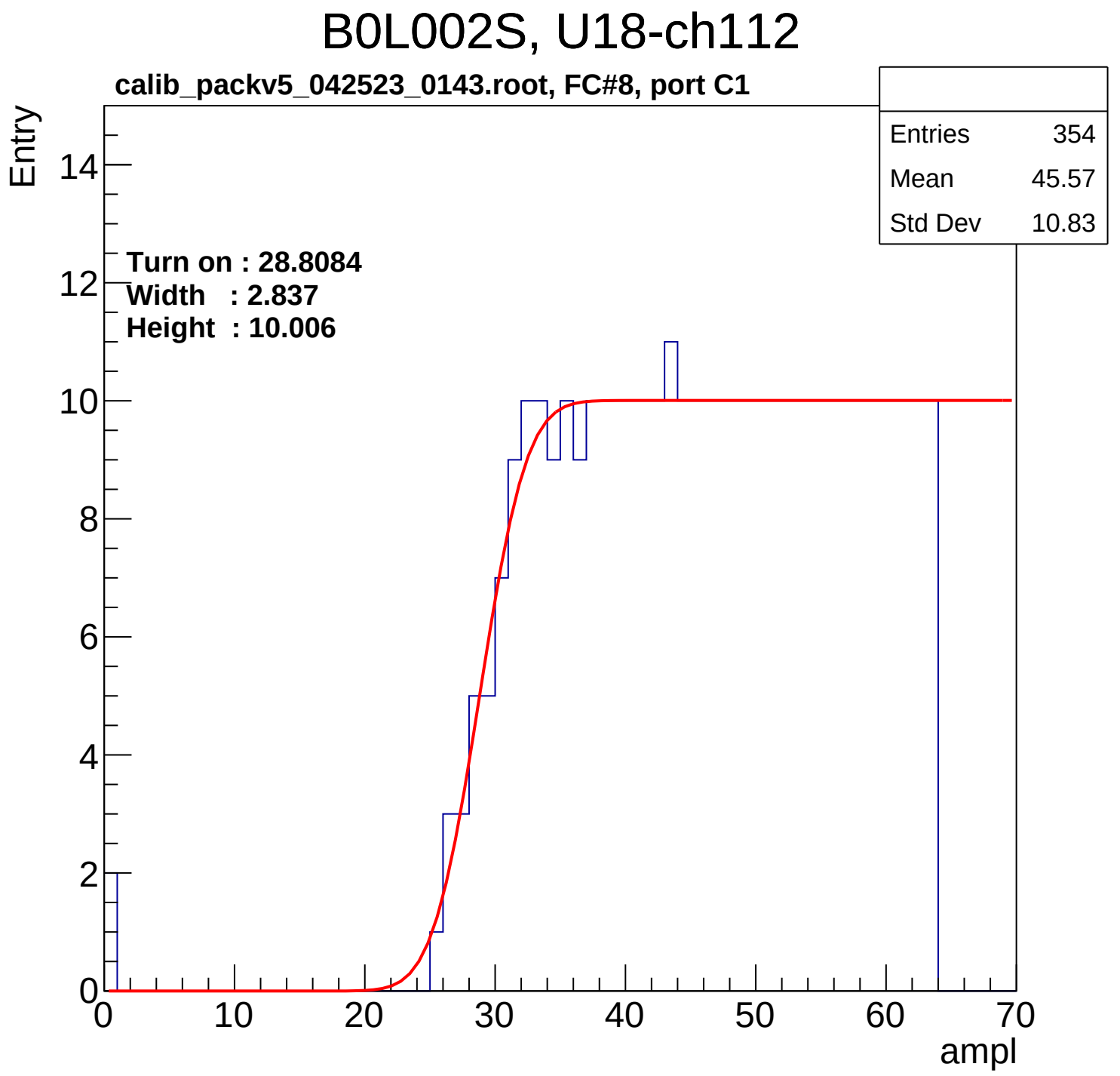

B0L002S, U18-ch107
calib_packv5_042523_0143.root, FC#8, port C1
Entries 366
Mean 44.95
Std Dev 11.17
Turn on : 28.1071
Width : 2.584
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

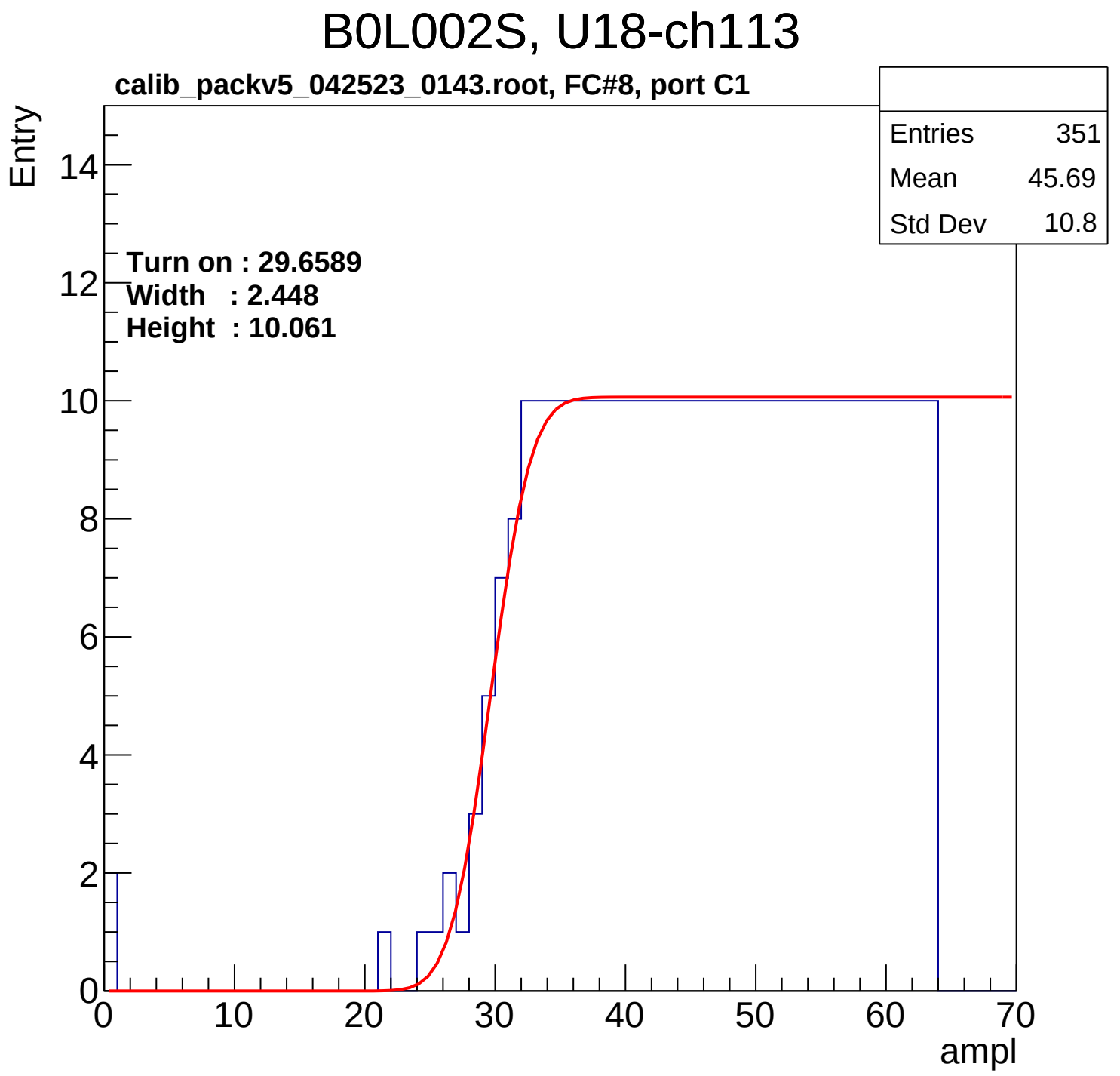

B0L002S, U18-ch108
calib_packv5_042523_0143.root, FC#8, port C1
Entries 378
Mean 44.22
Std Dev 11.84
Turn on : 27.1421
Width : 2.986
Height : 10.066
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

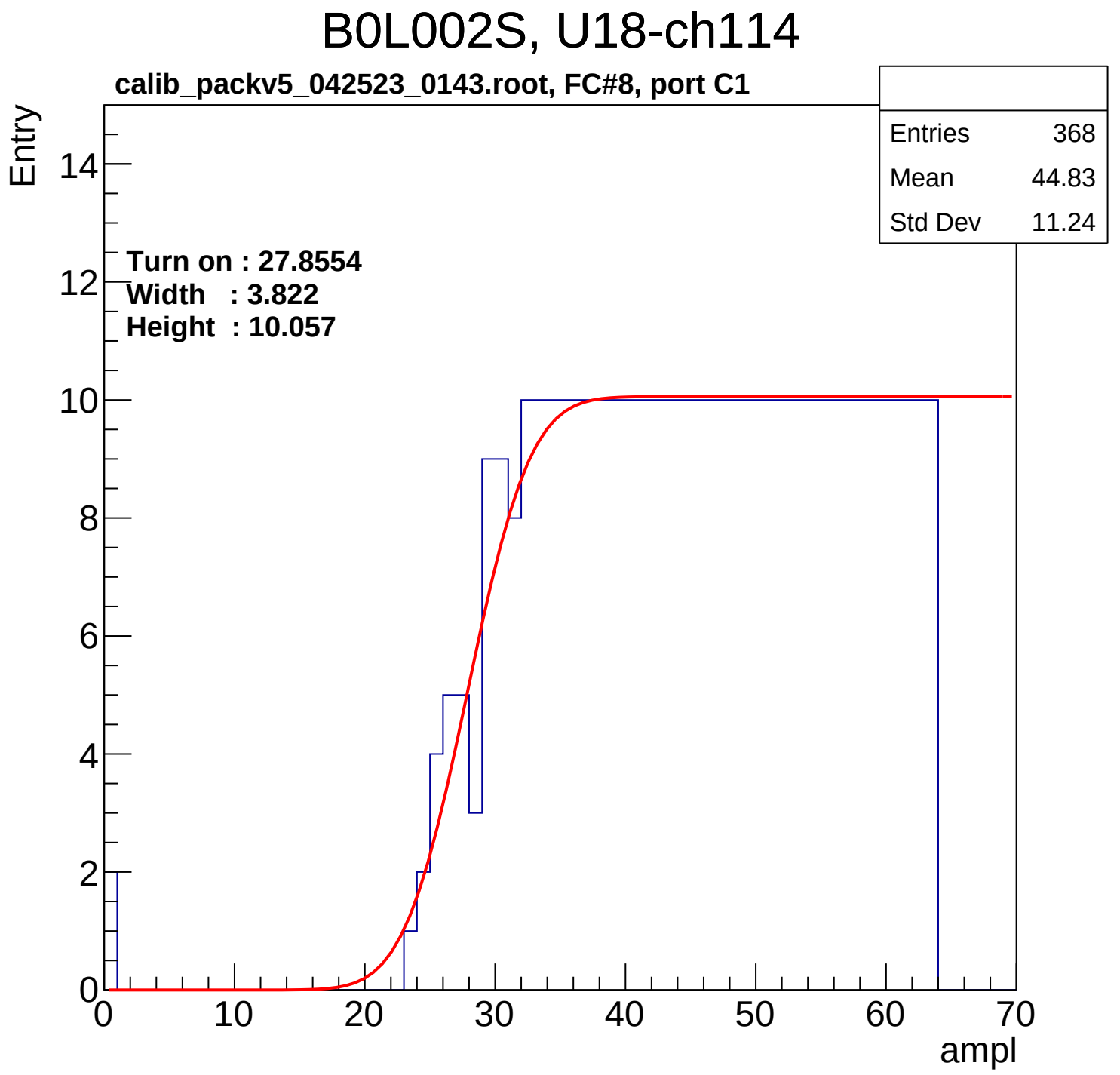

B0L002S, U18-ch109
calib_packv5_042523_0143.root, FC#8, port C1
Entries 381
Mean 44
Std Dev 12.09
Turn on : 26.2467
Width : 4.141
Height : 10.054
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

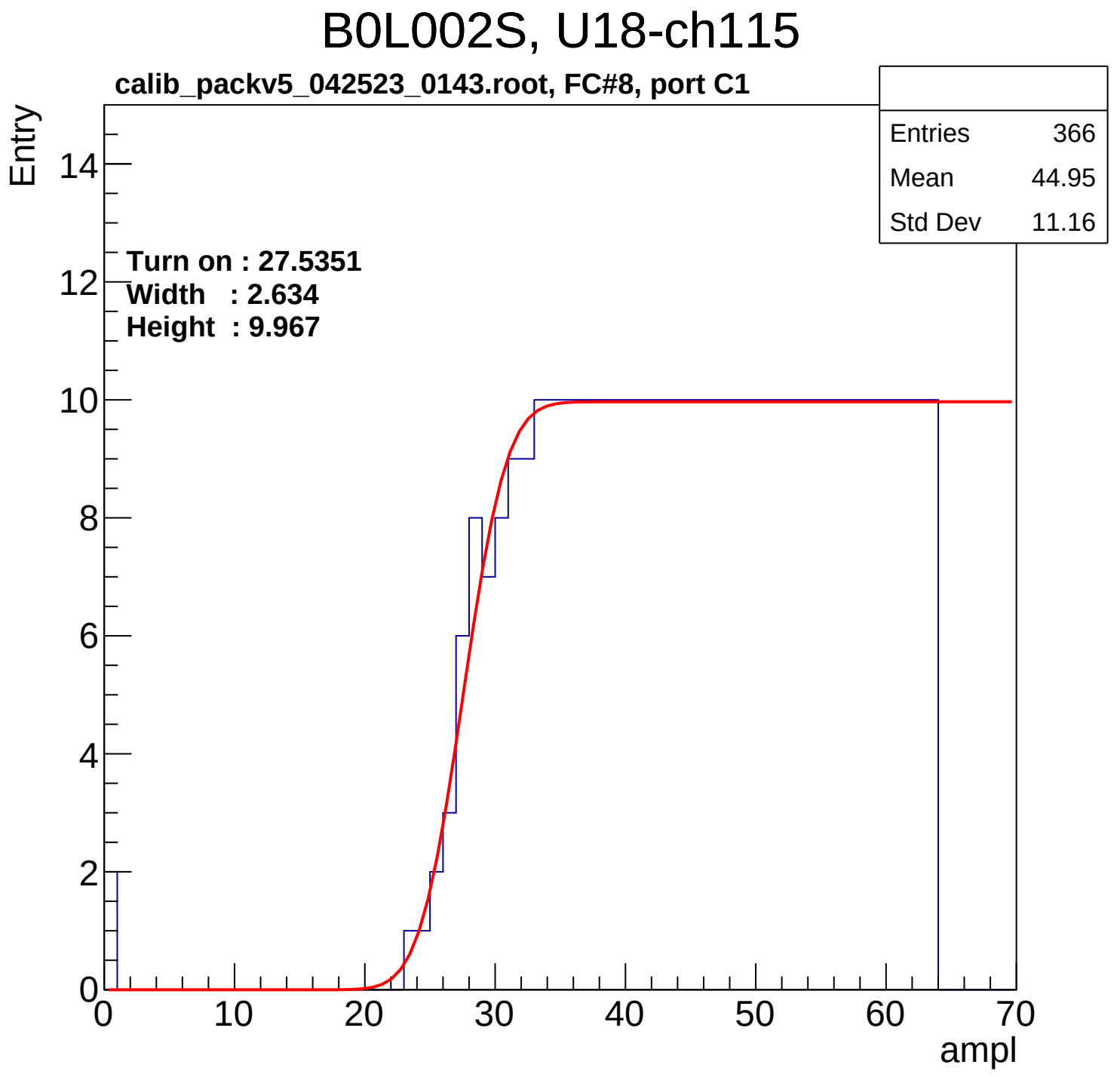

B0L002S, U18-ch110
calib_packv5_042523_0143.root, FC#8, port C1
Entries 385
Mean 43.85
Std Dev 12.15
Turn on : 26.2850
Width : 2.978
Height : 9.997
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

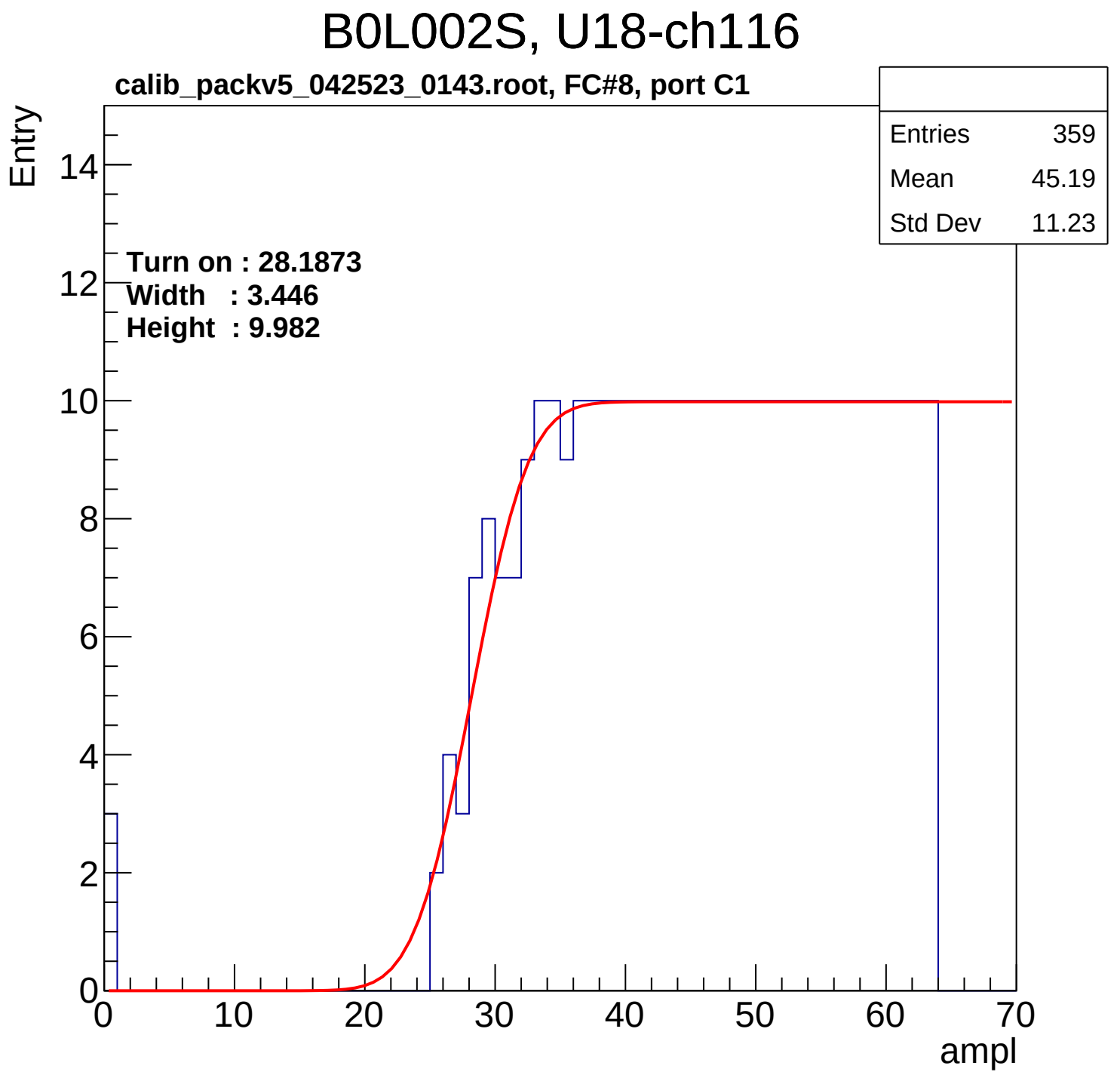

B0L002S, U18-ch111
calib_packv5_042523_0143.root, FC#8, port C1
Entries 354
Mean 45.45
Std Dev 11.1
Turn on : 28.8558
Width : 3.208
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

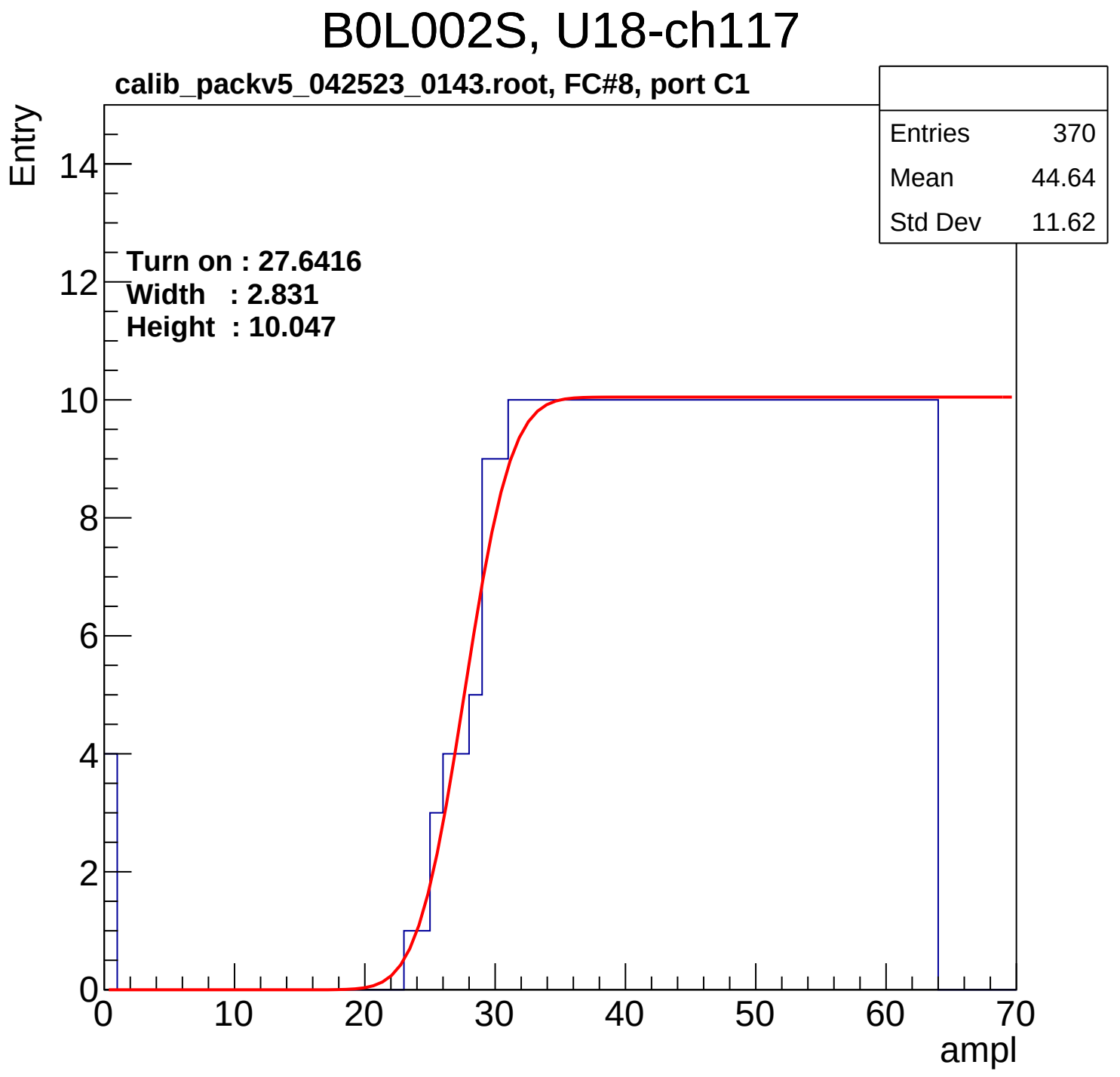

B0L002S, U18-ch112
calib_packv5_042523_0143.root, FC#8, port C1
Entries 354
Mean 45.57
Std Dev 10.83
Turn on : 28.8084
Width : 2.837
Height : 10.006
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

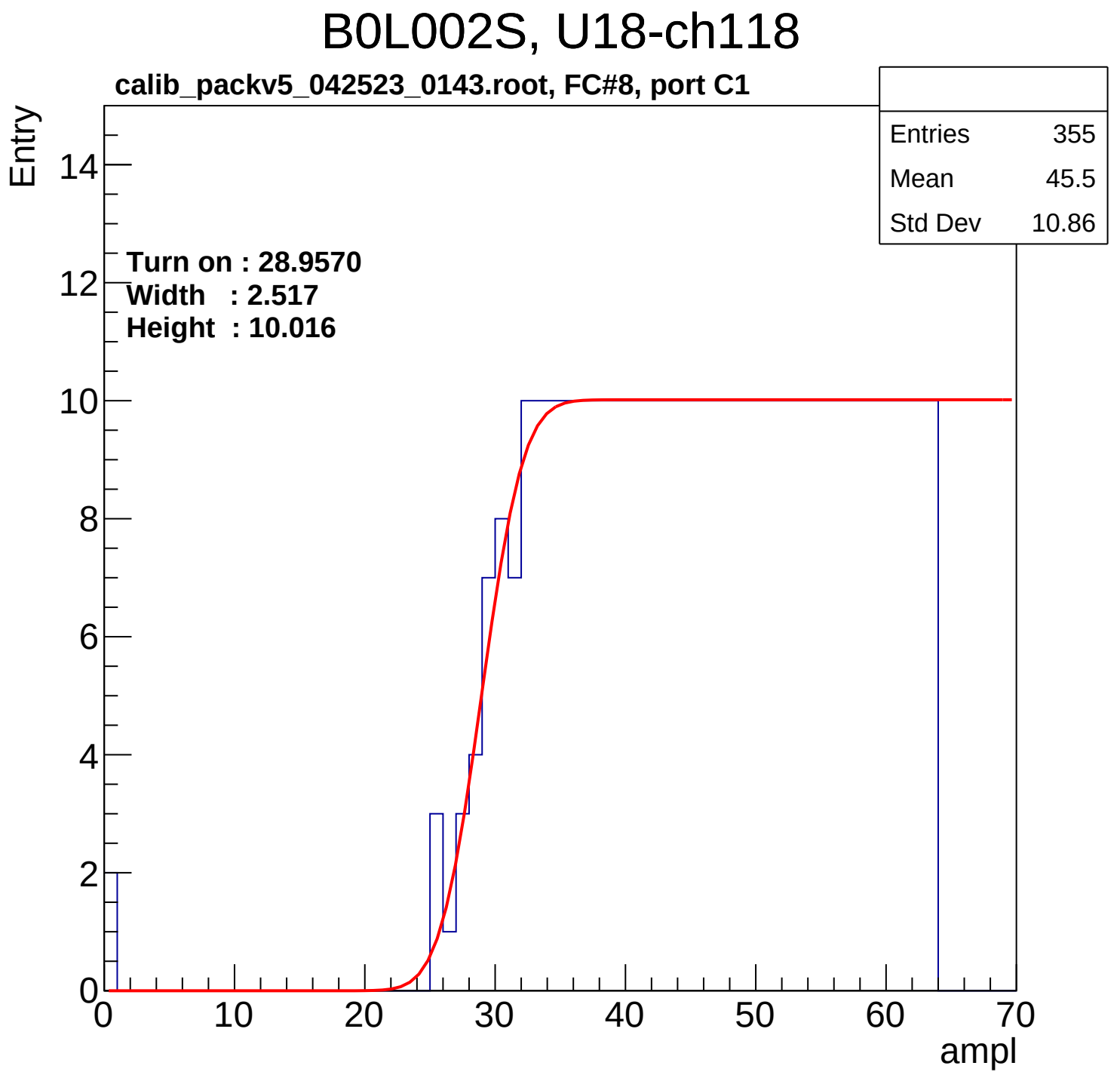

B0L002S, U18-ch113
calib_packv5_042523_0143.root, FC#8, port C1
Entries 351
Mean 45.69
Std Dev 10.8
Turn on : 29.6589
Width : 2.448
Height : 10.061
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

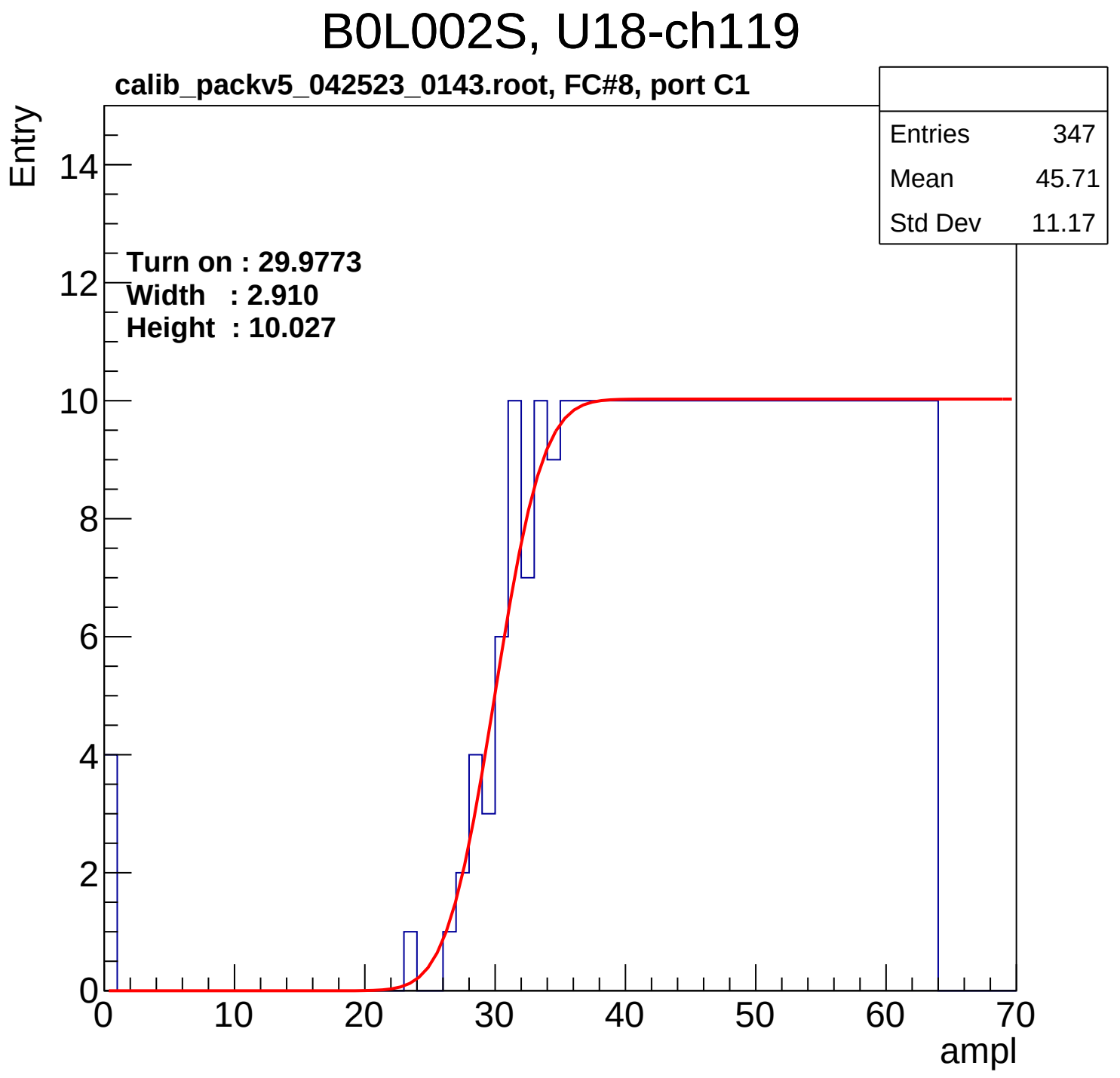

B0L002S, U18-ch114
calib_packv5_042523_0143.root, FC#8, port C1
Entries 368
Mean 44.83
Std Dev 11.24
Turn on : 27.8554
Width : 3.822
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

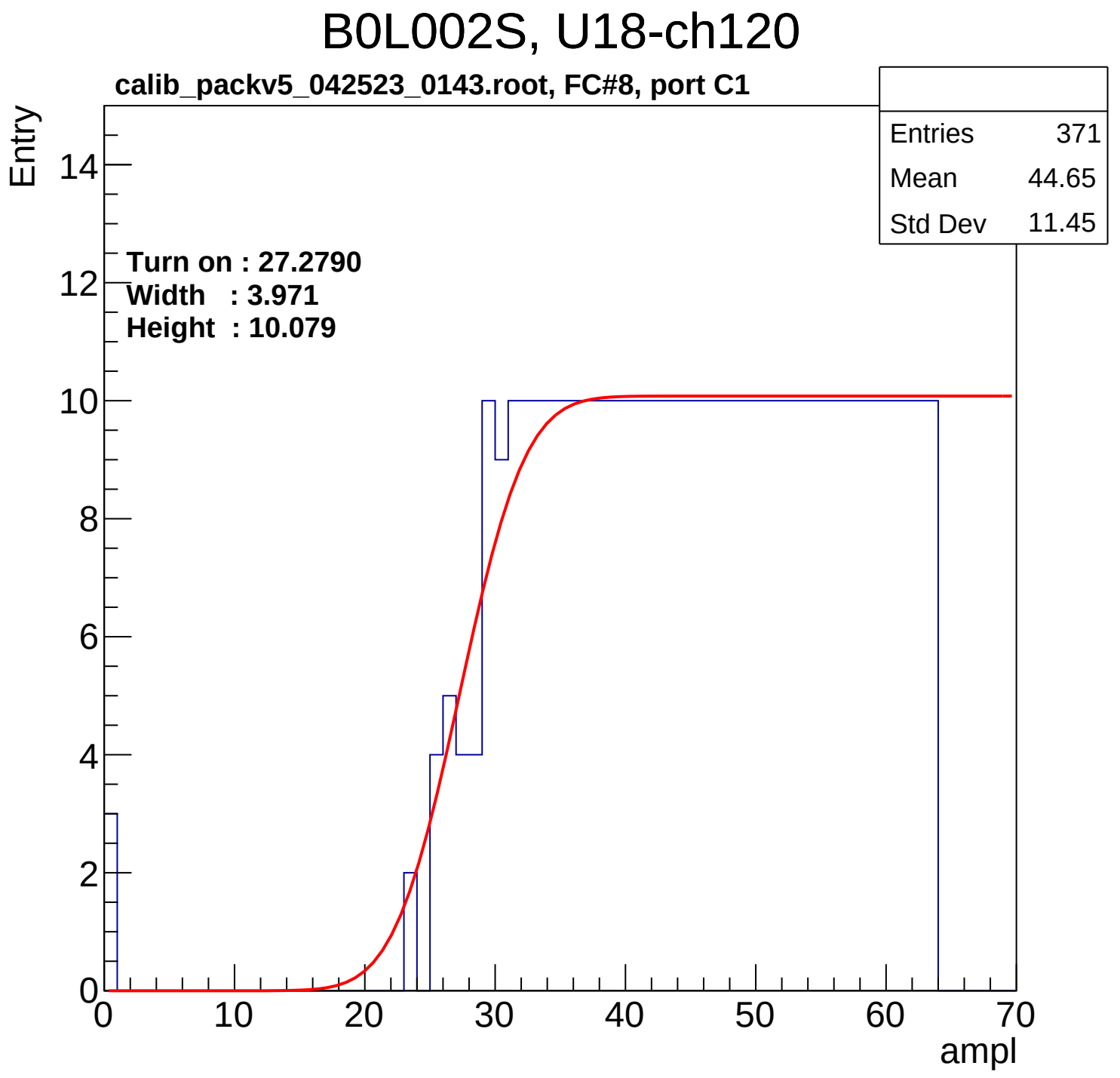

B0L002S, U18-ch115
calib_packv5_042523_0143.root, FC#8, port C1
Entries 366
Mean 44.95
Std Dev 11.16
Turn on : 27.5351
Width : 2.634
Height : 9.967
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

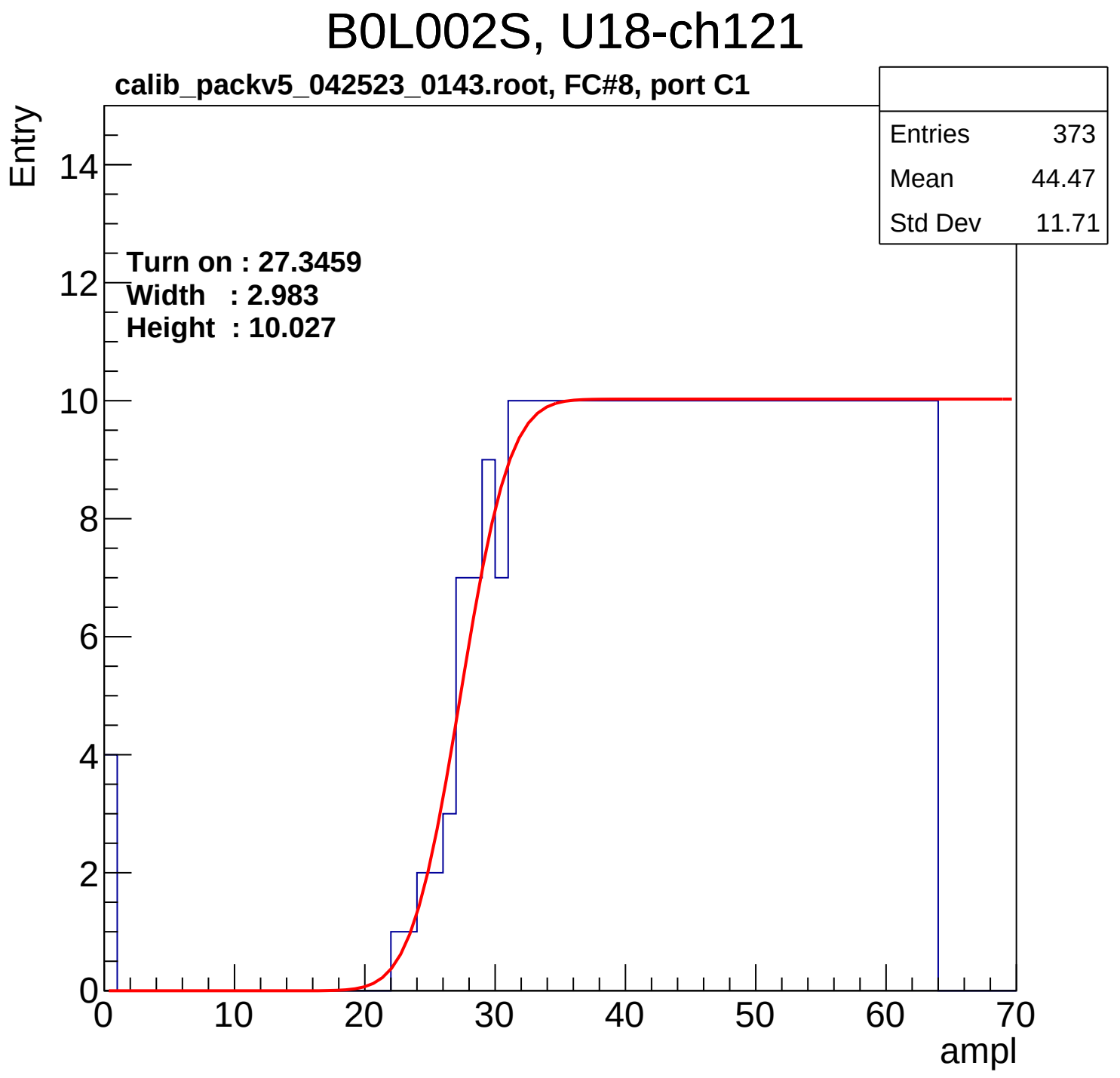

B0L002S, U18-ch116
calib_packv5_042523_0143.root, FC#8, port C1
Entries 359
Mean 45.19
Std Dev 11.23
Turn on : 28.1873
Width : 3.446
Height : 9.982
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

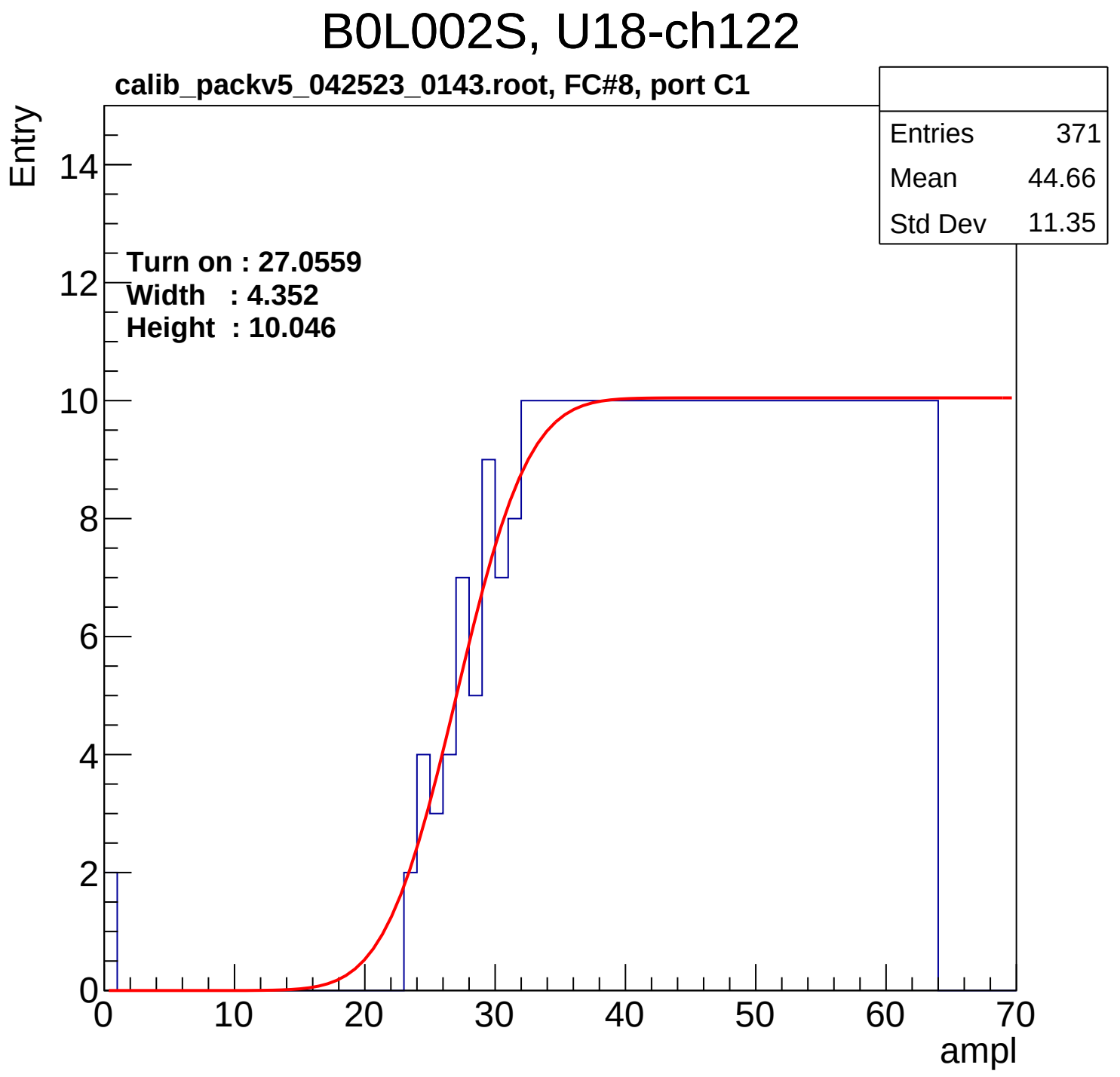

B0L002S, U18-ch117
calib_packv5_042523_0143.root, FC#8, port C1
Entries 370
Mean 44.64
Std Dev 11.62
Turn on : 27.6416
Width : 2.831
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

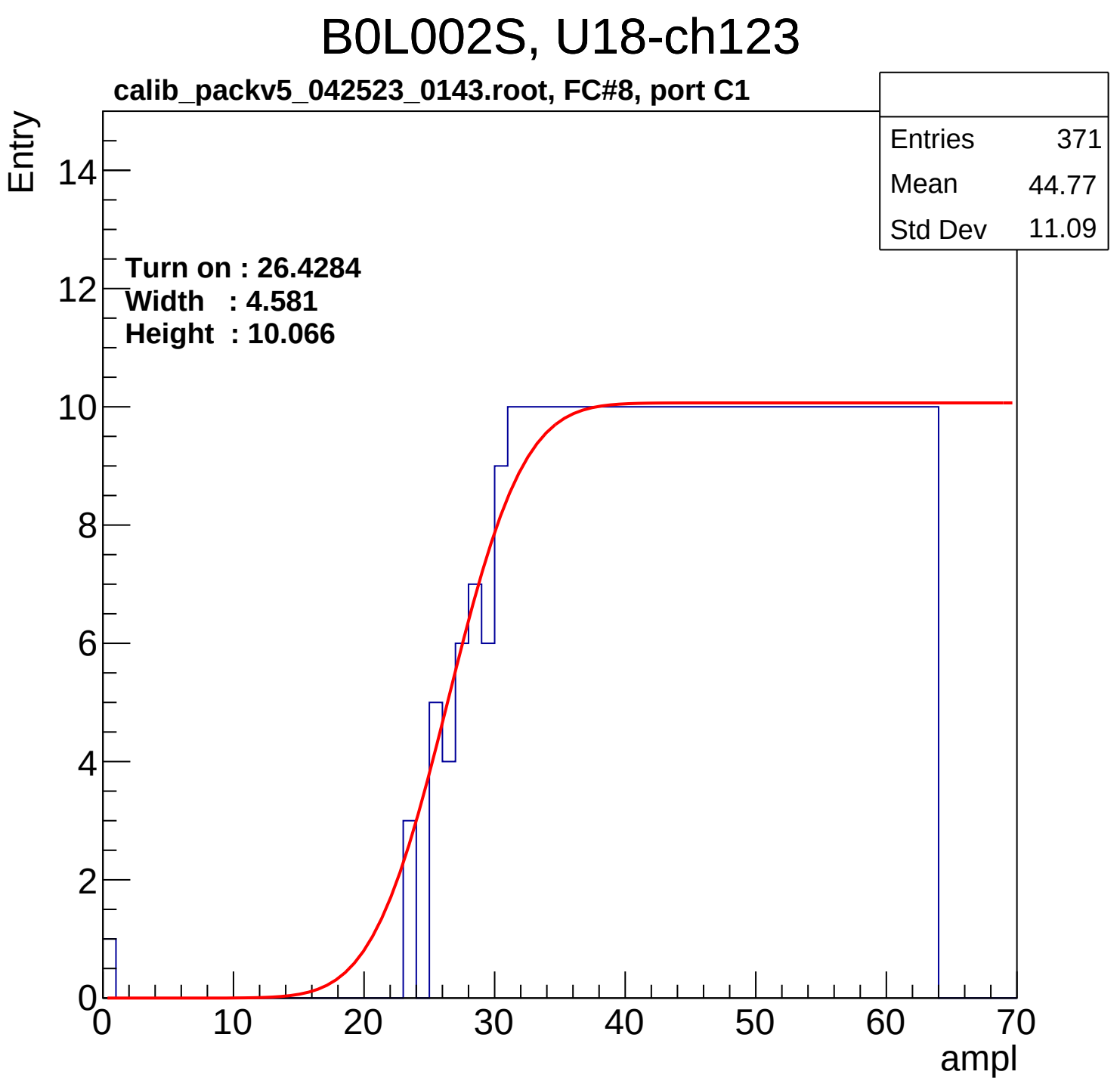

B0L002S, U18-ch118
calib_packv5_042523_0143.root, FC#8, port C1
Entries 355
Mean 45.5
Std Dev 10.86
Turn on : 28.9570
Width : 2.517
Height : 10.016
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

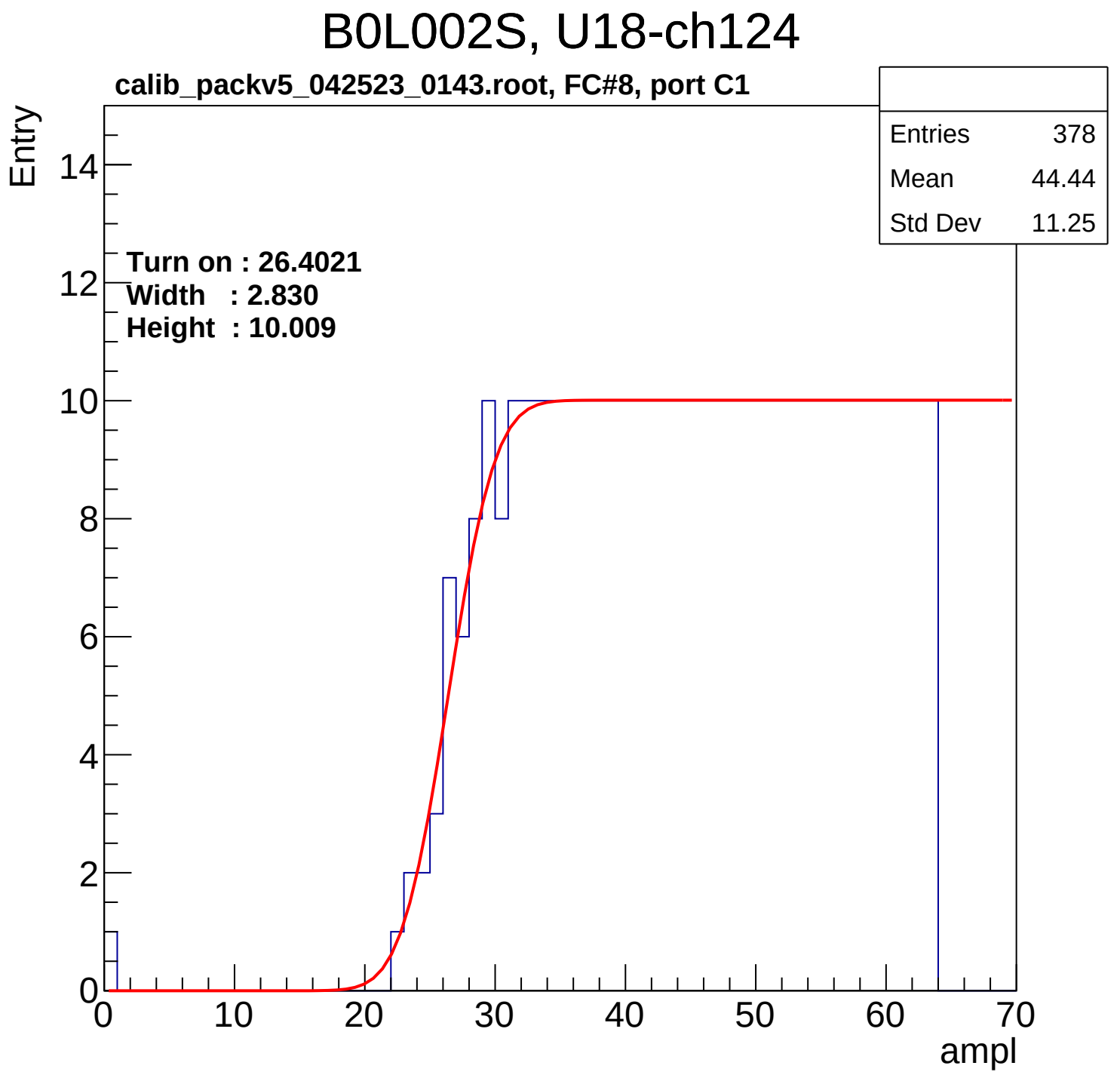

B0L002S, U18-ch119
calib_packv5_042523_0143.root, FC#8, port C1
Entries 347
Mean 45.71
Std Dev 11.17
Turn on : 29.9773
Width : 2.910
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

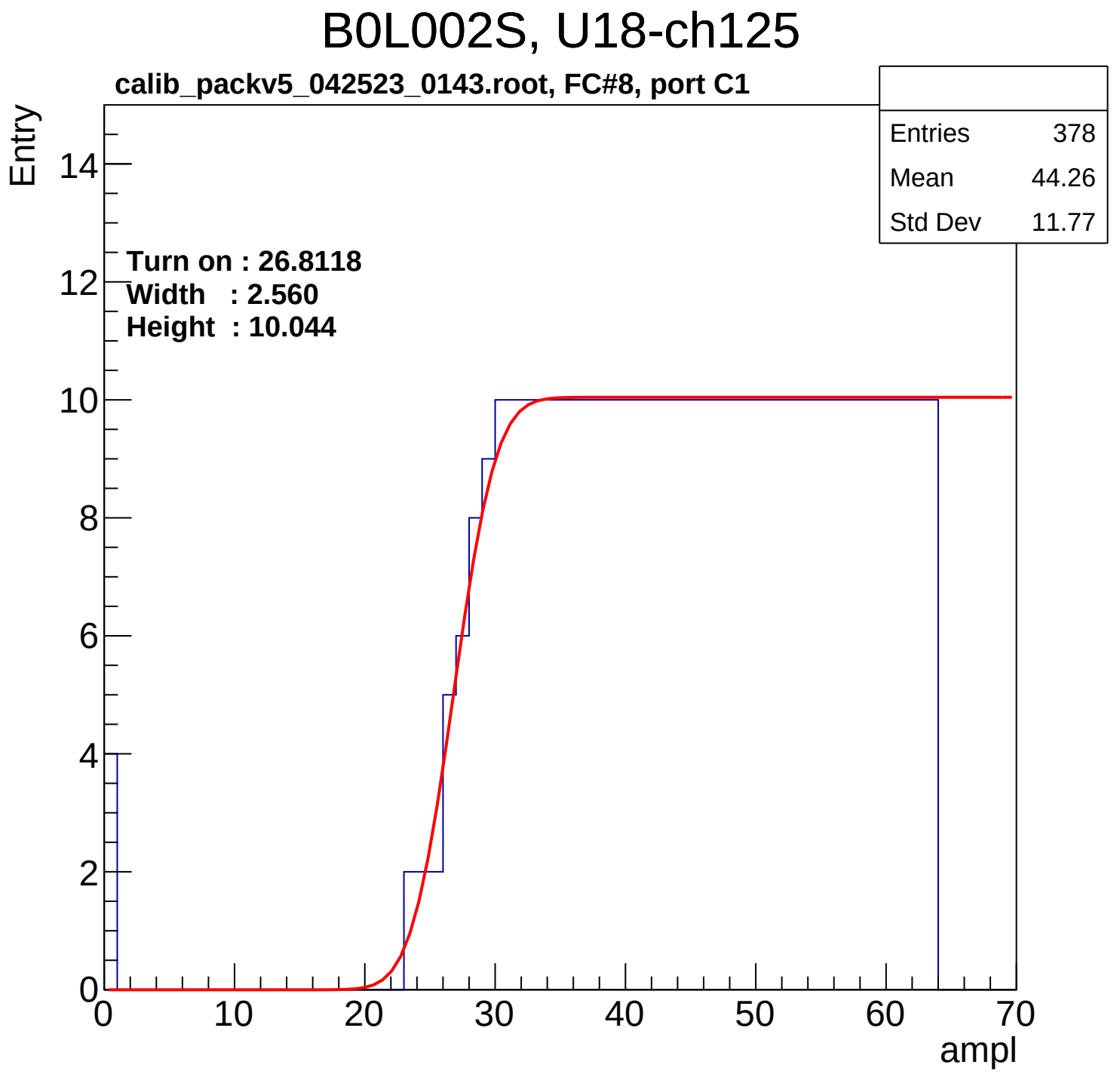

B0L002S, U18-ch120
calib_packv5_042523_0143.root, FC#8, port C1
Entries 371
Mean 44.65
Std Dev 11.45
Turn on : 27.2790
Width : 3.971
Height : 10.079
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

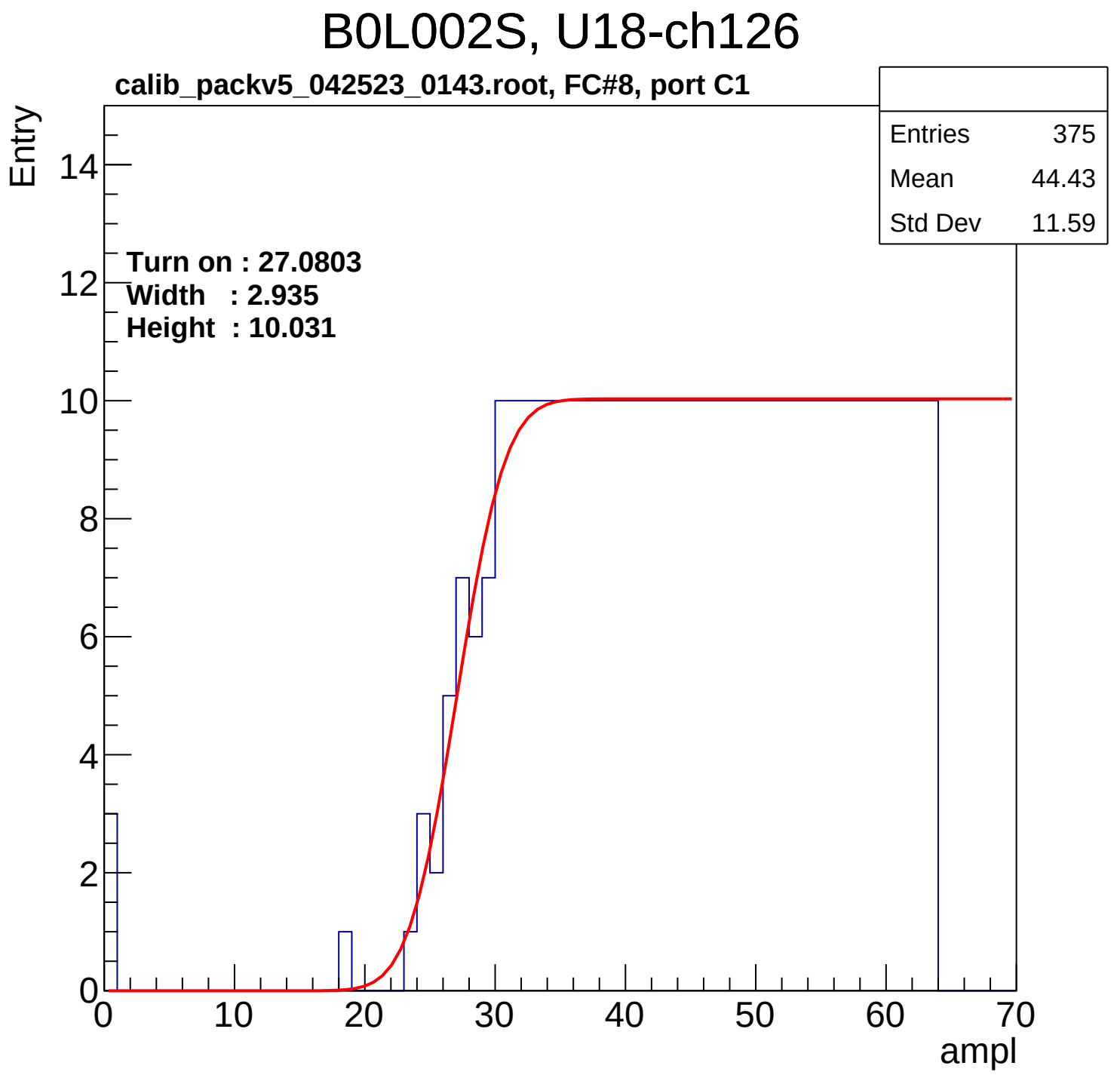

B0L002S, U18-ch121
calib_packv5_042523_0143.root, FC#8, port C1
Entries 373
Mean 44.47
Std Dev 11.71
Turn on : 27.3459
Width : 2.983
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

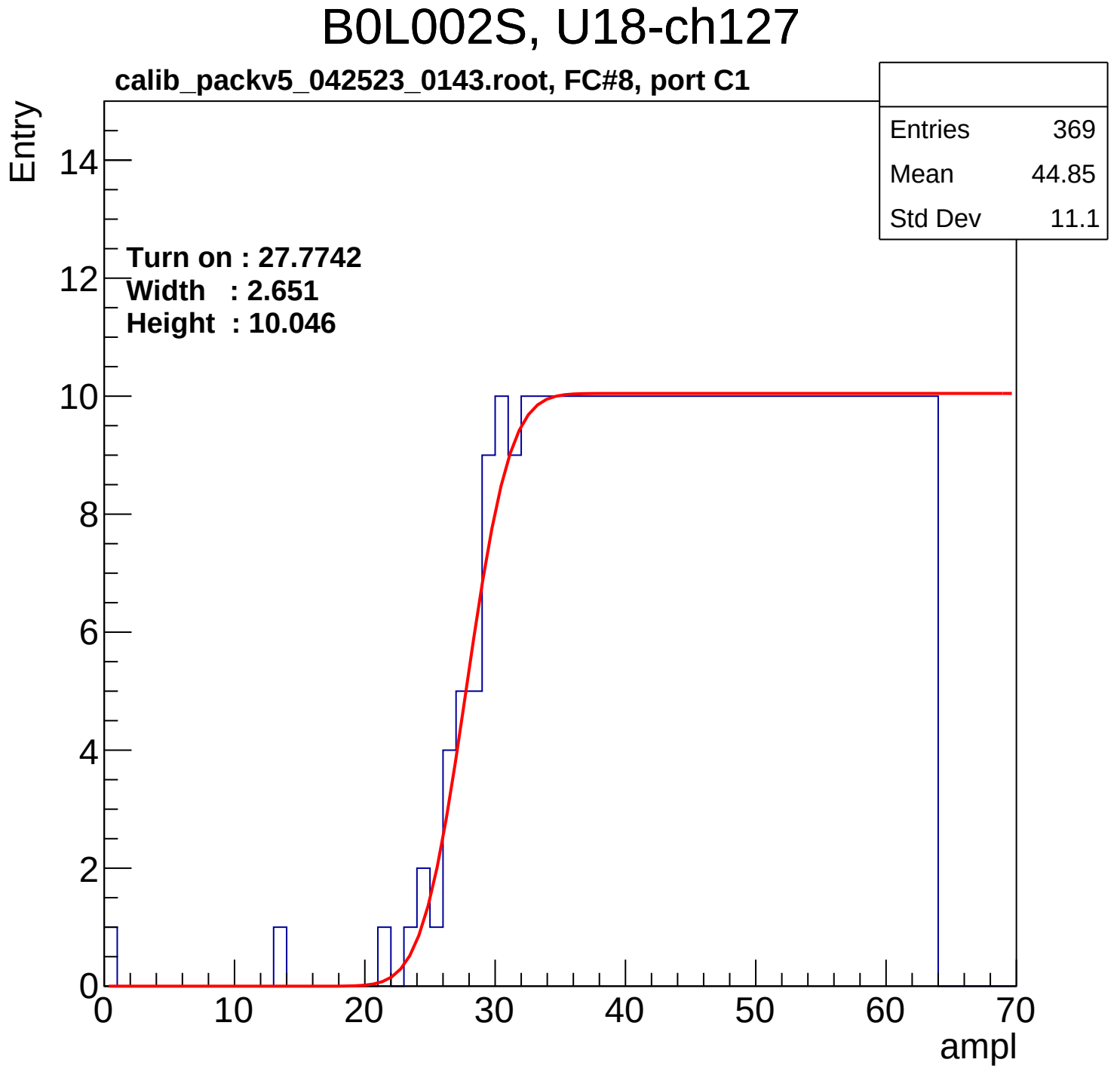

B0L002S, U18-ch122
calib_packv5_042523_0143.root, FC#8, port C1
Entries 371
Mean 44.66
Std Dev 11.35
Turn on : 27.0559
Width : 4.352
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

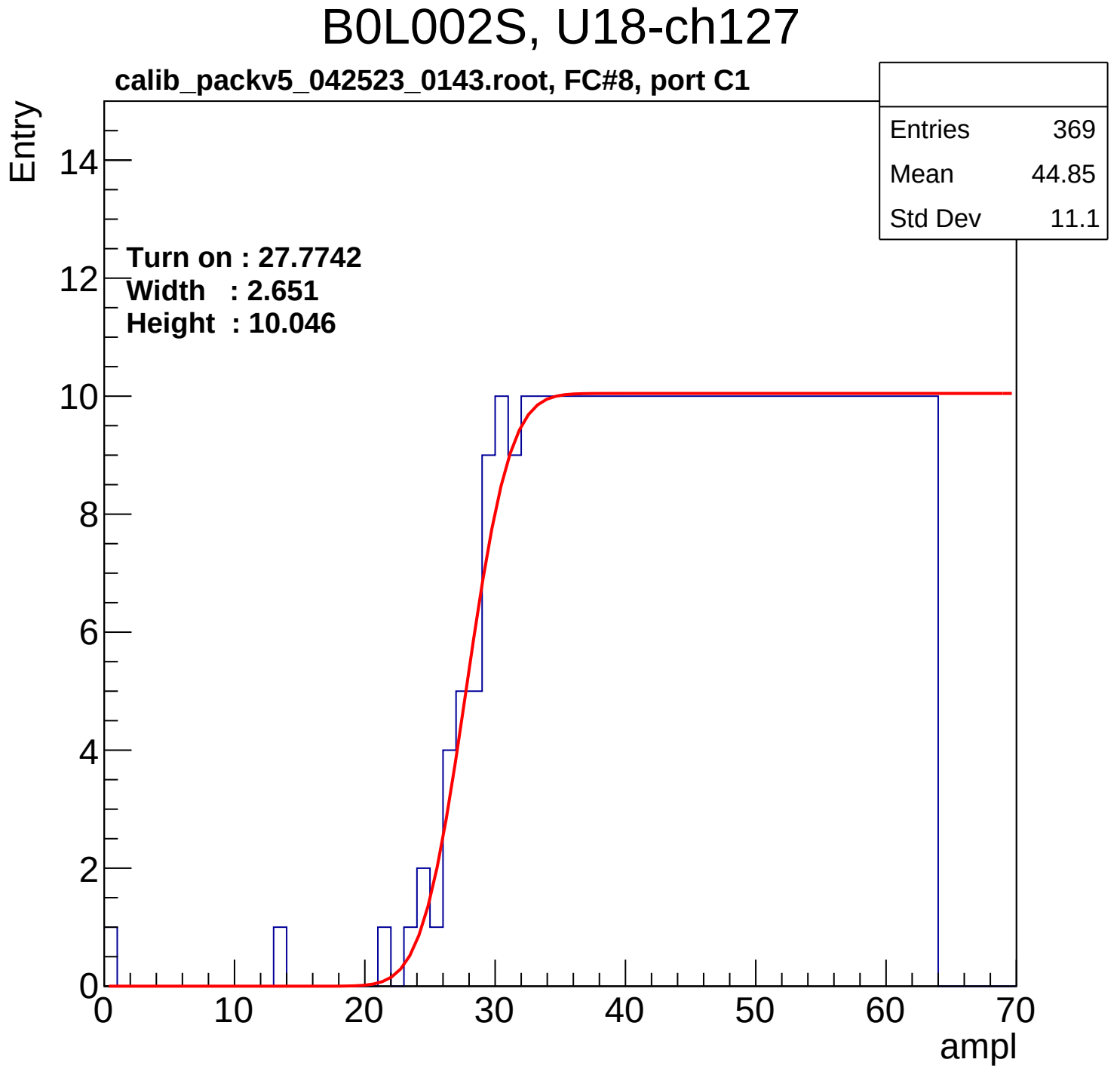

B0L002S, U18-ch123
calib_packv5_042523_0143.root, FC#8, port C1
Entries 371
Mean 44.77
Std Dev 11.09
Turn on : 26.4284
Width : 4.581
Height : 10.066
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L002S, U18-ch124
calib_packv5_042523_0143.root, FC#8, port C1
Entries 378
Mean 44.44
Std Dev 11.25
Turn on : 26.4021
Width : 2.830
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L002S, U18-ch125
calib_packv5_042523_0143.root, FC#8, port C1
Entries 378
Mean 44.26
Std Dev 11.77
Turn on : 26.8118
Width : 2.560
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L002S, U18-ch126
calib_packv5_042523_0143.root, FC#8, port C1
Entries 375
Mean 44.43
Std Dev 11.59
Turn on : 27.0803
Width : 2.935
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L002S, U18-ch127
calib_packv5_042523_0143.root, FC#8, port C1
Entries 369
Mean 44.85
Std Dev 11.1
Turn on : 27.7742
Width : 2.651
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L002S, U18-ch127
calib_packv5_042523_0143.root, FC#8, port C1
Entries 369
Mean 44.85
Std Dev 11.1
Turn on : 27.7742
Width : 2.651
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70