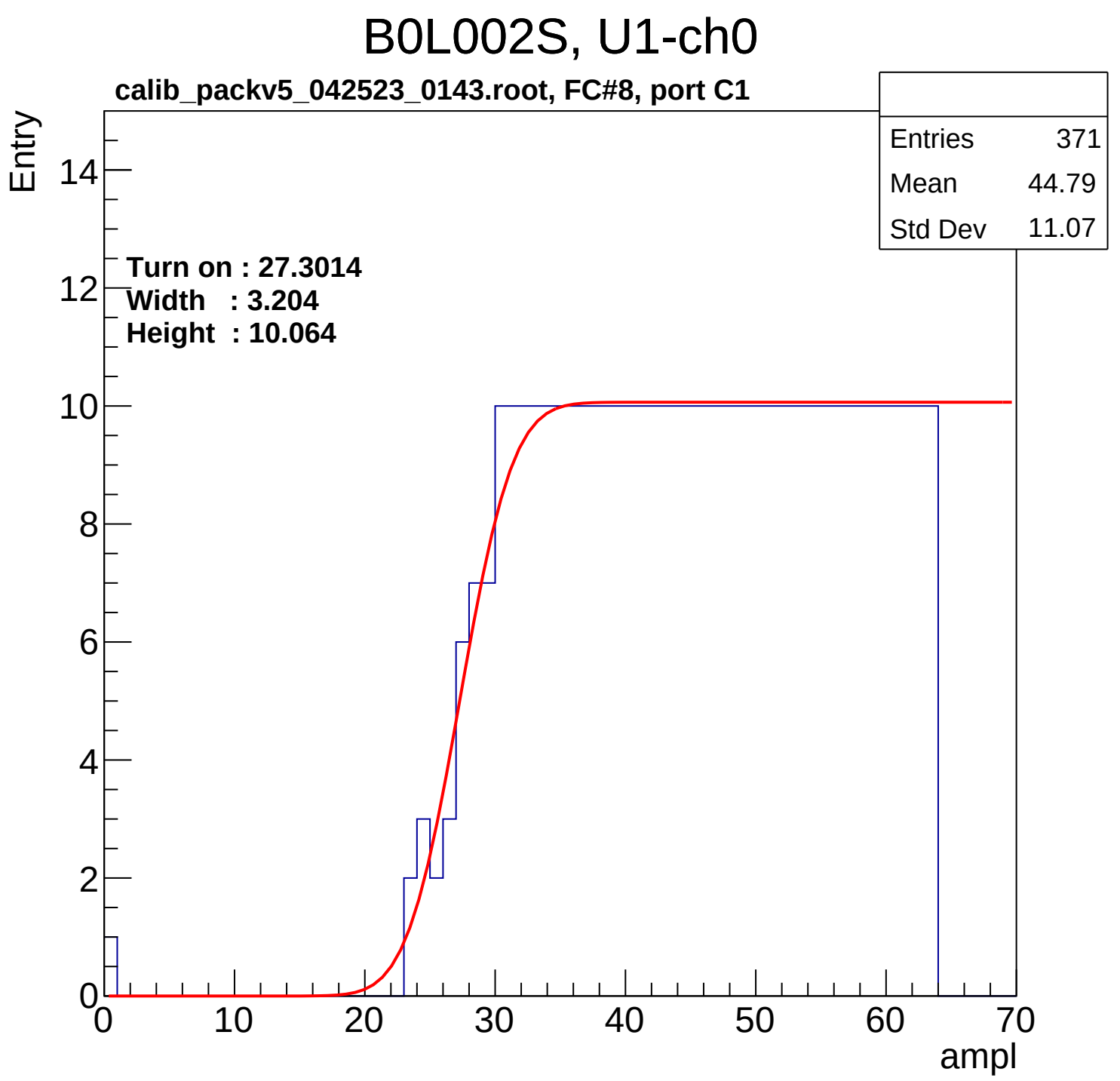
B0L002S, U1-ch0
calib_packv5_042523_0143.root, FC#8, port C1
Entries 371
Mean 44.79
Std Dev 11.07
Turn on : 27.3014
Width : 3.204
Height : 10.064
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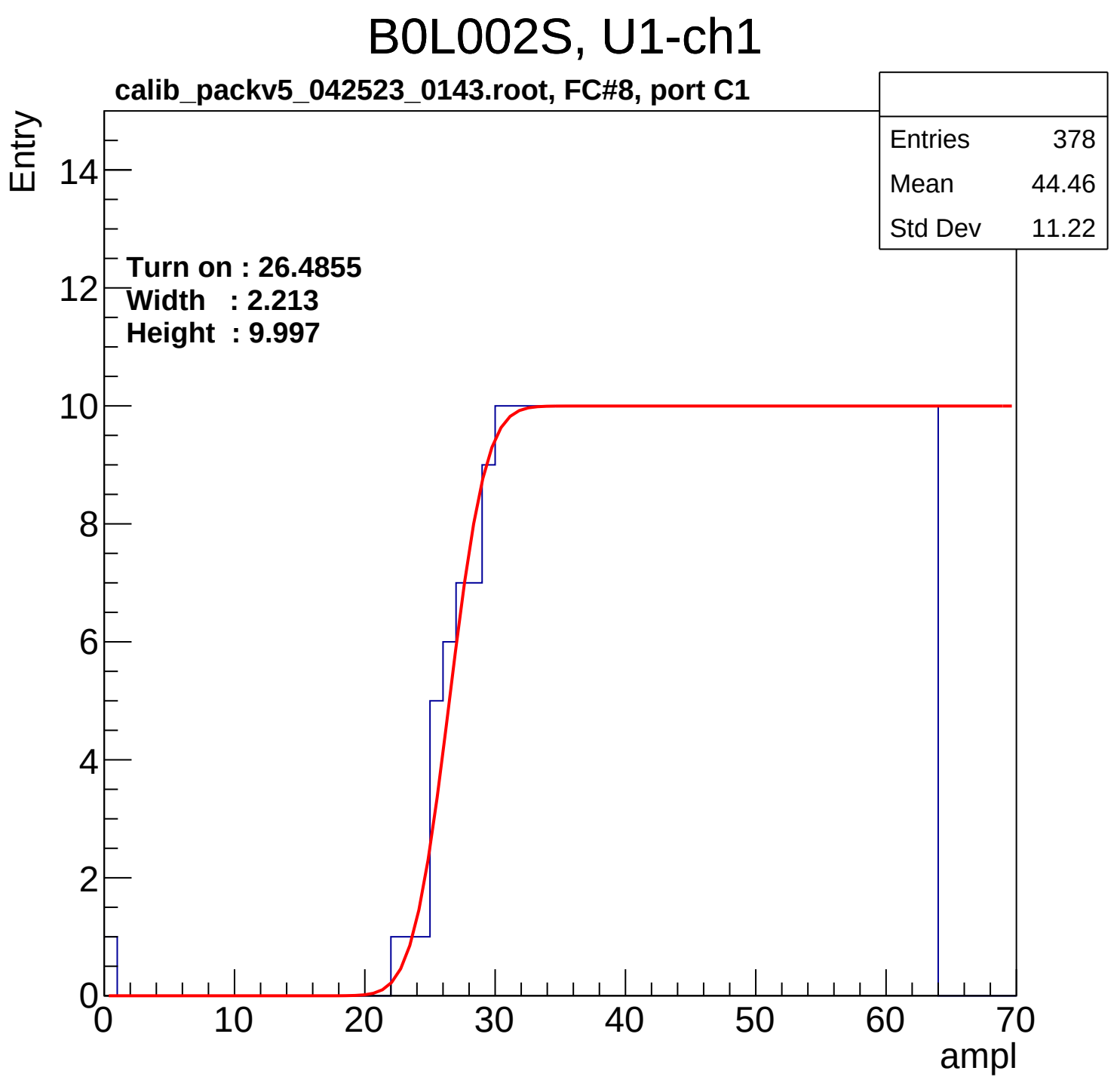
B0L002S, U1-ch1
calib_packv5_042523_0143.root, FC#8, port C1
Entries 378
Mean 44.46
Std Dev 11.22
Turn on : 26.4855
Width : 2.213
Height : 9.997
Entry
ampl
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2
4
6
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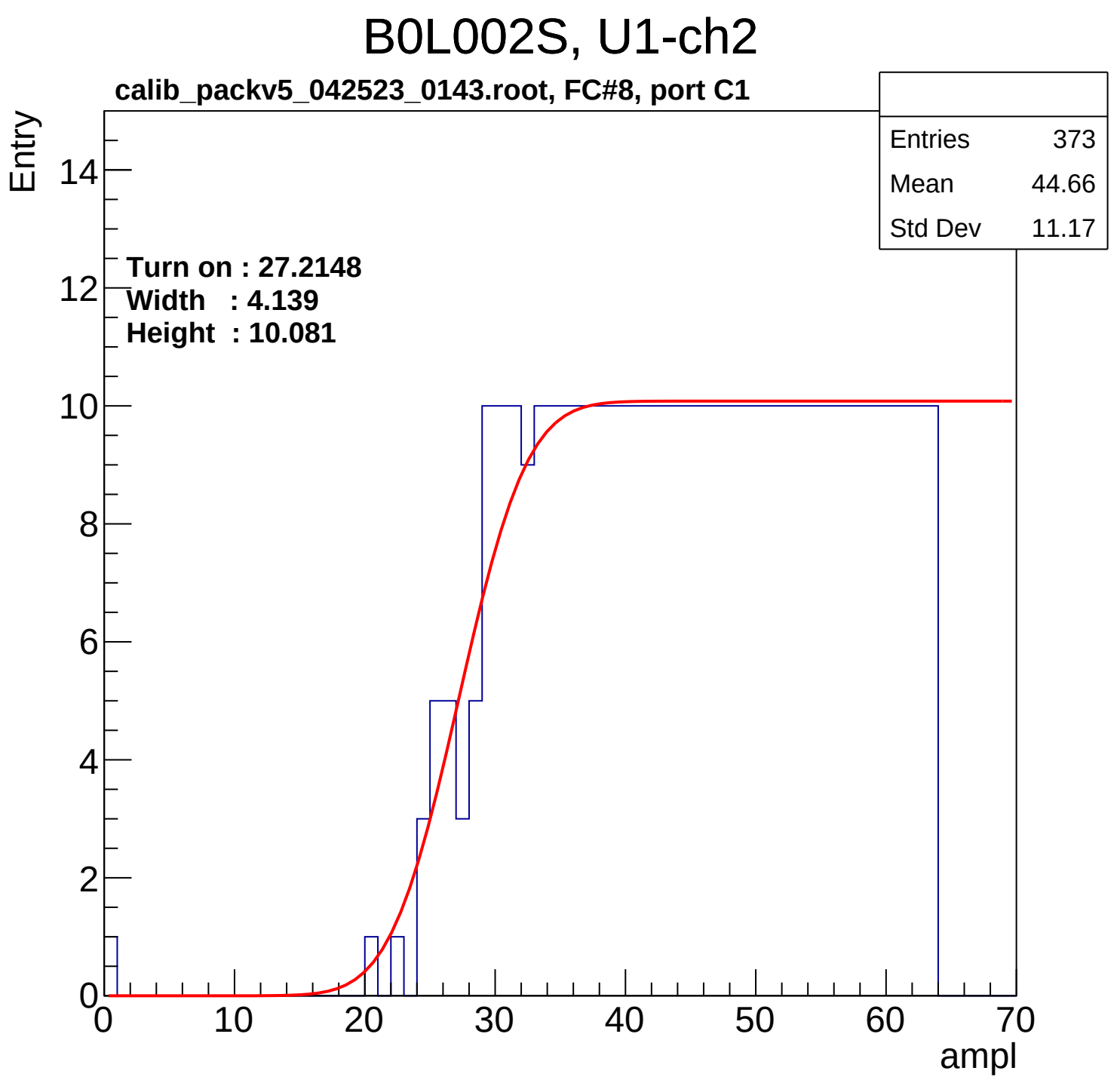
B0L002S, U1-ch2
calib_packv5_042523_0143.root, FC#8, port C1
Entries 373
Mean 44.66
Std Dev 11.17
Turn on : 27.2148
Width : 4.139
Height : 10.081
Entry
ampl
0
2
4
6
8
10
12
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0
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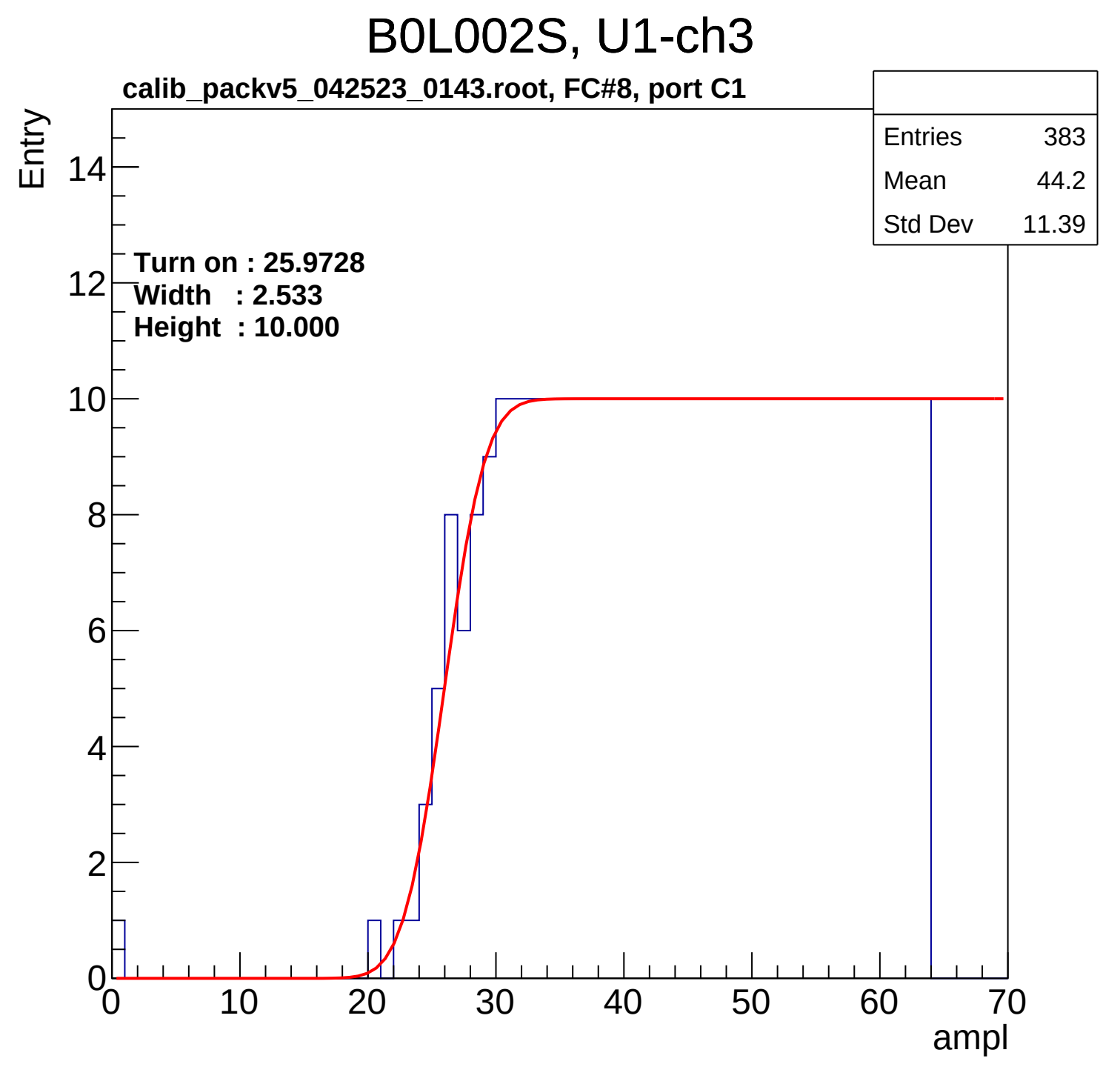
B0L002S, U1-ch3
calib_packv5_042523_0143.root, FC#8, port C1
Entries 383
Mean 44.2
Std Dev 11.39
Turn on : 25.9728
Width : 2.533
Height : 10.000
Entry
ampl
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2
4
6
8
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0
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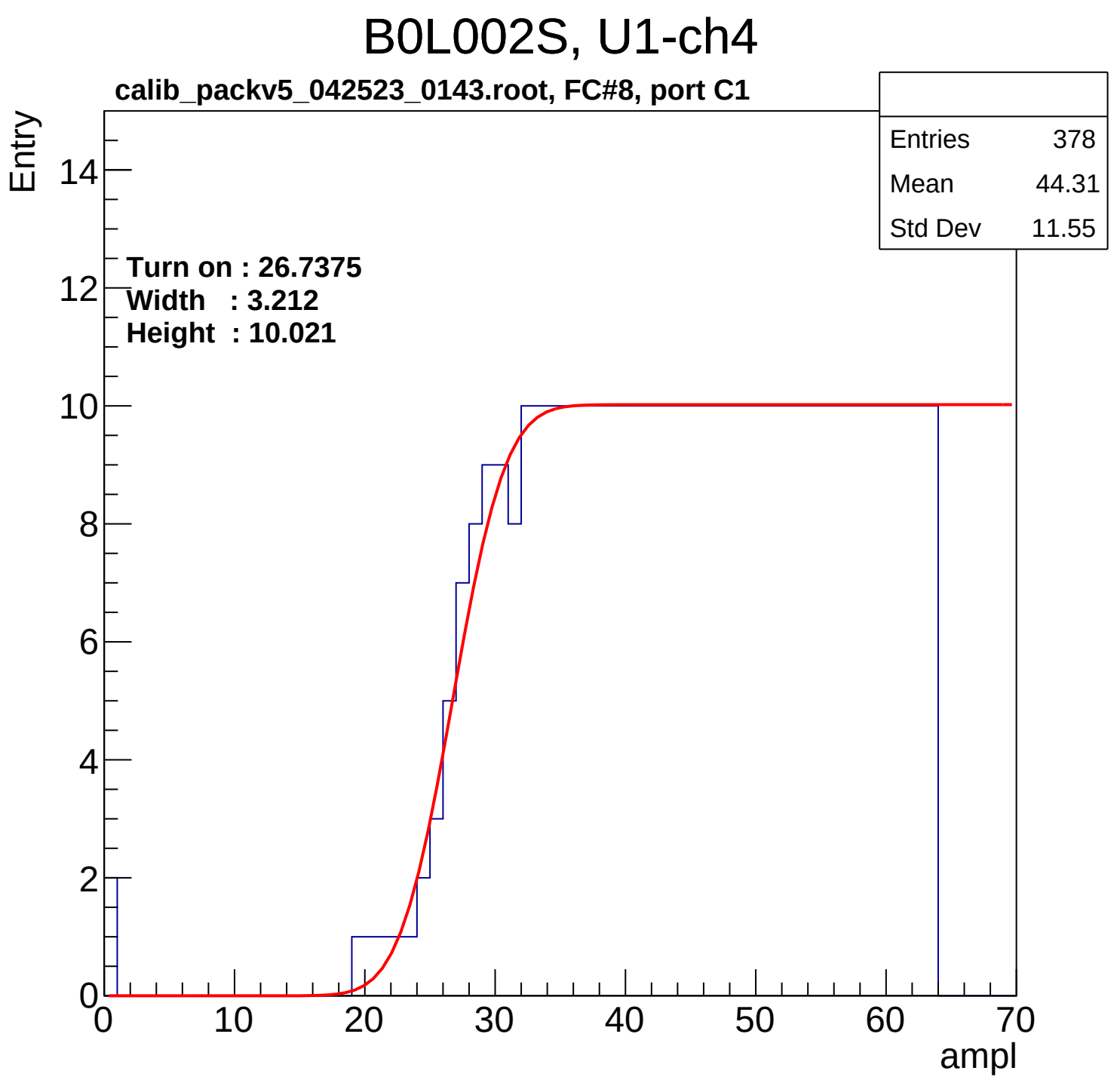
B0L002S, U1-ch4
calib_packv5_042523_0143.root, FC#8, port C1
Entries 378
Mean 44.31
Std Dev 11.55
Turn on : 26.7375
Width : 3.212
Height : 10.021
Entry
ampl
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2
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6
8
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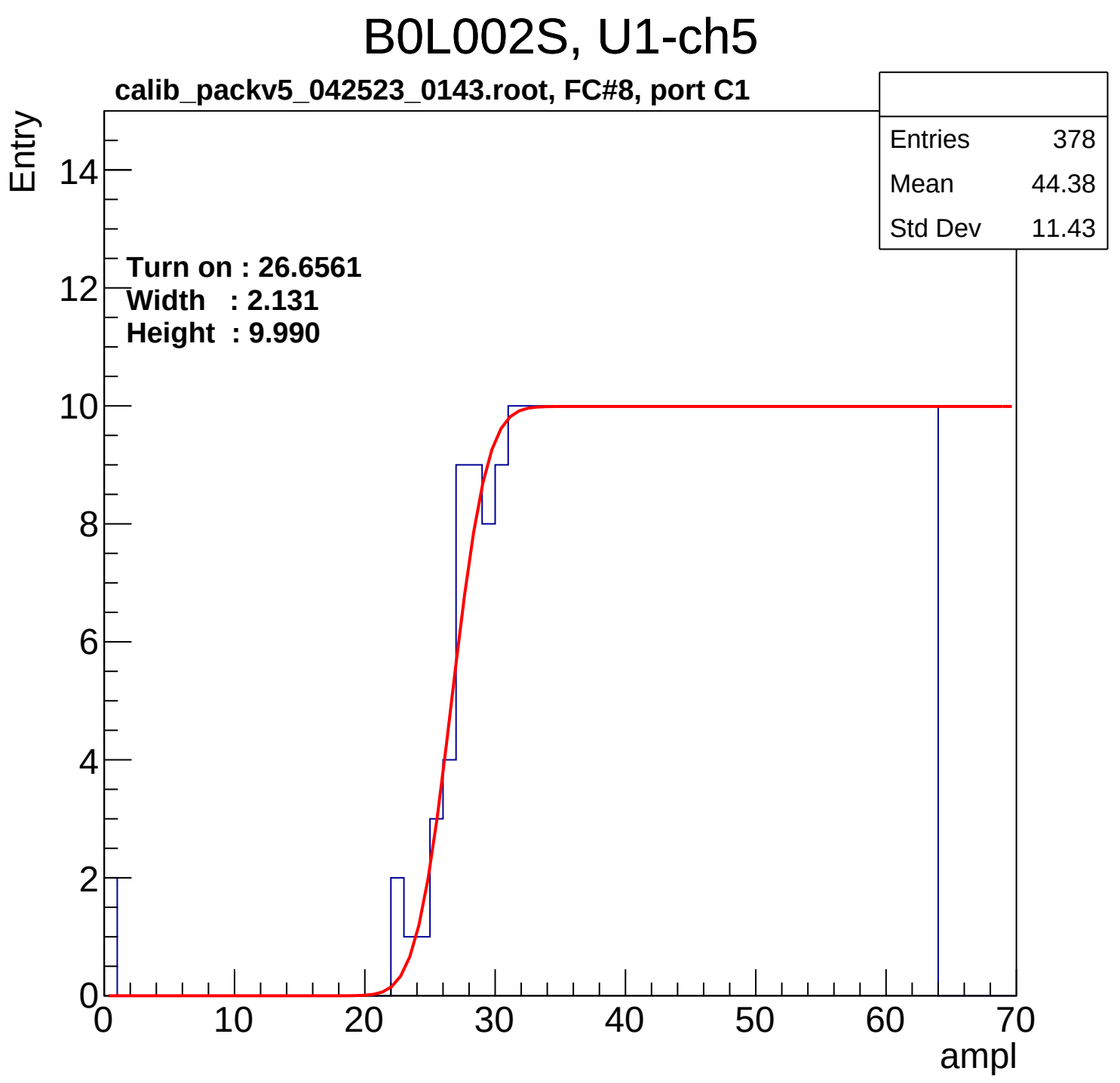
B0L002S, U1-ch5
calib_packv5_042523_0143.root, FC#8, port C1
Entries 378
Mean 44.38
Std Dev 11.43
Turn on : 26.6561
Width : 2.131
Height : 9.990
Entry
ampl
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2
4
6
8
10
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0
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60
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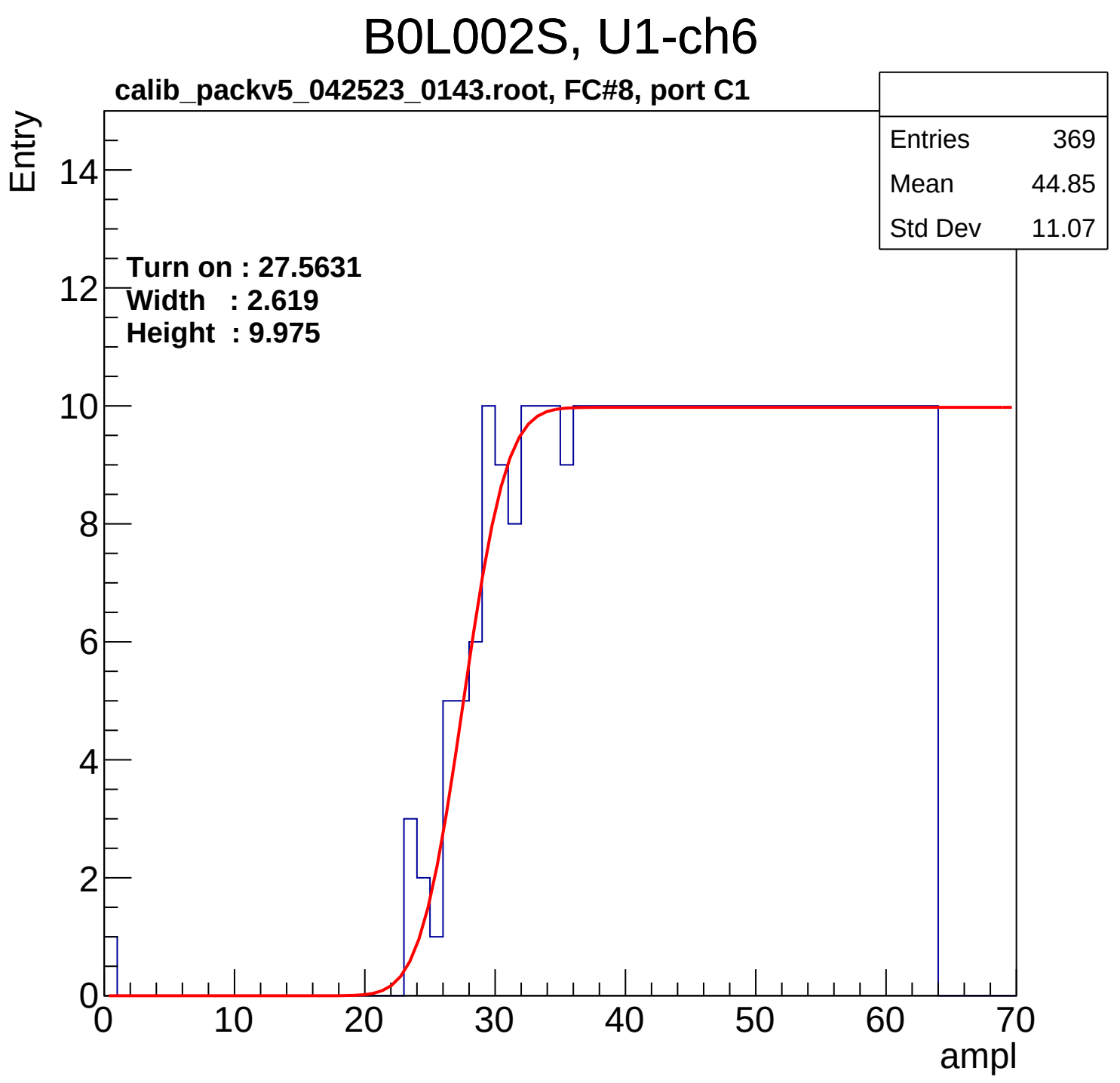
B0L002S, U1-ch6
calib_packv5_042523_0143.root, FC#8, port C1
Entries 369
Mean 44.85
Std Dev 11.07
Turn on : 27.5631
Width : 2.619
Height : 9.975
Entry
ampl
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2
4
6
8
10
12
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0
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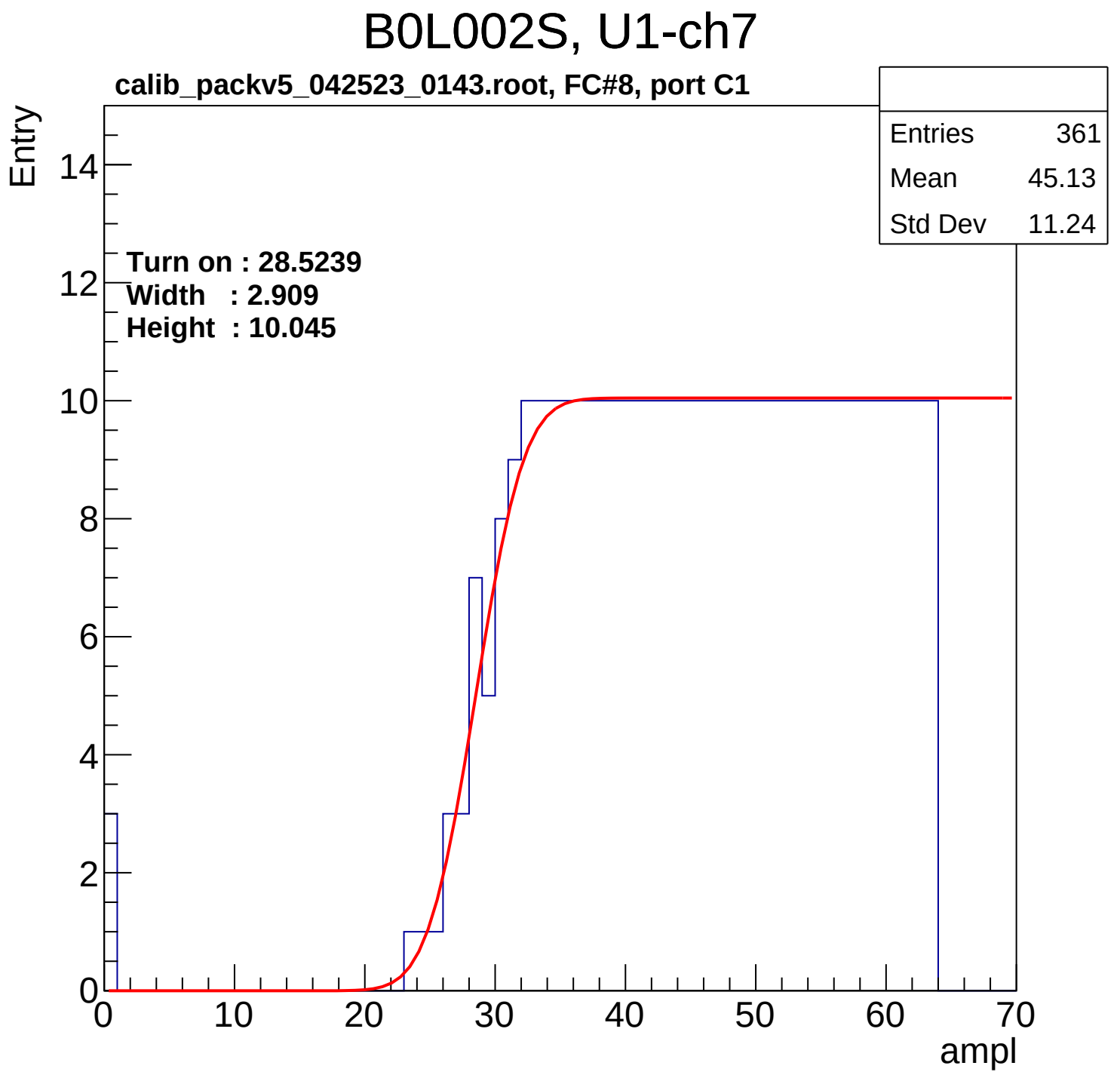
B0L002S, U1-ch7
calib_packv5_042523_0143.root, FC#8, port C1
Entries 361
Mean 45.13
Std Dev 11.24
Turn on : 28.5239
Width : 2.909
Height : 10.045
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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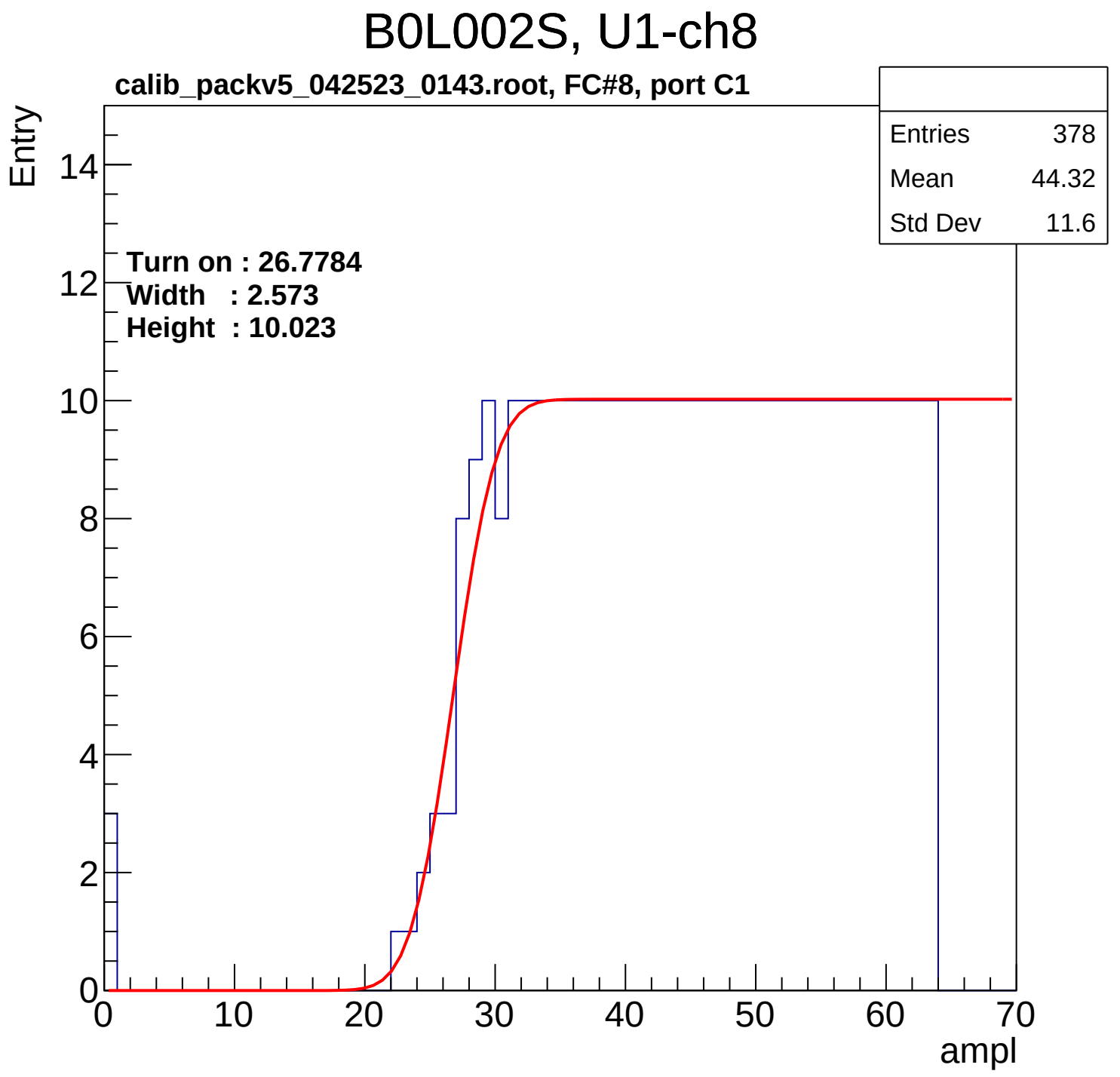
B0L002S, U1-ch8
calib_packv5_042523_0143.root, FC#8, port C1
Entries 378
Mean 44.32
Std Dev 11.6
Turn on : 26.7784
Width : 2.573
Height : 10.023
Entry
ampl
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2
4
6
8
10
12
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0
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20
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60
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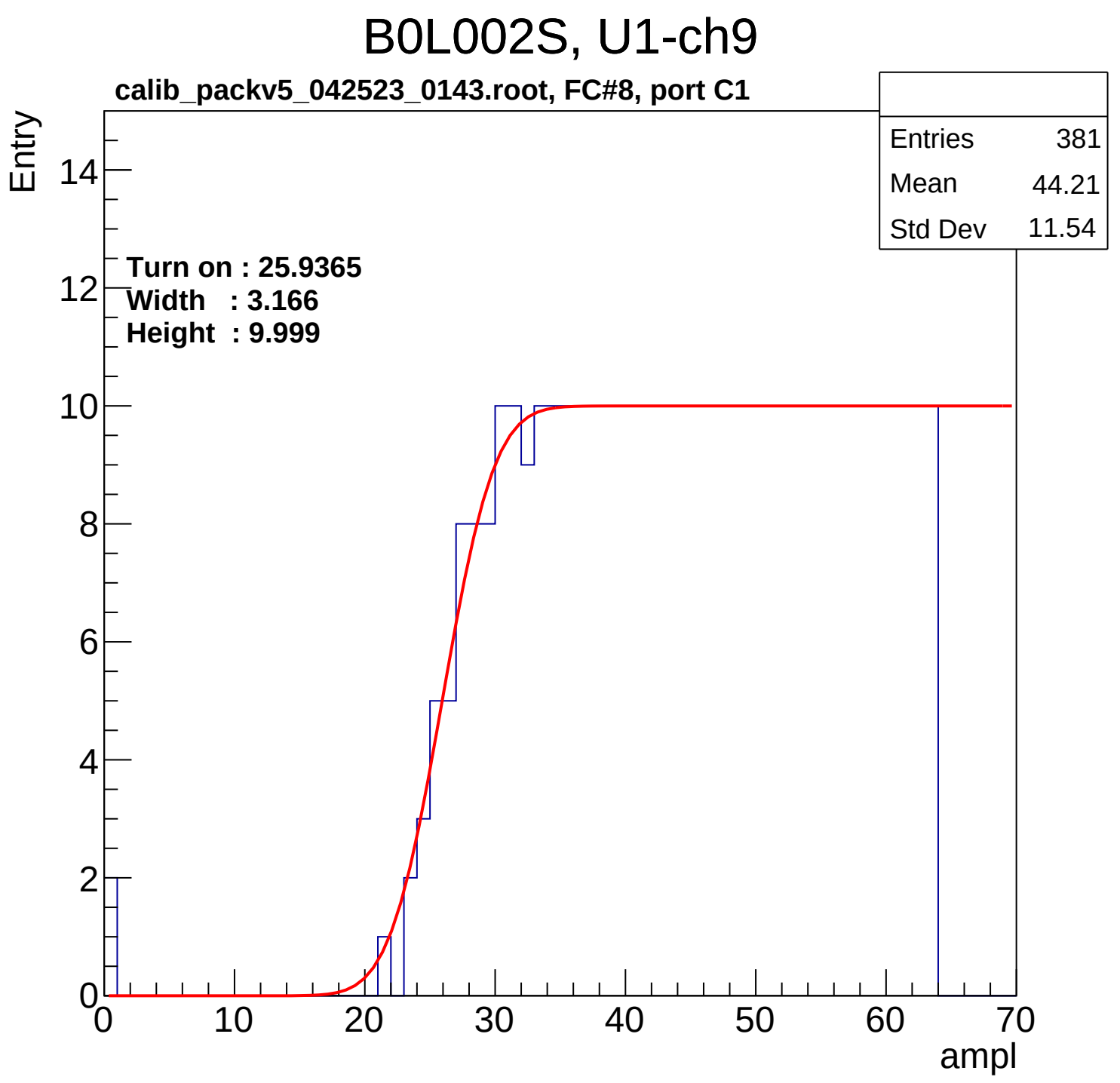
B0L002S, U1-ch9
calib_packv5_042523_0143.root, FC#8, port C1
Entries 381
Mean 44.21
Std Dev 11.54
Turn on : 25.9365
Width : 3.166
Height : 9.999
Entry
ampl
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2
4
6
8
10
12
14
0
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40
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60
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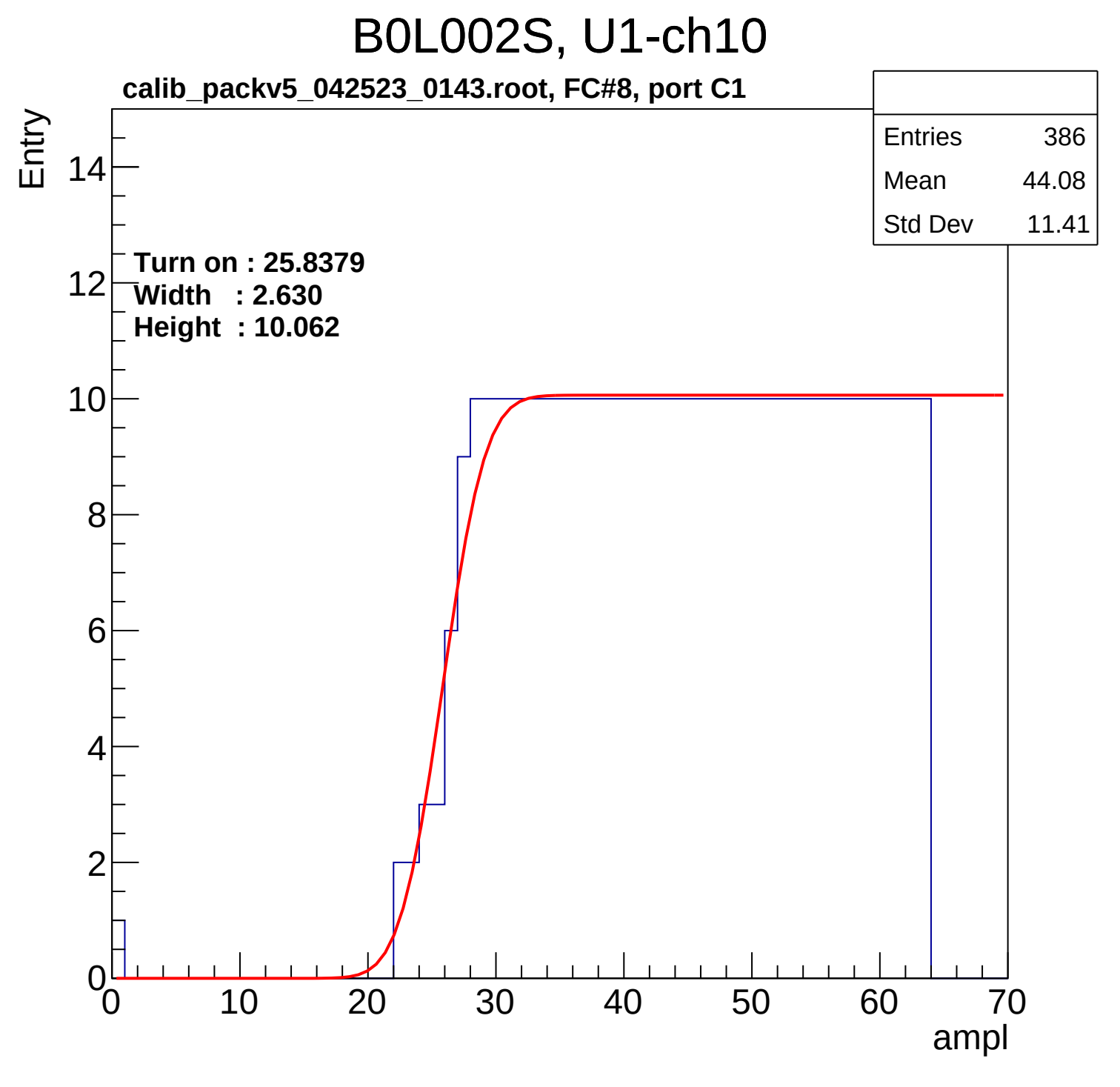
B0L002S, U1-ch10
calib_packv5_042523_0143.root, FC#8, port C1
Entries 386
Mean 44.08
Std Dev 11.41
Turn on : 25.8379
Width : 2.630
Height : 10.062
Entry
ampl
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2
4
6
8
10
12
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0
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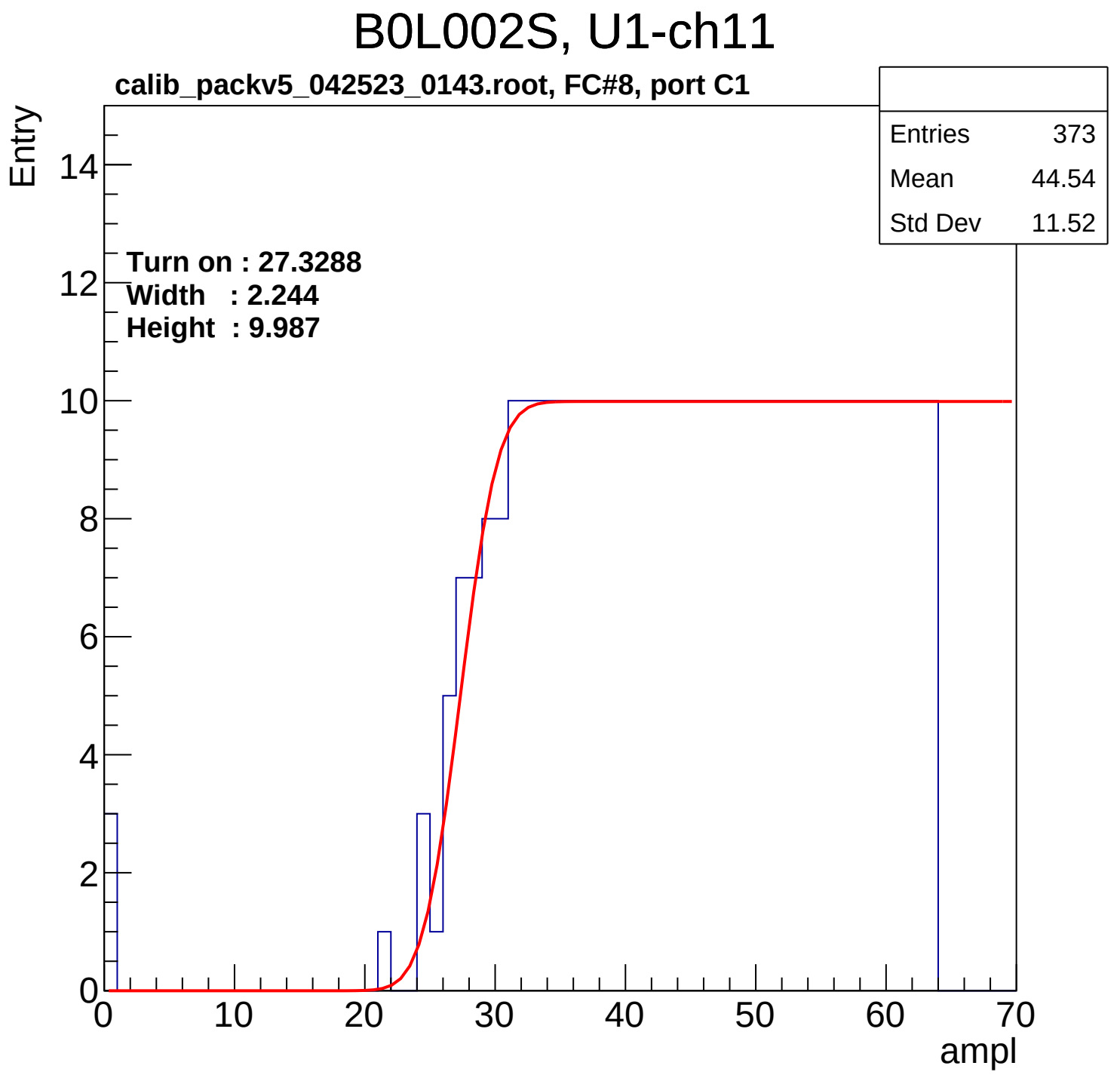
B0L002S, U1-ch11
calib_packv5_042523_0143.root, FC#8, port C1
Entries 373
Mean 44.54
Std Dev 11.52
Turn on : 27.3288
Width : 2.244
Height : 9.987
Entry
ampl
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4
6
8
10
12
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0
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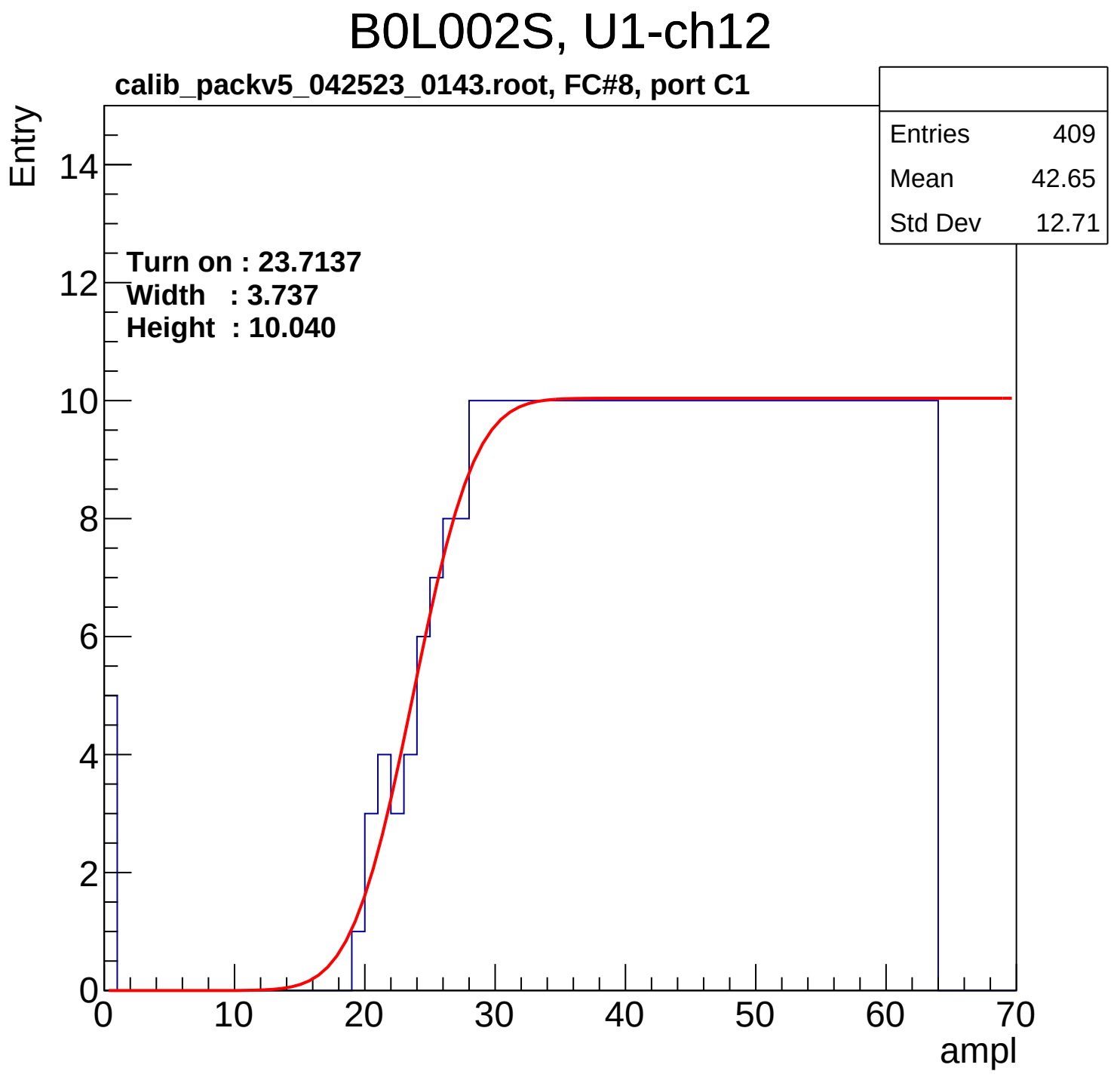
B0L002S, U1-ch12
calib_packv5_042523_0143.root, FC#8, port C1
Entries 409
Mean 42.65
Std Dev 12.71
Turn on : 23.7137
Width : 3.737
Height : 10.040
Entry
ampl
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2
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6
8
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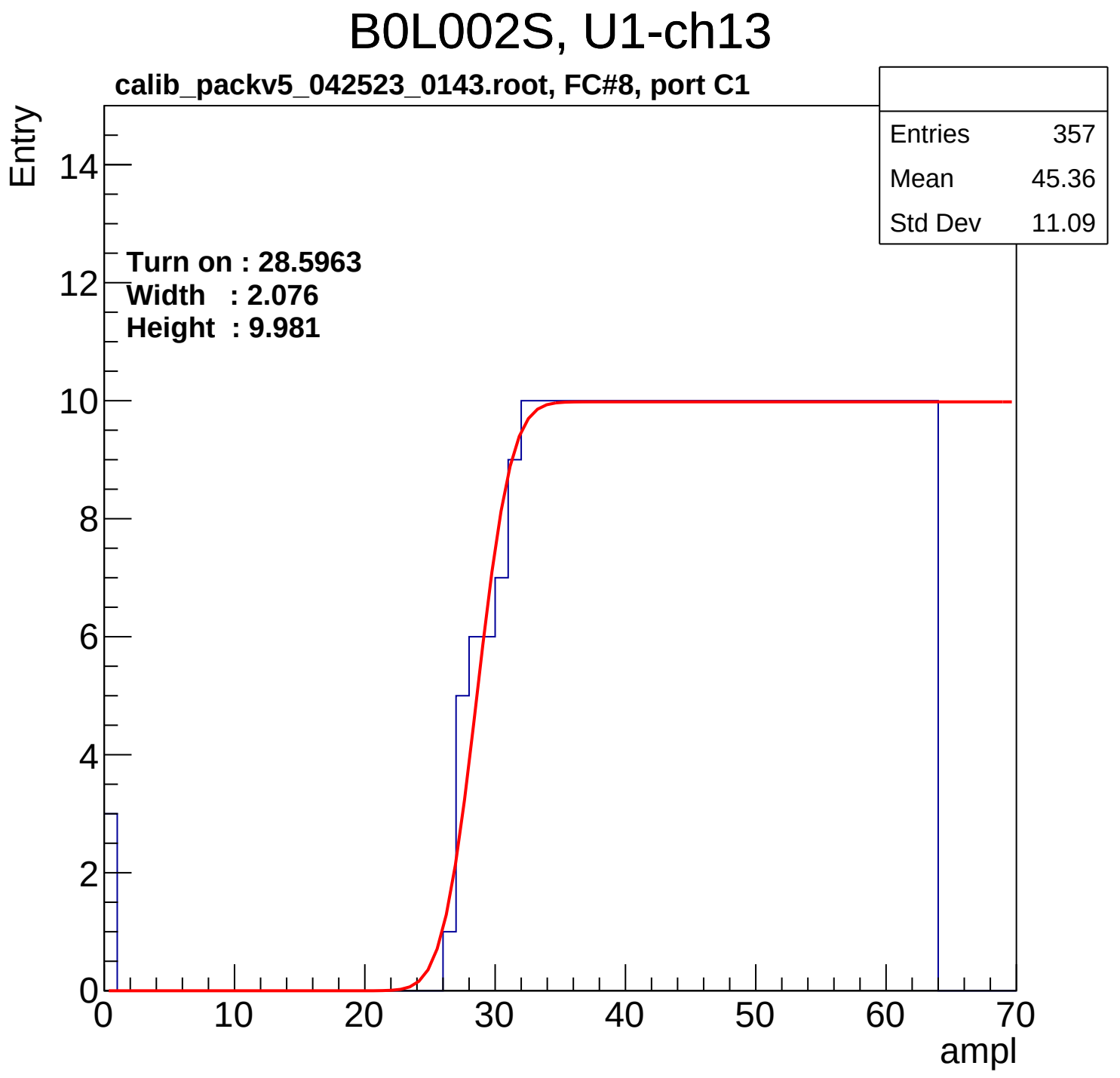
B0L002S, U1-ch13
calib_packv5_042523_0143.root, FC#8, port C1
Entries 357
Mean 45.36
Std Dev 11.09
Turn on : 28.5963
Width : 2.076
Height : 9.981
Entry
ampl
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6
8
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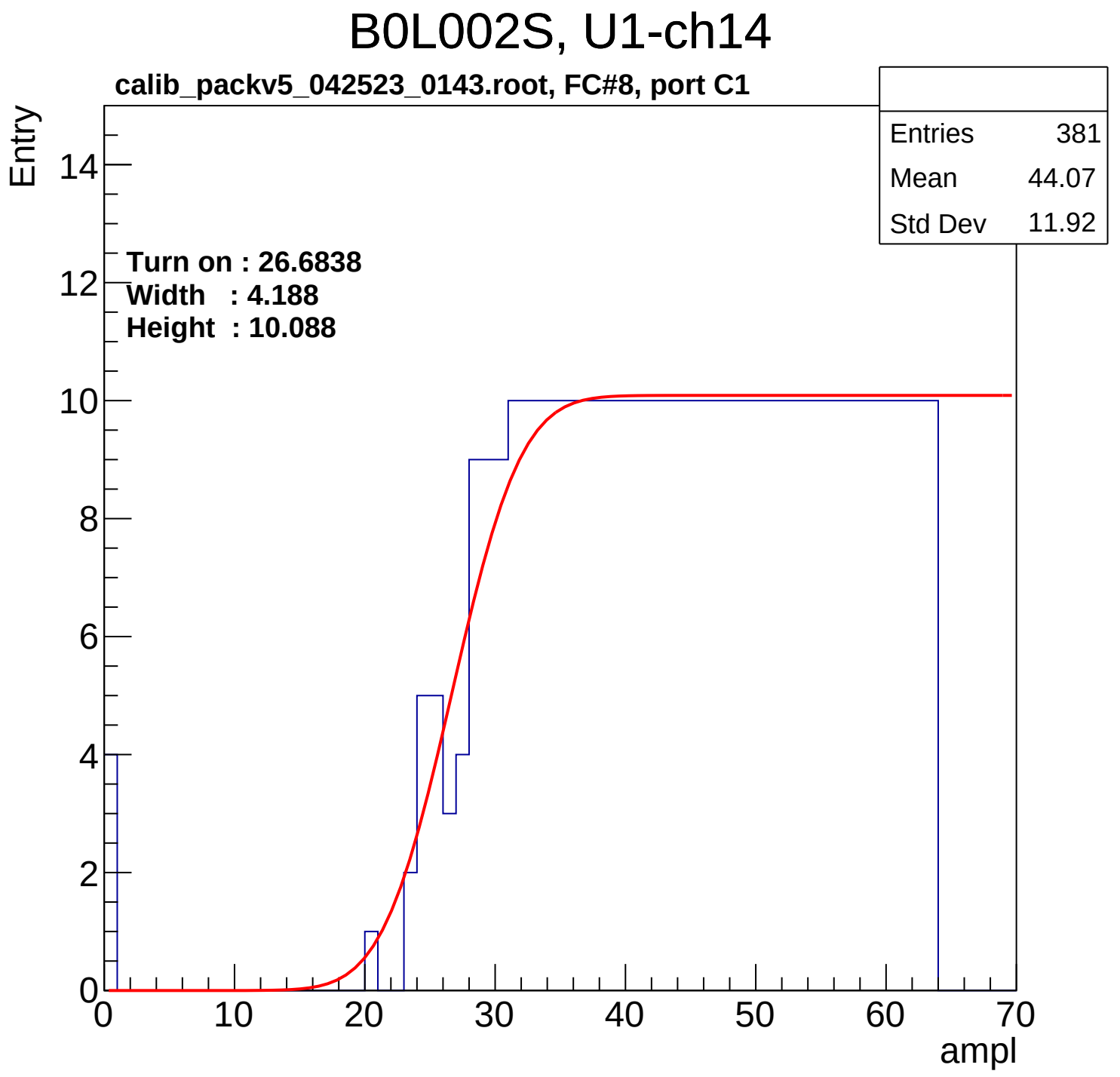
B0L002S, U1-ch14
calib_packv5_042523_0143.root, FC#8, port C1
Entries 381
Mean 44.07
Std Dev 11.92
Turn on : 26.6838
Width : 4.188
Height : 10.088
Entry
ampl
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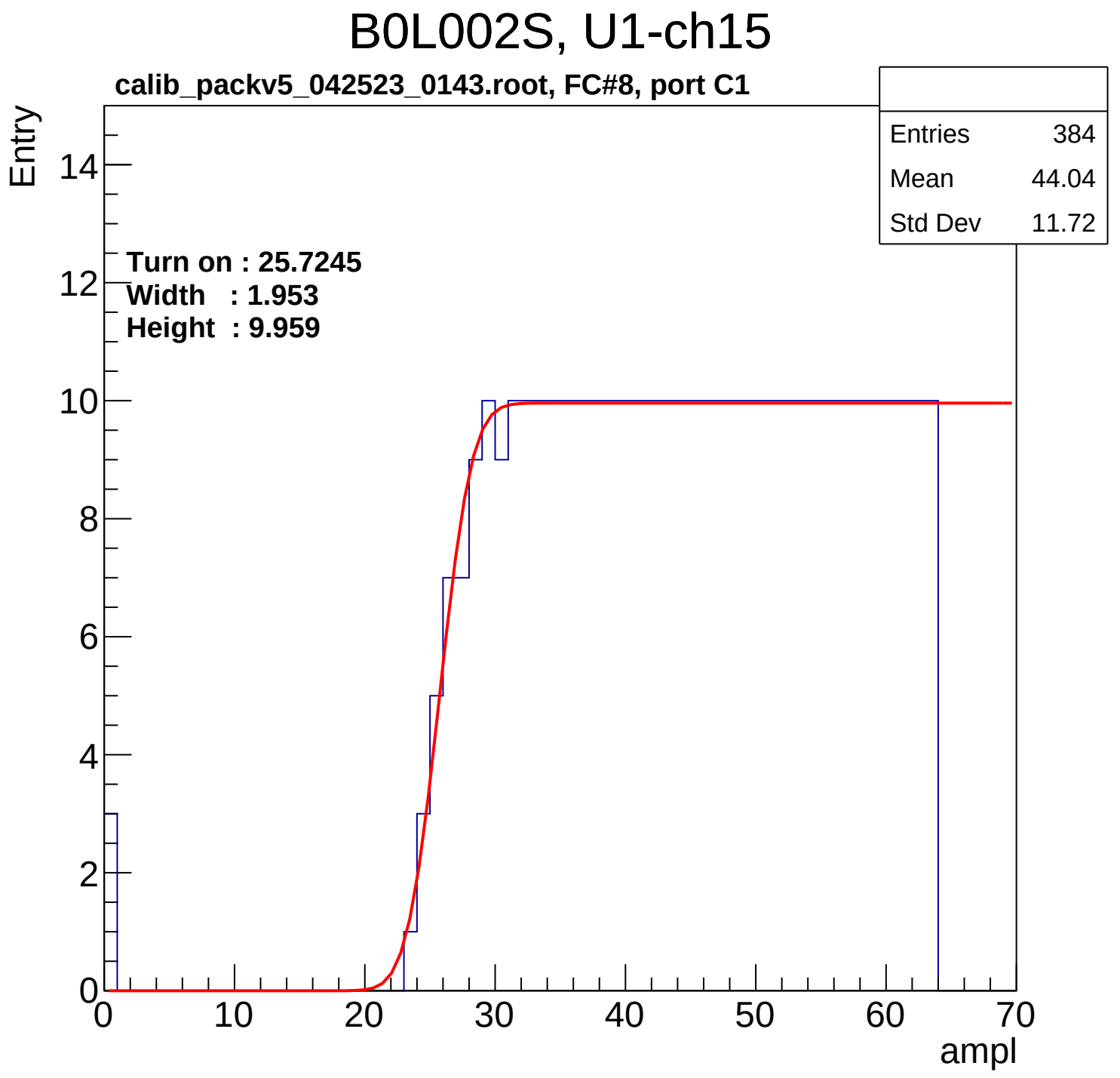
B0L002S, U1-ch15
calib_packv5_042523_0143.root, FC#8, port C1
Entries 384
Mean 44.04
Std Dev 11.72
Turn on : 25.7245
Width : 1.953
Height : 9.959
Entry
ampl
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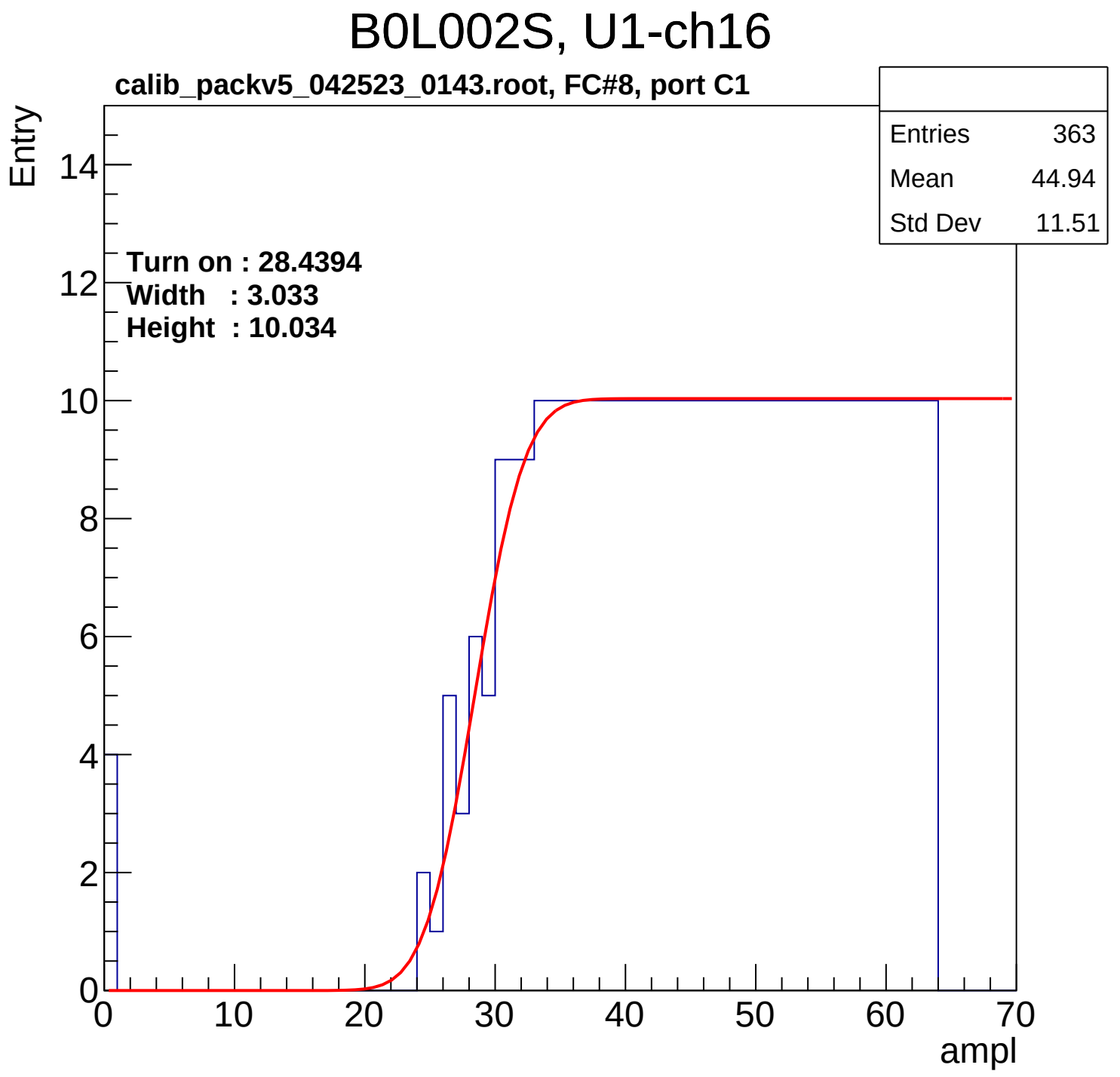
B0L002S, U1-ch16
calib_packv5_042523_0143.root, FC#8, port C1
Entries 363
Mean 44.94
Std Dev 11.51
Turn on : 28.4394
Width : 3.033
Height : 10.034
Entry
ampl
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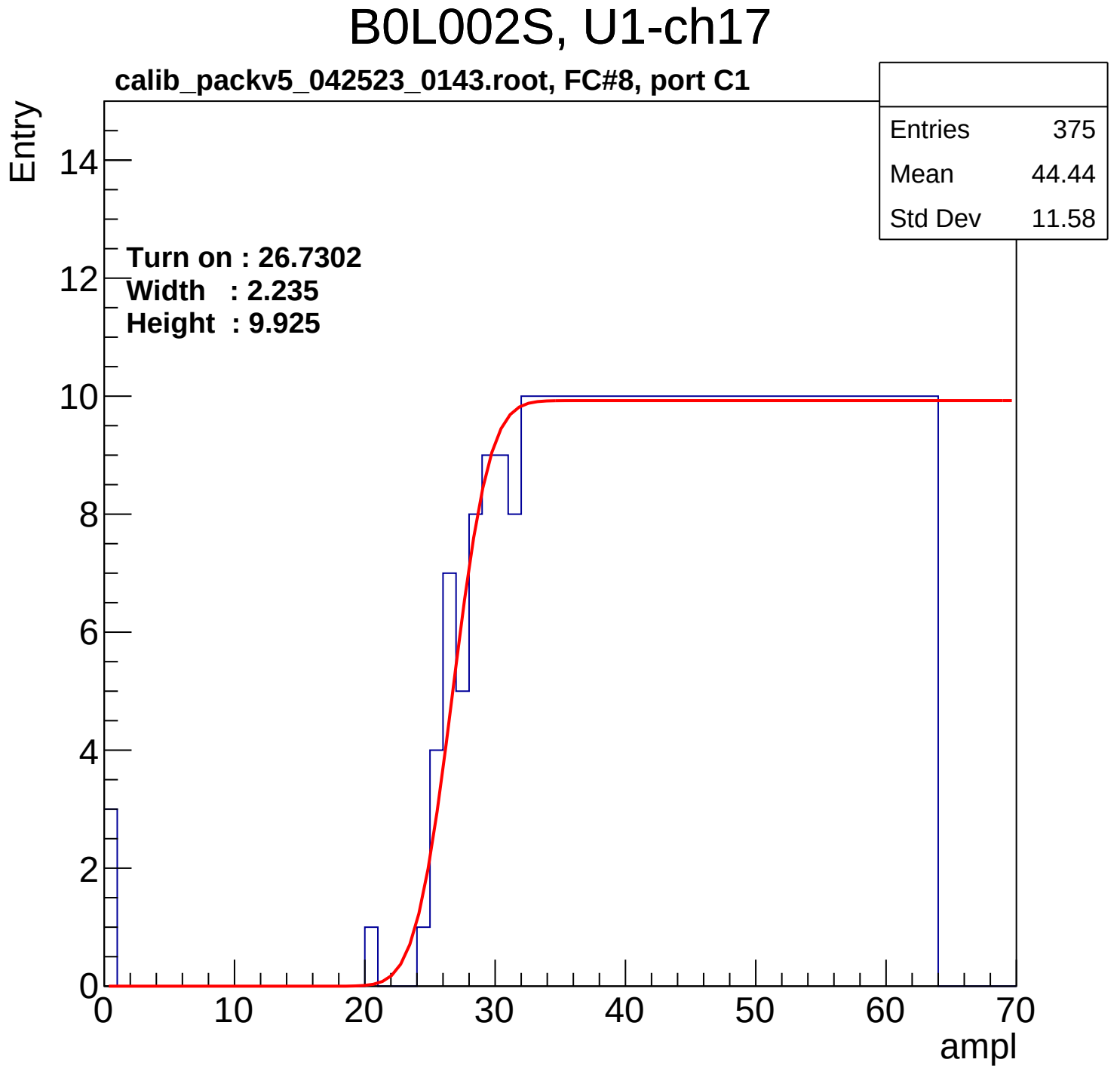
B0L002S, U1-ch17
calib_packv5_042523_0143.root, FC#8, port C1
Entries 375
Mean 44.44
Std Dev 11.58
Turn on : 26.7302
Width : 2.235
Height : 9.925
Entry
ampl
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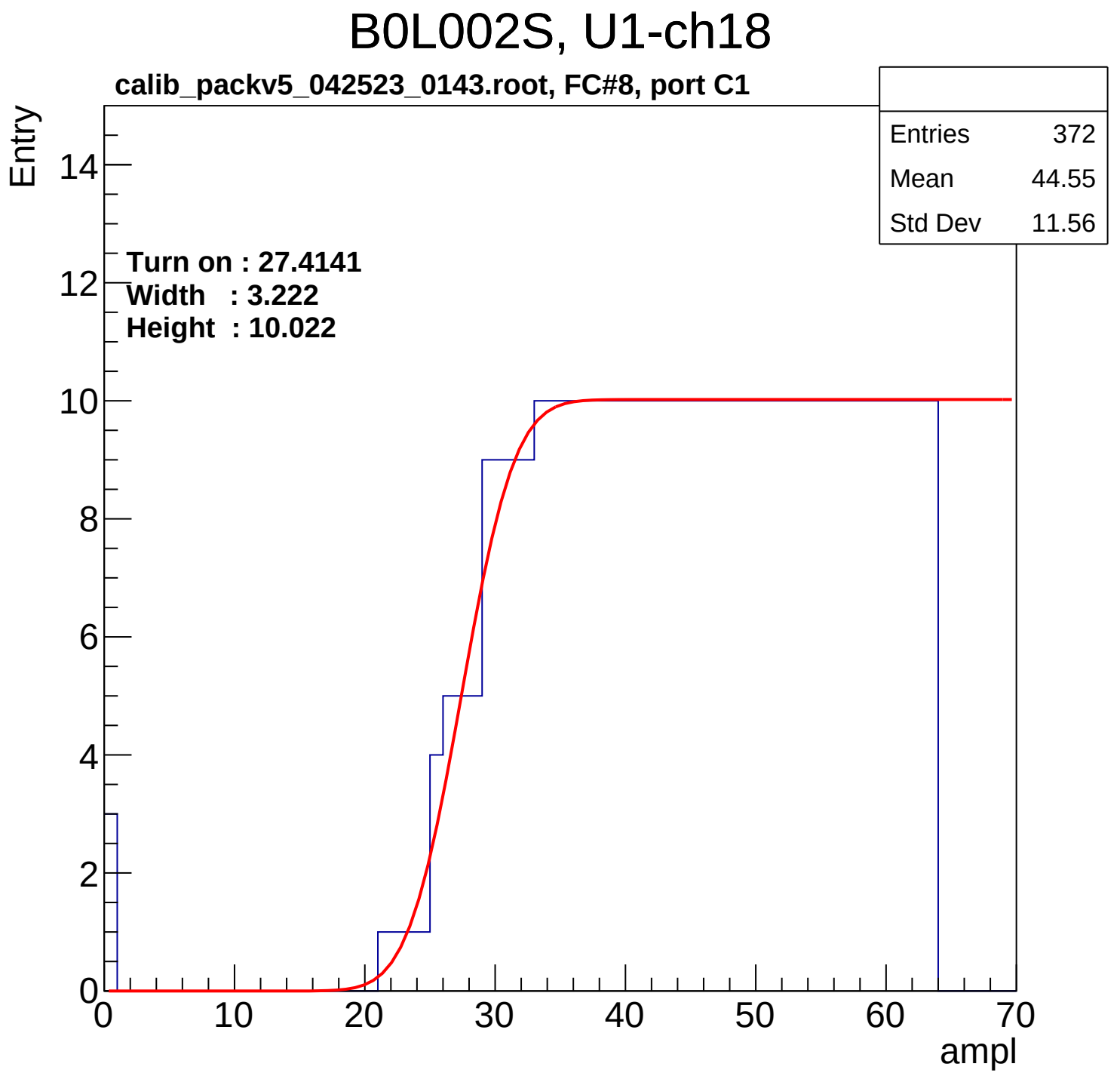
B0L002S, U1-ch18
calib_packv5_042523_0143.root, FC#8, port C1
Entries 372
Mean 44.55
Std Dev 11.56
Turn on : 27.4141
Width : 3.222
Height : 10.022
Entry
ampl
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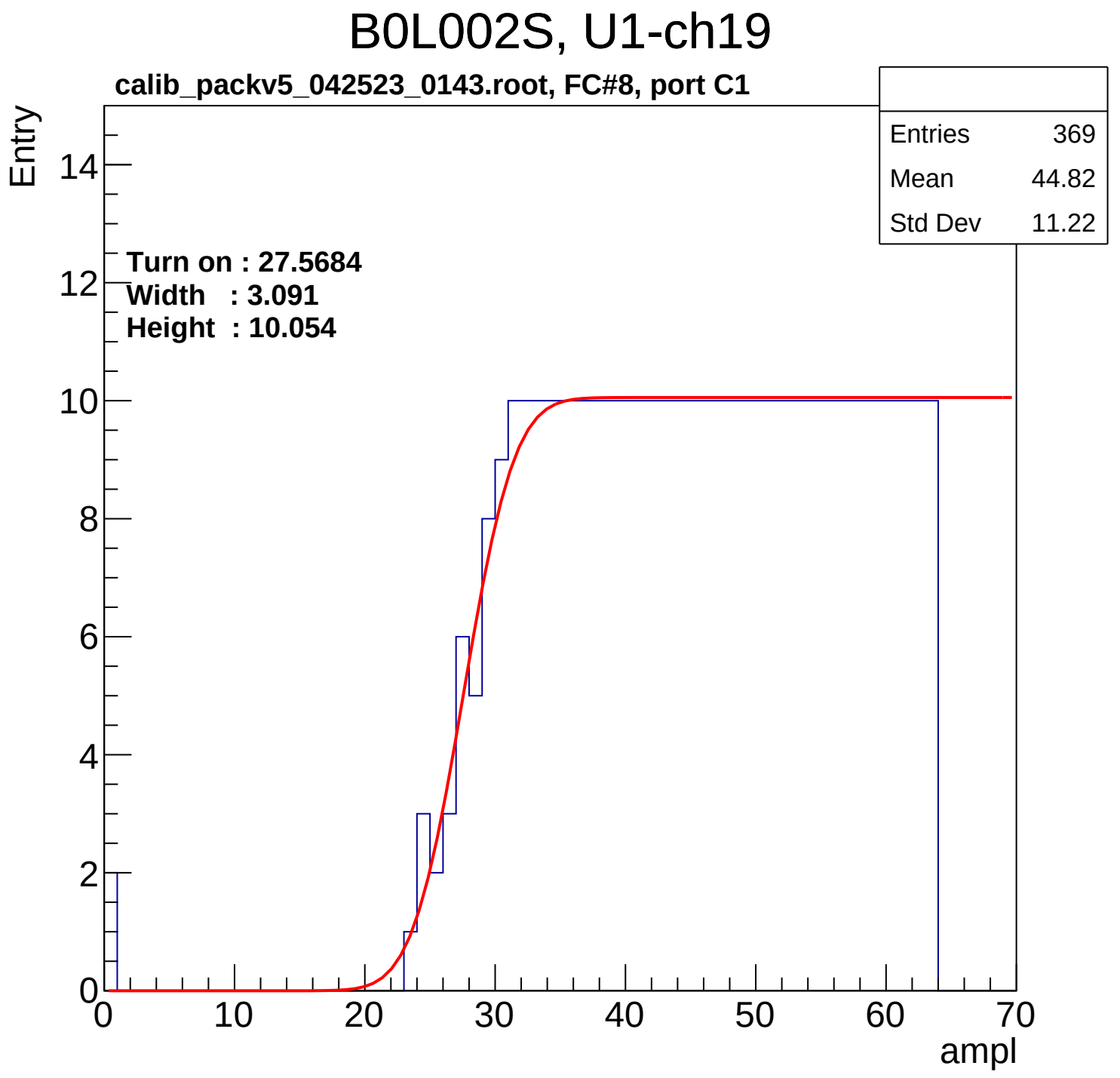
B0L002S, U1-ch19
calib_packv5_042523_0143.root, FC#8, port C1
Entries 369
Mean 44.82
Std Dev 11.22
Turn on : 27.5684
Width : 3.091
Height : 10.054
Entry
ampl
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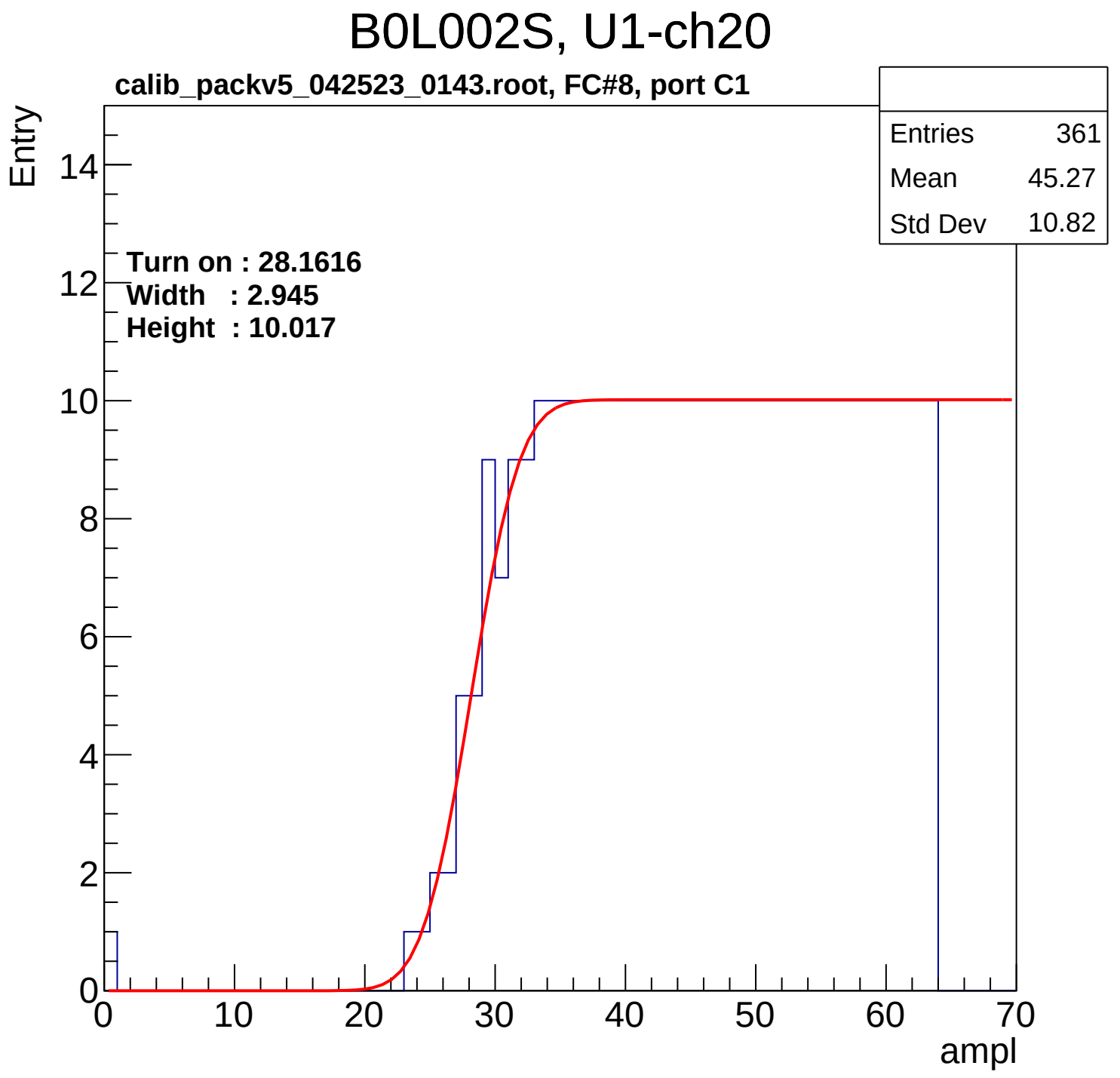
B0L002S, U1-ch20
calib_packv5_042523_0143.root, FC#8, port C1
Entries 361
Mean 45.27
Std Dev 10.82
Turn on : 28.1616
Width : 2.945
Height : 10.017
Entry
ampl
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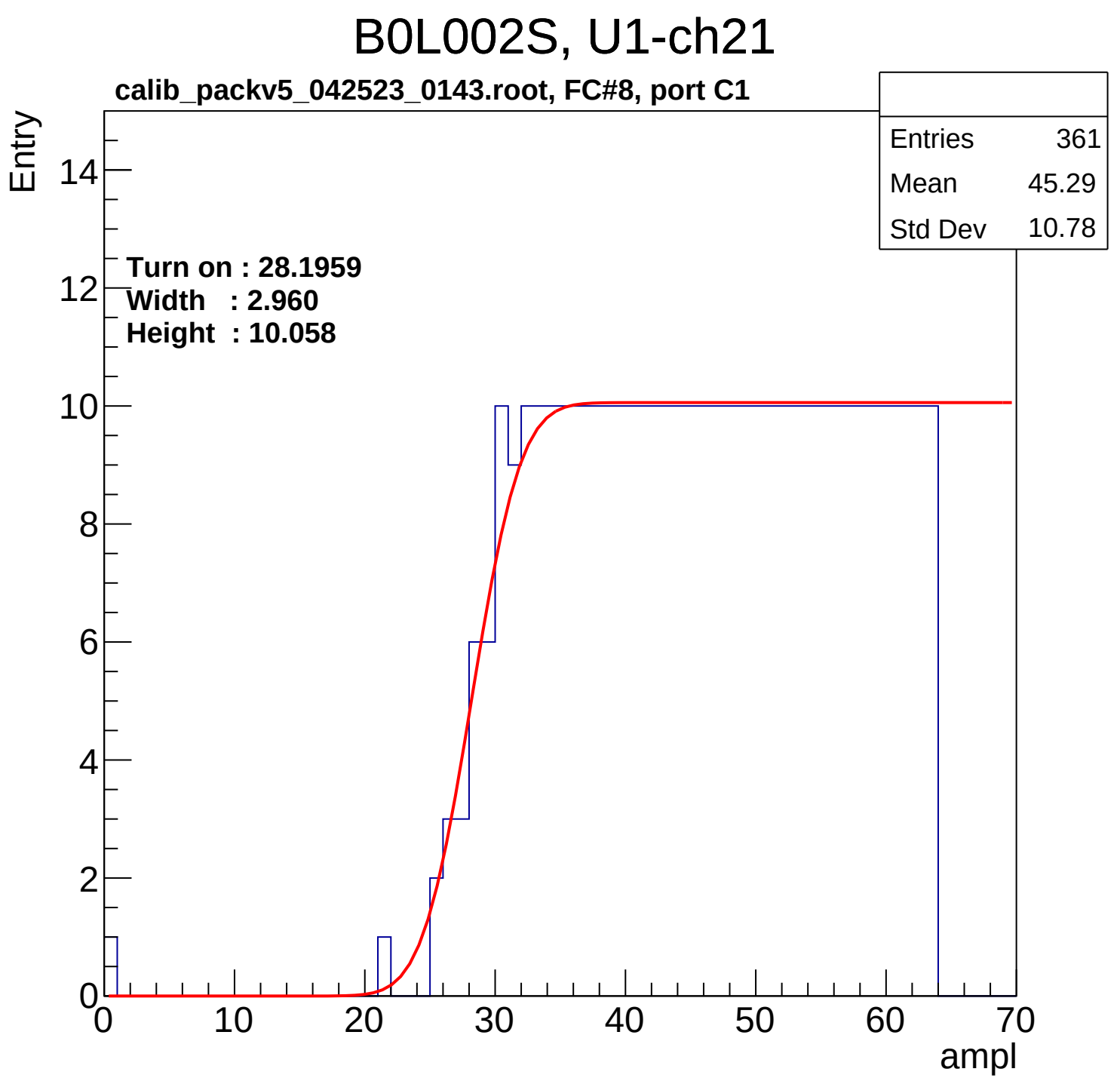
B0L002S, U1-ch21
calib_packv5_042523_0143.root, FC#8, port C1
Entries 361
Mean 45.29
Std Dev 10.78
Turn on : 28.1959
Width : 2.960
Height : 10.058
Entry
ampl
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2
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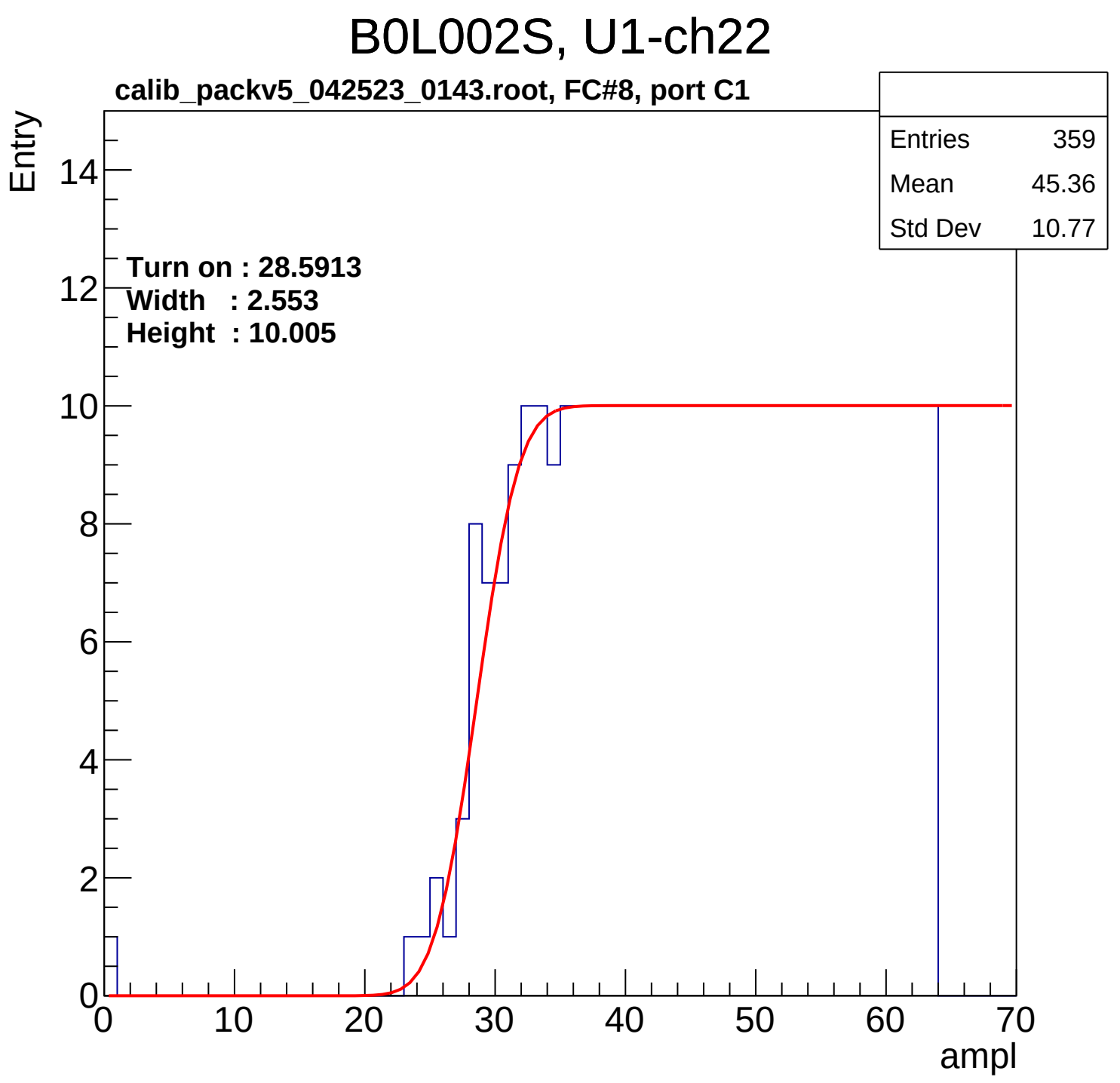
B0L002S, U1-ch22
calib_packv5_042523_0143.root, FC#8, port C1
Entries 359
Mean 45.36
Std Dev 10.77
Turn on : 28.5913
Width : 2.553
Height : 10.005
Entry
ampl
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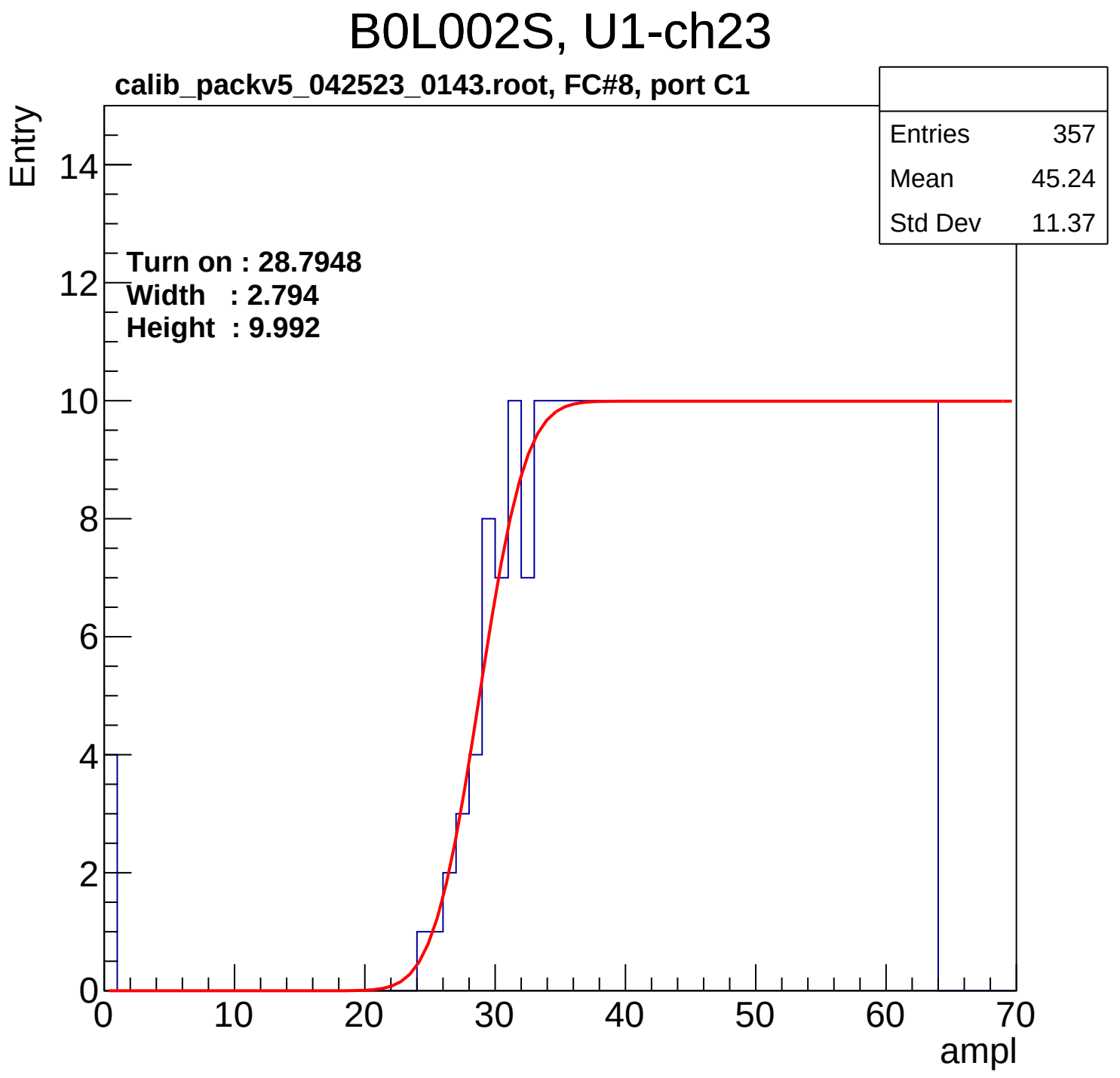
B0L002S, U1-ch23
calib_packv5_042523_0143.root, FC#8, port C1
Entries 357
Mean 45.24
Std Dev 11.37
Turn on : 28.7948
Width : 2.794
Height : 9.992
Entry
ampl
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4
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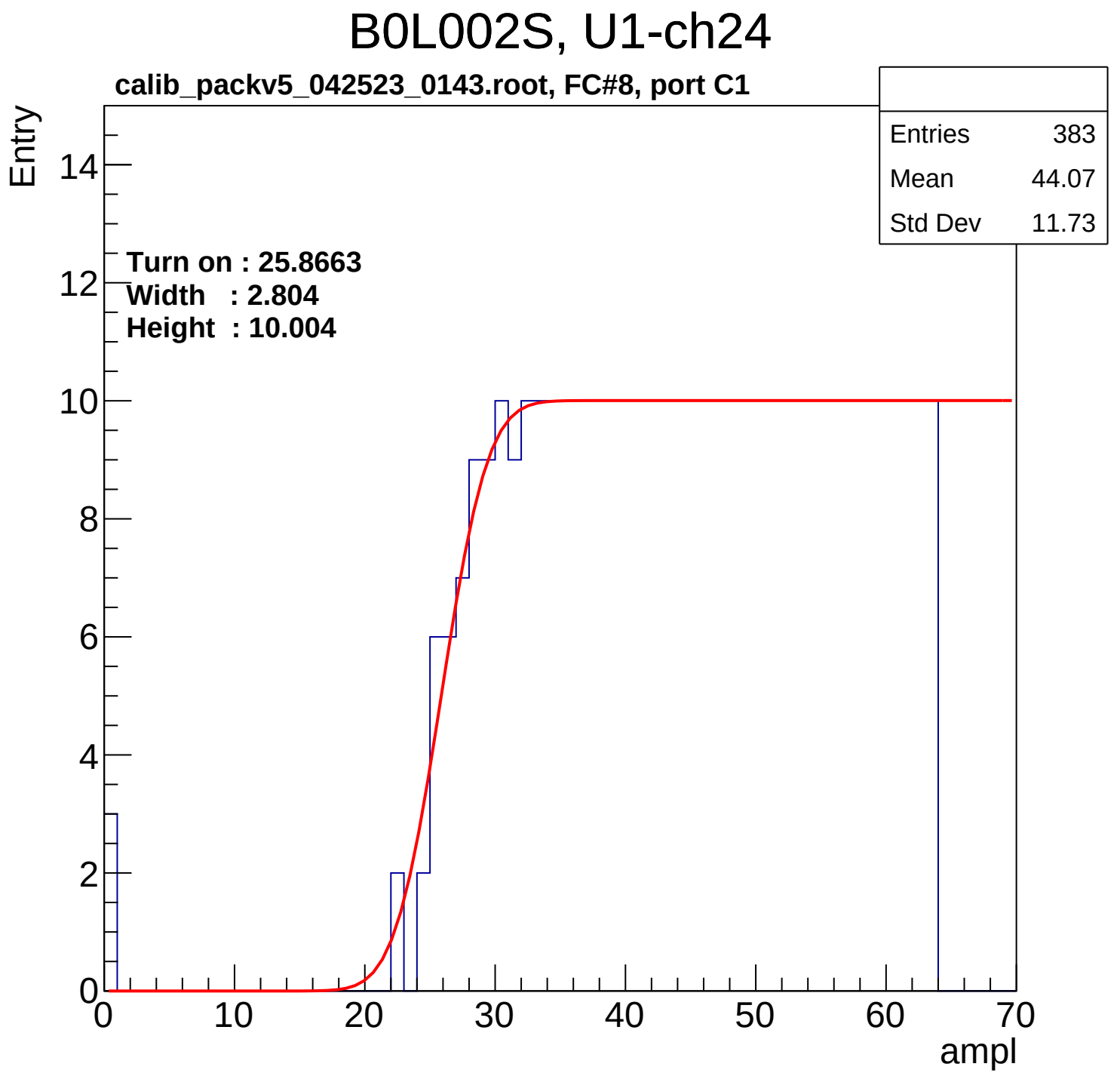
B0L002S, U1-ch24
calib_packv5_042523_0143.root, FC#8, port C1
Entries 383
Mean 44.07
Std Dev 11.73
Turn on : 25.8663
Width : 2.804
Height : 10.004
Entry
ampl
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6
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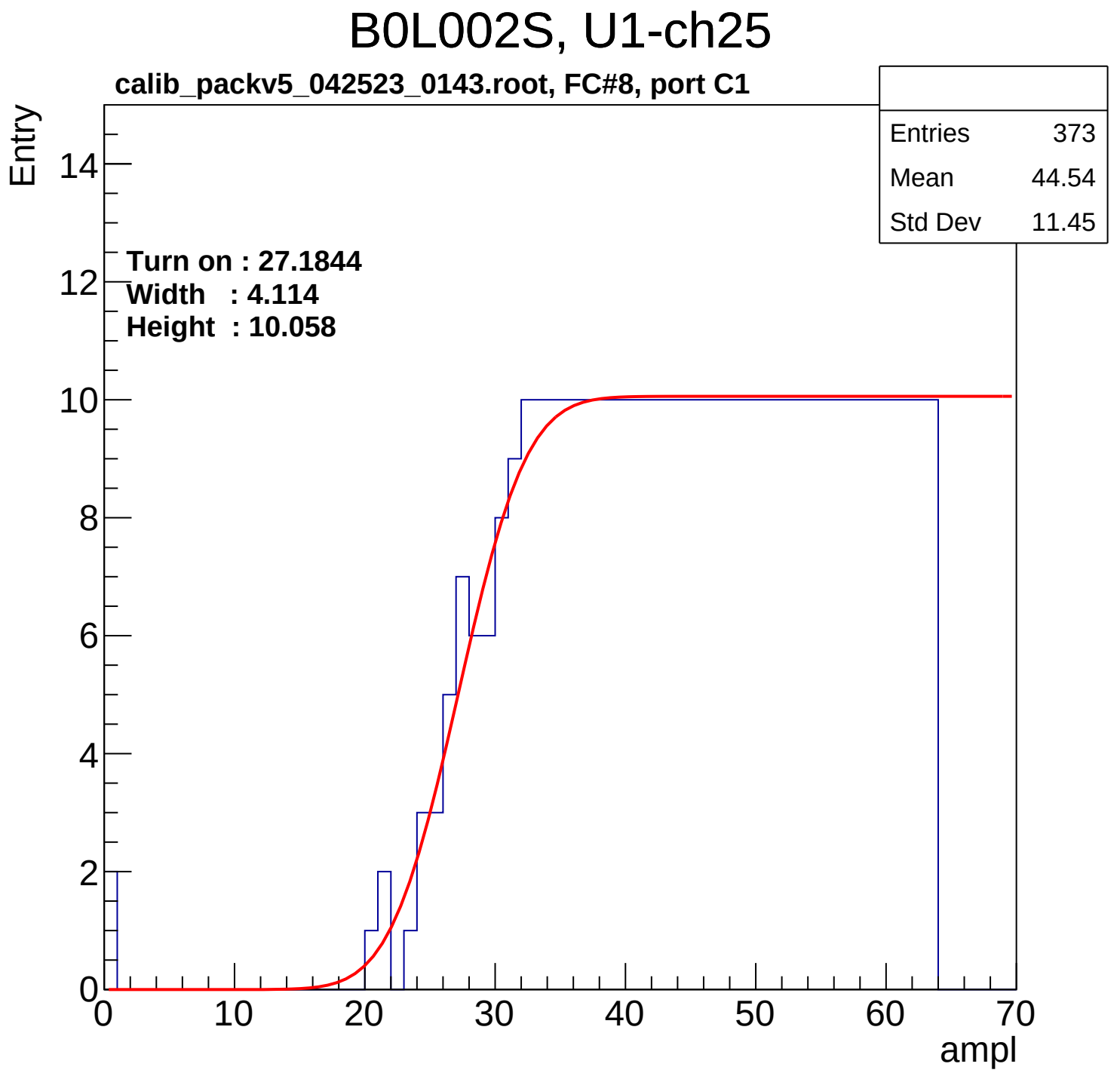
B0L002S, U1-ch25
calib_packv5_042523_0143.root, FC#8, port C1
Entries 373
Mean 44.54
Std Dev 11.45
Turn on : 27.1844
Width : 4.114
Height : 10.058
Entry
ampl
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6
8
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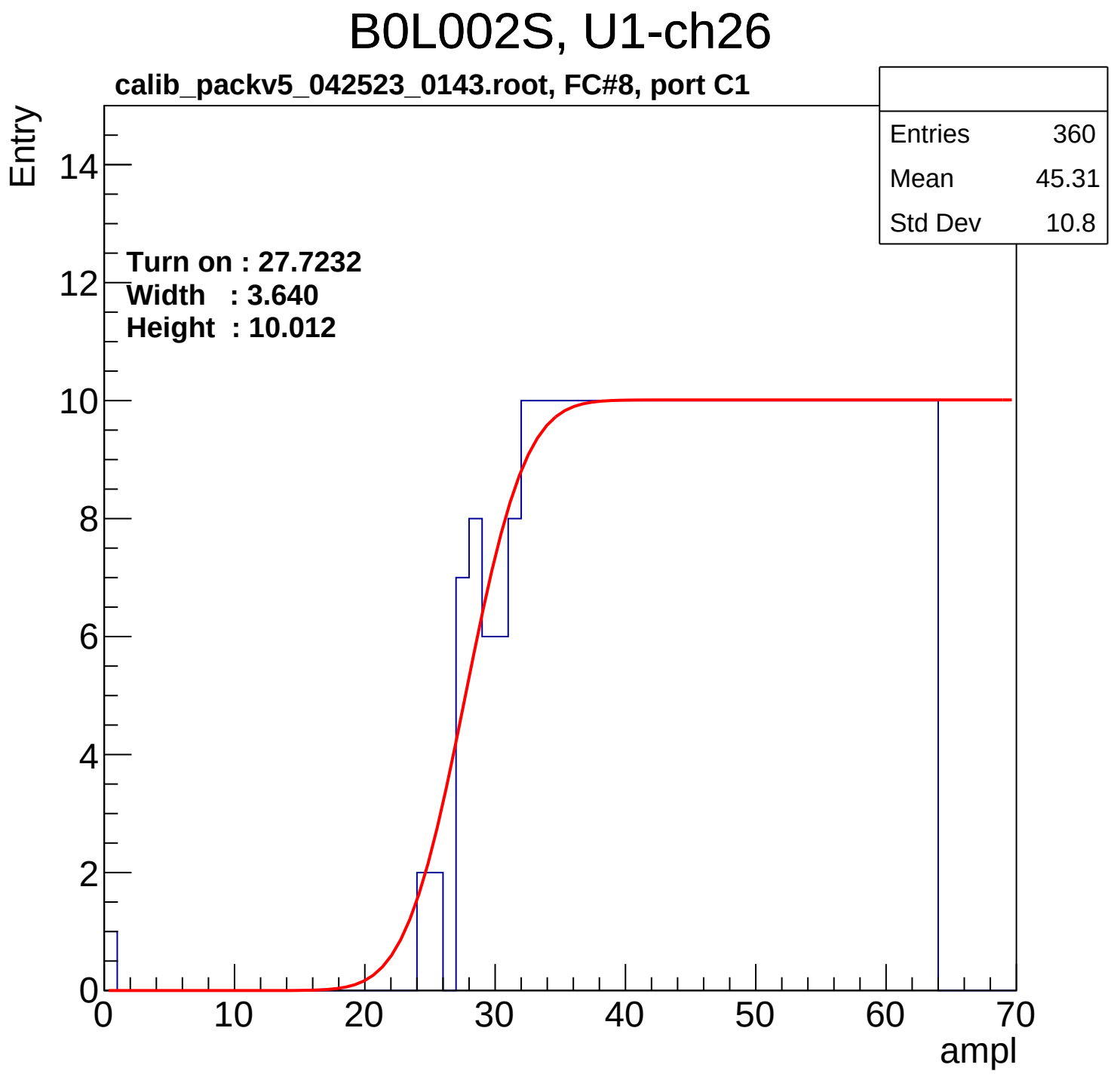
B0L002S, U1-ch26
calib_packv5_042523_0143.root, FC#8, port C1
Entries 360
Mean 45.31
Std Dev 10.8
Turn on : 27.7232
Width : 3.640
Height : 10.012
Entry
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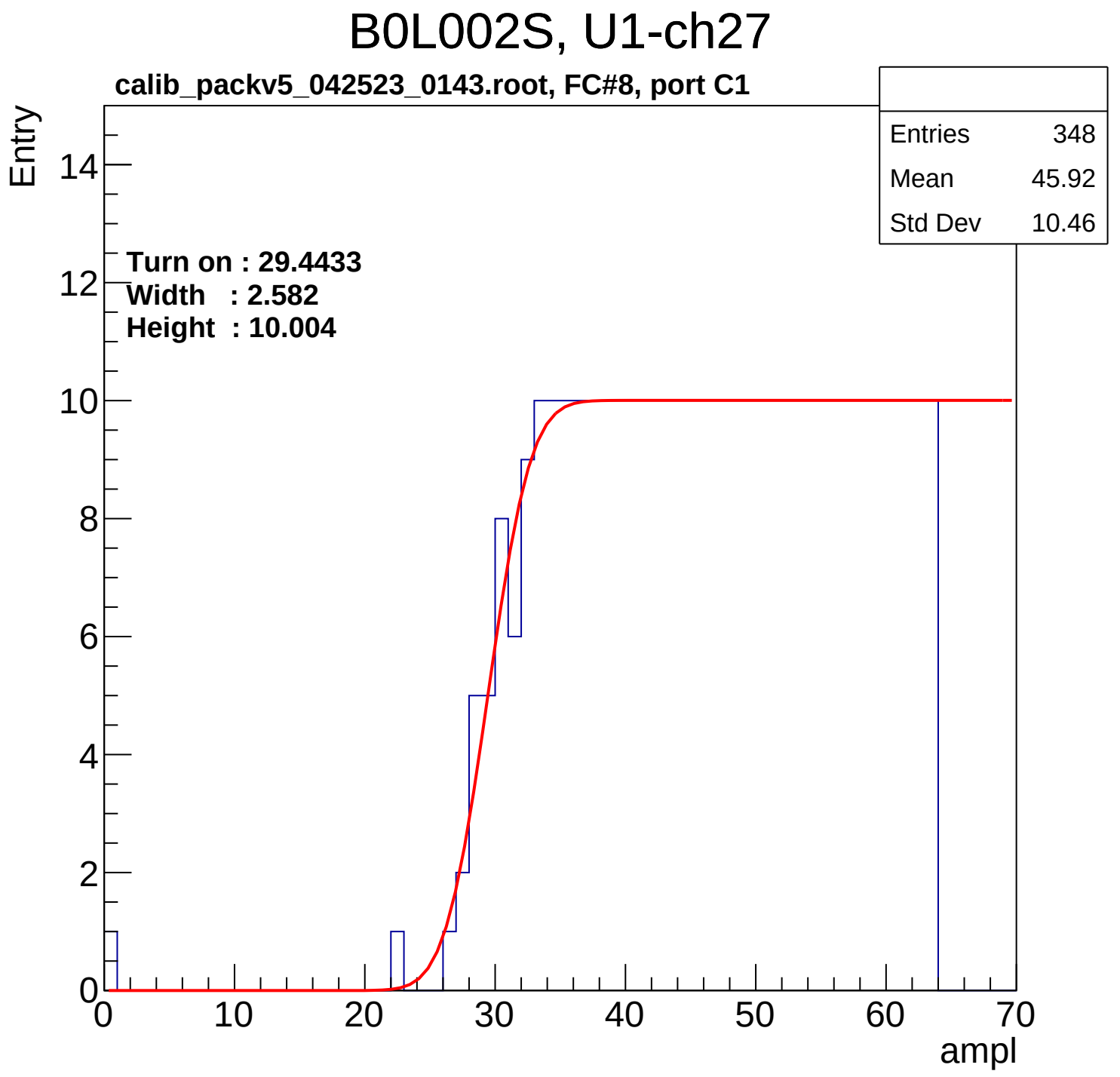
B0L002S, U1-ch27
calib_packv5_042523_0143.root, FC#8, port C1
Entries 348
Mean 45.92
Std Dev 10.46
Turn on : 29.4433
Width : 2.582
Height : 10.004
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ampl
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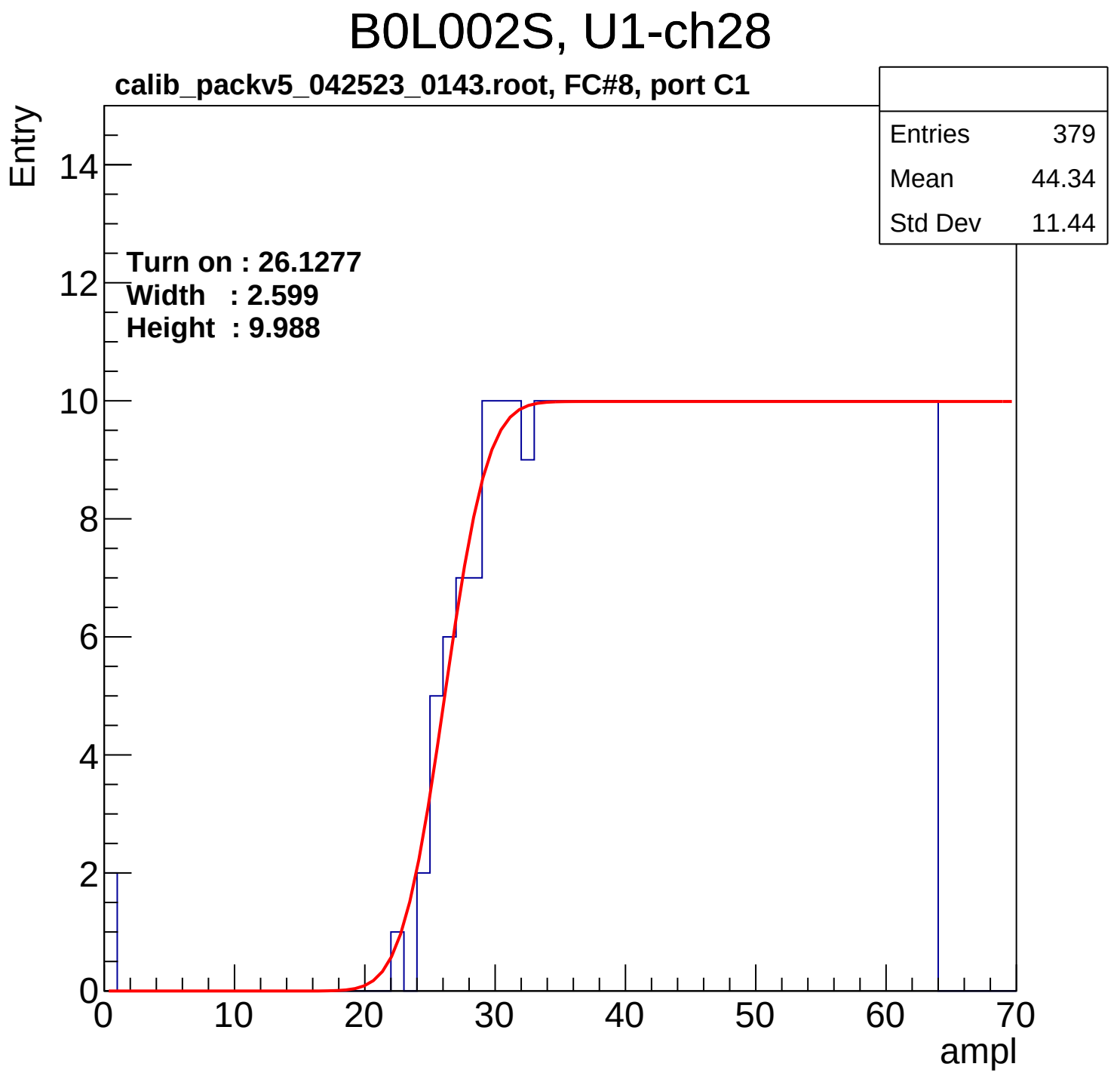
B0L002S, U1-ch28
calib_packv5_042523_0143.root, FC#8, port C1
Entries 379
Mean 44.34
Std Dev 11.44
Turn on : 26.1277
Width : 2.599
Height : 9.988
Entry
ampl
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4
6
8
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12
14
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10
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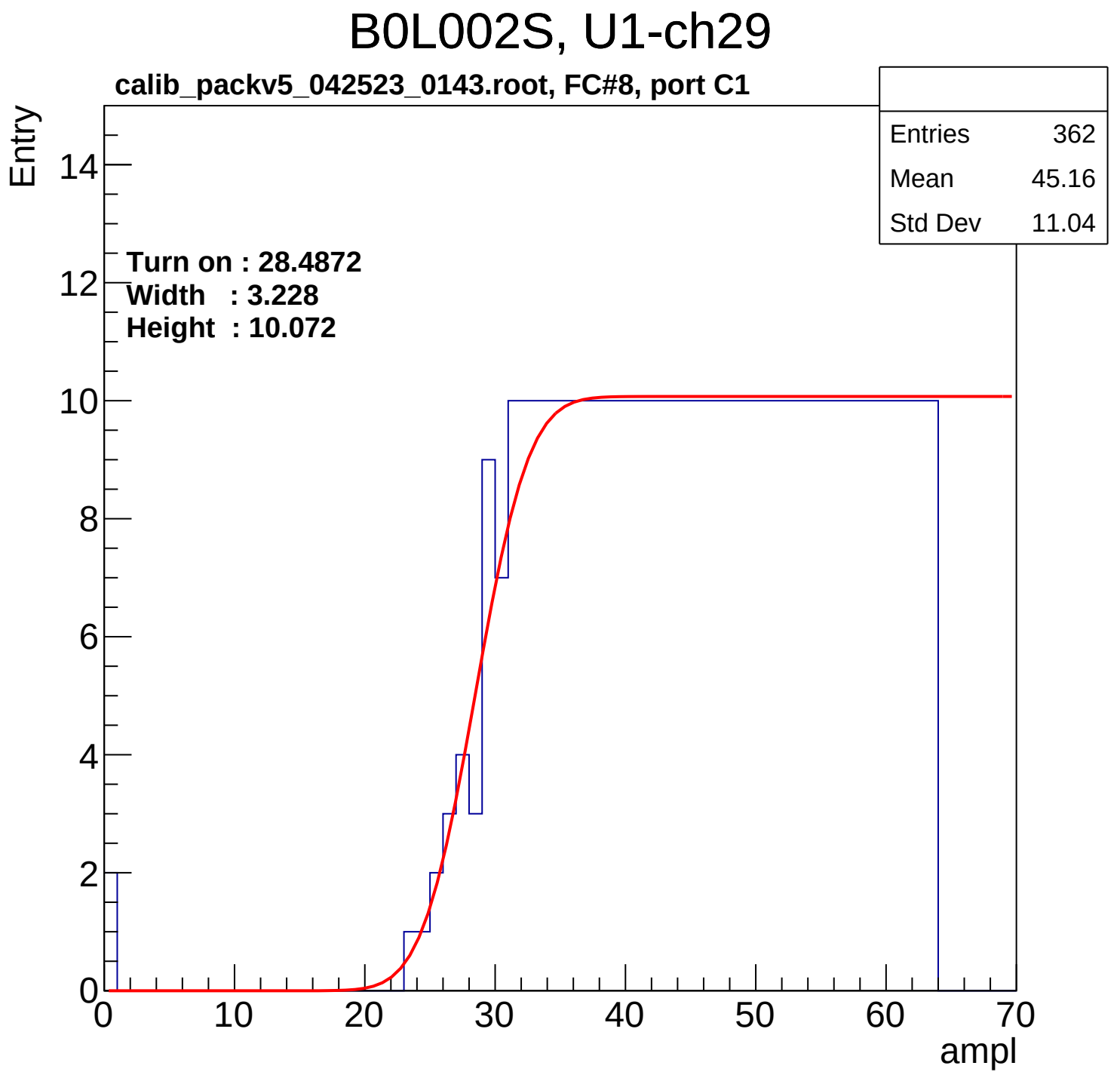
B0L002S, U1-ch29
calib_packv5_042523_0143.root, FC#8, port C1
Entries 362
Mean 45.16
Std Dev 11.04
Turn on : 28.4872
Width : 3.228
Height : 10.072
Entry
ampl
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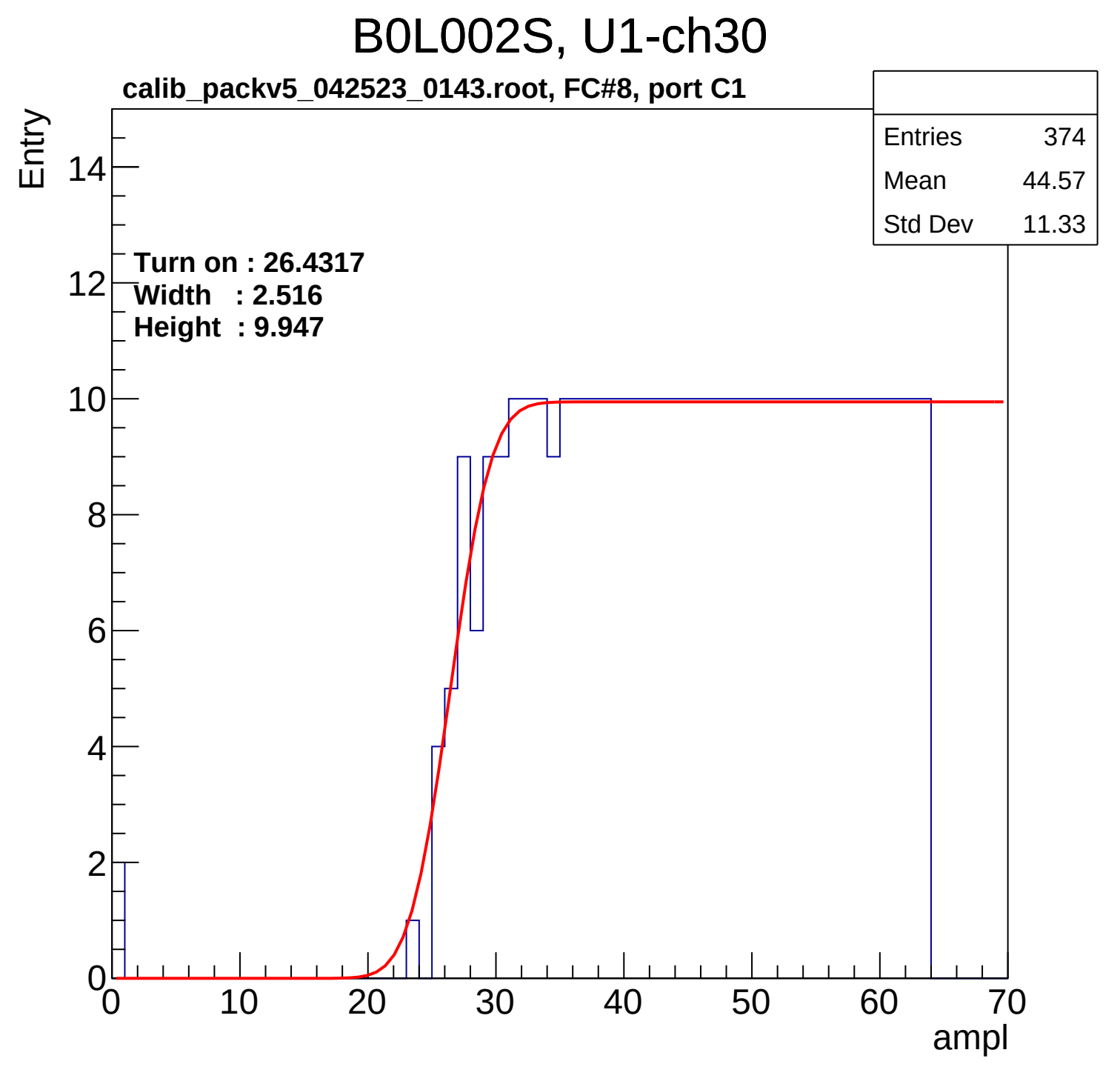
B0L002S, U1-ch30
calib_packv5_042523_0143.root, FC#8, port C1
Entries 374
Mean 44.57
Std Dev 11.33
Turn on : 26.4317
Width : 2.516
Height : 9.947
Entry
ampl
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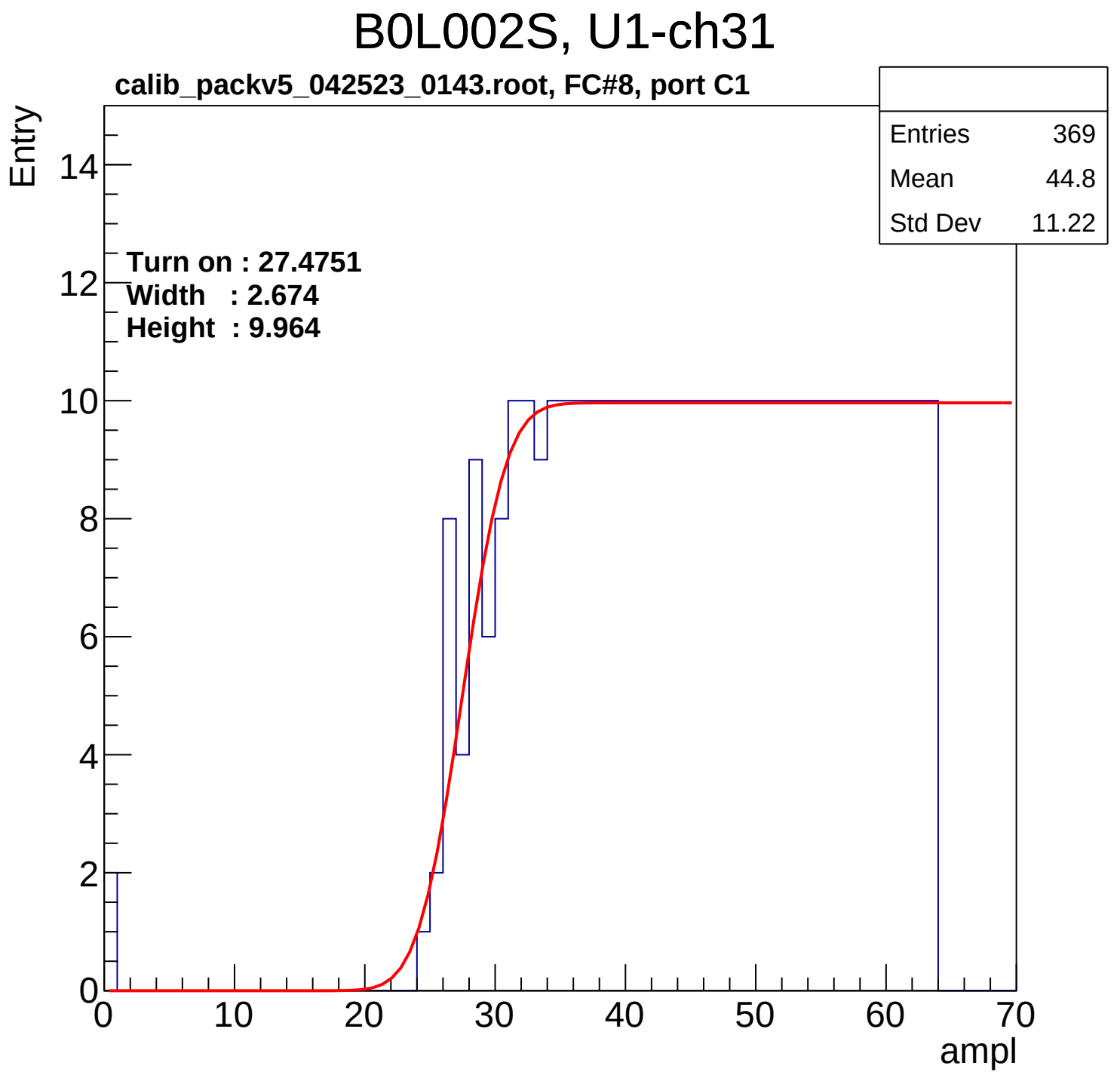
B0L002S, U1-ch31
calib_packv5_042523_0143.root, FC#8, port C1
Entries 369
Mean 44.8
Std Dev 11.22
Turn on : 27.4751
Width : 2.674
Height : 9.964
Entry
ampl
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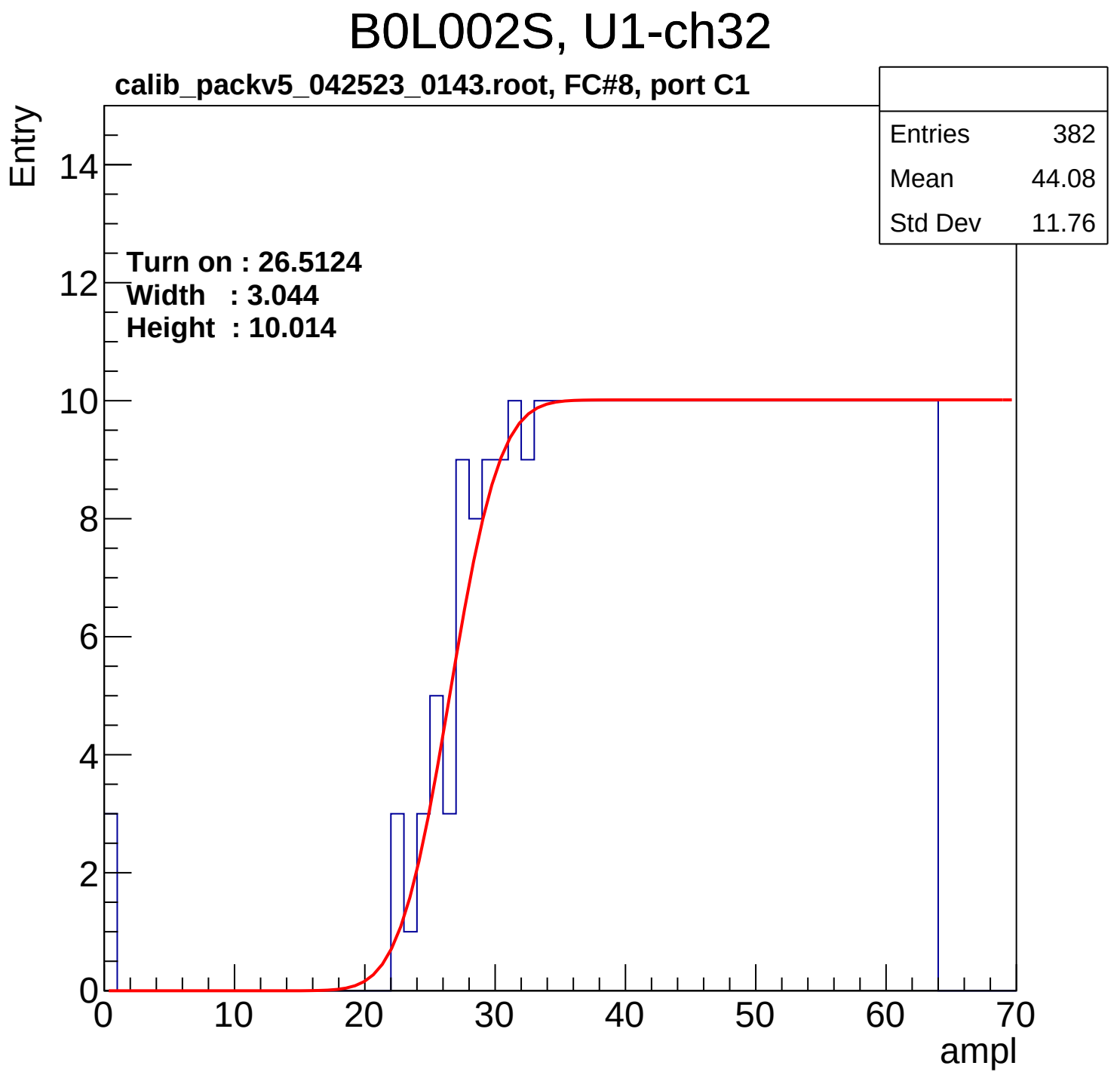
B0L002S, U1-ch32
calib_packv5_042523_0143.root, FC#8, port C1
Entries 382
Mean 44.08
Std Dev 11.76
Turn on : 26.5124
Width : 3.044
Height : 10.014
Entry
ampl
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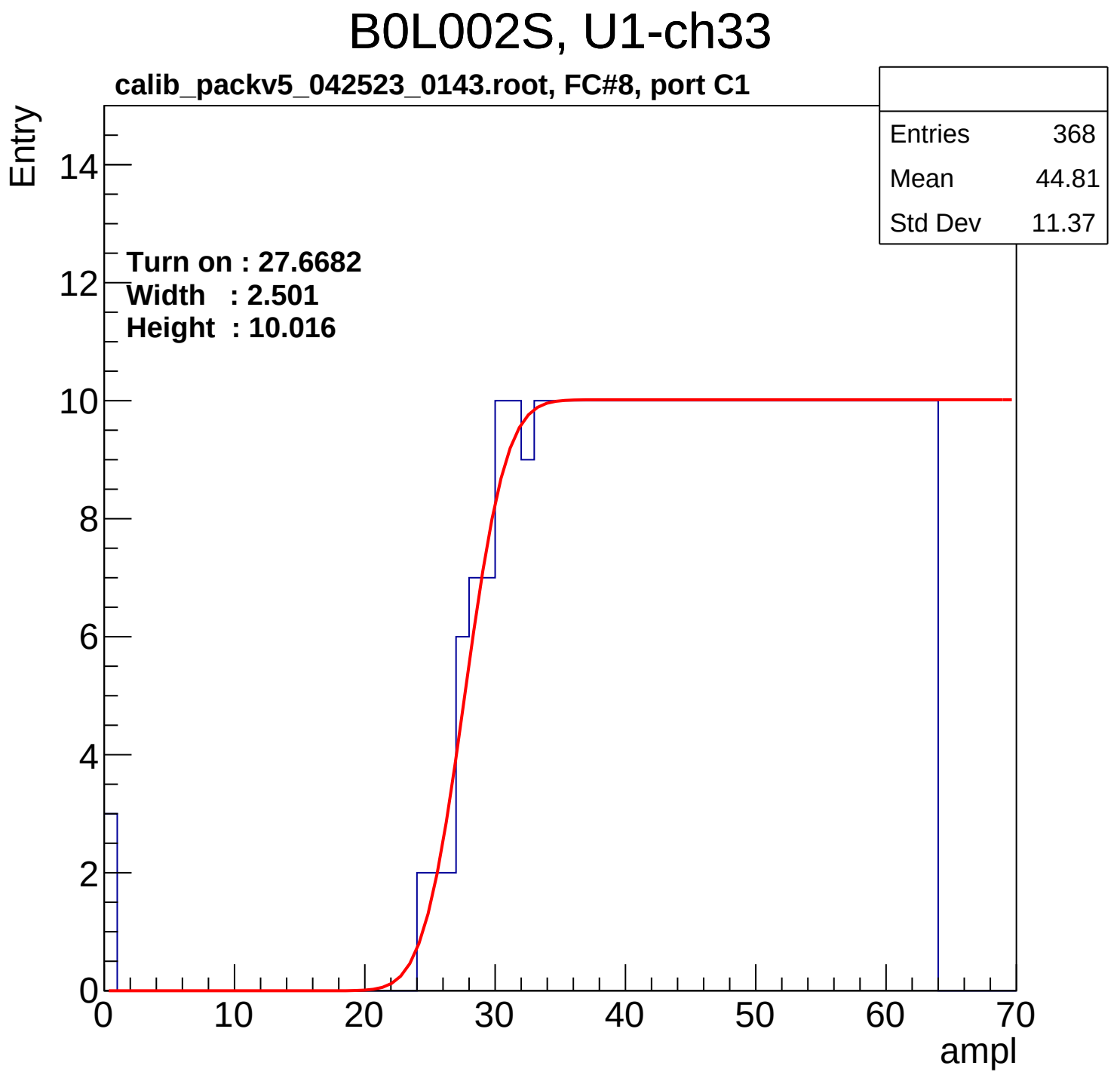
B0L002S, U1-ch33
calib_packv5_042523_0143.root, FC#8, port C1
Entries 368
Mean 44.81
Std Dev 11.37
Turn on : 27.6682
Width : 2.501
Height : 10.016
Entry
ampl
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2
4
6
8
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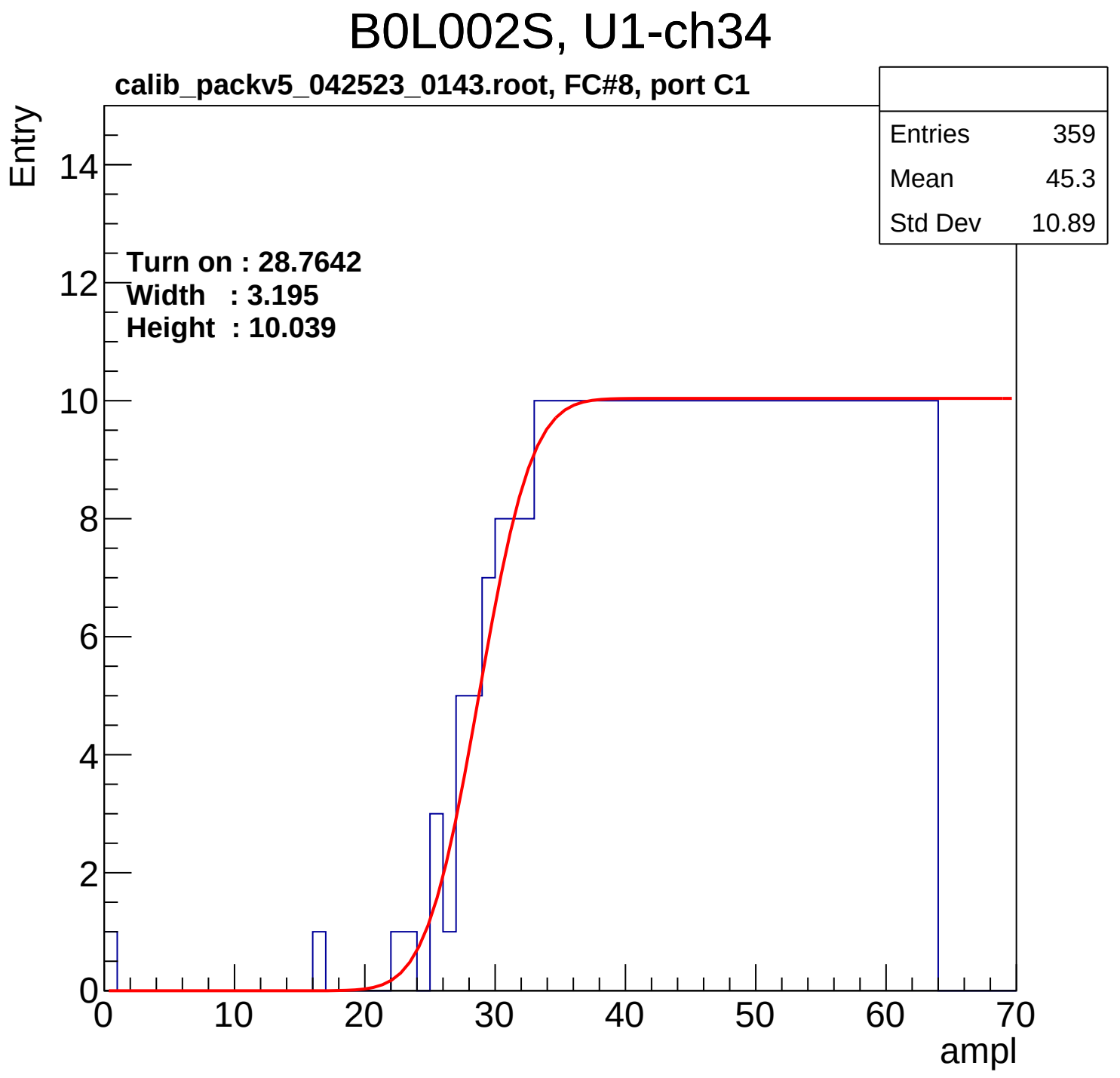
B0L002S, U1-ch34
calib_packv5_042523_0143.root, FC#8, port C1
Entries 359
Mean 45.3
Std Dev 10.89
Turn on : 28.7642
Width : 3.195
Height : 10.039
Entry
ampl
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6
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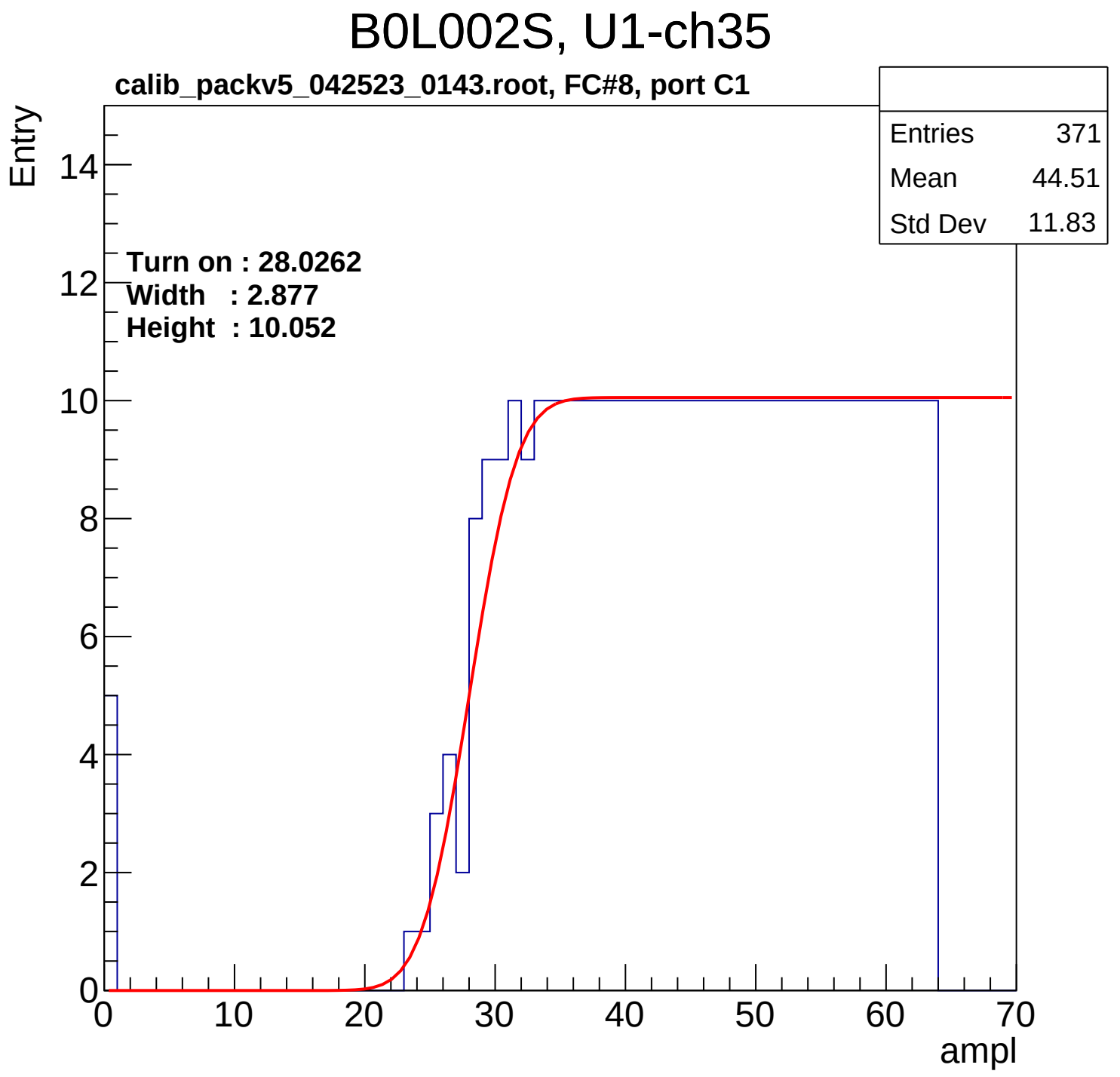
B0L002S, U1-ch35
calib_packv5_042523_0143.root, FC#8, port C1
Entries 371
Mean 44.51
Std Dev 11.83
Turn on : 28.0262
Width : 2.877
Height : 10.052
Entry
ampl
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2
4
6
8
10
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0
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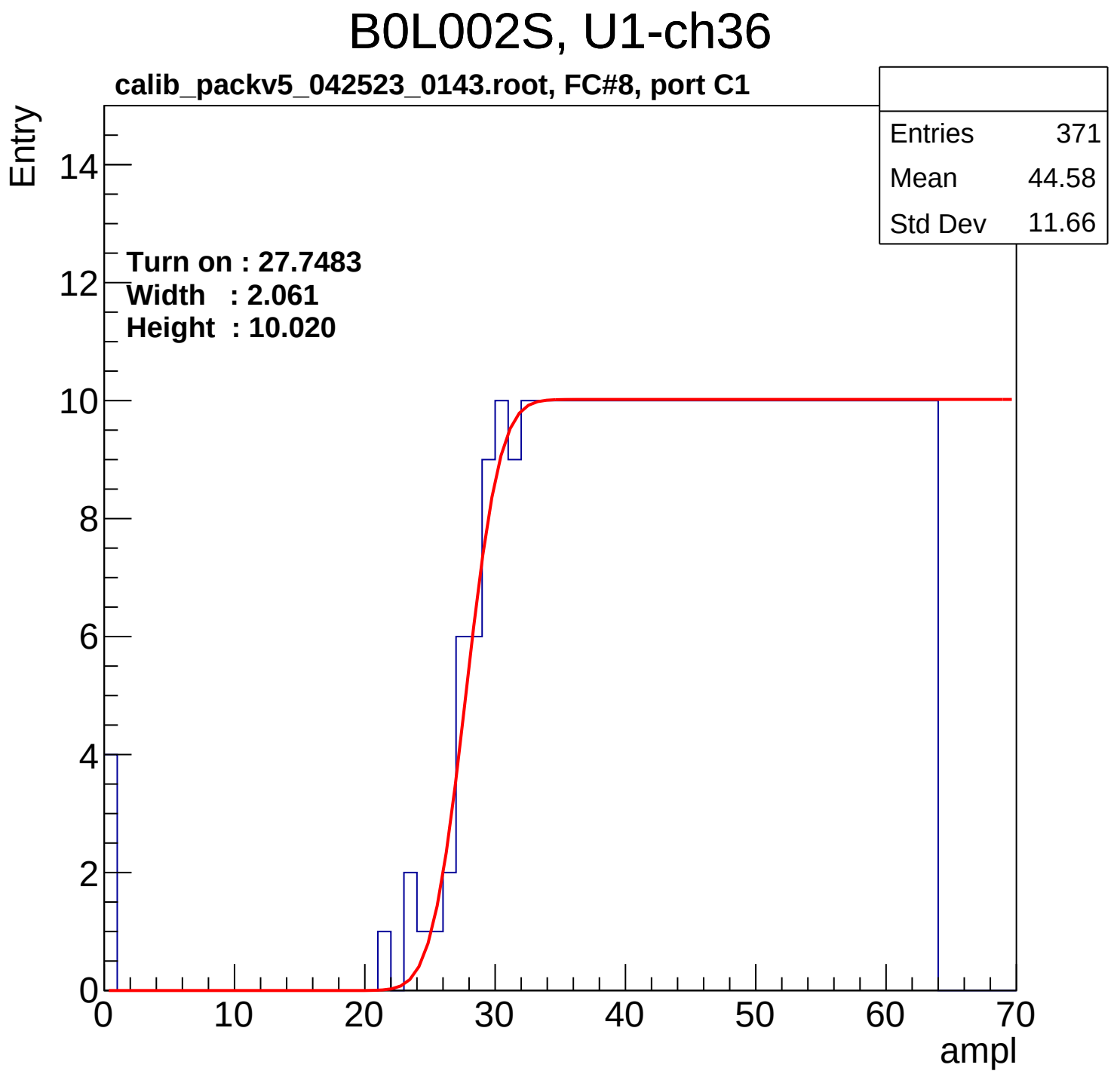
B0L002S, U1-ch36
calib_packv5_042523_0143.root, FC#8, port C1
Entries 371
Mean 44.58
Std Dev 11.66
Turn on : 27.7483
Width : 2.061
Height : 10.020
Entry
ampl
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2
4
6
8
10
12
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0
10
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60
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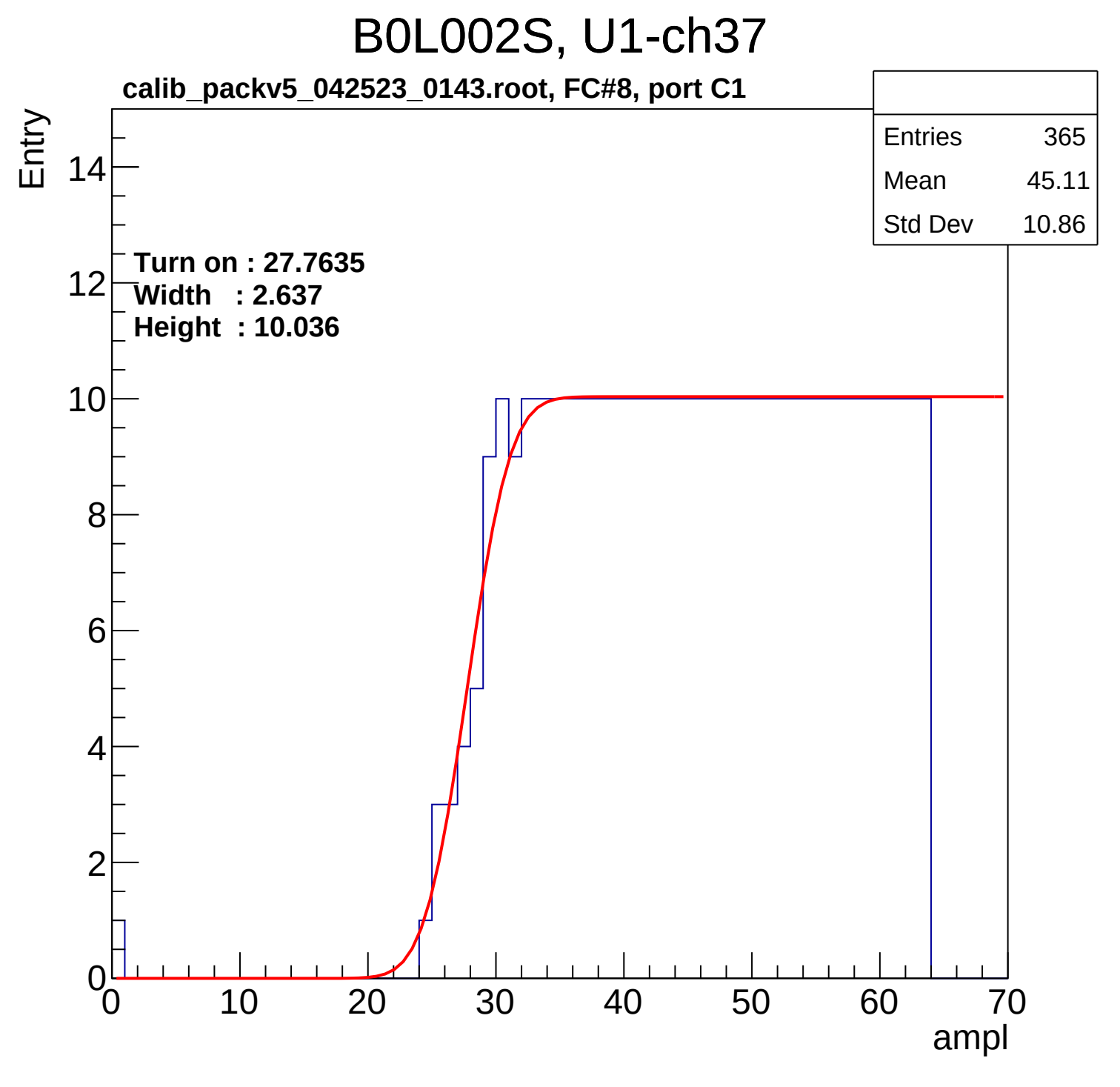
B0L002S, U1-ch37
calib_packv5_042523_0143.root, FC#8, port C1
Entries 365
Mean 45.11
Std Dev 10.86
Turn on : 27.7635
Width : 2.637
Height : 10.036
Entry
ampl
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2
4
6
8
10
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60
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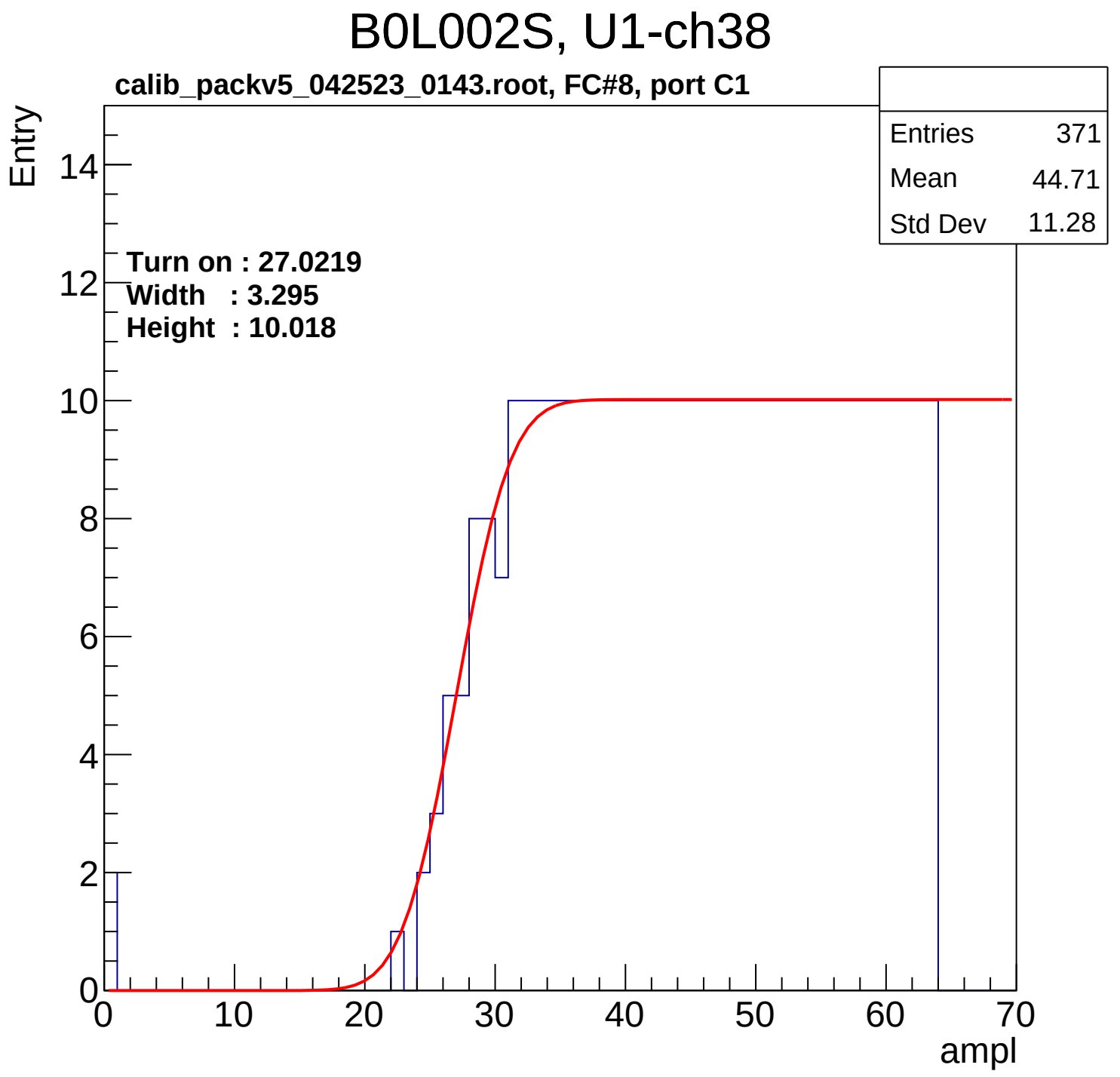
B0L002S, U1-ch38
calib_packv5_042523_0143.root, FC#8, port C1
Entries 371
Mean 44.71
Std Dev 11.28
Turn on : 27.0219
Width : 3.295
Height : 10.018
Entry
ampl
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2
4
6
8
10
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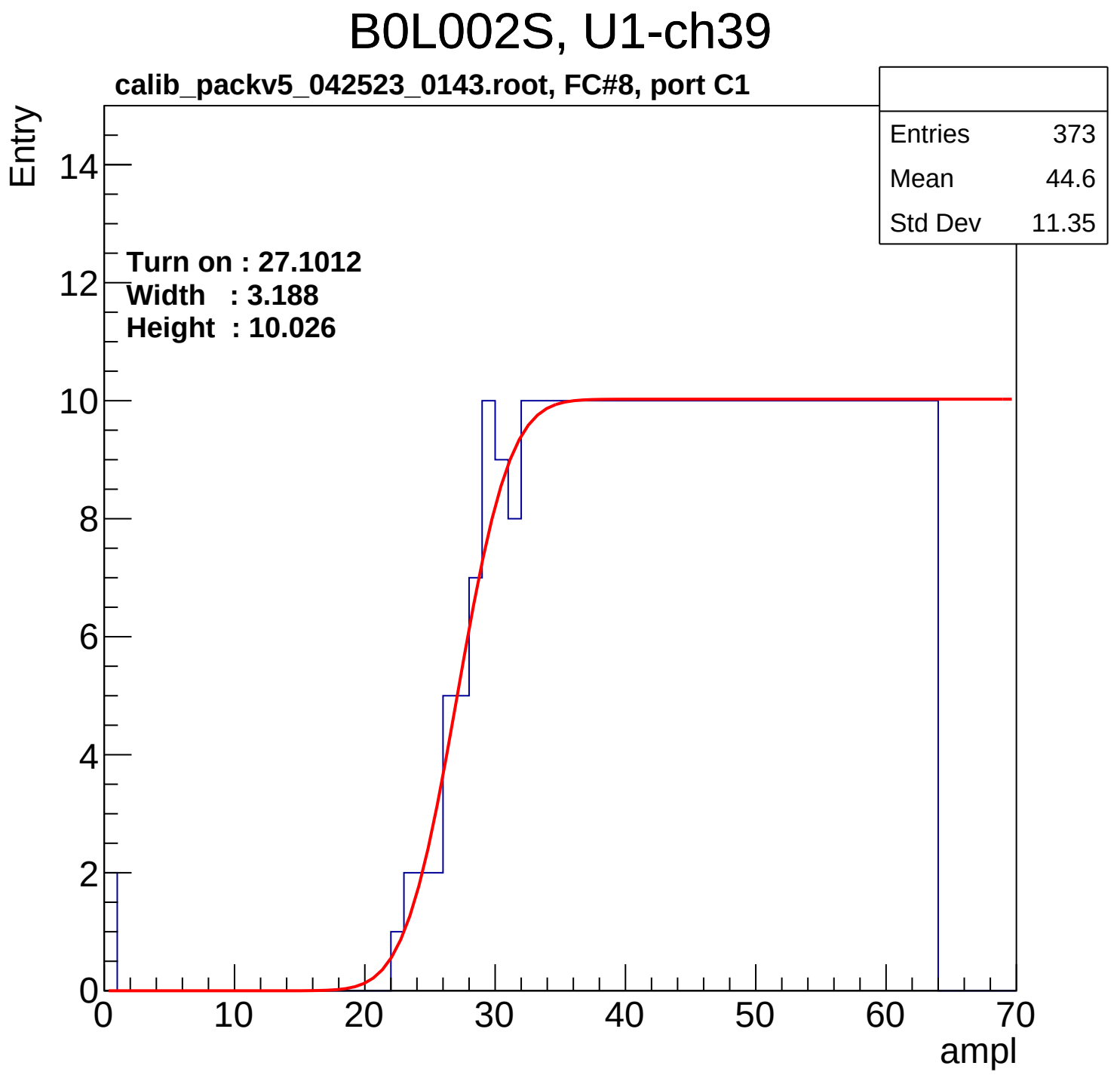
B0L002S, U1-ch39
calib_packv5_042523_0143.root, FC#8, port C1
Entries 373
Mean 44.6
Std Dev 11.35
Turn on : 27.1012
Width : 3.188
Height : 10.026
Entry
ampl
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2
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6
8
10
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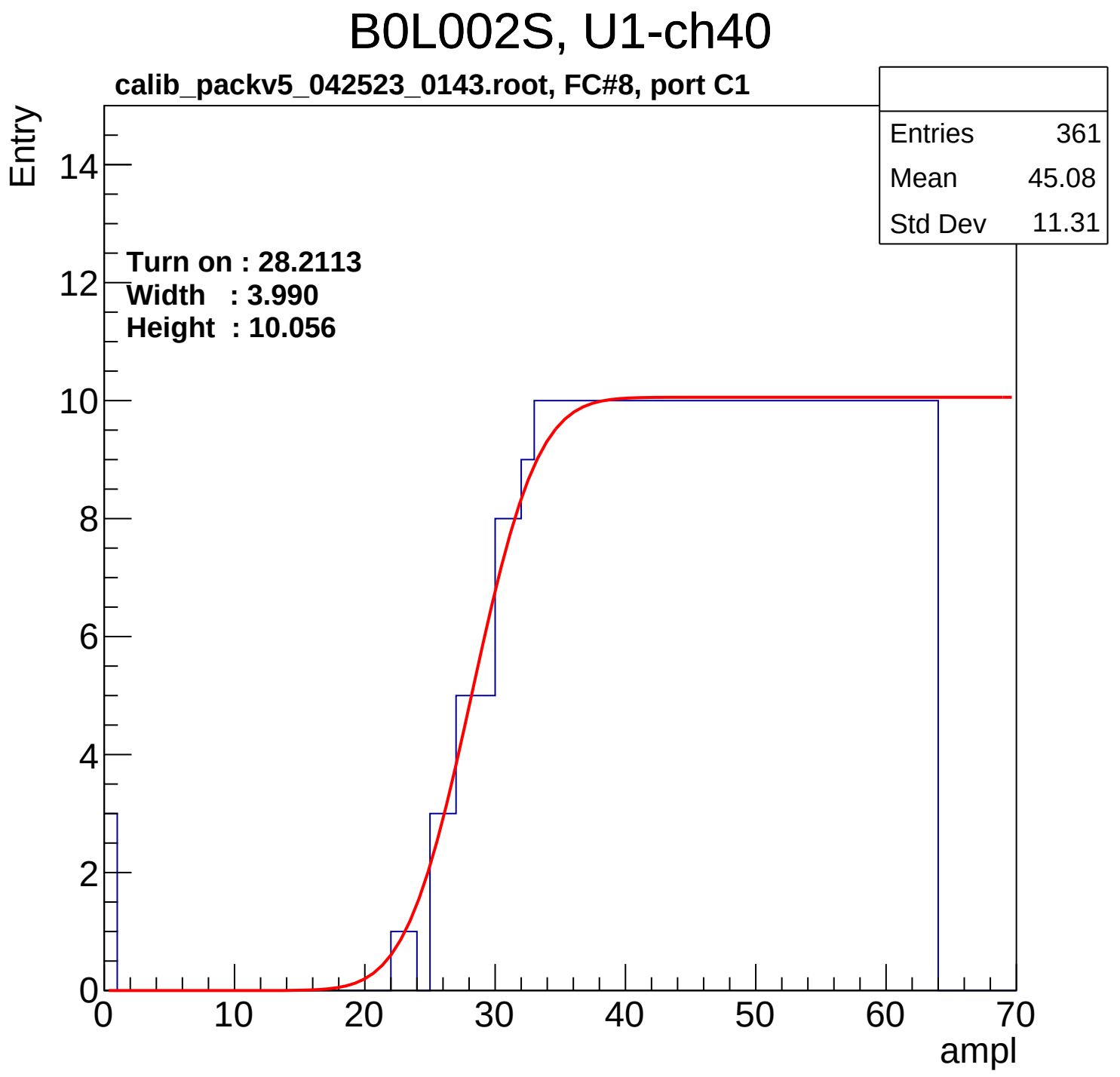
B0L002S, U1-ch40
calib_packv5_042523_0143.root, FC#8, port C1
Entries 361
Mean 45.08
Std Dev 11.31
Turn on : 28.2113
Width : 3.990
Height : 10.056
Entry
ampl
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6
8
10
12
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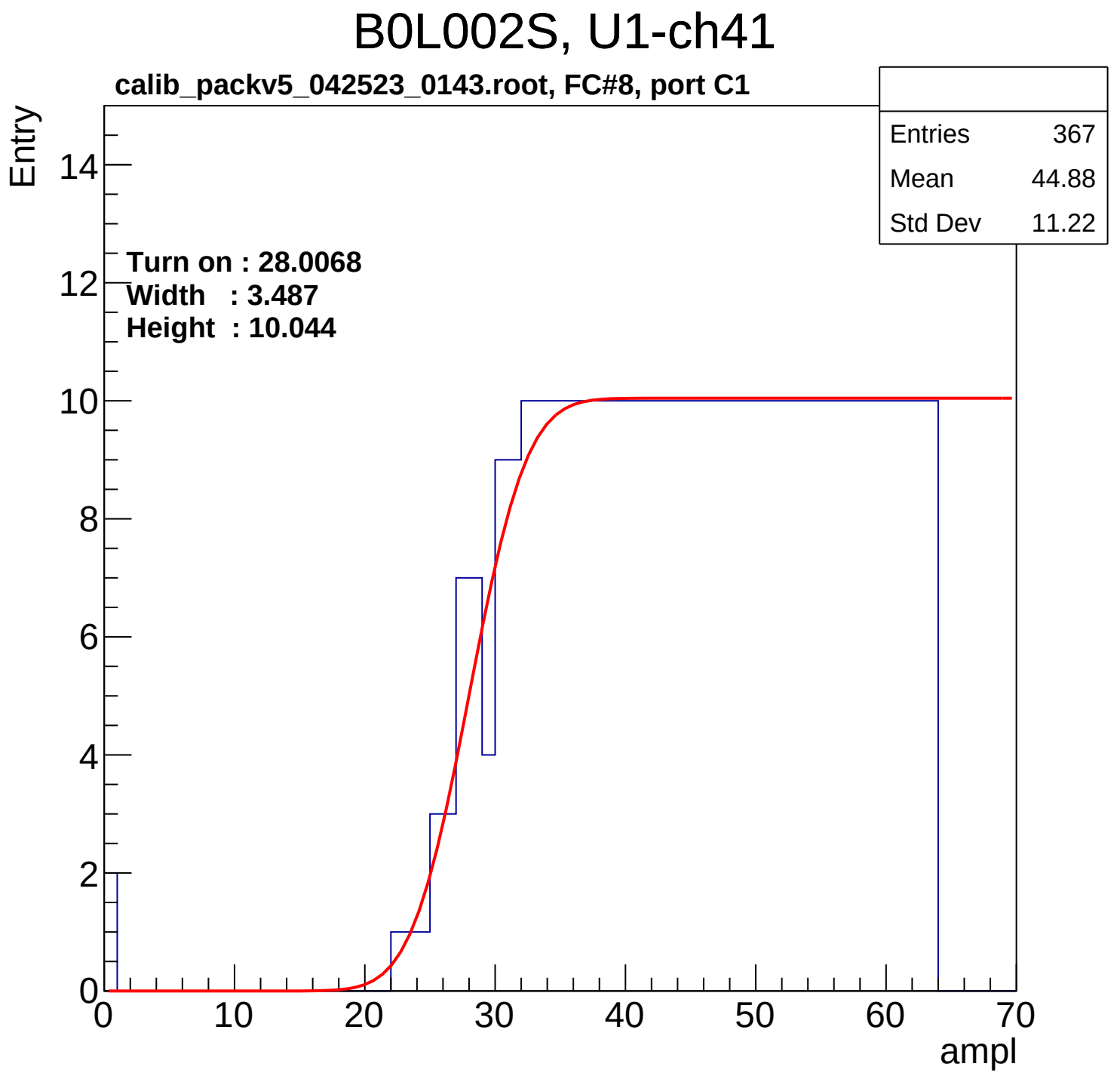
B0L002S, U1-ch41
calib_packv5_042523_0143.root, FC#8, port C1
Entries 367
Mean 44.88
Std Dev 11.22
Turn on : 28.0068
Width : 3.487
Height : 10.044
Entry
ampl
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2
4
6
8
10
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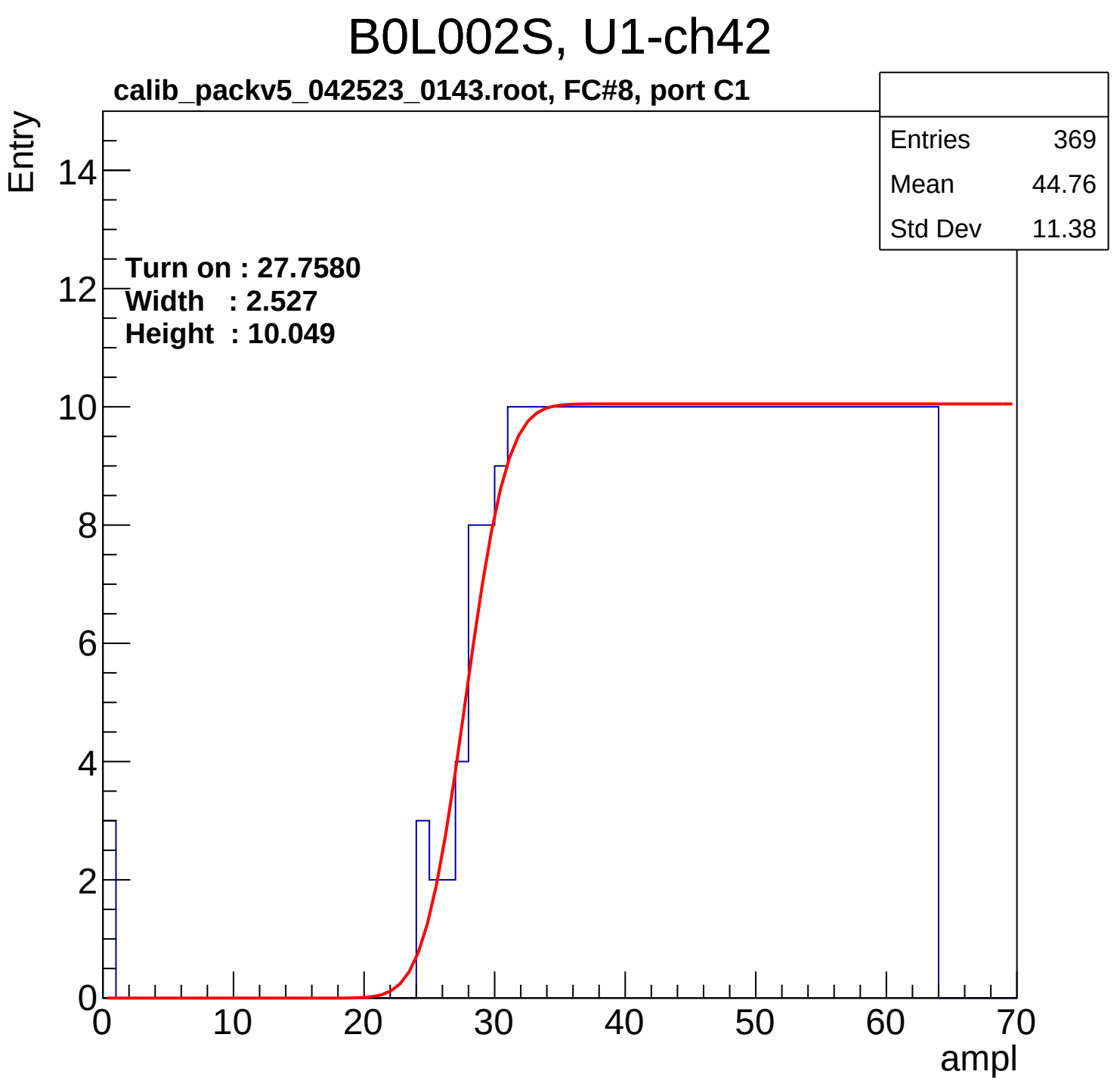
B0L002S, U1-ch42
calib_packv5_042523_0143.root, FC#8, port C1
Entries 369
Mean 44.76
Std Dev 11.38
Turn on : 27.7580
Width : 2.527
Height : 10.049
Entry
ampl
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6
8
10
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60
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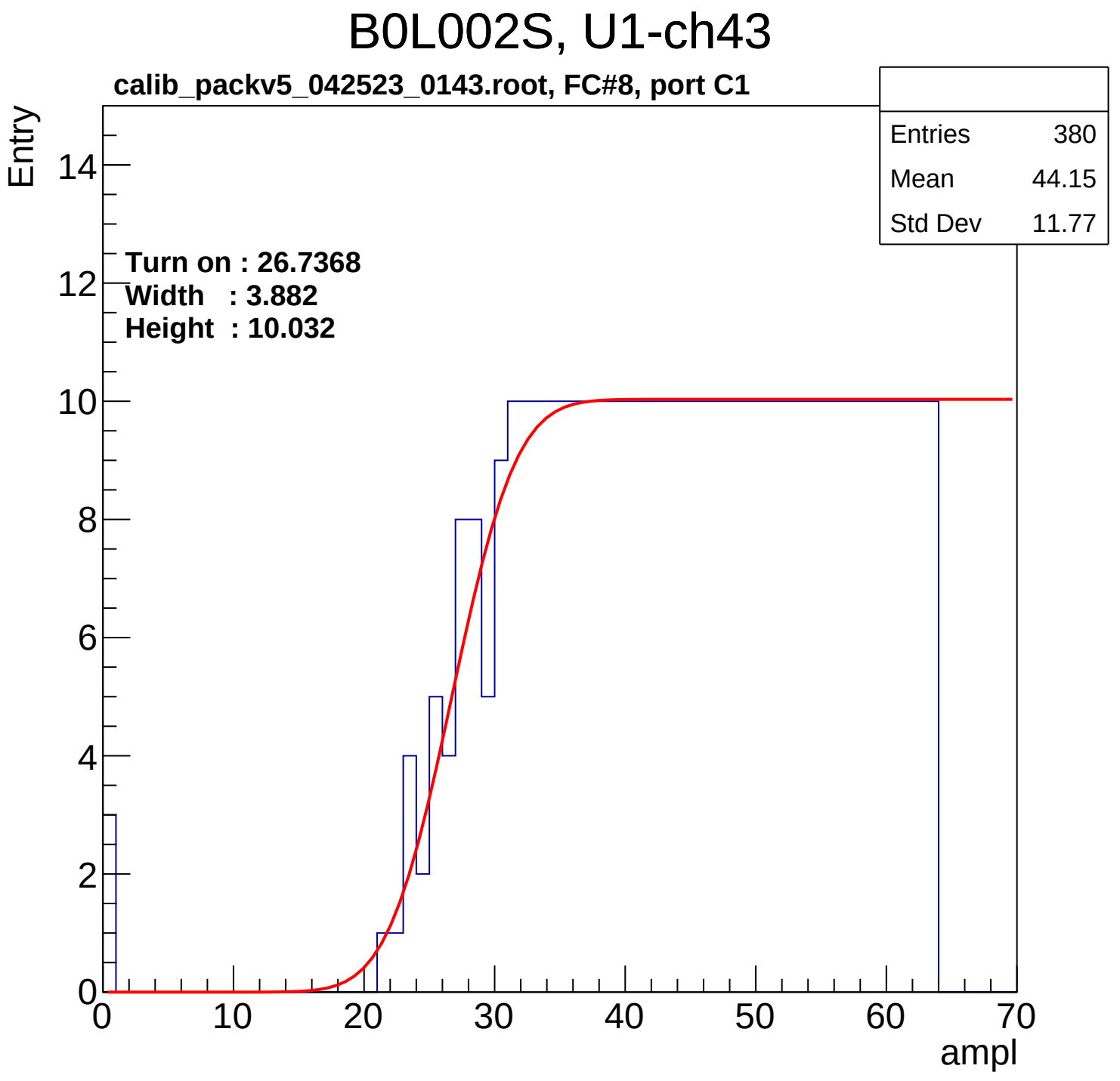
B0L002S, U1-ch43
calib_packv5_042523_0143.root, FC#8, port C1
Entries 380
Mean 44.15
Std Dev 11.77
Turn on : 26.7368
Width : 3.882
Height : 10.032
Entry
ampl
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6
8
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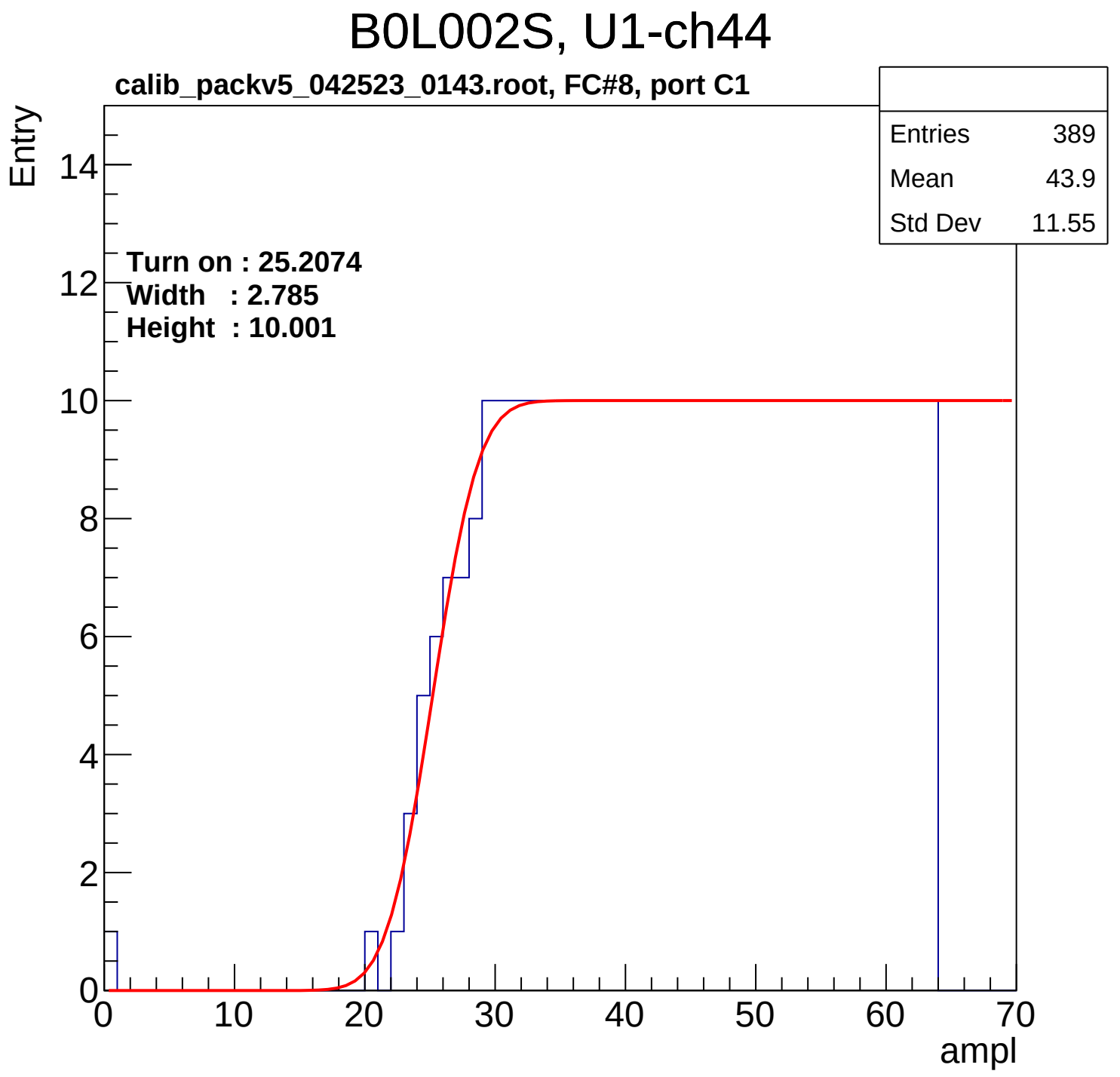
B0L002S, U1-ch44
calib_packv5_042523_0143.root, FC#8, port C1
Entries 389
Mean 43.9
Std Dev 11.55
Turn on : 25.2074
Width : 2.785
Height : 10.001
Entry
ampl
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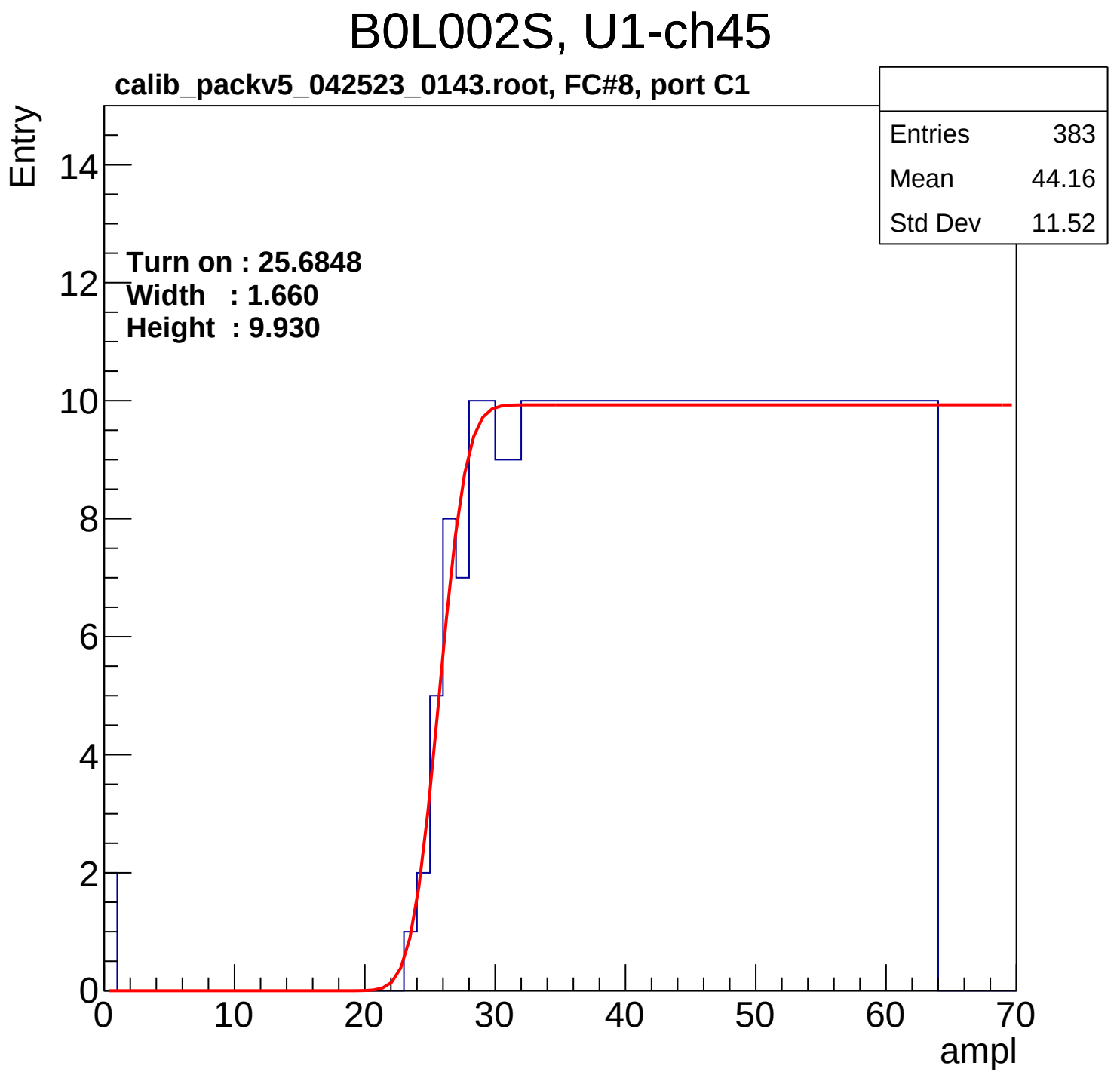
B0L002S, U1-ch45
calib_packv5_042523_0143.root, FC#8, port C1
Entries 383
Mean 44.16
Std Dev 11.52
Turn on : 25.6848
Width : 1.660
Height : 9.930
Entry
ampl
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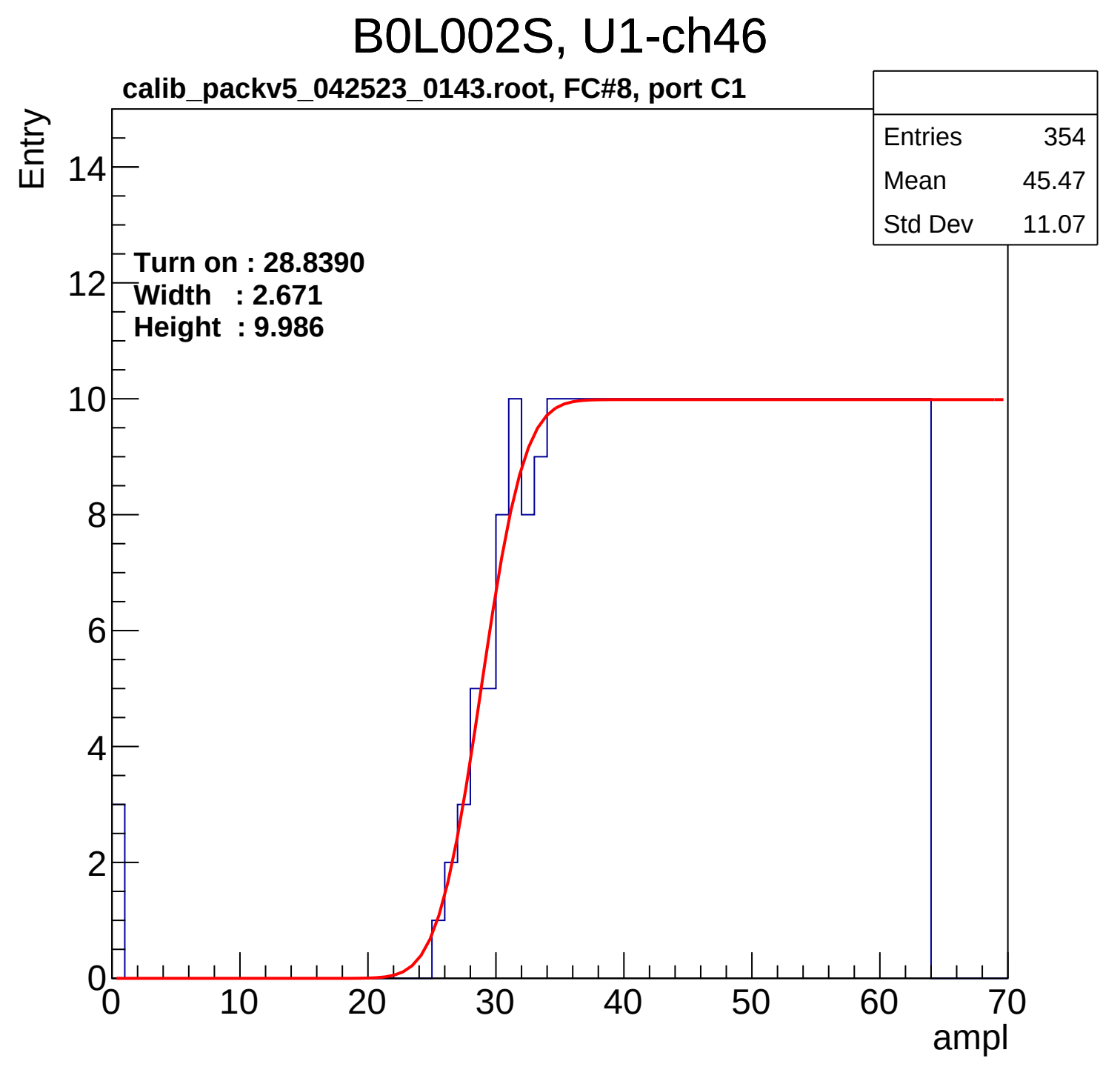
B0L002S, U1-ch46
calib_packv5_042523_0143.root, FC#8, port C1
Entries 354
Mean 45.47
Std Dev 11.07
Turn on : 28.8390
Width : 2.671
Height : 9.986
Entry
ampl
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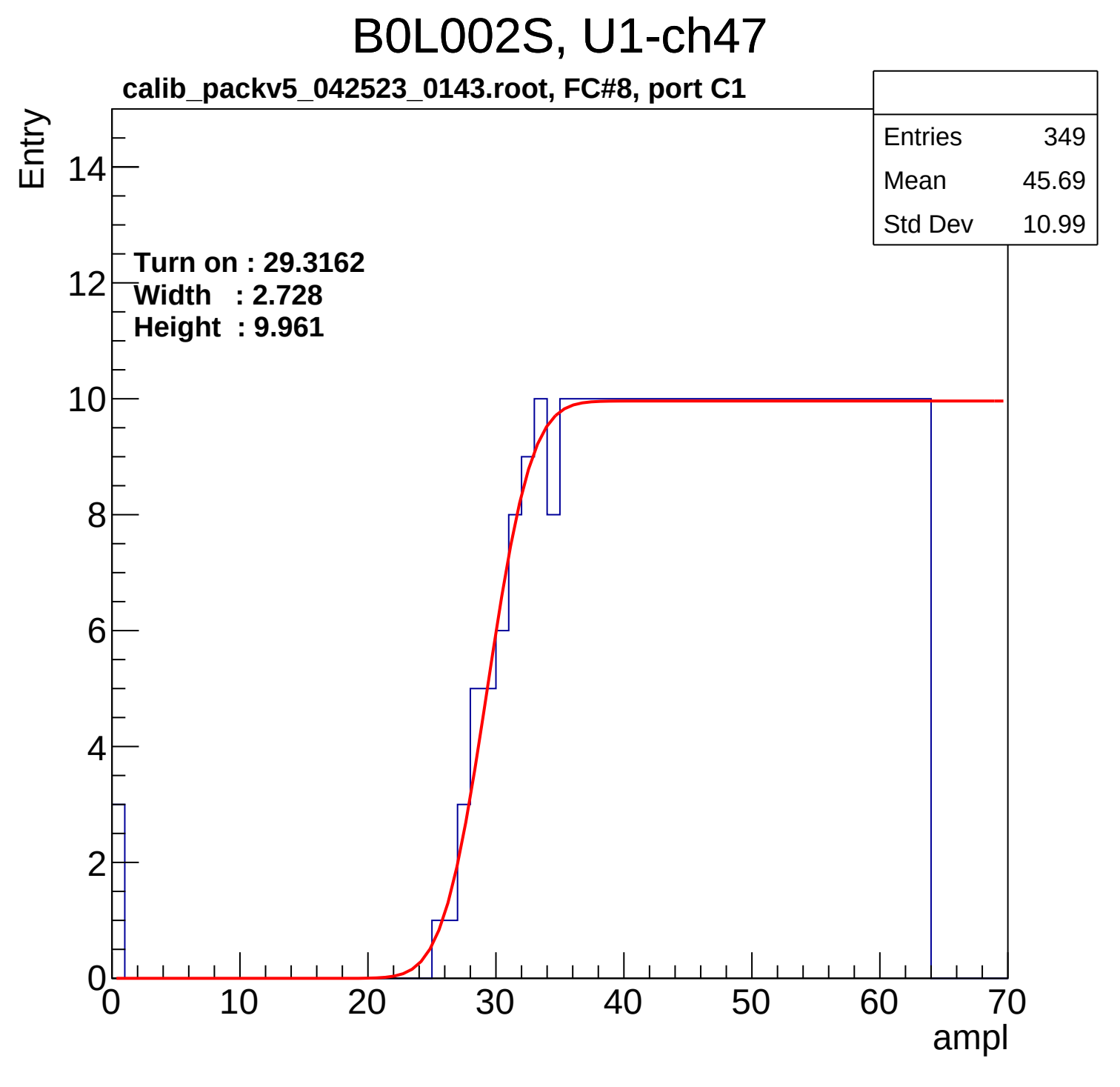
B0L002S, U1-ch47
calib_packv5_042523_0143.root, FC#8, port C1
Entries 349
Mean 45.69
Std Dev 10.99
Turn on : 29.3162
Width : 2.728
Height : 9.961
Entry
ampl
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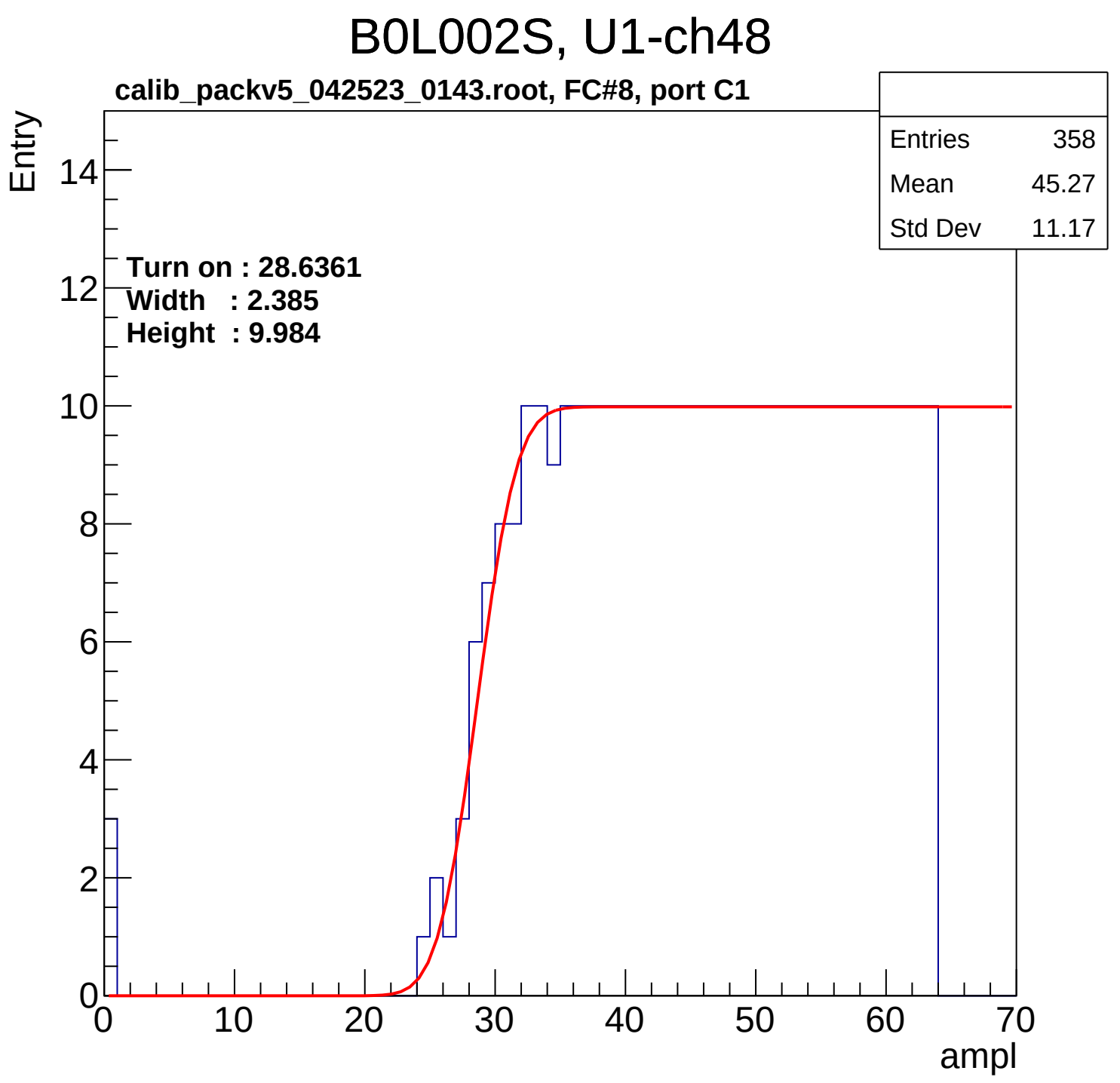
B0L002S, U1-ch48
calib_packv5_042523_0143.root, FC#8, port C1
Entries 358
Mean 45.27
Std Dev 11.17
Turn on : 28.6361
Width : 2.385
Height : 9.984
Entry
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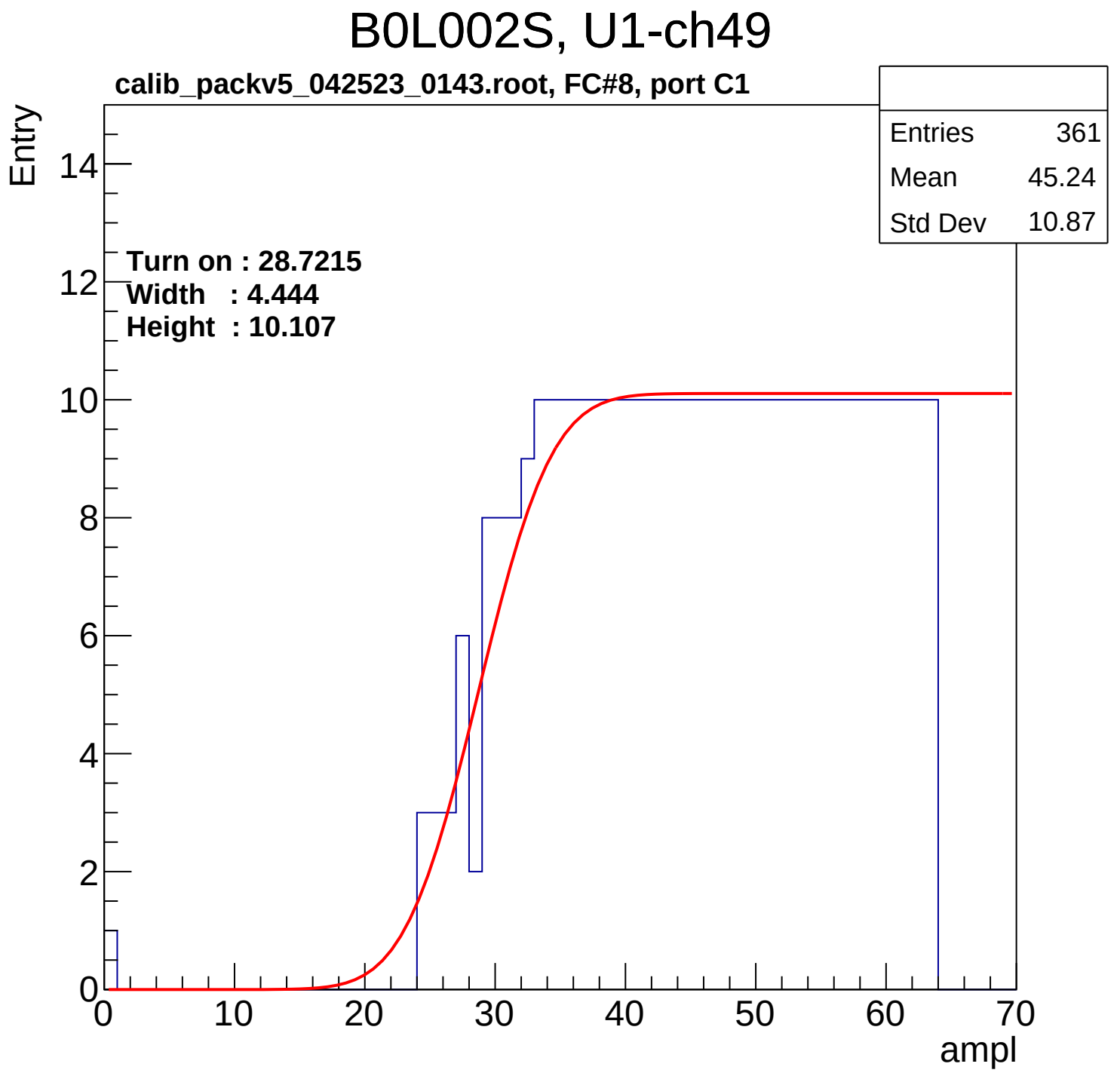
B0L002S, U1-ch49
calib_packv5_042523_0143.root, FC#8, port C1
Entries 361
Mean 45.24
Std Dev 10.87
Turn on : 28.7215
Width : 4.444
Height : 10.107
Entry
ampl
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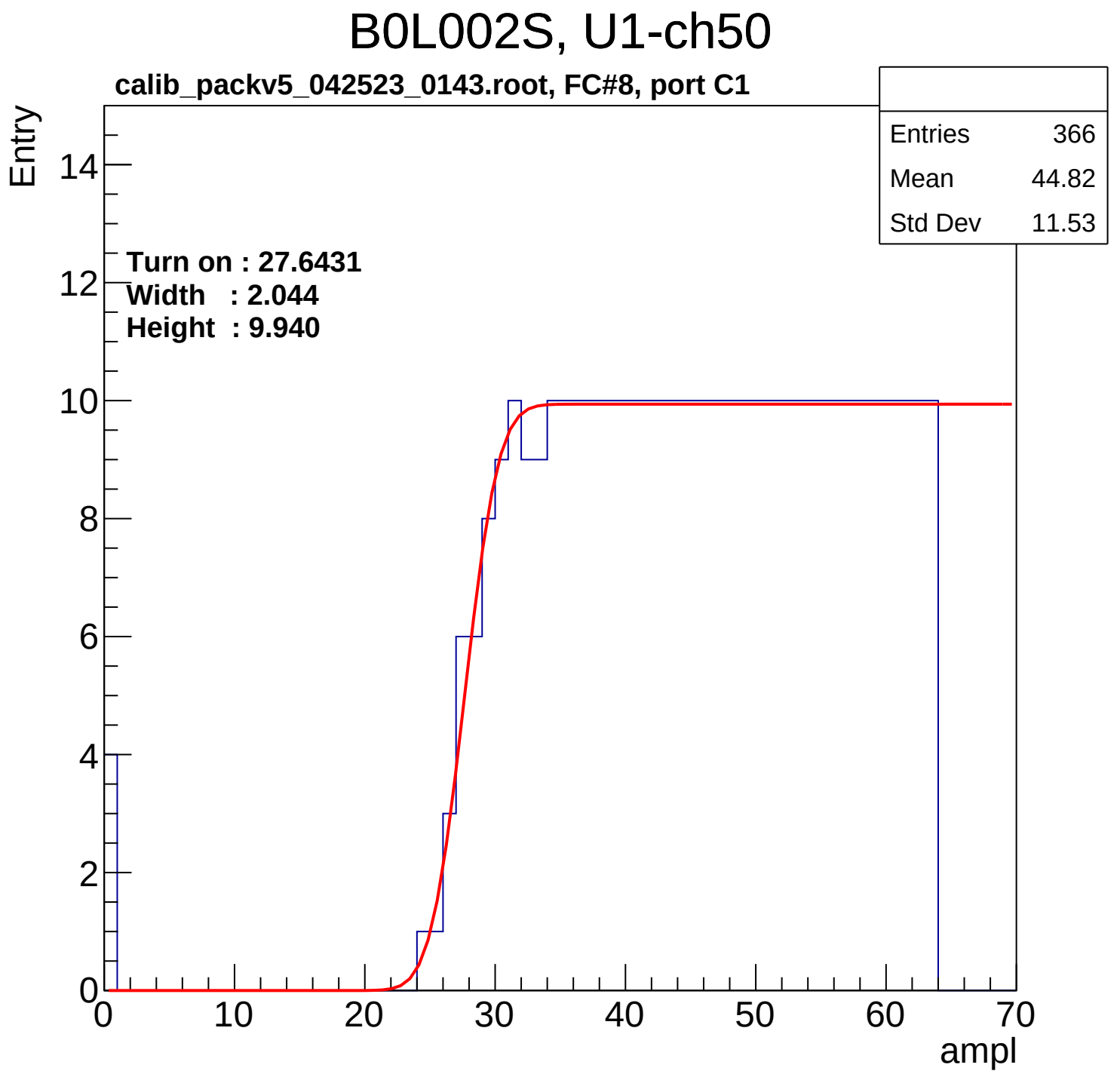
B0L002S, U1-ch50
calib_packv5_042523_0143.root, FC#8, port C1
Entries 366
Mean 44.82
Std Dev 11.53
Turn on : 27.6431
Width : 2.044
Height : 9.940
Entry
ampl
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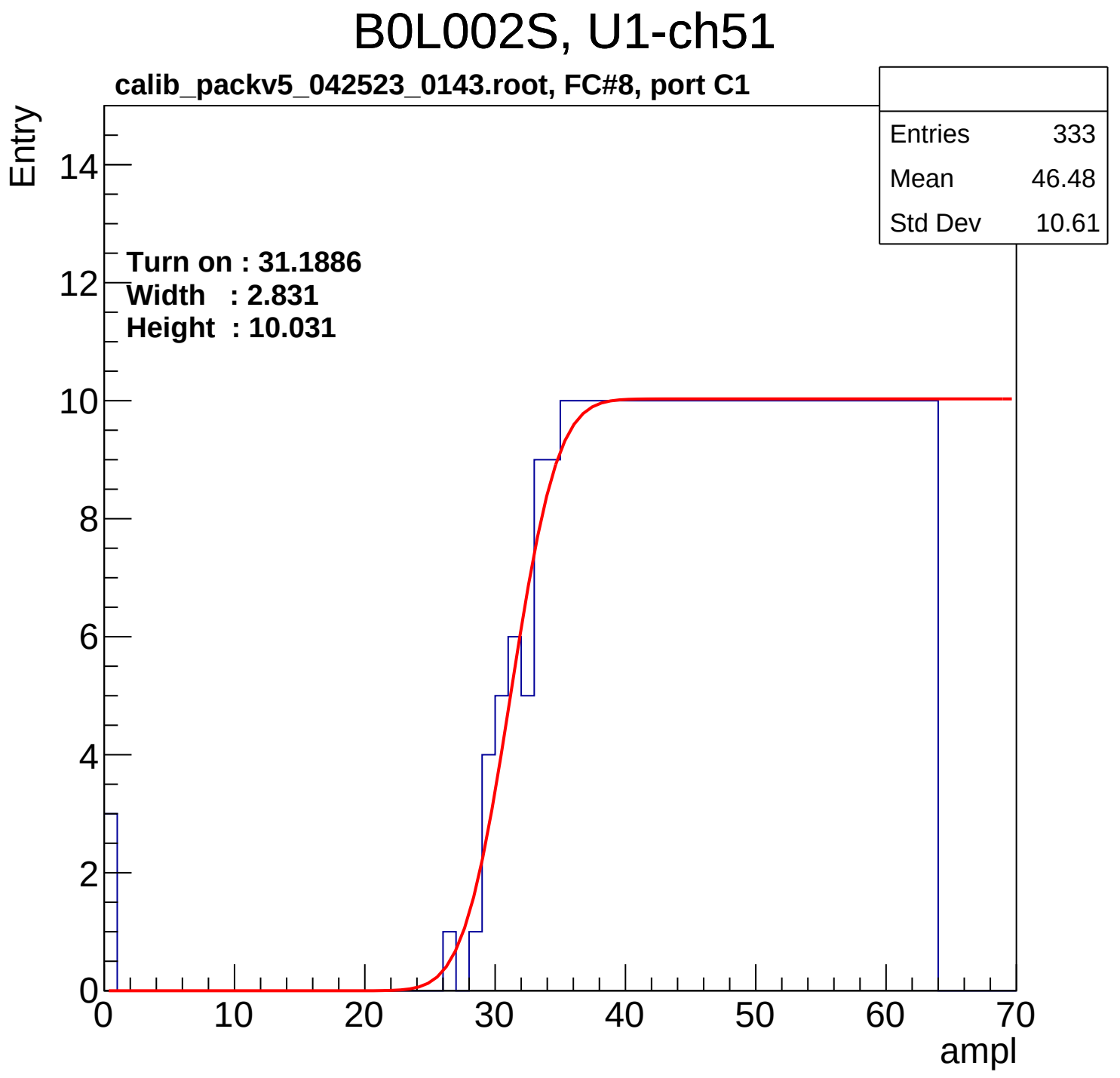
B0L002S, U1-ch51
calib_packv5_042523_0143.root, FC#8, port C1
Entries 333
Mean 46.48
Std Dev 10.61
Turn on : 31.1886
Width : 2.831
Height : 10.031
Entry
ampl
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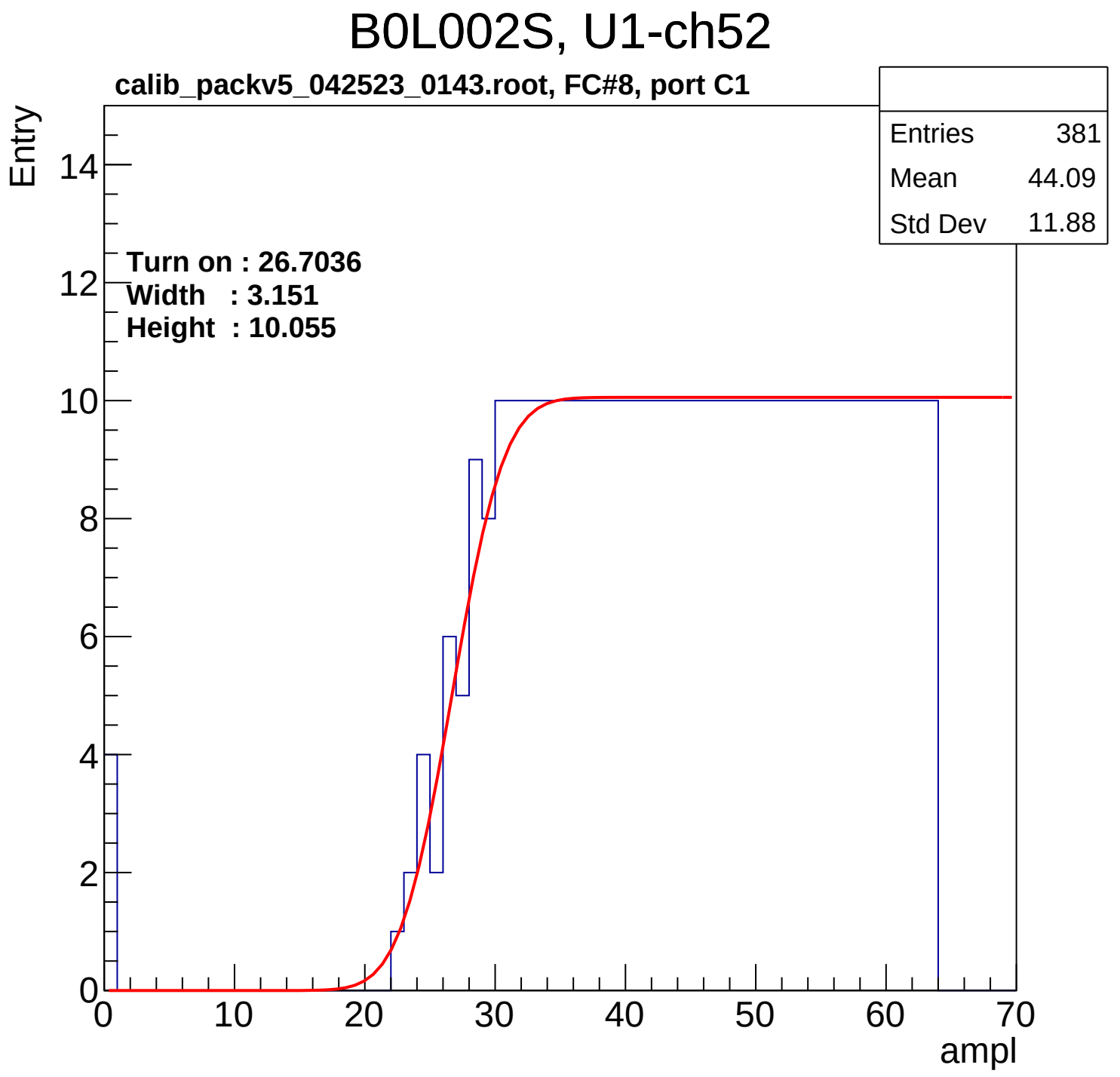
B0L002S, U1-ch52
calib_packv5_042523_0143.root, FC#8, port C1
Entries 381
Mean 44.09
Std Dev 11.88
Turn on : 26.7036
Width : 3.151
Height : 10.055
Entry
ampl
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4
6
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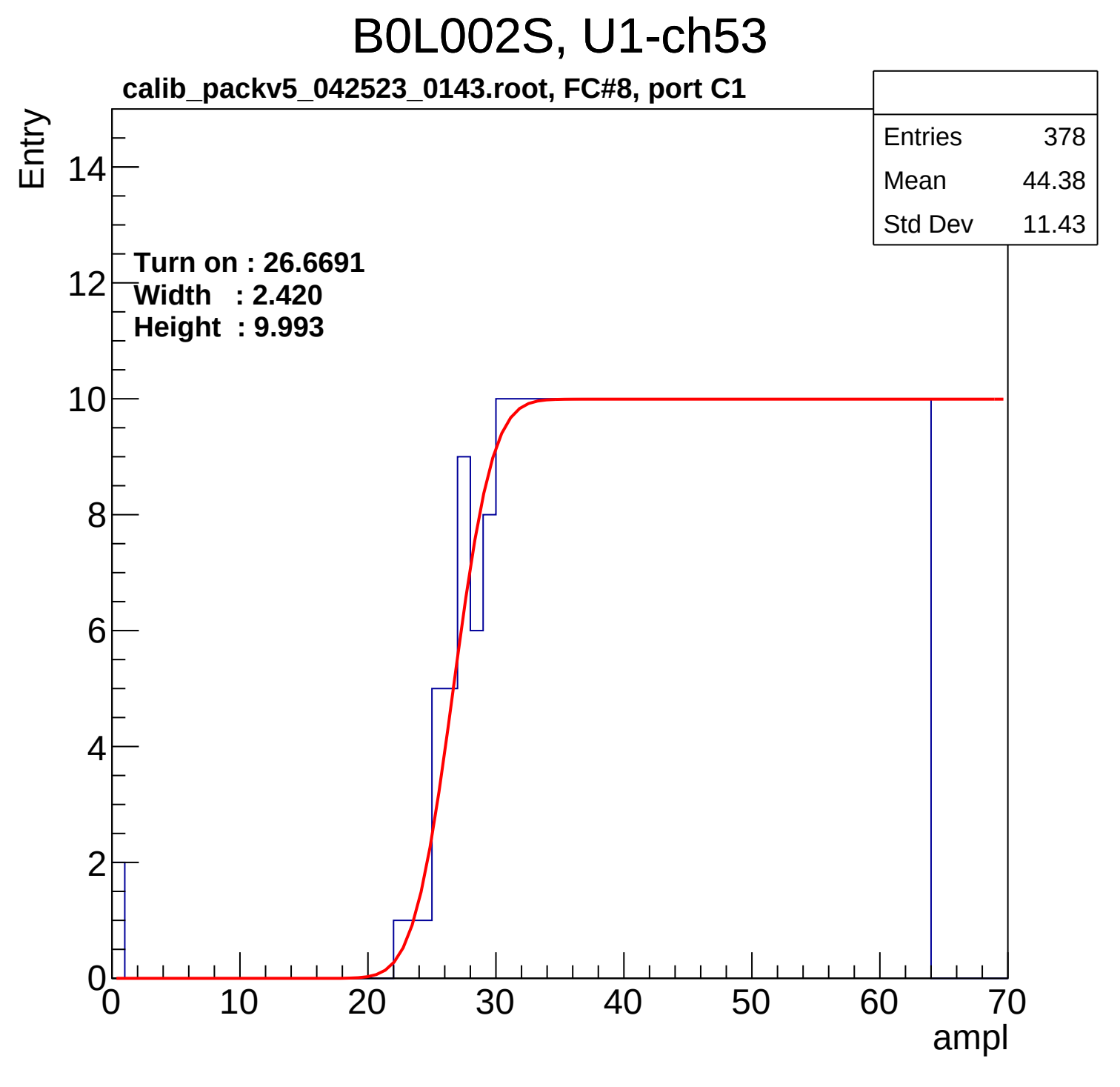
B0L002S, U1-ch53
calib_packv5_042523_0143.root, FC#8, port C1
Entries 378
Mean 44.38
Std Dev 11.43
Turn on : 26.6691
Width : 2.420
Height : 9.993
Entry
ampl
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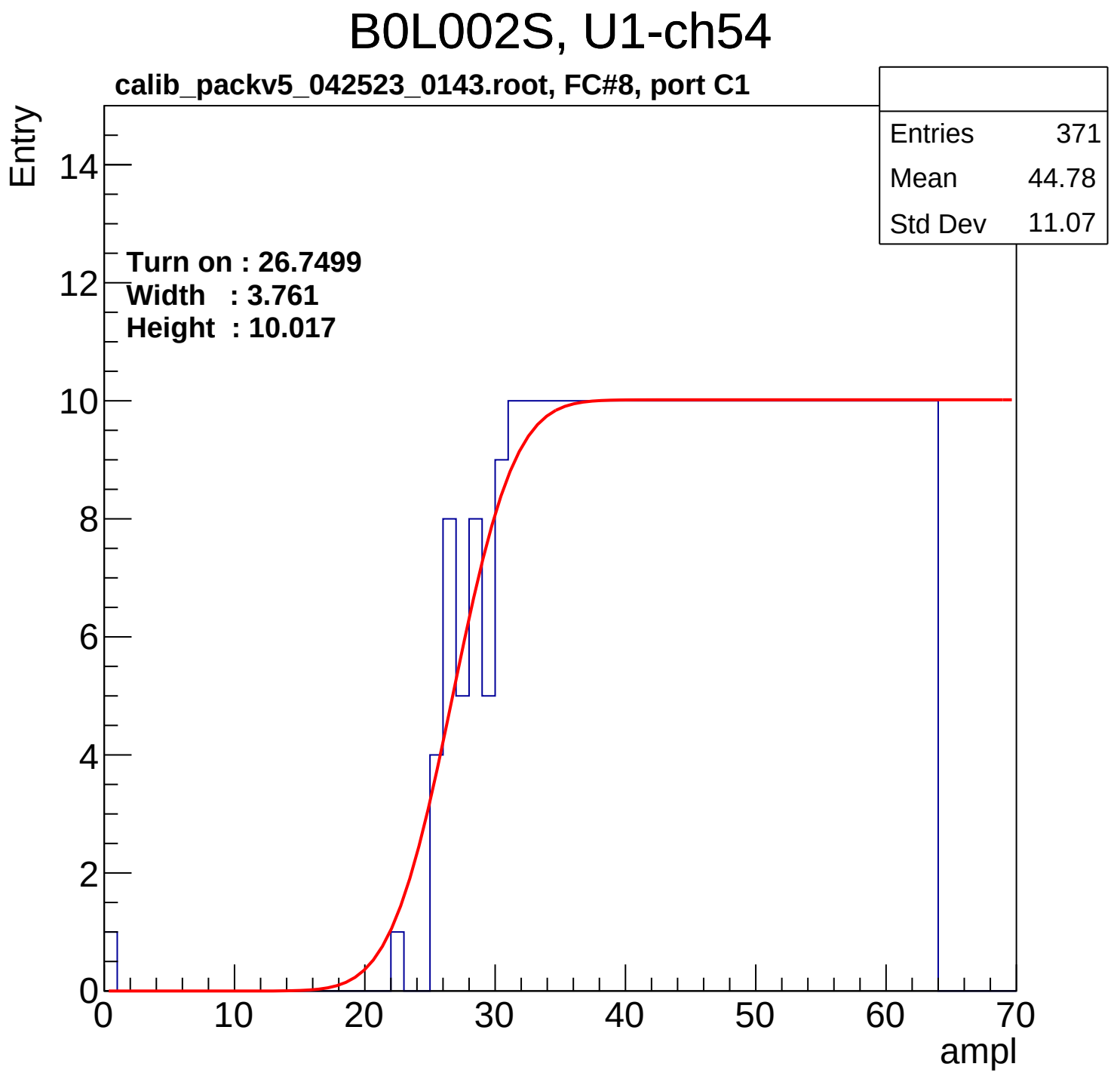
B0L002S, U1-ch54
calib_packv5_042523_0143.root, FC#8, port C1
Entries 371
Mean 44.78
Std Dev 11.07
Turn on : 26.7499
Width : 3.761
Height : 10.017
Entry
ampl
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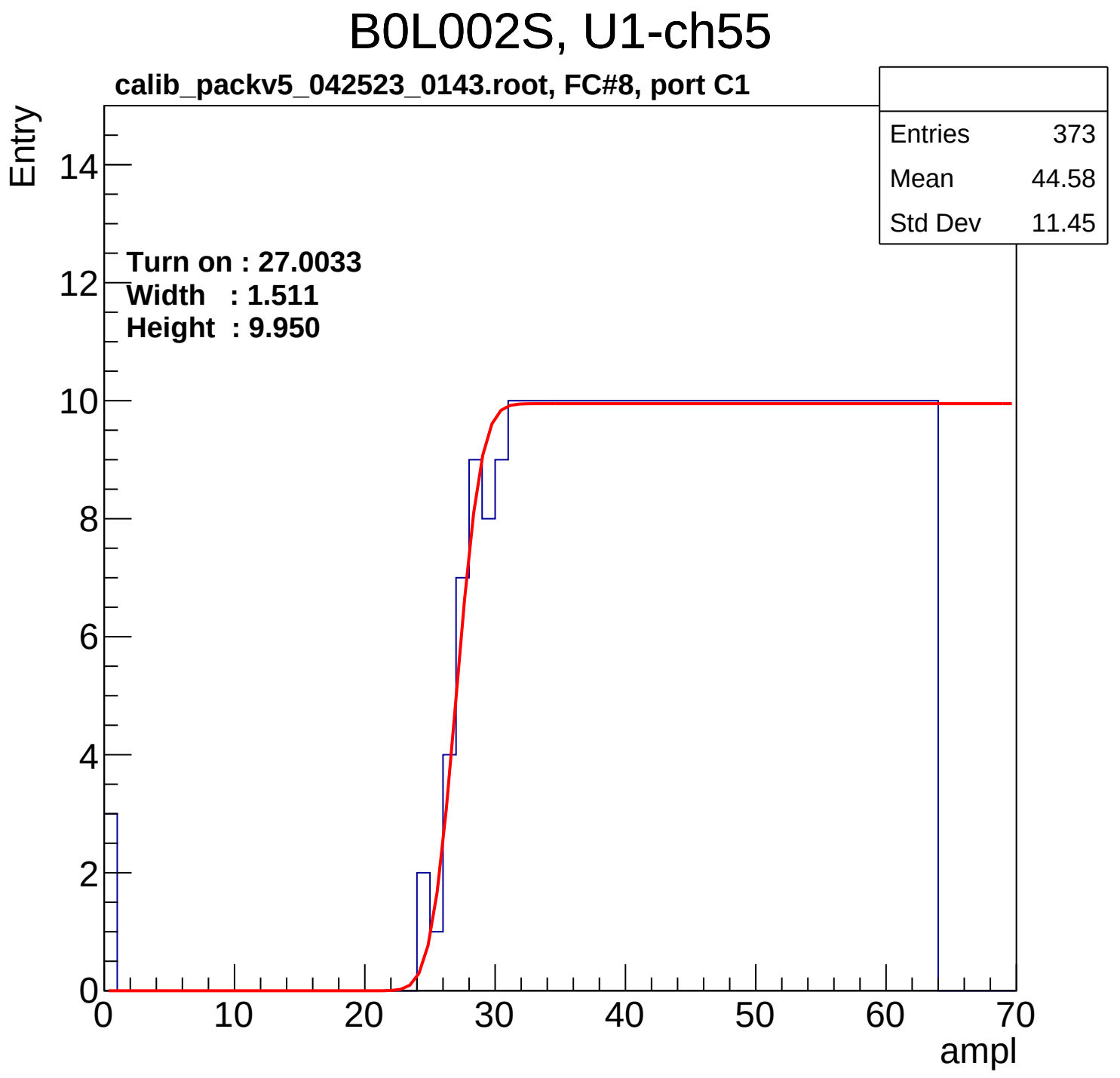
B0L002S, U1-ch55
calib_packv5_042523_0143.root, FC#8, port C1
Entries 373
Mean 44.58
Std Dev 11.45
Turn on : 27.0033
Width : 1.511
Height : 9.950
Entry
ampl
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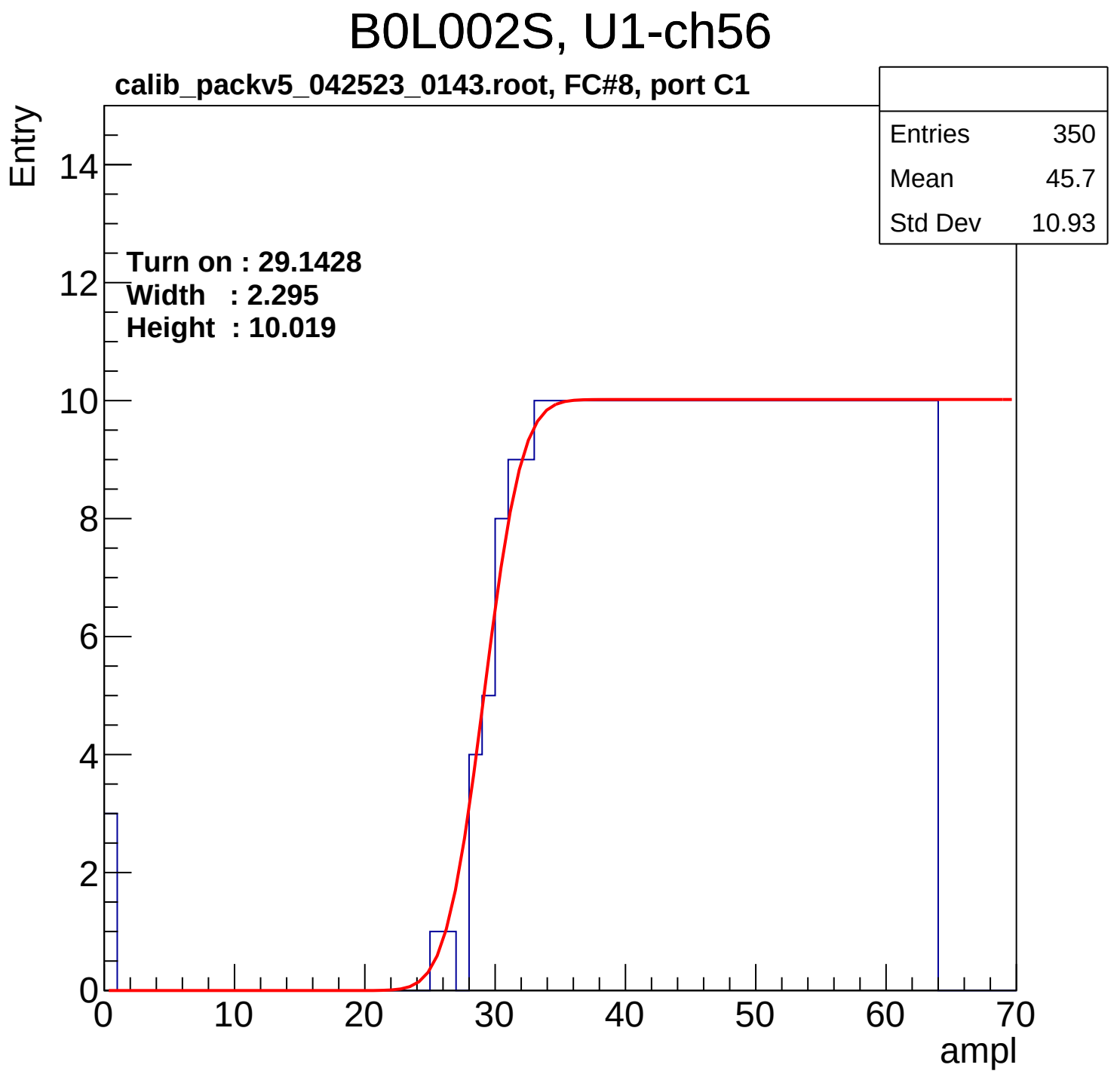
B0L002S, U1-ch56
calib_packv5_042523_0143.root, FC#8, port C1
Entries 350
Mean 45.7
Std Dev 10.93
Turn on : 29.1428
Width : 2.295
Height : 10.019
Entry
ampl
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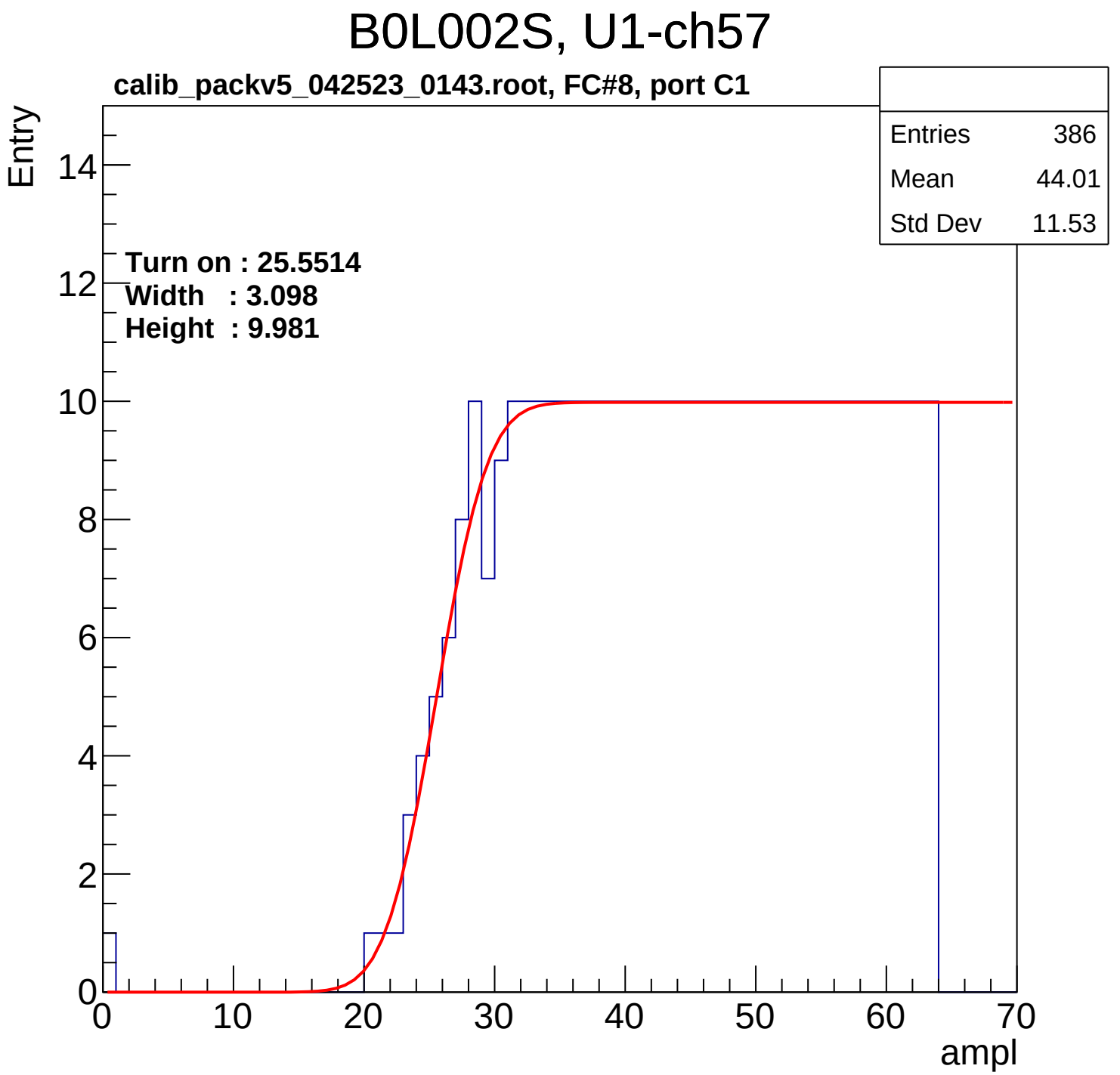
B0L002S, U1-ch57
calib_packv5_042523_0143.root, FC#8, port C1
Entries 386
Mean 44.01
Std Dev 11.53
Turn on : 25.5514
Width : 3.098
Height : 9.981
Entry
ampl
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4
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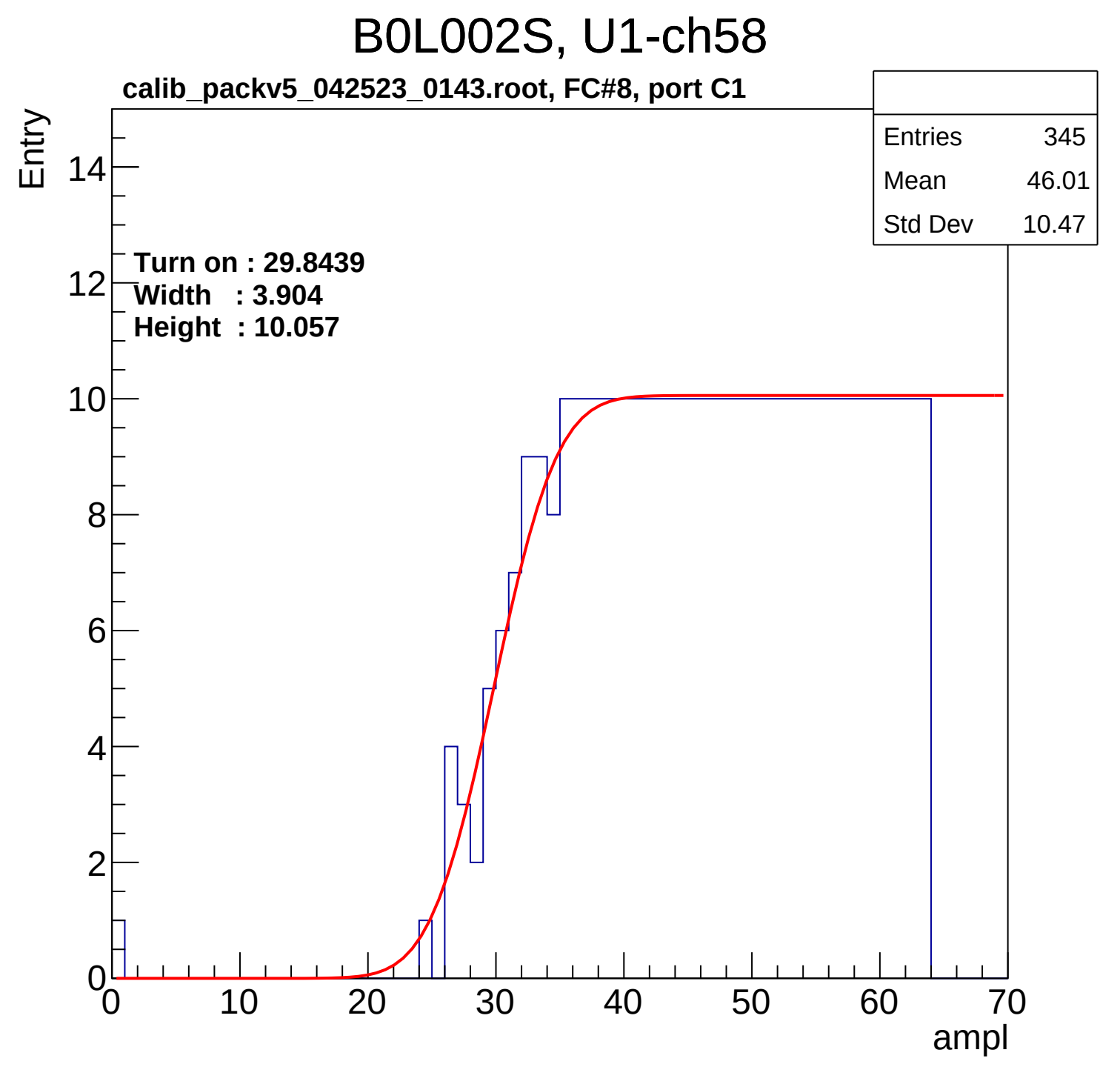
B0L002S, U1-ch58
calib_packv5_042523_0143.root, FC#8, port C1
Entries 345
Mean 46.01
Std Dev 10.47
Turn on : 29.8439
Width : 3.904
Height : 10.057
Entry
ampl
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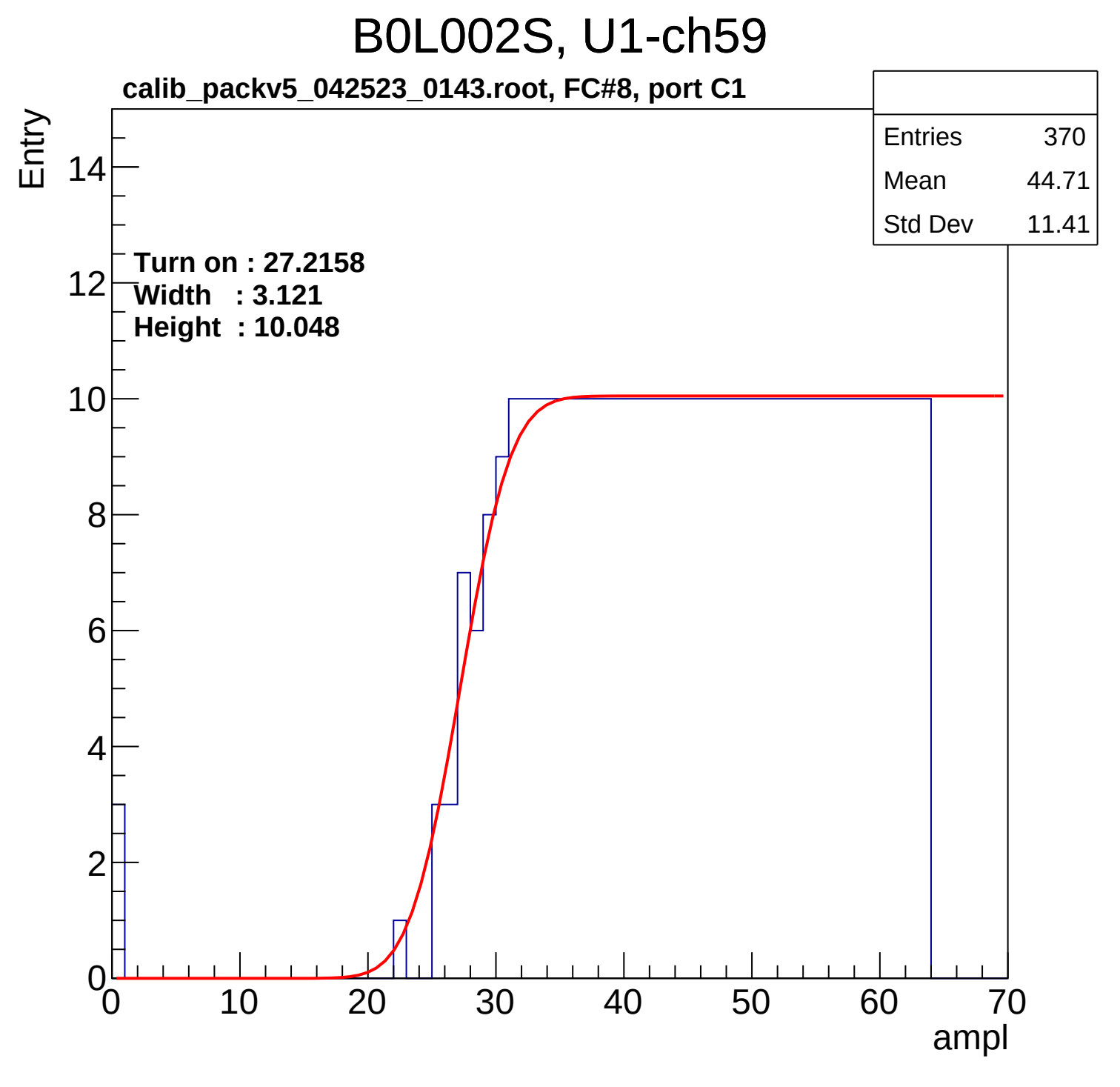
B0L002S, U1-ch59
calib_packv5_042523_0143.root, FC#8, port C1
Entries 370
Mean 44.71
Std Dev 11.41
Turn on : 27.2158
Width : 3.121
Height : 10.048
Entry
ampl
0
2
4
6
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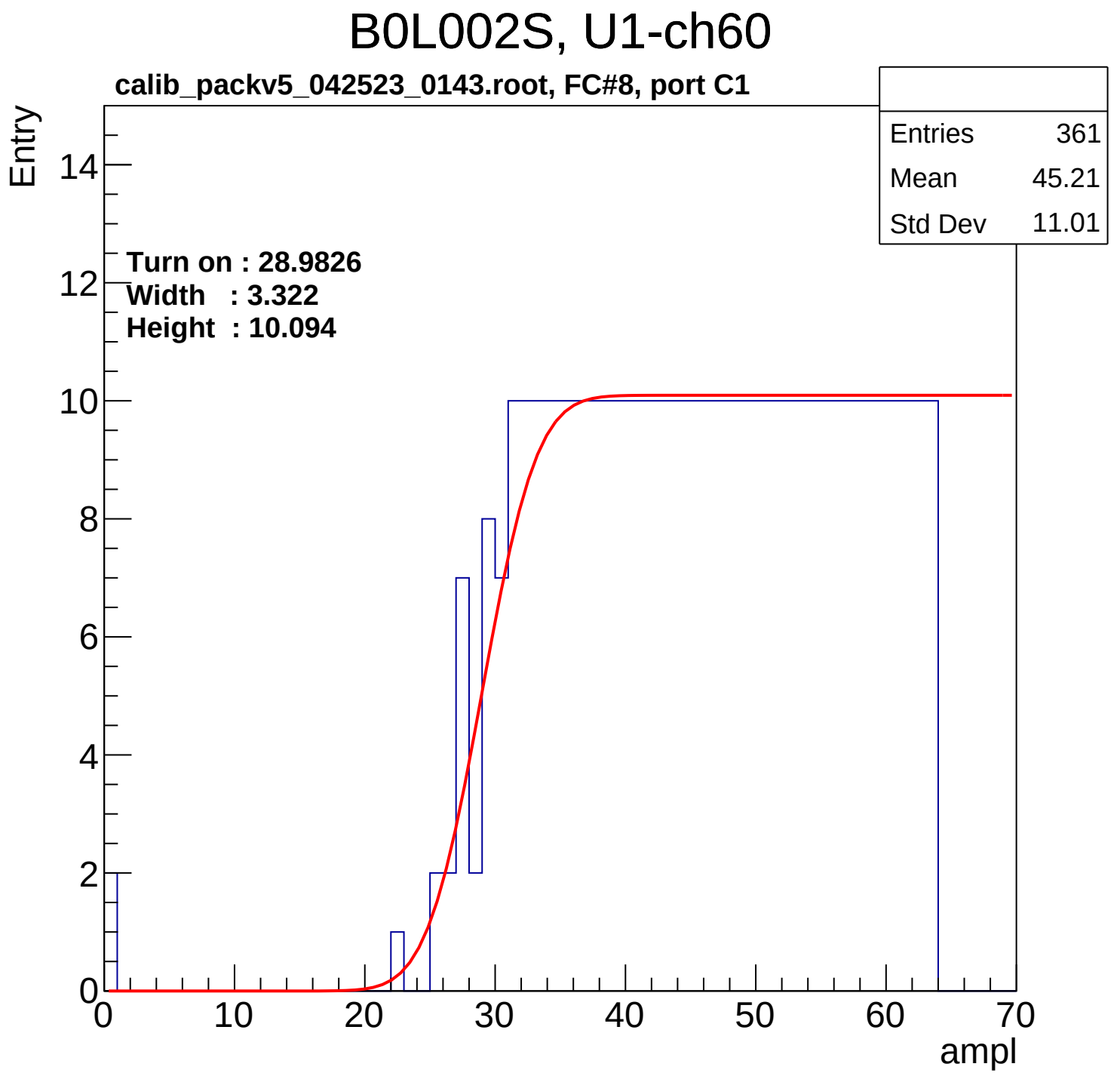
B0L002S, U1-ch60
calib_packv5_042523_0143.root, FC#8, port C1
Entries 361
Mean 45.21
Std Dev 11.01
Turn on : 28.9826
Width : 3.322
Height : 10.094
Entry
ampl
0
2
4
6
8
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0
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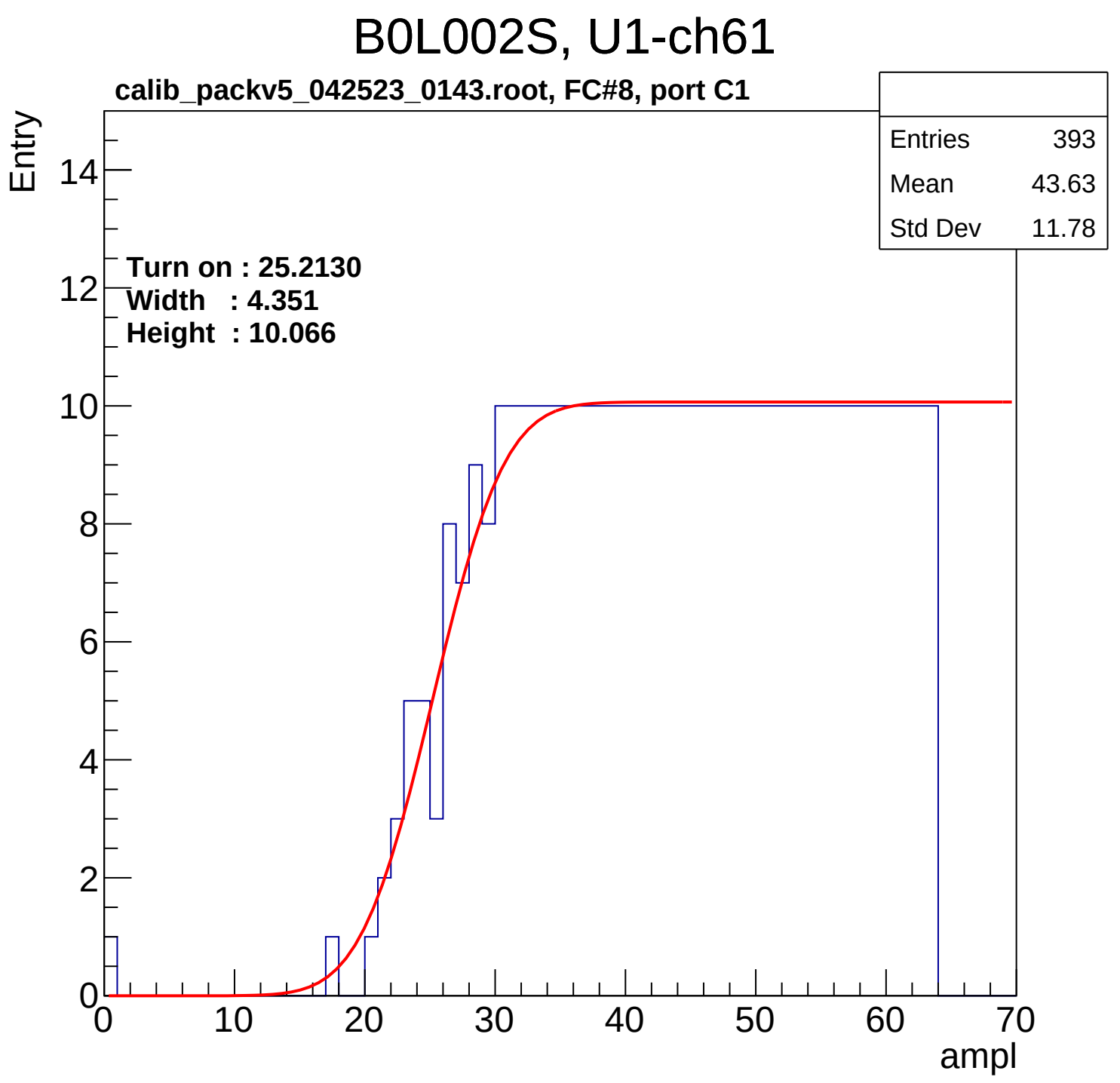
B0L002S, U1-ch61
calib_packv5_042523_0143.root, FC#8, port C1
Entries 393
Mean 43.63
Std Dev 11.78
Turn on : 25.2130
Width : 4.351
Height : 10.066
Entry
ampl
0
2
4
6
8
10
12
14
0
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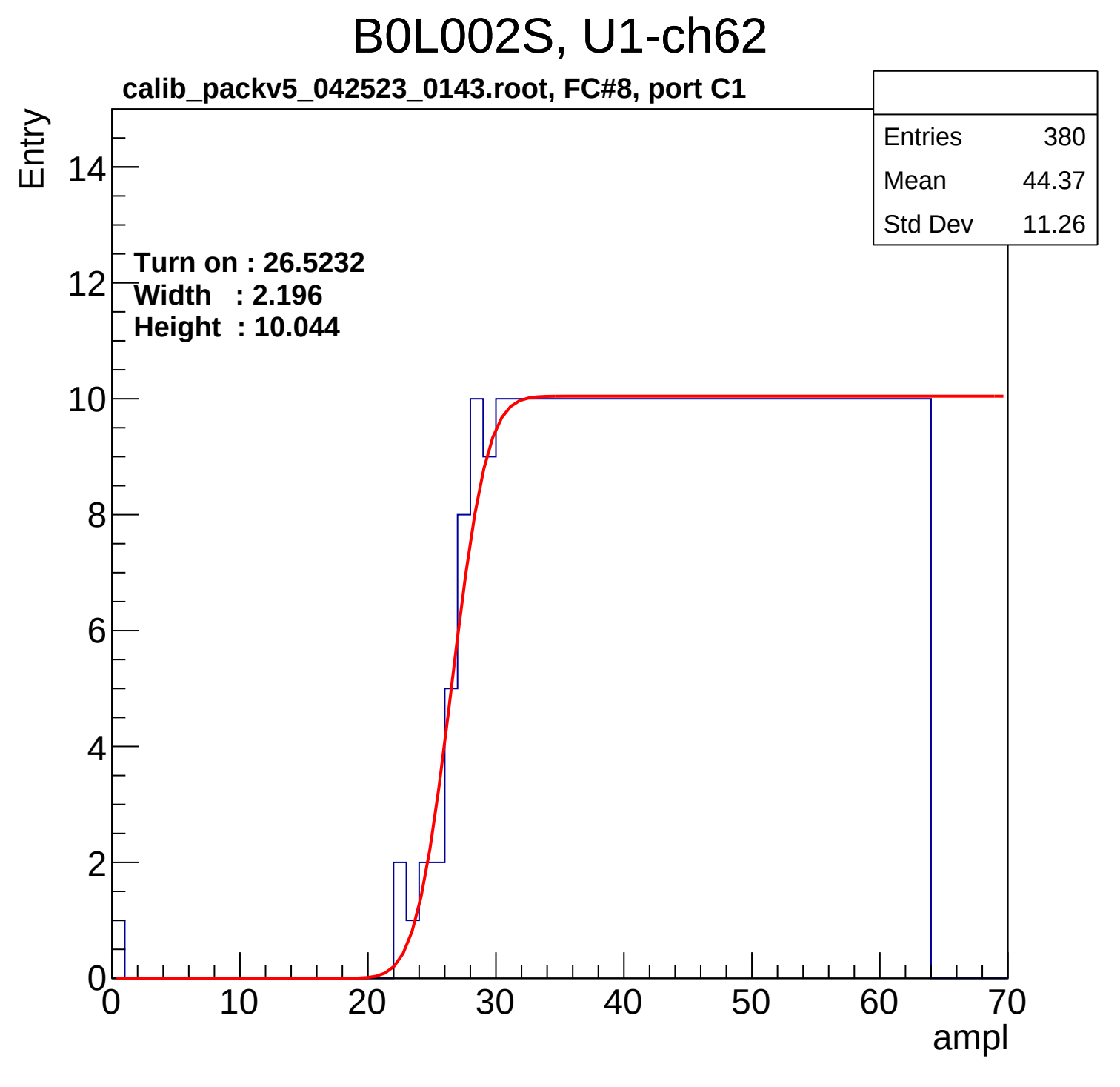
B0L002S, U1-ch62
calib_packv5_042523_0143.root, FC#8, port C1
Entries 380
Mean 44.37
Std Dev 11.26
Turn on : 26.5232
Width : 2.196
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
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0
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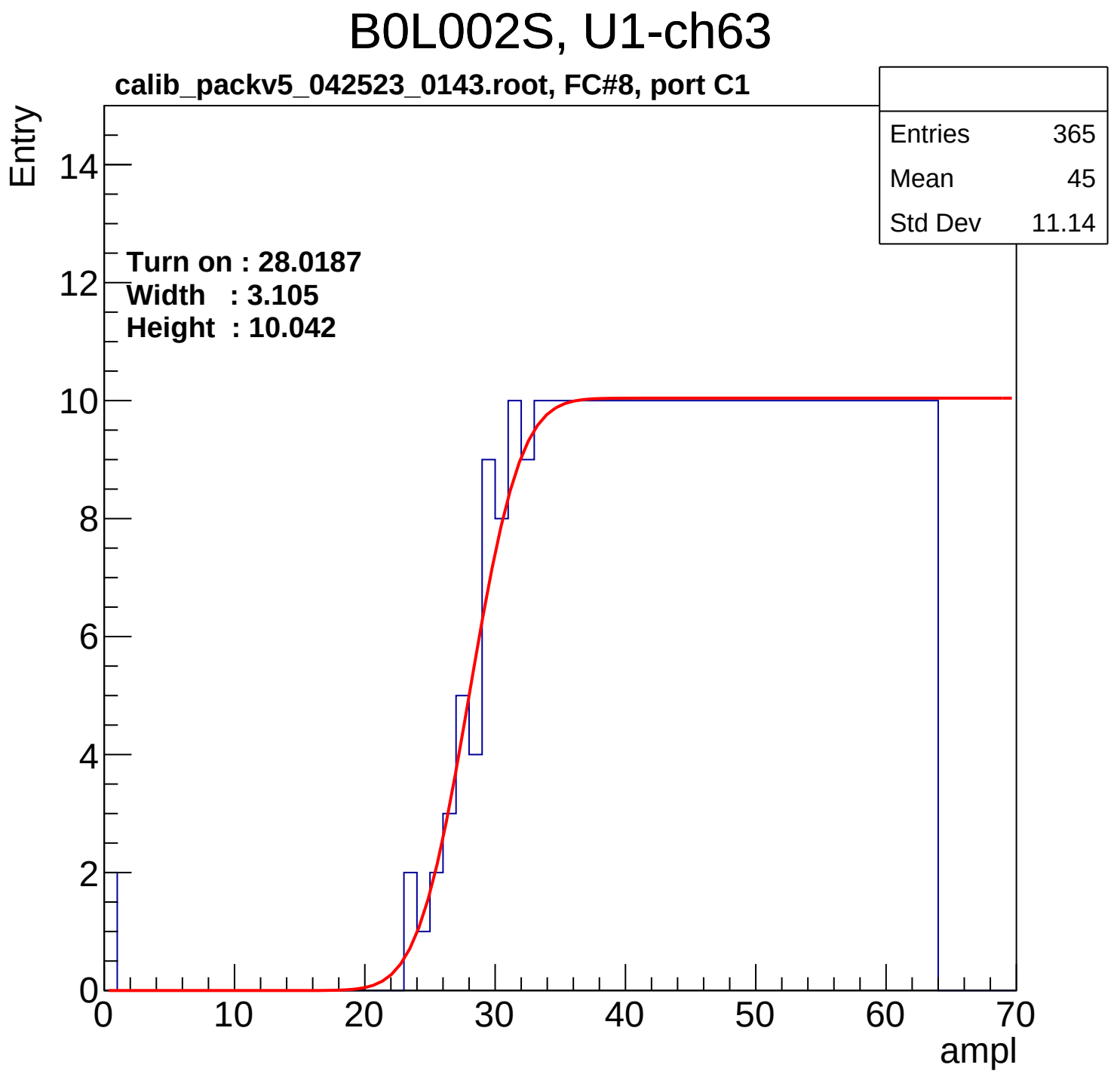
B0L002S, U1-ch63
calib_packv5_042523_0143.root, FC#8, port C1
Entries 365
Mean 45
Std Dev 11.14
Turn on : 28.0187
Width : 3.105
Height : 10.042
Entry
ampl
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2
4
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8
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12
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0
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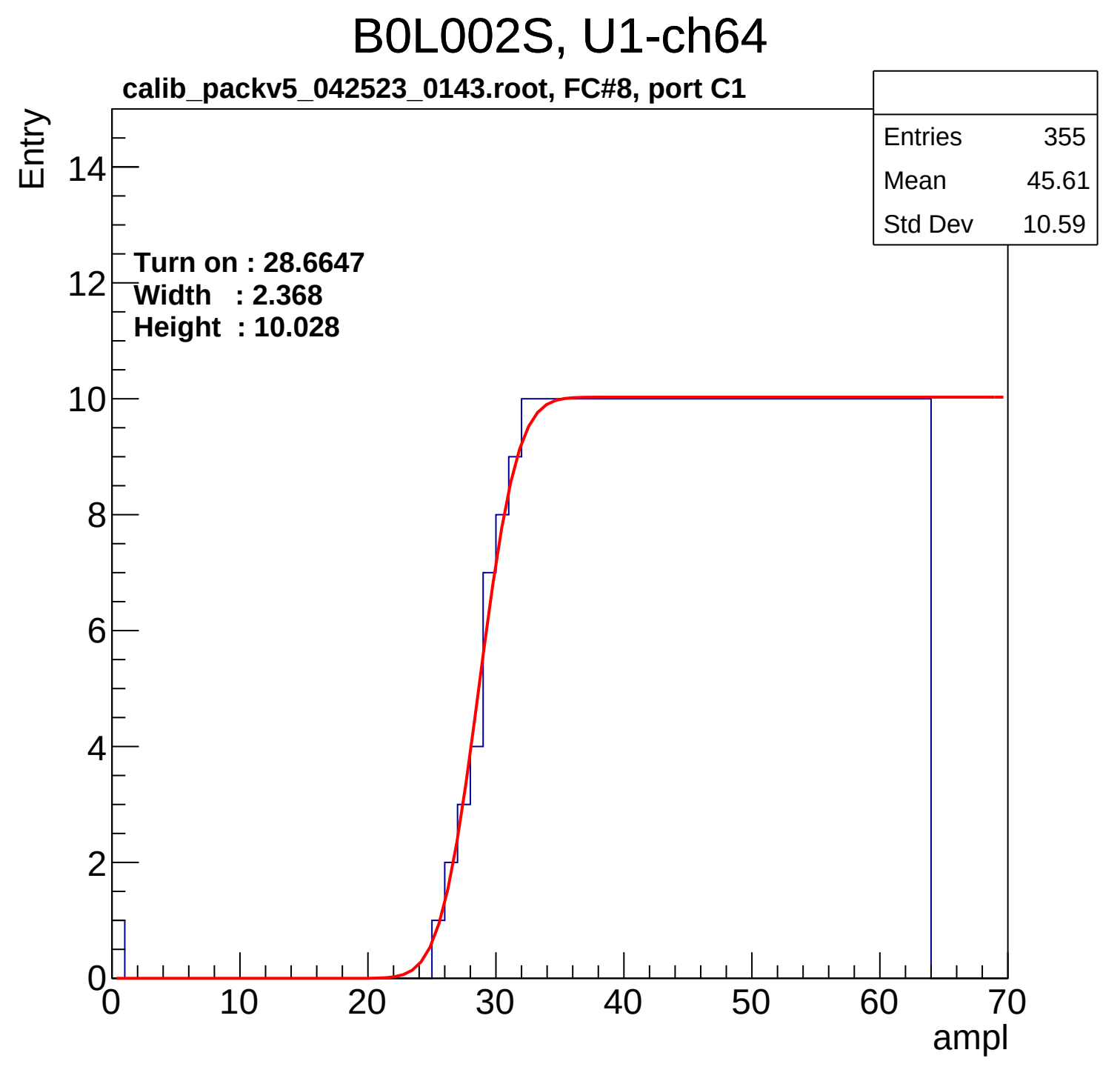
B0L002S, U1-ch64
calib_packv5_042523_0143.root, FC#8, port C1
Entries 355
Mean 45.61
Std Dev 10.59
Turn on : 28.6647
Width : 2.368
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
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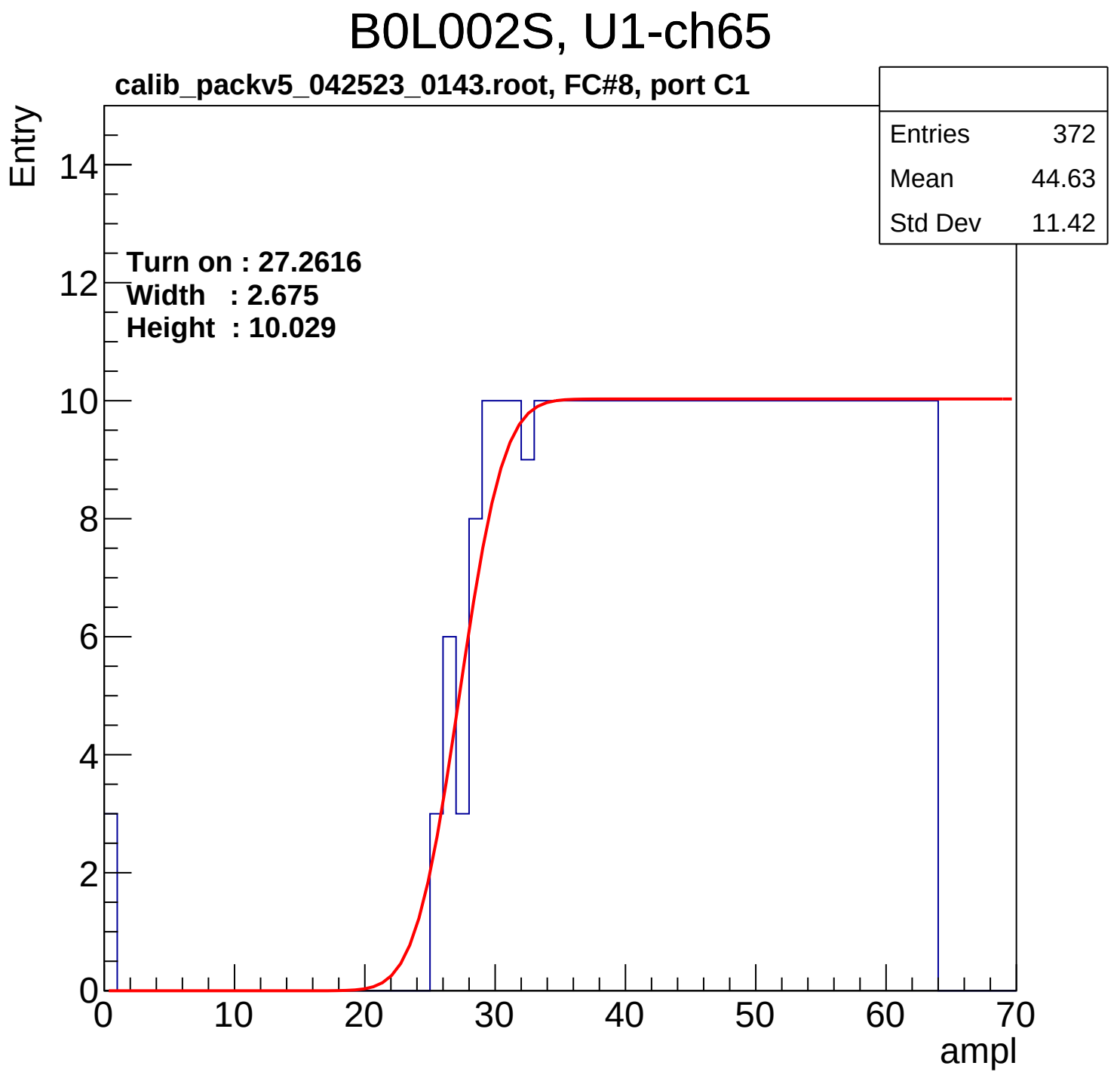
B0L002S, U1-ch65
calib_packv5_042523_0143.root, FC#8, port C1
Entries 372
Mean 44.63
Std Dev 11.42
Turn on : 27.2616
Width : 2.675
Height : 10.029
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
50
60
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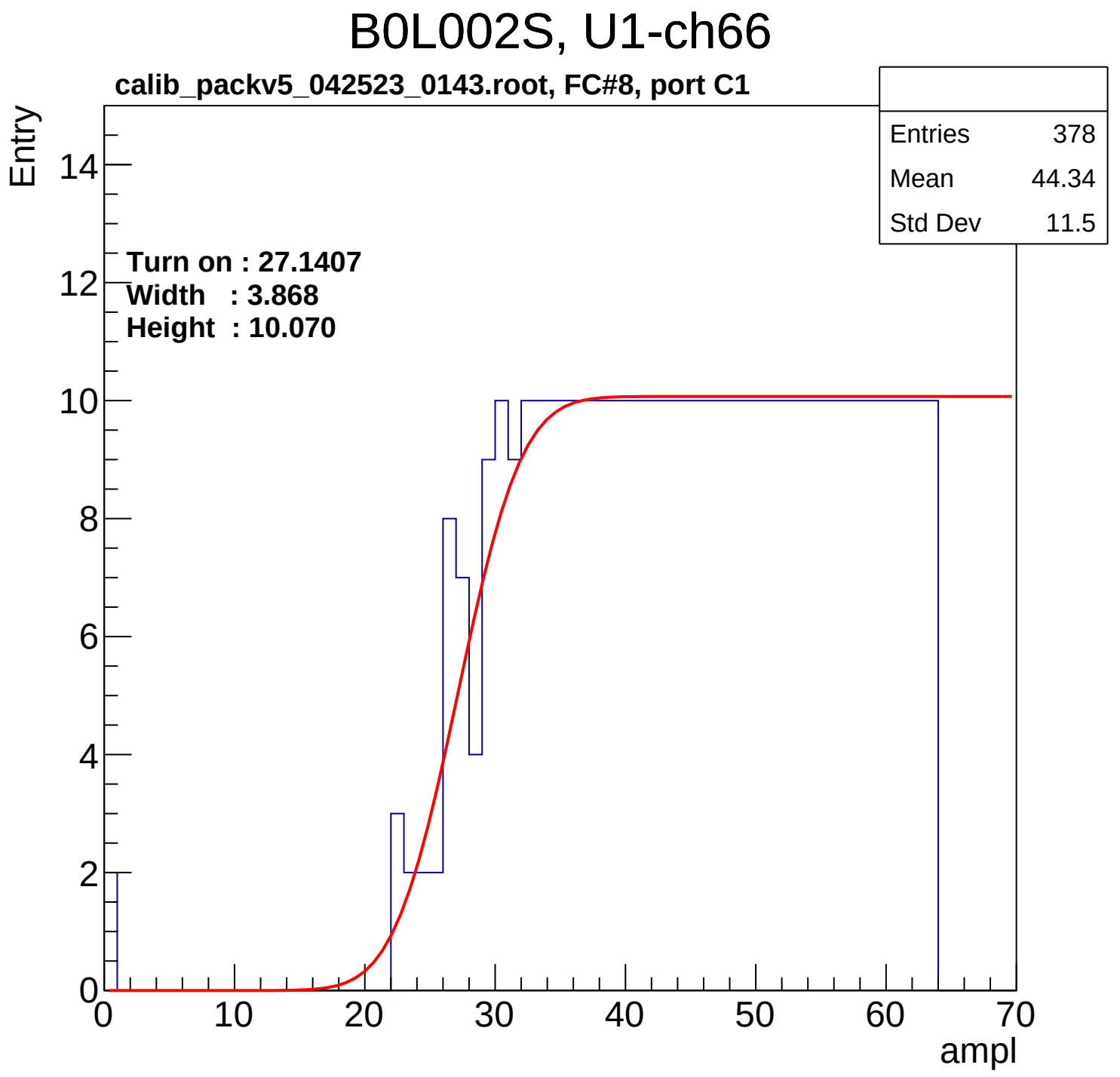
B0L002S, U1-ch66
calib_packv5_042523_0143.root, FC#8, port C1
Entries 378
Mean 44.34
Std Dev 11.5
Turn on : 27.1407
Width : 3.868
Height : 10.070
Entry
ampl
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4
6
8
10
12
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0
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60
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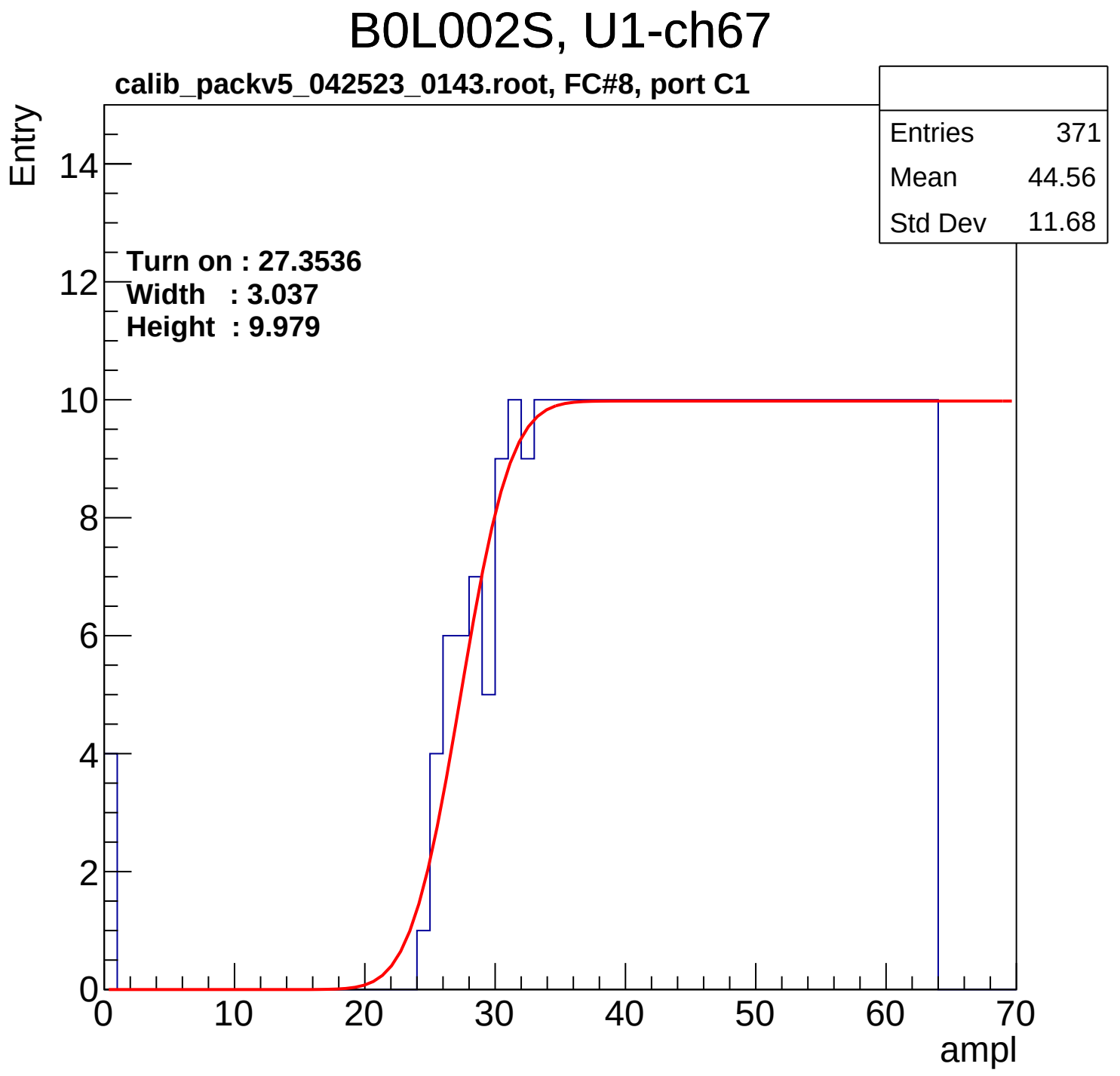
B0L002S, U1-ch67
calib_packv5_042523_0143.root, FC#8, port C1
Entries 371
Mean 44.56
Std Dev 11.68
Turn on : 27.3536
Width : 3.037
Height : 9.979
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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60
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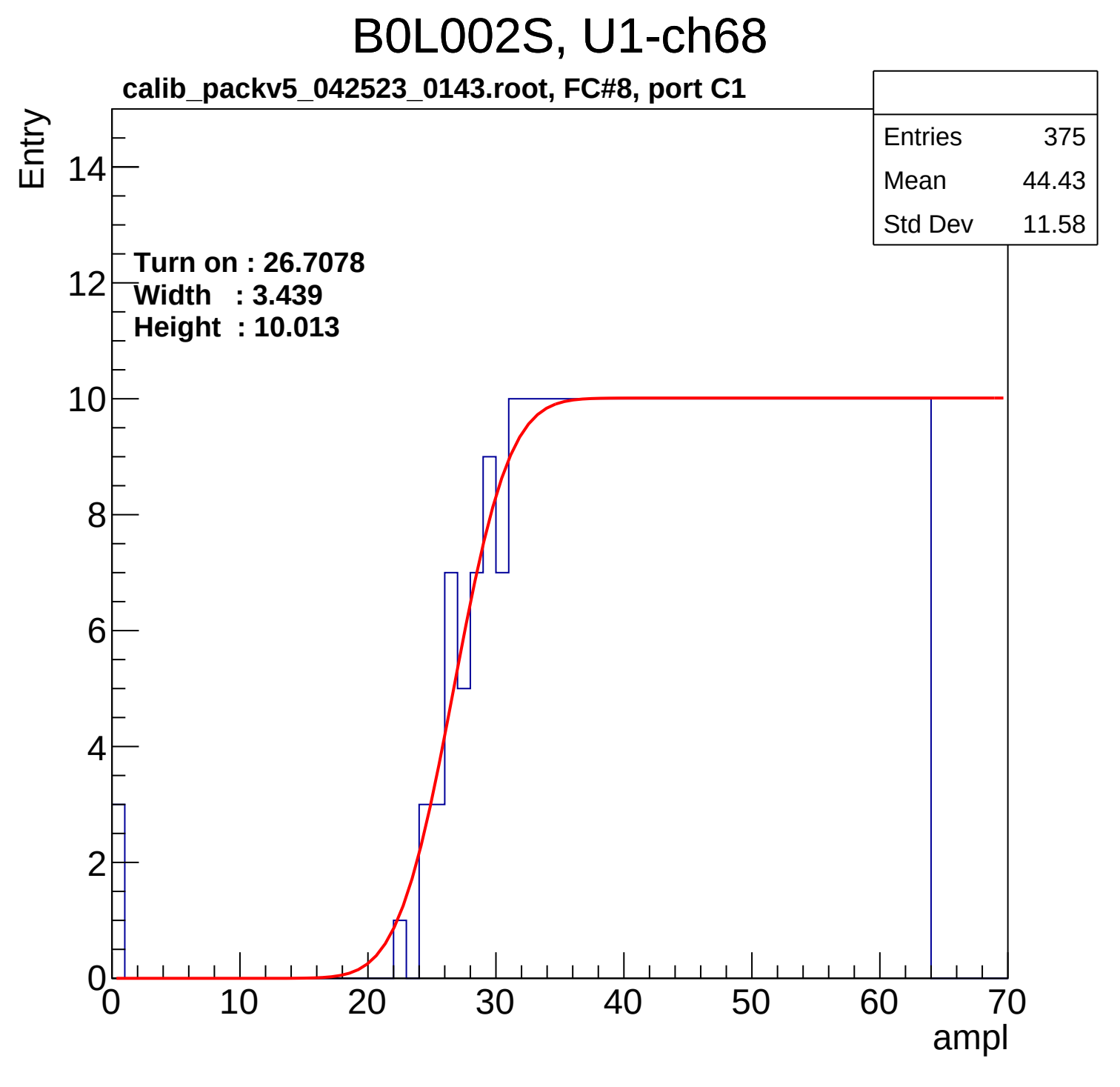
B0L002S, U1-ch68
calib_packv5_042523_0143.root, FC#8, port C1
Entries 375
Mean 44.43
Std Dev 11.58
Turn on : 26.7078
Width : 3.439
Height : 10.013
Entry
ampl
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6
8
10
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0
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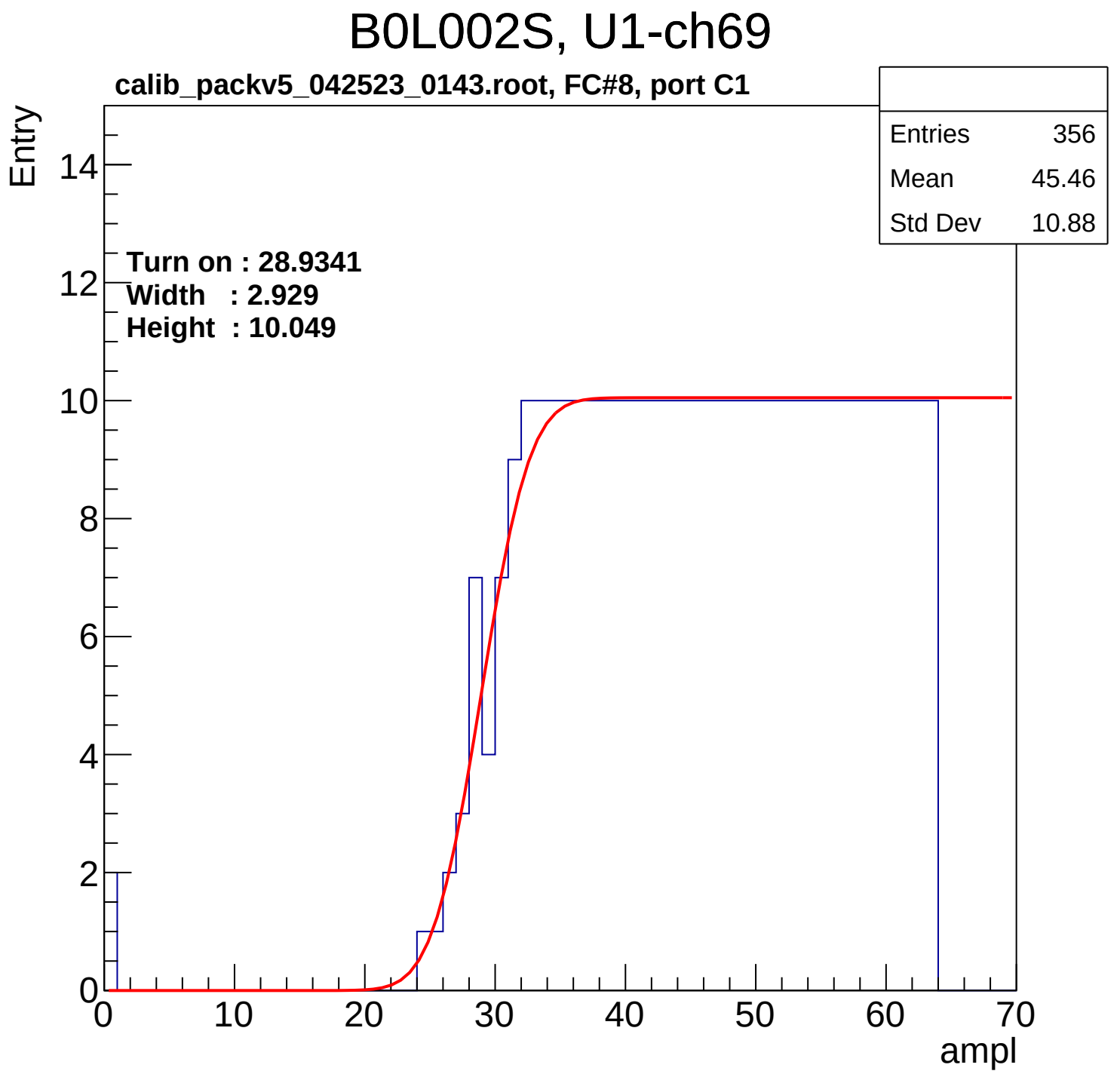
B0L002S, U1-ch69
calib_packv5_042523_0143.root, FC#8, port C1
Entries 356
Mean 45.46
Std Dev 10.88
Turn on : 28.9341
Width : 2.929
Height : 10.049
Entry
ampl
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2
4
6
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0
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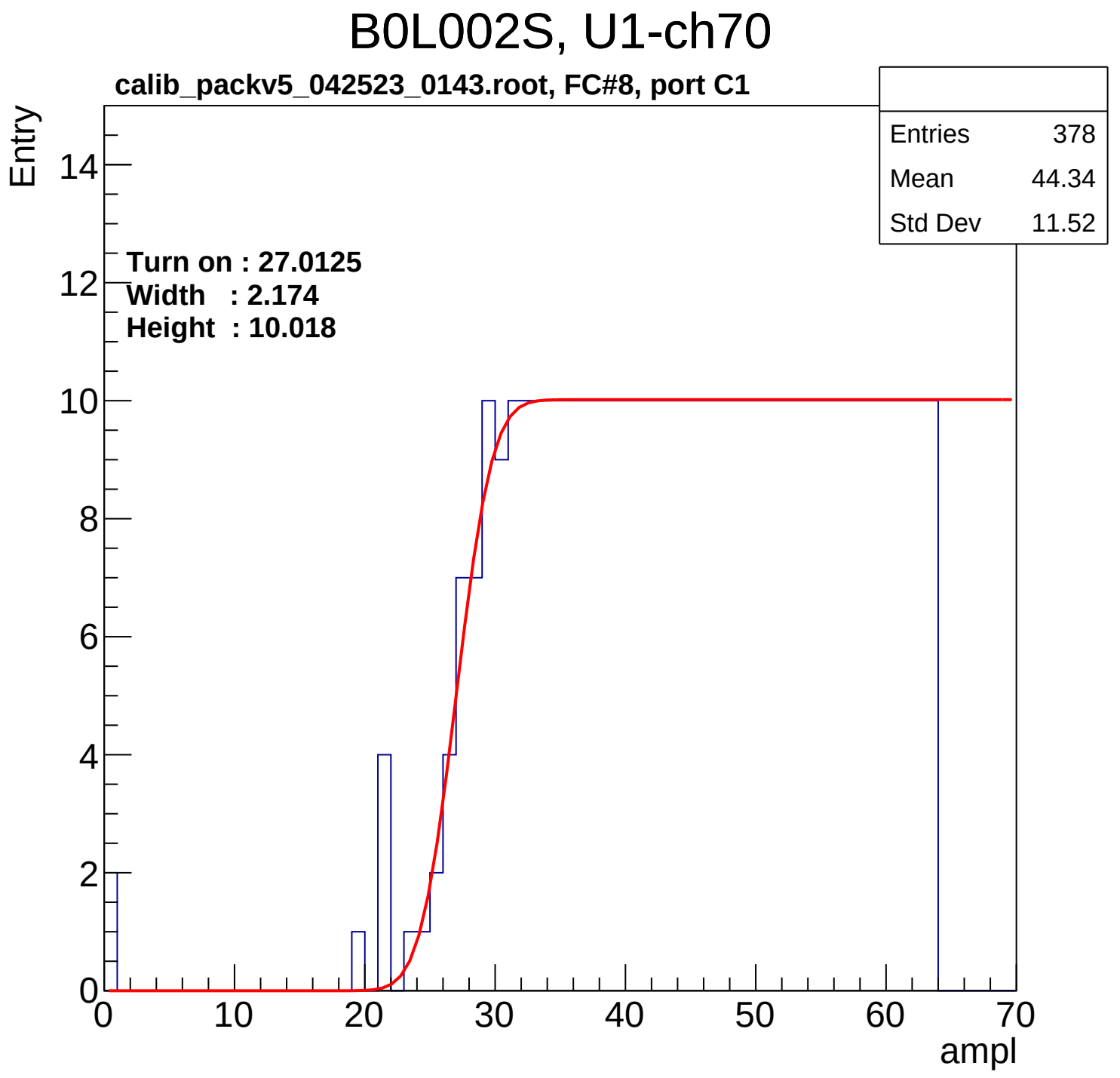
B0L002S, U1-ch70
calib_packv5_042523_0143.root, FC#8, port C1
Entries 378
Mean 44.34
Std Dev 11.52
Turn on : 27.0125
Width : 2.174
Height : 10.018
Entry
ampl
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0
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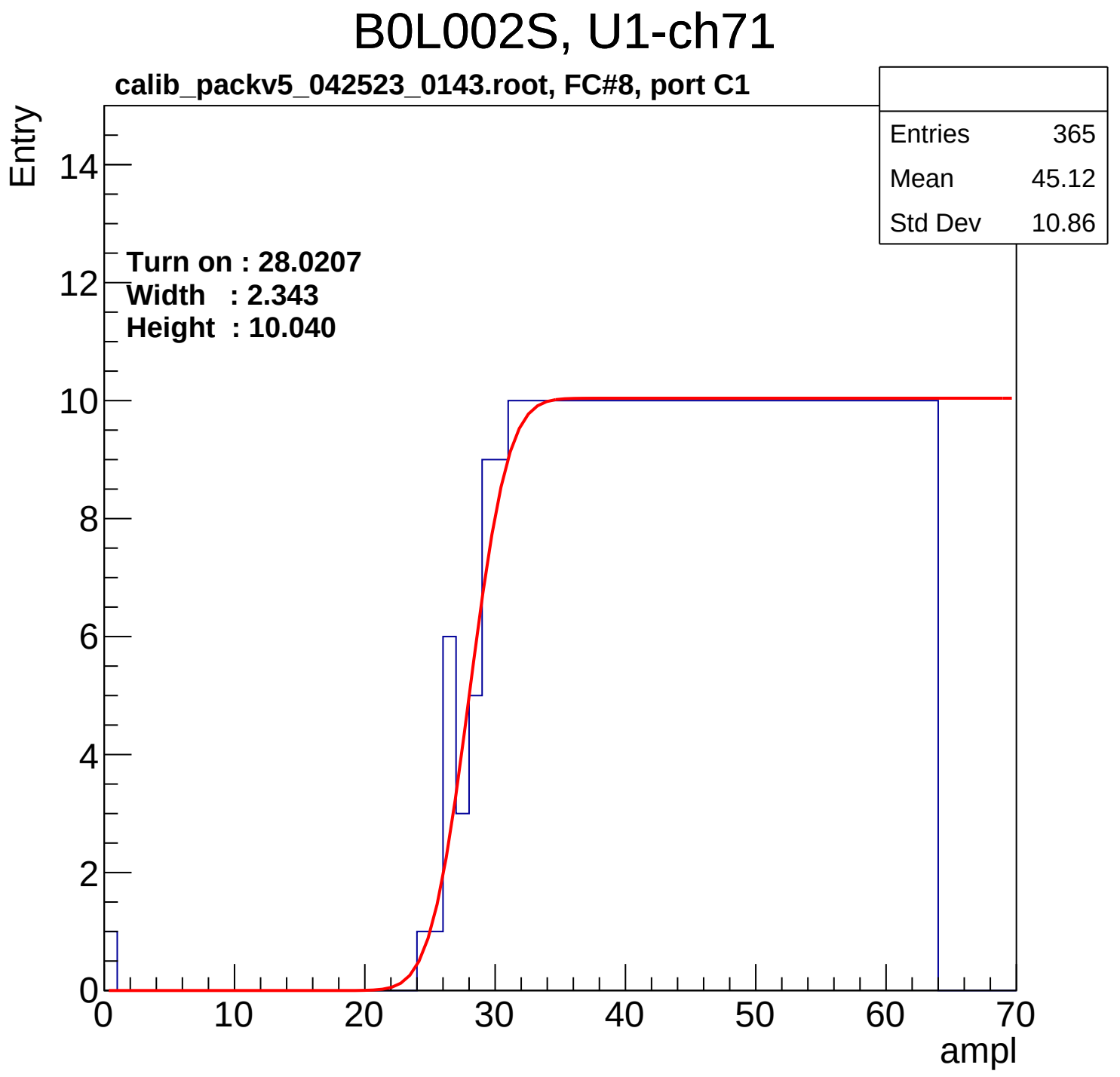
B0L002S, U1-ch71
calib_packv5_042523_0143.root, FC#8, port C1
Entries 365
Mean 45.12
Std Dev 10.86
Turn on : 28.0207
Width : 2.343
Height : 10.040
Entry
ampl
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2
4
6
8
10
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0
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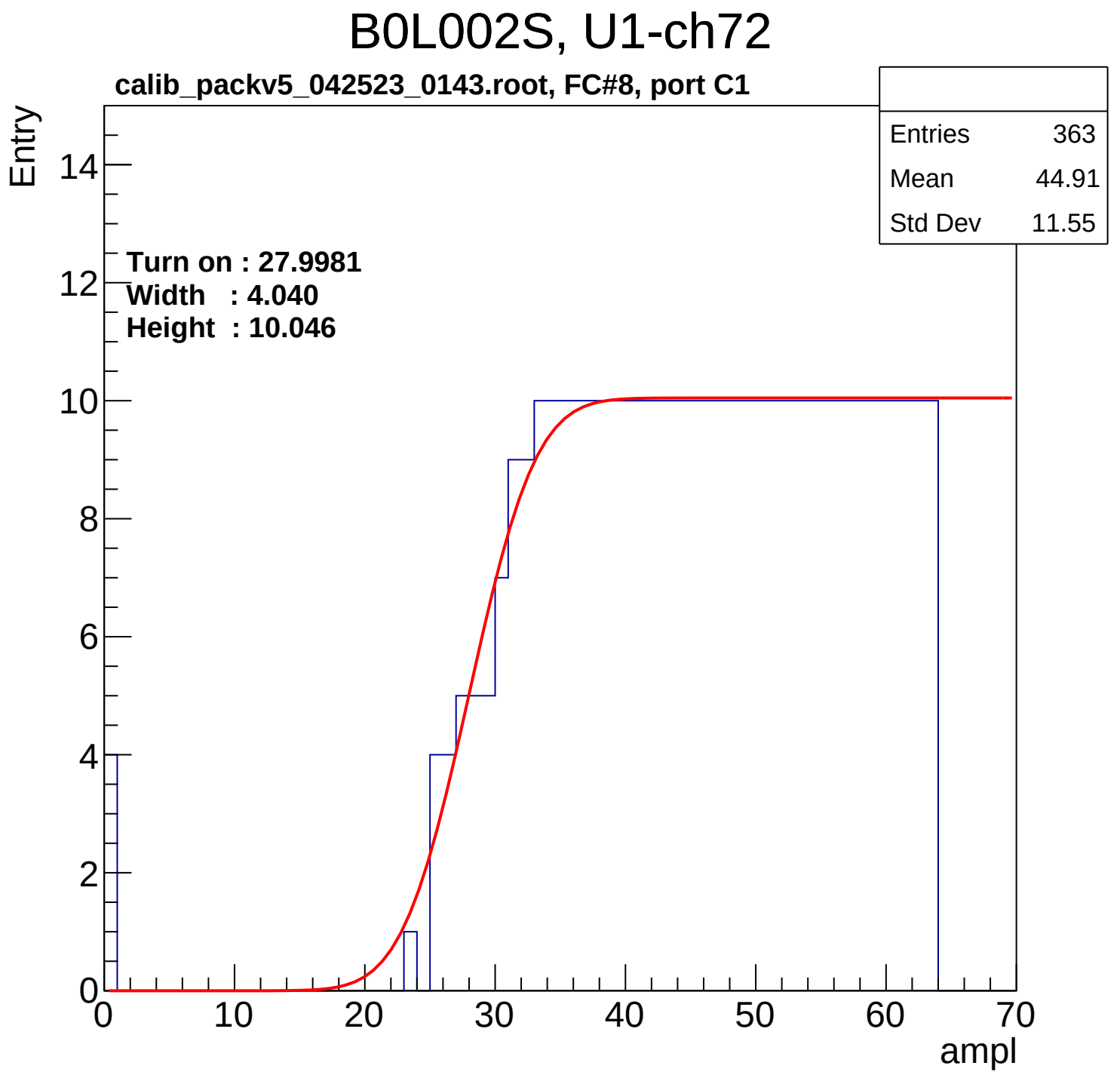
B0L002S, U1-ch72
calib_packv5_042523_0143.root, FC#8, port C1
Entries 363
Mean 44.91
Std Dev 11.55
Turn on : 27.9981
Width : 4.040
Height : 10.046
Entry
ampl
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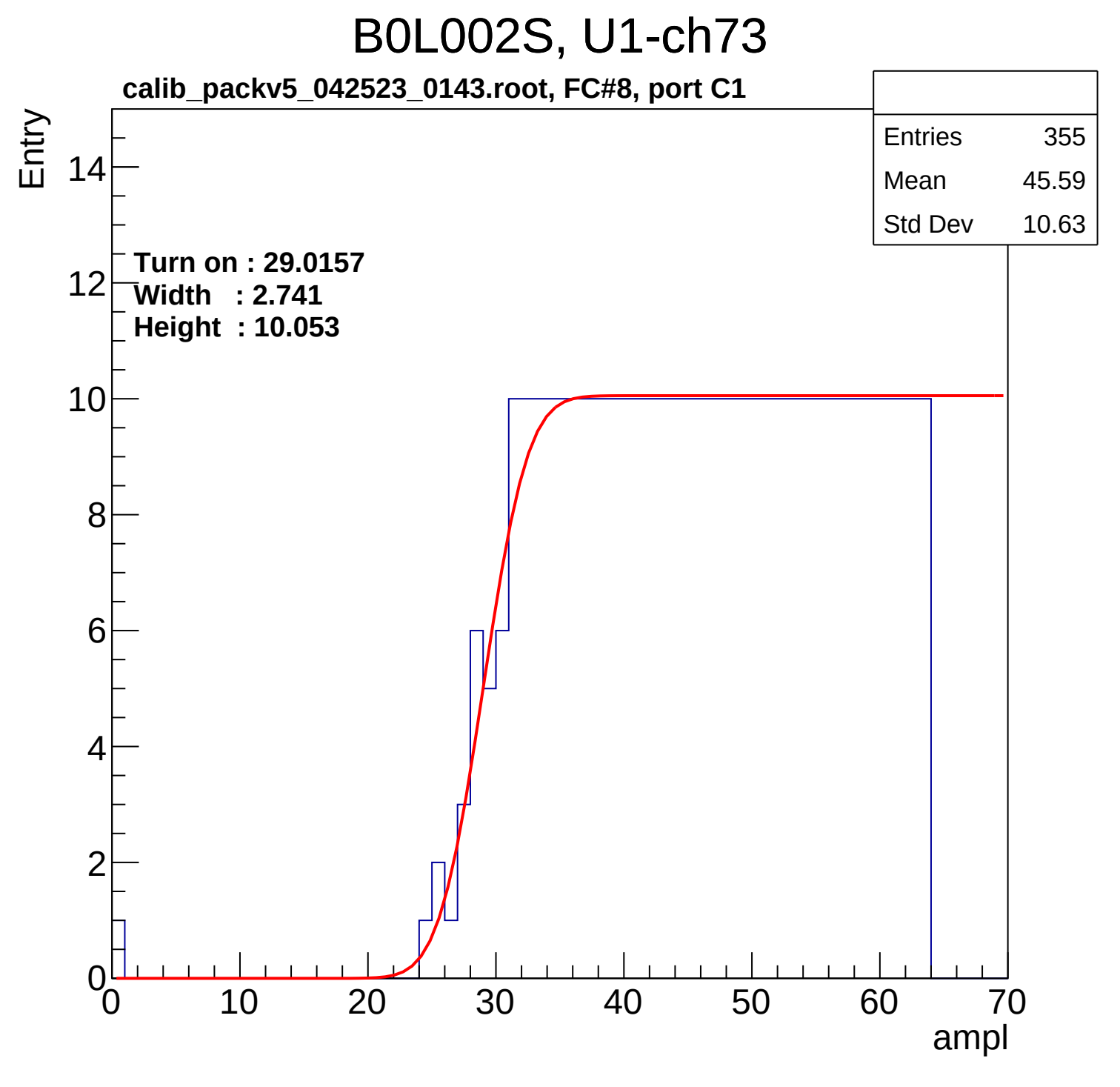
B0L002S, U1-ch73
calib_packv5_042523_0143.root, FC#8, port C1
Entries 355
Mean 45.59
Std Dev 10.63
Turn on : 29.0157
Width : 2.741
Height : 10.053
Entry
ampl
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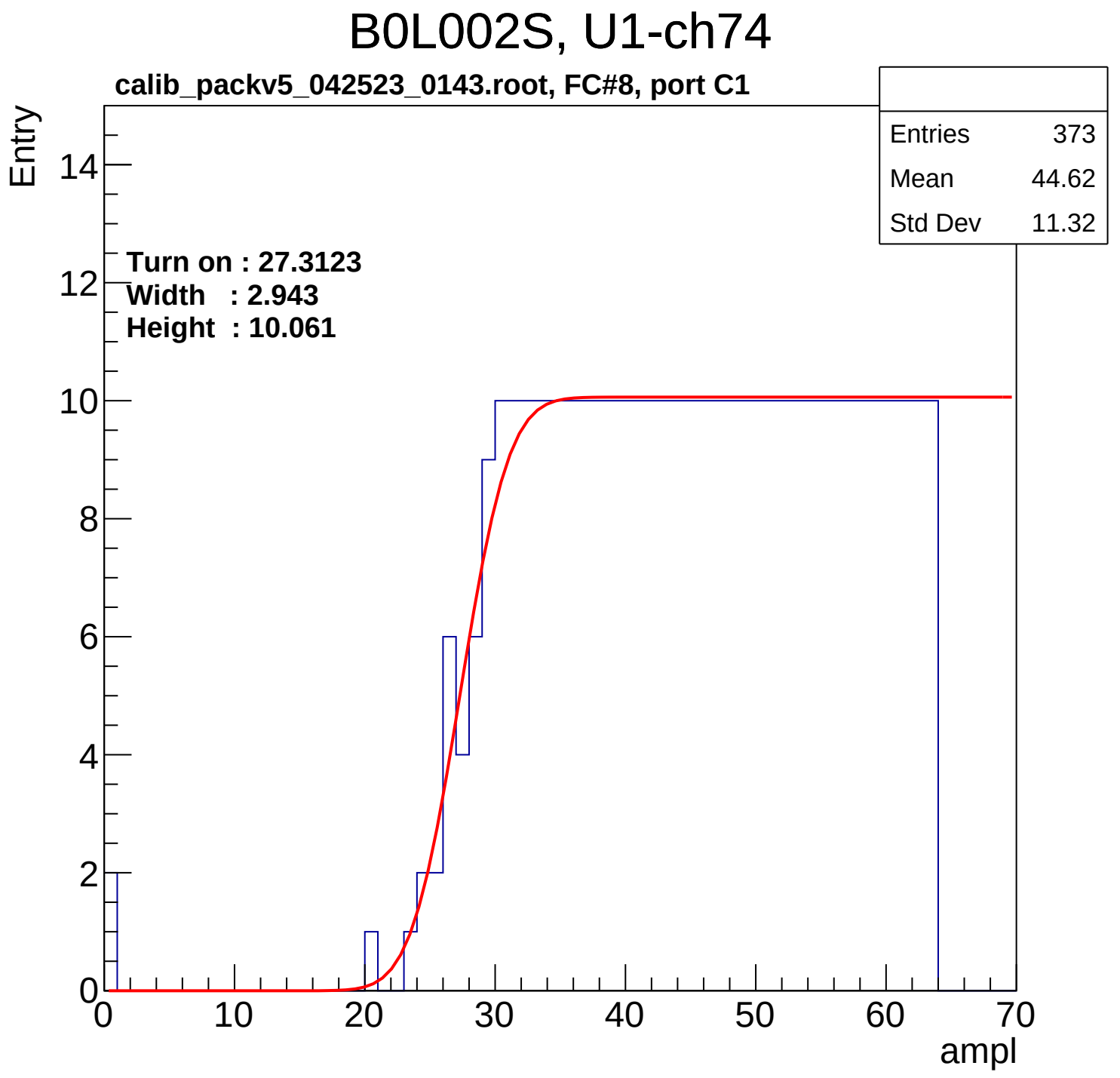
B0L002S, U1-ch74
calib_packv5_042523_0143.root, FC#8, port C1
Entries 373
Mean 44.62
Std Dev 11.32
Turn on : 27.3123
Width : 2.943
Height : 10.061
Entry
ampl
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10
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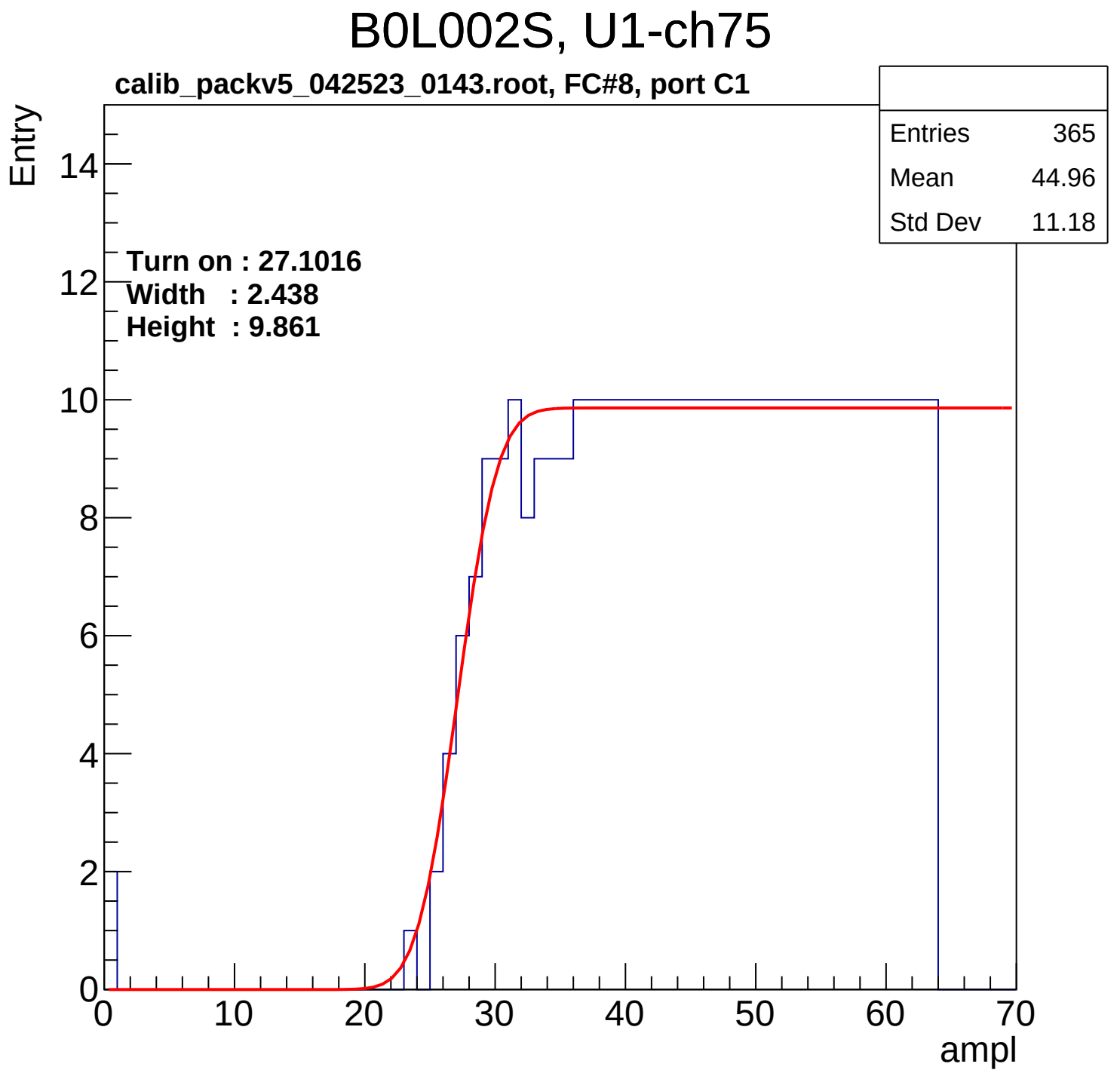
B0L002S, U1-ch75
calib_packv5_042523_0143.root, FC#8, port C1
Entries 365
Mean 44.96
Std Dev 11.18
Turn on : 27.1016
Width : 2.438
Height : 9.861
Entry
ampl
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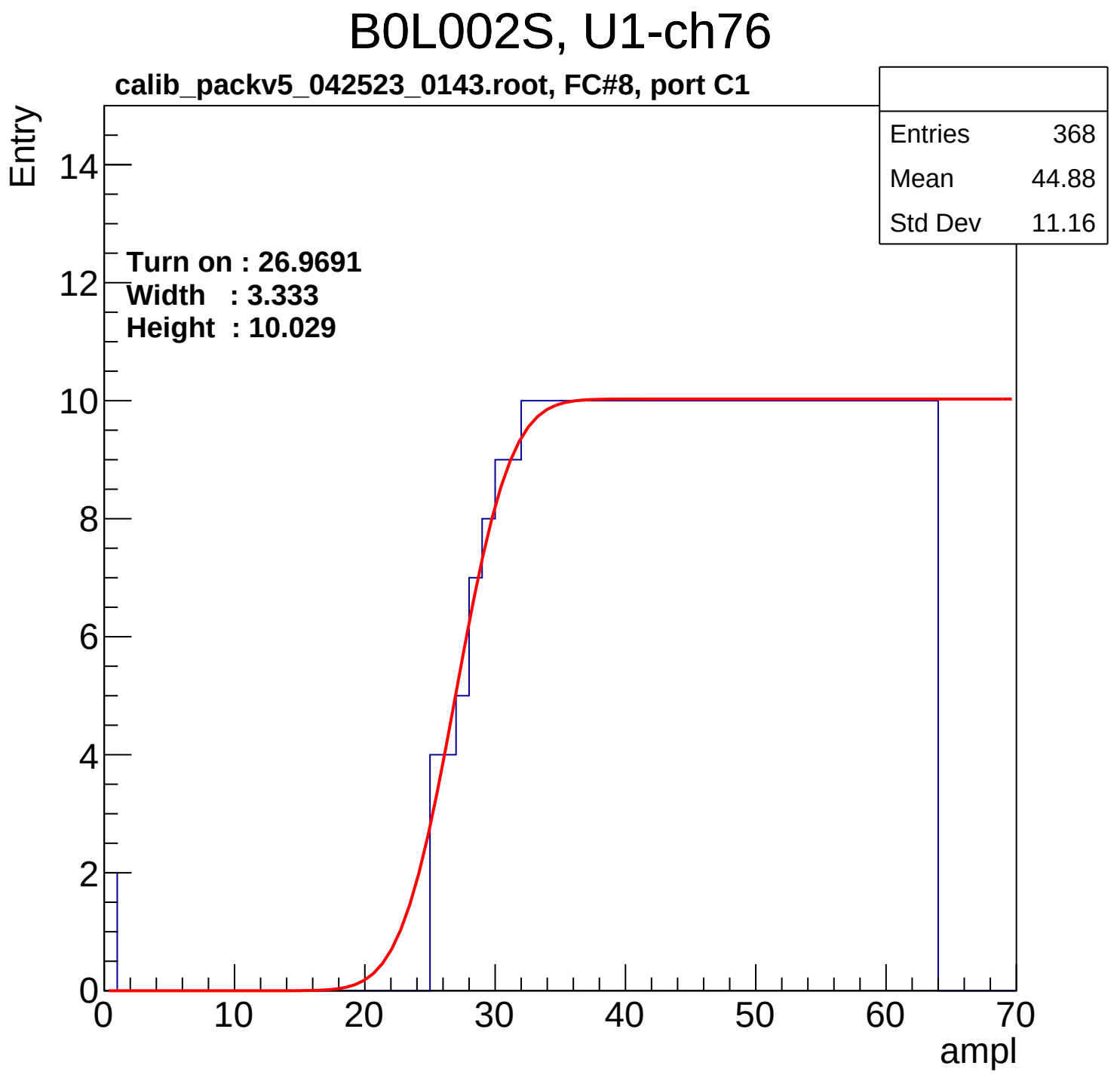
B0L002S, U1-ch76
calib_packv5_042523_0143.root, FC#8, port C1
Entries 368
Mean 44.88
Std Dev 11.16
Turn on : 26.9691
Width : 3.333
Height : 10.029
Entry
ampl
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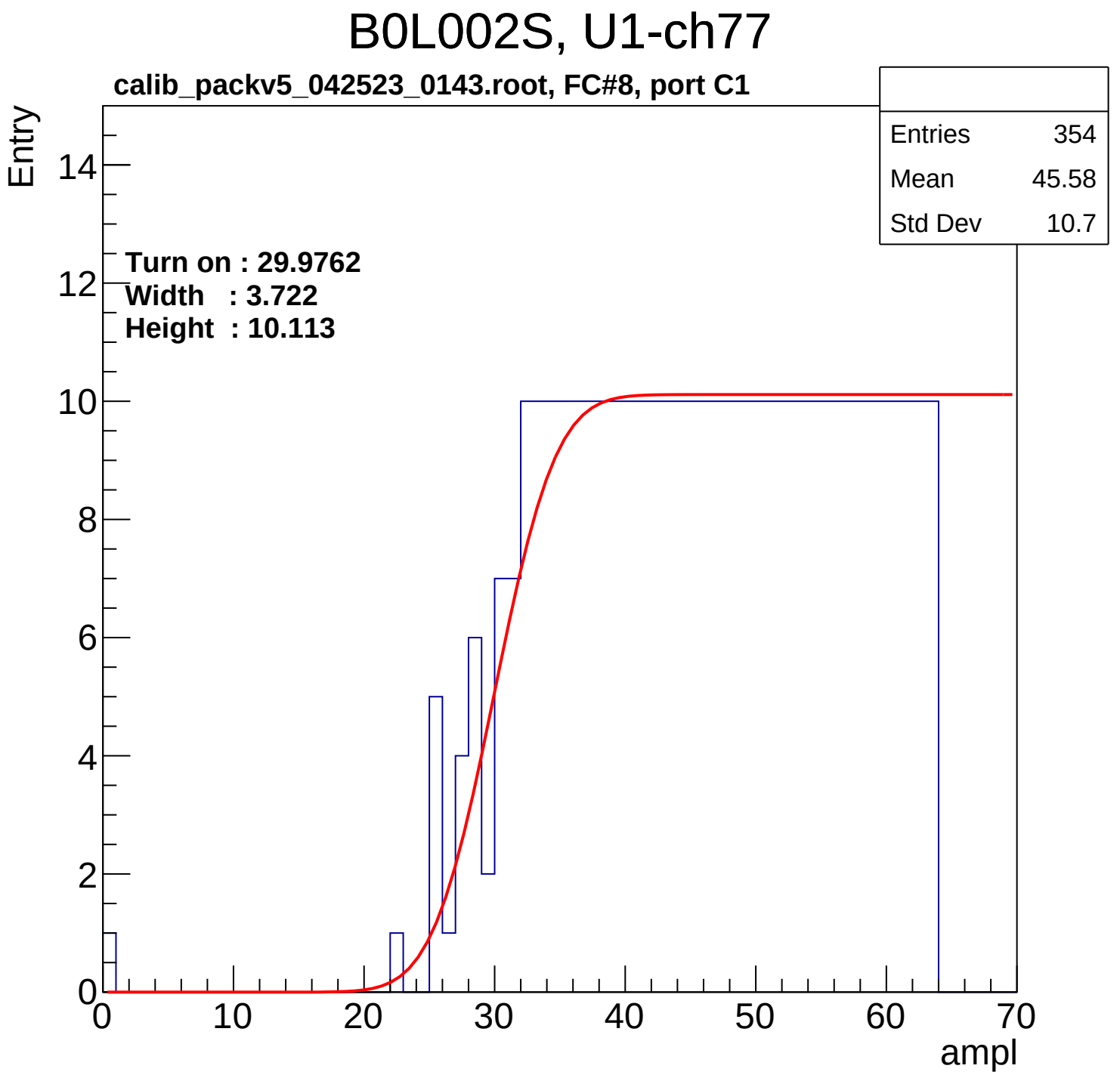
B0L002S, U1-ch77
calib_packv5_042523_0143.root, FC#8, port C1
Entries 354
Mean 45.58
Std Dev 10.7
Turn on : 29.9762
Width : 3.722
Height : 10.113
Entry
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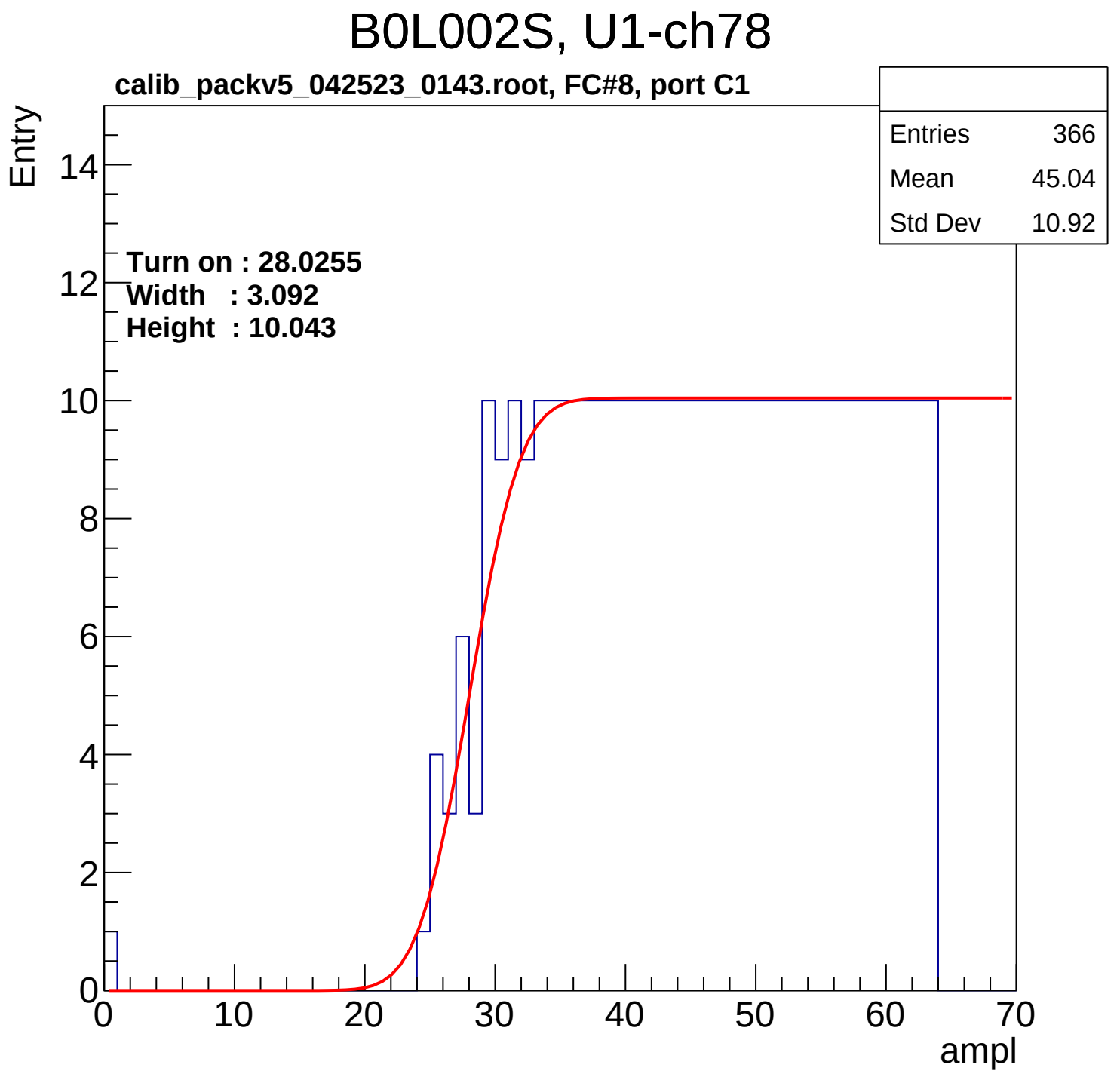
B0L002S, U1-ch78
calib_packv5_042523_0143.root, FC#8, port C1
Entries 366
Mean 45.04
Std Dev 10.92
Turn on : 28.0255
Width : 3.092
Height : 10.043
Entry
ampl
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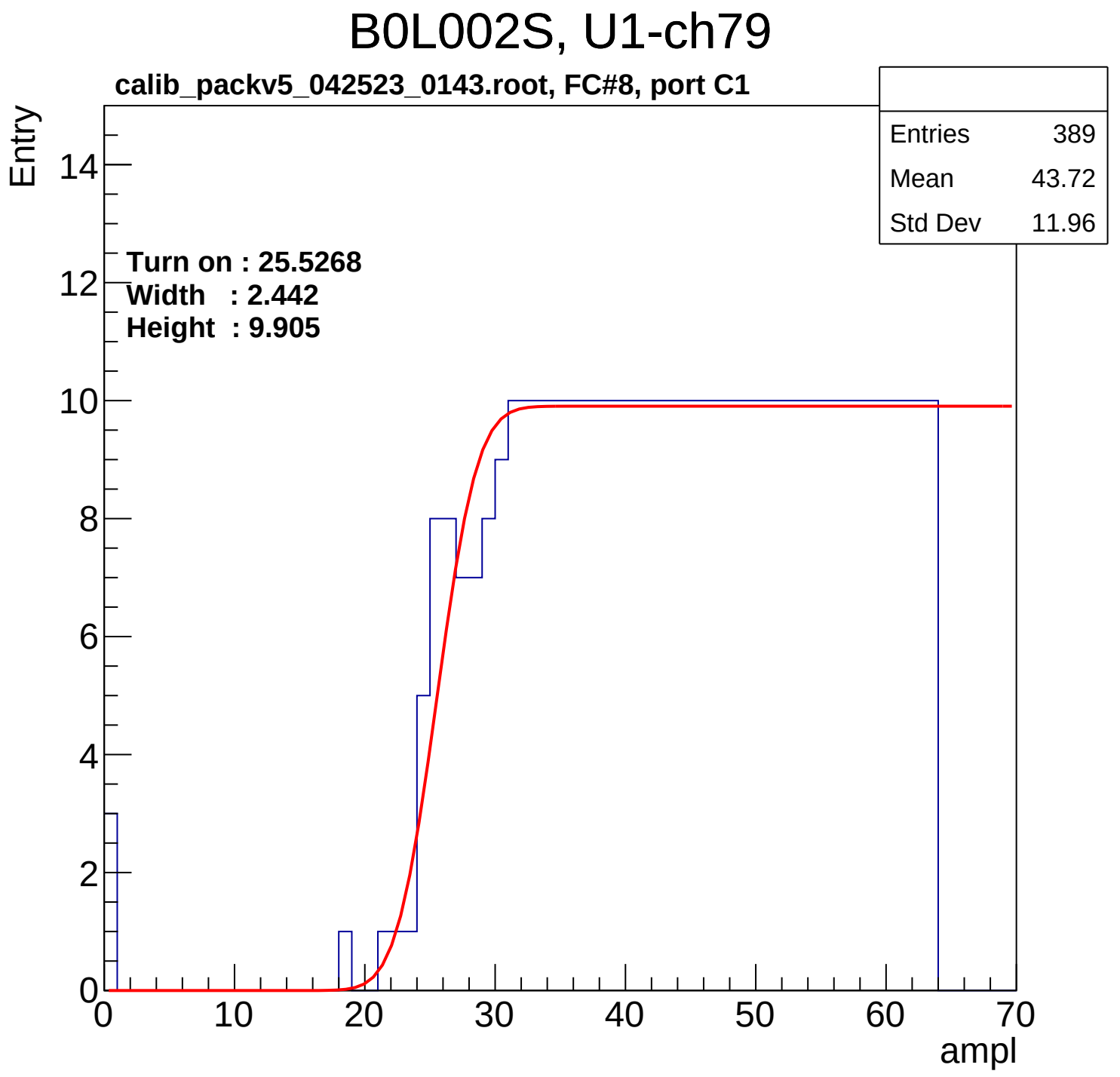
B0L002S, U1-ch79
calib_packv5_042523_0143.root, FC#8, port C1
Entries 389
Mean 43.72
Std Dev 11.96
Turn on : 25.5268
Width : 2.442
Height : 9.905
Entry
ampl
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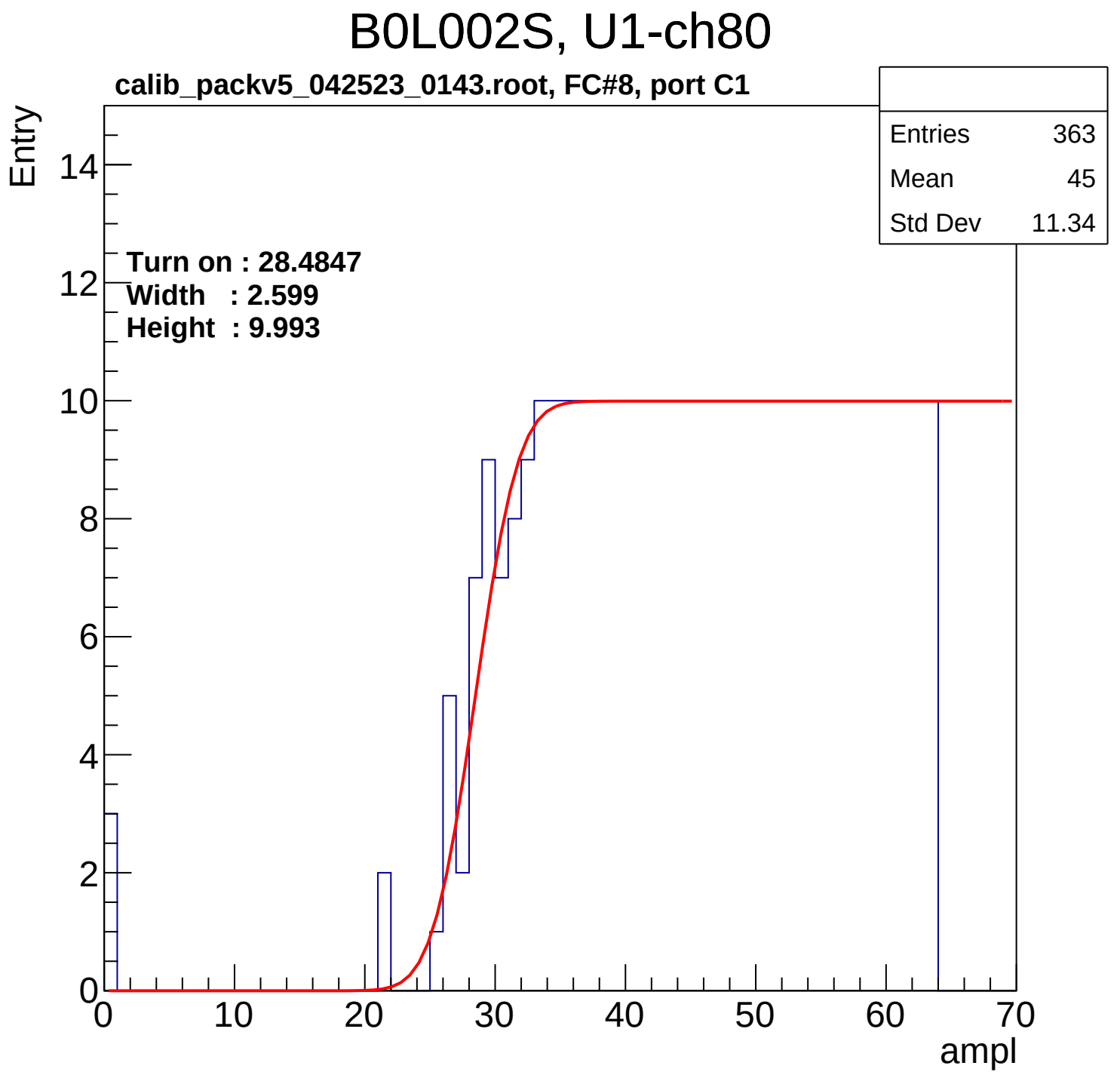
B0L002S, U1-ch80
calib_packv5_042523_0143.root, FC#8, port C1
Entries 363
Mean 45
Std Dev 11.34
Turn on : 28.4847
Width : 2.599
Height : 9.993
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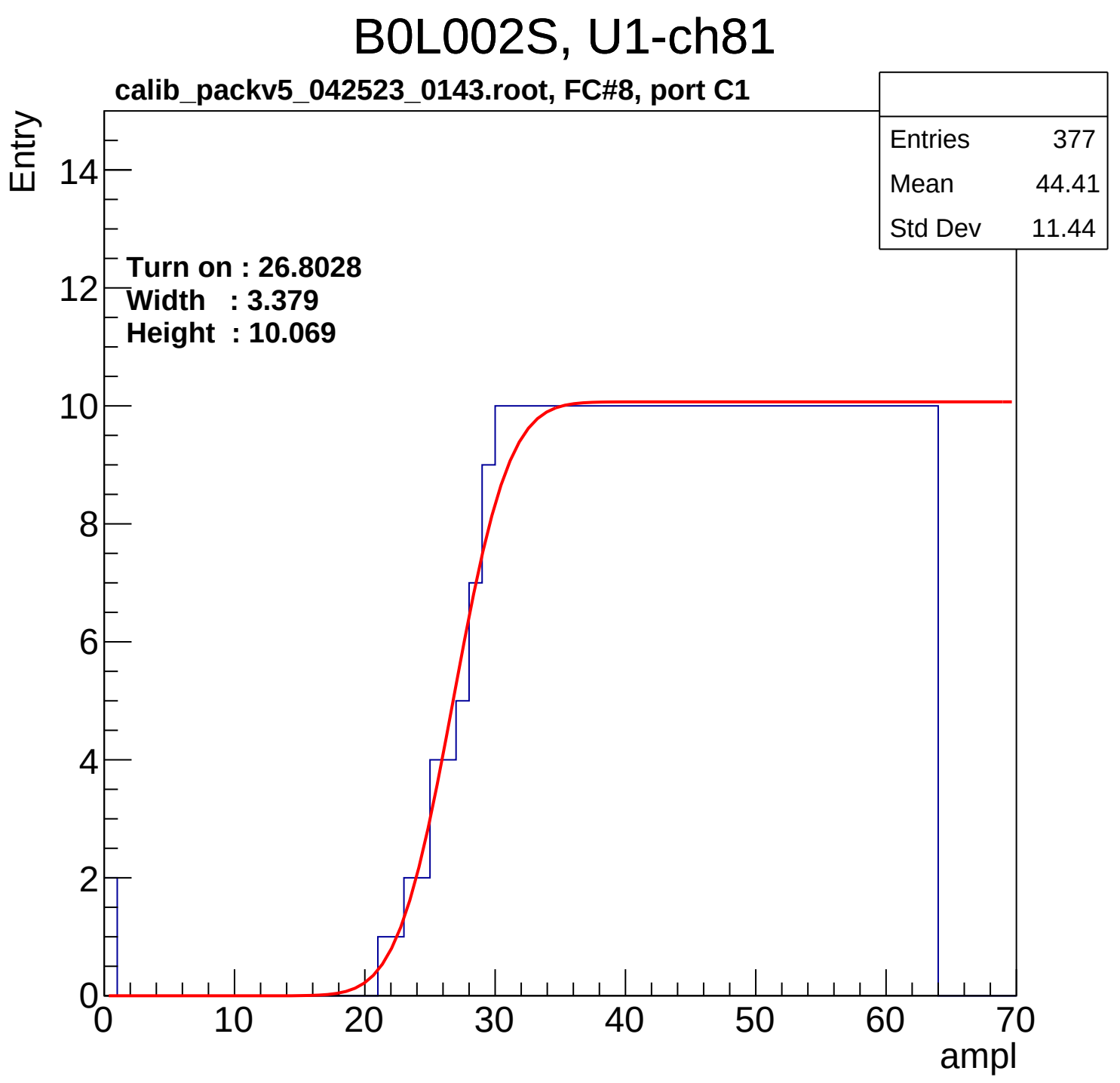
B0L002S, U1-ch81
calib_packv5_042523_0143.root, FC#8, port C1
Entries 377
Mean 44.41
Std Dev 11.44
Turn on : 26.8028
Width : 3.379
Height : 10.069
Entry
ampl
0
2
4
6
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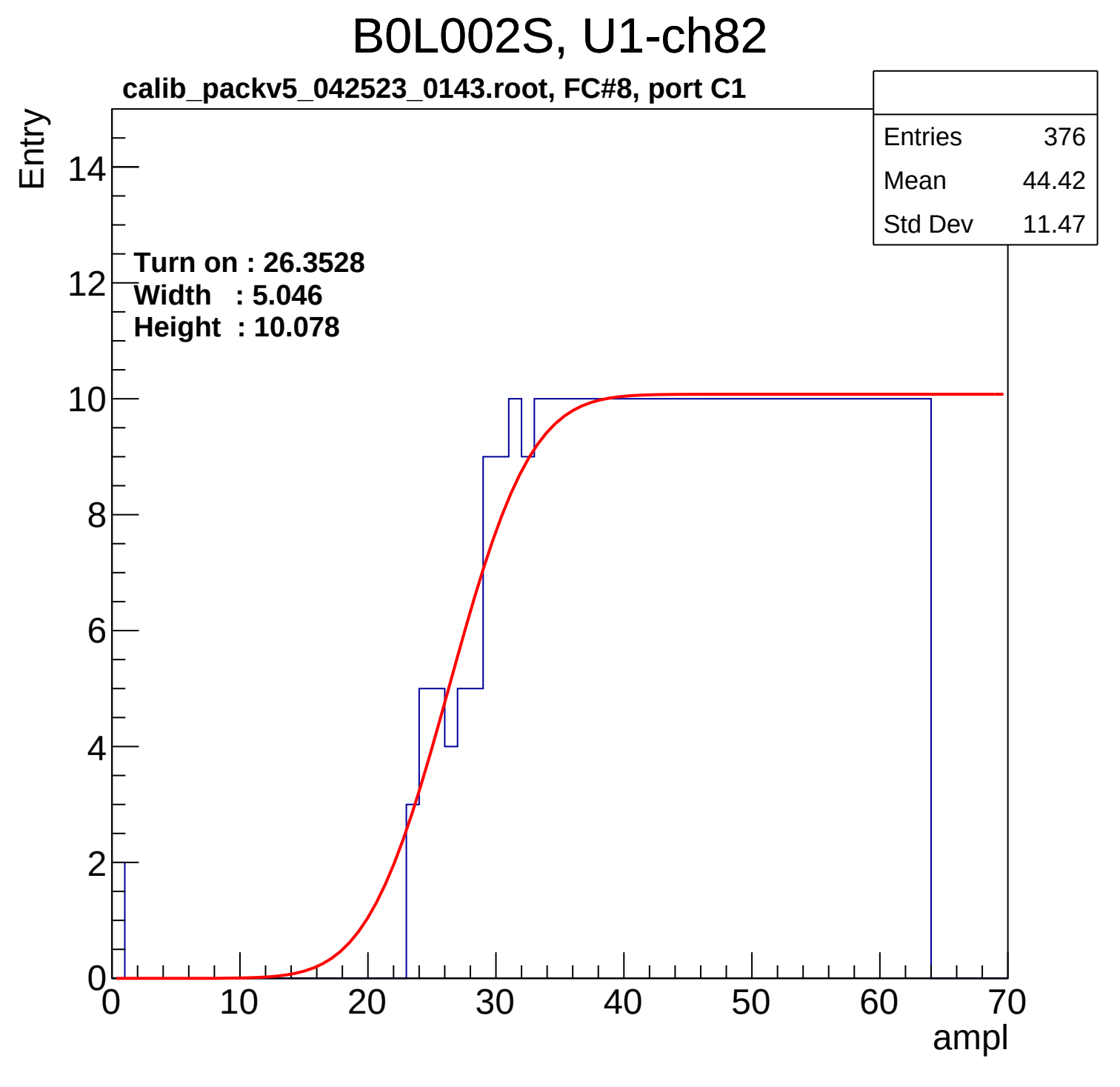
B0L002S, U1-ch82
calib_packv5_042523_0143.root, FC#8, port C1
Entries 376
Mean 44.42
Std Dev 11.47
Turn on : 26.3528
Width : 5.046
Height : 10.078
Entry
ampl
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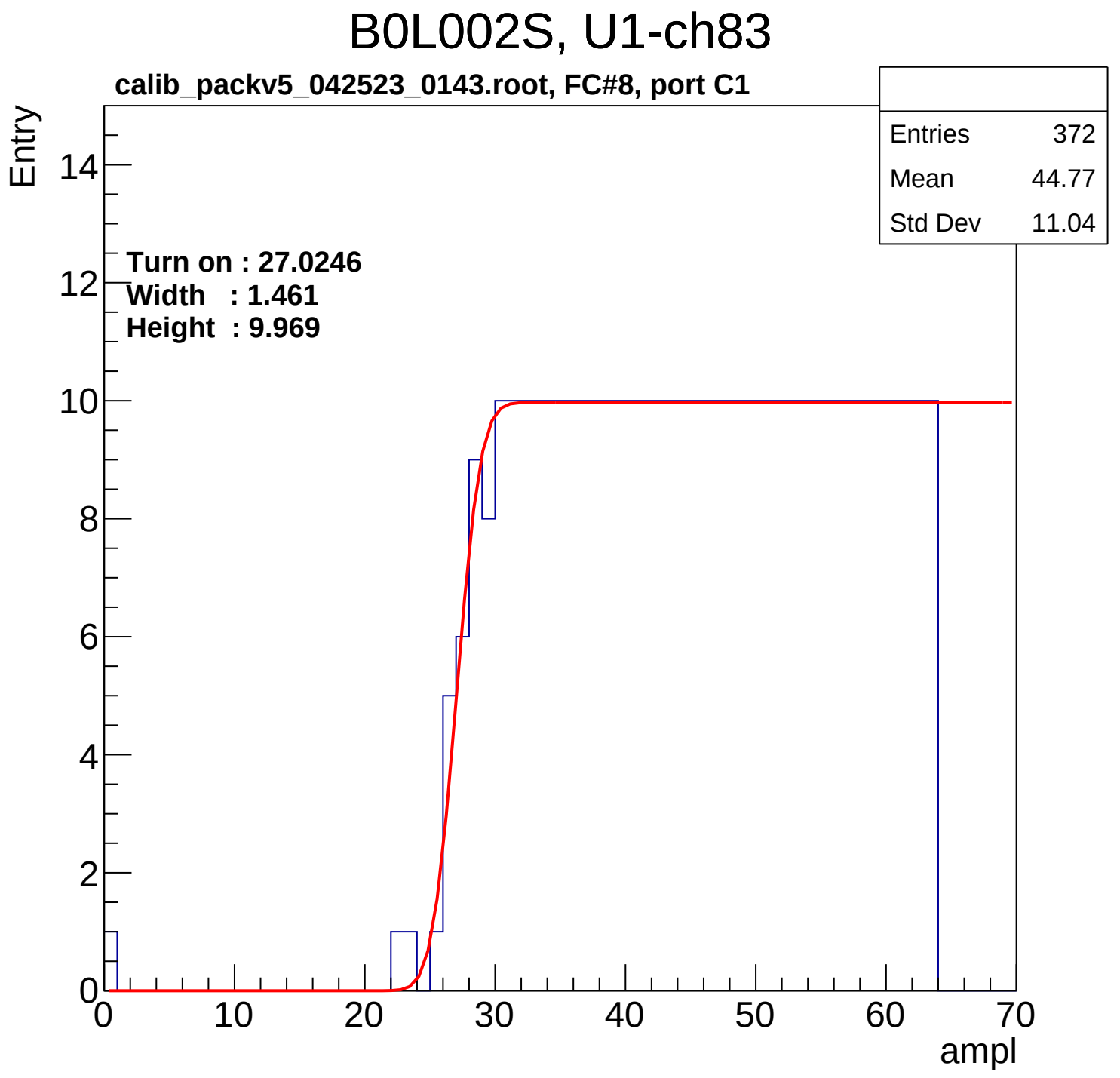
B0L002S, U1-ch83
calib_packv5_042523_0143.root, FC#8, port C1
Entries 372
Mean 44.77
Std Dev 11.04
Turn on : 27.0246
Width : 1.461
Height : 9.969
Entry
ampl
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6
8
10
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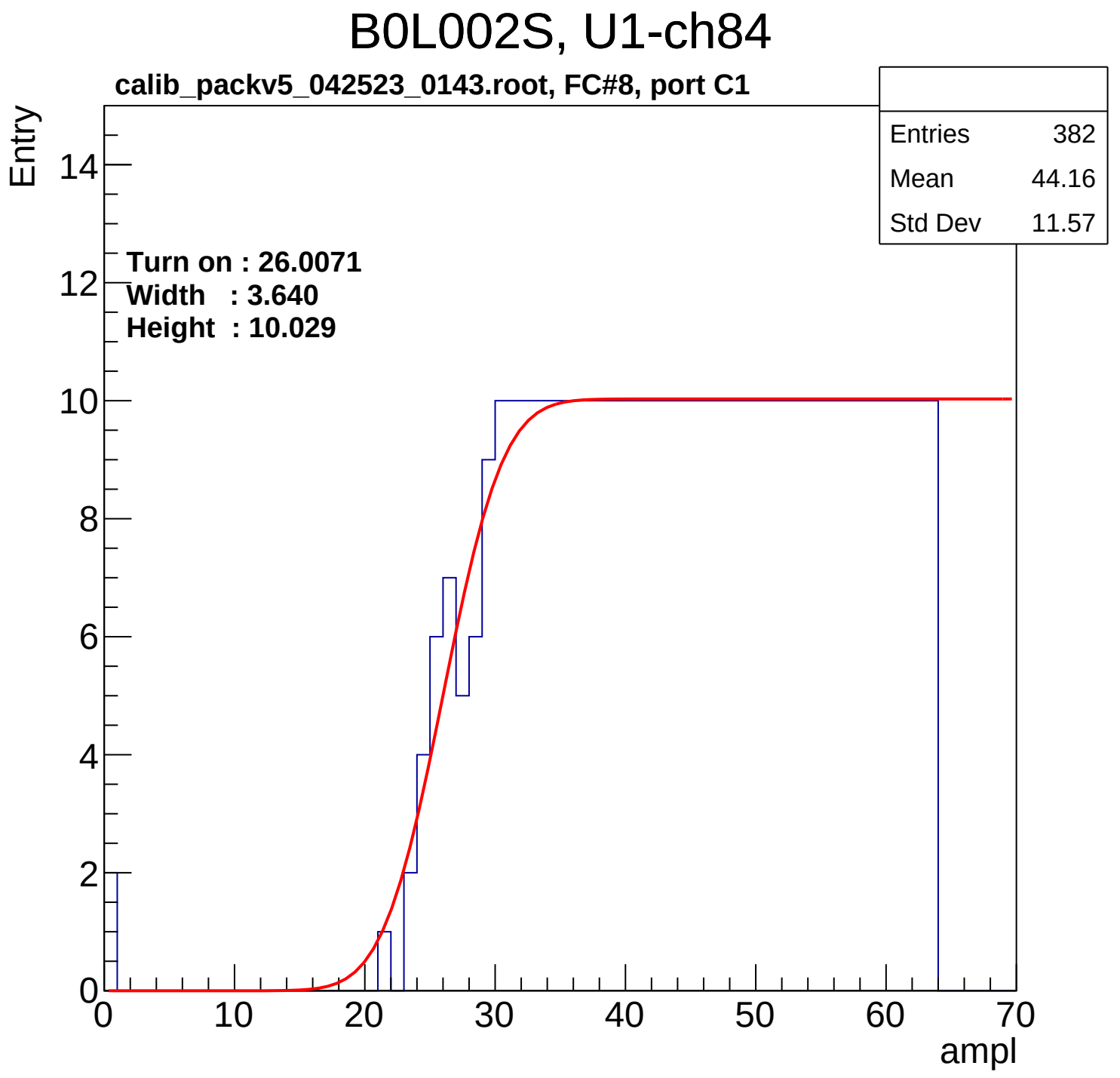
B0L002S, U1-ch84
calib_packv5_042523_0143.root, FC#8, port C1
Entries 382
Mean 44.16
Std Dev 11.57
Turn on : 26.0071
Width : 3.640
Height : 10.029
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ampl
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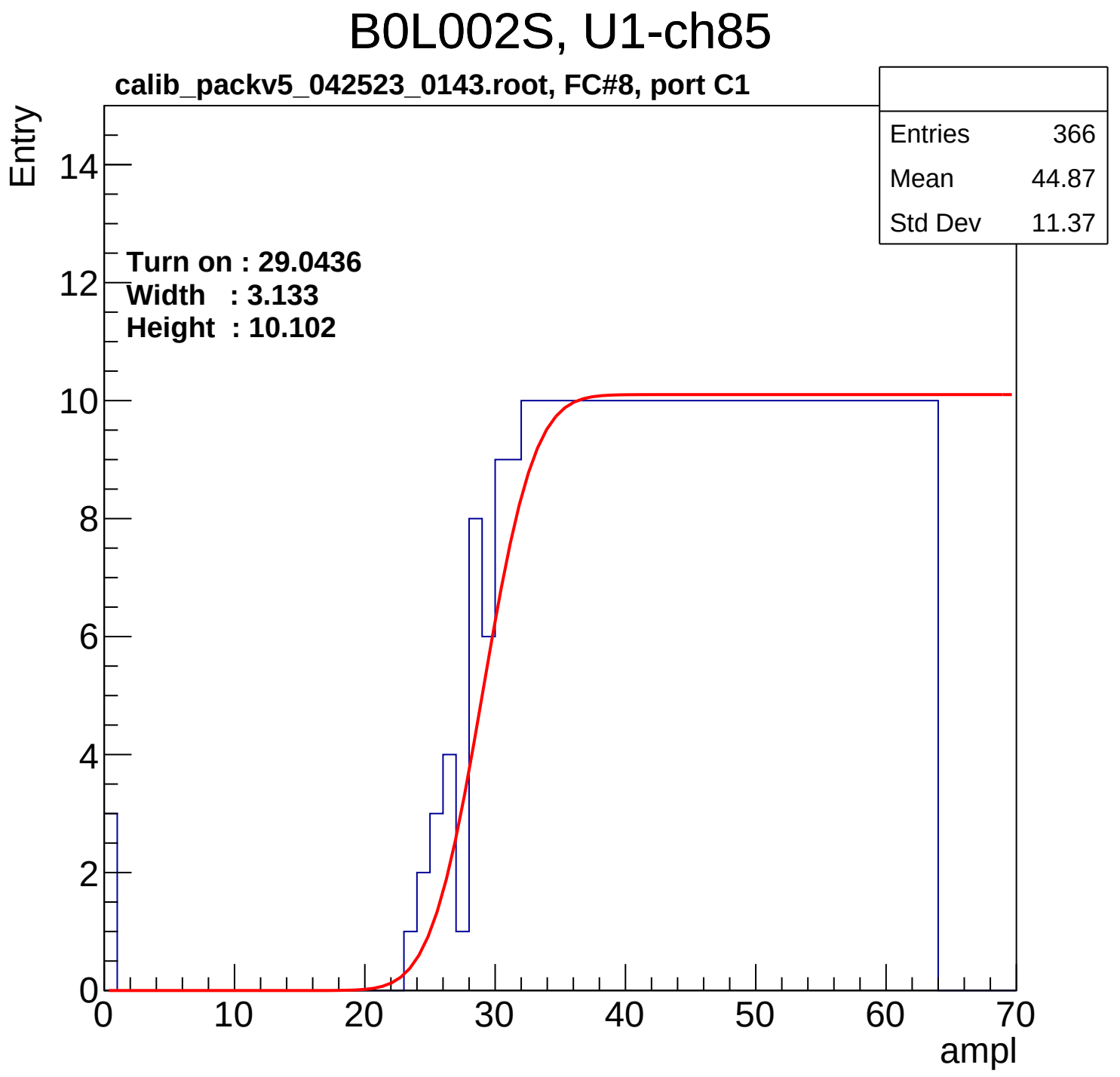
B0L002S, U1-ch85
calib_packv5_042523_0143.root, FC#8, port C1
Entries 366
Mean 44.87
Std Dev 11.37
Turn on : 29.0436
Width : 3.133
Height : 10.102
Entry
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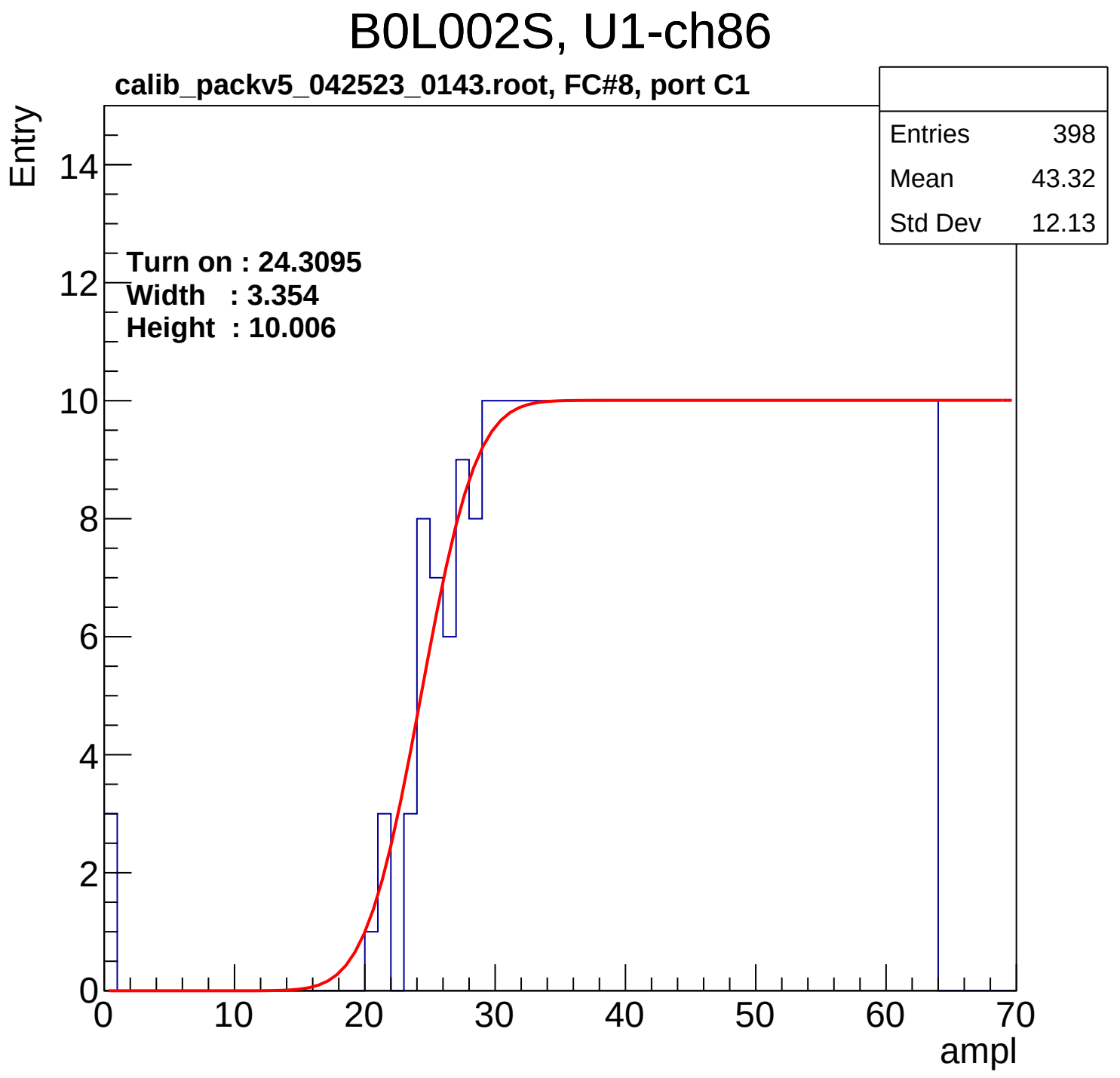
B0L002S, U1-ch86
calib_packv5_042523_0143.root, FC#8, port C1
Entries 398
Mean 43.32
Std Dev 12.13
Turn on : 24.3095
Width : 3.354
Height : 10.006
Entry
ampl
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4
6
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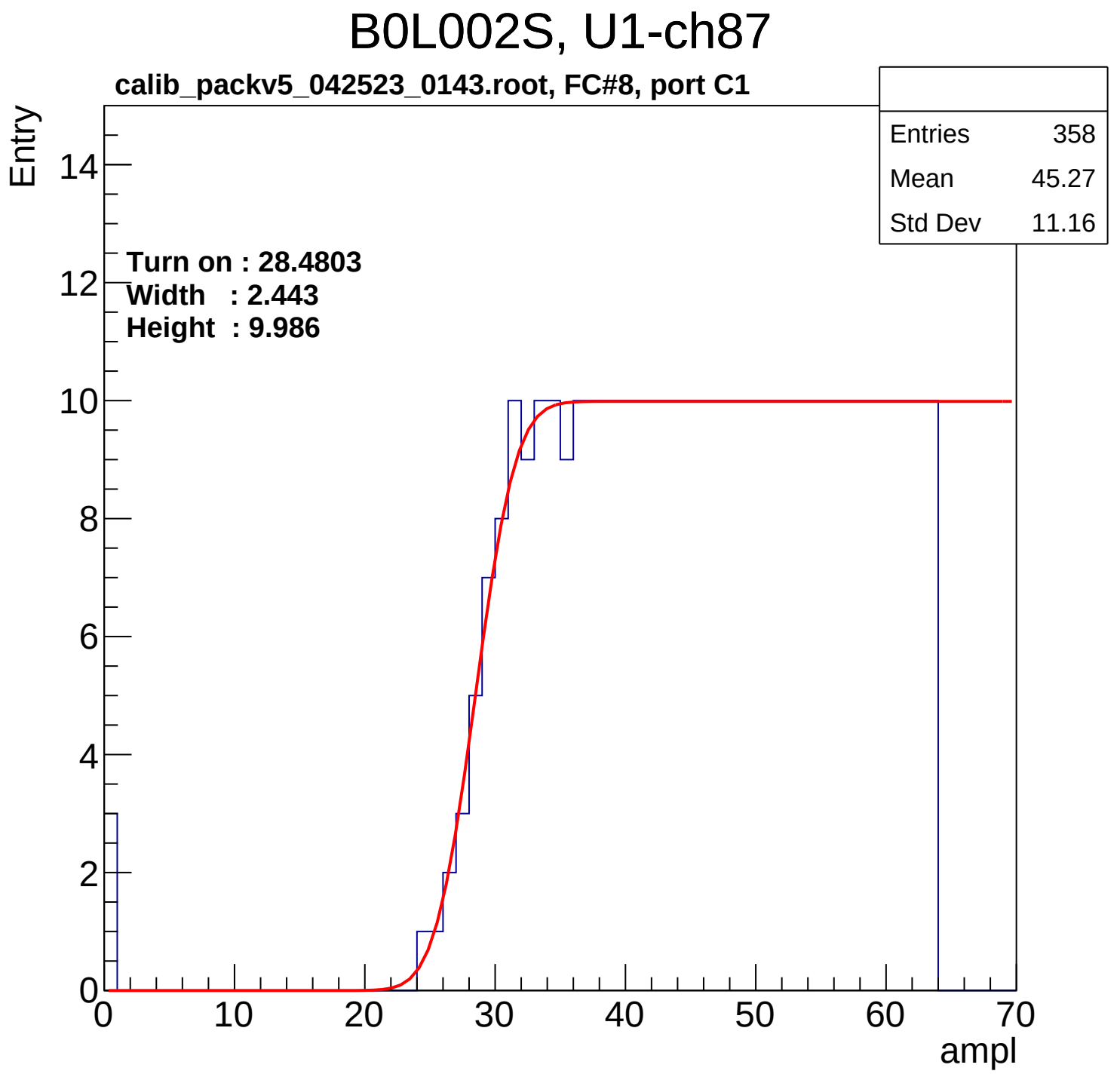
B0L002S, U1-ch87
calib_packv5_042523_0143.root, FC#8, port C1
Entries 358
Mean 45.27
Std Dev 11.16
Turn on : 28.4803
Width : 2.443
Height : 9.986
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ampl
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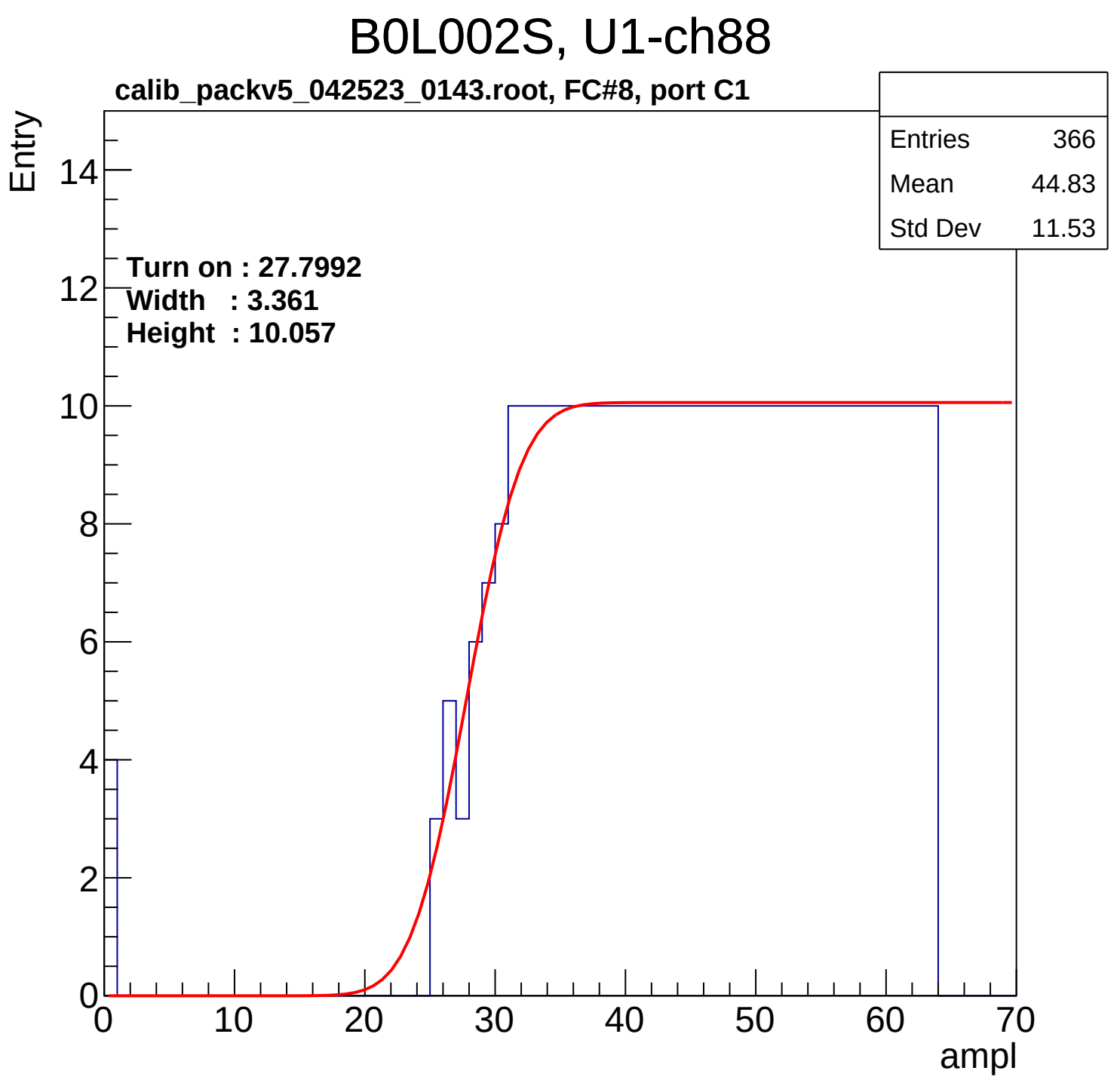
B0L002S, U1-ch88
calib_packv5_042523_0143.root, FC#8, port C1
Entries 366
Mean 44.83
Std Dev 11.53
Turn on : 27.7992
Width : 3.361
Height : 10.057
Entry
ampl
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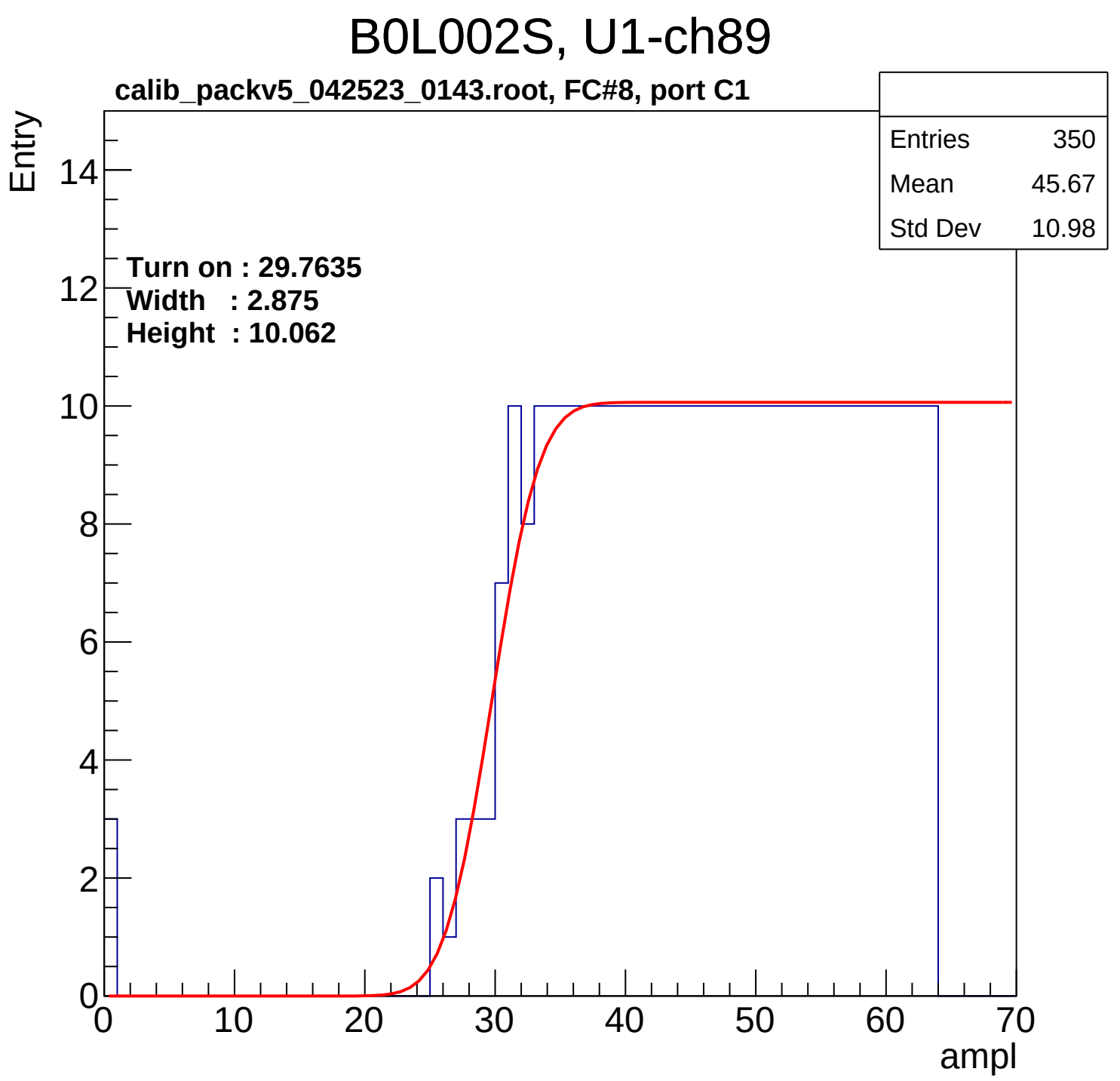
B0L002S, U1-ch89
calib_packv5_042523_0143.root, FC#8, port C1
Entries 350
Mean 45.67
Std Dev 10.98
Turn on : 29.7635
Width : 2.875
Height : 10.062
Entry
ampl
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2
4
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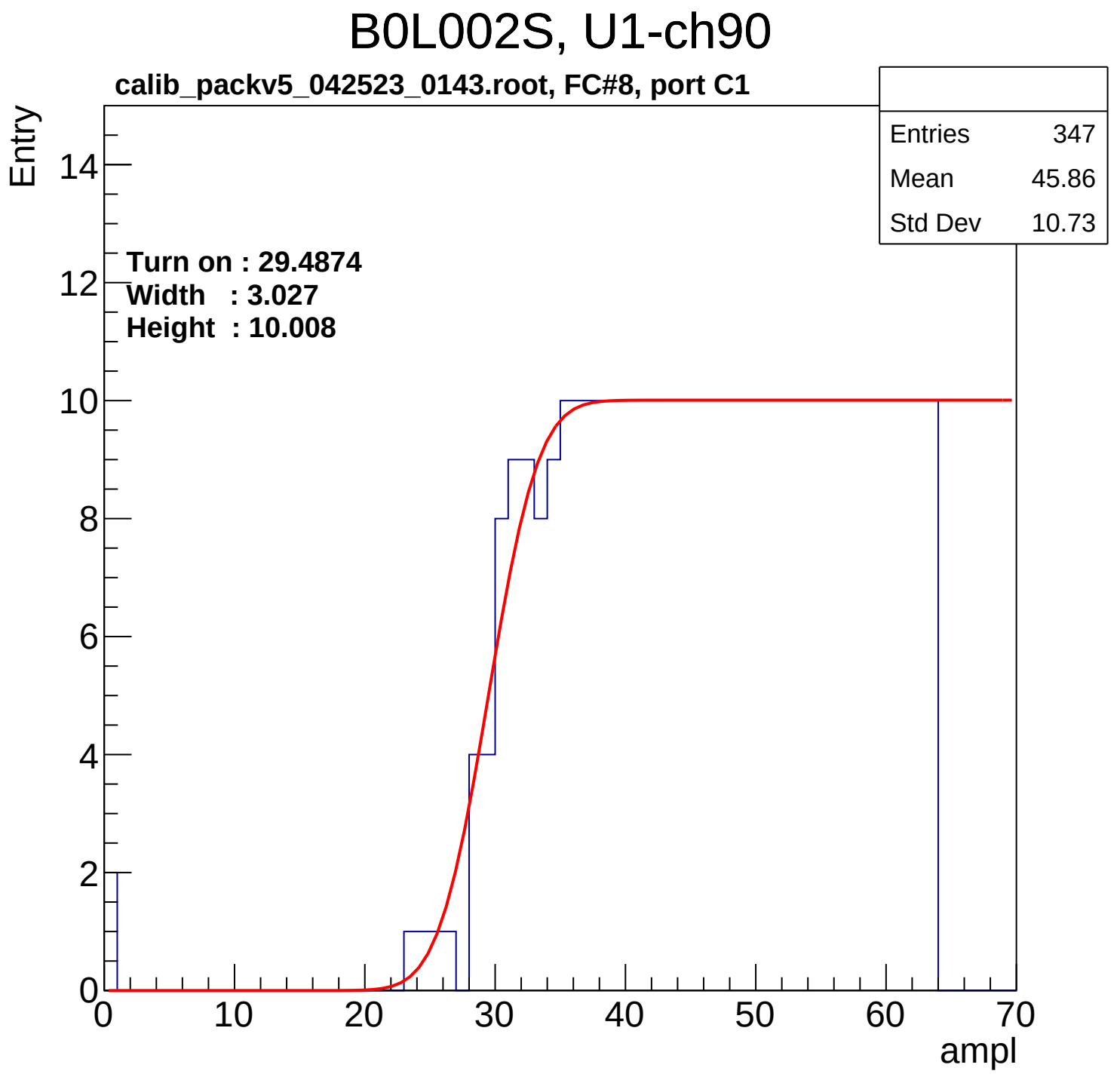
B0L002S, U1-ch90
calib_packv5_042523_0143.root, FC#8, port C1
Entries 347
Mean 45.86
Std Dev 10.73
Turn on : 29.4874
Width : 3.027
Height : 10.008
Entry
ampl
0
2
4
6
8
10
12
14
0
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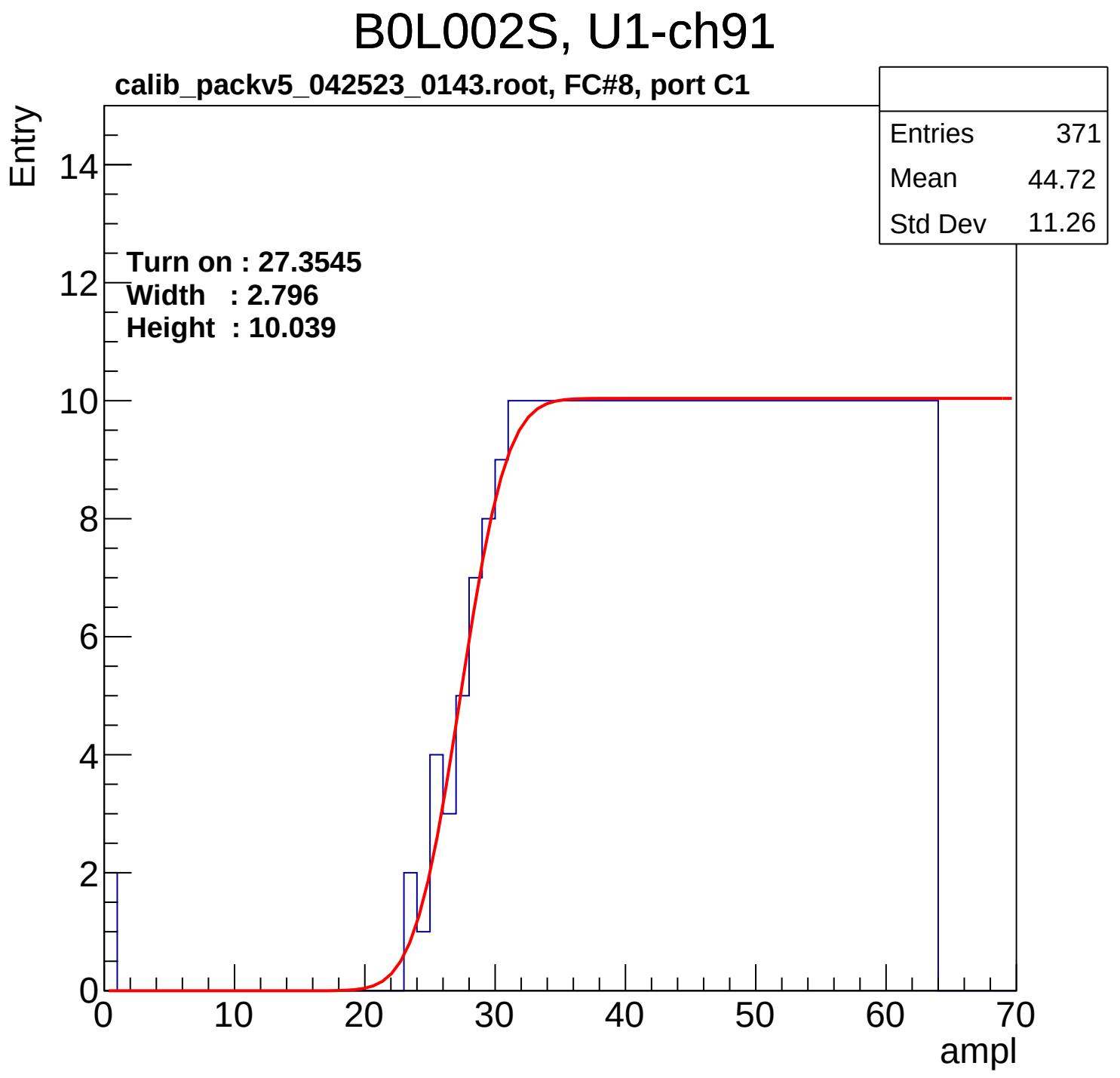
B0L002S, U1-ch91
calib_packv5_042523_0143.root, FC#8, port C1
Entries 371
Mean 44.72
Std Dev 11.26
Turn on : 27.3545
Width : 2.796
Height : 10.039
Entry
ampl
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2
4
6
8
10
12
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0
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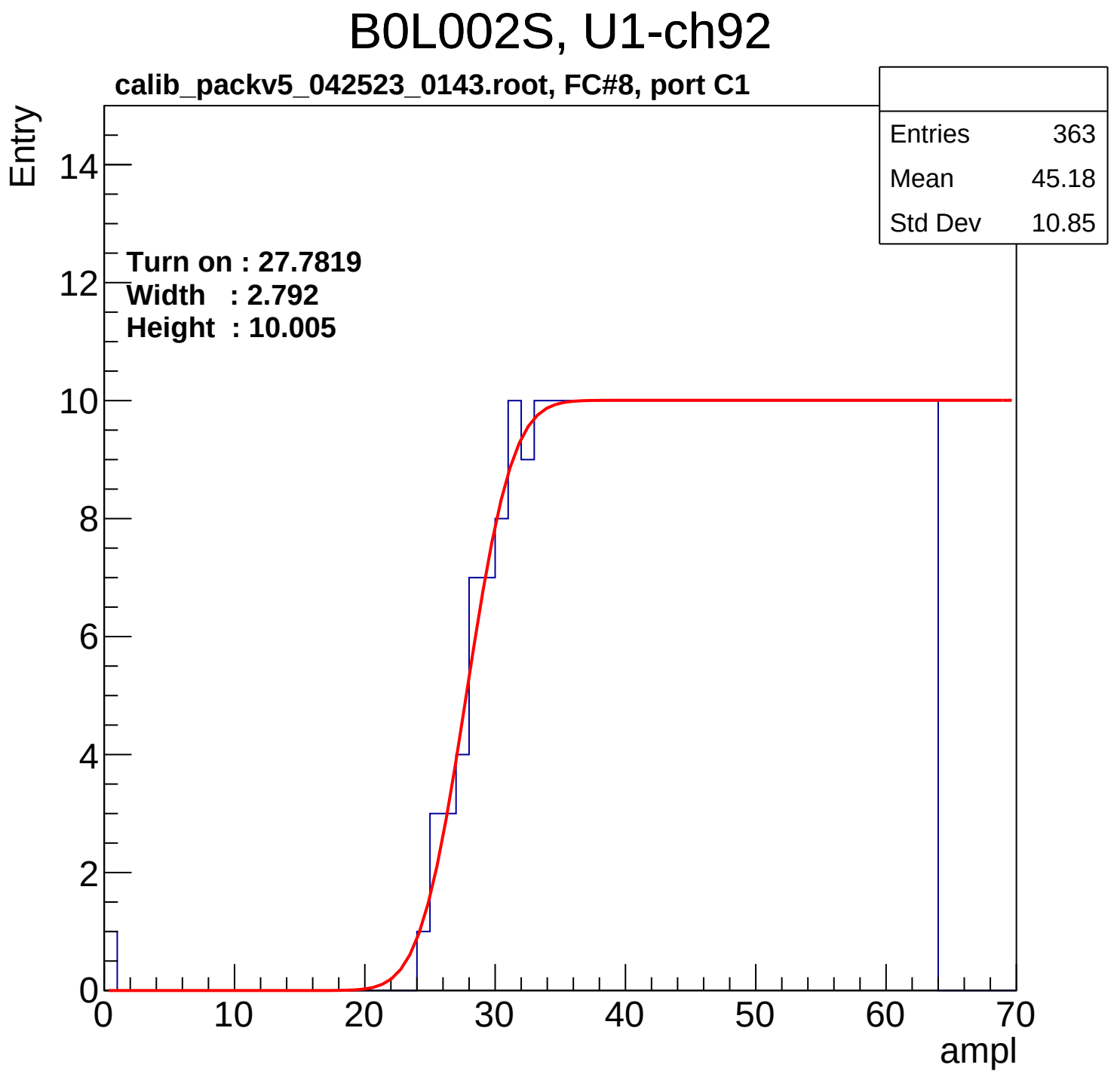
B0L002S, U1-ch92
calib_packv5_042523_0143.root, FC#8, port C1
Entries 363
Mean 45.18
Std Dev 10.85
Turn on : 27.7819
Width : 2.792
Height : 10.005
Entry
ampl
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2
4
6
8
10
12
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0
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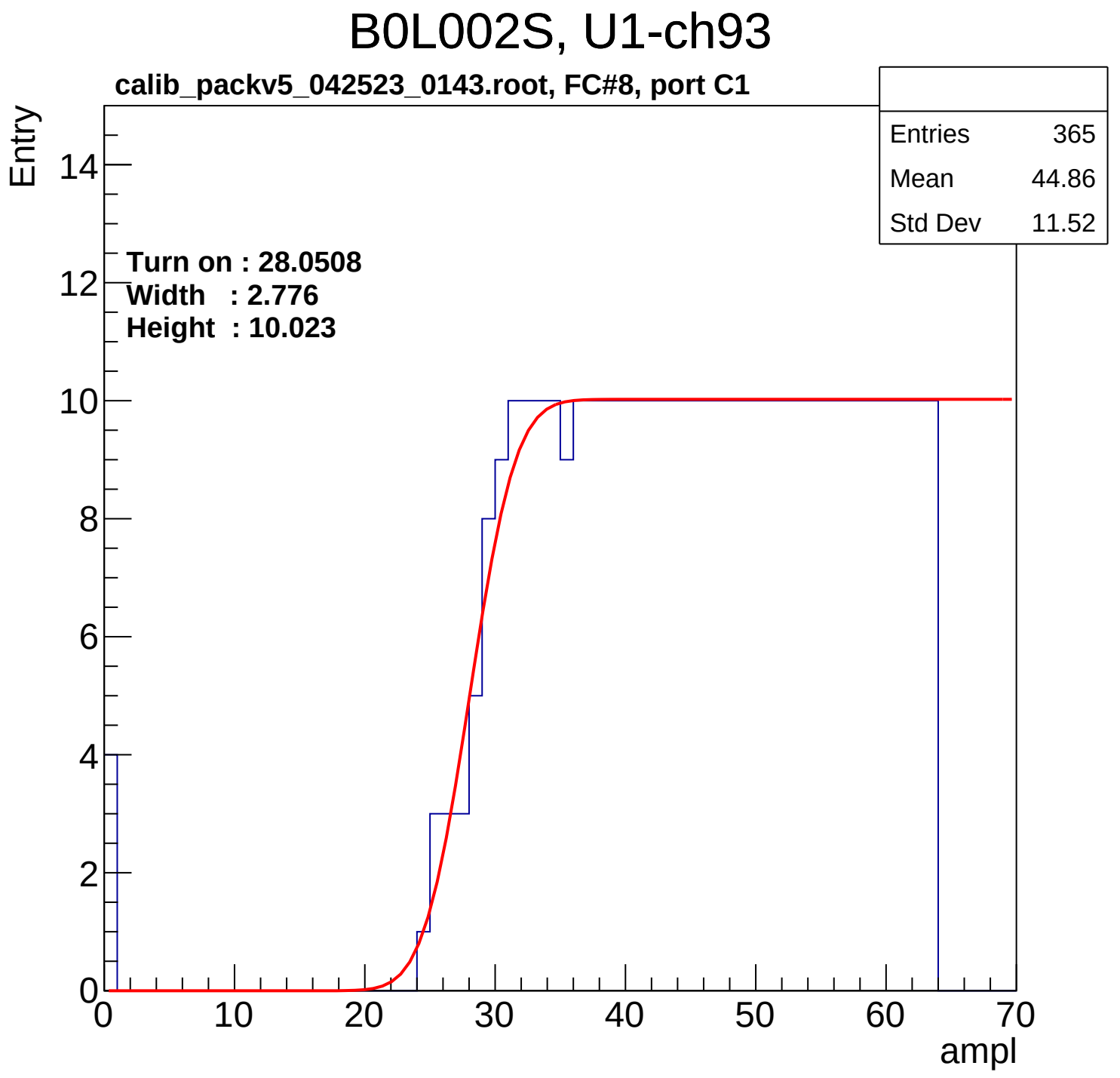
B0L002S, U1-ch93
calib_packv5_042523_0143.root, FC#8, port C1
Entries 365
Mean 44.86
Std Dev 11.52
Turn on : 28.0508
Width : 2.776
Height : 10.023
Entry
ampl
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6
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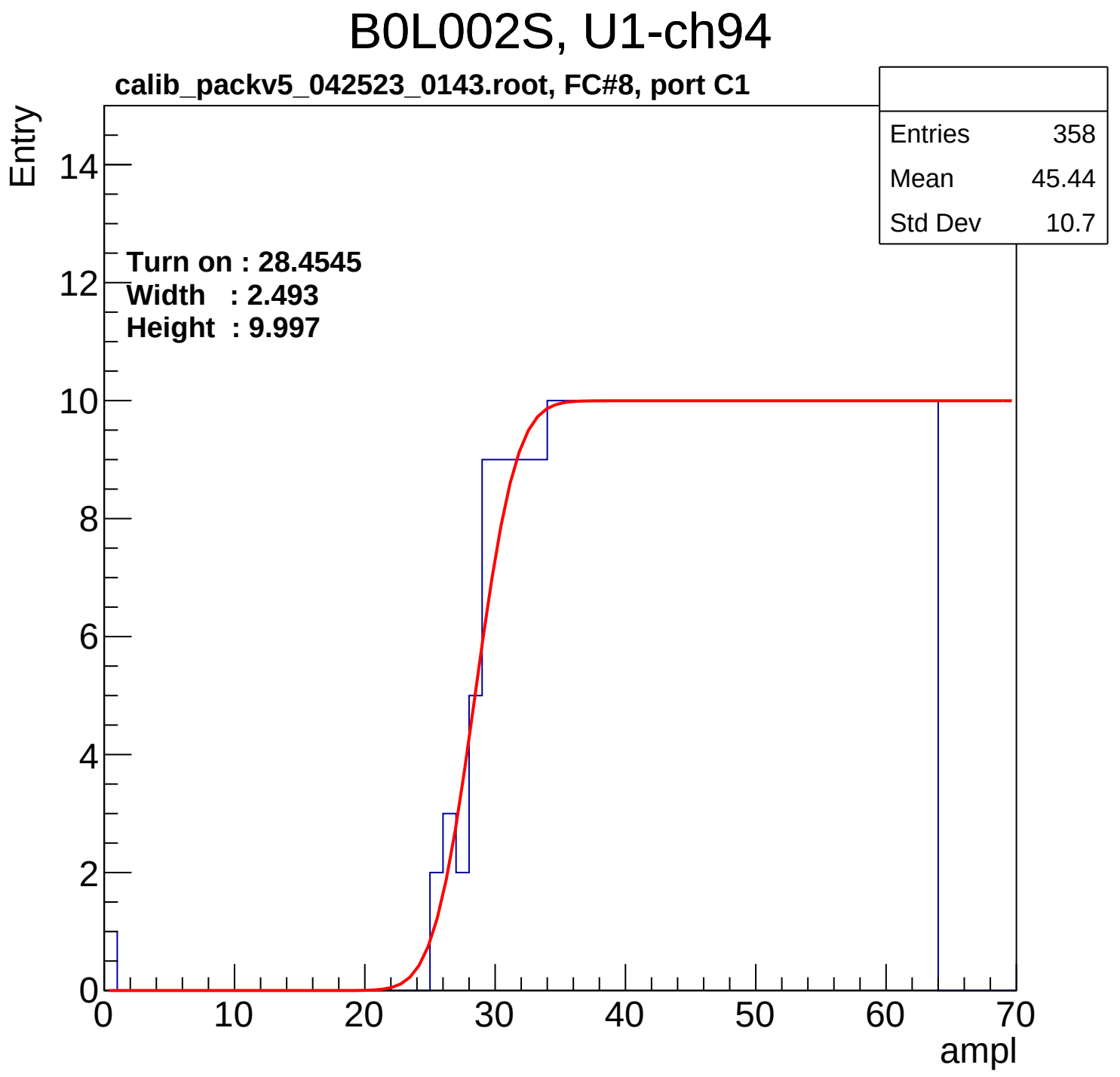
B0L002S, U1-ch94
calib_packv5_042523_0143.root, FC#8, port C1
Entries 358
Mean 45.44
Std Dev 10.7
Turn on : 28.4545
Width : 2.493
Height : 9.997
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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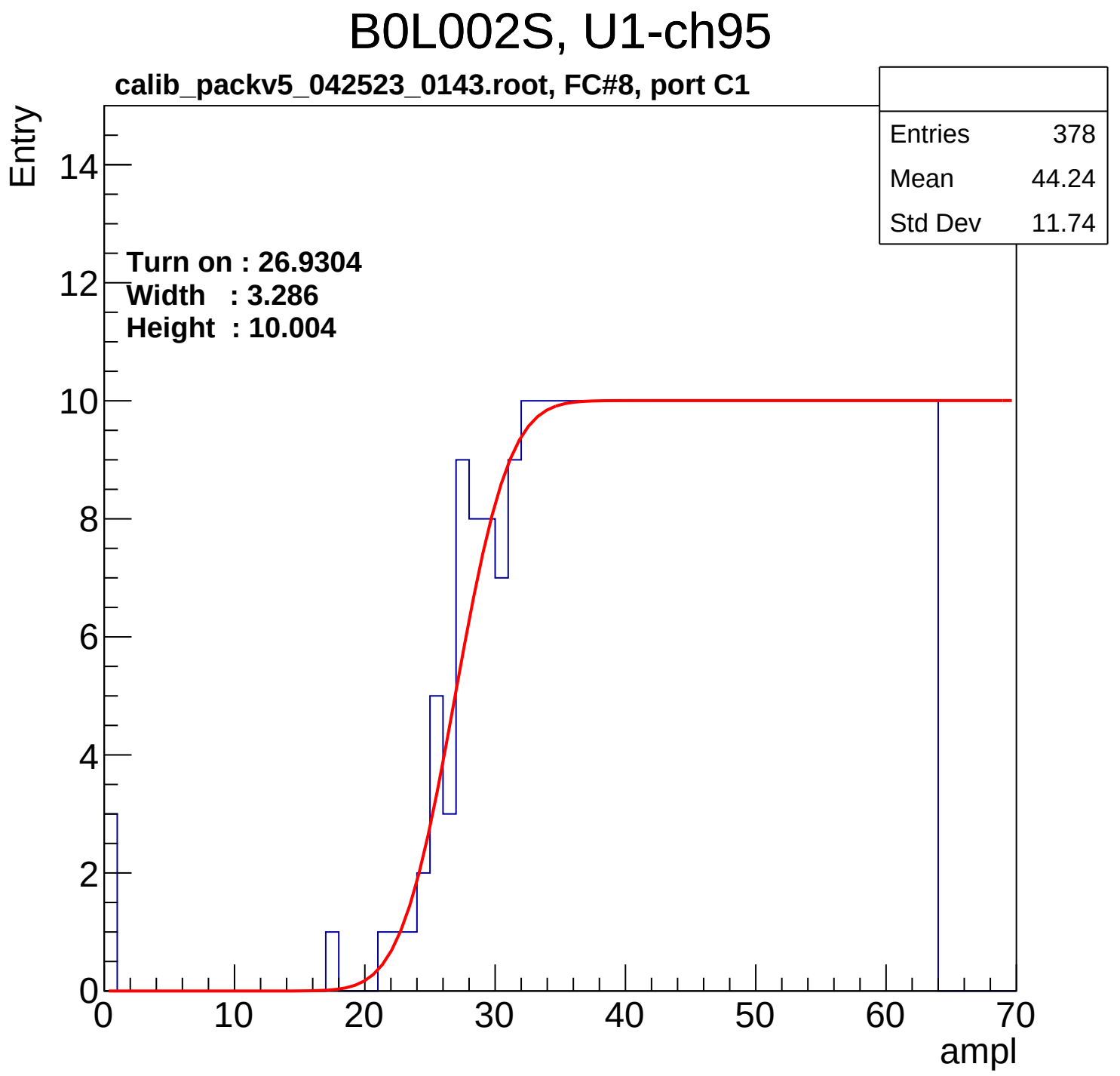
B0L002S, U1-ch95
calib_packv5_042523_0143.root, FC#8, port C1
Entries 378
Mean 44.24
Std Dev 11.74
Turn on : 26.9304
Width : 3.286
Height : 10.004
Entry
ampl
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2
4
6
8
10
12
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0
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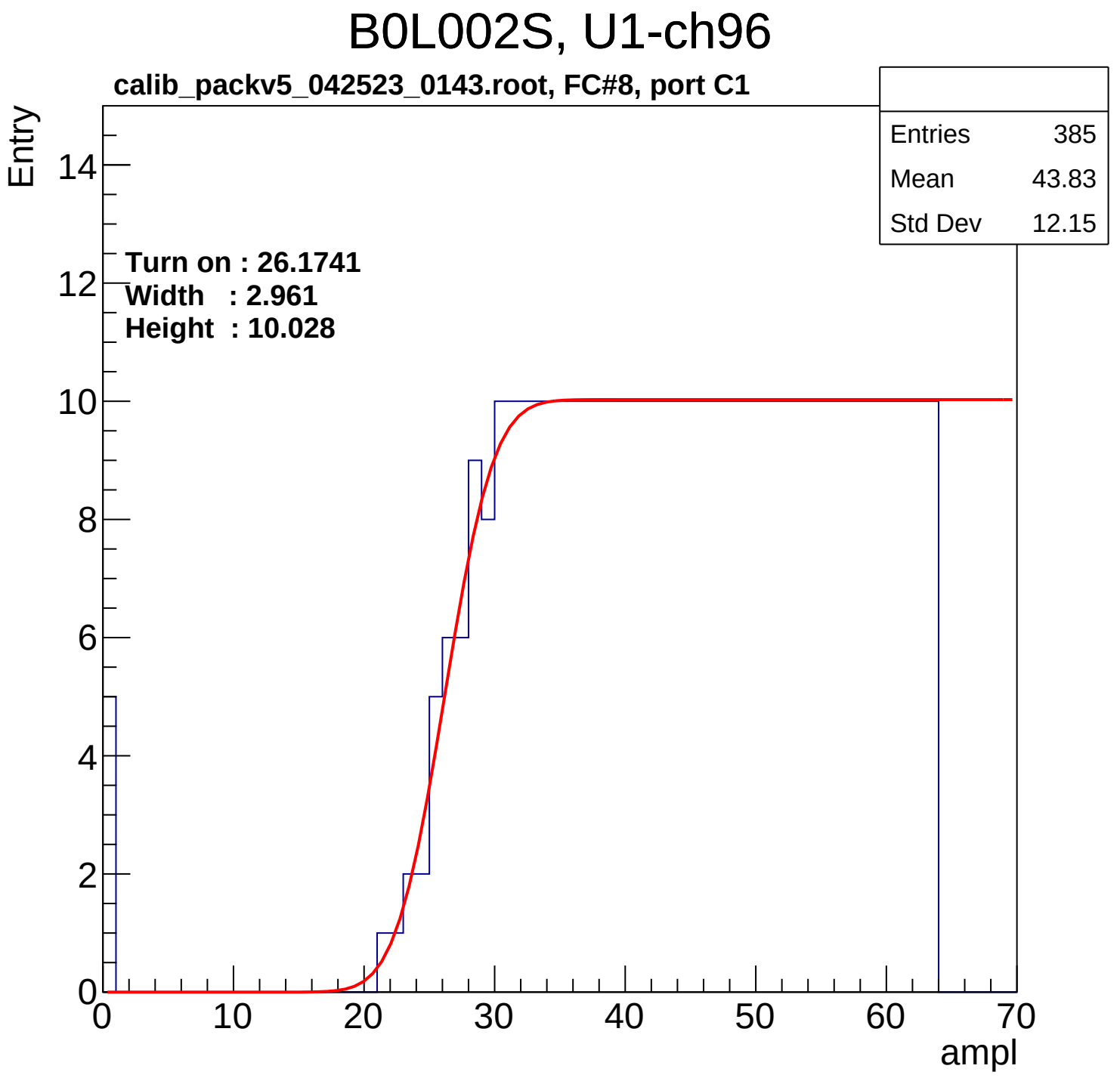
B0L002S, U1-ch96
calib_packv5_042523_0143.root, FC#8, port C1
Entries 385
Mean 43.83
Std Dev 12.15
Turn on : 26.1741
Width : 2.961
Height : 10.028
Entry
ampl
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2
4
6
8
10
12
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0
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60
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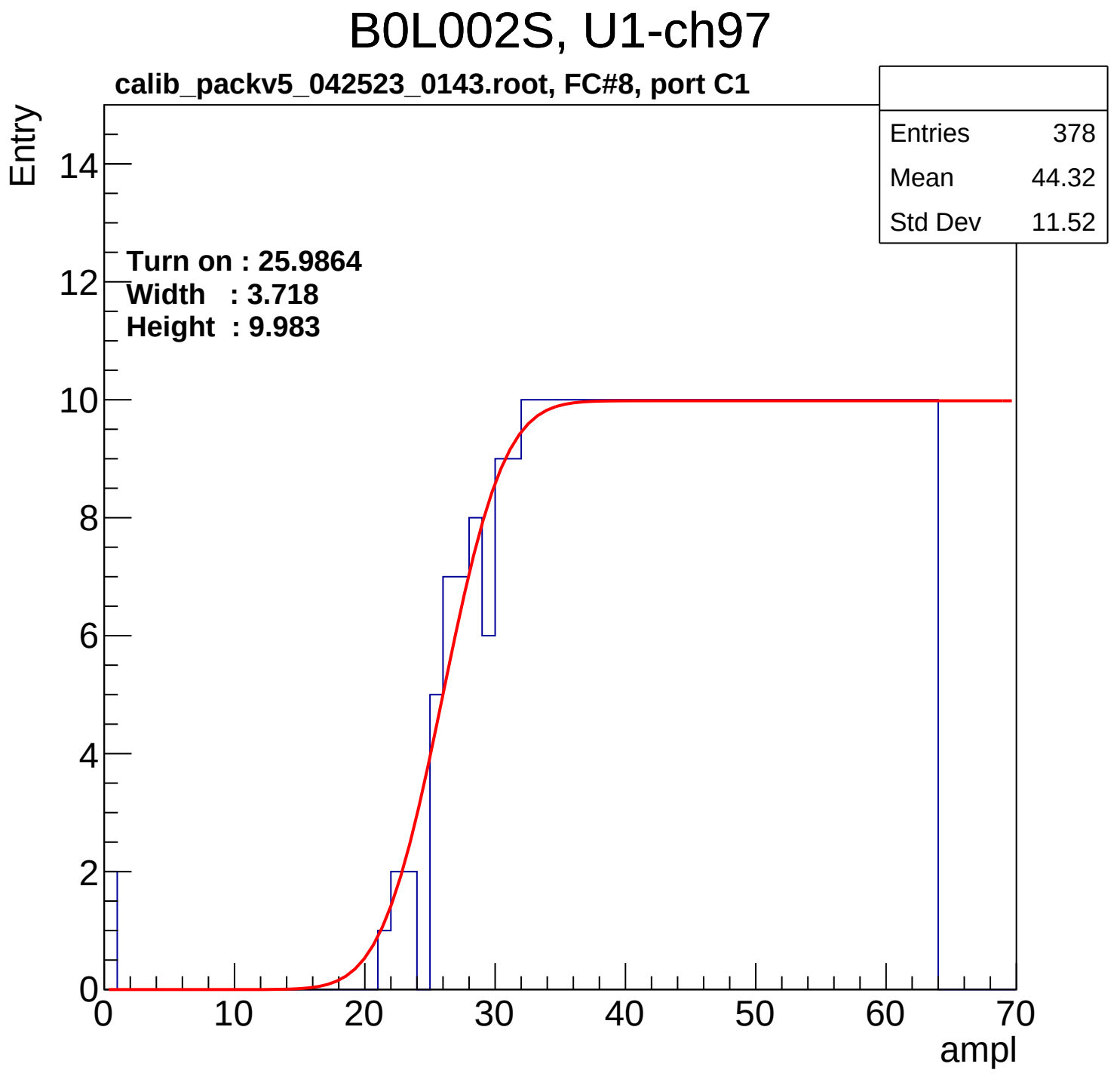
B0L002S, U1-ch97
calib_packv5_042523_0143.root, FC#8, port C1
Entries 378
Mean 44.32
Std Dev 11.52
Turn on : 25.9864
Width : 3.718
Height : 9.983
Entry
ampl
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2
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6
8
10
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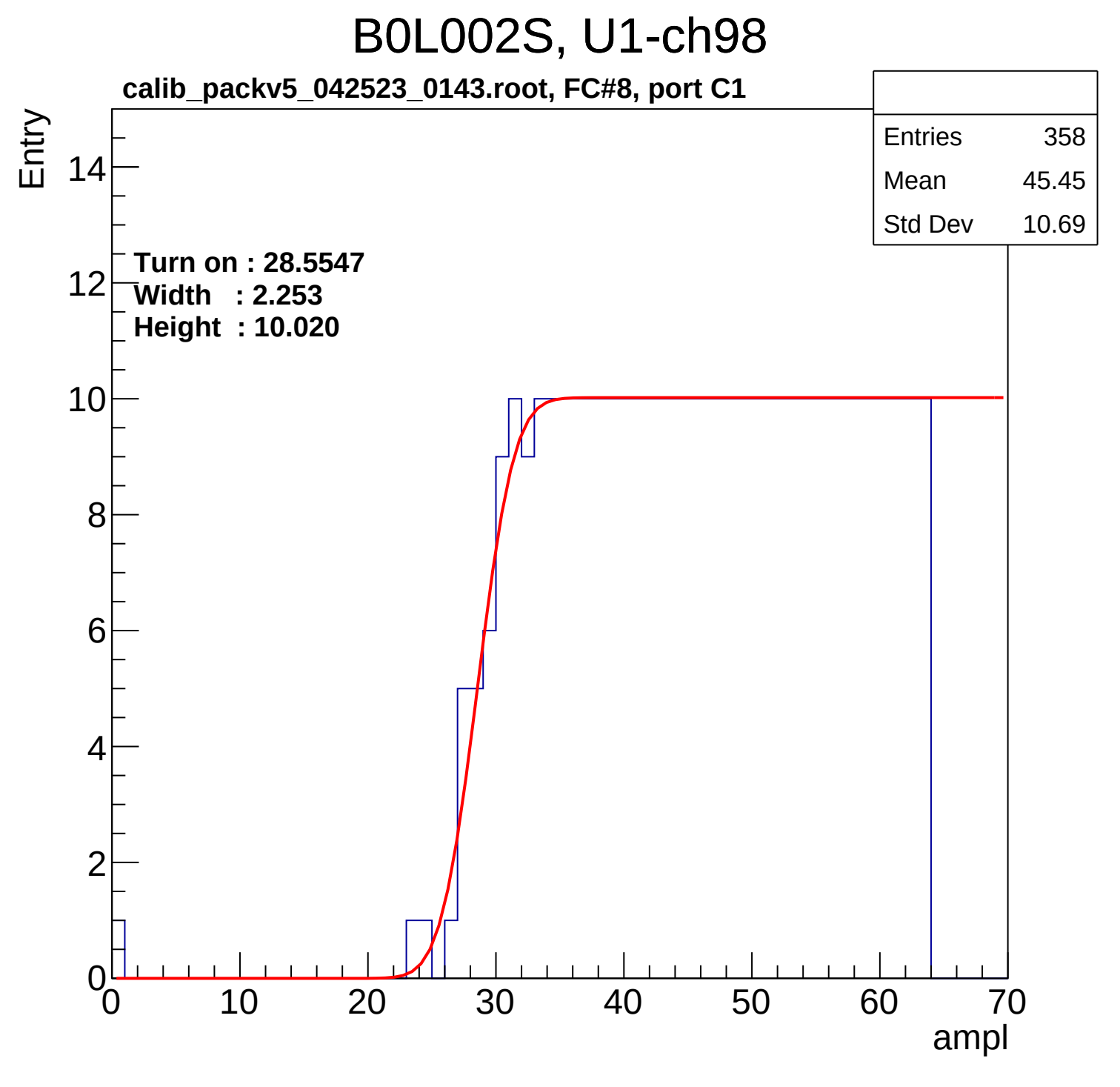
B0L002S, U1-ch98
calib_packv5_042523_0143.root, FC#8, port C1
Entries 358
Mean 45.45
Std Dev 10.69
Turn on : 28.5547
Width : 2.253
Height : 10.020
Entry
ampl
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6
8
10
12
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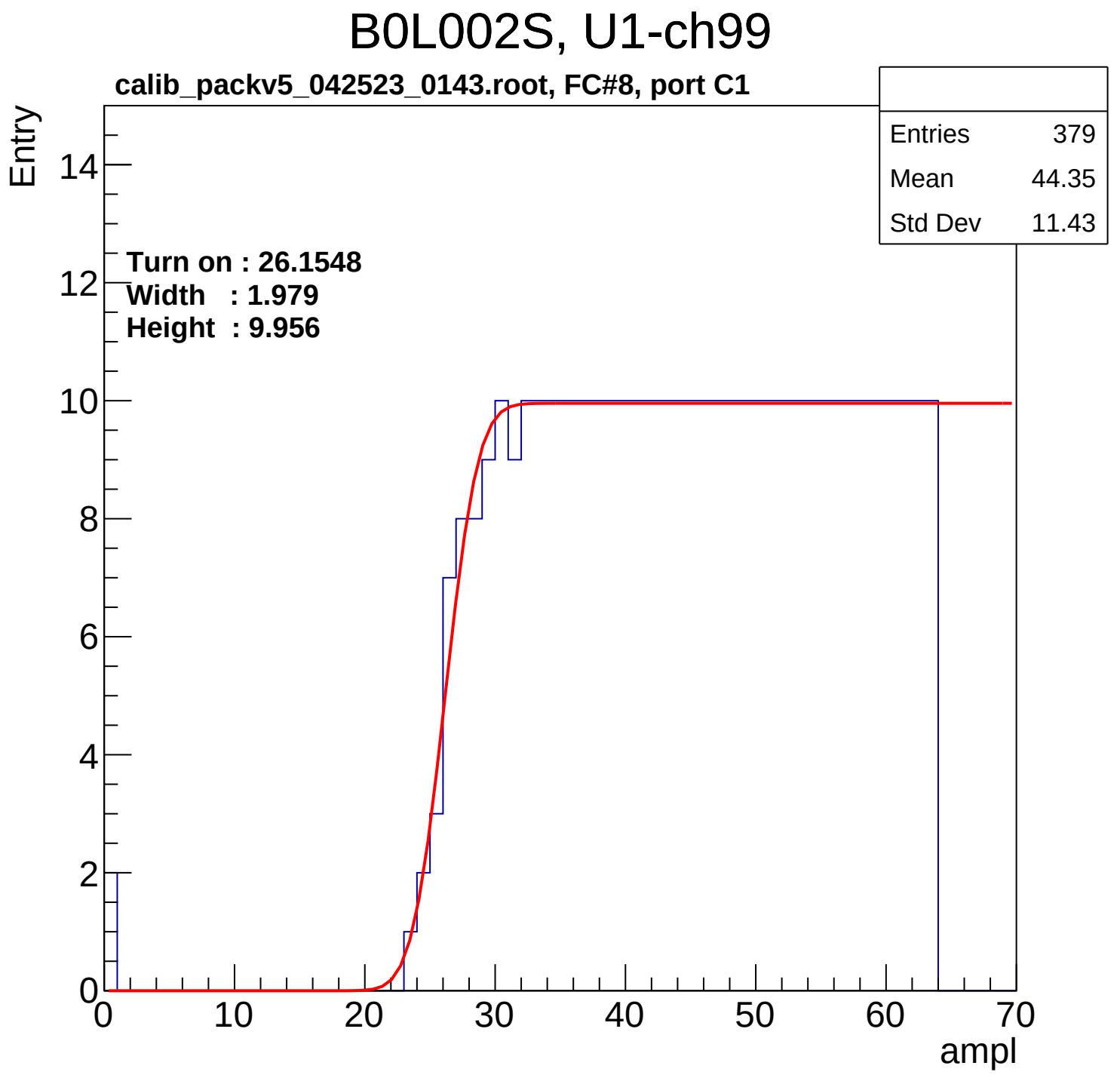
B0L002S, U1-ch99
calib_packv5_042523_0143.root, FC#8, port C1
Entries 379
Mean 44.35
Std Dev 11.43
Turn on : 26.1548
Width : 1.979
Height : 9.956
Entry
ampl
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6
8
10
12
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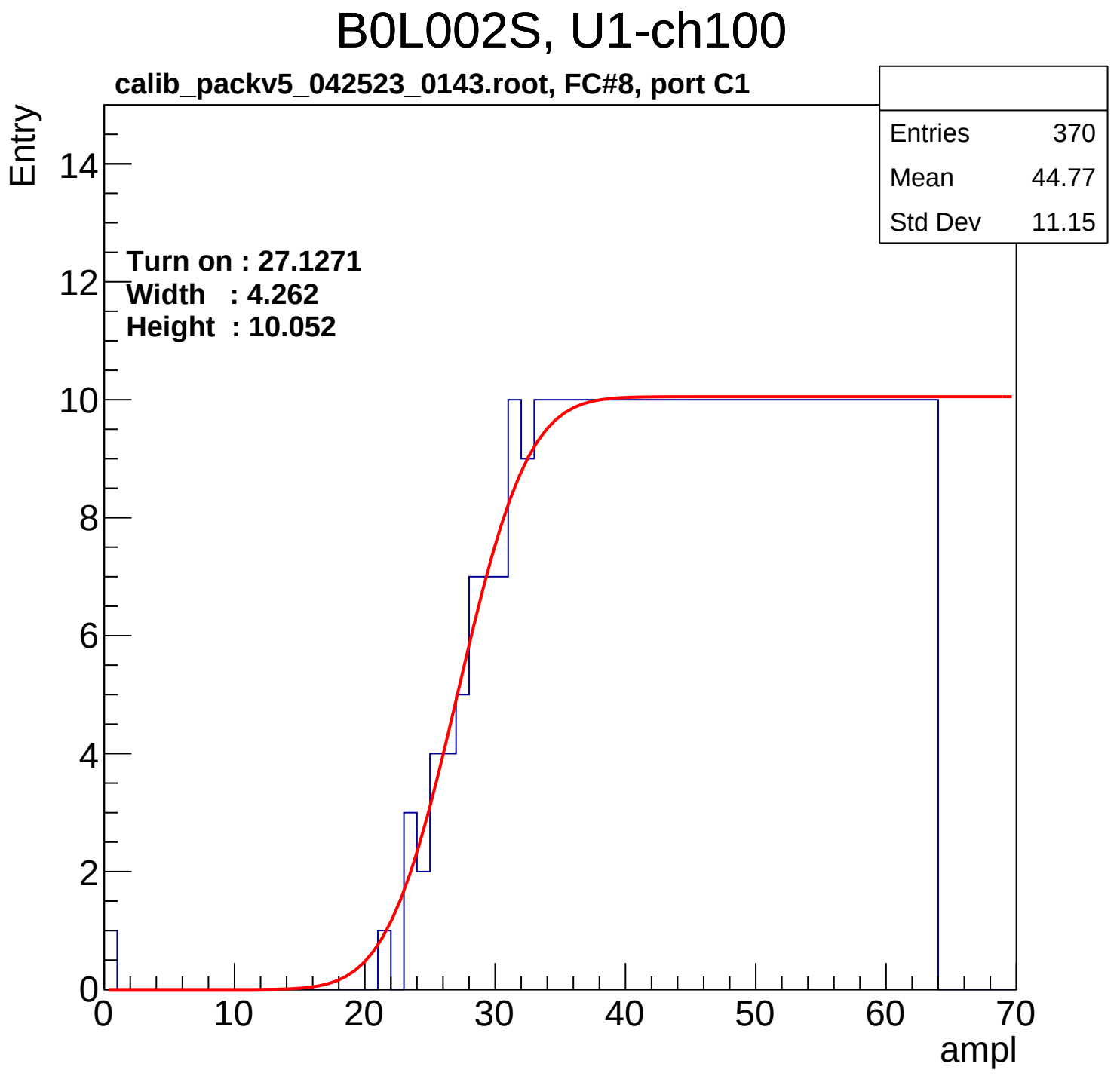
B0L002S, U1-ch100
calib_packv5_042523_0143.root, FC#8, port C1
Entries 370
Mean 44.77
Std Dev 11.15
Turn on : 27.1271
Width : 4.262
Height : 10.052
Entry
ampl
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4
6
8
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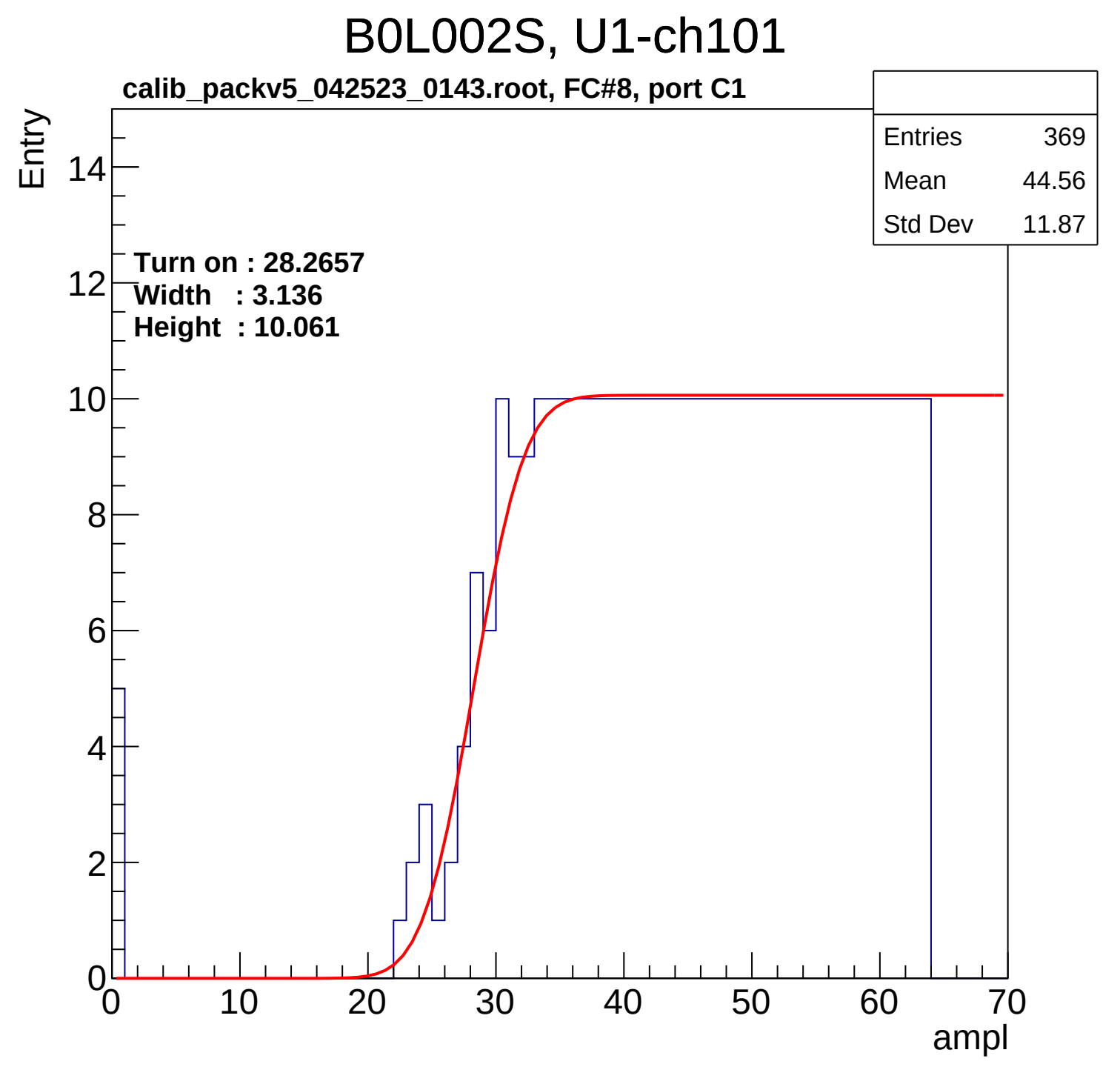
B0L002S, U1-ch101
calib_packv5_042523_0143.root, FC#8, port C1
Entries 369
Mean 44.56
Std Dev 11.87
Turn on : 28.2657
Width : 3.136
Height : 10.061
Entry
ampl
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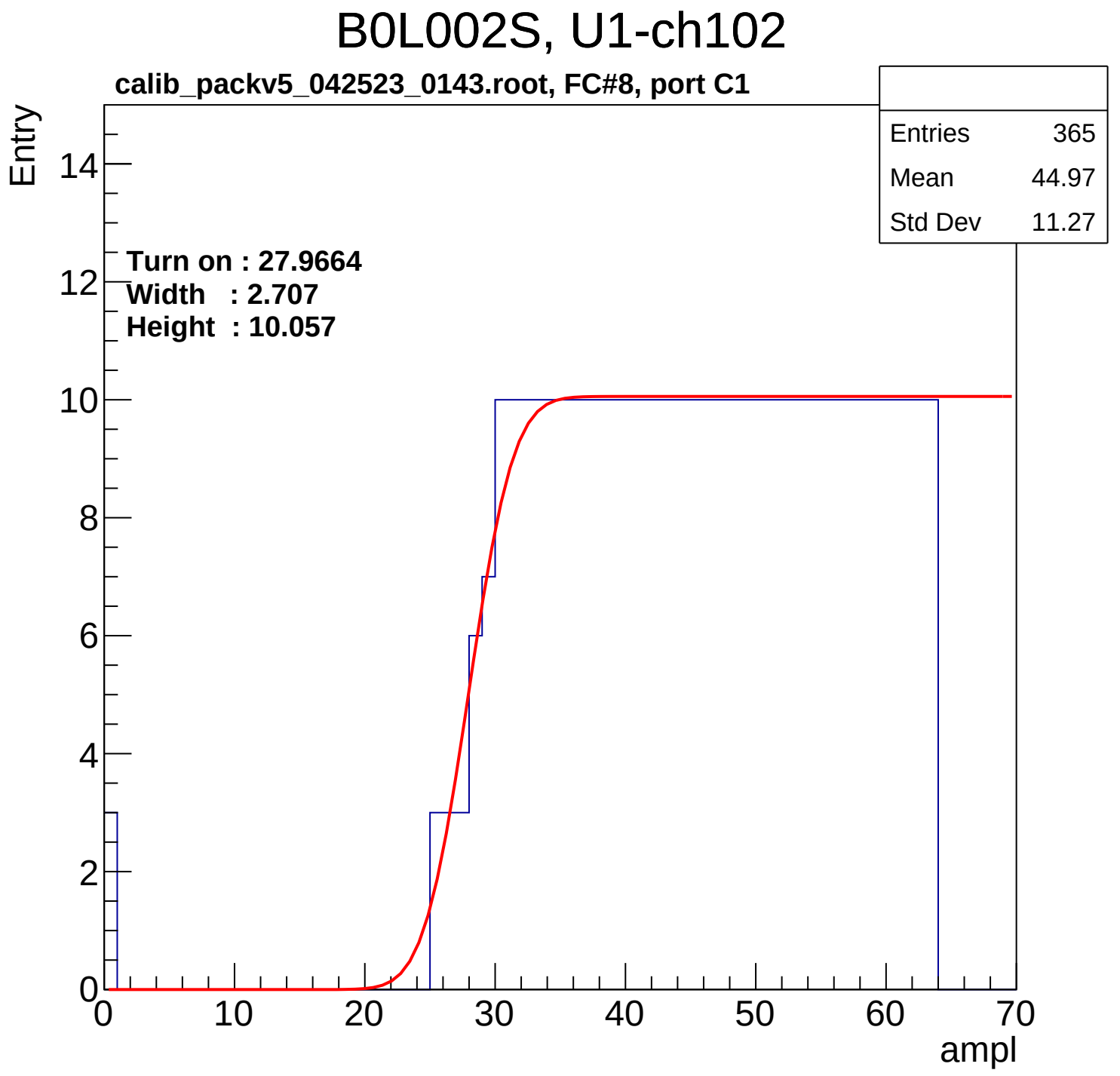
B0L002S, U1-ch102
calib_packv5_042523_0143.root, FC#8, port C1
Entries 365
Mean 44.97
Std Dev 11.27
Turn on : 27.9664
Width : 2.707
Height : 10.057
Entry
ampl
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10
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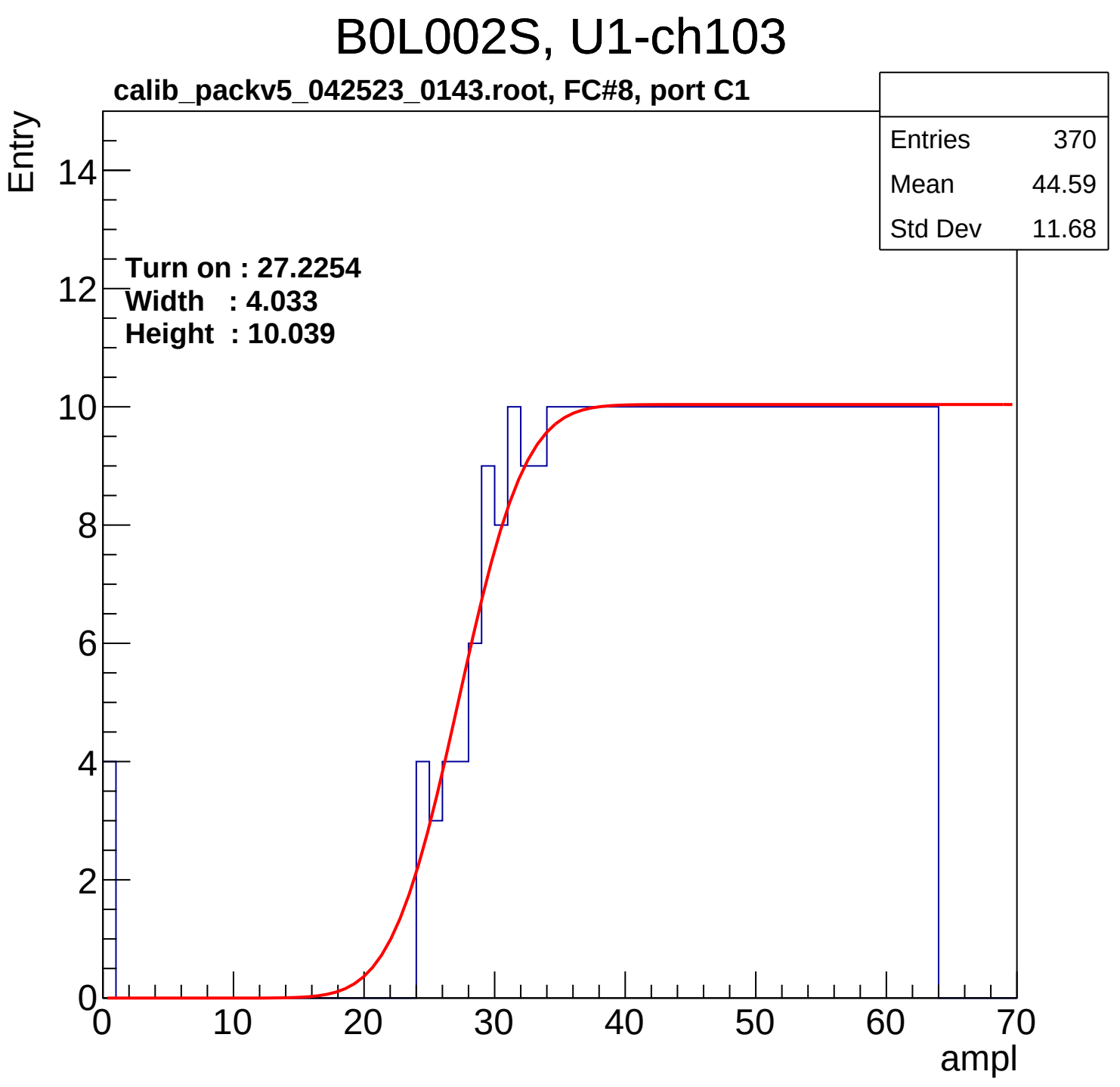
B0L002S, U1-ch103
calib_packv5_042523_0143.root, FC#8, port C1
Entries 370
Mean 44.59
Std Dev 11.68
Turn on : 27.2254
Width : 4.033
Height : 10.039
Entry
ampl
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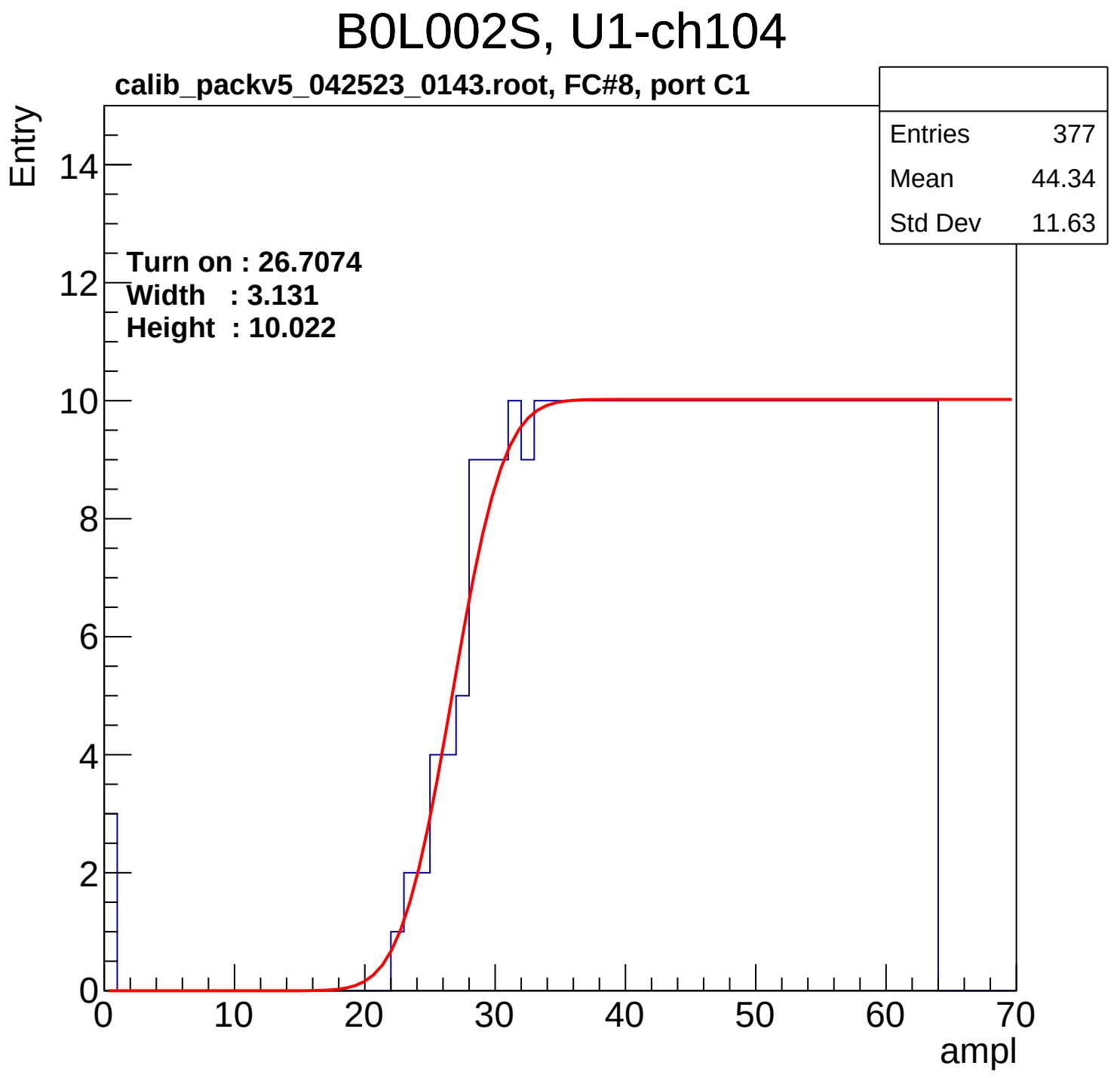
B0L002S, U1-ch104
calib_packv5_042523_0143.root, FC#8, port C1
Entries 377
Mean 44.34
Std Dev 11.63
Turn on : 26.7074
Width : 3.131
Height : 10.022
Entry
ampl
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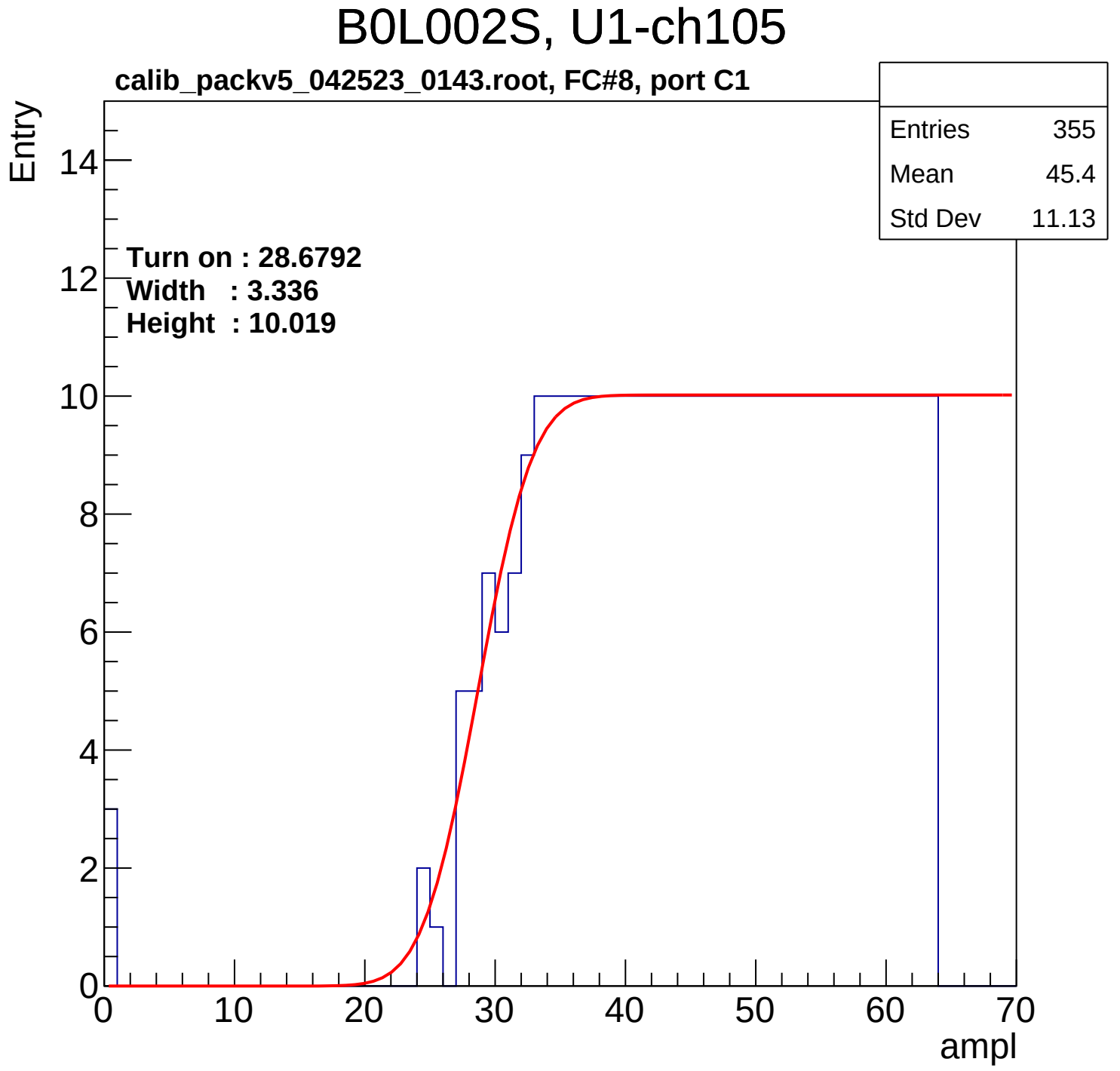
B0L002S, U1-ch105
calib_packv5_042523_0143.root, FC#8, port C1
Entries 355
Mean 45.4
Std Dev 11.13
Turn on : 28.6792
Width : 3.336
Height : 10.019
Entry
ampl
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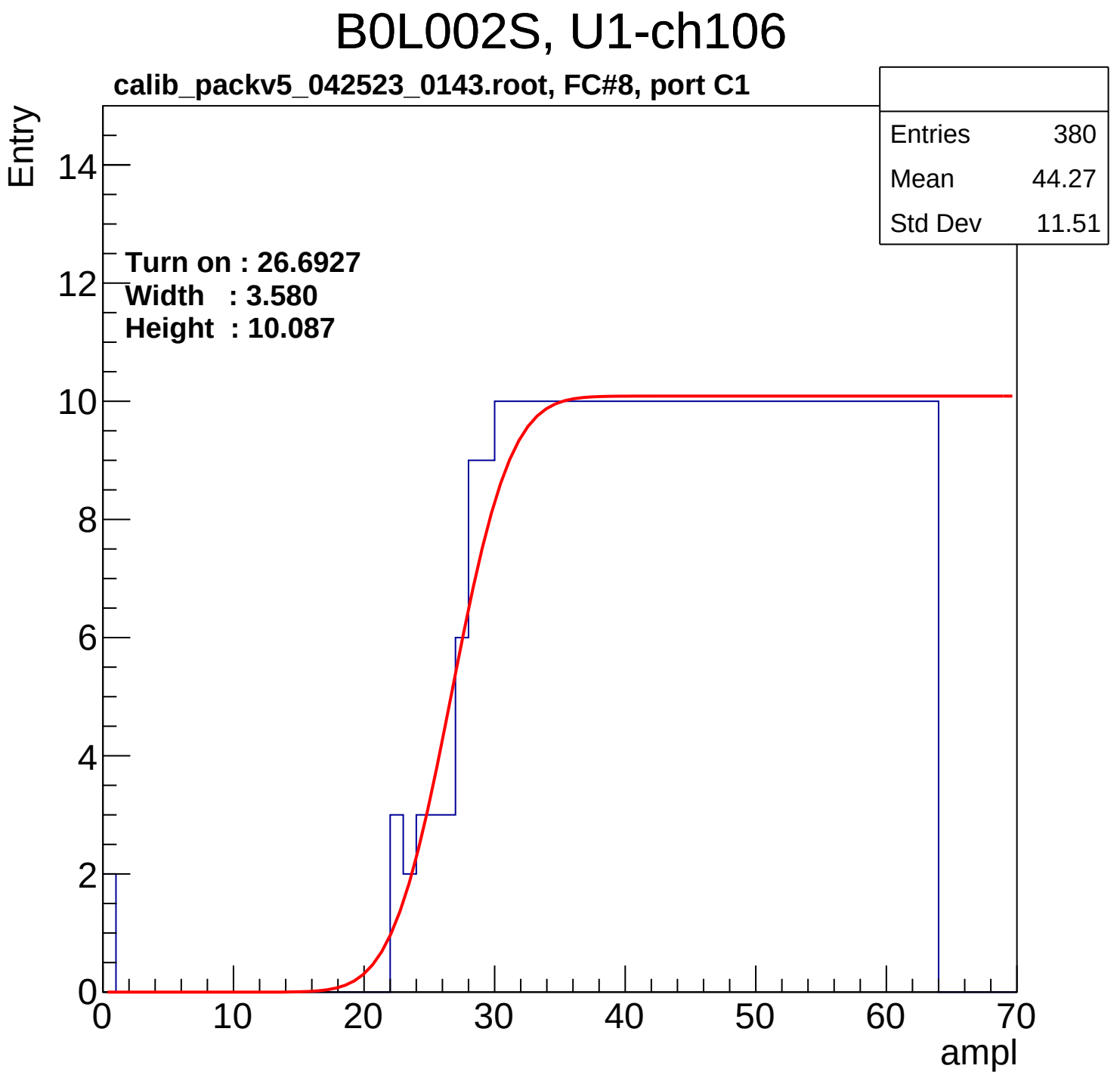
B0L002S, U1-ch106
calib_packv5_042523_0143.root, FC#8, port C1
Entries 380
Mean 44.27
Std Dev 11.51
Turn on : 26.6927
Width : 3.580
Height : 10.087
Entry
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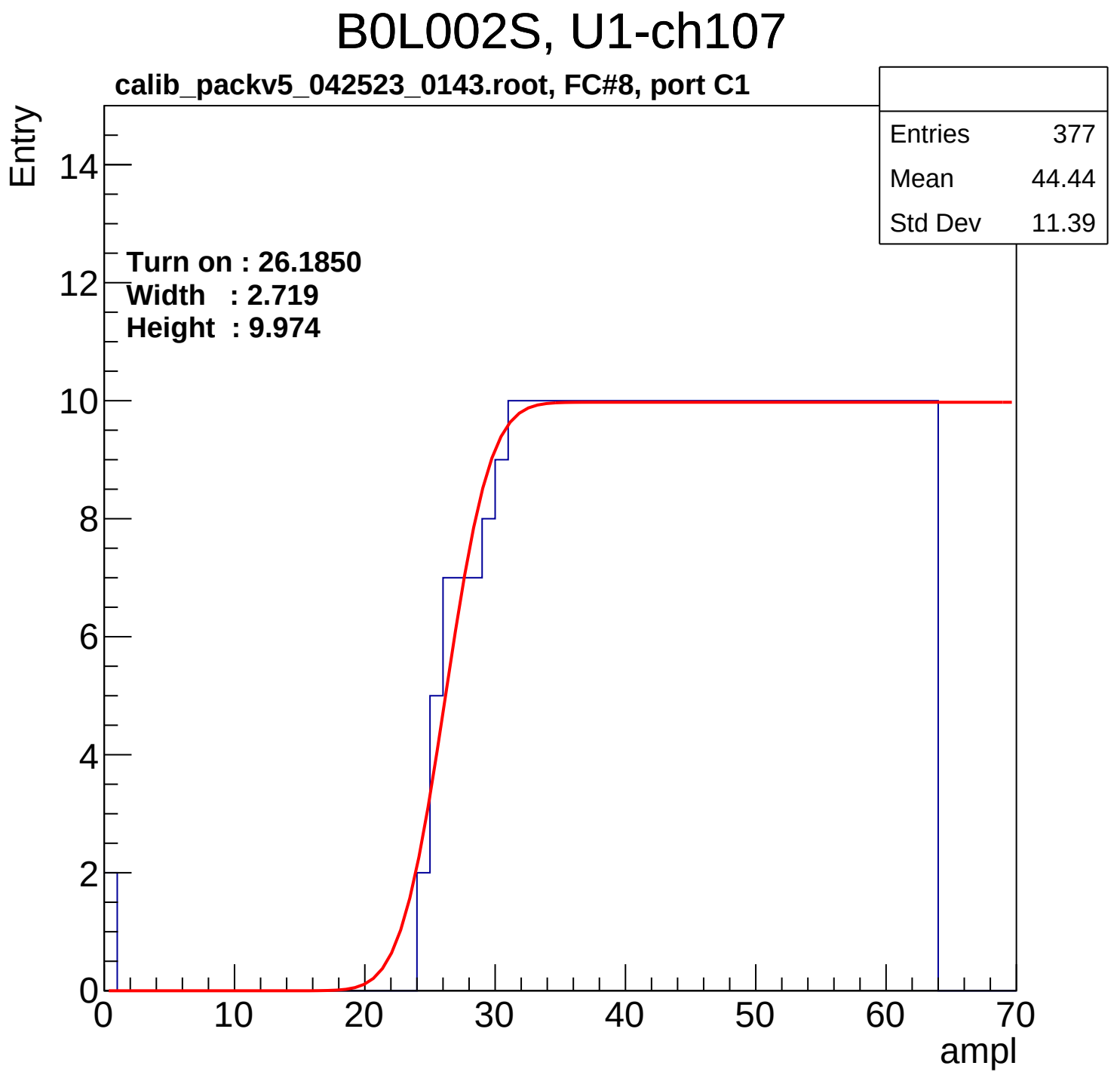
B0L002S, U1-ch107
calib_packv5_042523_0143.root, FC#8, port C1
Entries 377
Mean 44.44
Std Dev 11.39
Turn on : 26.1850
Width : 2.719
Height : 9.974
Entry
ampl
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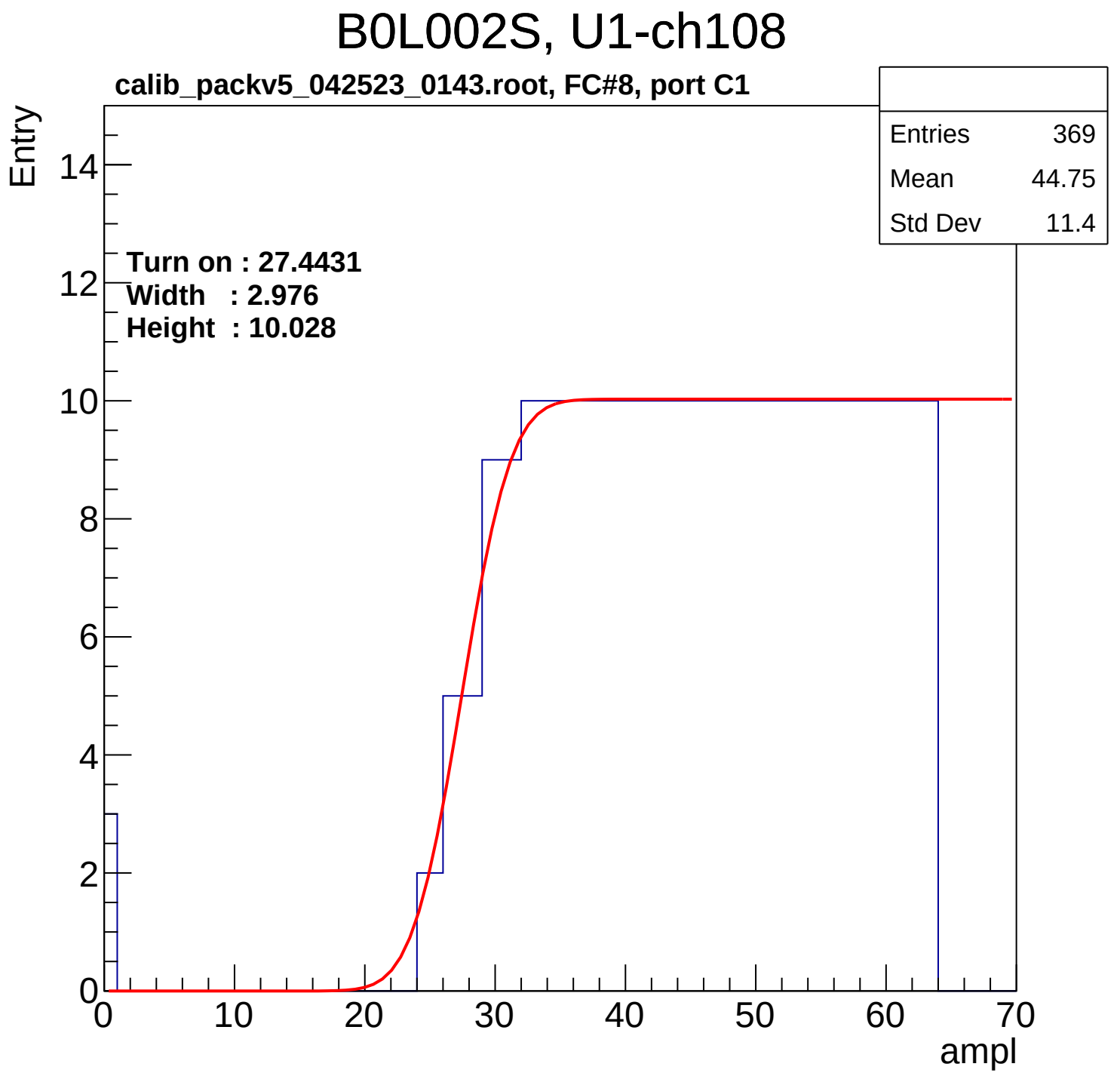
B0L002S, U1-ch108
calib_packv5_042523_0143.root, FC#8, port C1
Entries 369
Mean 44.75
Std Dev 11.4
Turn on : 27.4431
Width : 2.976
Height : 10.028
Entry
ampl
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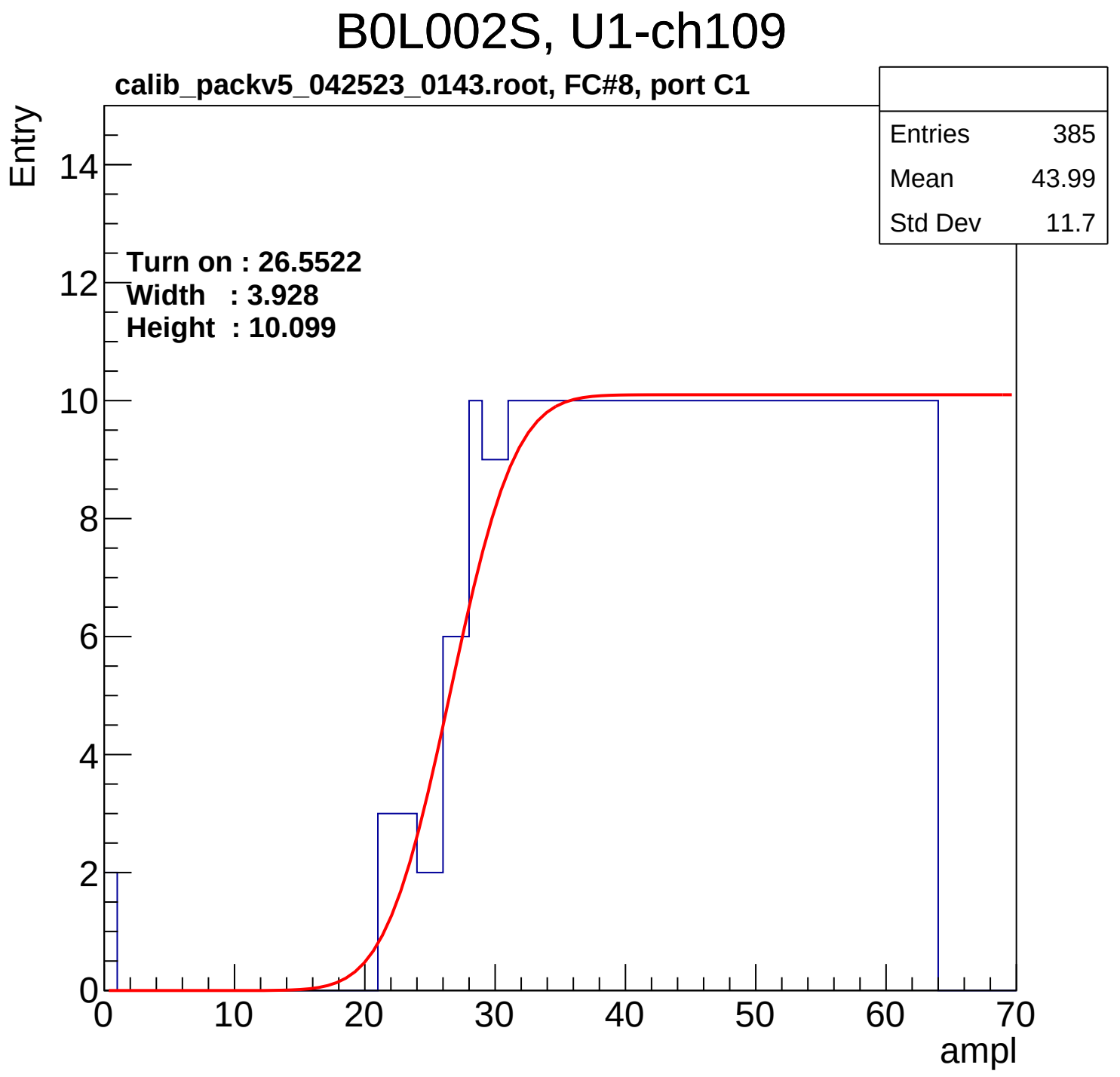
B0L002S, U1-ch109
calib_packv5_042523_0143.root, FC#8, port C1
Entries 385
Mean 43.99
Std Dev 11.7
Turn on : 26.5522
Width : 3.928
Height : 10.099
Entry
ampl
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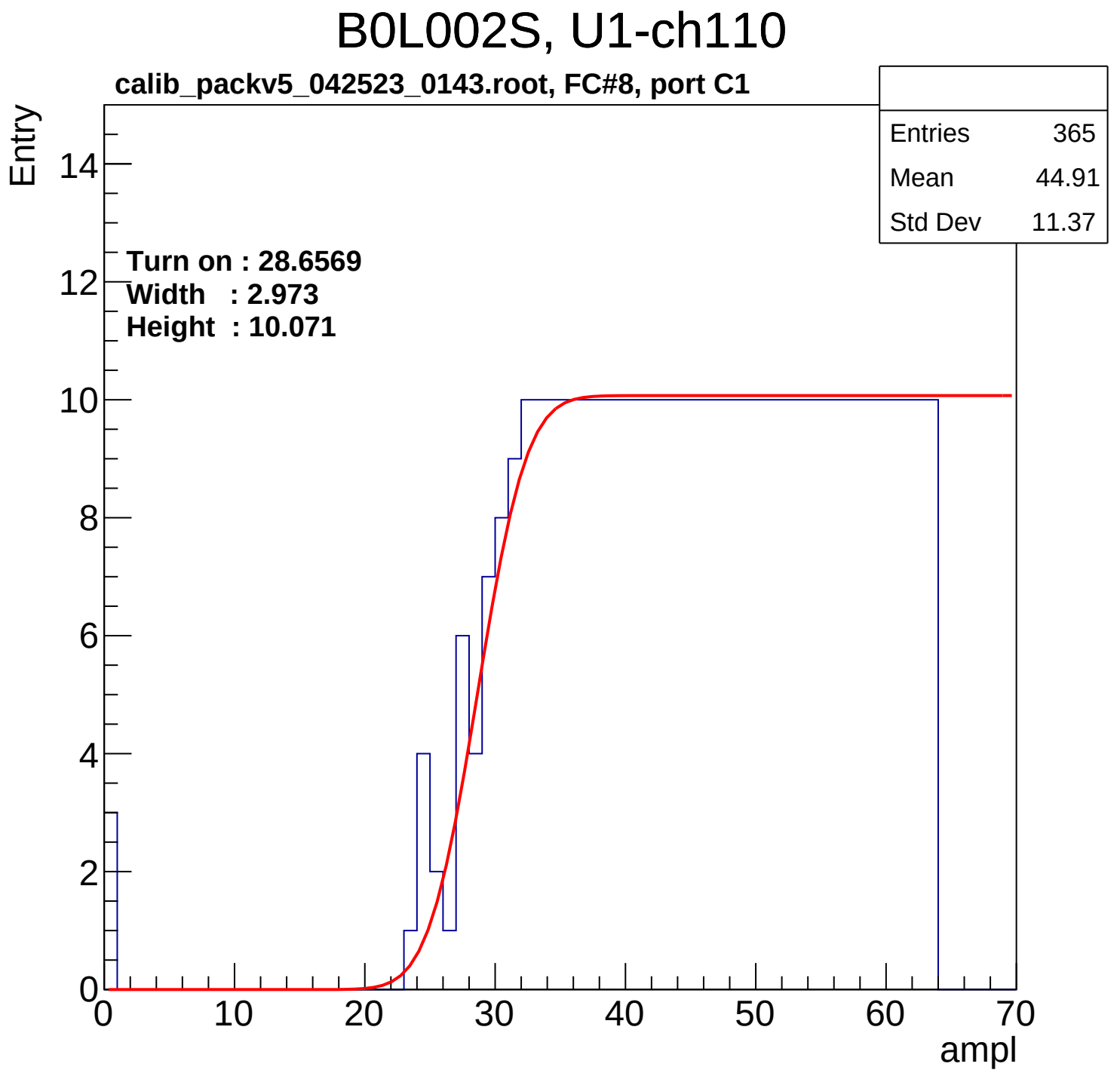
B0L002S, U1-ch110
calib_packv5_042523_0143.root, FC#8, port C1
Entries 365
Mean 44.91
Std Dev 11.37
Turn on : 28.6569
Width : 2.973
Height : 10.071
Entry
ampl
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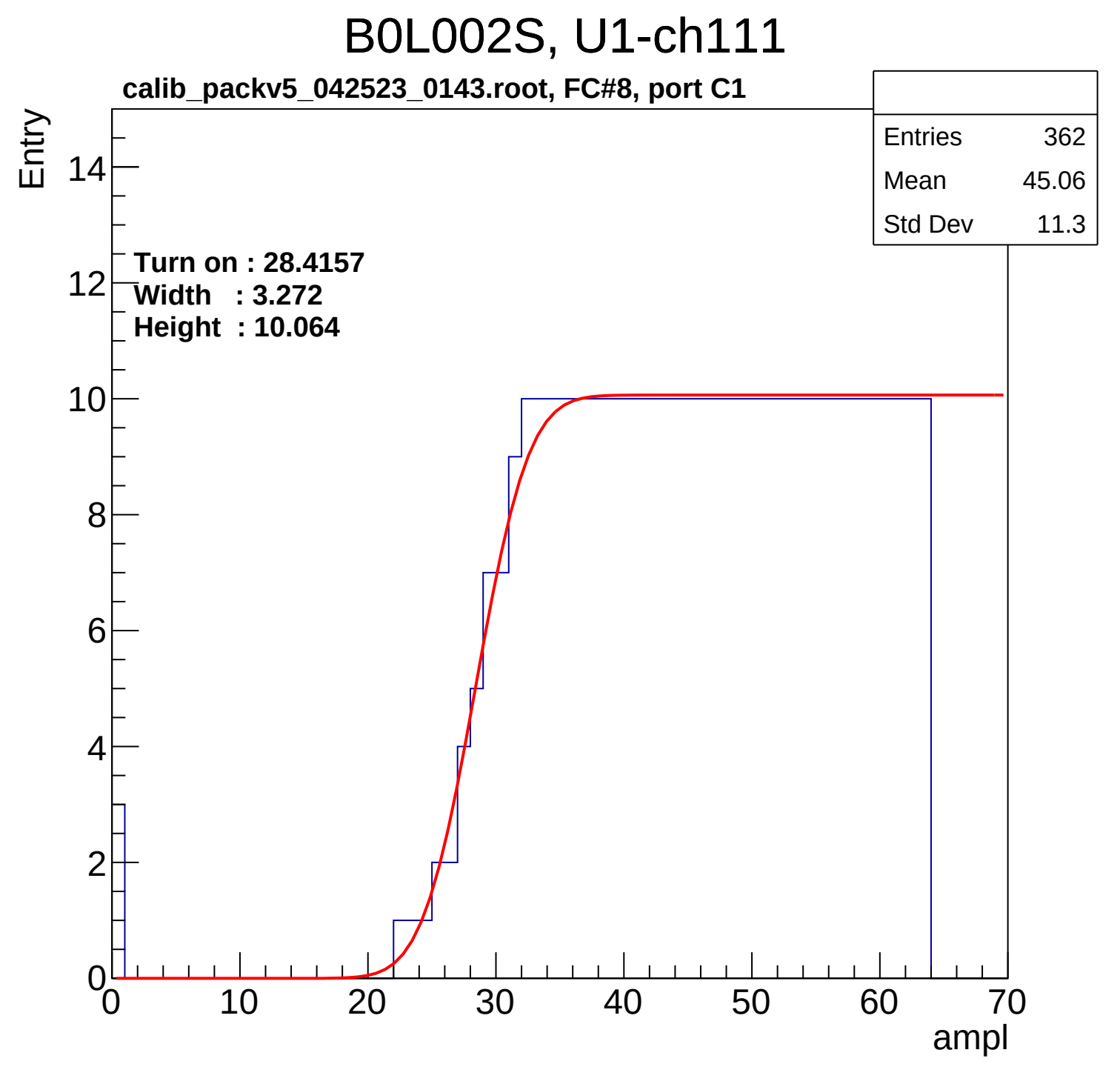
B0L002S, U1-ch111
calib_packv5_042523_0143.root, FC#8, port C1
Entries 362
Mean 45.06
Std Dev 11.3
Turn on : 28.4157
Width : 3.272
Height : 10.064
Entry
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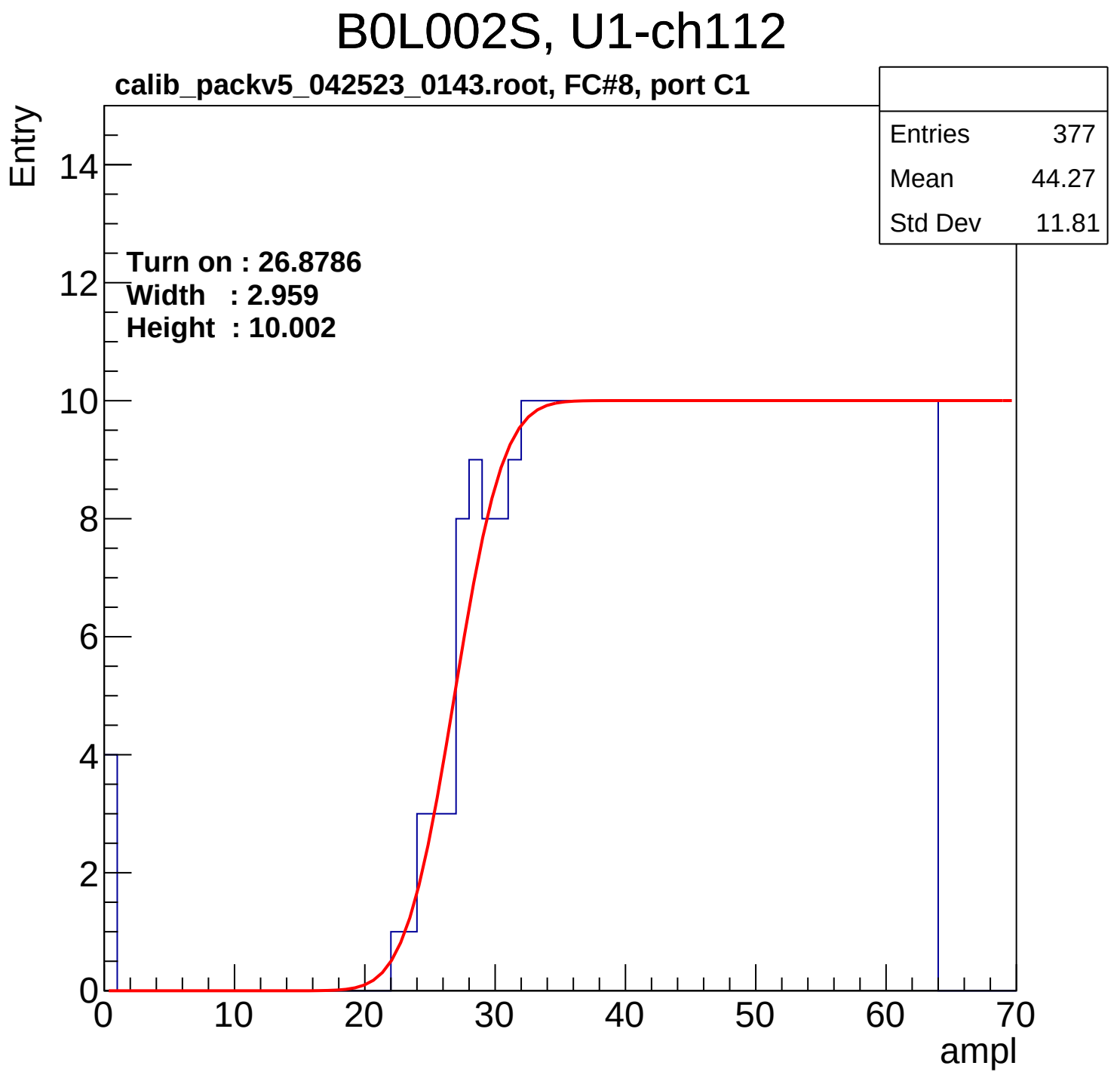
B0L002S, U1-ch112
calib_packv5_042523_0143.root, FC#8, port C1
Entries 377
Mean 44.27
Std Dev 11.81
Turn on : 26.8786
Width : 2.959
Height : 10.002
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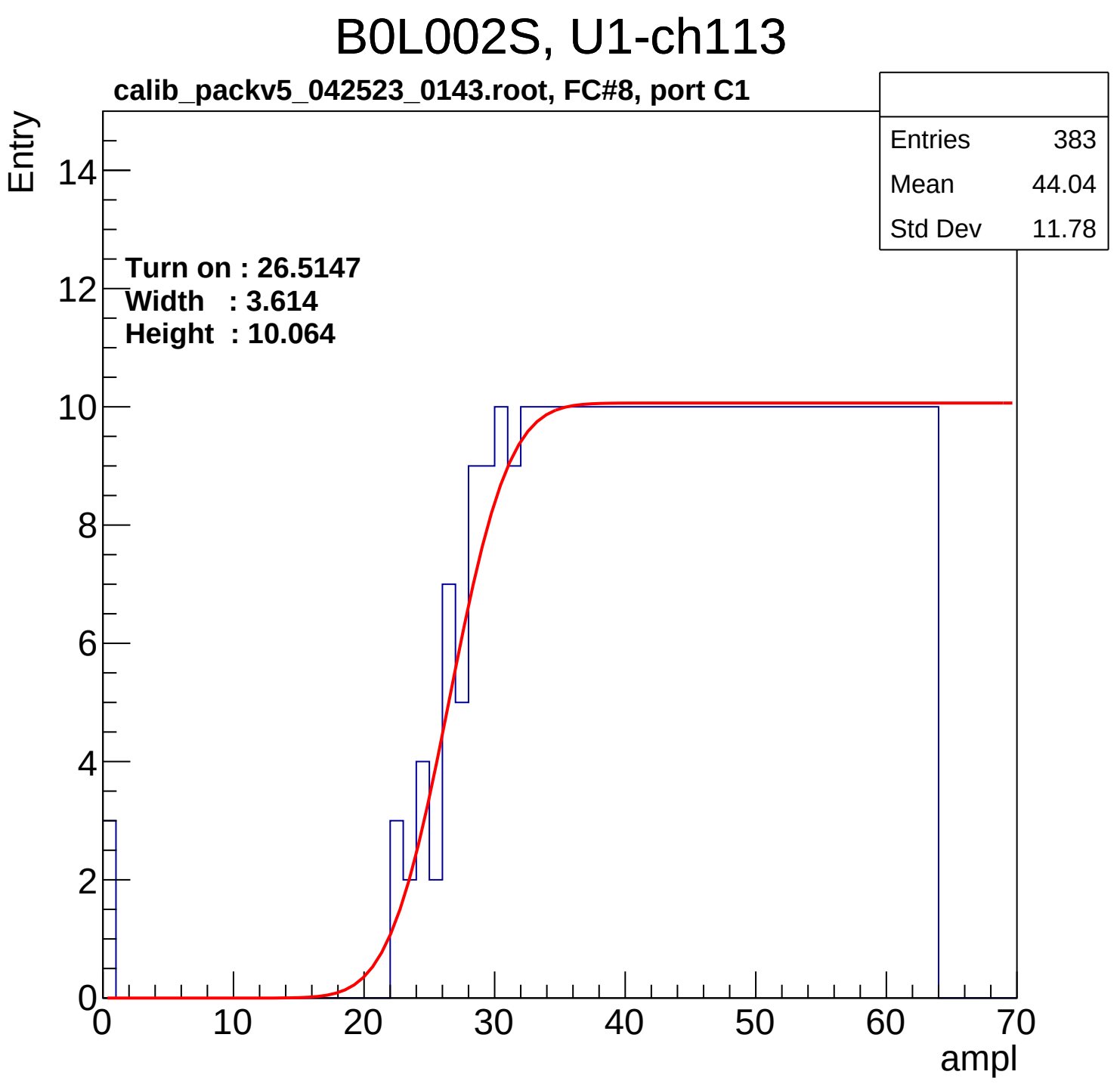
B0L002S, U1-ch113
calib_packv5_042523_0143.root, FC#8, port C1
Entries 383
Mean 44.04
Std Dev 11.78
Turn on : 26.5147
Width : 3.614
Height : 10.064
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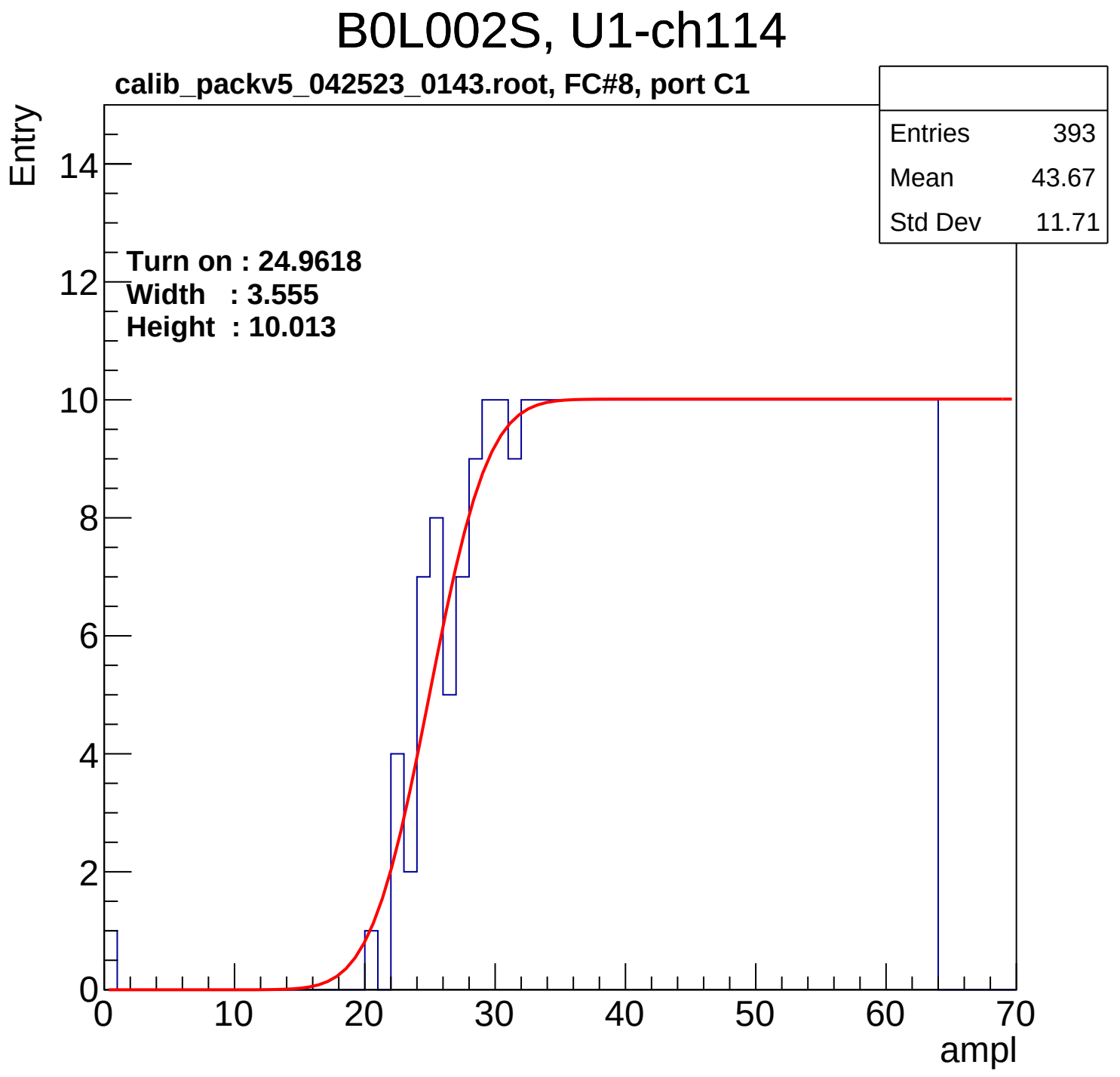
B0L002S, U1-ch114
calib_packv5_042523_0143.root, FC#8, port C1
Entries 393
Mean 43.67
Std Dev 11.71
Turn on : 24.9618
Width : 3.555
Height : 10.013
Entry
ampl
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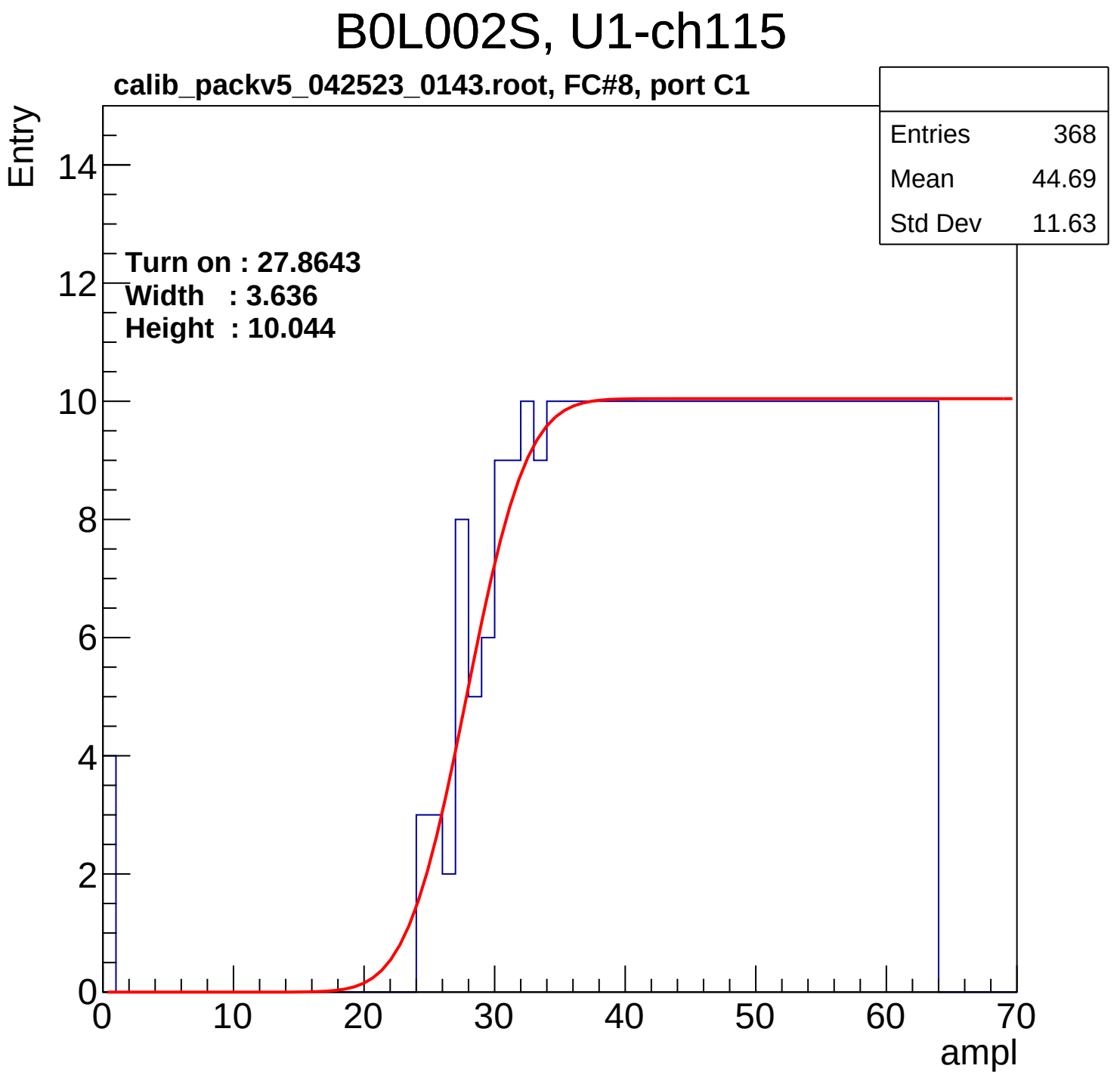
B0L002S, U1-ch115
calib_packv5_042523_0143.root, FC#8, port C1
Entries 368
Mean 44.69
Std Dev 11.63
Turn on : 27.8643
Width : 3.636
Height : 10.044
Entry
ampl
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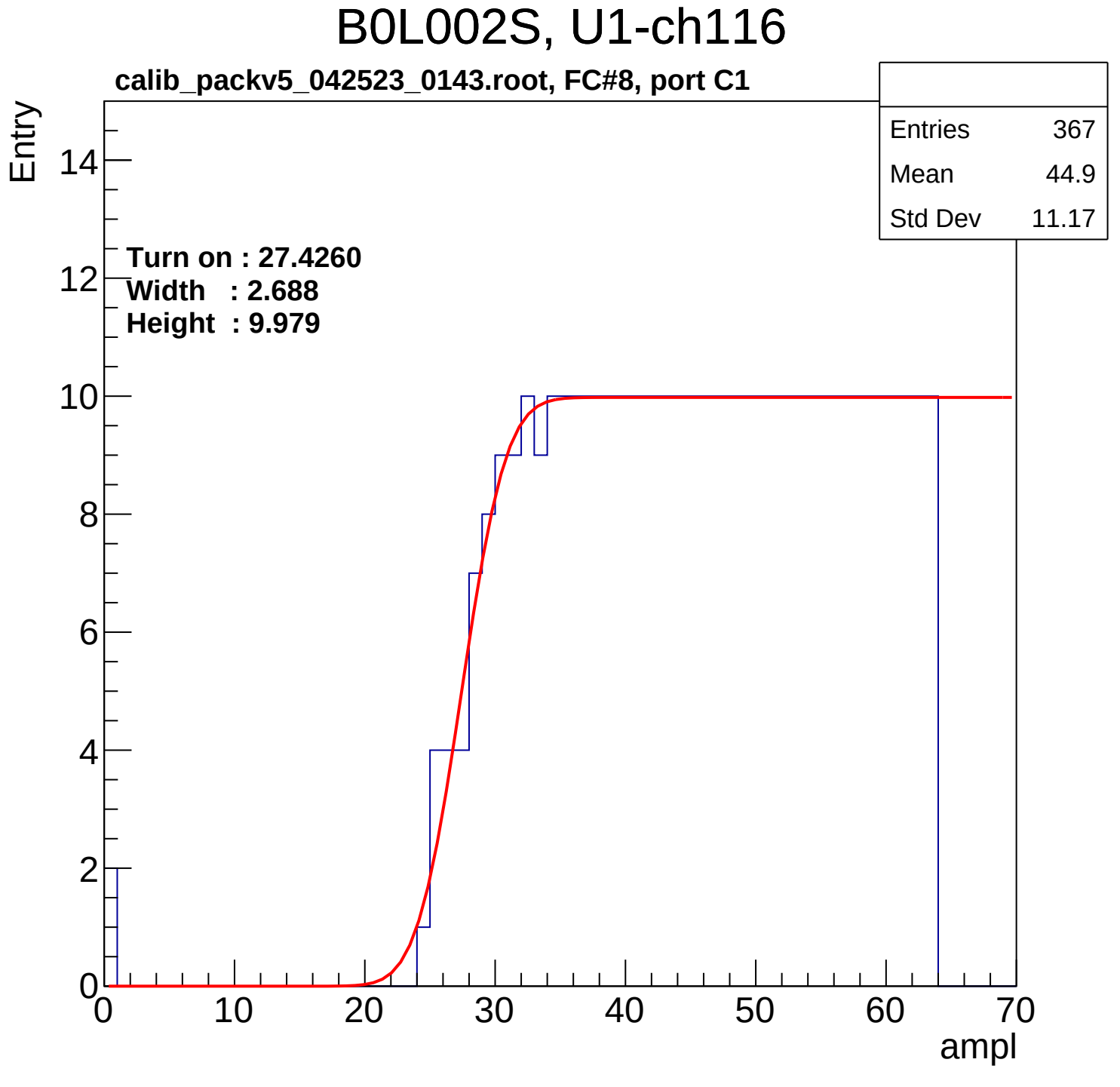
B0L002S, U1-ch116
calib_packv5_042523_0143.root, FC#8, port C1
Entries 367
Mean 44.9
Std Dev 11.17
Turn on : 27.4260
Width : 2.688
Height : 9.979
Entry
ampl
0
2
4
6
8
10
12
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0
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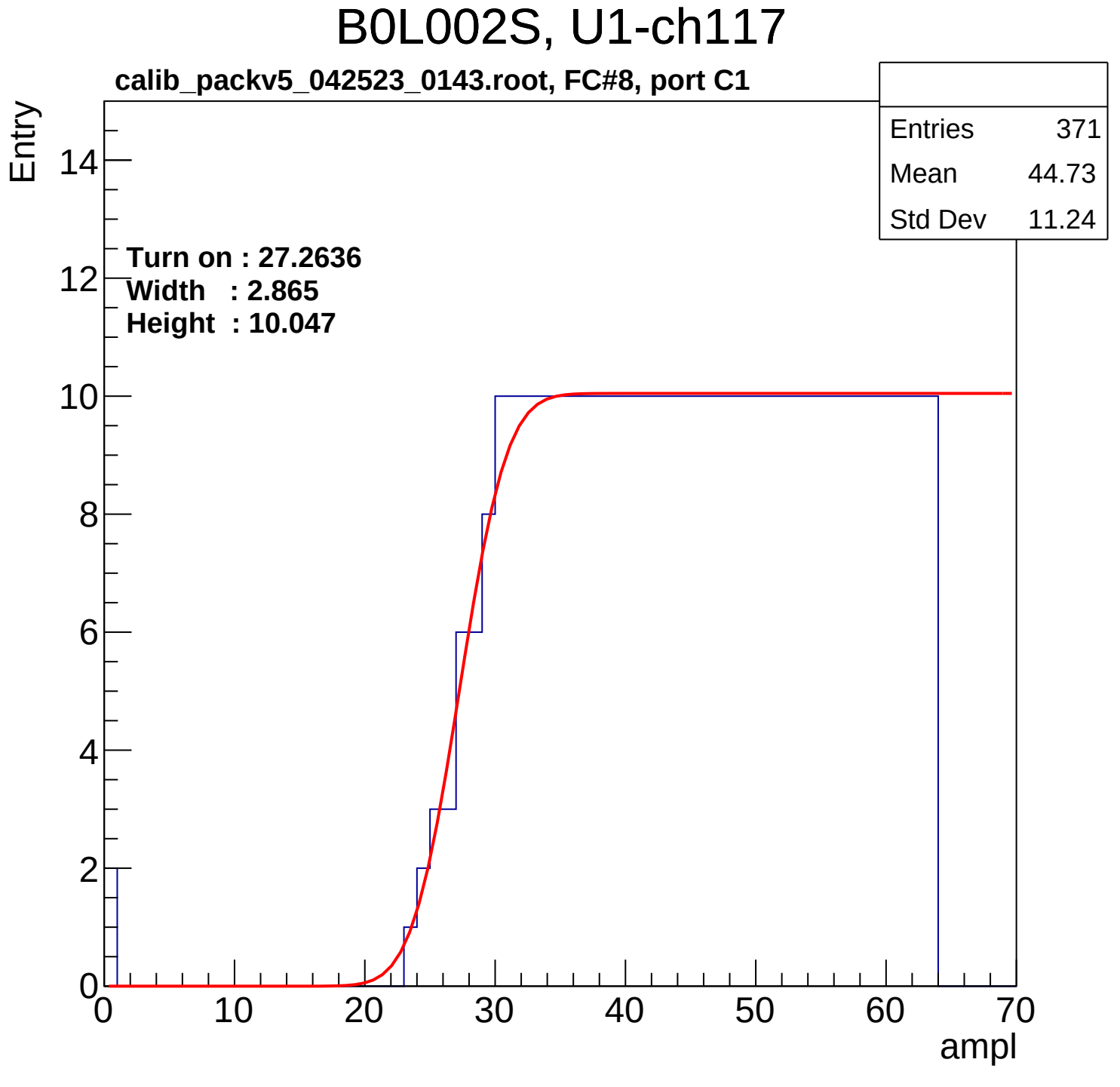
B0L002S, U1-ch117
calib_packv5_042523_0143.root, FC#8, port C1
Entries 371
Mean 44.73
Std Dev 11.24
Turn on : 27.2636
Width : 2.865
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
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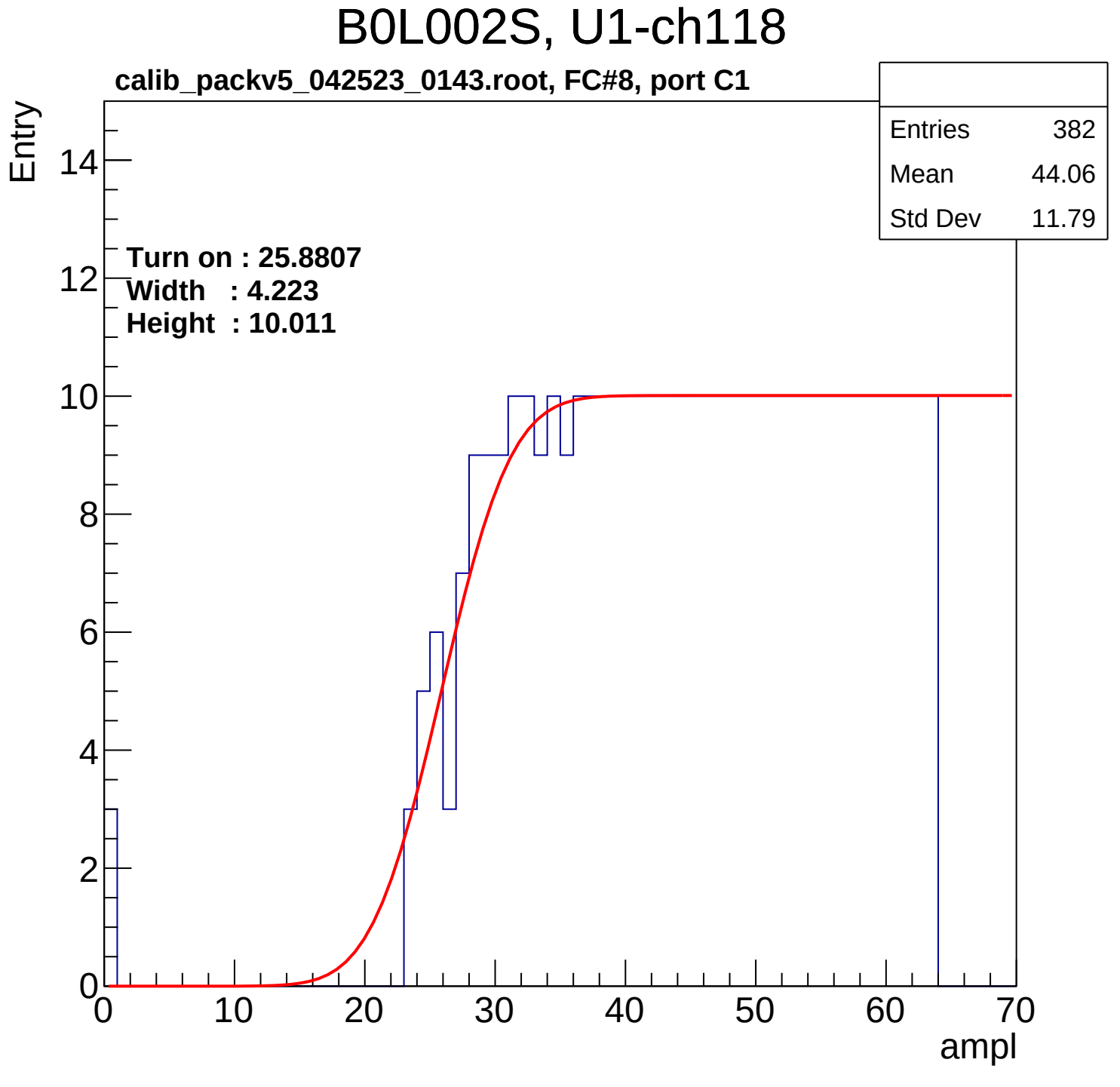
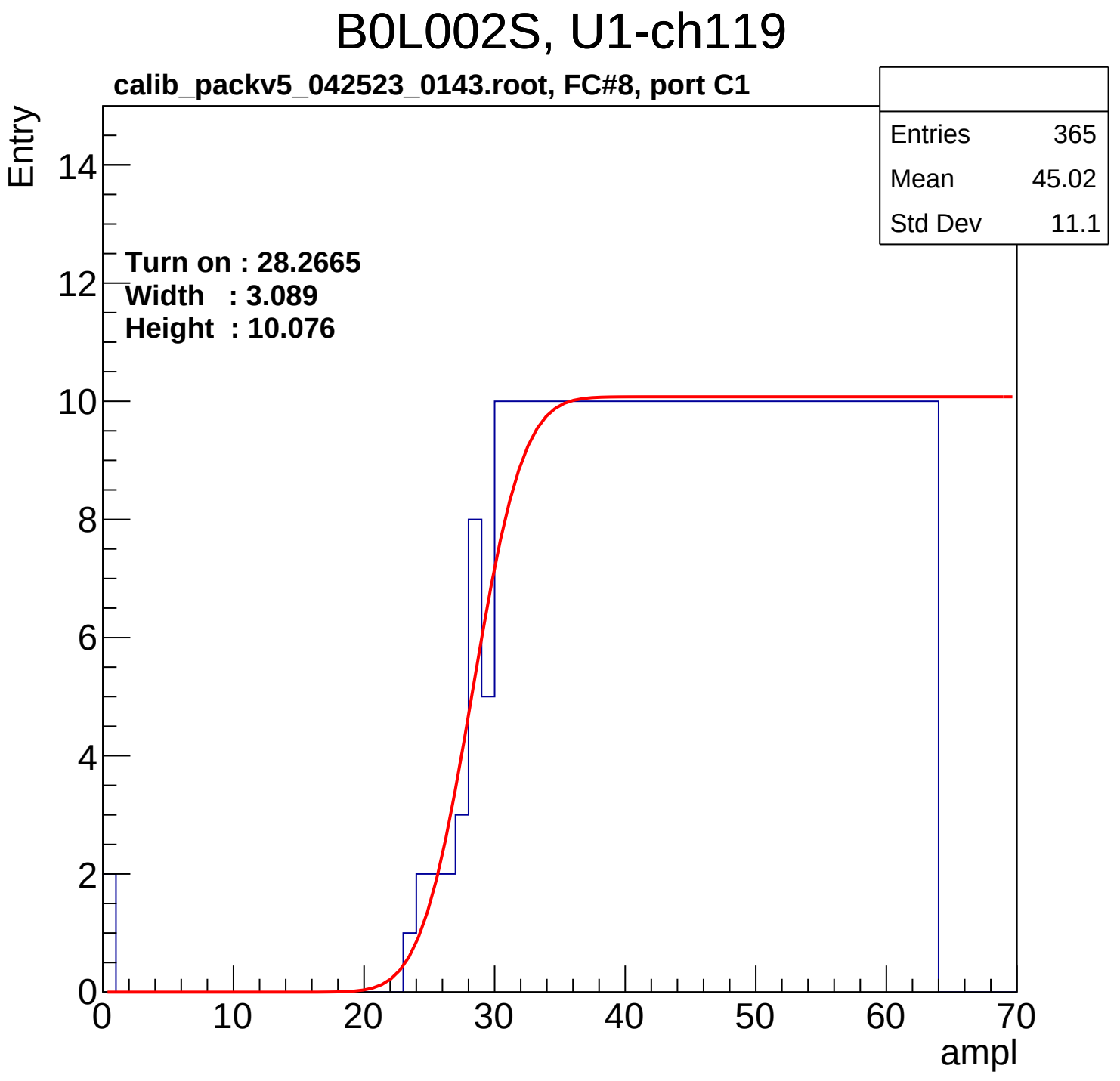
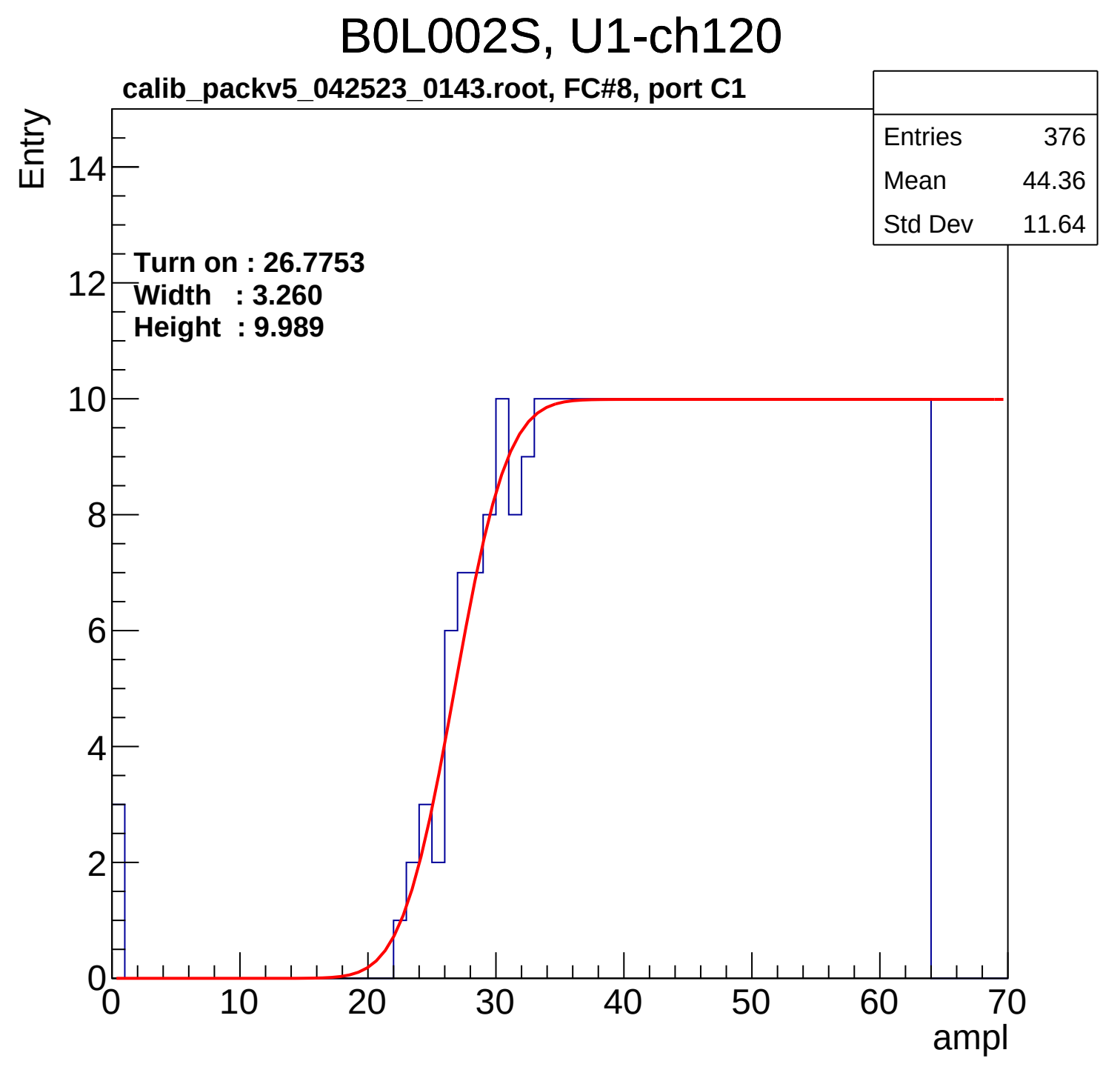

B0L002S, U1-ch118
calib_packv5_042523_0143.root, FC#8, port C1
Entries 382
Mean 44.06
Std Dev 11.79
Turn on : 25.8807
Width : 4.223
Height : 10.011
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L002S, U1-ch119
calib_packv5_042523_0143.root, FC#8, port C1
Entries 365
Mean 45.02
Std Dev 11.1
Turn on : 28.2665
Width : 3.089
Height : 10.076
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L002S, U1-ch120
calib_packv5_042523_0143.root, FC#8, port C1
Entries 376
Mean 44.36
Std Dev 11.64
Turn on : 26.7753
Width : 3.260
Height : 9.989
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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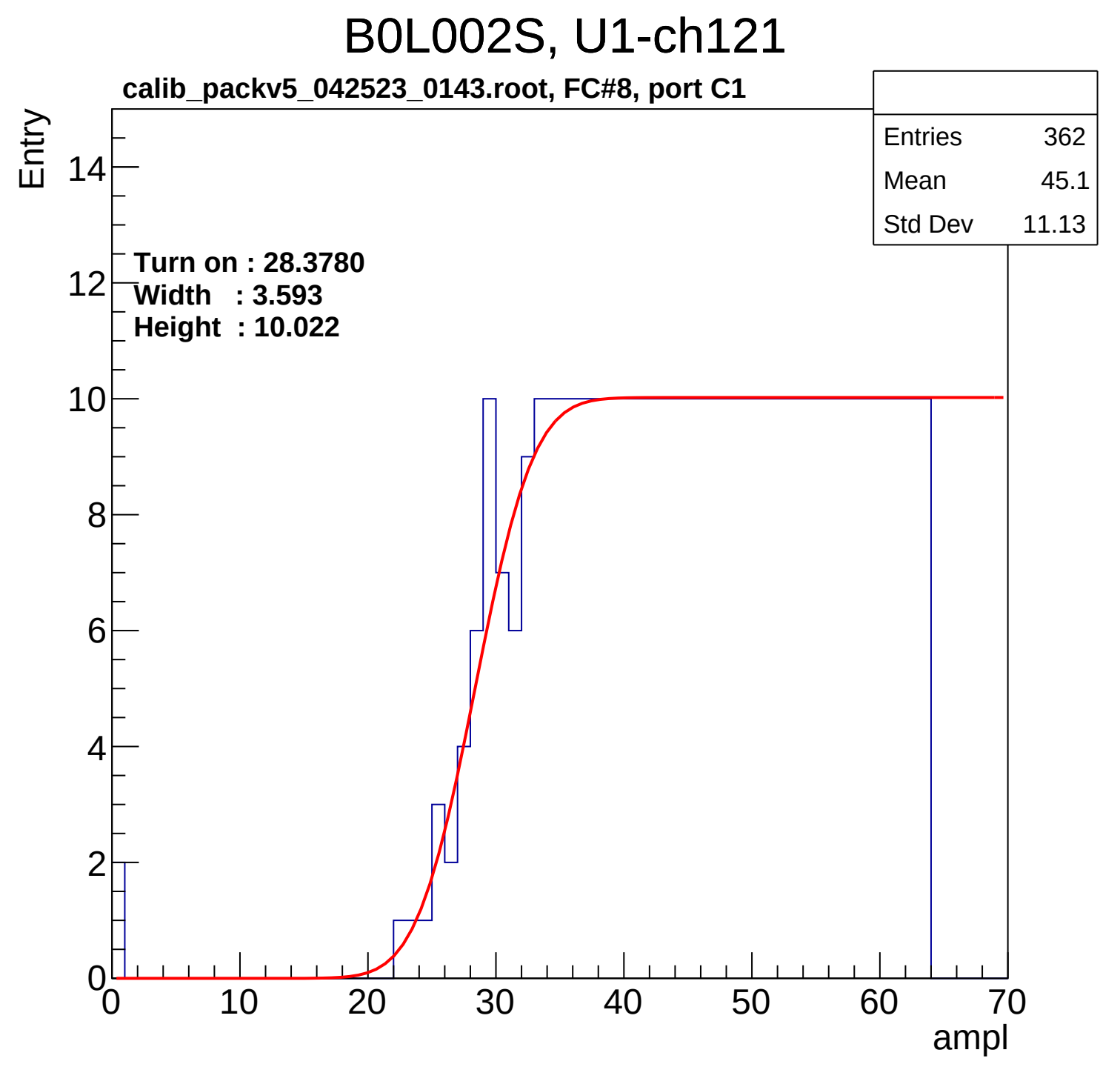
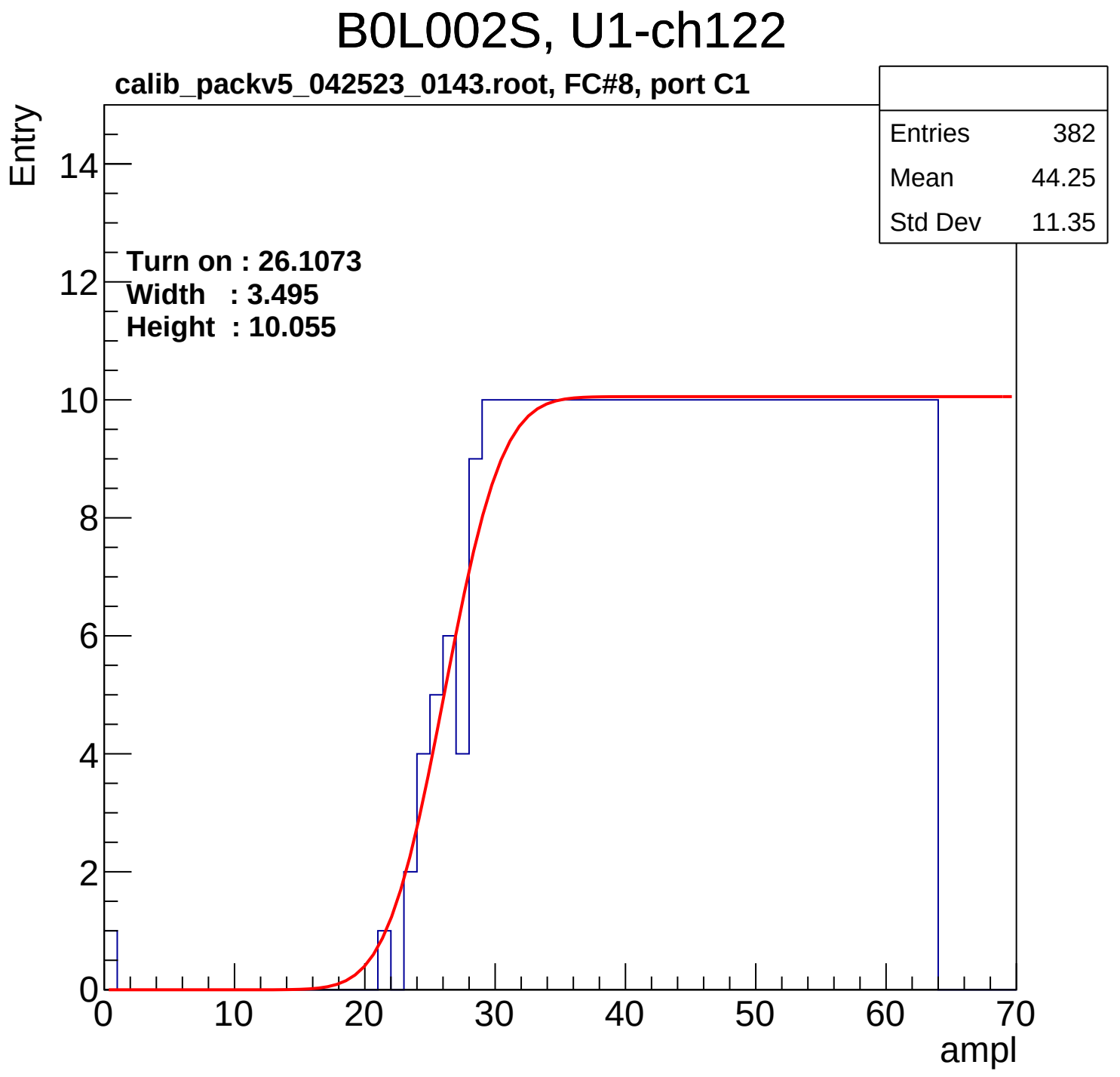
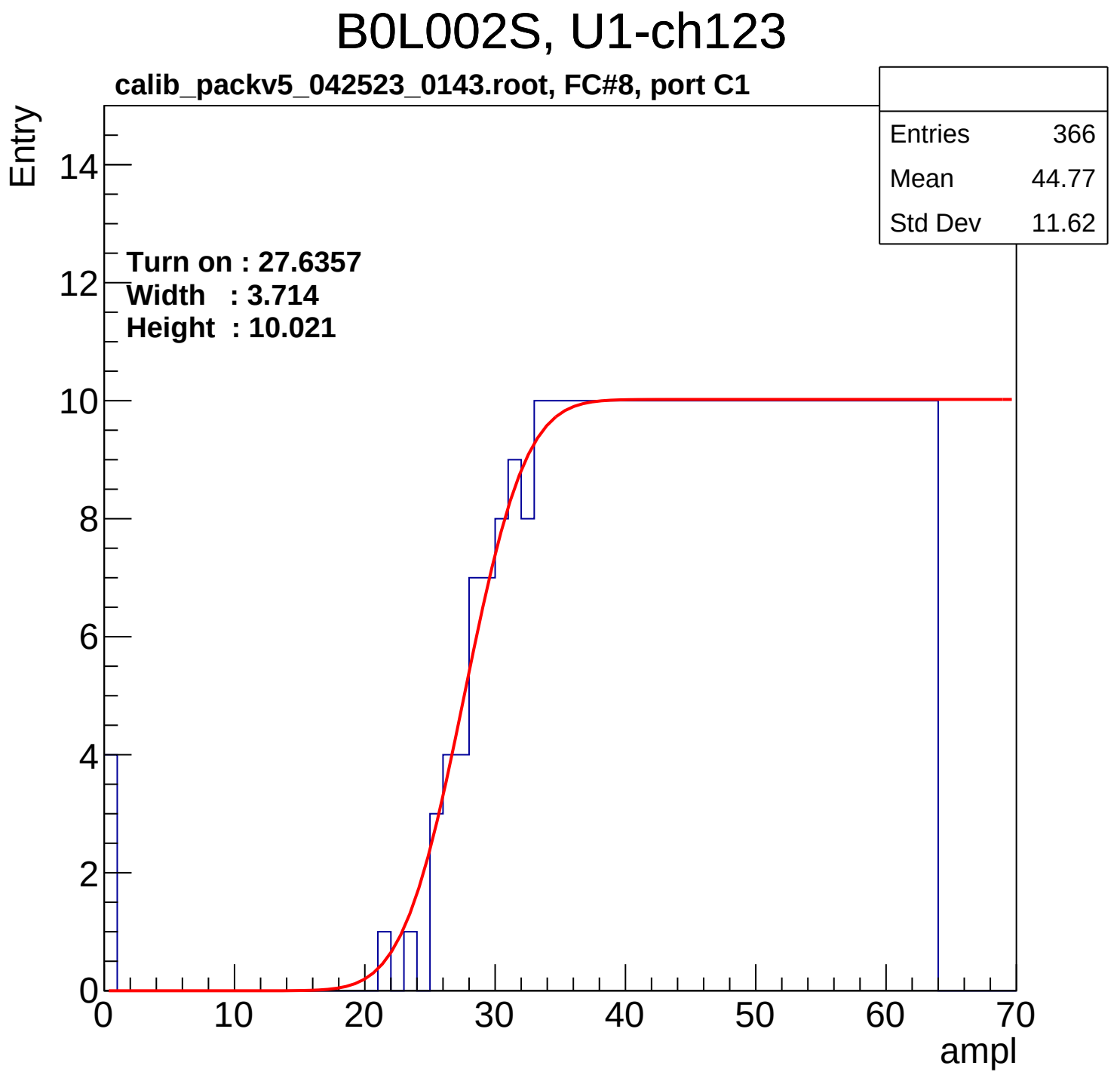
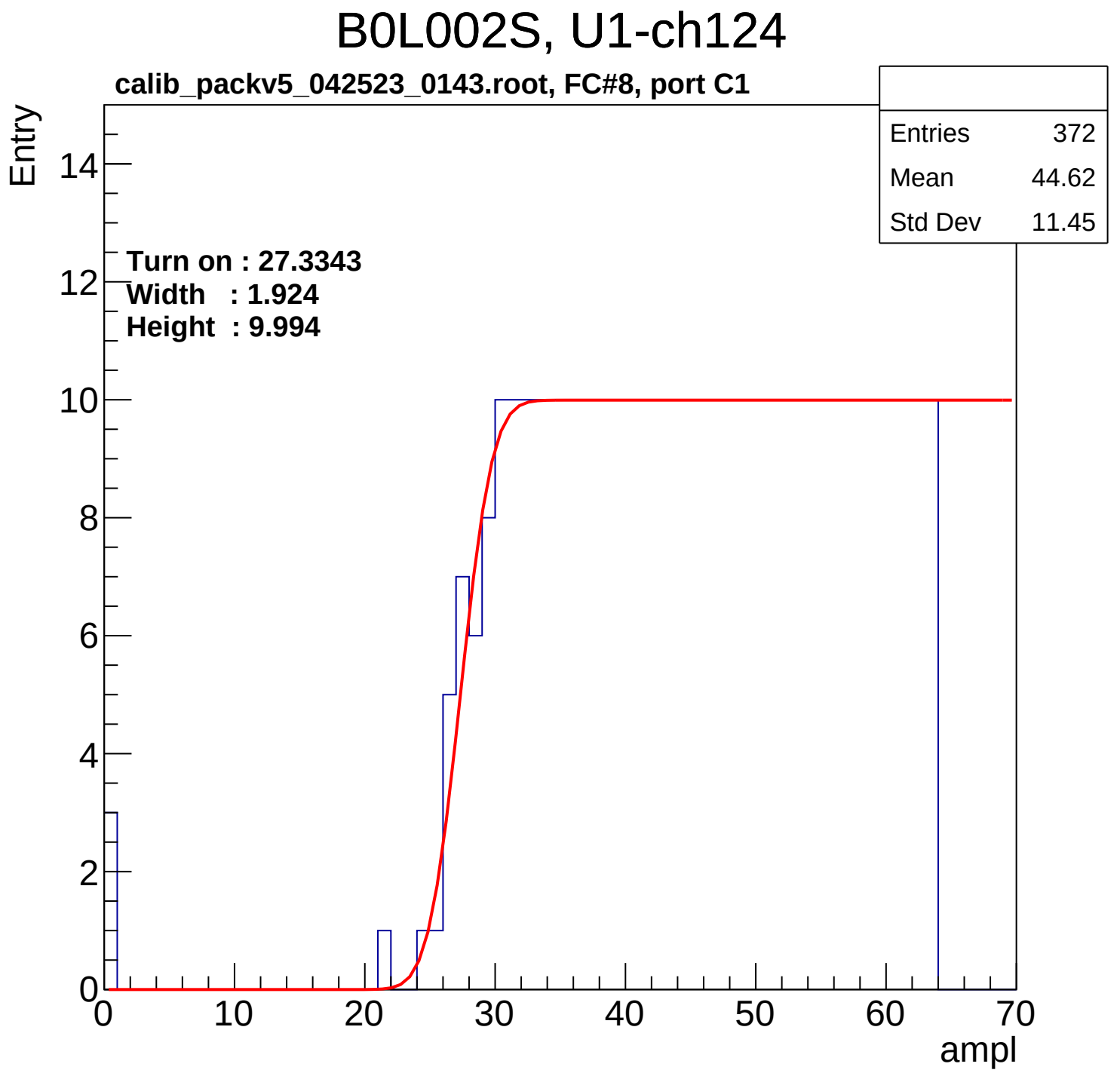
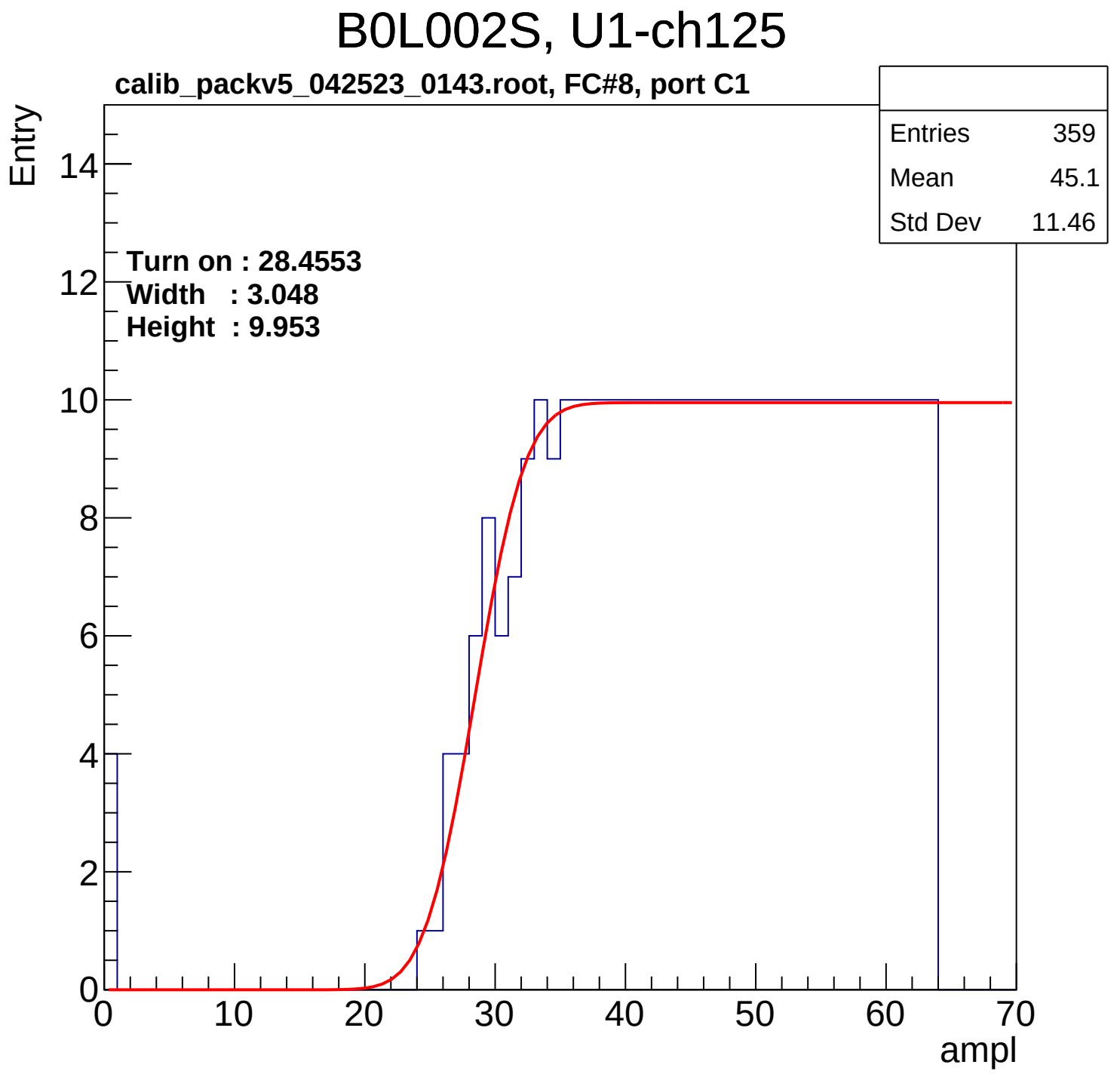

B0L002S, U1-ch121
calib_packv5_042523_0143.root, FC#8, port C1
Entries 362
Mean 45.1
Std Dev 11.13
Turn on : 28.3780
Width : 3.593
Height : 10.022
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L002S, U1-ch122
calib_packv5_042523_0143.root, FC#8, port C1
Entries 382
Mean 44.25
Std Dev 11.35
Turn on : 26.1073
Width : 3.495
Height : 10.055
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L002S, U1-ch123
calib_packv5_042523_0143.root, FC#8, port C1
Entries 366
Mean 44.77
Std Dev 11.62
Turn on : 27.6357
Width : 3.714
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L002S, U1-ch124
calib_packv5_042523_0143.root, FC#8, port C1
Entries 372
Mean 44.62
Std Dev 11.45
Turn on : 27.3343
Width : 1.924
Height : 9.994
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L002S, U1-ch125
calib_packv5_042523_0143.root, FC#8, port C1
Entries 359
Mean 45.1
Std Dev 11.46
Turn on : 28.4553
Width : 3.048
Height : 9.953
Entry
ampl
0
2
4
6
8
10
12
14
0
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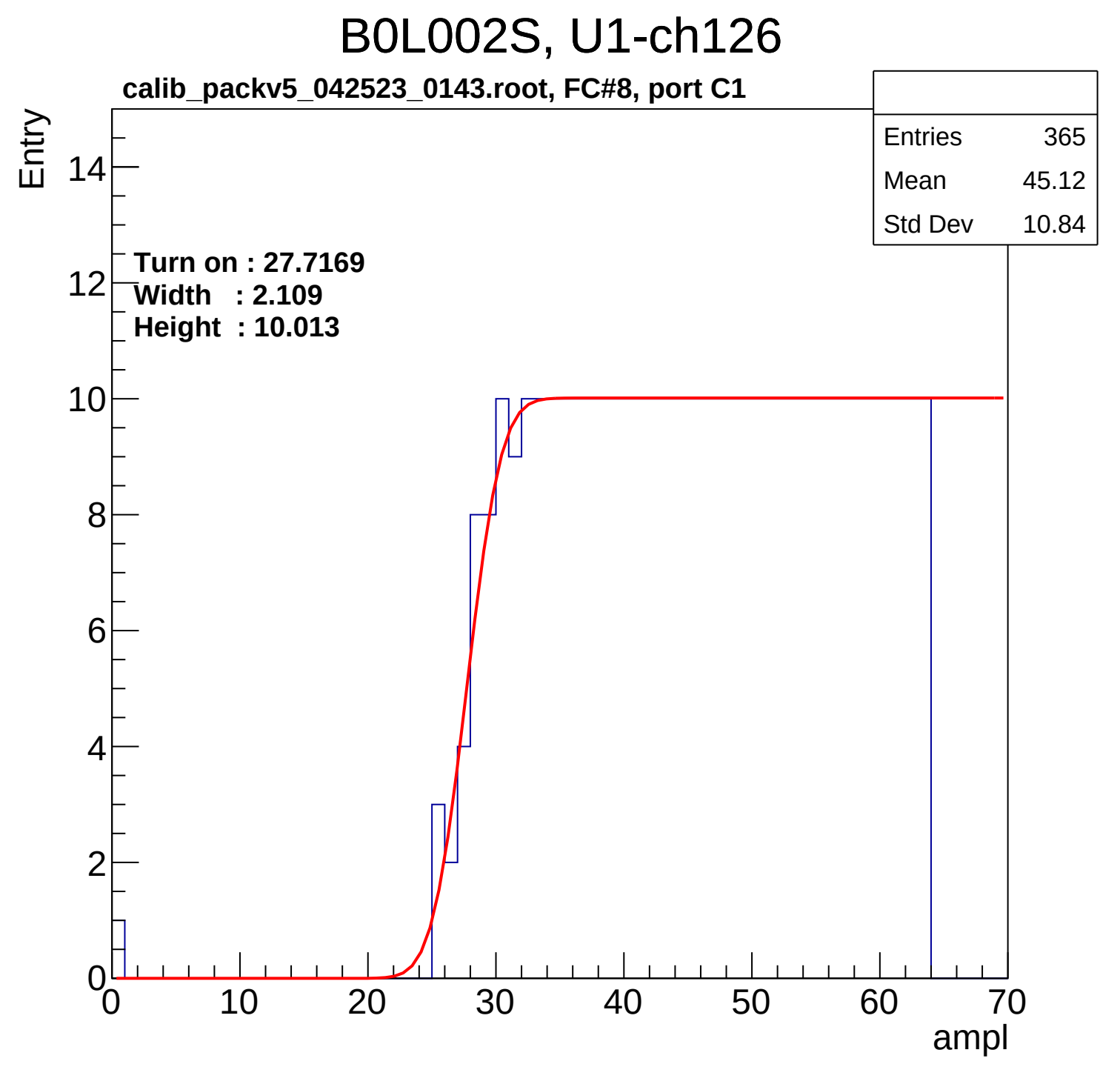
20
30
40
50
60
70


B0L002S, U1-ch126
calib_packv5_042523_0143.root, FC#8, port C1
Entries 365
Mean 45.12
Std Dev 10.84
Turn on : 27.7169
Width : 2.109
Height : 10.013
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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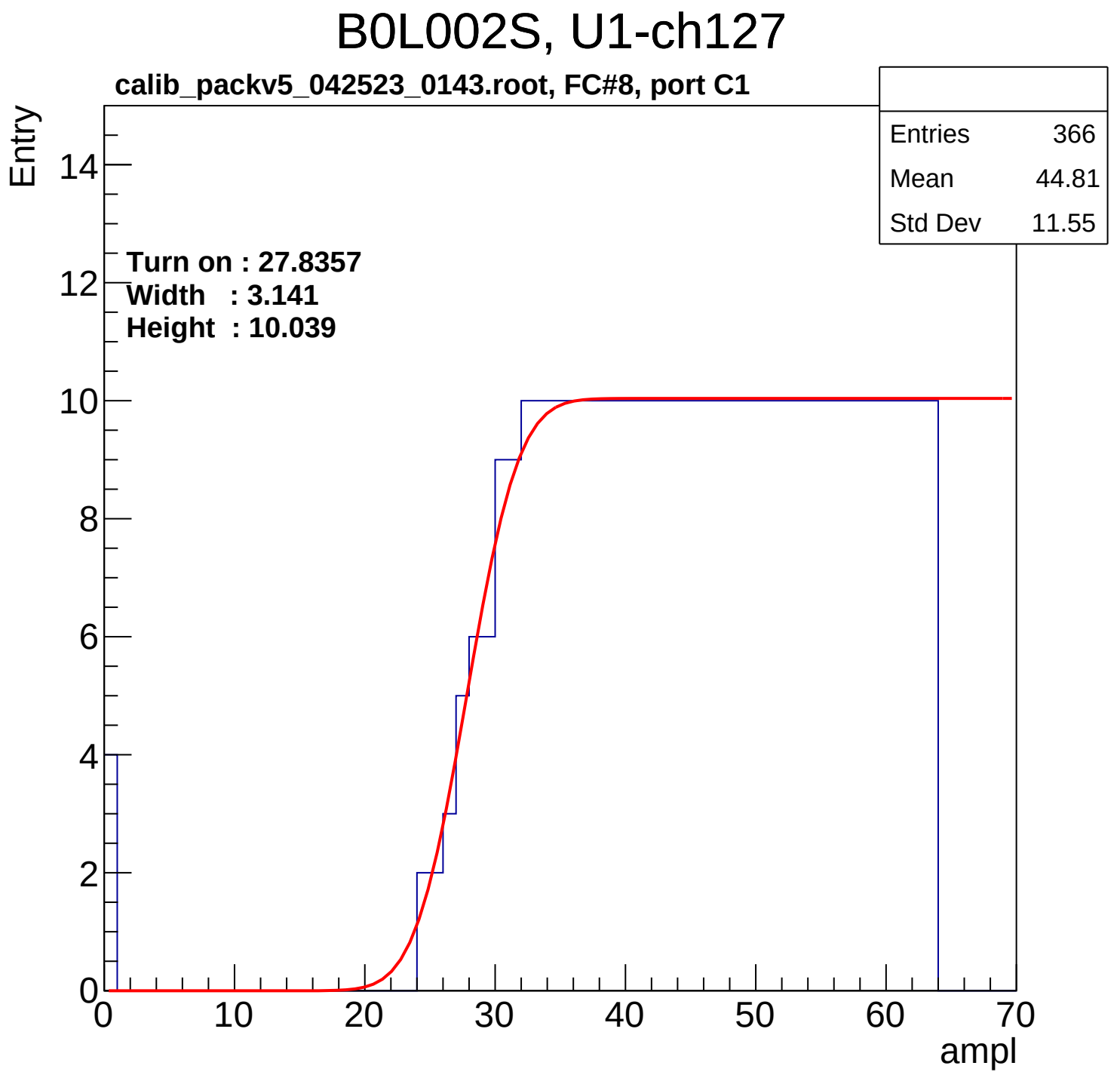
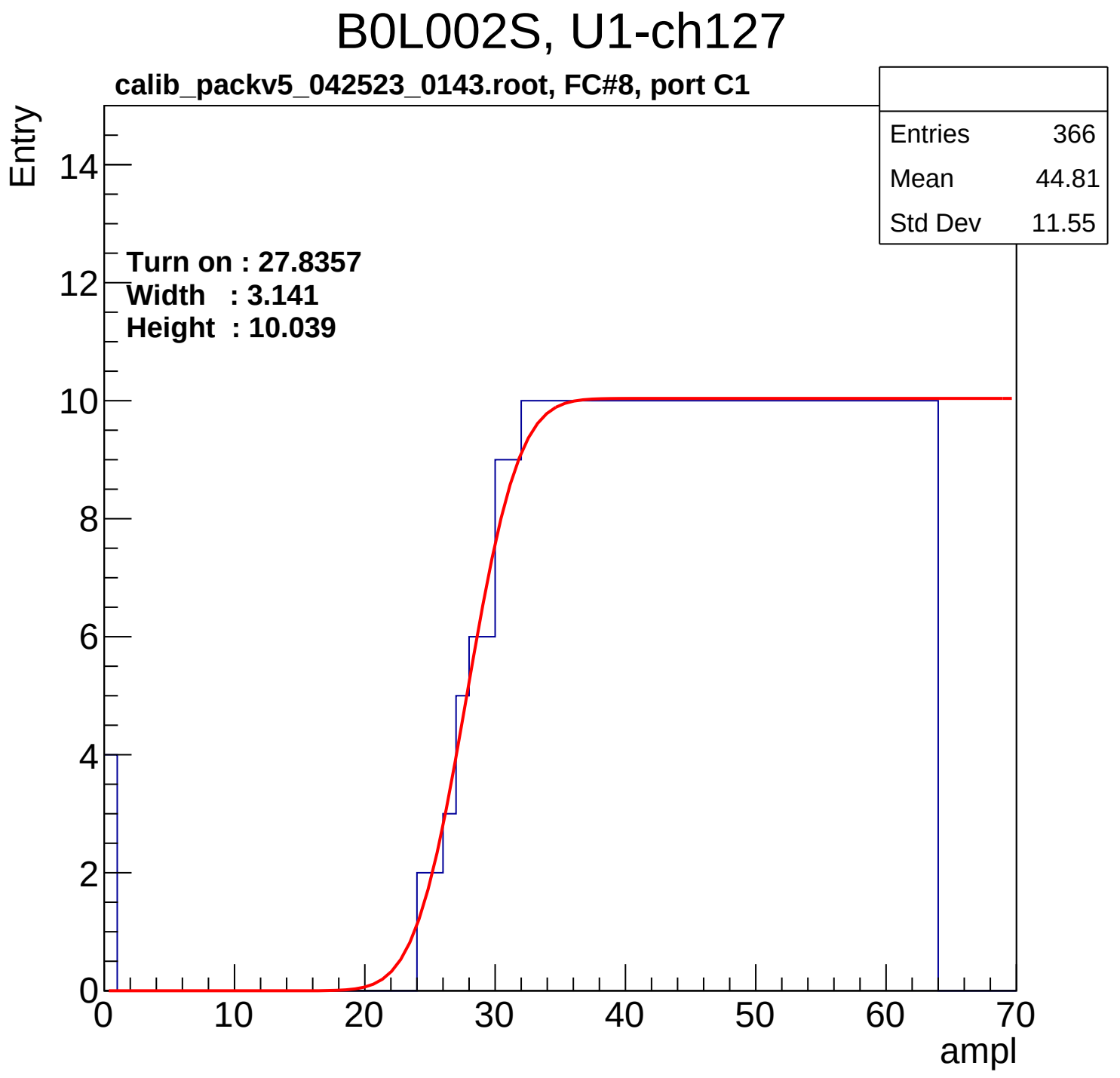

B0L002S, U1-ch127
calib_packv5_042523_0143.root, FC#8, port C1
Entries 366
Mean 44.81
Std Dev 11.55
Turn on : 27.8357
Width : 3.141
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L002S, U1-ch127
calib_packv5_042523_0143.root, FC#8, port C1
Entries 366
Mean 44.81
Std Dev 11.55
Turn on : 27.8357
Width : 3.141
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70