

B1L102S, U5-ch0

calib_packv5_042523_0143.root, FC#11, port A2

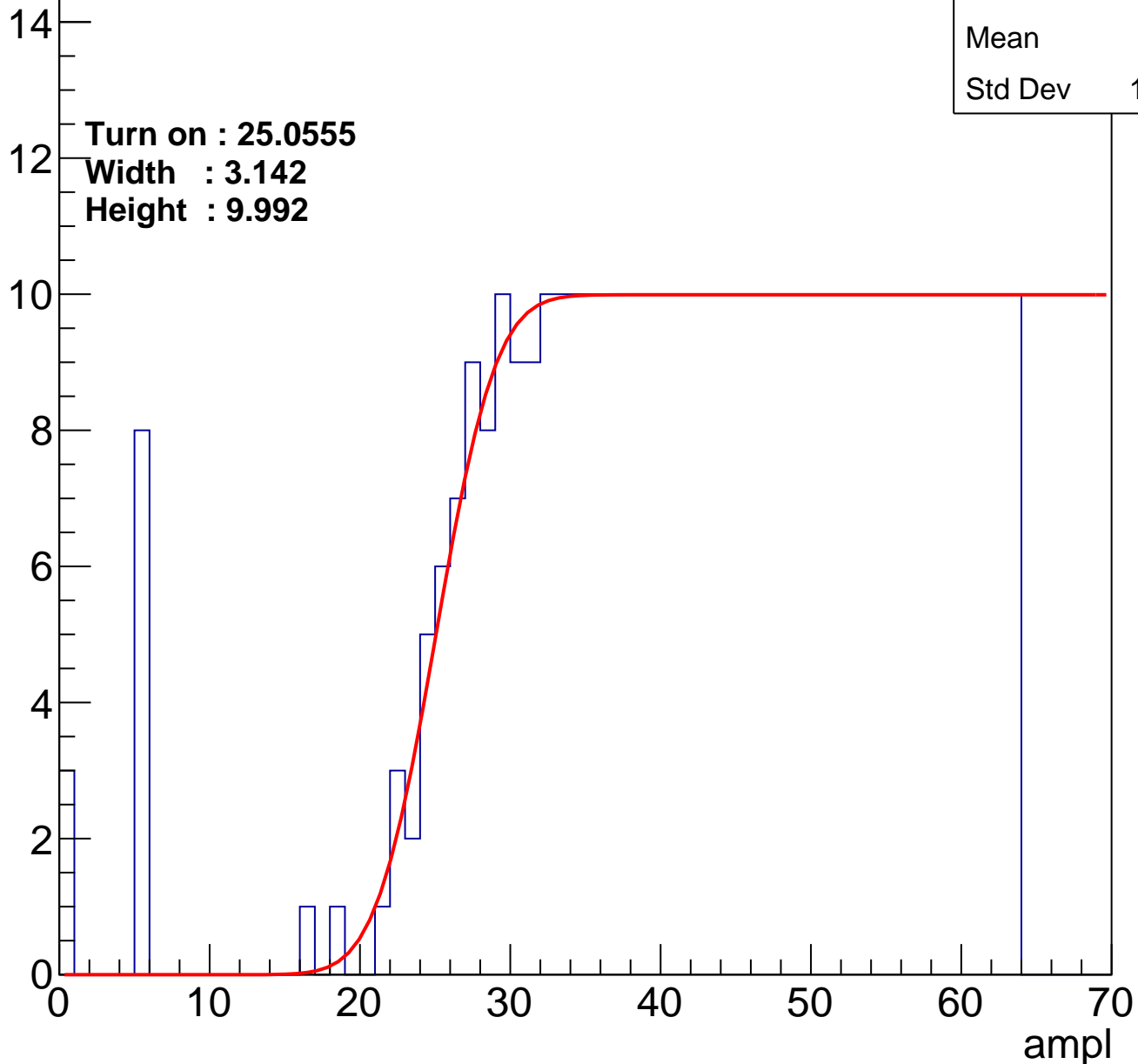
Entries	402
Mean	42.7
Std Dev	13.14

Turn on : 25.0555

Width : 3.142

Height : 9.992

Entry



B1L102S, U5-ch1

calib_packv5_042523_0143.root, FC#11, port A2

Entries	395
Mean	43.58
Std Dev	11.75

Turn on : 24.9777

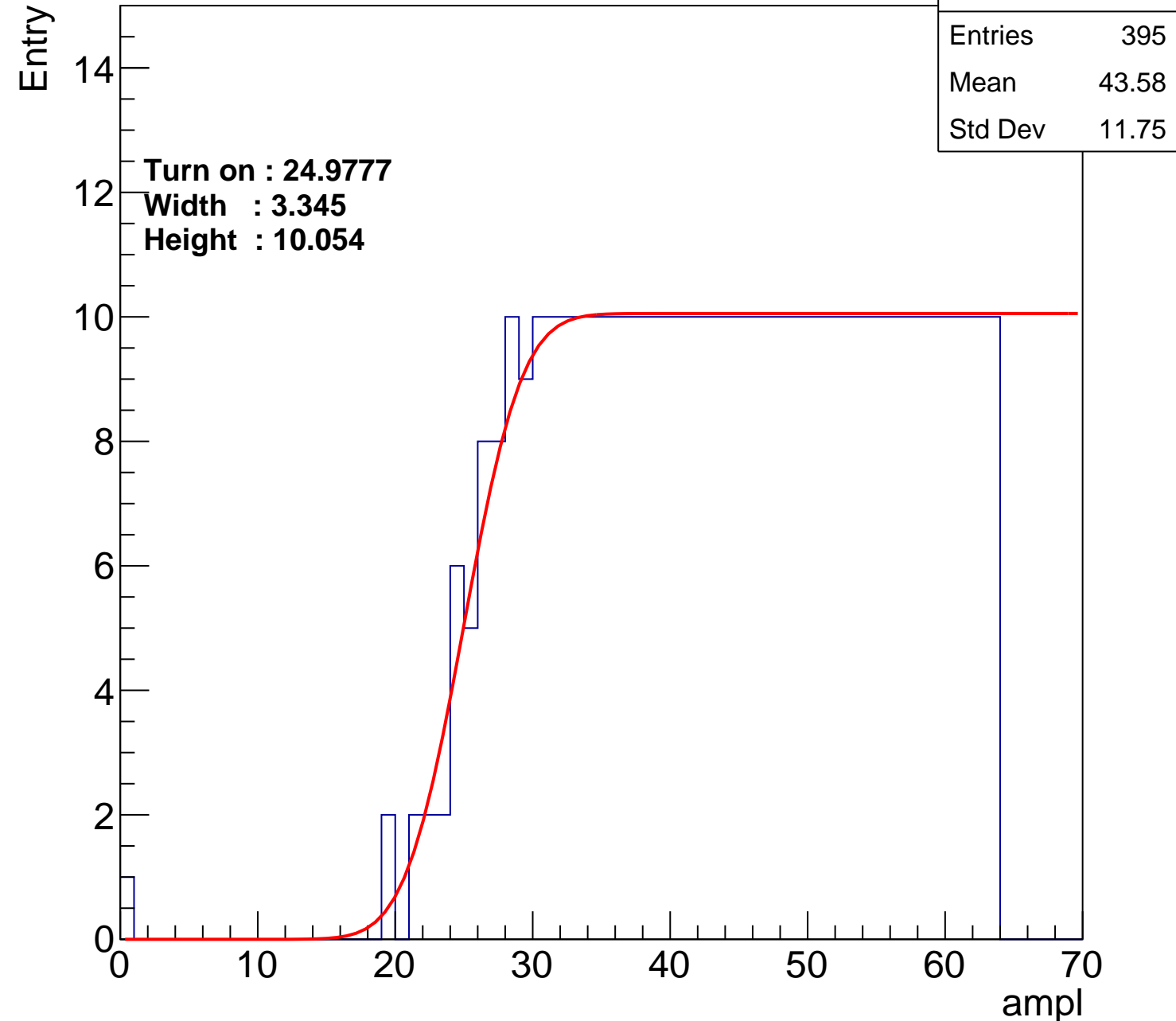
Width : 3.345

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch2

calib_packv5_042523_0143.root, FC#11, port A2

Entries	396
Mean	43.26
Std Dev	12.44

Turn on : 25.0950

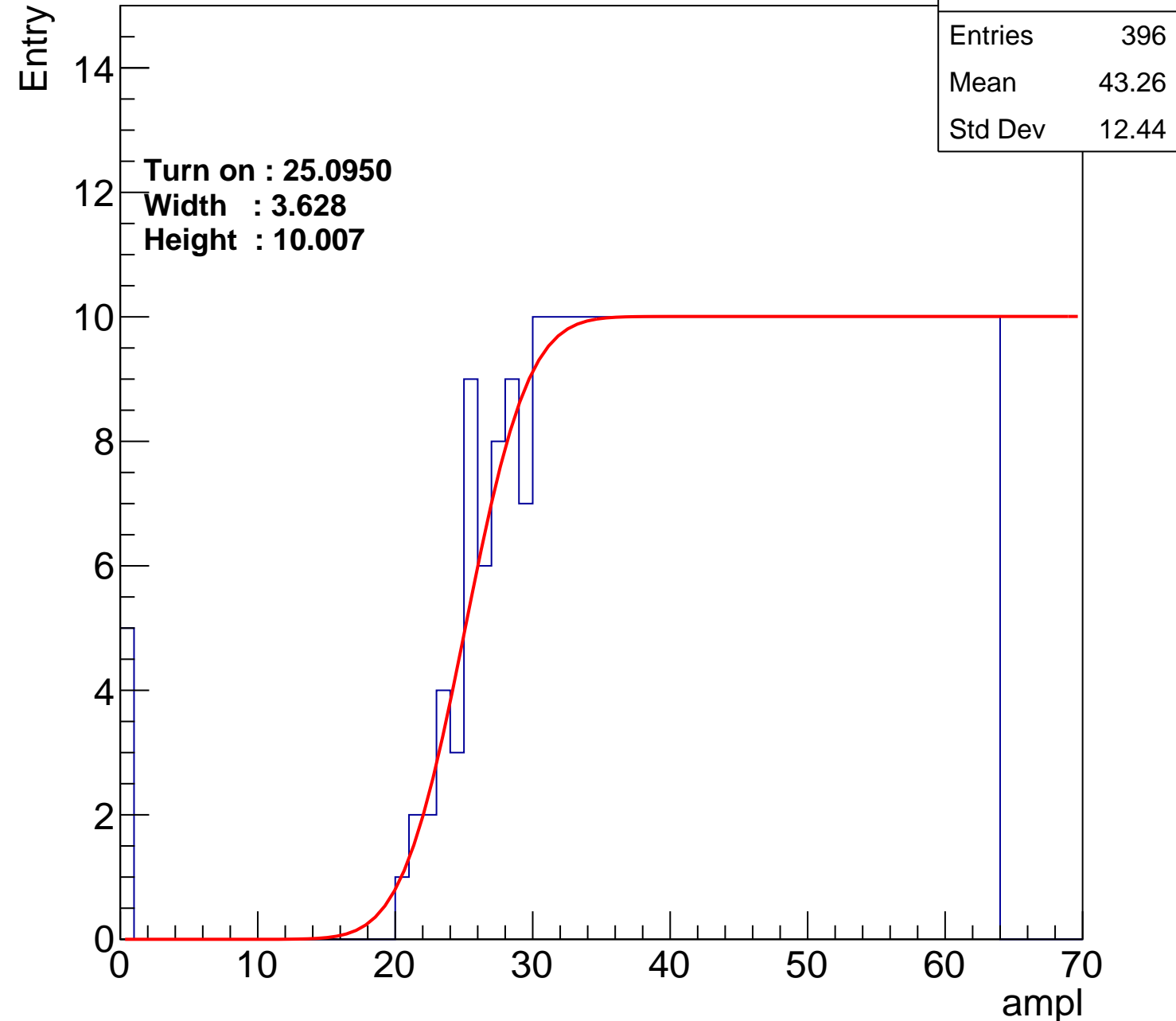
Width : 3.628

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch3

calib_packv5_042523_0143.root, FC#11, port A2

Entries	384
Mean	43.95
Std Dev	11.88

Turn on : 26.1180

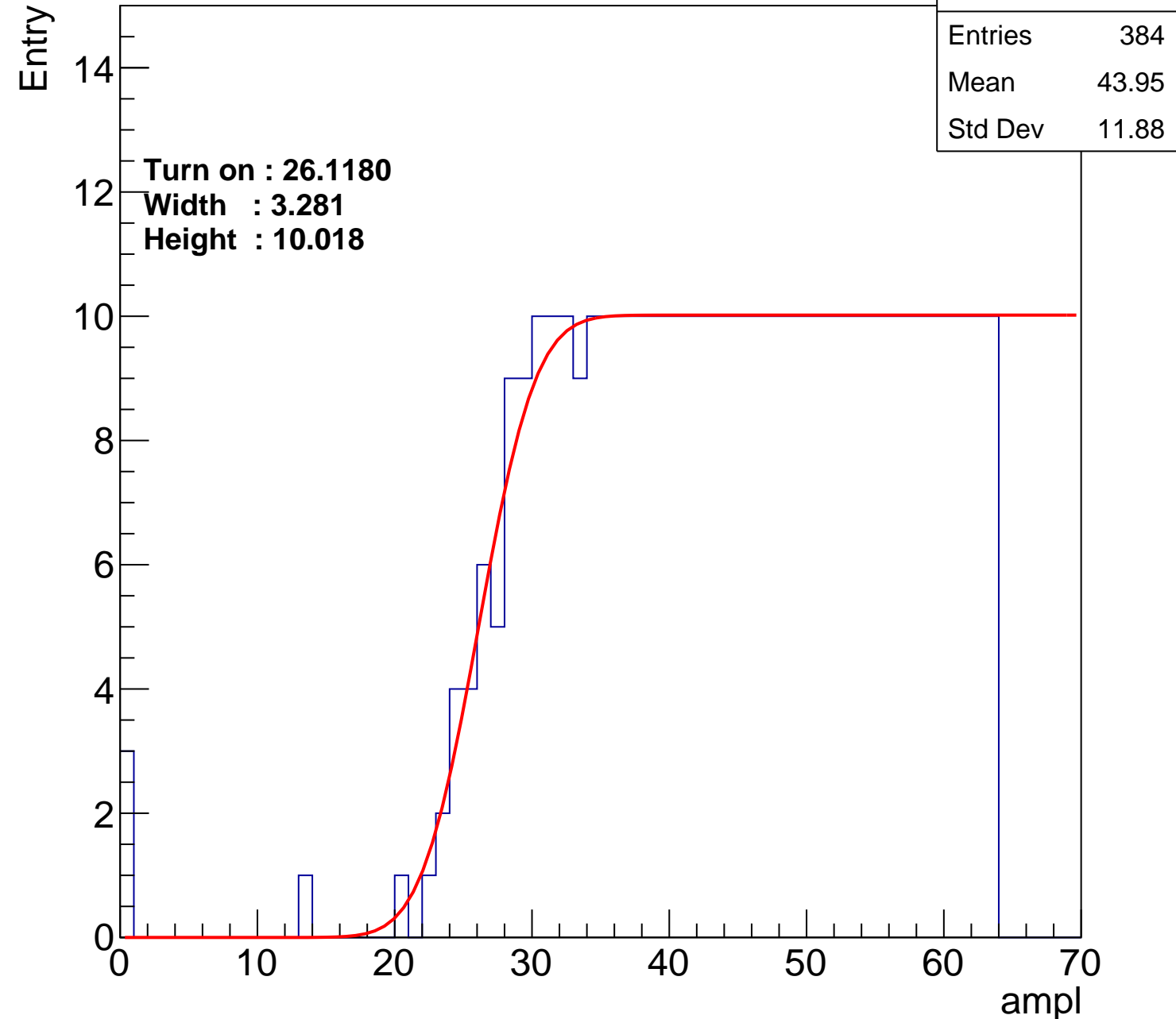
Width : 3.281

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch4

calib_packv5_042523_0143.root, FC#11, port A2

Entries	391
Mean	43.57
Std Dev	12.23

Turn on : 25.7131

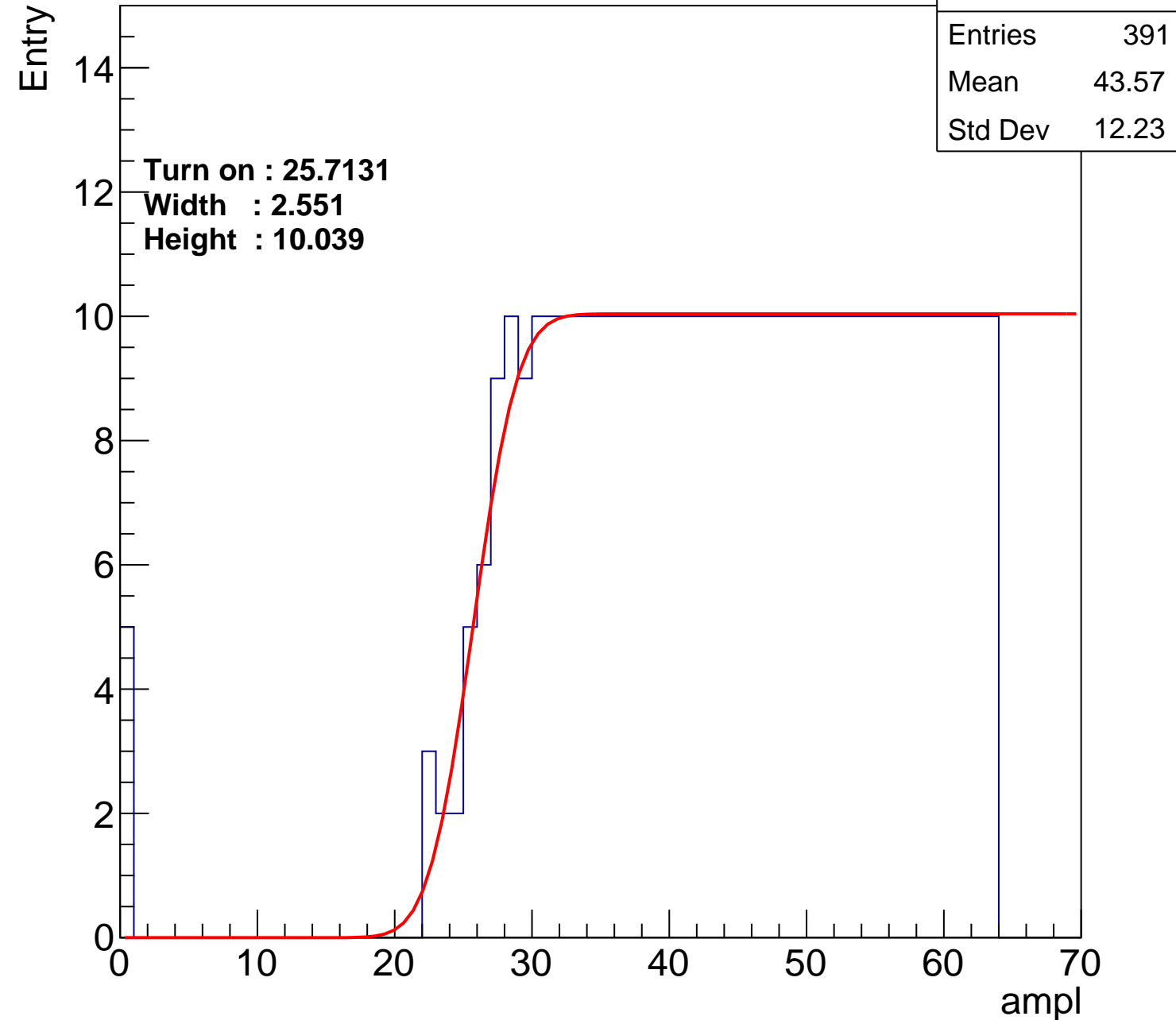
Width : 2.551

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch5

calib_packv5_042523_0143.root, FC#11, port A2

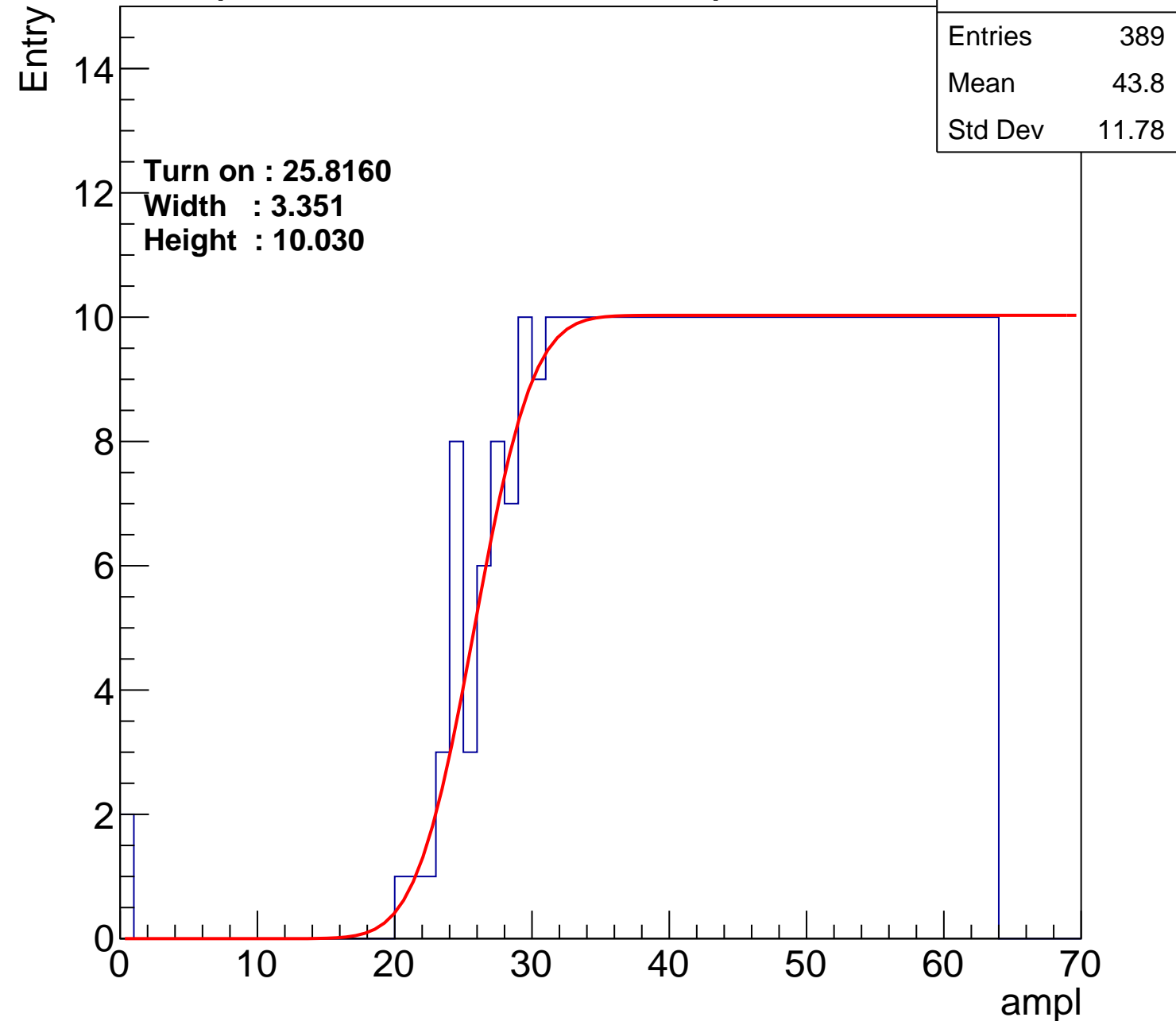
Entry

14
12
10
8
6
4
2
0

Turn on : 25.8160
Width : 3.351
Height : 10.030

Entries	389
Mean	43.8
Std Dev	11.78

ampl



B1L102S, U5-ch6

calib_packv5_042523_0143.root, FC#11, port A2

Entries	373
Mean	44.49
Std Dev	11.61

Turn on : 27.1741

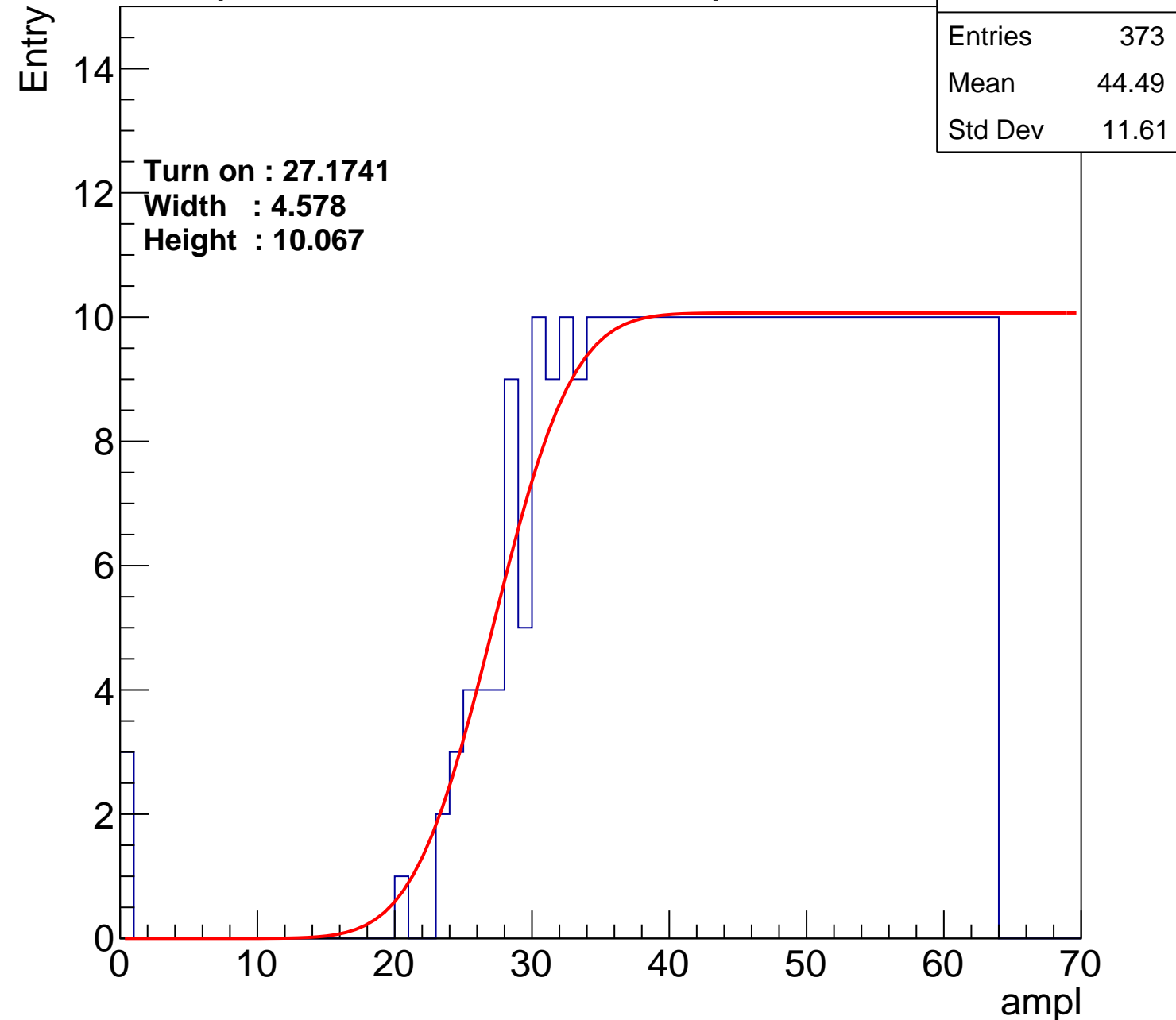
Width : 4.578

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch7

calib_packv5_042523_0143.root, FC#11, port A2

Entries	386
Mean	43.89
Std Dev	11.86

Turn on : 26.7500

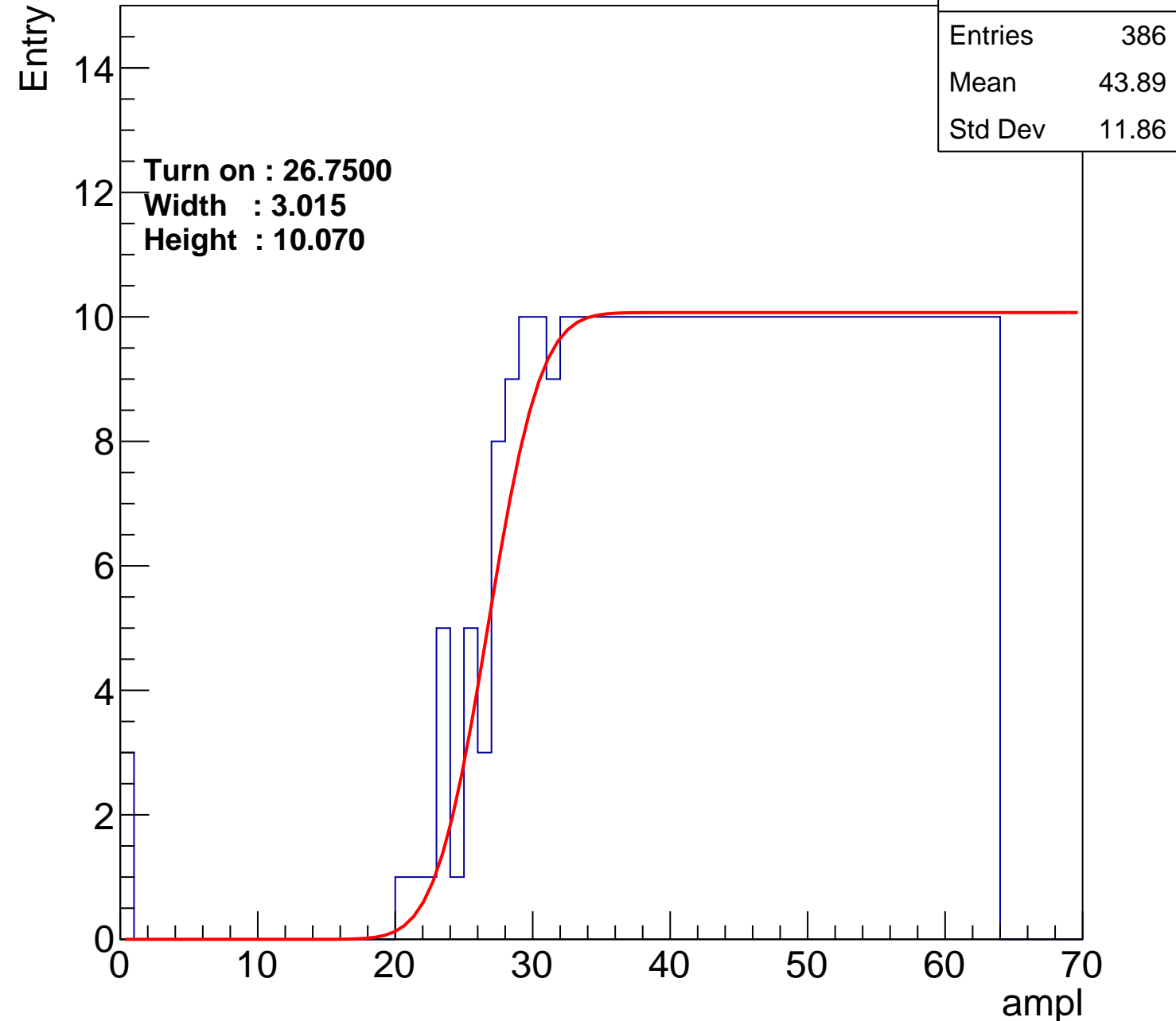
Width : 3.015

Height : 10.070

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch8

calib_packv5_042523_0143.root, FC#11, port A2

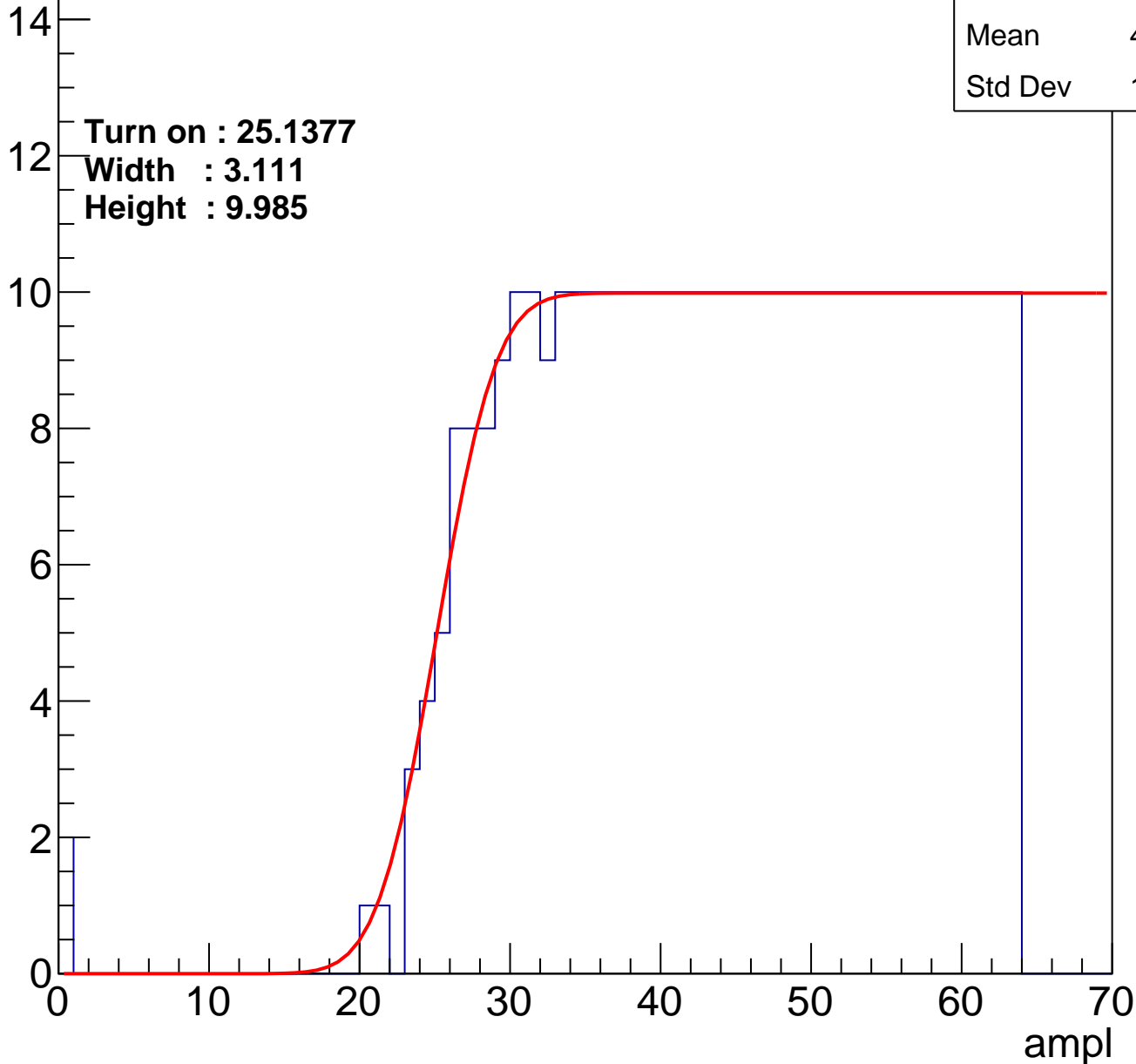
Entries	388
Mean	43.86
Std Dev	11.73

Turn on : 25.1377

Width : 3.111

Height : 9.985

Entry



B1L102S, U5-ch9

calib_packv5_042523_0143.root, FC#11, port A2

Entries	395
Mean	43.36
Std Dev	12.28

Turn on : 25.0604

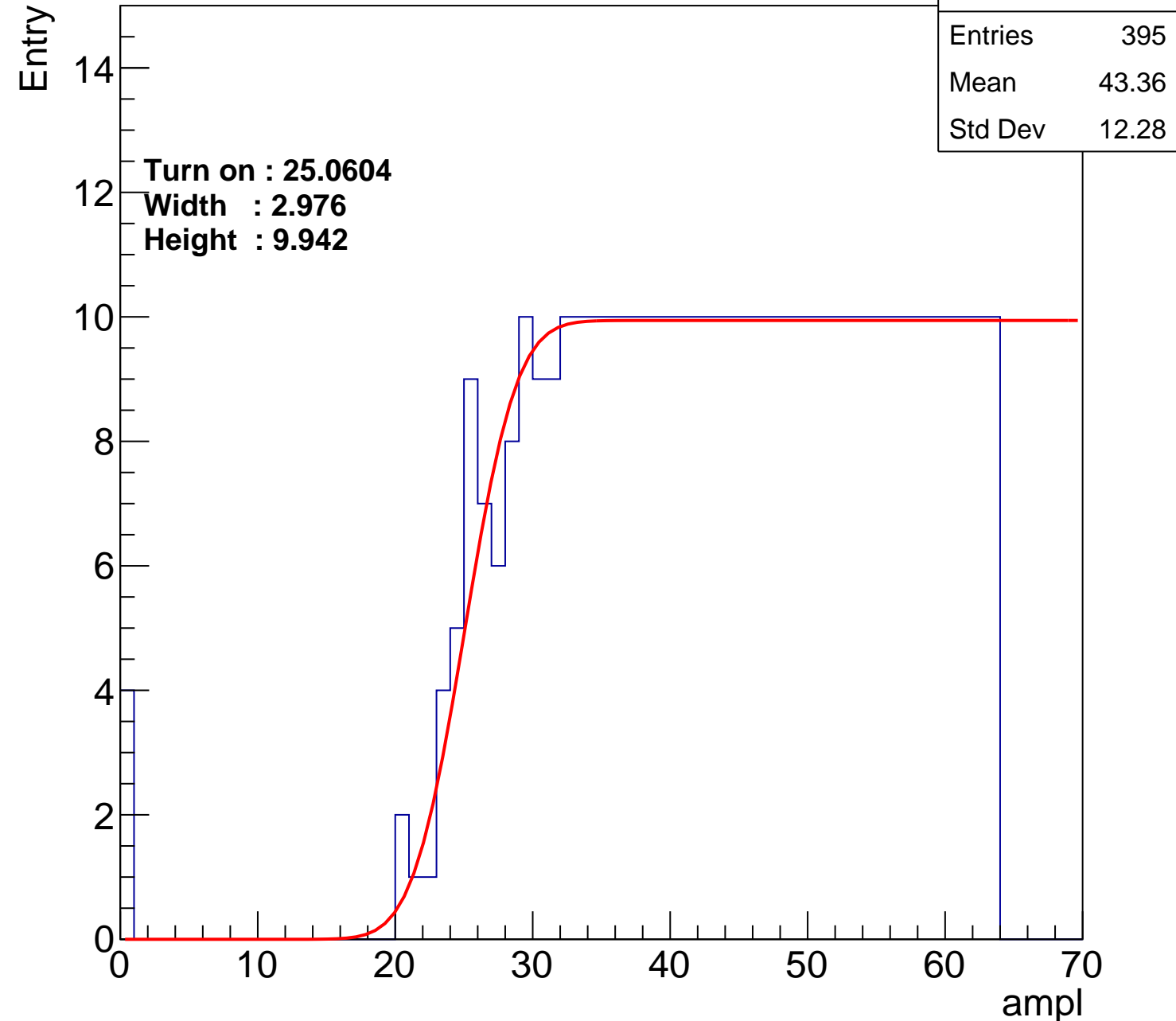
Width : 2.976

Height : 9.942

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch10

calib_packv5_042523_0143.root, FC#11, port A2

Entries	379
Mean	44.39
Std Dev	11.29

Turn on : 26.7537

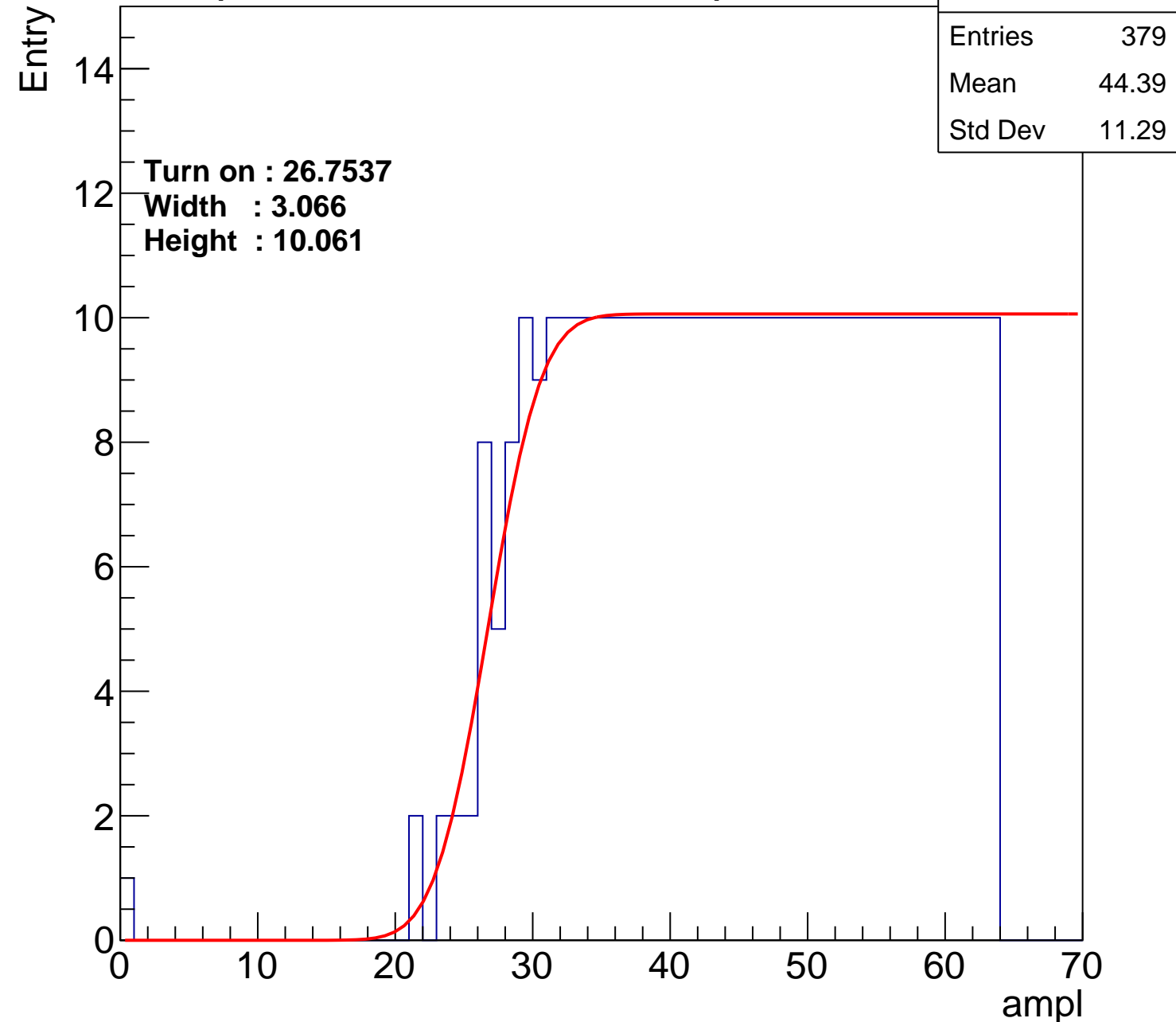
Width : 3.066

Height : 10.061

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch11

calib_packv5_042523_0143.root, FC#11, port A2

Entries	370
Mean	44.73
Std Dev	11.3

Turn on : 27.7099

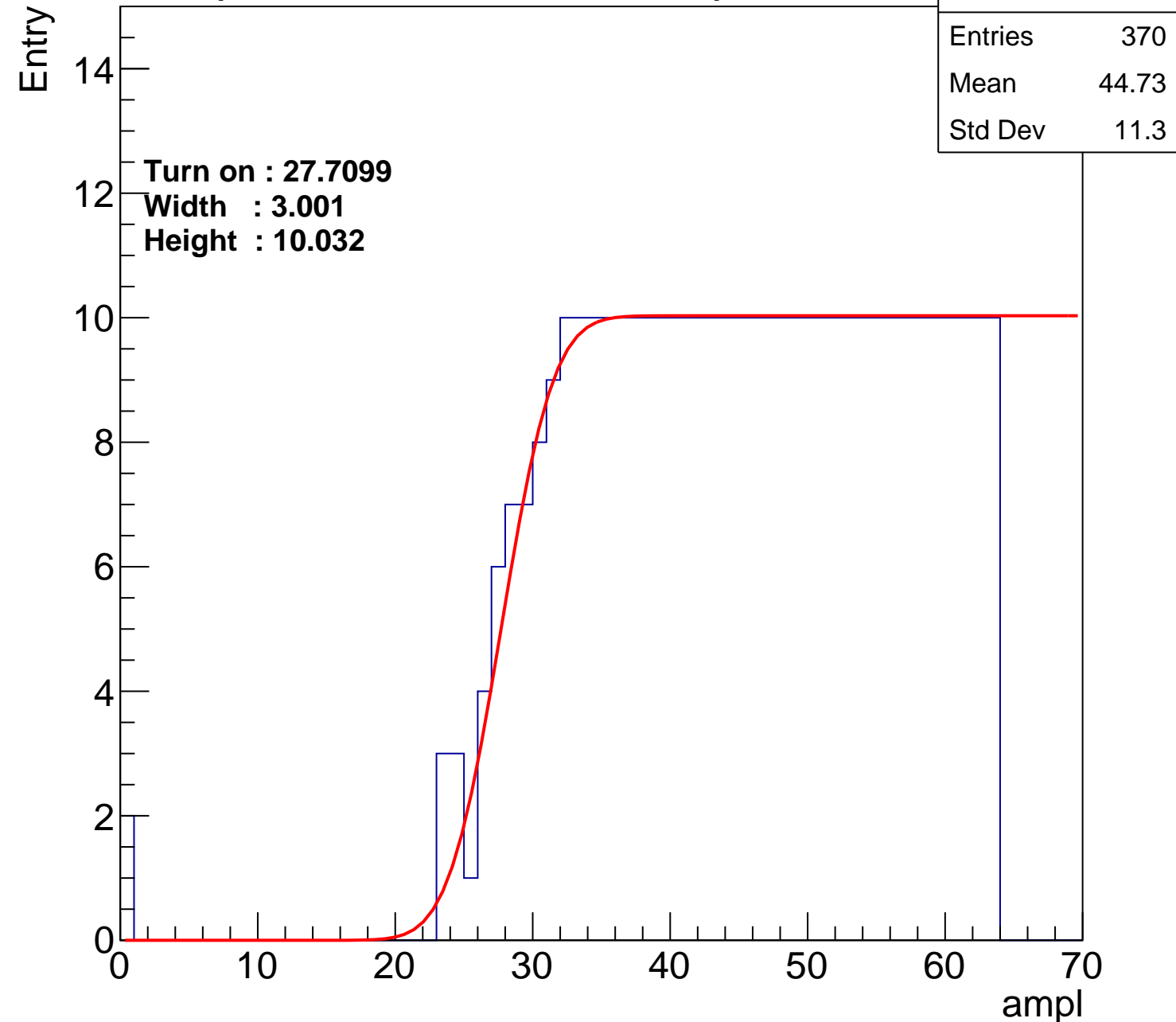
Width : 3.001

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch12

calib_packv5_042523_0143.root, FC#11, port A2

Entries	378
Mean	44.38
Std Dev	11.34

Turn on : 26.3778

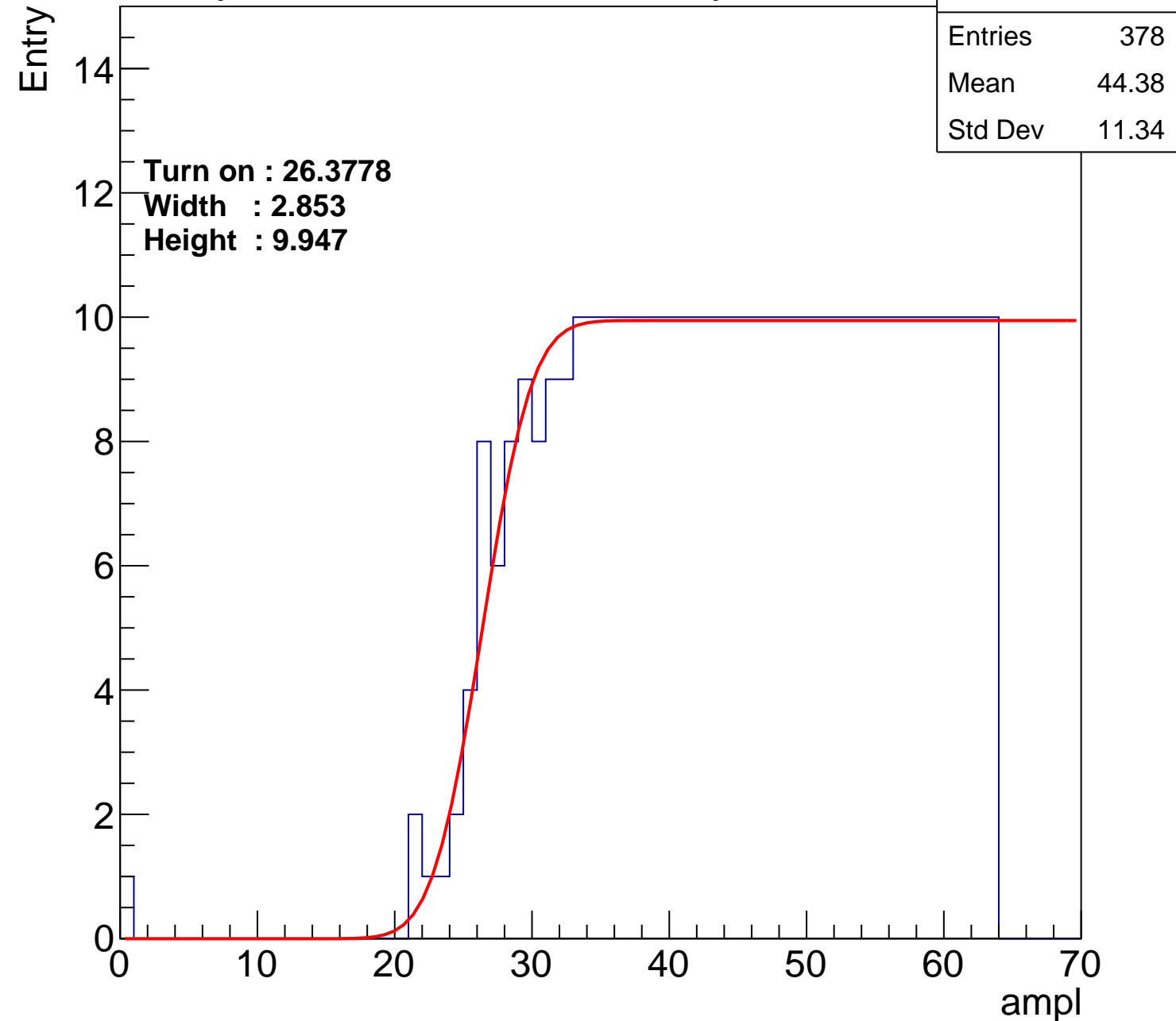
Width : 2.853

Height : 9.947

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch13

calib_packv5_042523_0143.root, FC#11, port A2

Entries	367
Mean	44.94
Std Dev	11.04

Turn on : 27.7211

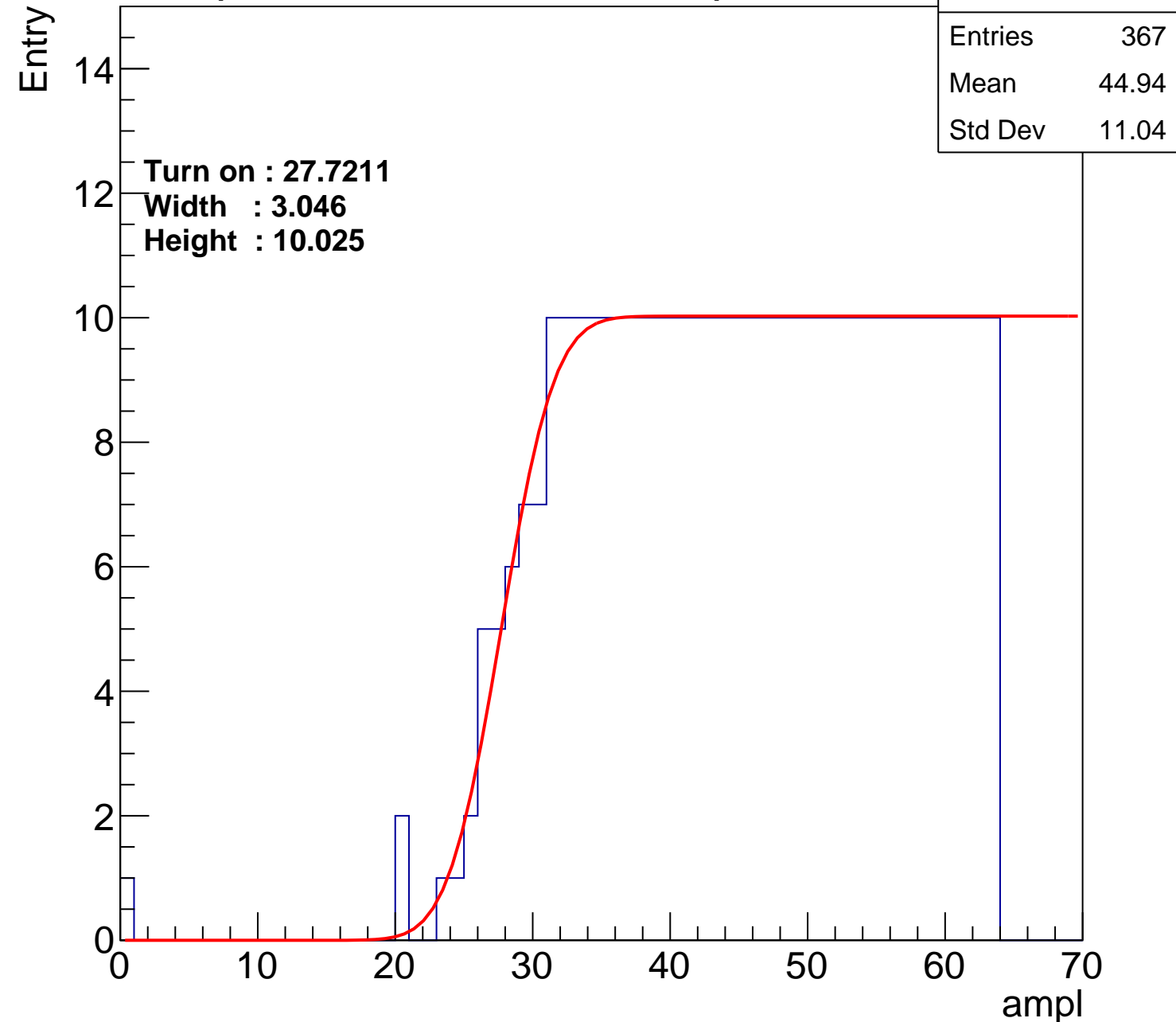
Width : 3.046

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch14

calib_packv5_042523_0143.root, FC#11, port A2

Entries	367
Mean	45.02
Std Dev	10.9

Turn on : 27.3420

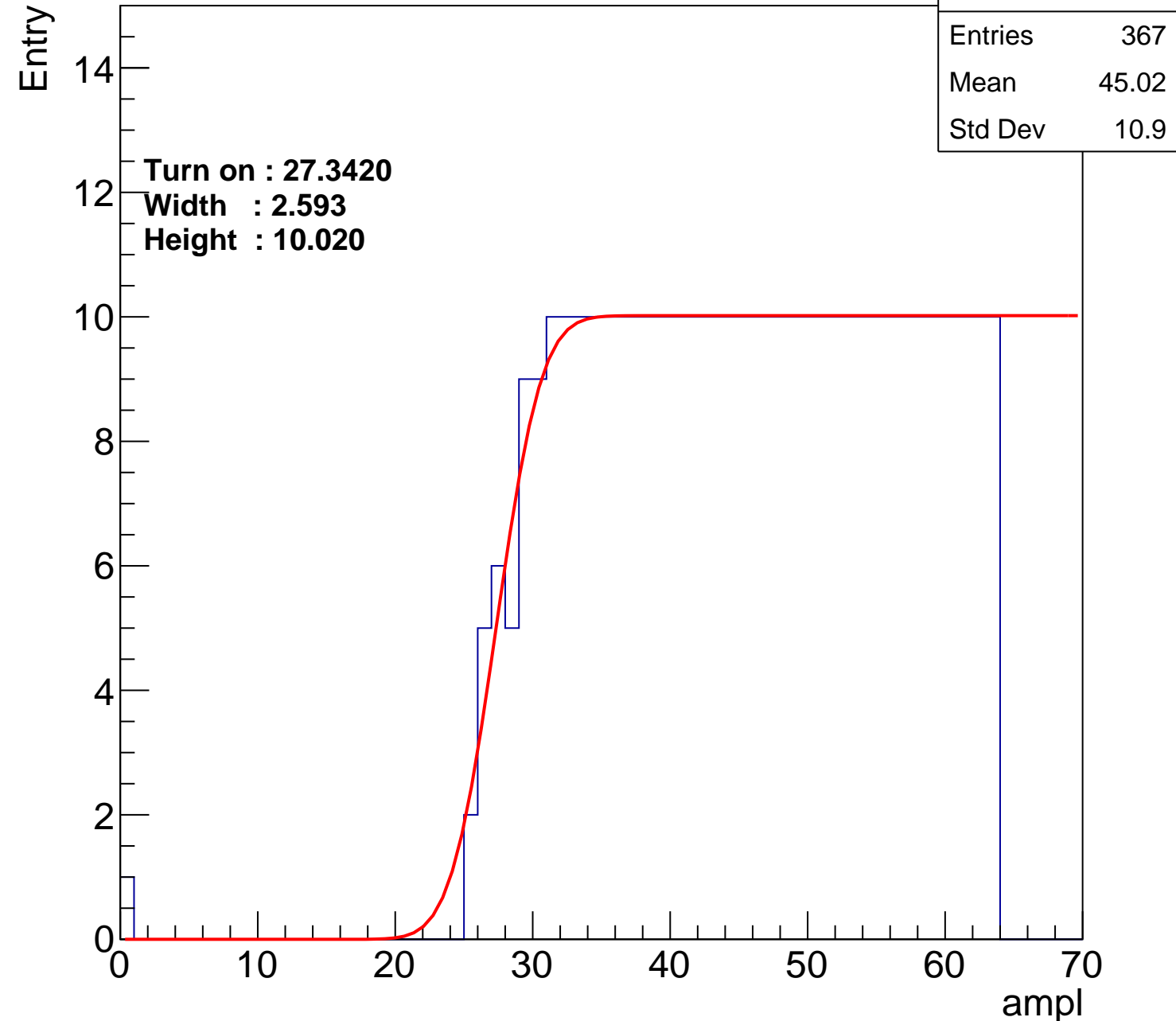
Width : 2.593

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch15

calib_packv5_042523_0143.root, FC#11, port A2

Entries	384
Mean	44.04
Std Dev	11.73

Turn on : 25.7253

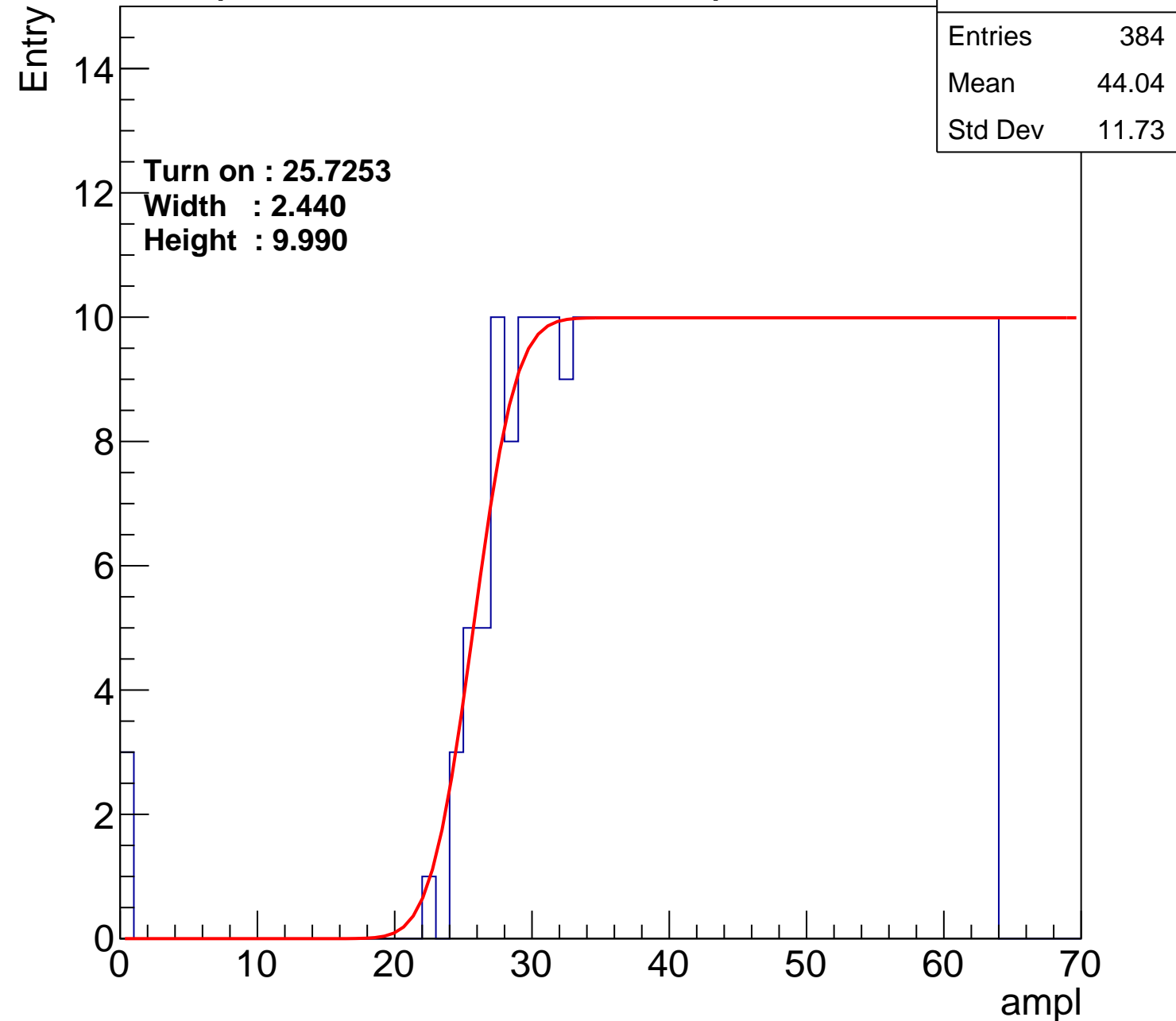
Width : 2.440

Height : 9.990

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch16

calib_packv5_042523_0143.root, FC#11, port A2

Entries	397
Mean	43.43
Std Dev	11.96

Turn on : 24.9015

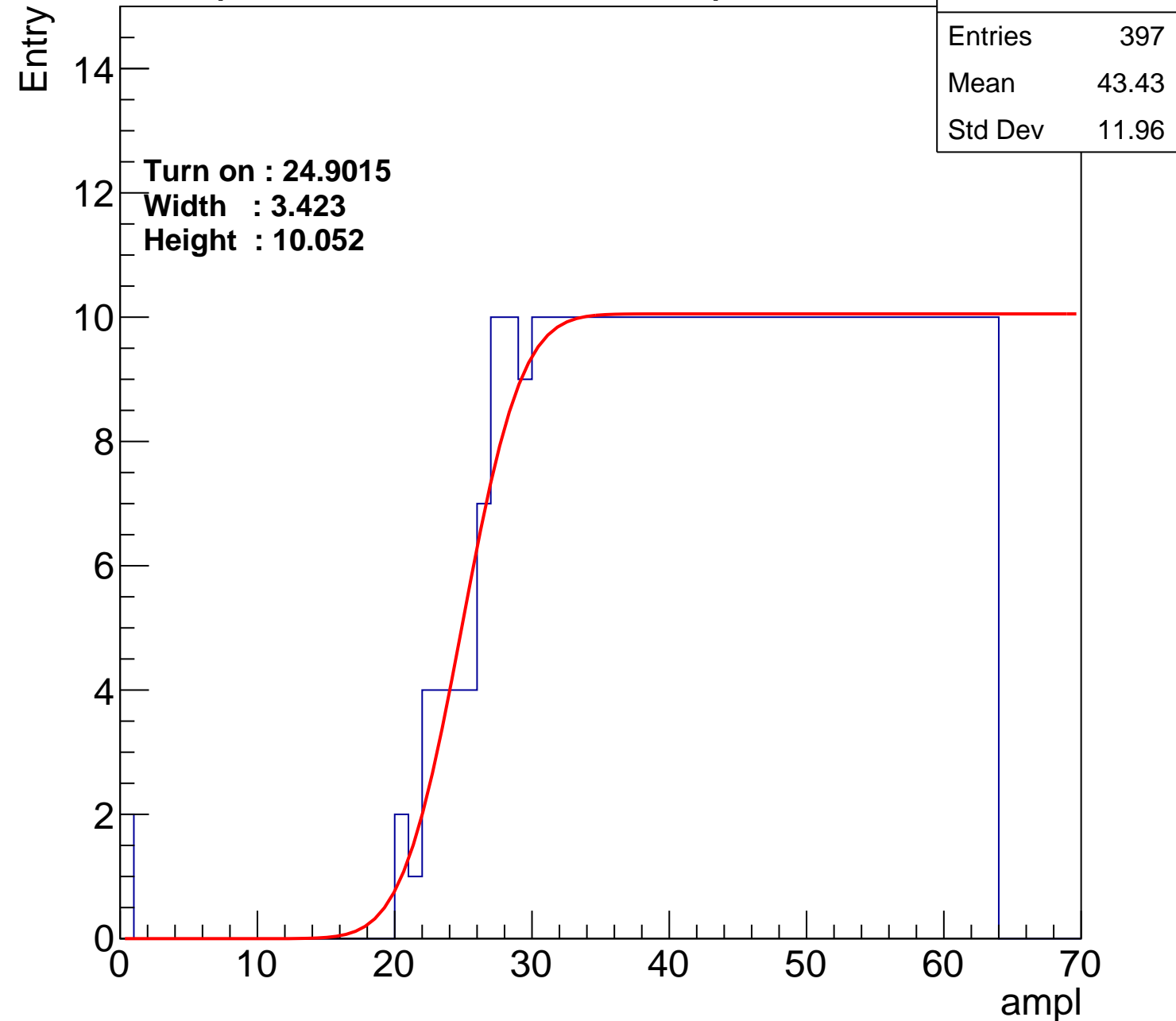
Width : 3.423

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch17

calib_packv5_042523_0143.root, FC#11, port A2

Entries	375
Mean	44.46
Std Dev	11.55

Turn on : 27.2218

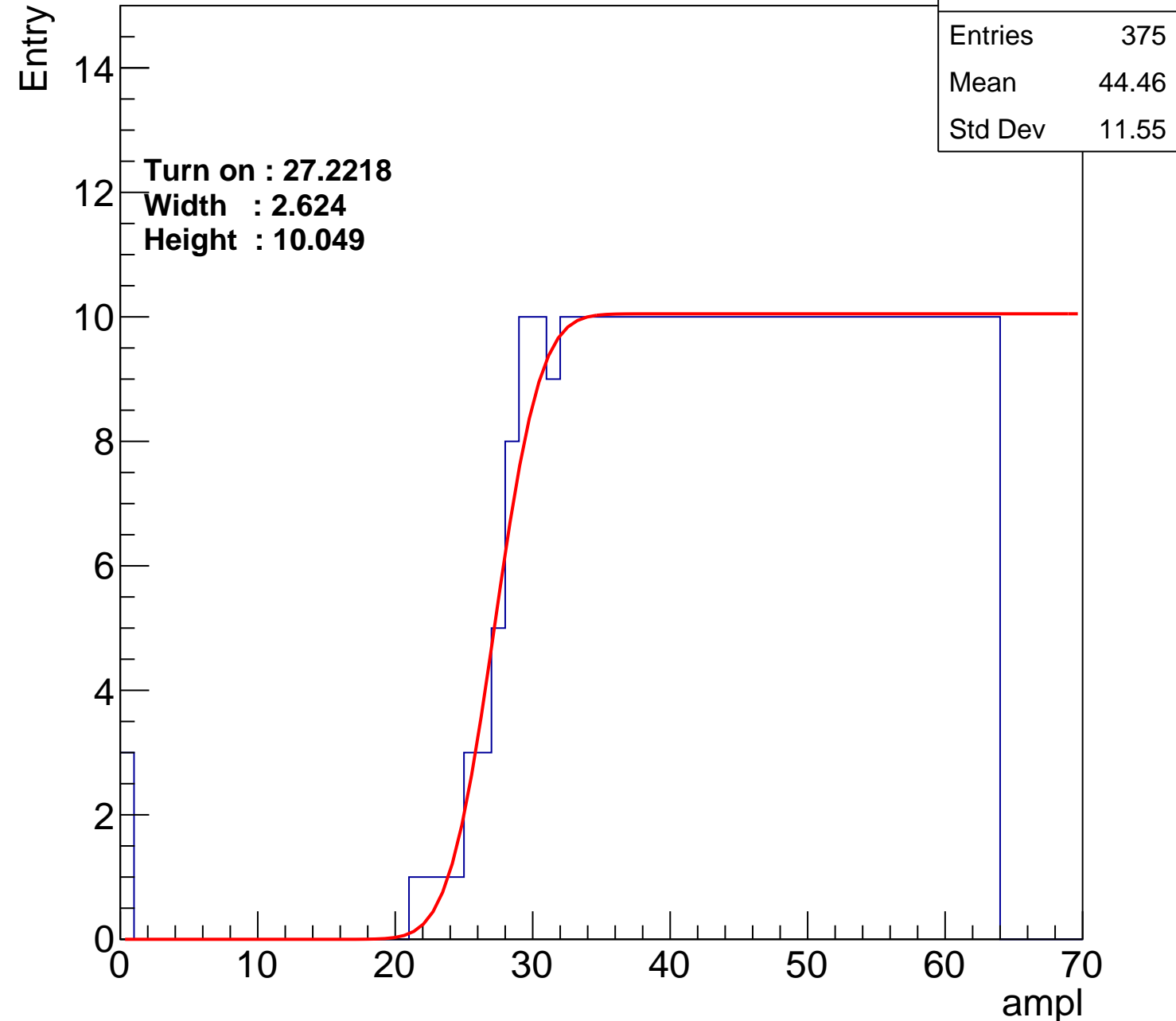
Width : 2.624

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch18

calib_packv5_042523_0143.root, FC#11, port A2

Entries	381
Mean	44.14
Std Dev	11.65

Turn on : 26.8875

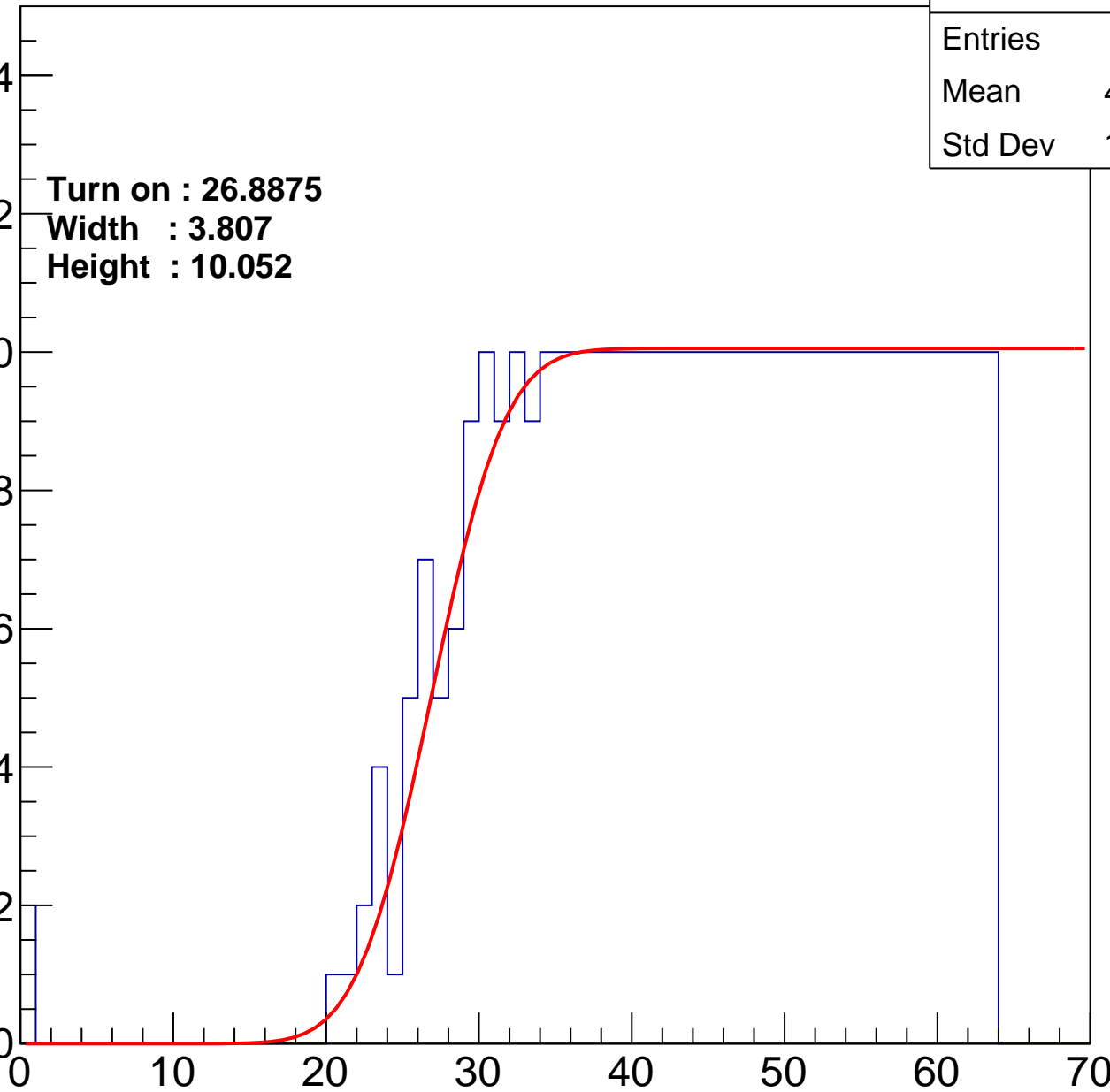
Width : 3.807

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch19

calib_packv5_042523_0143.root, FC#11, port A2

Entries	382
Mean	44.15
Std Dev	11.59

Turn on : 26.5948

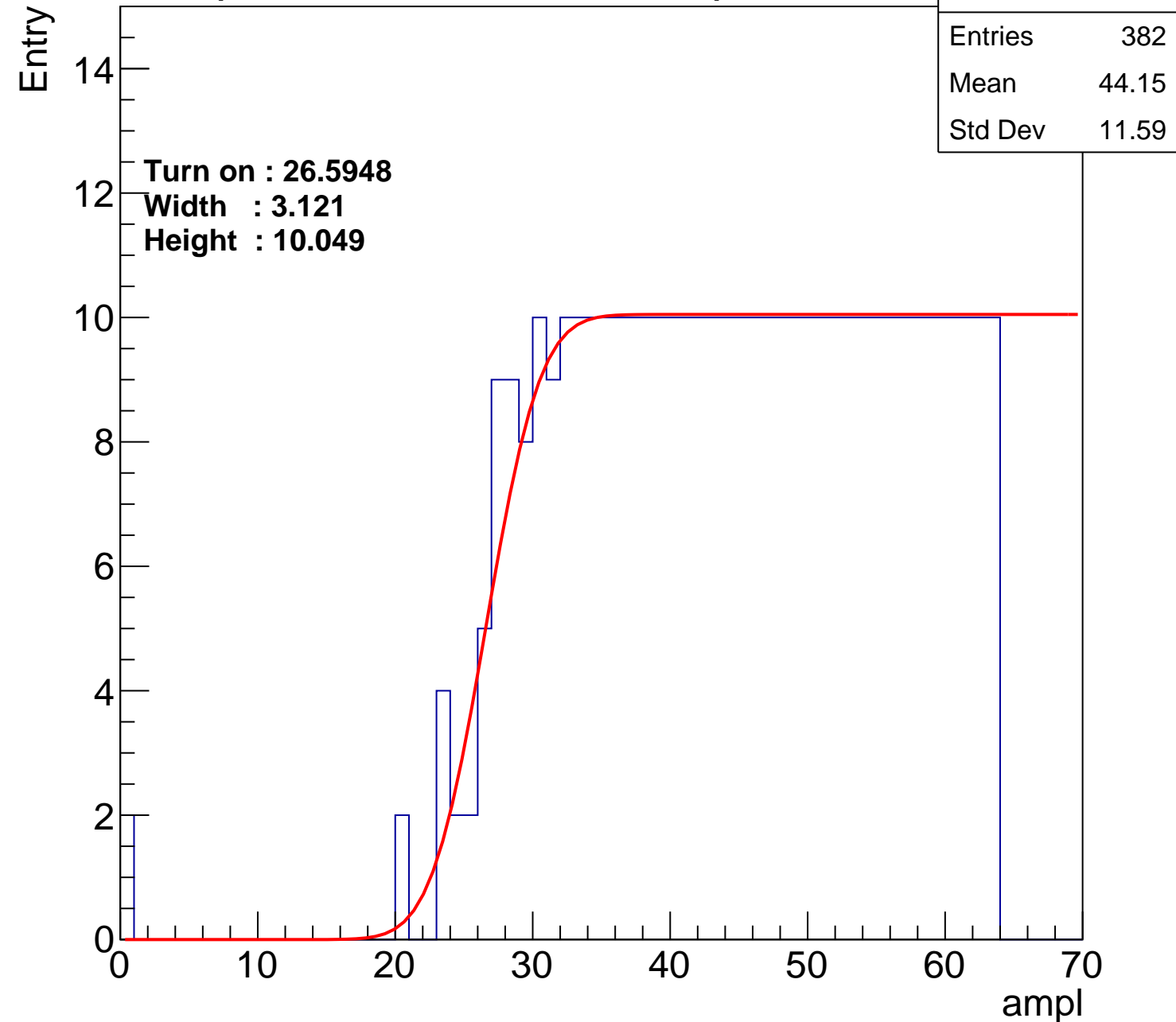
Width : 3.121

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch20

calib_packv5_042523_0143.root, FC#11, port A2

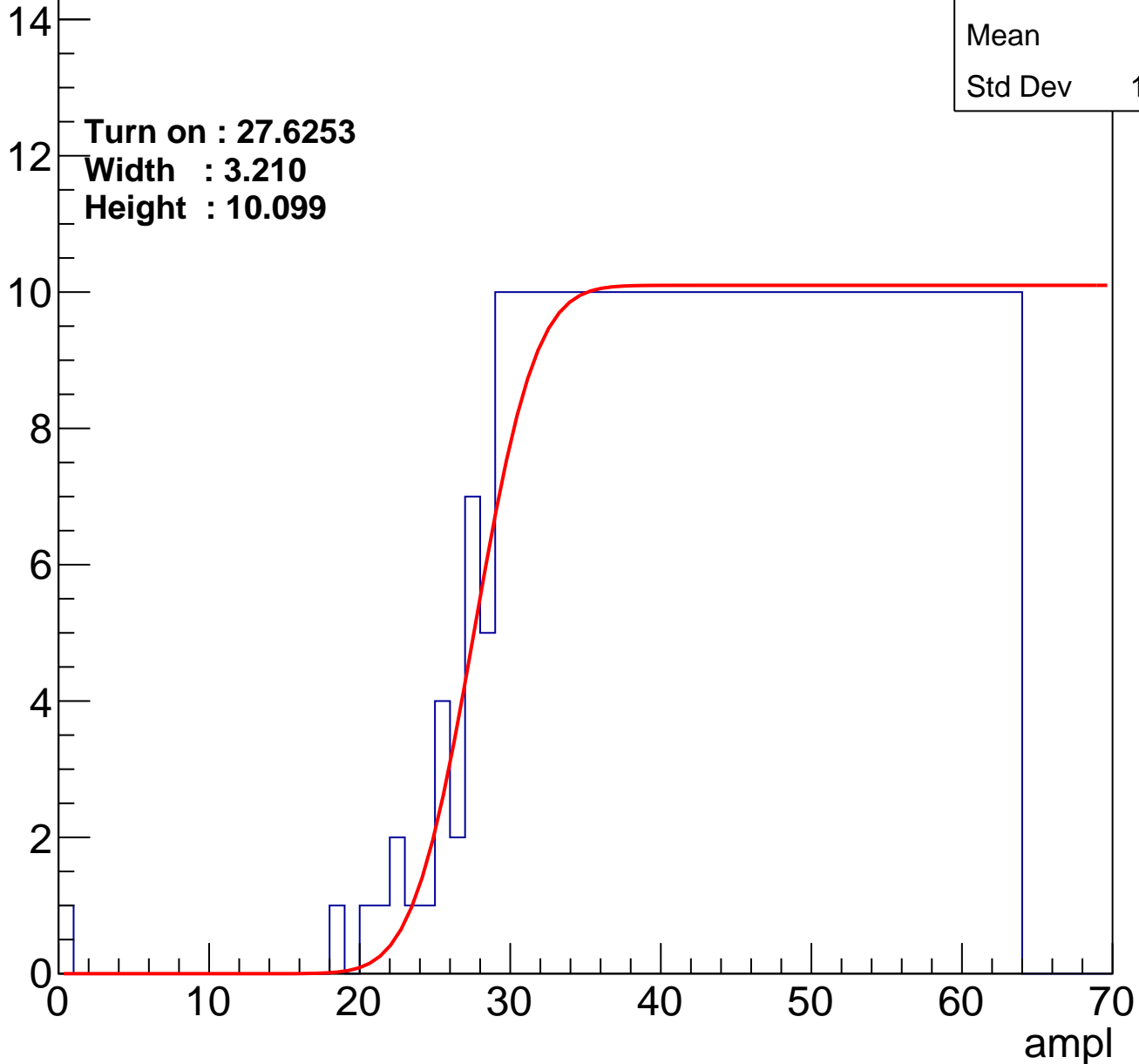
Entries	376
Mean	44.5
Std Dev	11.29

Turn on : 27.6253

Width : 3.210

Height : 10.099

Entry



B1L102S, U5-ch21

calib_packv5_042523_0143.root, FC#11, port A2

Entries	367
Mean	44.73
Std Dev	11.63

Turn on : 28.2567

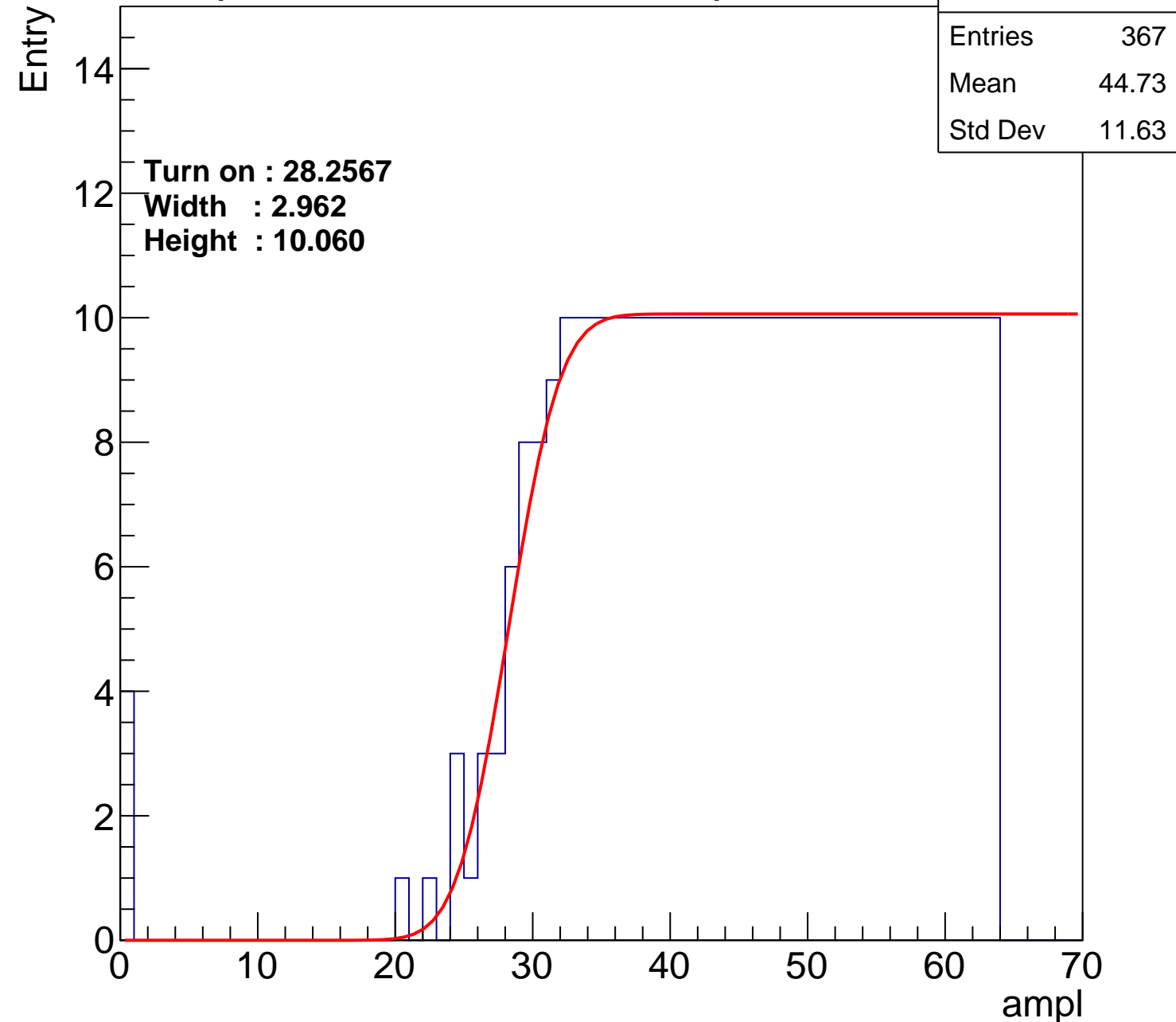
Width : 2.962

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch22

calib_packv5_042523_0143.root, FC#11, port A2

Entries	391
Mean	43.65
Std Dev	11.91

Turn on : 25.1730

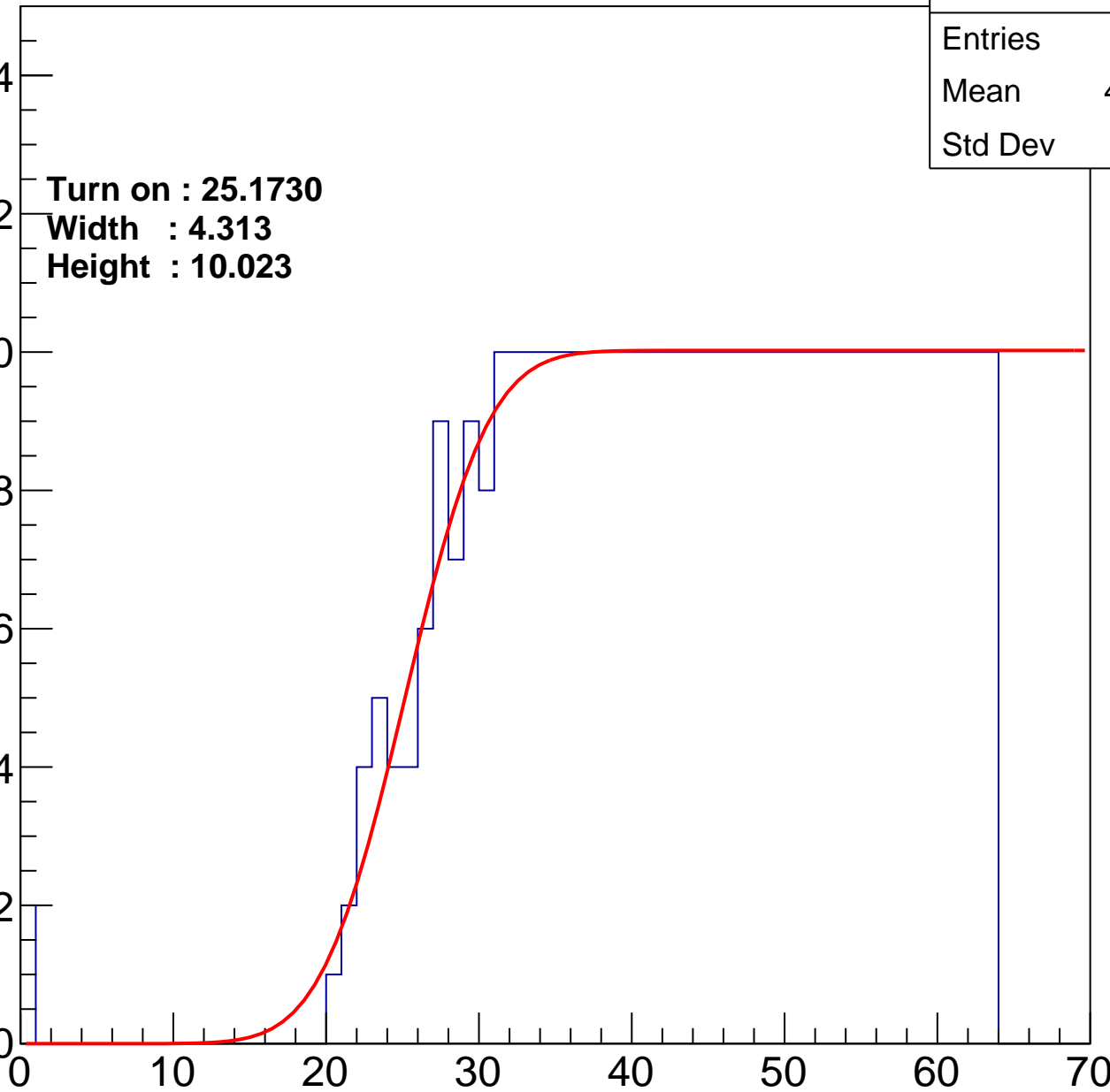
Width : 4.313

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch23

calib_packv5_042523_0143.root, FC#11, port A2

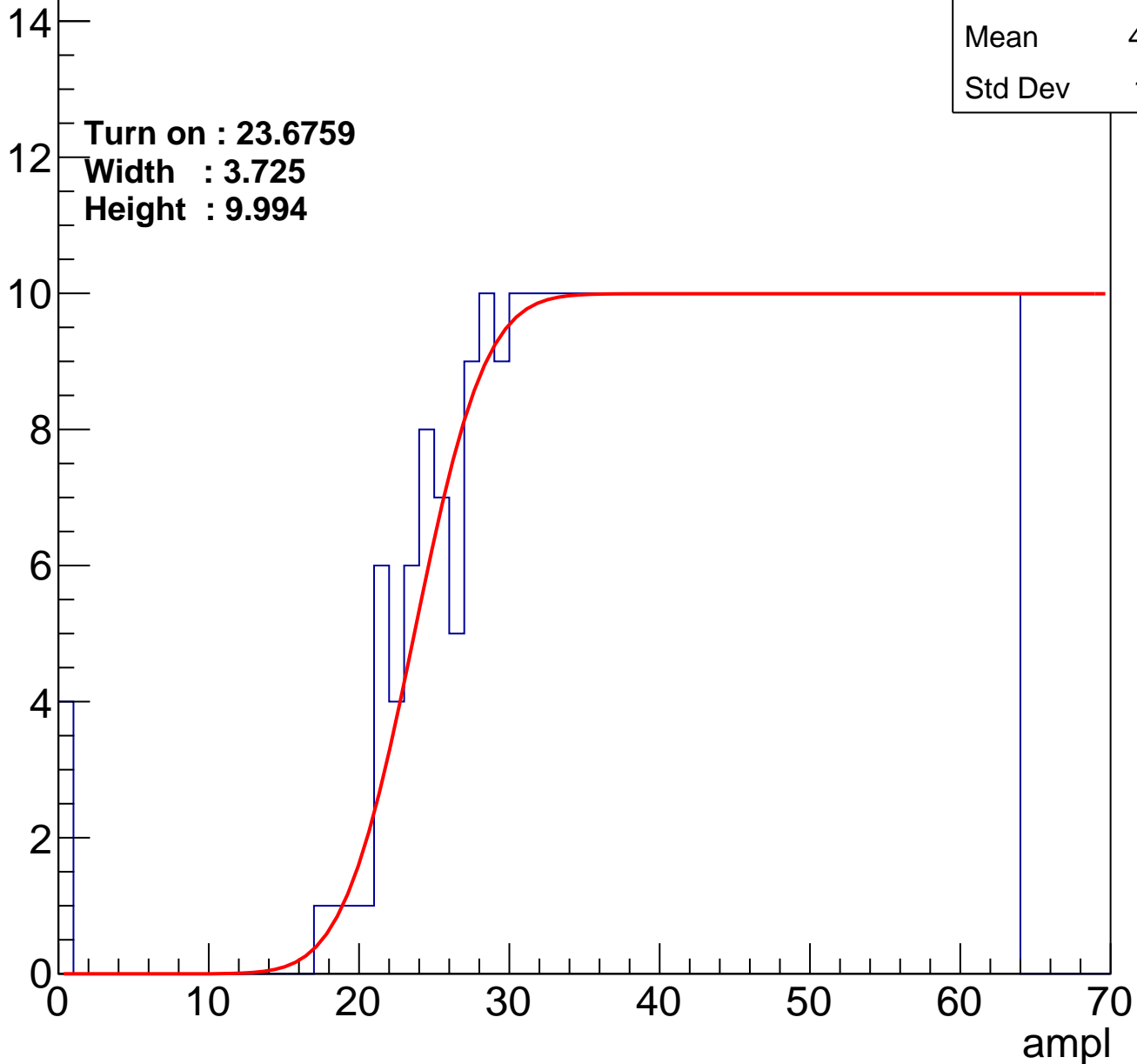
Entries	412
Mean	42.52
Std Dev	12.71

Turn on : 23.6759

Width : 3.725

Height : 9.994

Entry



B1L102S, U5-ch24

calib_packv5_042523_0143.root, FC#11, port A2

Entries	410
Mean	42.52
Std Dev	12.96

Turn on : 23.5935

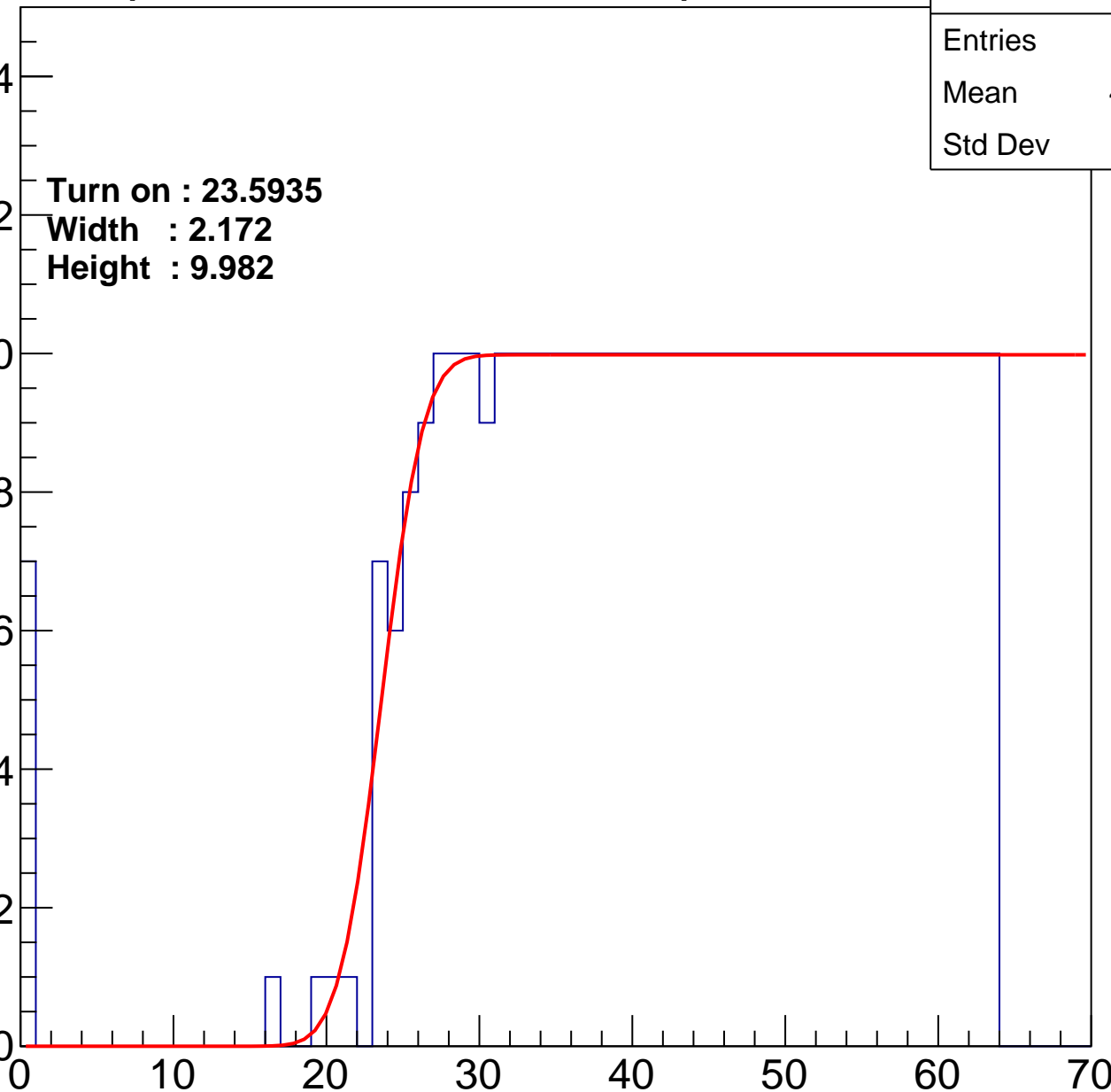
Width : 2.172

Height : 9.982

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch25

calib_packv5_042523_0143.root, FC#11, port A2

Entries	358
Mean	45.31
Std Dev	11

Turn on : 27.9738

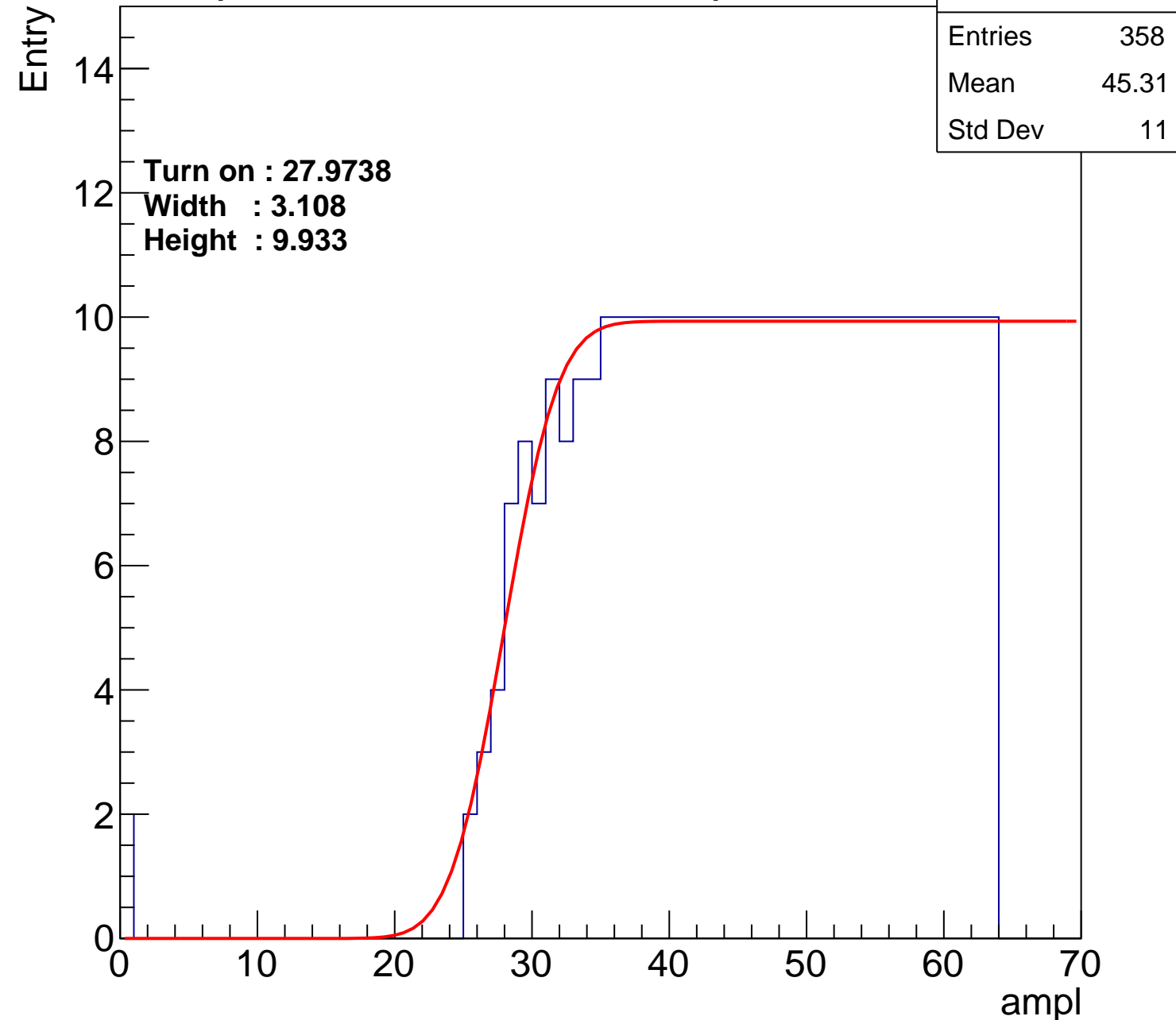
Width : 3.108

Height : 9.933

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch26

calib_packv5_042523_0143.root, FC#11, port A2

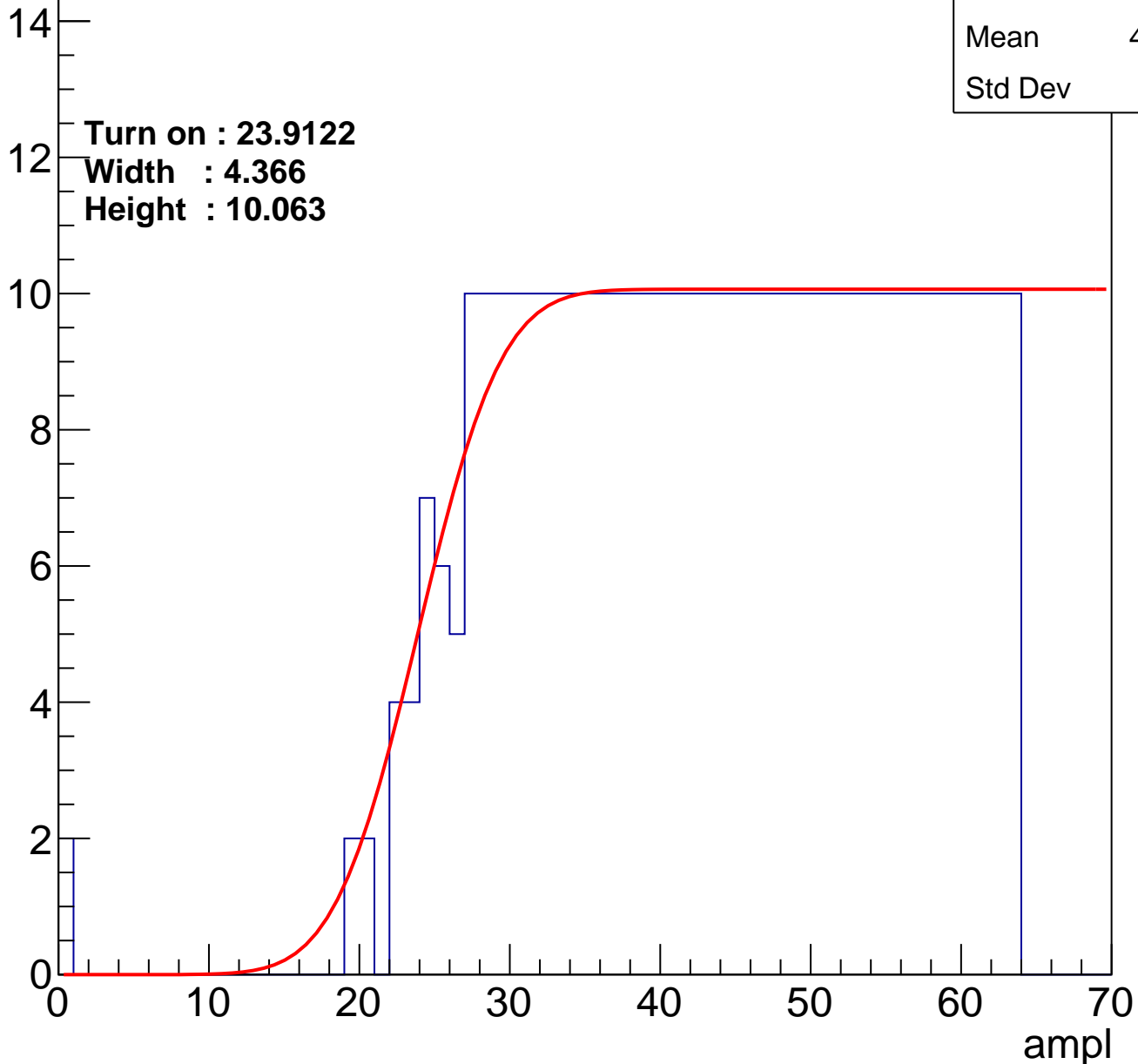
Entries	402
Mean	43.17
Std Dev	12.1

Turn on : 23.9122

Width : 4.366

Height : 10.063

Entry



B1L102S, U5-ch27

calib_packv5_042523_0143.root, FC#11, port A2

Entries	403
Mean	43.13
Std Dev	12.12

Turn on : 24.1662

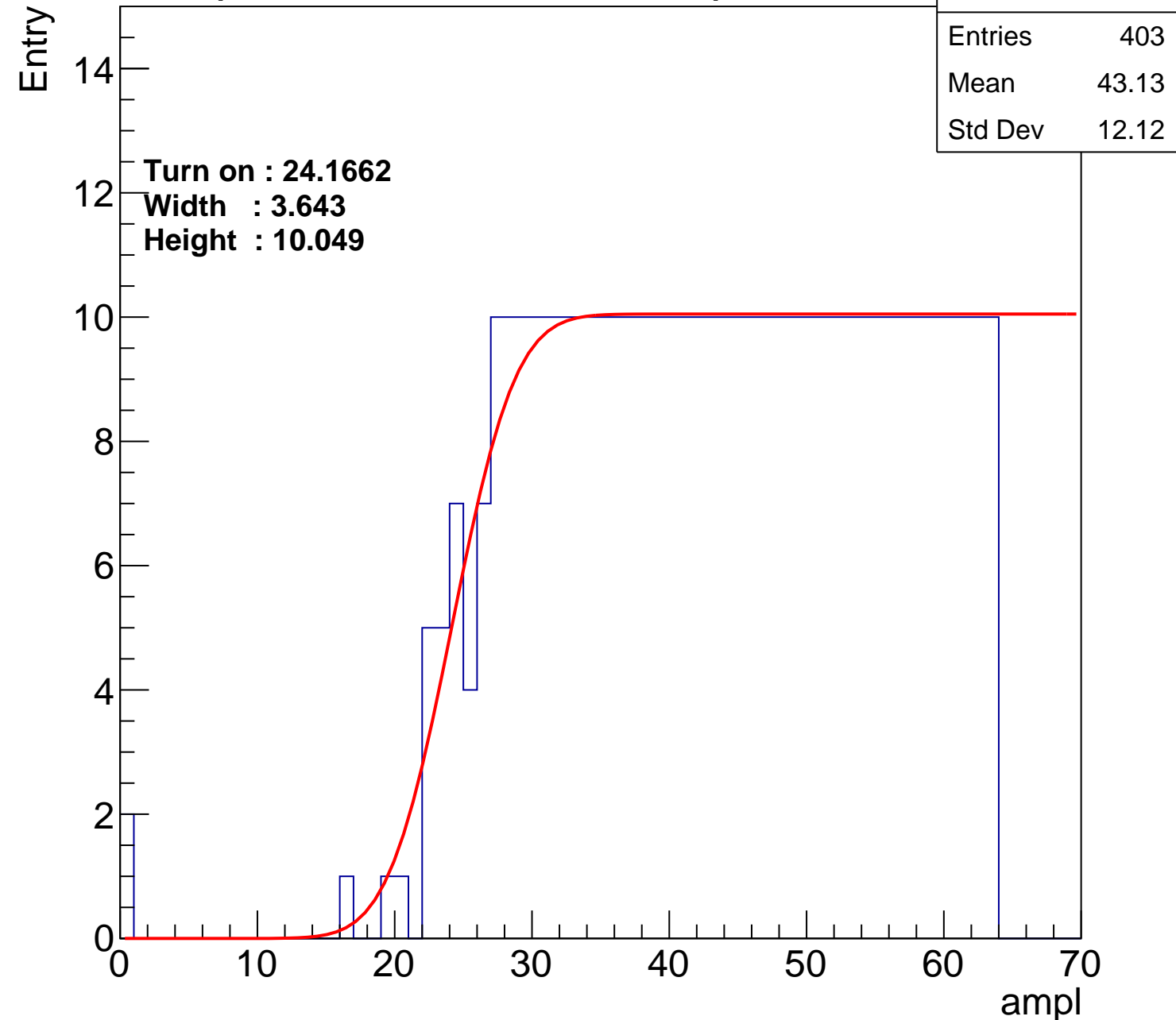
Width : 3.643

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch28

calib_packv5_042523_0143.root, FC#11, port A2

Entries	378
Mean	44.32
Std Dev	11.6

Turn on : 26.8308

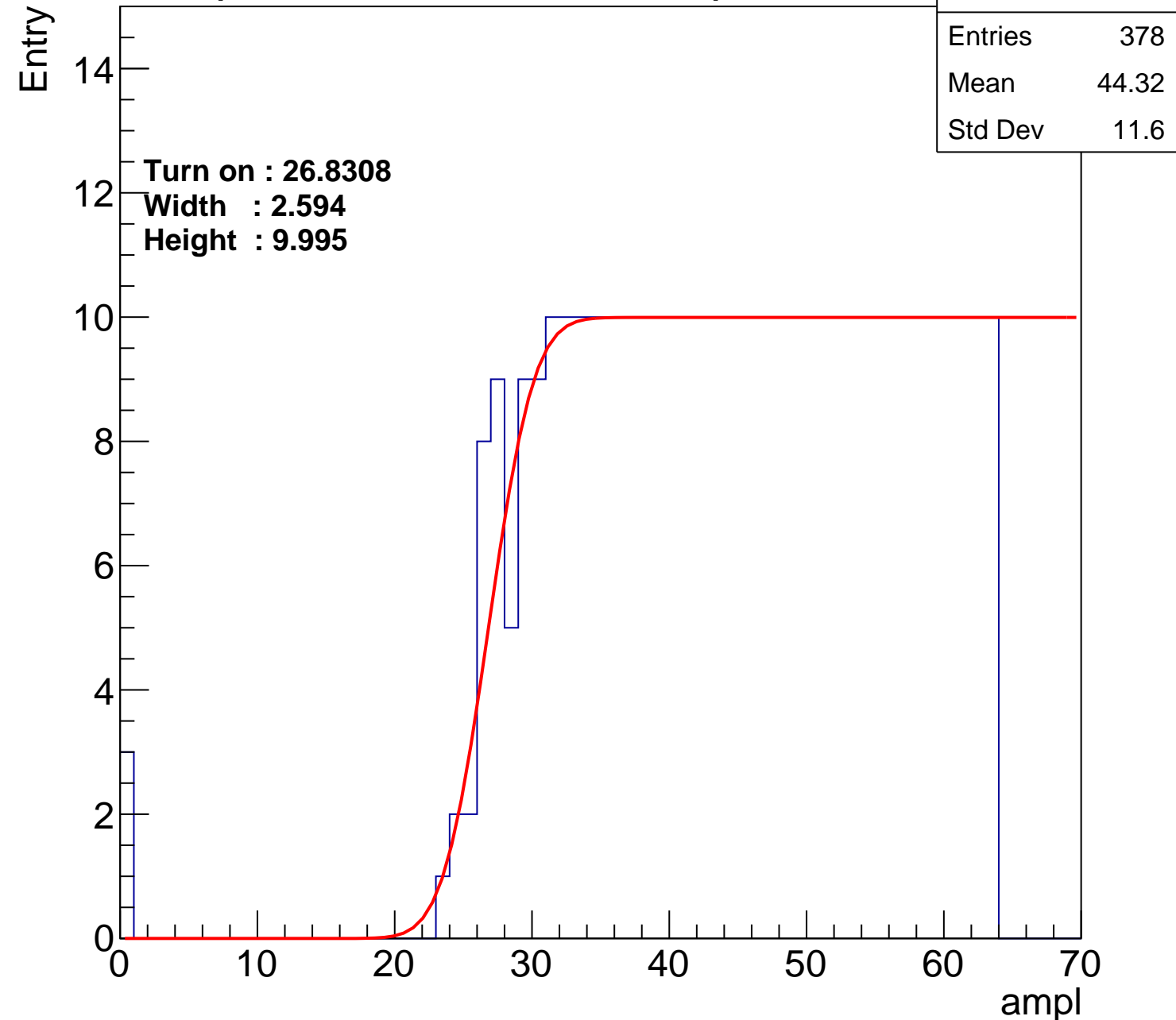
Width : 2.594

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch29

calib_packv5_042523_0143.root, FC#11, port A2

Entries	384
Mean	44.03
Std Dev	11.7

Turn on : 26.7861

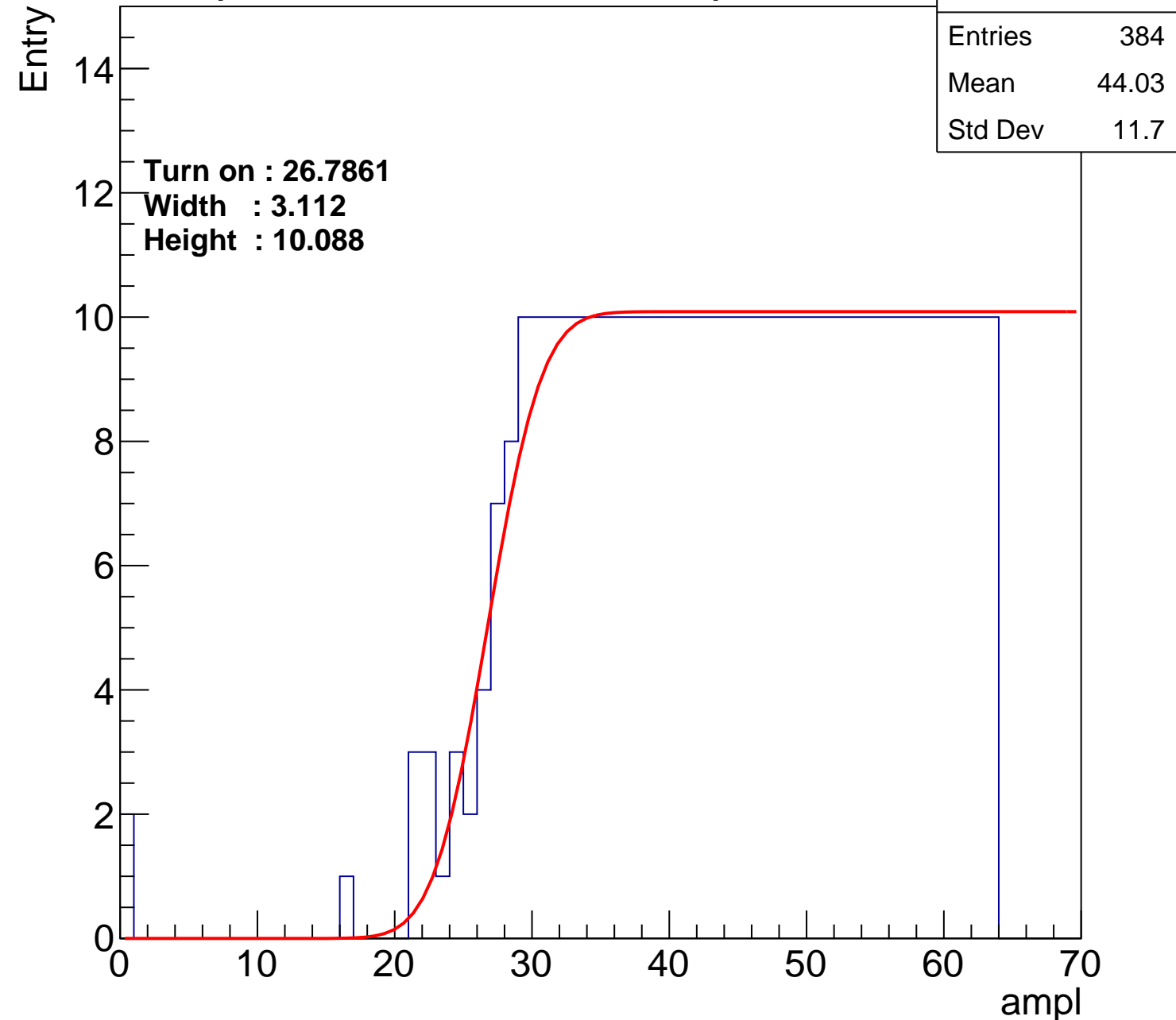
Width : 3.112

Height : 10.088

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch30

calib_packv5_042523_0143.root, FC#11, port A2

Entries	365
Mean	44.98
Std Dev	11.16

Turn on : 27.8889

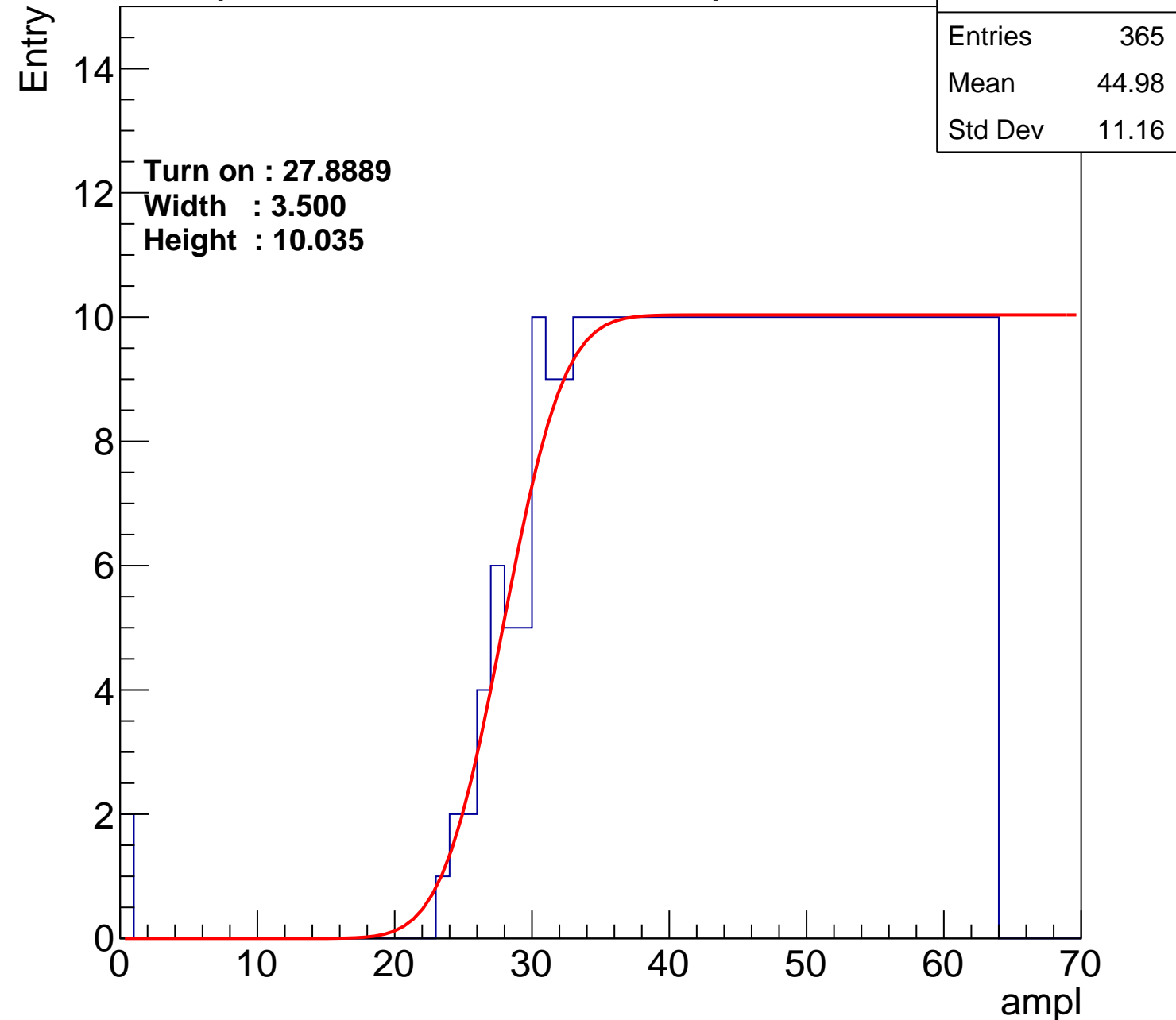
Width : 3.500

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch31

calib_packv5_042523_0143.root, FC#11, port A2

Entries	390
Mean	43.77
Std Dev	11.78

Turn on : 25.6734

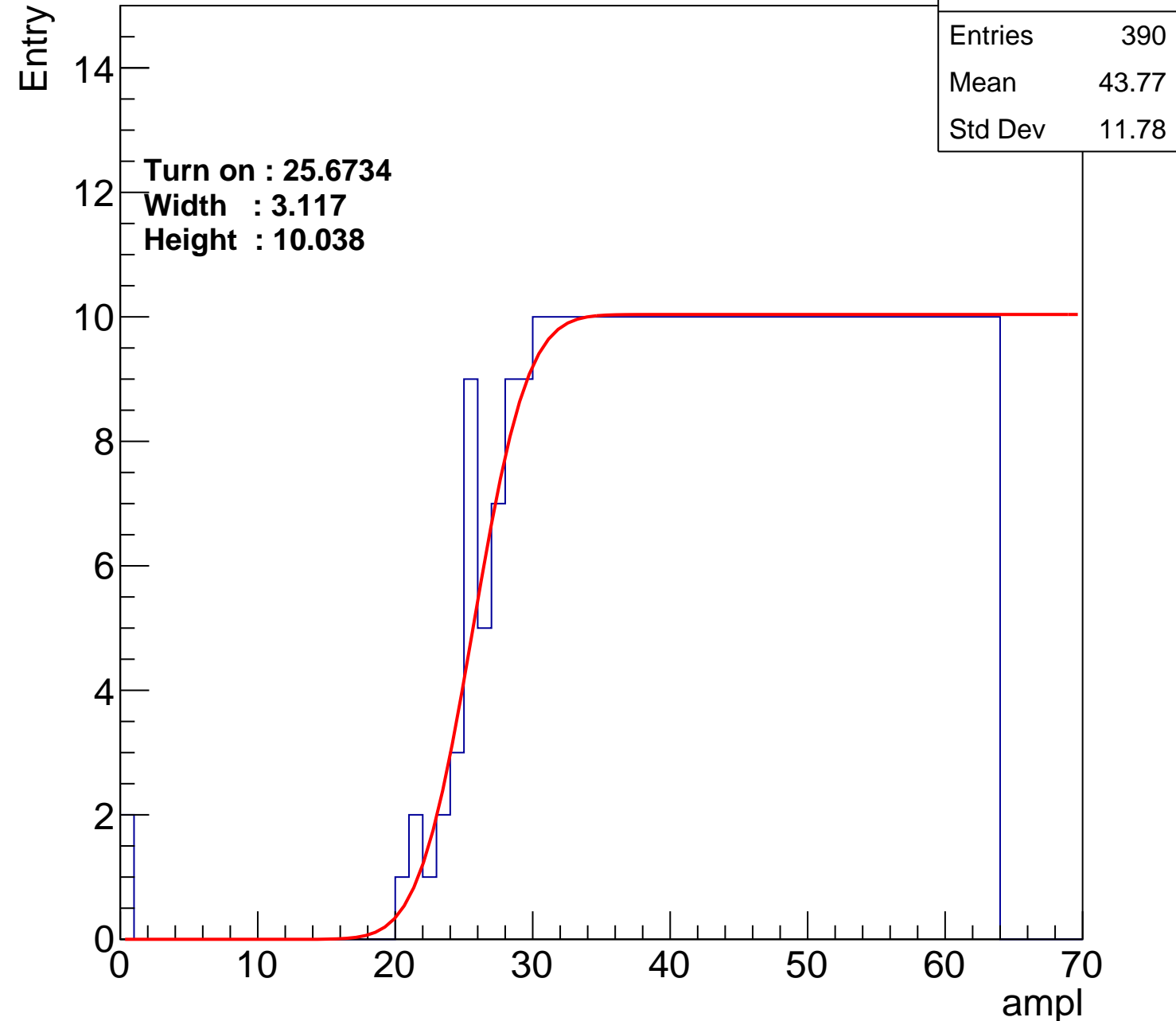
Width : 3.117

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch32

calib_packv5_042523_0143.root, FC#11, port A2

Entries	386
Mean	43.92
Std Dev	11.74

Turn on : 25.3454

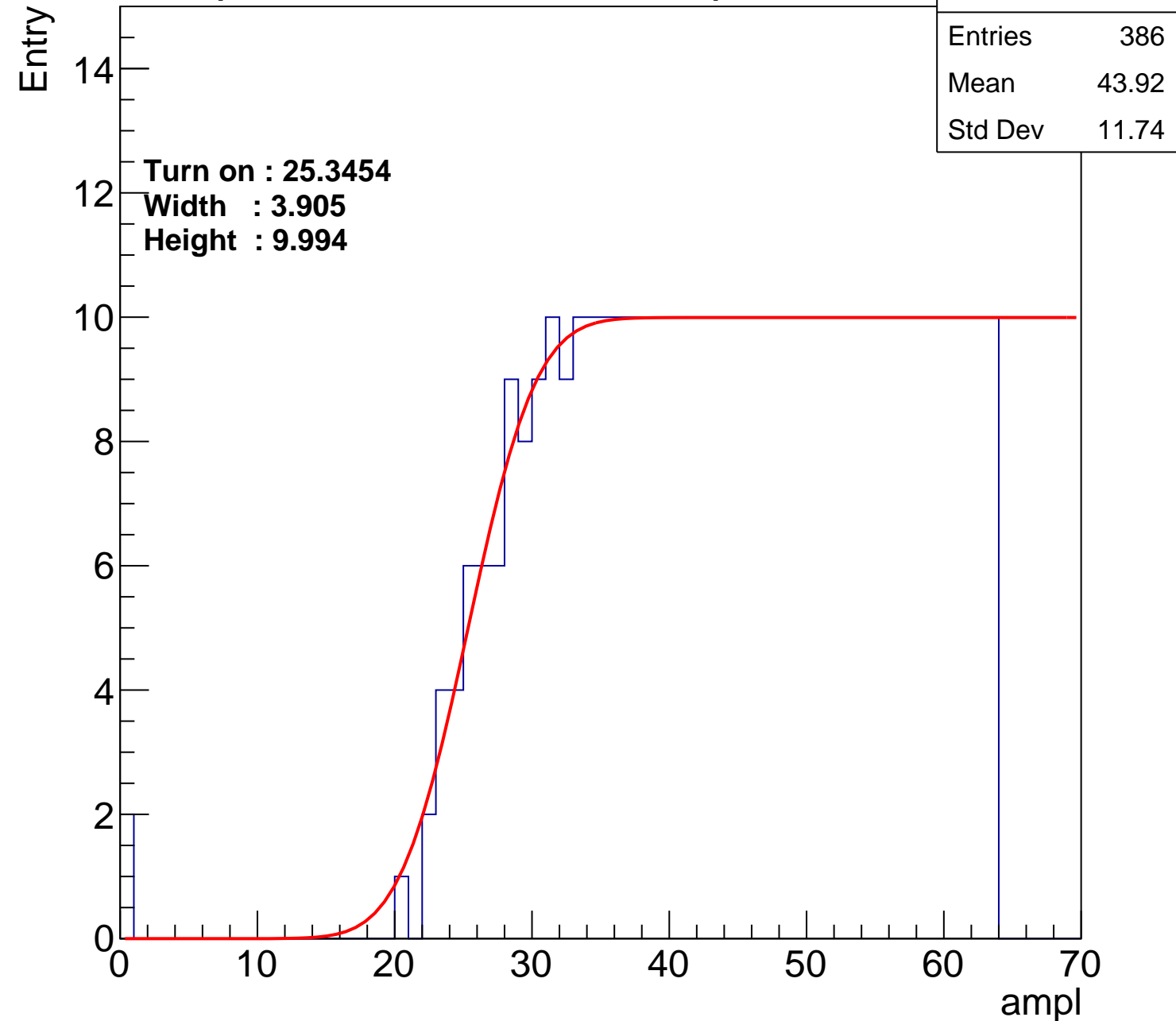
Width : 3.905

Height : 9.994

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch33

calib_packv5_042523_0143.root, FC#11, port A2

Entries	389
Mean	43.51
Std Dev	12.48

Turn on : 25.9658

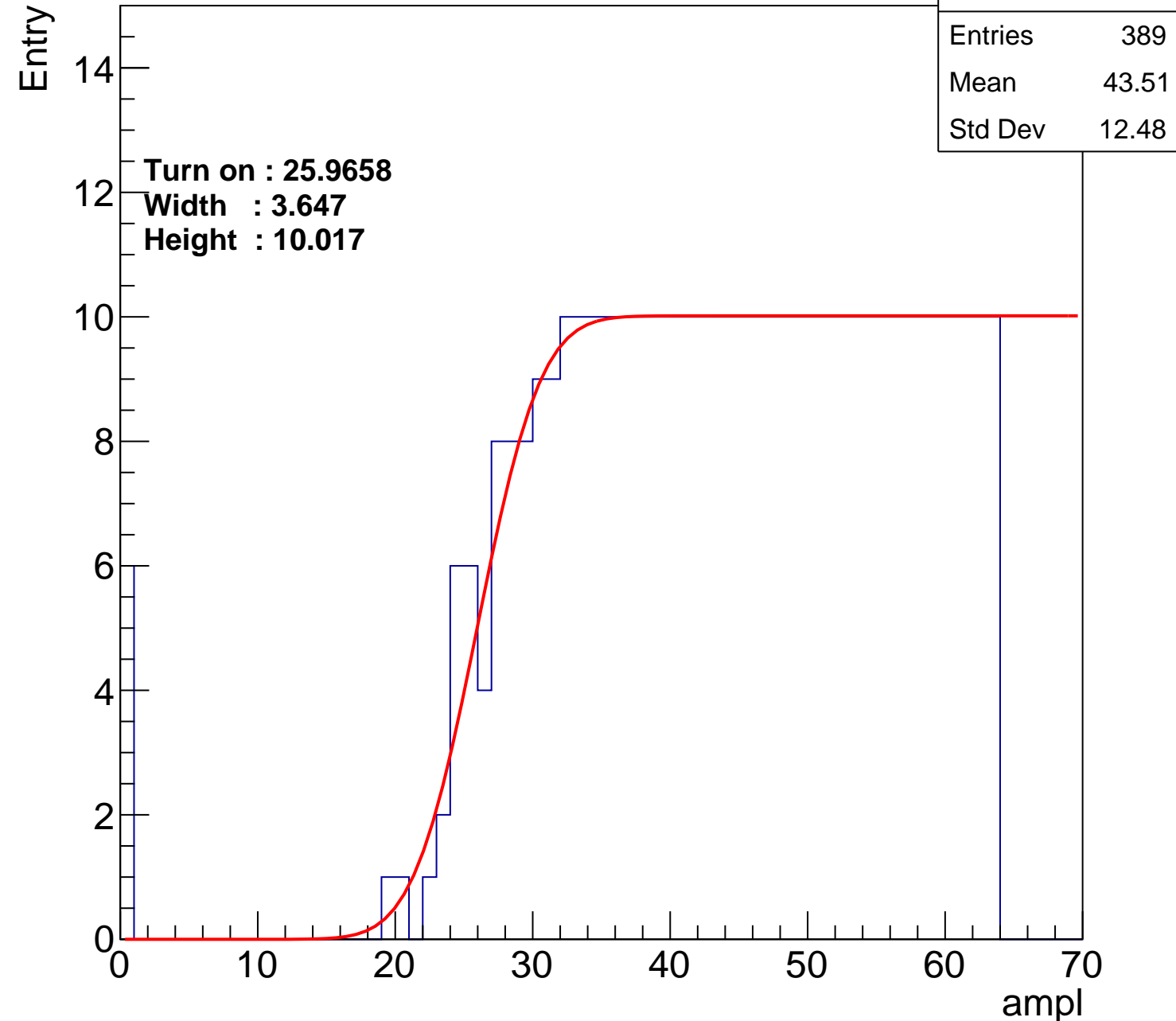
Width : 3.647

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch34

calib_packv5_042523_0143.root, FC#11, port A2

Entries	408
Mean	42.76
Std Dev	12.5

Turn on : 24.3510

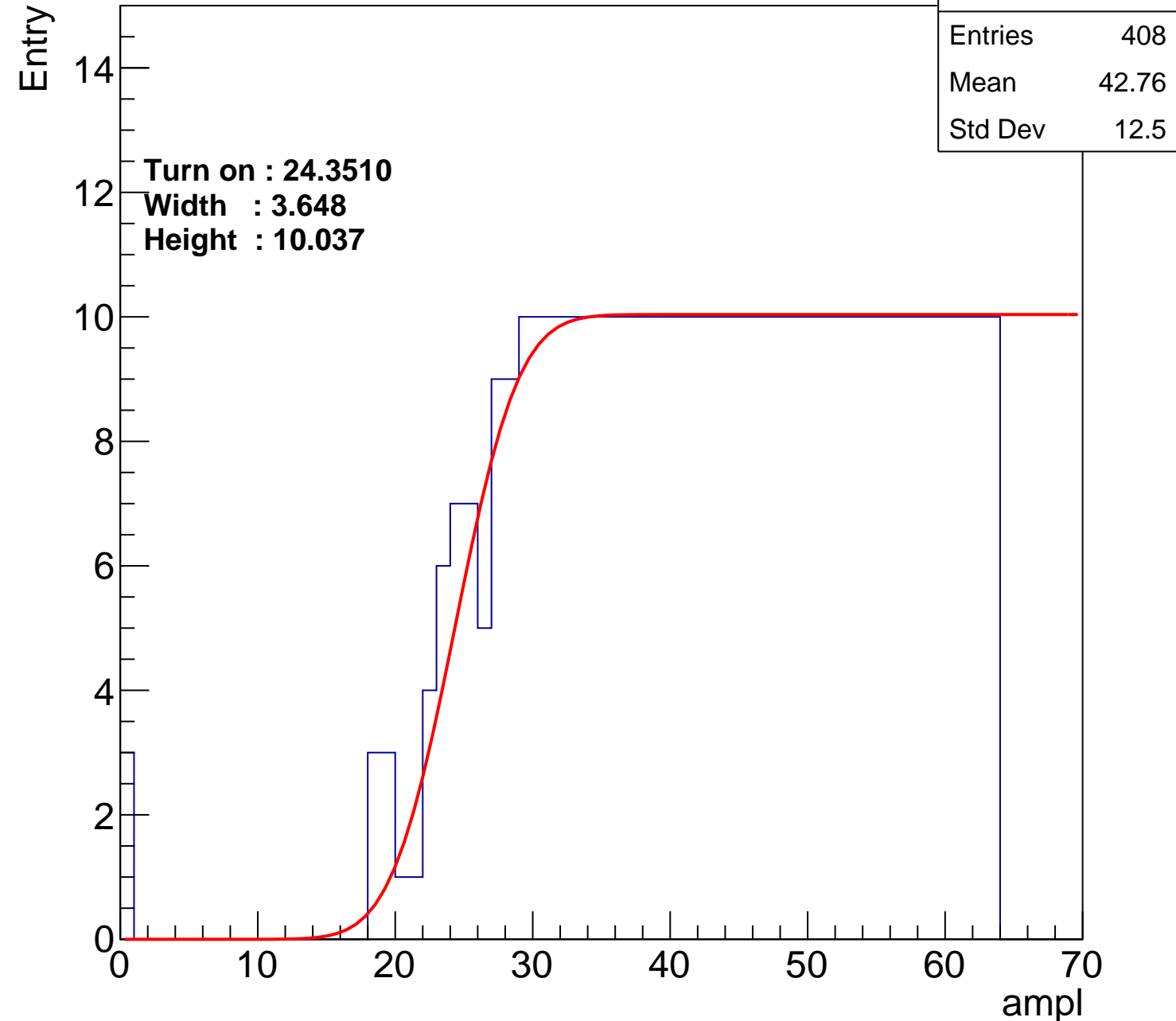
Width : 3.648

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch35

calib_packv5_042523_0143.root, FC#11, port A2

Entries	390
Mean	43.83
Std Dev	11.61

Turn on : 25.3010

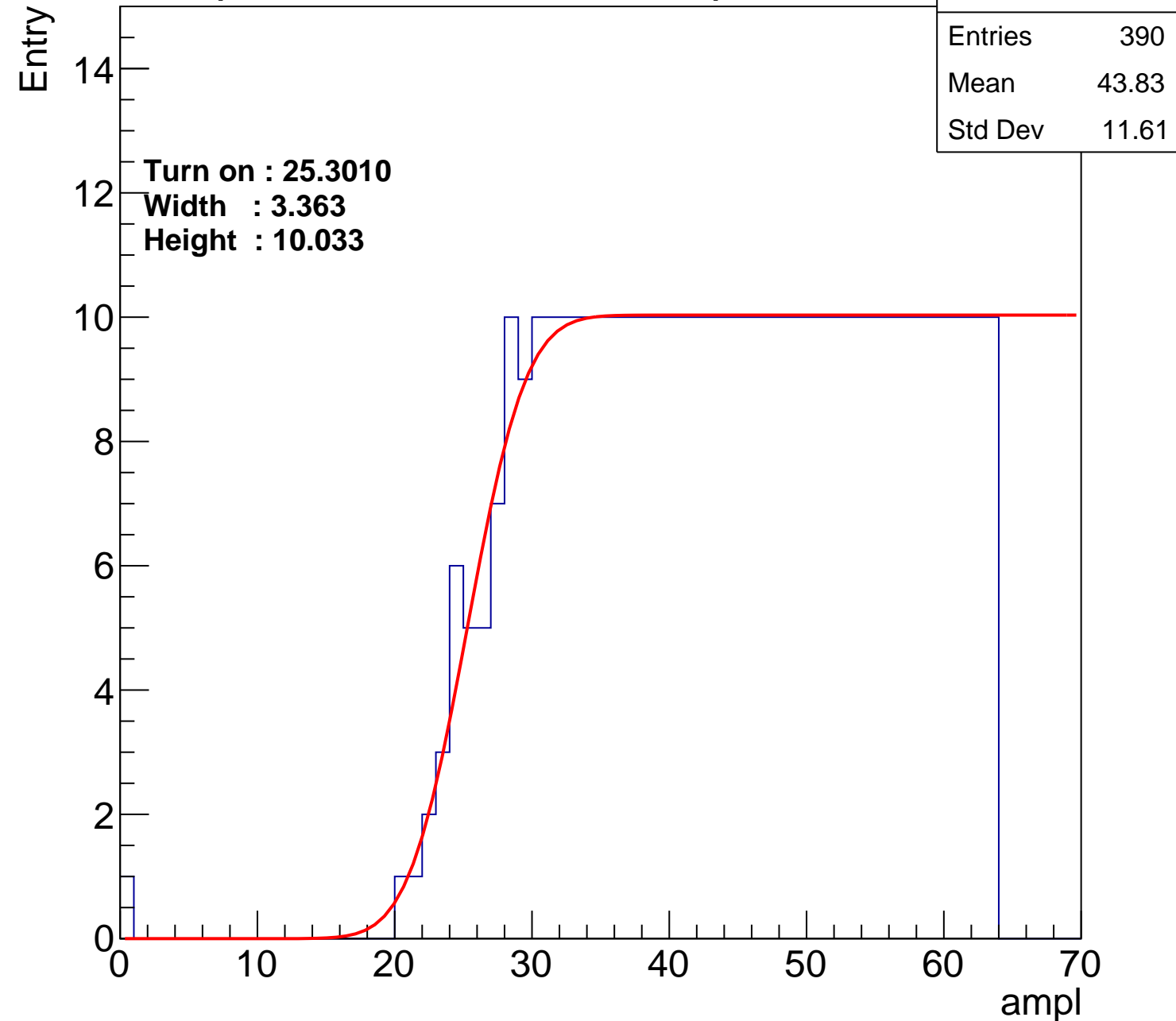
Width : 3.363

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch36

calib_packv5_042523_0143.root, FC#11, port A2

Entries	397
Mean	43.05
Std Dev	12.82

Turn on : 26.0742

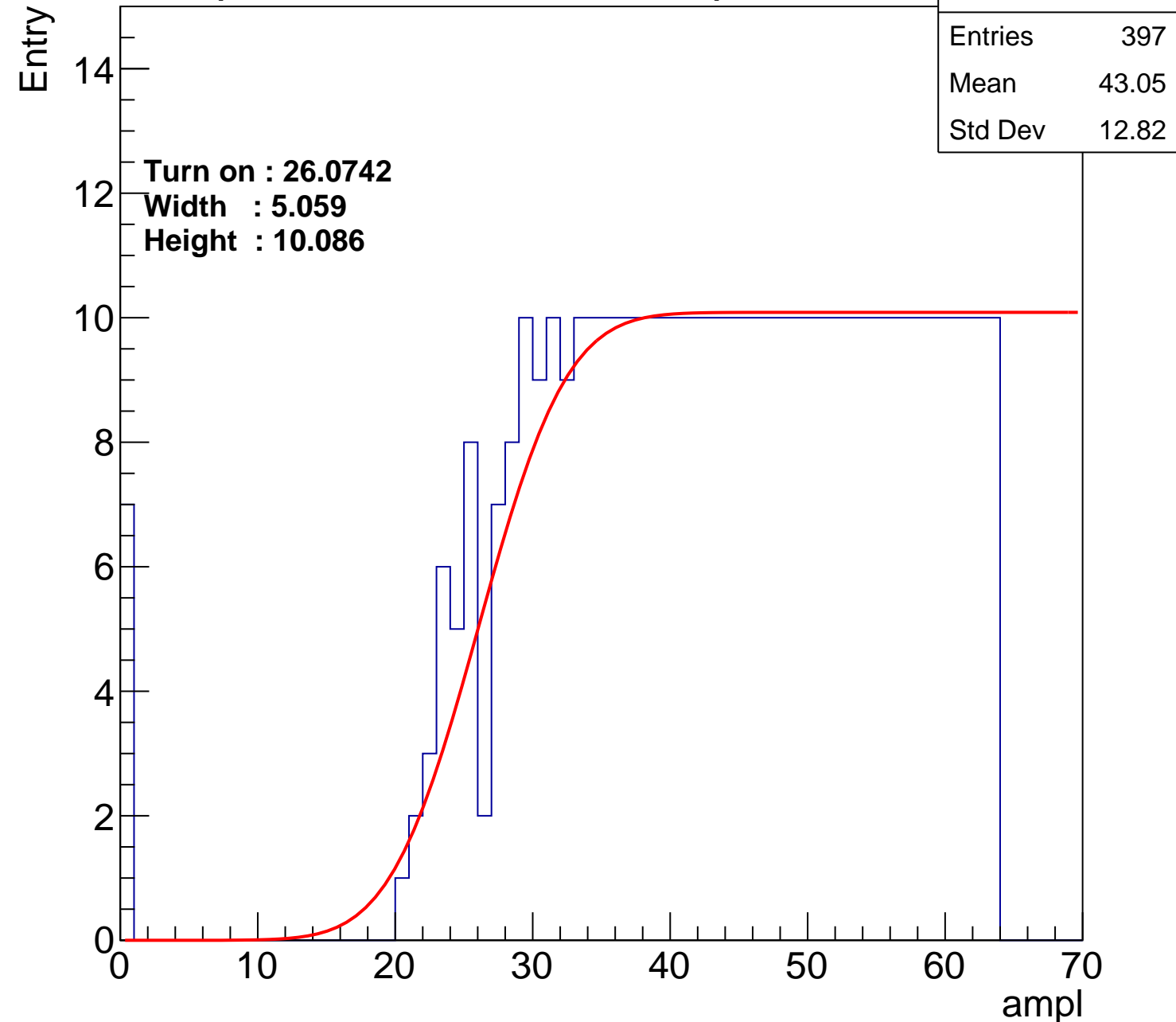
Width : 5.059

Height : 10.086

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch37

calib_packv5_042523_0143.root, FC#11, port A2

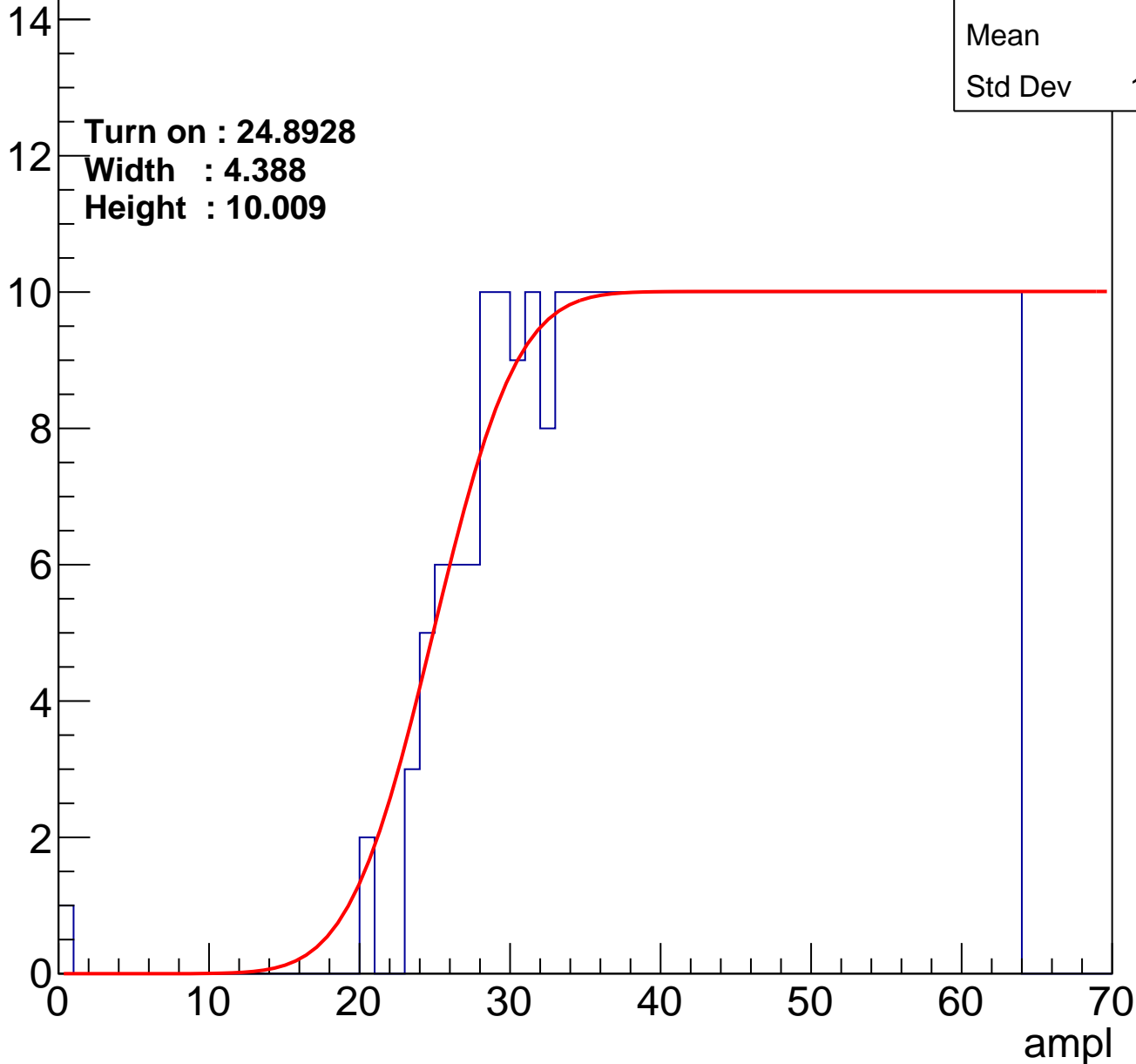
Entries	386
Mean	44
Std Dev	11.54

Turn on : 24.8928

Width : 4.388

Height : 10.009

Entry



B1L102S, U5-ch38

calib_packv5_042523_0143.root, FC#11, port A2

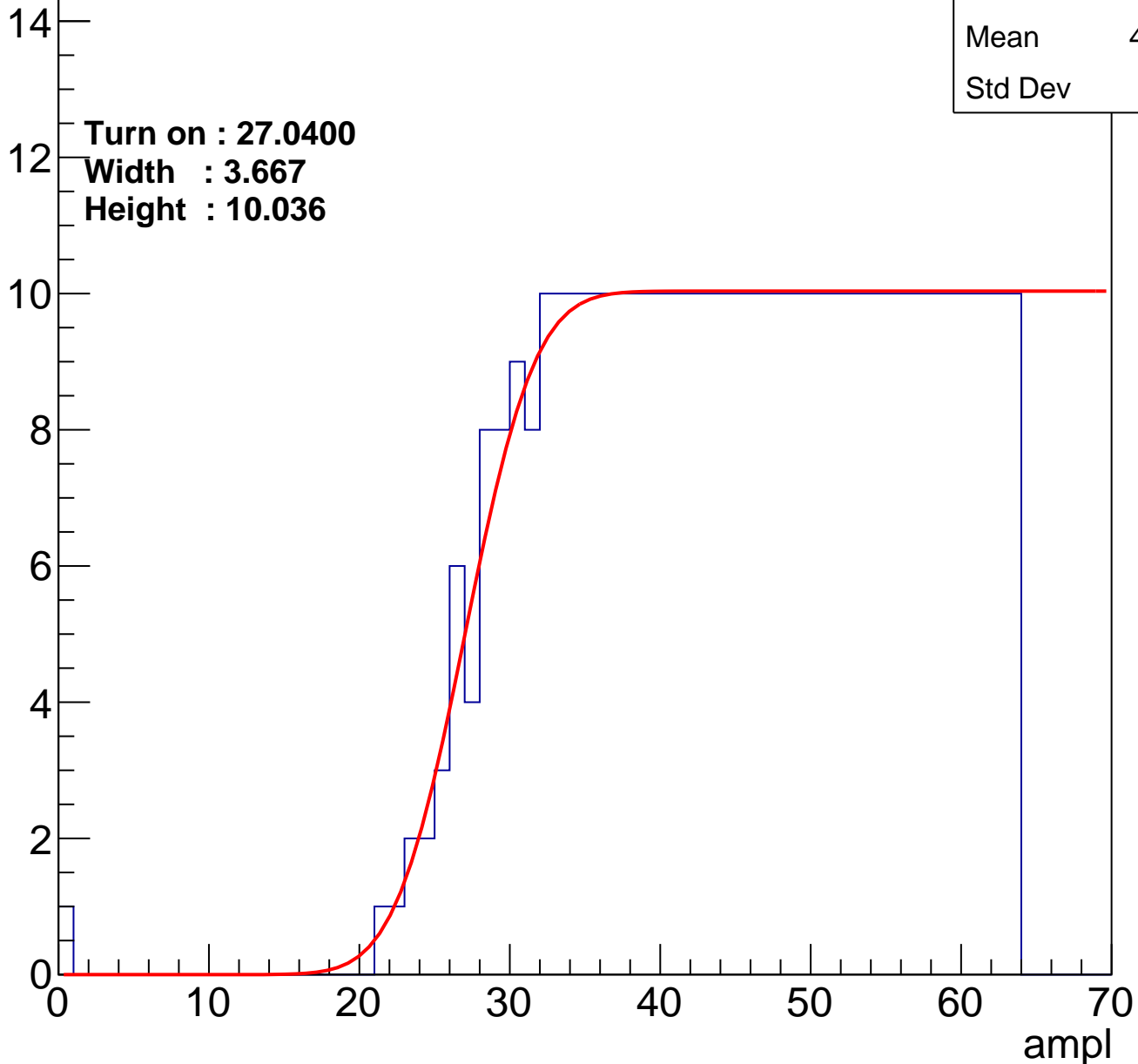
Entries	373
Mean	44.64
Std Dev	11.2

Turn on : 27.0400

Width : 3.667

Height : 10.036

Entry



B1L102S, U5-ch39

calib_packv5_042523_0143.root, FC#11, port A2

Entries	384
Mean	43.88
Std Dev	12.05

Turn on : 25.9037

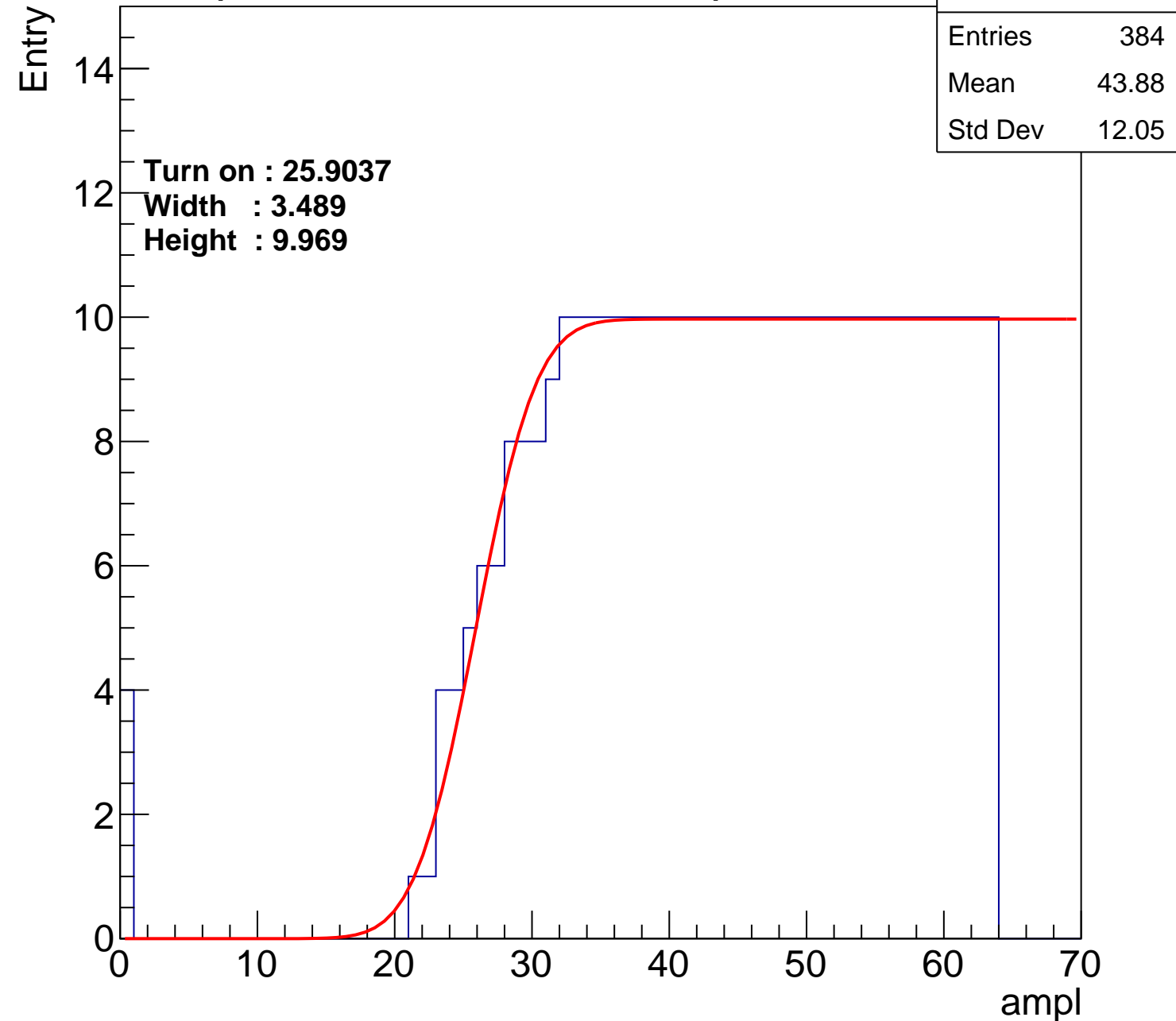
Width : 3.489

Height : 9.969

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch40

calib_packv5_042523_0143.root, FC#11, port A2

Entries	386
Mean	43.81
Std Dev	12.06

Turn on : 26.1106

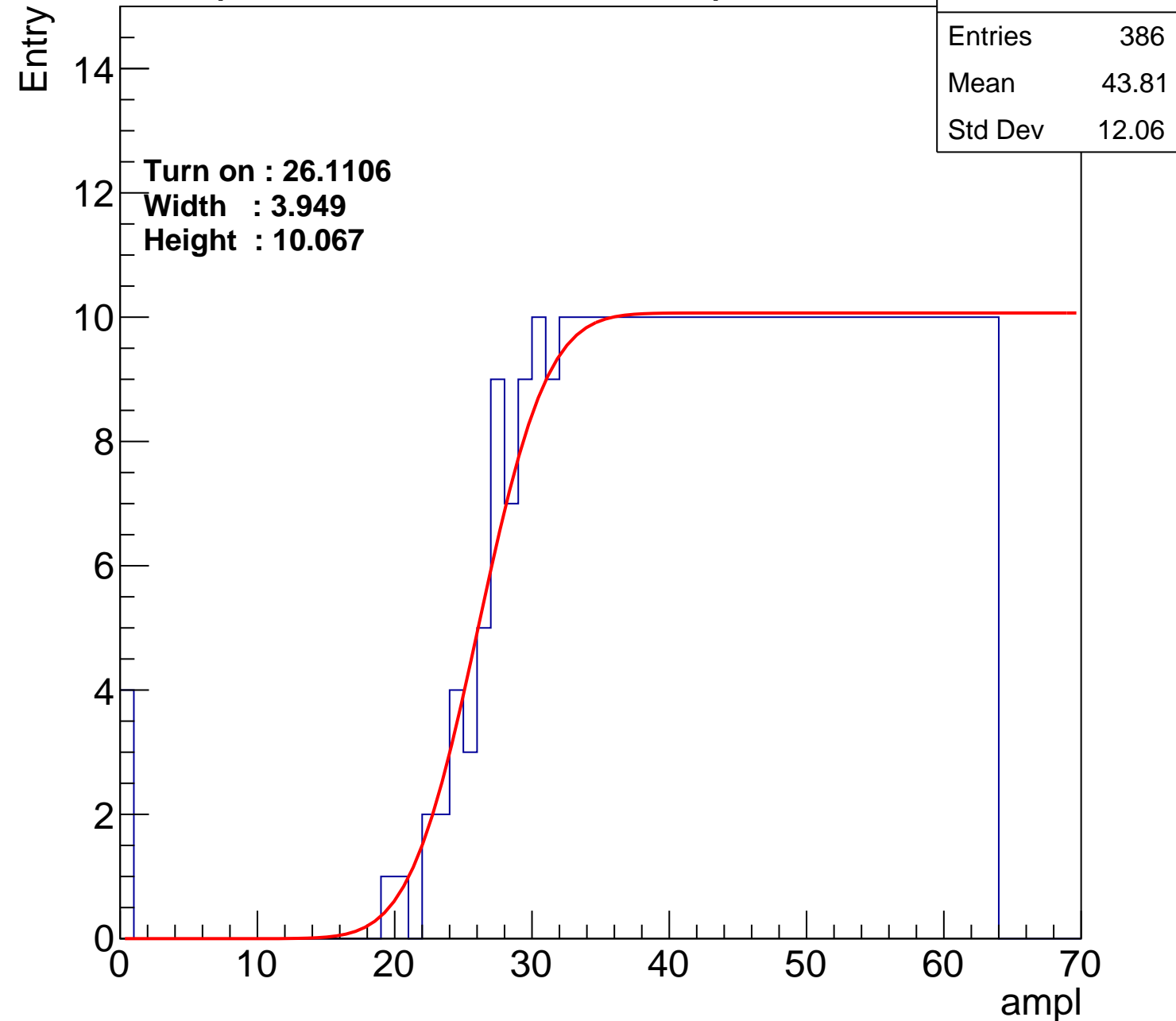
Width : 3.949

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch41

calib_packv5_042523_0143.root, FC#11, port A2

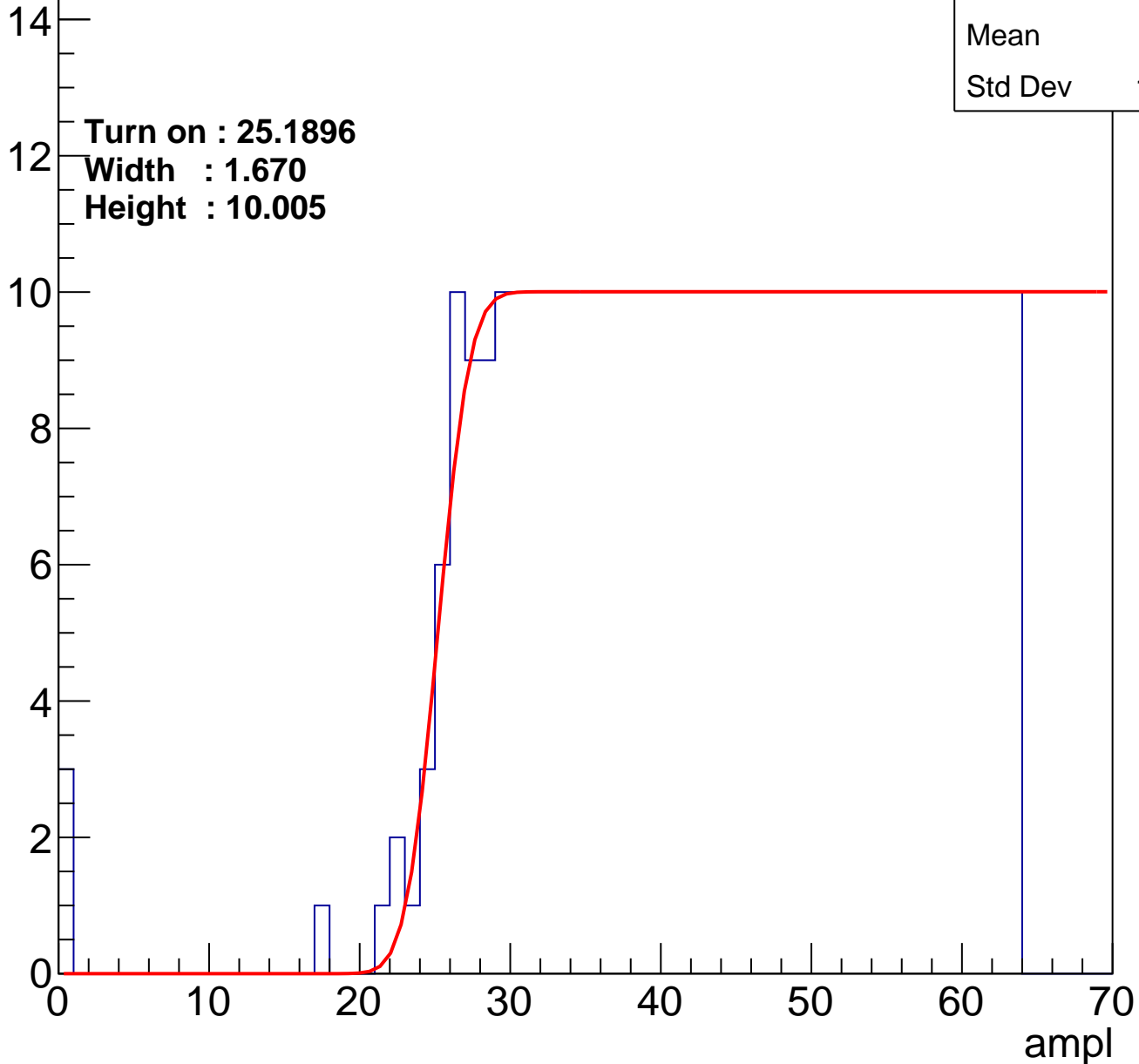
Entries	395
Mean	43.5
Std Dev	12.01

Turn on : 25.1896

Width : 1.670

Height : 10.005

Entry



B1L102S, U5-ch42

calib_packv5_042523_0143.root, FC#11, port A2

Entries	415
Mean	42.48
Std Dev	12.57

Turn on : 23.0026

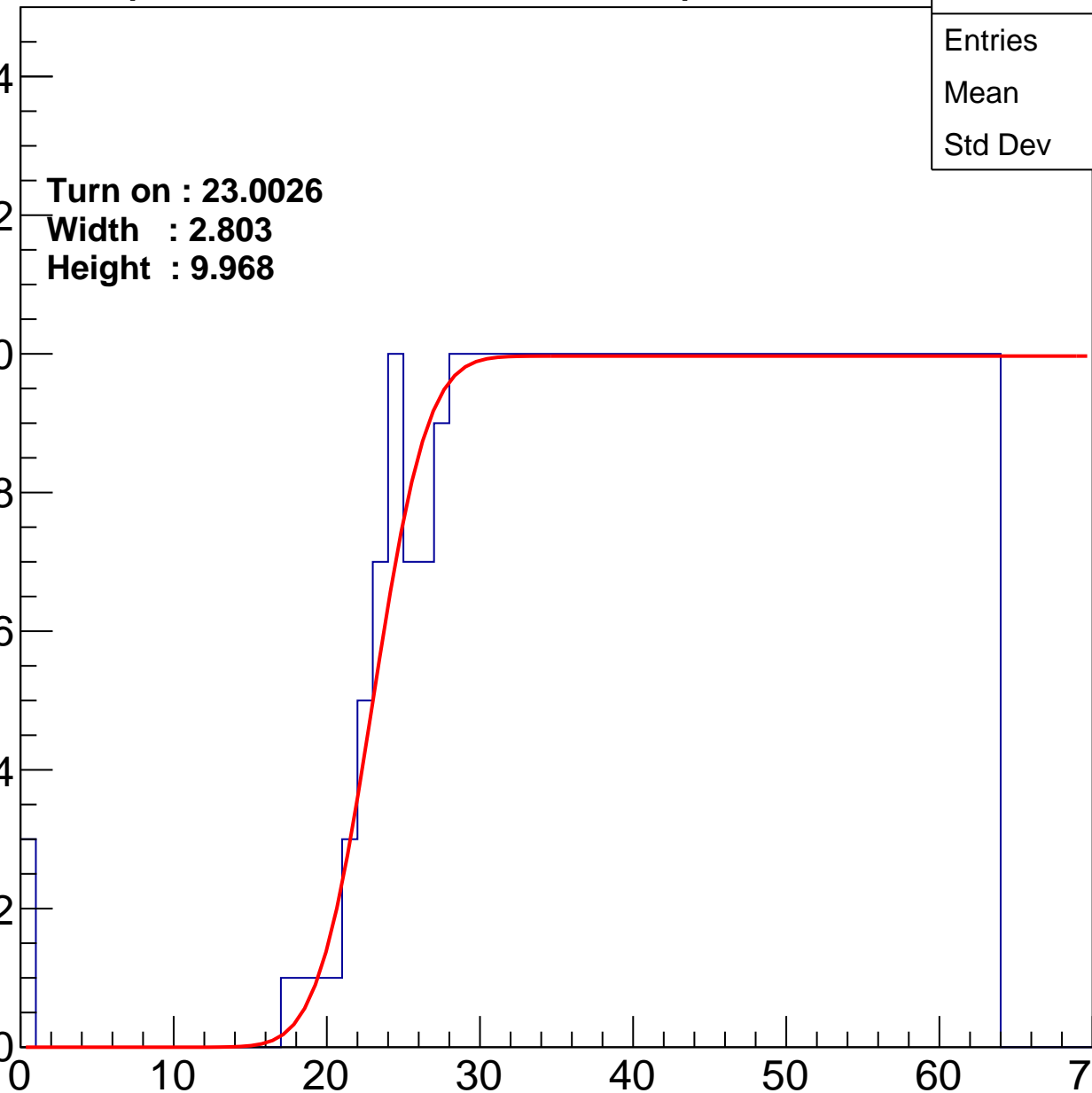
Width : 2.803

Height : 9.968

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch43

calib_packv5_042523_0143.root, FC#11, port A2

Entries	381
Mean	44.17
Std Dev	11.69

Turn on : 26.1712

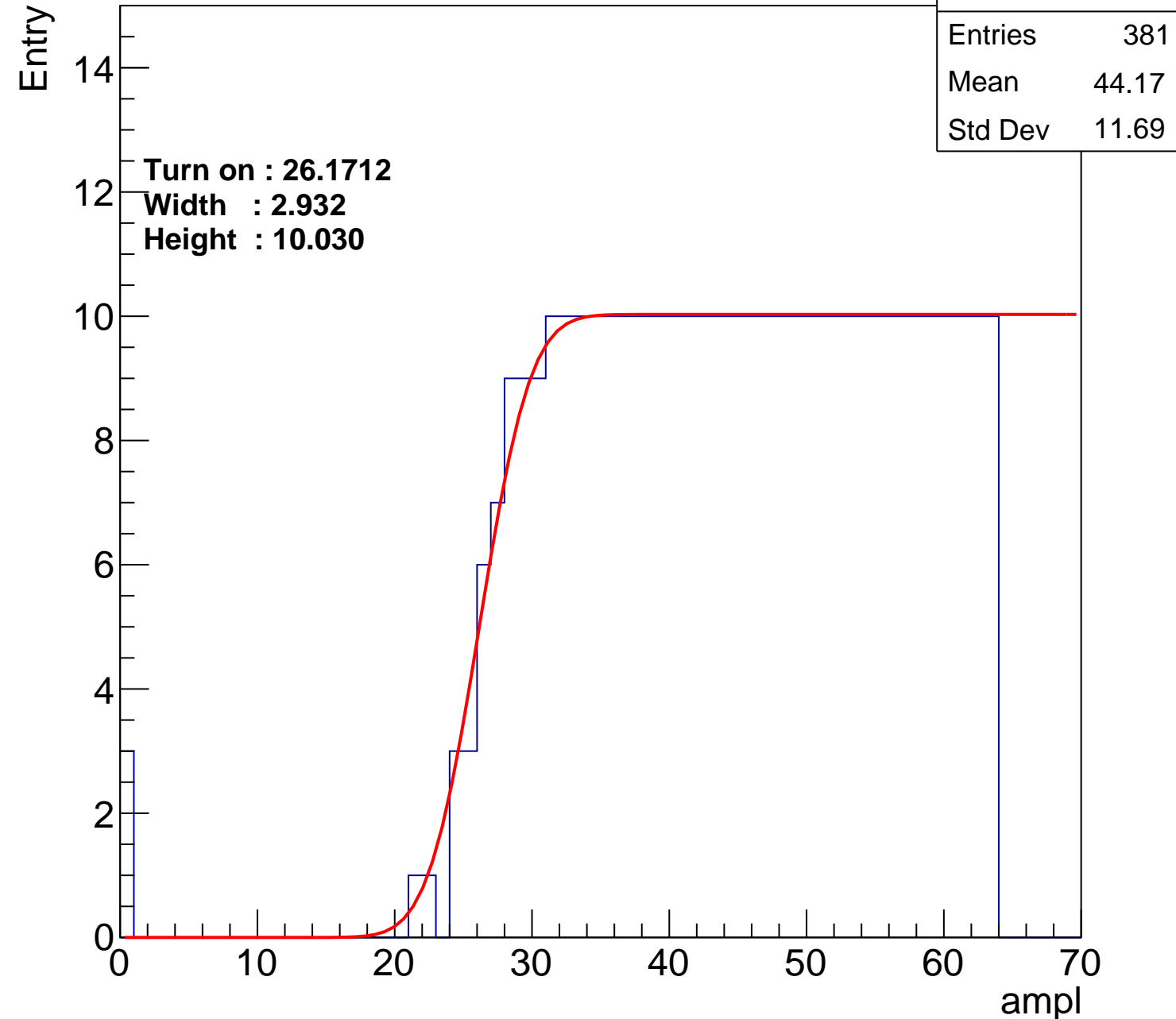
Width : 2.932

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch44

calib_packv5_042523_0143.root, FC#11, port A2

Entries	404
Mean	43.06
Std Dev	12.16

Turn on : 24.0701

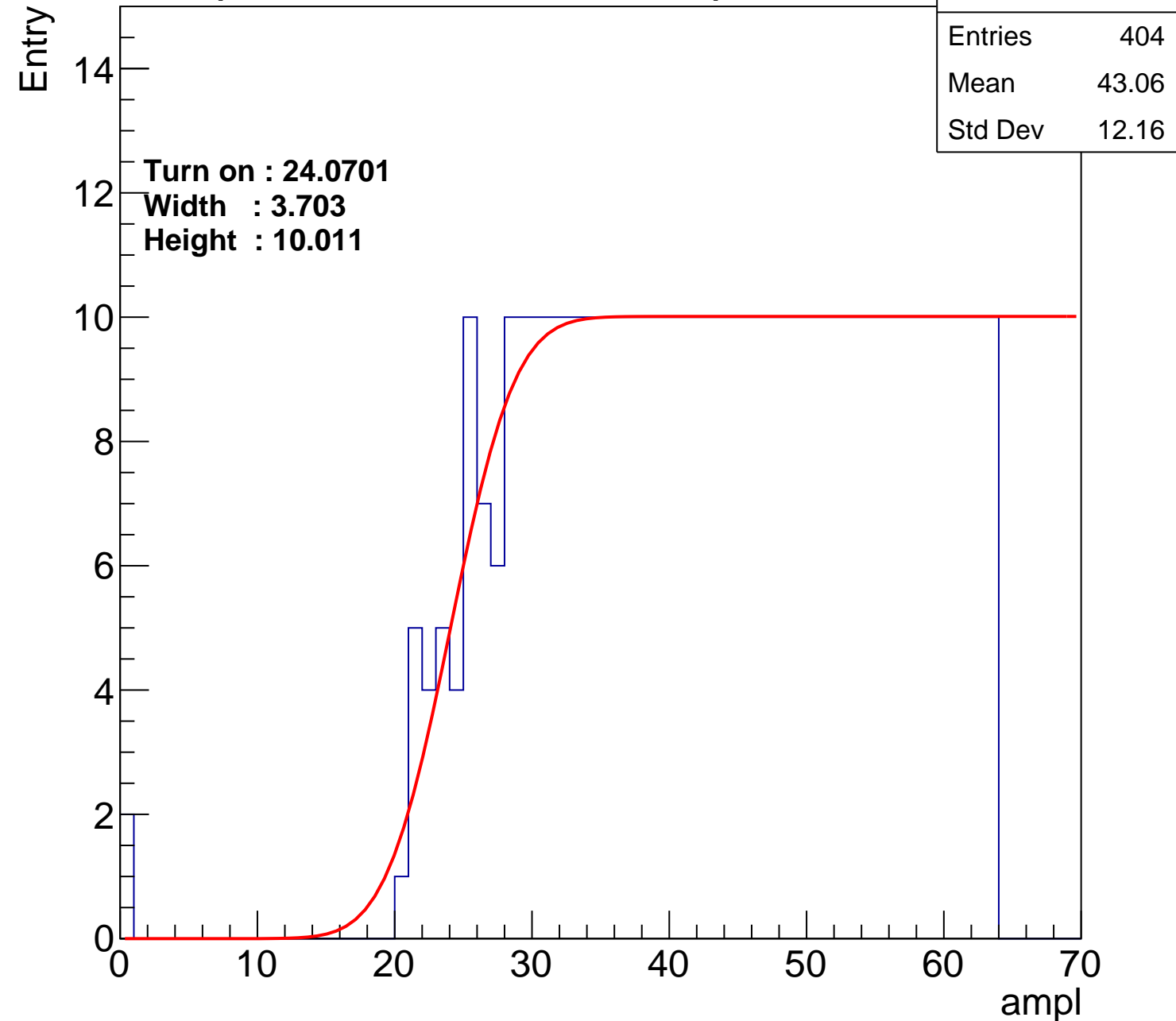
Width : 3.703

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch45

calib_packv5_042523_0143.root, FC#11, port A2

Entries	393
Mean	43.65
Std Dev	11.74

Turn on : 25.1767

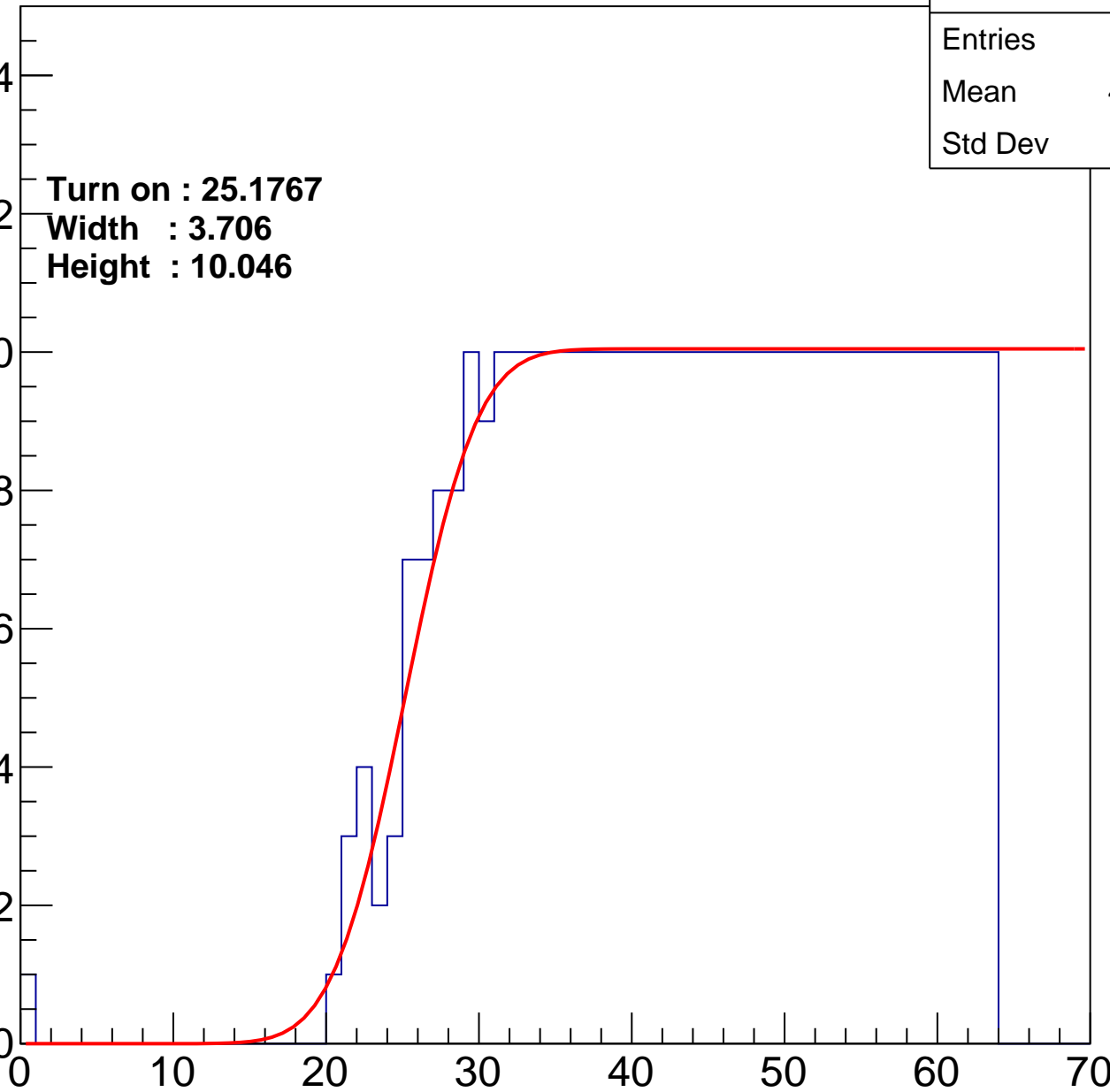
Width : 3.706

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch46

calib_packv5_042523_0143.root, FC#11, port A2

Entries	398
Mean	43.33
Std Dev	12.12

Turn on : 24.3773

Width : 2.869

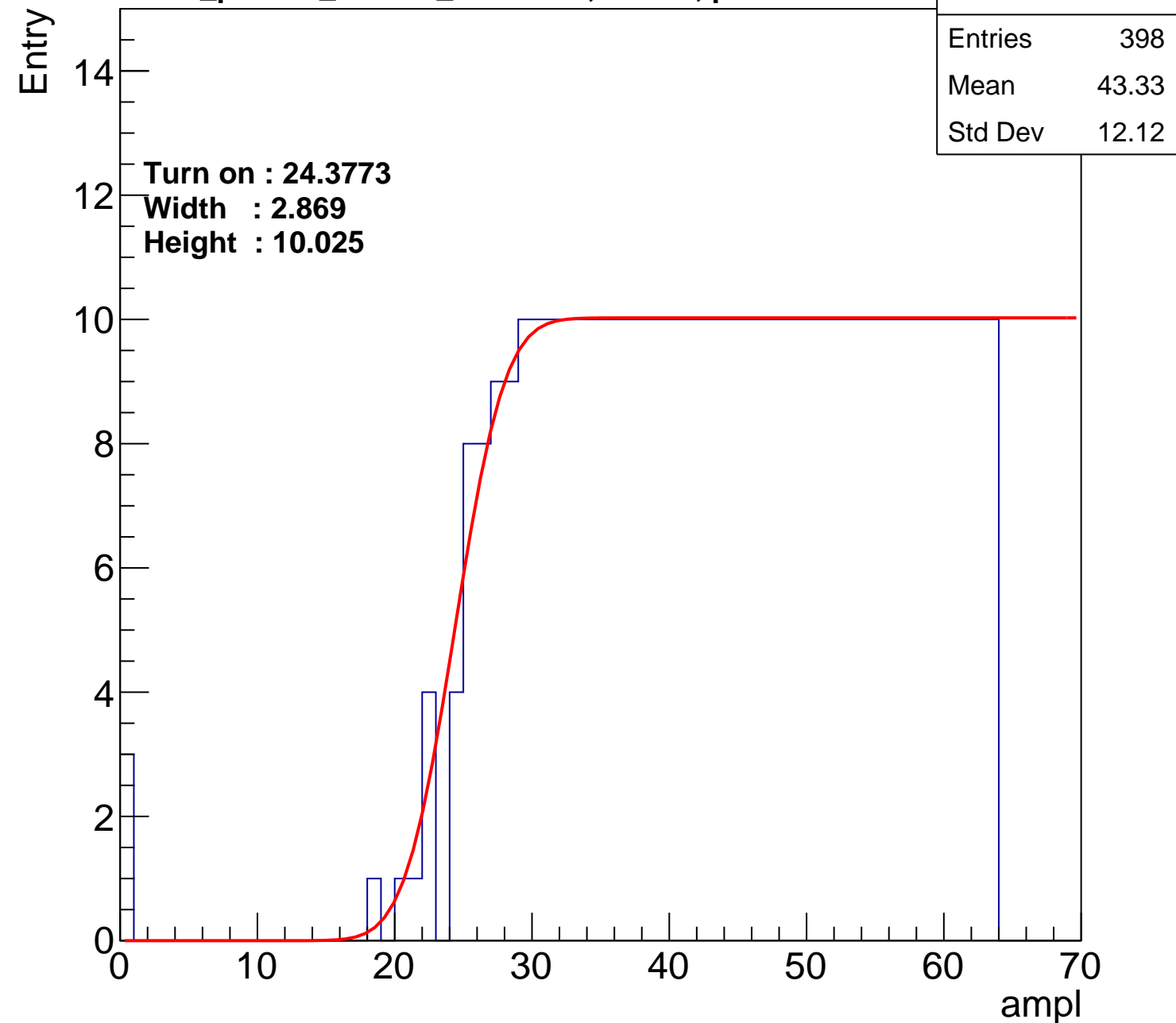
Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L102S, U5-ch47

calib_packv5_042523_0143.root, FC#11, port A2

Entries	385
Mean	43.97
Std Dev	11.79

Turn on : 26.2935

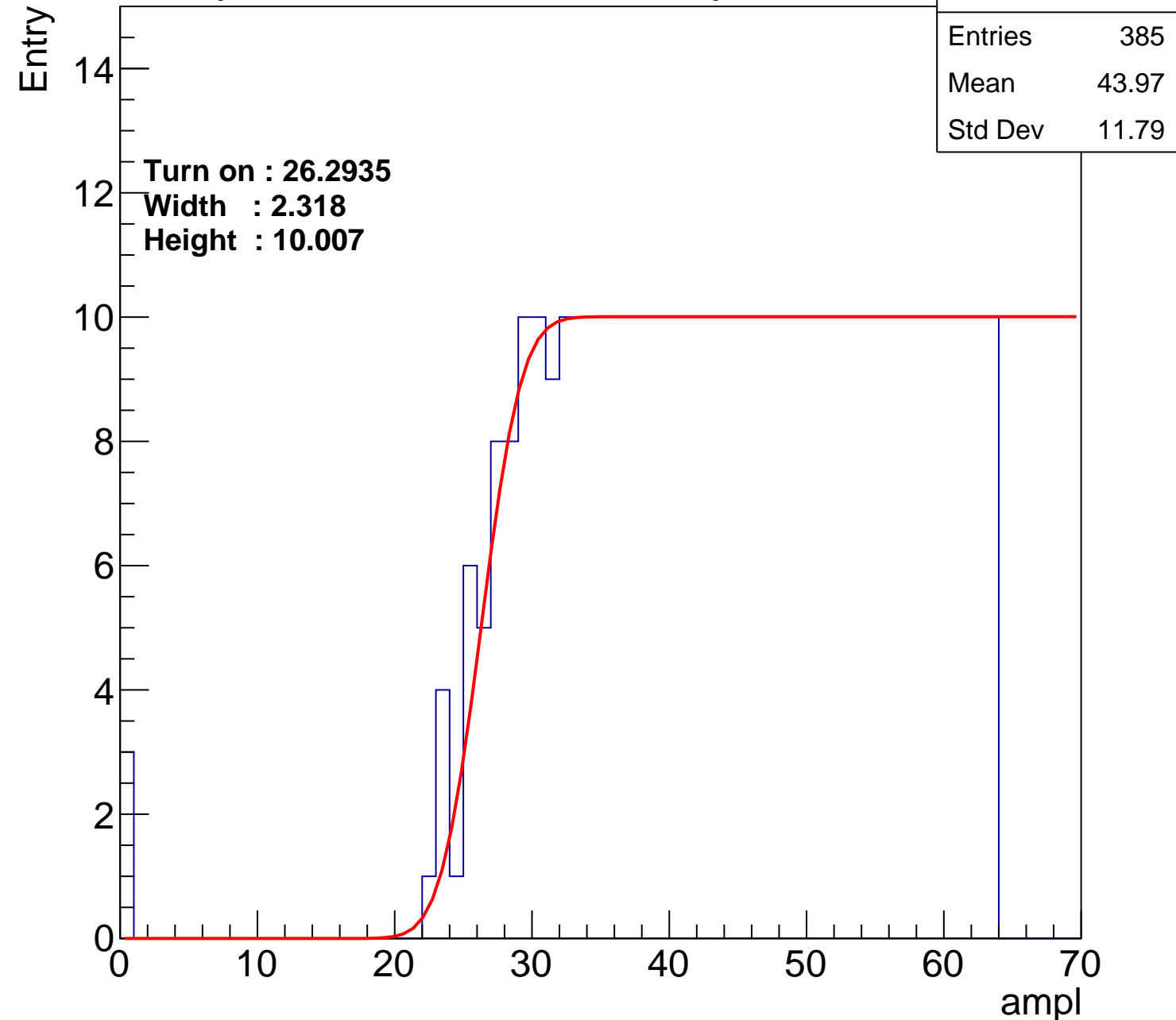
Width : 2.318

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch48

calib_packv5_042523_0143.root, FC#11, port A2

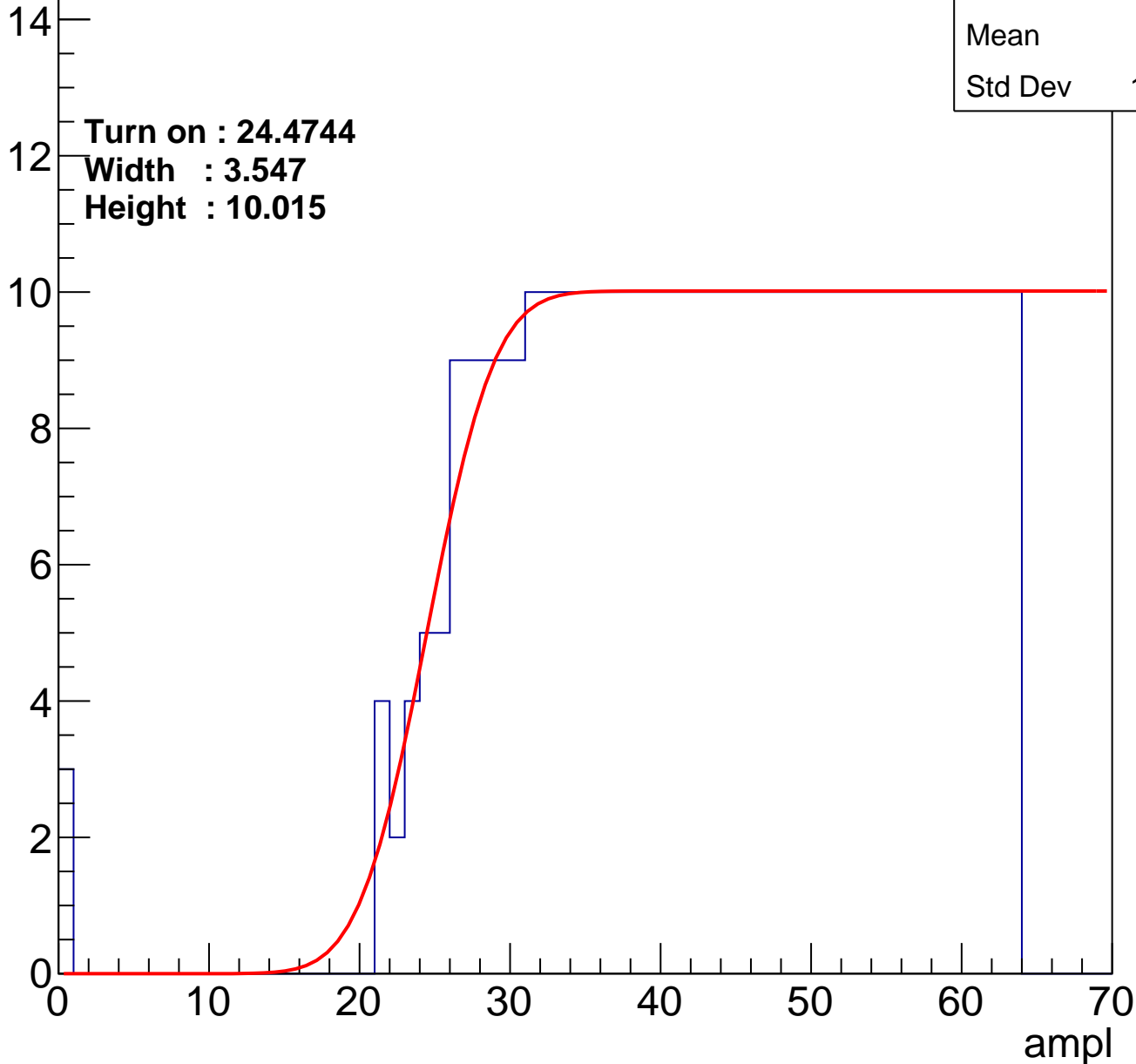
Entries	398
Mean	43.3
Std Dev	12.15

Turn on : 24.4744

Width : 3.547

Height : 10.015

Entry



B1L102S, U5-ch49

calib_packv5_042523_0143.root, FC#11, port A2

Entries	382
Mean	44.17
Std Dev	11.49

Turn on : 26.4873

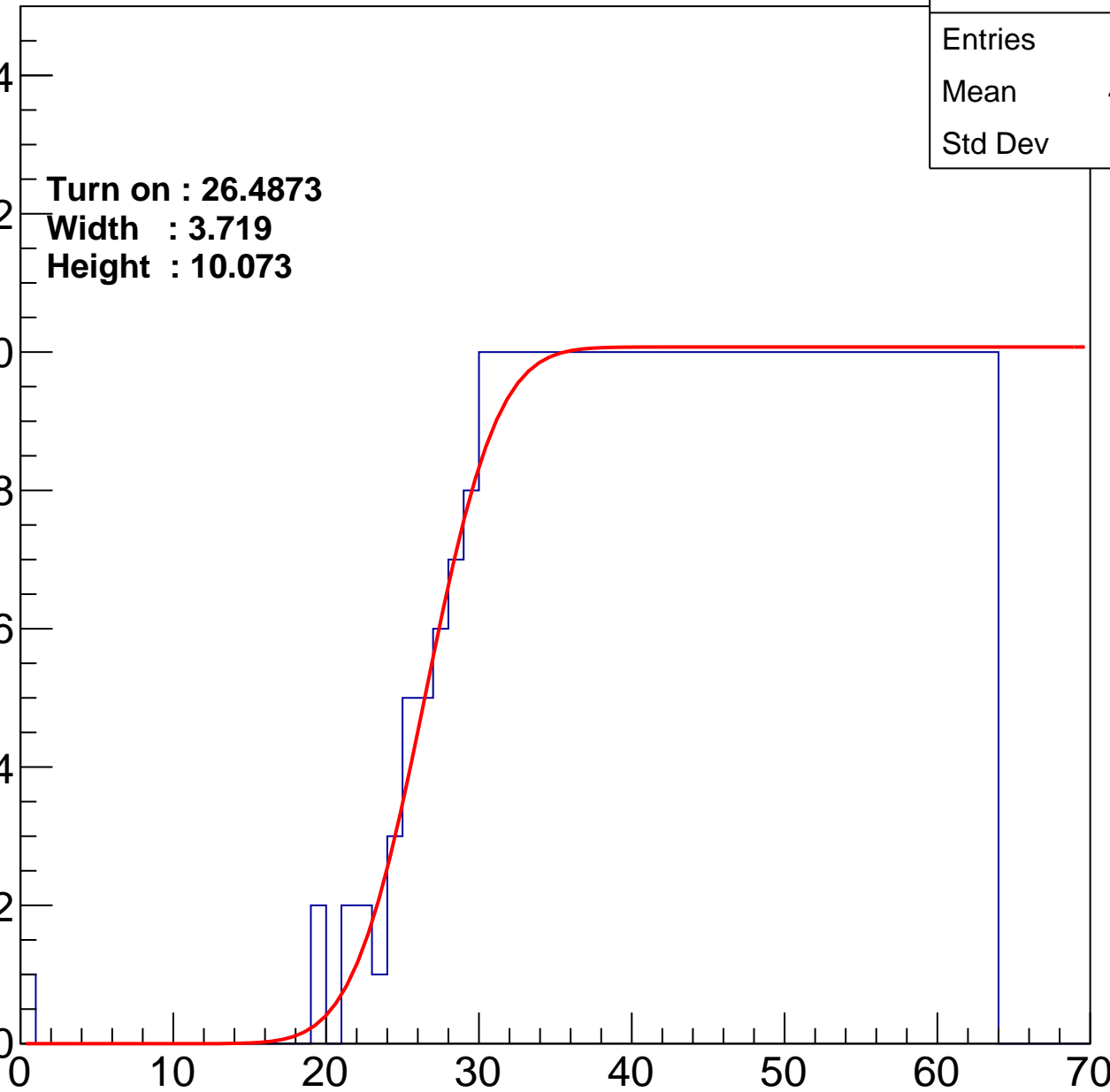
Width : 3.719

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch50

calib_packv5_042523_0143.root, FC#11, port A2

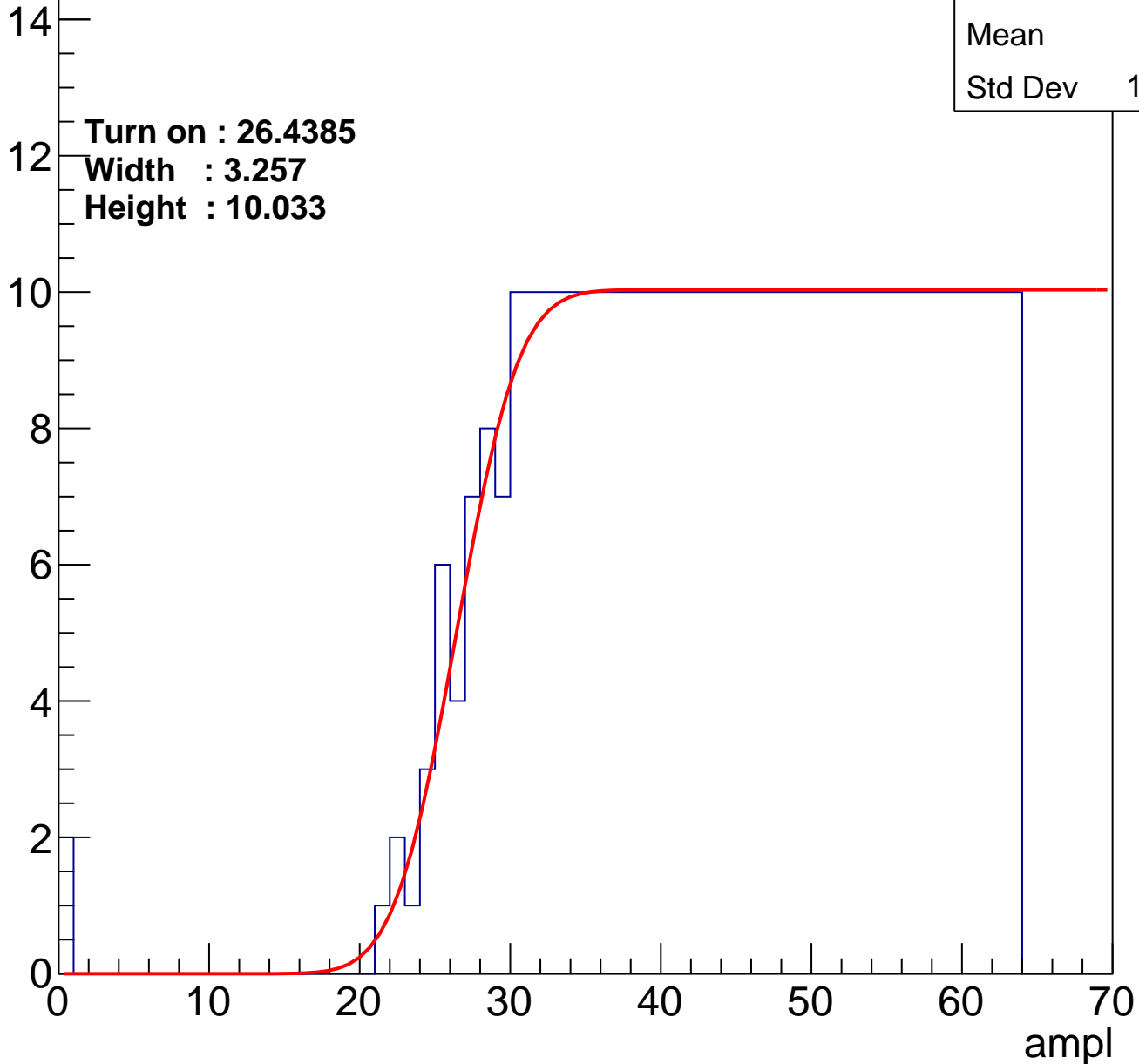
Entries	381
Mean	44.2
Std Dev	11.56

Turn on : 26.4385

Width : 3.257

Height : 10.033

Entry



B1L102S, U5-ch51

calib_packv5_042523_0143.root, FC#11, port A2

Entries	390
Mean	43.77
Std Dev	11.77

Turn on : 25.1871

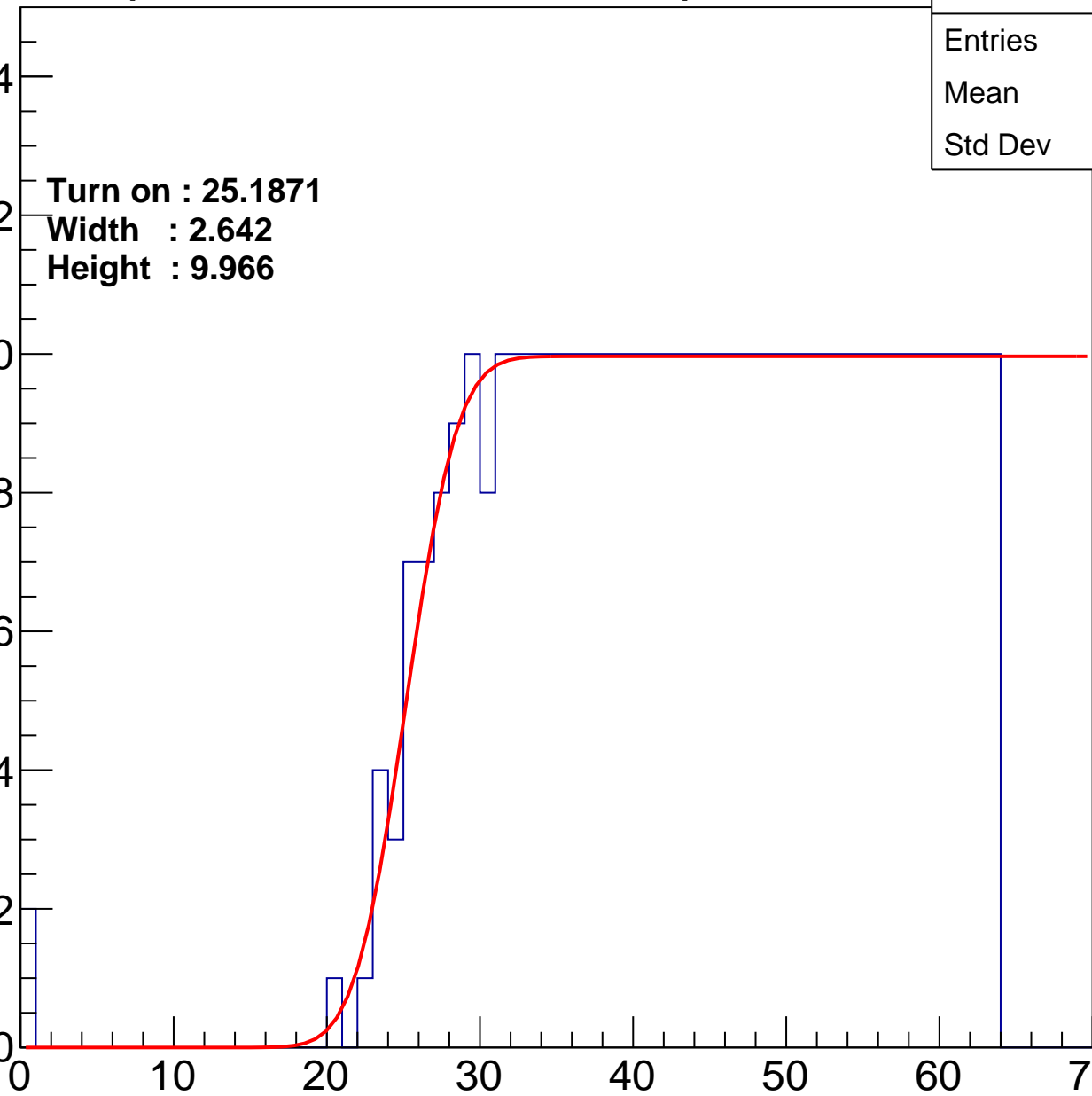
Width : 2.642

Height : 9.966

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch52

calib_packv5_042523_0143.root, FC#11, port A2

Entries	386
Mean	43.95
Std Dev	11.69

Turn on : 25.8537

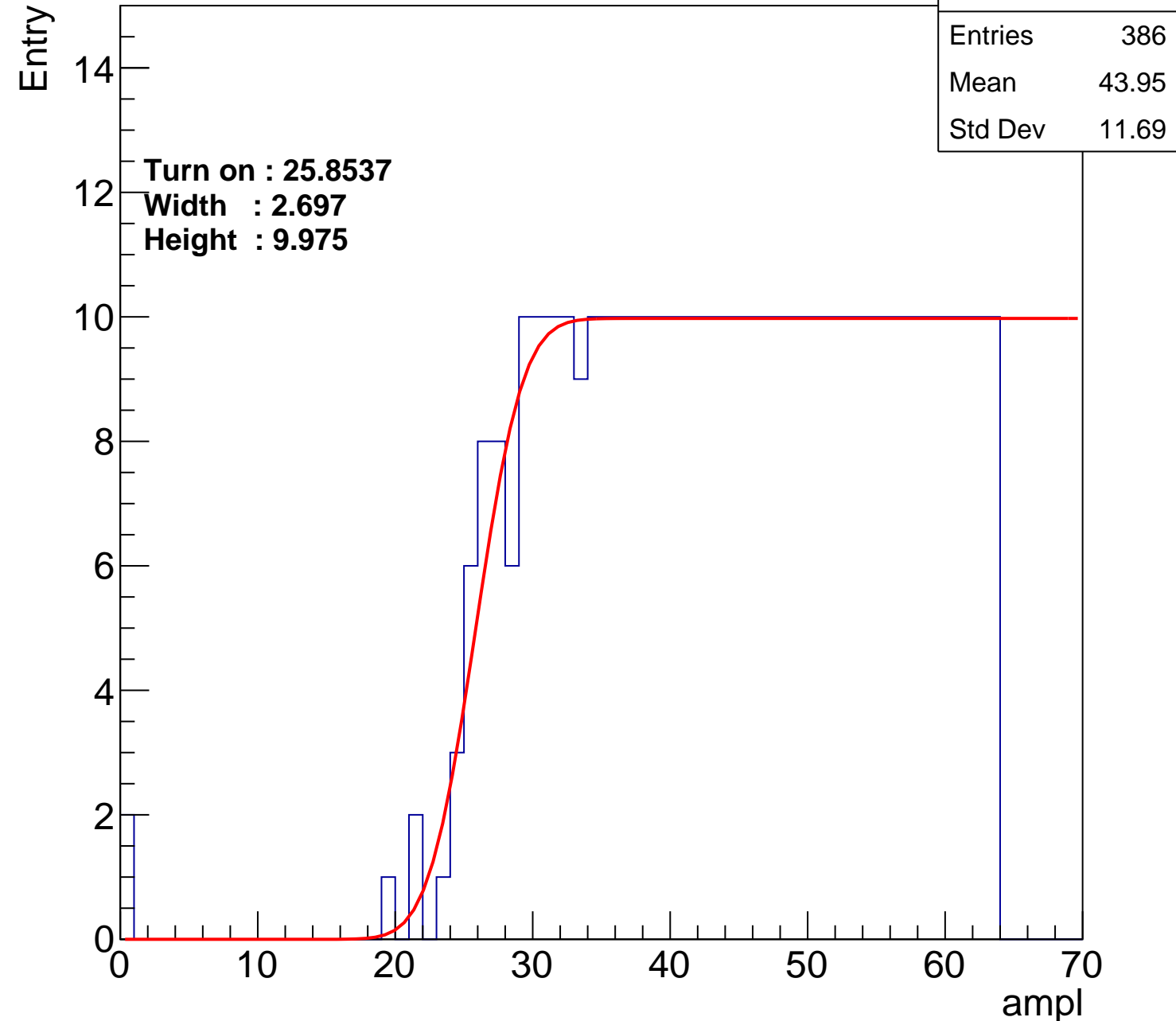
Width : 2.697

Height : 9.975

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch53

calib_packv5_042523_0143.root, FC#11, port A2

Entries	394
Mean	43.62
Std Dev	11.73

Turn on : 25.2568

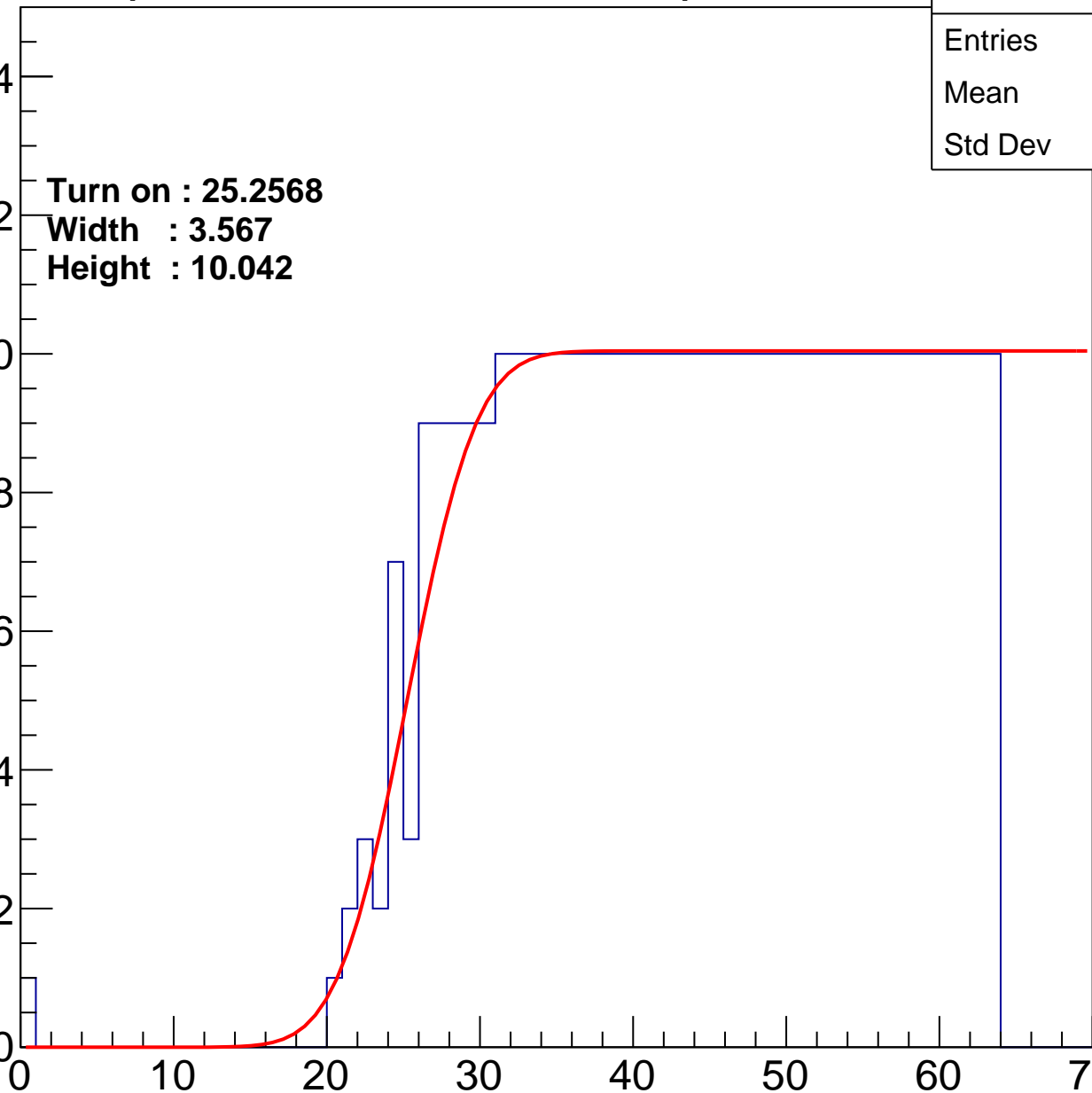
Width : 3.567

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch54

calib_packv5_042523_0143.root, FC#11, port A2

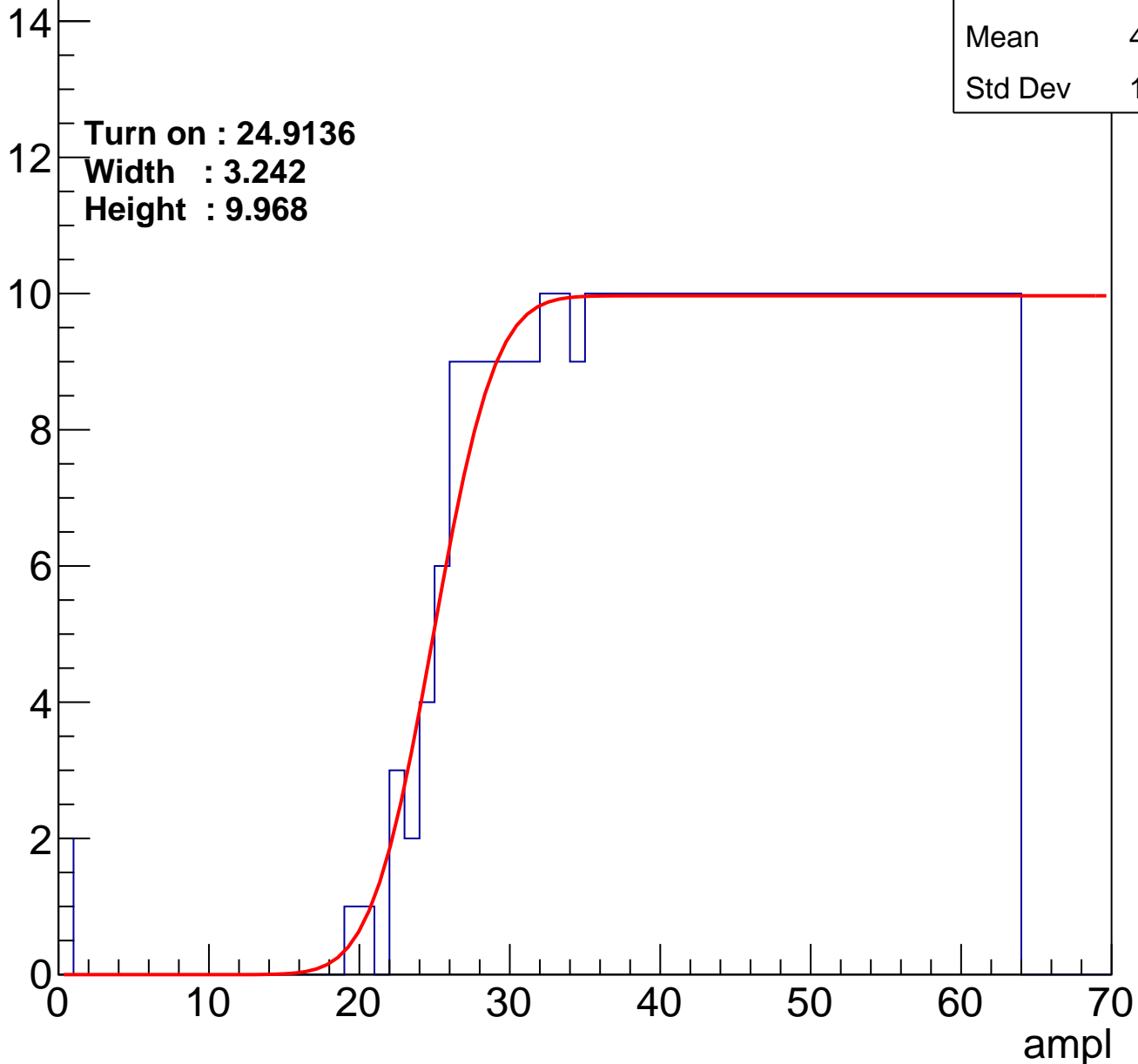
Entries	392
Mean	43.63
Std Dev	11.88

Turn on : 24.9136

Width : 3.242

Height : 9.968

Entry



B1L102S, U5-ch55

calib_packv5_042523_0143.root, FC#11, port A2

Entries	370
Mean	44.78
Std Dev	11.13

Turn on : 28.3218

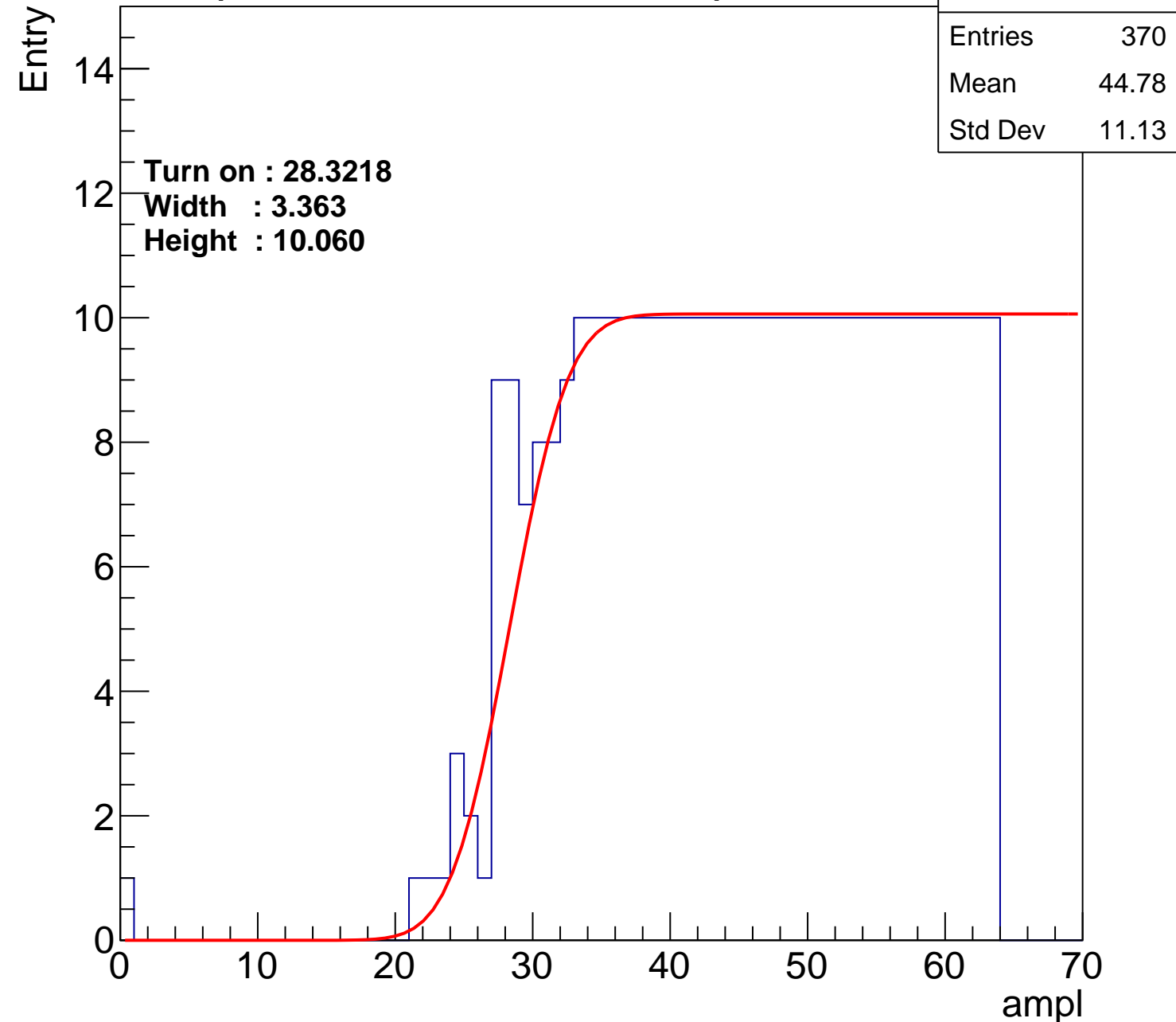
Width : 3.363

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch56

calib_packv5_042523_0143.root, FC#11, port A2

Entries	380
Mean	44.32
Std Dev	11.35

Turn on : 26.3155

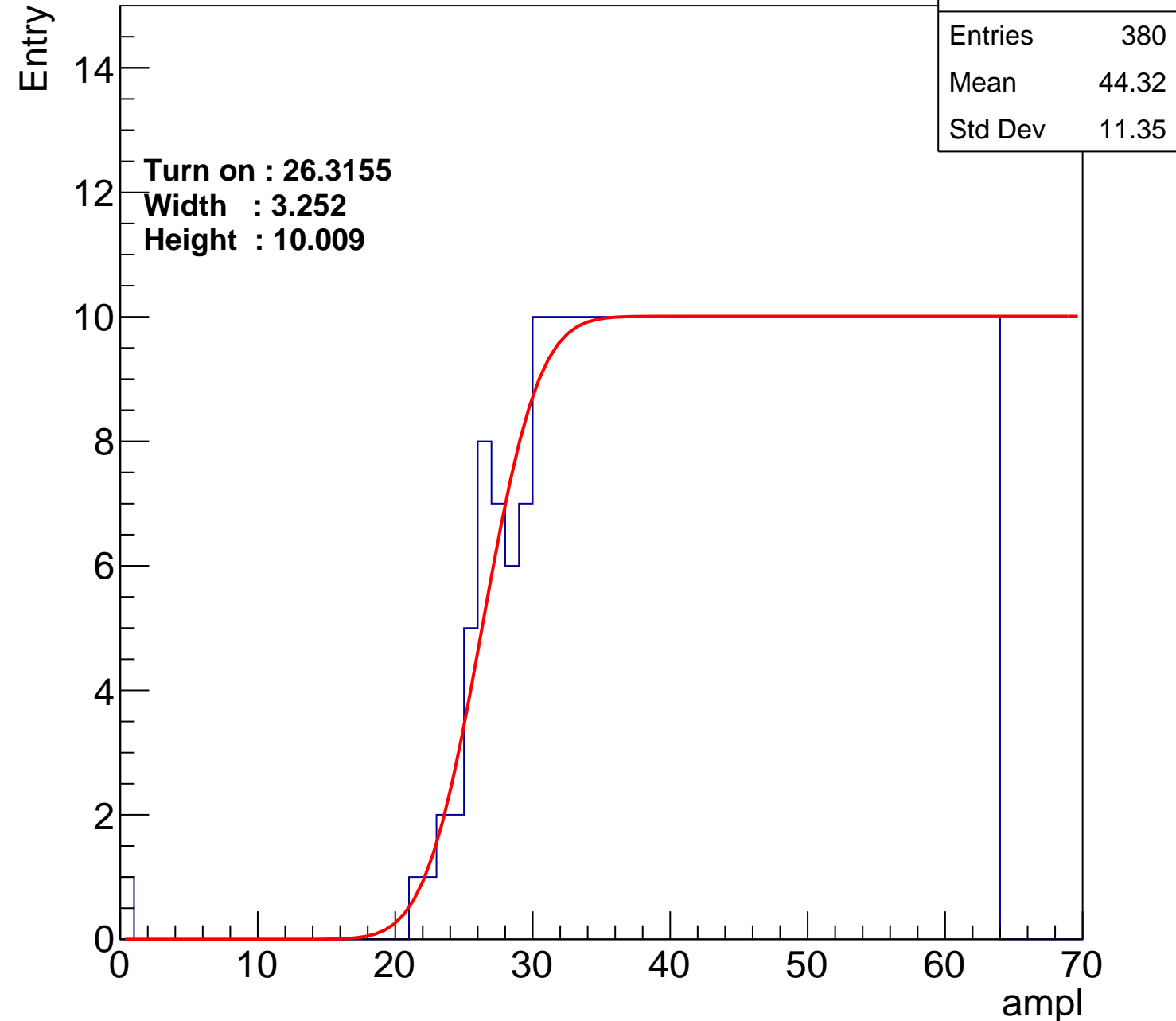
Width : 3.252

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch57

calib_packv5_042523_0143.root, FC#11, port A2

Entries	392
Mean	43.55
Std Dev	12.14

Turn on : 26.2288

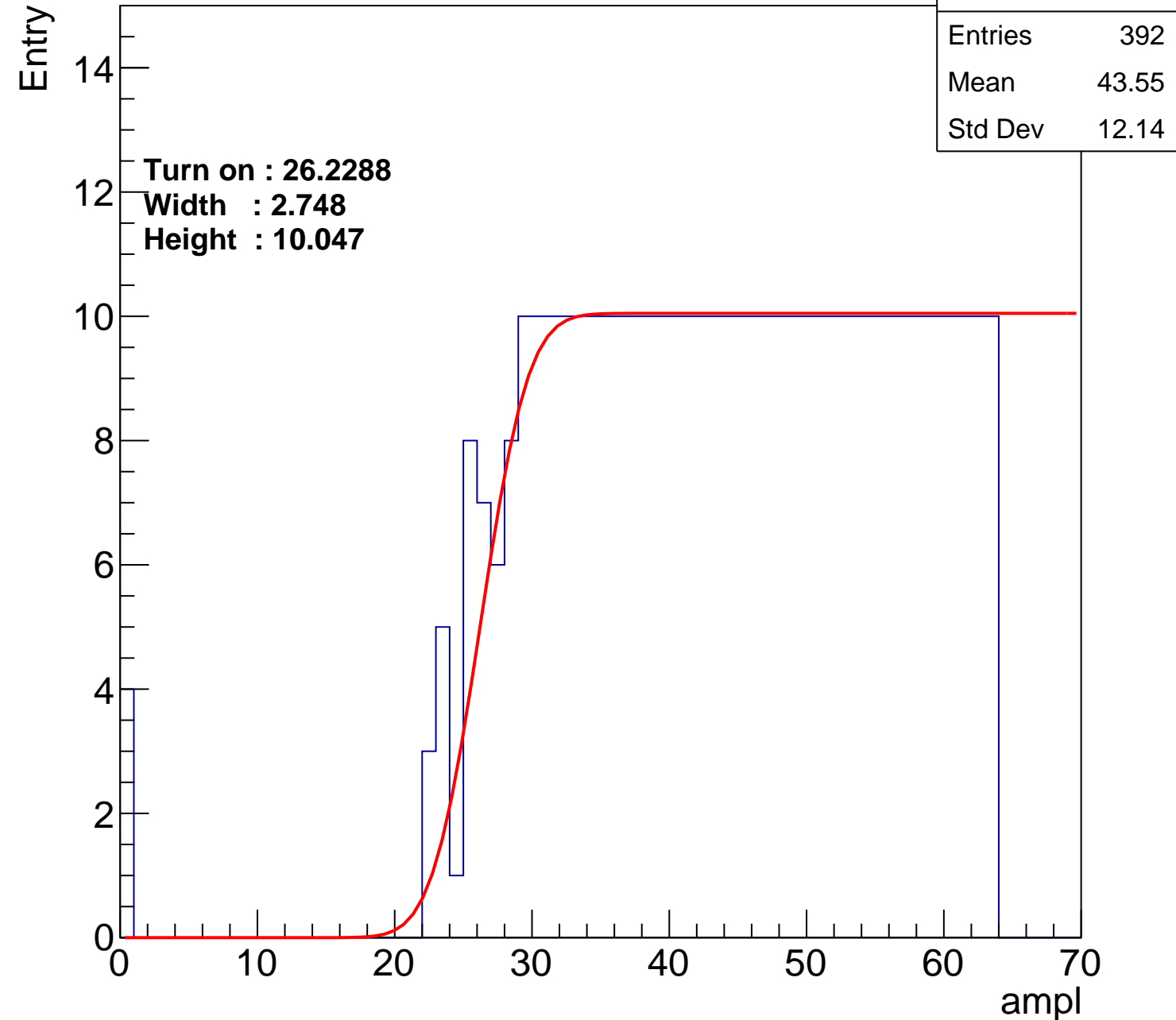
Width : 2.748

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch58

calib_packv5_042523_0143.root, FC#11, port A2

Entries	376
Mean	44.34
Std Dev	11.69

Turn on : 27.1651

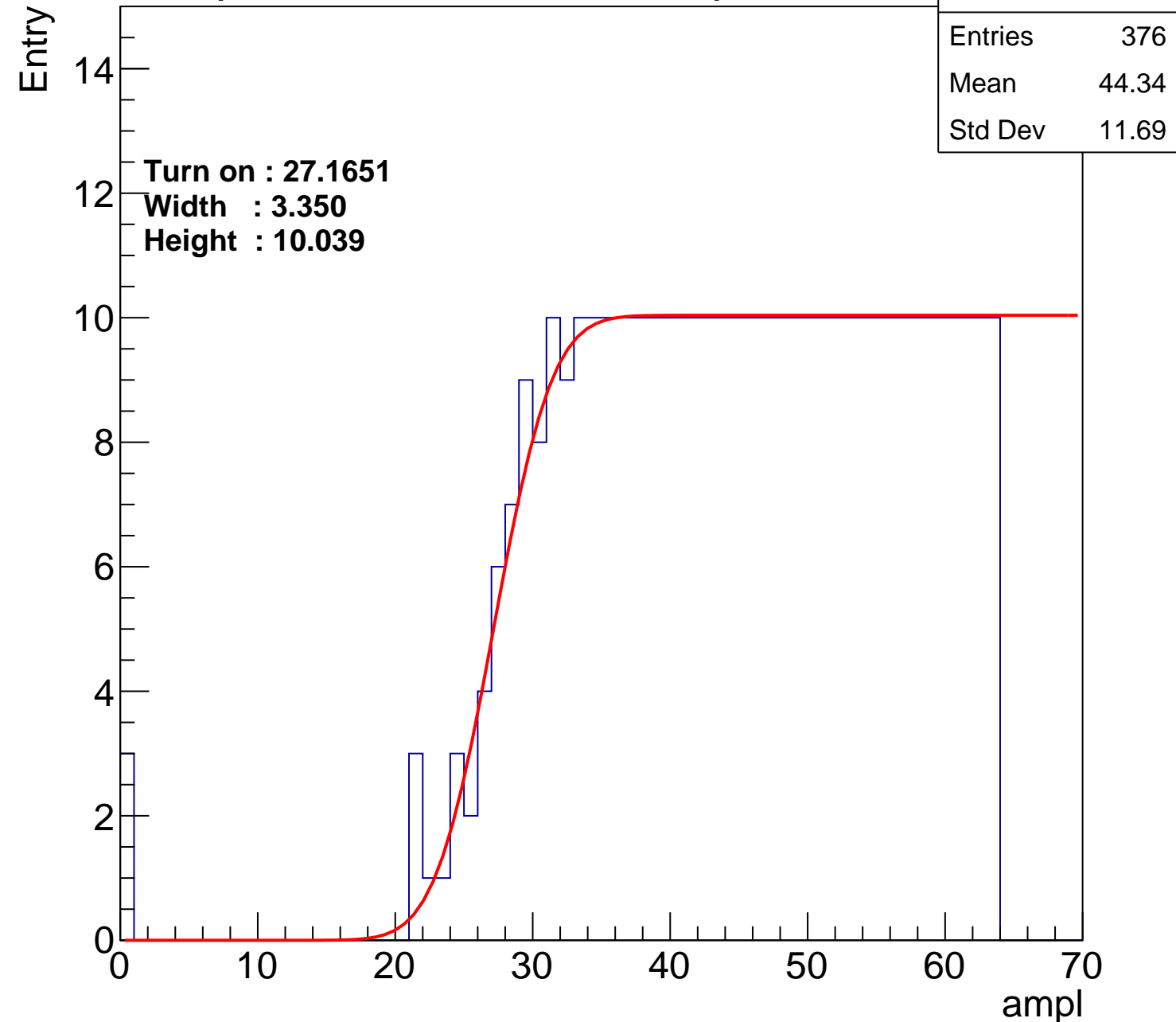
Width : 3.350

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch59

calib_packv5_042523_0143.root, FC#11, port A2

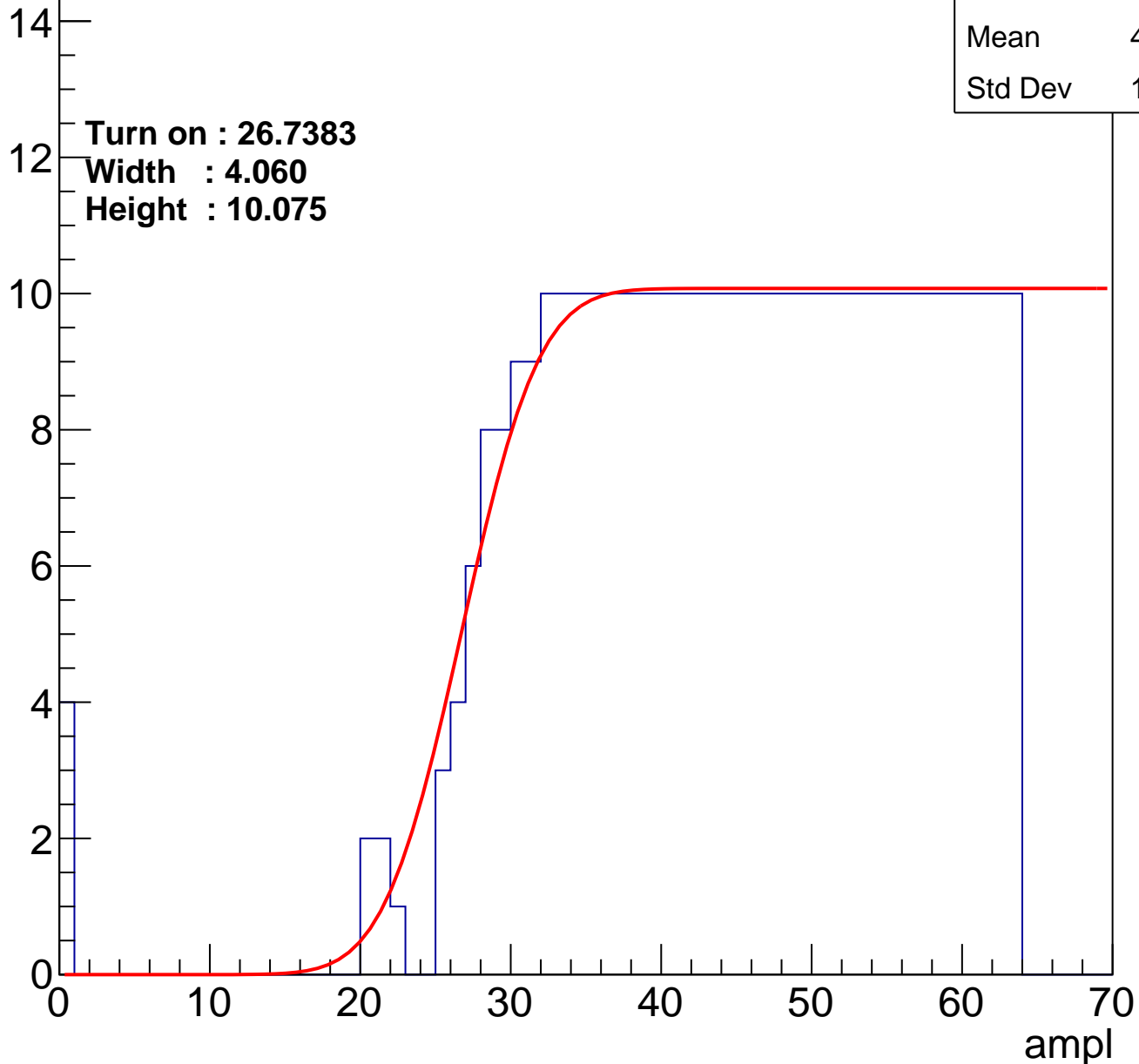
Entries	376
Mean	44.28
Std Dev	11.86

Turn on : 26.7383

Width : 4.060

Height : 10.075

Entry



B1L102S, U5-ch60

calib_packv5_042523_0143.root, FC#11, port A2

Entries	391
Mean	43.66
Std Dev	11.95

Turn on : 25.4505

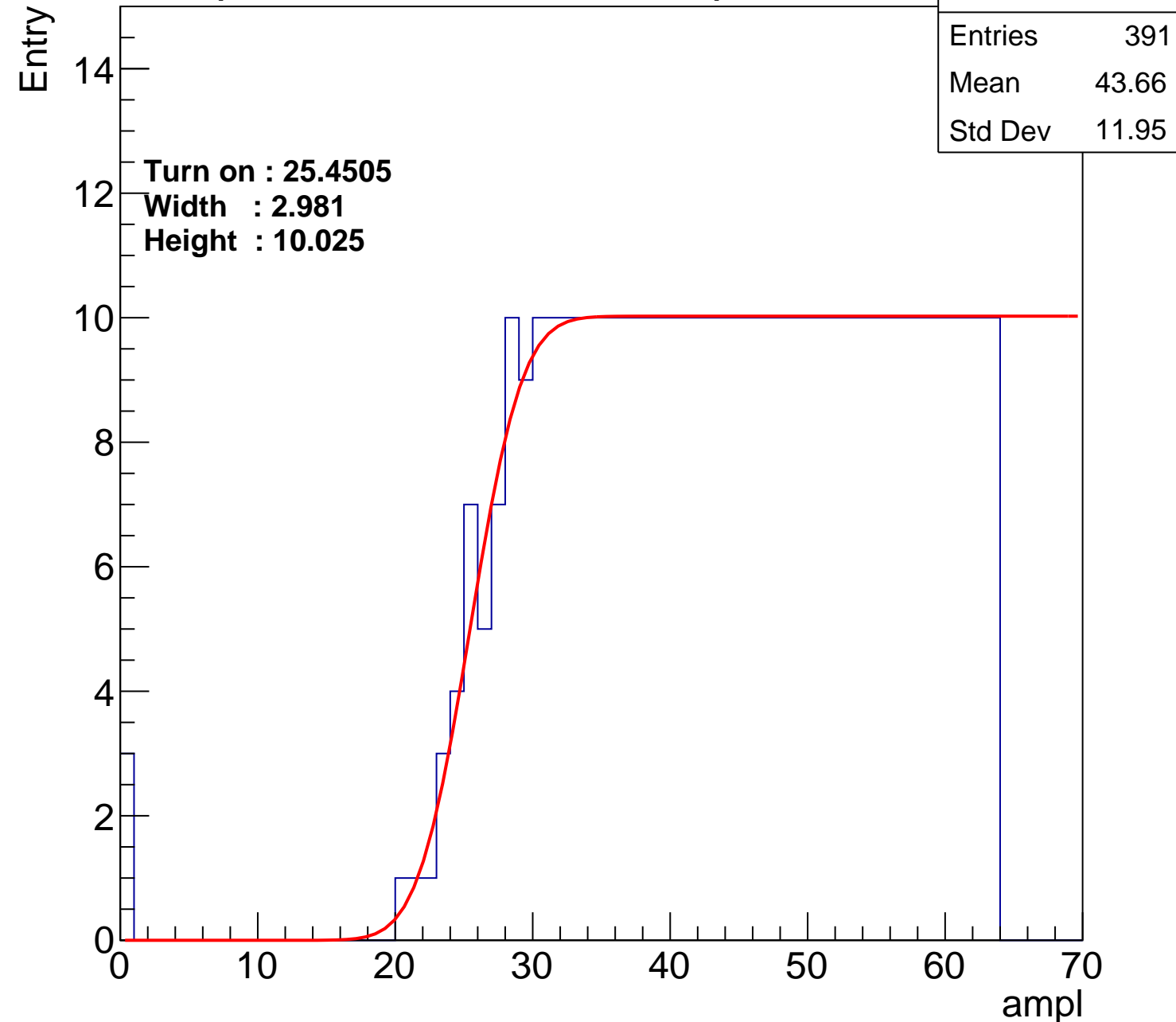
Width : 2.981

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch61

calib_packv5_042523_0143.root, FC#11, port A2

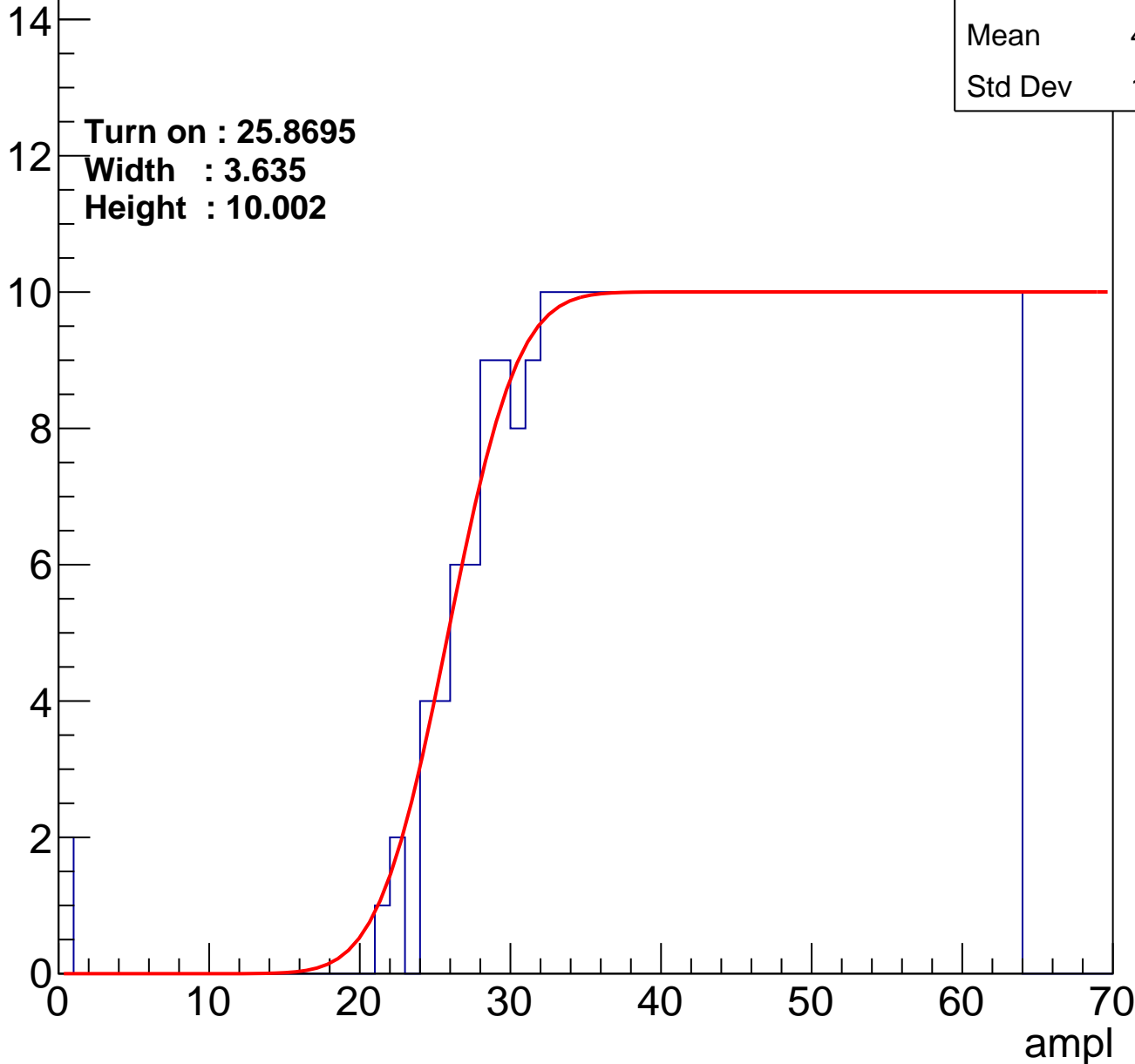
Entries	380
Mean	44.24
Std Dev	11.55

Turn on : 25.8695

Width : 3.635

Height : 10.002

Entry



B1L102S, U5-ch62

calib_packv5_042523_0143.root, FC#11, port A2

Entries	380
Mean	44.26
Std Dev	11.52

Turn on : 26.4983

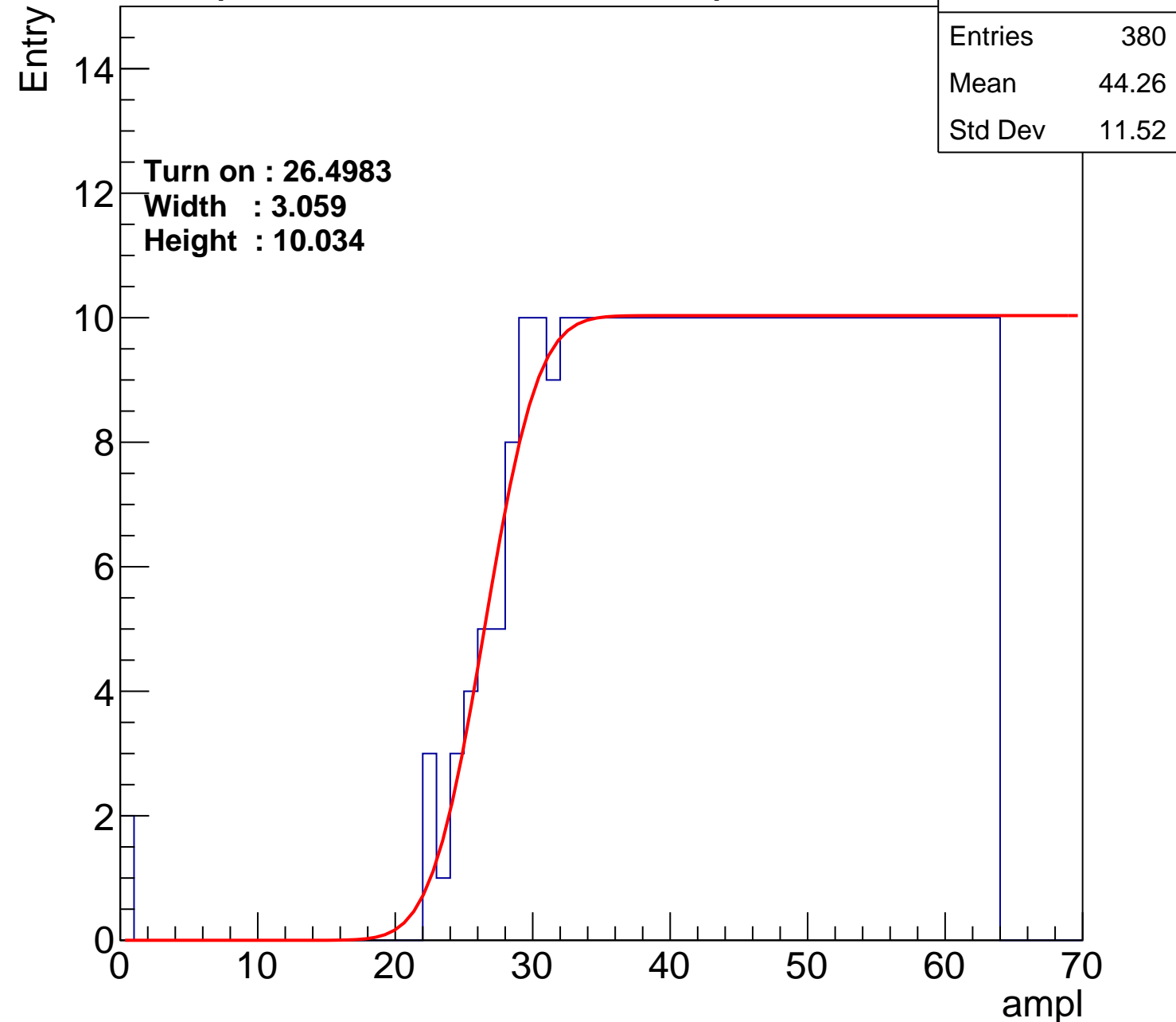
Width : 3.059

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch63

calib_packv5_042523_0143.root, FC#11, port A2

Entries	387
Mean	43.98
Std Dev	11.52

Turn on : 25.5044

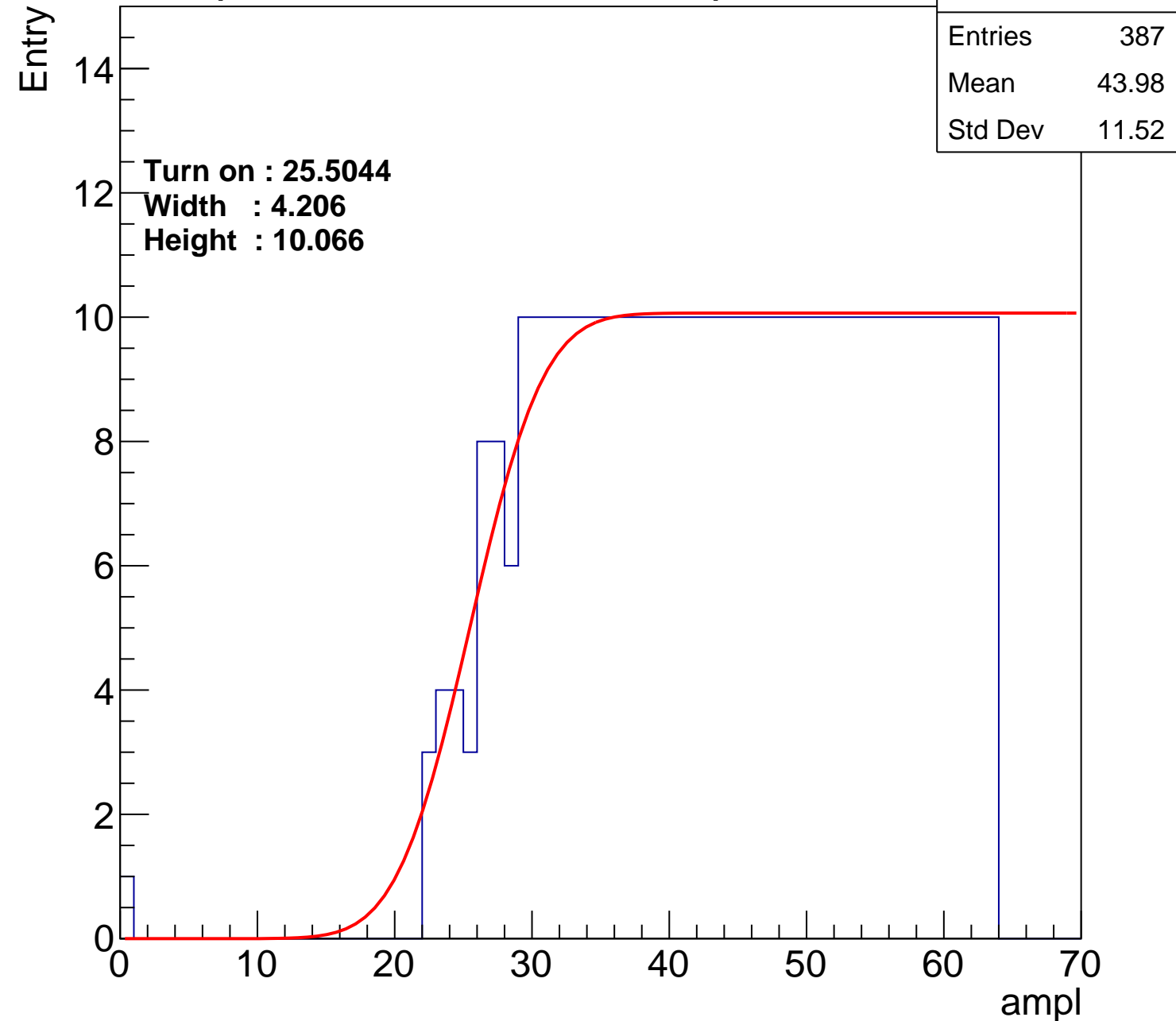
Width : 4.206

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch64

calib_packv5_042523_0143.root, FC#11, port A2

Entries	374
Mean	44.42
Std Dev	11.67

Turn on : 27.2633

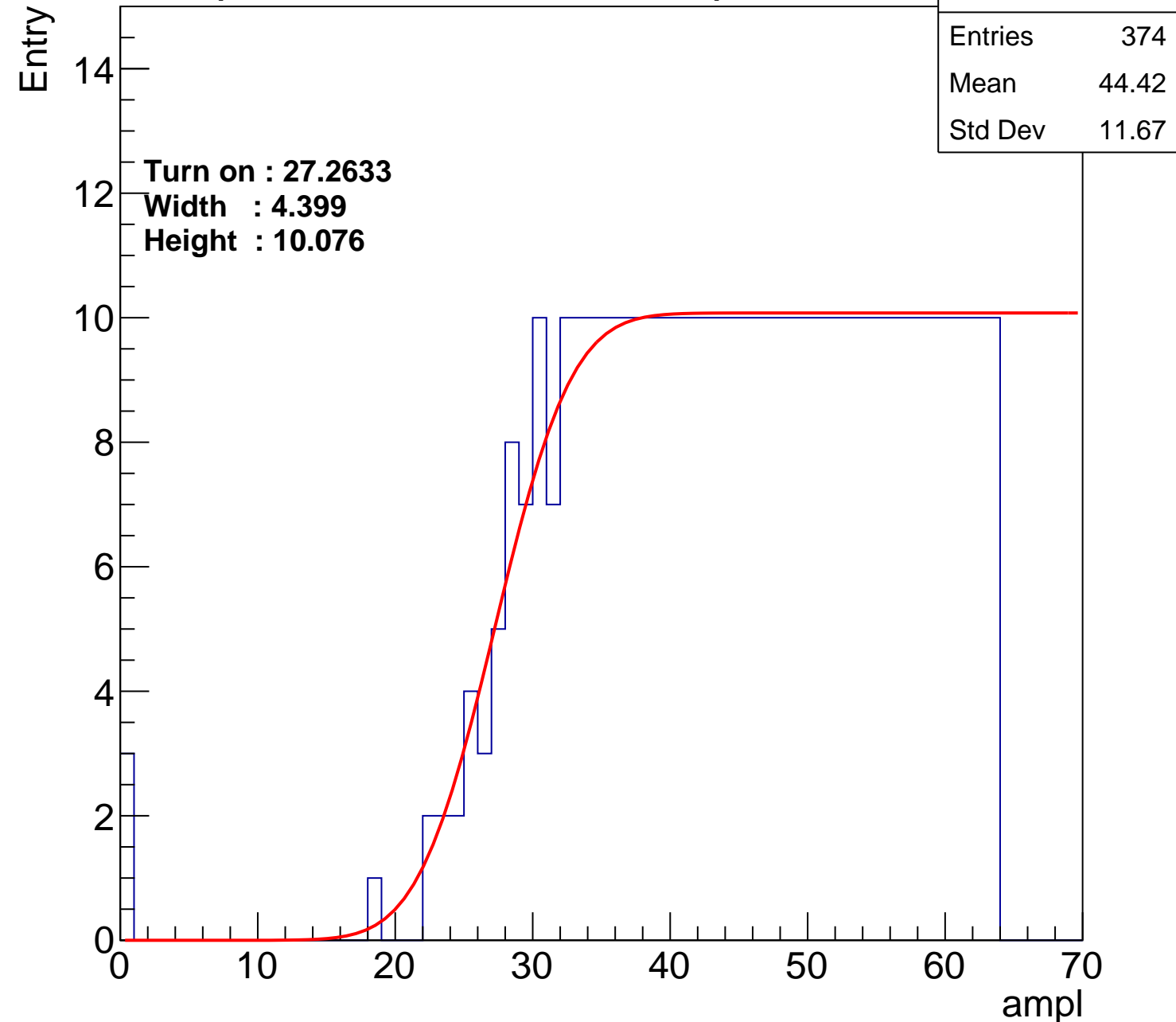
Width : 4.399

Height : 10.076

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch65

calib_packv5_042523_0143.root, FC#11, port A2

Entries	403
Mean	43.02
Std Dev	12.4

Turn on : 24.6282

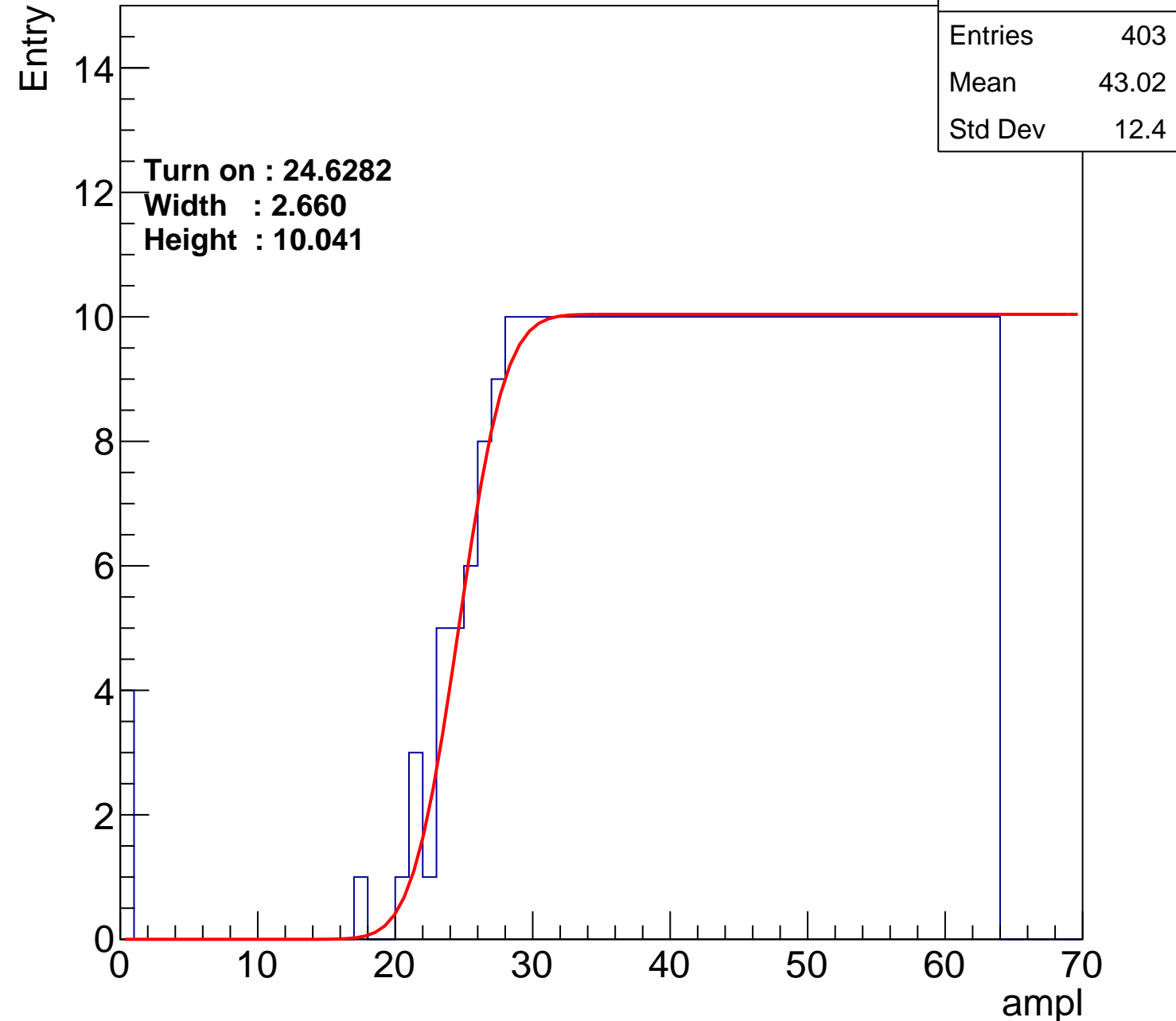
Width : 2.660

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch66

calib_packv5_042523_0143.root, FC#11, port A2

Entries	398
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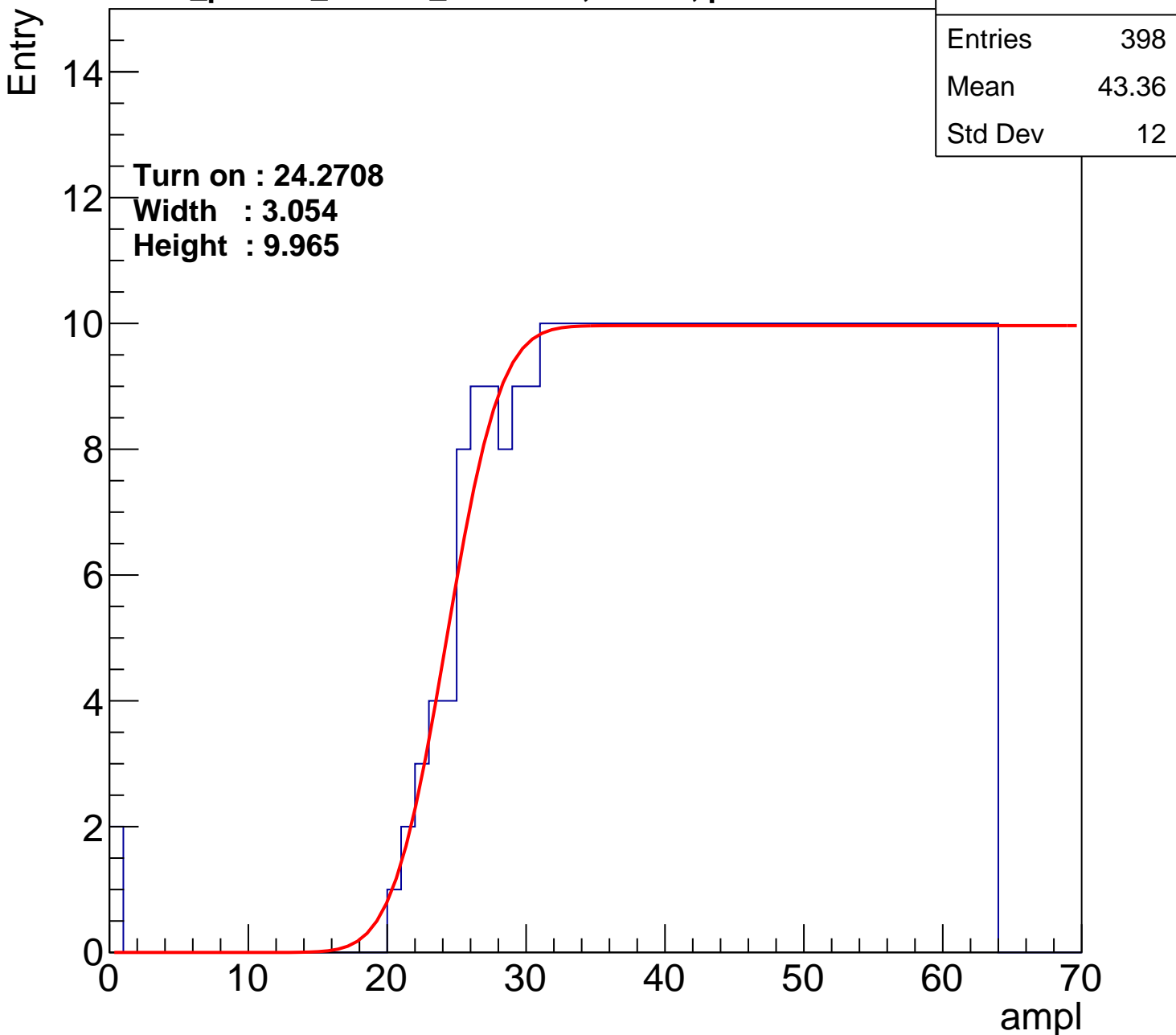
Mean	43.36
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Std Dev	12
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Turn on : 24.2708

Width : 3.054

Height : 9.965



B1L102S, U5-ch67

calib_packv5_042523_0143.root, FC#11, port A2

Entries	370
Mean	44.86
Std Dev	11

Turn on : 27.4893

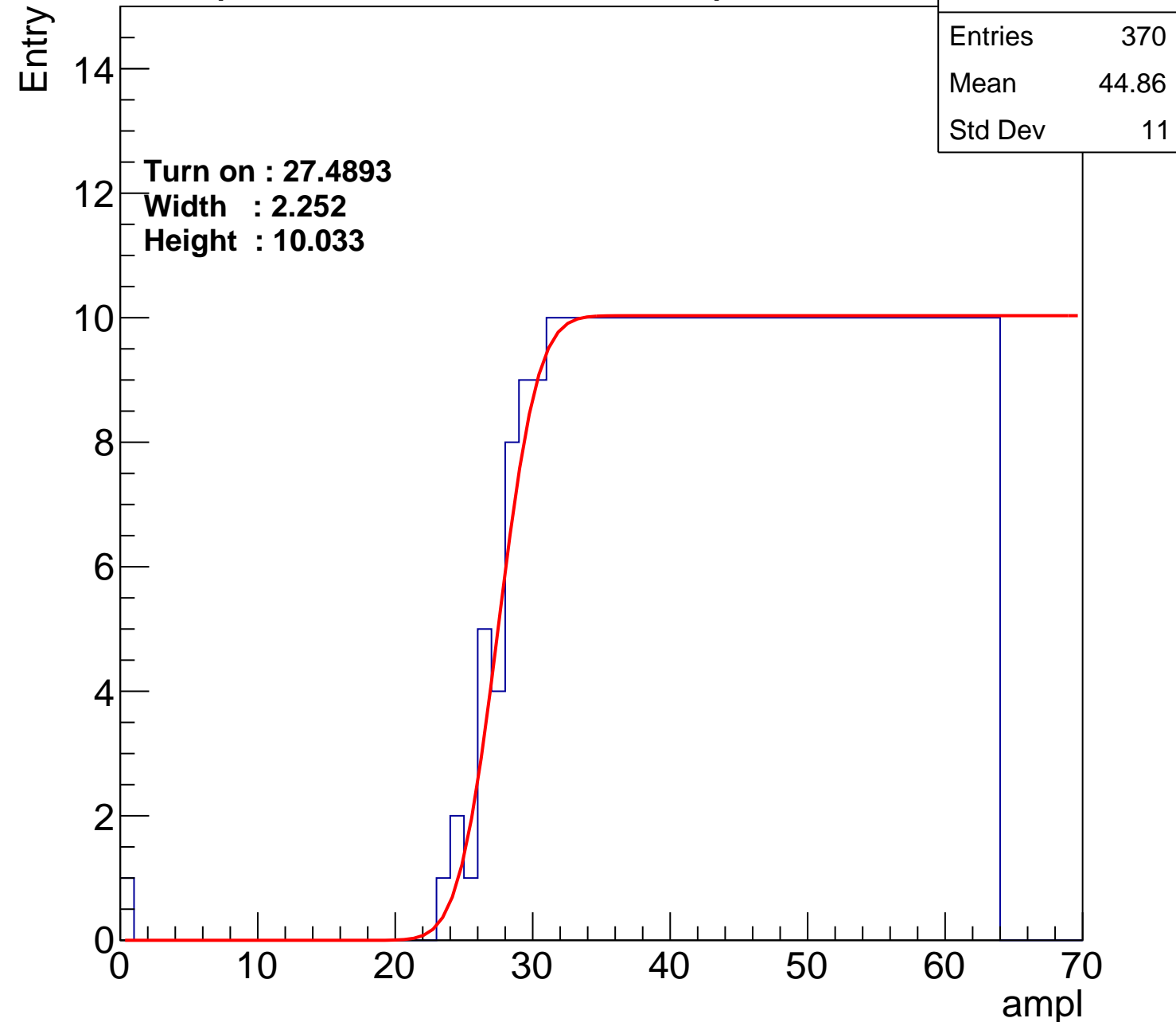
Width : 2.252

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch68

calib_packv5_042523_0143.root, FC#11, port A2

Entries	385
Mean	44.03
Std Dev	11.55

Turn on : 26.0388

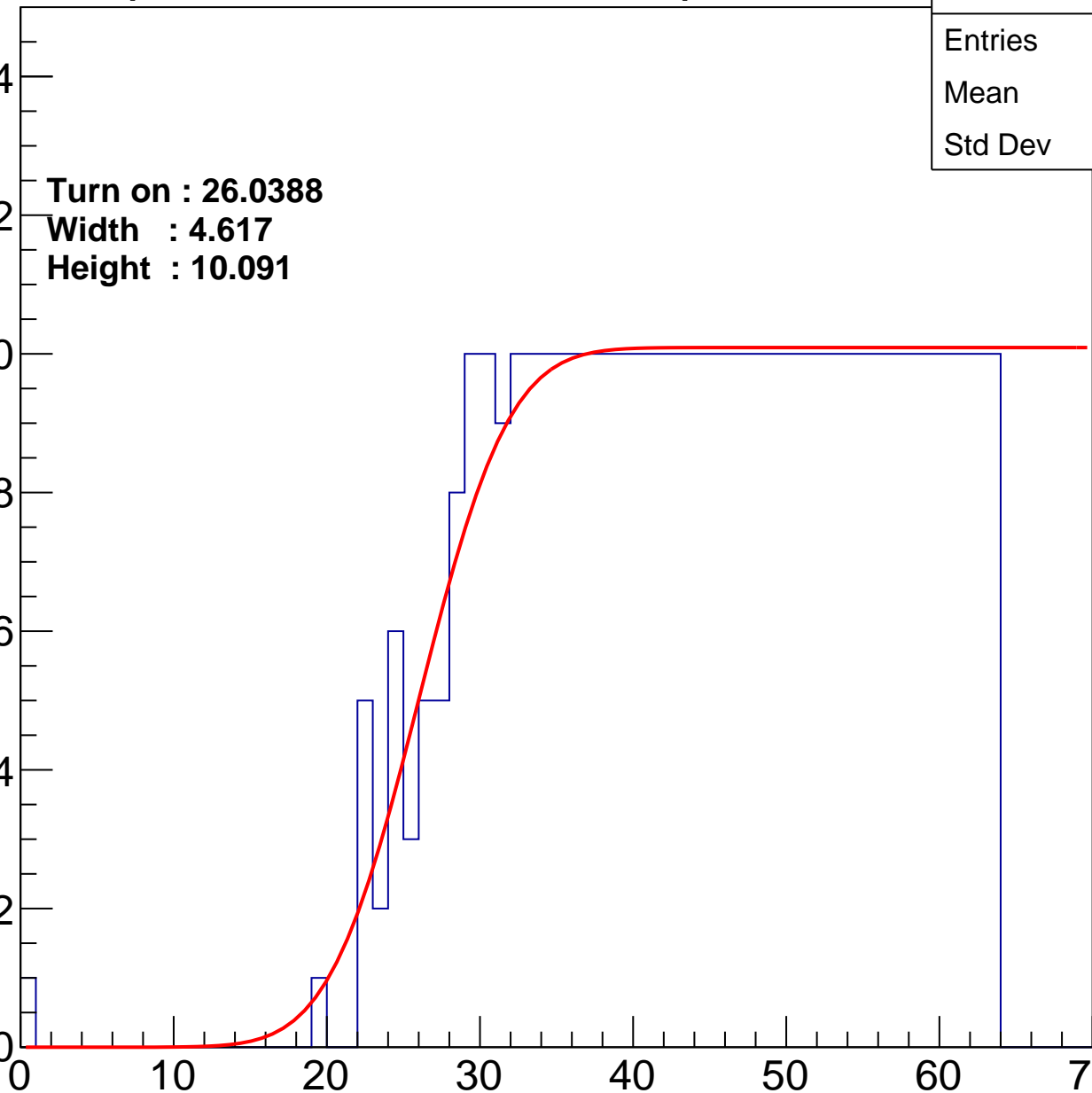
Width : 4.617

Height : 10.091

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch69

calib_packv5_042523_0143.root, FC#11, port A2

Entries	412
Mean	42.55
Std Dev	12.72

Turn on : 23.3036

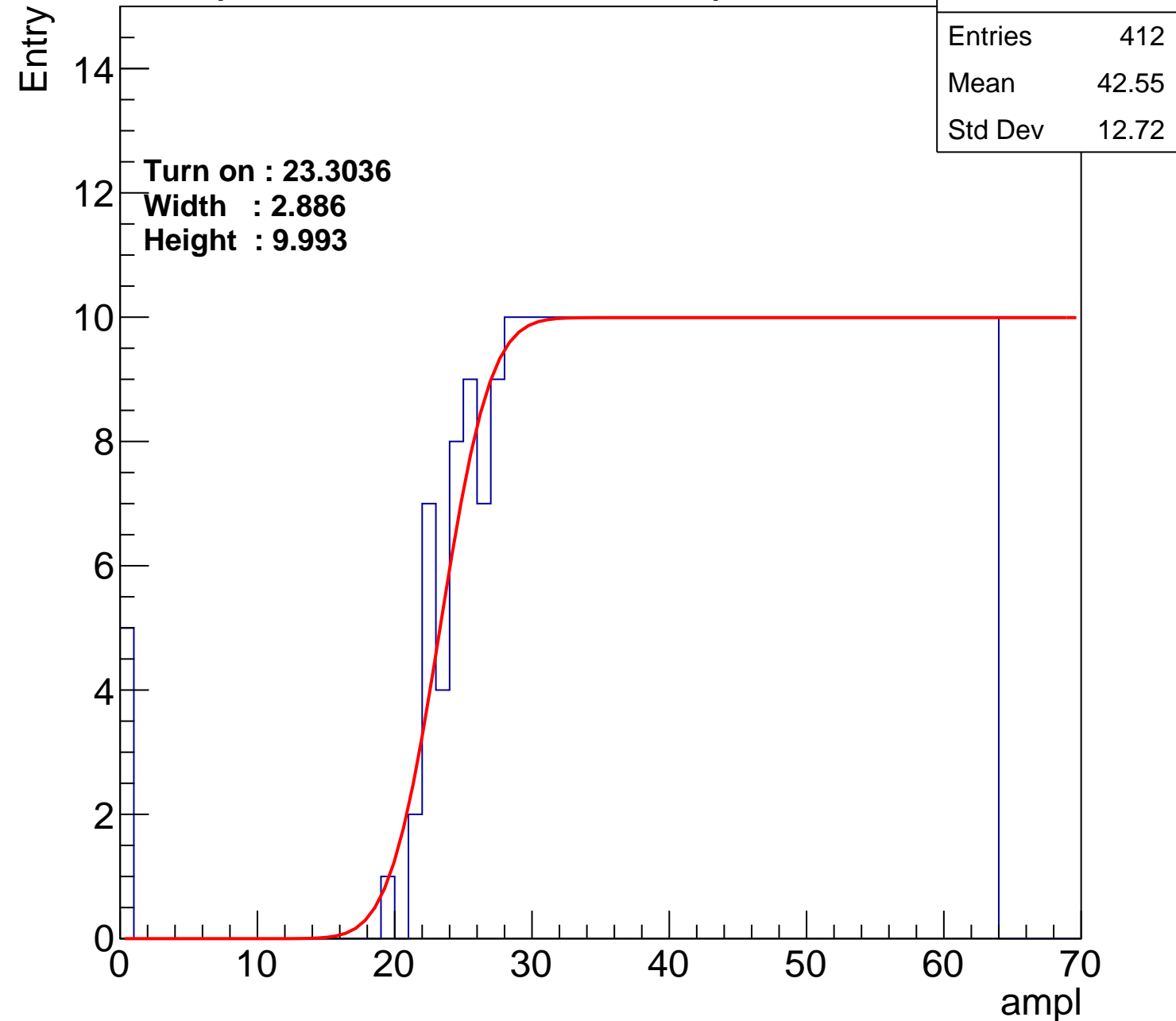
Width : 2.886

Height : 9.993

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch70

calib_packv5_042523_0143.root, FC#11, port A2

Entries	382
Mean	44.11
Std Dev	11.66

Turn on : 27.9254

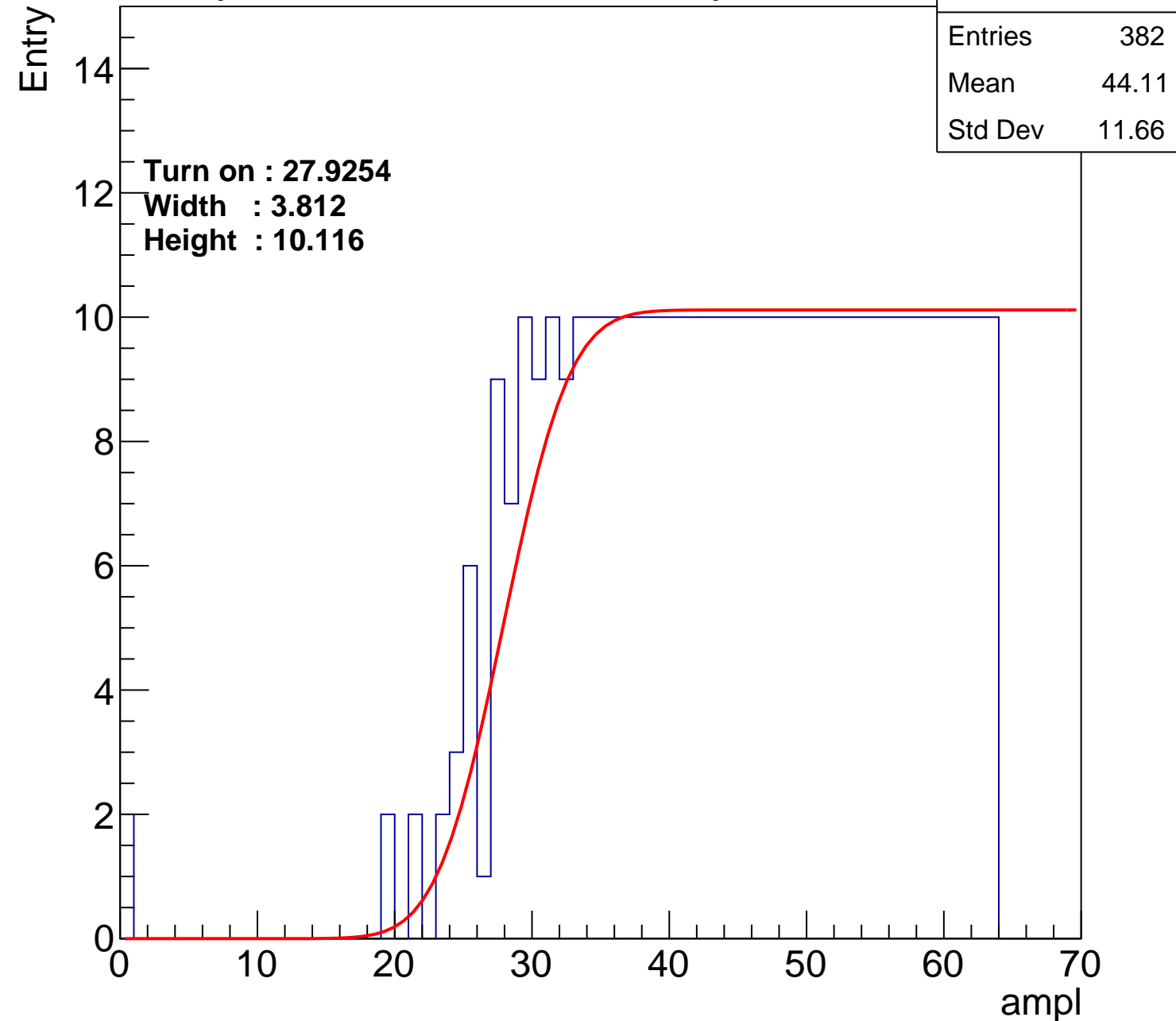
Width : 3.812

Height : 10.116

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch71

calib_packv5_042523_0143.root, FC#11, port A2

Entries	391
Mean	43.46
Std Dev	12.4

Turn on : 26.0028

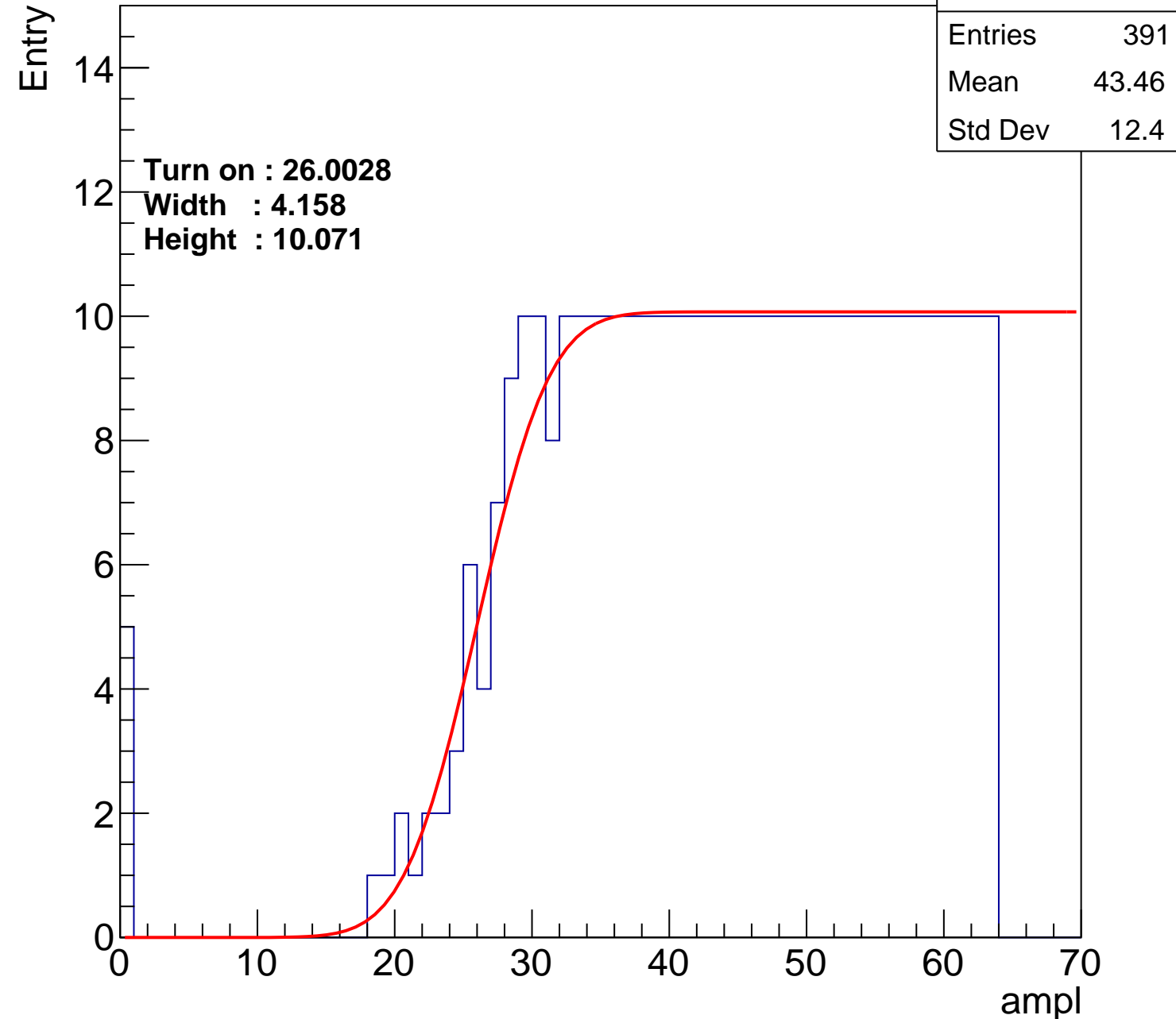
Width : 4.158

Height : 10.071

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch72

calib_packv5_042523_0143.root, FC#11, port A2

Entries	414
Mean	42.59
Std Dev	12.4

Turn on : 22.9180

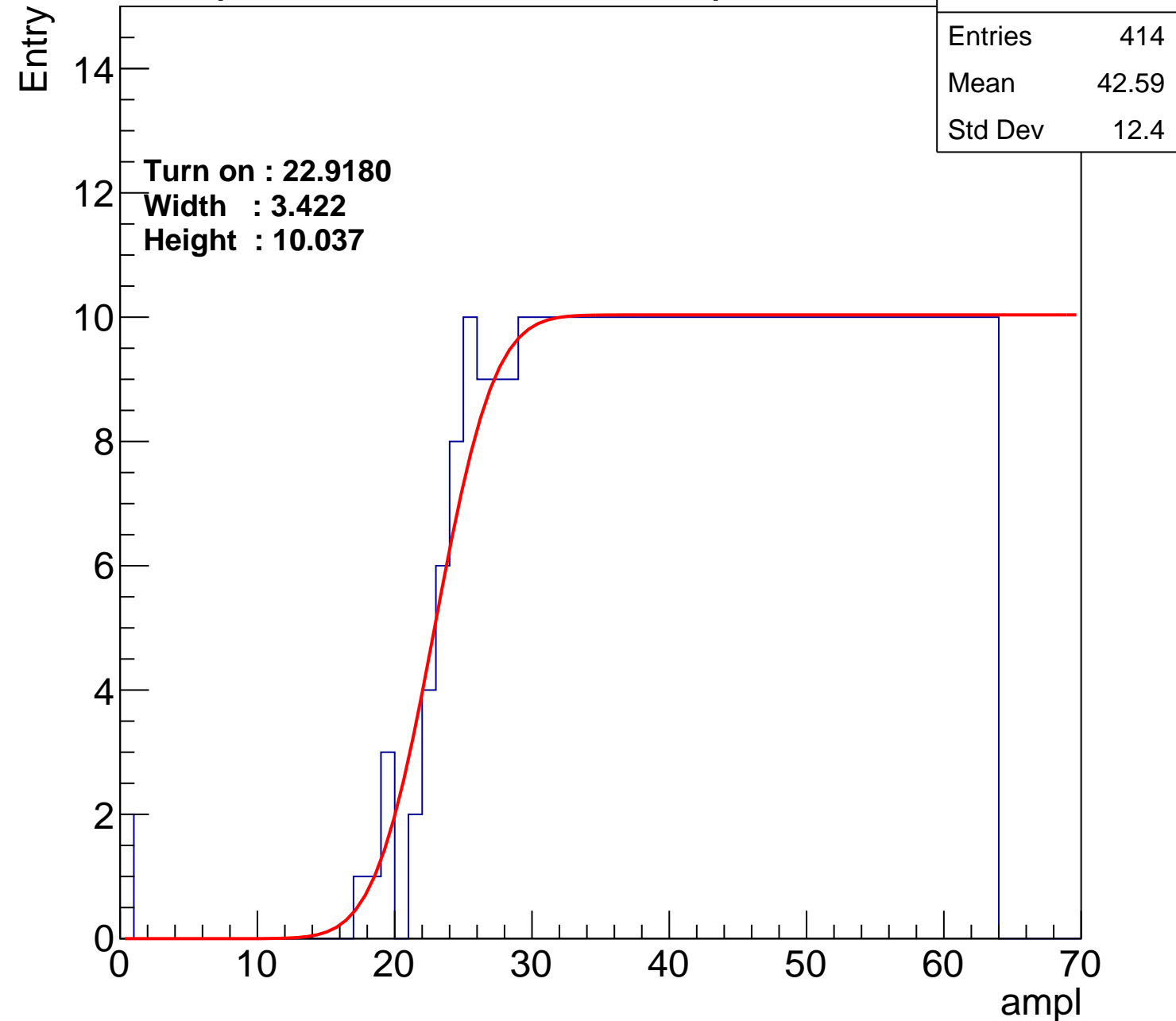
Width : 3.422

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch73

calib_packv5_042523_0143.root, FC#11, port A2

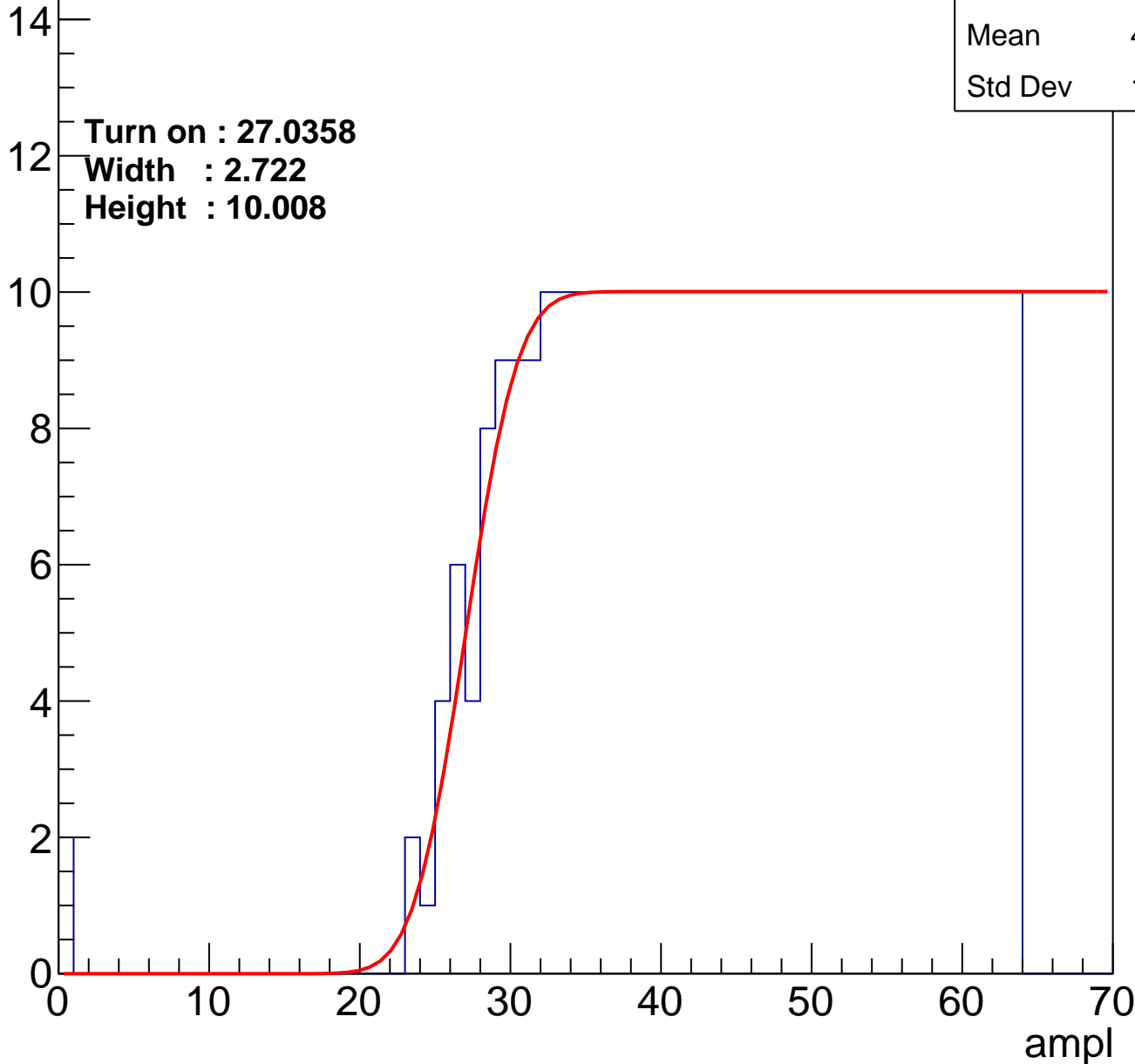
Entries	374
Mean	44.57
Std Dev	11.34

Turn on : 27.0358

Width : 2.722

Height : 10.008

Entry



B1L102S, U5-ch74

calib_packv5_042523_0143.root, FC#11, port A2

Entries	393
Mean	43.56
Std Dev	12.02

Turn on : 25.3374

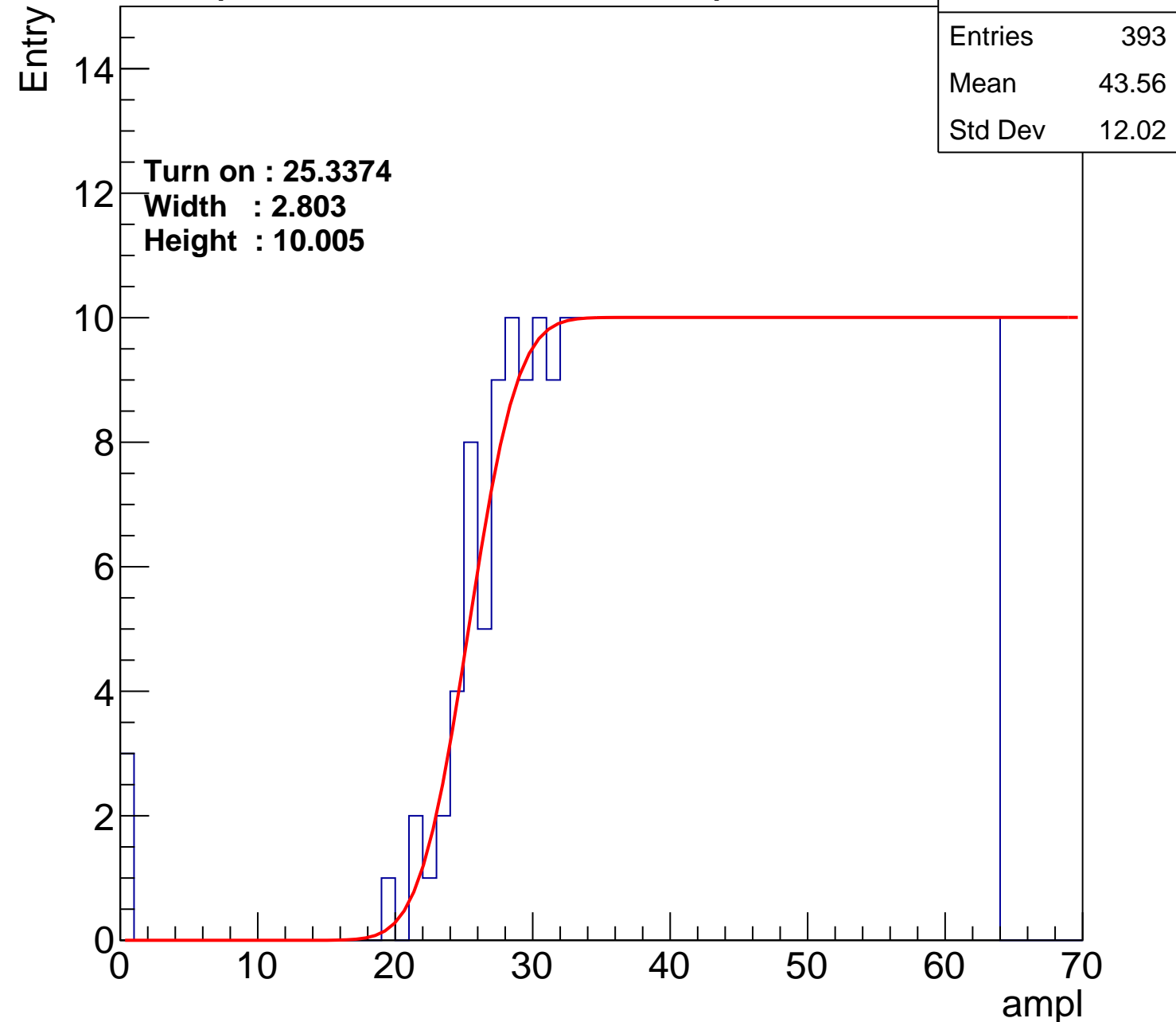
Width : 2.803

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch75

calib_packv5_042523_0143.root, FC#11, port A2

Entries	387
Mean	43.78
Std Dev	12.05

Turn on : 25.7510

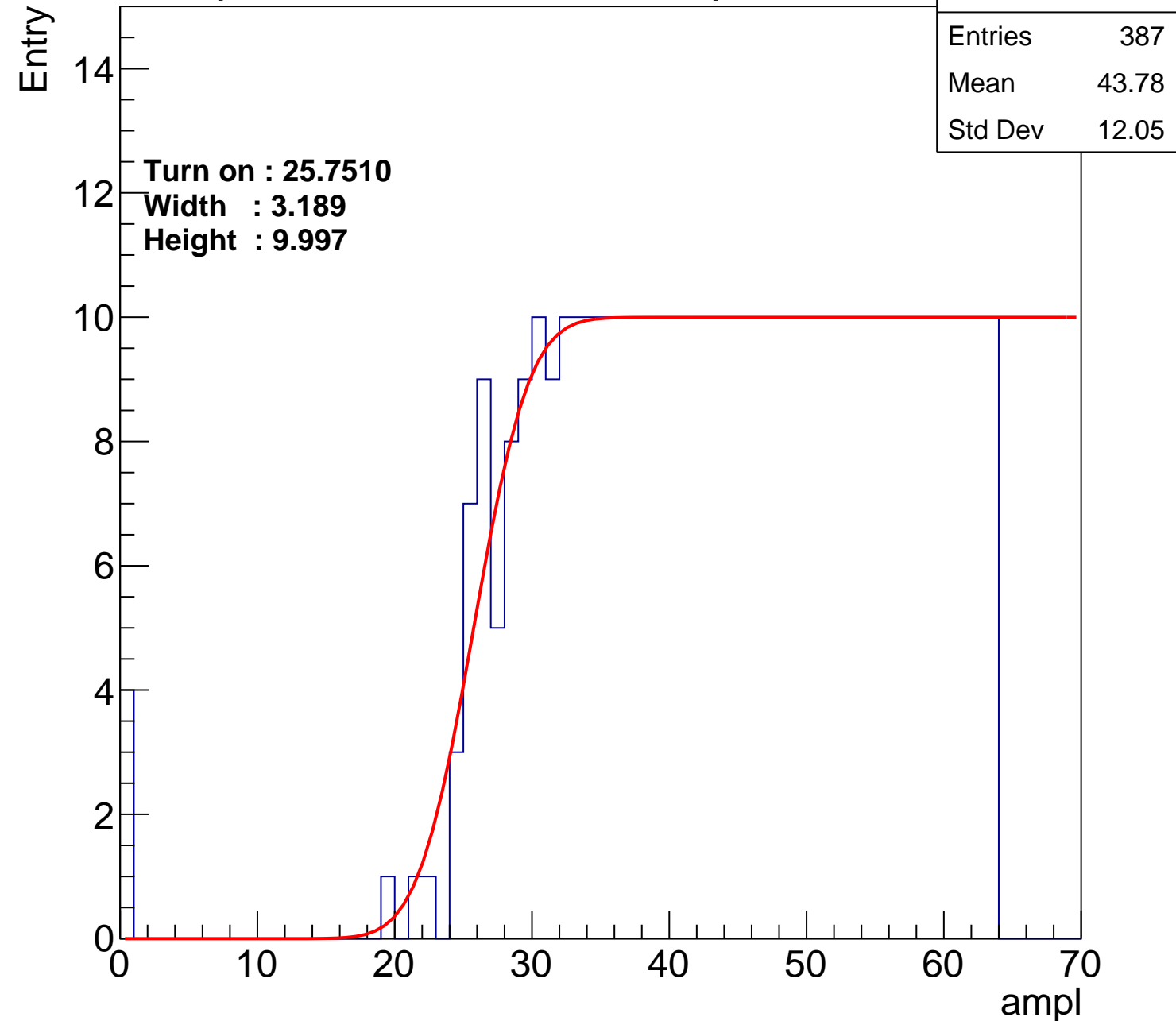
Width : 3.189

Height : 9.997

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch76

calib_packv5_042523_0143.root, FC#11, port A2

Entries	378
Mean	44.18
Std Dev	11.9

Turn on : 26.9319

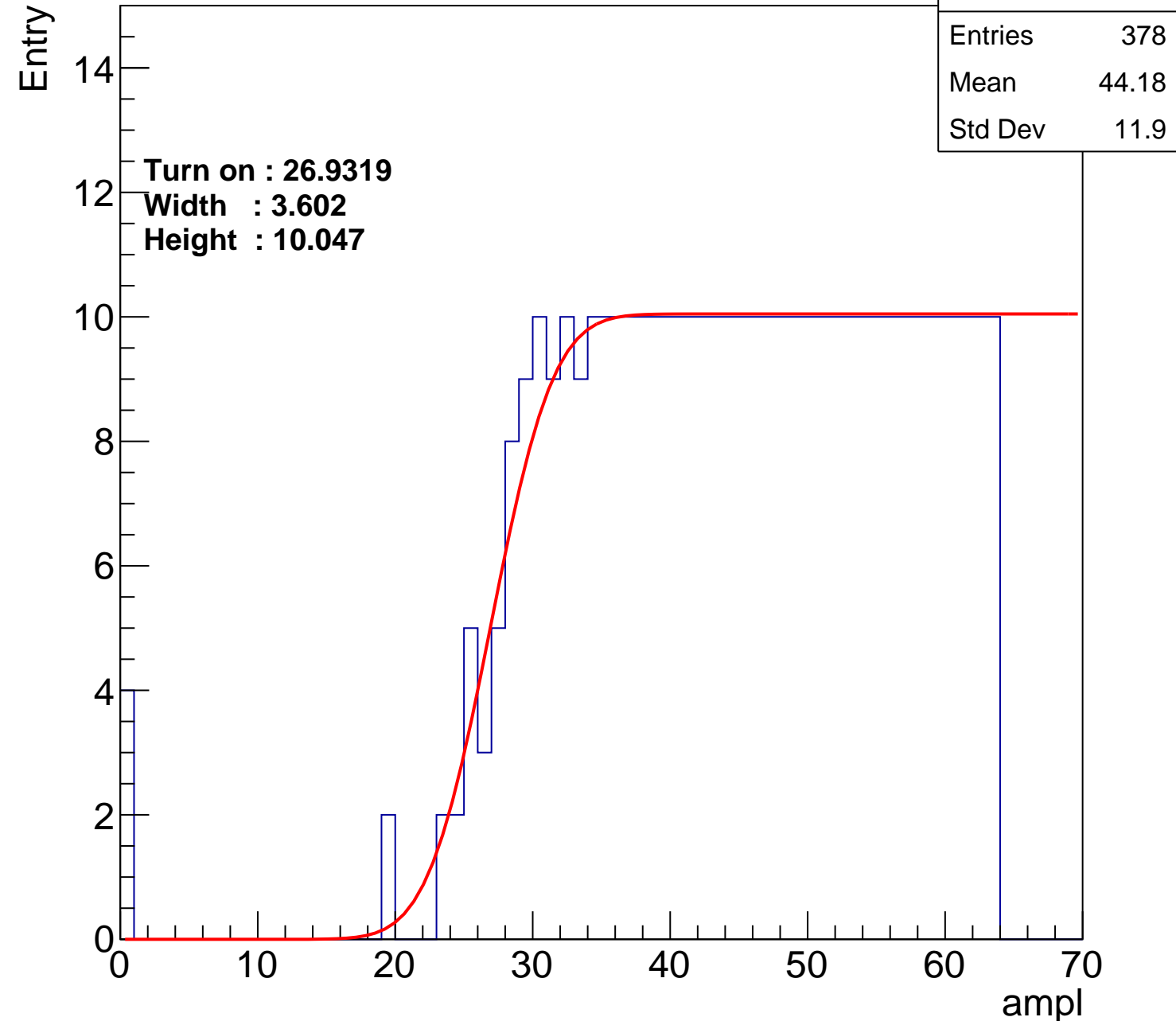
Width : 3.602

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch77

calib_packv5_042523_0143.root, FC#11, port A2

Entries	387
Mean	43.98
Std Dev	11.52

Turn on : 25.1104

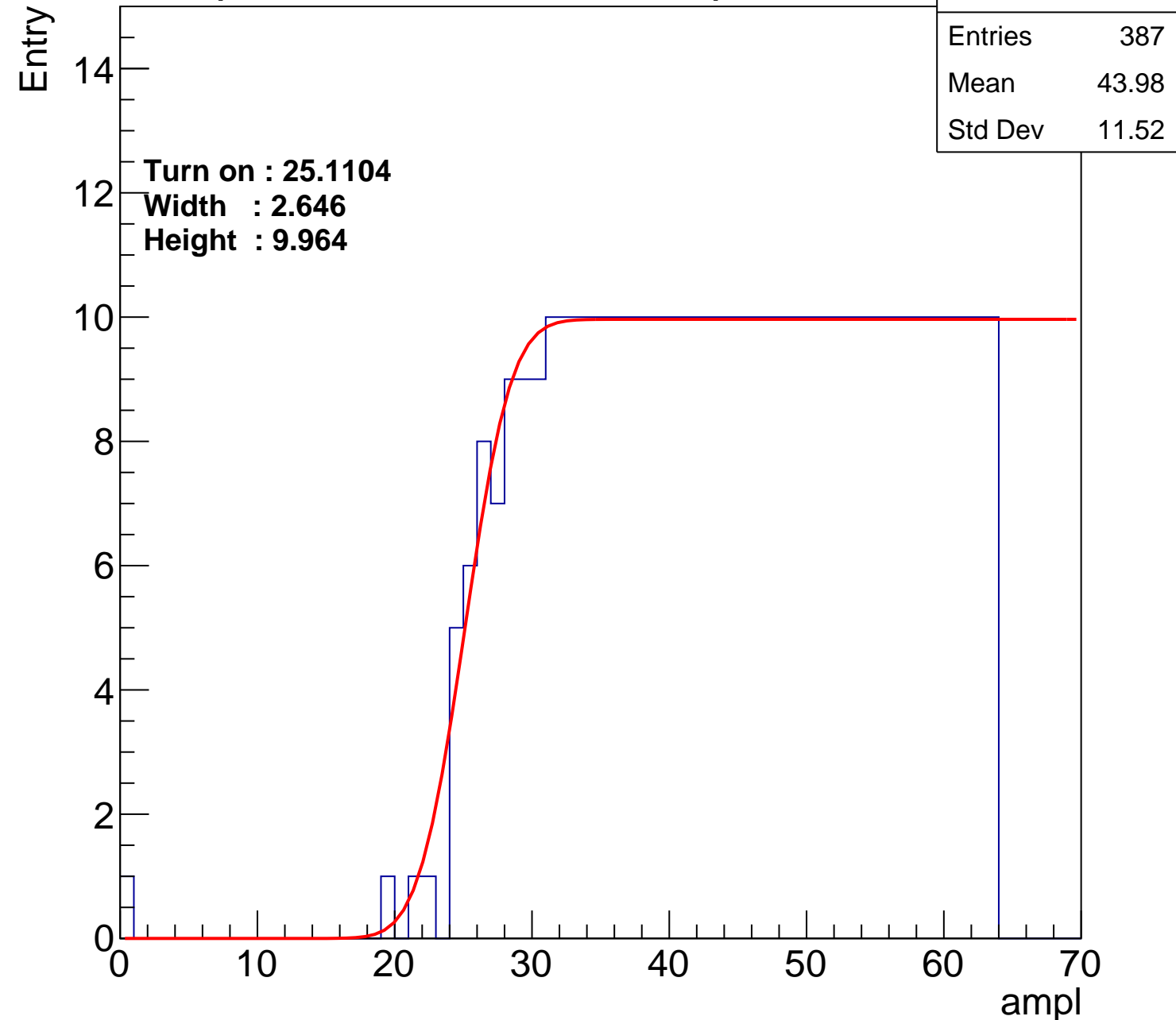
Width : 2.646

Height : 9.964

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch78

calib_packv5_042523_0143.root, FC#11, port A2

Entries	377
Mean	44.38
Std Dev	11.4

Turn on : 26.7357

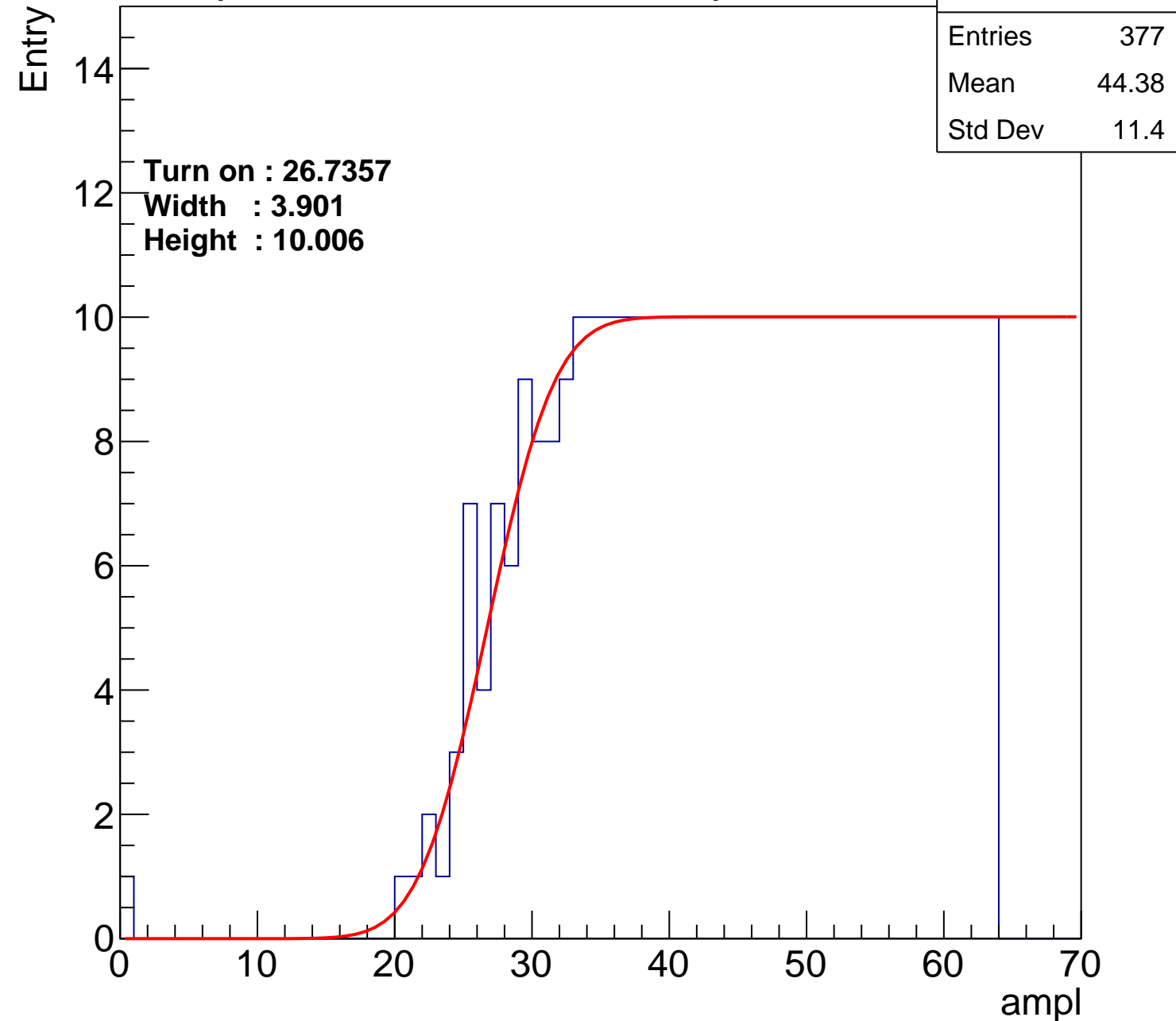
Width : 3.901

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch79

calib_packv5_042523_0143.root, FC#11, port A2

Entries	392
Mean	43.55
Std Dev	12.14

Turn on : 25.4237

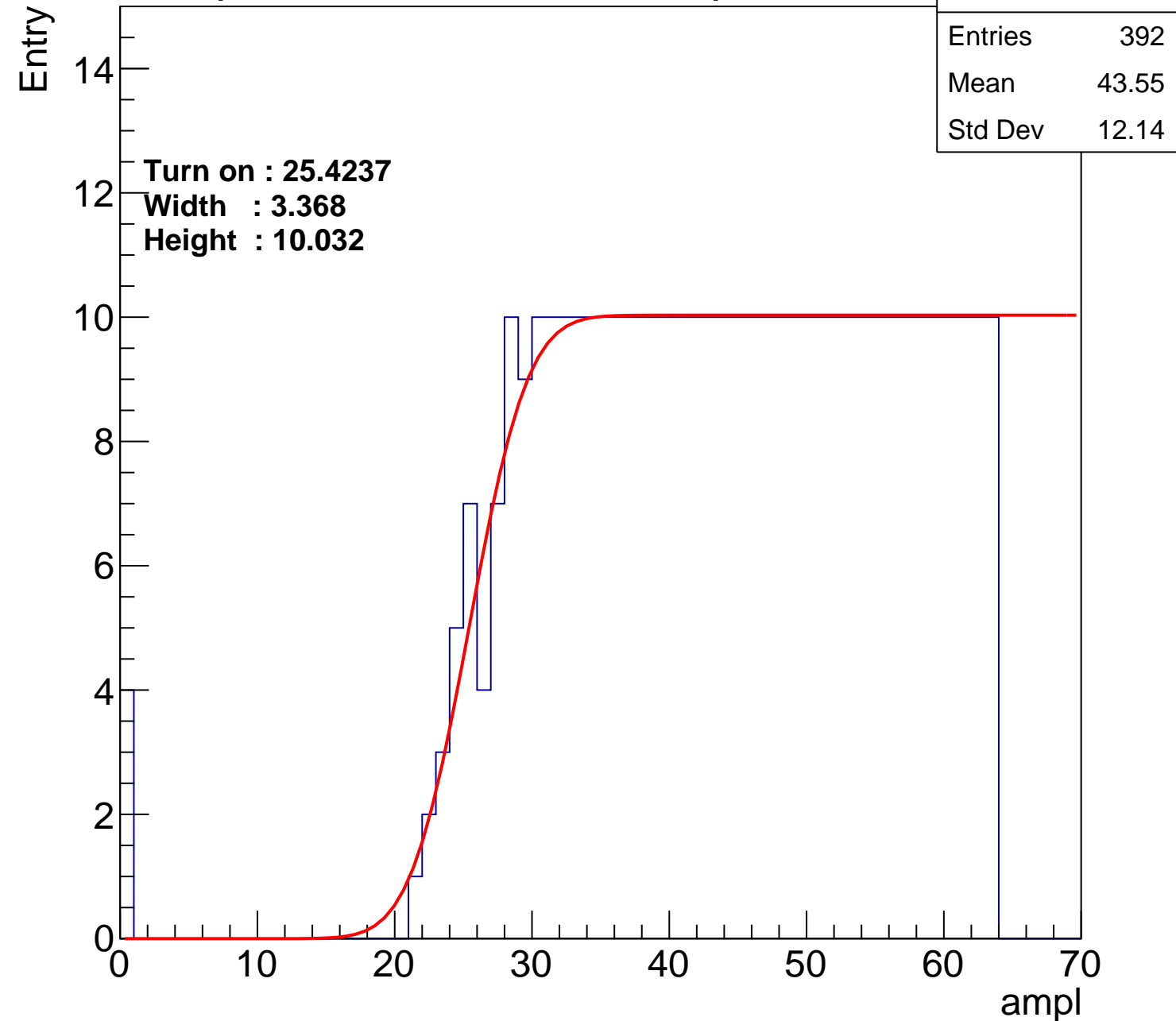
Width : 3.368

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch80

calib_packv5_042523_0143.root, FC#11, port A2

Entries	404
Mean	43.05
Std Dev	12.18

Turn on : 24.0013

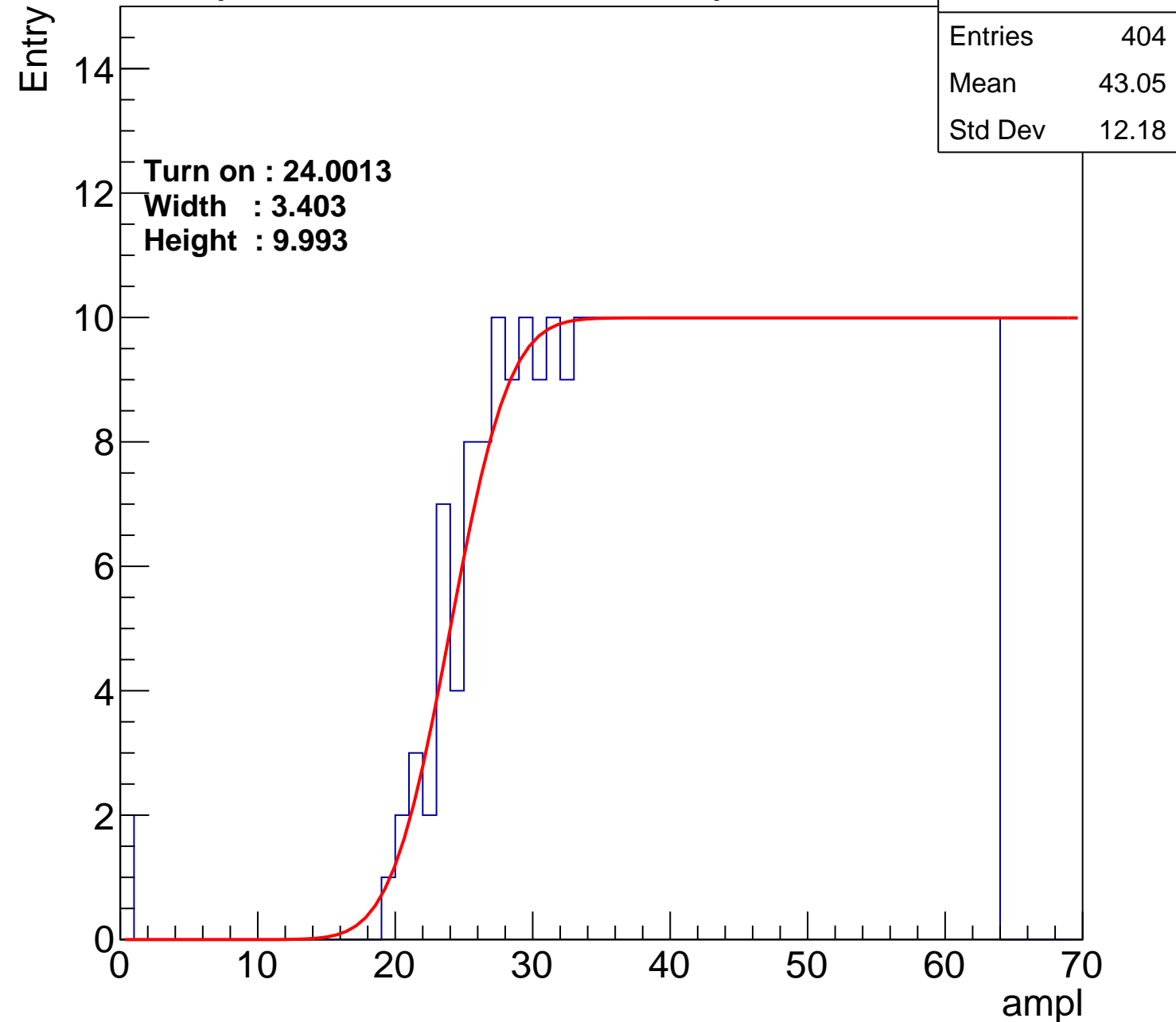
Width : 3.403

Height : 9.993

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch81

calib_packv5_042523_0143.root, FC#11, port A2

Entries	390
Mean	43.73
Std Dev	11.89

Turn on : 25.2397

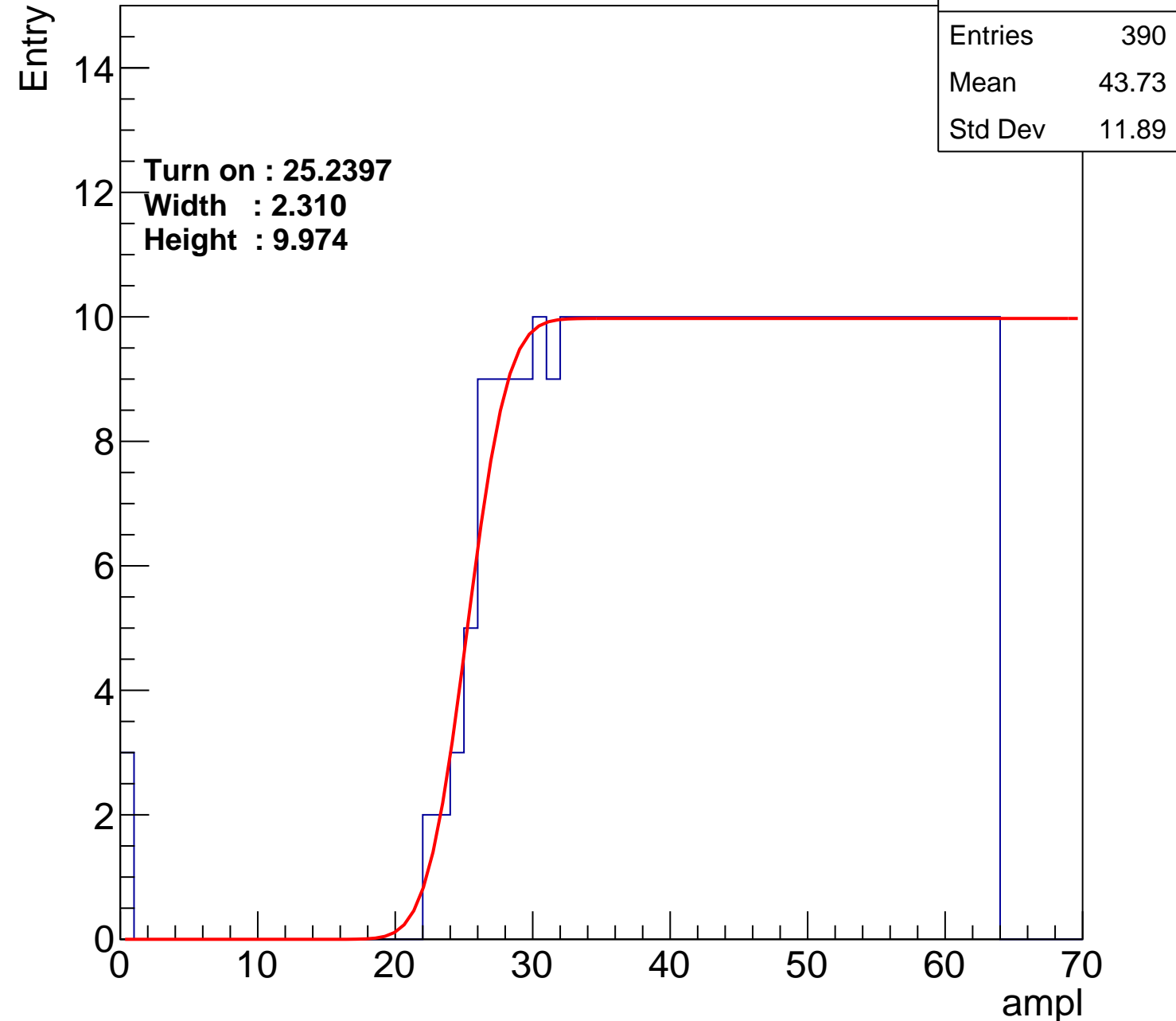
Width : 2.310

Height : 9.974

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch82

calib_packv5_042523_0143.root, FC#11, port A2

Entries	379
Mean	44.24
Std Dev	11.68

Turn on : 27.3475

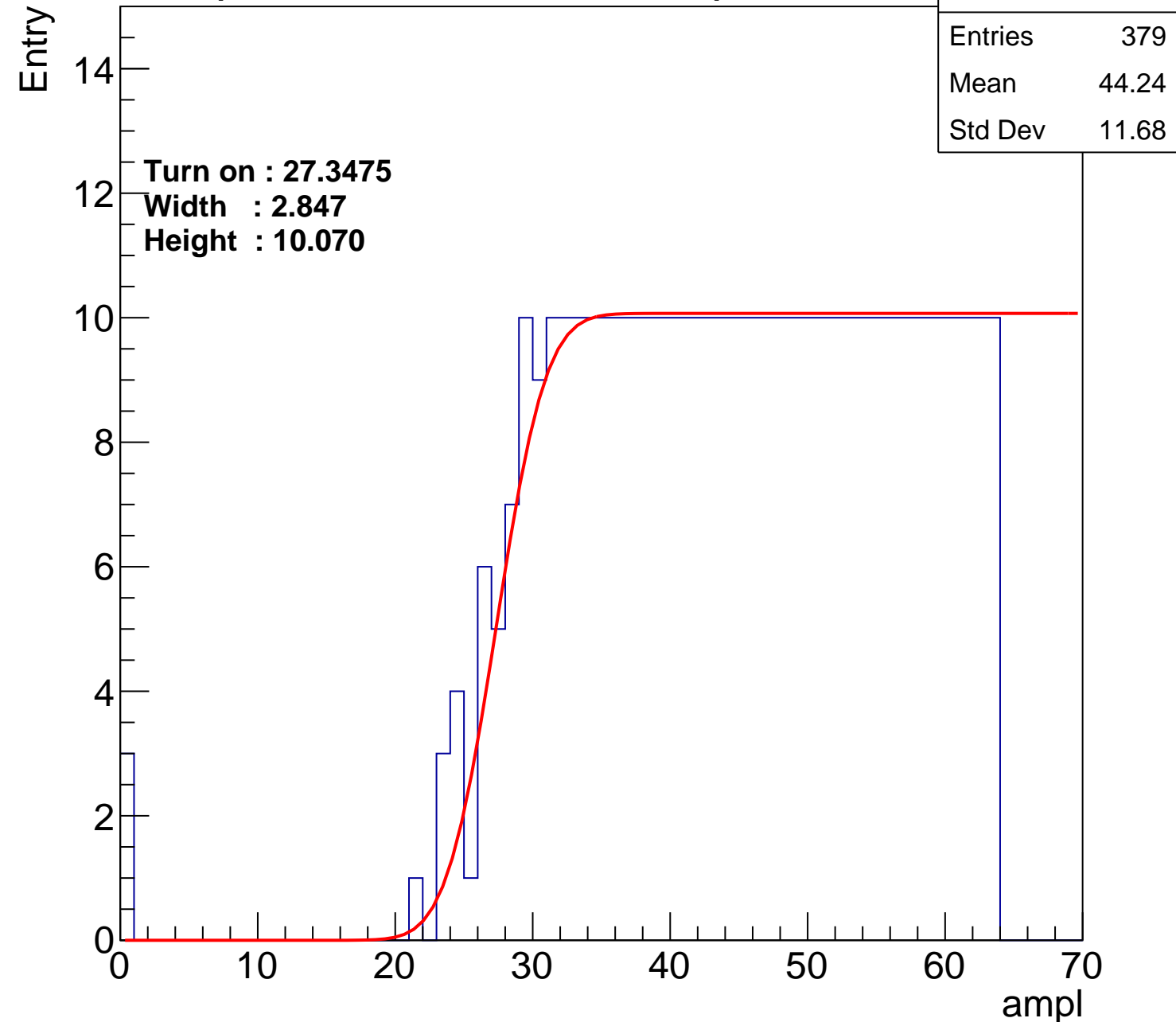
Width : 2.847

Height : 10.070

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch83

calib_packv5_042523_0143.root, FC#11, port A2

Entries	383
Mean	44.04
Std Dev	11.79

Turn on : 26.1947

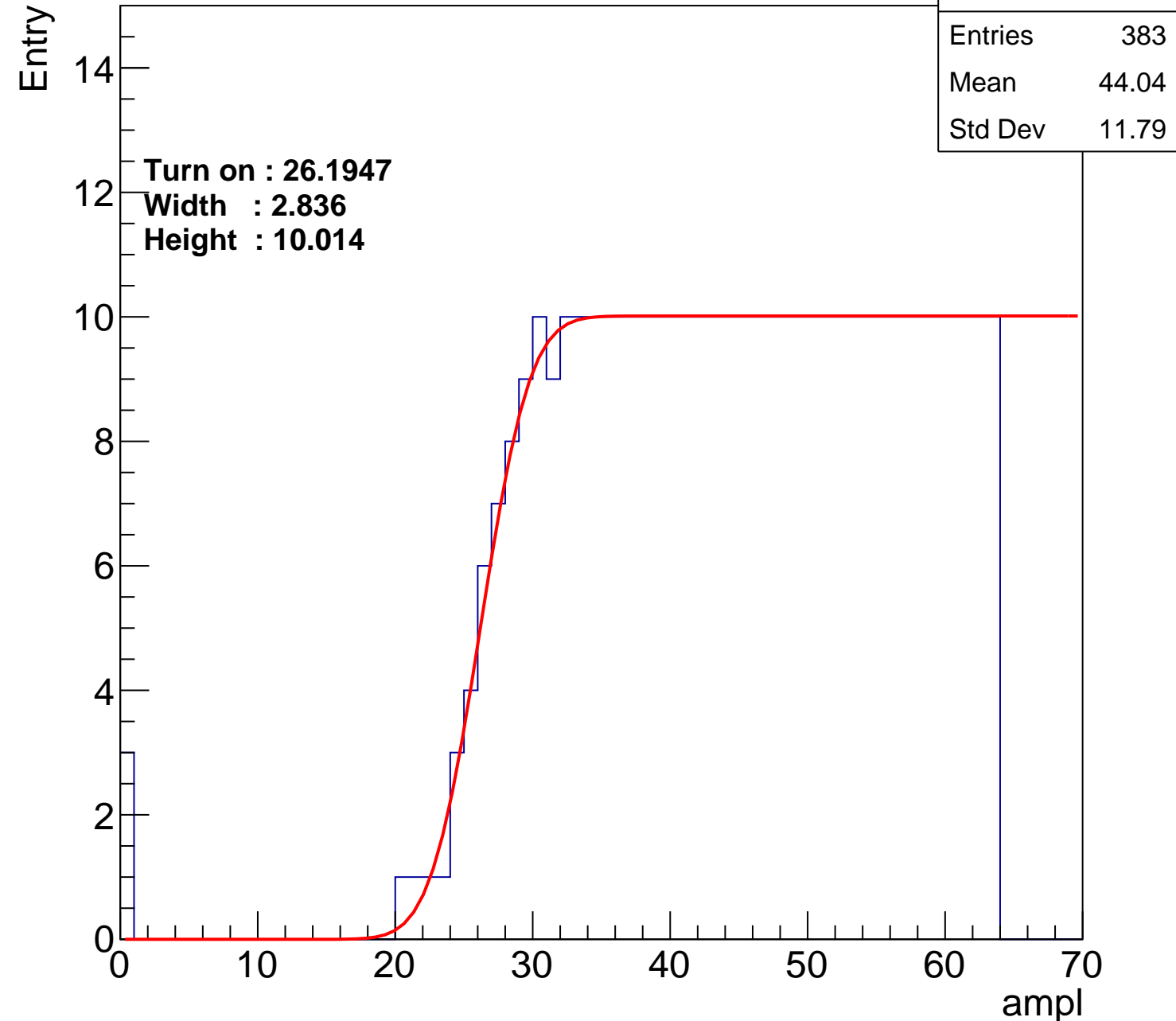
Width : 2.836

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch84

calib_packv5_042523_0143.root, FC#11, port A2

Entries	383
Mean	44.01
Std Dev	11.84

Turn on : 26.6443

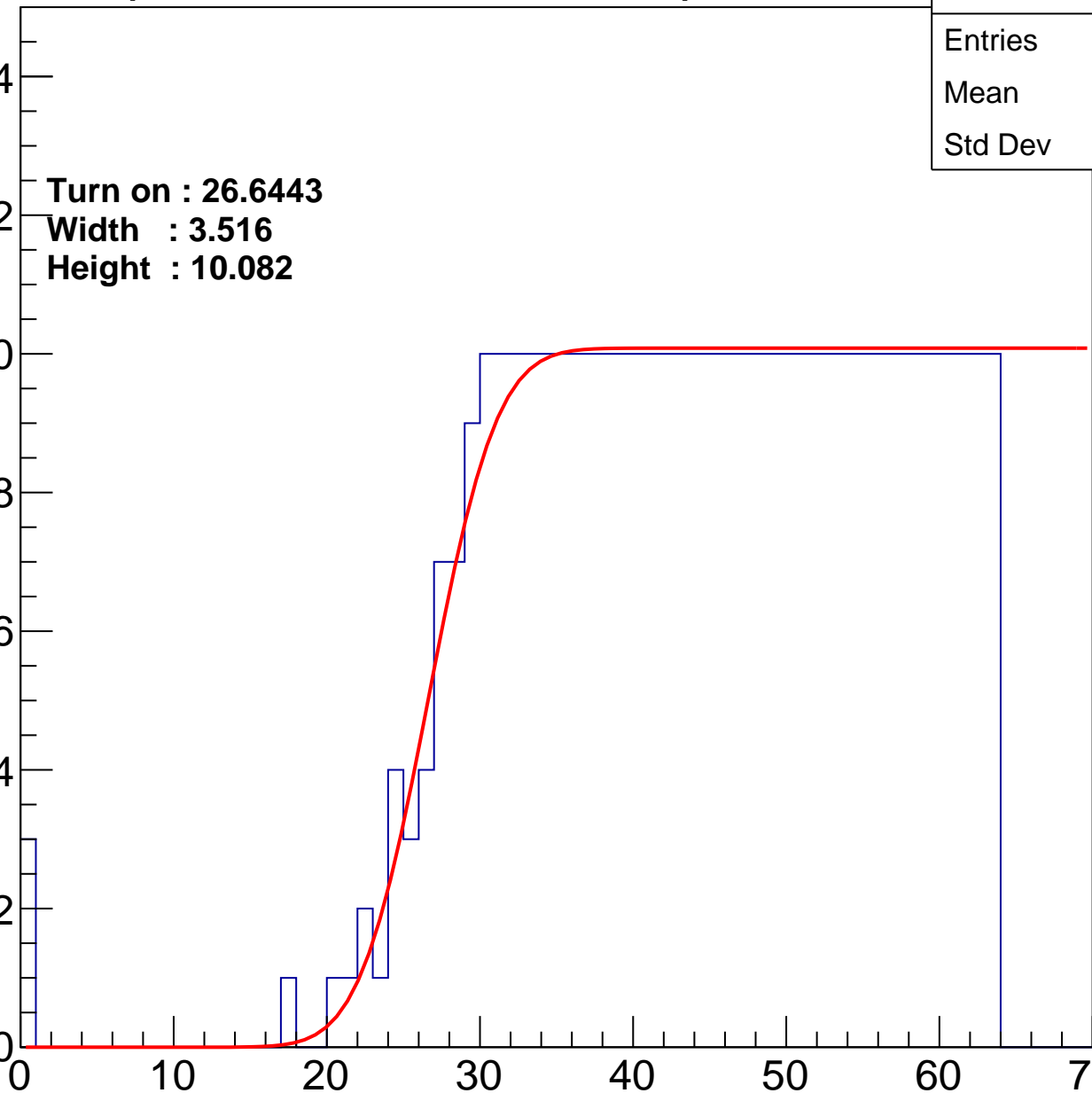
Width : 3.516

Height : 10.082

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch85

calib_packv5_042523_0143.root, FC#11, port A2

Entries	382
Mean	43.96
Std Dev	12.04

Turn on : 26.7783

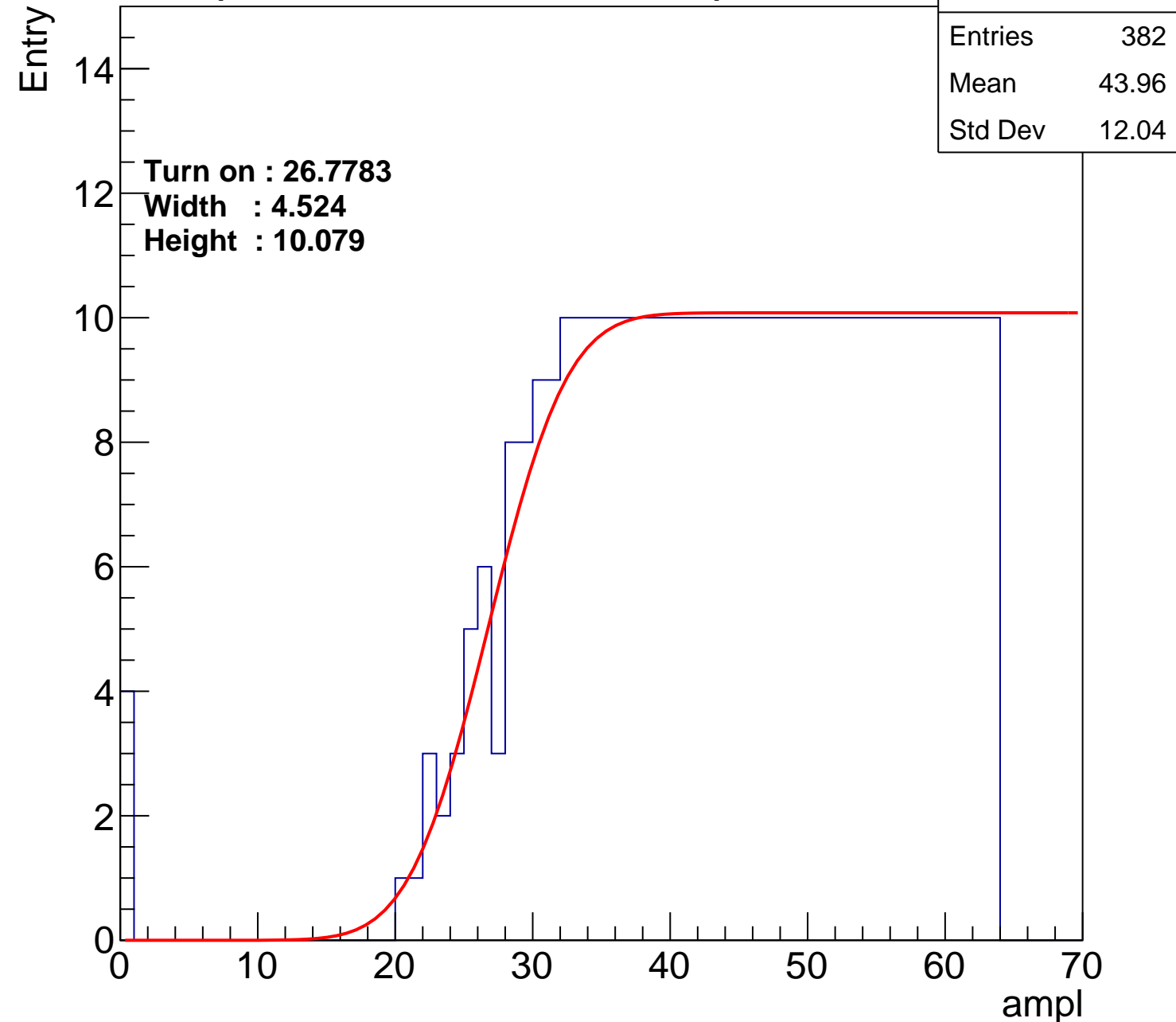
Width : 4.524

Height : 10.079

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch86

calib_packv5_042523_0143.root, FC#11, port A2

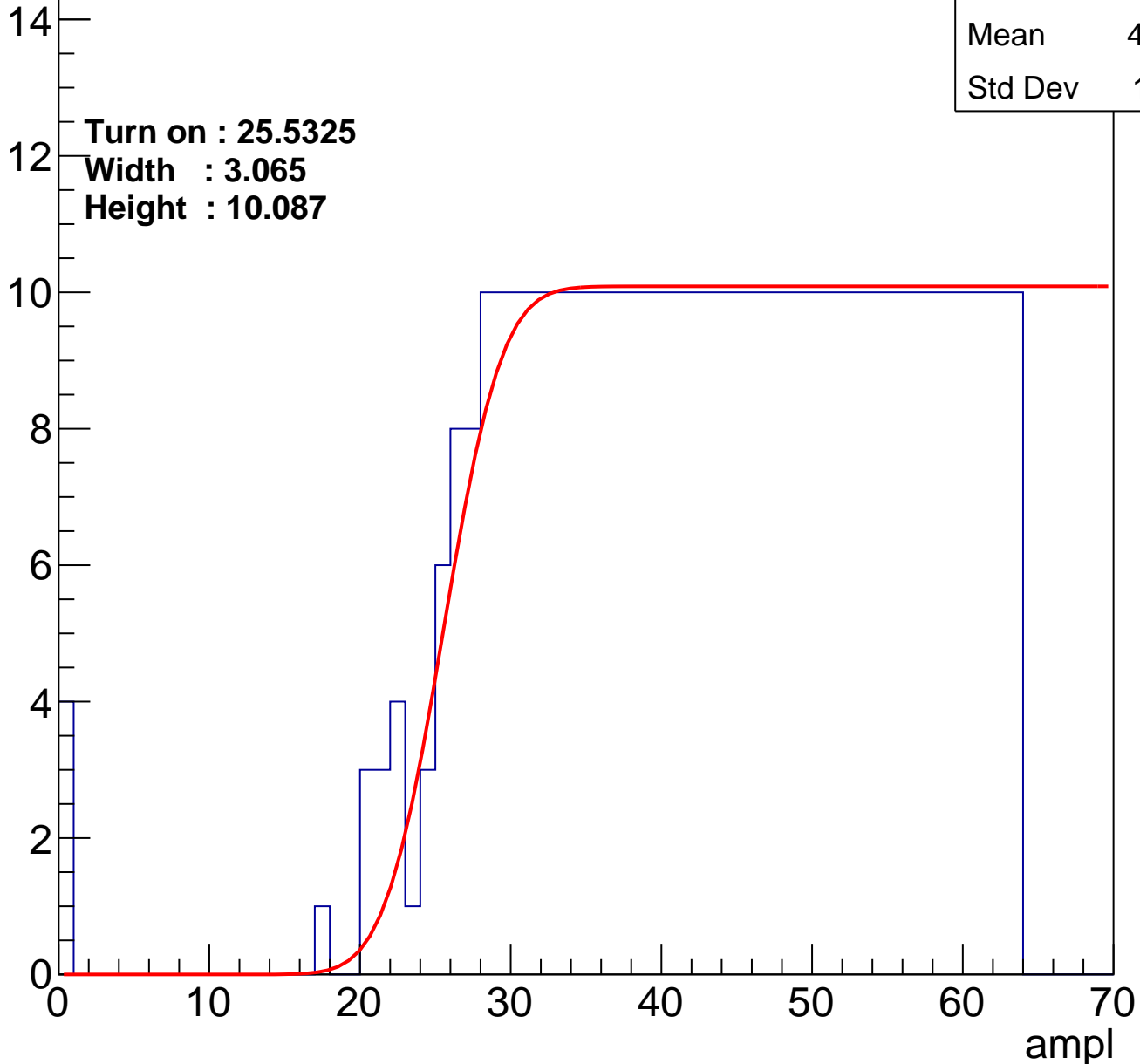
Entries	401
Mean	43.08
Std Dev	12.41

Turn on : 25.5325

Width : 3.065

Height : 10.087

Entry



B1L102S, U5-ch87

calib_packv5_042523_0143.root, FC#11, port A2

Entries	393
Mean	43.83
Std Dev	11.72

Turn on : 25.0985

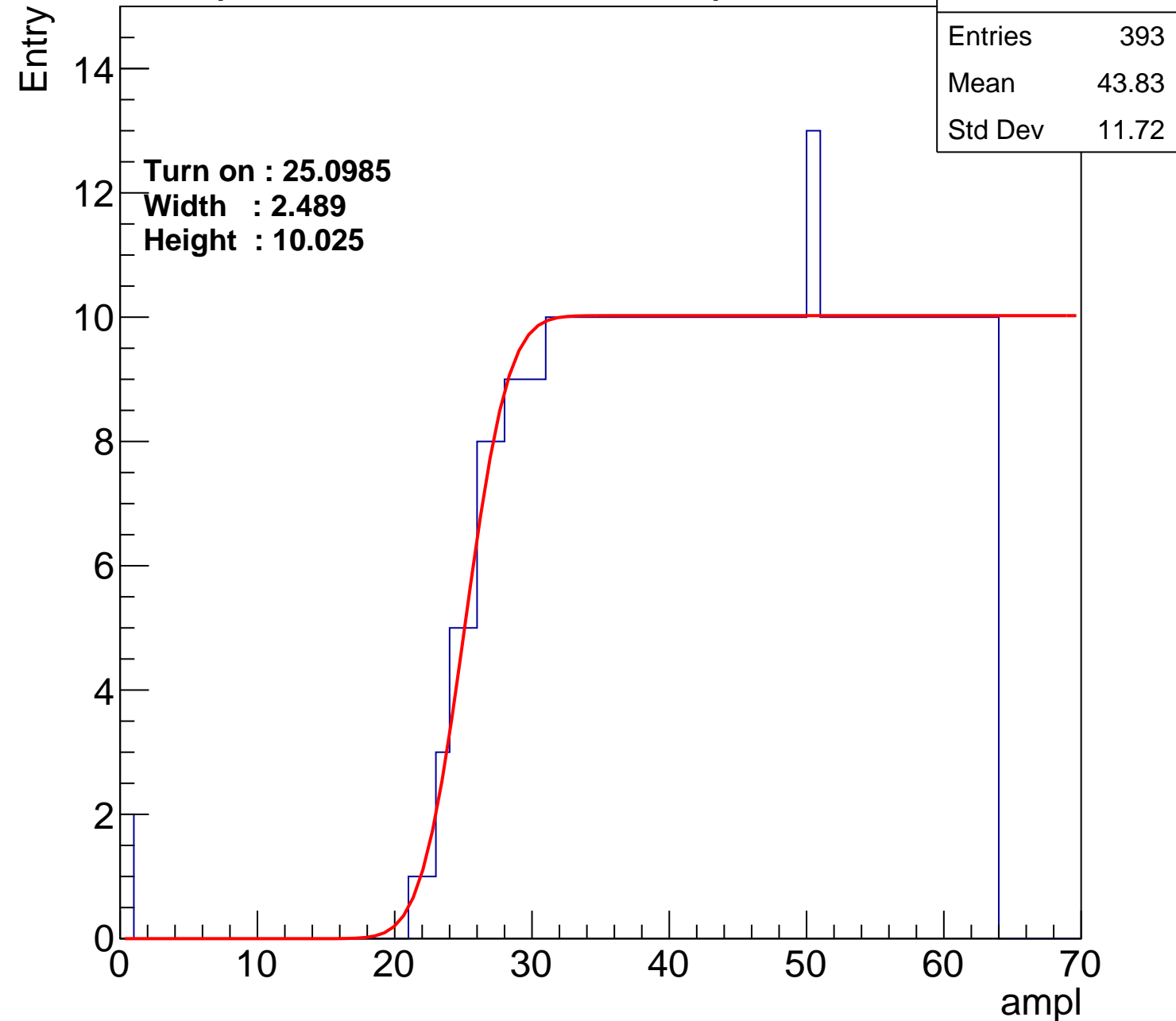
Width : 2.489

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch88

calib_packv5_042523_0143.root, FC#11, port A2

Entries	399
Mean	43.02
Std Dev	12.7

Turn on : 24.4635

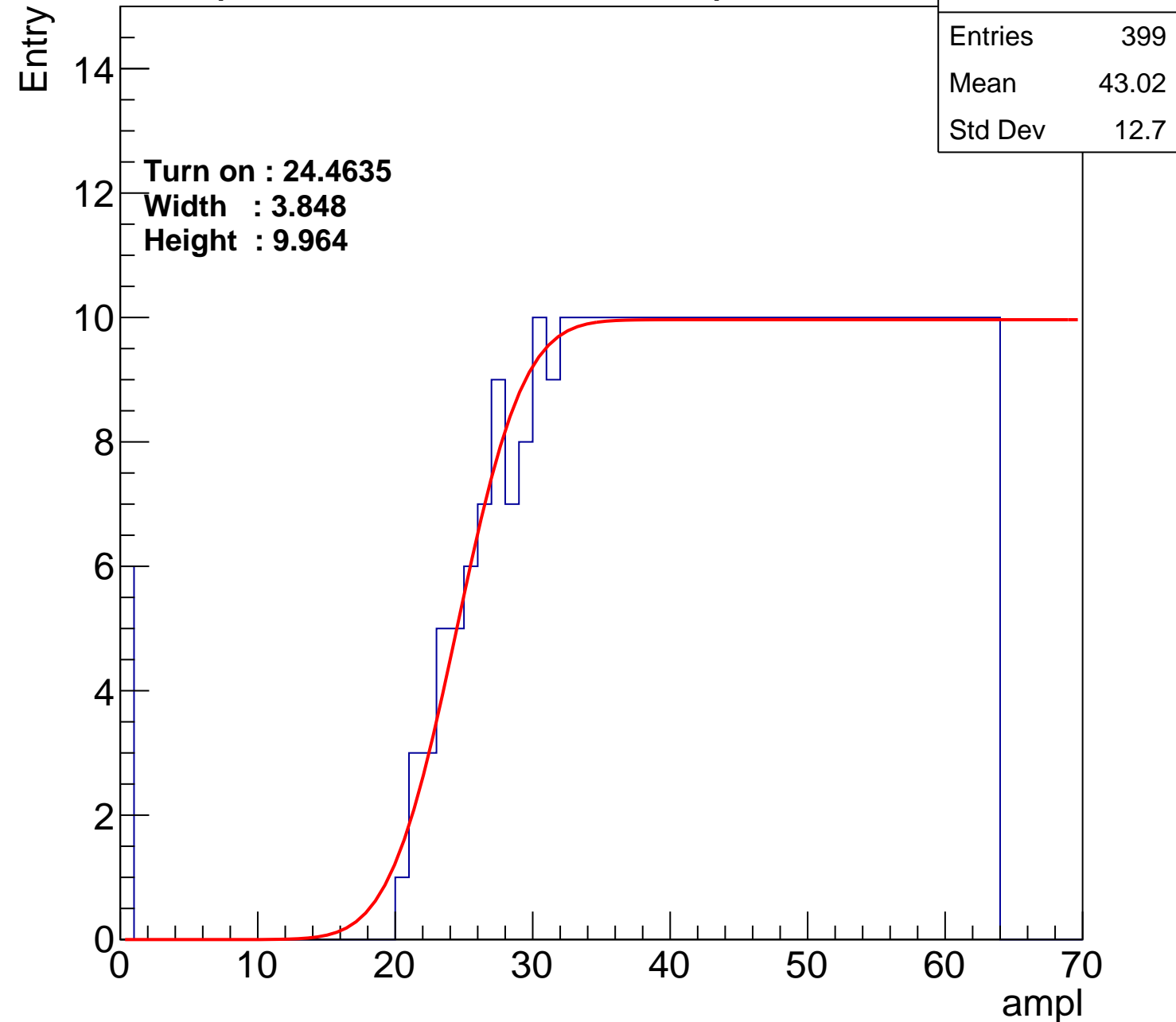
Width : 3.848

Height : 9.964

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch89

calib_packv5_042523_0143.root, FC#11, port A2

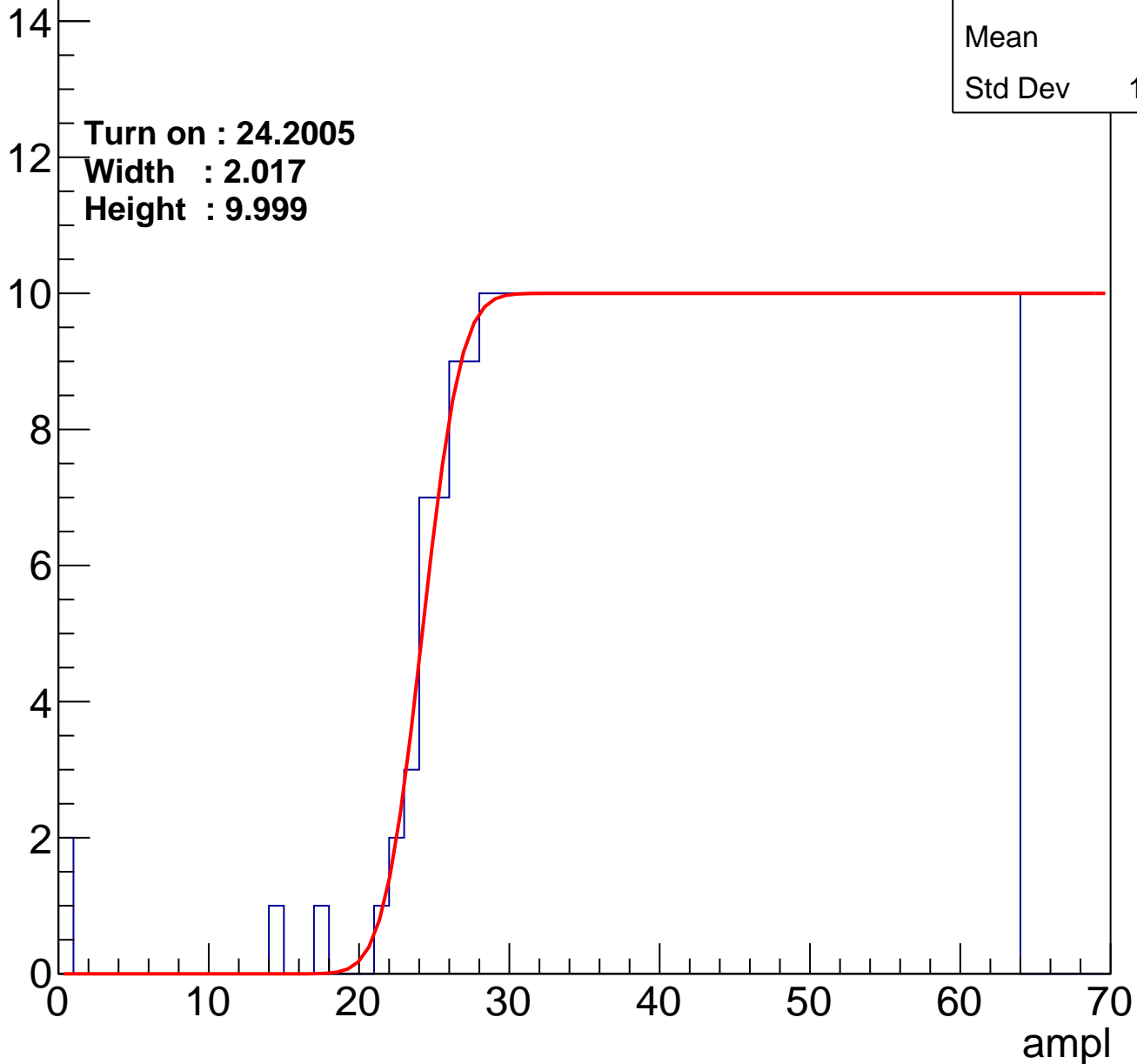
Entries	402
Mean	43.2
Std Dev	12.07

Turn on : 24.2005

Width : 2.017

Height : 9.999

Entry



B1L102S, U5-ch90

calib_packv5_042523_0143.root, FC#11, port A2

Entries	390
Mean	43.71
Std Dev	11.93

Turn on : 25.3864

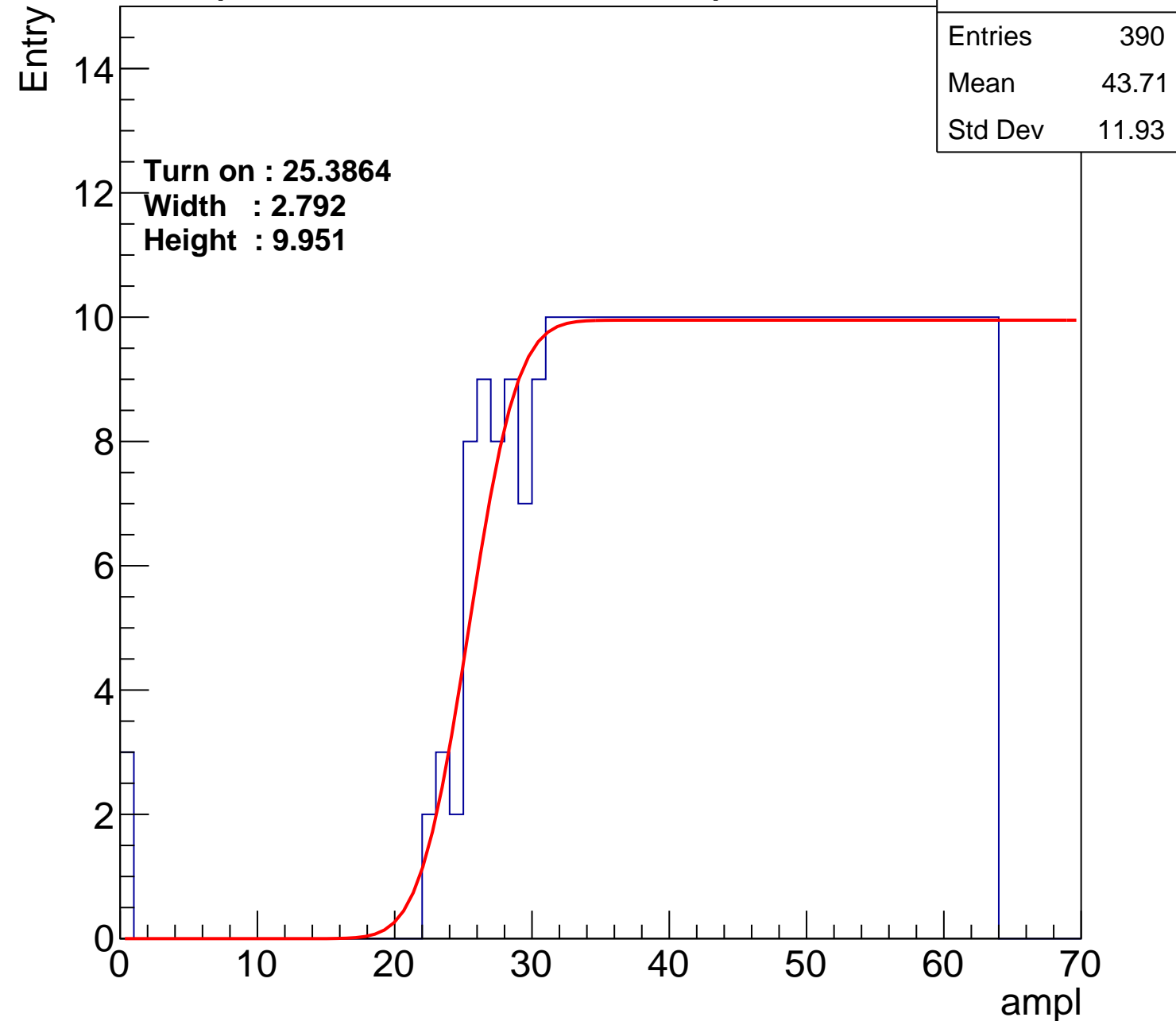
Width : 2.792

Height : 9.951

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch91

calib_packv5_042523_0143.root, FC#11, port A2

Entries	394
Mean	43.43
Std Dev	12.22

Turn on : 24.8811

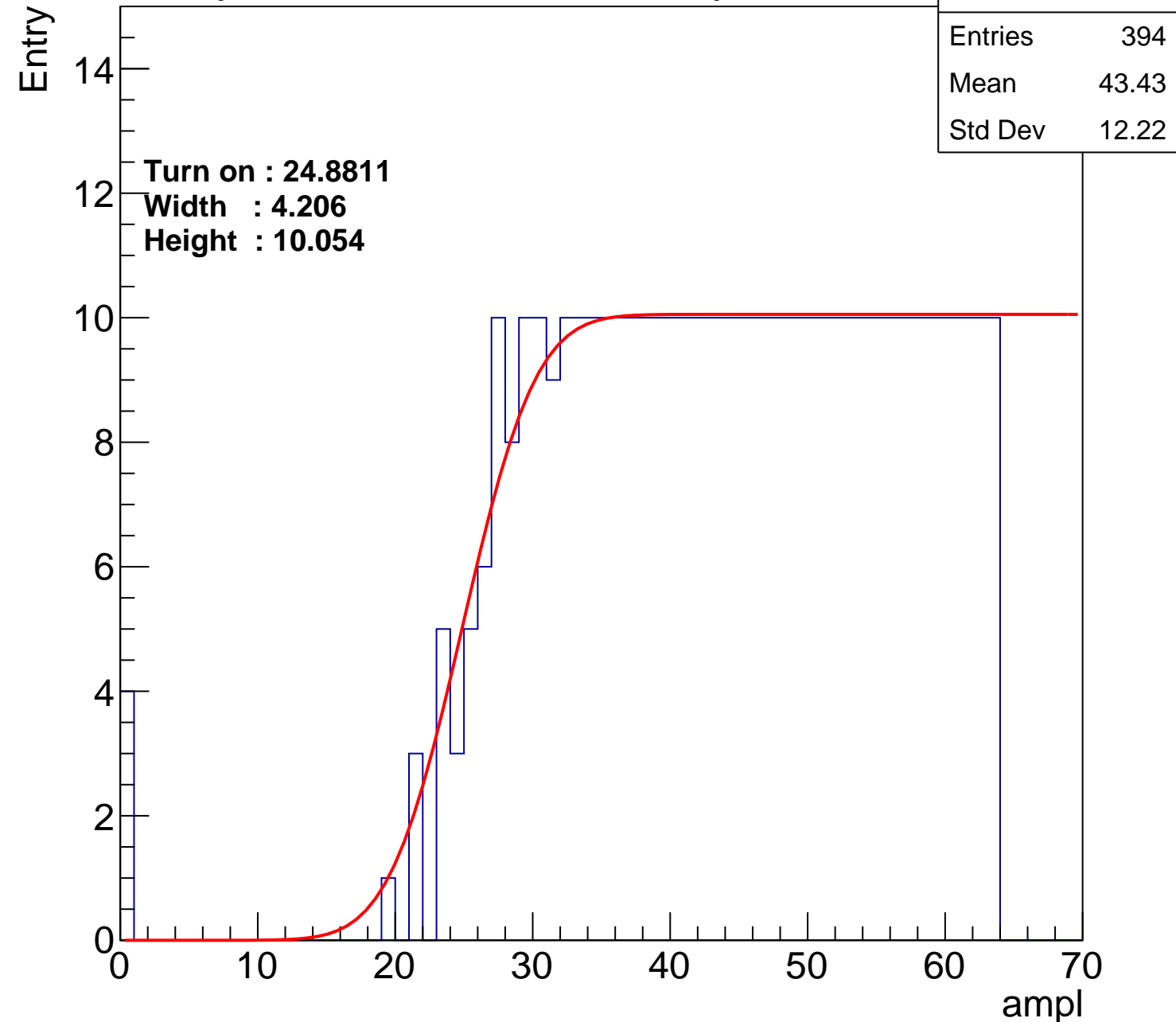
Width : 4.206

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch92

calib_packv5_042523_0143.root, FC#11, port A2

Entries	394
Mean	43.59
Std Dev	11.84

Turn on : 24.9850

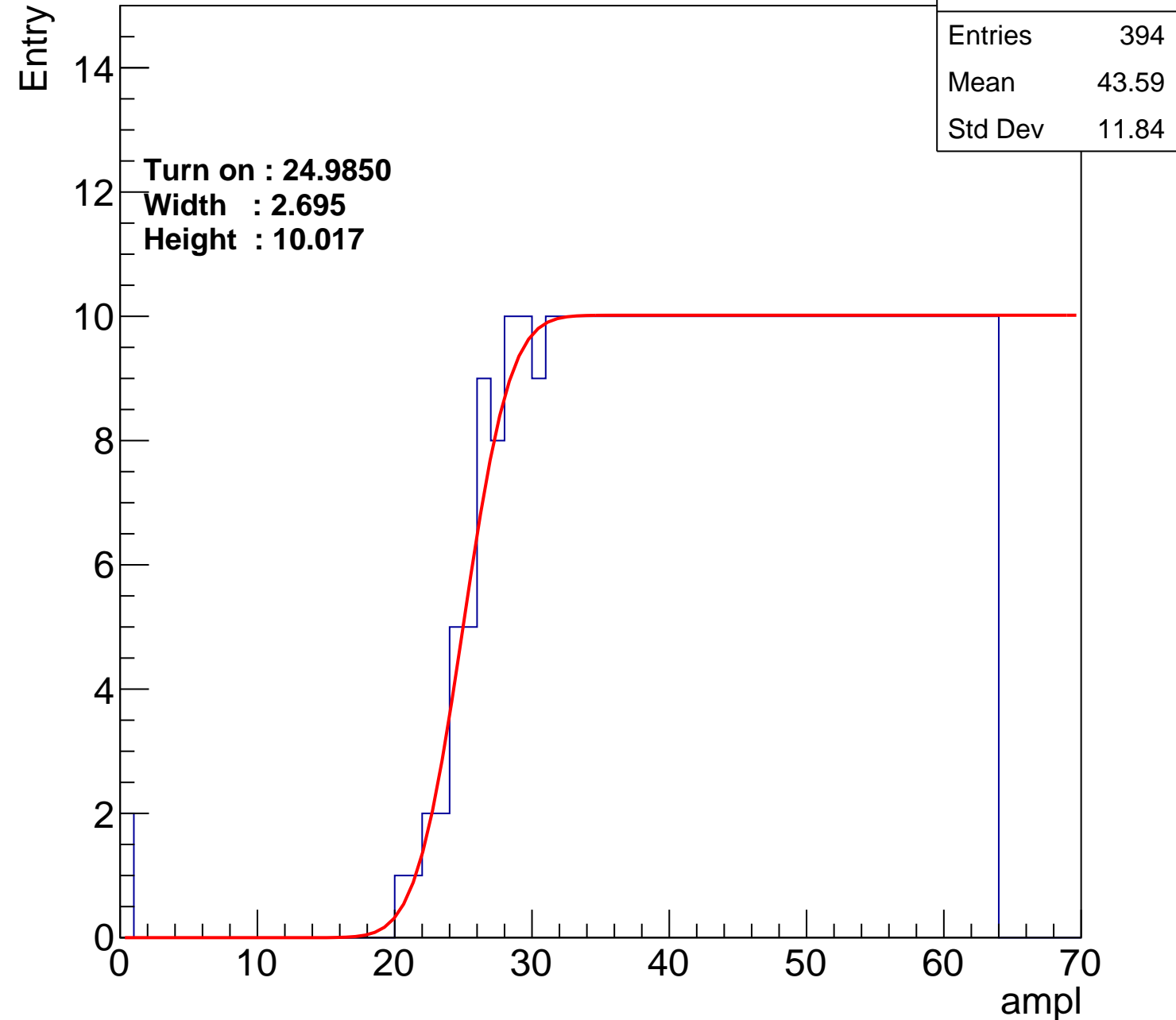
Width : 2.695

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch93

calib_packv5_042523_0143.root, FC#11, port A2

Entries	378
Mean	44.2
Std Dev	11.86

Turn on : 27.1049

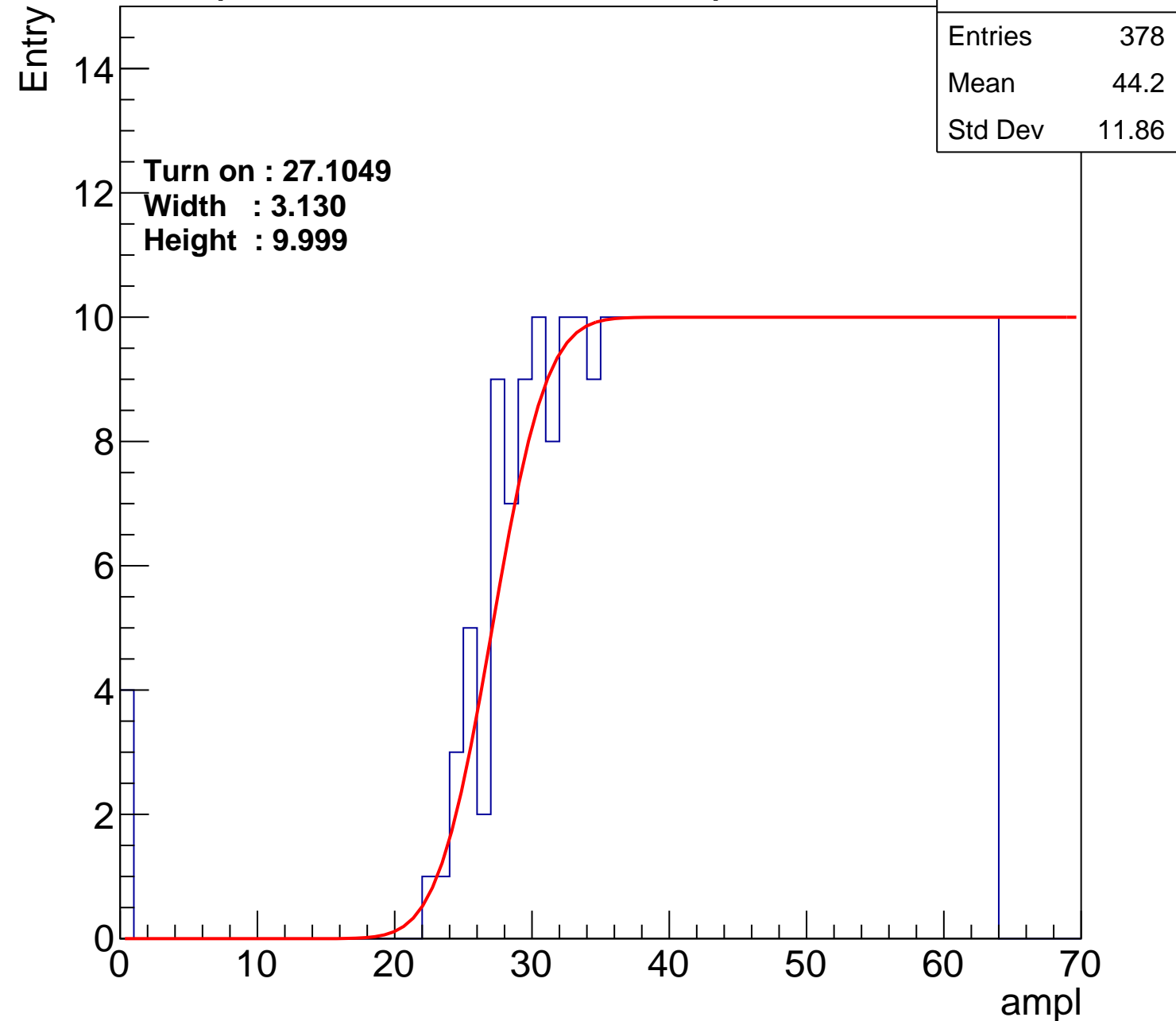
Width : 3.130

Height : 9.999

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch94

calib_packv5_042523_0143.root, FC#11, port A2

Entries	373
Mean	44.63
Std Dev	11.21

Turn on : 26.8735

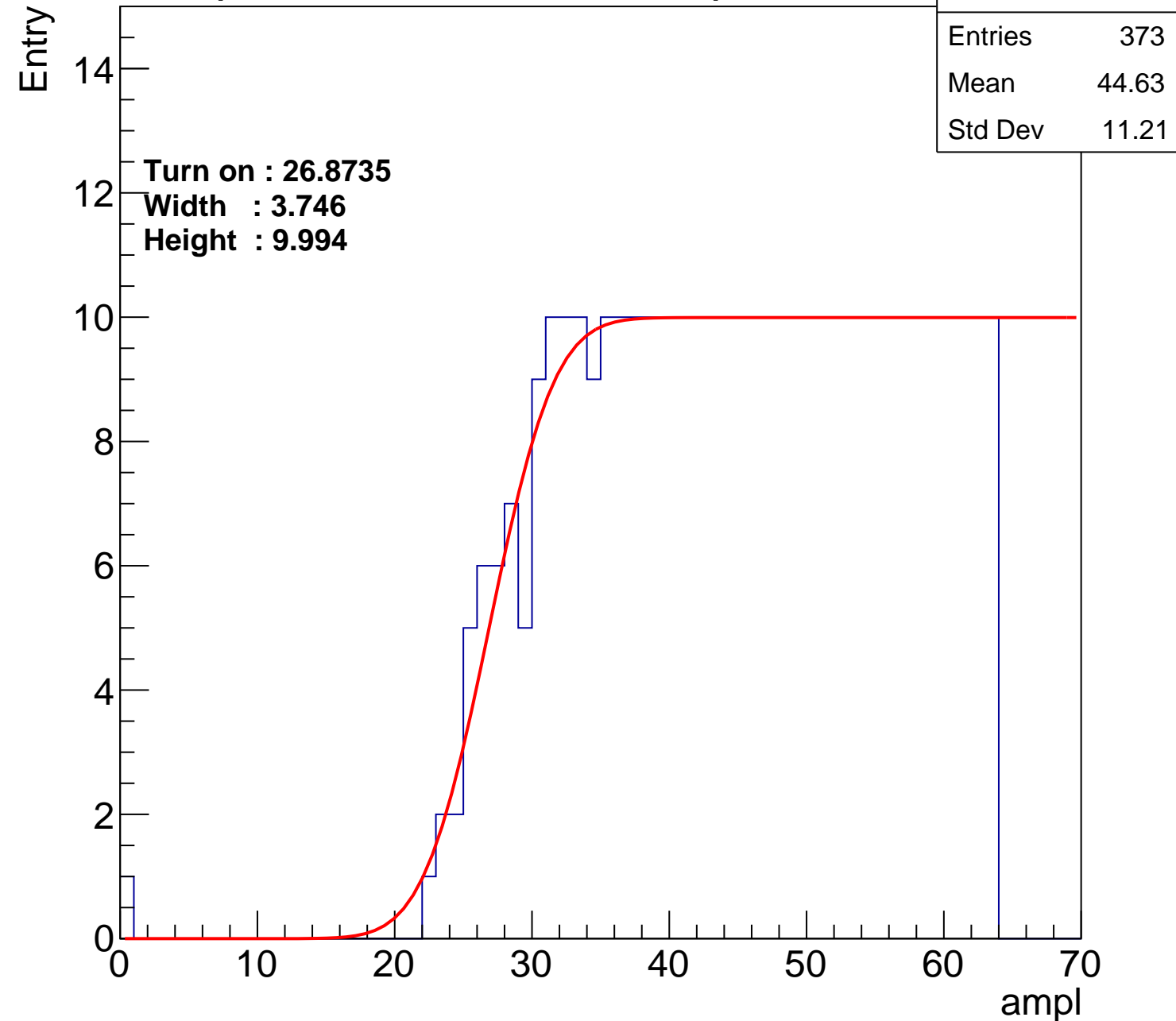
Width : 3.746

Height : 9.994

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch95

calib_packv5_042523_0143.root, FC#11, port A2

Entries	396
Mean	43.44
Std Dev	11.99

Turn on : 24.8655

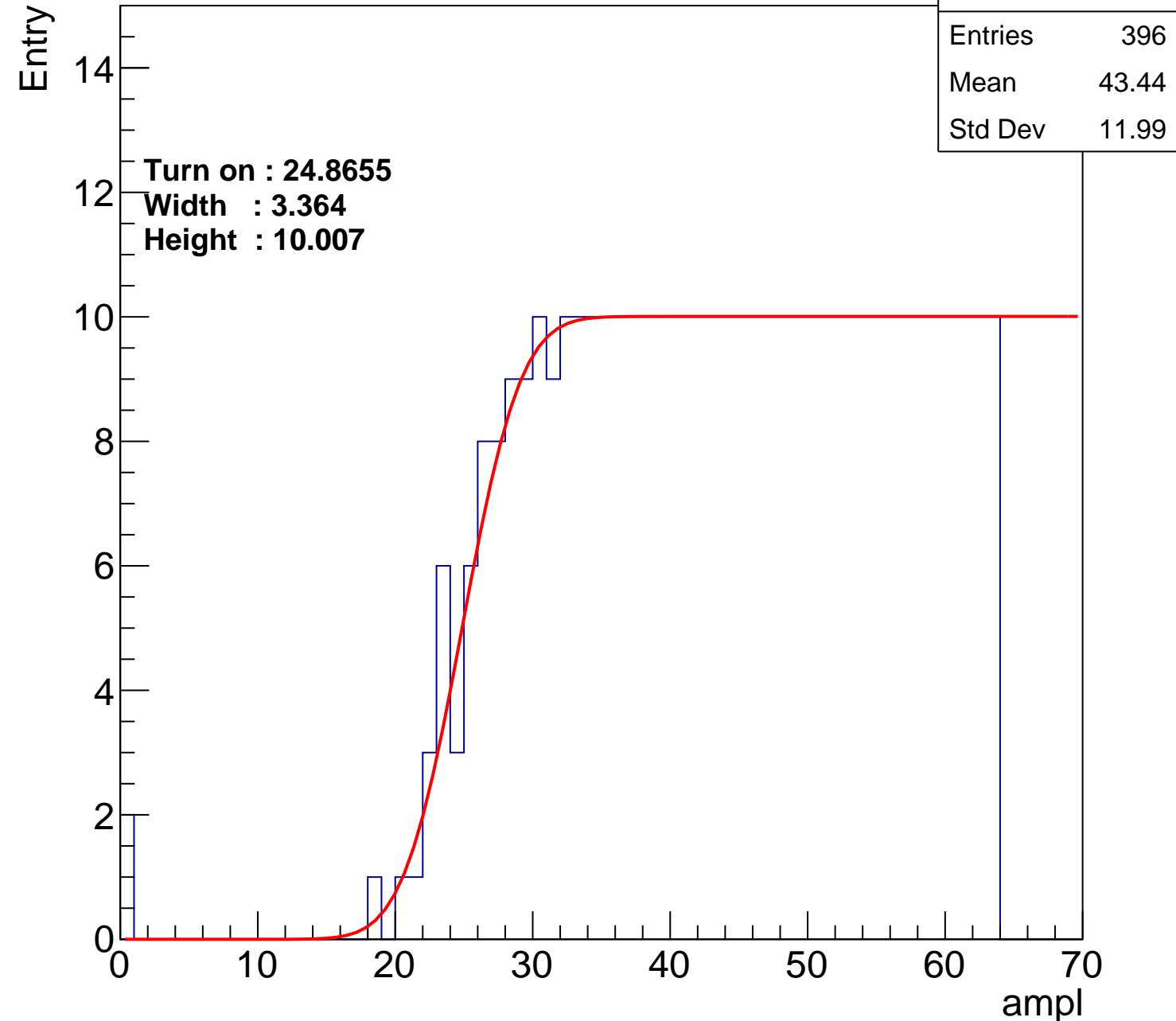
Width : 3.364

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch96

calib_packv5_042523_0143.root, FC#11, port A2

Entries	398
Mean	43.23
Std Dev	12.33

Turn on : 24.8882

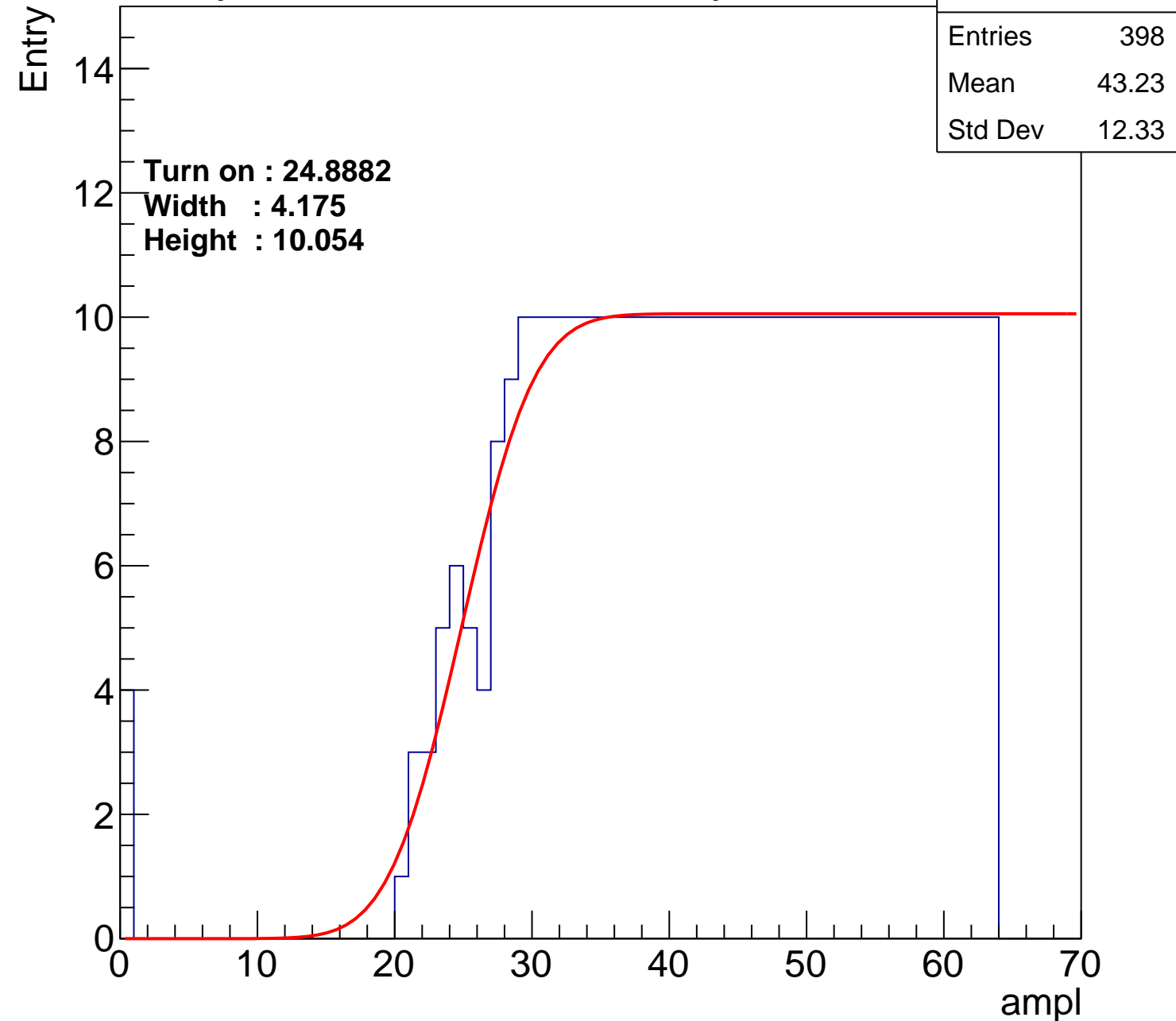
Width : 4.175

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch97

calib_packv5_042523_0143.root, FC#11, port A2

Entries	396
Mean	43.37
Std Dev	12.15

Turn on : 24.8642

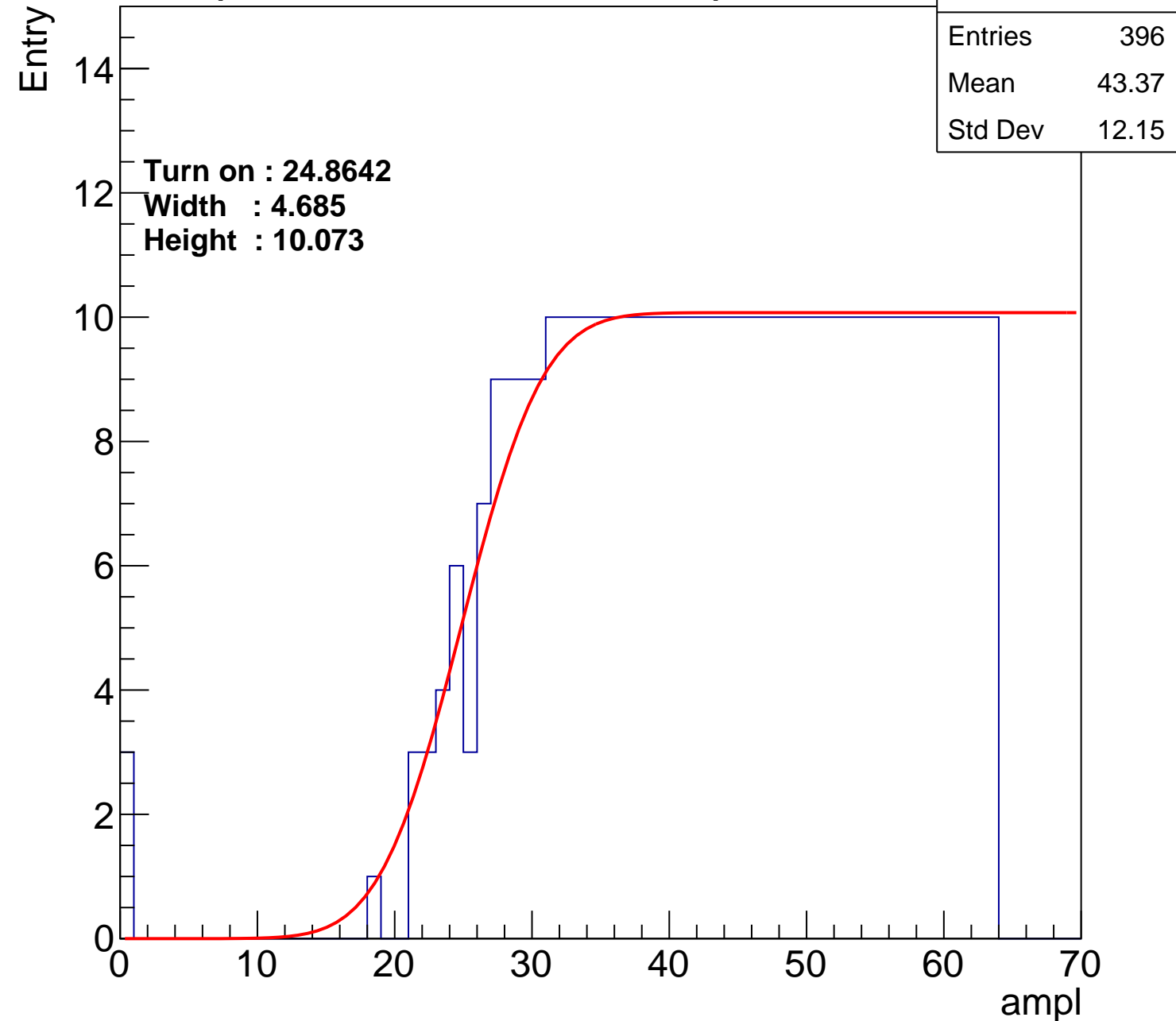
Width : 4.685

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch98

calib_packv5_042523_0143.root, FC#11, port A2

Entries	399
Mean	43.37
Std Dev	11.87

Turn on : 24.8463

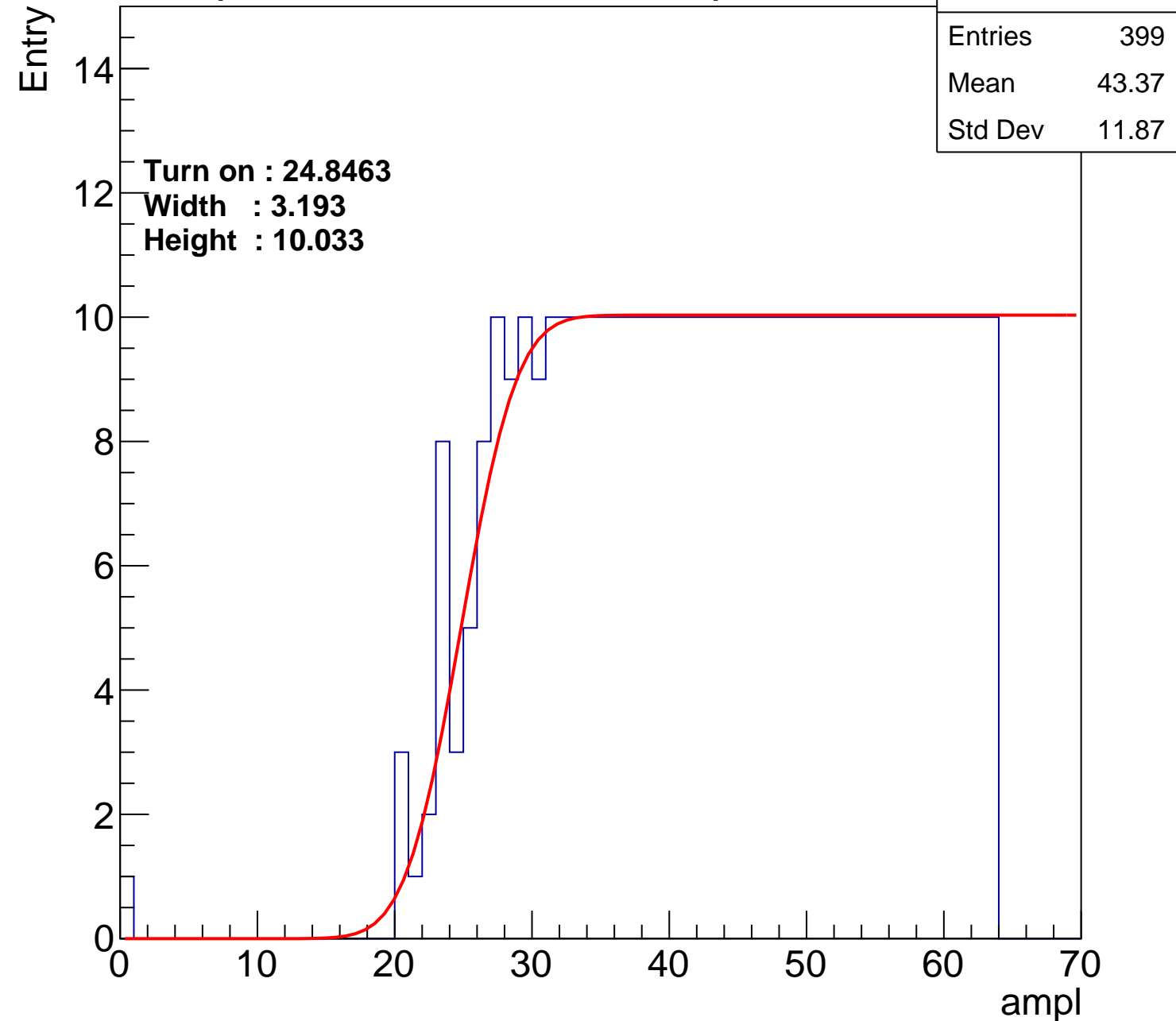
Width : 3.193

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch99

calib_packv5_042523_0143.root, FC#11, port A2

Entries	392
Mean	43.51
Std Dev	12.2

Turn on : 24.5093

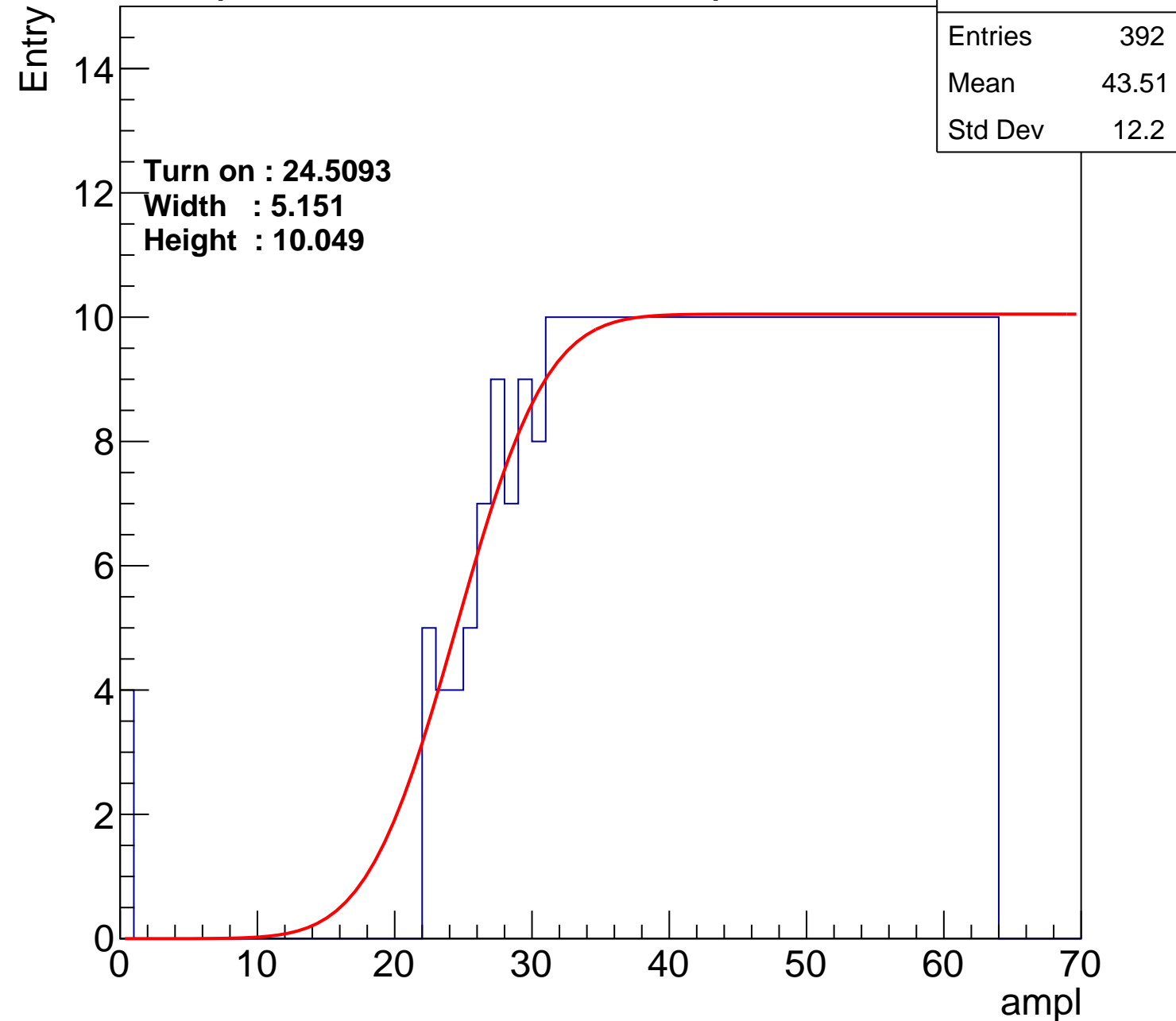
Width : 5.151

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch100

calib_packv5_042523_0143.root, FC#11, port A2

Entries	395
Mean	43.55
Std Dev	11.8

Turn on : 25.1955

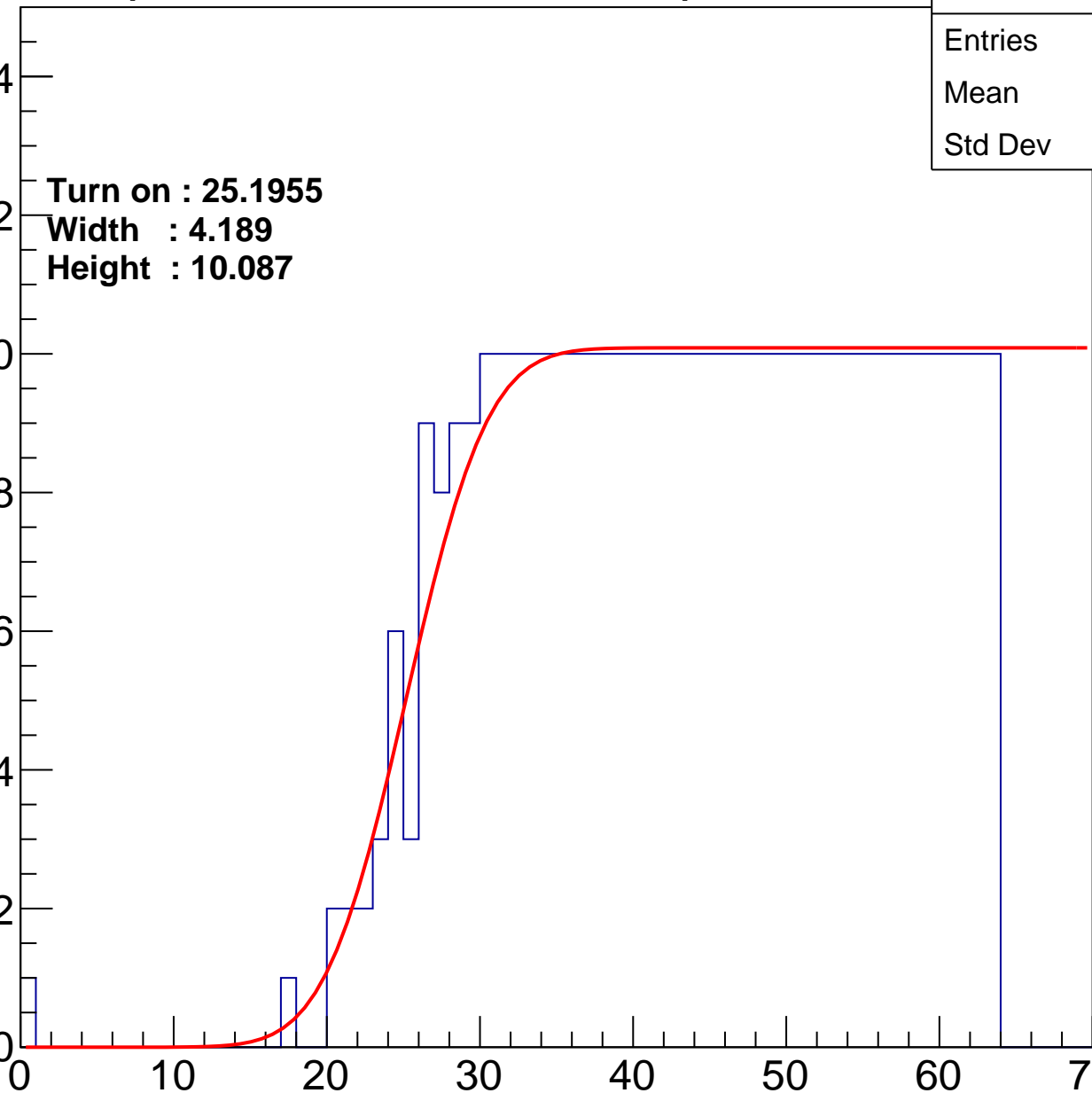
Width : 4.189

Height : 10.087

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch101

calib_packv5_042523_0143.root, FC#11, port A2

Entries	376
Mean	44.32
Std Dev	11.78

Turn on : 26.8162

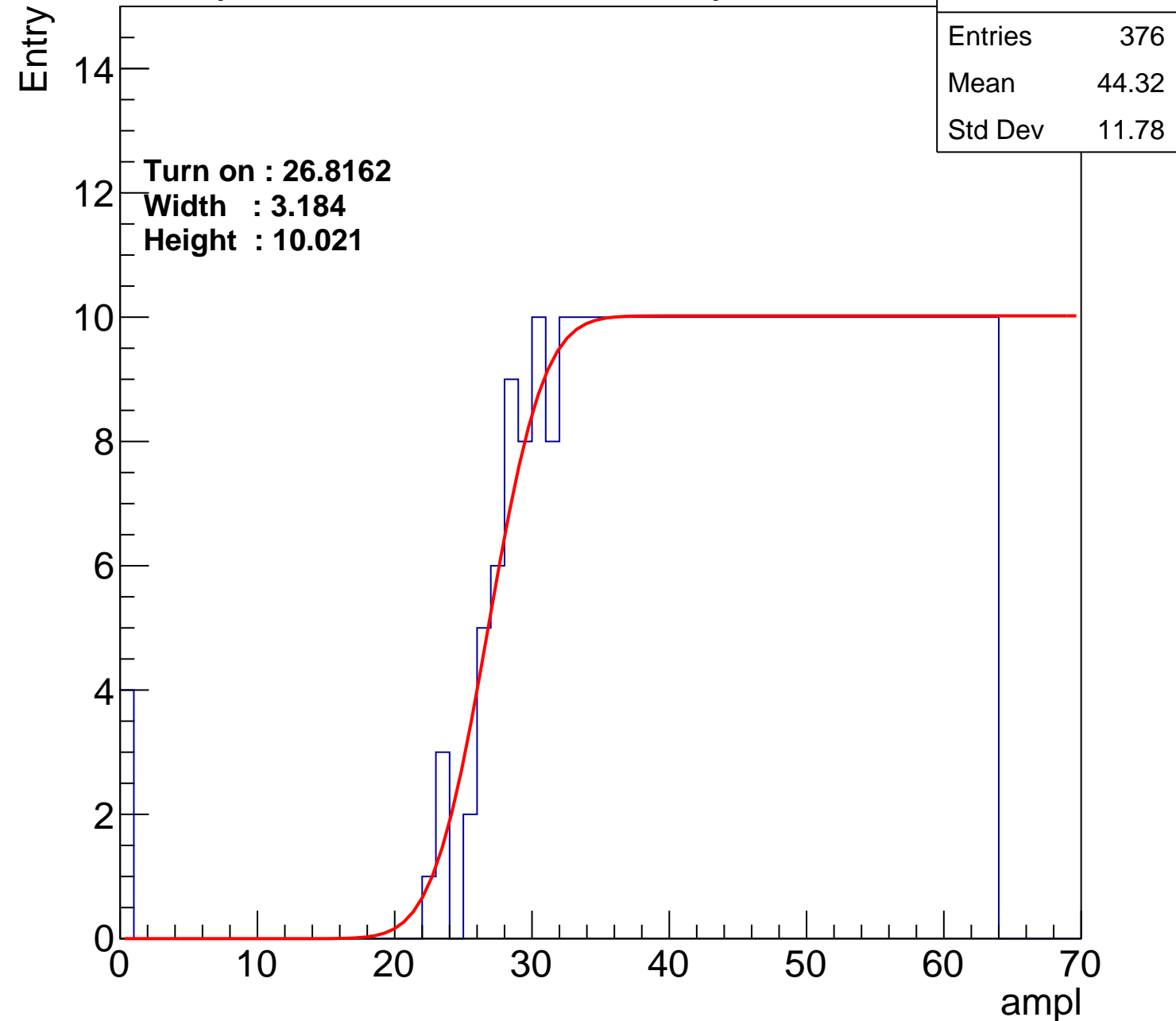
Width : 3.184

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch102

calib_packv5_042523_0143.root, FC#11, port A2

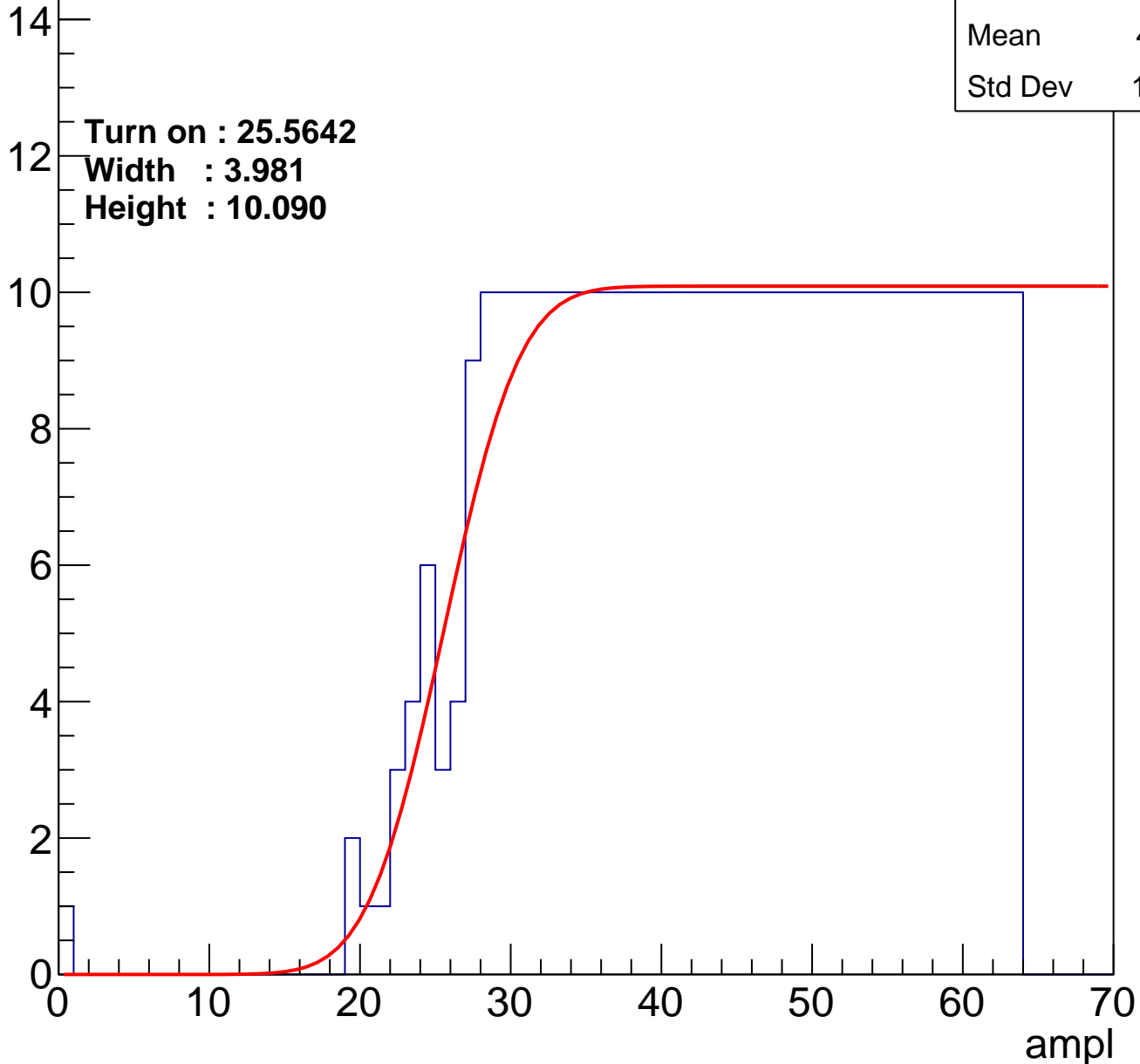
Entries	394
Mean	43.61
Std Dev	11.76

Turn on : 25.5642

Width : 3.981

Height : 10.090

Entry



B1L102S, U5-ch103

calib_packv5_042523_0143.root, FC#11, port A2

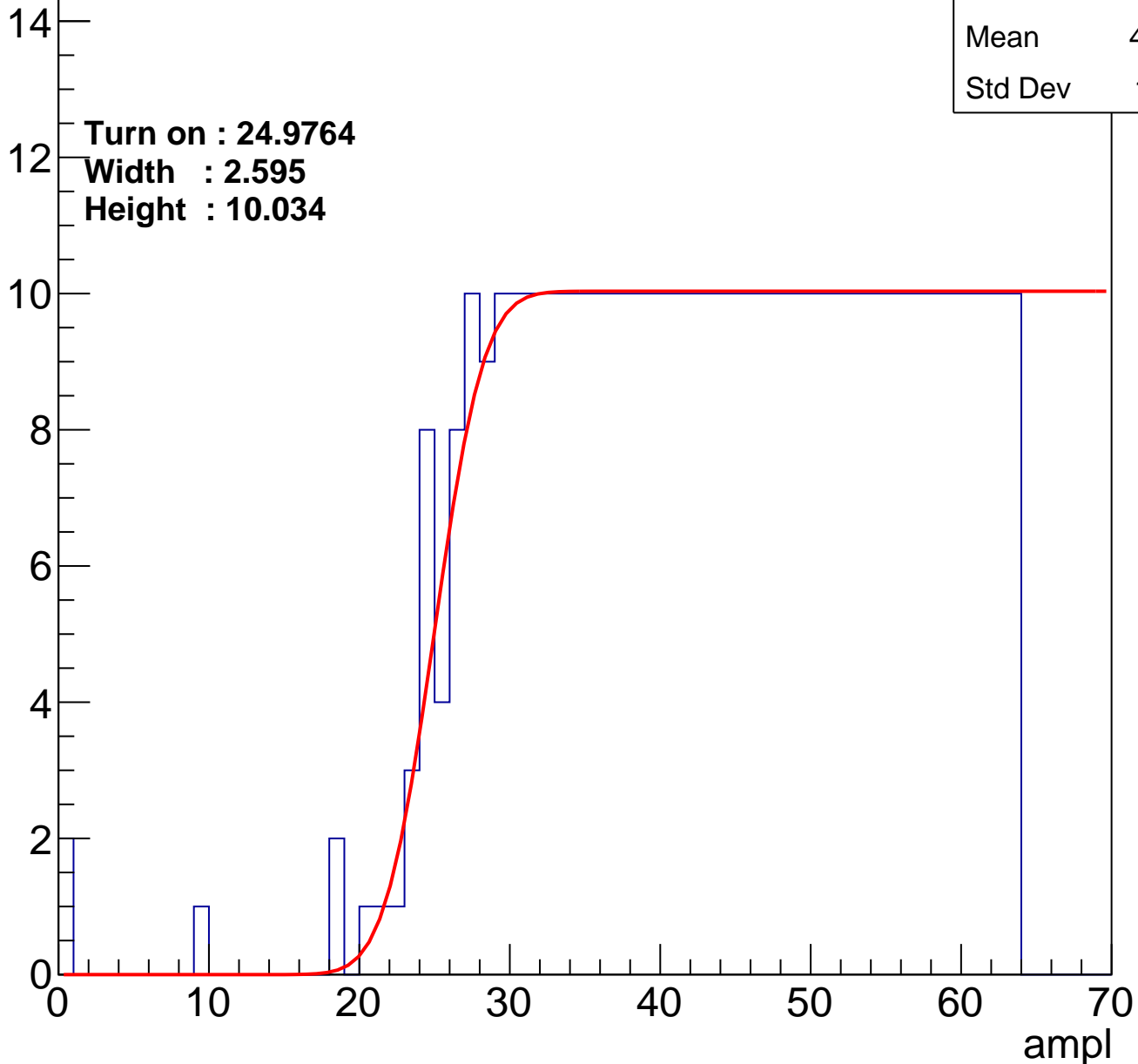
Entries	400
Mean	43.25
Std Dev	12.11

Turn on : 24.9764

Width : 2.595

Height : 10.034

Entry



B1L102S, U5-ch104

calib_packv5_042523_0143.root, FC#11, port A2

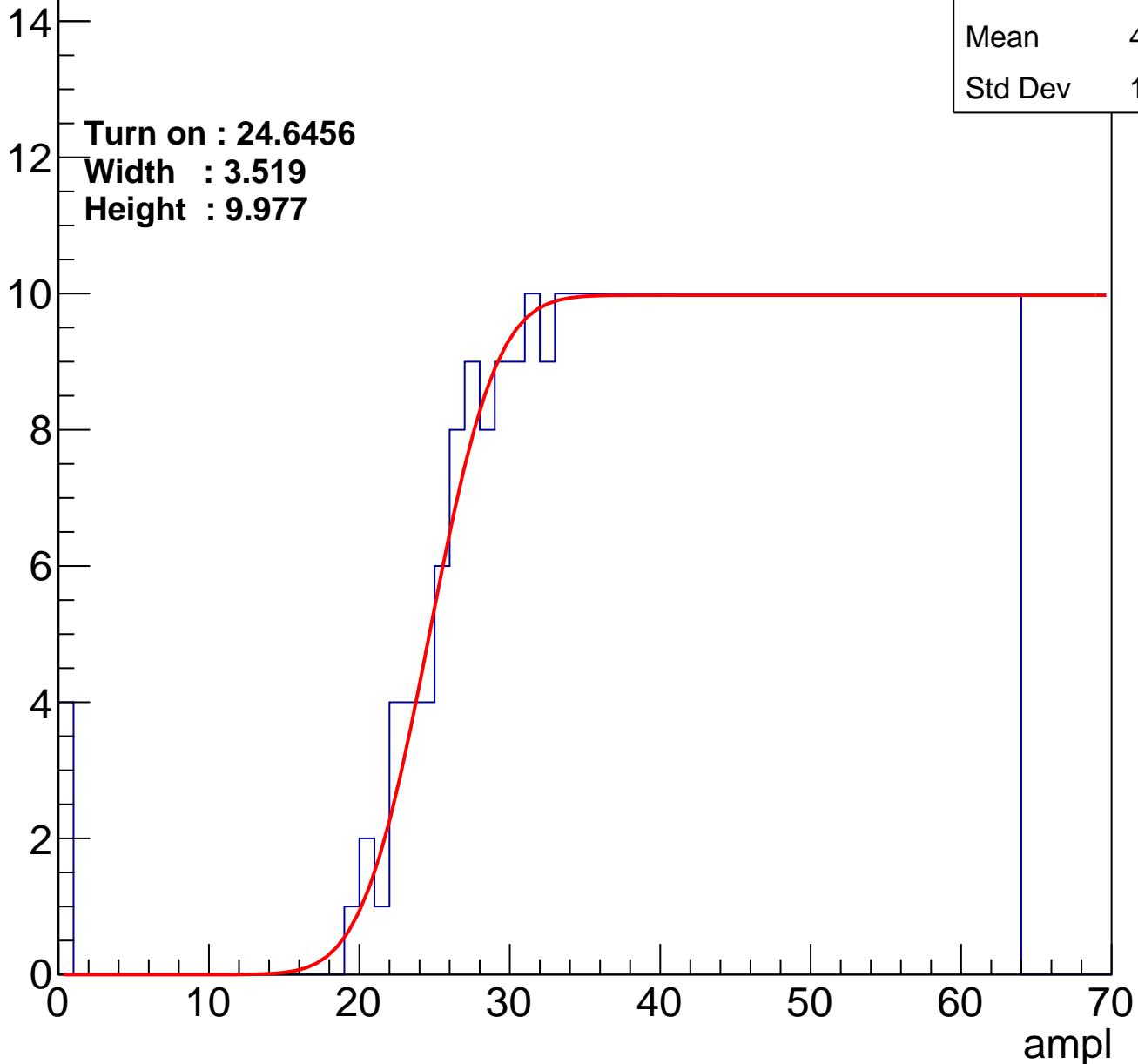
Entries	398
Mean	43.19
Std Dev	12.38

Turn on : 24.6456

Width : 3.519

Height : 9.977

Entry



B1L102S, U5-ch105

calib_packv5_042523_0143.root, FC#11, port A2

Entries	380
Mean	44.34
Std Dev	11.31

Turn on : 26.0580

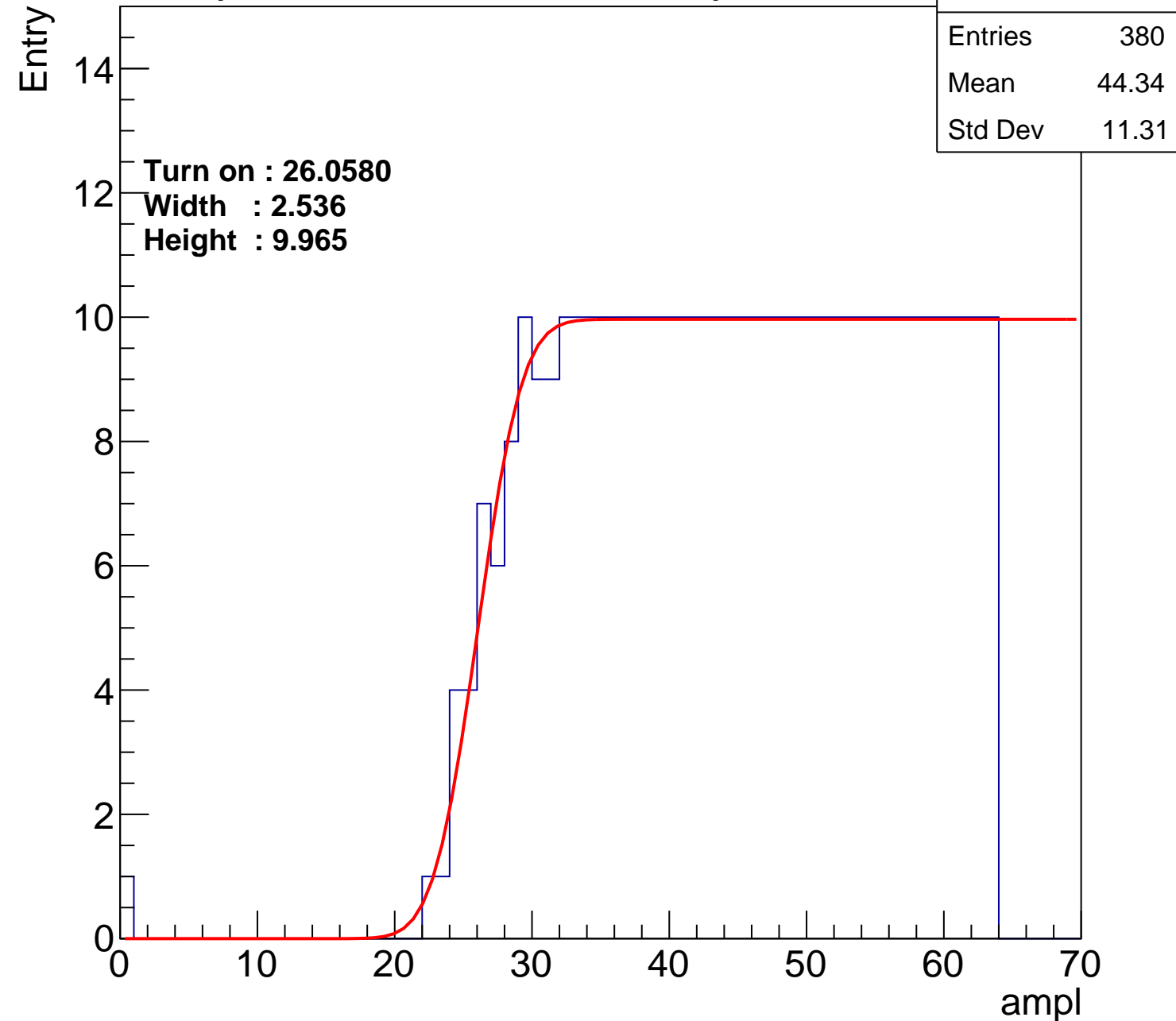
Width : 2.536

Height : 9.965

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch106

calib_packv5_042523_0143.root, FC#11, port A2

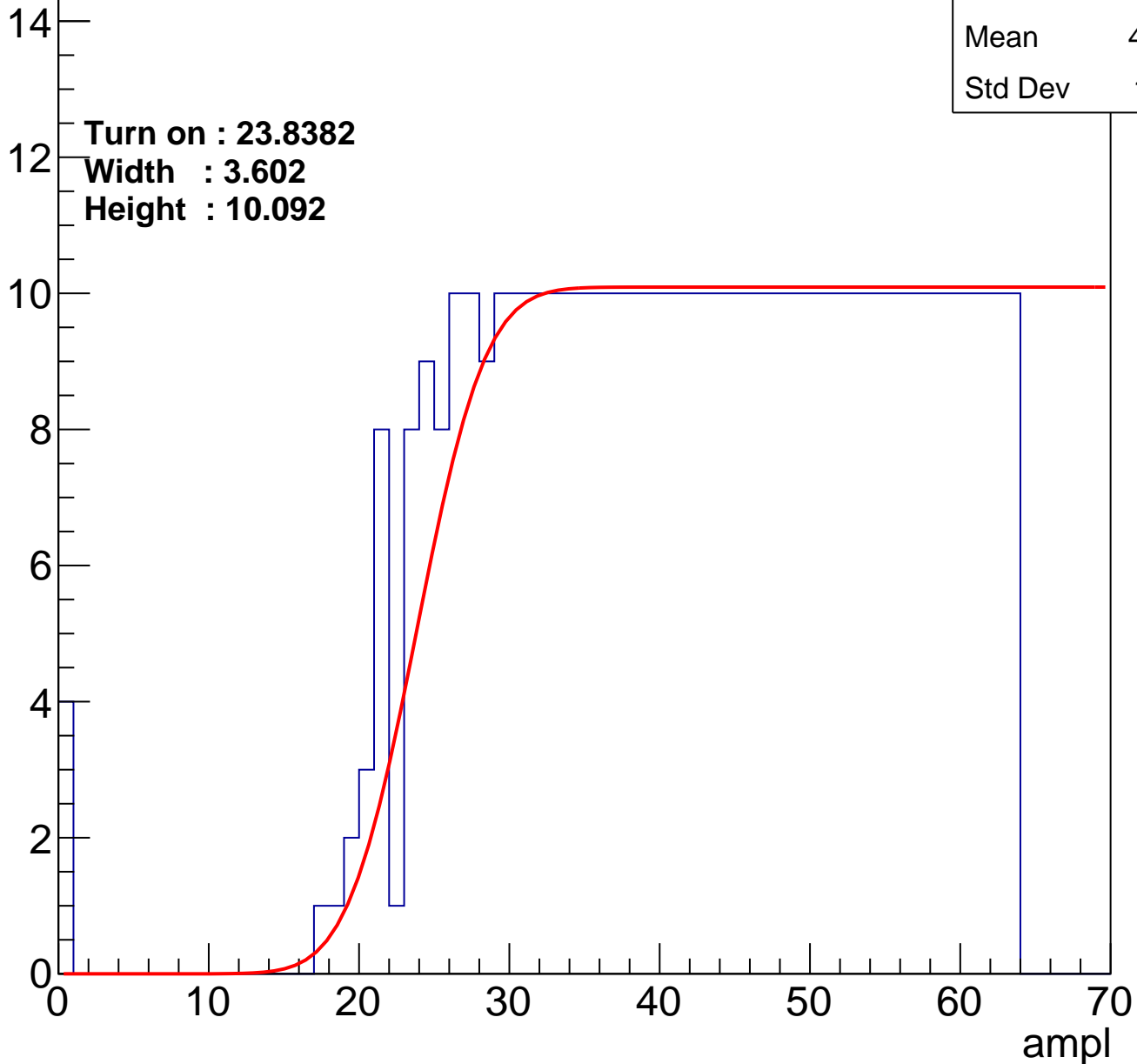
Entries	424
Mean	41.99
Std Dev	12.91

Turn on : 23.8382

Width : 3.602

Height : 10.092

Entry



B1L102S, U5-ch107

calib_packv5_042523_0143.root, FC#11, port A2

Entries	387
Mean	43.78
Std Dev	12.04

Turn on : 25.5945

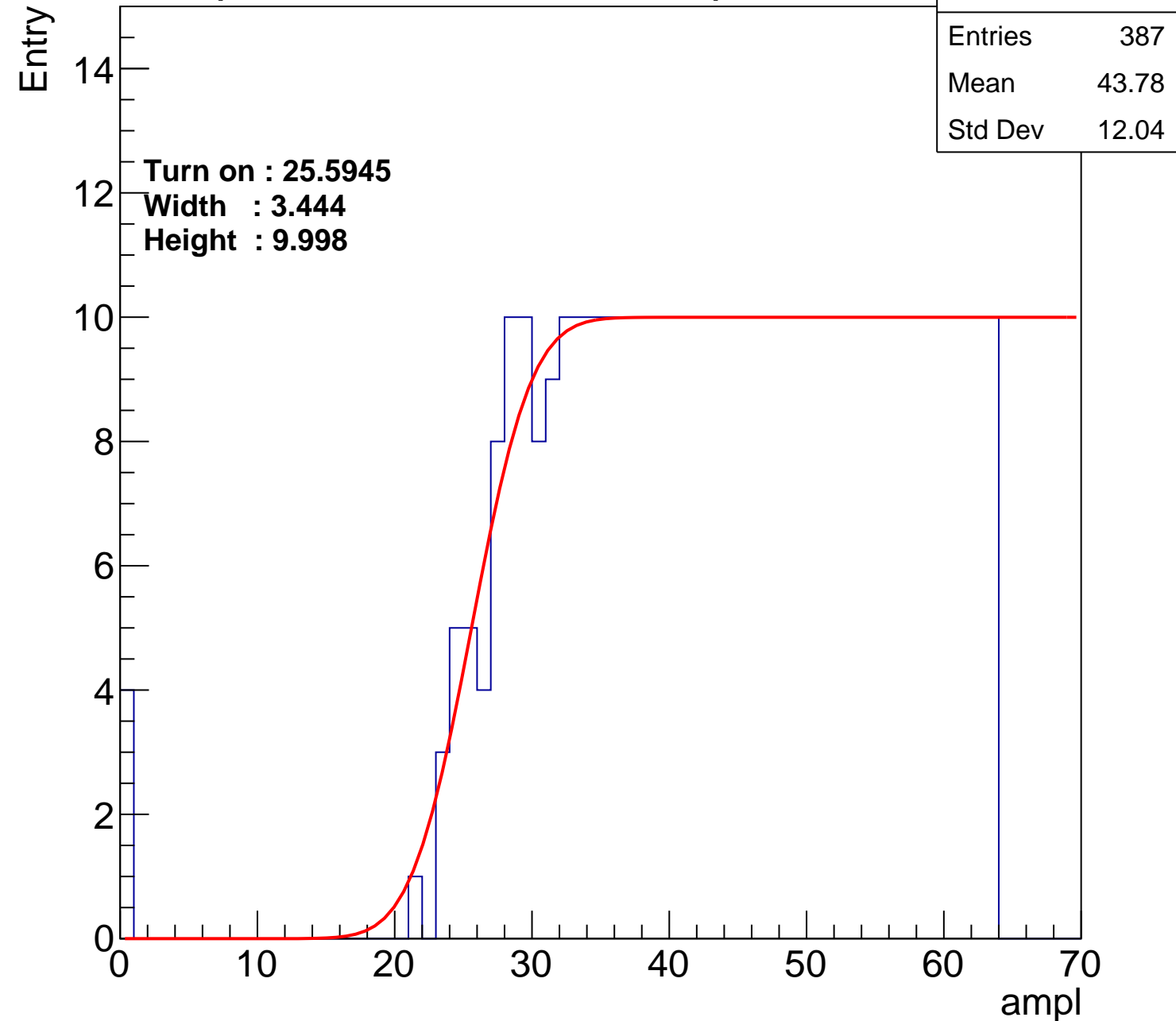
Width : 3.444

Height : 9.998

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch108

calib_packv5_042523_0143.root, FC#11, port A2

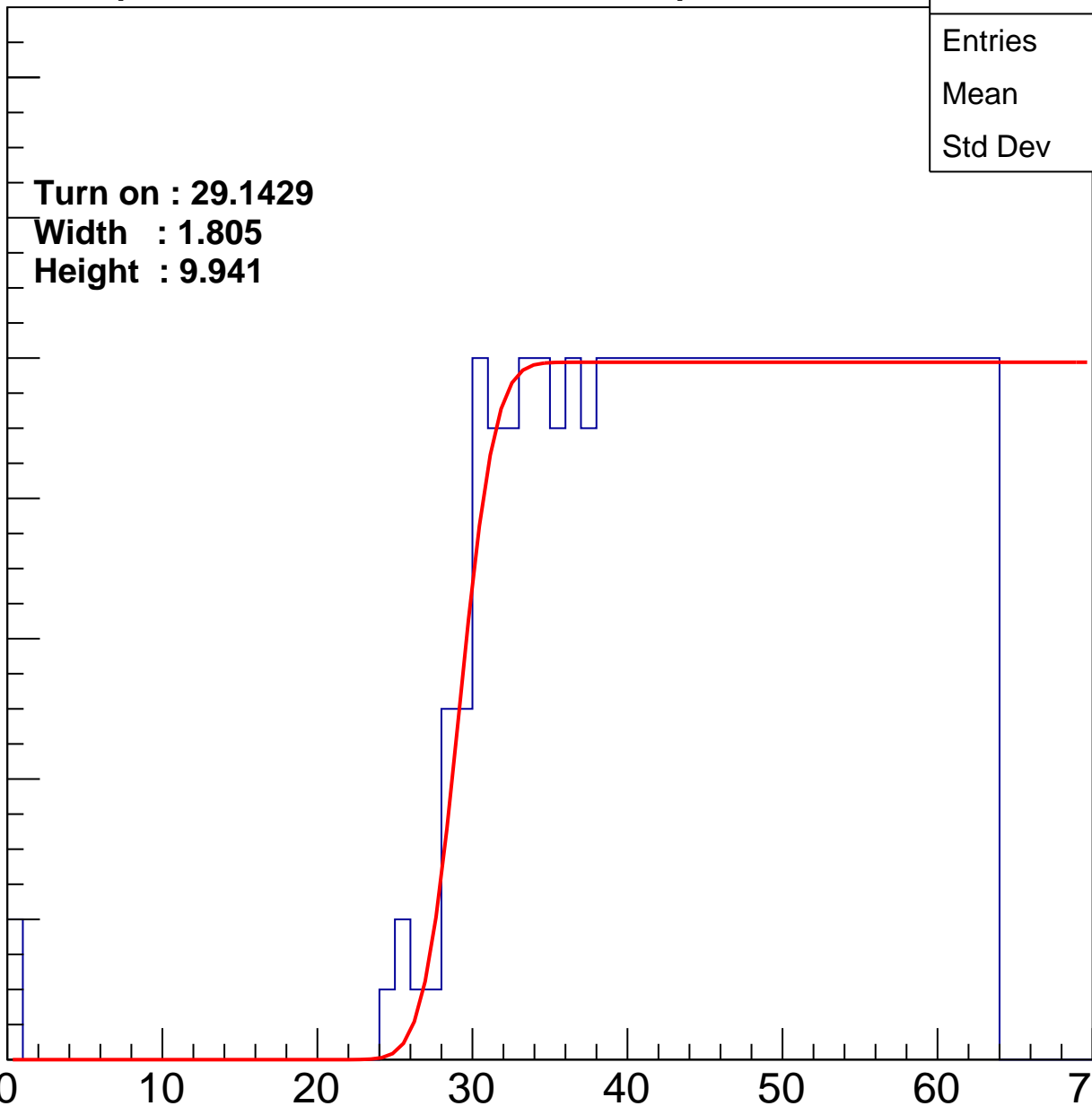
Entry

14
12
10
8
6
4
2
0

Turn on : 29.1429
Width : 1.805
Height : 9.941

Entries	353
Mean	45.57
Std Dev	10.85

ampl



B1L102S, U5-ch109

calib_packv5_042523_0143.root, FC#11, port A2

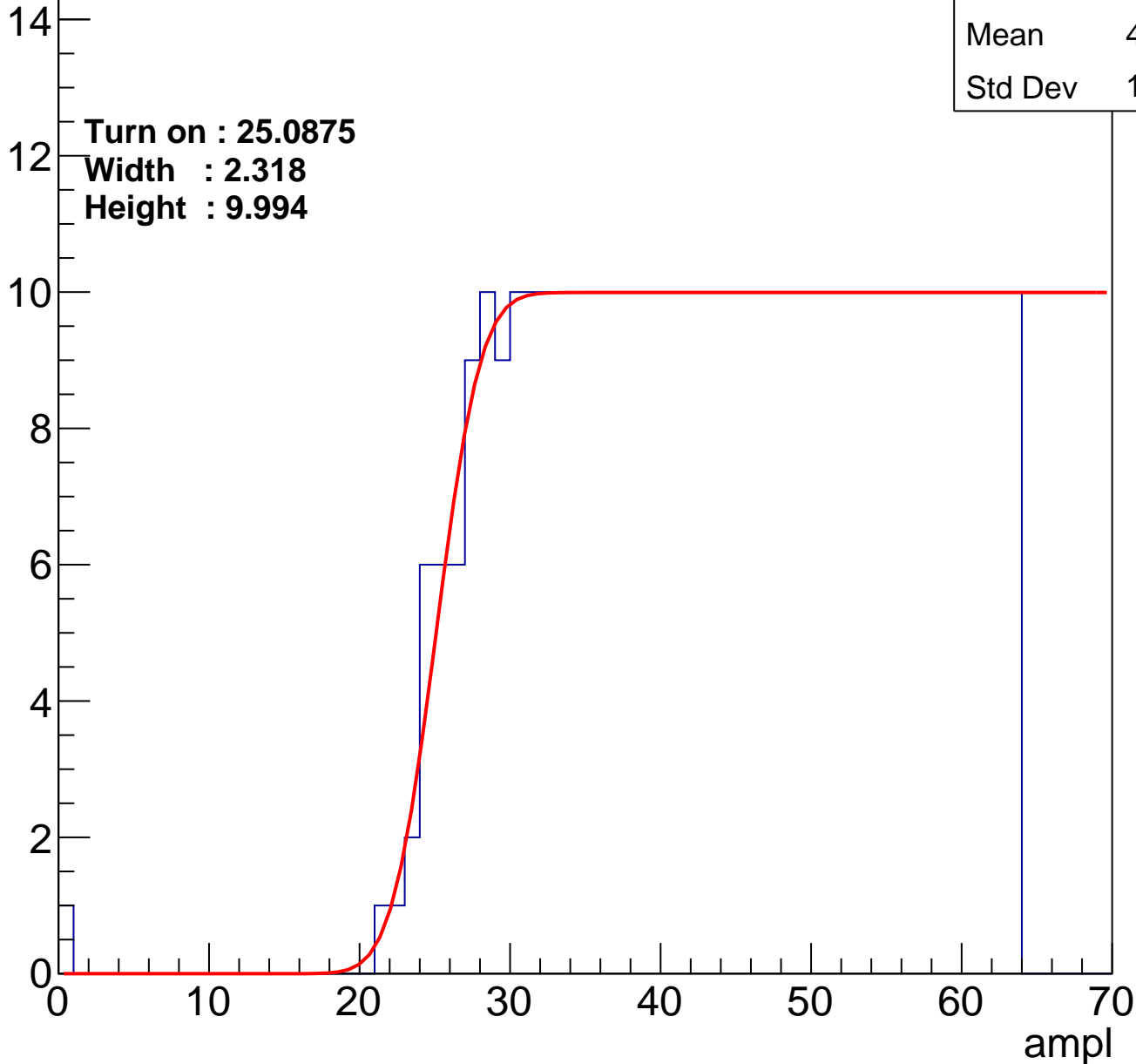
Entries	391
Mean	43.82
Std Dev	11.57

Turn on : 25.0875

Width : 2.318

Height : 9.994

Entry



B1L102S, U5-ch110

calib_packv5_042523_0143.root, FC#11, port A2

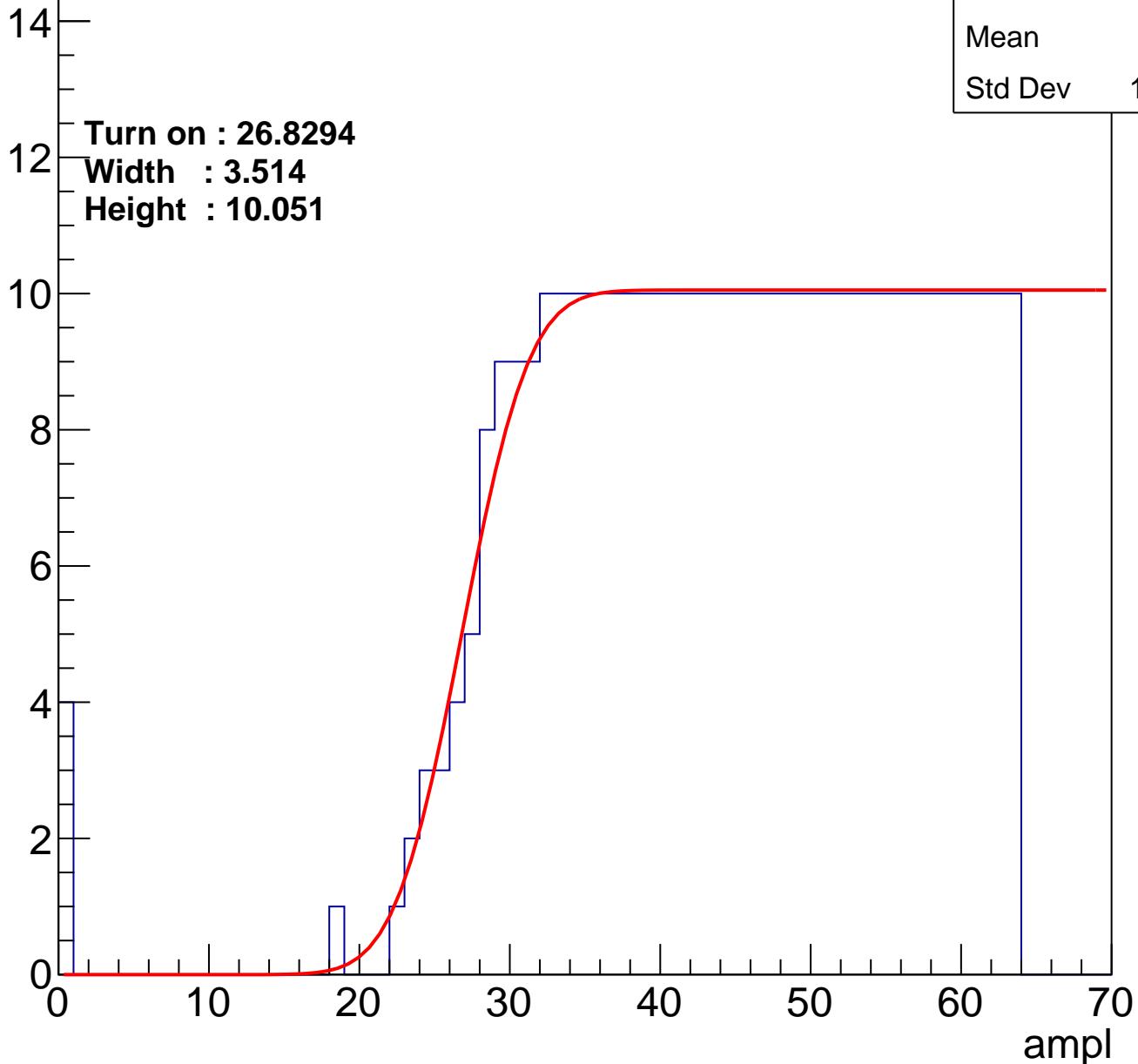
Entries	378
Mean	44.2
Std Dev	11.88

Turn on : 26.8294

Width : 3.514

Height : 10.051

Entry



B1L102S, U5-ch111

calib_packv5_042523_0143.root, FC#11, port A2

Entries	365
Mean	44.95
Std Dev	11.22

Turn on : 28.0520

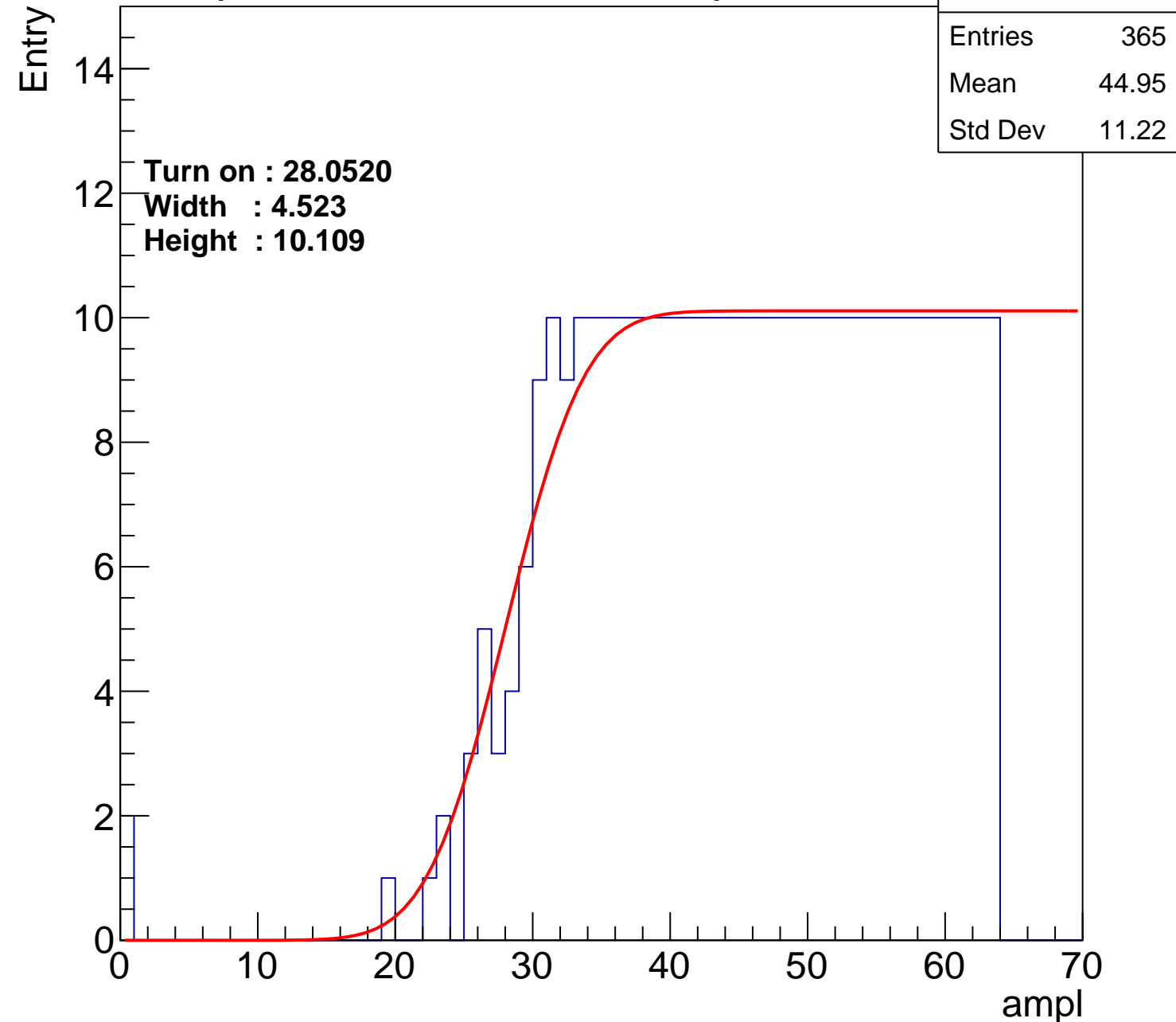
Width : 4.523

Height : 10.109

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch112

calib_packv5_042523_0143.root, FC#11, port A2

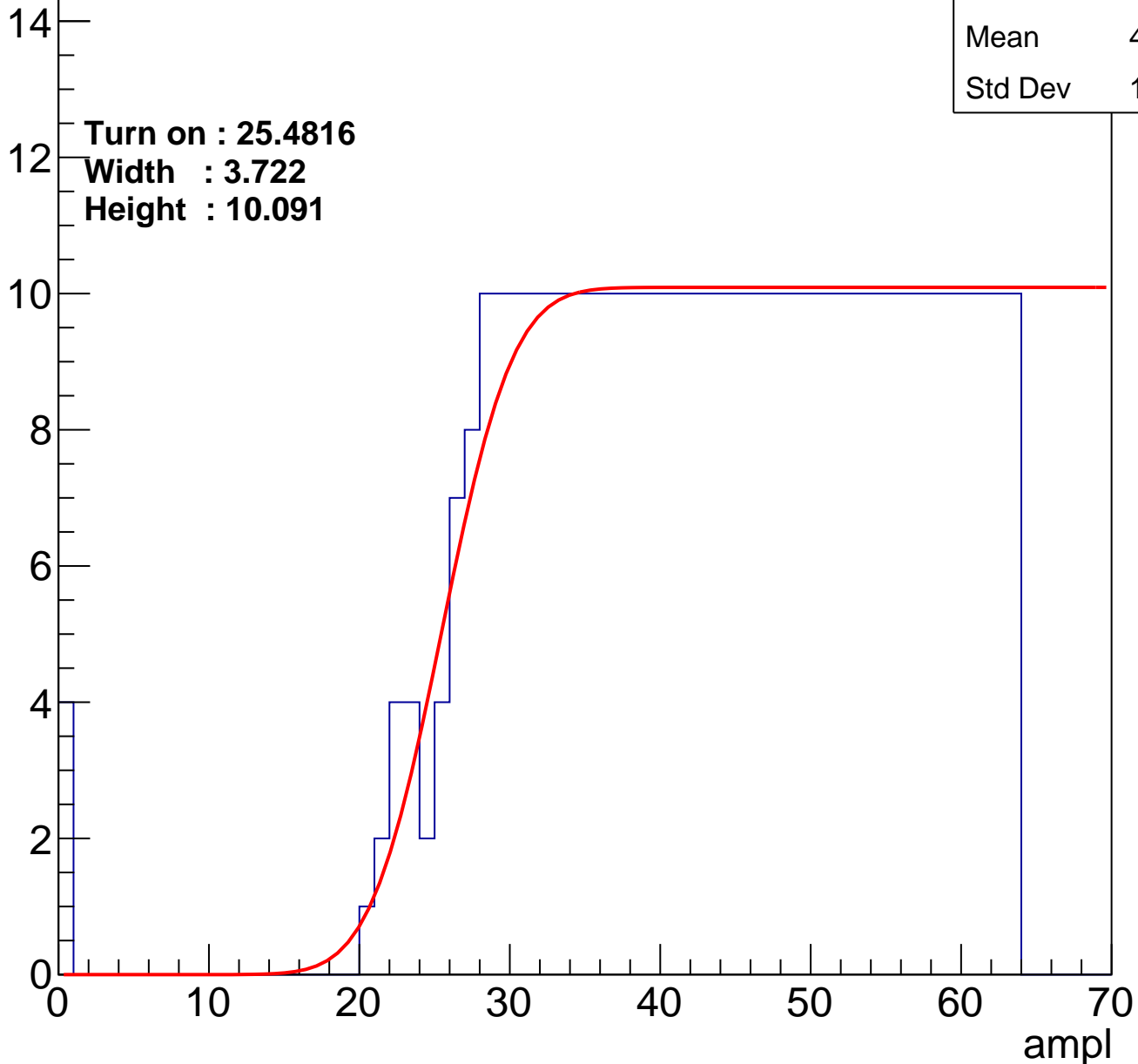
Entries	396
Mean	43.35
Std Dev	12.25

Turn on : 25.4816

Width : 3.722

Height : 10.091

Entry



B1L102S, U5-ch113

calib_packv5_042523_0143.root, FC#11, port A2

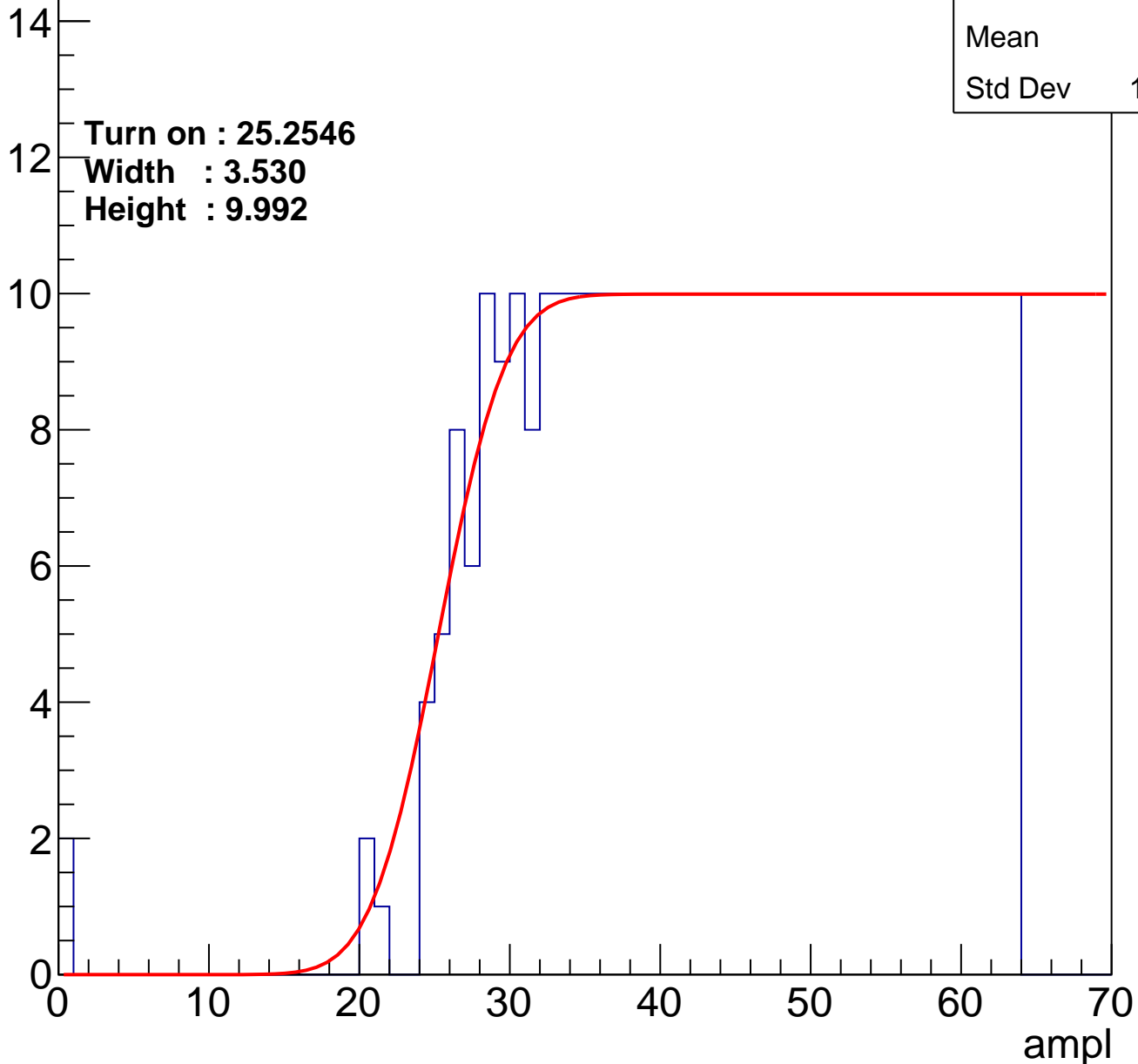
Entries	385
Mean	44
Std Dev	11.66

Turn on : 25.2546

Width : 3.530

Height : 9.992

Entry



B1L102S, U5-ch114

calib_packv5_042523_0143.root, FC#11, port A2

Entries	390
Mean	43.66
Std Dev	12.01

Turn on : 25.7620

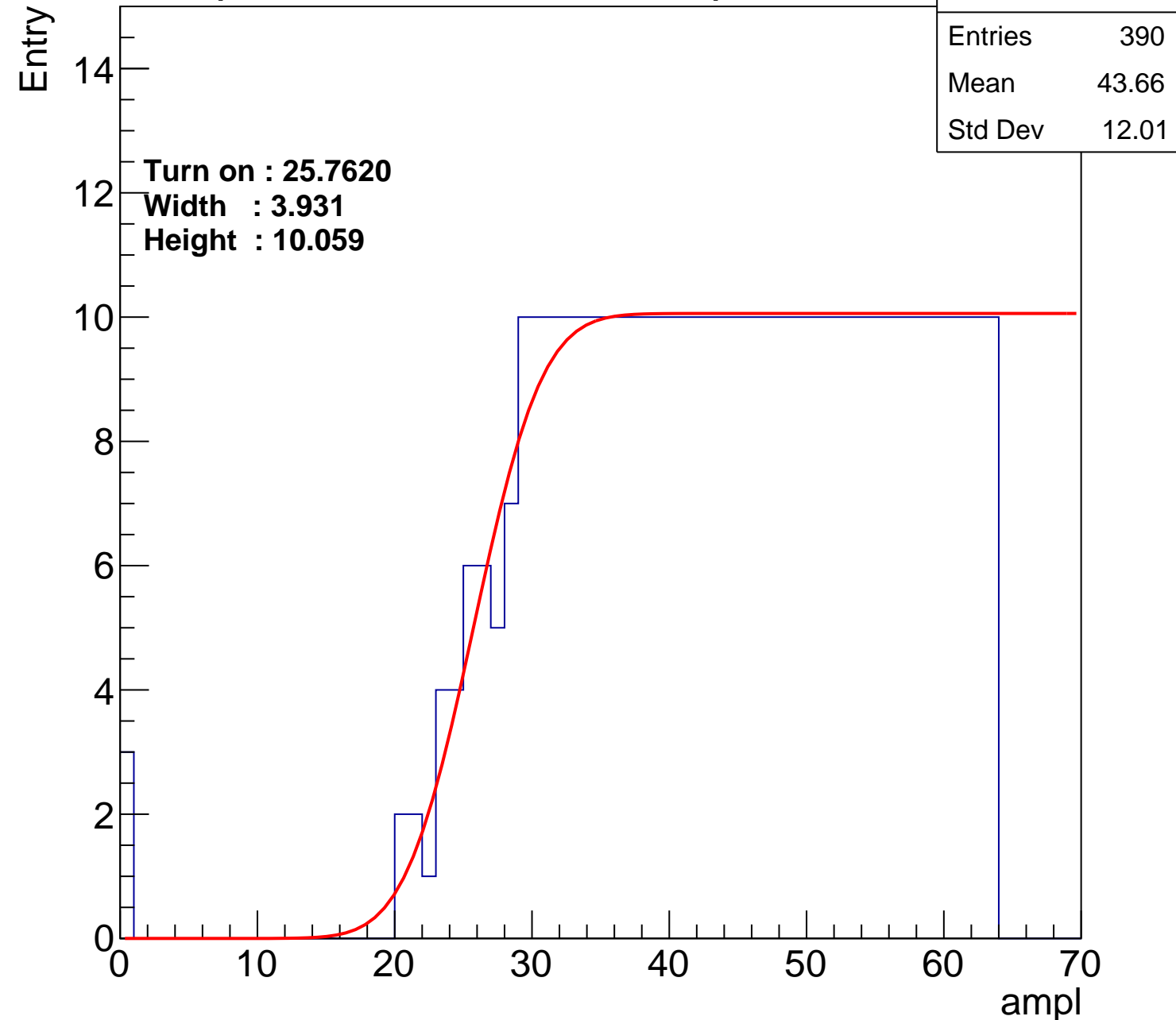
Width : 3.931

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch115

calib_packv5_042523_0143.root, FC#11, port A2

Entries	387
Mean	43.91
Std Dev	11.7

Turn on : 25.2456

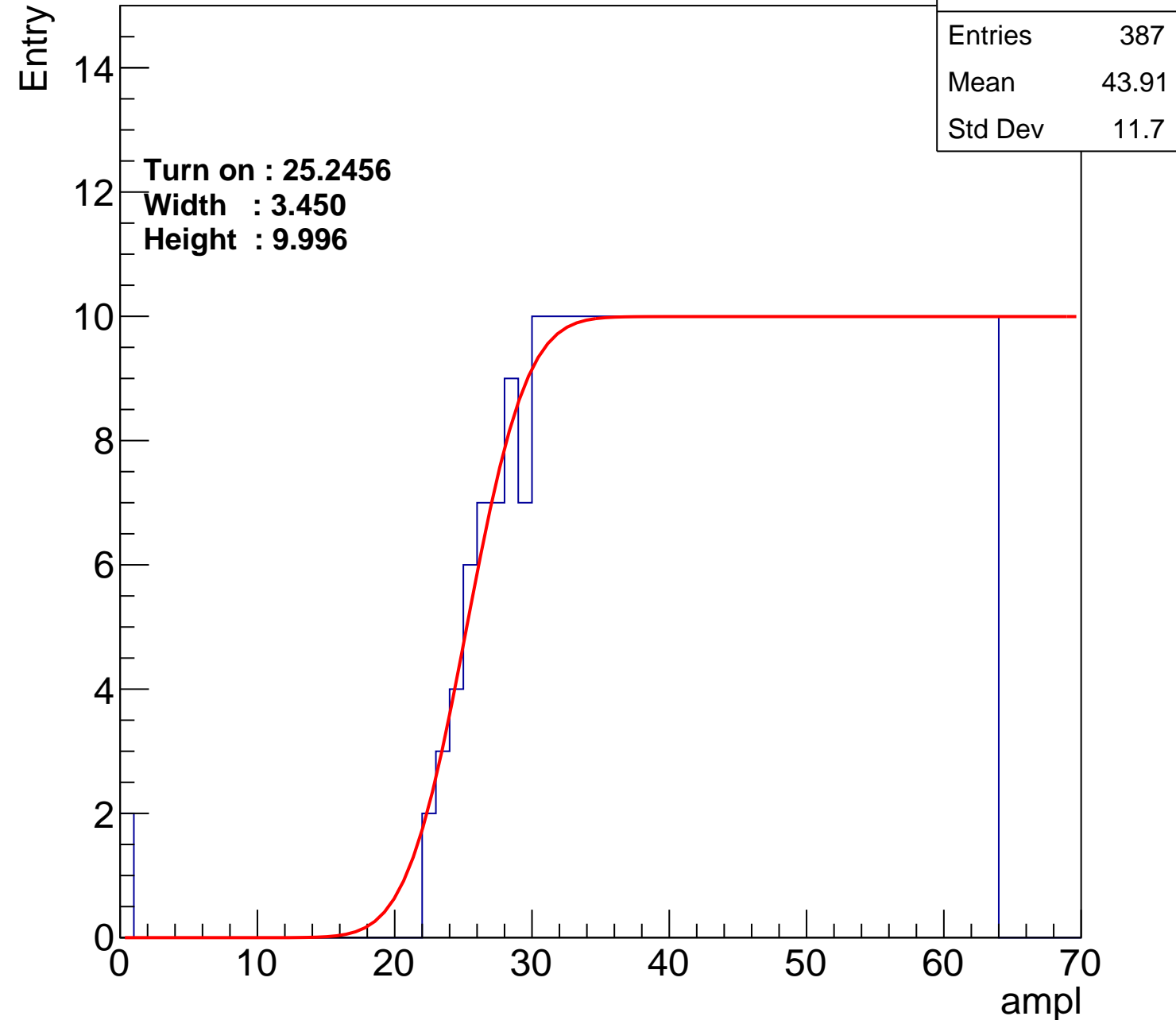
Width : 3.450

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch116

calib_packv5_042523_0143.root, FC#11, port A2

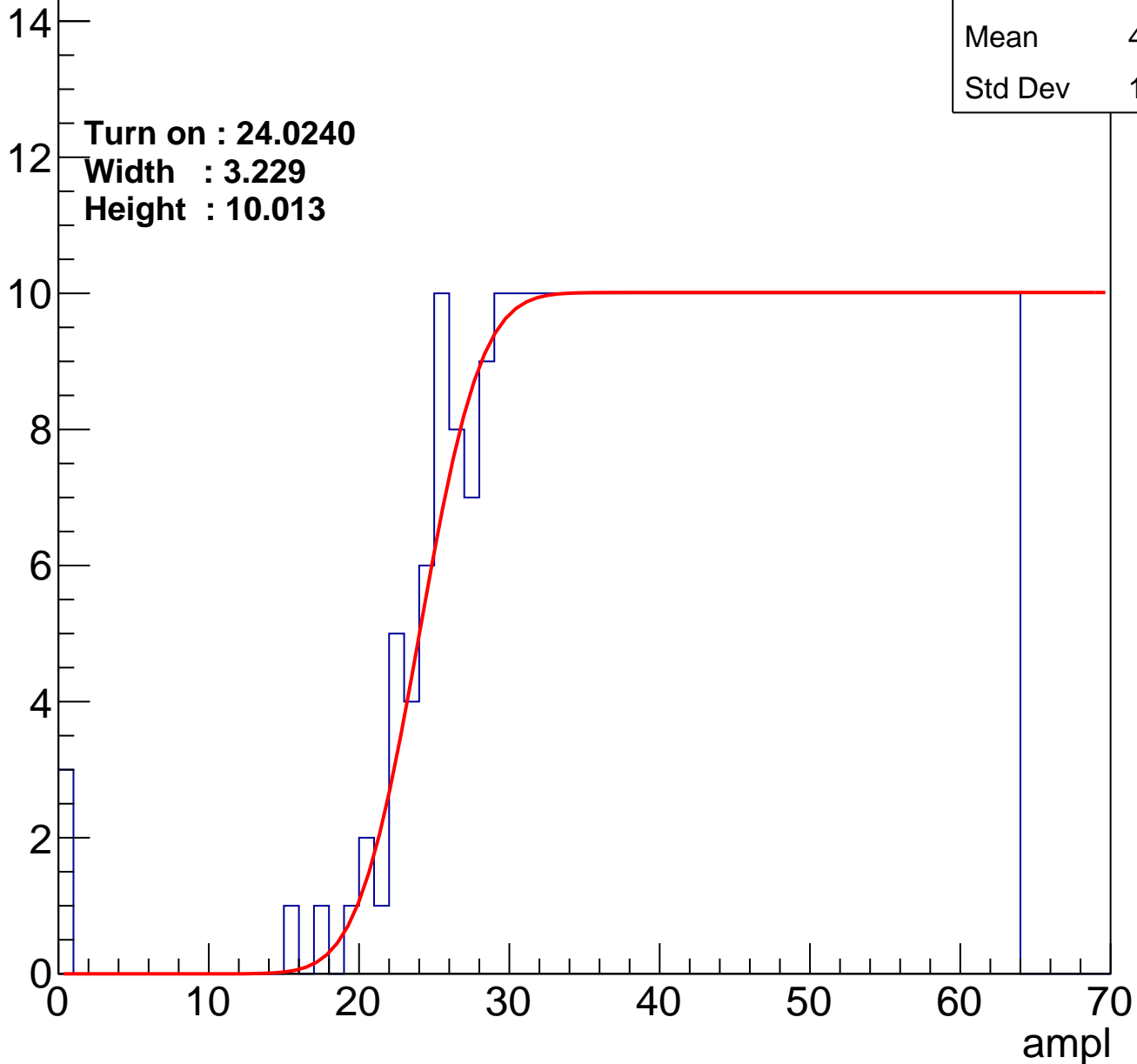
Entries	408
Mean	42.79
Std Dev	12.46

Turn on : 24.0240

Width : 3.229

Height : 10.013

Entry



B1L102S, U5-ch117

calib_packv5_042523_0143.root, FC#11, port A2

Entries	395
Mean	43.3
Std Dev	12.45

Turn on : 24.9260

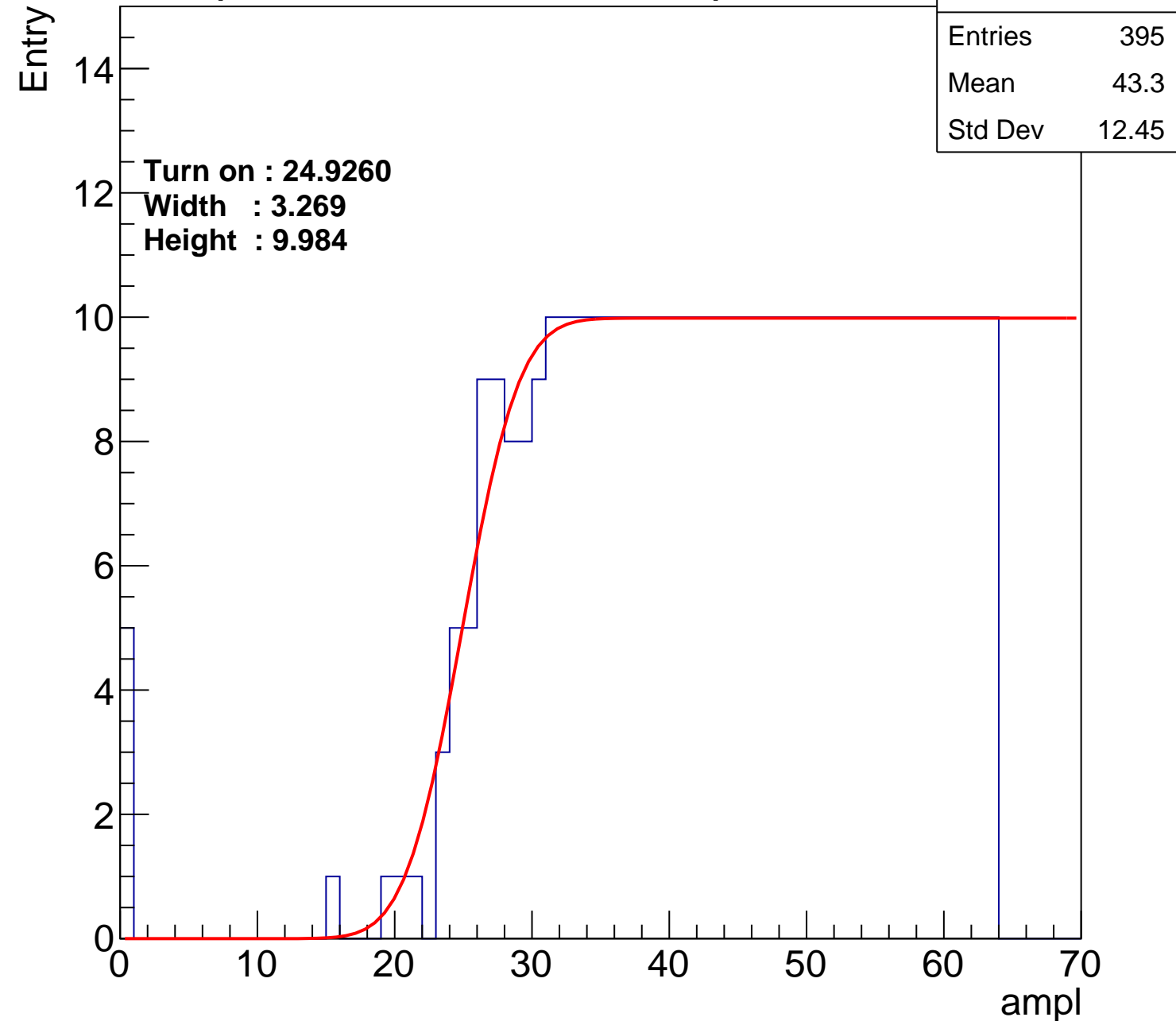
Width : 3.269

Height : 9.984

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch118

calib_packv5_042523_0143.root, FC#11, port A2

Entries	417
Mean	42.26
Std Dev	12.9

Turn on : 22.8588

Width : 2.717

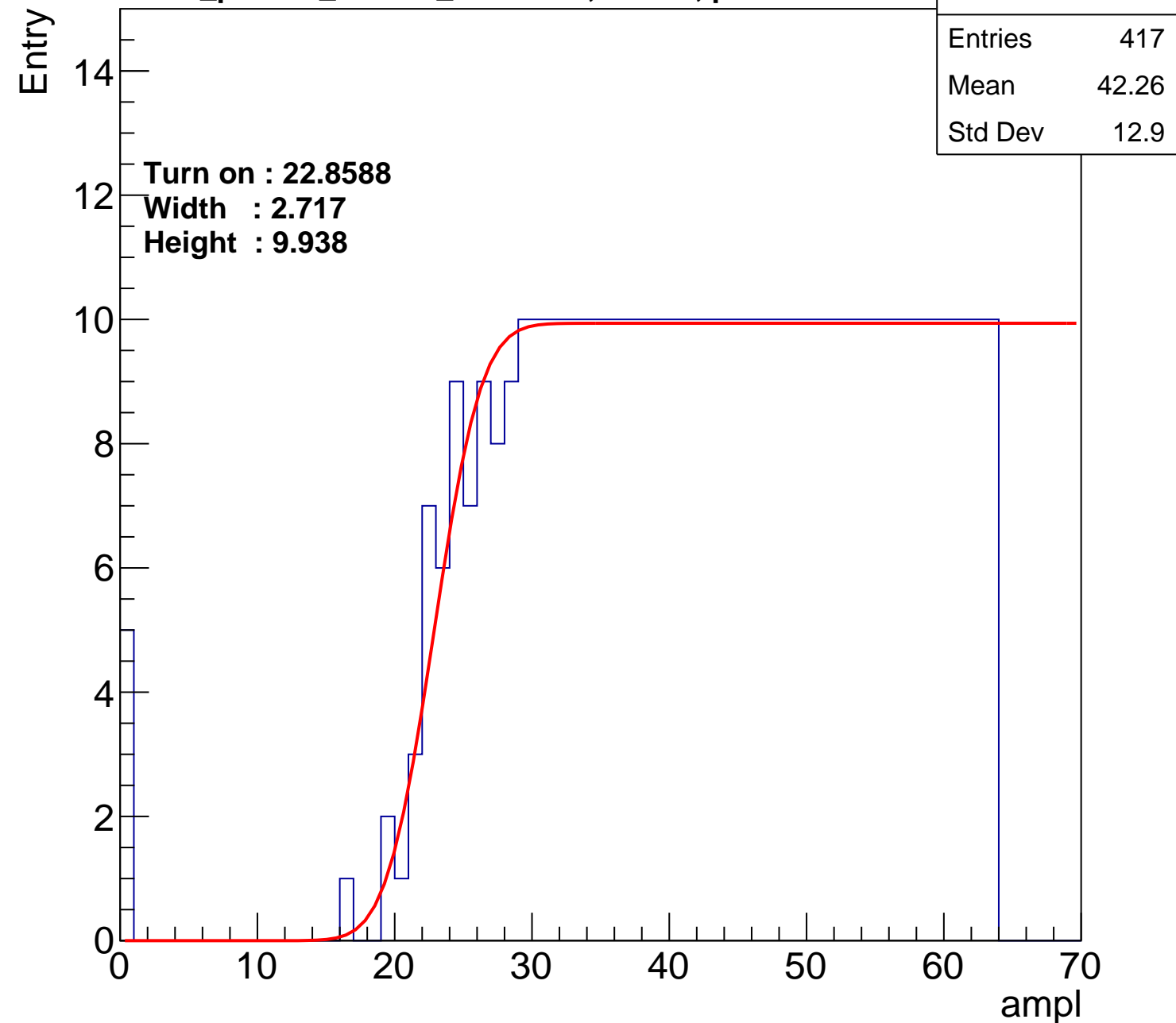
Height : 9.938

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L102S, U5-ch119

calib_packv5_042523_0143.root, FC#11, port A2

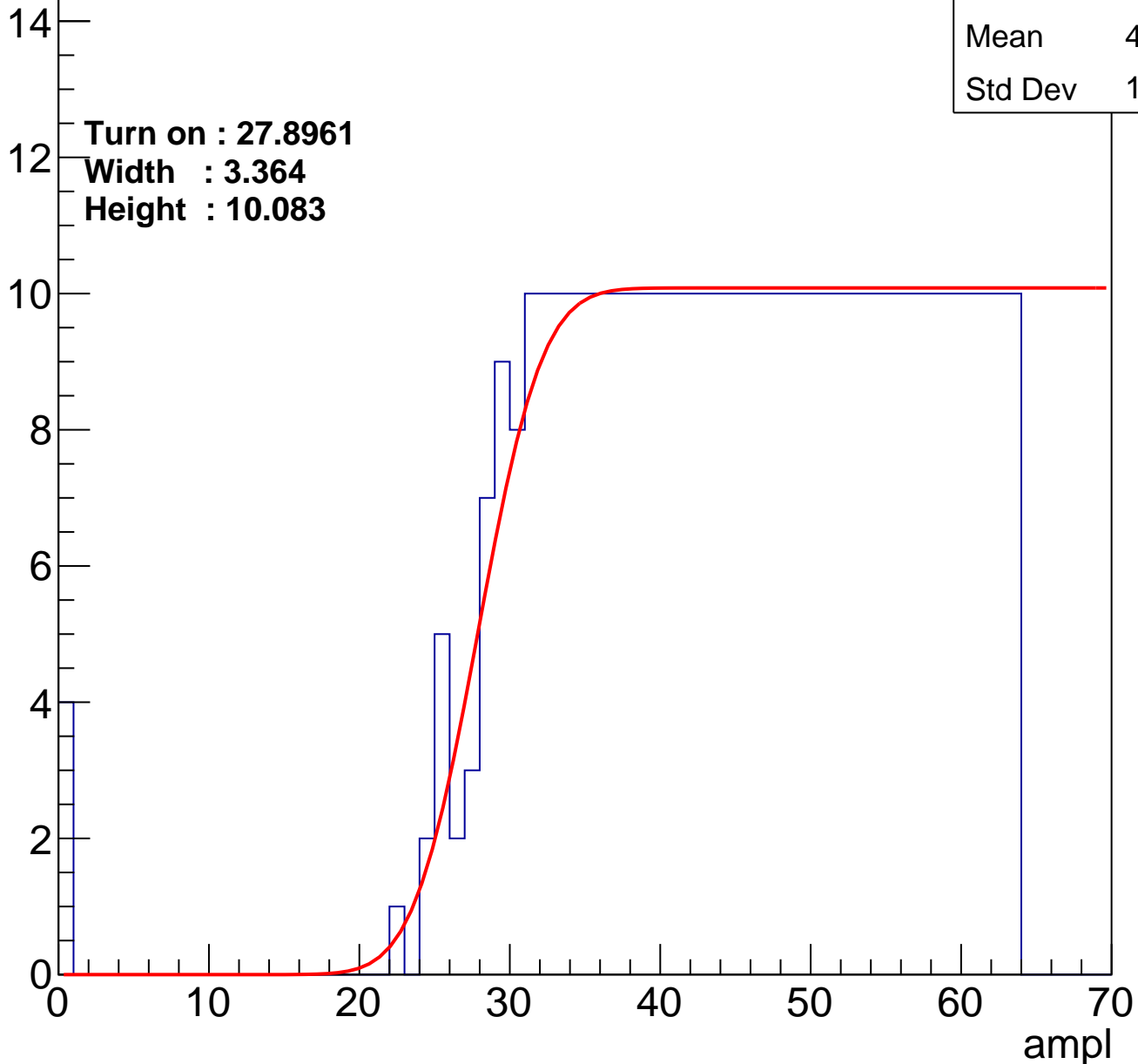
Entry

Entries	371
Mean	44.57
Std Dev	11.67

Turn on : 27.8961

Width : 3.364

Height : 10.083



B1L102S, U5-ch120

calib_packv5_042523_0143.root, FC#11, port A2

Entries	381
Mean	44.17
Std Dev	11.62

Turn on : 26.2149

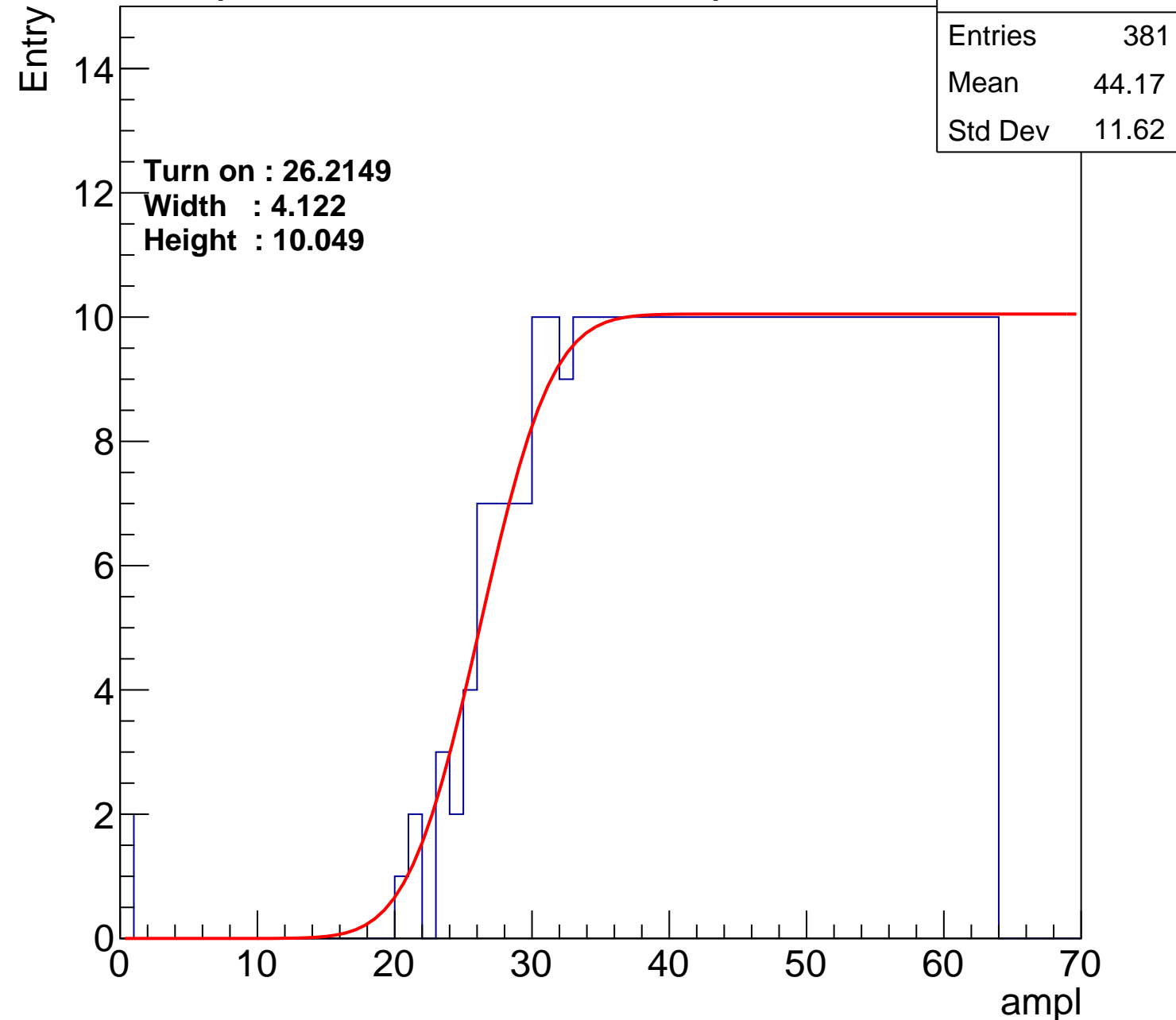
Width : 4.122

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch121

calib_packv5_042523_0143.root, FC#11, port A2

Entries	381
Mean	43.97
Std Dev	12.13

Turn on : 26.4301

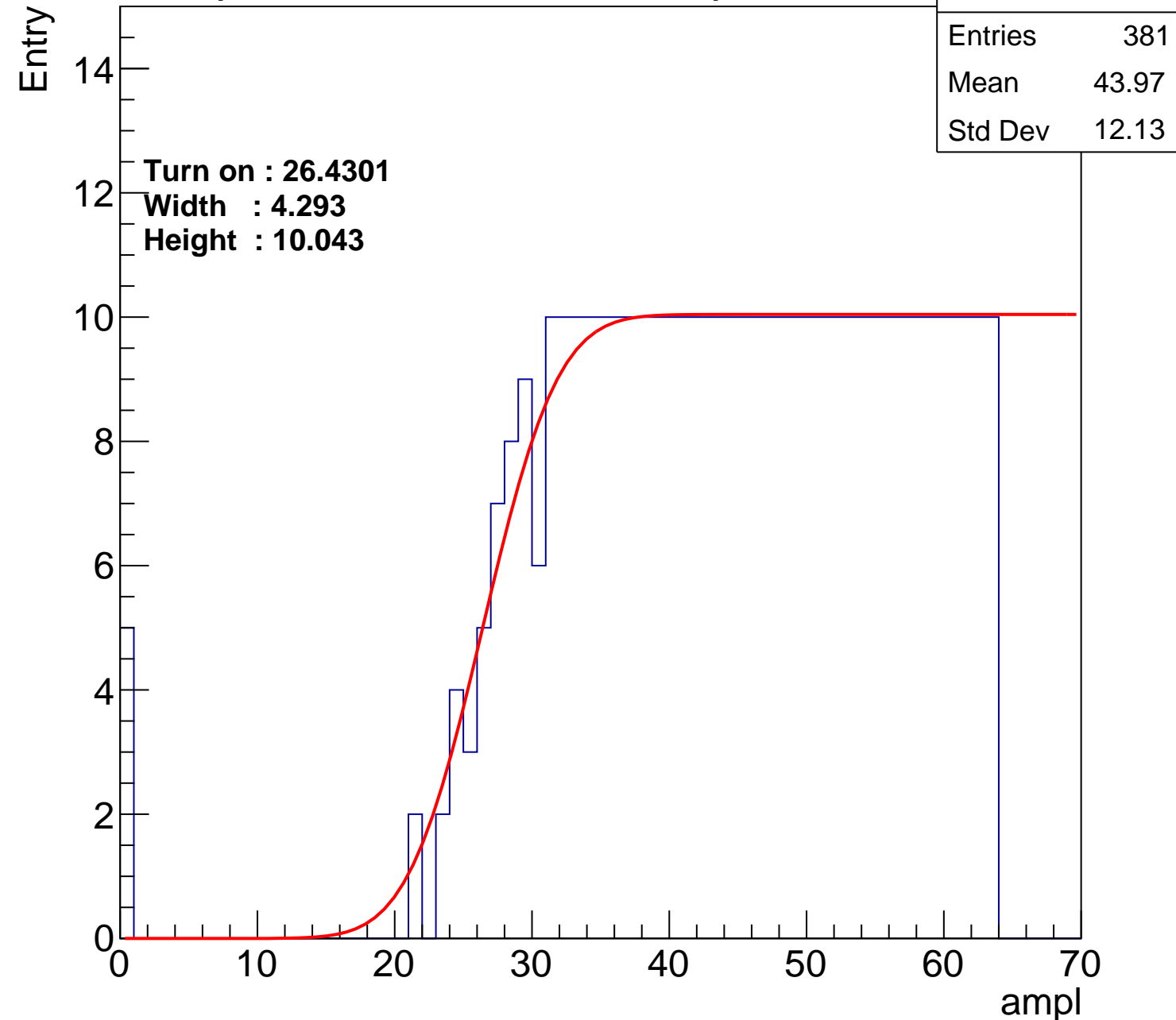
Width : 4.293

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch122

calib_packv5_042523_0143.root, FC#11, port A2

Entries	377
Mean	44.38
Std Dev	11.42

Turn on : 26.4981

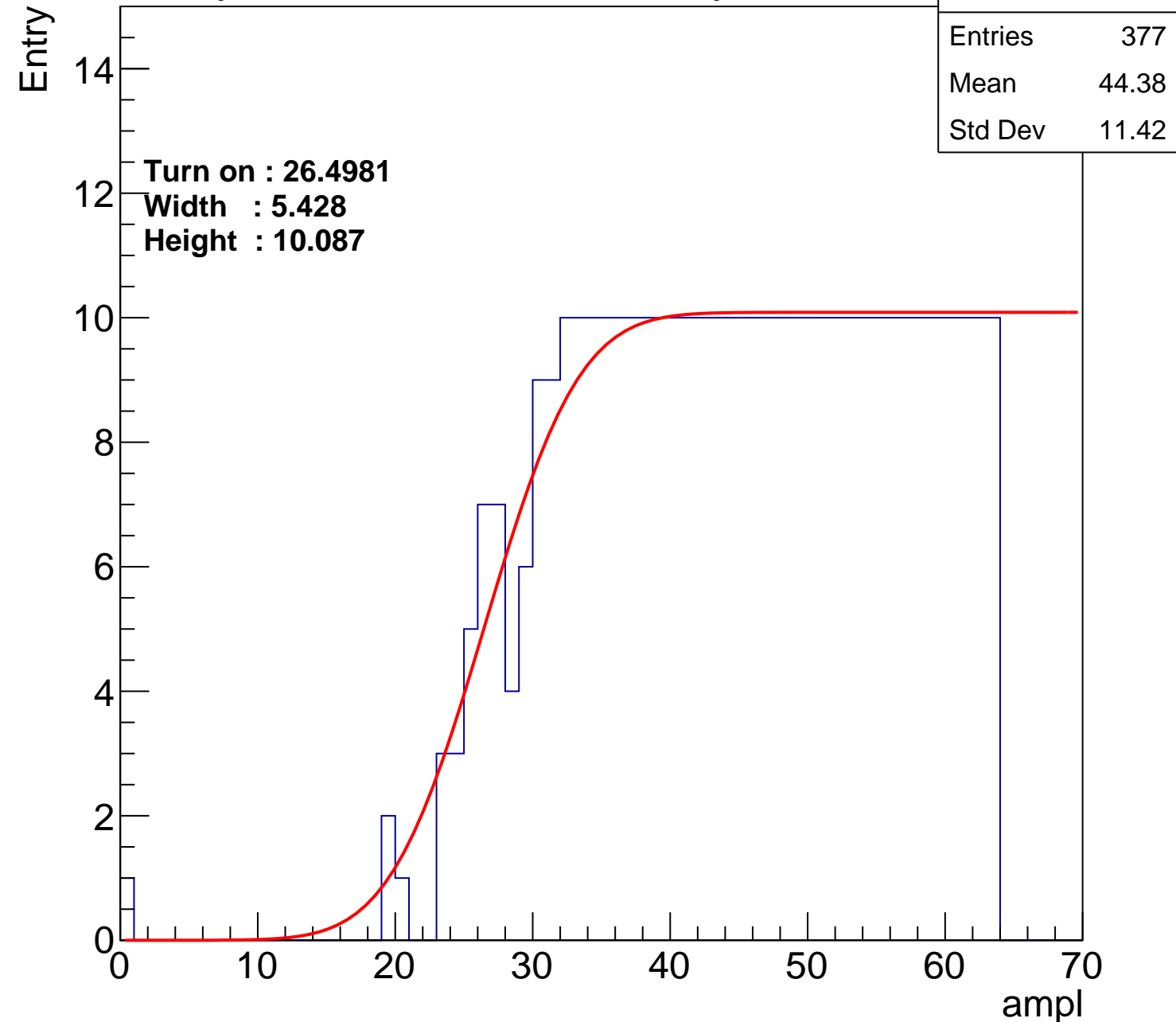
Width : 5.428

Height : 10.087

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch123

calib_packv5_042523_0143.root, FC#11, port A2

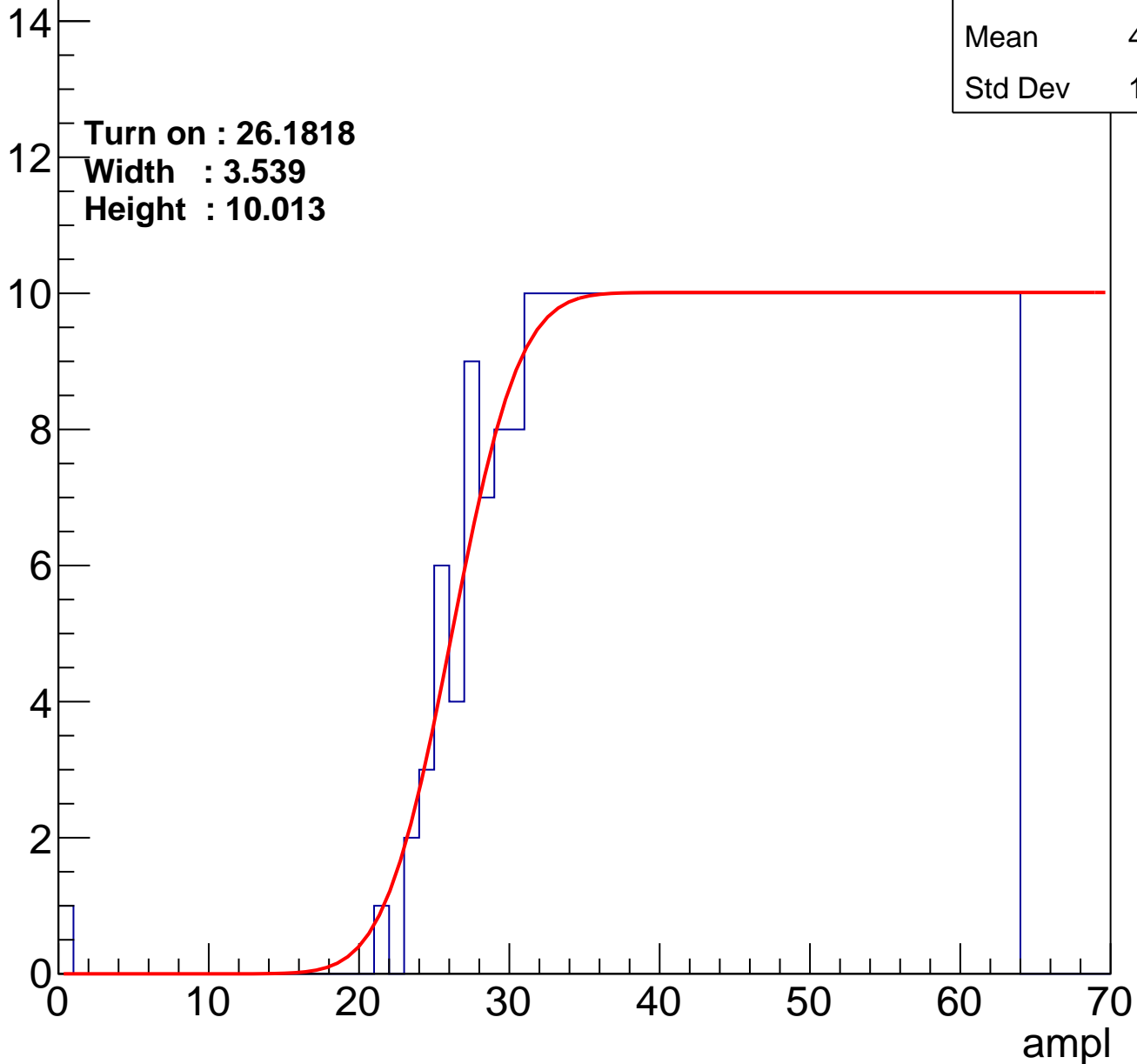
Entries	379
Mean	44.36
Std Dev	11.33

Turn on : 26.1818

Width : 3.539

Height : 10.013

Entry



B1L102S, U5-ch124

calib_packv5_042523_0143.root, FC#11, port A2

Entries	385
Mean	44.05
Std Dev	11.52

Turn on : 26.0061

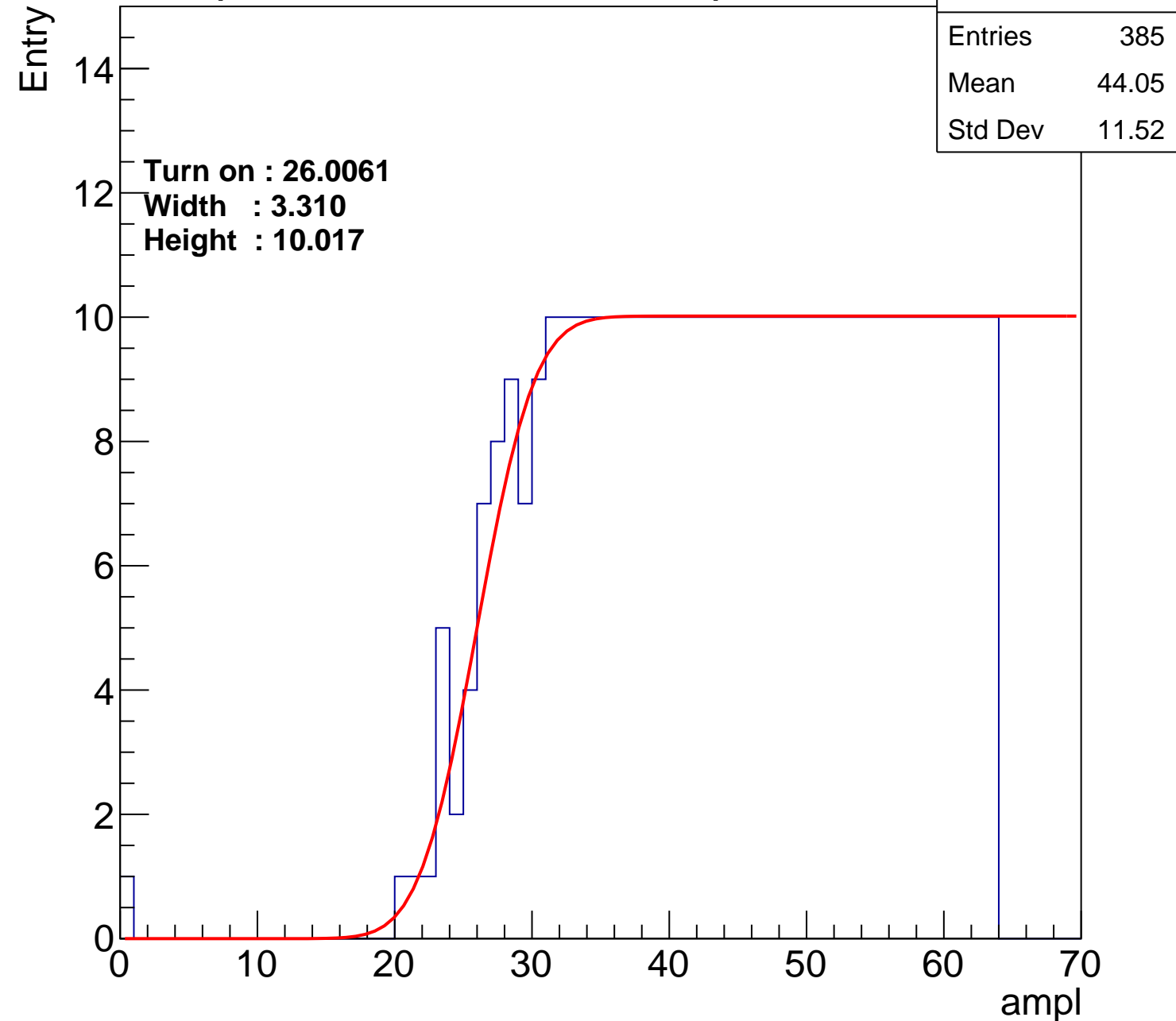
Width : 3.310

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L102S, U5-ch125

calib_packv5_042523_0143.root, FC#11, port A2

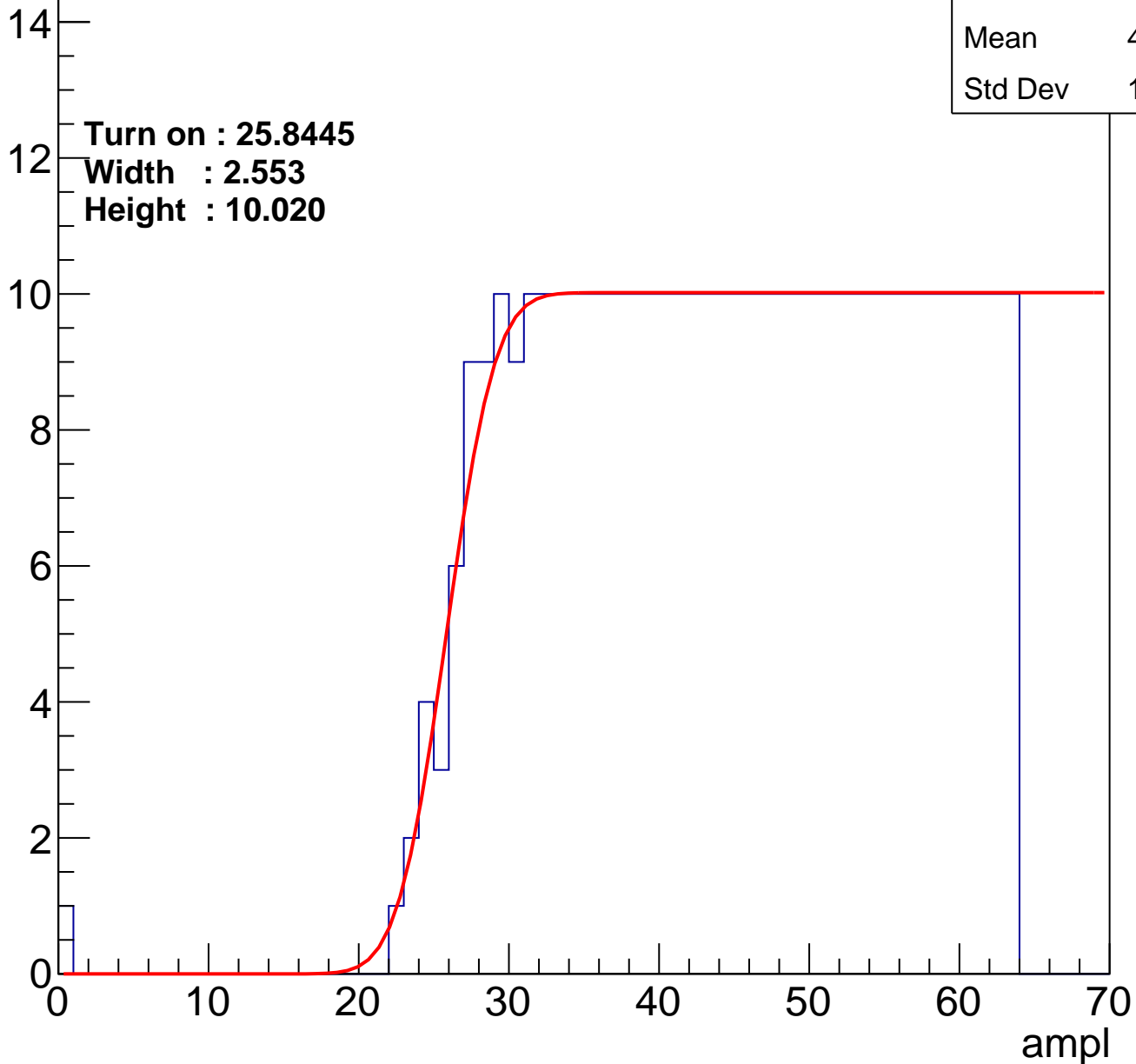
Entries	384
Mean	44.17
Std Dev	11.38

Turn on : 25.8445

Width : 2.553

Height : 10.020

Entry



B1L102S, U5-ch126

calib_packv5_042523_0143.root, FC#11, port A2

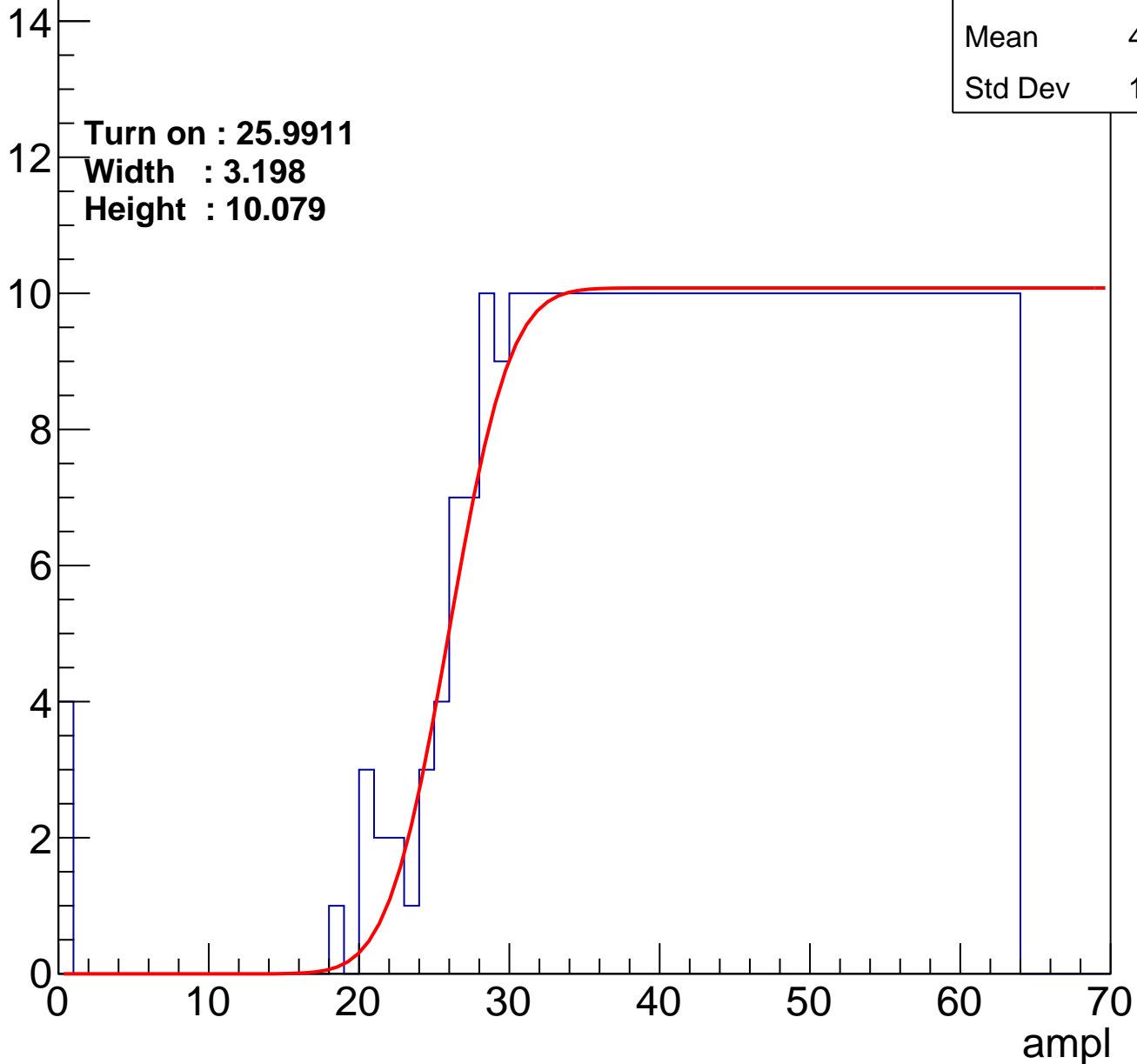
Entries	393
Mean	43.46
Std Dev	12.24

Turn on : 25.9911

Width : 3.198

Height : 10.079

Entry



B1L102S, U5-ch127

calib_packv5_042523_0143.root, FC#11, port A2

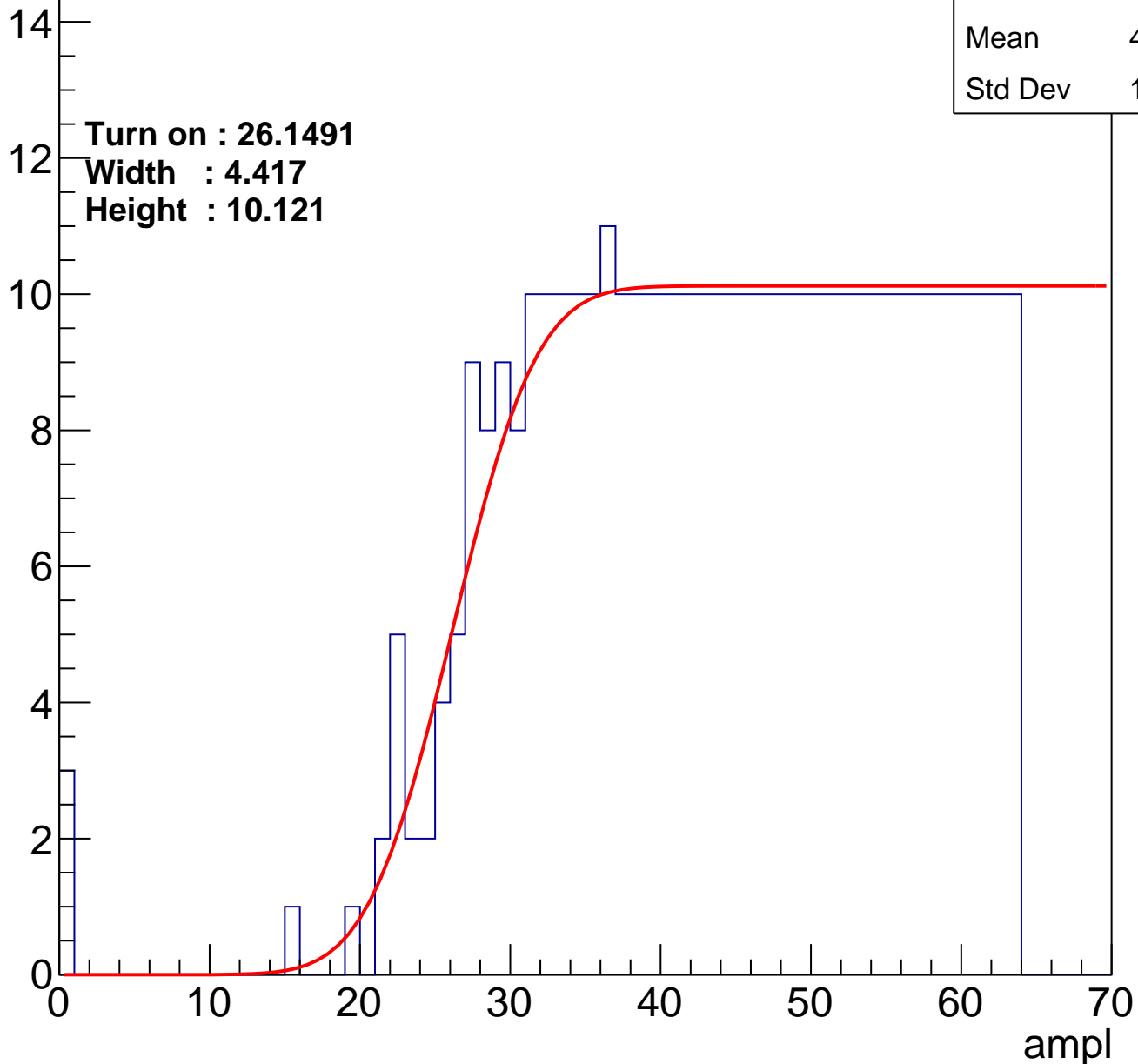
Entries	390
Mean	43.65
Std Dev	12.05

Turn on : 26.1491

Width : 4.417

Height : 10.121

Entry



B1L102S, U5-ch127

calib_packv5_042523_0143.root, FC#11, port A2

Entries	390
Mean	43.65
Std Dev	12.05

Turn on : 26.1491

Width : 4.417

Height : 10.121

Entry

14
12
10
8
6
4
2
0

ampl

