

B1L103S, U14-ch0, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	57
Mean	22.49
Std Dev	12.05

Entry

10

8

6

4

2

0

0

10

20

30

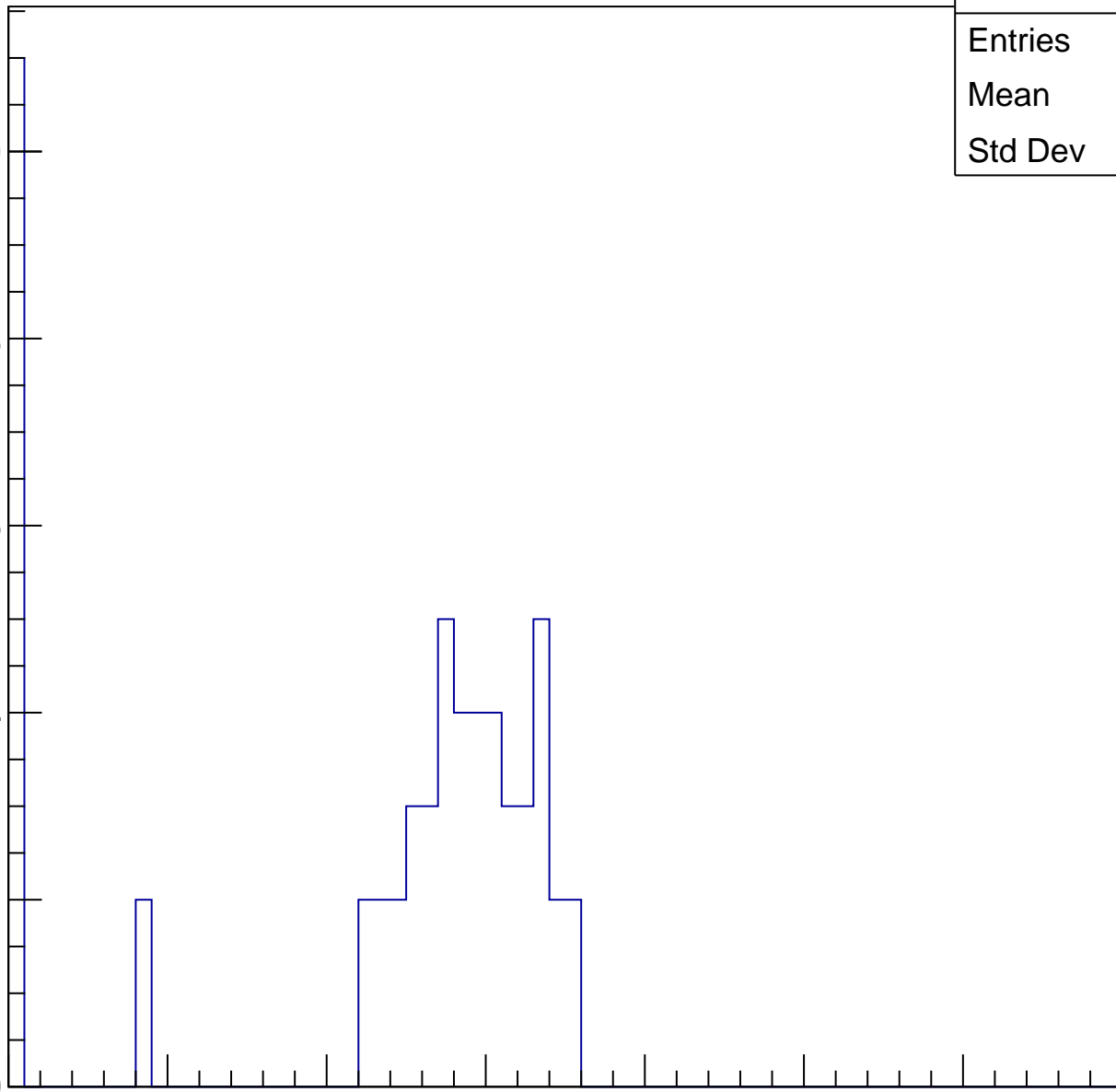
40

50

60

70

ampl

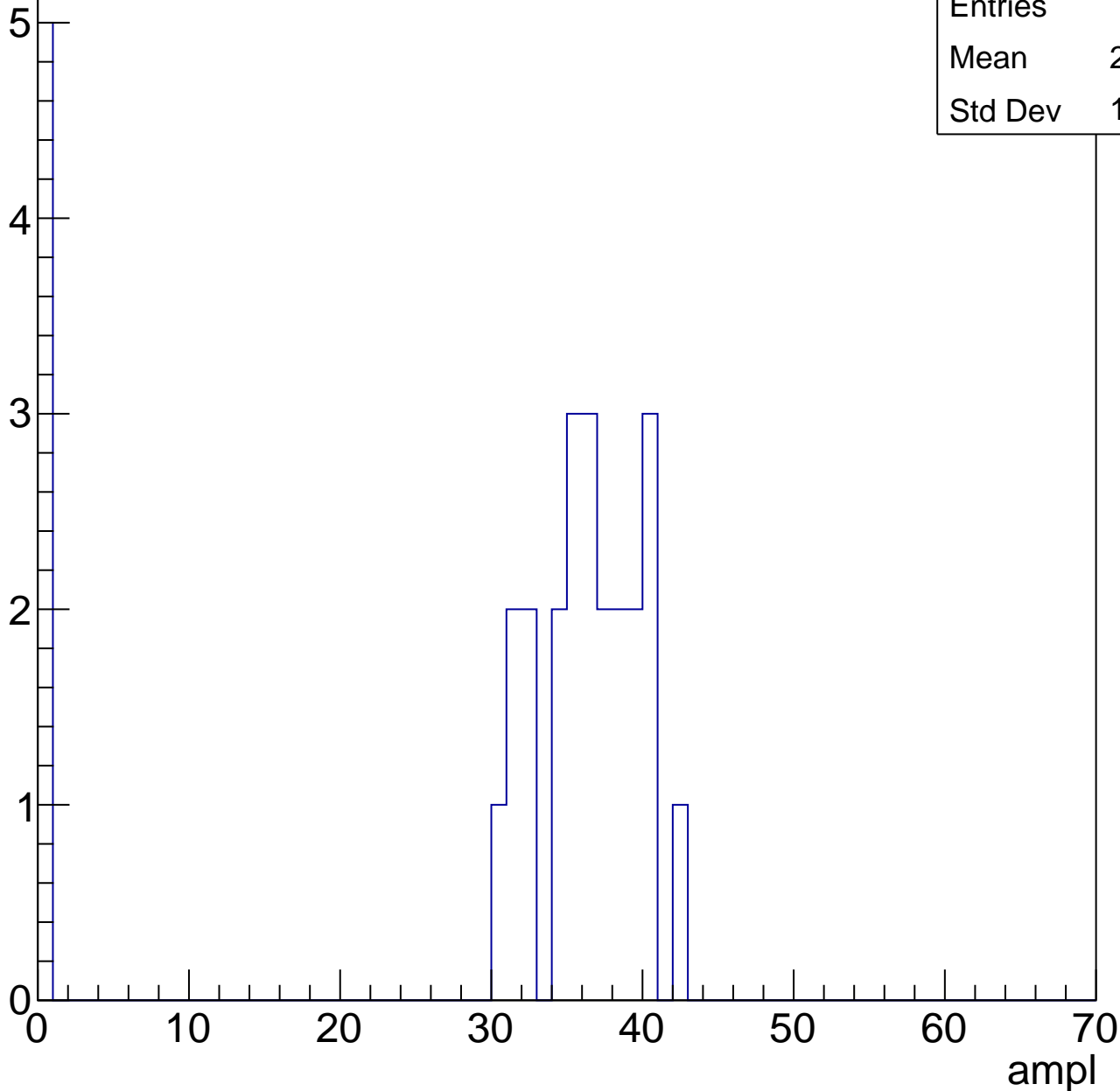


B1L103S, U14-ch0, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	28
Mean	29.54
Std Dev	14.08

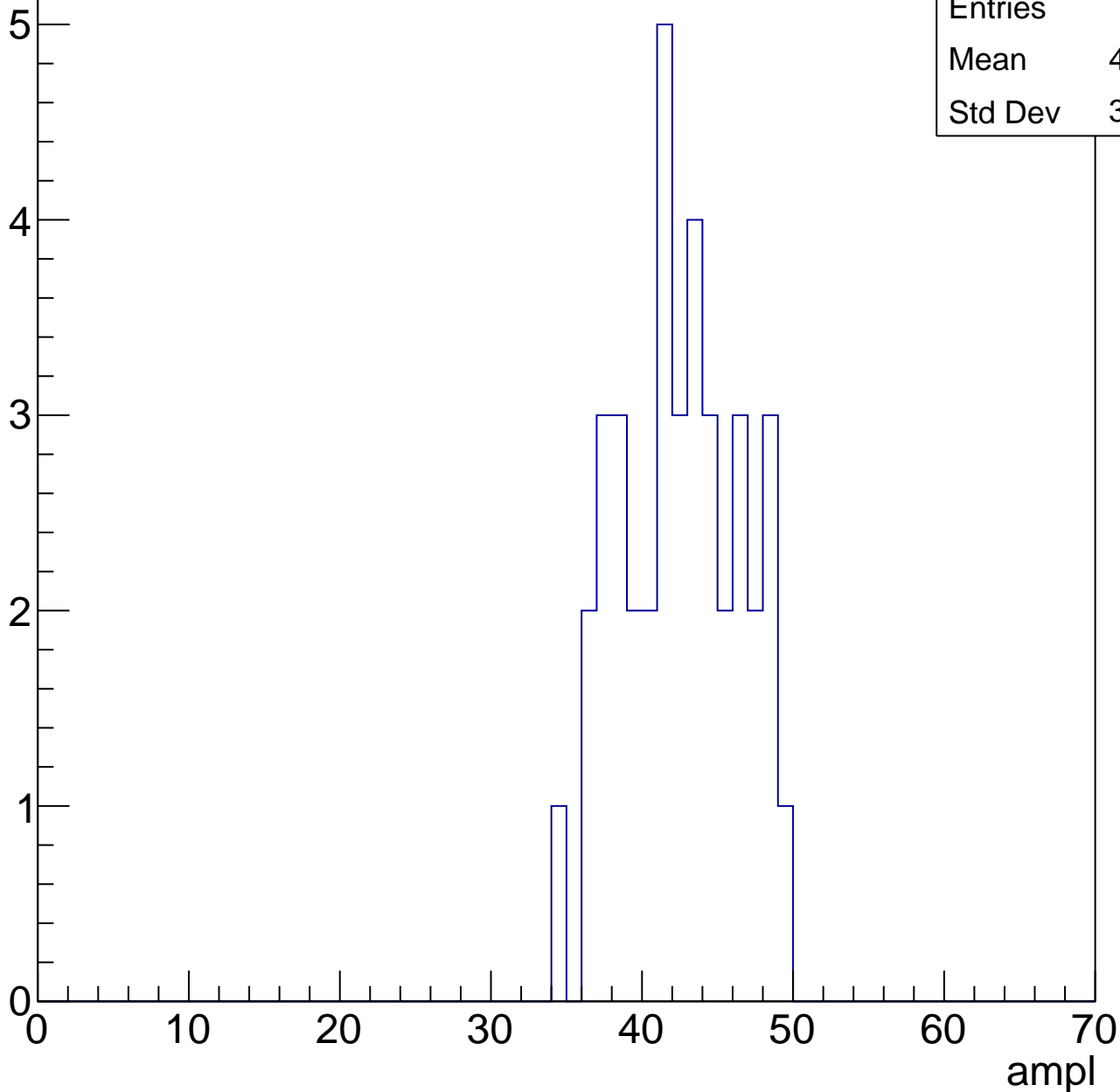


B1L103S, U14-ch0, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

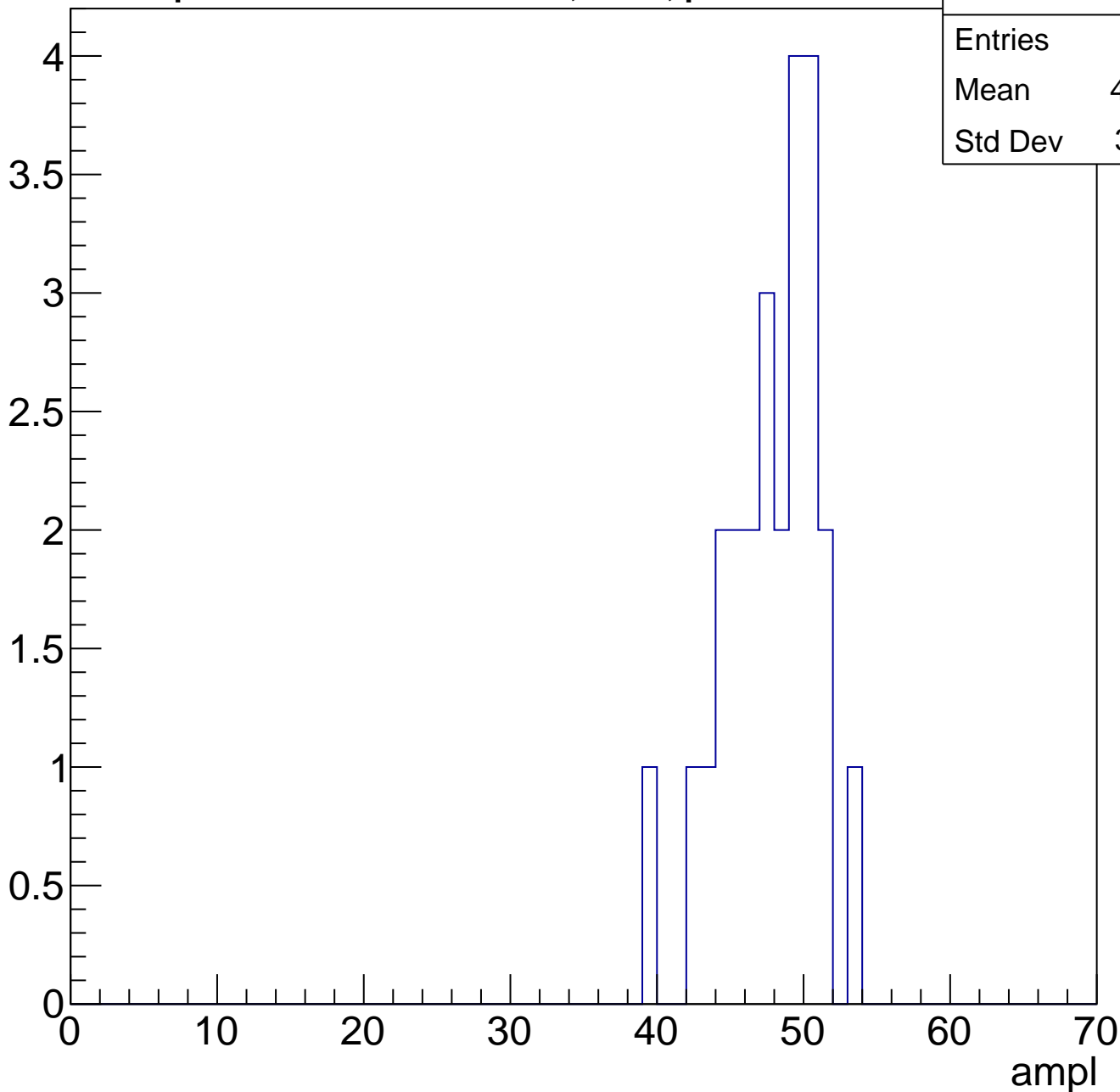
Entries	39
Mean	42.03
Std Dev	3.853



B1L103S, U14-ch0, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry



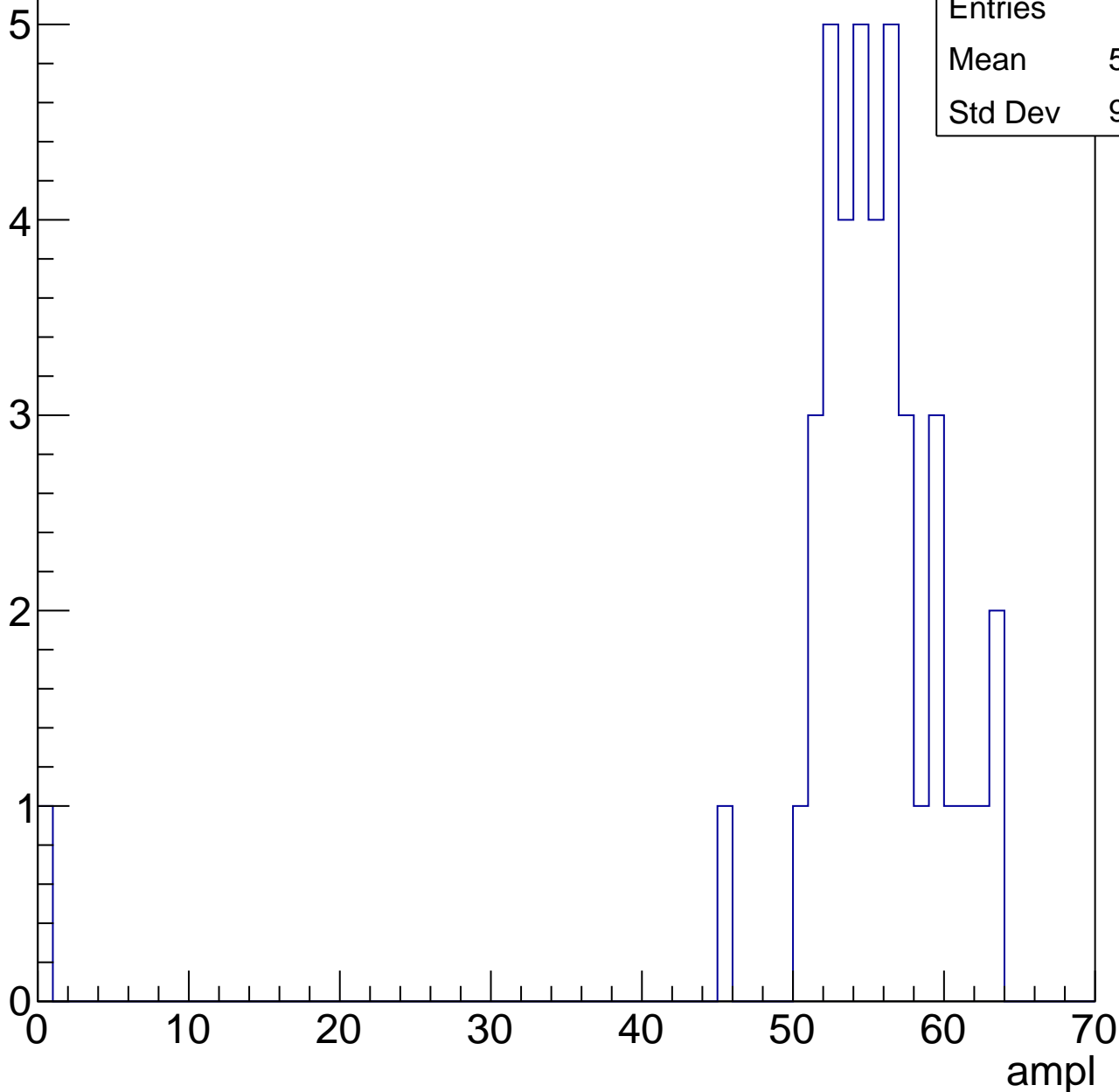
Entries	25
Mean	47.28
Std Dev	3.181

B1L103S, U14-ch0, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

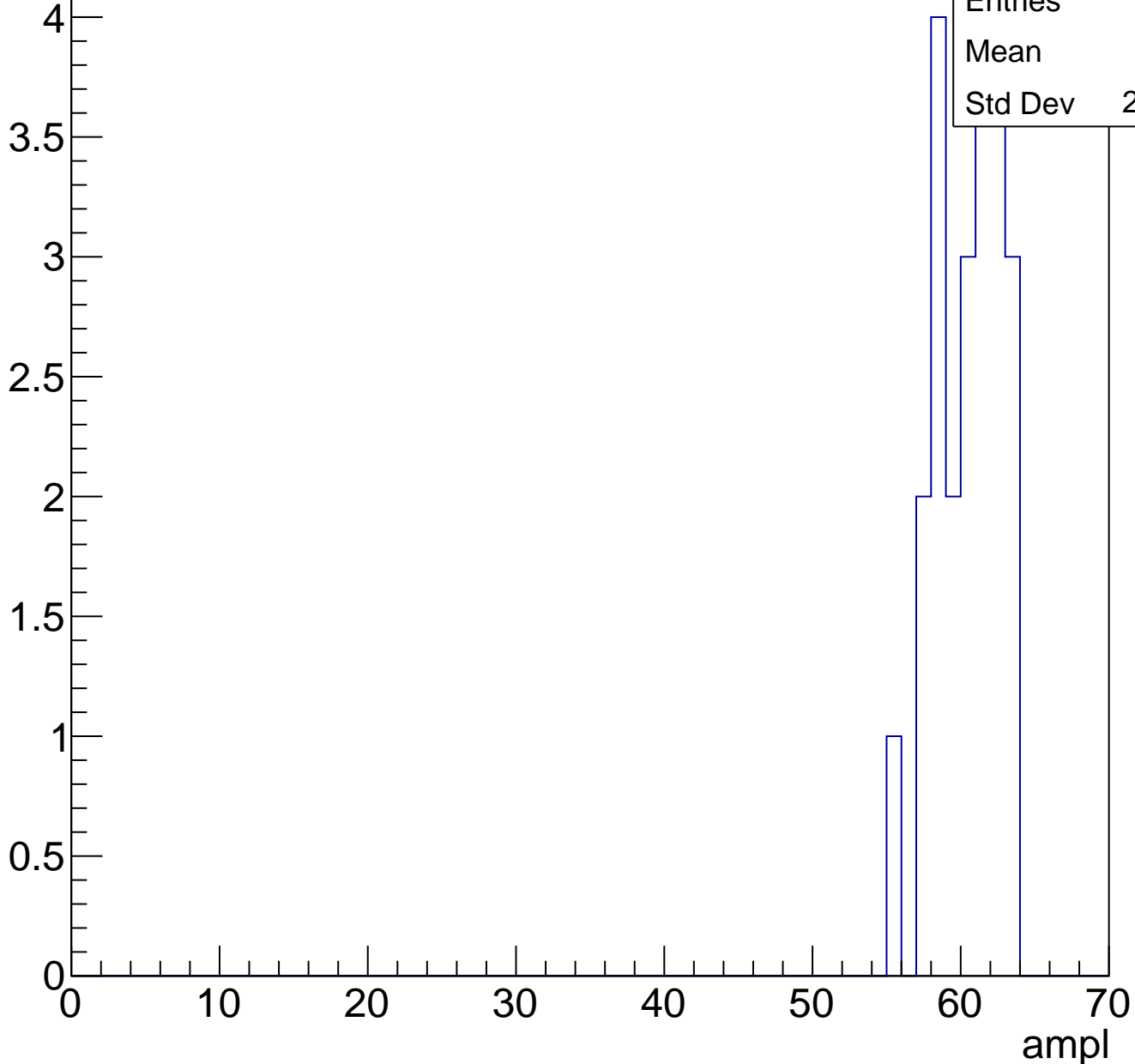
Entries	41
Mean	53.78
Std Dev	9.259



B1L103S, U14-ch0, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch0, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

1
0.8
0.6
0.4
0.2
0

Entries	1
Mean	60
Std Dev	0

ampl

B1L103S, U14-ch0, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

Entries

11

Mean

0

Std Dev

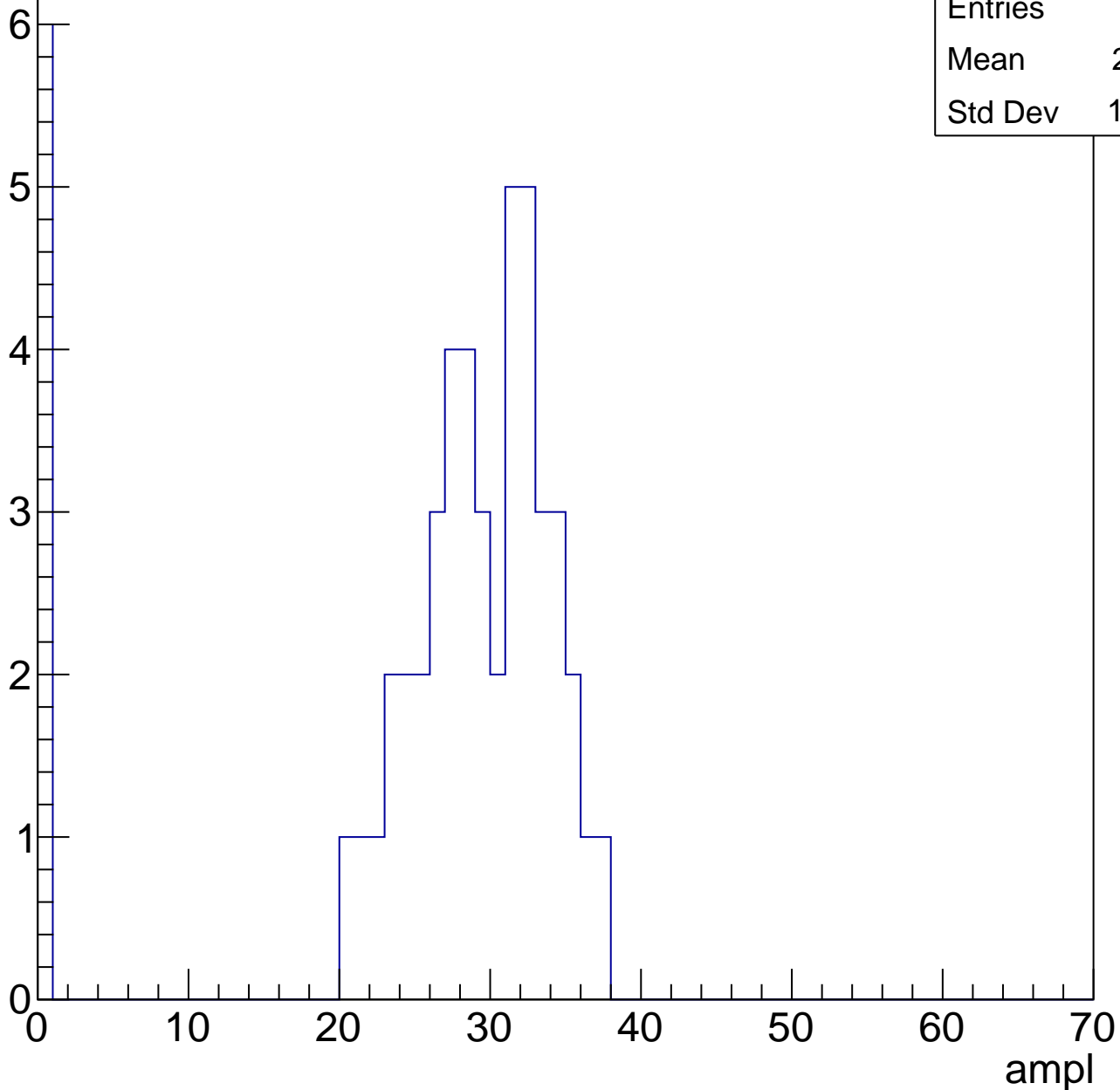
0

B1L103S, U14-ch1, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

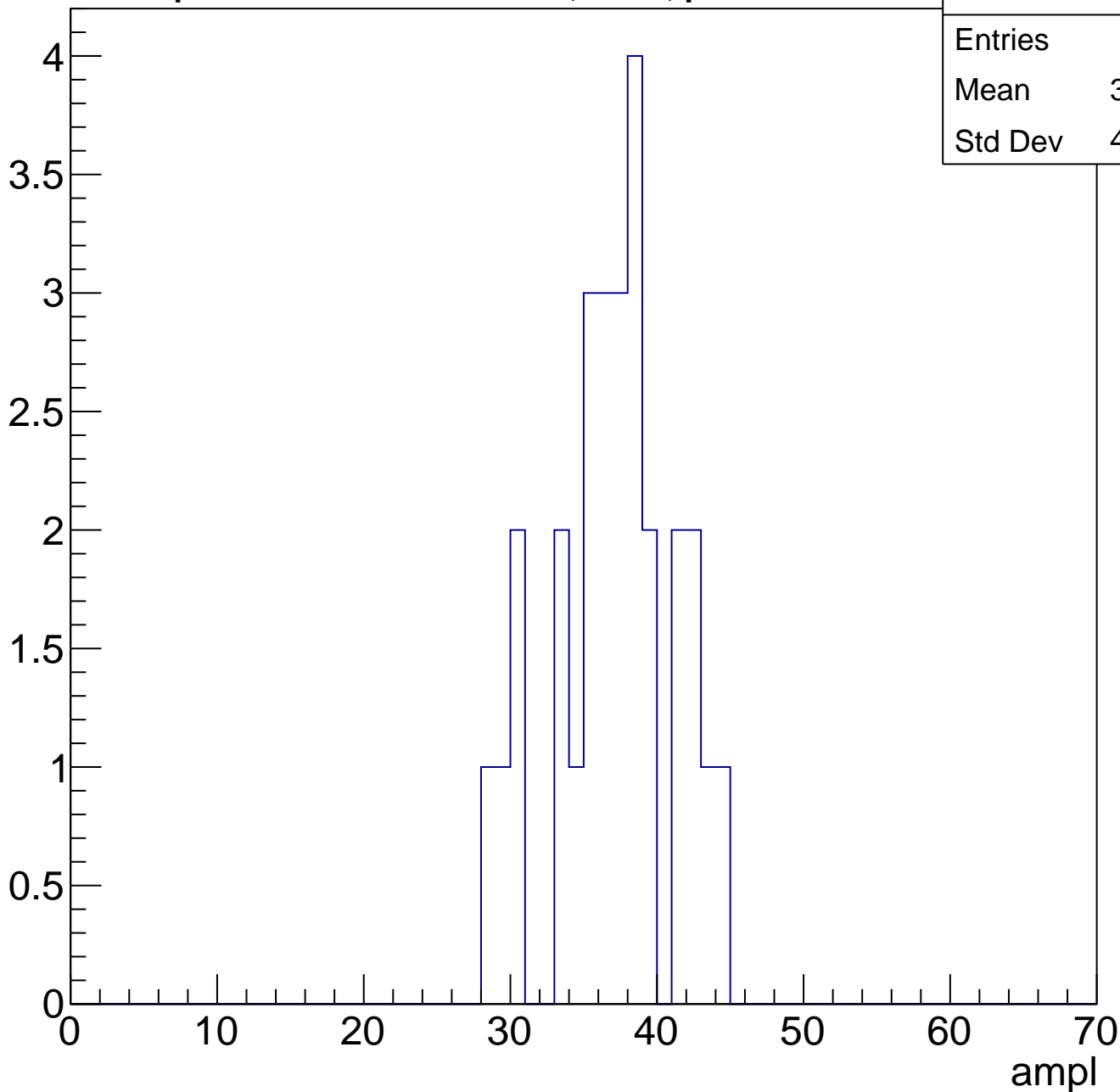
Entries	51
Mean	25.71
Std Dev	10.16



B1L103S, U14-ch1, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry



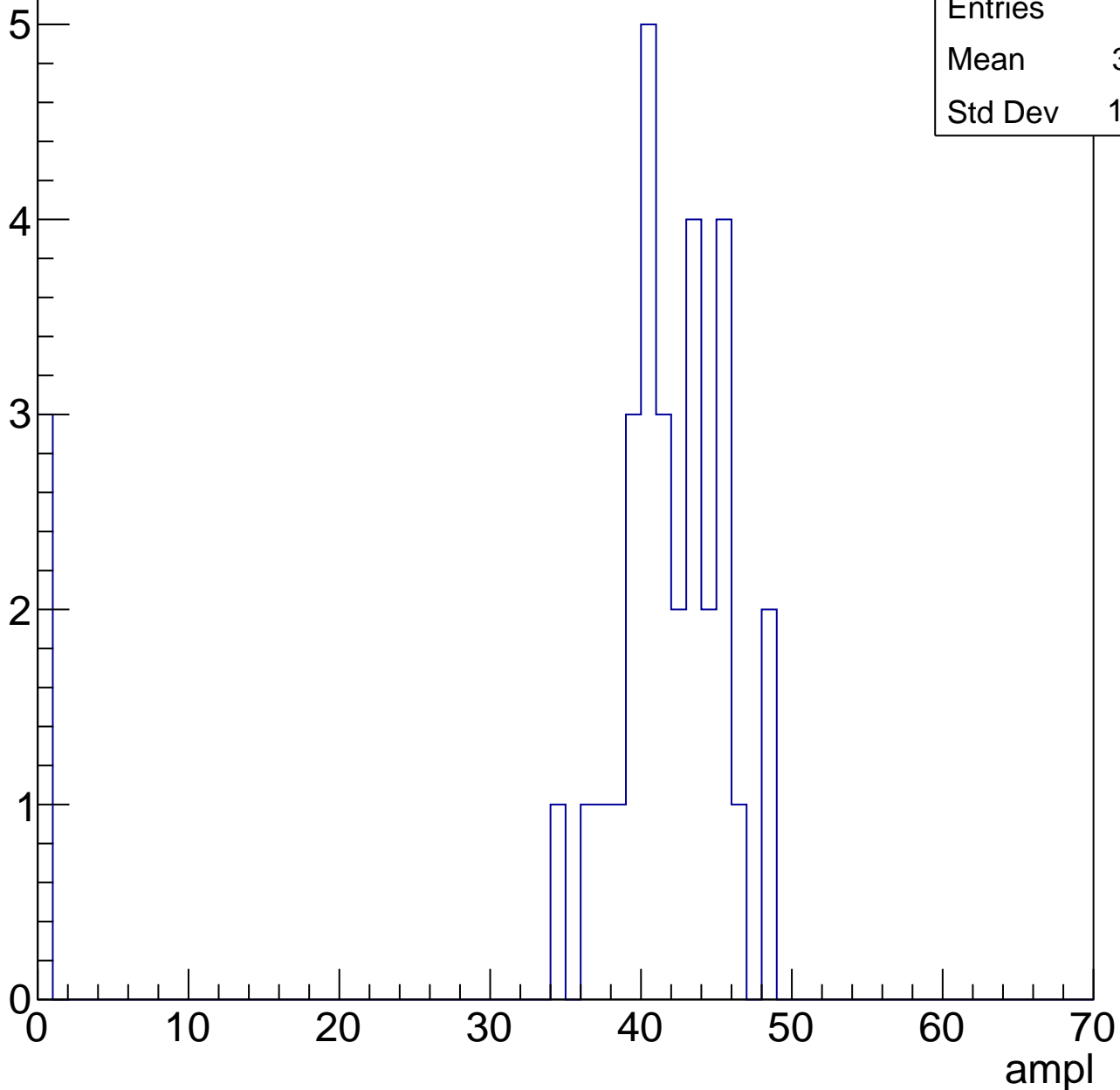
Entries	28
Mean	36.57
Std Dev	4.109

B1L103S, U14-ch1, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	33
Mean	37.91
Std Dev	12.39

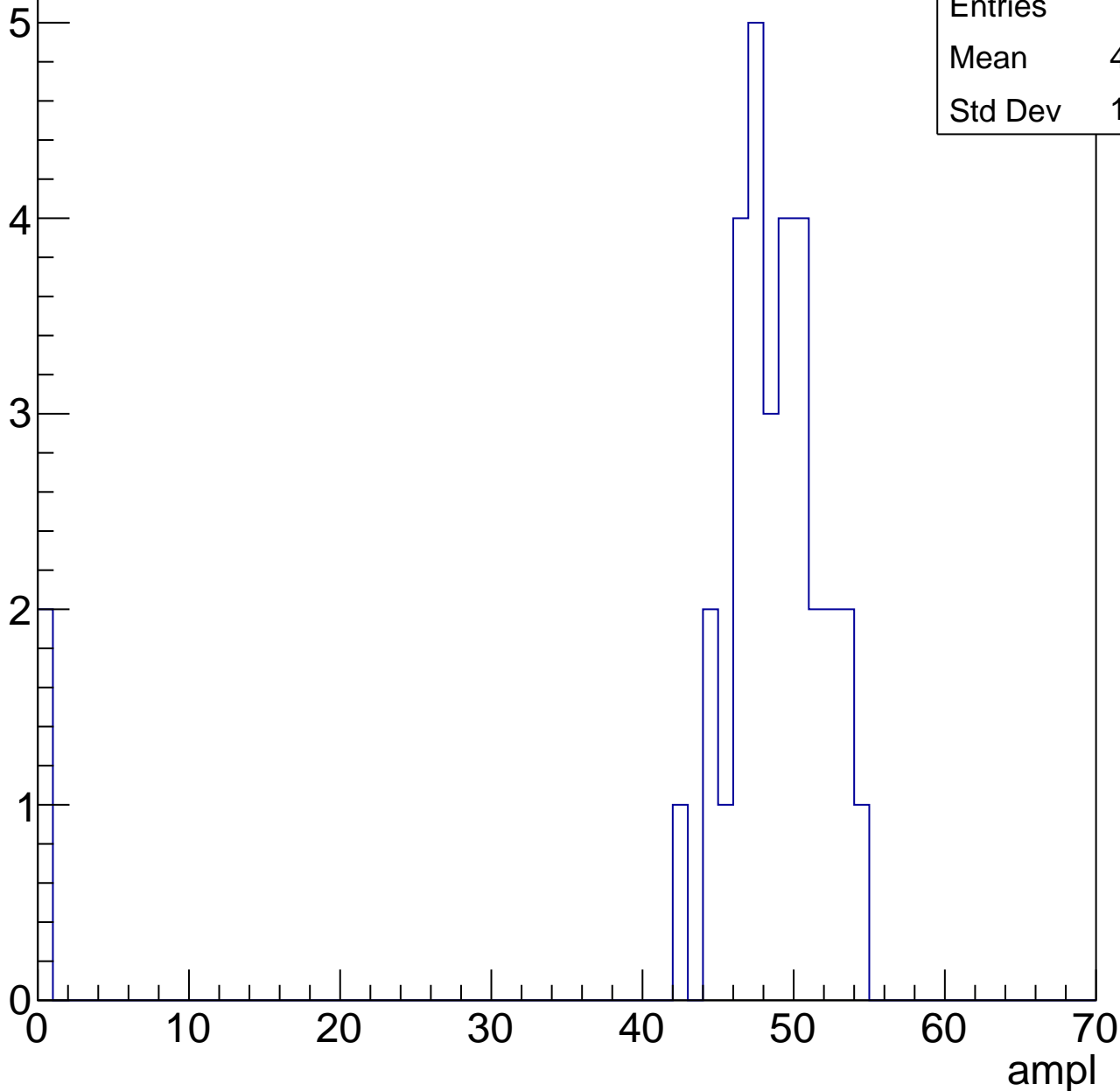


B1L103S, U14-ch1, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	33
Mean	45.45
Std Dev	11.87

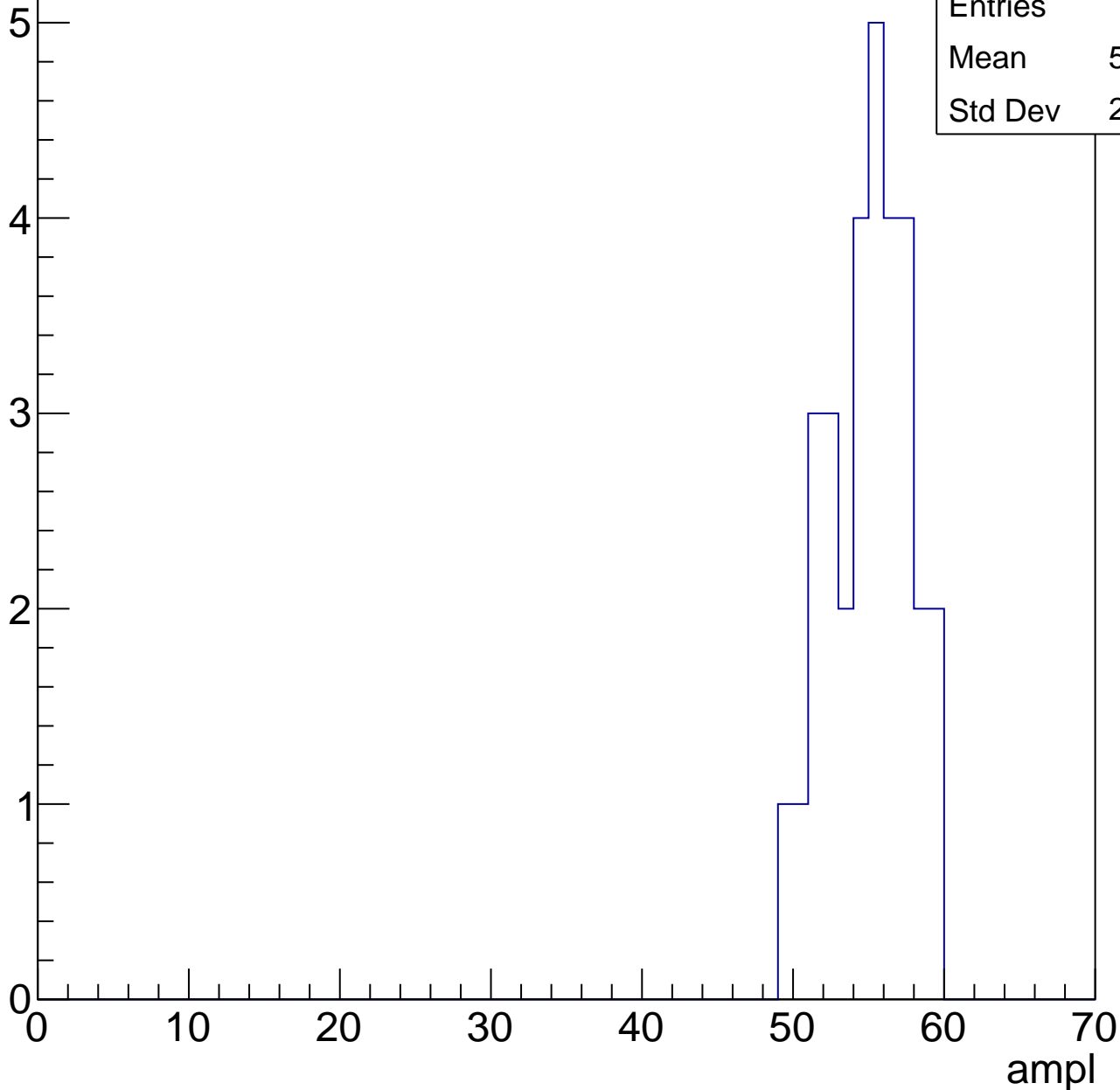


B1L103S, U14-ch1, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	31
Mean	54.55
Std Dev	2.613

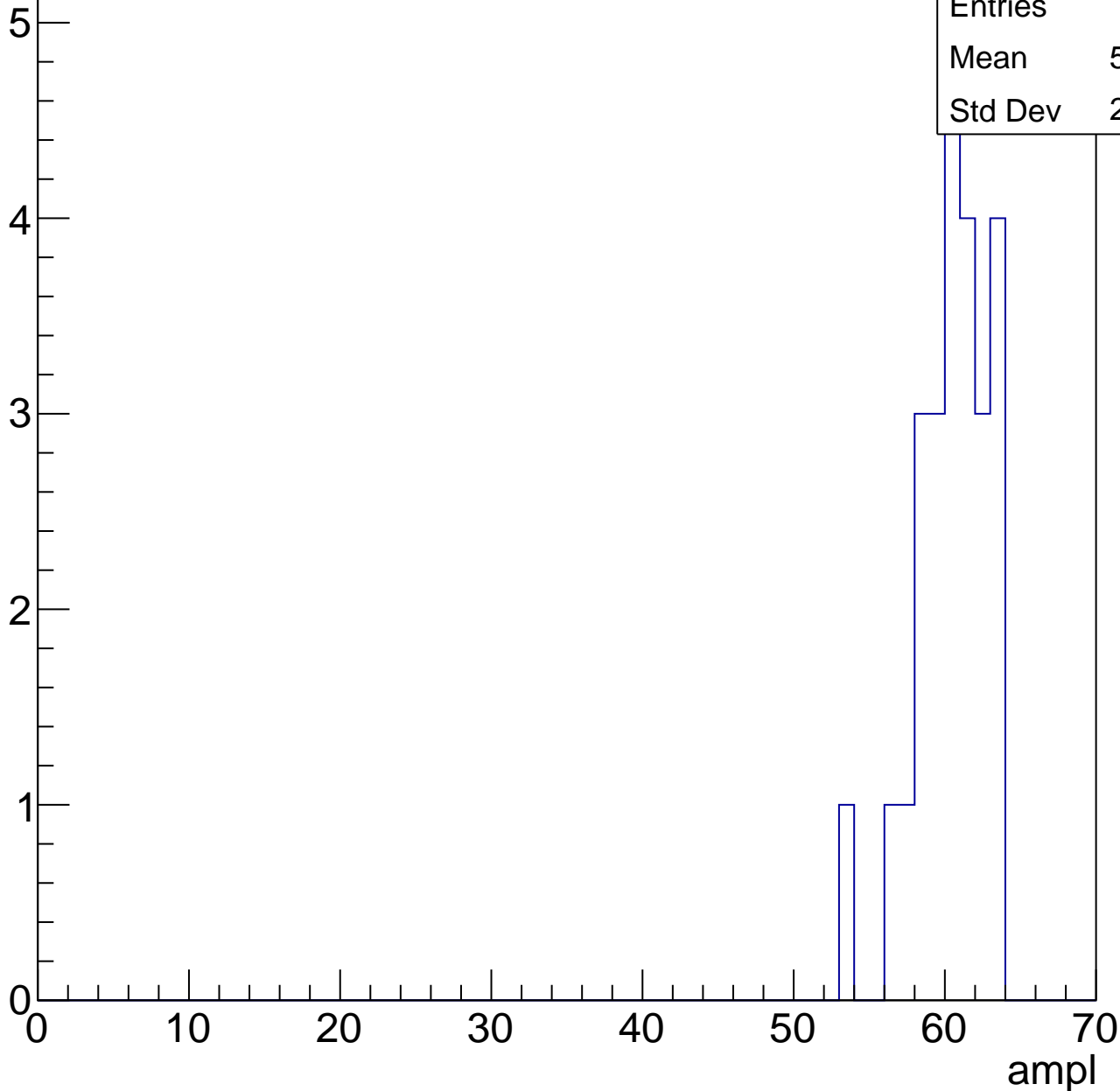


B1L103S, U14-ch1, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	25
Mean	59.96
Std Dev	2.375



B1L103S, U14-ch1, adc6

calib_packv5_041523_1651.root, FC#0, port C2

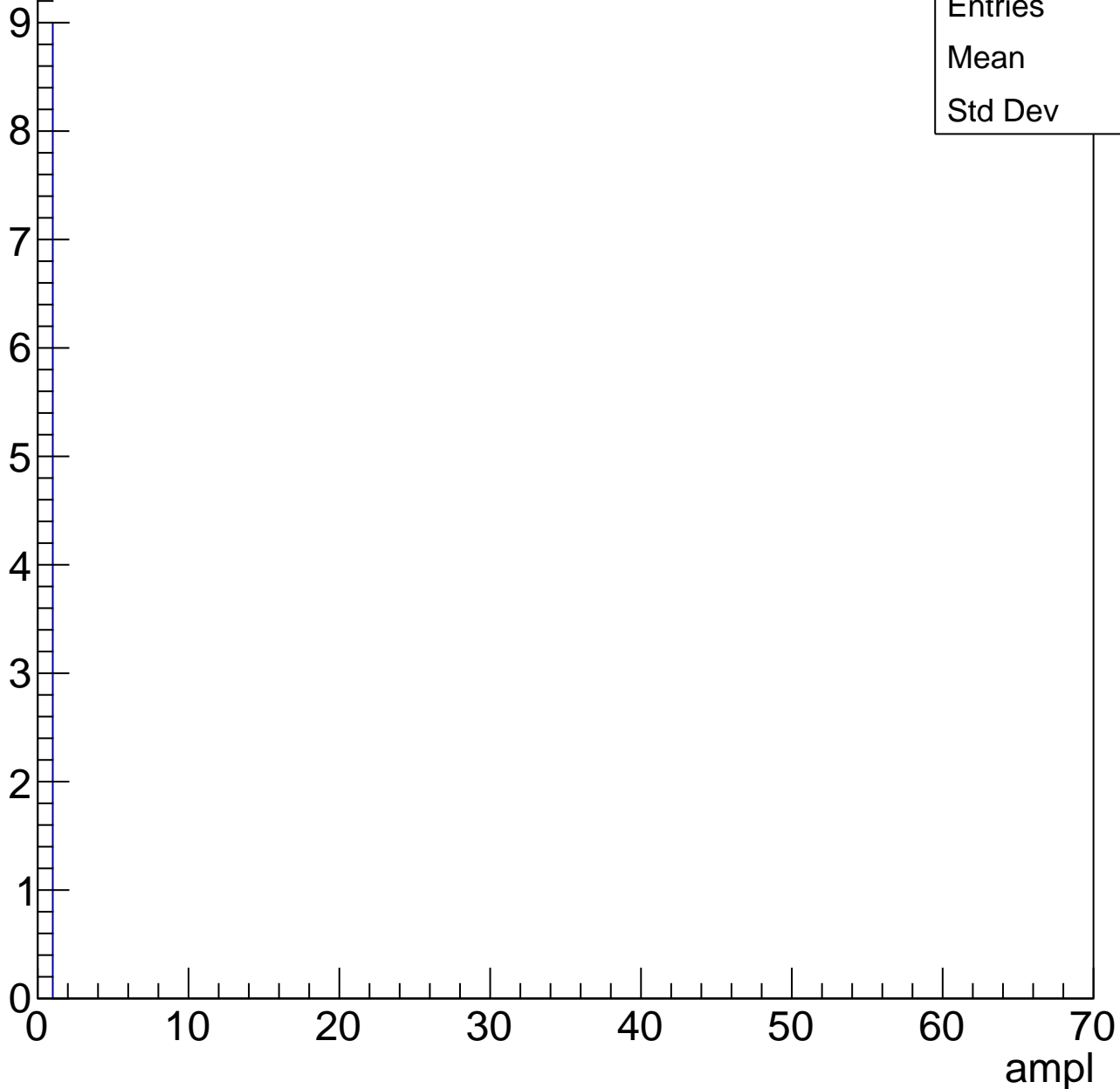
Entry



B1L103S, U14-ch1, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



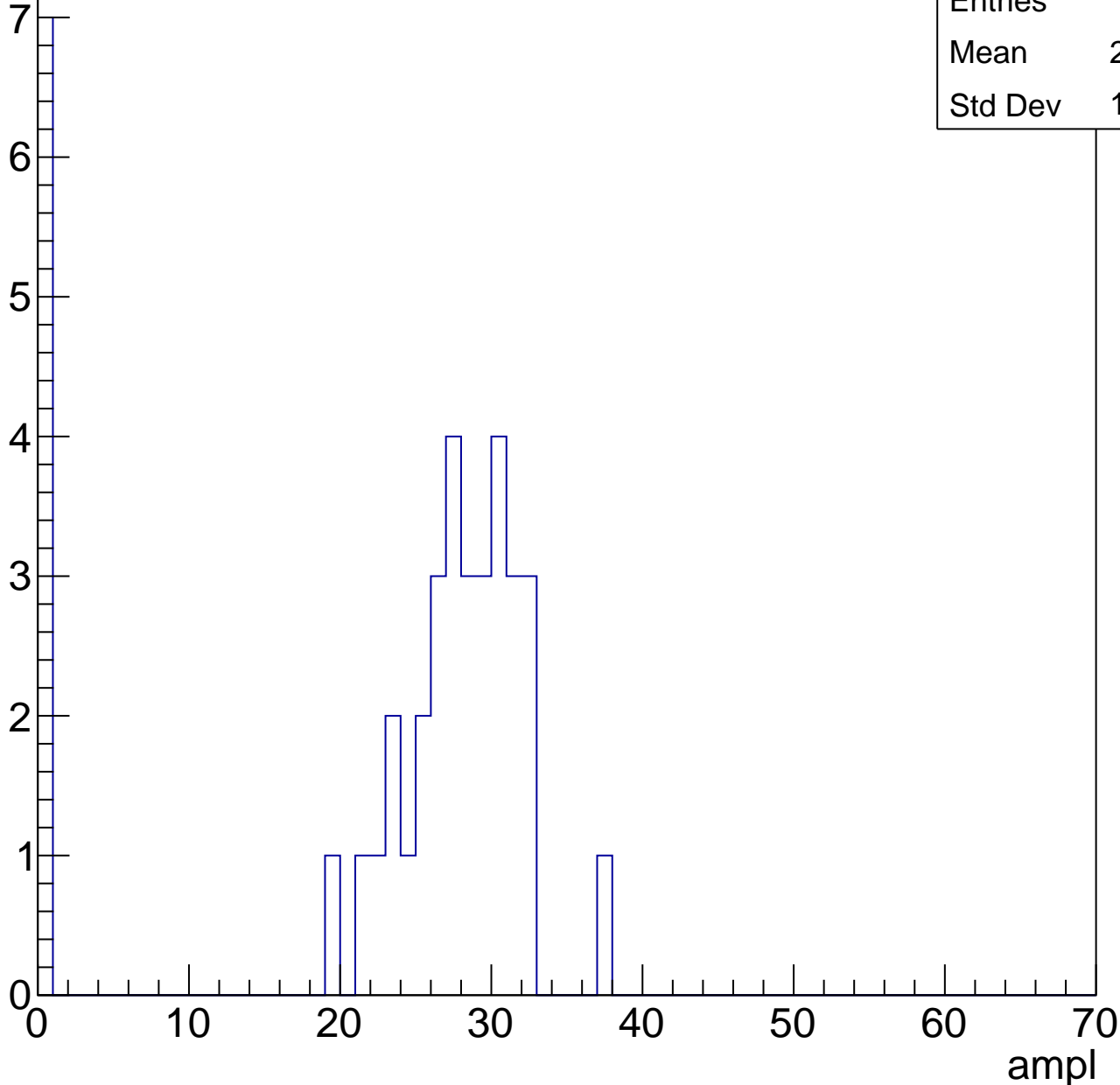
Entries	9
Mean	0
Std Dev	0

B1L103S, U14-ch2, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	22.69
Std Dev	11.13

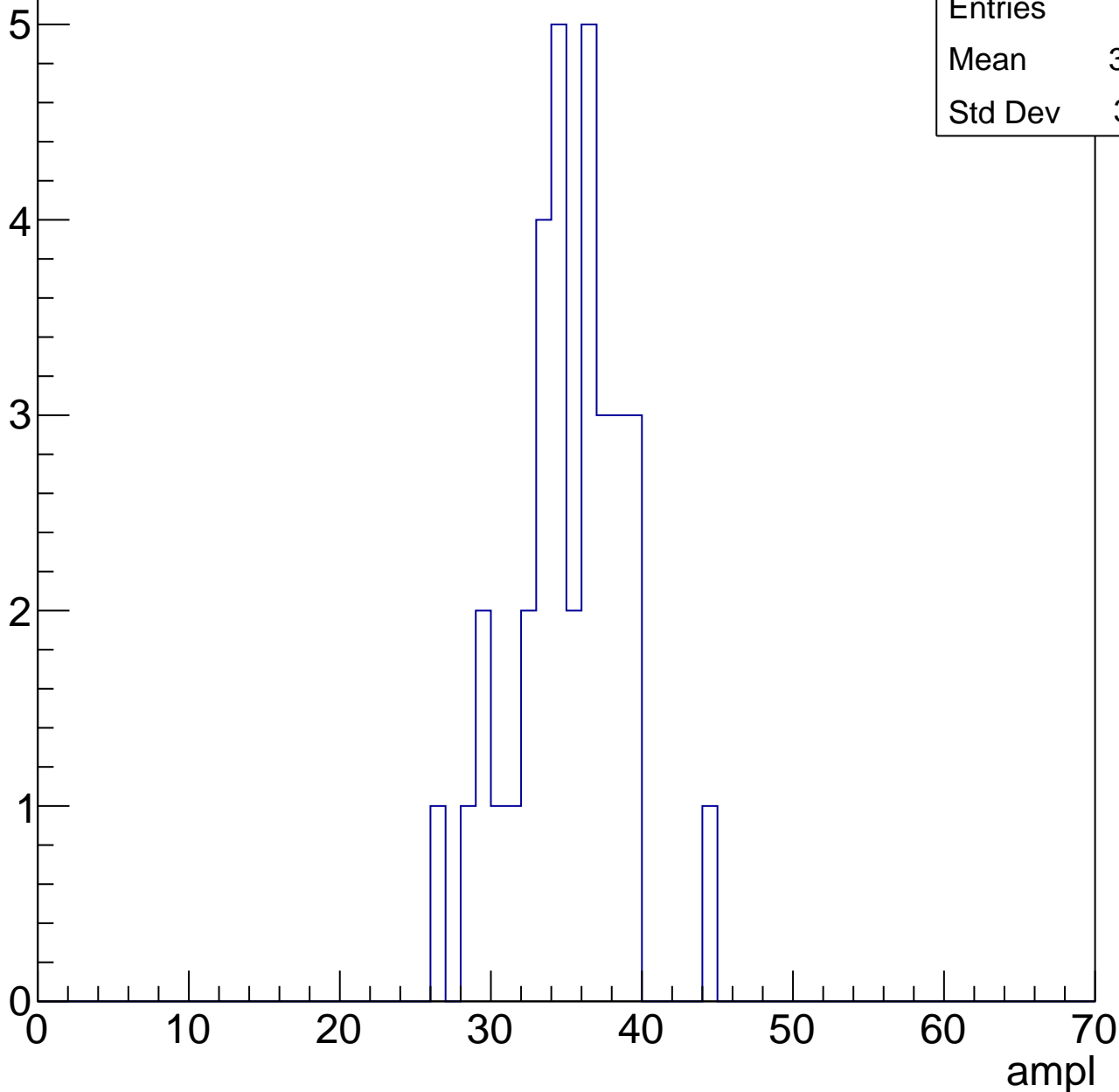


B1L103S, U14-ch2, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	34
Mean	34.56
Std Dev	3.631

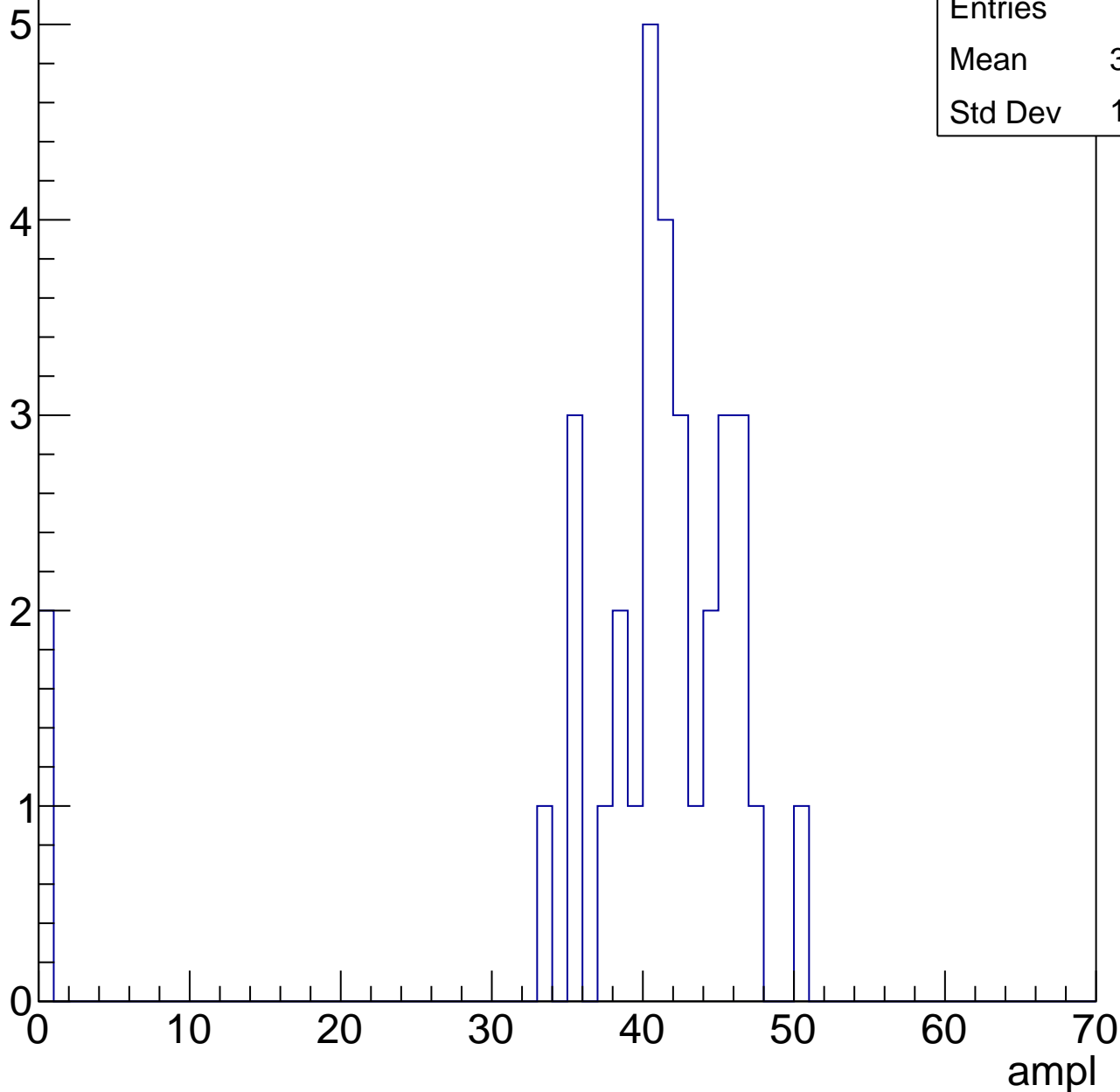


B1L103S, U14-ch2, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	33
Mean	38.82
Std Dev	10.57

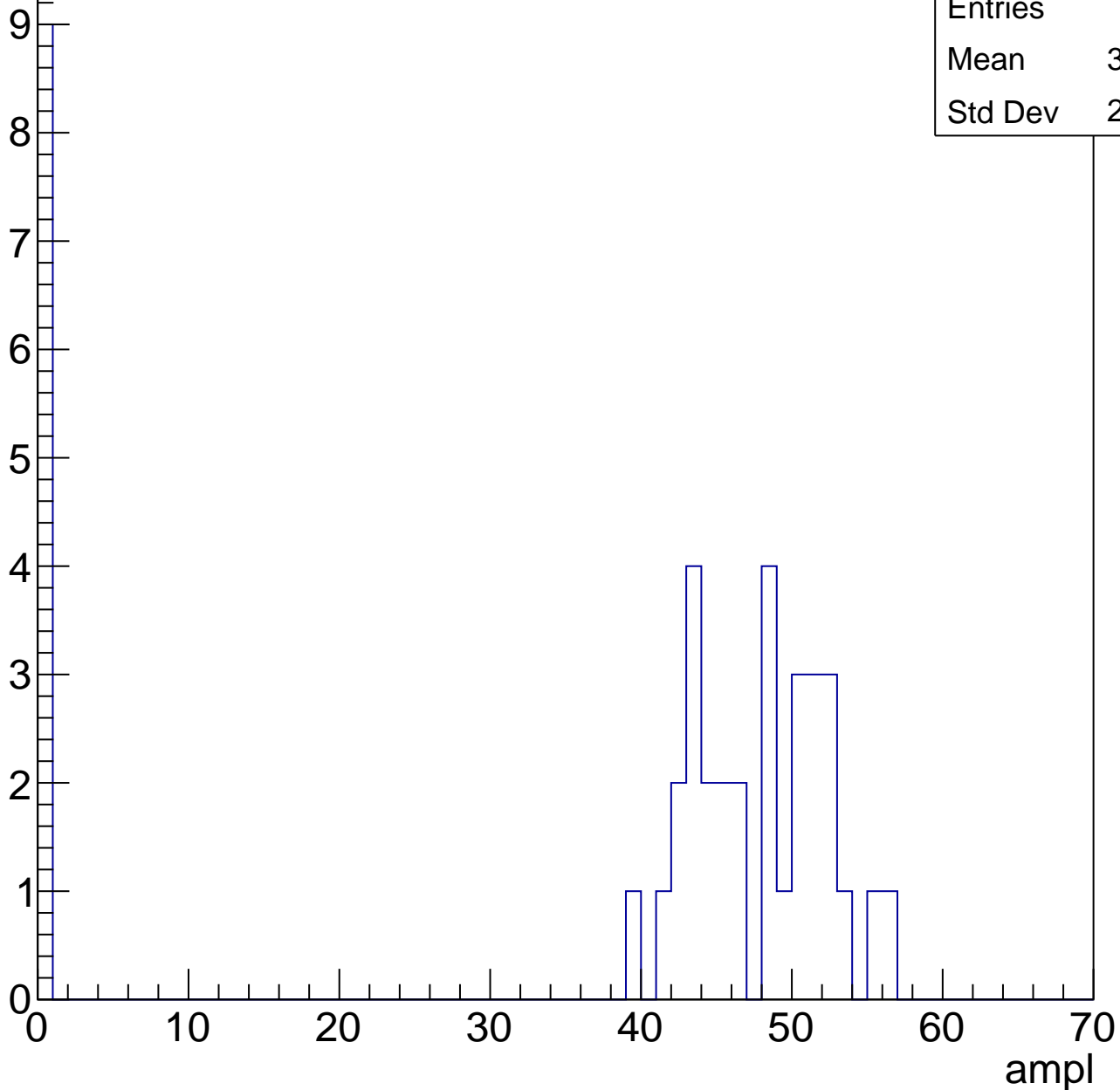


B1L103S, U14-ch2, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

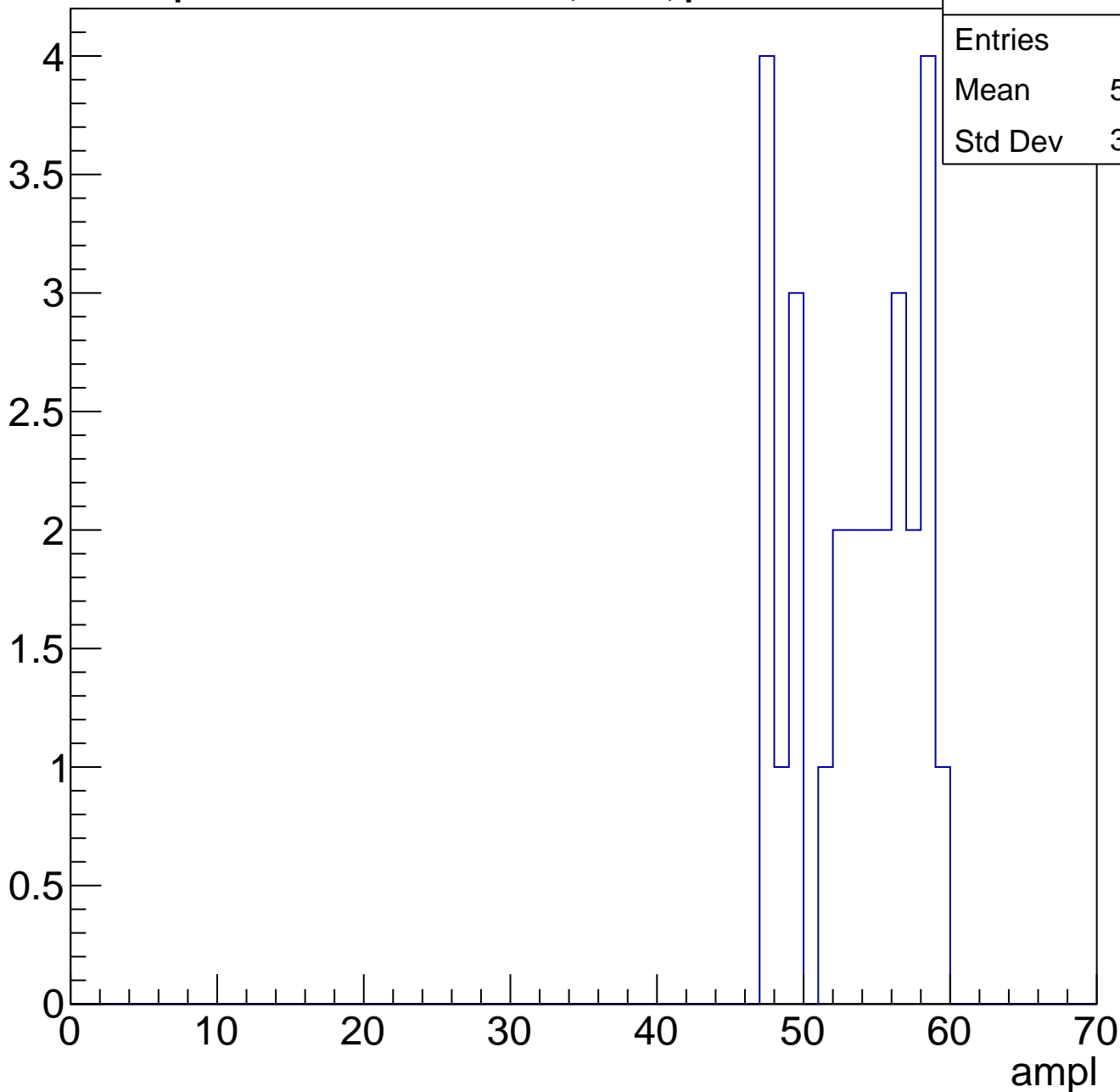
Entries	40
Mean	36.75
Std Dev	20.16



B1L103S, U14-ch2, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



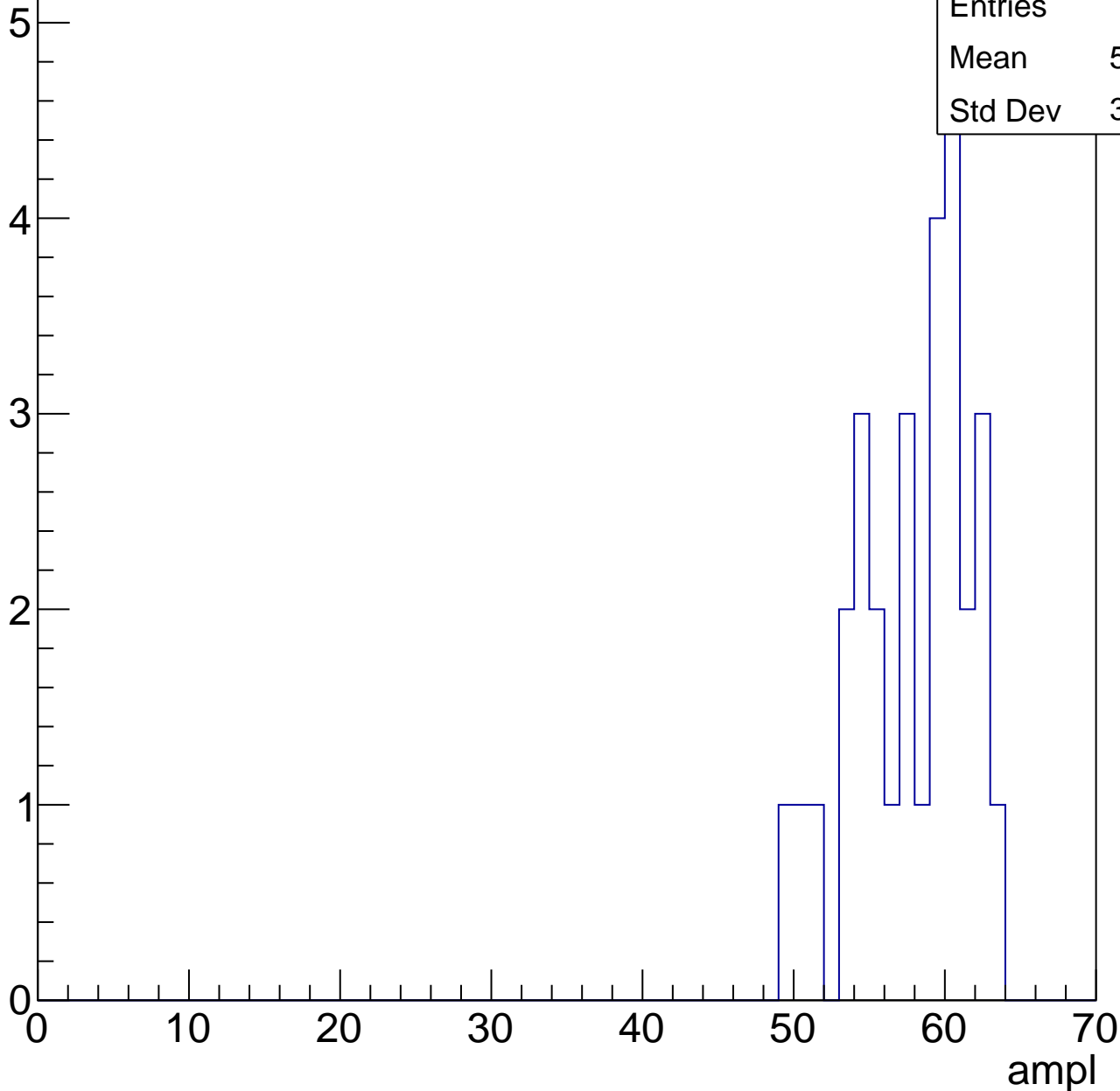
Entries	27
Mean	53.15
Std Dev	3.979

B1L103S, U14-ch2, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

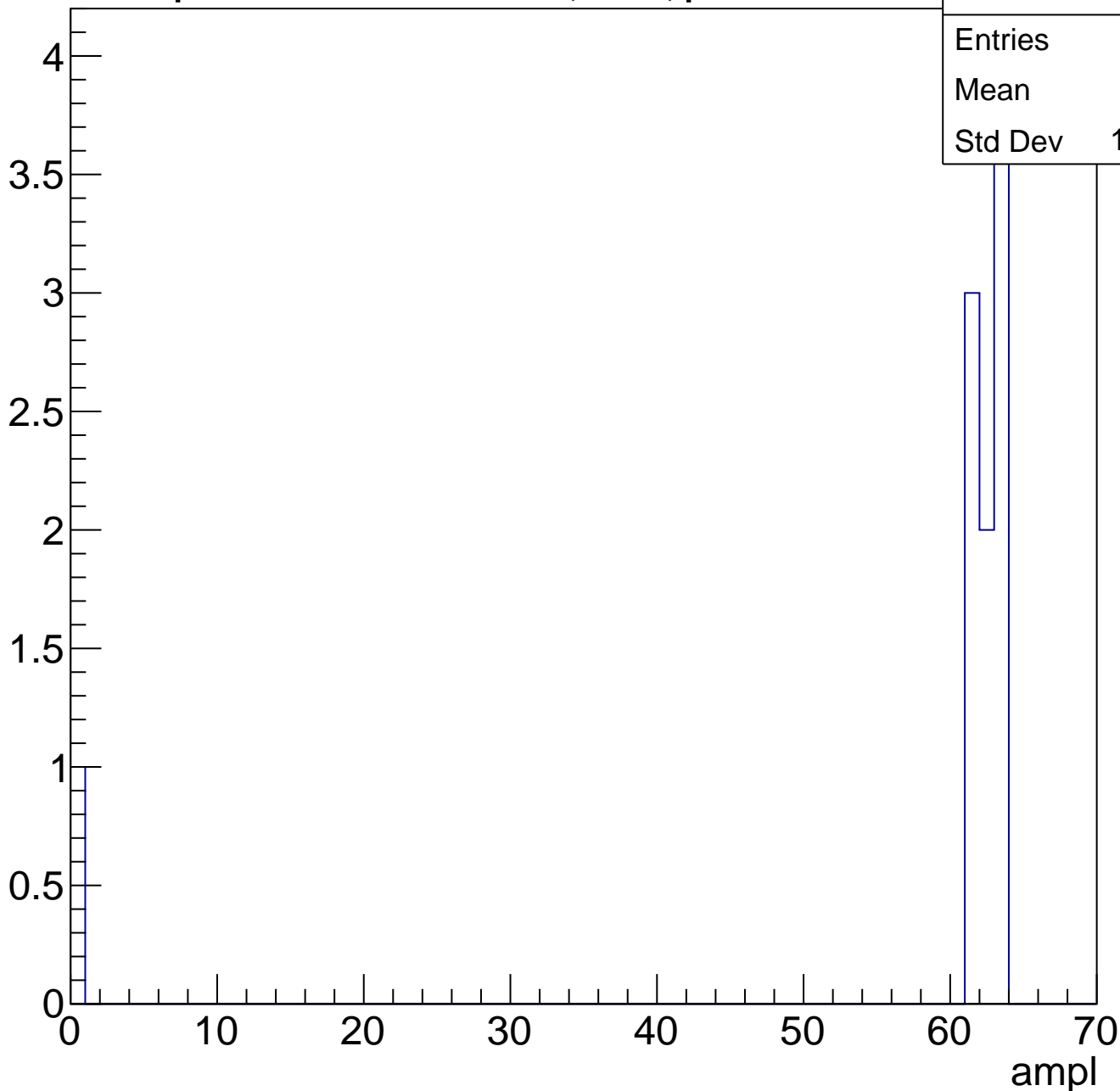
Entries	30
Mean	57.33
Std Dev	3.736



B1L103S, U14-ch2, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

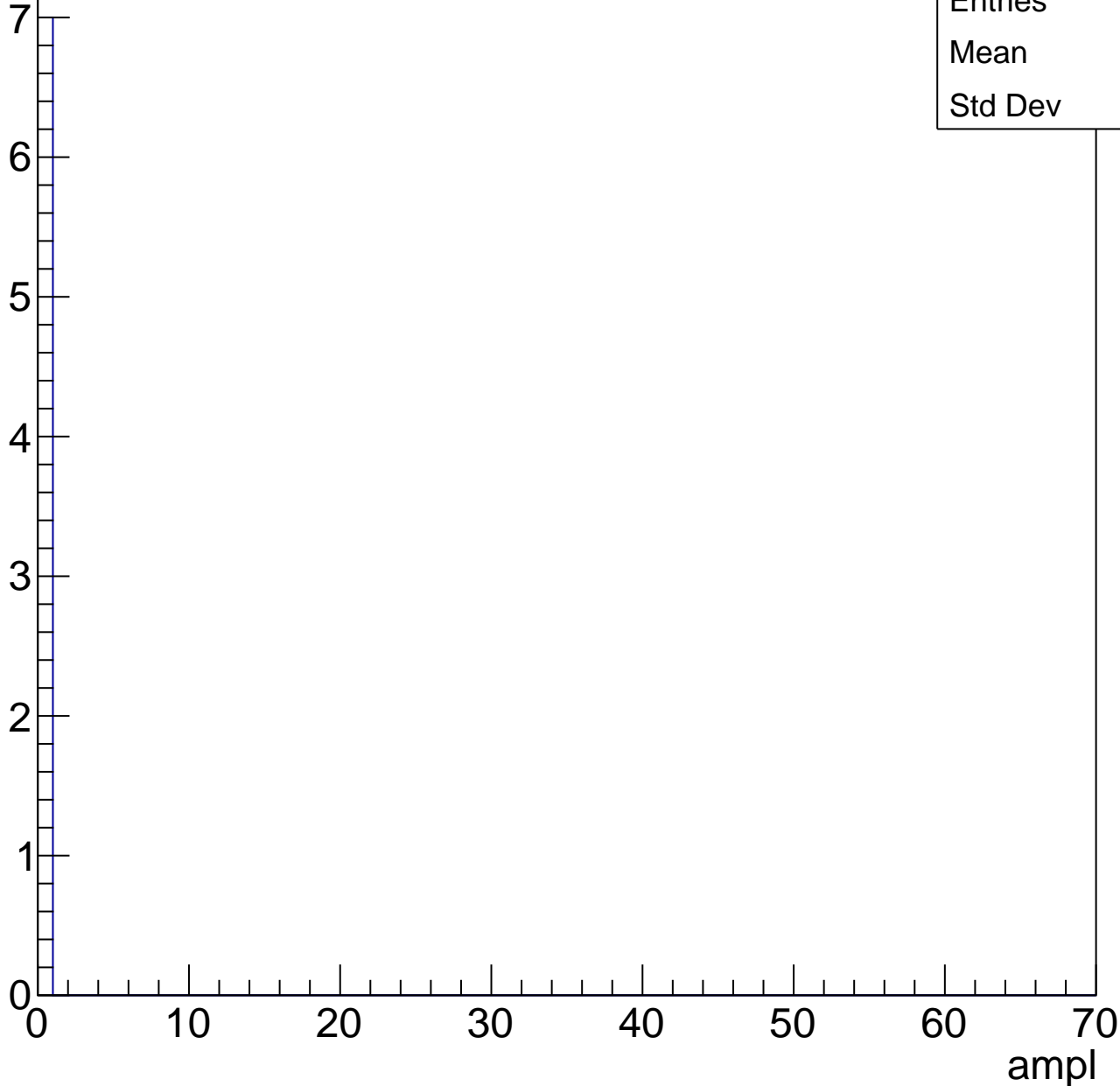


B1L103S, U14-ch2, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	7
Mean	0
Std Dev	0

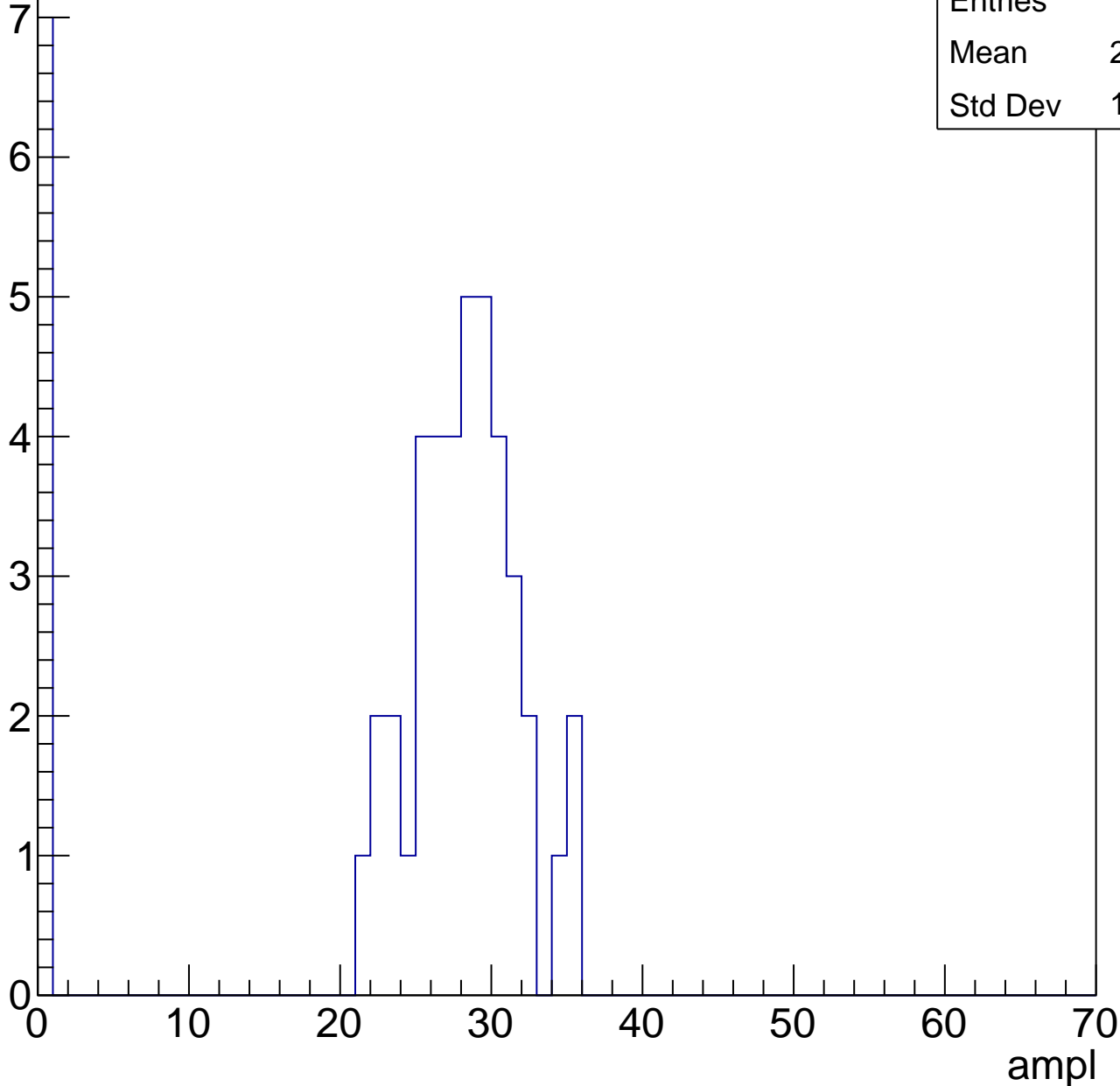


B1L103S, U14-ch3, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	47
Mean	23.68
Std Dev	10.38

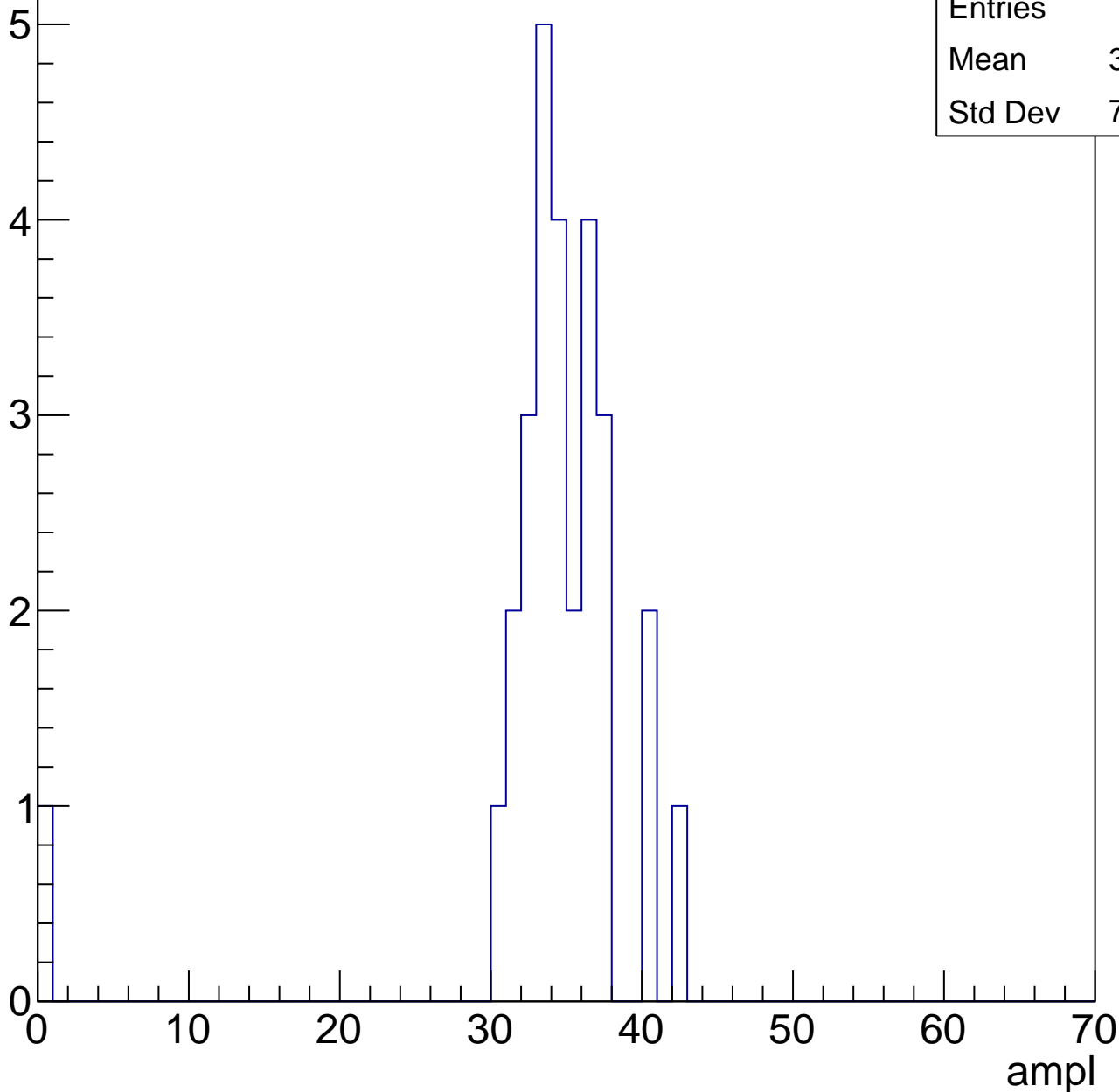


B1L103S, U14-ch3, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	28
Mean	33.43
Std Dev	7.017

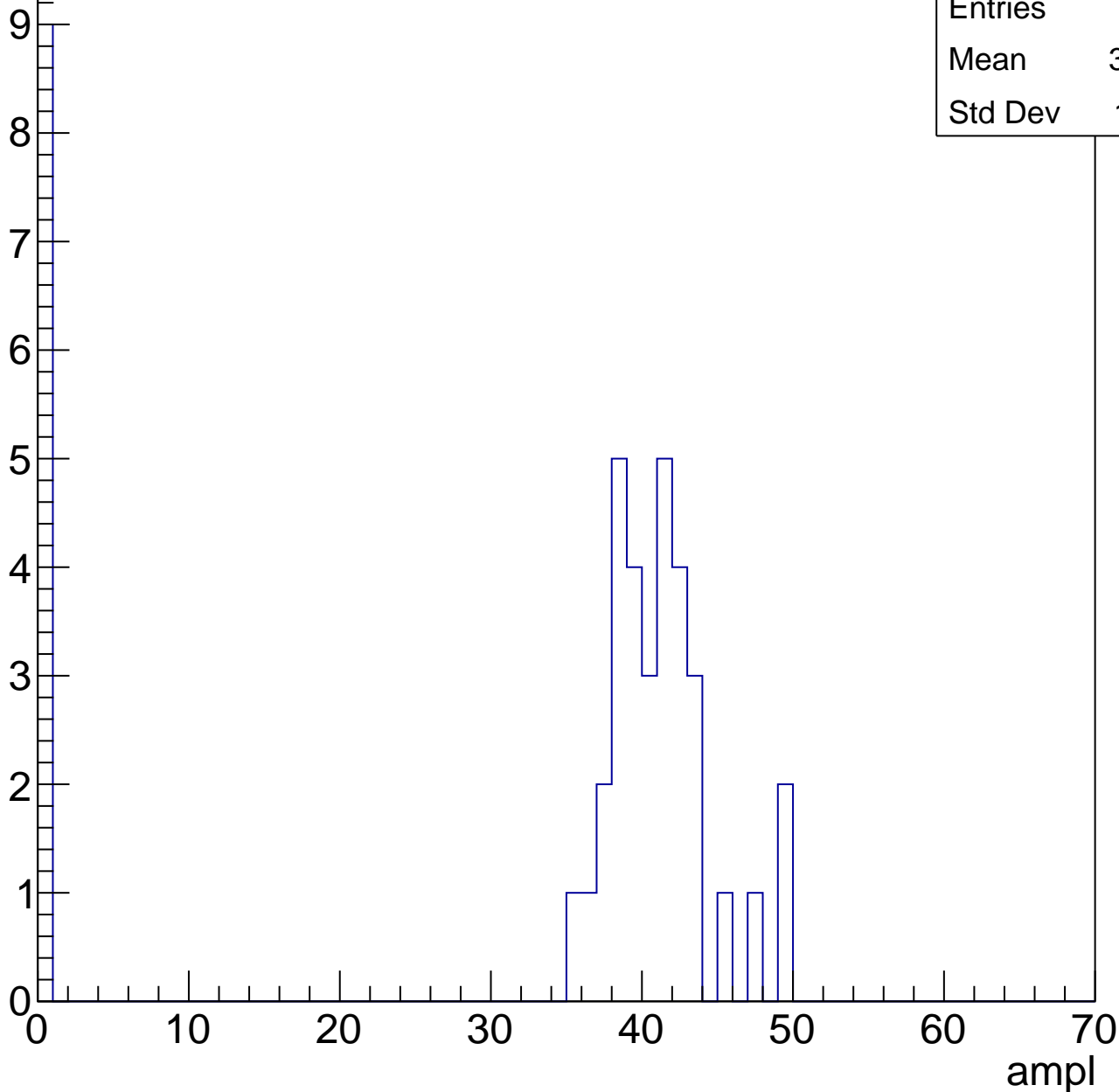


B1L103S, U14-ch3, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	41
Mean	31.78
Std Dev	17.11

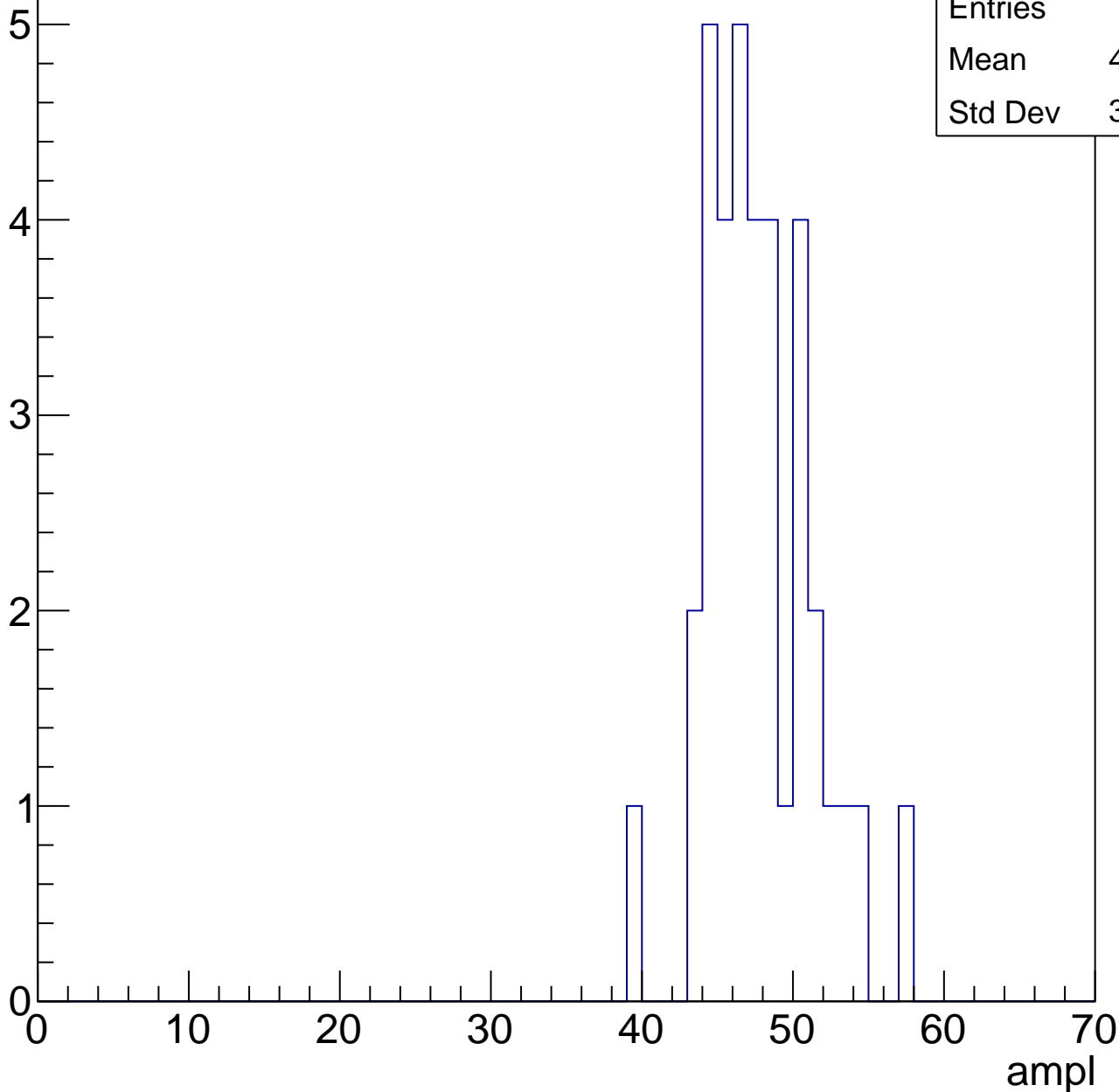


B1L103S, U14-ch3, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

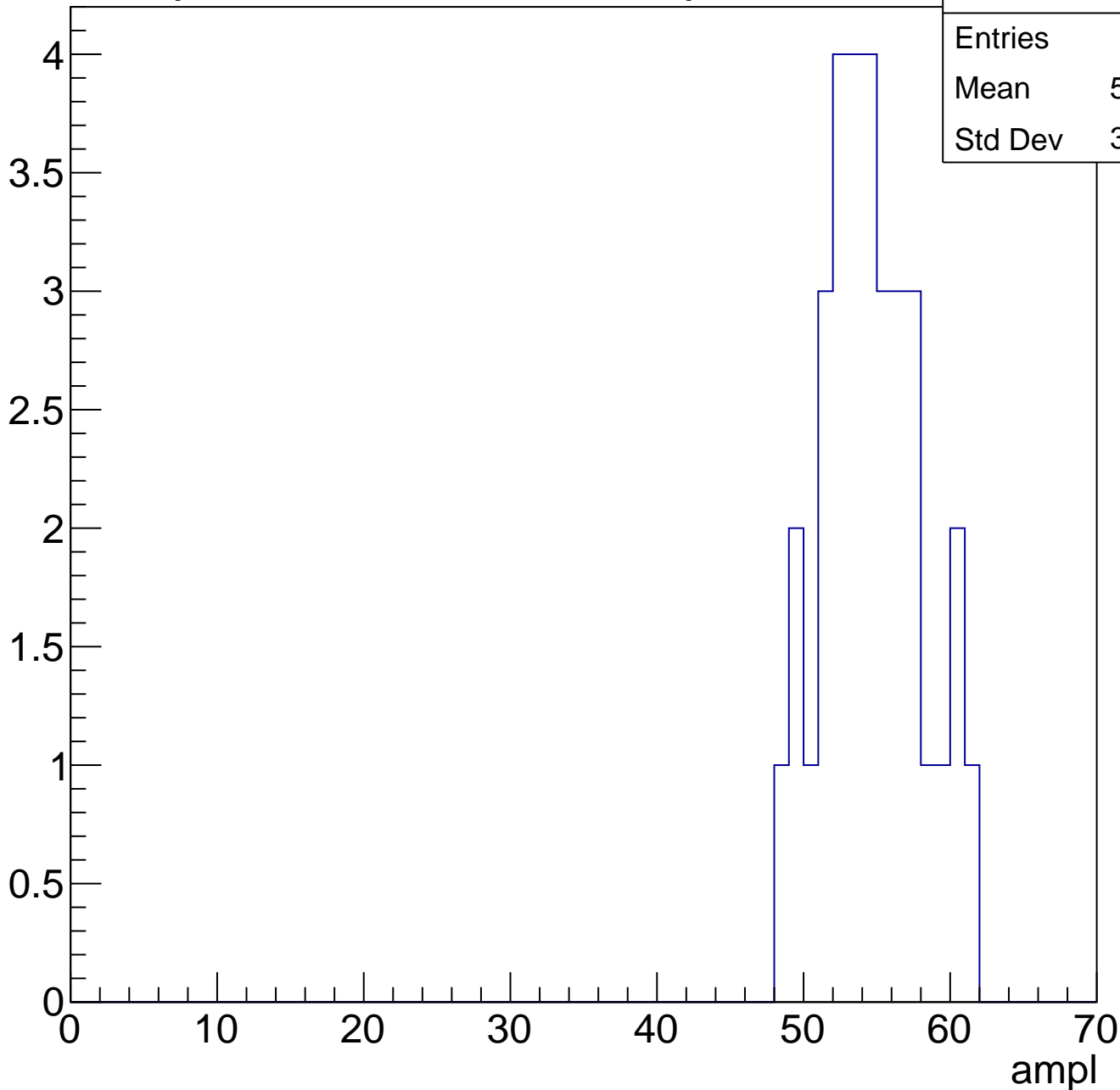
Entries	36
Mean	47.28
Std Dev	3.517



B1L103S, U14-ch3, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

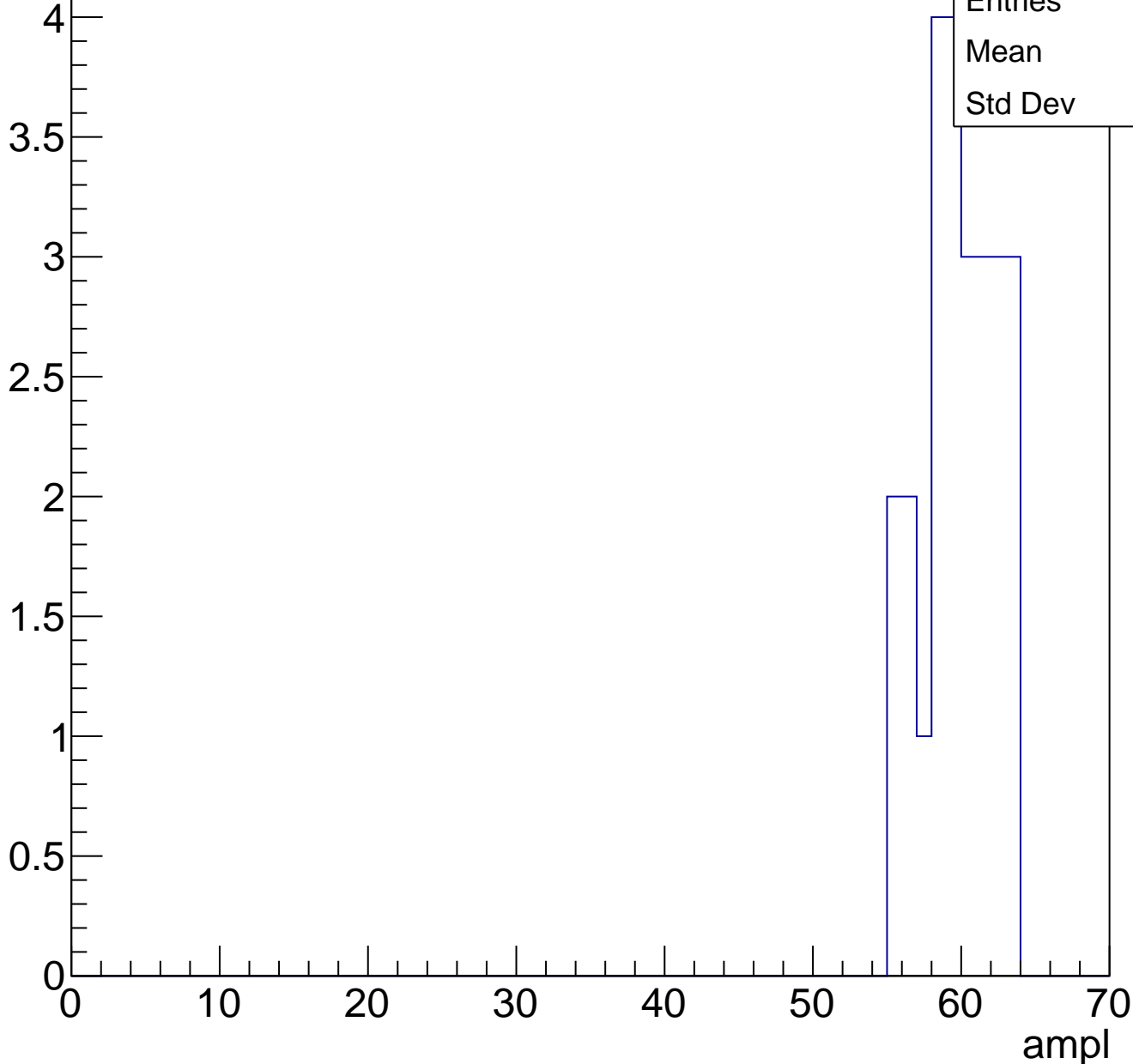


Entries	33
Mean	54.15
Std Dev	3.267

B1L103S, U14-ch3, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch3, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	5
Mean	62.2
Std Dev	0.7483

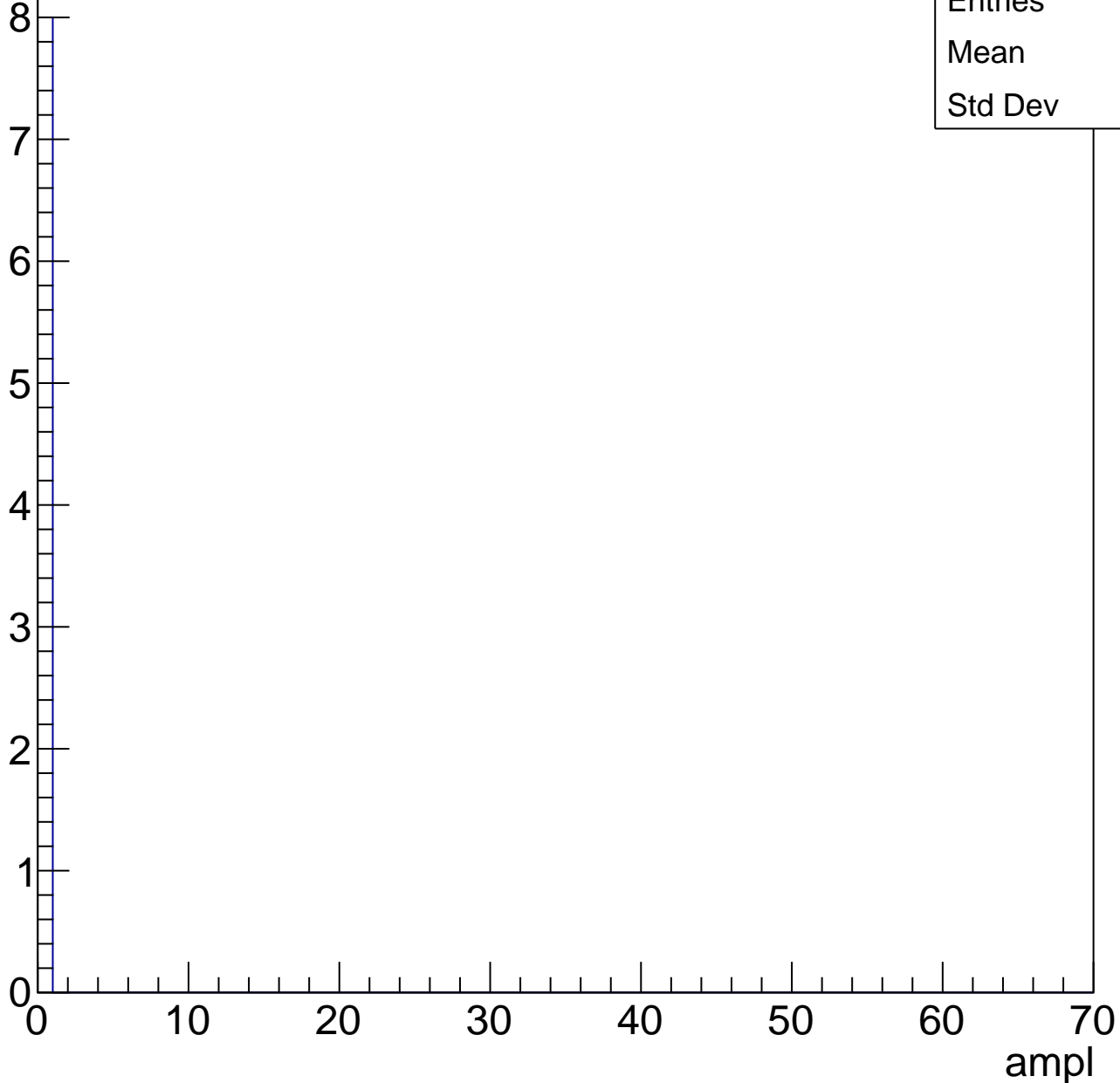
ampl

0 10 20 30 40 50 60 70

B1L103S, U14-ch3, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



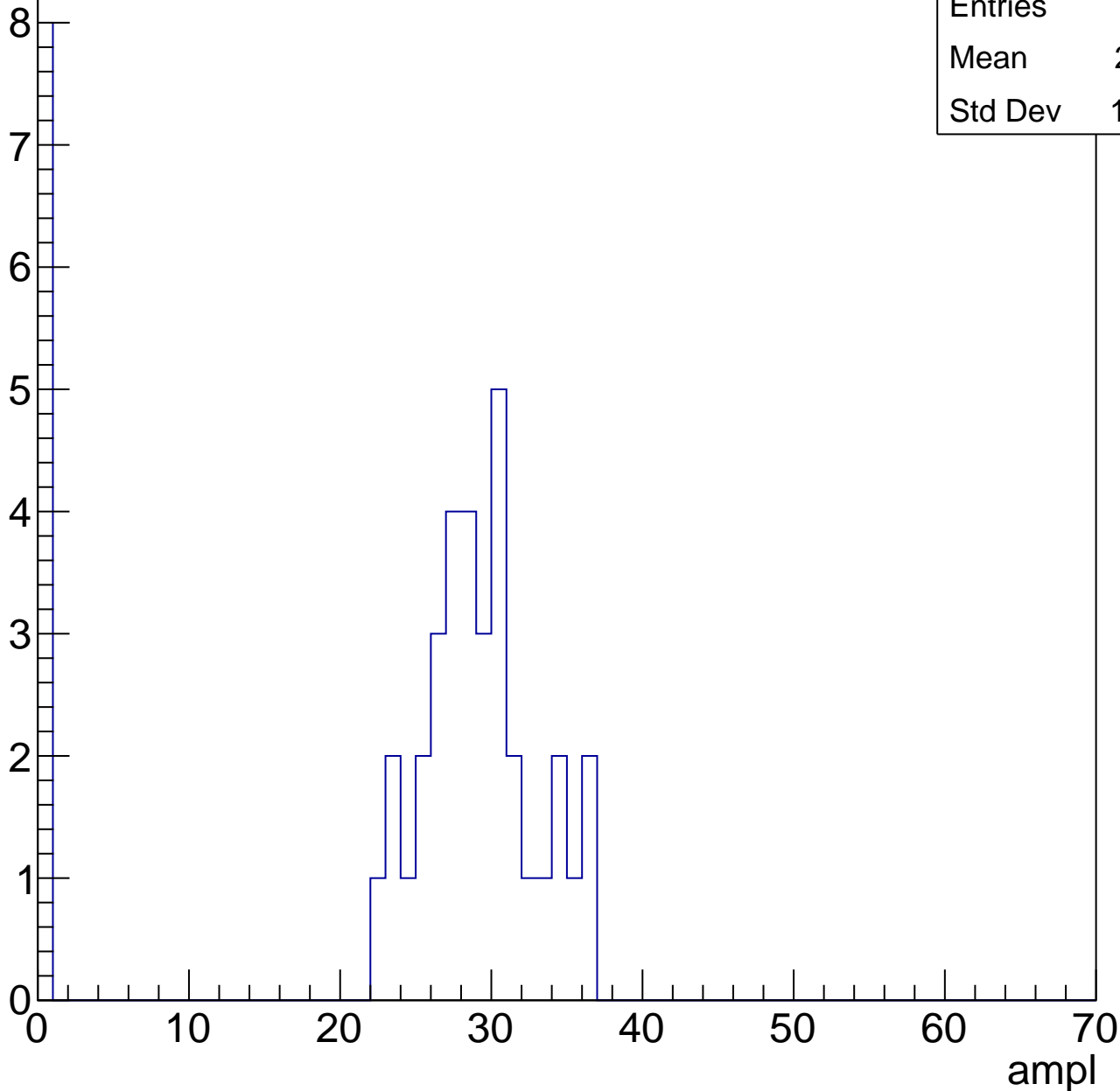
Entries	8
Mean	0
Std Dev	0

B1L103S, U14-ch4, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

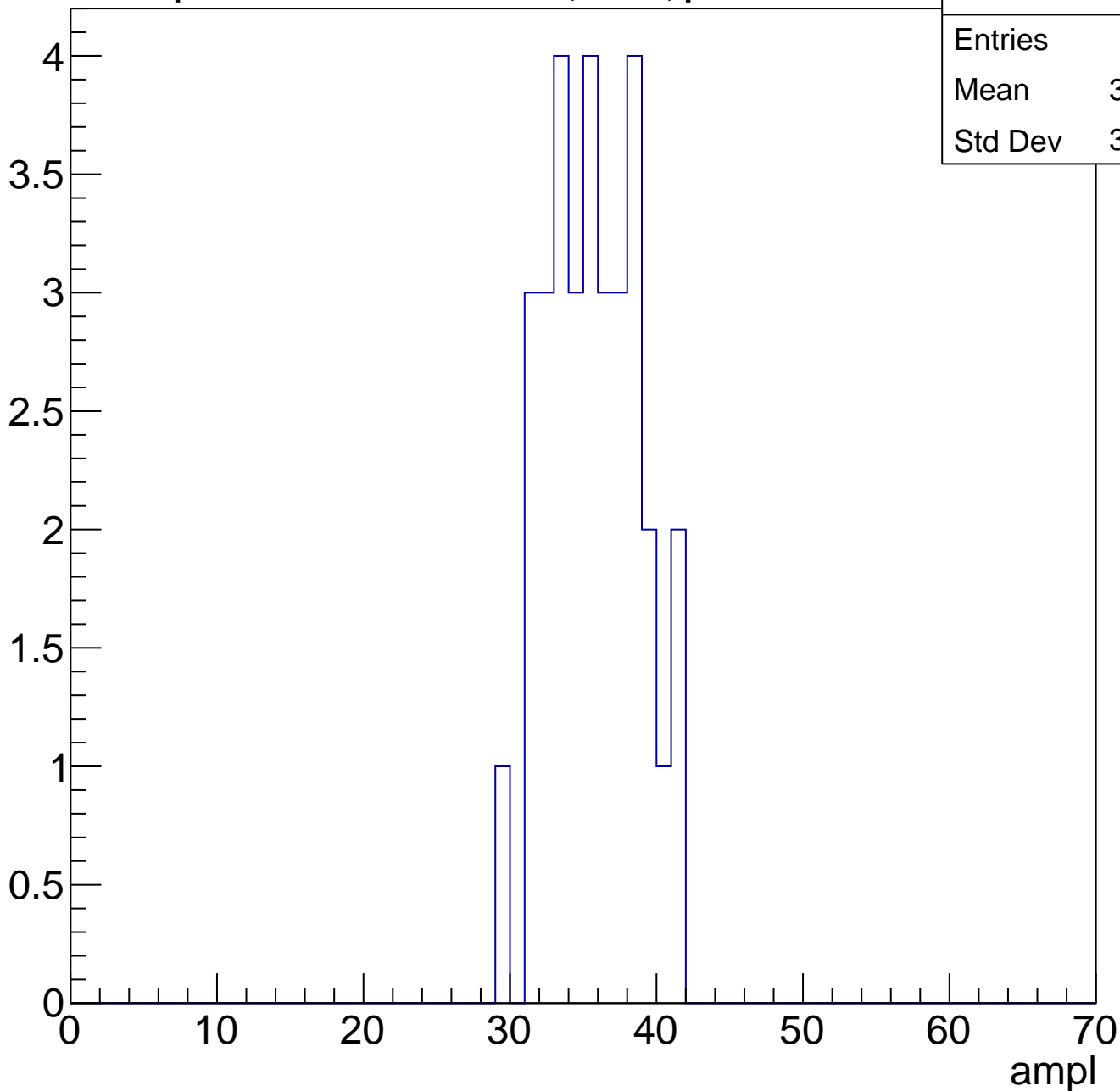
Entries	42
Mean	23.31
Std Dev	11.77



B1L103S, U14-ch4, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

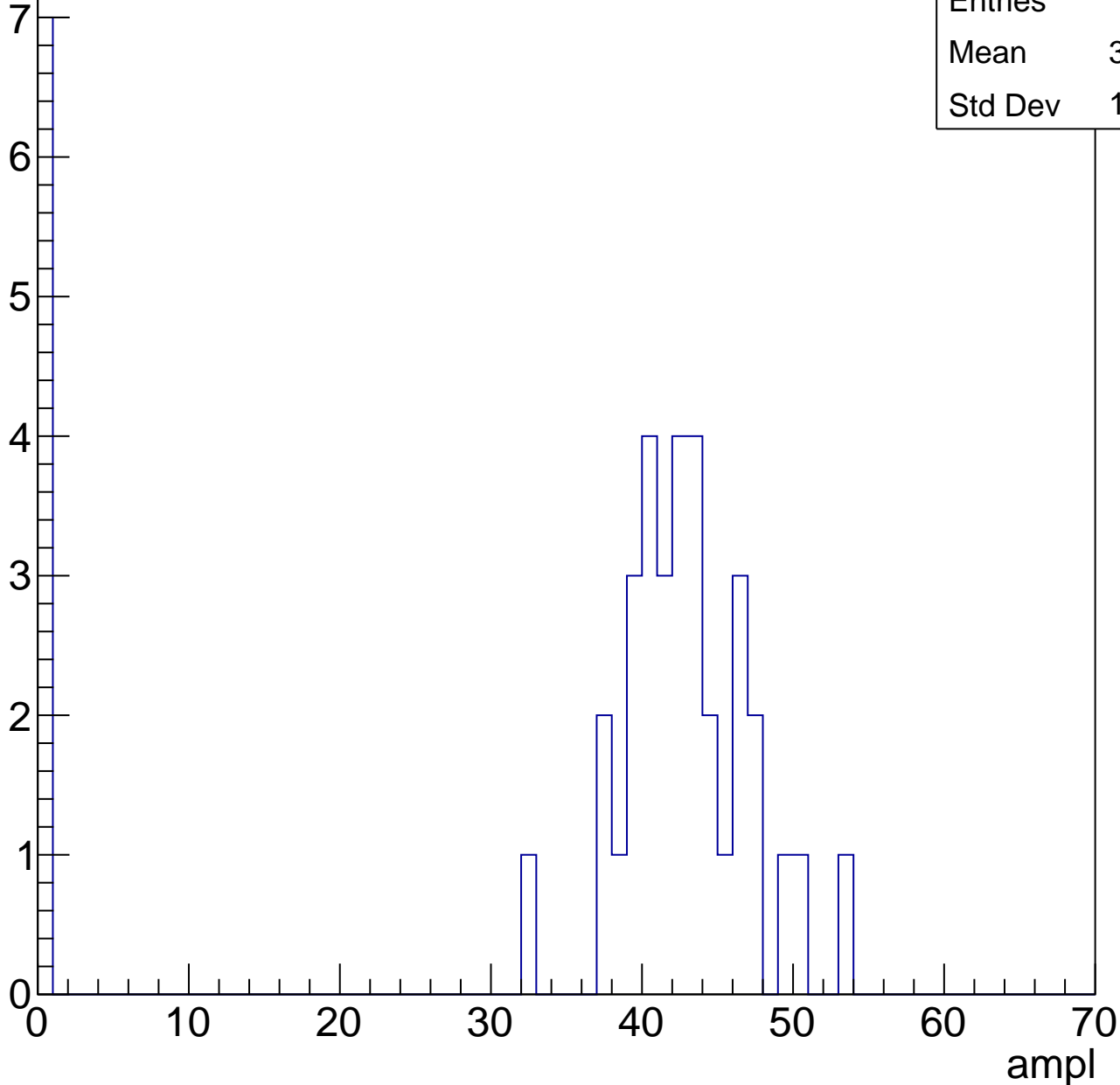


B1L103S, U14-ch4, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	35.02
Std Dev	16.56

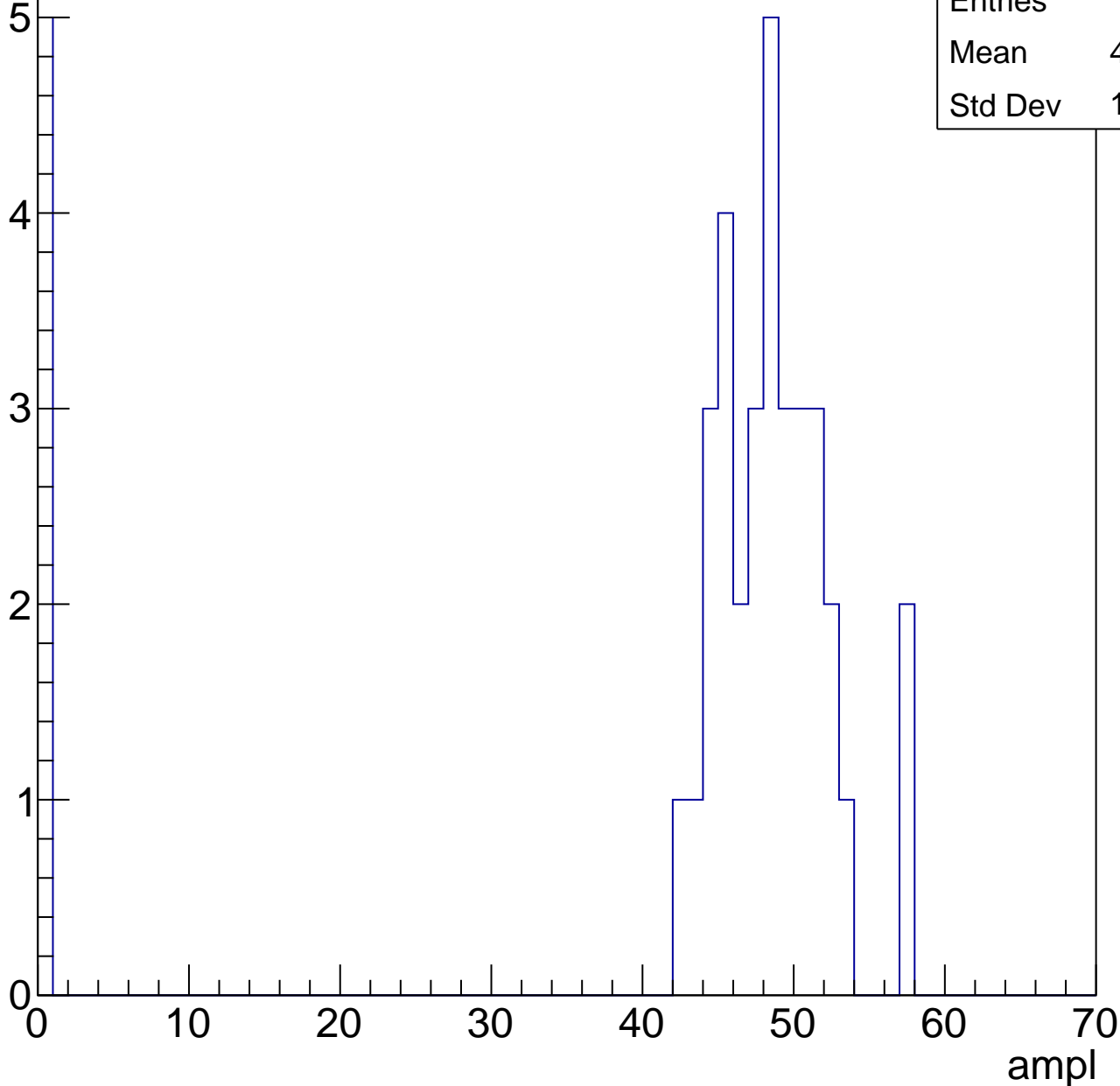


B1L103S, U14-ch4, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

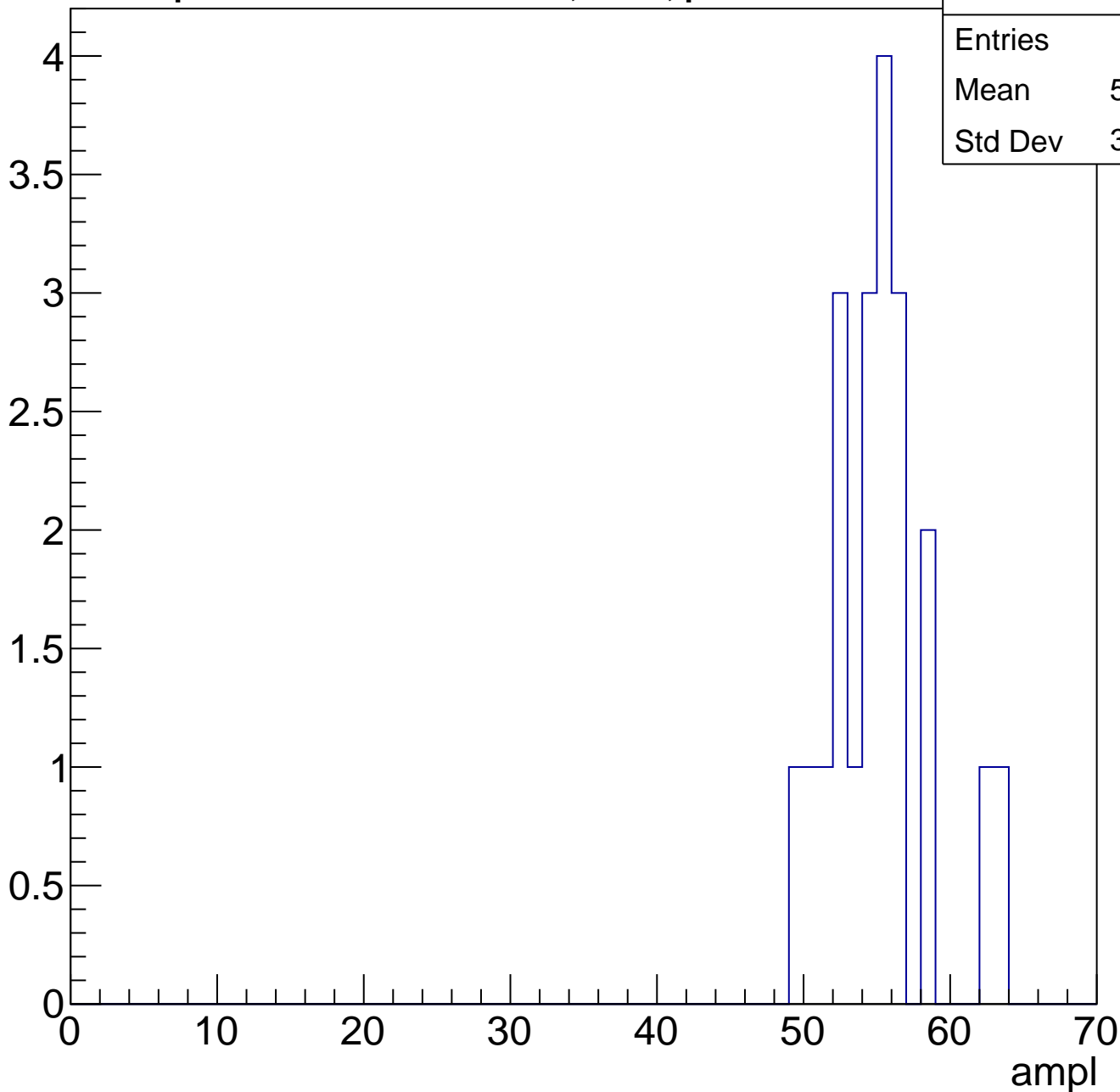
Entries	38
Mean	41.87
Std Dev	16.63



B1L103S, U14-ch4, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

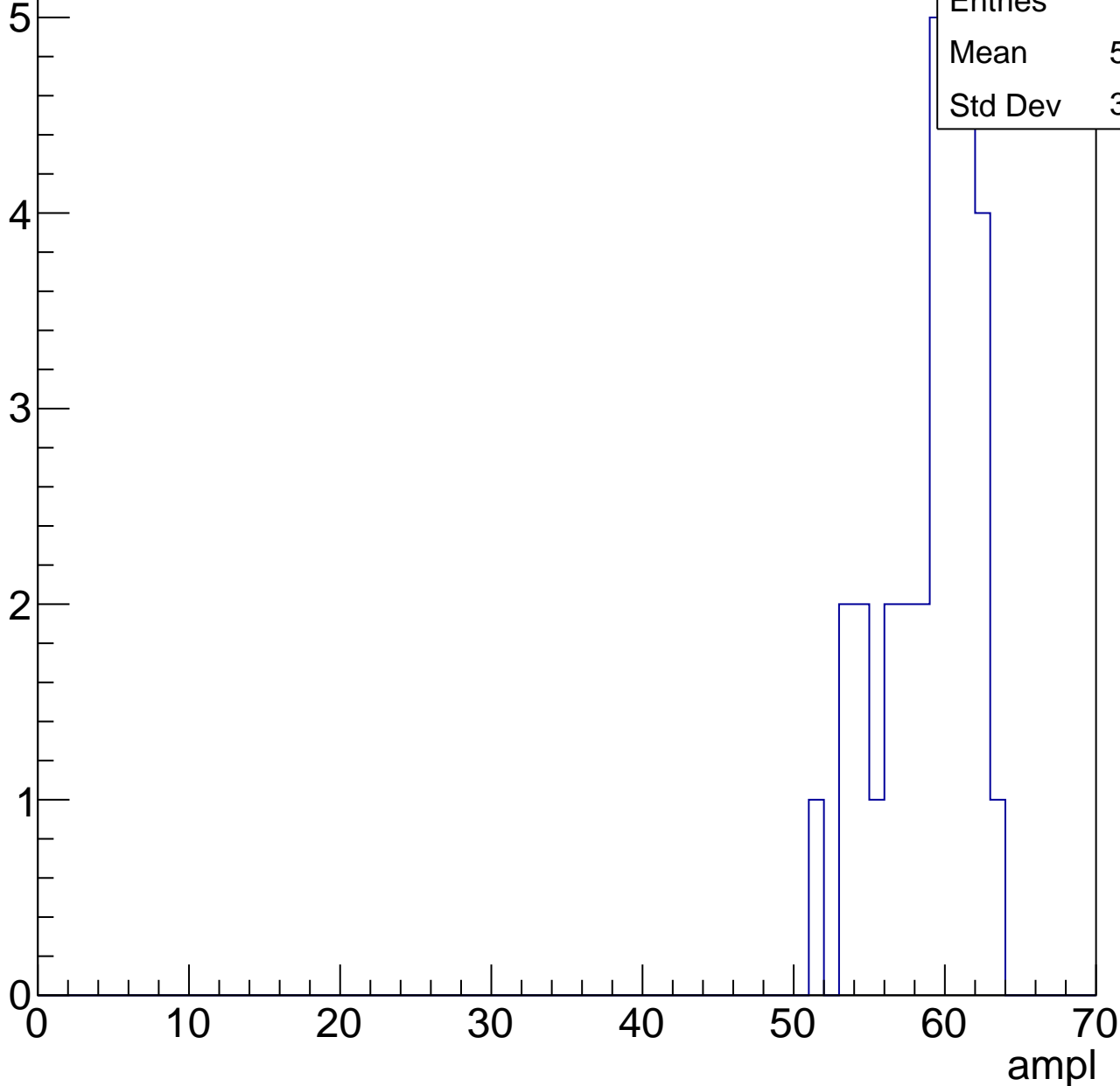


B1L103S, U14-ch4, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

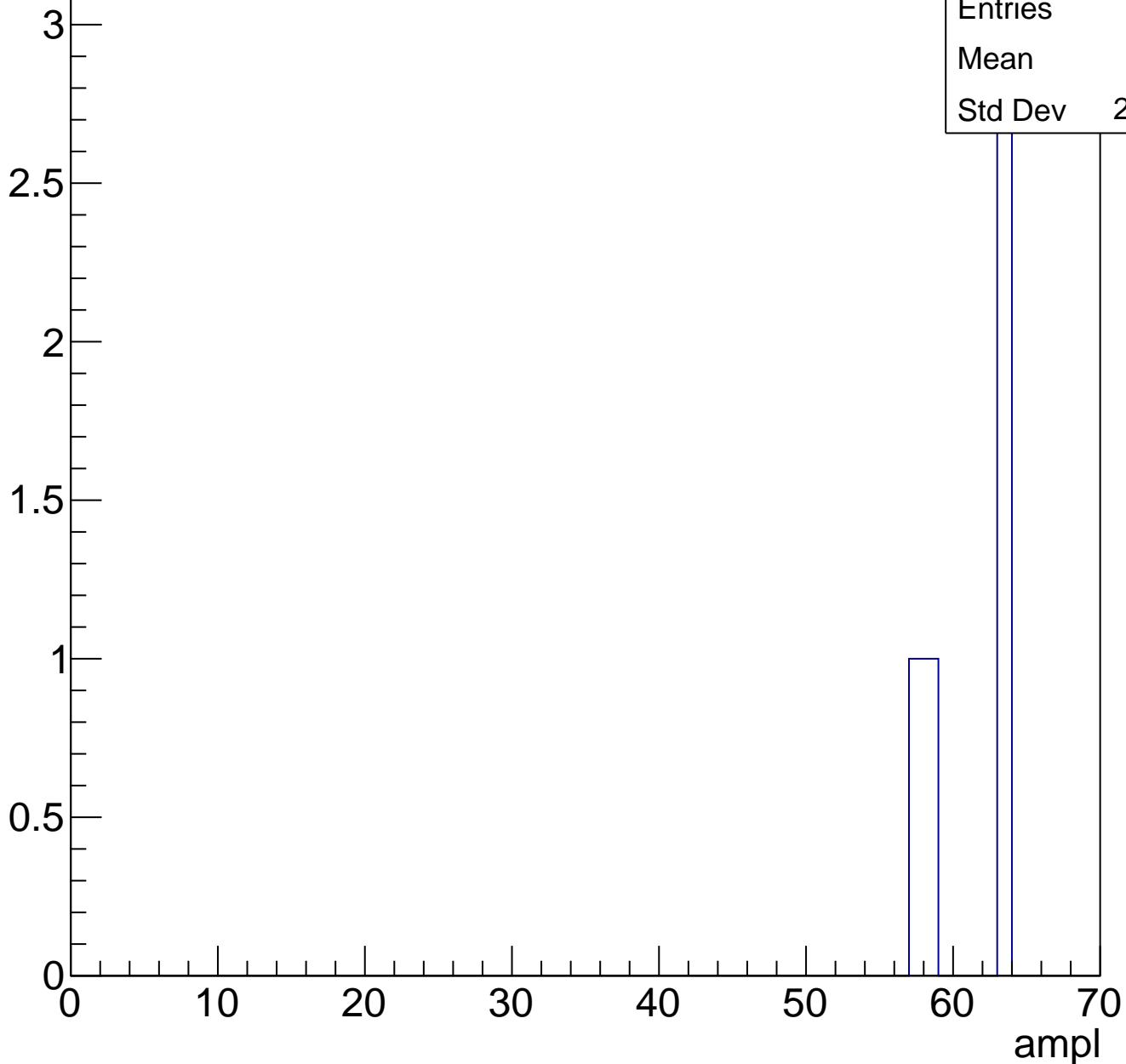
Entries	32
Mean	58.53
Std Dev	3.062



B1L103S, U14-ch4, adc6

calib_packv5_041523_1651.root, FC#0, port C2

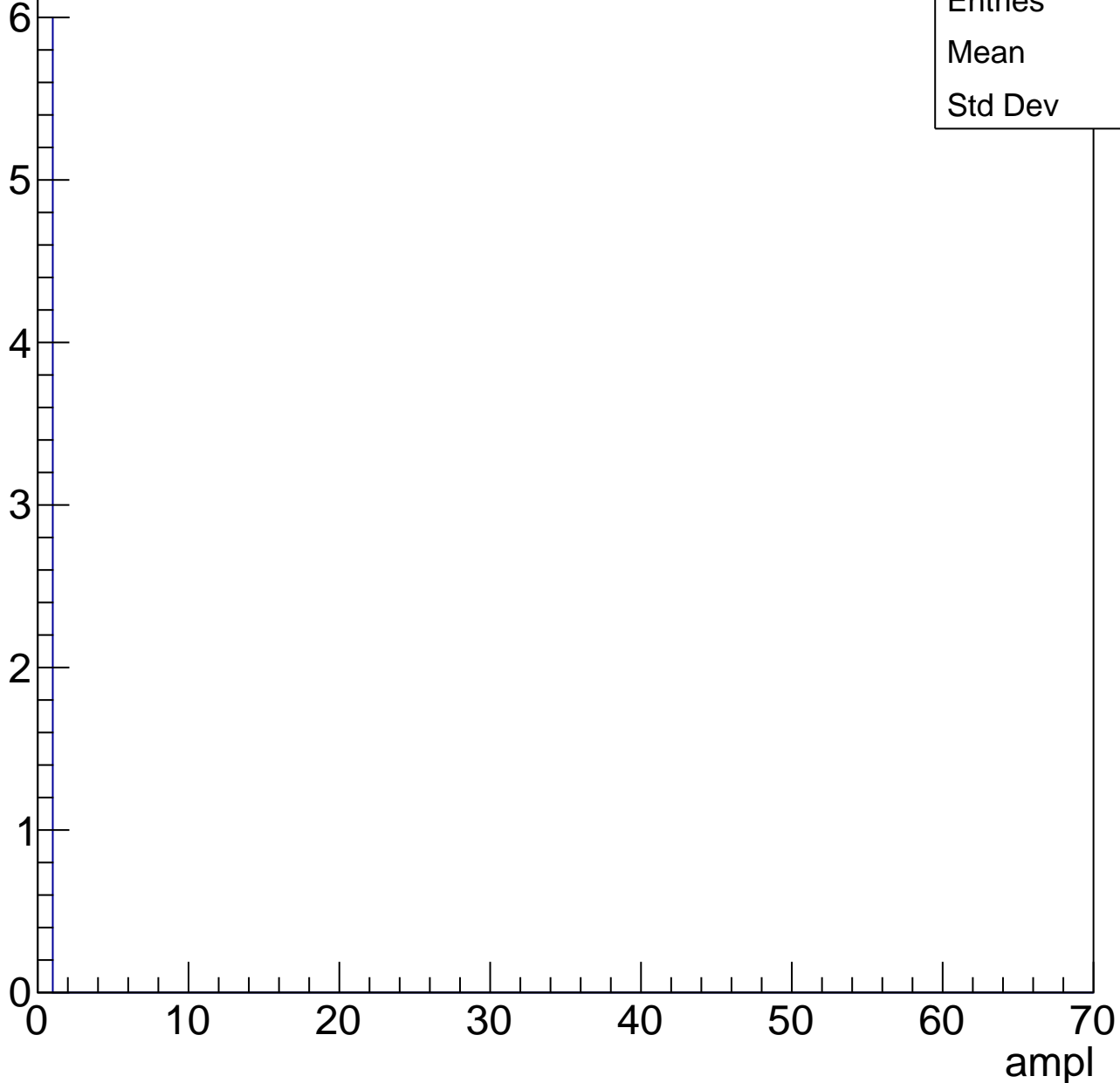
Entry



B1L103S, U14-ch4, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

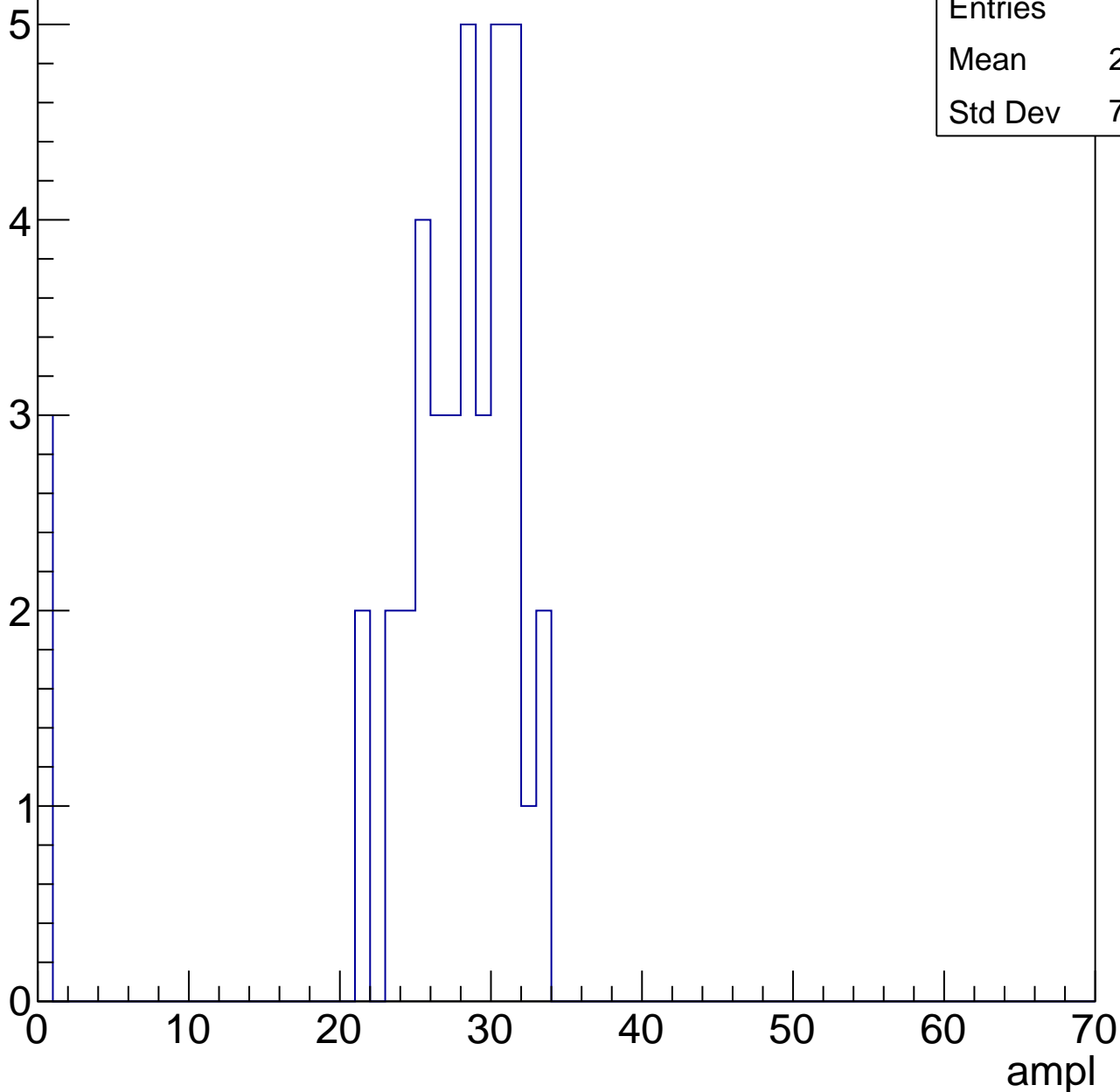


B1L103S, U14-ch5, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	25.62
Std Dev	7.892

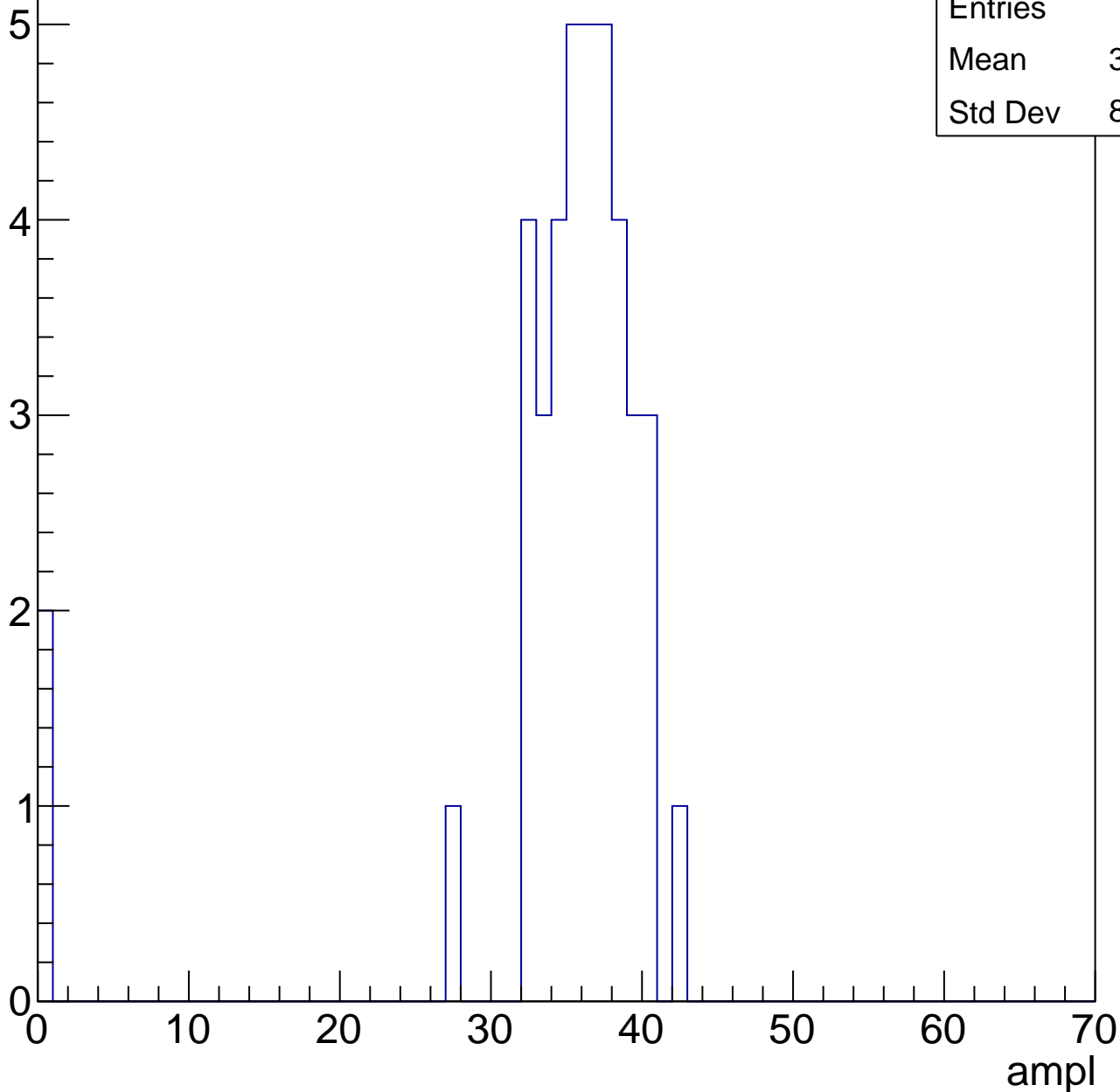


B1L103S, U14-ch5, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

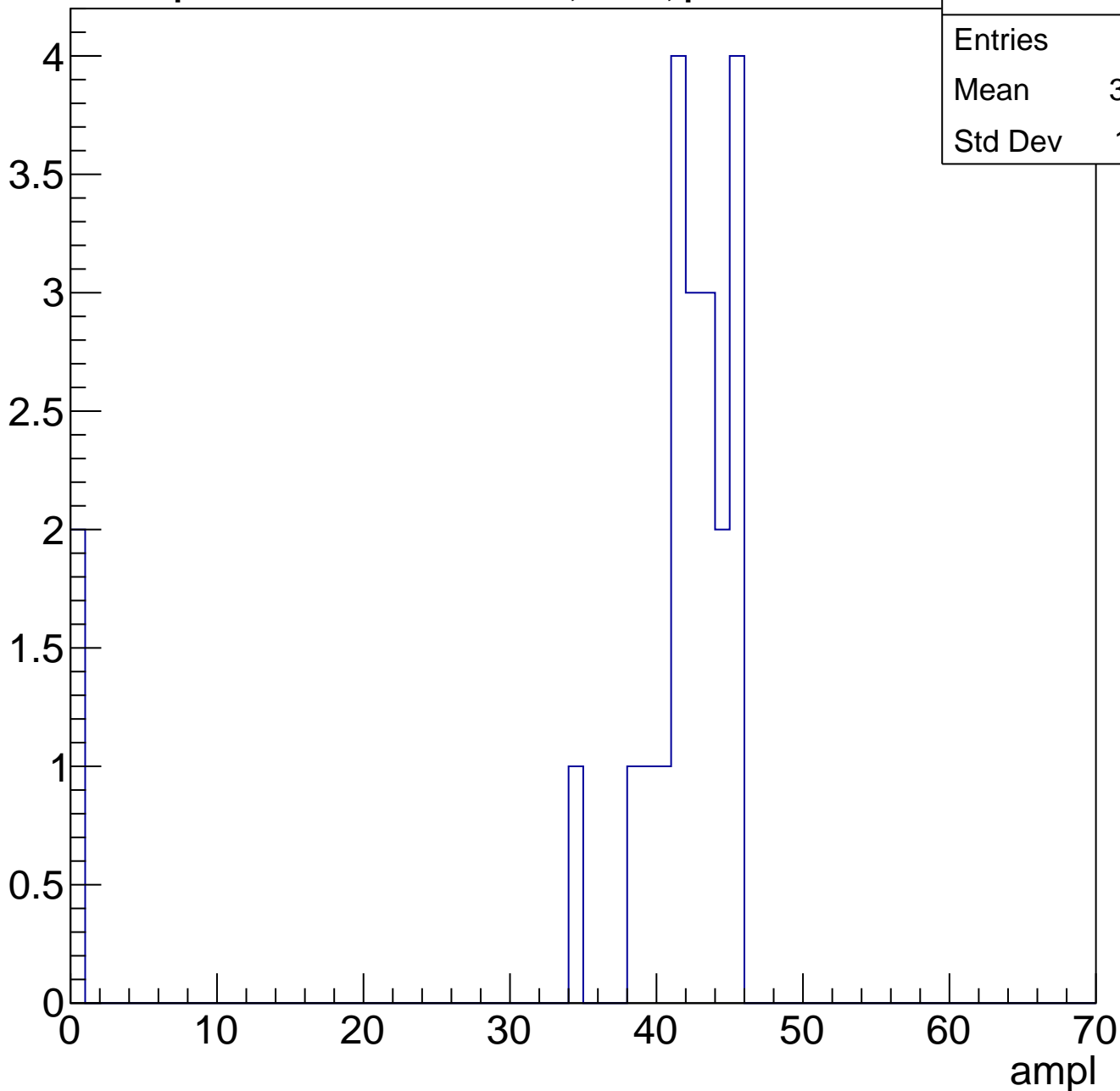
Entries	40
Mean	34.02
Std Dev	8.308



B1L103S, U14-ch5, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

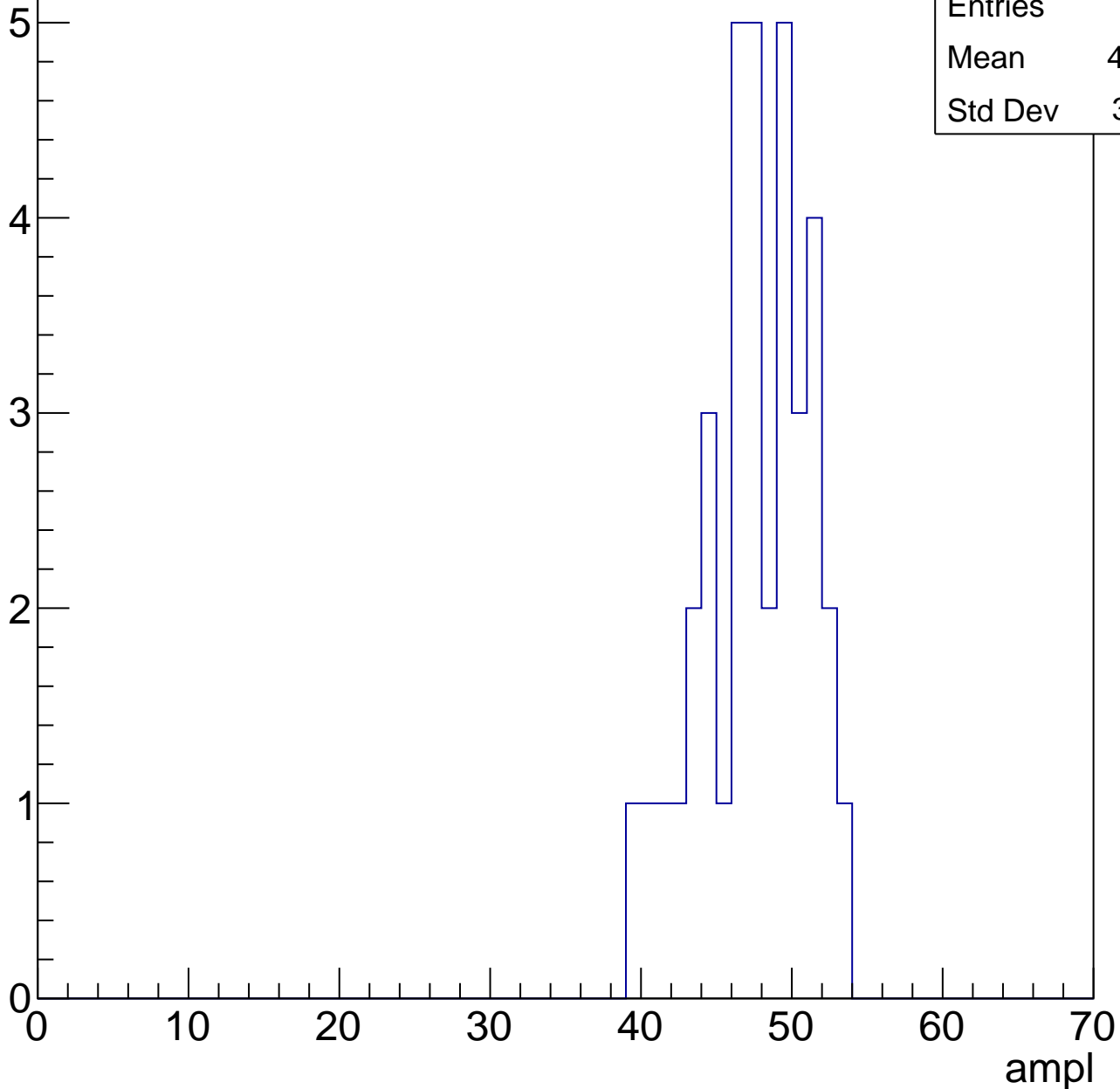


B1L103S, U14-ch5, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

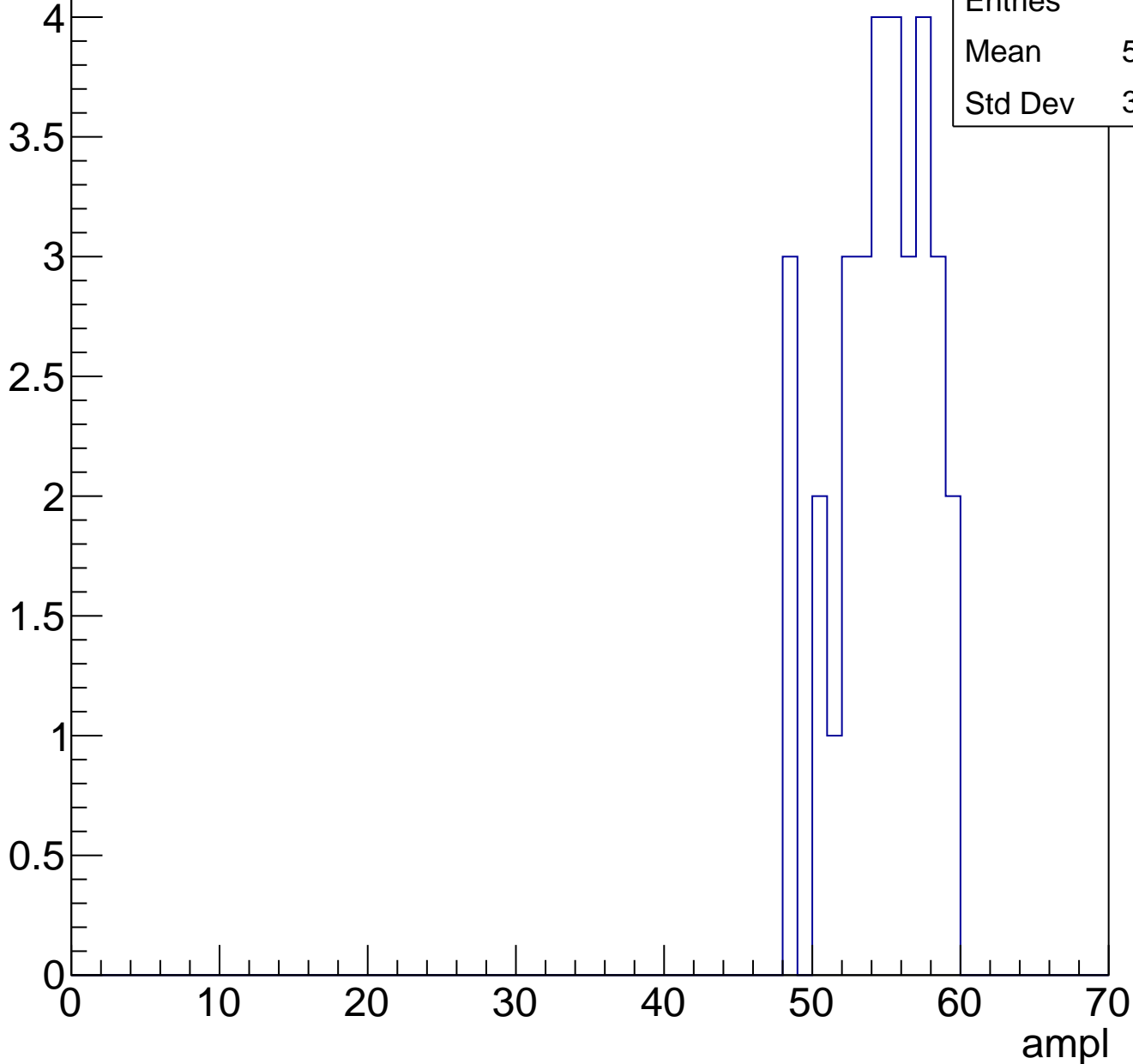
Entries	37
Mean	47.08
Std Dev	3.451



B1L103S, U14-ch5, adc4

calib_packv5_041523_1651.root, FC#0, port C2

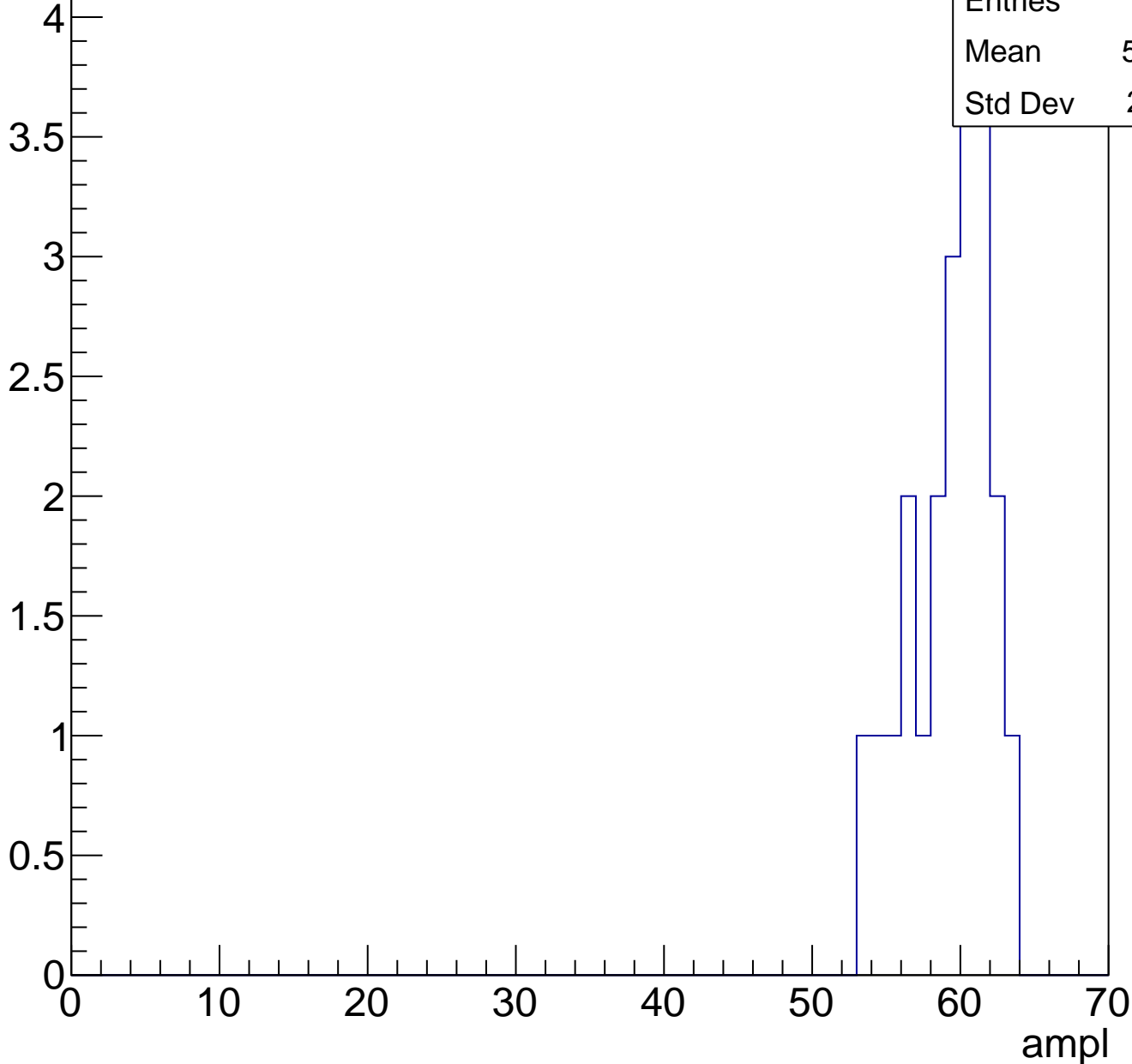
Entry



B1L103S, U14-ch5, adc5

calib_packv5_041523_1651.root, FC#0, port C2

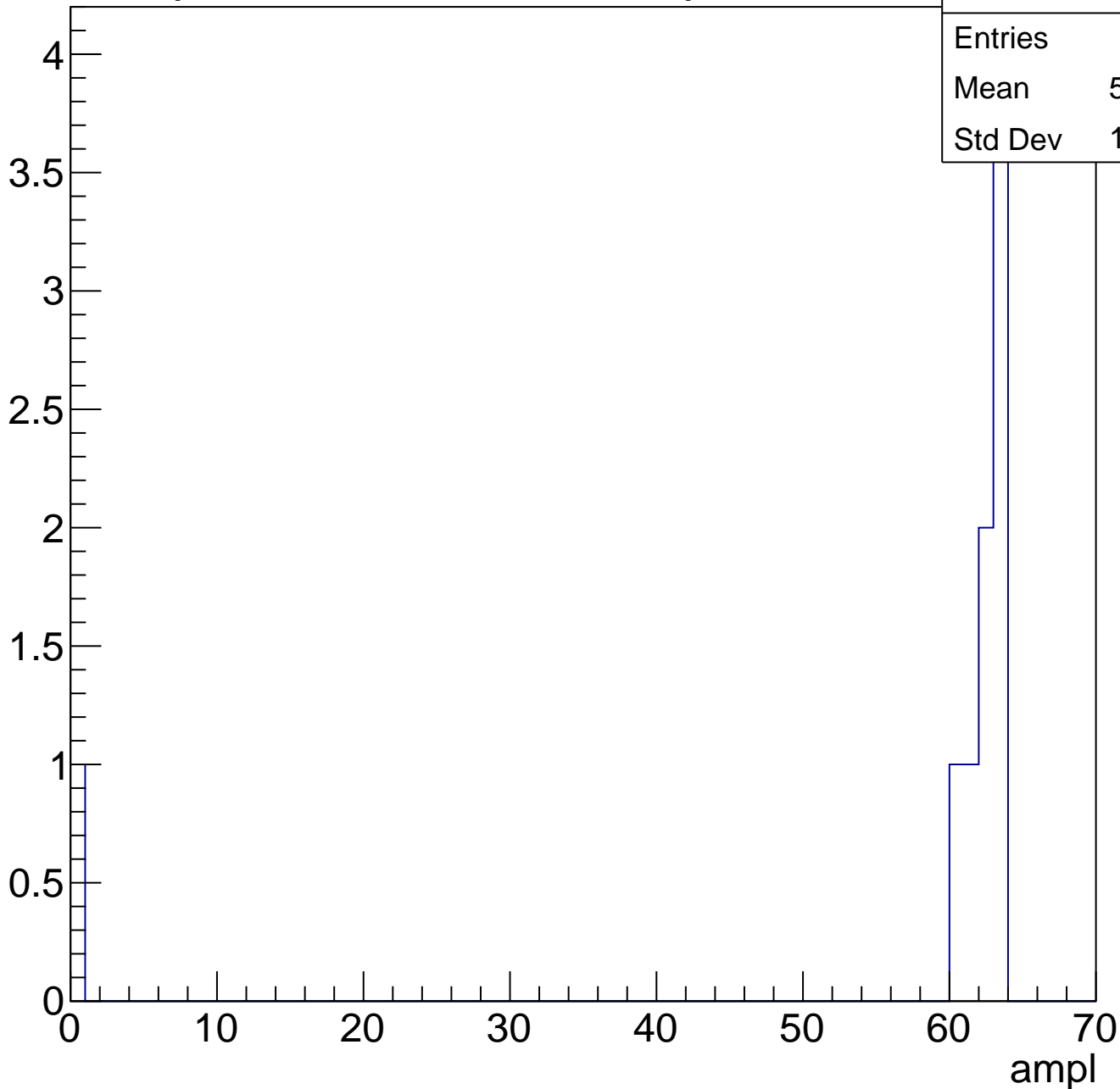
Entry



B1L103S, U14-ch5, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch5, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	12
Mean	5.167
Std Dev	17.14

Entry

10

8

6

4

2

0

0

10

20

30

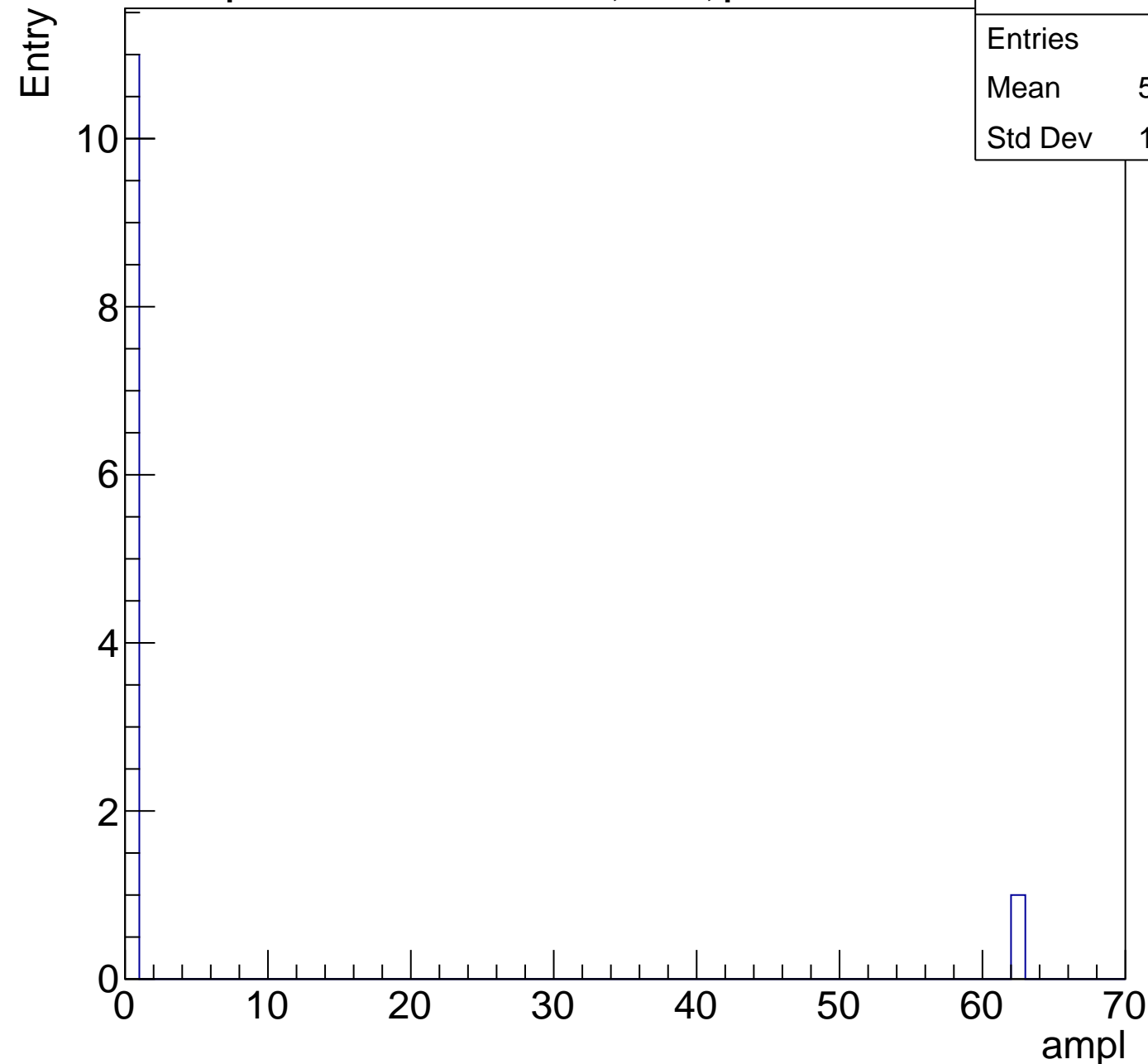
40

50

60

70

ampl

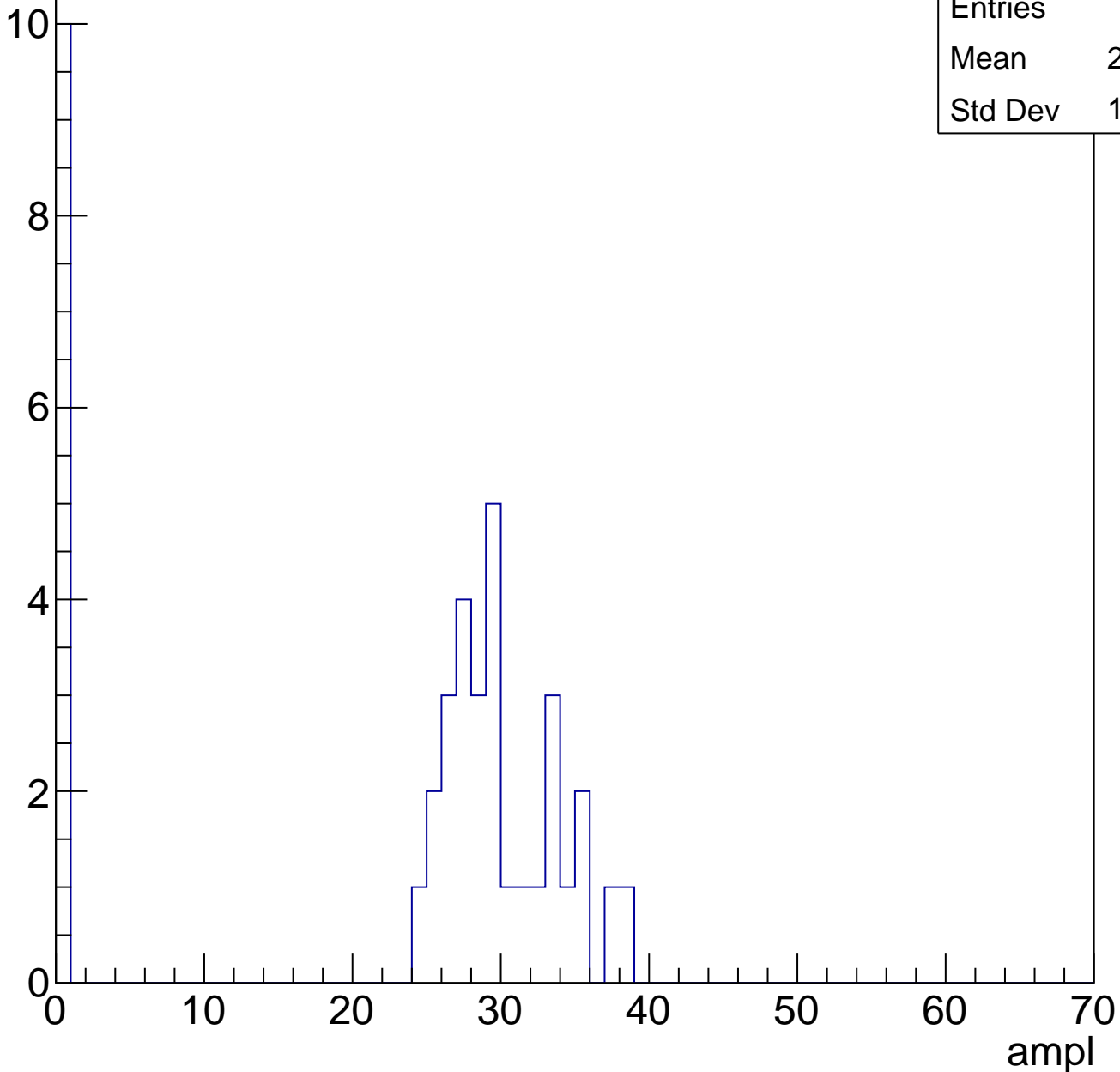


B1L103S, U14-ch6, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	39
Mean	22.05
Std Dev	13.33

Entry

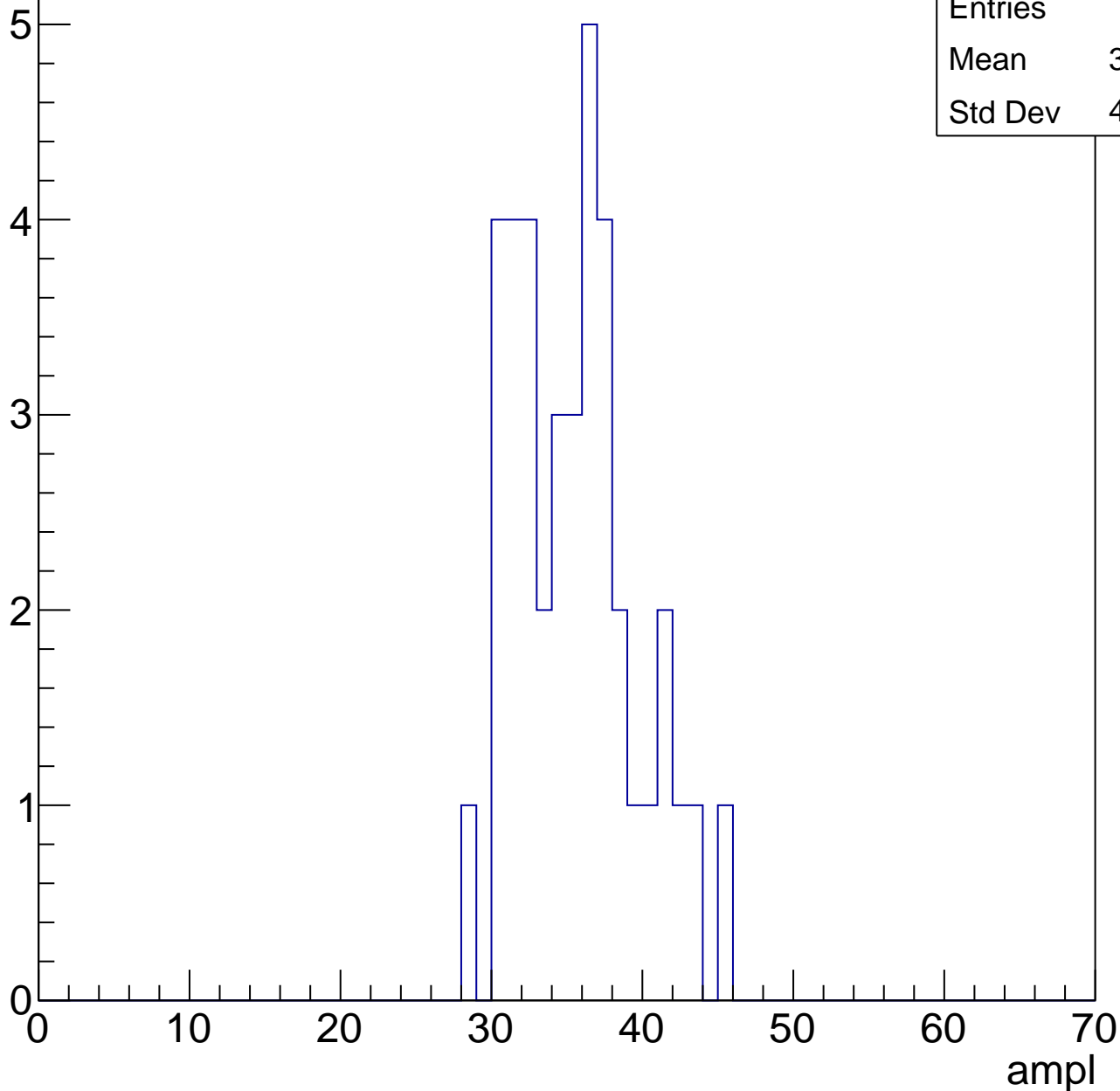


B1L103S, U14-ch6, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	35.08
Std Dev	4.002

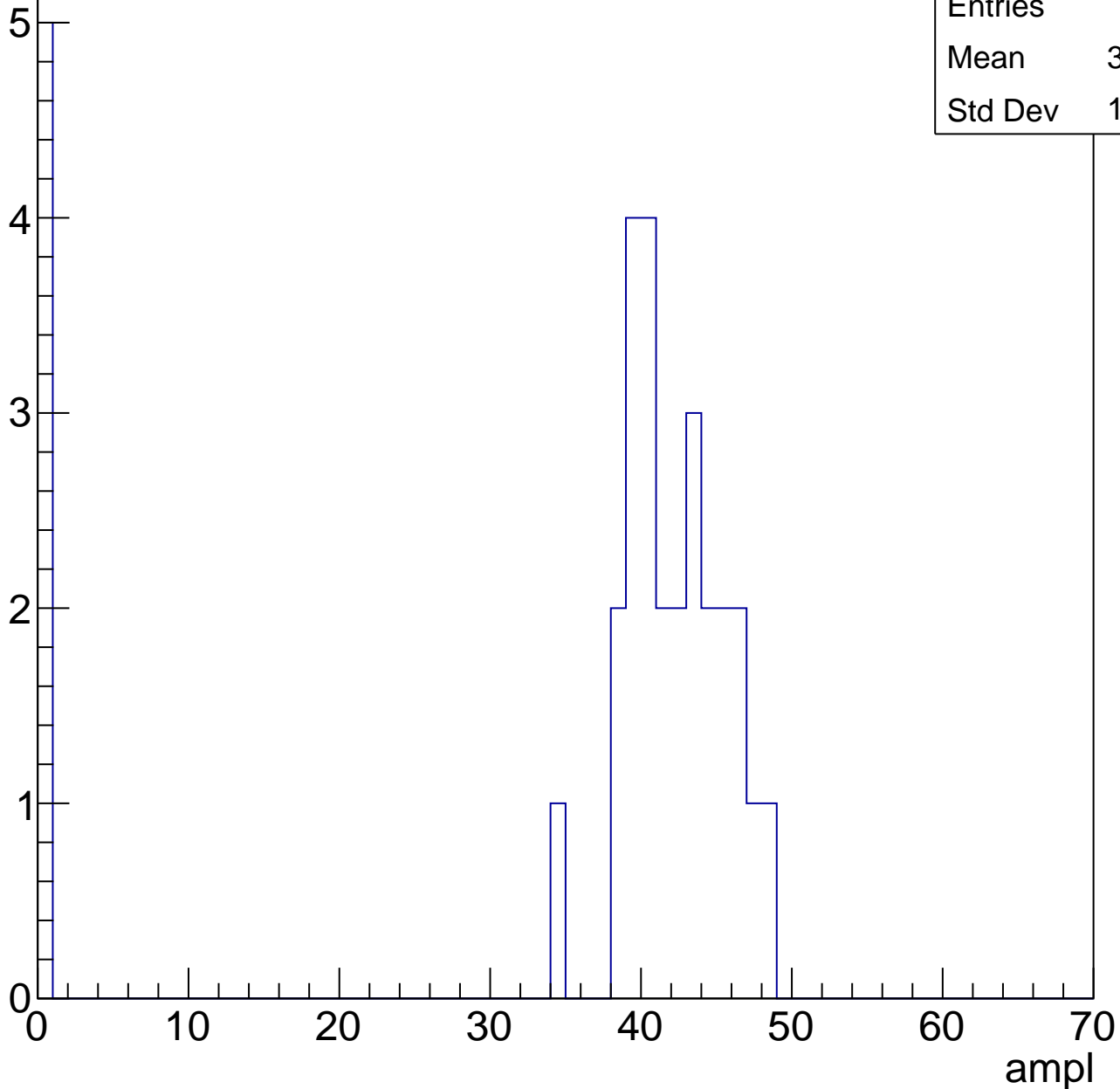


B1L103S, U14-ch6, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

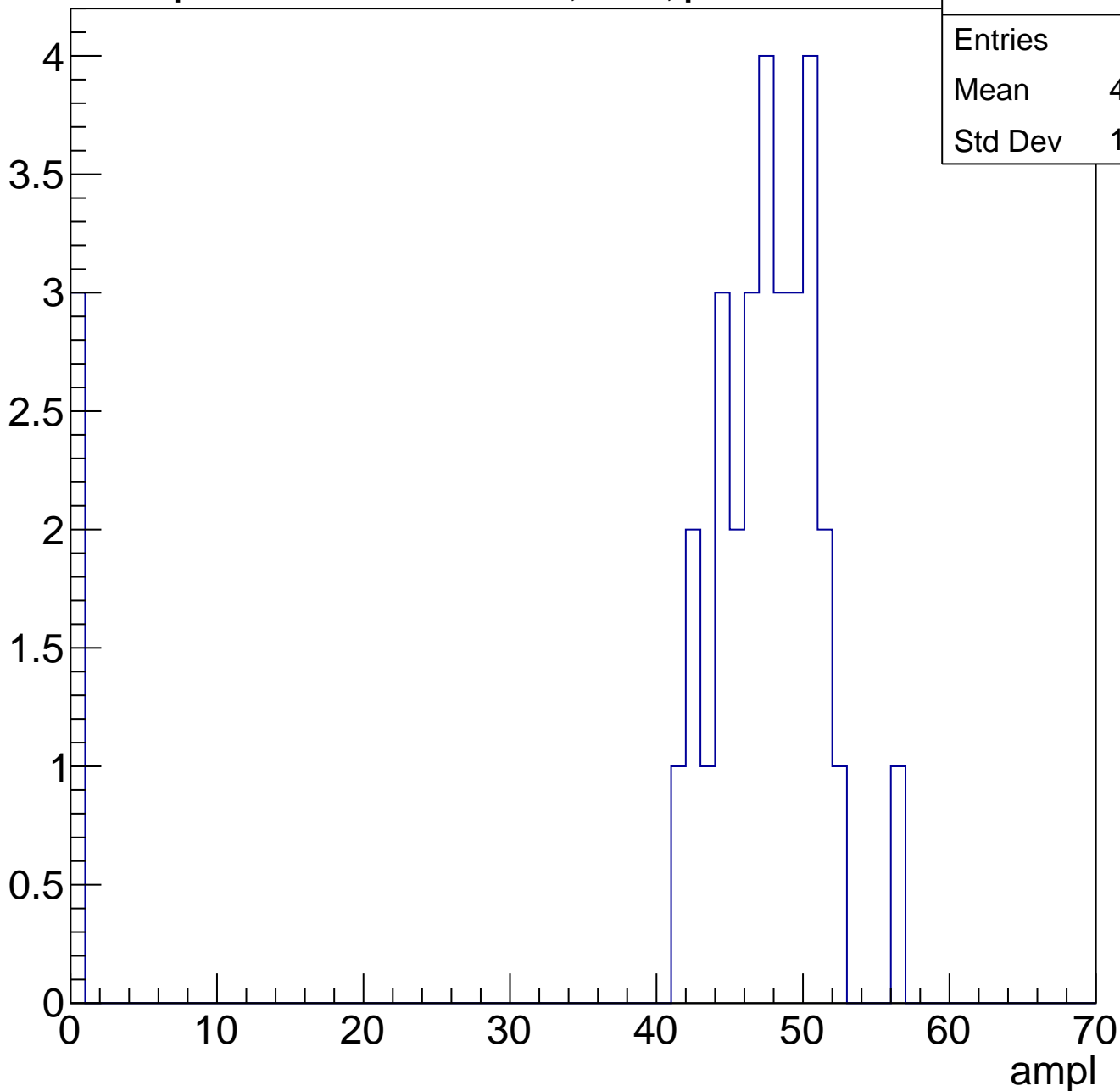
Entries	31
Mean	35.03
Std Dev	15.64



B1L103S, U14-ch6, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

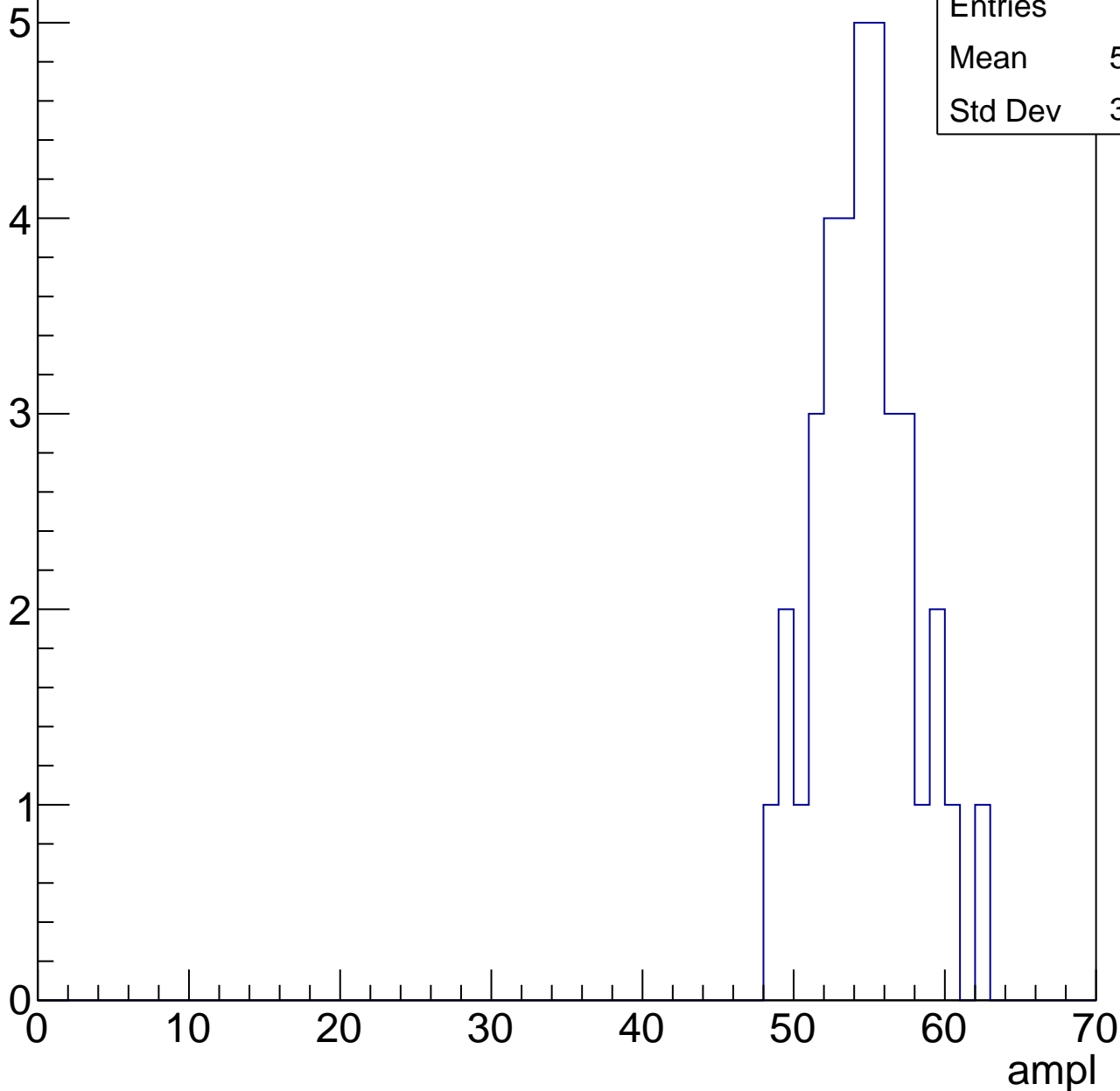


B1L103S, U14-ch6, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	36
Mean	54.19
Std Dev	3.152

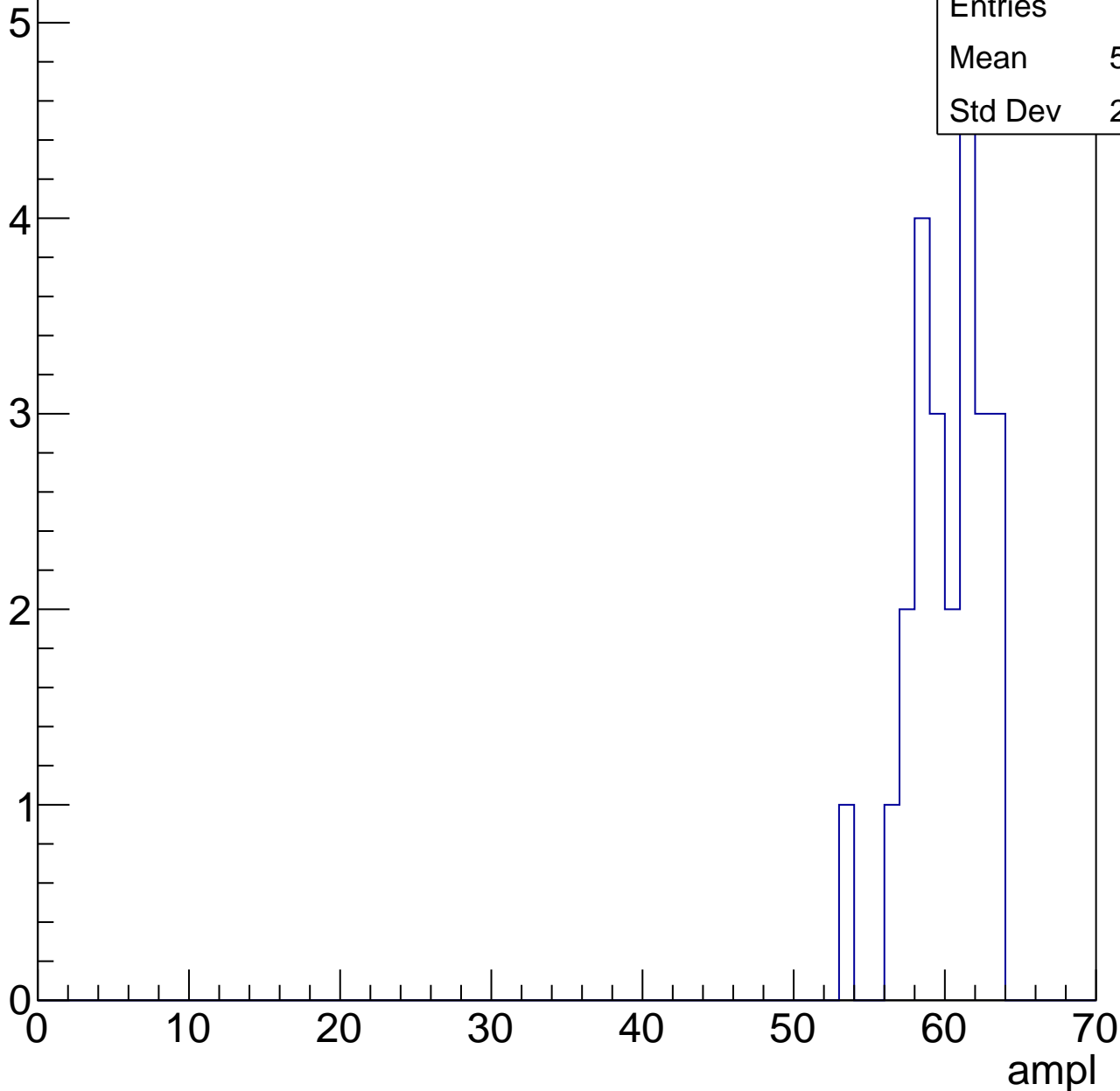


B1L103S, U14-ch6, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	24
Mean	59.67
Std Dev	2.444



B1L103S, U14-ch6, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	5
Mean	61.6
Std Dev	1.356

ampl

0 10 20 30 40 50 60 70

B1L103S, U14-ch6, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch7, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	45
Mean	21.78
Std Dev	12.88

Entry

10

8

6

4

2

0

0

10

20

30

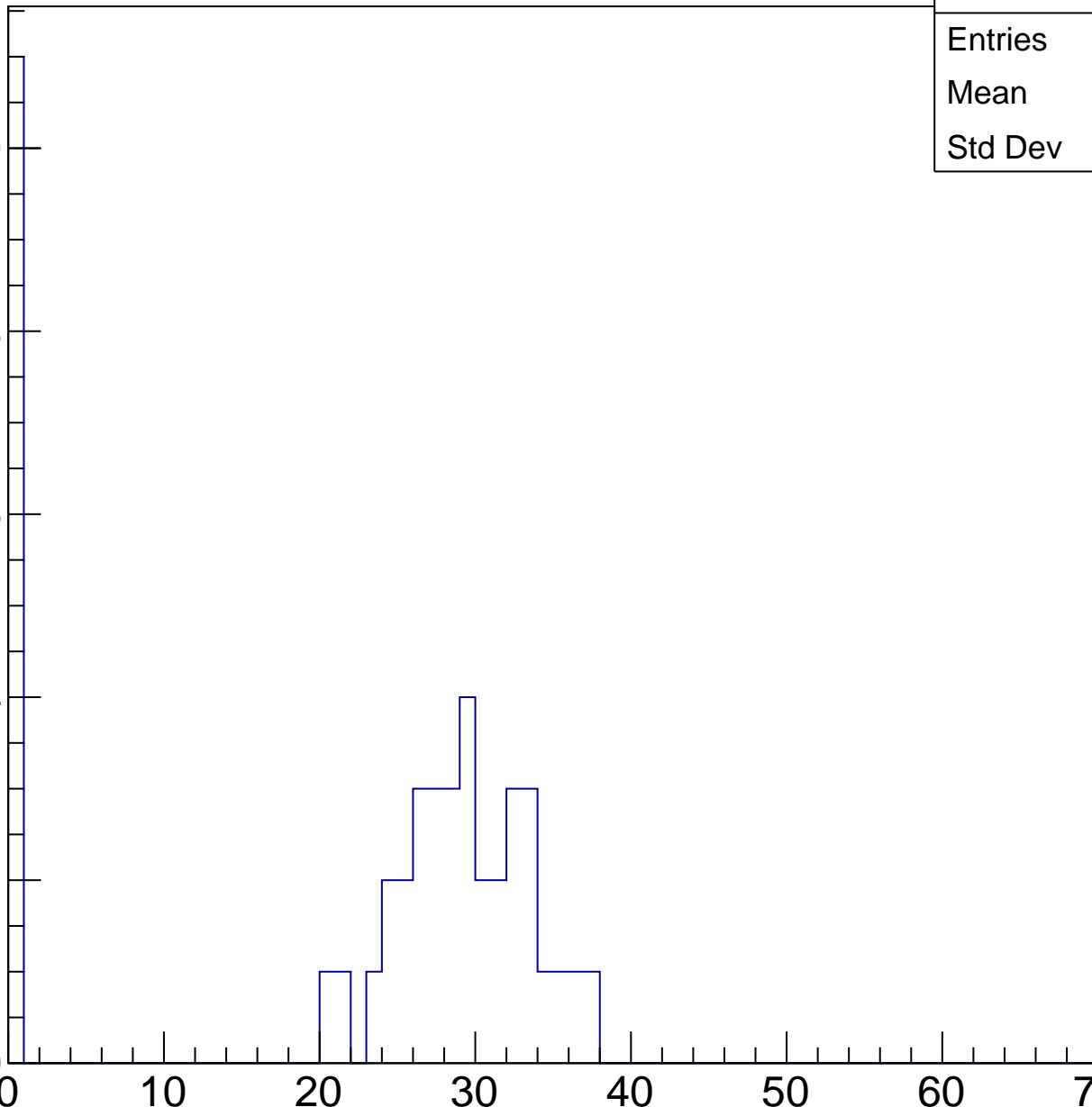
40

50

60

70

ampl

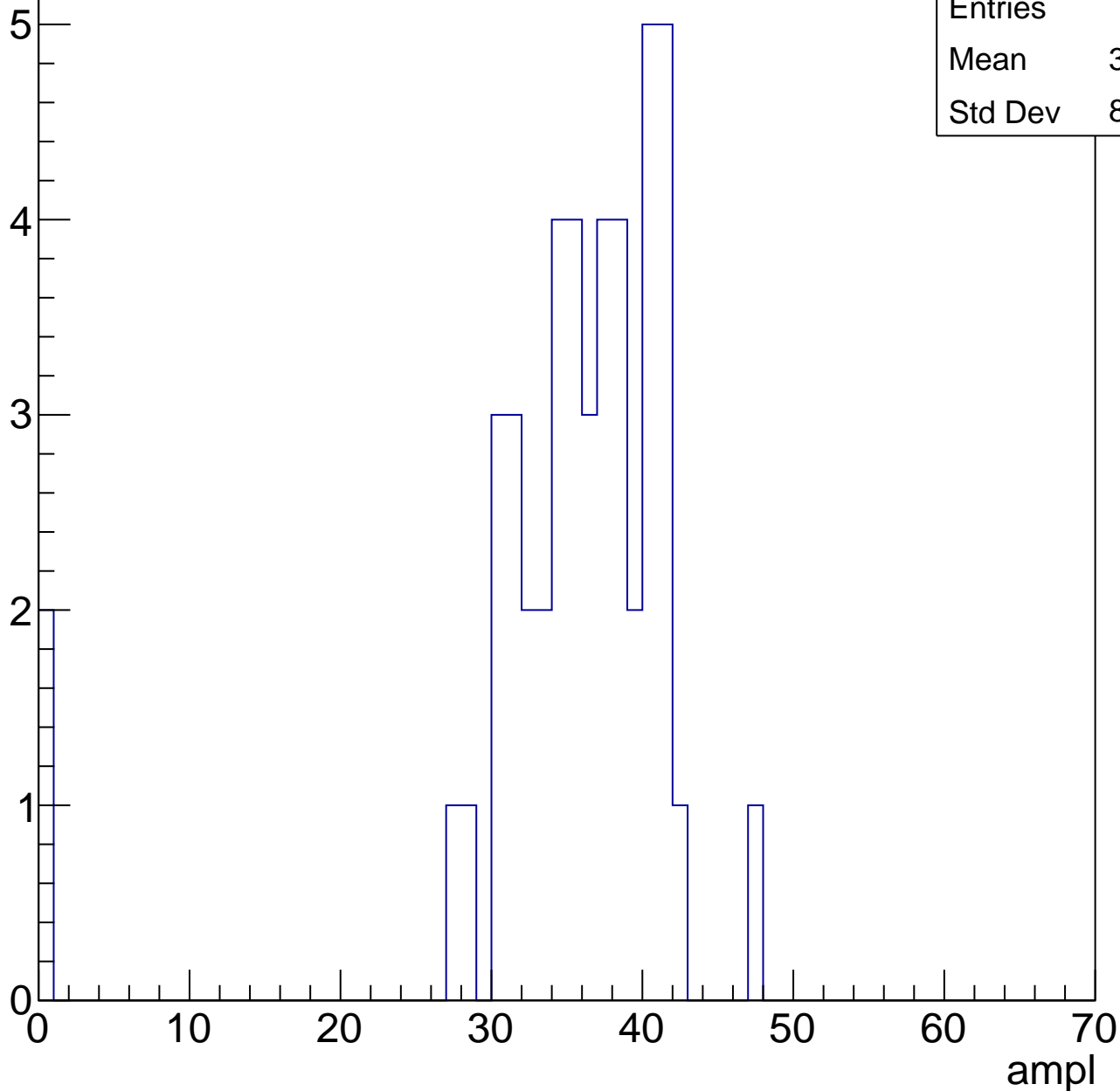


B1L103S, U14-ch7, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	47
Mean	34.55
Std Dev	8.369

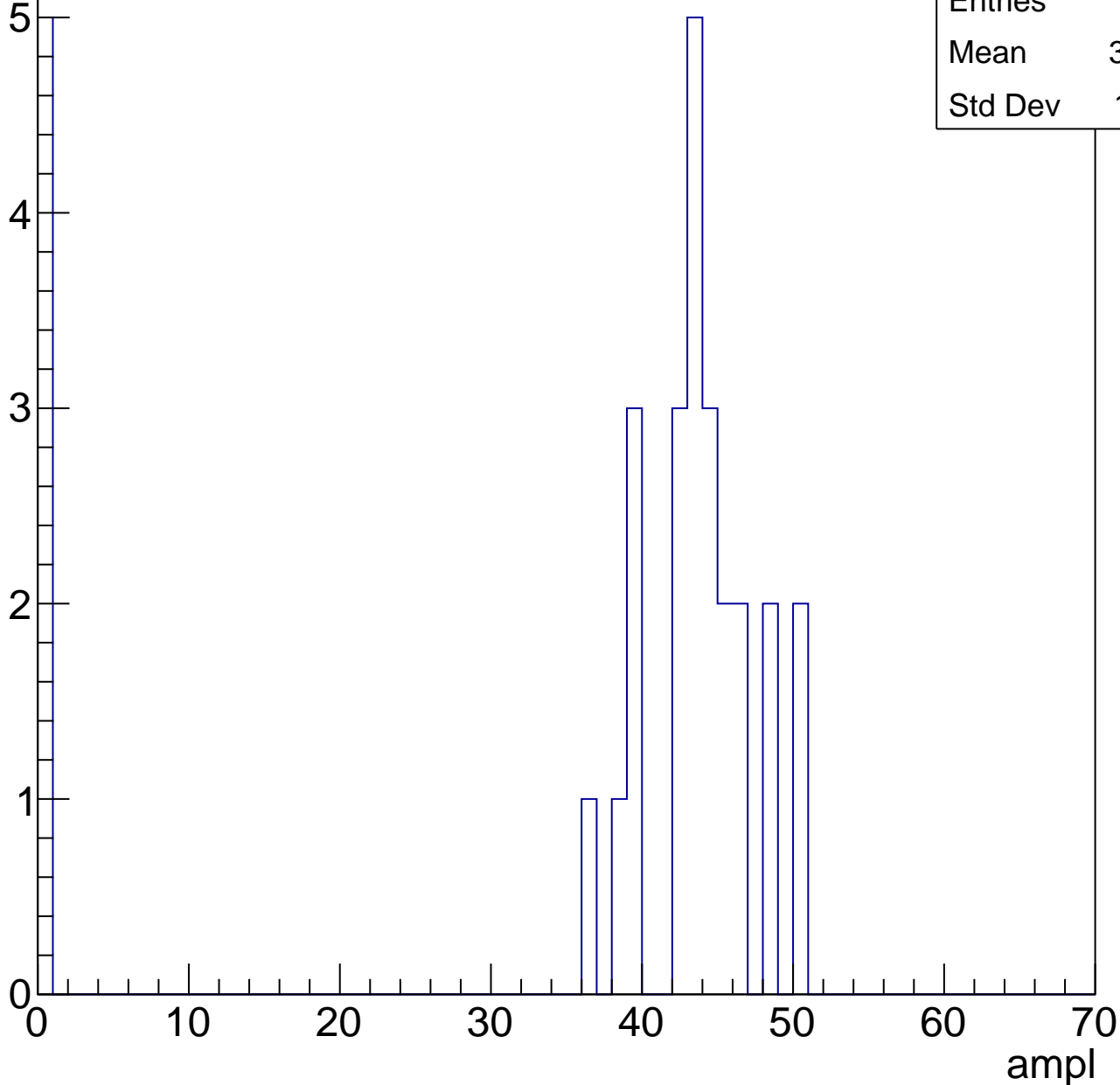


B1L103S, U14-ch7, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

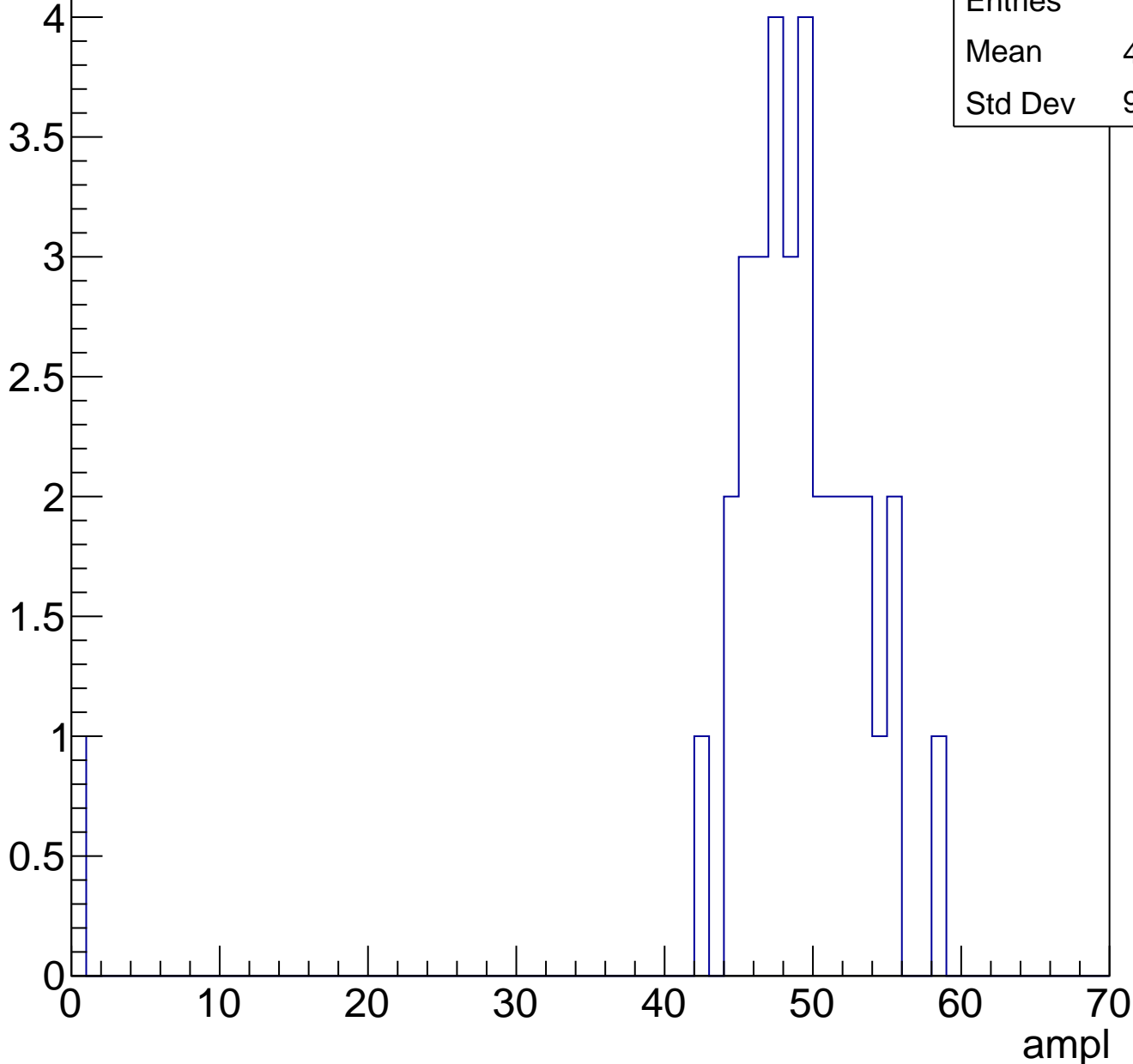
Entries	29
Mean	35.93
Std Dev	16.71



B1L103S, U14-ch7, adc3

calib_packv5_041523_1651.root, FC#0, port C2

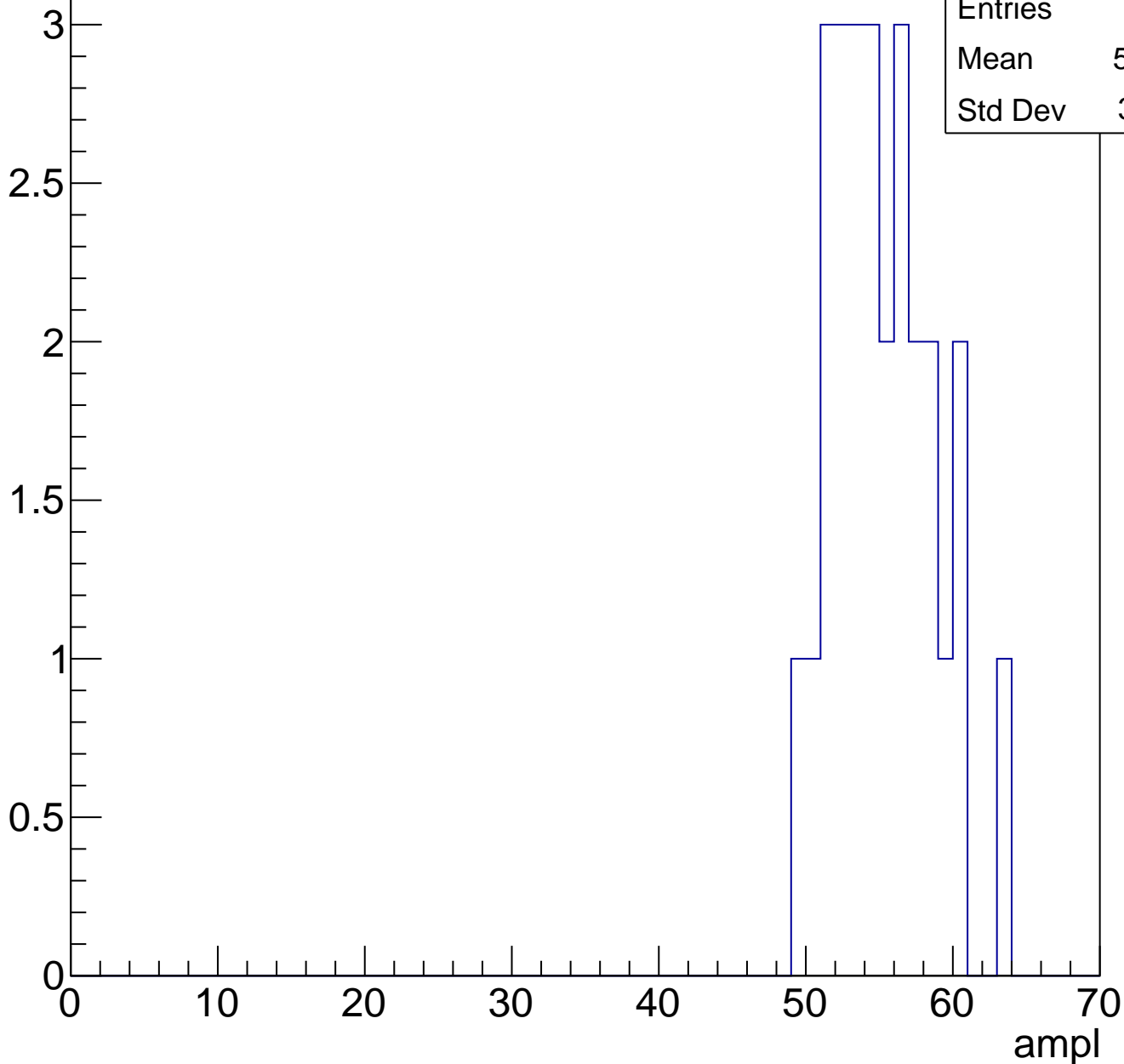
Entry



B1L103S, U14-ch7, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

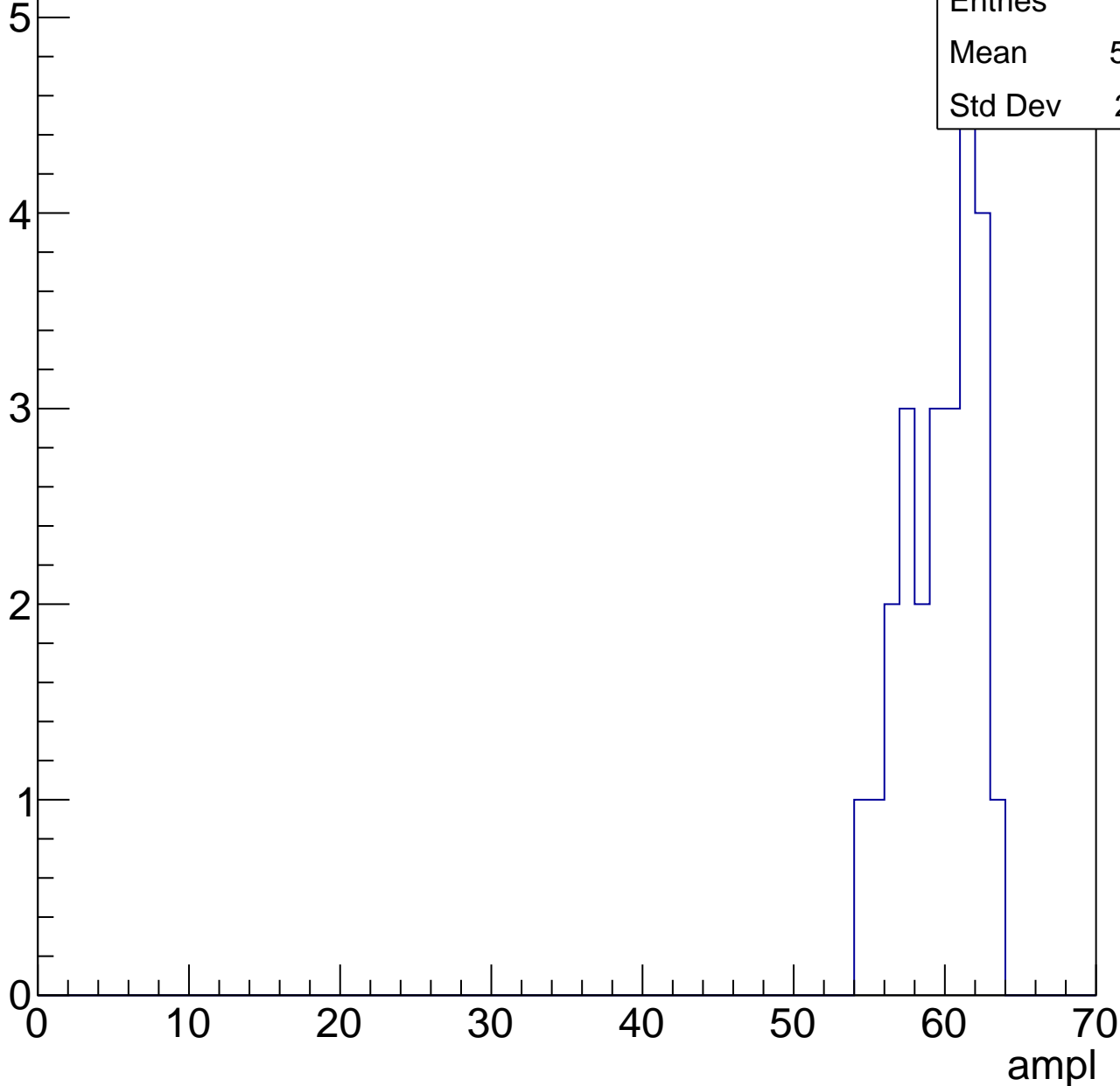


B1L103S, U14-ch7, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

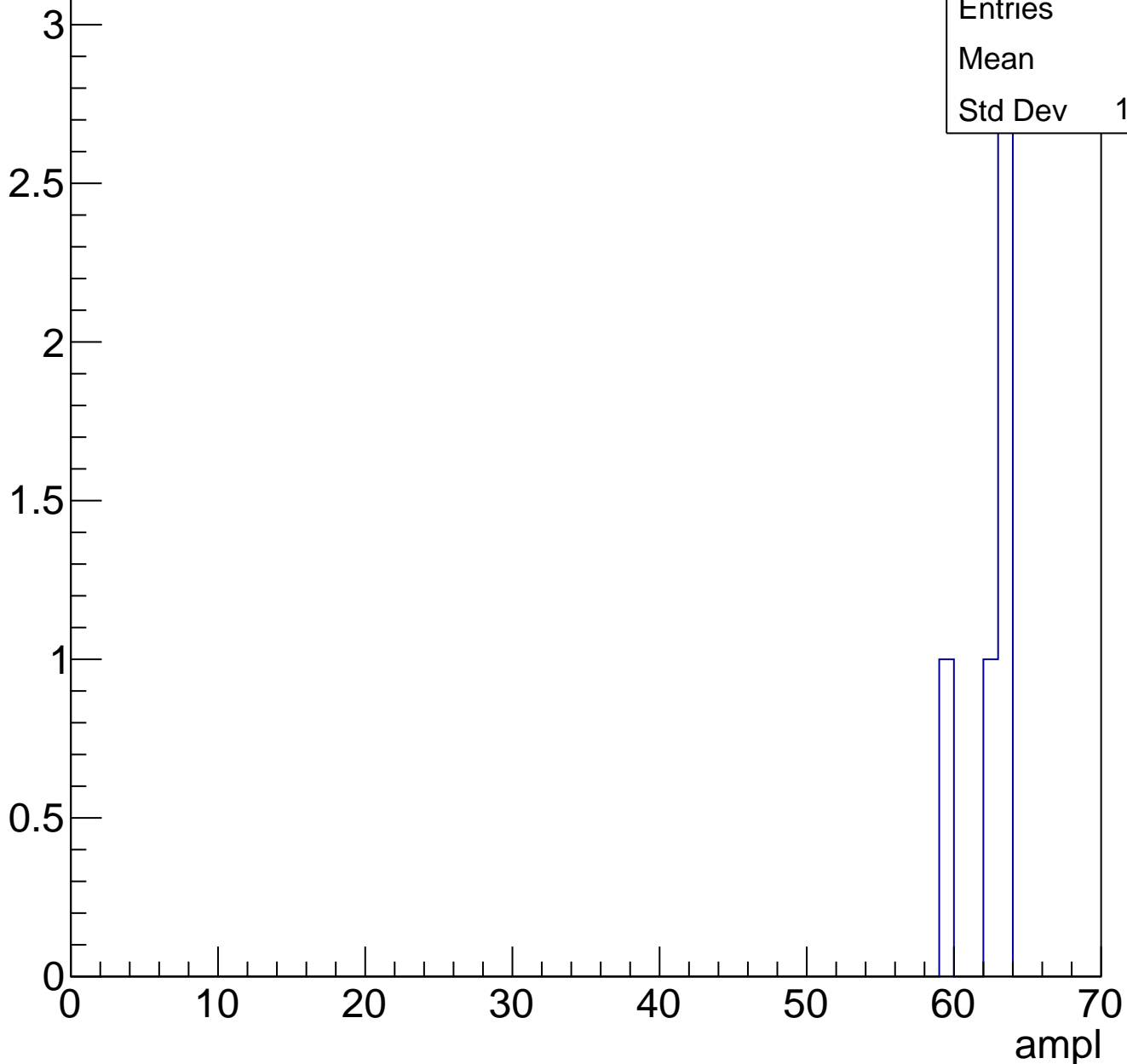
Entries	25
Mean	59.24
Std Dev	2.421



B1L103S, U14-ch7, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch7, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

Entries

11

Mean

0

Std Dev

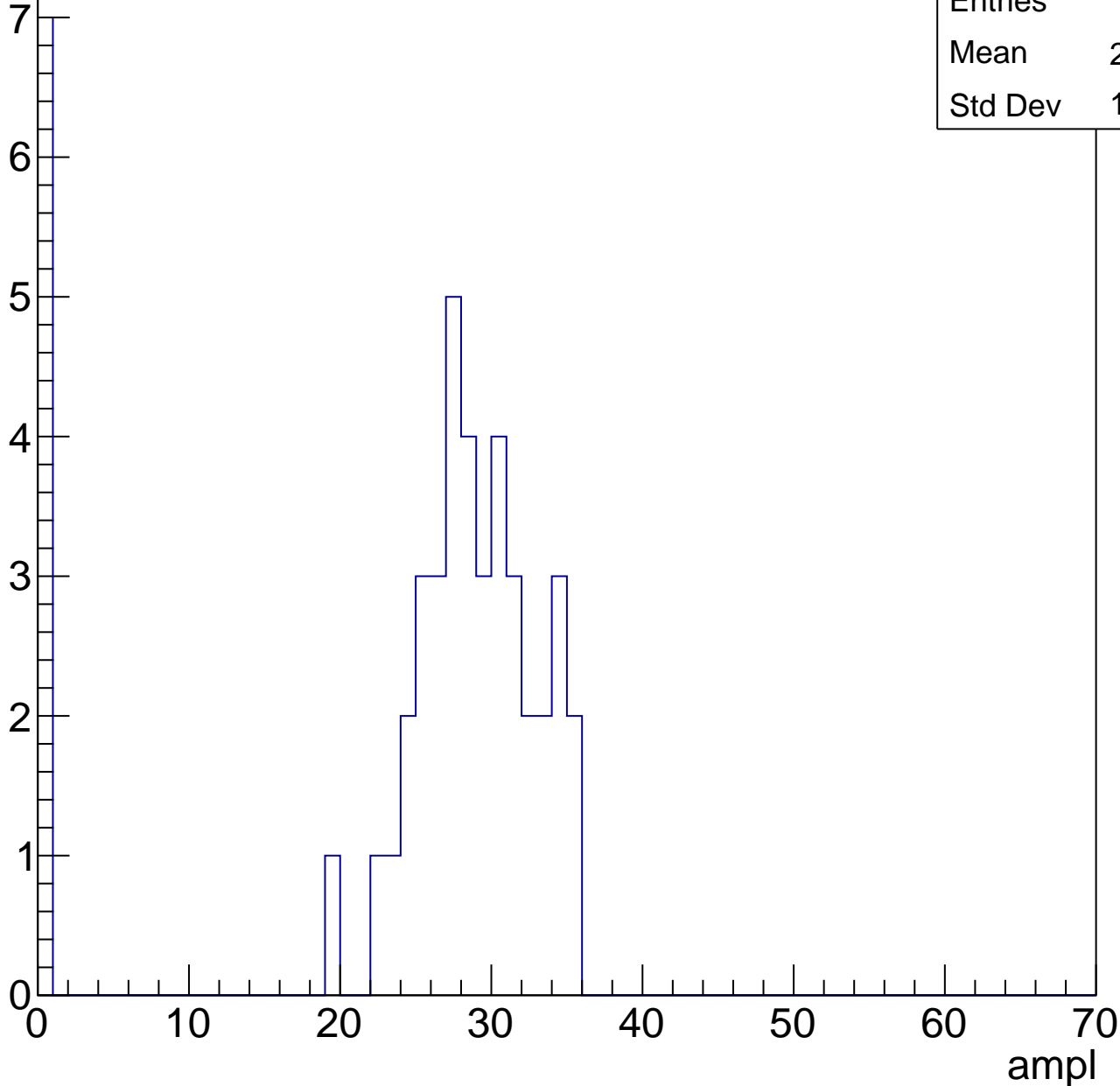
0

B1L103S, U14-ch8, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	46
Mean	24.22
Std Dev	10.82

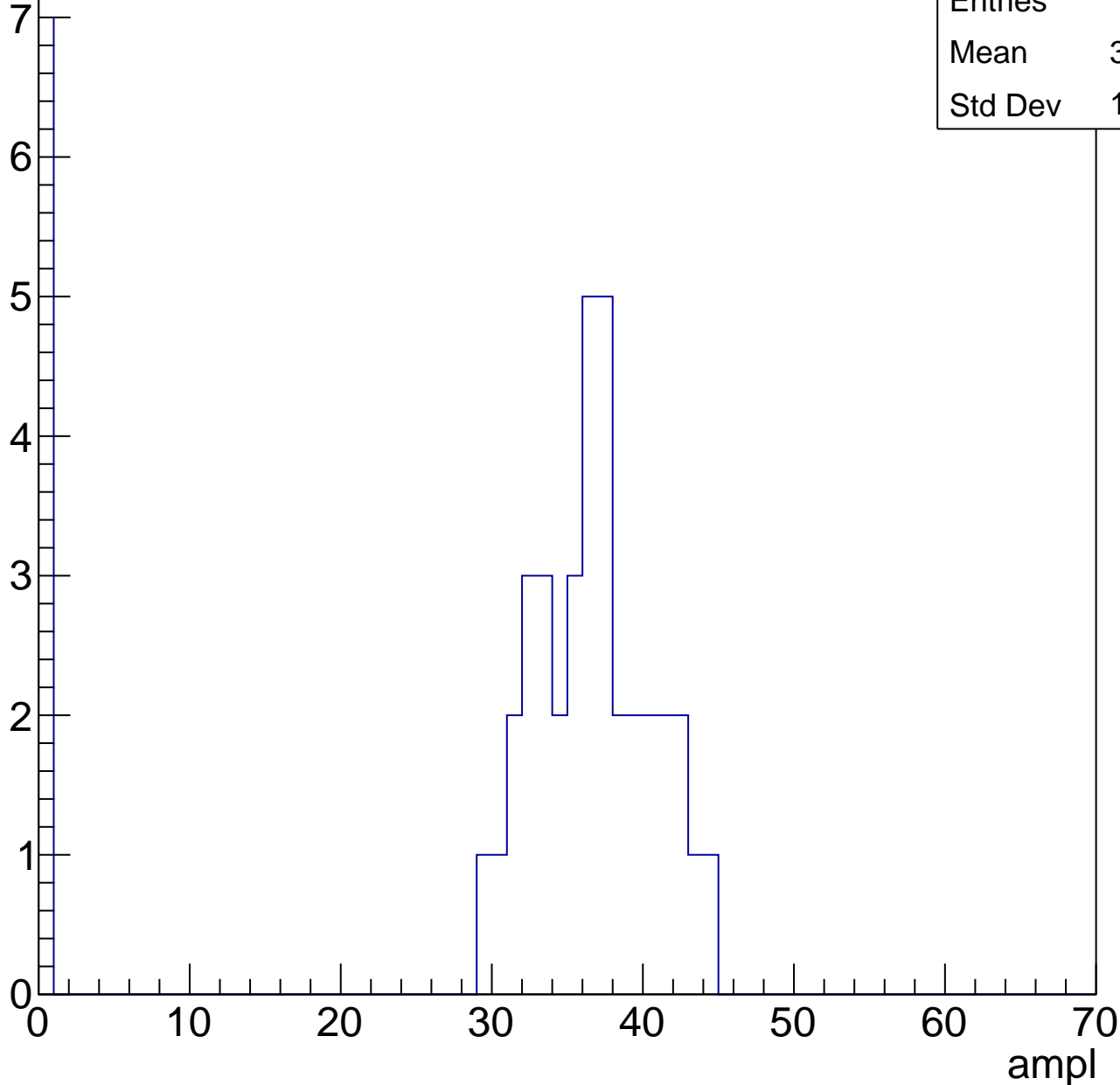


B1L103S, U14-ch8, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

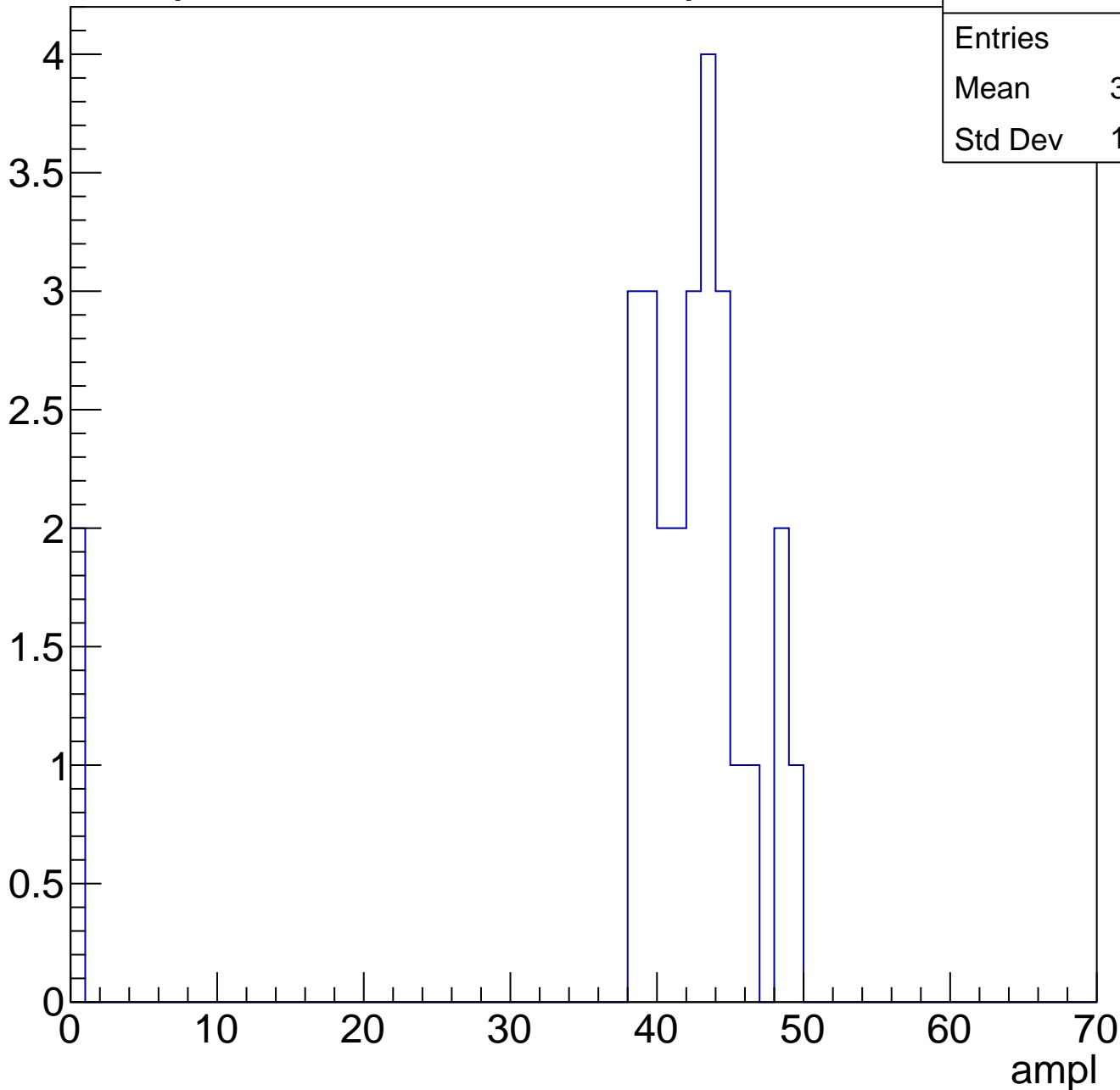
Entries	44
Mean	30.48
Std Dev	13.69



B1L103S, U14-ch8, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

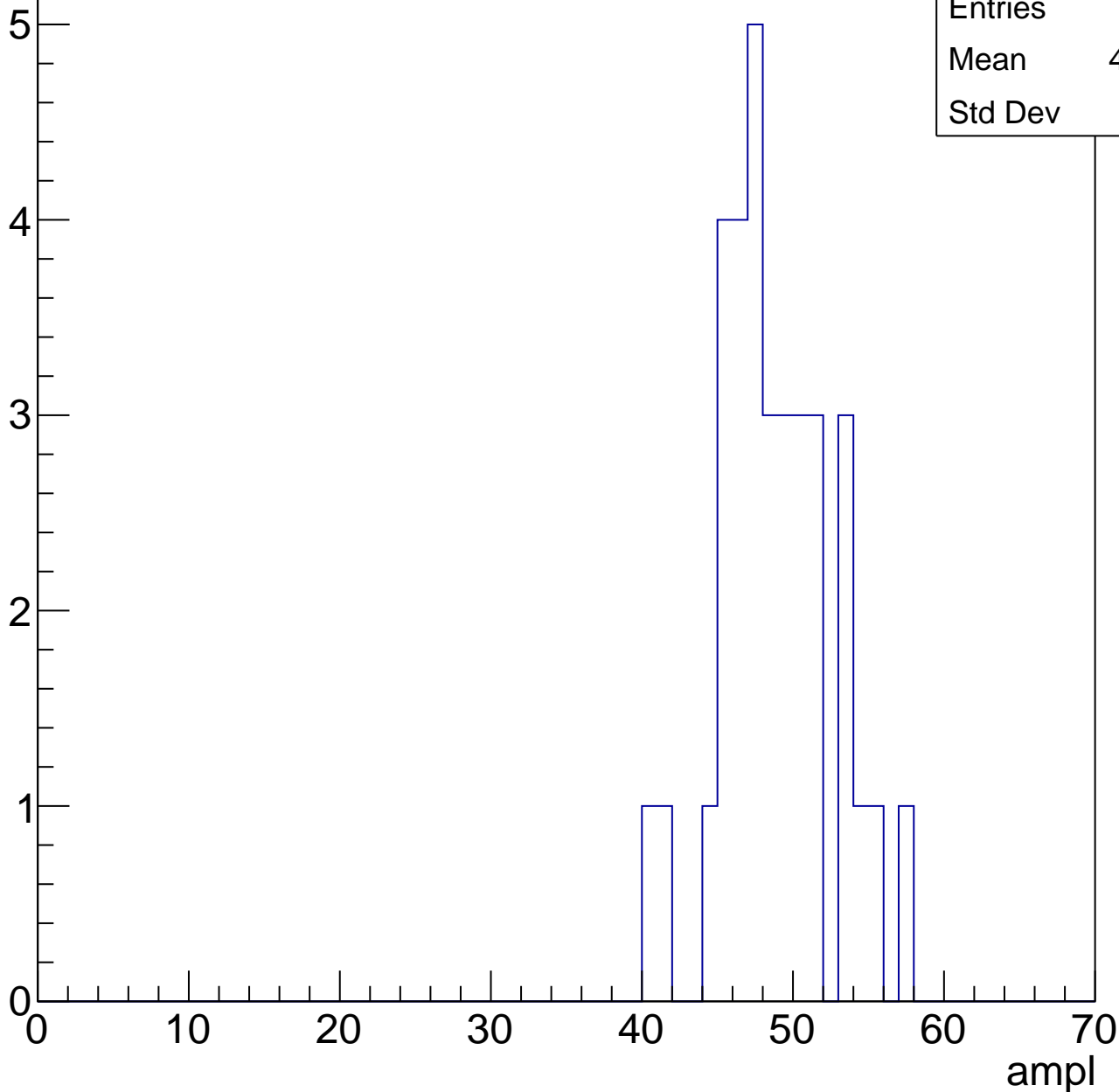


B1L103S, U14-ch8, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	34
Mean	48.32
Std Dev	3.7

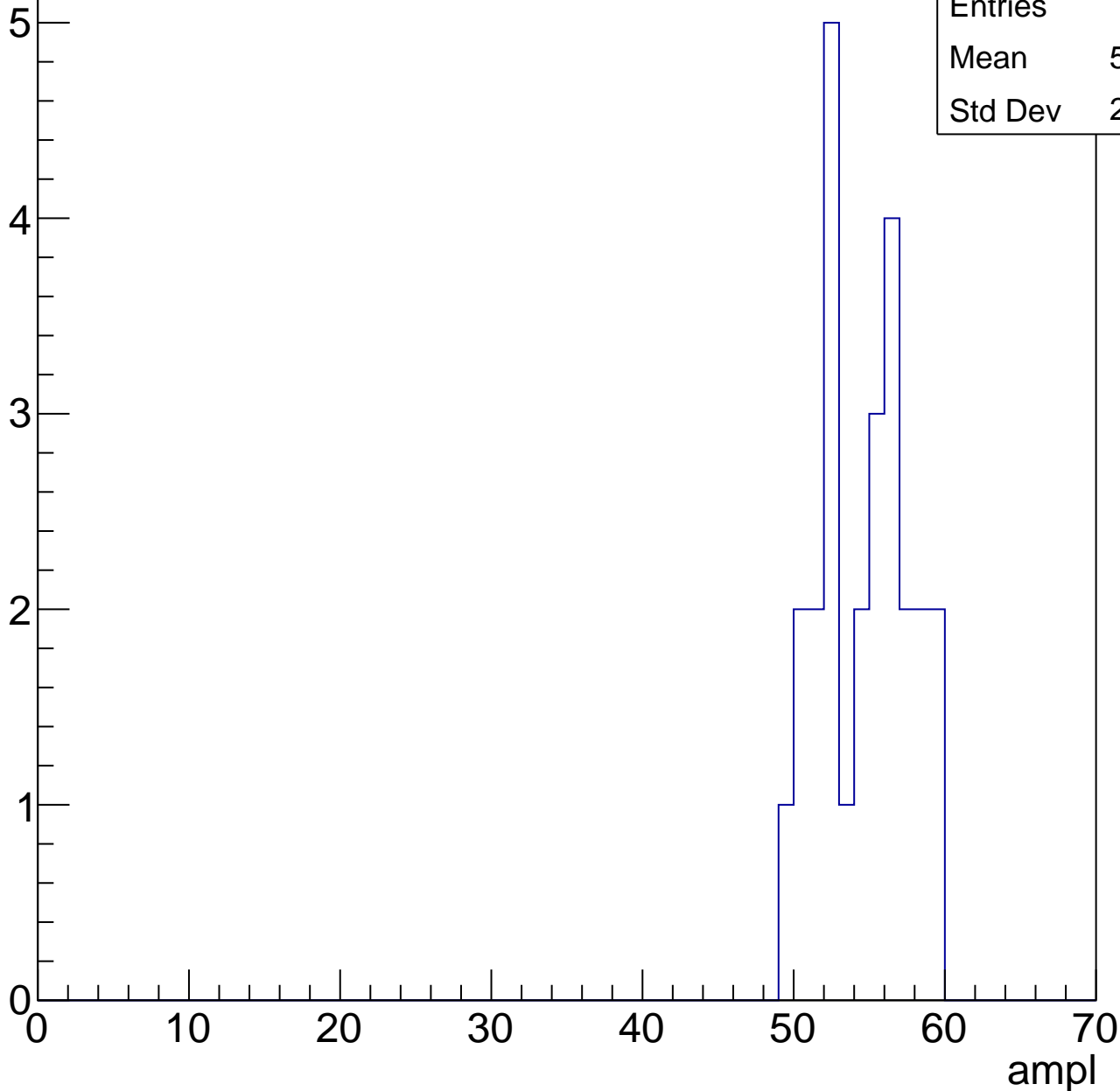


B1L103S, U14-ch8, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

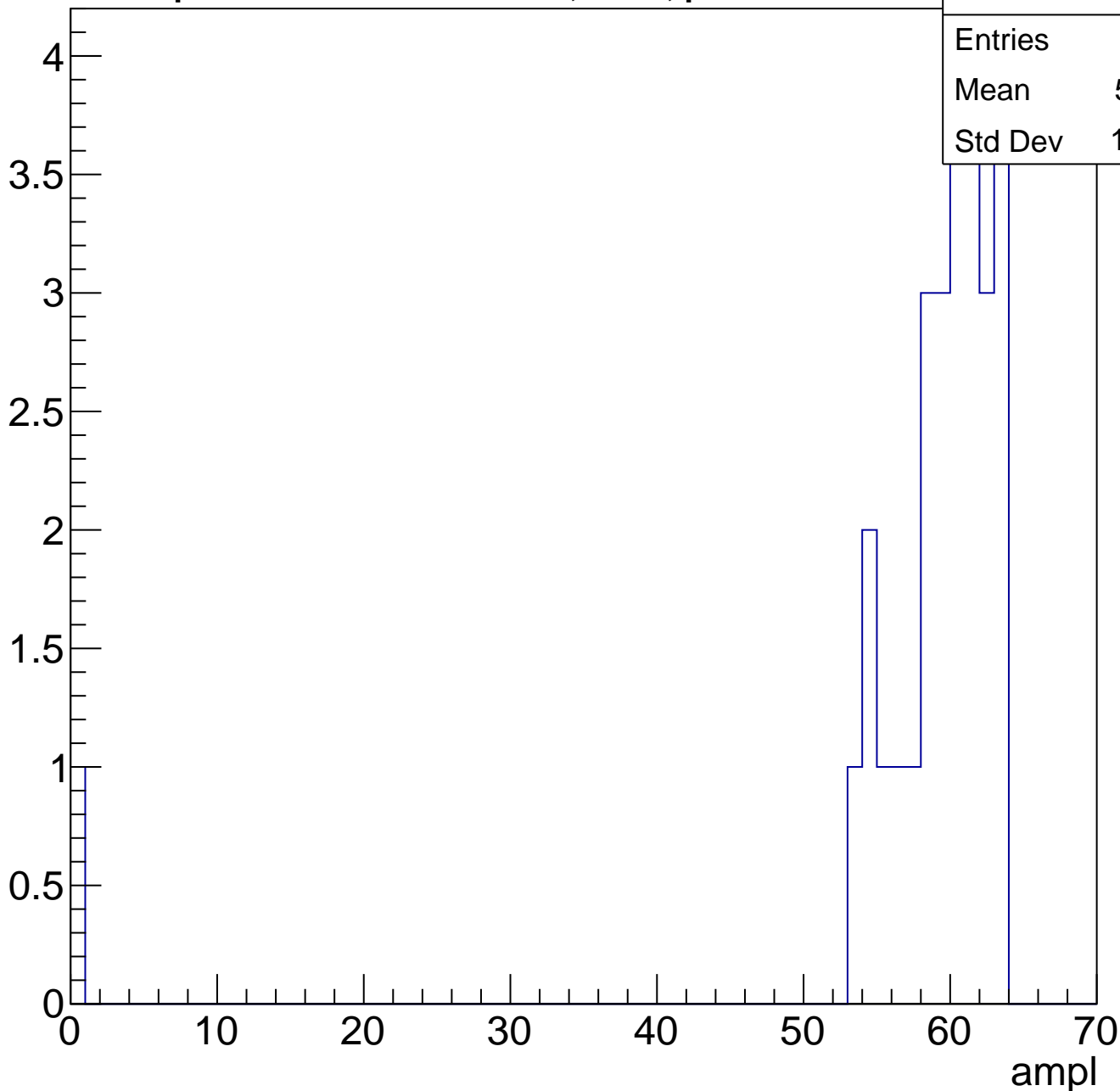
Entries	26
Mean	54.19
Std Dev	2.869



B1L103S, U14-ch8, adc5

calib_packv5_041523_1651.root, FC#0, port C2

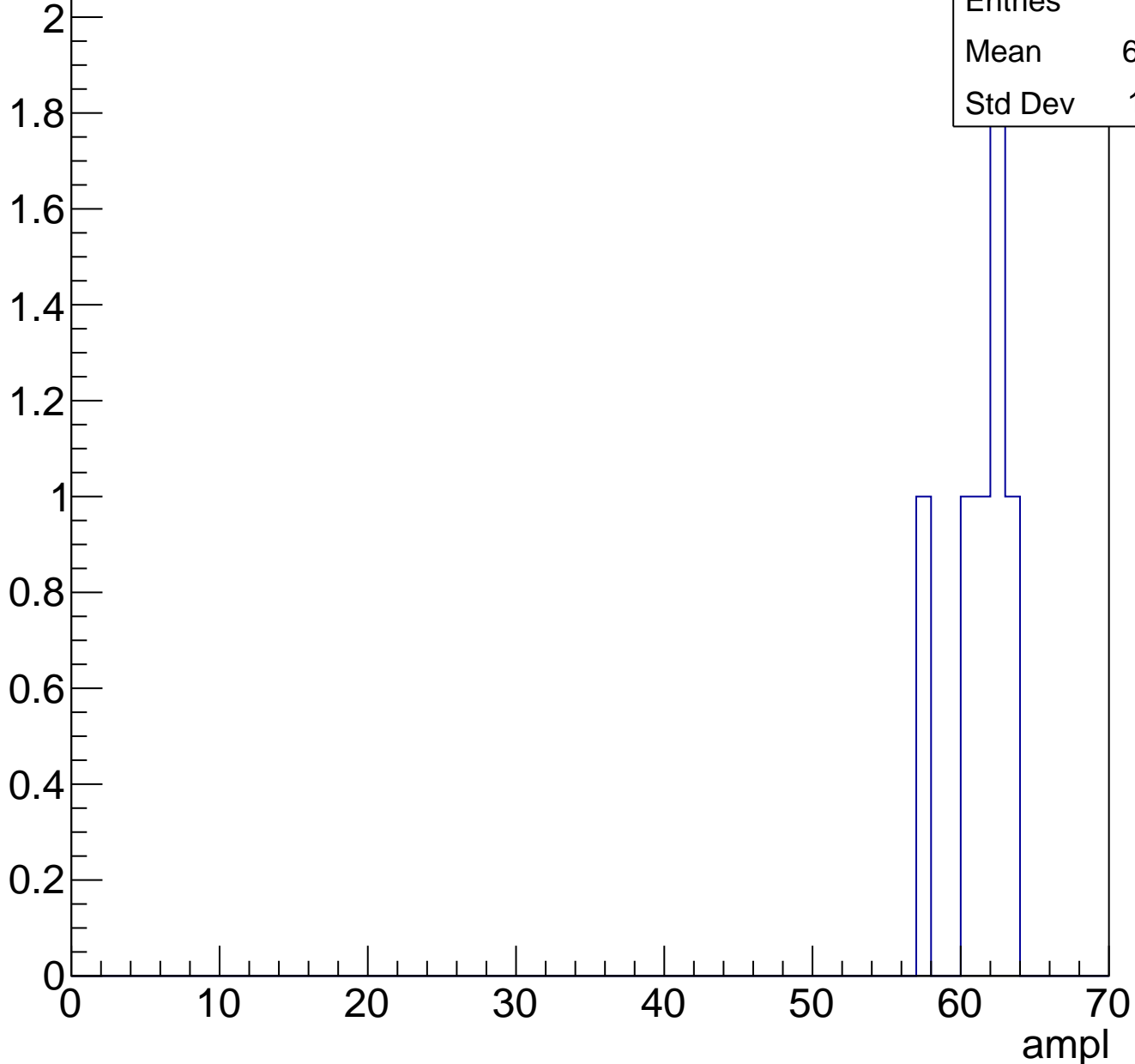
Entry



B1L103S, U14-ch8, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

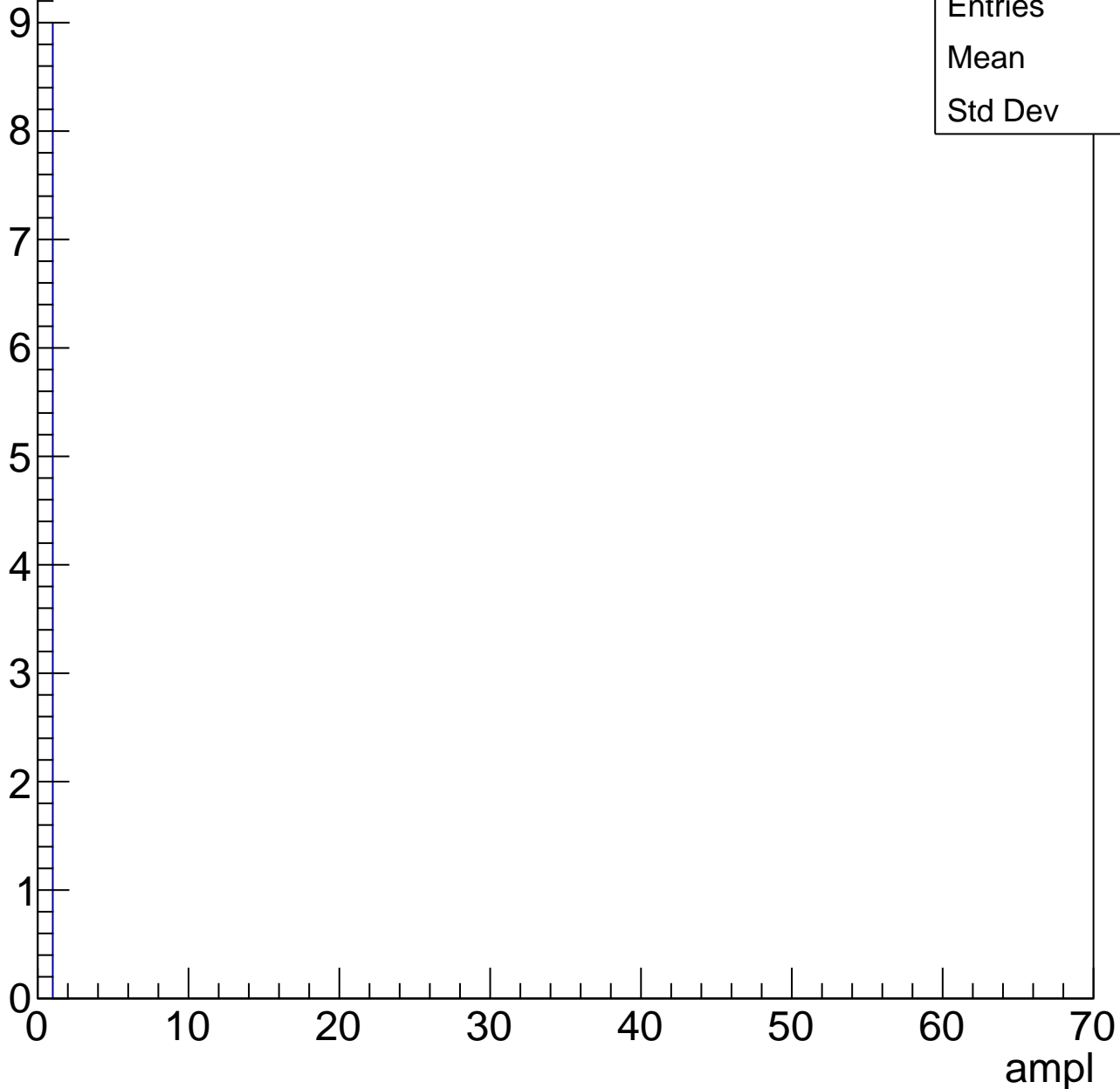


Entries	6
Mean	60.83
Std Dev	1.951

B1L103S, U14-ch8, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

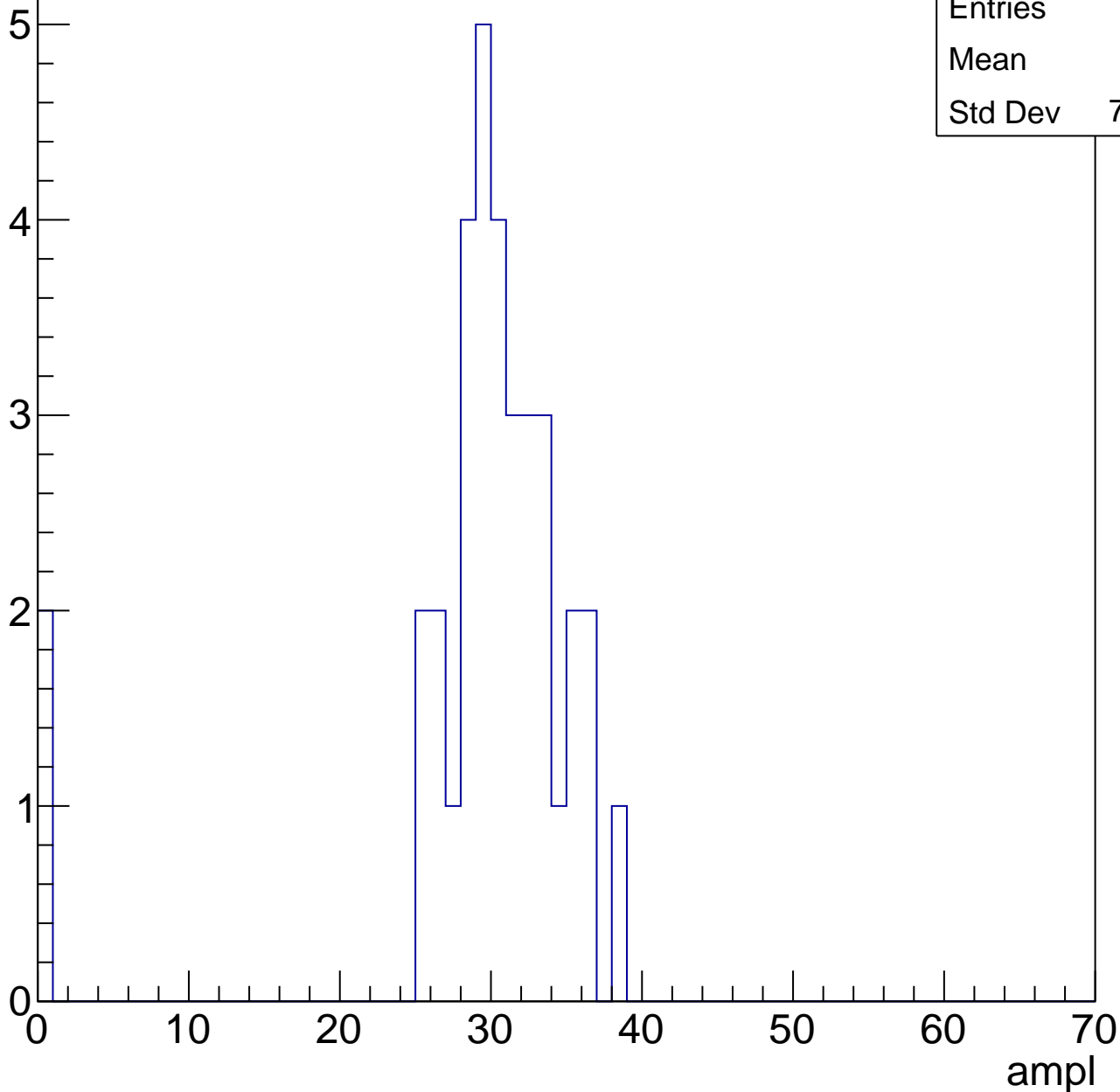


B1L103S, U14-ch9, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

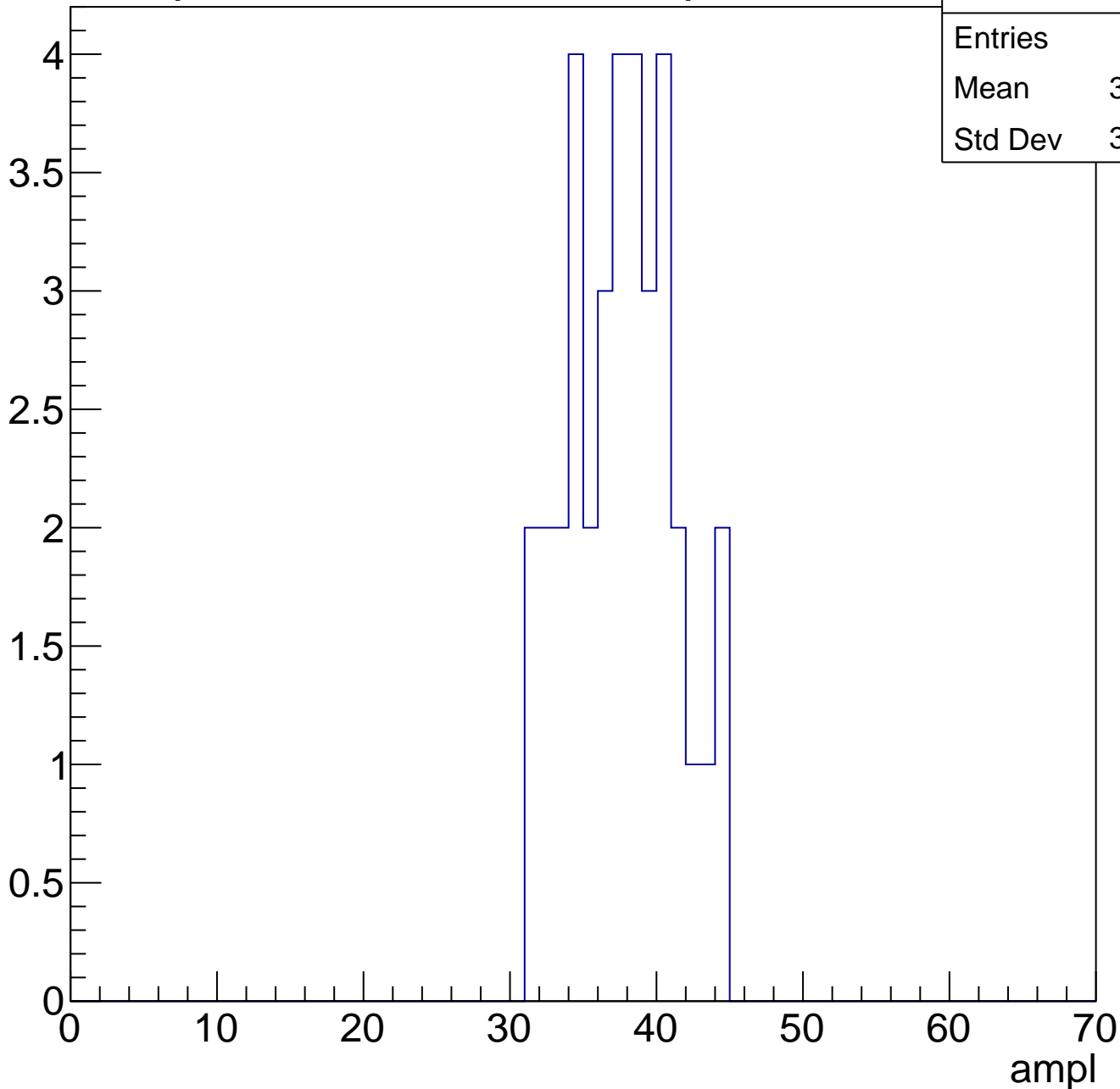
Entries	35
Mean	28.8
Std Dev	7.756



B1L103S, U14-ch9, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

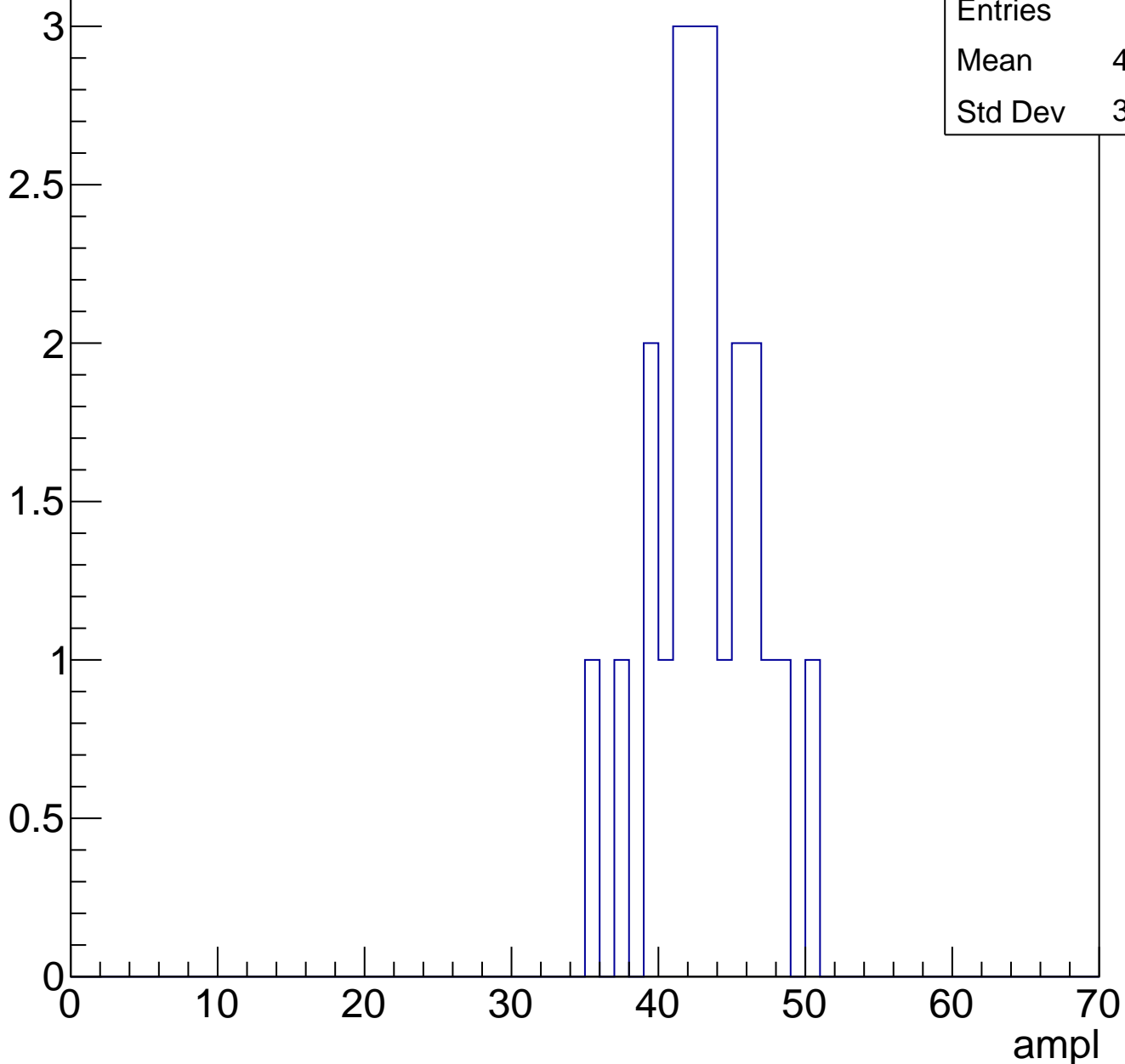


Entries	36
Mean	37.17
Std Dev	3.508

B1L103S, U14-ch9, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry



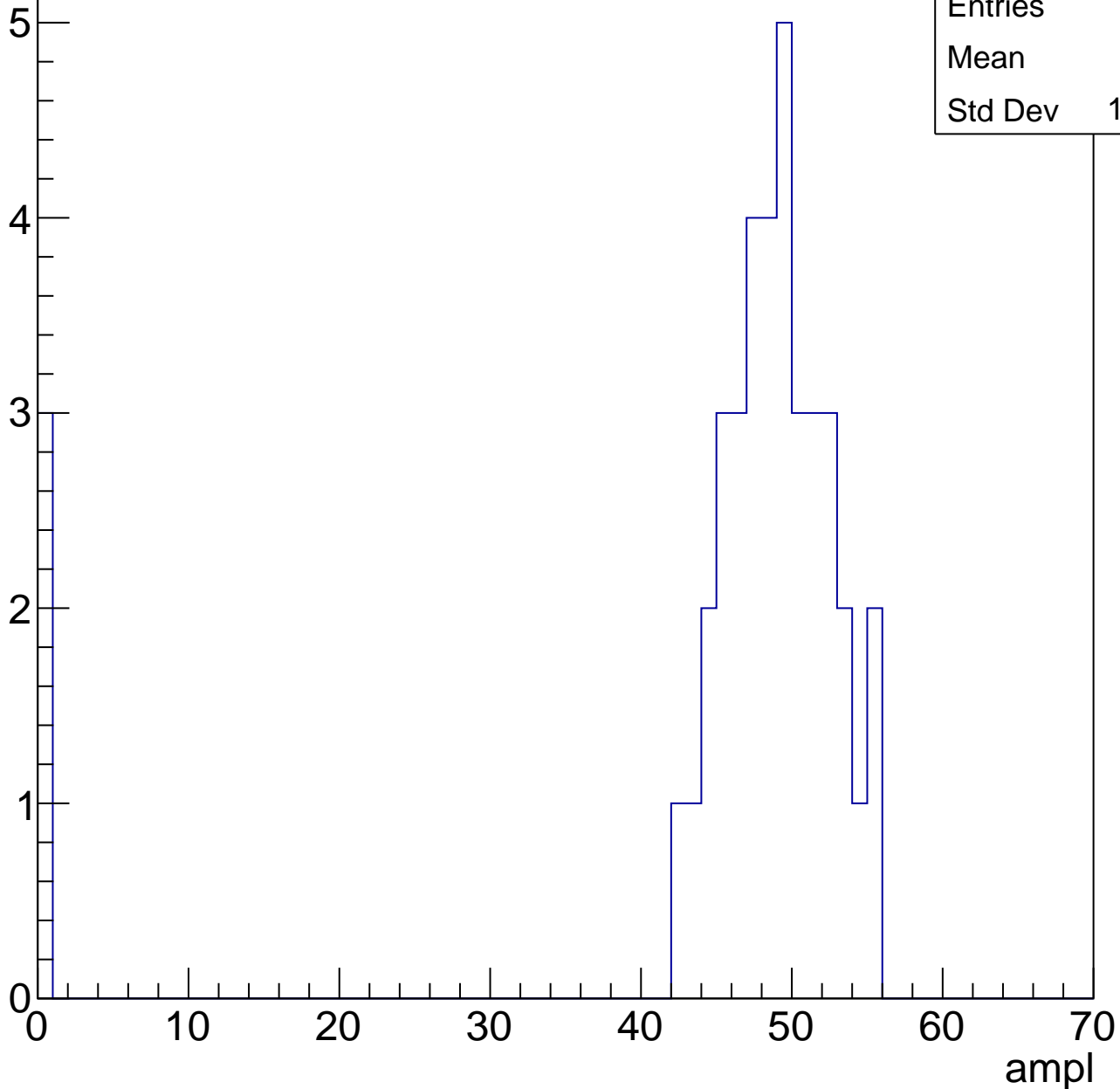
Entries	22
Mean	42.68
Std Dev	3.508

B1L103S, U14-ch9, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	45
Std Dev	13.19

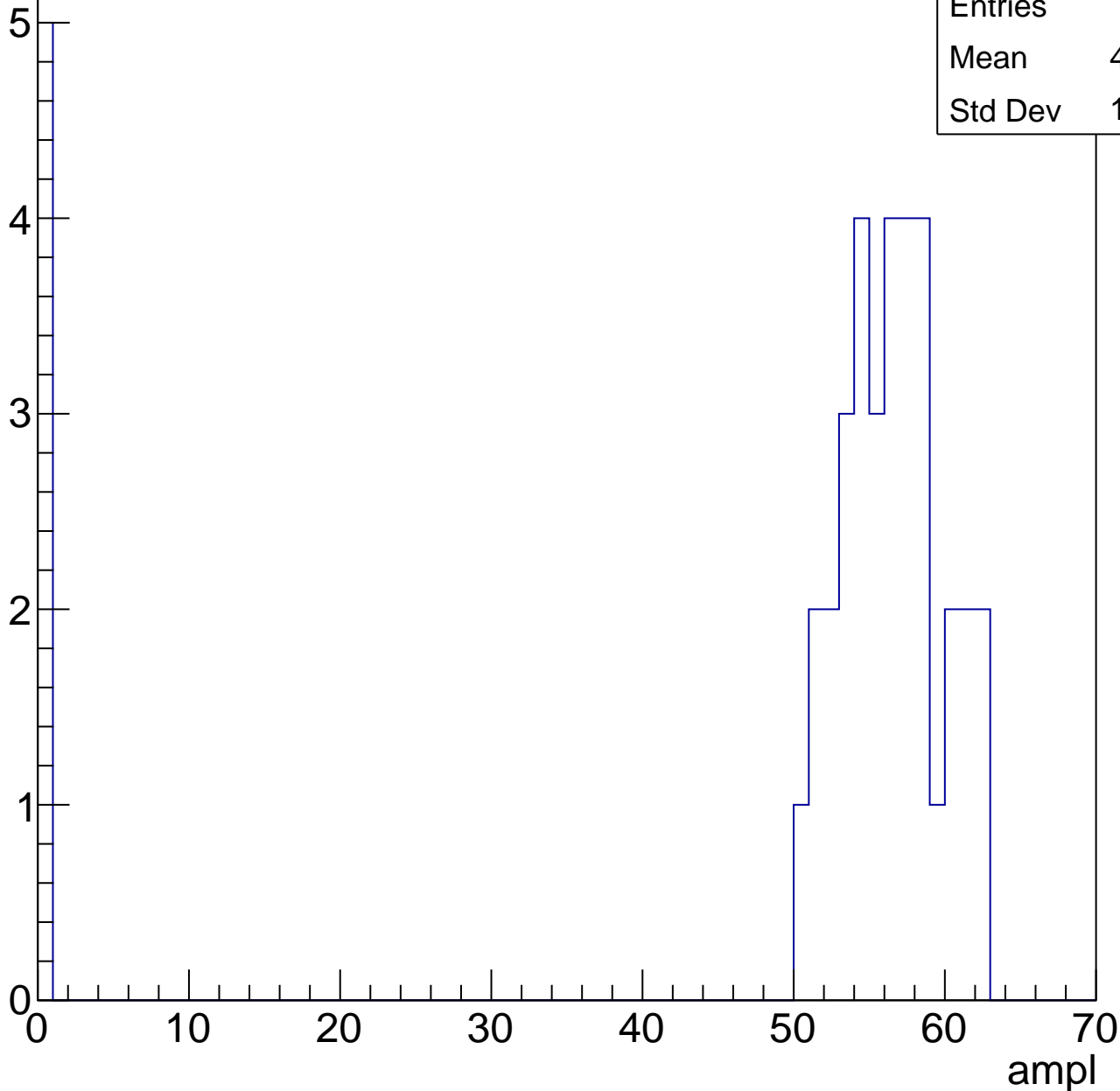


B1L103S, U14-ch9, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	48.85
Std Dev	18.97



B1L103S, U14-ch9, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

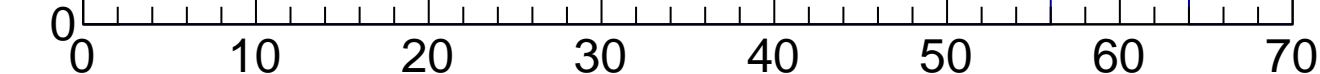
50

60

70

ampl

Entries	16
Mean	60.06
Std Dev	1.952



B1L103S, U14-ch9, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch9, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	8
Mean	0
Std Dev	0

8
7
6
5
4
3
2
1
0

0 10 20 30 40 50 60 70

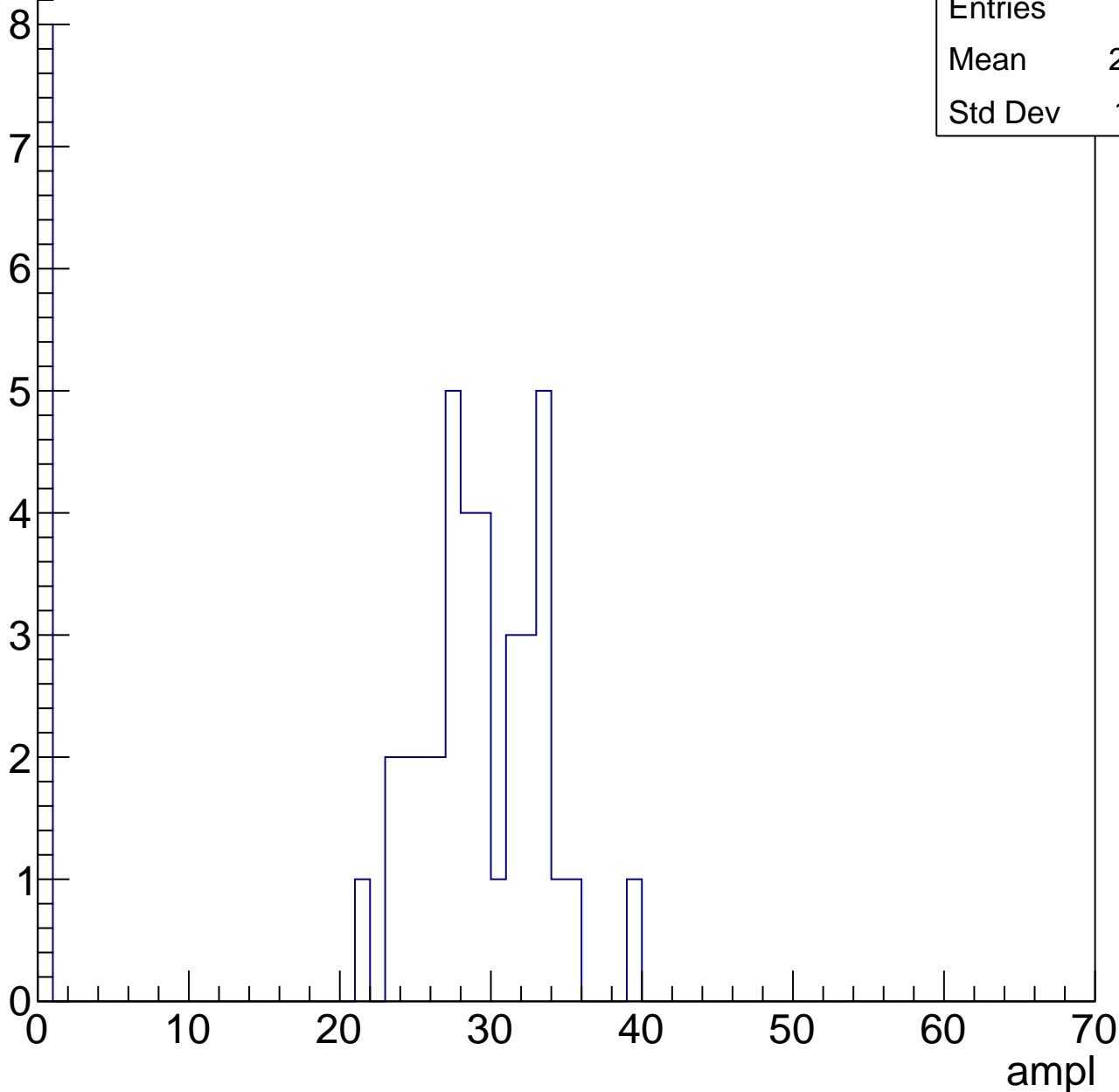
ampl

B1L103S, U14-ch10, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

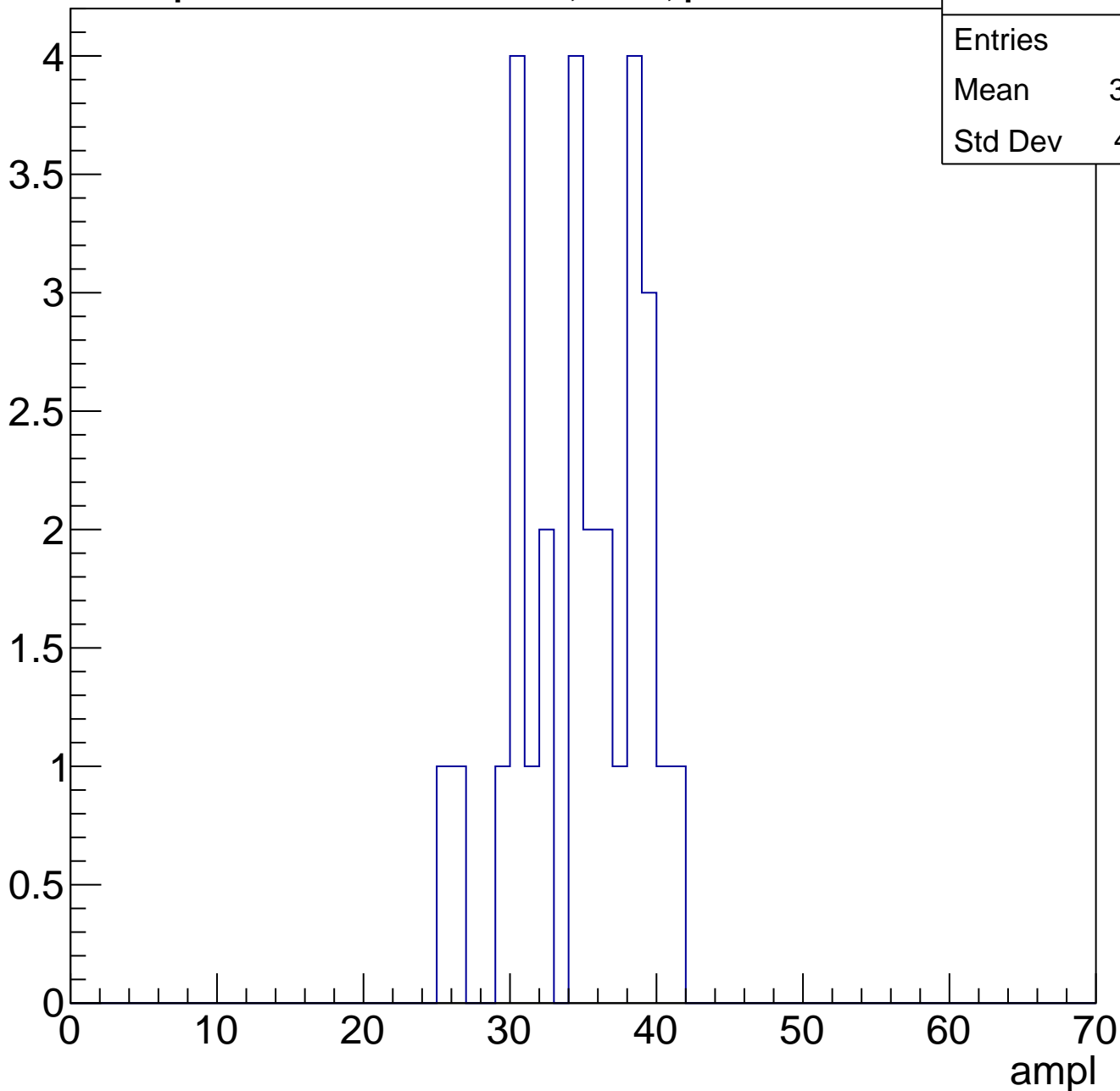
Entries	45
Mean	23.82
Std Dev	11.61



B1L103S, U14-ch10, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

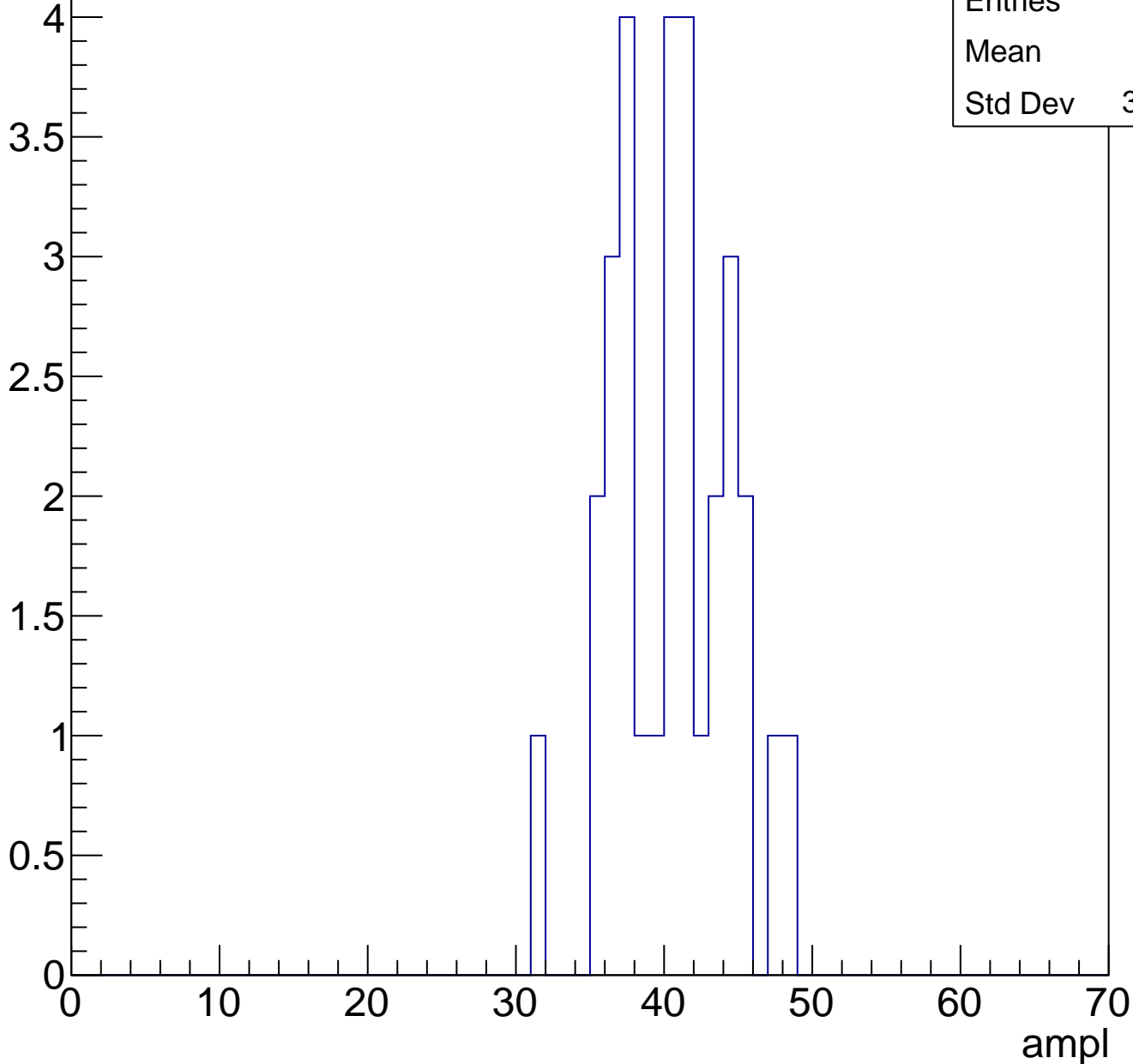


Entries	28
Mean	34.29
Std Dev	4.191

B1L103S, U14-ch10, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

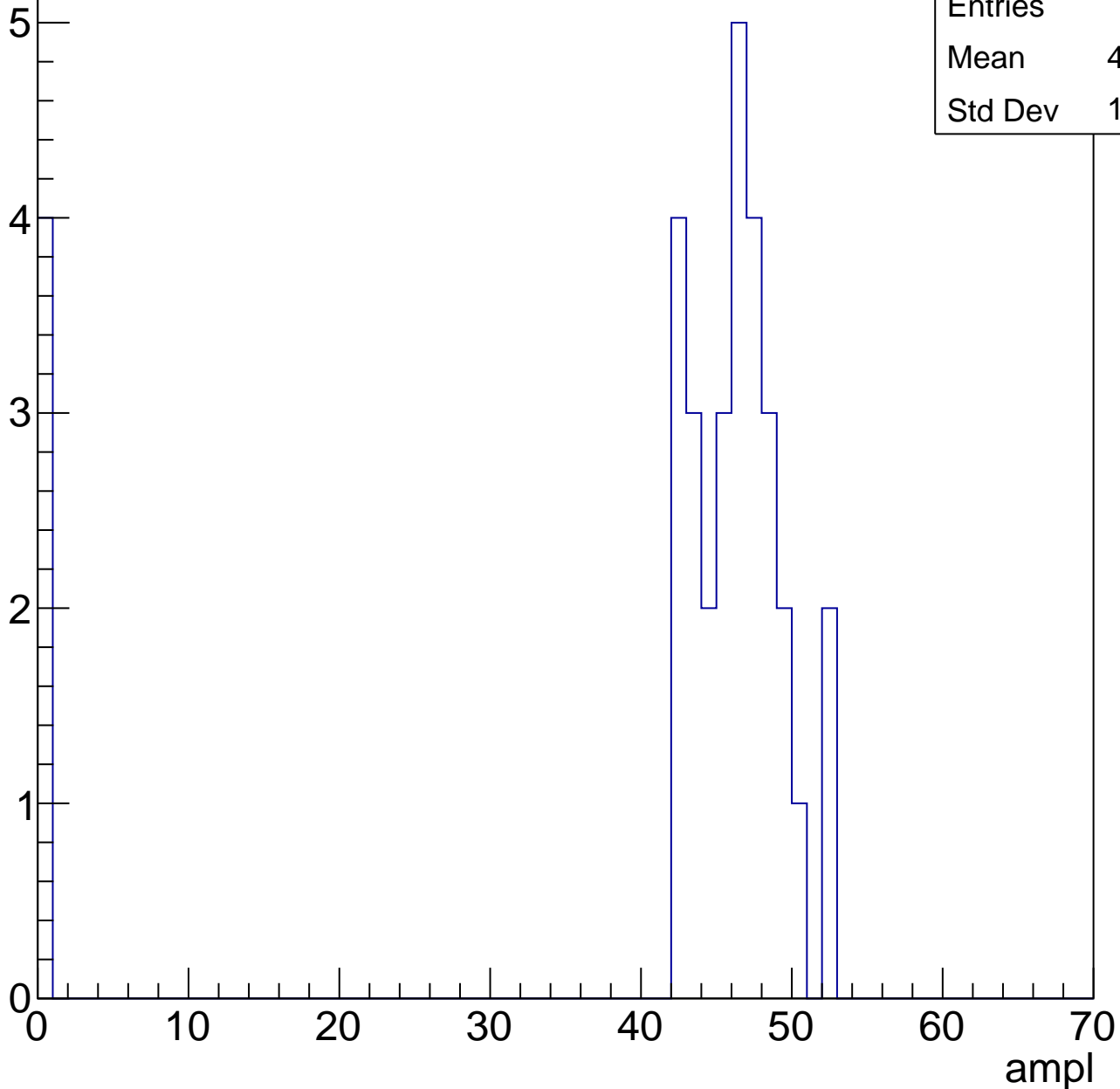


B1L103S, U14-ch10, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	33
Mean	40.42
Std Dev	15.24

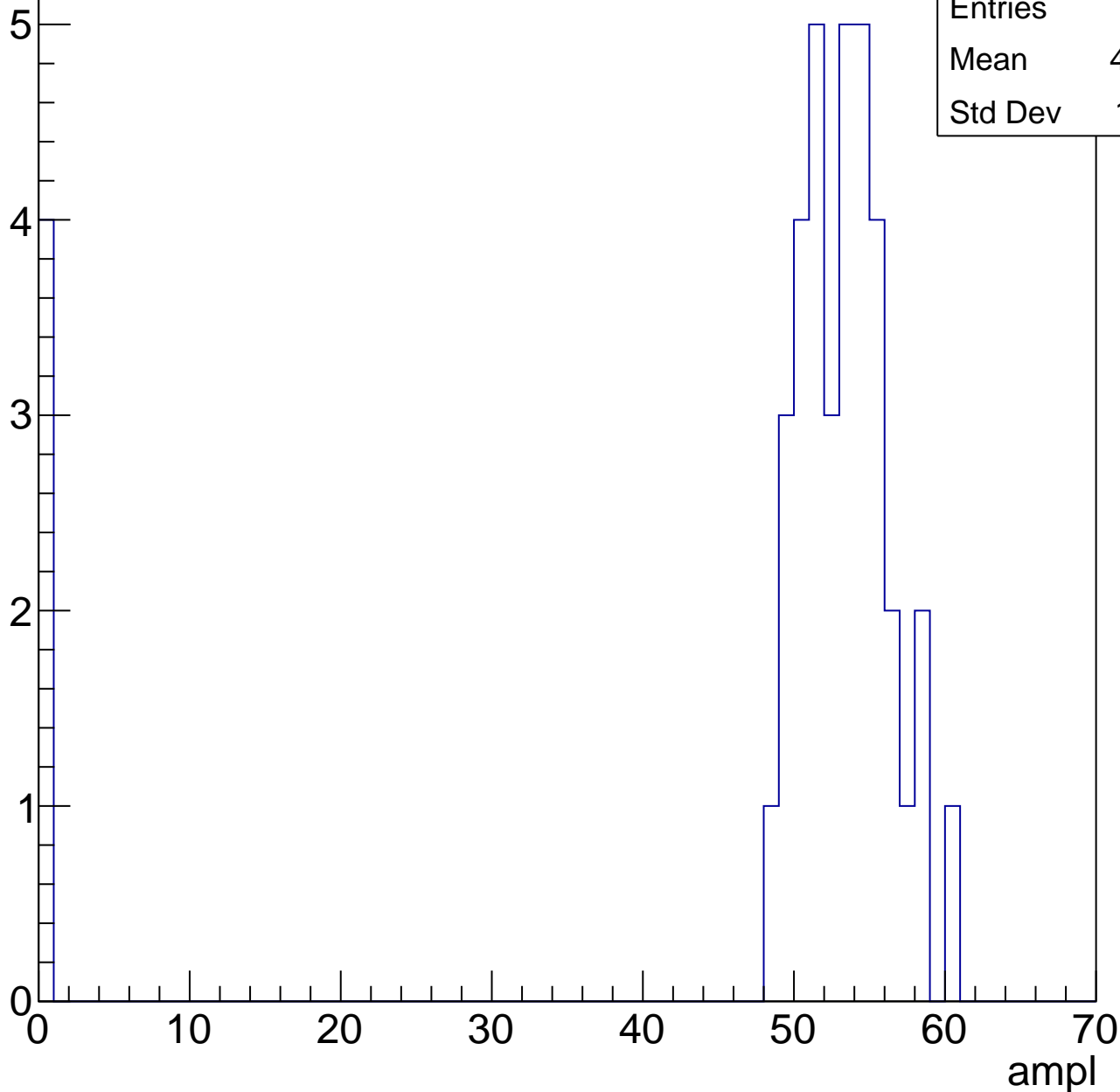


B1L103S, U14-ch10, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	47.65
Std Dev	16.11

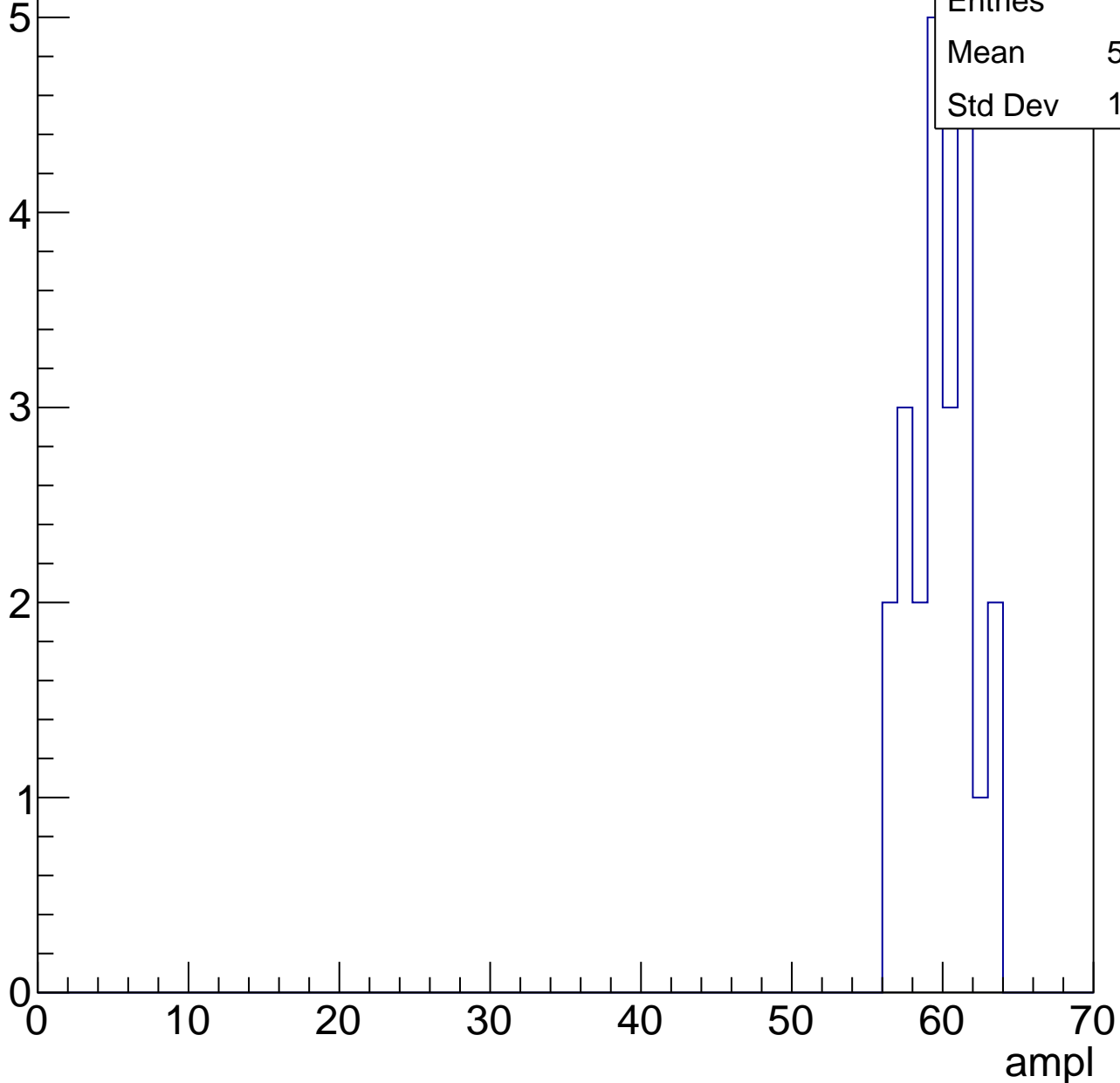


B1L103S, U14-ch10, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	23
Mean	59.43
Std Dev	1.996



B1L103S, U14-ch10, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

ampl

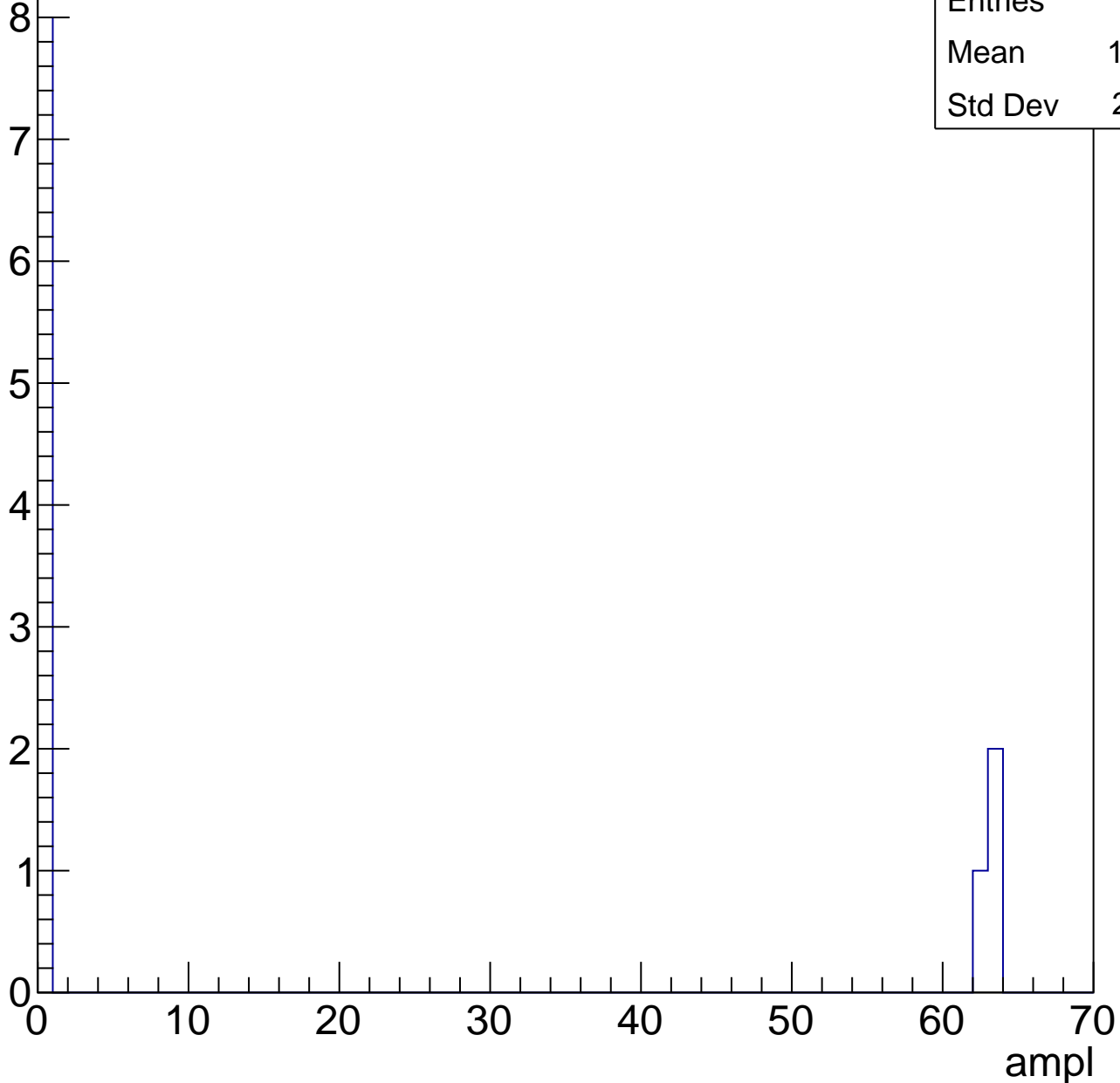
Entries	9
Mean	59.44
Std Dev	2.833

B1L103S, U14-ch10, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	11
Mean	17.09
Std Dev	27.91

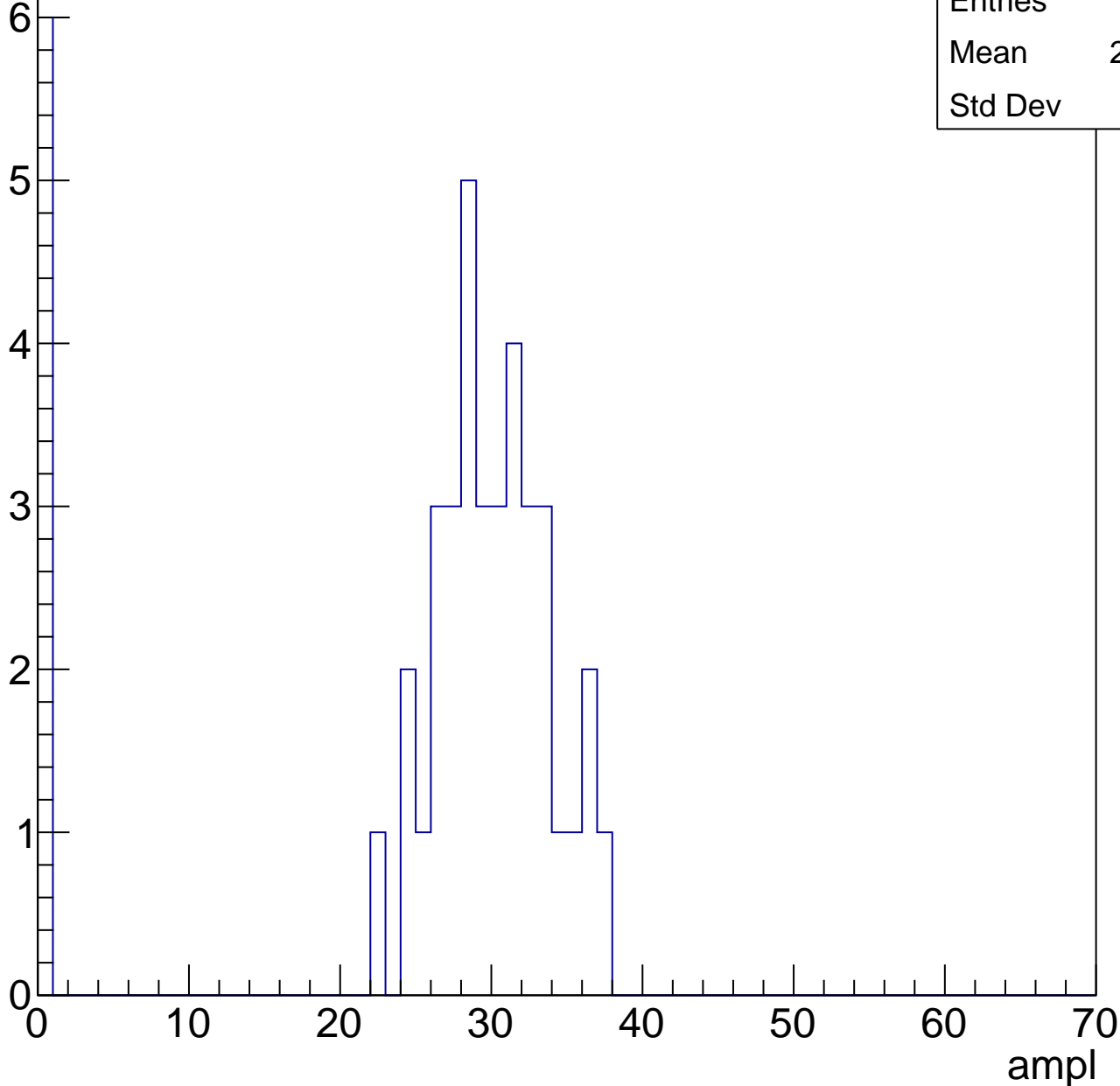


B1L103S, U14-ch11, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

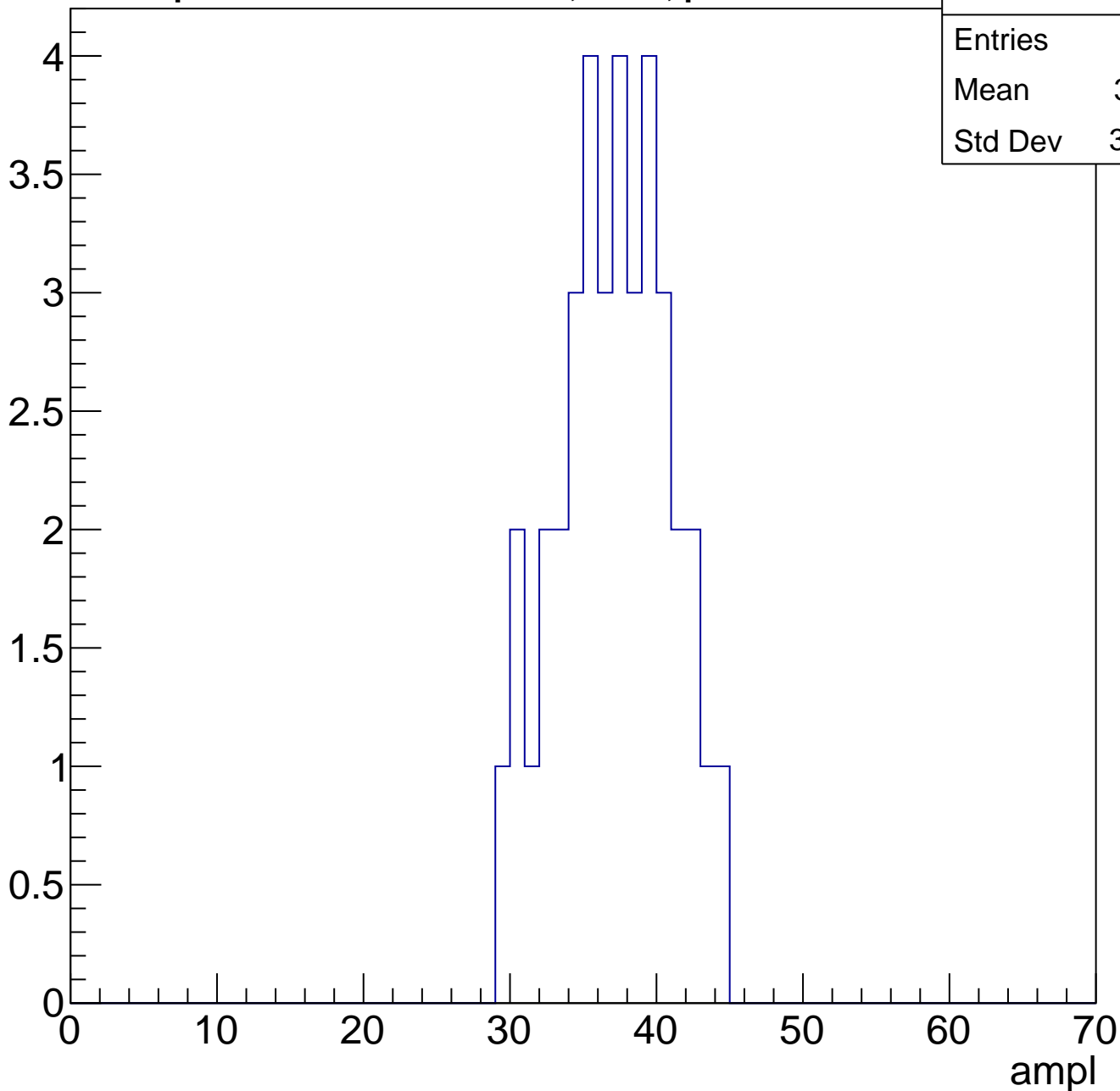
Entries	42
Mean	25.43
Std Dev	10.9



B1L103S, U14-ch11, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry



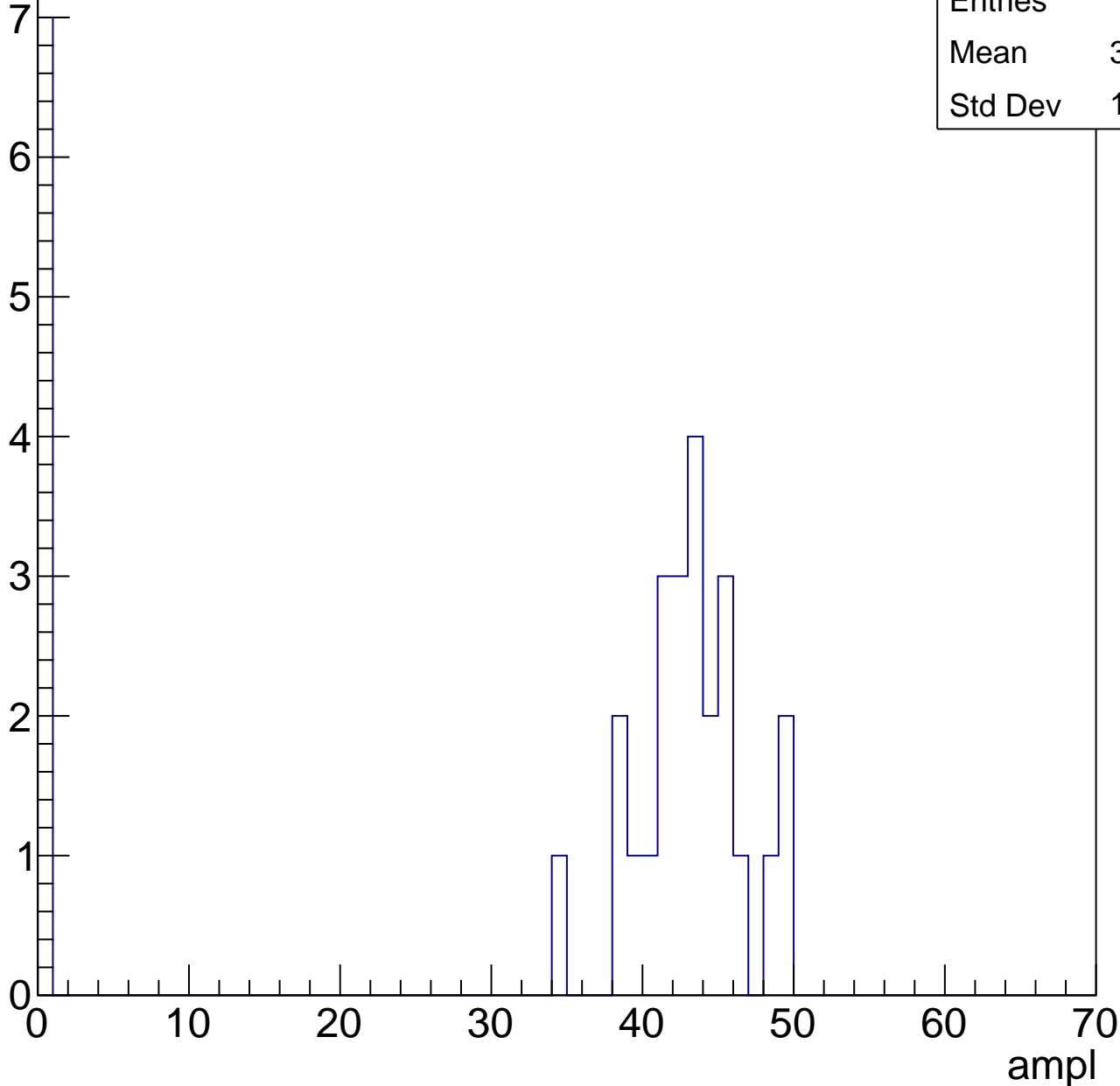
Entries	38
Mean	36.61
Std Dev	3.745

B1L103S, U14-ch11, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	31
Mean	33.06
Std Dev	18.12

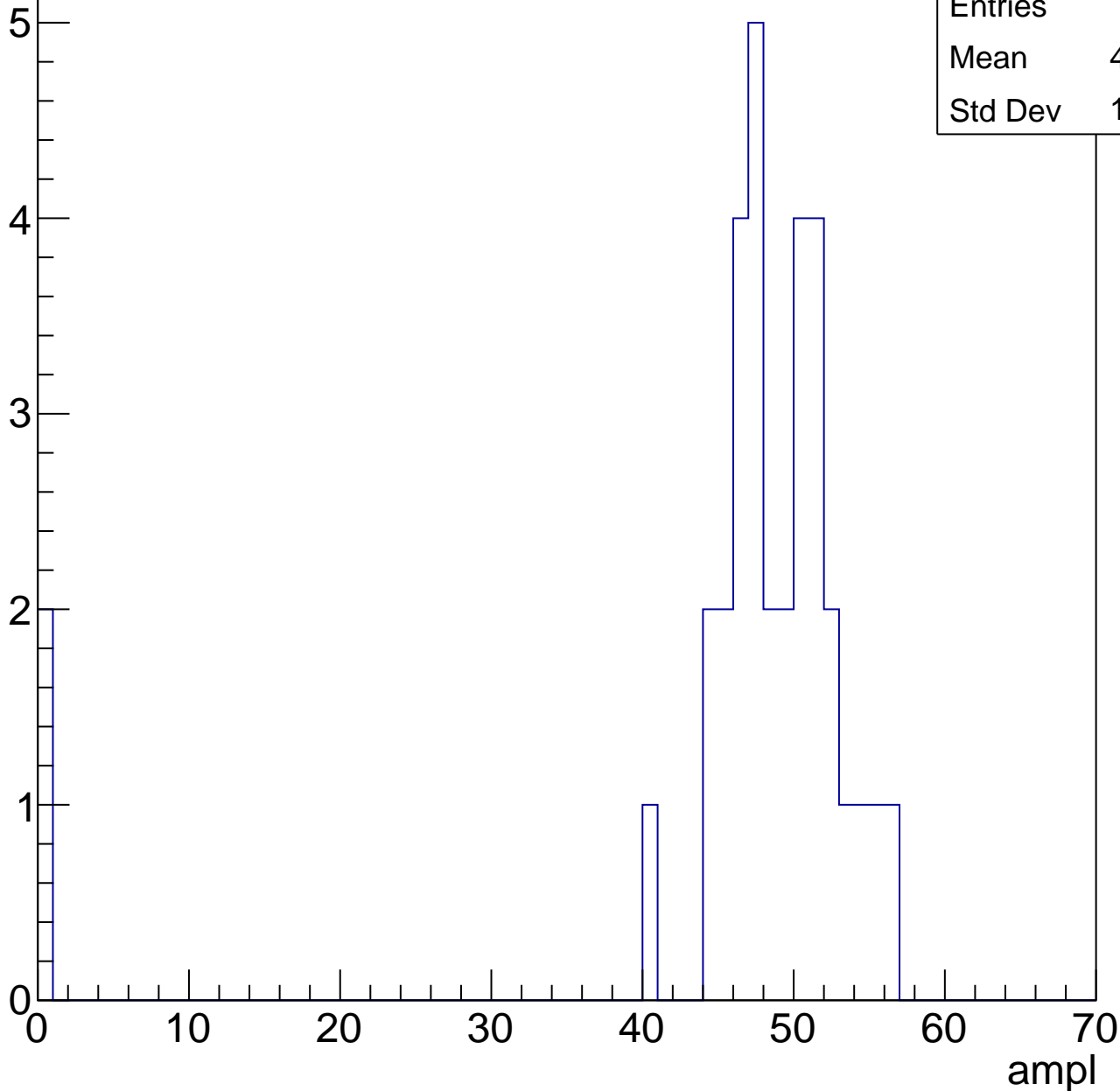


B1L103S, U14-ch11, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

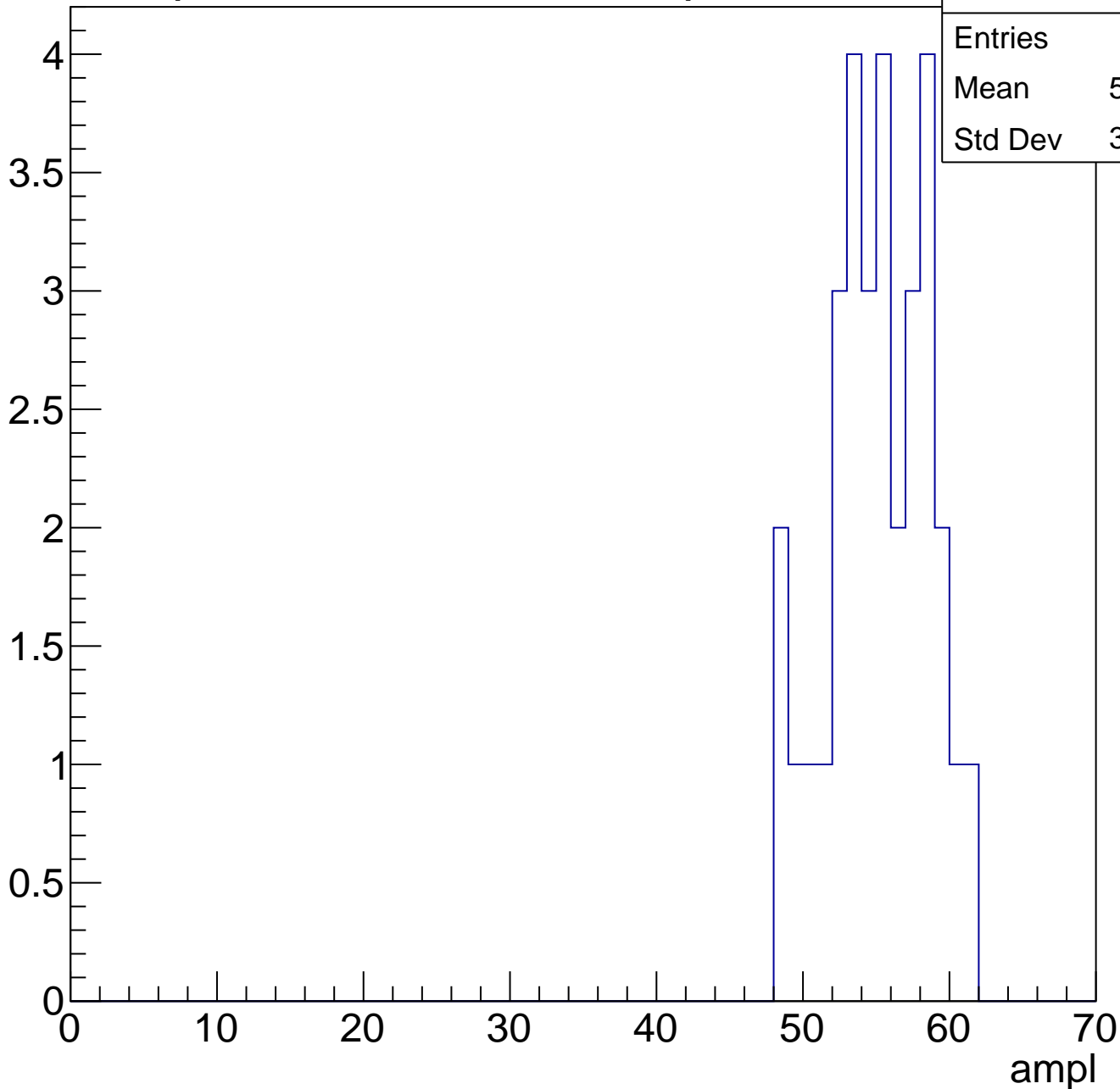
Entries	34
Mean	45.79
Std Dev	11.93



B1L103S, U14-ch11, adc4

calib_packv5_041523_1651.root, FC#0, port C2

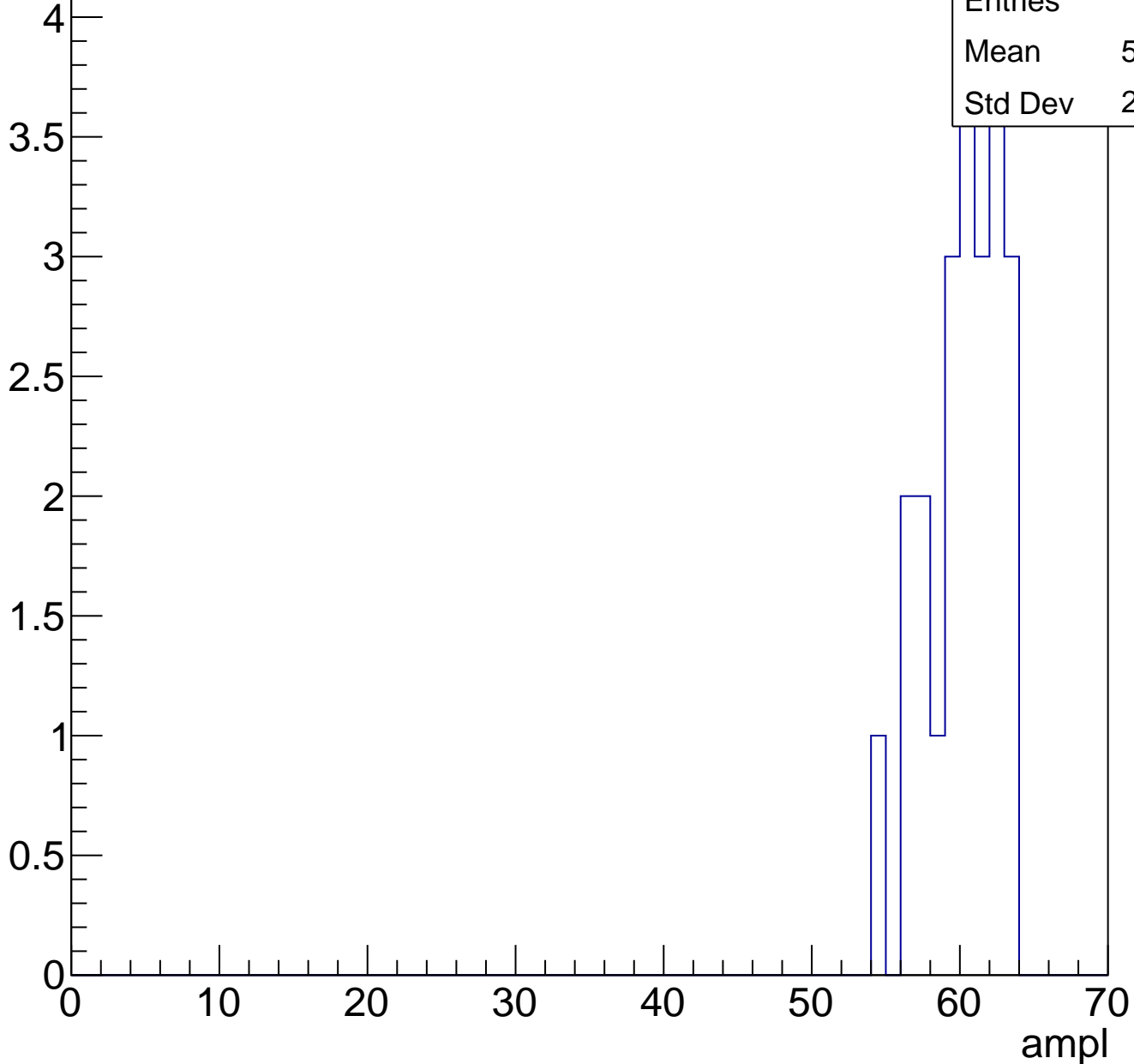
Entry



B1L103S, U14-ch11, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch11, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



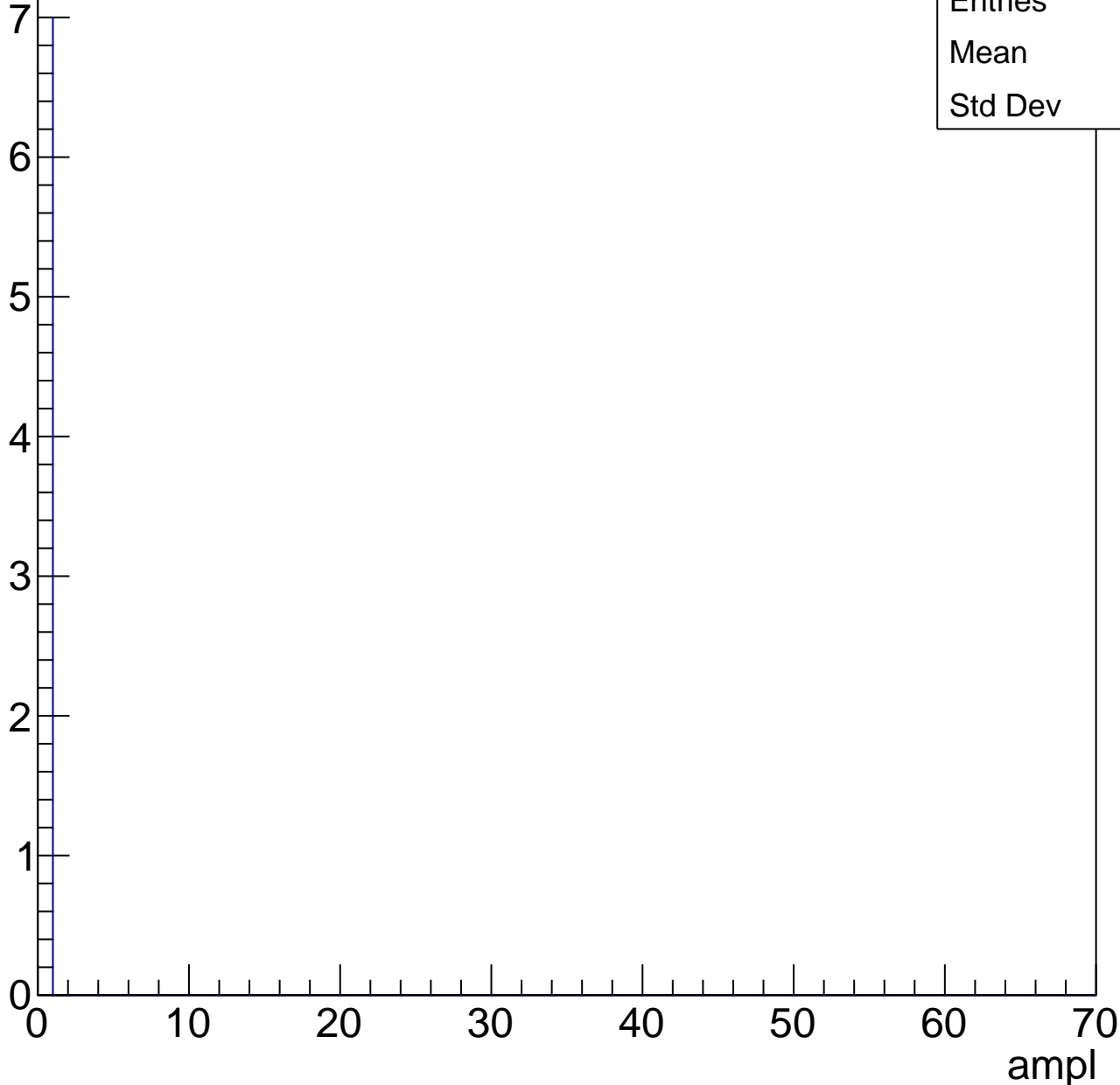
Entries	5
Mean	49.8
Std Dev	24.91

B1L103S, U14-ch11, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	7
Mean	0
Std Dev	0



B1L103S, U14-ch12, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

8

6

4

2

0

0

10

20

30

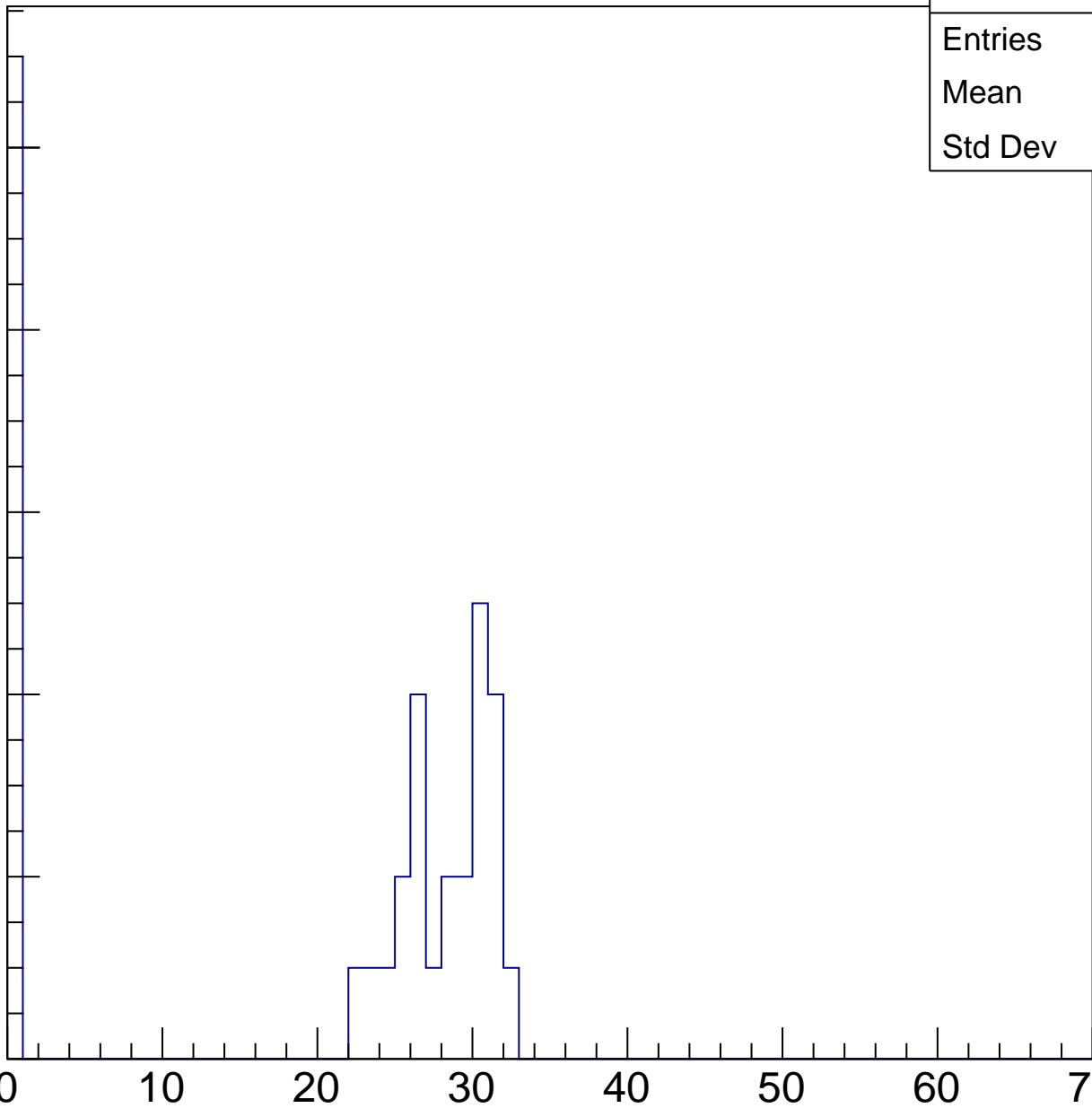
40

50

60

ampl

Entries	35
Mean	19.14
Std Dev	13.16

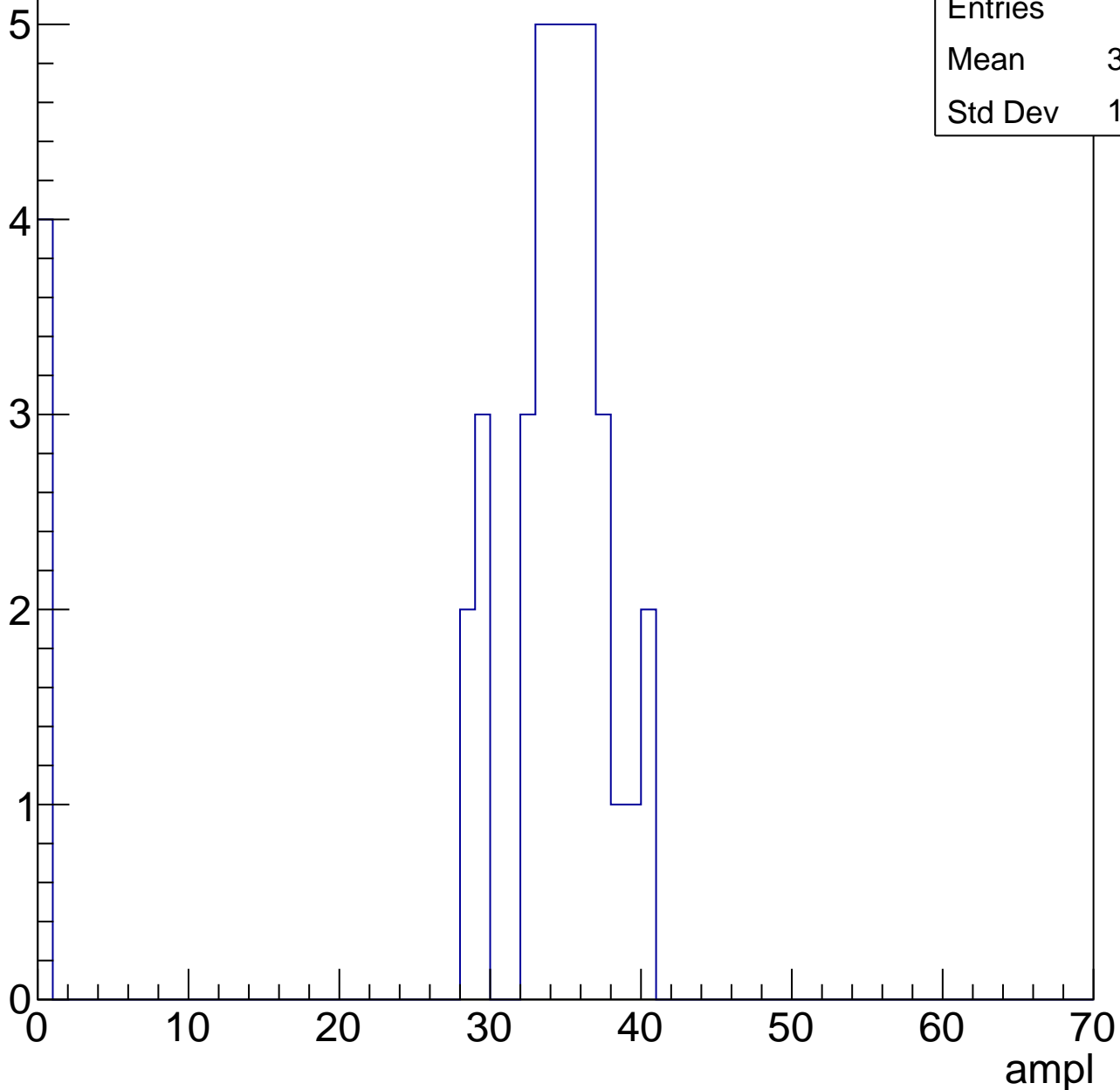


B1L103S, U14-ch12, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	30.69
Std Dev	10.77

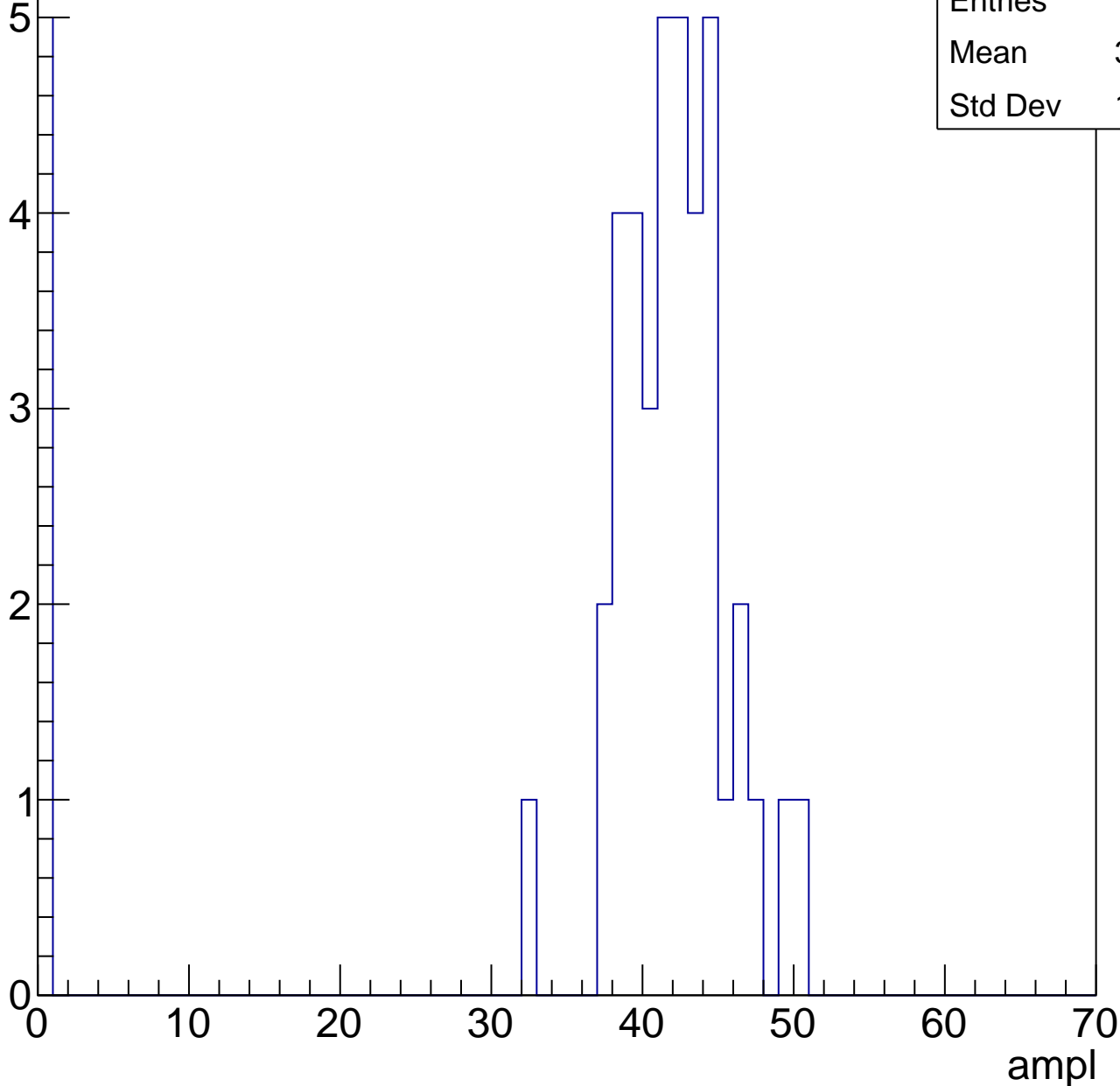


B1L103S, U14-ch12, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	44
Mean	36.91
Std Dev	13.61

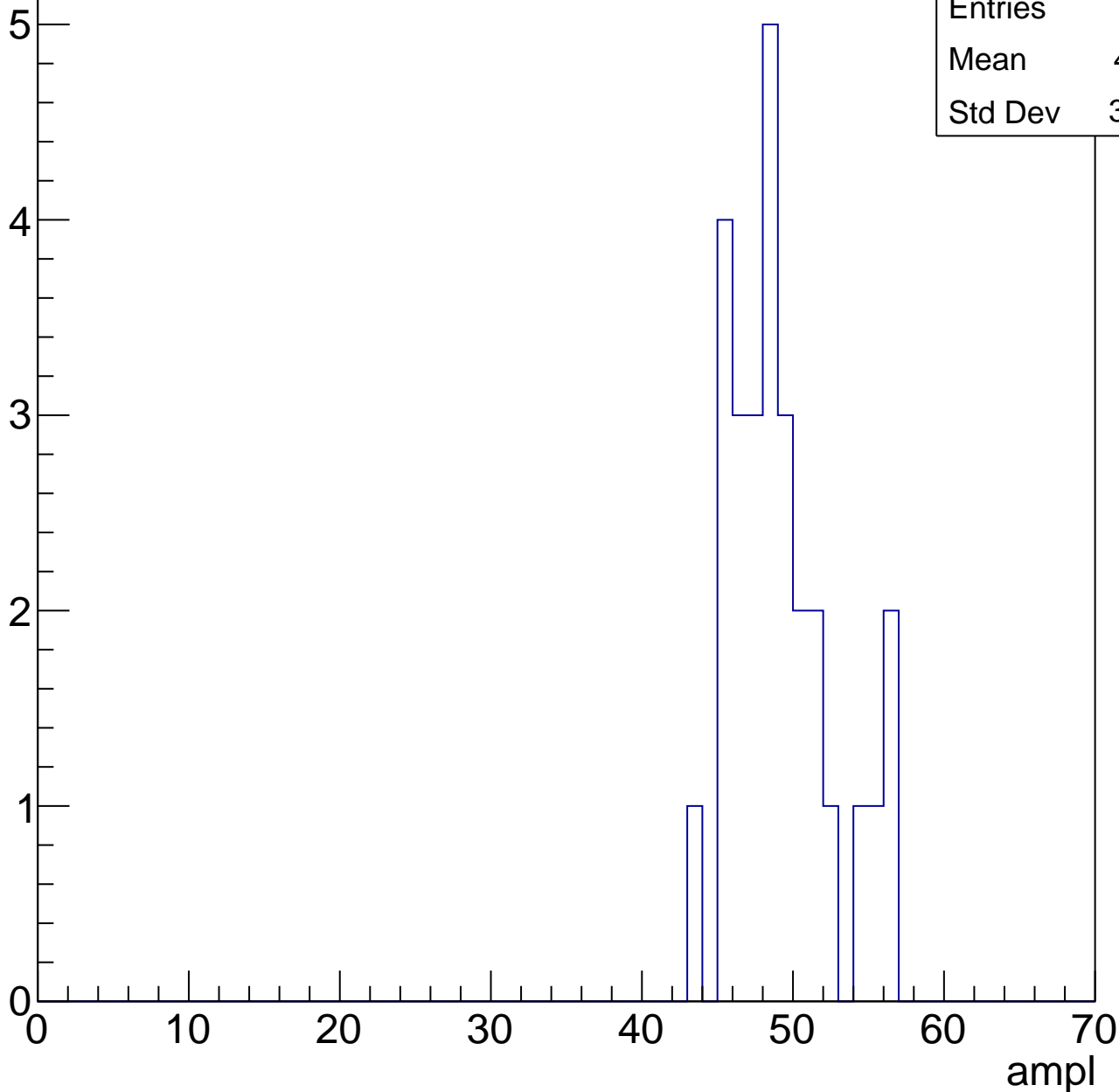


B1L103S, U14-ch12, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

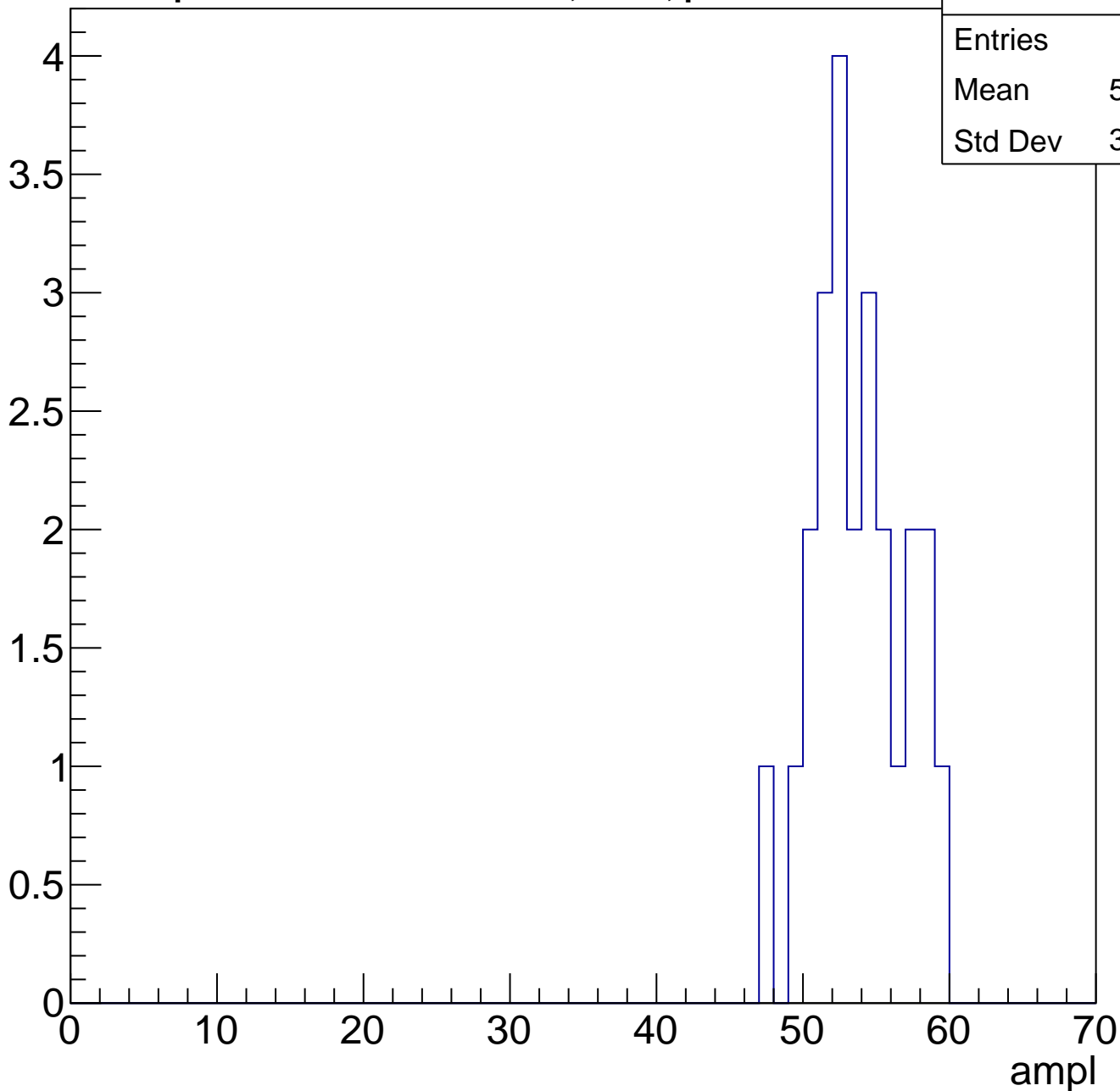
Entries	28
Mean	48.71
Std Dev	3.379



B1L103S, U14-ch12, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



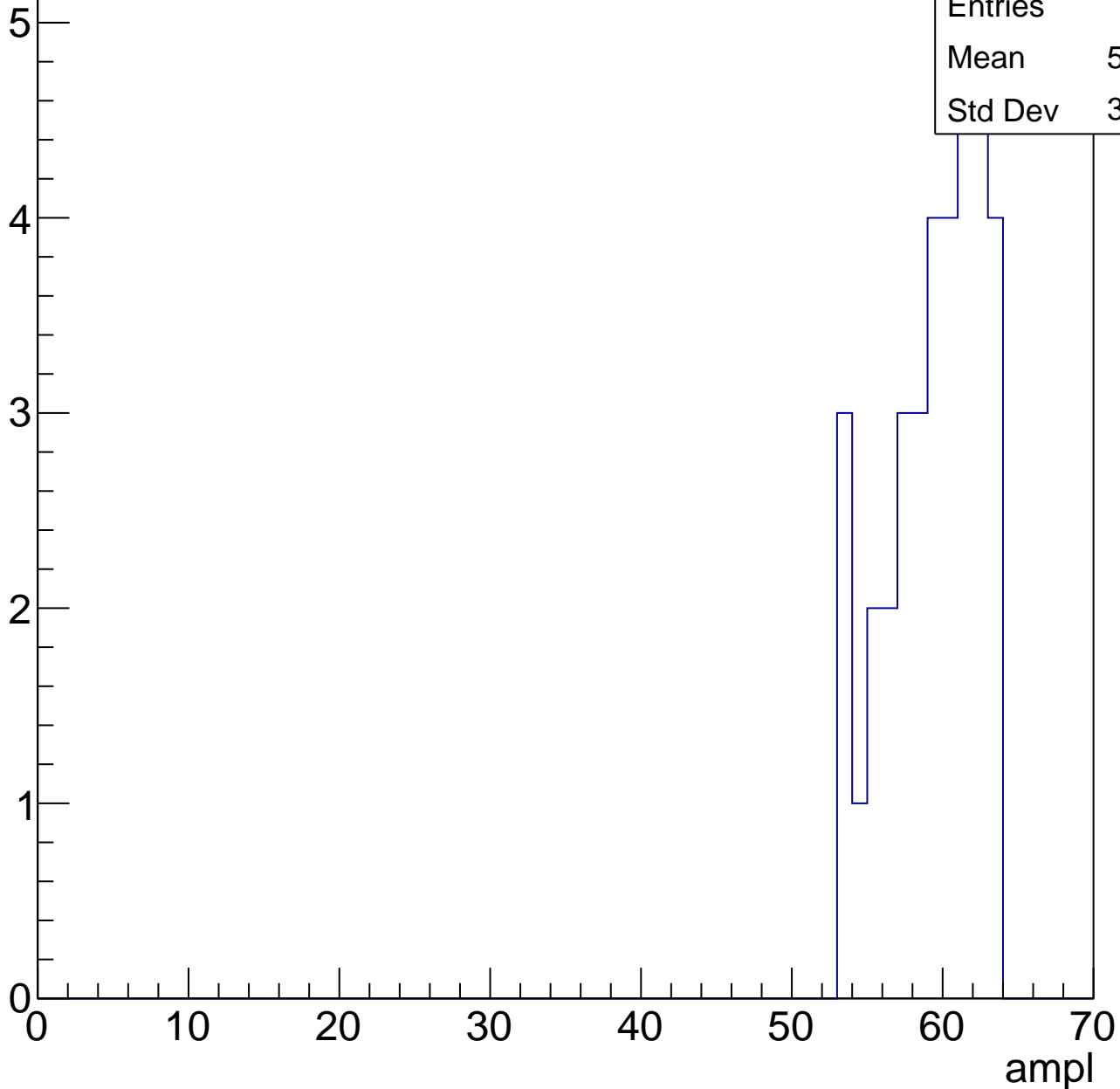
Entries	24
Mean	53.33
Std Dev	3.037

B1L103S, U14-ch12, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

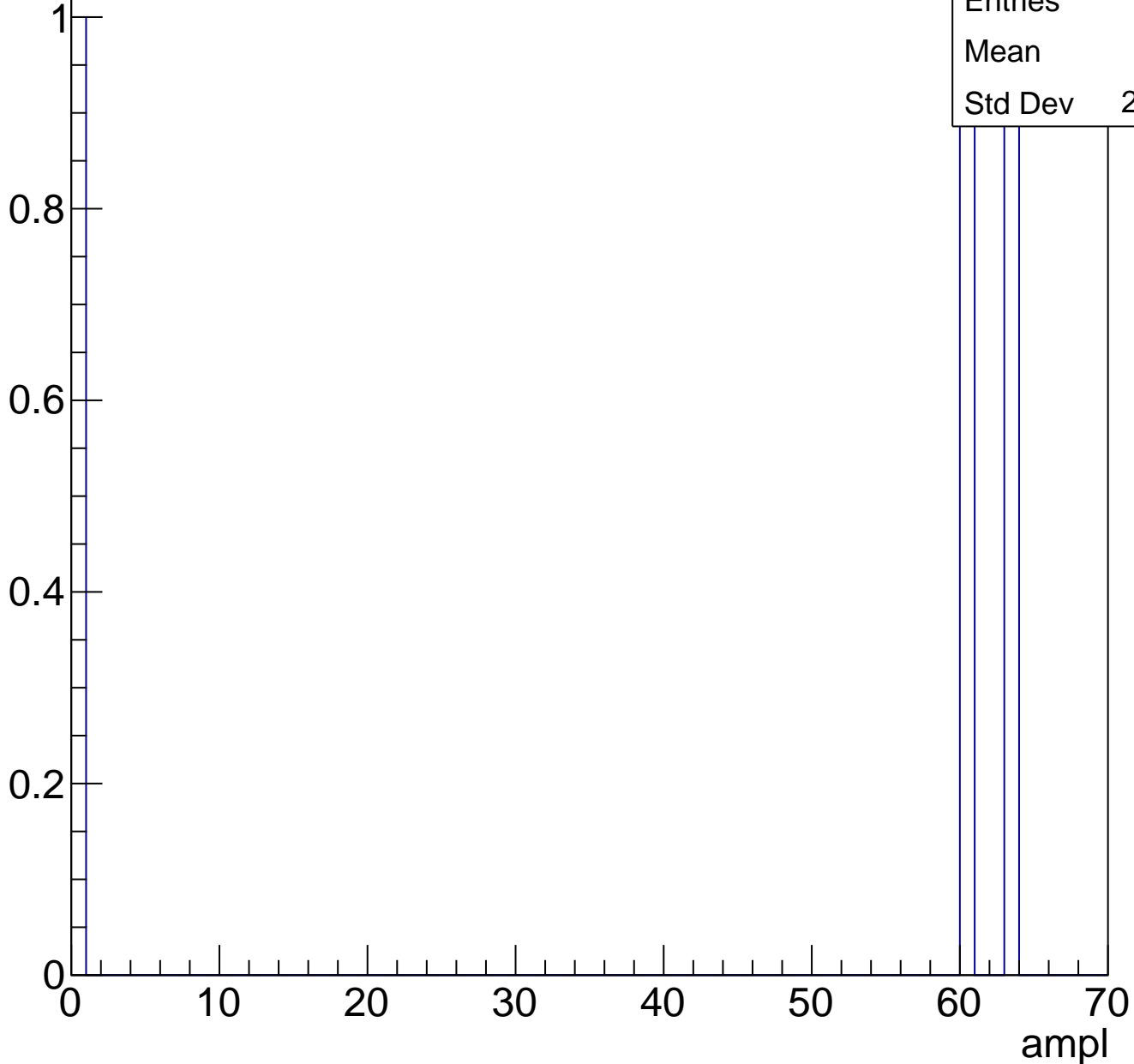
Entries	36
Mean	58.97
Std Dev	3.032



B1L103S, U14-ch12, adc6

calib_packv5_041523_1651.root, FC#0, port C2

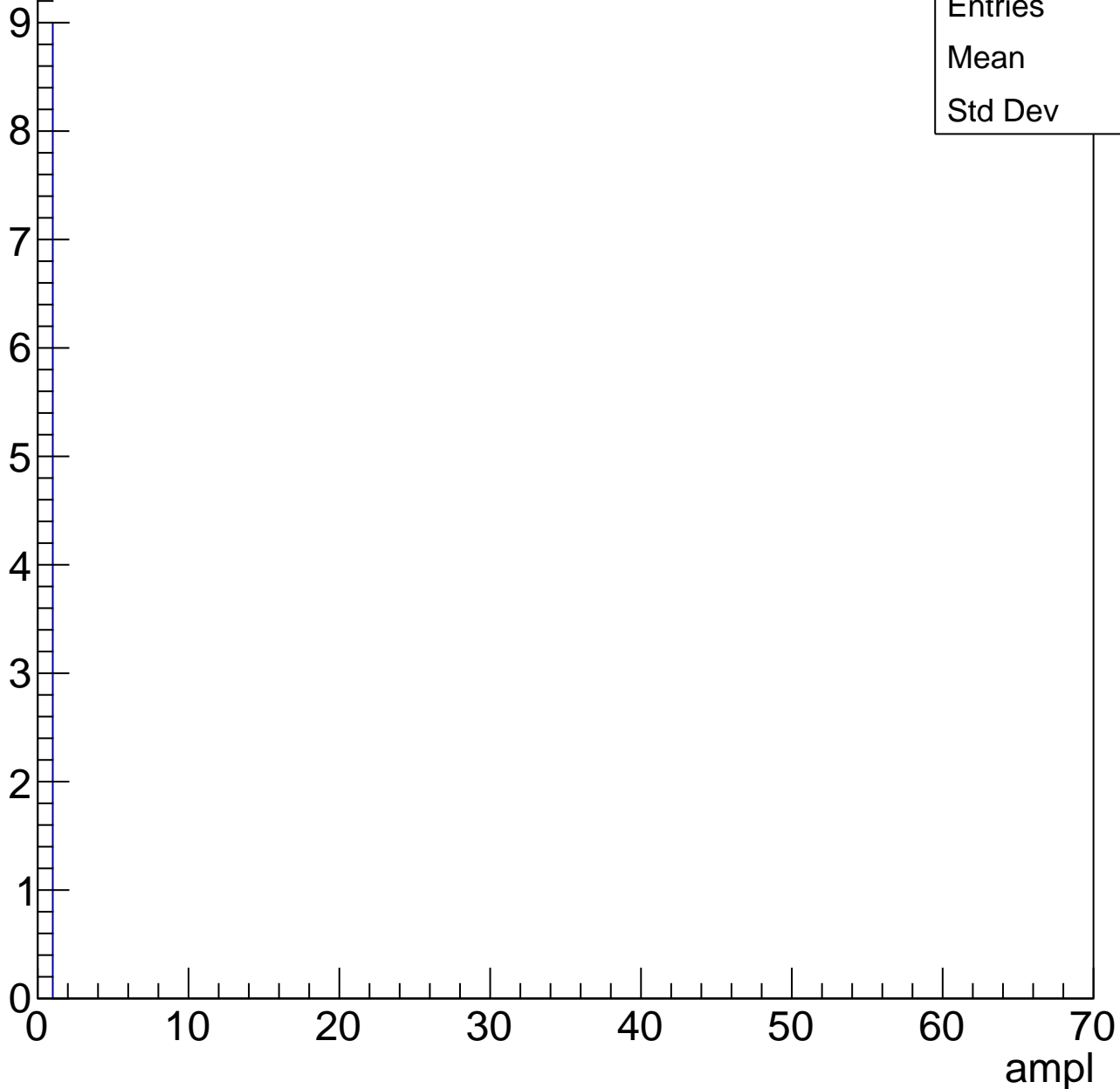
Entry



B1L103S, U14-ch12, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

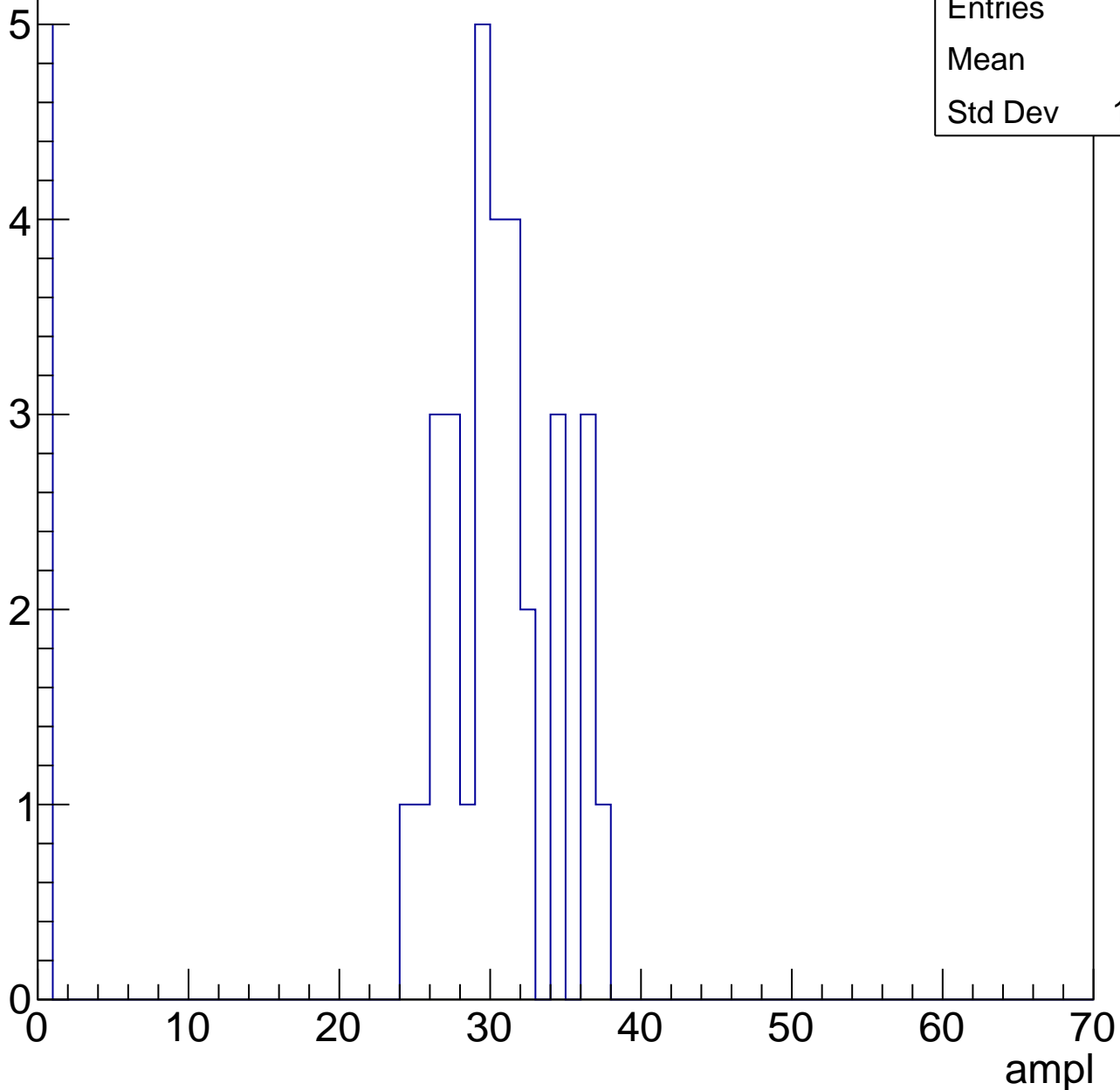


B1L103S, U14-ch13, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	36
Mean	26
Std Dev	10.91

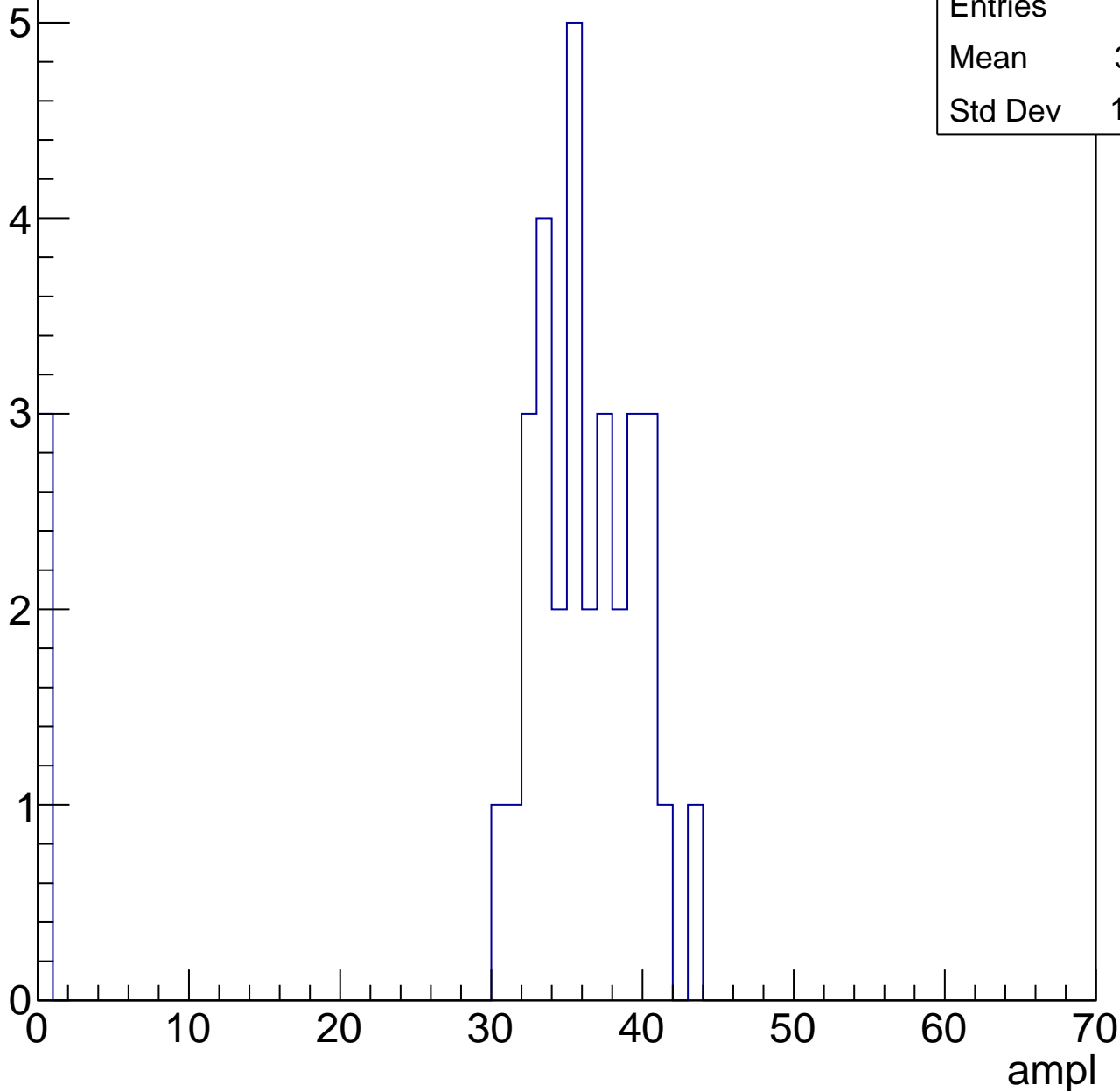


B1L103S, U14-ch13, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	34
Mean	32.71
Std Dev	10.62

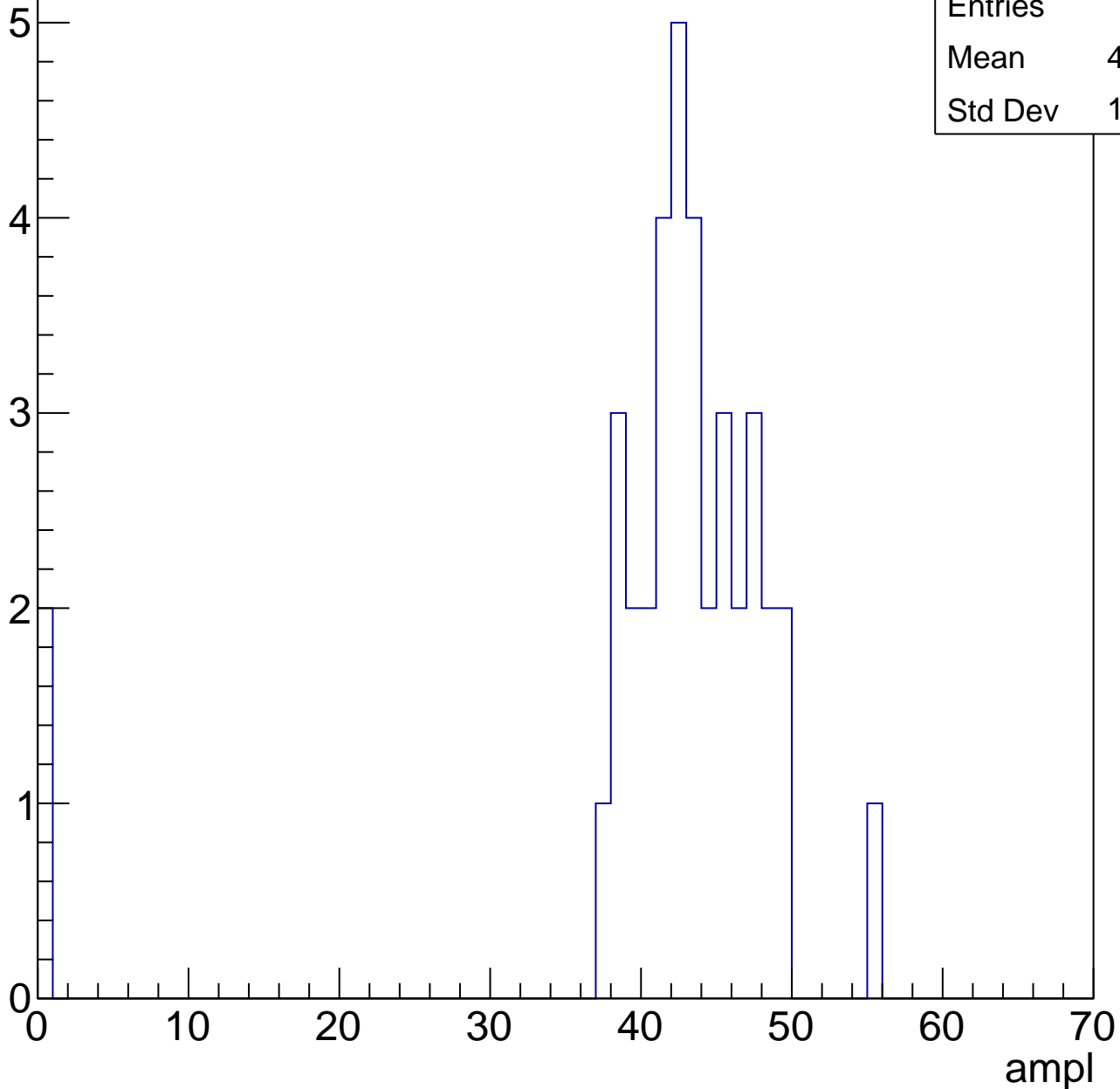


B1L103S, U14-ch13, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

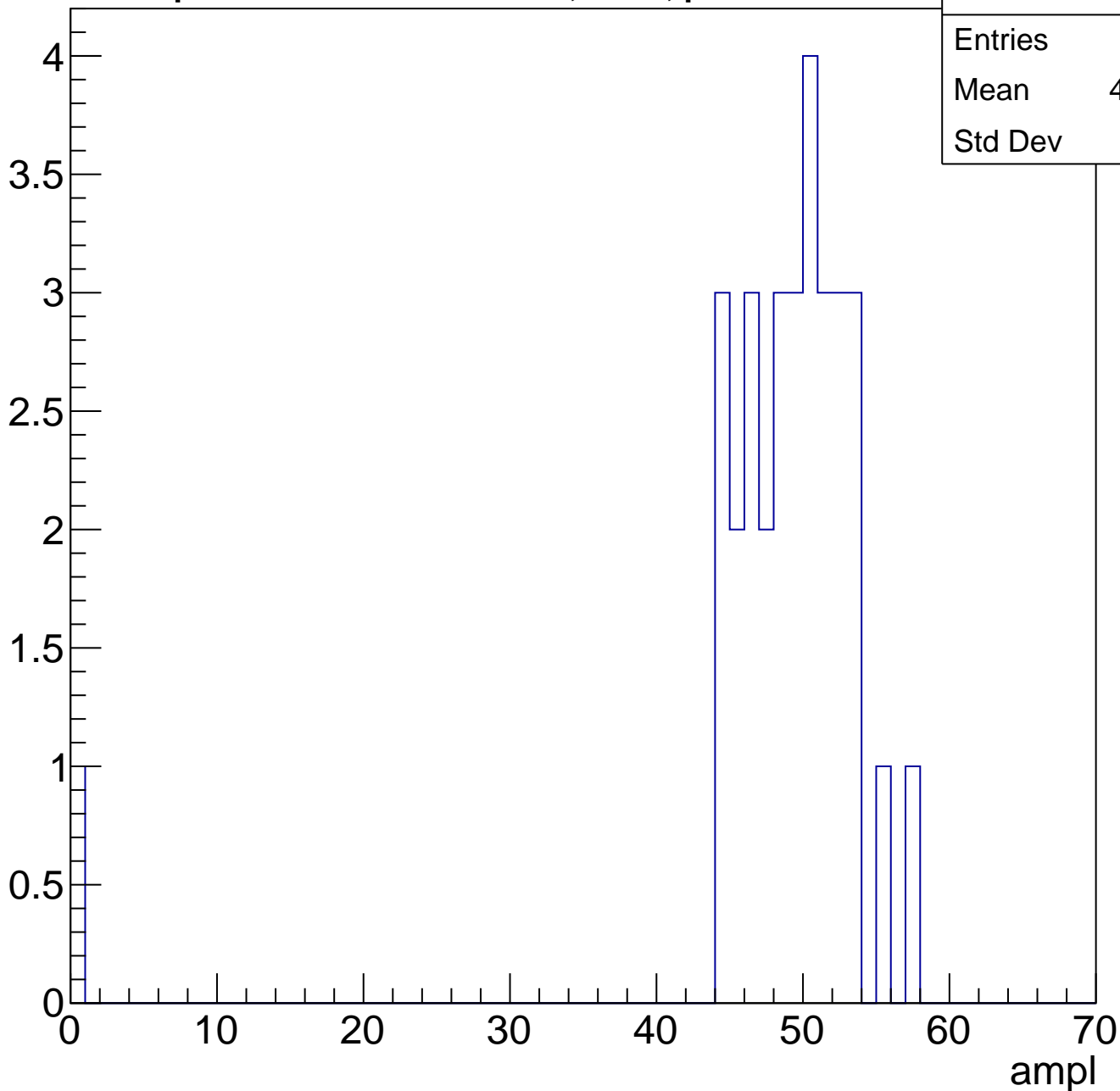
Entries	38
Mean	41.05
Std Dev	10.36



B1L103S, U14-ch13, adc3

calib_packv5_041523_1651.root, FC#0, port C2

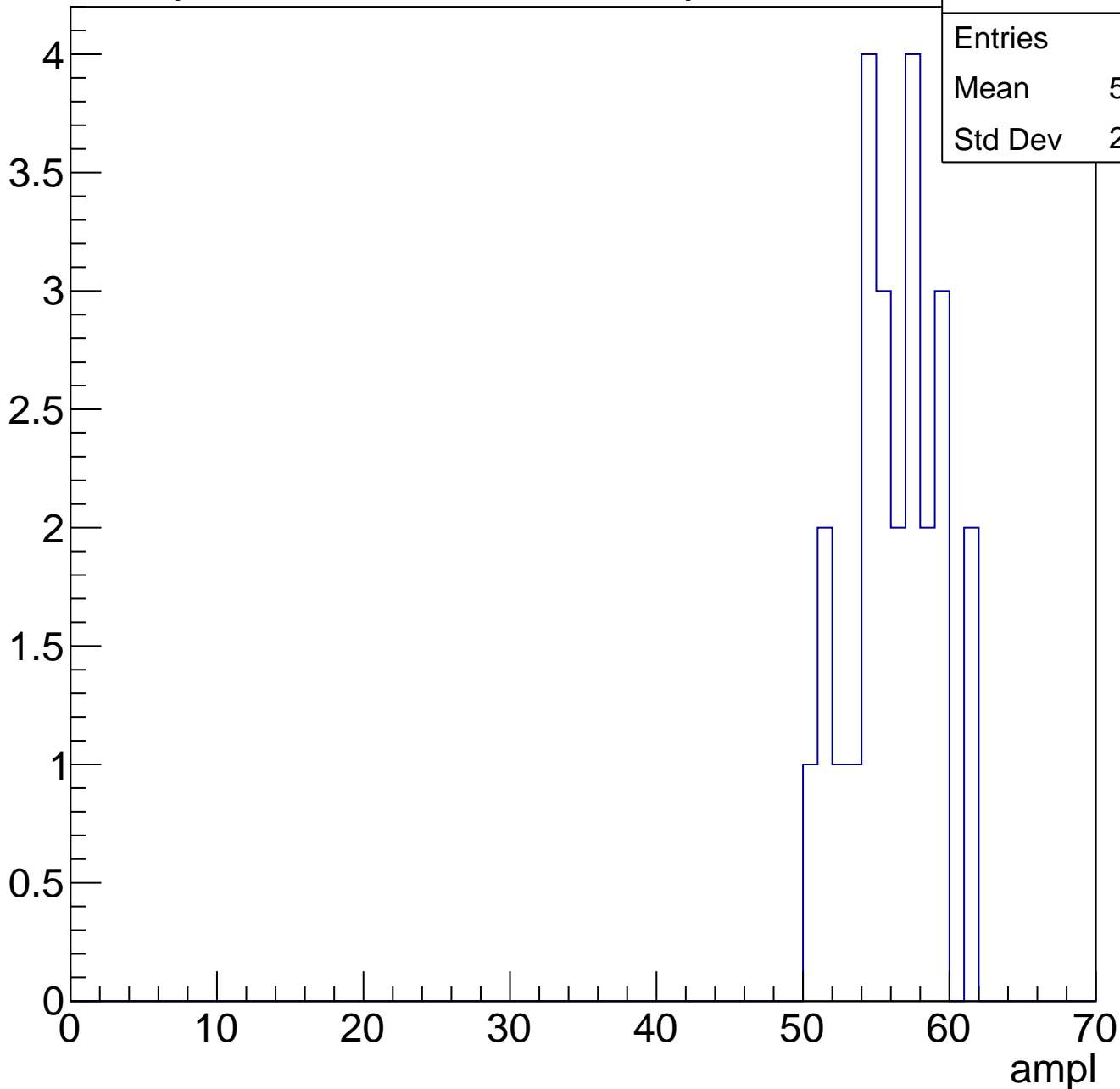
Entry



B1L103S, U14-ch13, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

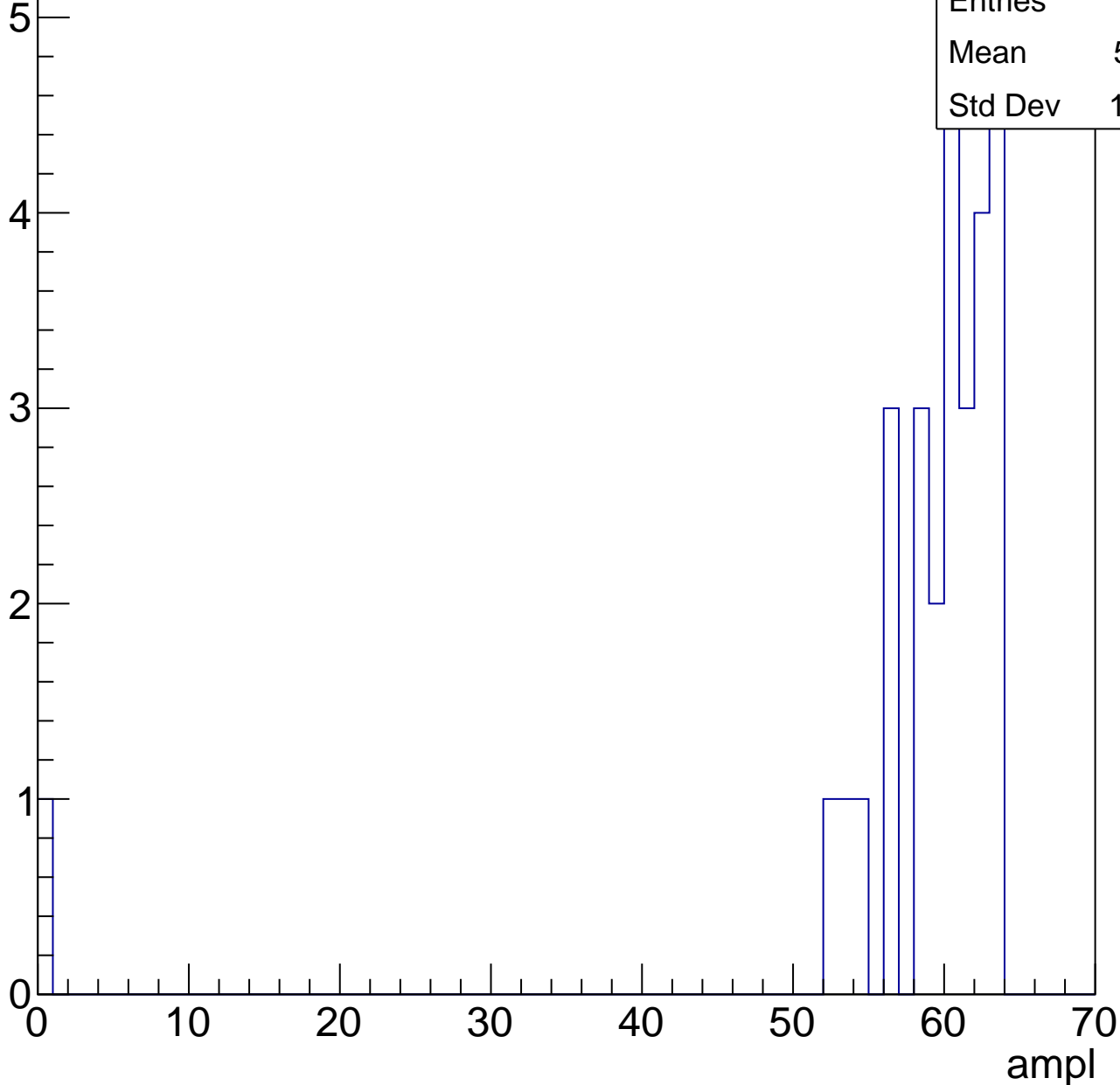


B1L103S, U14-ch13, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	29
Mean	57.41
Std Dev	11.27



B1L103S, U14-ch13, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch13, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

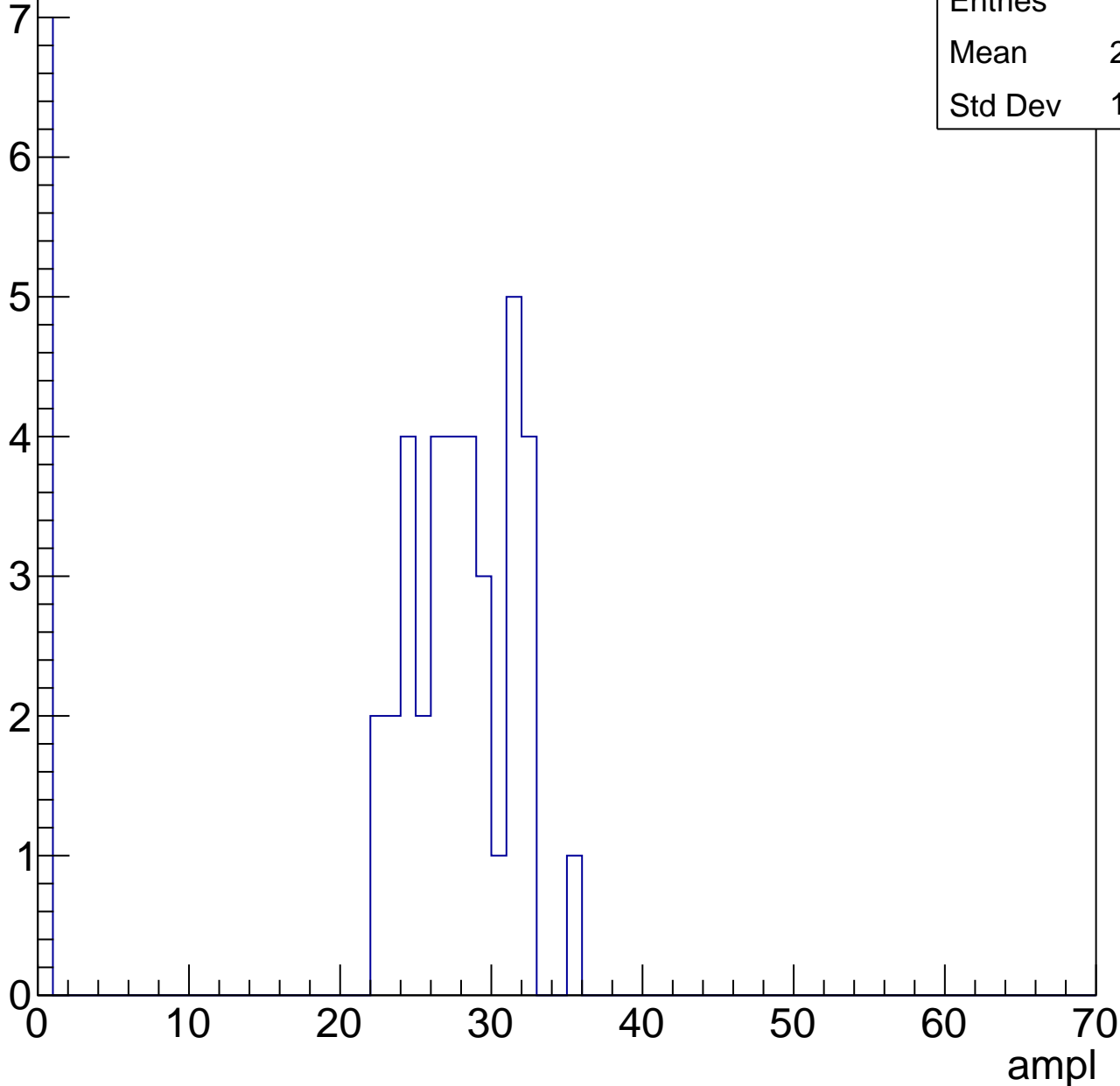


B1L103S, U14-ch14, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	43
Mean	23.14
Std Dev	10.63

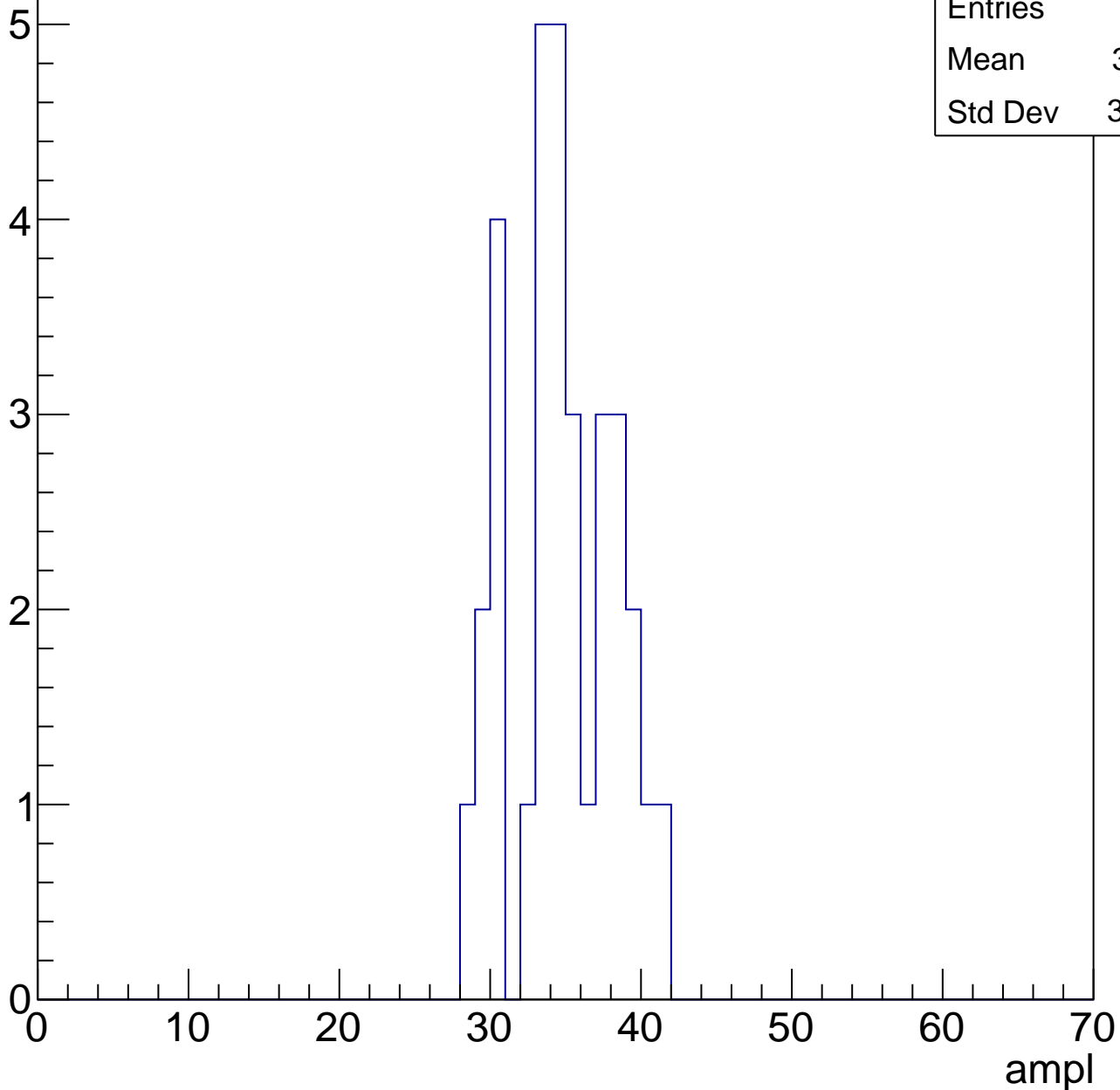


B1L103S, U14-ch14, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	32
Mean	34.31
Std Dev	3.414

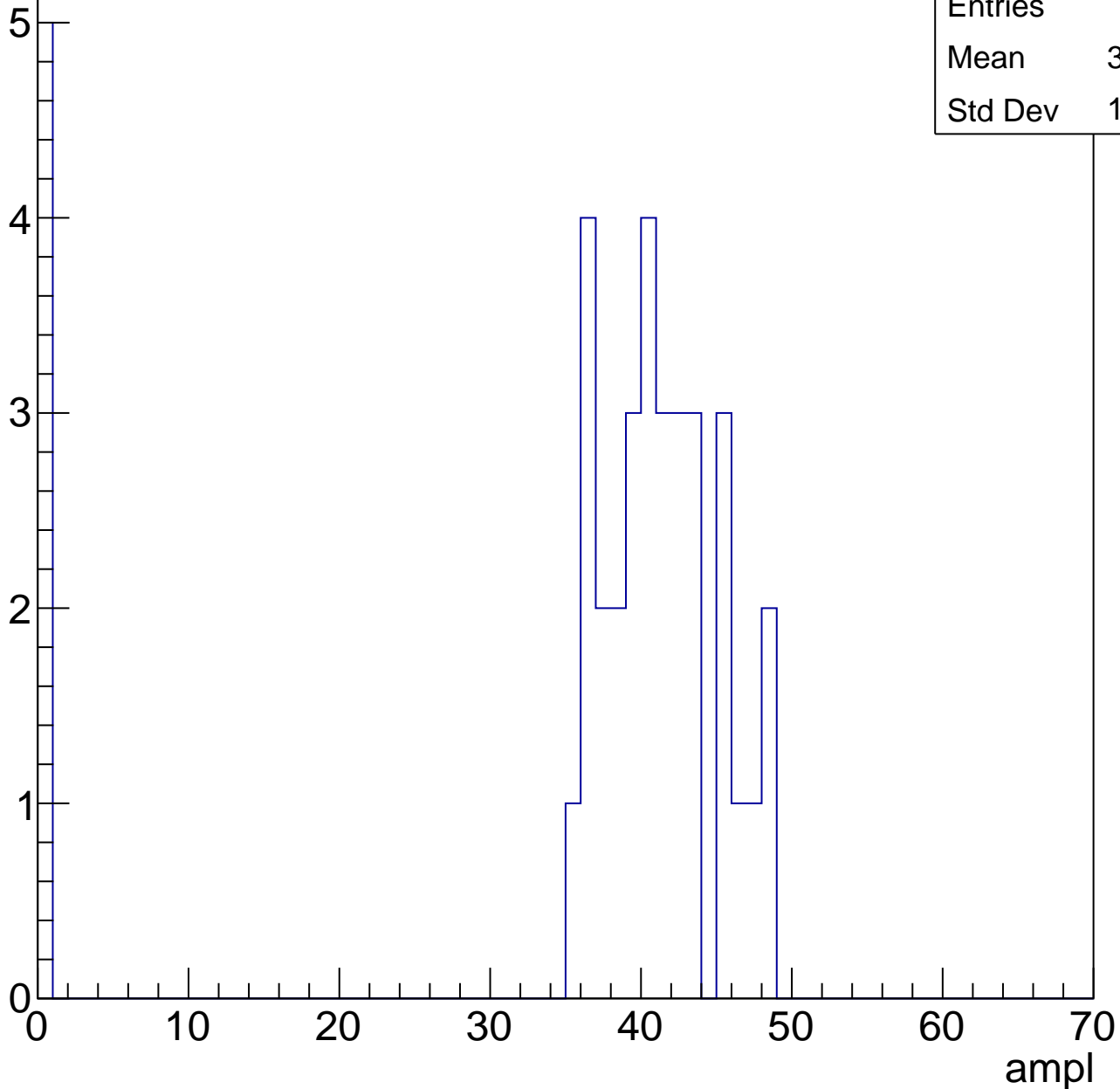


B1L103S, U14-ch14, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

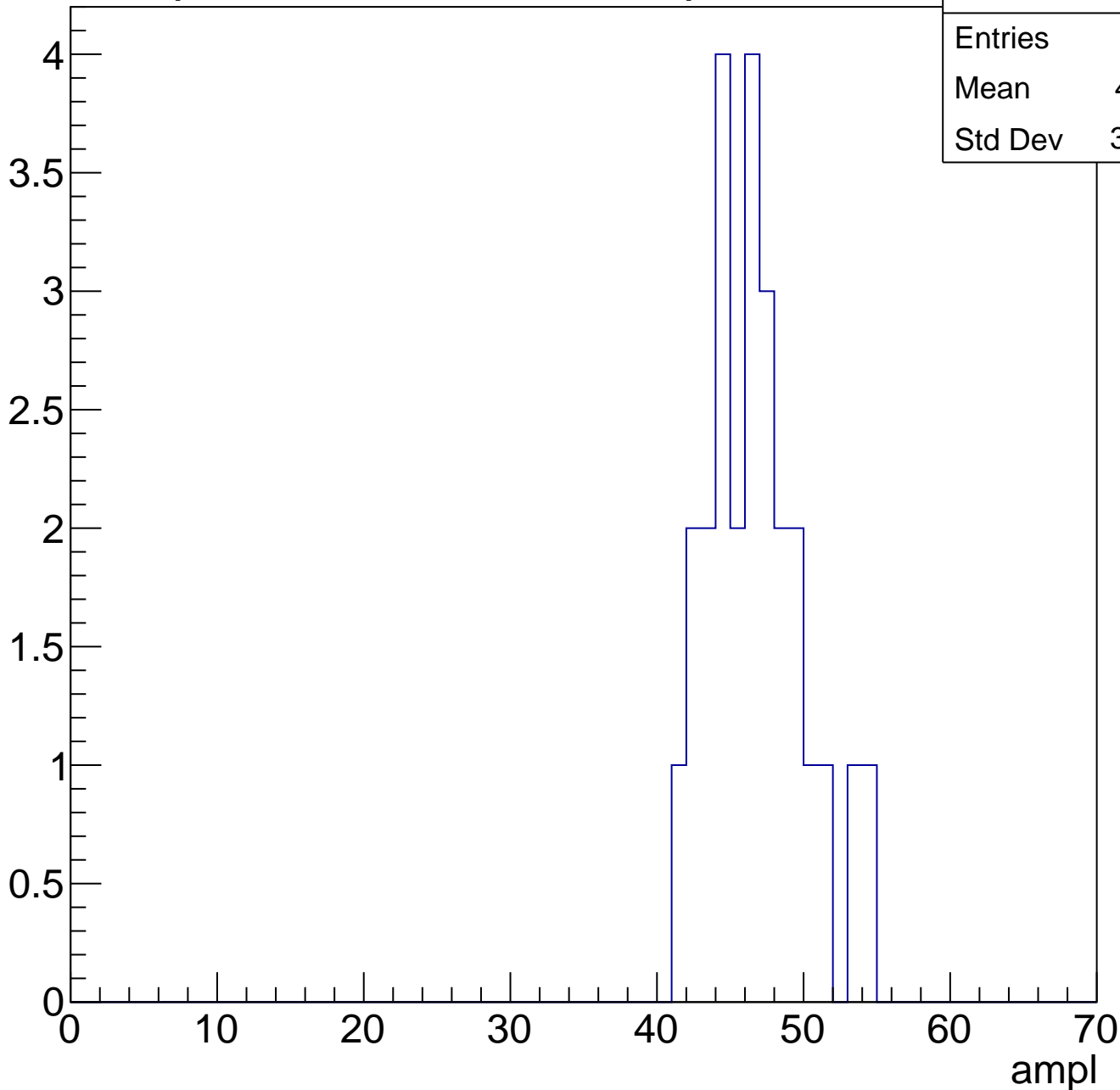
Entries	37
Mean	35.35
Std Dev	14.38



B1L103S, U14-ch14, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

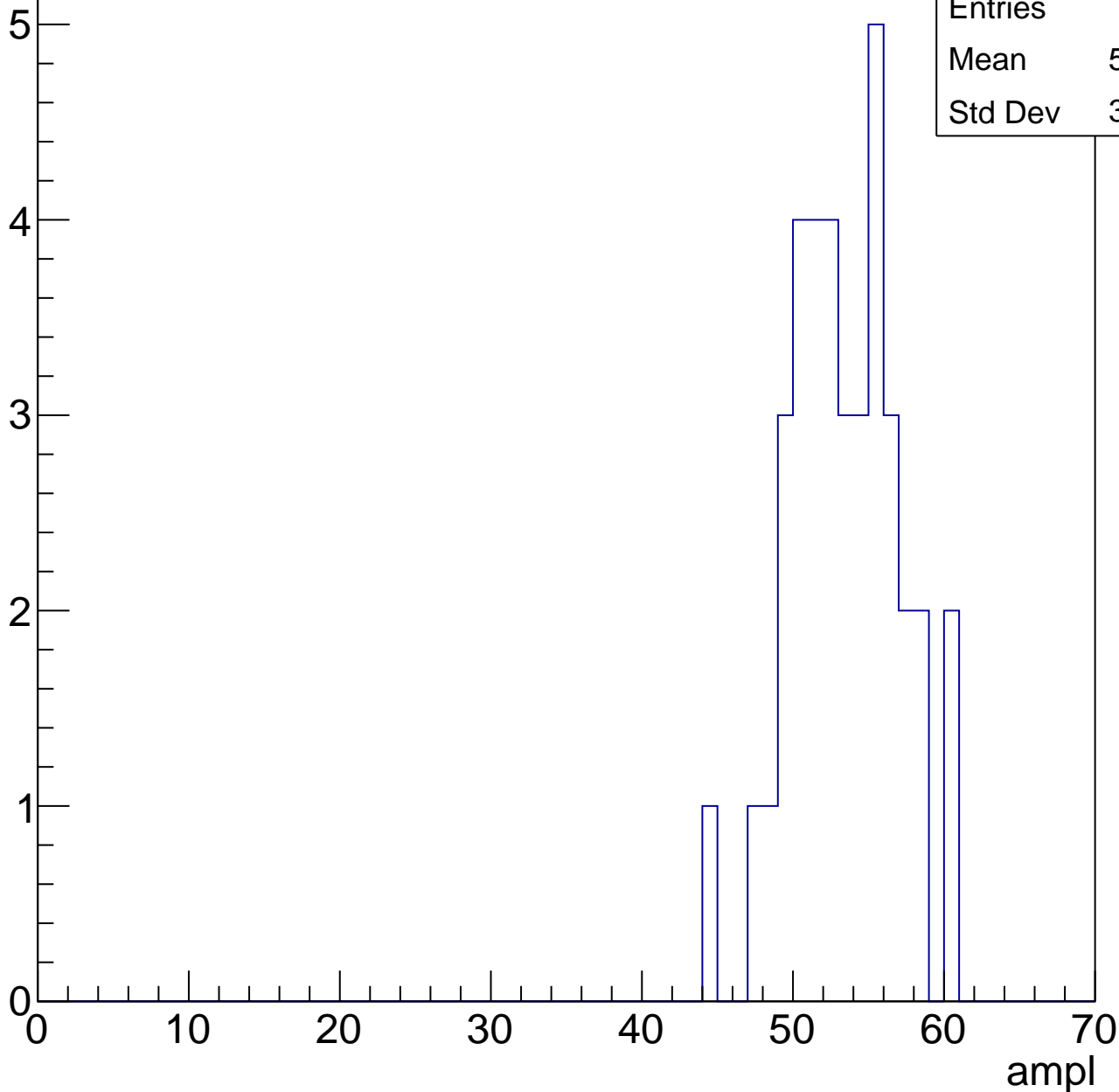


B1L103S, U14-ch14, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

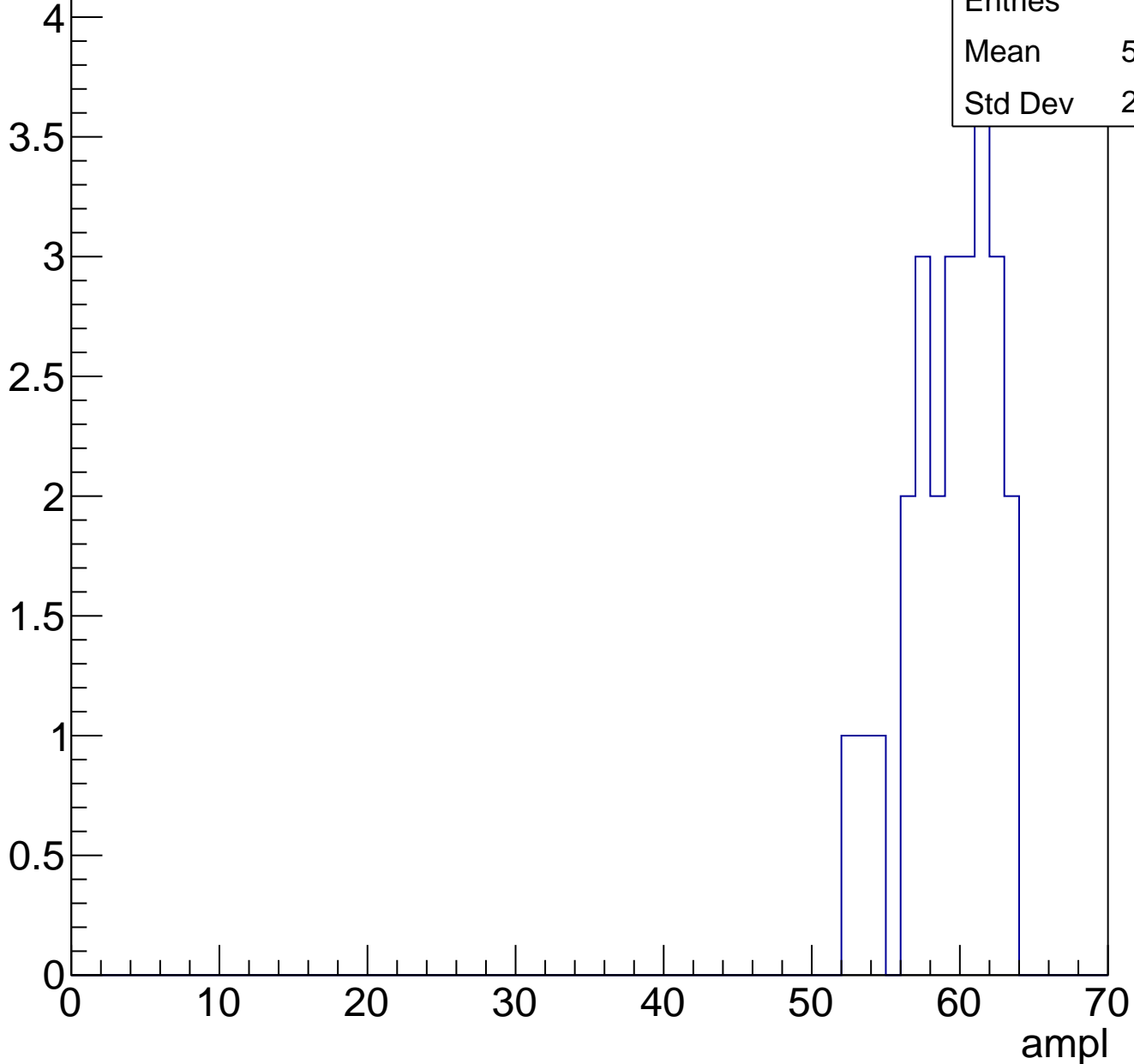
Entries	38
Mean	52.95
Std Dev	3.539



B1L103S, U14-ch14, adc5

calib_packv5_041523_1651.root, FC#0, port C2

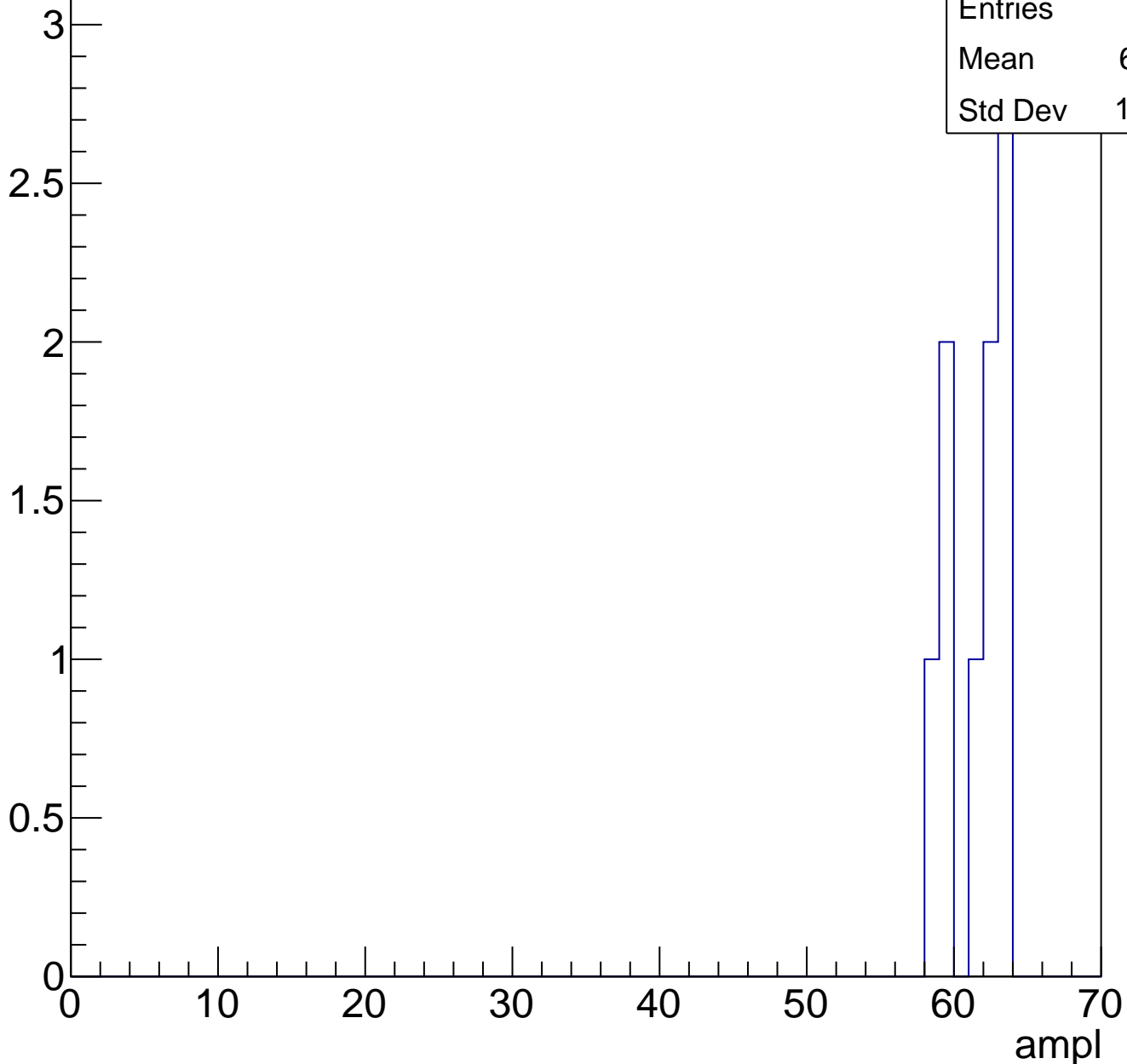
Entry



B1L103S, U14-ch14, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch14, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

12
10
8
6
4
2
0

Entries	12
Mean	0
Std Dev	0

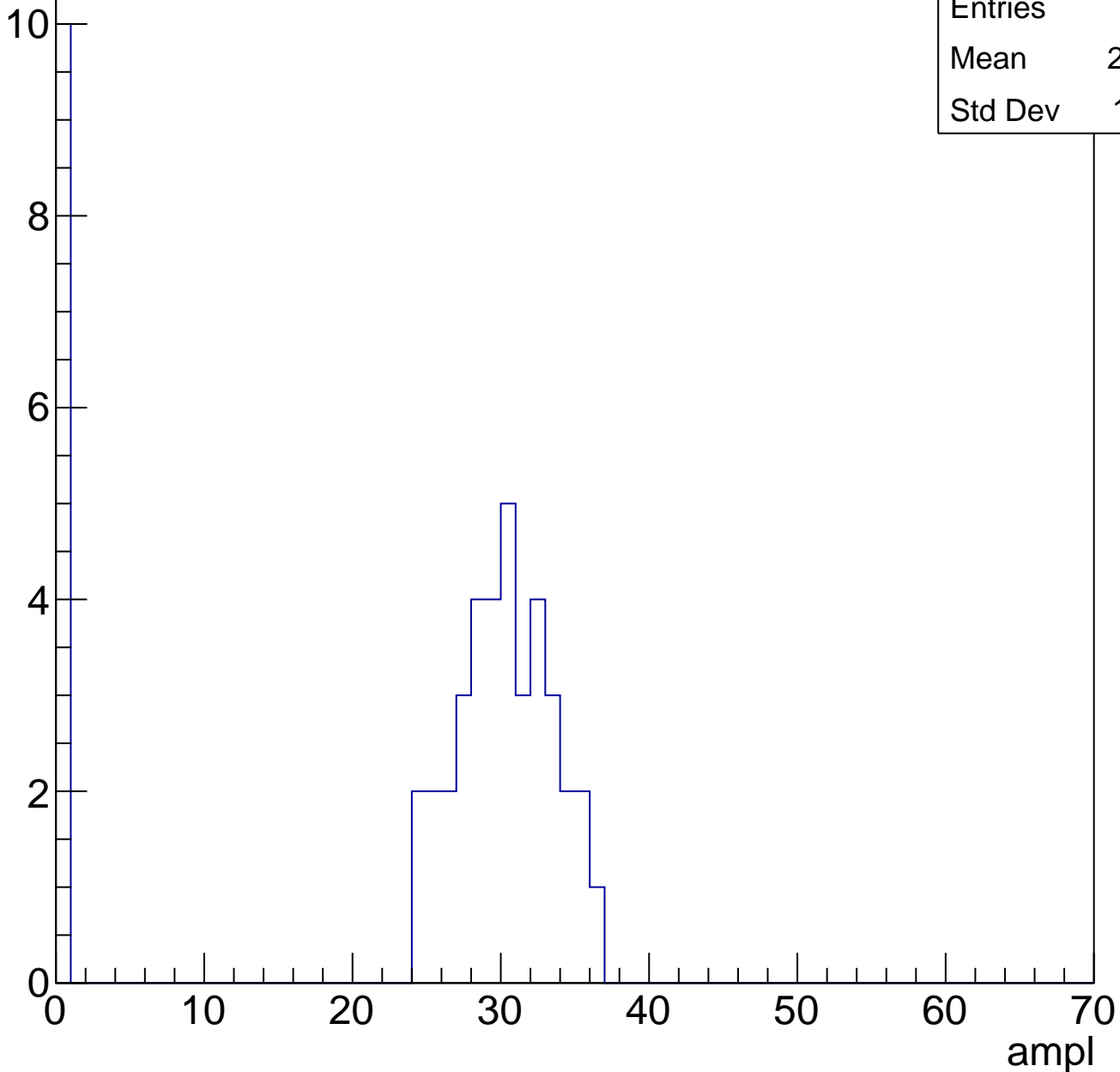
ampl

B1L103S, U14-ch15, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	47
Mean	23.47
Std Dev	12.51

Entry

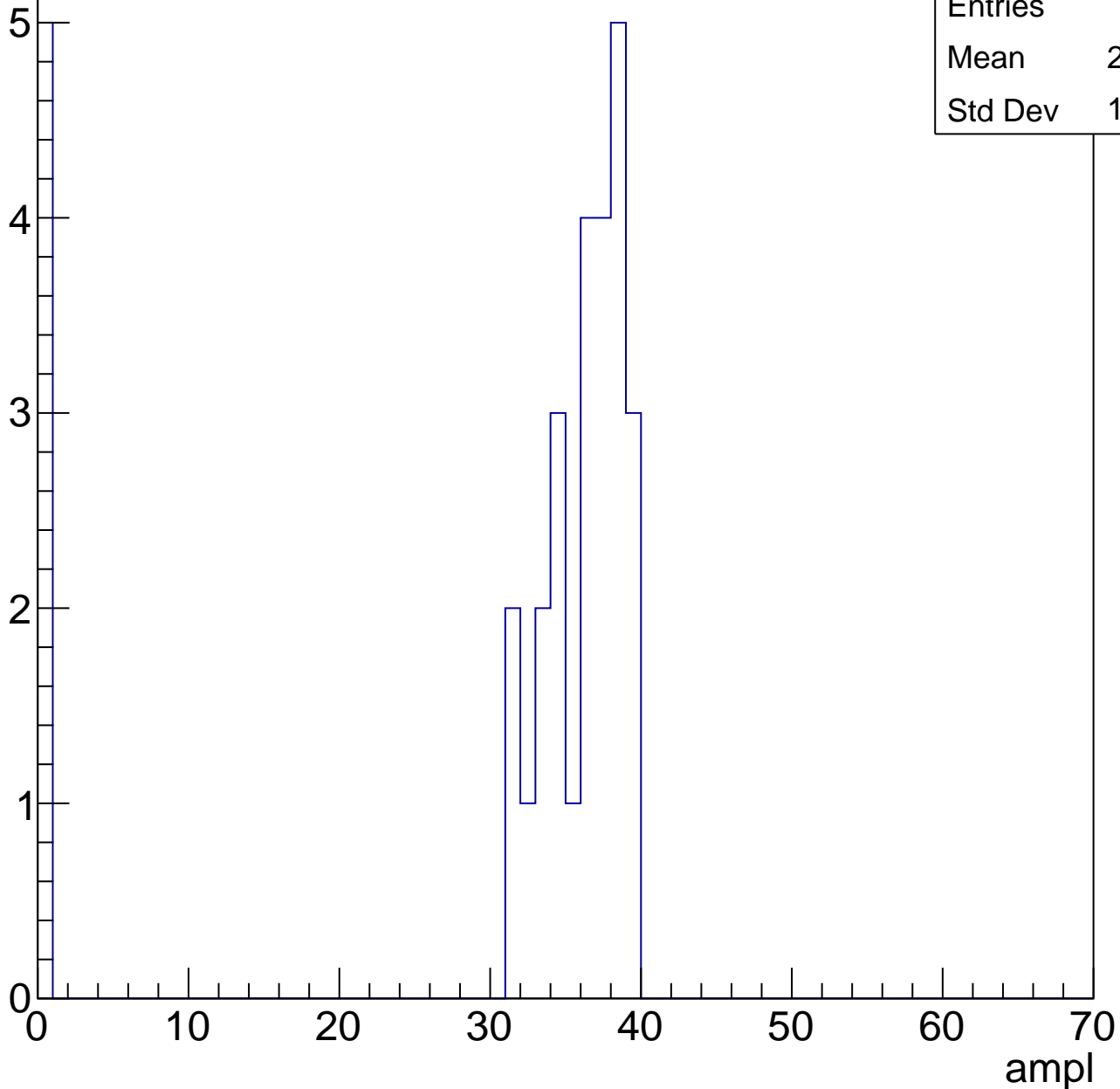


B1L103S, U14-ch15, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	30
Mean	29.87
Std Dev	13.54

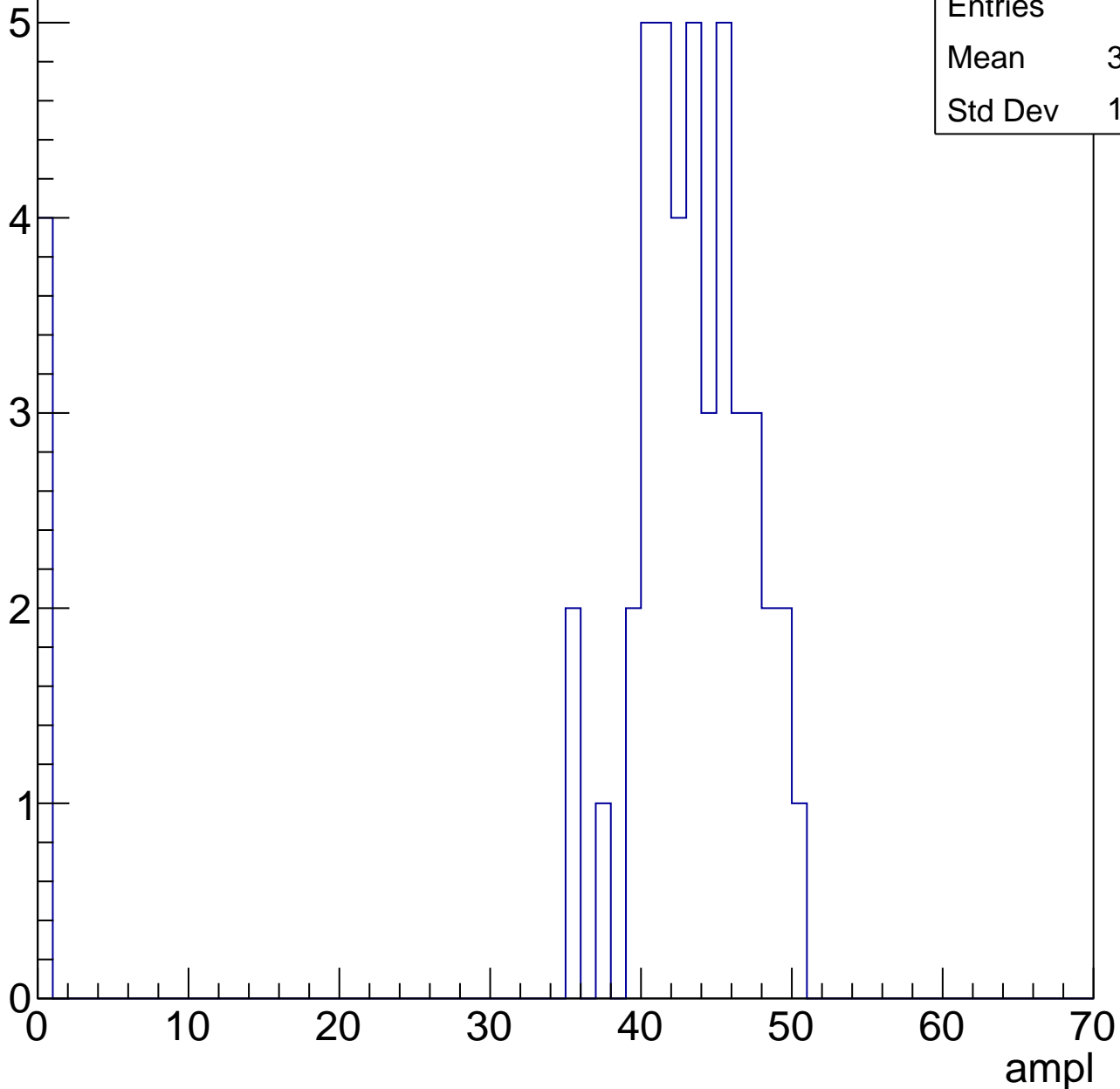


B1L103S, U14-ch15, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

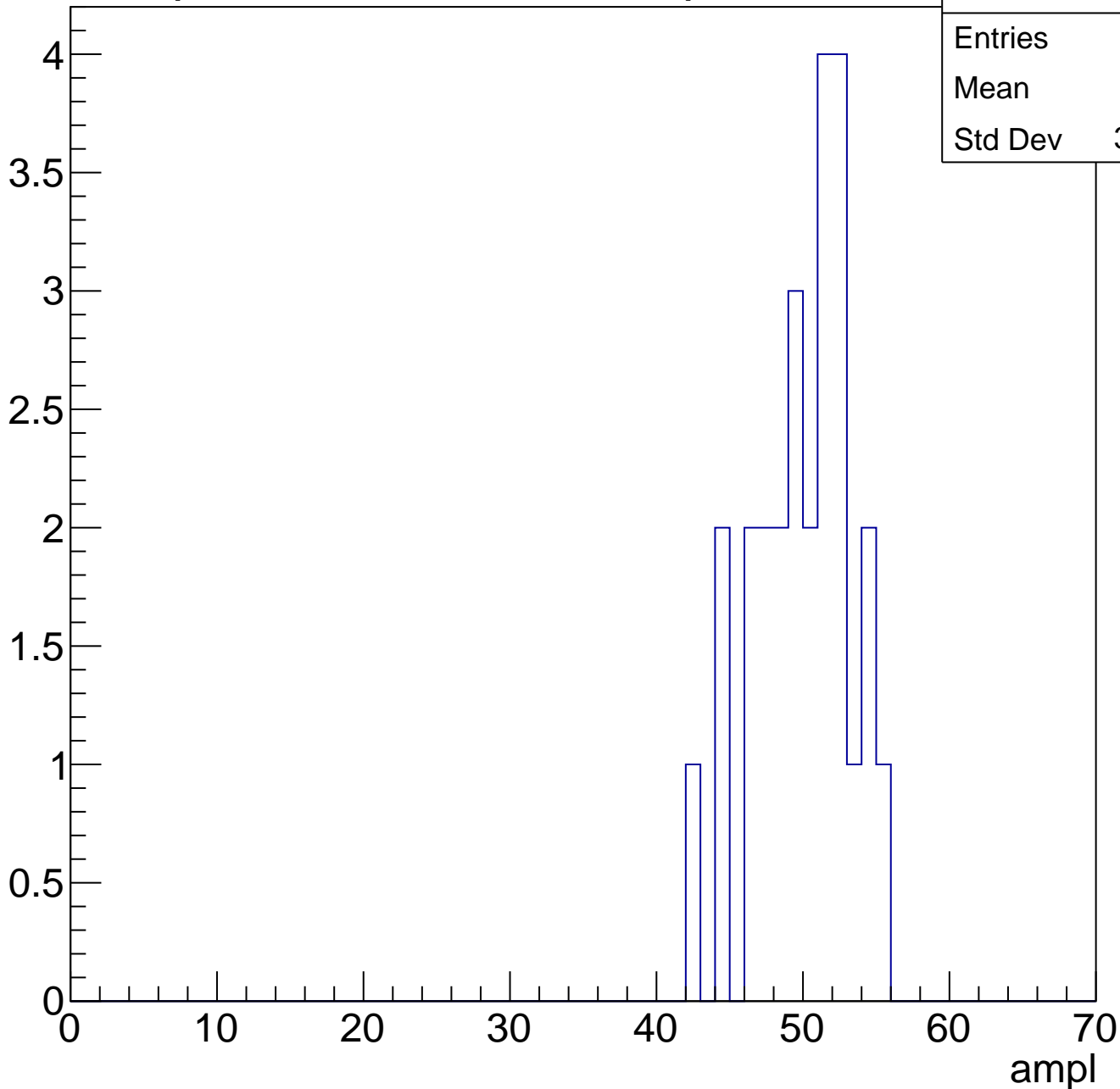
Entries	47
Mean	39.43
Std Dev	12.49



B1L103S, U14-ch15, adc3

calib_packv5_041523_1651.root, FC#0, port C2

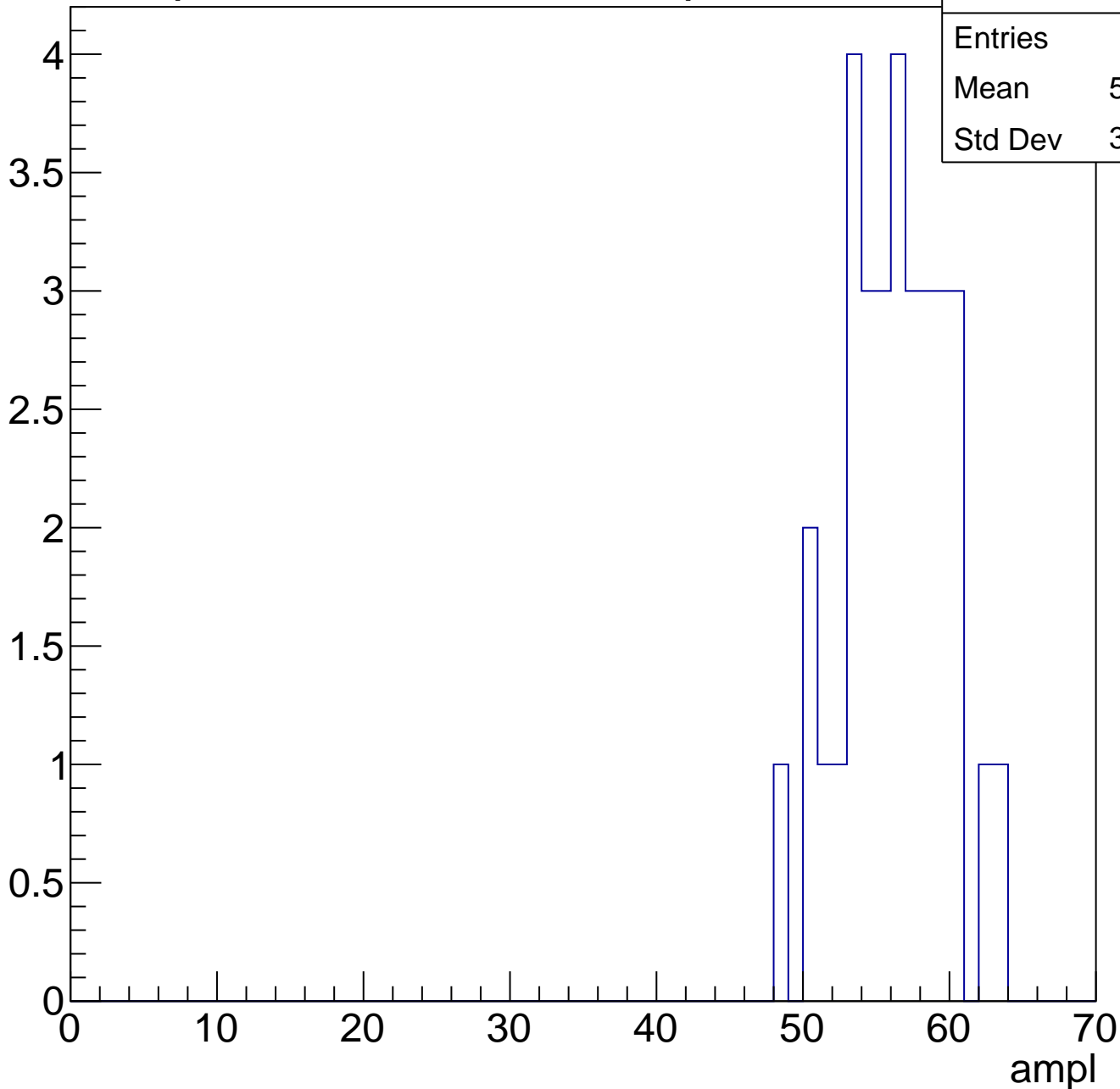
Entry



B1L103S, U14-ch15, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



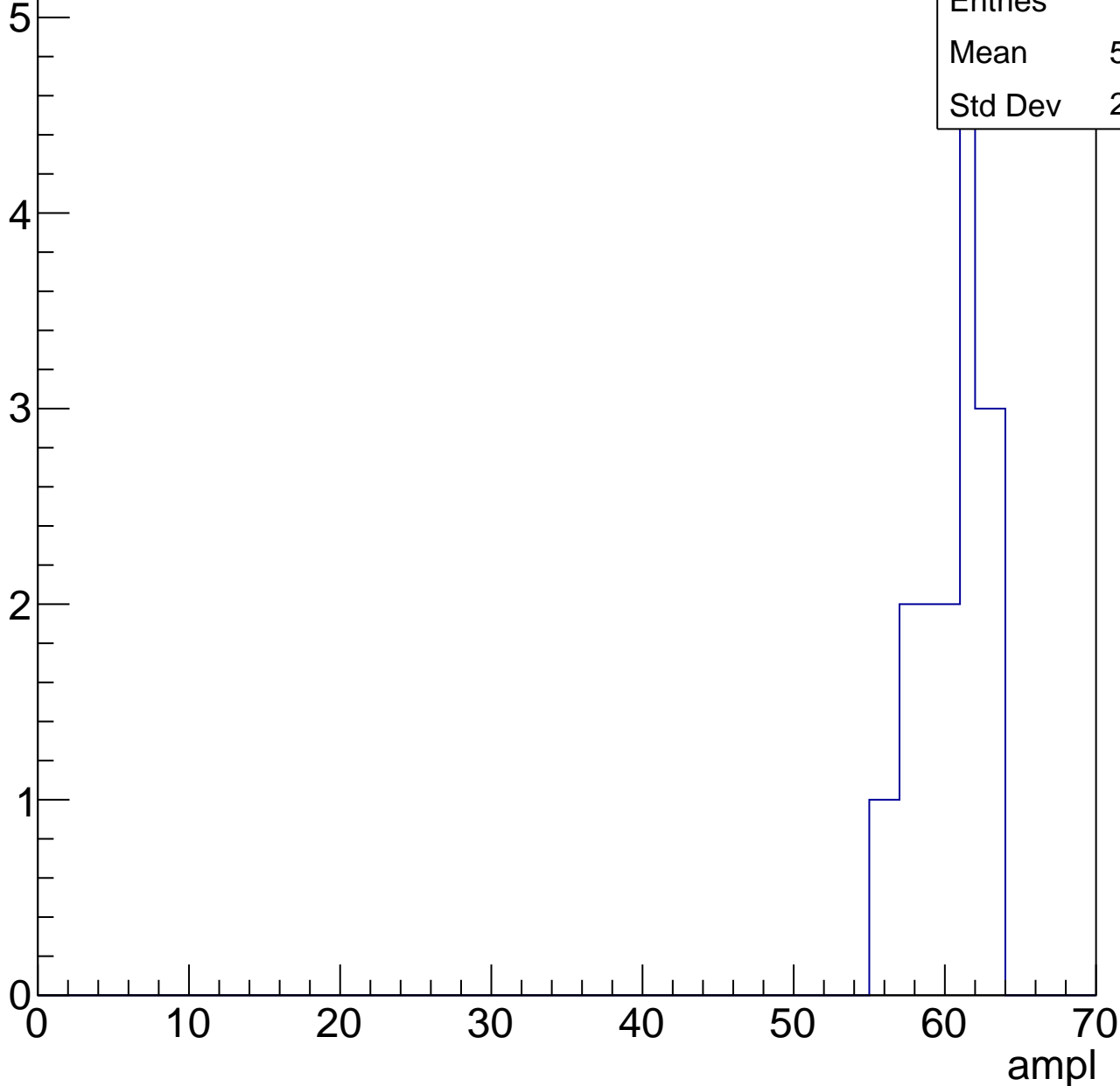
Entries	33
Mean	55.79
Std Dev	3.488

B1L103S, U14-ch15, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	21
Mean	59.95
Std Dev	2.319



B1L103S, U14-ch15, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch15, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

Entries	10
---------	----

Mean	0
------	---

Std Dev	0
---------	---

8

6

4

2

0

0

10

20

30

40

50

60

70

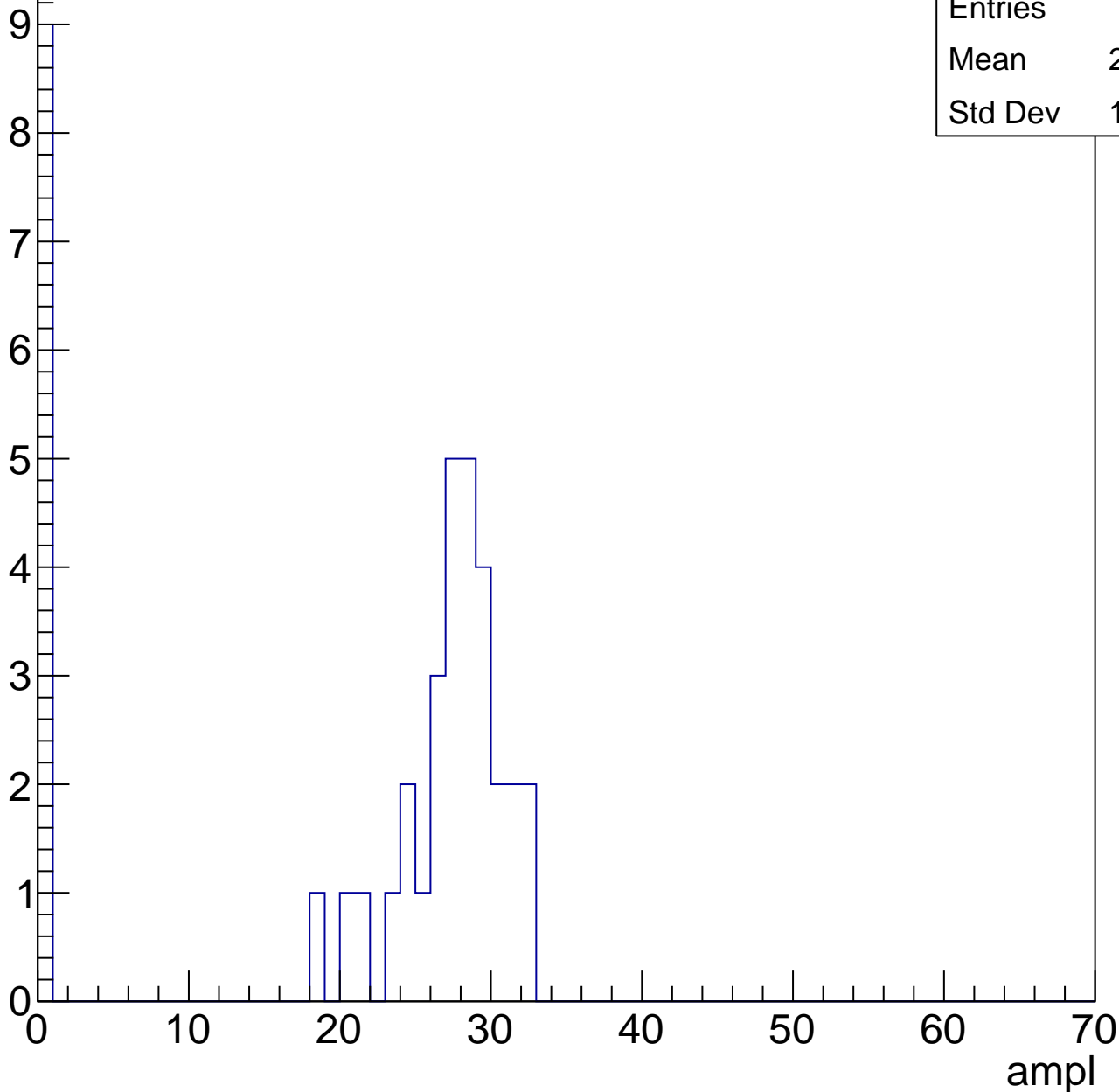
ampl

B1L103S, U14-ch16, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	20.77
Std Dev	11.74

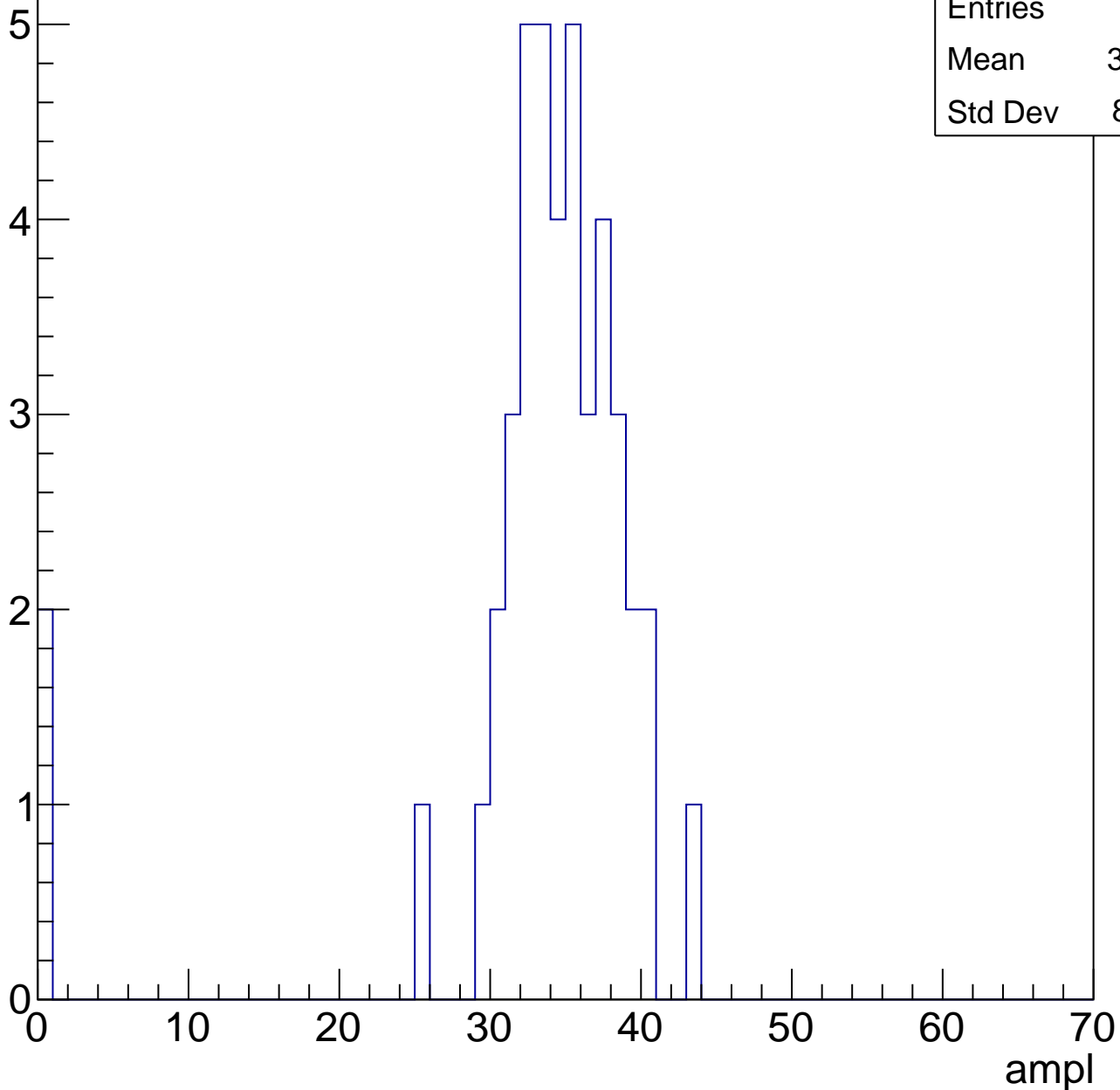


B1L103S, U14-ch16, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	43
Mean	32.88
Std Dev	8.001

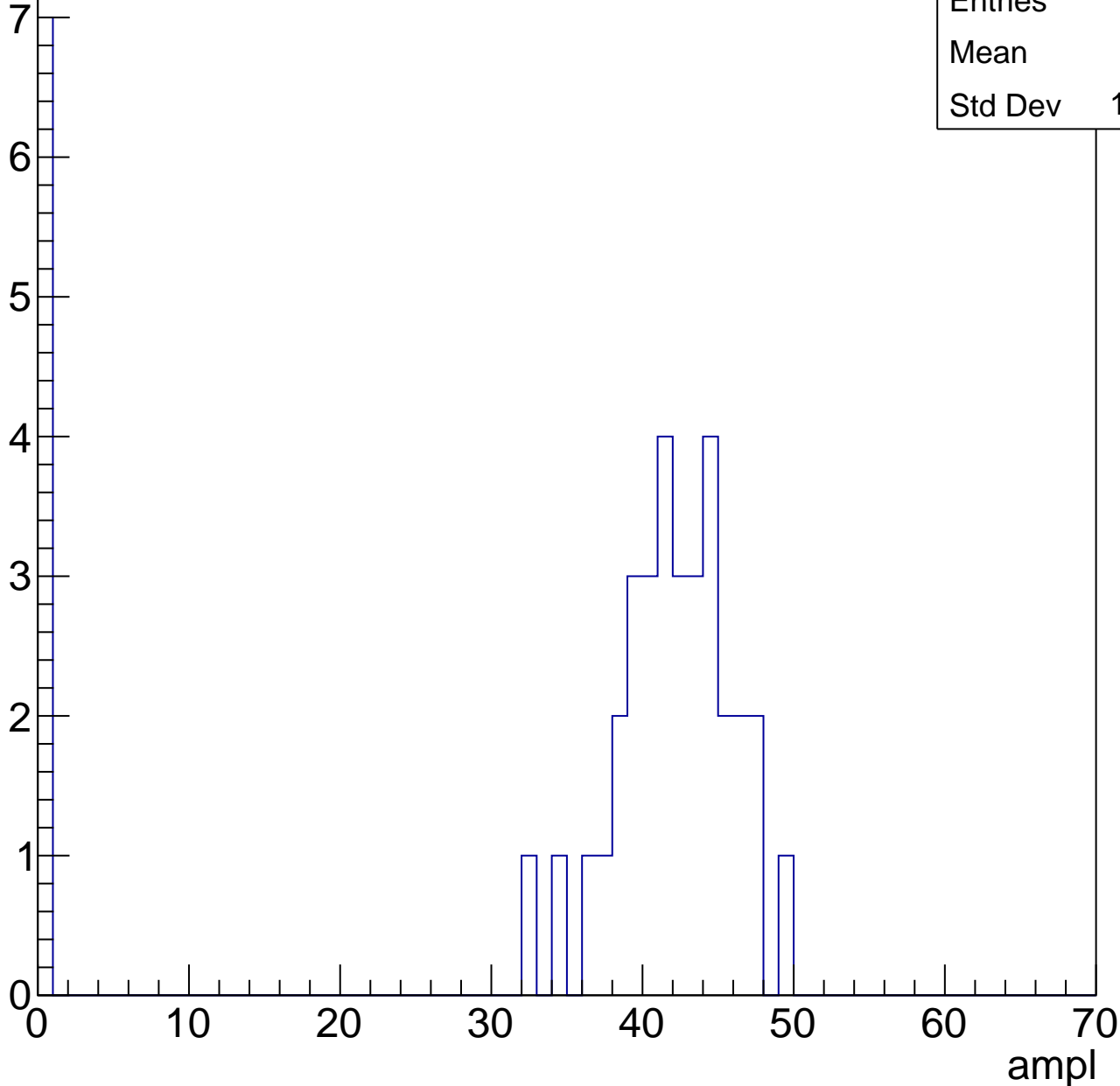


B1L103S, U14-ch16, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	34.3
Std Dev	16.16

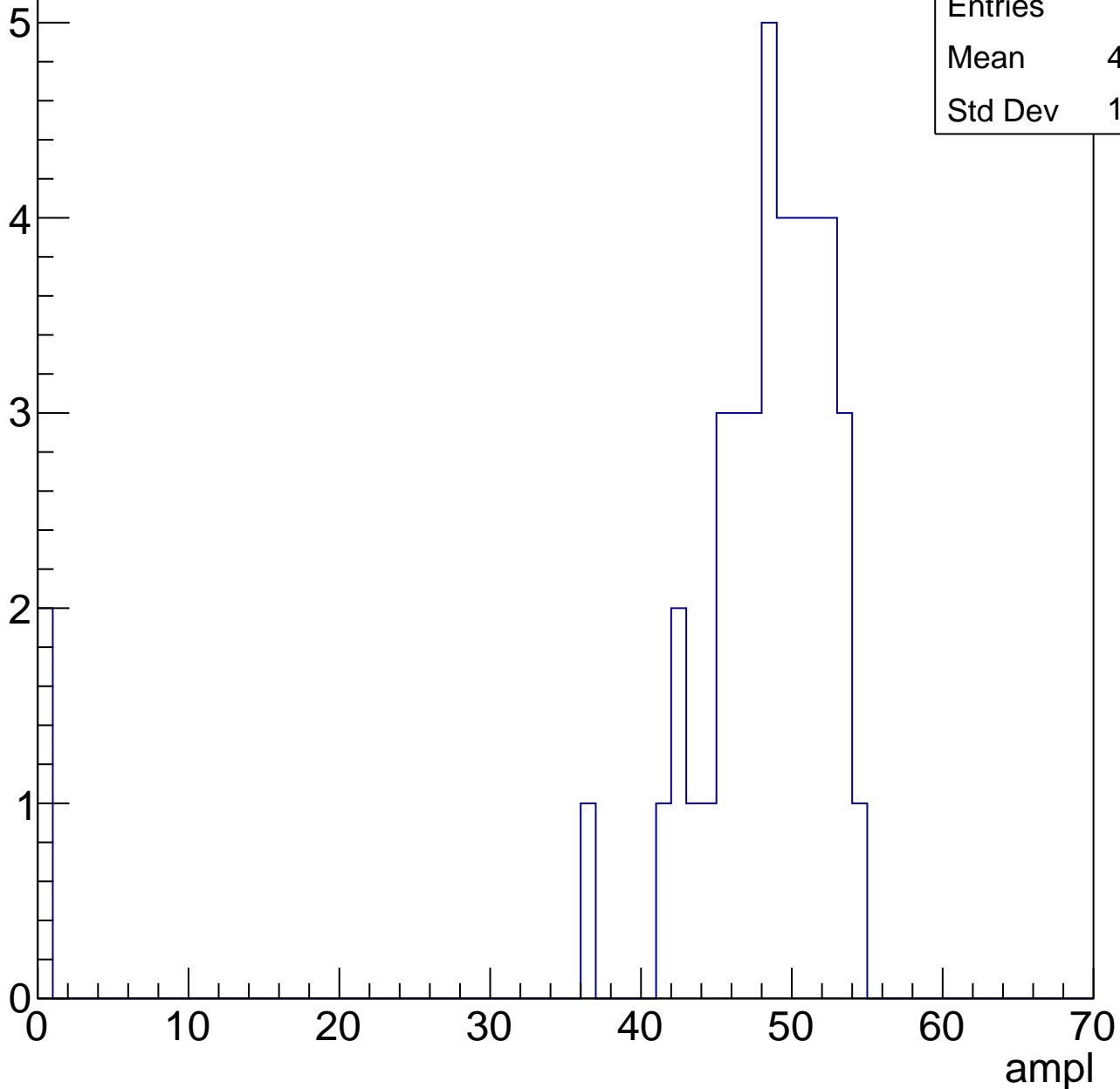


B1L103S, U14-ch16, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

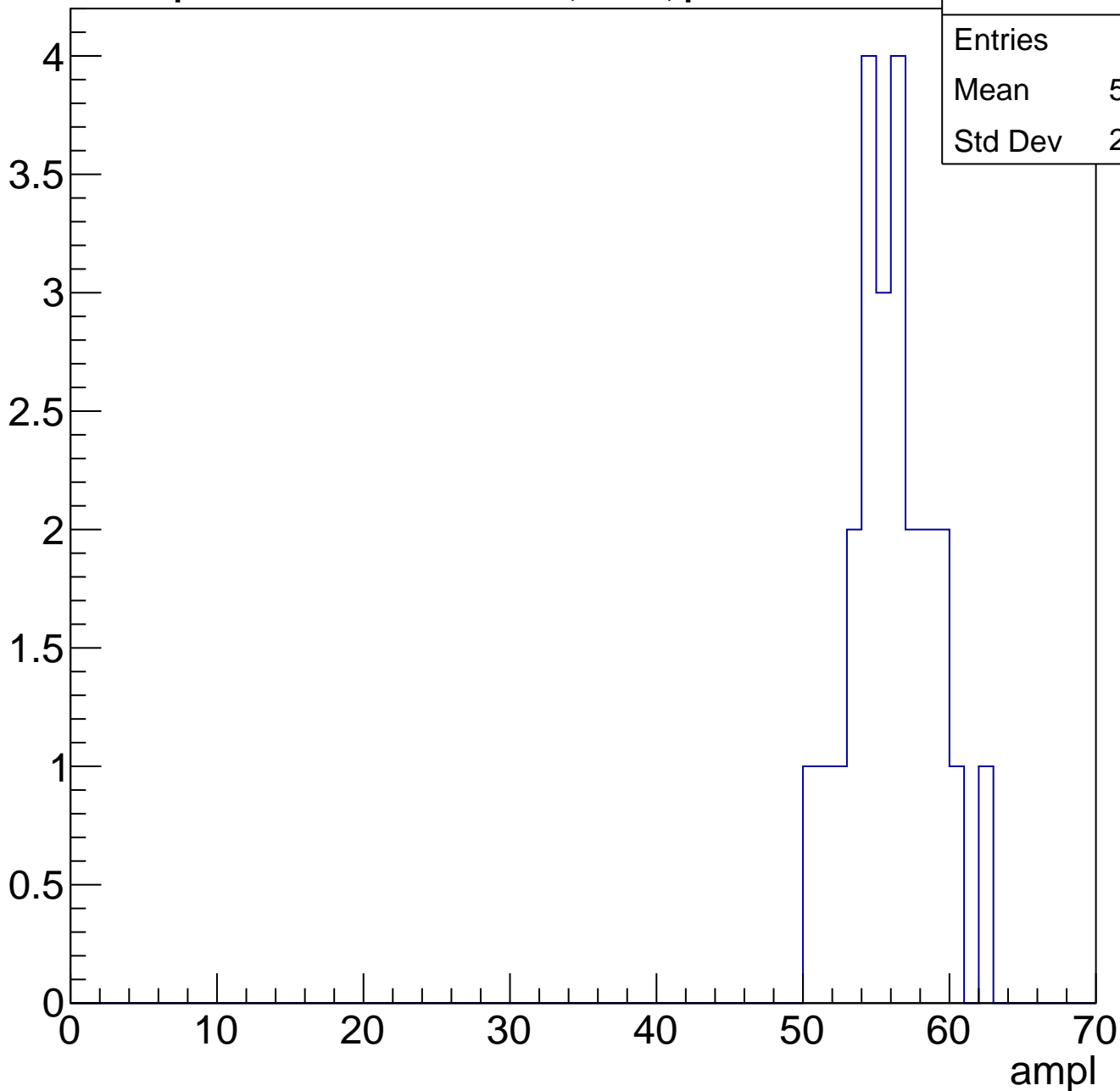
Entries	42
Mean	45.79
Std Dev	10.89



B1L103S, U14-ch16, adc4

calib_packv5_041523_1651.root, FC#0, port C2

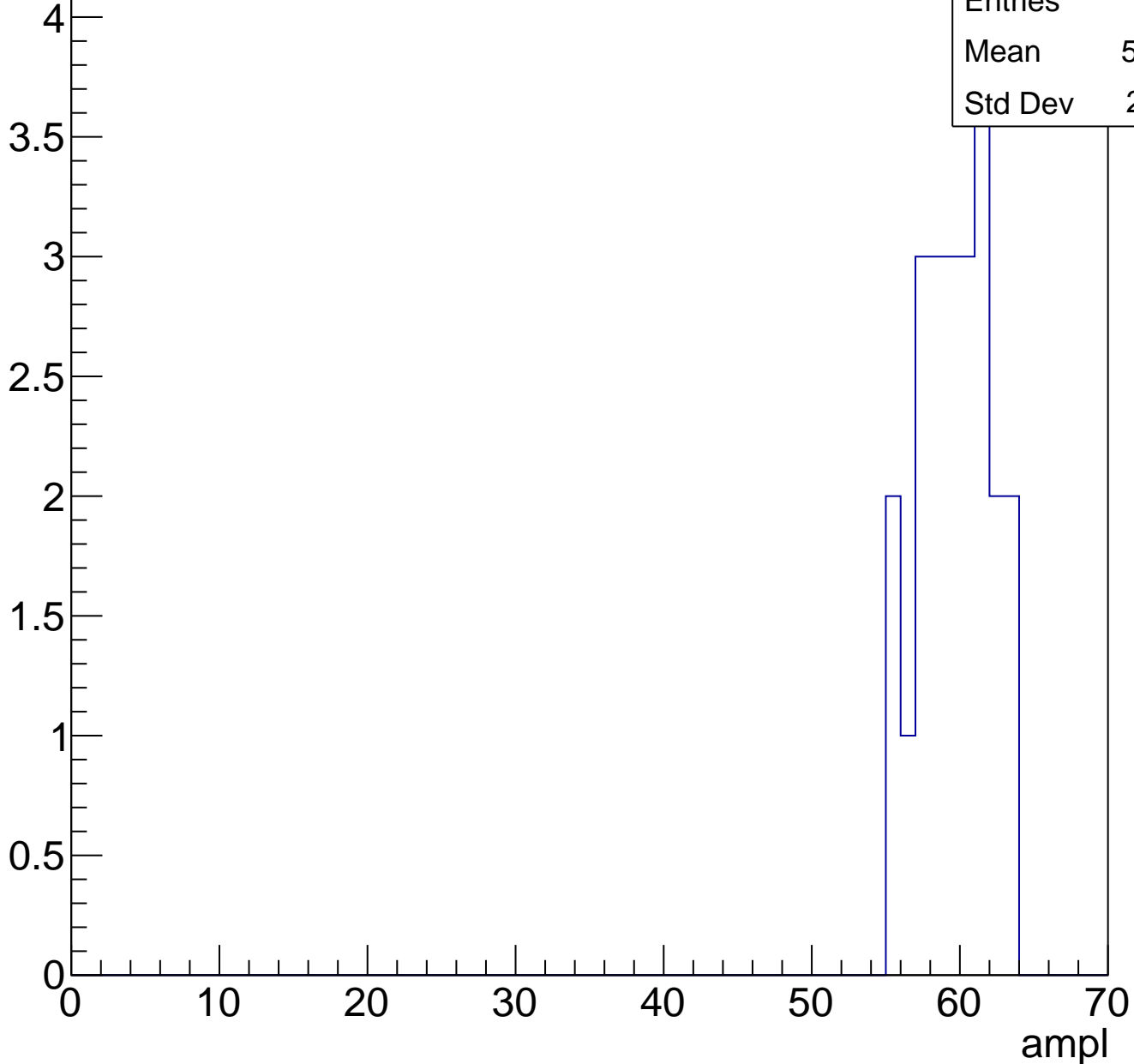
Entry



B1L103S, U14-ch16, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch16, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

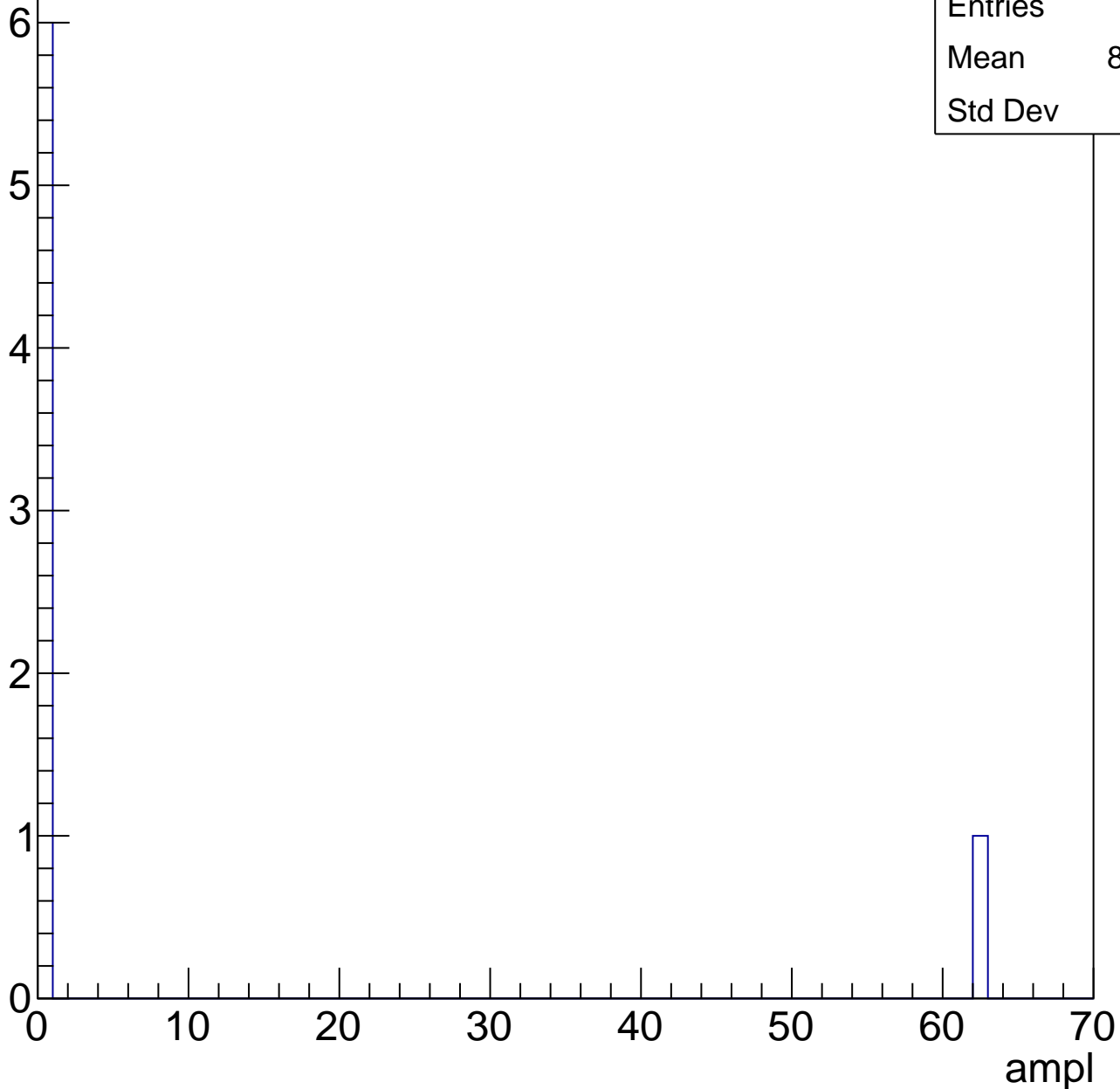


B1L103S, U14-ch16, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	7
Mean	8.857
Std Dev	21.7

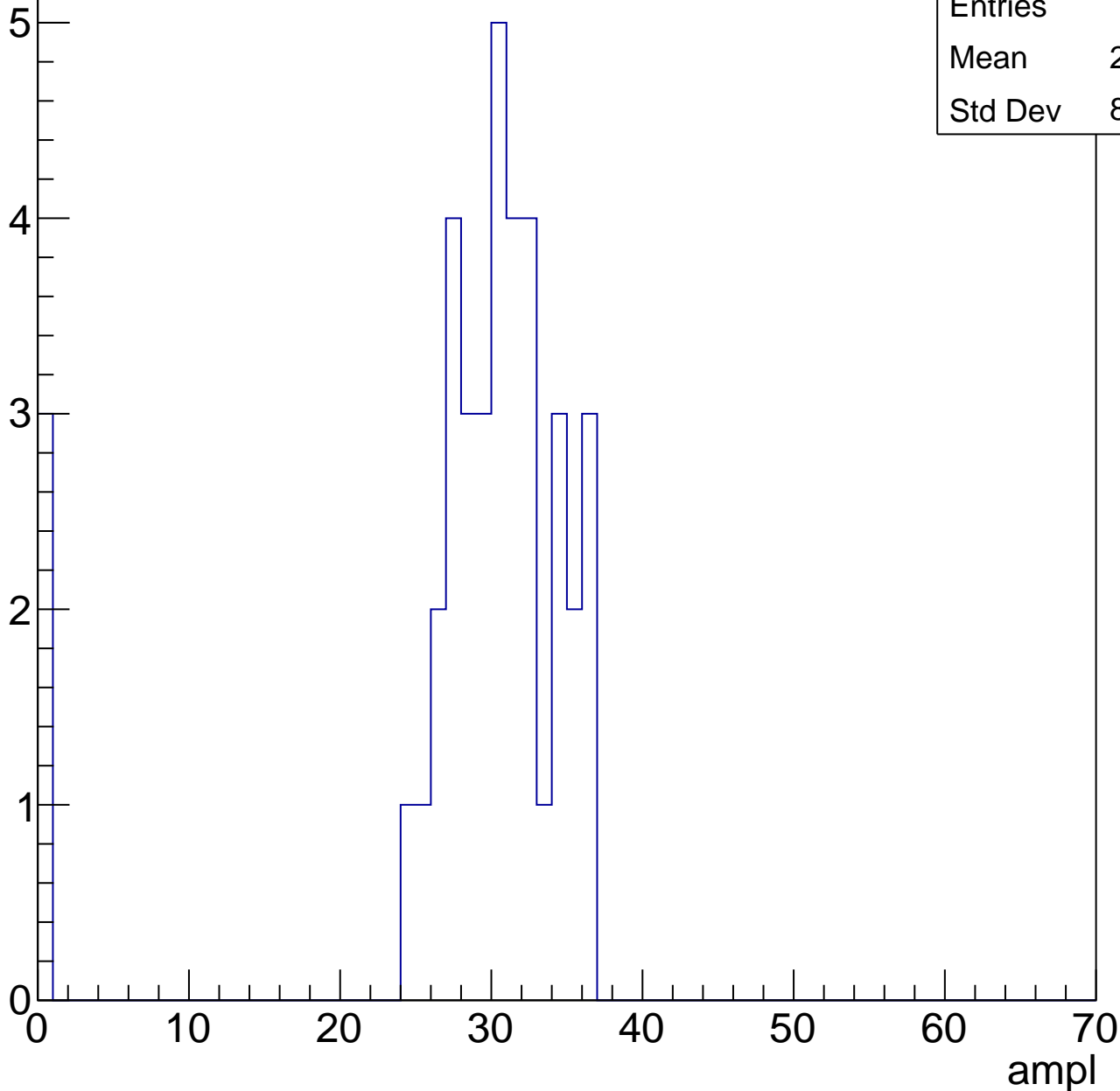


B1L103S, U14-ch17, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

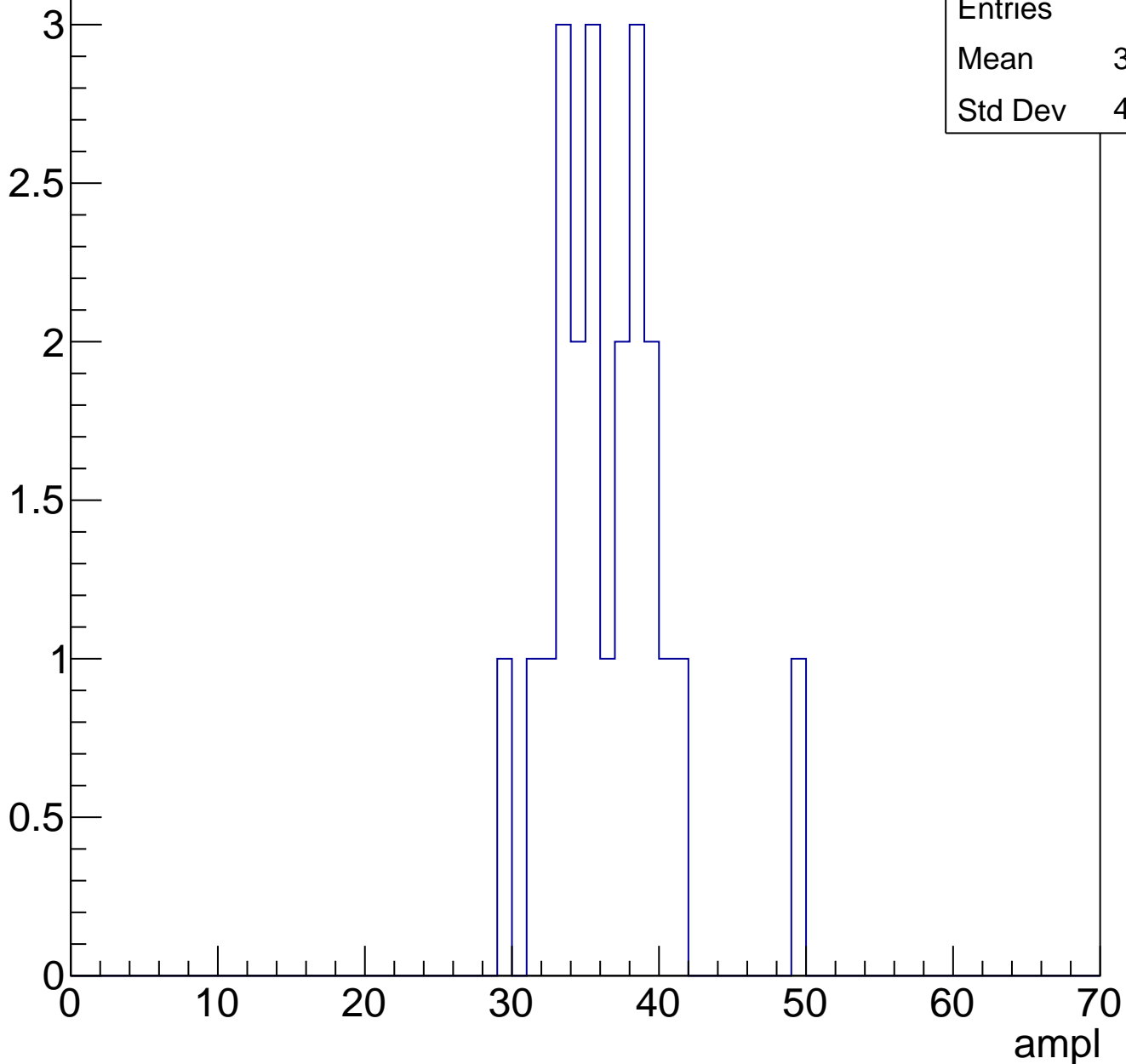
Entries	39
Mean	28.08
Std Dev	8.675



B1L103S, U14-ch17, adc1

calib_packv5_041523_1651.root, FC#0, port C2

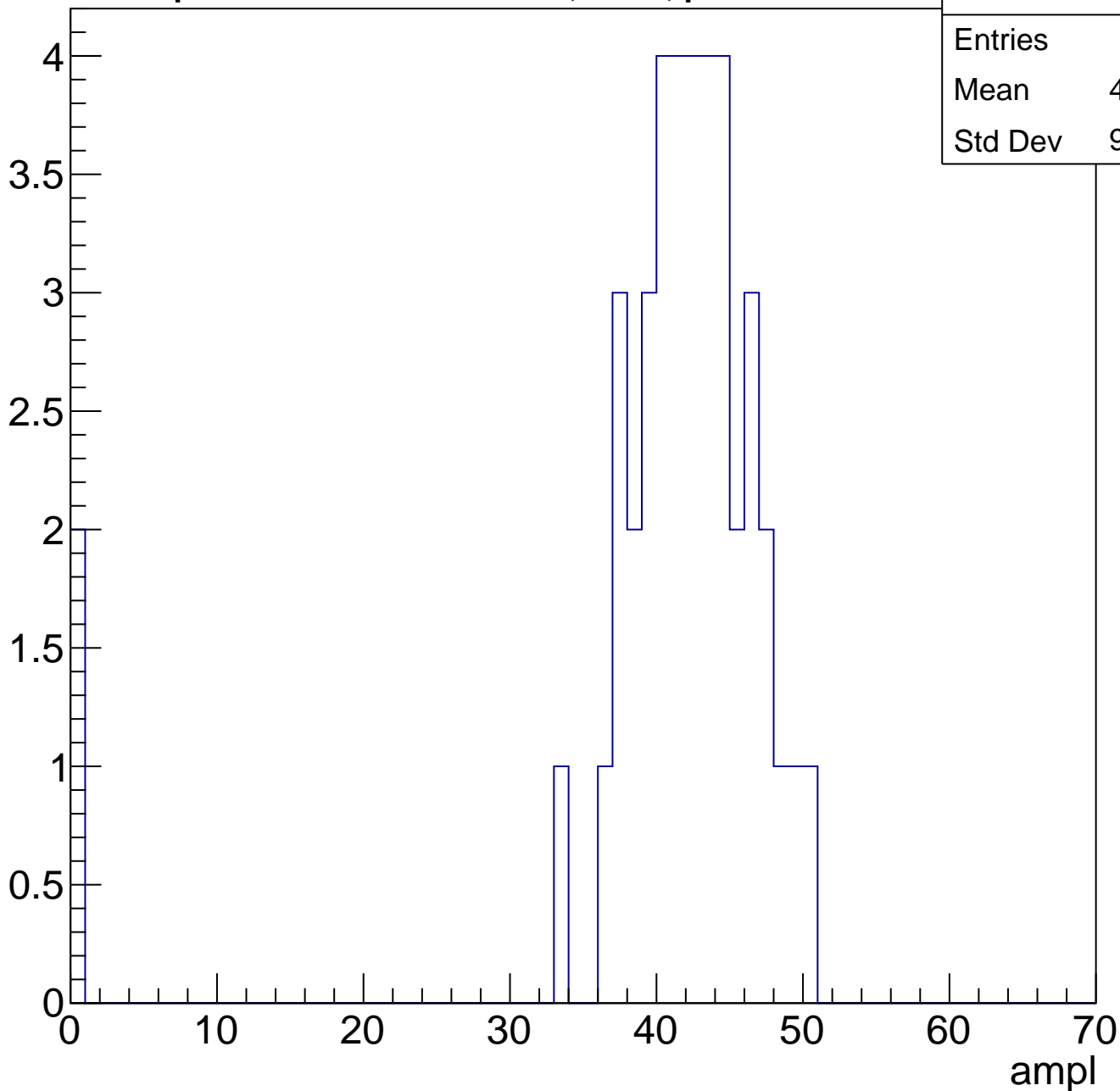
Entry



B1L103S, U14-ch17, adc2

calib_packv5_041523_1651.root, FC#0, port C2

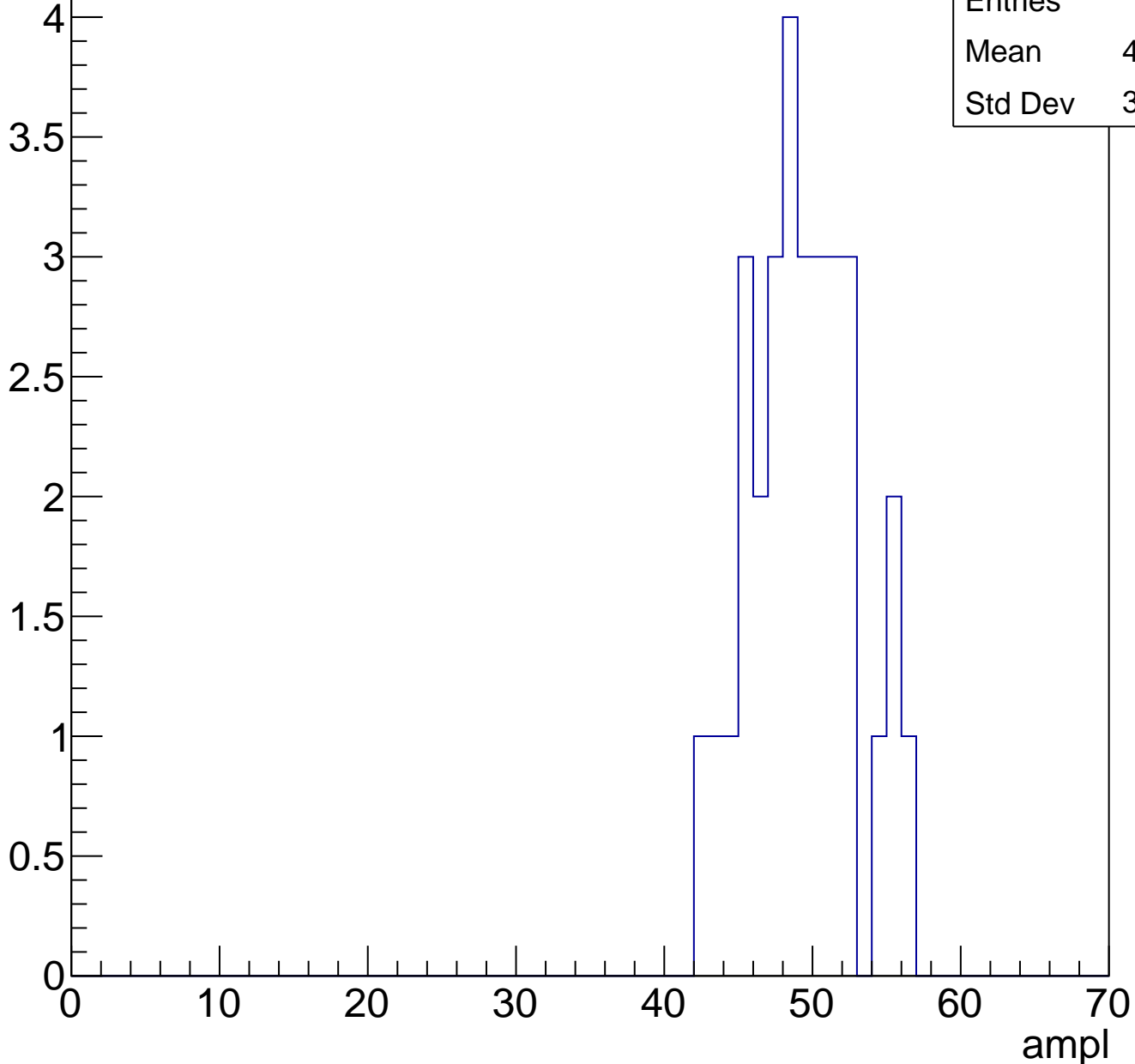
Entry



B1L103S, U14-ch17, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry



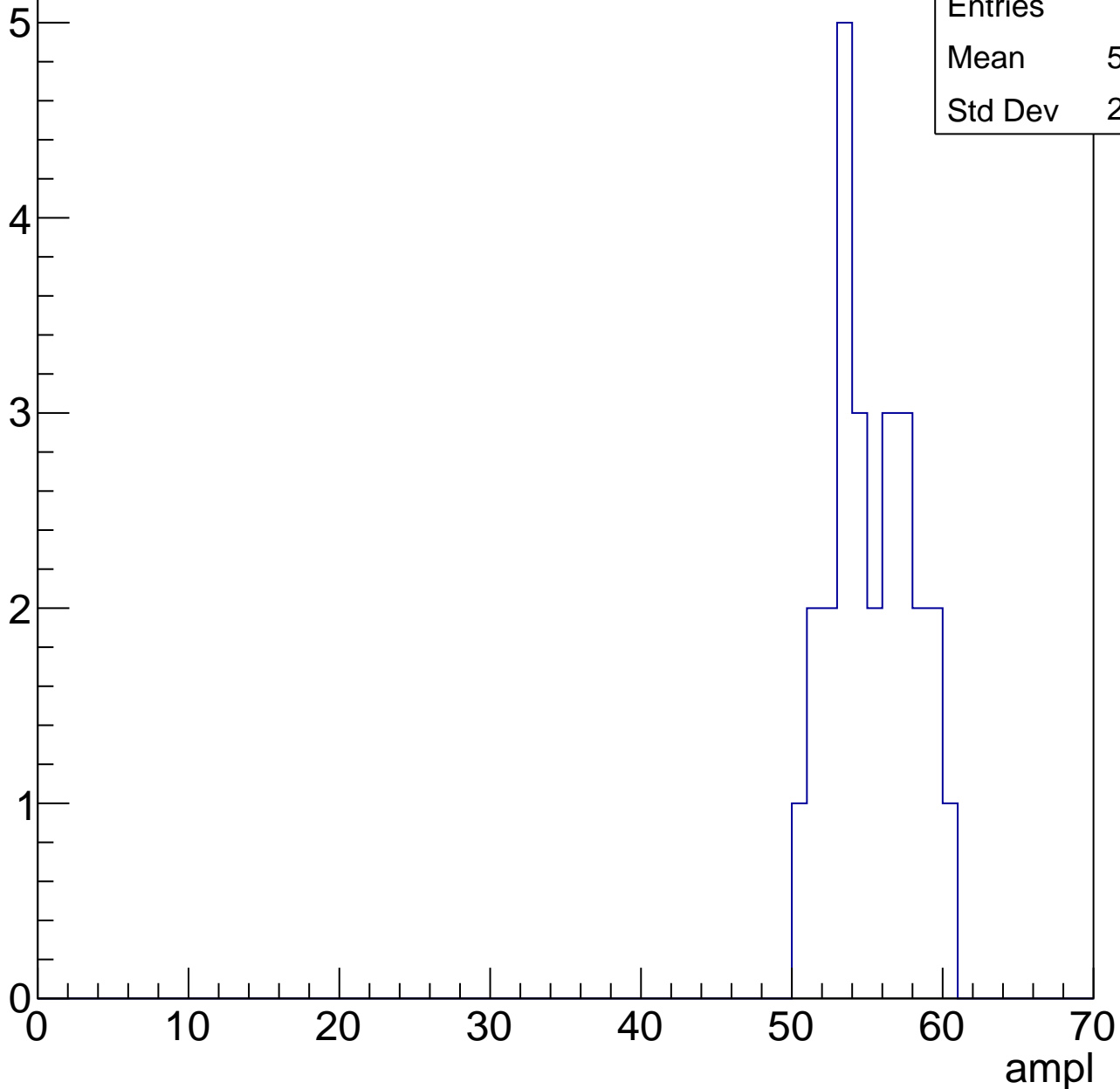
Entries	31
Mean	48.87
Std Dev	3.499

B1L103S, U14-ch17, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	26
Mean	54.85
Std Dev	2.685



B1L103S, U14-ch17, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

5

4

3

2

1

0

Entries	26
Mean	60.04
Std Dev	2.244

ampl

0

10

20

30

40

50

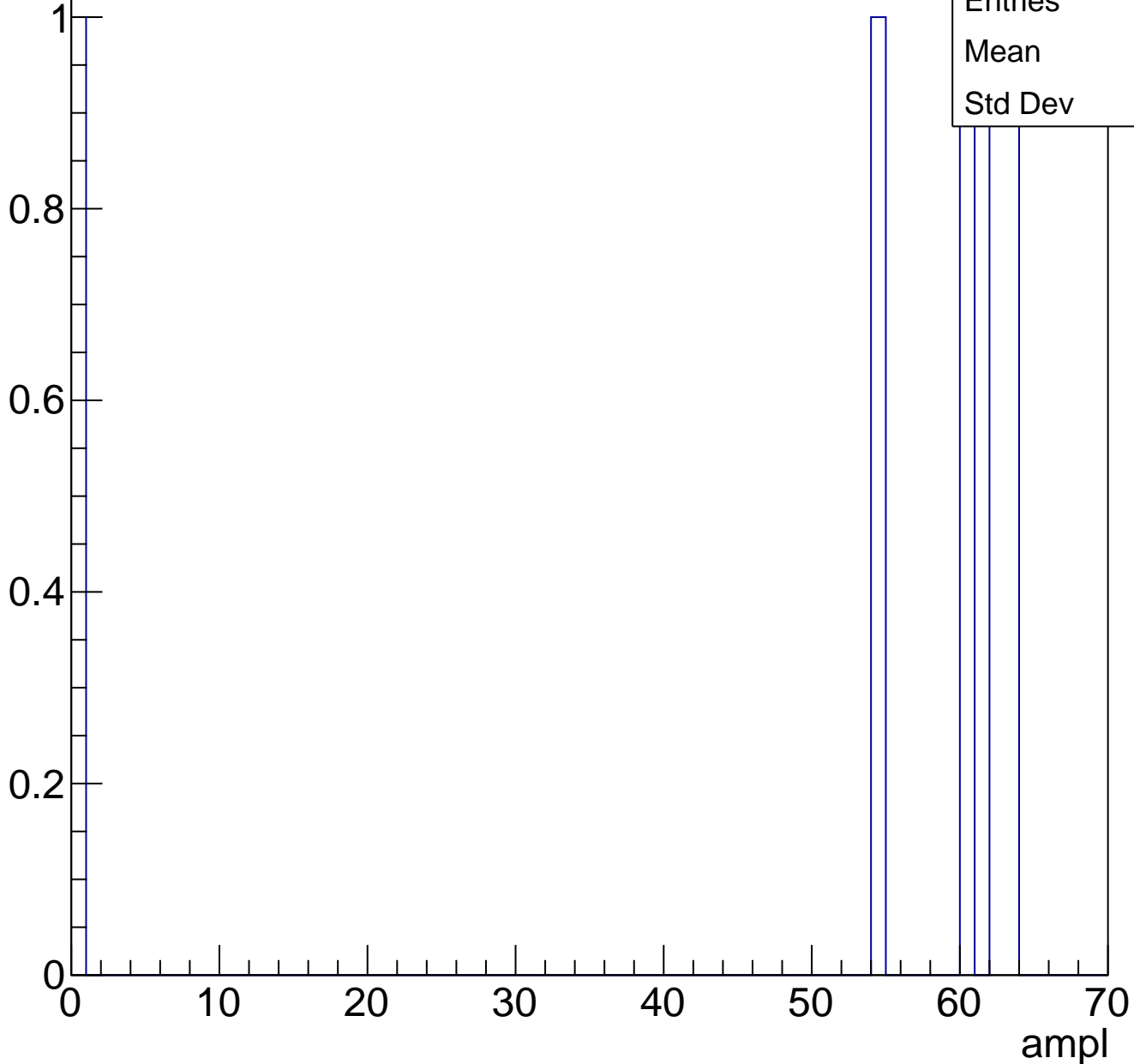
60

70

B1L103S, U14-ch17, adc6

calib_packv5_041523_1651.root, FC#0, port C2

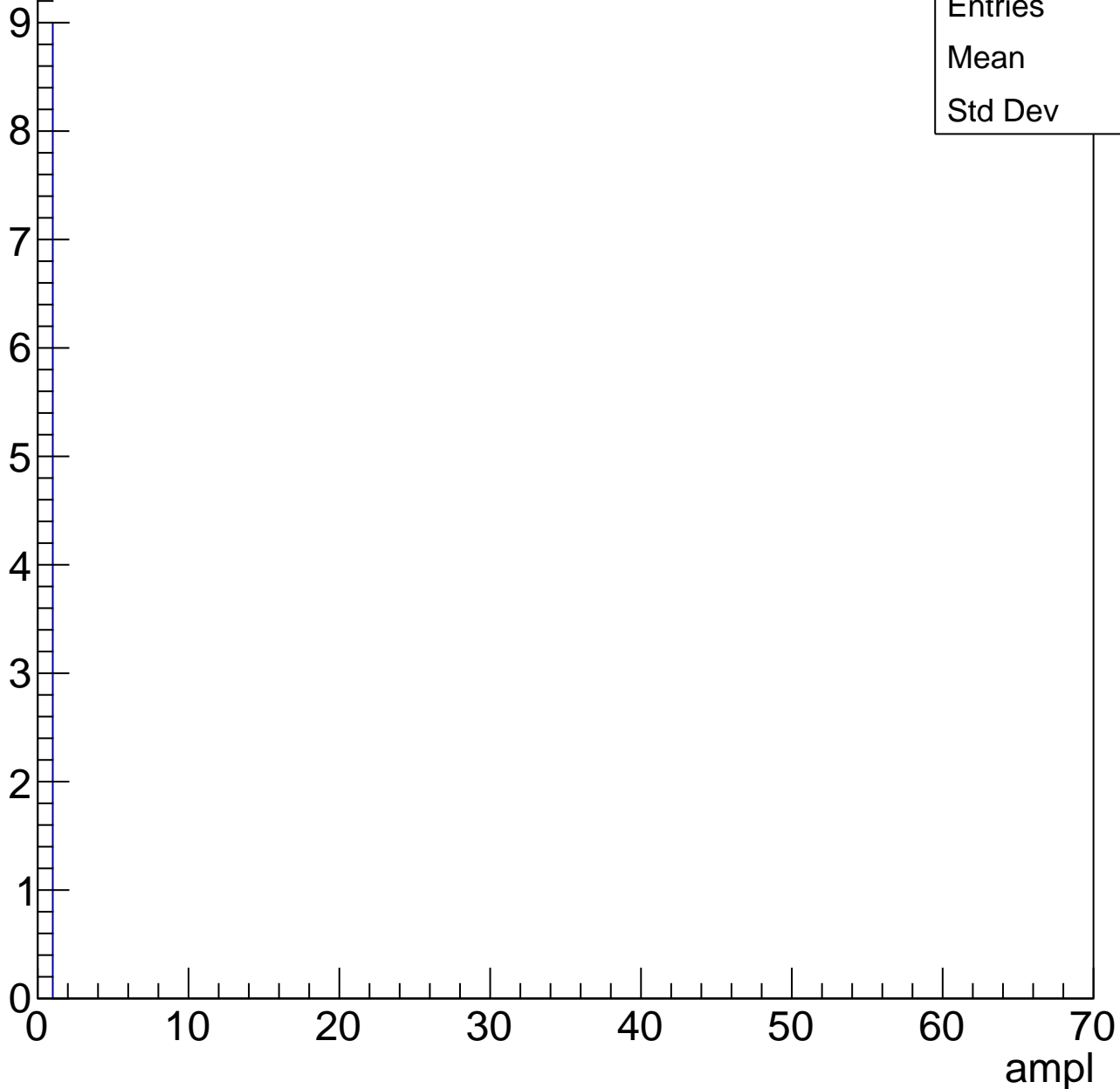
Entry



B1L103S, U14-ch17, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch18, adc0

calib_packv5_041523_1651.root, FC#0, port C2

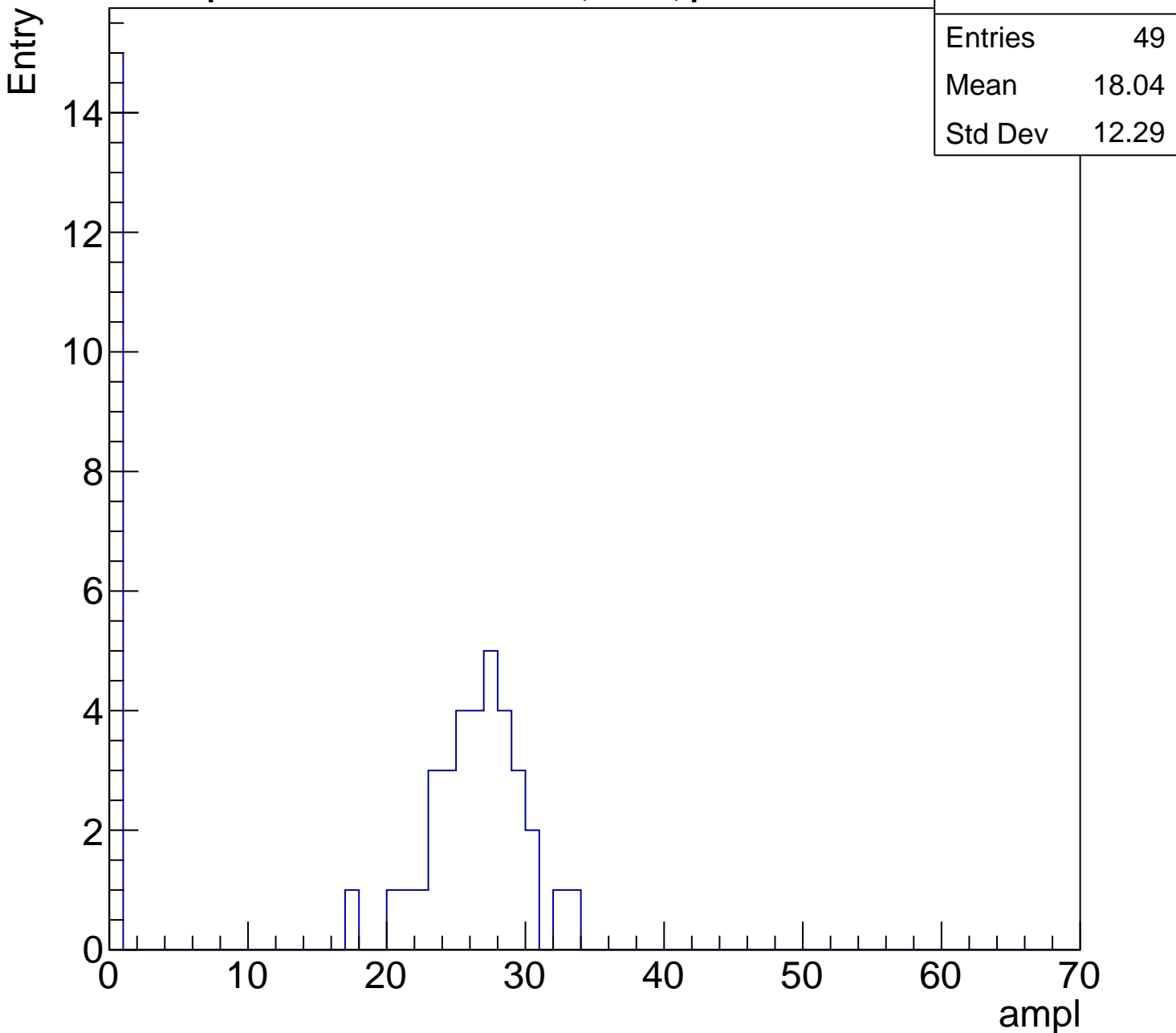
Entries	49
Mean	18.04
Std Dev	12.29

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

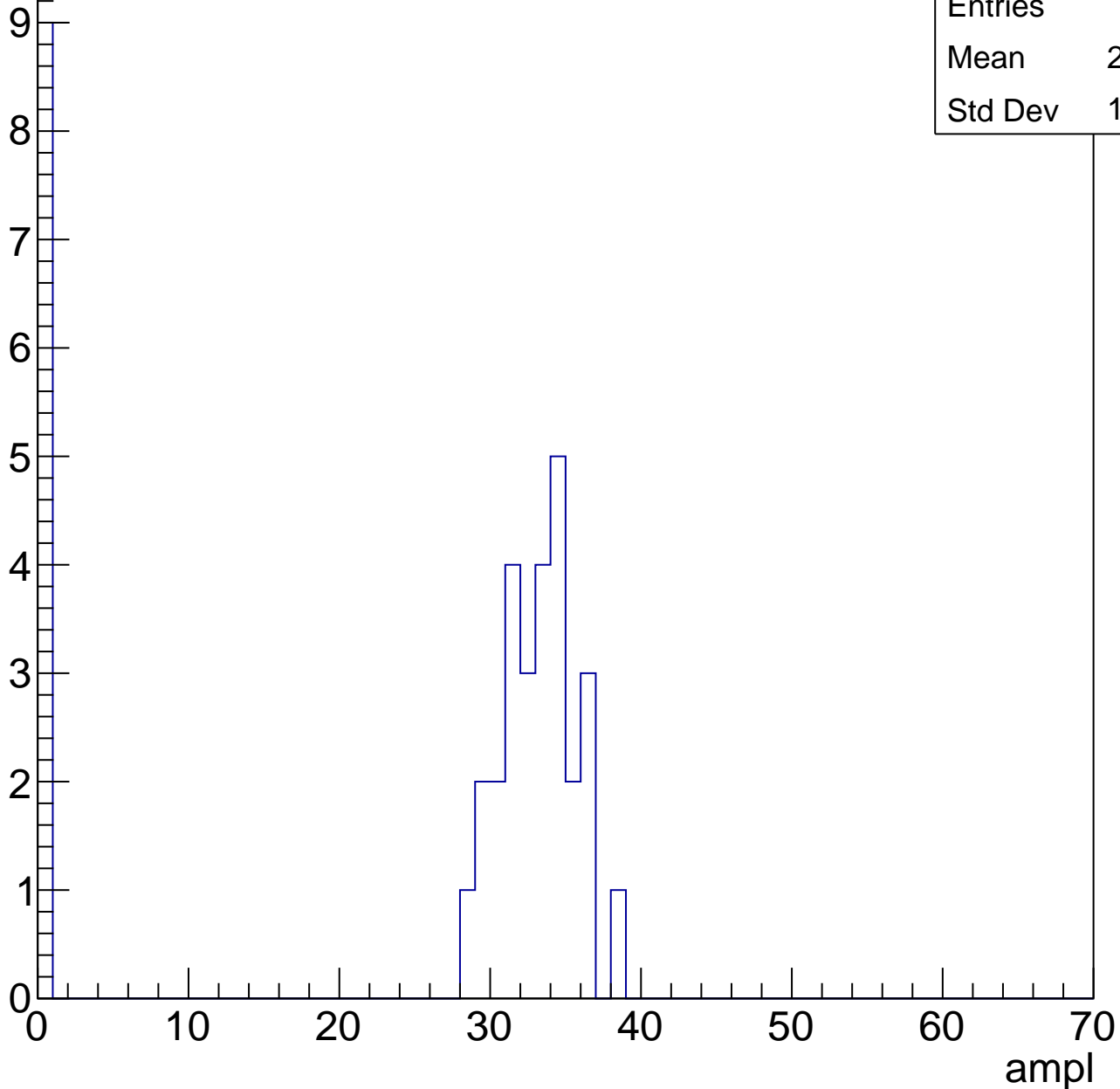


B1L103S, U14-ch18, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	36
Mean	24.56
Std Dev	14.33

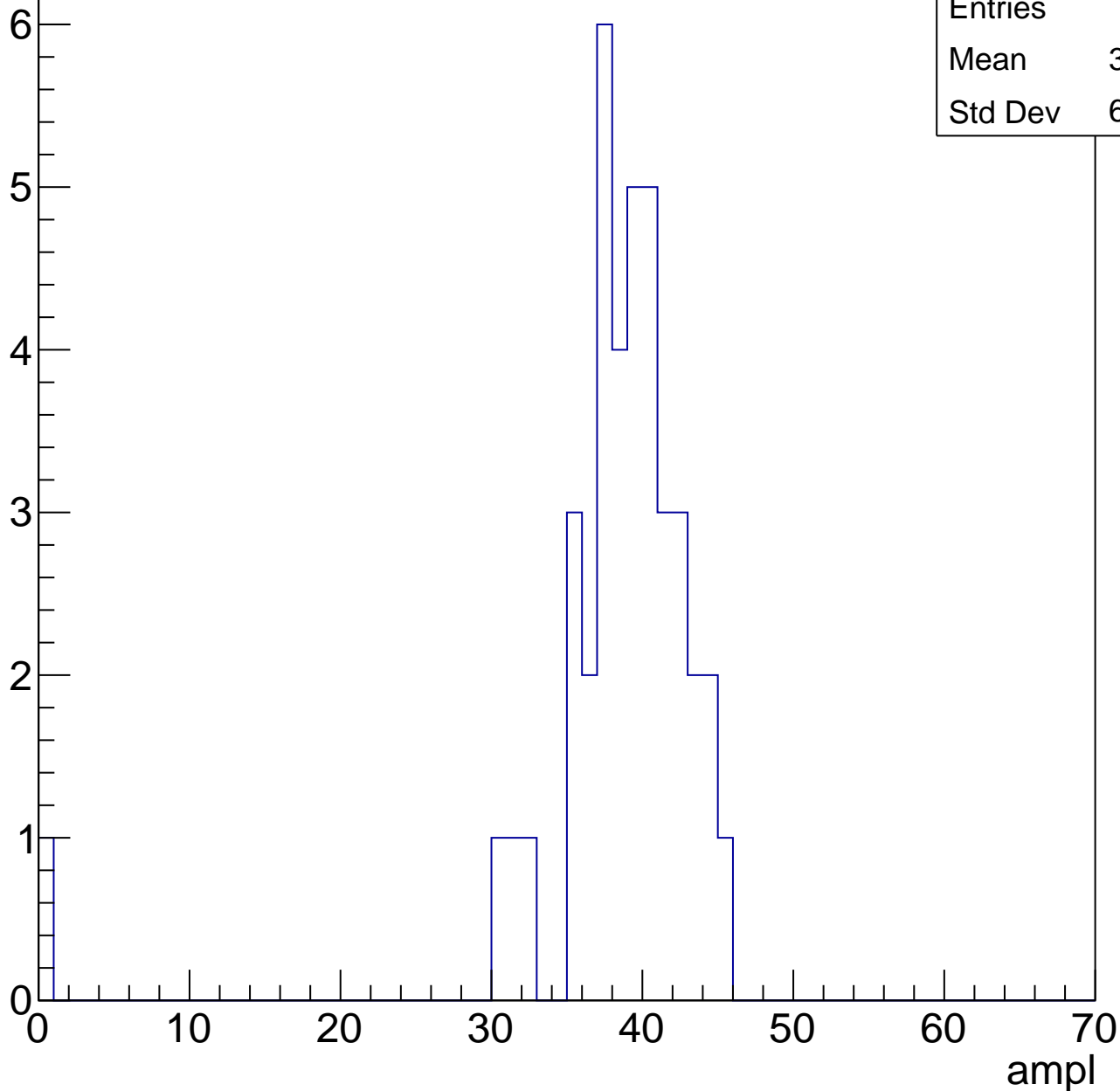


B1L103S, U14-ch18, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	37.67
Std Dev	6.893

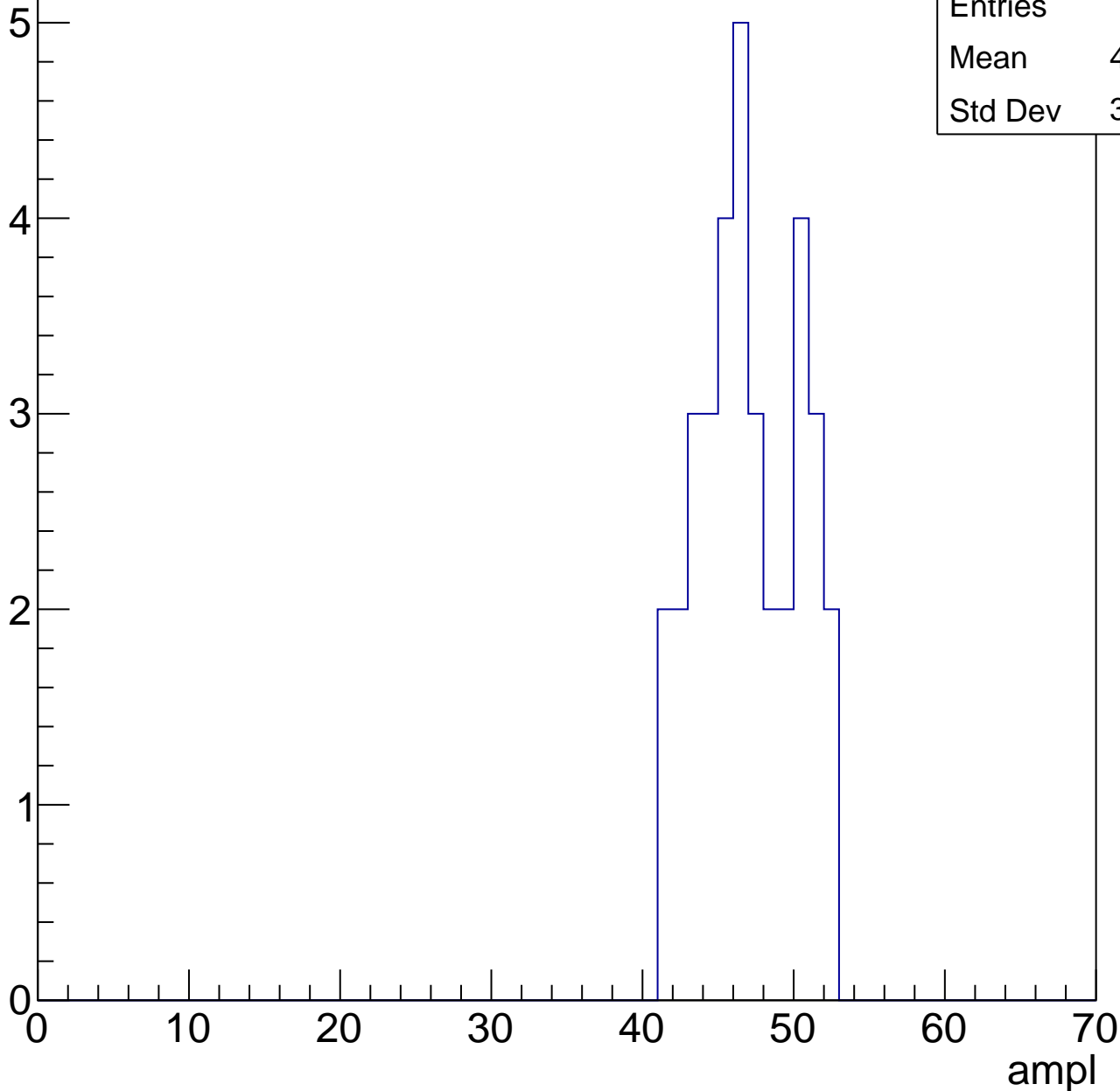


B1L103S, U14-ch18, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

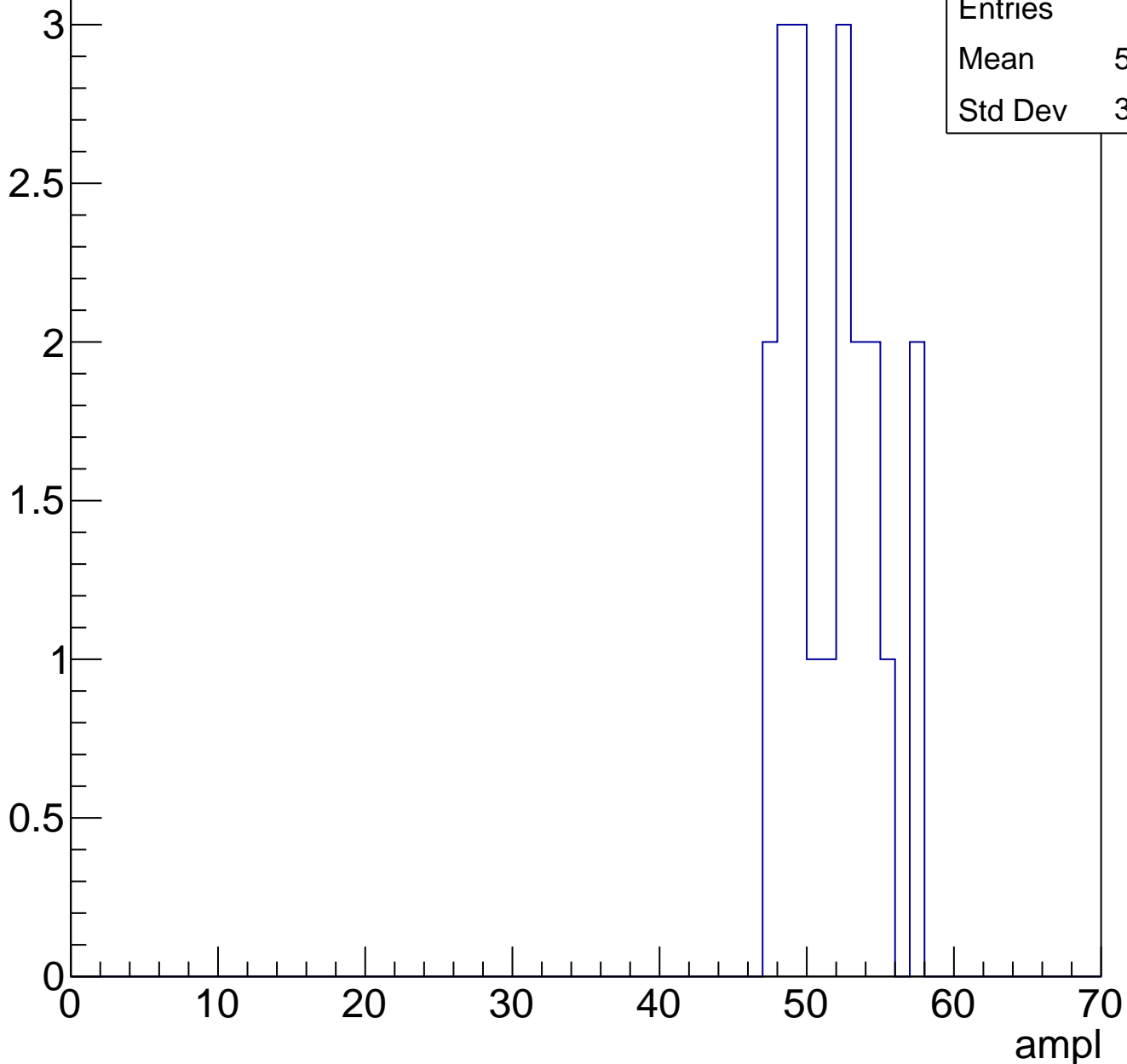
Entries	35
Mean	46.54
Std Dev	3.183



B1L103S, U14-ch18, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

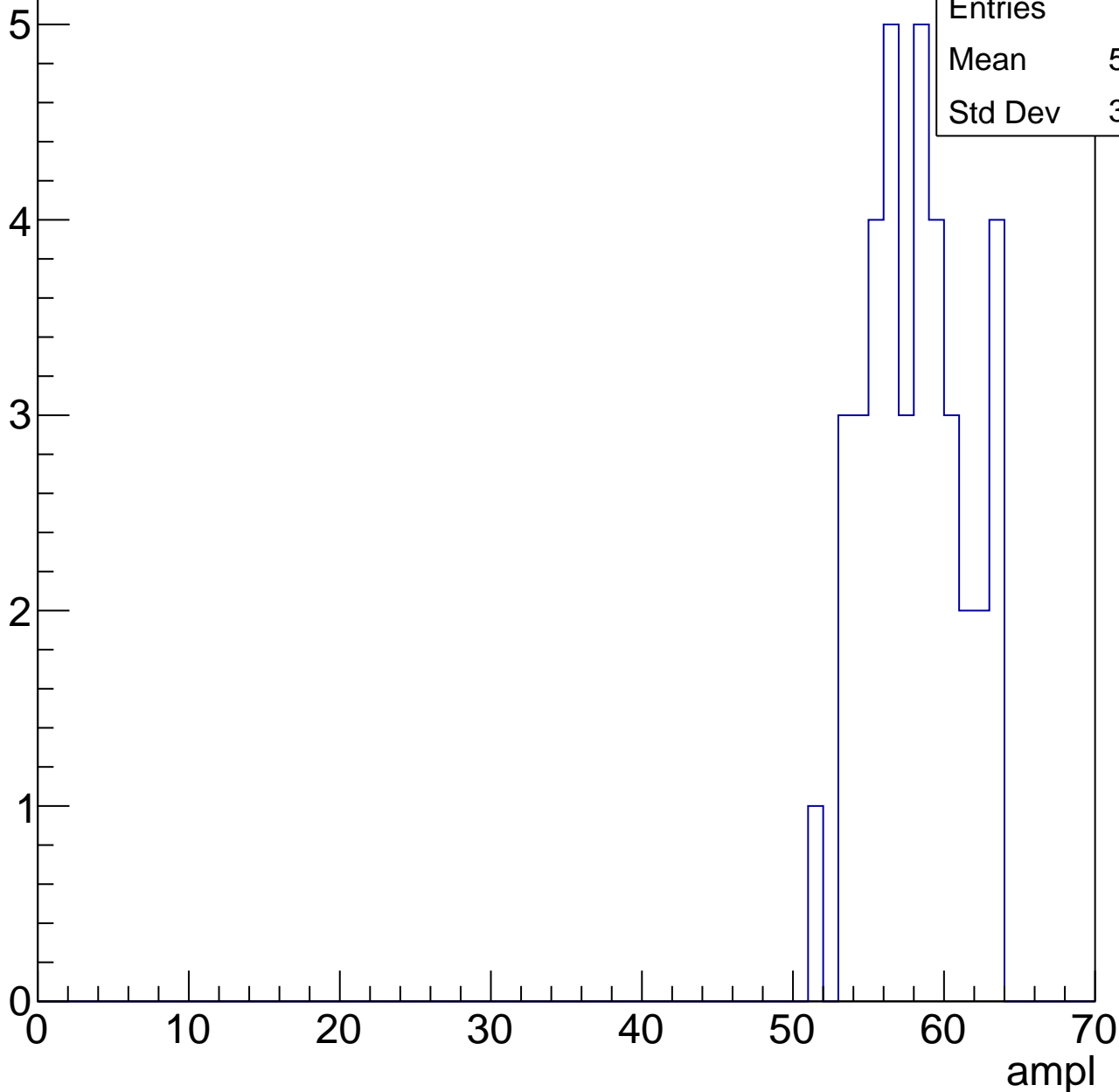


B1L103S, U14-ch18, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	57.62
Std Dev	3.167



B1L103S, U14-ch18, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

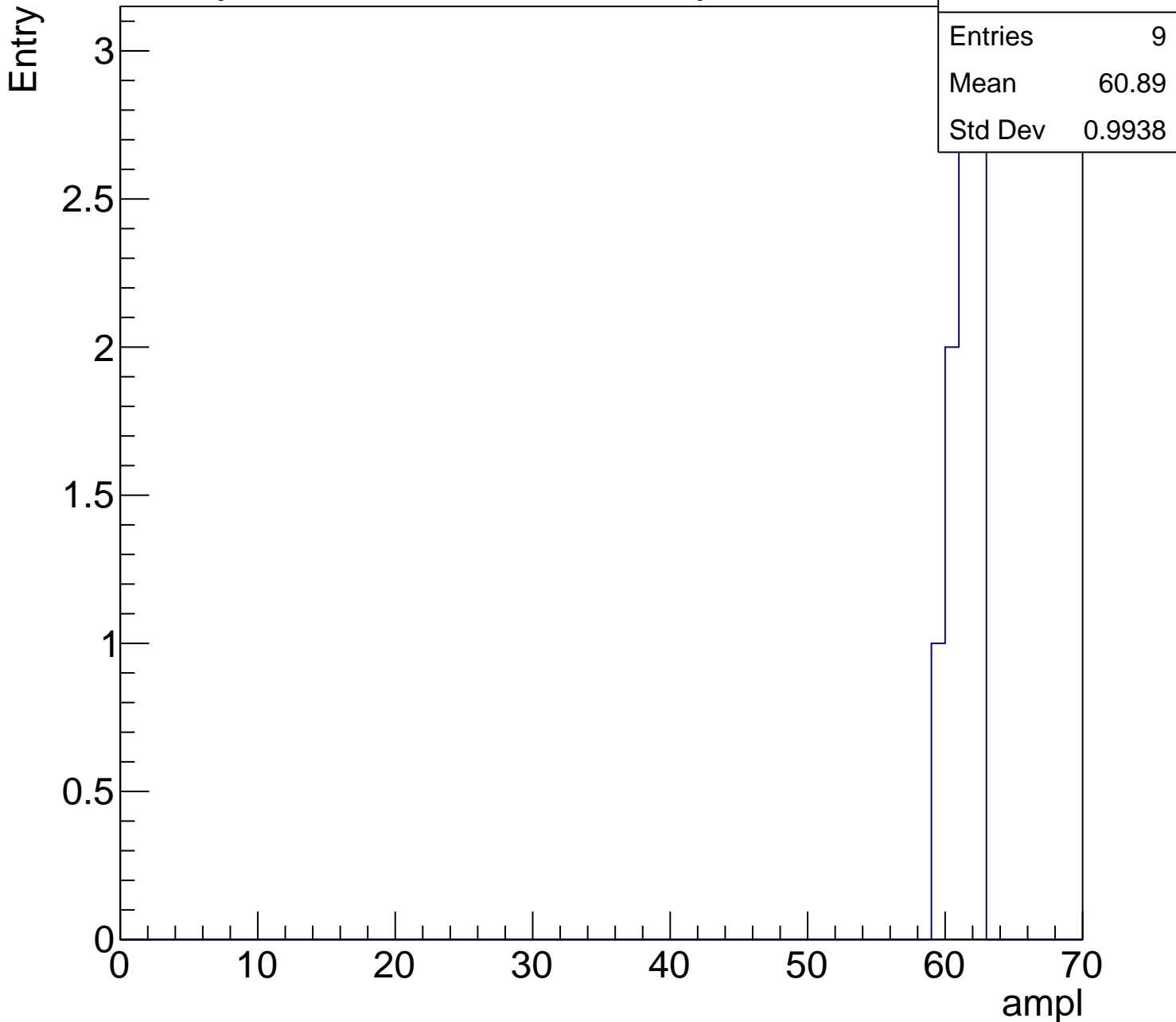
9

Mean

60.89

Std Dev

0.9938

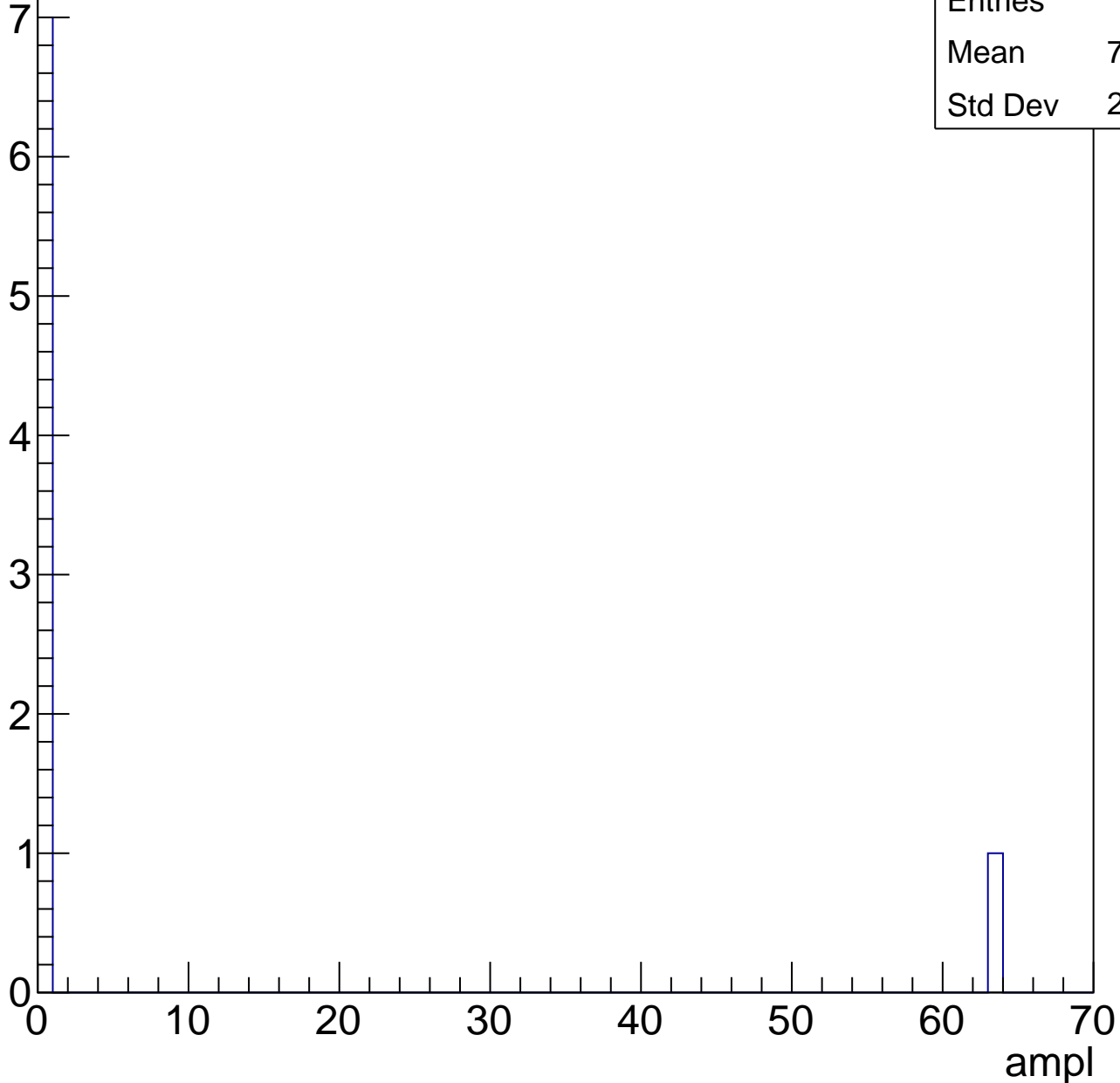


B1L103S, U14-ch18, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	8
Mean	7.875
Std Dev	20.84

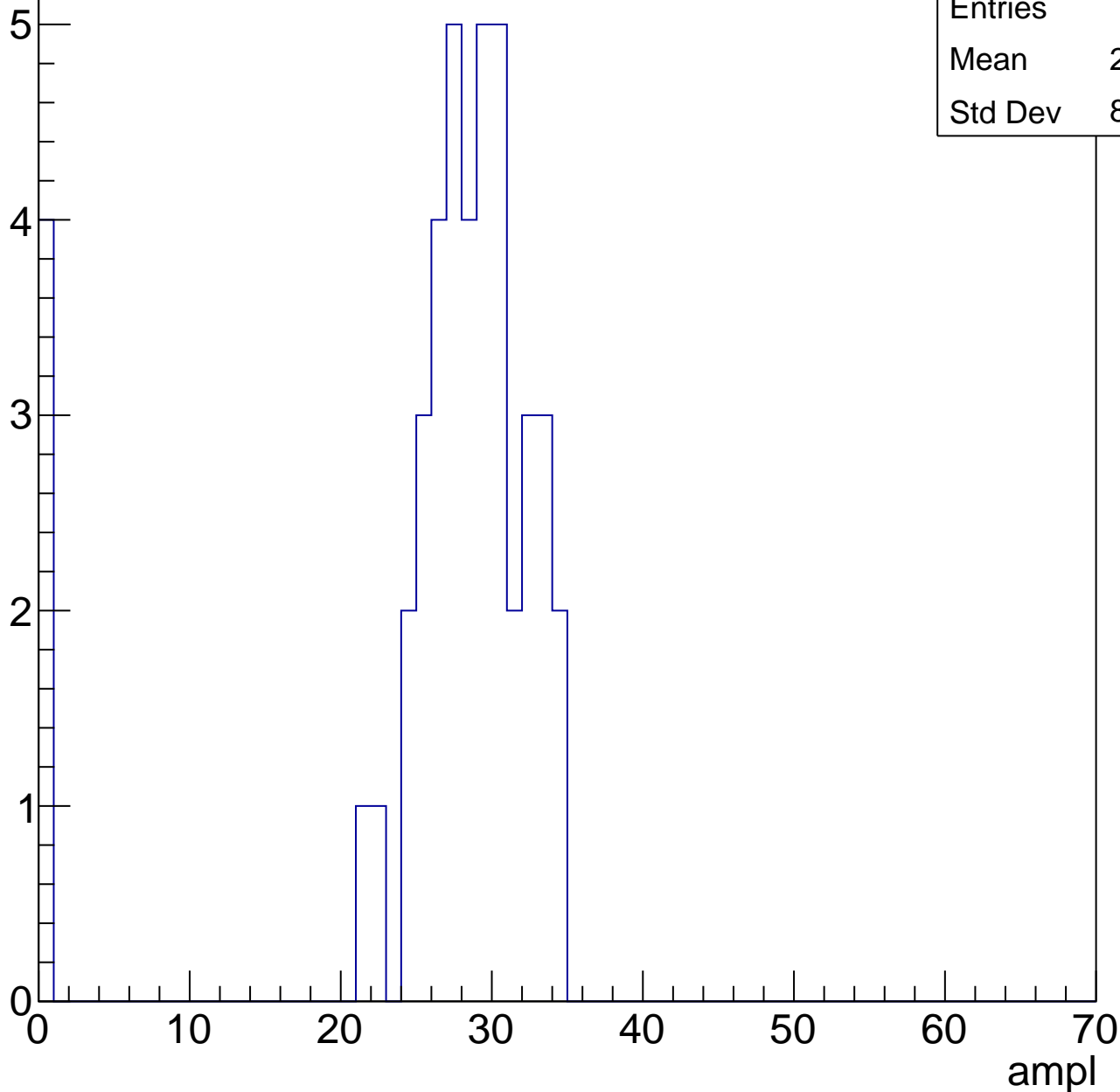


B1L103S, U14-ch19, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	44
Mean	25.84
Std Dev	8.705

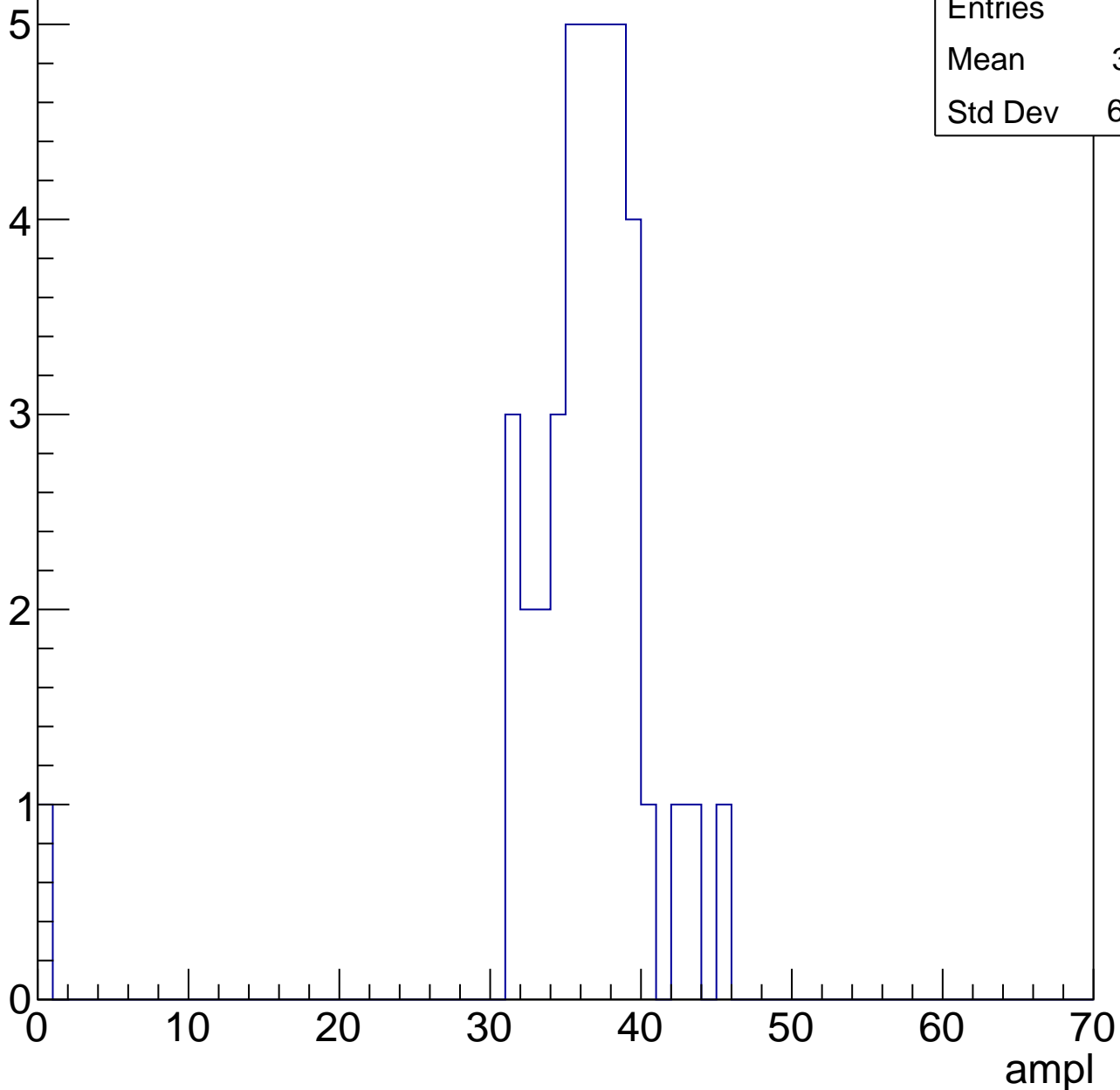


B1L103S, U14-ch19, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	35.41
Std Dev	6.539

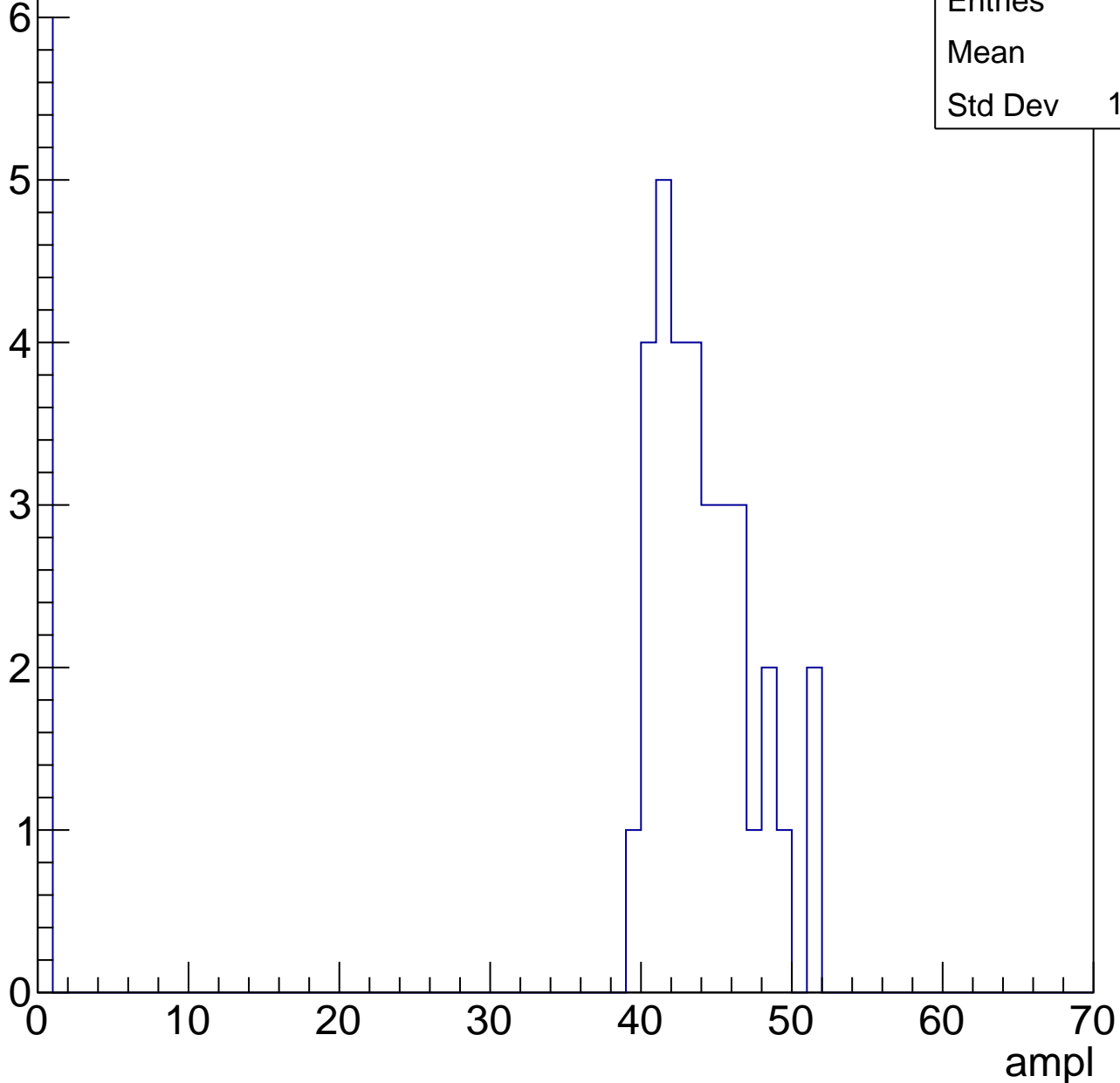


B1L103S, U14-ch19, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	37
Std Dev	16.04

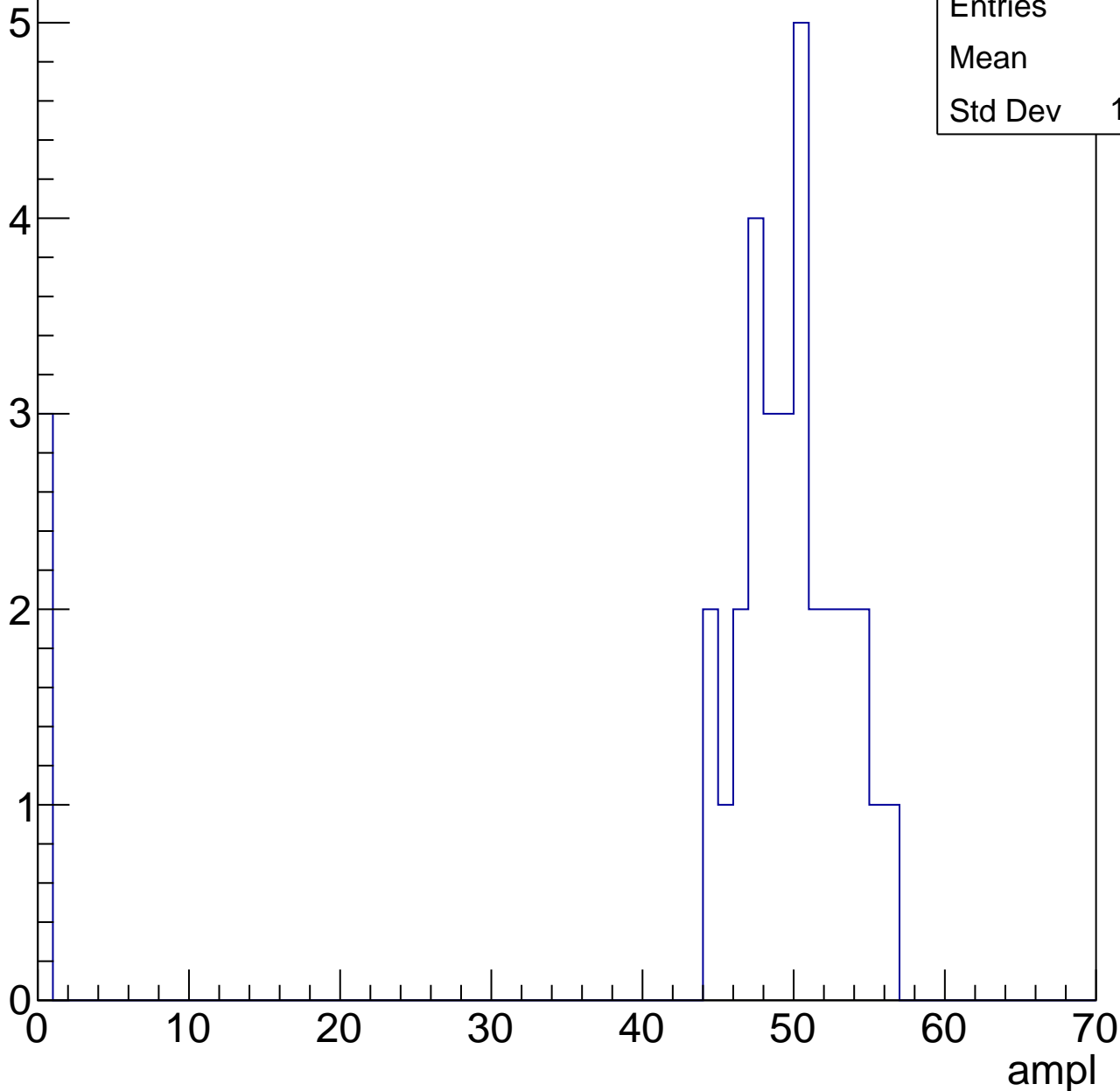


B1L103S, U14-ch19, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

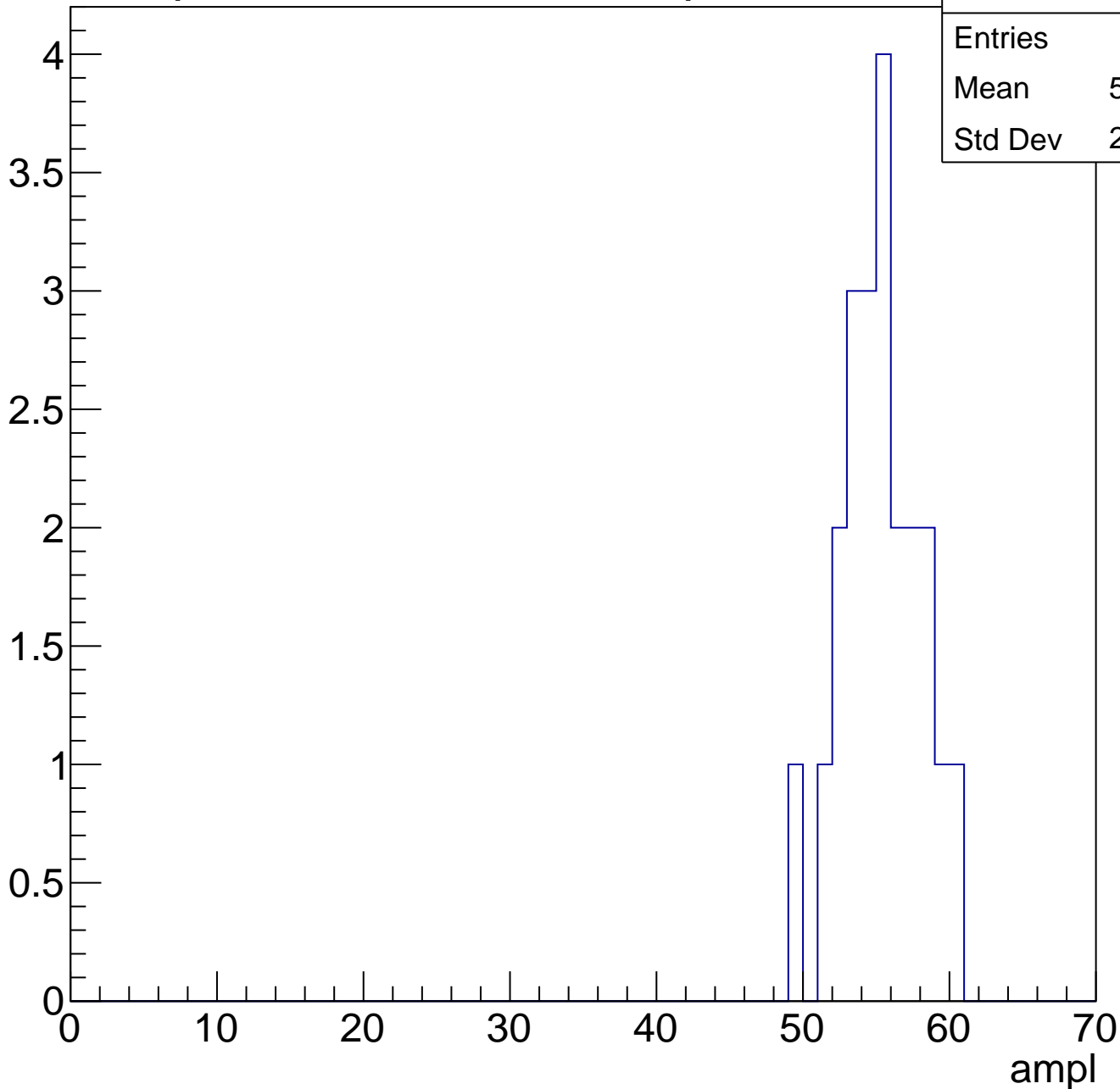
Entries	33
Mean	45
Std Dev	14.54



B1L103S, U14-ch19, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

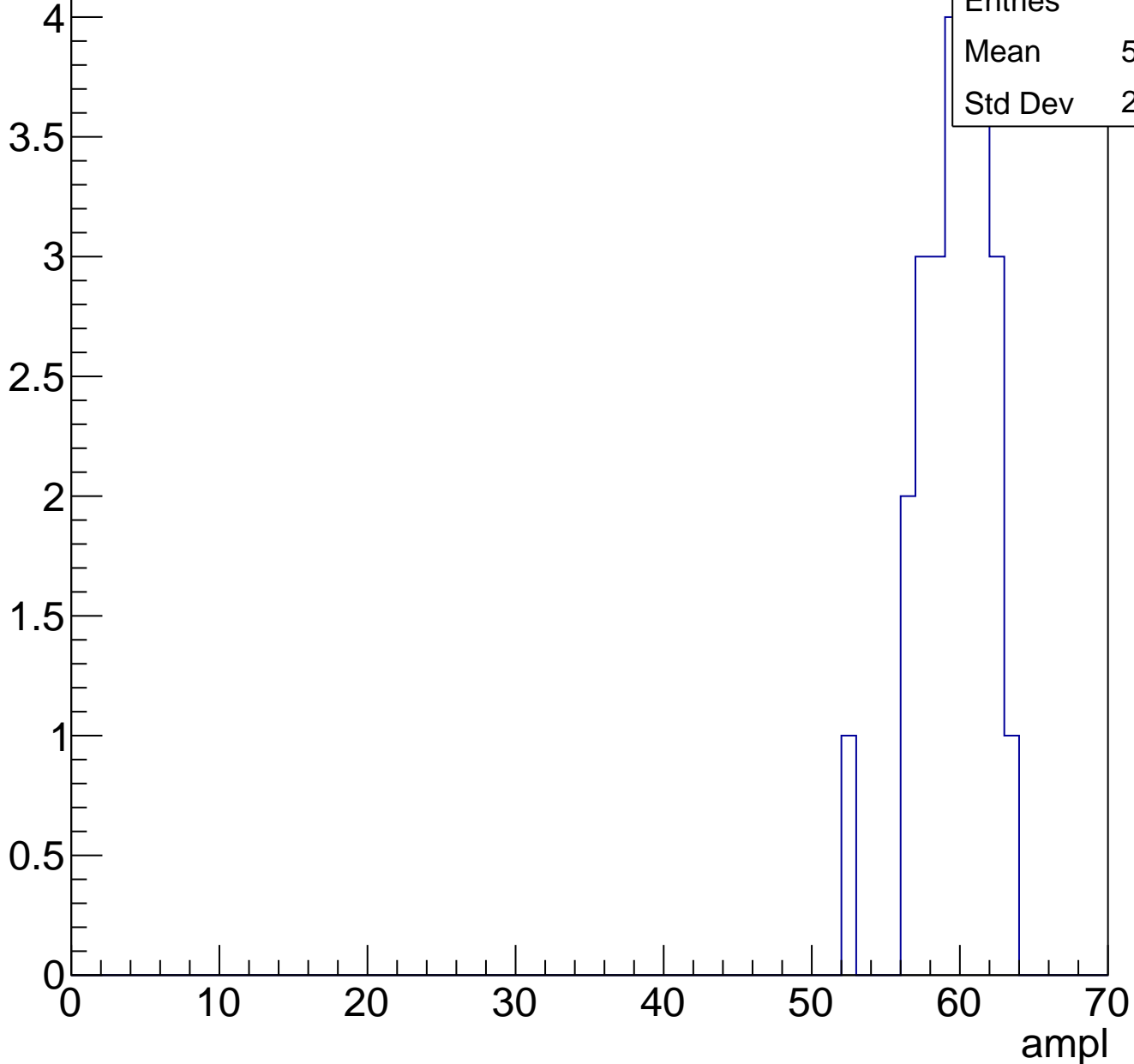


Entries	22
Mean	54.82
Std Dev	2.639

B1L103S, U14-ch19, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch19, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

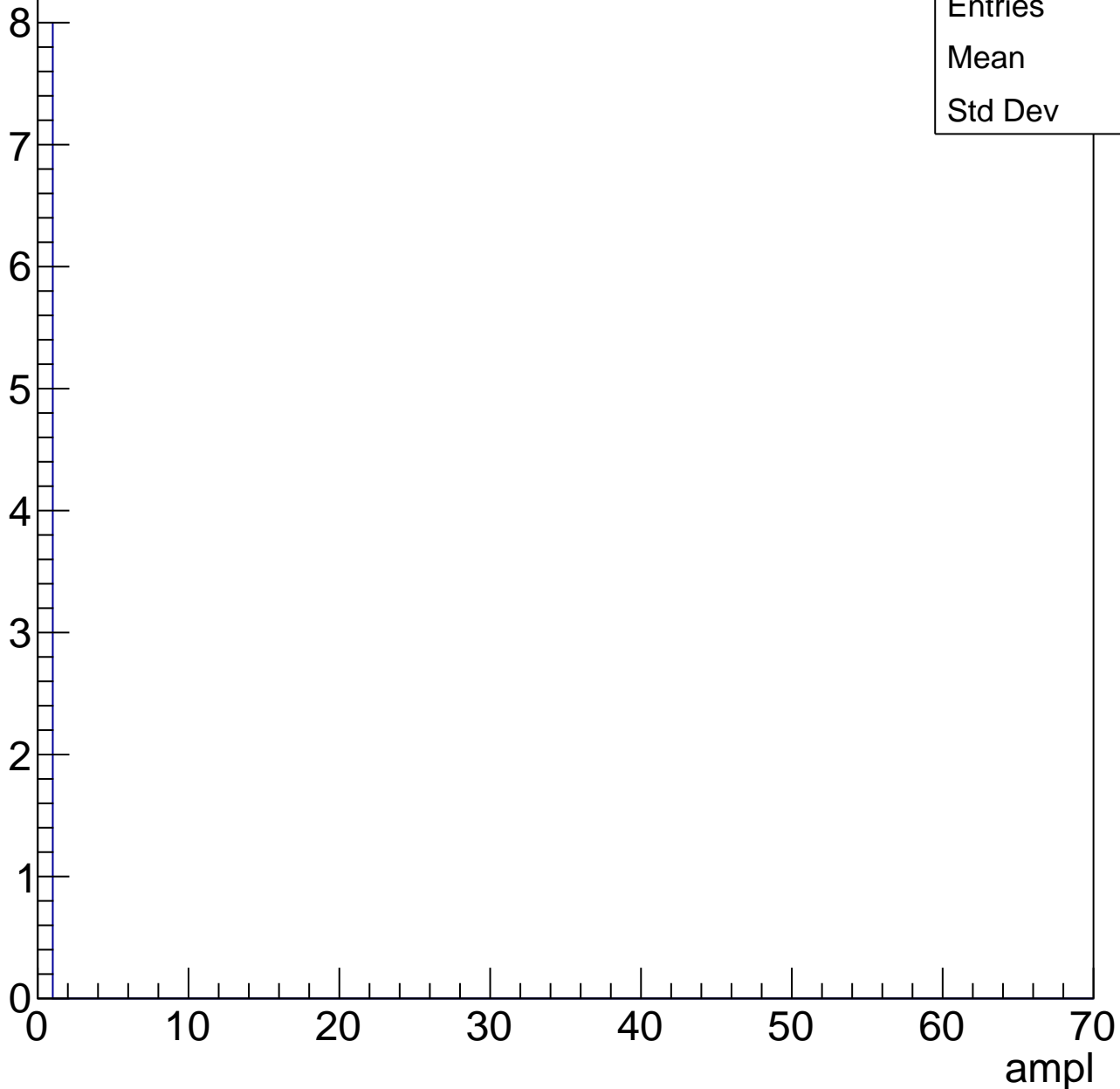


B1L103S, U14-ch19, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	8
Mean	0
Std Dev	0



B1L103S, U14-ch20, adc0

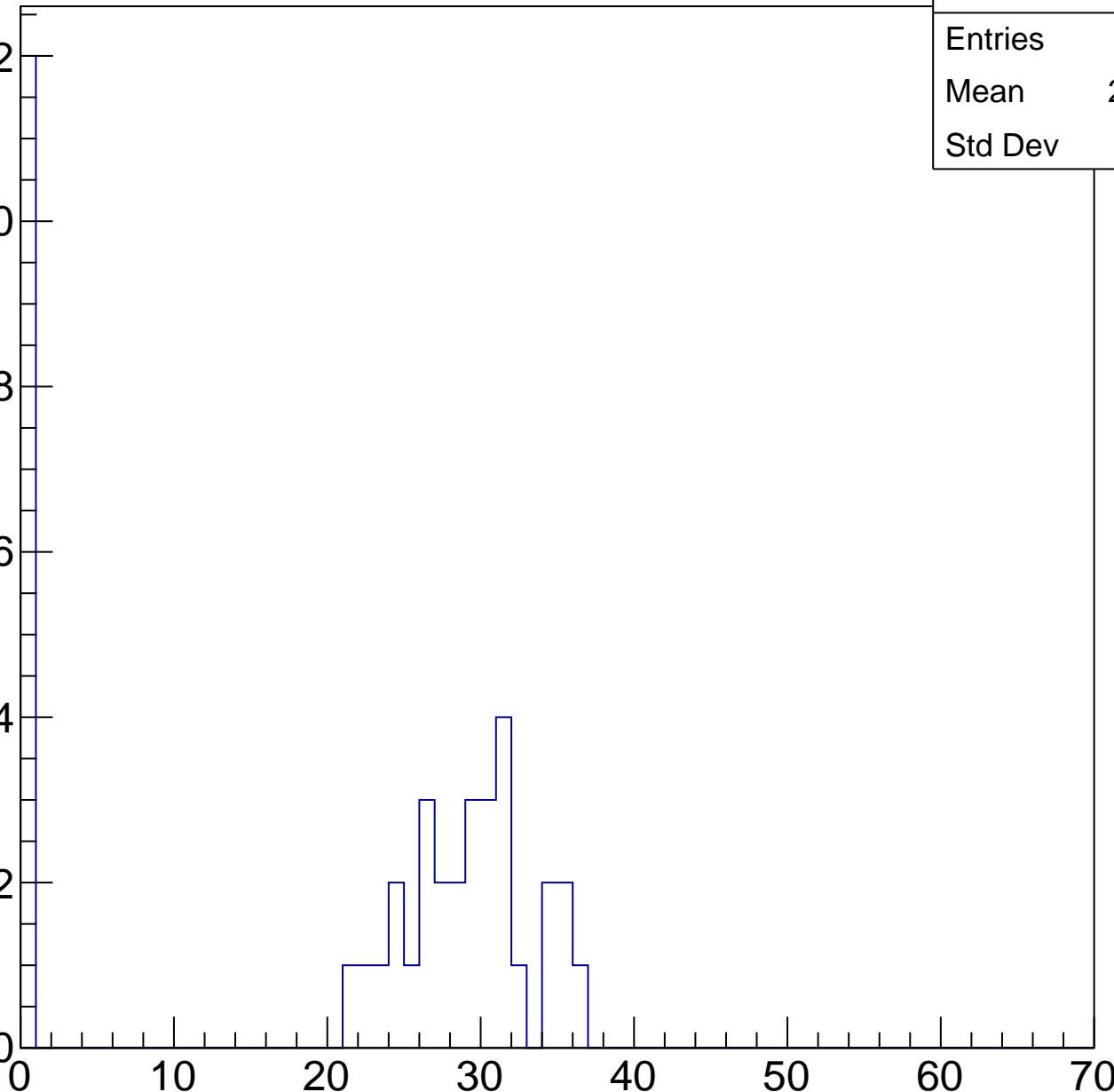
calib_packv5_041523_1651.root, FC#0, port C2

Entry

12
10
8
6
4
2
0

Entries	41
Mean	20.34
Std Dev	13.5

ampl

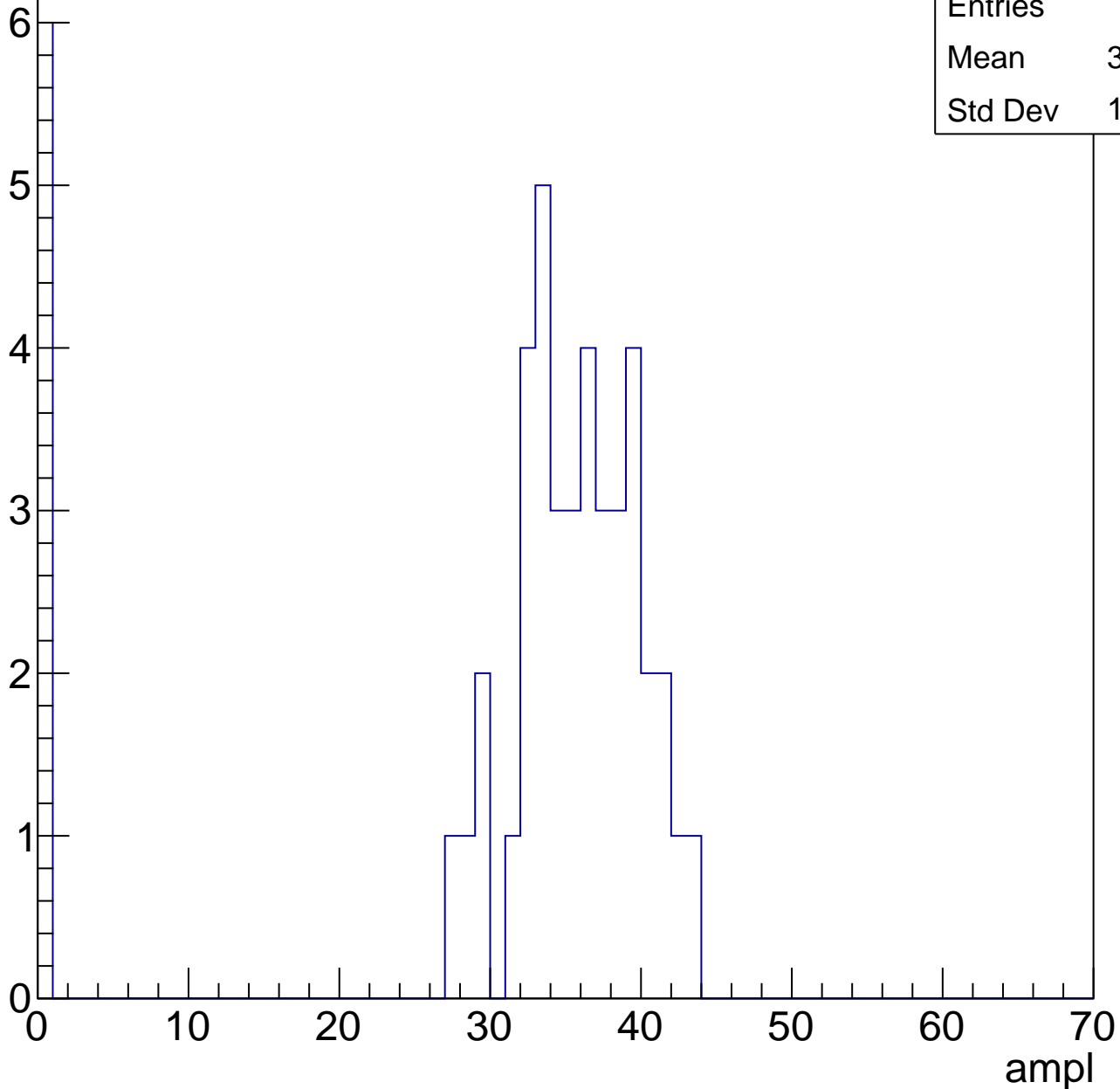


B1L103S, U14-ch20, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

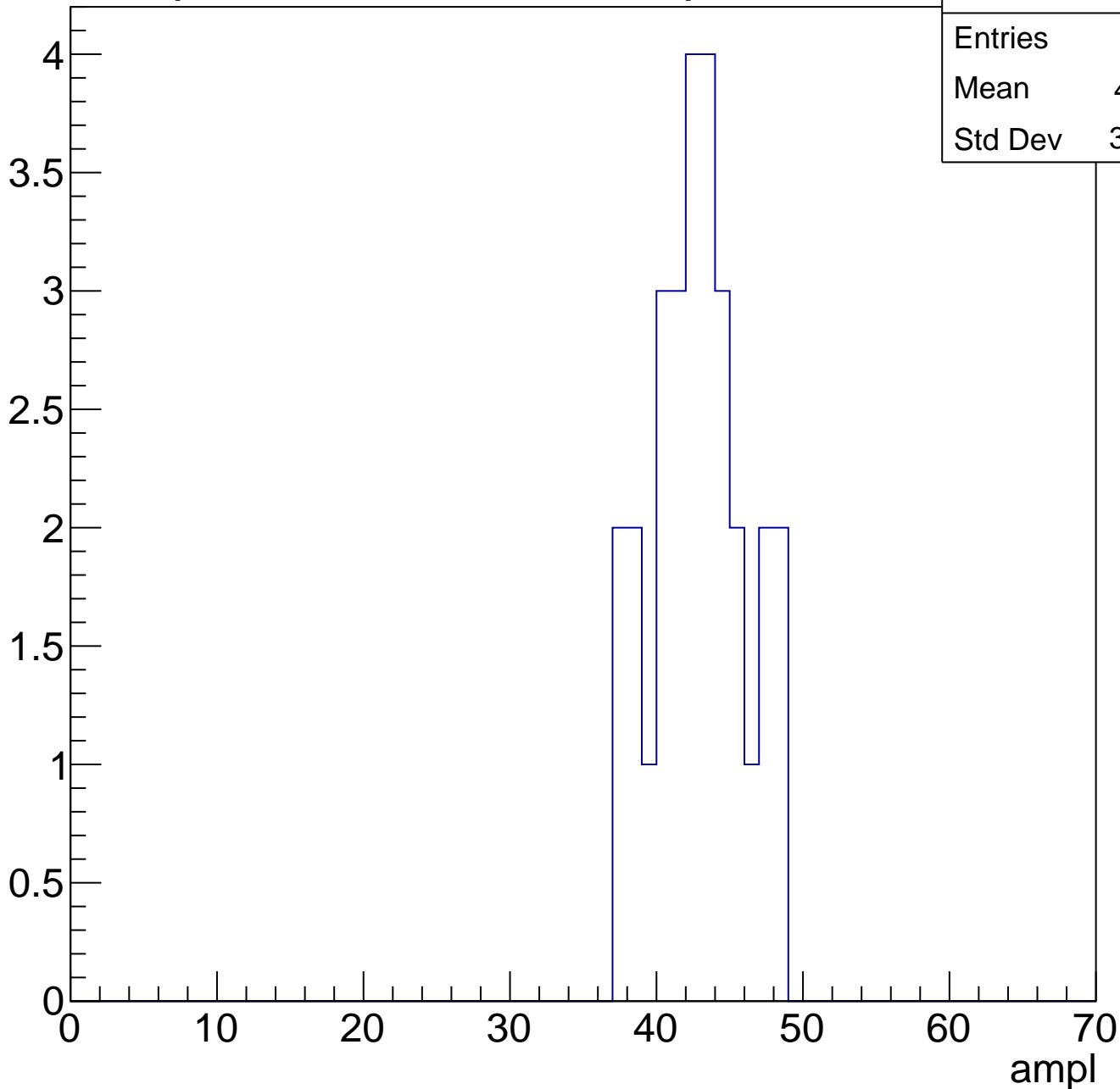
Entries	46
Mean	30.78
Std Dev	12.45



B1L103S, U14-ch20, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch20, adc3

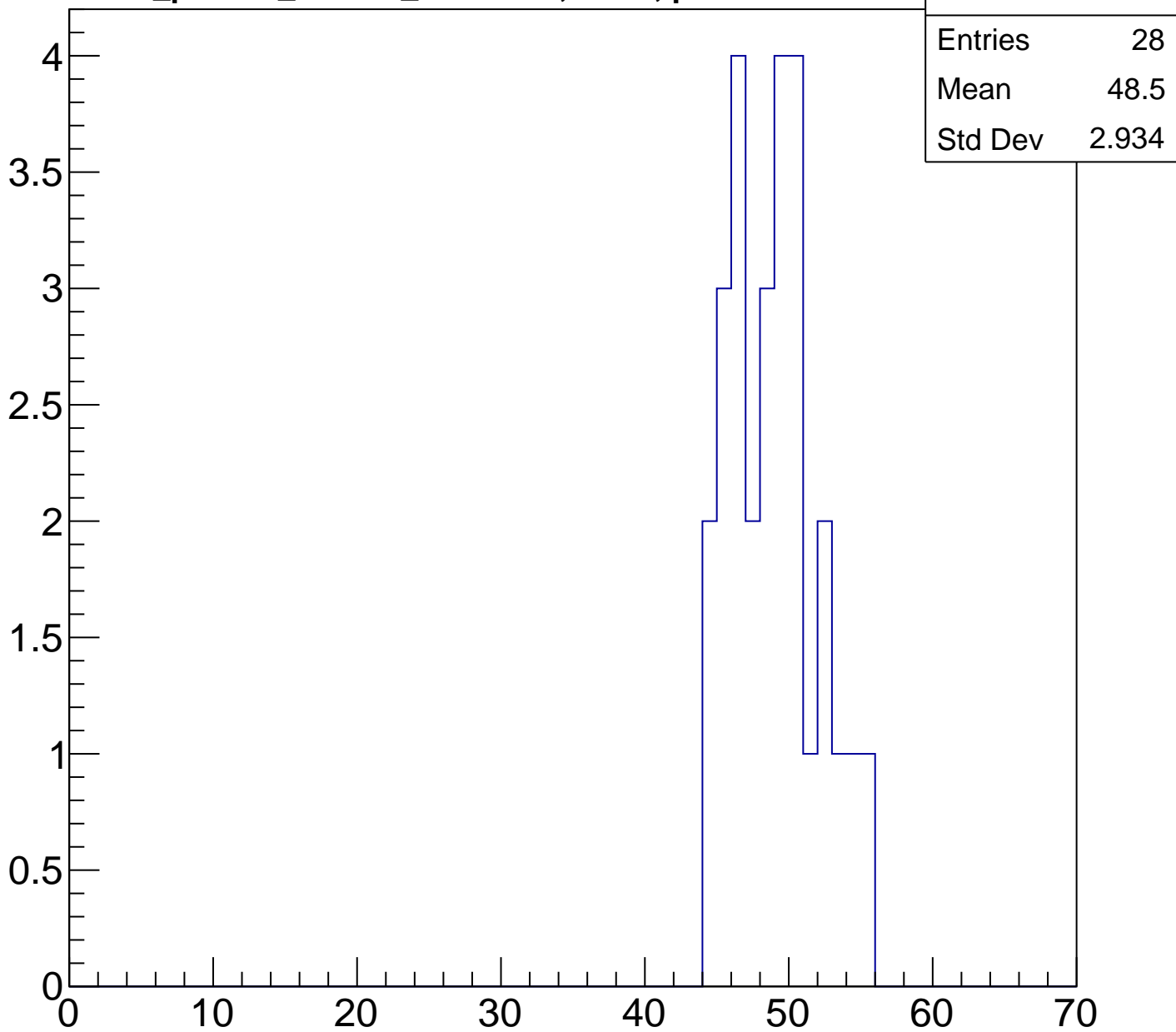
calib_packv5_041523_1651.root, FC#0, port C2

Entry

4
3.5
3
2.5
2
1.5
1
0.5
0

Entries	28
Mean	48.5
Std Dev	2.934

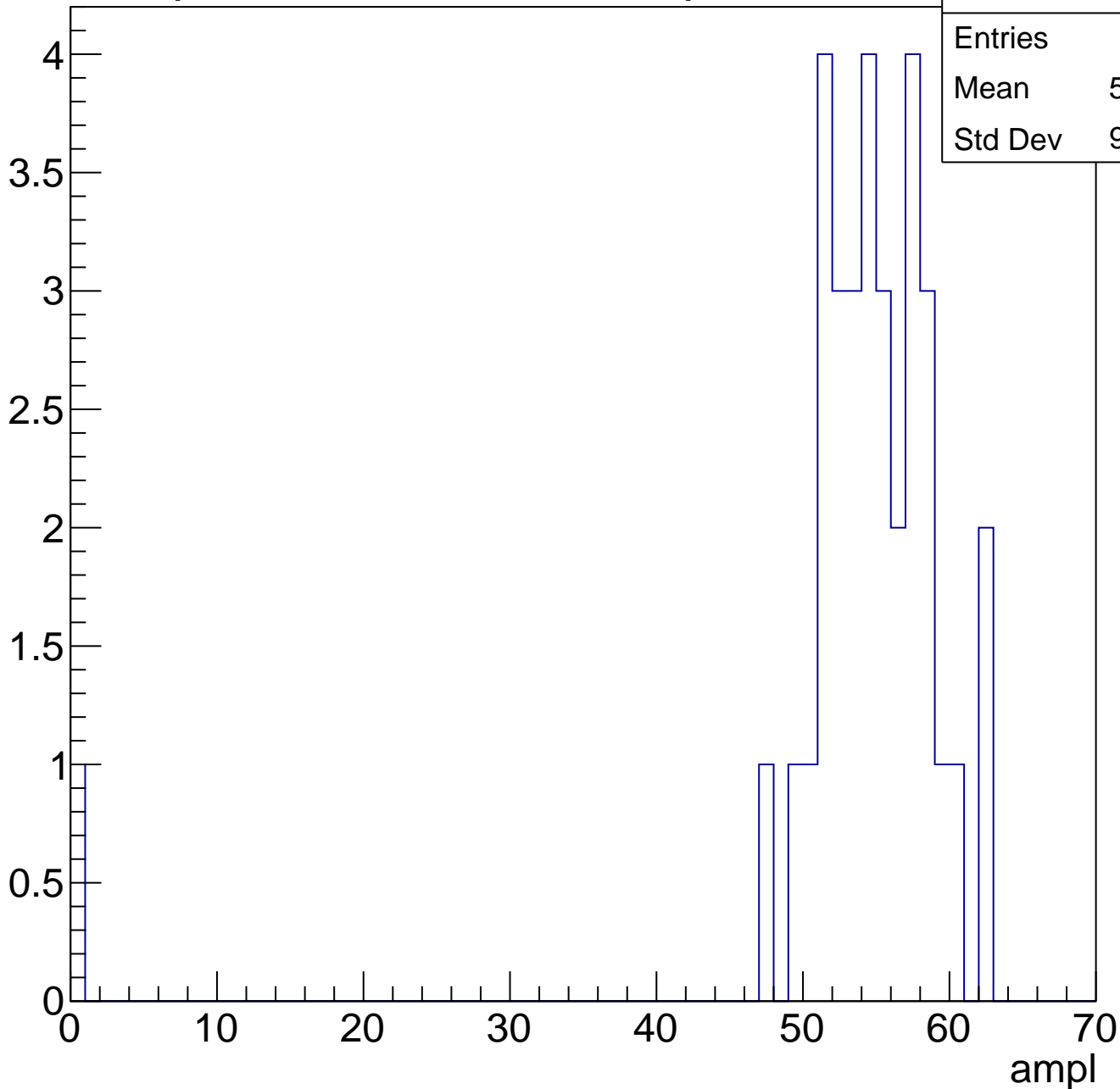
ampl



B1L103S, U14-ch20, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

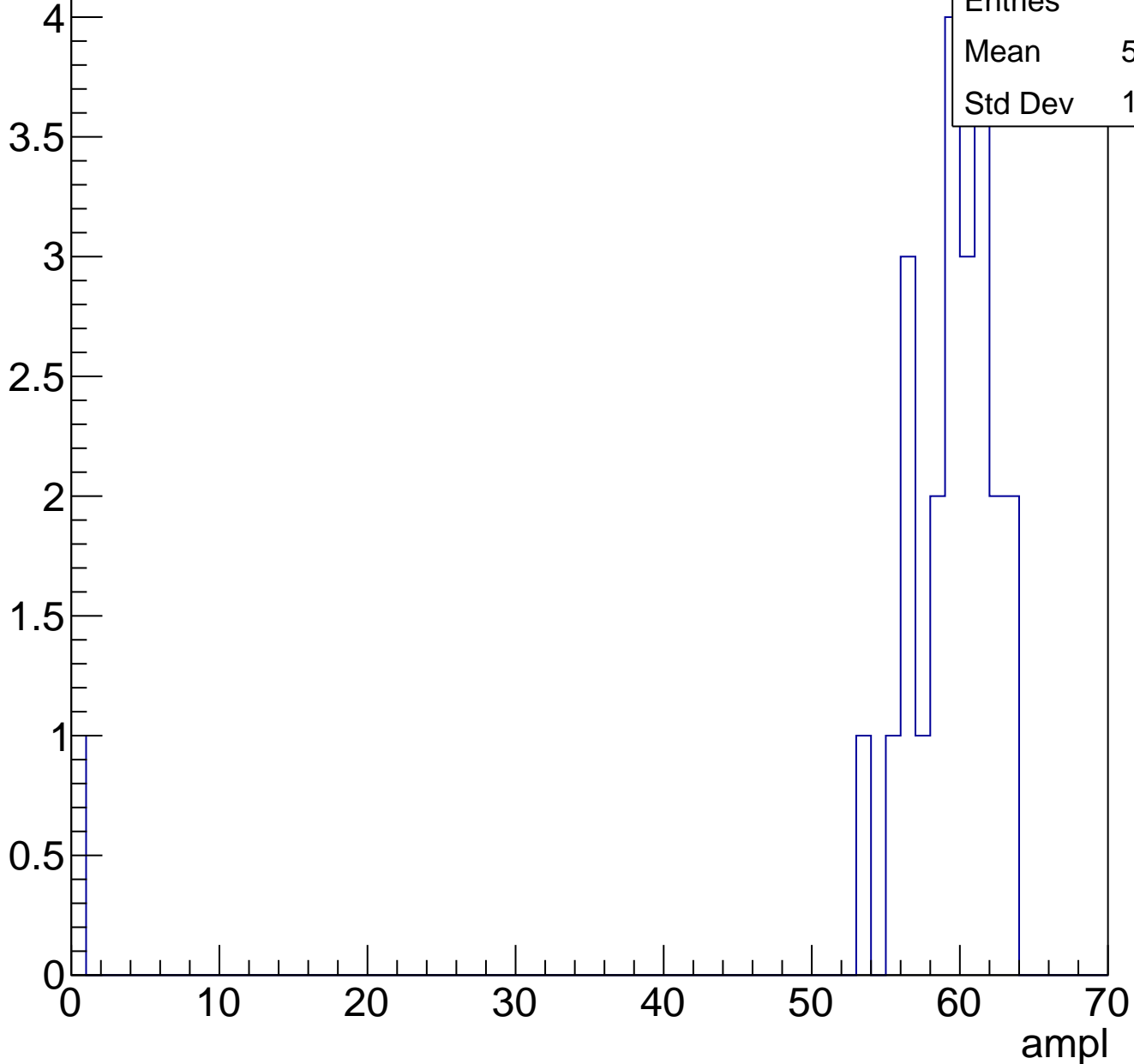


Entries	34
Mean	53.03
Std Dev	9.865

B1L103S, U14-ch20, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch20, adc6

calib_packv5_041523_1651.root, FC#0, port C2

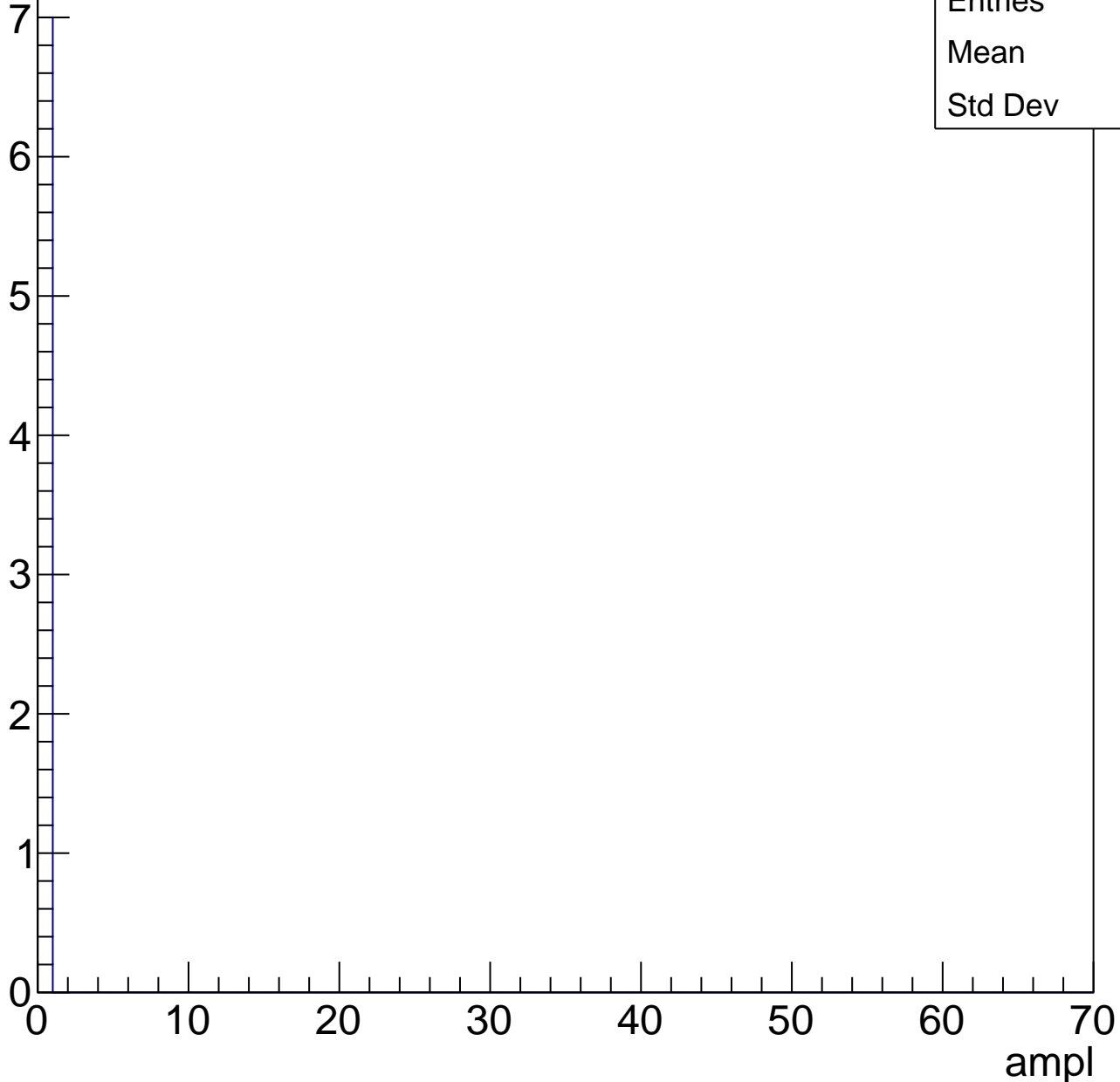
Entry



B1L103S, U14-ch20, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	7
Mean	0
Std Dev	0

B1L103S, U14-ch21, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	46
Mean	22.39
Std Dev	12.86

Entry

10

8

6

4

2

0

0

10

20

30

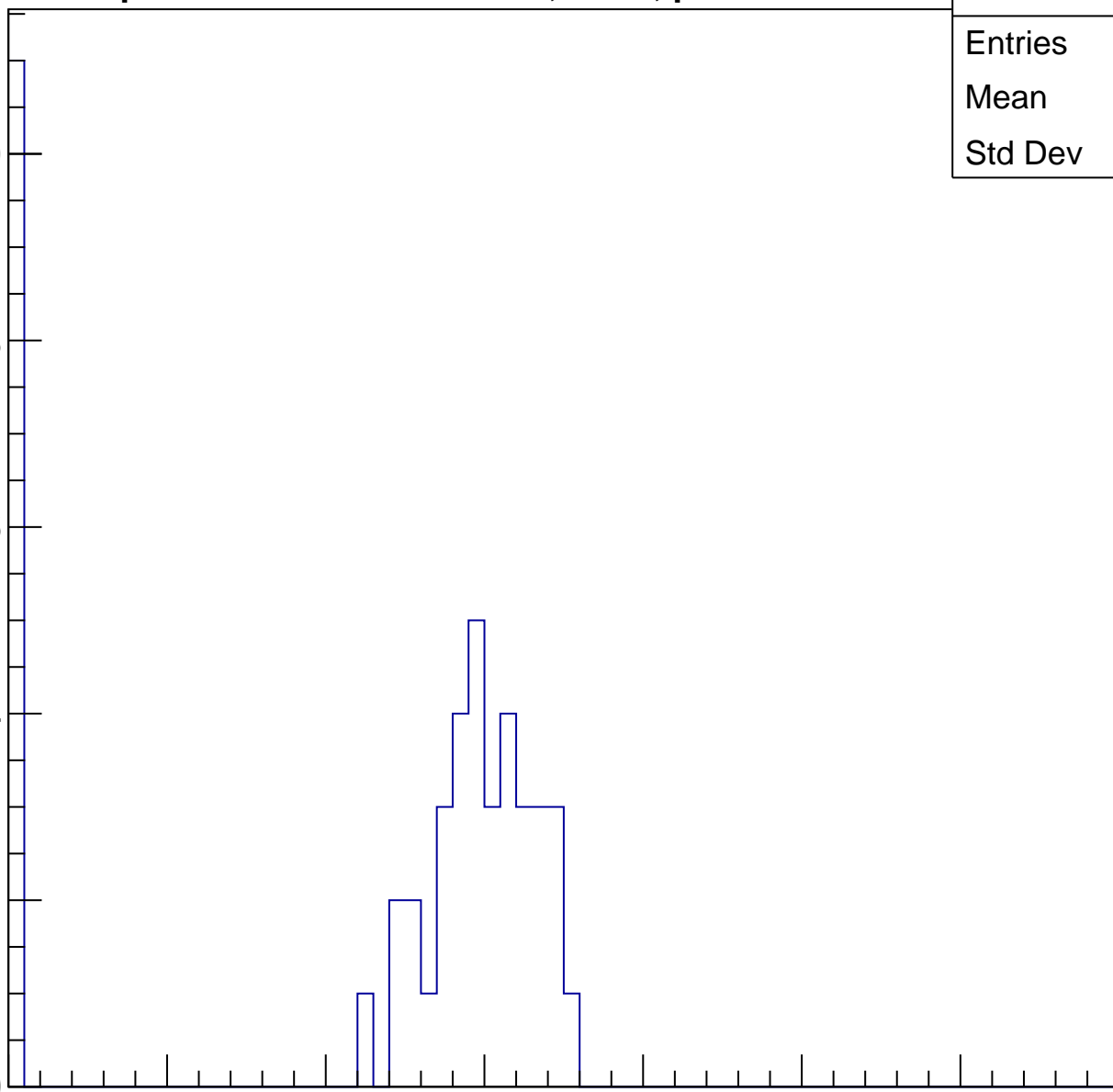
40

50

60

70

ampl

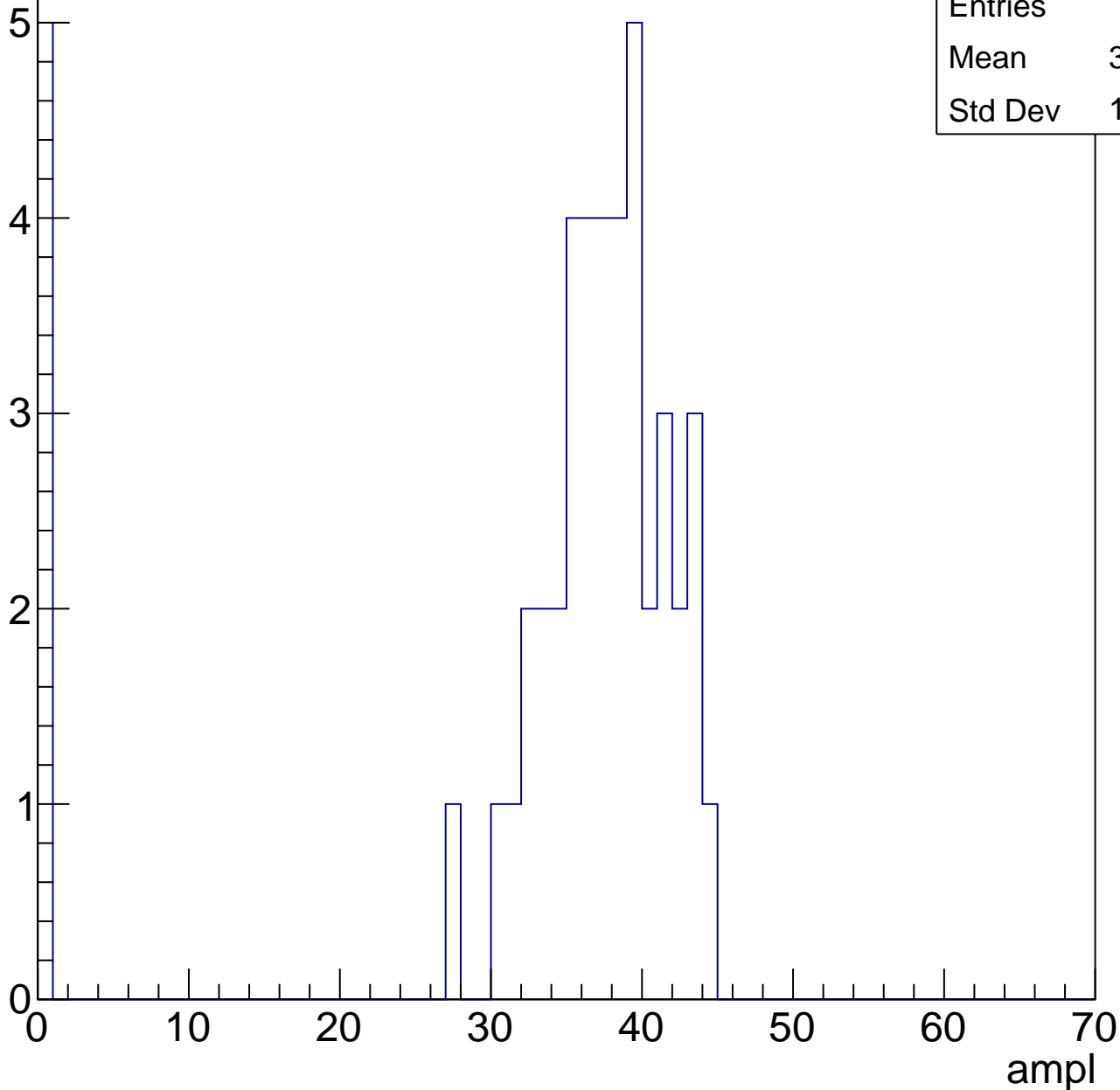


B1L103S, U14-ch21, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	46
Mean	33.15
Std Dev	12.13

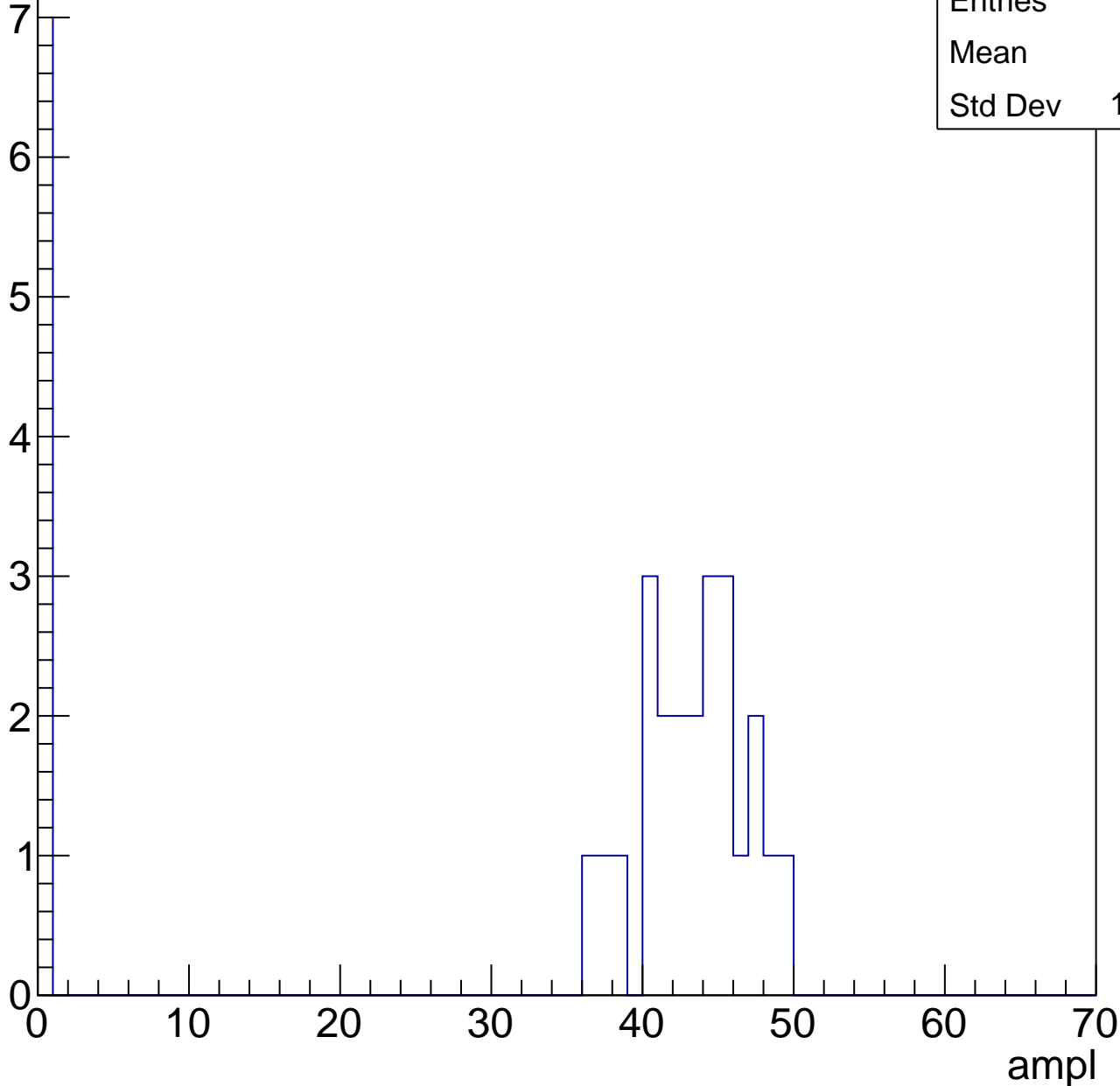


B1L103S, U14-ch21, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

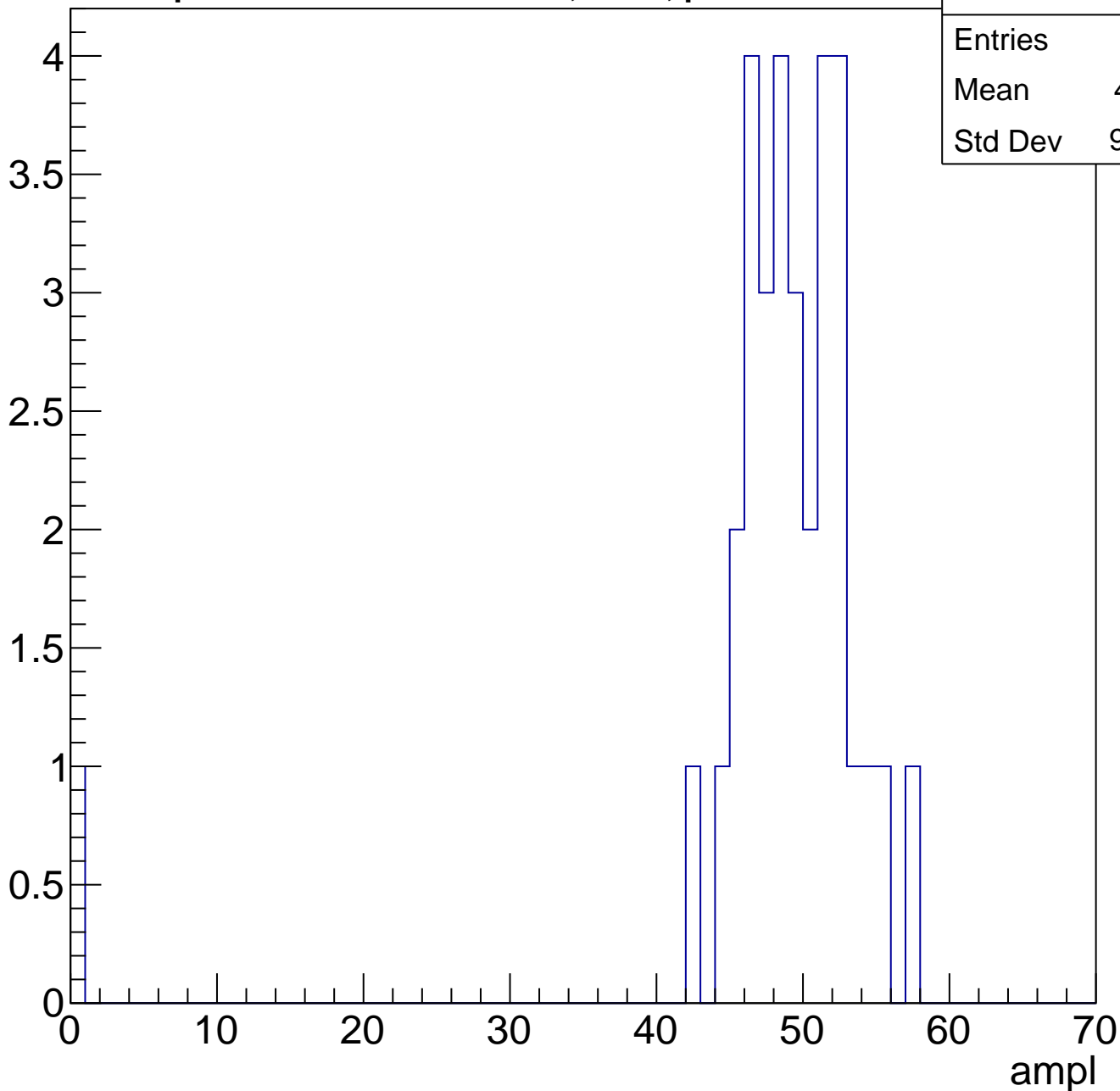
Entries	30
Mean	32.9
Std Dev	18.39



B1L103S, U14-ch21, adc3

calib_packv5_041523_1651.root, FC#0, port C2

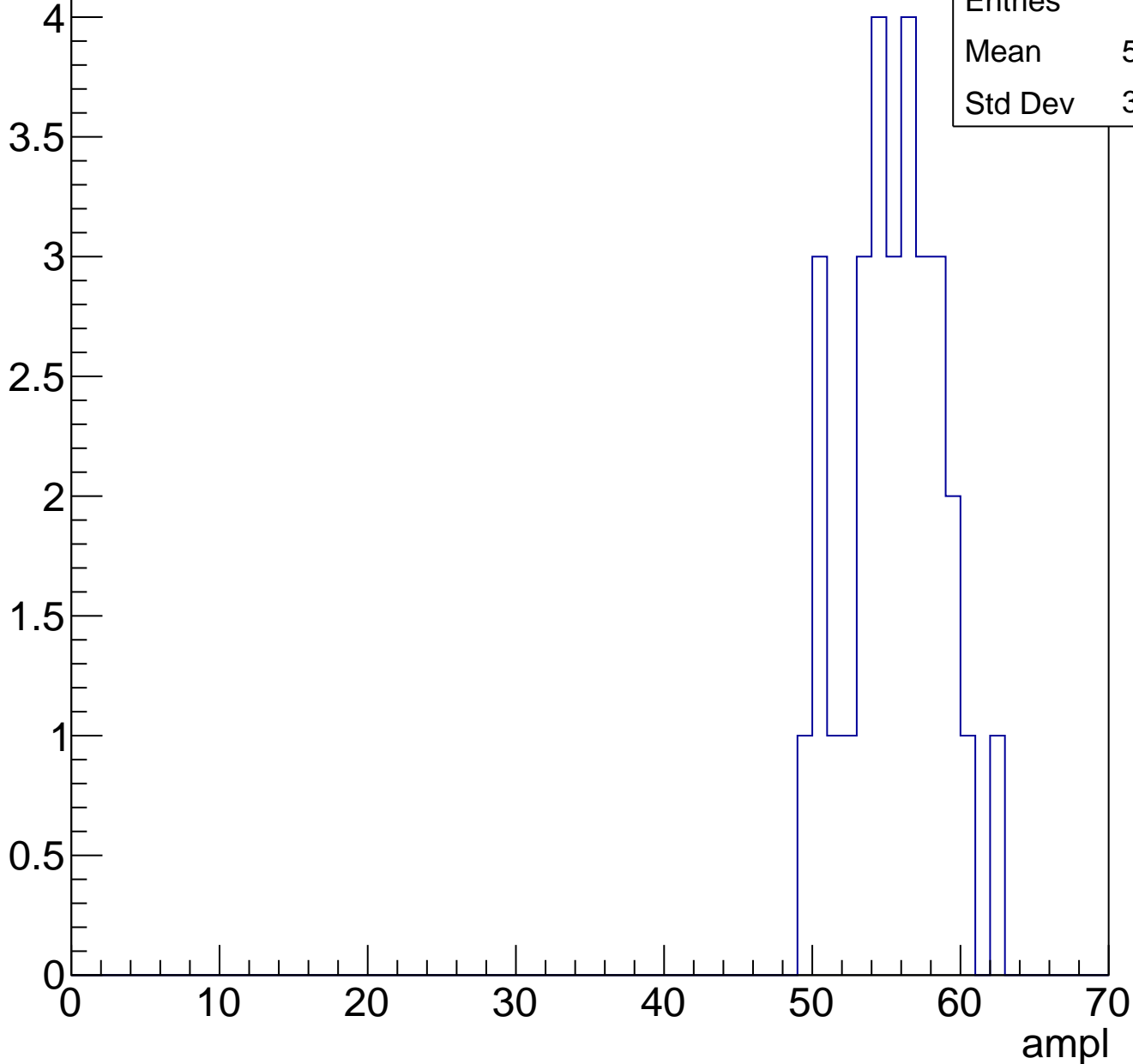
Entry



B1L103S, U14-ch21, adc4

calib_packv5_041523_1651.root, FC#0, port C2

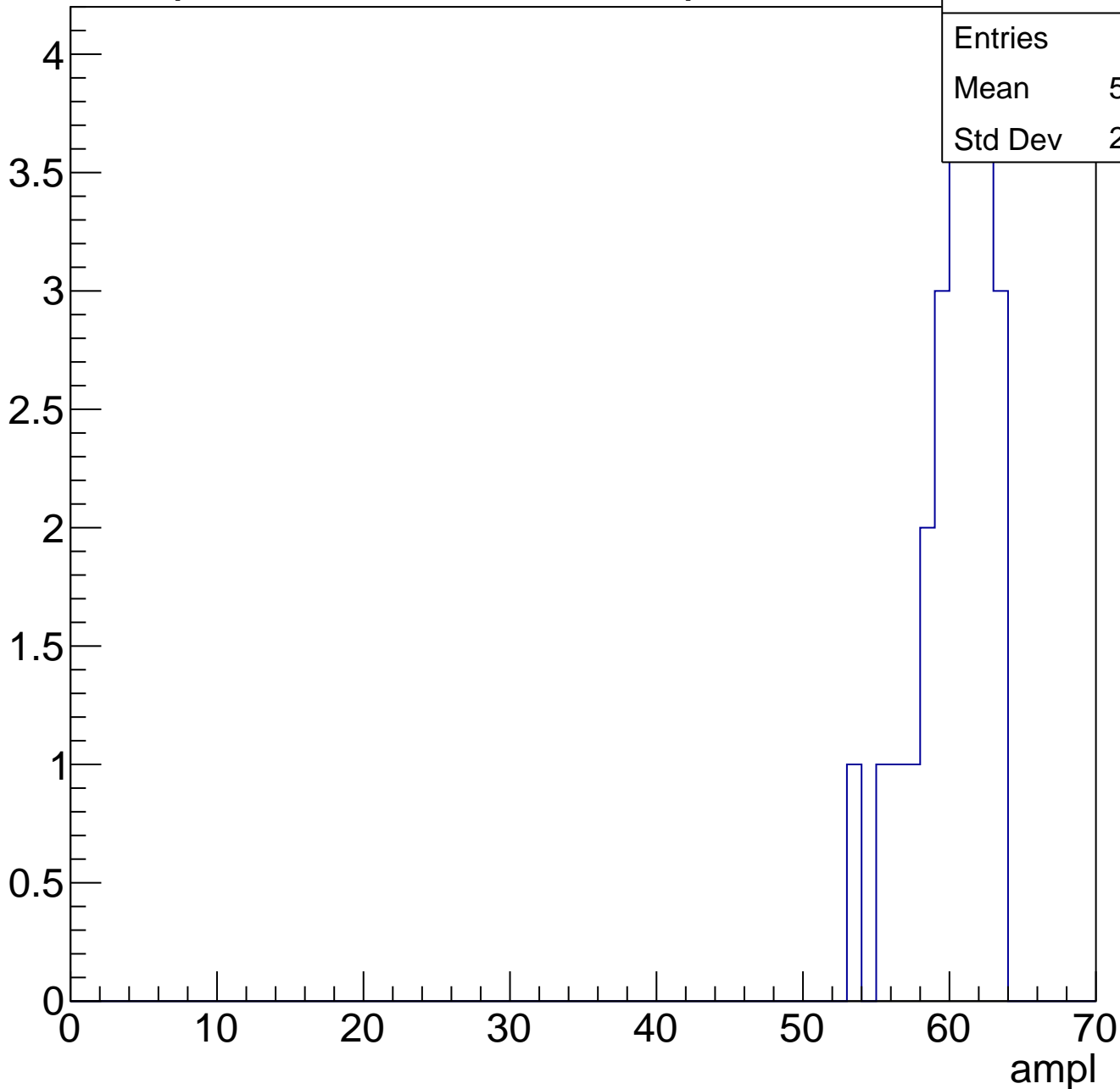
Entry



B1L103S, U14-ch21, adc5

calib_packv5_041523_1651.root, FC#0, port C2

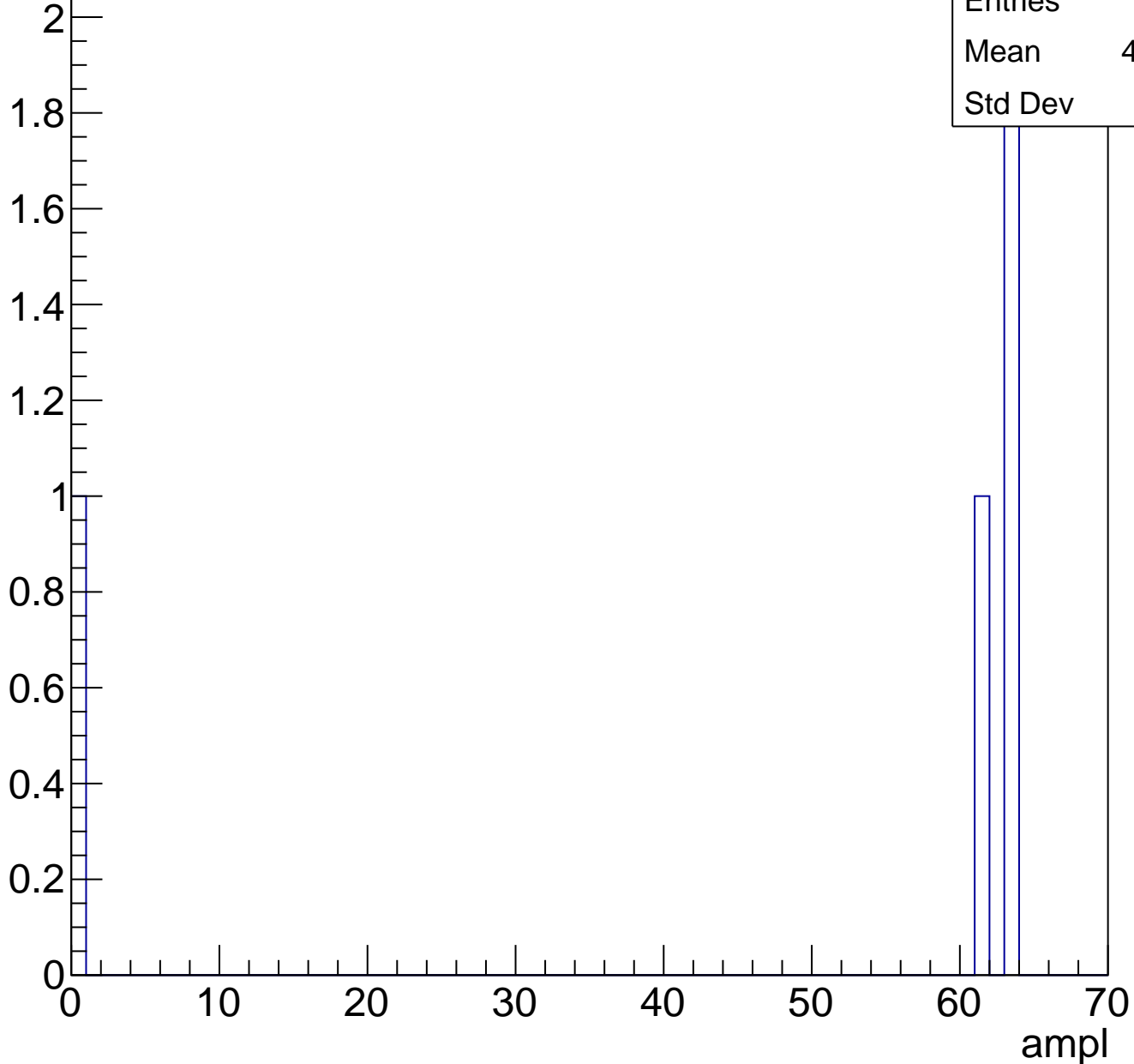
Entry



B1L103S, U14-ch21, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

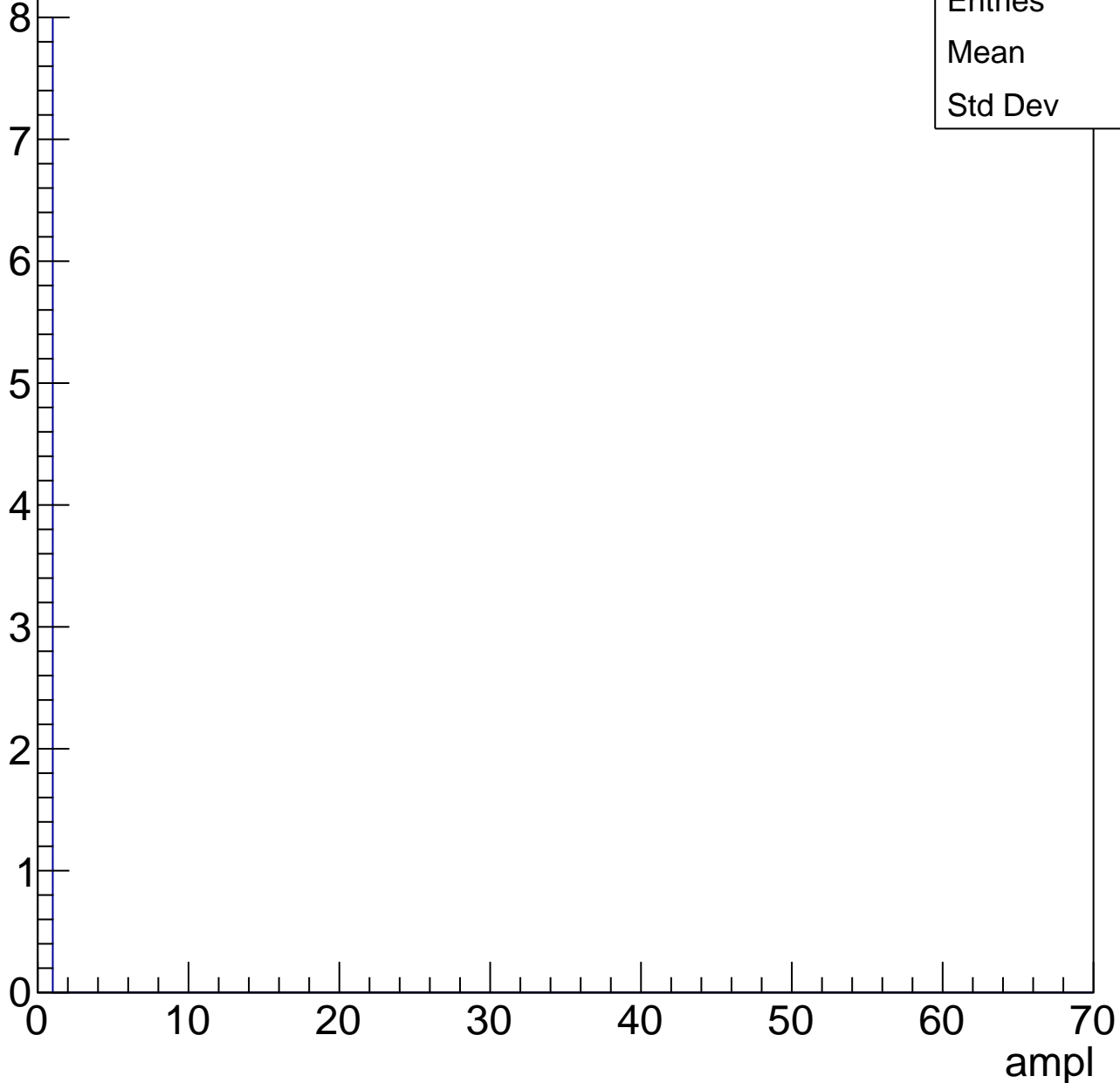


B1L103S, U14-ch21, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	8
Mean	0
Std Dev	0

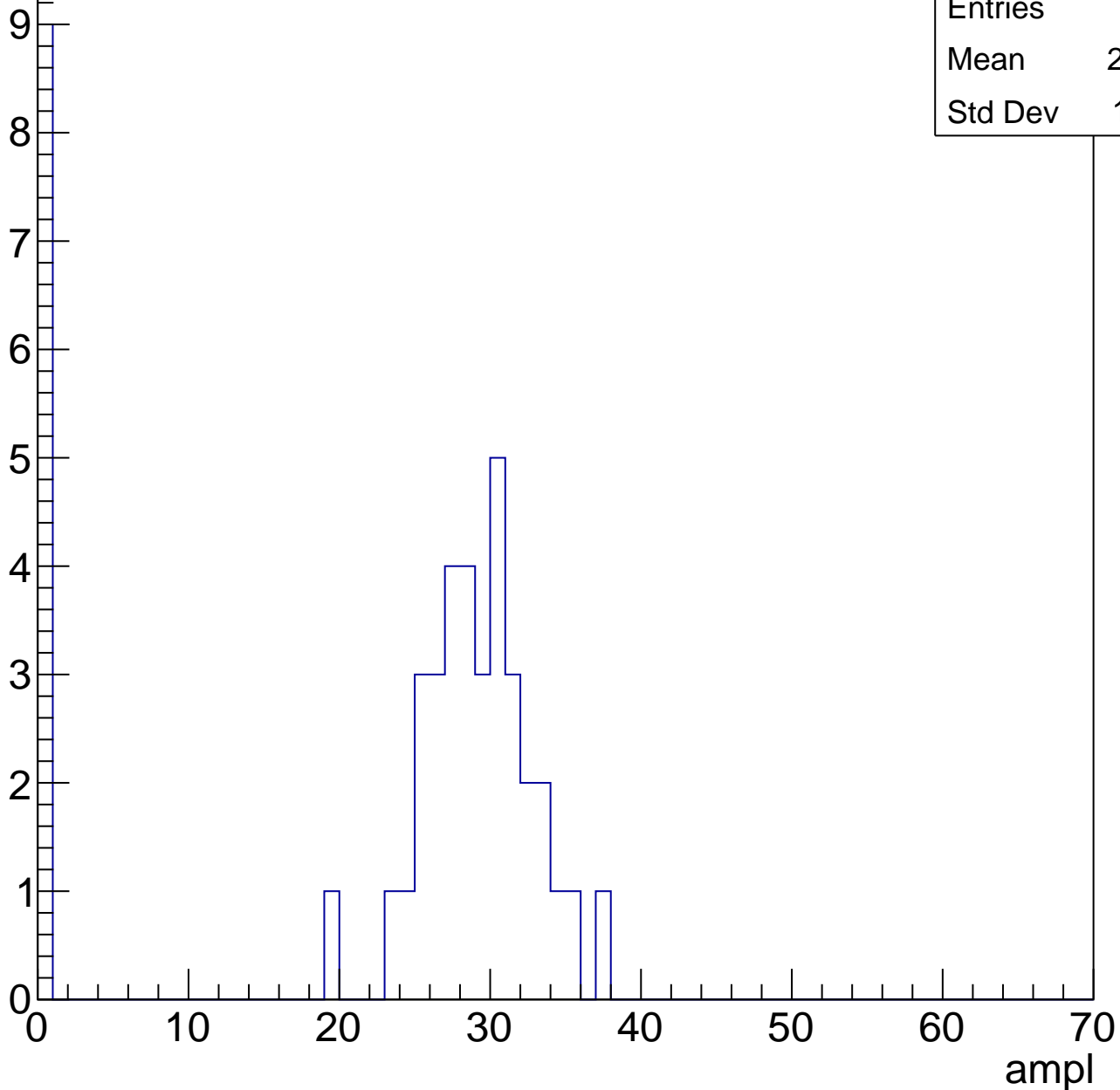


B1L103S, U14-ch22, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	44
Mean	22.84
Std Dev	12.01

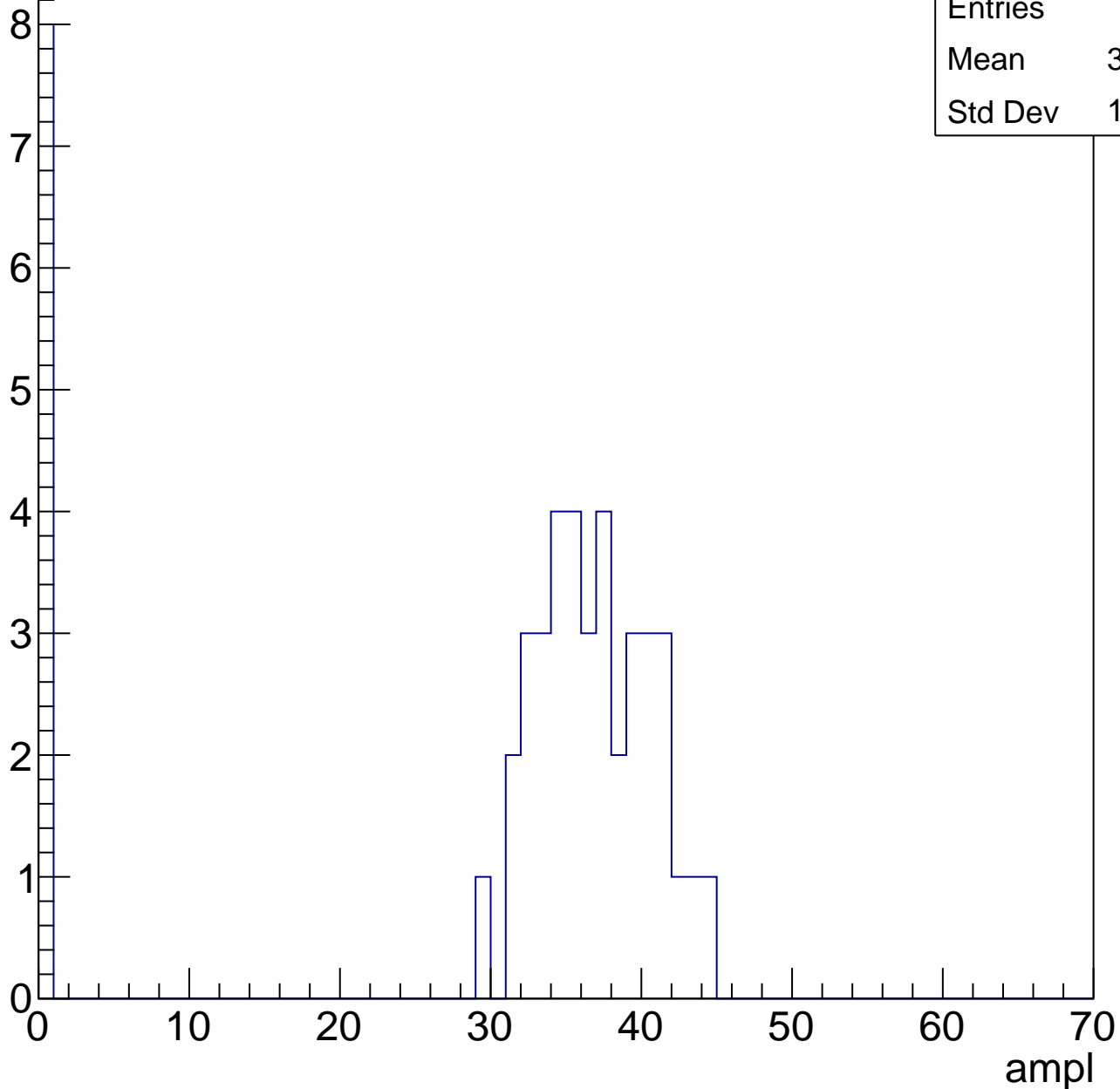


B1L103S, U14-ch22, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

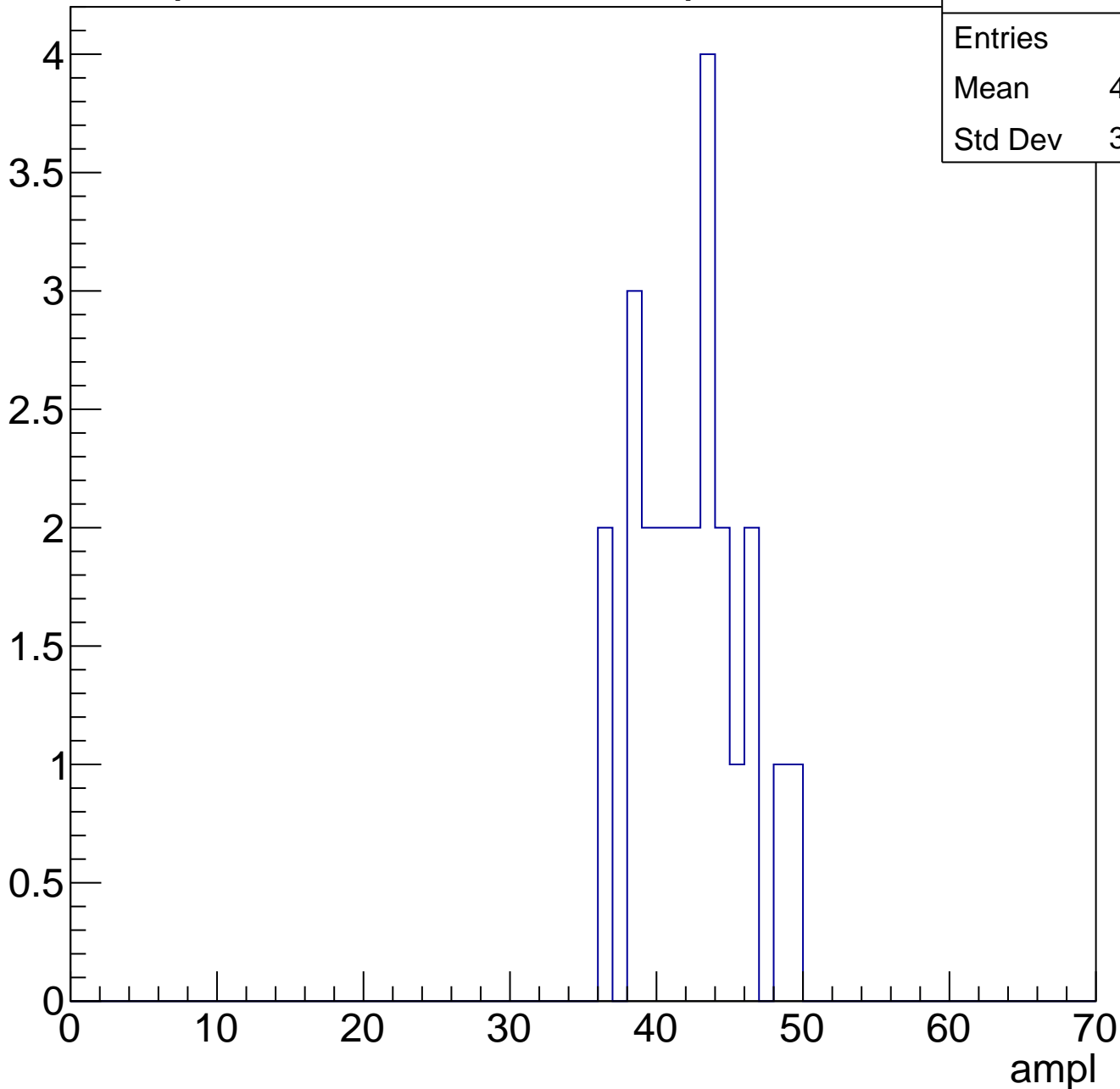
Entries	46
Mean	30.07
Std Dev	14.18



B1L103S, U14-ch22, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

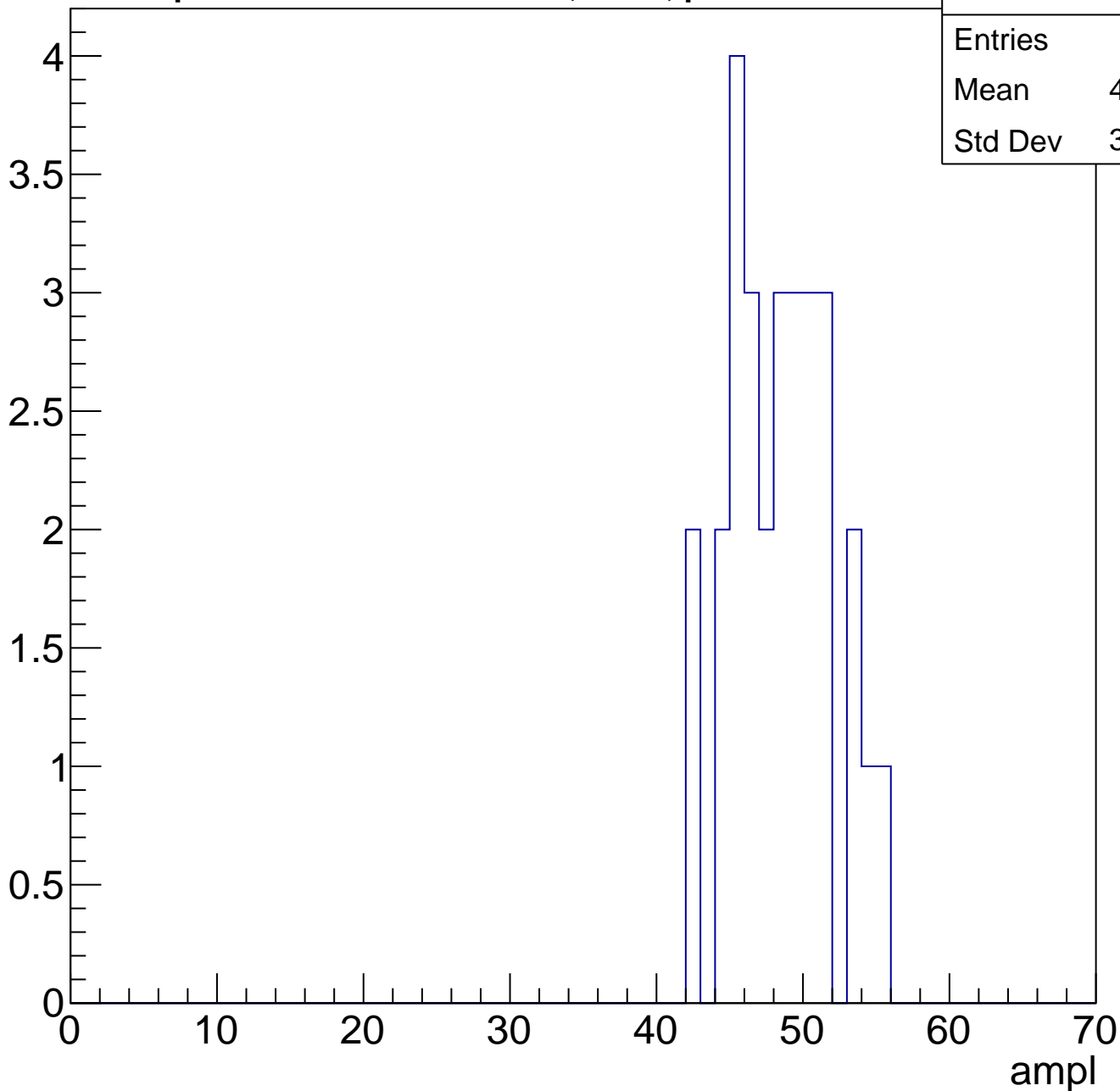


Entries	24
Mean	41.83
Std Dev	3.448

B1L103S, U14-ch22, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry



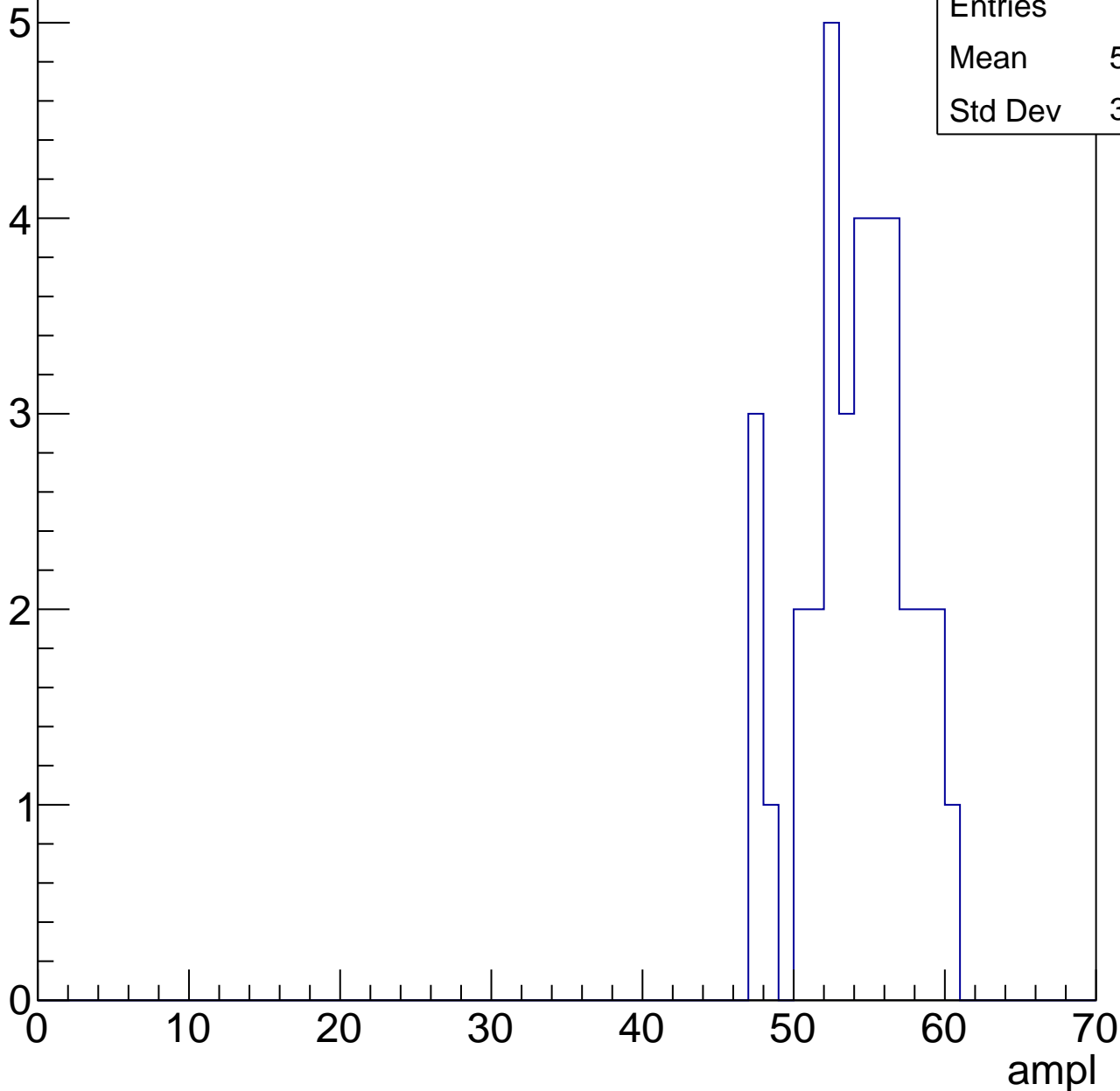
Entries	29
Mean	48.03
Std Dev	3.378

B1L103S, U14-ch22, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

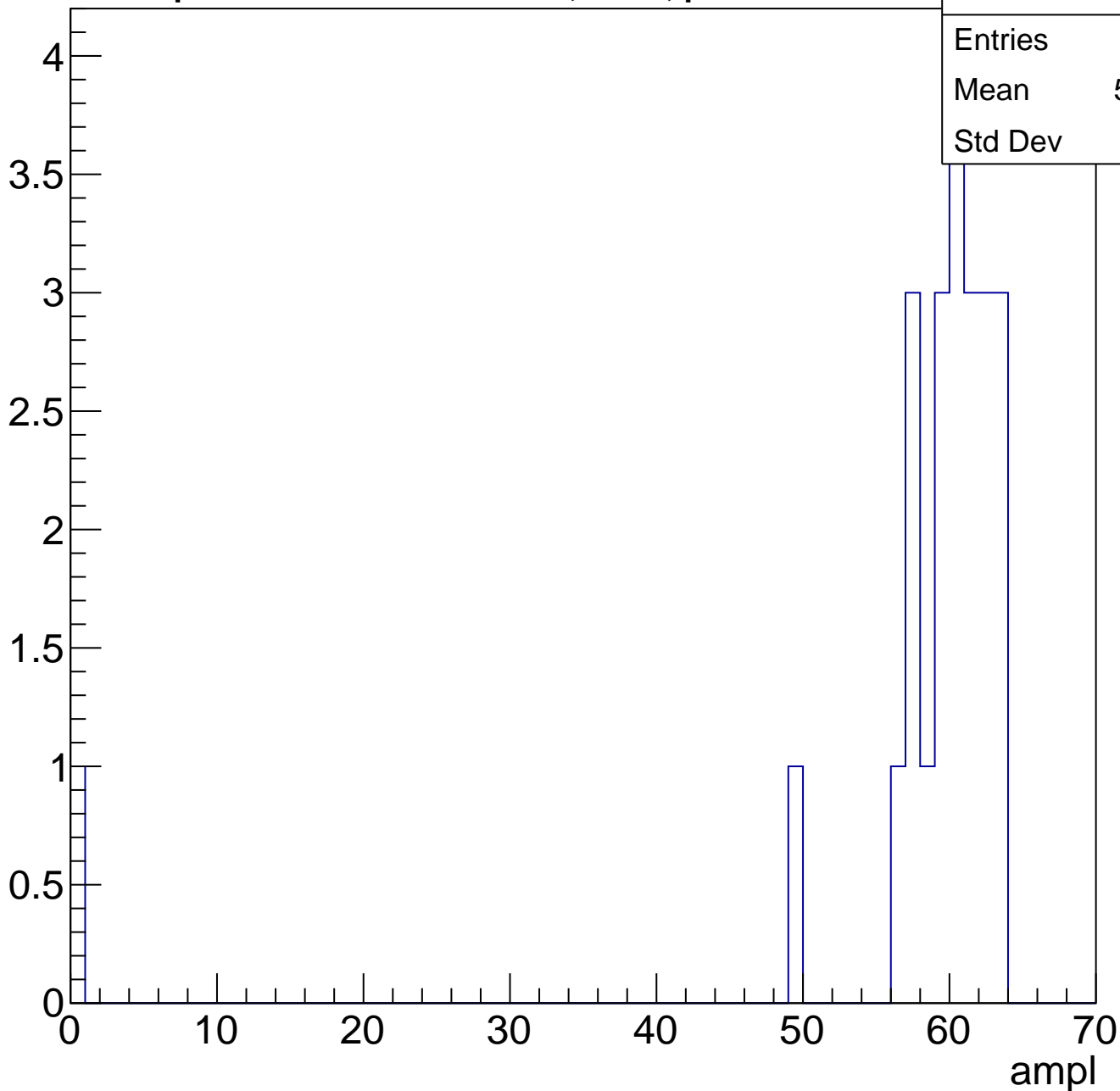
Entries	35
Mean	53.66
Std Dev	3.414



B1L103S, U14-ch22, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch22, adc6

calib_packv5_041523_1651.root, FC#0, port C2

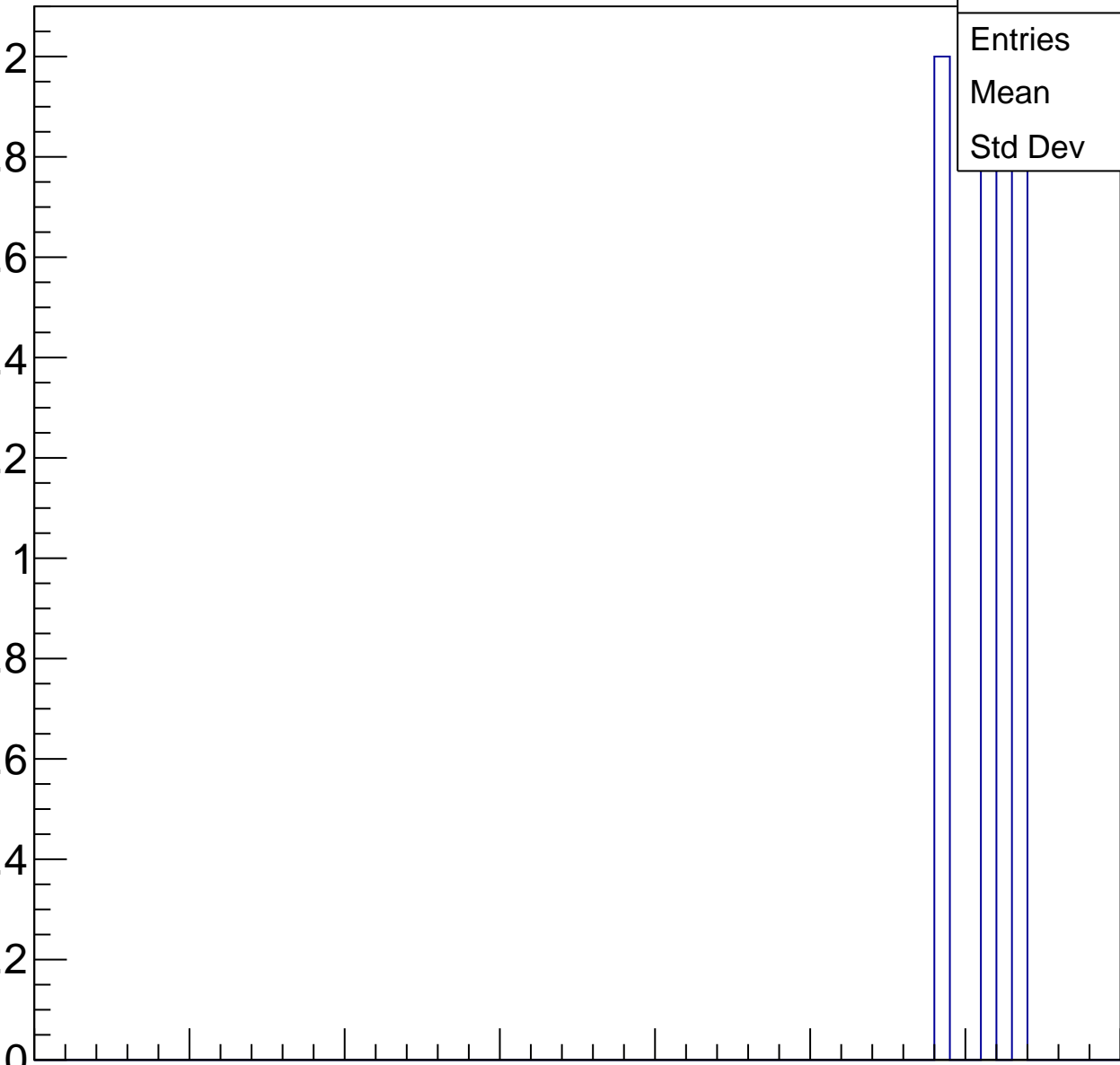
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	6
Mean	60.67
Std Dev	2.055

0 10 20 30 40 50 60 70

ampl

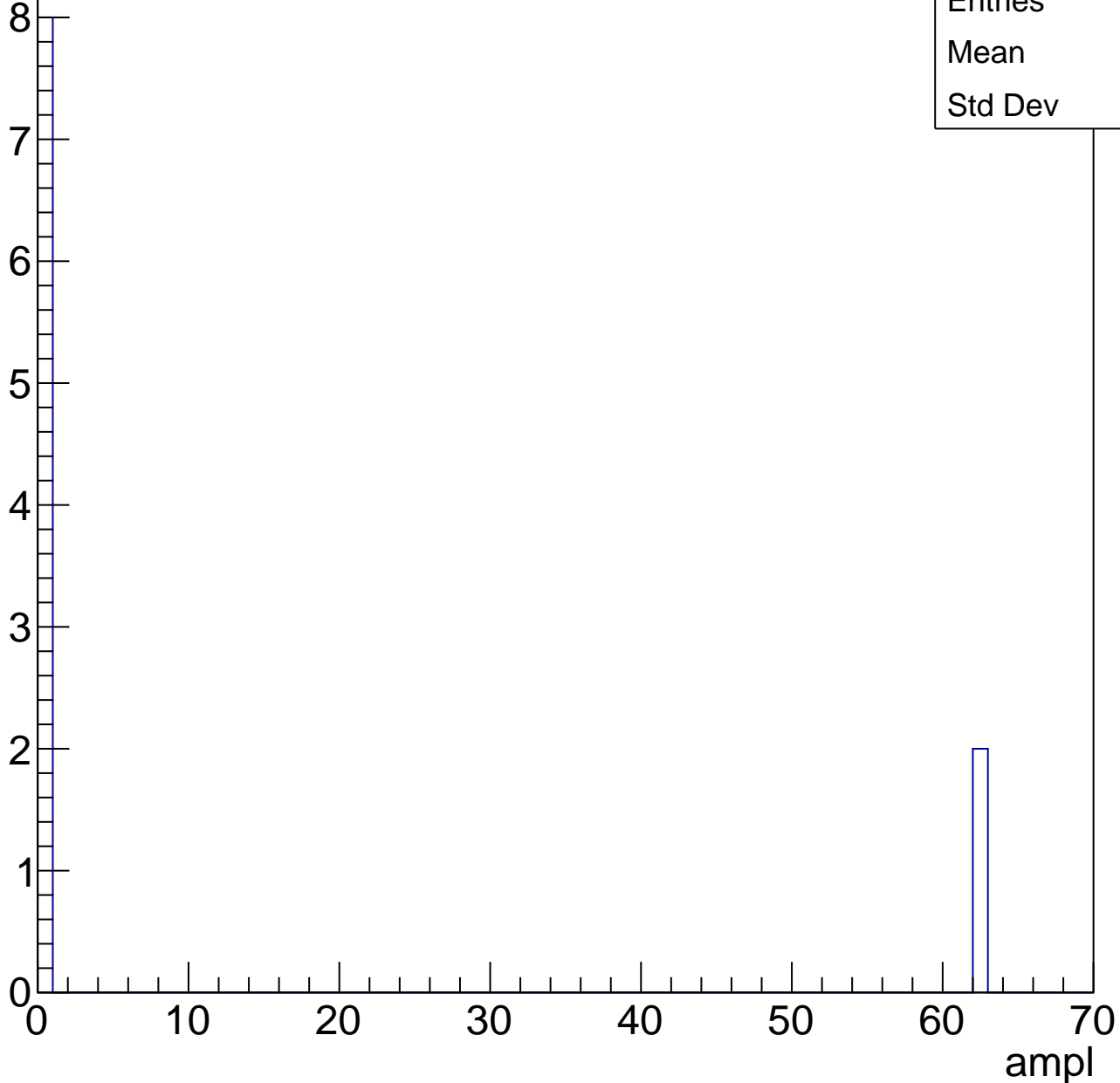


B1L103S, U14-ch22, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	10
Mean	12.4
Std Dev	24.8

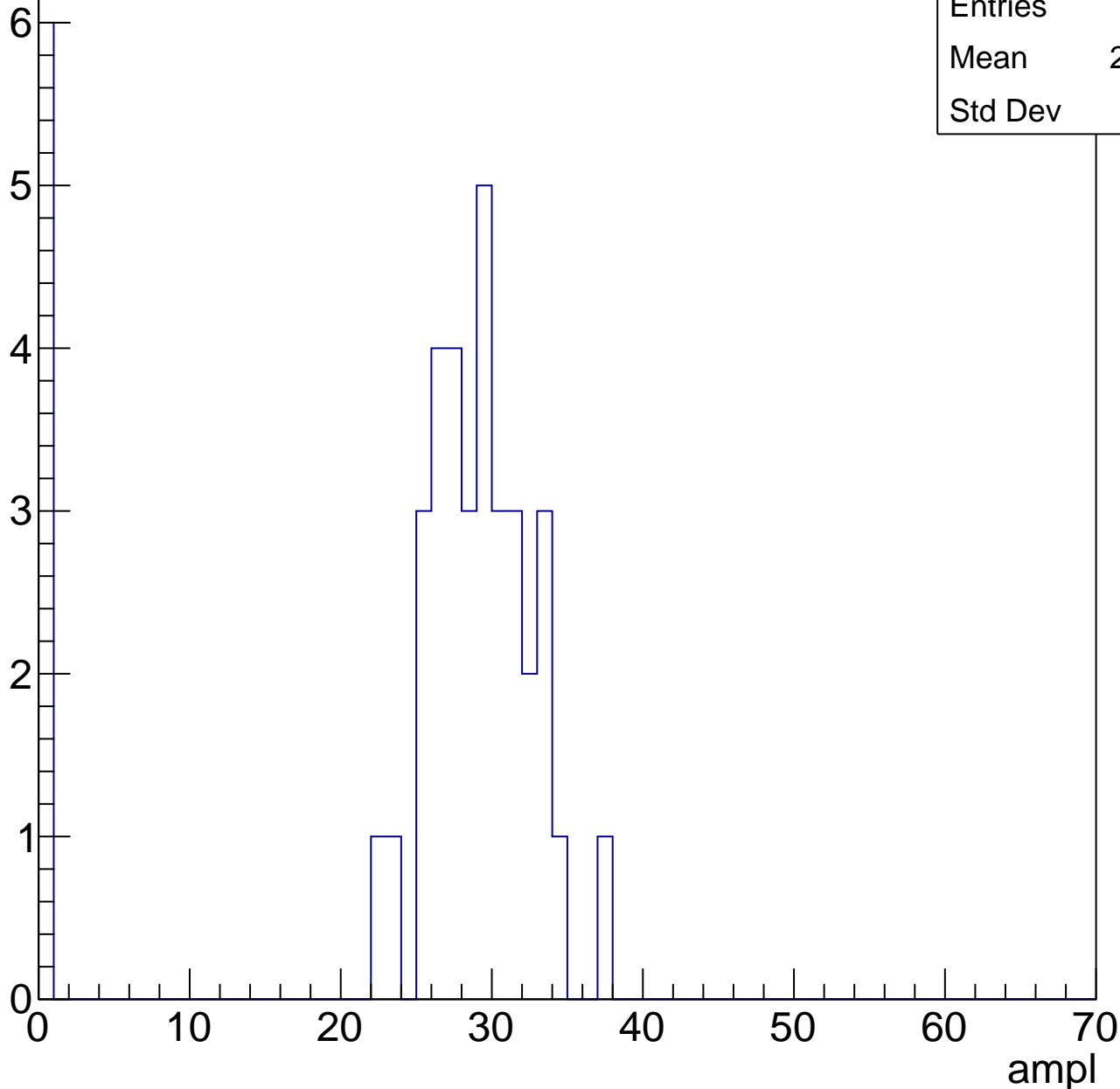


B1L103S, U14-ch23, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

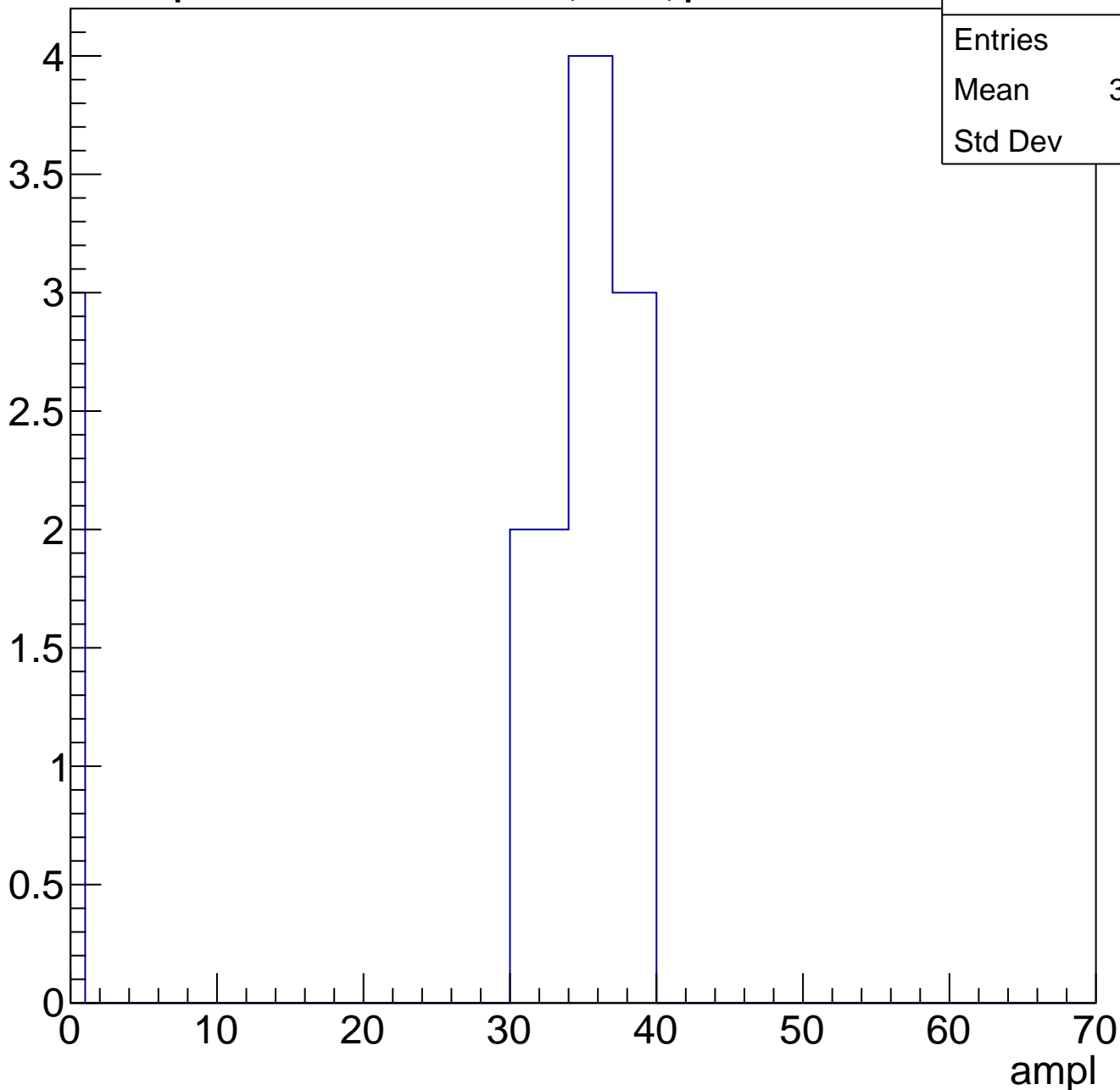
Entries	40
Mean	24.45
Std Dev	10.7



B1L103S, U14-ch23, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry



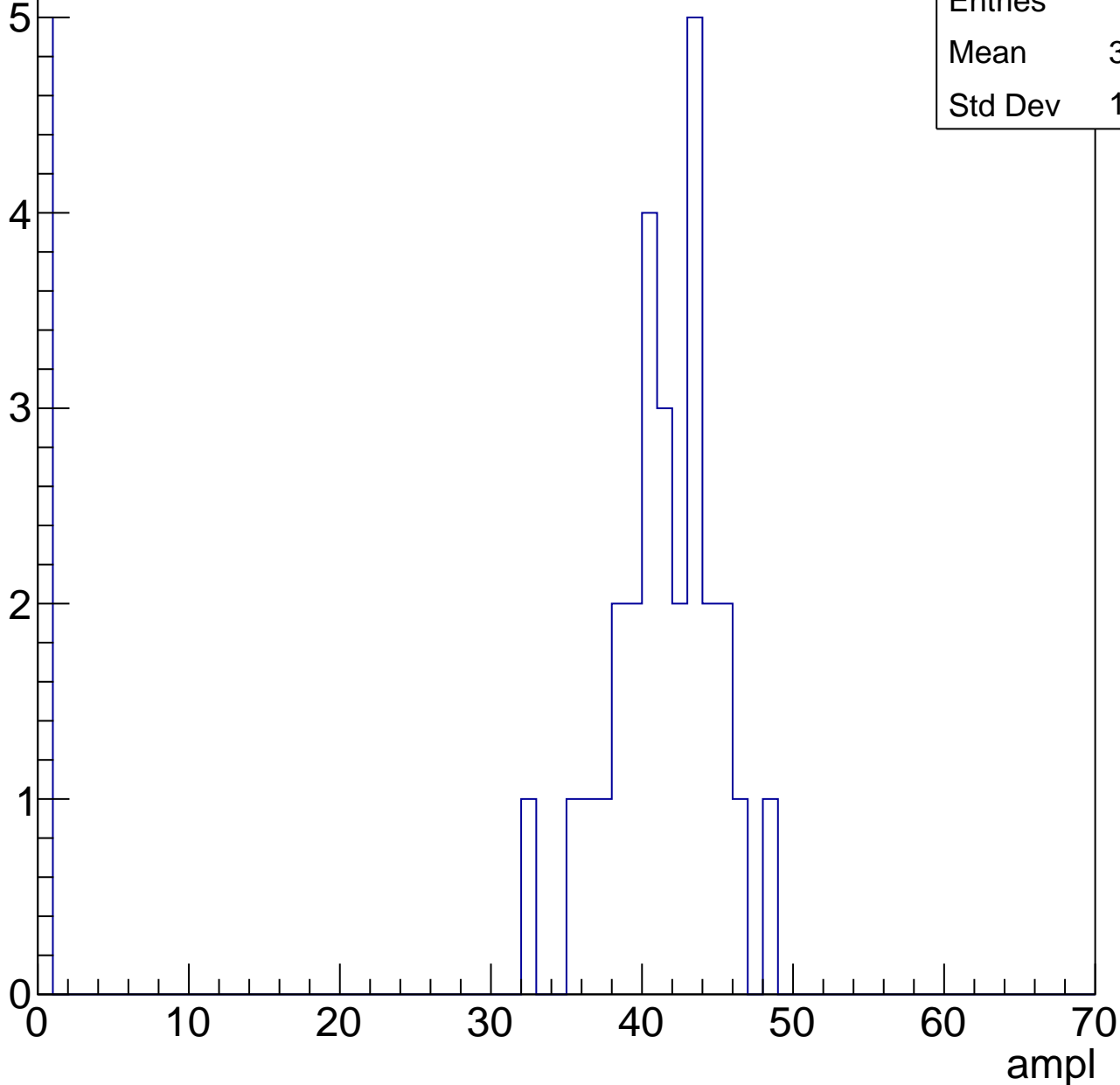
Entries	32
Mean	31.69
Std Dev	10.5

B1L103S, U14-ch23, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	33
Mean	34.79
Std Dev	15.04

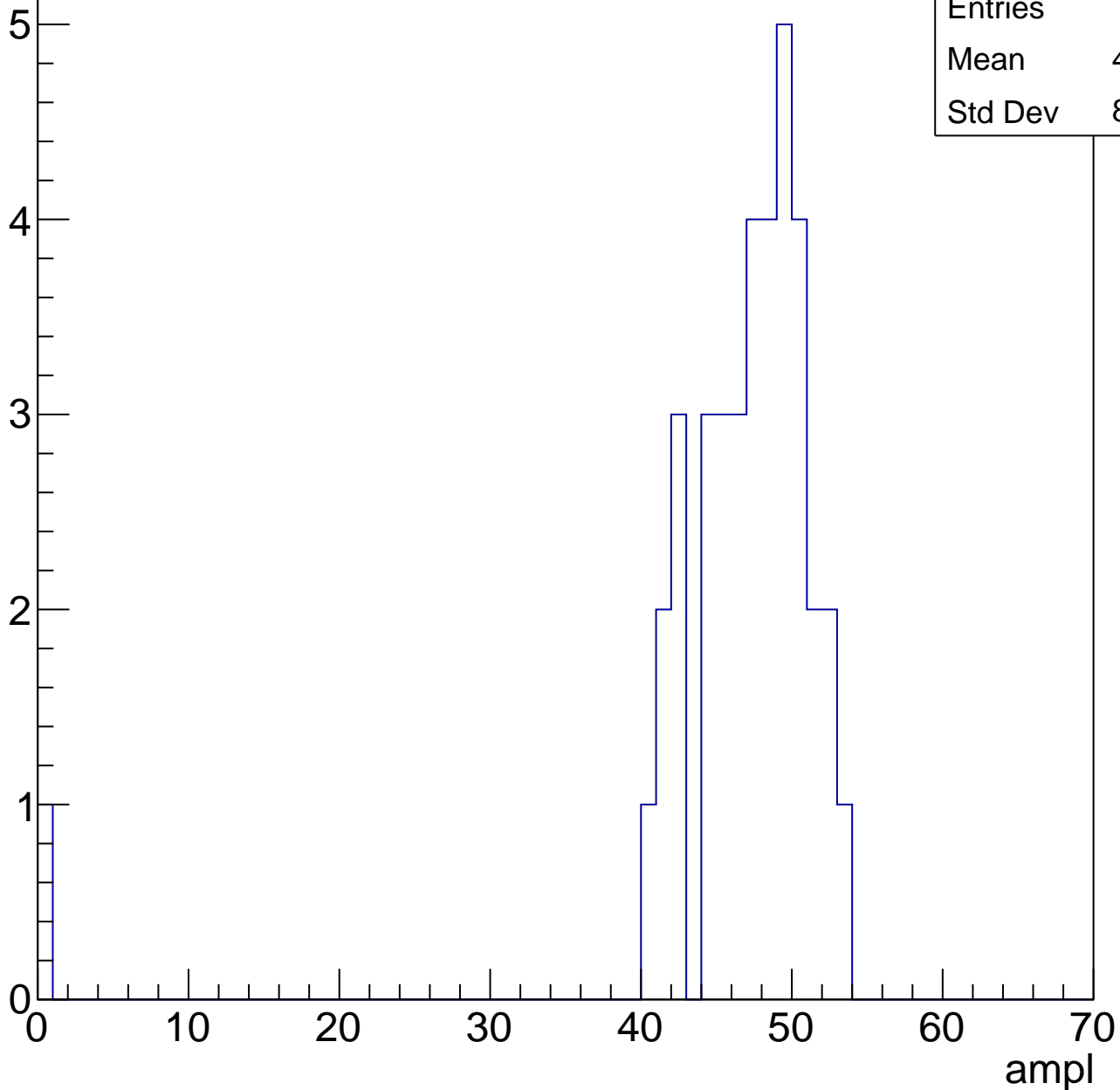


B1L103S, U14-ch23, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

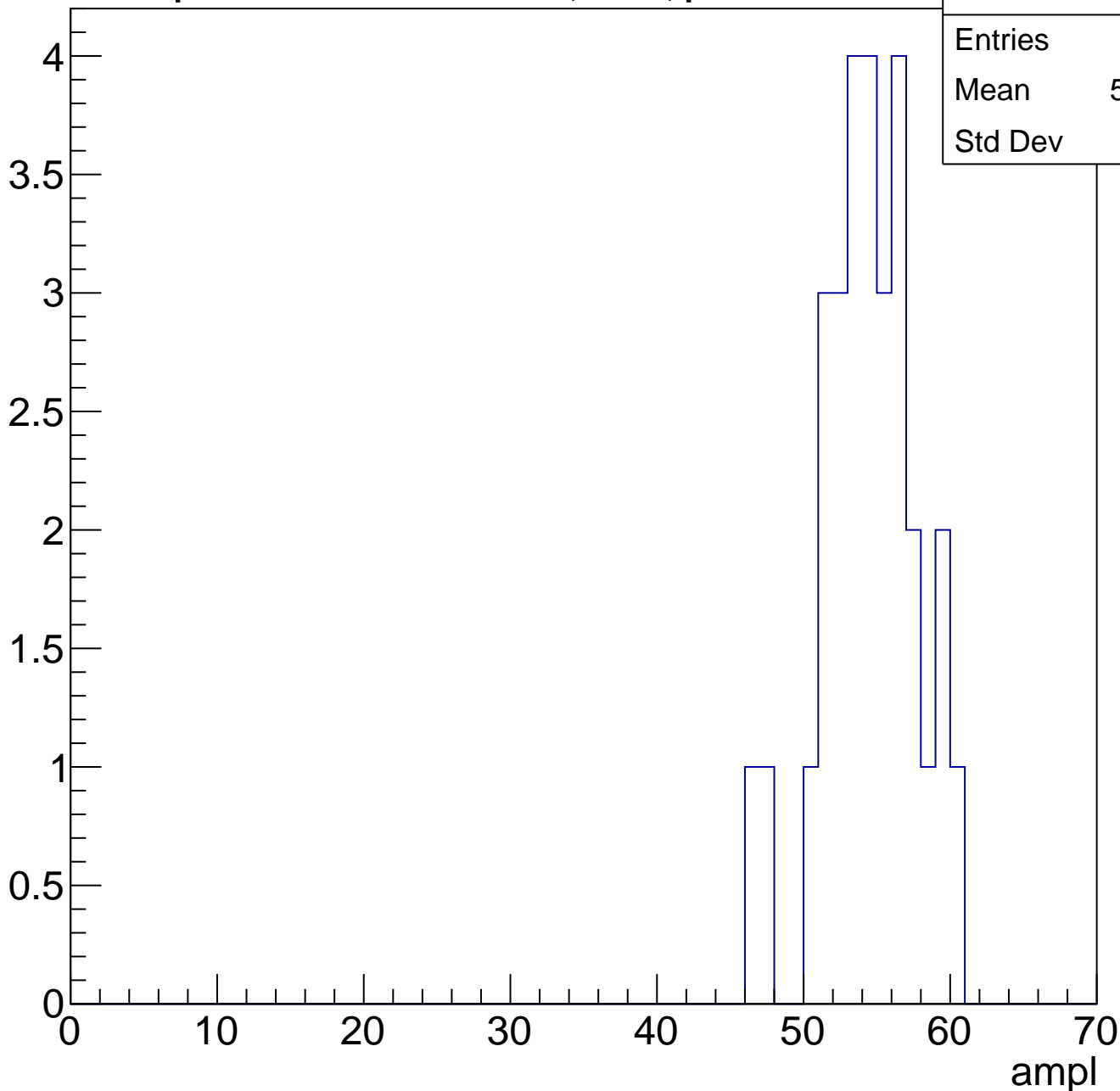
Entries	38
Mean	45.71
Std Dev	8.211



B1L103S, U14-ch23, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	30
Mean	53.97
Std Dev	3.22

B1L103S, U14-ch23, adc5

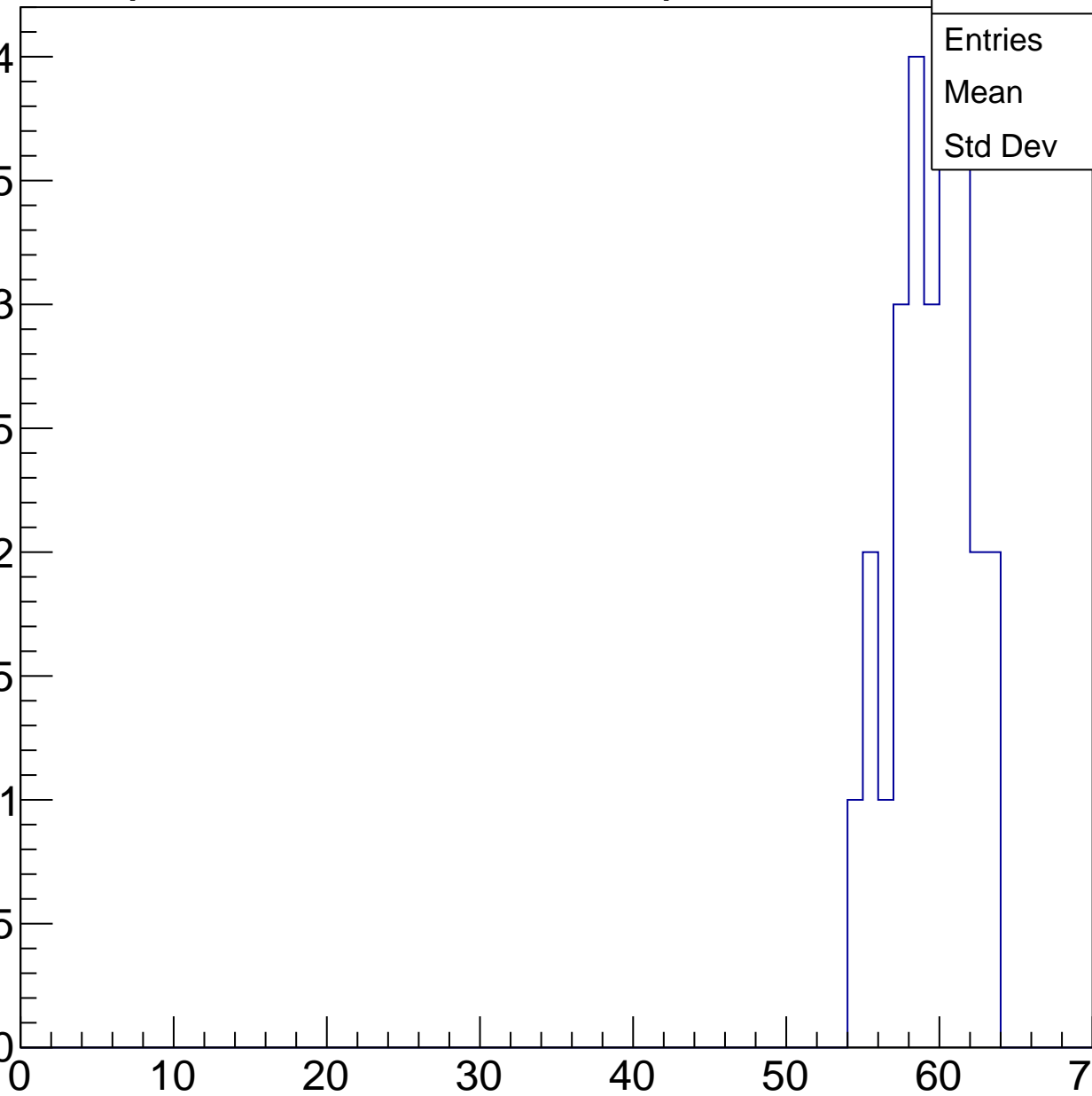
calib_packv5_041523_1651.root, FC#0, port C2

Entry

4
3.5
3
2.5
2
1.5
1
0.5
0

Entries	26
Mean	59
Std Dev	2.418

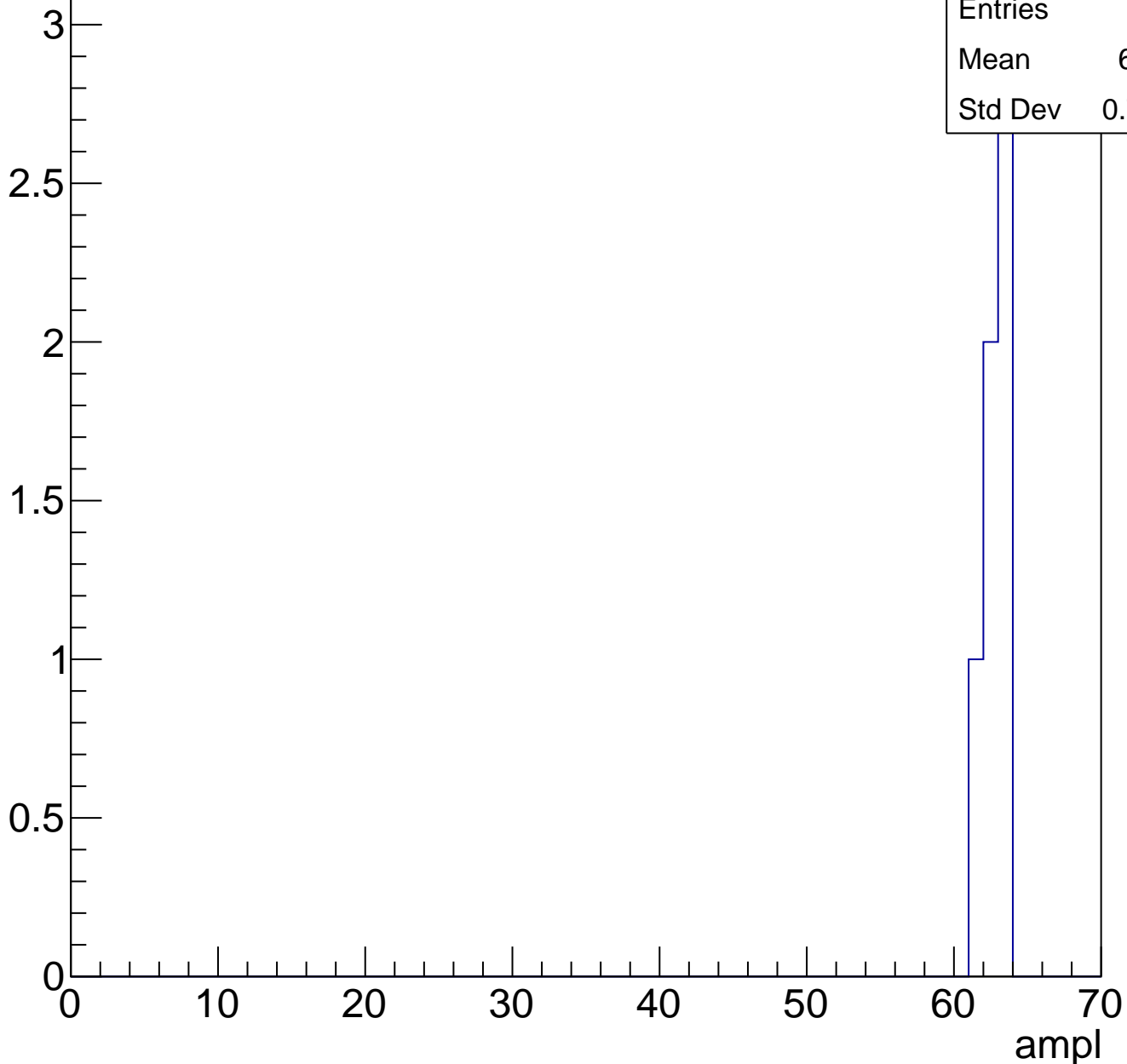
ampl



B1L103S, U14-ch23, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

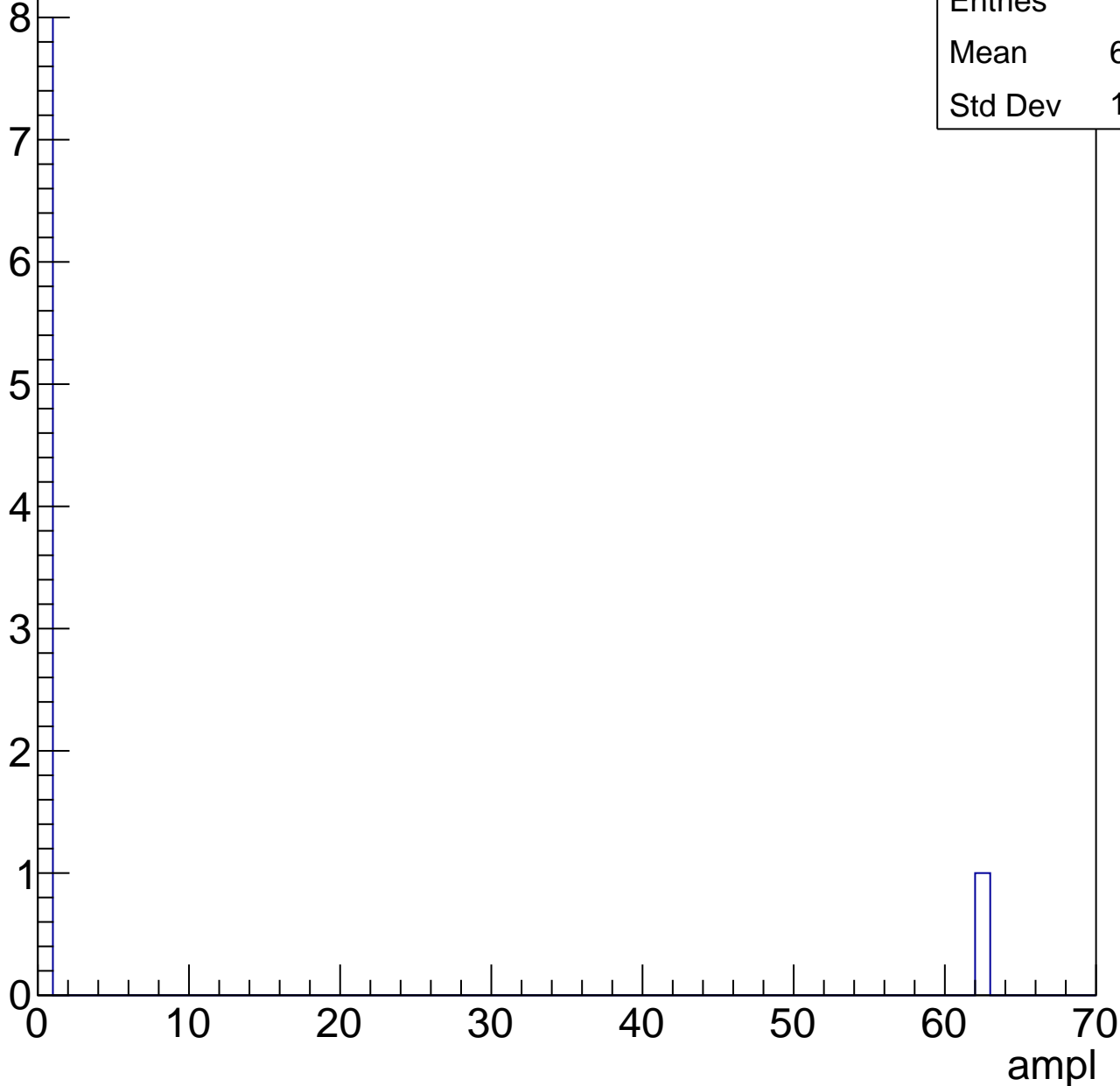


B1L103S, U14-ch23, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	9
Mean	6.889
Std Dev	19.48

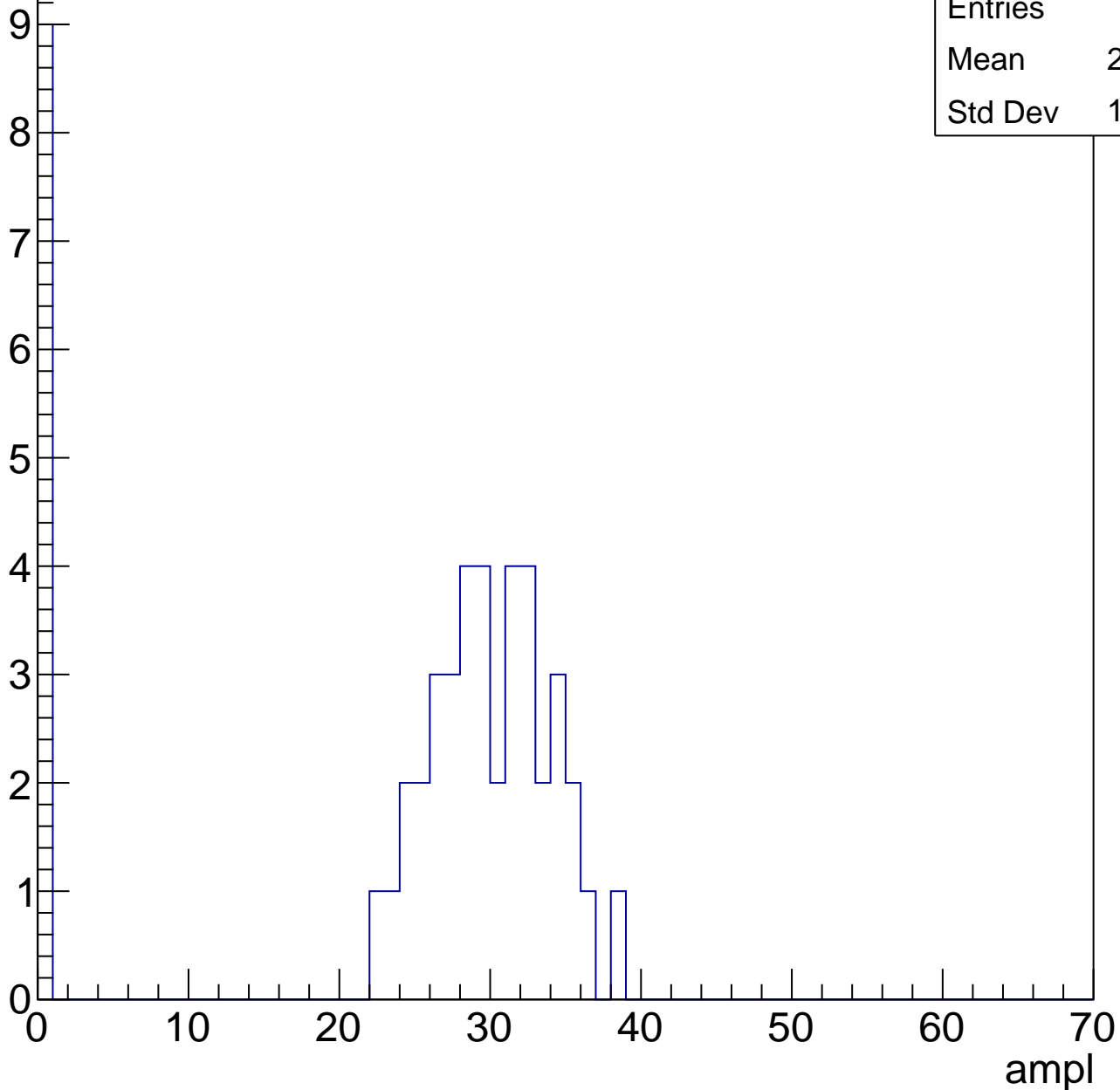


B1L103S, U14-ch24, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

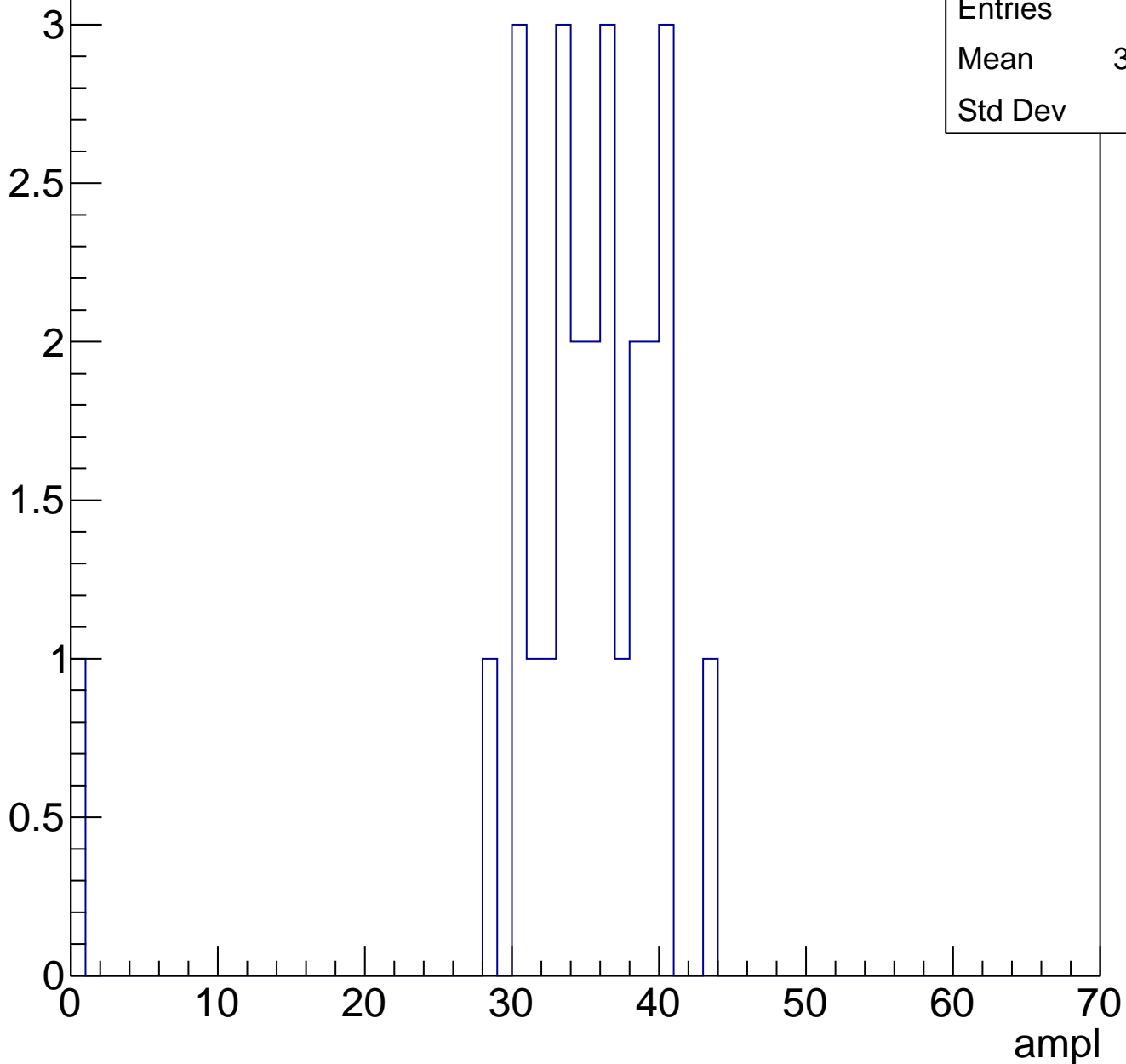
Entries	48
Mean	24.04
Std Dev	12.04



B1L103S, U14-ch24, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

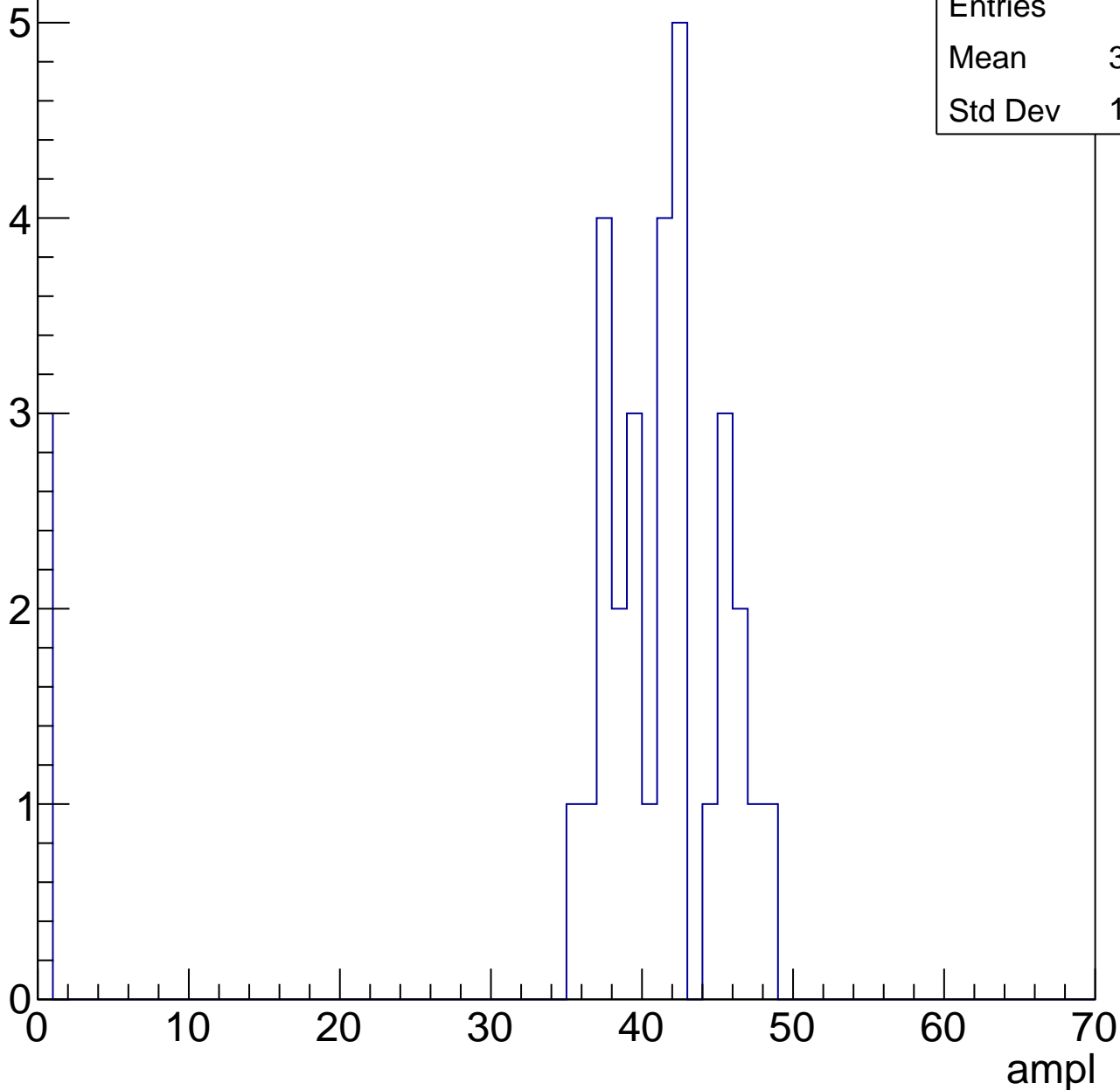


B1L103S, U14-ch24, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	32
Mean	37.25
Std Dev	12.43

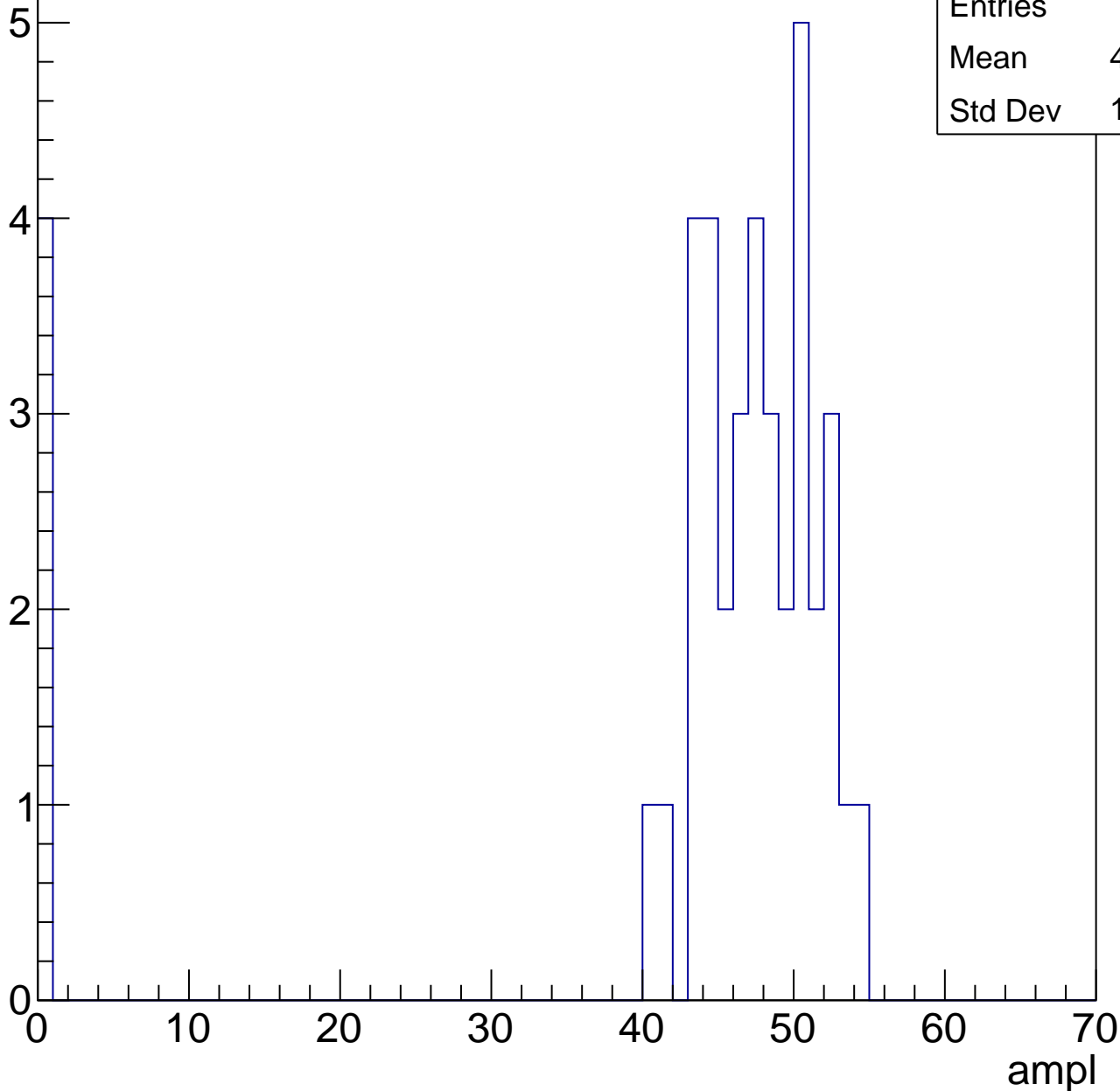


B1L103S, U14-ch24, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

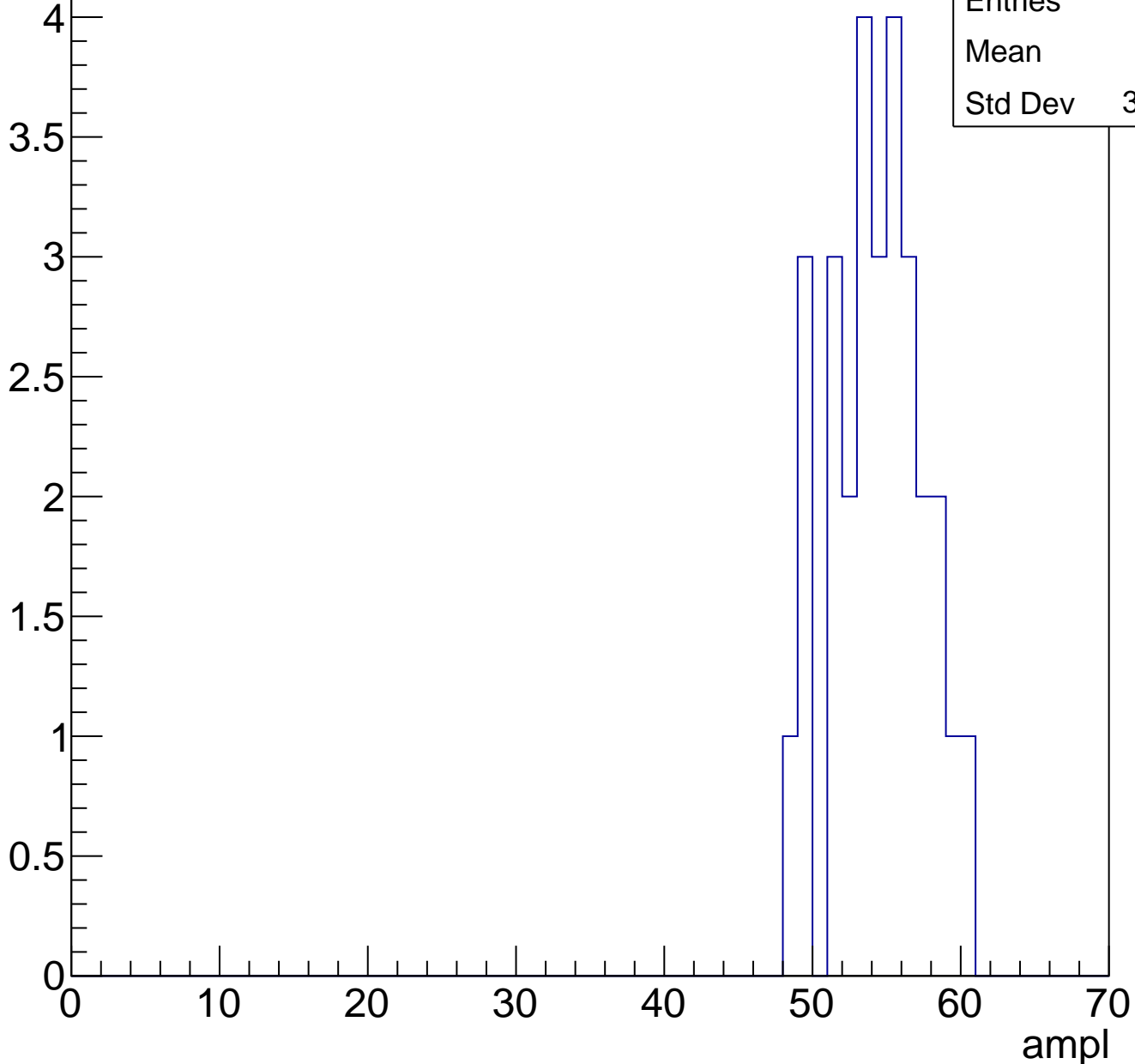
Entries	40
Mean	42.55
Std Dev	14.57



B1L103S, U14-ch24, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



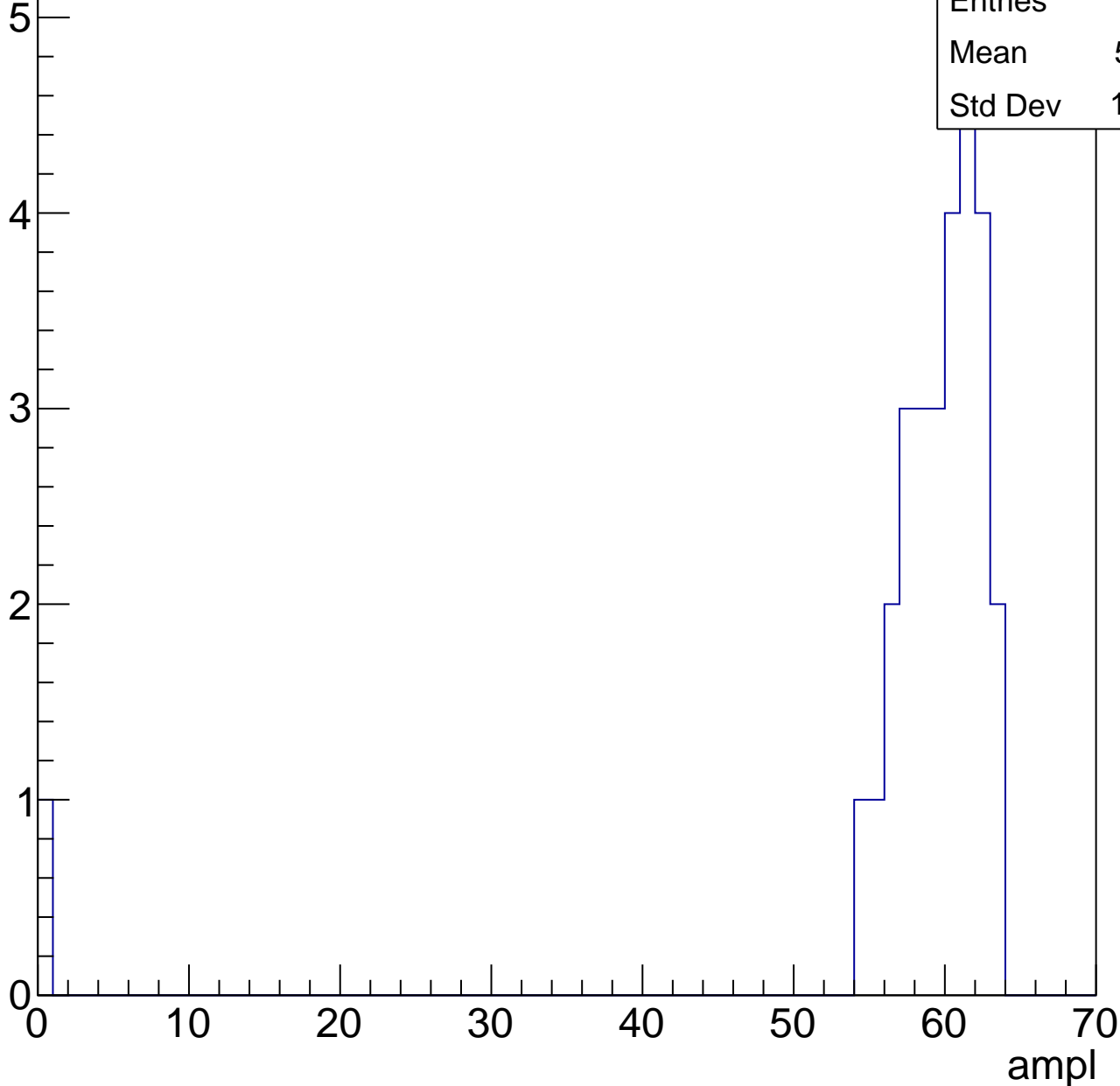
Entries	29
Mean	53.9
Std Dev	3.089

B1L103S, U14-ch24, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	29
Mean	57.31
Std Dev	11.09



B1L103S, U14-ch24, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

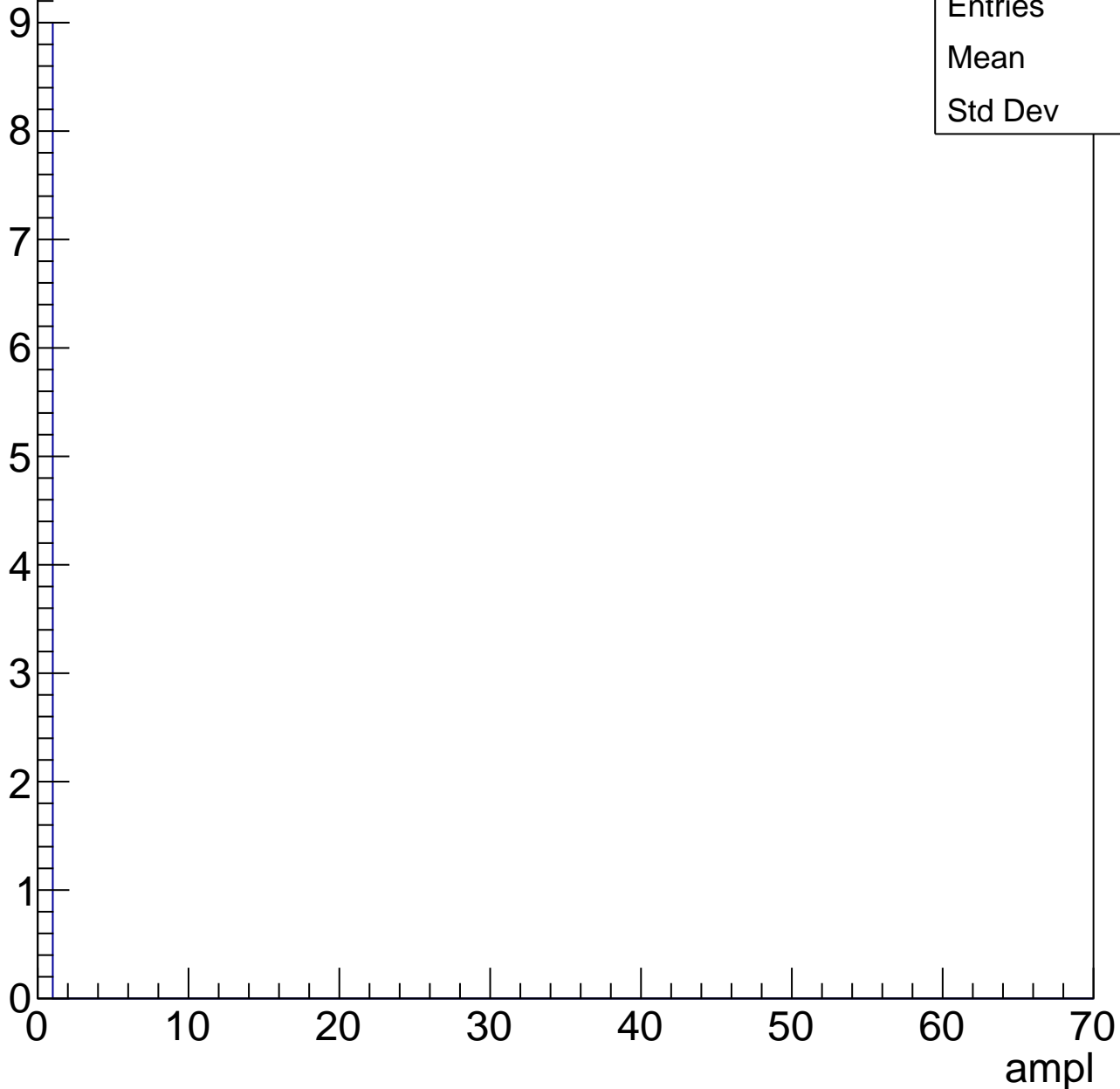


B1L103S, U14-ch24, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	9
Mean	0
Std Dev	0

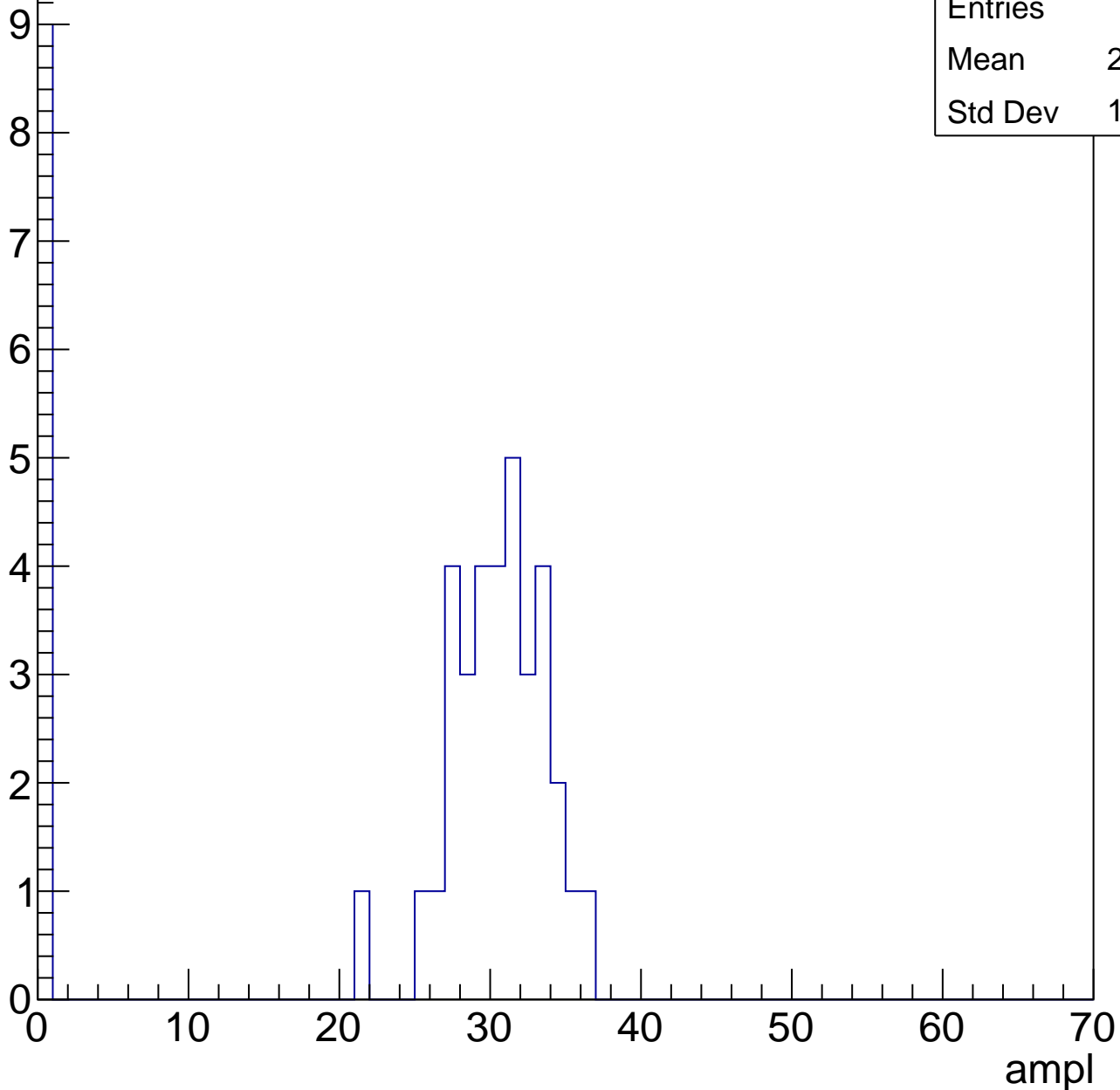


B1L103S, U14-ch25, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	43
Mean	23.77
Std Dev	12.53

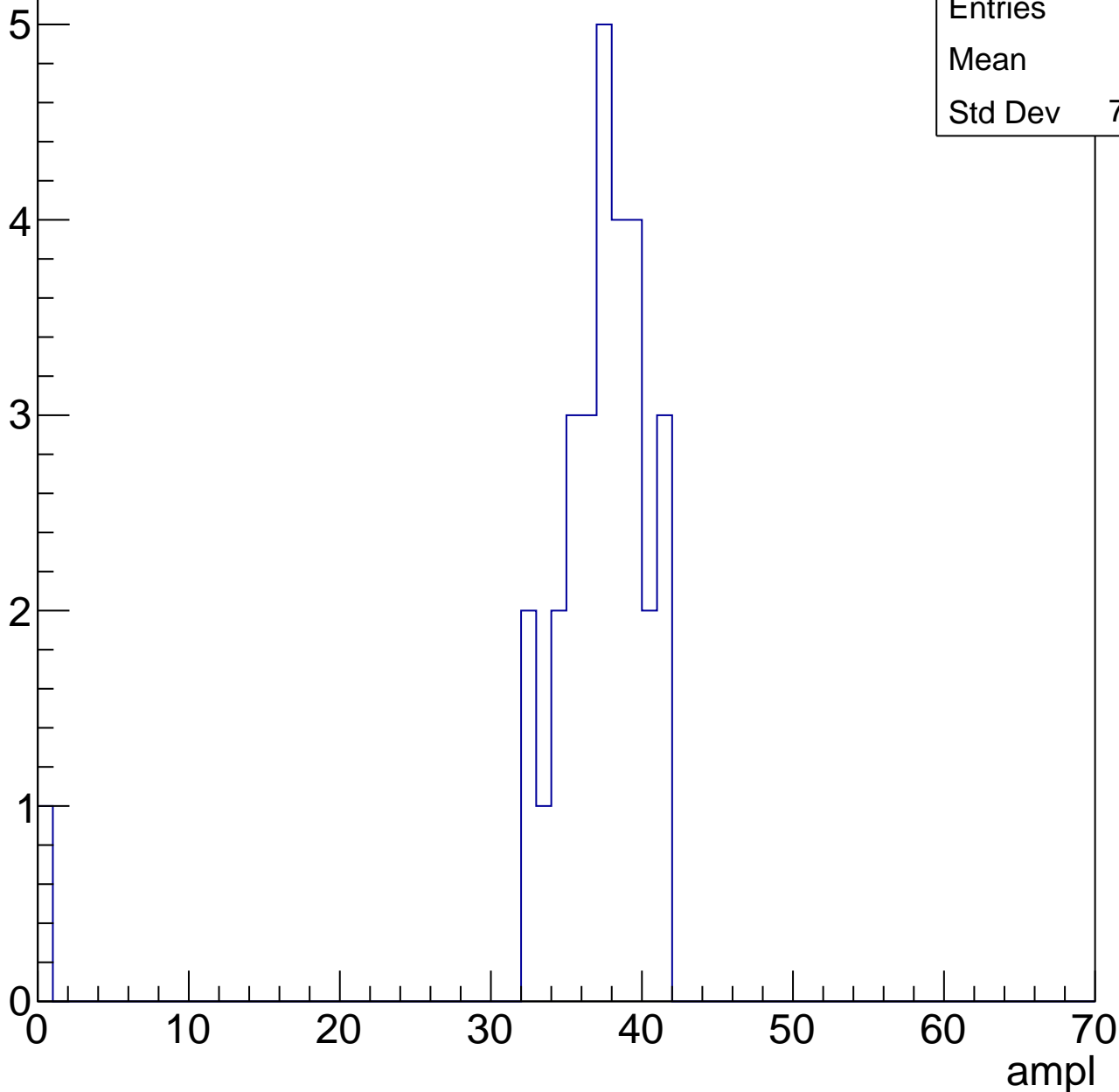


B1L103S, U14-ch25, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	30
Mean	35.8
Std Dev	7.096

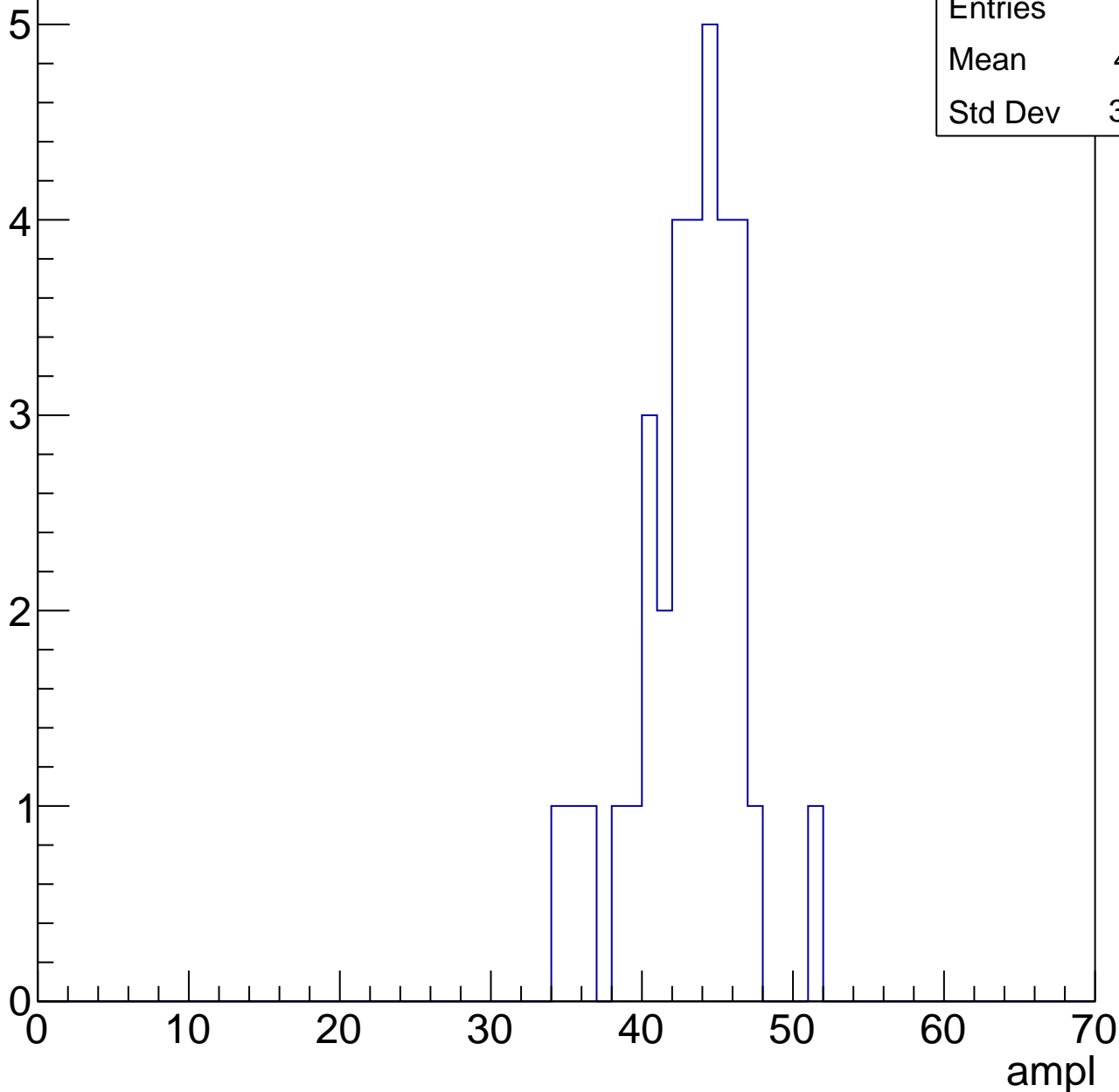


B1L103S, U14-ch25, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	33
Mean	42.61
Std Dev	3.507

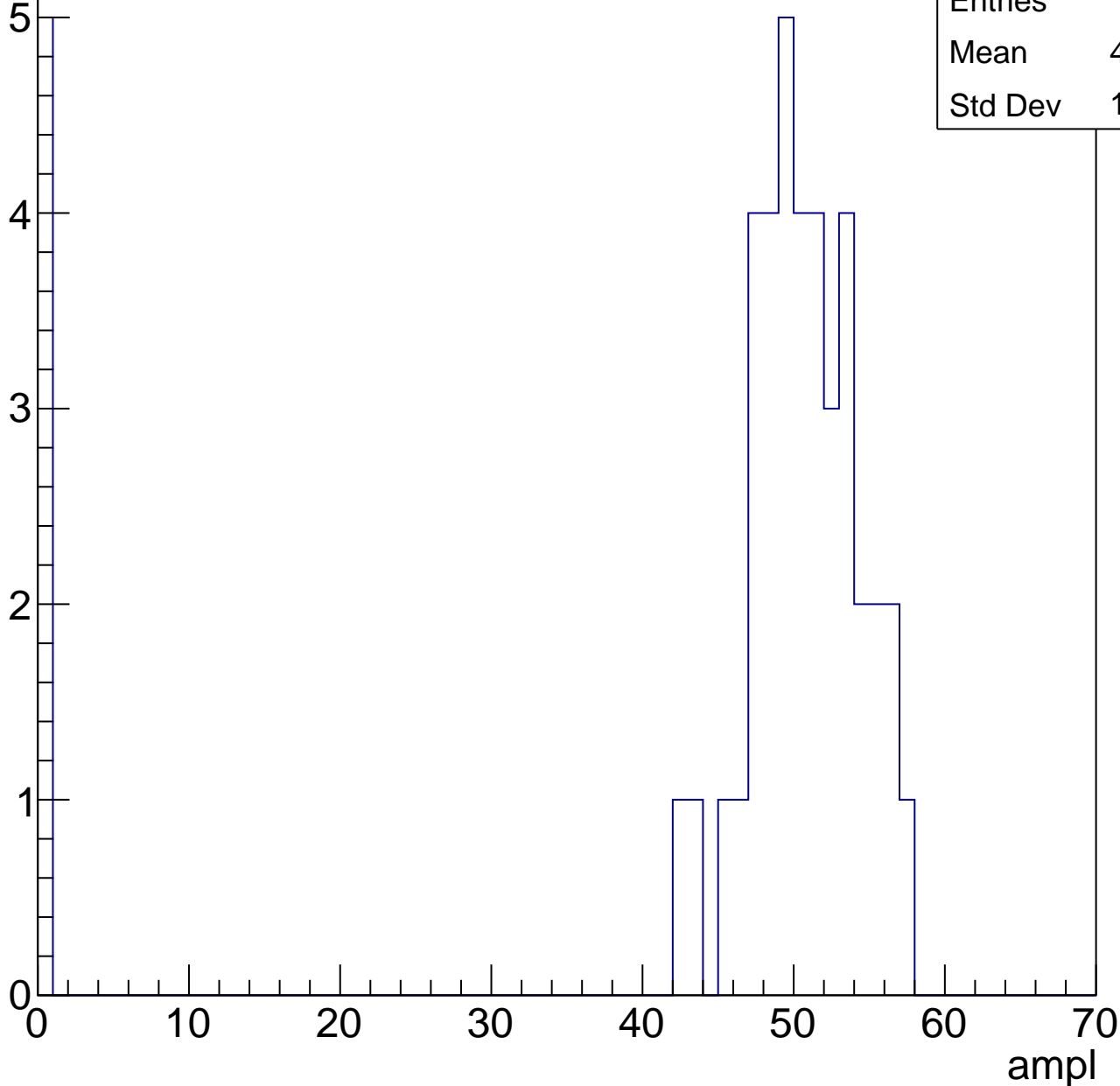


B1L103S, U14-ch25, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

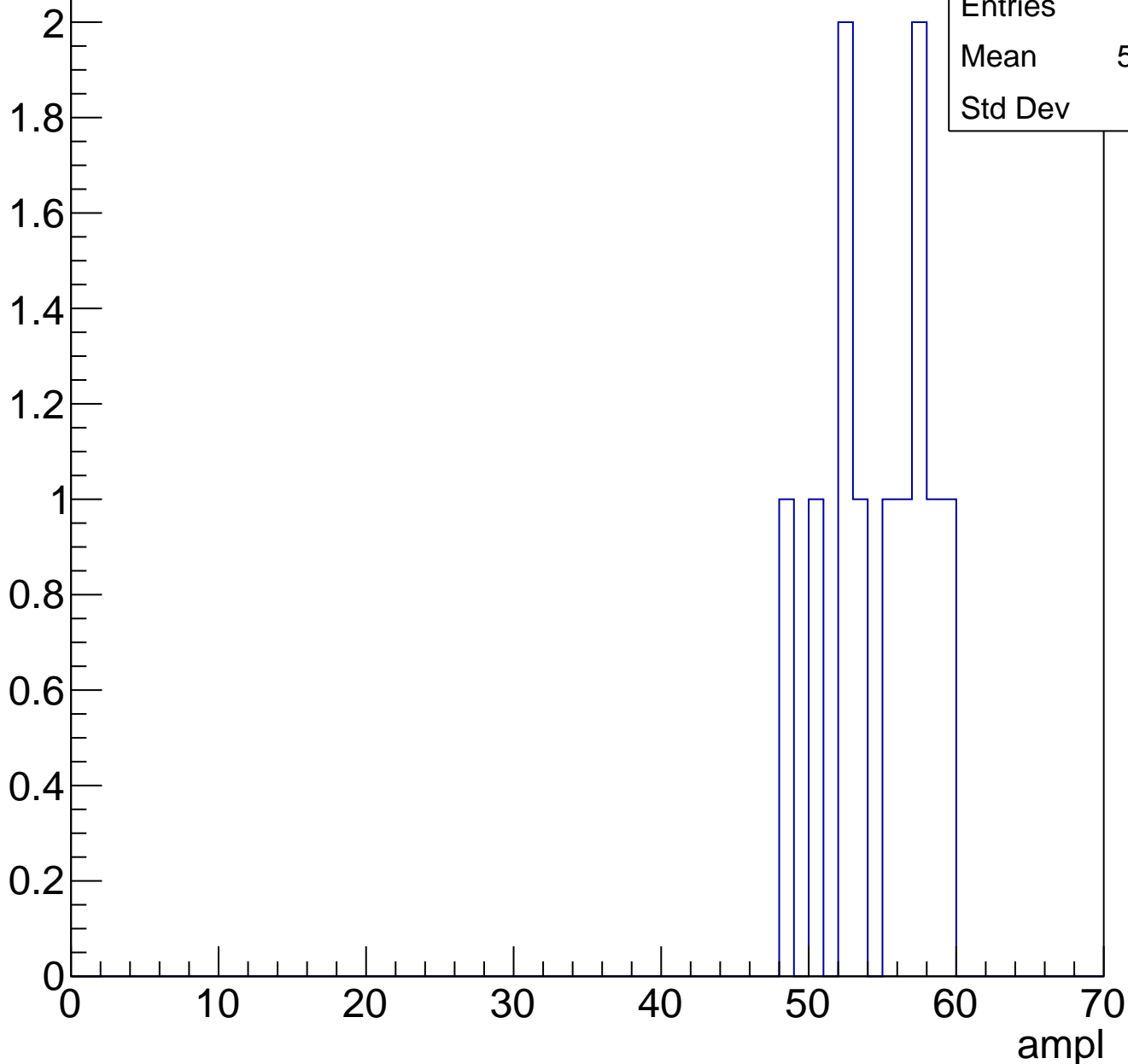
Entries	44
Mean	44.55
Std Dev	16.28



B1L103S, U14-ch25, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

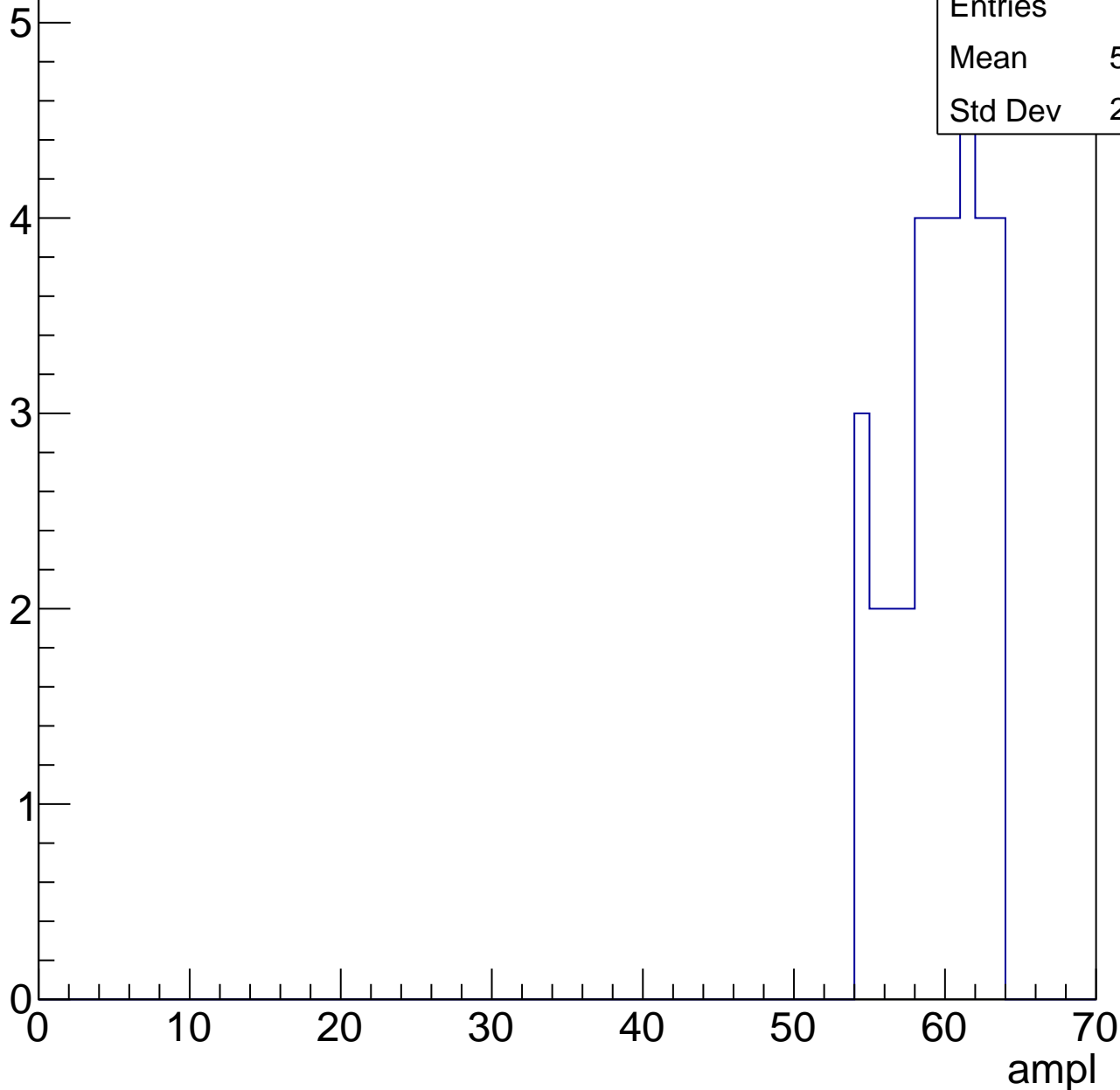


B1L103S, U14-ch25, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

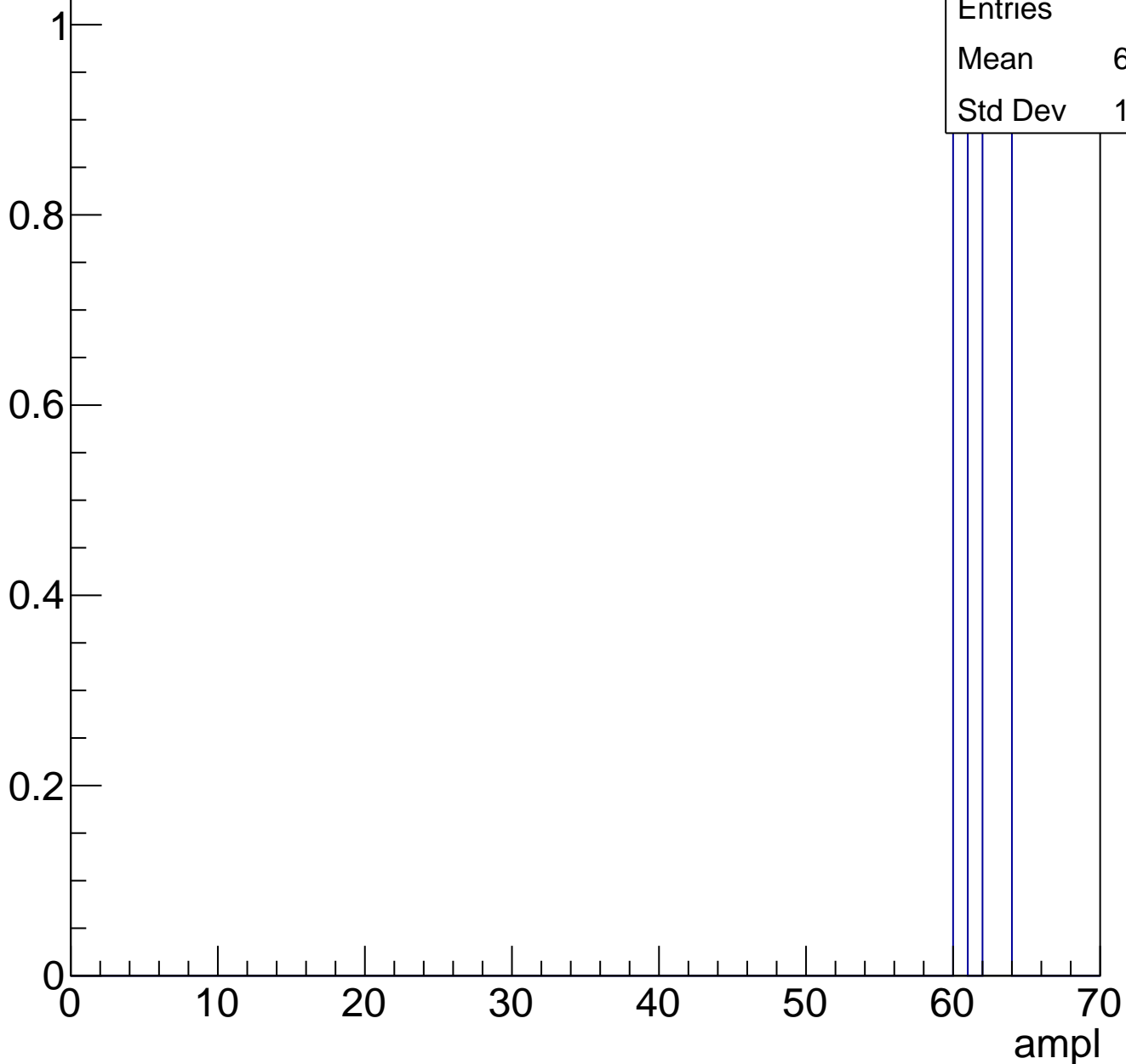
Entries	34
Mean	59.15
Std Dev	2.767



B1L103S, U14-ch25, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch25, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	12
Mean	1.5
Std Dev	4.975

Entry

10

8

6

4

2

0

0

10

20

30

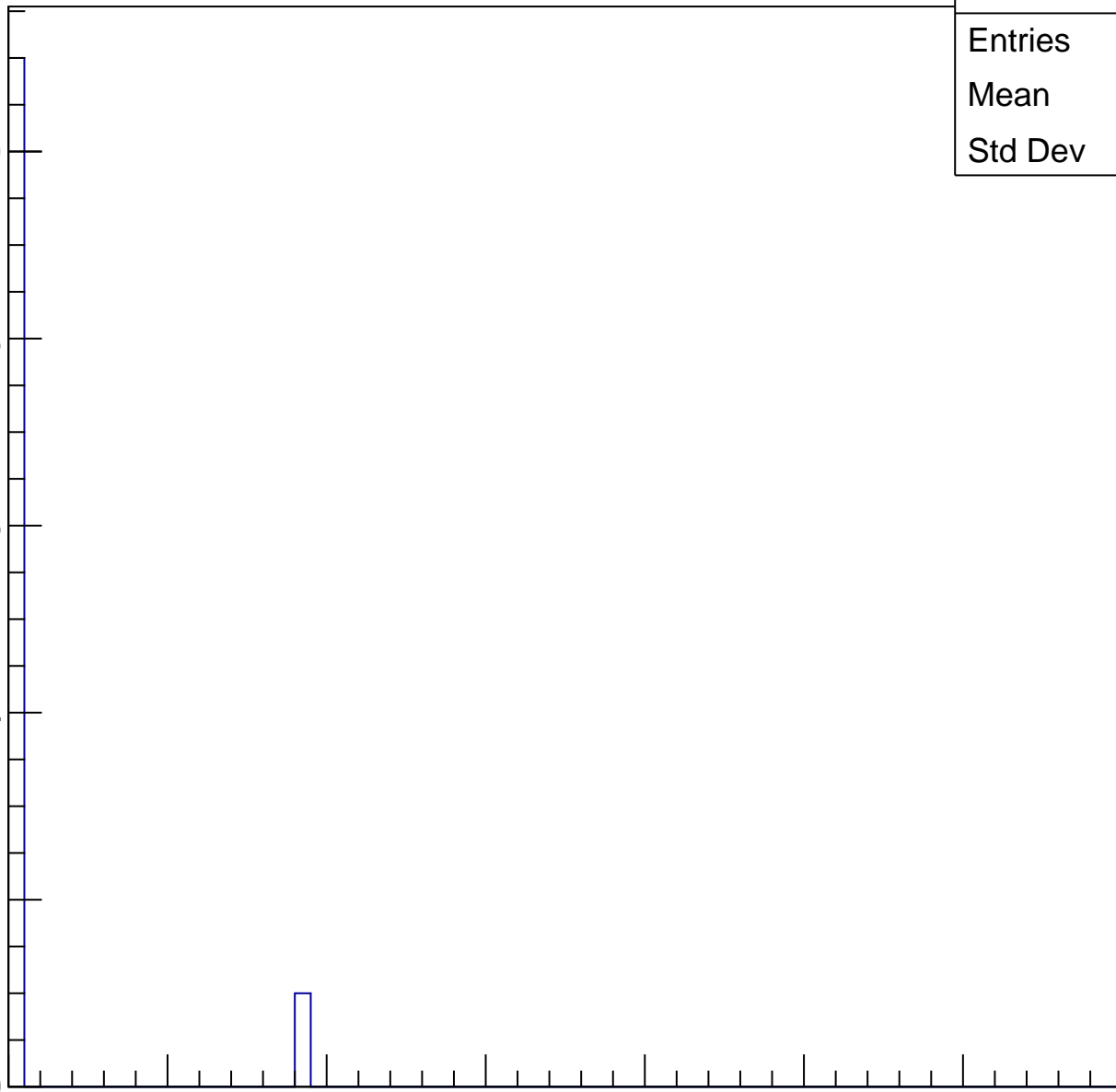
40

50

60

70

ampl



B1L103S, U14-ch26, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	47
Mean	22.19
Std Dev	12.55

Entry

10

8

6

4

2

0

0

10

20

30

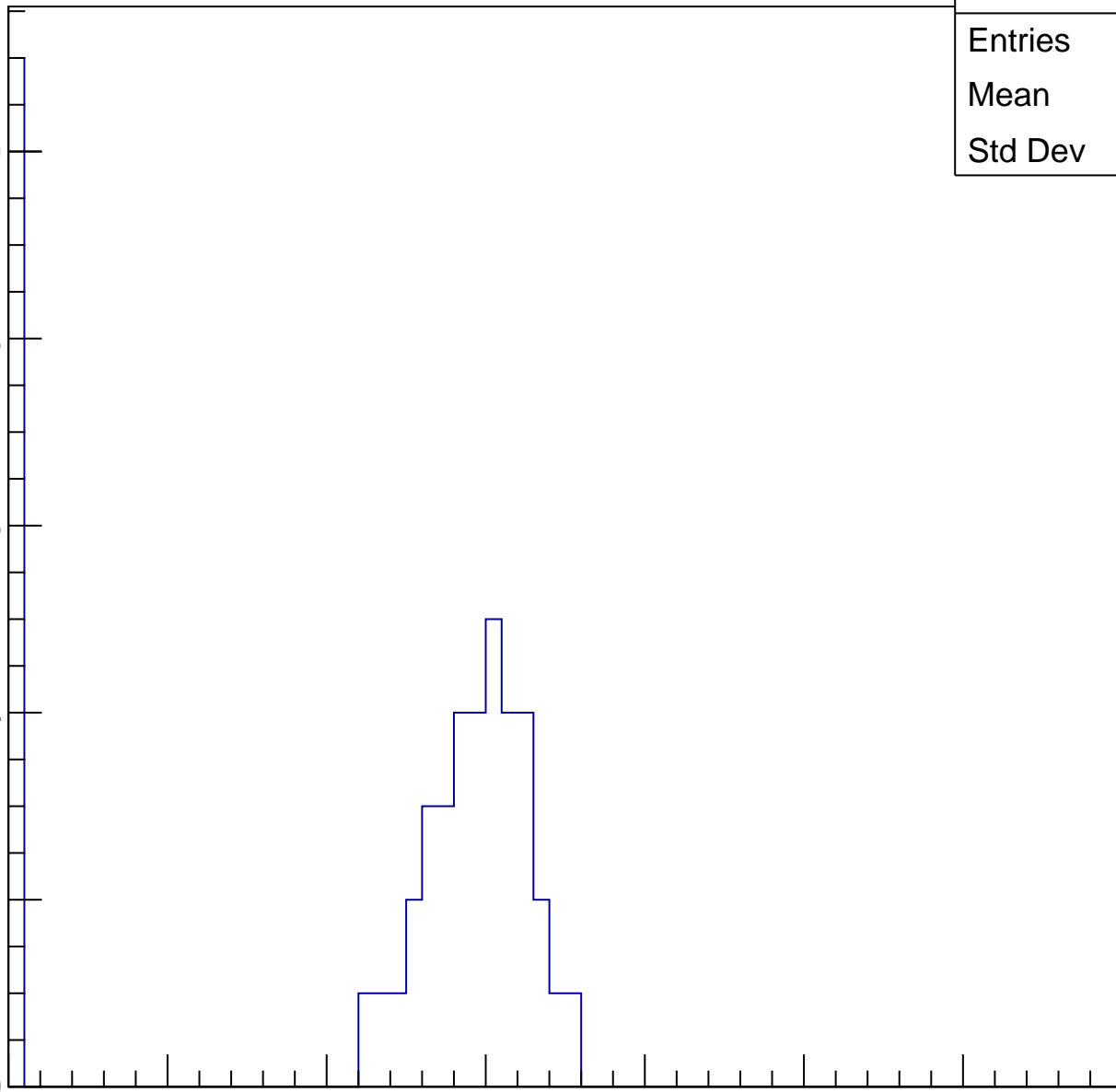
40

50

60

70

ampl

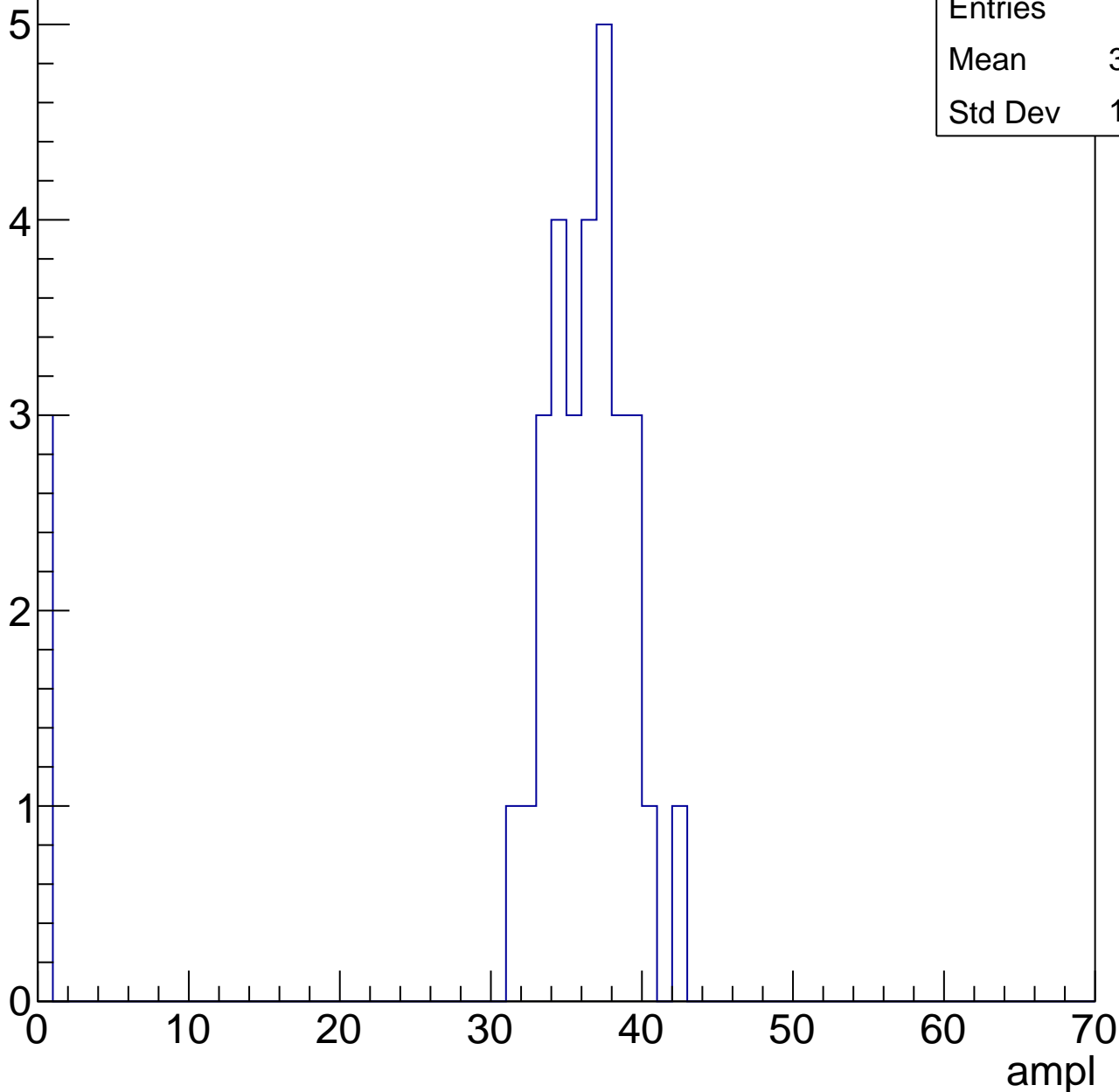


B1L103S, U14-ch26, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	32
Mean	32.66
Std Dev	10.77

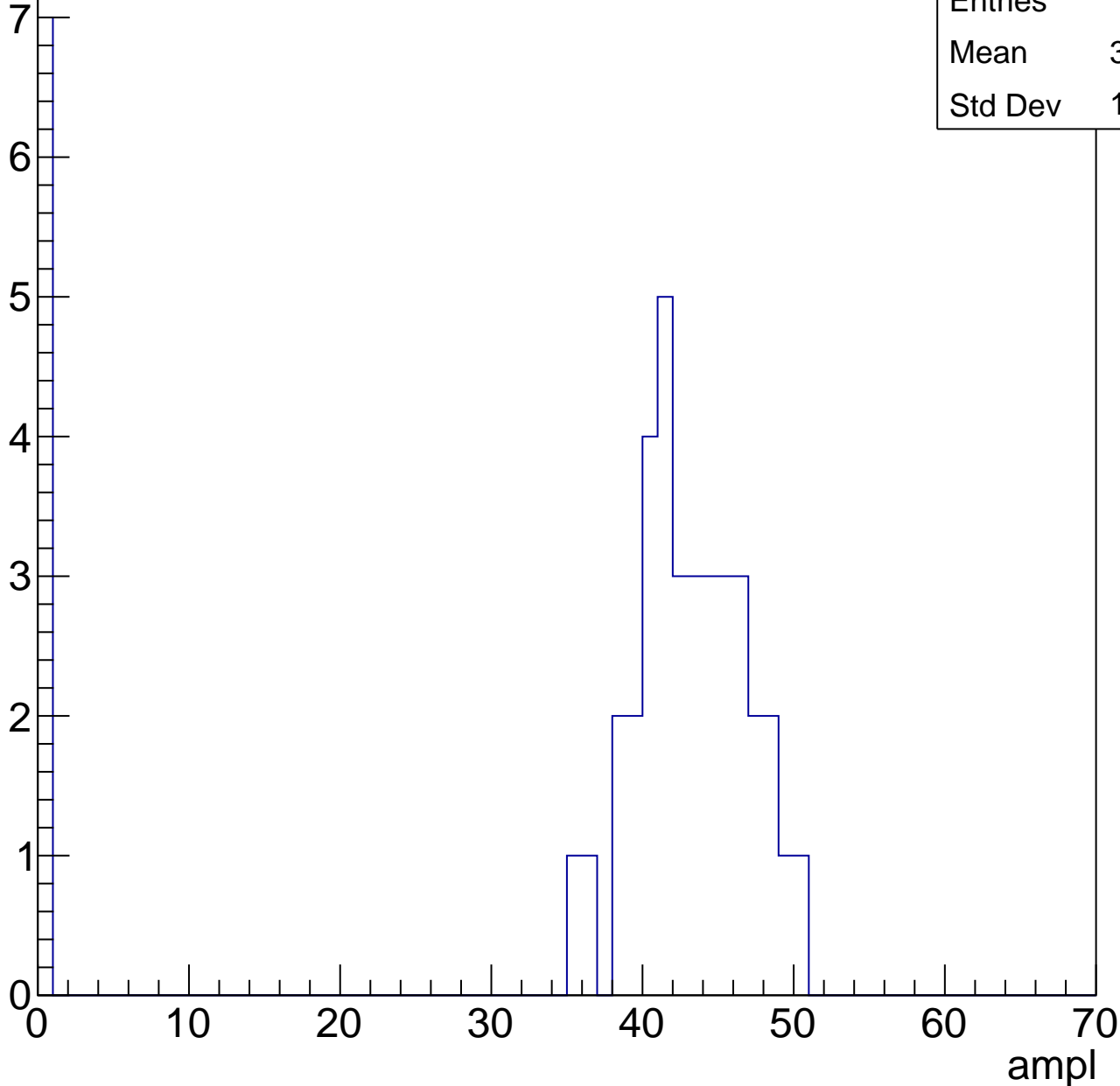


B1L103S, U14-ch26, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

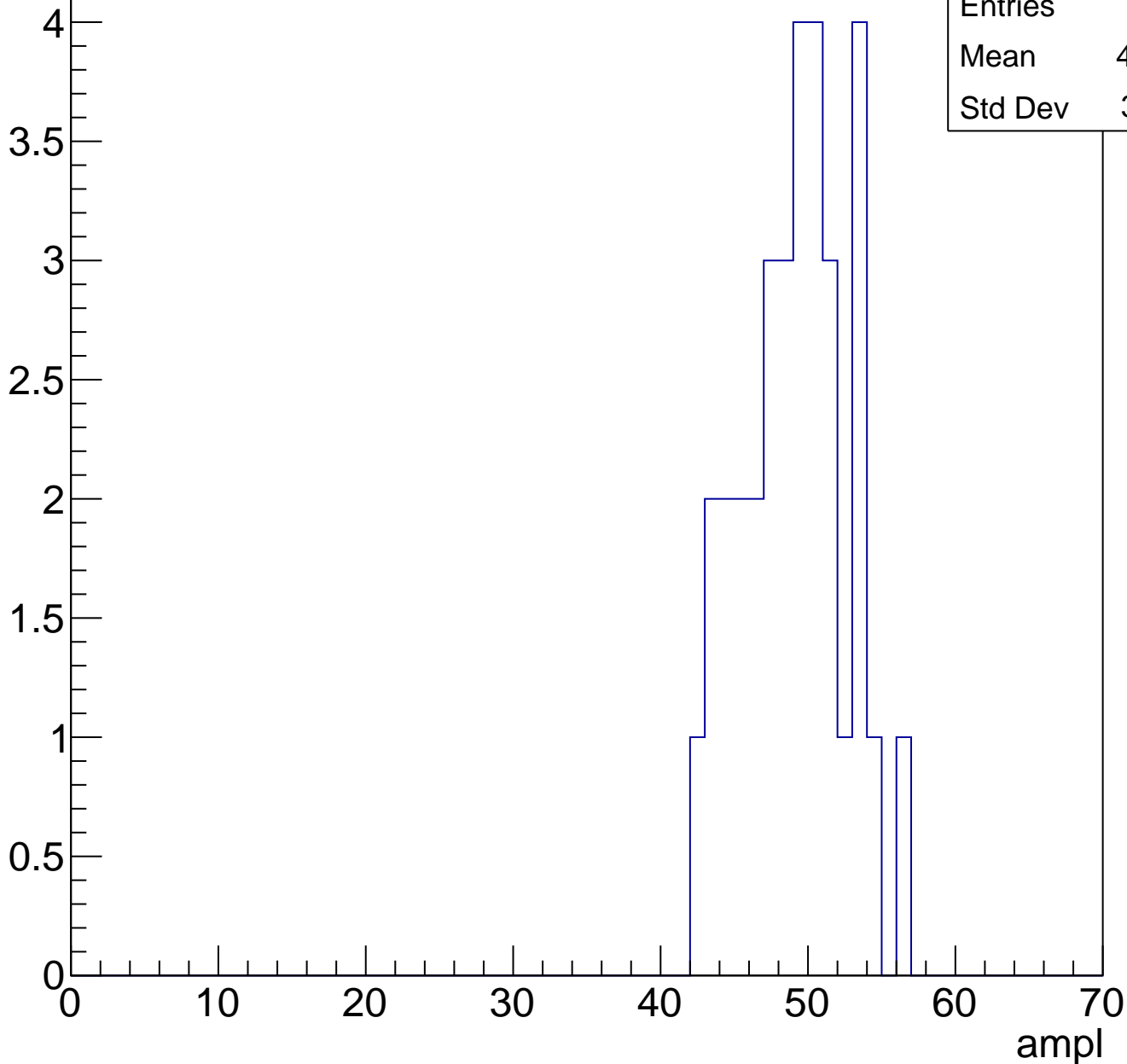
Entries	43
Mean	35.79
Std Dev	16.12



B1L103S, U14-ch26, adc3

calib_packv5_041523_1651.root, FC#0, port C2

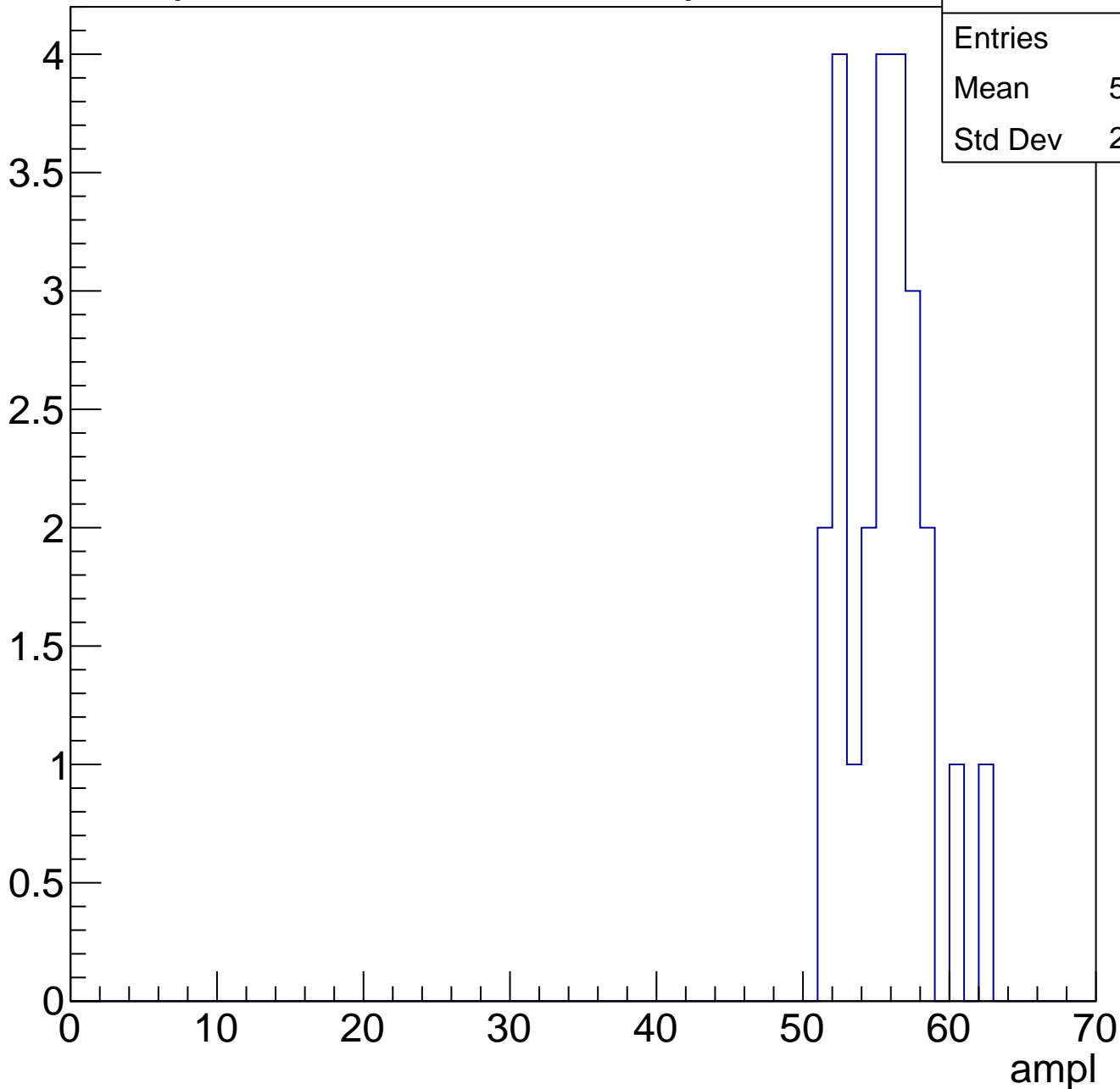
Entry



B1L103S, U14-ch26, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch26, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

5

4

3

2

1

0

Entries	25
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Mean	59.36
------	-------

Std Dev	2.559
---------	-------

0

10

20

30

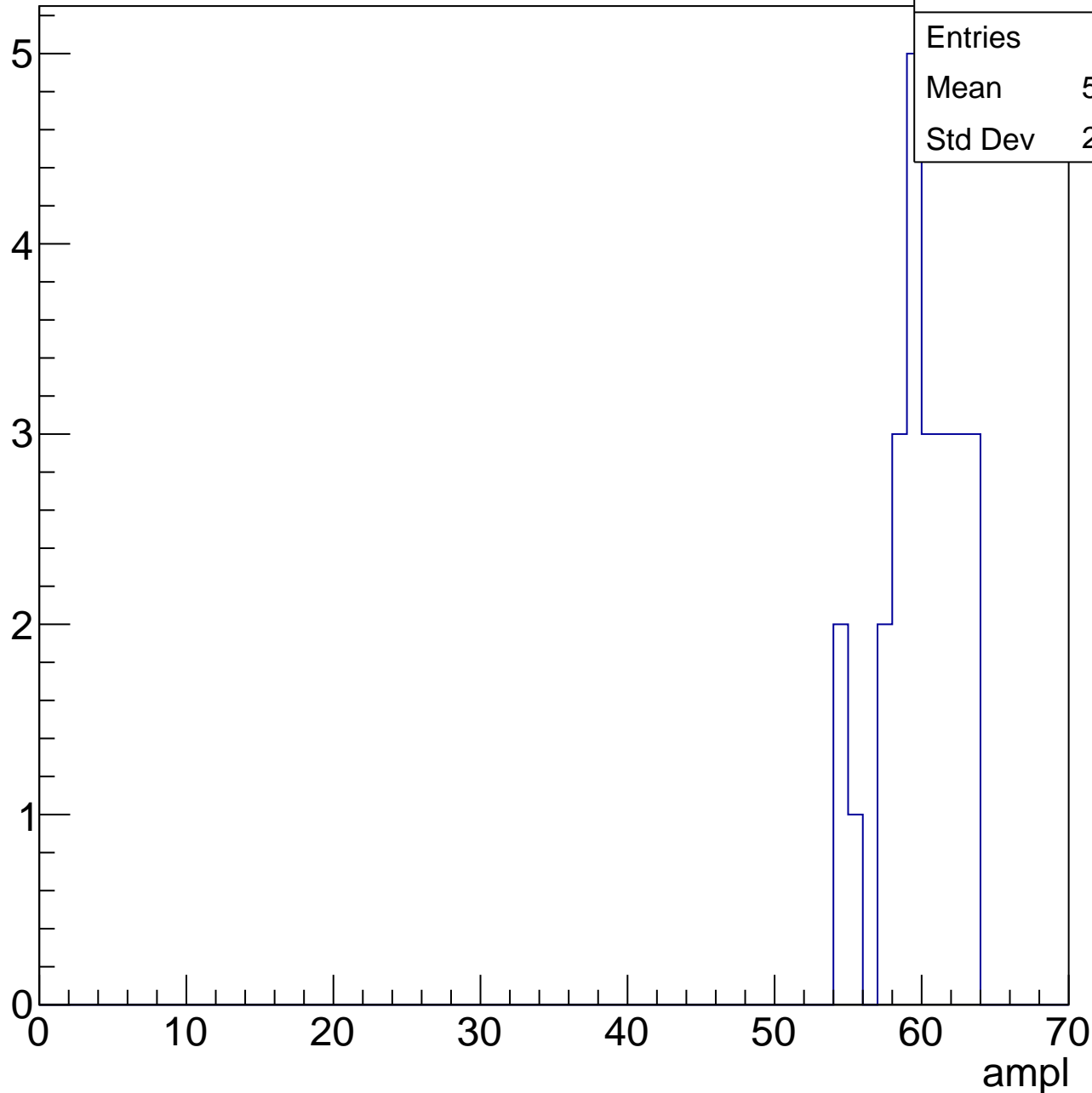
40

50

60

70

ampl



B1L103S, U14-ch26, adc6

calib_packv5_041523_1651.root, FC#0, port C2

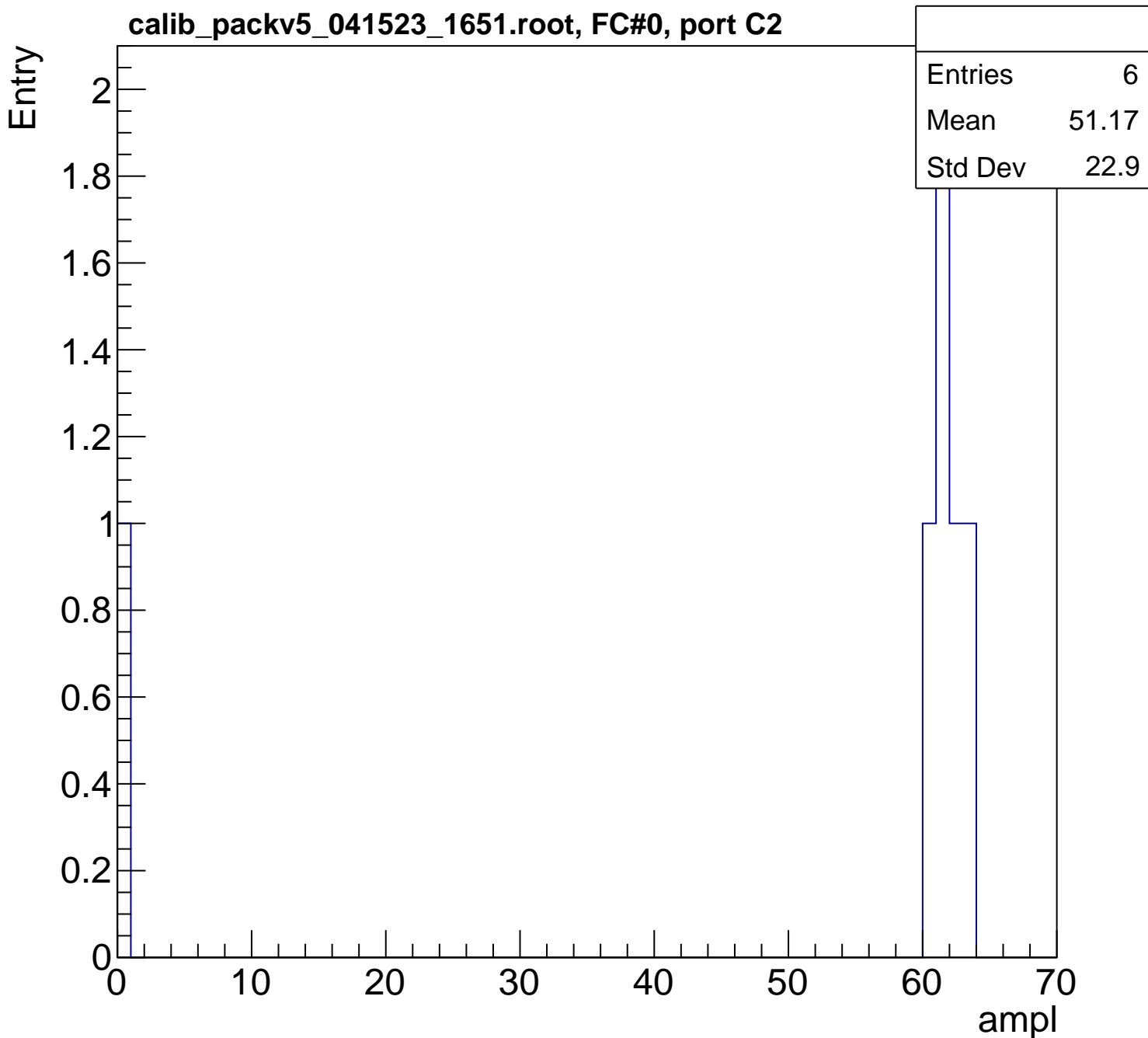
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	6
Mean	51.17
Std Dev	22.9

ampl

0 10 20 30 40 50 60 70

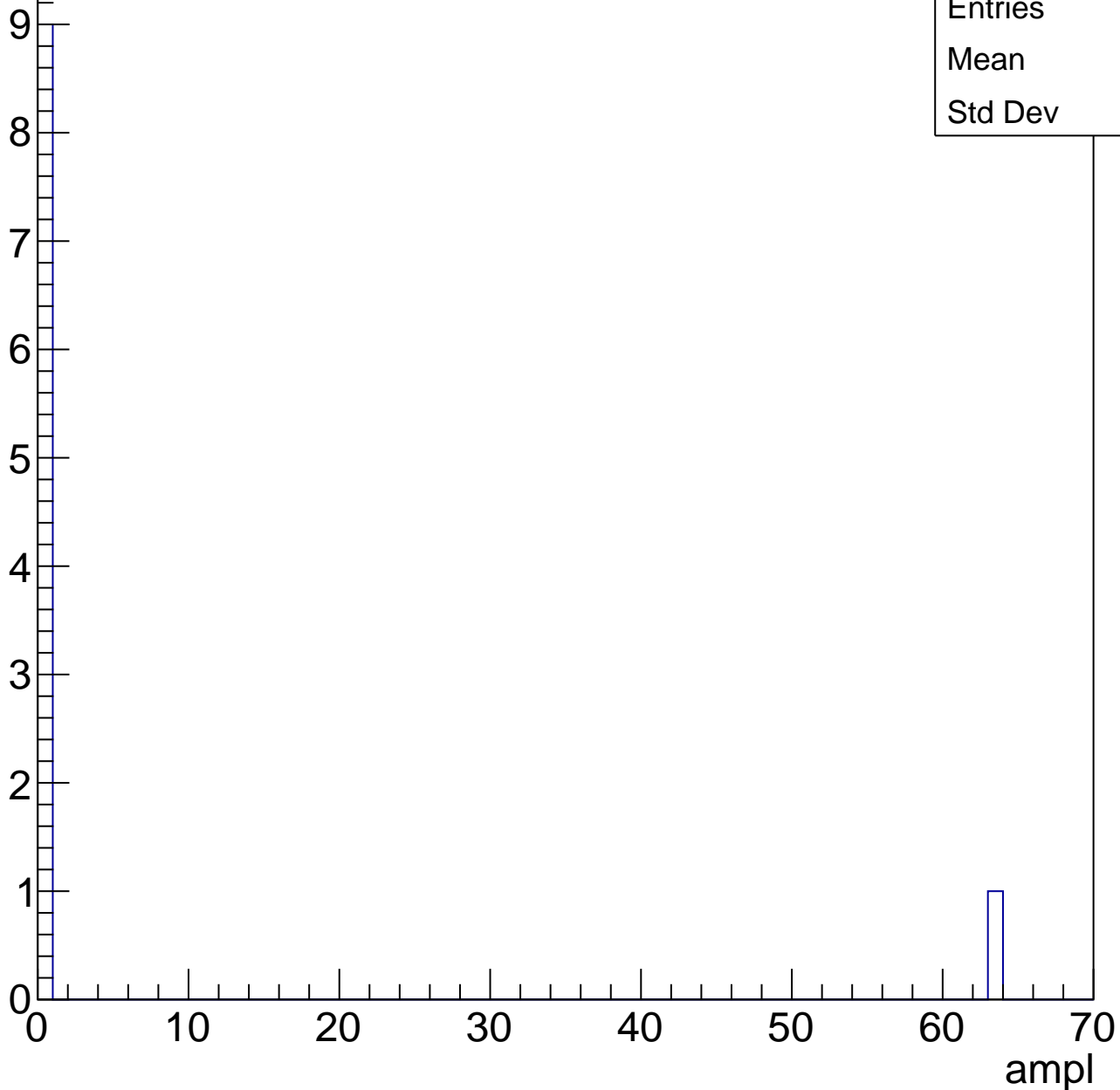


B1L103S, U14-ch26, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	10
Mean	6.3
Std Dev	18.9

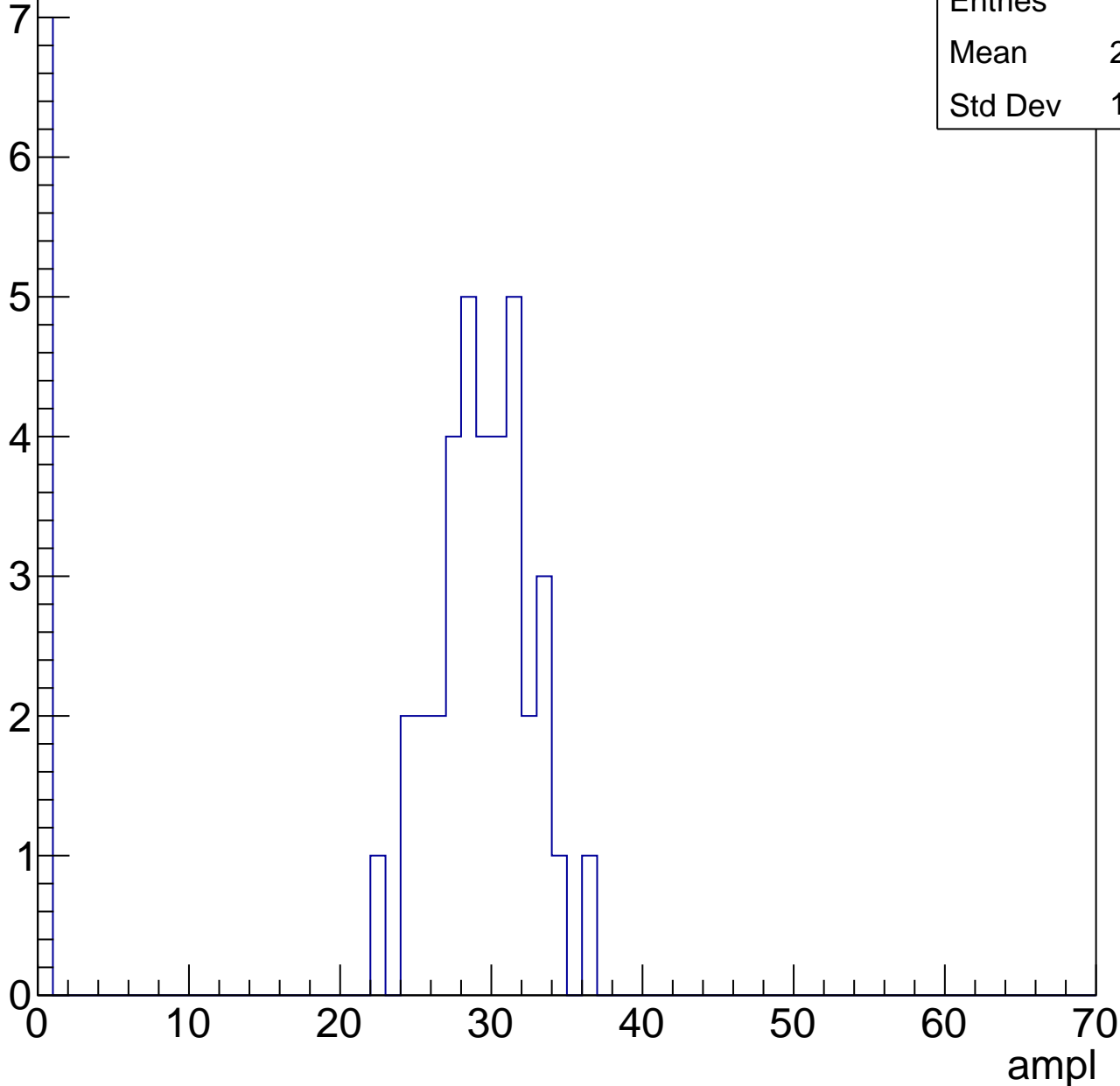


B1L103S, U14-ch27, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	43
Mean	24.28
Std Dev	11.06

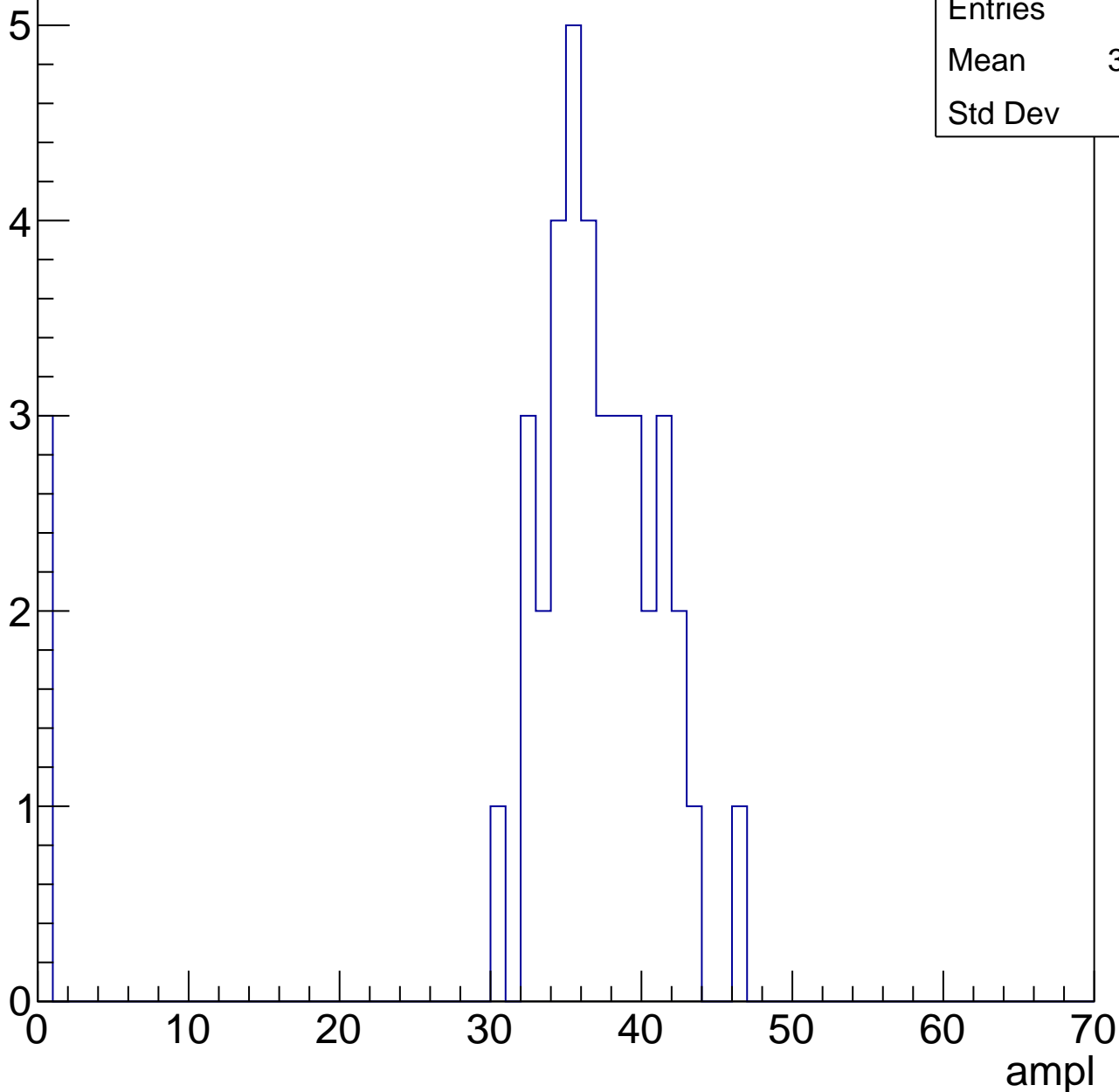


B1L103S, U14-ch27, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	34.12
Std Dev	10.3

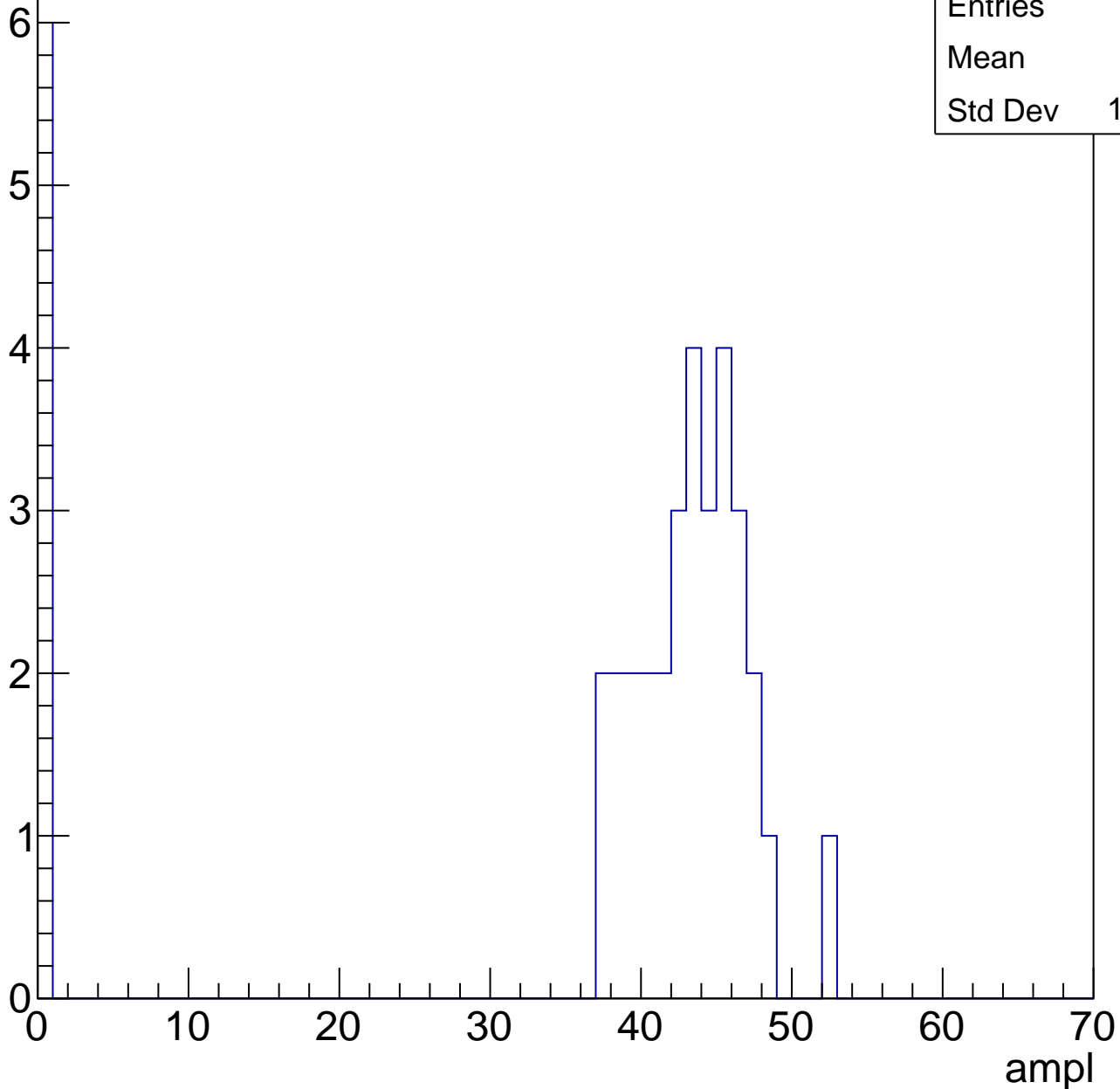


B1L103S, U14-ch27, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	37
Mean	36
Std Dev	16.15

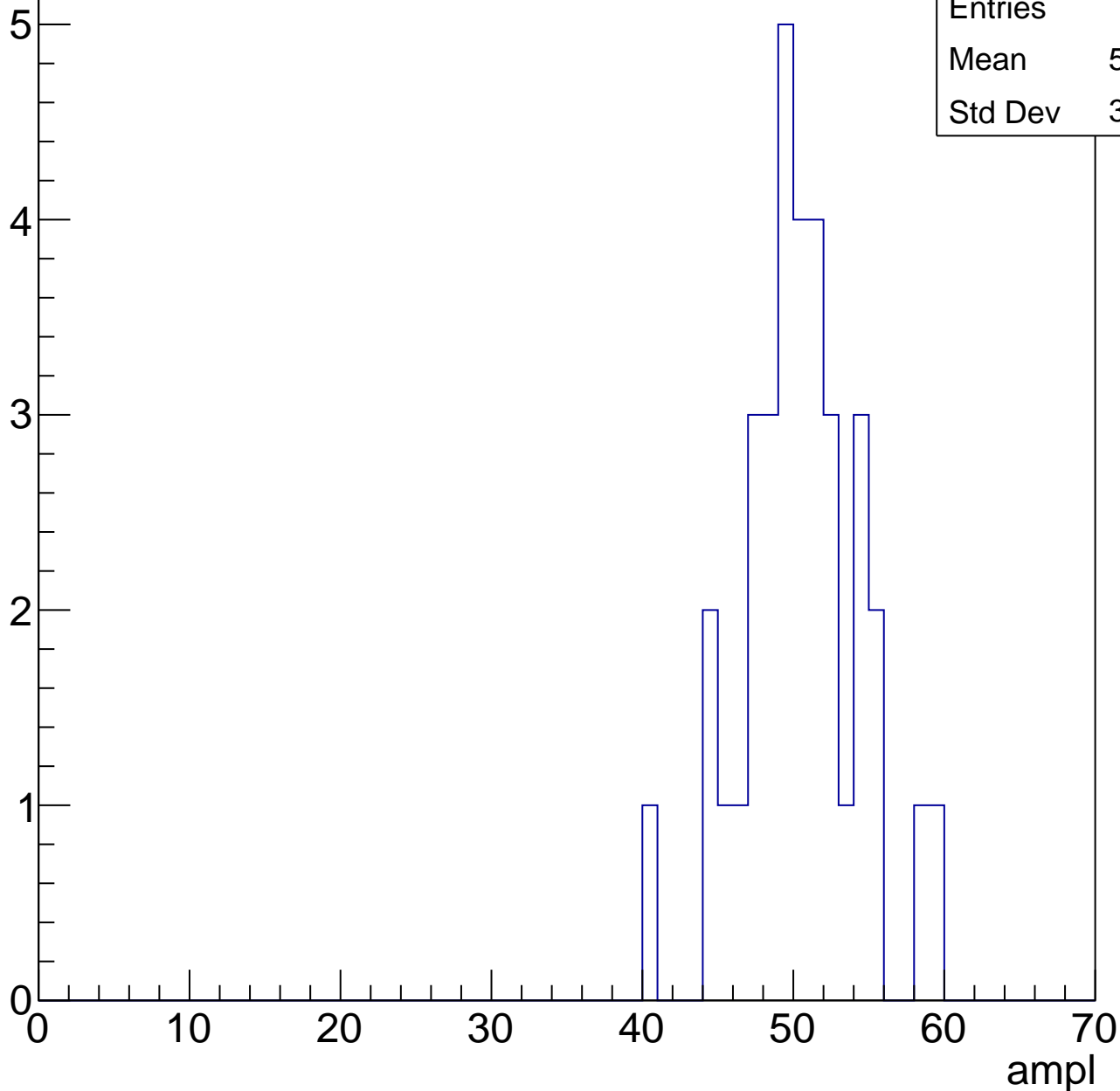


B1L103S, U14-ch27, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	35
Mean	50.03
Std Dev	3.873

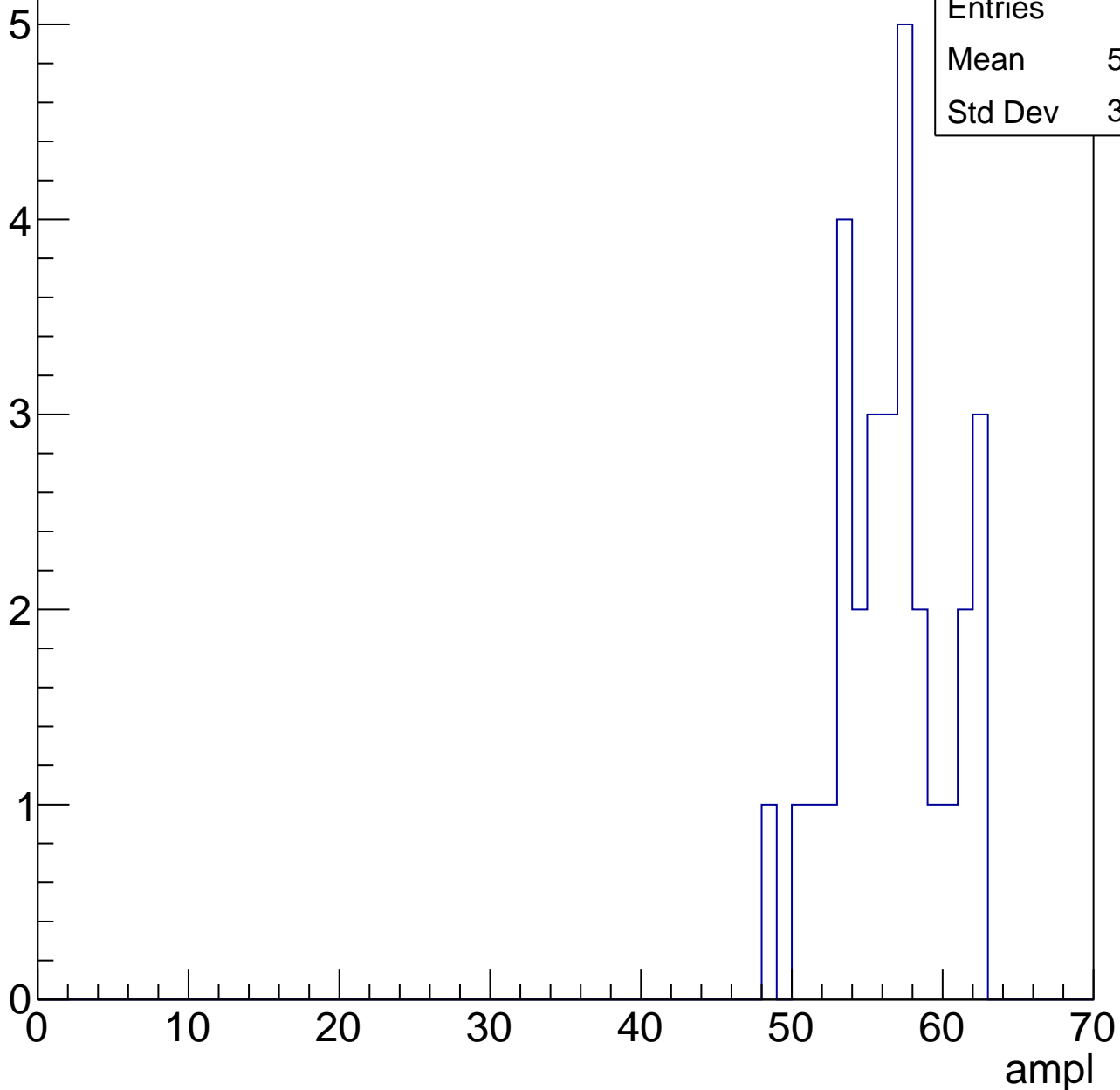


B1L103S, U14-ch27, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

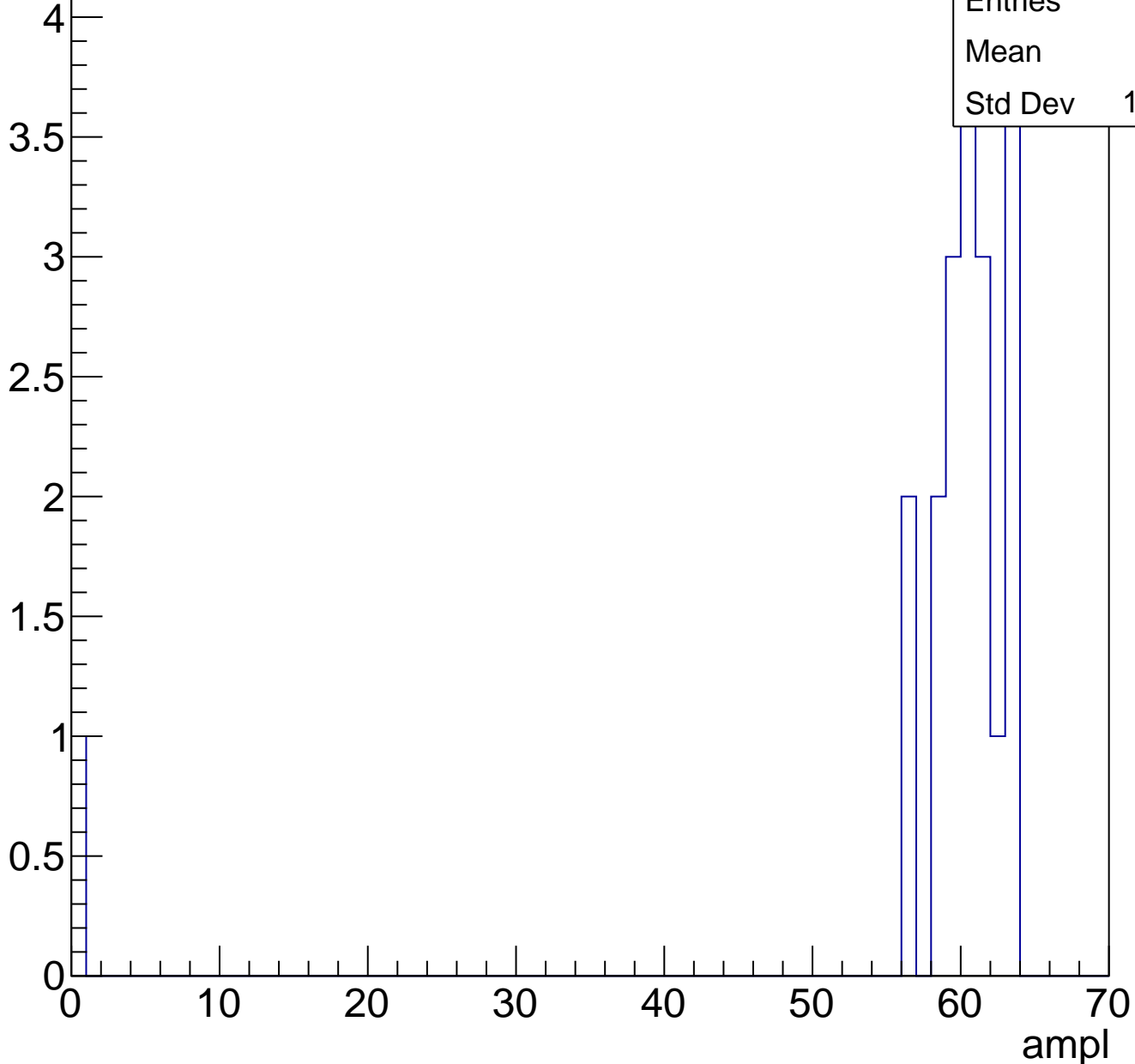
Entries	30
Mean	56.07
Std Dev	3.577



B1L103S, U14-ch27, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch27, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

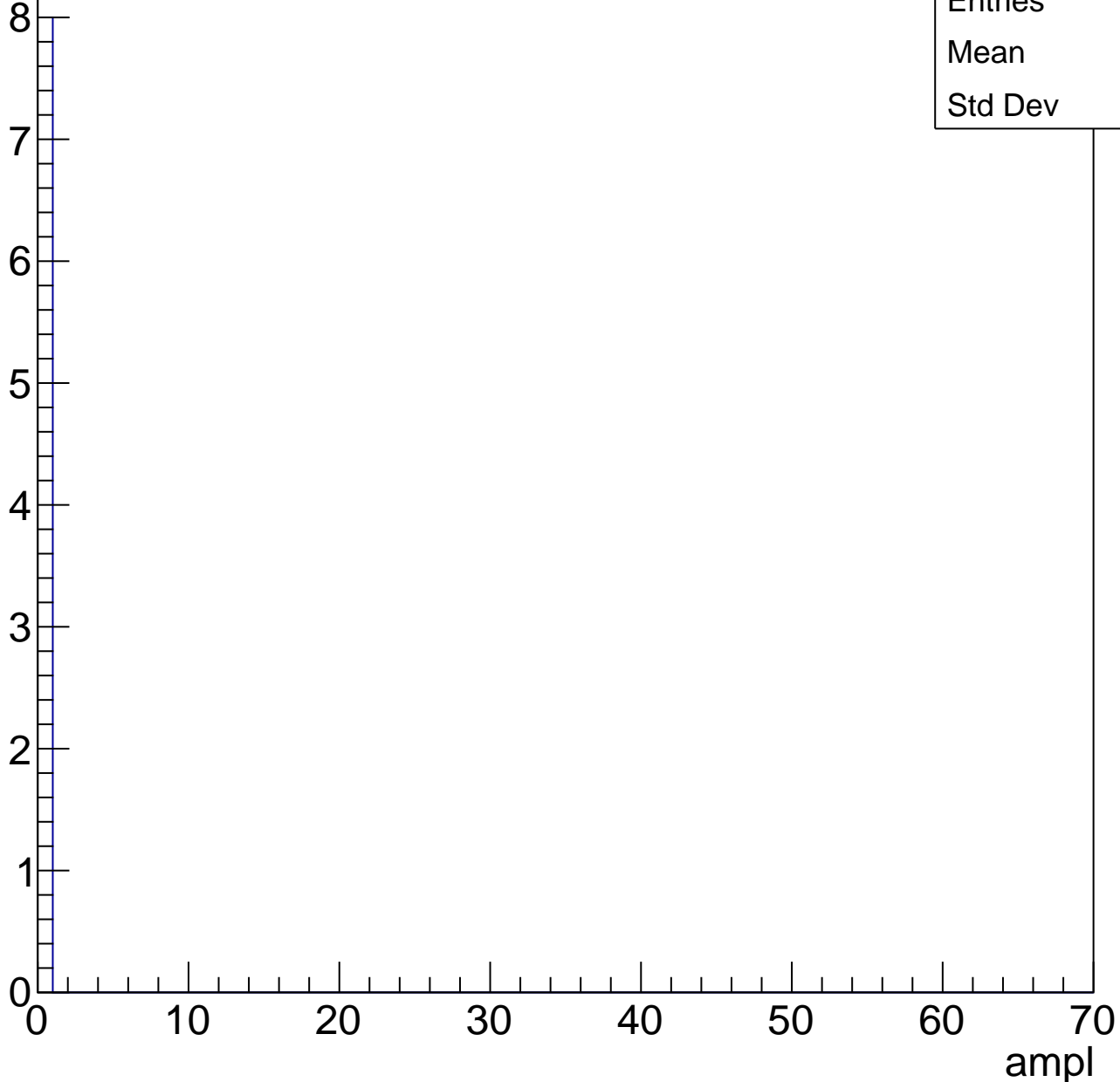


B1L103S, U14-ch27, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	8
Mean	0
Std Dev	0



B1L103S, U14-ch28, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	42
Mean	19.5
Std Dev	13.3

Entry

12

10

8

6

4

2

0

0

10

20

30

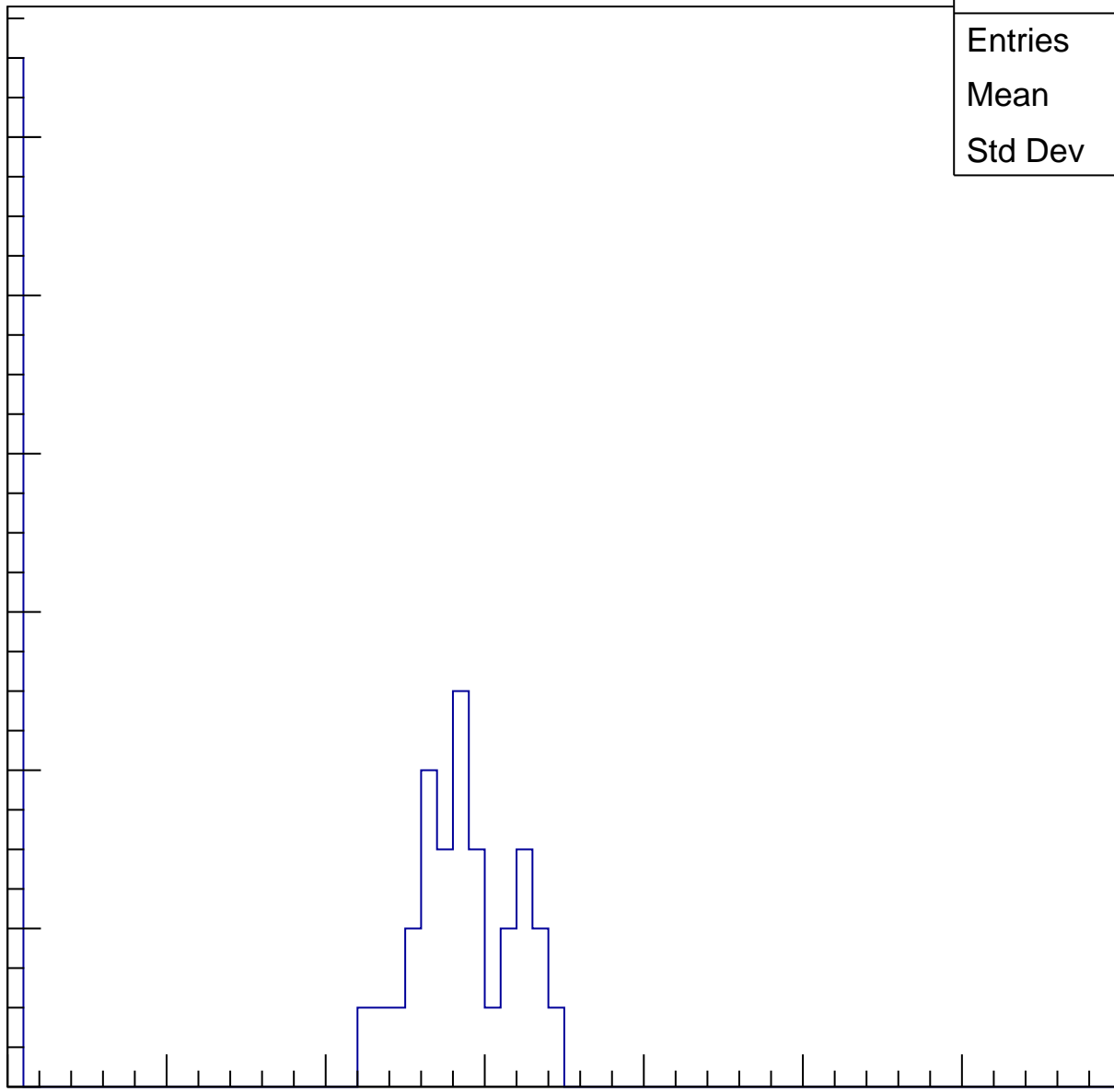
40

50

60

70

ampl

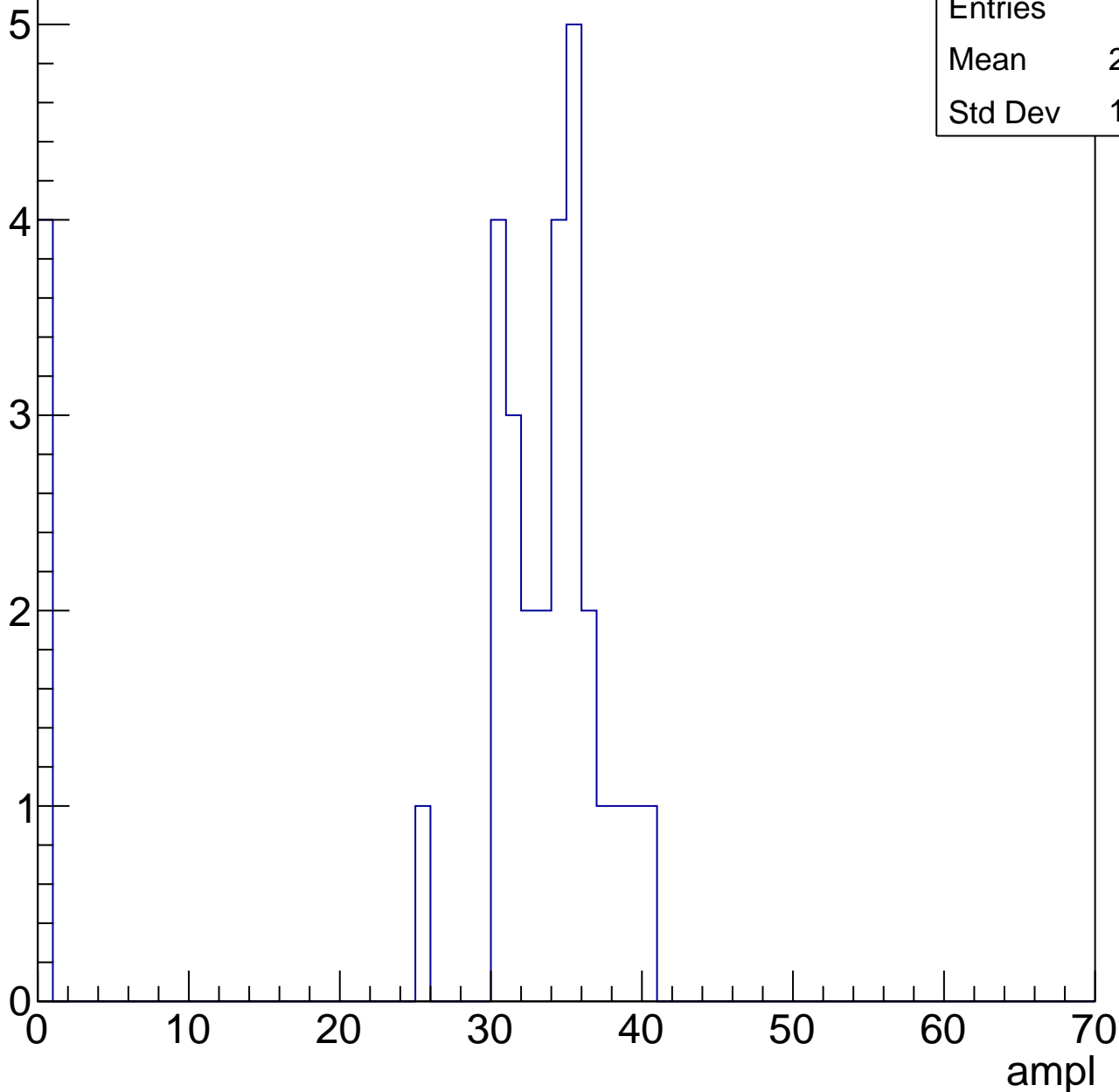


B1L103S, U14-ch28, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

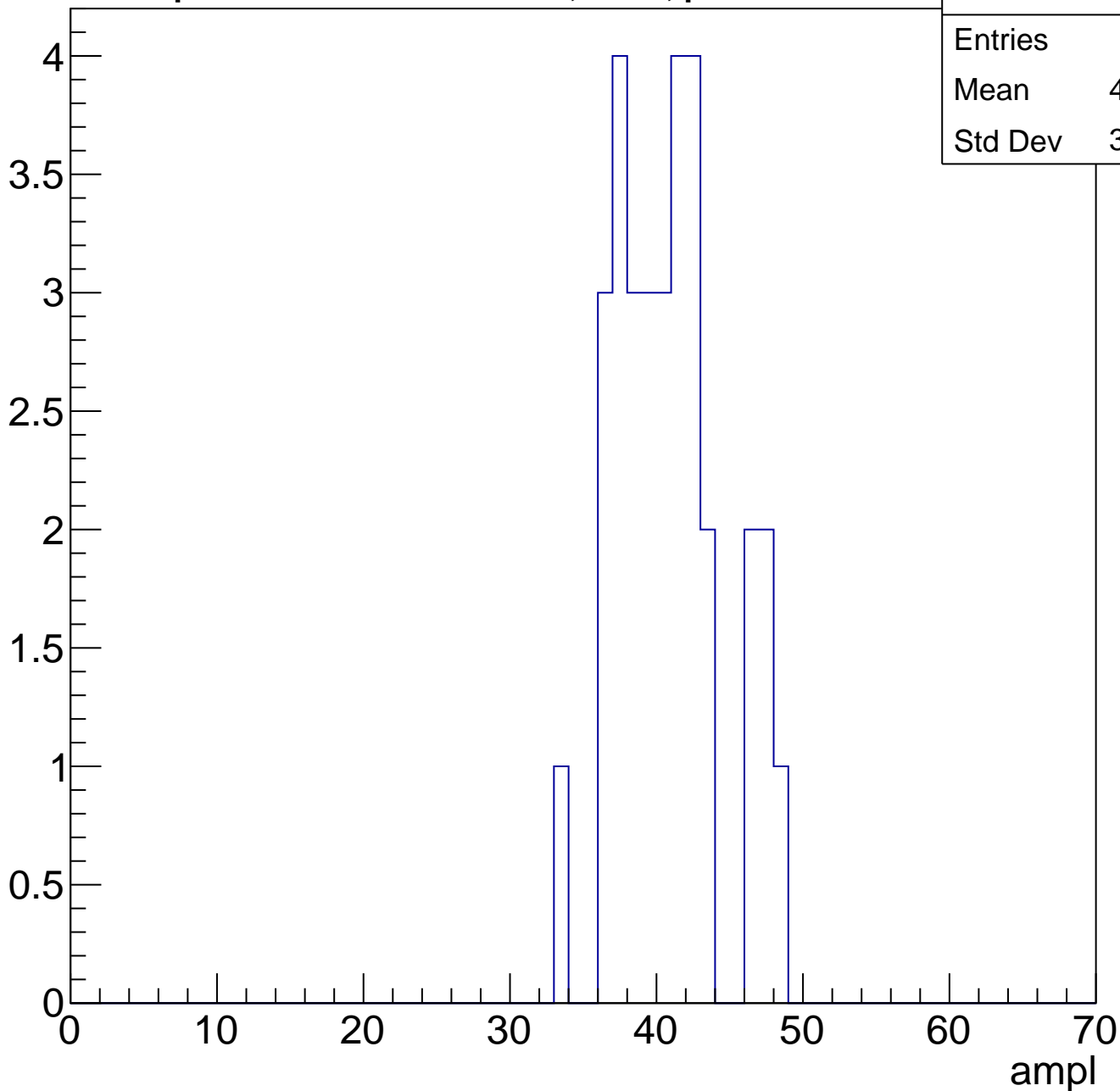
Entries	31
Mean	29.19
Std Dev	11.62



B1L103S, U14-ch28, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry



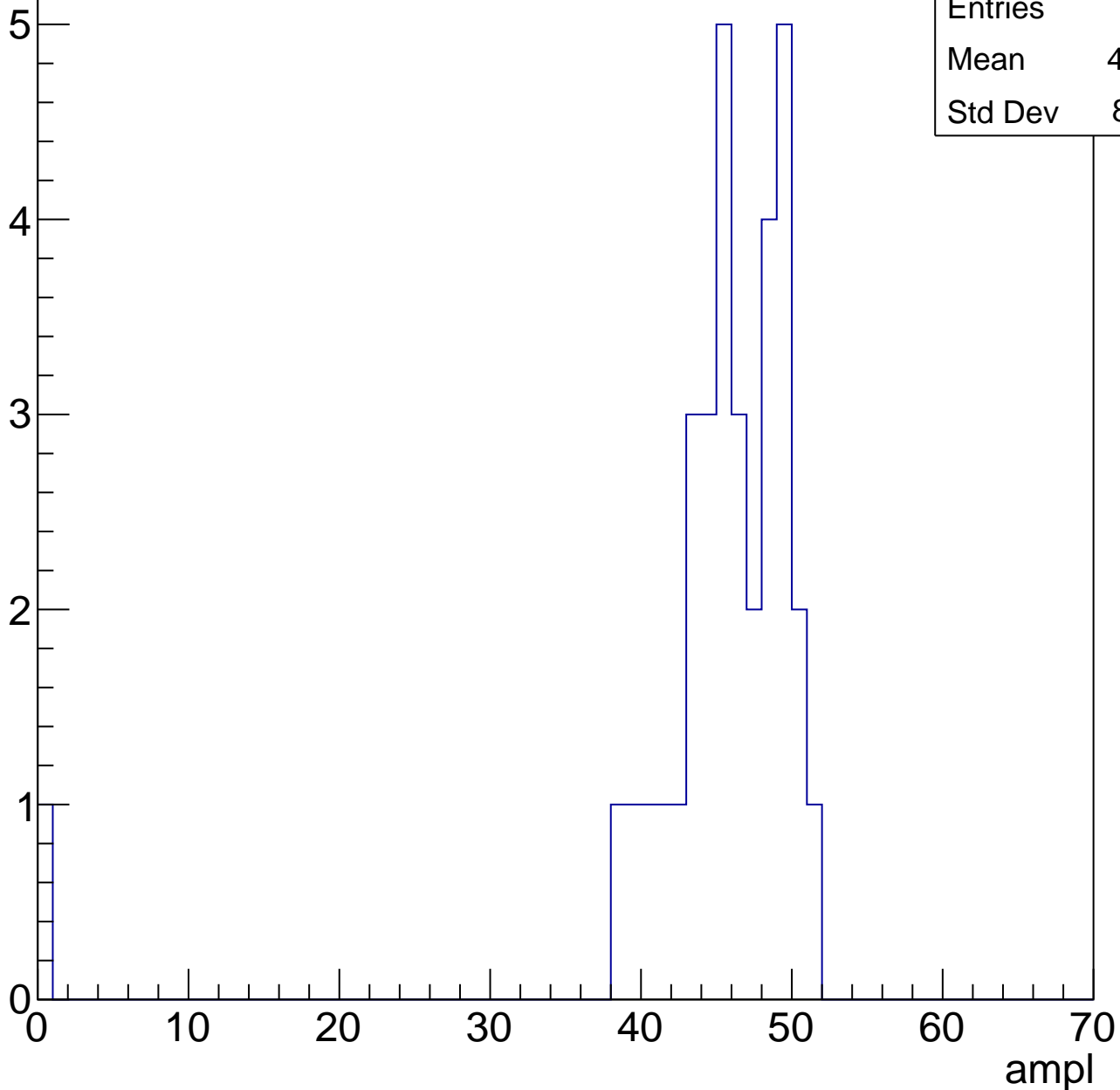
Entries	32
Mean	40.38
Std Dev	3.603

B1L103S, U14-ch28, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	34
Mean	44.29
Std Dev	8.351

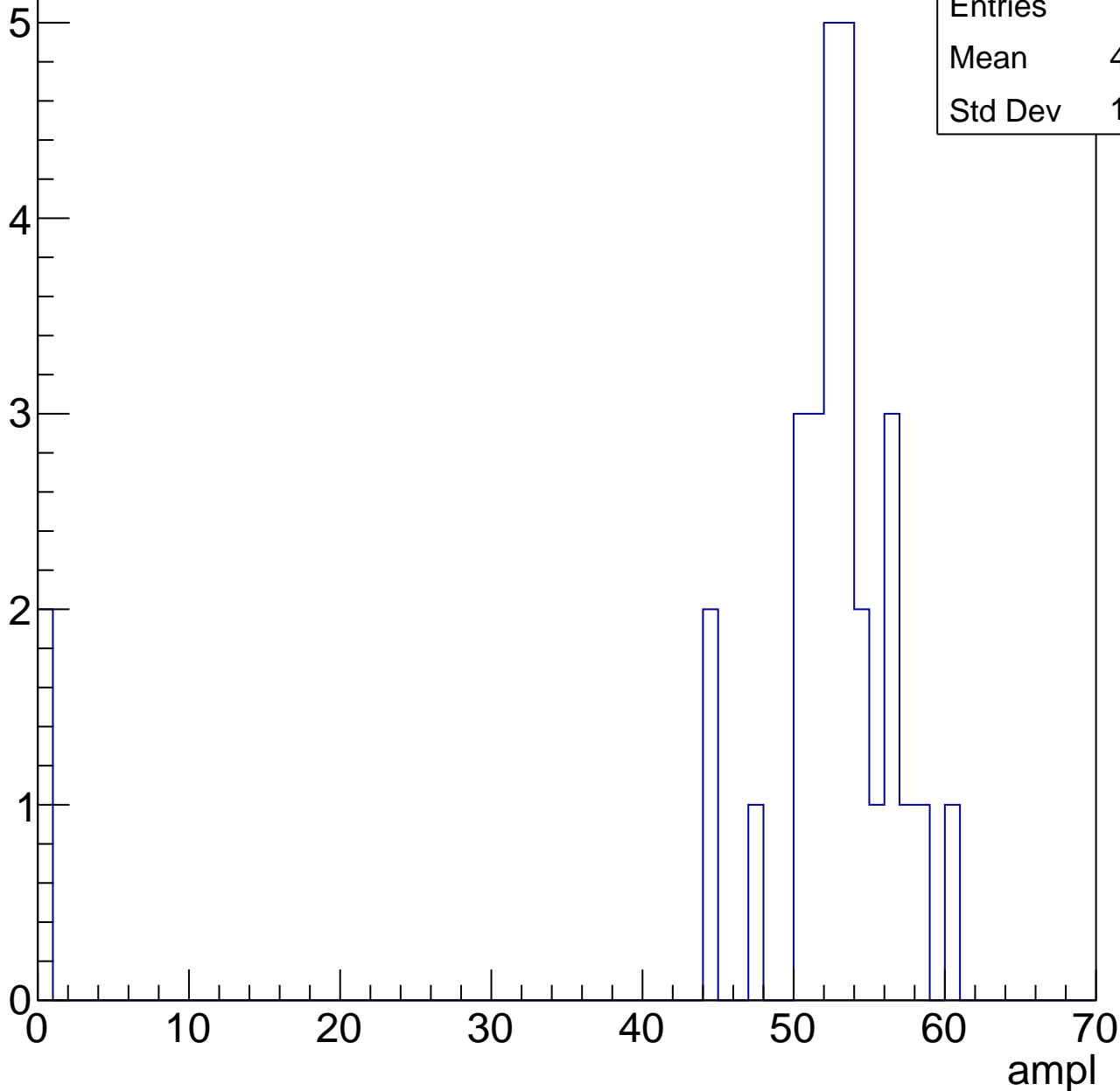


B1L103S, U14-ch28, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

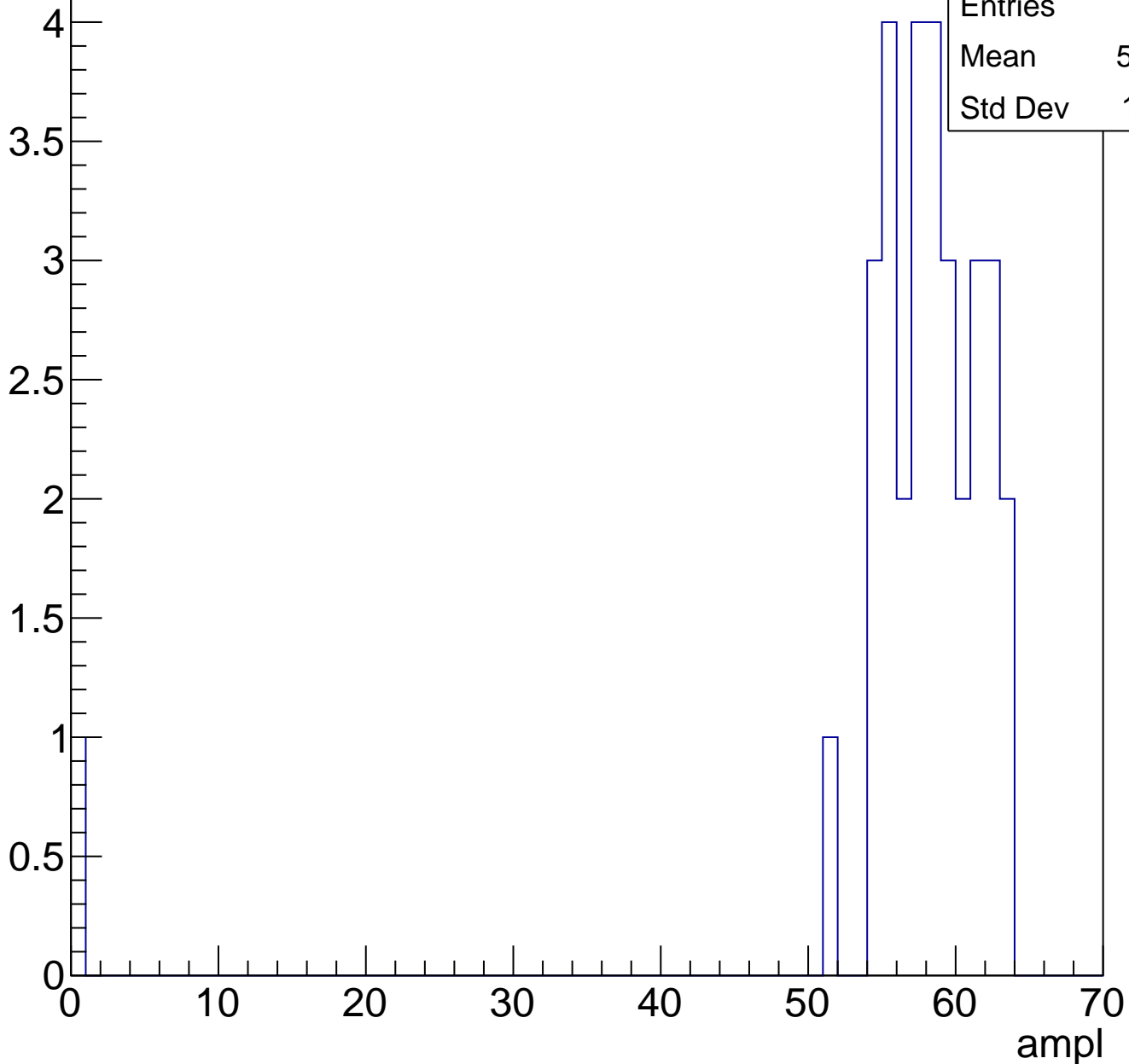
Entries	30
Mean	48.97
Std Dev	13.53



B1L103S, U14-ch28, adc5

calib_packv5_041523_1651.root, FC#0, port C2

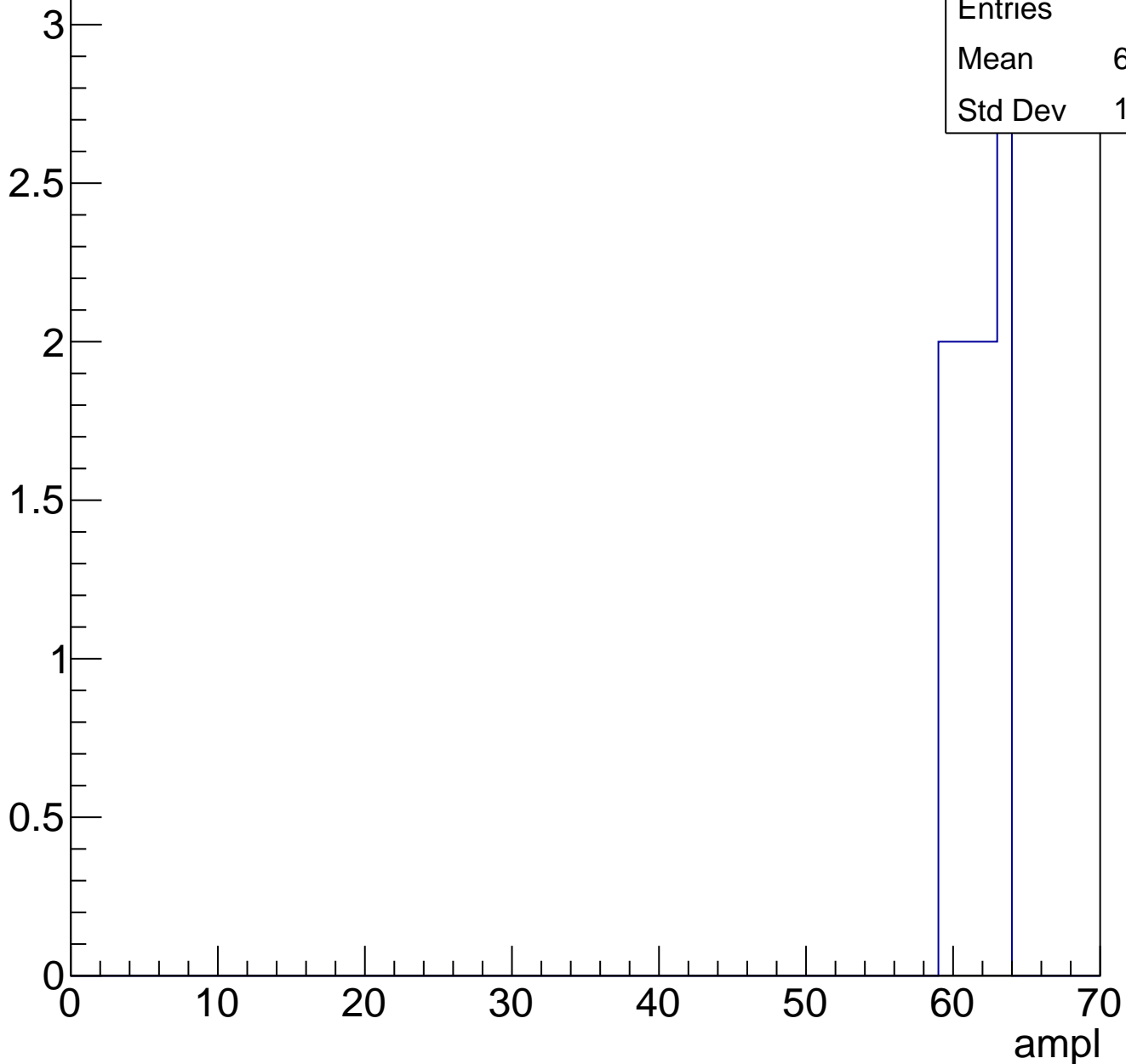
Entry



B1L103S, U14-ch28, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch28, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

12
10
8
6
4
2
0

Entries	12
Mean	0
Std Dev	0

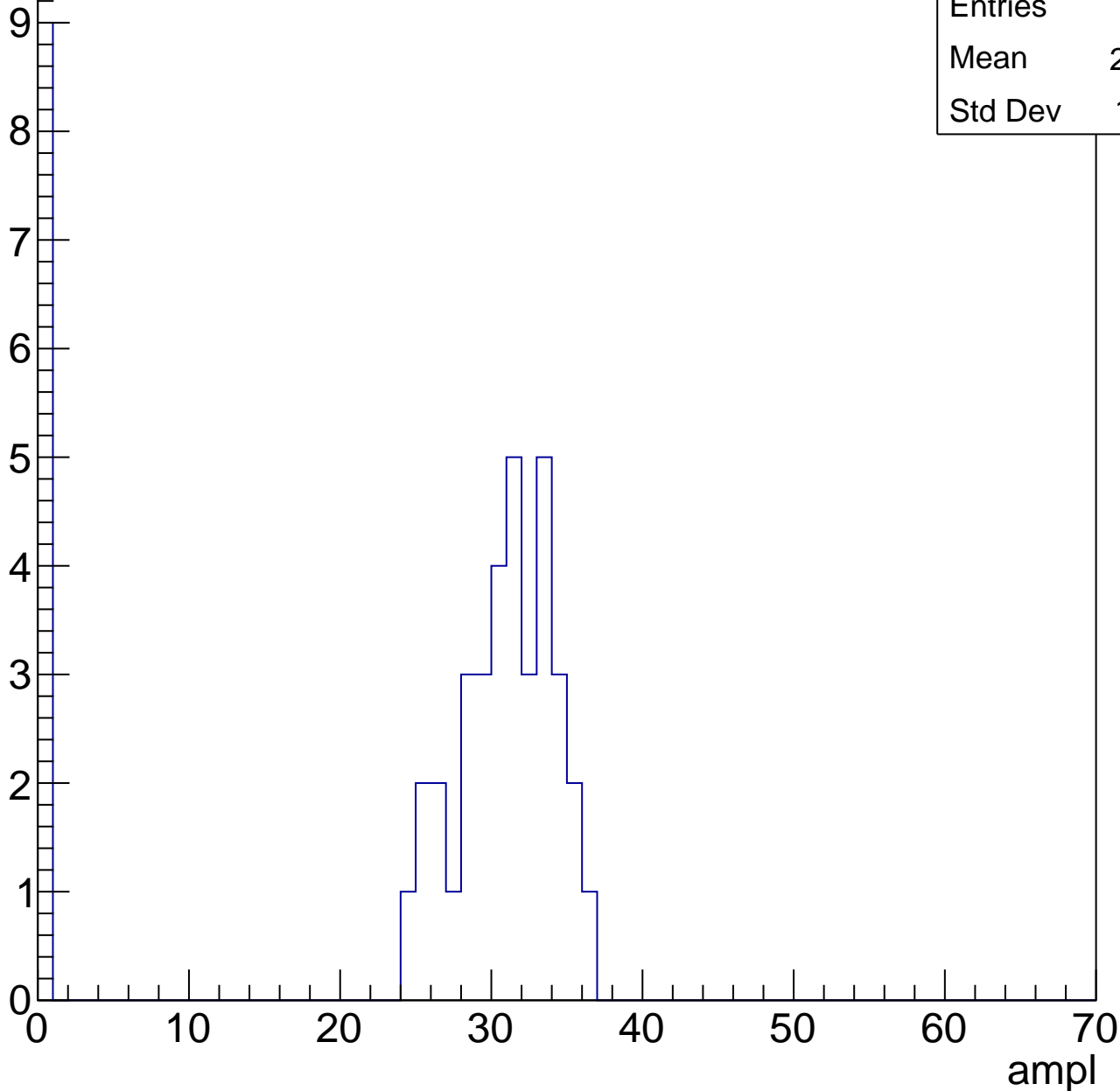
ampl

B1L103S, U14-ch29, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	44
Mean	24.27
Std Dev	12.61

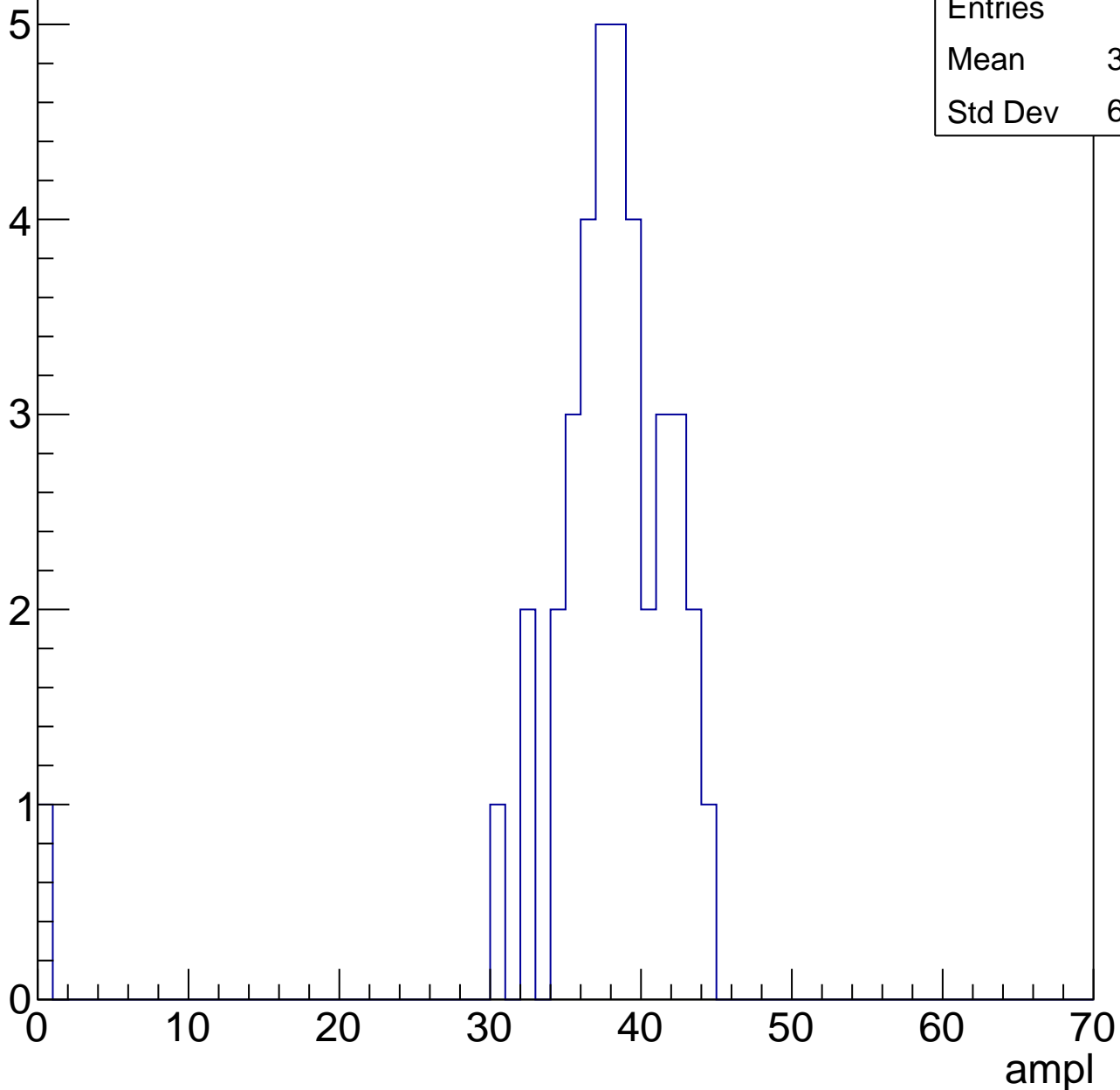


B1L103S, U14-ch29, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	38
Mean	36.87
Std Dev	6.852

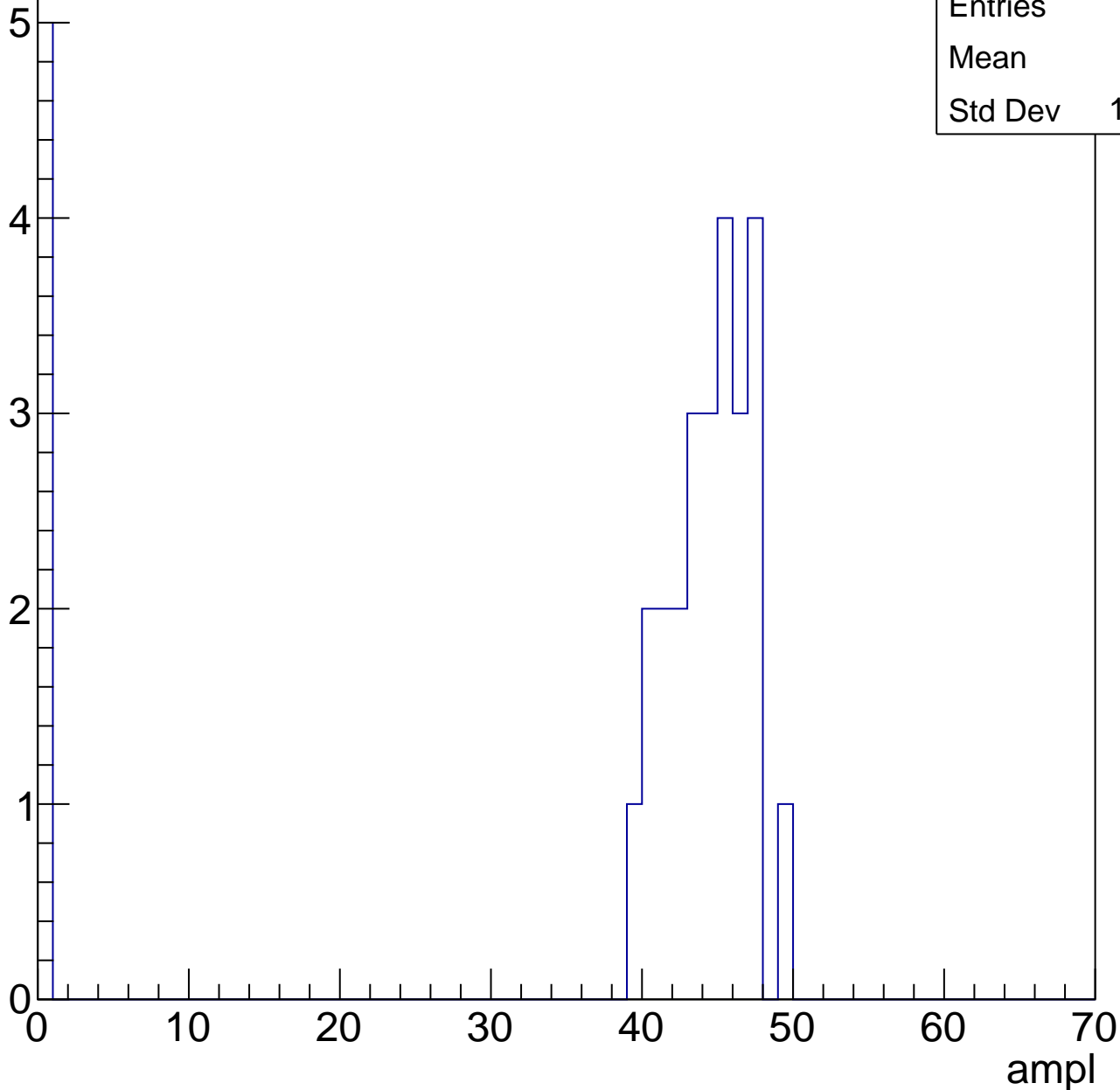


B1L103S, U14-ch29, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	30
Mean	36.7
Std Dev	16.58

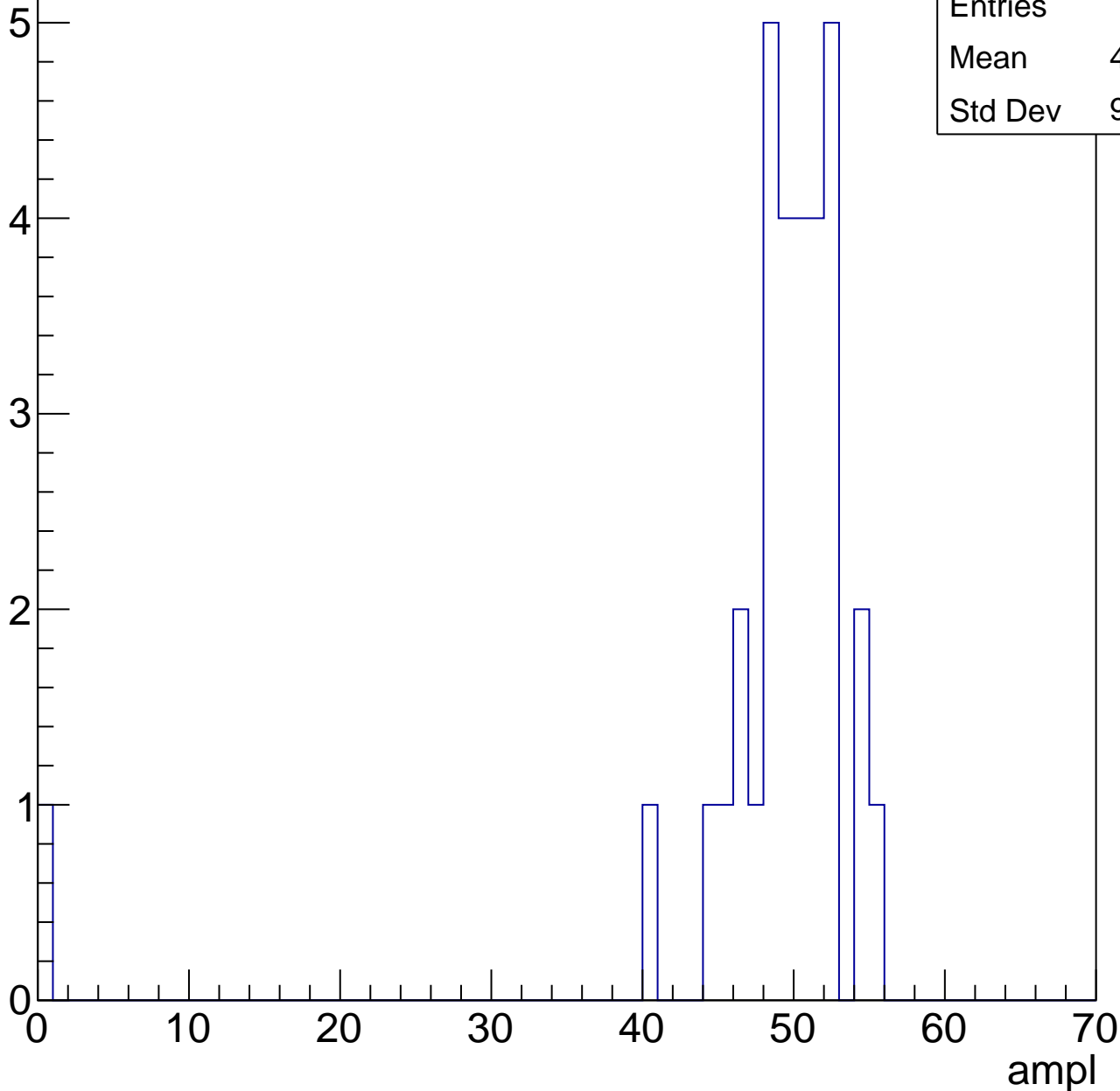


B1L103S, U14-ch29, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	32
Mean	47.84
Std Dev	9.114

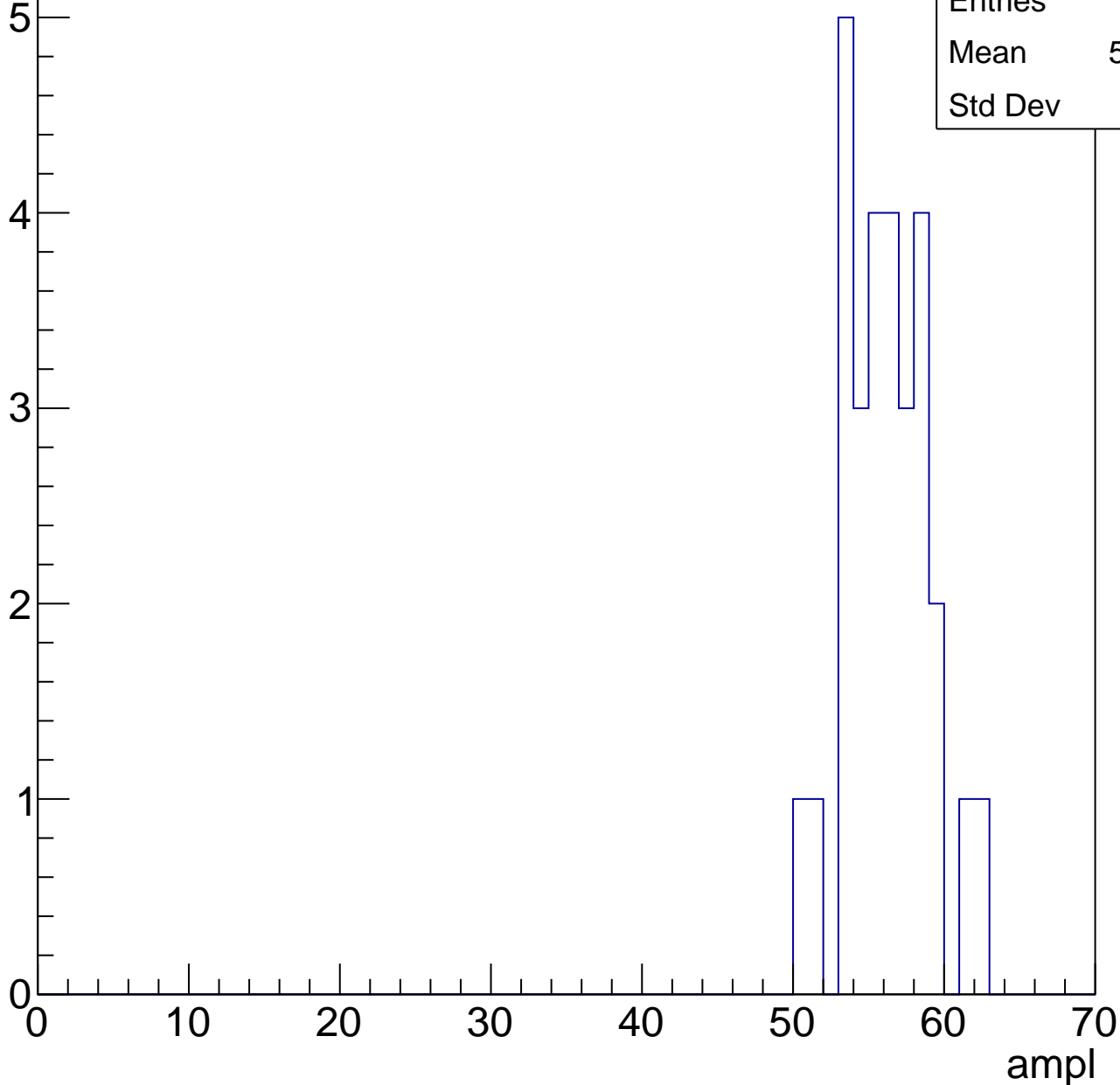


B1L103S, U14-ch29, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	29
Mean	55.72
Std Dev	2.74



B1L103S, U14-ch29, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

5

4

3

2

1

0

Entries	23
Mean	60.35
Std Dev	2.013

ampl

0

10

20

30

40

50

60

70

B1L103S, U14-ch29, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch29, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

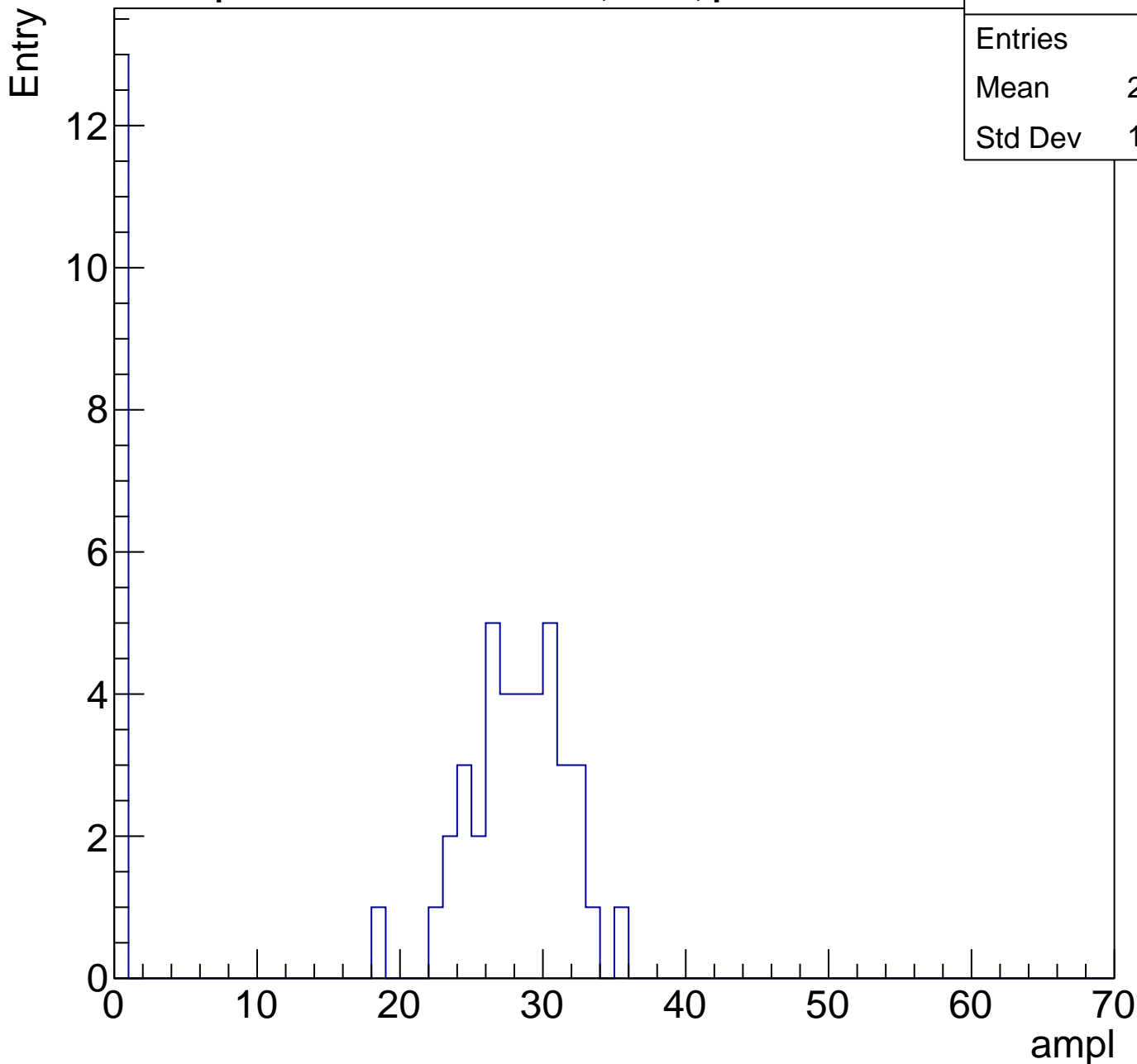
ampl

Entries	10
Mean	0
Std Dev	0

B1L103S, U14-ch30, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	52
Mean	20.79
Std Dev	12.35

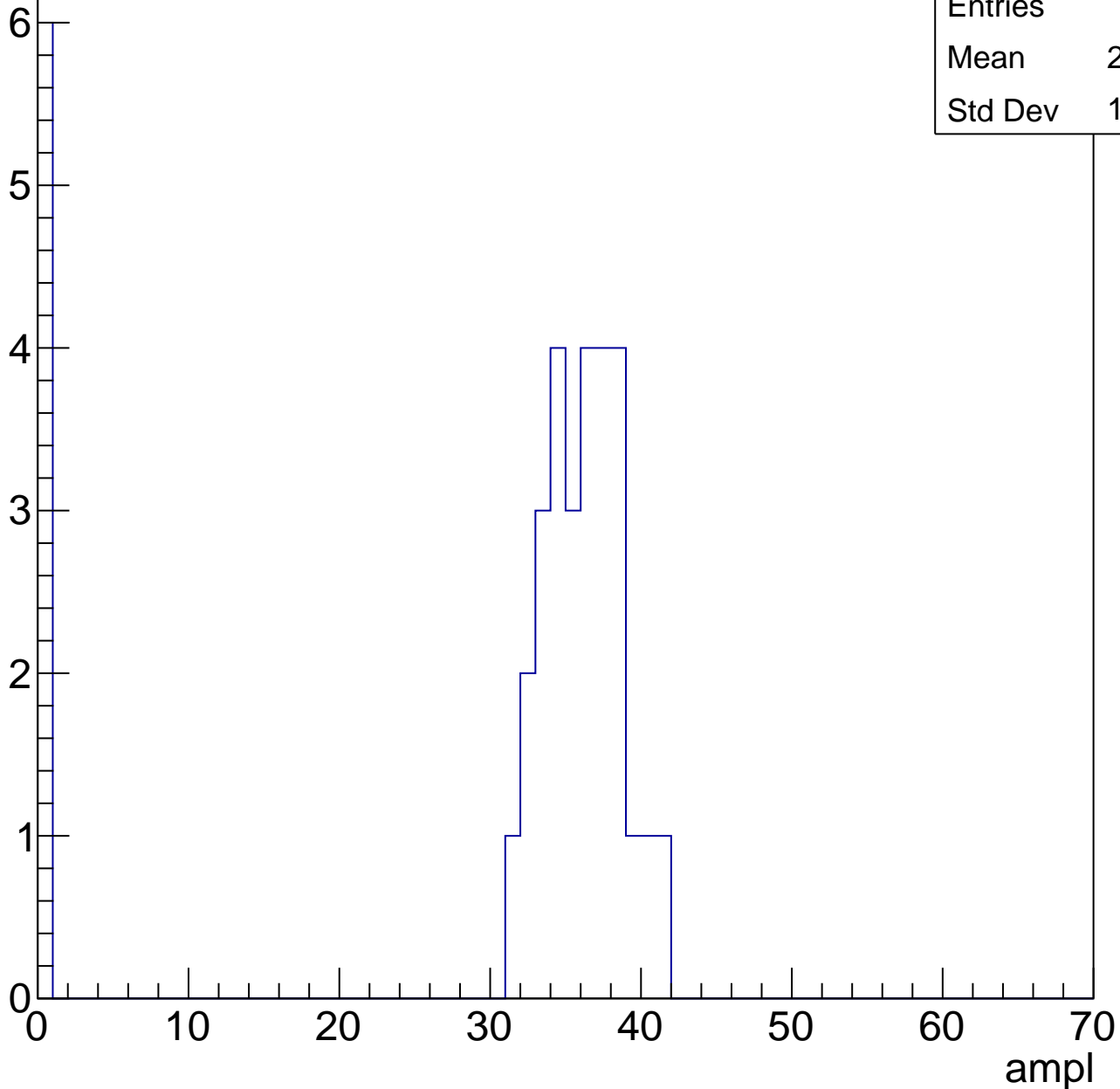


B1L103S, U14-ch30, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

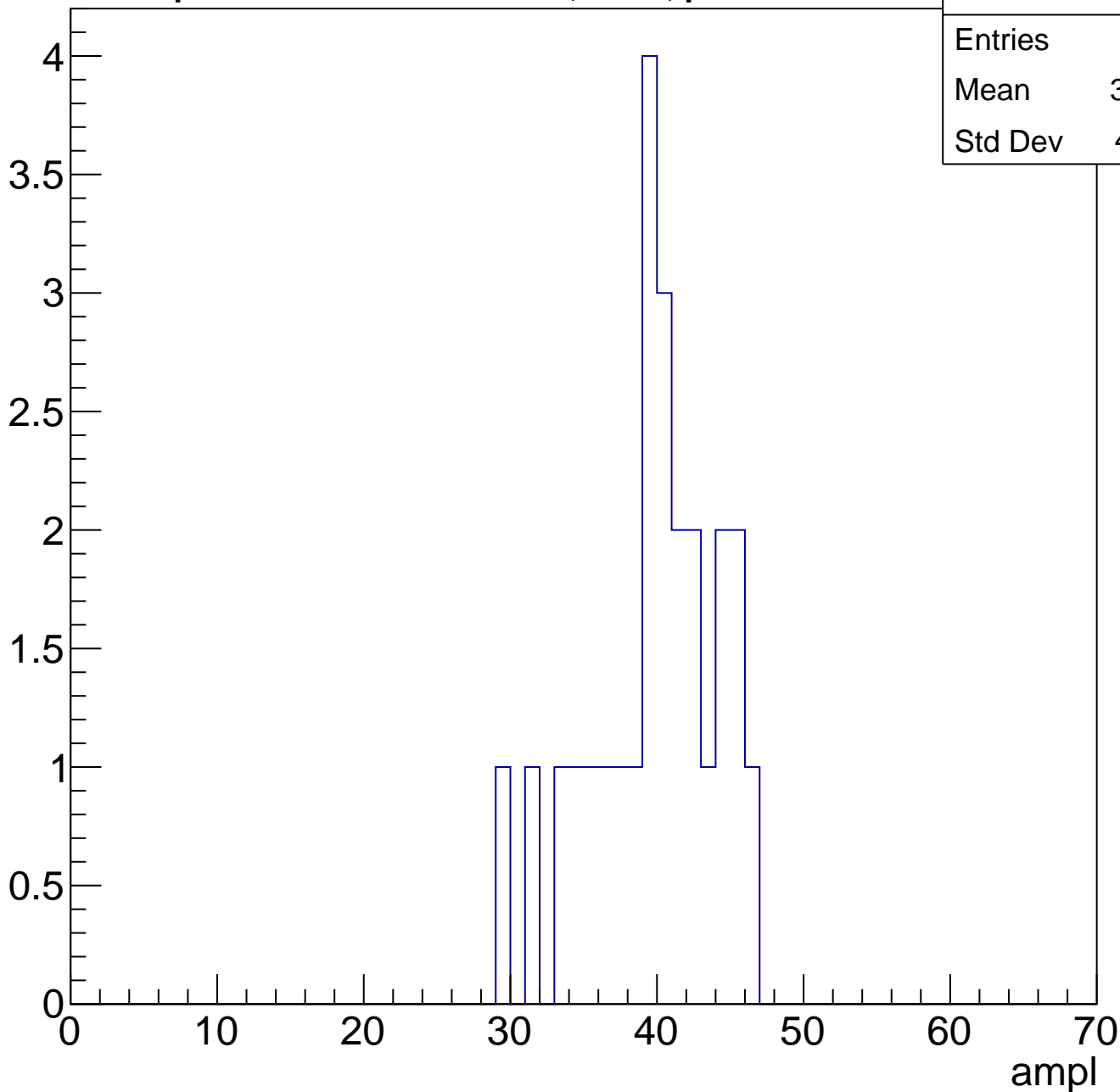
Entries	34
Mean	29.38
Std Dev	13.78



B1L103S, U14-ch30, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry



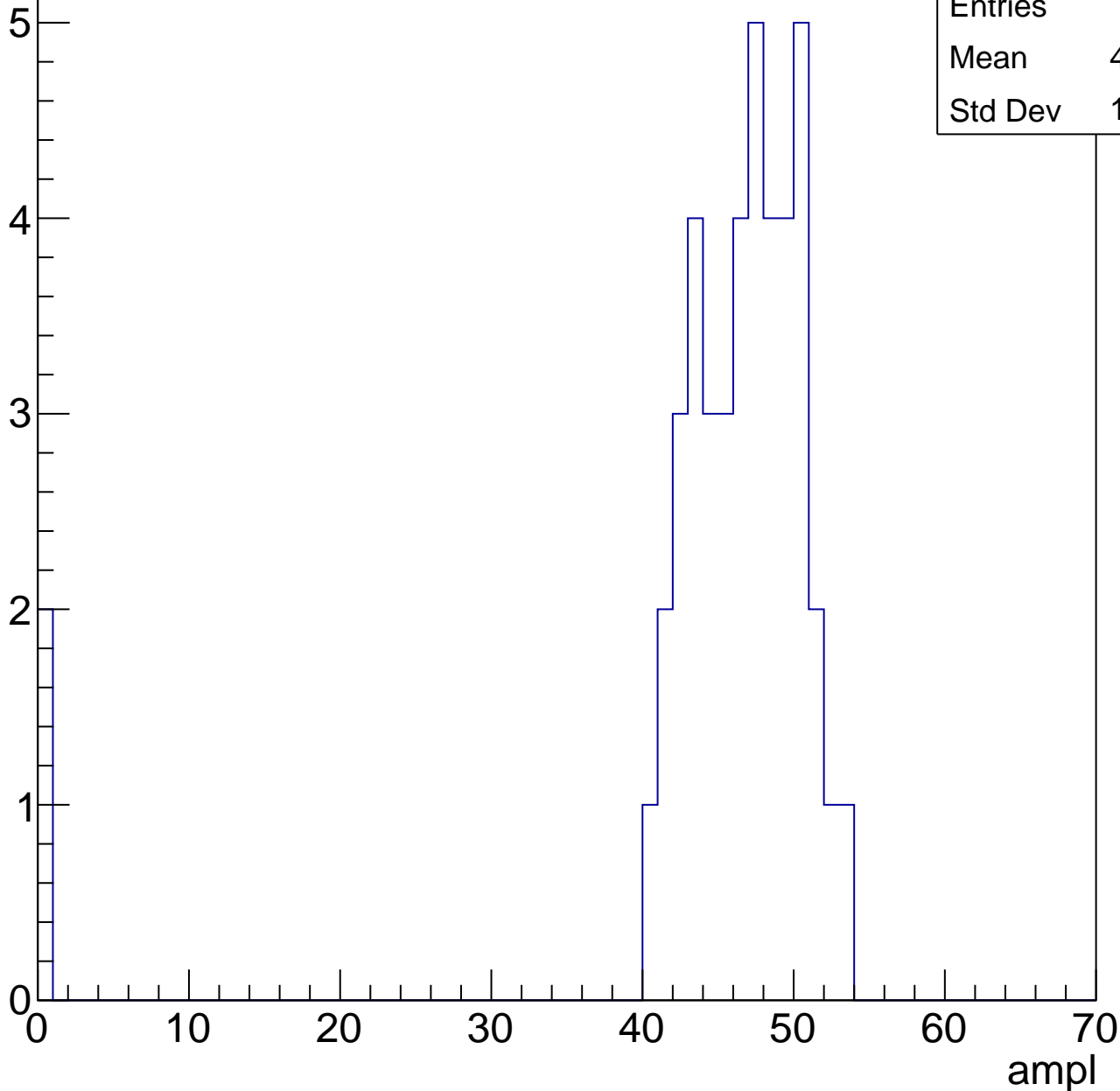
Entries	25
Mean	39.28
Std Dev	4.331

B1L103S, U14-ch30, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

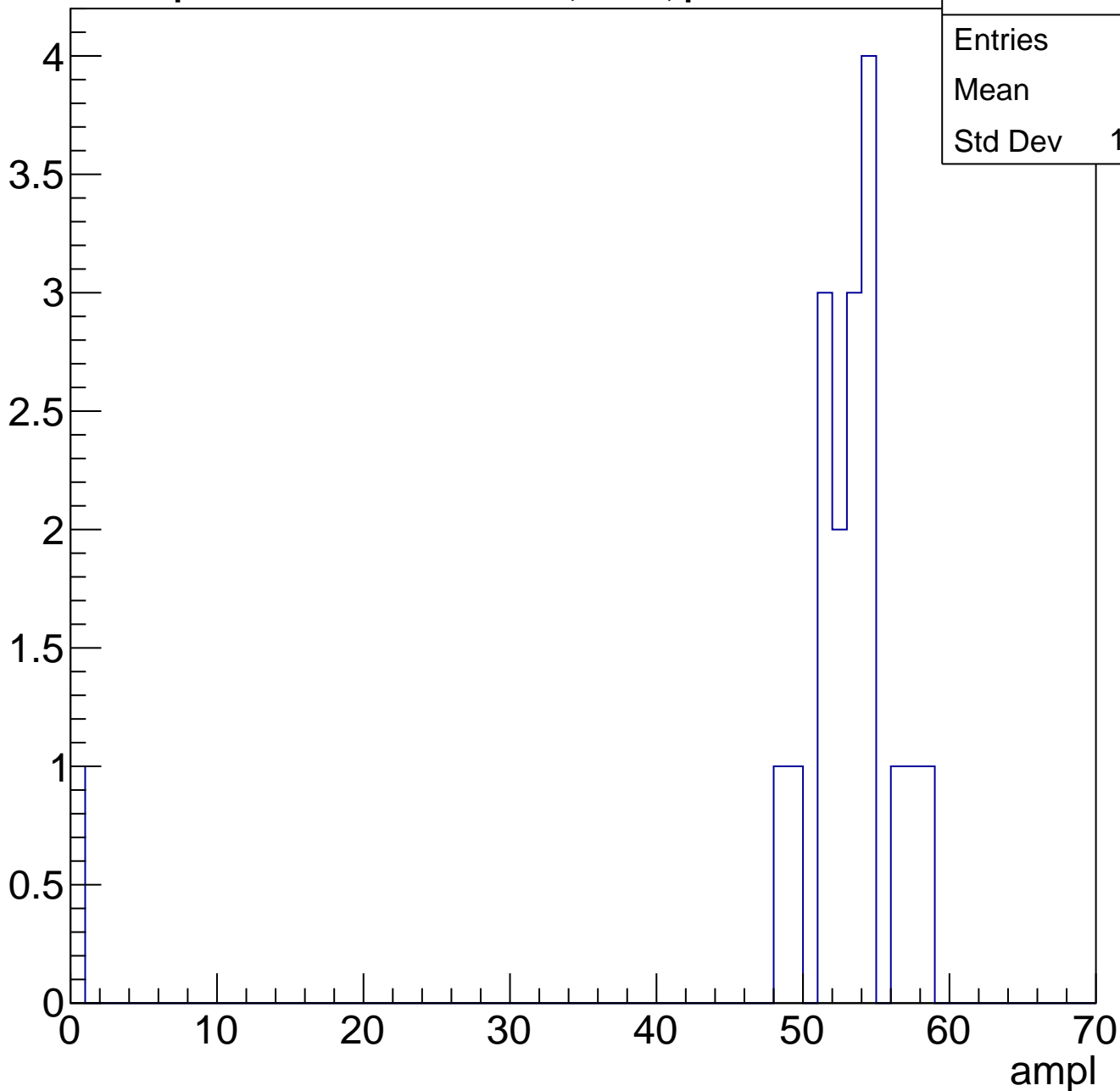
Entries	44
Mean	44.34
Std Dev	10.19



B1L103S, U14-ch30, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

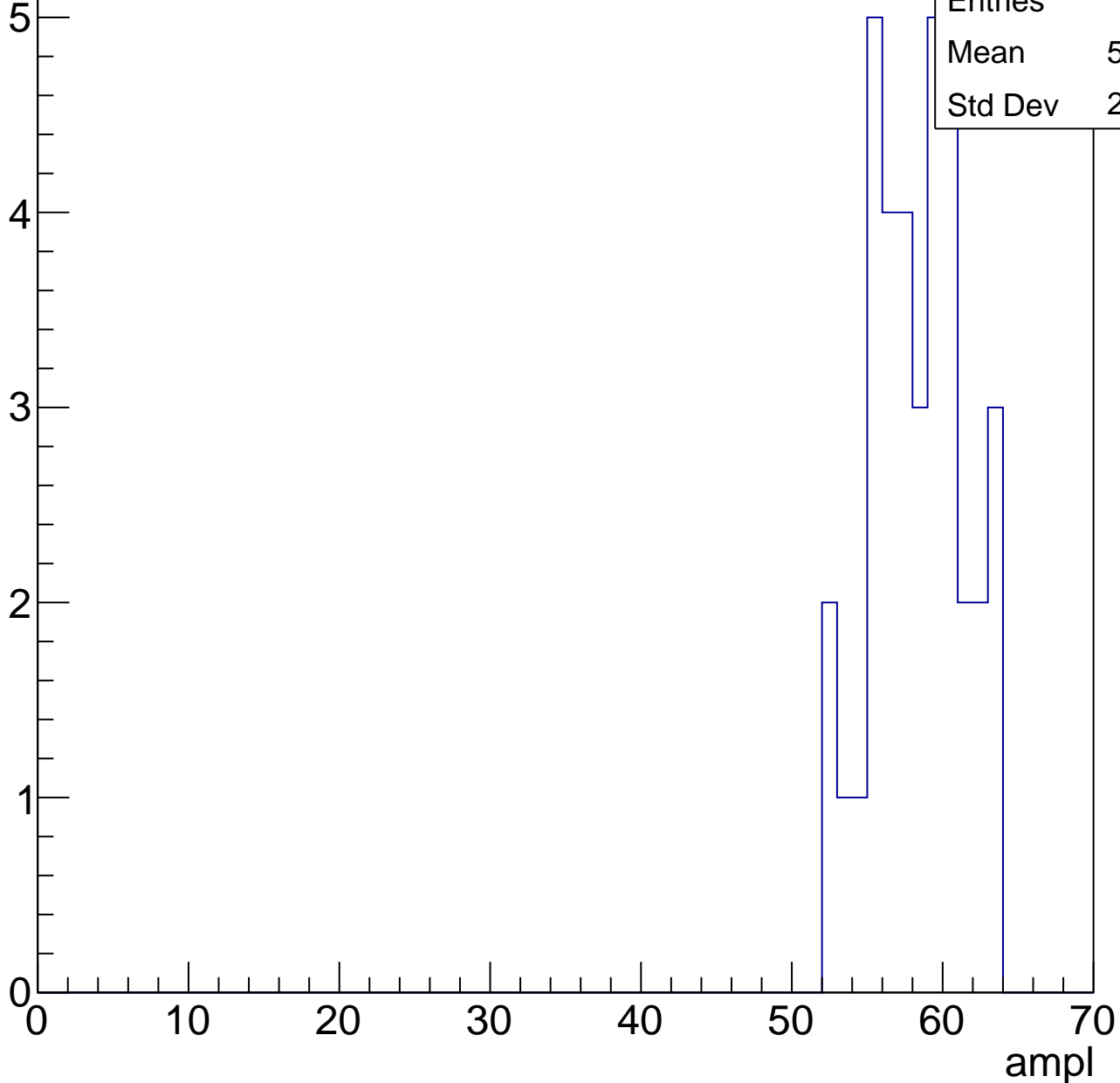


B1L103S, U14-ch30, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

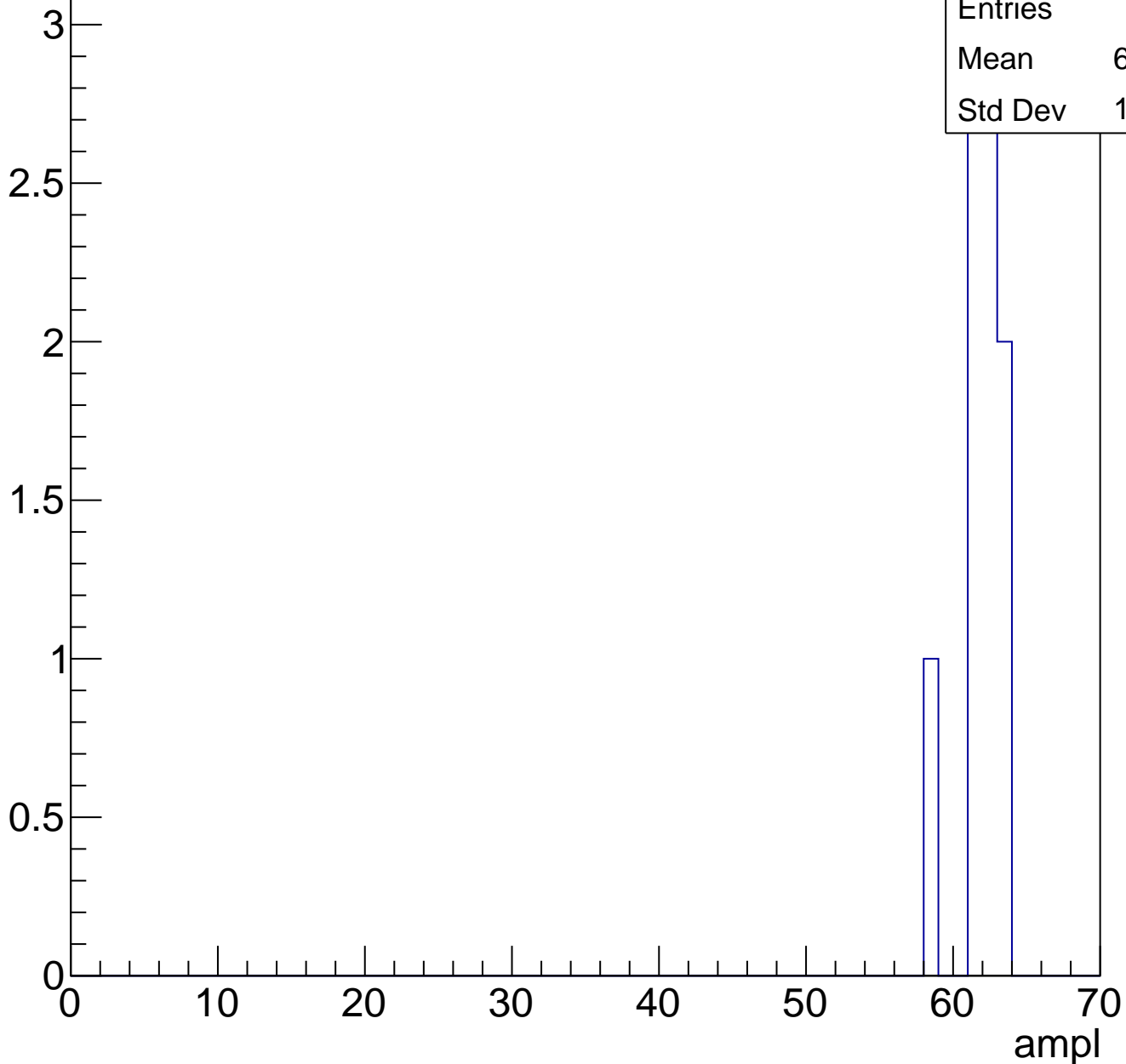
Entries	37
Mean	57.89
Std Dev	2.975



B1L103S, U14-ch30, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

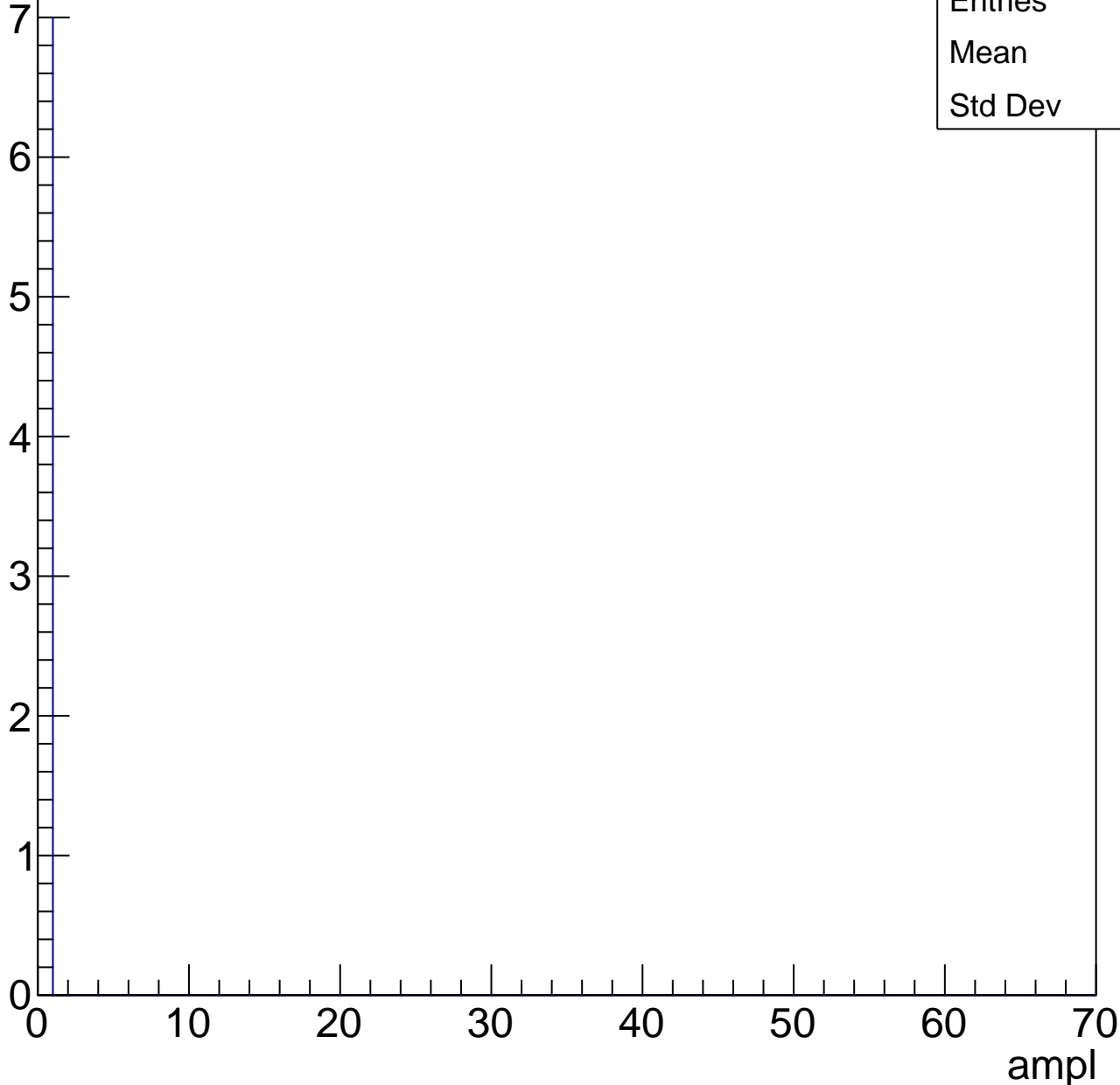


B1L103S, U14-ch30, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	7
Mean	0
Std Dev	0



B1L103S, U14-ch31, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	47
Mean	21.34
Std Dev	13.52

Entry

12

10

8

6

4

2

0

0

10

20

30

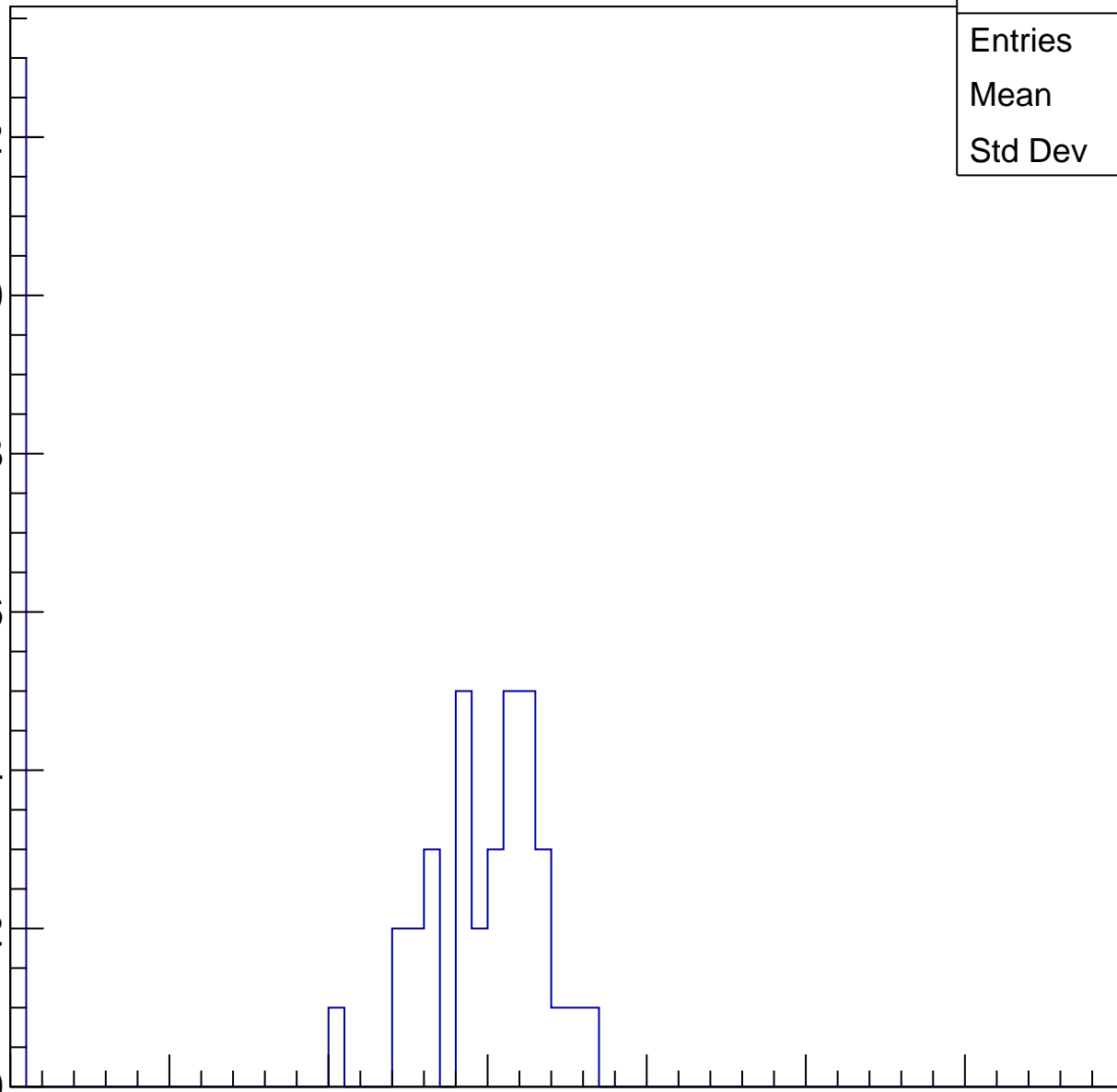
40

50

60

70

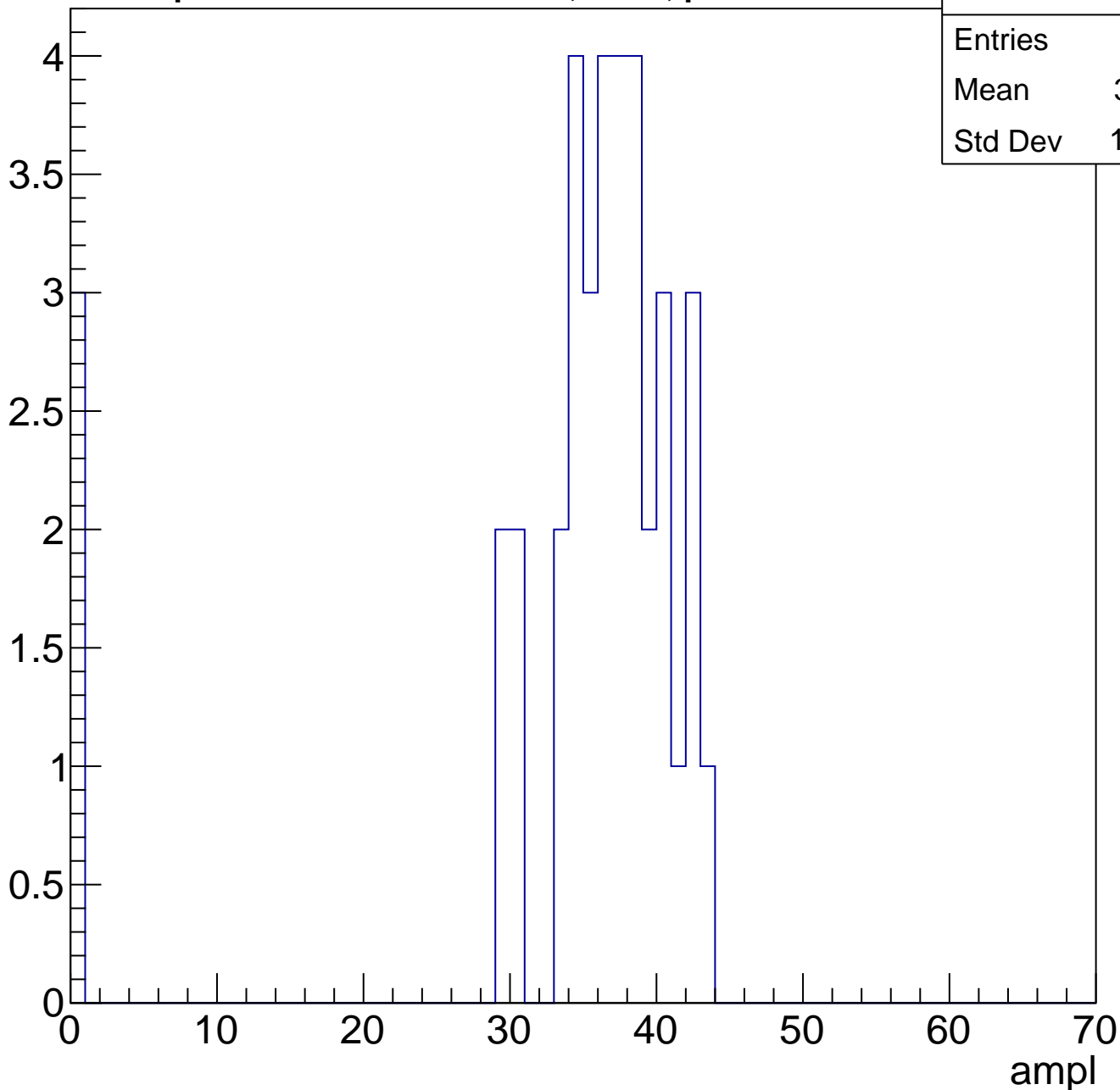
ampl



B1L103S, U14-ch31, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry



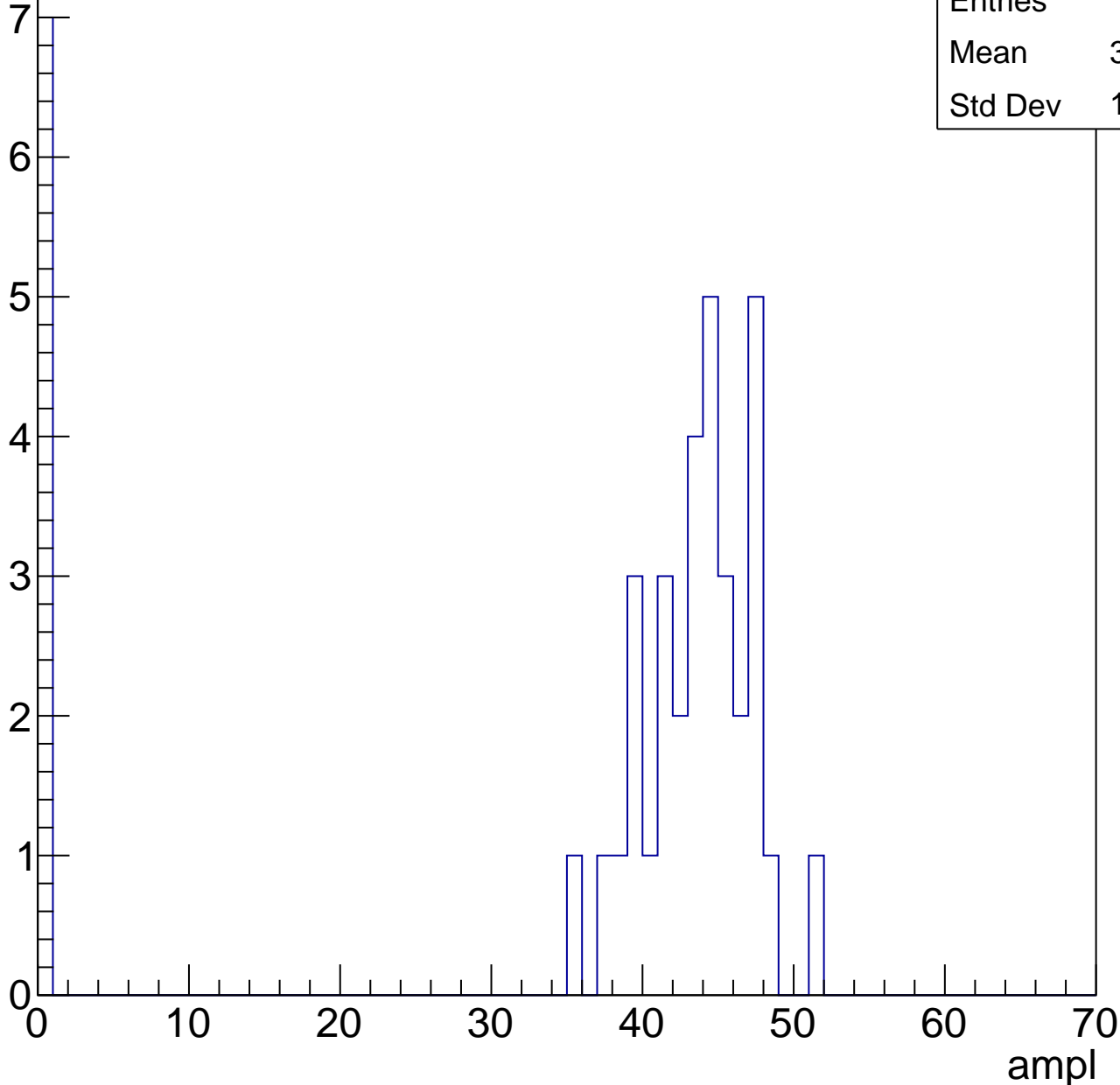
Entries	38
Mean	33.61
Std Dev	10.44

B1L103S, U14-ch31, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

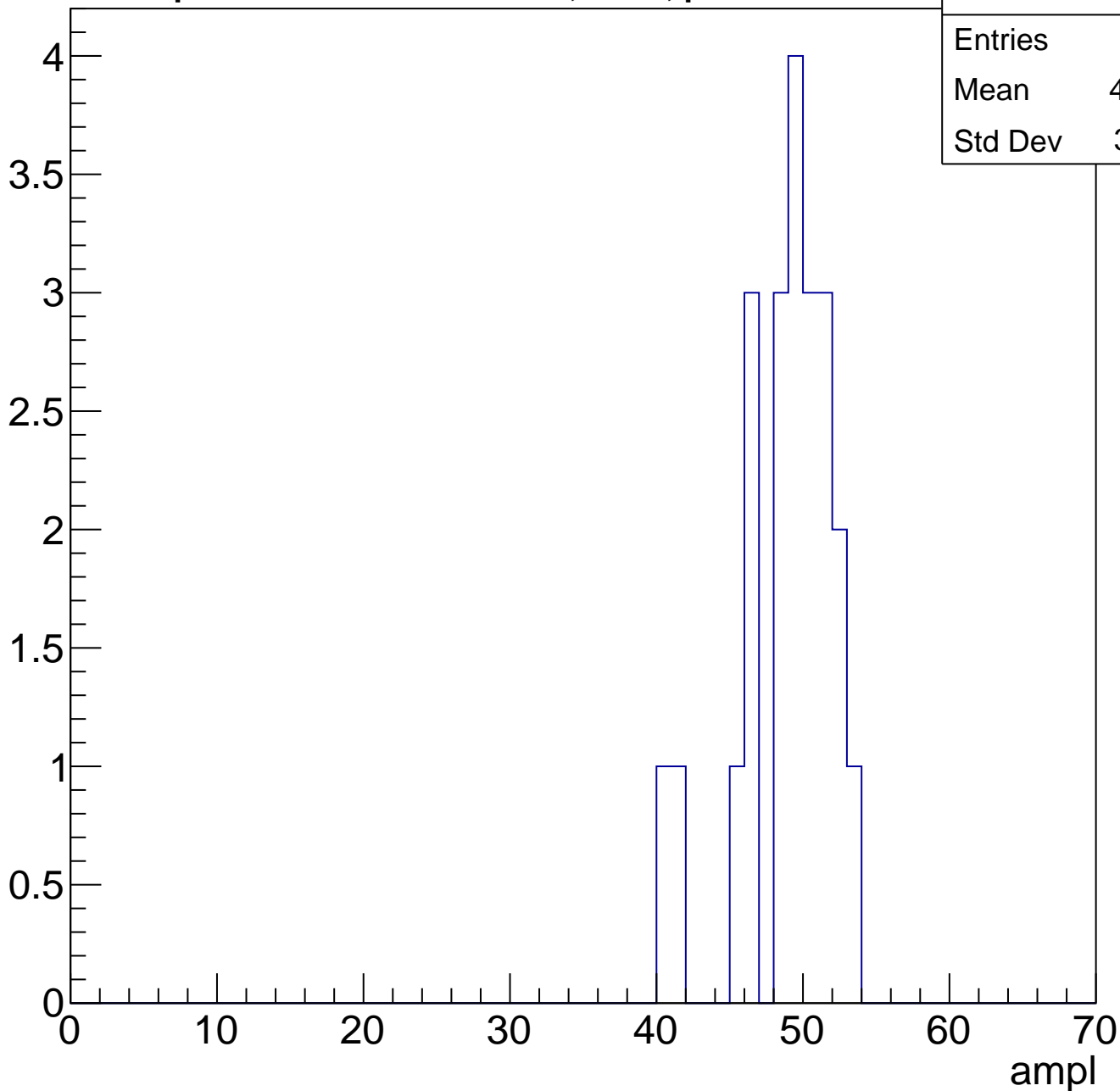
Entries	40
Mean	35.67
Std Dev	16.73



B1L103S, U14-ch31, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry



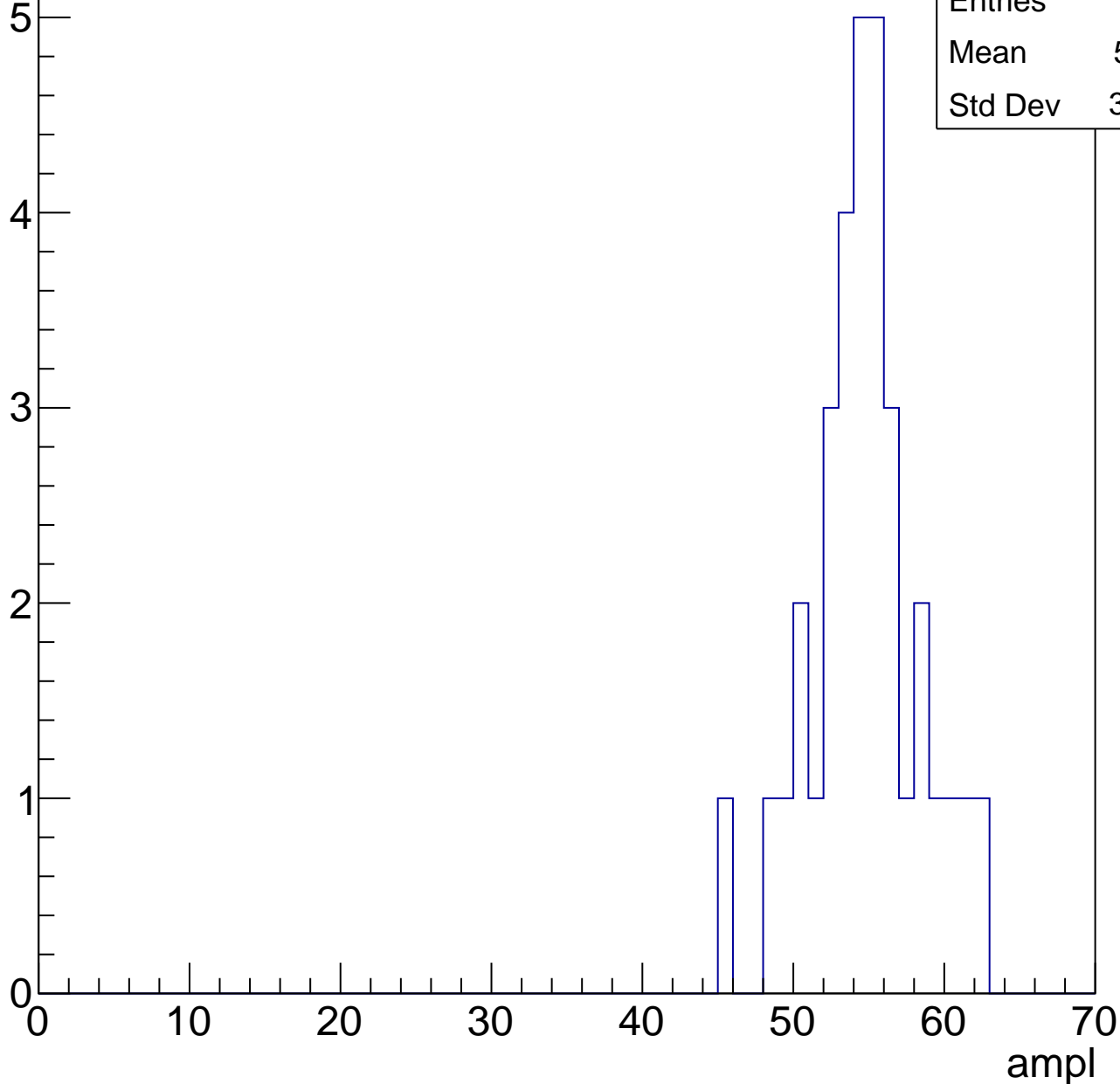
Entries	22
Mean	48.36
Std Dev	3.241

B1L103S, U14-ch31, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

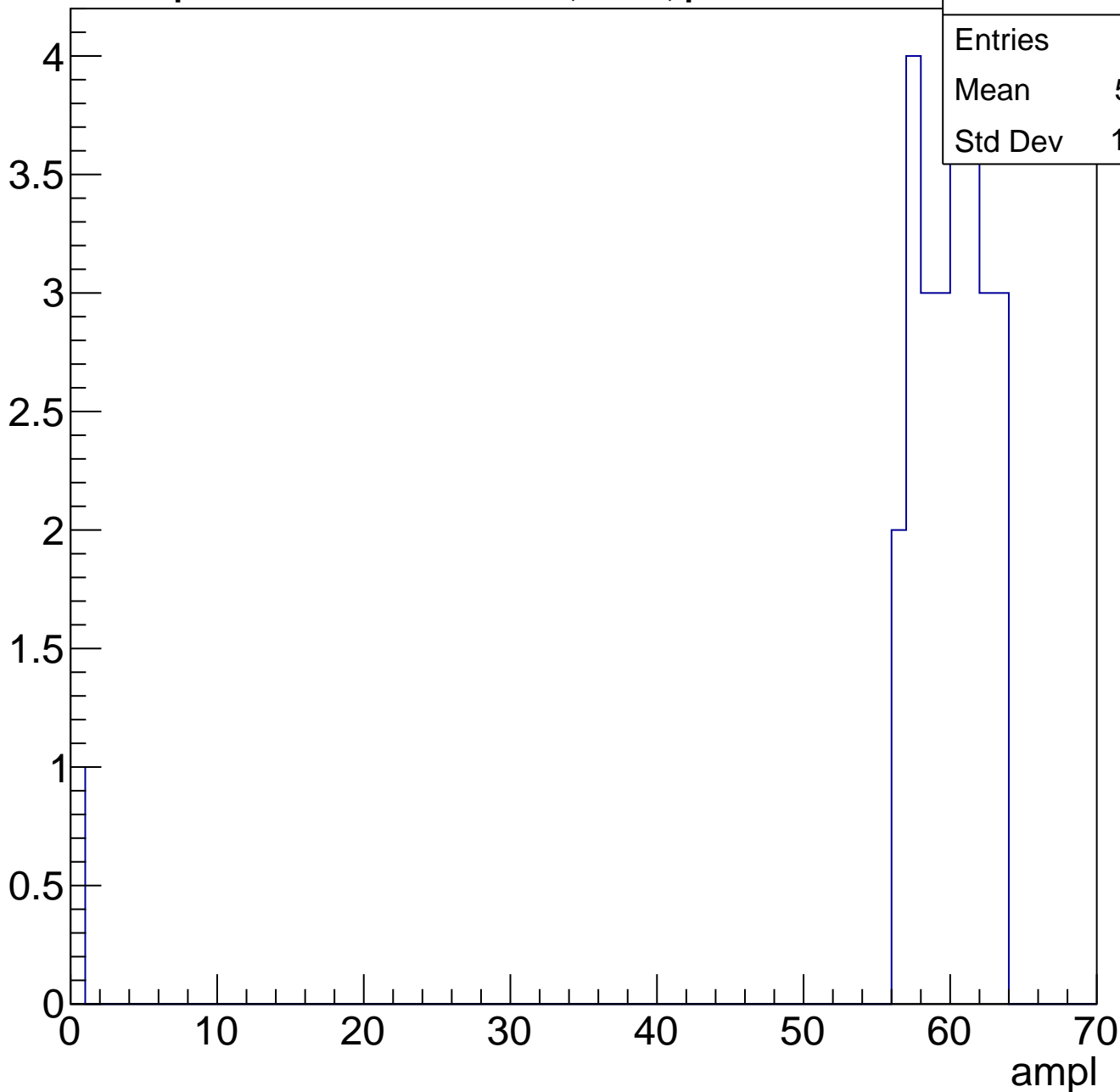
Entries	33
Mean	54.21
Std Dev	3.608



B1L103S, U14-ch31, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch31, adc6

calib_packv5_041523_1651.root, FC#0, port C2

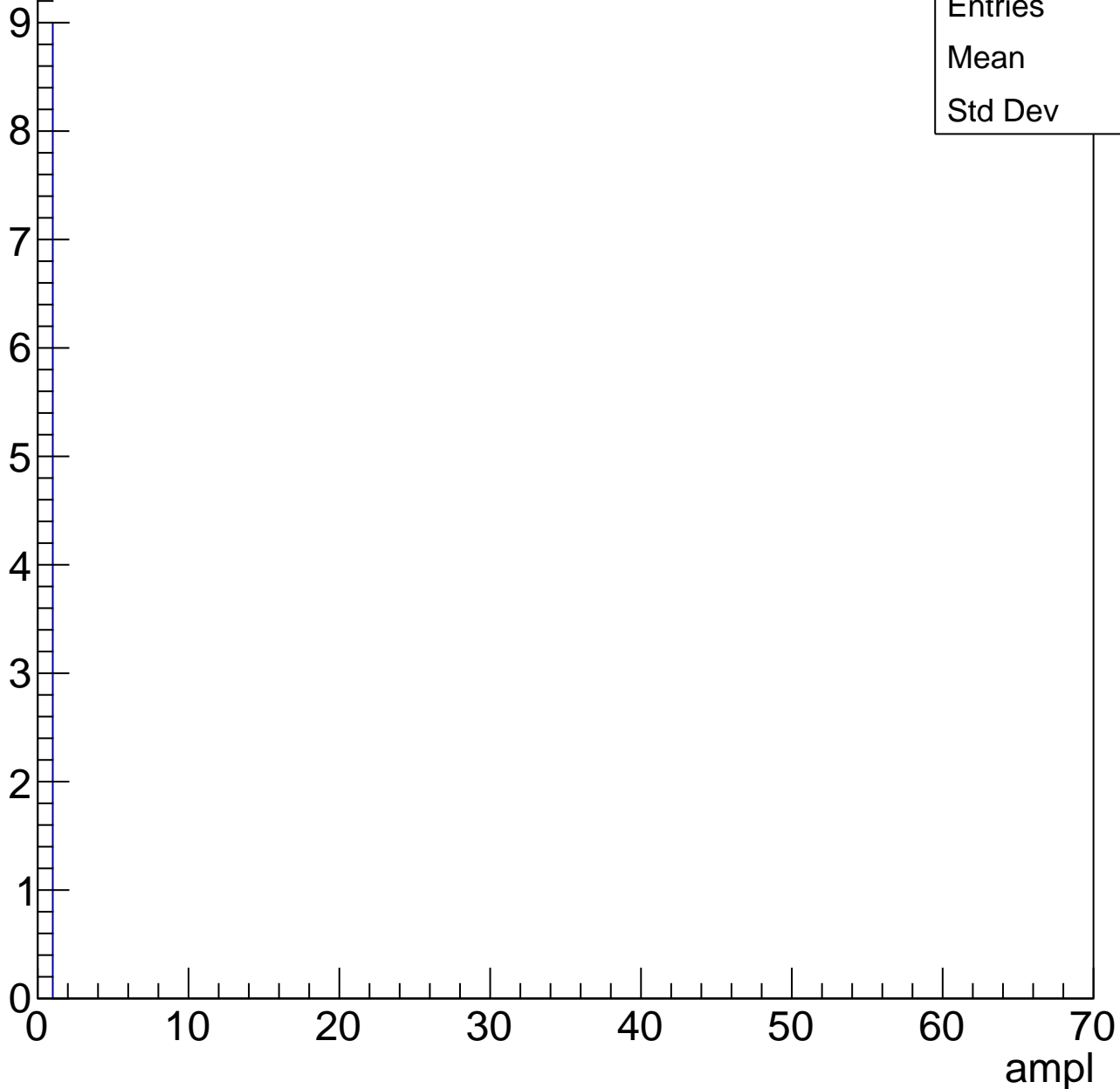
Entry



B1L103S, U14-ch31, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

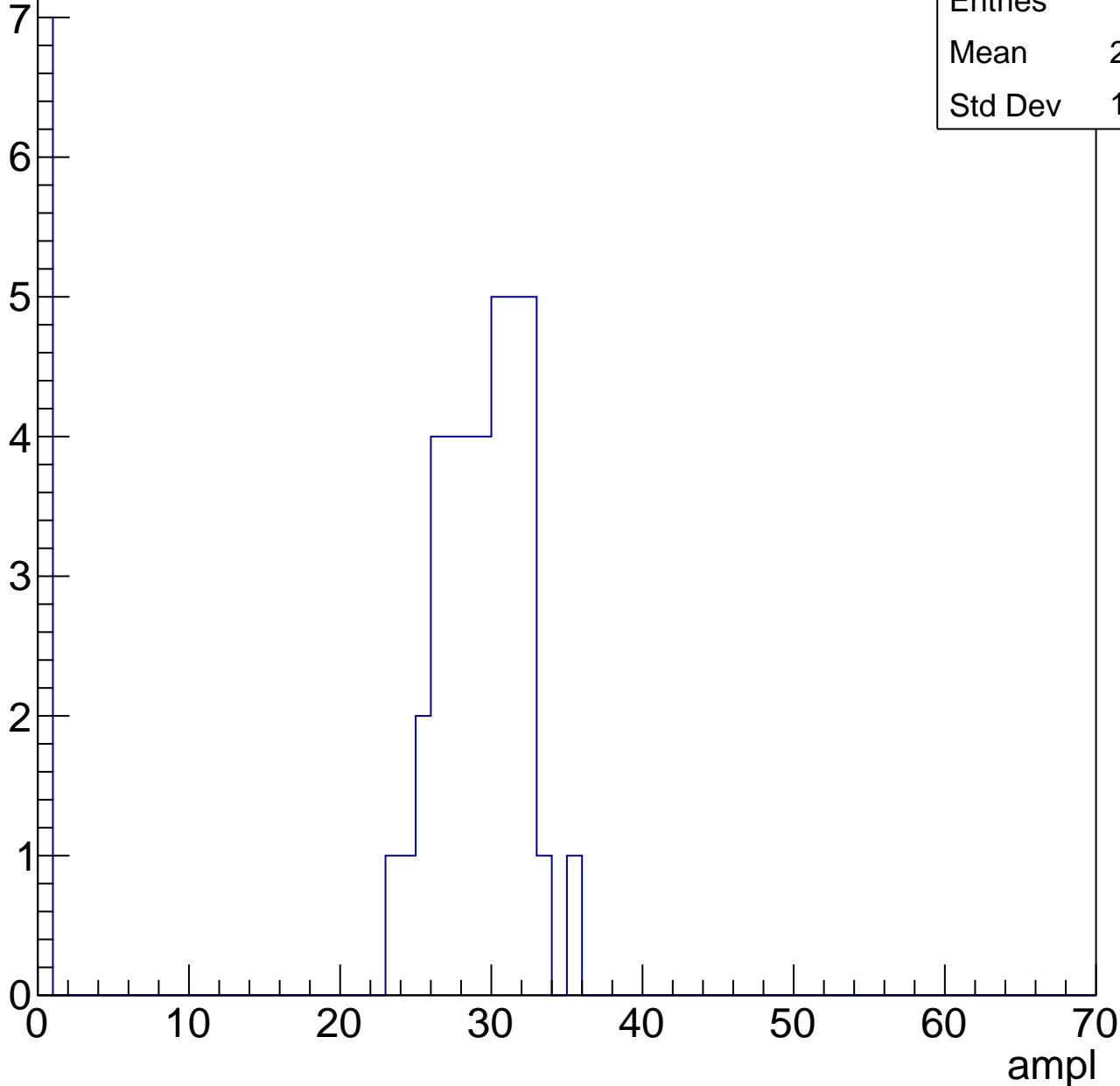


B1L103S, U14-ch32, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	44
Mean	24.32
Std Dev	10.86

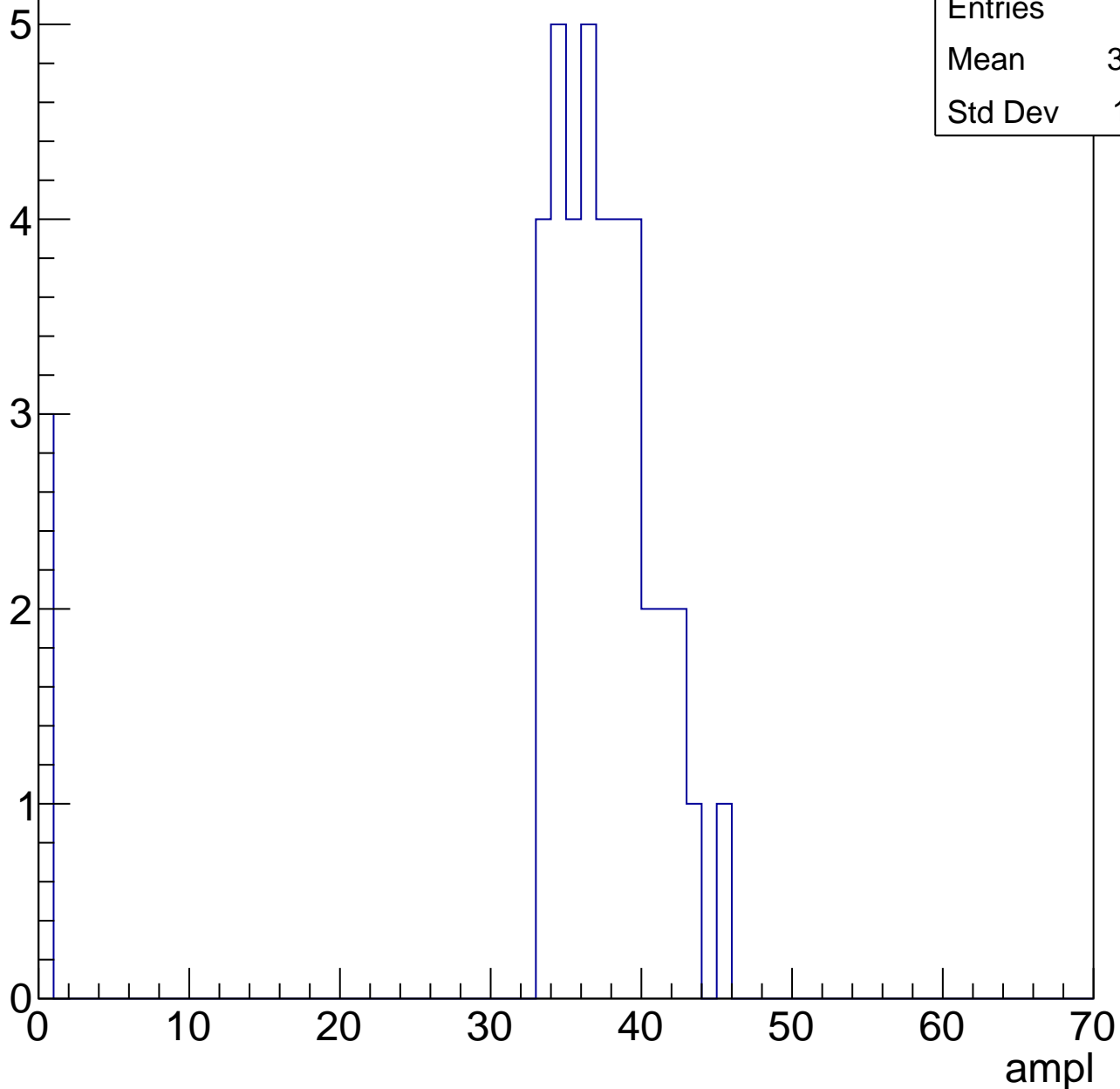


B1L103S, U14-ch32, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

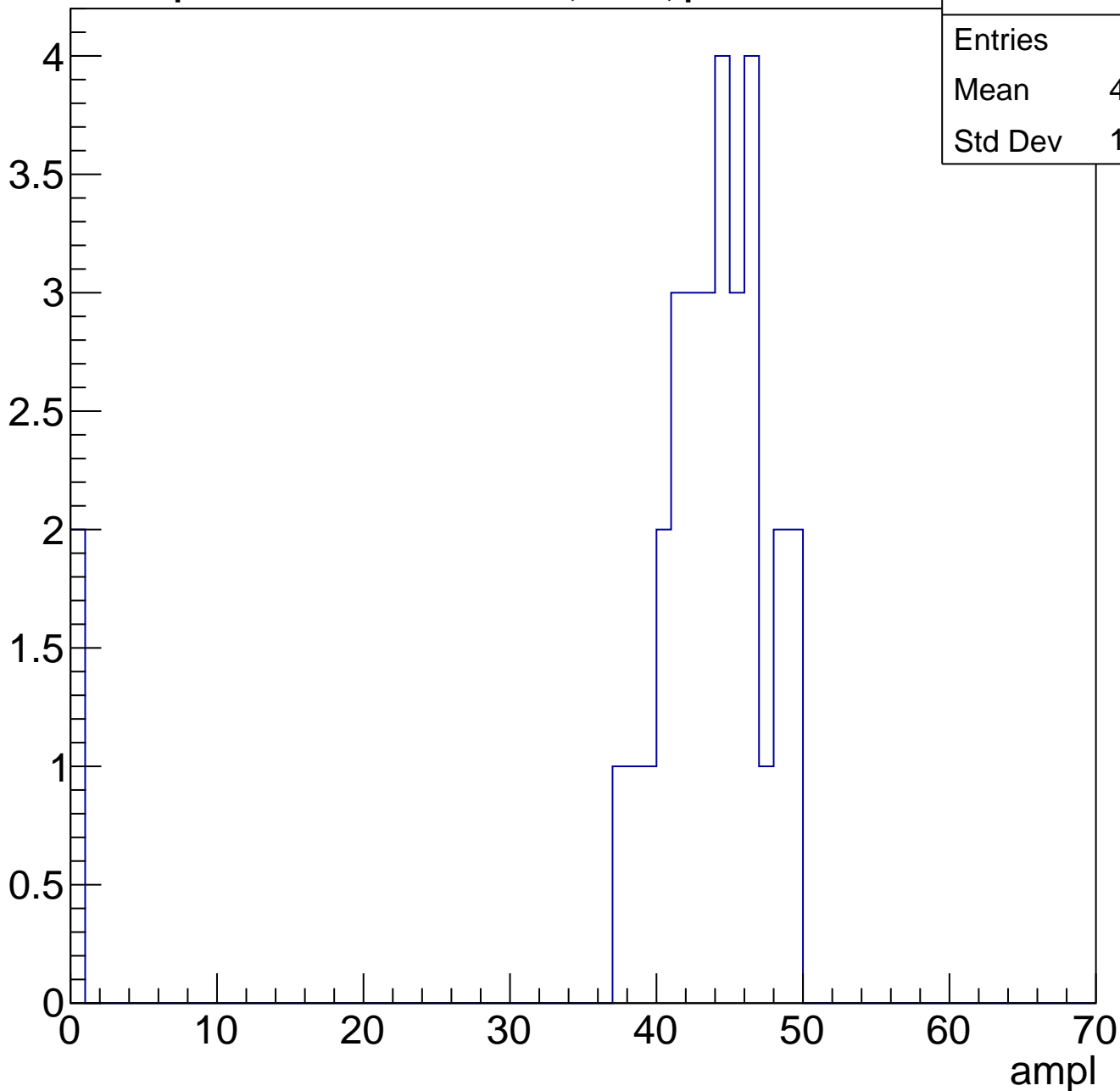
Entries	41
Mean	34.44
Std Dev	10.11



B1L103S, U14-ch32, adc2

calib_packv5_041523_1651.root, FC#0, port C2

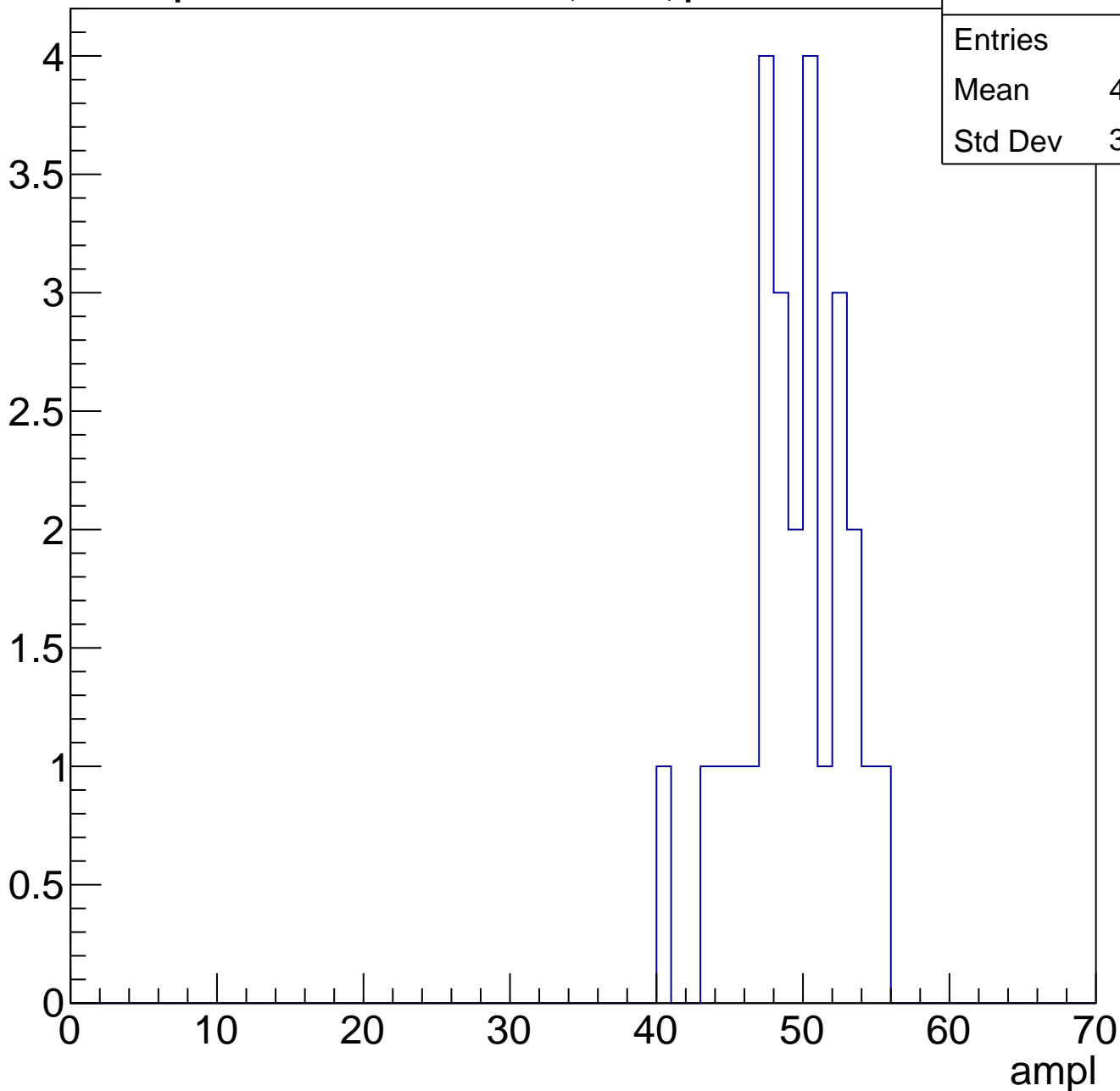
Entry



B1L103S, U14-ch32, adc3

calib_packv5_041523_1651.root, FC#0, port C2

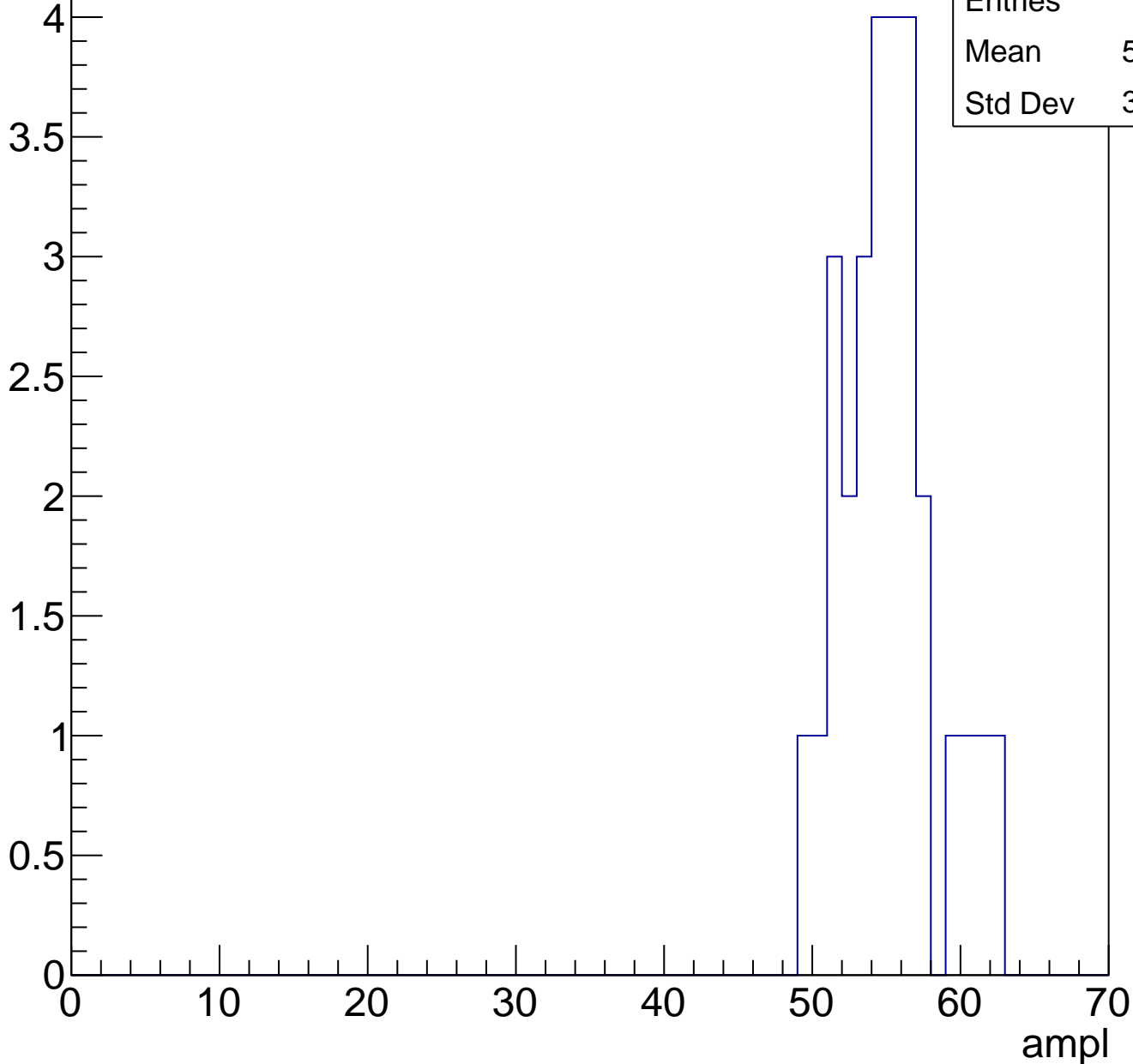
Entry



B1L103S, U14-ch32, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch32, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

5

4

3

2

1

0

Entries	27
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Mean	59.41
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Std Dev	2.614
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ampl

0

10

20

30

40

50

60

70

1

2

3

4

5

B1L103S, U14-ch32, adc6

calib_packv5_041523_1651.root, FC#0, port C2

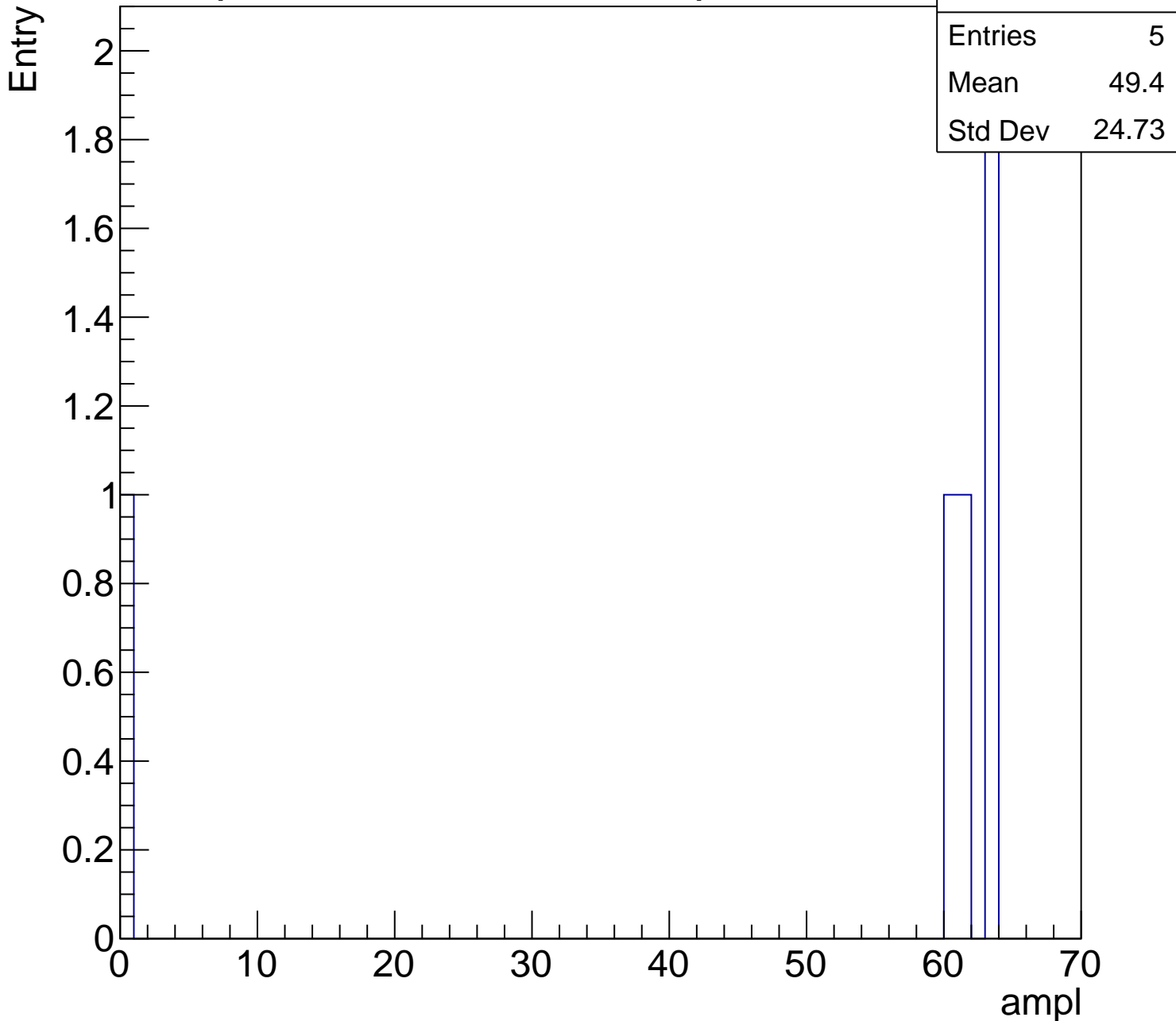
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	5
Mean	49.4
Std Dev	24.73

0 10 20 30 40 50 60 70

ampl



B1L103S, U14-ch32, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

12
10
8
6
4
2
0

Entries	12
Mean	0
Std Dev	0

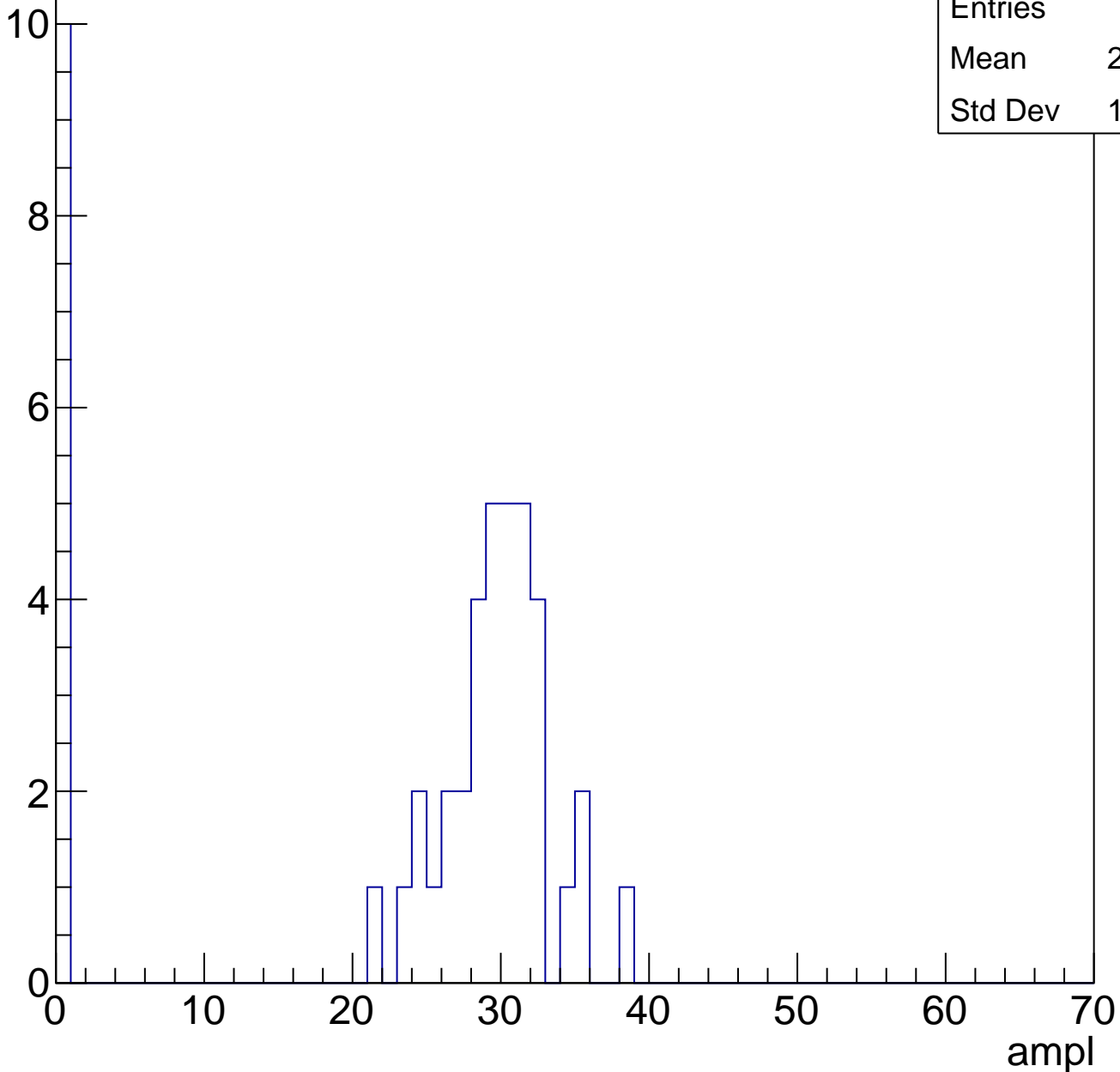
ampl

B1L103S, U14-ch33, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	46
Mean	22.93
Std Dev	12.47

Entry

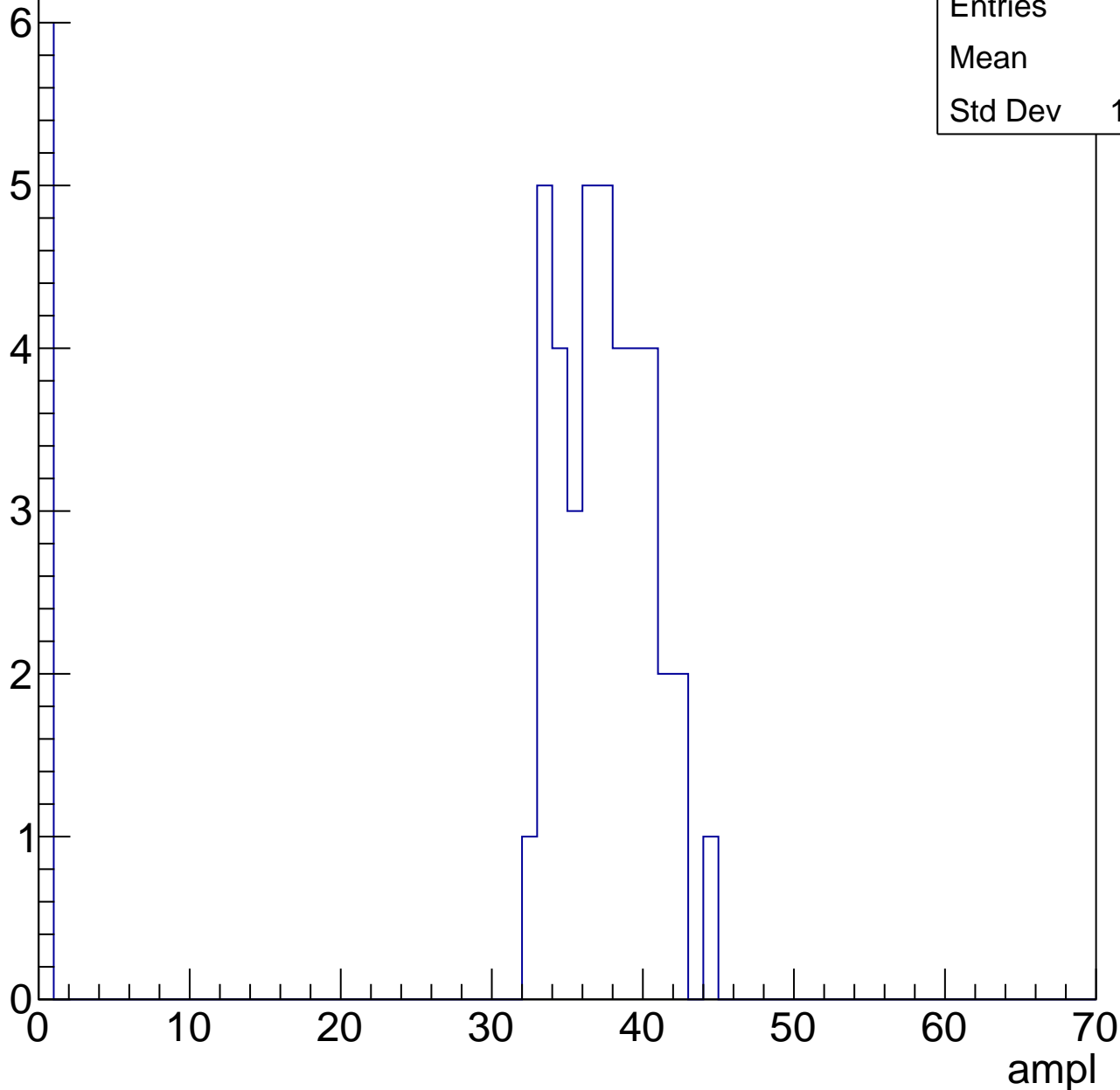


B1L103S, U14-ch33, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

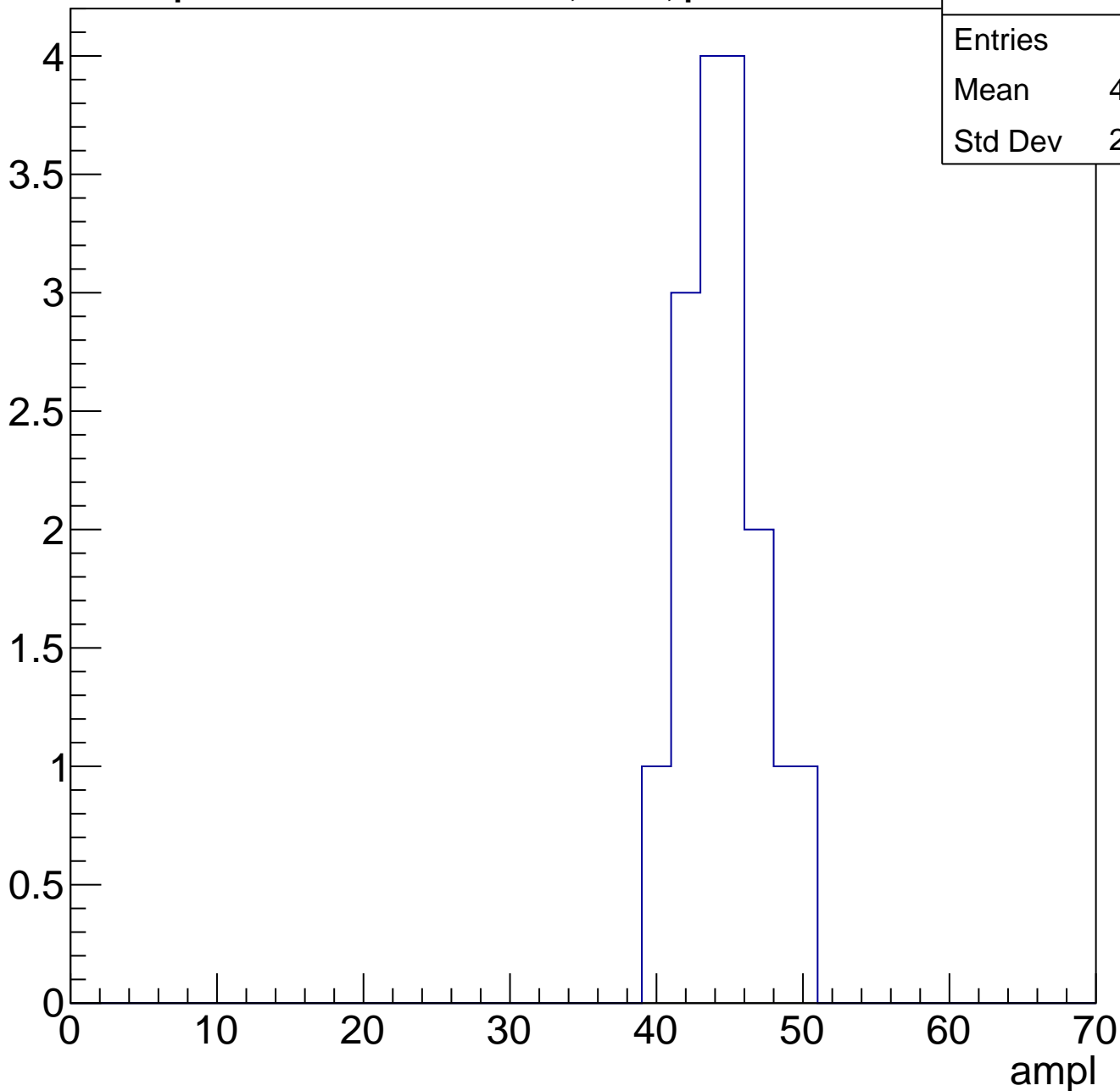
Entries	46
Mean	32.2
Std Dev	12.77



B1L103S, U14-ch33, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry



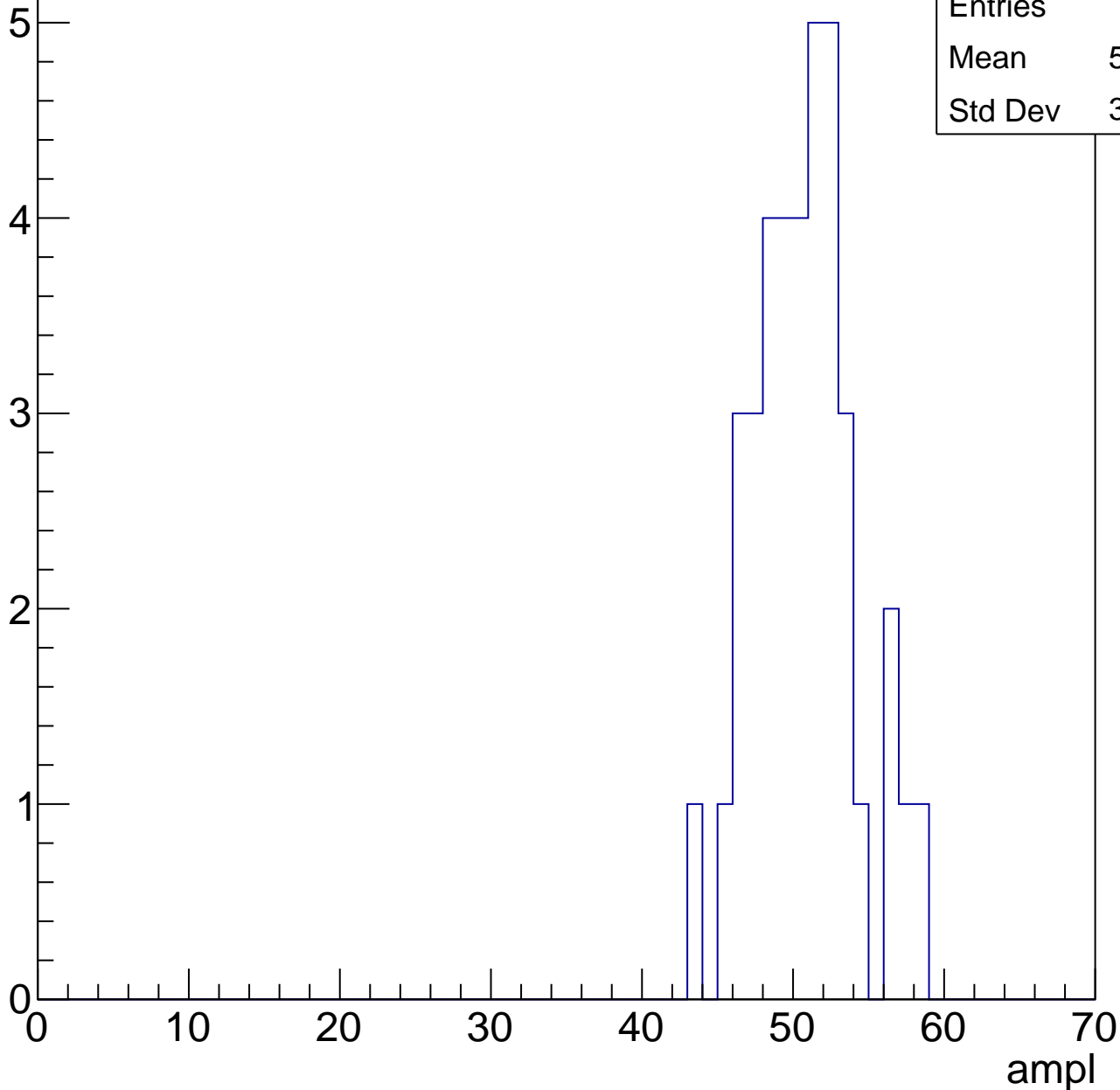
Entries	27
Mean	44.04
Std Dev	2.659

B1L103S, U14-ch33, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

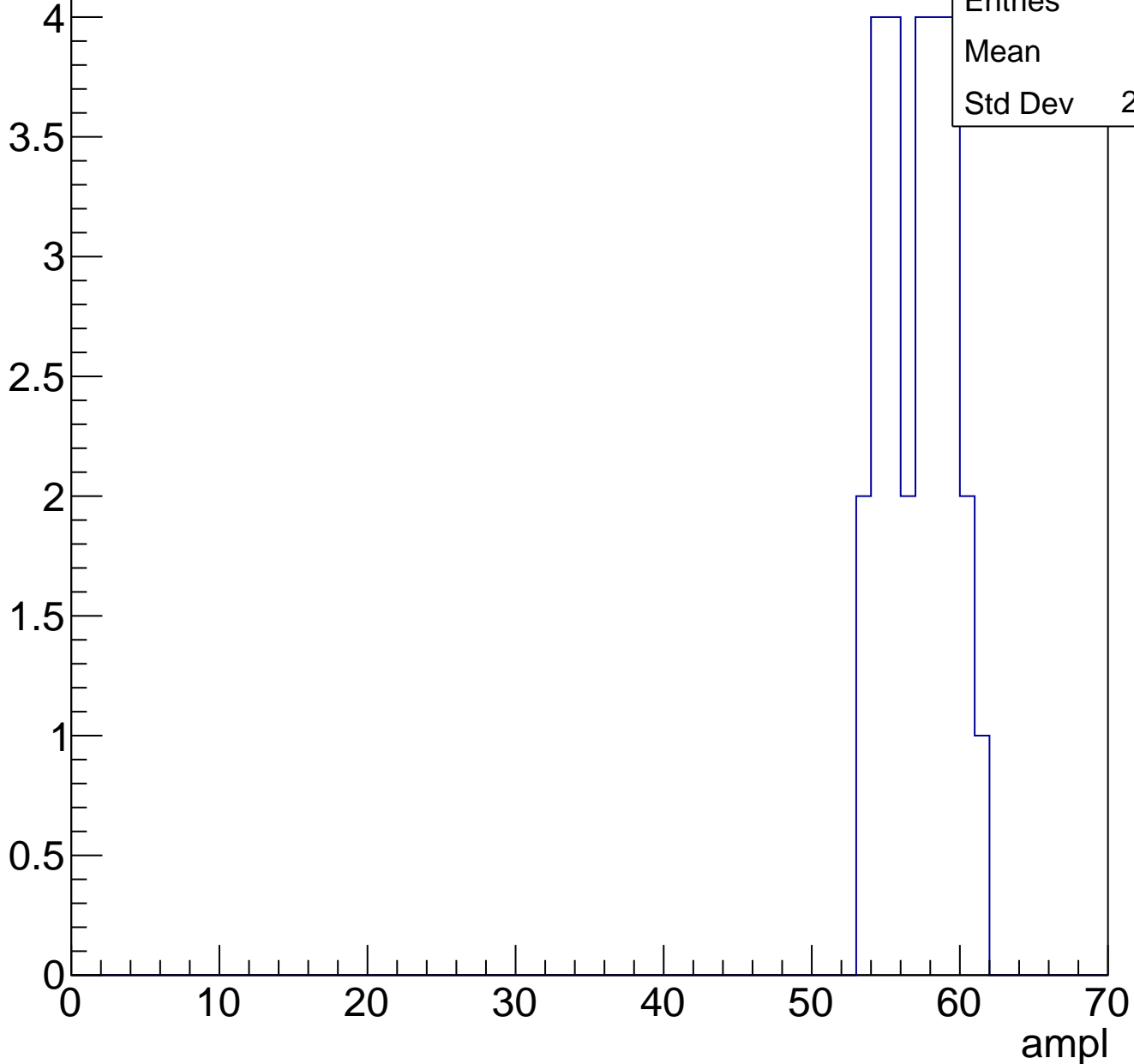
Entries	38
Mean	50.26
Std Dev	3.322



B1L103S, U14-ch33, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



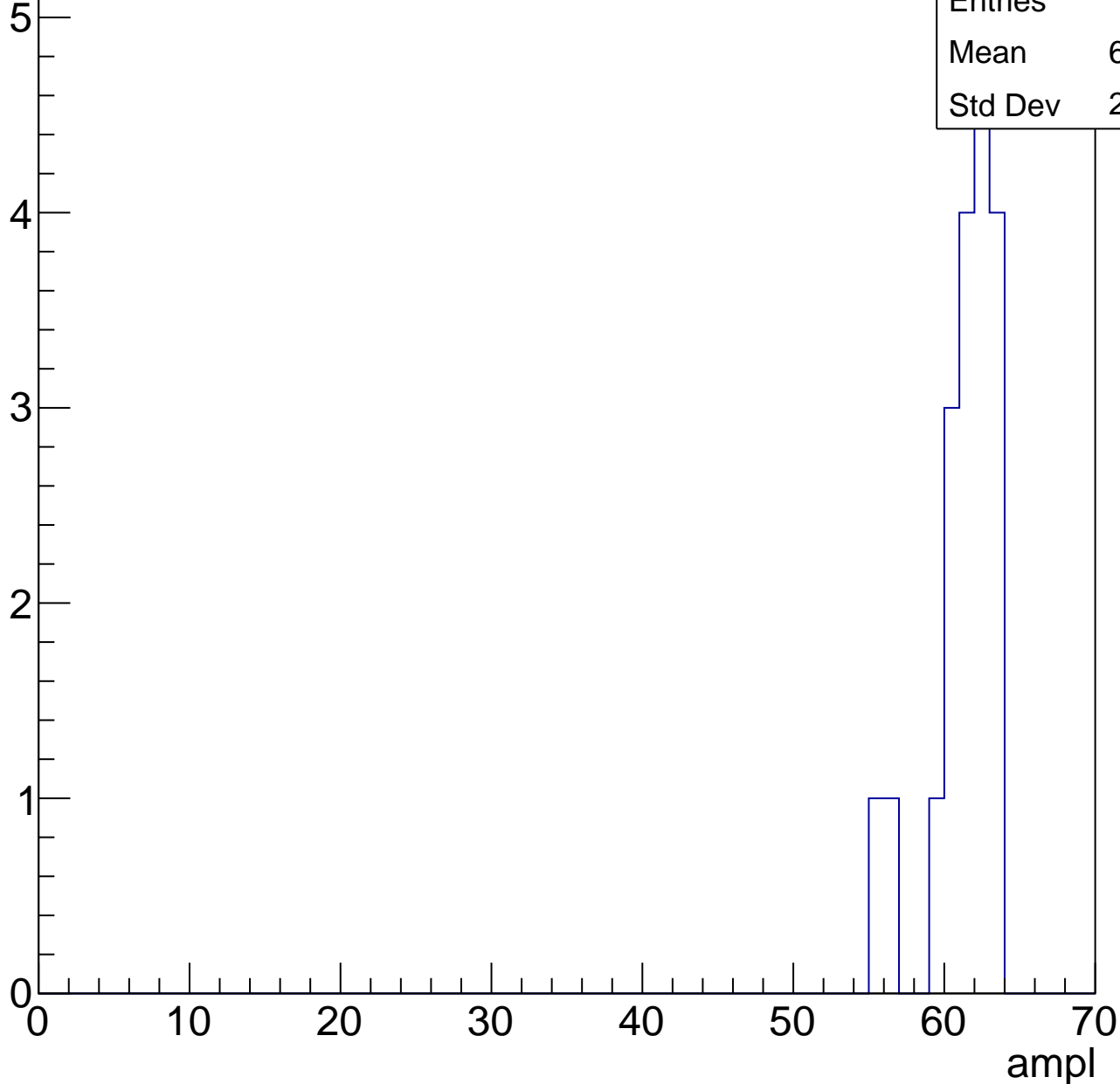
Entries	27
Mean	56.7
Std Dev	2.258

B1L103S, U14-ch33, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	19
Mean	60.84
Std Dev	2.159



B1L103S, U14-ch33, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch33, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

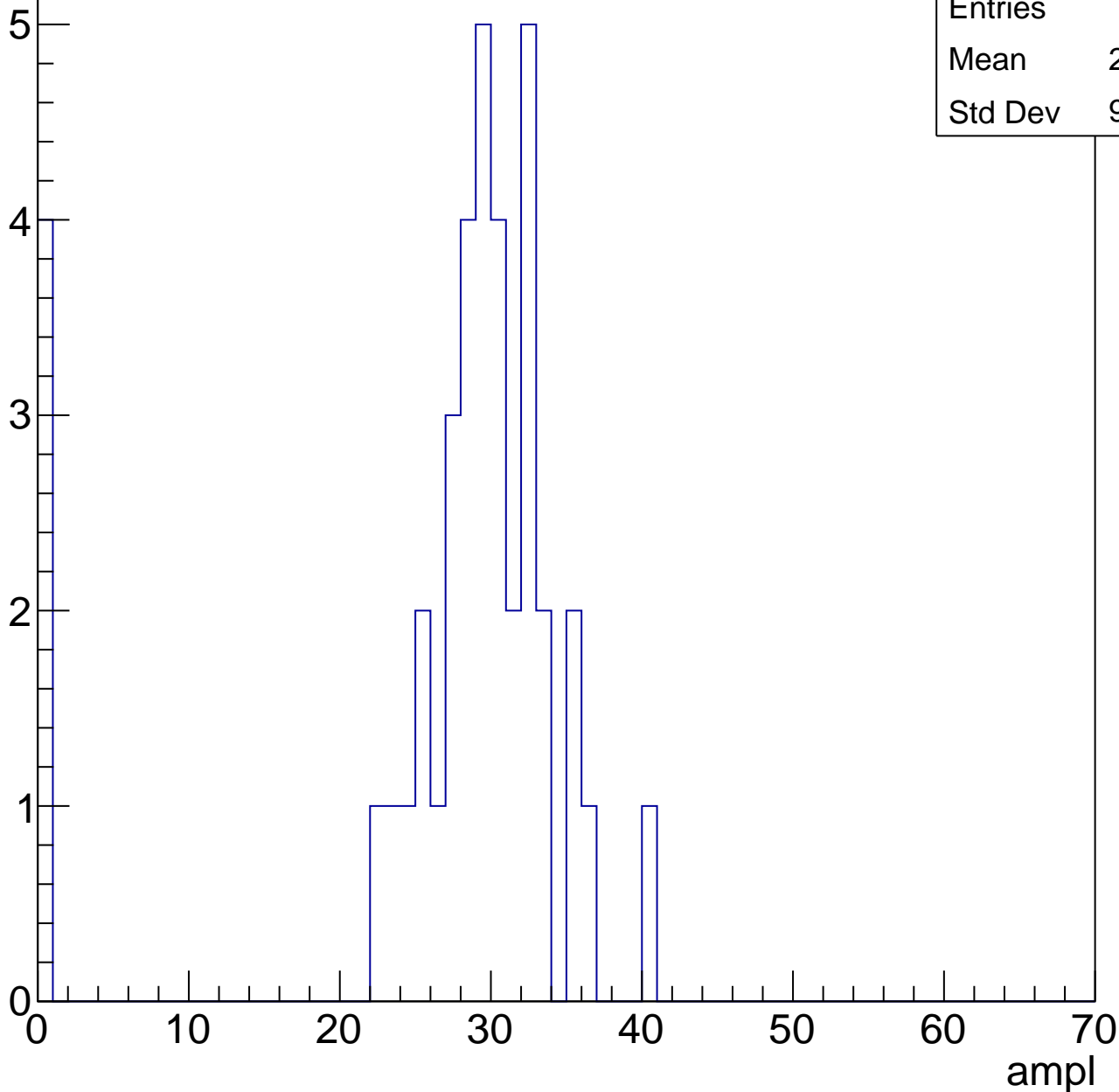
Entries	11
Mean	0
Std Dev	0

B1L103S, U14-ch34, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	26.59
Std Dev	9.655

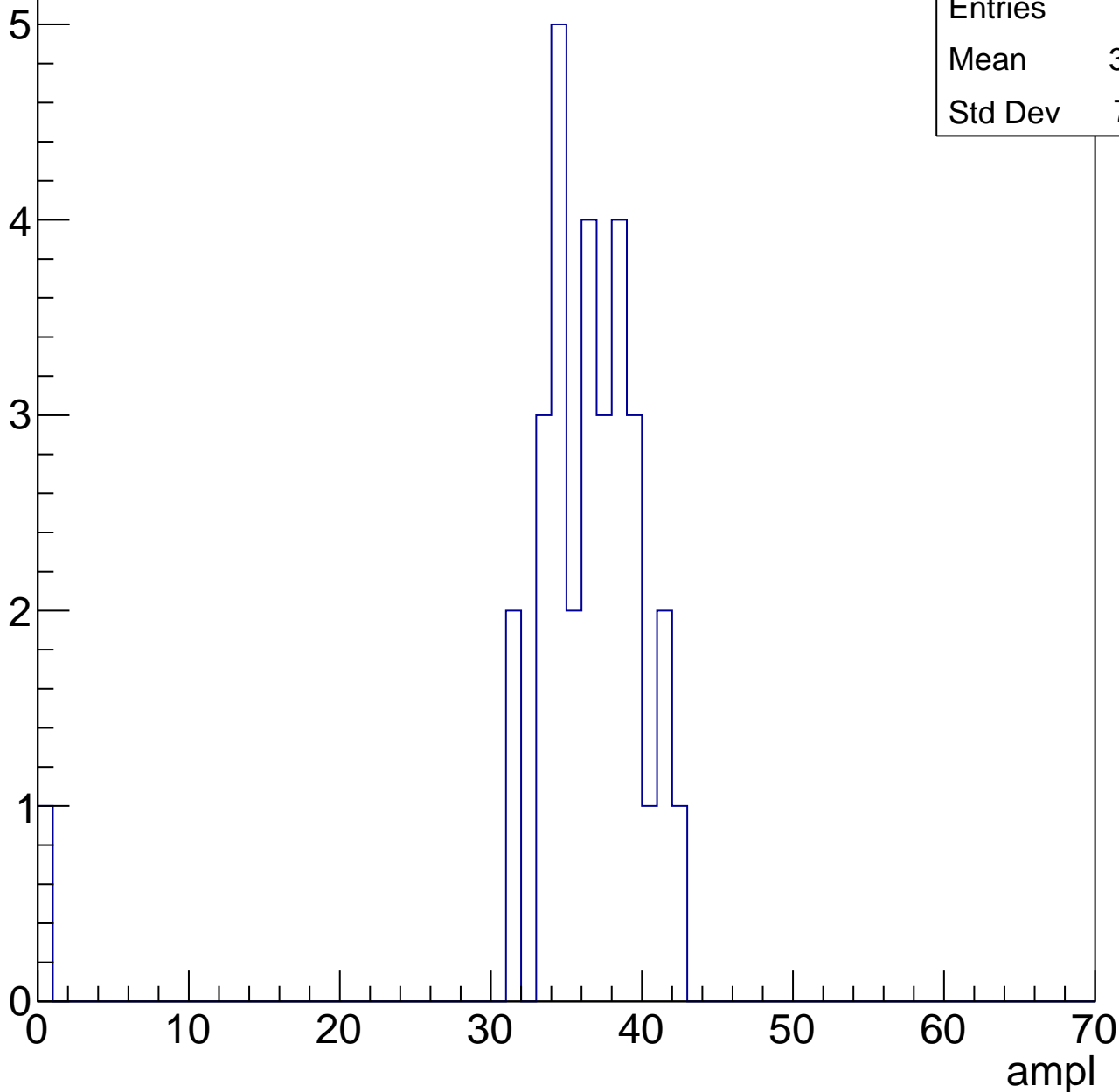


B1L103S, U14-ch34, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	31
Mean	35.13
Std Dev	7.001

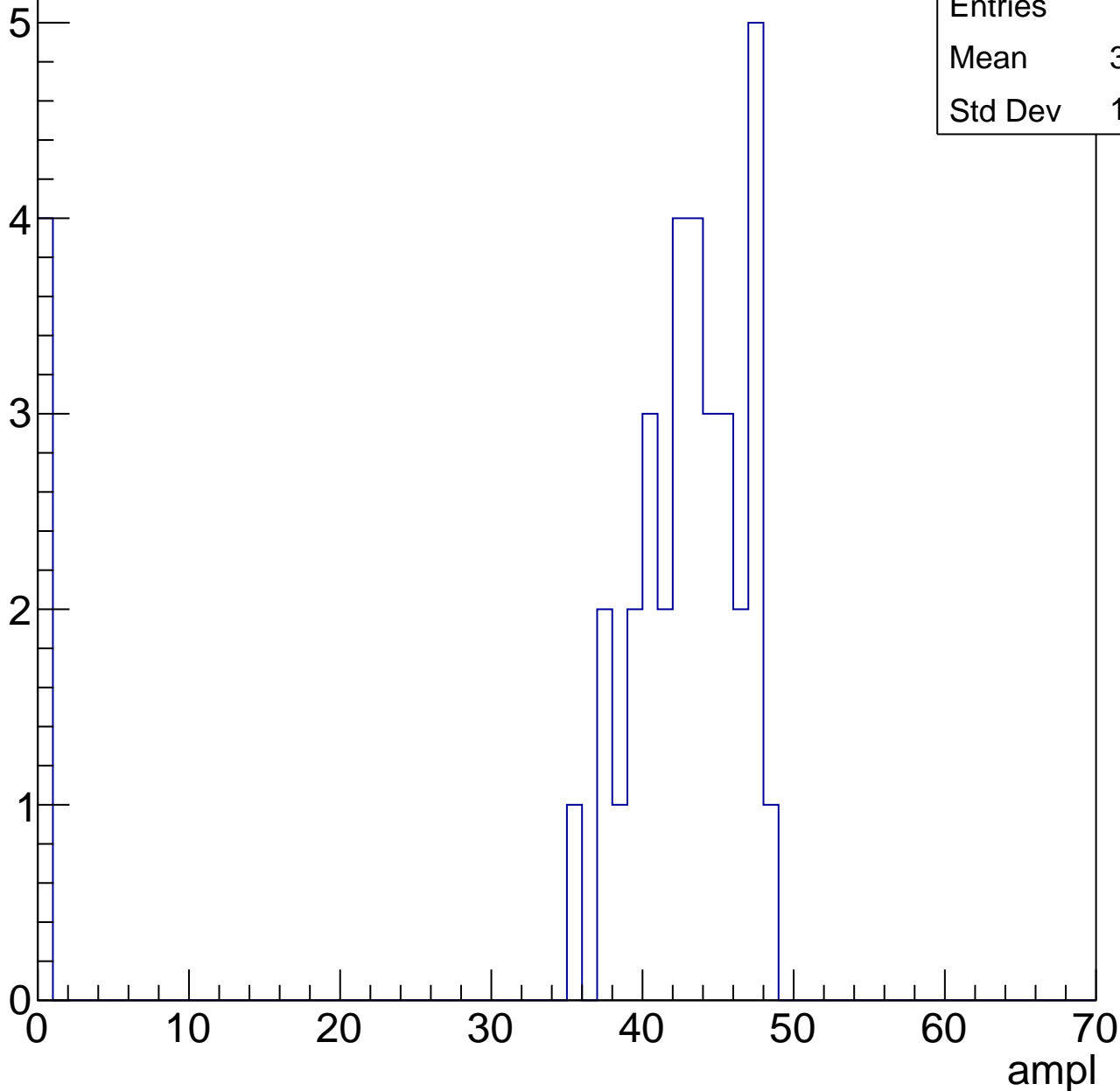


B1L103S, U14-ch34, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	37
Mean	38.08
Std Dev	13.63

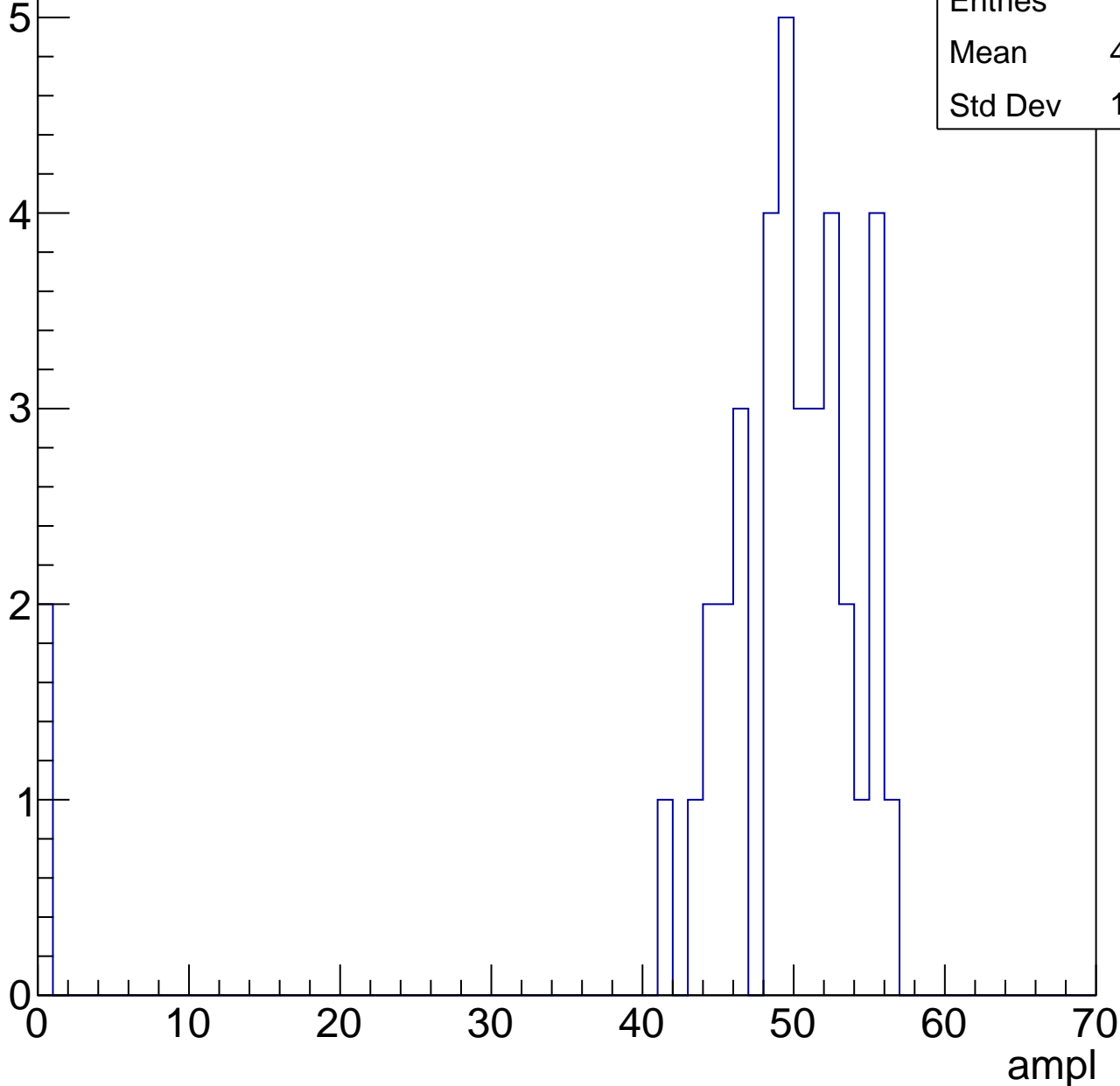


B1L103S, U14-ch34, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

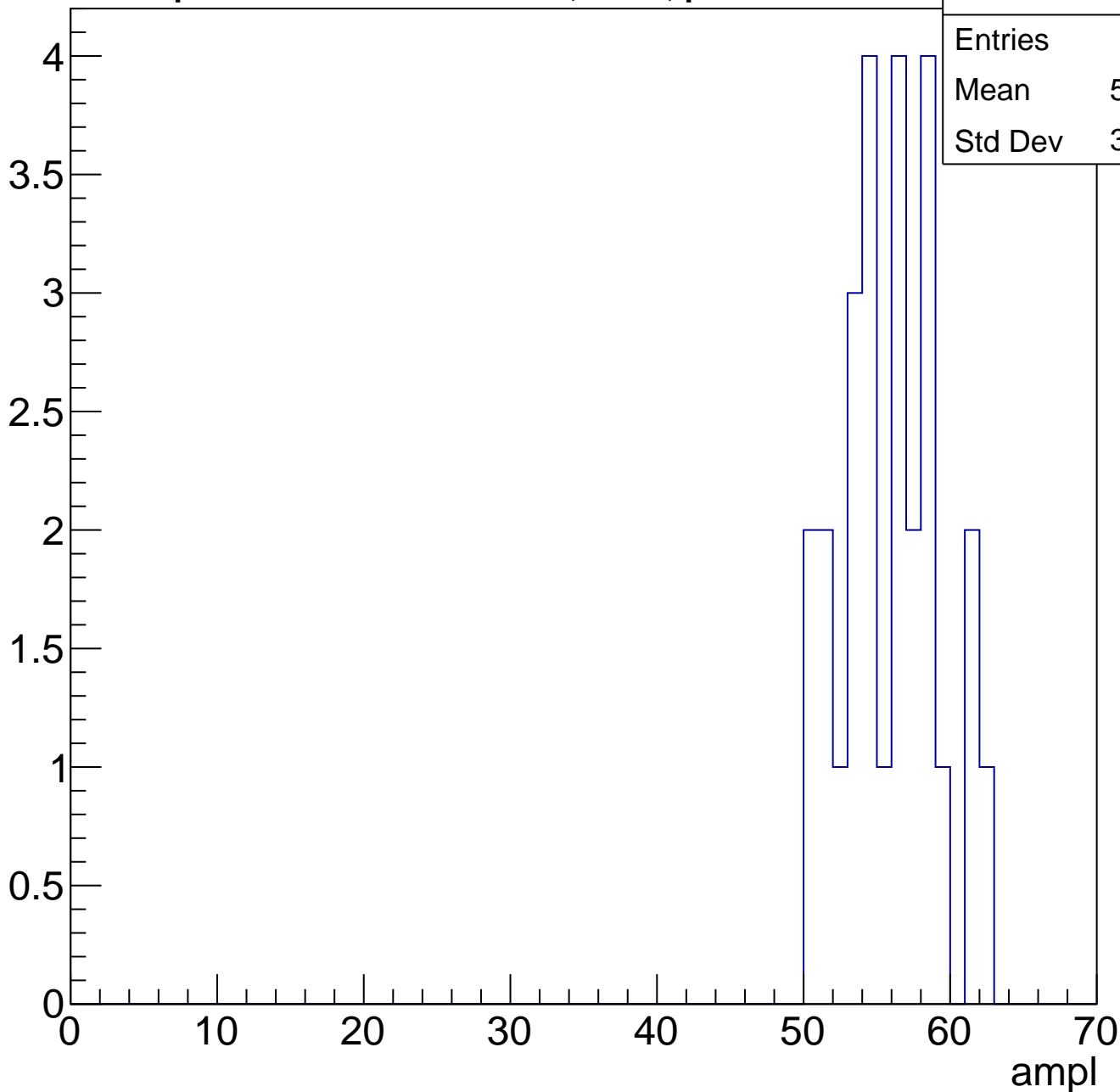
Entries	38
Mean	46.95
Std Dev	11.65



B1L103S, U14-ch34, adc4

calib_packv5_041523_1651.root, FC#0, port C2

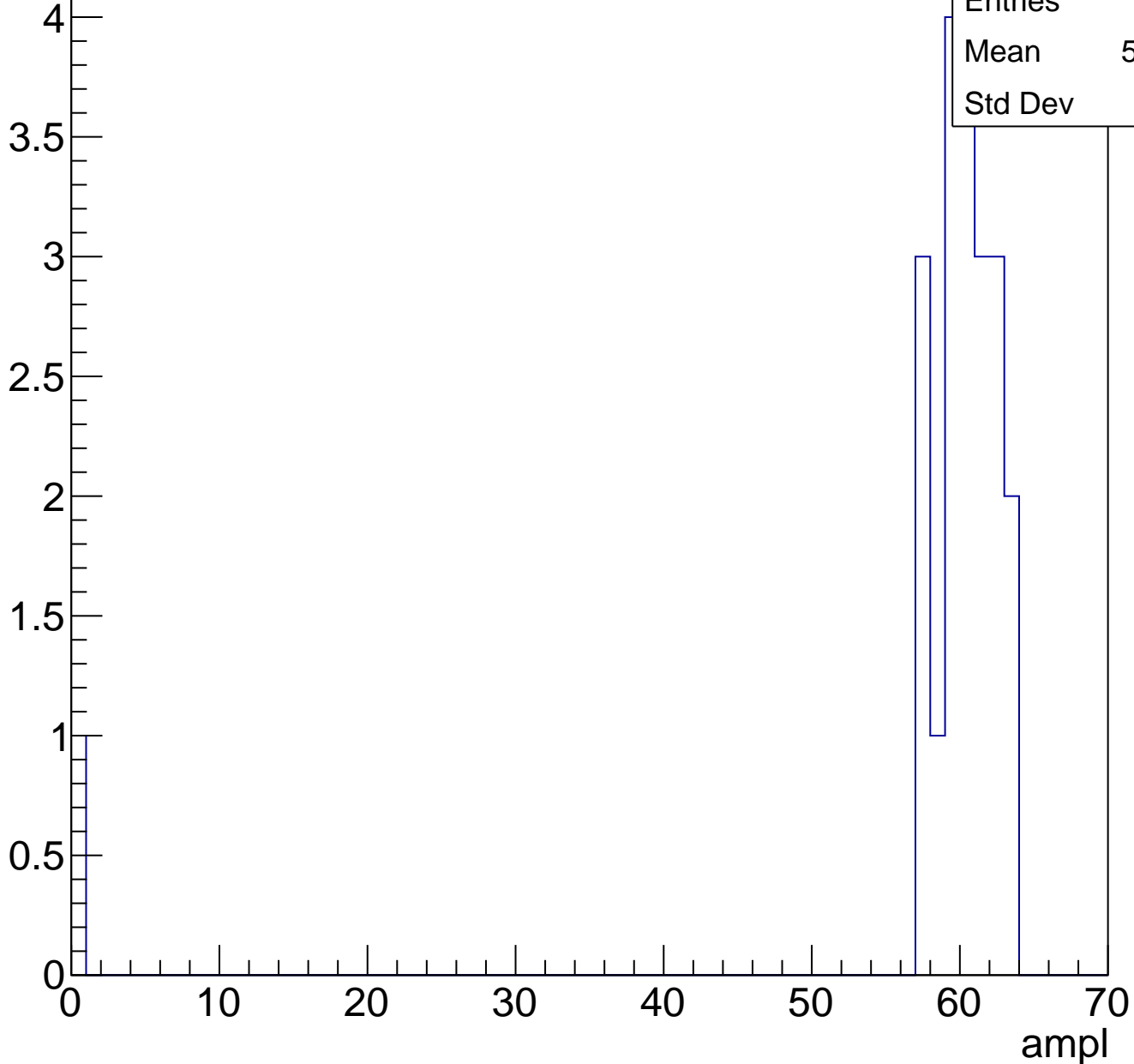
Entry



B1L103S, U14-ch34, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch34, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	4
Mean	62
Std Dev	1.225

ampl

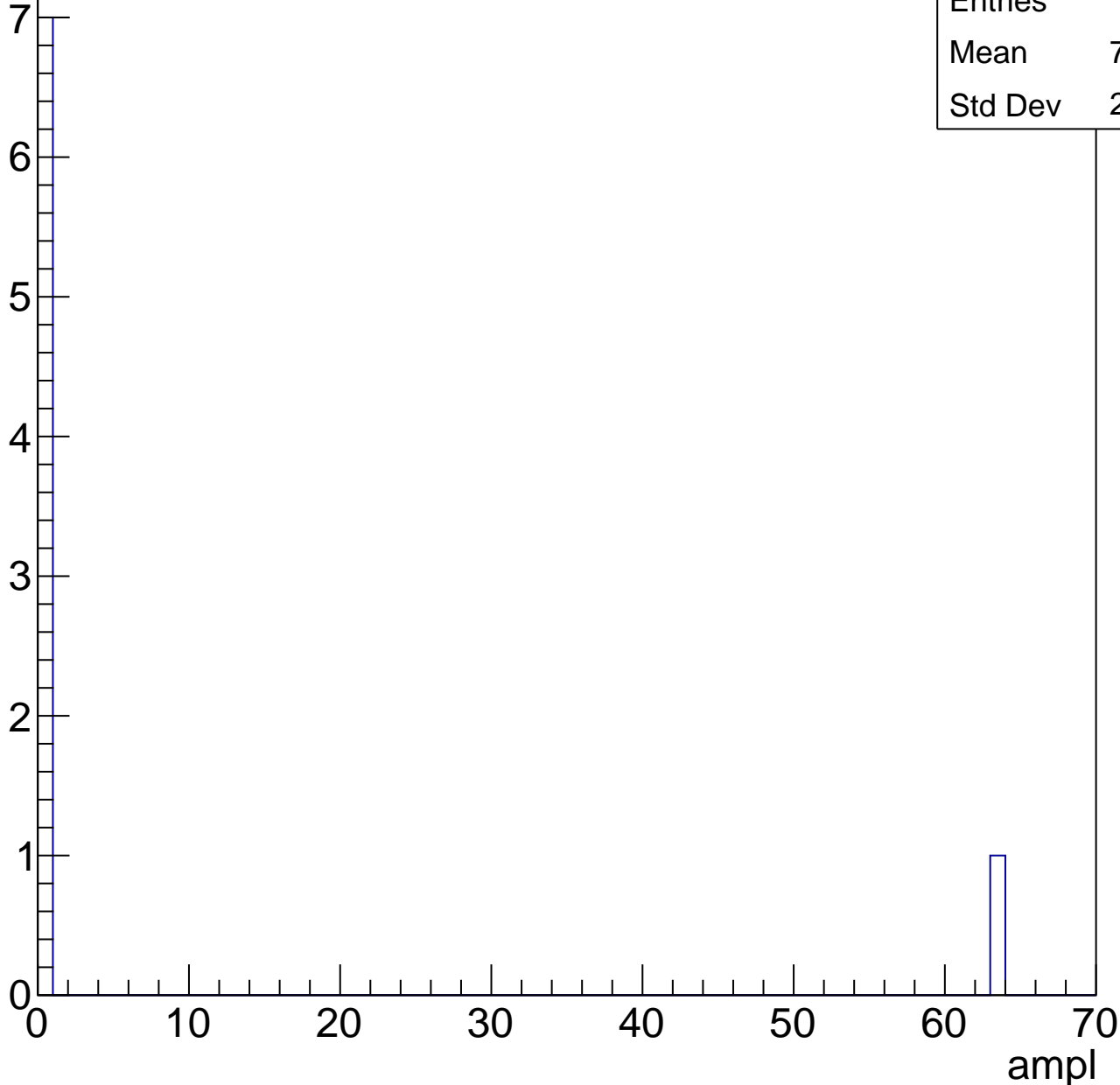
0 10 20 30 40 50 60 70

B1L103S, U14-ch34, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	8
Mean	7.875
Std Dev	20.84

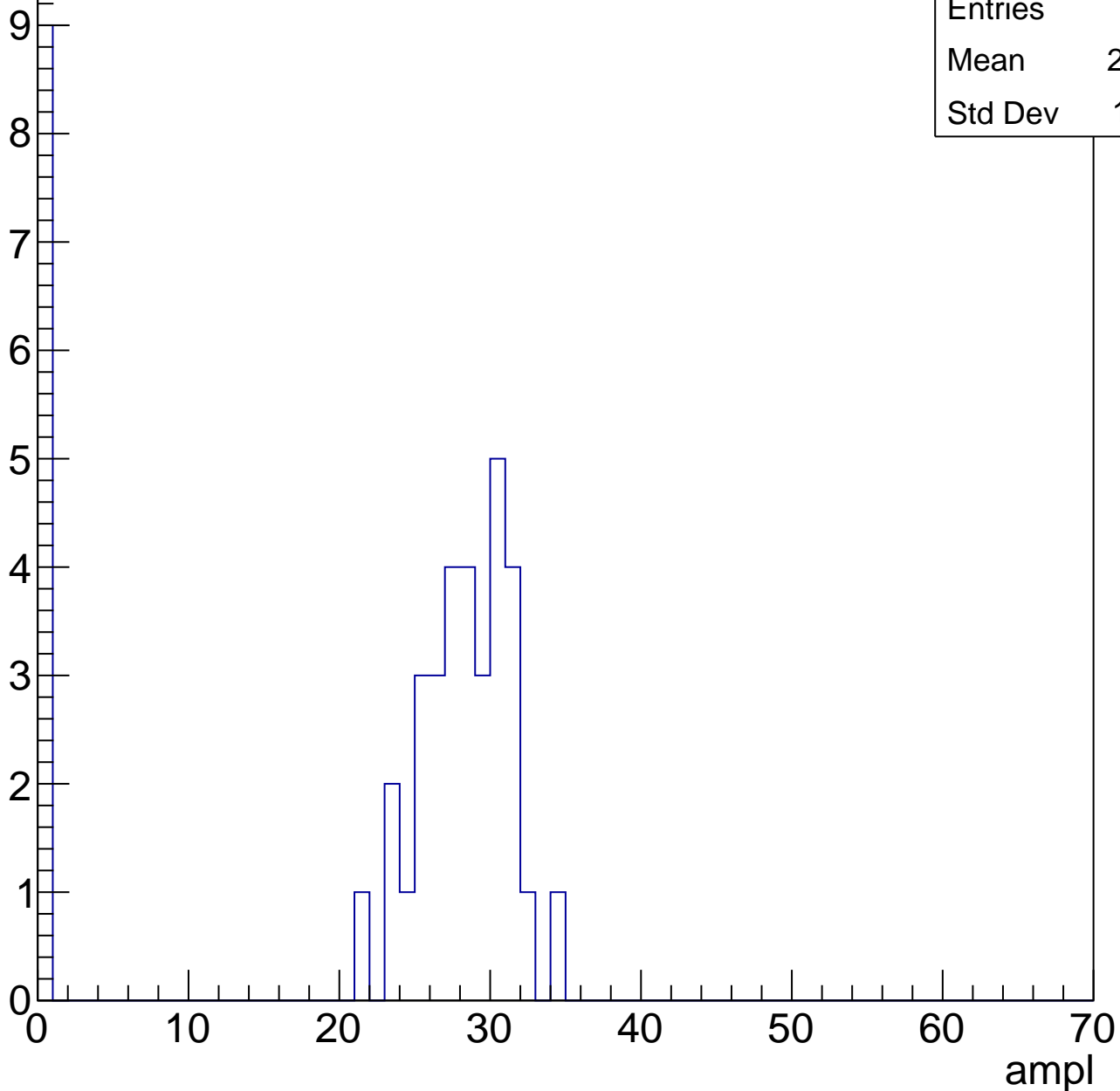


B1L103S, U14-ch35, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

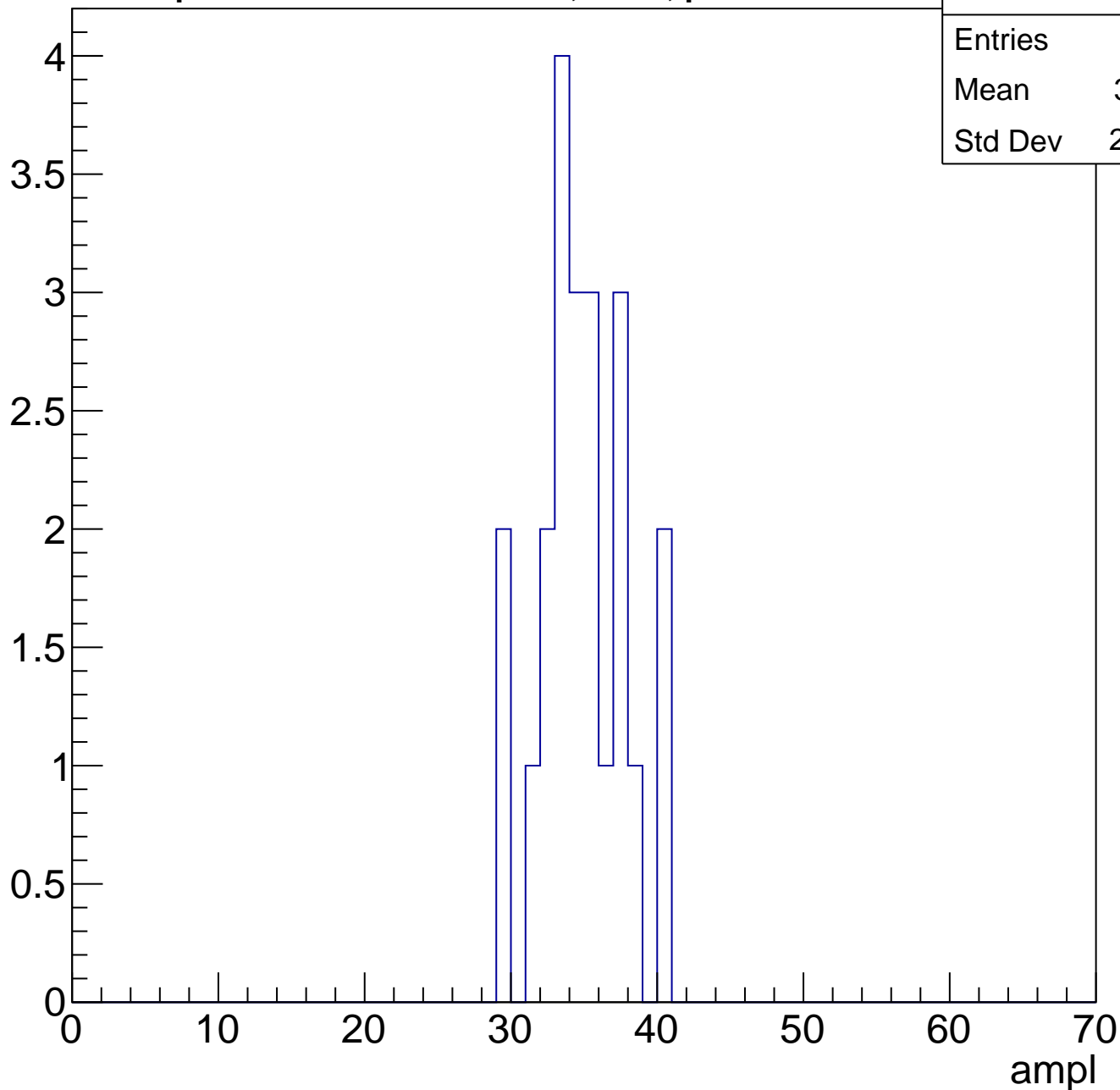
Entries	41
Mean	21.73
Std Dev	11.81



B1L103S, U14-ch35, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry



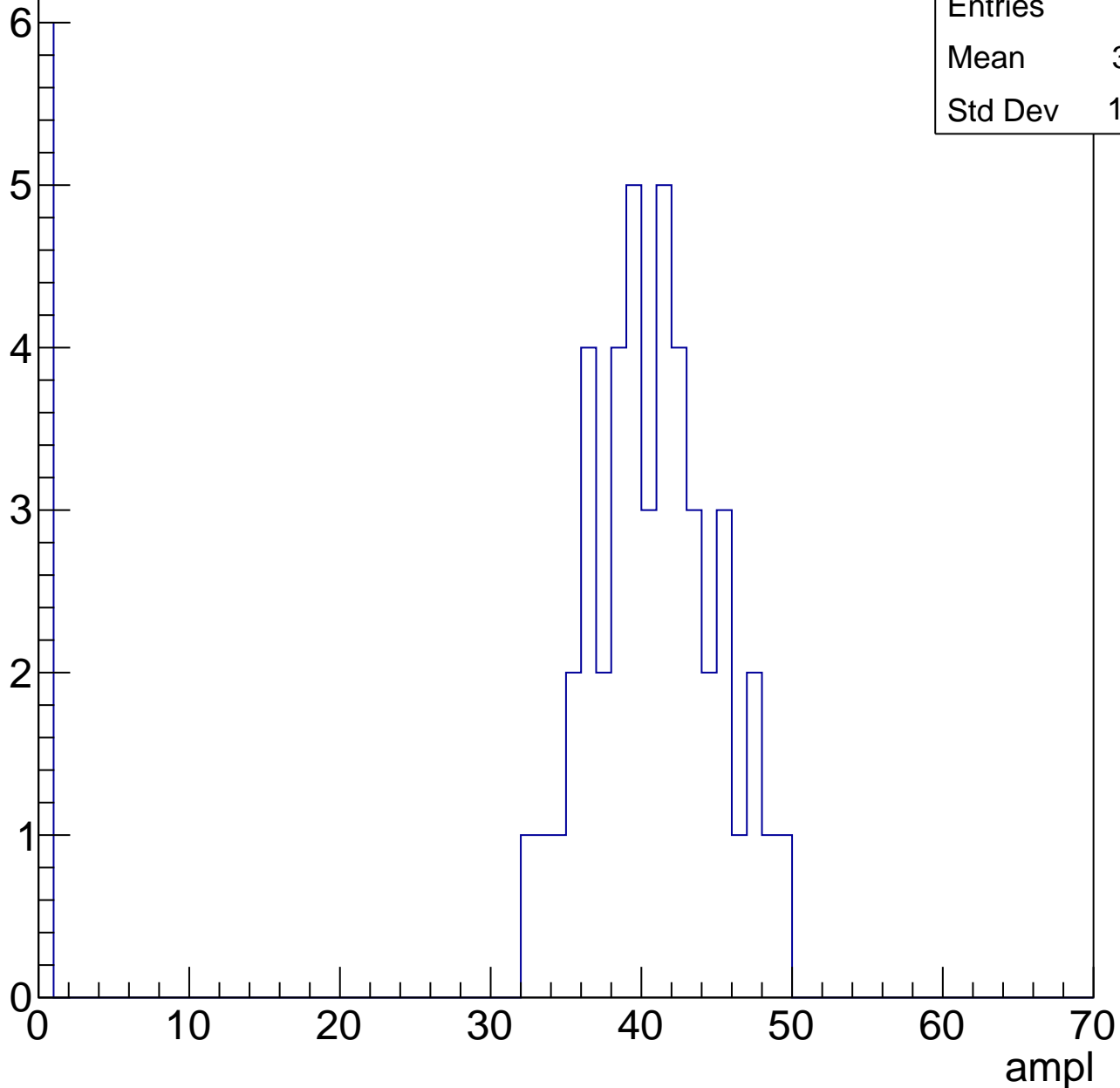
Entries	22
Mean	34.41
Std Dev	2.933

B1L103S, U14-ch35, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

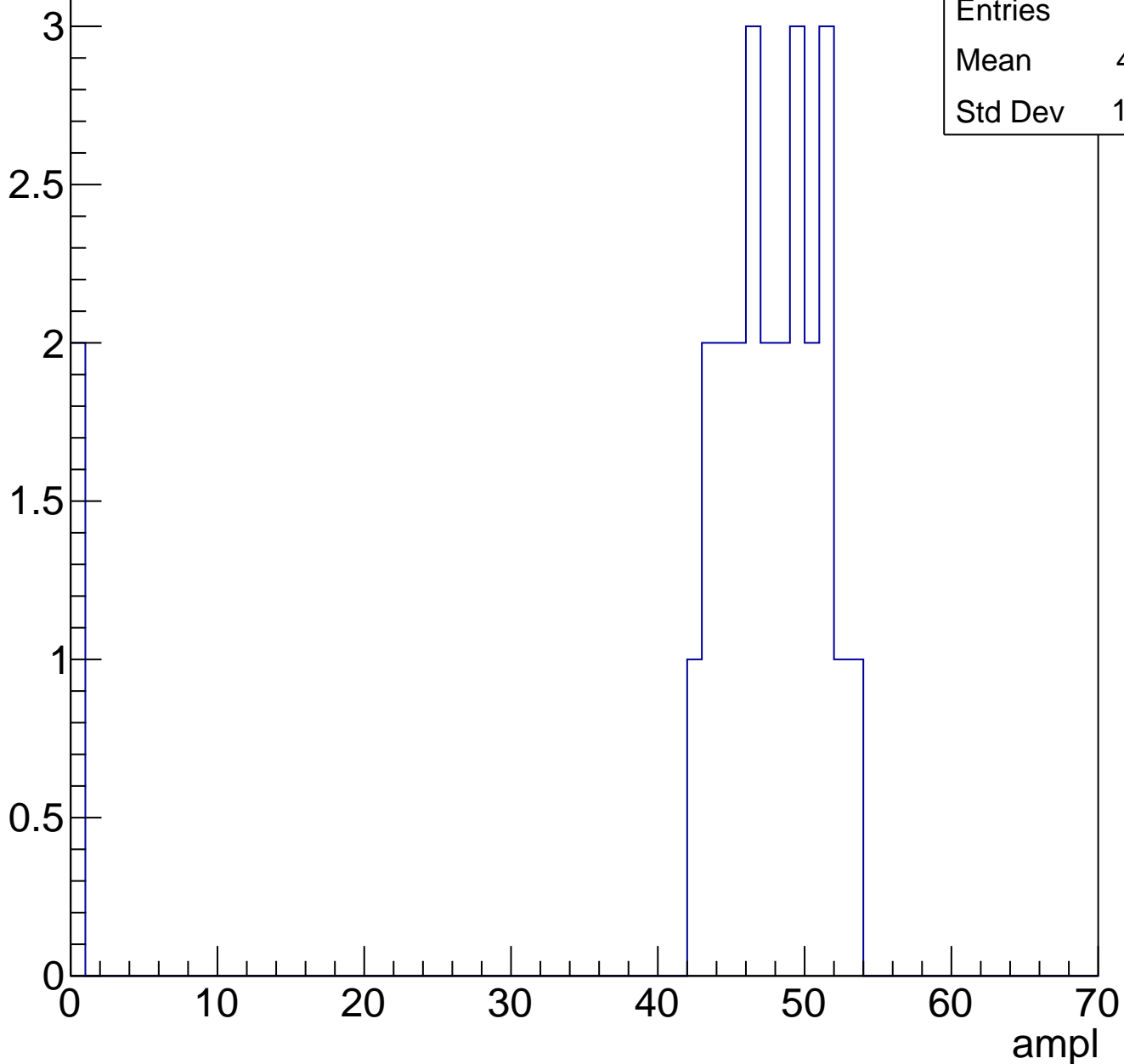
Entries	51
Mean	35.61
Std Dev	13.54



B1L103S, U14-ch35, adc3

calib_packv5_041523_1651.root, FC#0, port C2

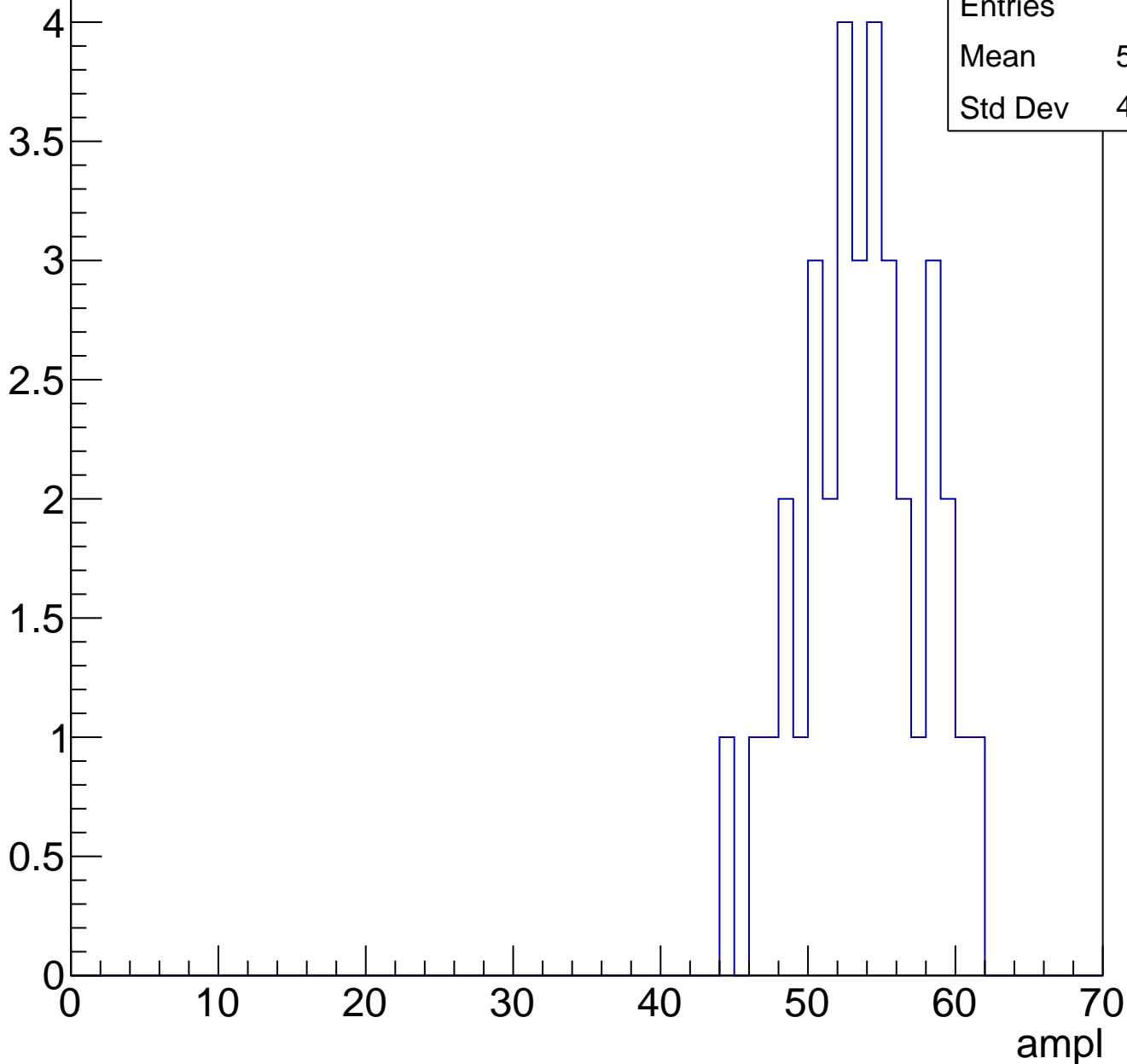
Entry



B1L103S, U14-ch35, adc4

calib_packv5_041523_1651.root, FC#0, port C2

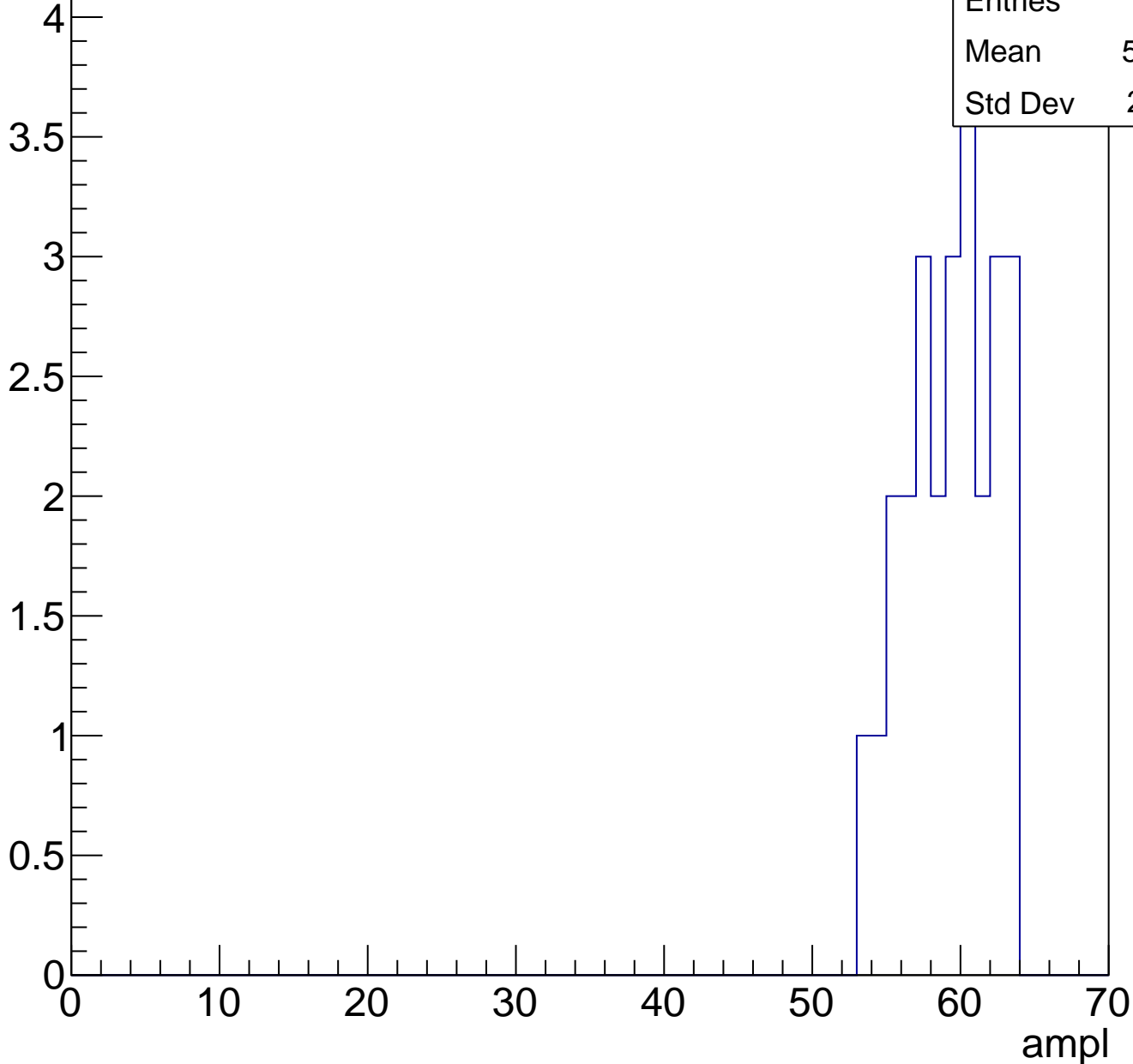
Entry



B1L103S, U14-ch35, adc5

calib_packv5_041523_1651.root, FC#0, port C2

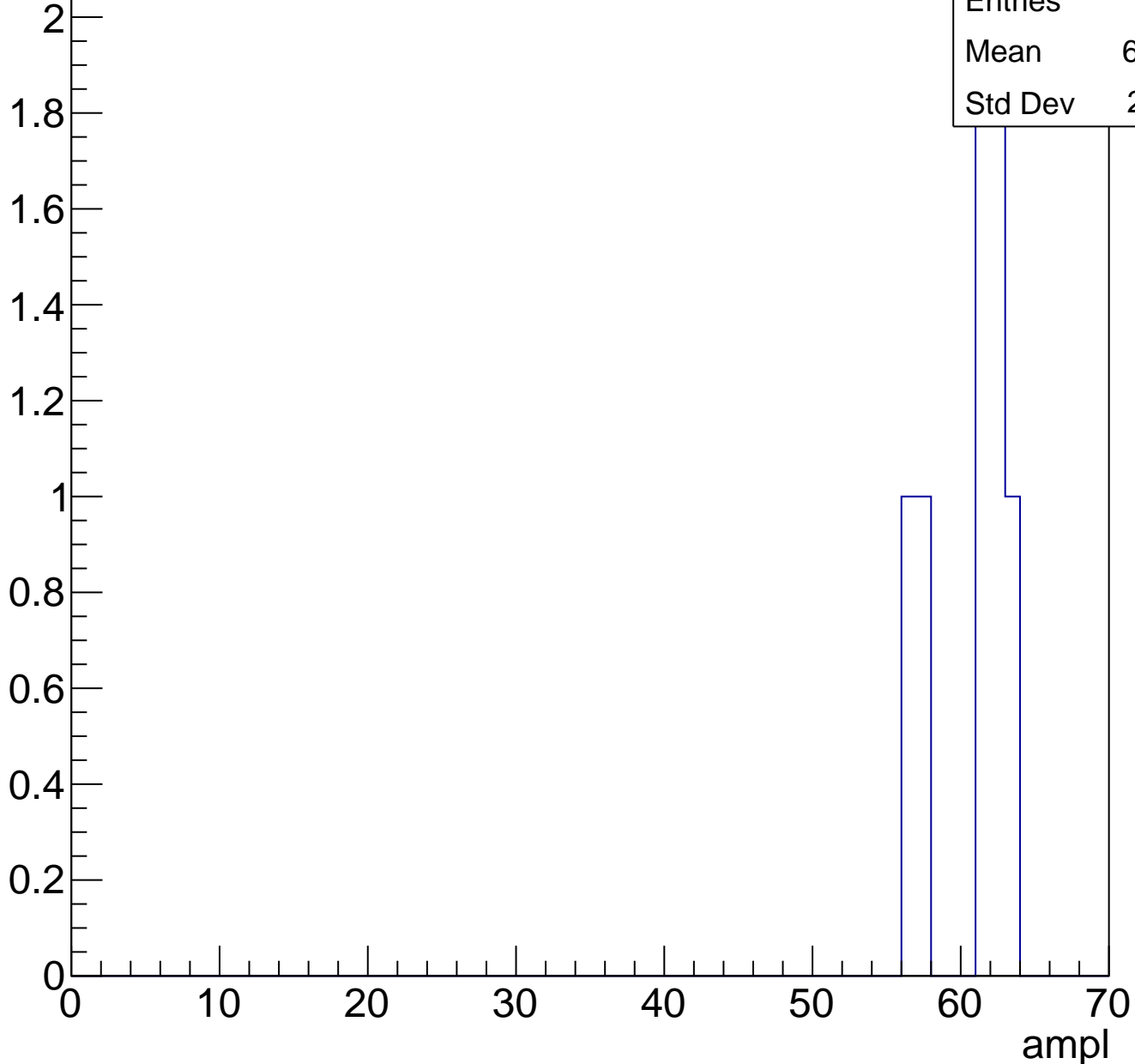
Entry



B1L103S, U14-ch35, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



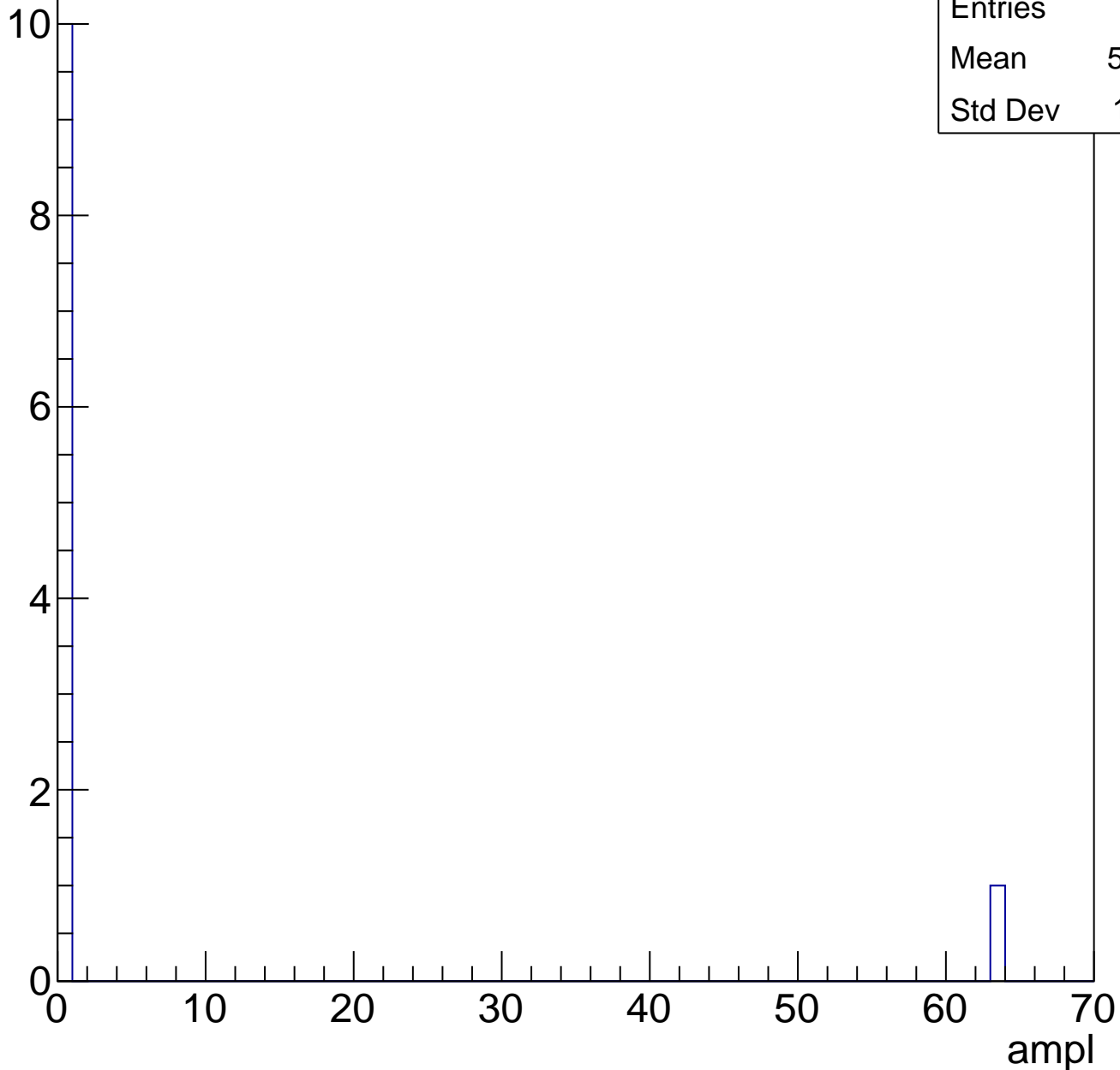
Entries	7
Mean	60.29
Std Dev	2.491

B1L103S, U14-ch35, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	11
Mean	5.727
Std Dev	18.11

Entry



B1L103S, U14-ch36, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	41
Mean	20.9
Std Dev	13.07

Entry

10

8

6

4

2

0

0

10

20

30

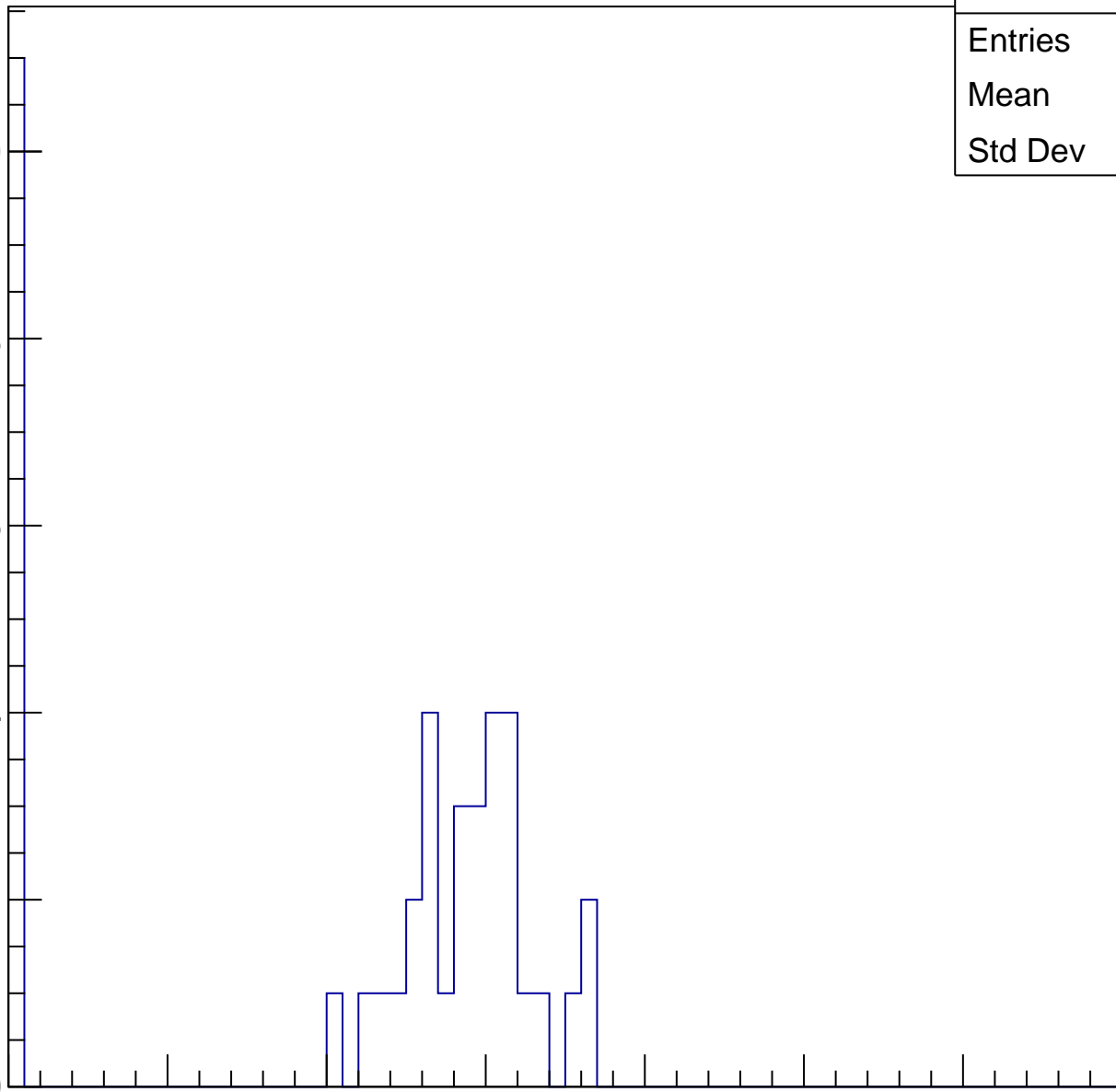
40

50

60

70

ampl

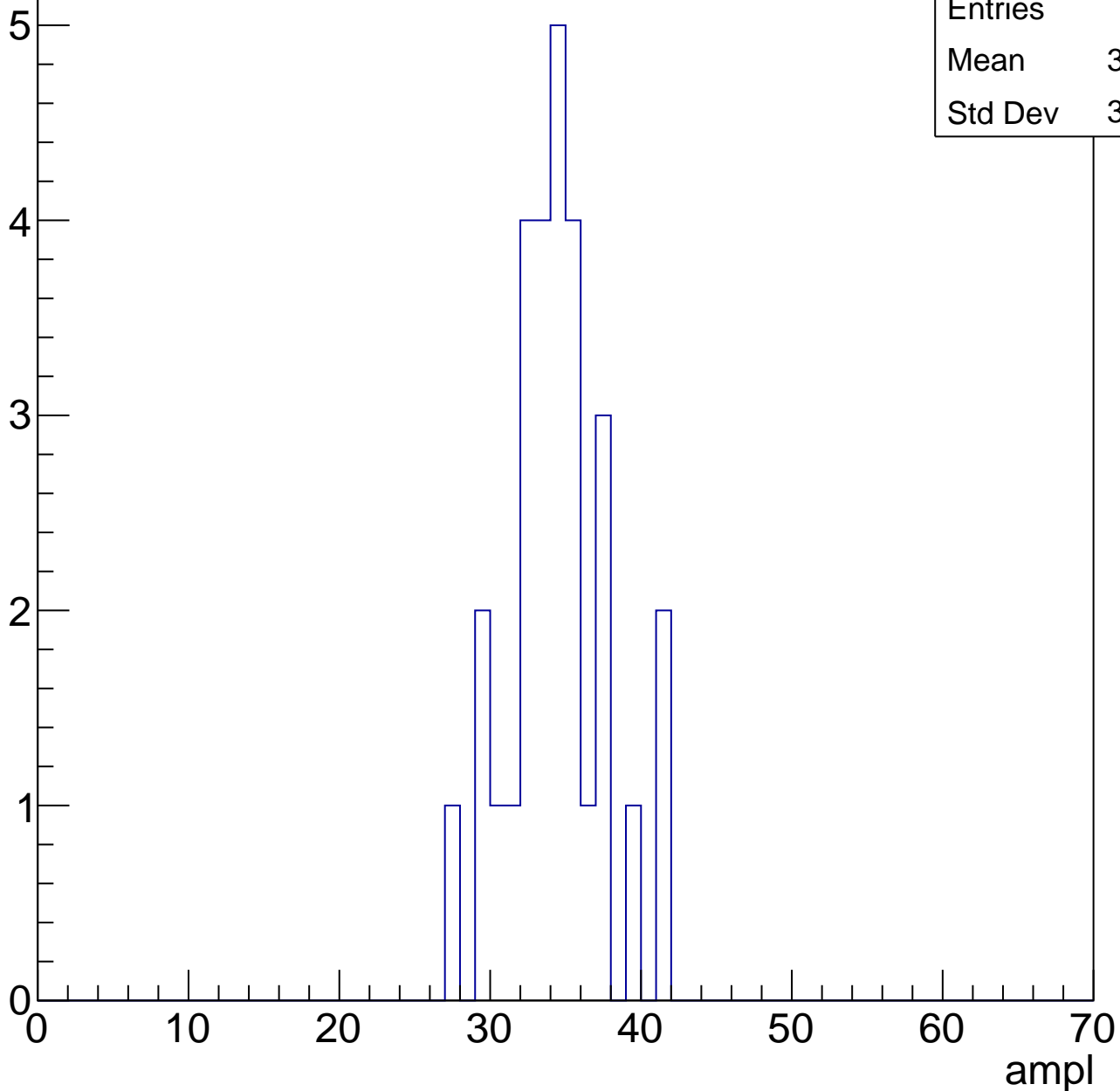


B1L103S, U14-ch36, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	29
Mean	33.93
Std Dev	3.226

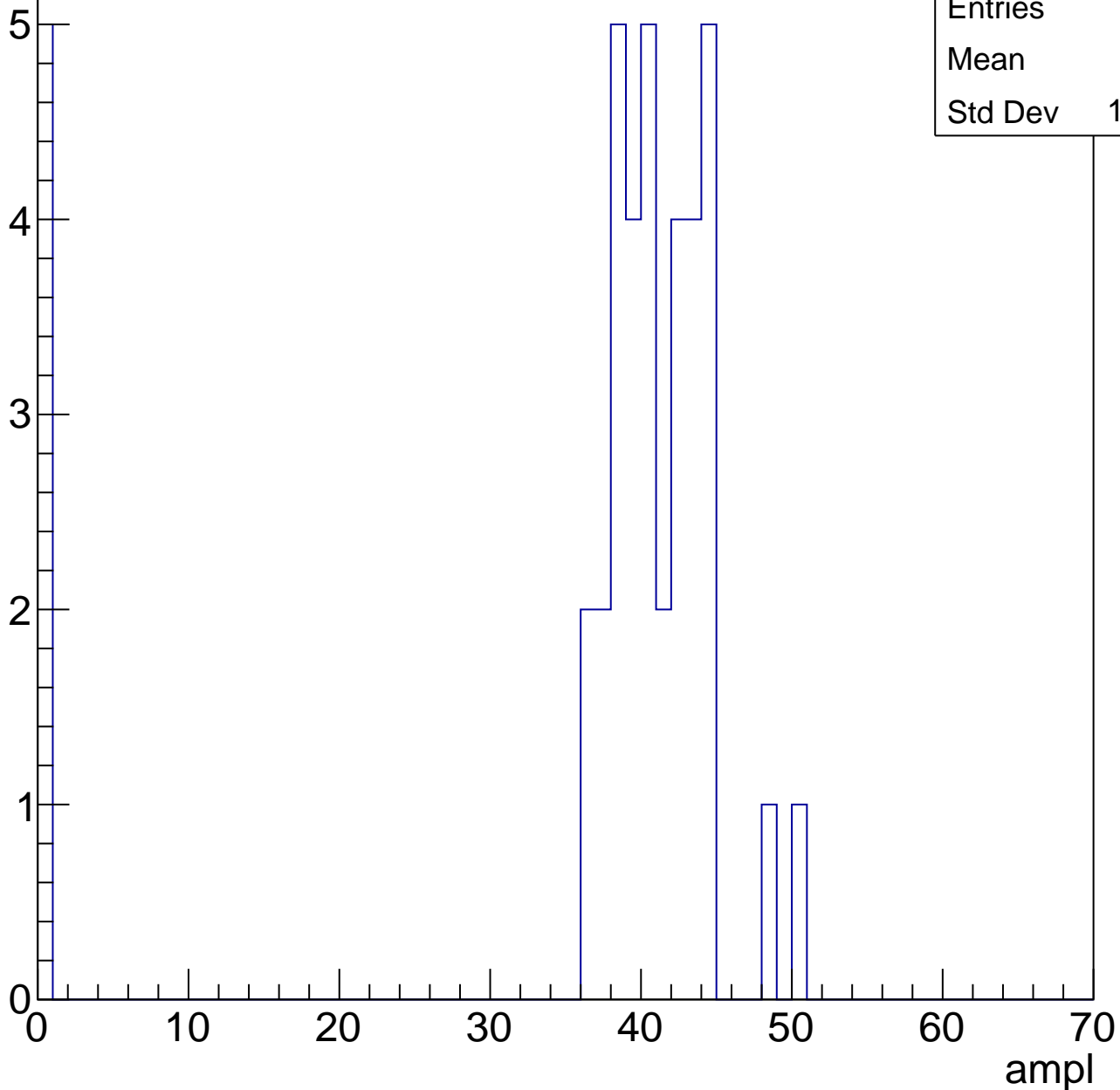


B1L103S, U14-ch36, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	35.8
Std Dev	13.84

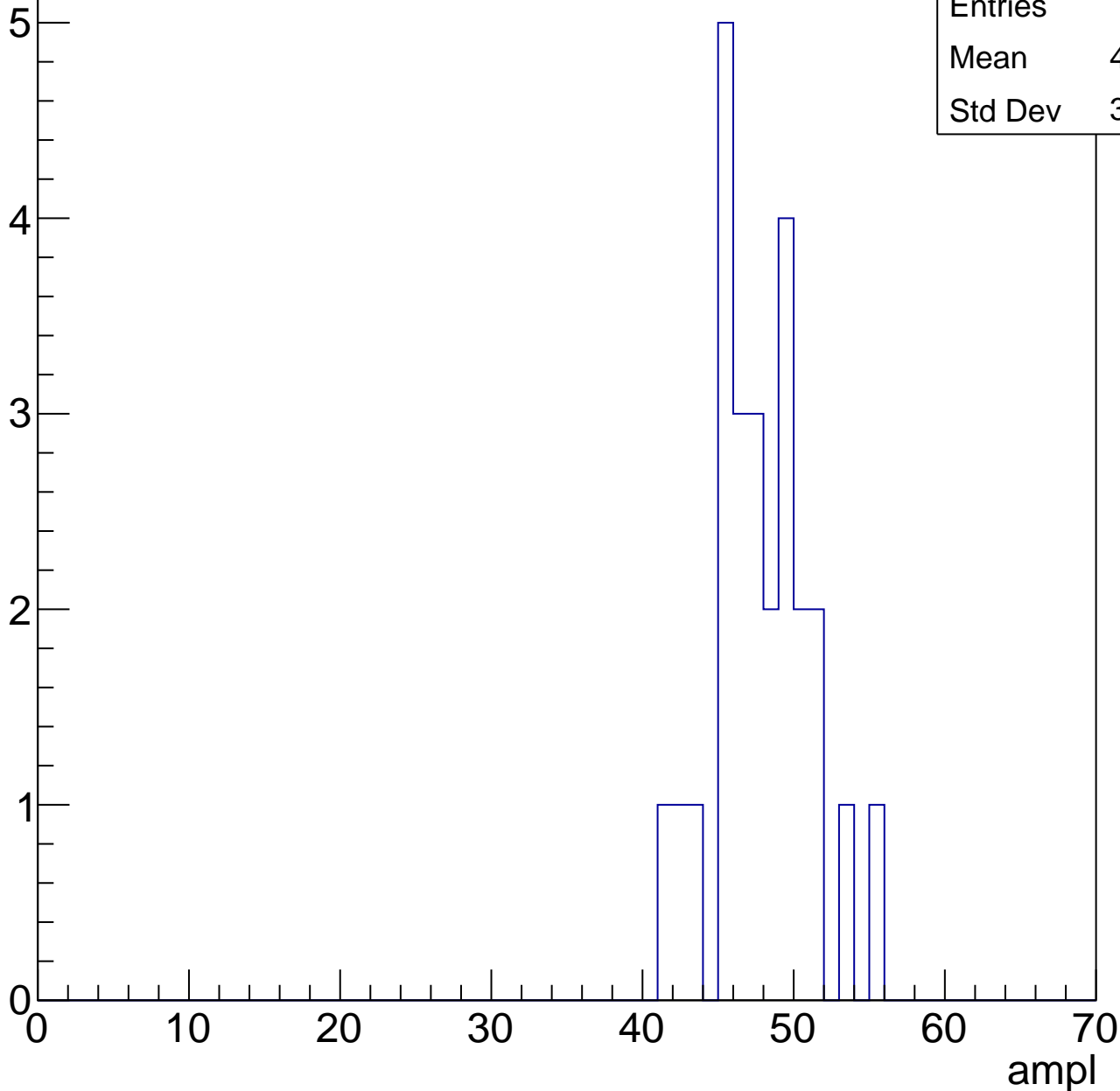


B1L103S, U14-ch36, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	26
Mean	47.38
Std Dev	3.187

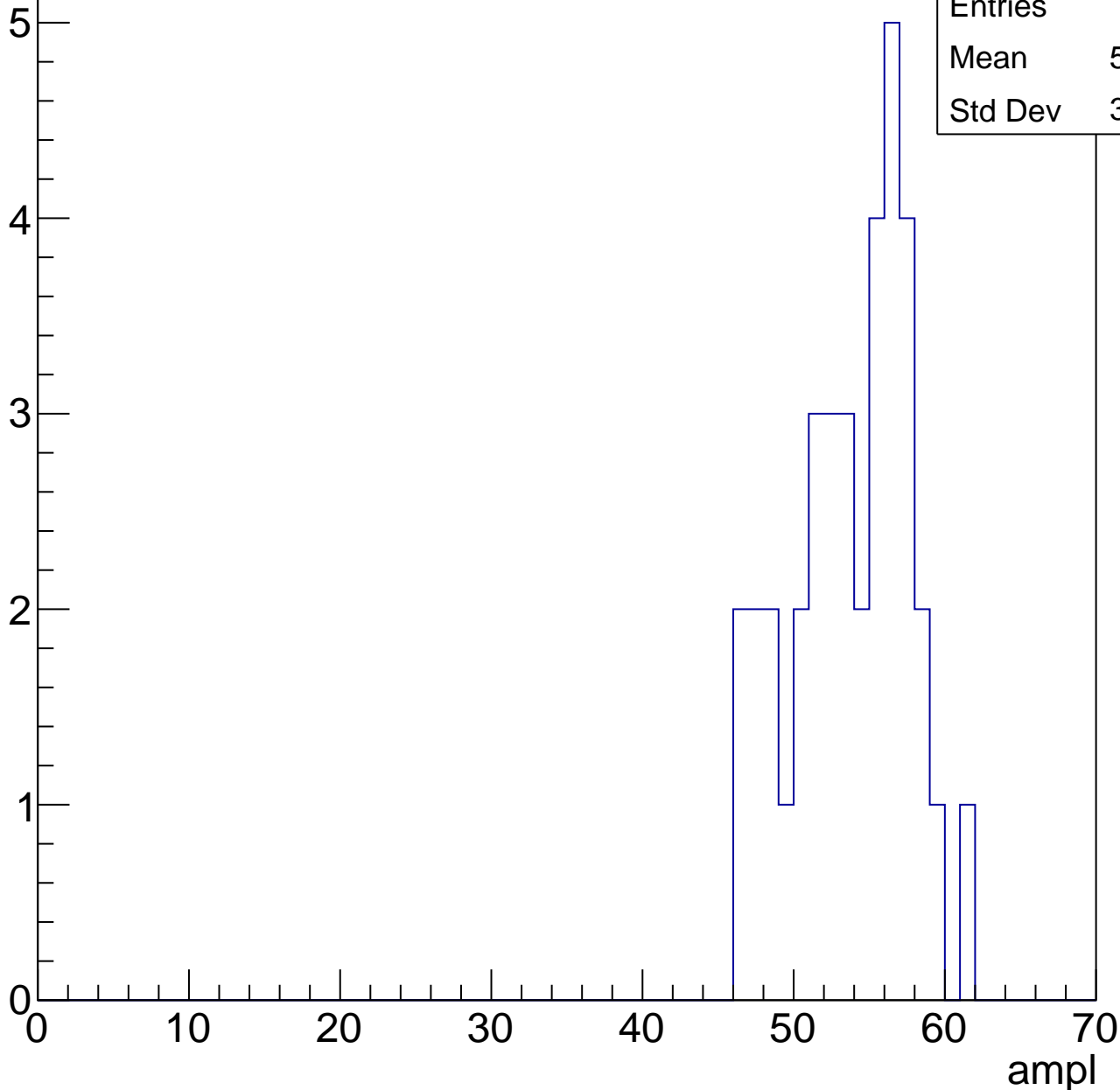


B1L103S, U14-ch36, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

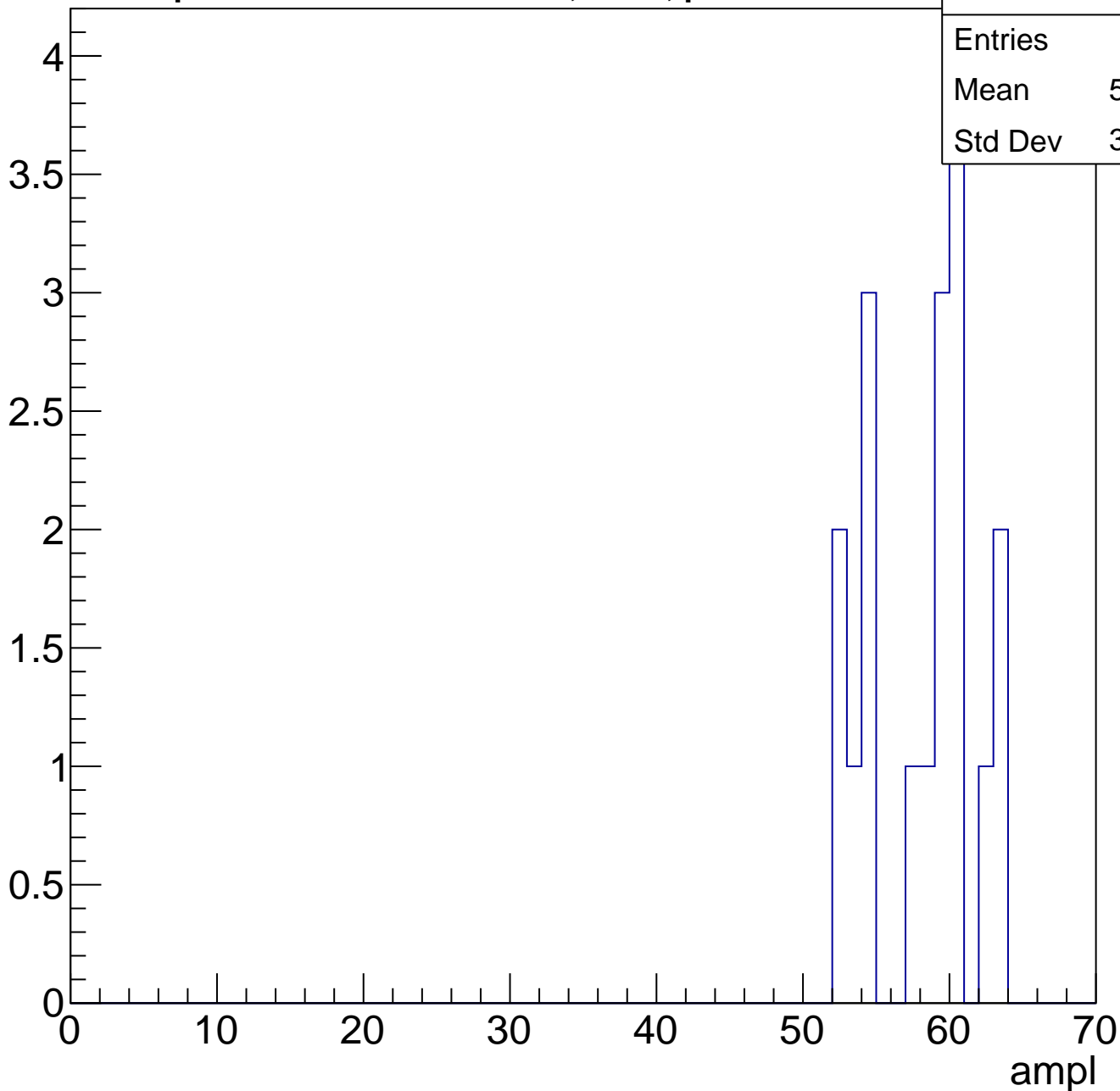
Entries	37
Mean	53.27
Std Dev	3.832



B1L103S, U14-ch36, adc5

calib_packv5_041523_1651.root, FC#0, port C2

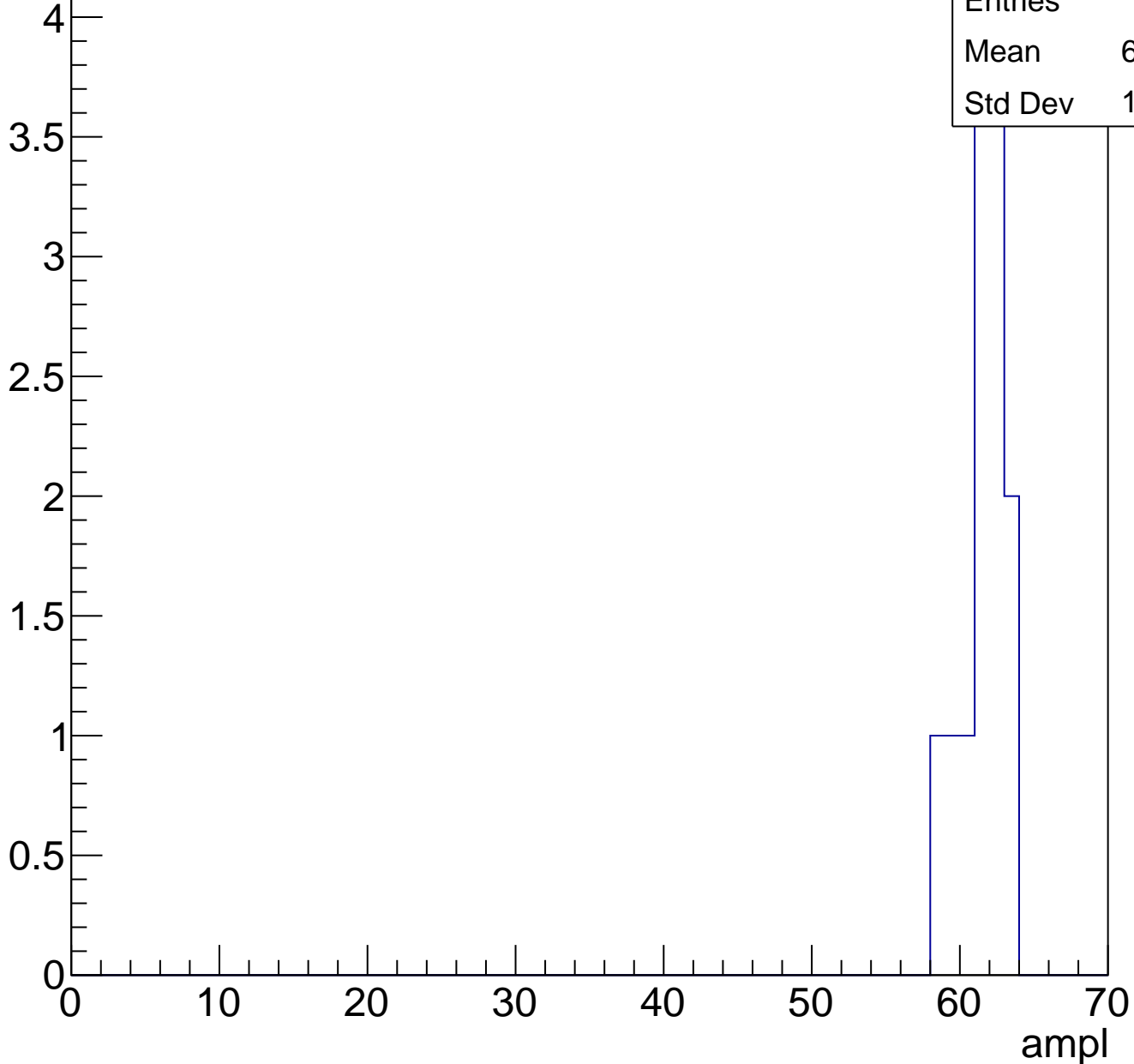
Entry



B1L103S, U14-ch36, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

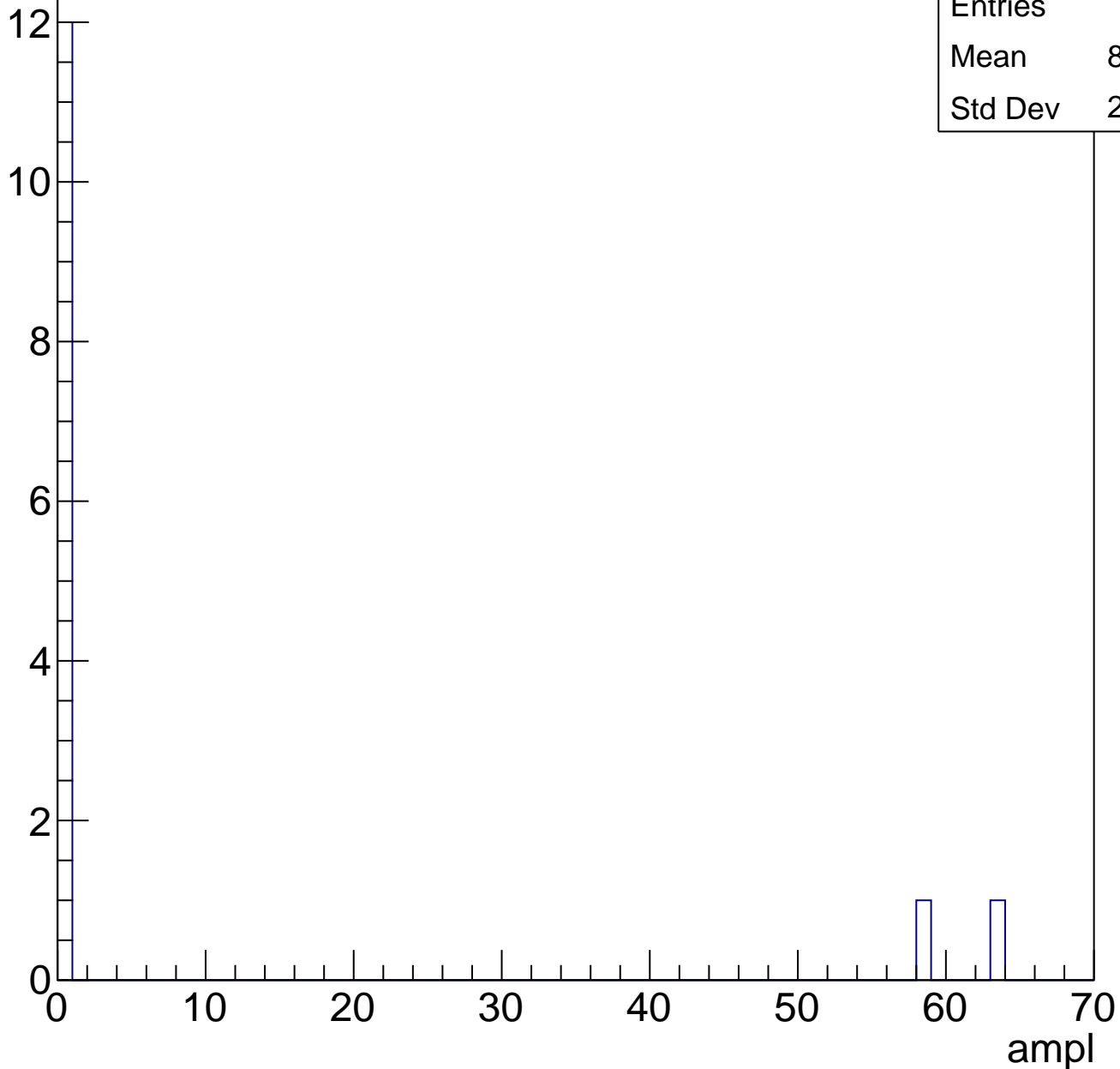


B1L103S, U14-ch36, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	14
Mean	8.643
Std Dev	21.19

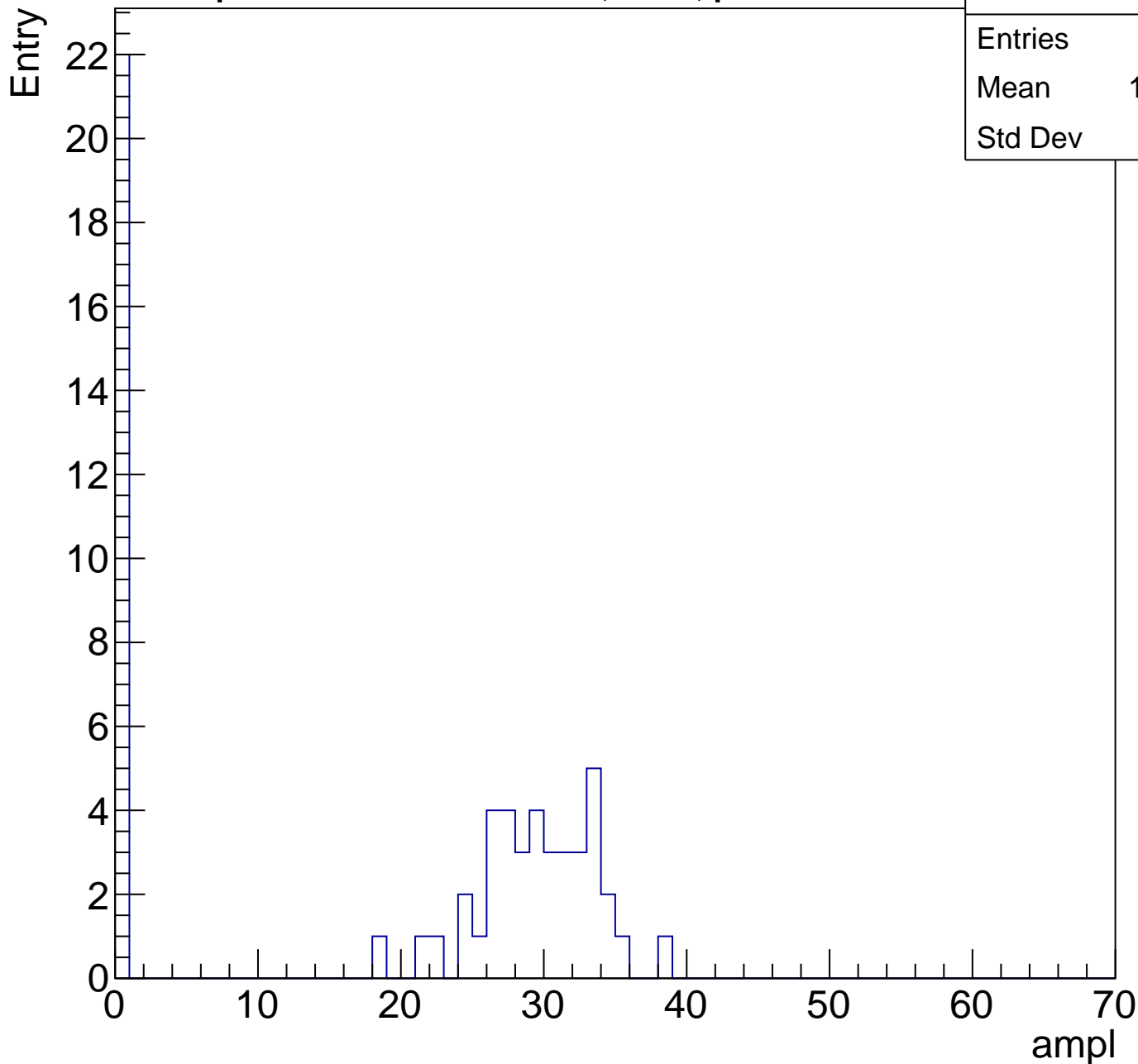
Entry



B1L103S, U14-ch37, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	61
Mean	18.54
Std Dev	14.3

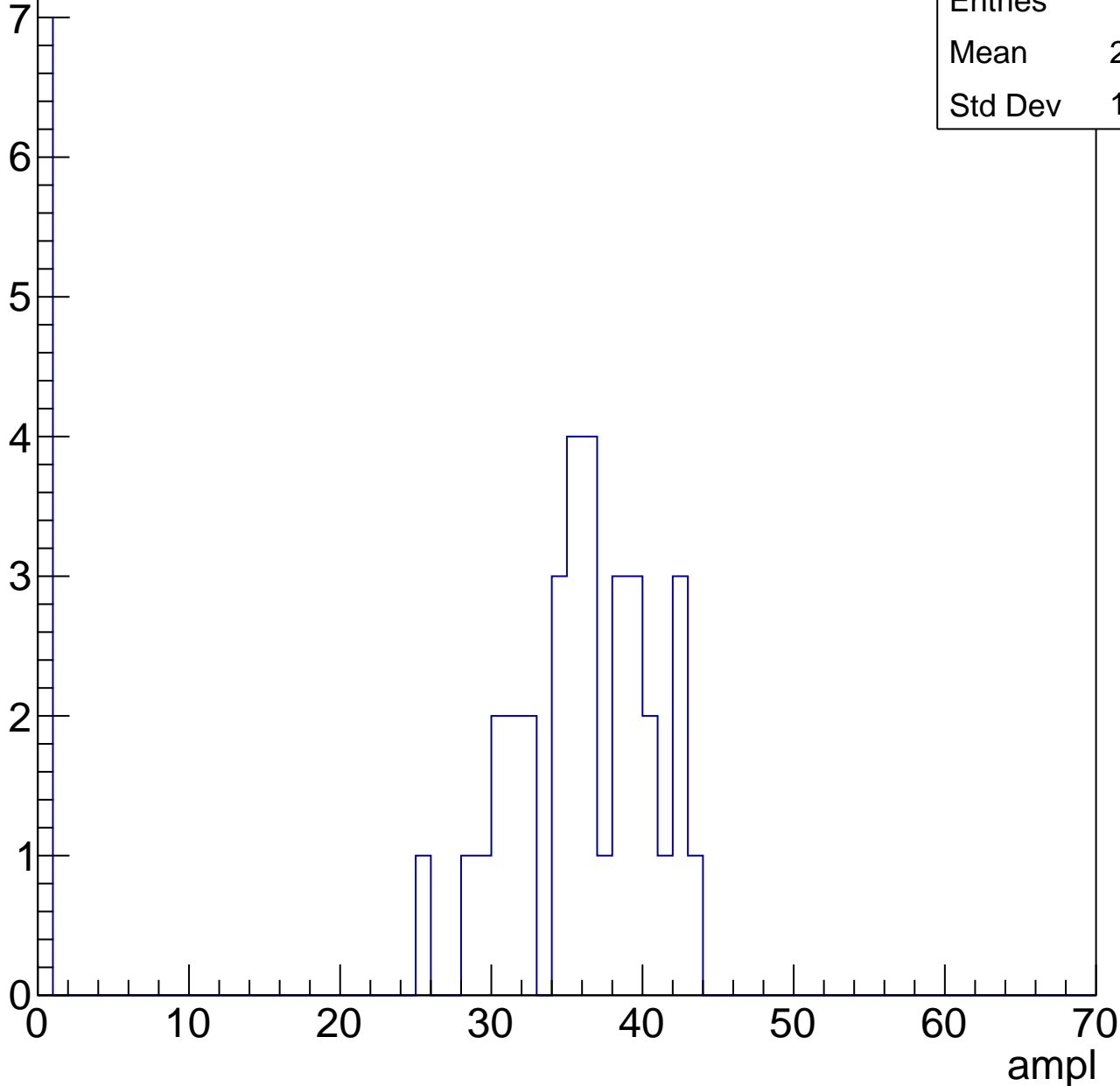


B1L103S, U14-ch37, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

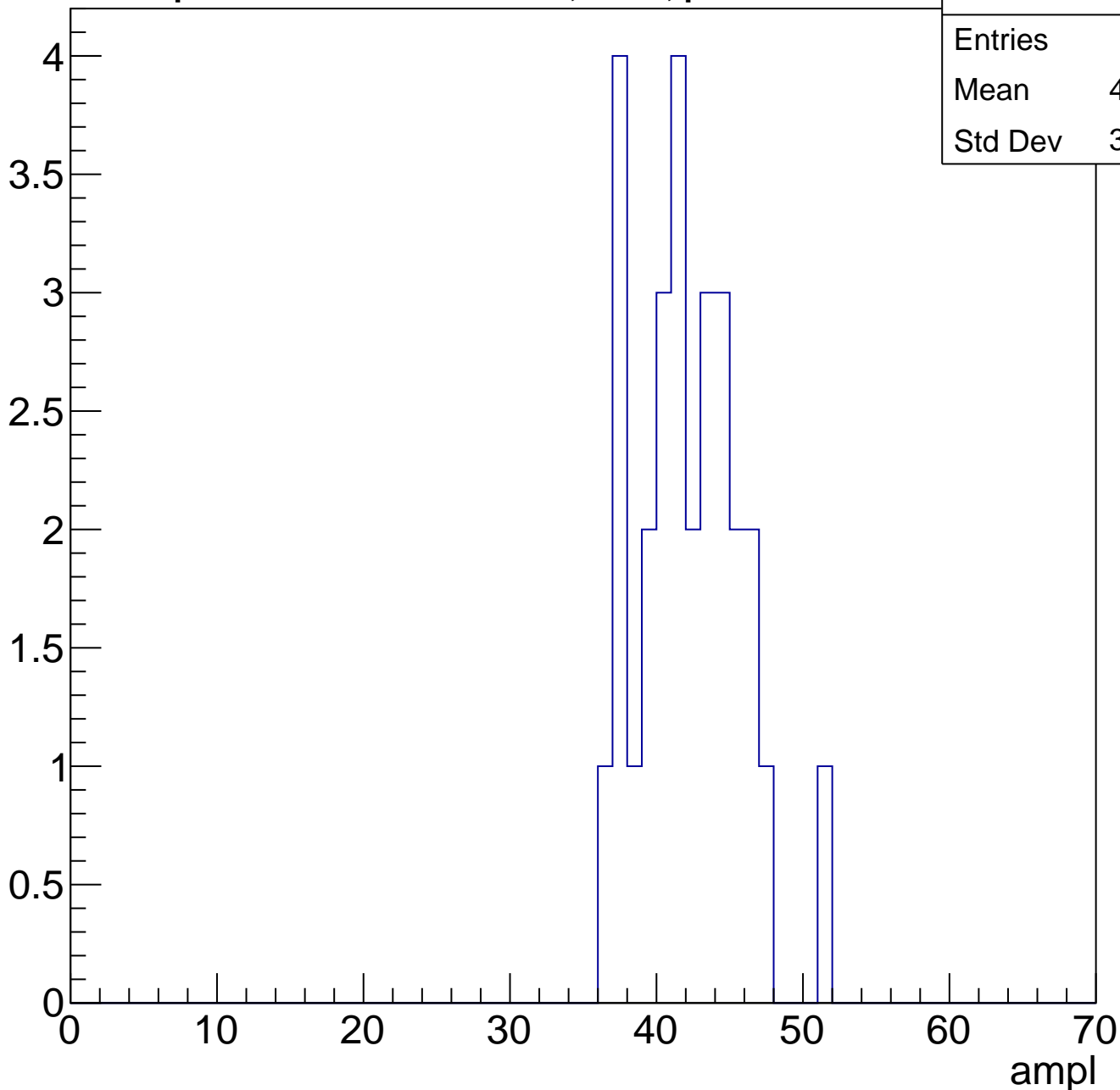
Entries	41
Mean	29.56
Std Dev	13.99



B1L103S, U14-ch37, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

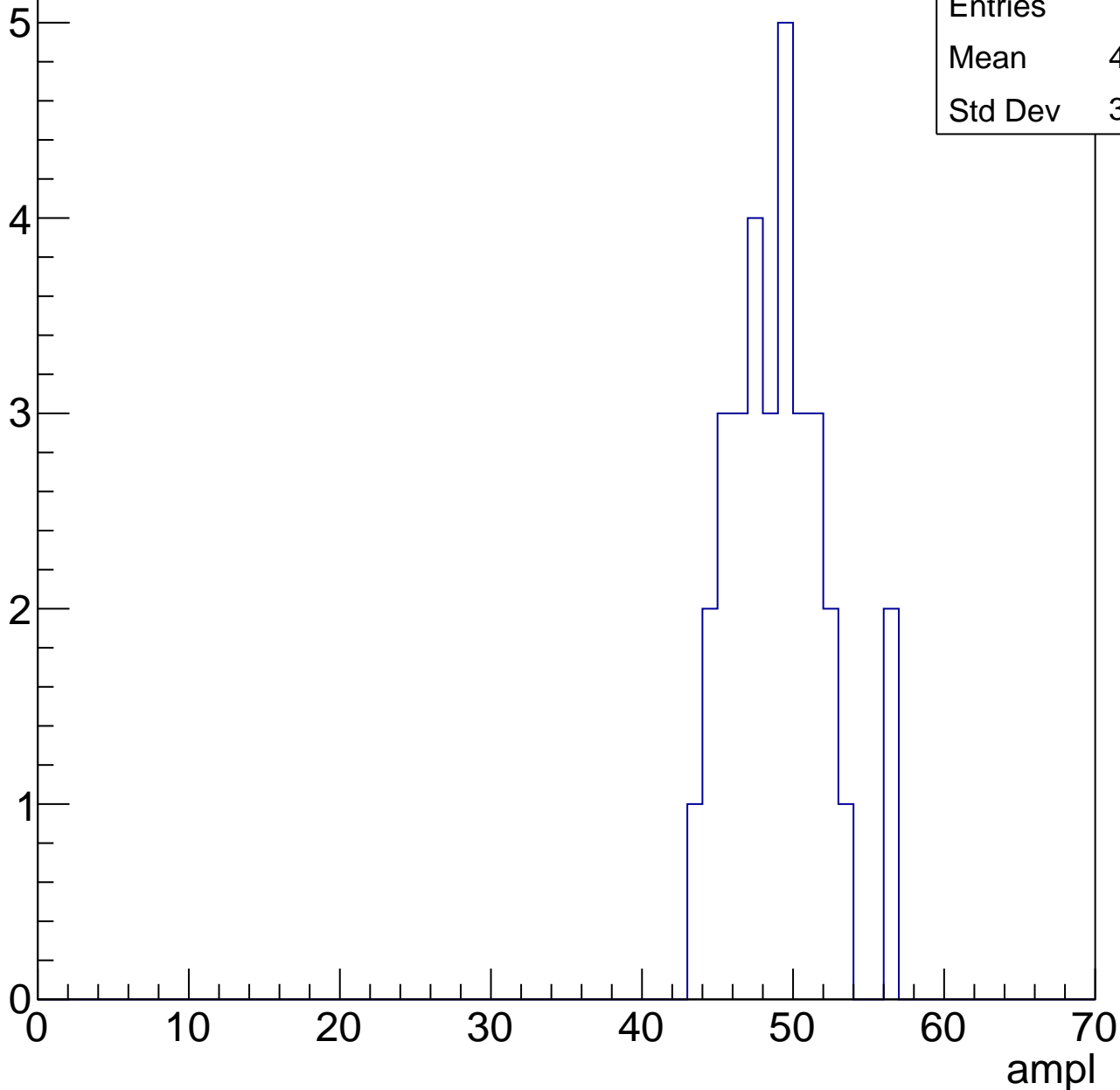


B1L103S, U14-ch37, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	32
Mean	48.53
Std Dev	3.162

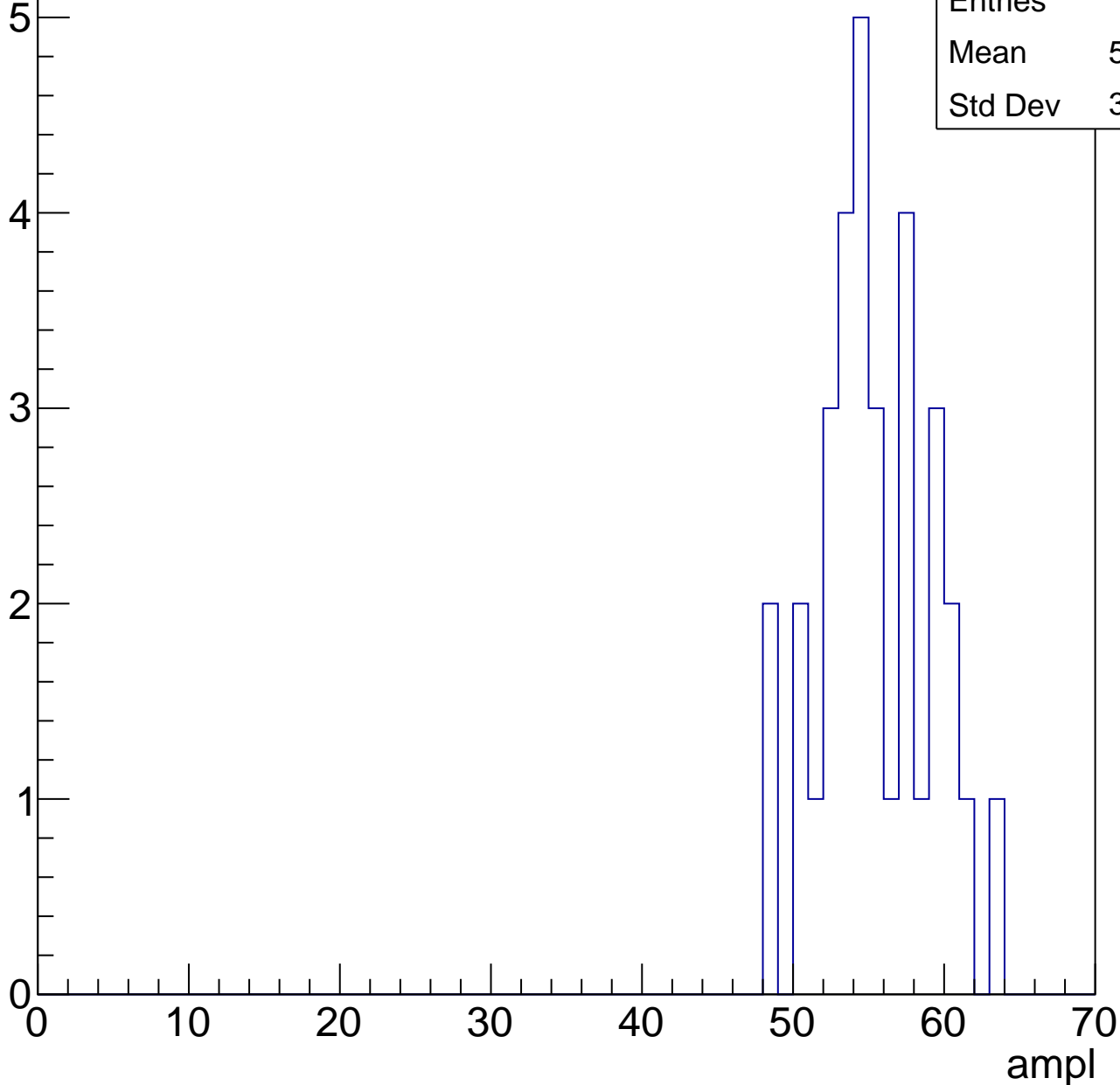


B1L103S, U14-ch37, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

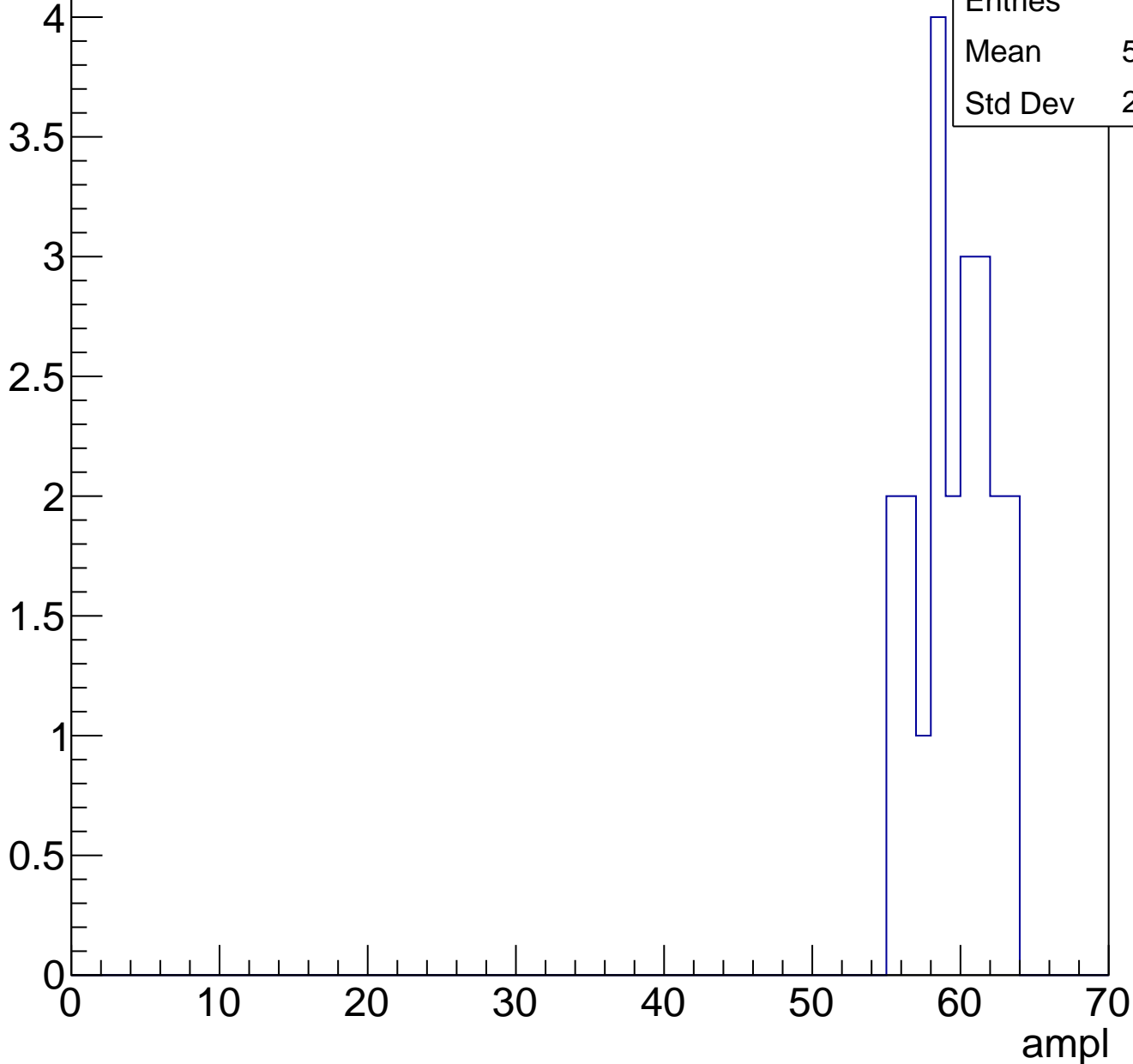
Entries	33
Mean	54.94
Std Dev	3.634



B1L103S, U14-ch37, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch37, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

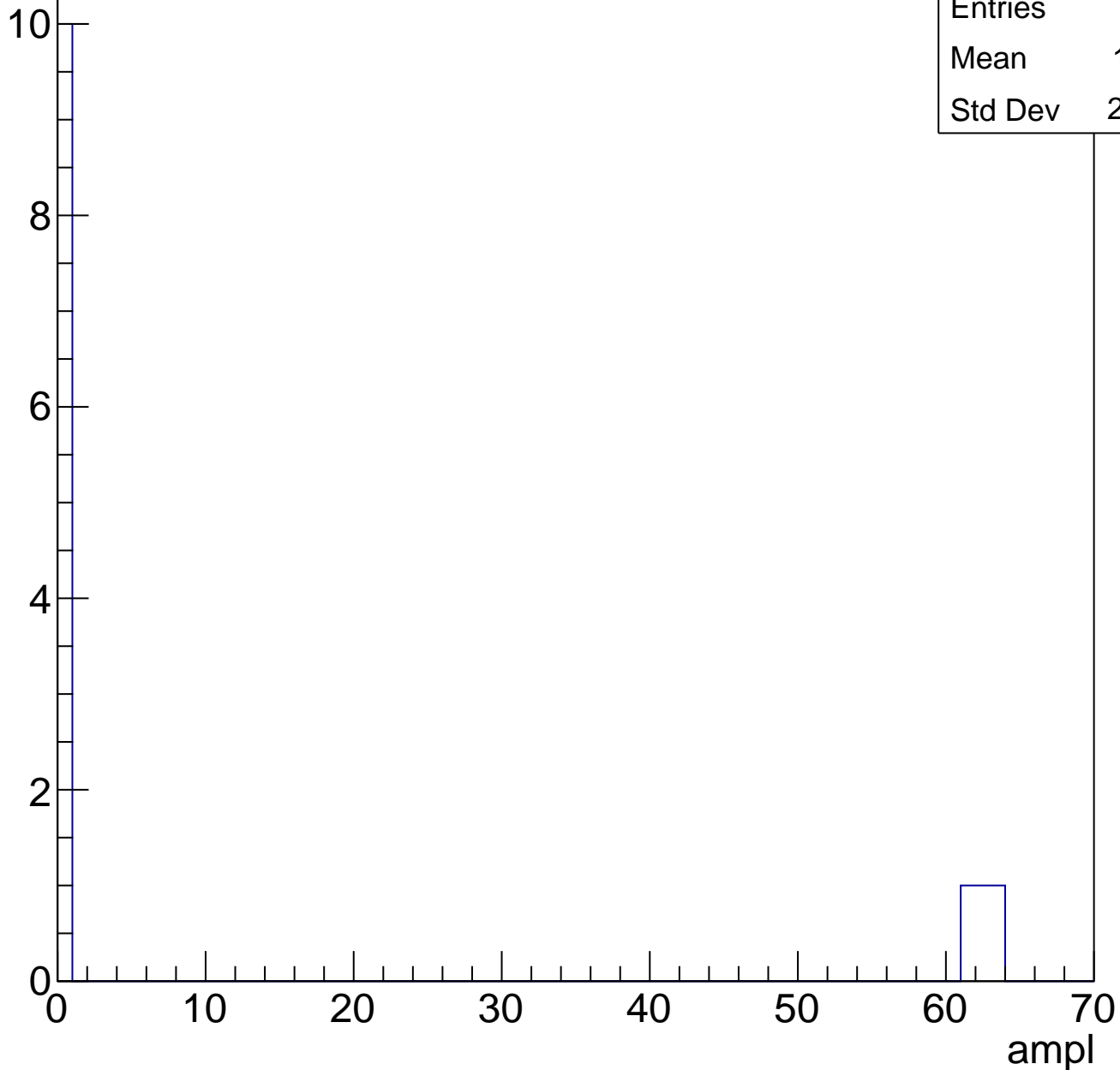


B1L103S, U14-ch37, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	13
Mean	14.31
Std Dev	26.13

Entry

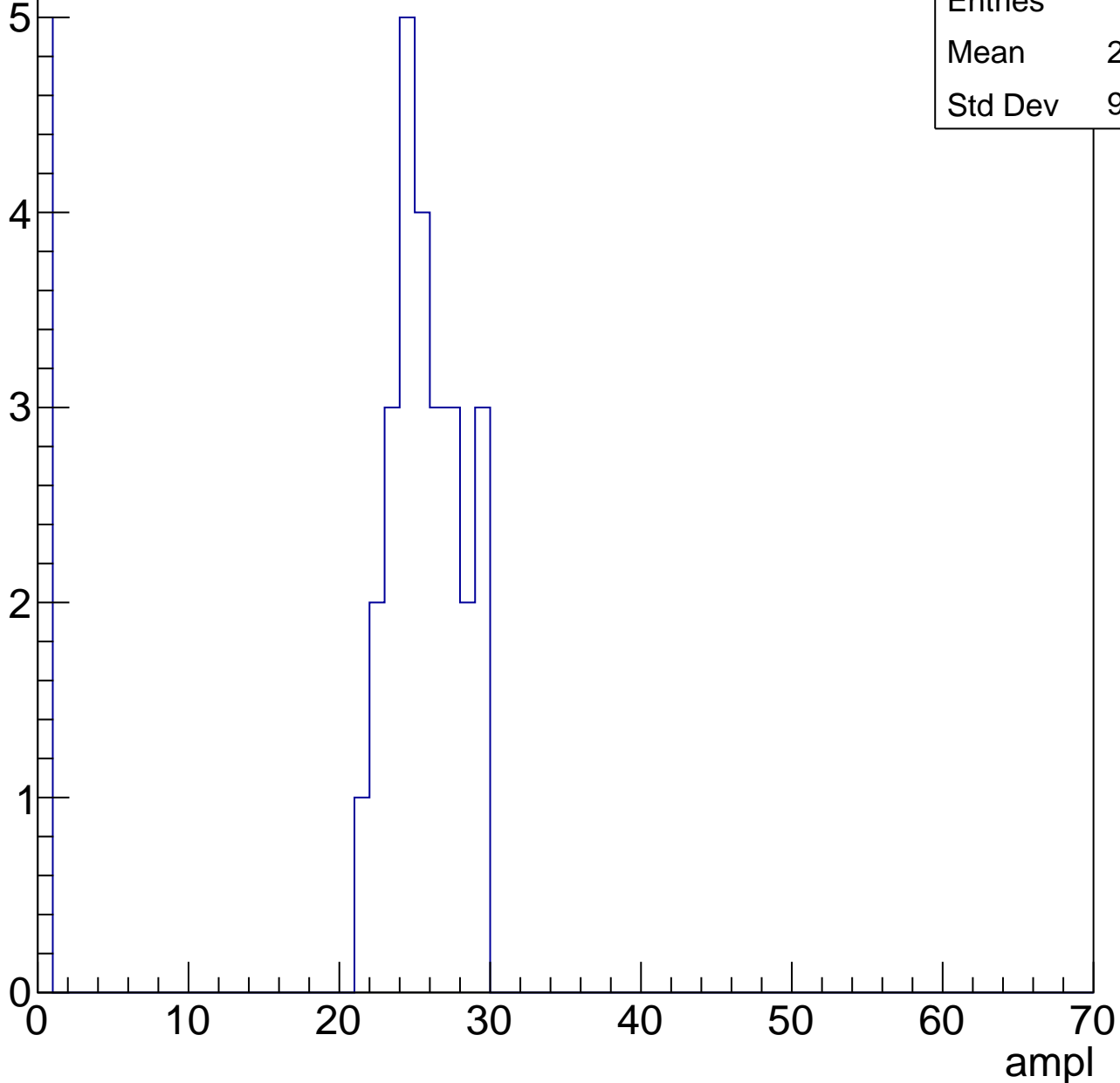


B1L103S, U14-ch38, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	31
Mean	21.16
Std Dev	9.504

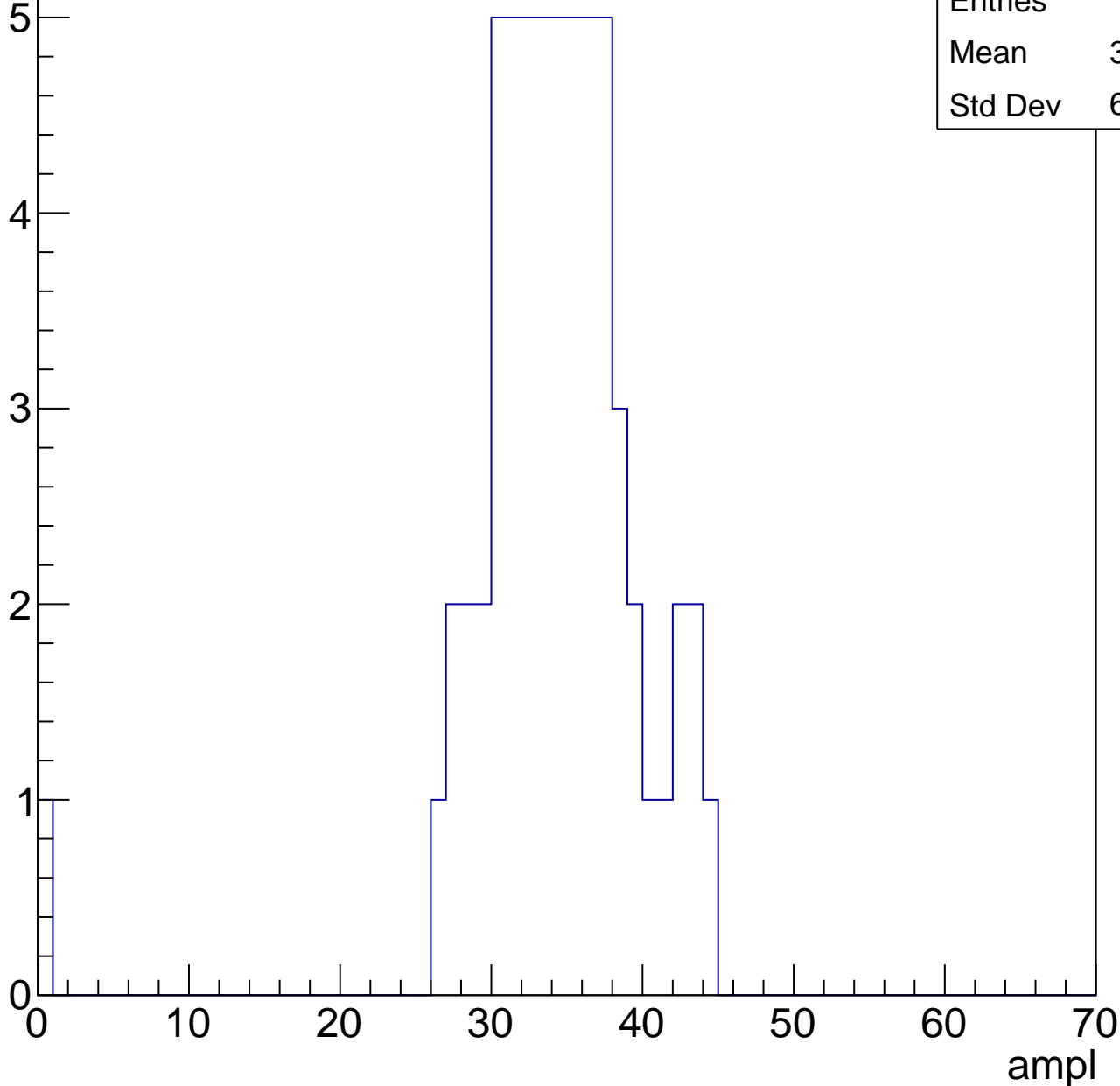


B1L103S, U14-ch38, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

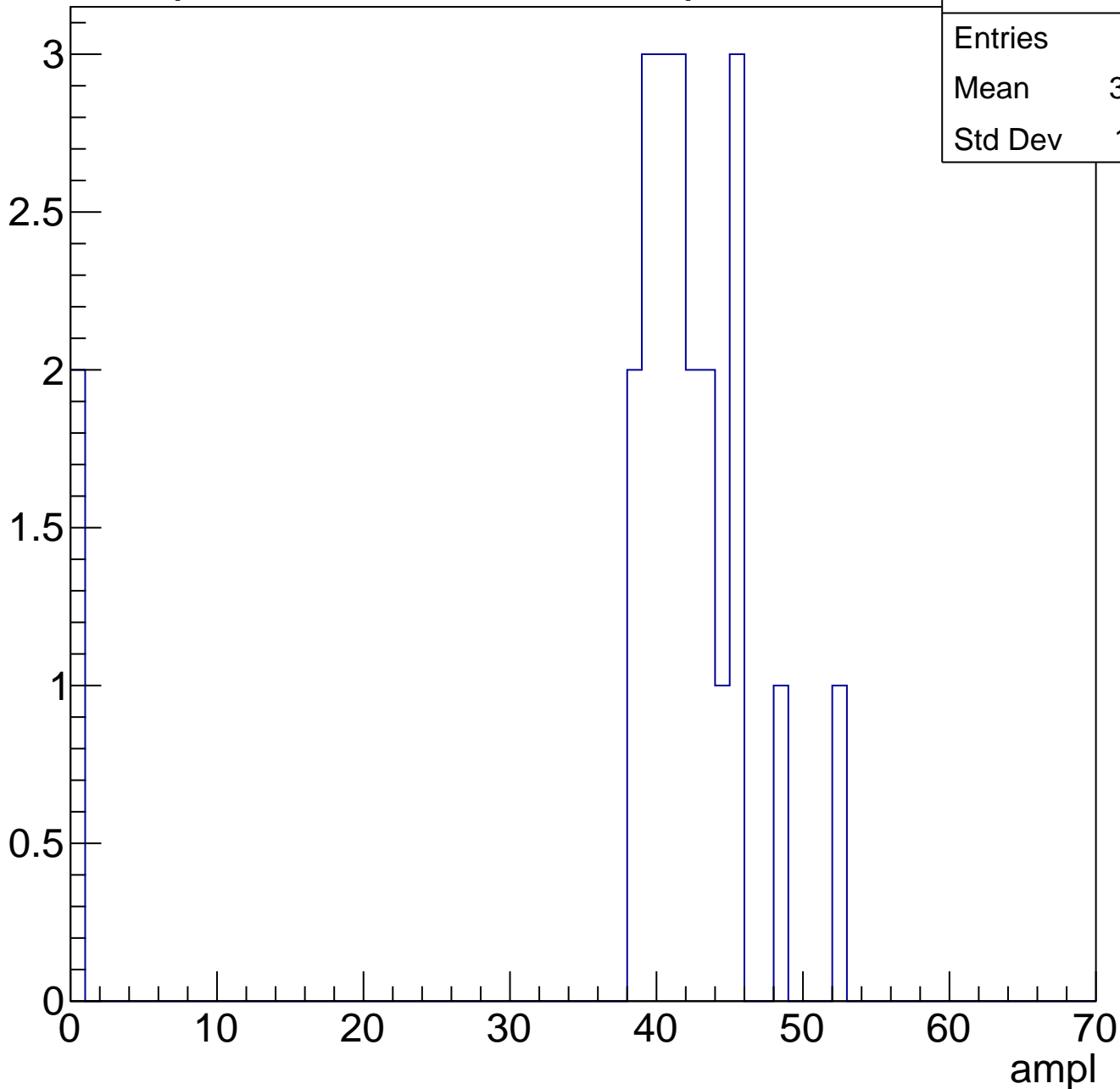
Entries	60
Mean	33.68
Std Dev	6.092



B1L103S, U14-ch38, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry



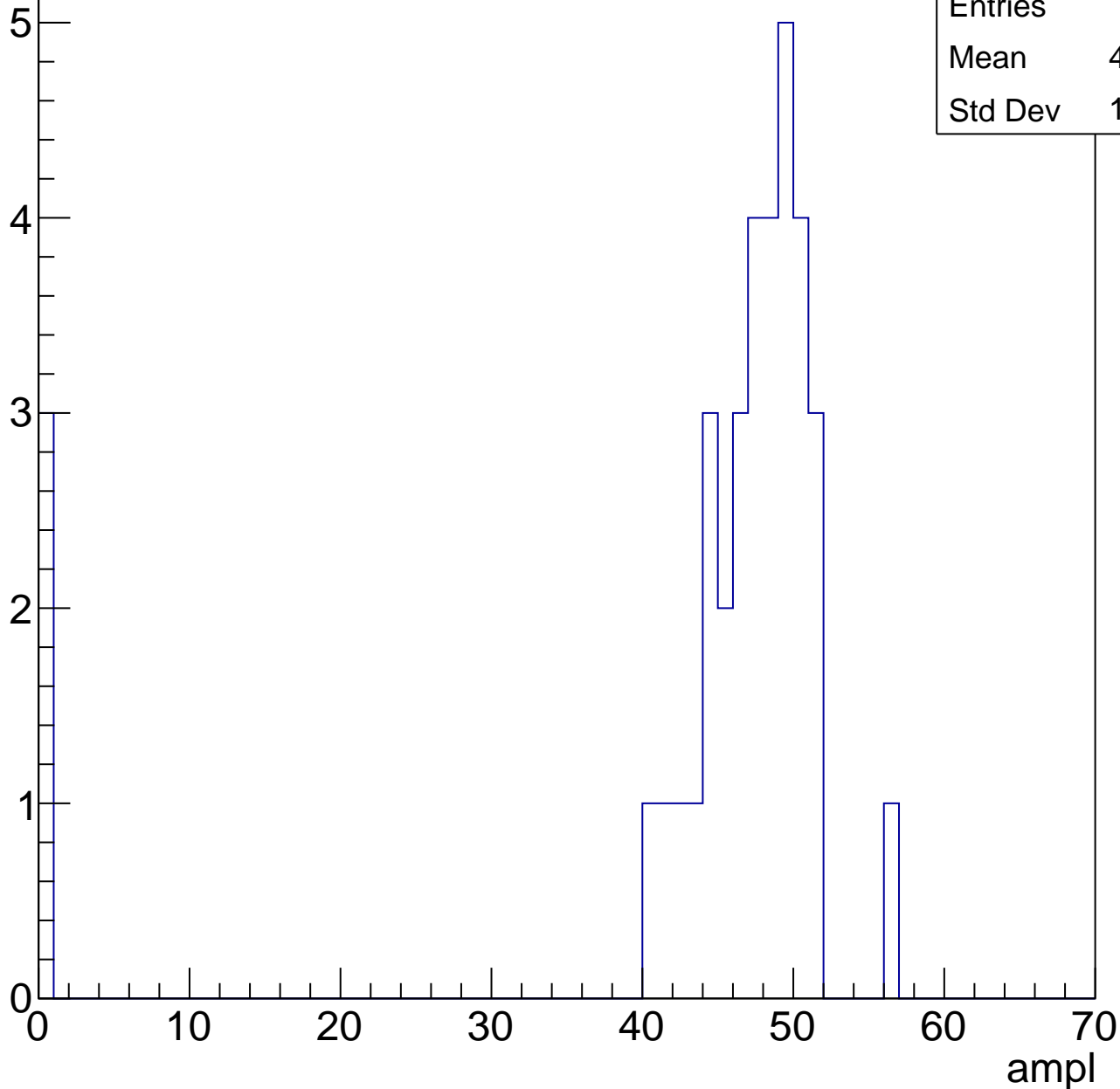
Entries	23
Mean	38.48
Std Dev	12.31

B1L103S, U14-ch38, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	36
Mean	43.33
Std Dev	13.43

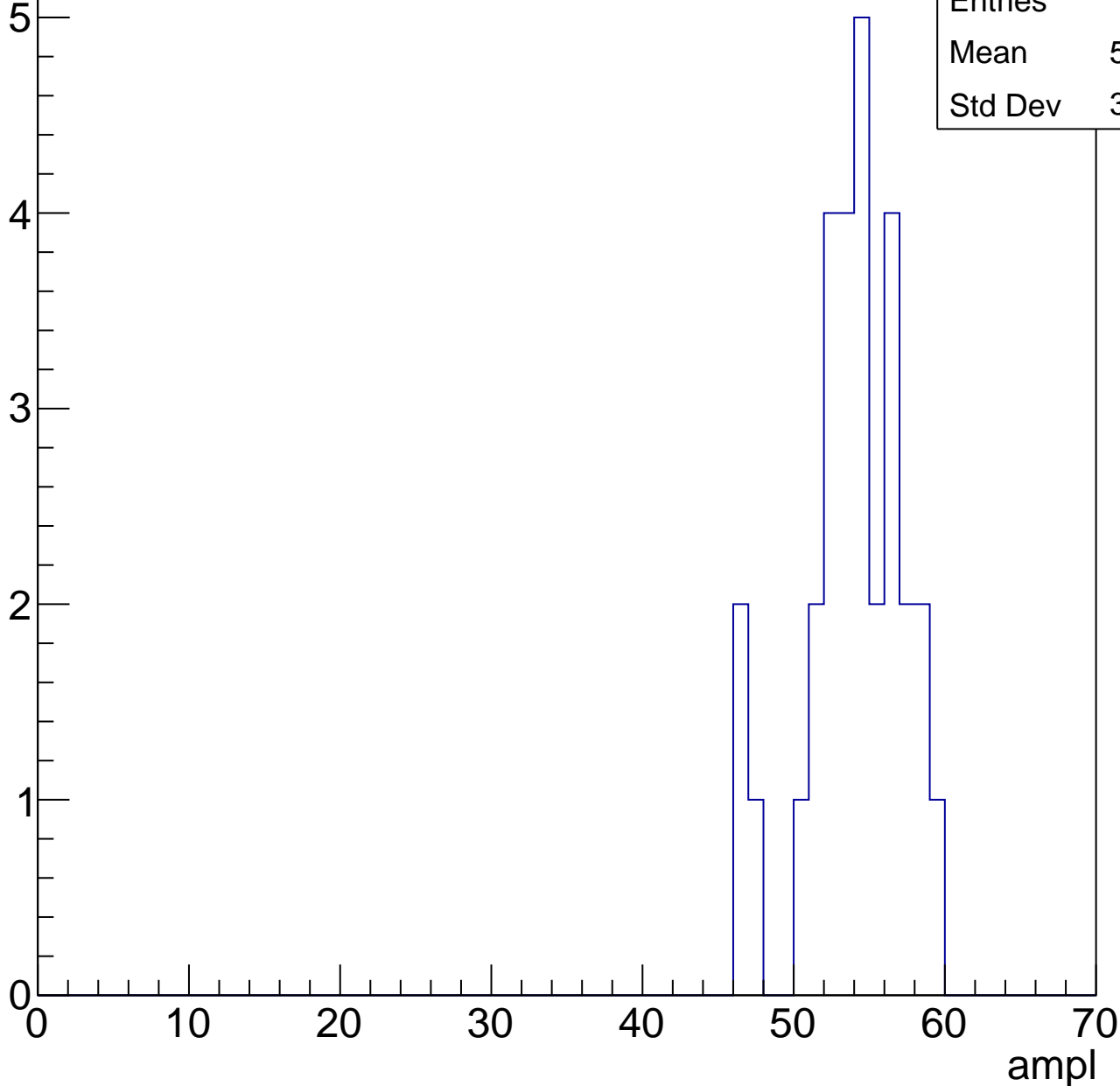


B1L103S, U14-ch38, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

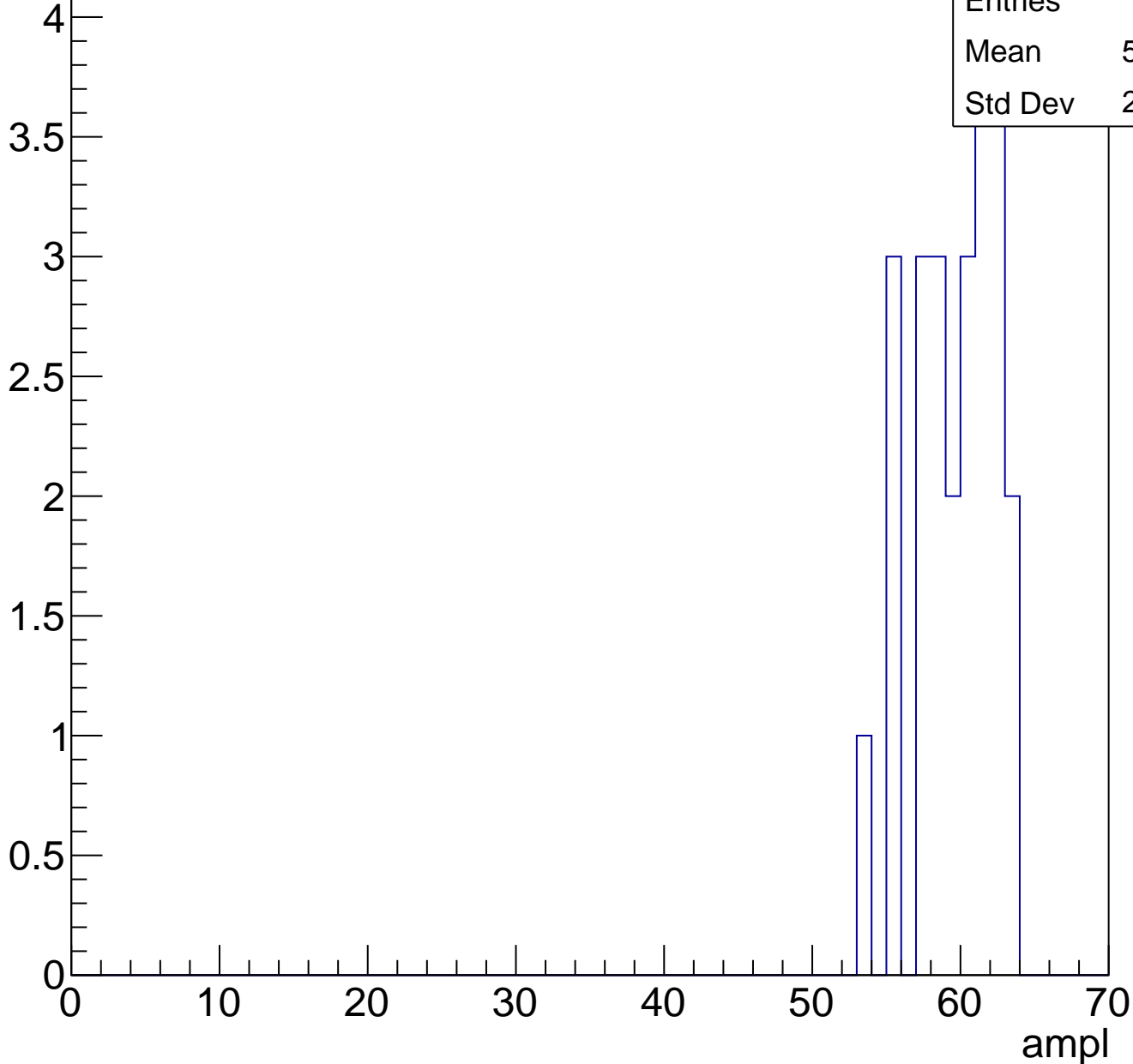
Entries	30
Mean	53.47
Std Dev	3.243



B1L103S, U14-ch38, adc5

calib_packv5_041523_1651.root, FC#0, port C2

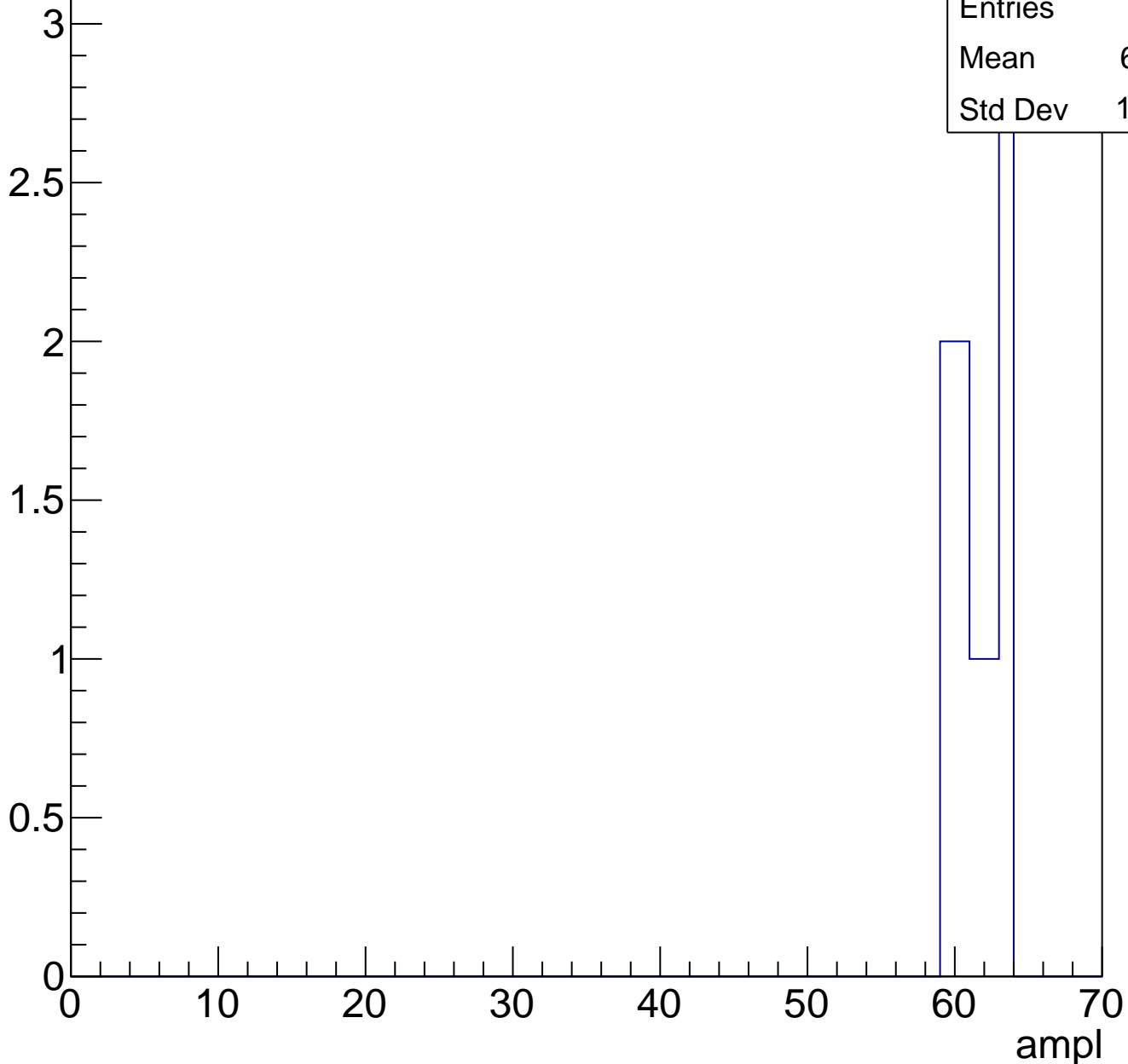
Entry



B1L103S, U14-ch38, adc6

calib_packv5_041523_1651.root, FC#0, port C2

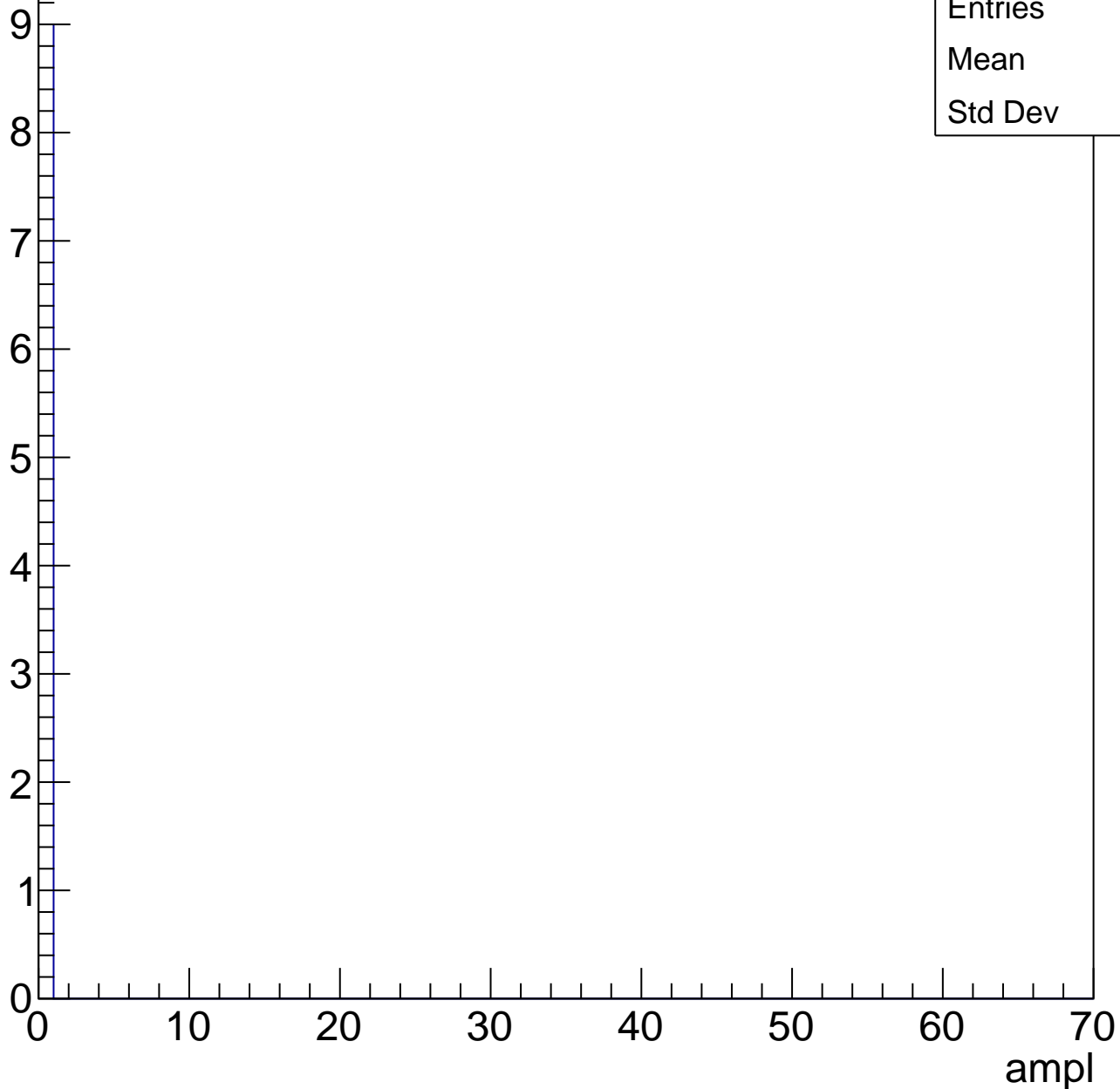
Entry



B1L103S, U14-ch38, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

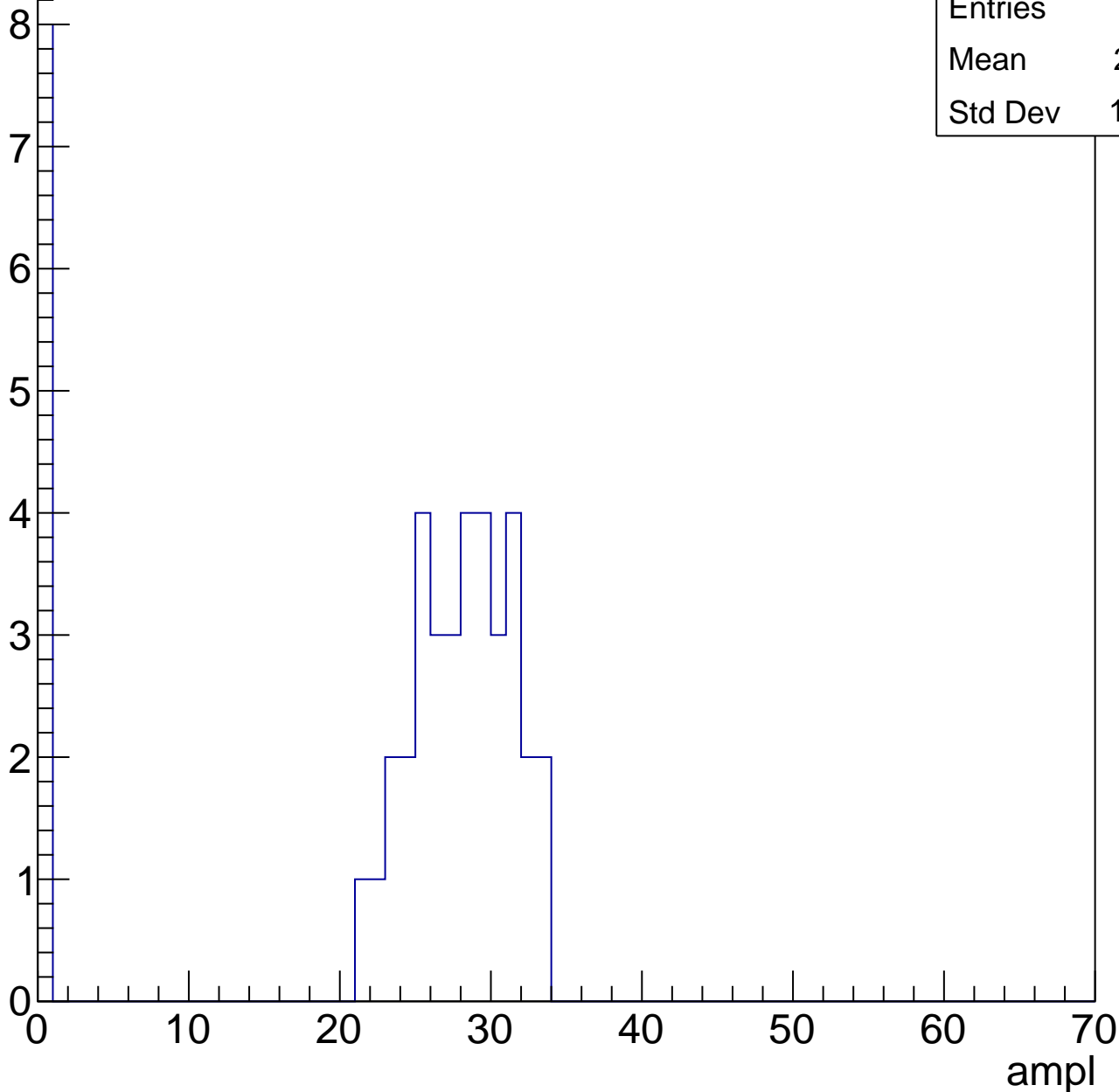


B1L103S, U14-ch39, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	43
Mean	22.51
Std Dev	11.13

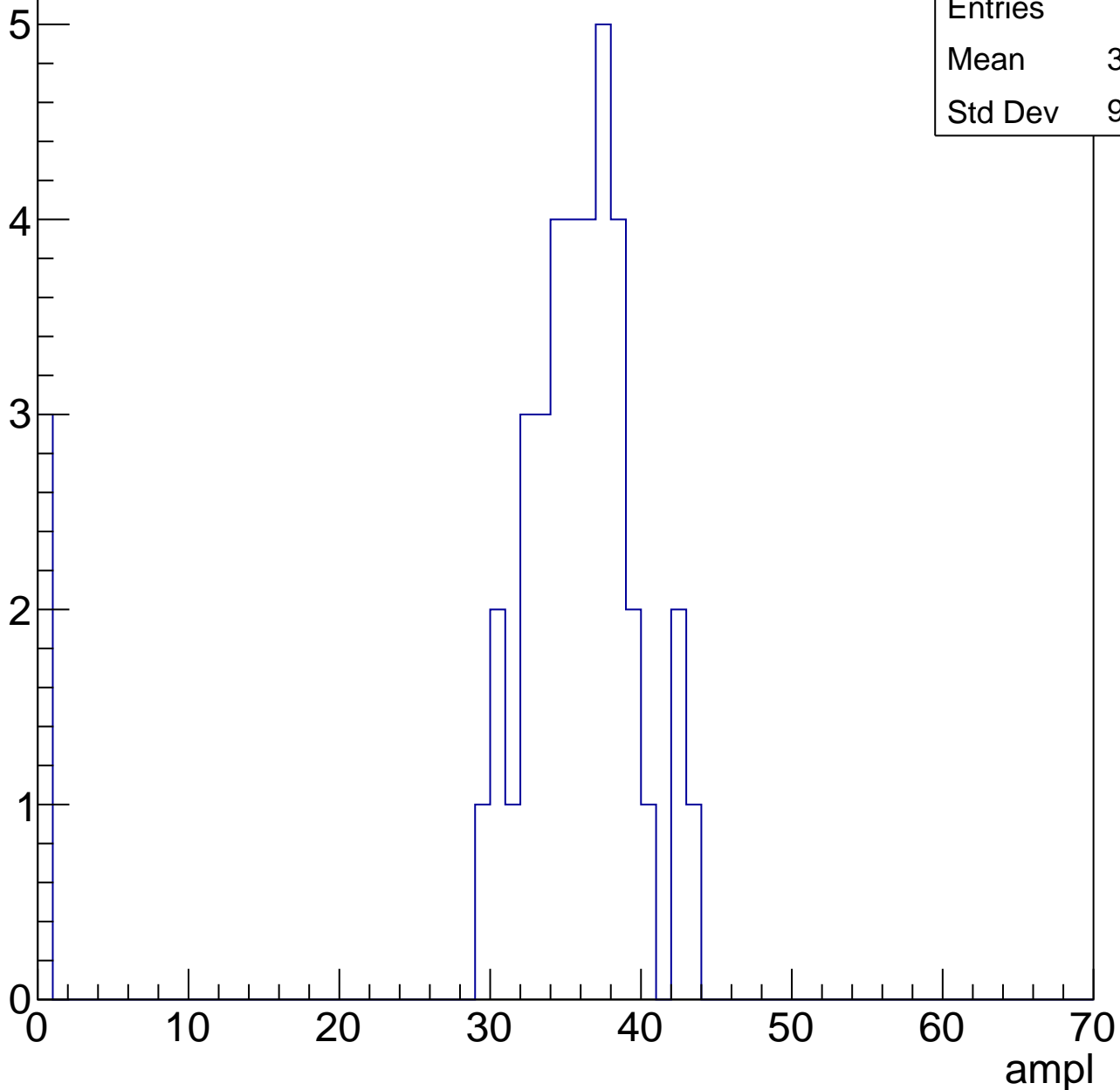


B1L103S, U14-ch39, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

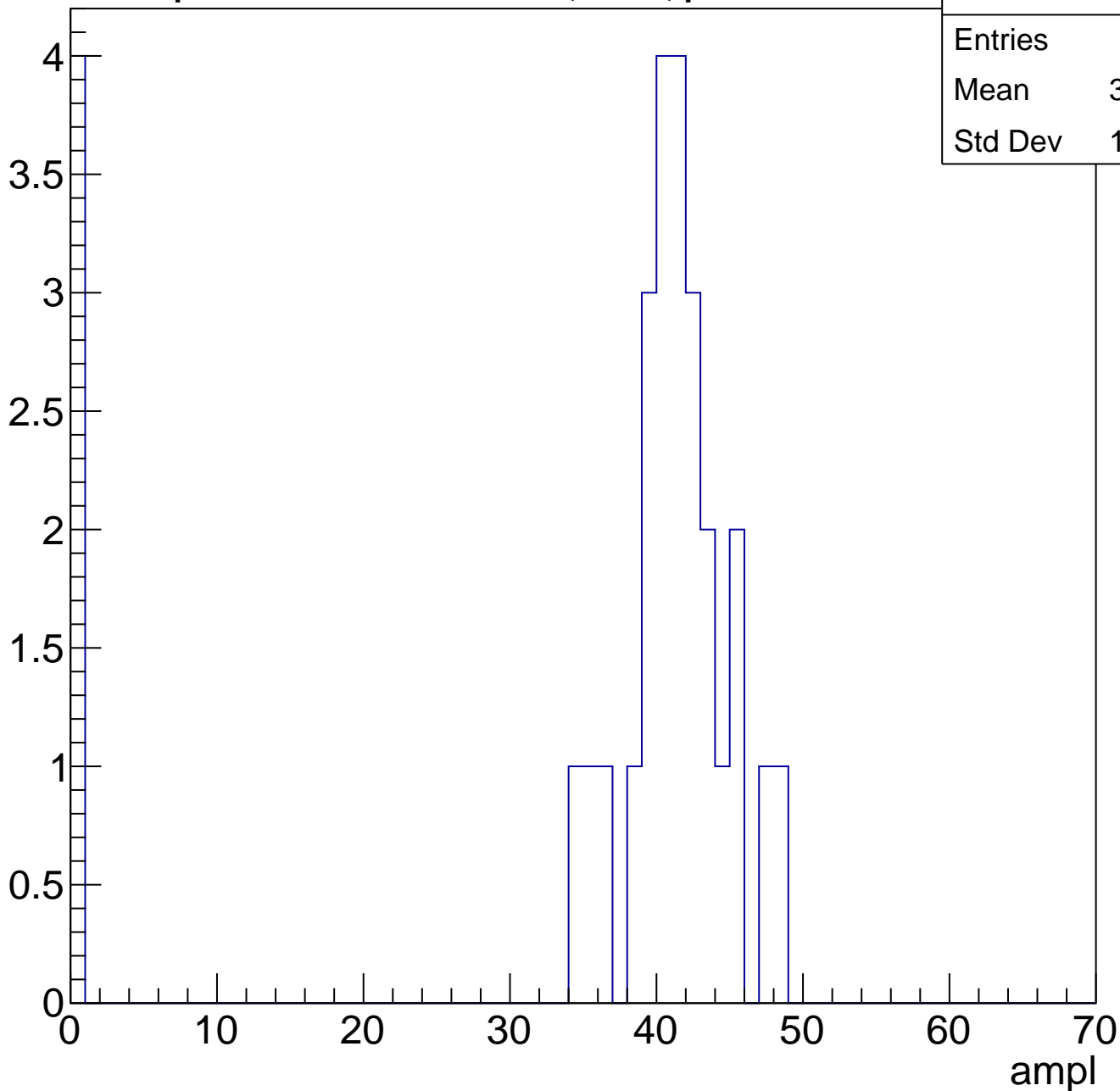
Entries	40
Mean	32.92
Std Dev	9.908



B1L103S, U14-ch39, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry



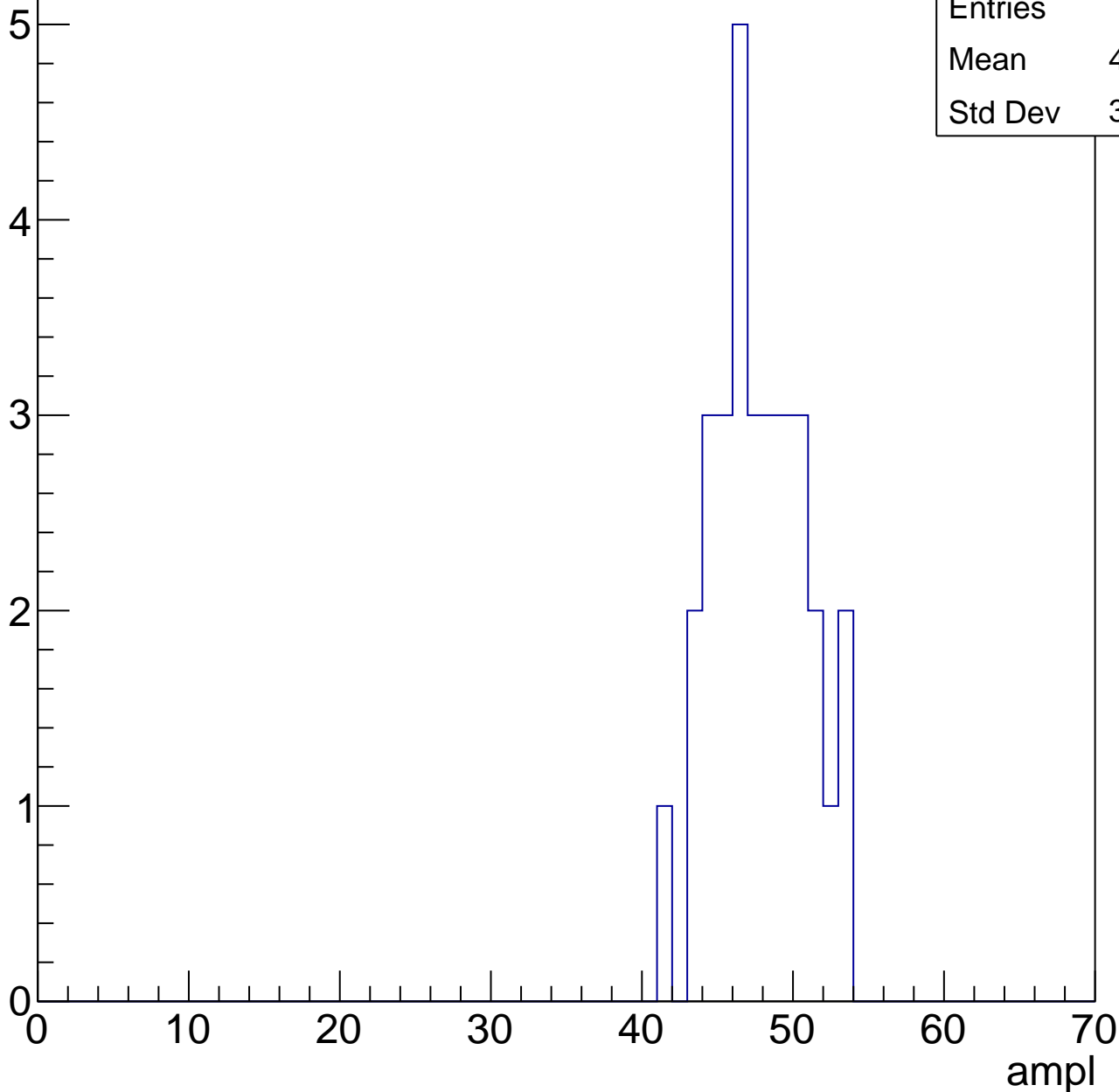
Entries	29
Mean	35.34
Std Dev	14.47

B1L103S, U14-ch39, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

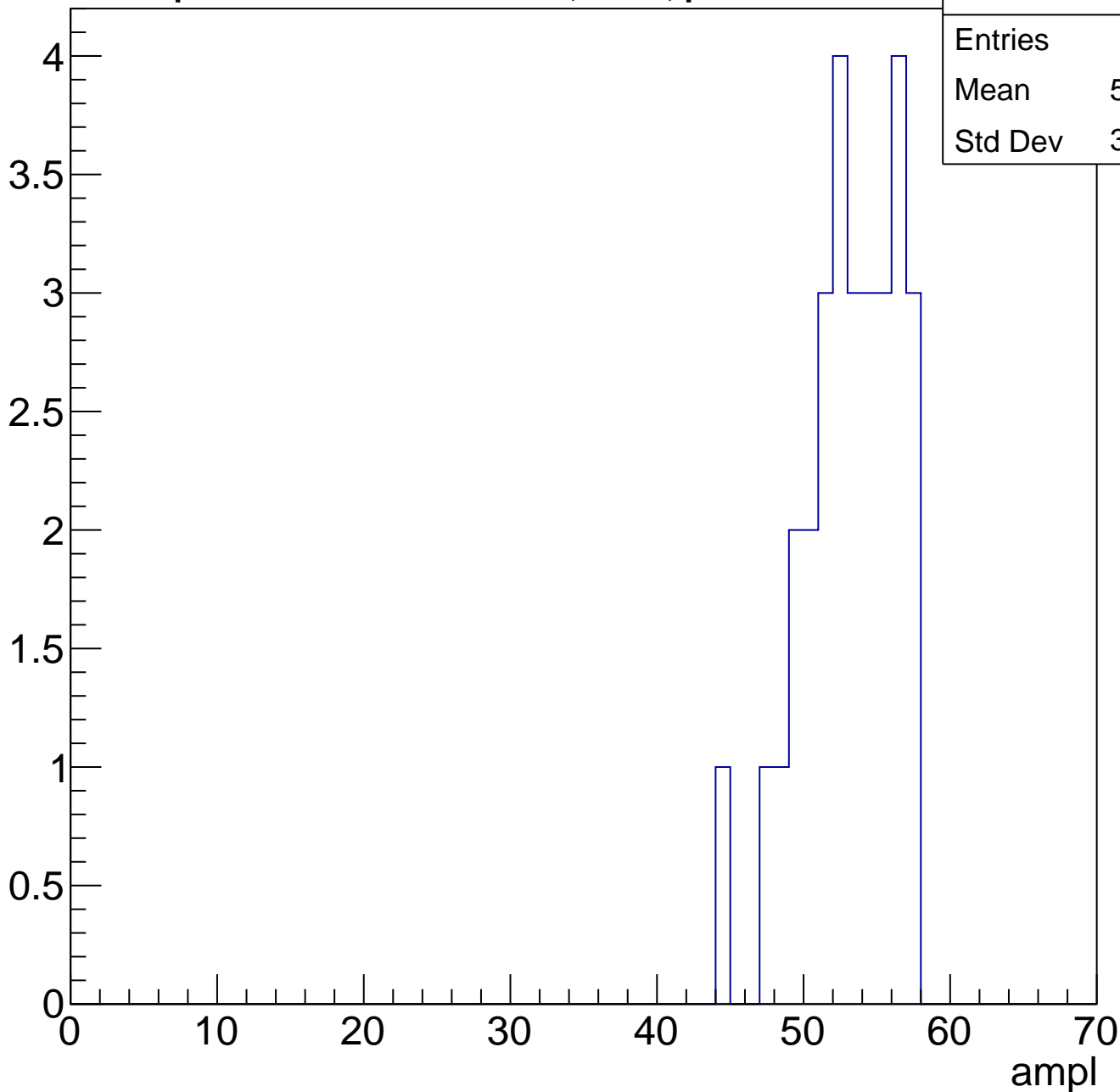
Entries	31
Mean	47.29
Std Dev	3.007



B1L103S, U14-ch39, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



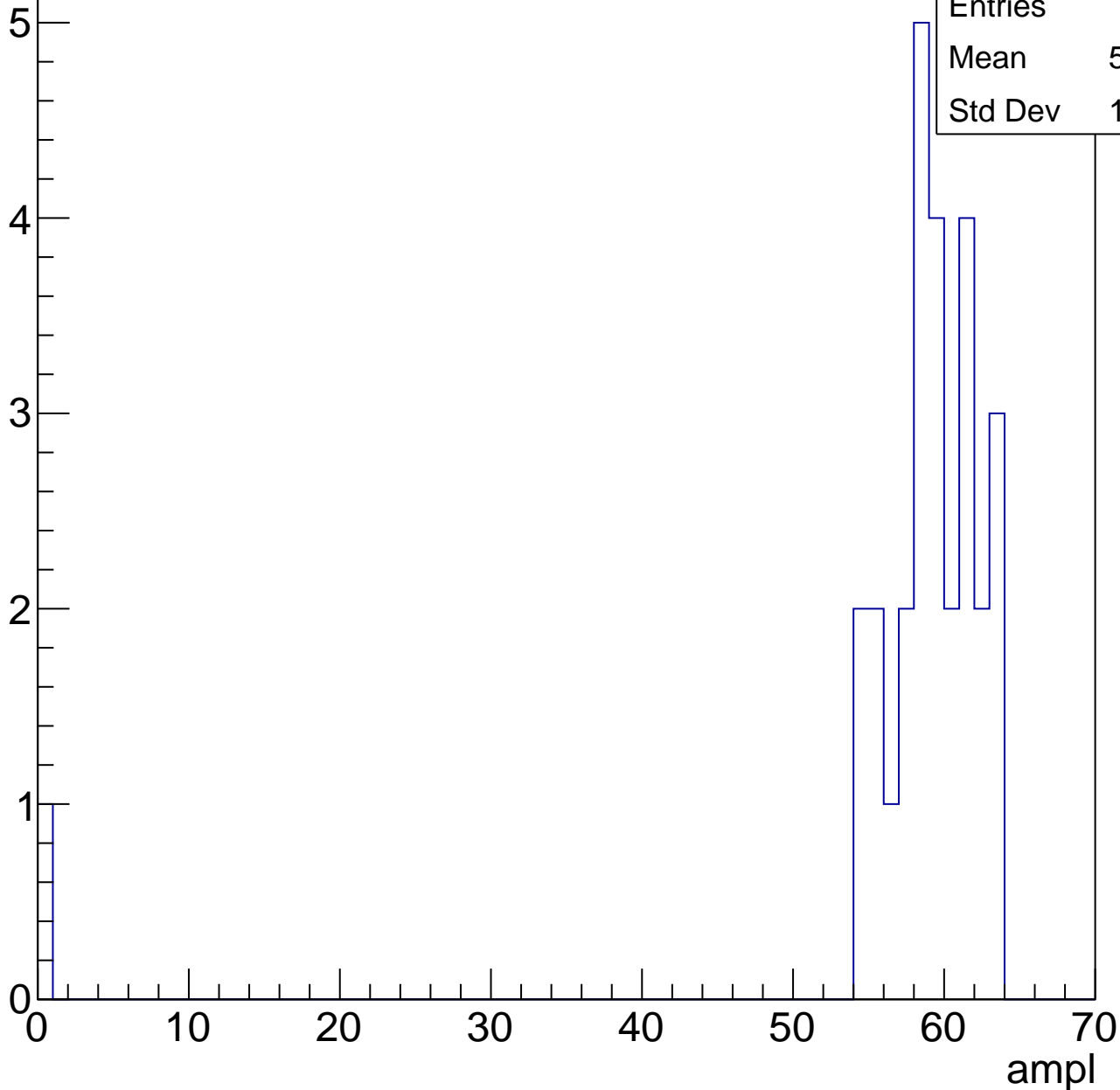
Entries	30
Mean	52.63
Std Dev	3.178

B1L103S, U14-ch39, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

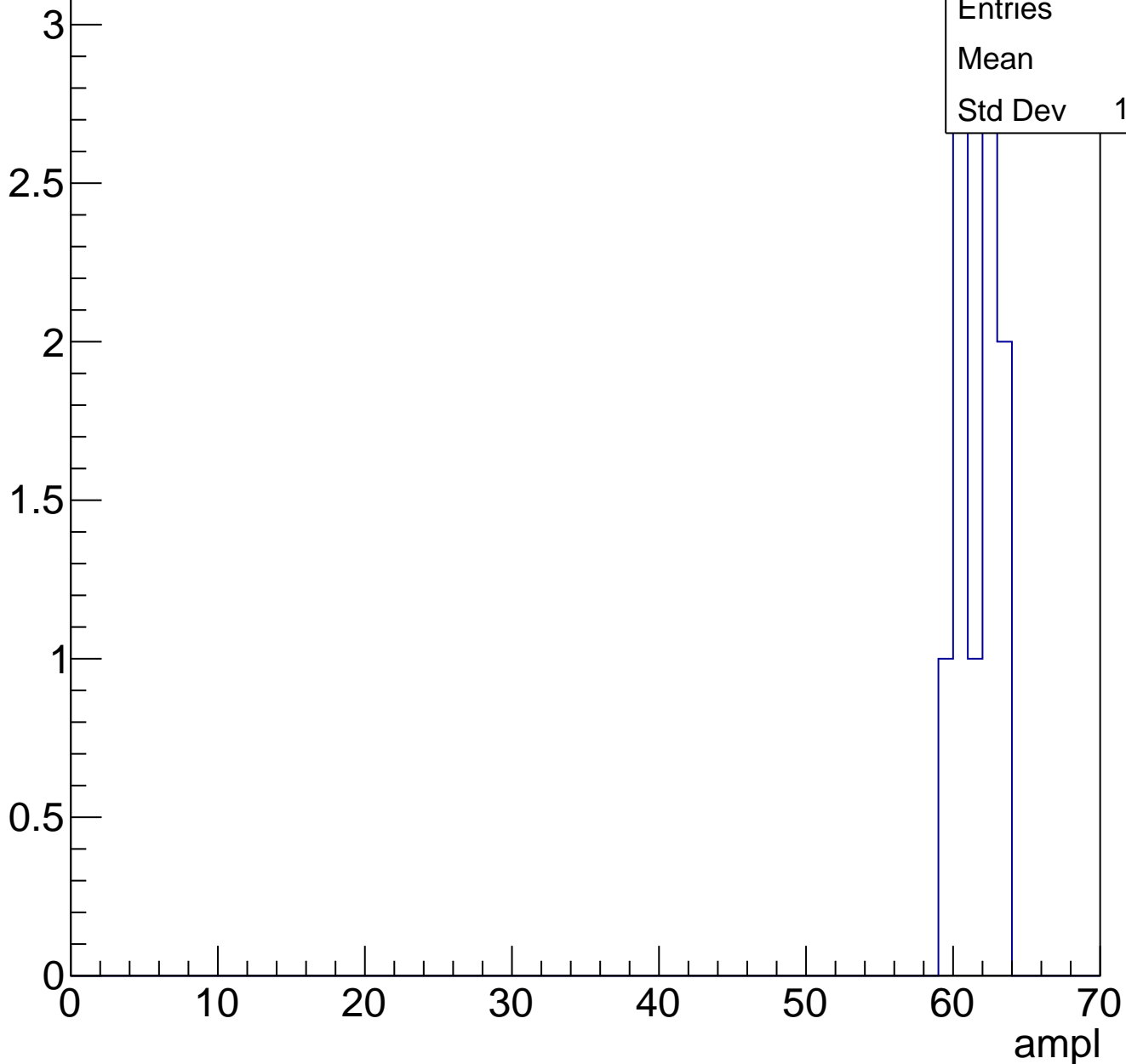
Entries	28
Mean	56.82
Std Dev	11.24



B1L103S, U14-ch39, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

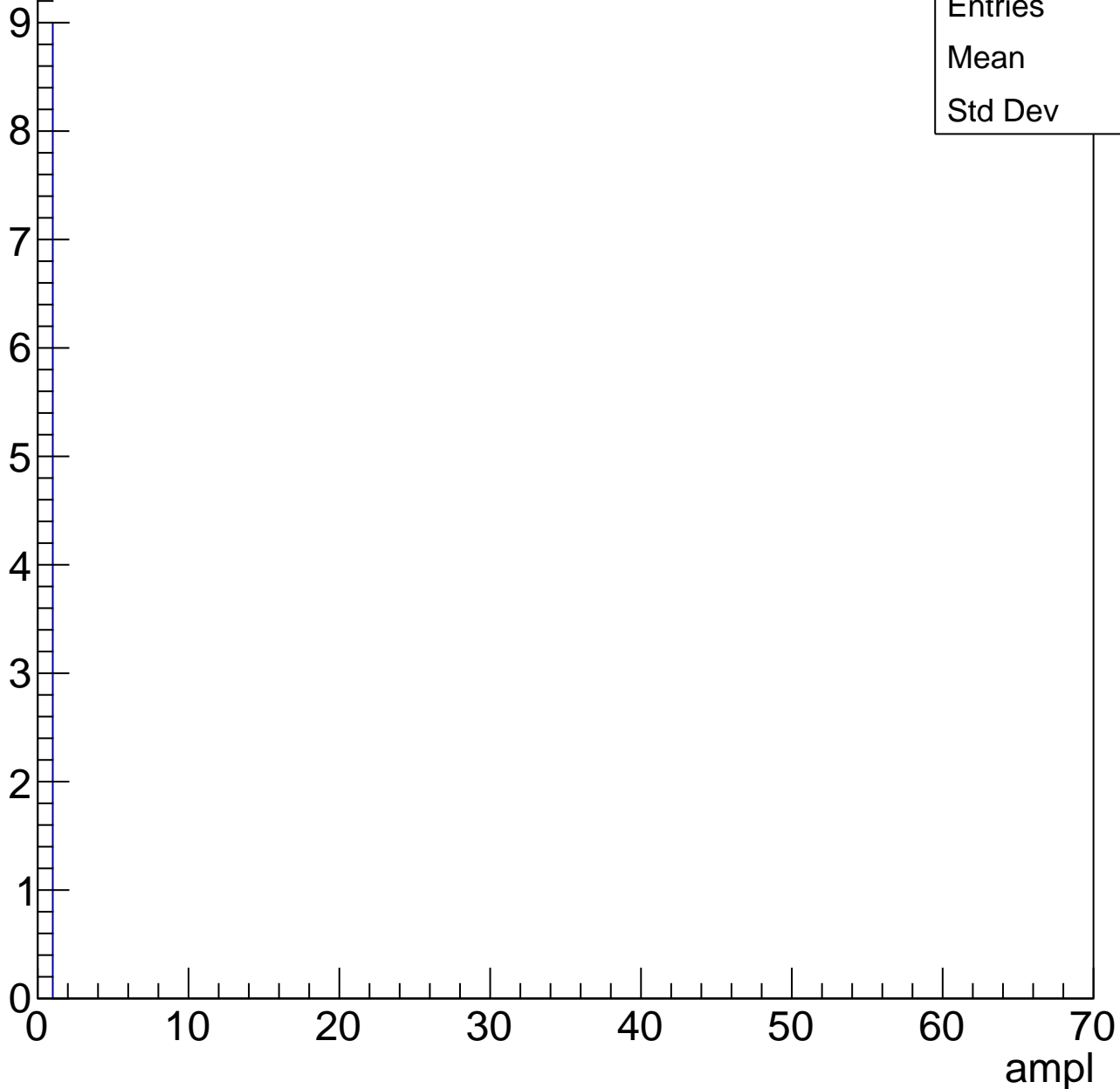


Entries	10
Mean	61.2
Std Dev	1.327

B1L103S, U14-ch39, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



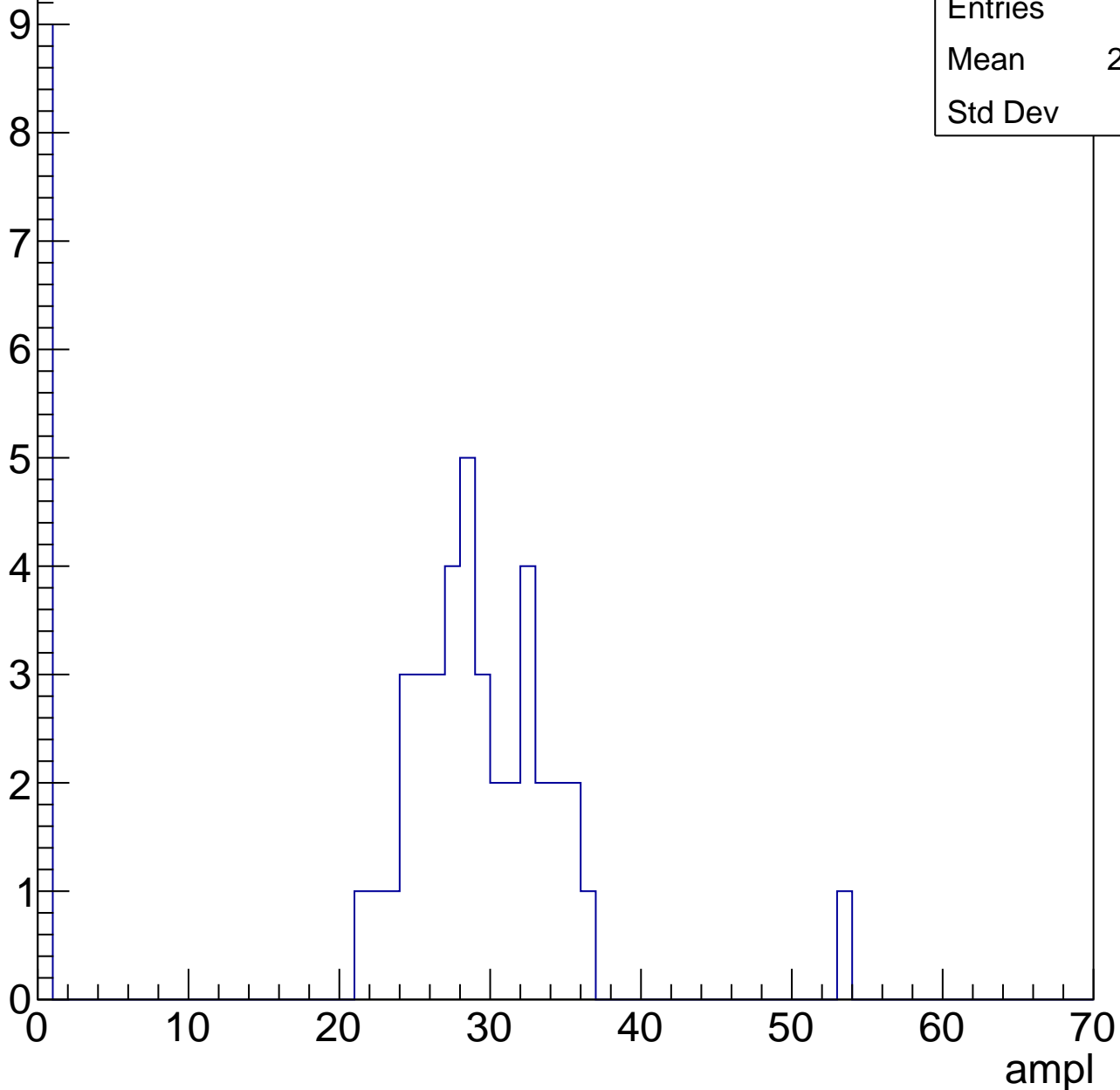
Entries	9
Mean	0
Std Dev	0

B1L103S, U14-ch40, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	23.86
Std Dev	12.3

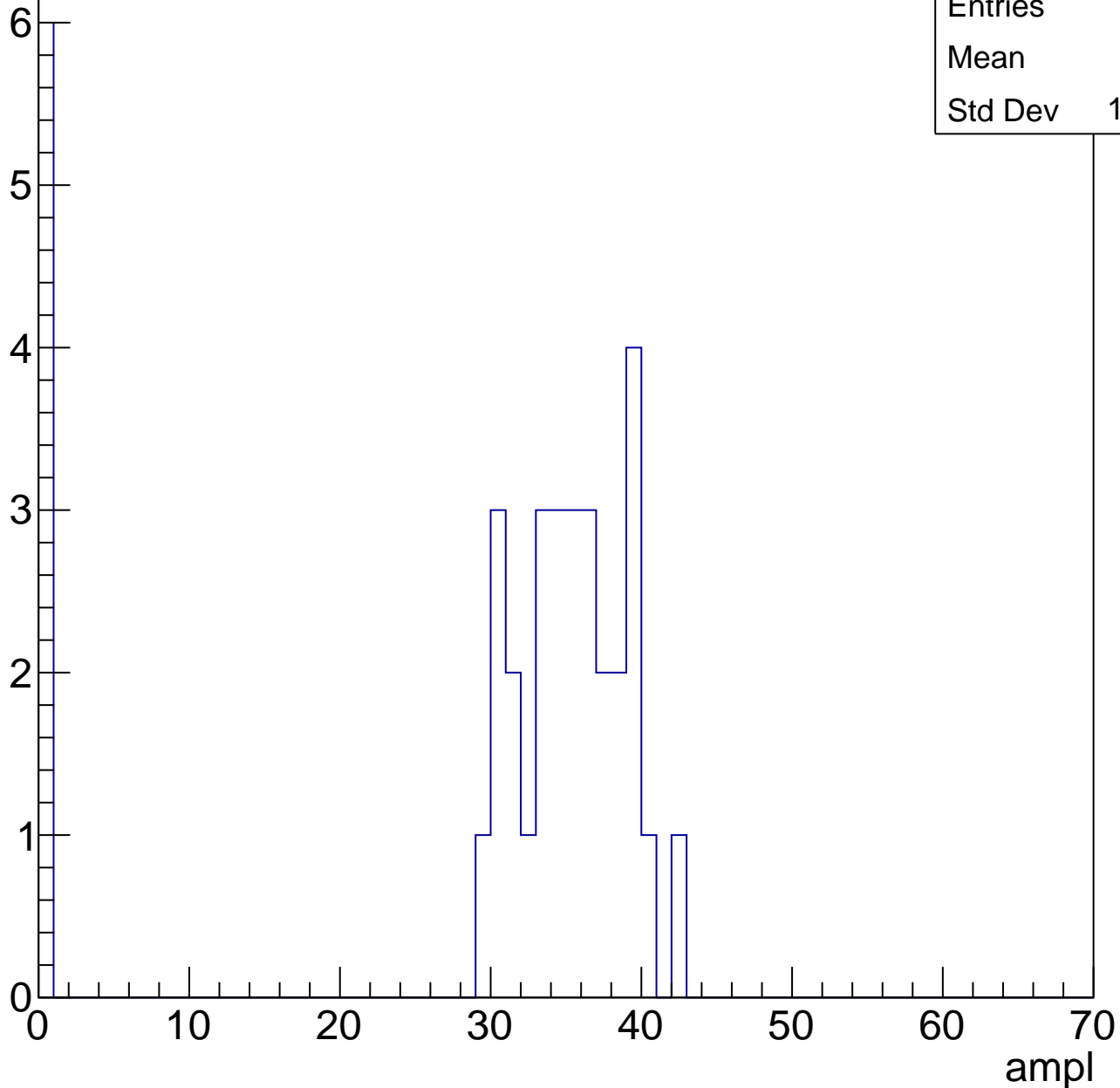


B1L103S, U14-ch40, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	35
Mean	29
Std Dev	13.55

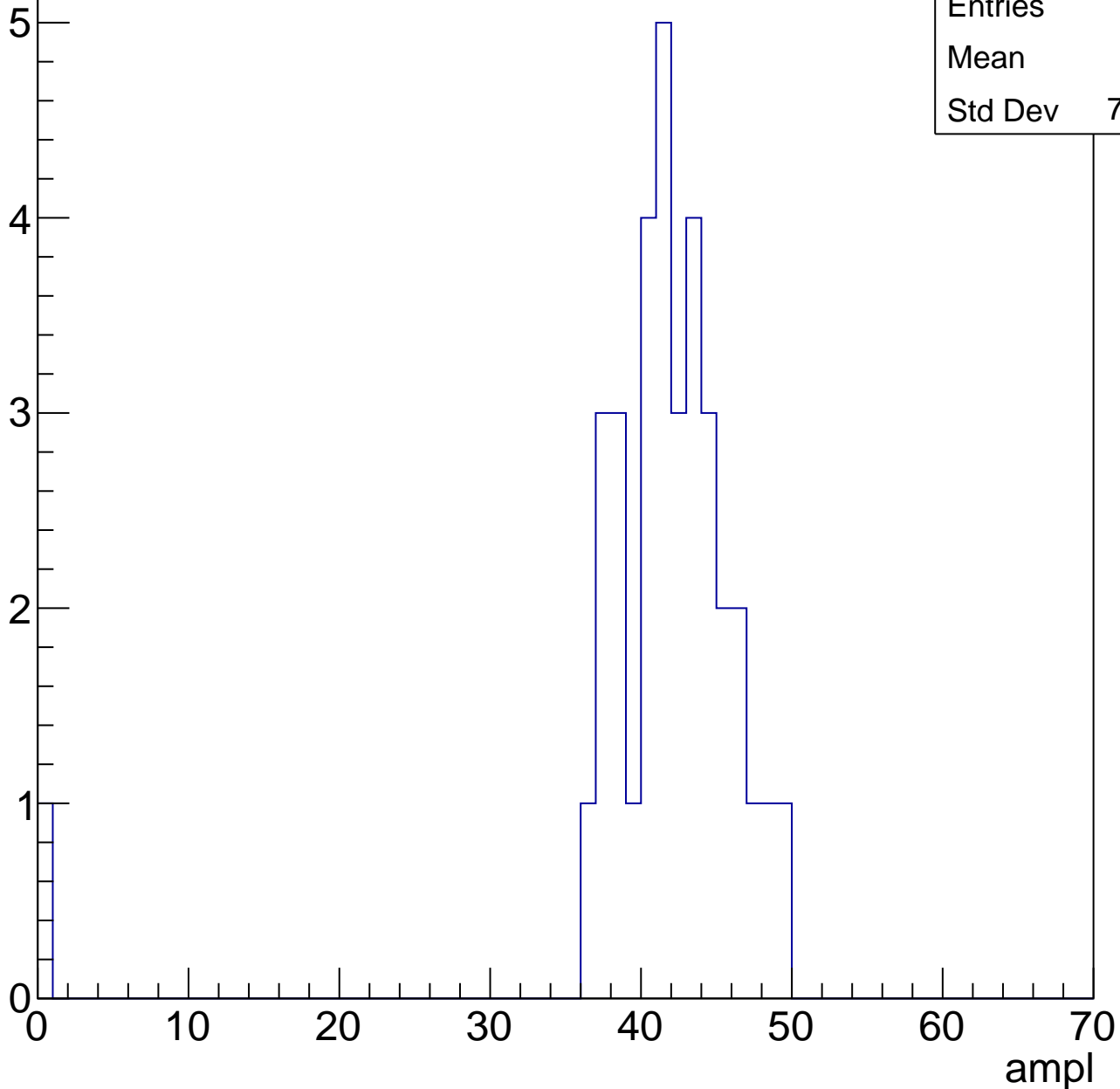


B1L103S, U14-ch40, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

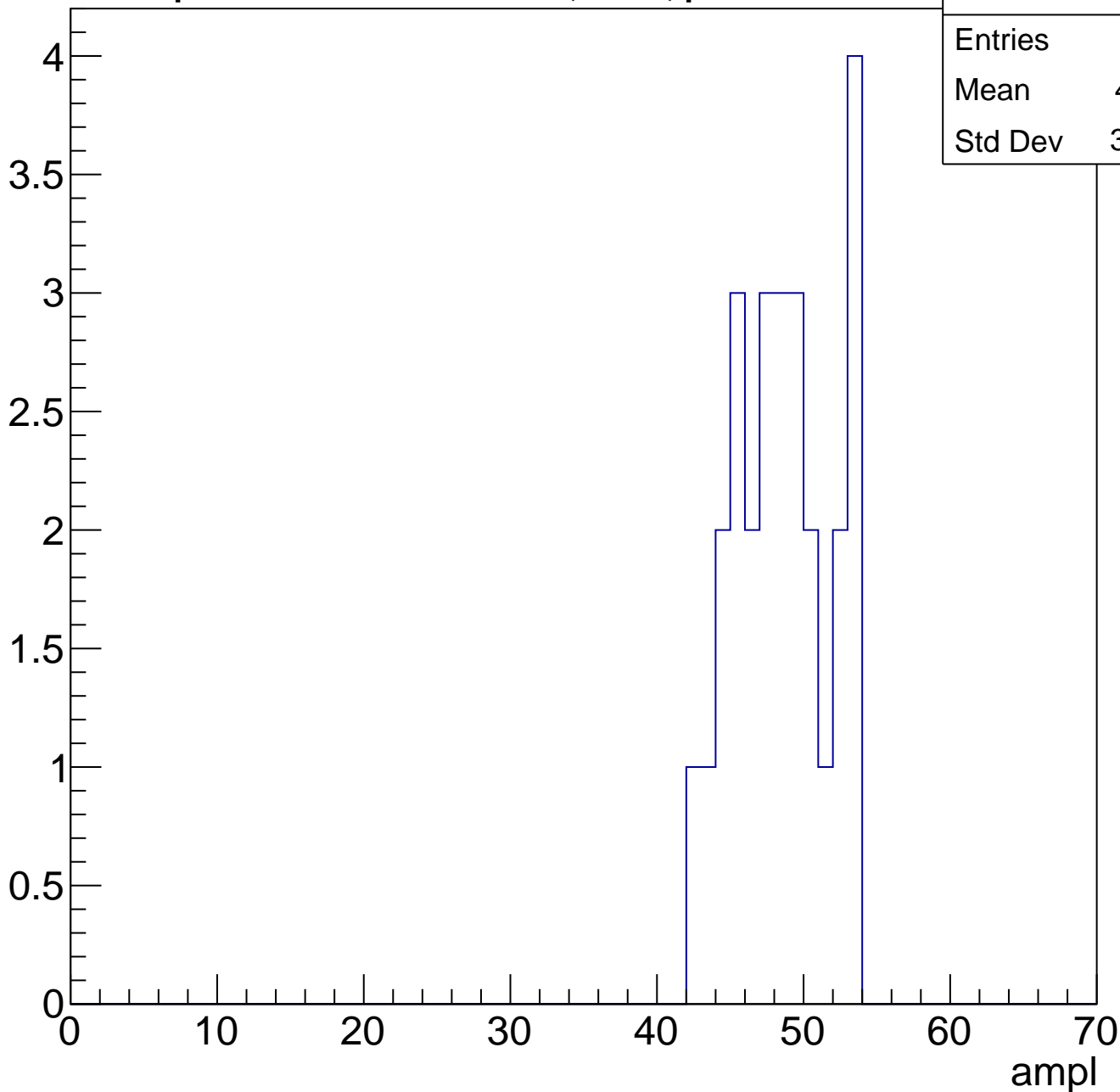
Entries	35
Mean	40.6
Std Dev	7.673



B1L103S, U14-ch40, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

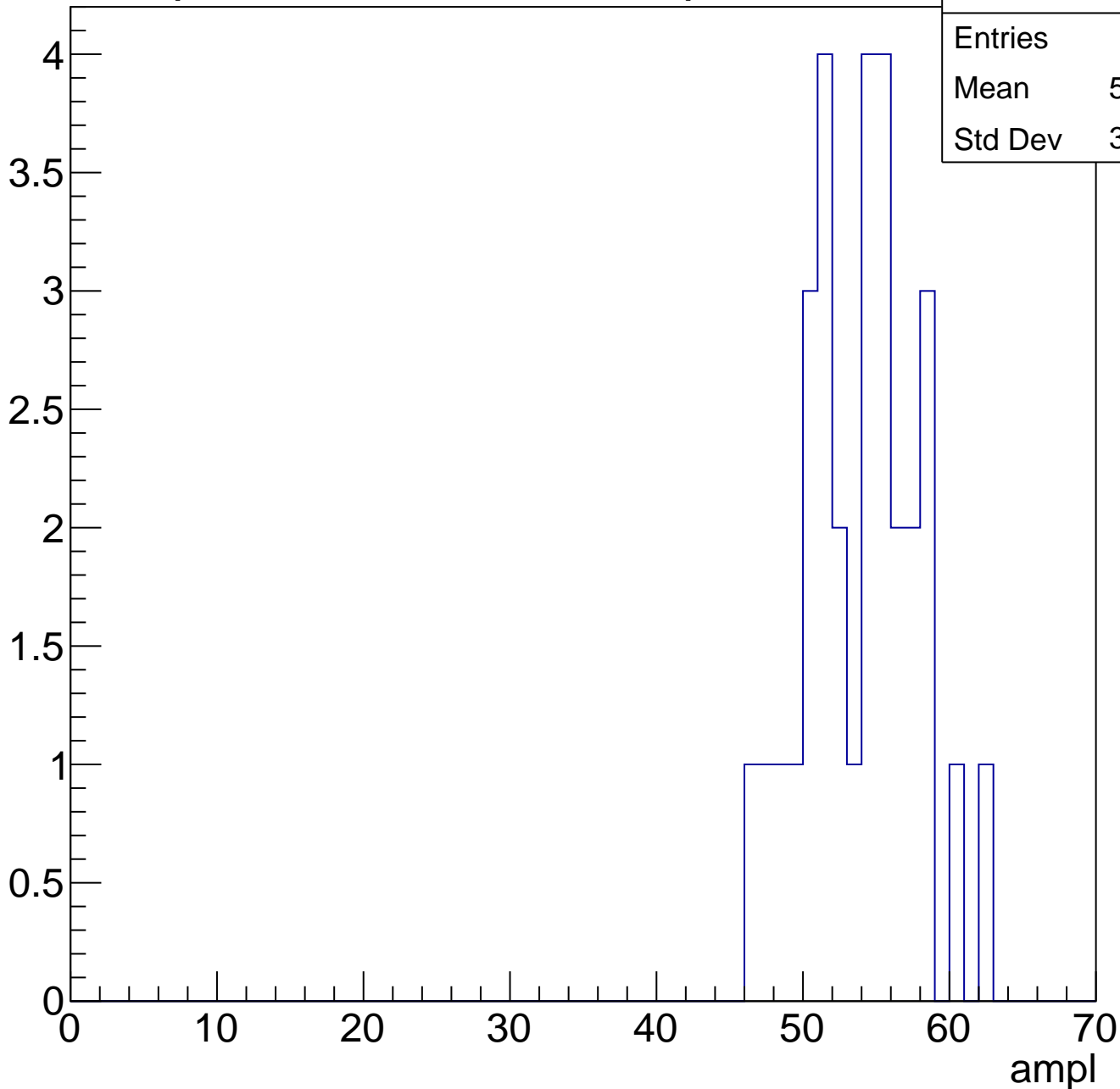


Entries	27
Mean	48.11
Std Dev	3.236

B1L103S, U14-ch40, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

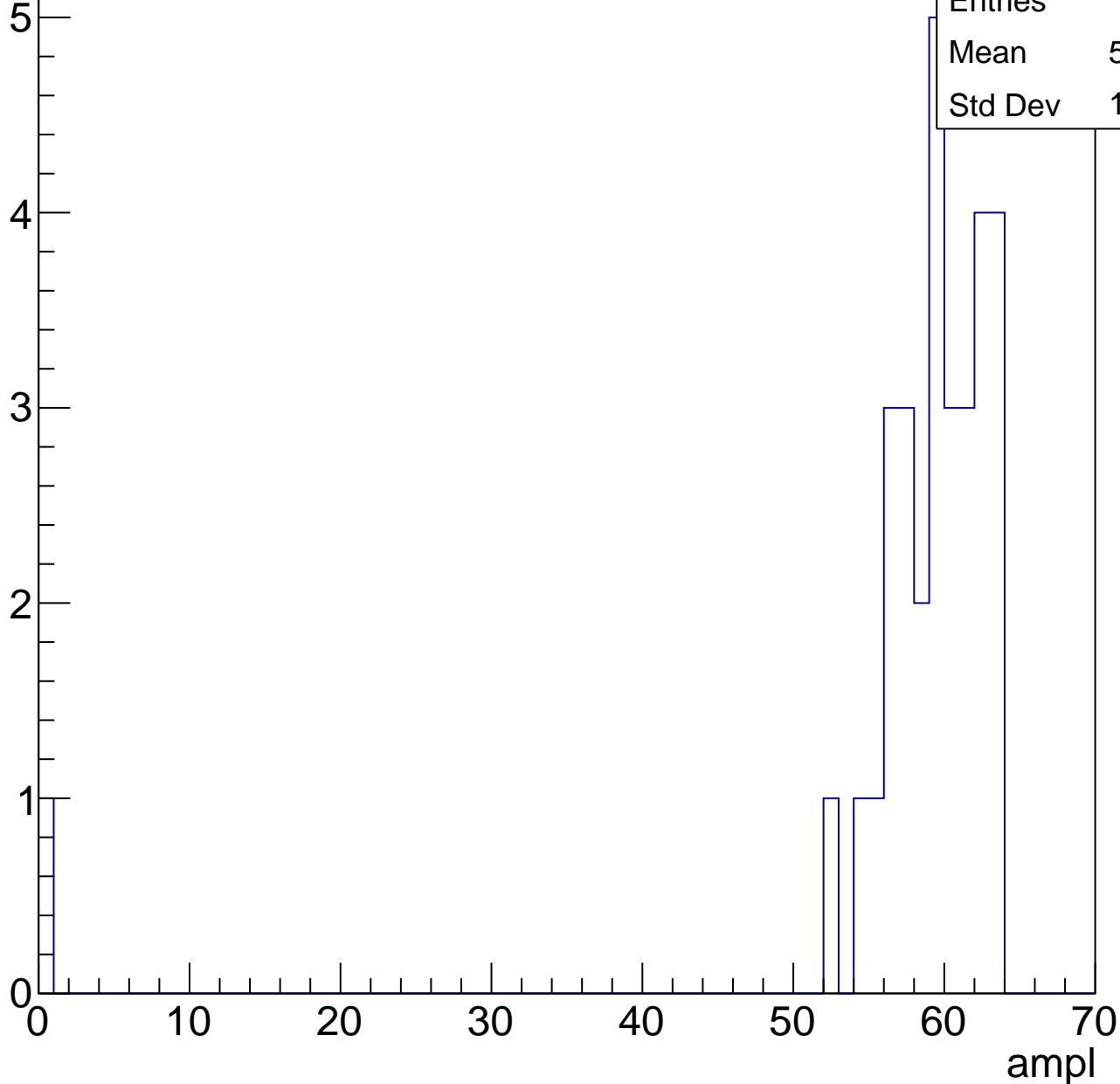


B1L103S, U14-ch40, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

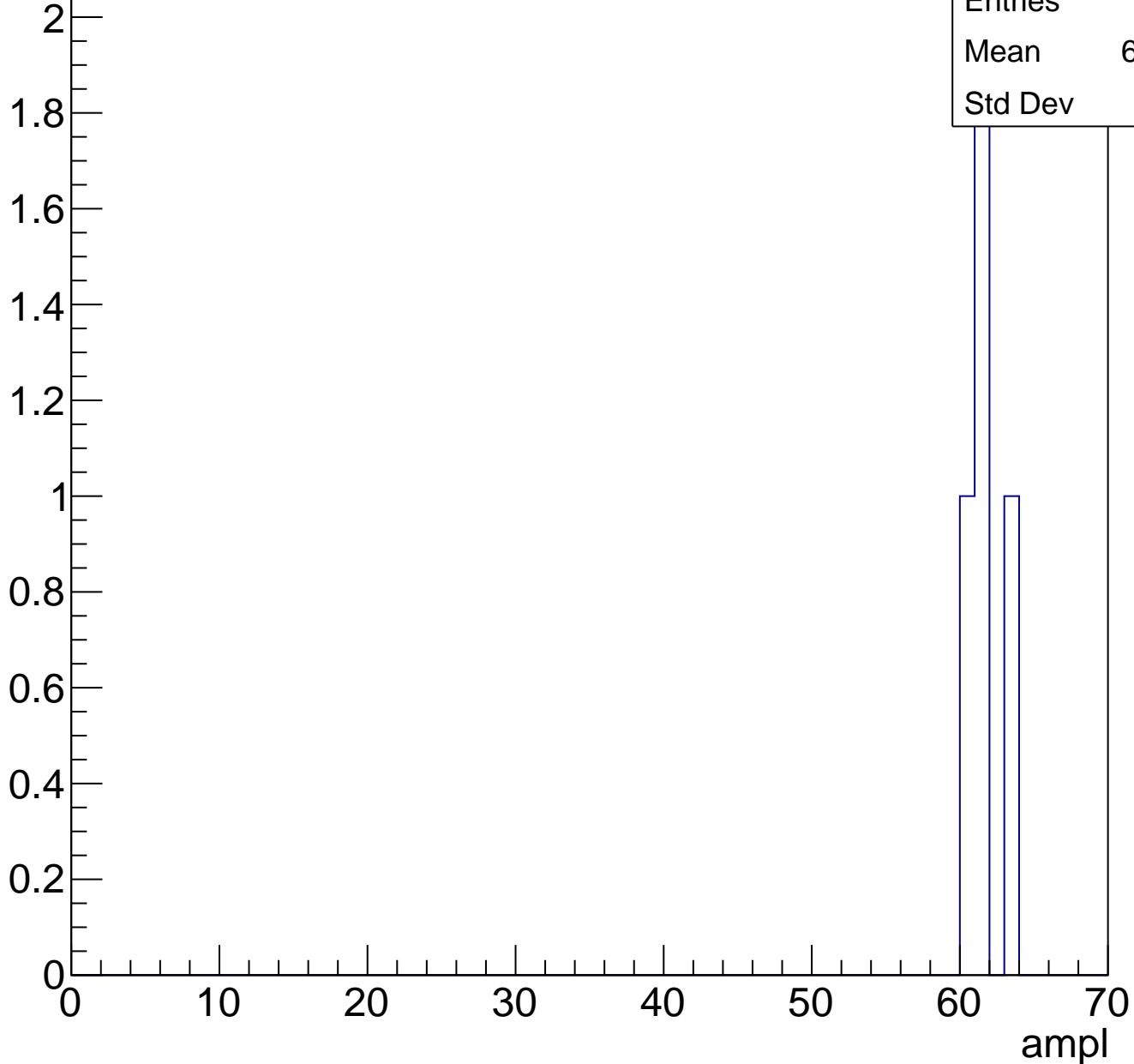
Entries	31
Mean	57.23
Std Dev	10.82



B1L103S, U14-ch40, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

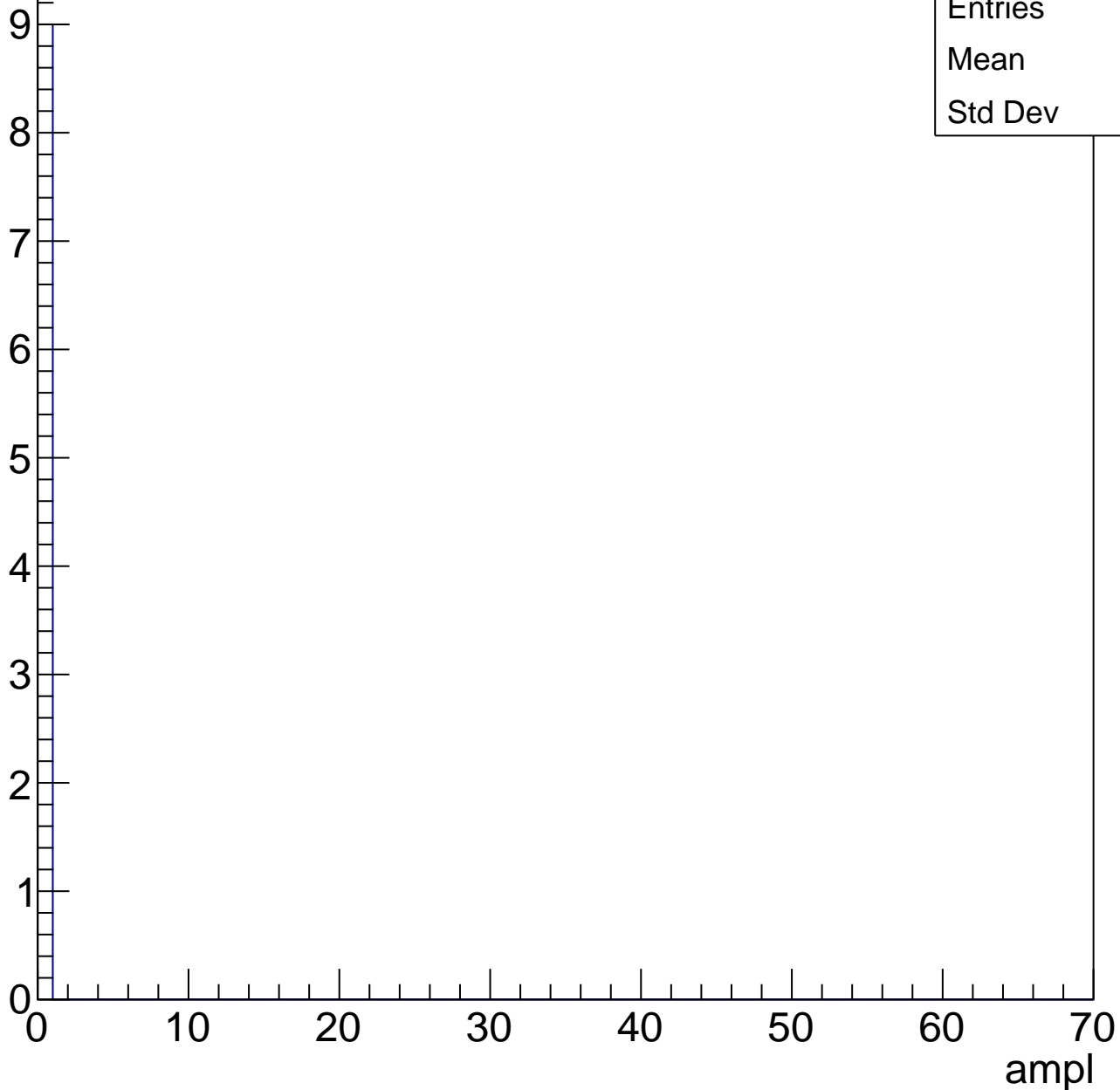


B1L103S, U14-ch40, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	9
Mean	0
Std Dev	0

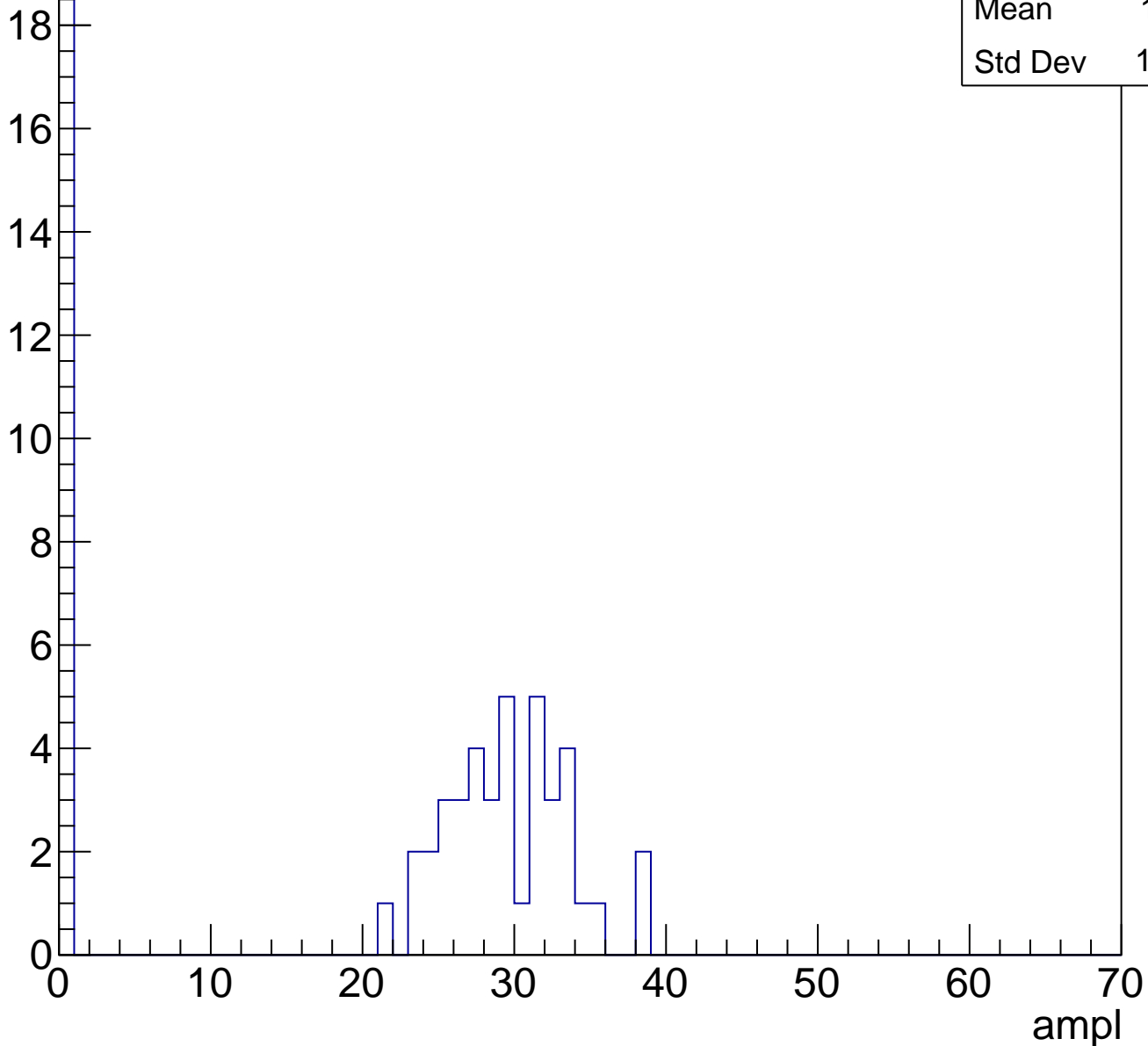


B1L103S, U14-ch41, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	59
Mean	19.71
Std Dev	13.96

Entry

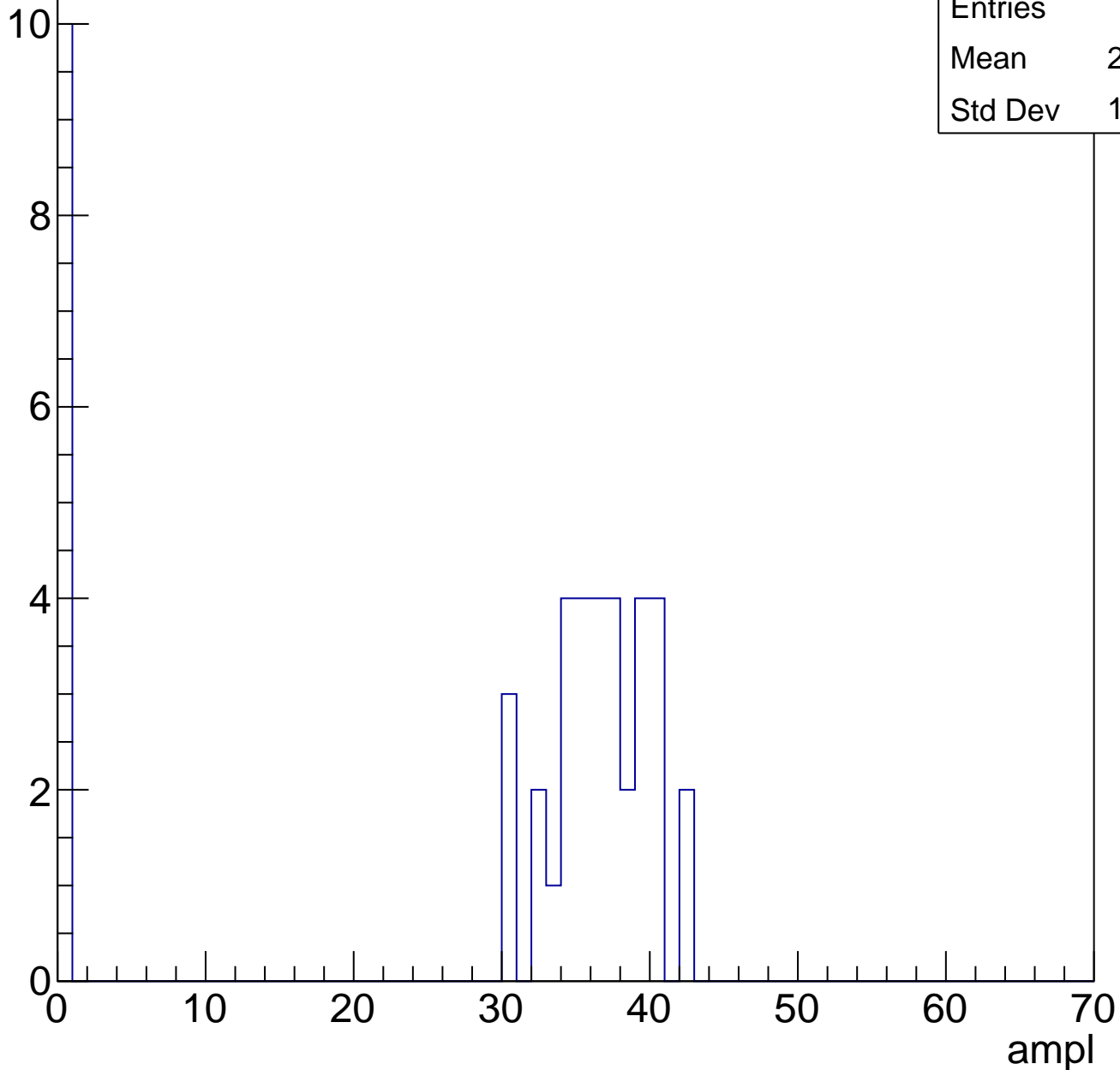


B1L103S, U14-ch41, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	44
Mean	27.98
Std Dev	15.43

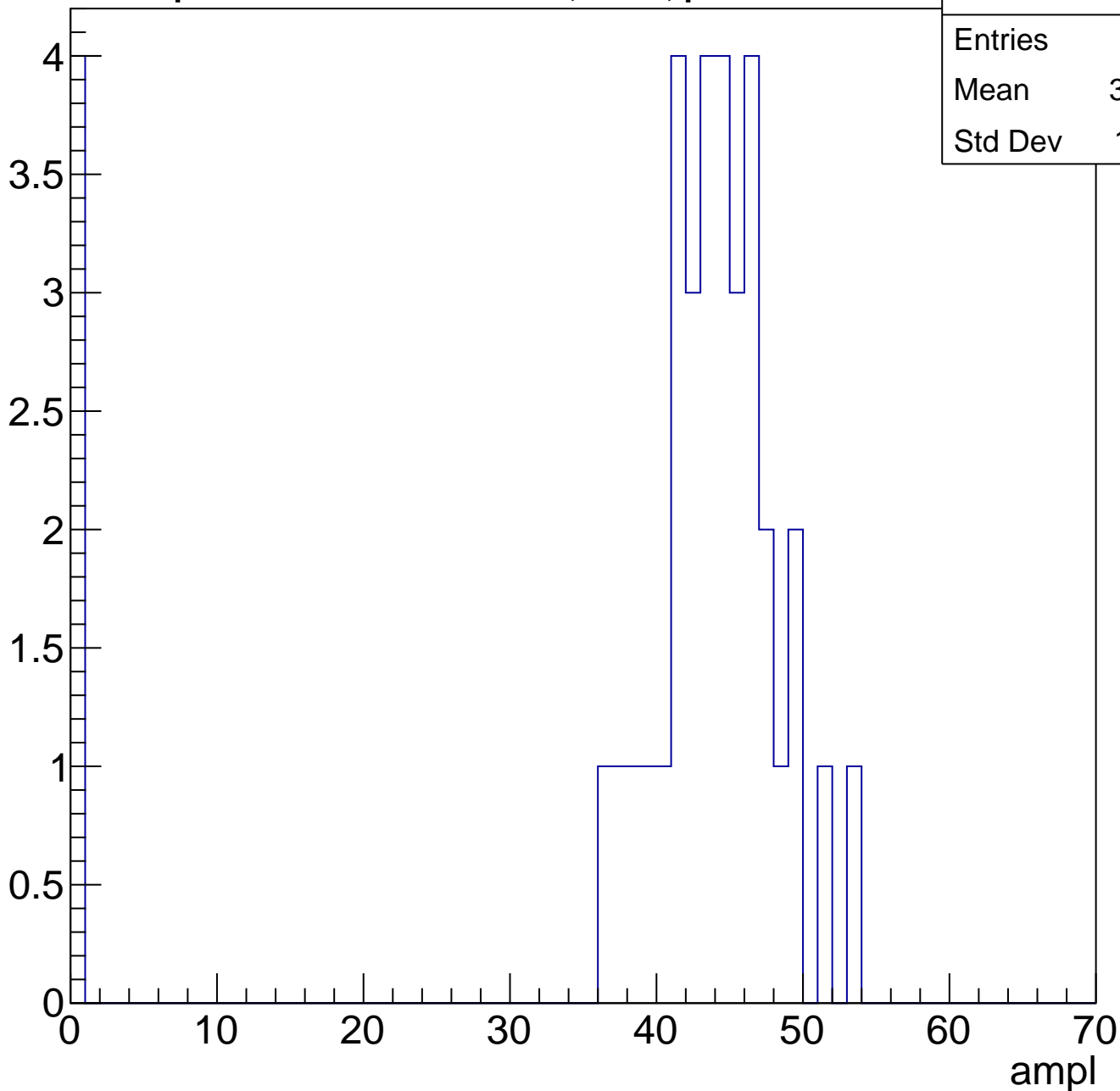
Entry



B1L103S, U14-ch41, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

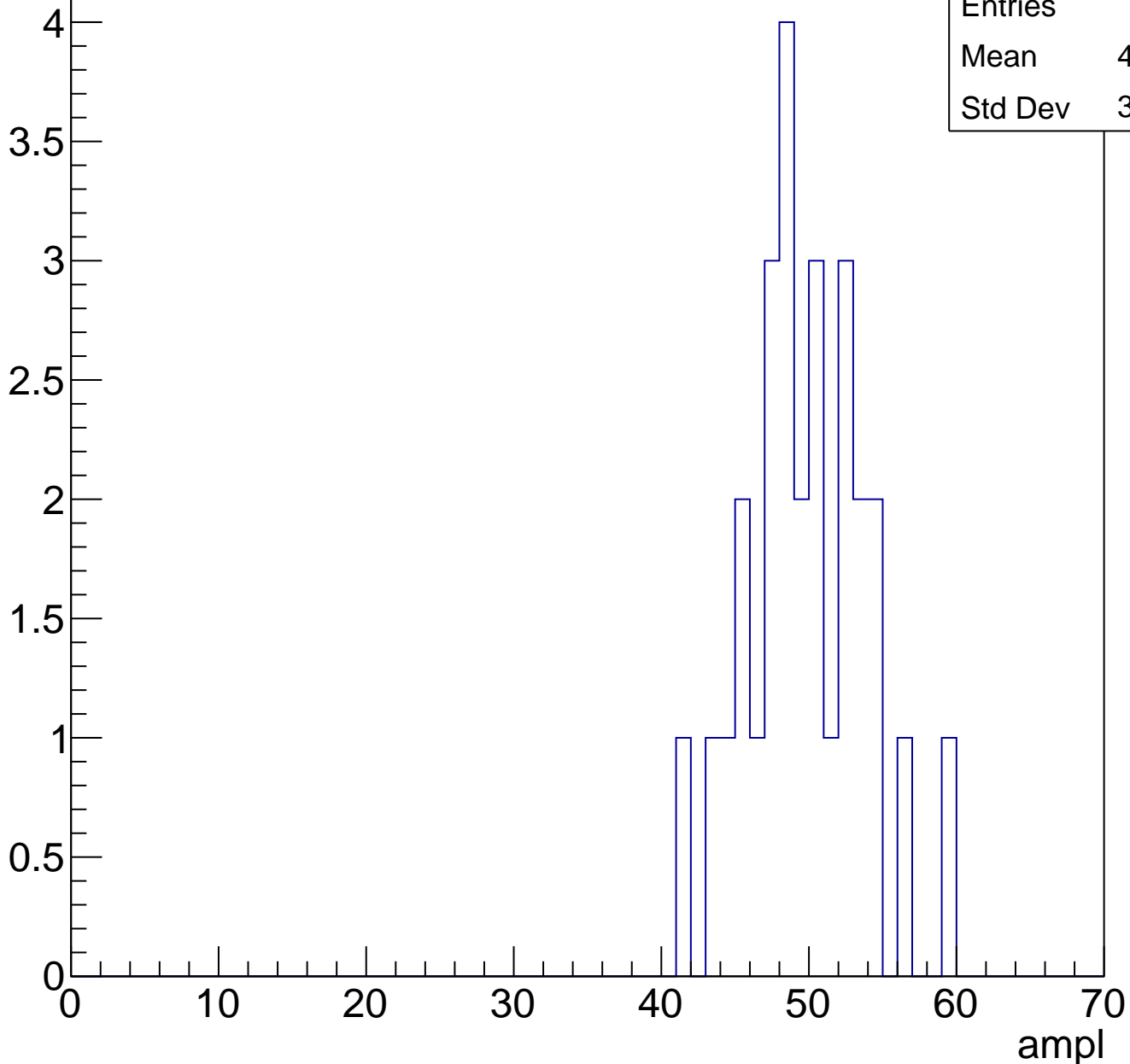


Entries	38
Mean	39.24
Std Dev	13.91

B1L103S, U14-ch41, adc3

calib_packv5_041523_1651.root, FC#0, port C2

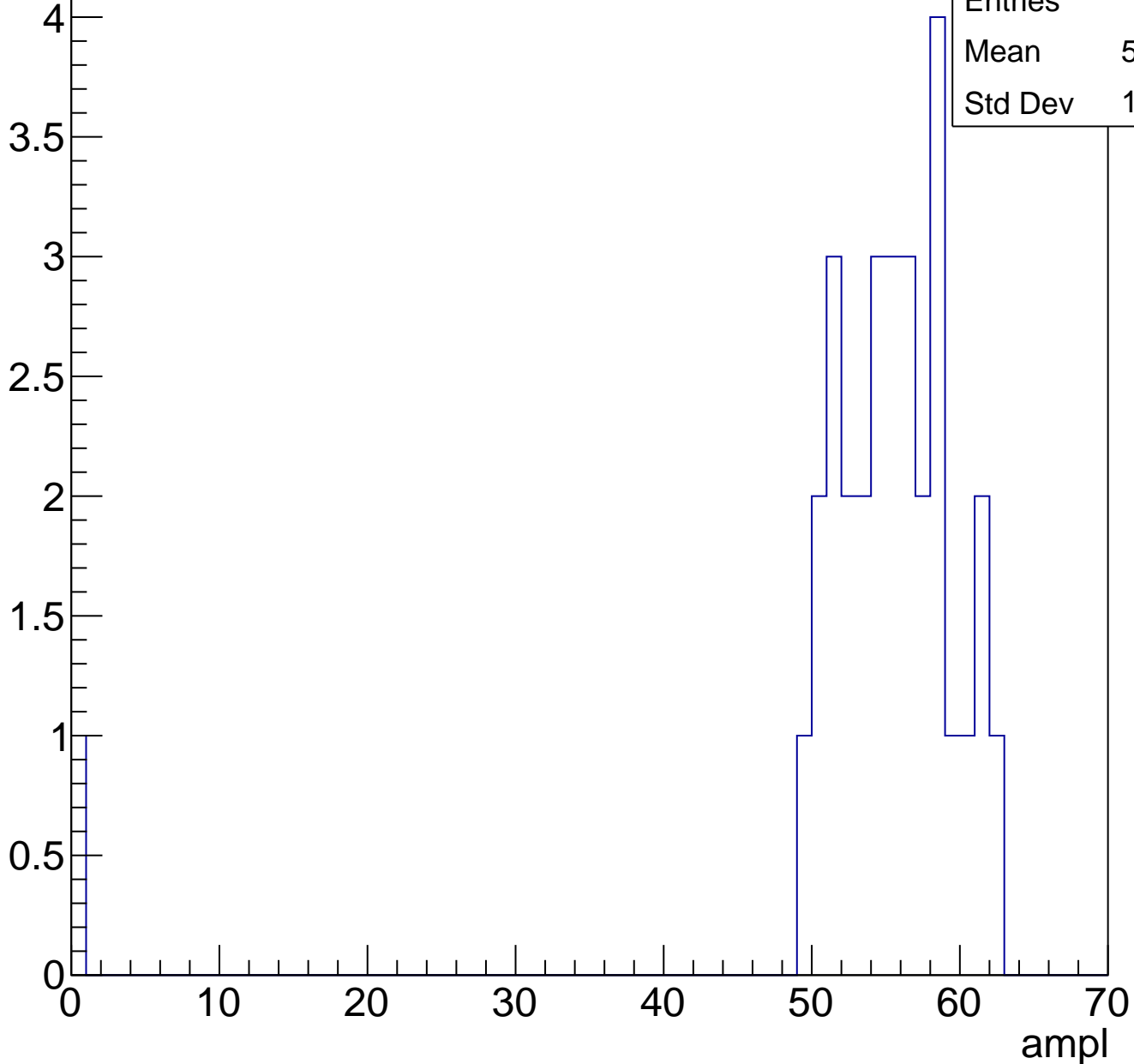
Entry



B1L103S, U14-ch41, adc4

calib_packv5_041523_1651.root, FC#0, port C2

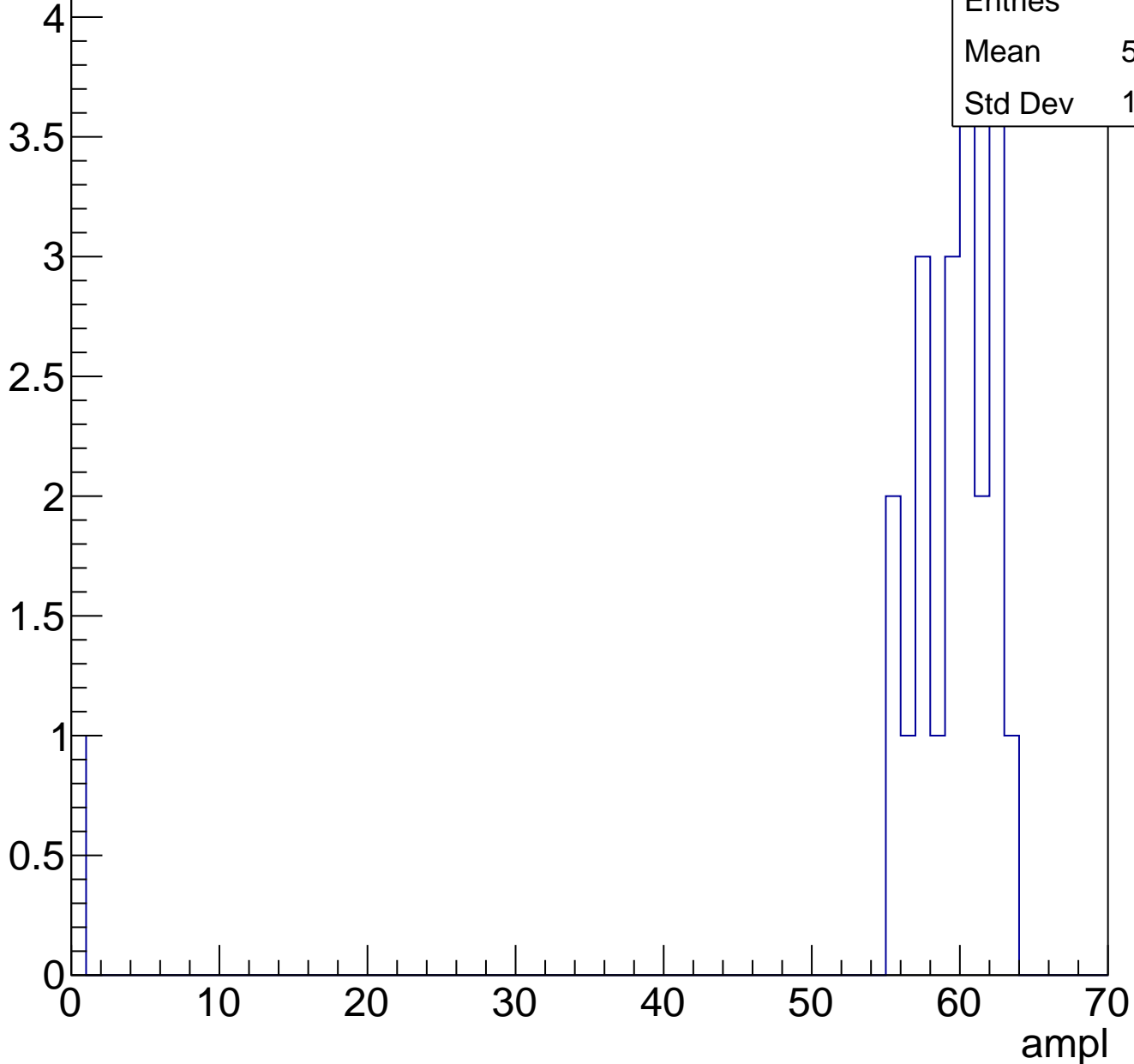
Entry



B1L103S, U14-ch41, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch41, adc6

calib_packv5_041523_1651.root, FC#0, port C2

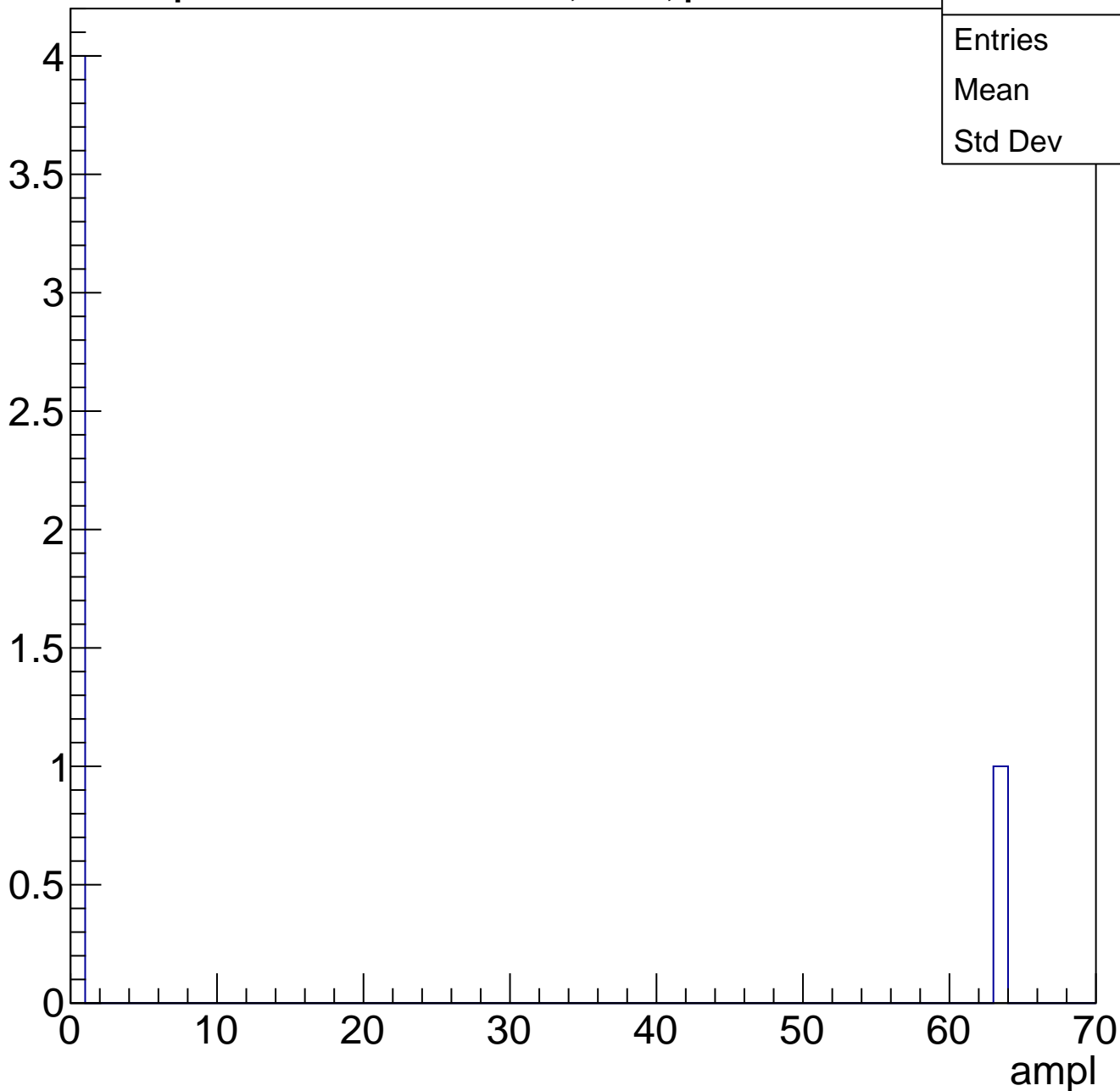
Entry



B1L103S, U14-ch41, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

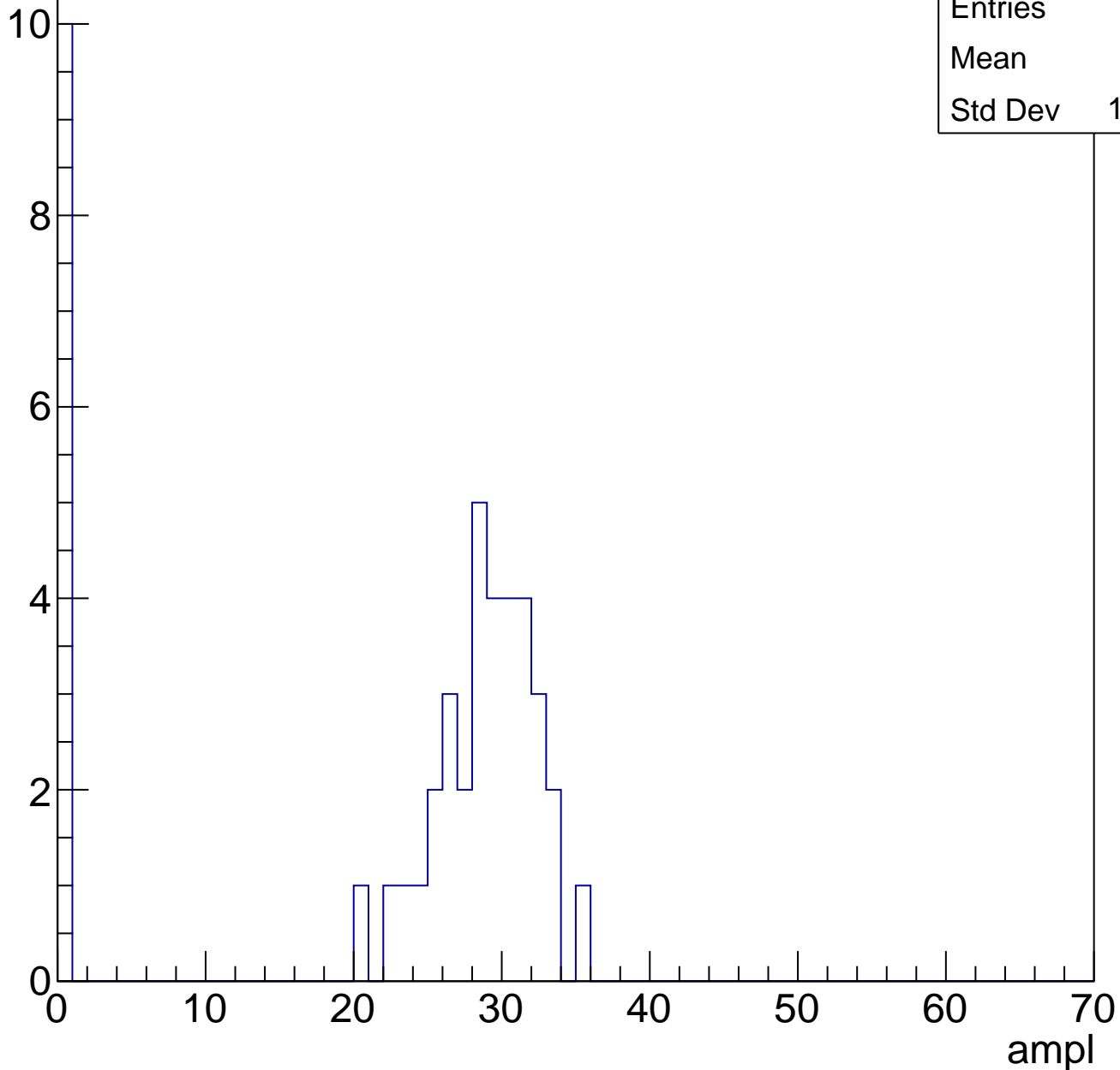


B1L103S, U14-ch42, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	44
Mean	22
Std Dev	12.28

Entry

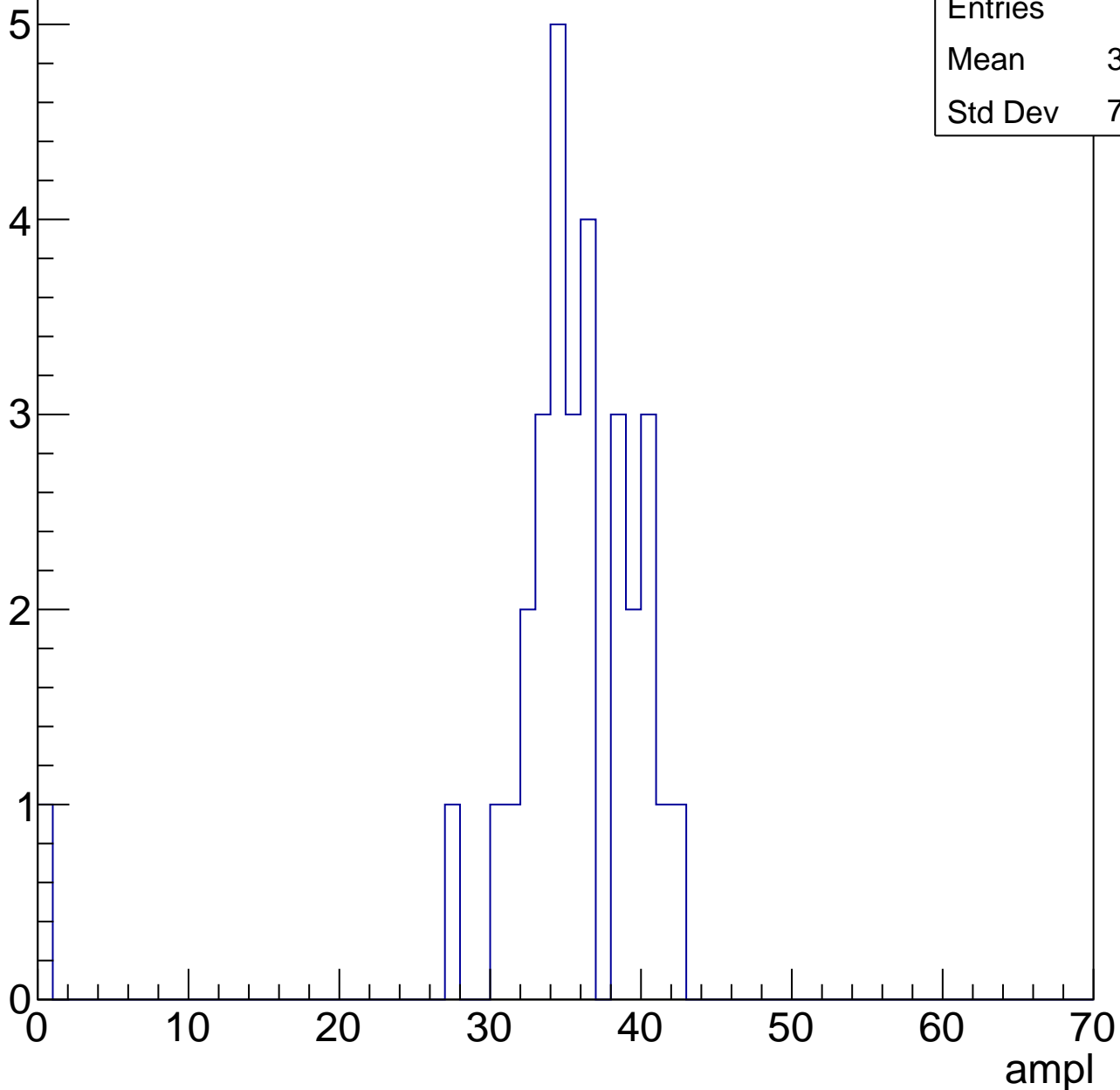


B1L103S, U14-ch42, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	31
Mean	34.35
Std Dev	7.128

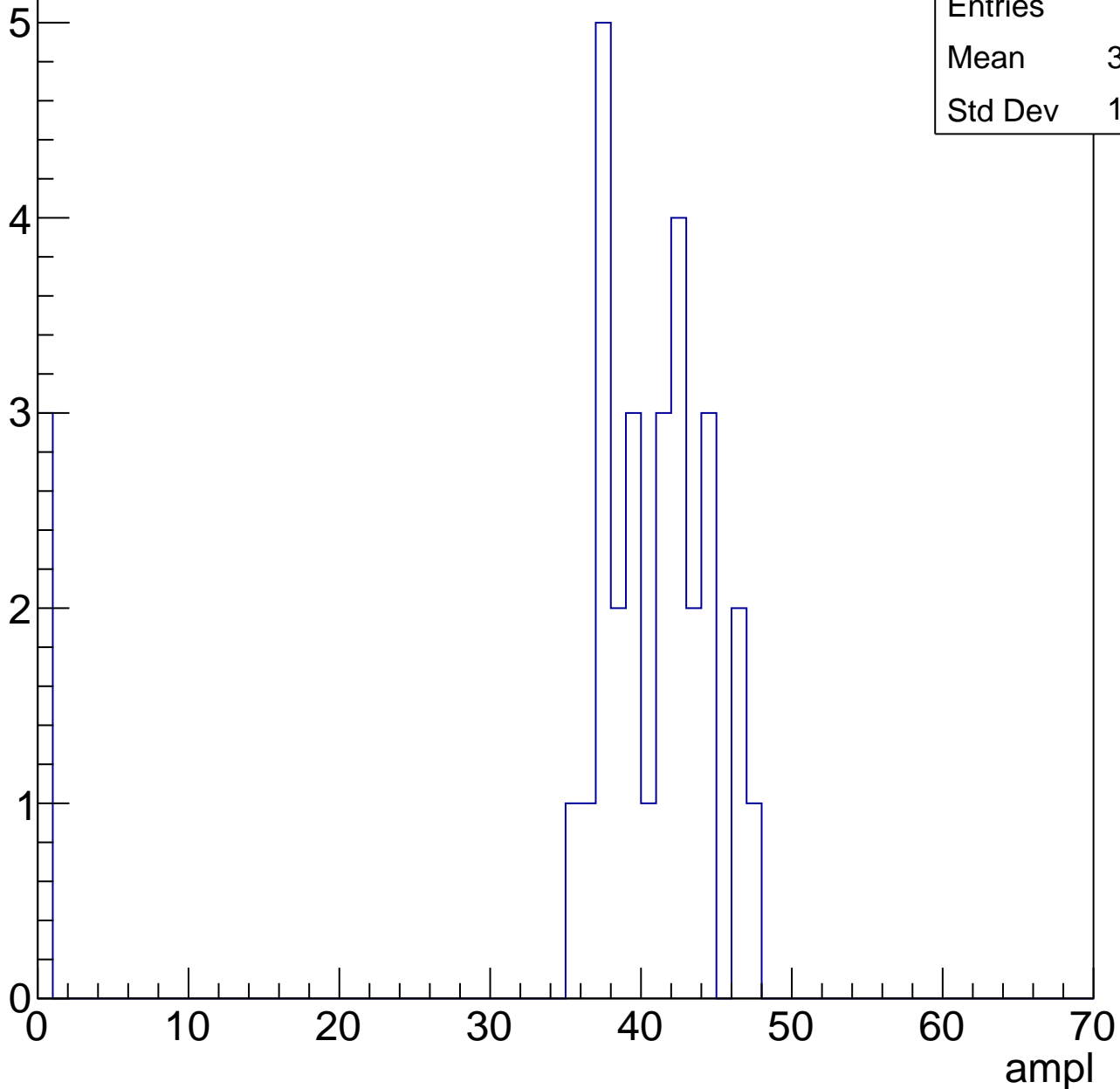


B1L103S, U14-ch42, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	31
Mean	36.68
Std Dev	12.39

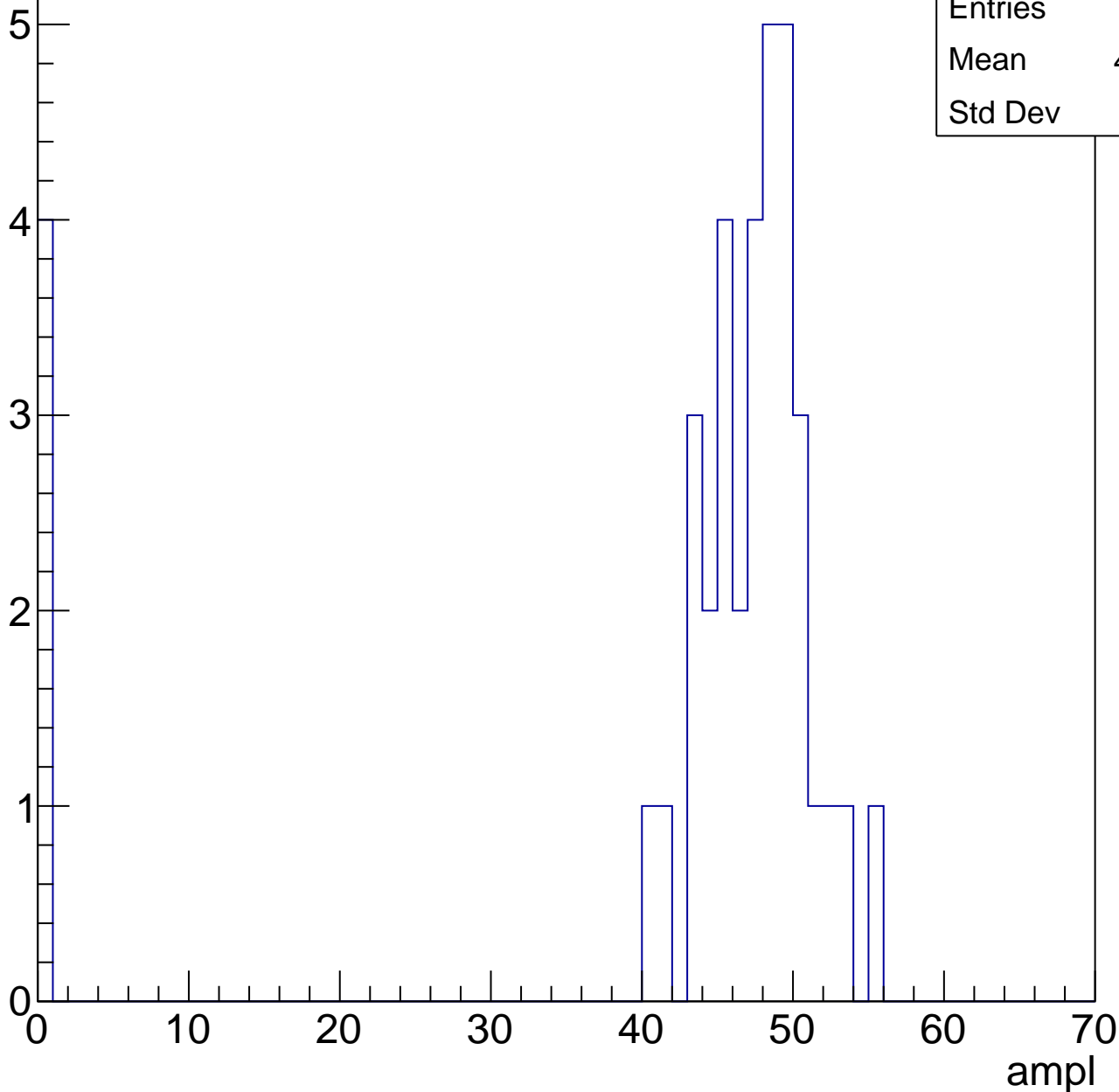


B1L103S, U14-ch42, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

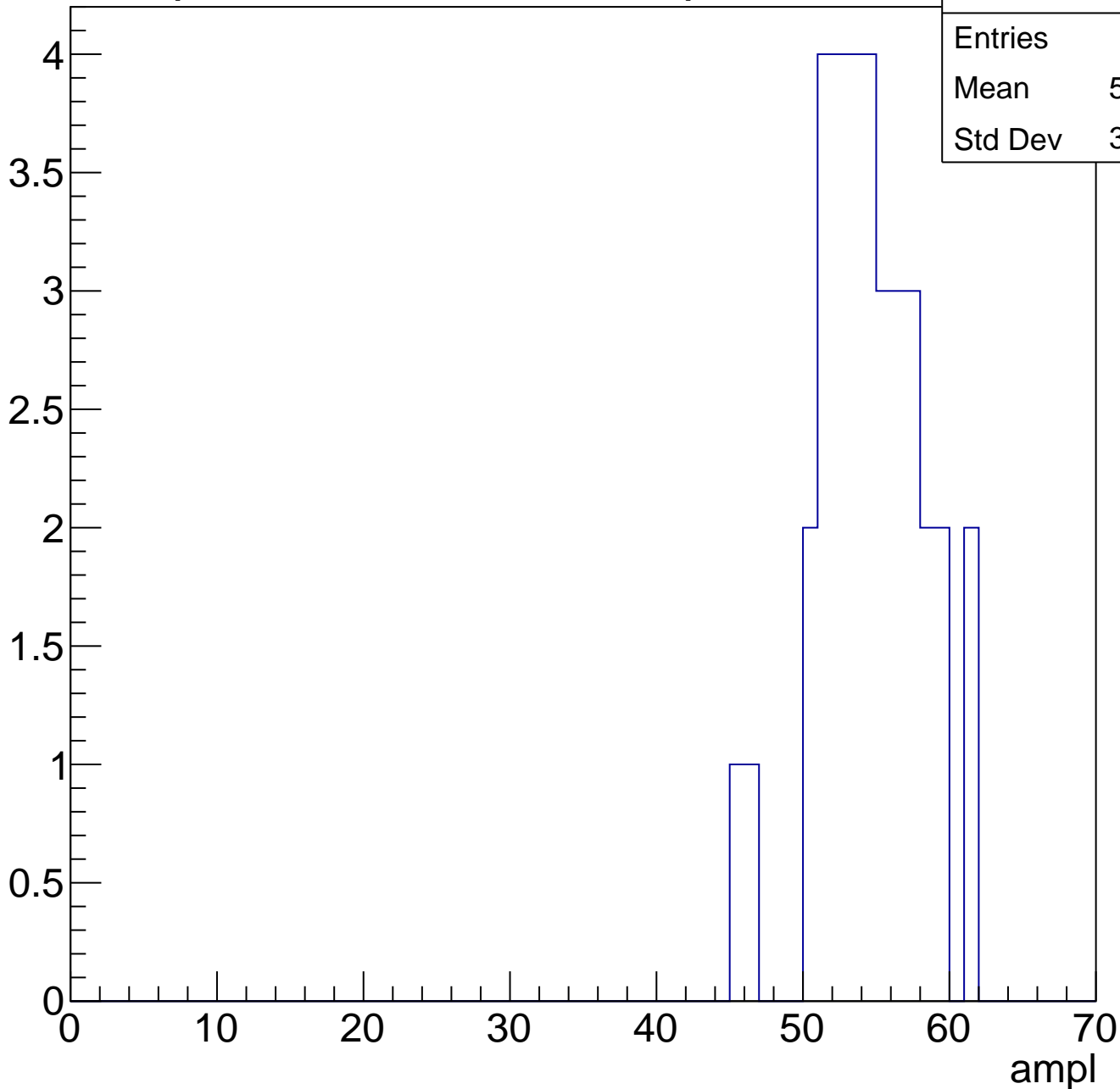
Entries	38
Mean	42.21
Std Dev	14.8



B1L103S, U14-ch42, adc4

calib_packv5_041523_1651.root, FC#0, port C2

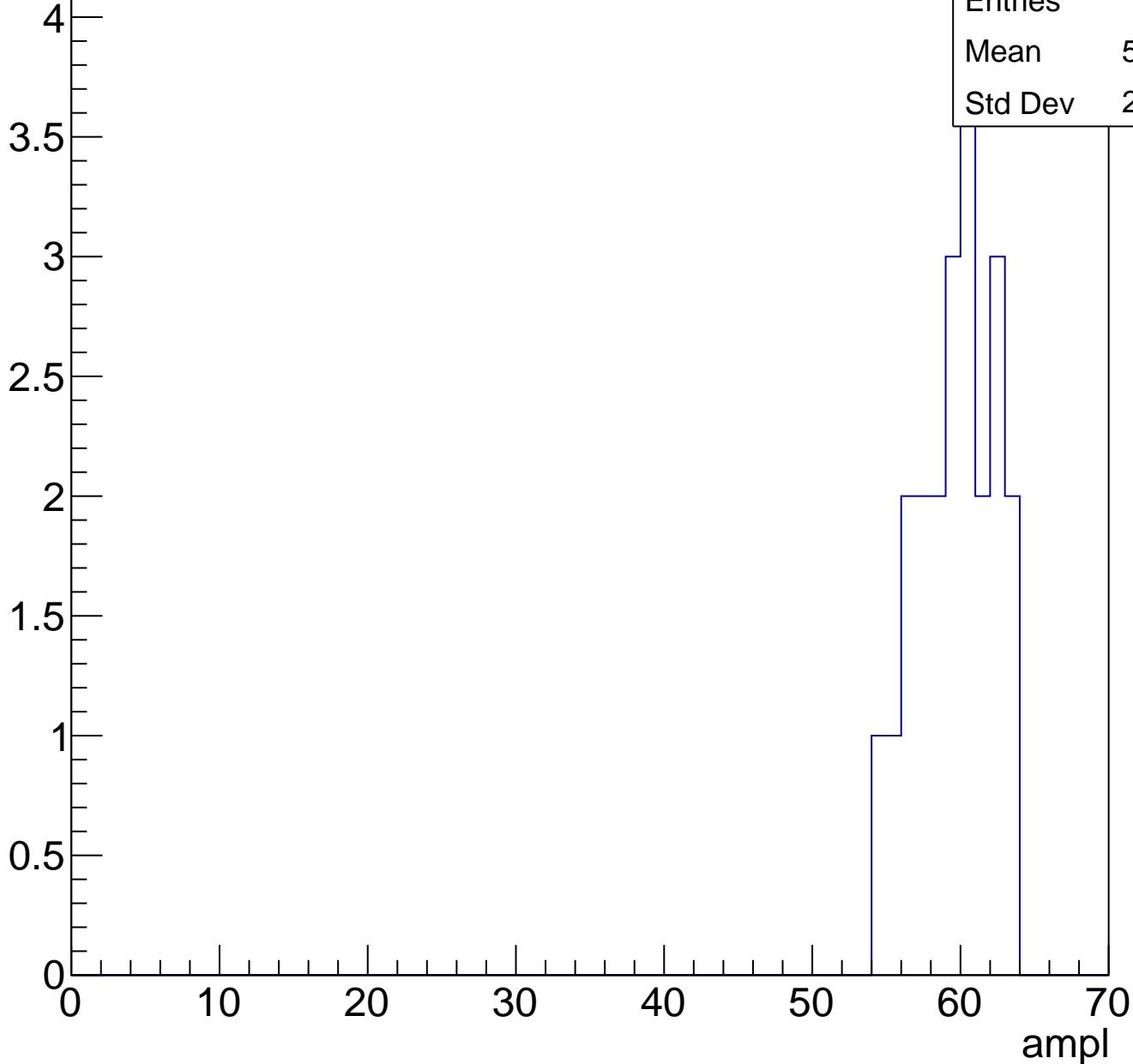
Entry



B1L103S, U14-ch42, adc5

calib_packv5_041523_1651.root, FC#0, port C2

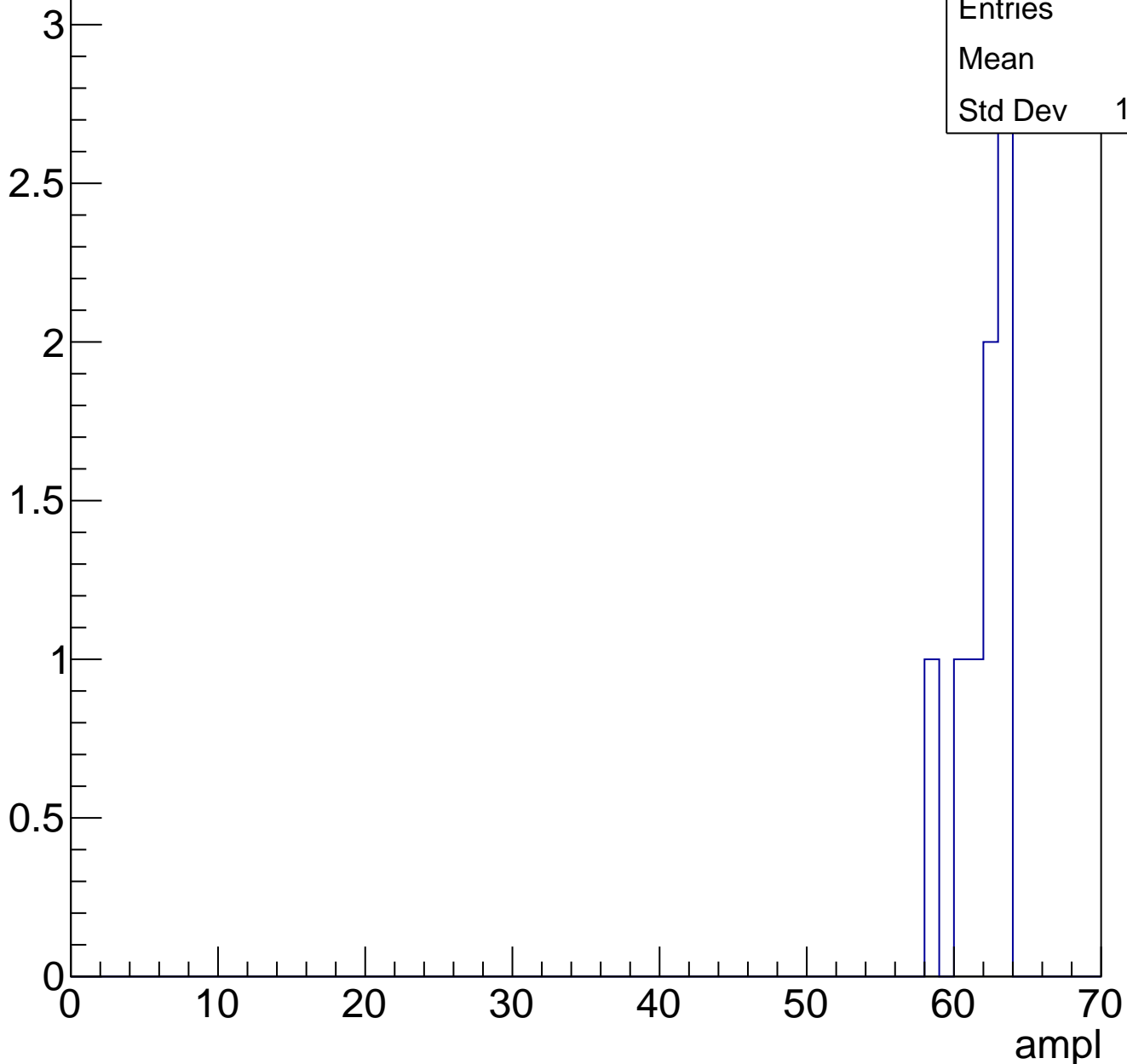
Entry



B1L103S, U14-ch42, adc6

calib_packv5_041523_1651.root, FC#0, port C2

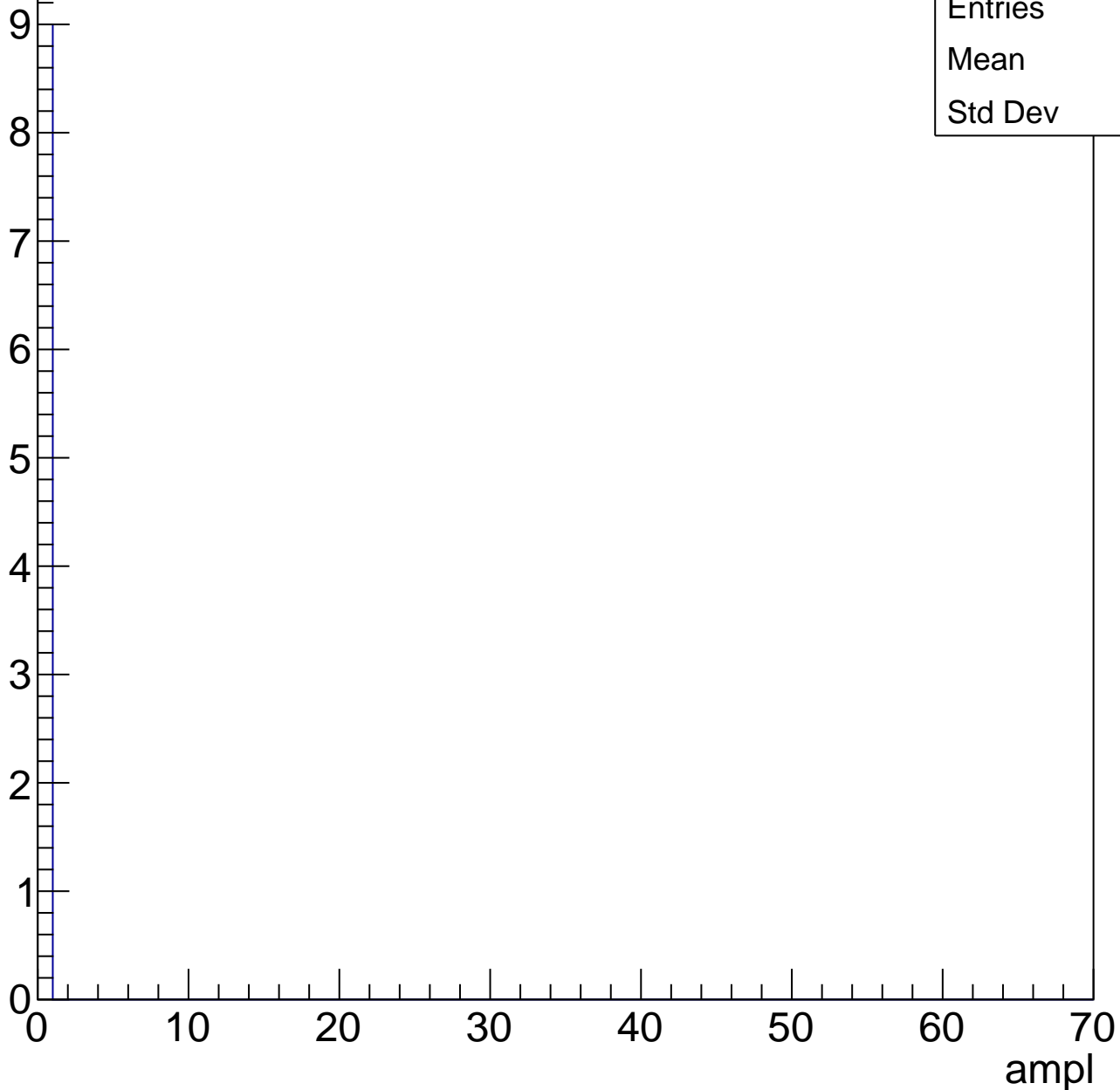
Entry



B1L103S, U14-ch42, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

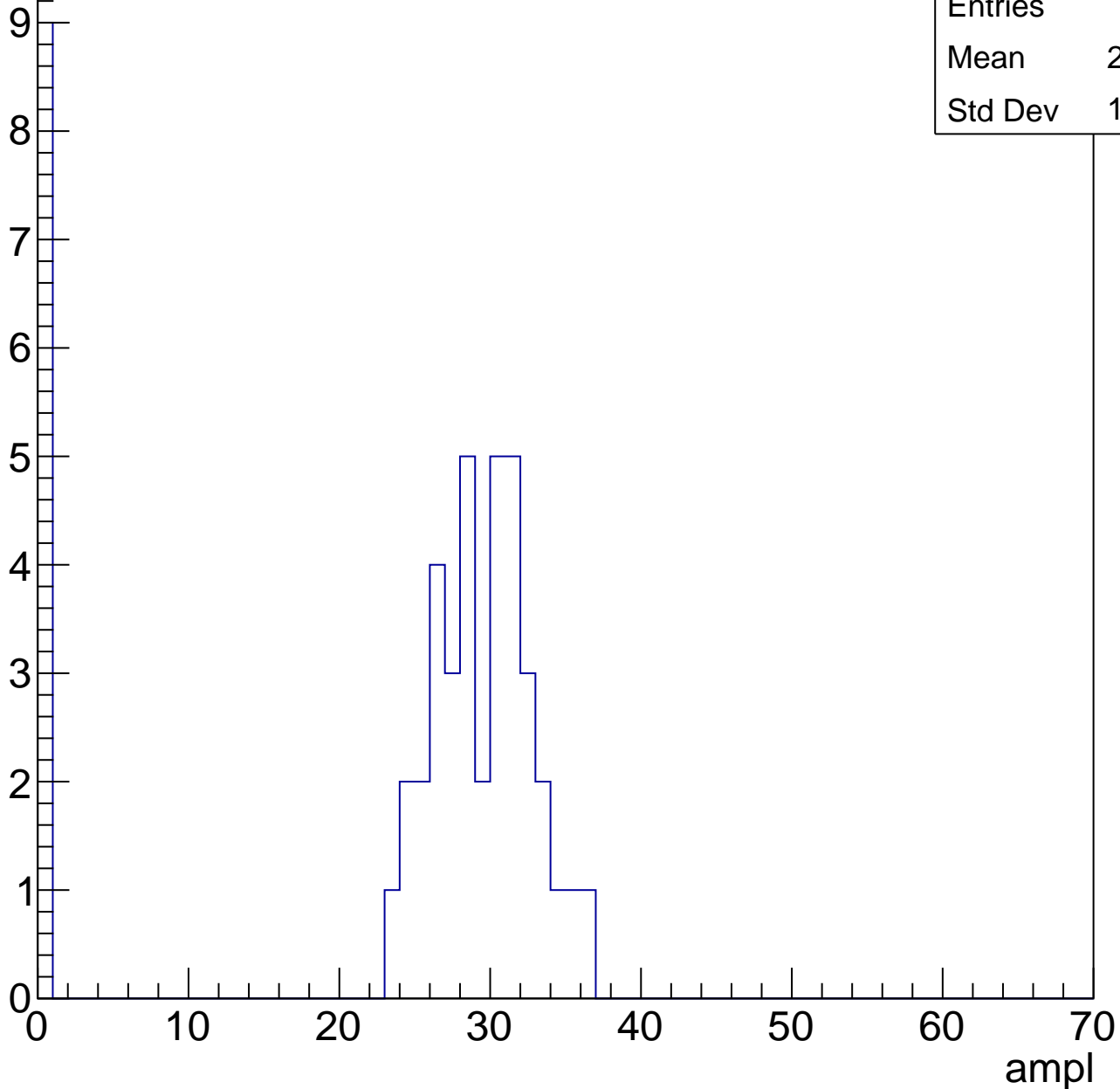


B1L103S, U14-ch43, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	46
Mean	23.39
Std Dev	11.88

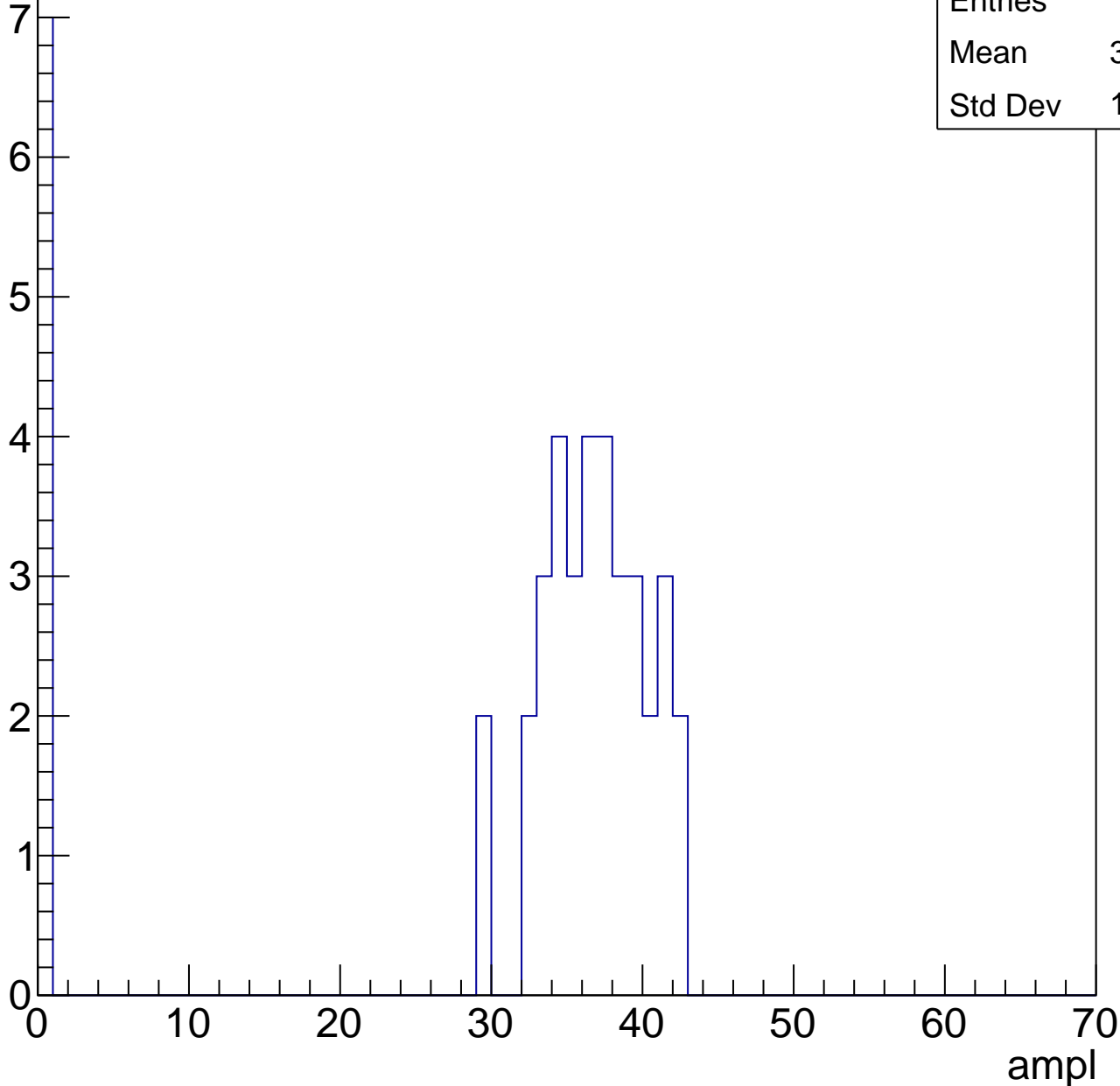


B1L103S, U14-ch43, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	42
Mean	30.29
Std Dev	13.89

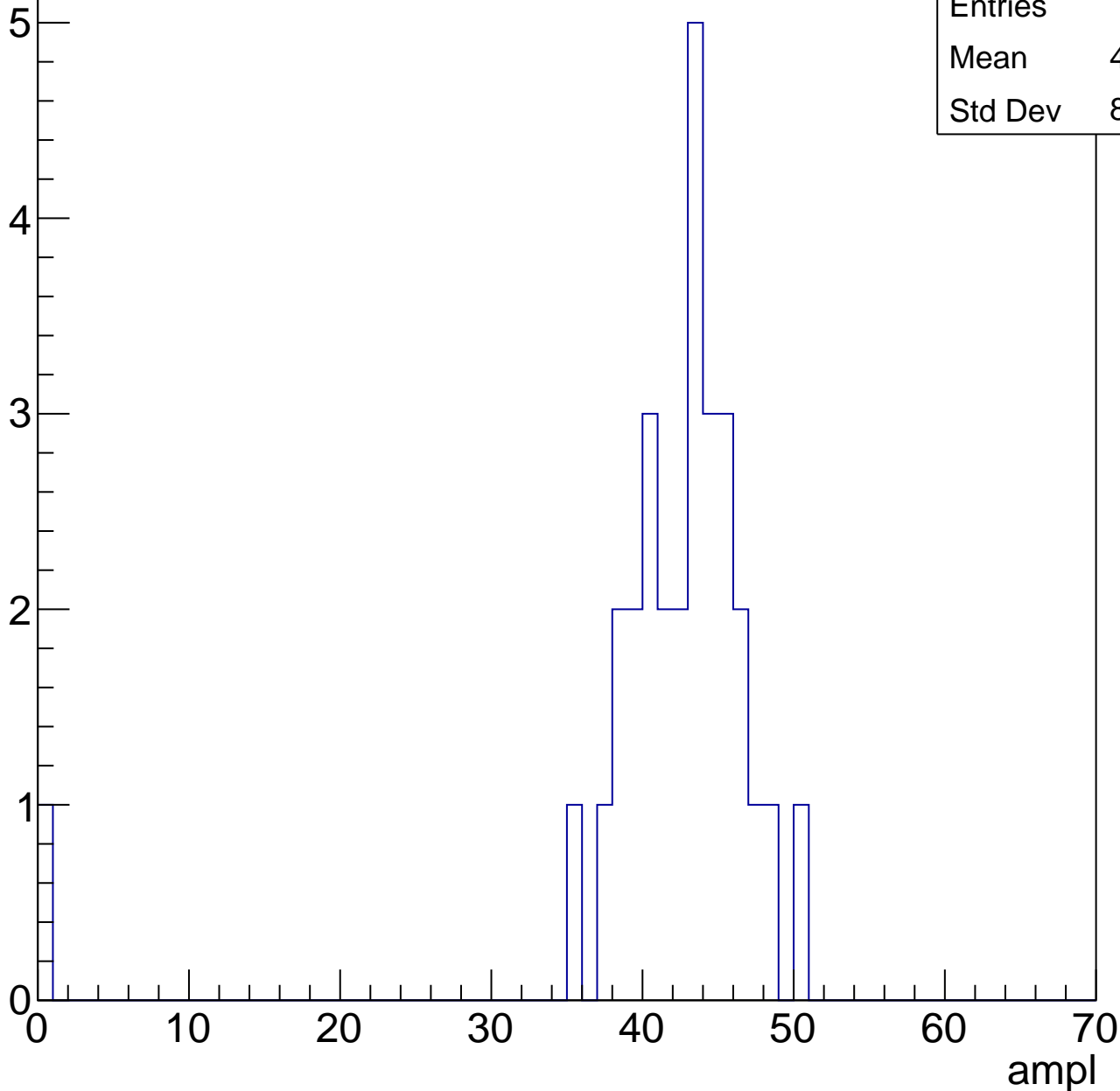


B1L103S, U14-ch43, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	30
Mean	41.03
Std Dev	8.317

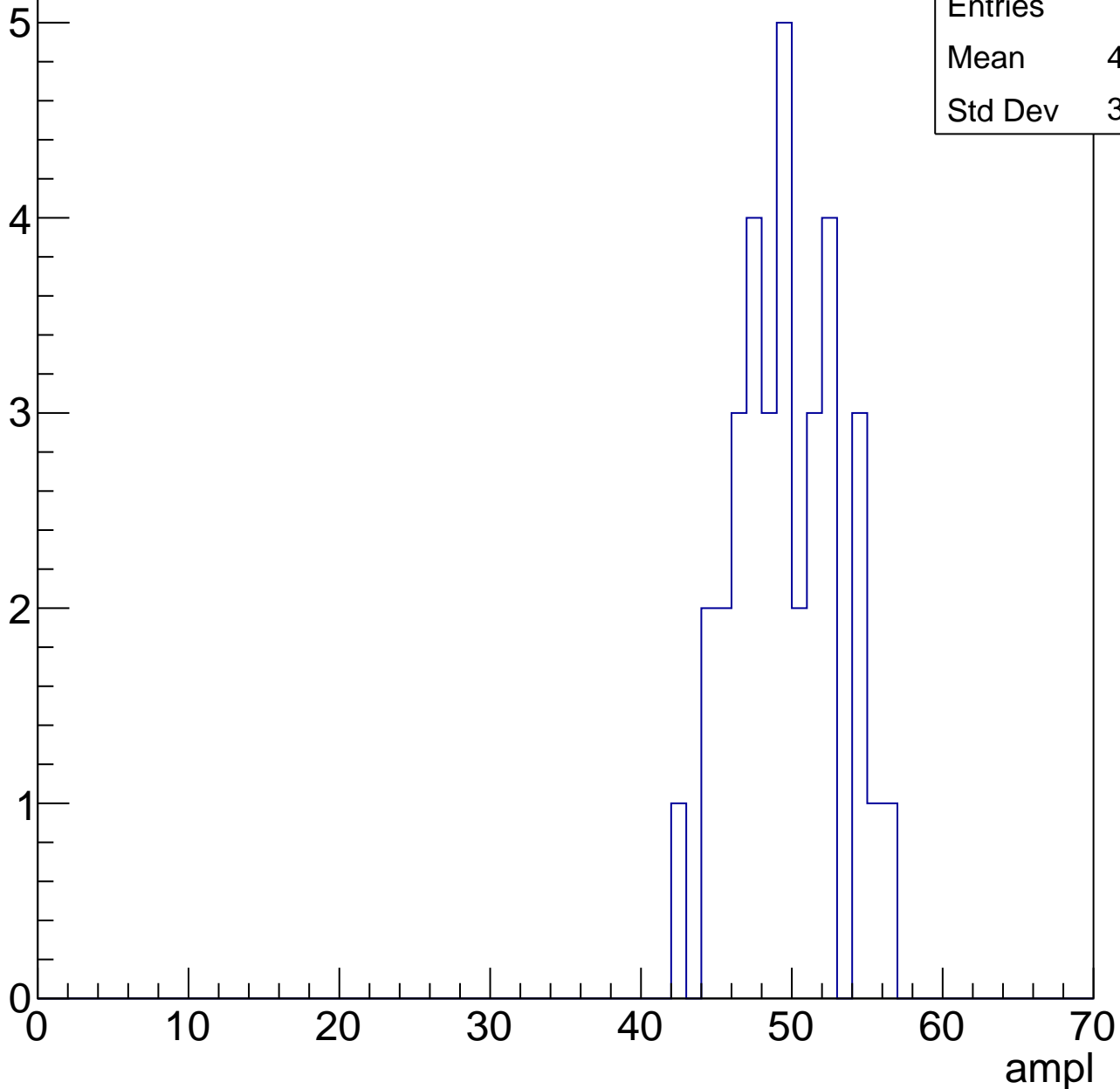


B1L103S, U14-ch43, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	34
Mean	49.09
Std Dev	3.373

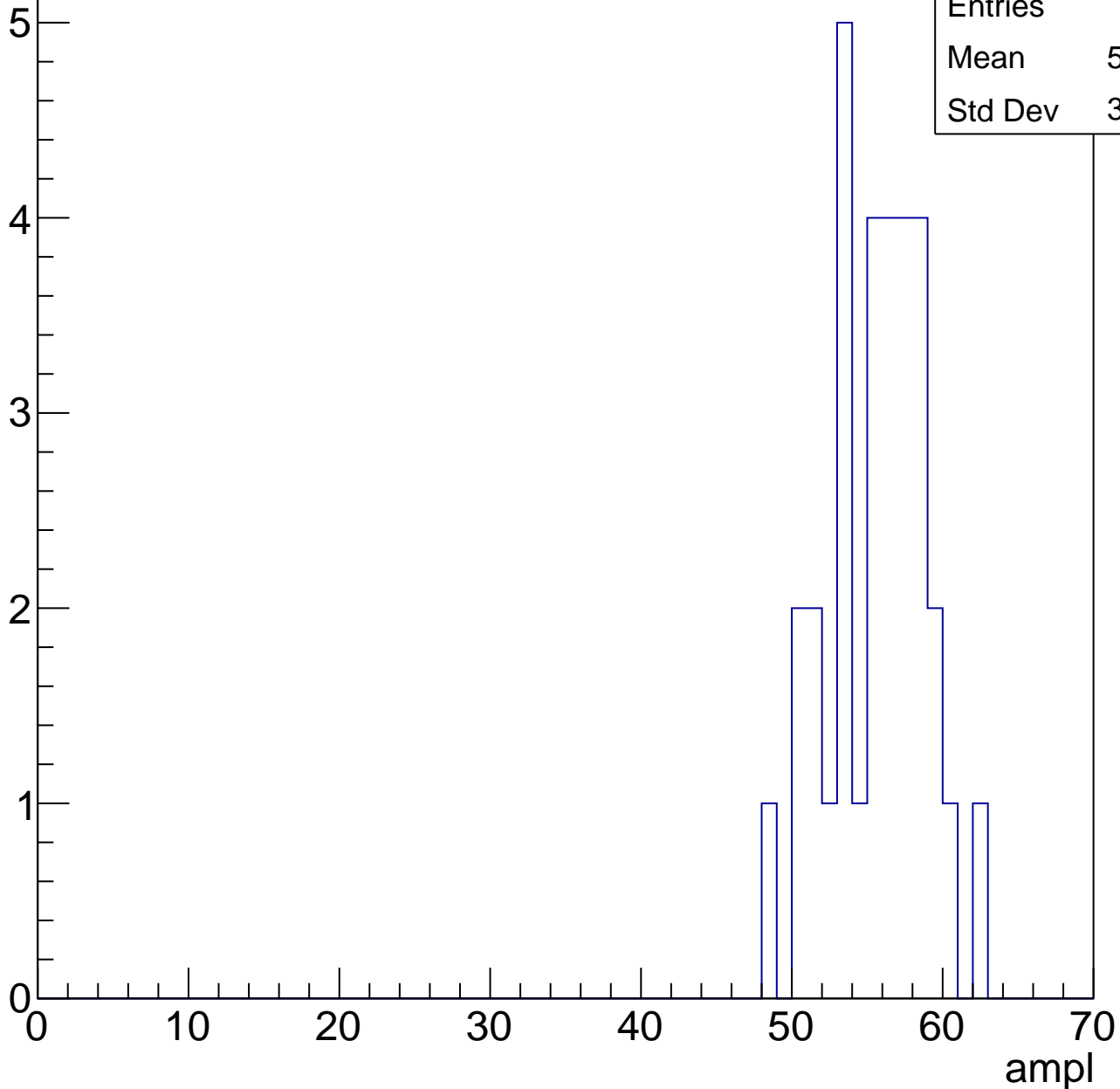


B1L103S, U14-ch43, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	32
Mean	55.16
Std Dev	3.173

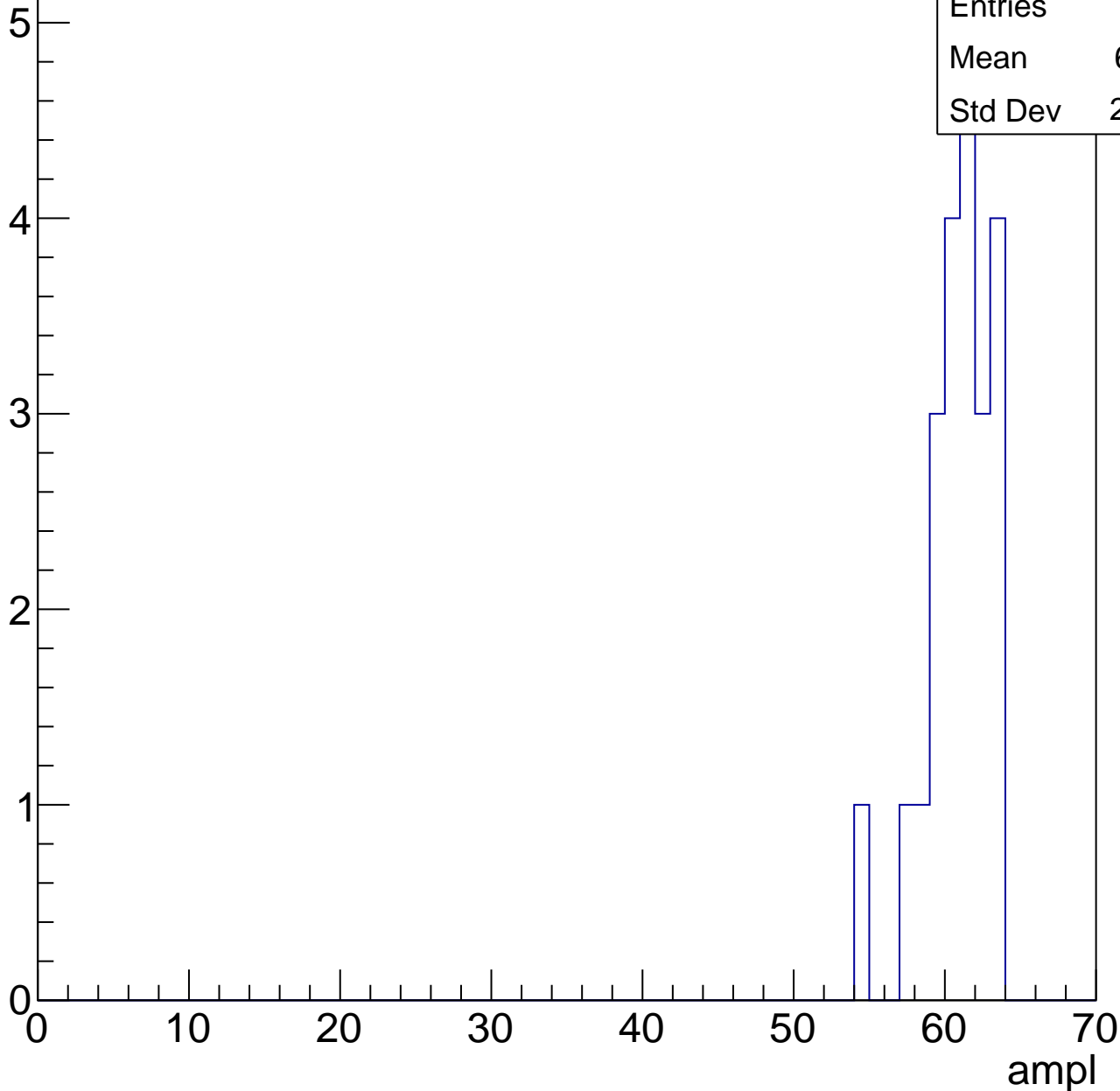


B1L103S, U14-ch43, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	22
Mean	60.41
Std Dev	2.146



B1L103S, U14-ch43, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

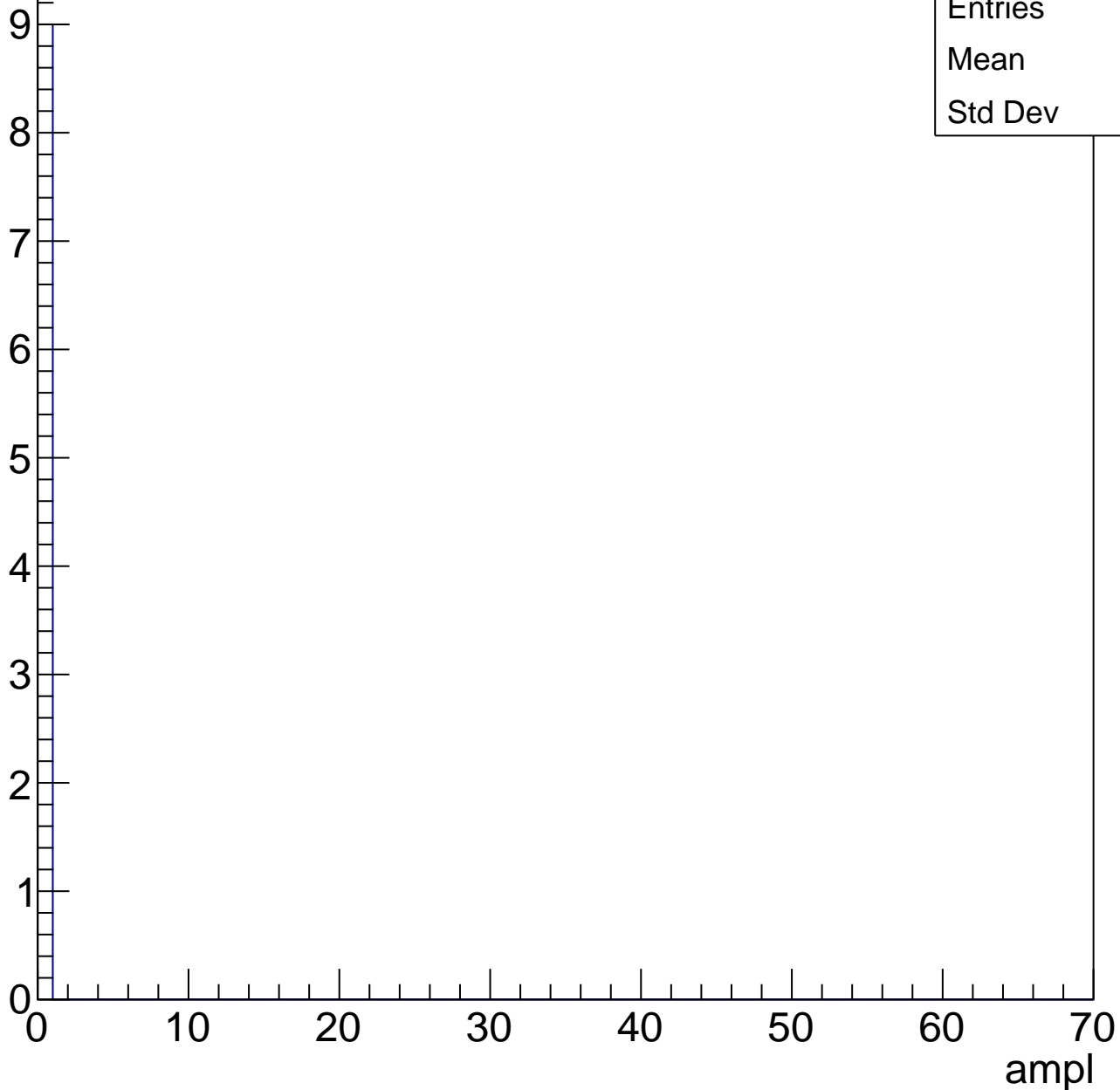


B1L103S, U14-ch43, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	9
Mean	0
Std Dev	0



B1L103S, U14-ch44, adc0

calib_packv5_041523_1651.root, FC#0, port C2

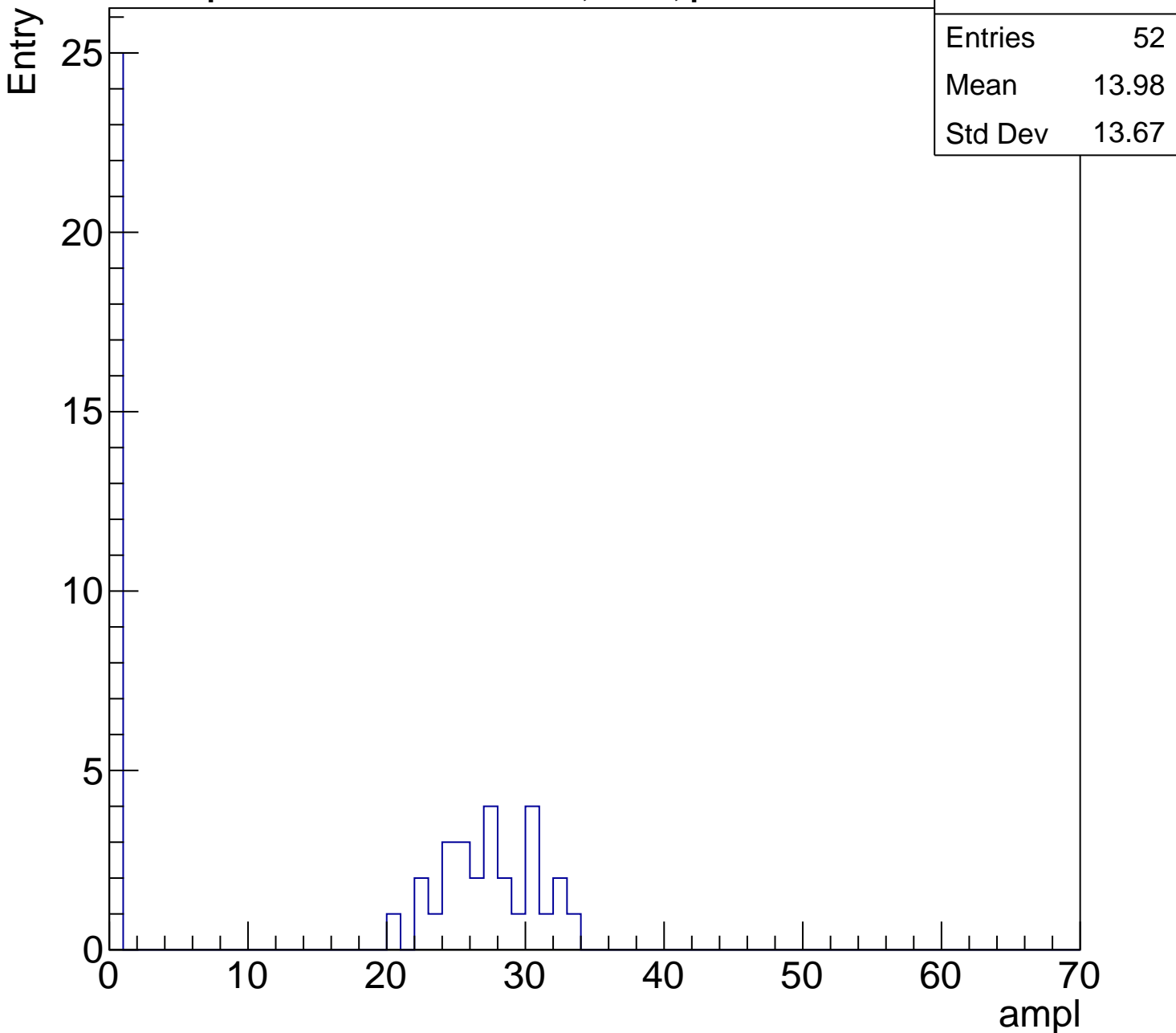
Entries	52
Mean	13.98
Std Dev	13.67

Entry

25
20
15
10
5
0

0 10 20 30 40 50 60 70

ampl

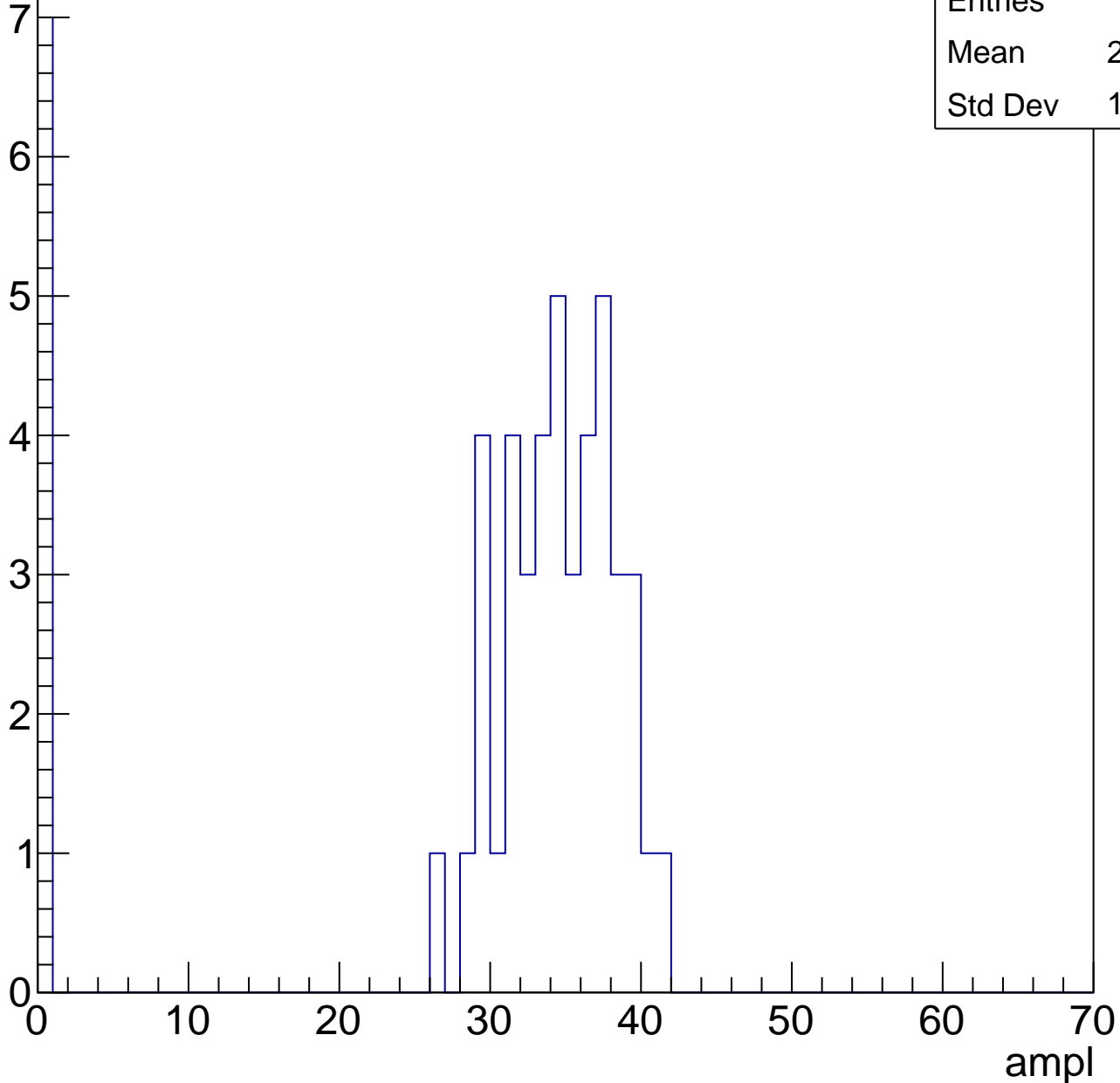


B1L103S, U14-ch44, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

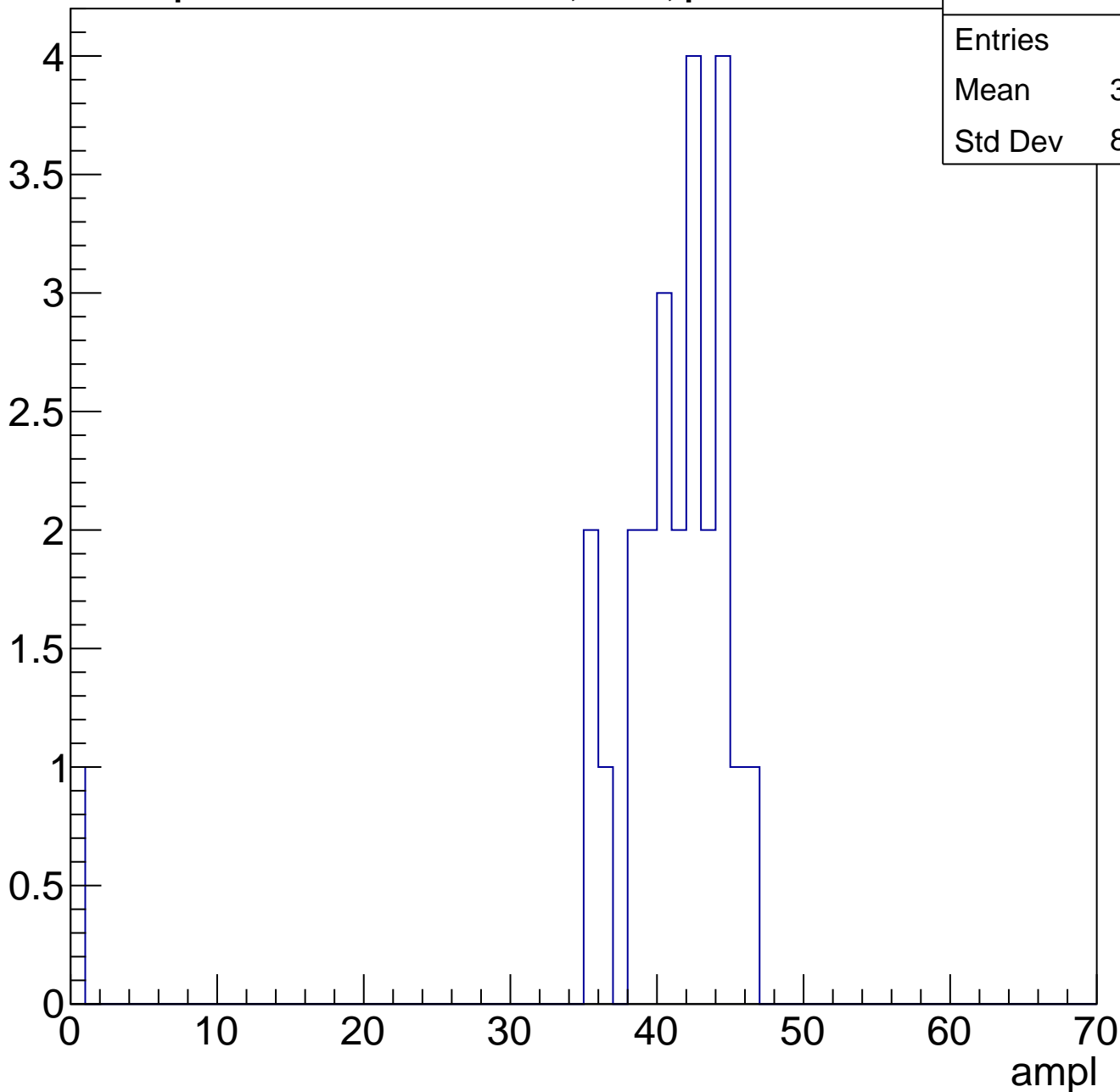
Entries	50
Mean	29.36
Std Dev	12.29



B1L103S, U14-ch44, adc2

calib_packv5_041523_1651.root, FC#0, port C2

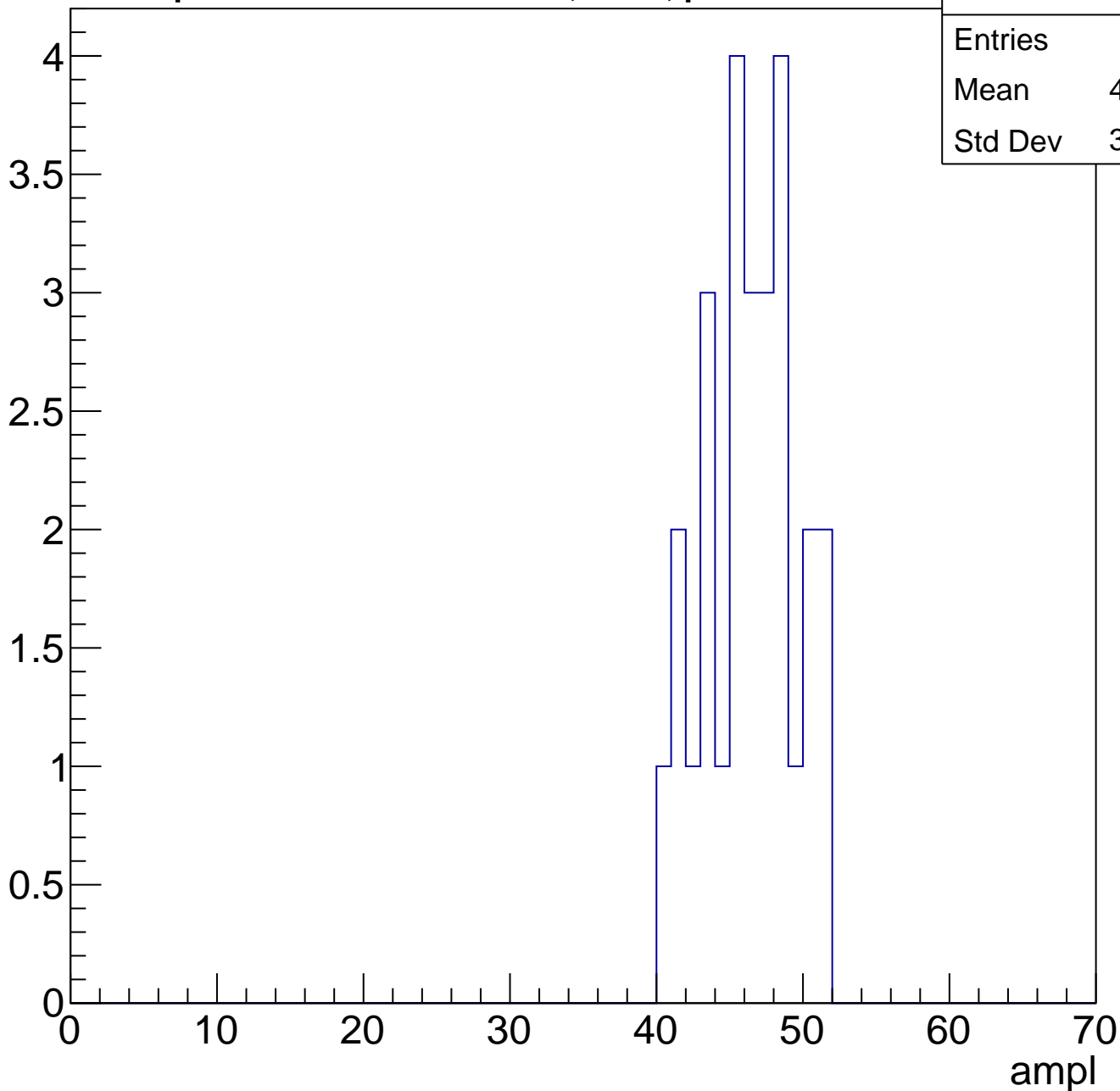
Entry



B1L103S, U14-ch44, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry



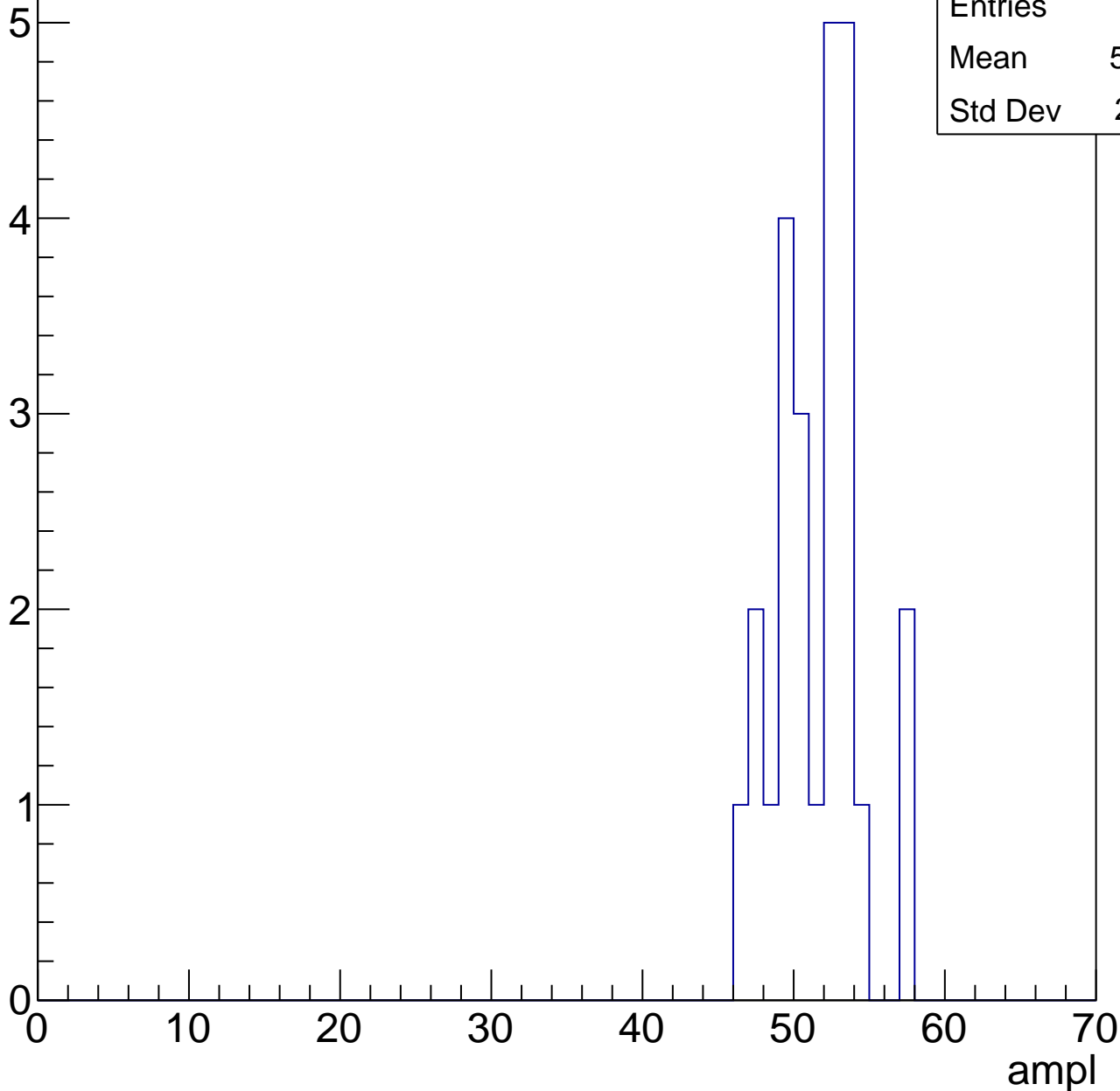
Entries	27
Mean	45.89
Std Dev	3.023

B1L103S, U14-ch44, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	25
Mean	51.12
Std Dev	2.761

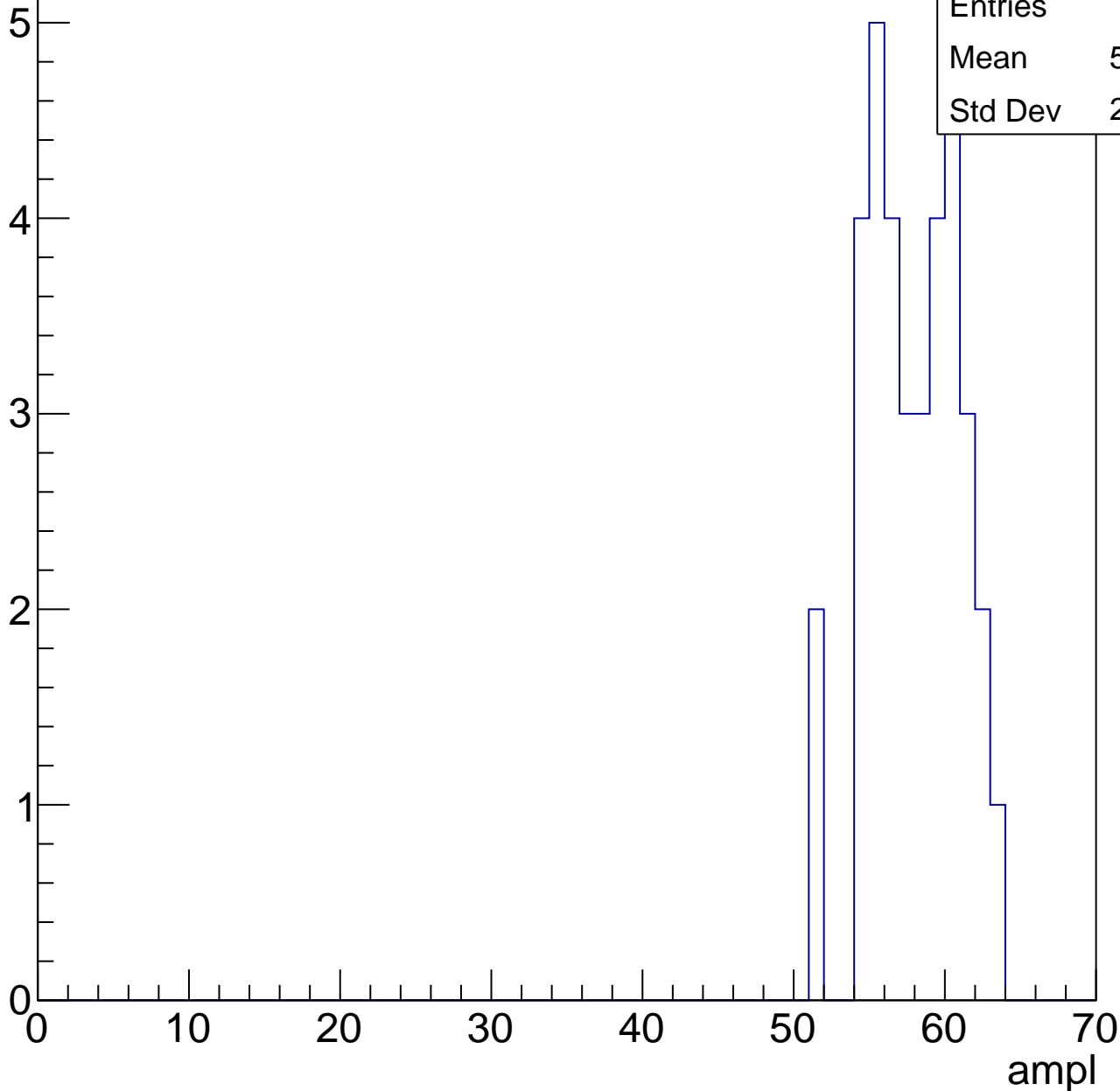


B1L103S, U14-ch44, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

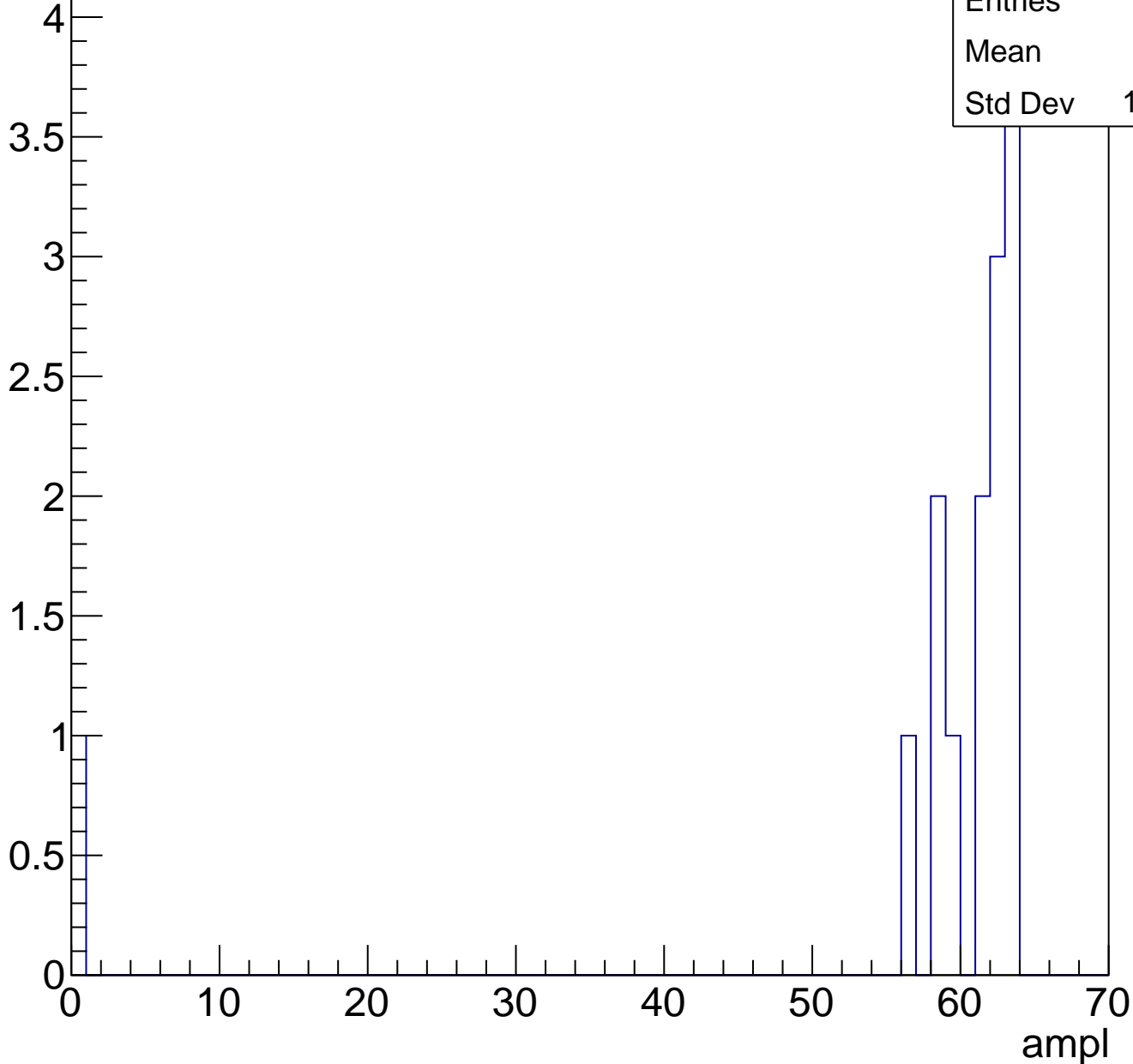
Entries	36
Mean	57.44
Std Dev	2.995



B1L103S, U14-ch44, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

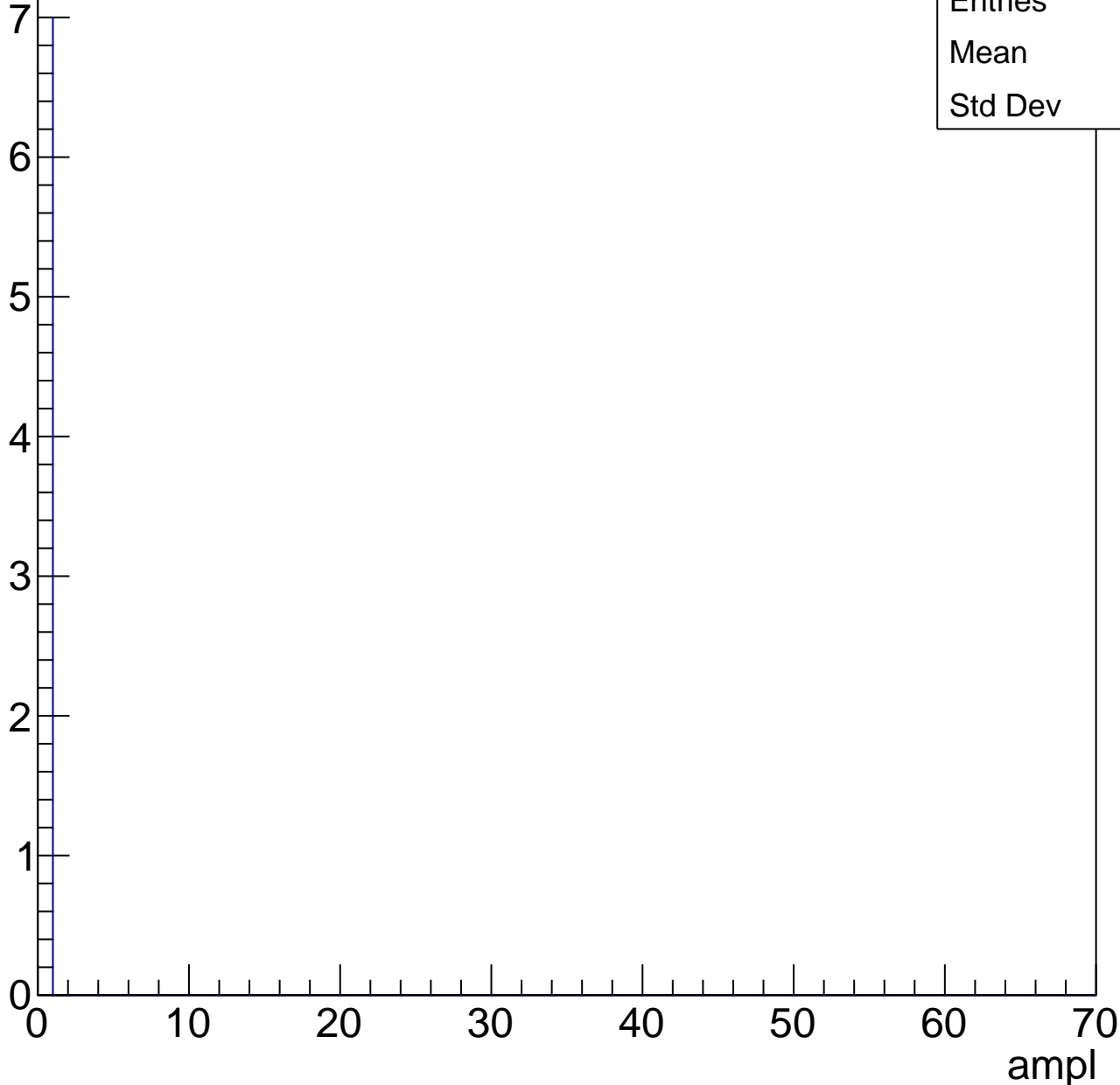


B1L103S, U14-ch44, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	7
Mean	0
Std Dev	0

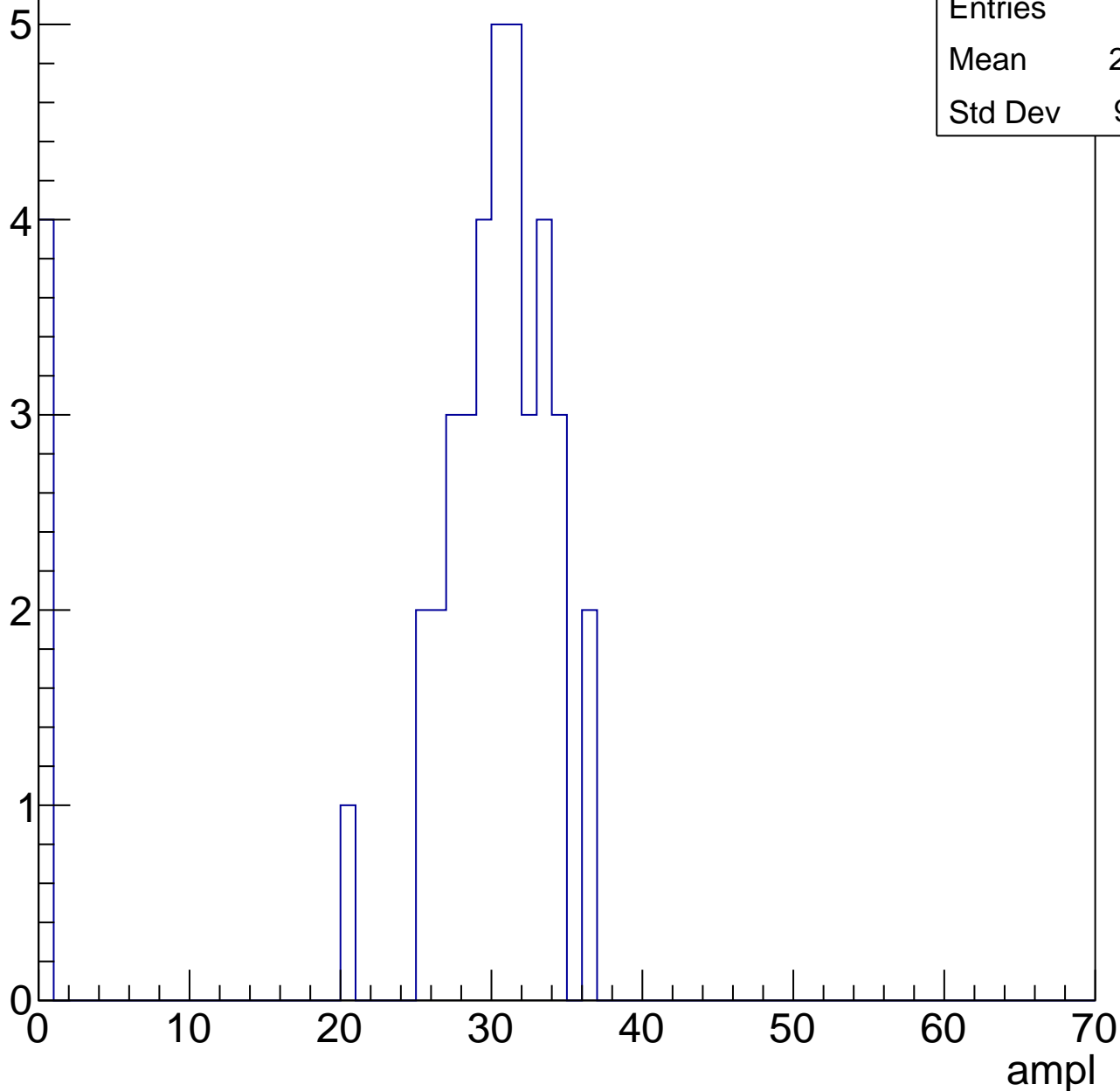


B1L103S, U14-ch45, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

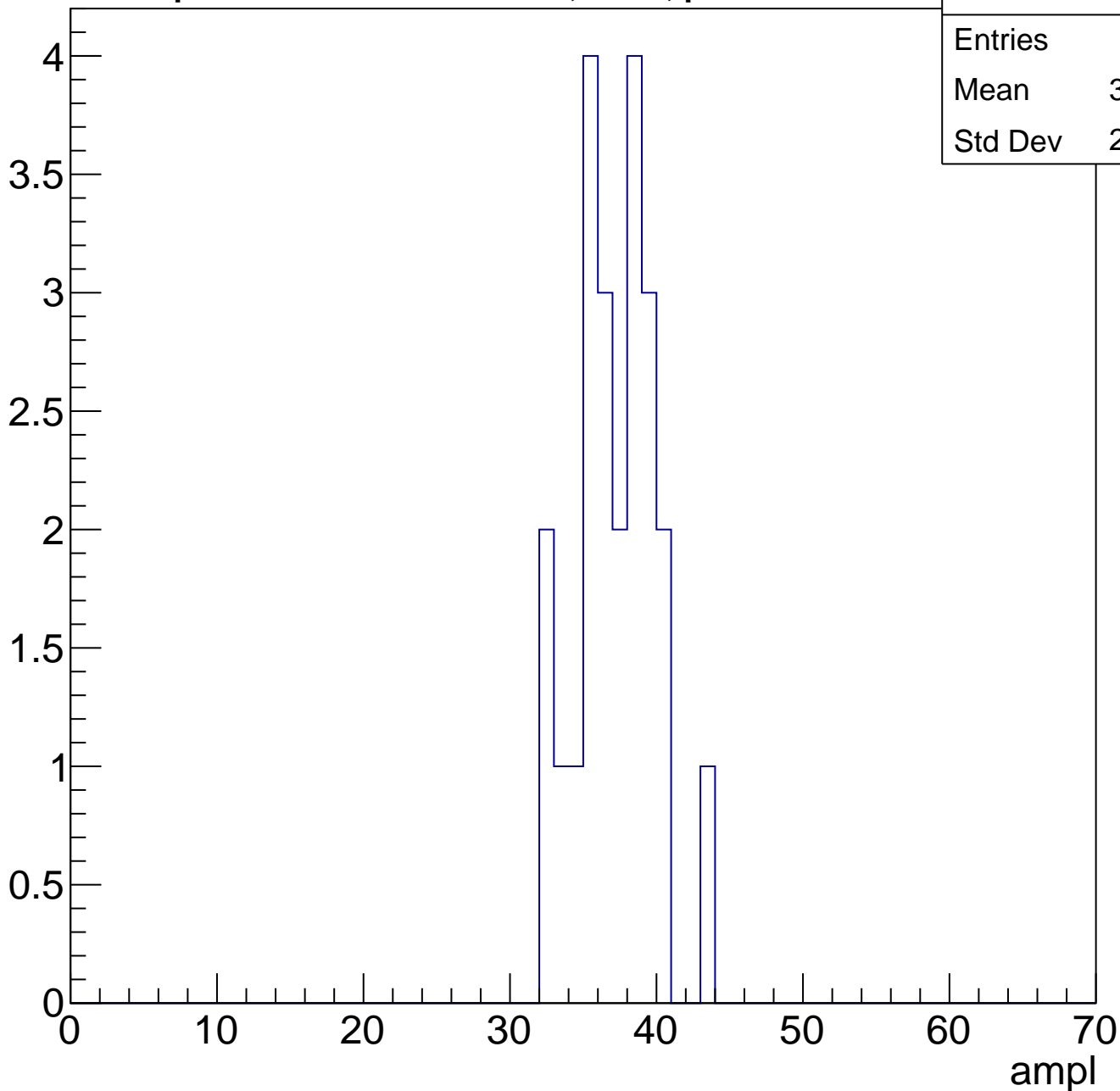
Entries	41
Mean	27.07
Std Dev	9.431



B1L103S, U14-ch45, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

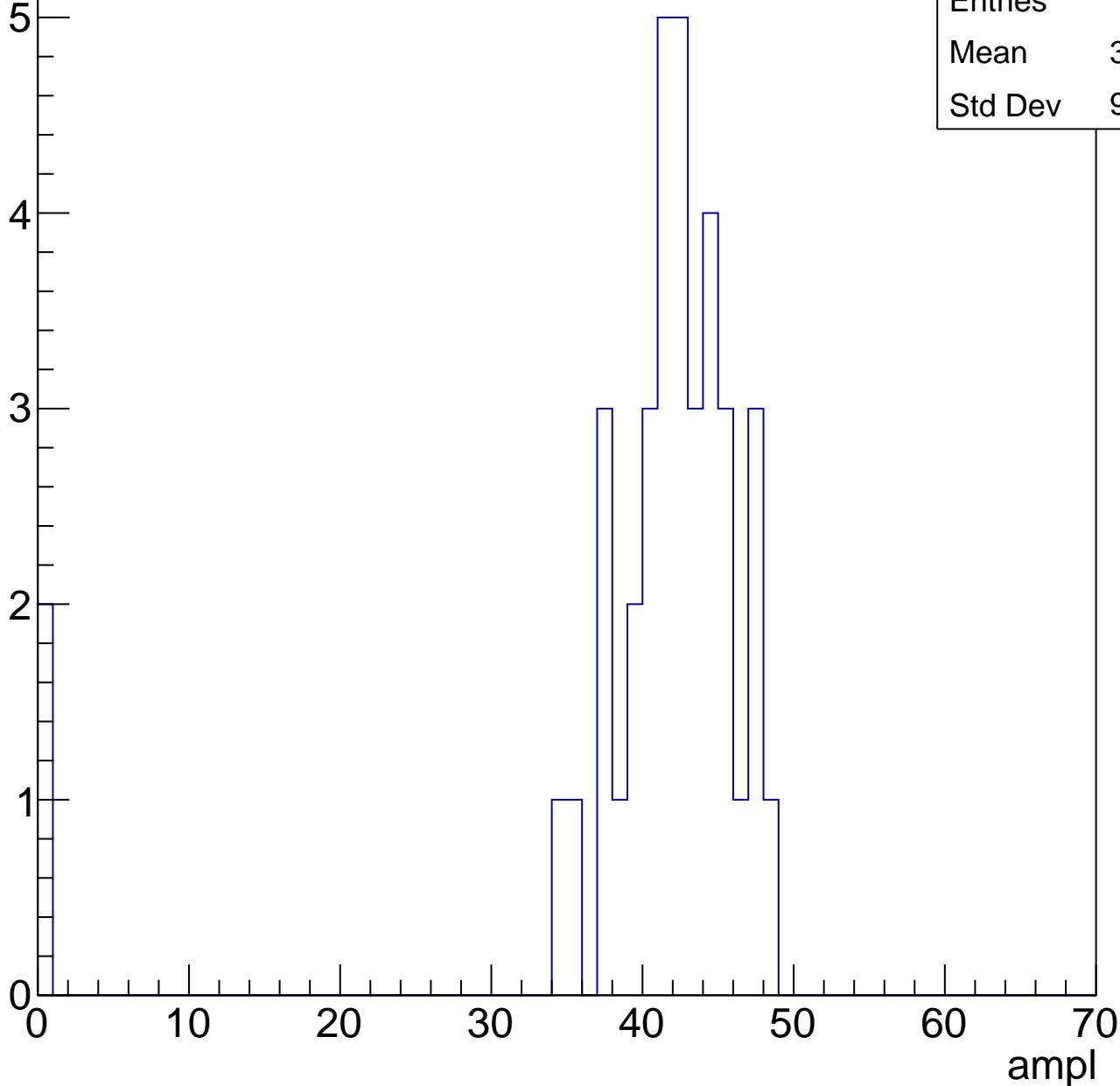


B1L103S, U14-ch45, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	38
Mean	39.63
Std Dev	9.903

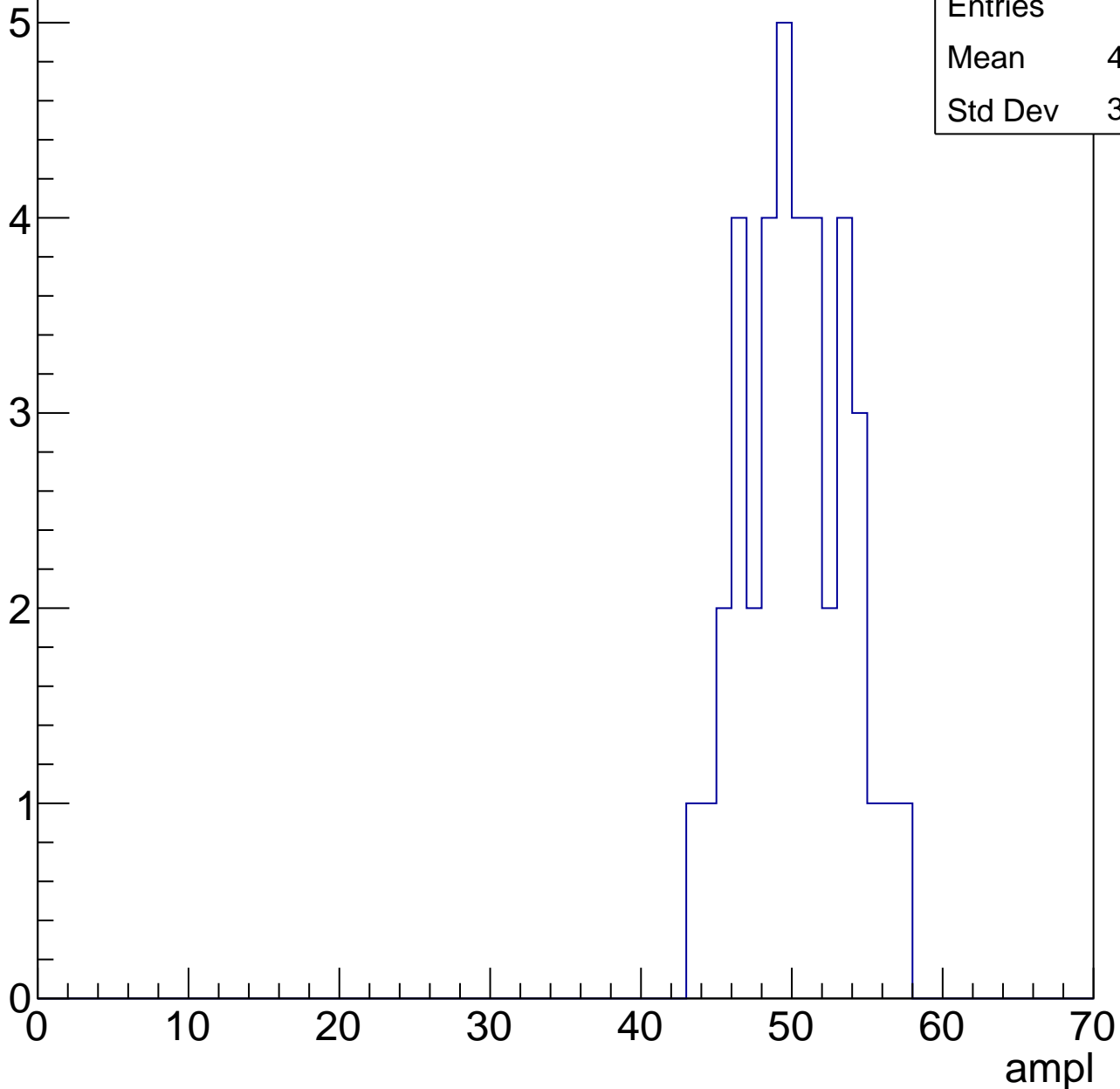


B1L103S, U14-ch45, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

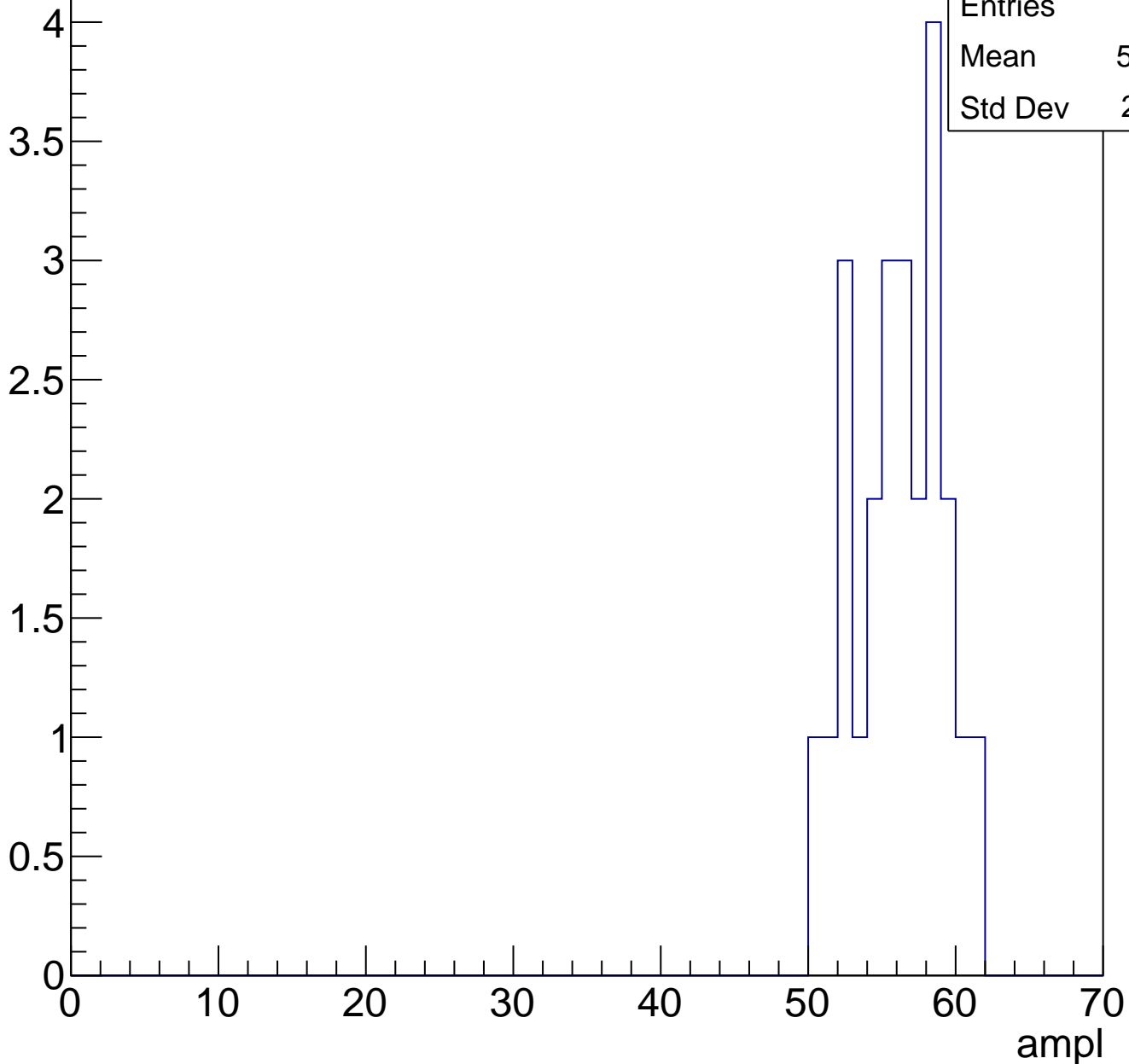
Entries	39
Mean	49.79
Std Dev	3.368



B1L103S, U14-ch45, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



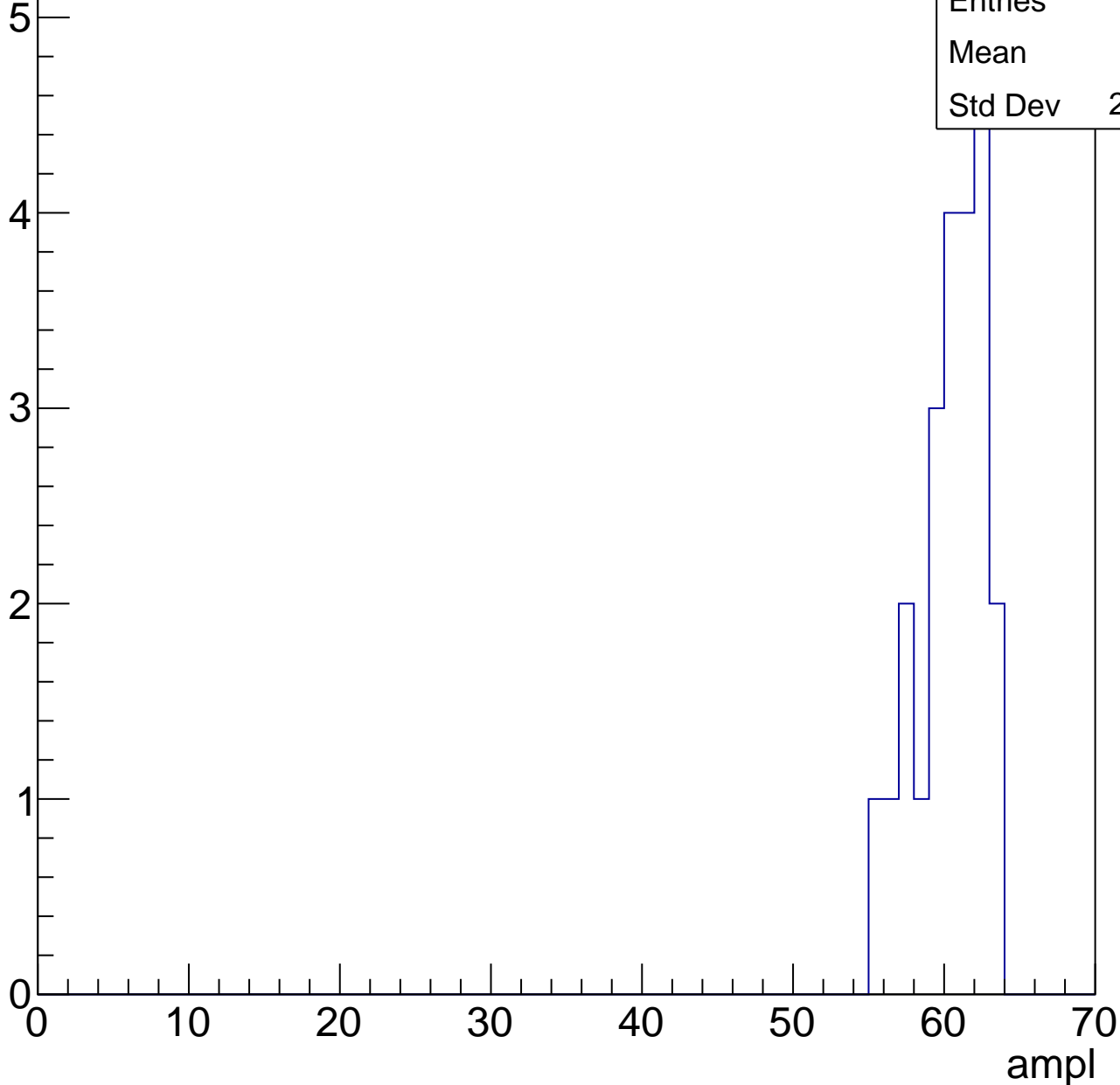
Entries	24
Mean	55.67
Std Dev	2.911

B1L103S, U14-ch45, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	23
Mean	60
Std Dev	2.167



B1L103S, U14-ch45, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch45, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

12
10
8
6
4
2
0

Entries	12
Mean	0
Std Dev	0

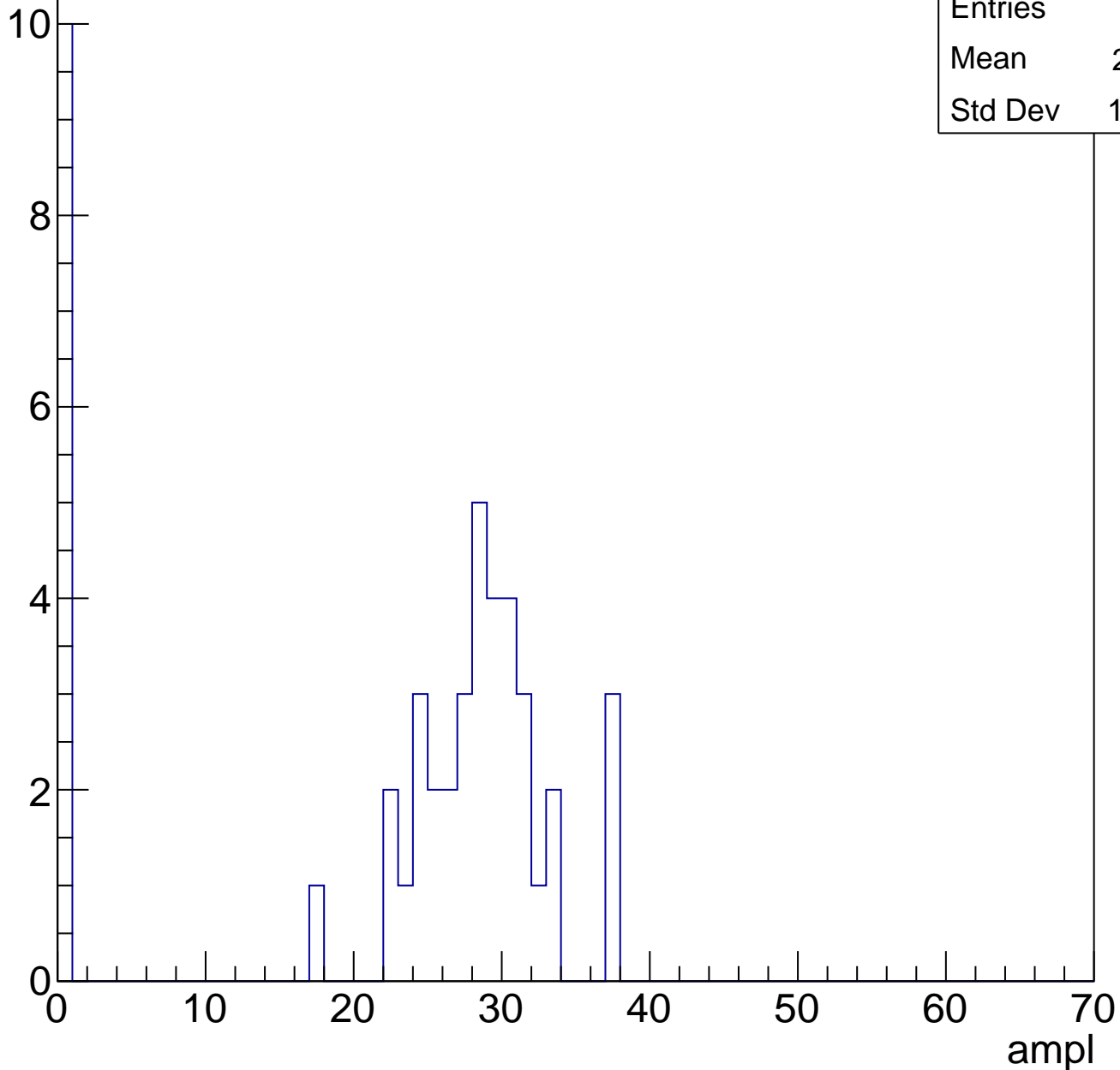
ampl

B1L103S, U14-ch46, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	46
Mean	22.11
Std Dev	12.24

Entry

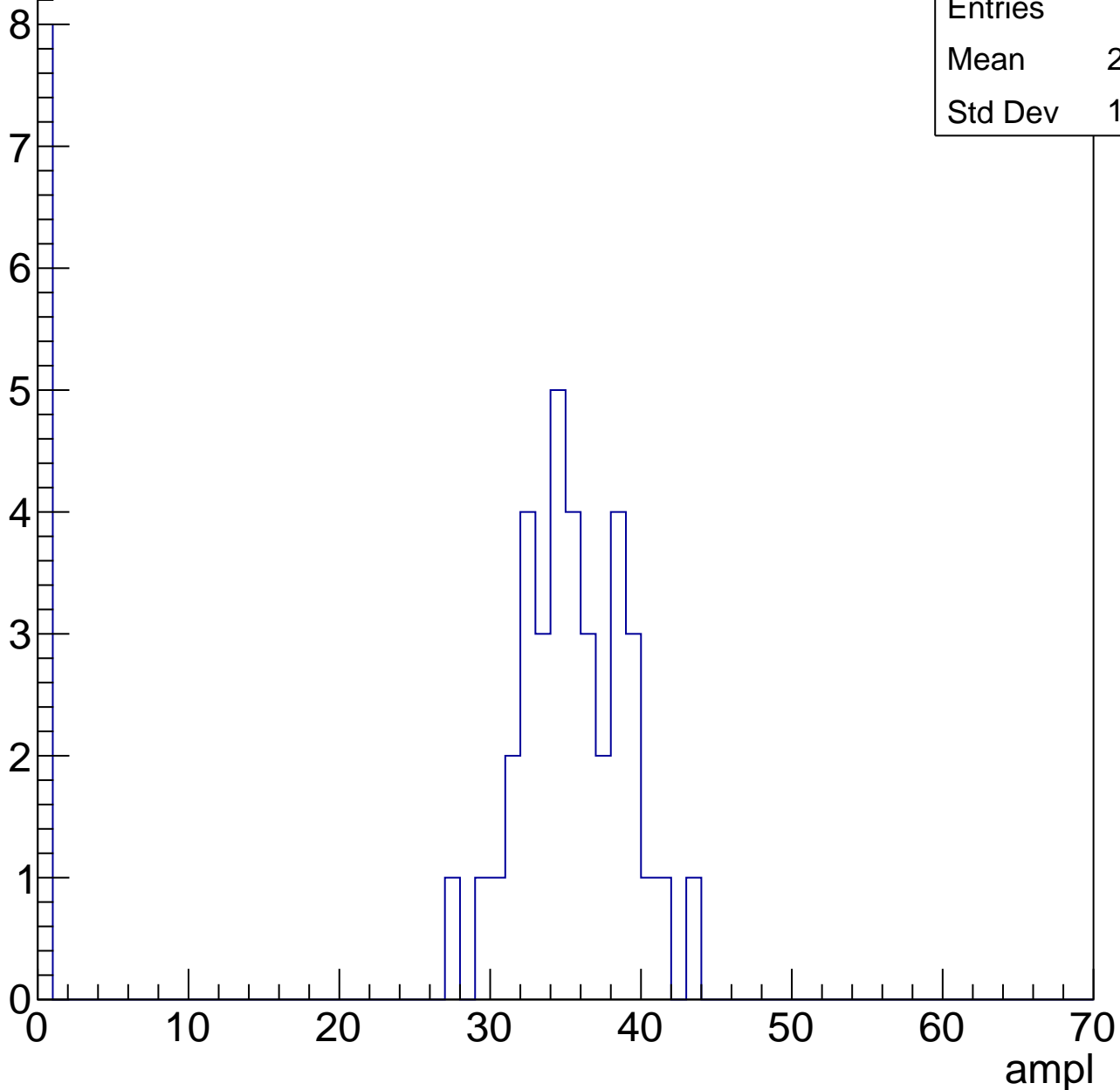


B1L103S, U14-ch46, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

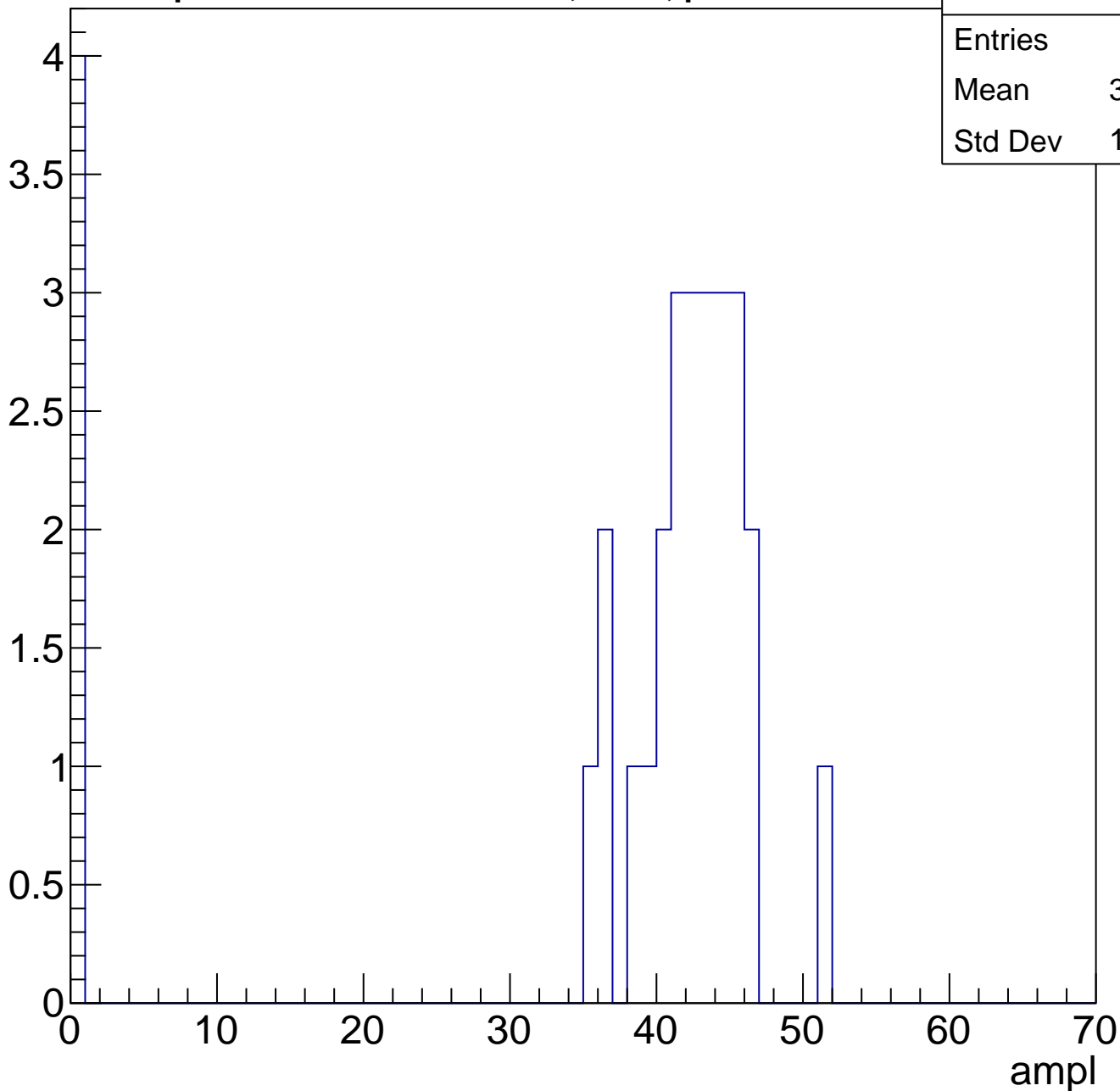
Entries	44
Mean	28.64
Std Dev	13.86



B1L103S, U14-ch46, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

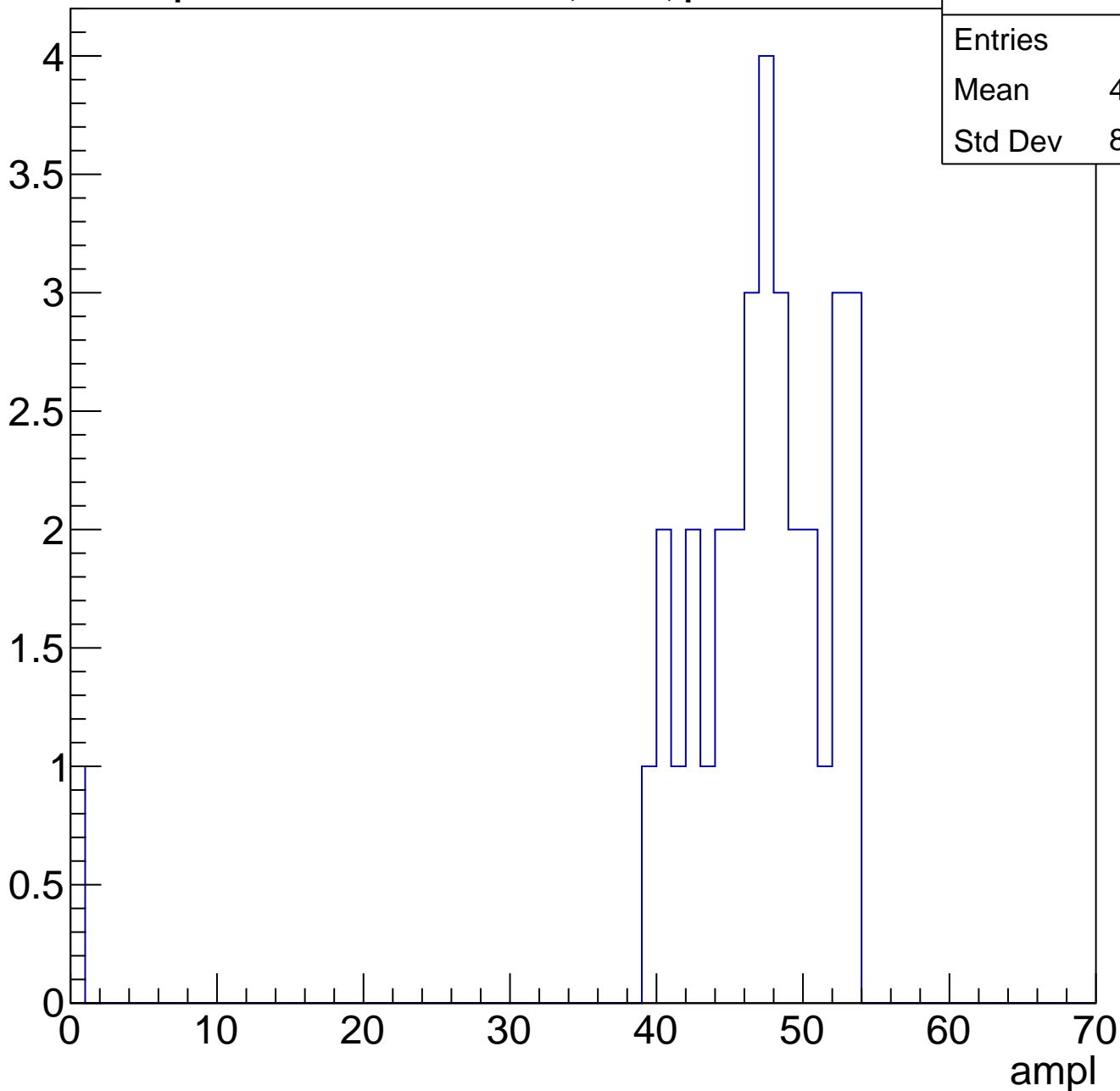


Entries	29
Mean	36.28
Std Dev	14.88

B1L103S, U14-ch46, adc3

calib_packv5_041523_1651.root, FC#0, port C2

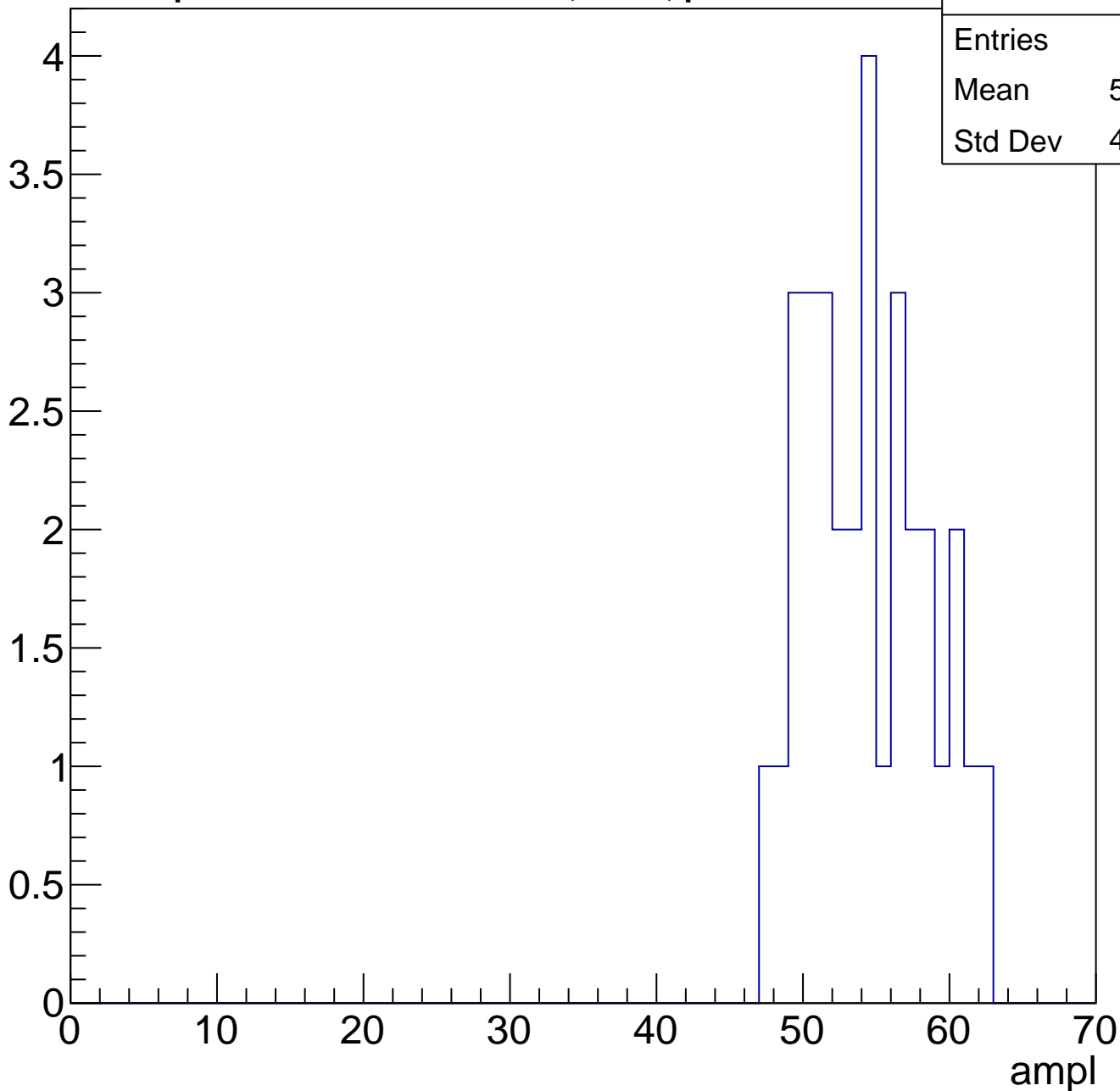
Entry



B1L103S, U14-ch46, adc4

calib_packv5_041523_1651.root, FC#0, port C2

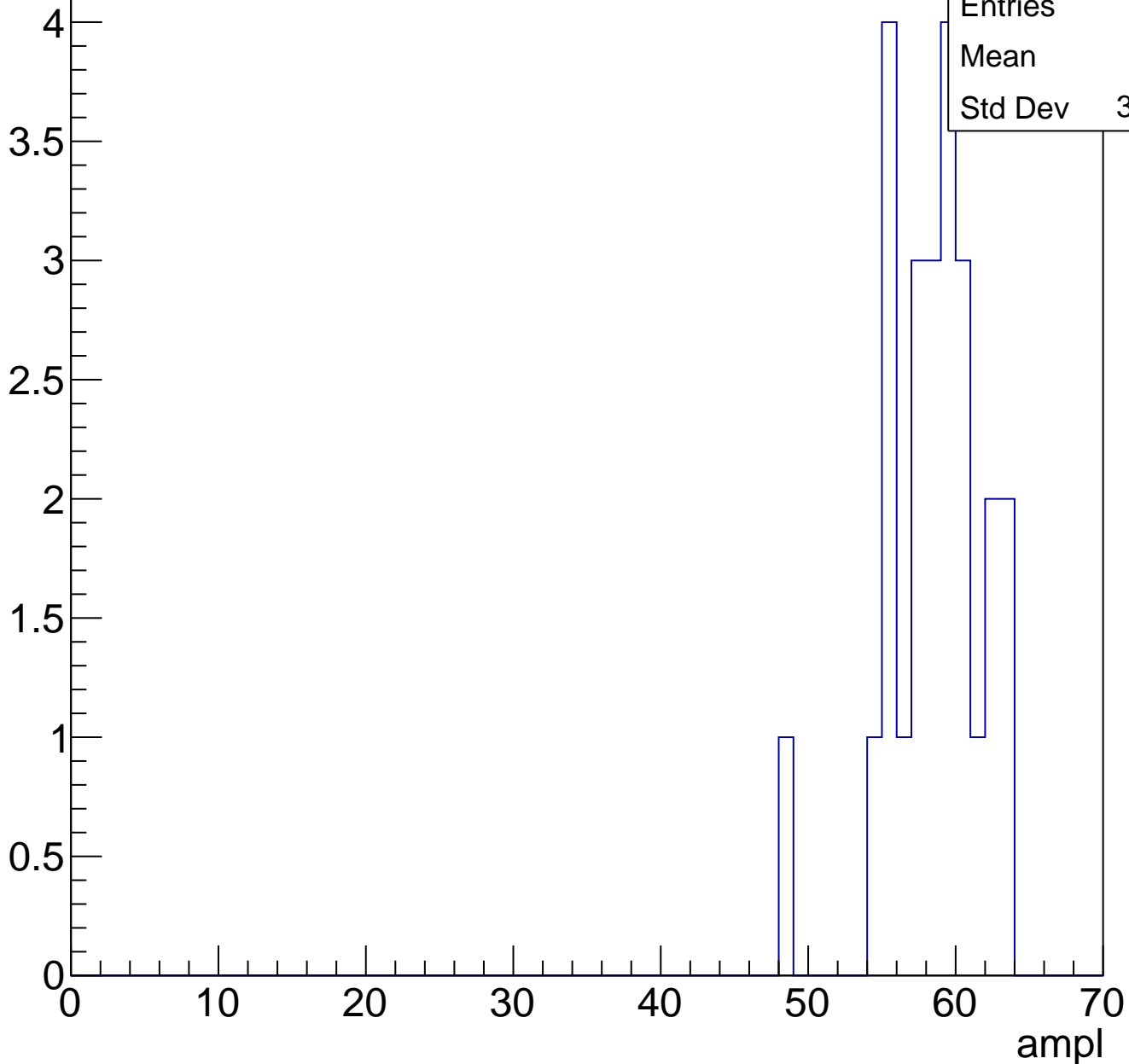
Entry



B1L103S, U14-ch46, adc5

calib_packv5_041523_1651.root, FC#0, port C2

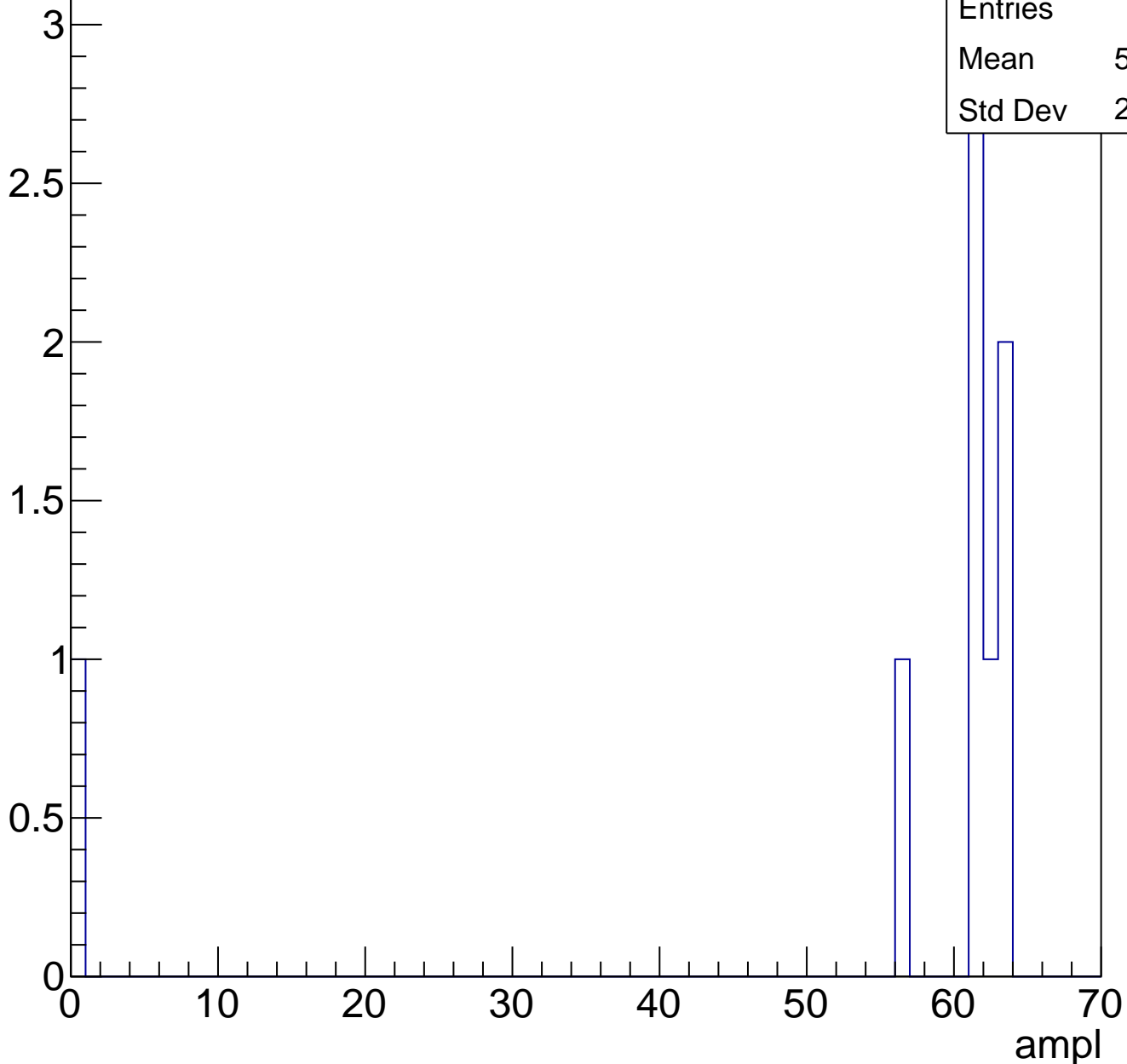
Entry



B1L103S, U14-ch46, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

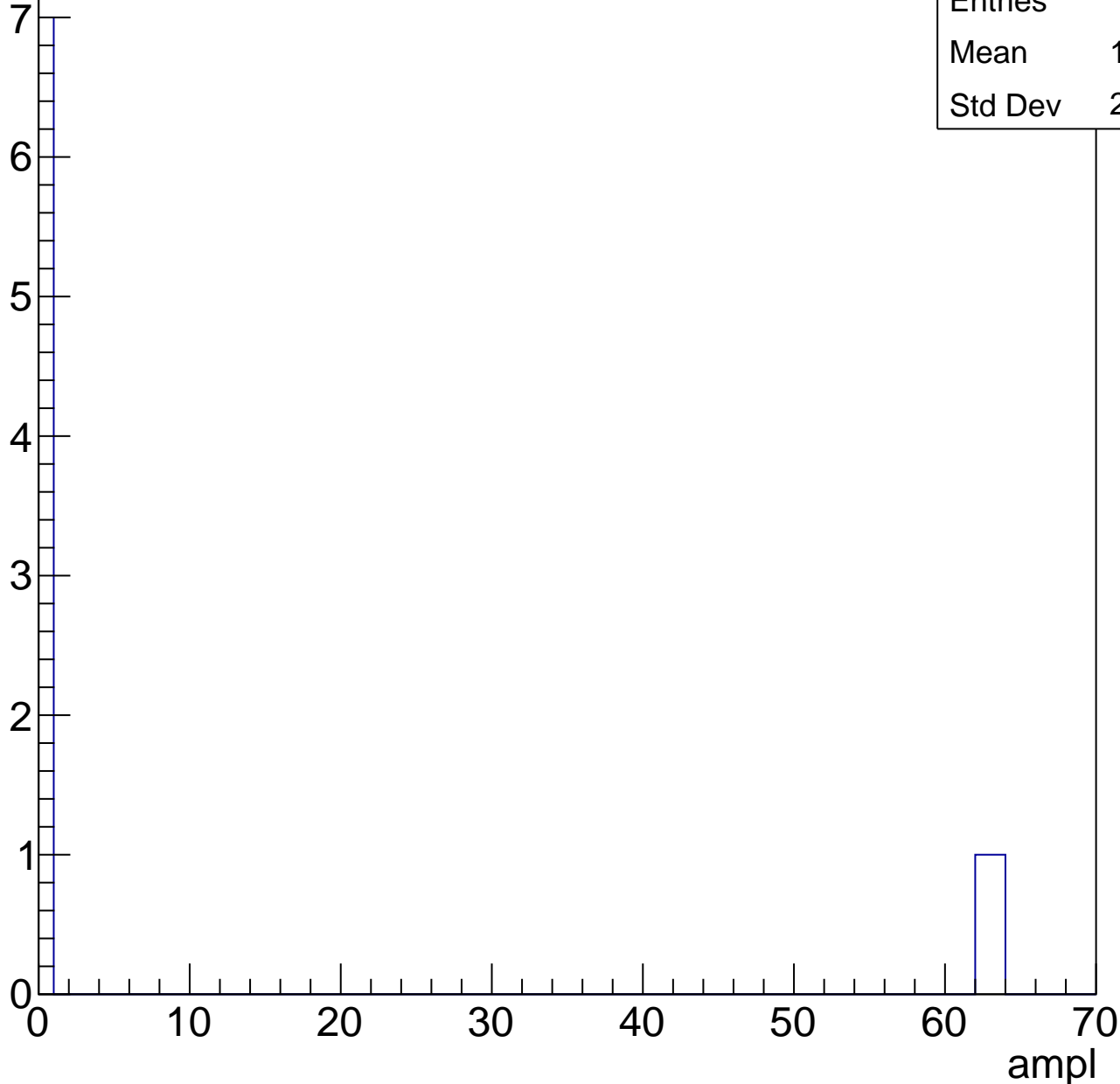


B1L103S, U14-ch46, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	9
Mean	13.89
Std Dev	25.98

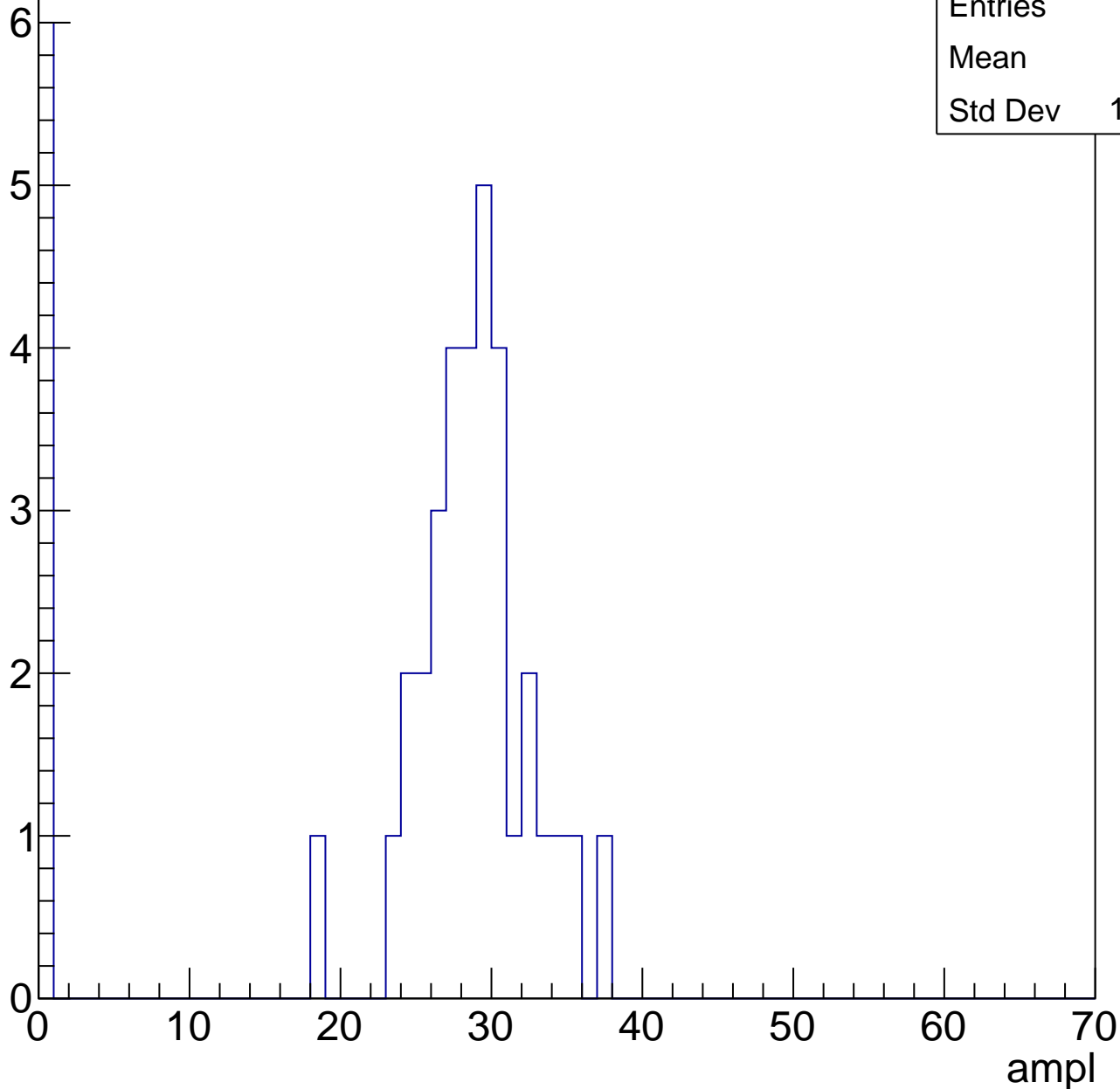


B1L103S, U14-ch47, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	24
Std Dev	10.77

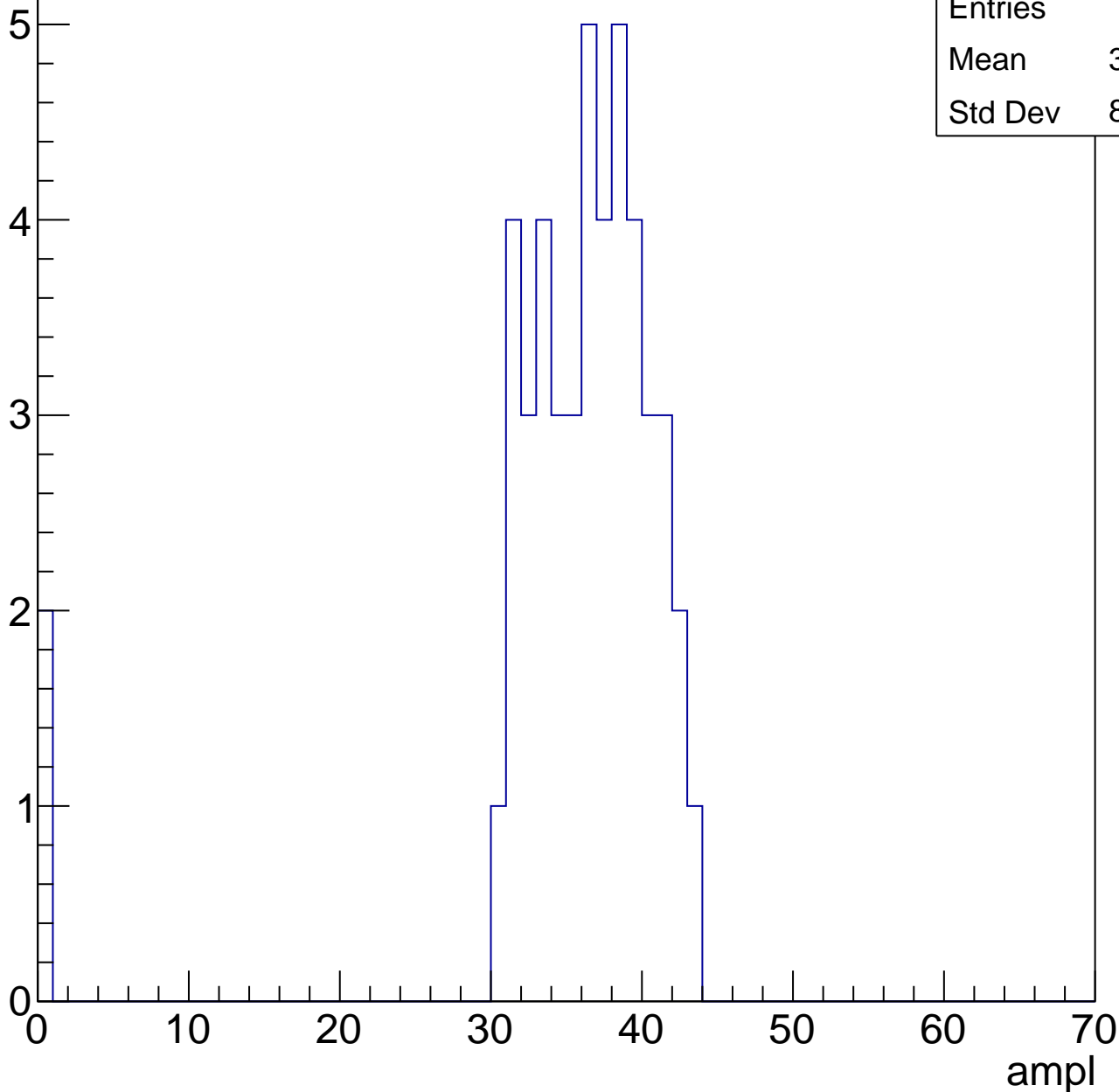


B1L103S, U14-ch47, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

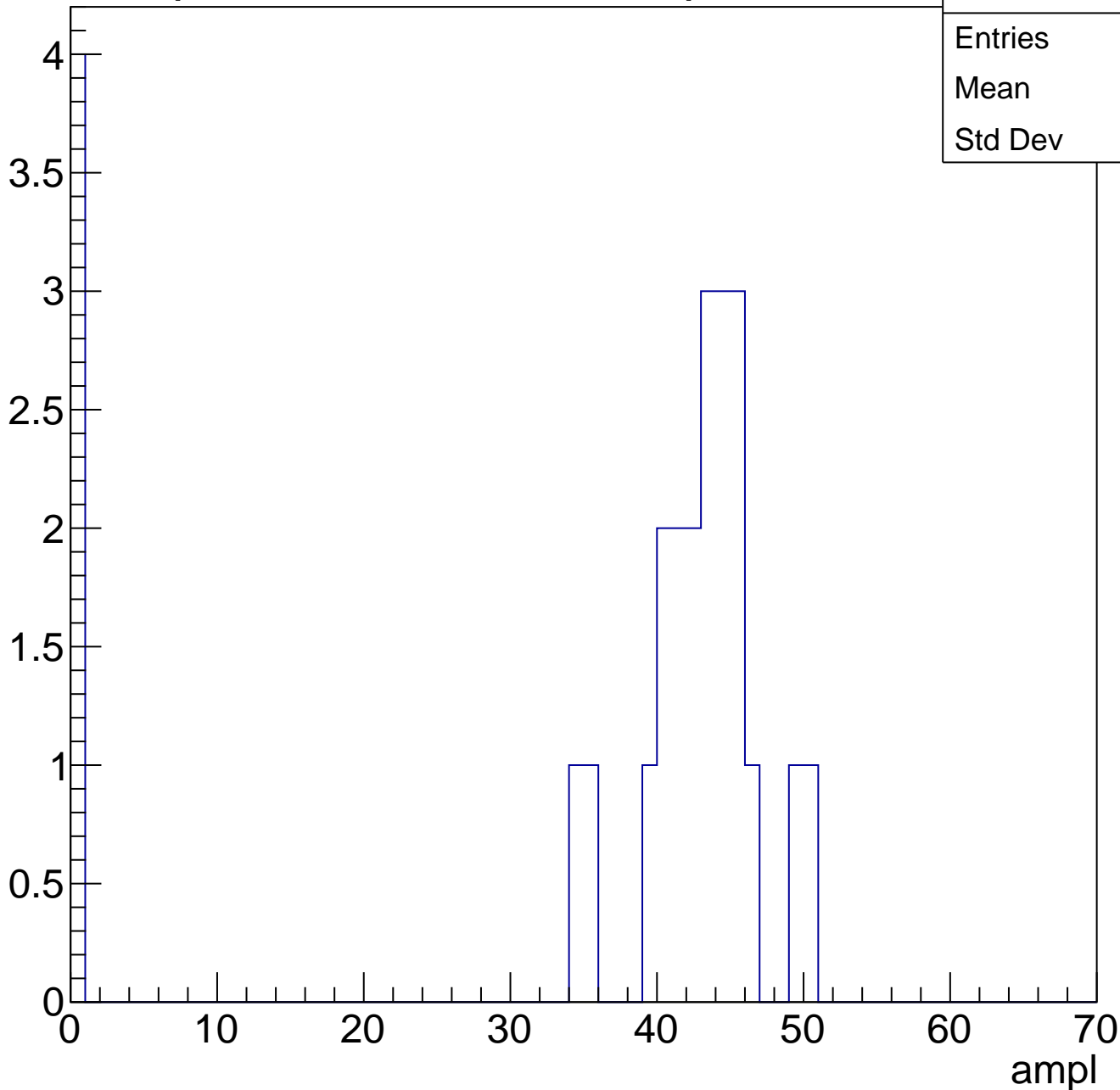
Entries	47
Mean	34.74
Std Dev	8.065



B1L103S, U14-ch47, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry



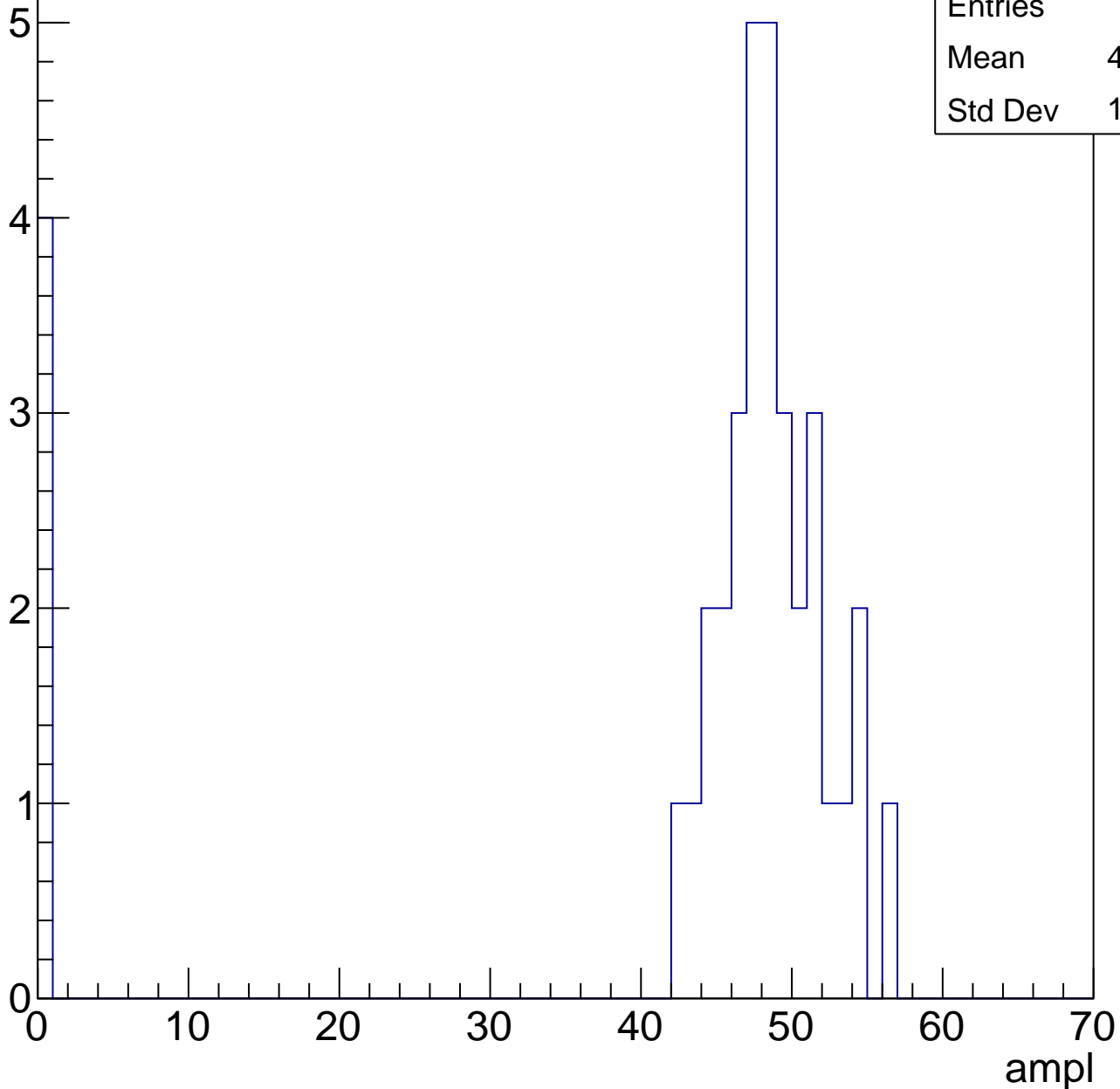
Entries	25
Mean	35.8
Std Dev	16

B1L103S, U14-ch47, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

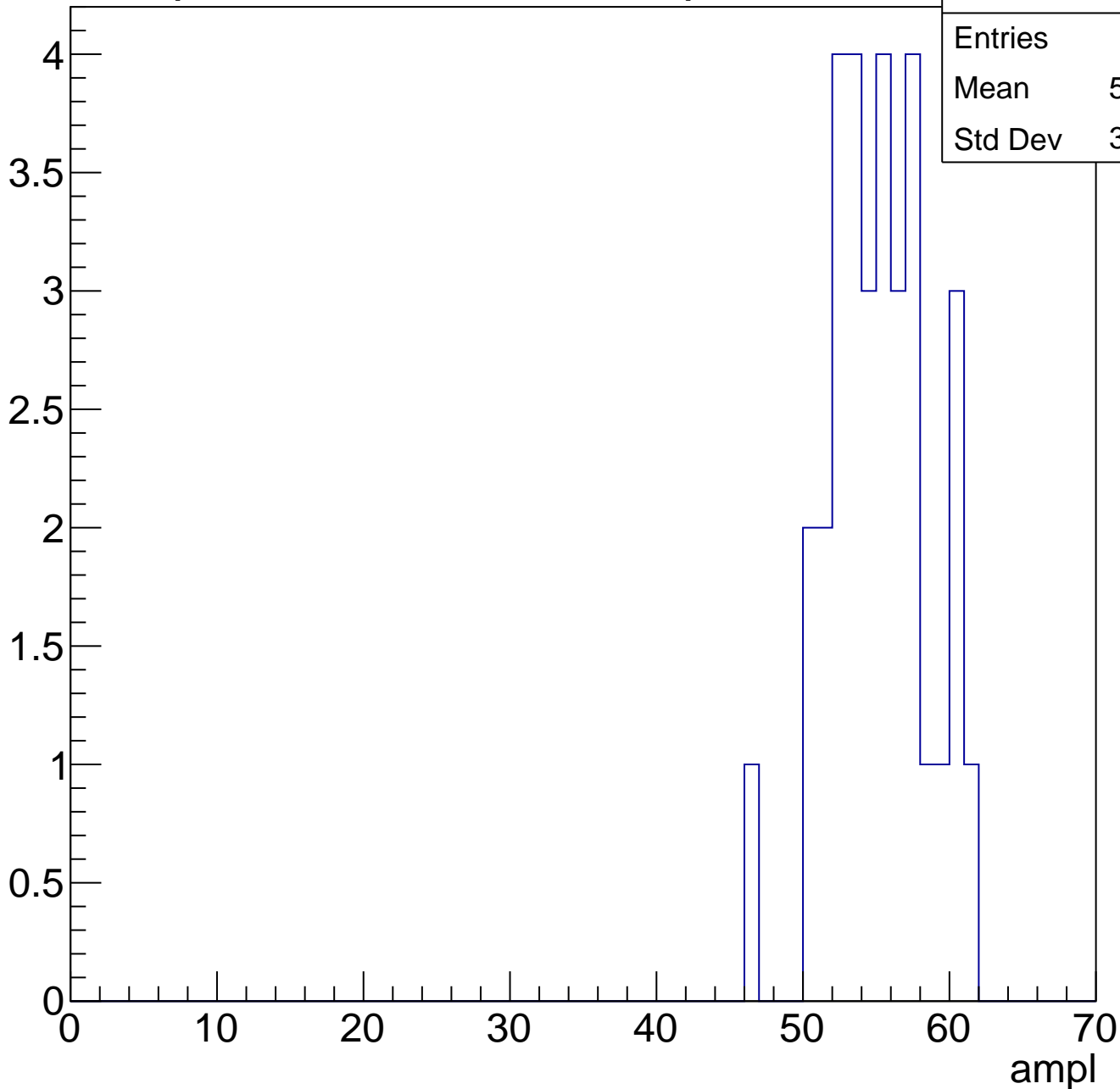
Entries	36
Mean	42.92
Std Dev	15.48



B1L103S, U14-ch47, adc4

calib_packv5_041523_1651.root, FC#0, port C2

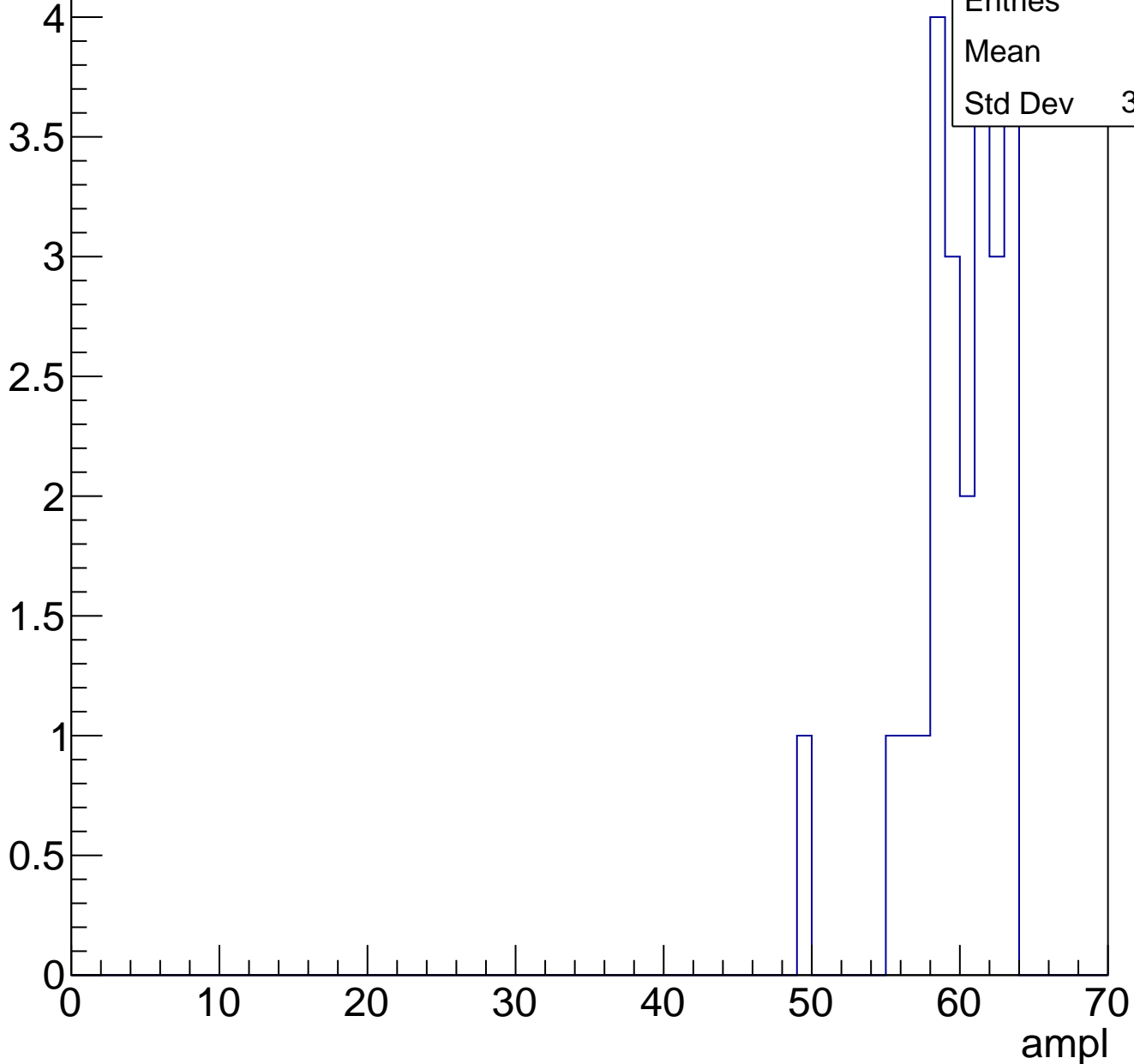
Entry



B1L103S, U14-ch47, adc5

calib_packv5_041523_1651.root, FC#0, port C2

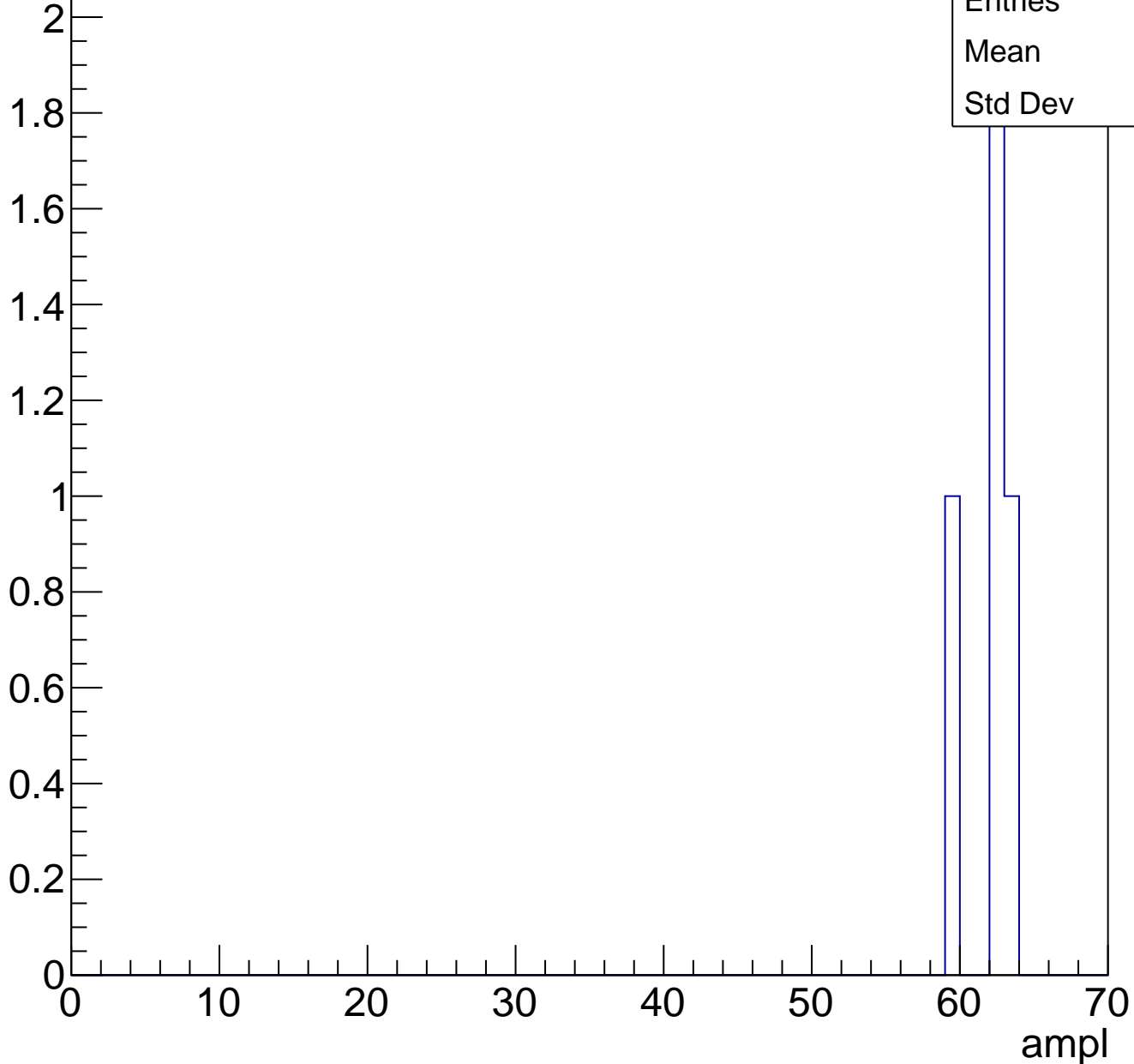
Entry



B1L103S, U14-ch47, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

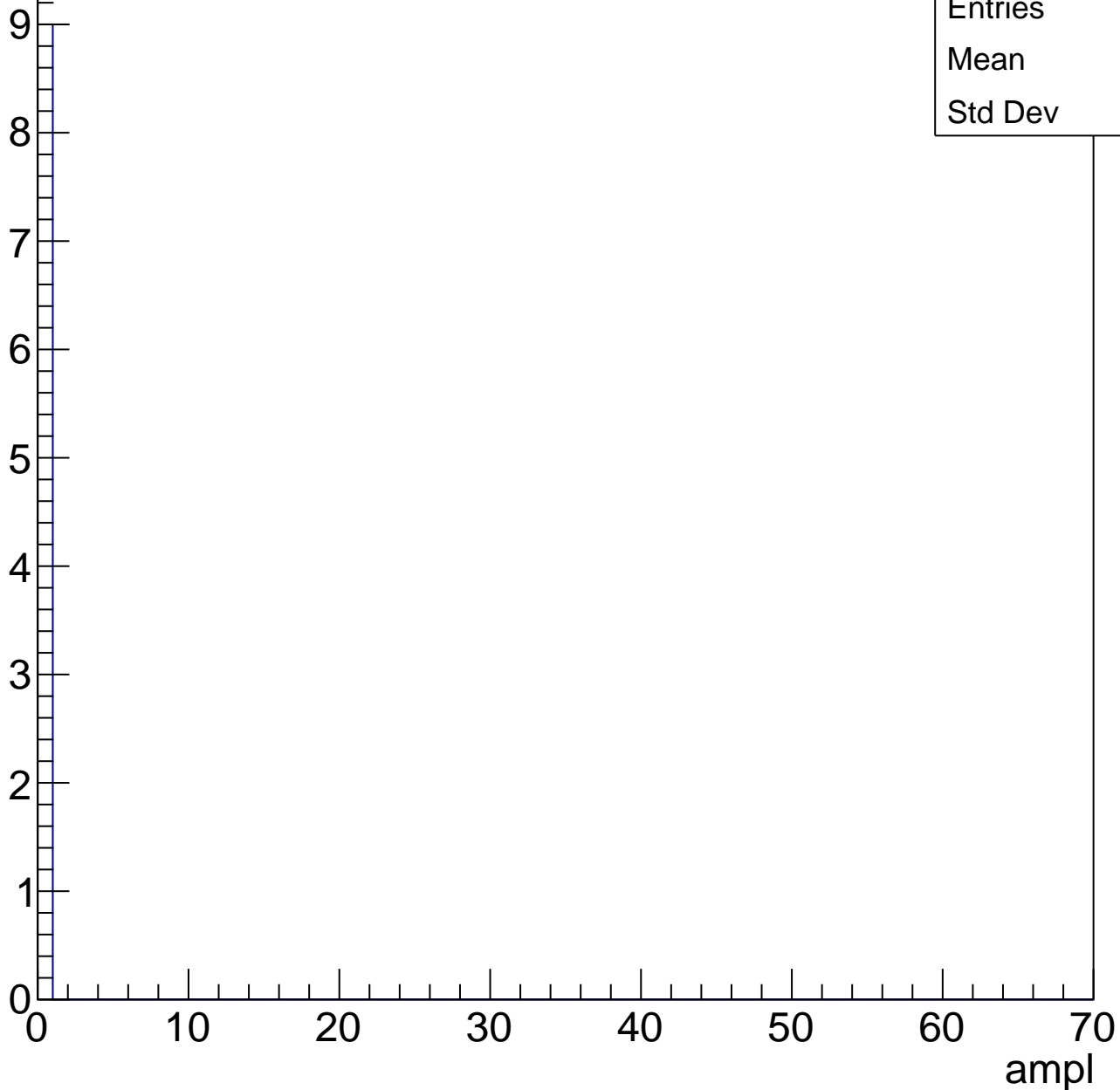


B1L103S, U14-ch47, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	9
Mean	0
Std Dev	0

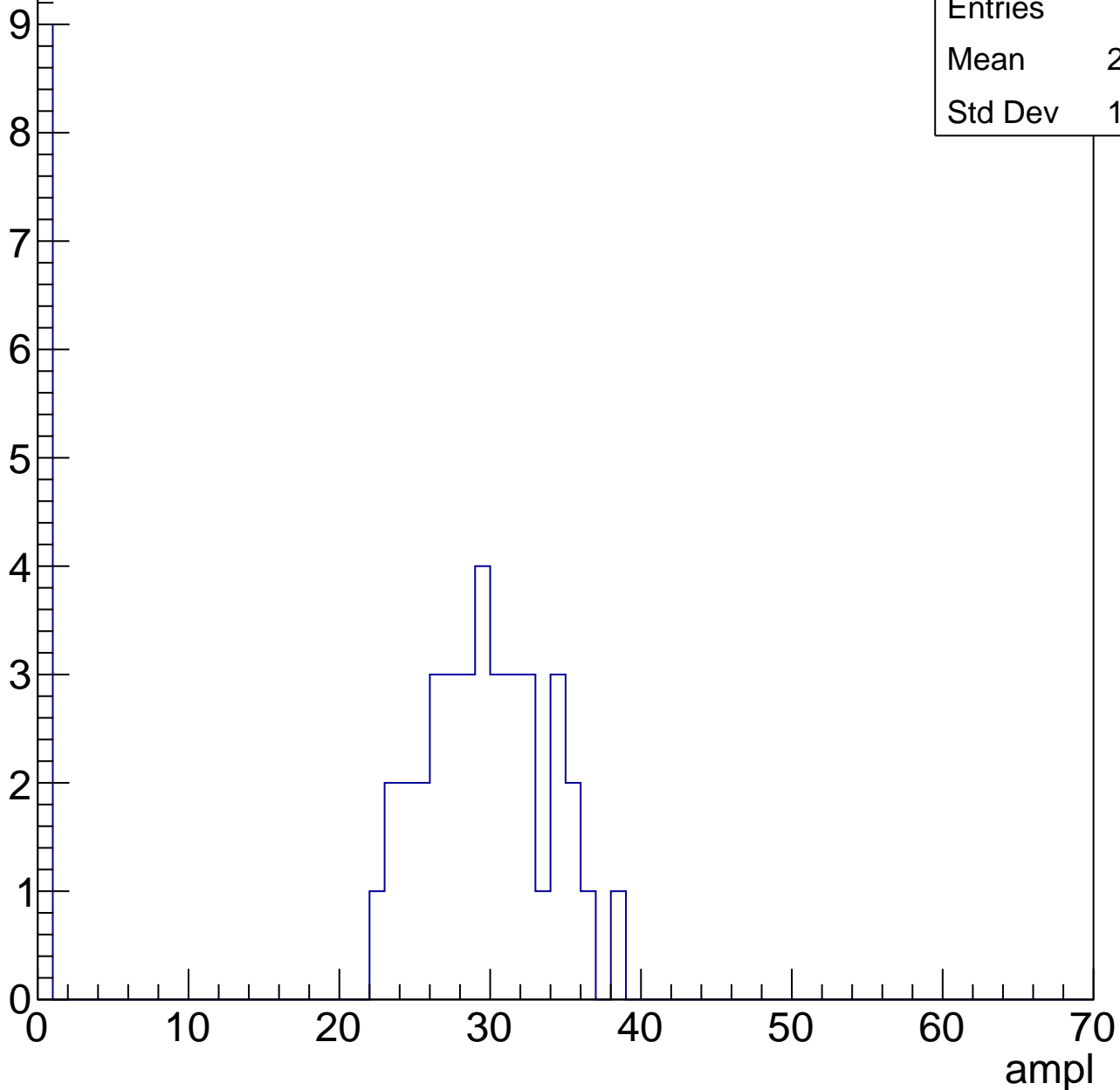


B1L103S, U14-ch48, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

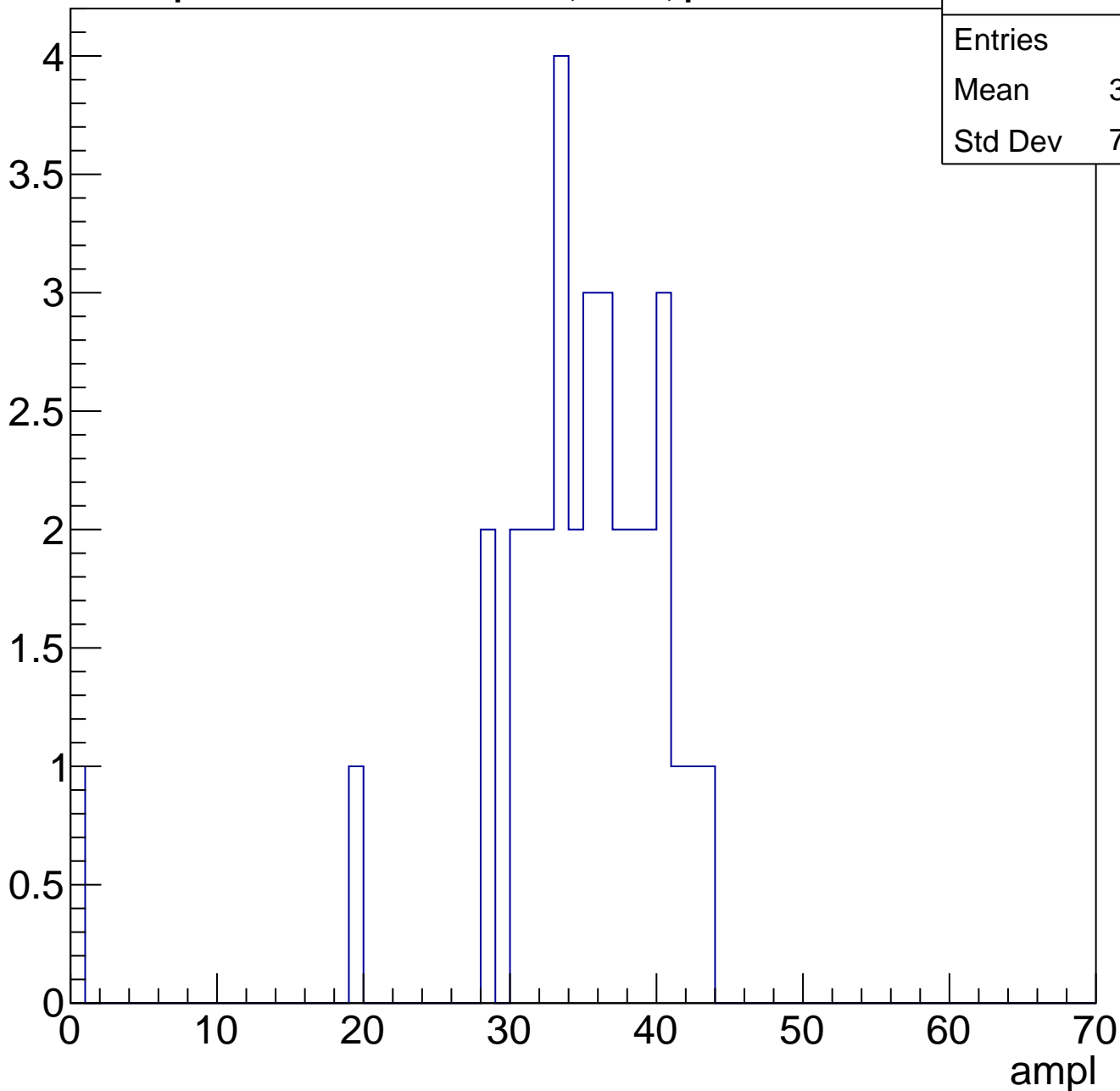
Entries	46
Mean	23.54
Std Dev	12.14



B1L103S, U14-ch48, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

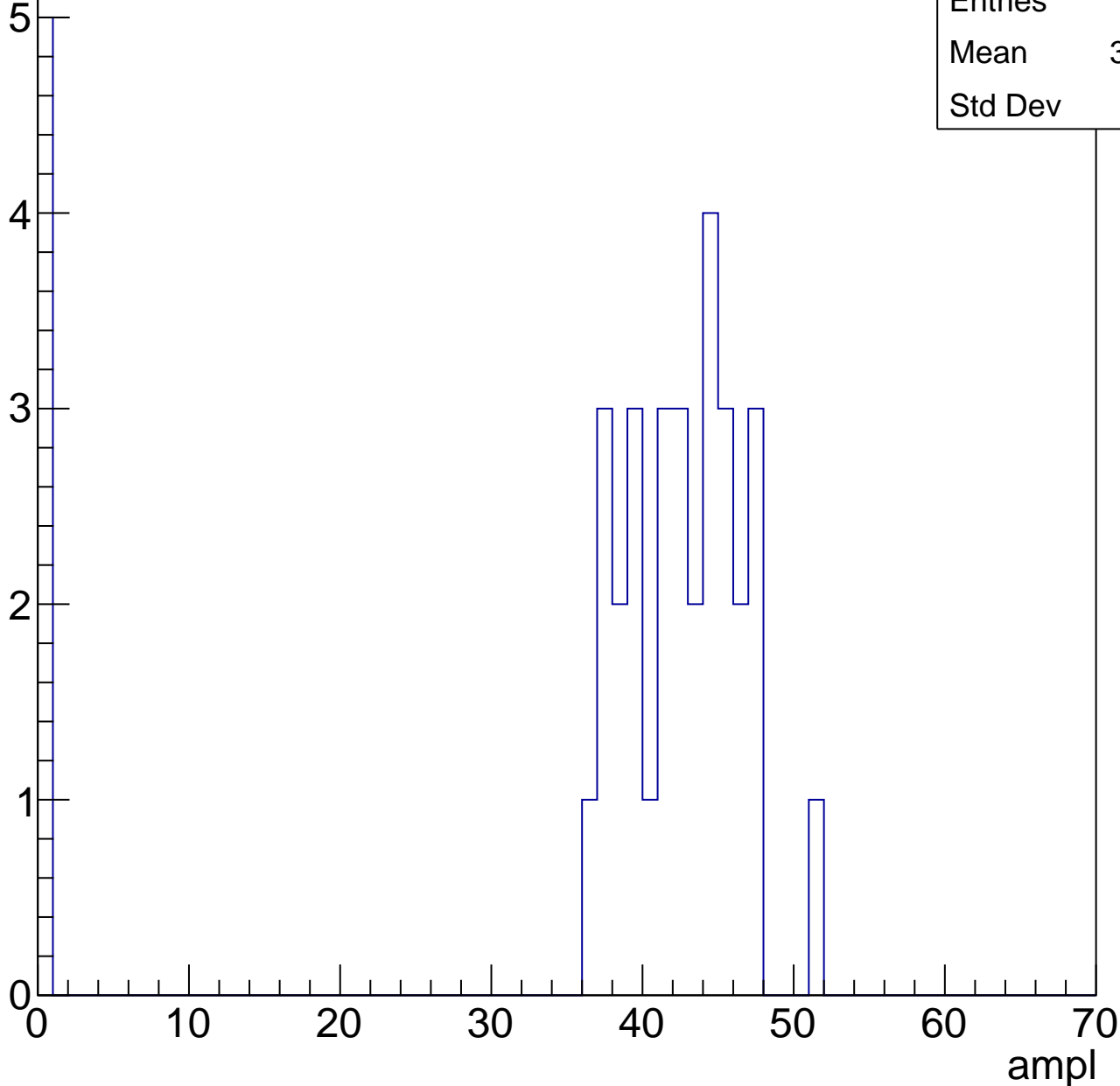


B1L103S, U14-ch48, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	36
Mean	36.39
Std Dev	15

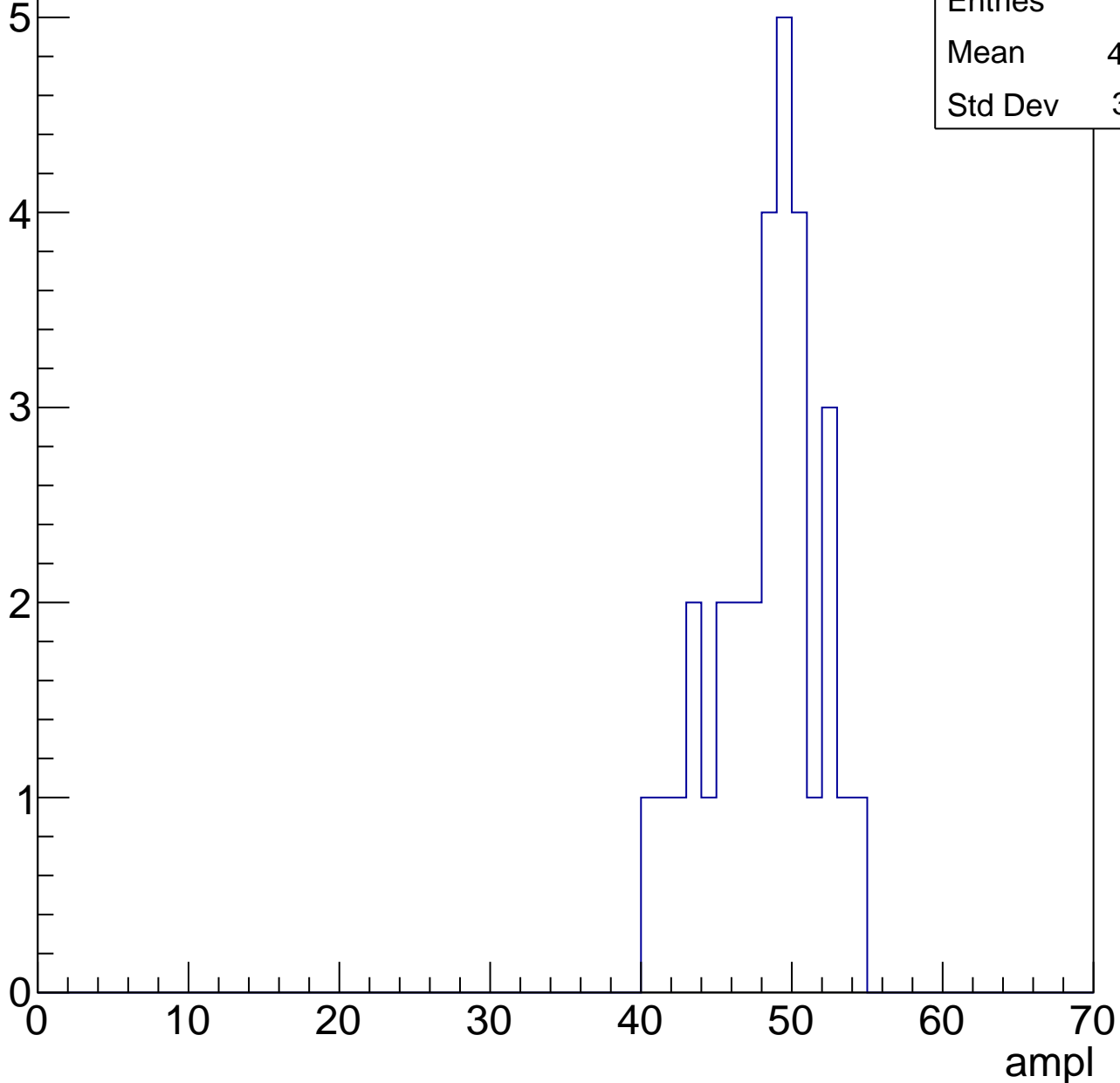


B1L103S, U14-ch48, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

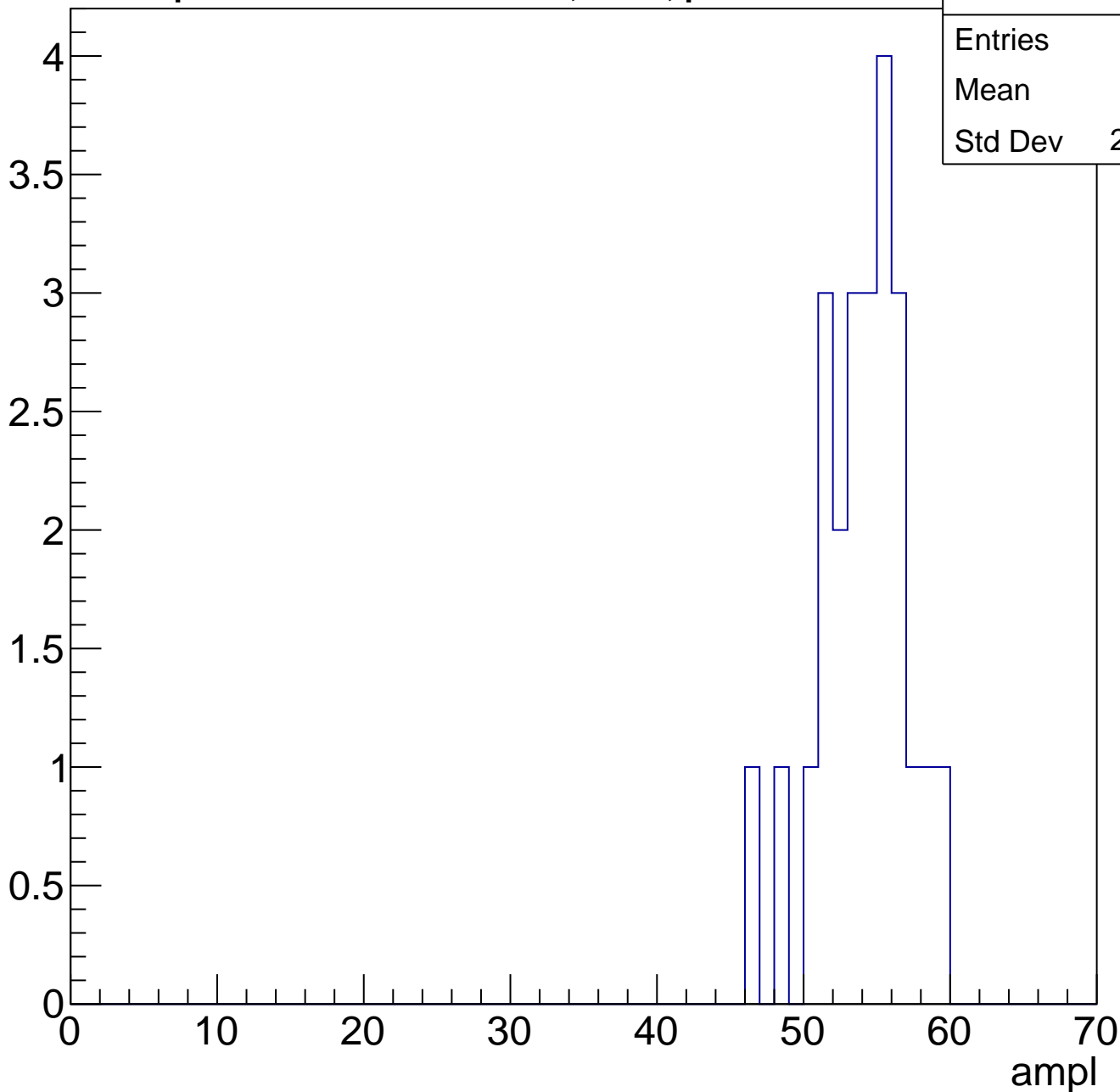
Entries	31
Mean	47.74
Std Dev	3.501



B1L103S, U14-ch48, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

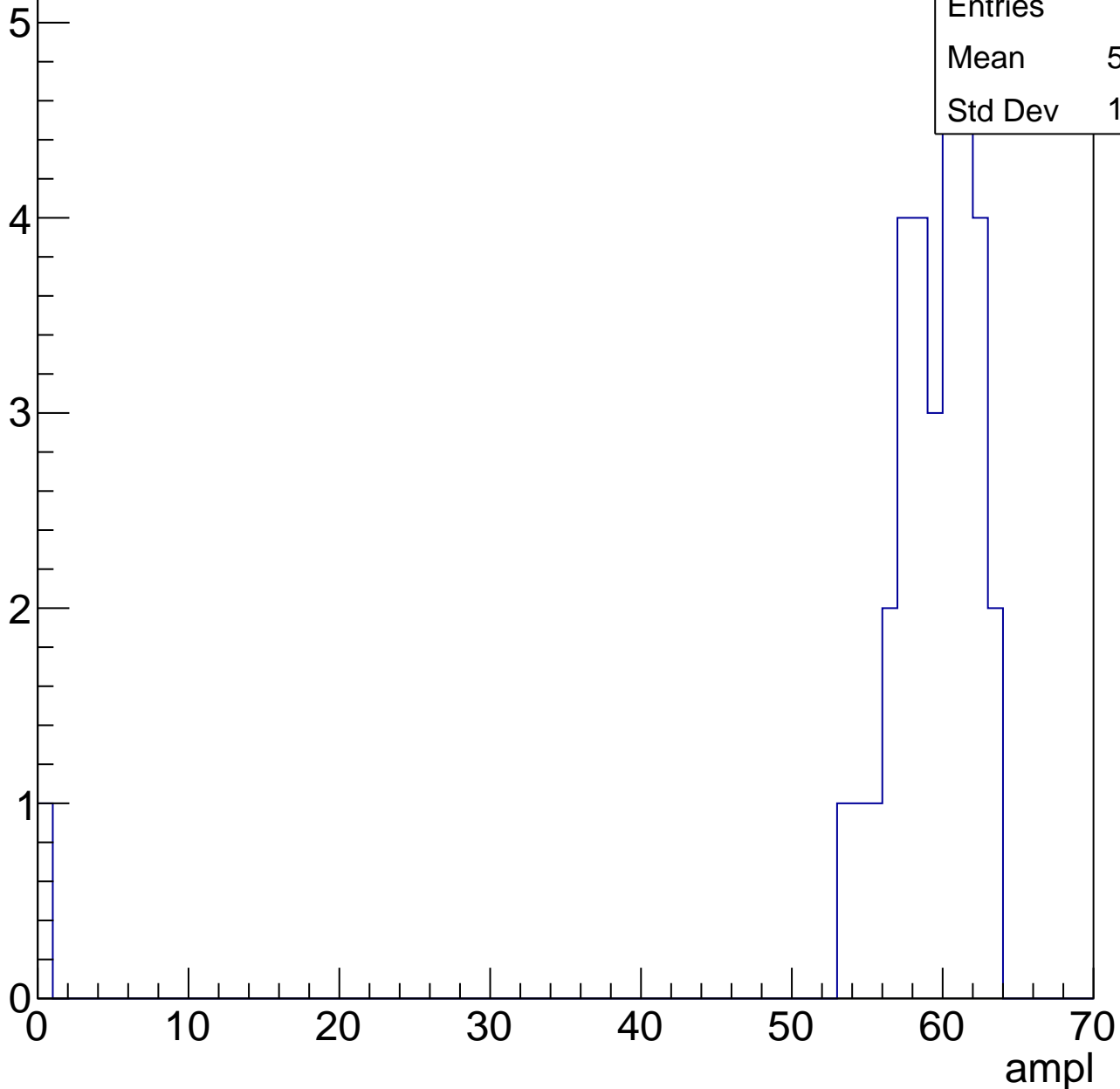


B1L103S, U14-ch48, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	33
Mean	57.27
Std Dev	10.43



B1L103S, U14-ch48, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

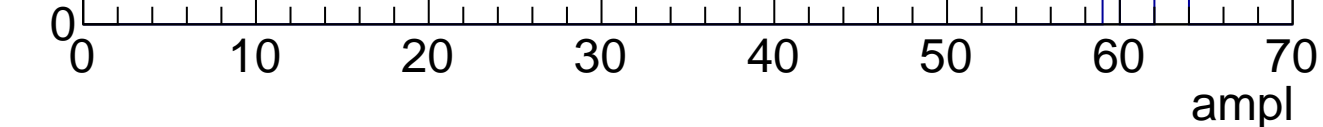
5

Mean

62

Std Dev

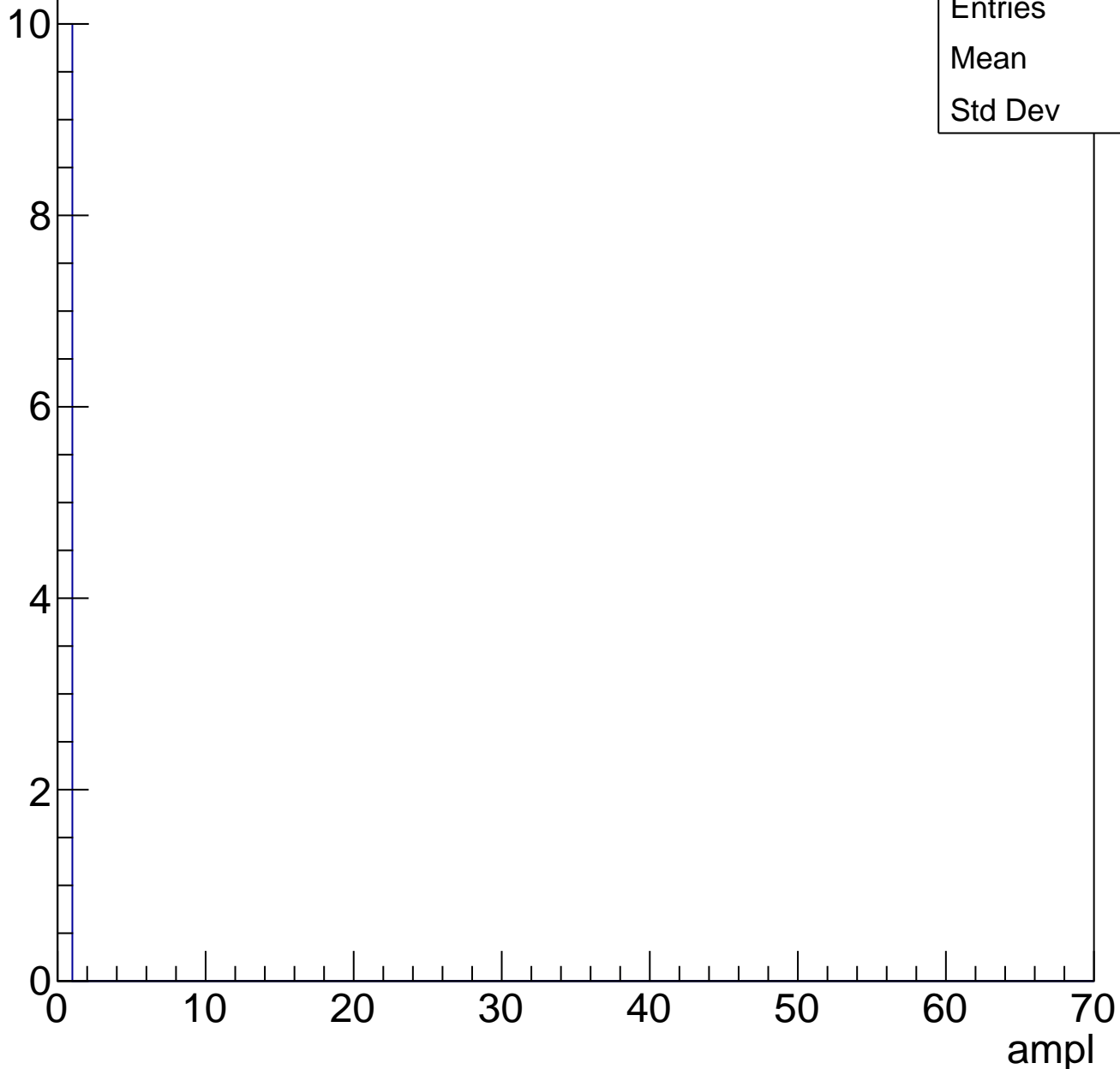
1.549



B1L103S, U14-ch48, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



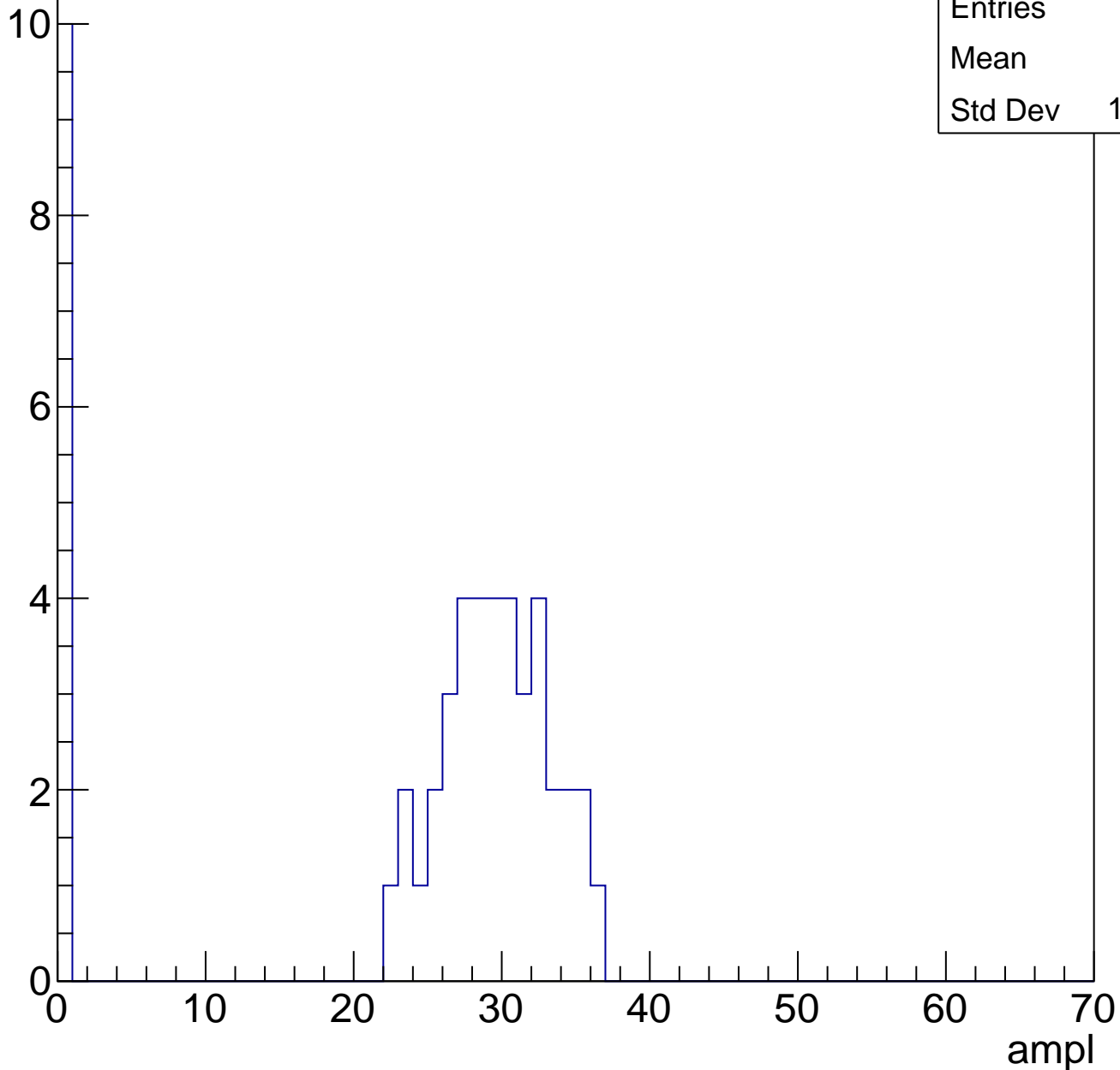
Entries	10
Mean	0
Std Dev	0

B1L103S, U14-ch49, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	49
Mean	23.2
Std Dev	12.16

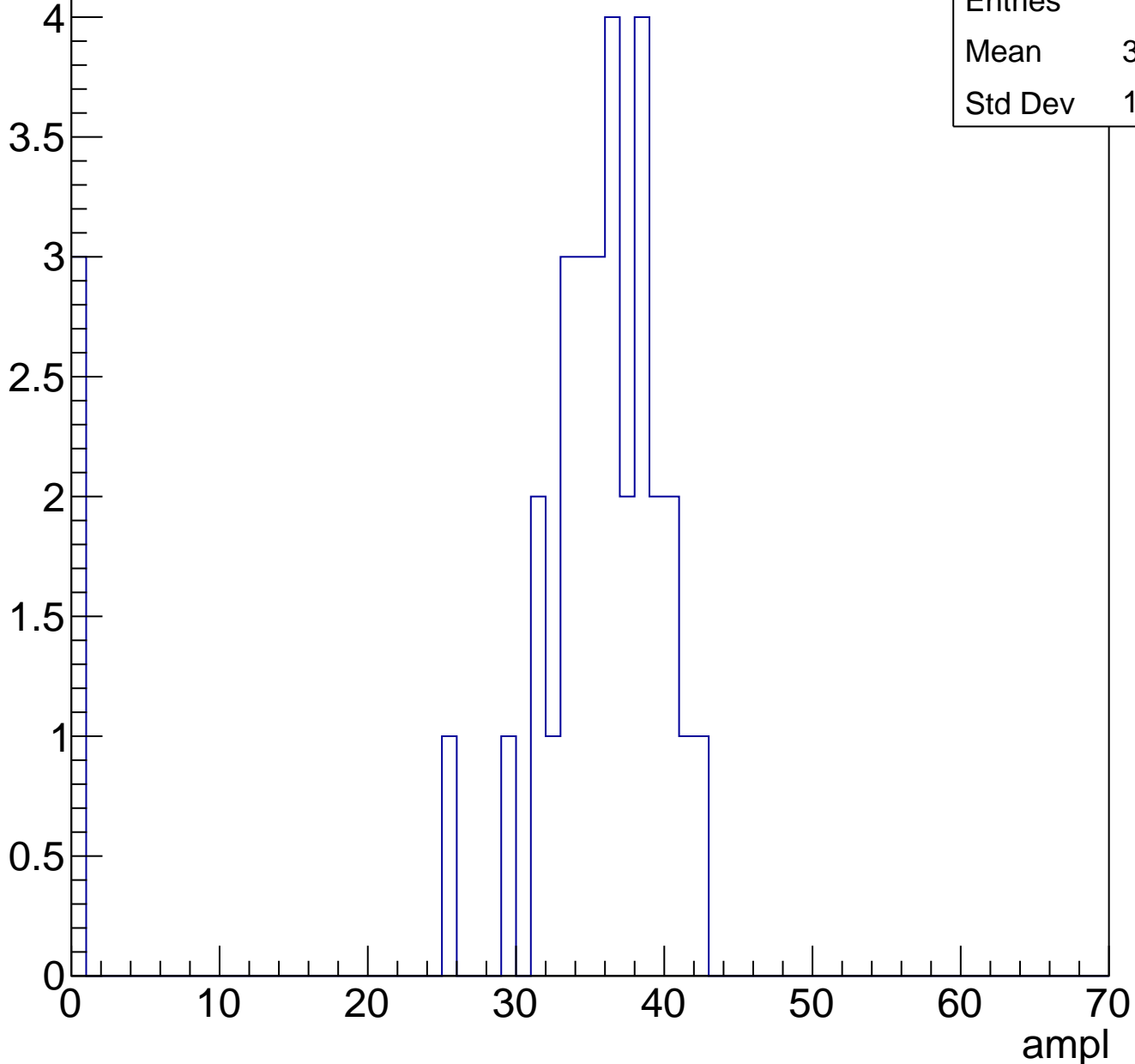
Entry



B1L103S, U14-ch49, adc1

calib_packv5_041523_1651.root, FC#0, port C2

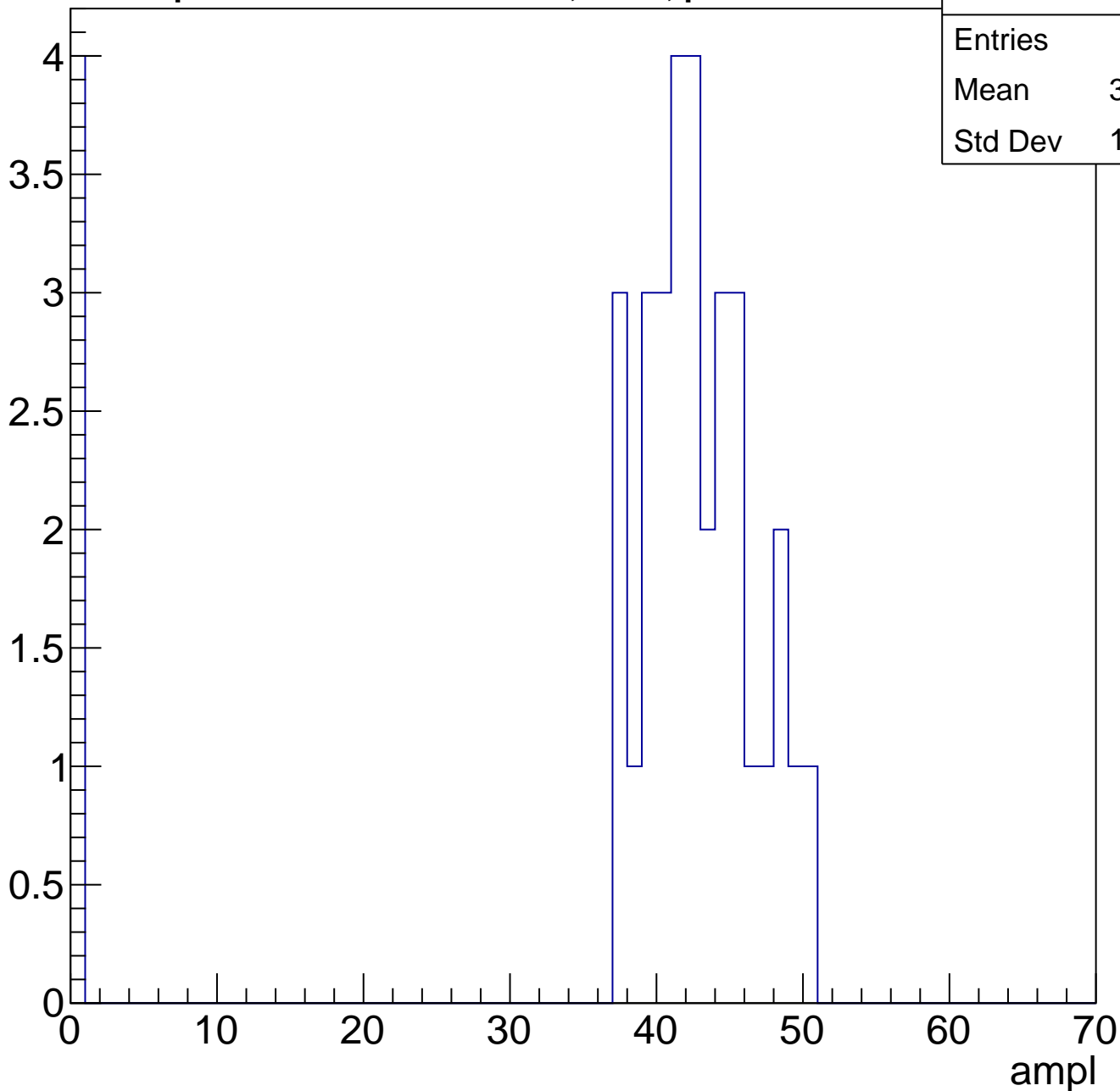
Entry



B1L103S, U14-ch49, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

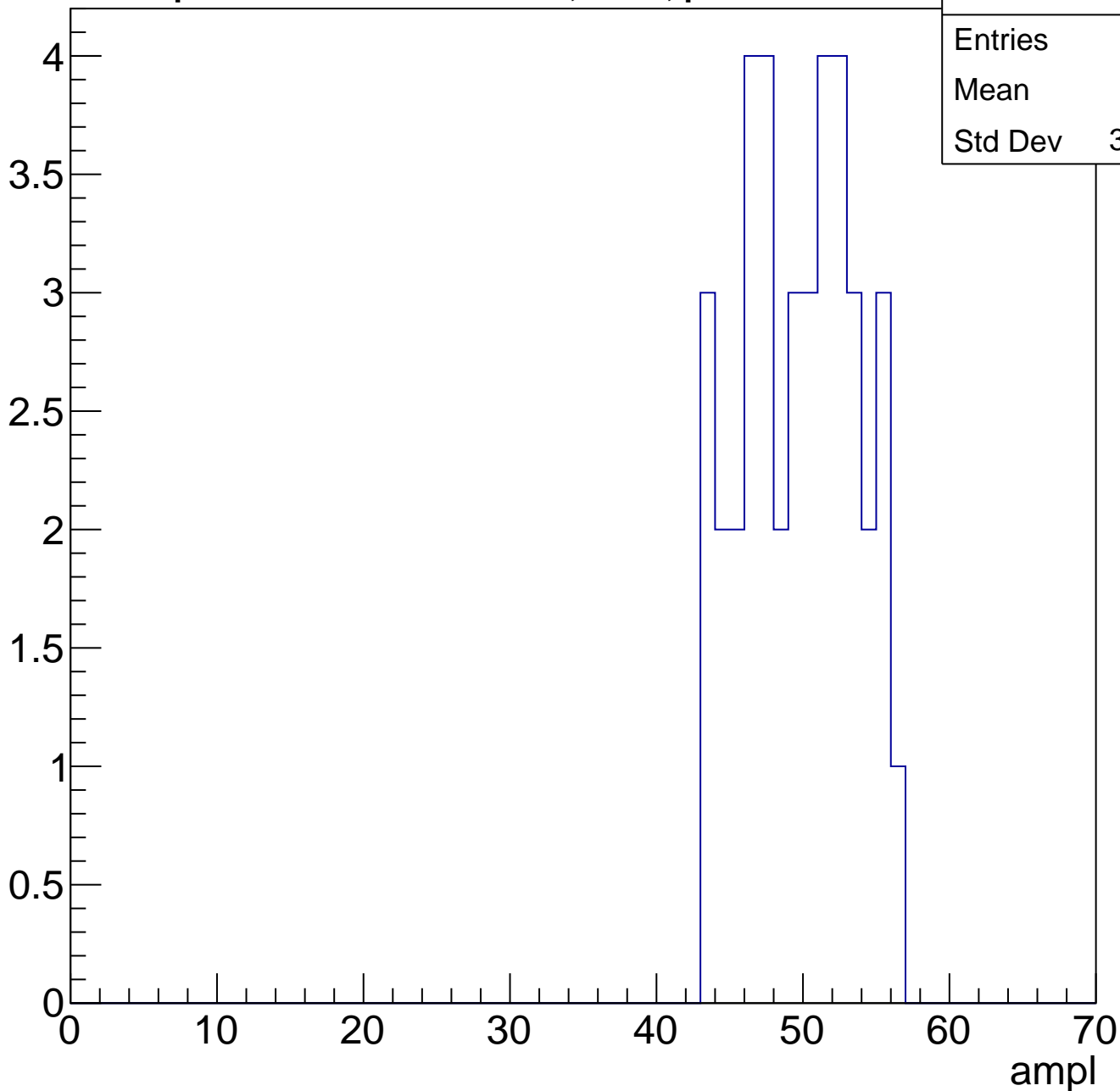


Entries	36
Mean	37.75
Std Dev	13.75

B1L103S, U14-ch49, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	40
Mean	49.3
Std Dev	3.709

B1L103S, U14-ch49, adc4

calib_packv5_041523_1651.root, FC#0, port C2

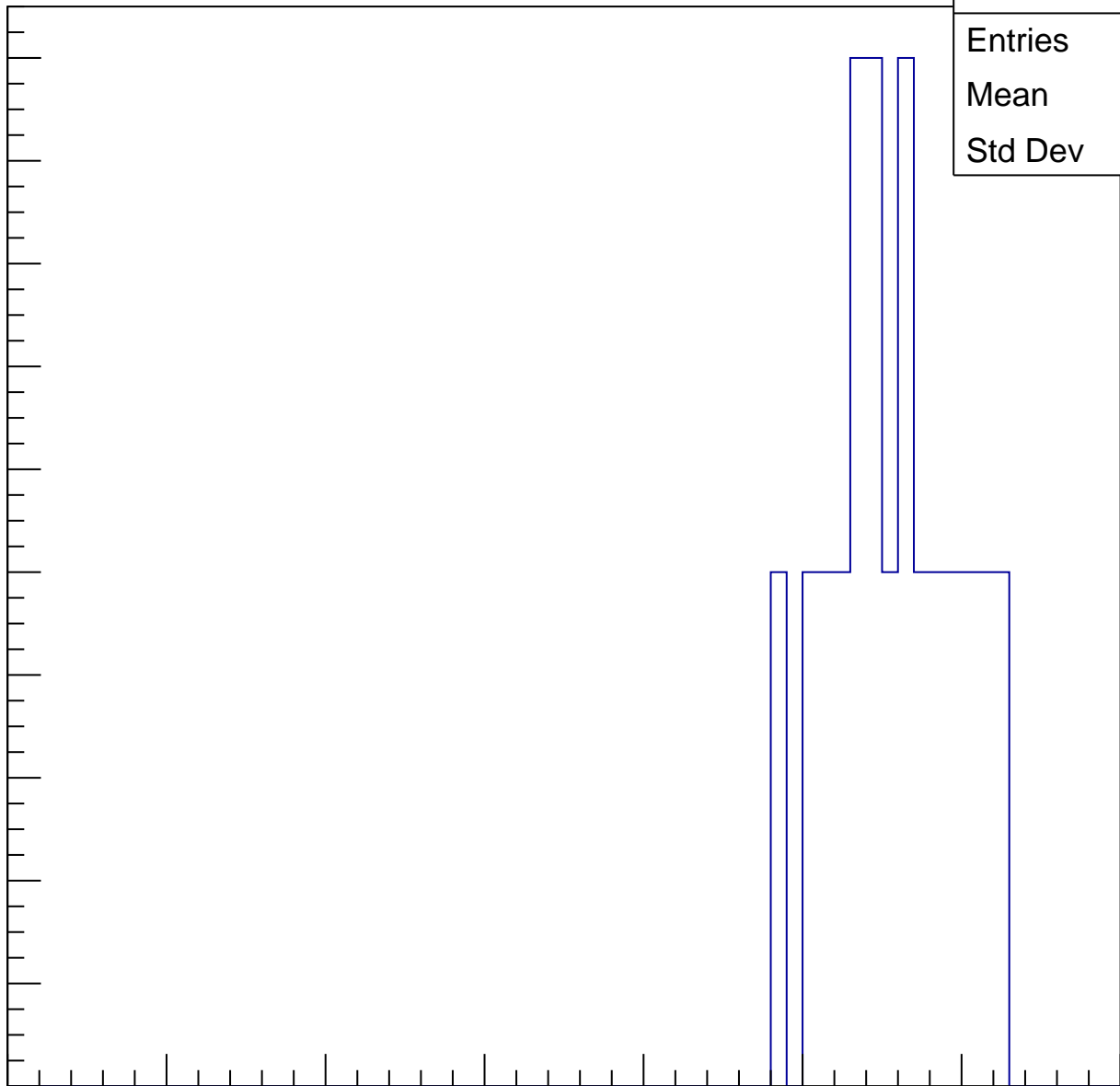
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	17
Mean	55.24
Std Dev	3.828

ampl

0 10 20 30 40 50 60 70

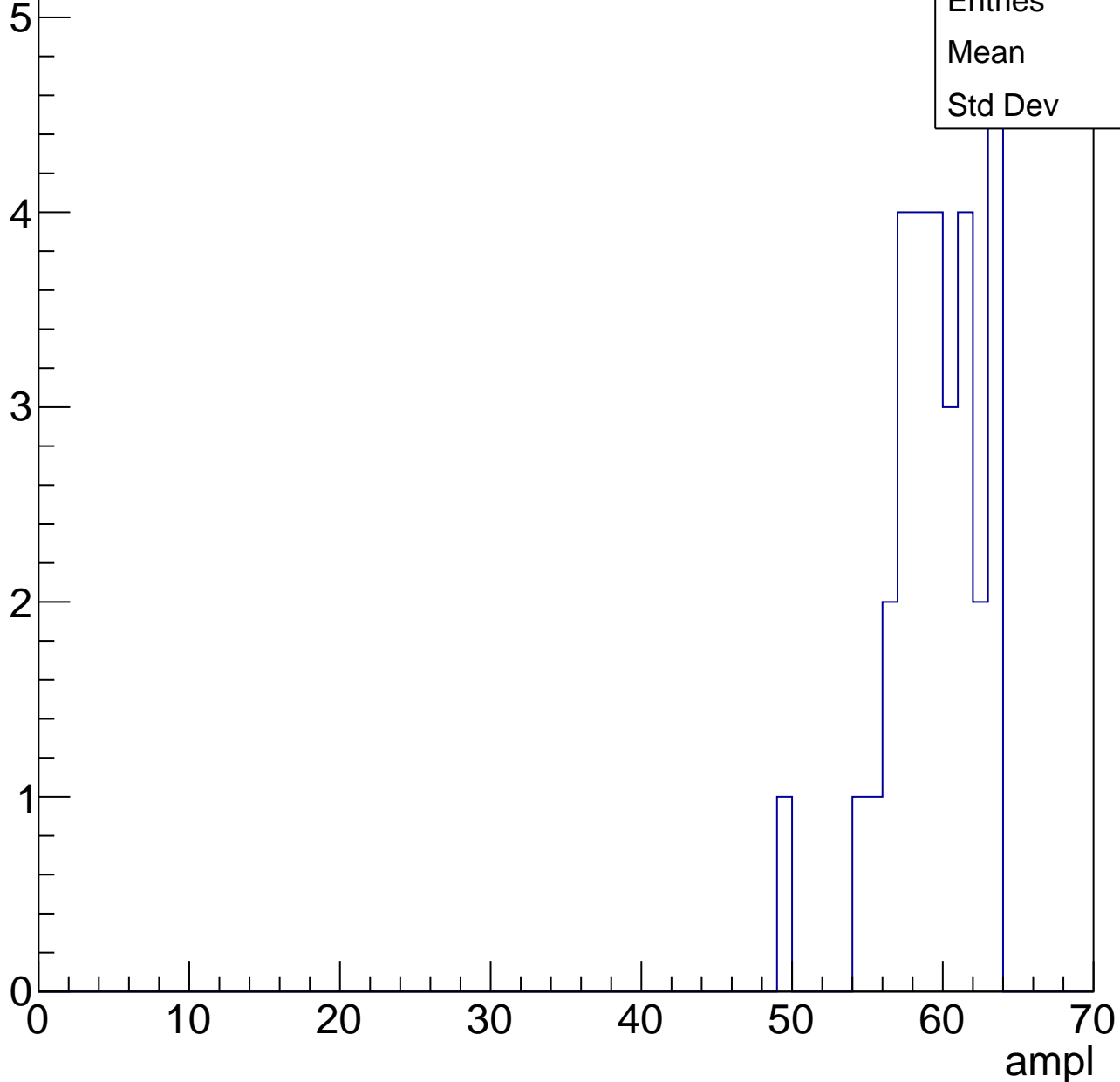


B1L103S, U14-ch49, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

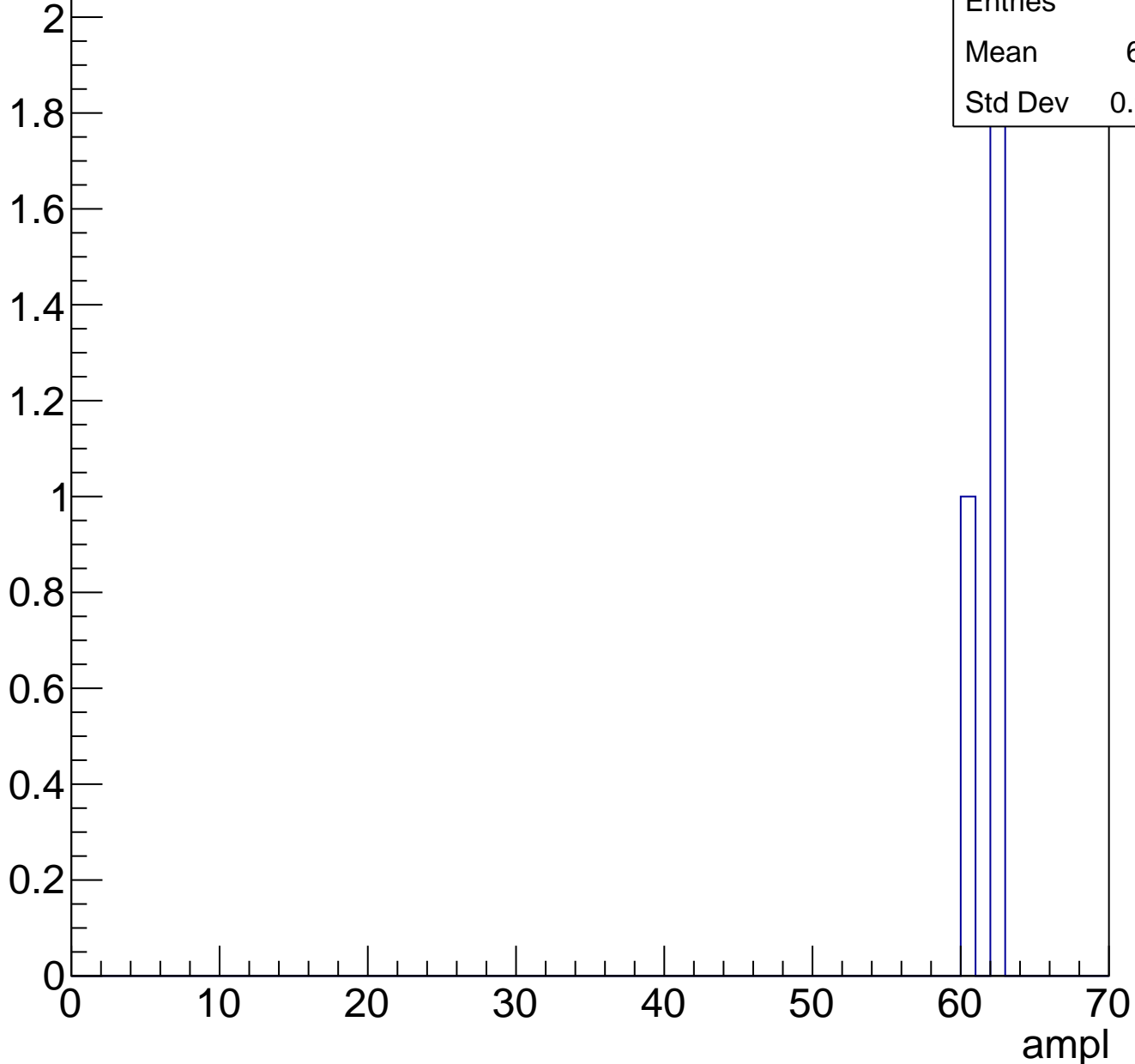
Entries	31
Mean	59
Std Dev	3.09



B1L103S, U14-ch49, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	3
Mean	61.33
Std Dev	0.9428

B1L103S, U14-ch49, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



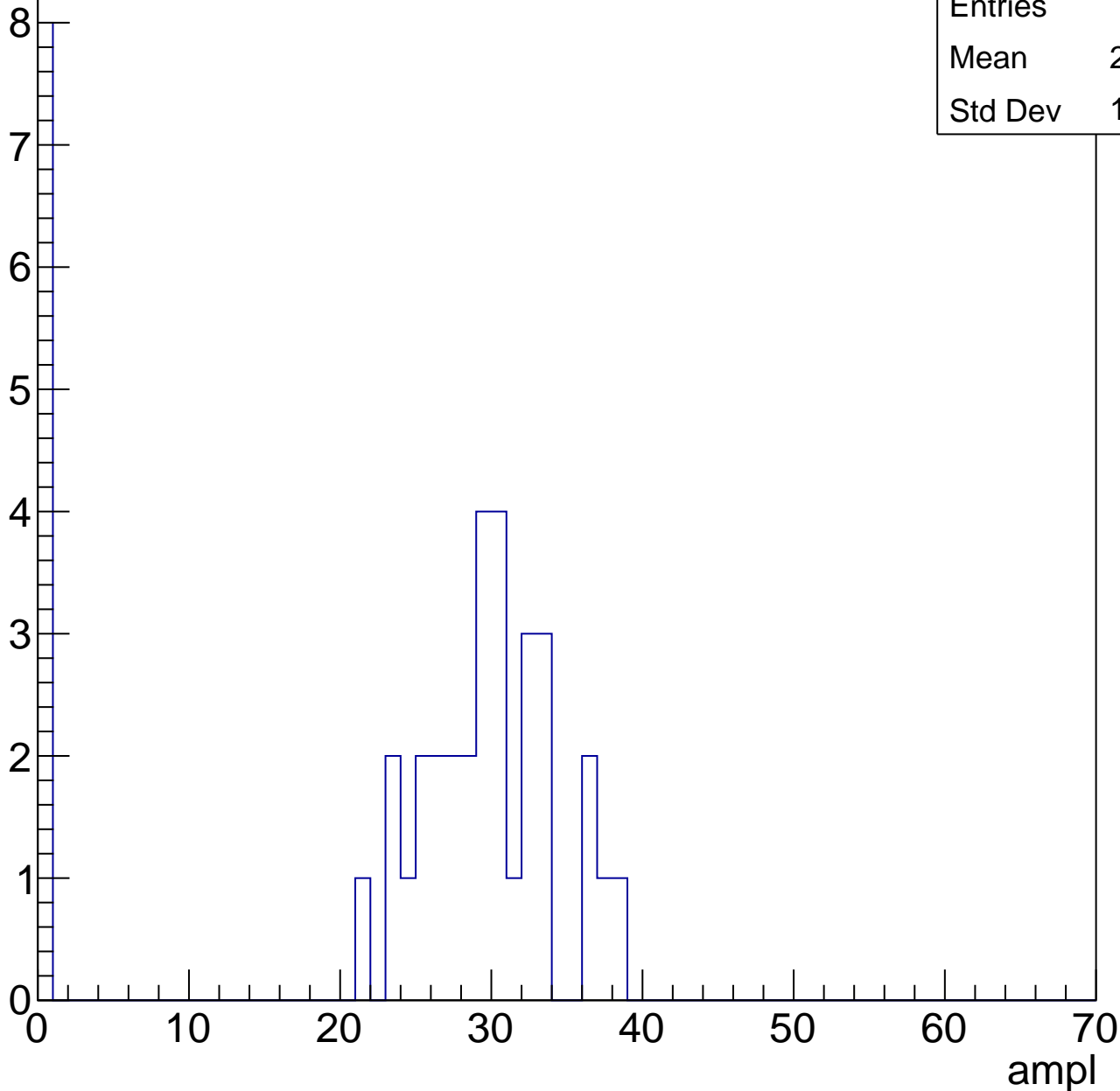
Entries	10
Mean	0
Std Dev	0

B1L103S, U14-ch50, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	23.38
Std Dev	12.45

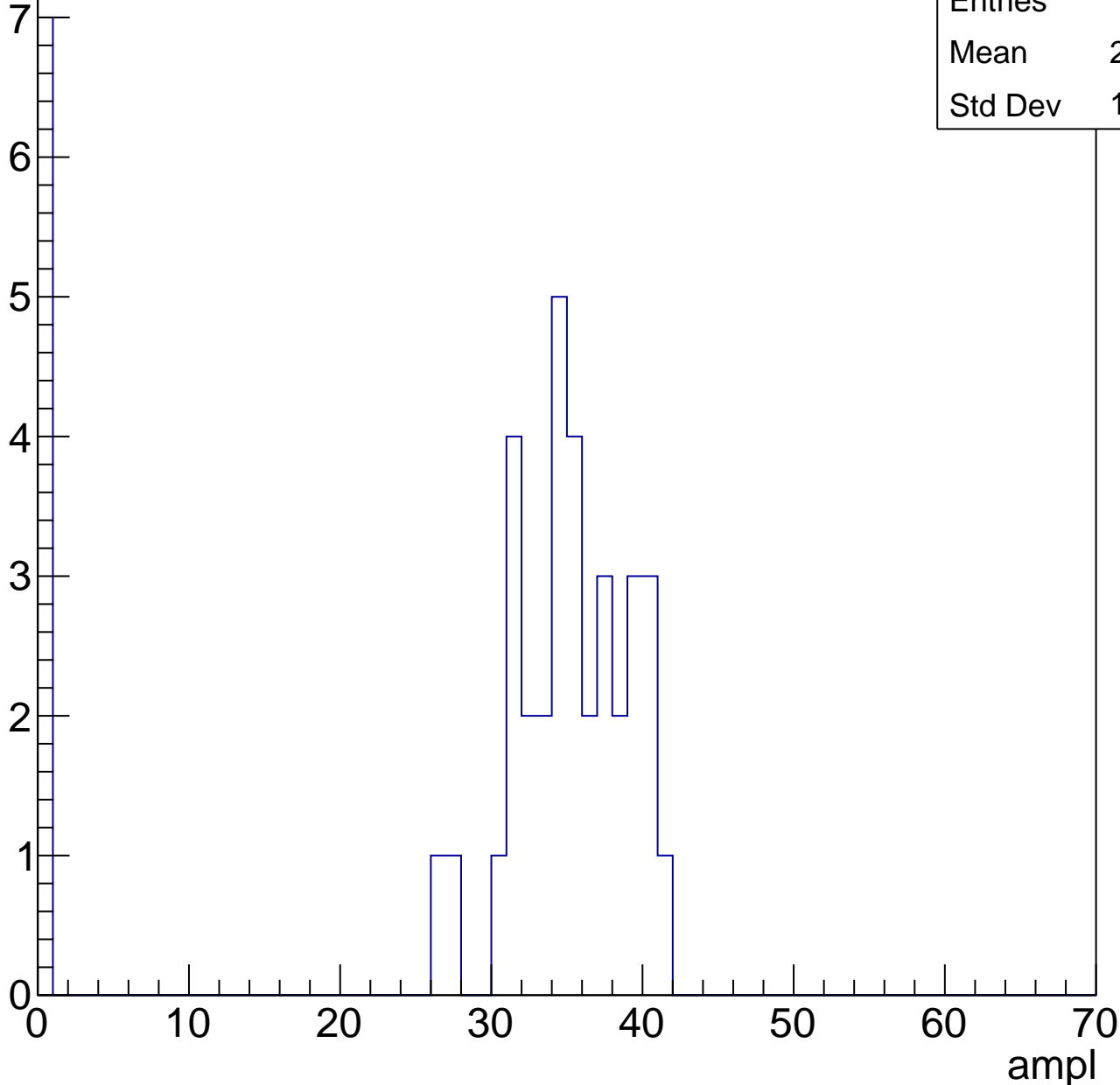


B1L103S, U14-ch50, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	41
Mean	28.88
Std Dev	13.52

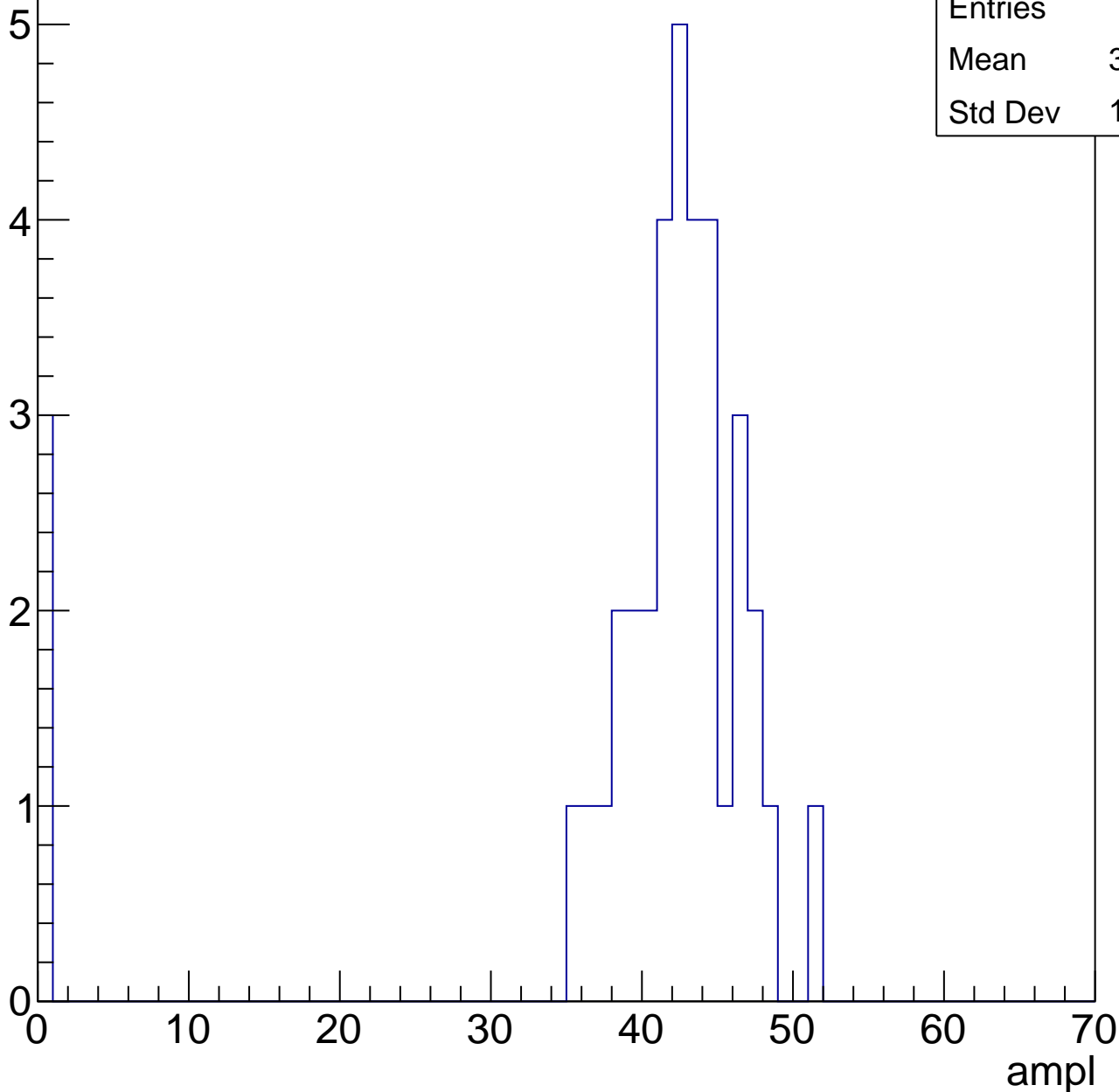


B1L103S, U14-ch50, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	37
Mean	38.92
Std Dev	12.03

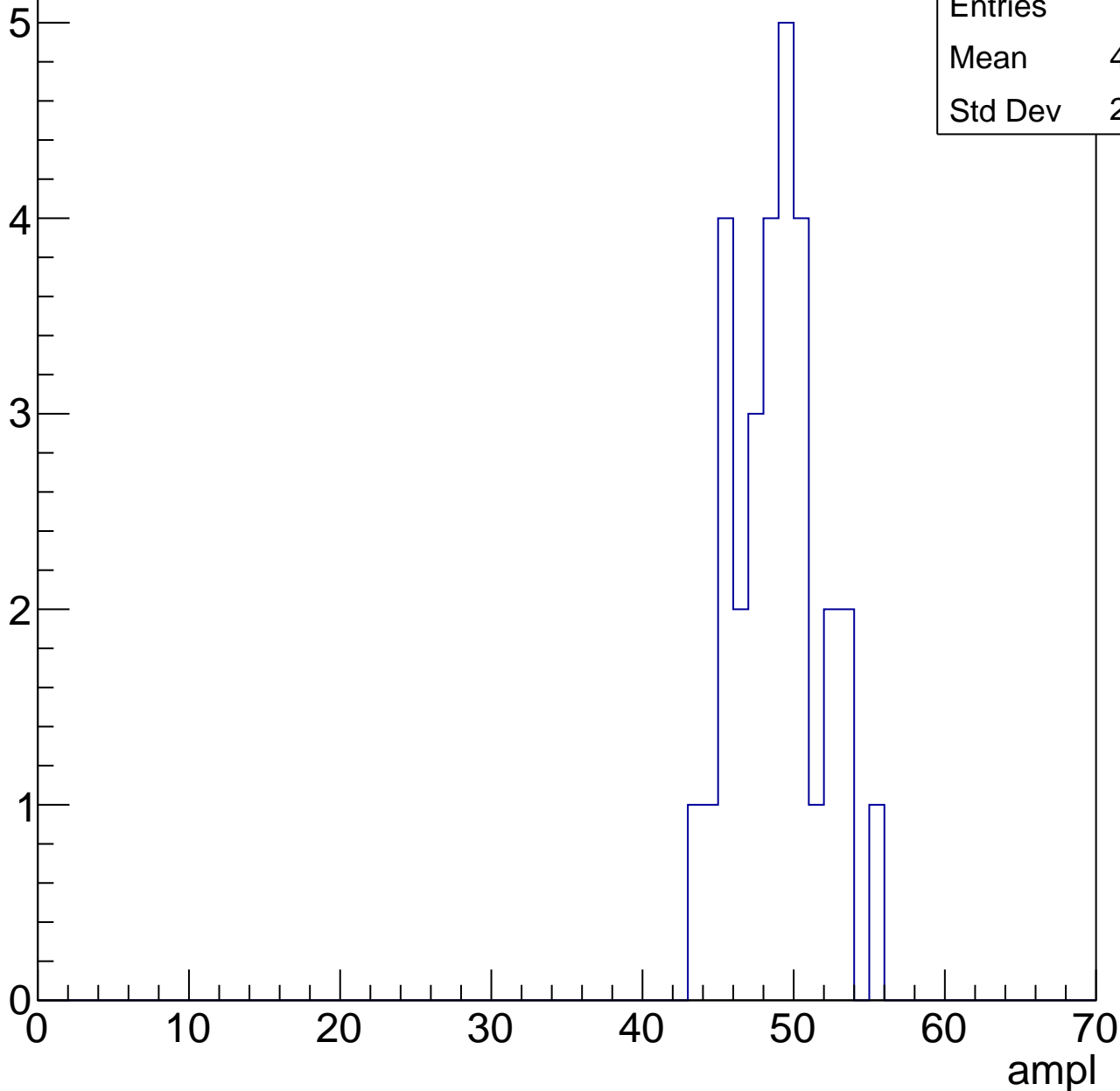


B1L103S, U14-ch50, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

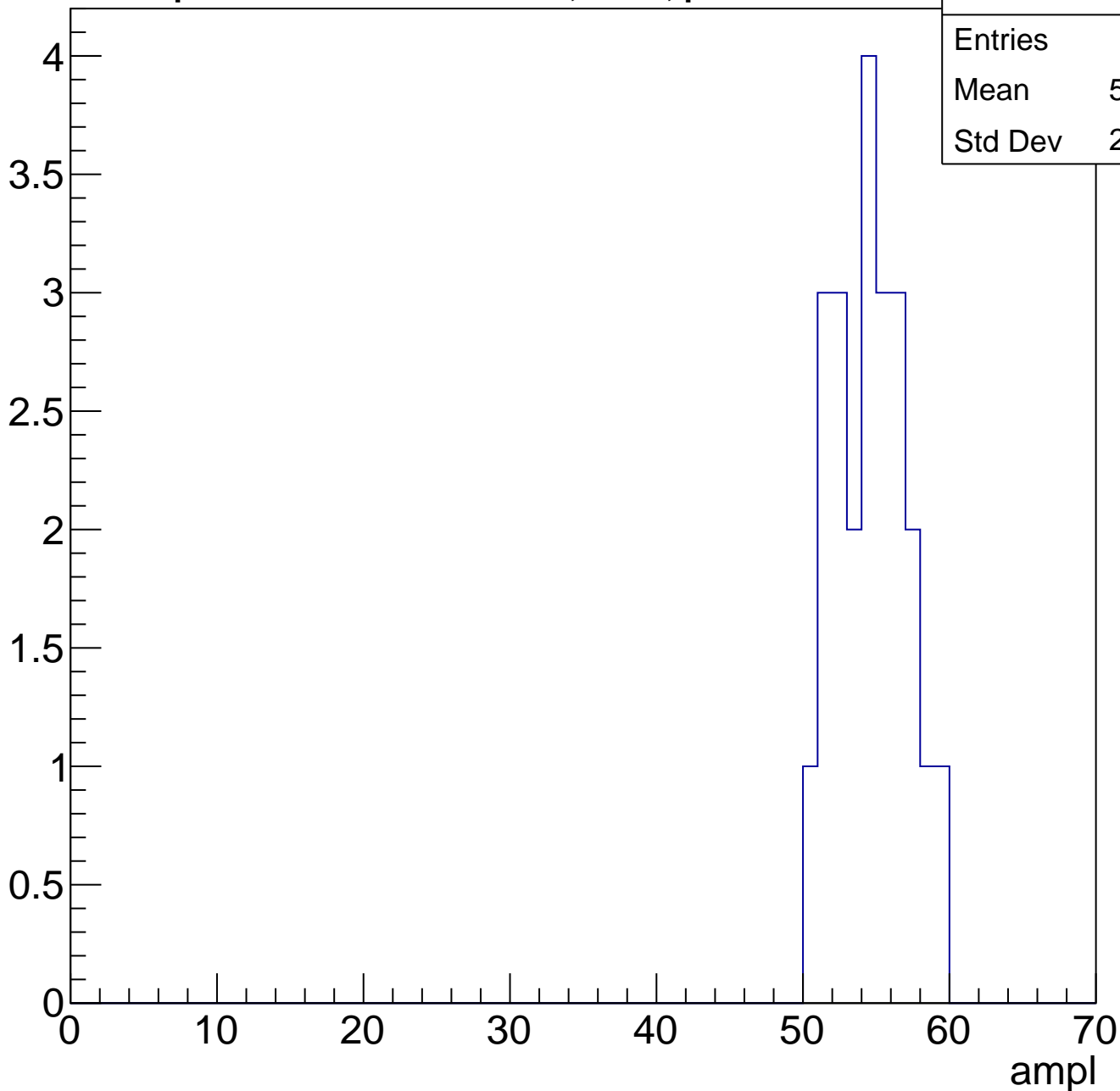
Entries	30
Mean	48.43
Std Dev	2.848



B1L103S, U14-ch50, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



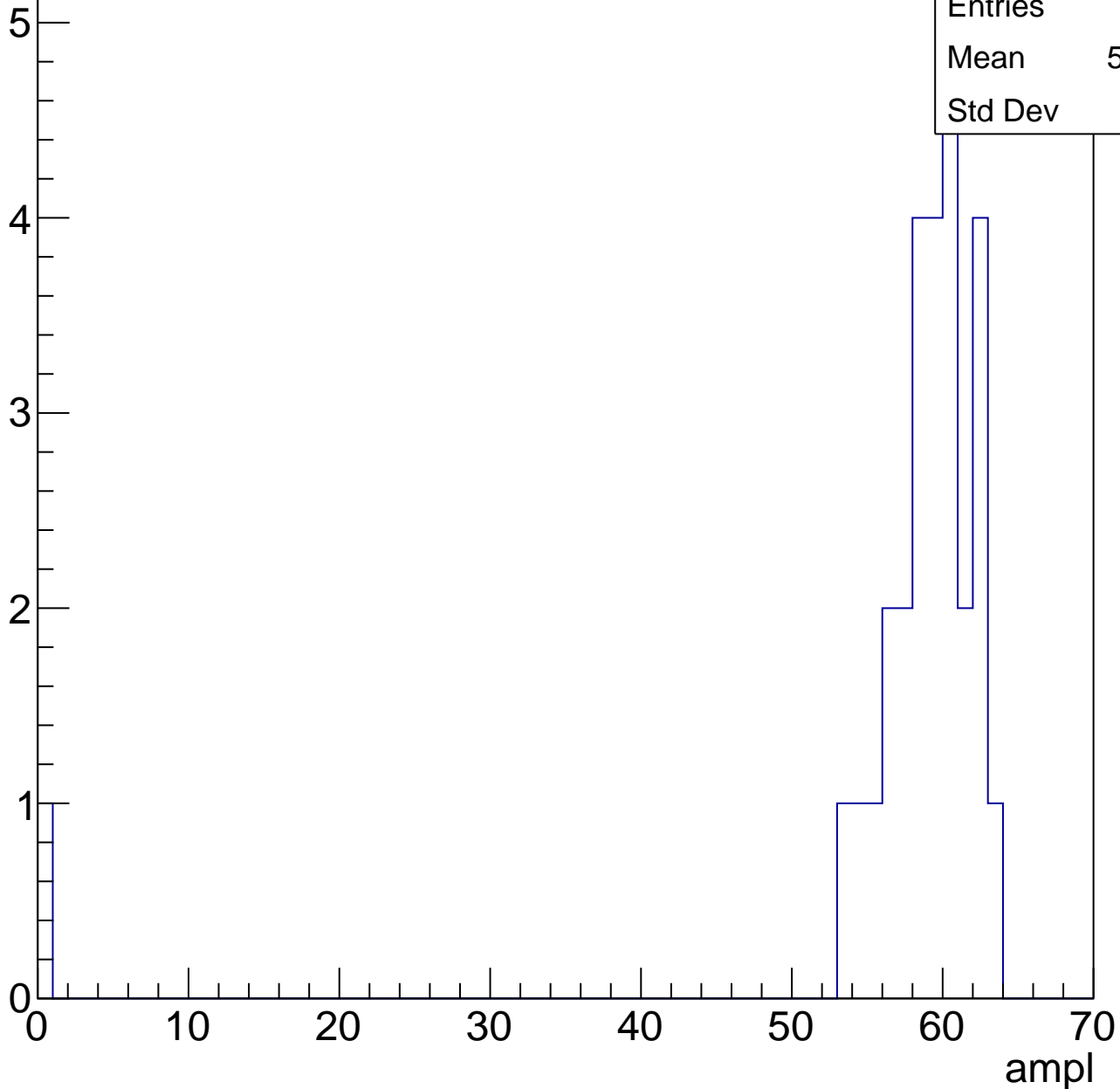
Entries	23
Mean	54.13
Std Dev	2.383

B1L103S, U14-ch50, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

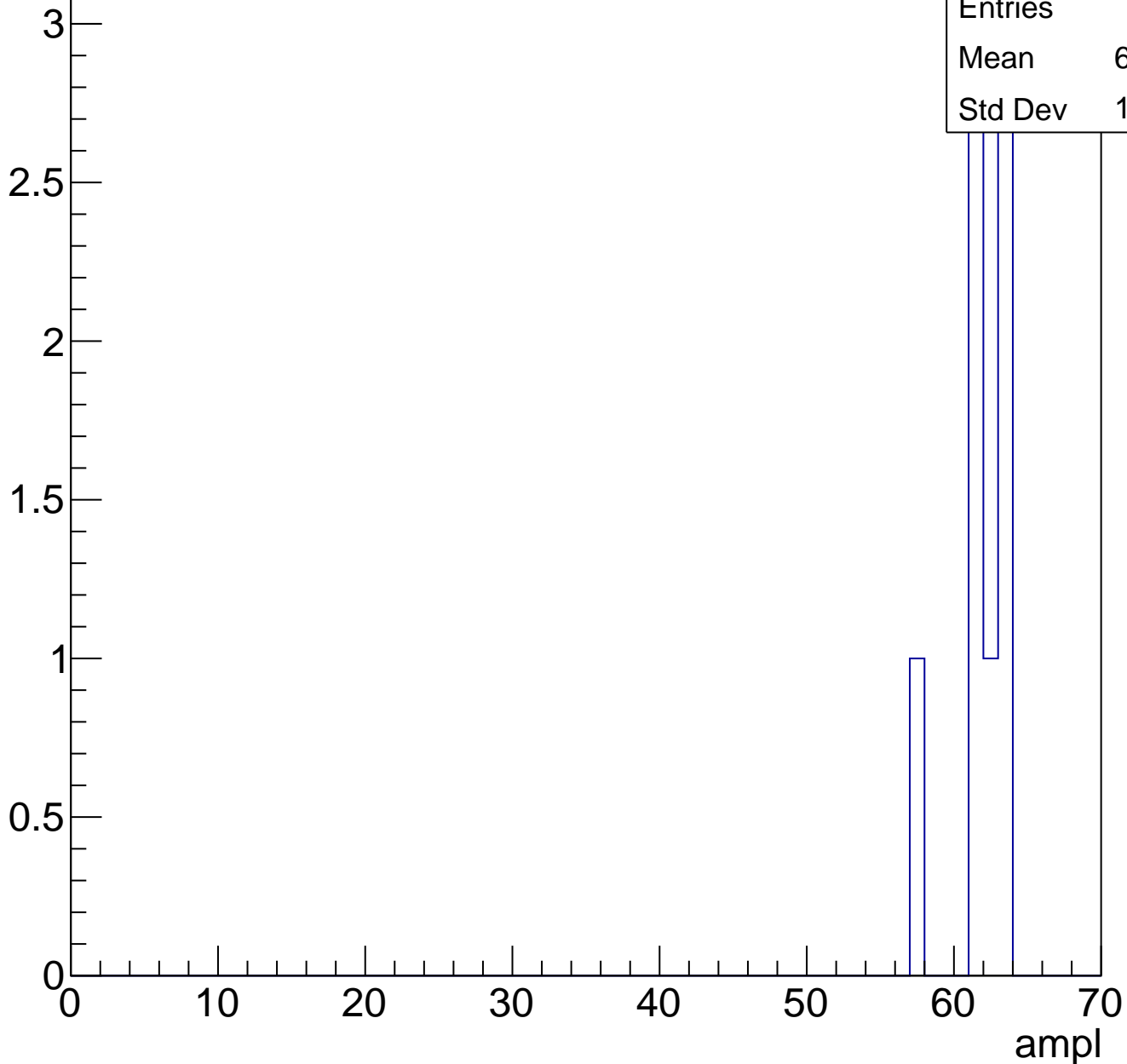
Entries	28
Mean	56.75
Std Dev	11.2



B1L103S, U14-ch50, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

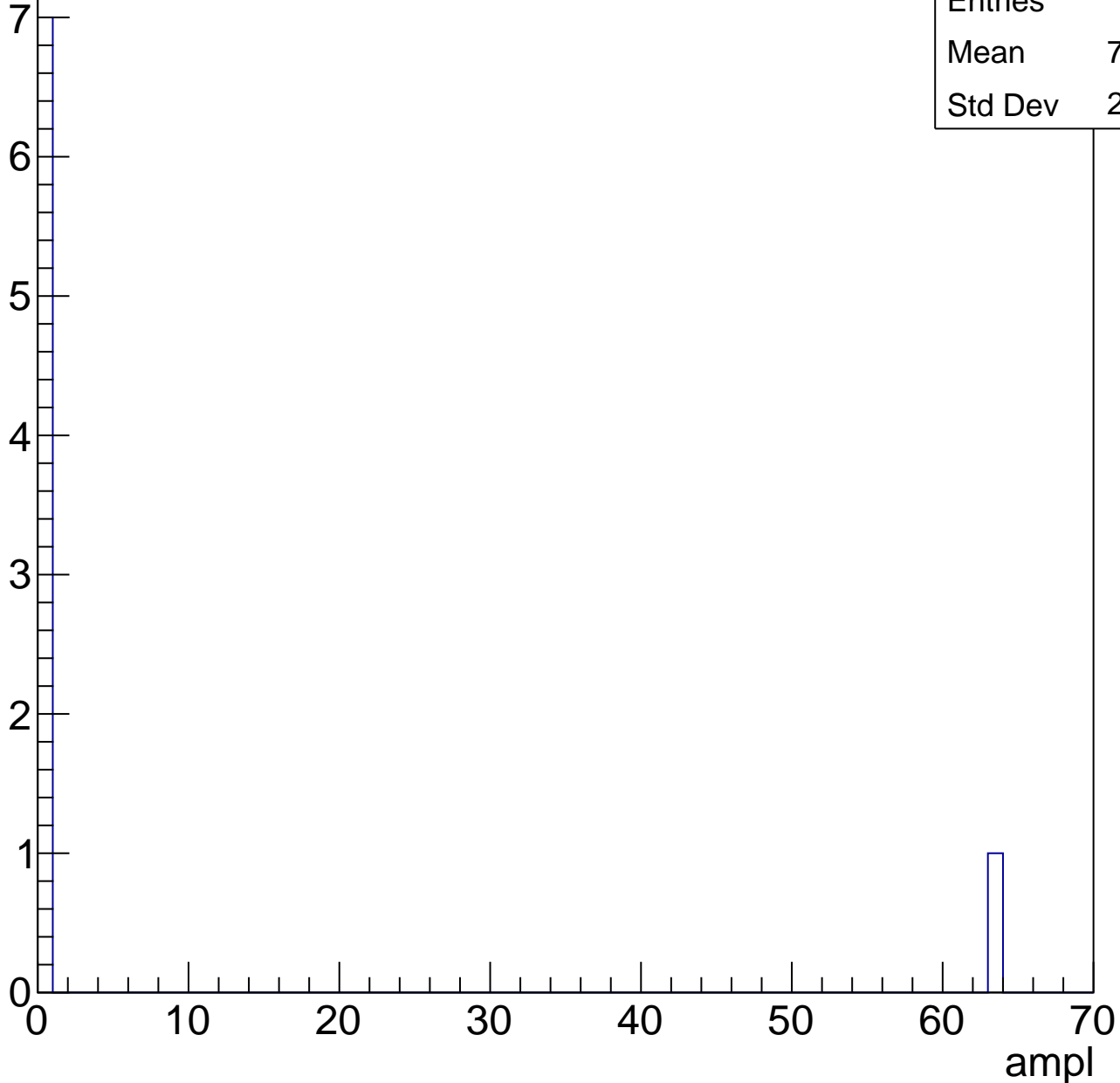


B1L103S, U14-ch50, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	8
Mean	7.875
Std Dev	20.84

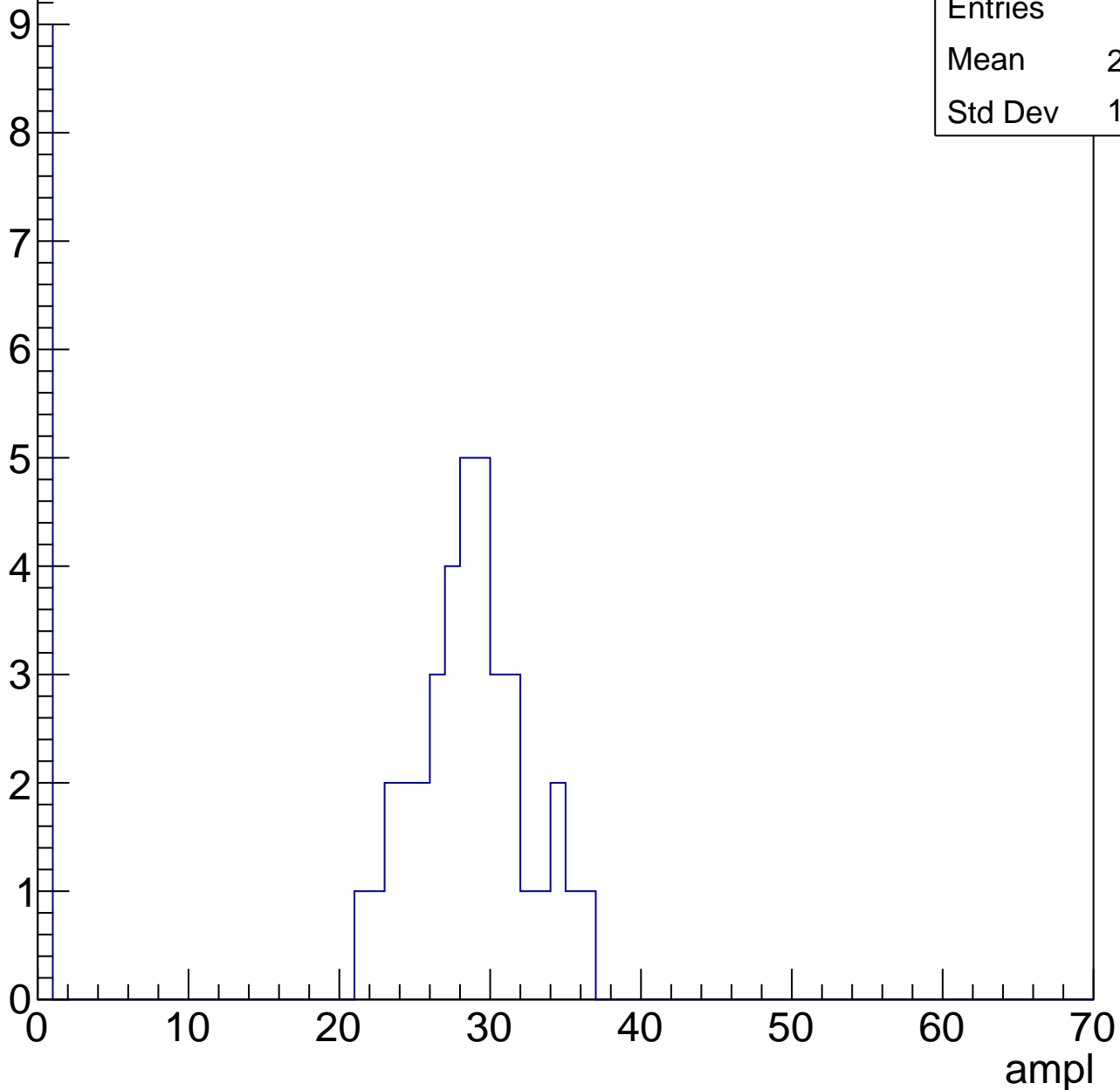


B1L103S, U14-ch51, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

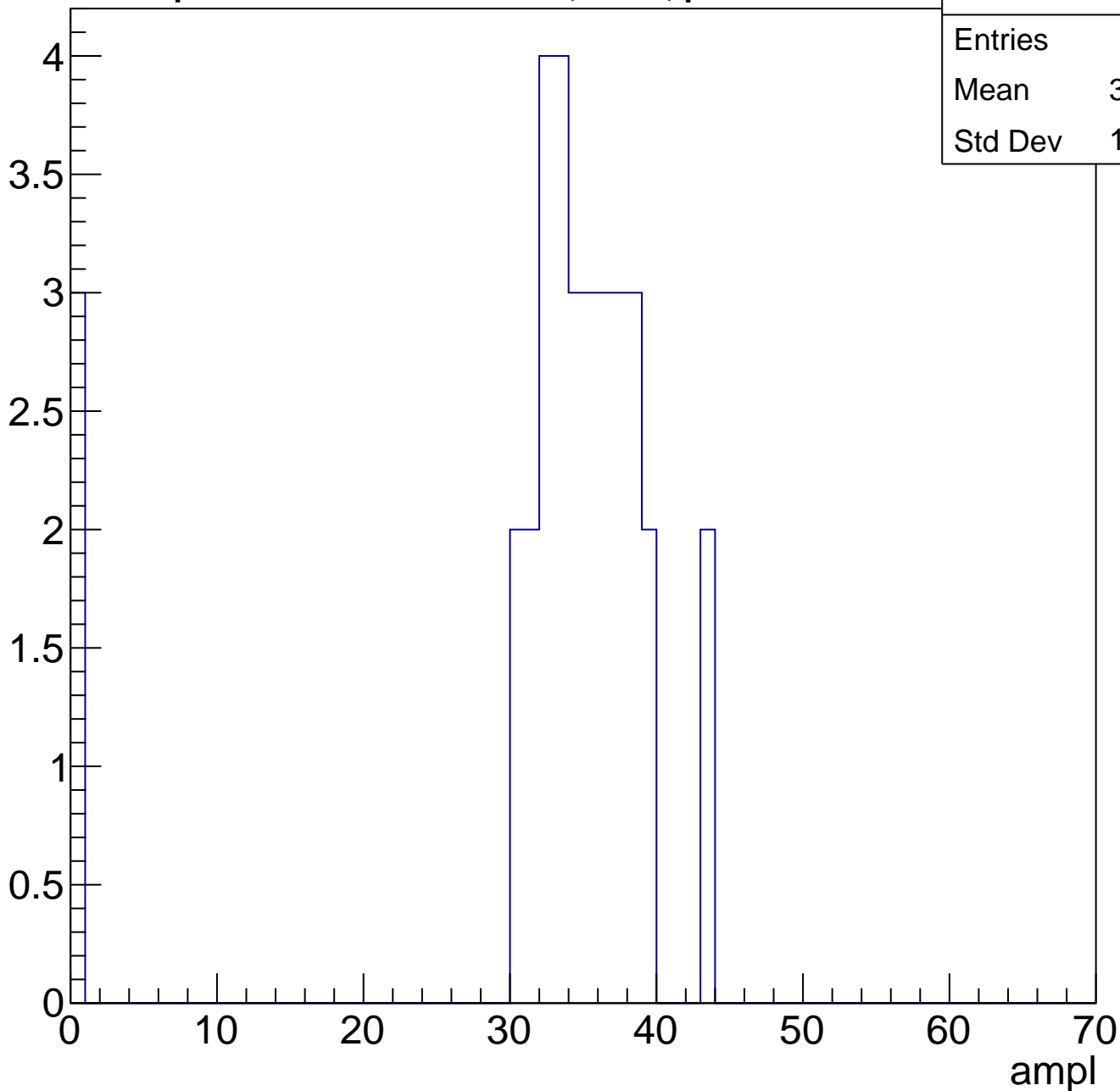
Entries	46
Mean	22.72
Std Dev	11.65



B1L103S, U14-ch51, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry



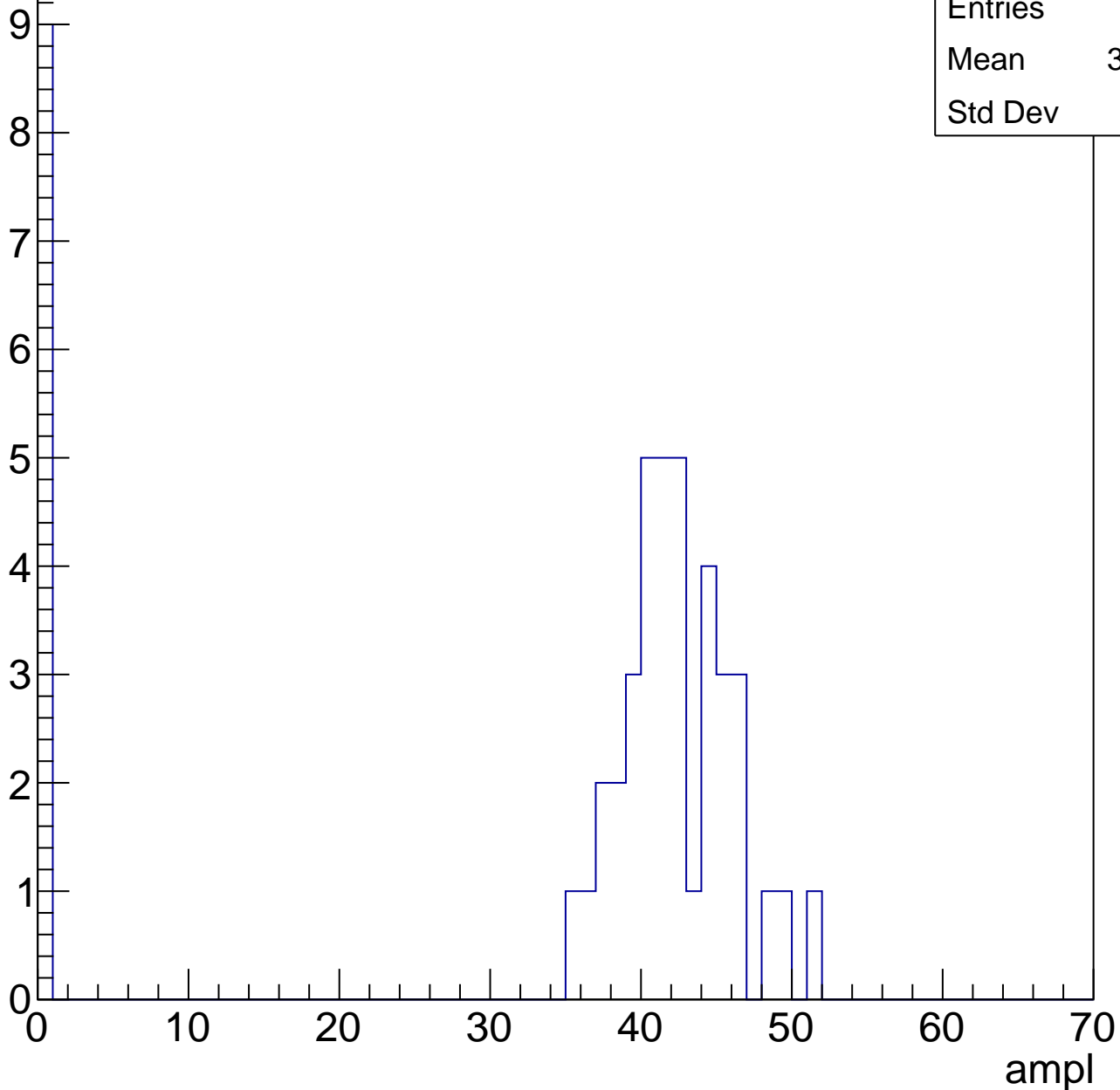
Entries	34
Mean	31.94
Std Dev	10.43

B1L103S, U14-ch51, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

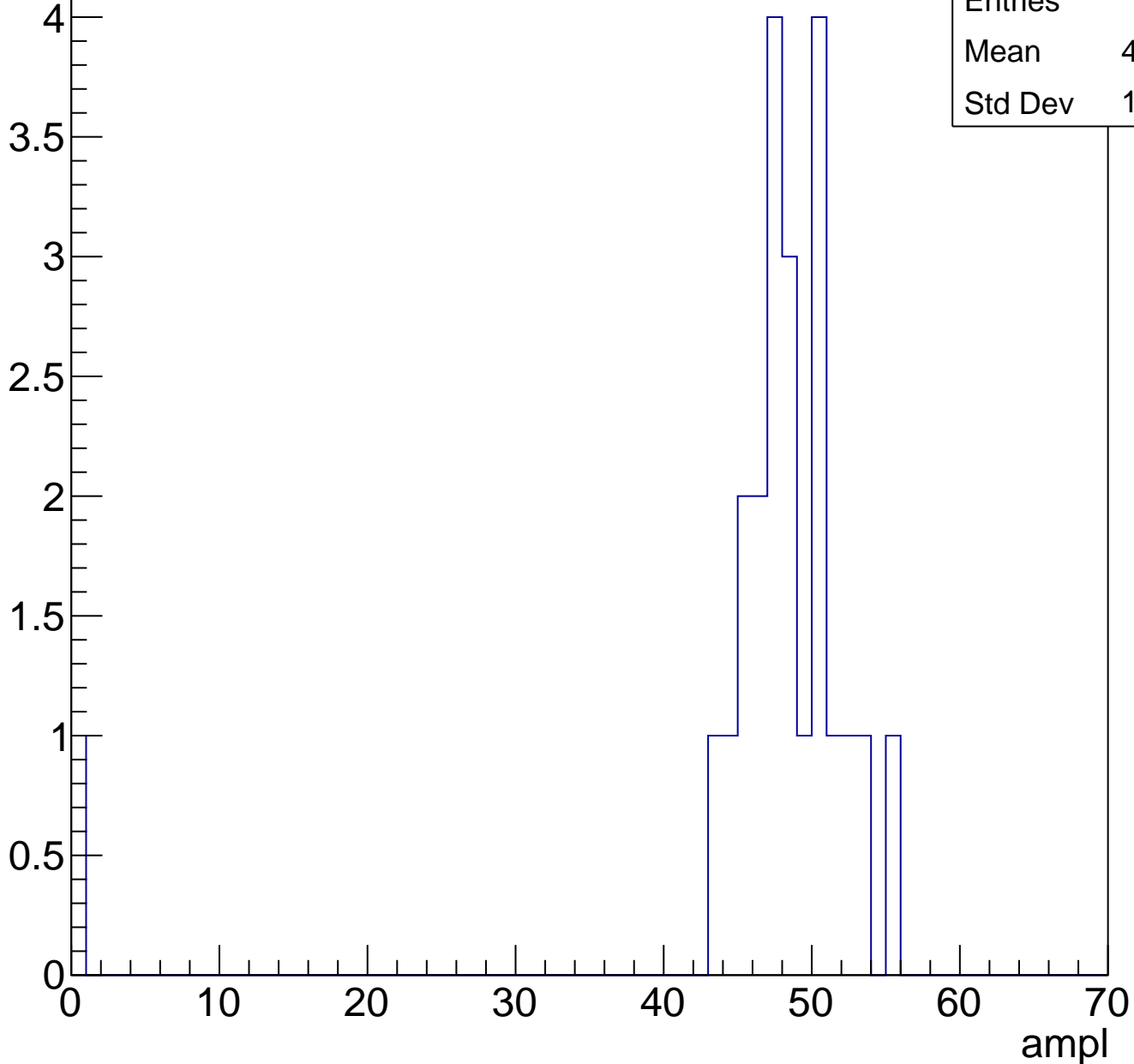
Entries	47
Mean	33.89
Std Dev	16.8



B1L103S, U14-ch51, adc3

calib_packv5_041523_1651.root, FC#0, port C2

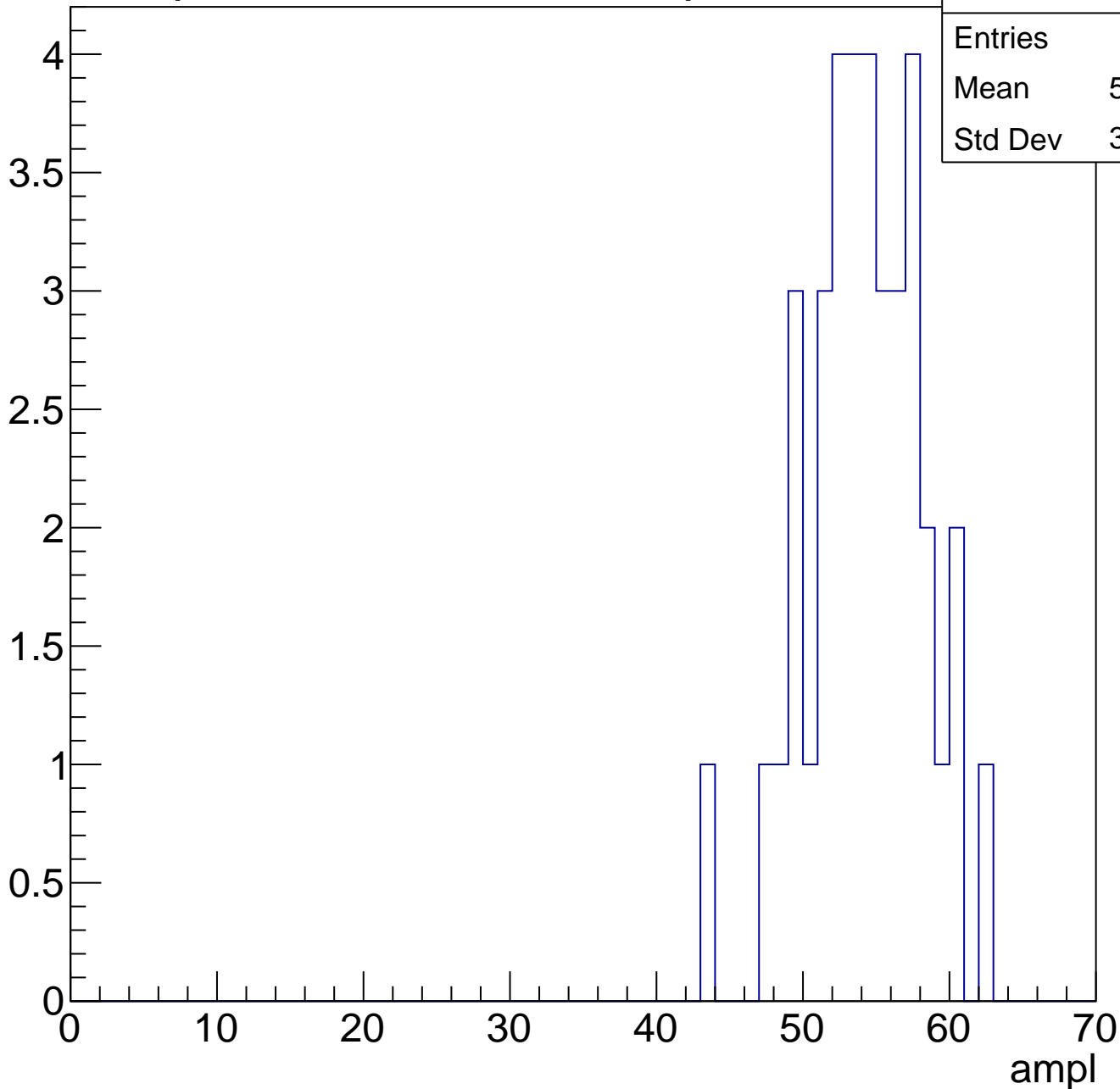
Entry



B1L103S, U14-ch51, adc4

calib_packv5_041523_1651.root, FC#0, port C2

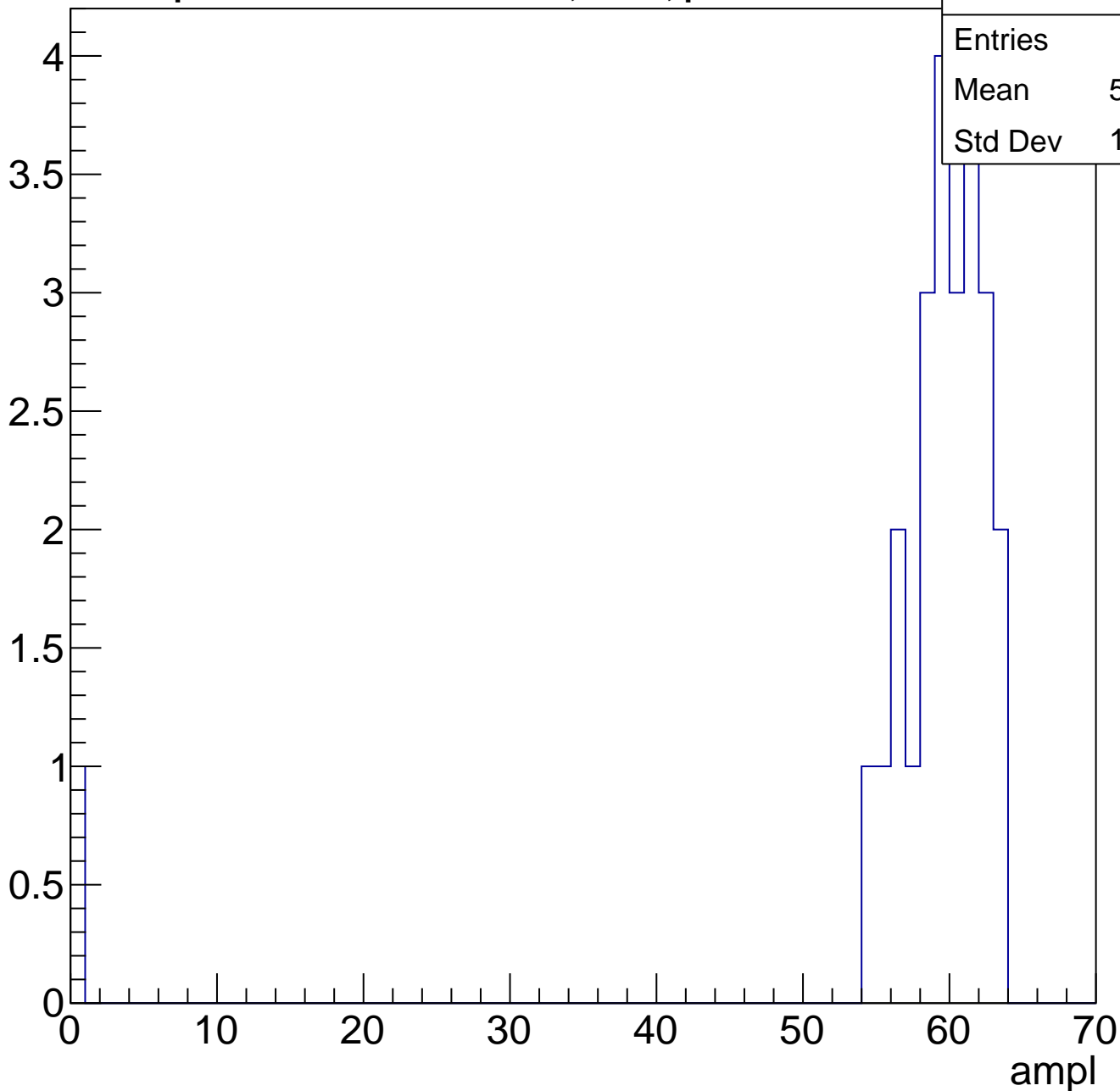
Entry



B1L103S, U14-ch51, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch51, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

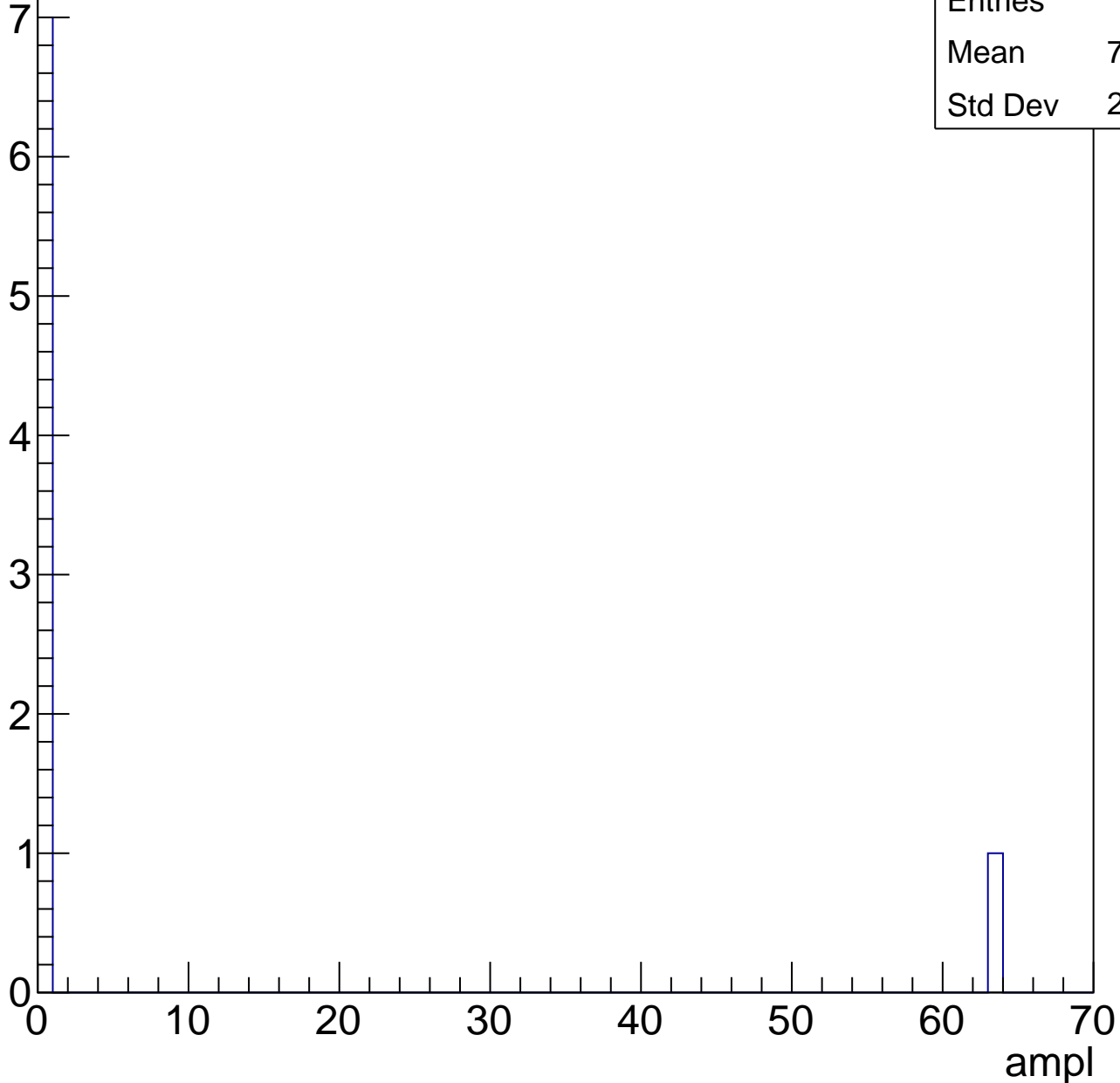


B1L103S, U14-ch51, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	8
Mean	7.875
Std Dev	20.84

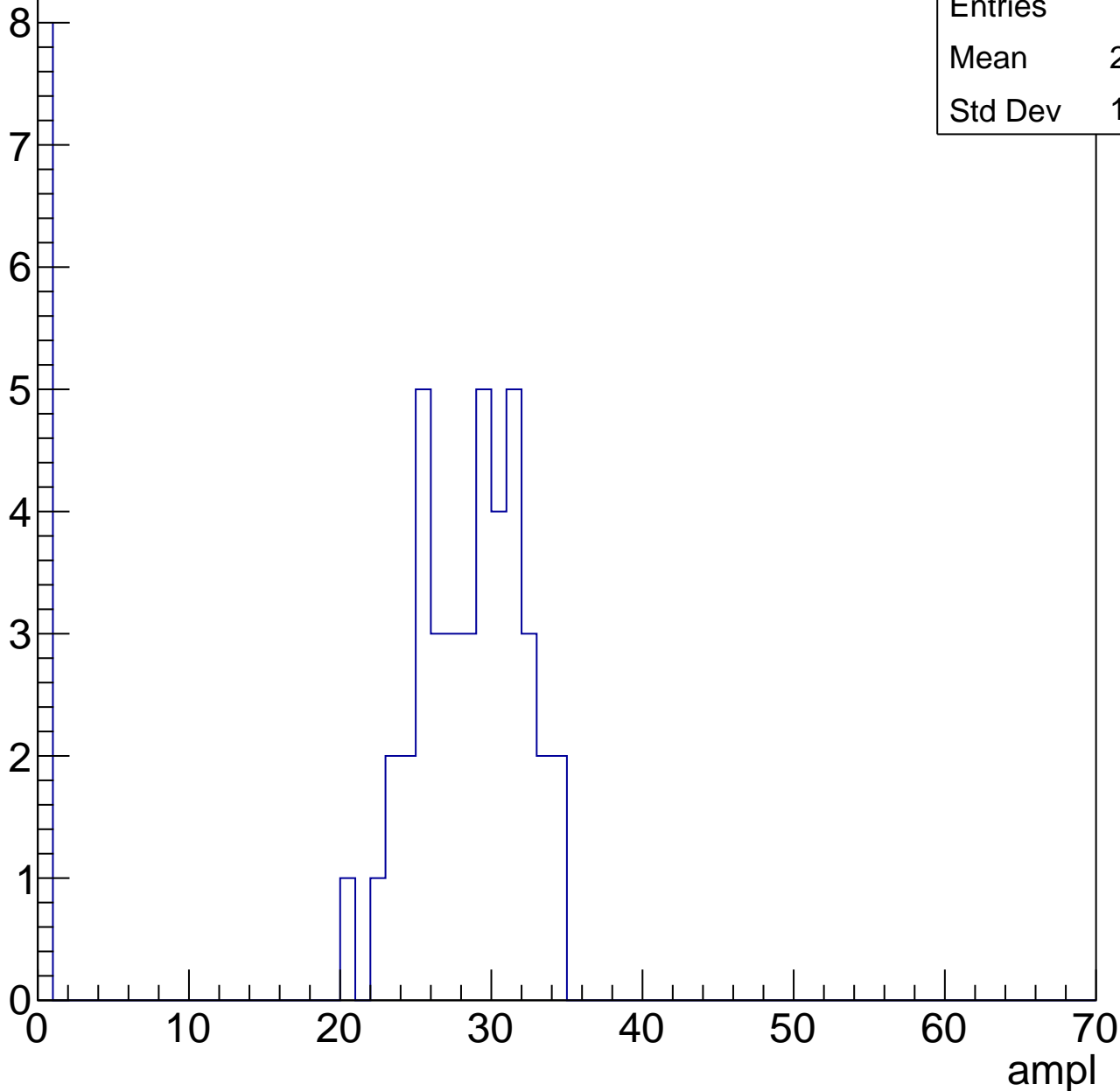


B1L103S, U14-ch52, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

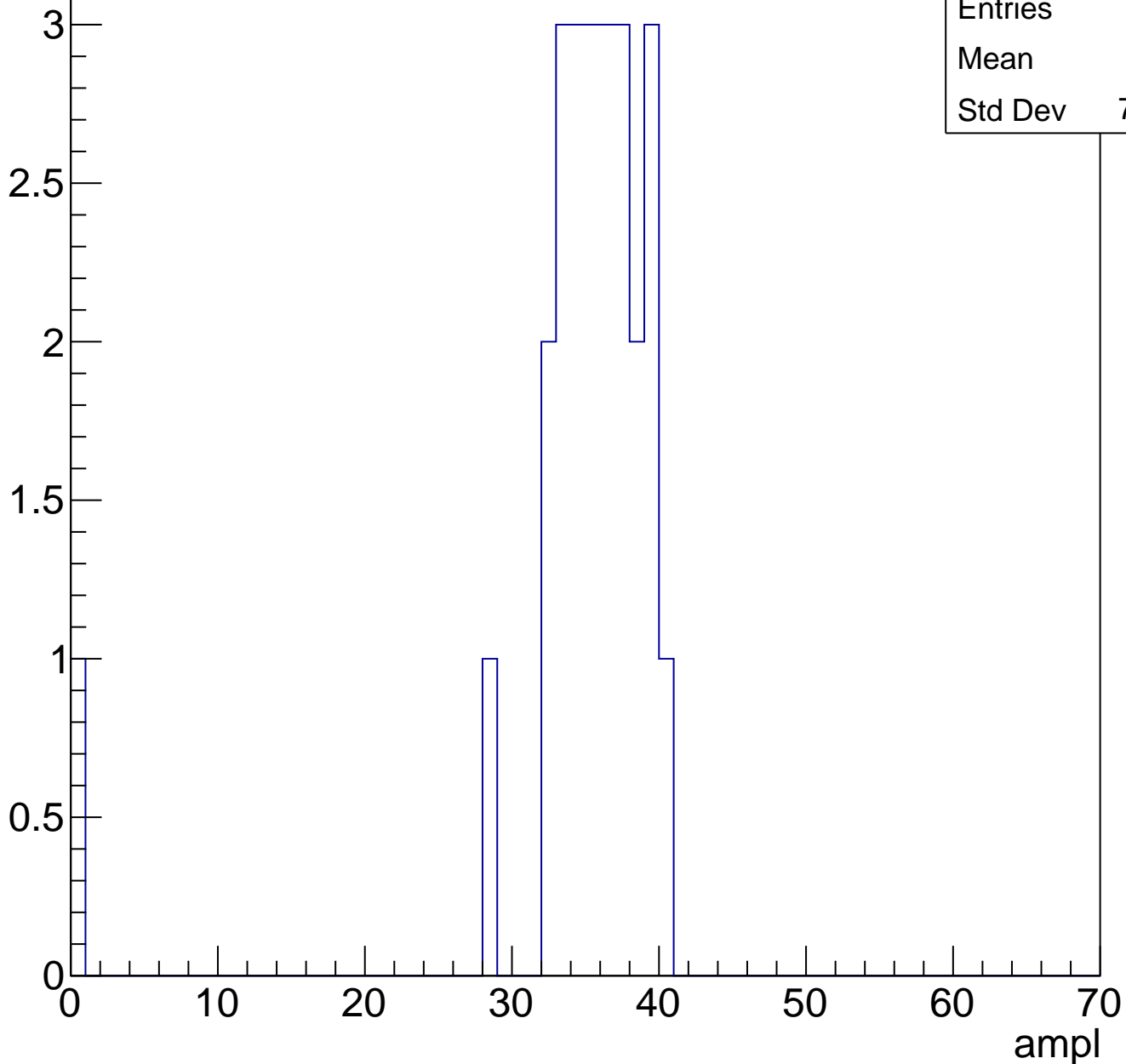
Entries	49
Mean	23.55
Std Dev	10.86



B1L103S, U14-ch52, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

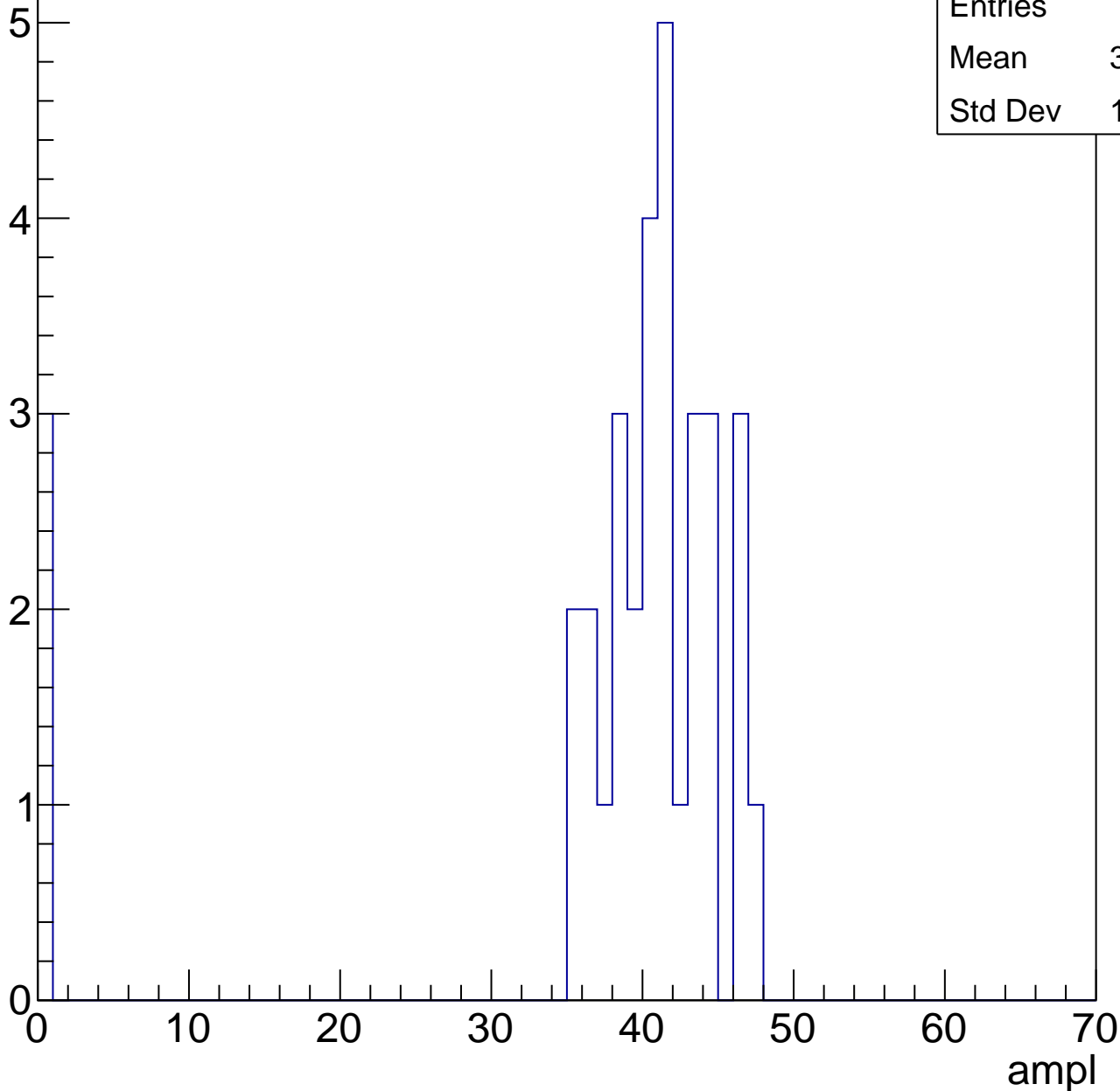


B1L103S, U14-ch52, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	33
Mean	37.09
Std Dev	12.14

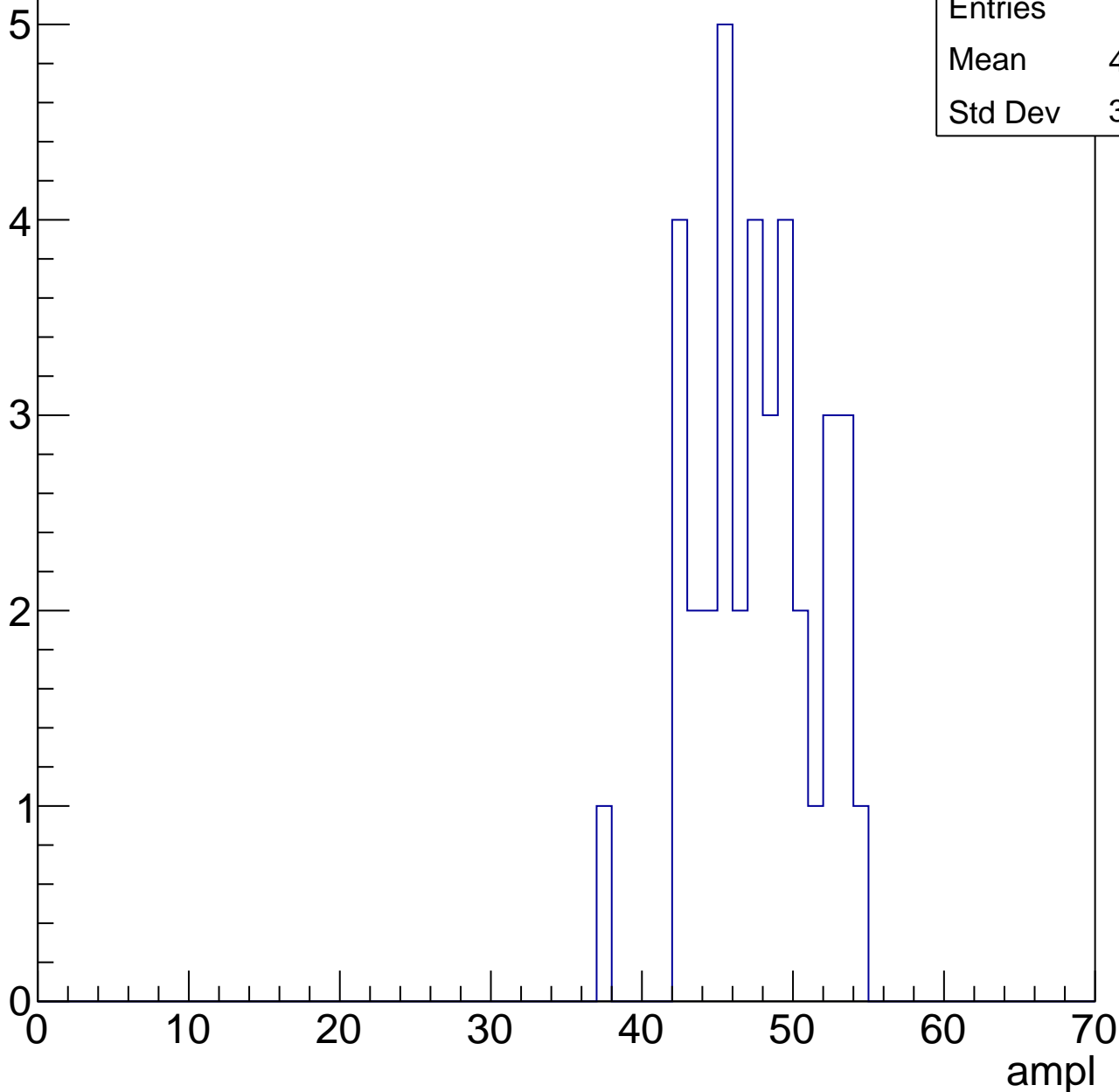


B1L103S, U14-ch52, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	37
Mean	47.14
Std Dev	3.878

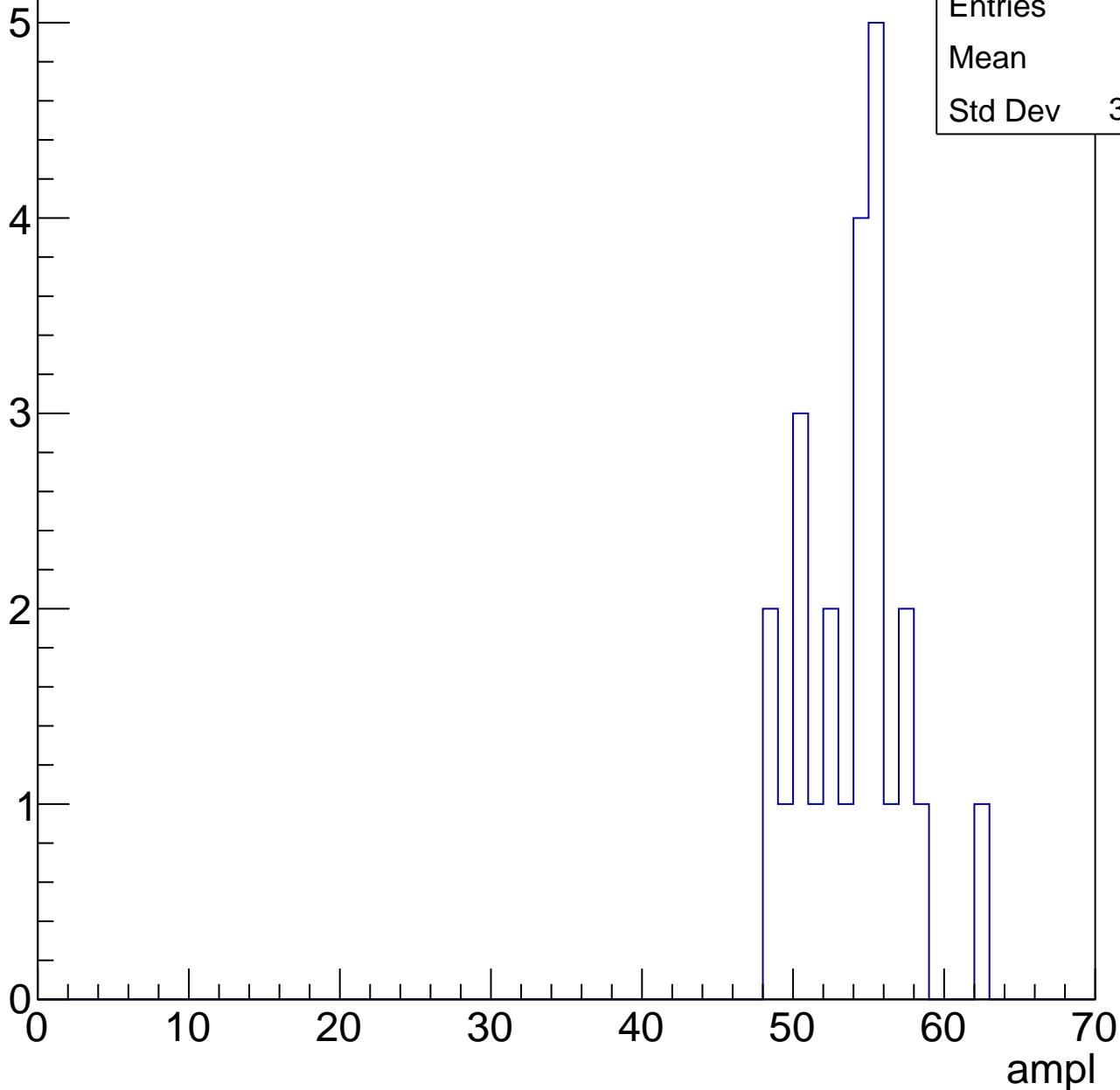


B1L103S, U14-ch52, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

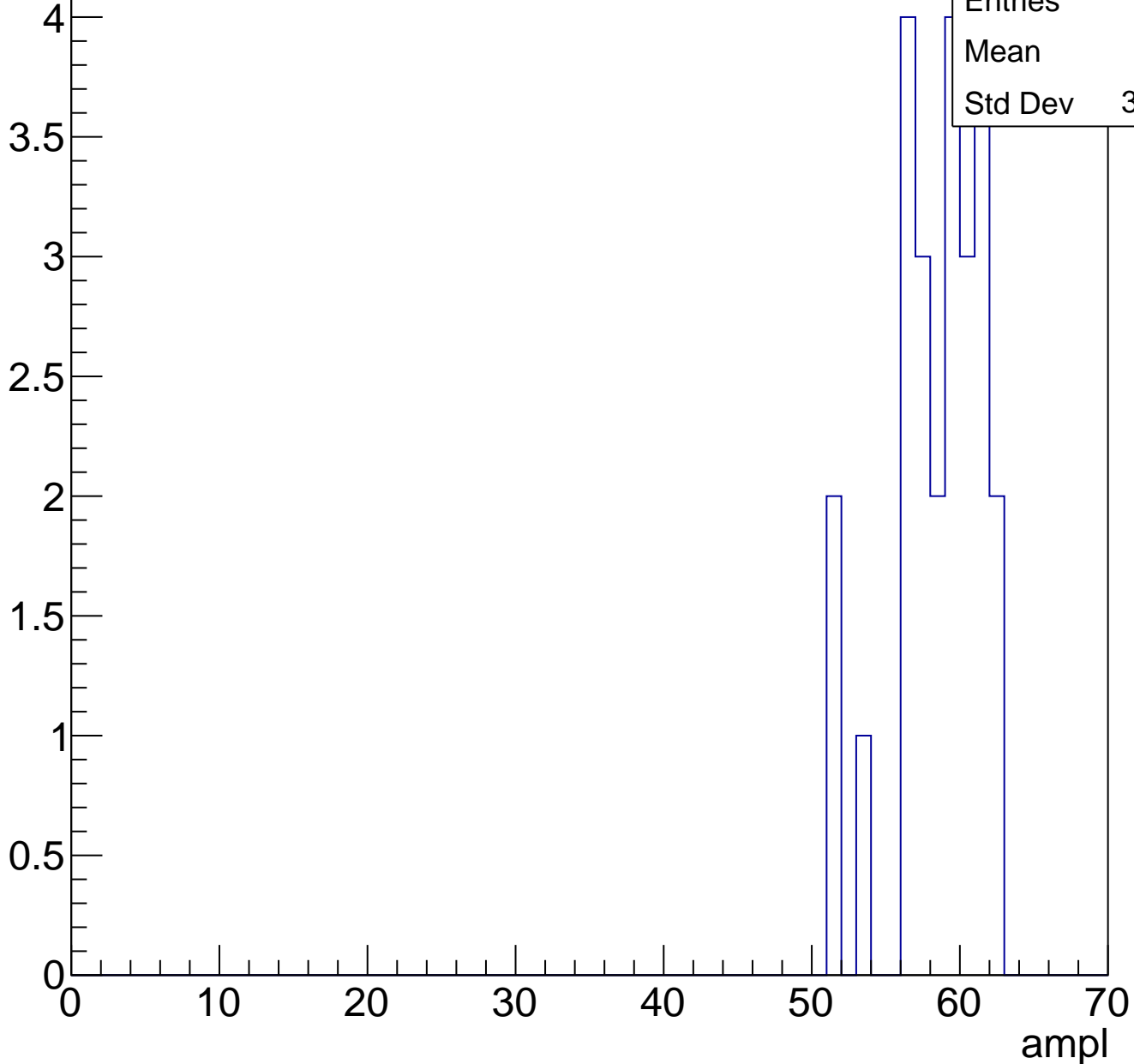
Entries	24
Mean	53.5
Std Dev	3.317



B1L103S, U14-ch52, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

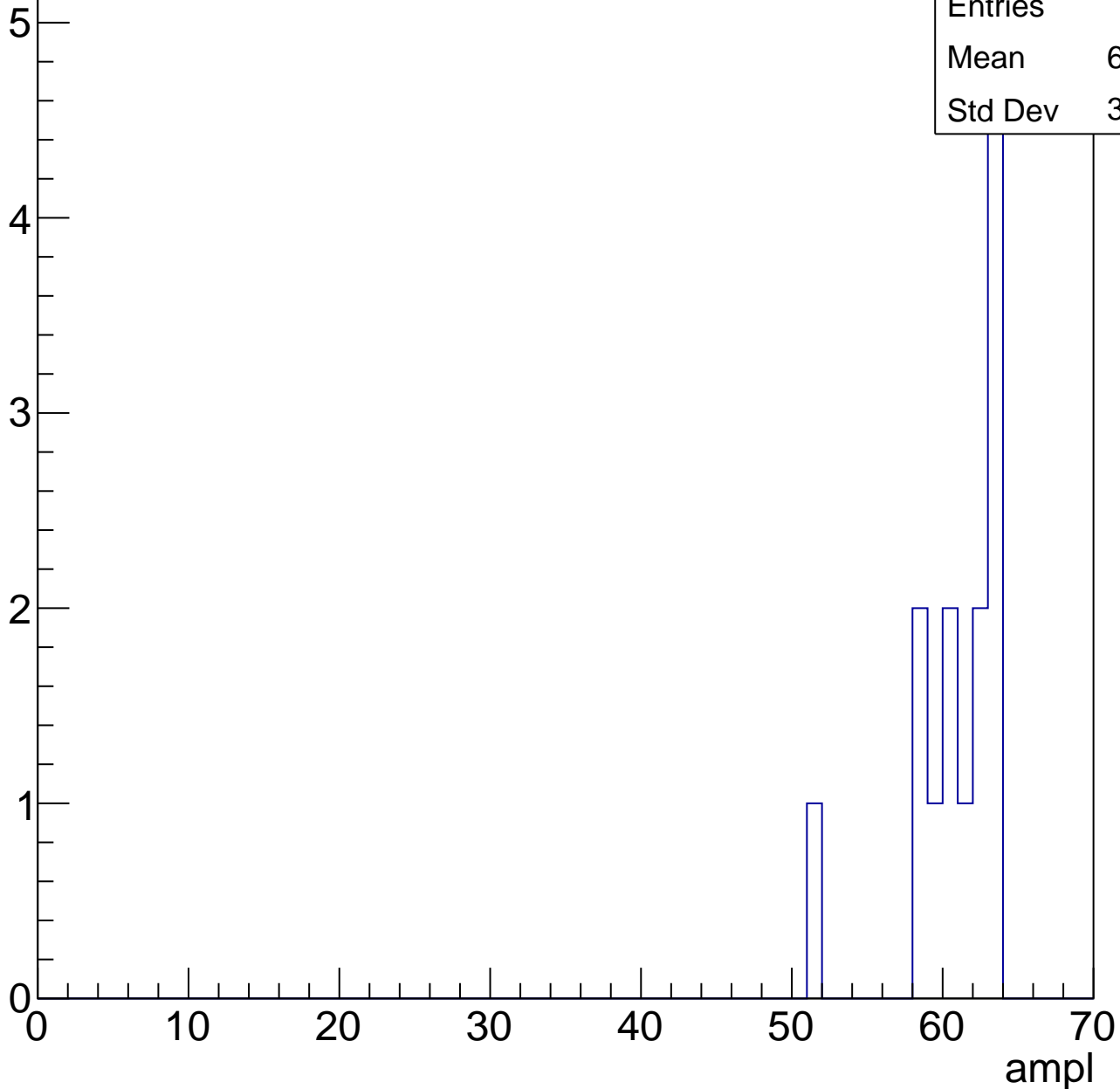


B1L103S, U14-ch52, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	14
Mean	60.43
Std Dev	3.178



B1L103S, U14-ch52, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

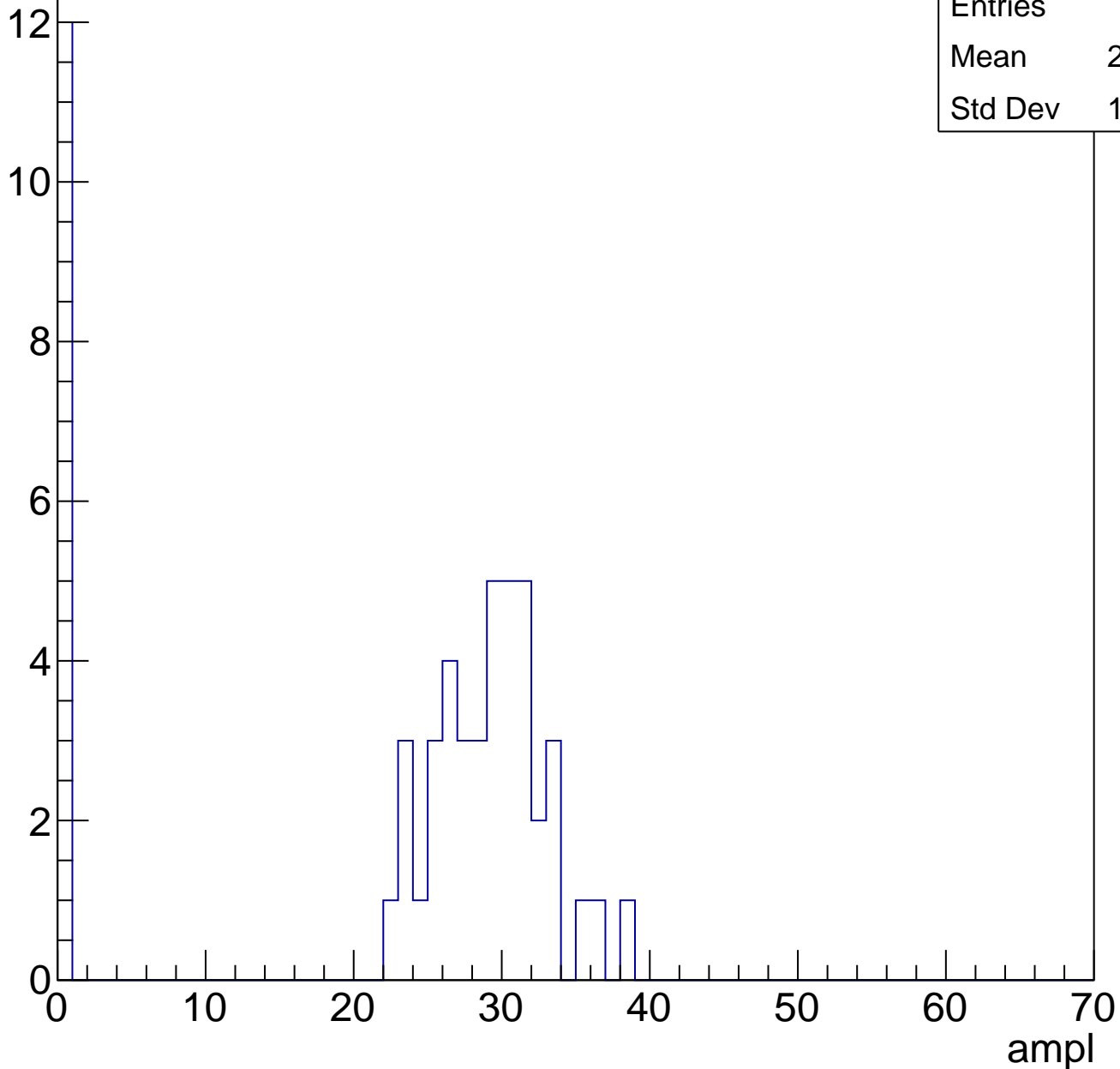
Entries	11
Mean	0
Std Dev	0

B1L103S, U14-ch53, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	53
Mean	22.28
Std Dev	12.47

Entry

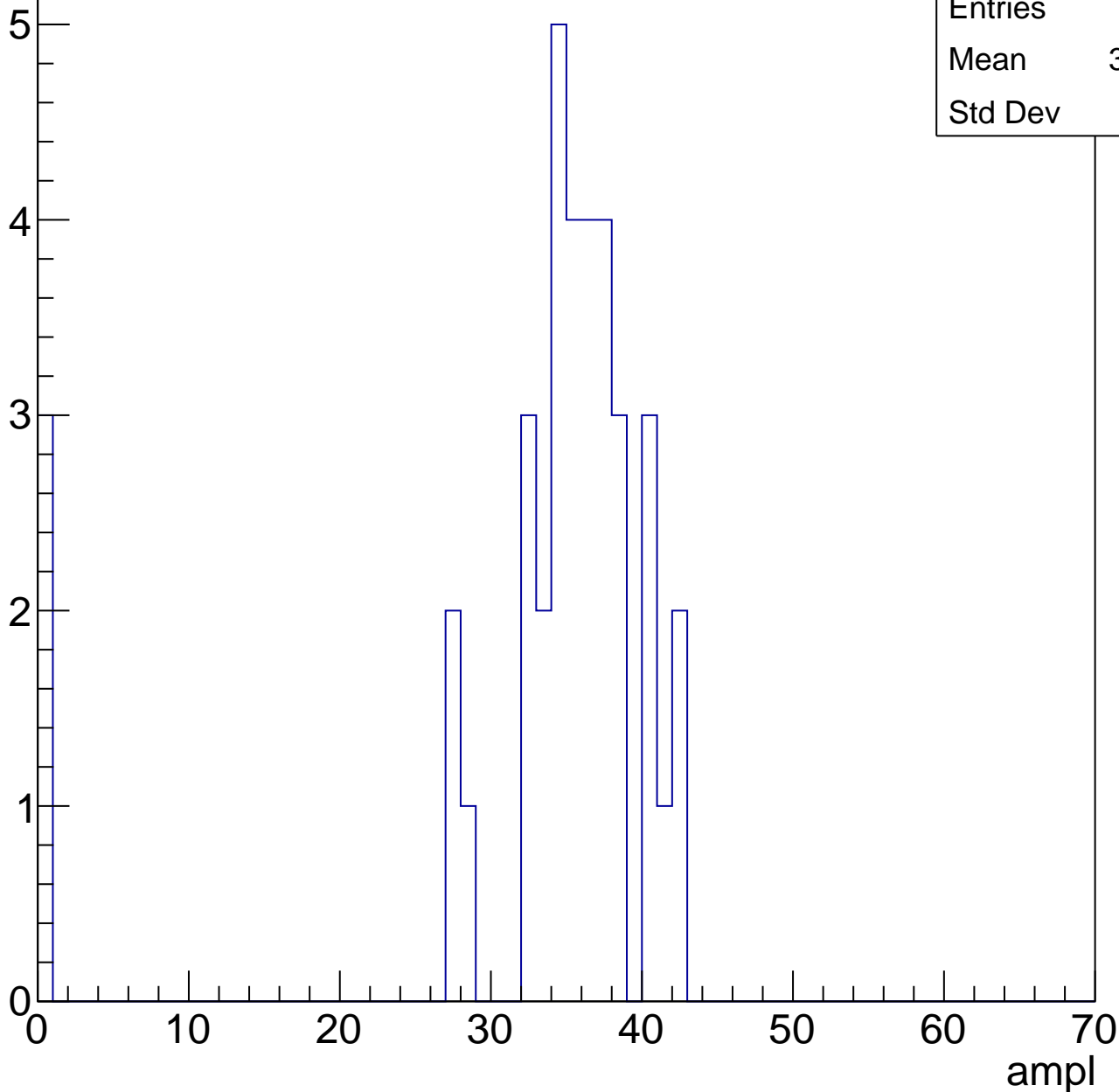


B1L103S, U14-ch53, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	37
Mean	32.57
Std Dev	10.3

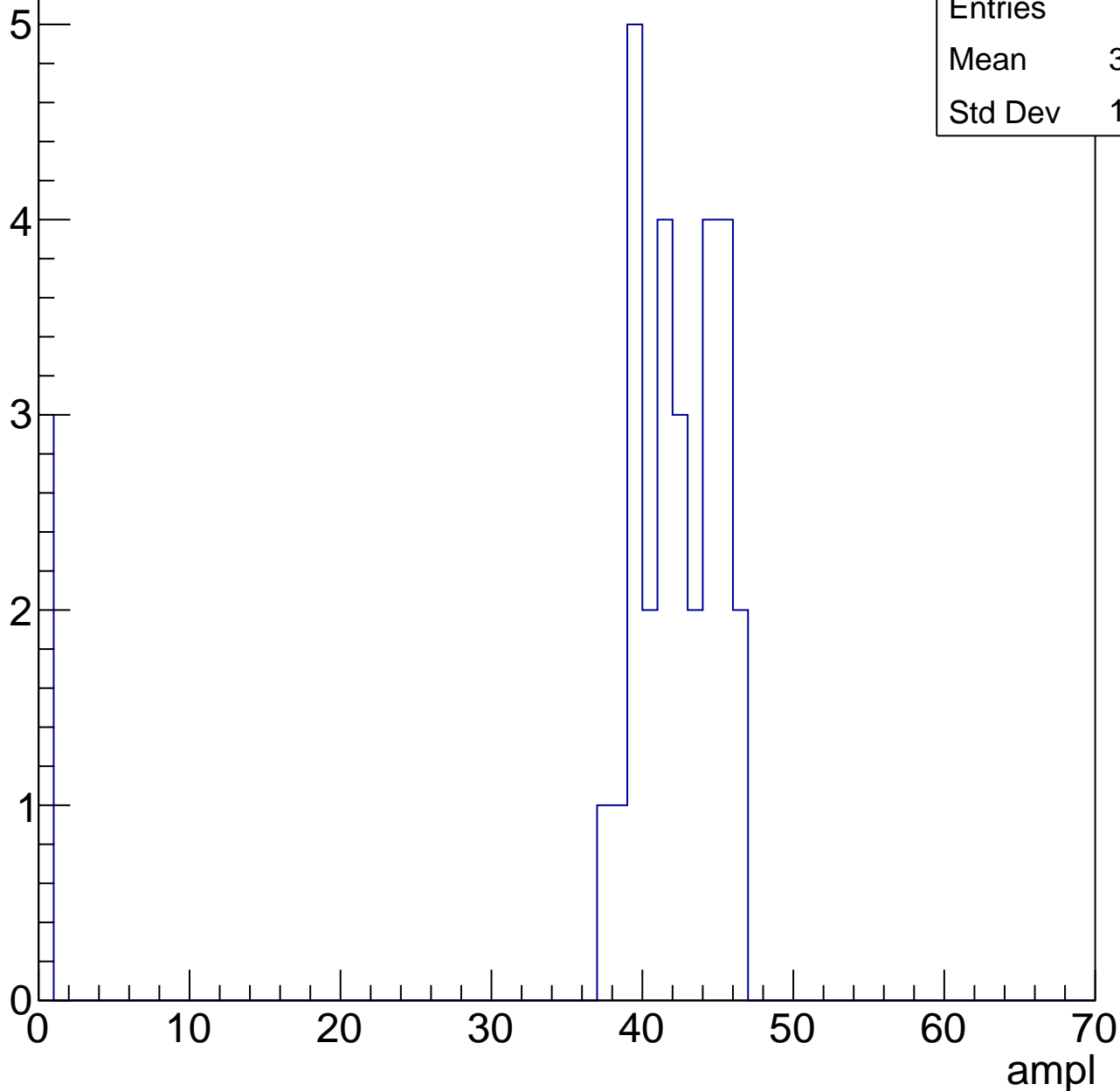


B1L103S, U14-ch53, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

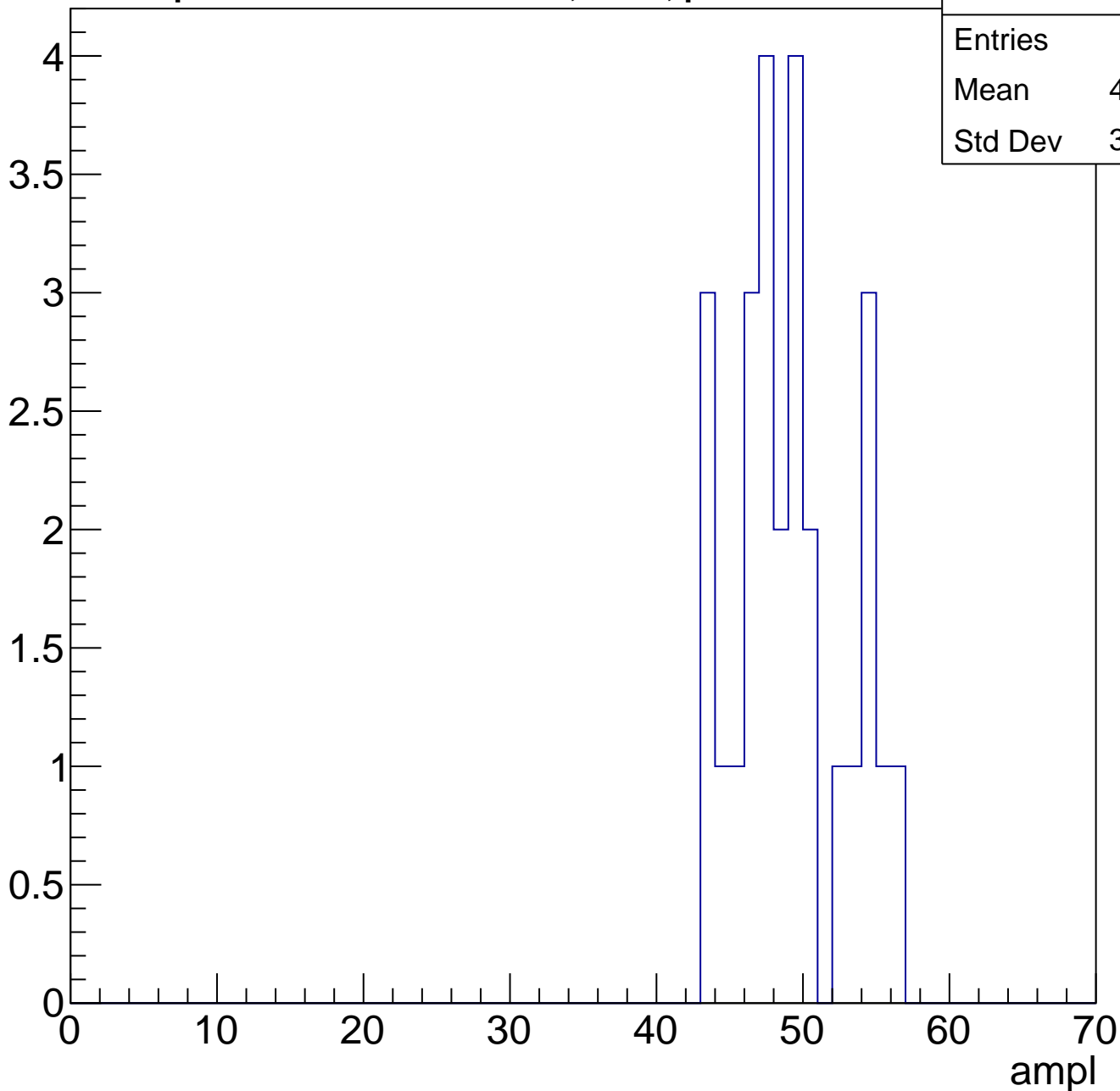
Entries	31
Mean	37.87
Std Dev	12.63



B1L103S, U14-ch53, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

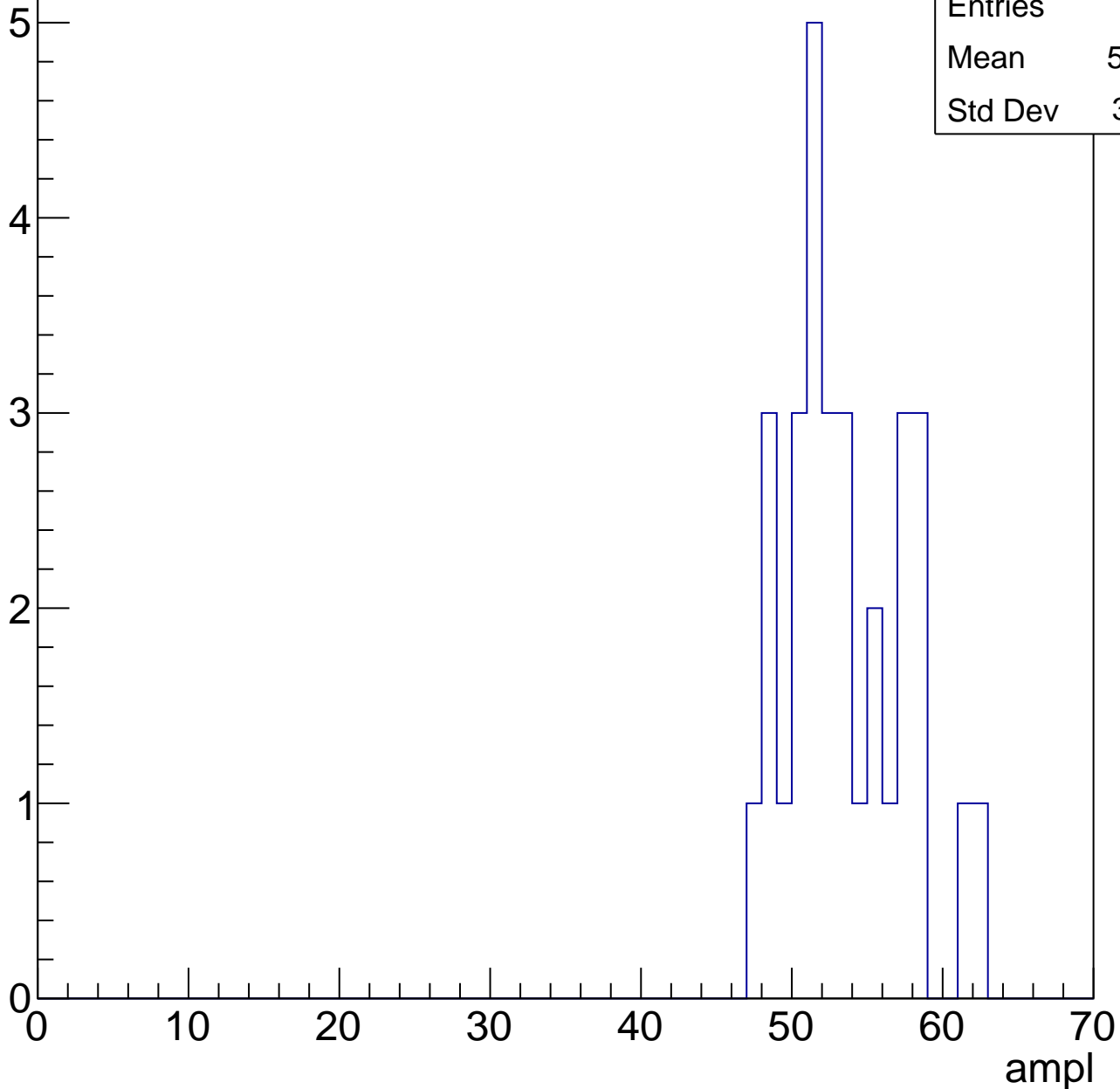


B1L103S, U14-ch53, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

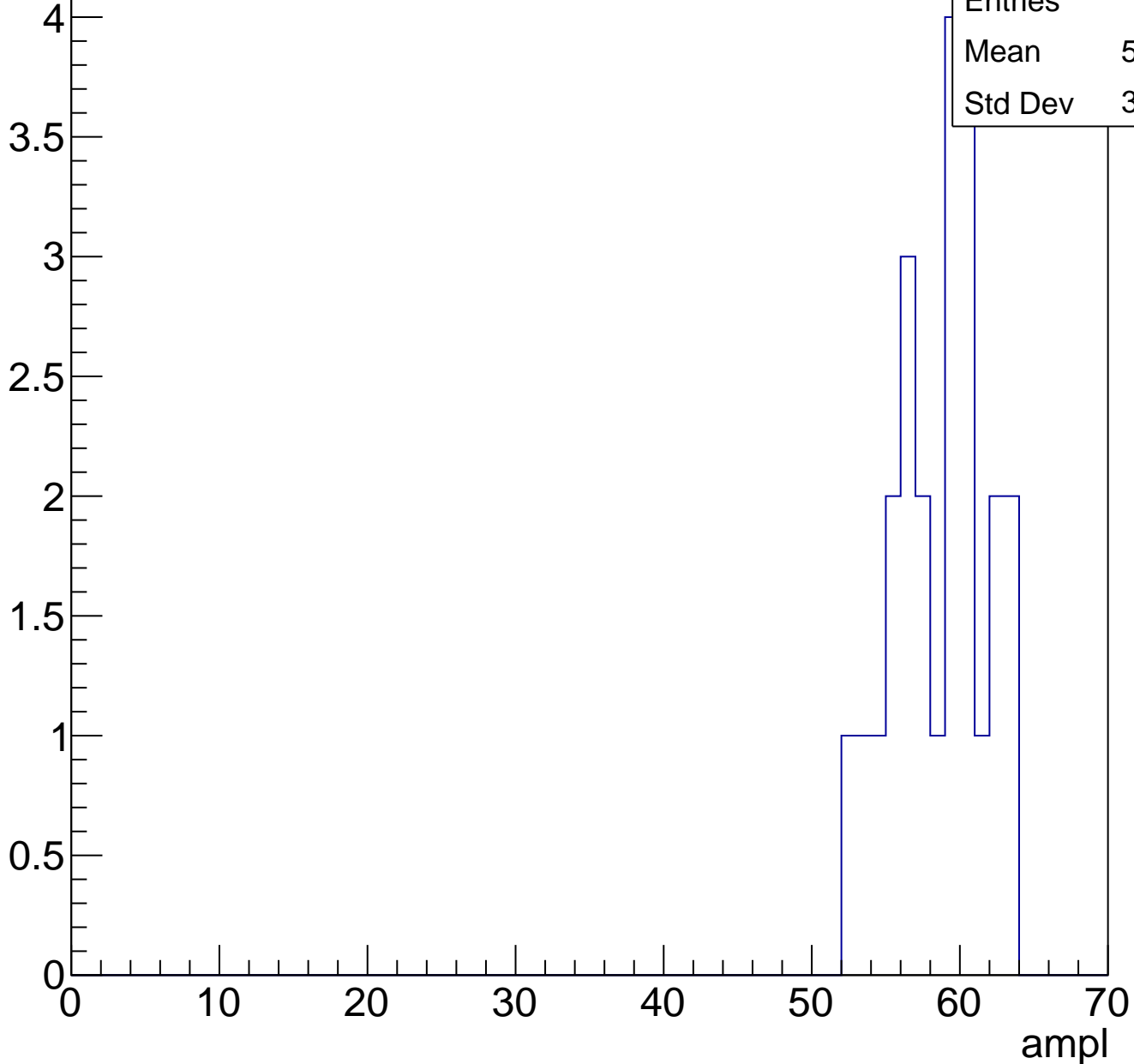
Entries	31
Mean	53.16
Std Dev	3.861



B1L103S, U14-ch53, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch53, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries	11
Mean	61.18
Std Dev	1.585

B1L103S, U14-ch53, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

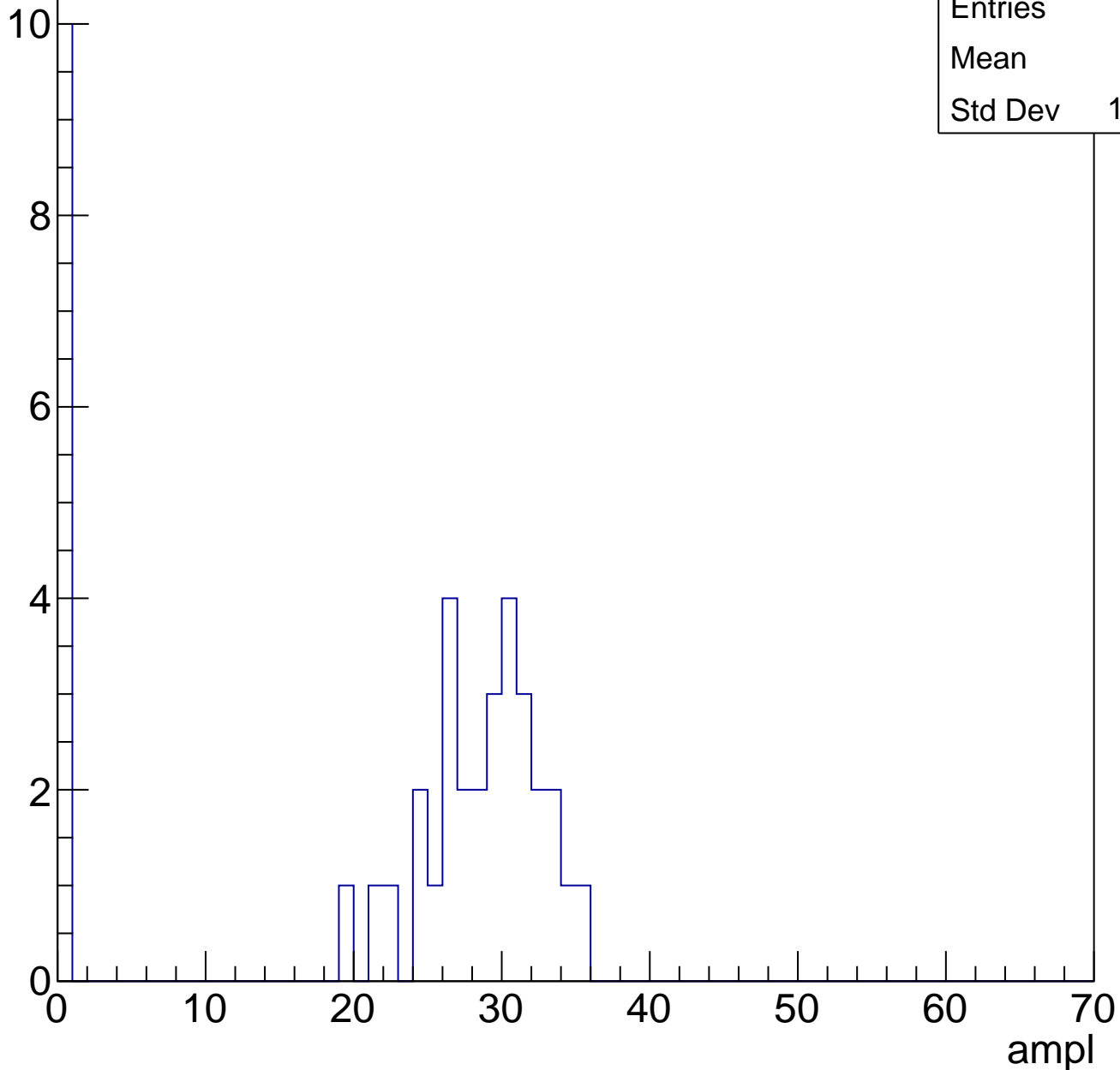
Entries	11
Mean	0
Std Dev	0

B1L103S, U14-ch54, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	40
Mean	21.2
Std Dev	12.68

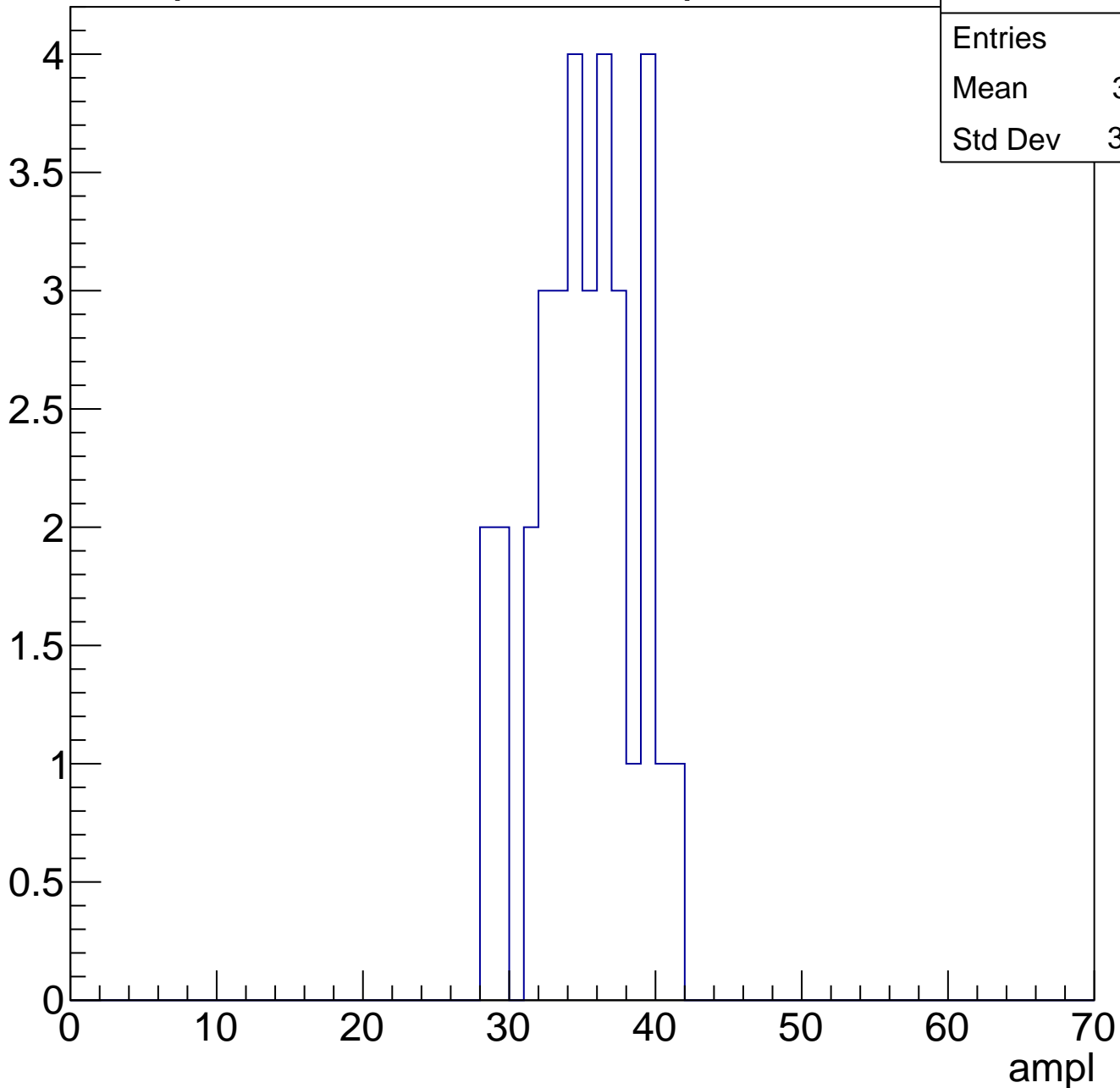
Entry



B1L103S, U14-ch54, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

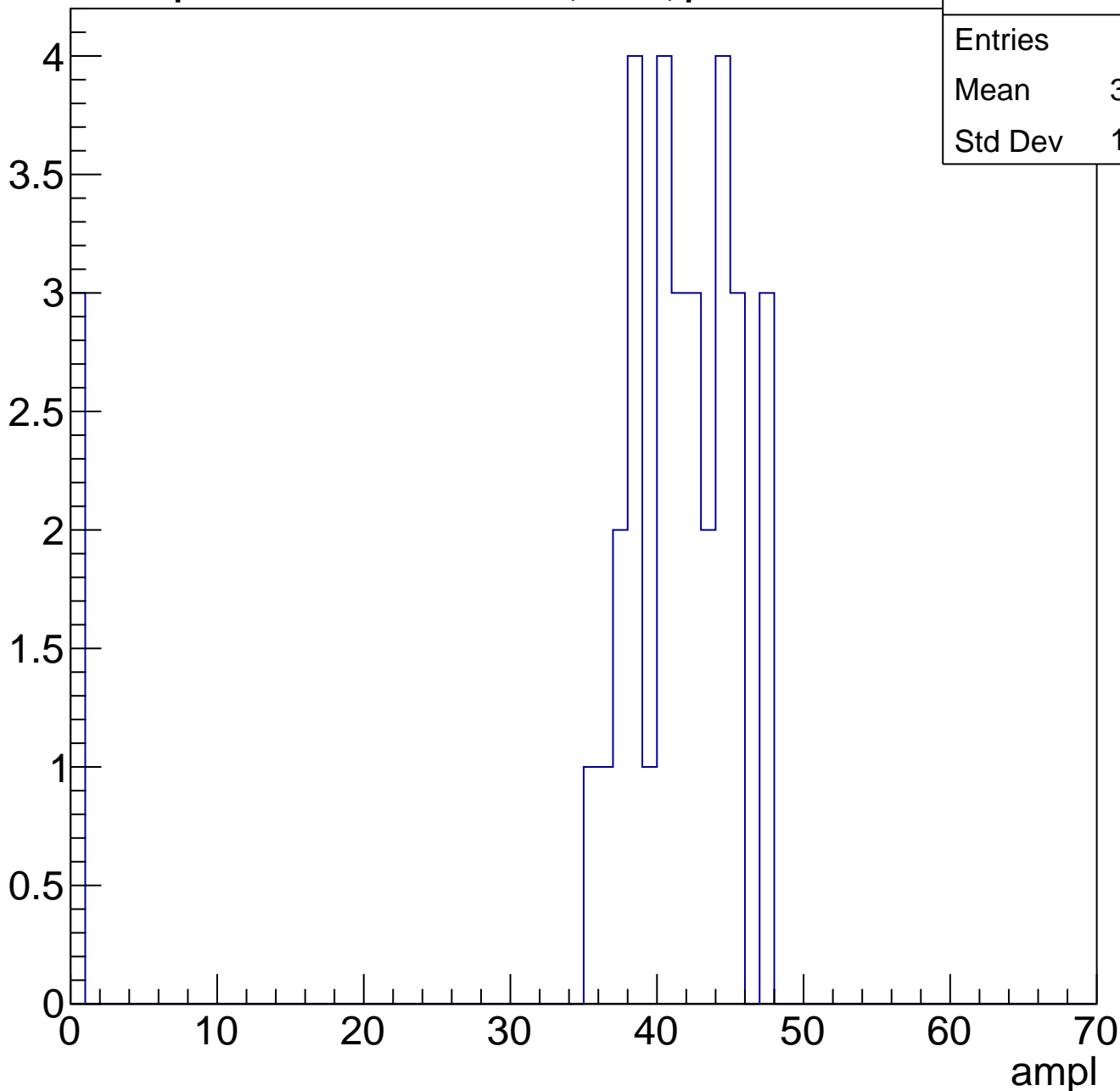


Entries	33
Mean	34.61
Std Dev	3.437

B1L103S, U14-ch54, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry



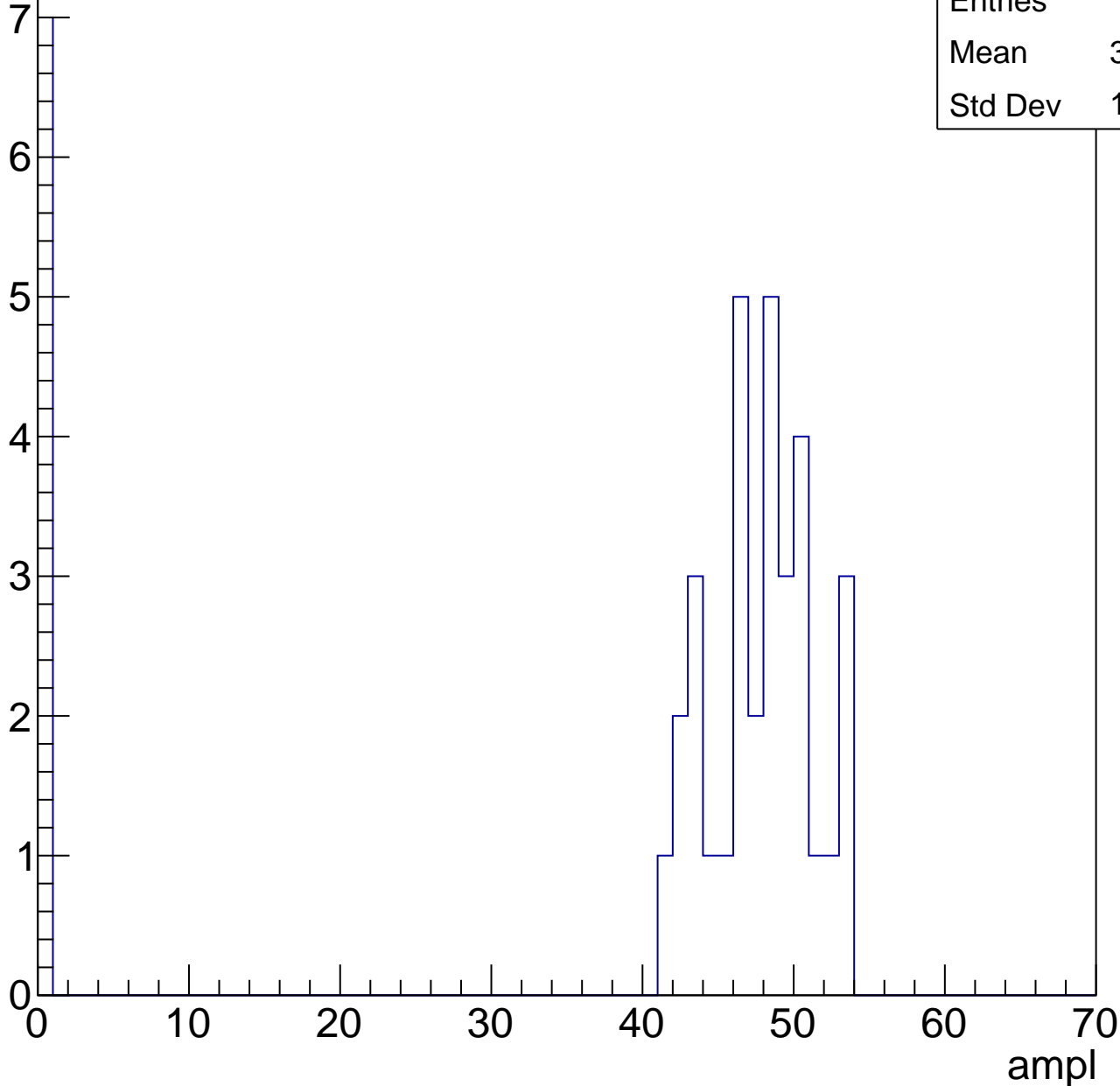
Entries	34
Mean	37.74
Std Dev	12.15

B1L103S, U14-ch54, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	38.87
Std Dev	18.43

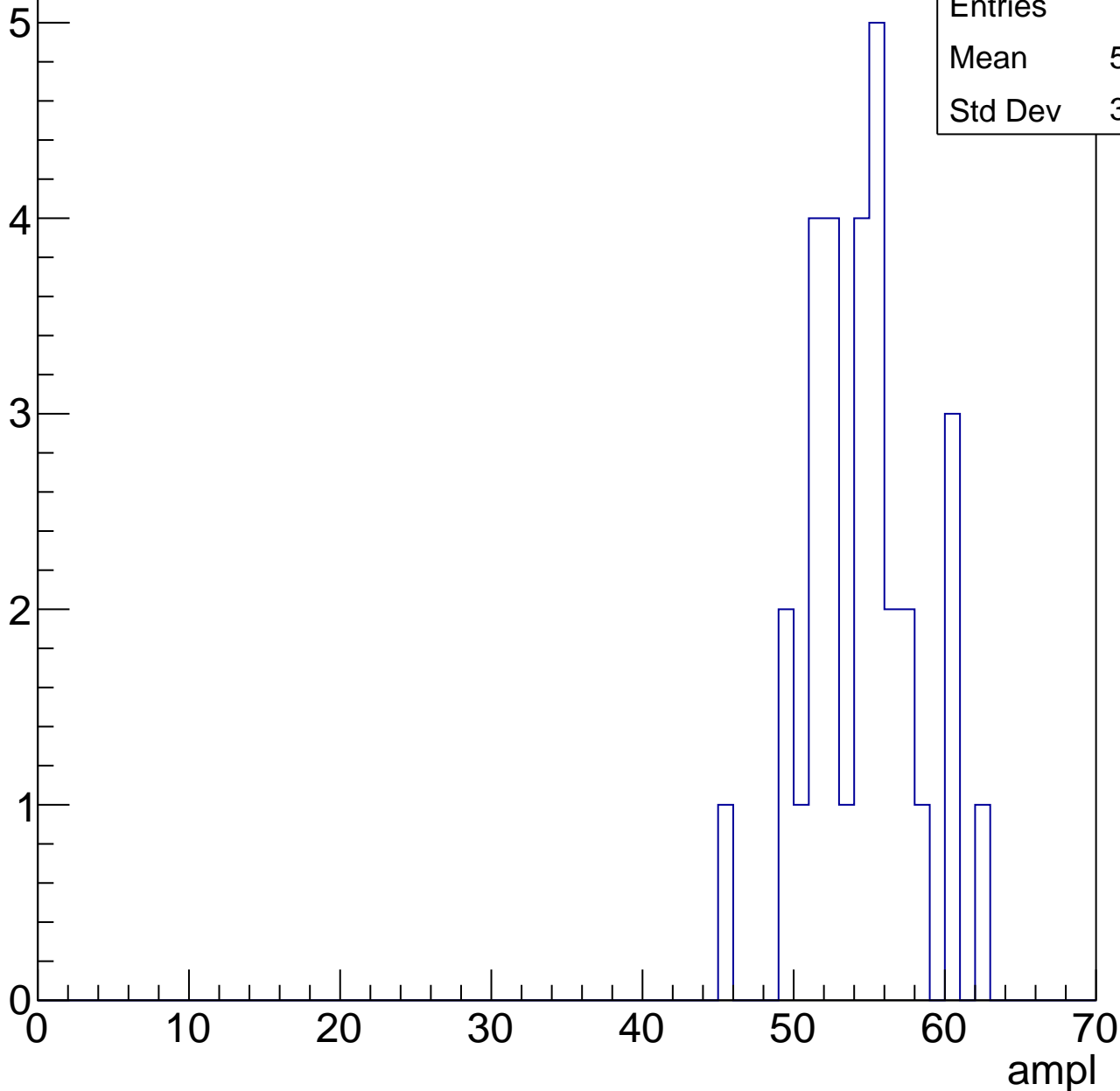


B1L103S, U14-ch54, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

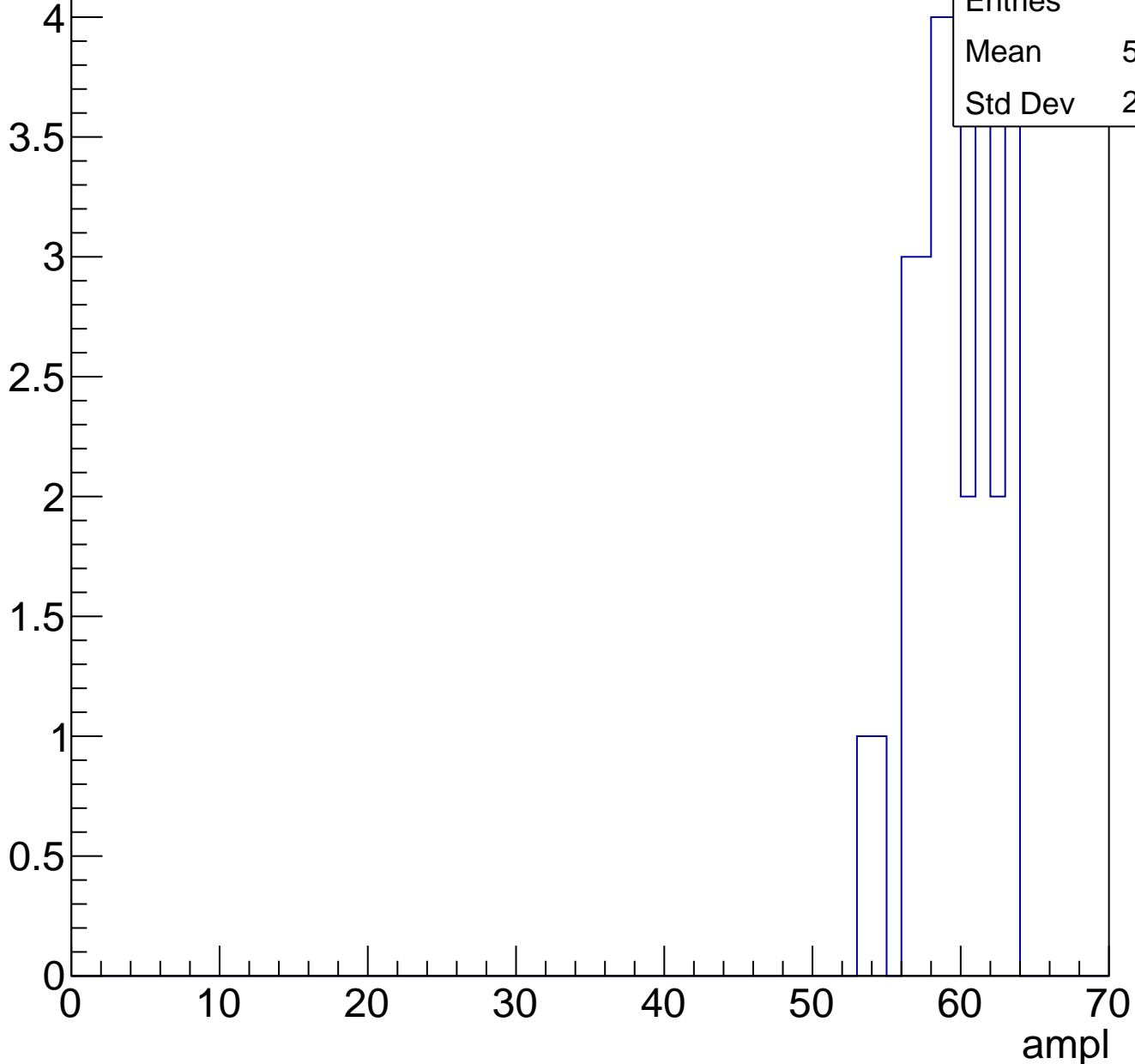
Entries	31
Mean	54.03
Std Dev	3.676



B1L103S, U14-ch54, adc5

calib_packv5_041523_1651.root, FC#0, port C2

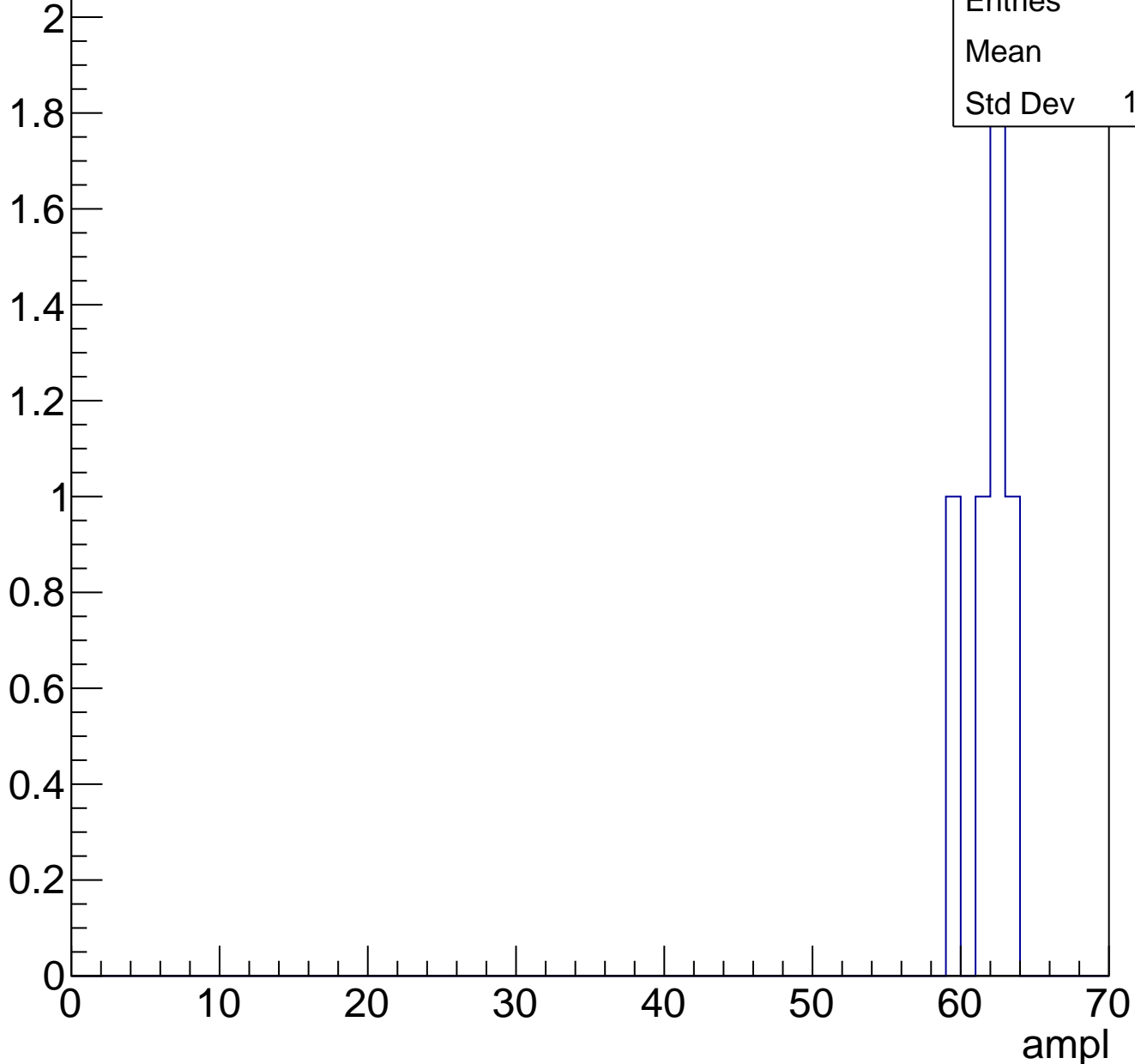
Entry



B1L103S, U14-ch54, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



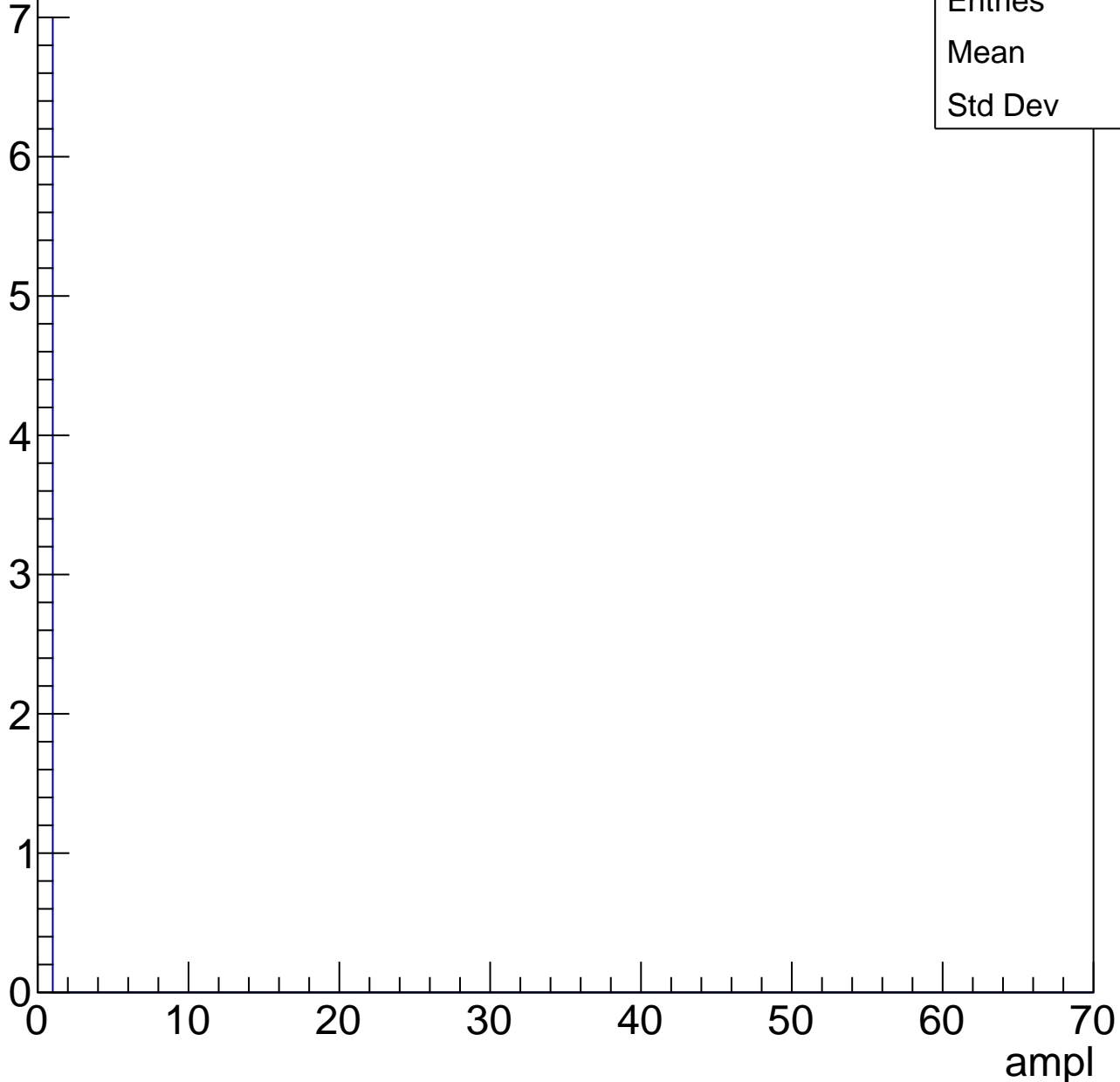
Entries	5
Mean	61.4
Std Dev	1.356

B1L103S, U14-ch54, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	7
Mean	0
Std Dev	0

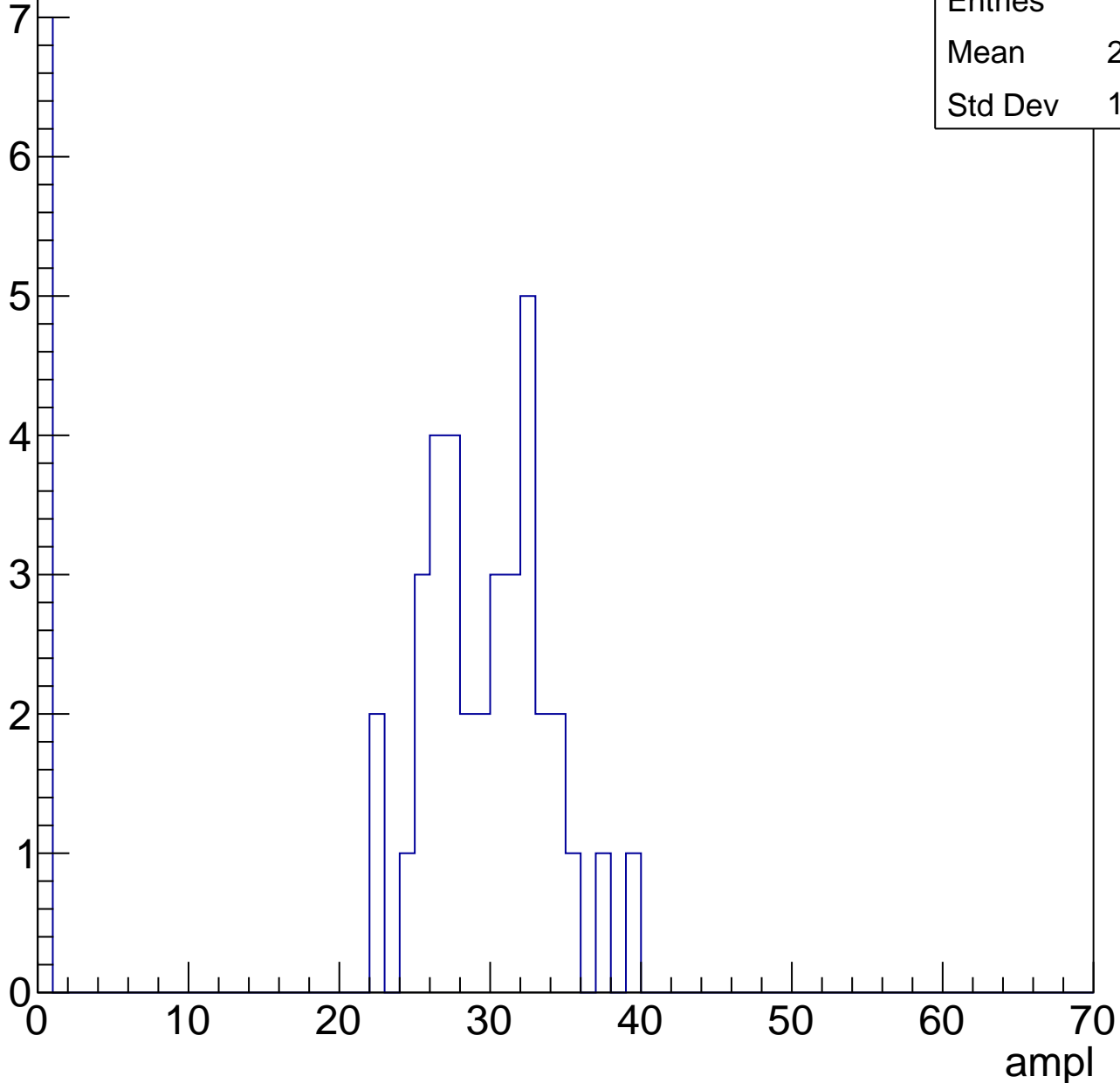


B1L103S, U14-ch55, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	43
Mean	24.58
Std Dev	11.43

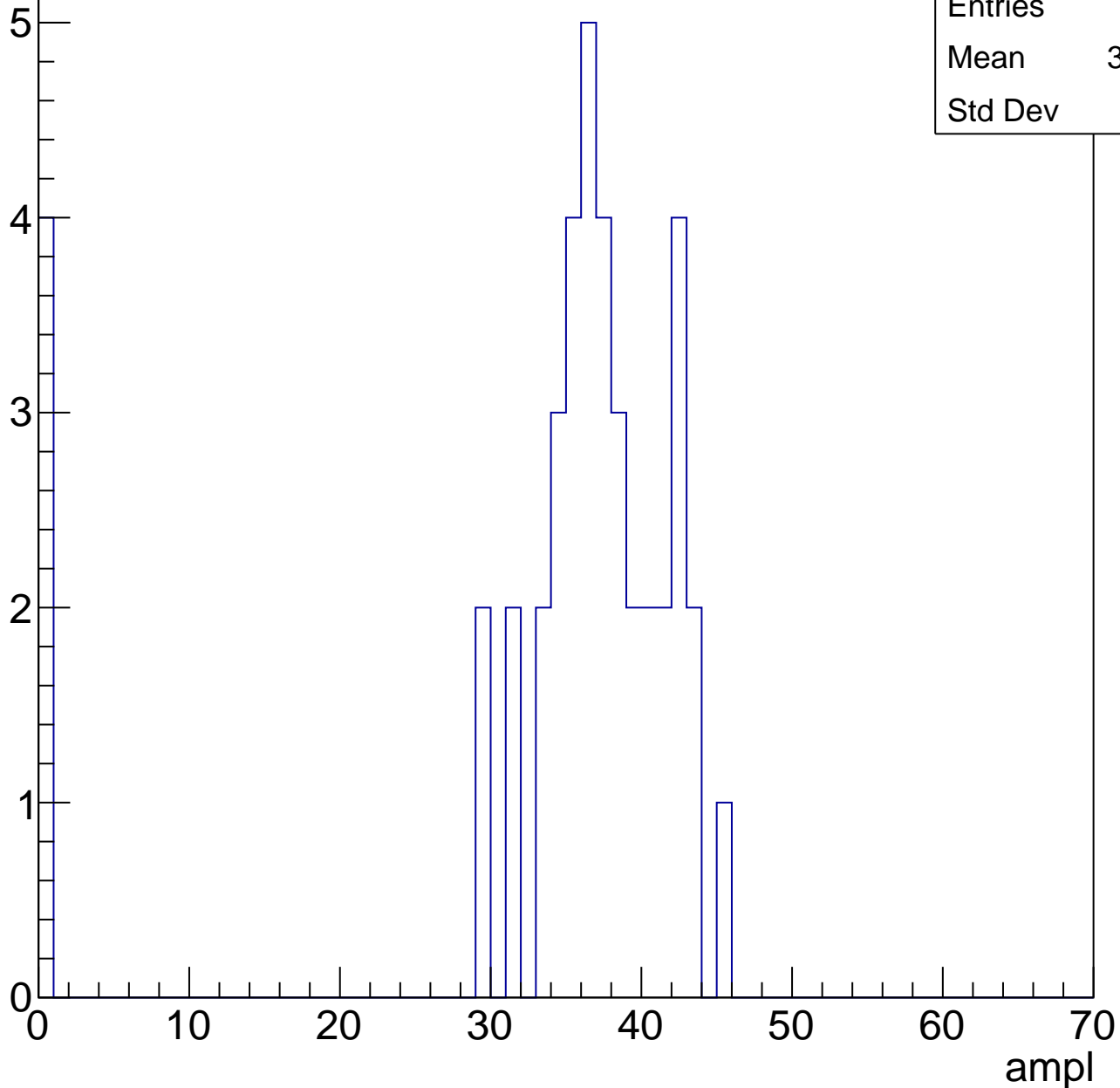


B1L103S, U14-ch55, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

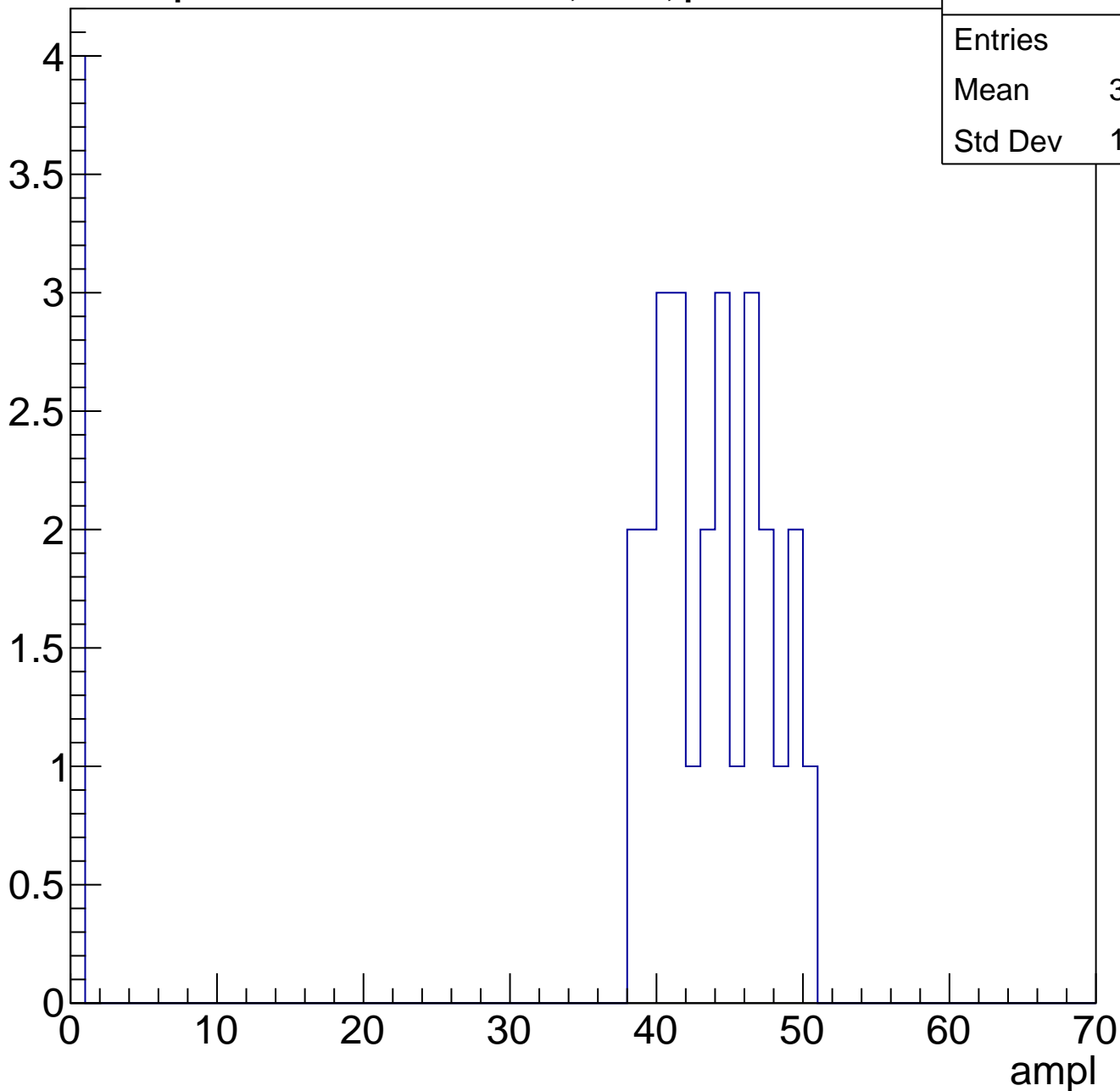
Entries	42
Mean	33.55
Std Dev	11.5



B1L103S, U14-ch55, adc2

calib_packv5_041523_1651.root, FC#0, port C2

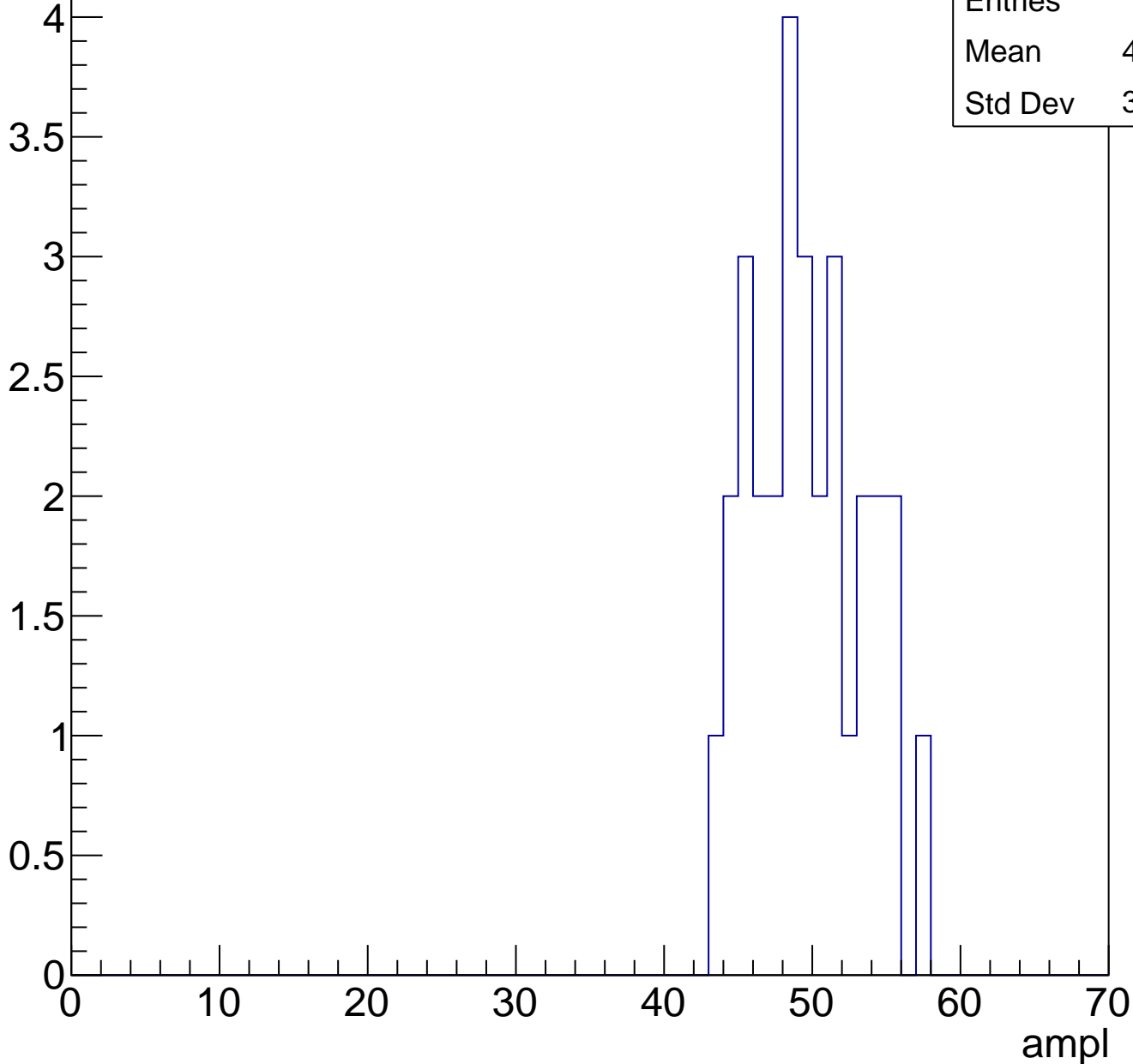
Entry



B1L103S, U14-ch55, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

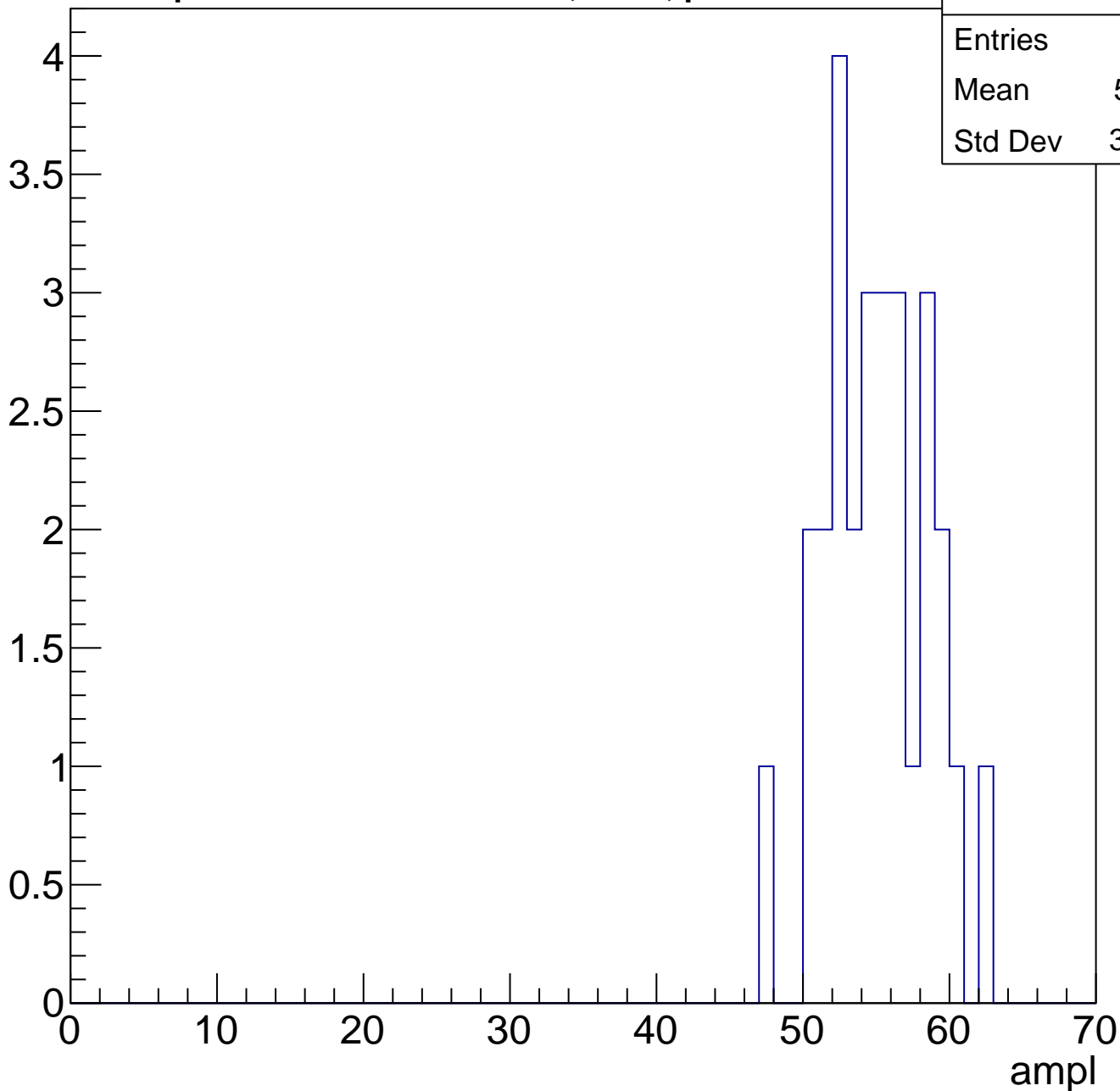


Entries	30
Mean	49.23
Std Dev	3.667

B1L103S, U14-ch55, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

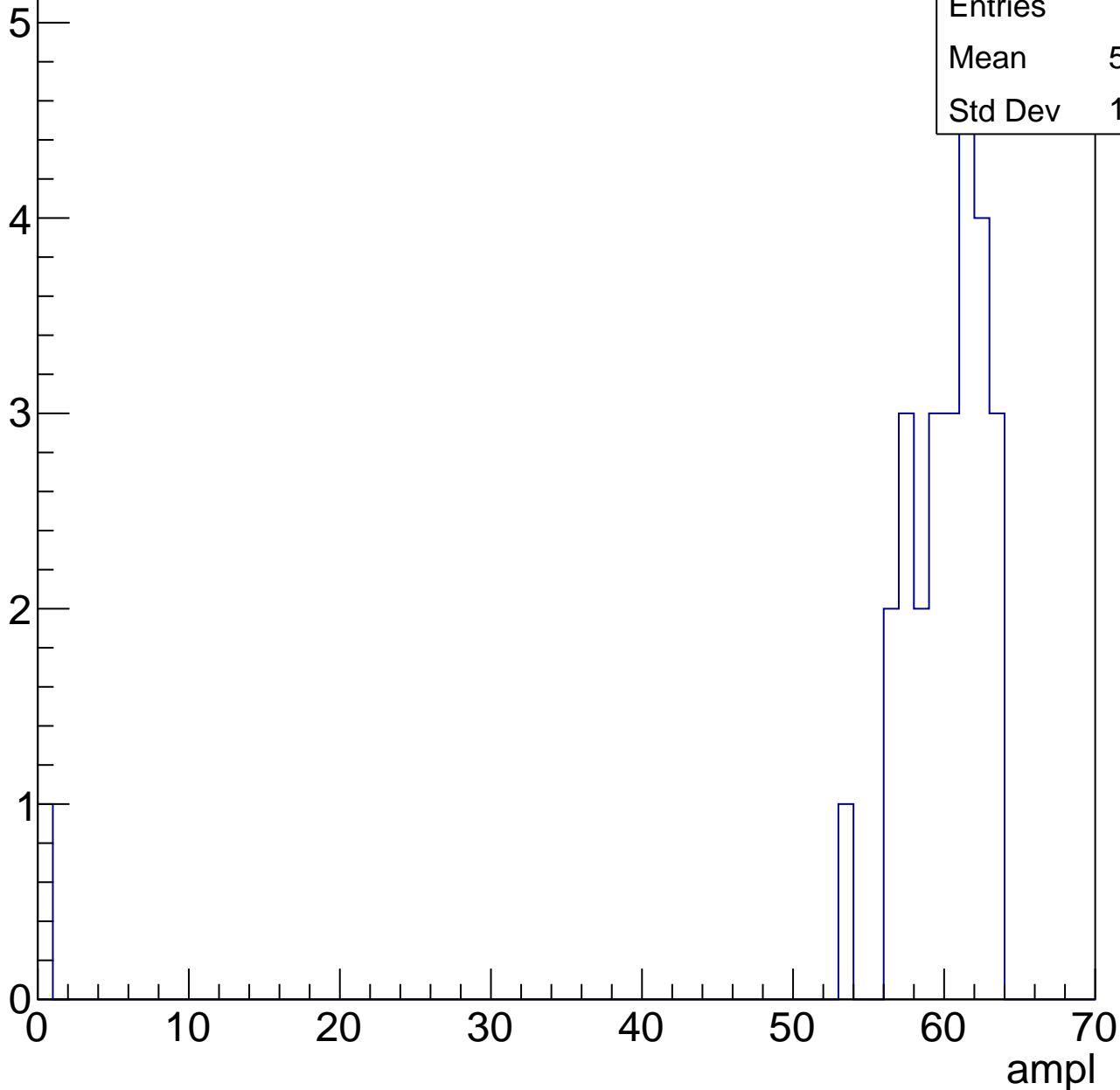


B1L103S, U14-ch55, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	27
Mean	57.44
Std Dev	11.53



B1L103S, U14-ch55, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

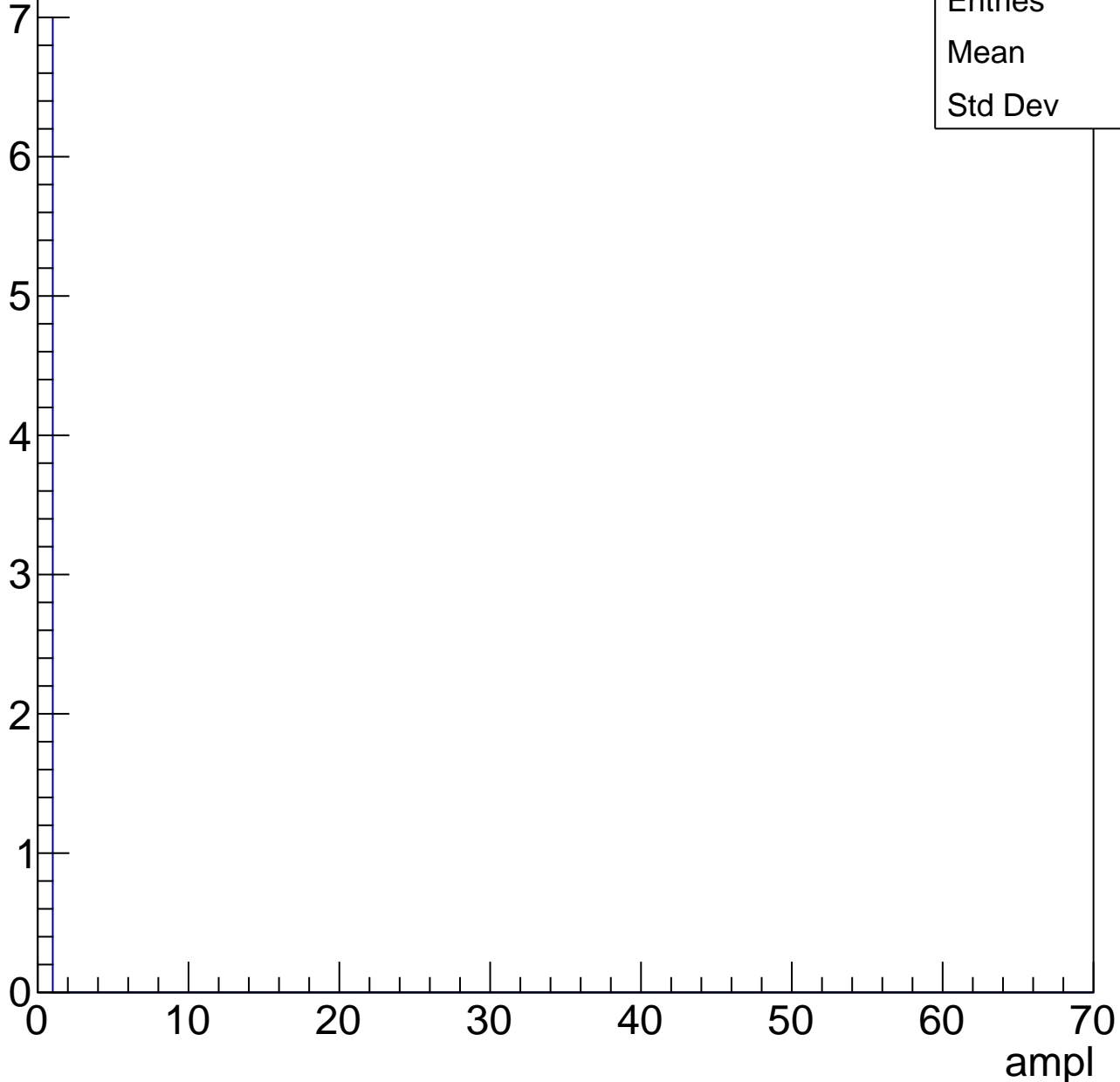


B1L103S, U14-ch55, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

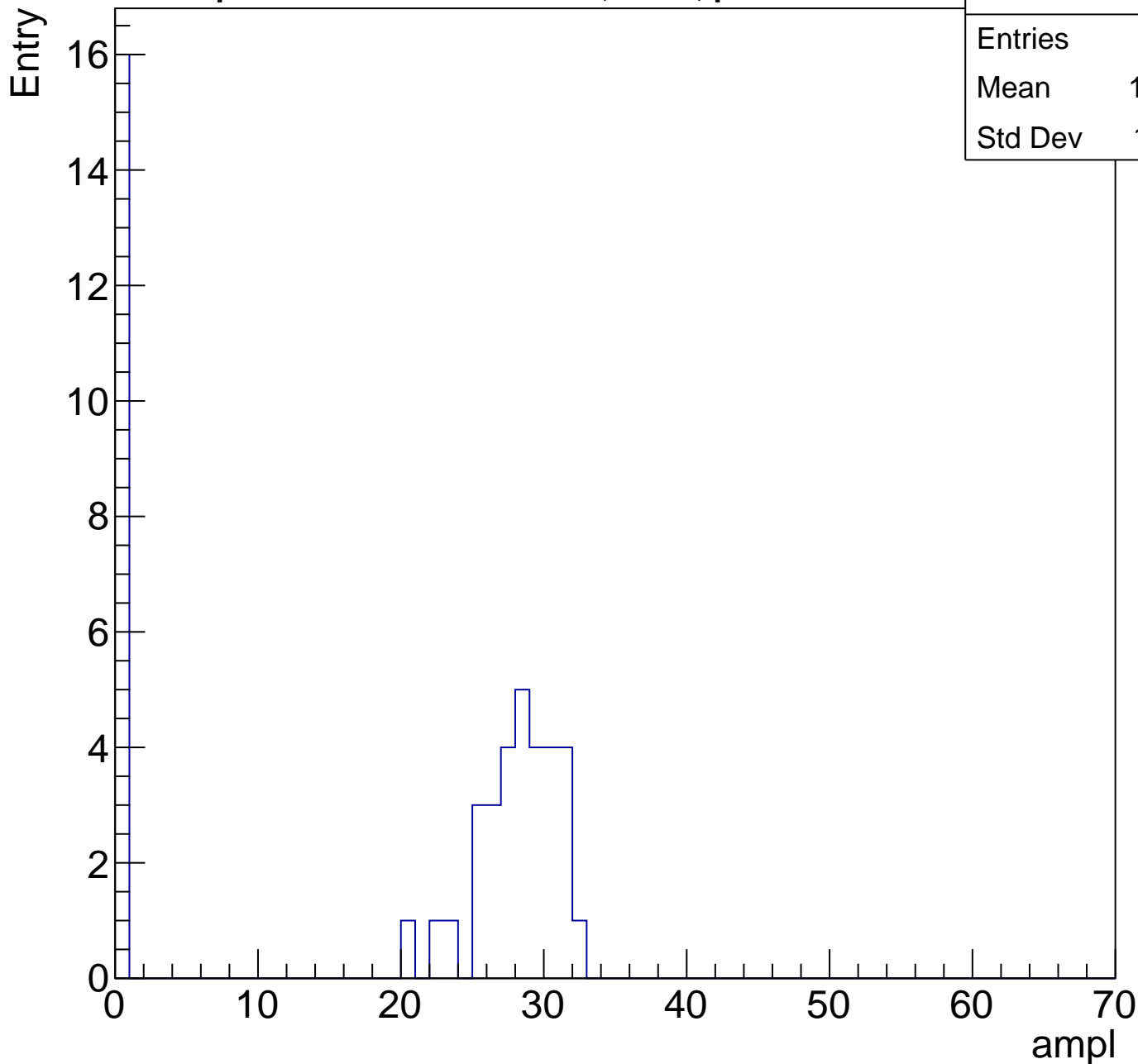
Entries	7
Mean	0
Std Dev	0



B1L103S, U14-ch56, adc0

calib_packv5_041523_1651.root, FC#0, port C2

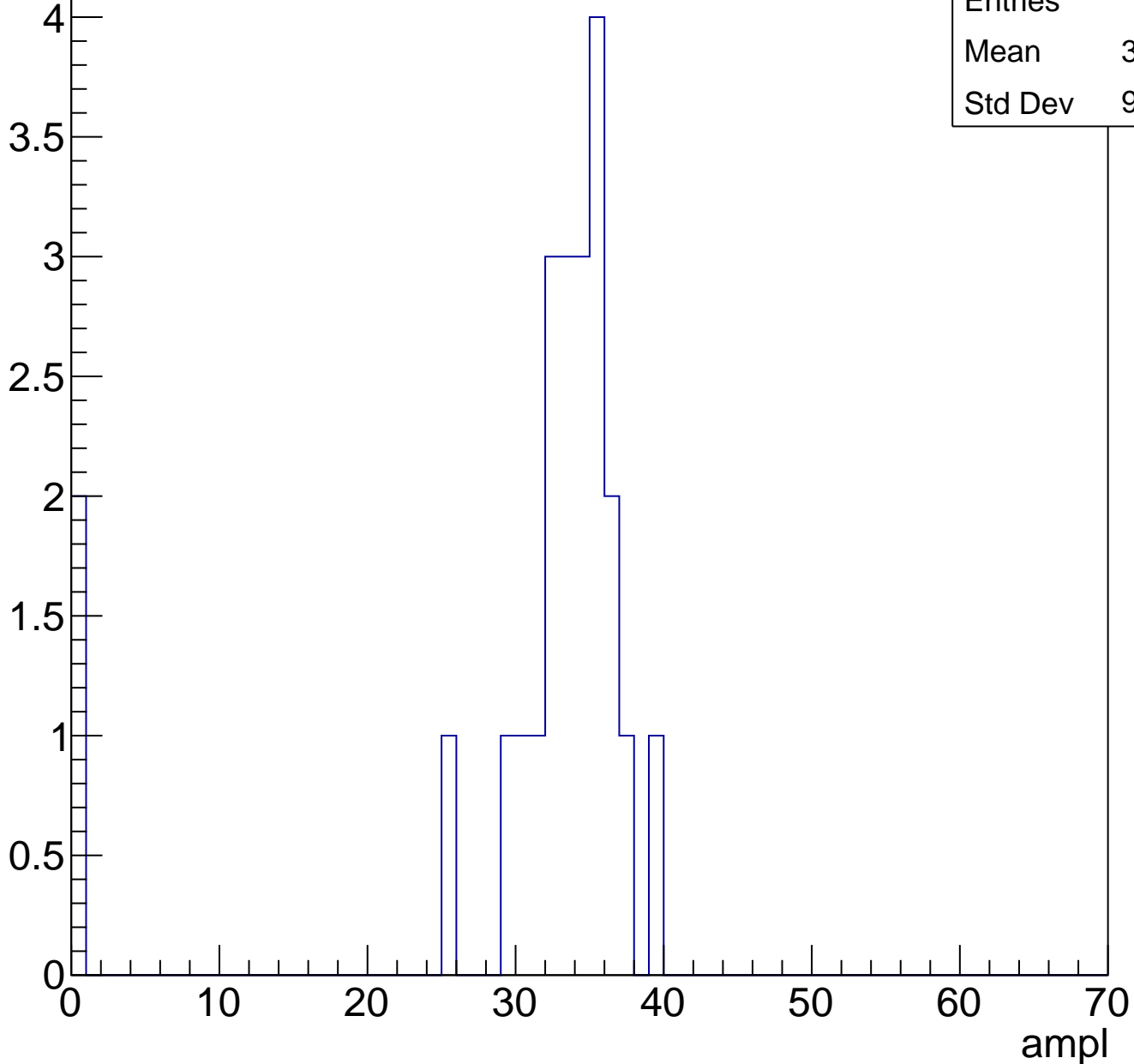
Entries	47
Mean	18.26
Std Dev	13.31



B1L103S, U14-ch56, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

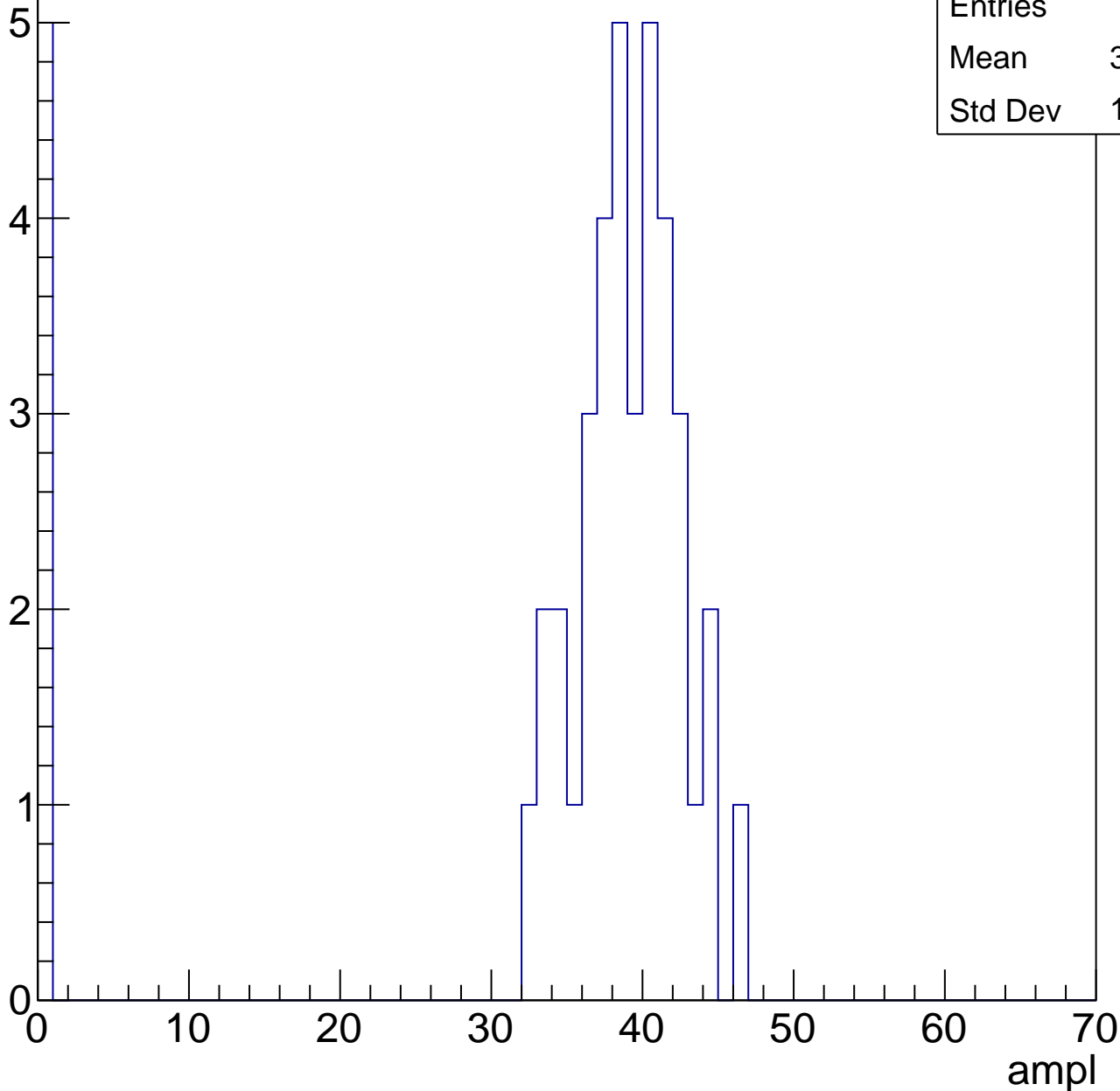


B1L103S, U14-ch56, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	42
Mean	34.07
Std Dev	12.89

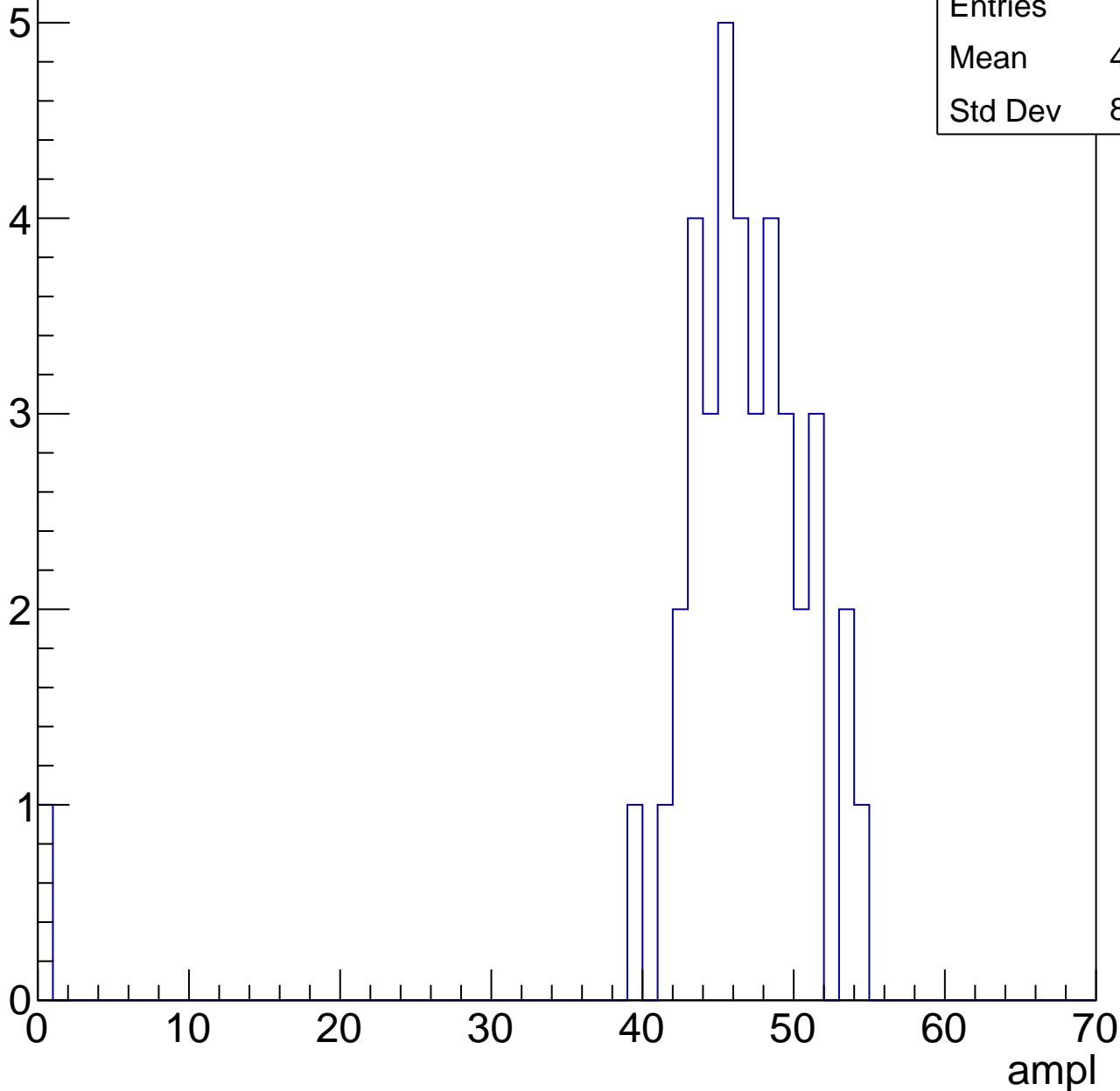


B1L103S, U14-ch56, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	45.38
Std Dev	8.126

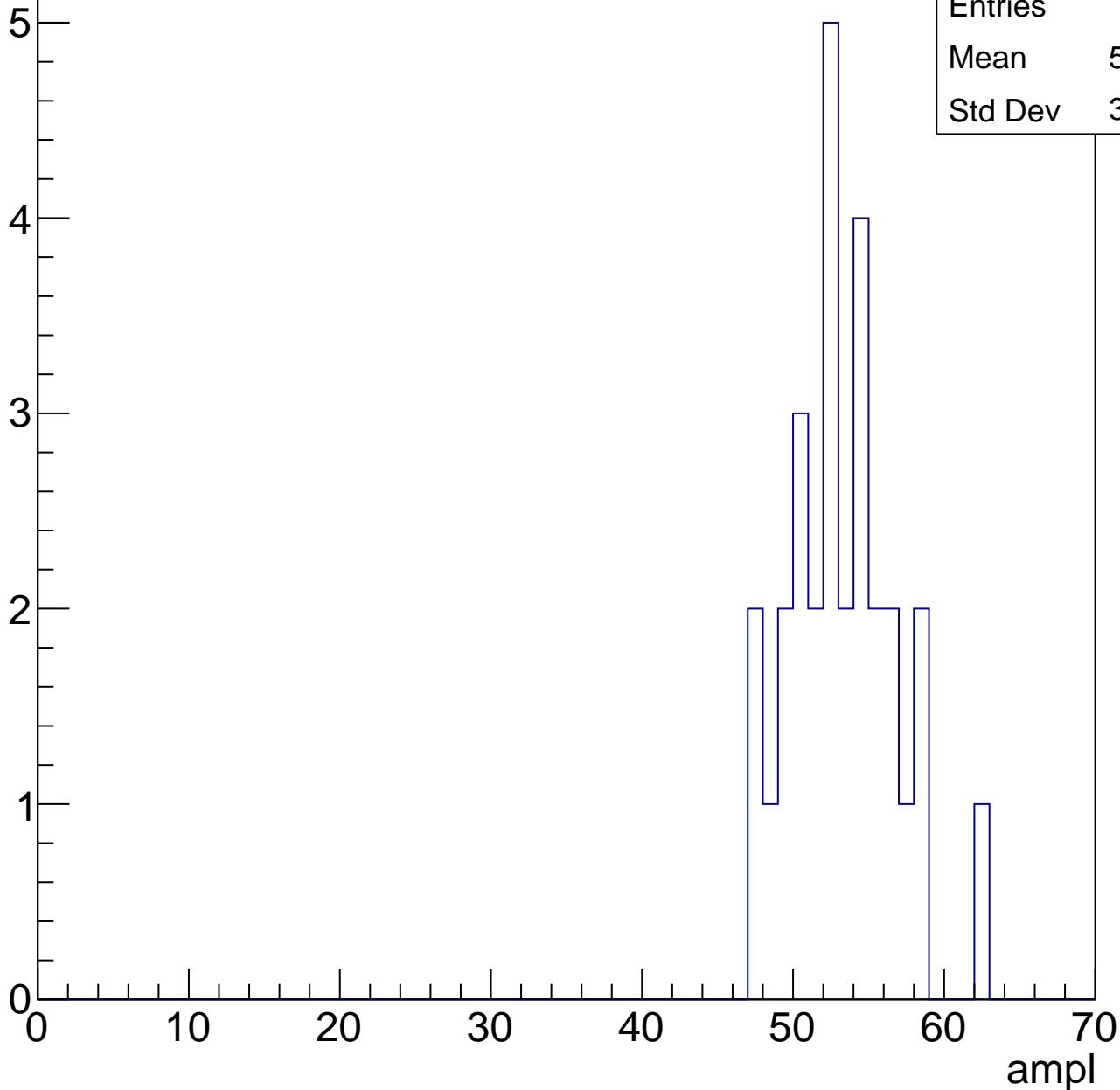


B1L103S, U14-ch56, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	29
Mean	52.79
Std Dev	3.448

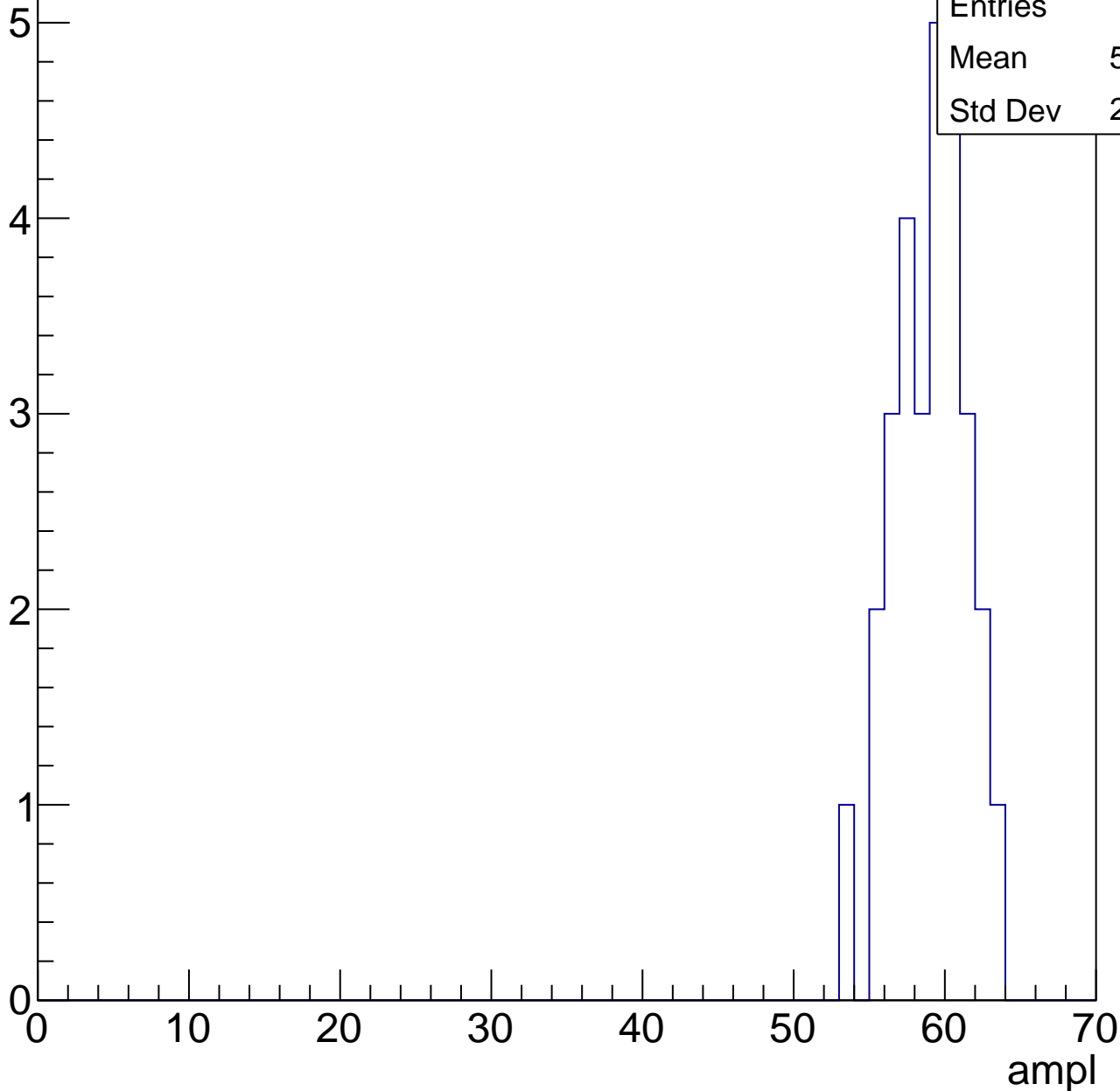


B1L103S, U14-ch56, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	29
Mean	58.55
Std Dev	2.343



B1L103S, U14-ch56, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	6
Mean	60.67
Std Dev	2.625

0 10 20 30 40 50 60 70

ampl

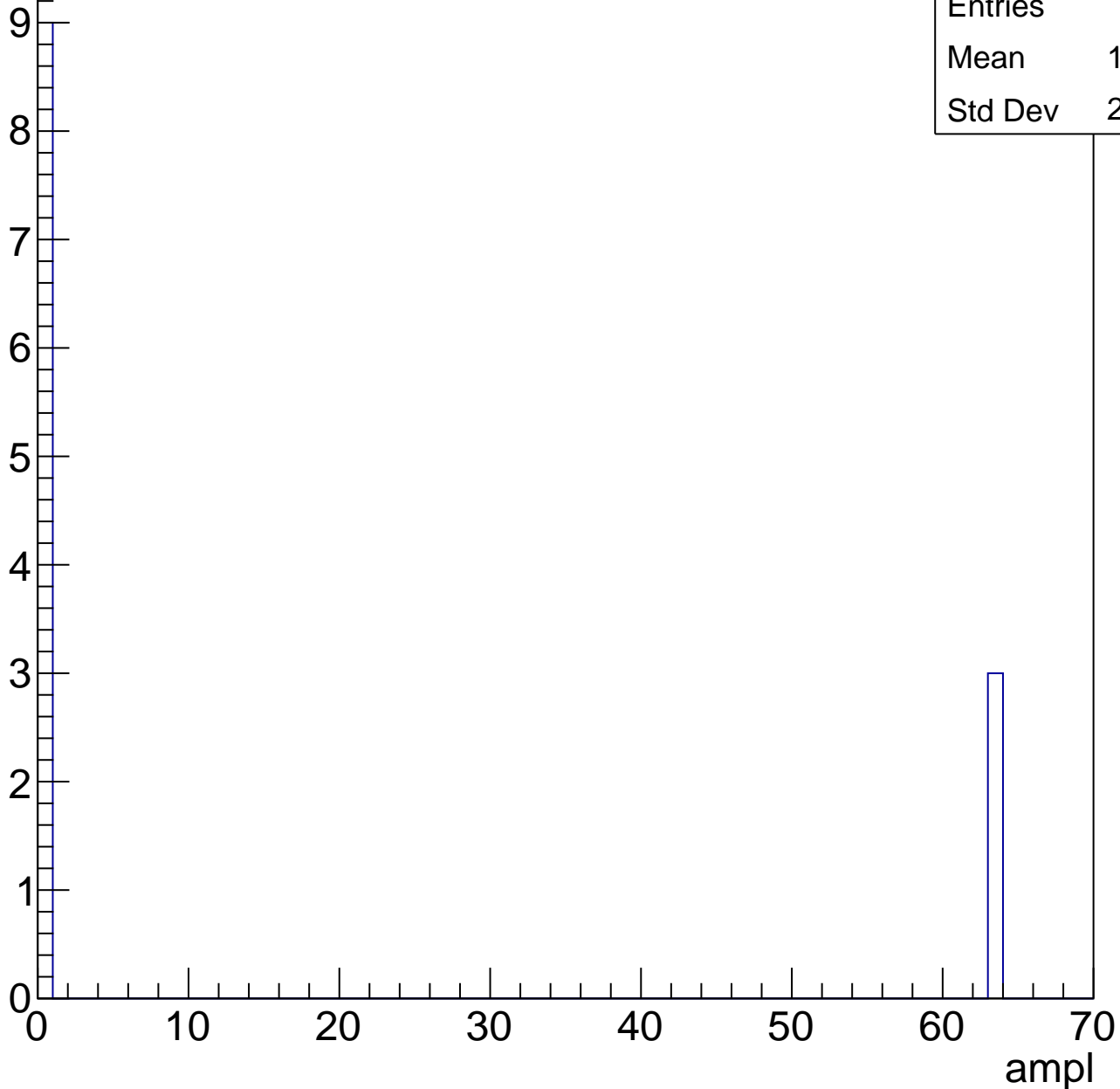
55 60 65

B1L103S, U14-ch56, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	12
Mean	15.75
Std Dev	27.28

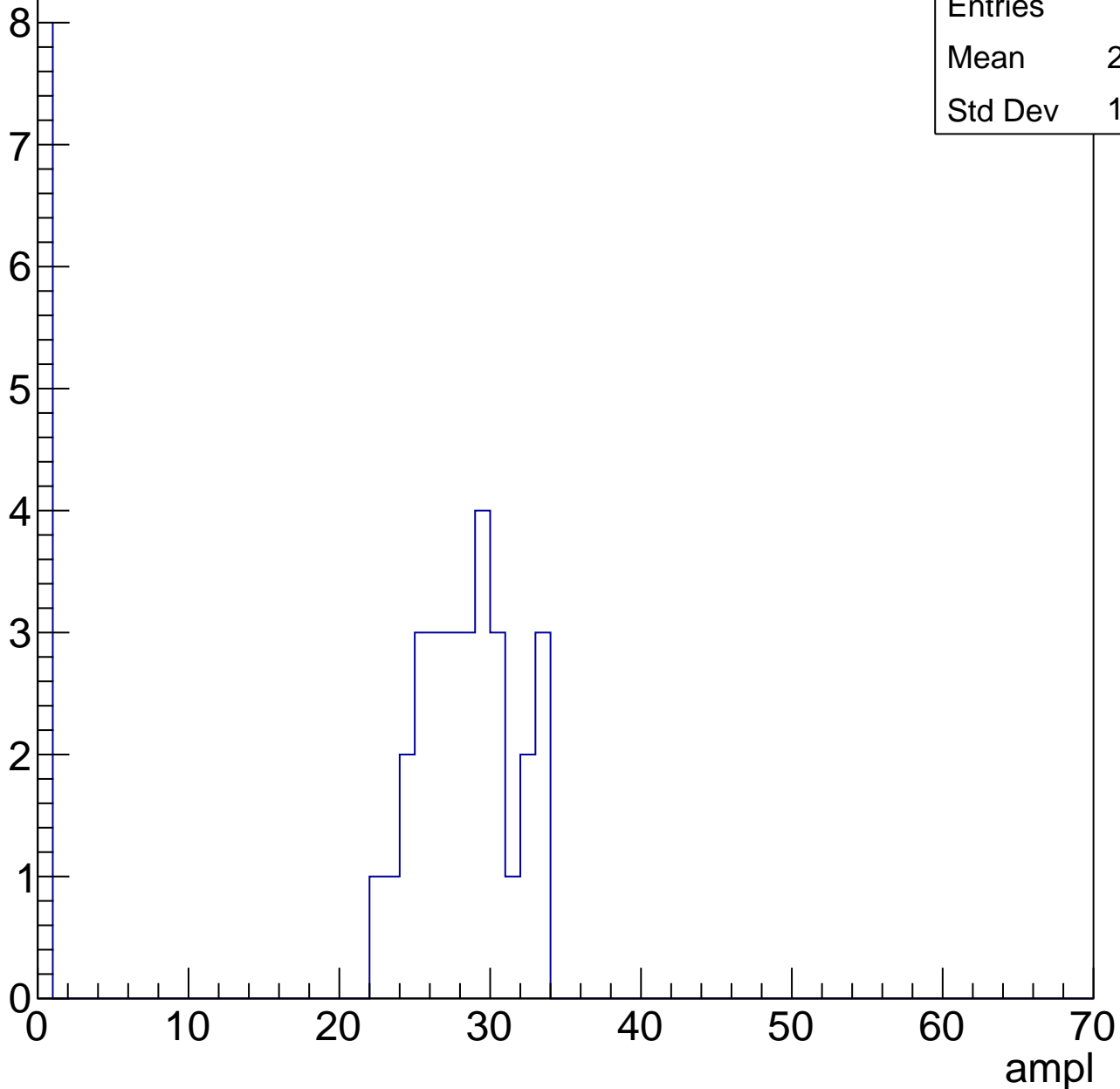


B1L103S, U14-ch57, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	37
Mean	21.92
Std Dev	11.82

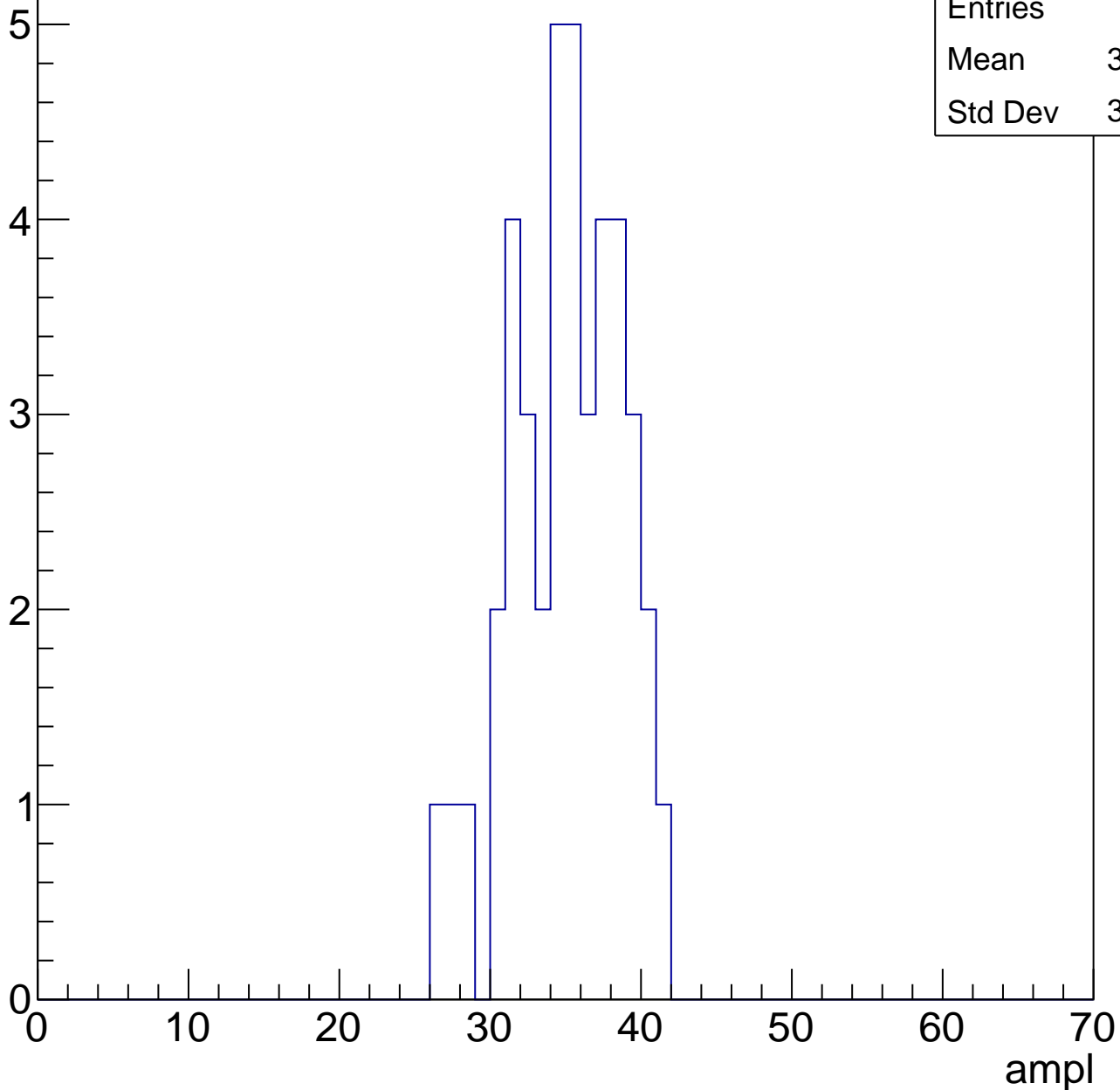


B1L103S, U14-ch57, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	41
Mean	34.59
Std Dev	3.595

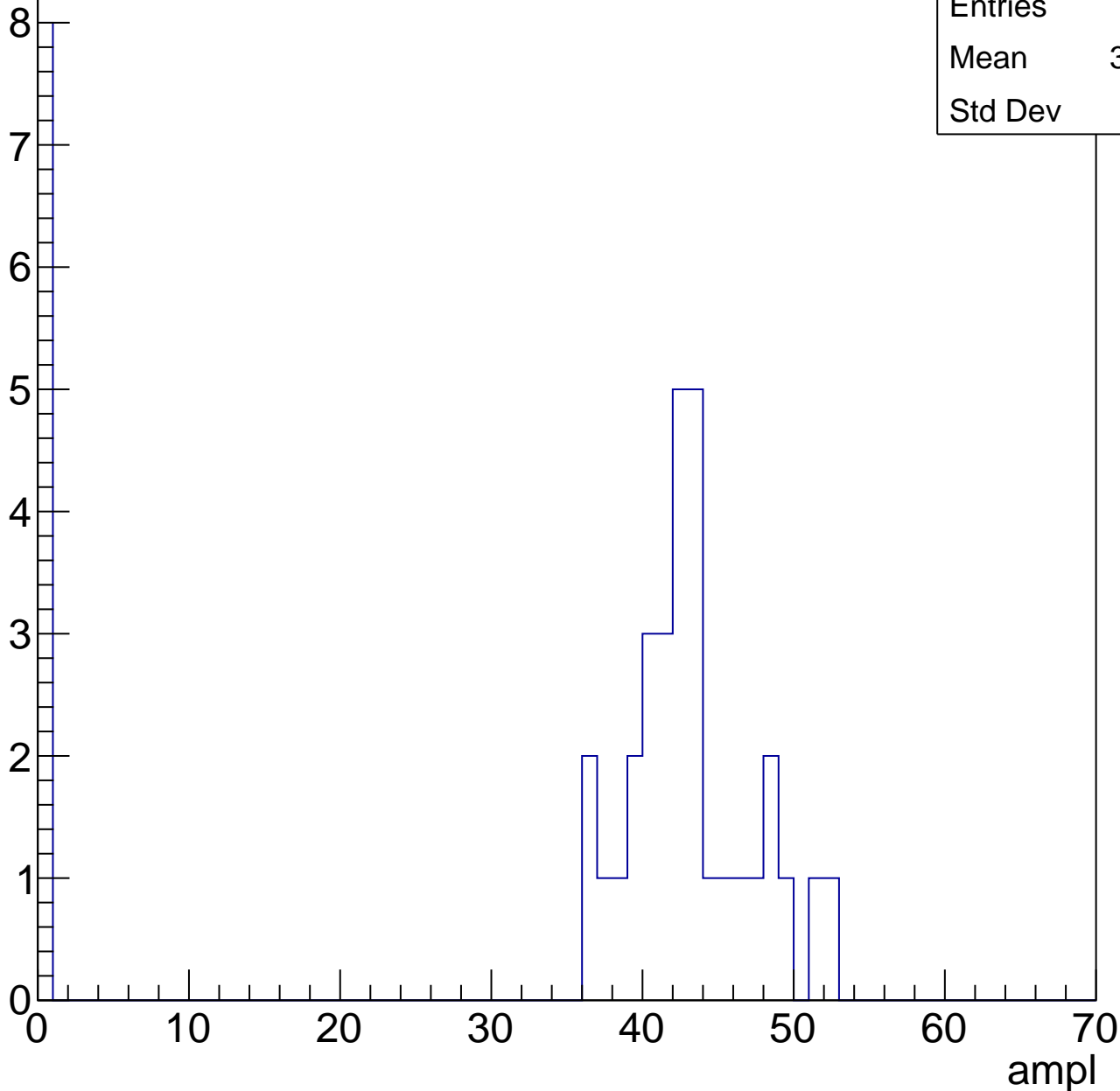


B1L103S, U14-ch57, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

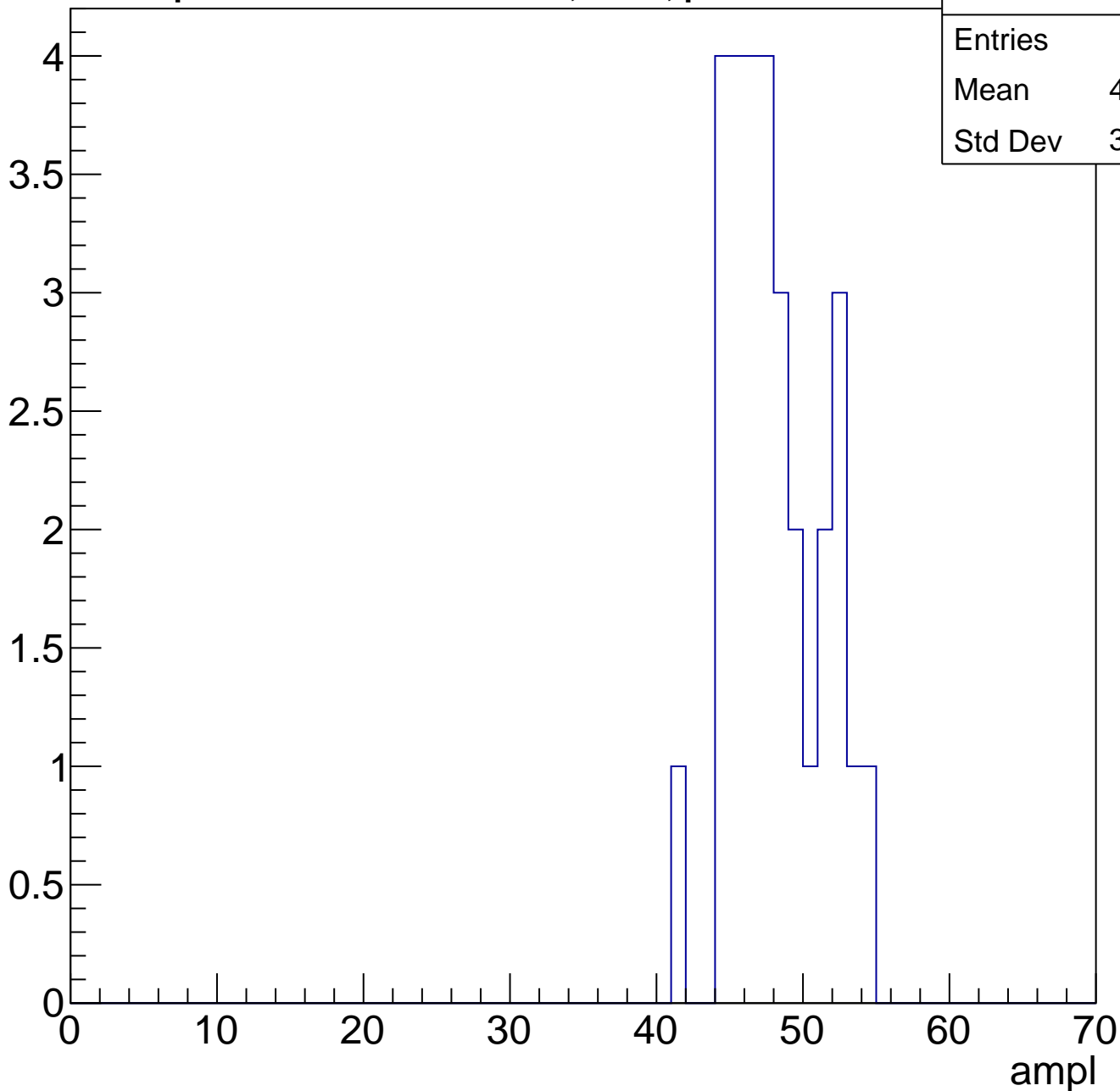
Entries	39
Mean	33.92
Std Dev	17.6



B1L103S, U14-ch57, adc3

calib_packv5_041523_1651.root, FC#0, port C2

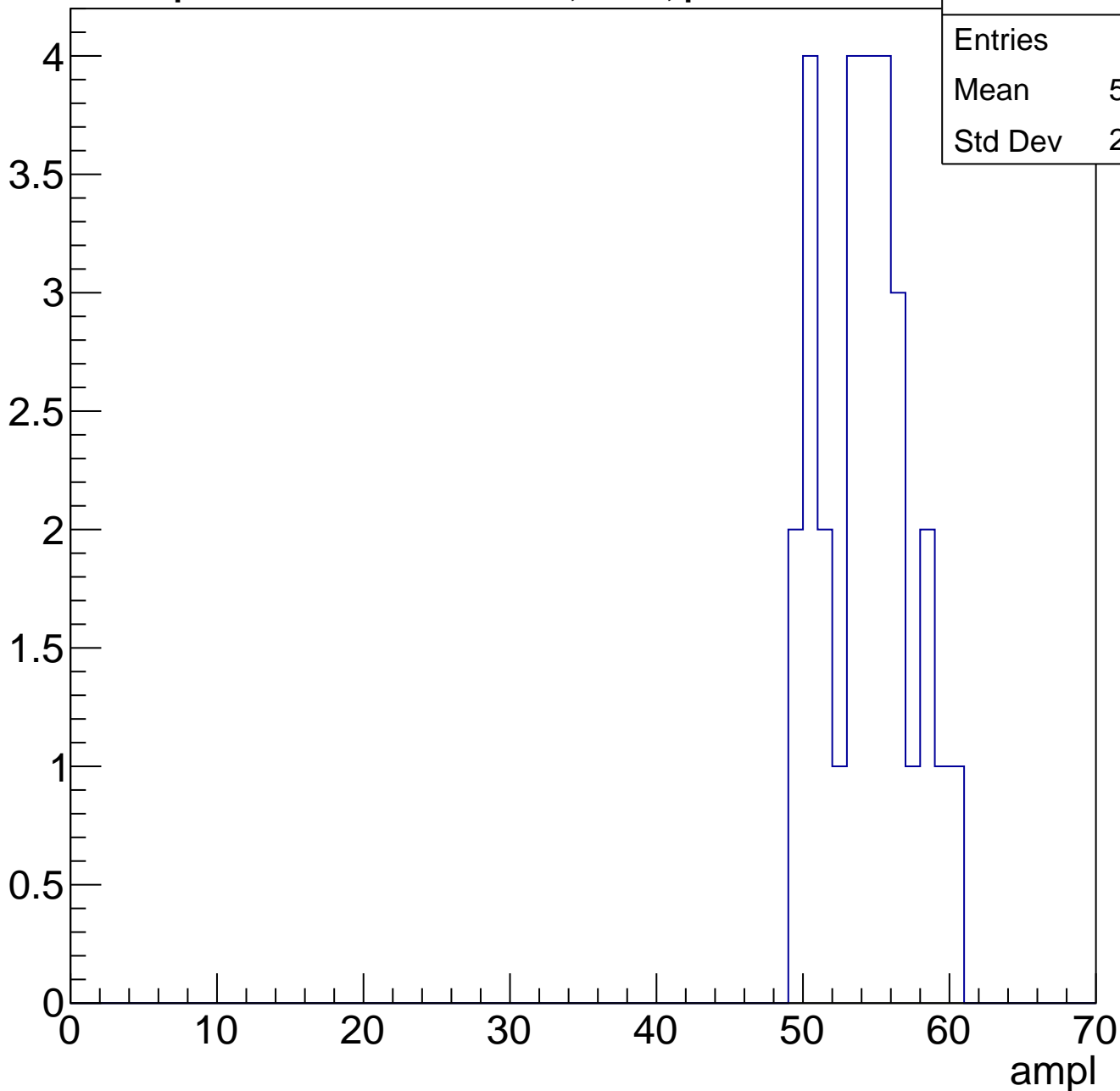
Entry



B1L103S, U14-ch57, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

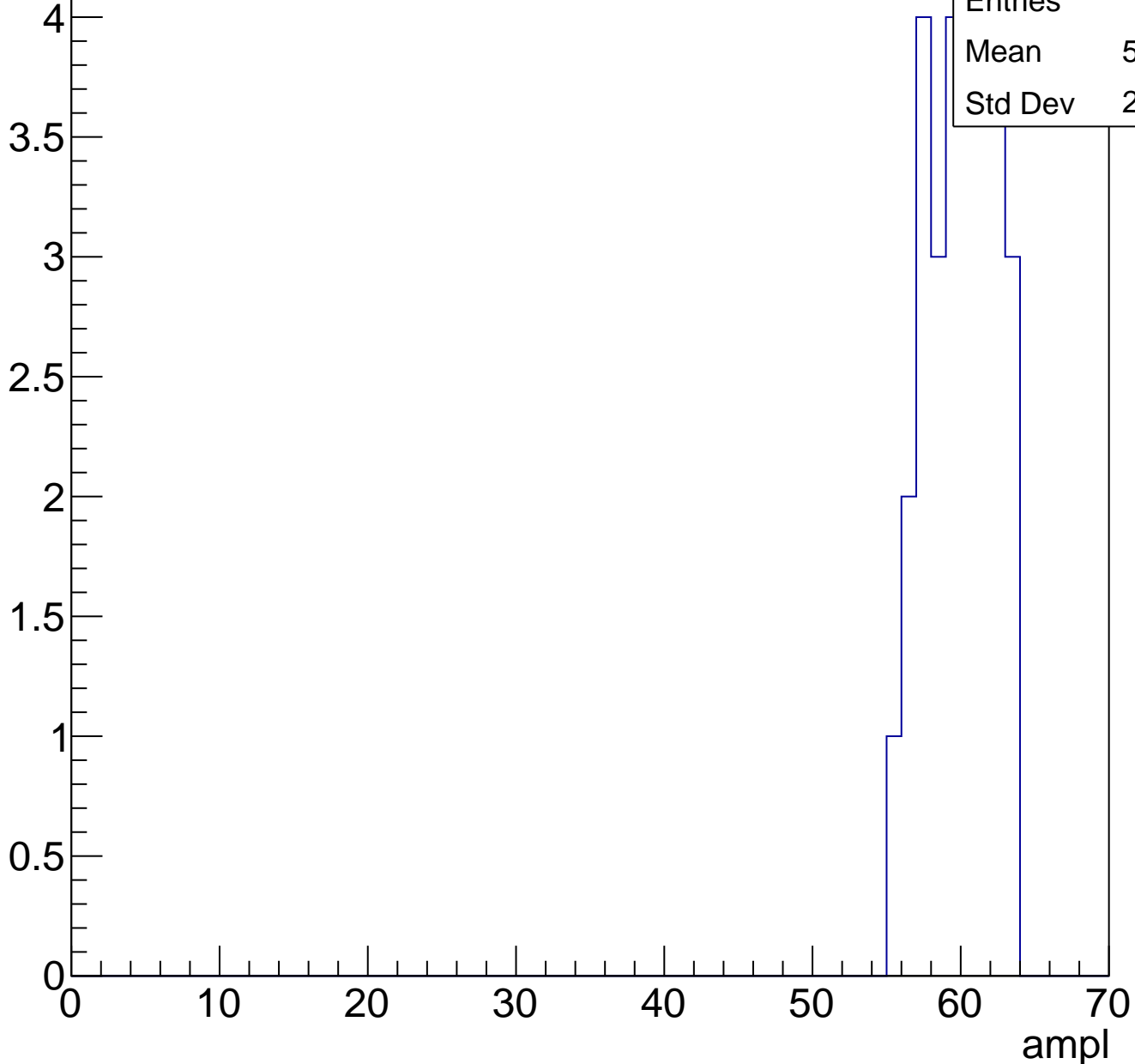


Entries	29
Mean	53.79
Std Dev	2.976

B1L103S, U14-ch57, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	29
Mean	59.52
Std Dev	2.269

B1L103S, U14-ch57, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

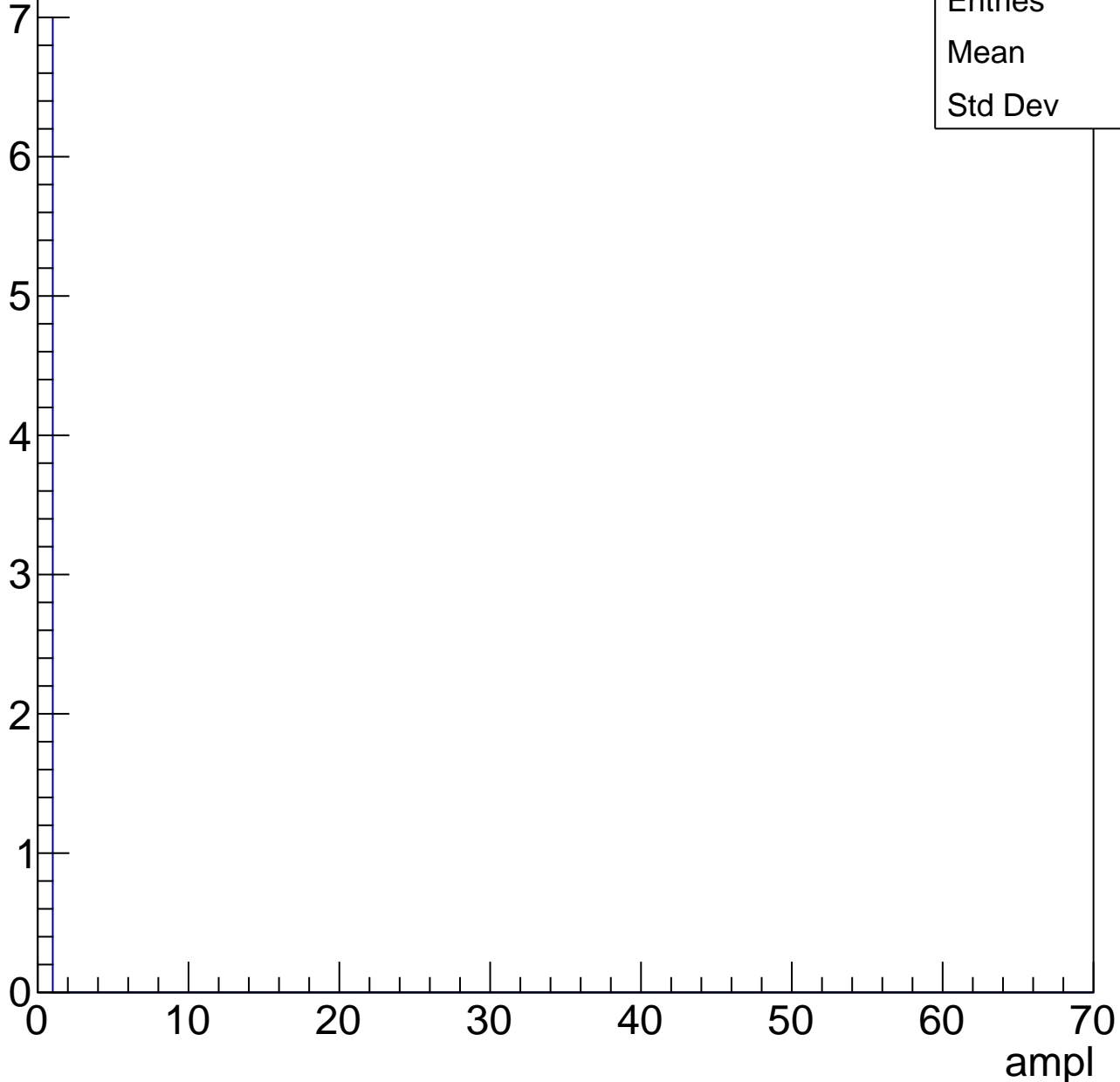


B1L103S, U14-ch57, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	7
Mean	0
Std Dev	0



B1L103S, U14-ch58, adc0

calib_packv5_041523_1651.root, FC#0, port C2

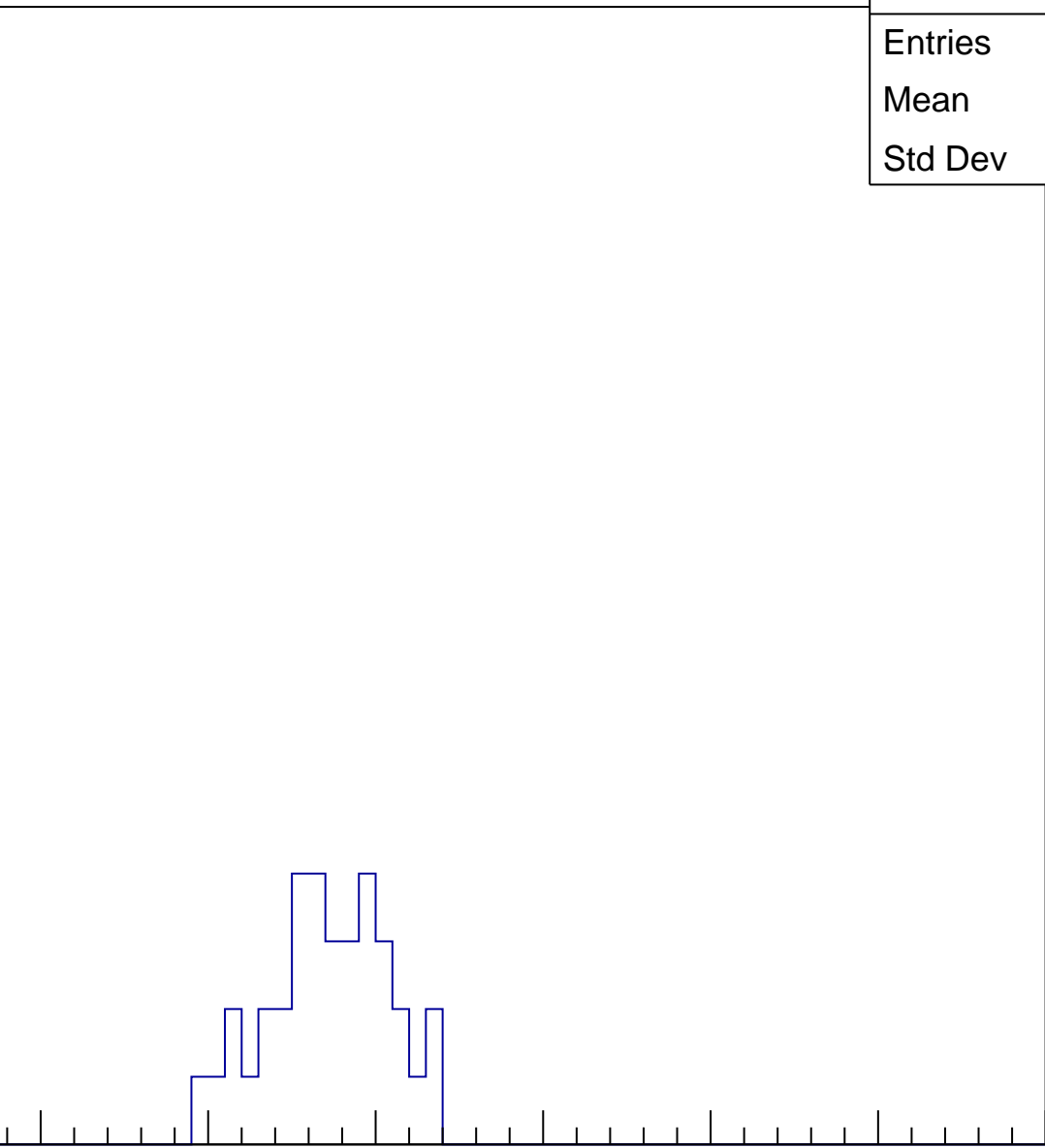
Entries	51
Mean	18.27
Std Dev	12.71

Entry

16
14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

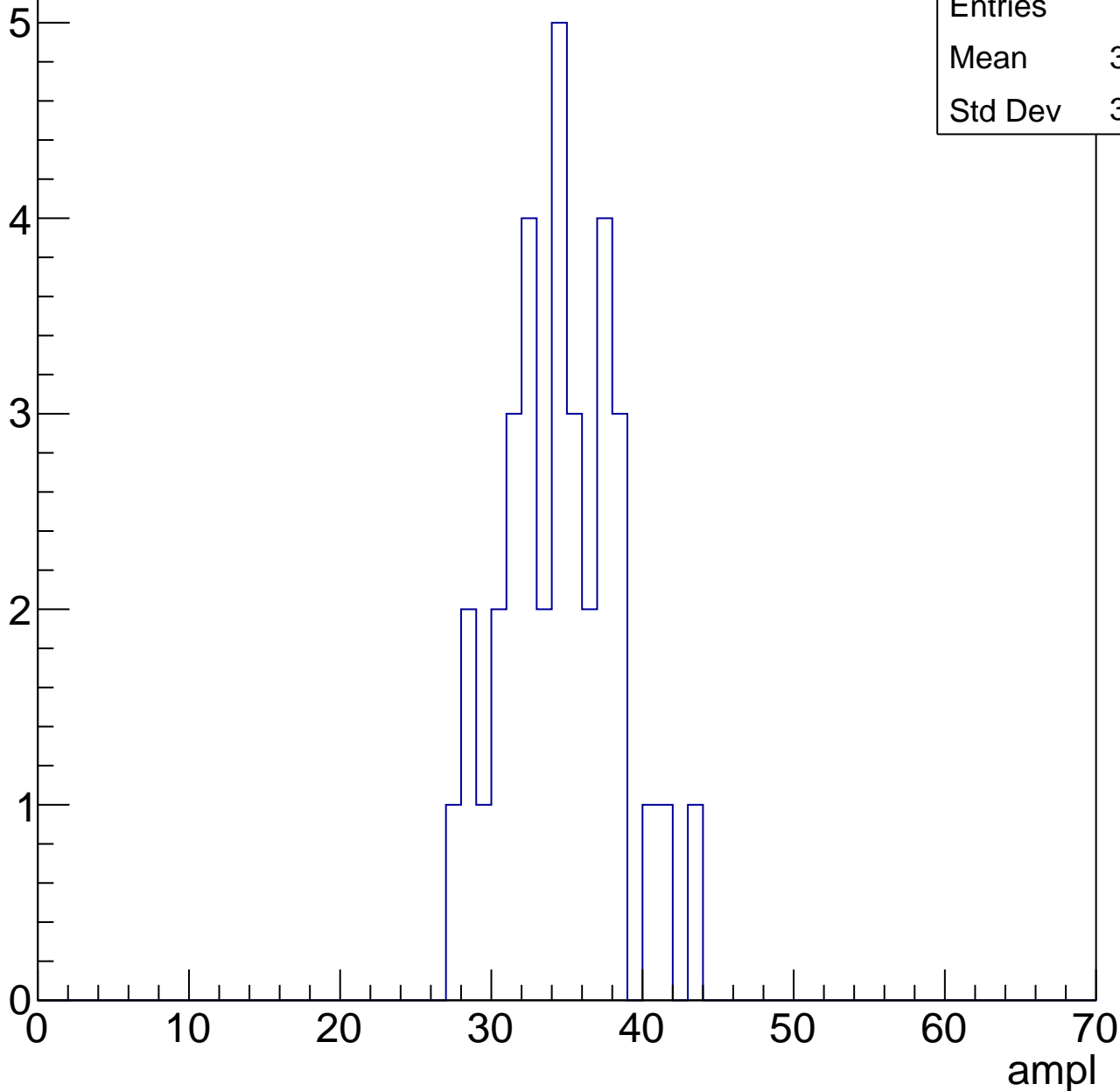


B1L103S, U14-ch58, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	35
Mean	34.06
Std Dev	3.718

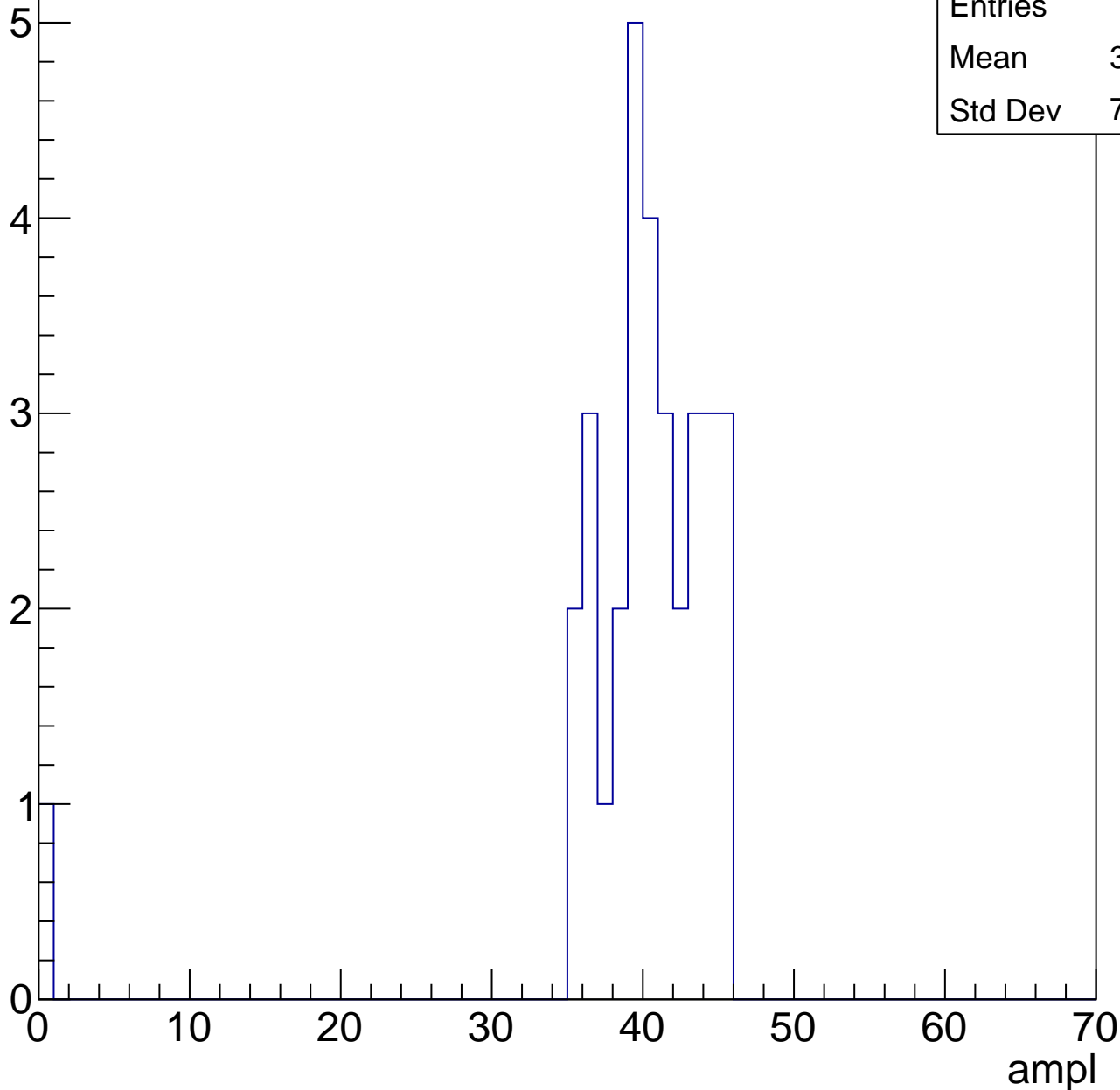


B1L103S, U14-ch58, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	32
Mean	39.03
Std Dev	7.605

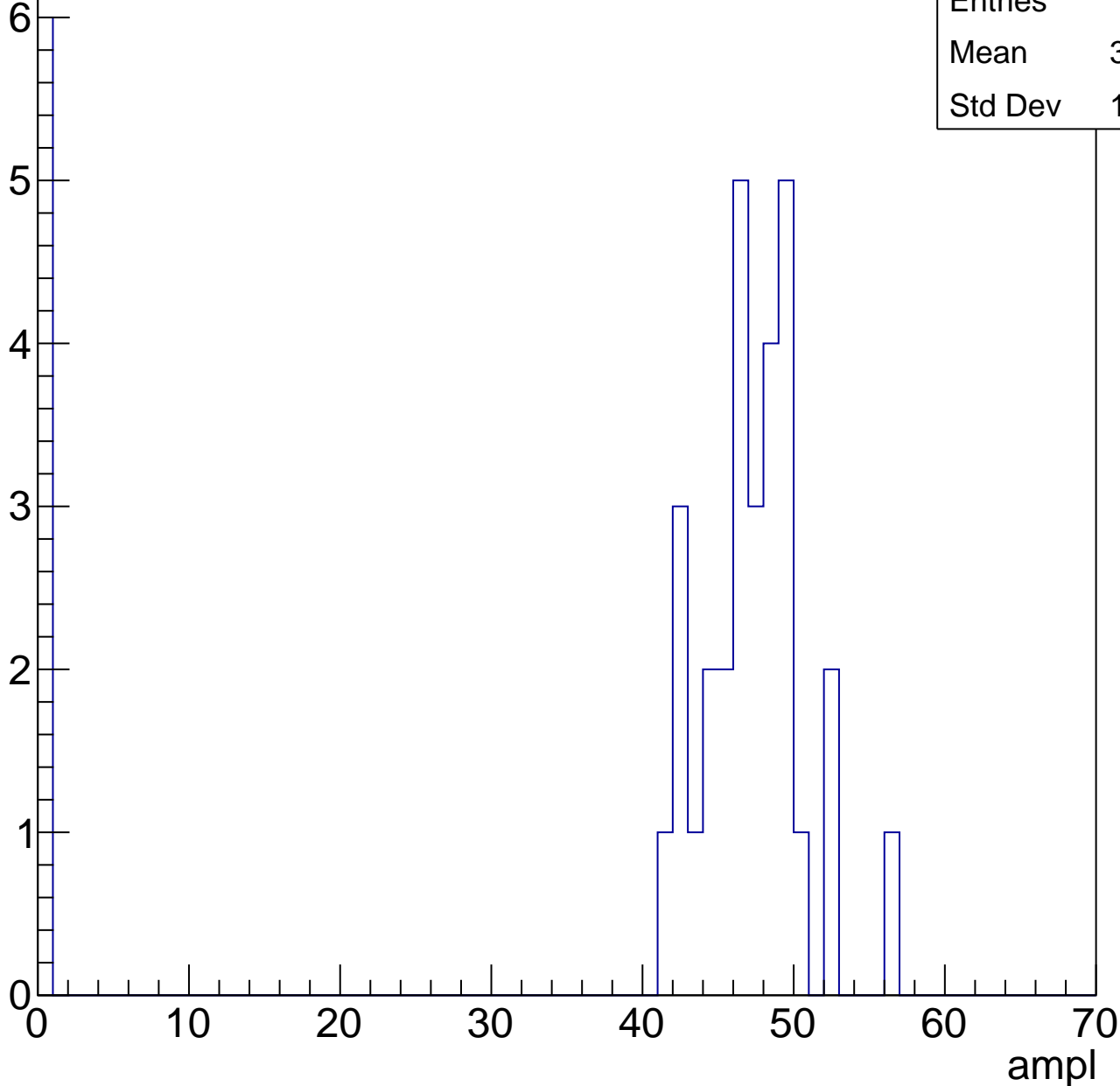


B1L103S, U14-ch58, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	36
Mean	39.06
Std Dev	17.72

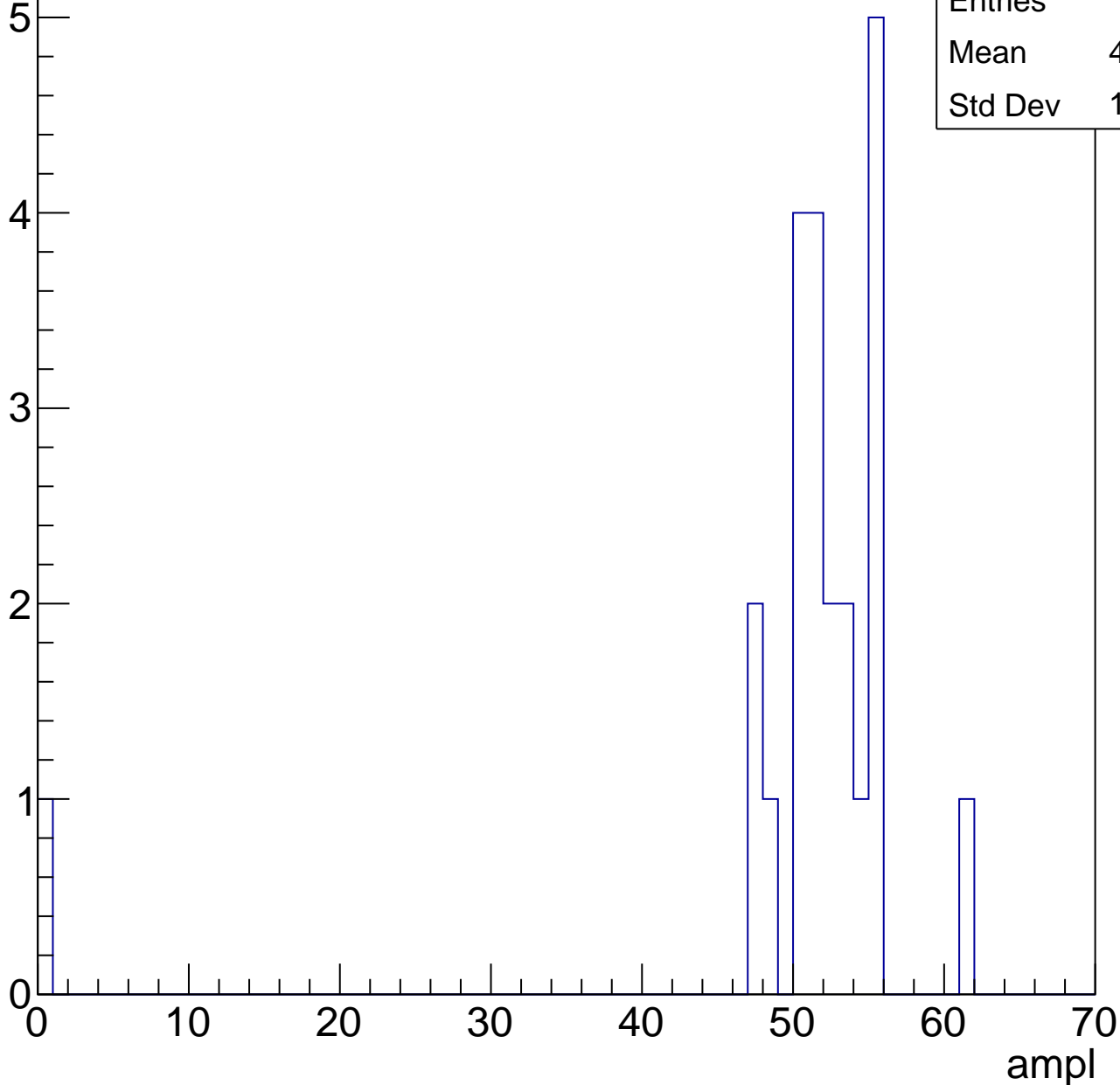


B1L103S, U14-ch58, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	23
Mean	49.83
Std Dev	11.06



B1L103S, U14-ch58, adc5

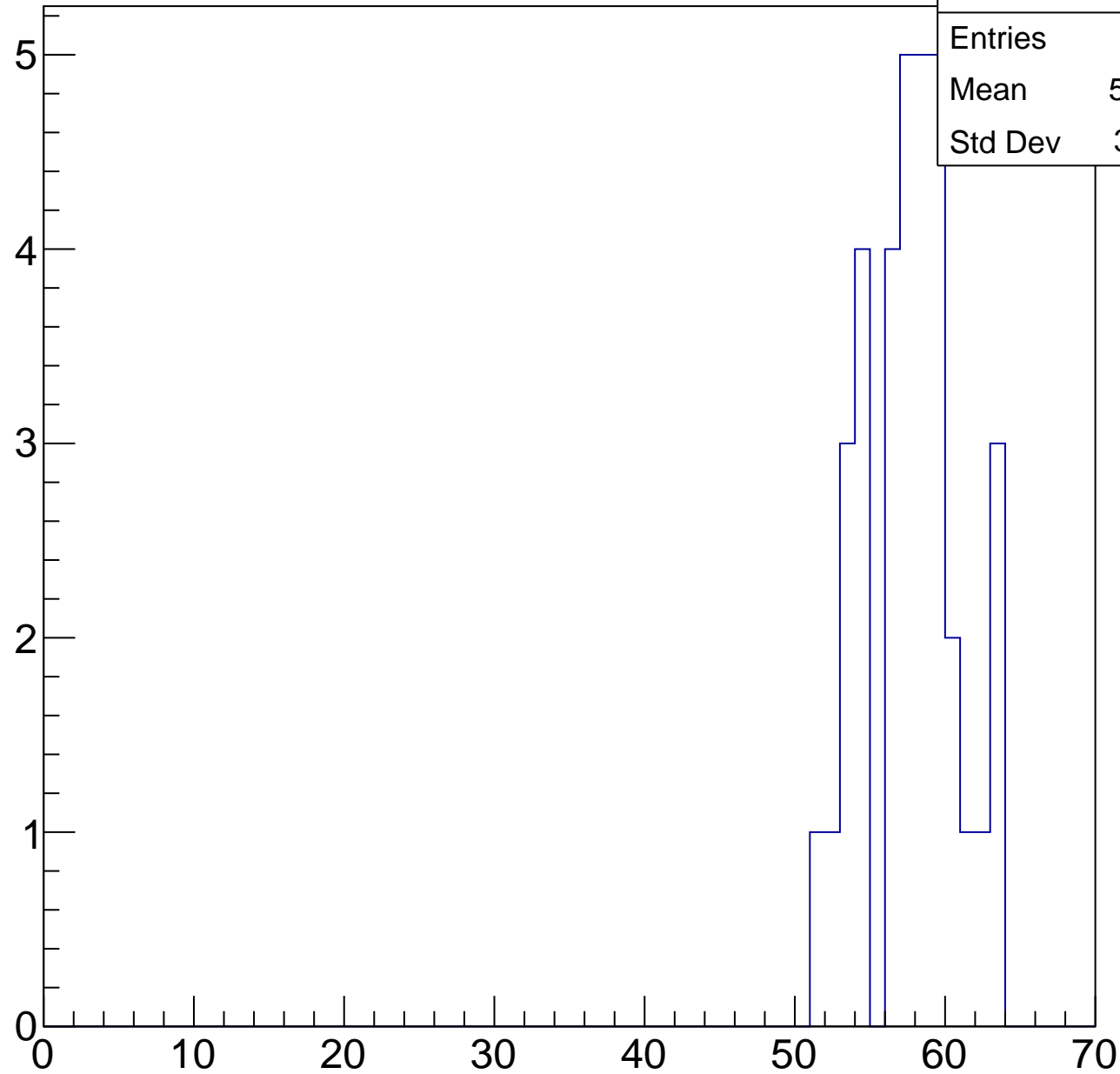
calib_packv5_041523_1651.root, FC#0, port C2

Entry

5
4
3
2
1
0

Entries	35
Mean	57.26
Std Dev	3.111

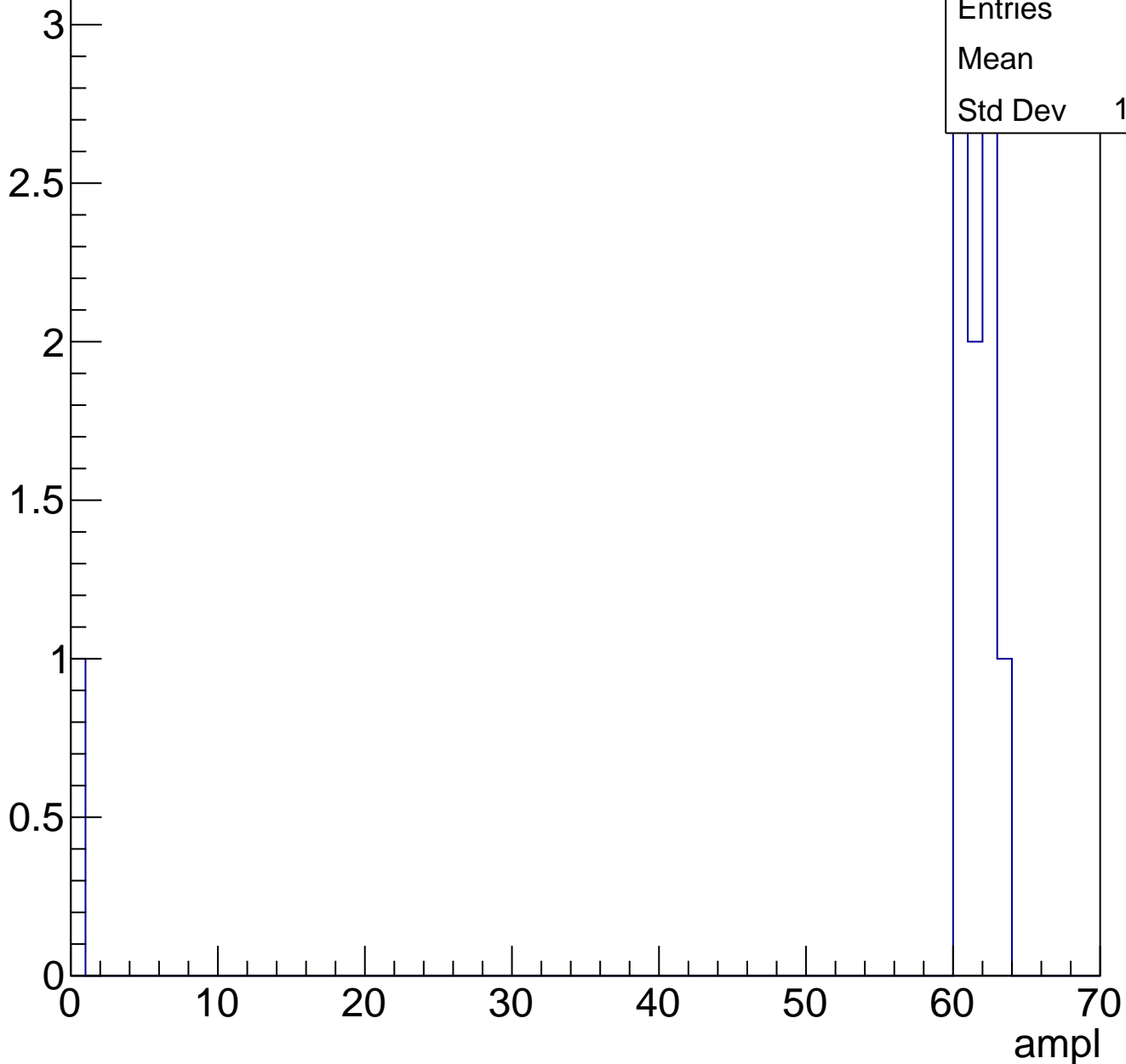
ampl



B1L103S, U14-ch58, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

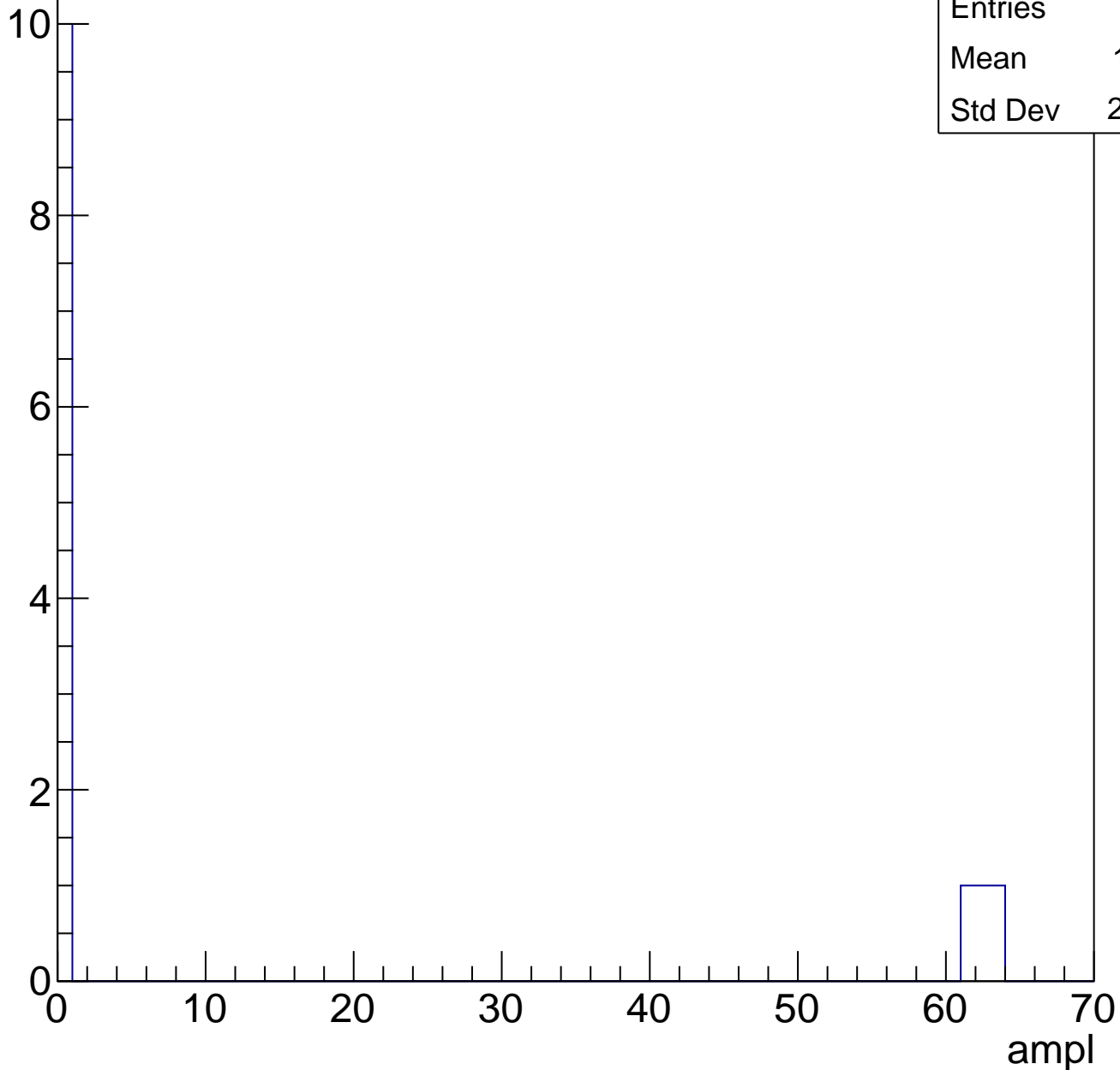


B1L103S, U14-ch58, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	13
Mean	14.31
Std Dev	26.13

Entry

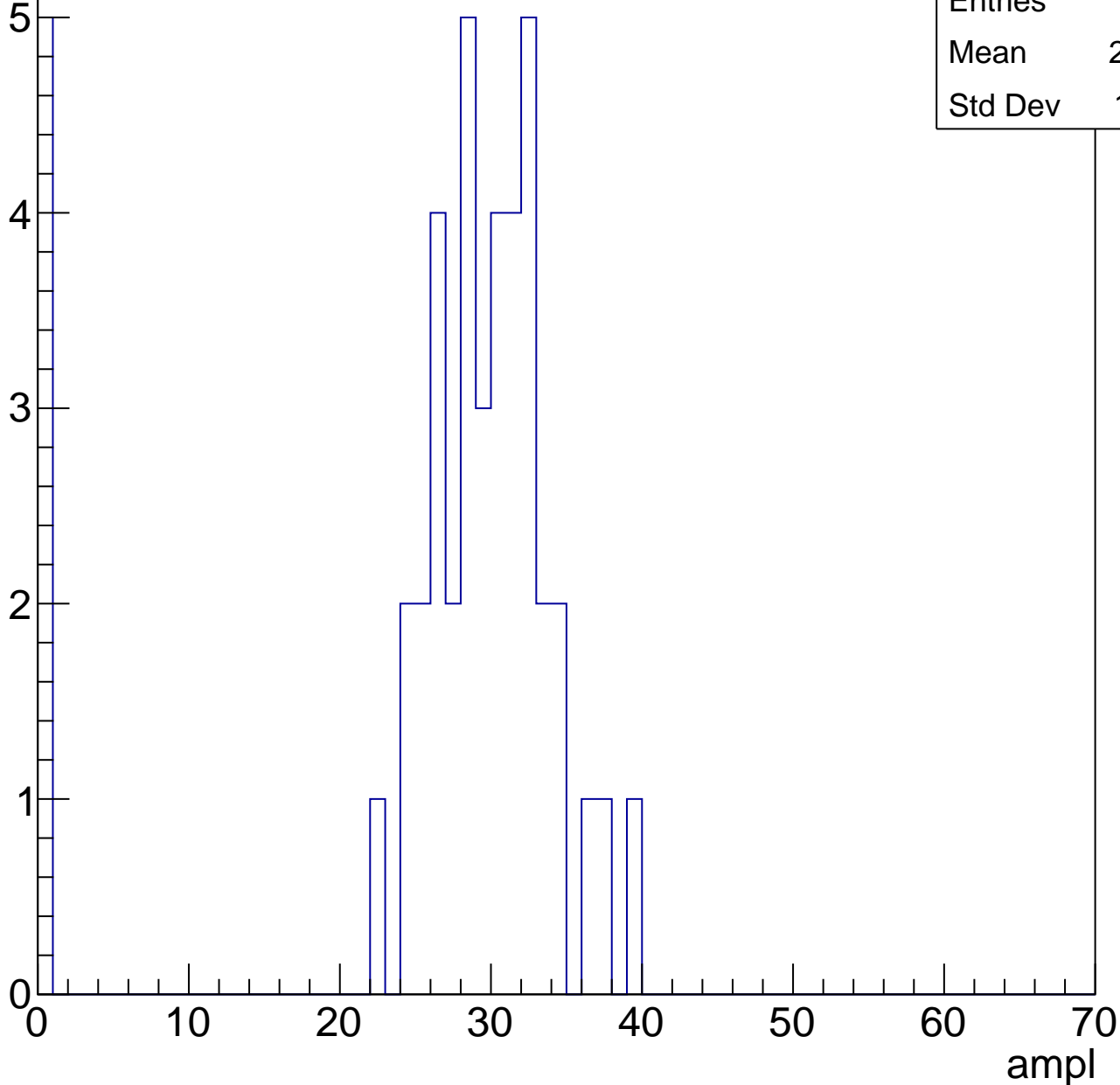


B1L103S, U14-ch59, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	44
Mean	26.25
Std Dev	10.01

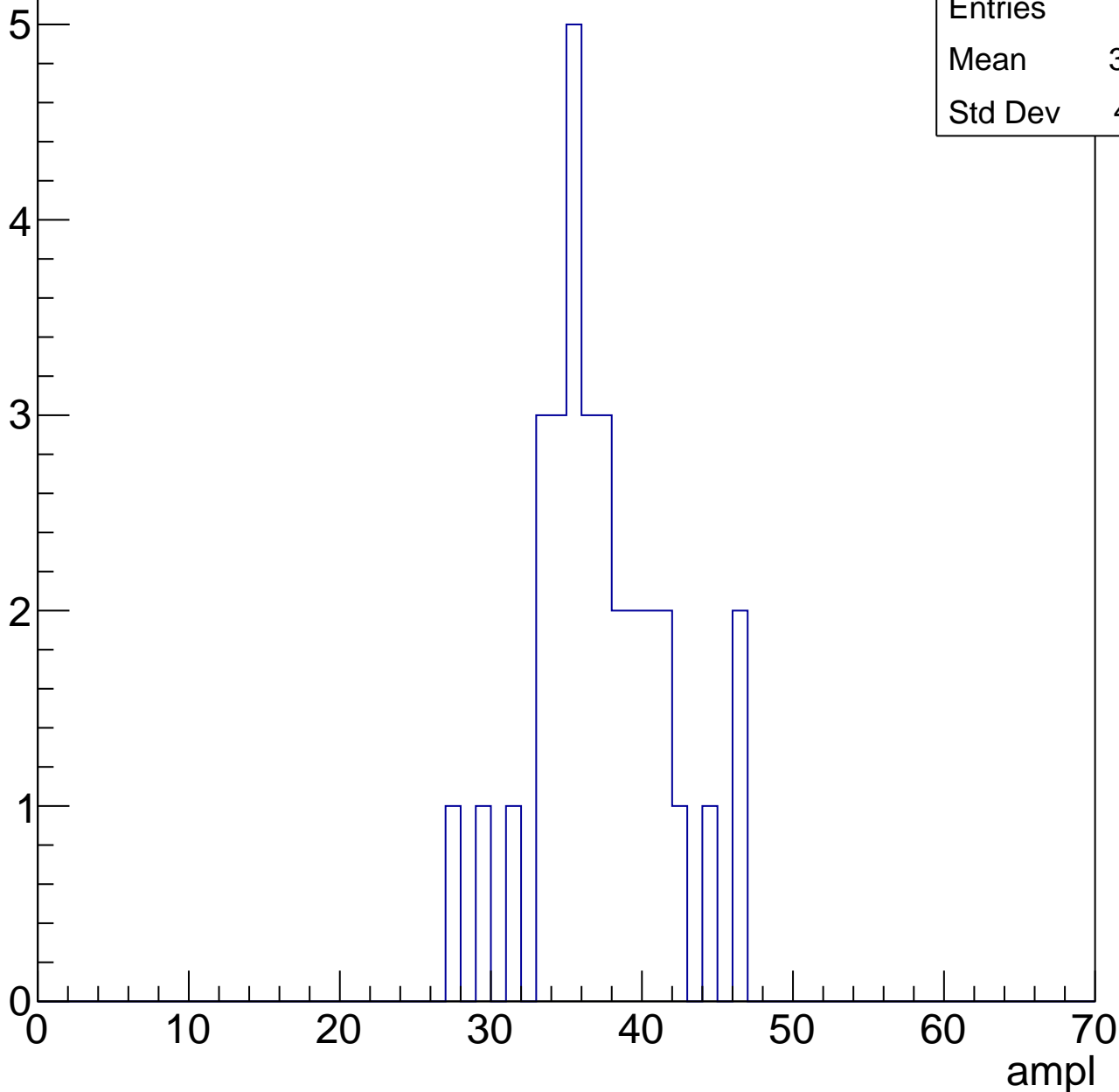


B1L103S, U14-ch59, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	32
Mean	36.75
Std Dev	4.301

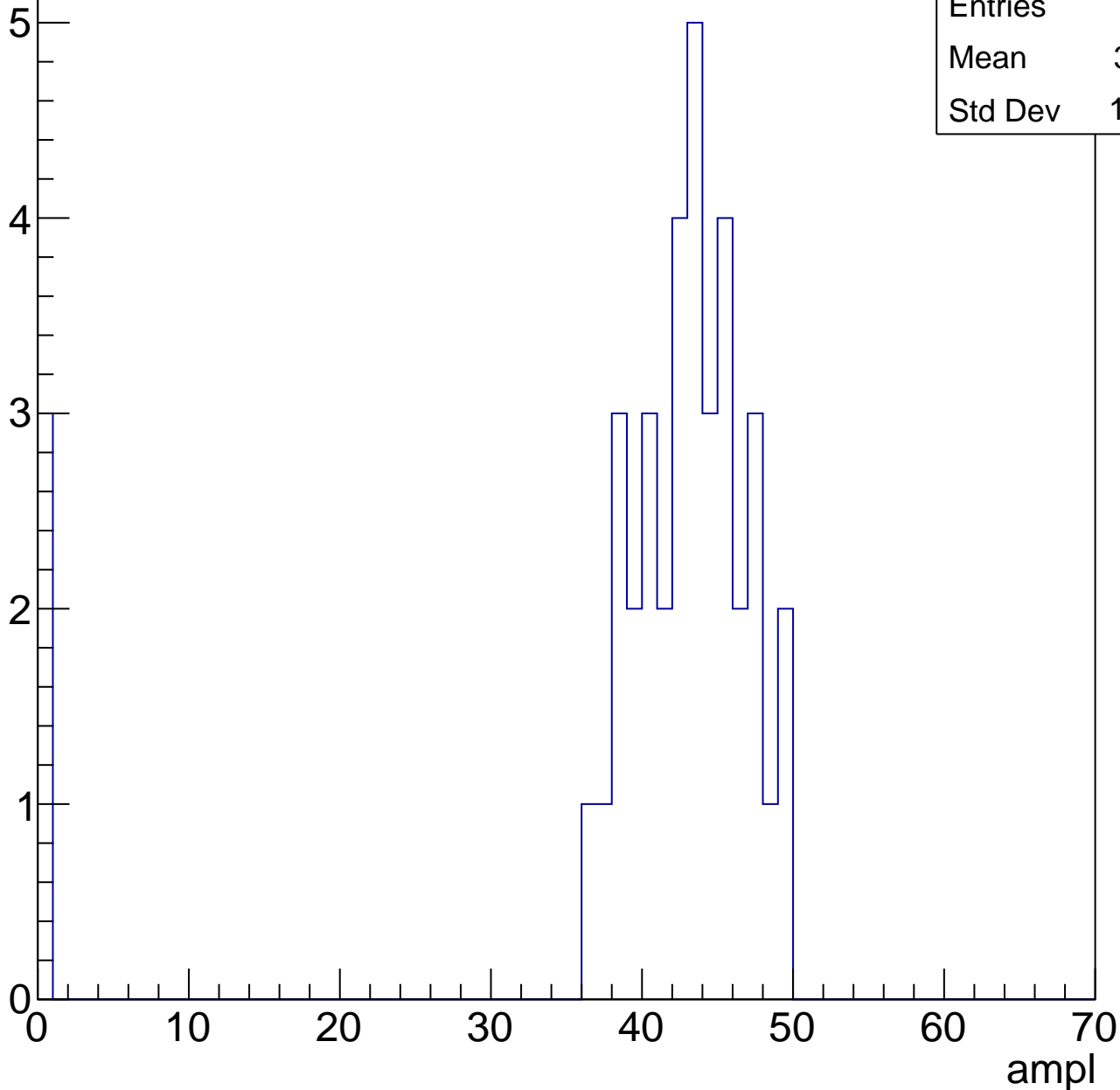


B1L103S, U14-ch59, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

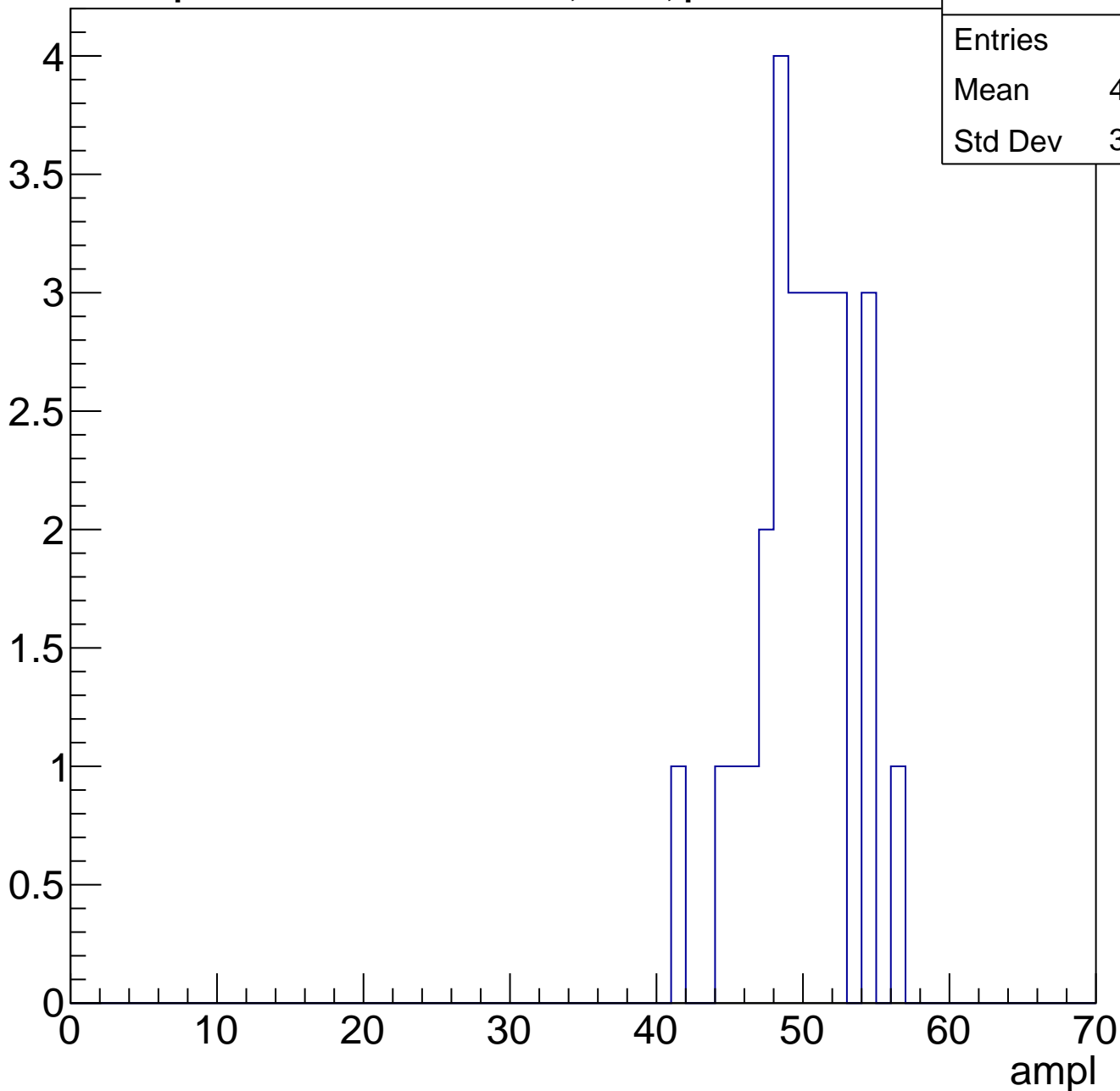
Entries	39
Mean	39.51
Std Dev	11.86



B1L103S, U14-ch59, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry



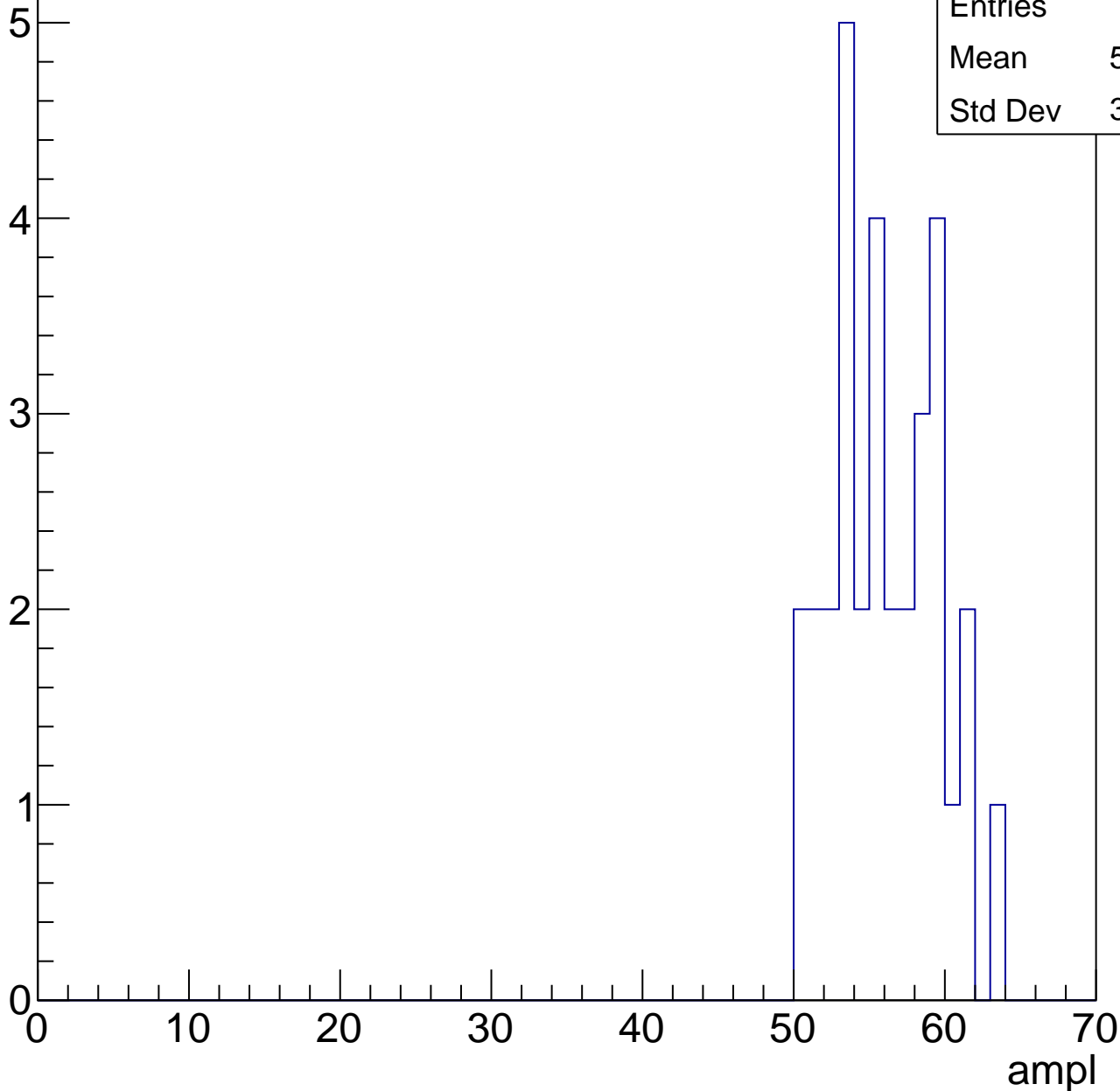
Entries	26
Mean	49.46
Std Dev	3.319

B1L103S, U14-ch59, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

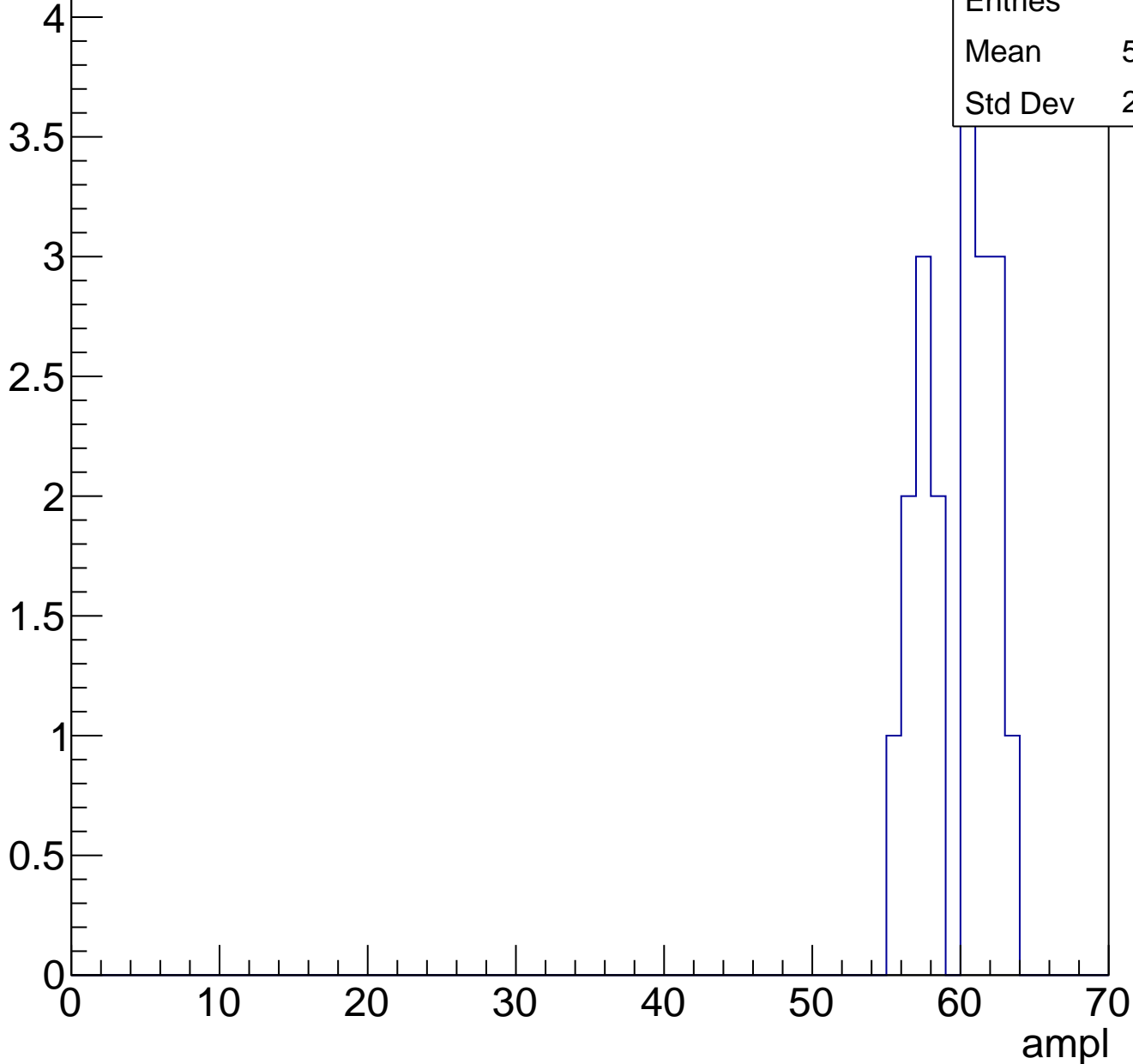
Entries	32
Mean	55.62
Std Dev	3.407



B1L103S, U14-ch59, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch59, adc6

calib_packv5_041523_1651.root, FC#0, port C2

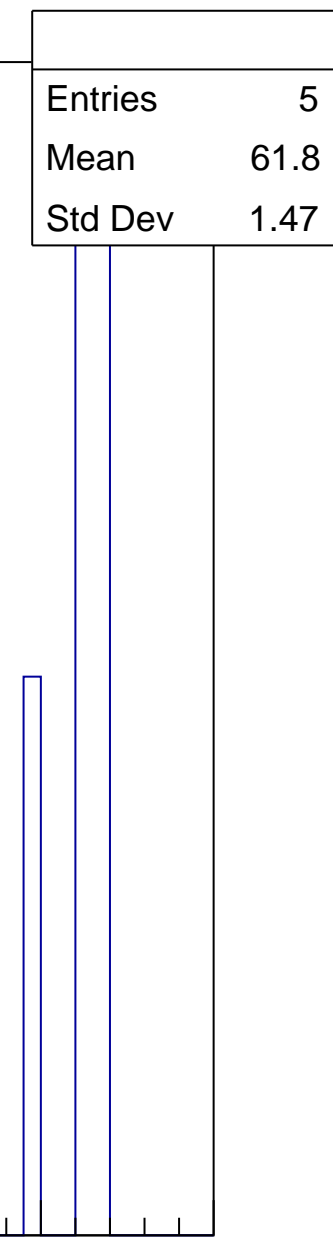
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	5
Mean	61.8
Std Dev	1.47

0 10 20 30 40 50 60 70

ampl



B1L103S, U14-ch59, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	14
Mean	4.5
Std Dev	16.22

Entry

12

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

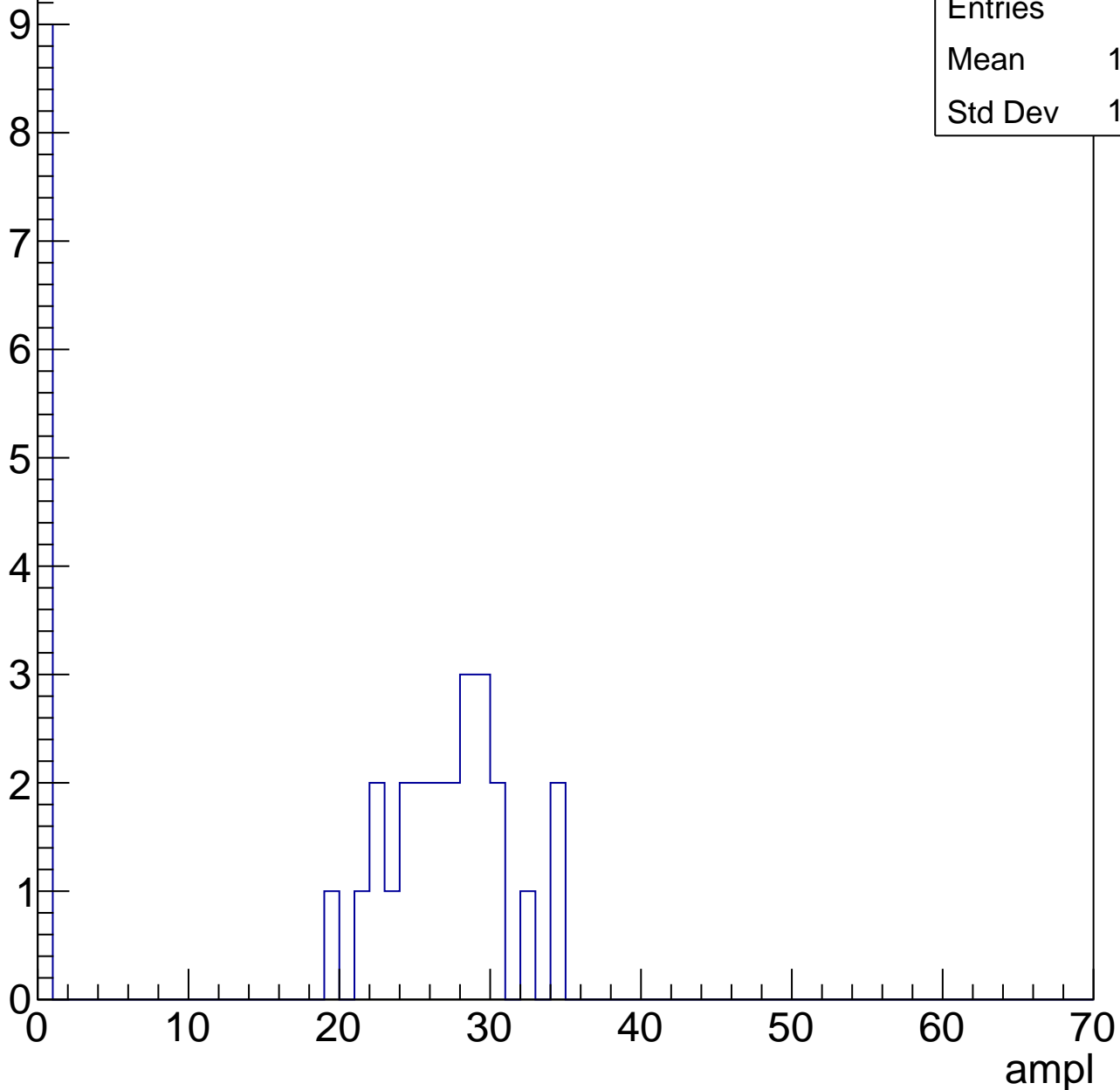
70

B1L103S, U14-ch60, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	33
Mean	19.45
Std Dev	12.35

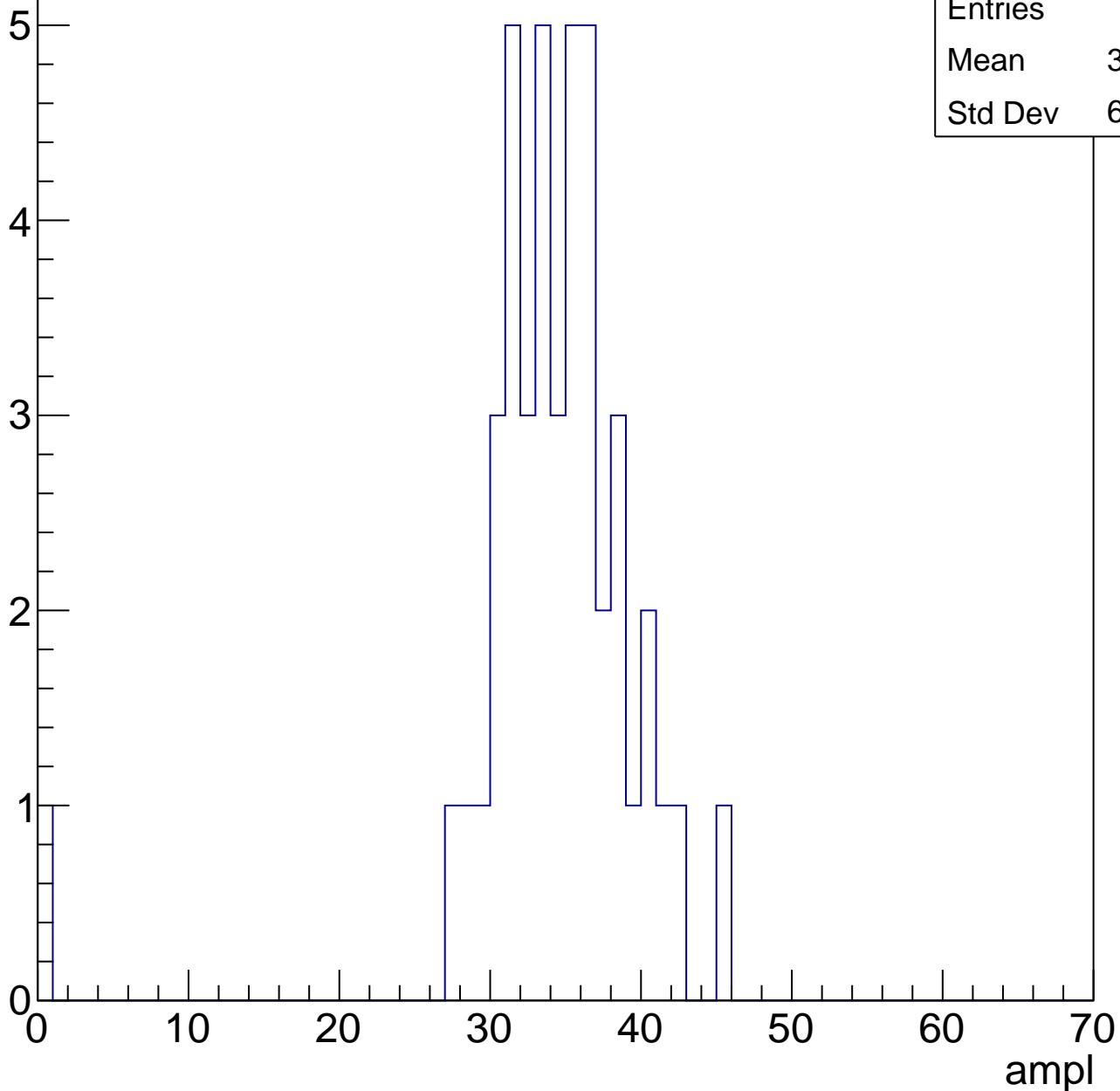


B1L103S, U14-ch60, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	44
Mean	33.68
Std Dev	6.385

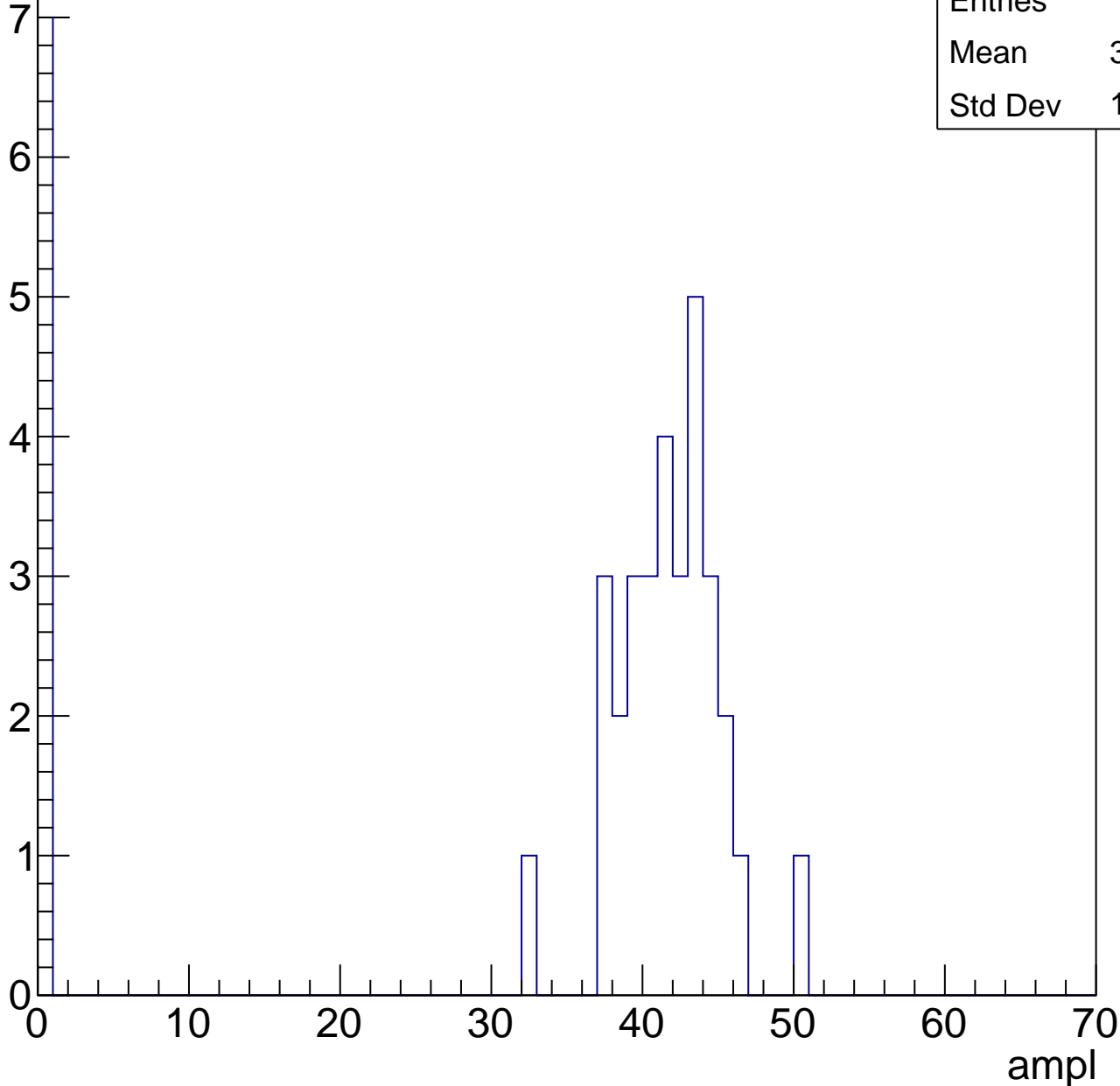


B1L103S, U14-ch60, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	38
Mean	33.66
Std Dev	16.28

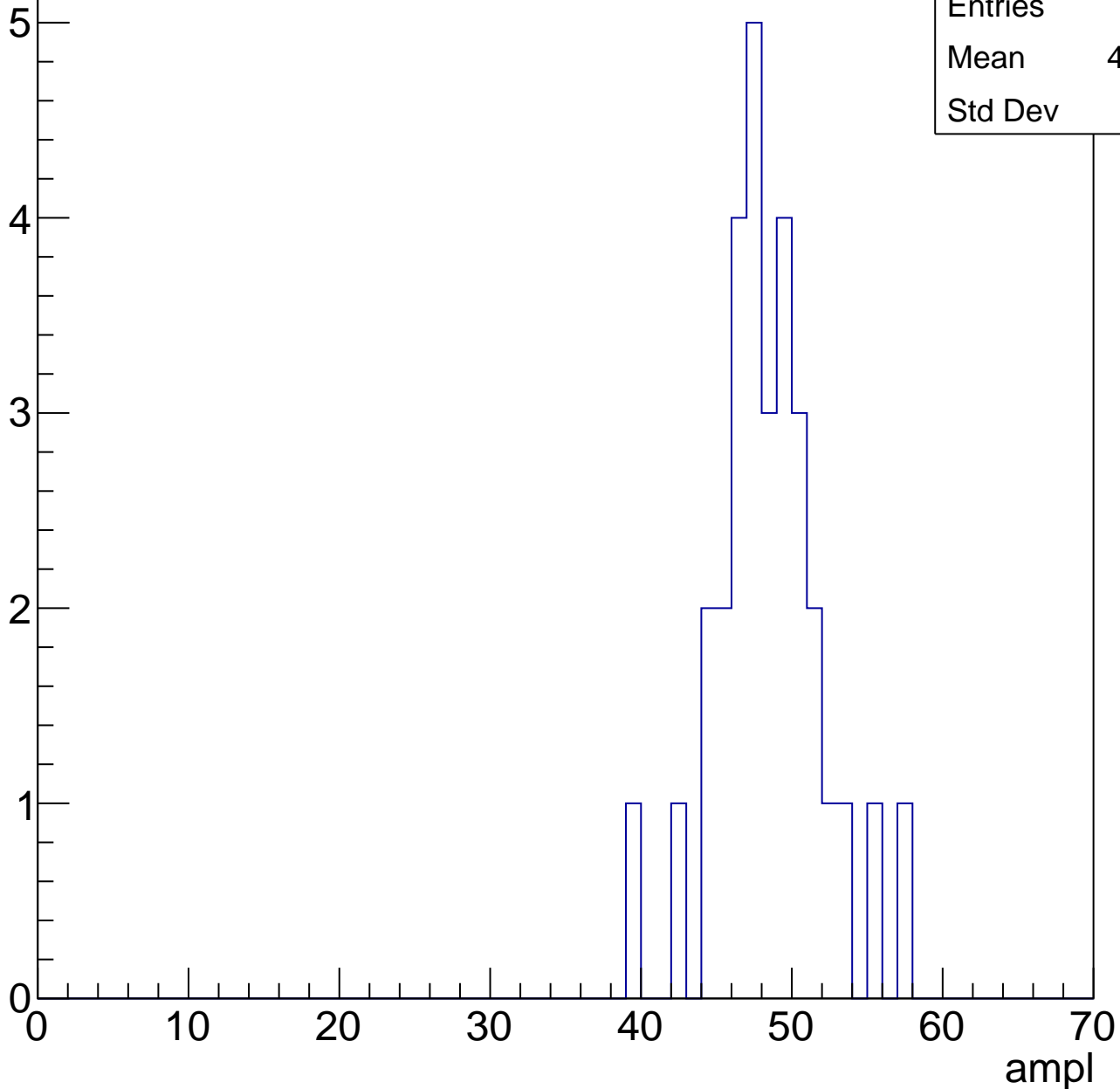


B1L103S, U14-ch60, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

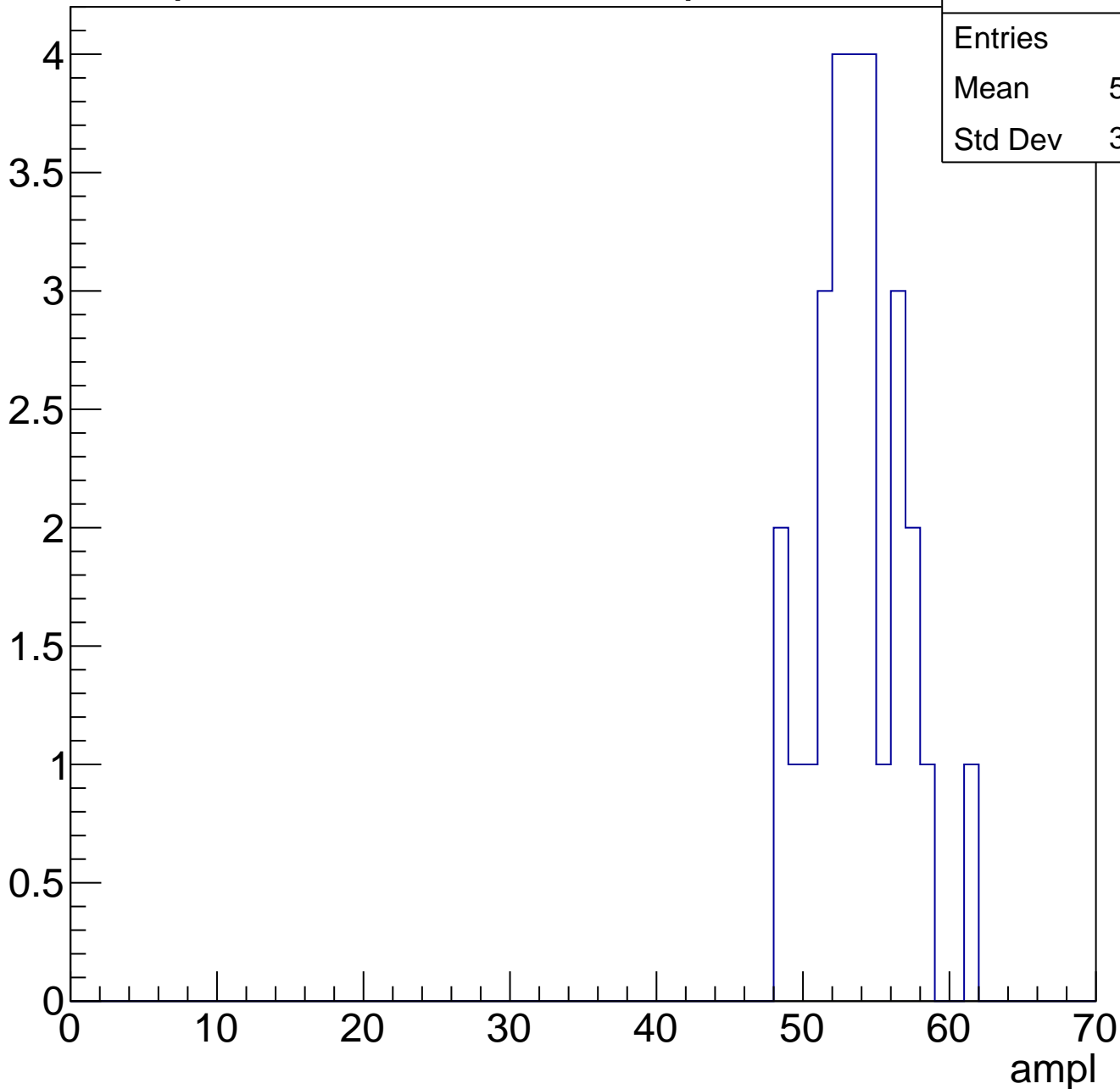
Entries	31
Mean	47.97
Std Dev	3.56



B1L103S, U14-ch60, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	27
Mean	53.33
Std Dev	3.006

B1L103S, U14-ch60, adc5

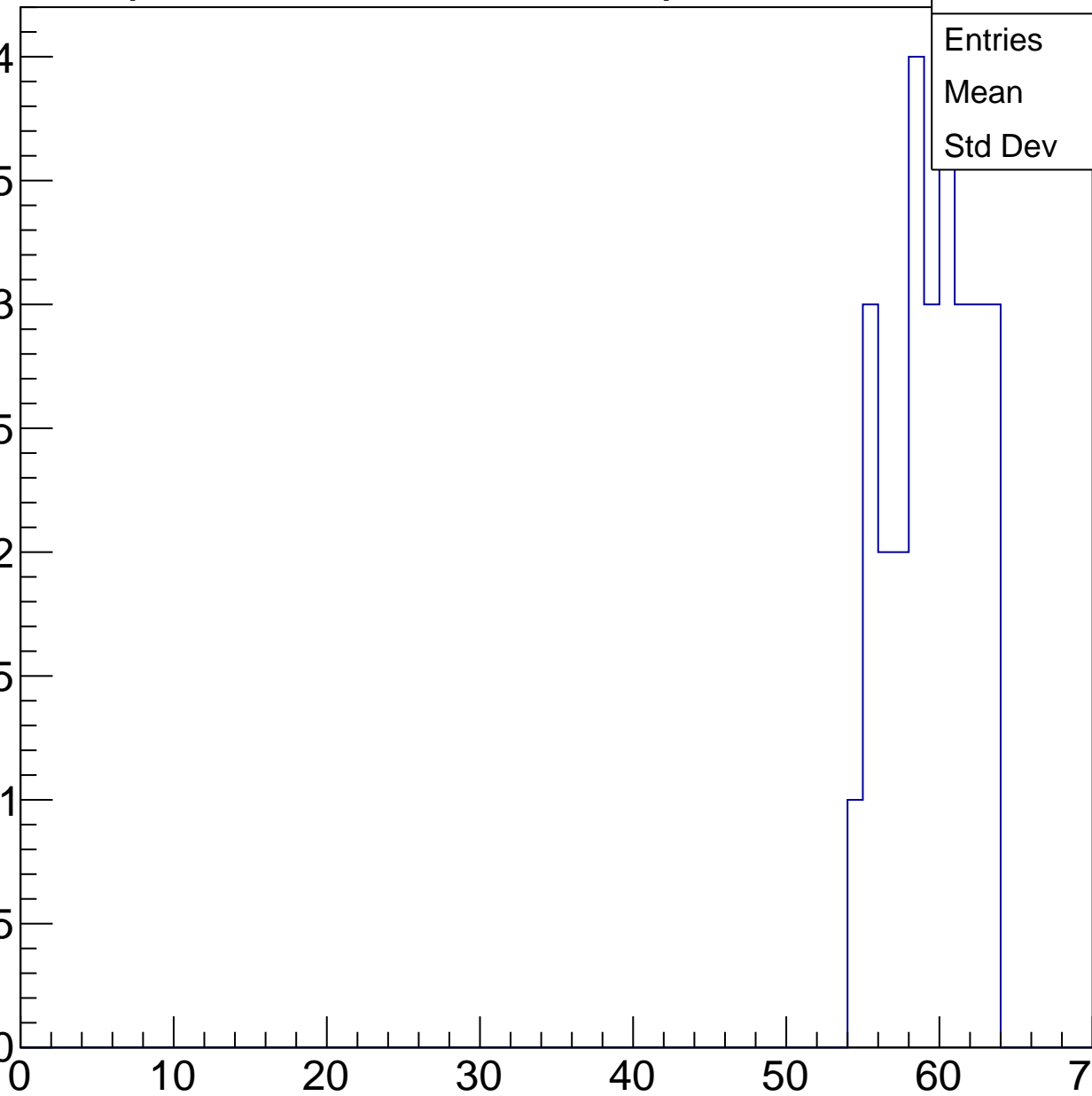
calib_packv5_041523_1651.root, FC#0, port C2

Entry

4
3.5
3
2.5
2
1.5
1
0.5
0

Entries	28
Mean	59
Std Dev	2.632

ampl



B1L103S, U14-ch60, adc6

calib_packv5_041523_1651.root, FC#0, port C2

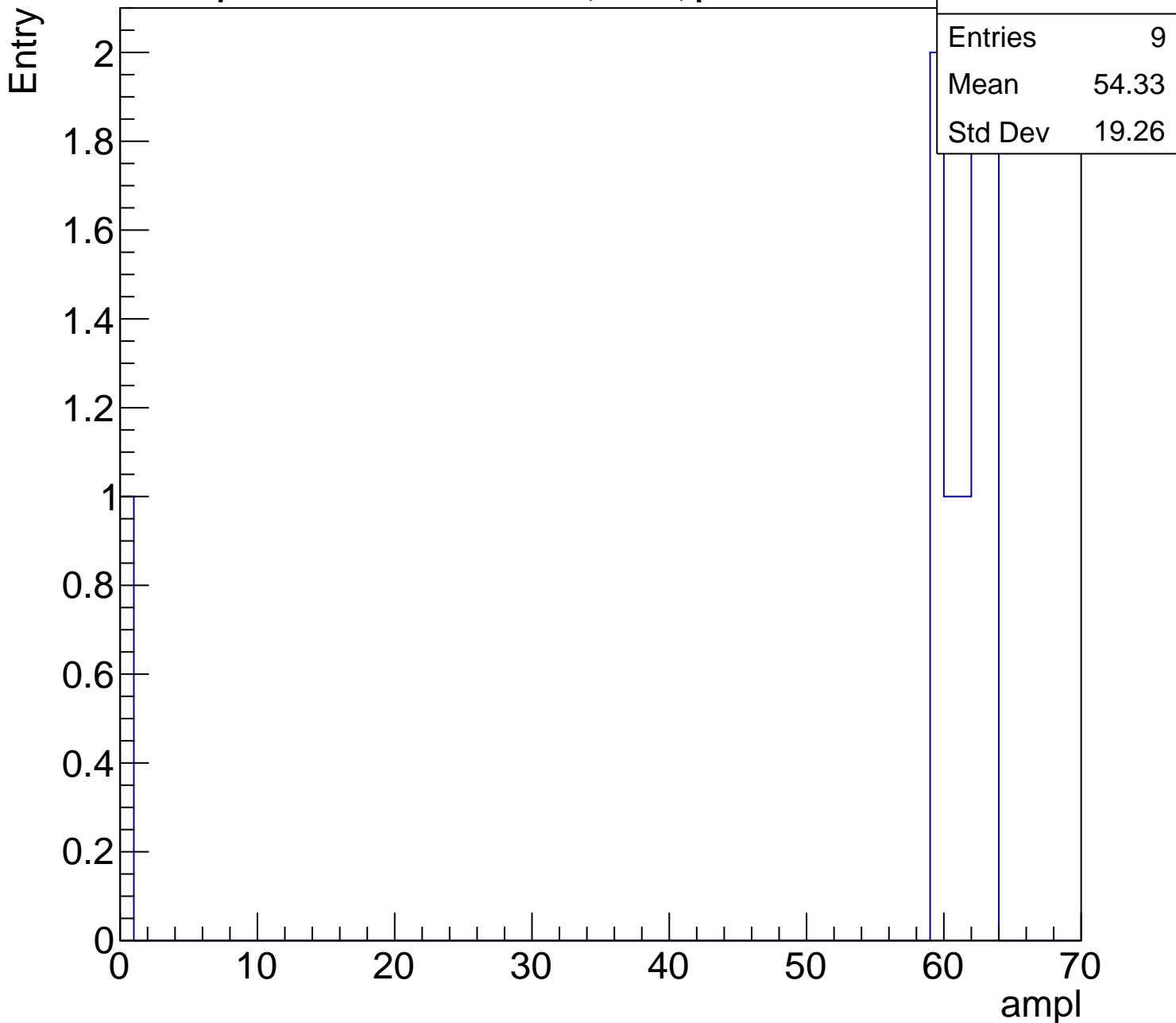
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	9
Mean	54.33
Std Dev	19.26

0 10 20 30 40 50 60 70

ampl



B1L103S, U14-ch60, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch61, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	48
Mean	21.4
Std Dev	13.35

Entry

12

10

8

6

4

2

0

0

10

20

30

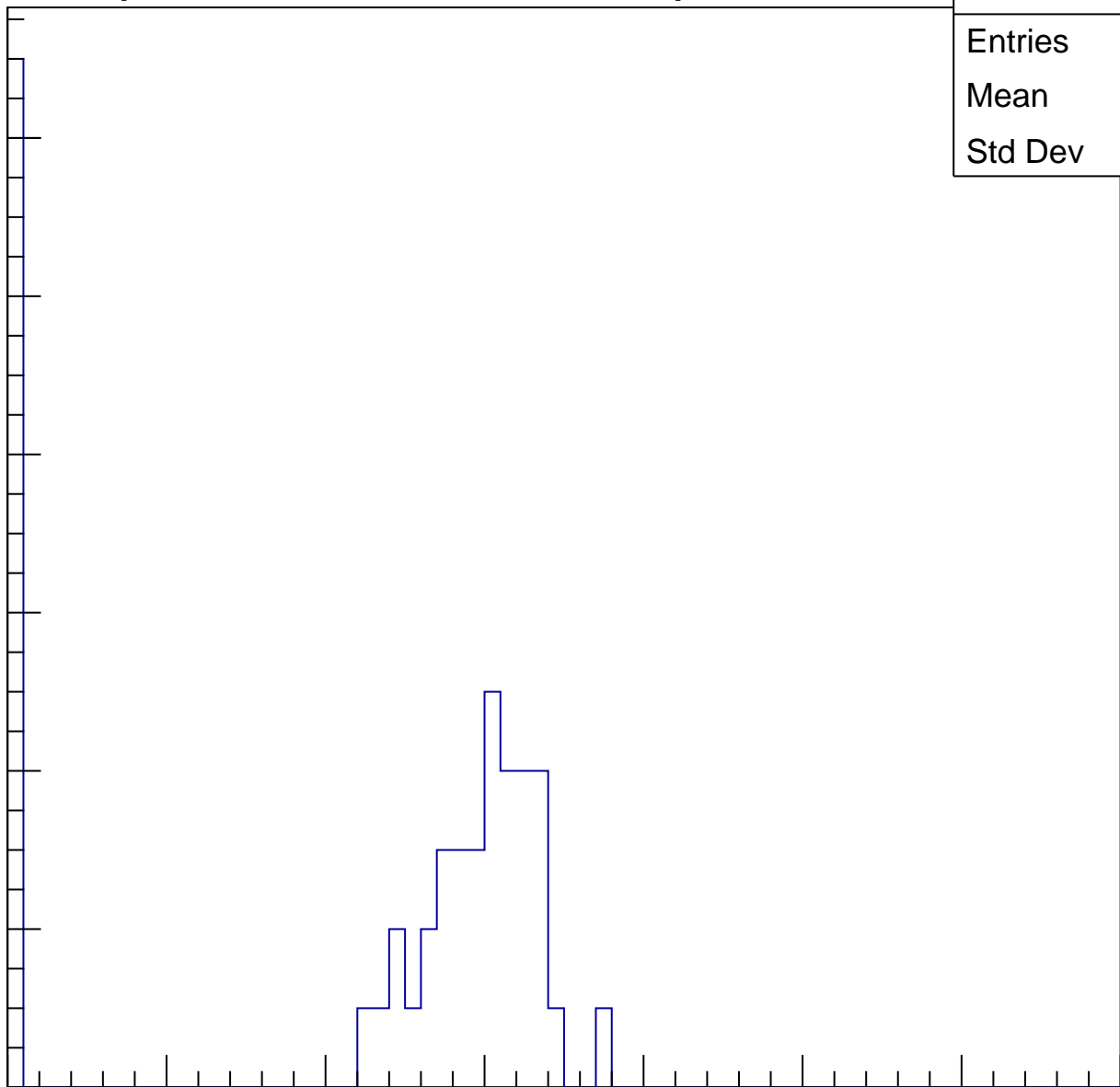
40

50

60

70

ampl

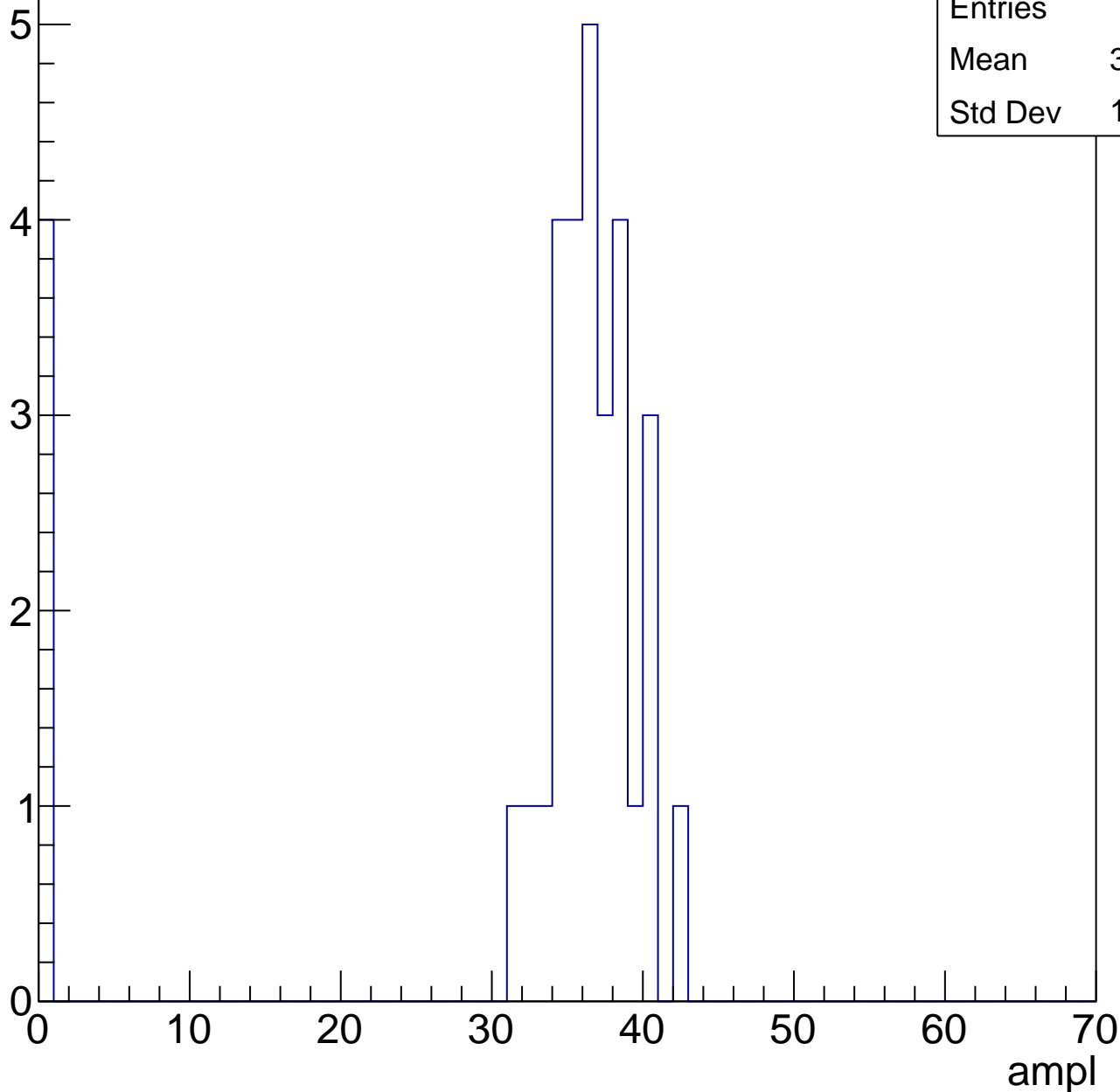


B1L103S, U14-ch61, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	32
Mean	31.75
Std Dev	12.23

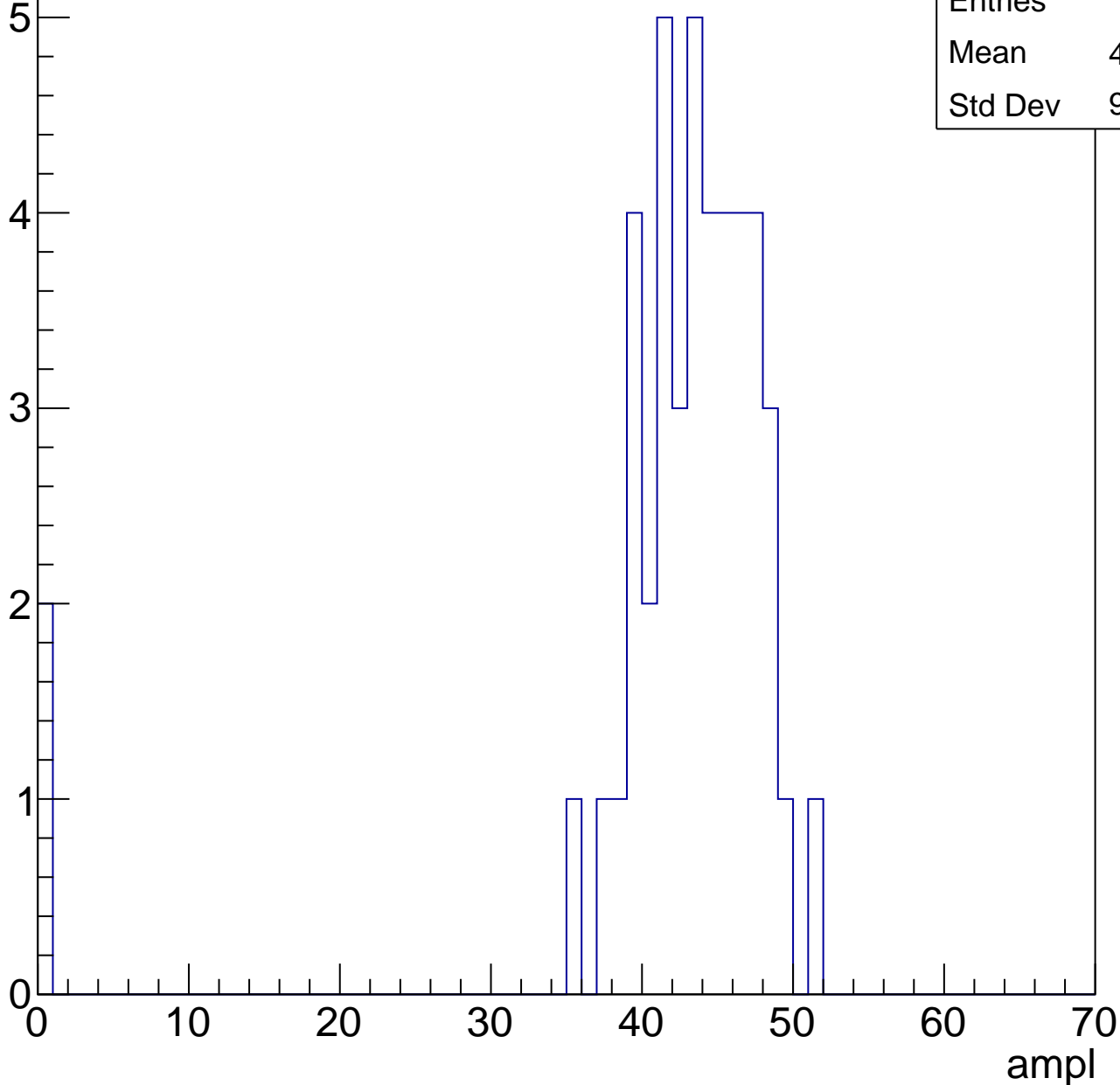


B1L103S, U14-ch61, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	45
Mean	41.42
Std Dev	9.558

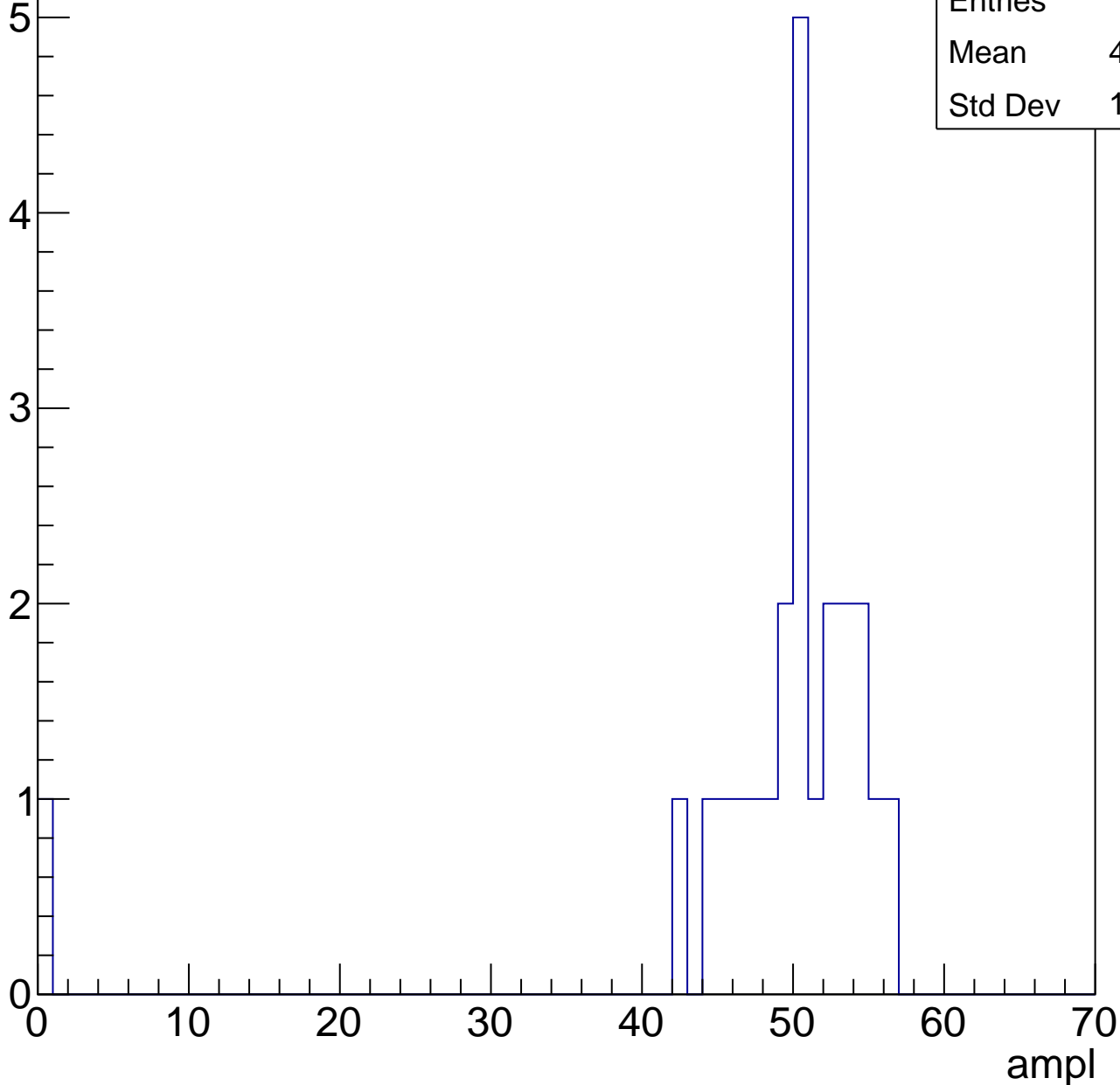


B1L103S, U14-ch61, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

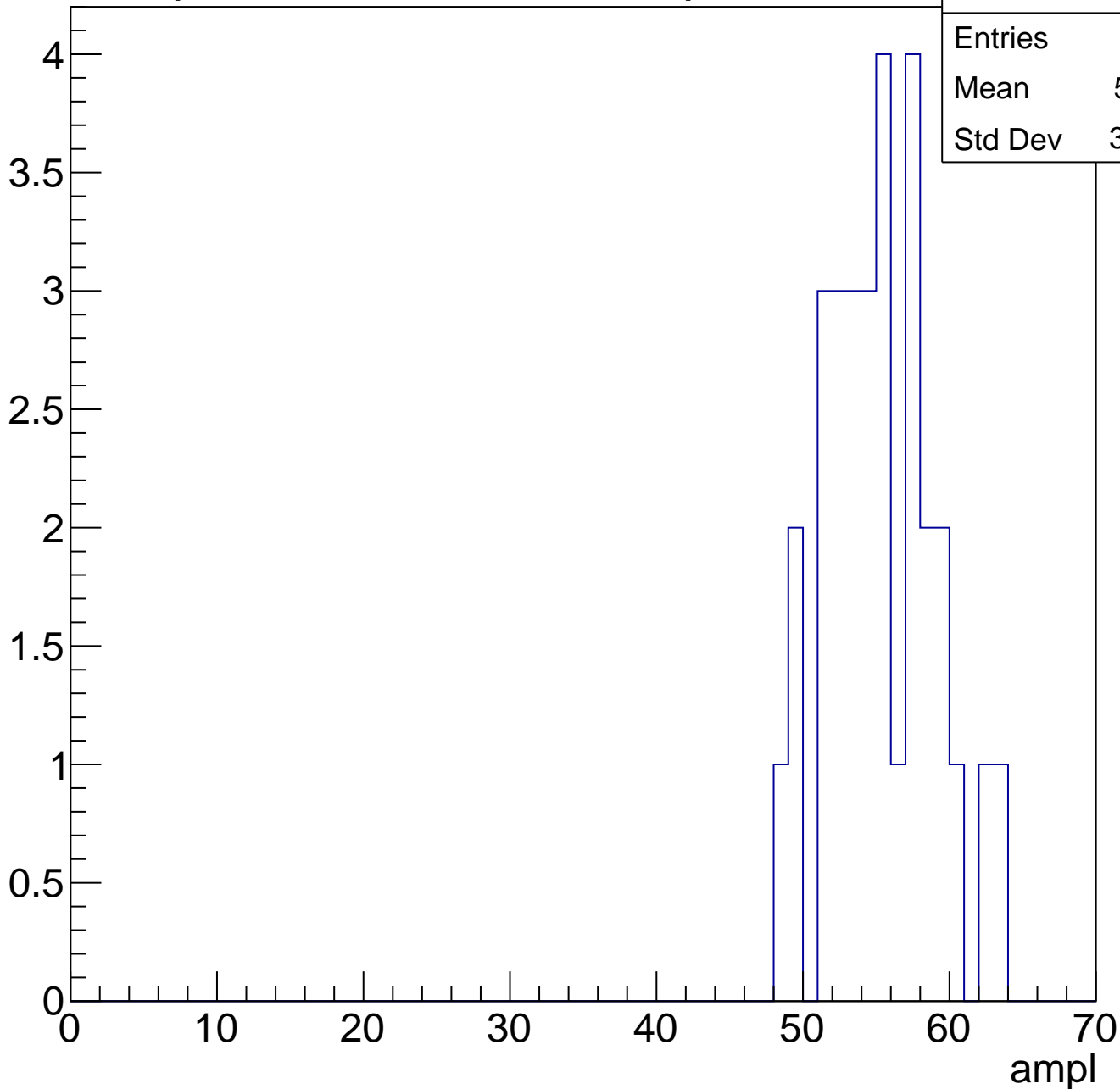
Entries	23
Mean	47.83
Std Dev	10.77



B1L103S, U14-ch61, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch61, adc5

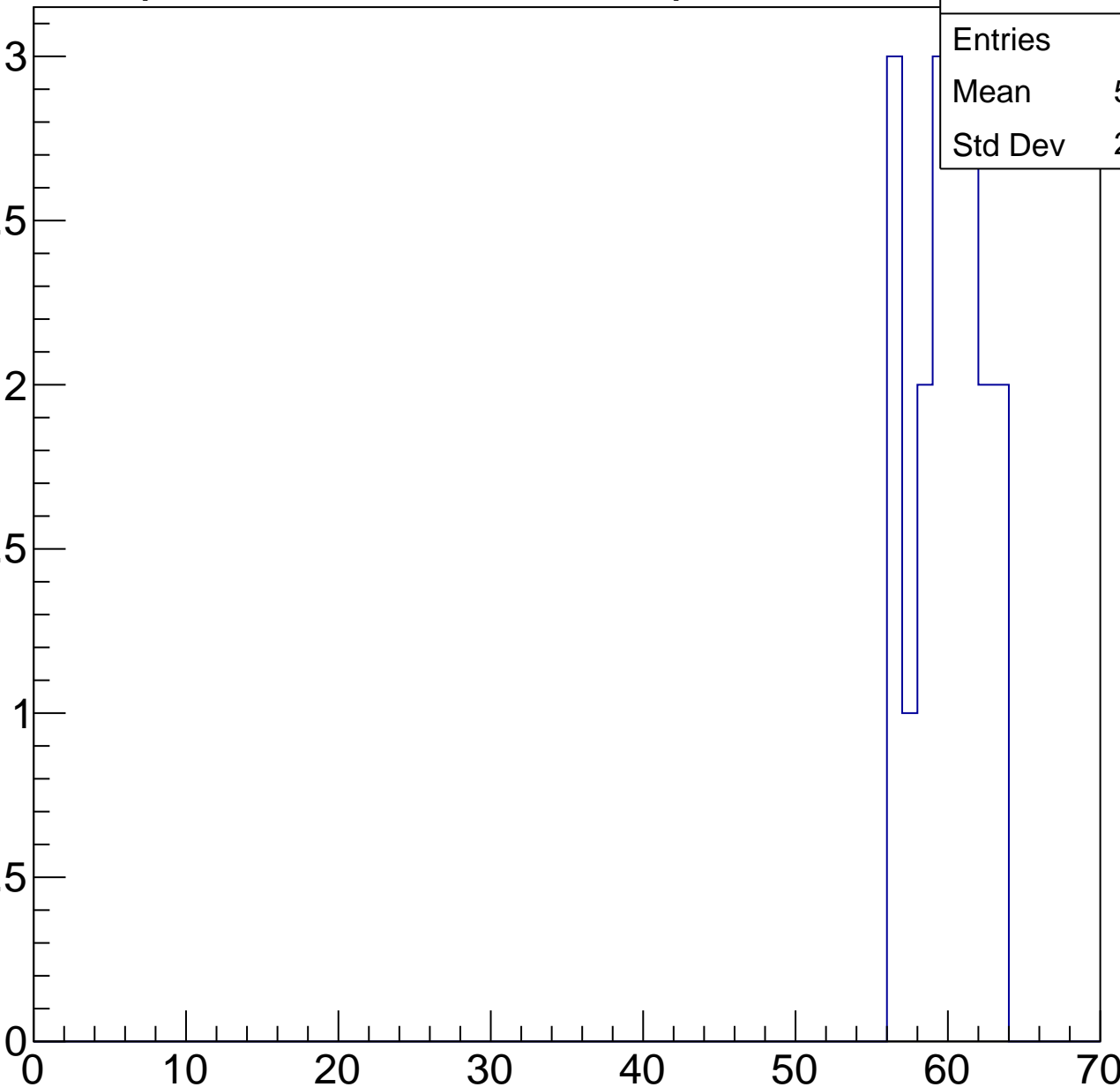
calib_packv5_041523_1651.root, FC#0, port C2

Entry

3
2.5
2
1.5
1
0.5
0

Entries	19
Mean	59.53
Std Dev	2.209

ampl



B1L103S, U14-ch61, adc6

calib_packv5_041523_1651.root, FC#0, port C2

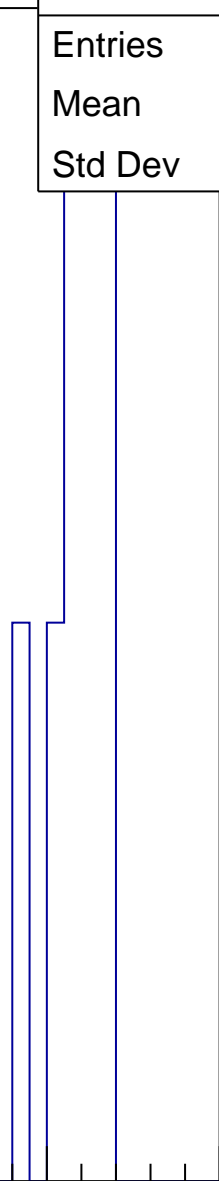
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	8
Mean	61.25
Std Dev	1.561

0 10 20 30 40 50 60 70

ampl



B1L103S, U14-ch61, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

12
10
8
6
4
2
0

Entries	12
Mean	0
Std Dev	0

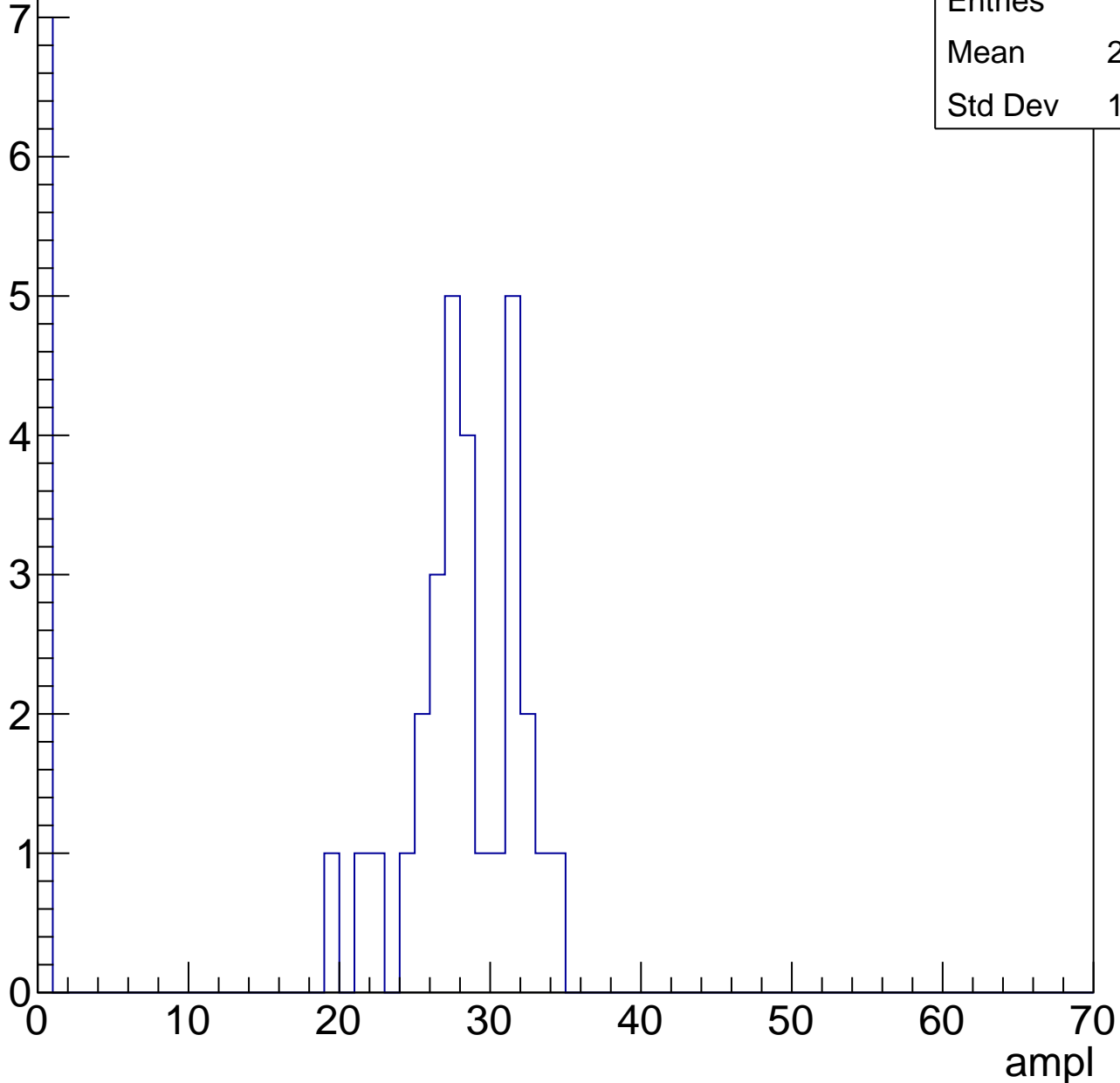
ampl

B1L103S, U14-ch62, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	36
Mean	22.39
Std Dev	11.44

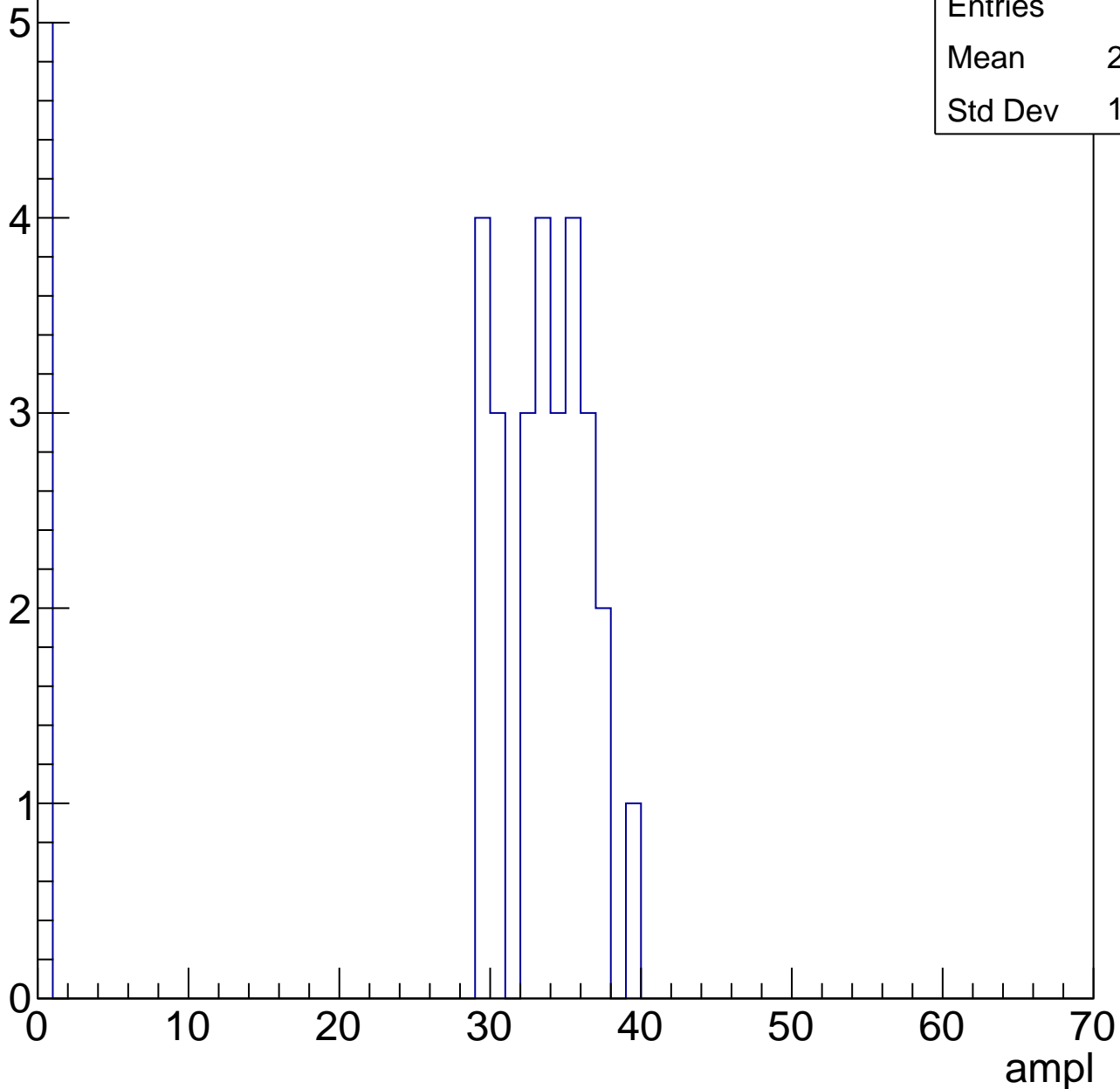


B1L103S, U14-ch62, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	32
Mean	28.03
Std Dev	12.33

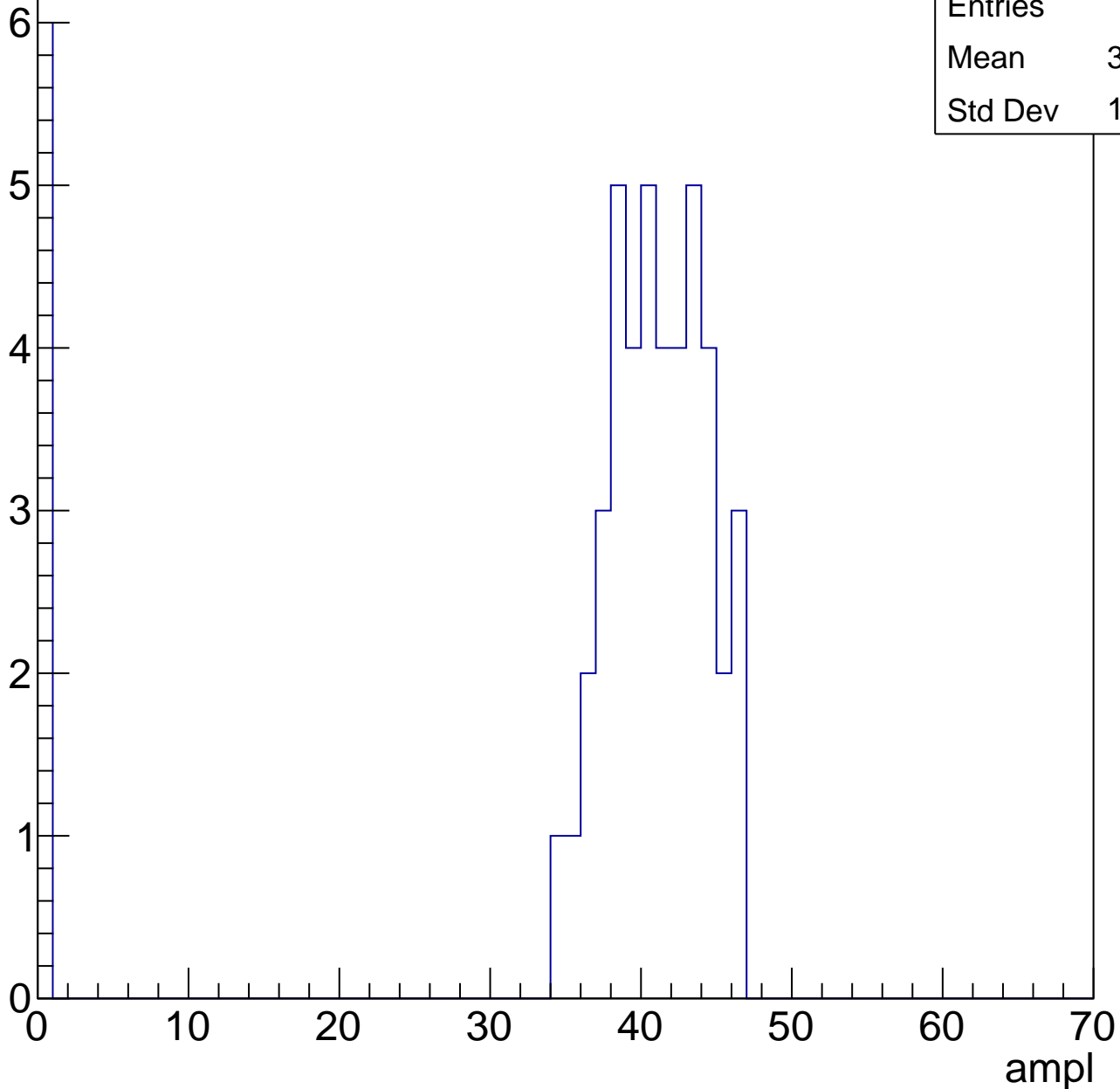


B1L103S, U14-ch62, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

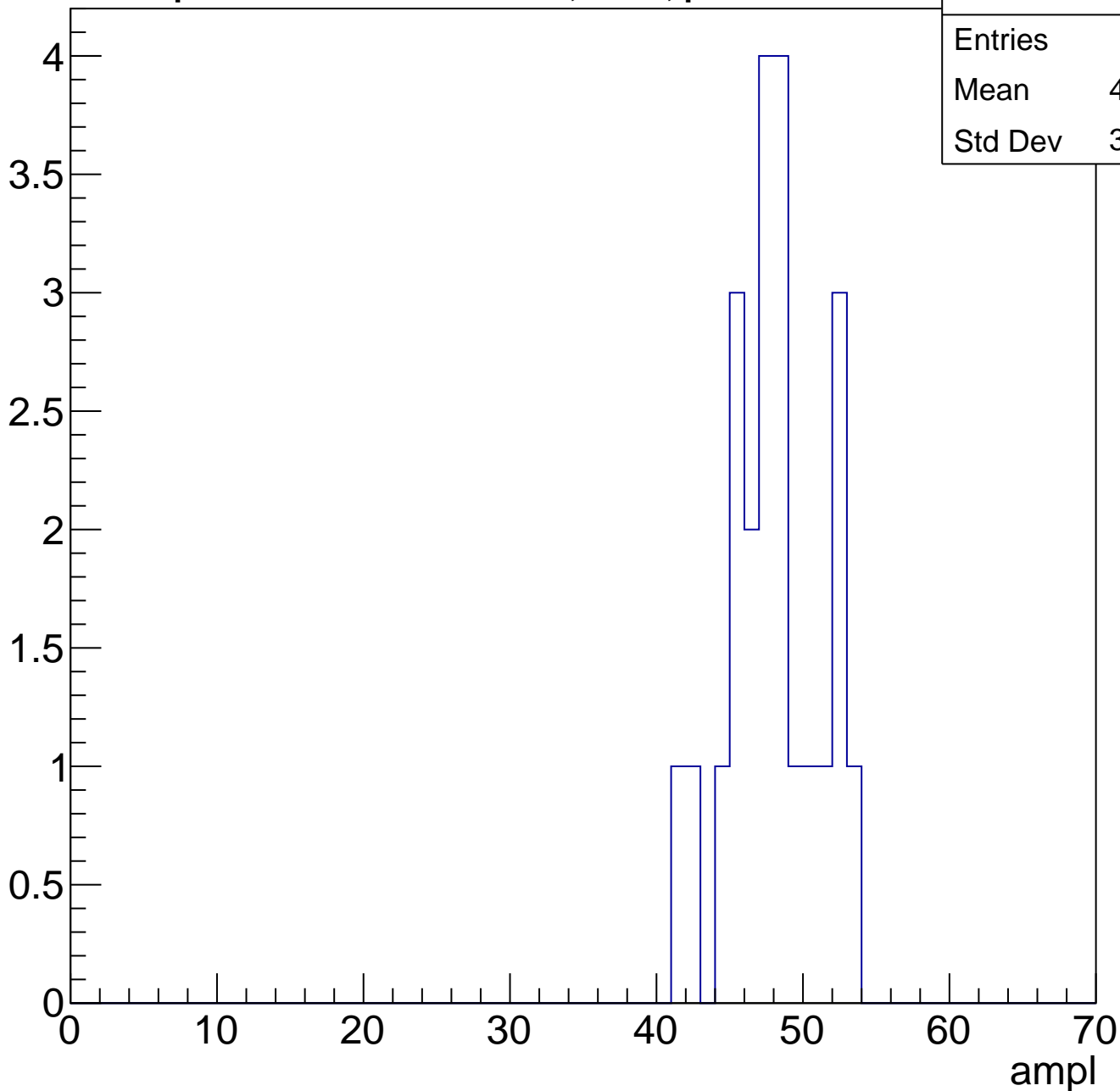
Entries	49
Mean	35.69
Std Dev	13.64



B1L103S, U14-ch62, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

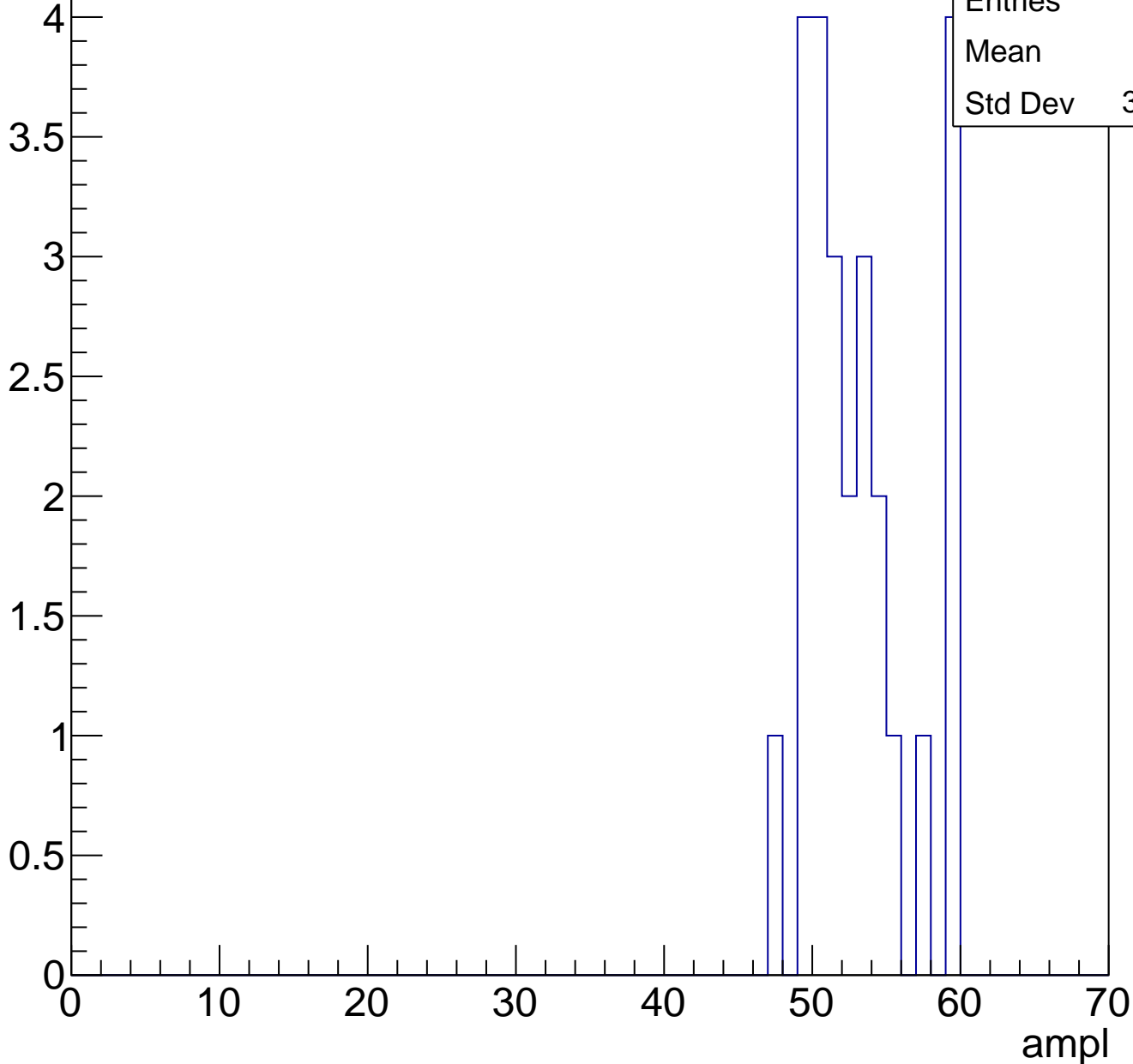


Entries	23
Mean	47.52
Std Dev	3.105

B1L103S, U14-ch62, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

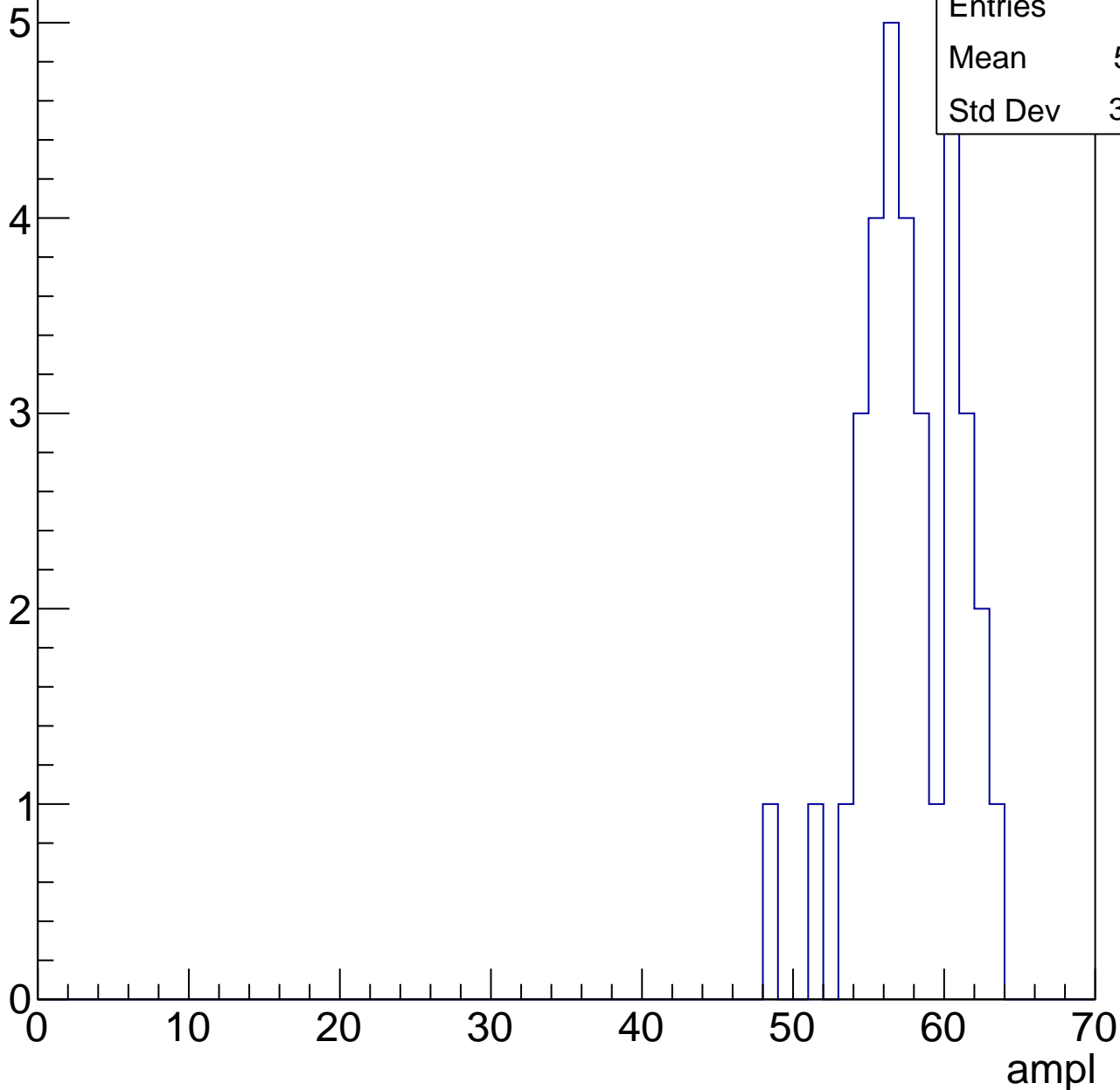


B1L103S, U14-ch62, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

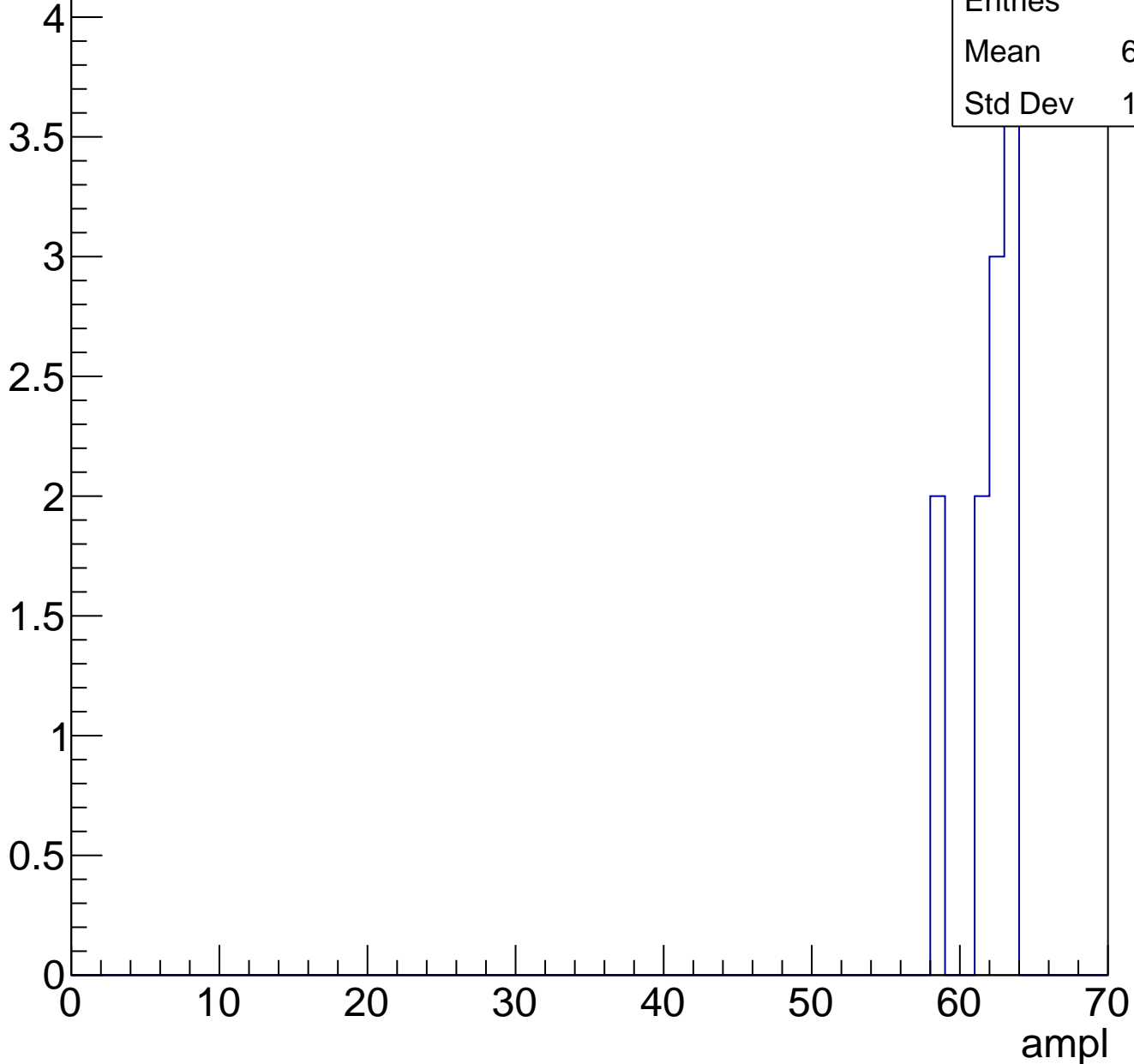
Entries	34
Mean	57.21
Std Dev	3.279



B1L103S, U14-ch62, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



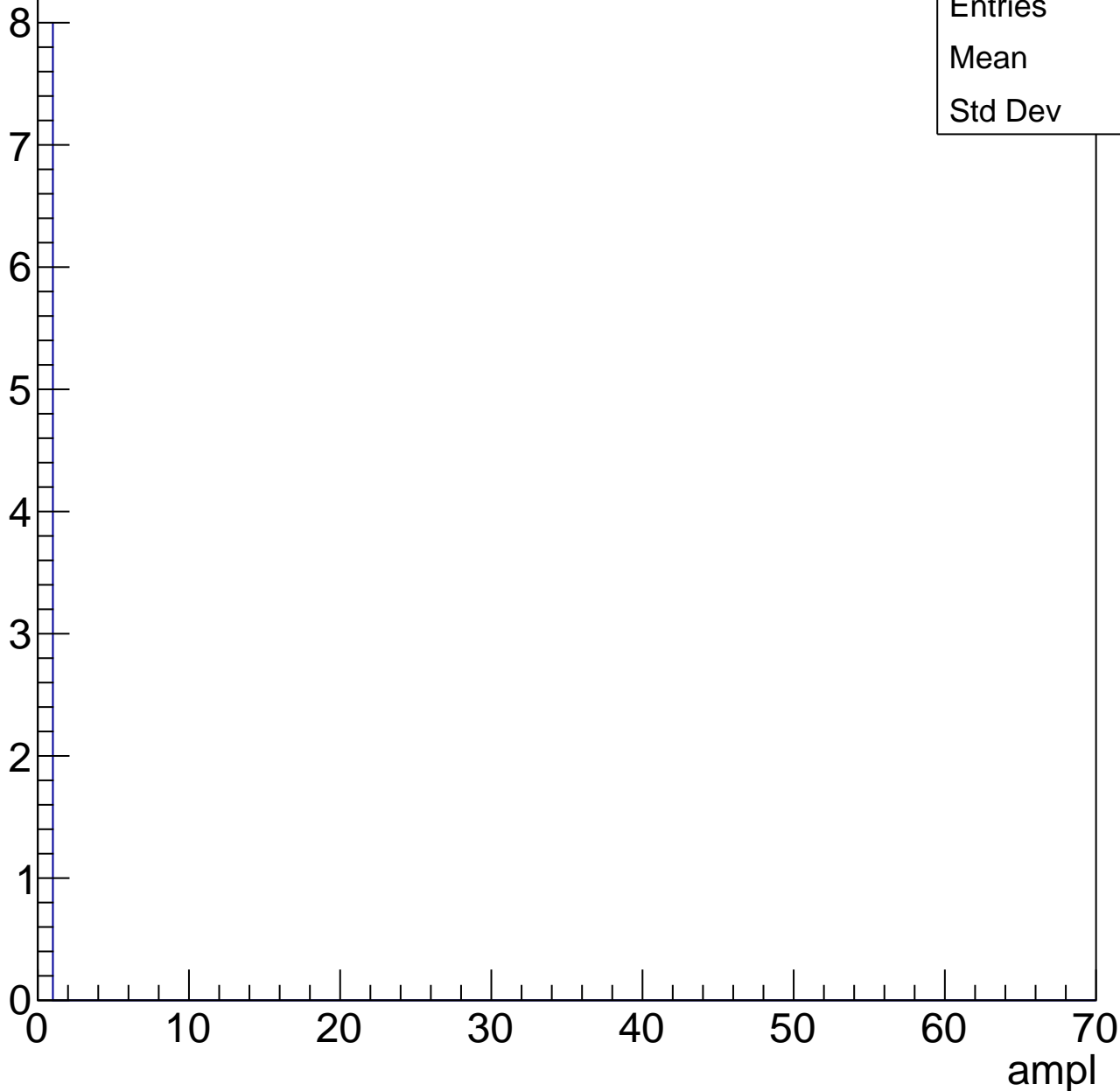
Entries	11
Mean	61.45
Std Dev	1.777

B1L103S, U14-ch62, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	8
Mean	0
Std Dev	0



B1L103S, U14-ch63, adc0

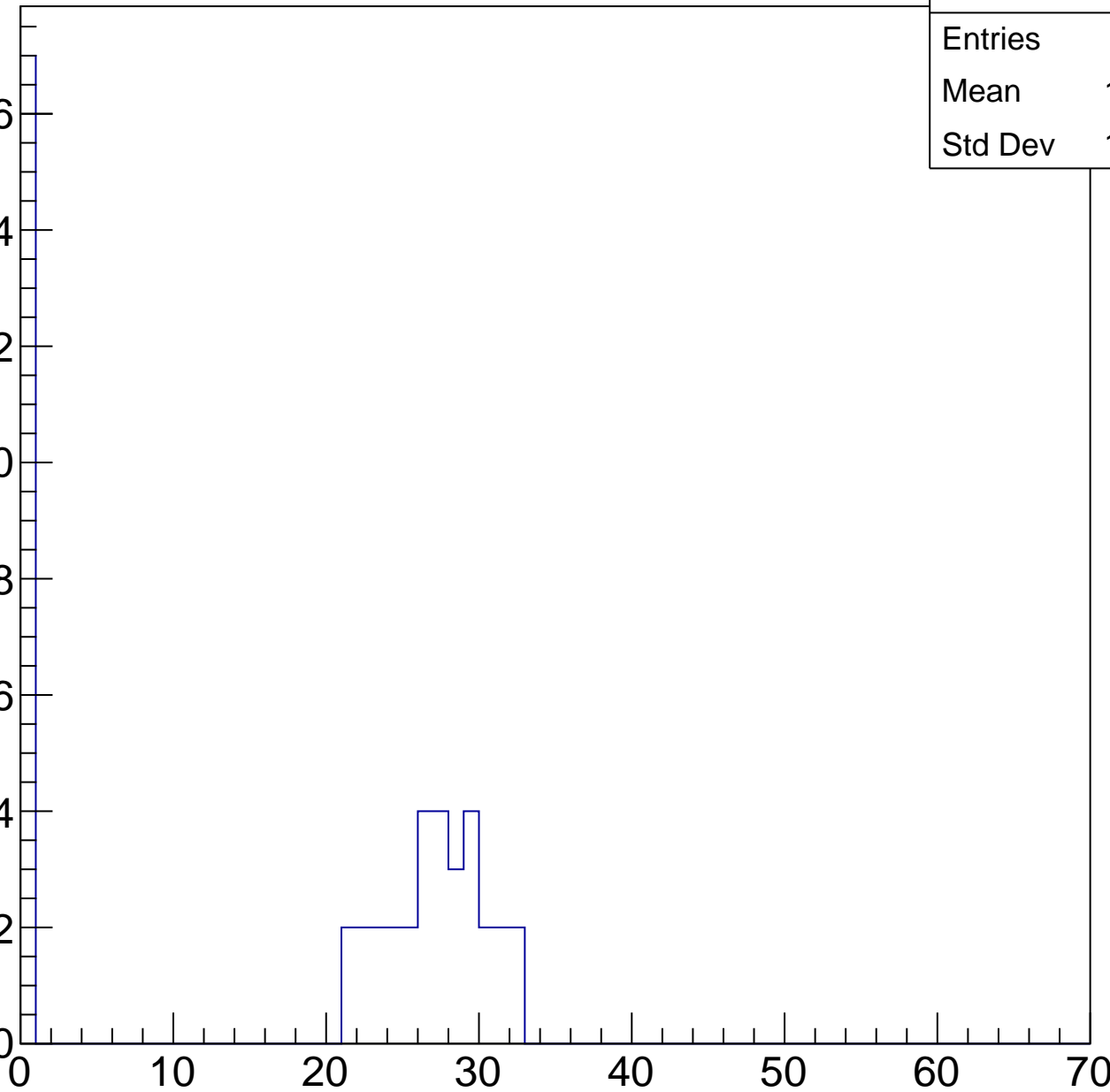
calib_packv5_041523_1651.root, FC#0, port C2

Entries	48
Mean	17.25
Std Dev	13.02

Entry

16
14
12
10
8
6
4
2
0

ampl

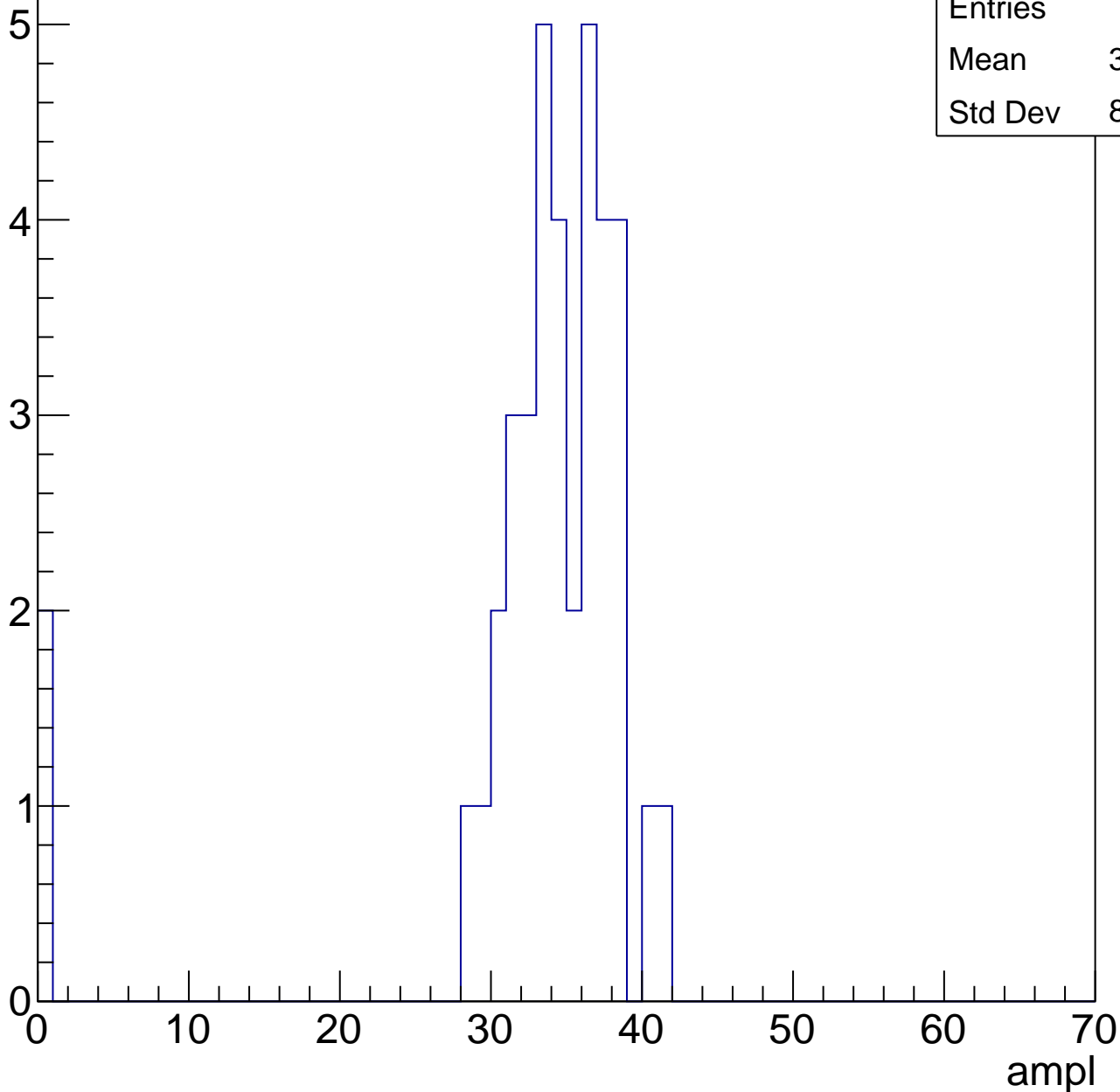


B1L103S, U14-ch63, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	38
Mean	32.58
Std Dev	8.239

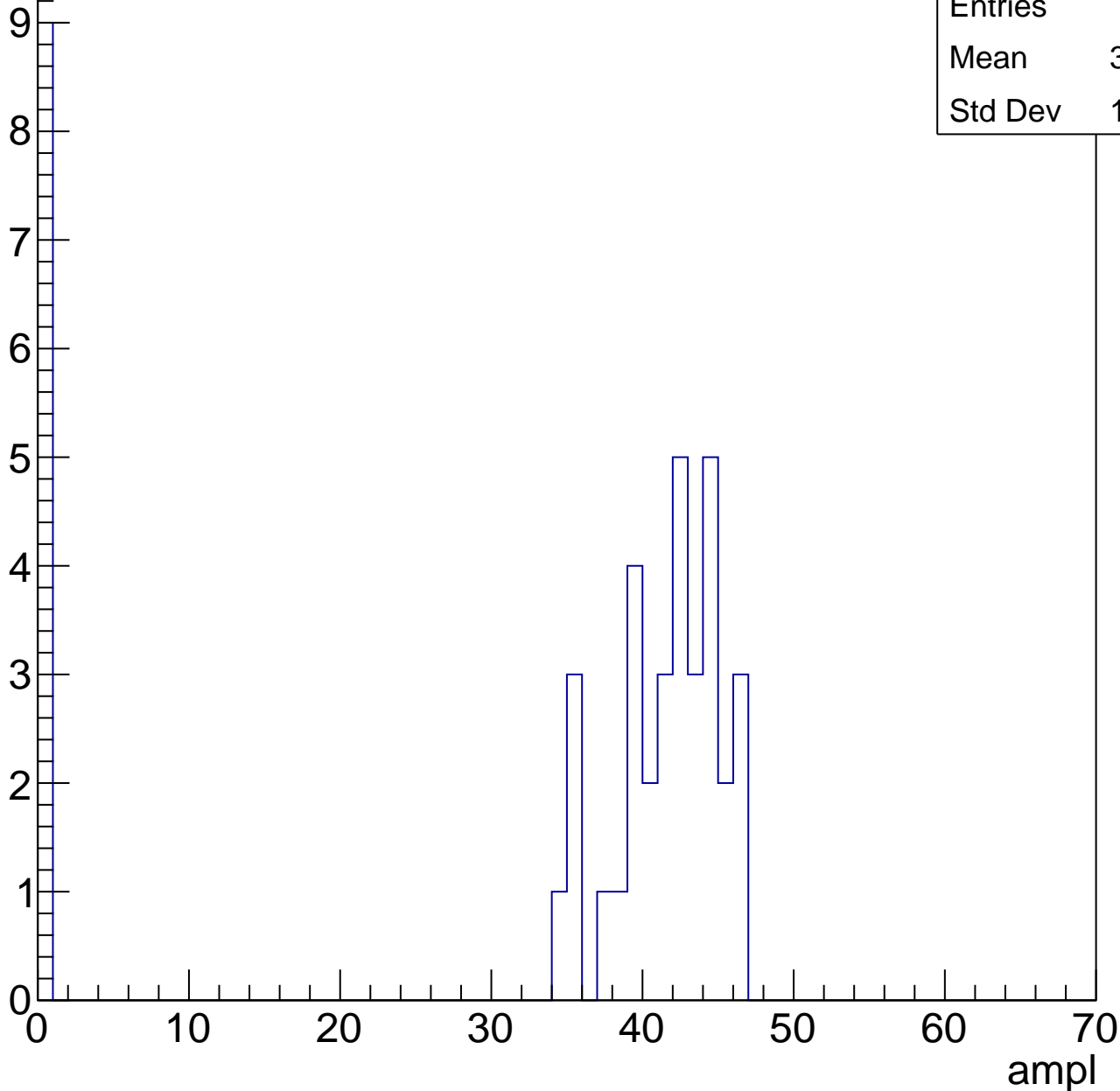


B1L103S, U14-ch63, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	42
Mean	32.38
Std Dev	17.17

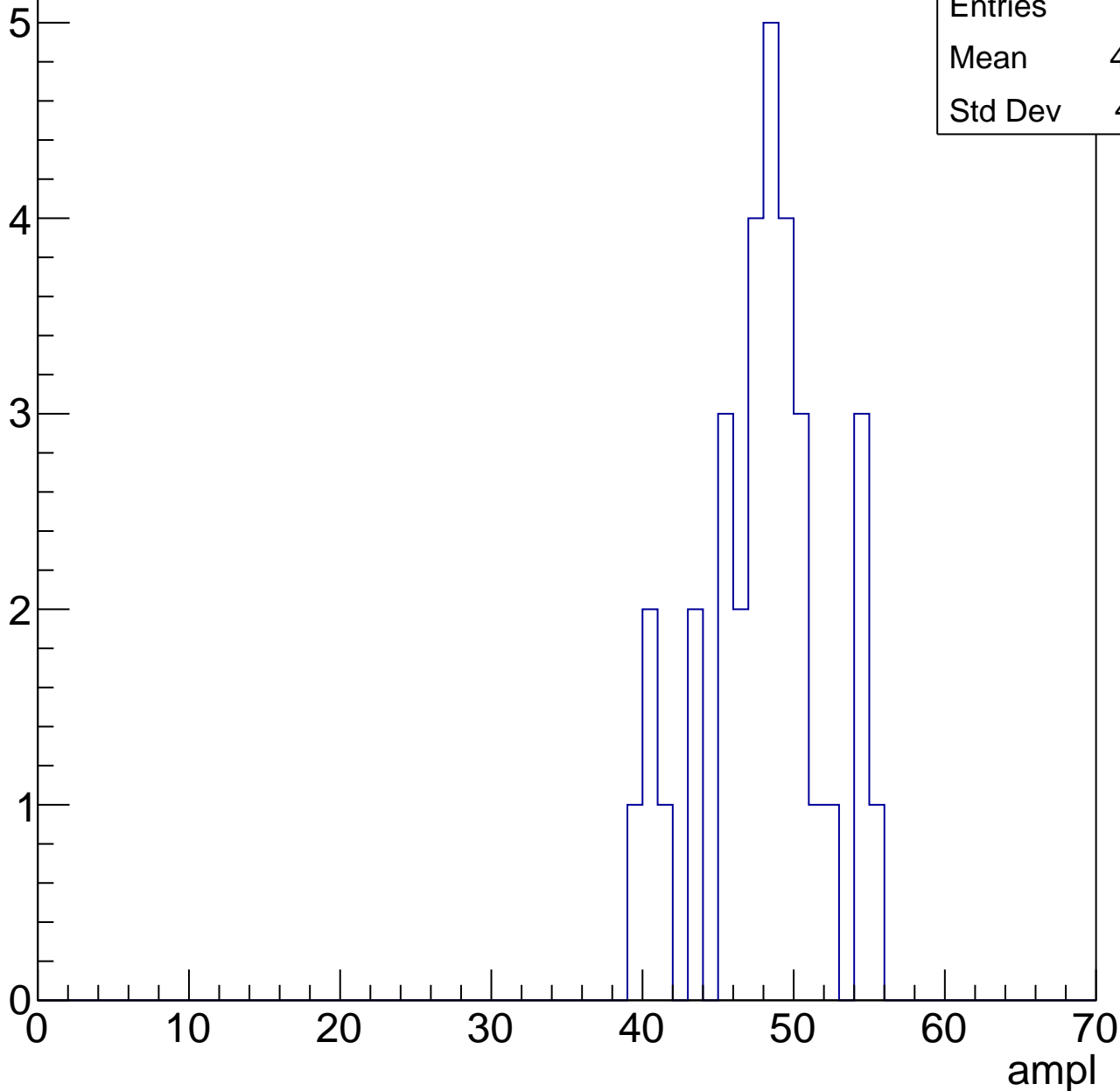


B1L103S, U14-ch63, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	33
Mean	47.48
Std Dev	4.031

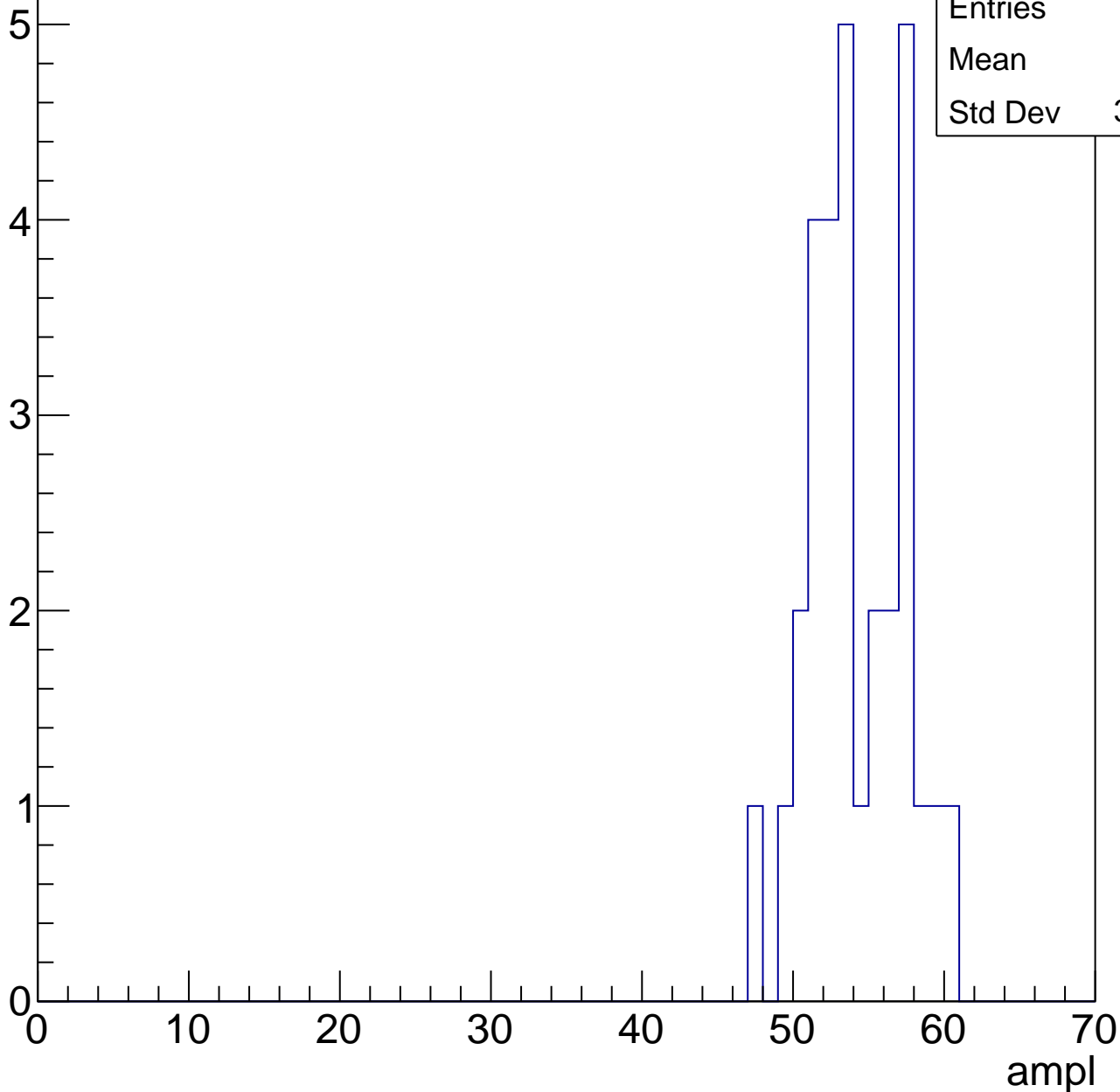


B1L103S, U14-ch63, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

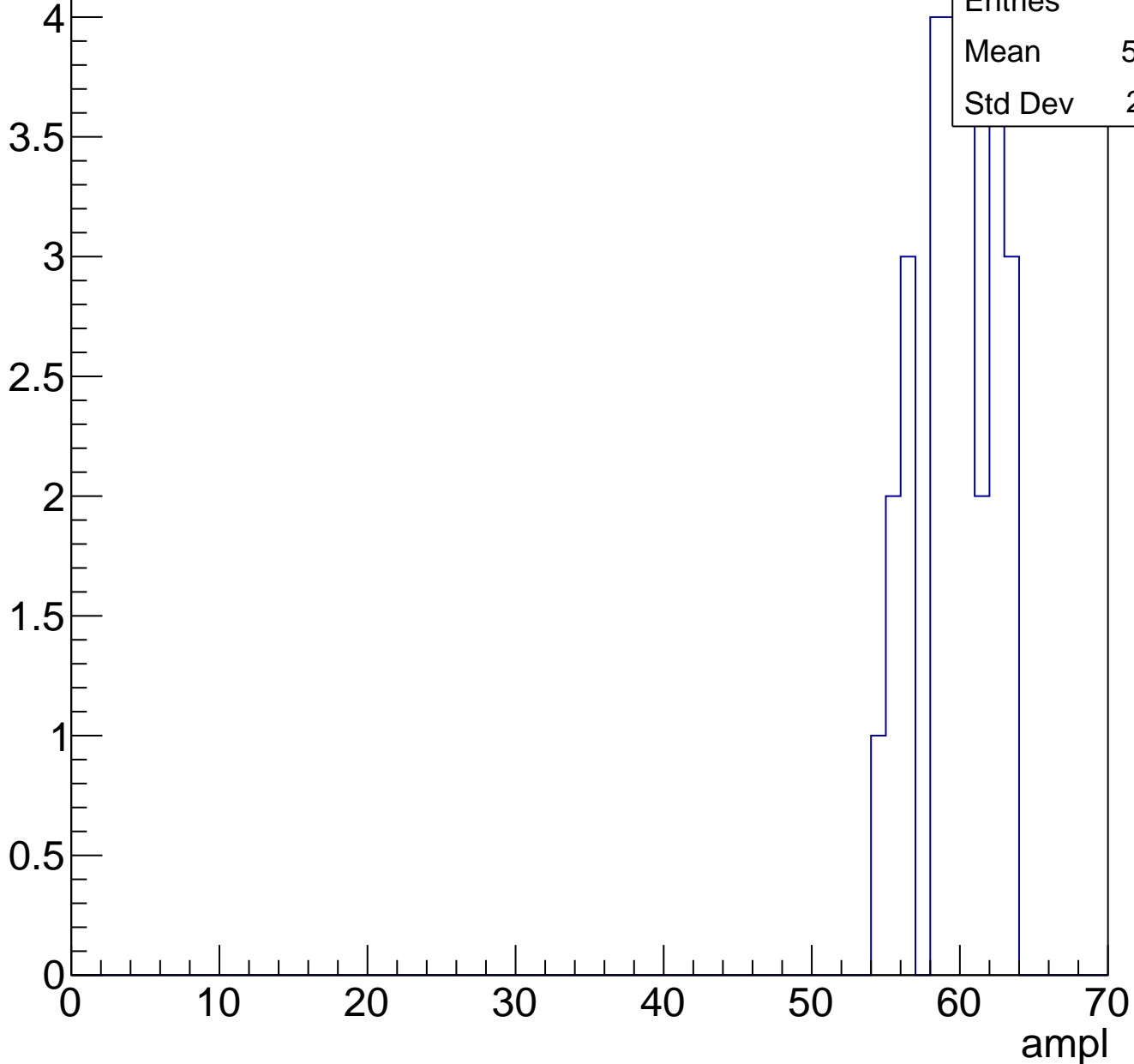
Entries	30
Mean	53.7
Std Dev	3.121



B1L103S, U14-ch63, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

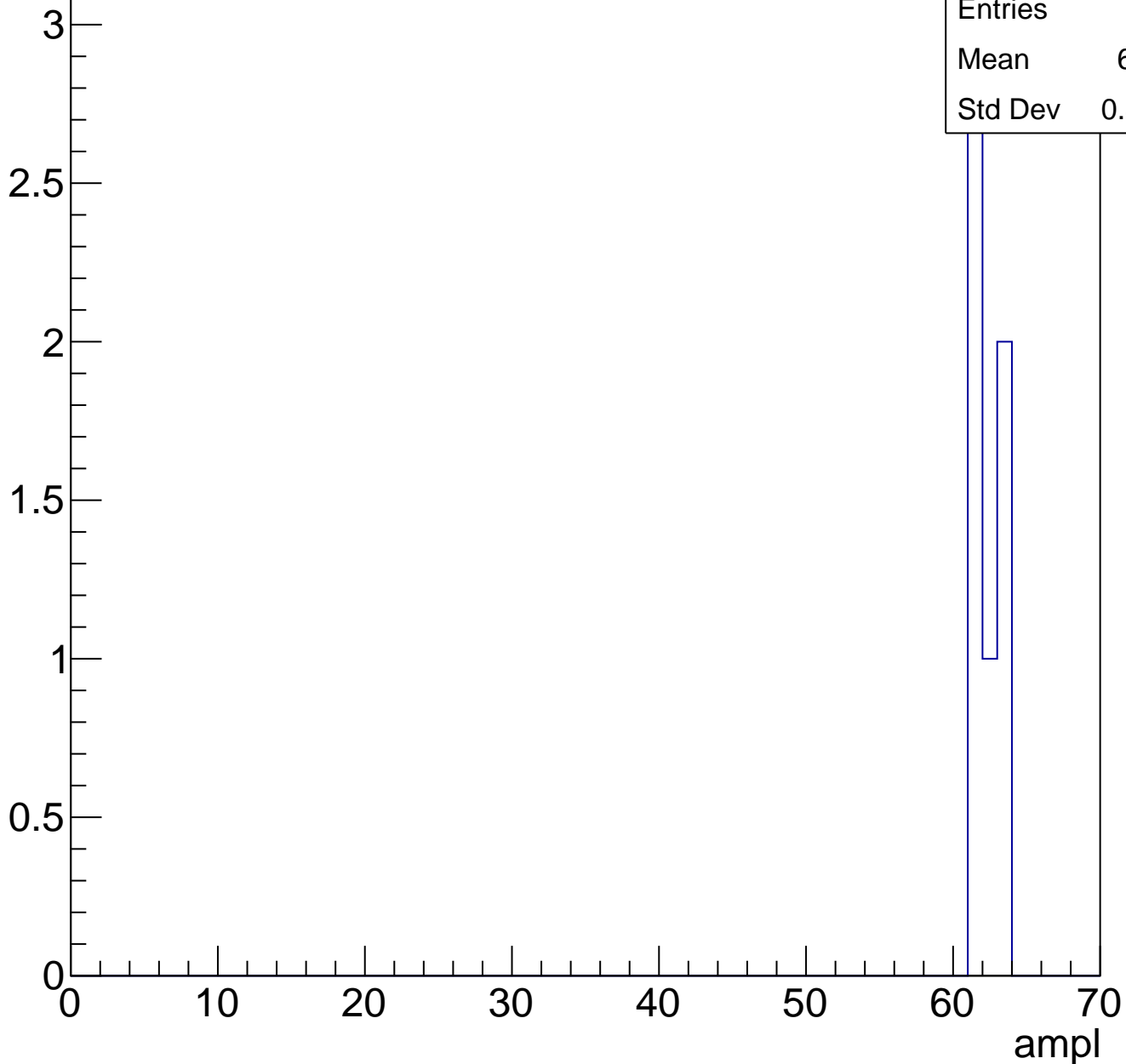


Entries	27
Mean	59.22
Std Dev	2.601

B1L103S, U14-ch63, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

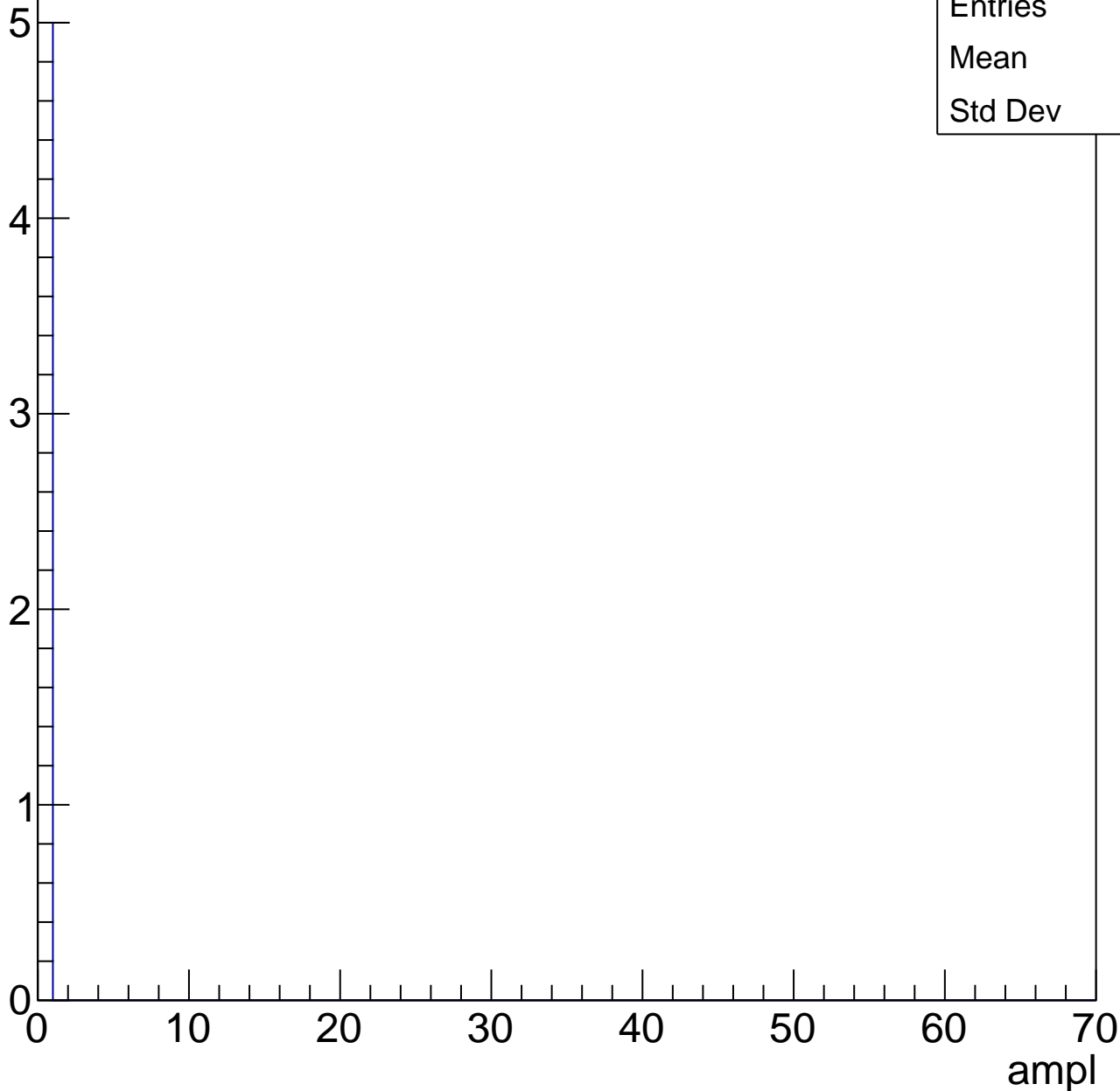


B1L103S, U14-ch63, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	5
Mean	0
Std Dev	0

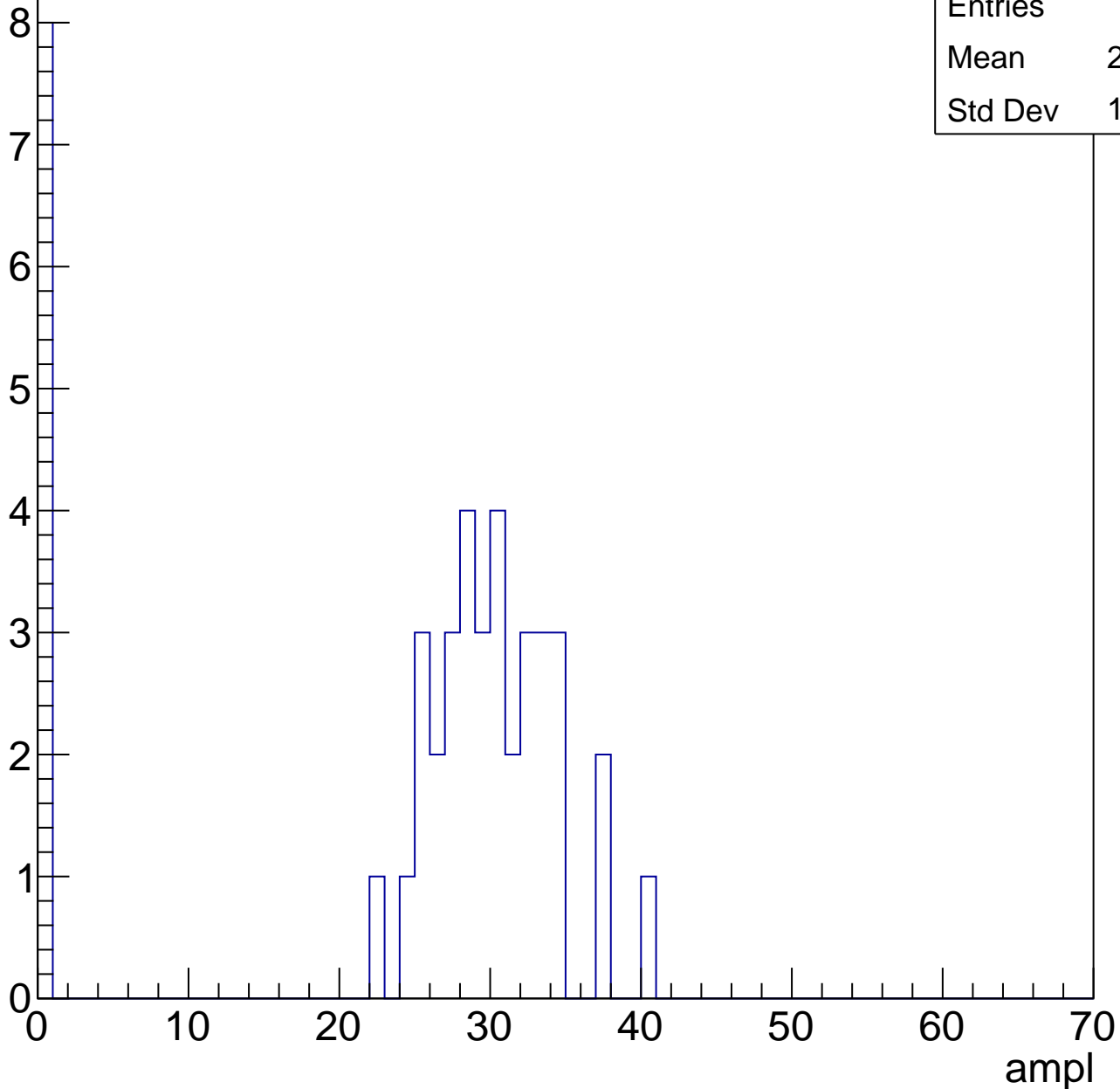


B1L103S, U14-ch64, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	43
Mean	24.33
Std Dev	12.16

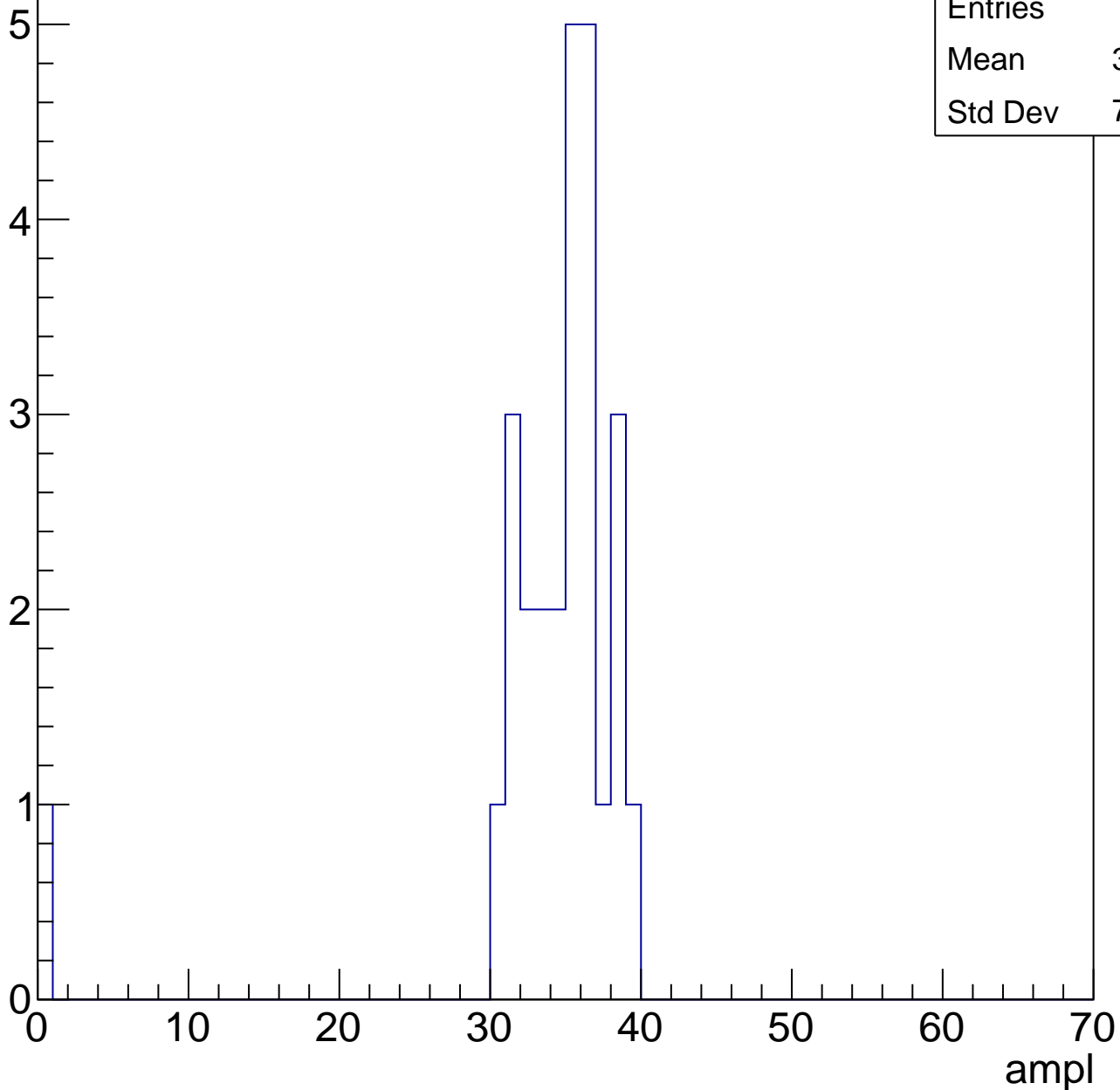


B1L103S, U14-ch64, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	26
Mean	33.31
Std Dev	7.081

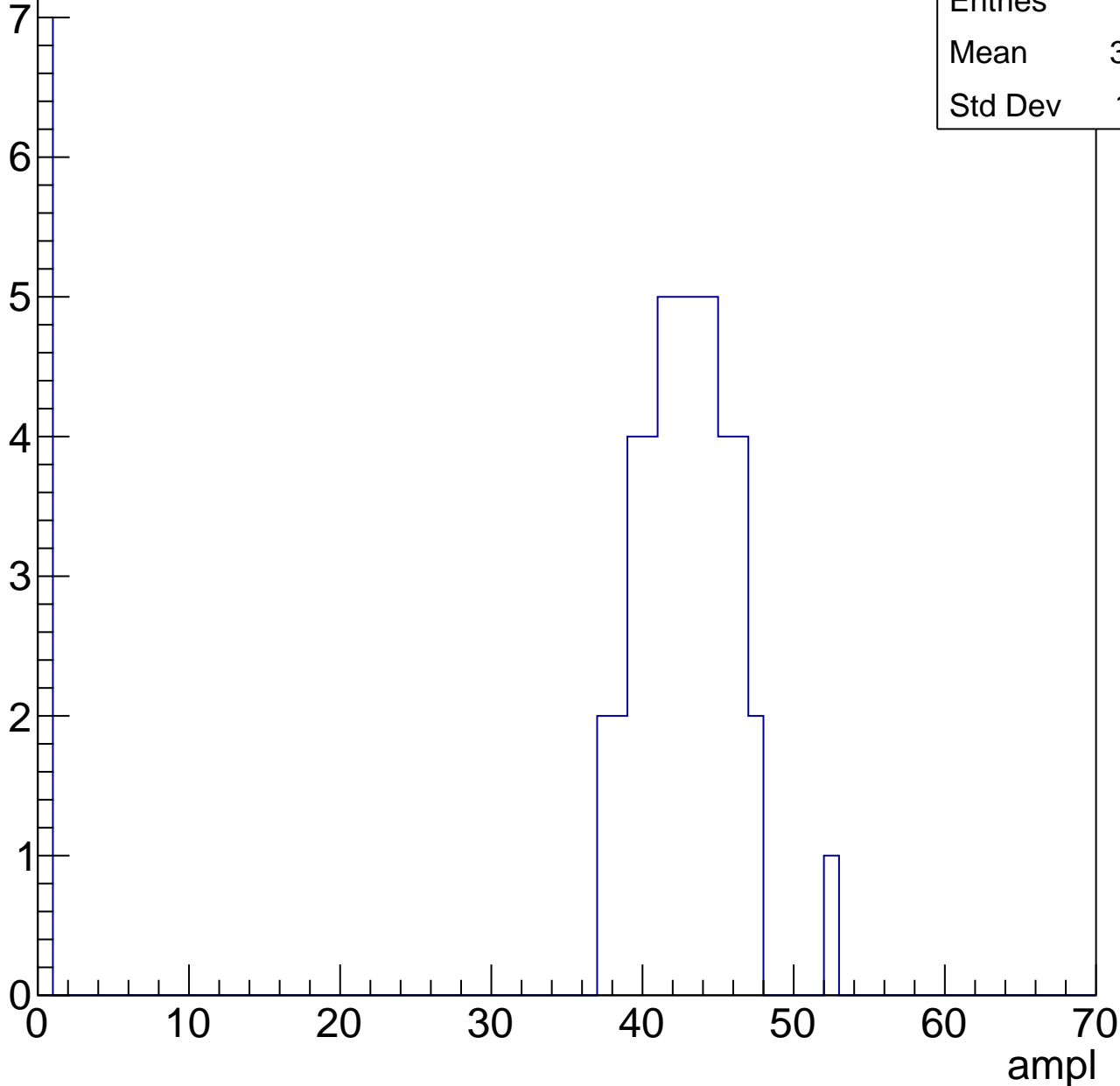


B1L103S, U14-ch64, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	36.52
Std Dev	15.01

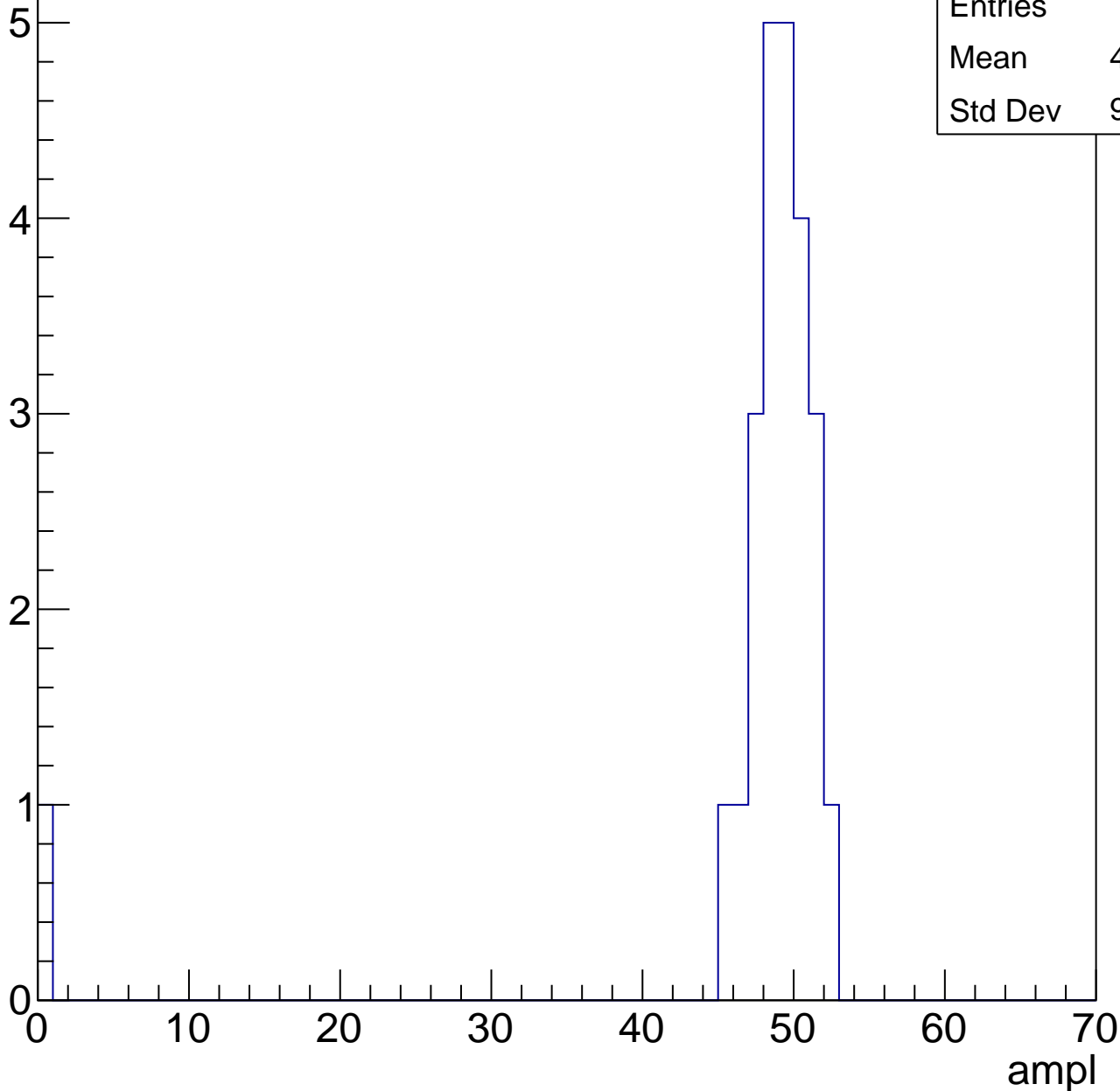


B1L103S, U14-ch64, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	24
Mean	46.75
Std Dev	9.888

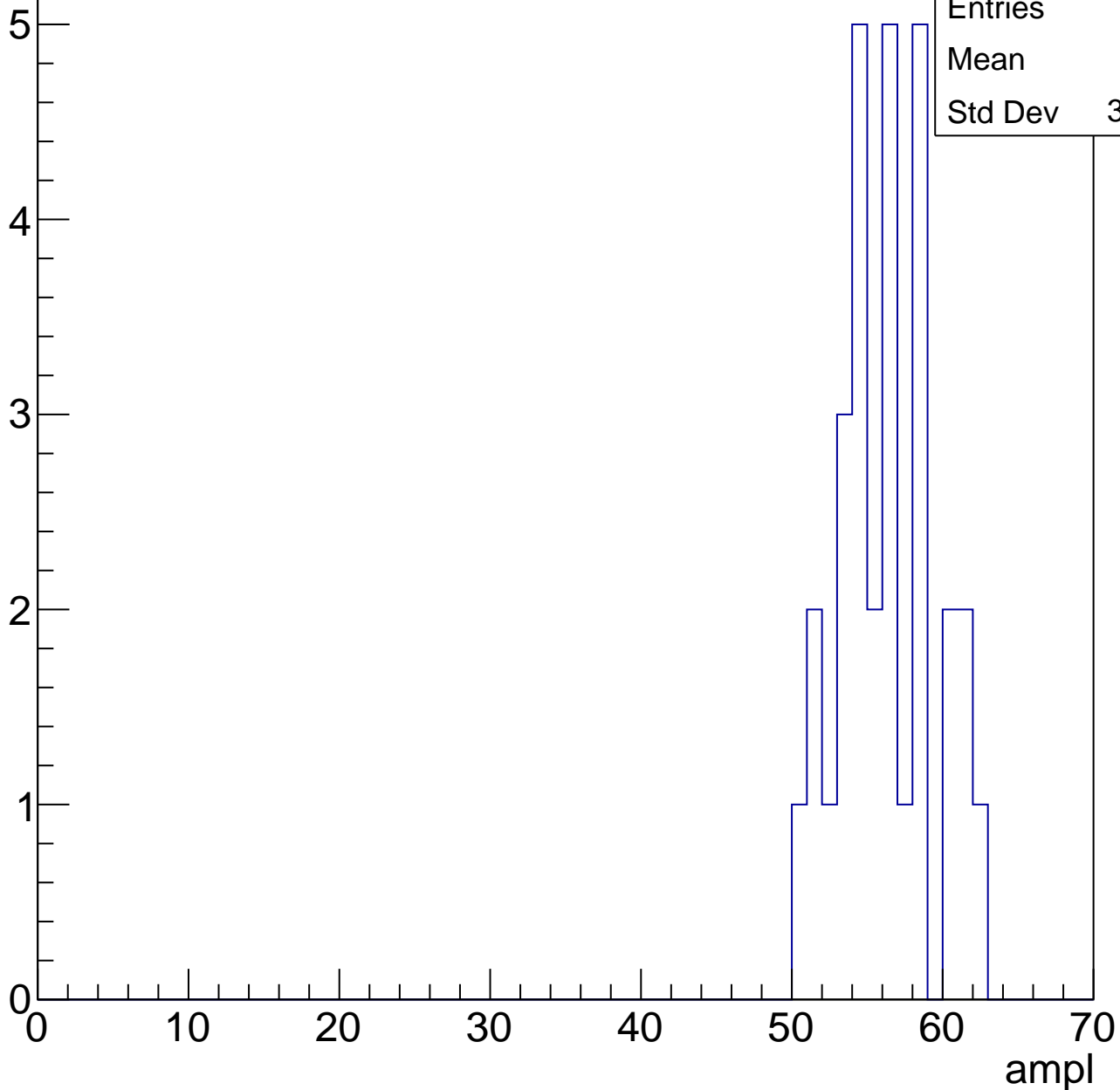


B1L103S, U14-ch64, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

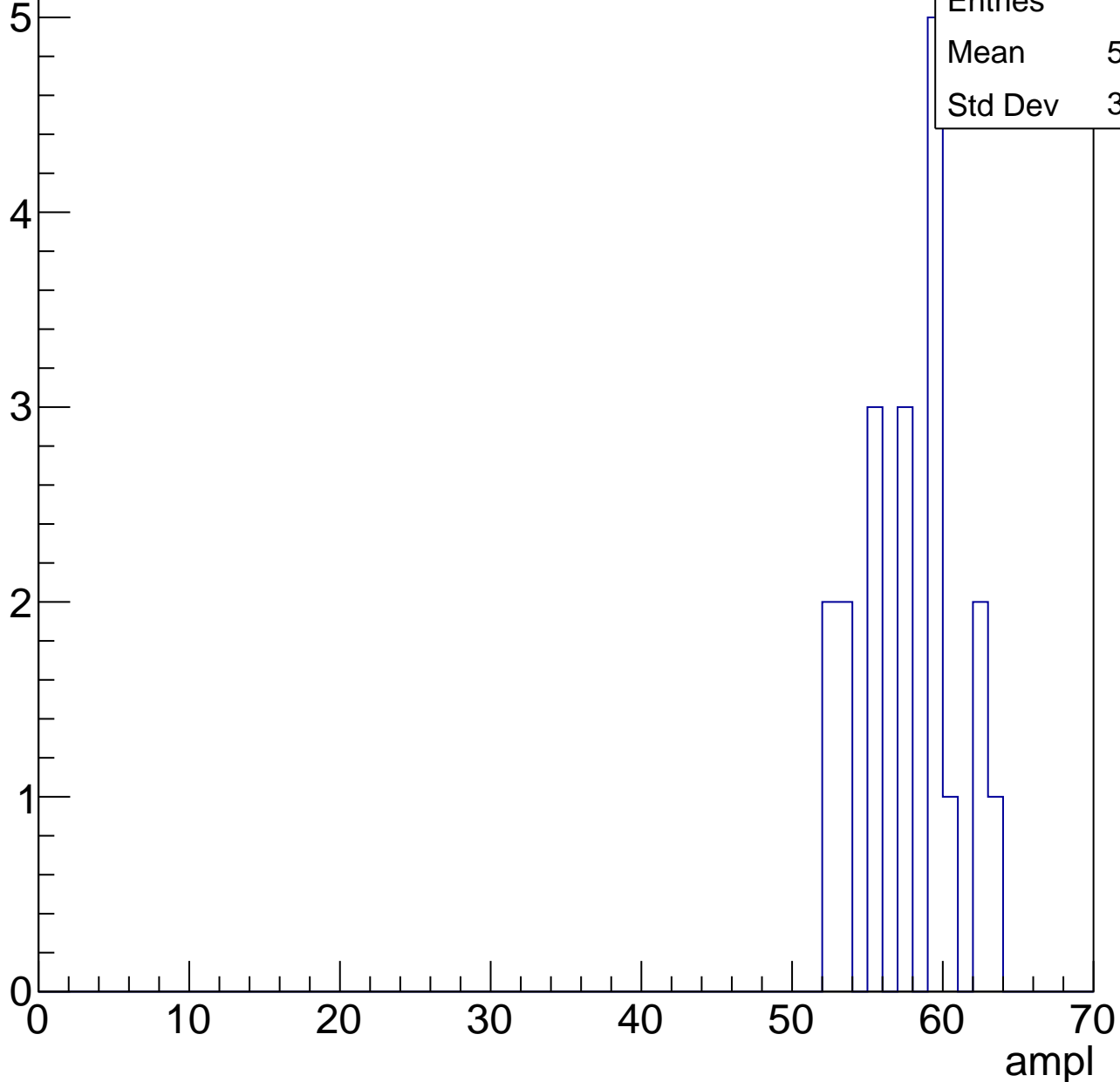
Entries	30
Mean	55.8
Std Dev	3.103



B1L103S, U14-ch64, adc5

calib_packv5_041523_1651.root, FC#0, port C2

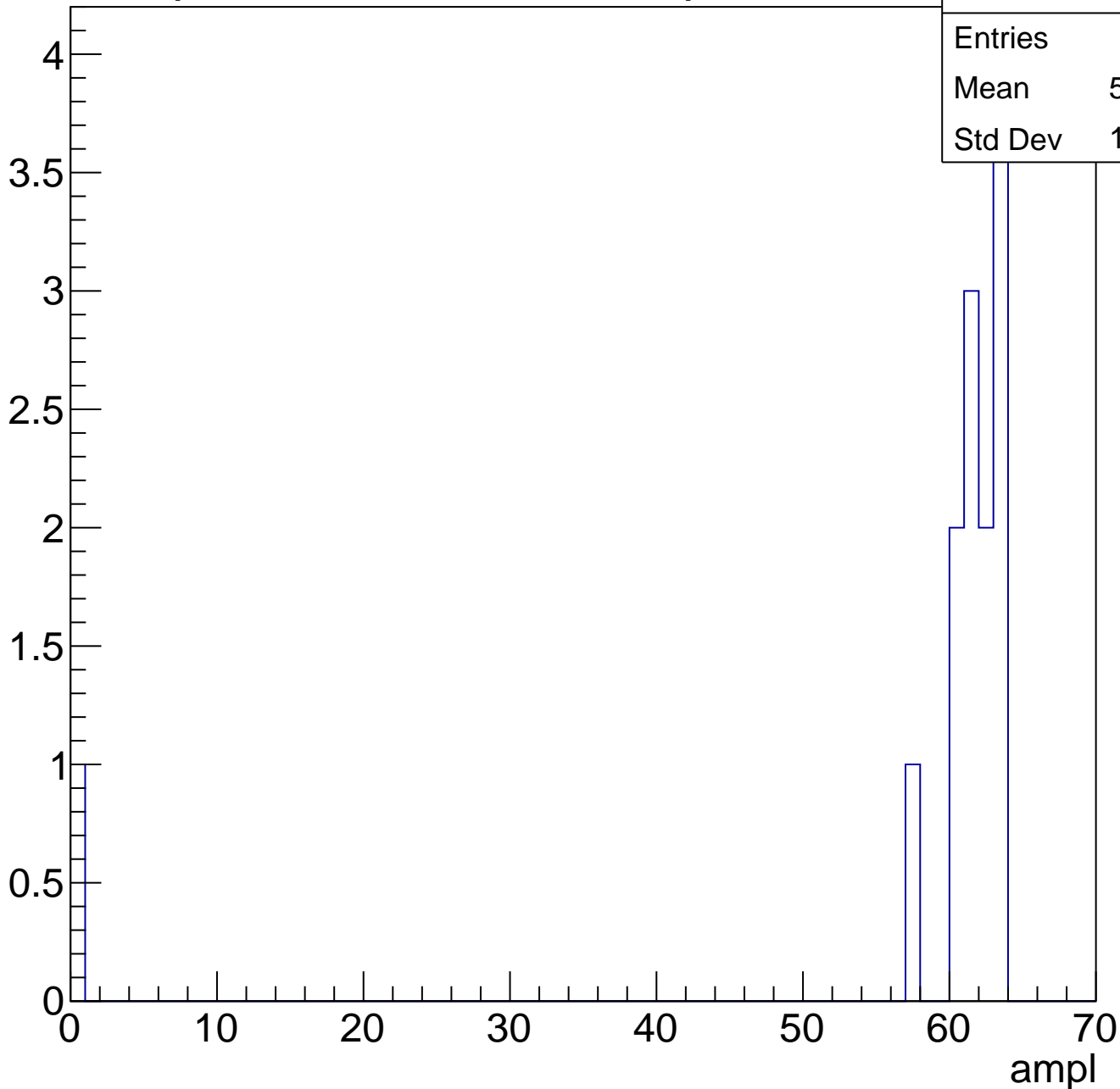
Entry



B1L103S, U14-ch64, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch64, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

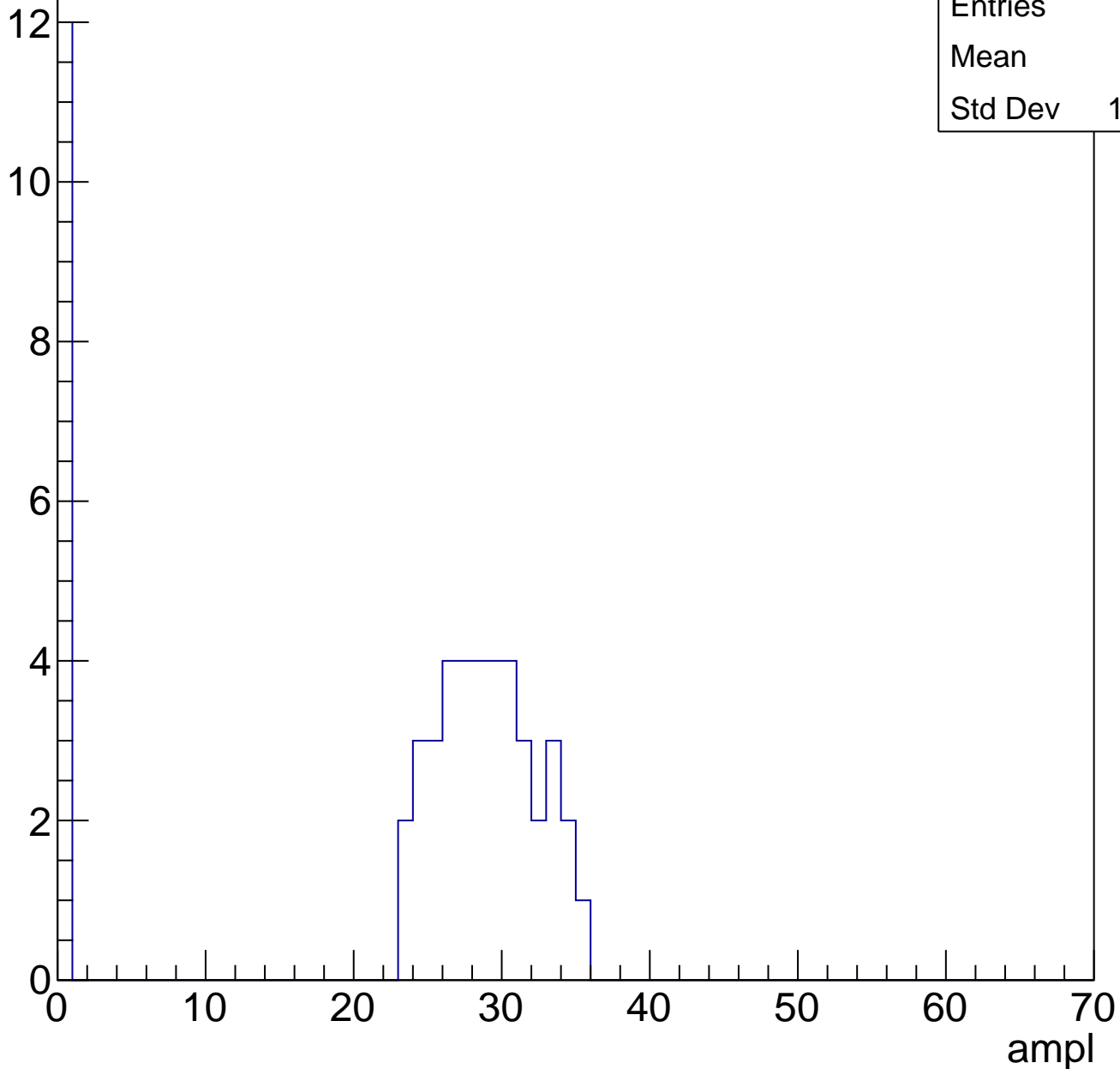
Entries	11
Mean	0
Std Dev	0

B1L103S, U14-ch65, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	51
Mean	21.8
Std Dev	12.42

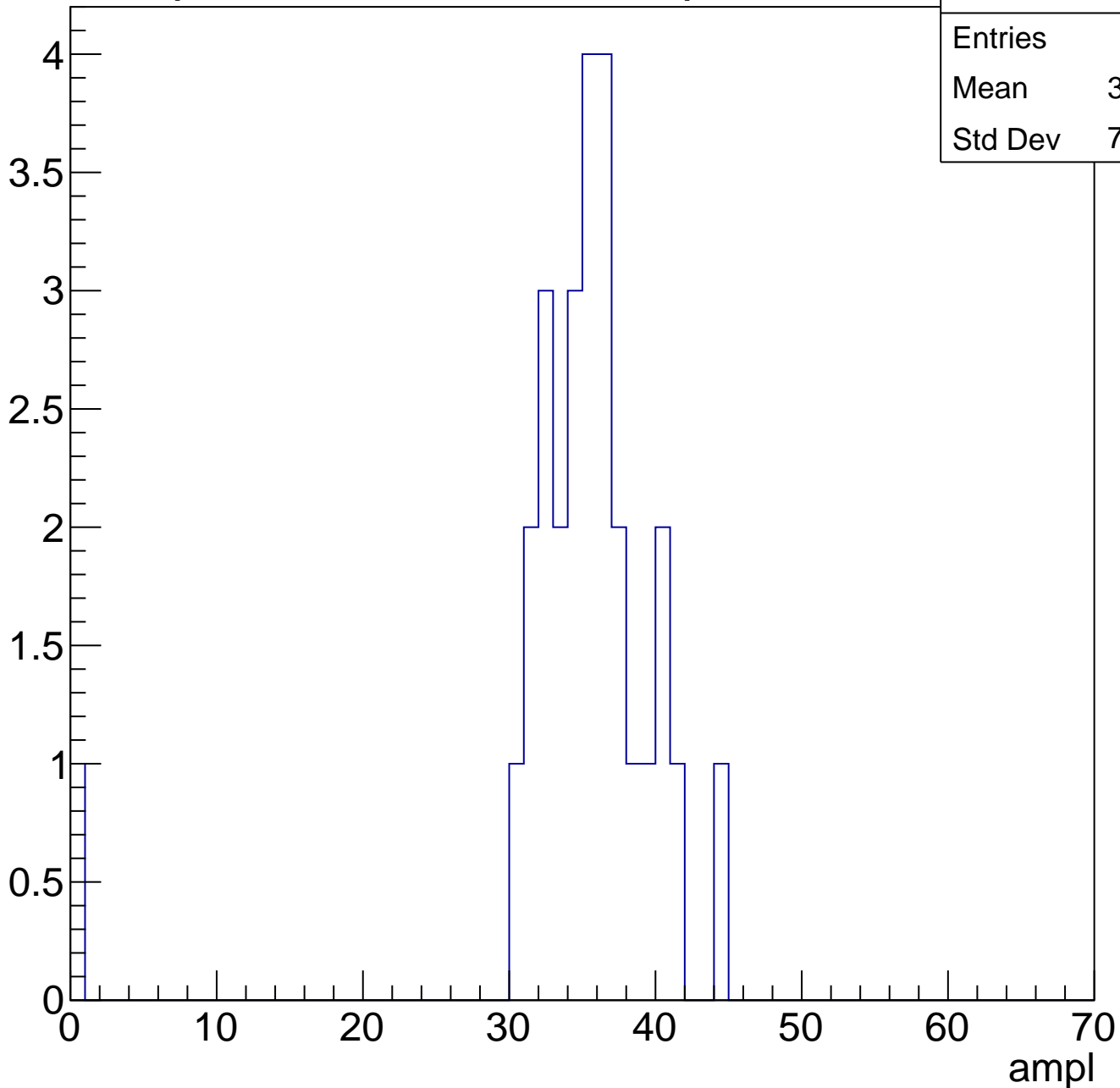
Entry



B1L103S, U14-ch65, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

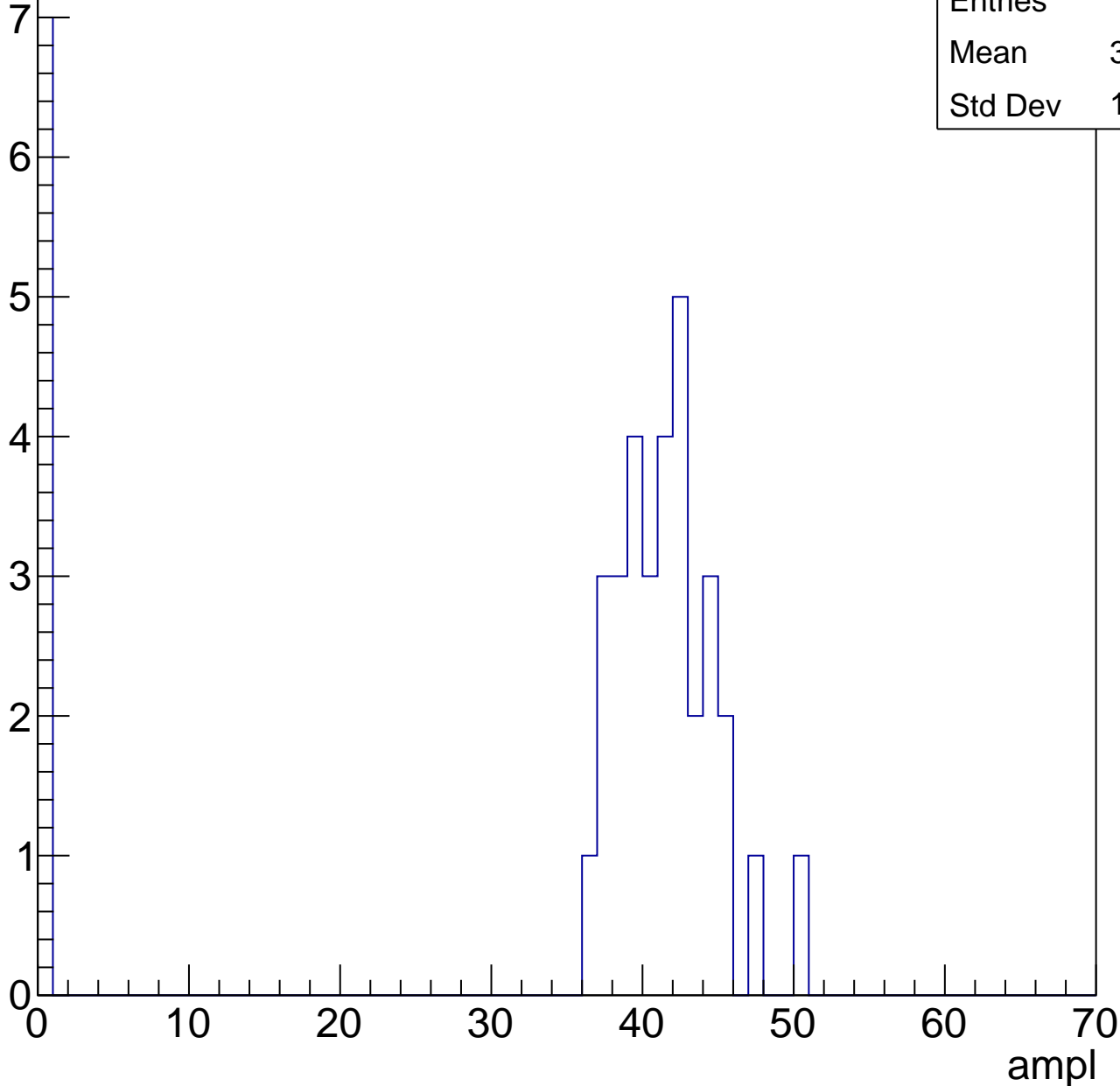


B1L103S, U14-ch65, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	33.74
Std Dev	16.03

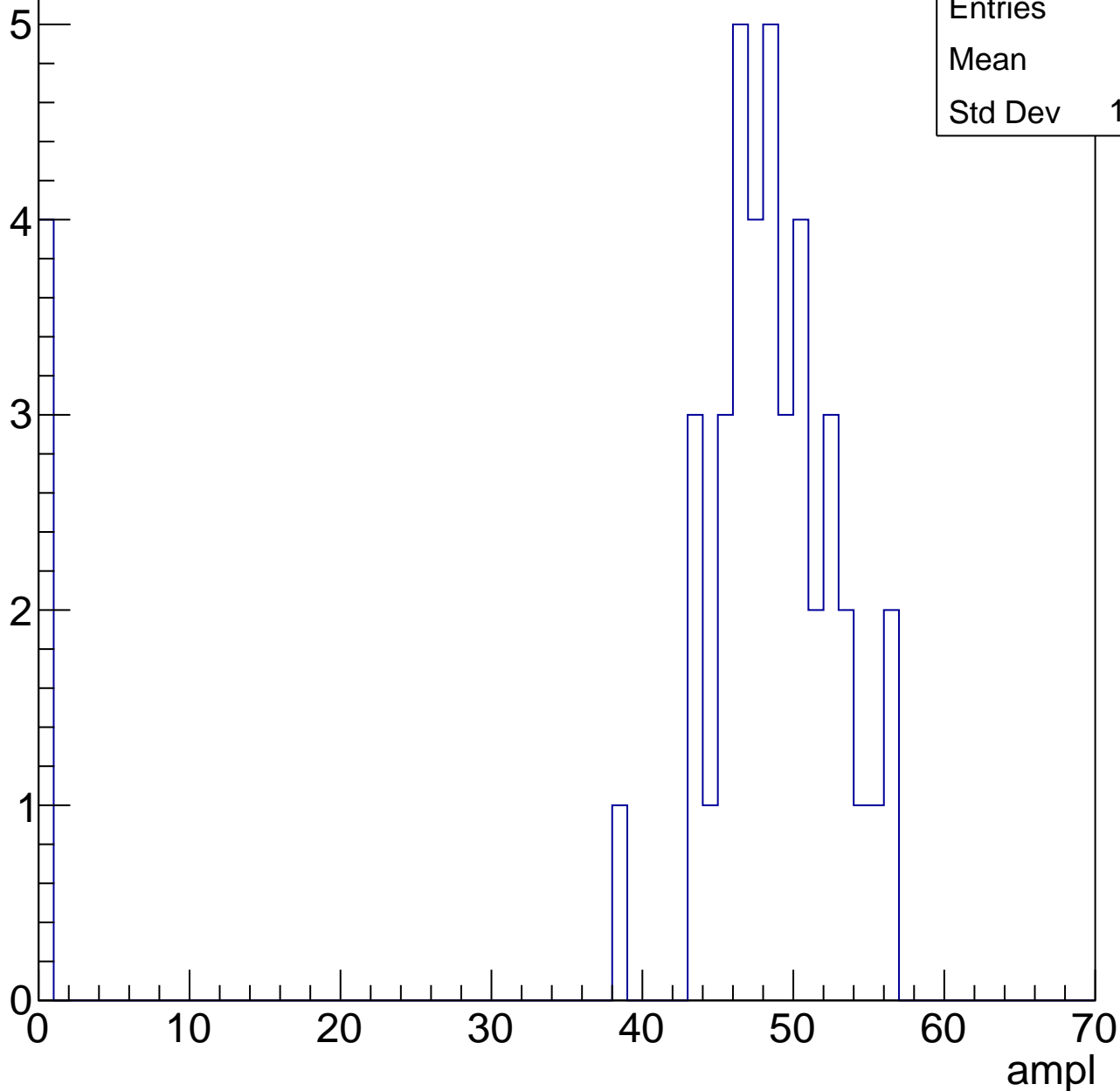


B1L103S, U14-ch65, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

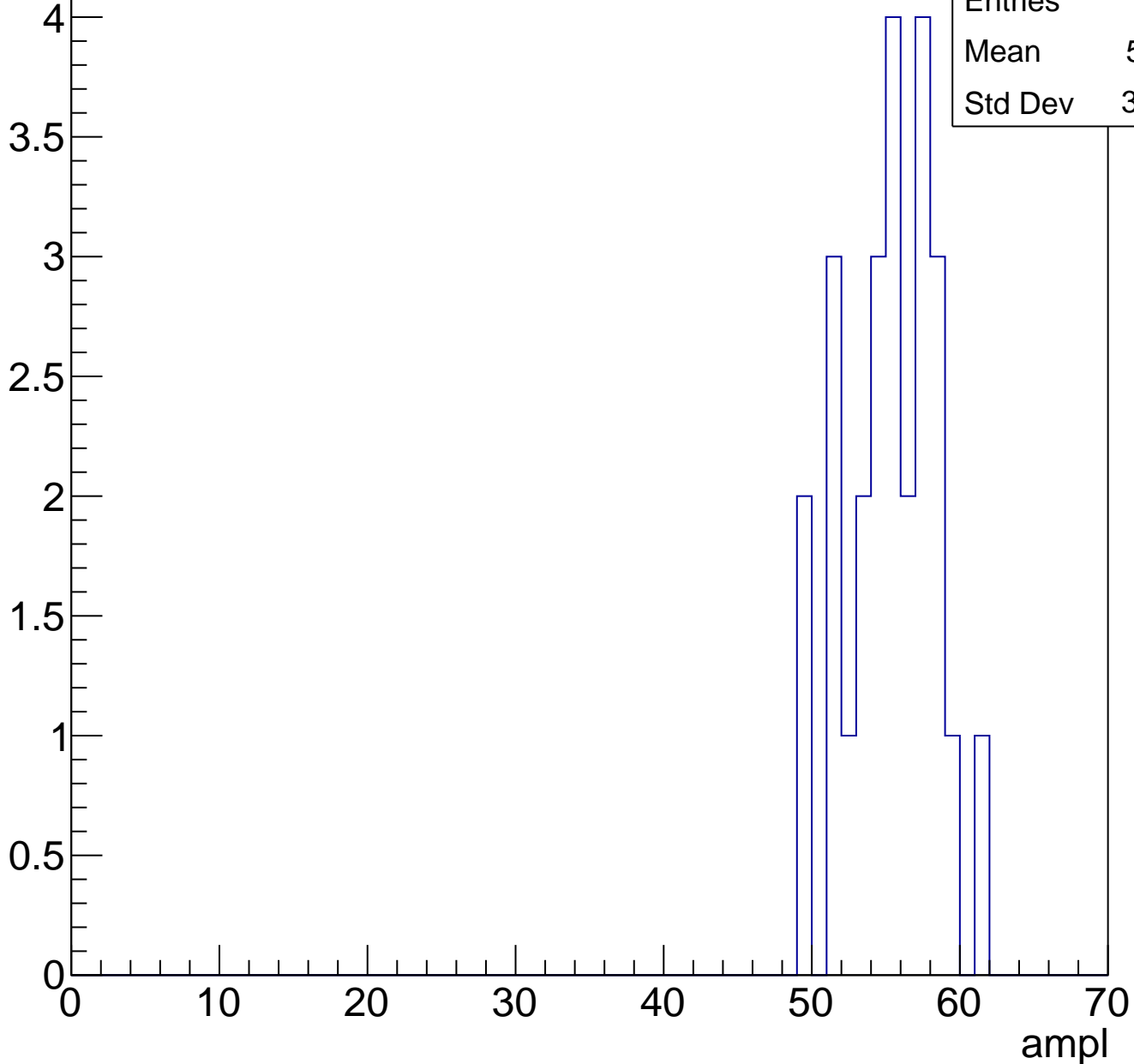
Entries	44
Mean	44
Std Dev	14.38



B1L103S, U14-ch65, adc4

calib_packv5_041523_1651.root, FC#0, port C2

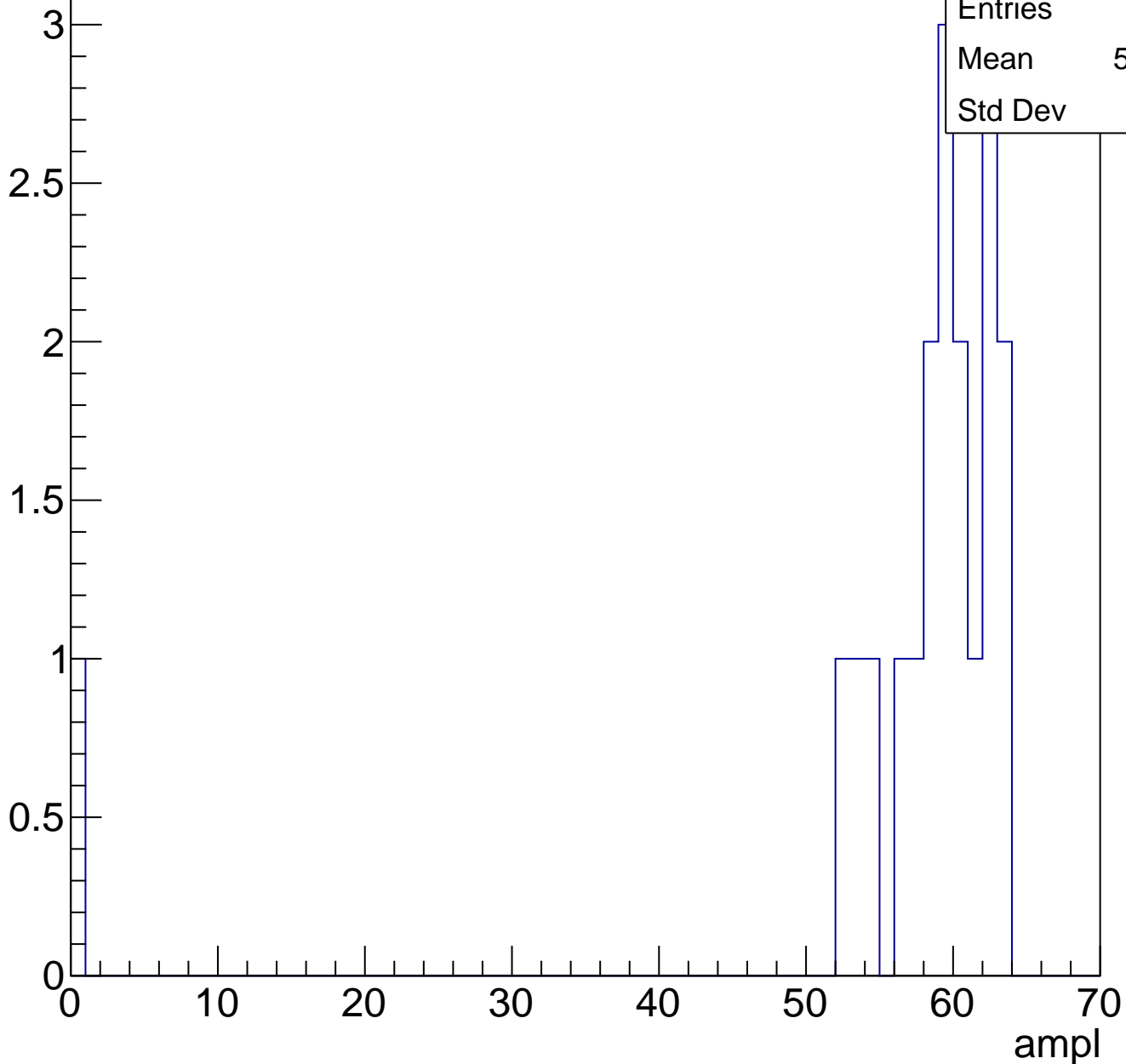
Entry



B1L103S, U14-ch65, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch65, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

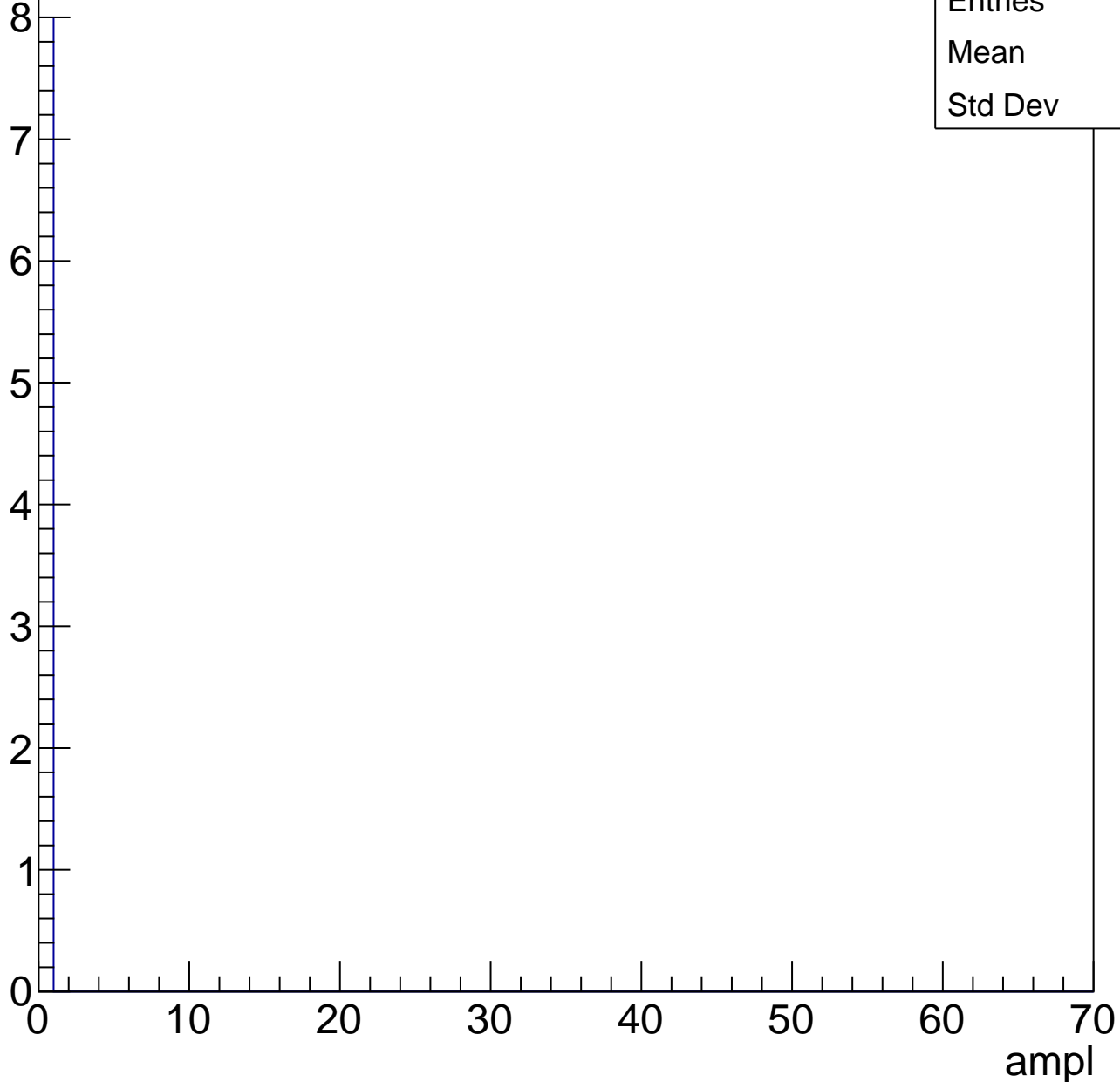
ampl

Entries	12
Mean	61.25
Std Dev	1.299

B1L103S, U14-ch65, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



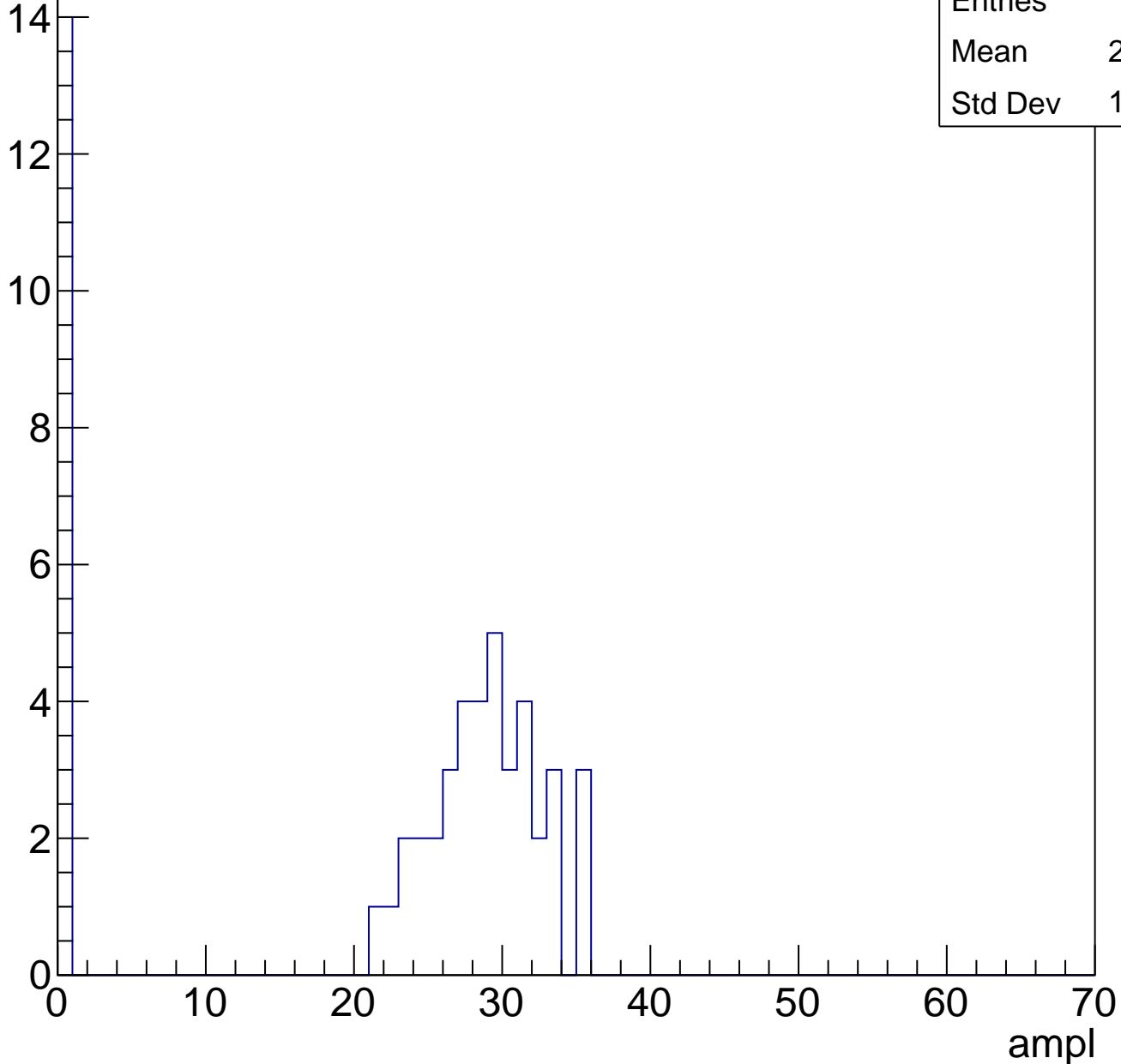
Entries	8
Mean	0
Std Dev	0

B1L103S, U14-ch66, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	53
Mean	20.98
Std Dev	12.94

Entry

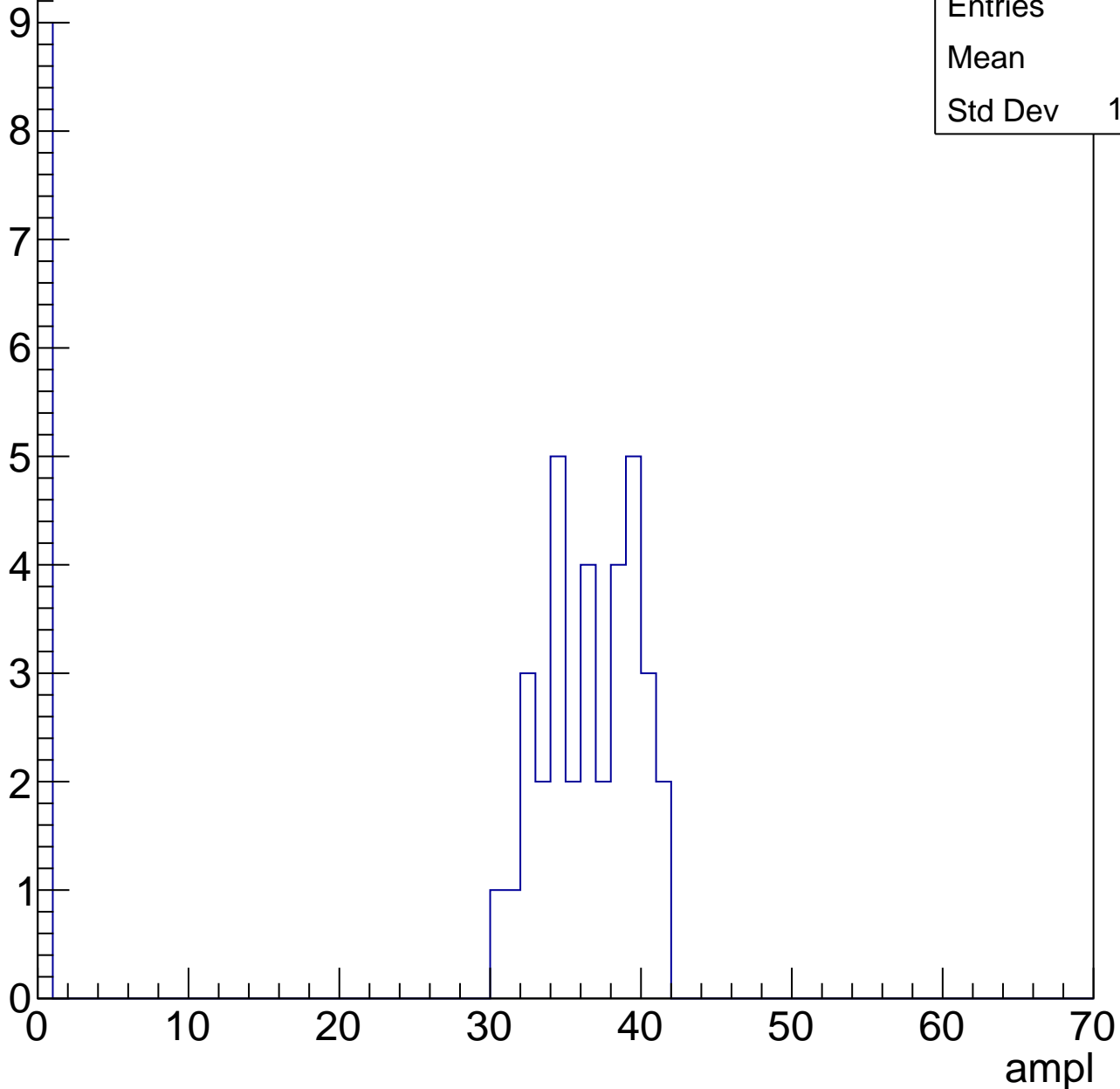


B1L103S, U14-ch66, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	43
Mean	28.6
Std Dev	14.96

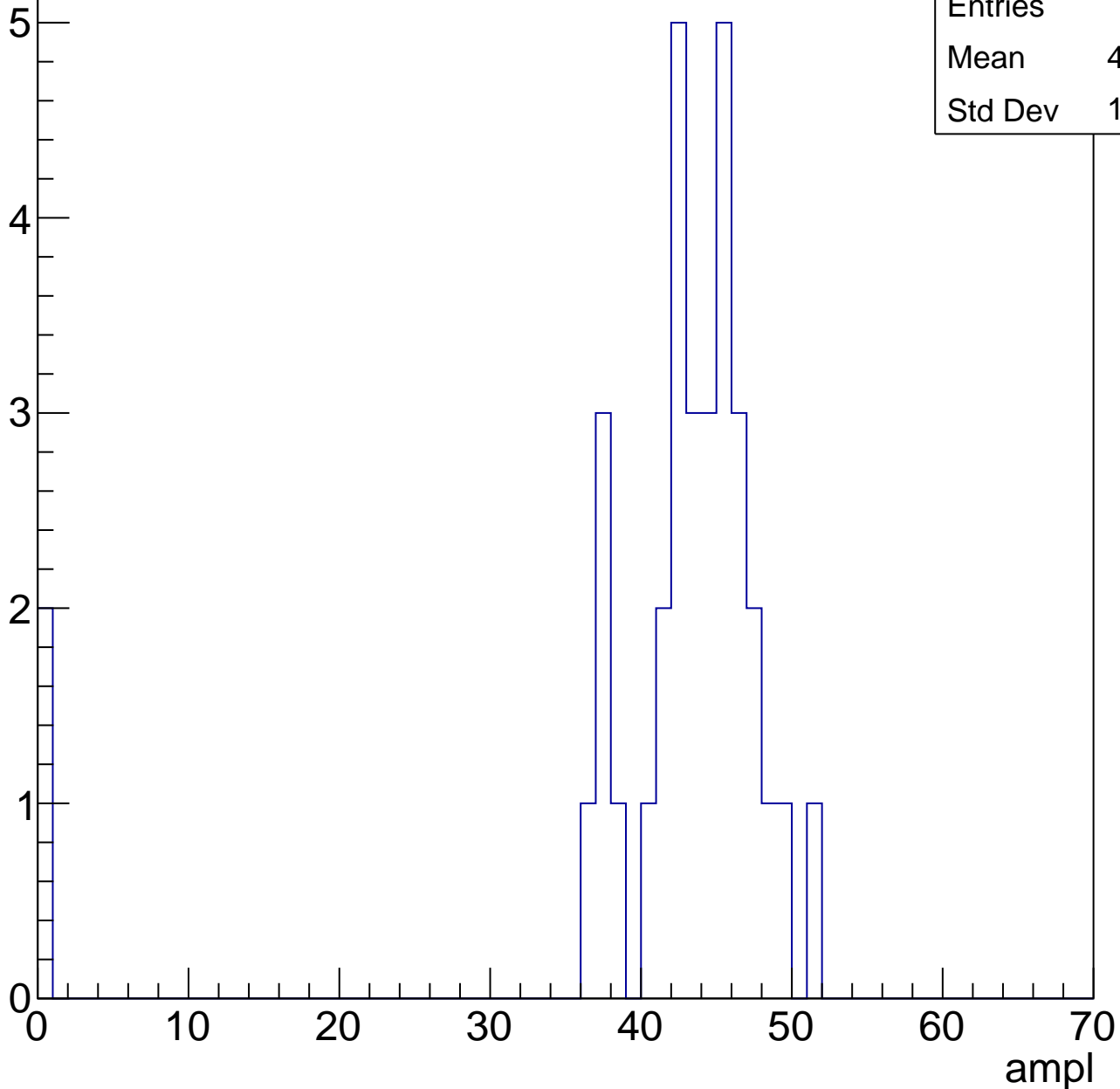


B1L103S, U14-ch66, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

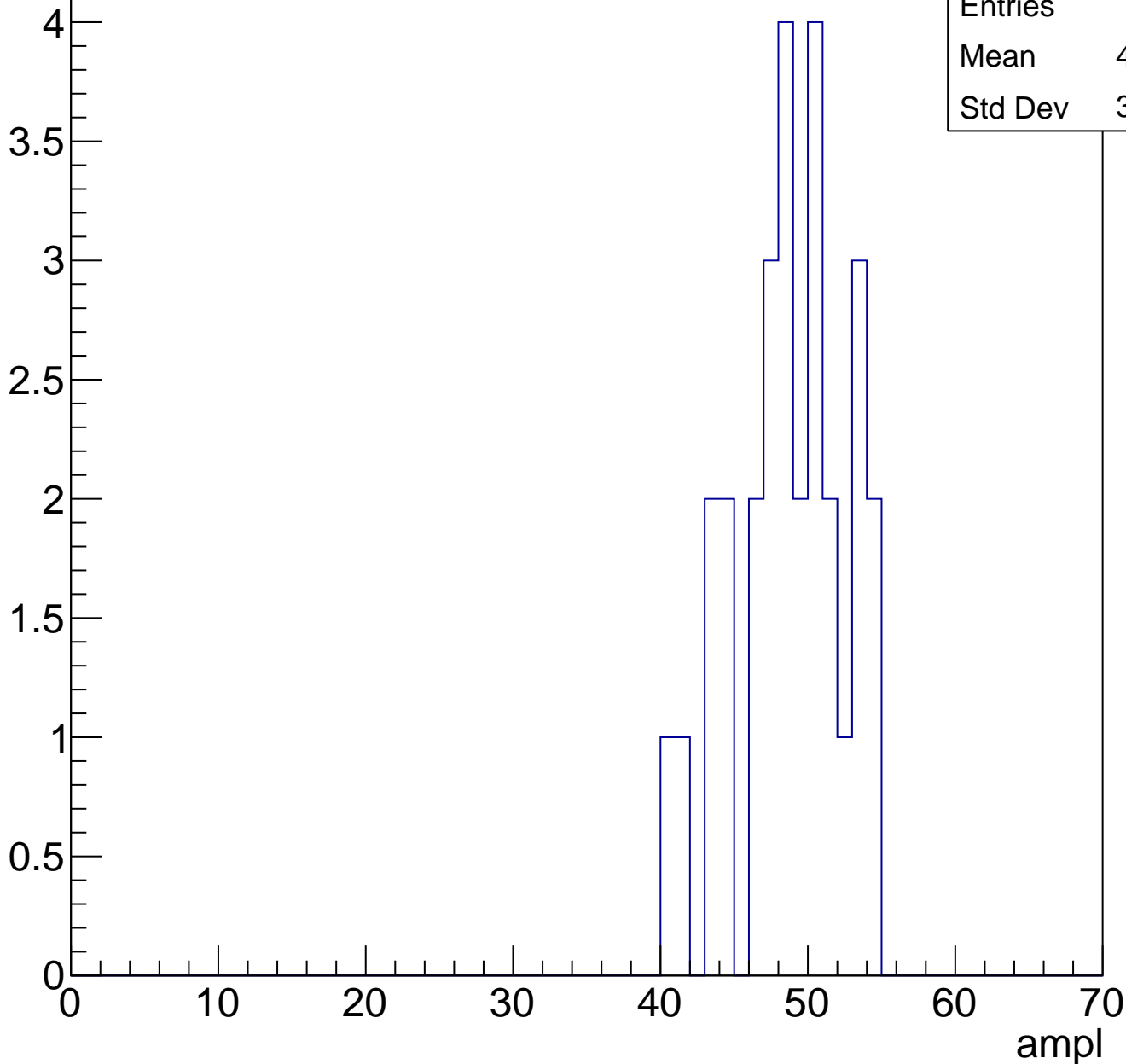
Entries	34
Mean	40.68
Std Dev	10.74



B1L103S, U14-ch66, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

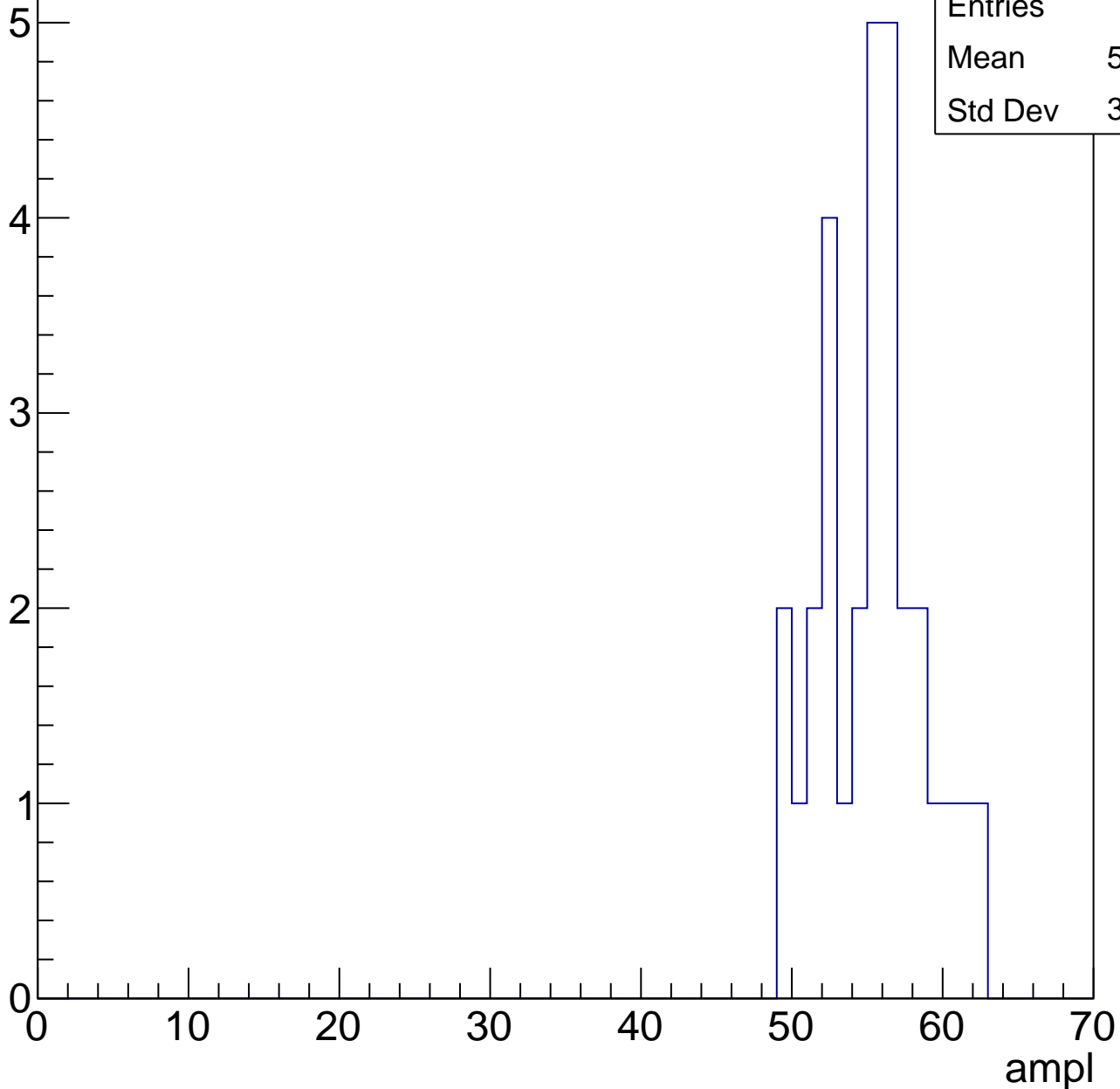


B1L103S, U14-ch66, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

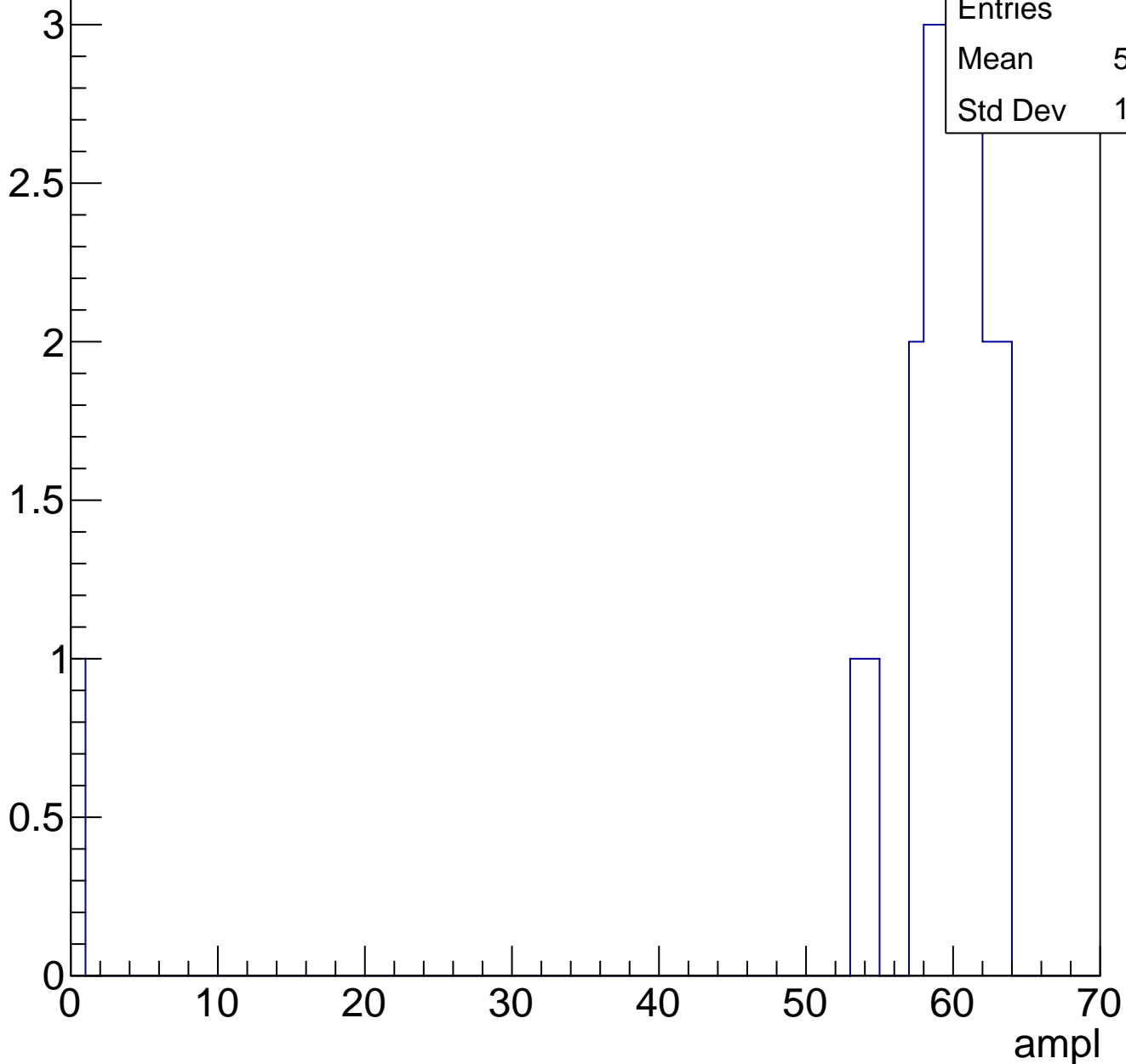
Entries	30
Mean	54.87
Std Dev	3.304



B1L103S, U14-ch66, adc5

calib_packv5_041523_1651.root, FC#0, port C2

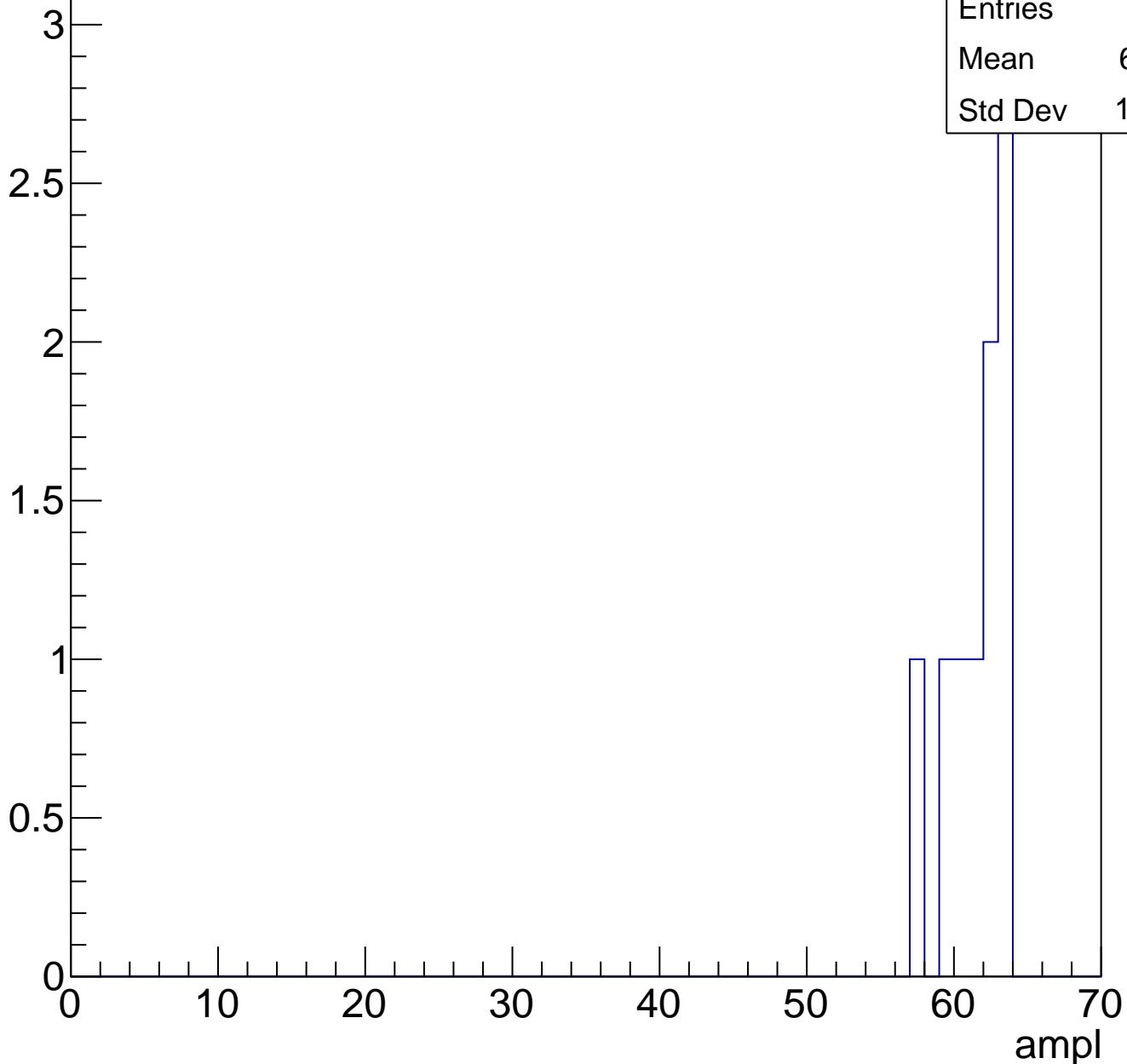
Entry



B1L103S, U14-ch66, adc6

calib_packv5_041523_1651.root, FC#0, port C2

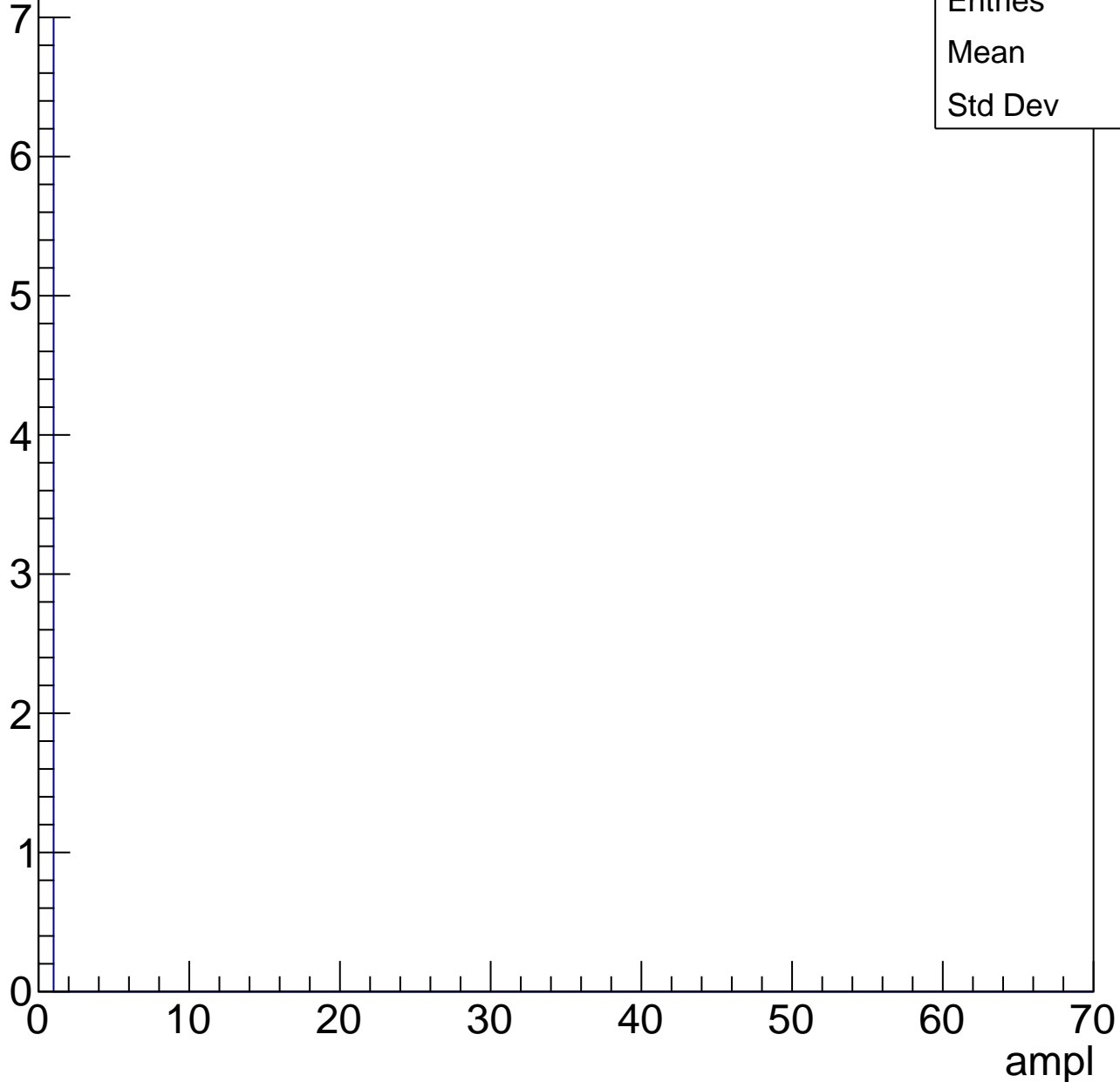
Entry



B1L103S, U14-ch66, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



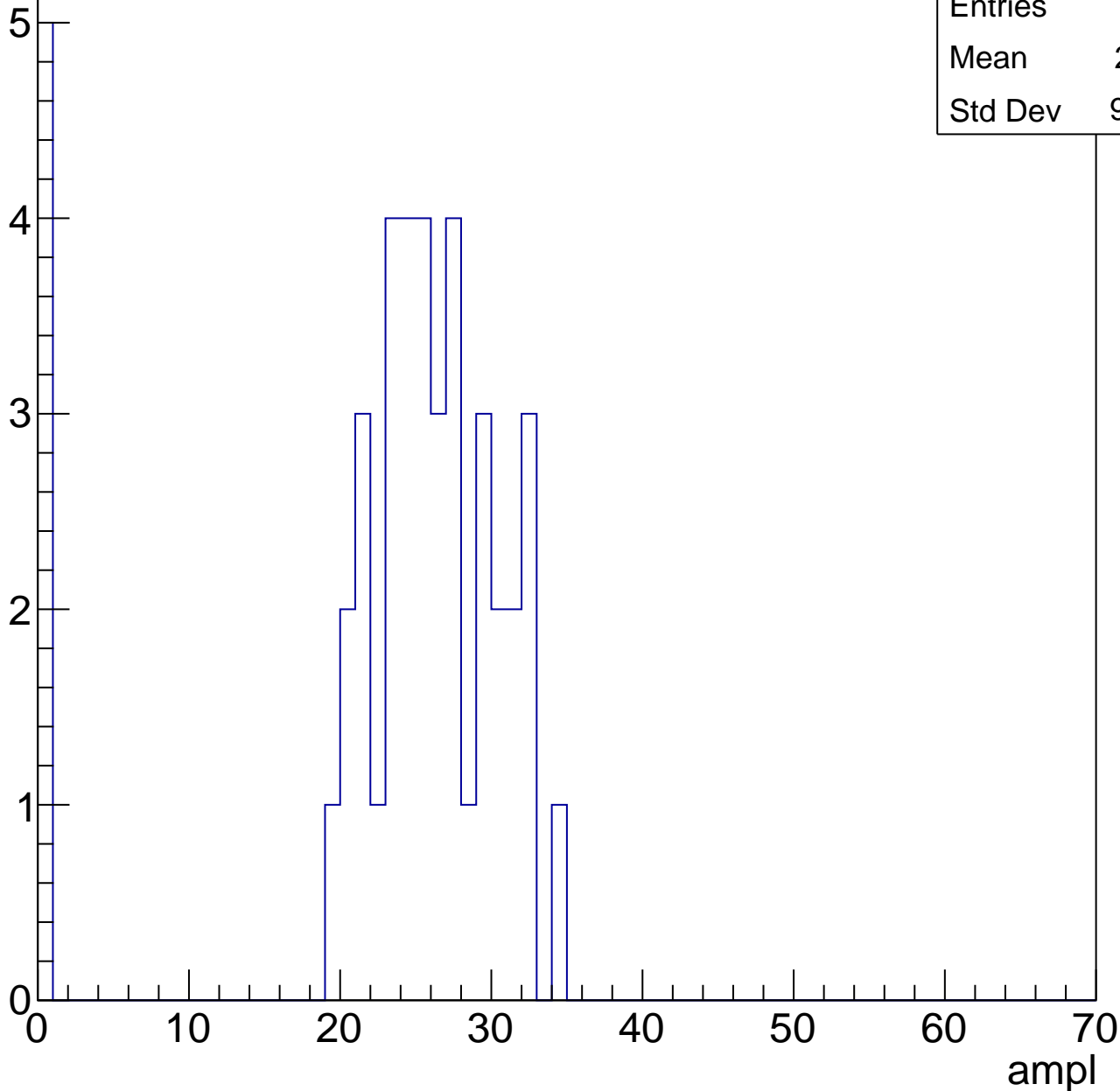
Entries	7
Mean	0
Std Dev	0

B1L103S, U14-ch67, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	43
Mean	22.91
Std Dev	9.055



B1L103S, U14-ch67, adc1

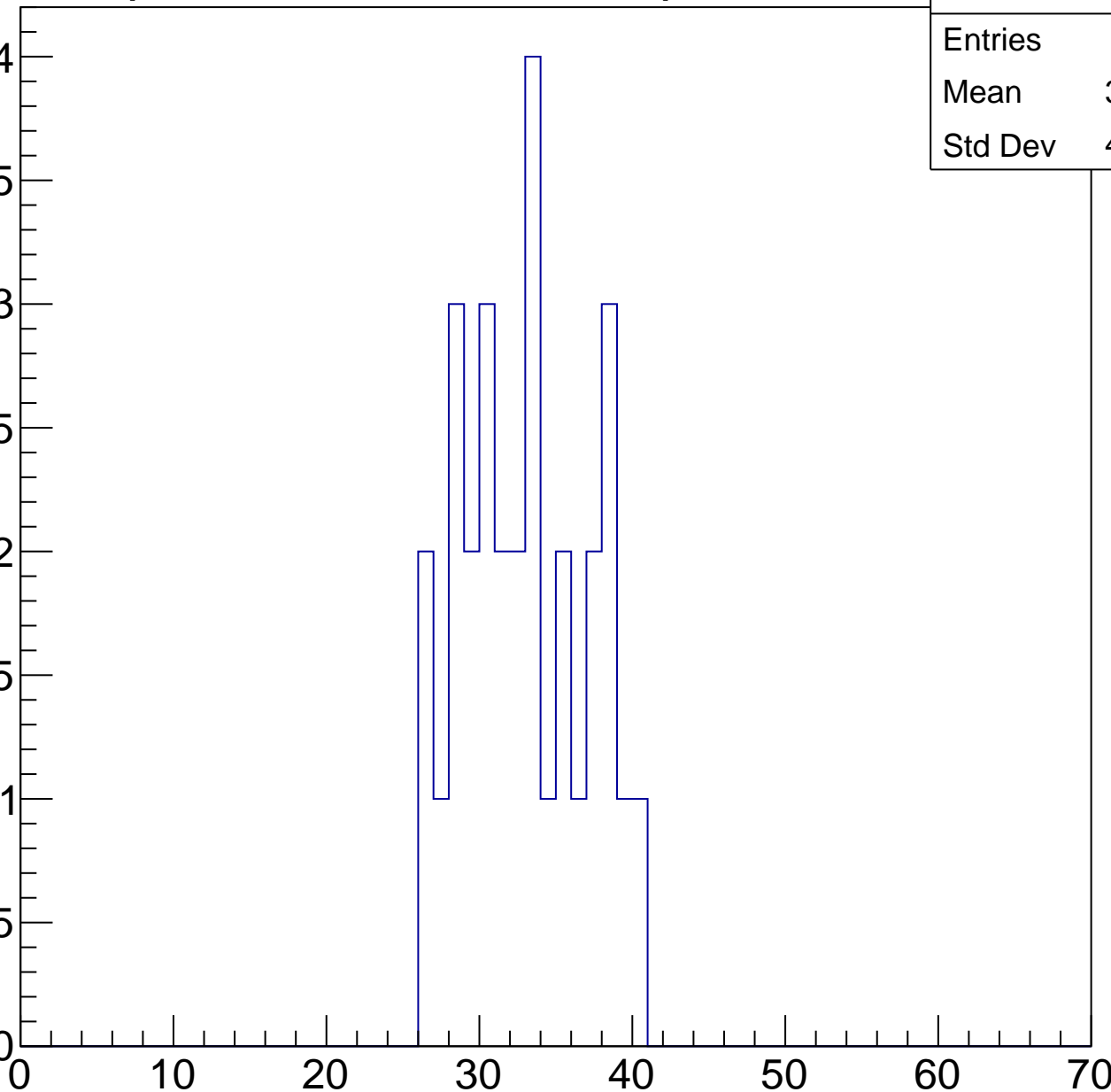
calib_packv5_041523_1651.root, FC#0, port C2

Entry

4
3.5
3
2.5
2
1.5
1
0.5
0

Entries	30
Mean	32.53
Std Dev	4.006

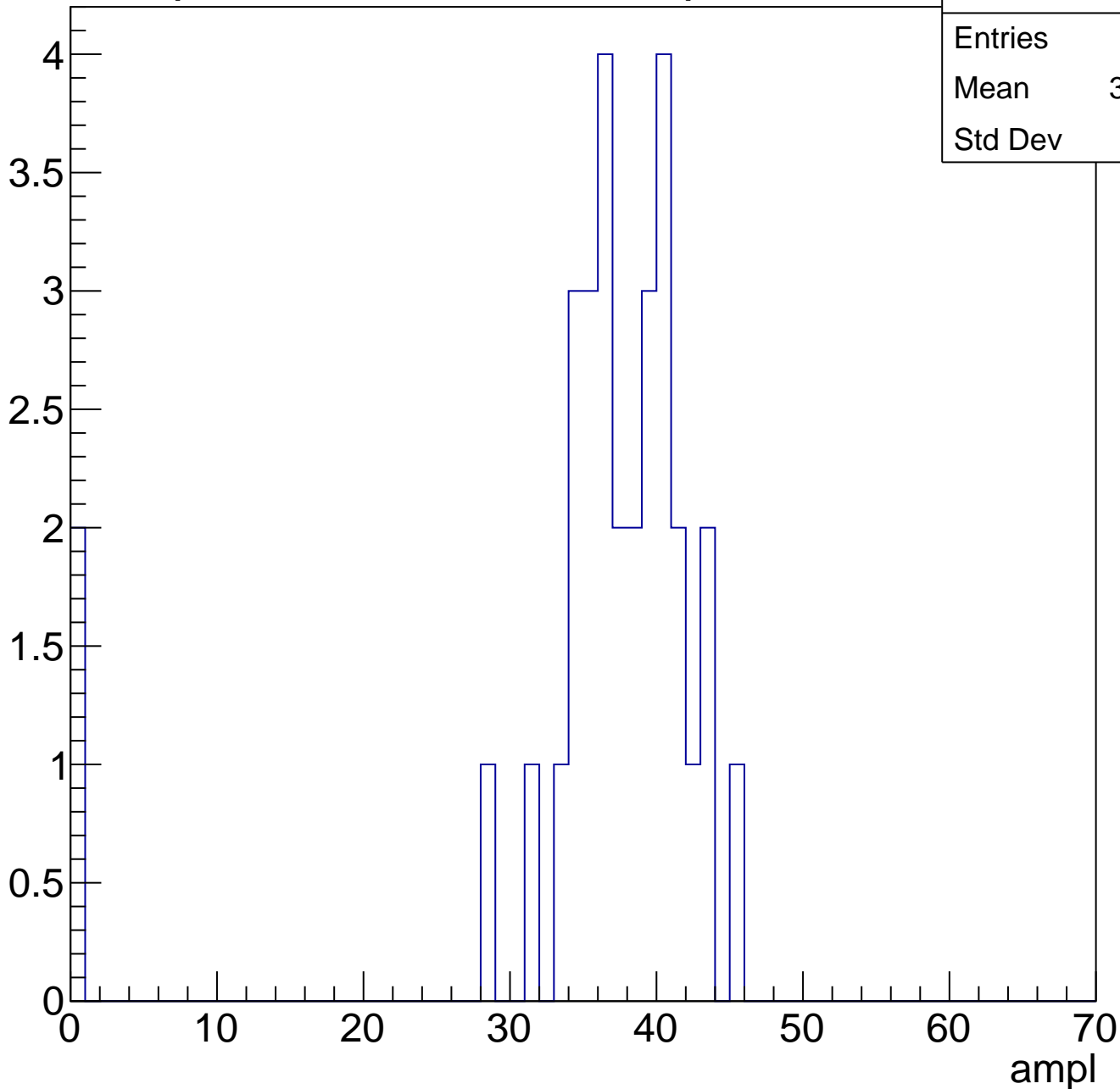
ampl



B1L103S, U14-ch67, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

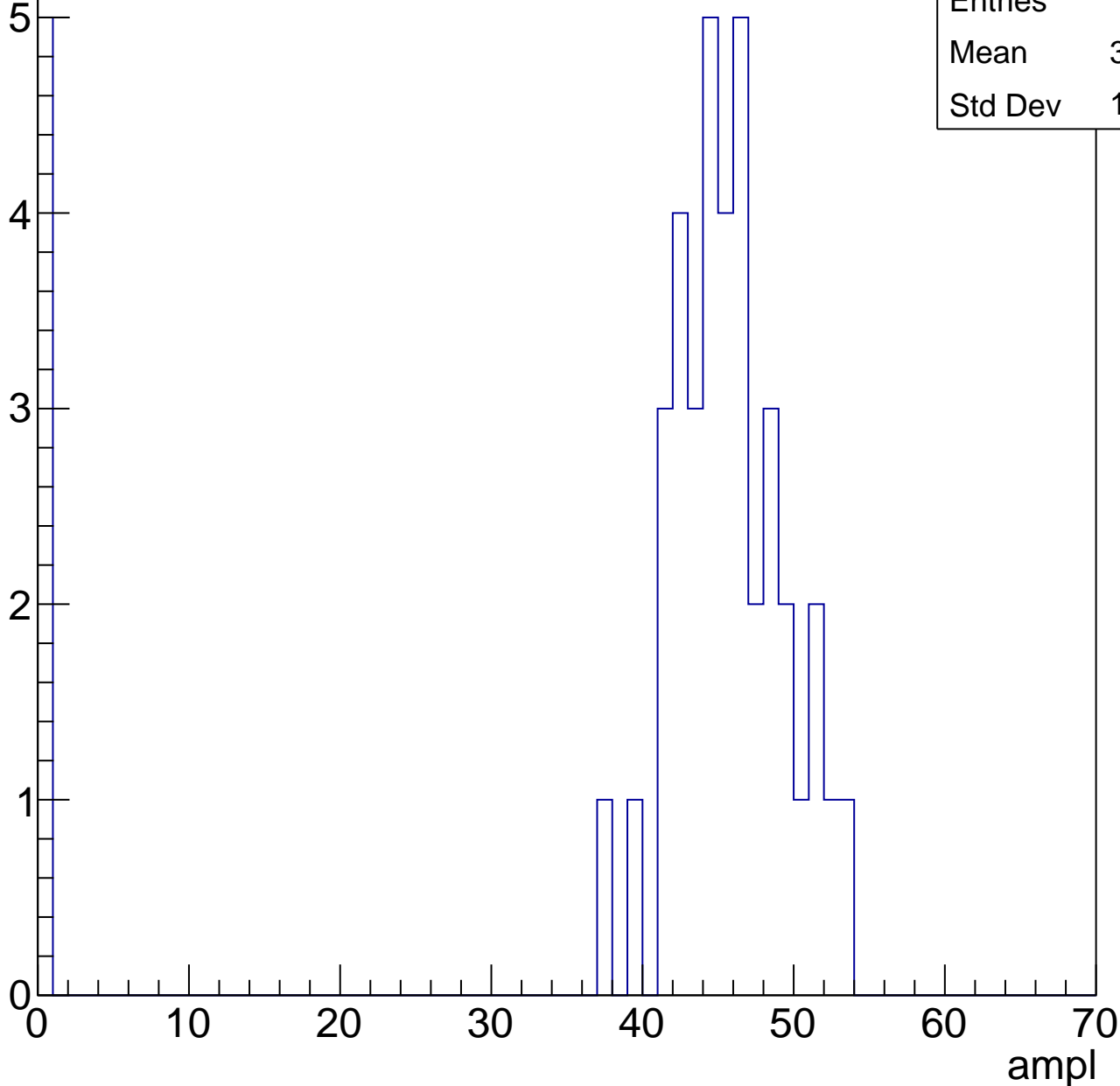


B1L103S, U14-ch67, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	43
Mean	39.98
Std Dev	14.88



B1L103S, U14-ch67, adc4

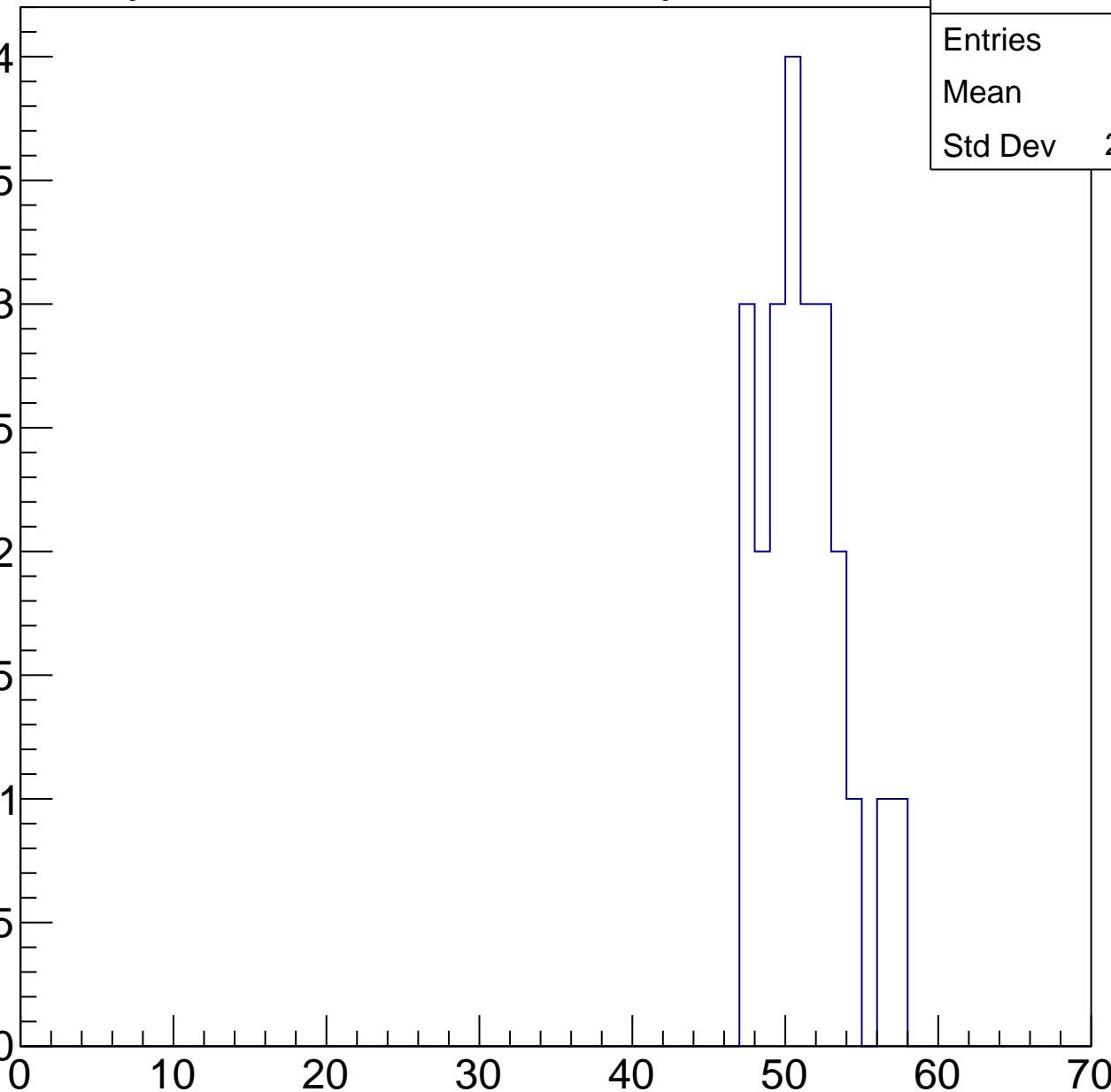
calib_packv5_041523_1651.root, FC#0, port C2

Entry

4
3.5
3
2.5
2
1.5
1
0.5
0

Entries	23
Mean	50.7
Std Dev	2.645

ampl

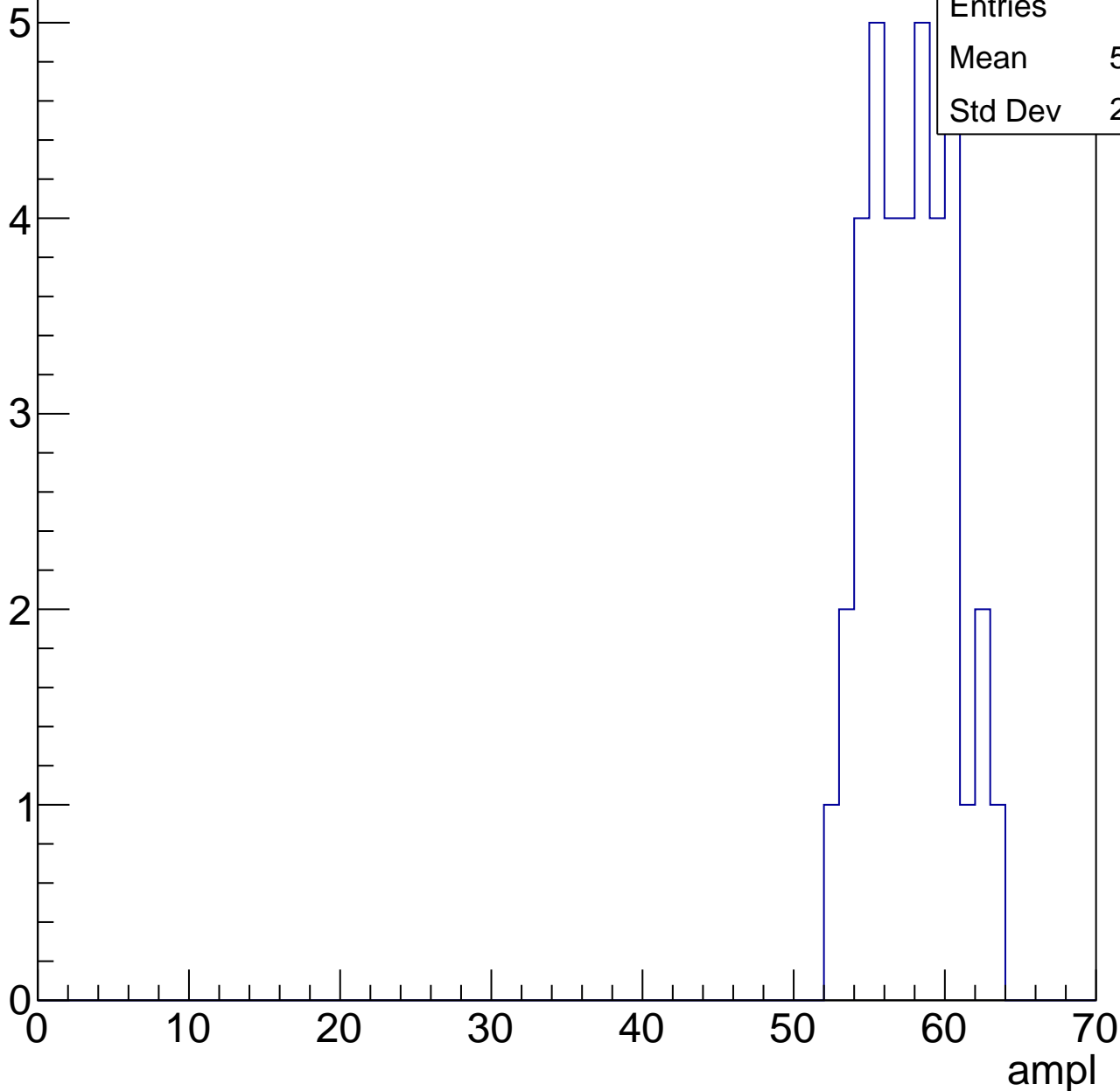


B1L103S, U14-ch67, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

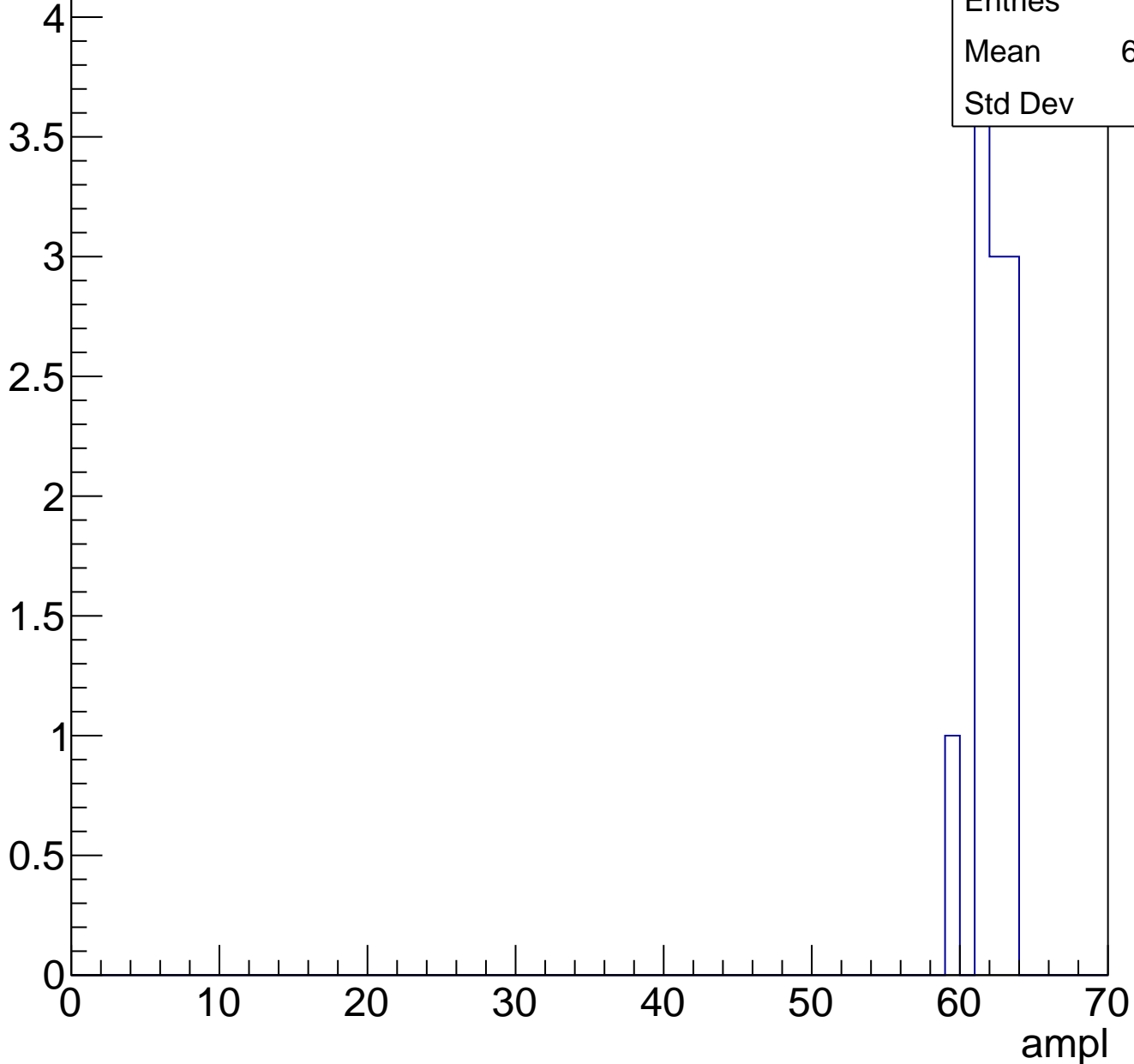
Entries	38
Mean	57.24
Std Dev	2.728



B1L103S, U14-ch67, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

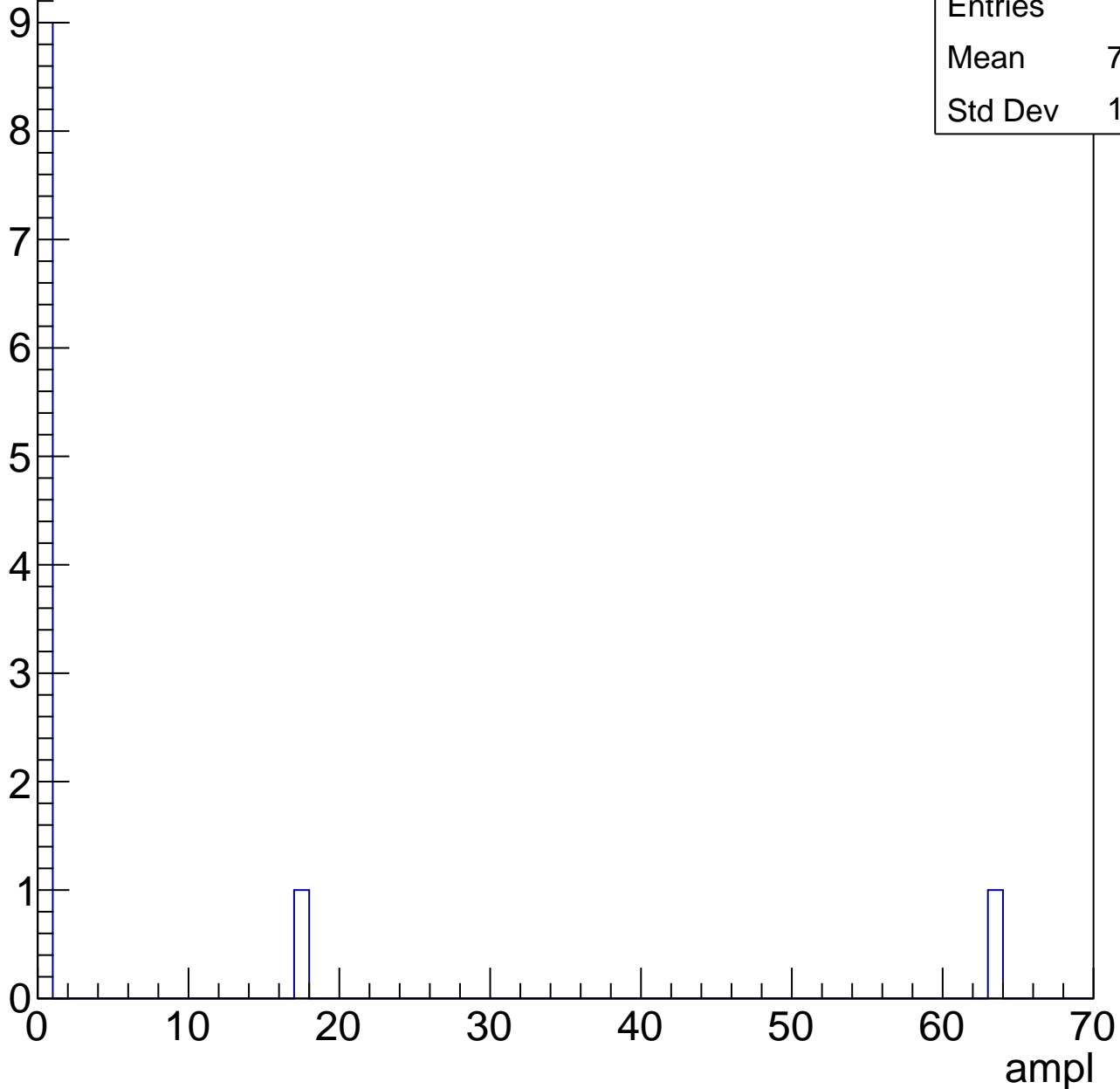


B1L103S, U14-ch67, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	11
Mean	7.273
Std Dev	18.28

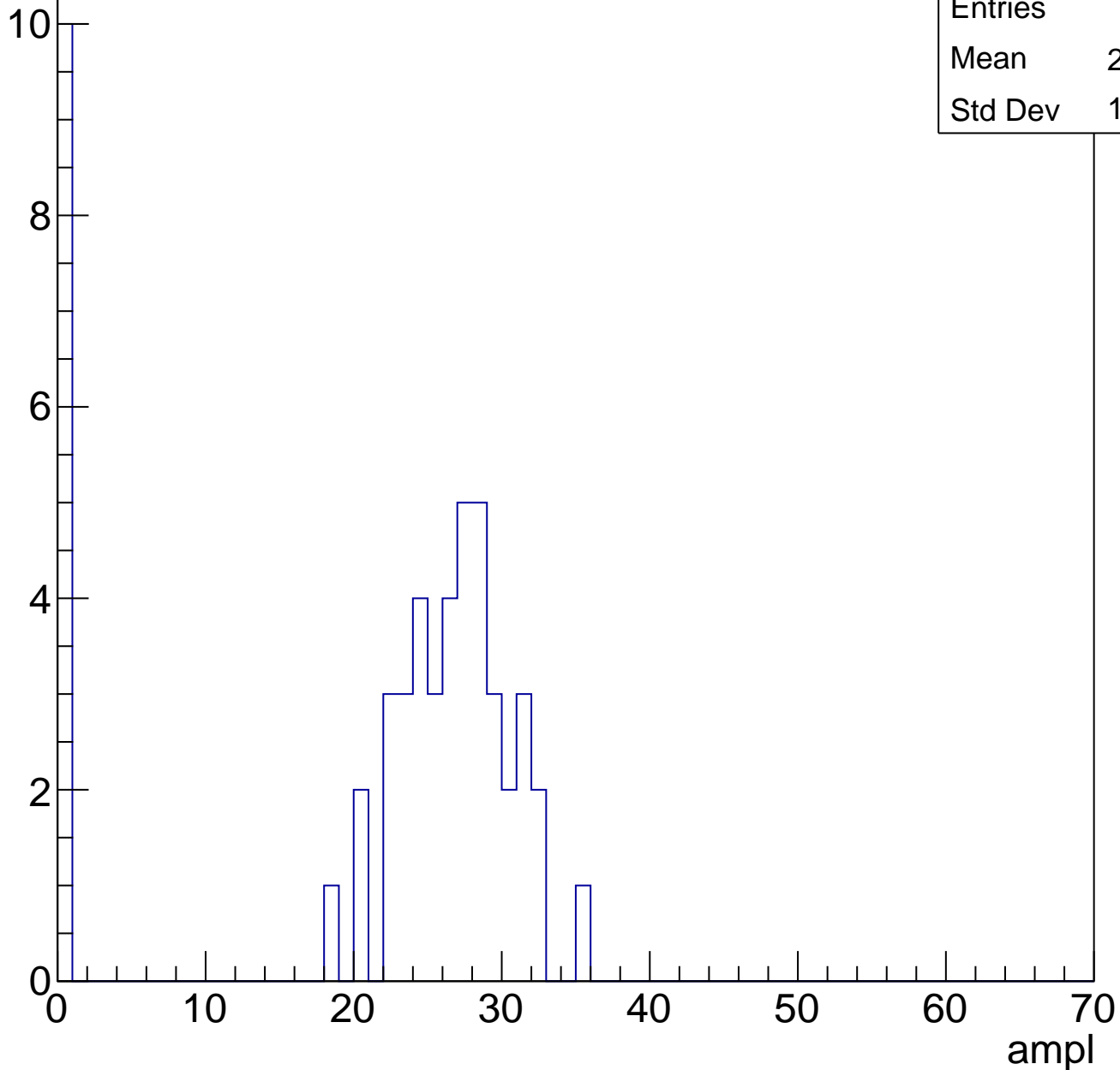


B1L103S, U14-ch68, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	51
Mean	21.22
Std Dev	10.97

Entry

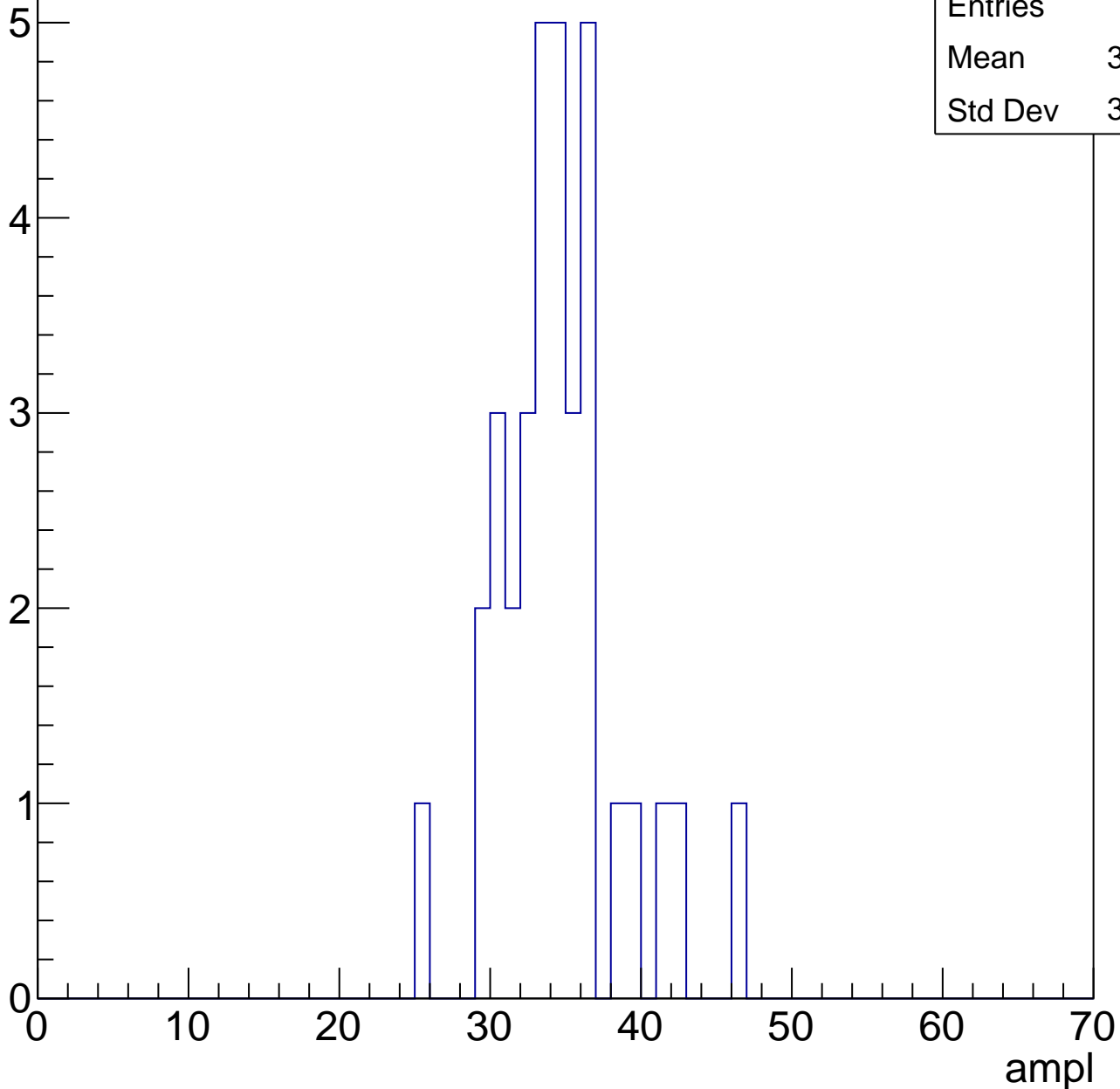


B1L103S, U14-ch68, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	34
Mean	34.03
Std Dev	3.967

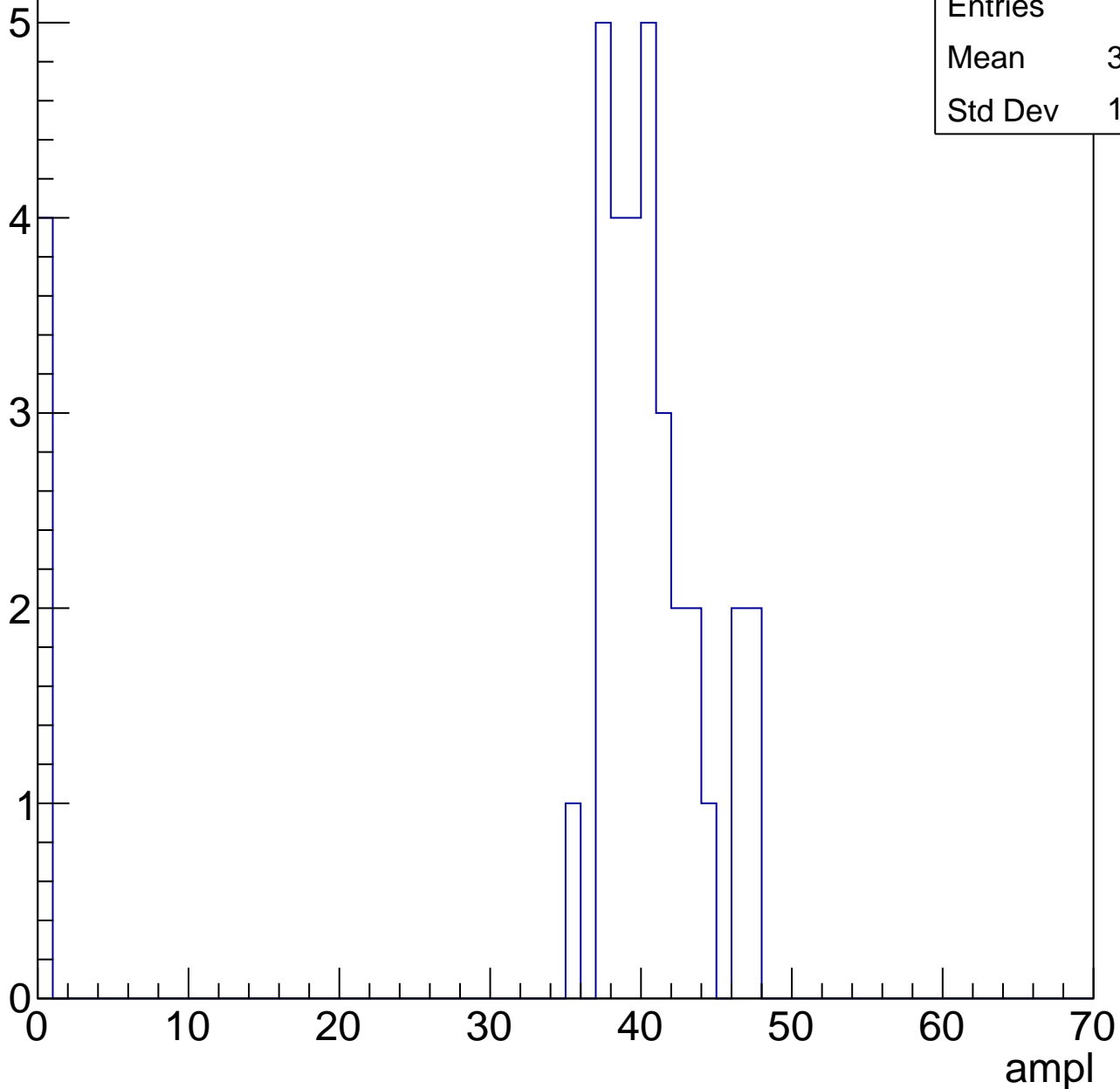


B1L103S, U14-ch68, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	35
Mean	35.74
Std Dev	13.17

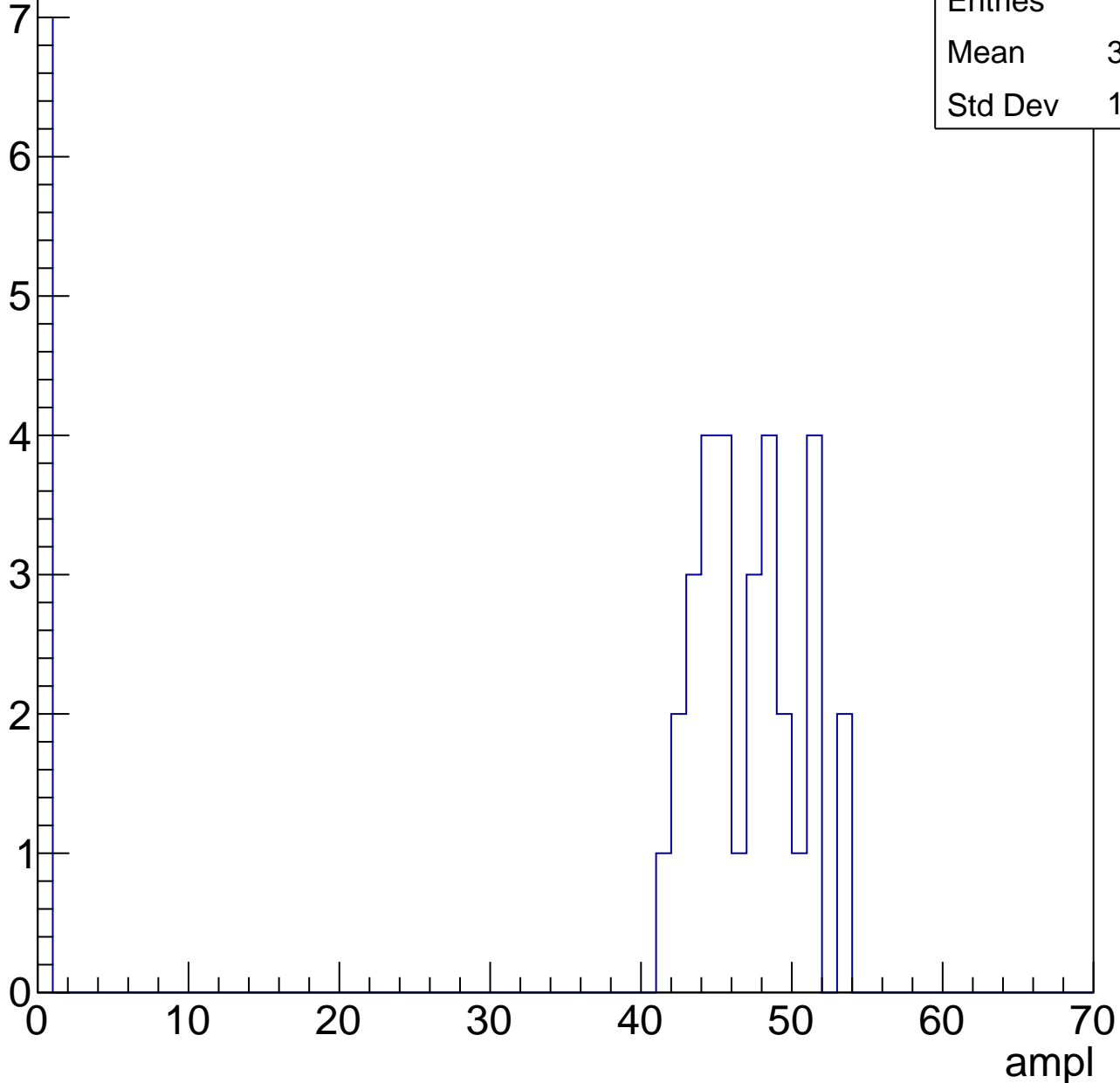


B1L103S, U14-ch68, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	38
Mean	38.08
Std Dev	18.34

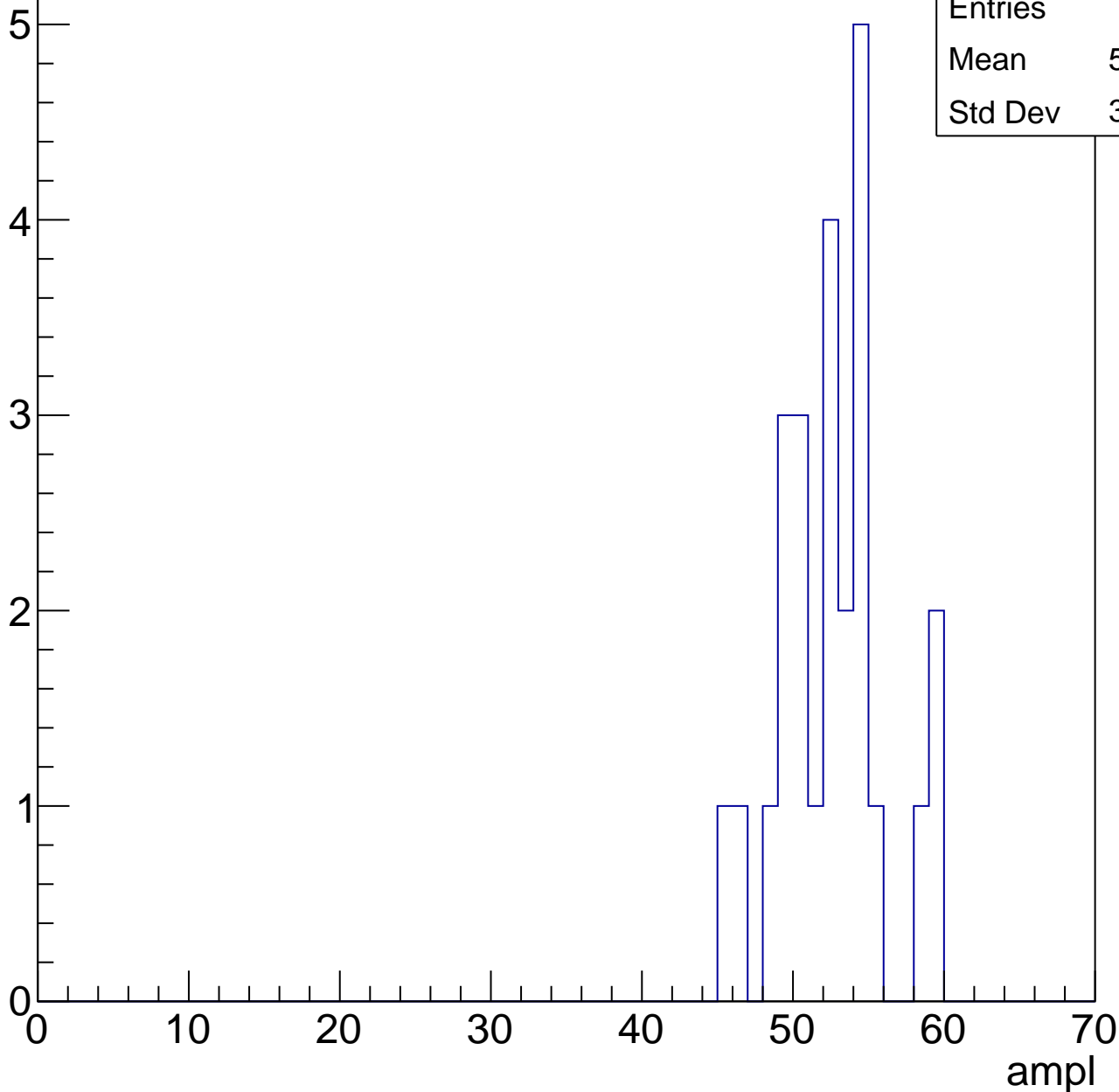


B1L103S, U14-ch68, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	25
Mean	52.08
Std Dev	3.498

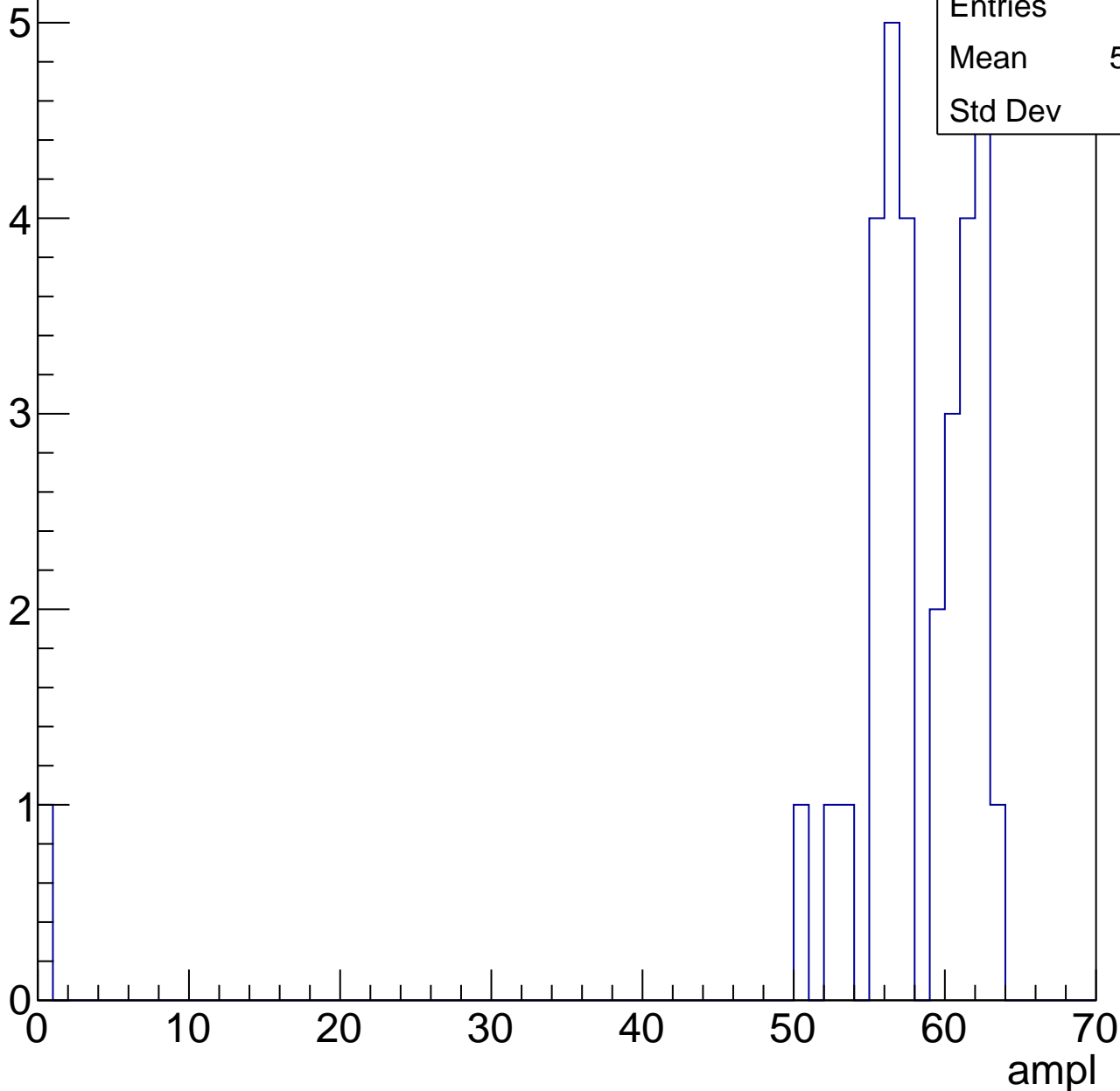


B1L103S, U14-ch68, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

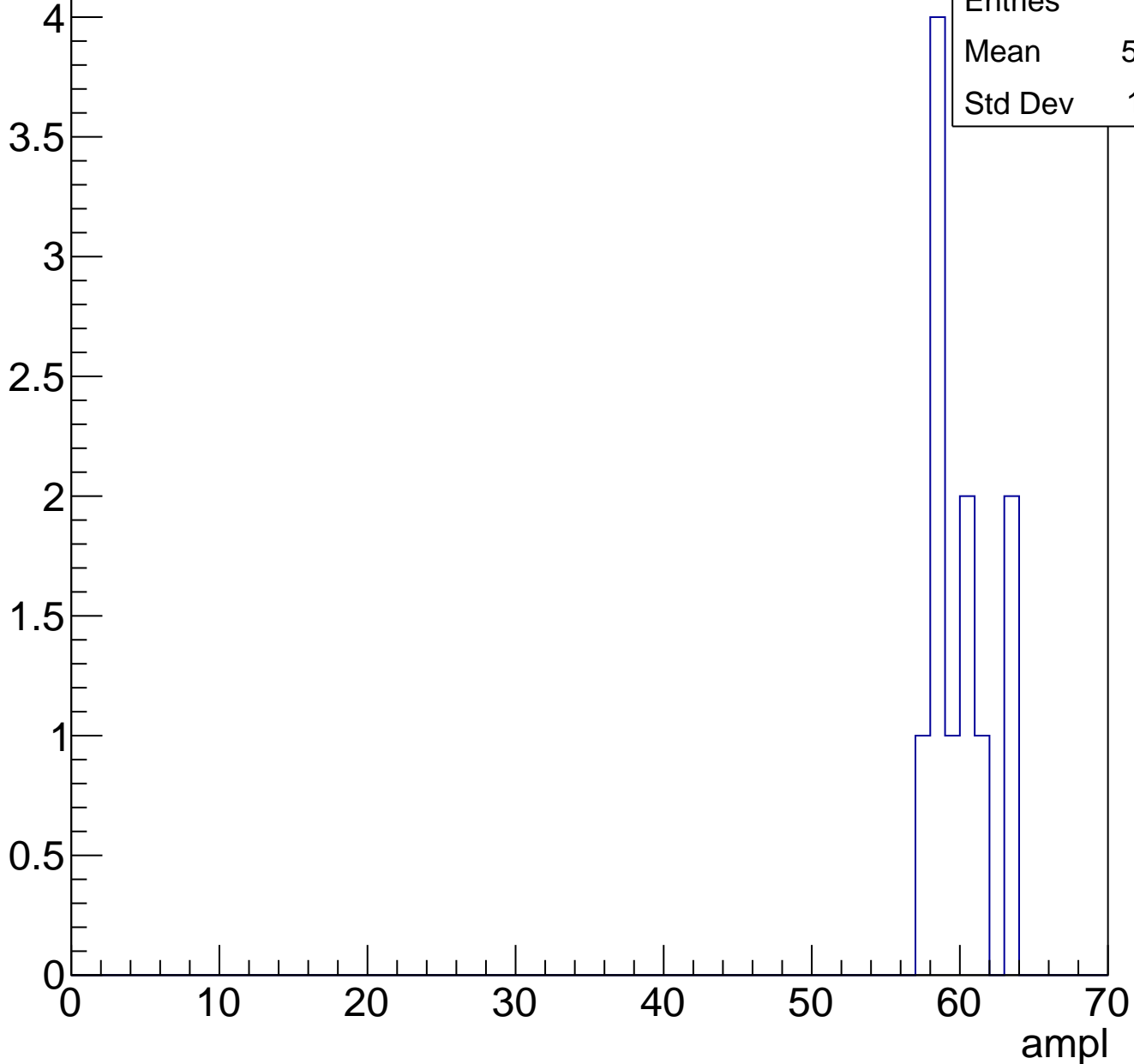
Entries	32
Mean	56.19
Std Dev	10.6



B1L103S, U14-ch68, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

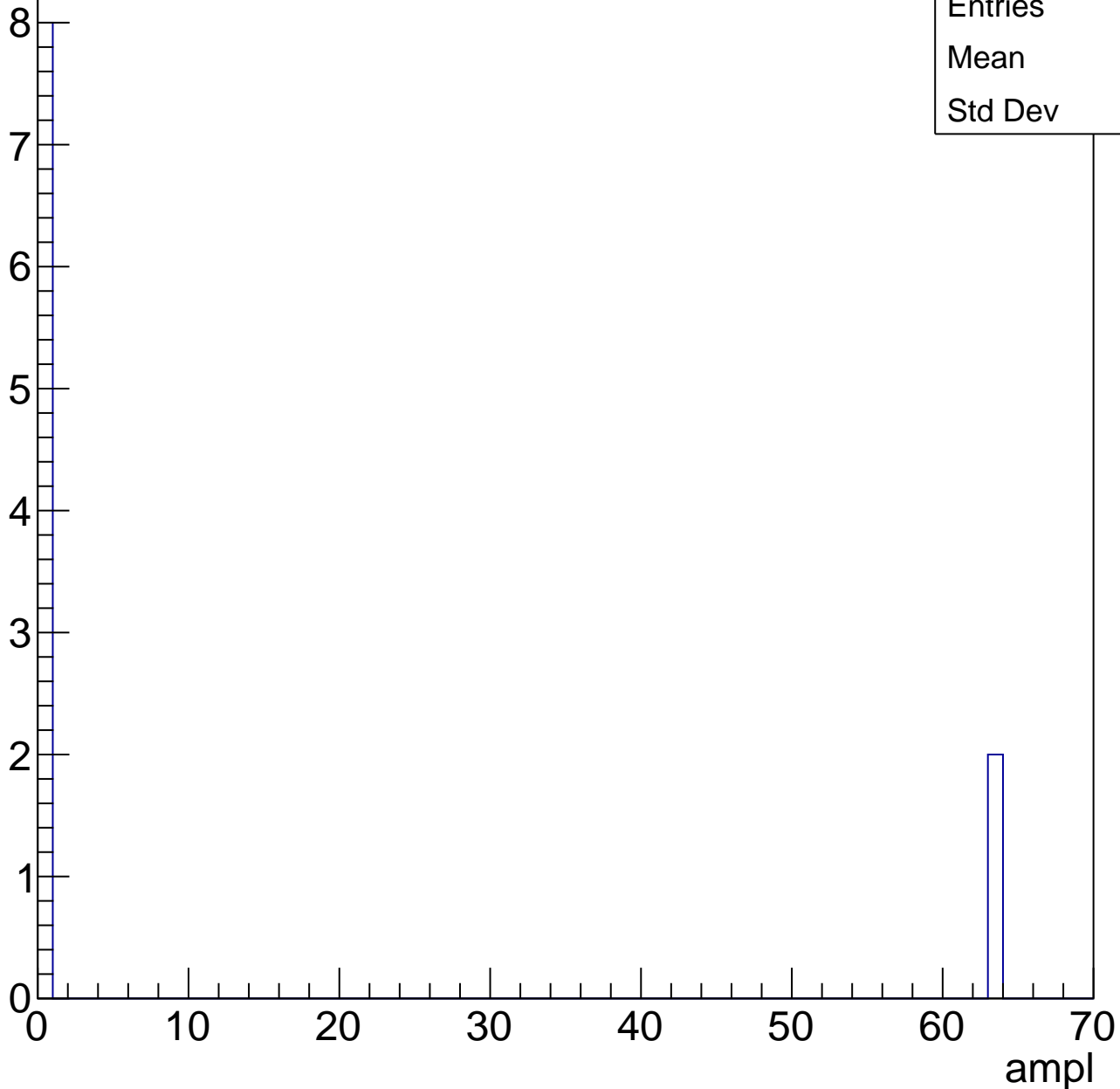


B1L103S, U14-ch68, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	10
Mean	12.6
Std Dev	25.2

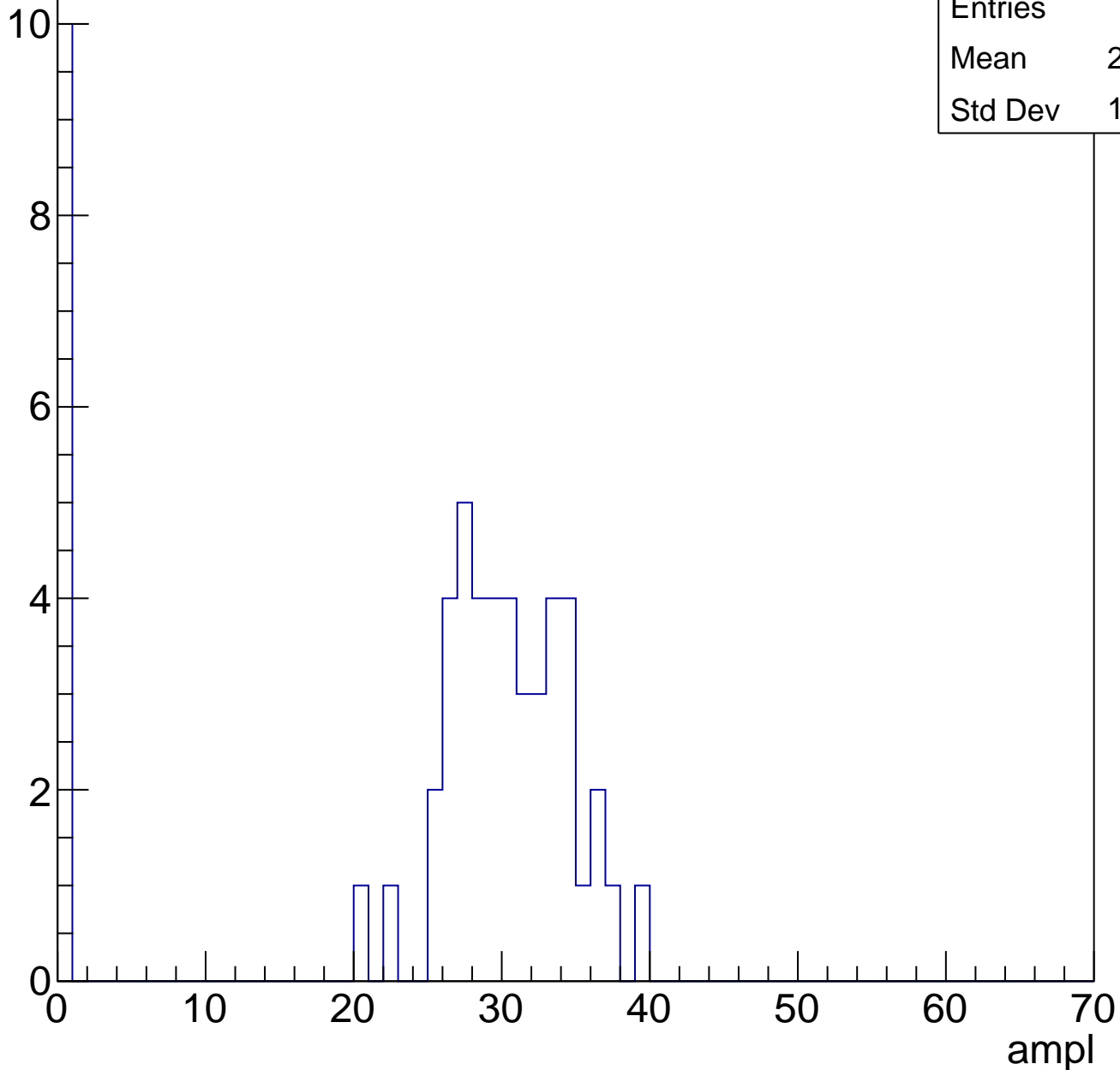


B1L103S, U14-ch69, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	54
Mean	24.43
Std Dev	12.18

Entry

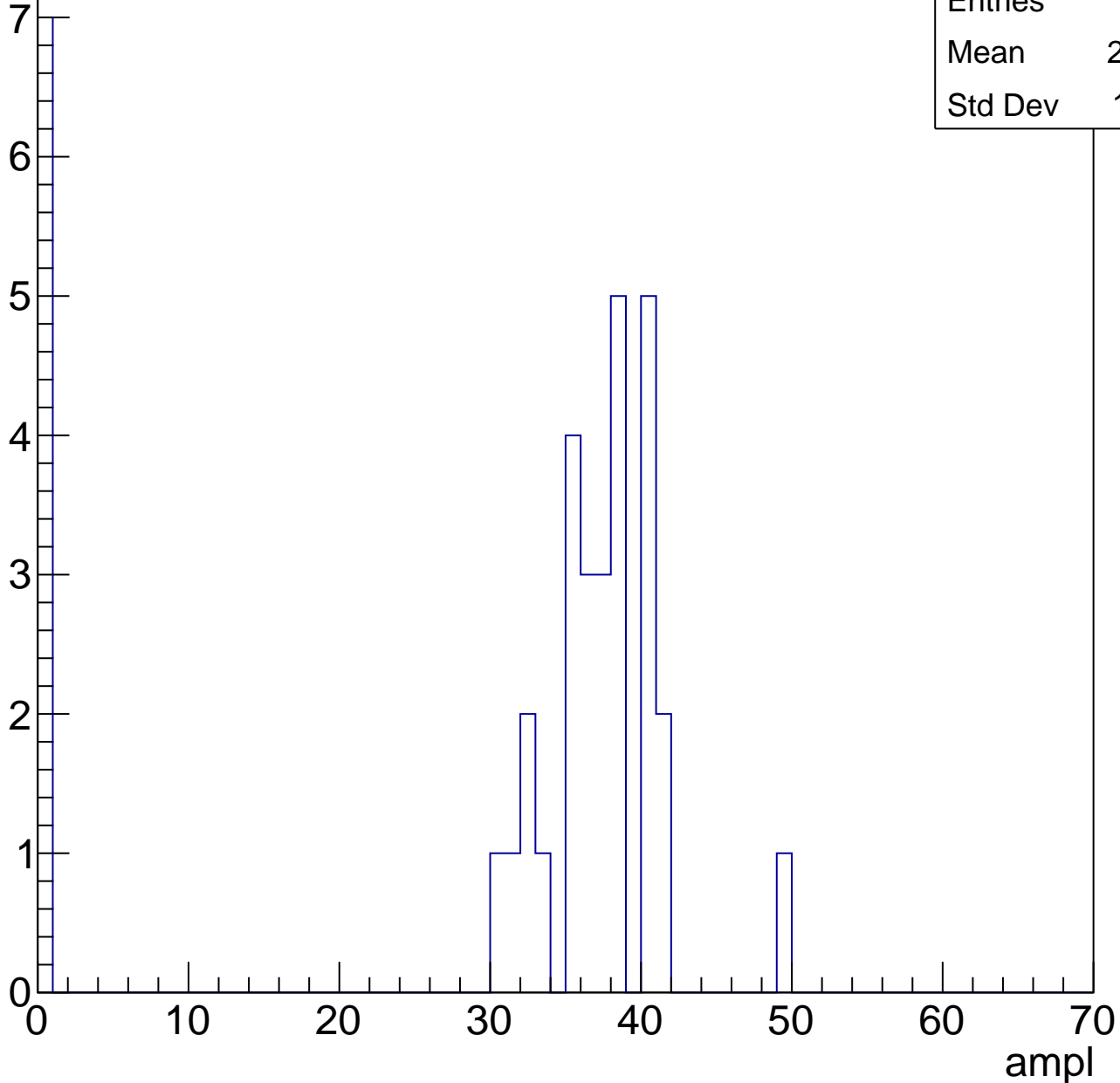


B1L103S, U14-ch69, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	35
Mean	29.66
Std Dev	15.21

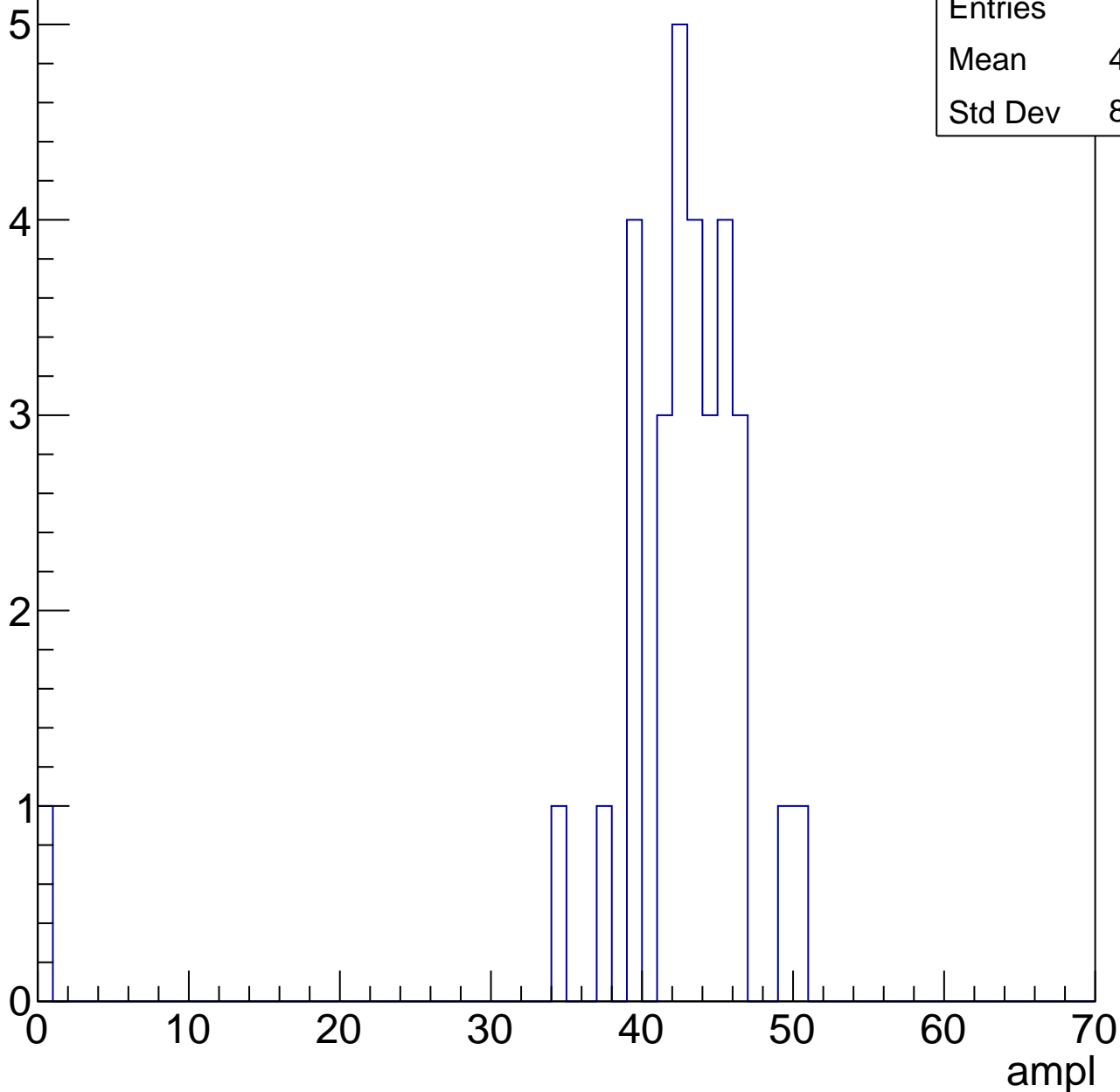


B1L103S, U14-ch69, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	31
Mean	41.32
Std Dev	8.212

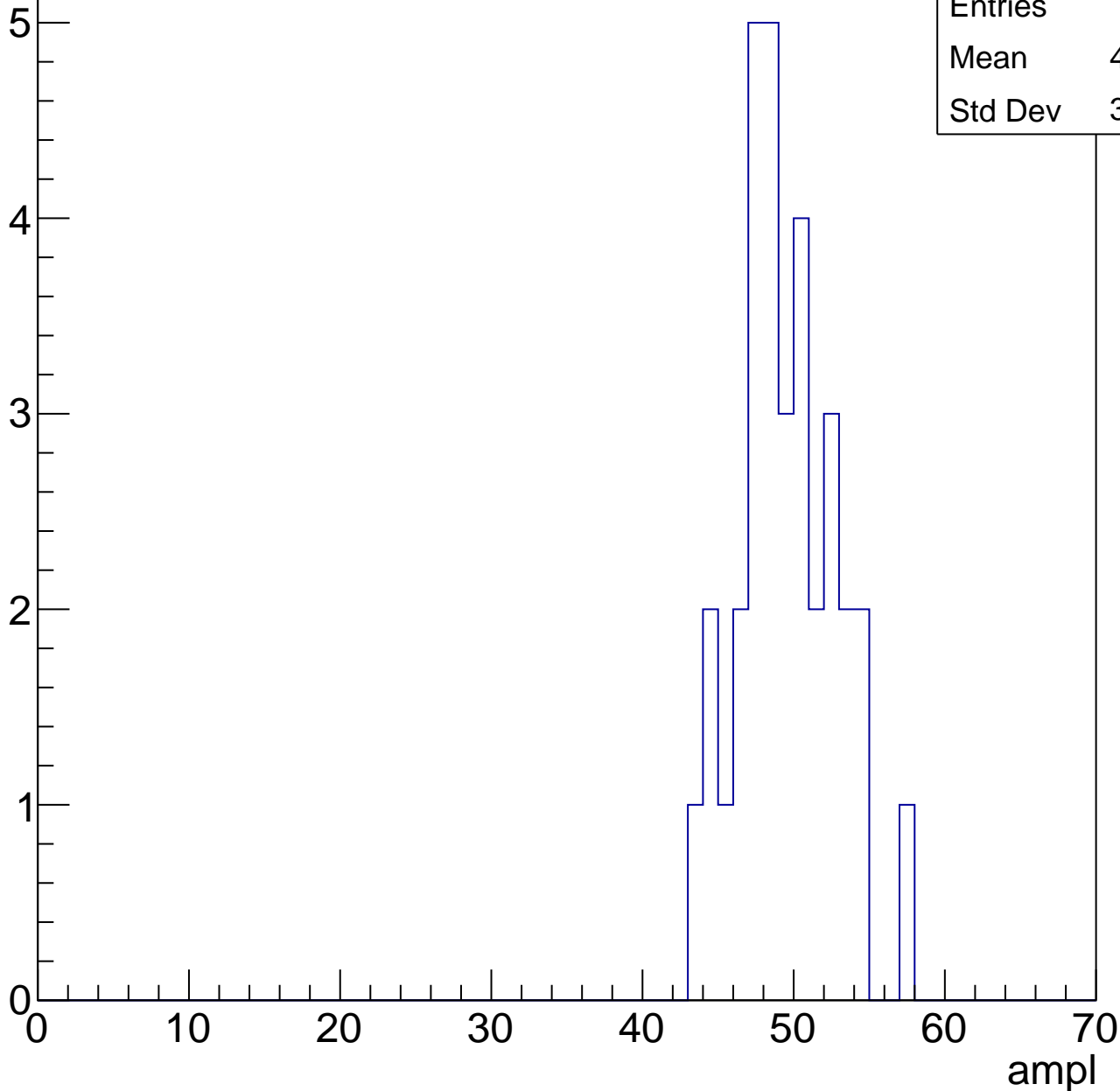


B1L103S, U14-ch69, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	33
Mean	49.06
Std Dev	3.162

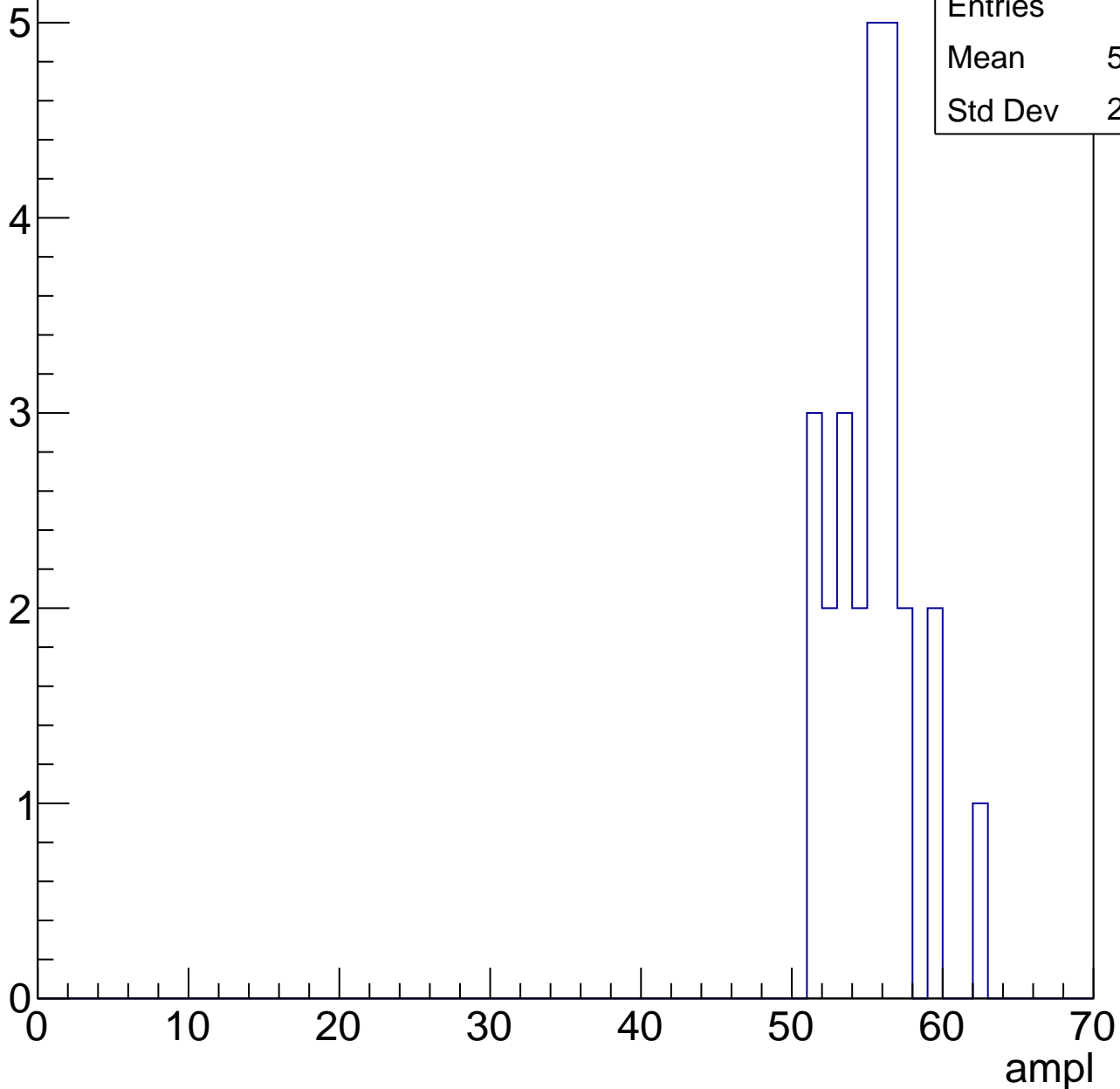


B1L103S, U14-ch69, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	25
Mean	54.92
Std Dev	2.637

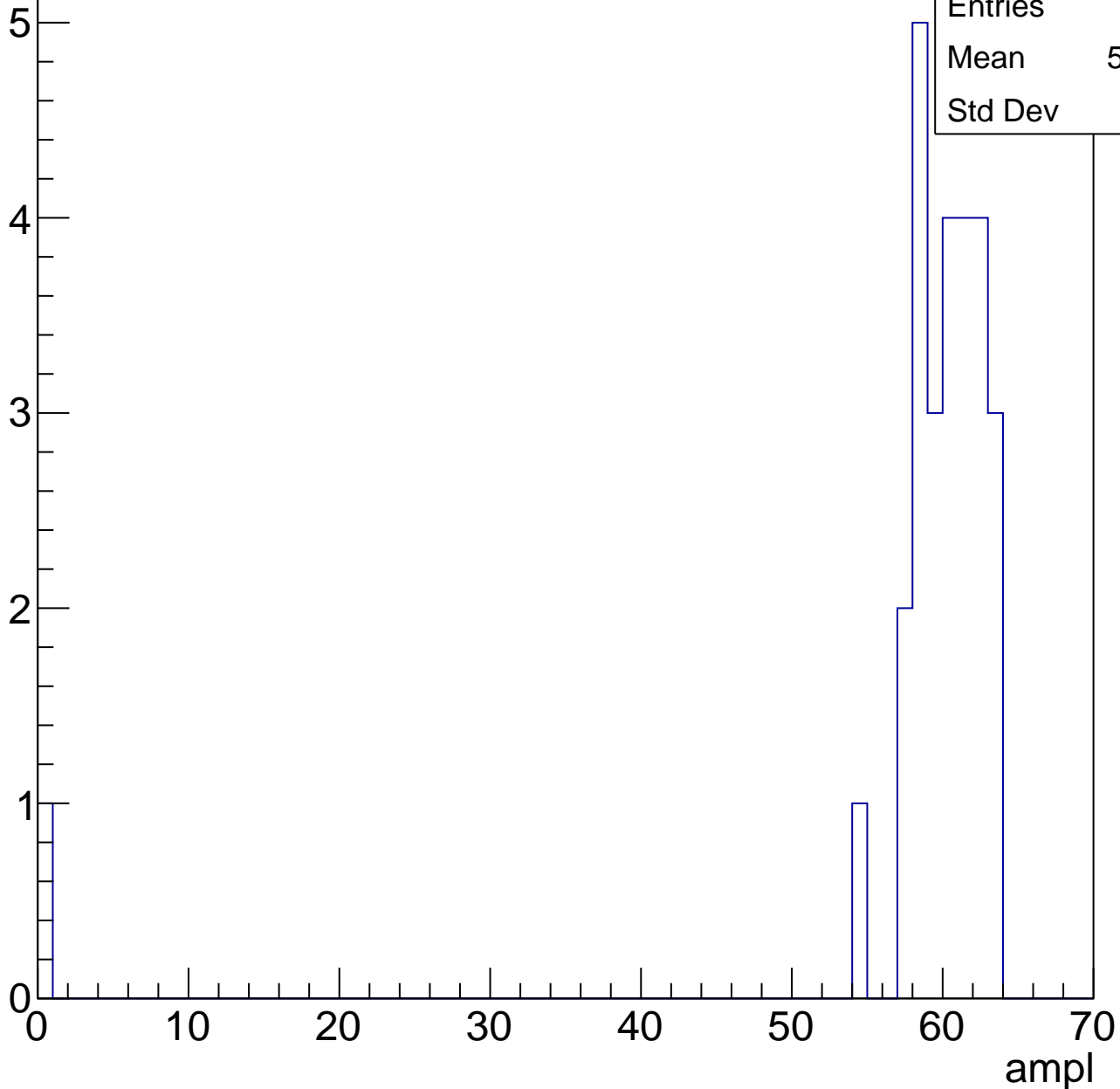


B1L103S, U14-ch69, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	27
Mean	57.63
Std Dev	11.5



B1L103S, U14-ch69, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

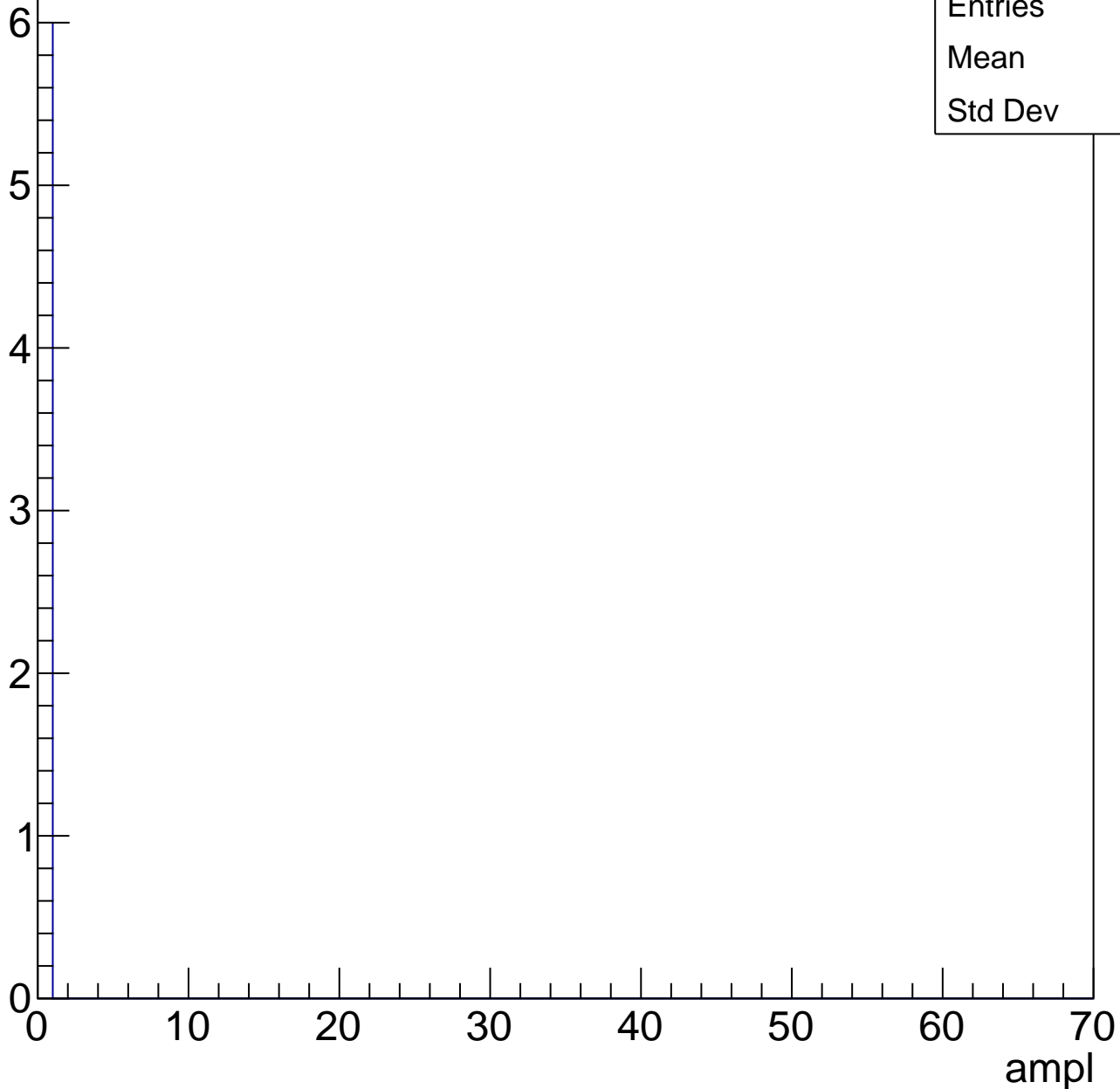


B1L103S, U14-ch69, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	6
Mean	0
Std Dev	0



B1L103S, U14-ch70, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	44
Mean	20.14
Std Dev	12.04

Entry

10

8

6

4

2

0

0

10

20

30

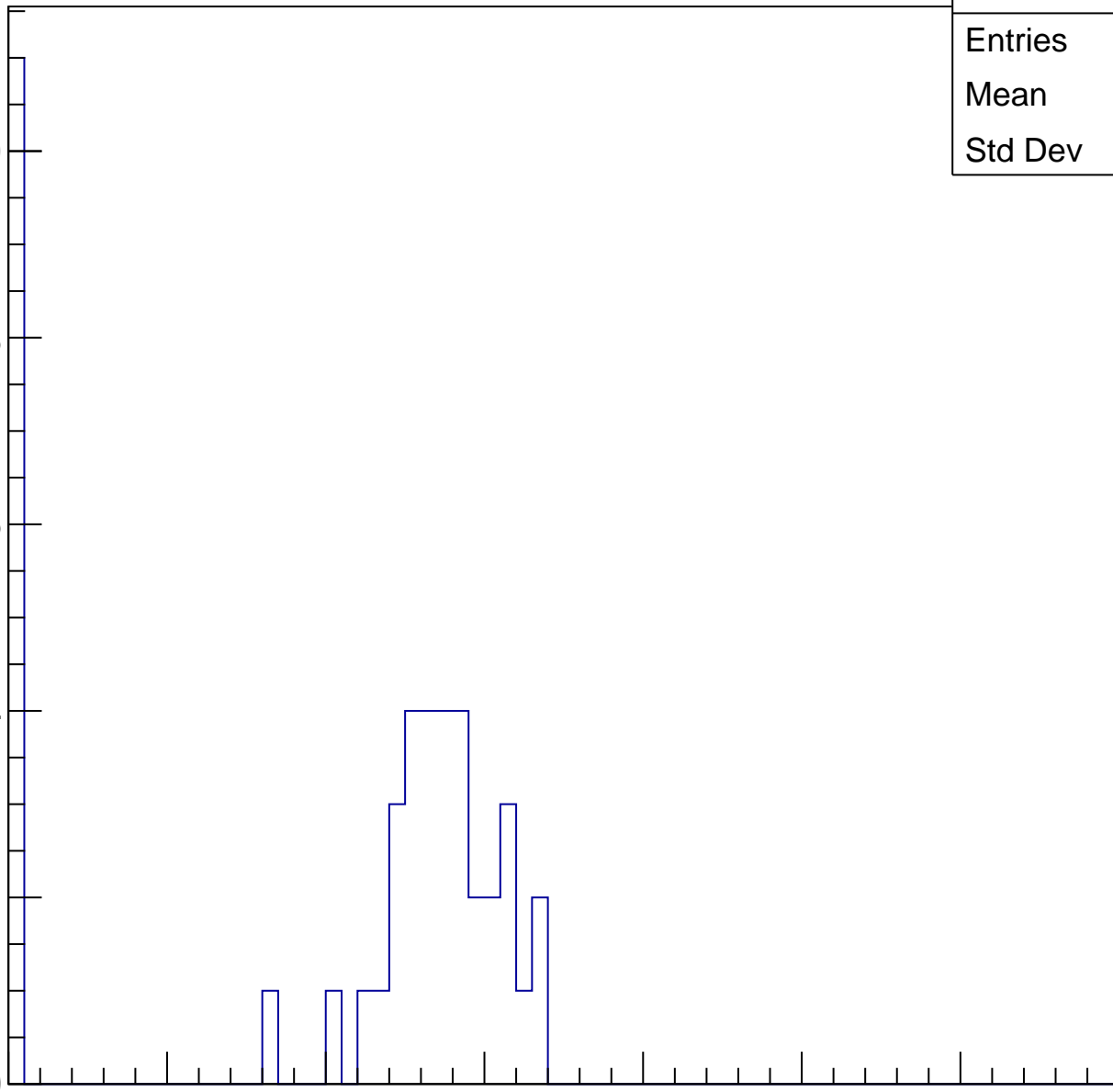
40

50

60

70

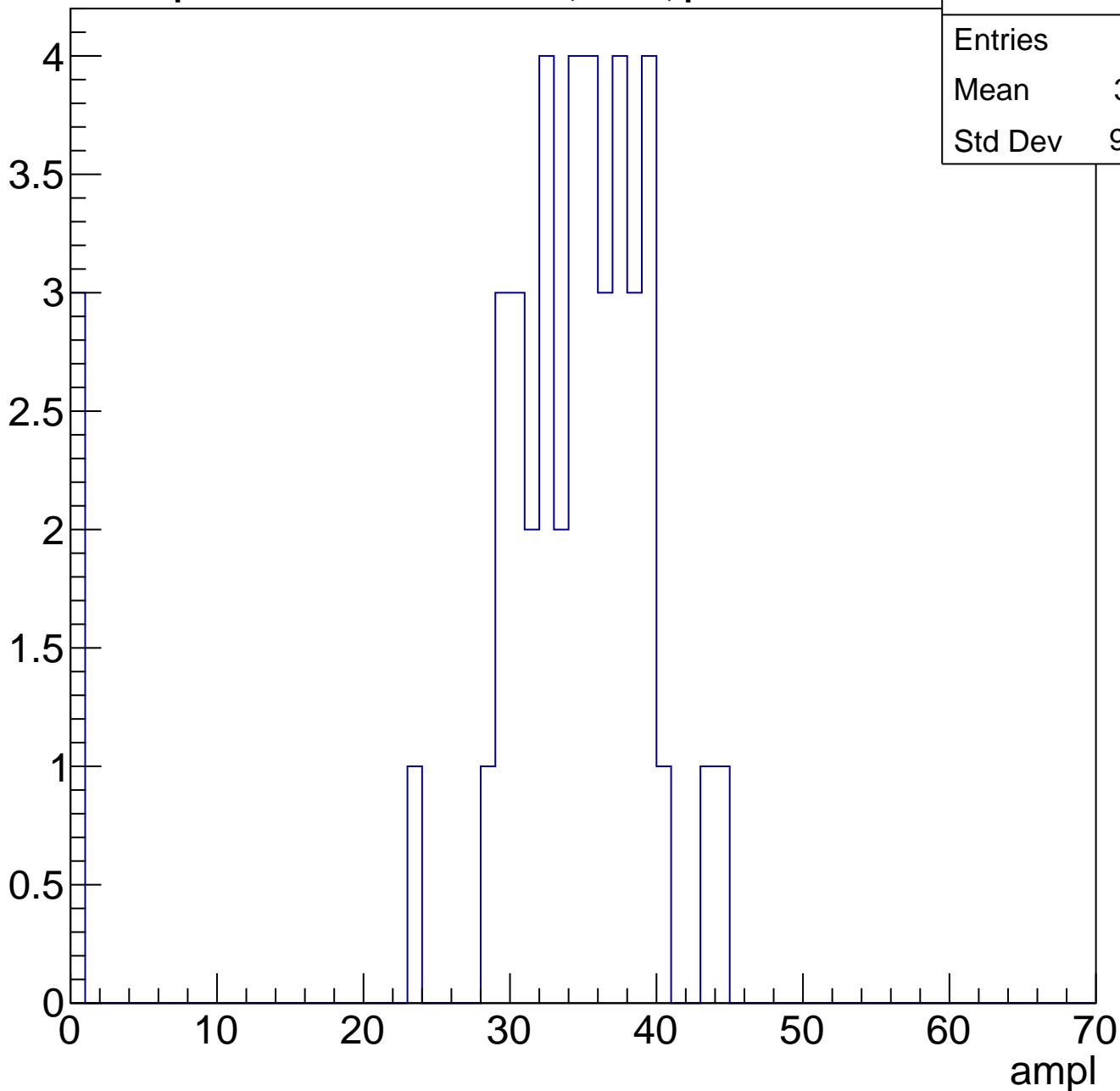
ampl



B1L103S, U14-ch70, adc1

calib_packv5_041523_1651.root, FC#0, port C2

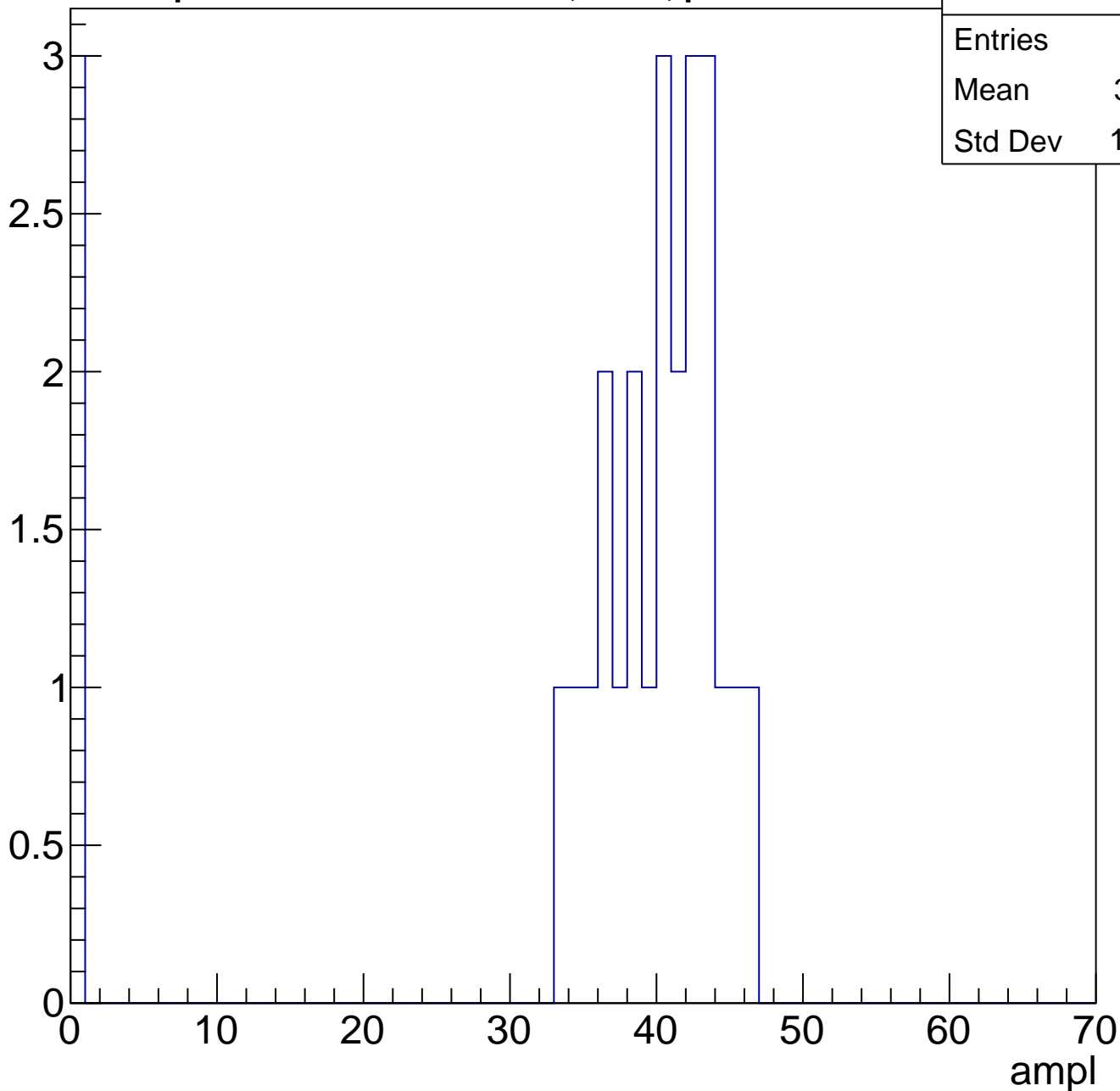
Entry



B1L103S, U14-ch70, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

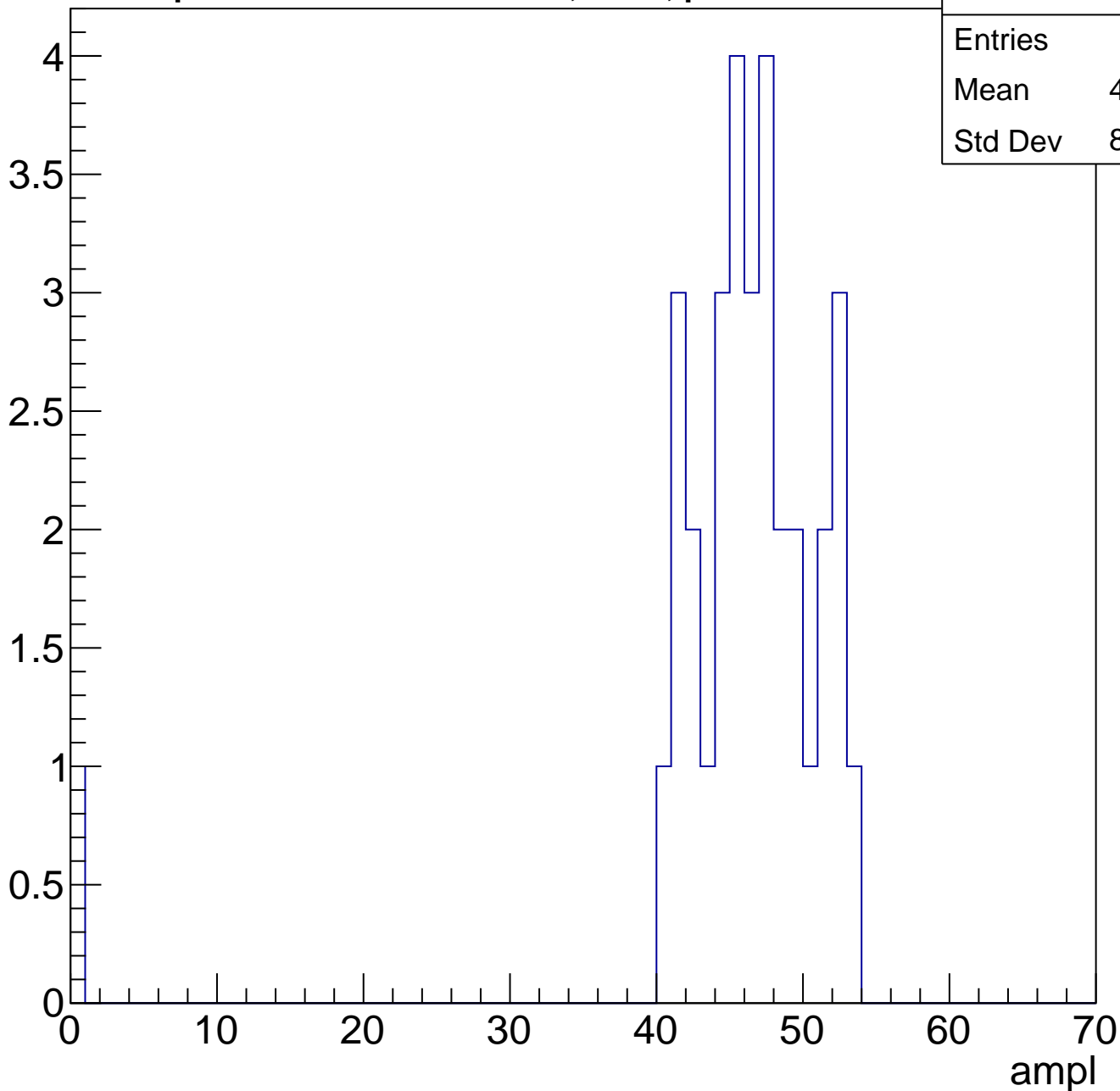


Entries	26
Mean	35.31
Std Dev	13.16

B1L103S, U14-ch70, adc3

calib_packv5_041523_1651.root, FC#0, port C2

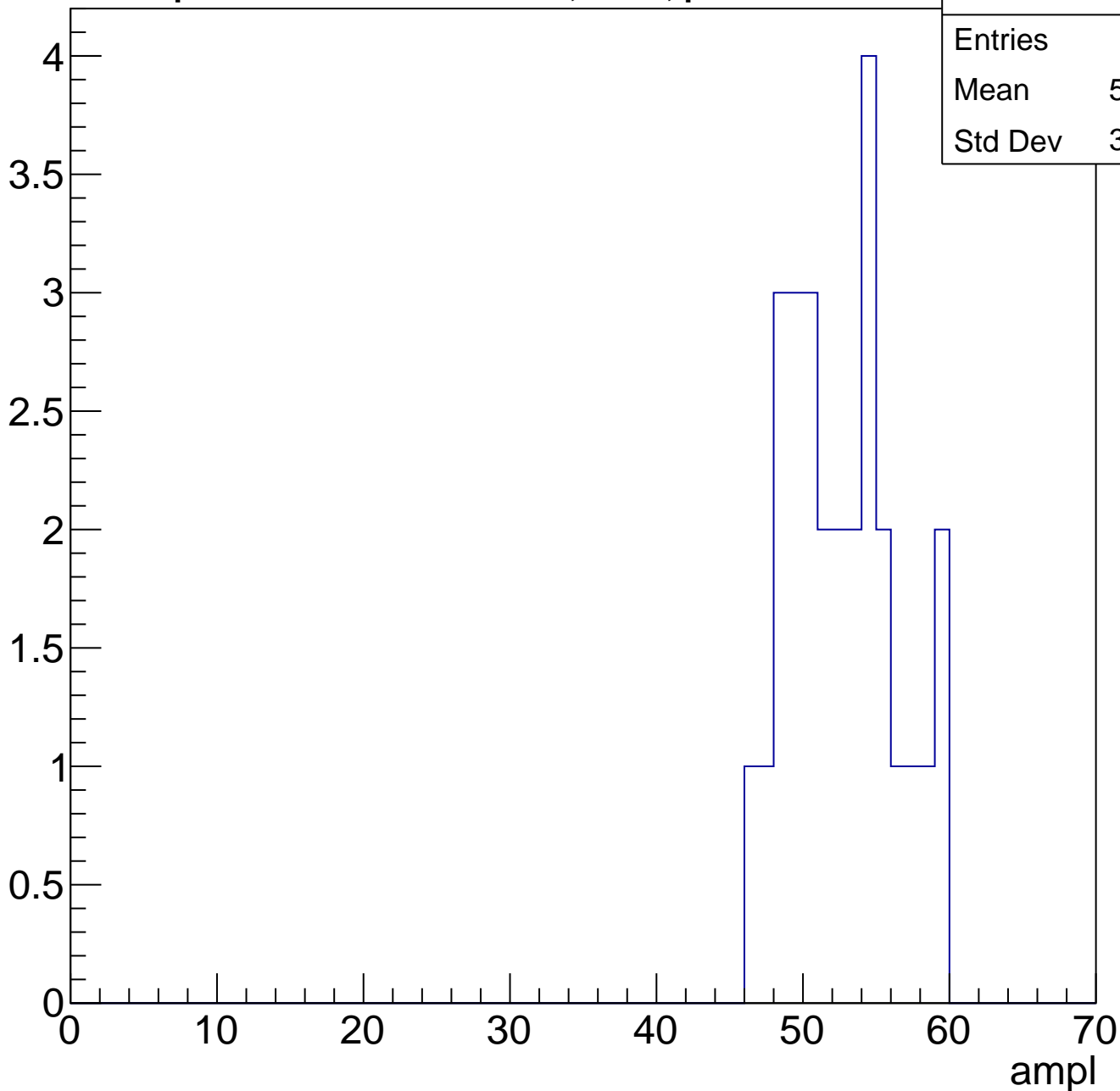
Entry



B1L103S, U14-ch70, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch70, adc5

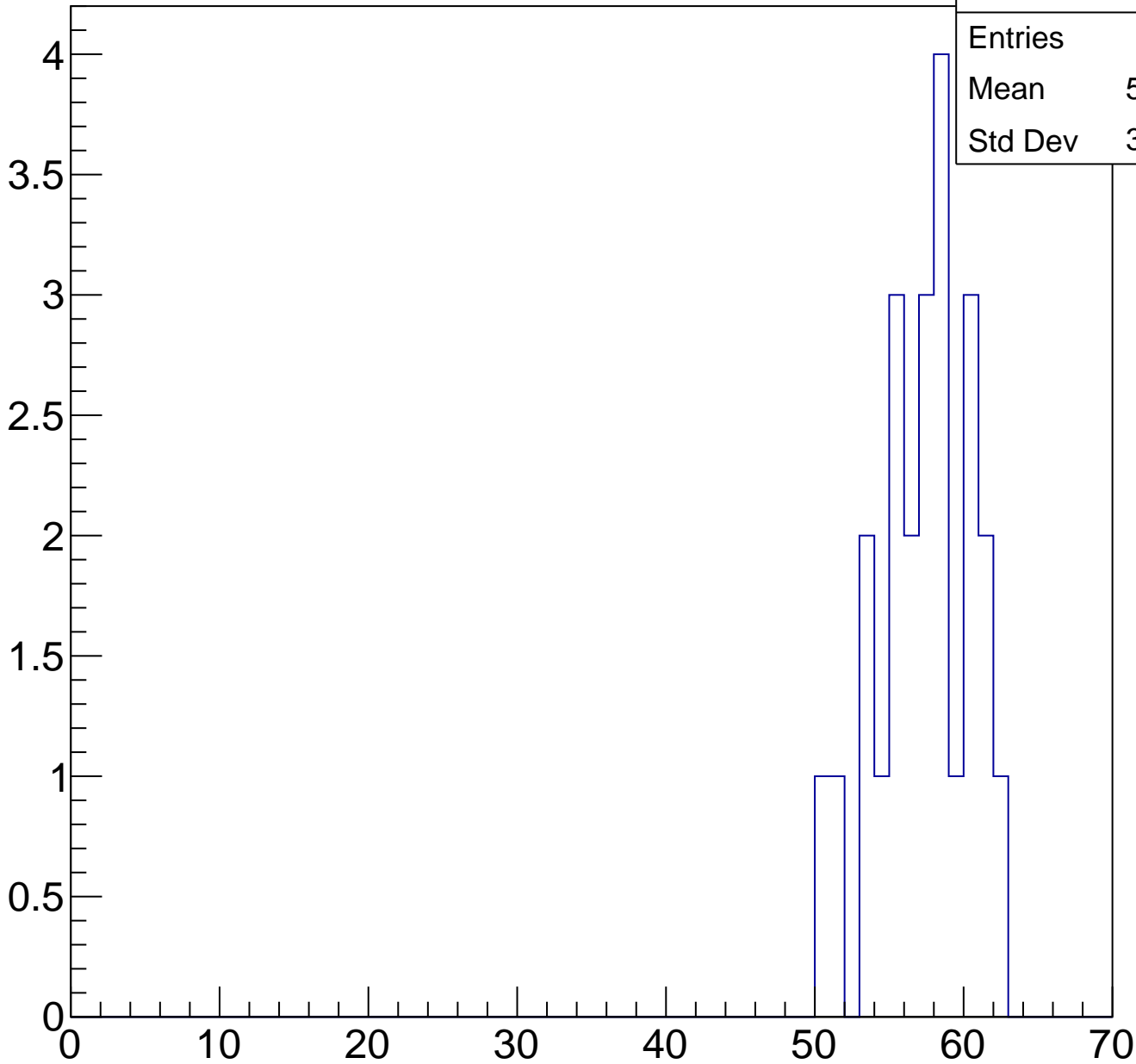
calib_packv5_041523_1651.root, FC#0, port C2

Entry

4
3.5
3
2.5
2
1.5
1
0.5
0

Entries	24
Mean	56.83
Std Dev	3.105

ampl

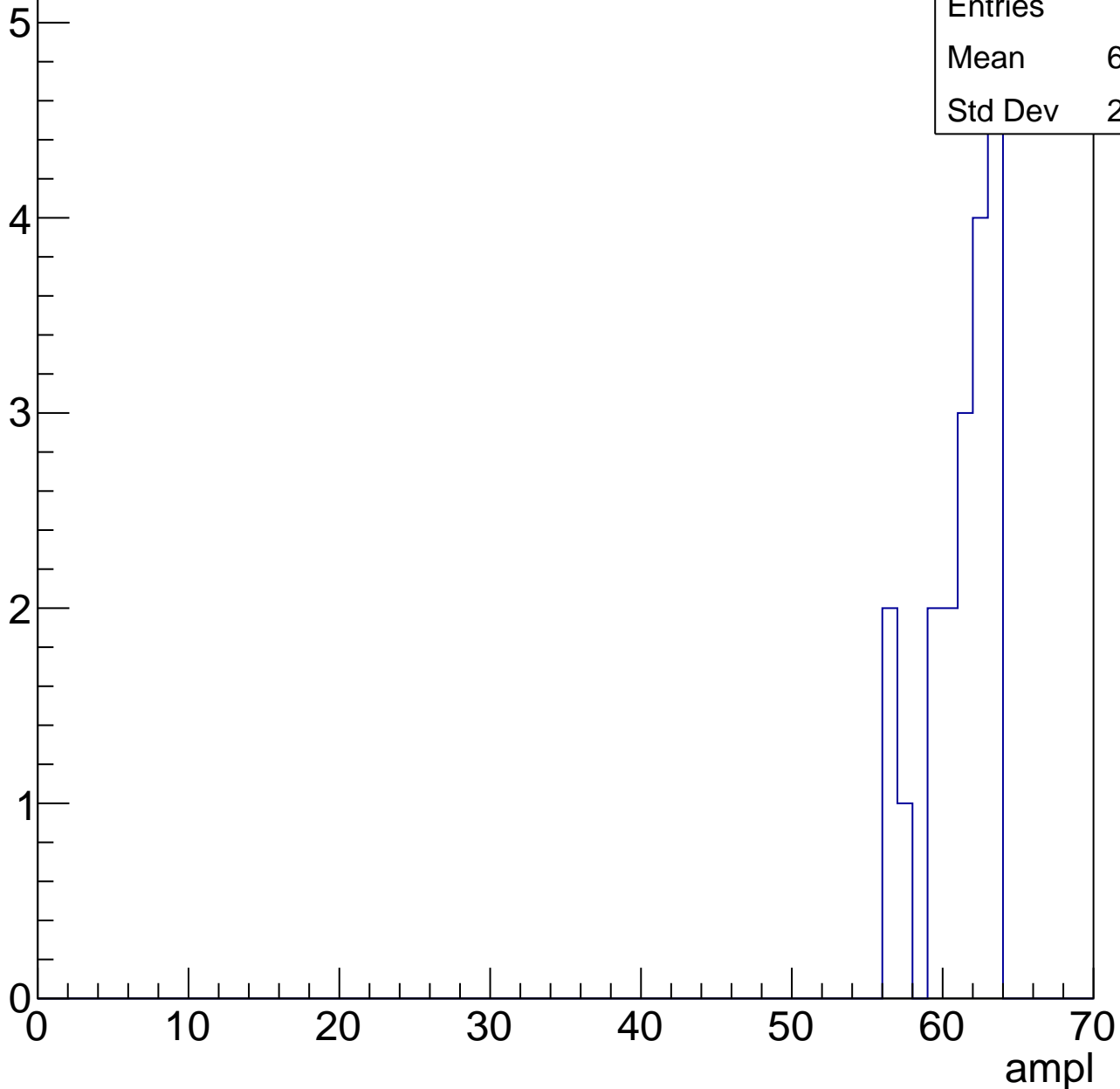


B1L103S, U14-ch70, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	19
Mean	60.68
Std Dev	2.272

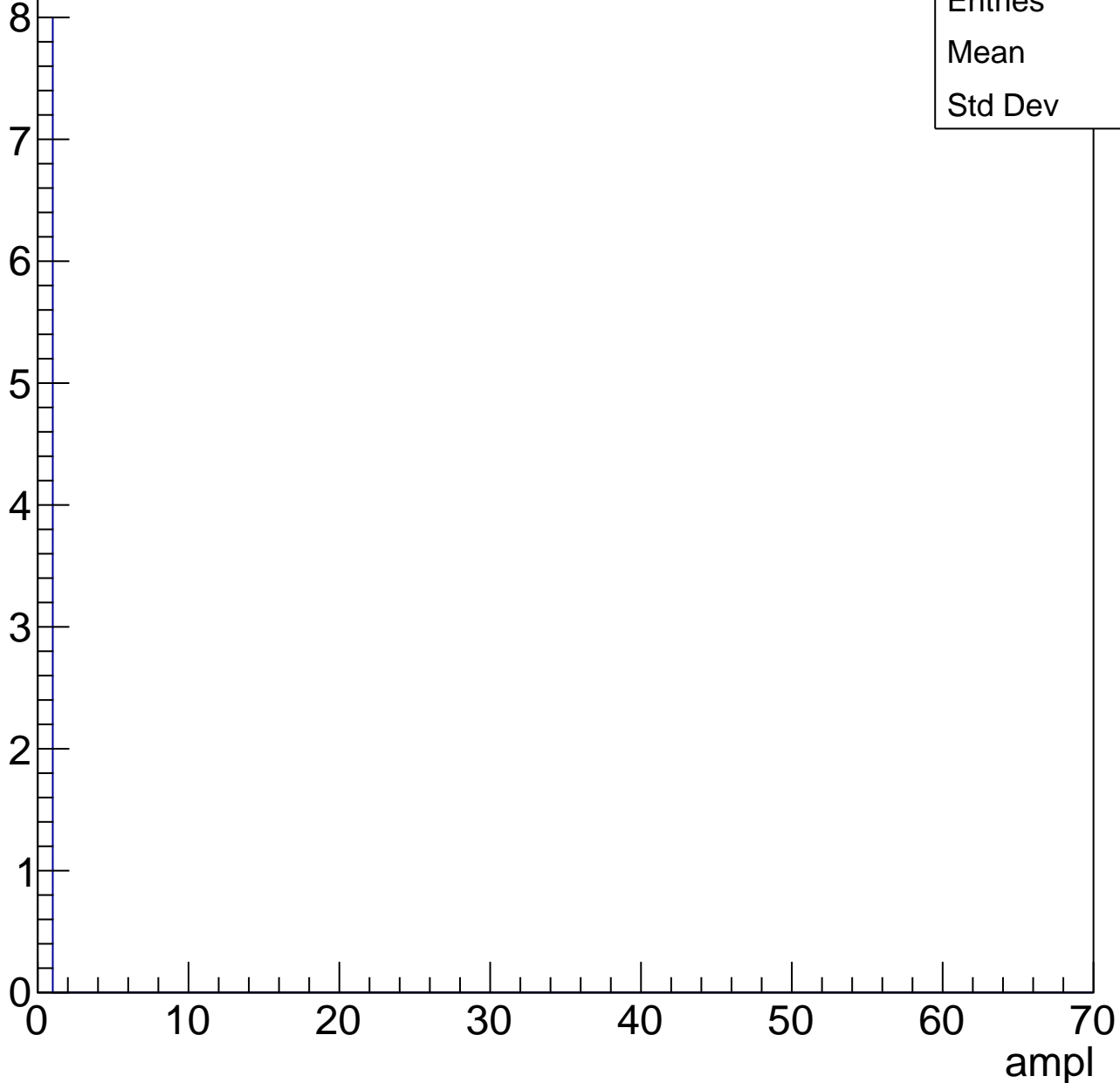


B1L103S, U14-ch70, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	8
Mean	0
Std Dev	0

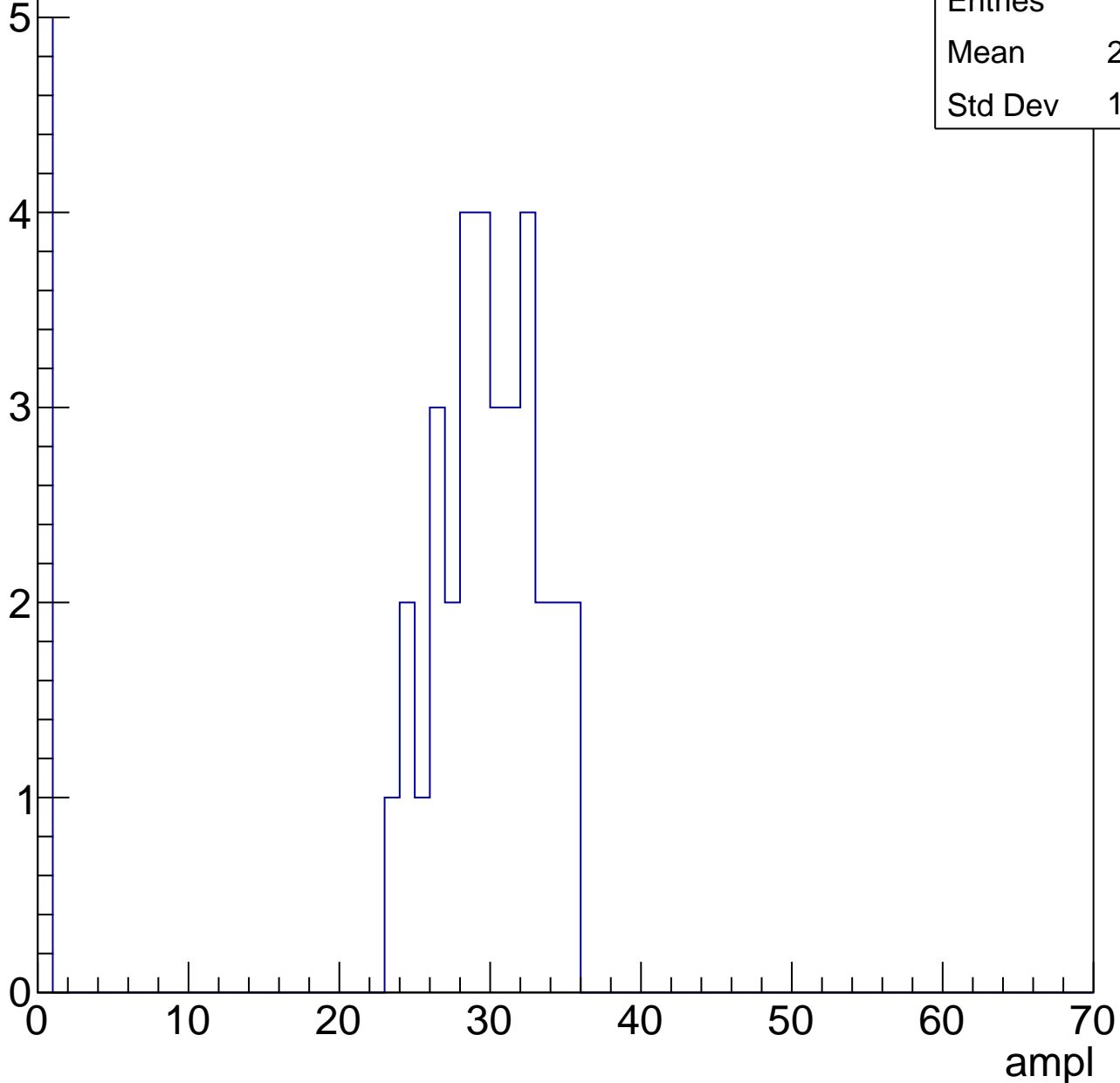


B1L103S, U14-ch71, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	38
Mean	25.55
Std Dev	10.39

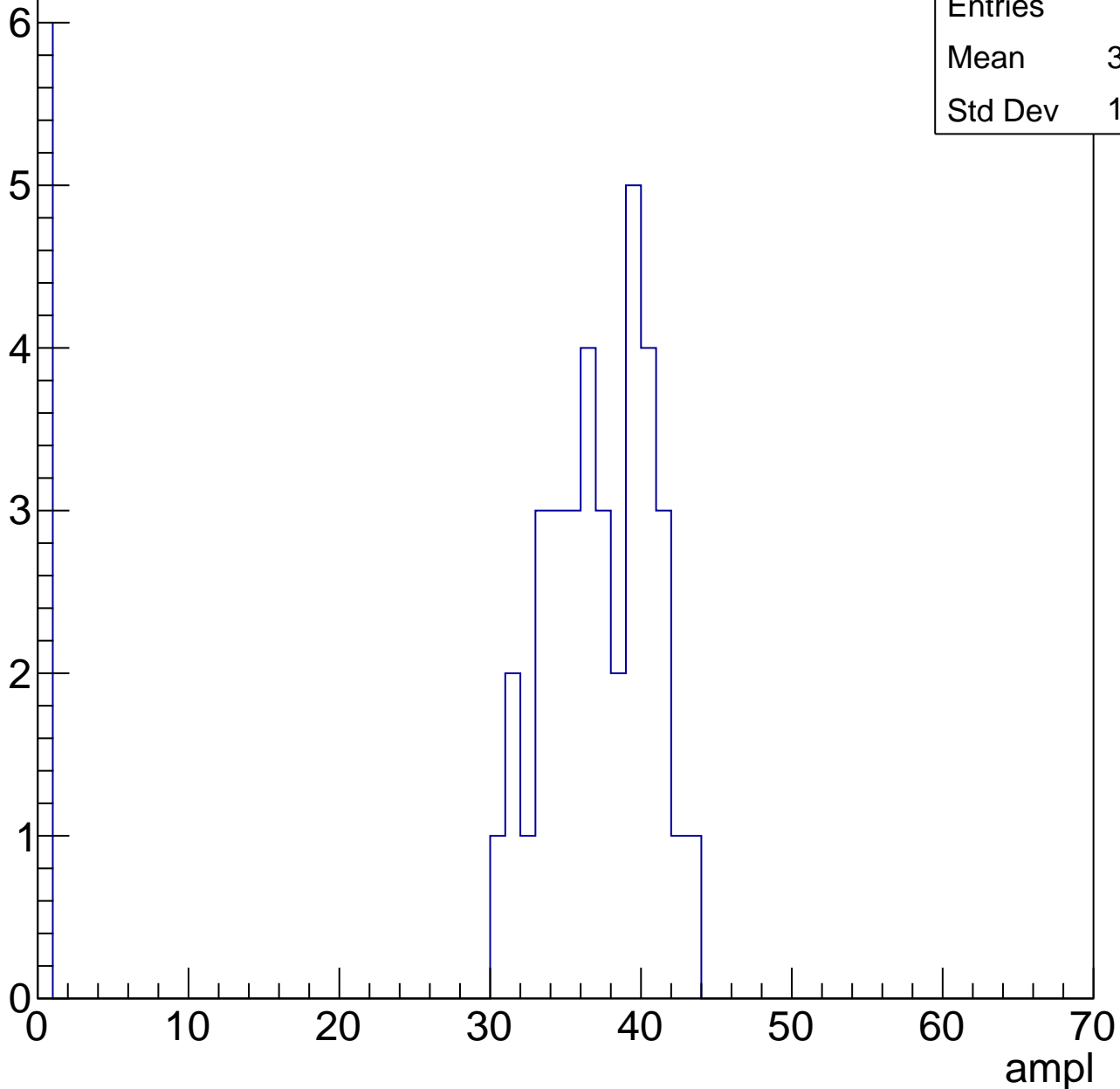


B1L103S, U14-ch71, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	42
Mean	31.52
Std Dev	13.24

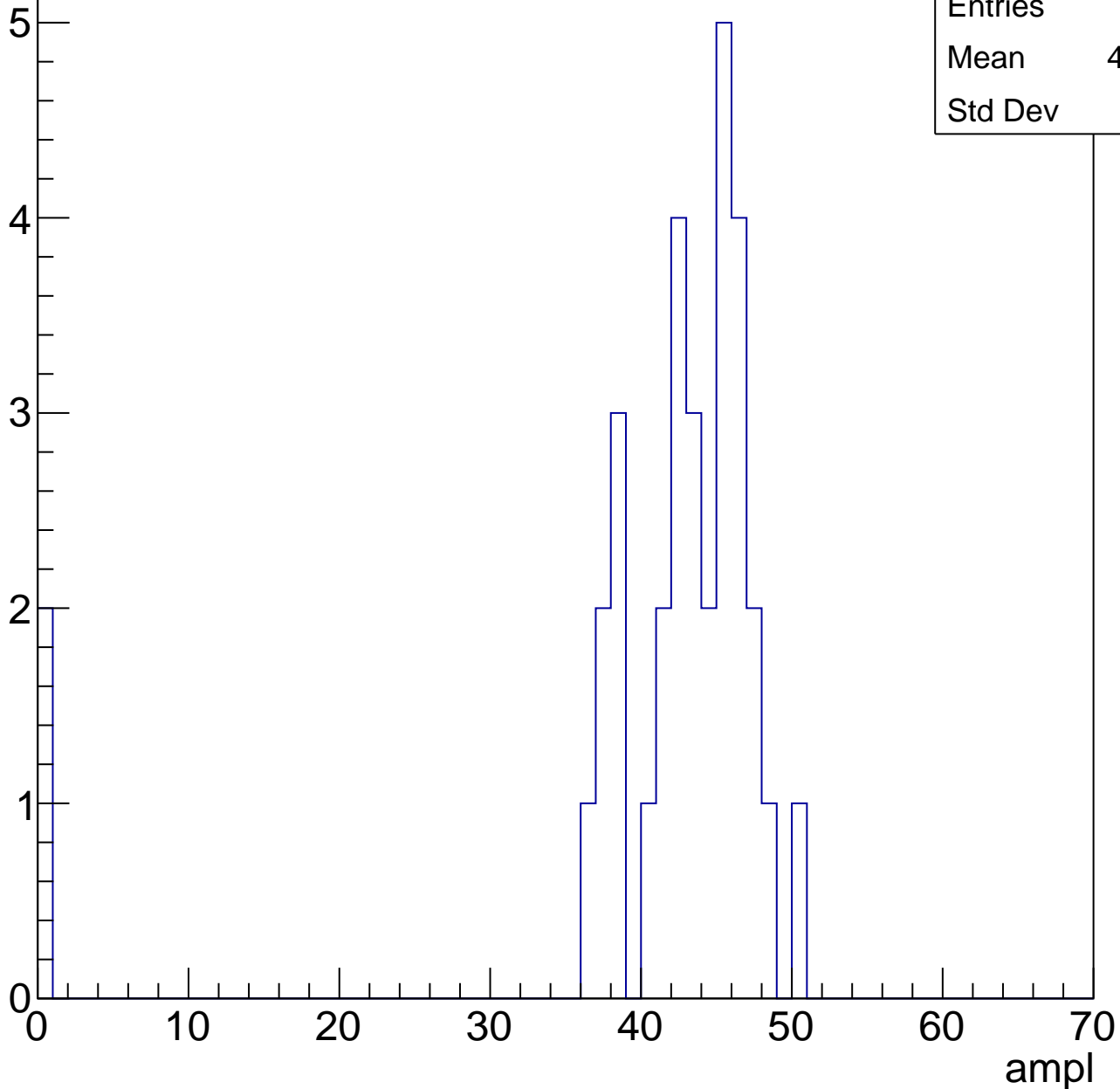


B1L103S, U14-ch71, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	33
Mean	40.36
Std Dev	10.8

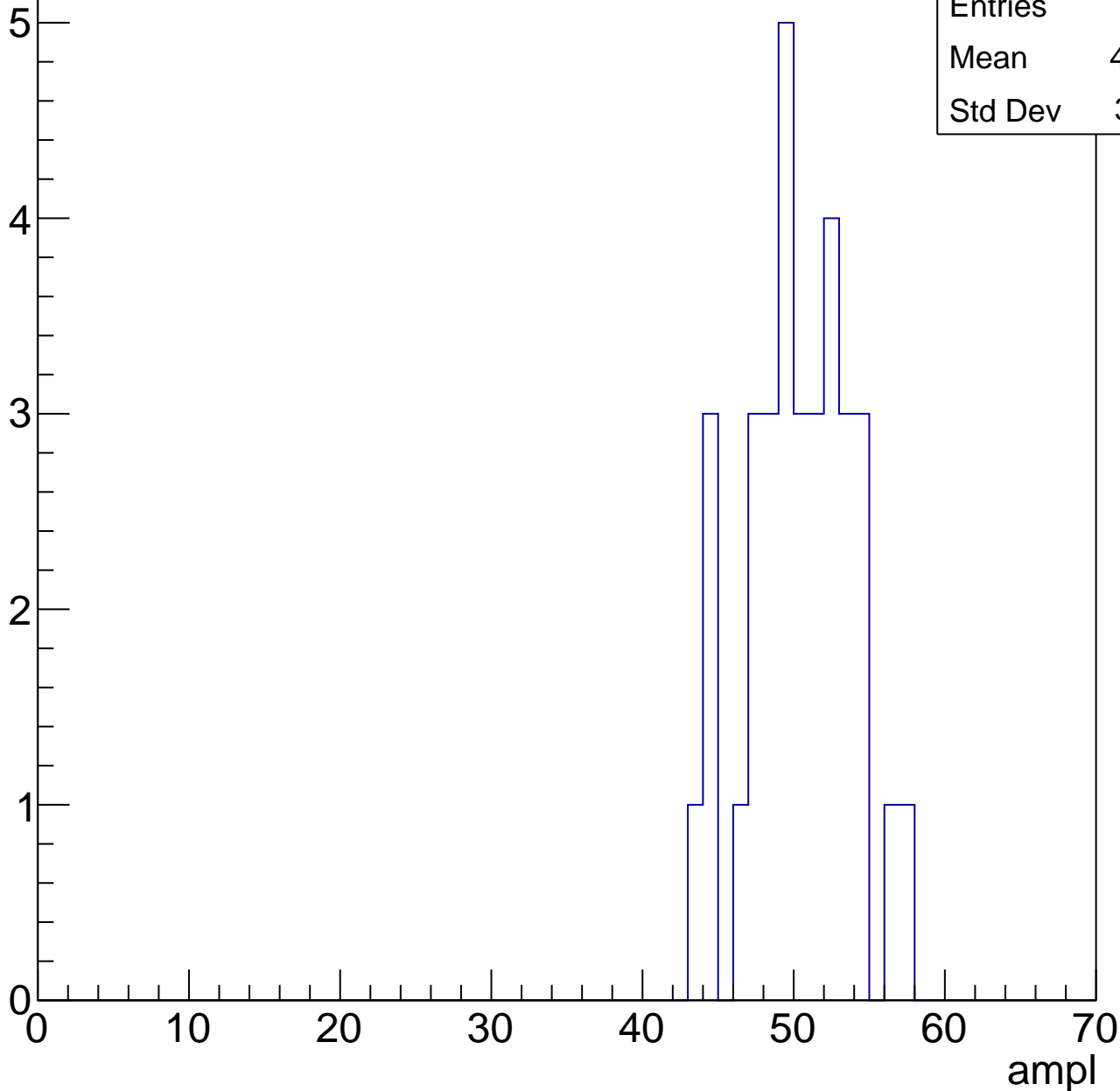


B1L103S, U14-ch71, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	34
Mean	49.88
Std Dev	3.411

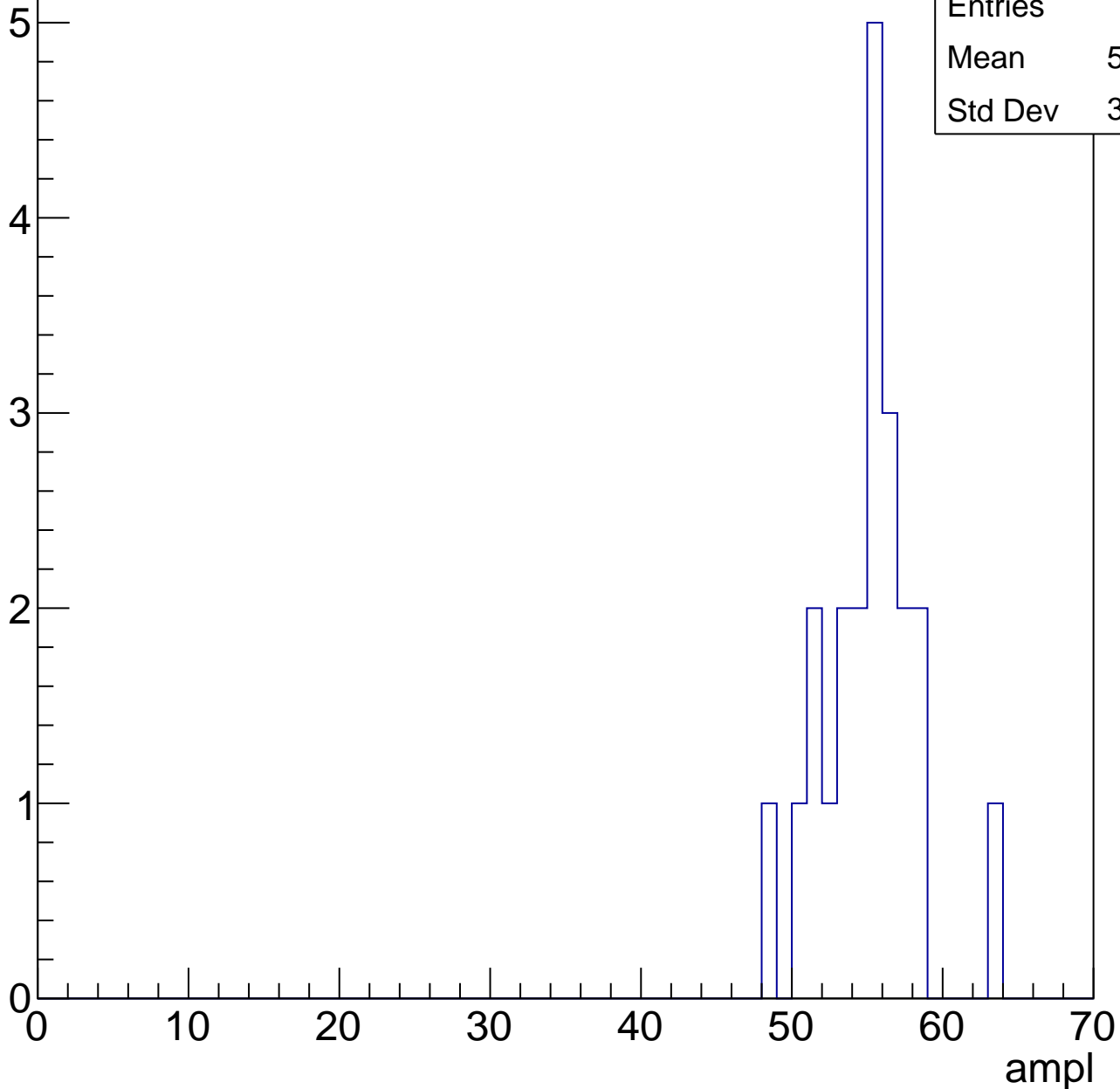


B1L103S, U14-ch71, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

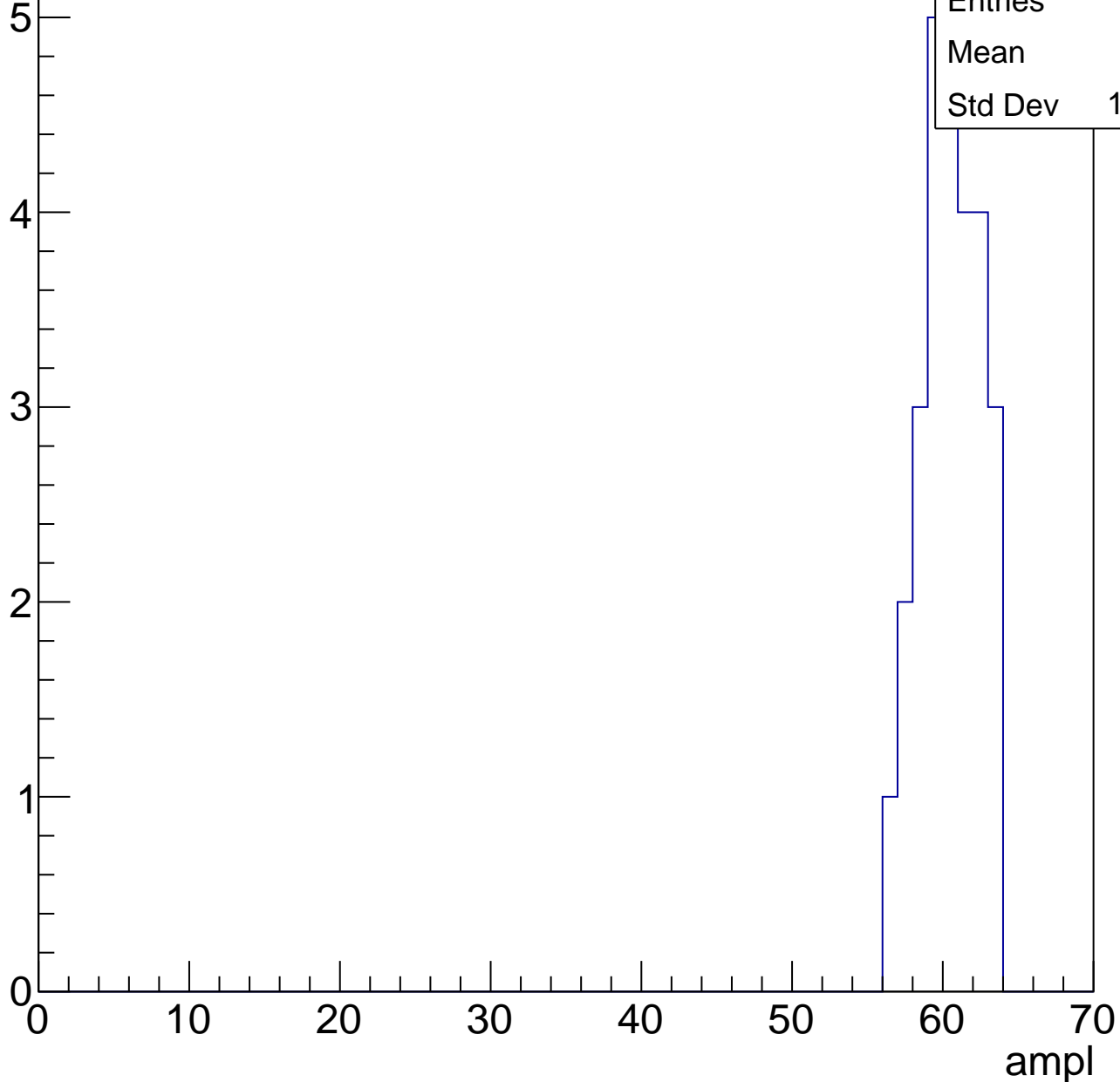
Entries	22
Mean	54.64
Std Dev	3.127



B1L103S, U14-ch71, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	27
Mean	60
Std Dev	1.905

B1L103S, U14-ch71, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch71, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

Entries

11

Mean

0

Std Dev

0

B1L103S, U14-ch72, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	43
Mean	19.77
Std Dev	11.95

Entry

10

8

6

4

2

0

0

10

20

30

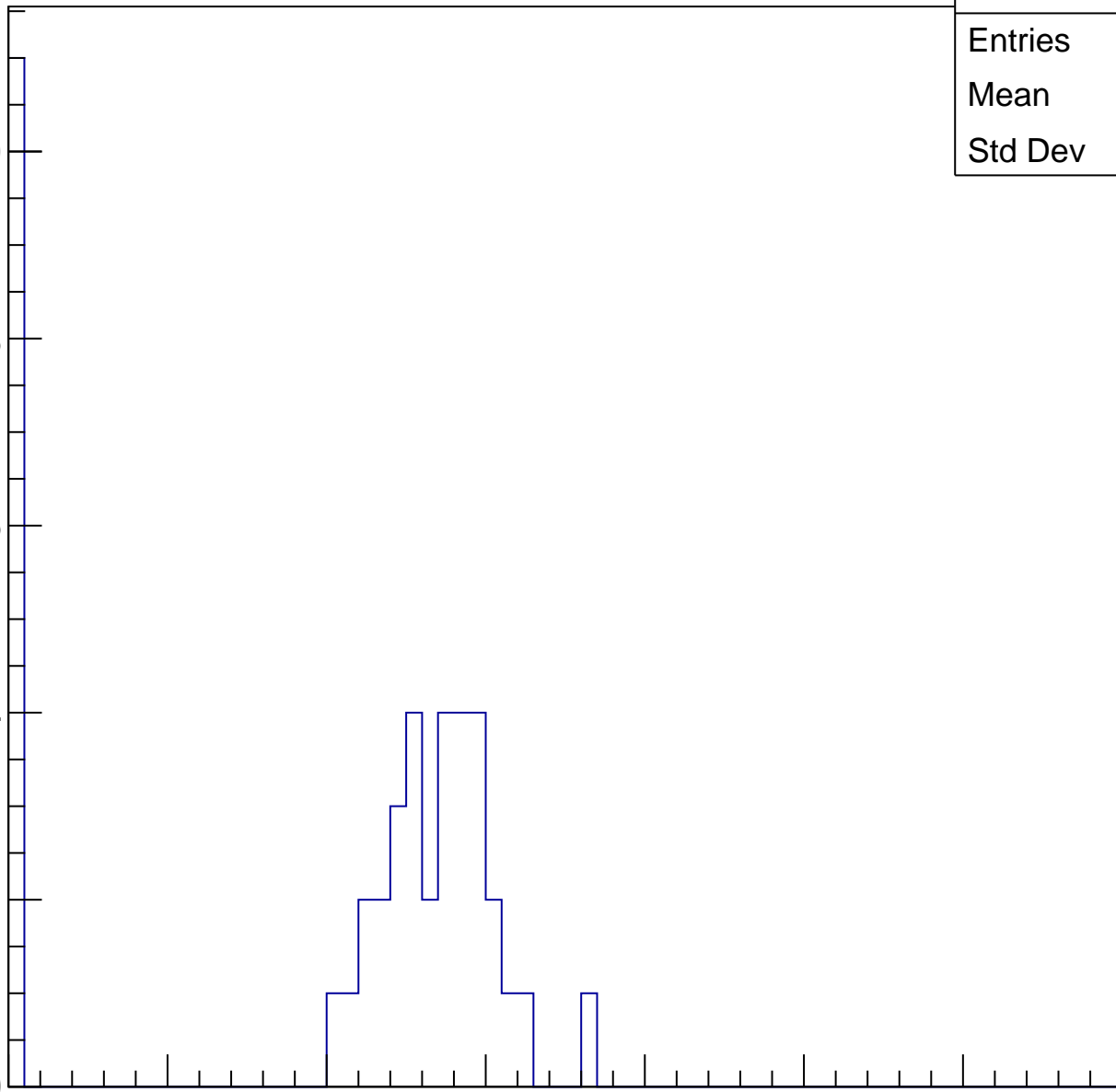
40

50

60

70

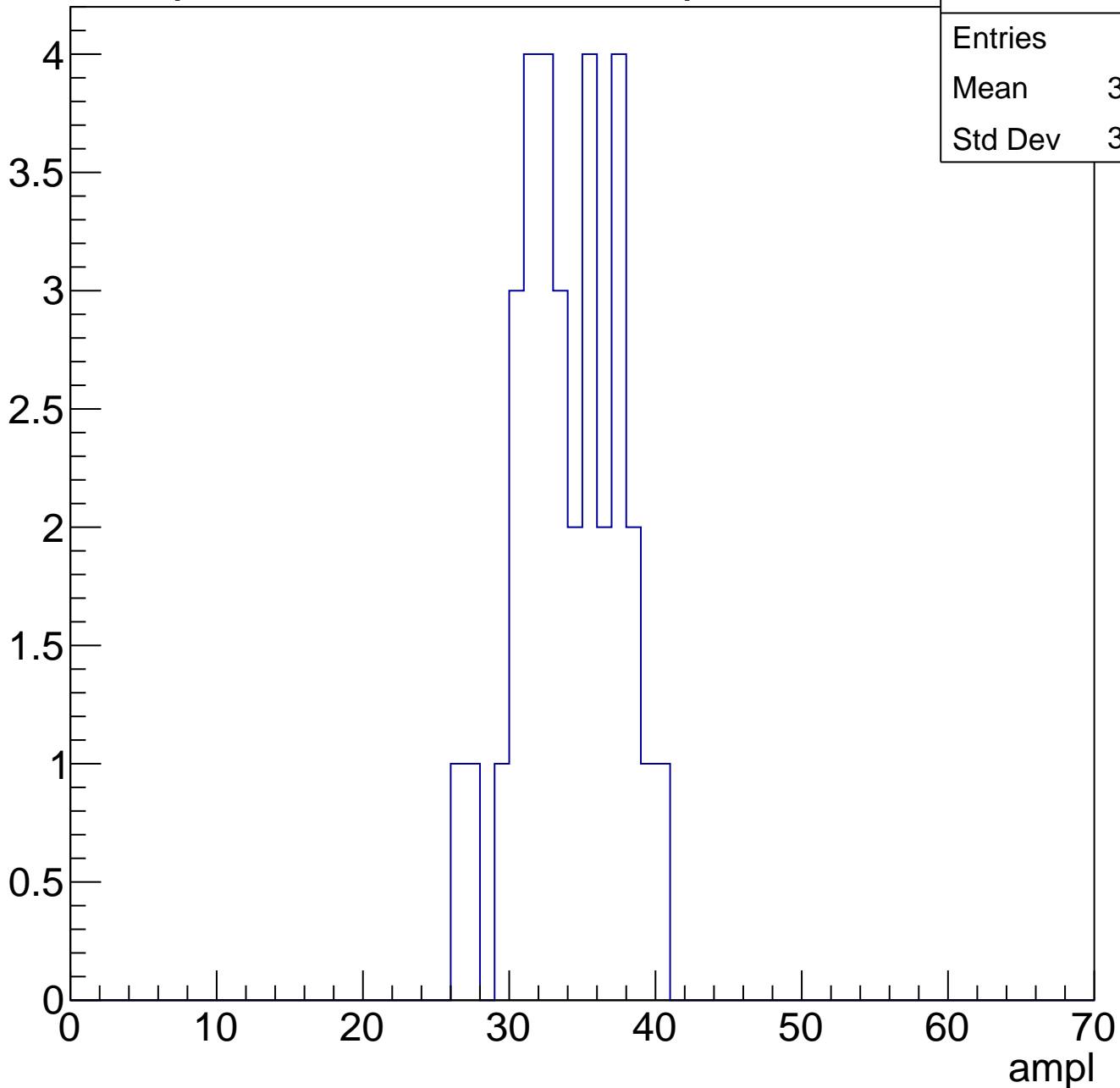
ampl



B1L103S, U14-ch72, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry



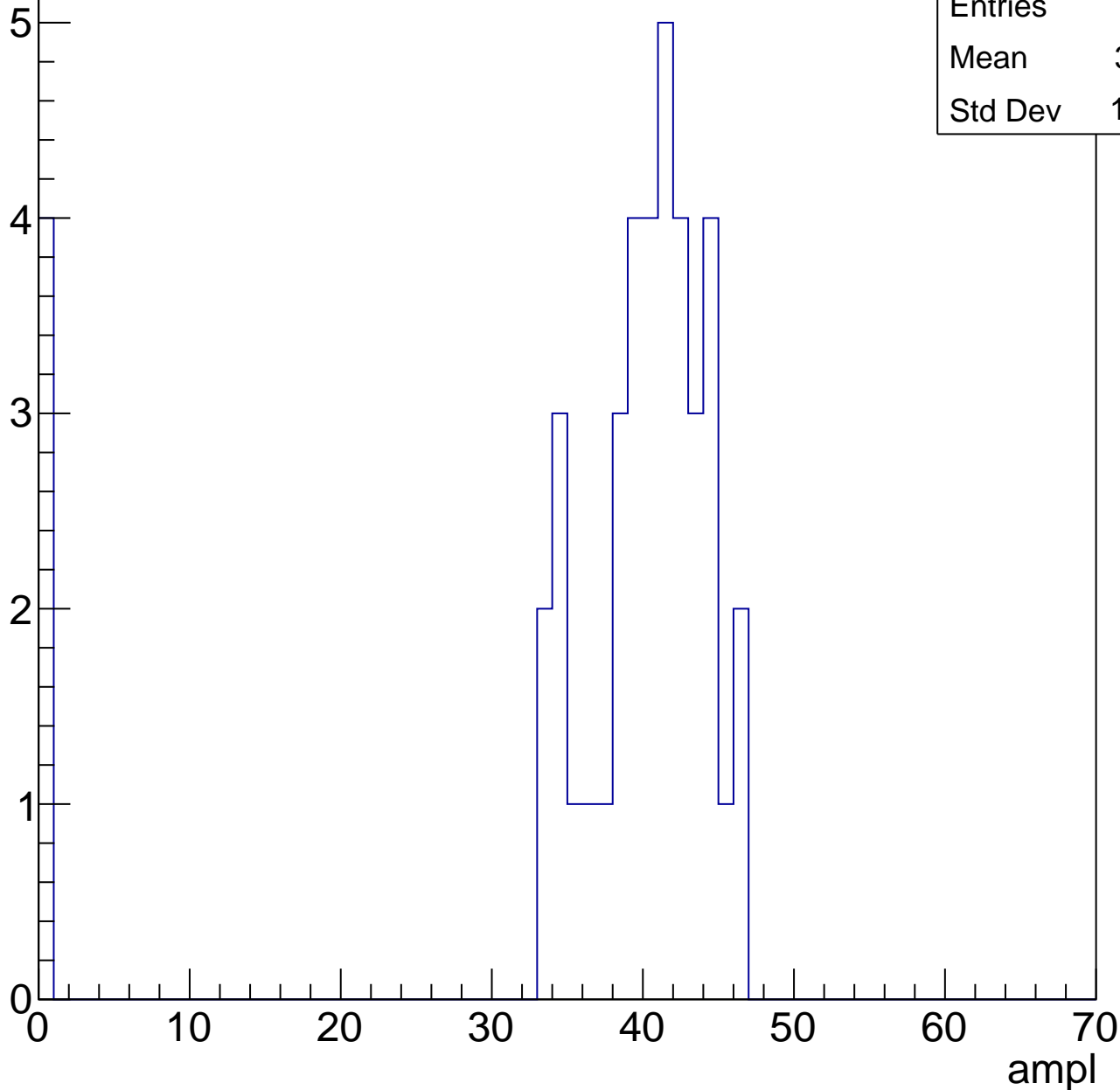
Entries	33
Mean	33.52
Std Dev	3.368

B1L103S, U14-ch72, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	42
Mean	36.21
Std Dev	12.23

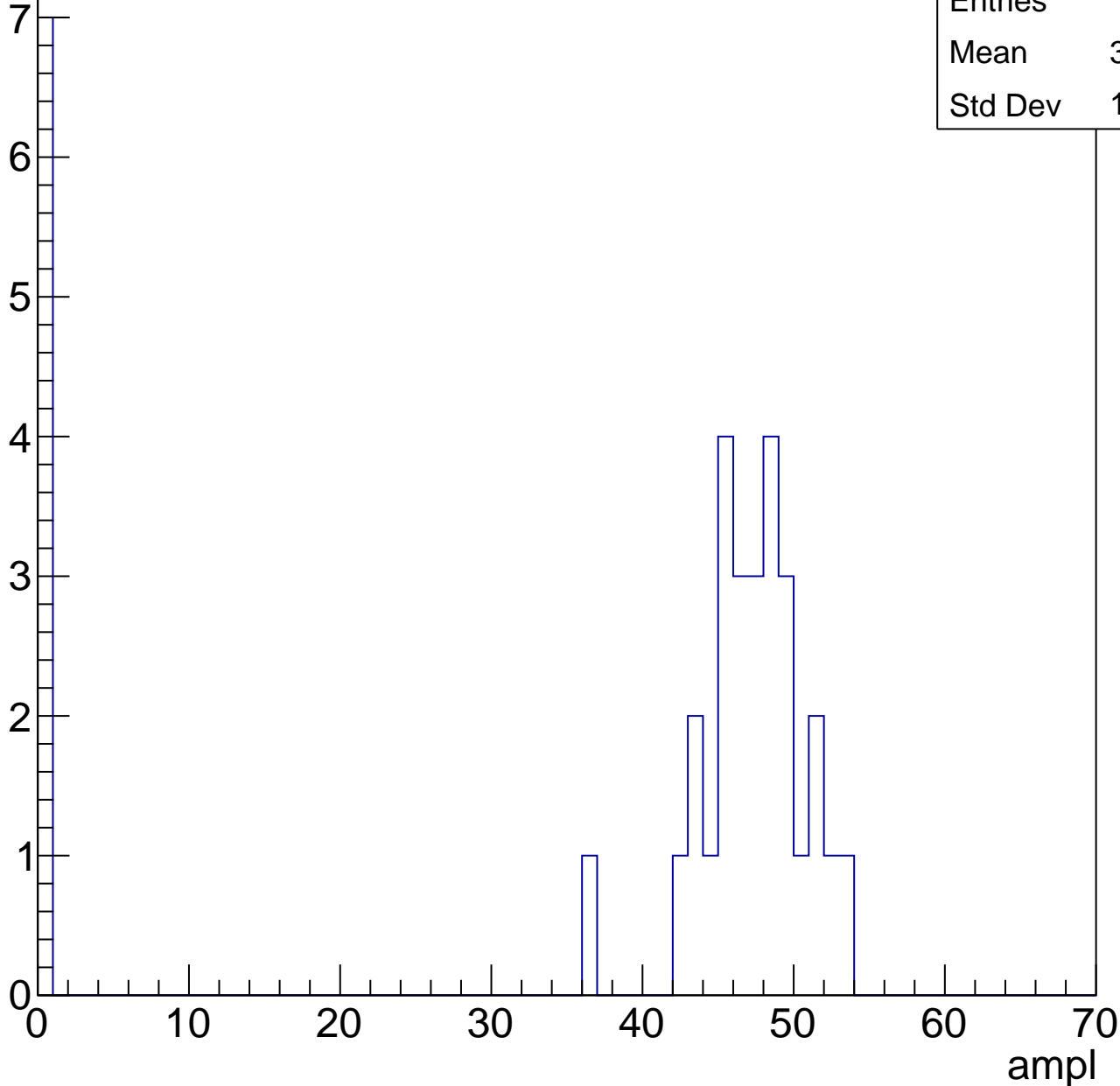


B1L103S, U14-ch72, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

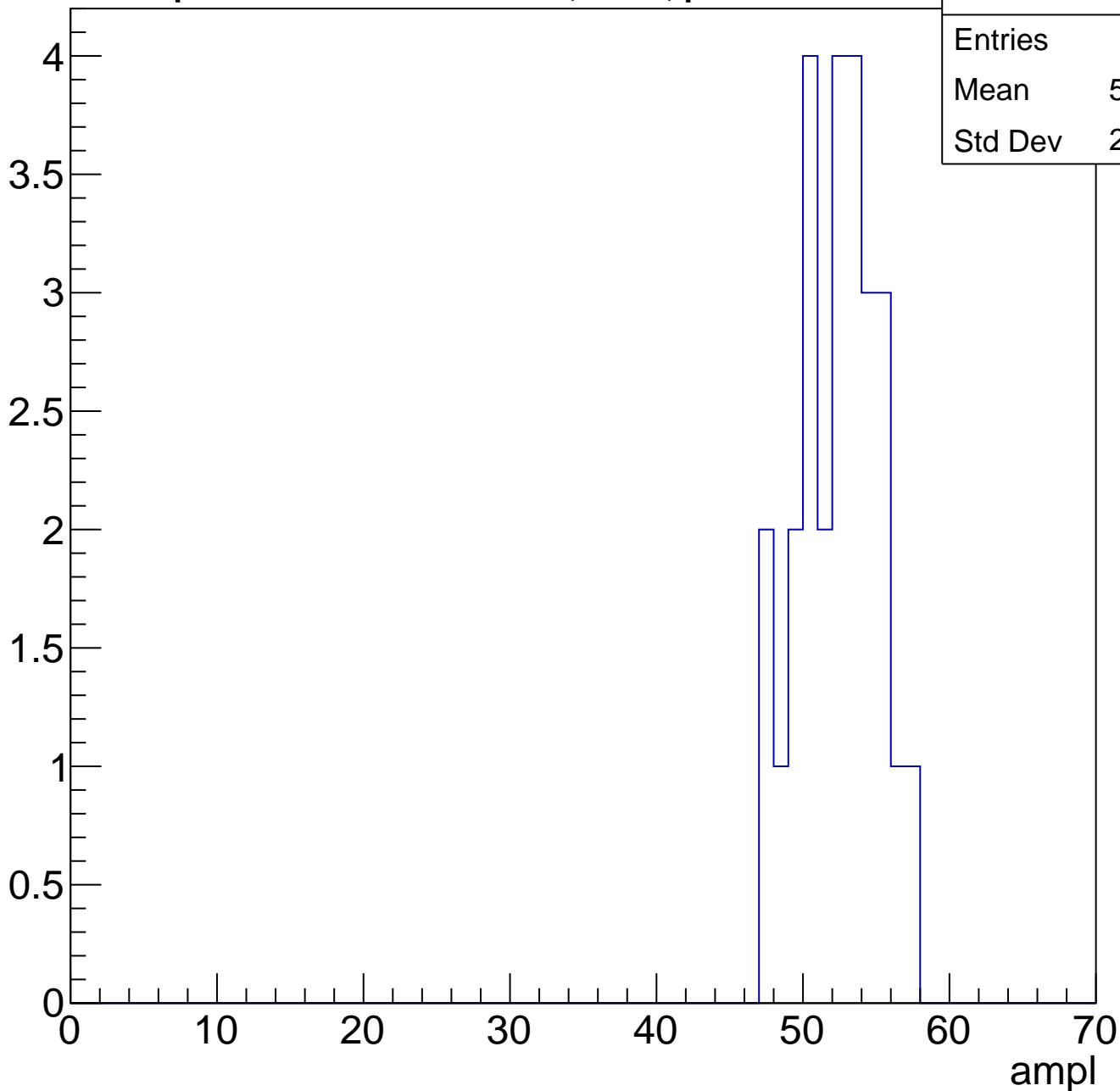
Entries	34
Mean	37.15
Std Dev	19.16



B1L103S, U14-ch72, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



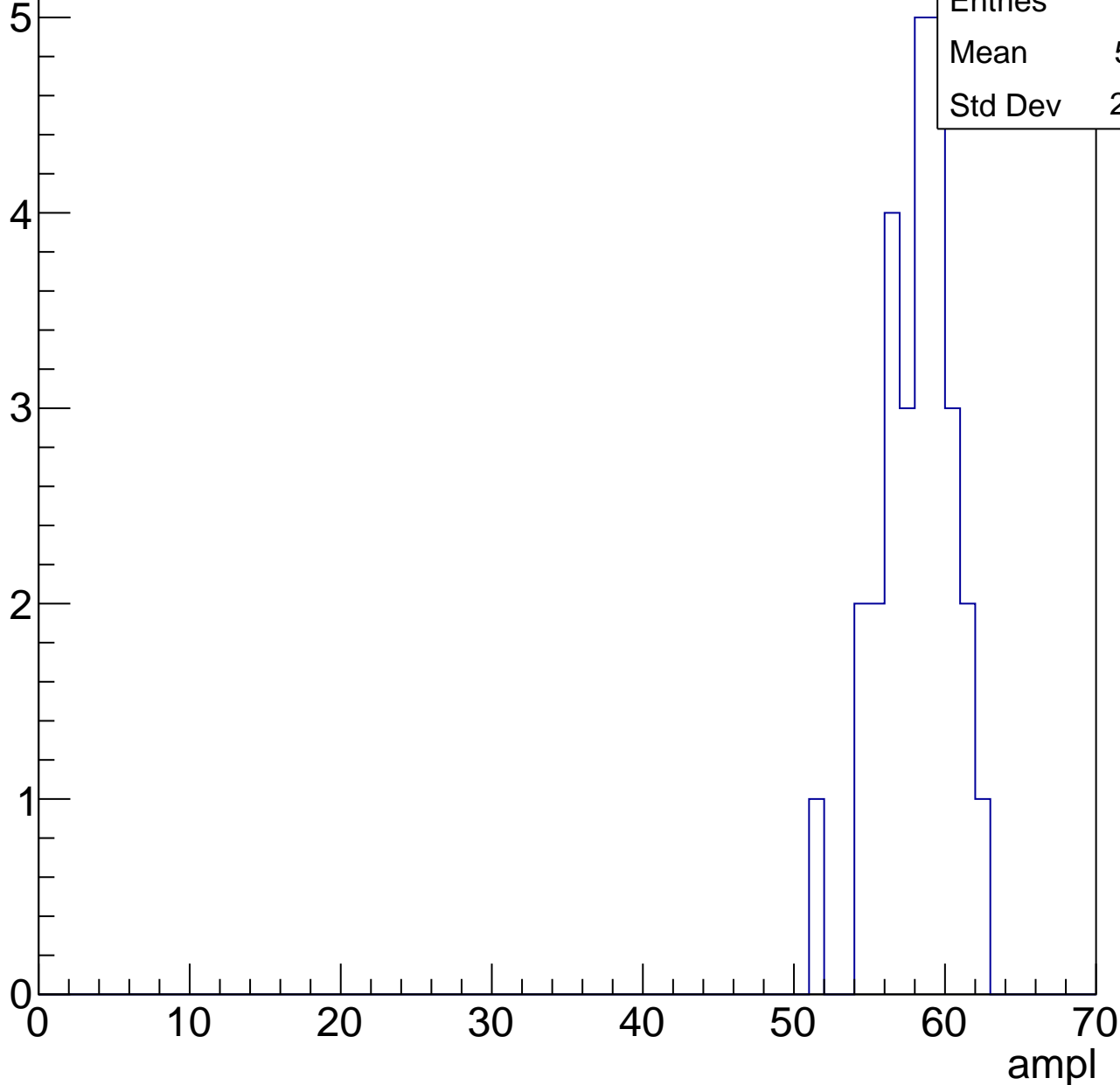
Entries	27
Mean	51.93
Std Dev	2.624

B1L103S, U14-ch72, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

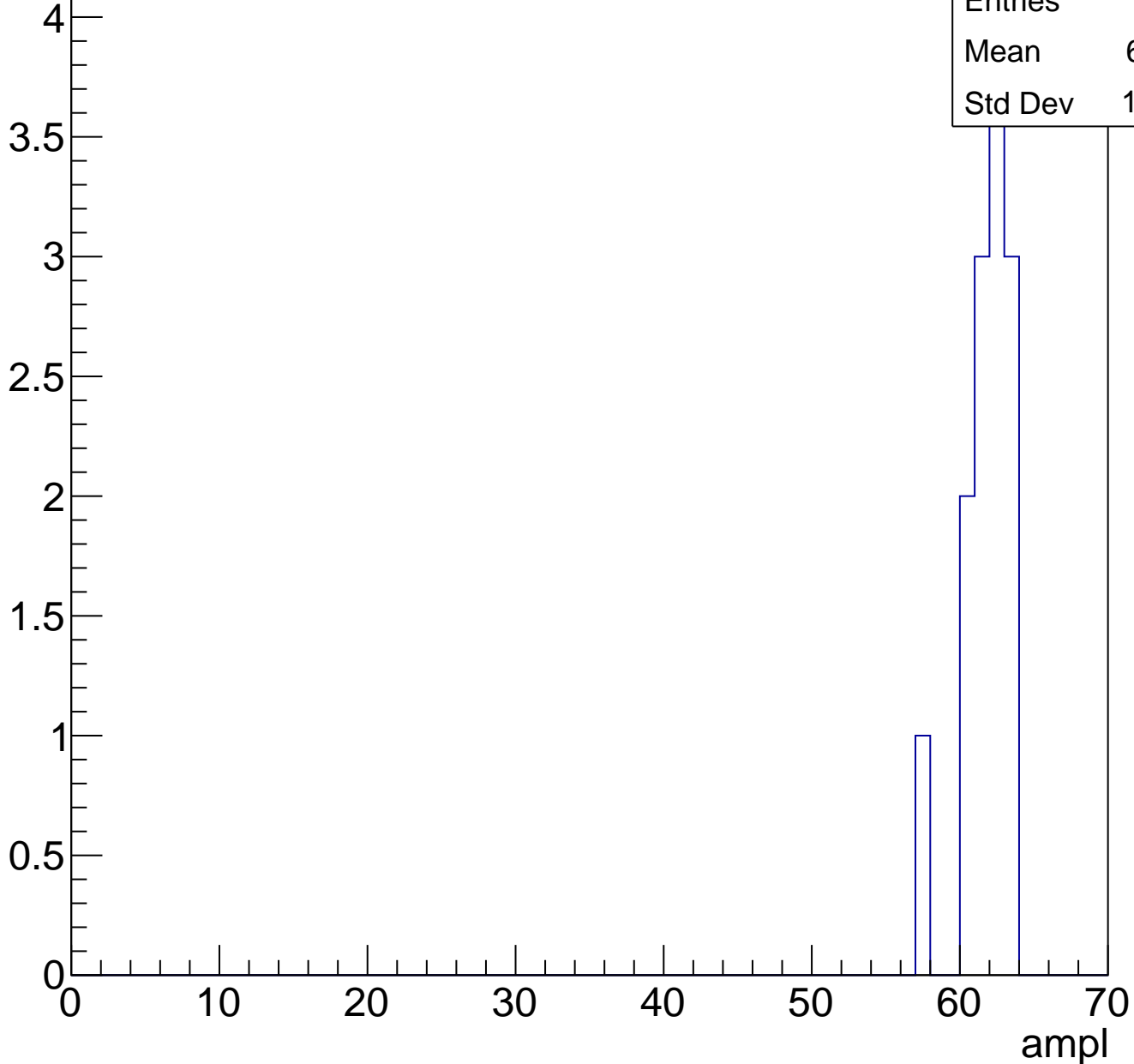
Entries	28
Mean	57.61
Std Dev	2.425



B1L103S, U14-ch72, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

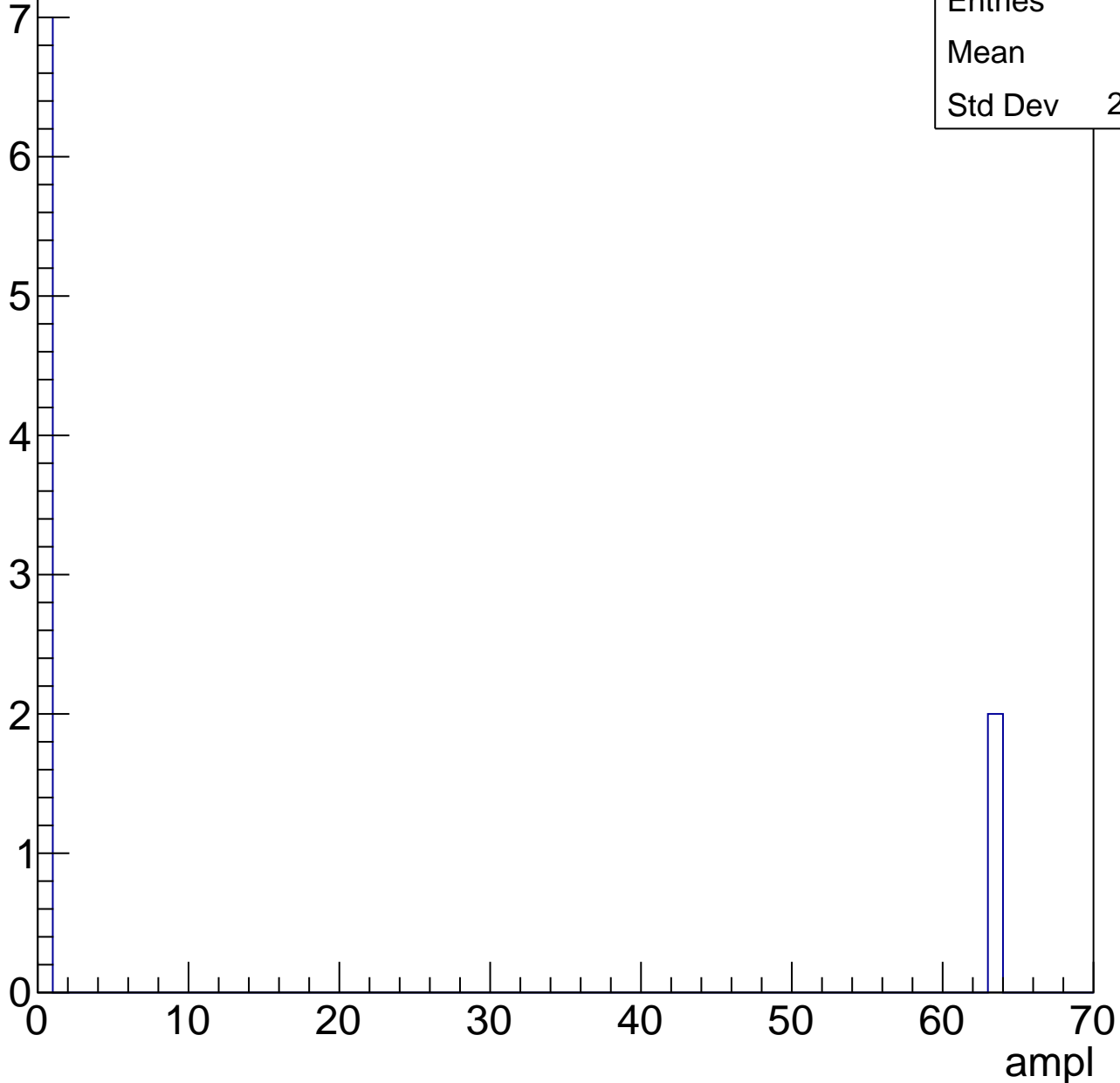


B1L103S, U14-ch72, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	9
Mean	14
Std Dev	26.19



B1L103S, U14-ch73, adc0

calib_packv5_041523_1651.root, FC#0, port C2

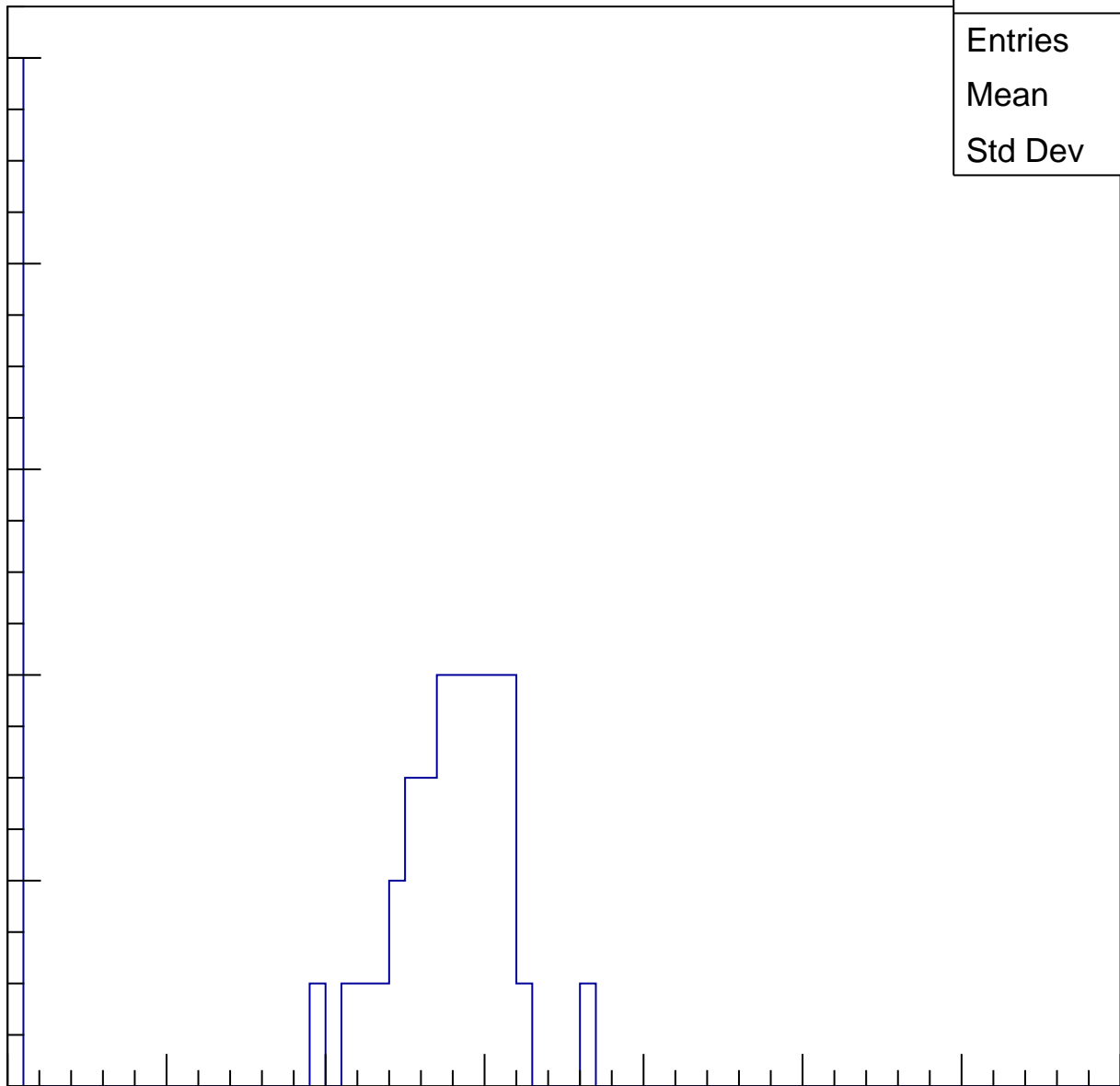
Entries	44
Mean	21.23
Std Dev	11.89

Entry

10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

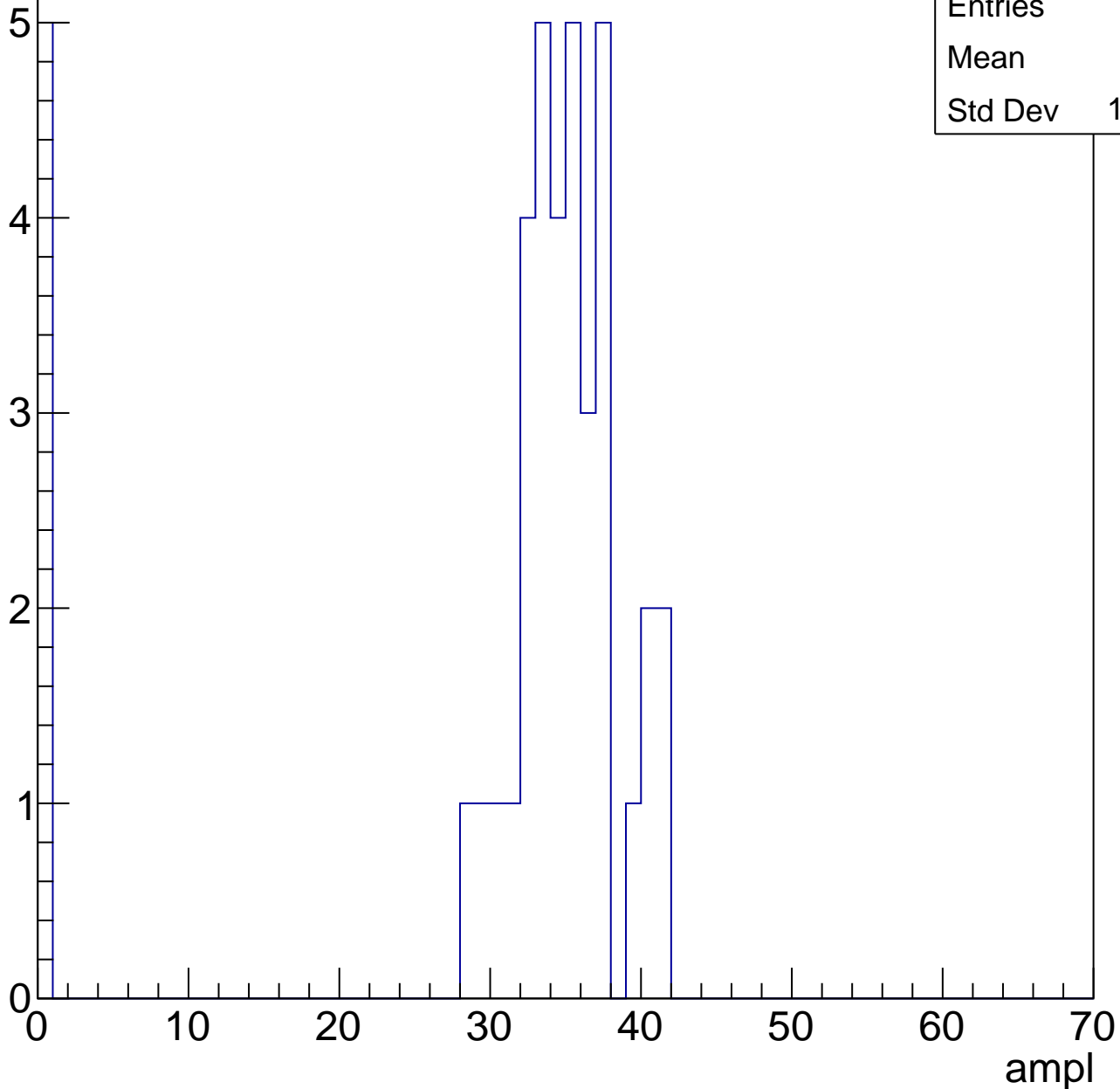


B1L103S, U14-ch73, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	30.4
Std Dev	11.86

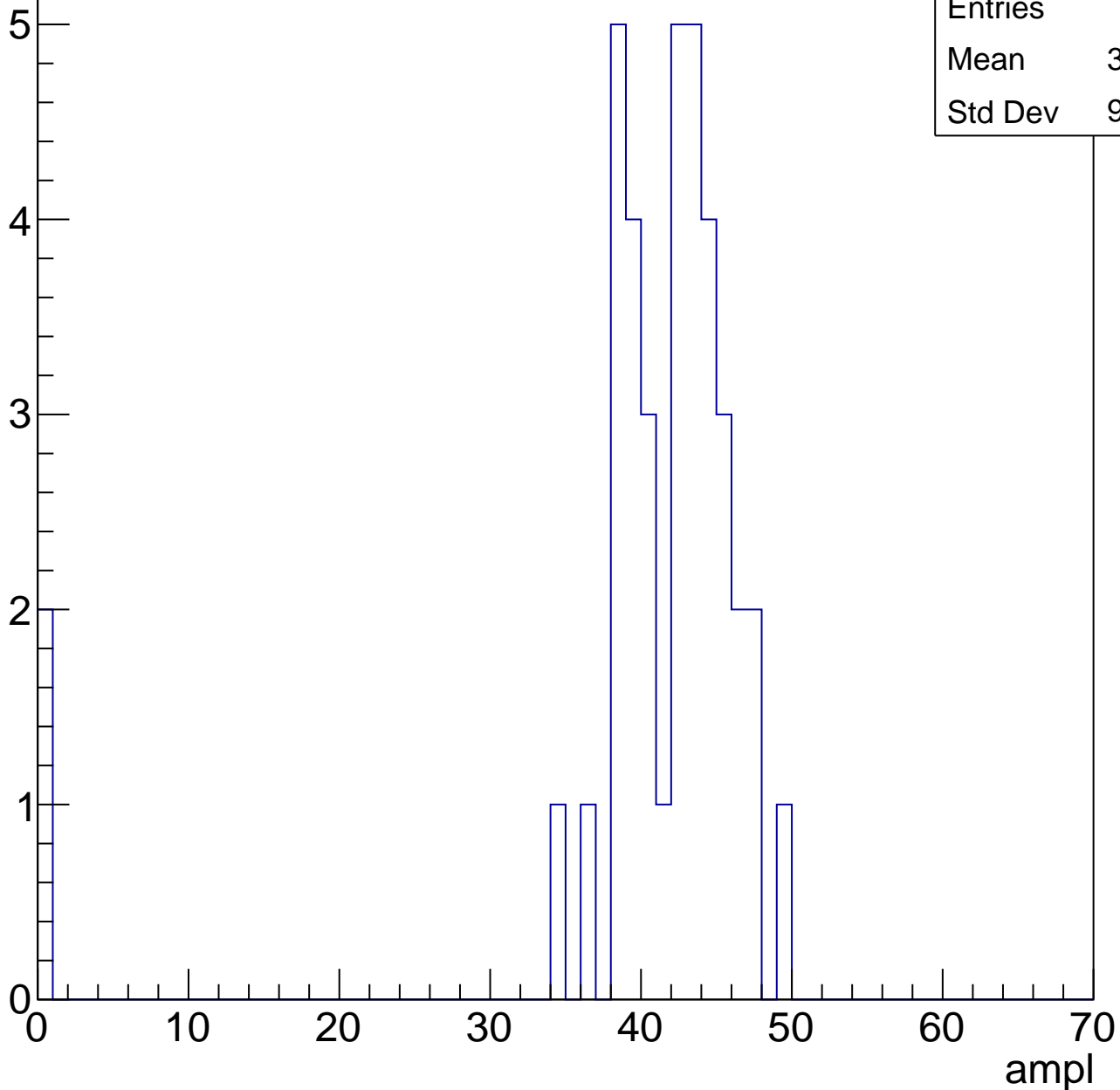


B1L103S, U14-ch73, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

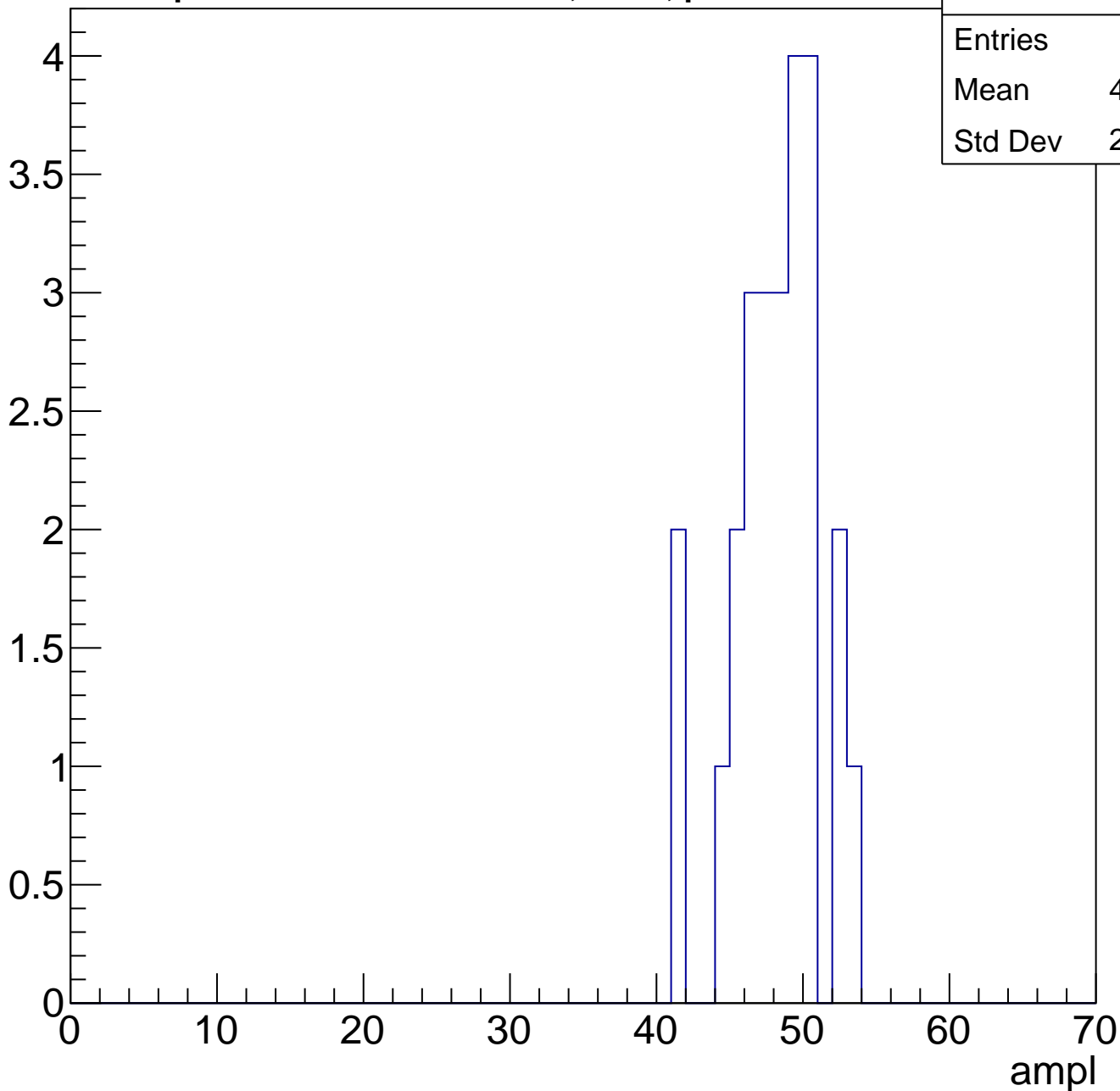
Entries	39
Mean	39.69
Std Dev	9.777



B1L103S, U14-ch73, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

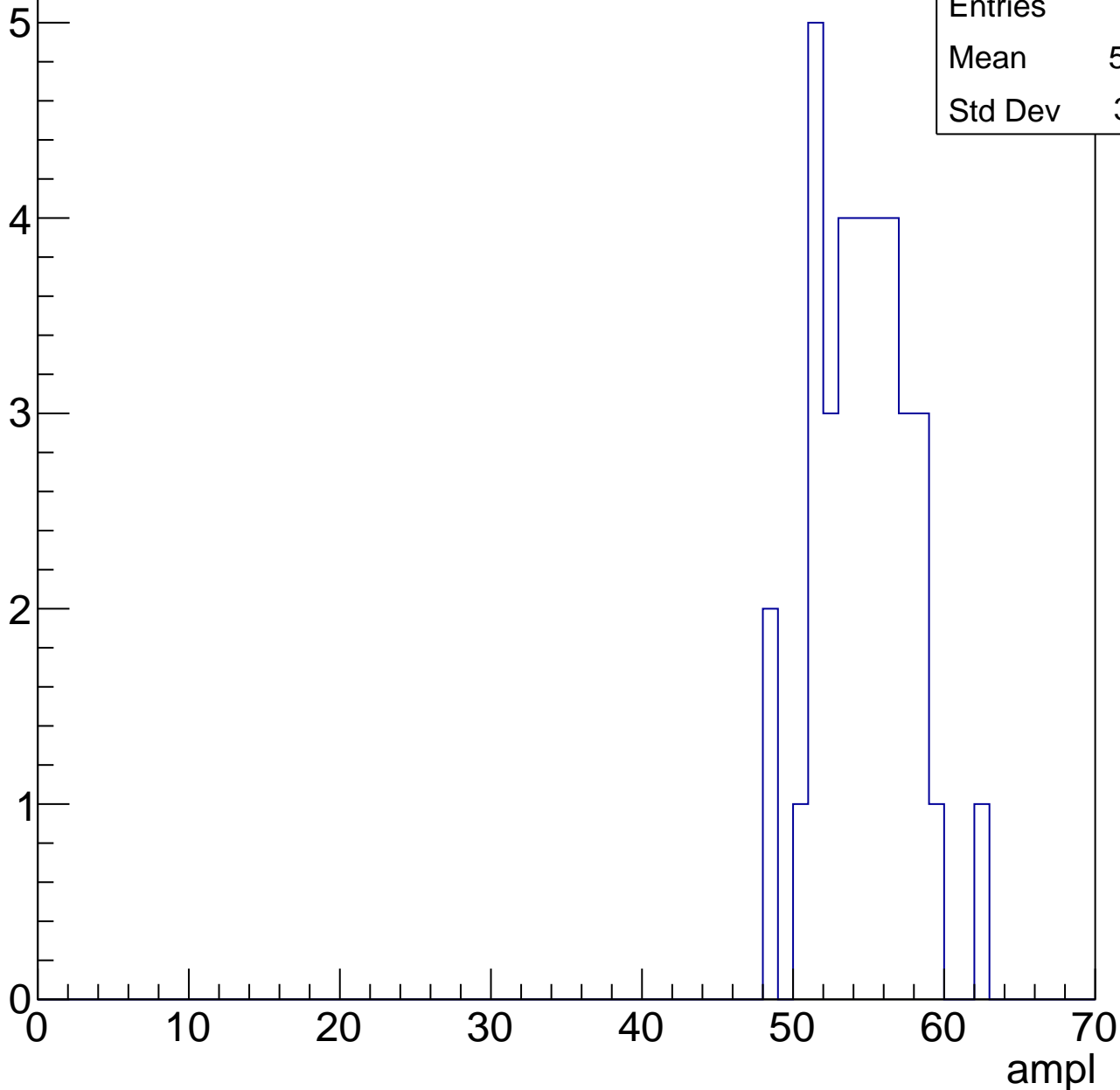


B1L103S, U14-ch73, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

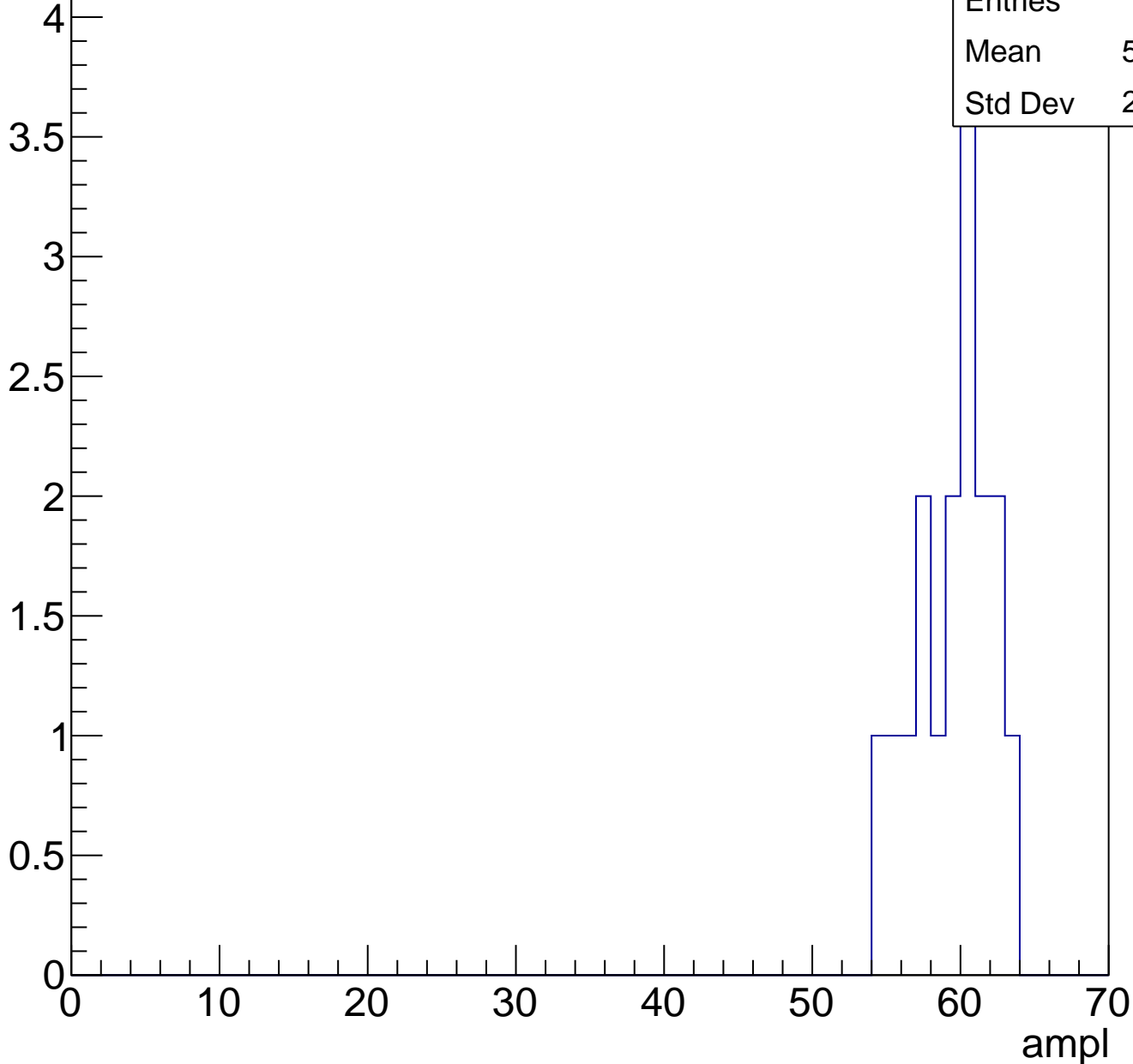
Entries	35
Mean	54.14
Std Dev	3.081



B1L103S, U14-ch73, adc5

calib_packv5_041523_1651.root, FC#0, port C2

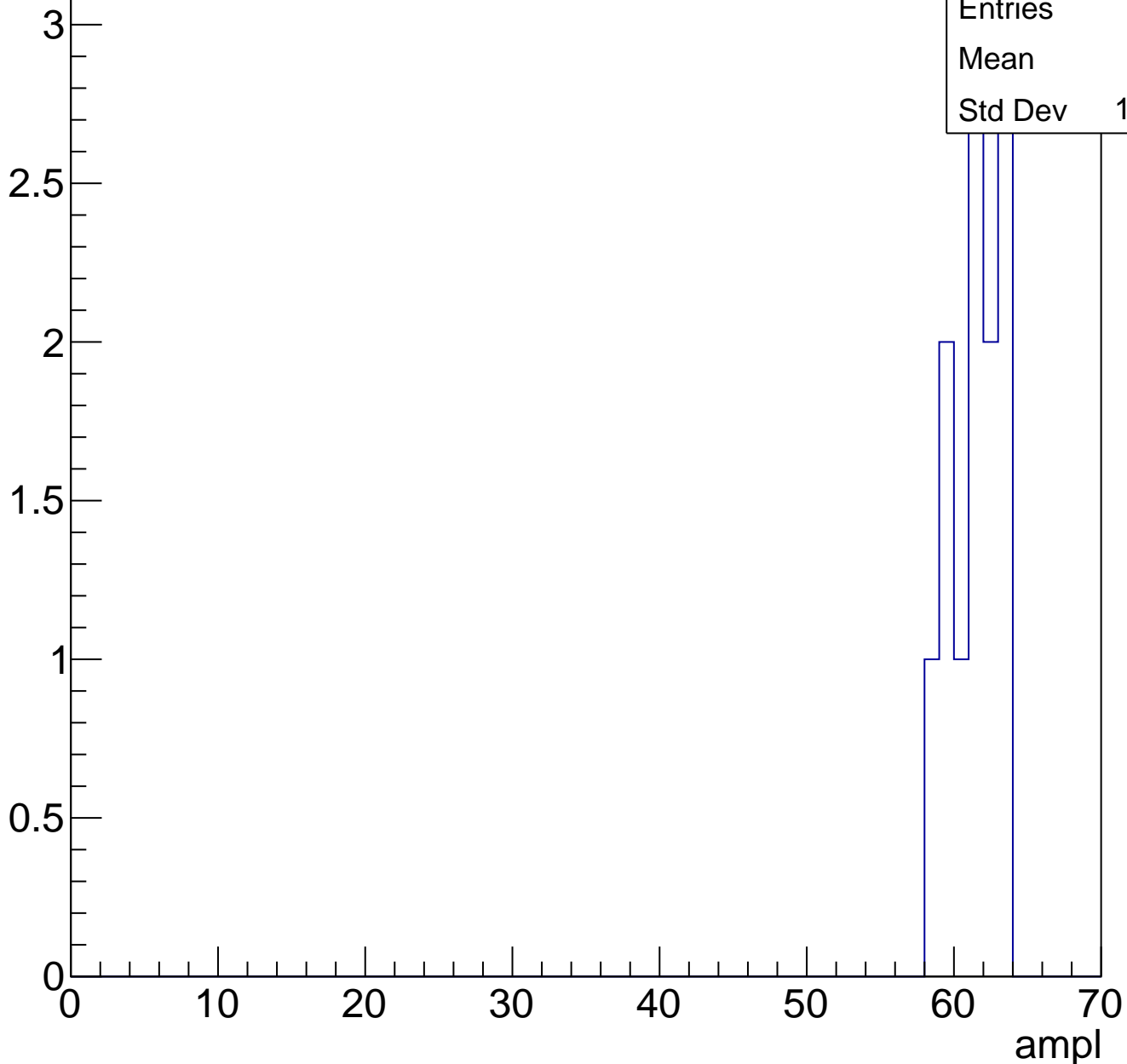
Entry



B1L103S, U14-ch73, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch73, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

8

6

4

2

0

Entries	11
Mean	5.727
Std Dev	18.11

ampl

0

10

20

30

40

50

60

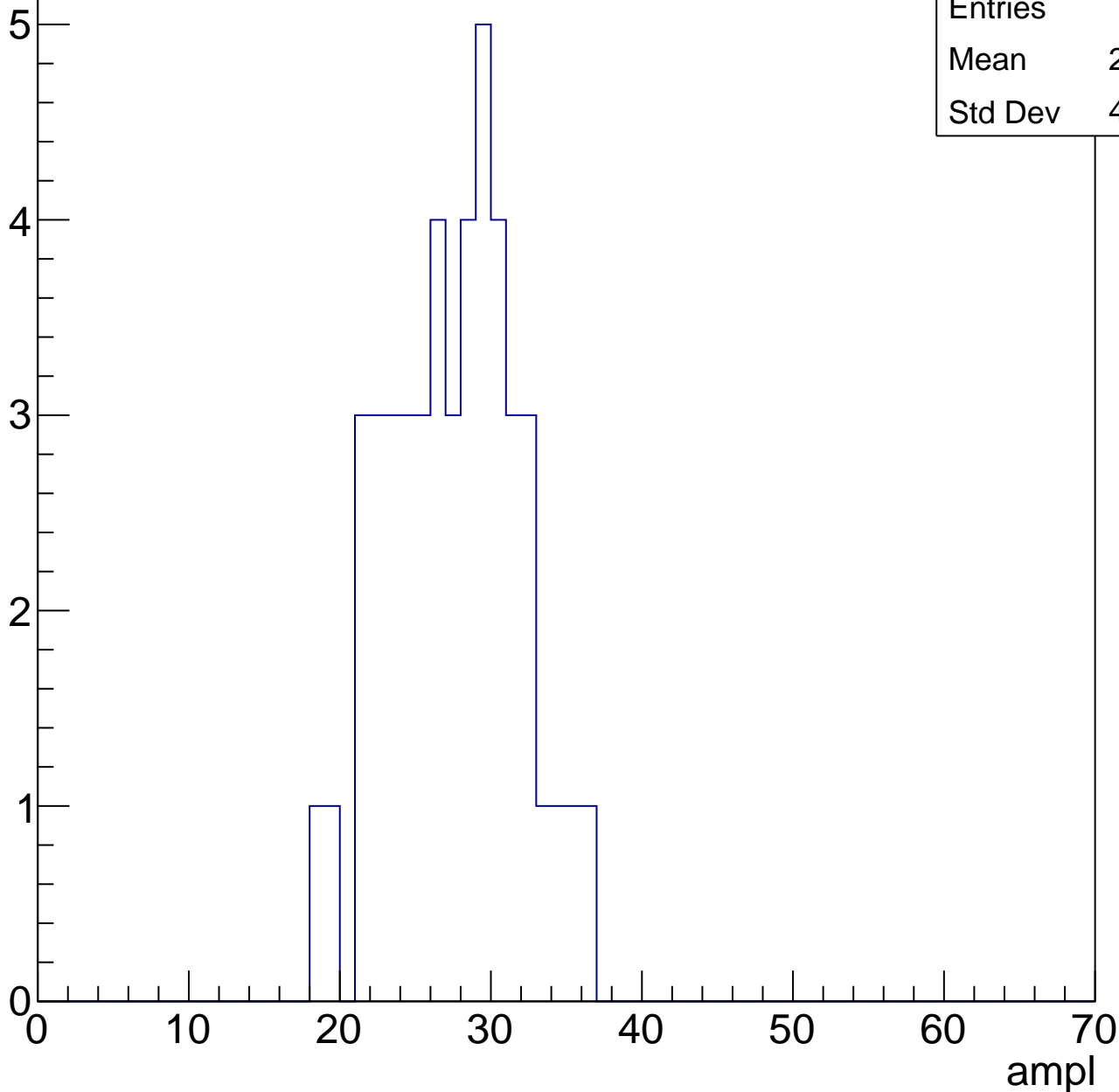
70

B1L103S, U14-ch74, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

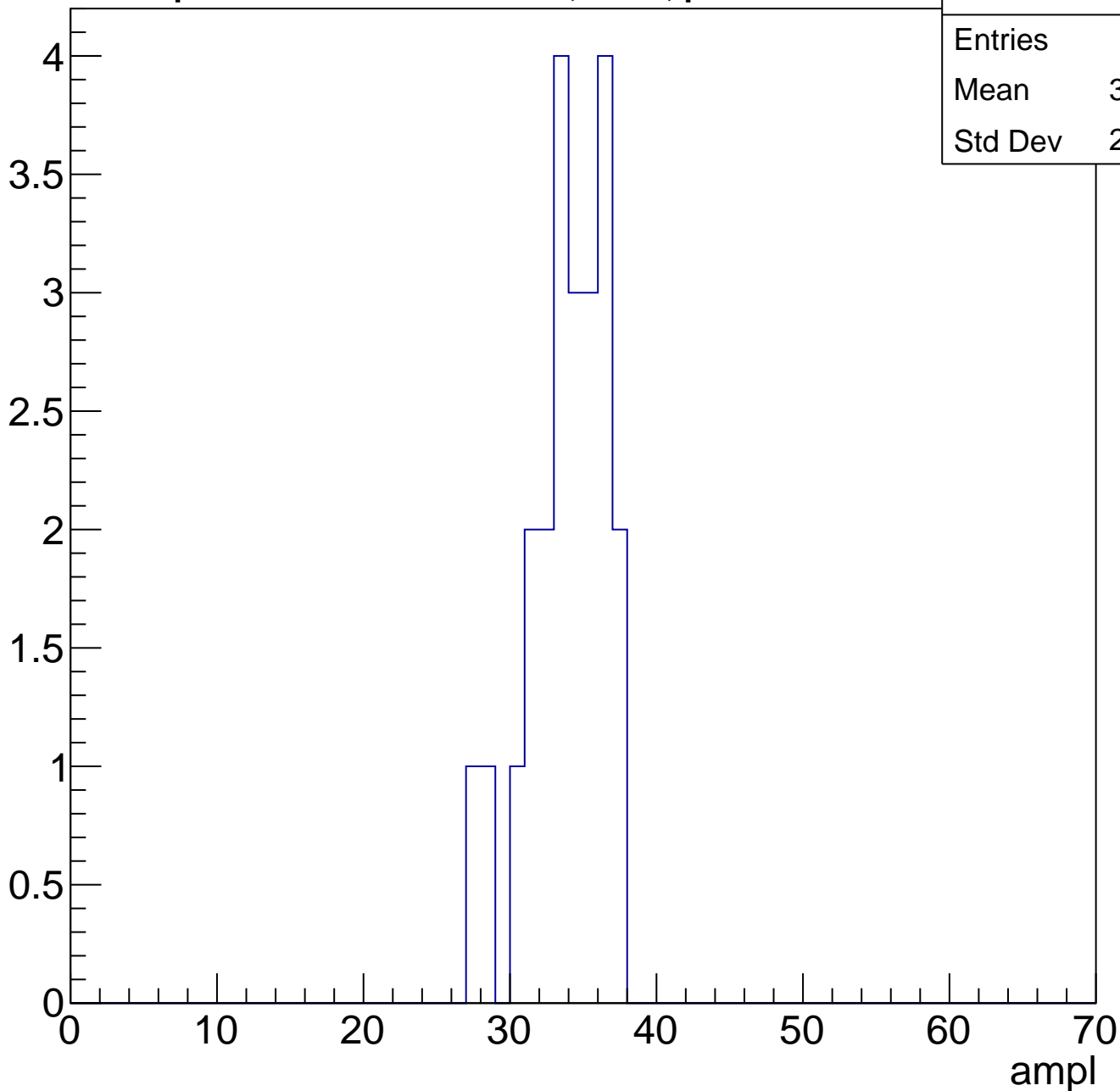
Entries	47
Mean	27.04
Std Dev	4.207



B1L103S, U14-ch74, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry



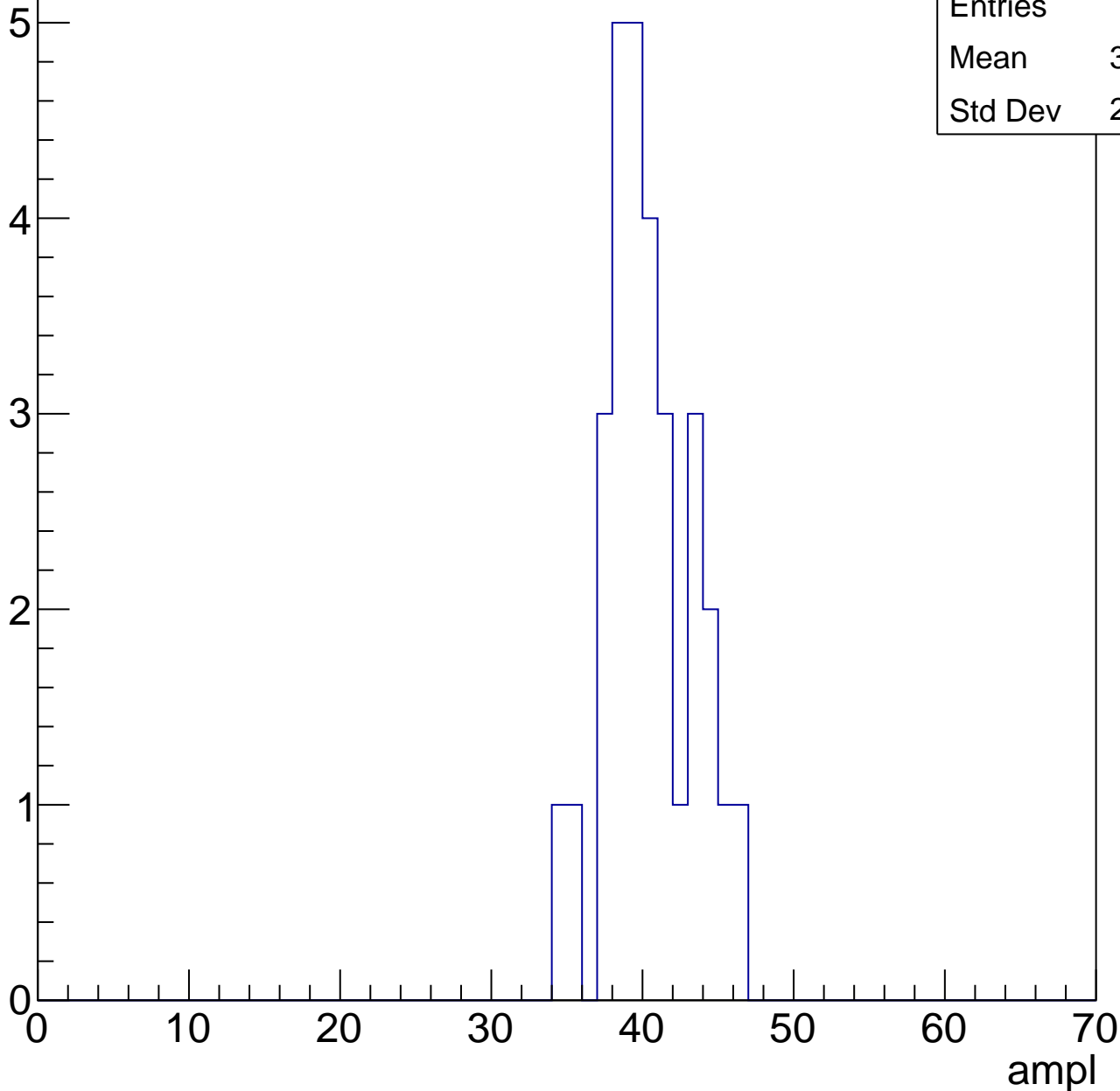
Entries	23
Mean	33.39
Std Dev	2.633

B1L103S, U14-ch74, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	30
Mean	39.93
Std Dev	2.828

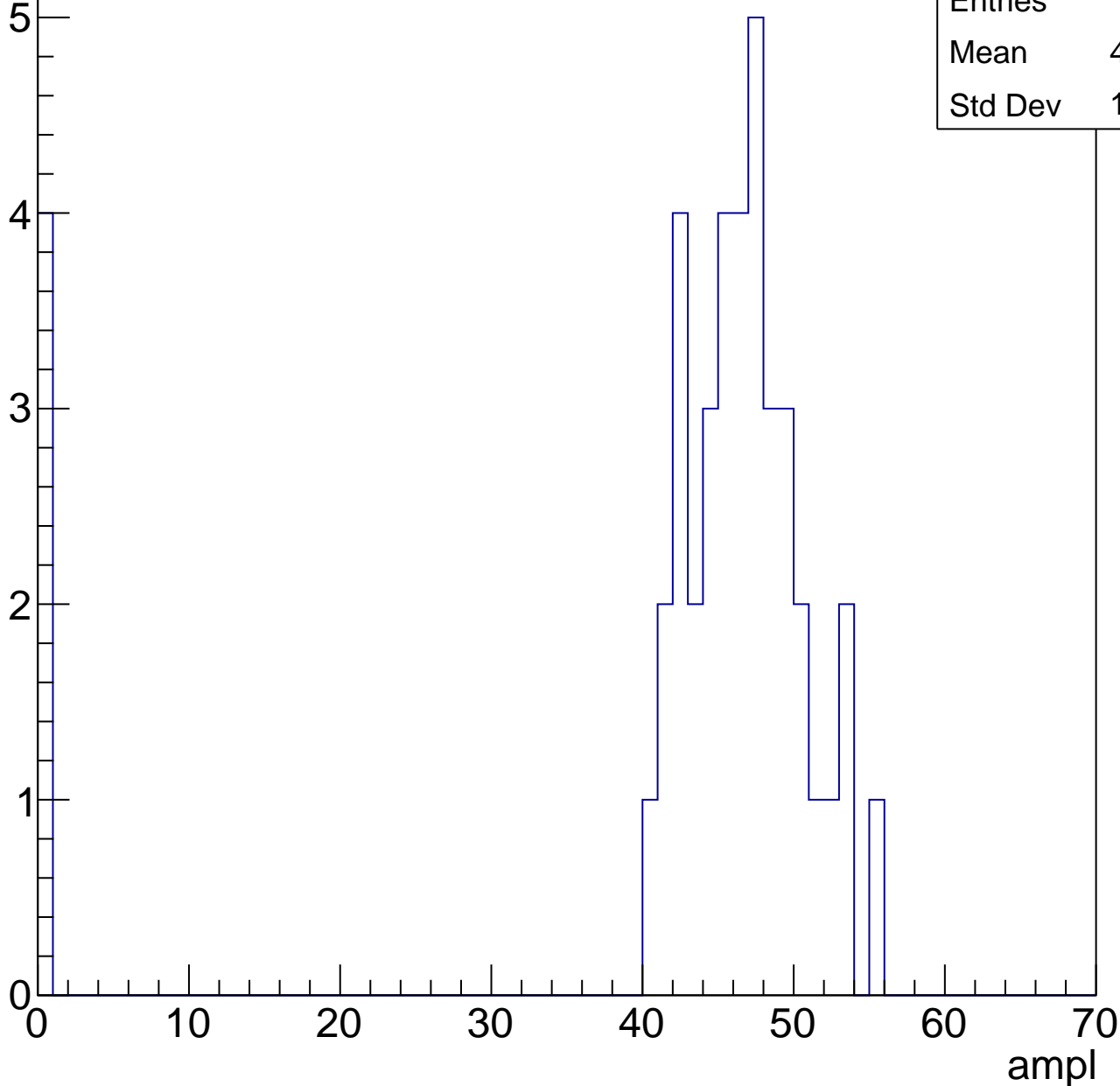


B1L103S, U14-ch74, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

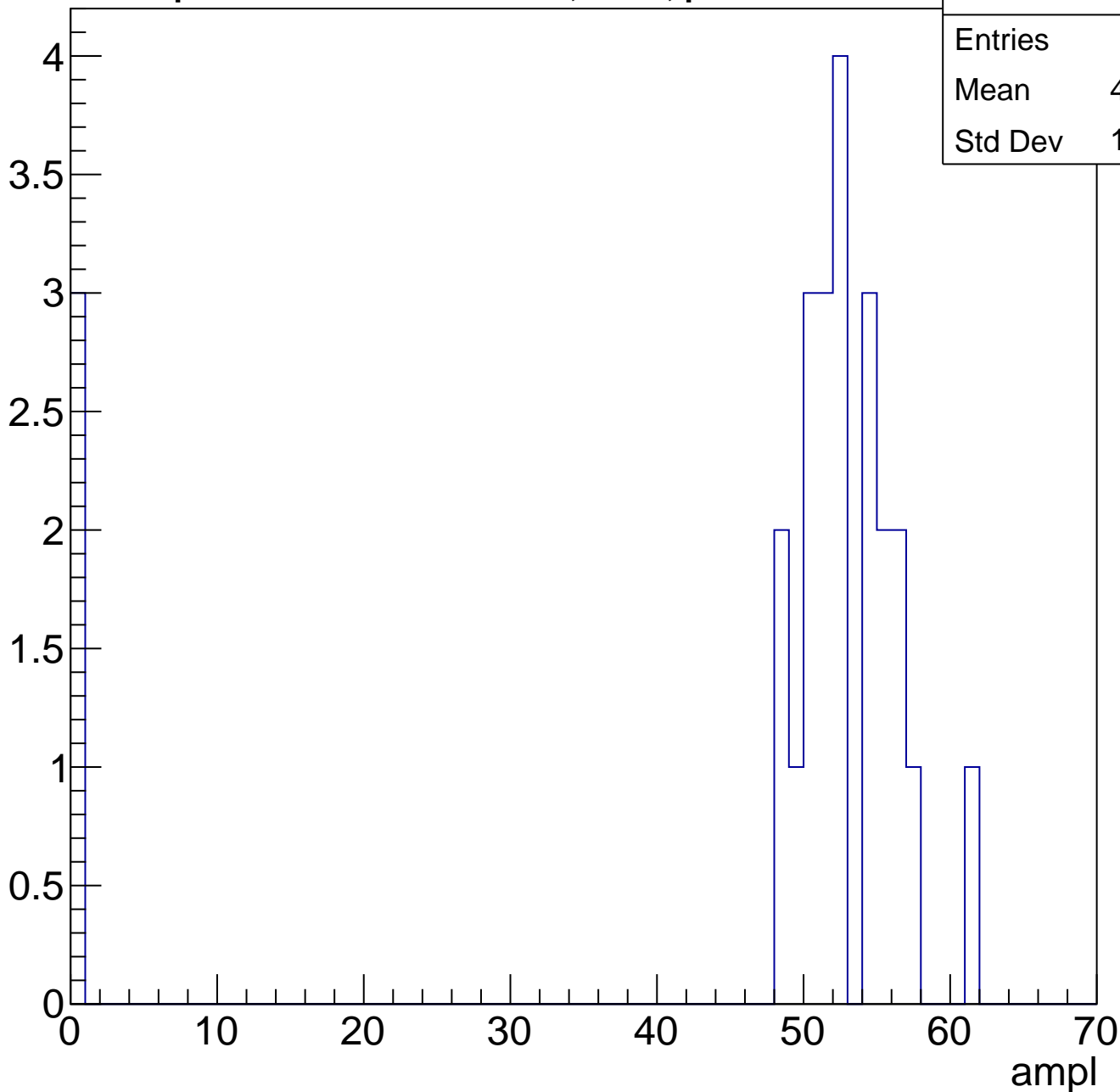
Entries	42
Mean	41.95
Std Dev	14.04



B1L103S, U14-ch74, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

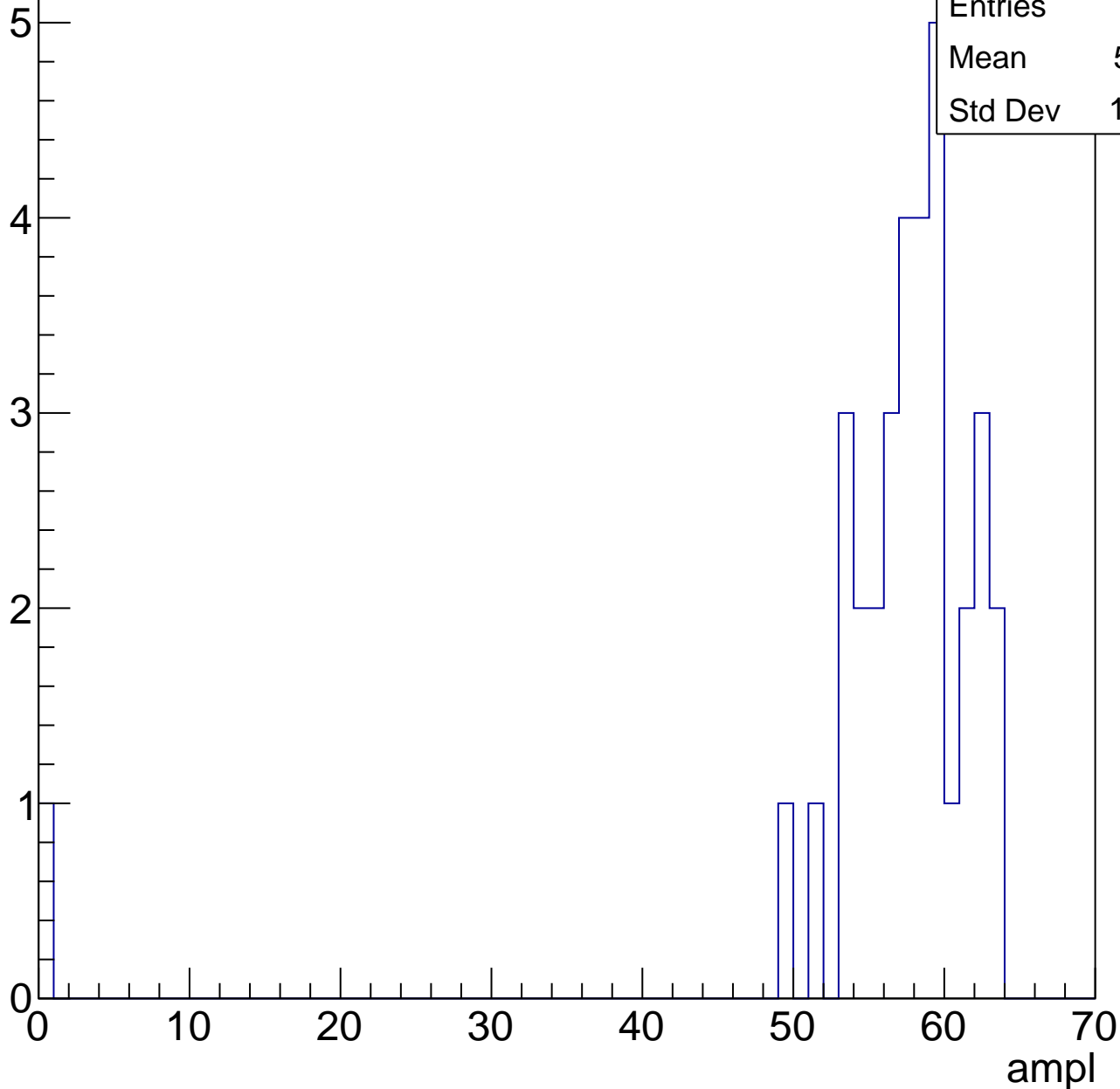


B1L103S, U14-ch74, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

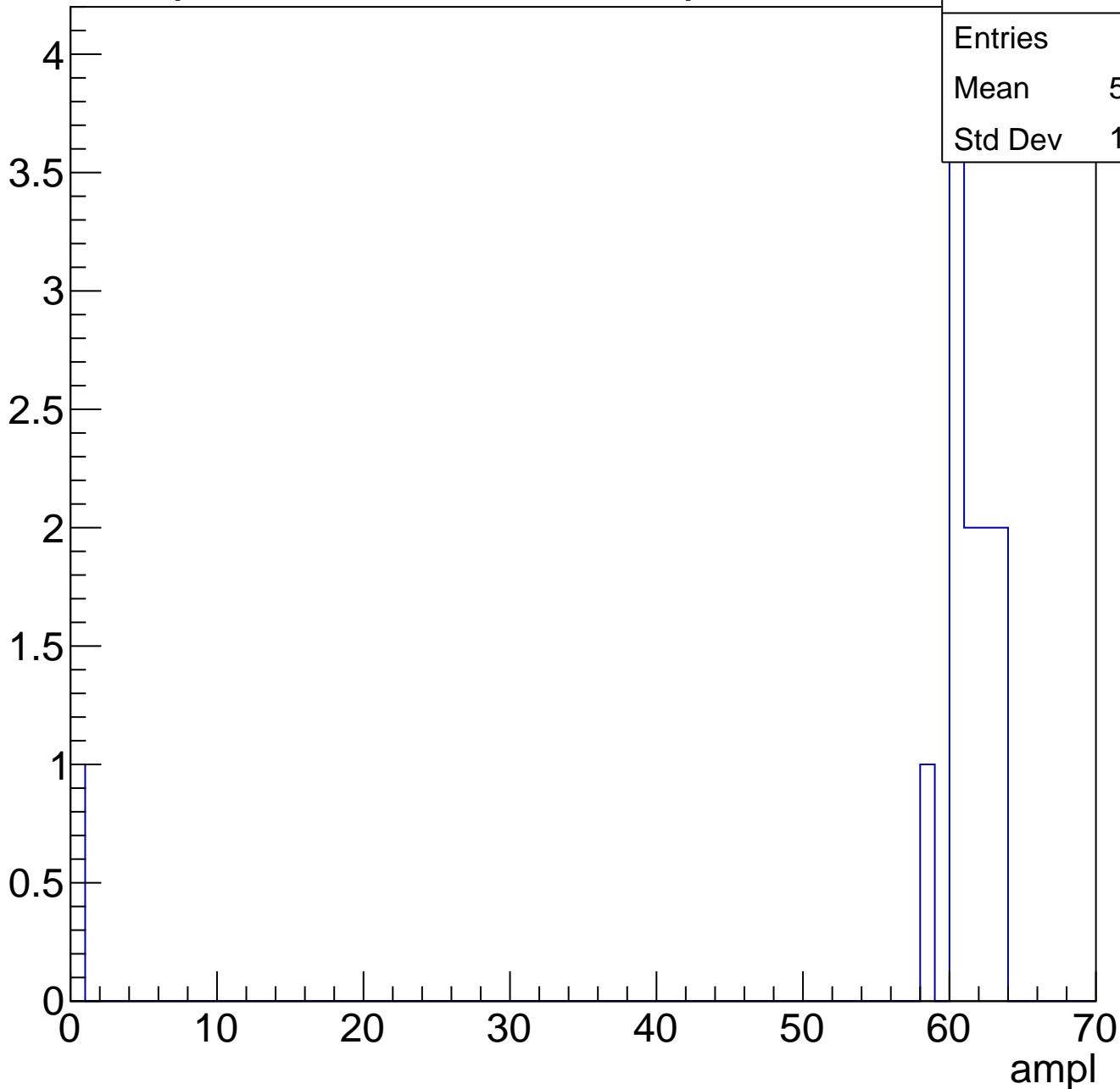
Entries	34
Mean	55.71
Std Dev	10.26



B1L103S, U14-ch74, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

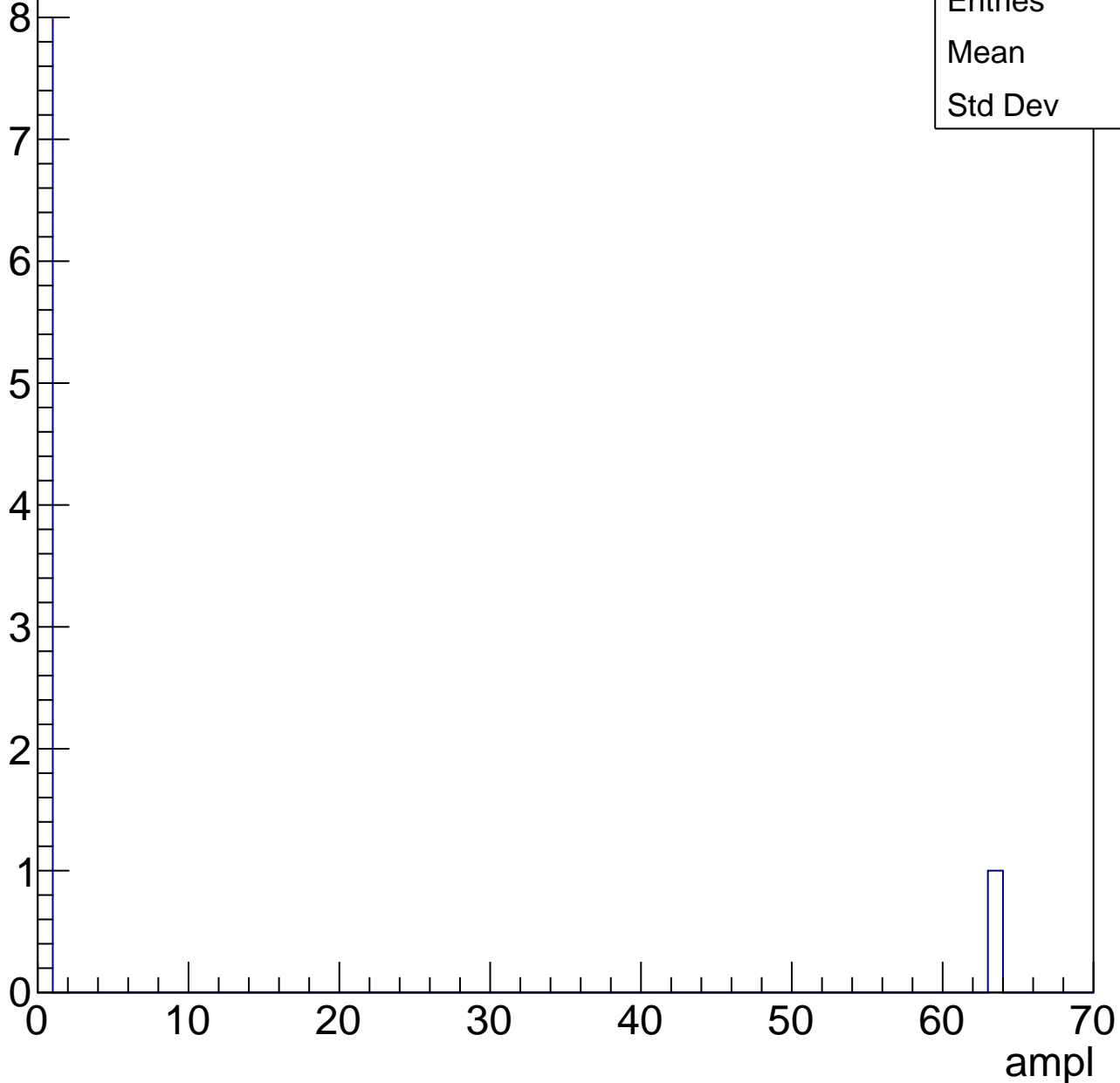


B1L103S, U14-ch74, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	9
Mean	7
Std Dev	19.8

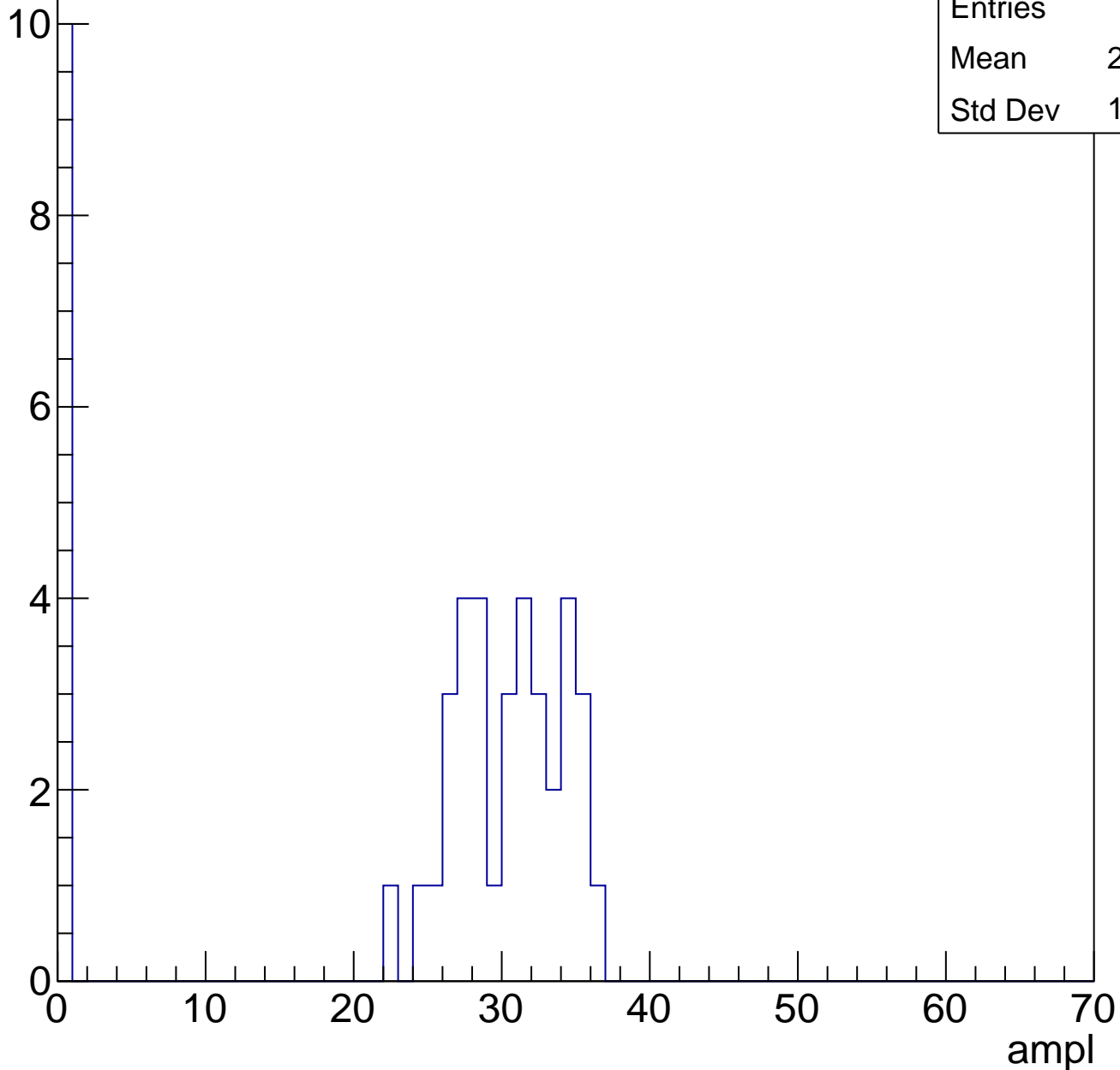


B1L103S, U14-ch75, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	45
Mean	23.36
Std Dev	12.87

Entry

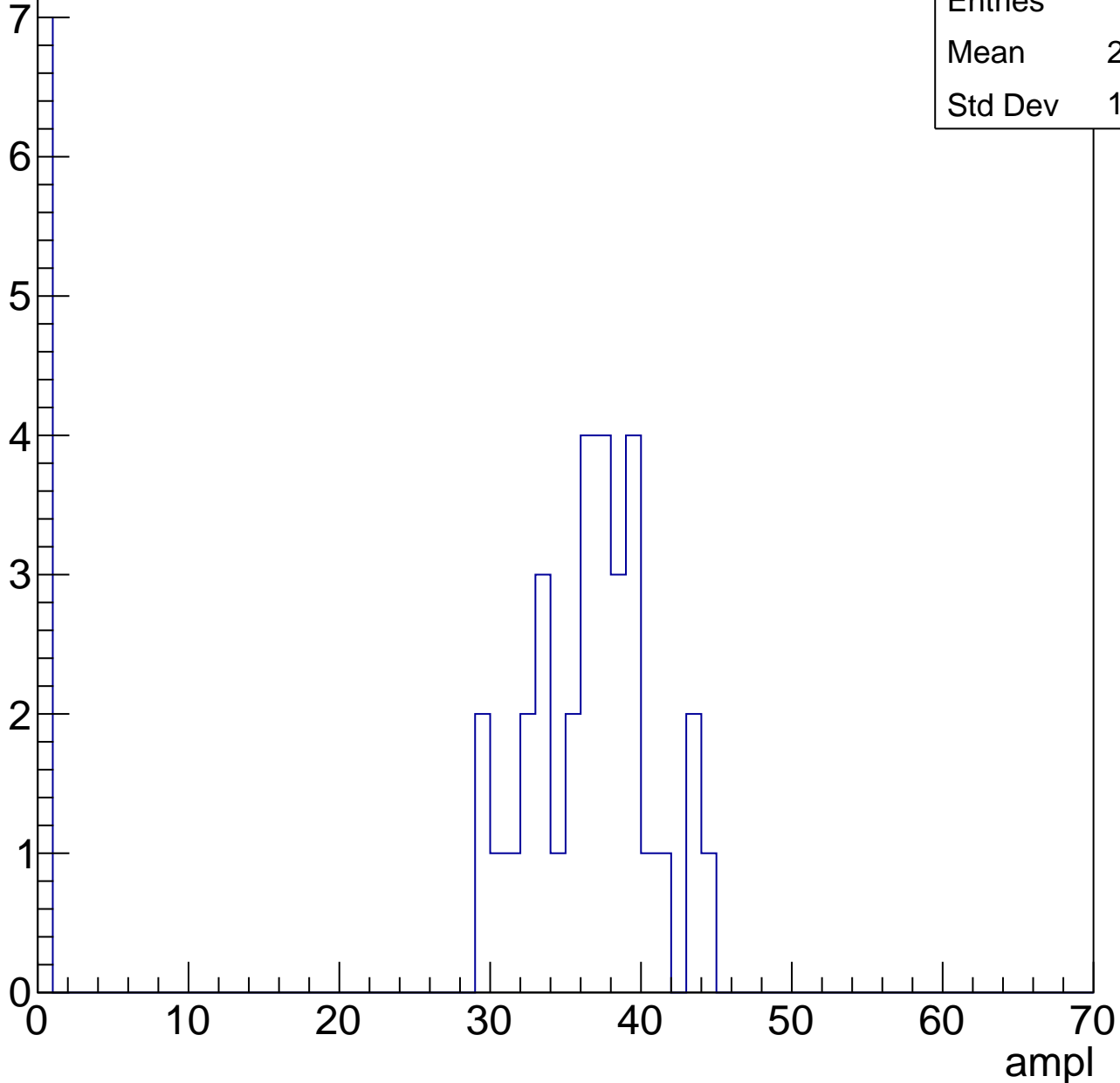


B1L103S, U14-ch75, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	29.72
Std Dev	14.33

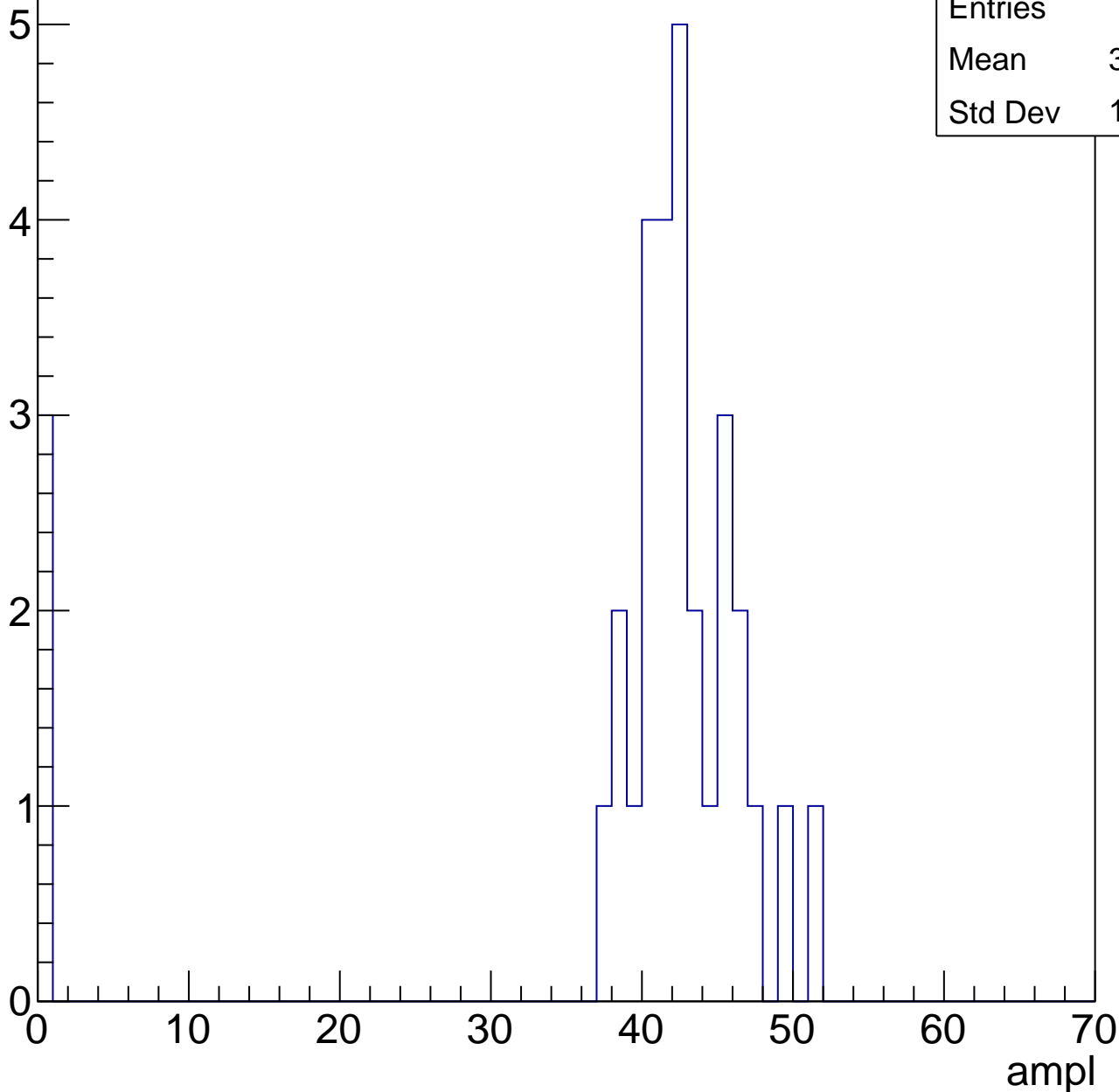


B1L103S, U14-ch75, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

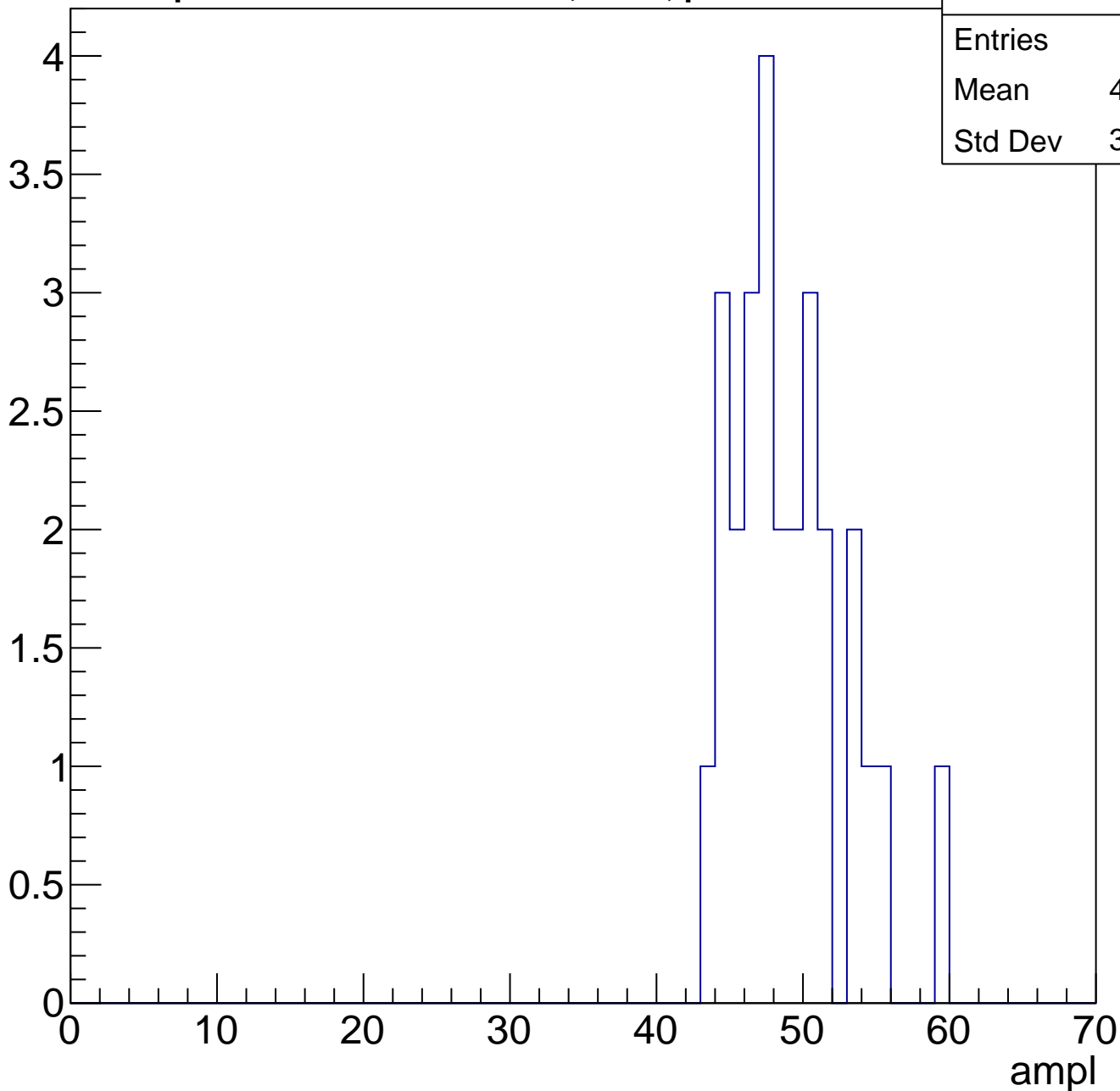
Entries	31
Mean	38.39
Std Dev	12.94



B1L103S, U14-ch75, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

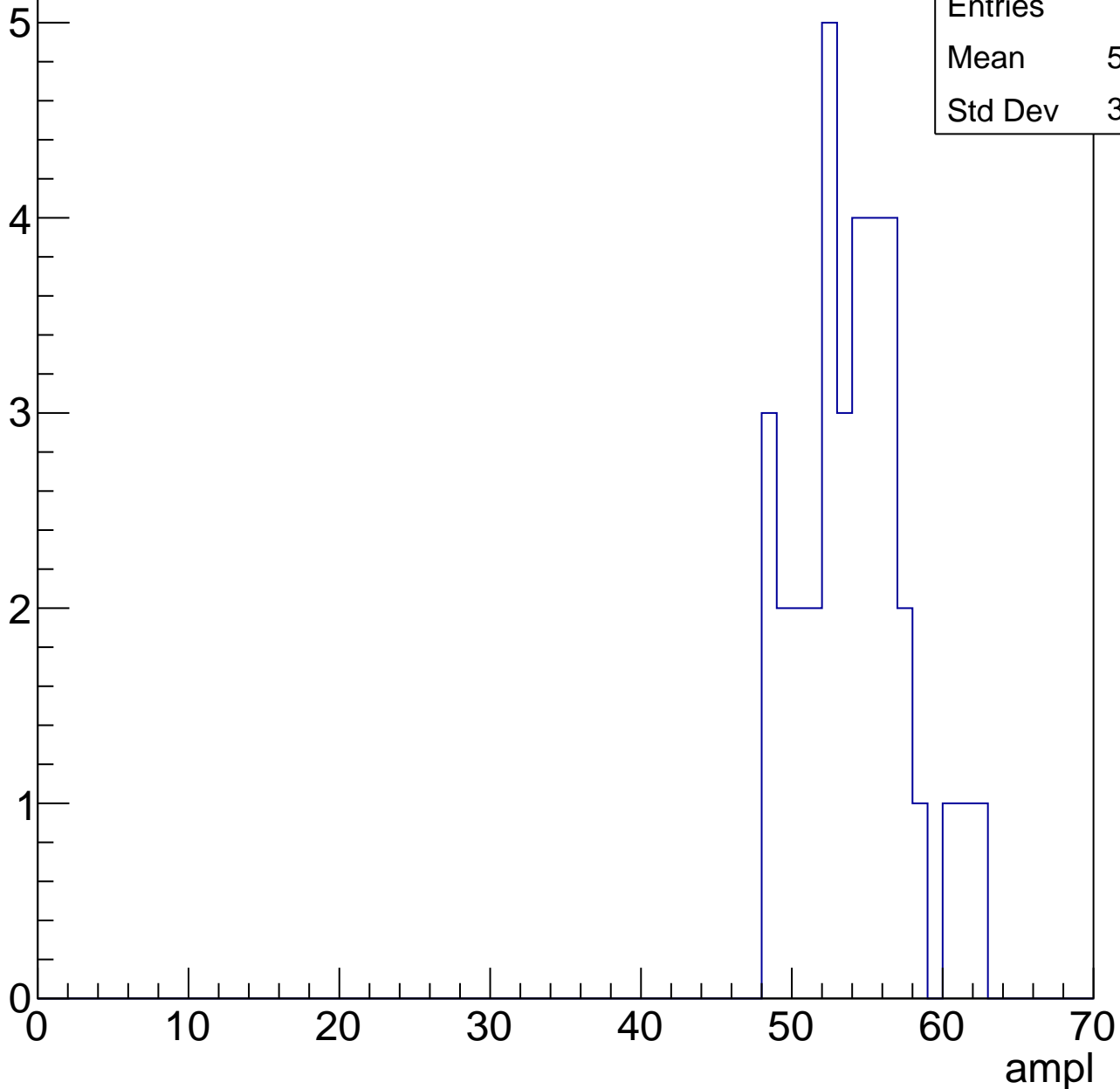


B1L103S, U14-ch75, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

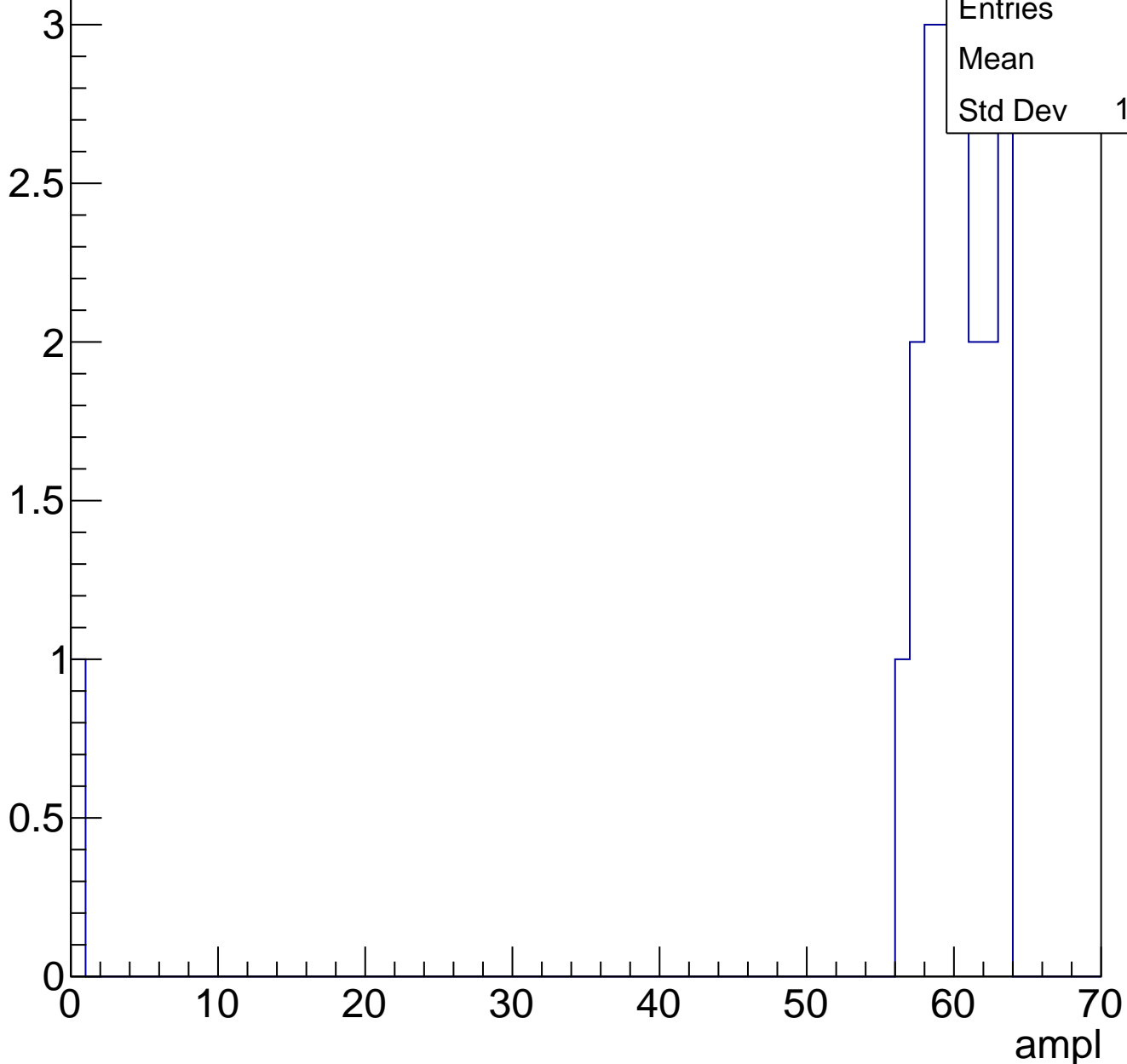
Entries	35
Mean	53.66
Std Dev	3.505



B1L103S, U14-ch75, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch75, adc6

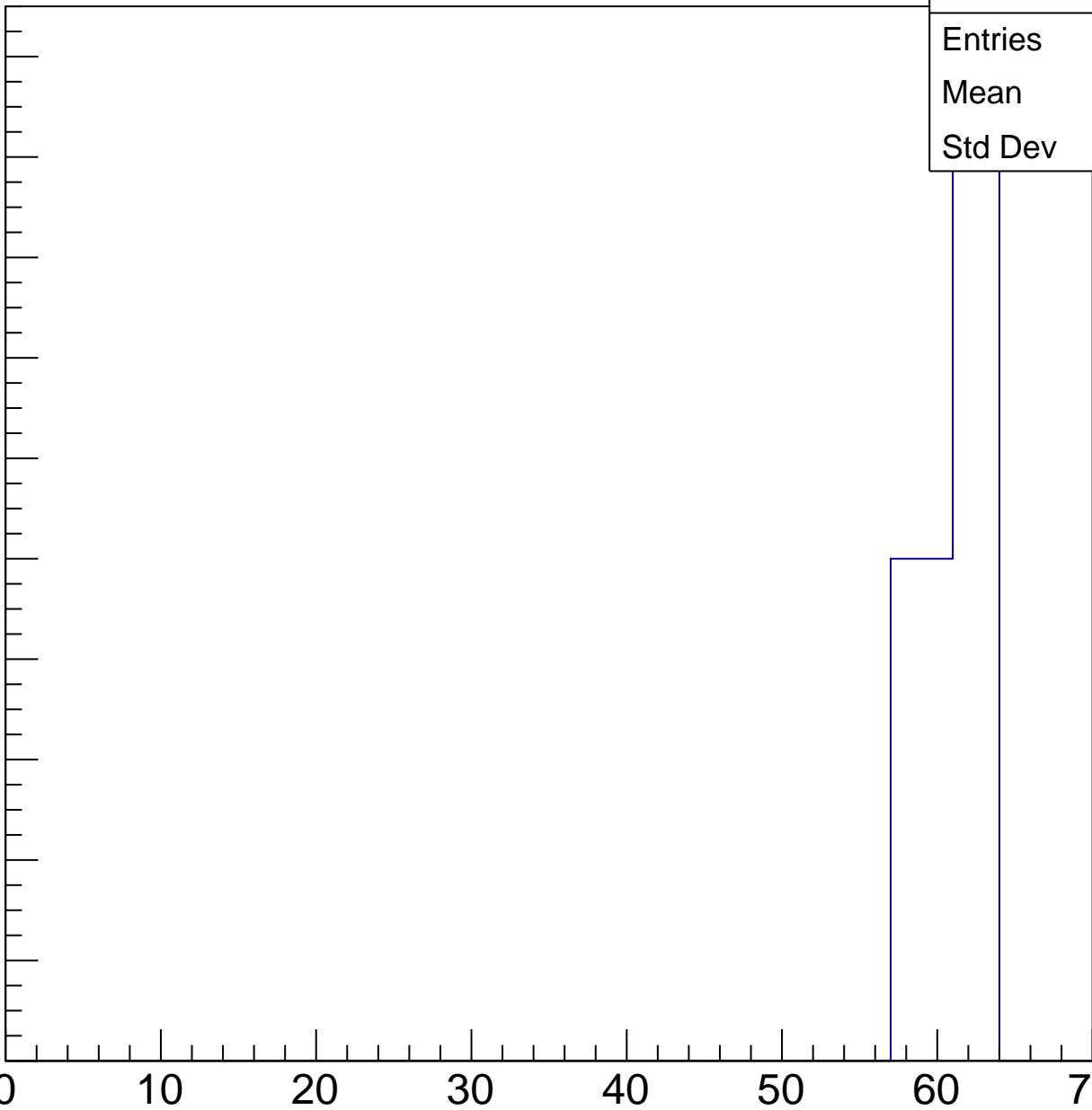
calib_packv5_041523_1651.root, FC#0, port C2

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	10
Mean	60.6
Std Dev	1.96

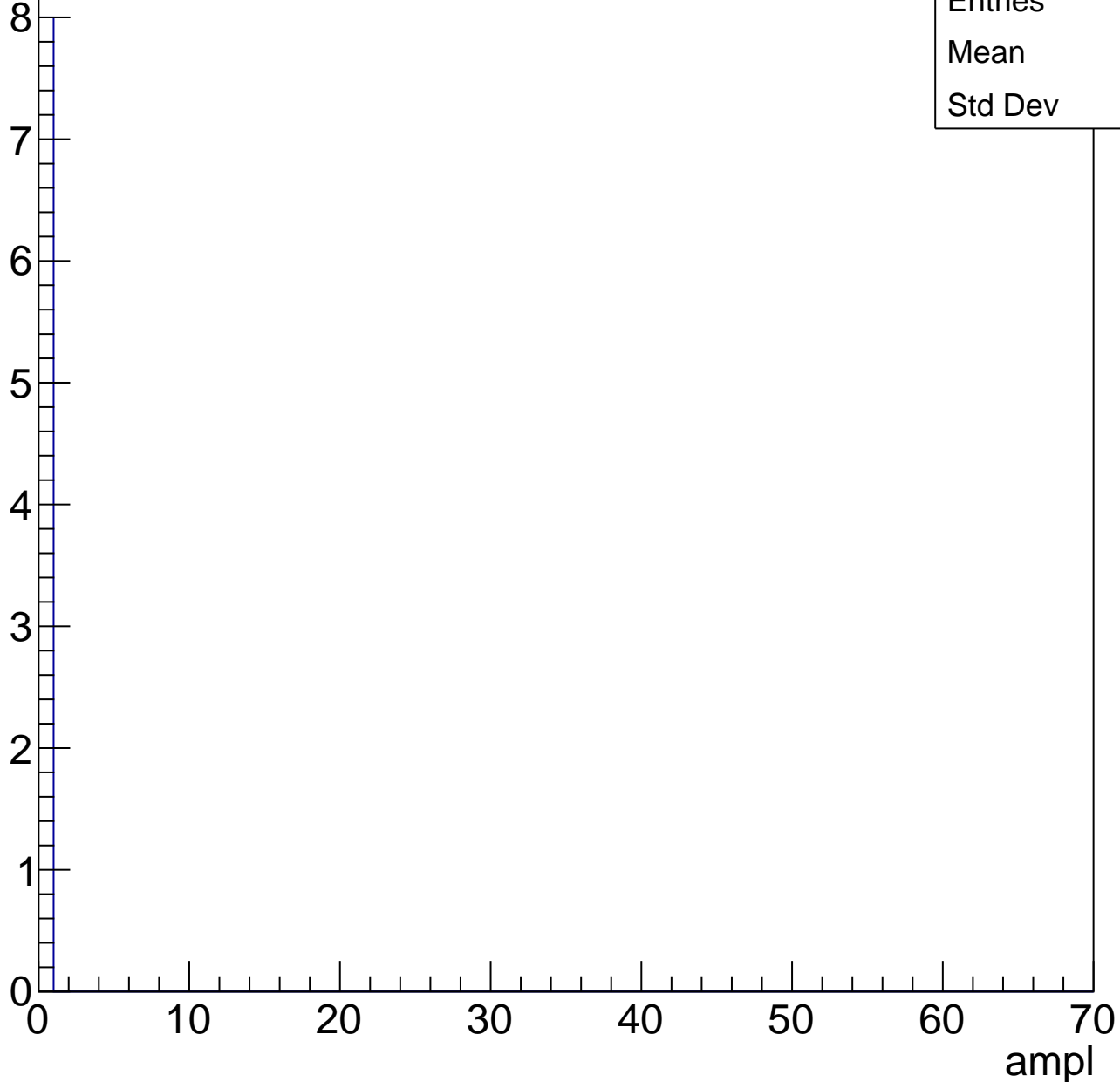
ampl



B1L103S, U14-ch75, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	8
Mean	0
Std Dev	0

B1L103S, U14-ch76, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	51
Mean	21.57
Std Dev	11.82

Entry

10

8

6

4

2

0

0

10

20

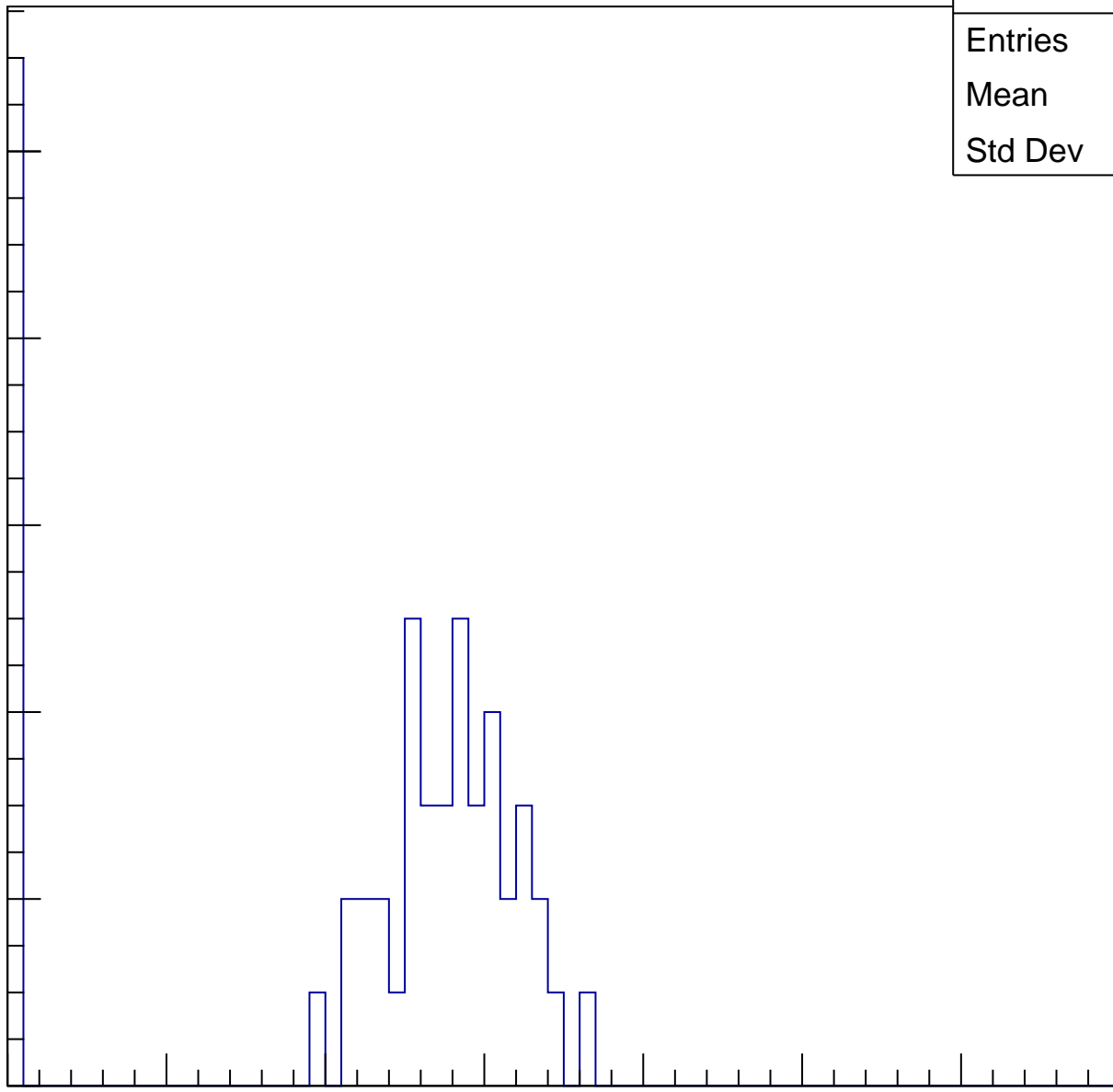
30

40

50

60

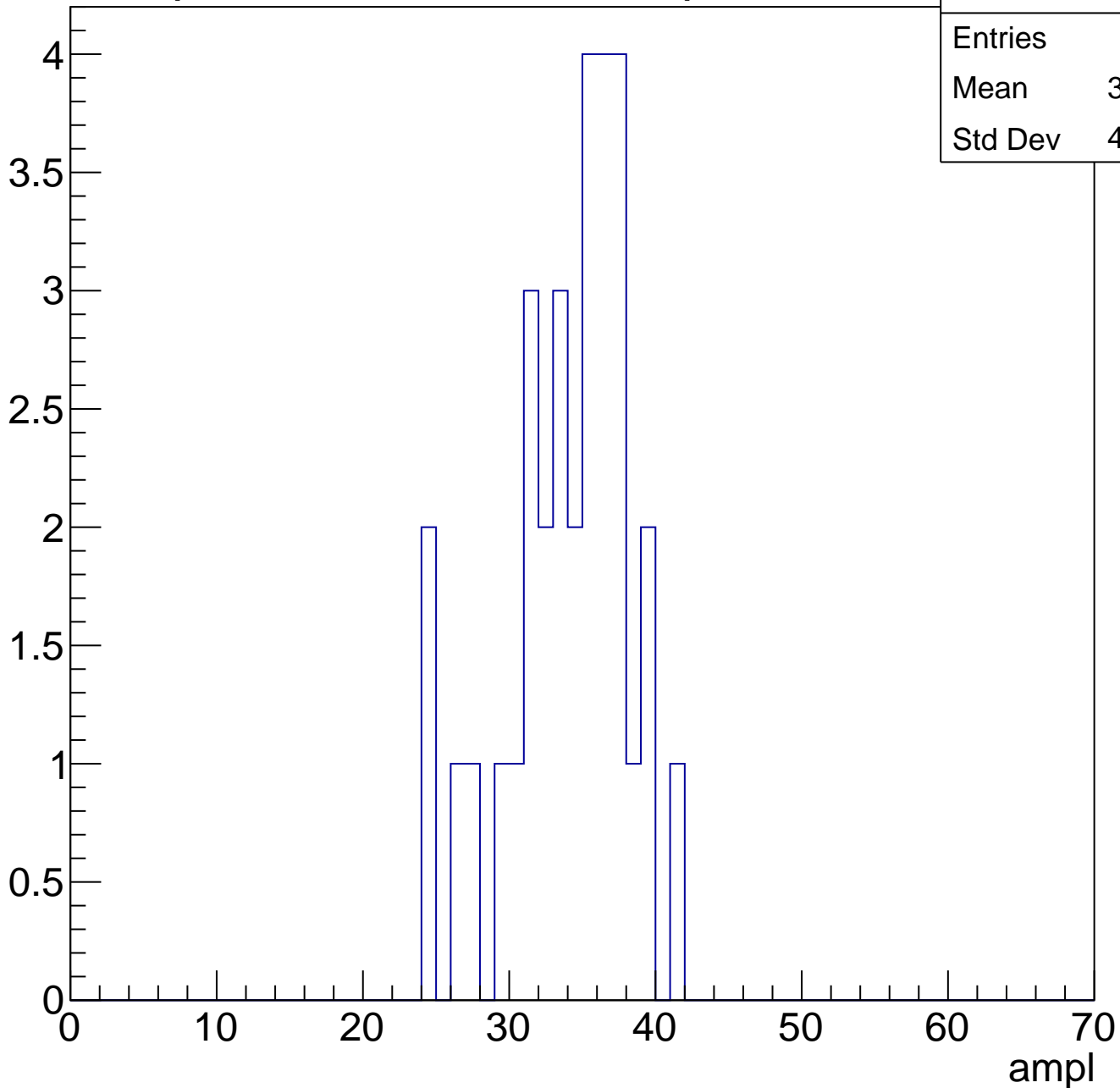
ampl



B1L103S, U14-ch76, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry



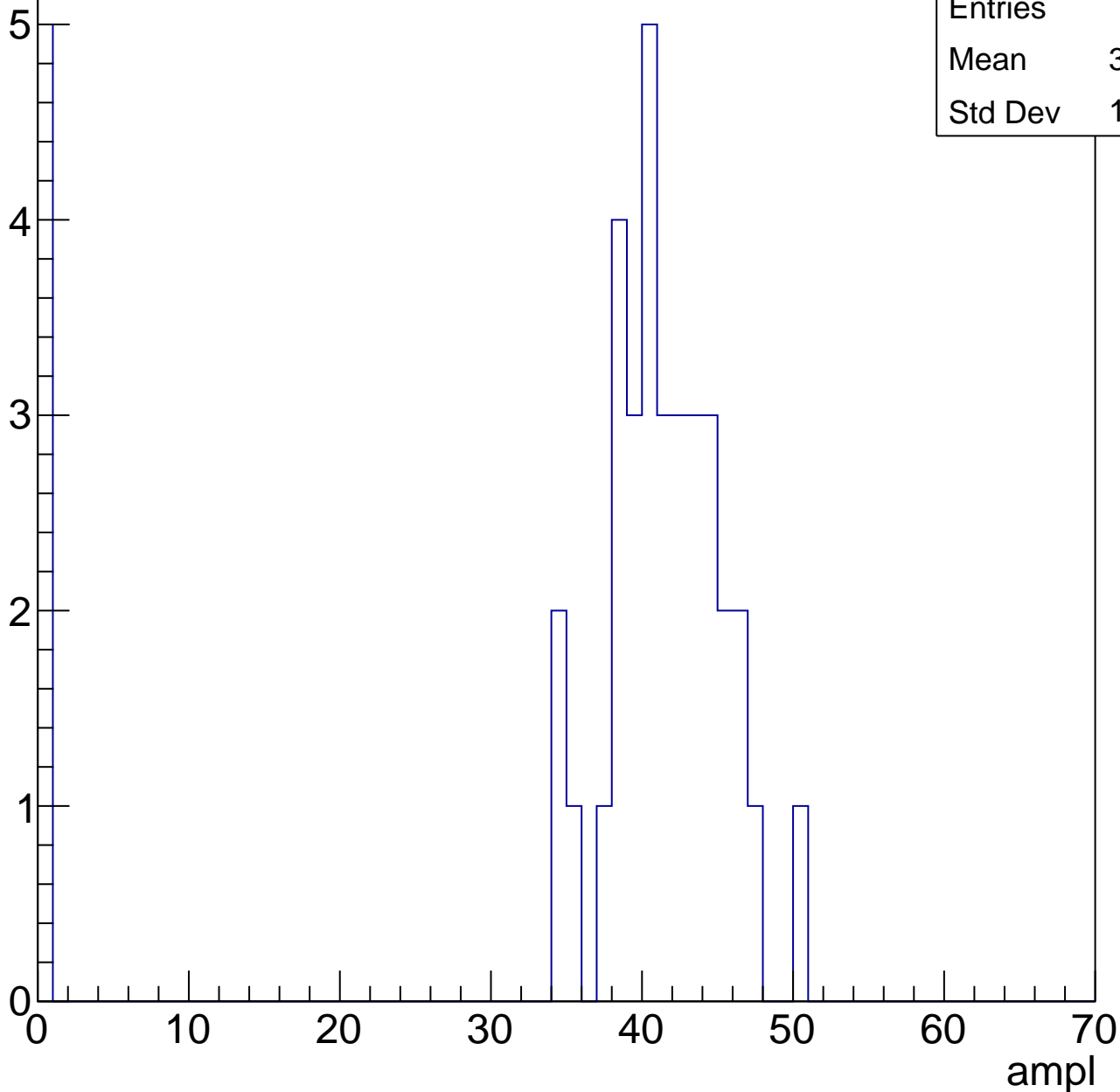
Entries	32
Mean	33.53
Std Dev	4.168

B1L103S, U14-ch76, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

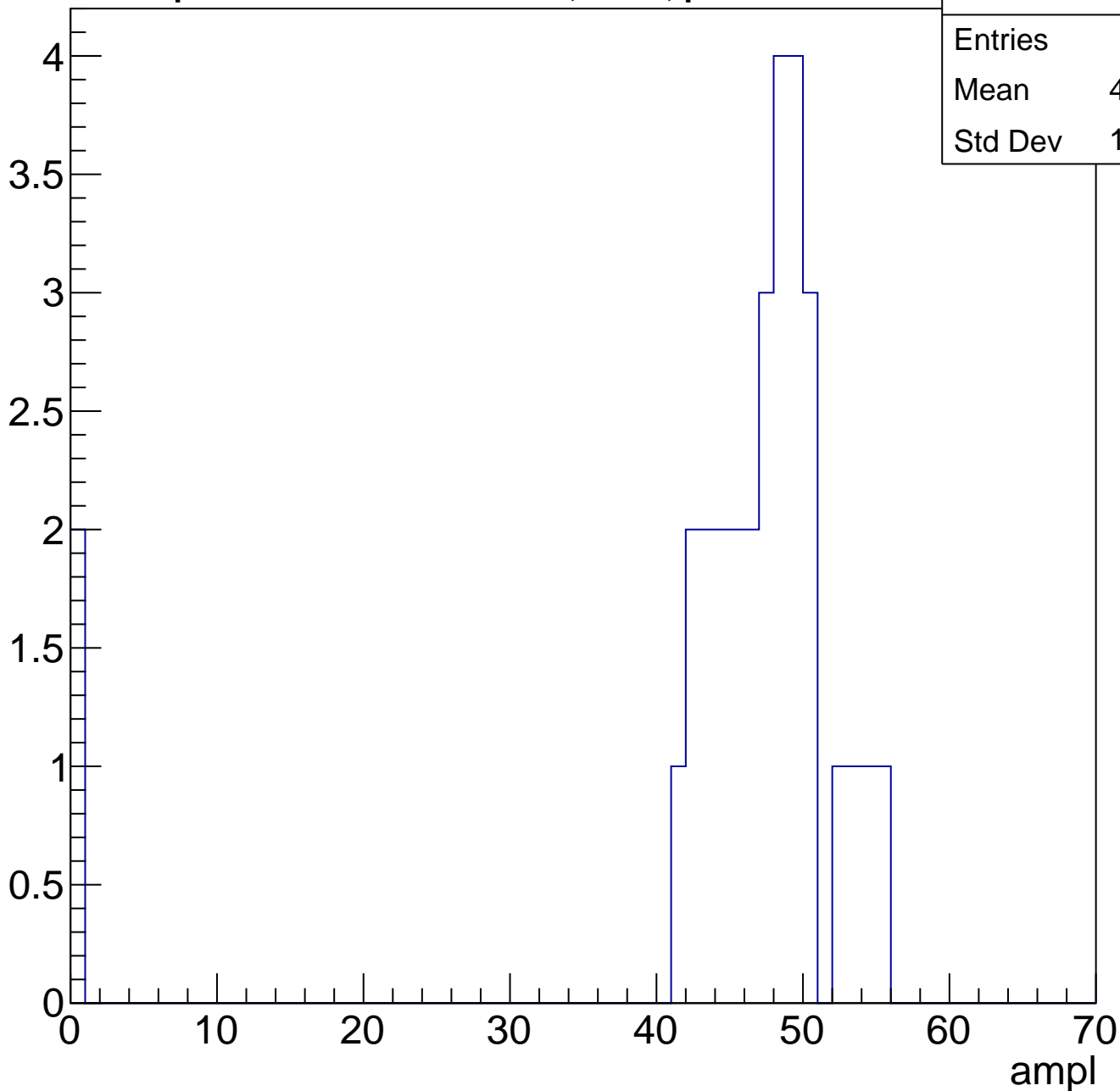
Entries	39
Mean	35.85
Std Dev	14.15



B1L103S, U14-ch76, adc3

calib_packv5_041523_1651.root, FC#0, port C2

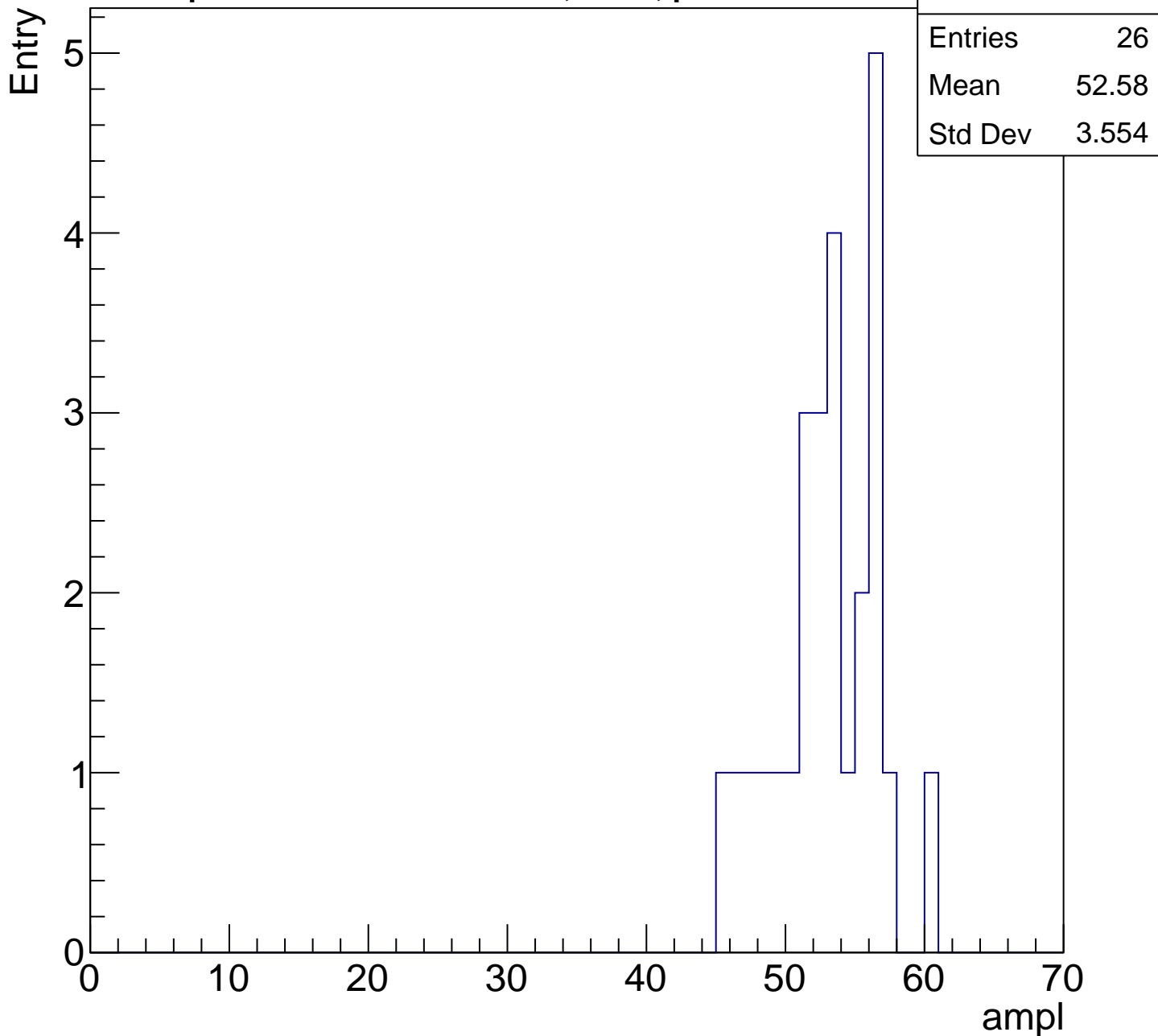
Entry



Entries	31
Mean	44.32
Std Dev	12.13

B1L103S, U14-ch76, adc4

calib_packv5_041523_1651.root, FC#0, port C2

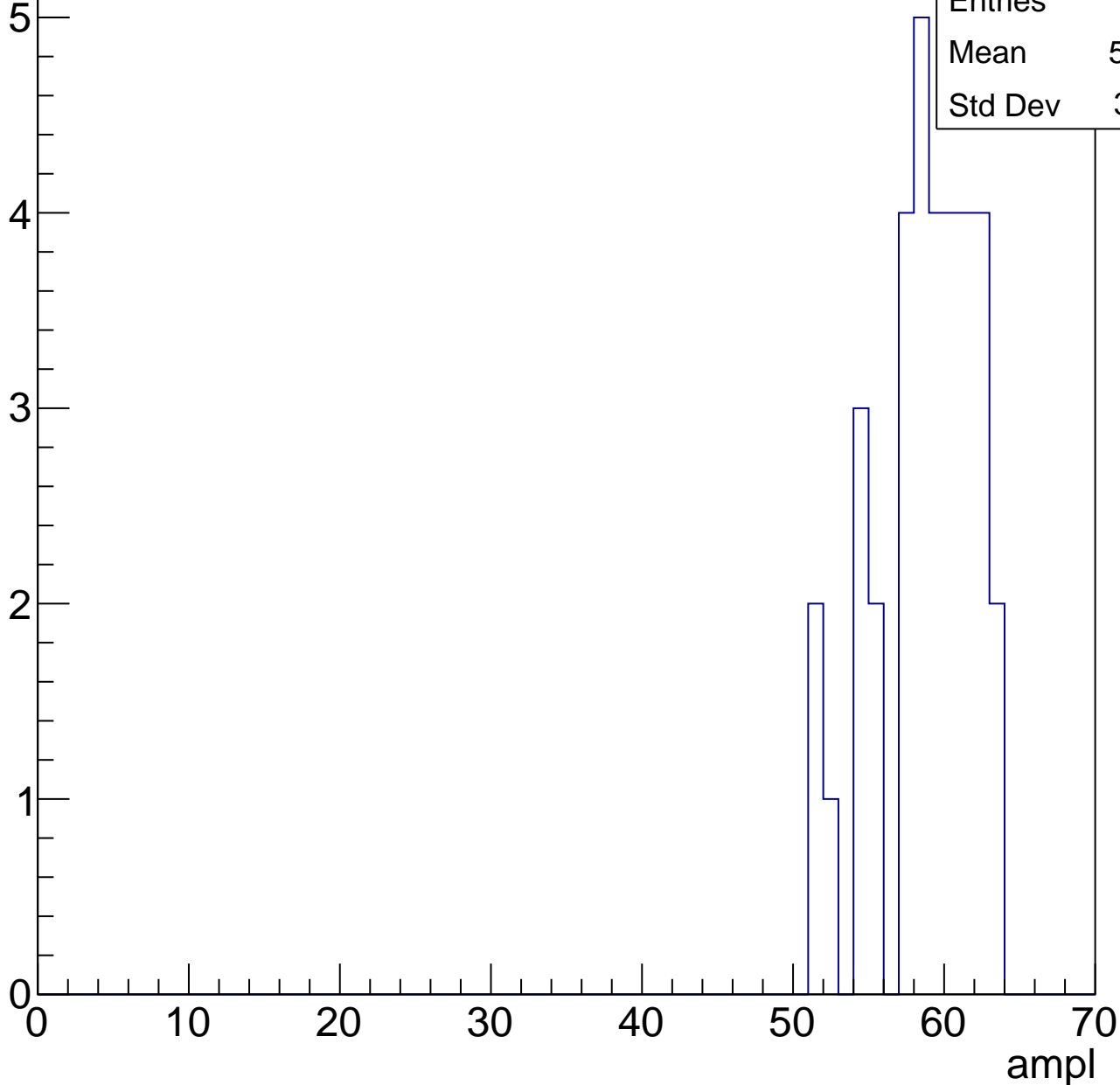


B1L103S, U14-ch76, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

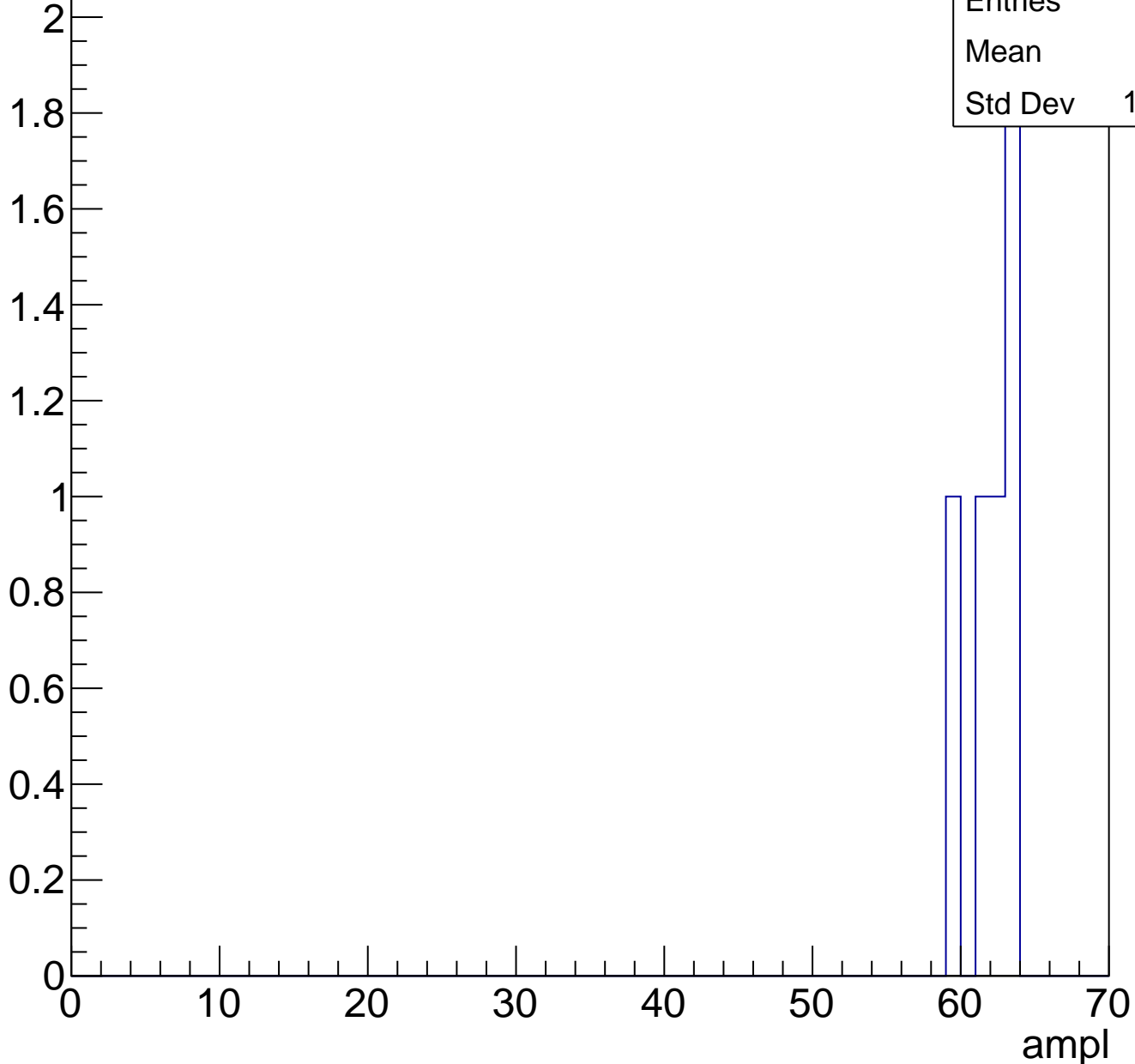
Entries	35
Mean	58.23
Std Dev	3.261



B1L103S, U14-ch76, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

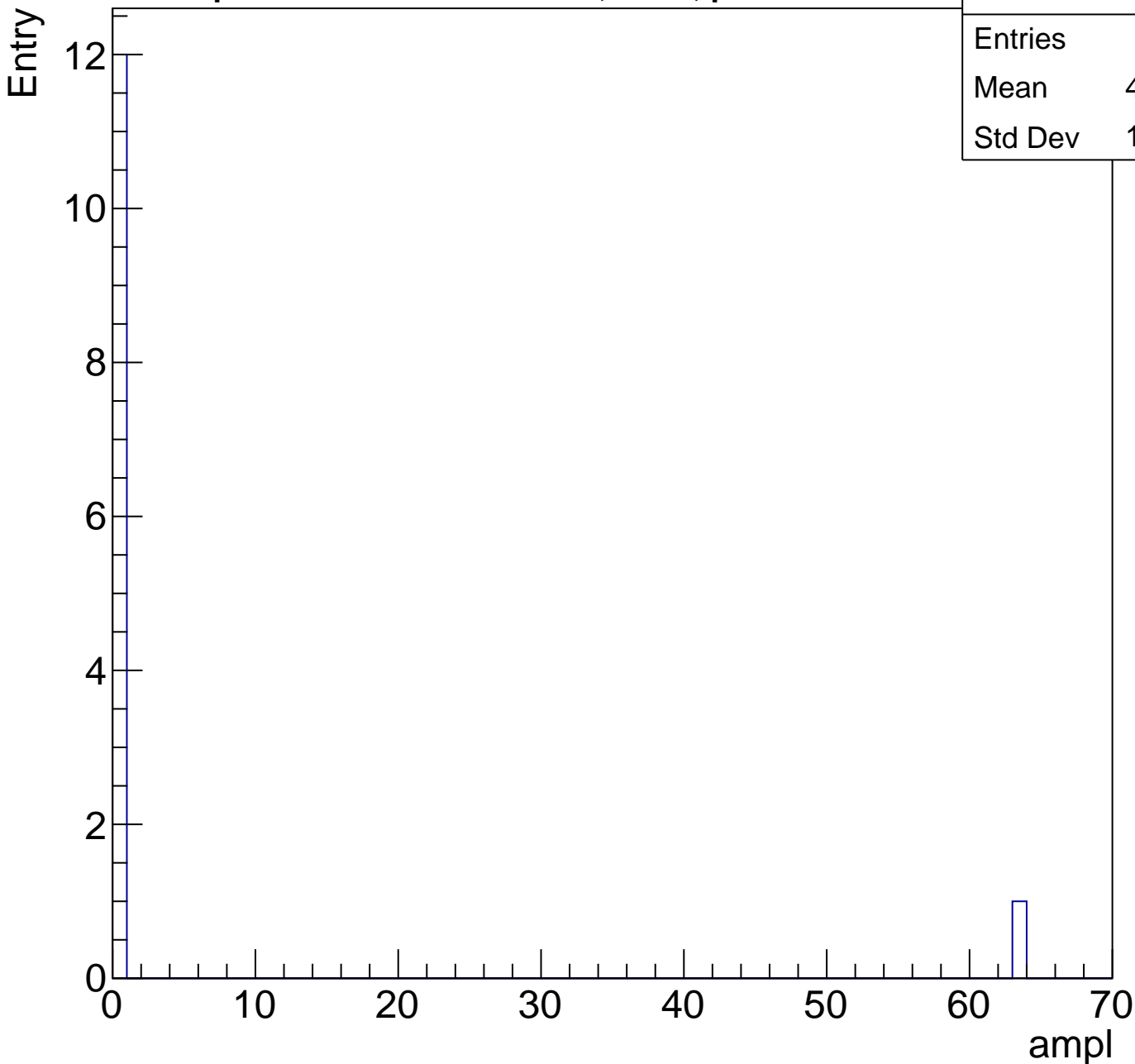


Entries	5
Mean	61.6
Std Dev	1.497

B1L103S, U14-ch76, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	13
Mean	4.846
Std Dev	16.79

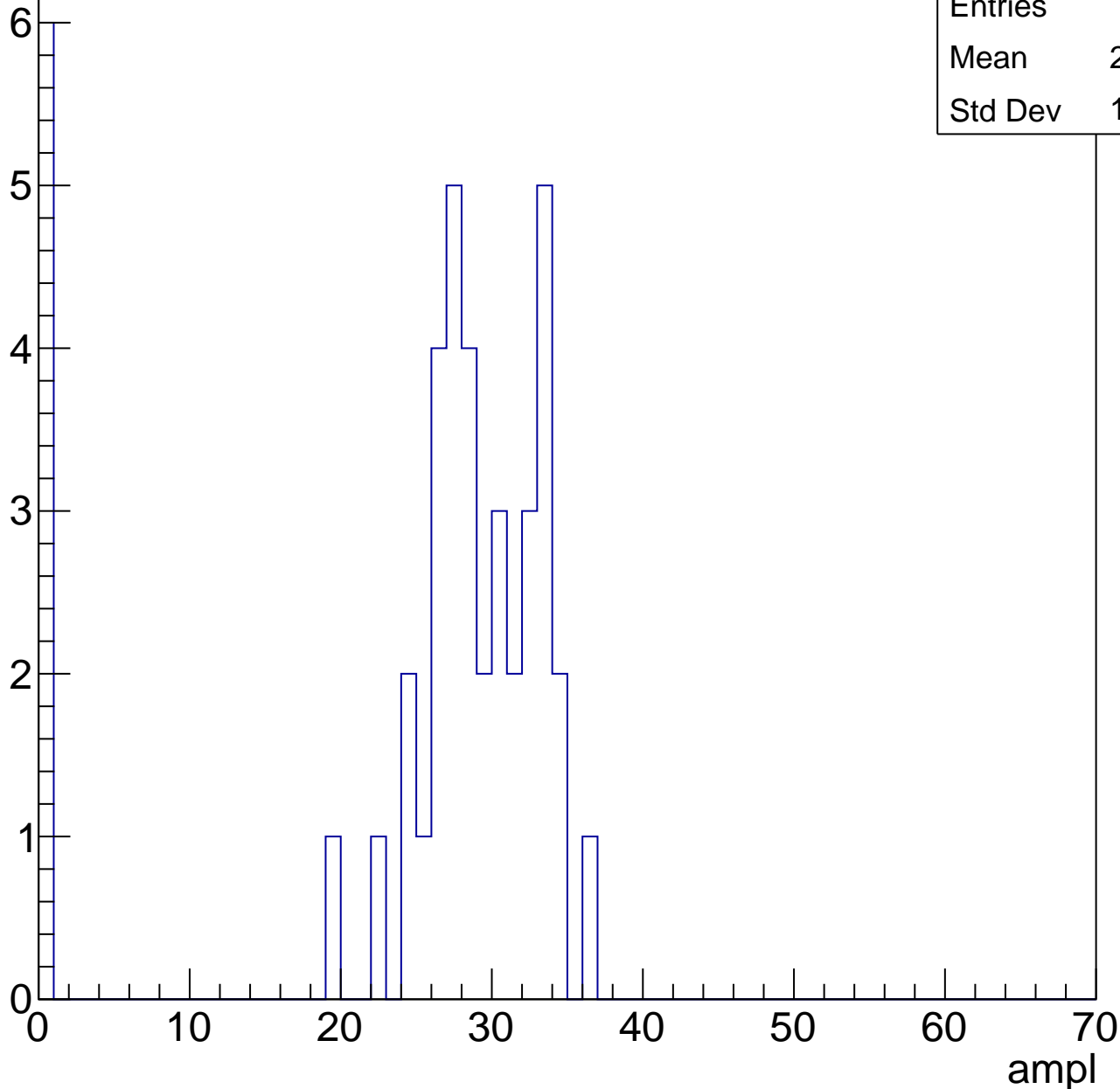


B1L103S, U14-ch77, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	42
Mean	24.76
Std Dev	10.67

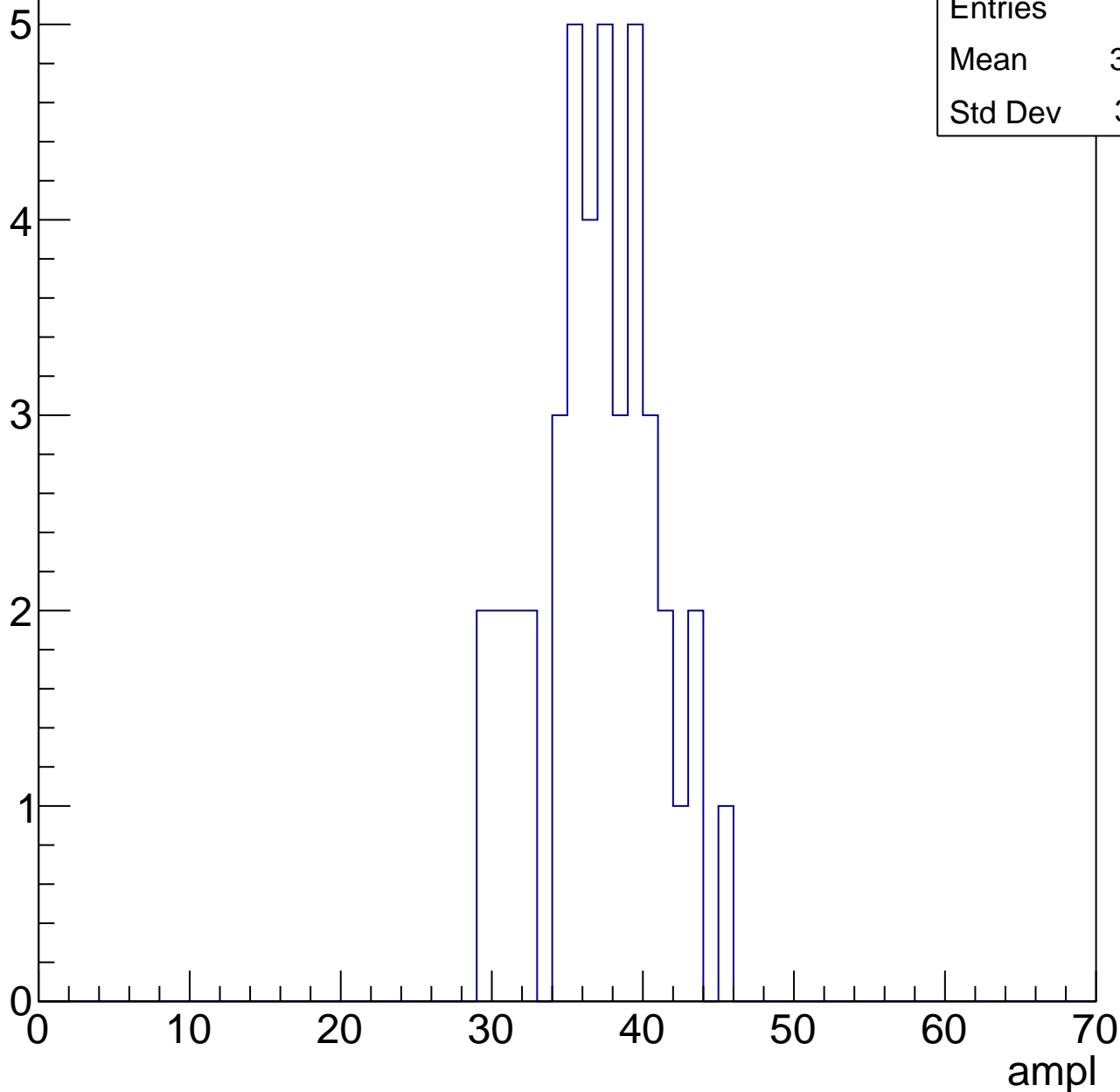


B1L103S, U14-ch77, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

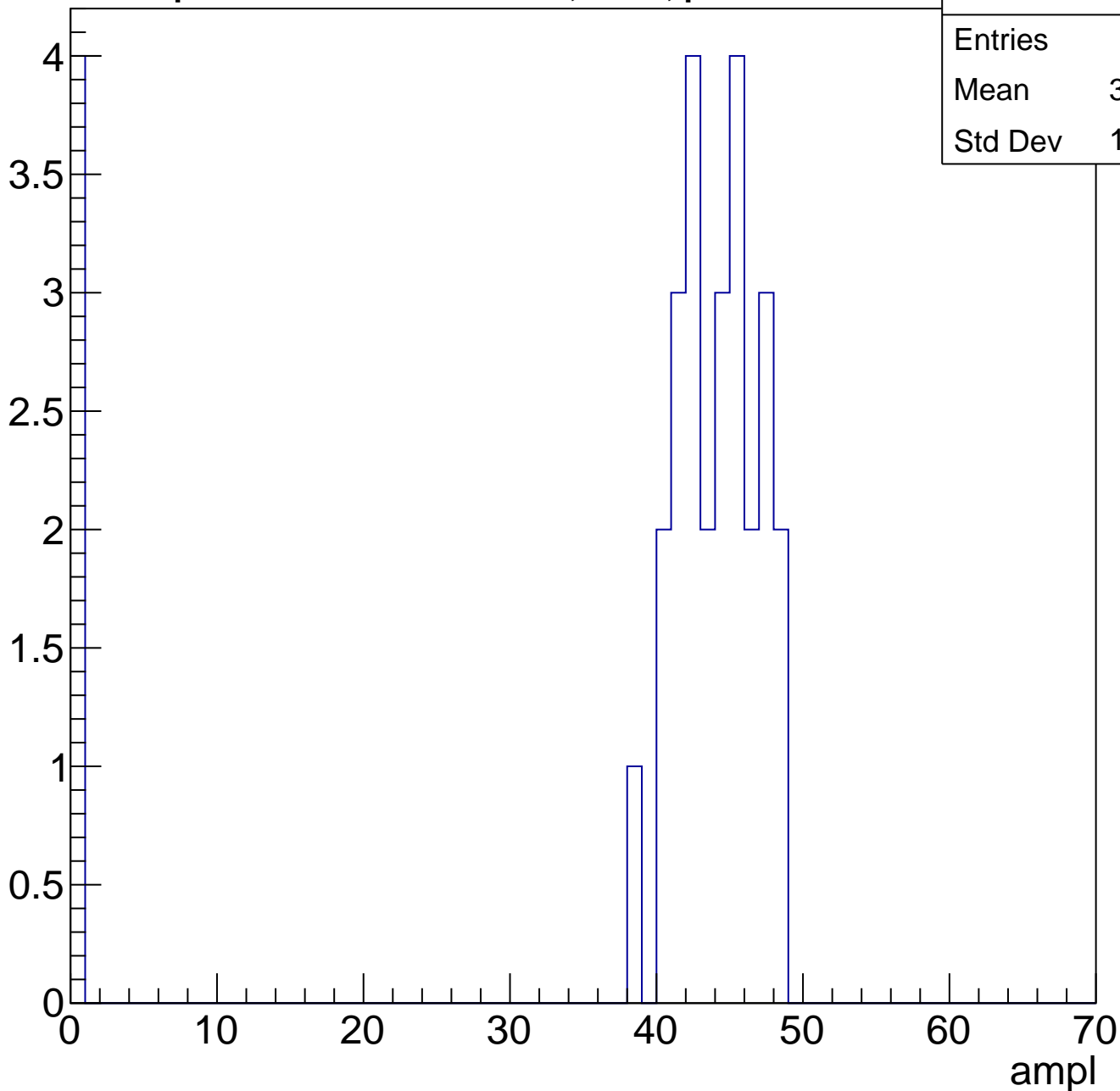
Entries	42
Mean	36.52
Std Dev	3.881



B1L103S, U14-ch77, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

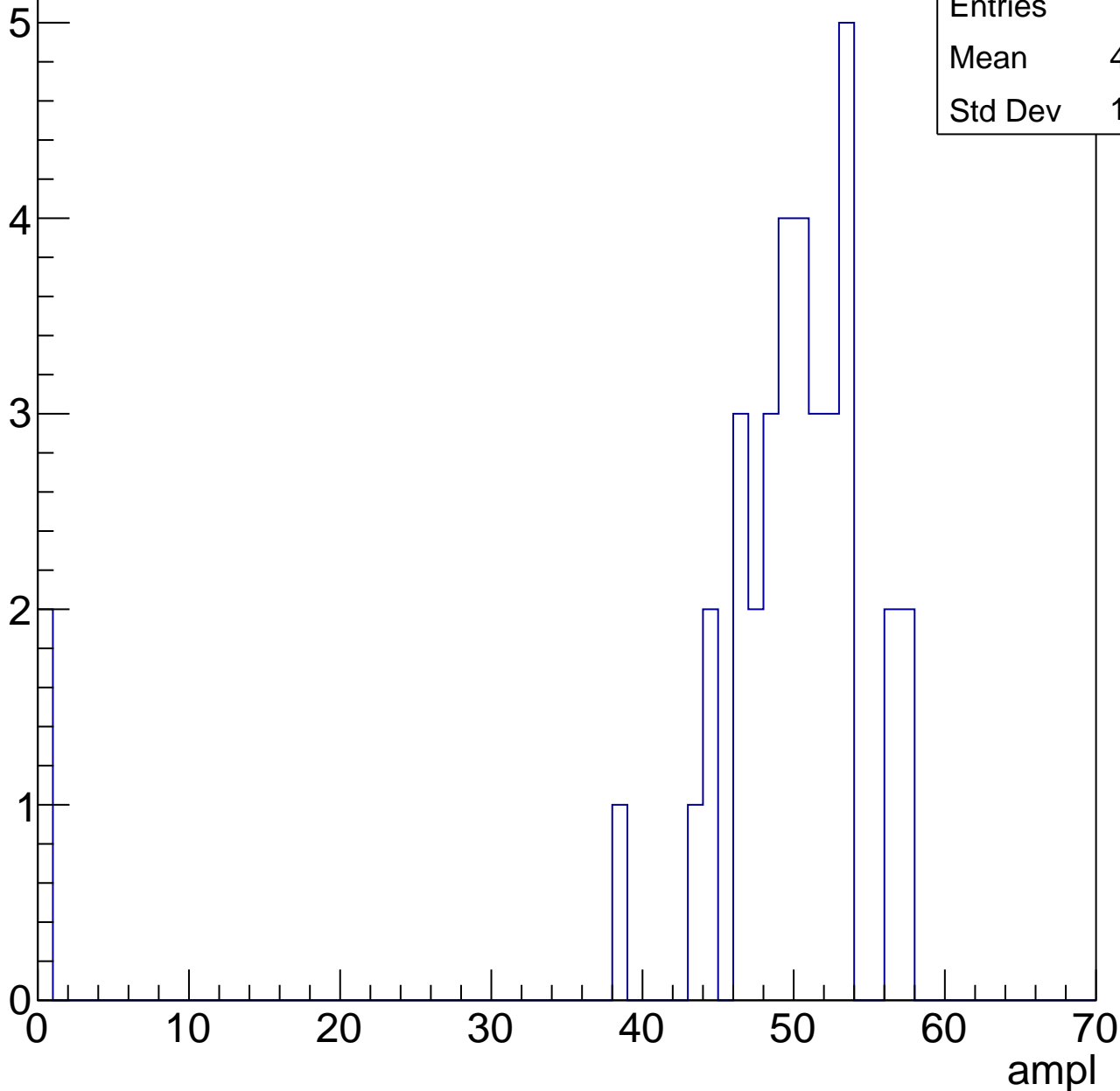


B1L103S, U14-ch77, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	37
Mean	47.05
Std Dev	11.92

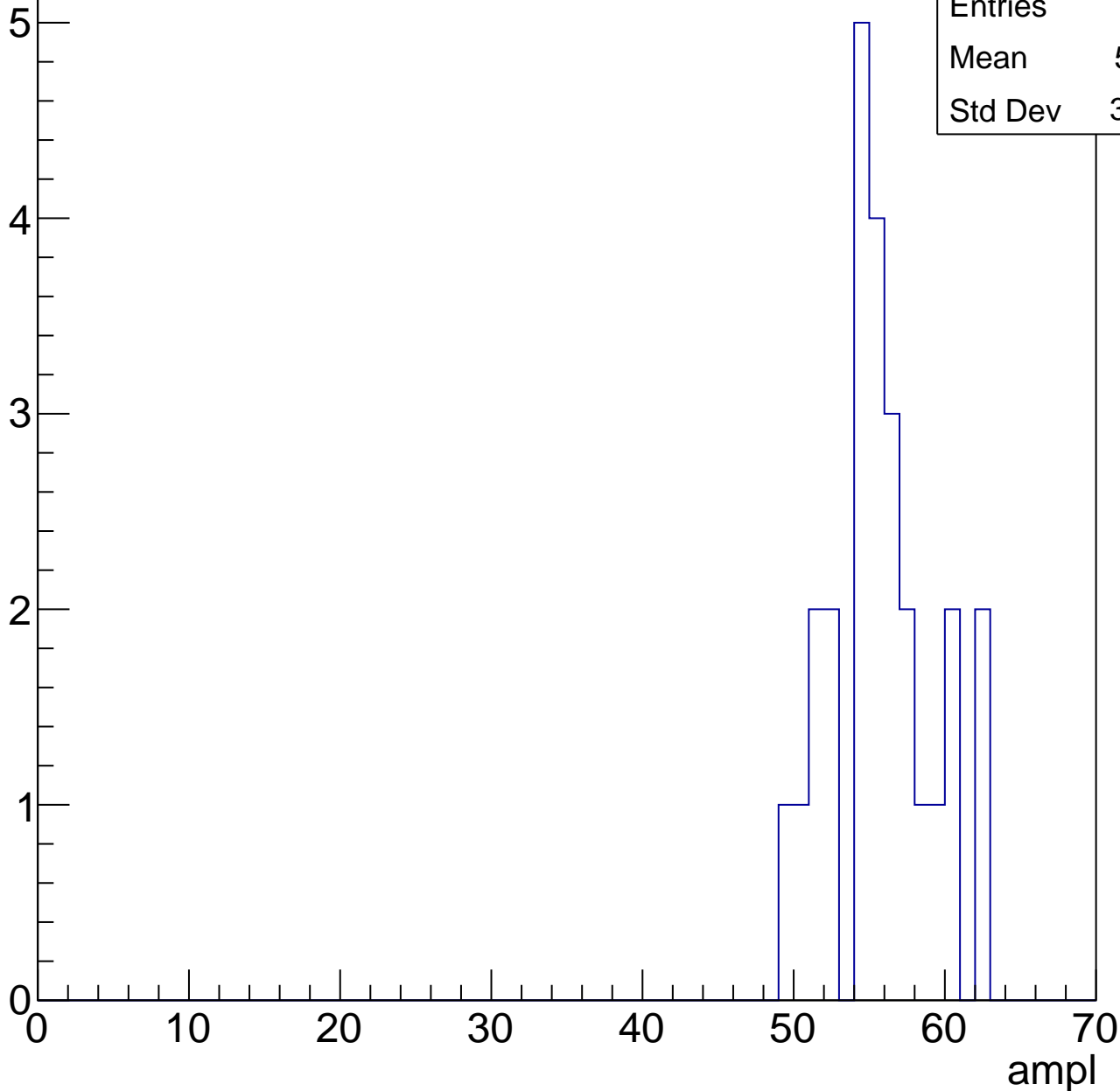


B1L103S, U14-ch77, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	26
Mean	55.31
Std Dev	3.383

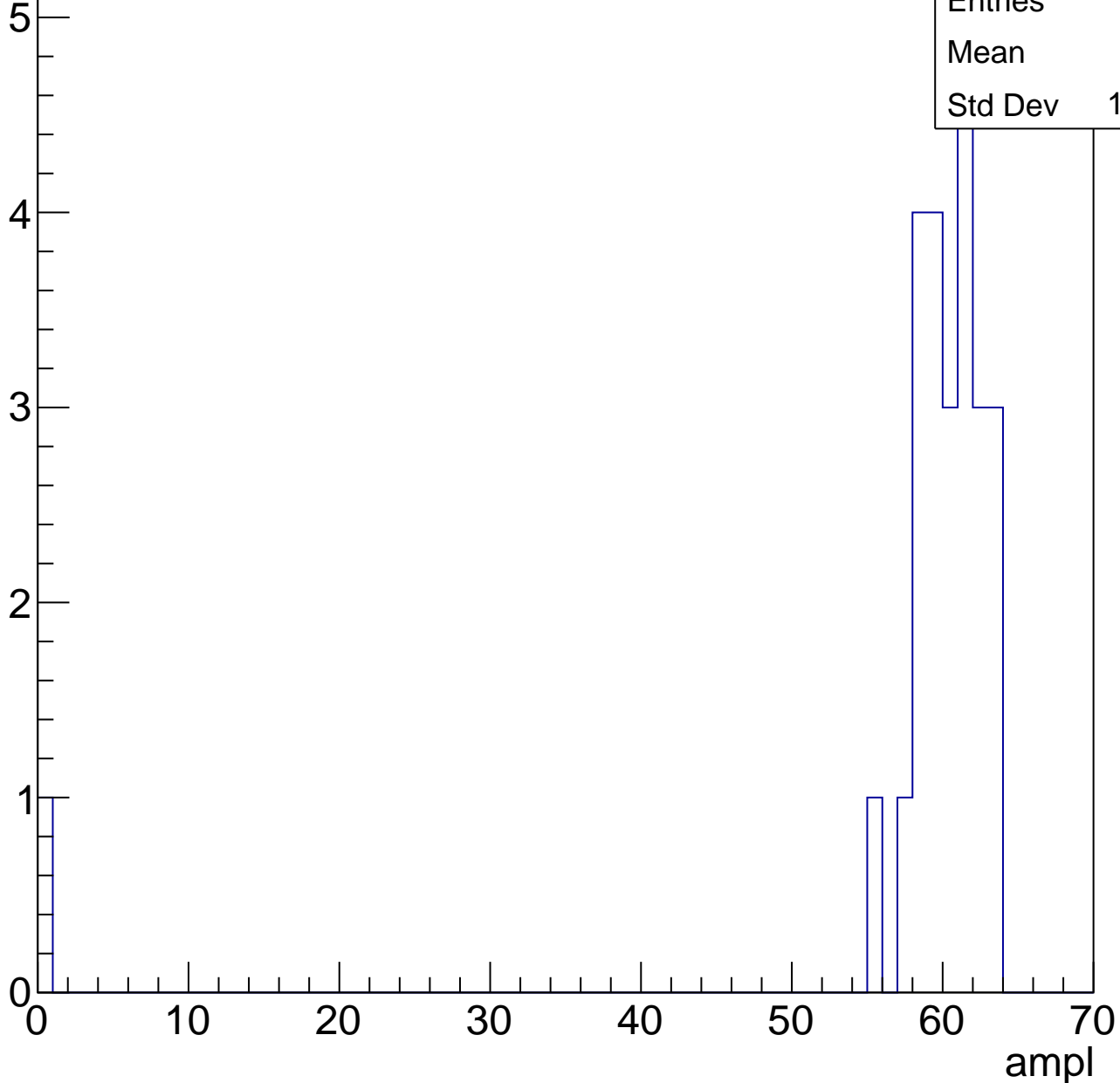


B1L103S, U14-ch77, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	25
Mean	57.6
Std Dev	11.92



B1L103S, U14-ch77, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

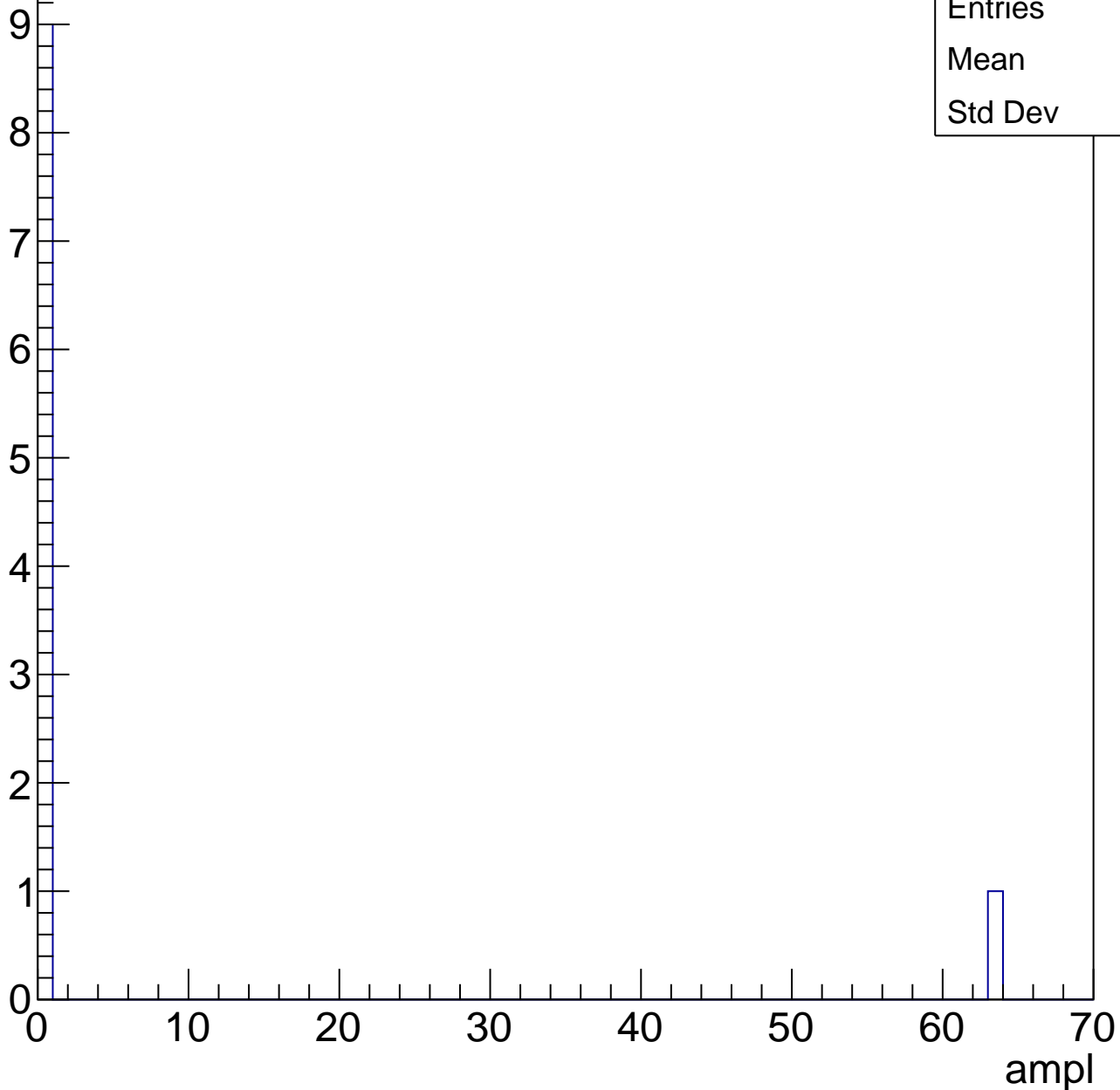


B1L103S, U14-ch77, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	10
Mean	6.3
Std Dev	18.9



B1L103S, U14-ch78, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	46
Mean	20.59
Std Dev	12.08

Entry

10

8

6

4

2

0

0

10

20

30

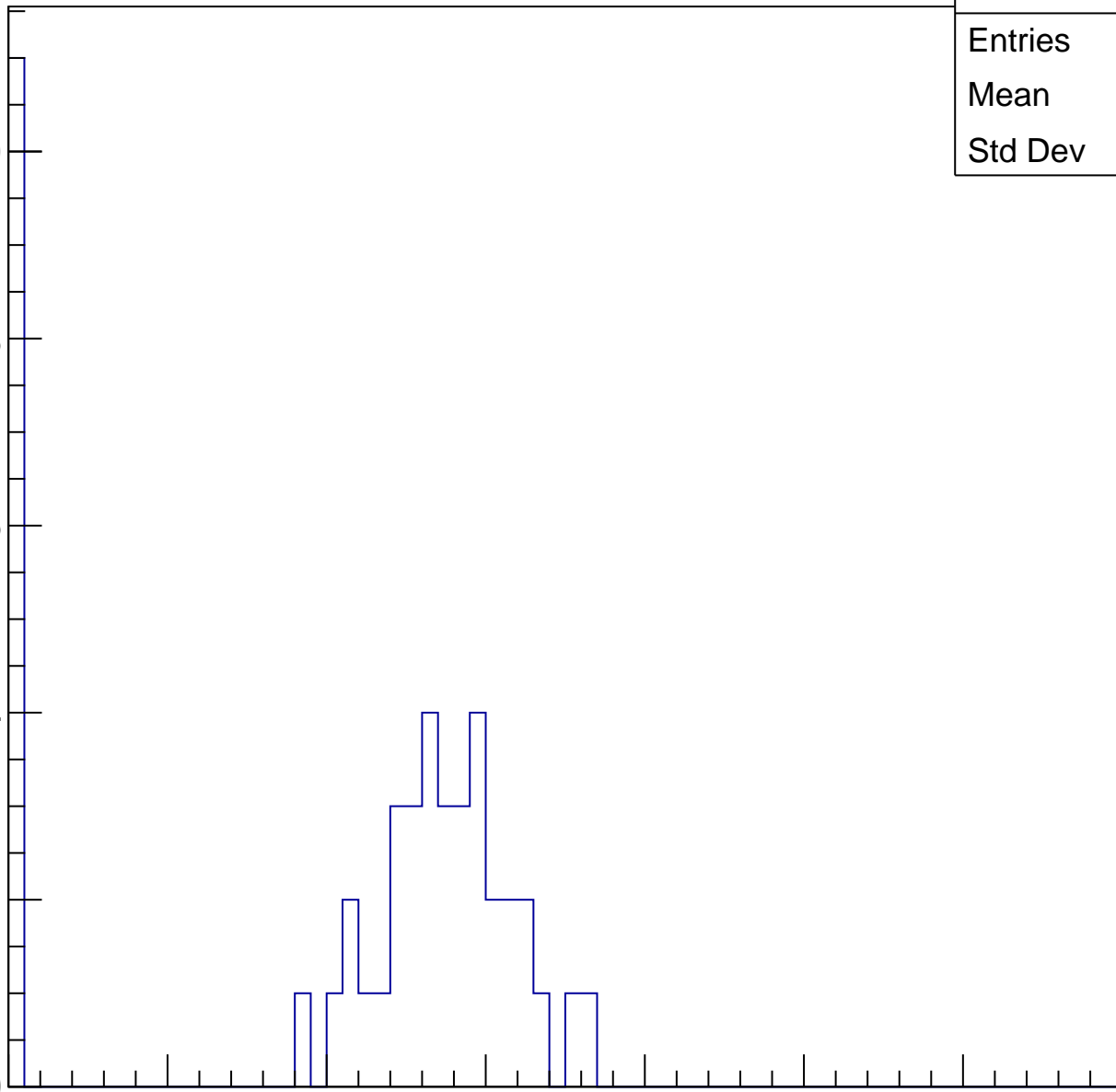
40

50

60

70

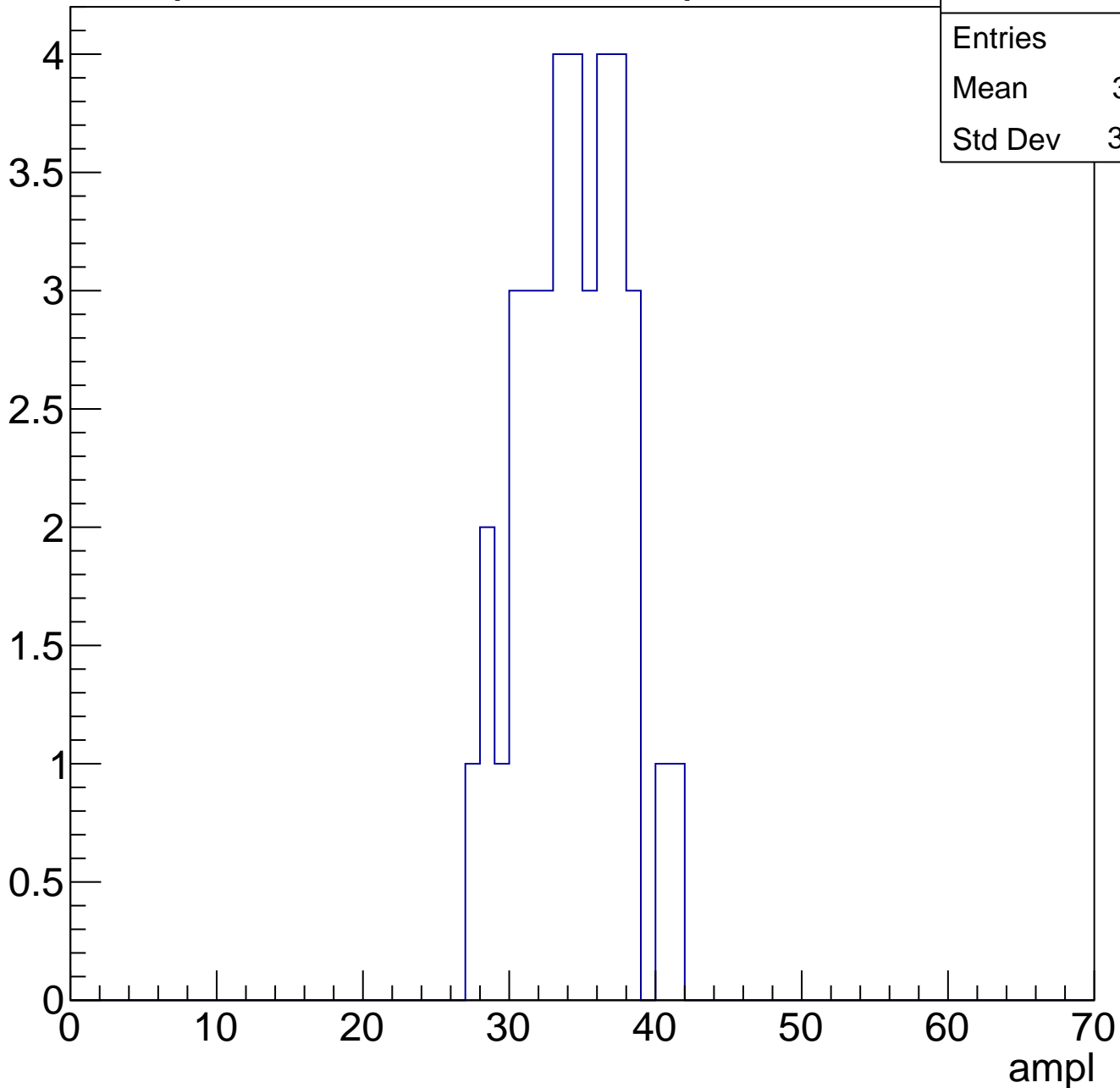
ampl



B1L103S, U14-ch78, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry



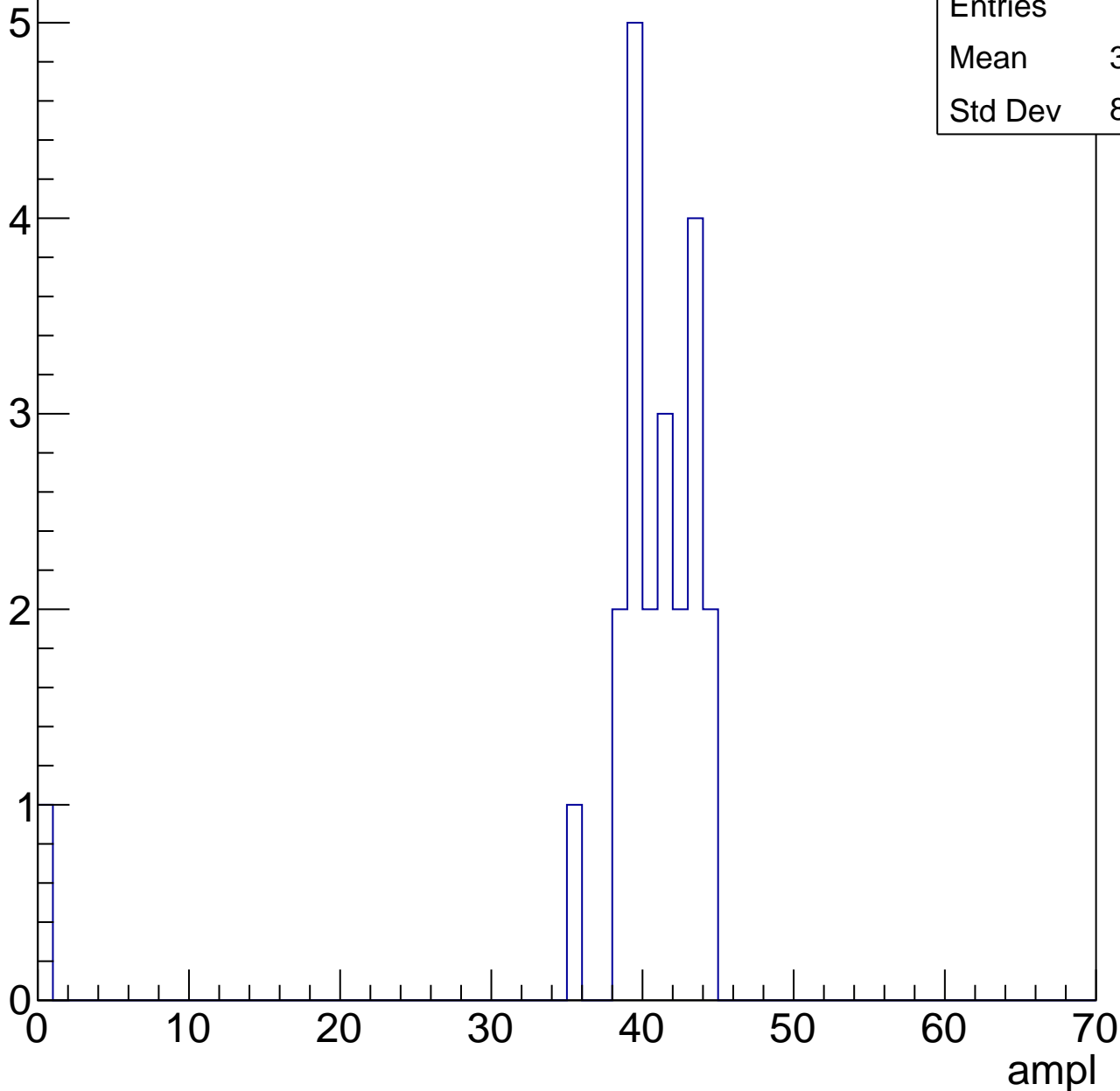
Entries	37
Mean	33.81
Std Dev	3.384

B1L103S, U14-ch78, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	22
Mean	38.77
Std Dev	8.749

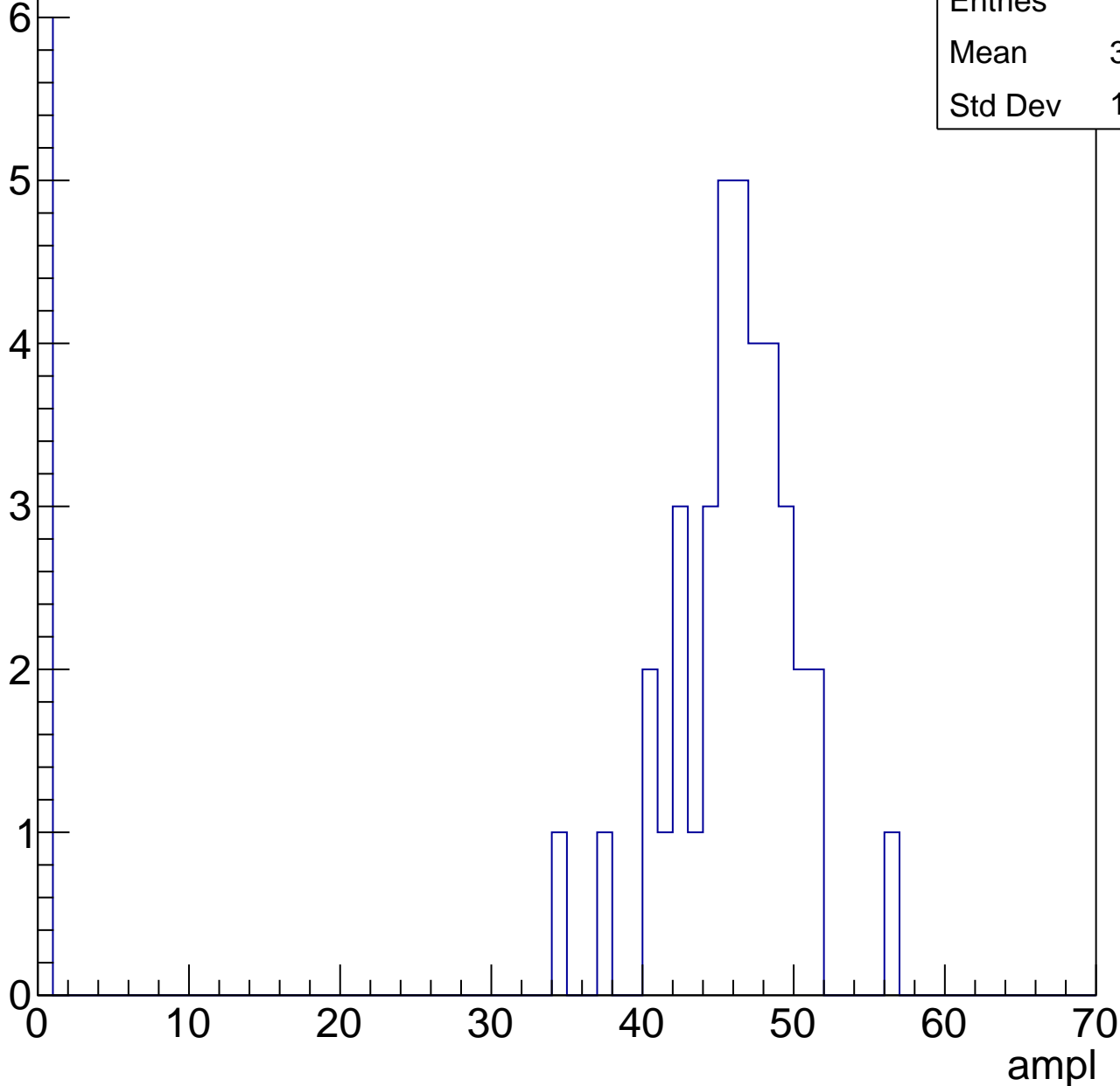


B1L103S, U14-ch78, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

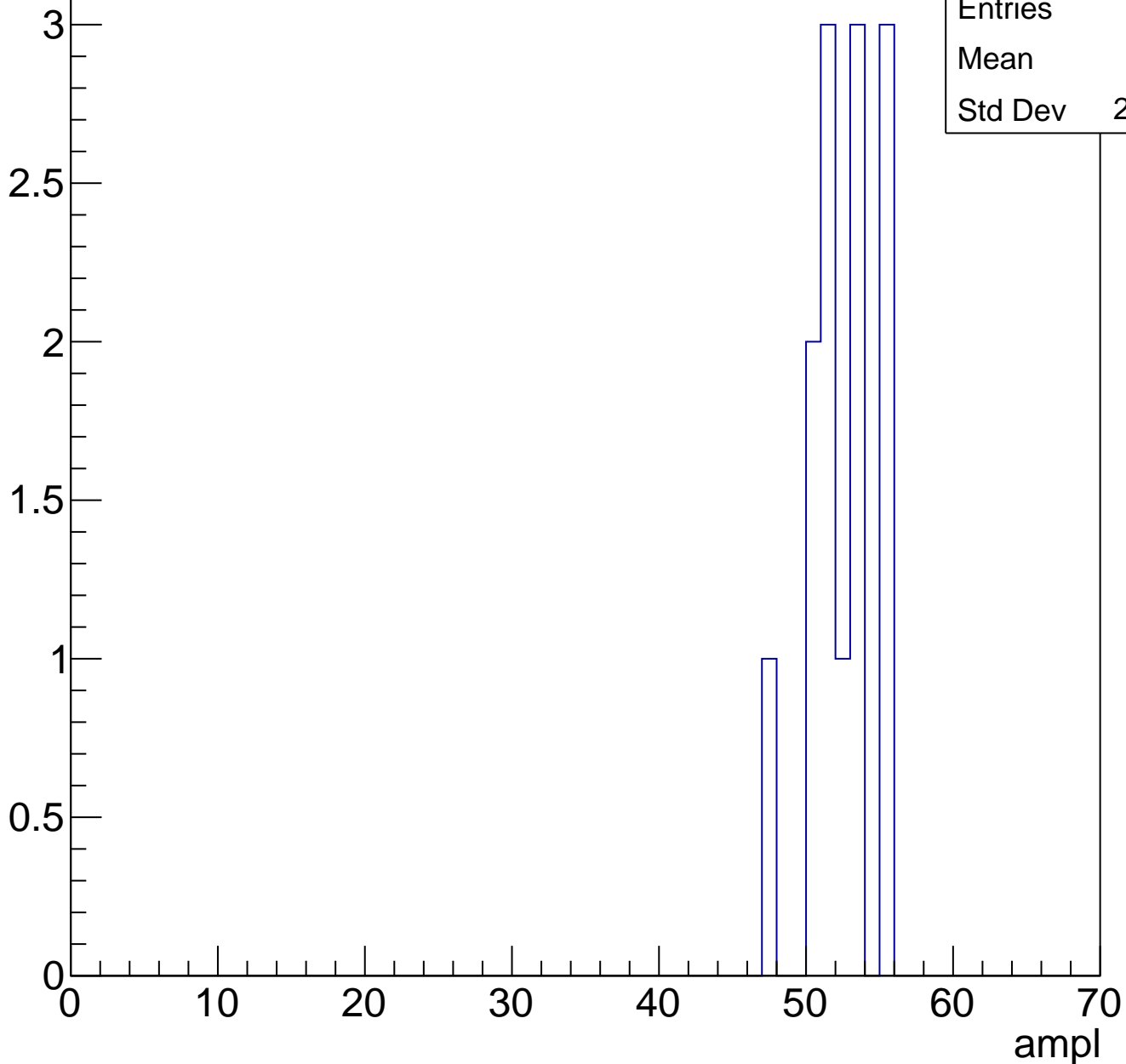
Entries	44
Mean	39.39
Std Dev	16.09



B1L103S, U14-ch78, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

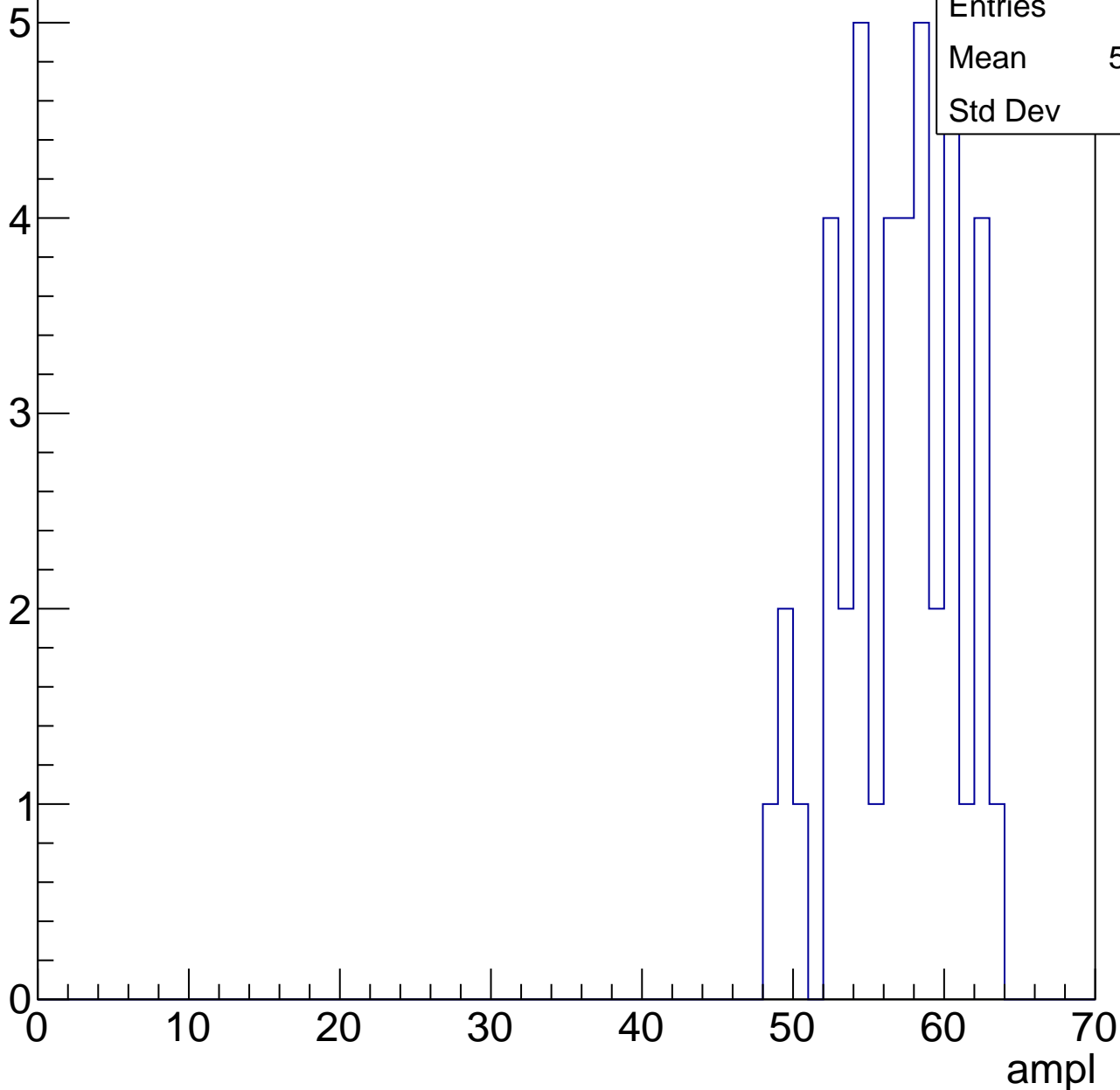


B1L103S, U14-ch78, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

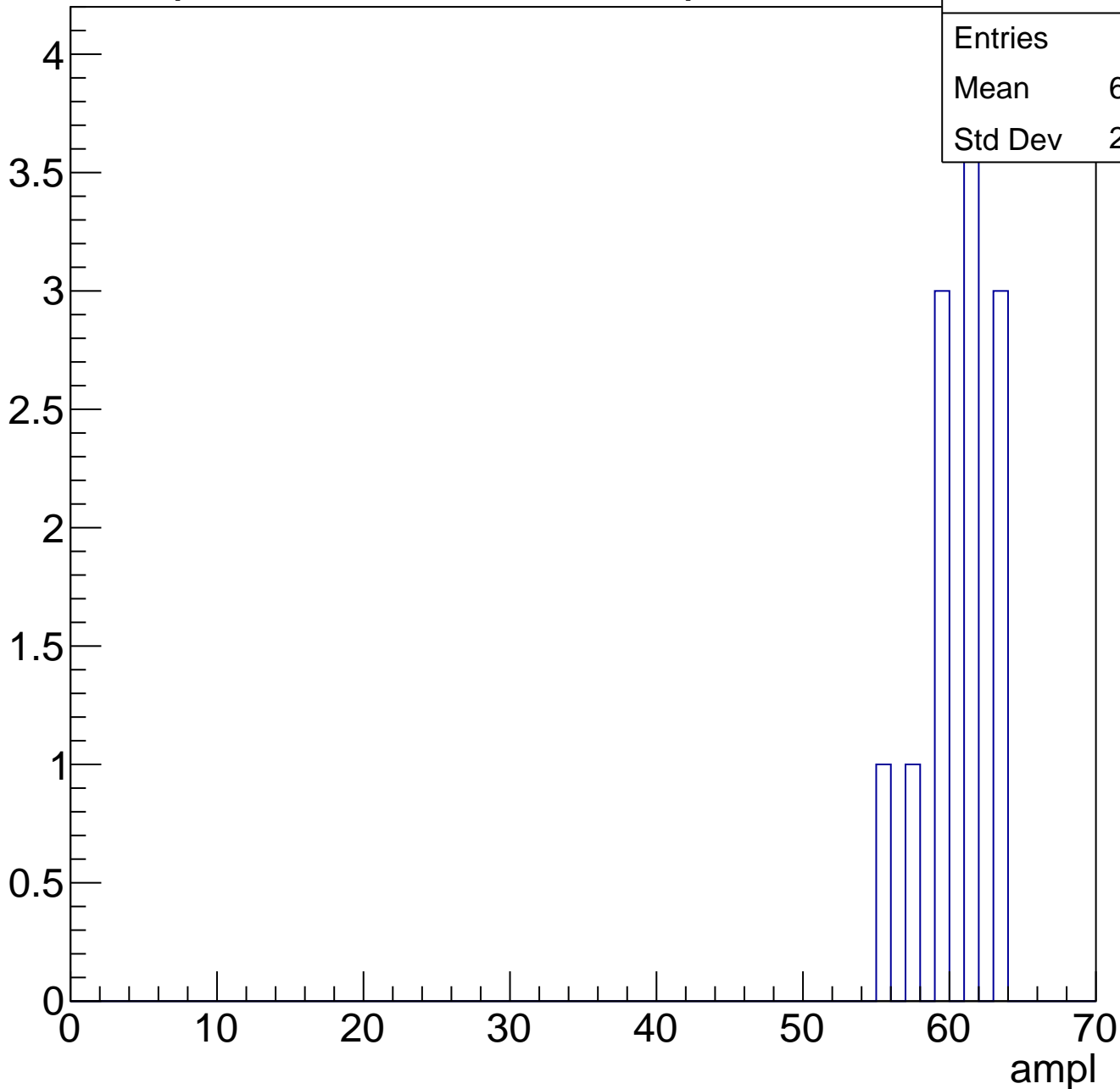
Entries	42
Mean	56.36
Std Dev	3.89



B1L103S, U14-ch78, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch78, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	13
Mean	9.615
Std Dev	22.55

Entry

10

8

6

4

2

0

0

10

20

30

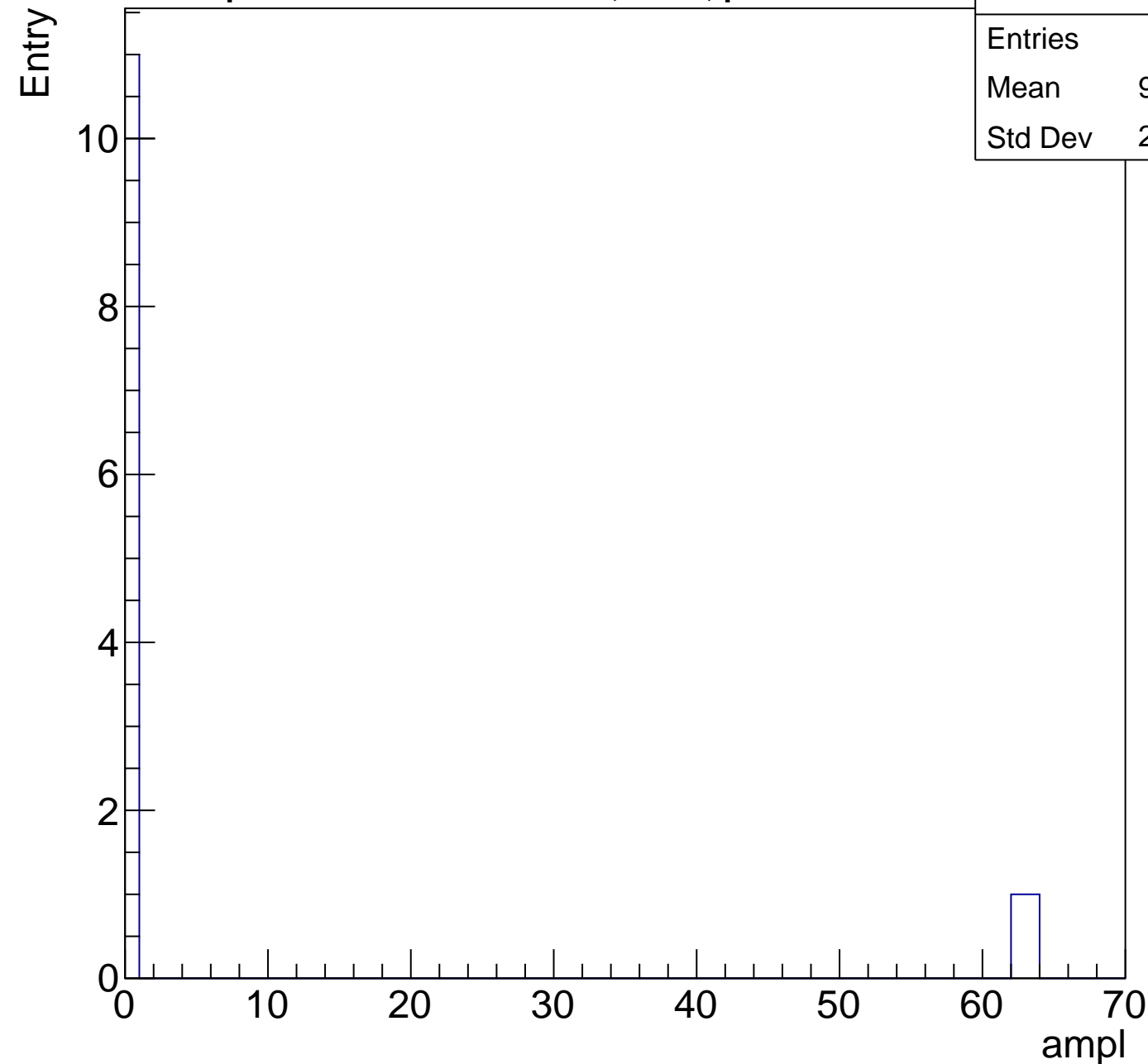
40

50

60

70

ampl

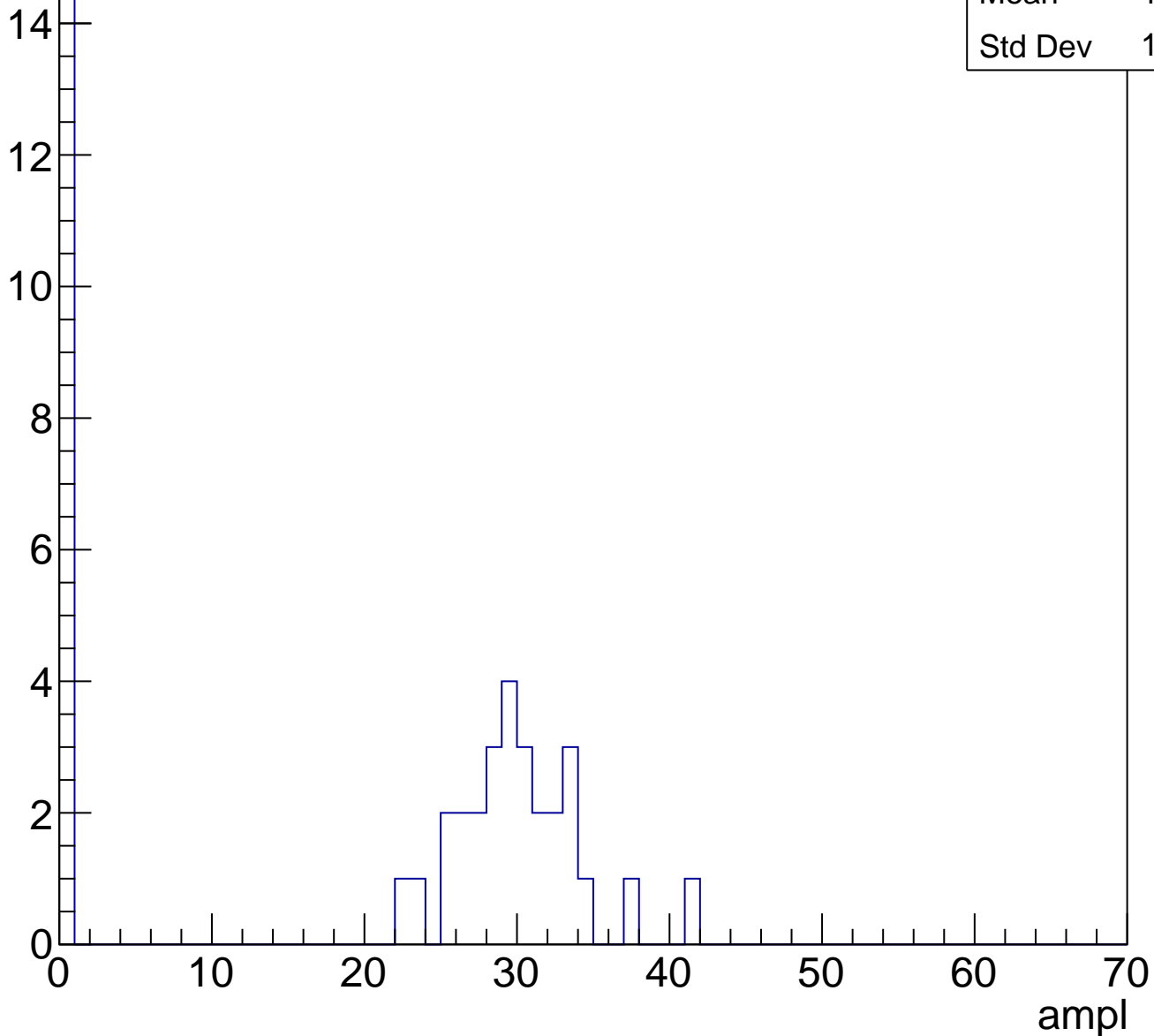


B1L103S, U14-ch79, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	43
Mean	19.26
Std Dev	14.46

Entry

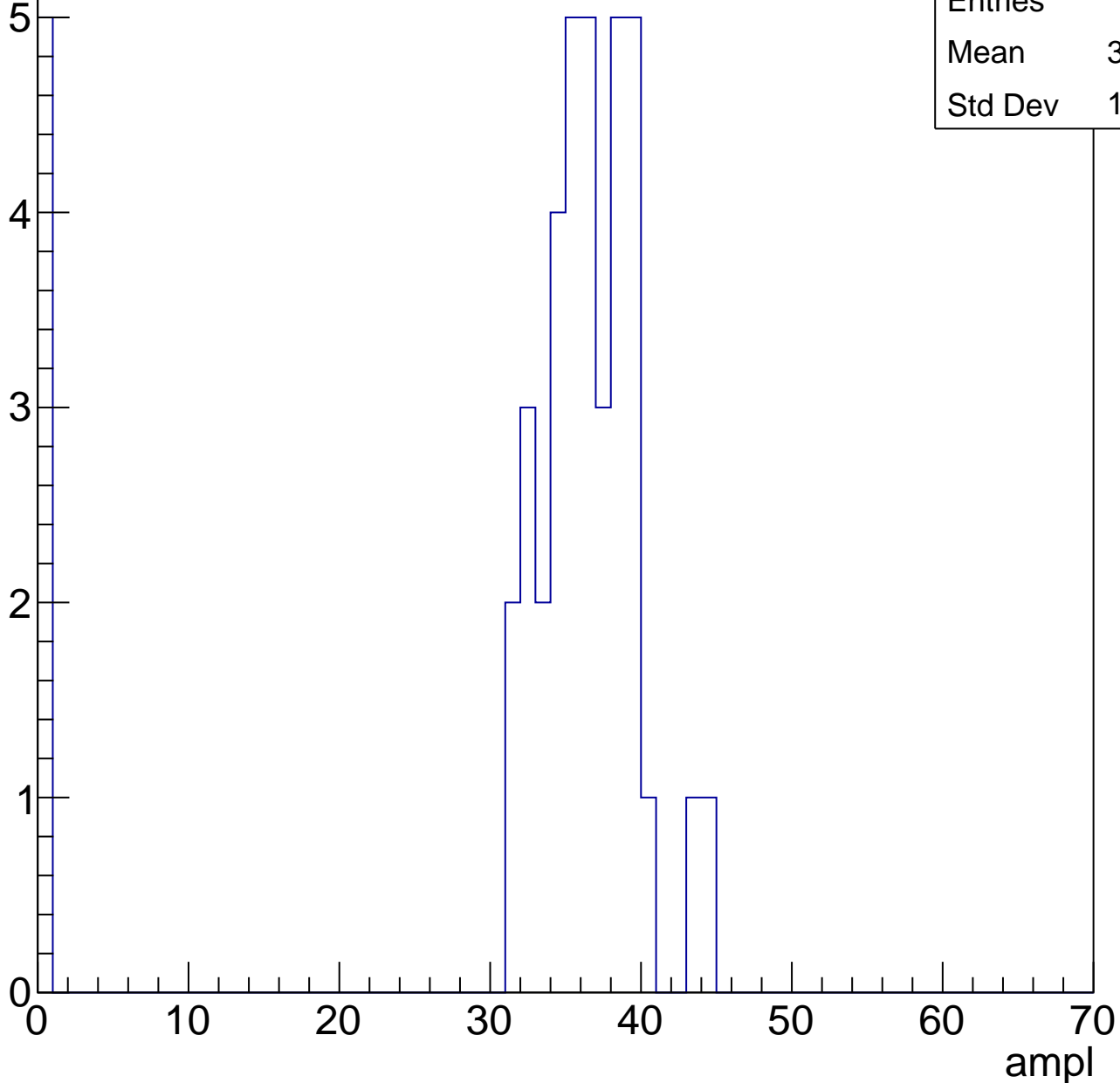


B1L103S, U14-ch79, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	42
Mean	31.86
Std Dev	12.04

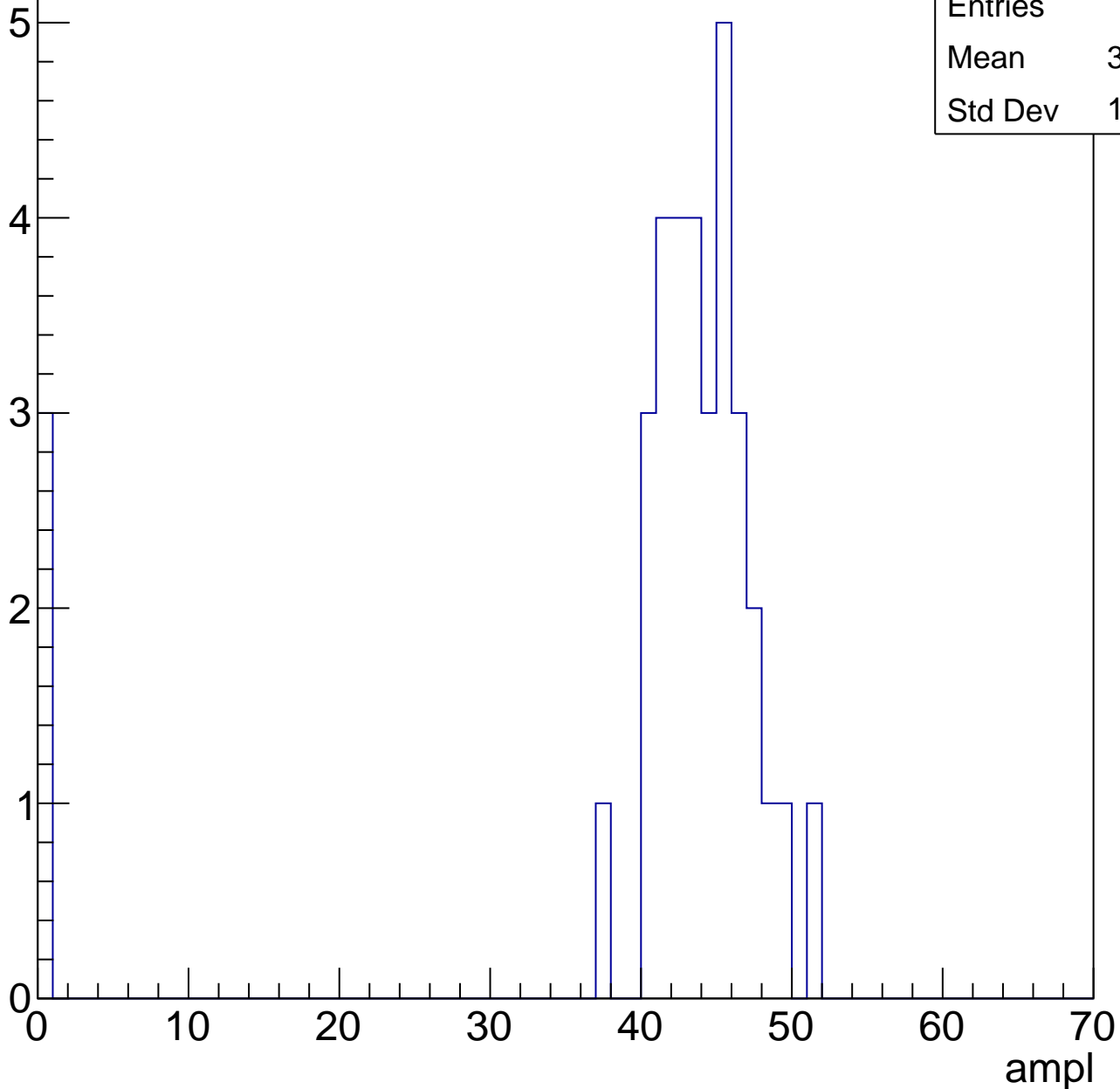


B1L103S, U14-ch79, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

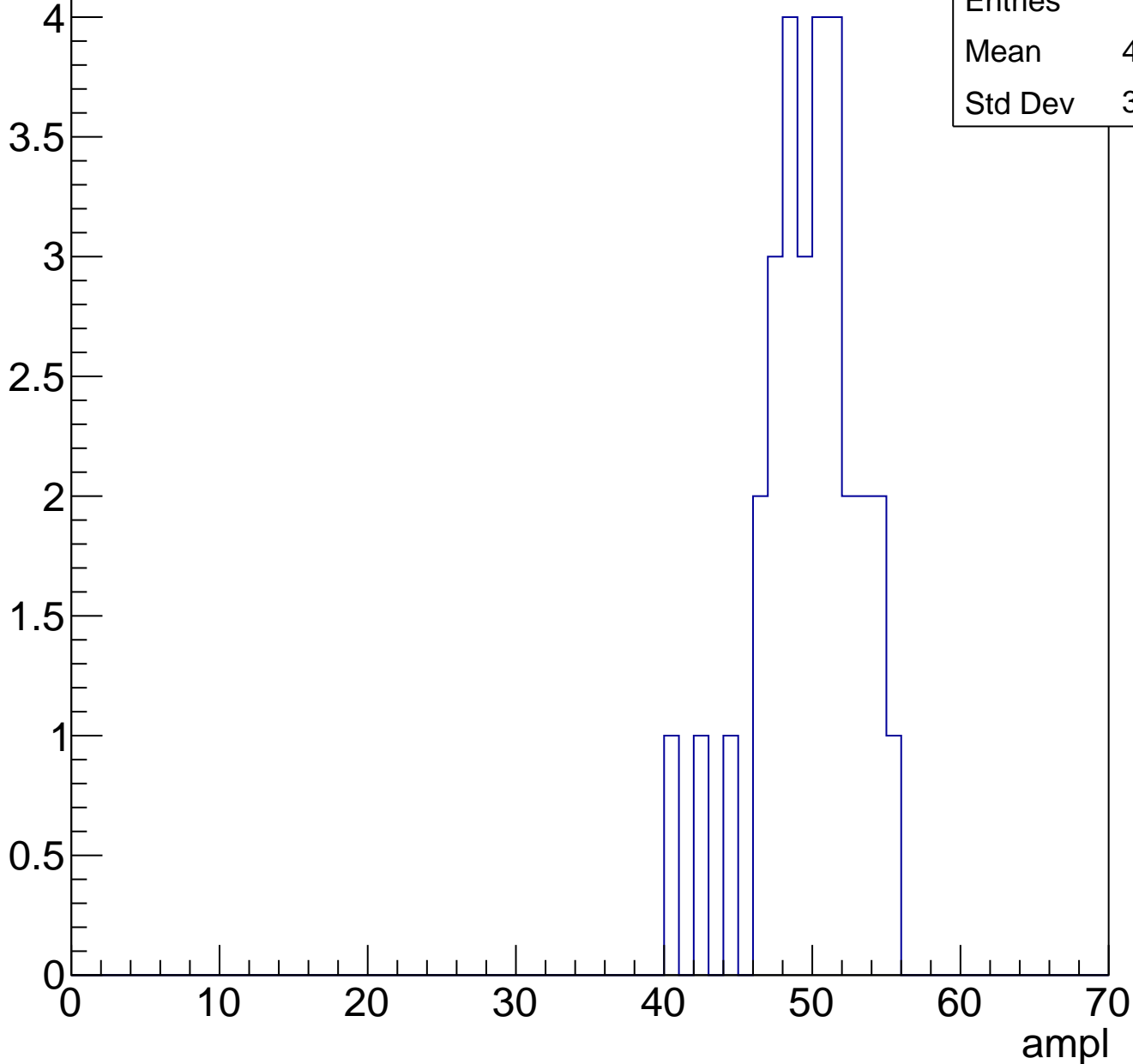
Entries	35
Mean	39.94
Std Dev	12.55



B1L103S, U14-ch79, adc3

calib_packv5_041523_1651.root, FC#0, port C2

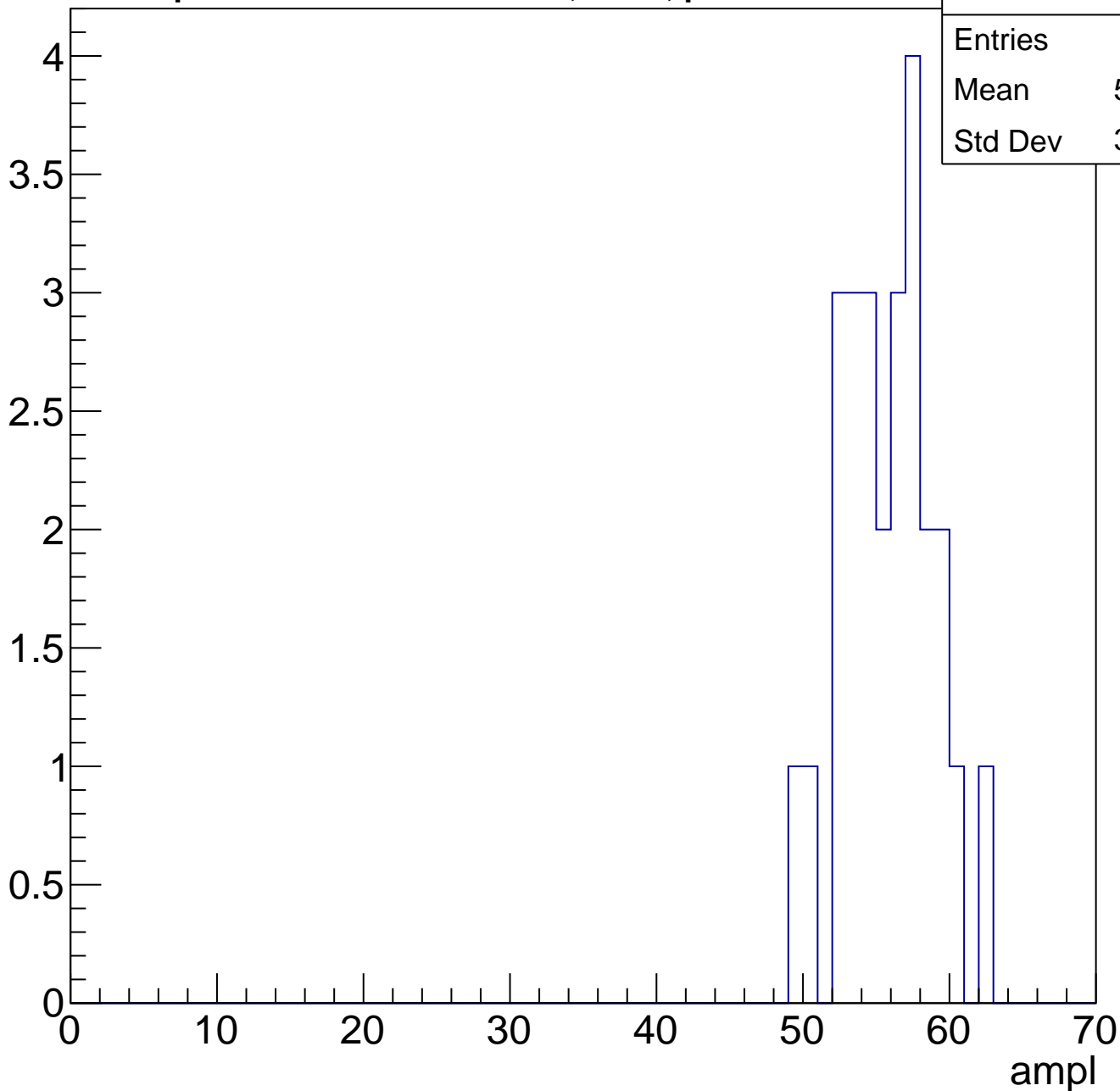
Entry



B1L103S, U14-ch79, adc4

calib_packv5_041523_1651.root, FC#0, port C2

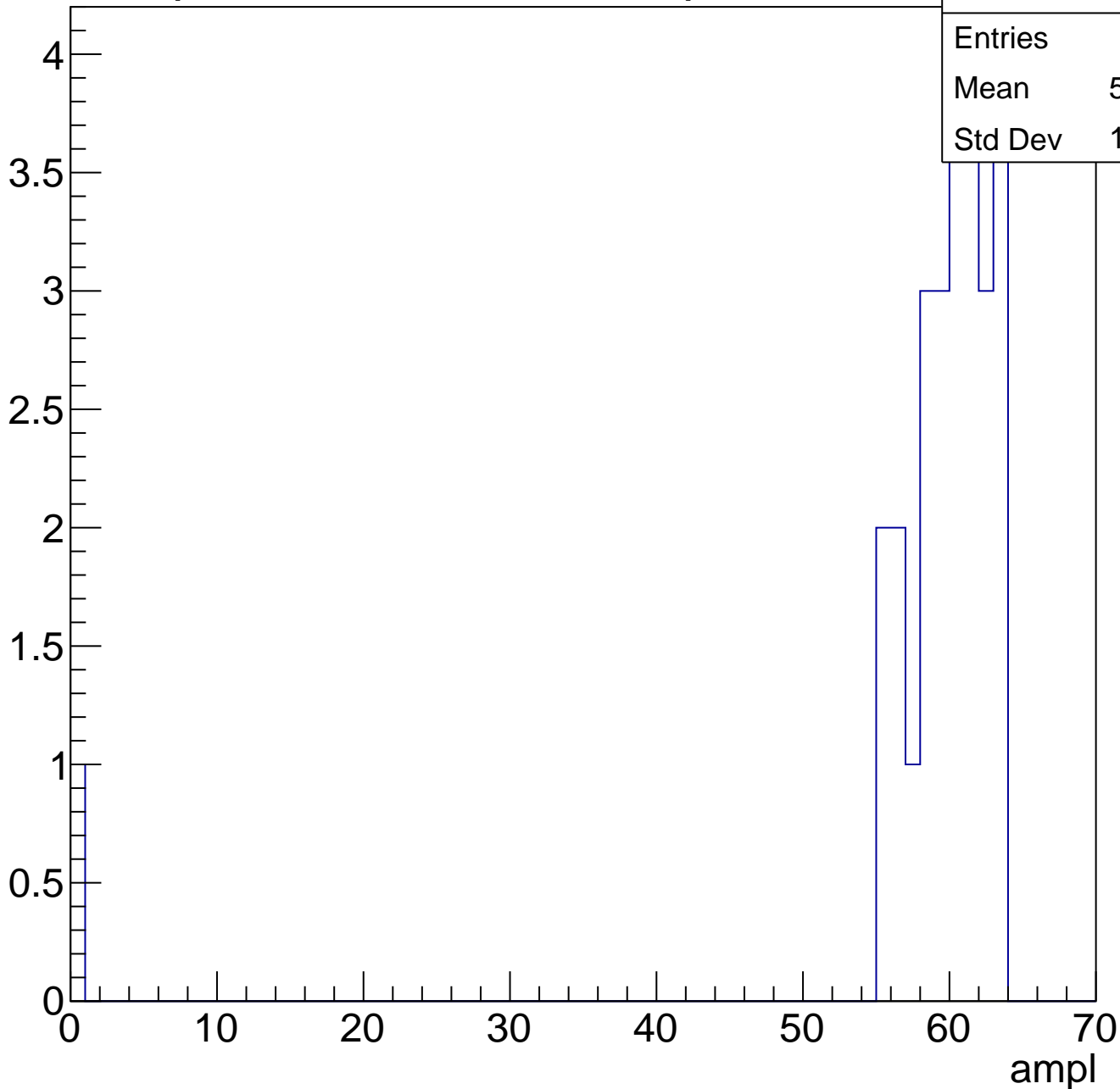
Entry



B1L103S, U14-ch79, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch79, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch79, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

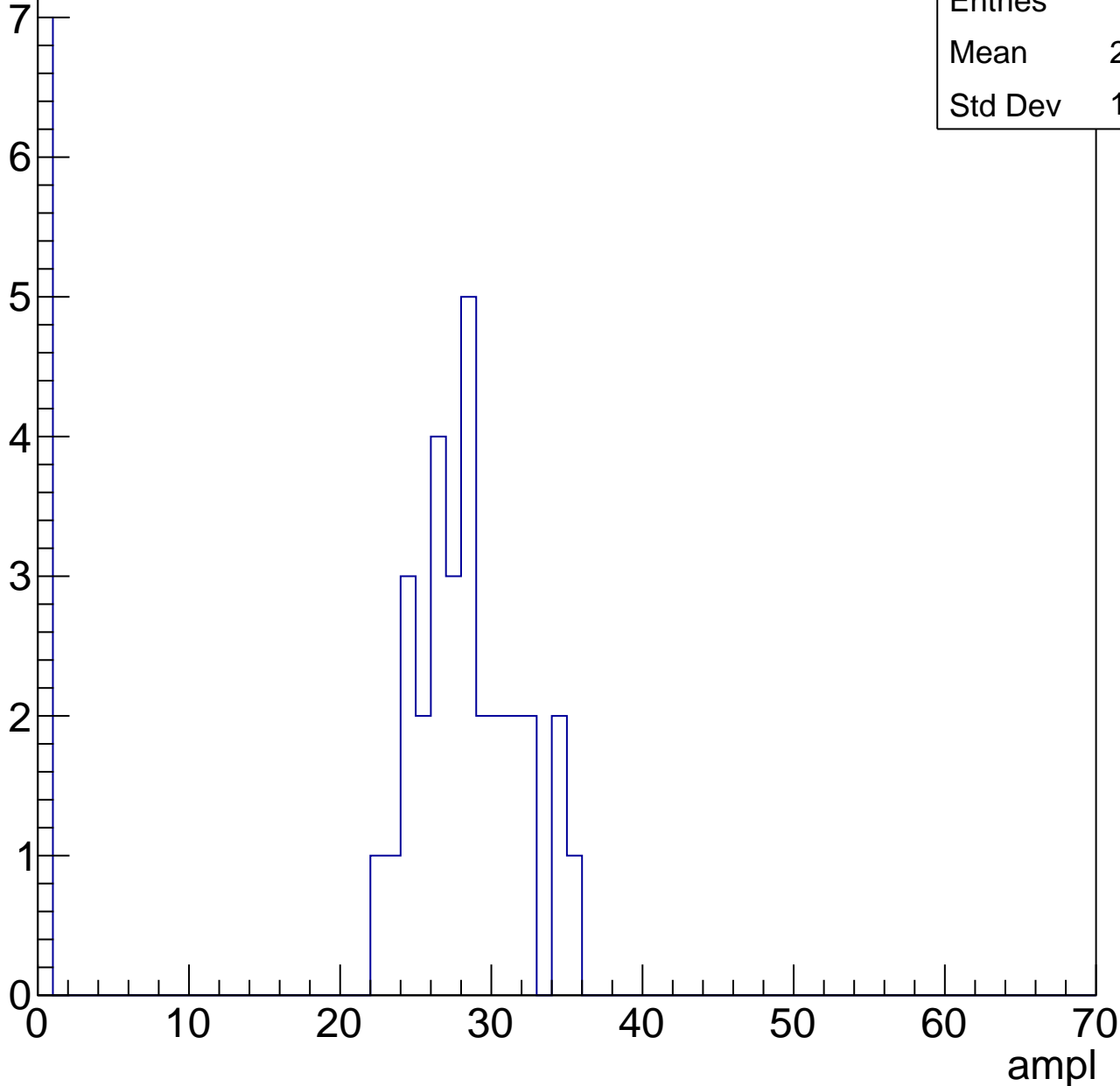
Entries	11
Mean	0
Std Dev	0

B1L103S, U14-ch80, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	37
Mean	22.68
Std Dev	11.35

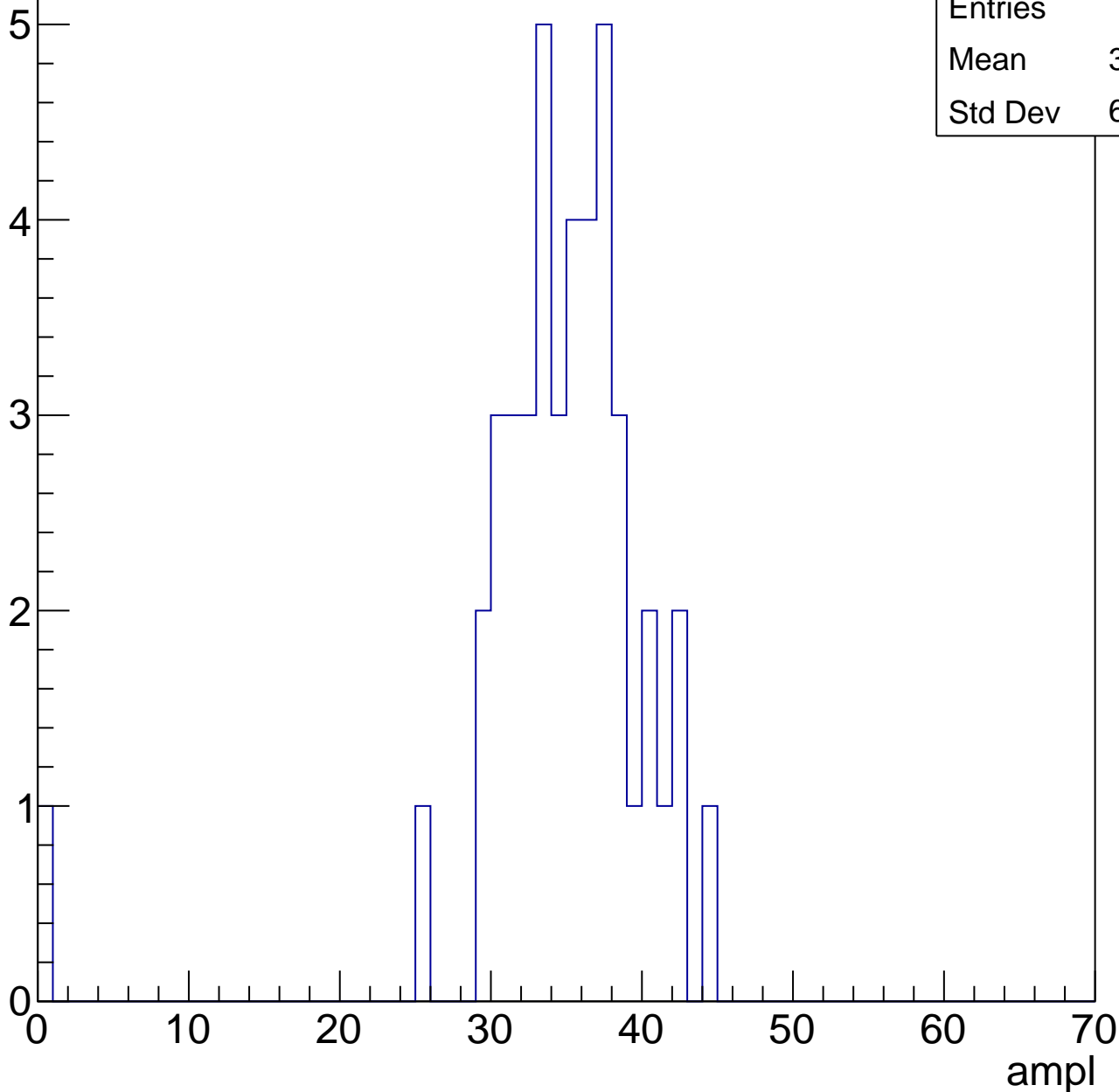


B1L103S, U14-ch80, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	44
Mean	34.09
Std Dev	6.512

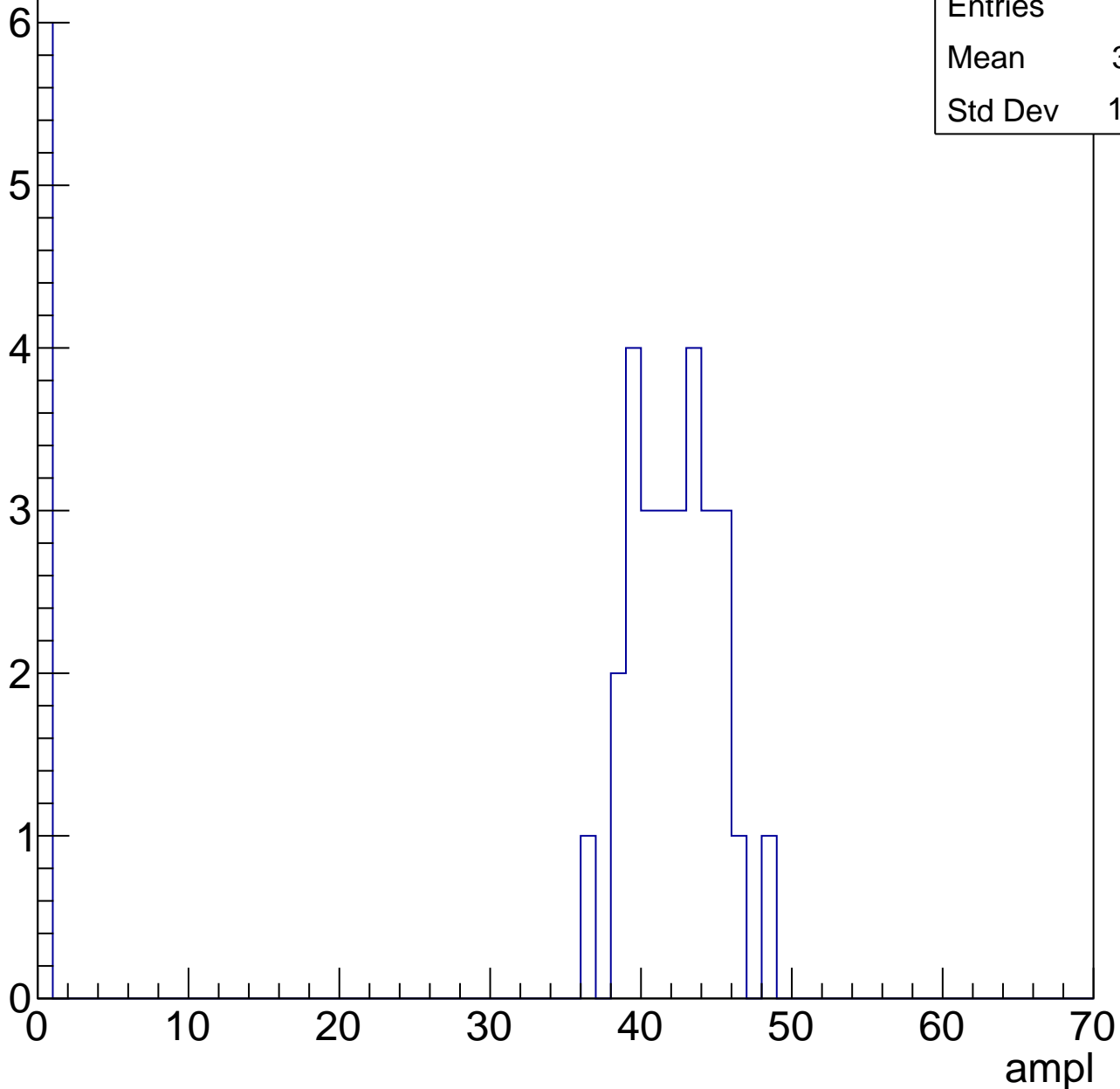


B1L103S, U14-ch80, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

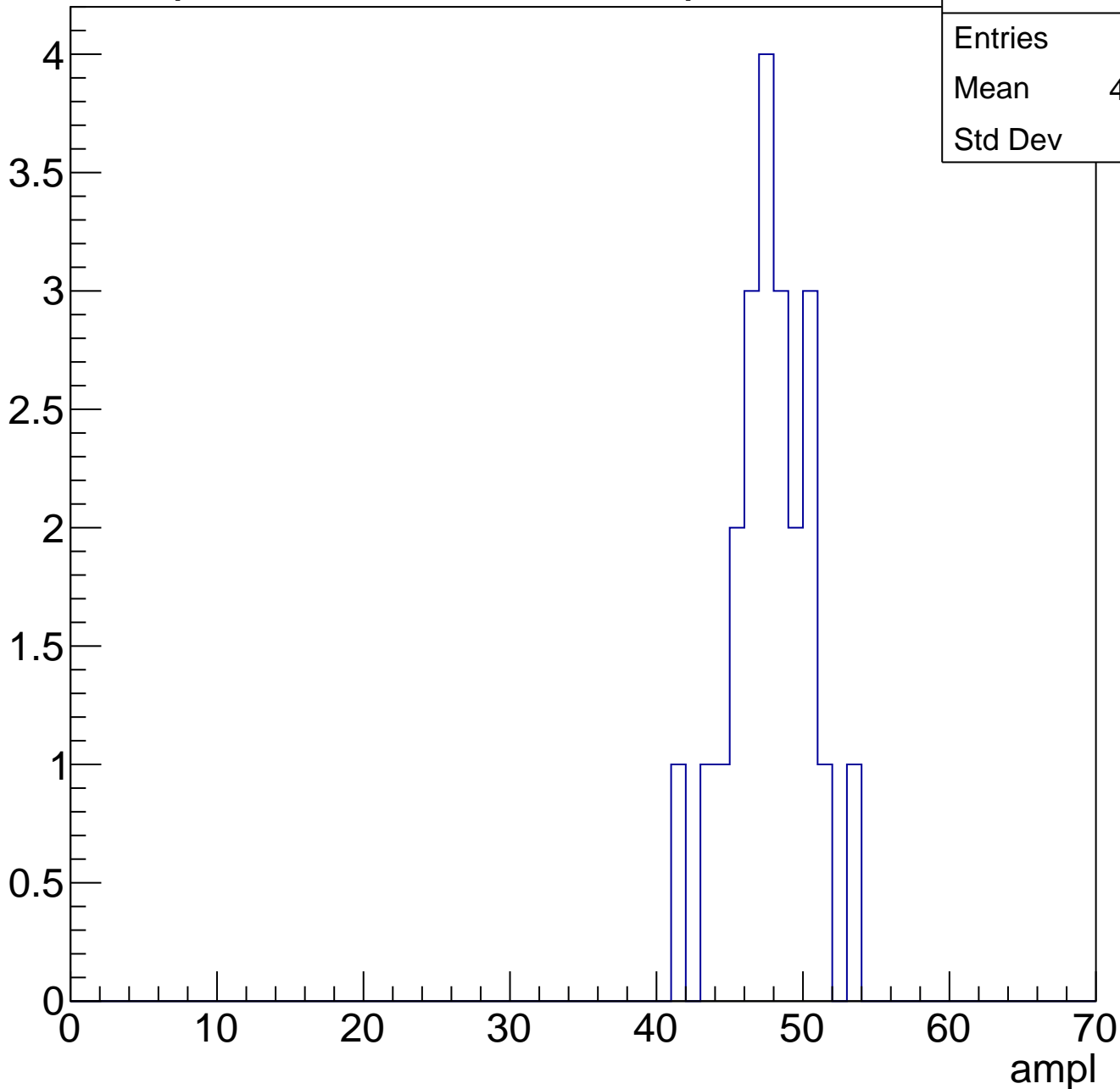
Entries	34
Mean	34.41
Std Dev	16.12



B1L103S, U14-ch80, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry



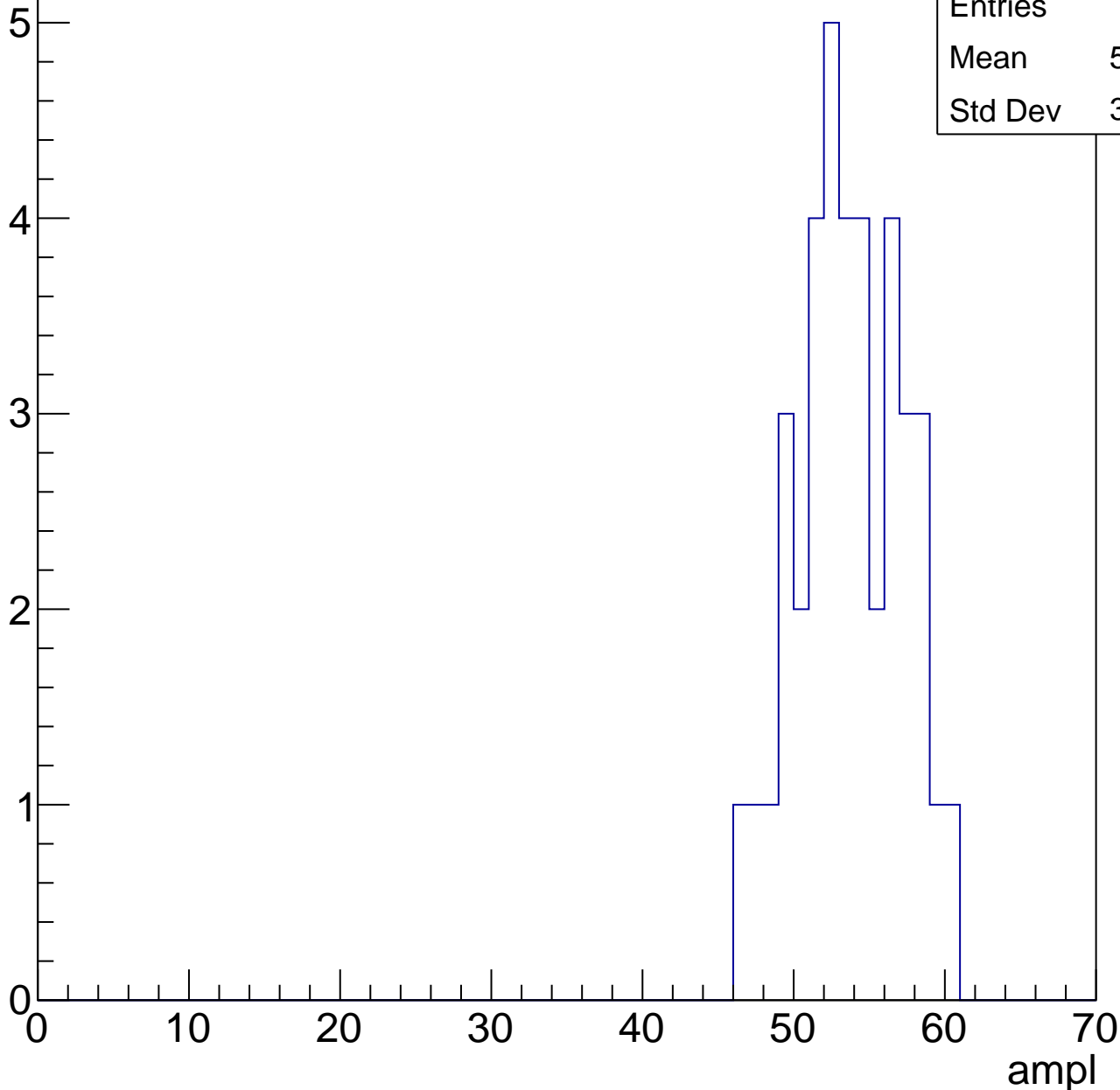
Entries	22
Mean	47.27
Std Dev	2.7

B1L103S, U14-ch80, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

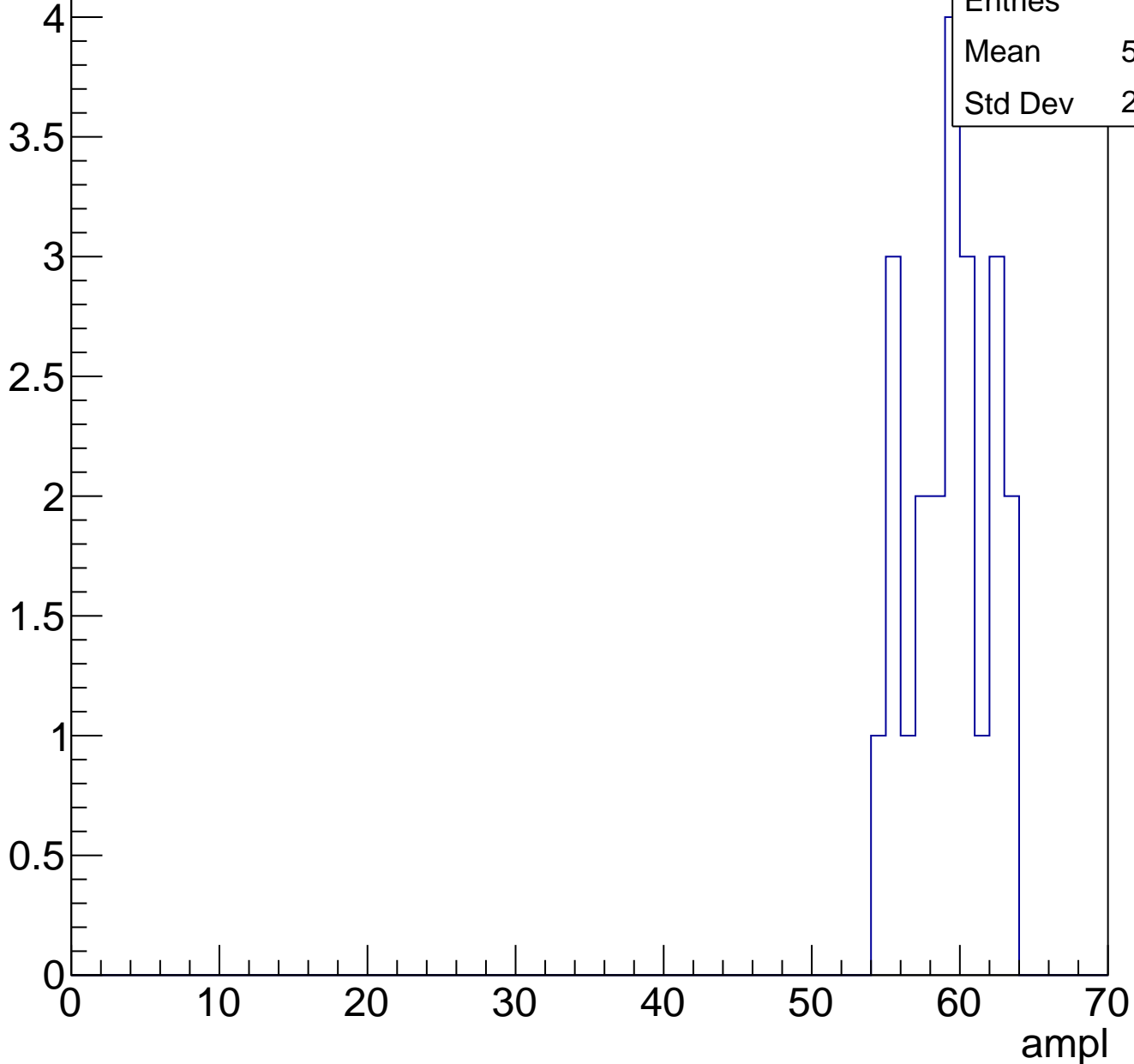
Entries	39
Mean	53.28
Std Dev	3.396



B1L103S, U14-ch80, adc5

calib_packv5_041523_1651.root, FC#0, port C2

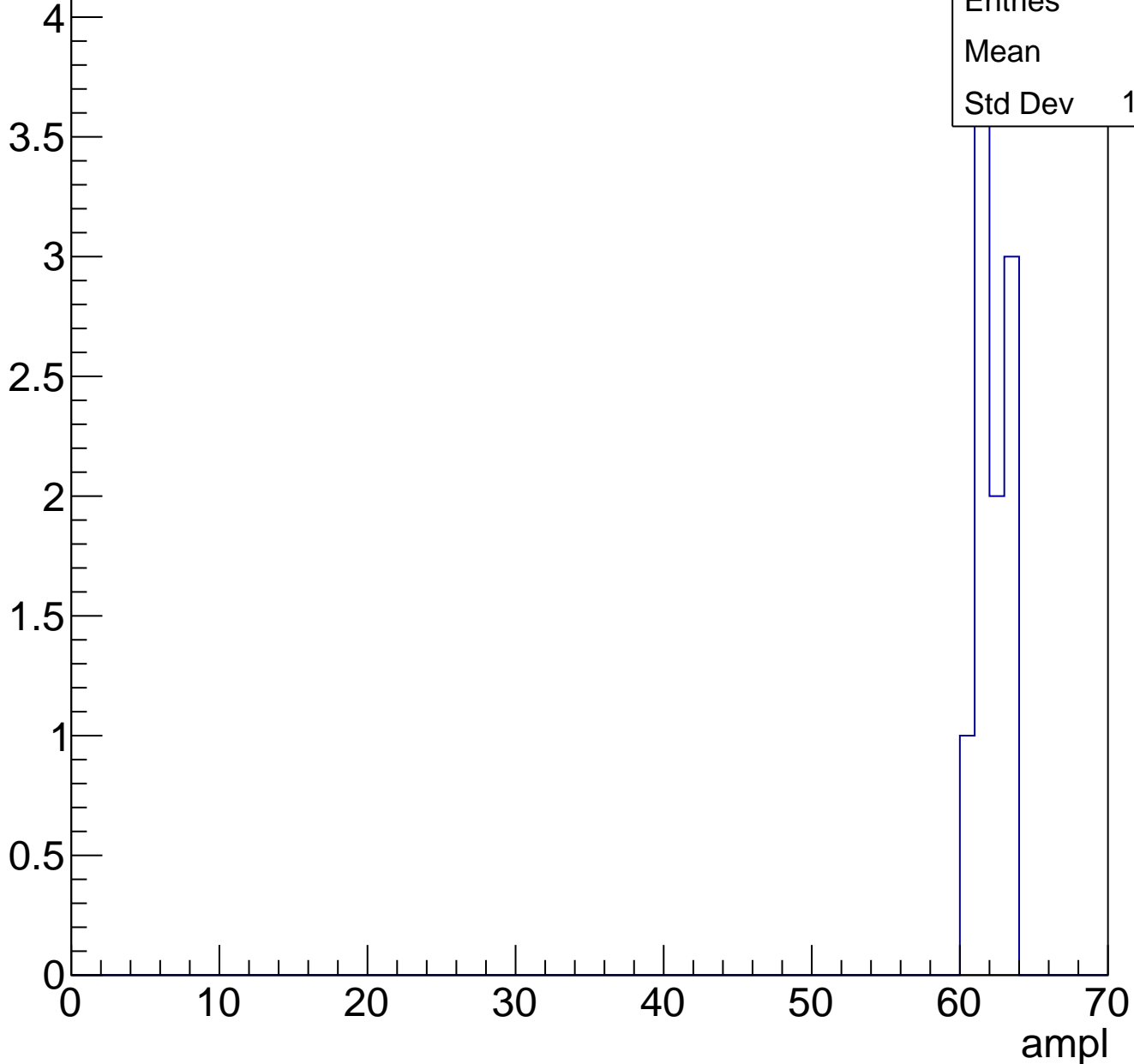
Entry



B1L103S, U14-ch80, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



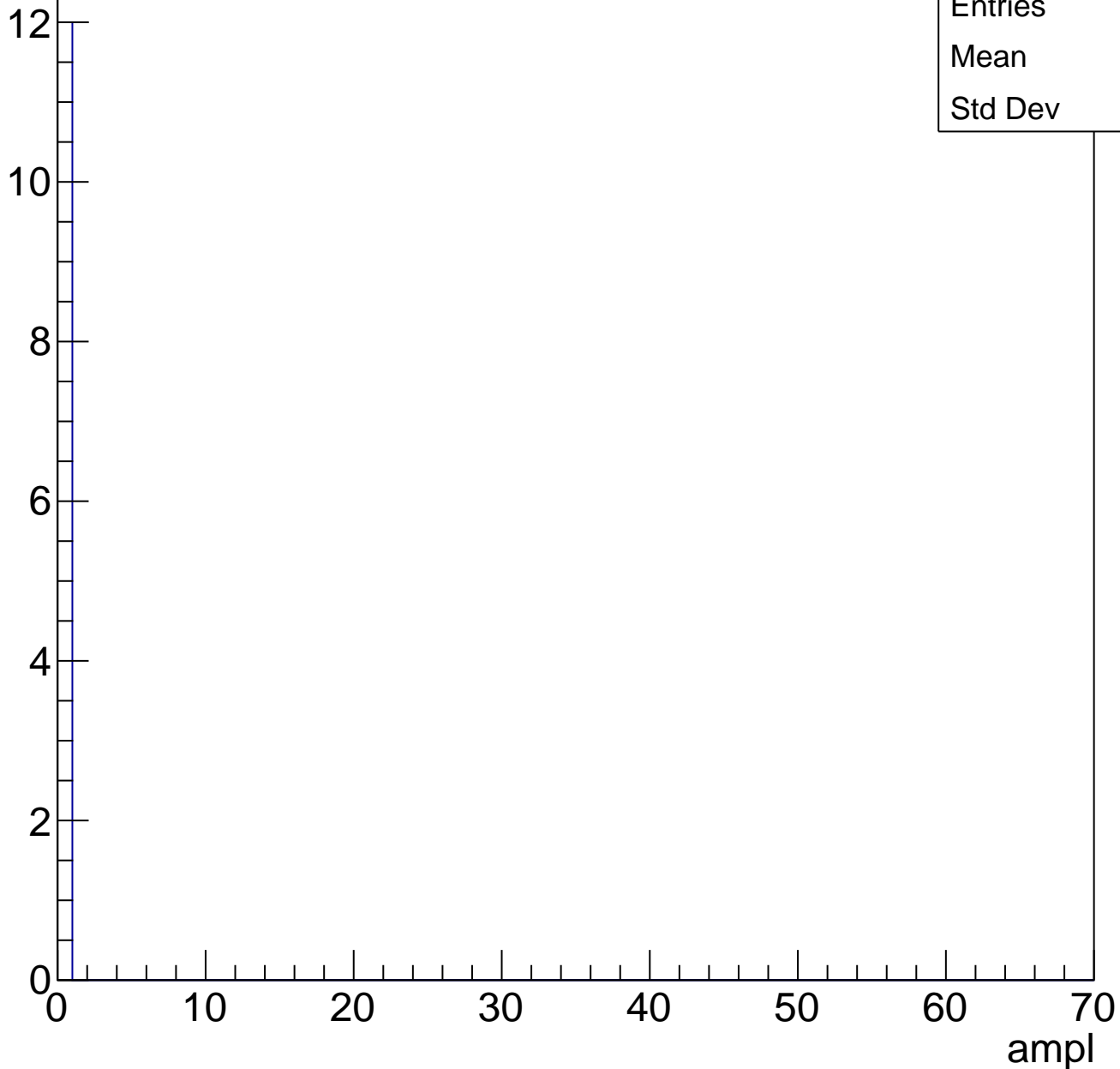
Entries	10
Mean	61.7
Std Dev	1.005

B1L103S, U14-ch80, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	12
Mean	0
Std Dev	0

Entry

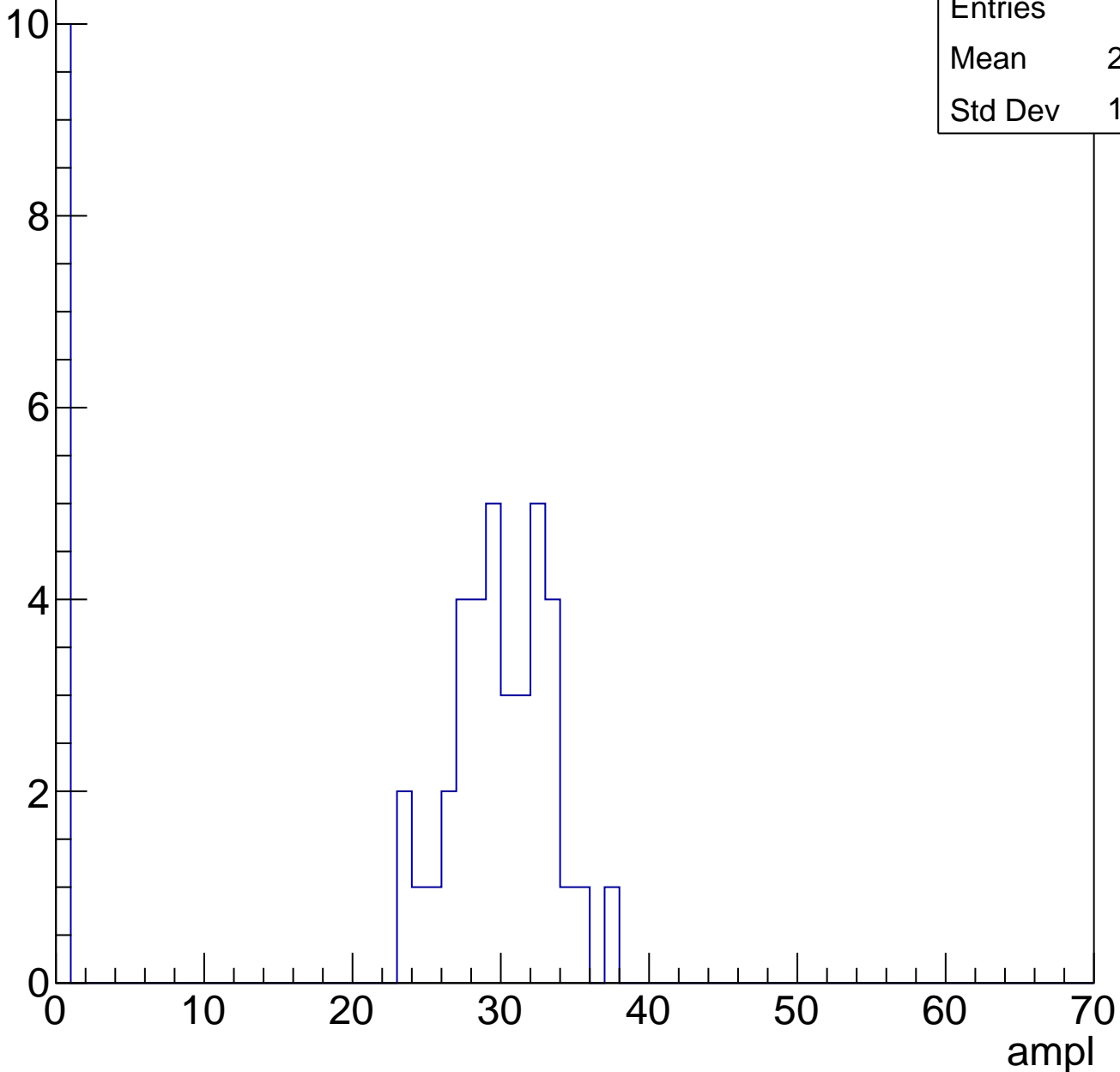


B1L103S, U14-ch81, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	47
Mean	23.26
Std Dev	12.43

Entry

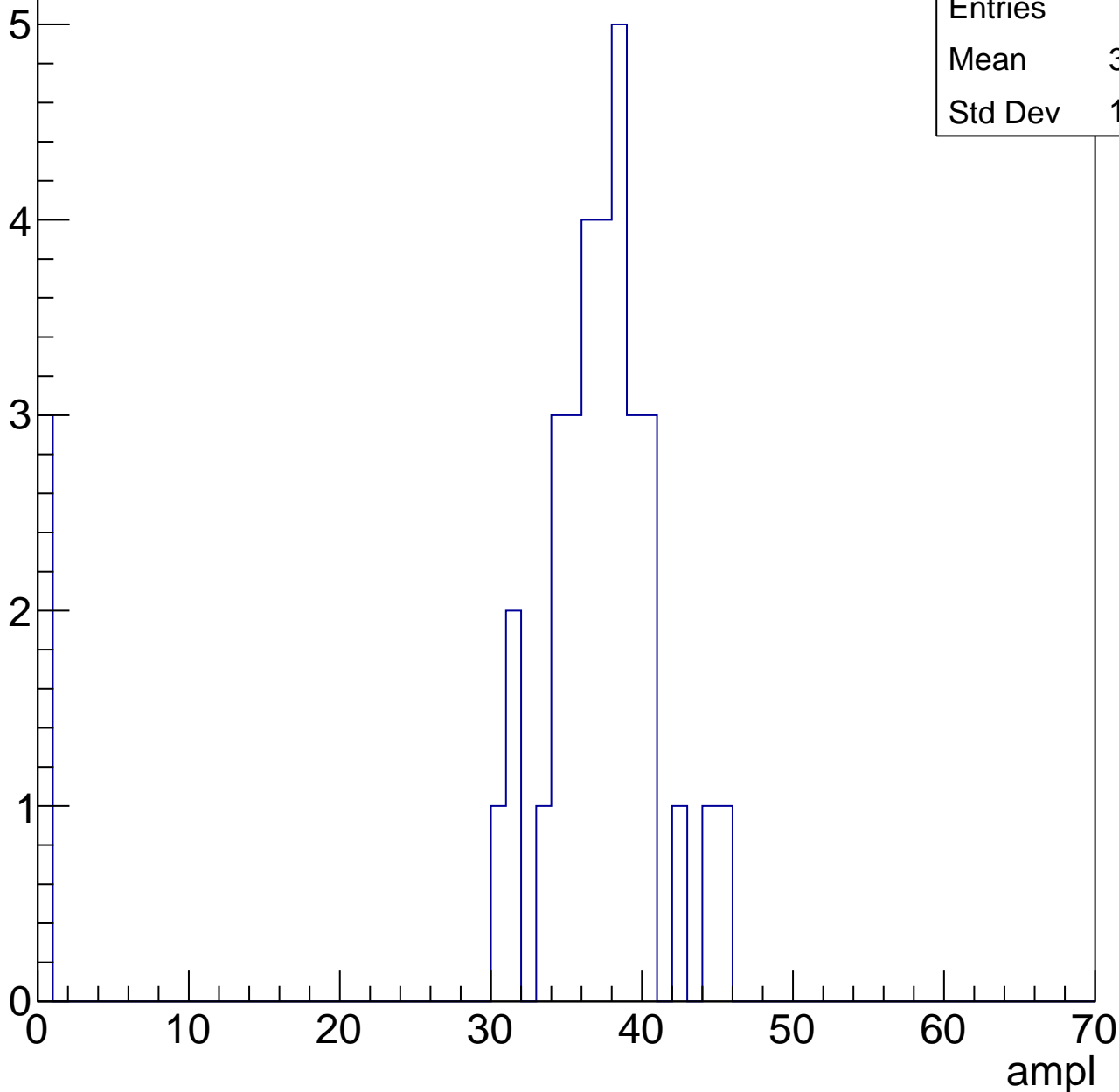


B1L103S, U14-ch81, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	35
Mean	33.77
Std Dev	10.83

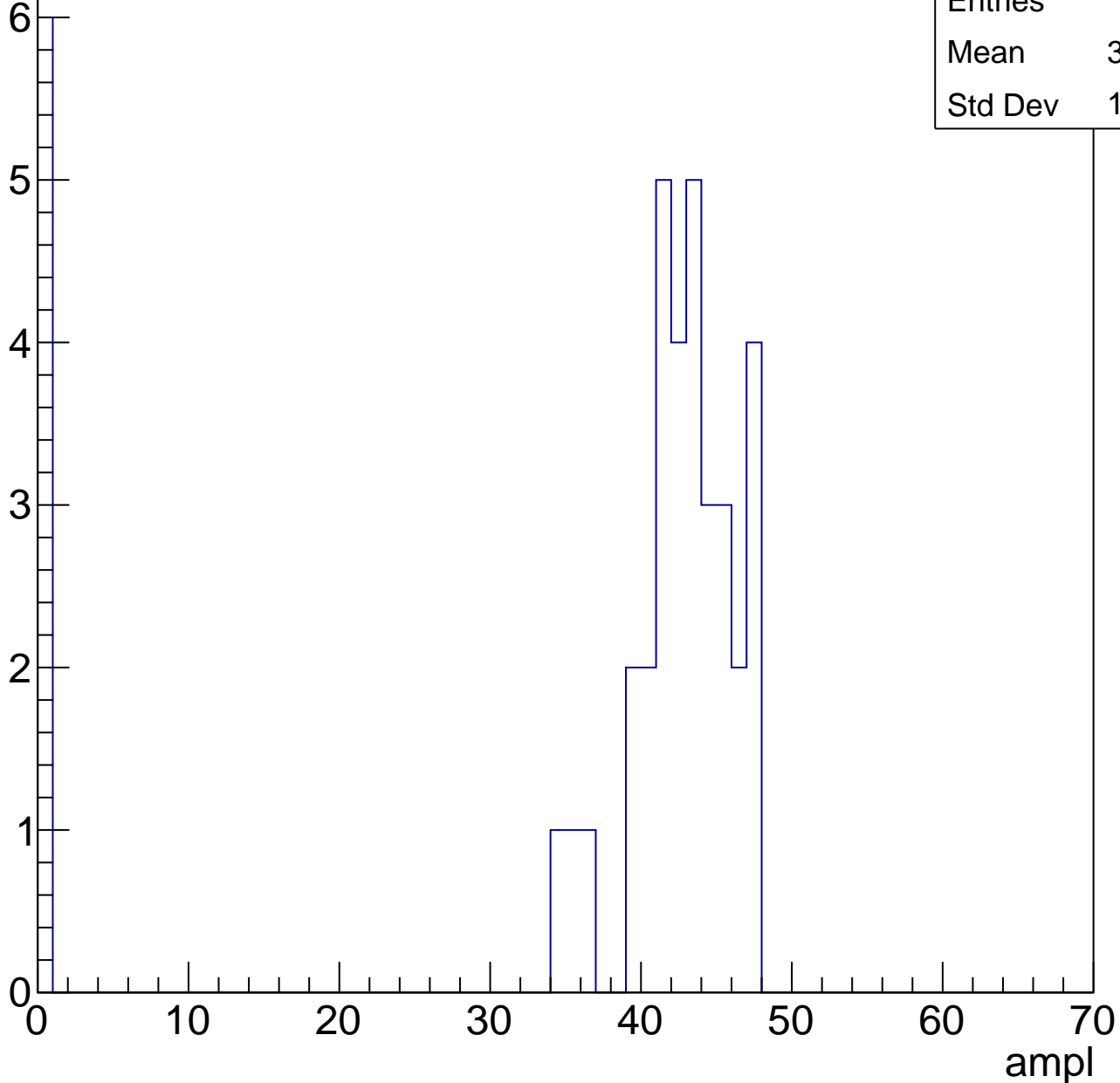


B1L103S, U14-ch81, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	35.85
Std Dev	15.58



B1L103S, U14-ch81, adc3

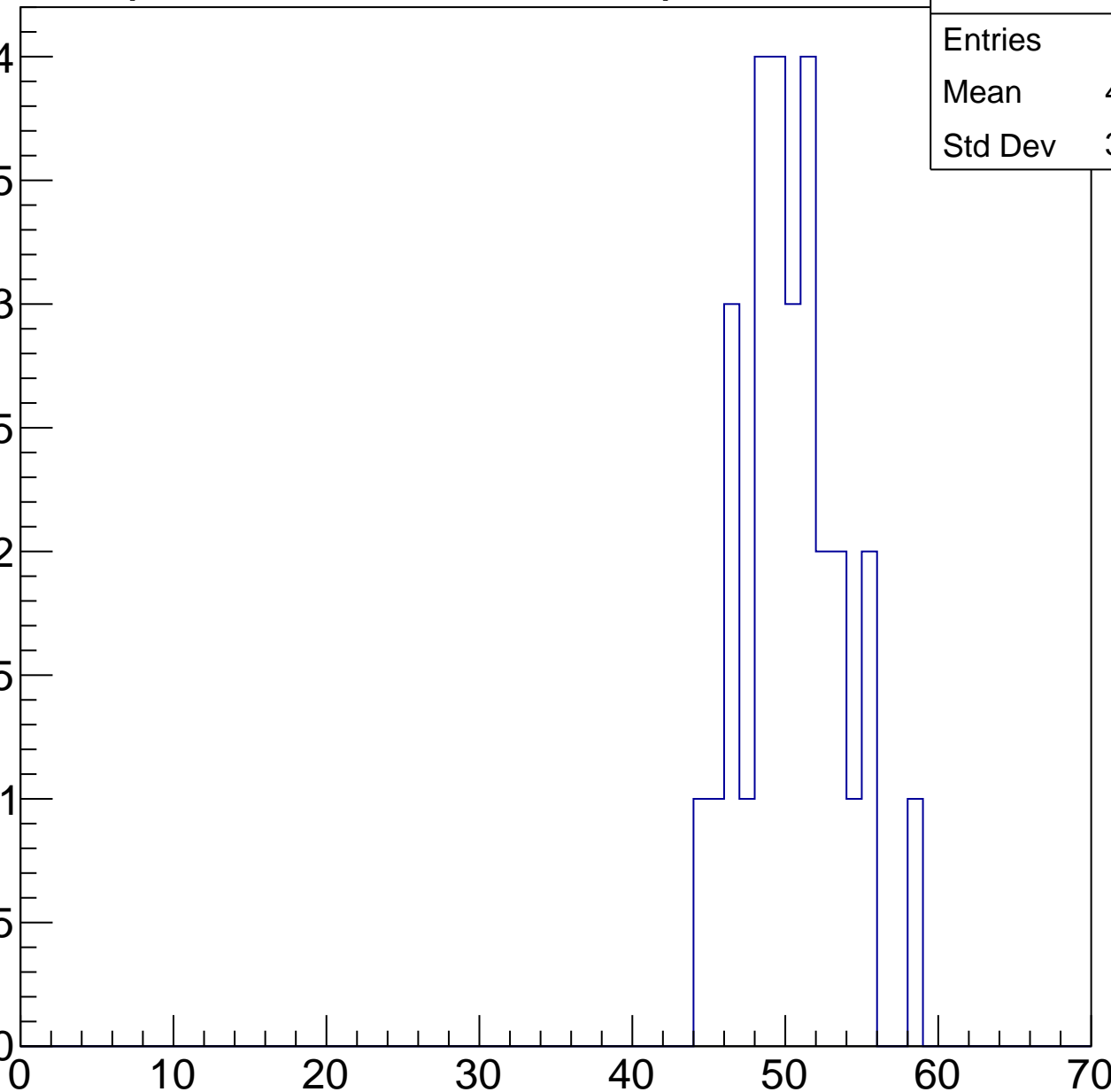
calib_packv5_041523_1651.root, FC#0, port C2

Entry

4
3.5
3
2.5
2
1.5
1
0.5
0

Entries	29
Mean	49.93
Std Dev	3.205

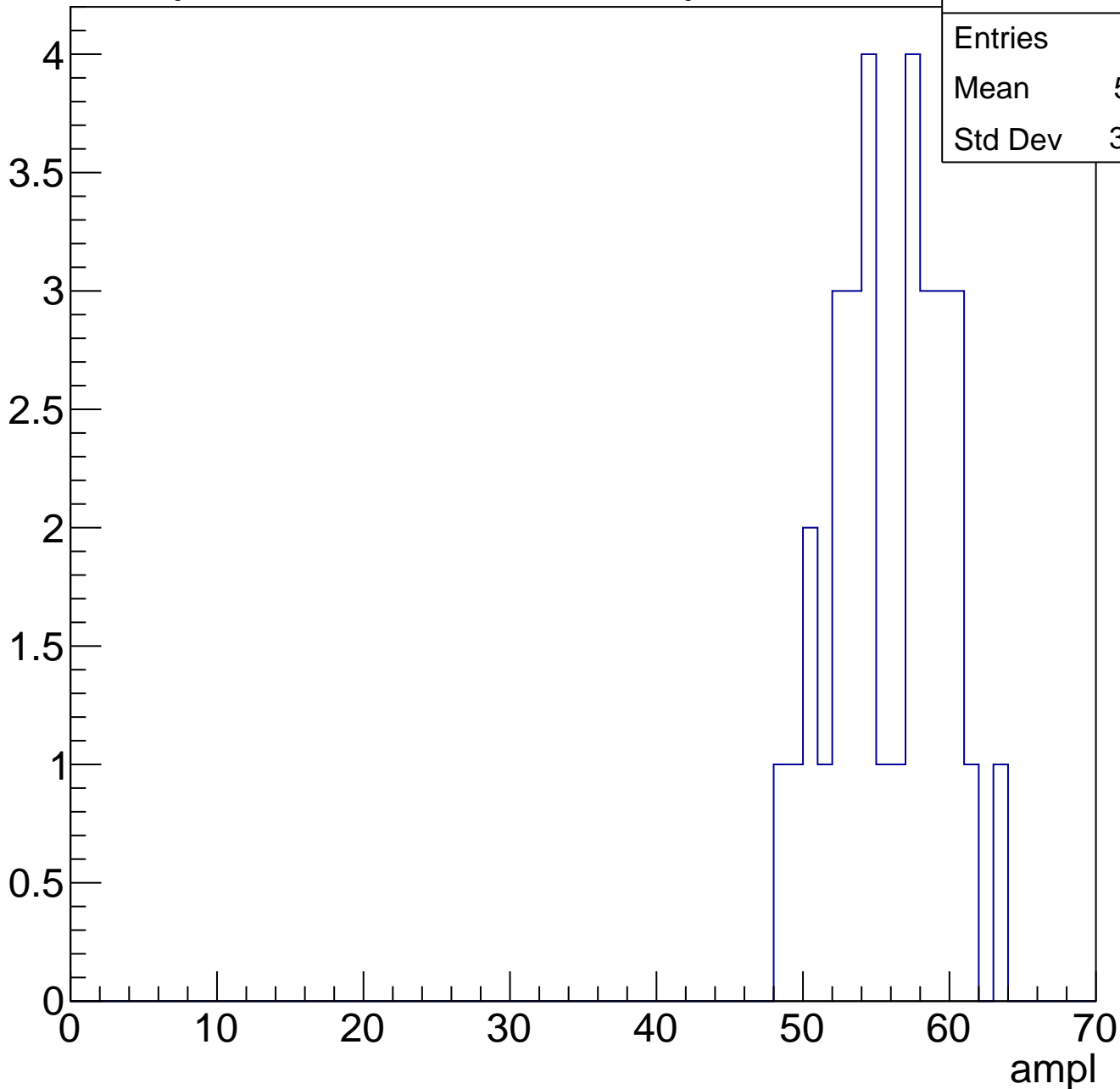
ampl



B1L103S, U14-ch81, adc4

calib_packv5_041523_1651.root, FC#0, port C2

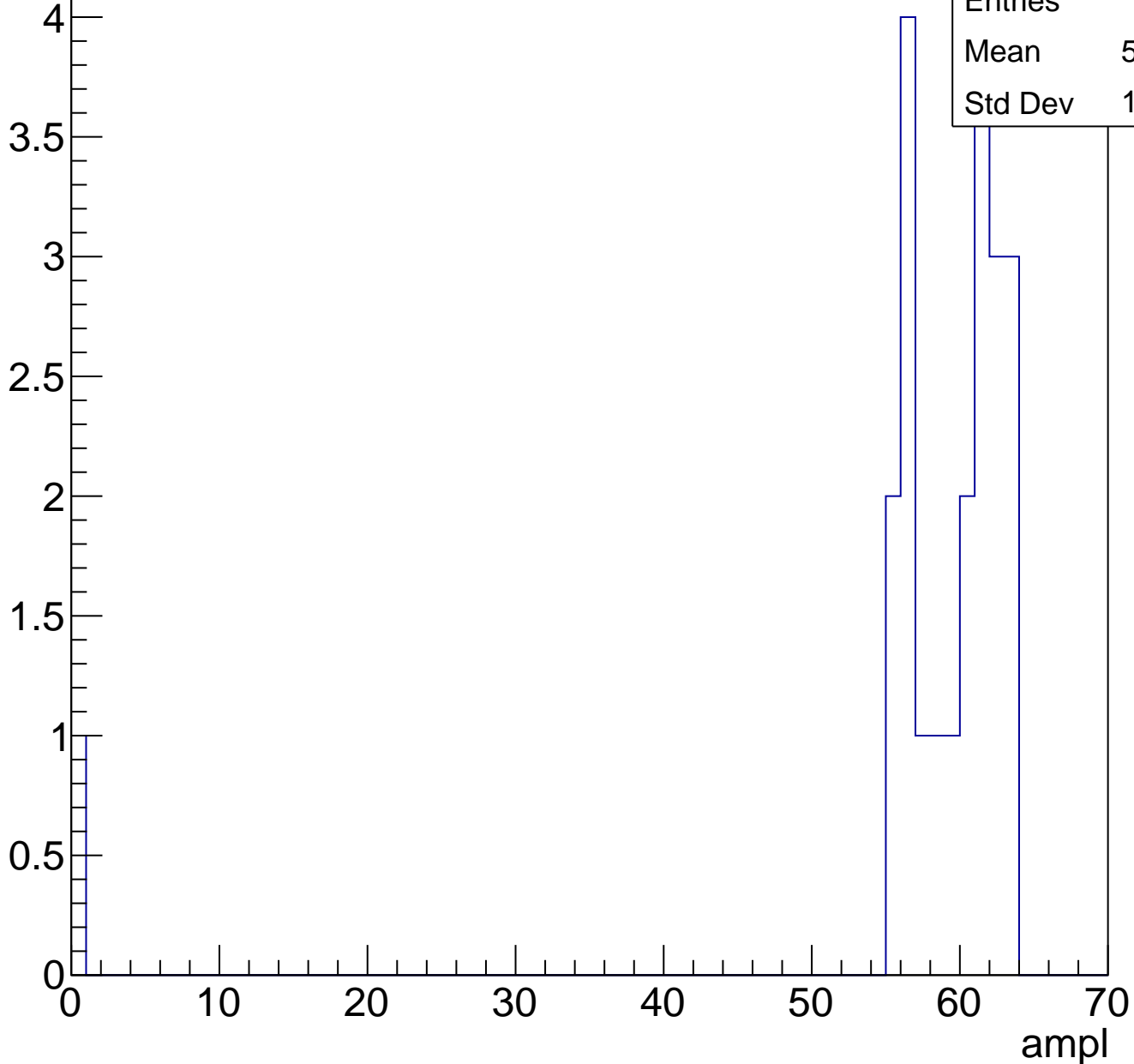
Entry



B1L103S, U14-ch81, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch81, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	4
Mean	61.5
Std Dev	1.5

B1L103S, U14-ch81, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch82, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	50
Mean	19.38
Std Dev	13.28

Entry

10

8

6

4

2

0

0

10

20

30

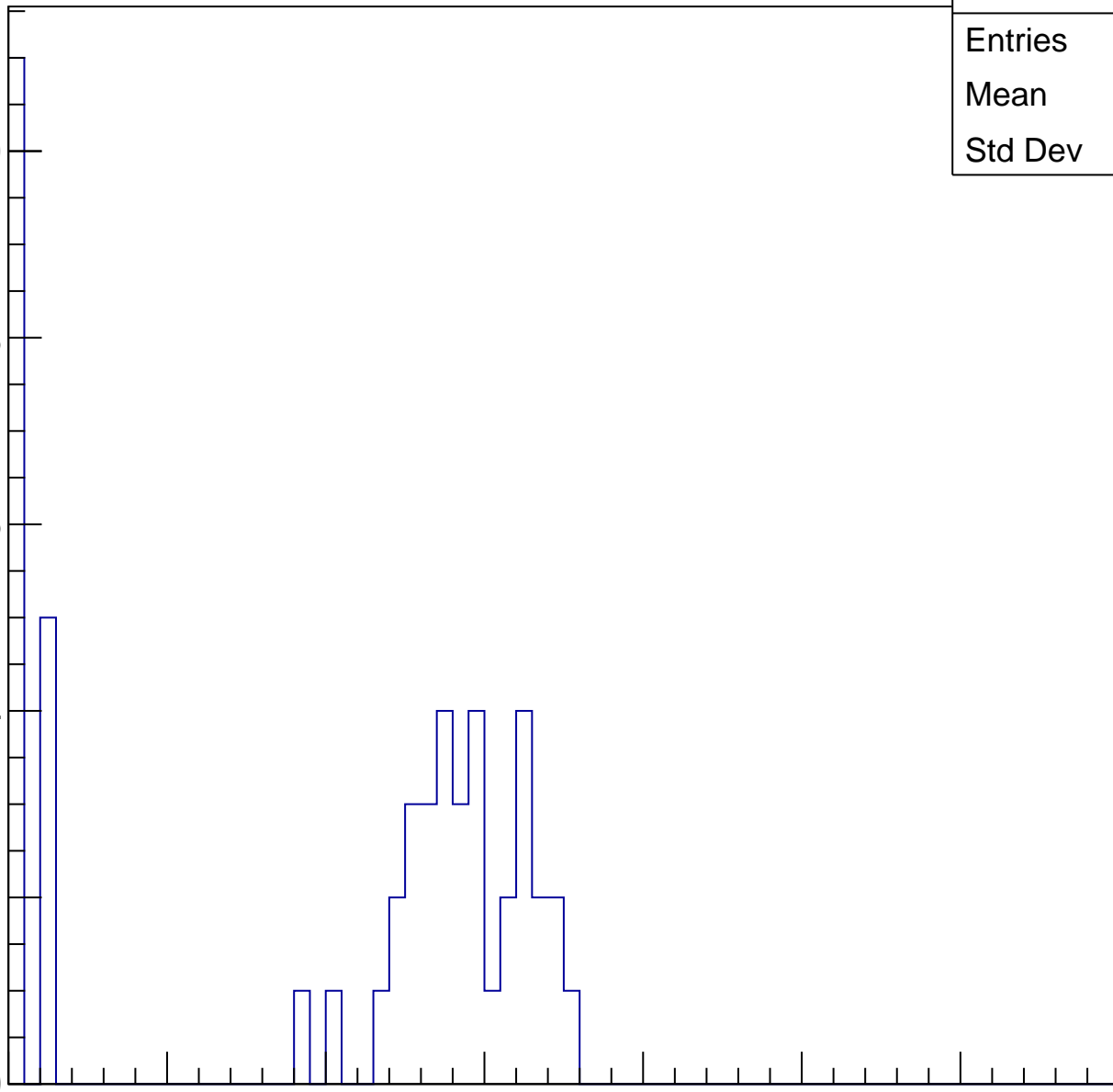
40

50

60

70

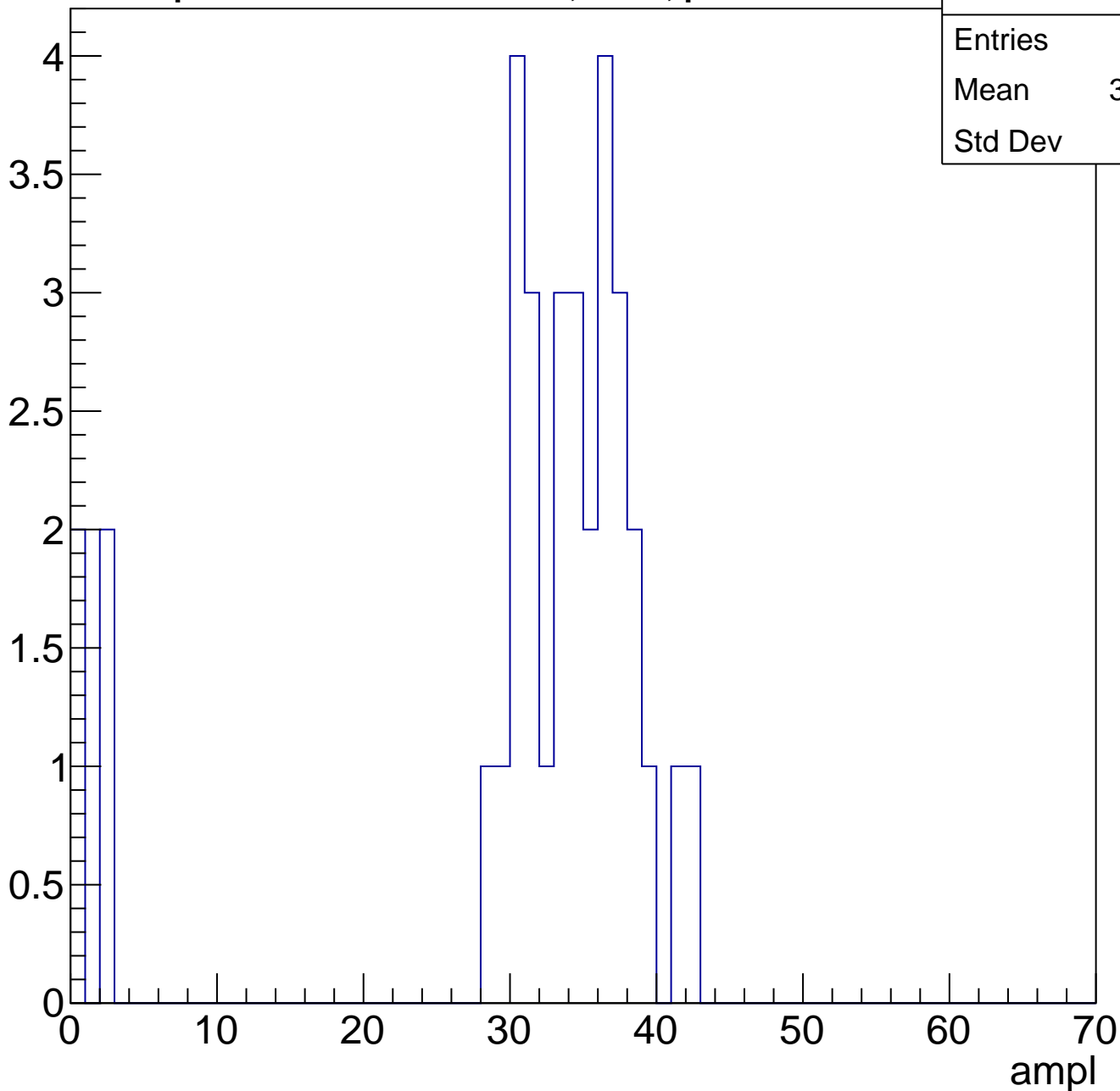
ampl



B1L103S, U14-ch82, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

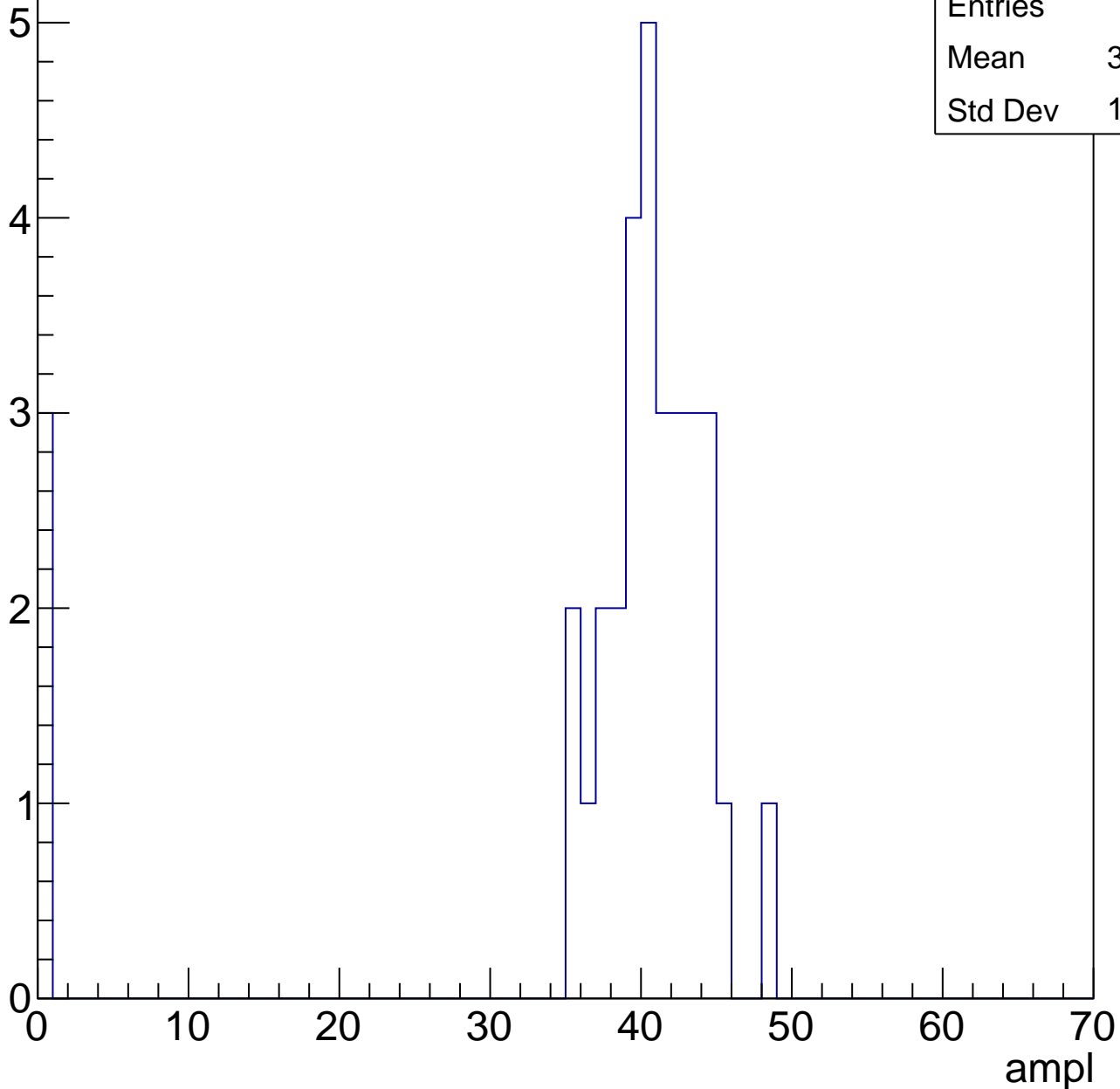


B1L103S, U14-ch82, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	33
Mean	36.82
Std Dev	11.99

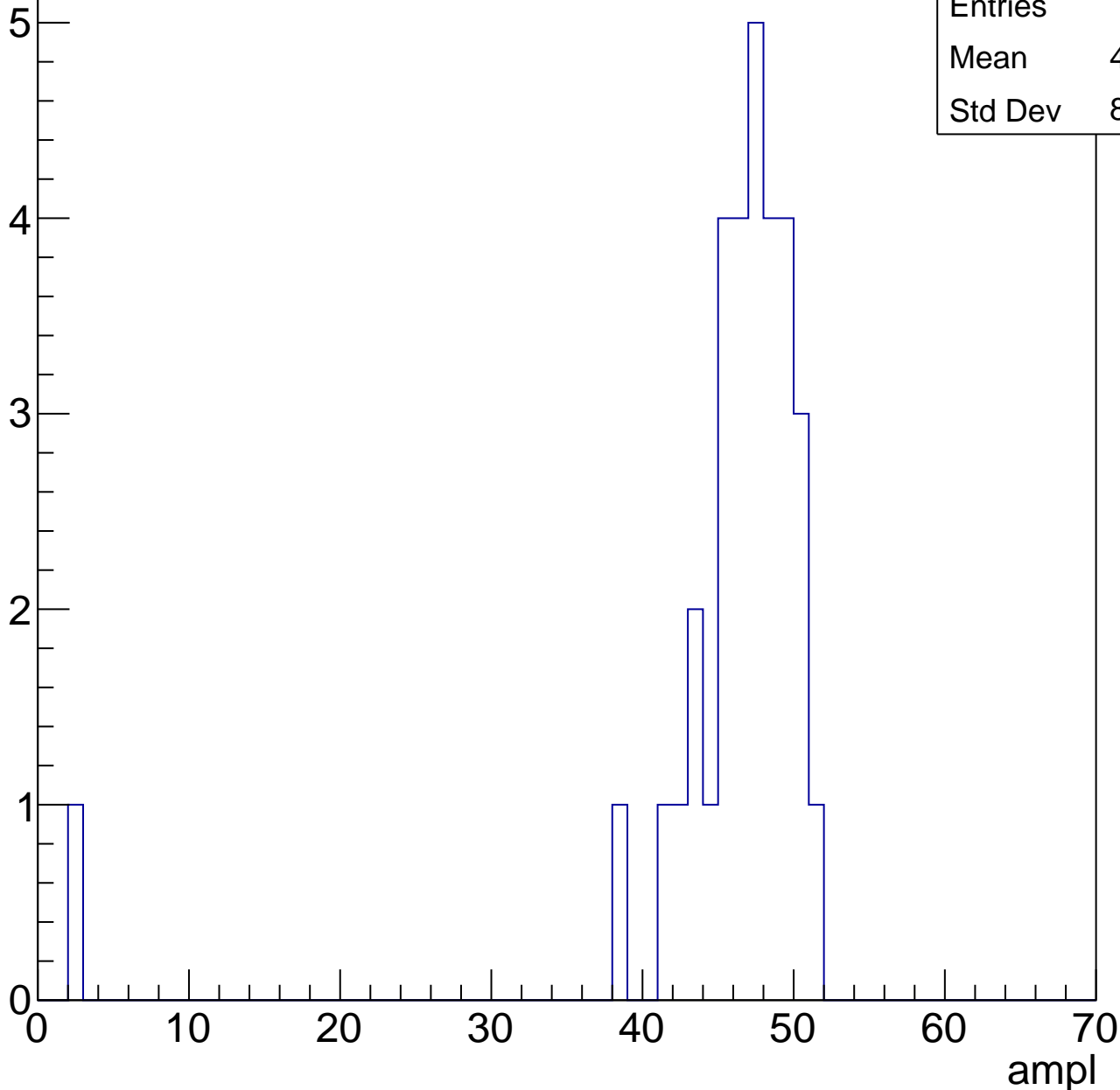


B1L103S, U14-ch82, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

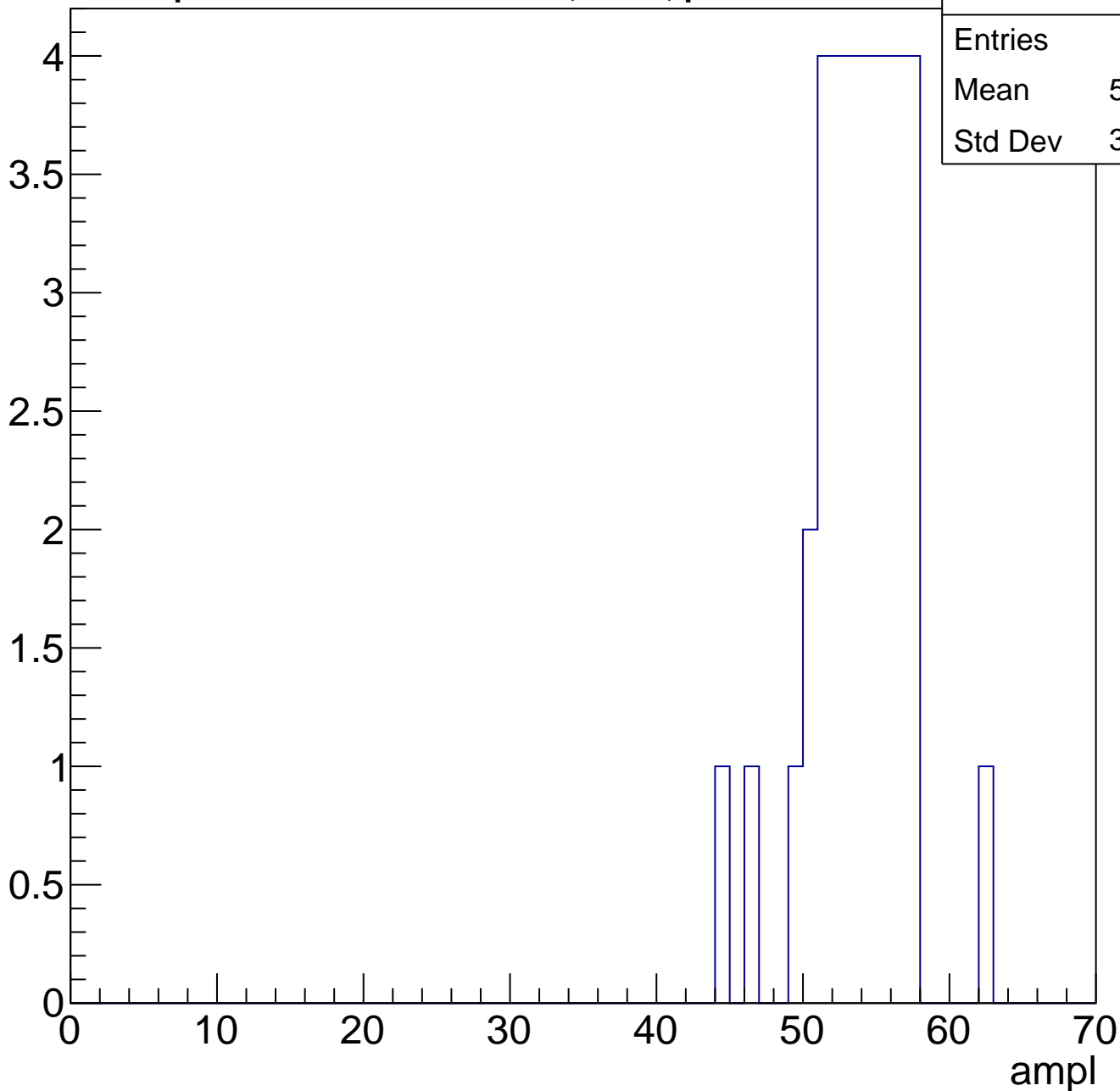
Entries	32
Mean	45.03
Std Dev	8.229



B1L103S, U14-ch82, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



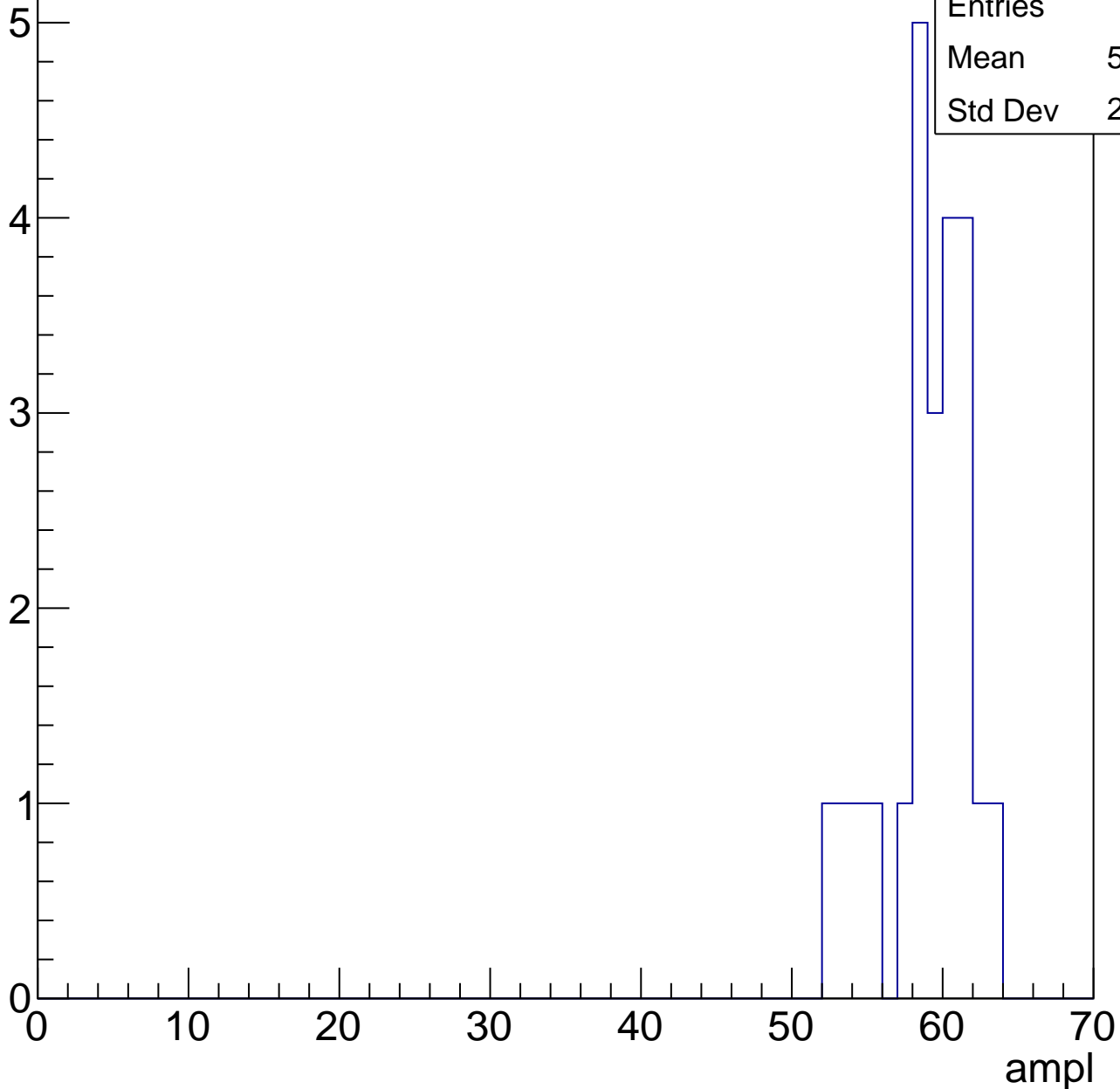
Entries	34
Mean	53.32
Std Dev	3.349

B1L103S, U14-ch82, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	23
Mean	58.57
Std Dev	2.764



B1L103S, U14-ch82, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries	11
Mean	60.91
Std Dev	2.109

B1L103S, U14-ch82, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	14
Mean	4.5
Std Dev	16.22

Entry

12

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

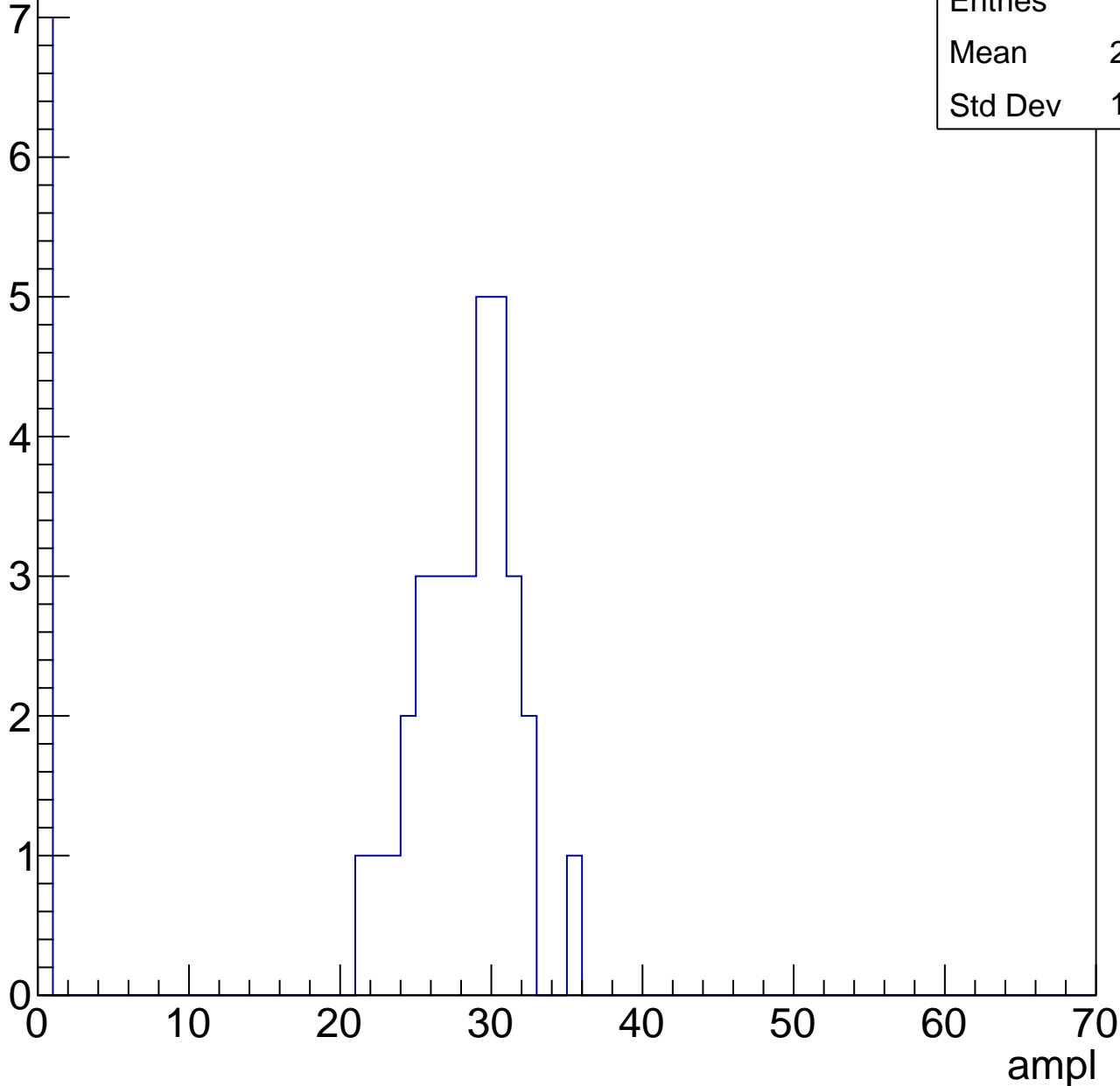
70

B1L103S, U14-ch83, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	22.98
Std Dev	10.95

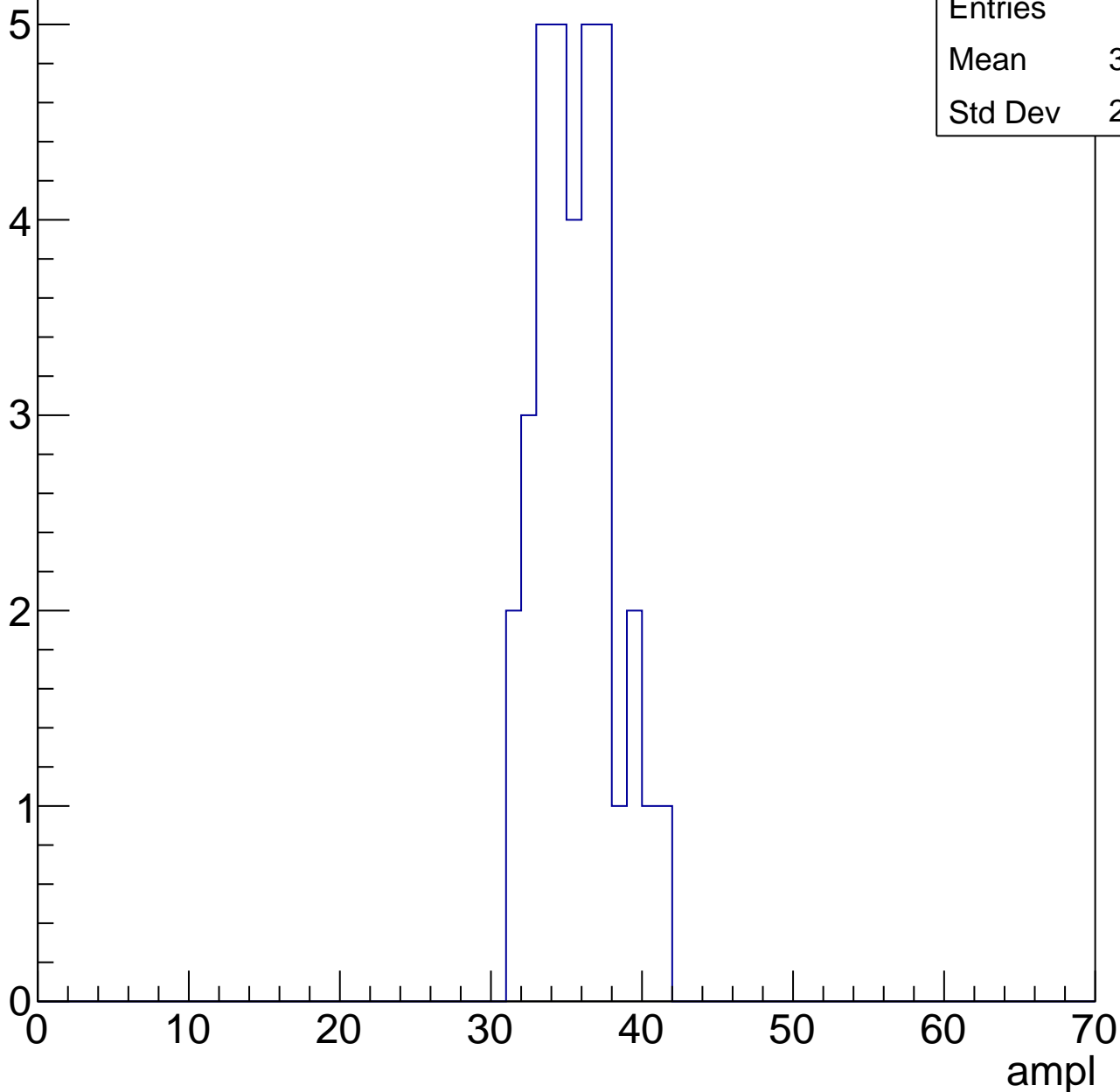


B1L103S, U14-ch83, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

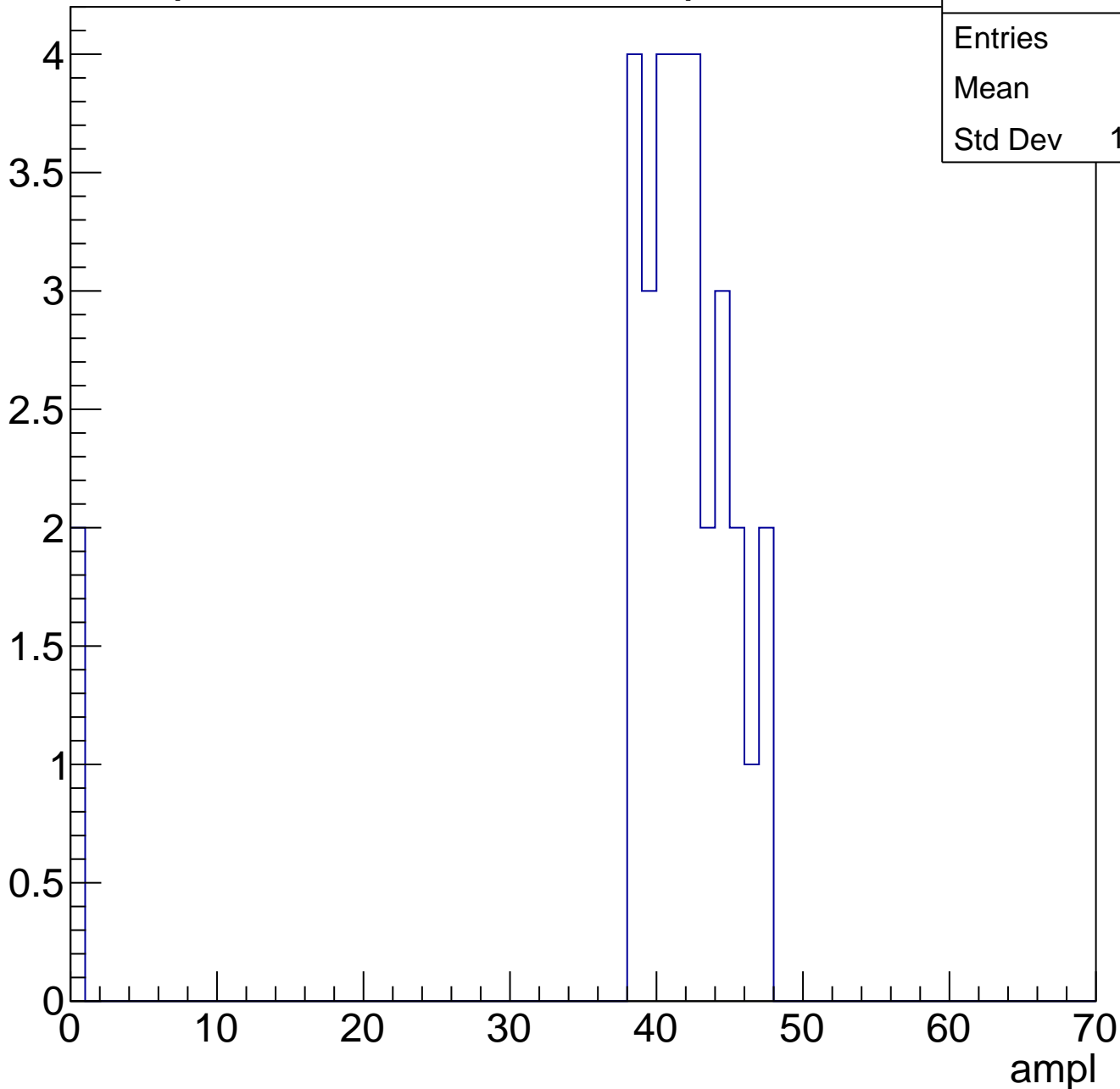
Entries	34
Mean	35.15
Std Dev	2.487



B1L103S, U14-ch83, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry



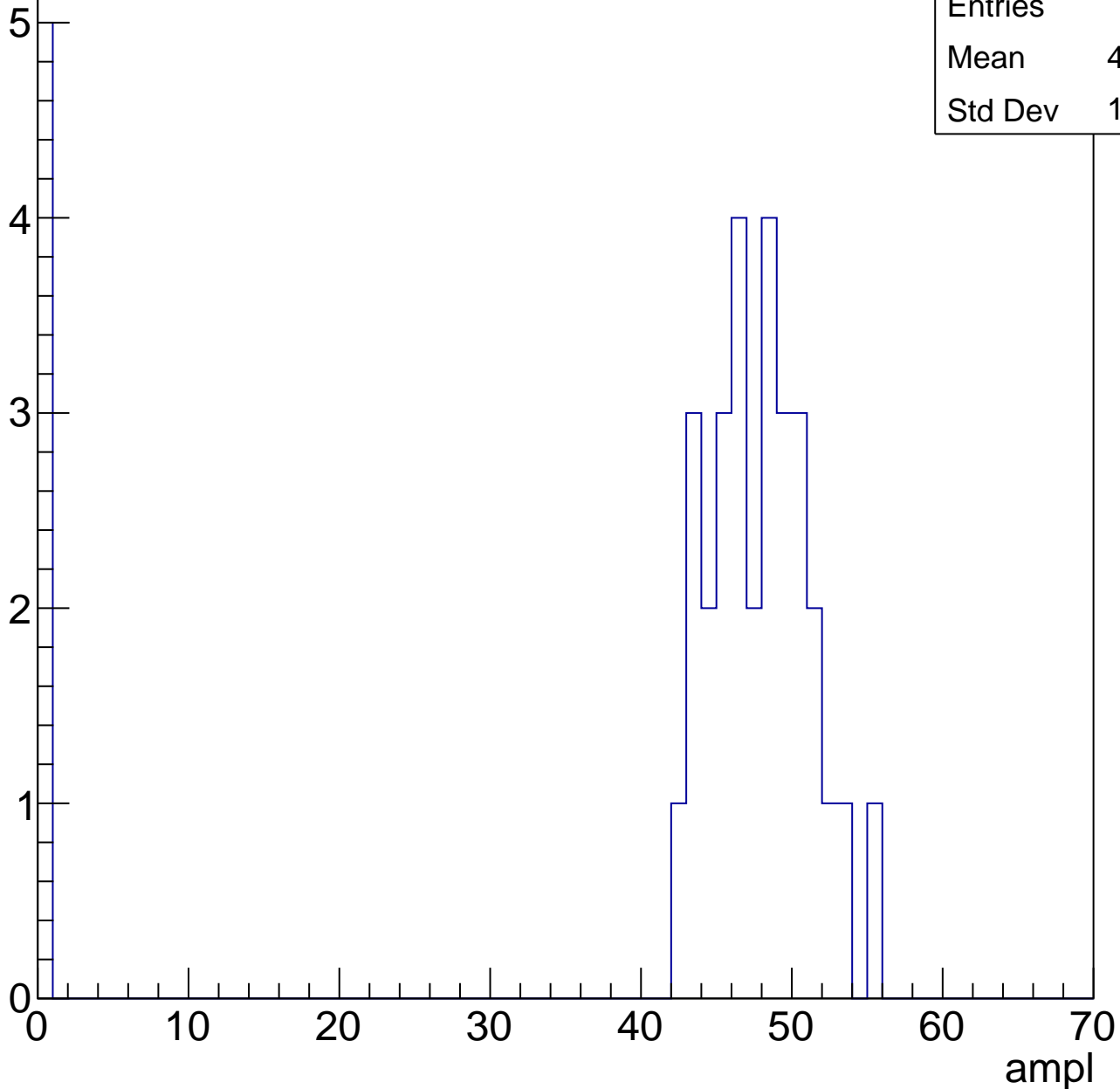
Entries	31
Mean	39
Std Dev	10.56

B1L103S, U14-ch83, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	35
Mean	40.66
Std Dev	16.86



B1L103S, U14-ch83, adc4

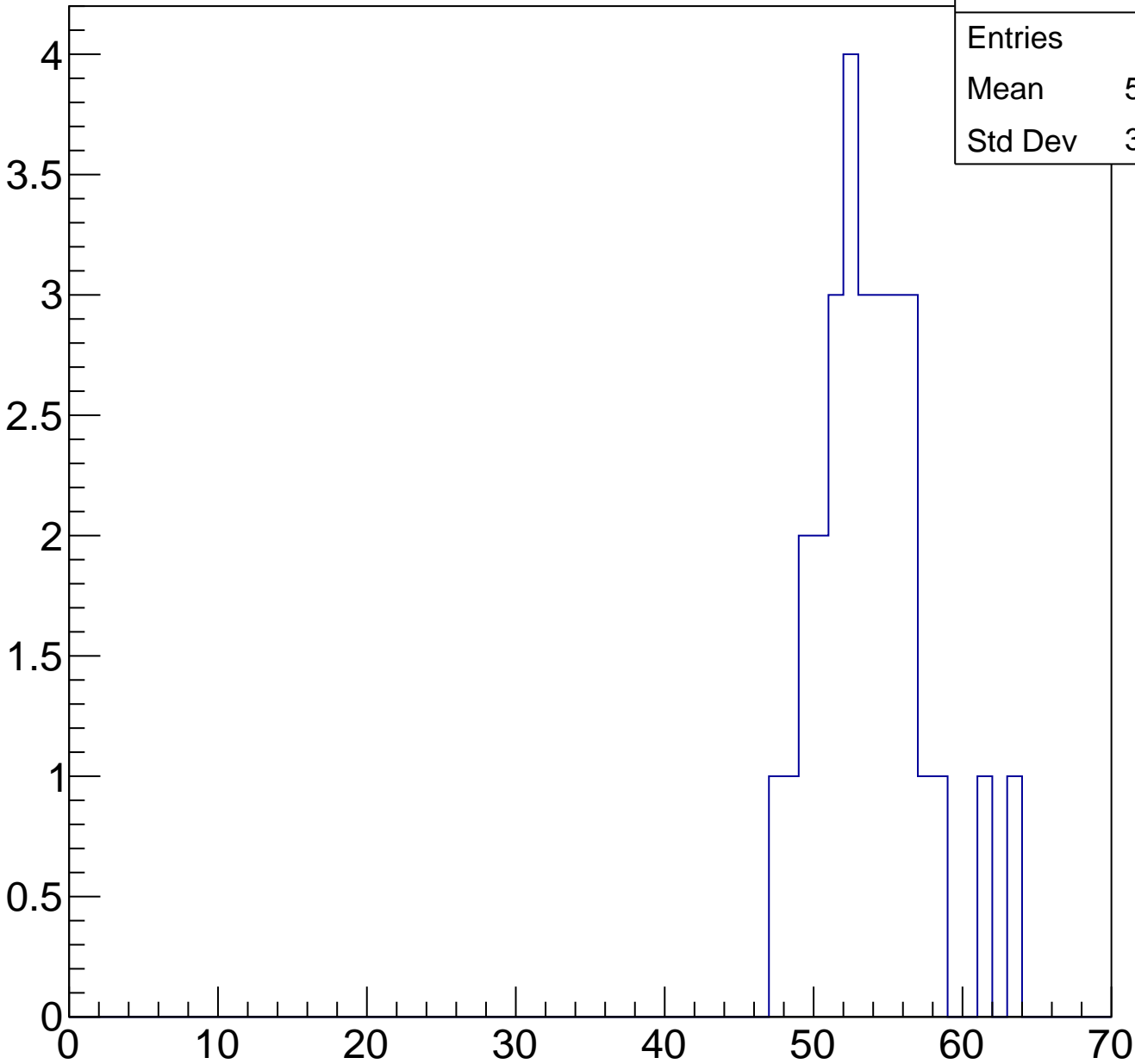
calib_packv5_041523_1651.root, FC#0, port C2

Entry

4
3.5
3
2.5
2
1.5
1
0.5
0

Entries	29
Mean	53.34
Std Dev	3.575

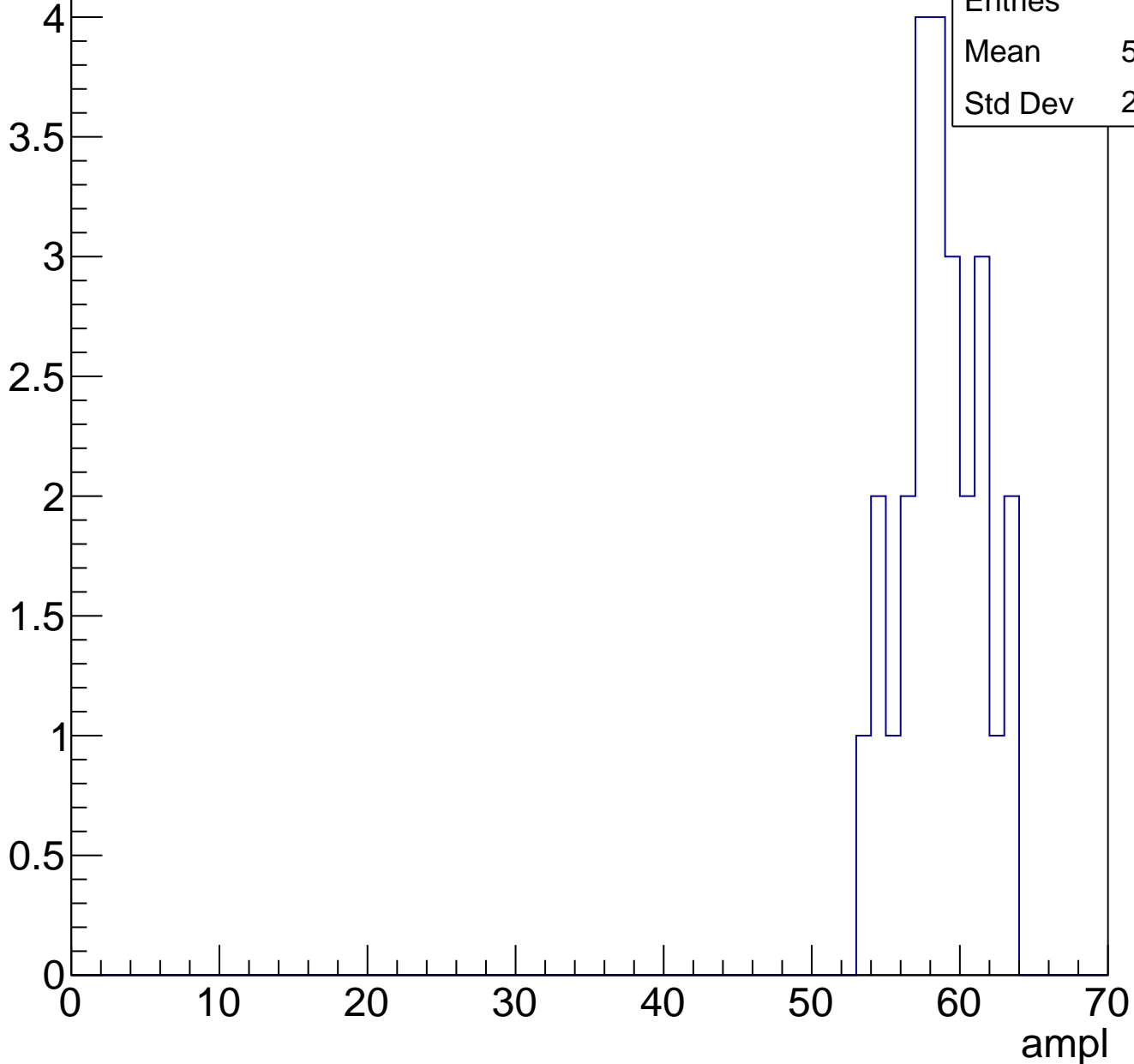
ampl



B1L103S, U14-ch83, adc5

calib_packv5_041523_1651.root, FC#0, port C2

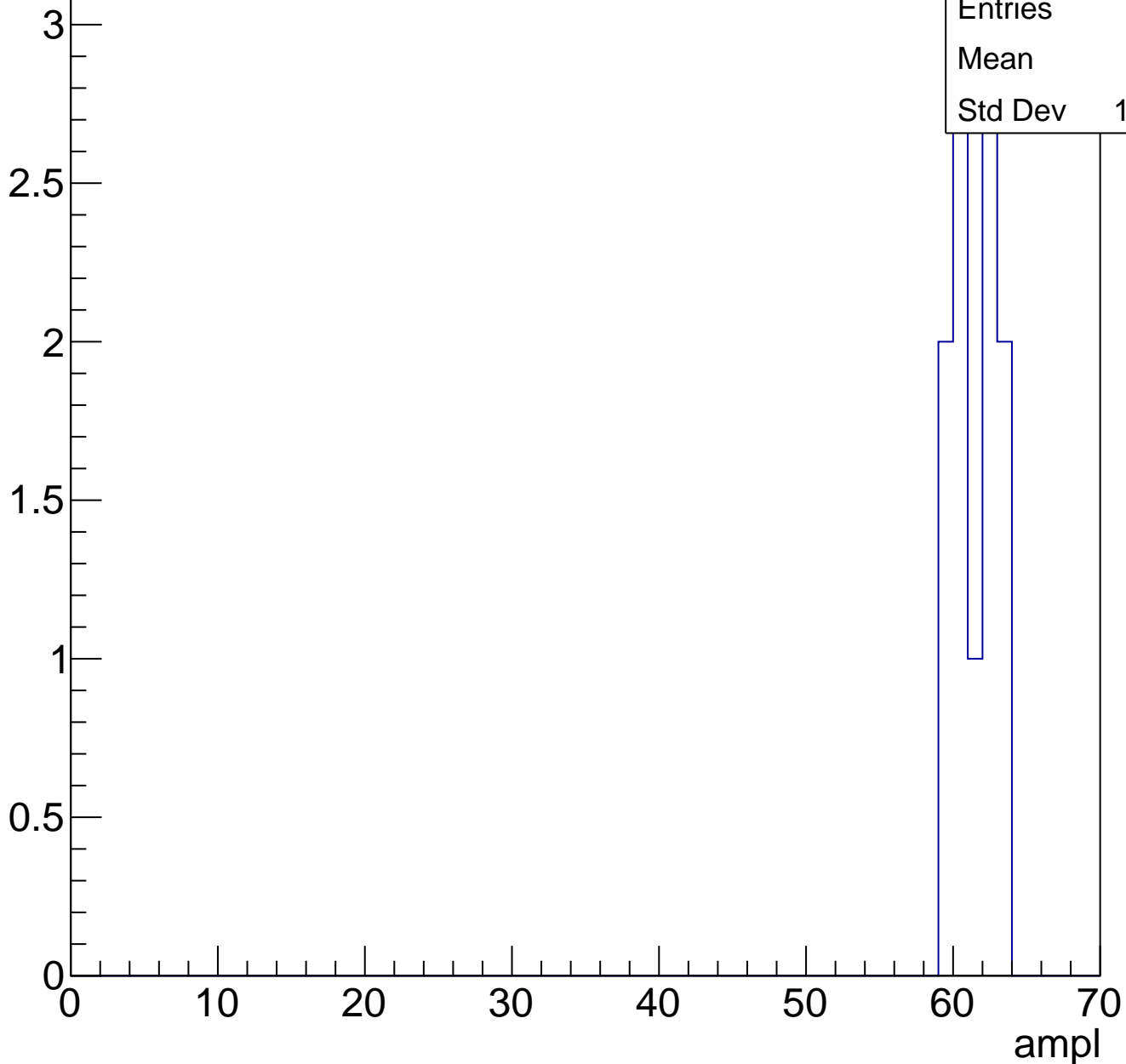
Entry



B1L103S, U14-ch83, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

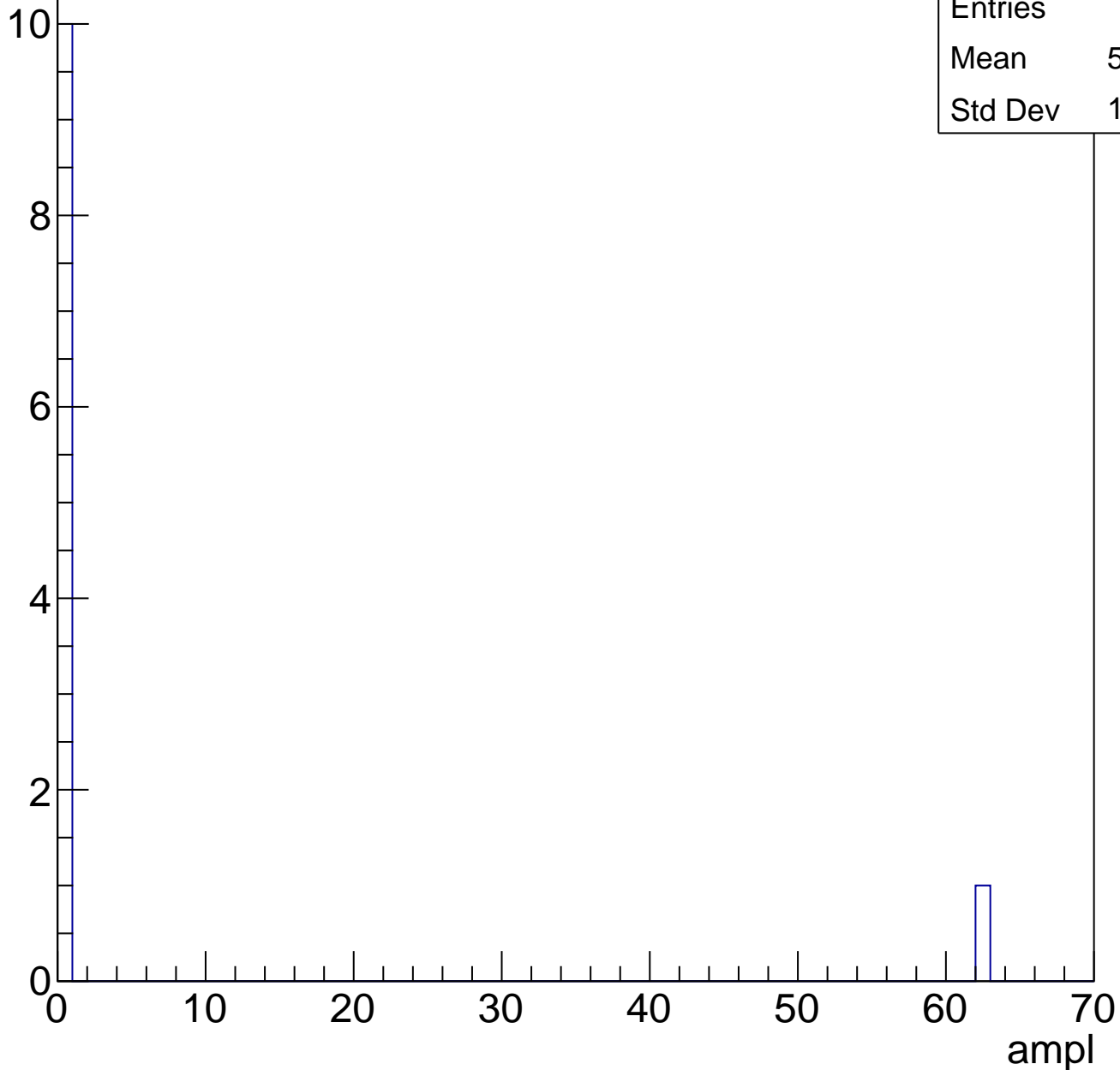


B1L103S, U14-ch83, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	11
Mean	5.636
Std Dev	17.82

Entry

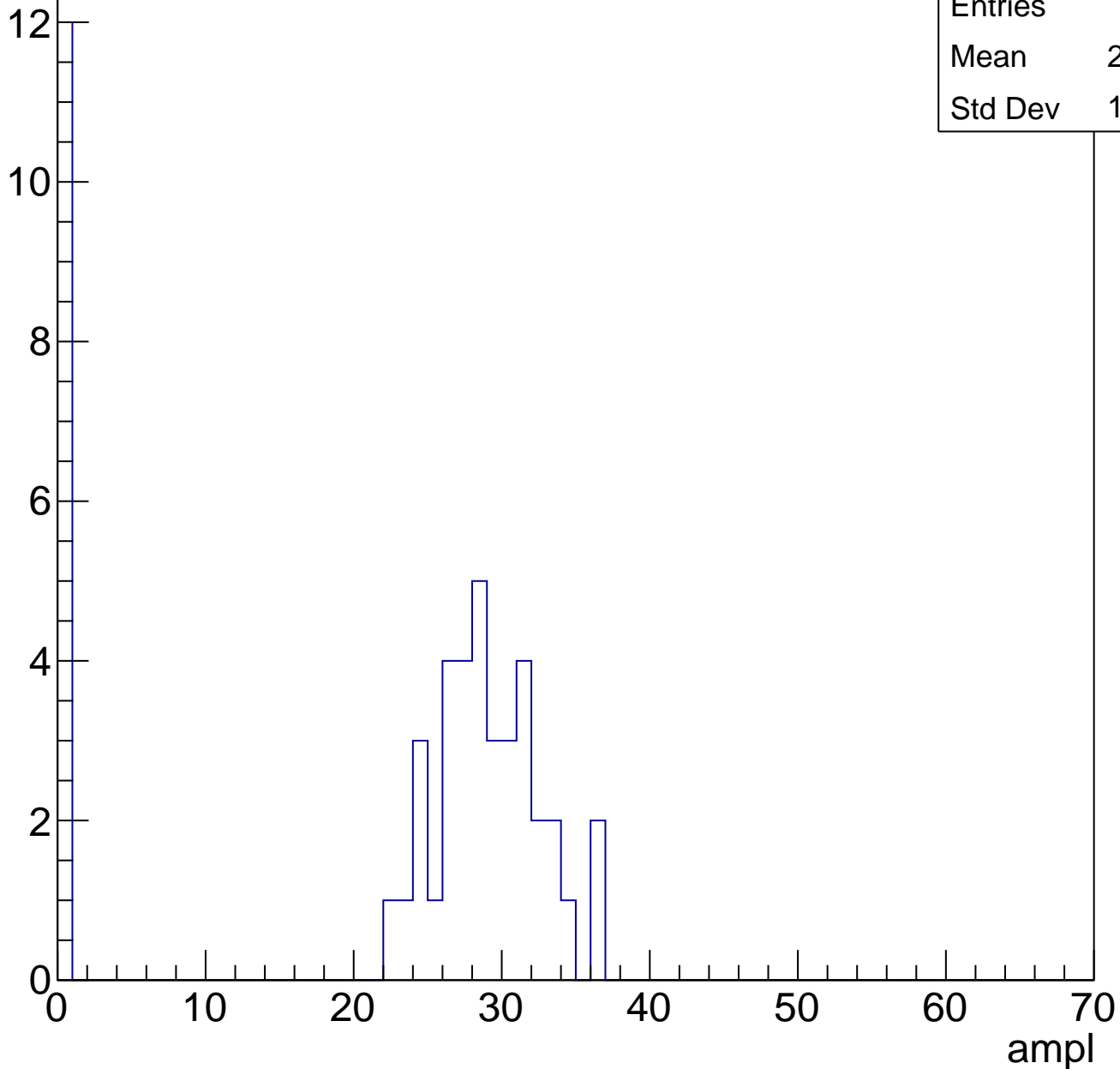


B1L103S, U14-ch84, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	48
Mean	21.48
Std Dev	12.75

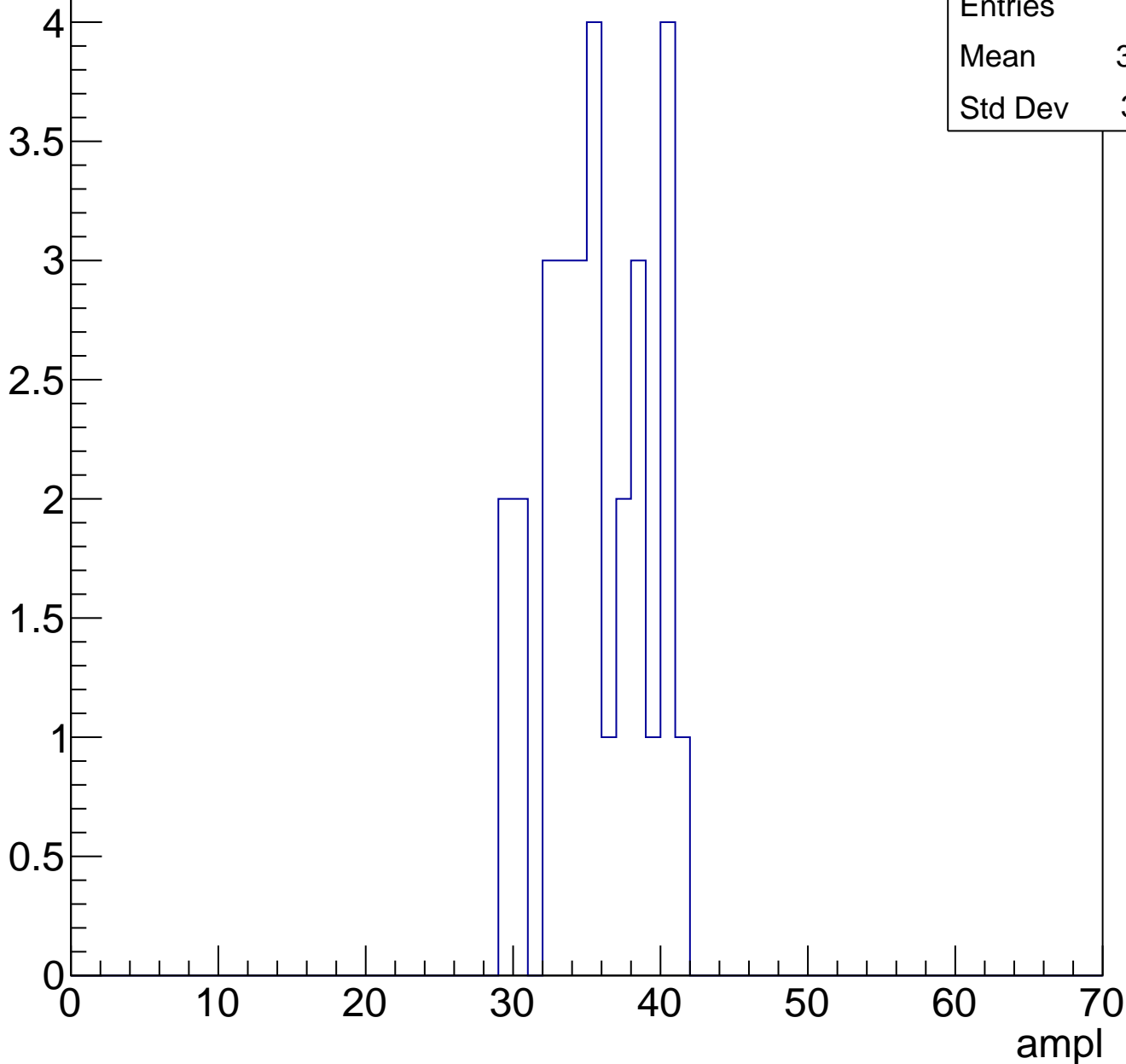
Entry



B1L103S, U14-ch84, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

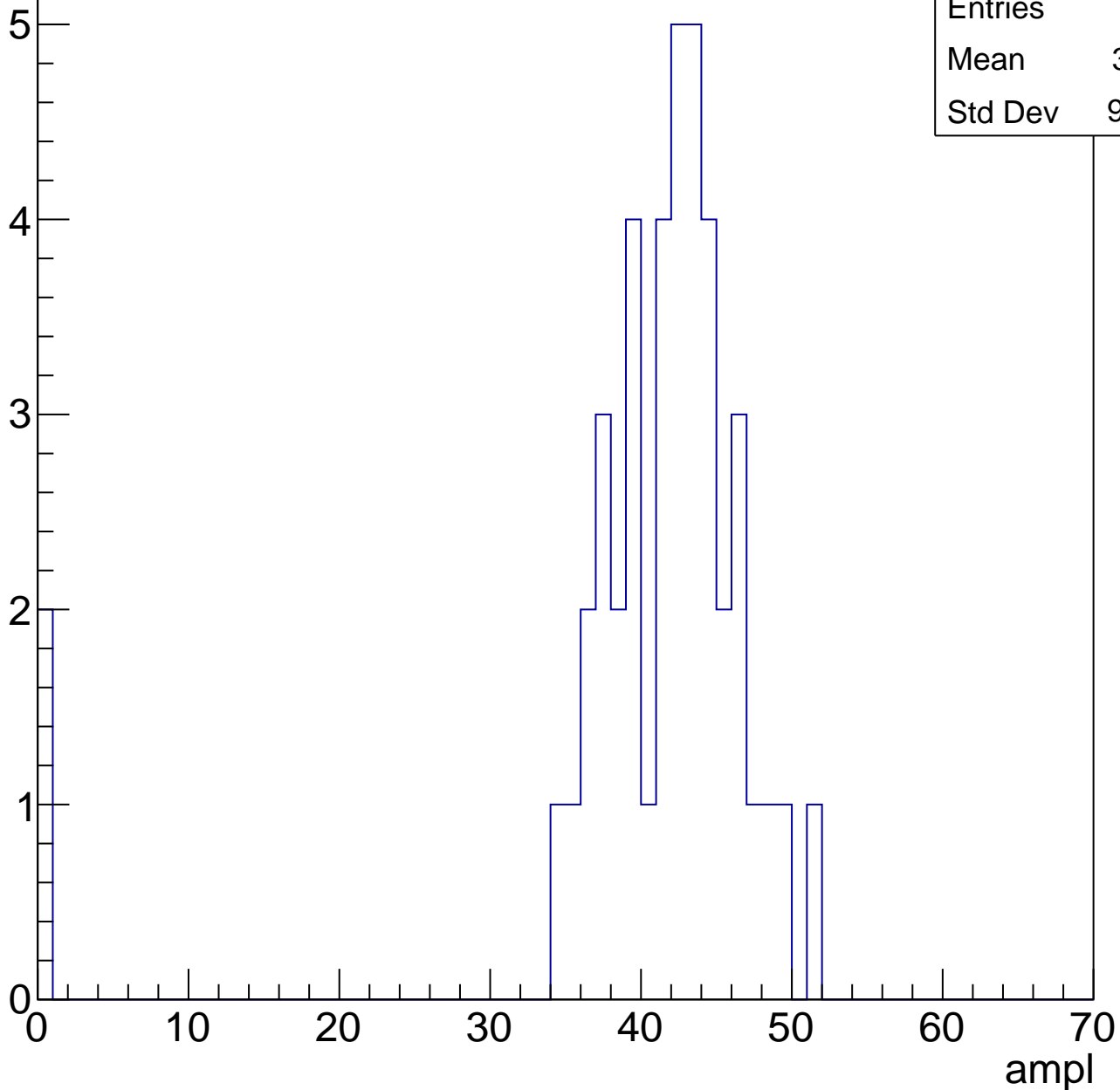


B1L103S, U14-ch84, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

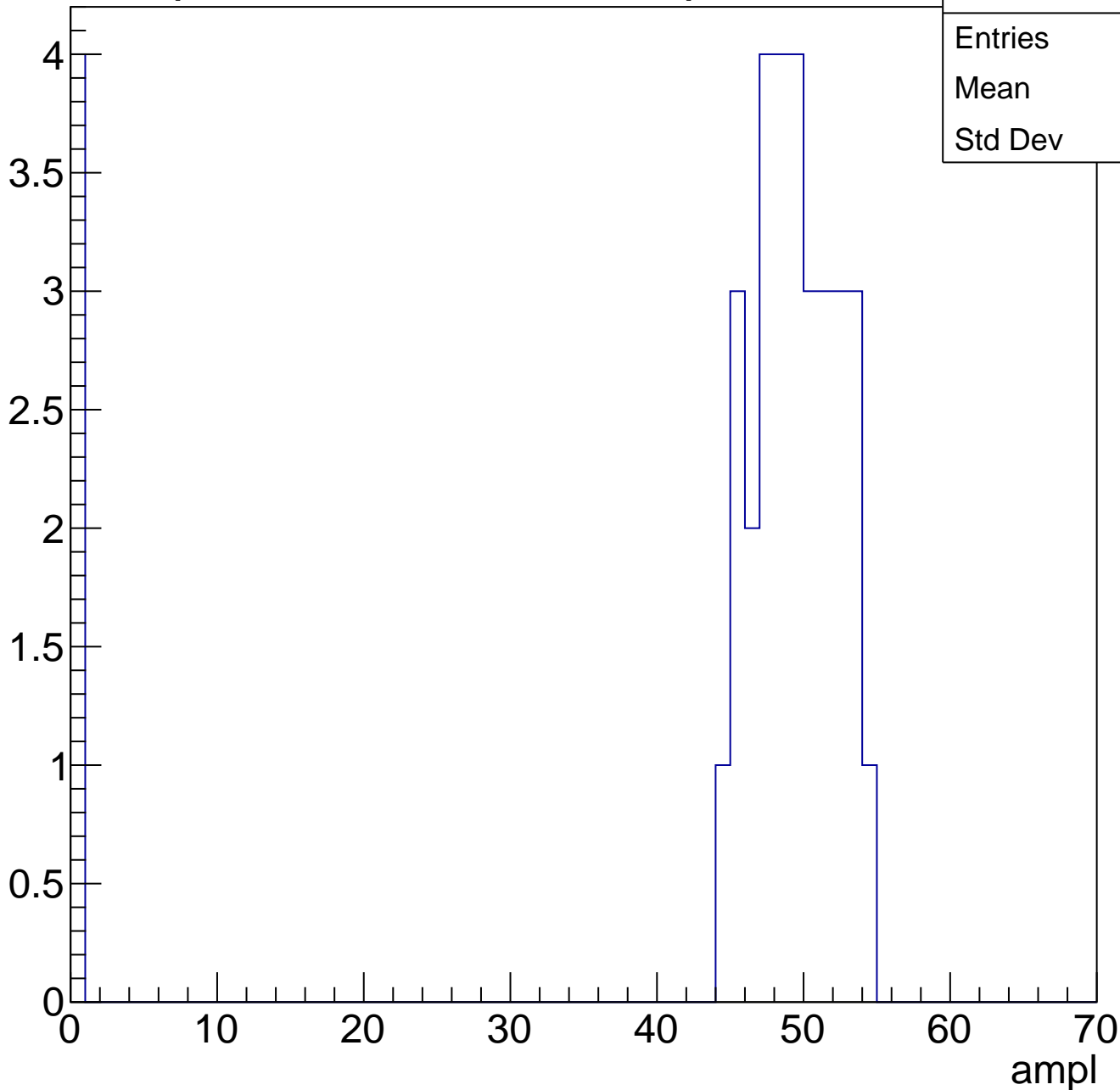
Entries	43
Mean	39.81
Std Dev	9.568



B1L103S, U14-ch84, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

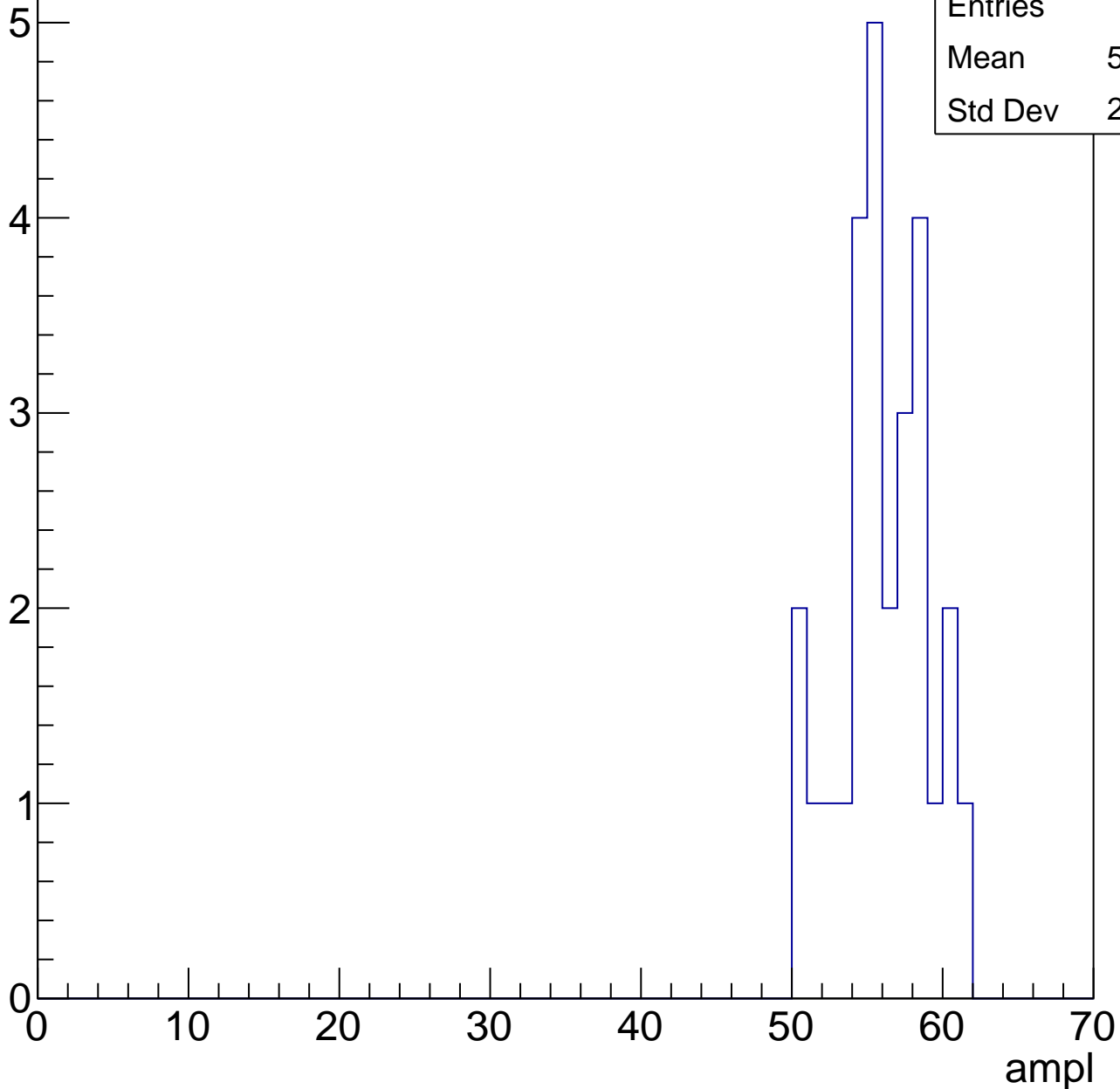


B1L103S, U14-ch84, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

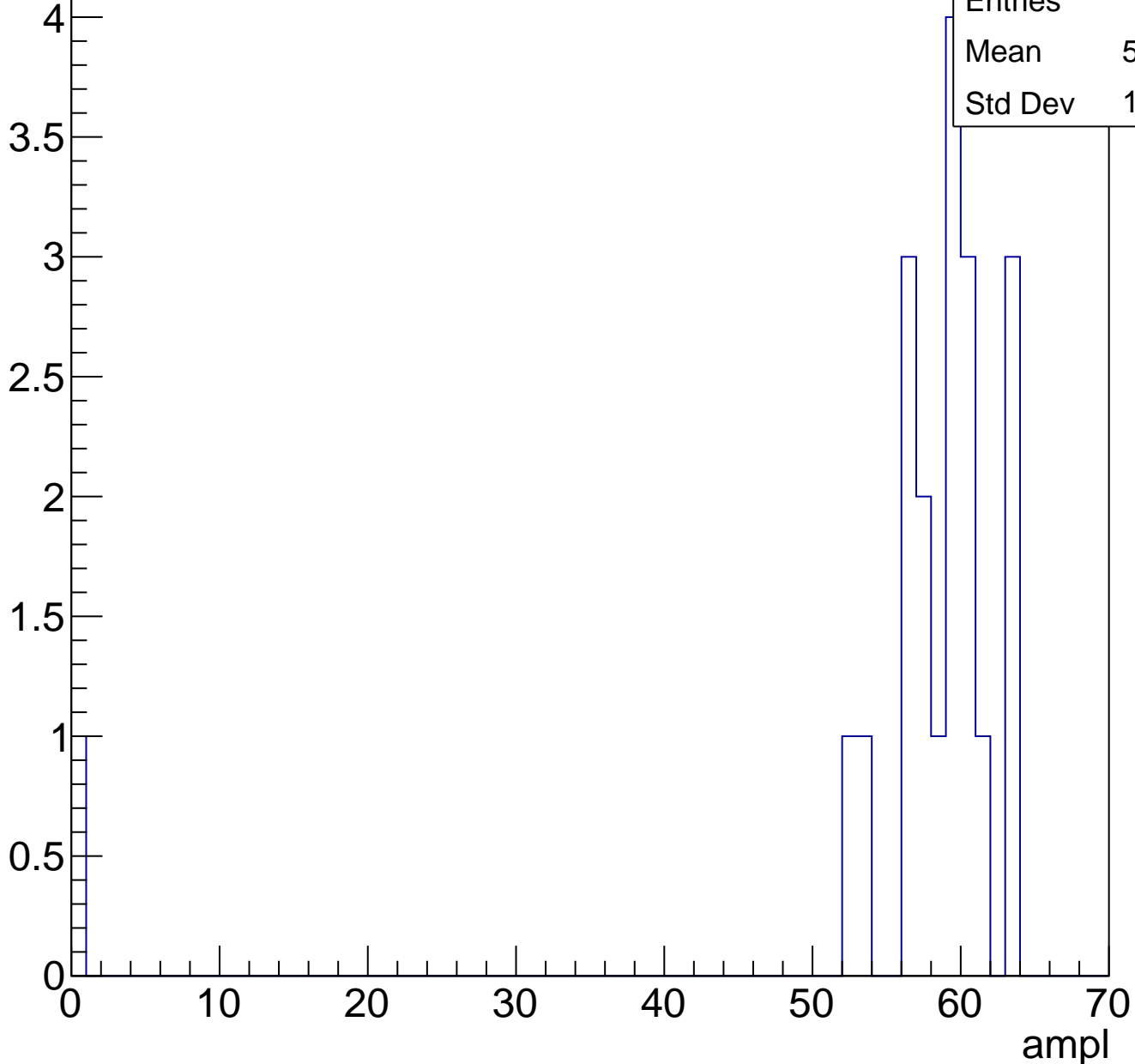
Entries	27
Mean	55.63
Std Dev	2.882



B1L103S, U14-ch84, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

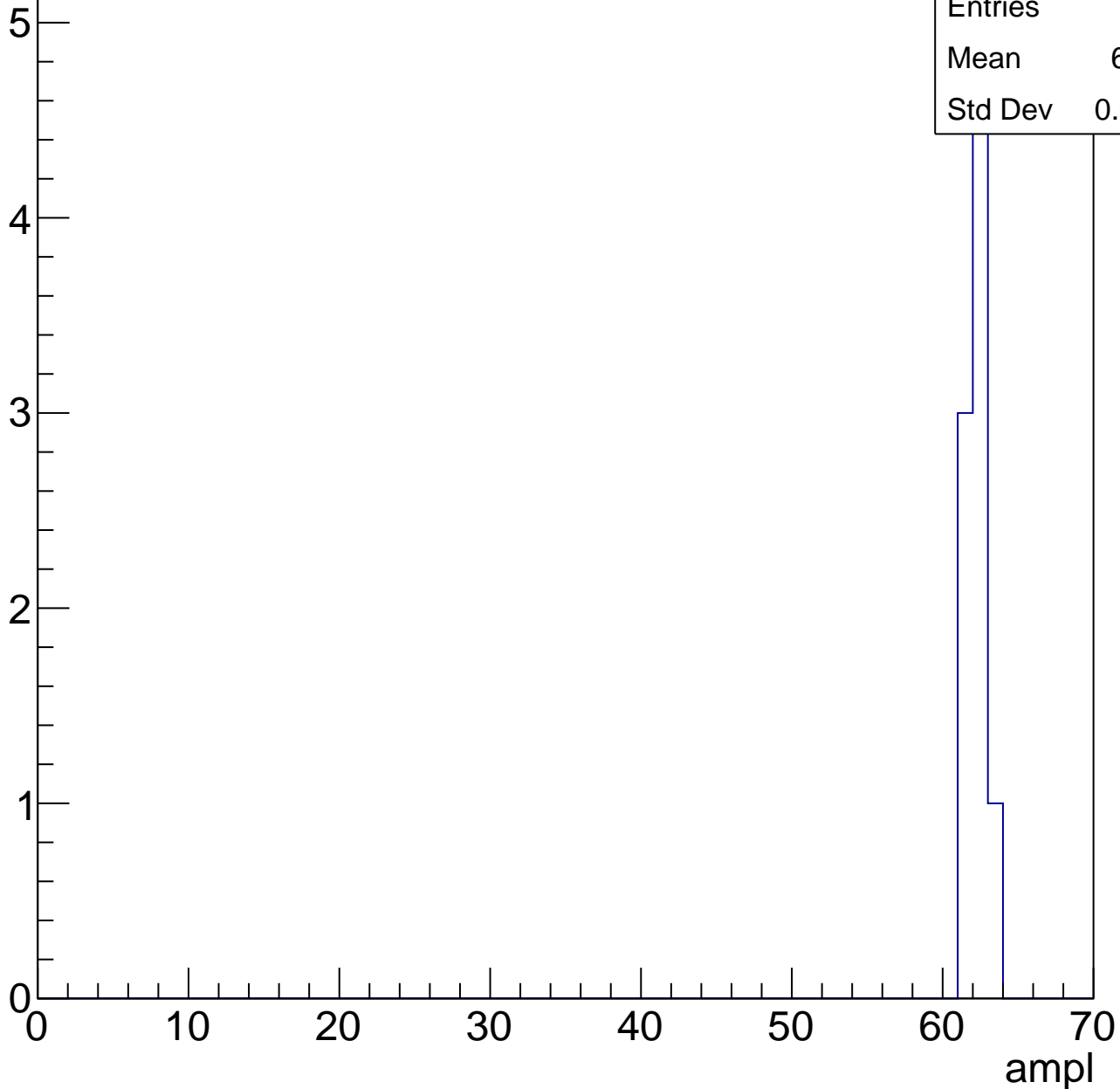


B1L103S, U14-ch84, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	9
Mean	61.78
Std Dev	0.6285



B1L103S, U14-ch84, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	12
Mean	5.25
Std Dev	17.41

Entry

10

8

6

4

2

0

0

10

20

30

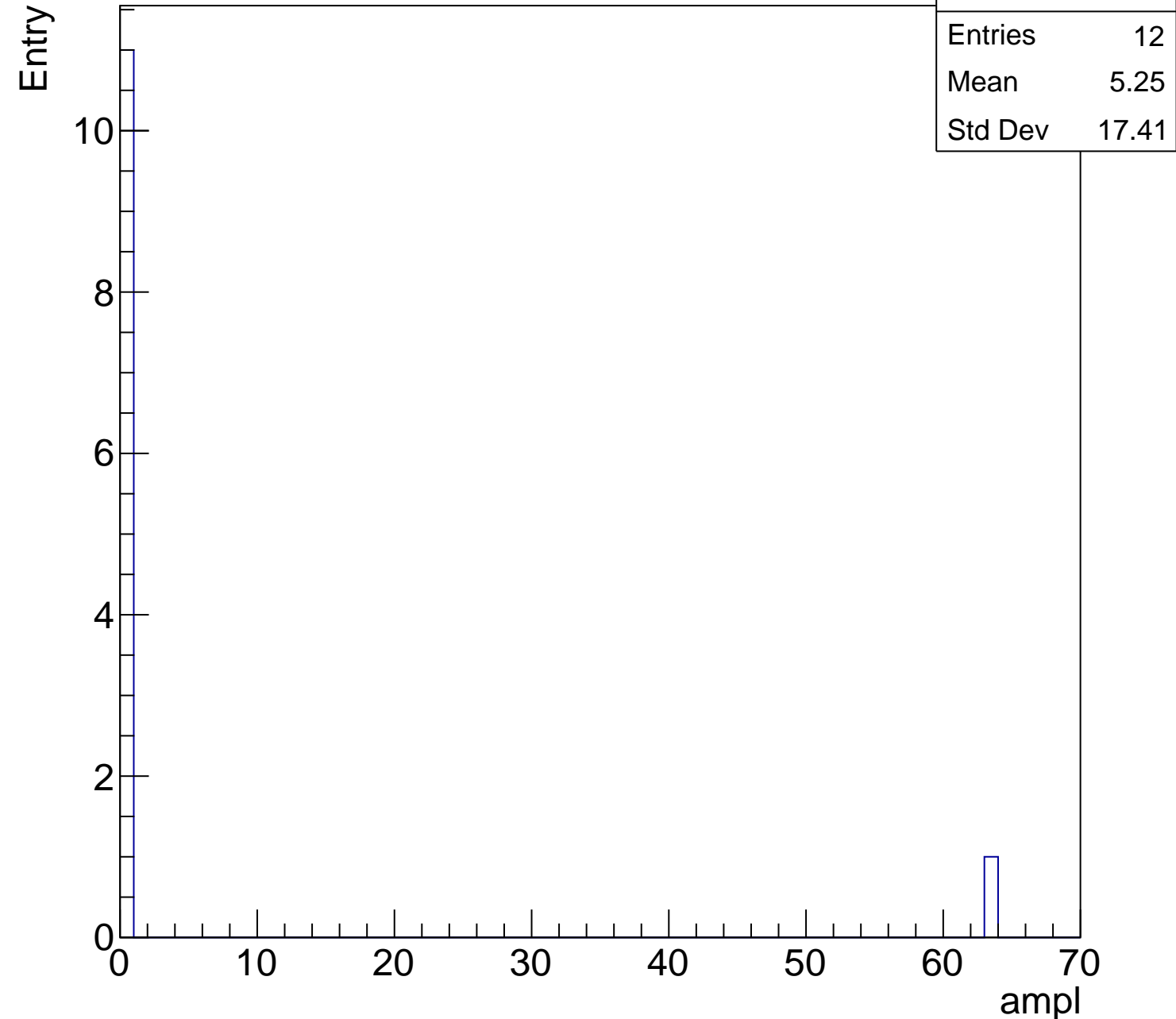
40

50

60

ampl

70

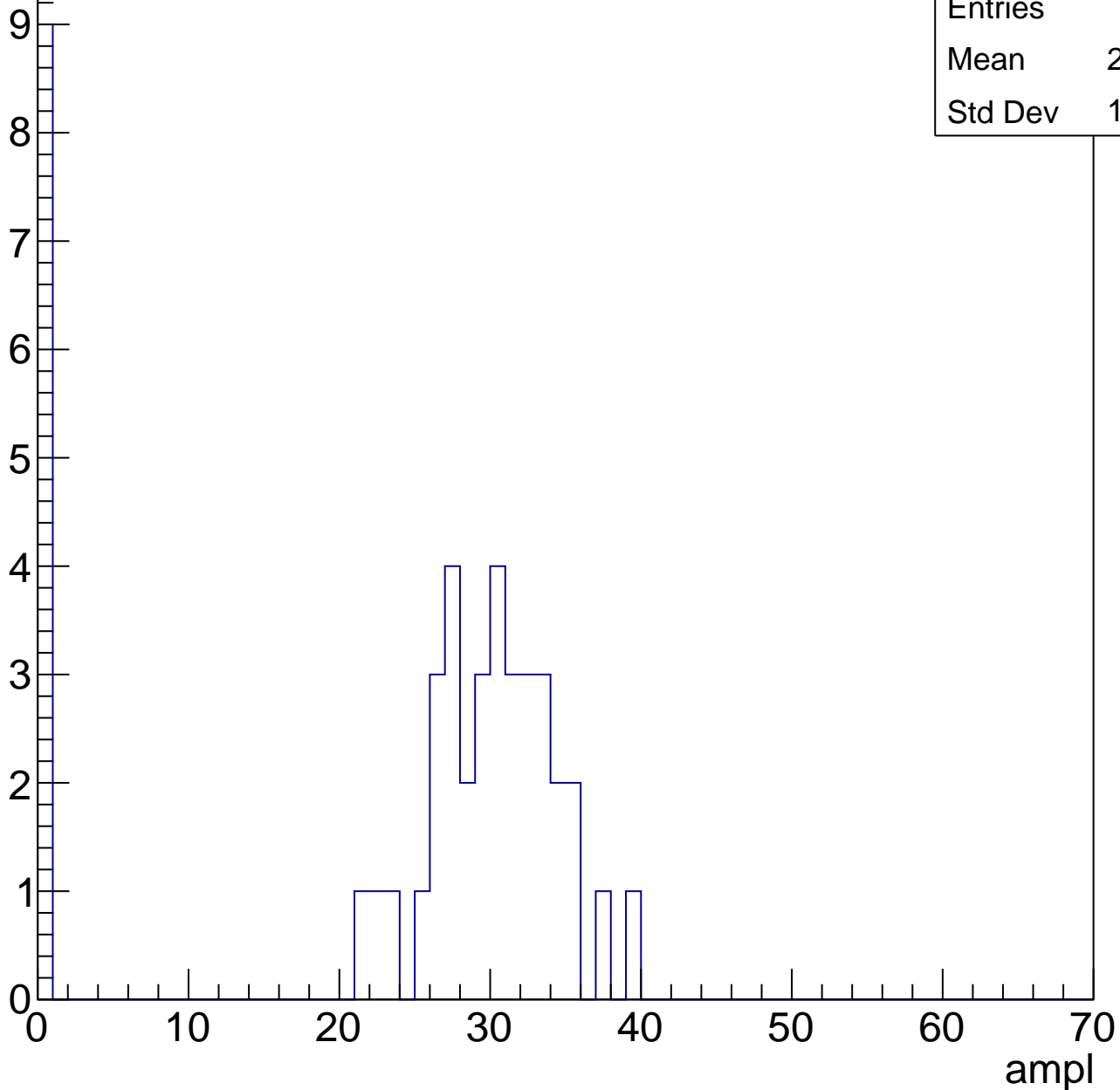


B1L103S, U14-ch85, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	44
Mean	23.68
Std Dev	12.53

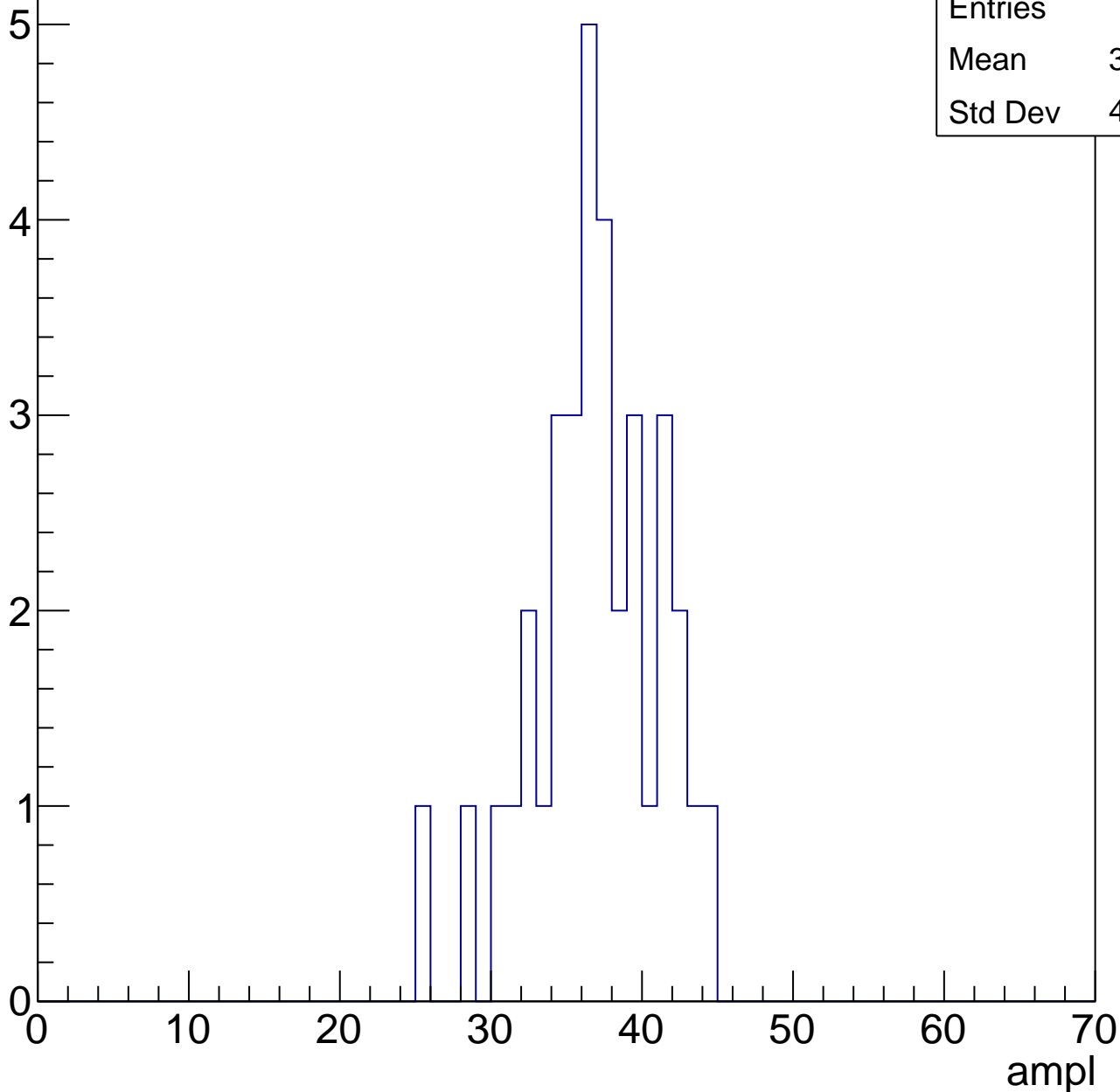


B1L103S, U14-ch85, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

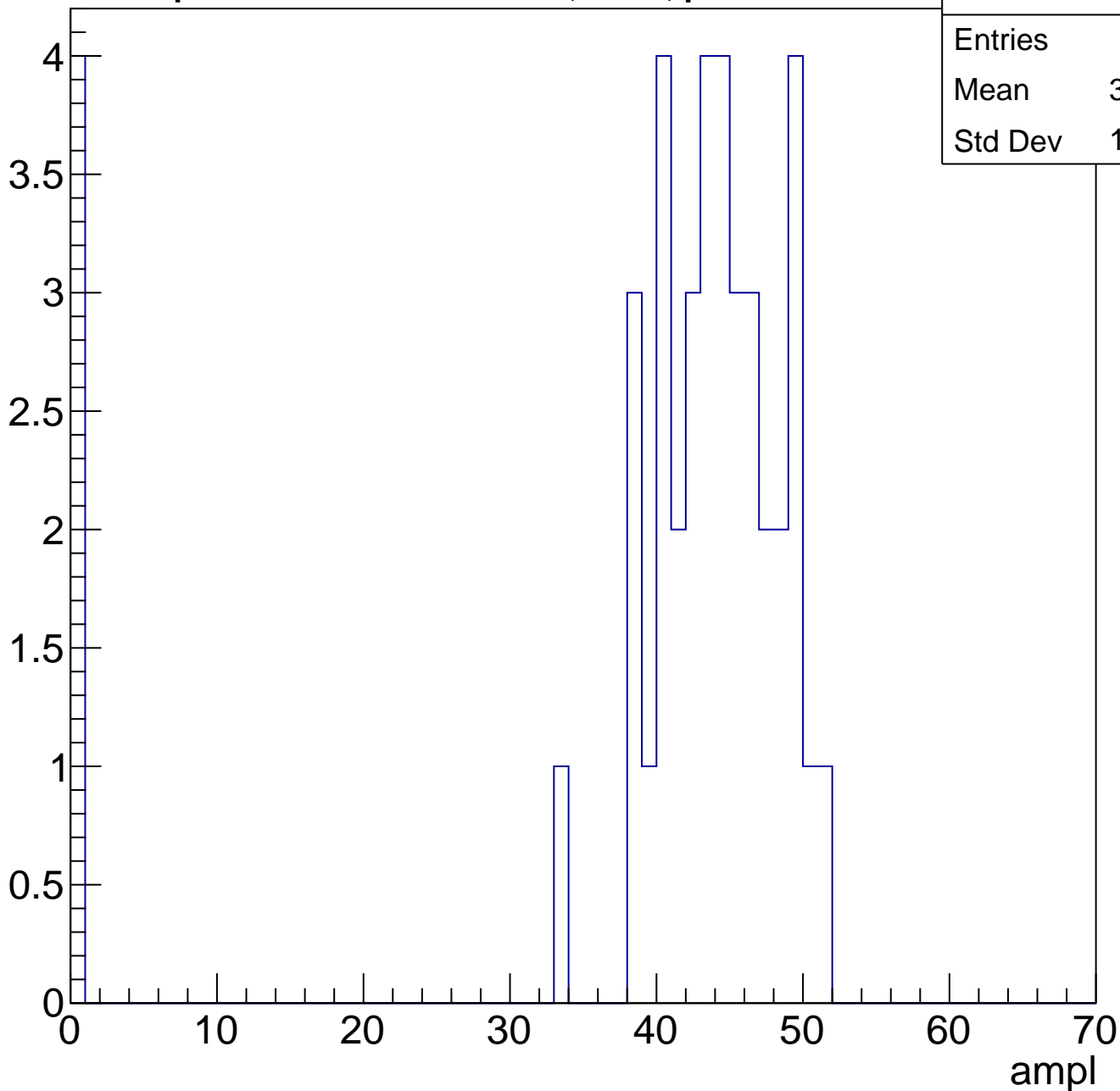
Entries	35
Mean	36.37
Std Dev	4.182



B1L103S, U14-ch85, adc2

calib_packv5_041523_1651.root, FC#0, port C2

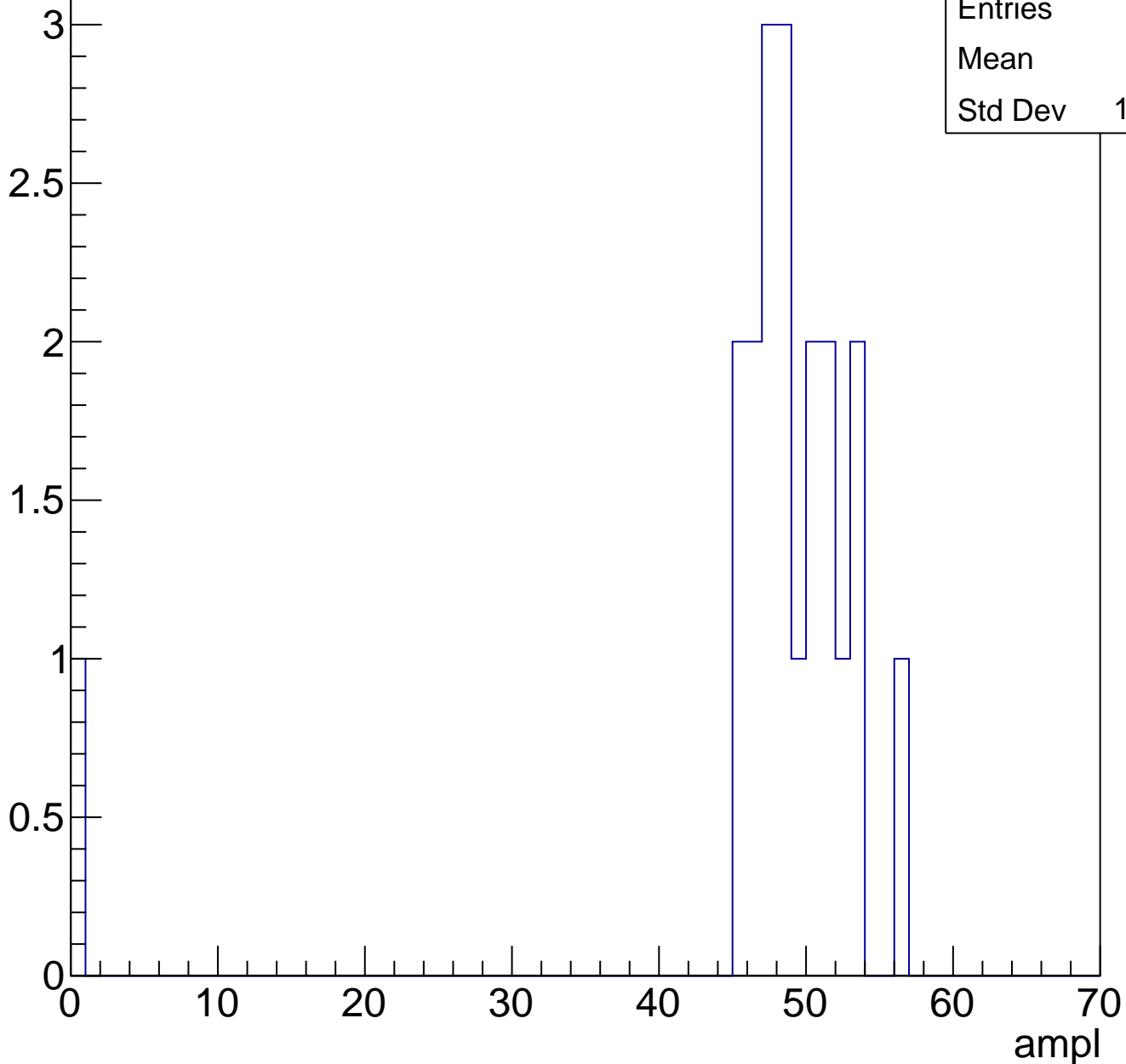
Entry



B1L103S, U14-ch85, adc3

calib_packv5_041523_1651.root, FC#0, port C2

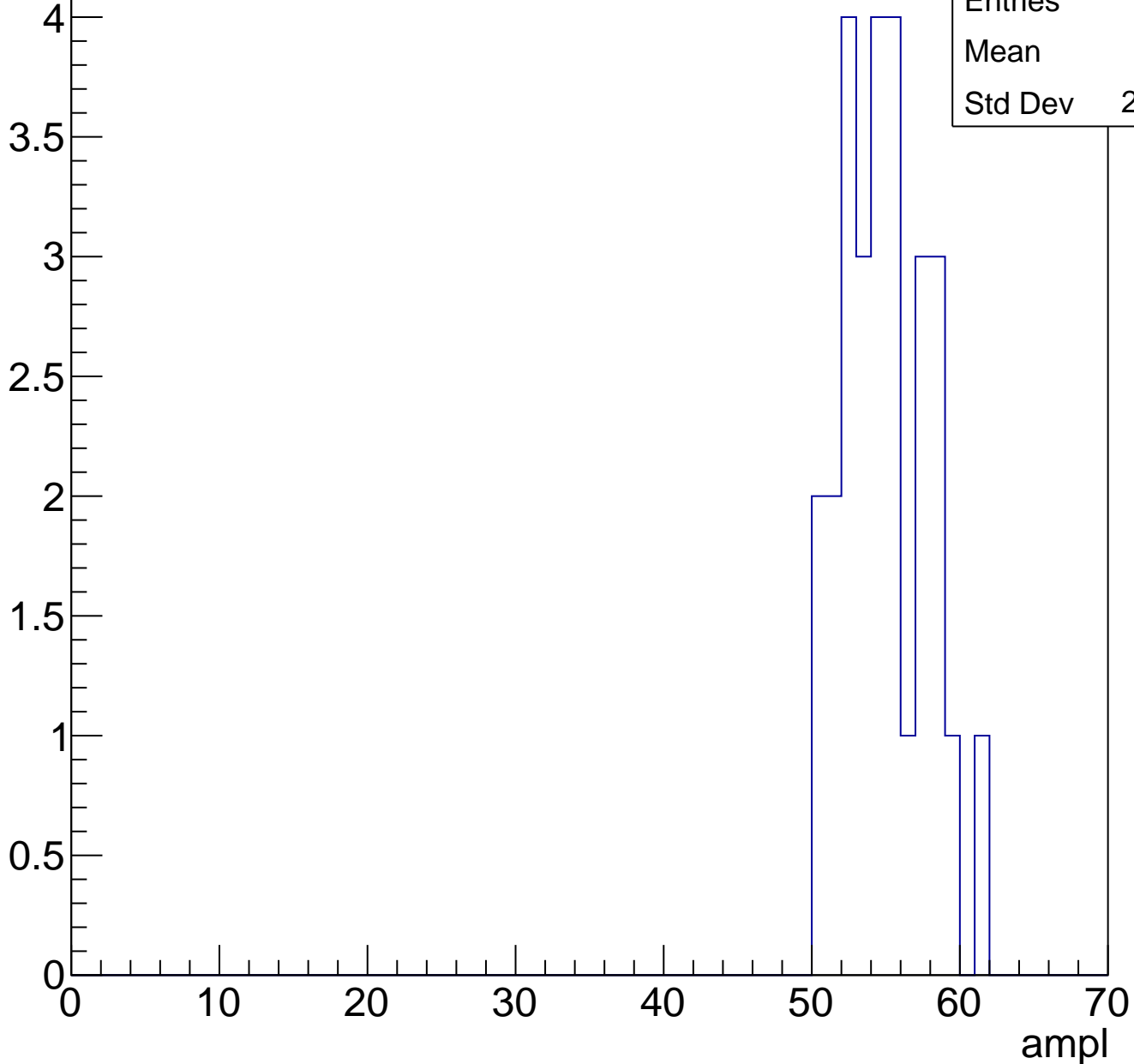
Entry



B1L103S, U14-ch85, adc4

calib_packv5_041523_1651.root, FC#0, port C2

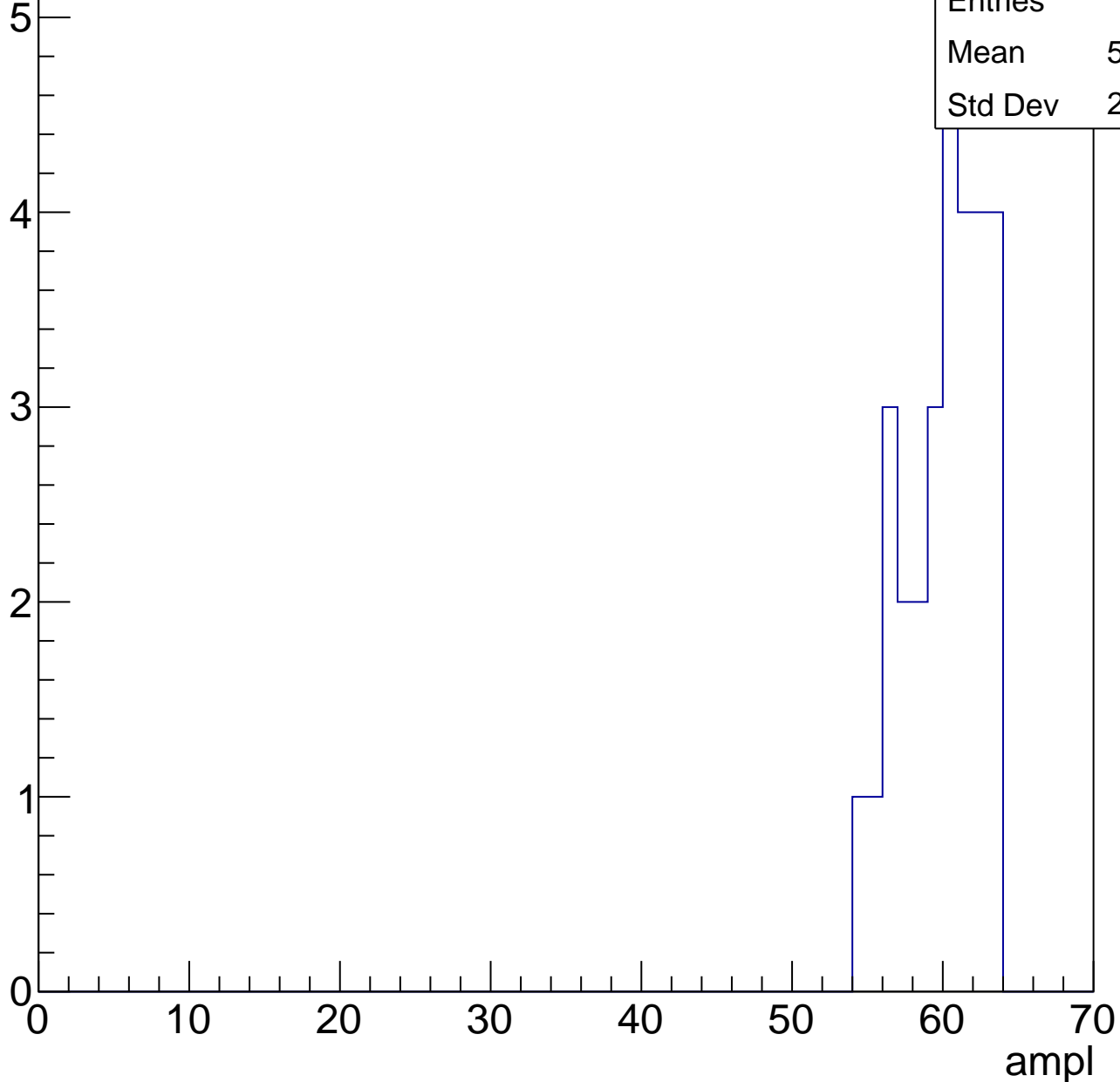
Entry



B1L103S, U14-ch85, adc5

calib_packv5_041523_1651.root, FC#0, port C2

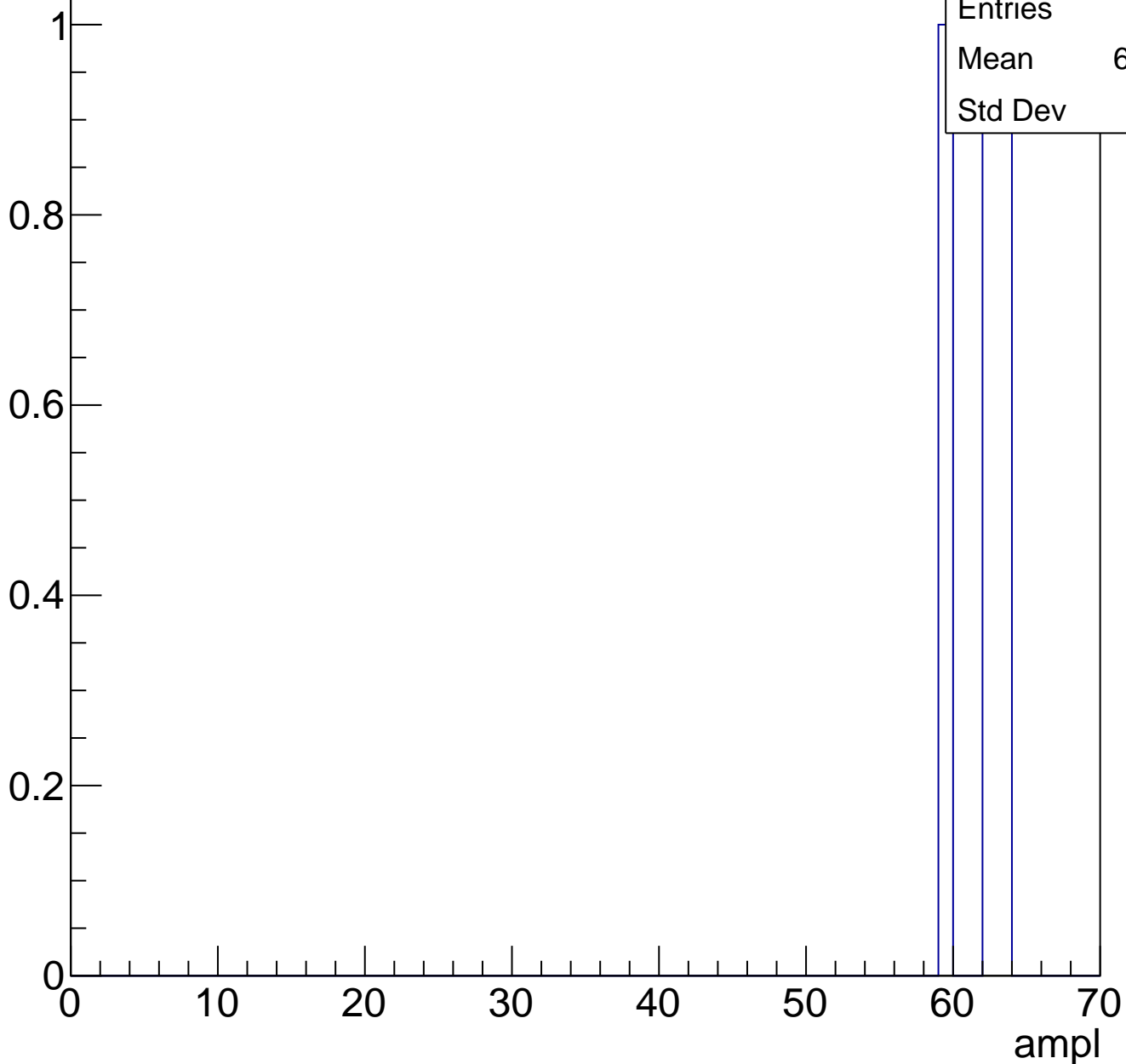
Entry



B1L103S, U14-ch85, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch85, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

12

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

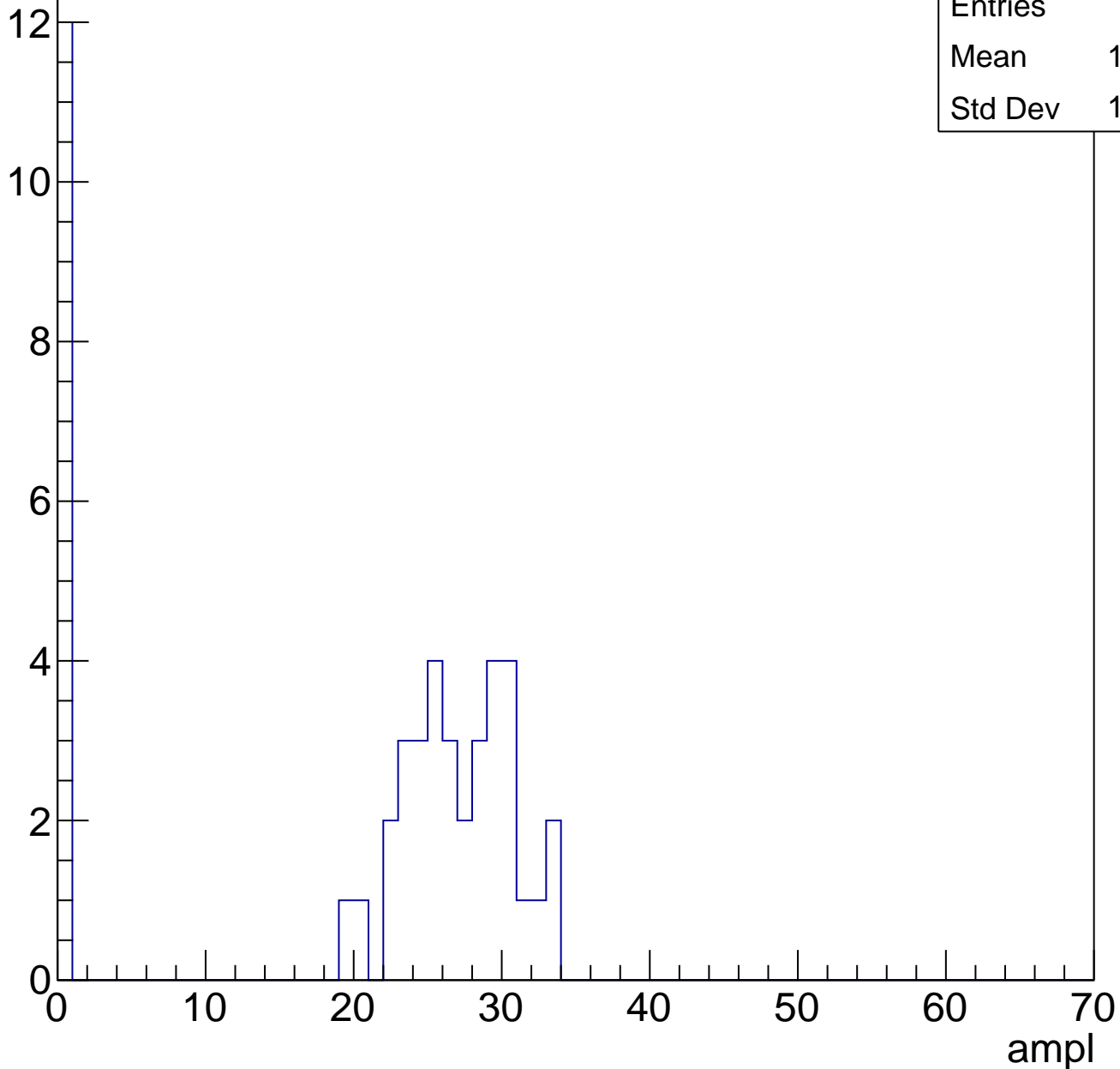
Entries	12
Mean	0
Std Dev	0

B1L103S, U14-ch86, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	46
Mean	19.67
Std Dev	12.07

Entry

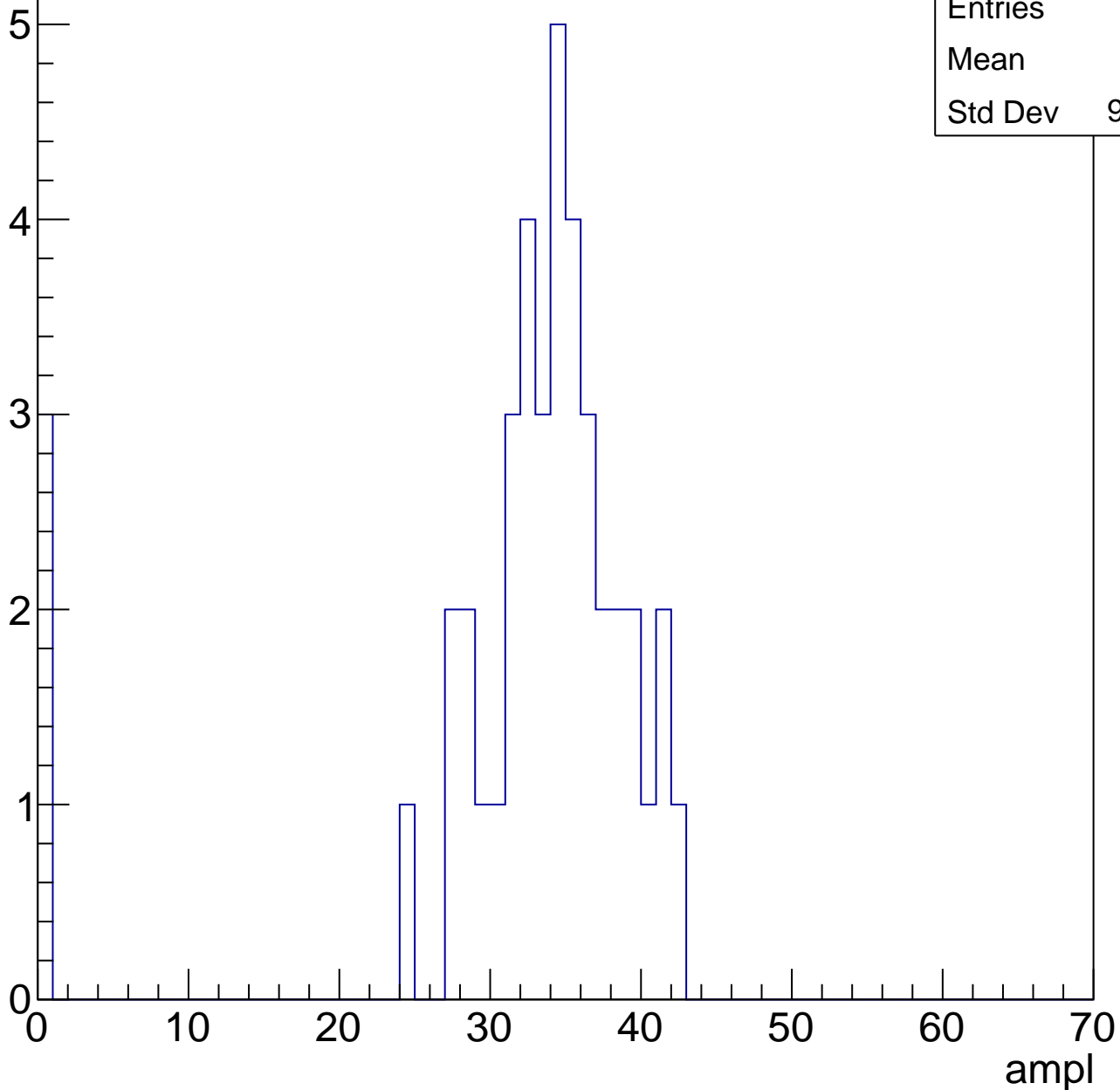


B1L103S, U14-ch86, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	42
Mean	31.5
Std Dev	9.607

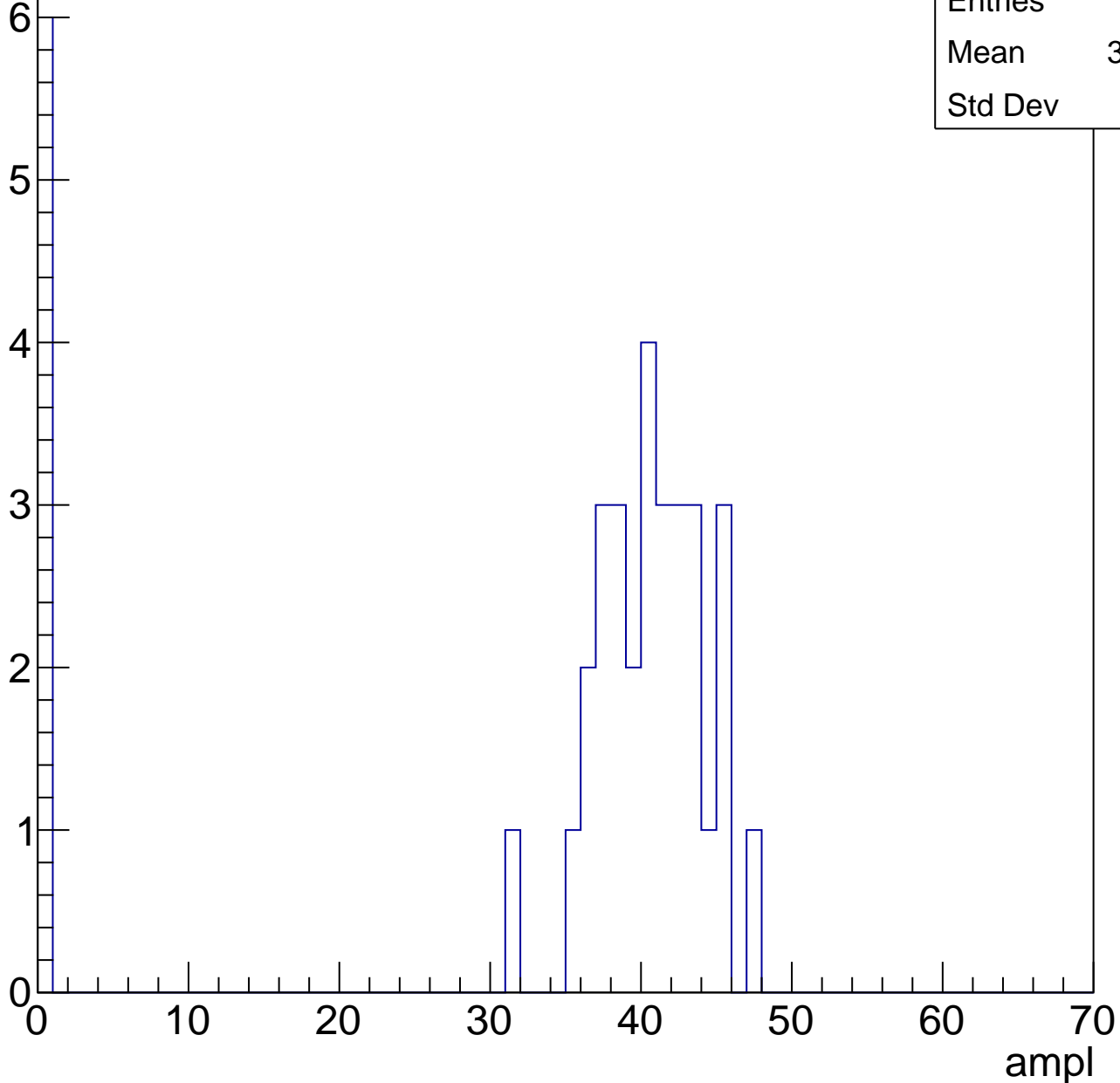


B1L103S, U14-ch86, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	36
Mean	33.47
Std Dev	15.3

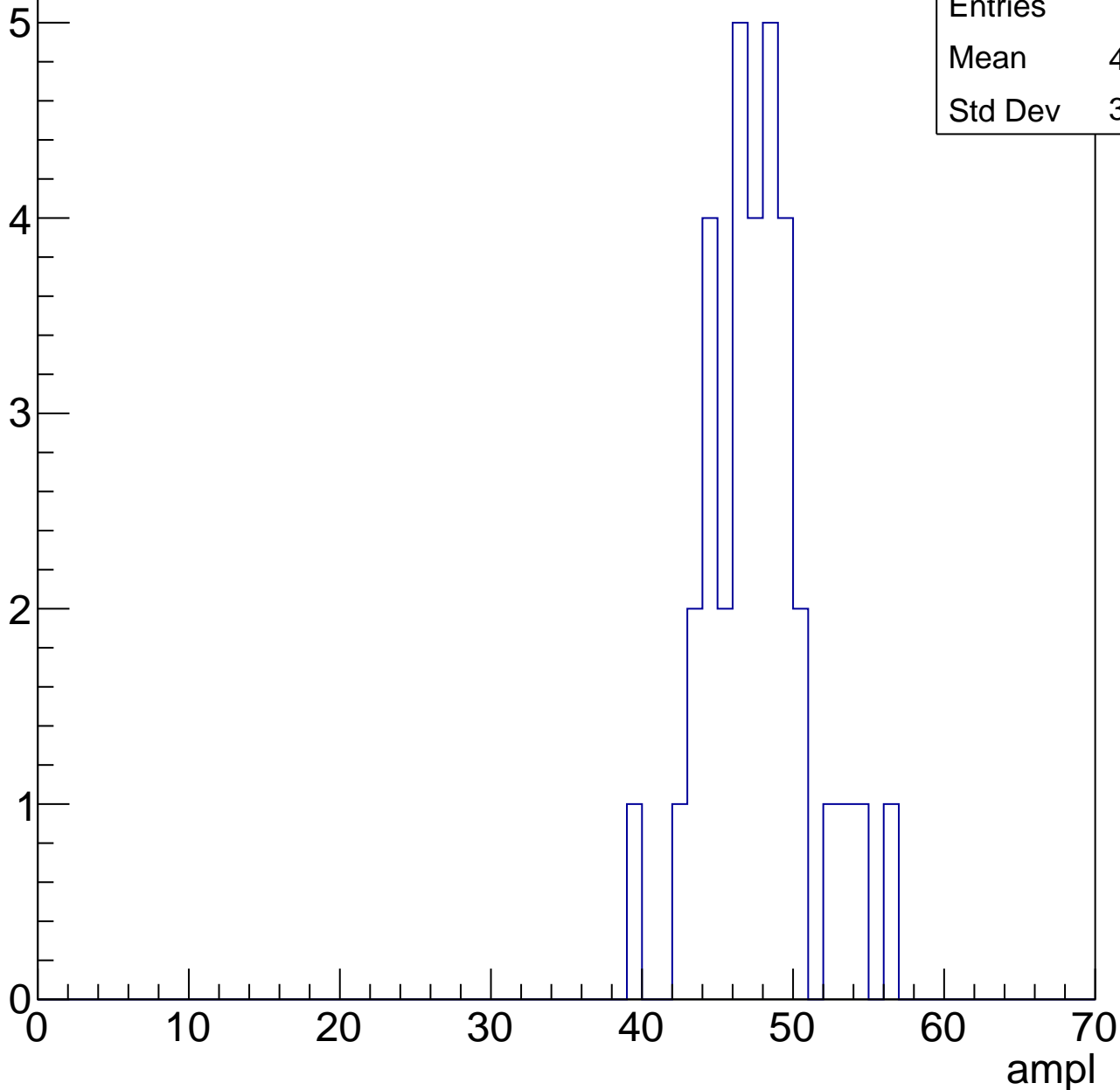


B1L103S, U14-ch86, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	34
Mean	47.12
Std Dev	3.428

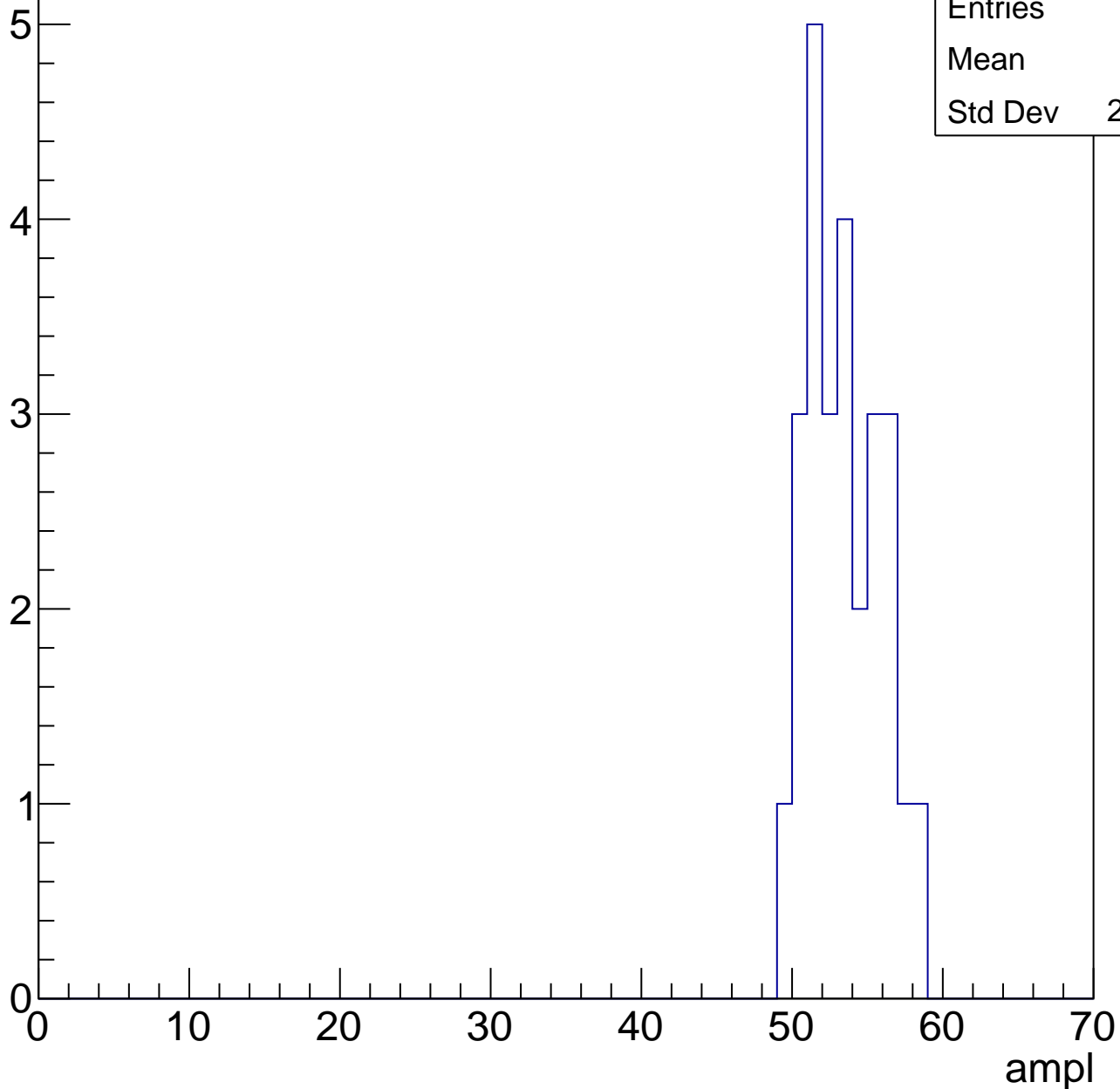


B1L103S, U14-ch86, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

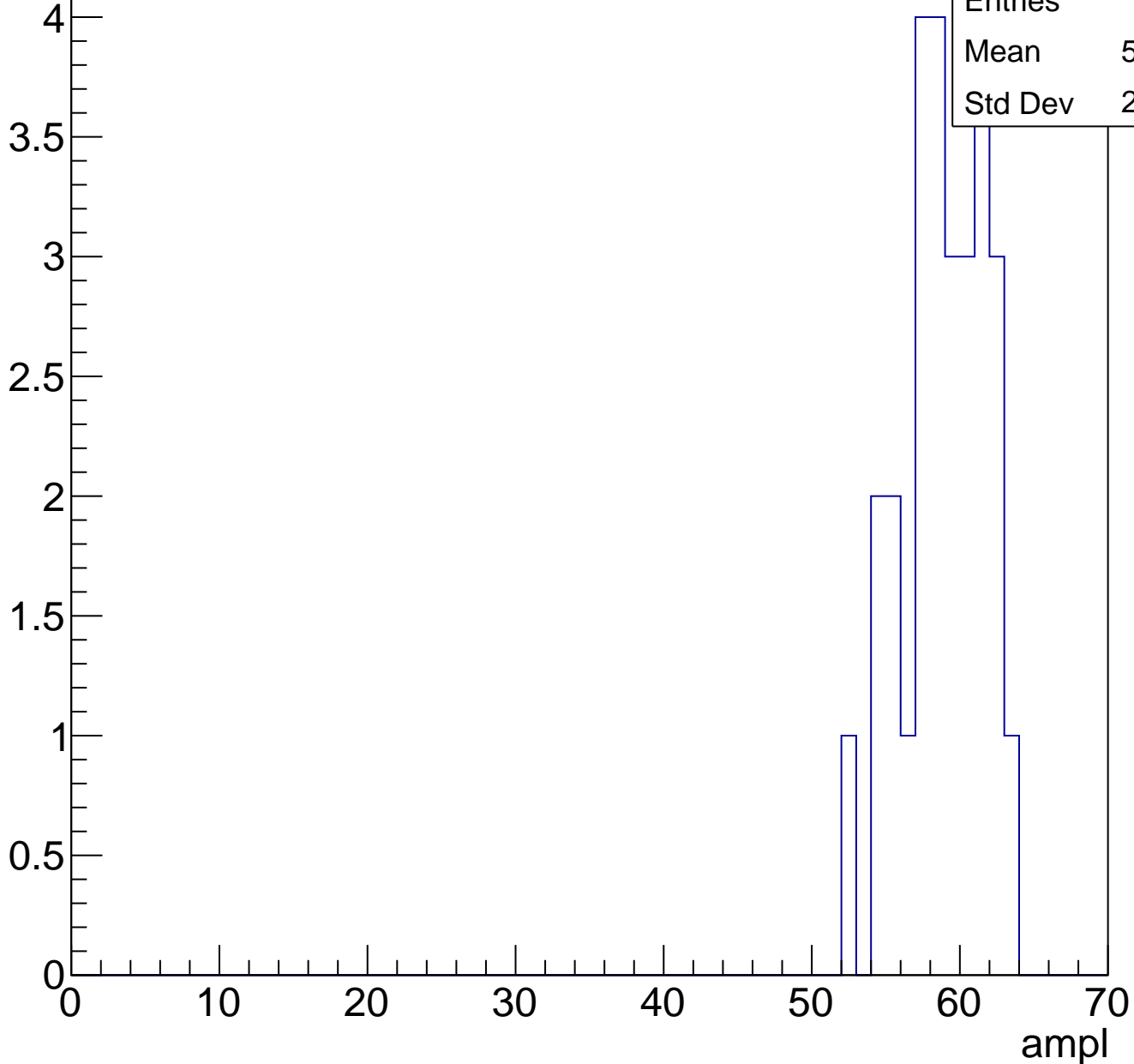
Entries	26
Mean	53
Std Dev	2.386



B1L103S, U14-ch86, adc5

calib_packv5_041523_1651.root, FC#0, port C2

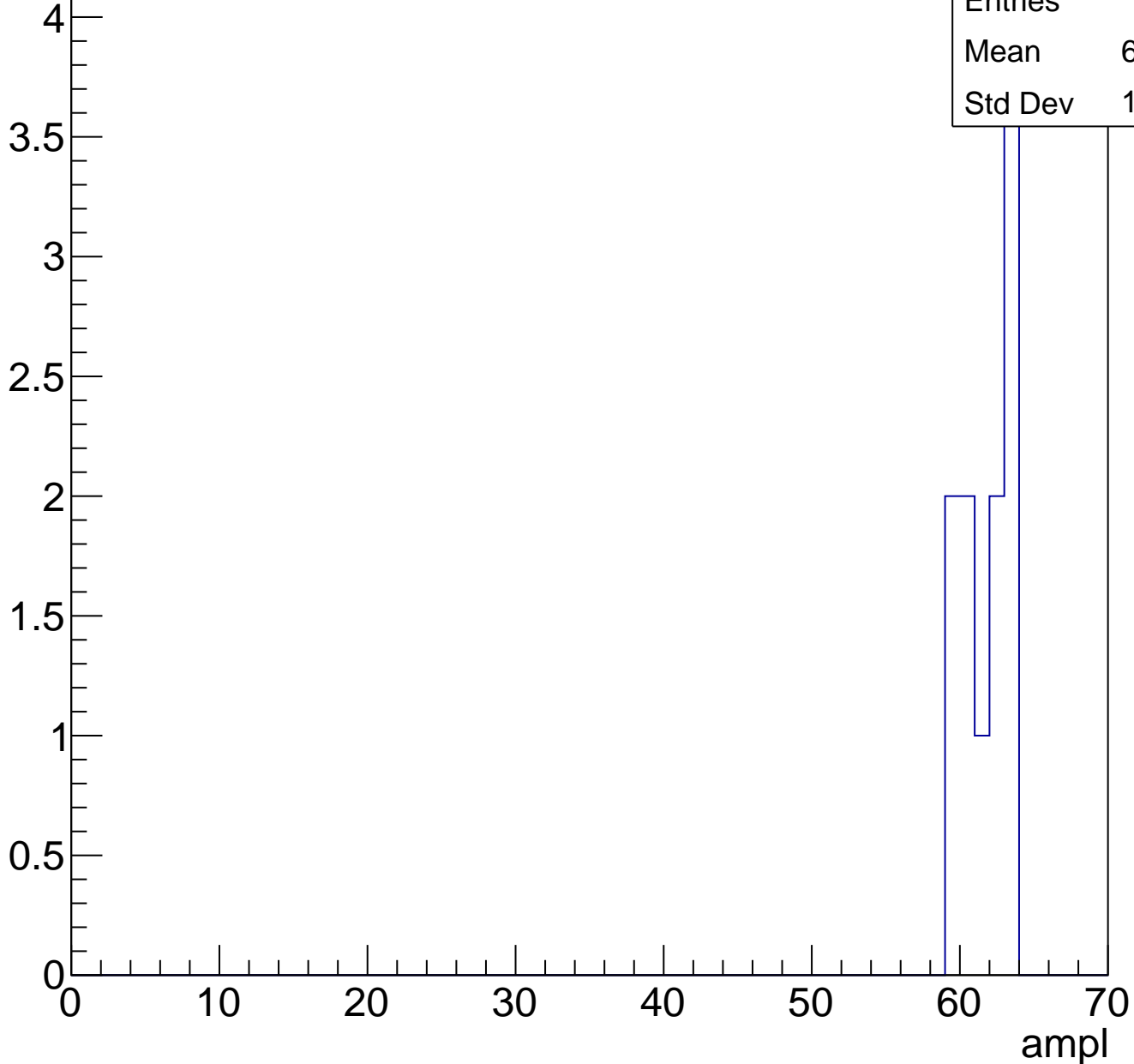
Entry



B1L103S, U14-ch86, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch86, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



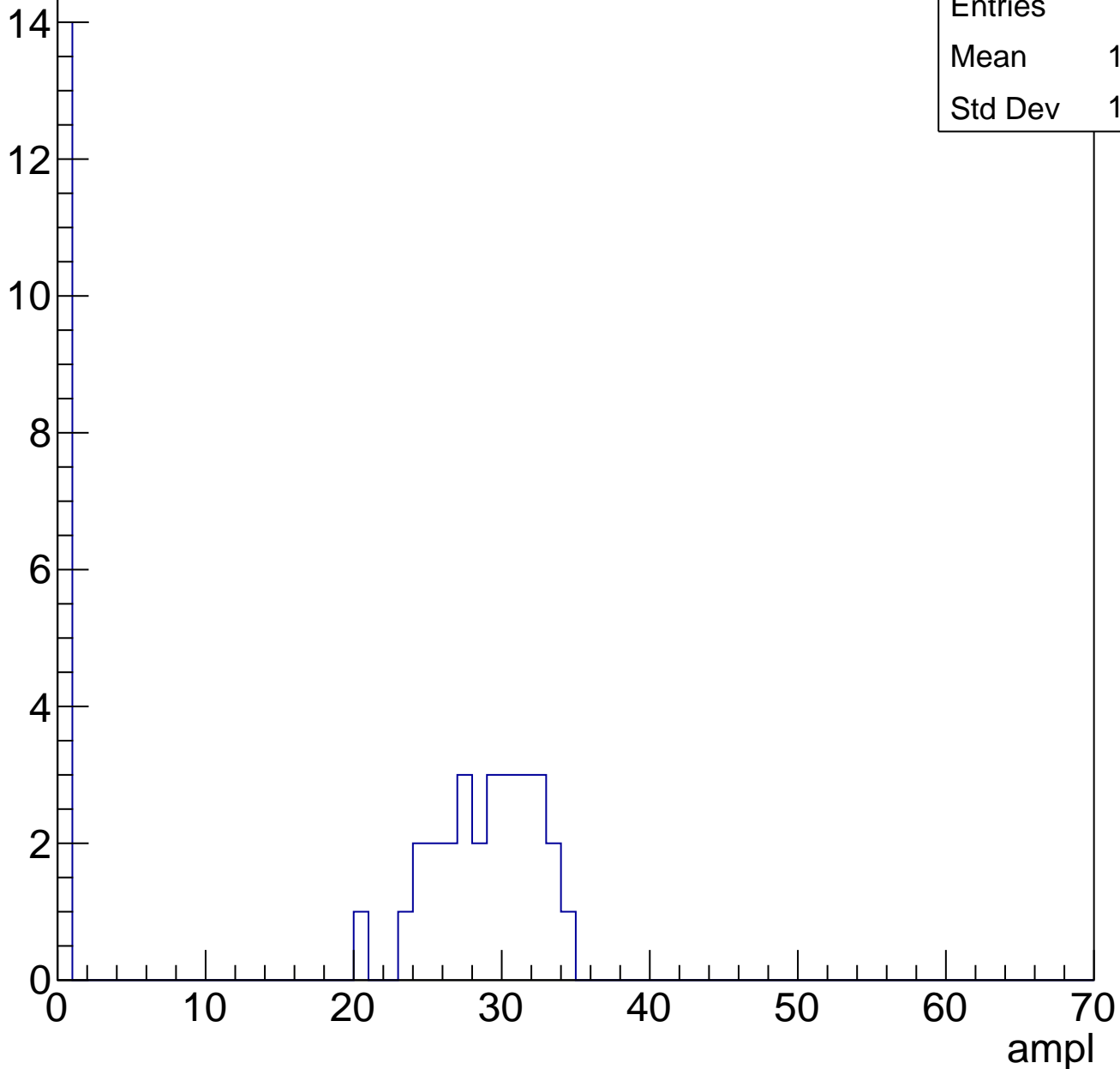
Entries	10
Mean	0
Std Dev	0

B1L103S, U14-ch87, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	42
Mean	18.95
Std Dev	13.68

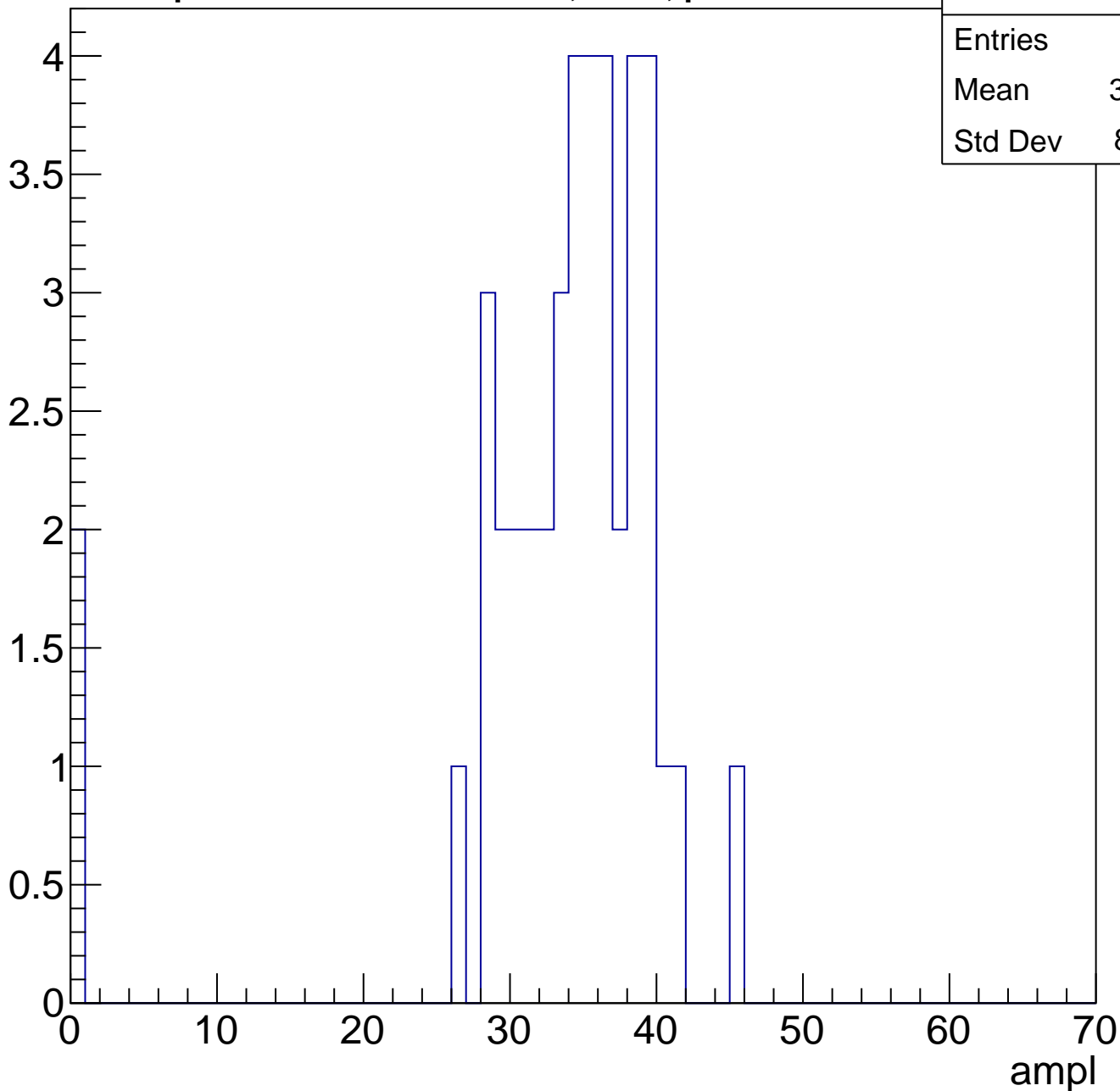
Entry



B1L103S, U14-ch87, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

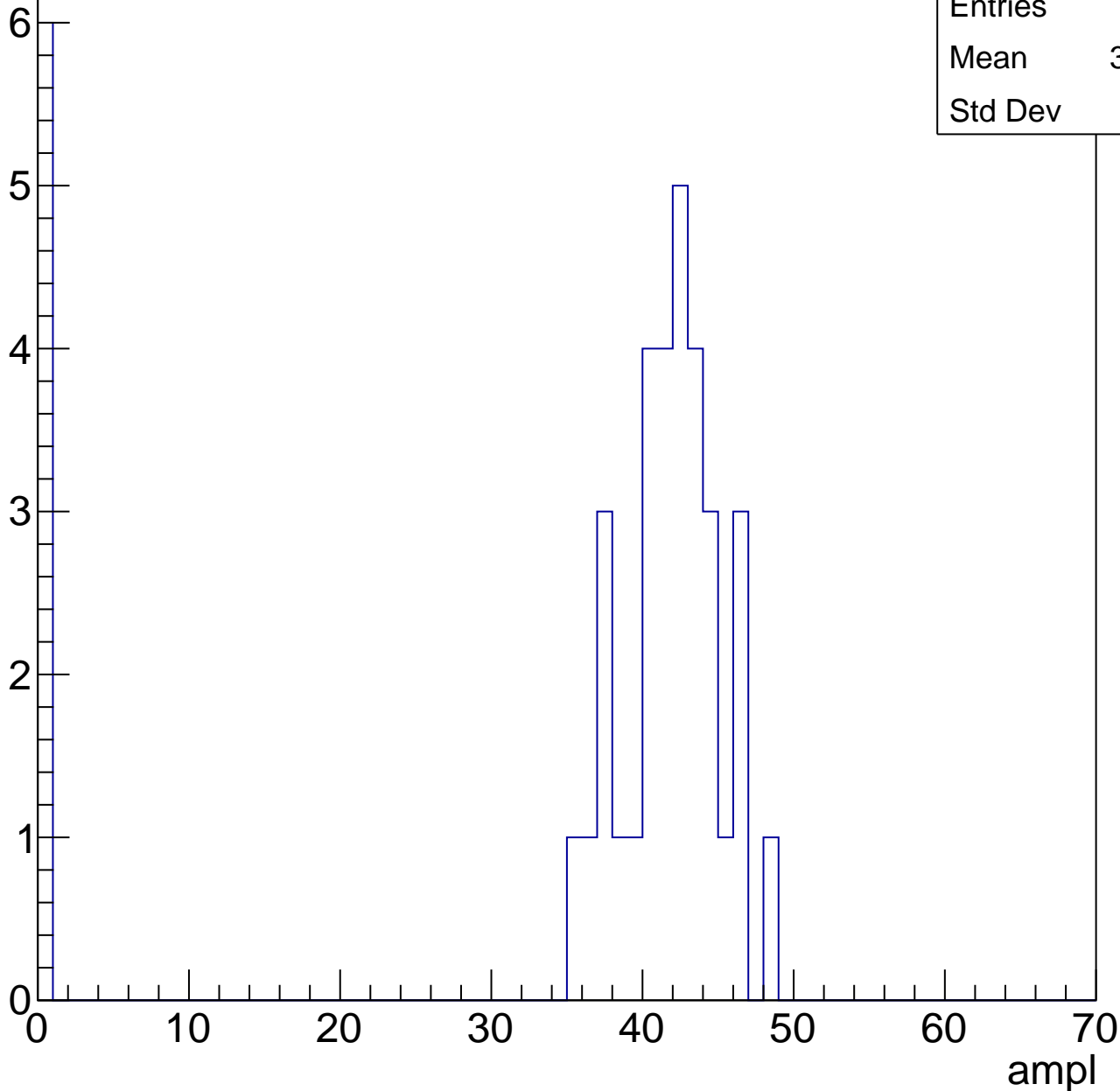


B1L103S, U14-ch87, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	38
Mean	34.95
Std Dev	15.4

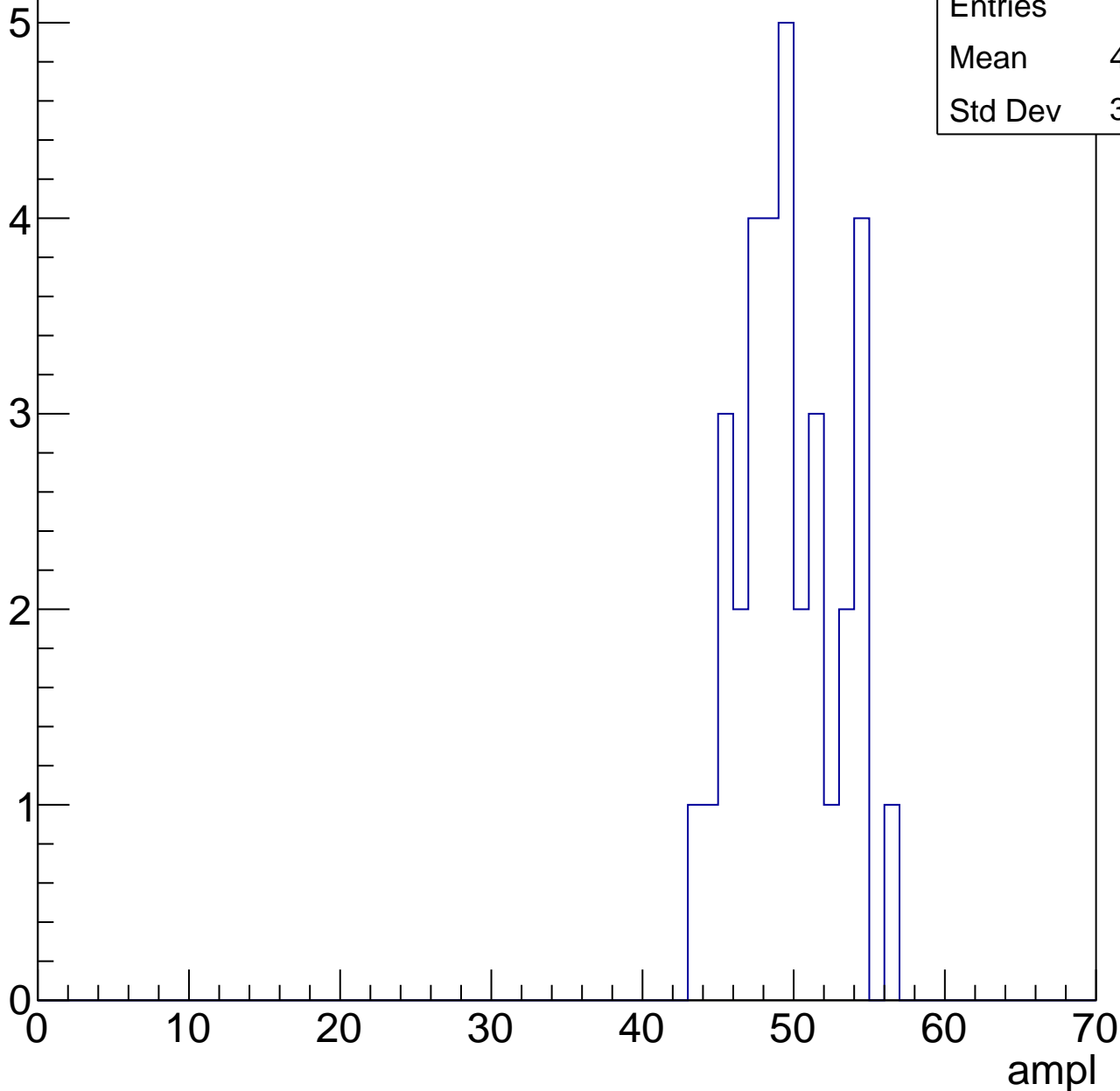


B1L103S, U14-ch87, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

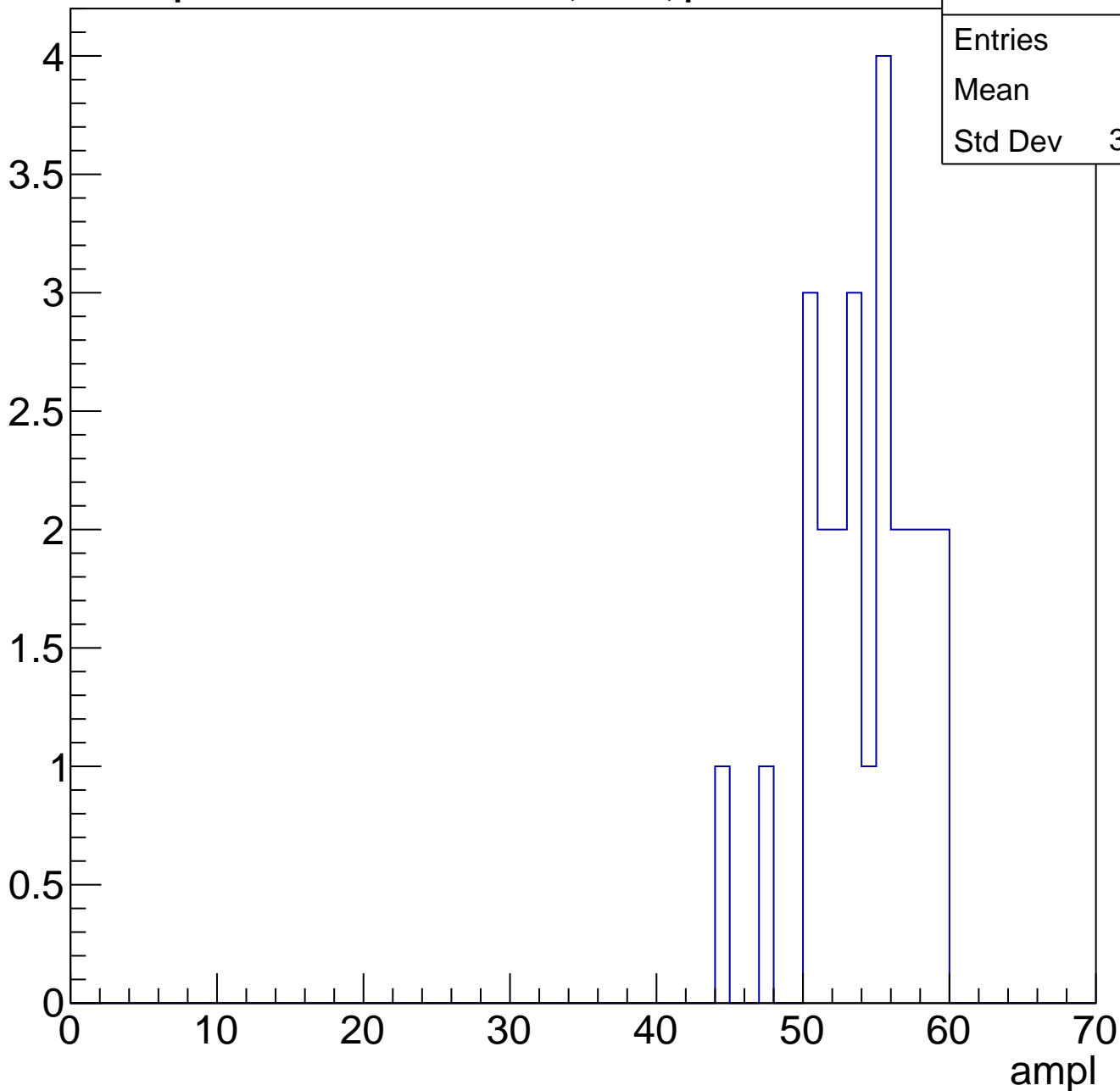
Entries	33
Mean	49.15
Std Dev	3.258



B1L103S, U14-ch87, adc4

calib_packv5_041523_1651.root, FC#0, port C2

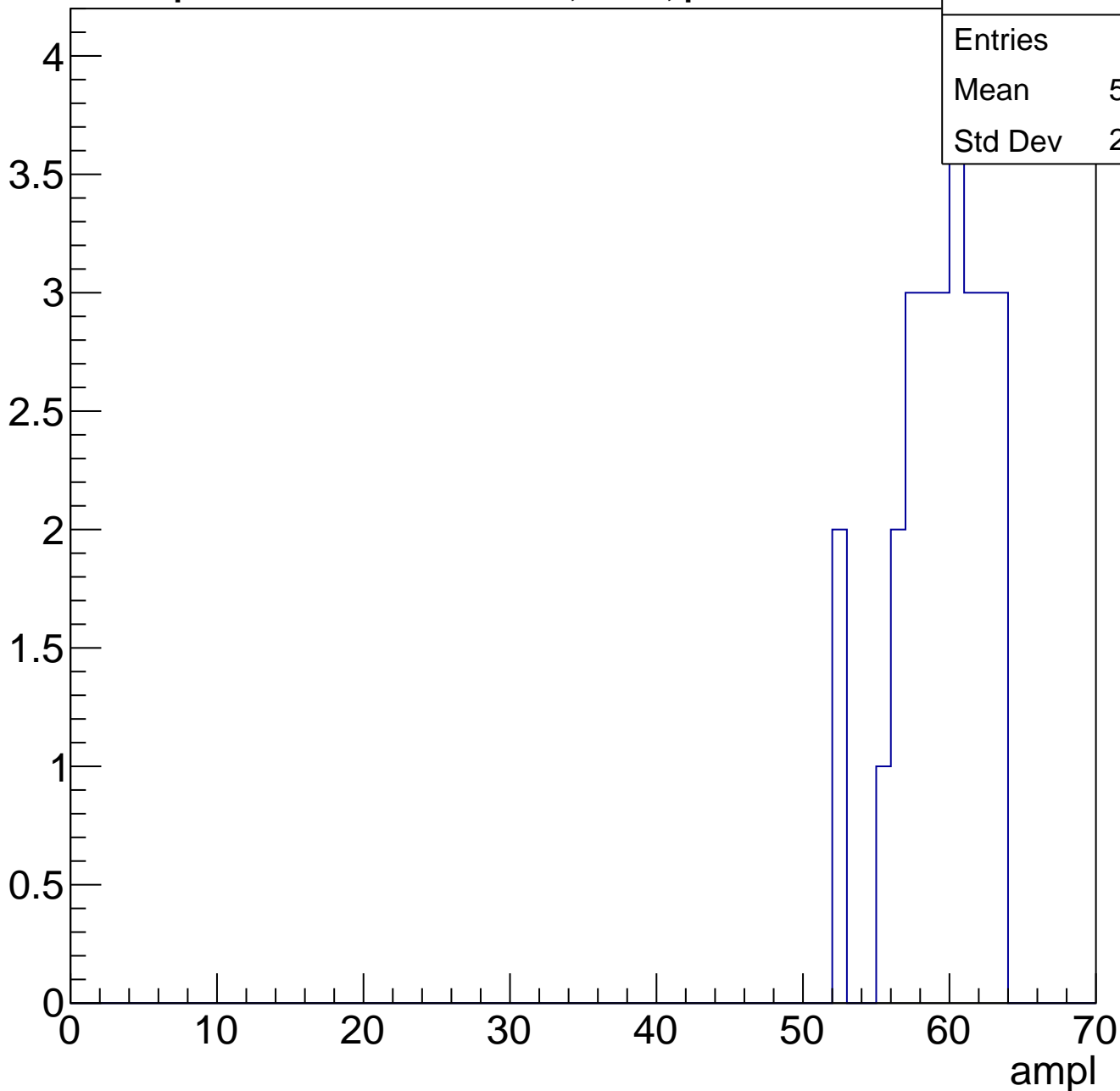
Entry



B1L103S, U14-ch87, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch87, adc6

calib_packv5_041523_1651.root, FC#0, port C2

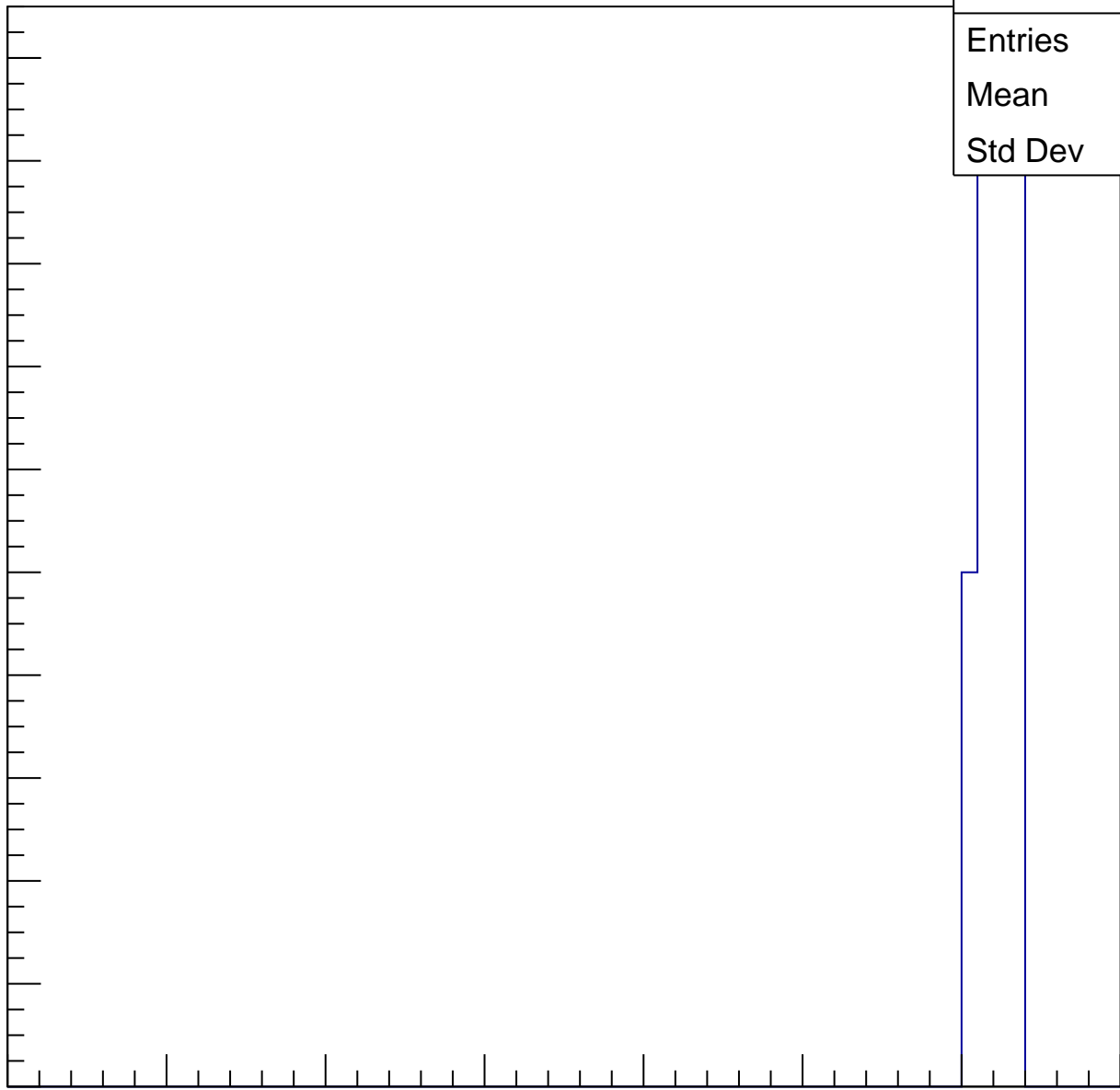
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	7
Mean	61.71
Std Dev	1.03

ampl

0 10 20 30 40 50 60 70



B1L103S, U14-ch87, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

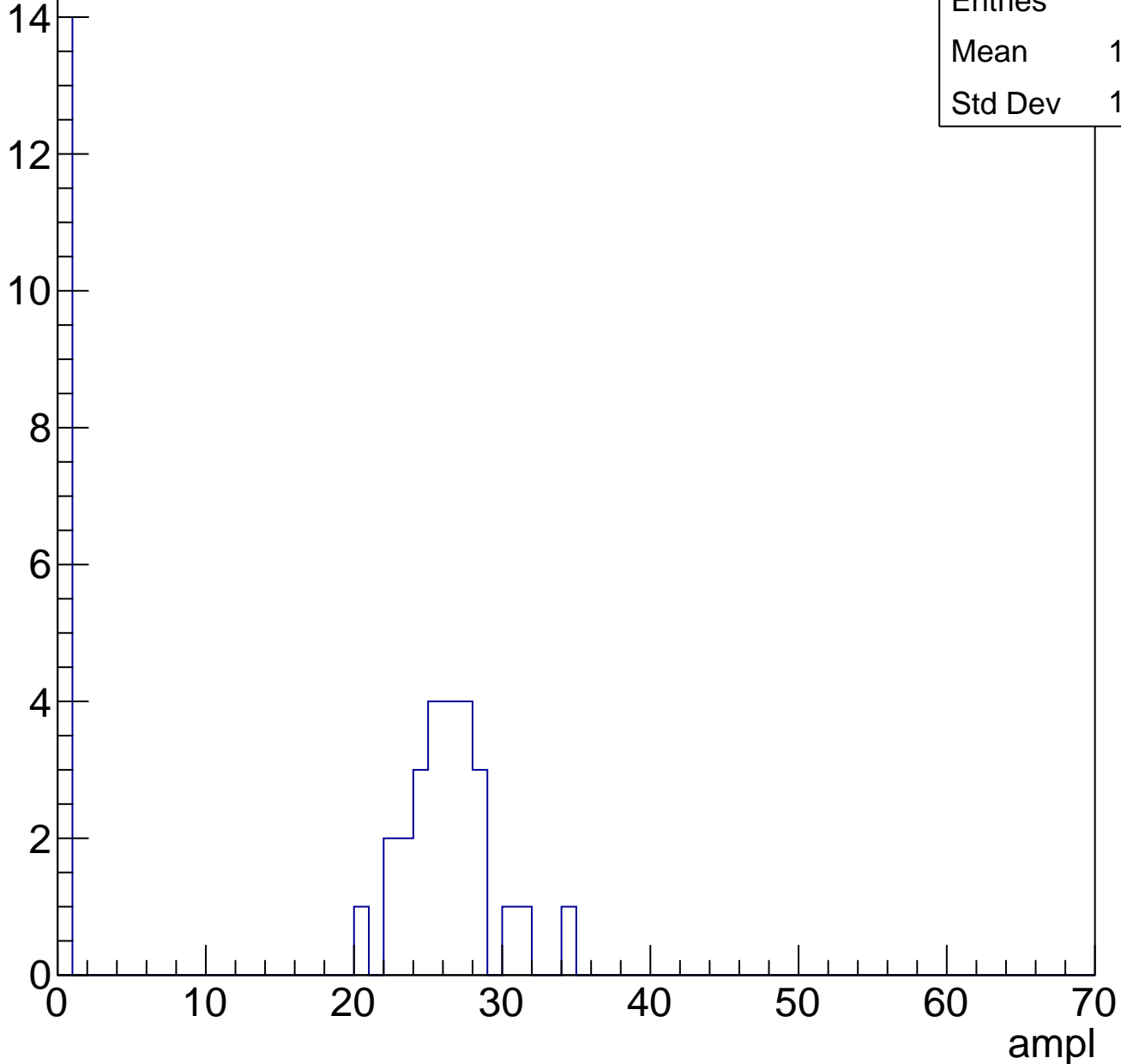


B1L103S, U14-ch88, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	40
Mean	16.82
Std Dev	12.57

Entry

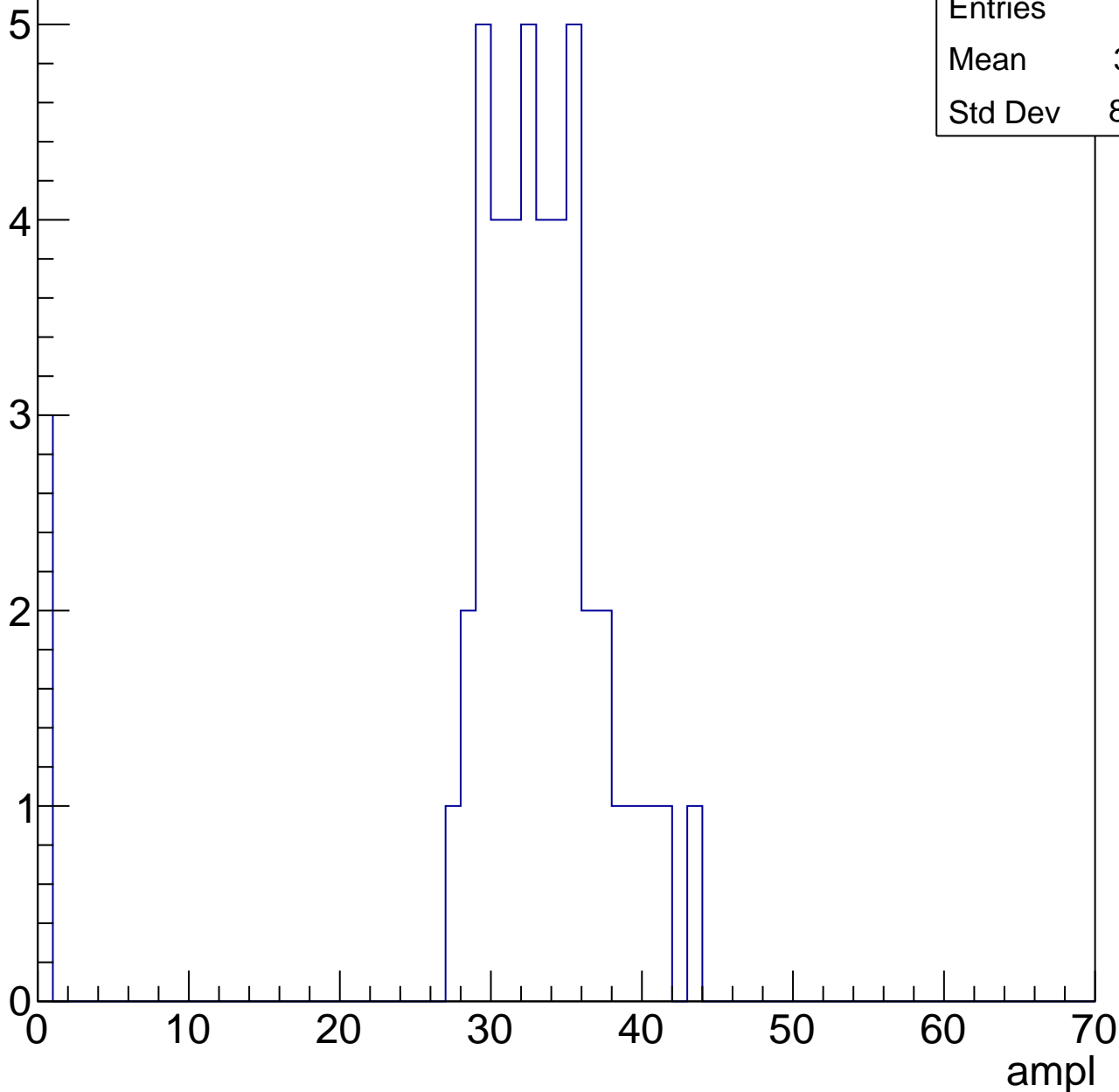


B1L103S, U14-ch88, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

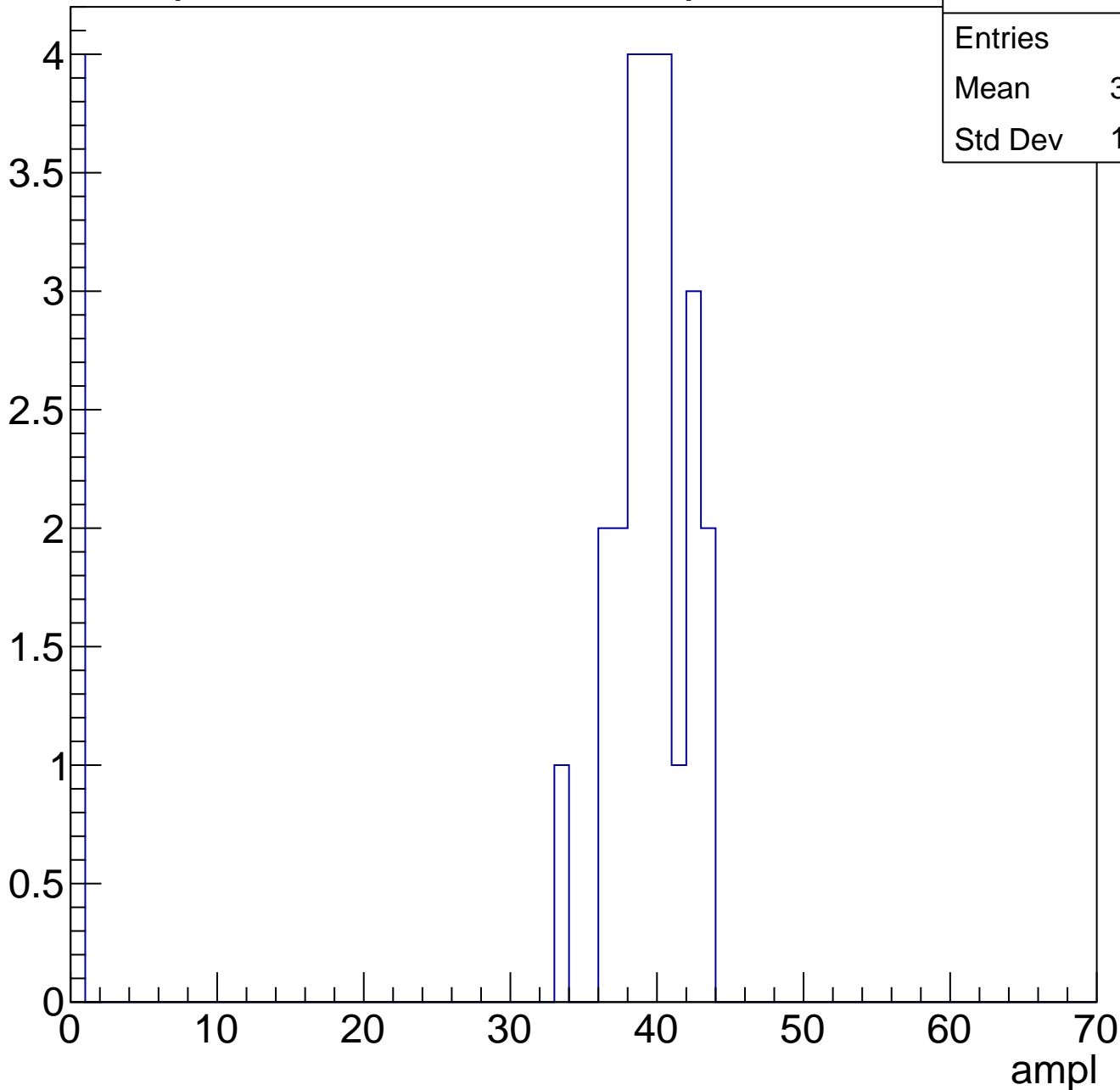
Entries	46
Mean	30.91
Std Dev	8.893



B1L103S, U14-ch88, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

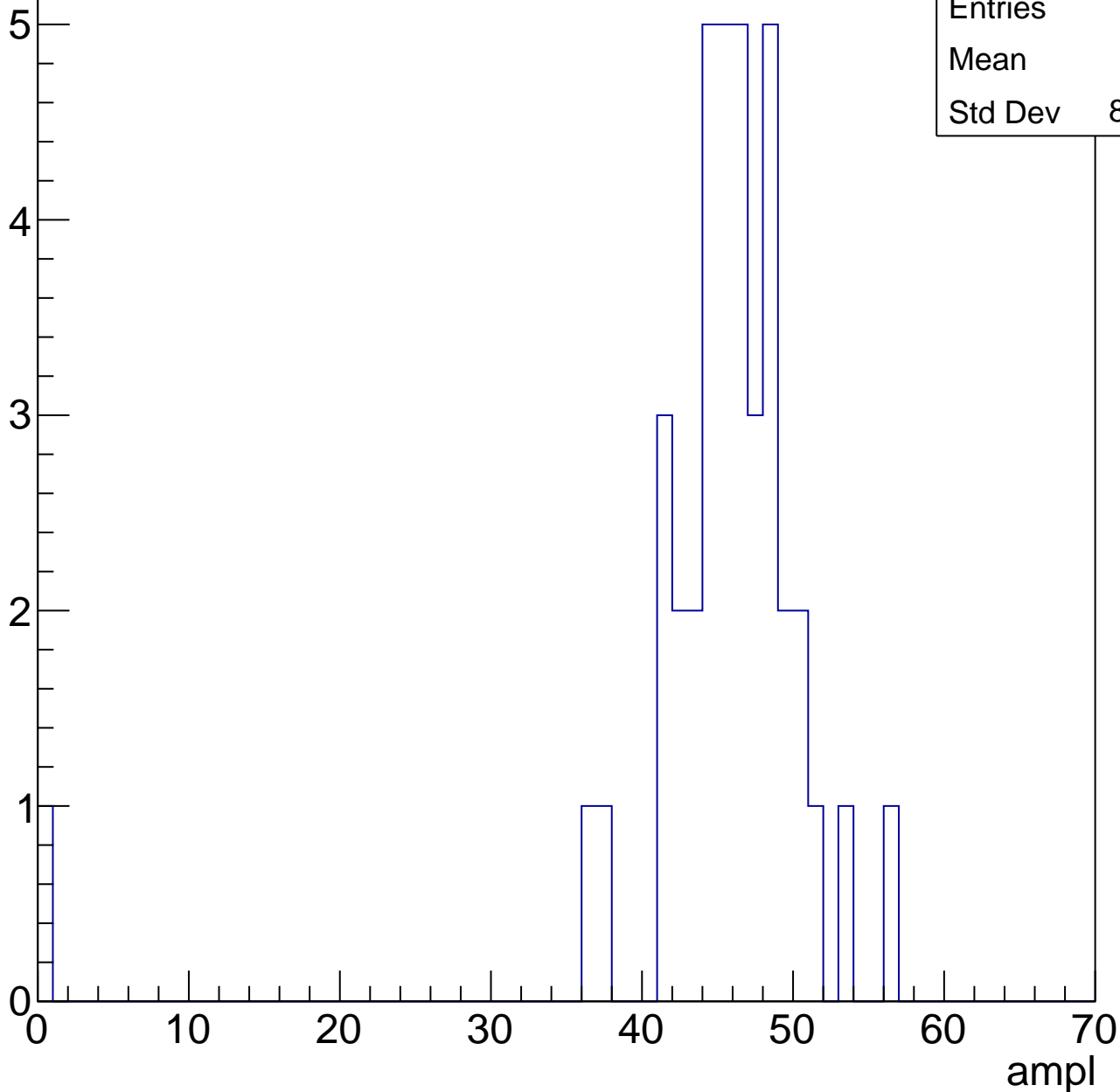


B1L103S, U14-ch88, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

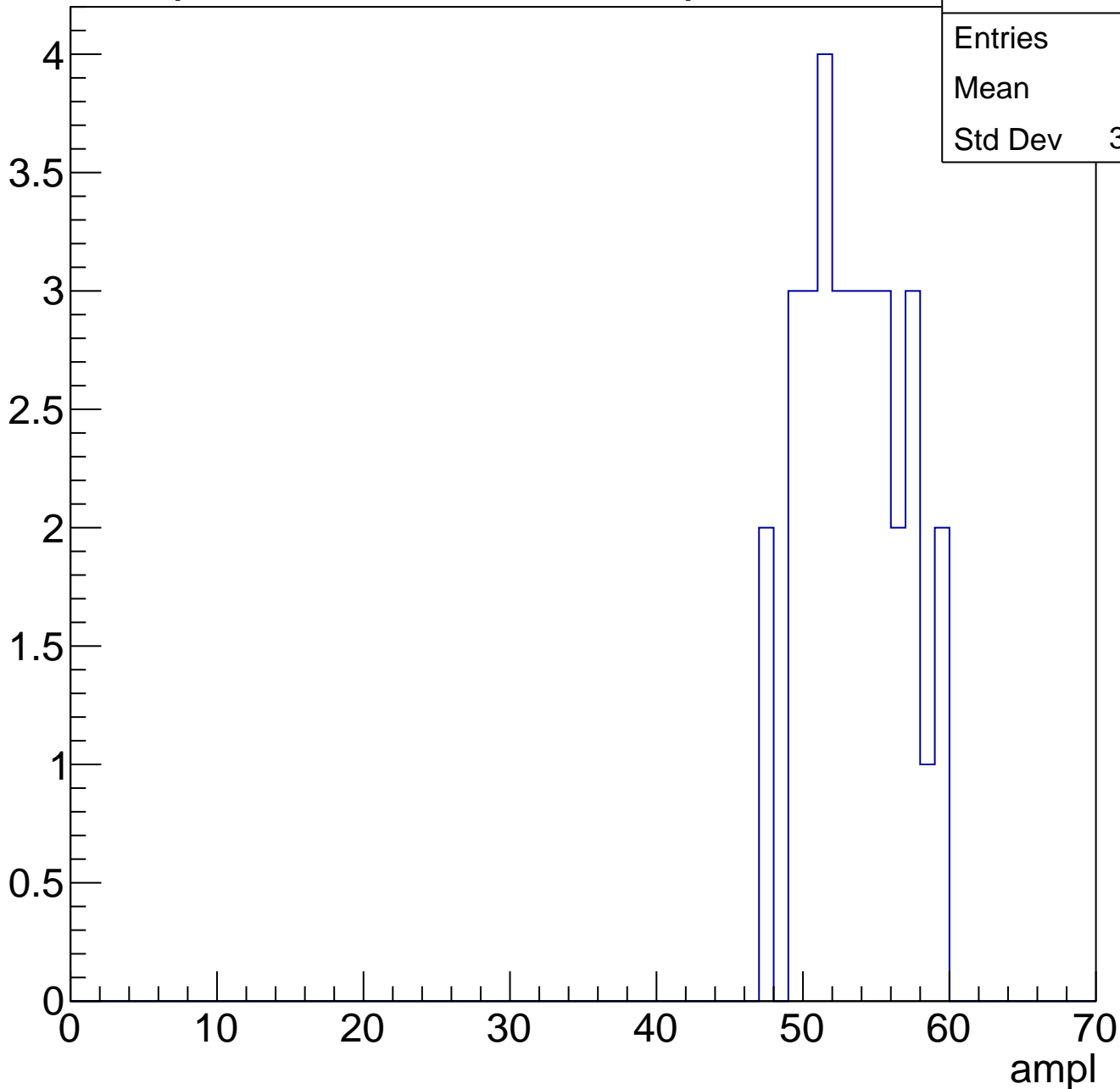
Entries	40
Mean	44.5
Std Dev	8.068



B1L103S, U14-ch88, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

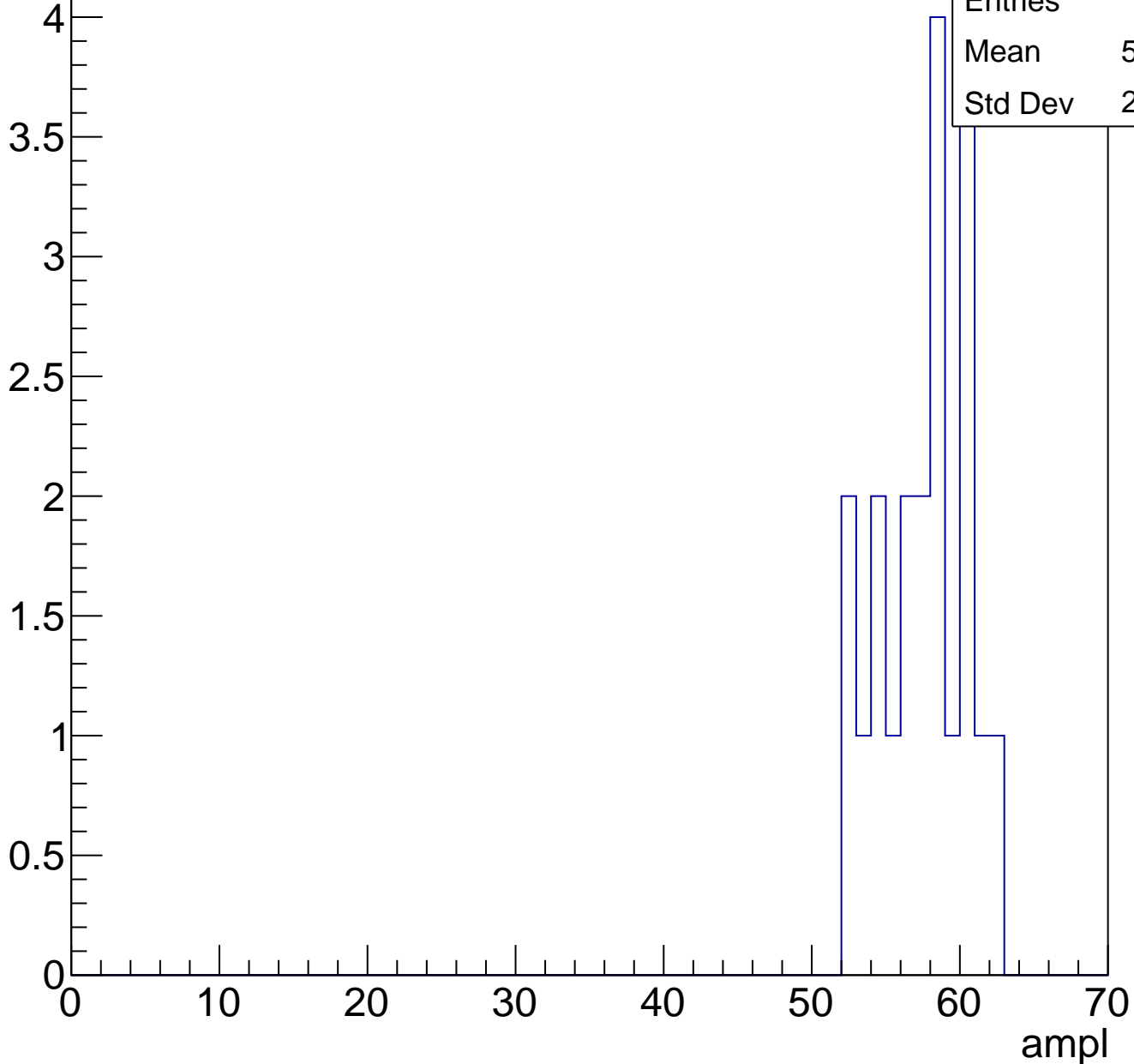


Entries	32
Mean	53
Std Dev	3.279

B1L103S, U14-ch88, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

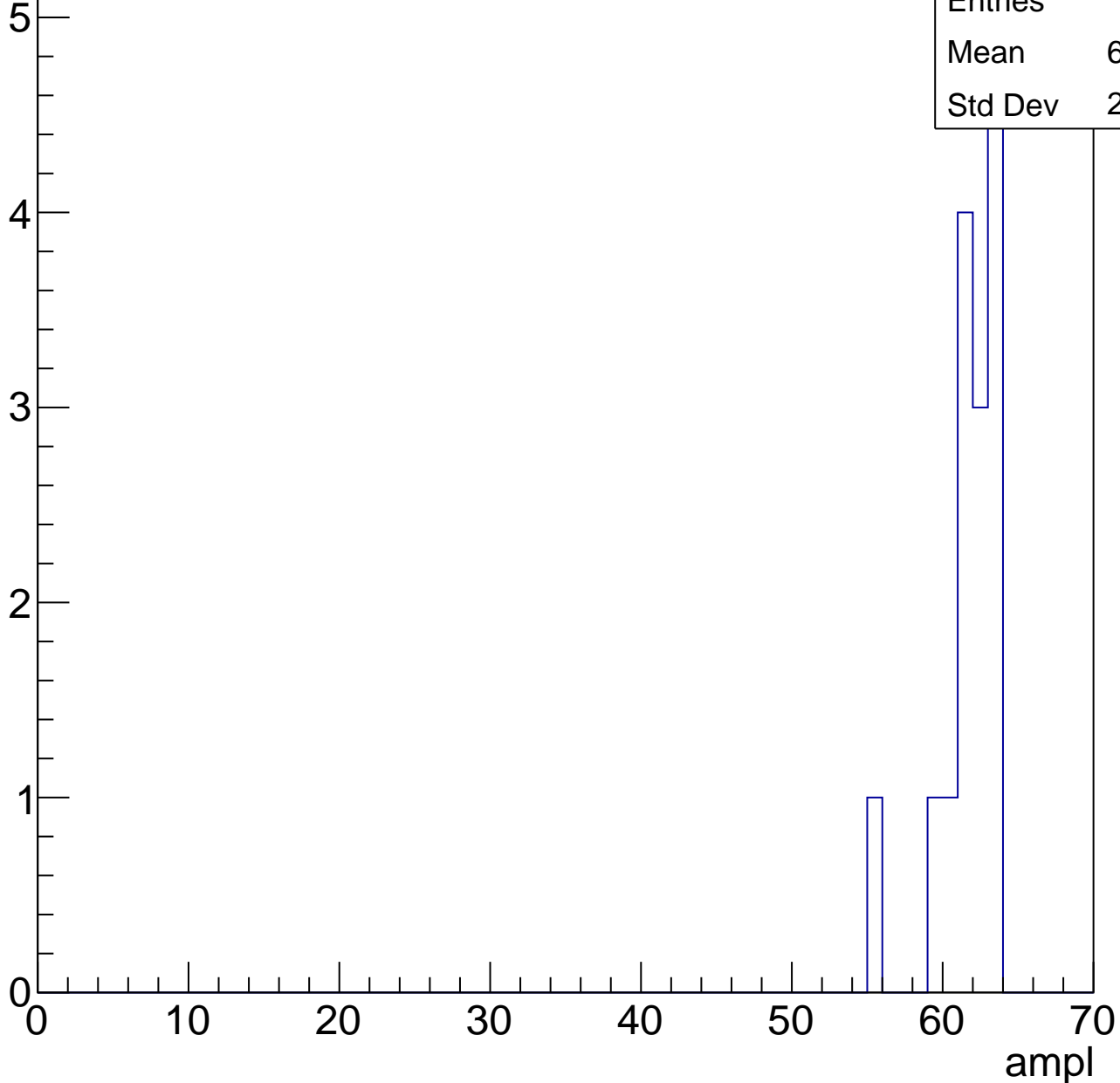


B1L103S, U14-ch88, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	15
Mean	61.27
Std Dev	2.048

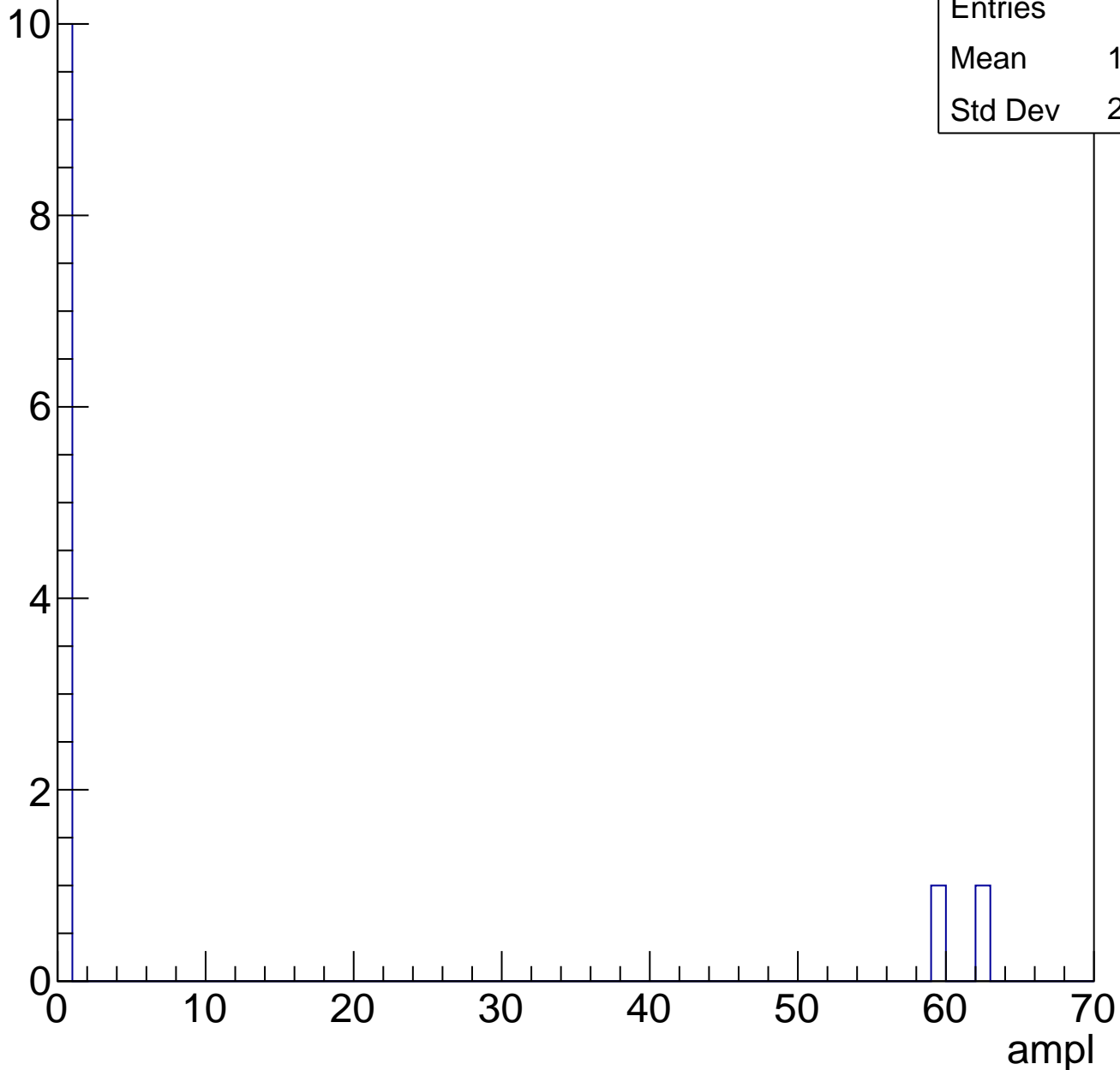


B1L103S, U14-ch88, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	12
Mean	10.08
Std Dev	22.56

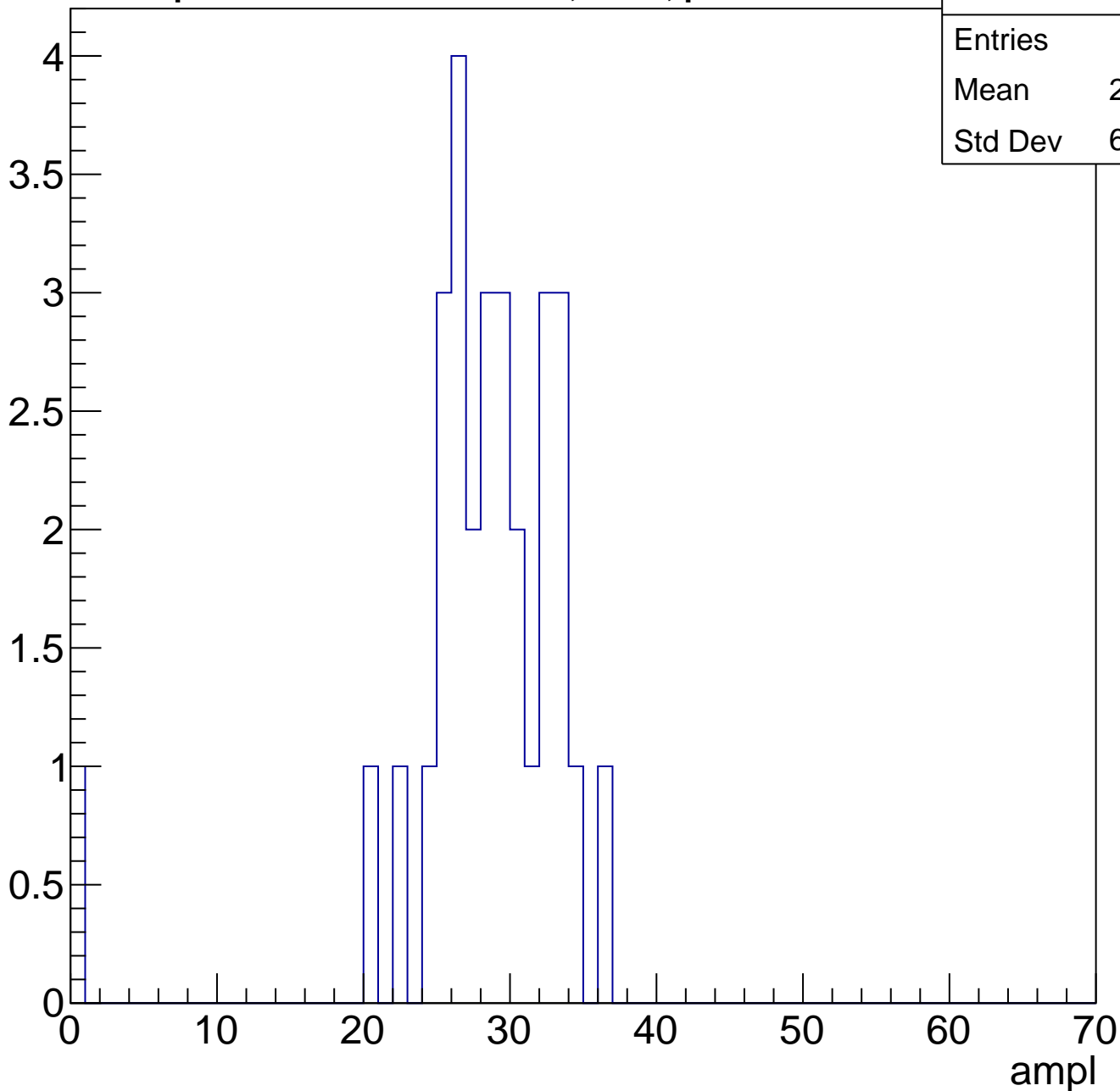
Entry



B1L103S, U14-ch89, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

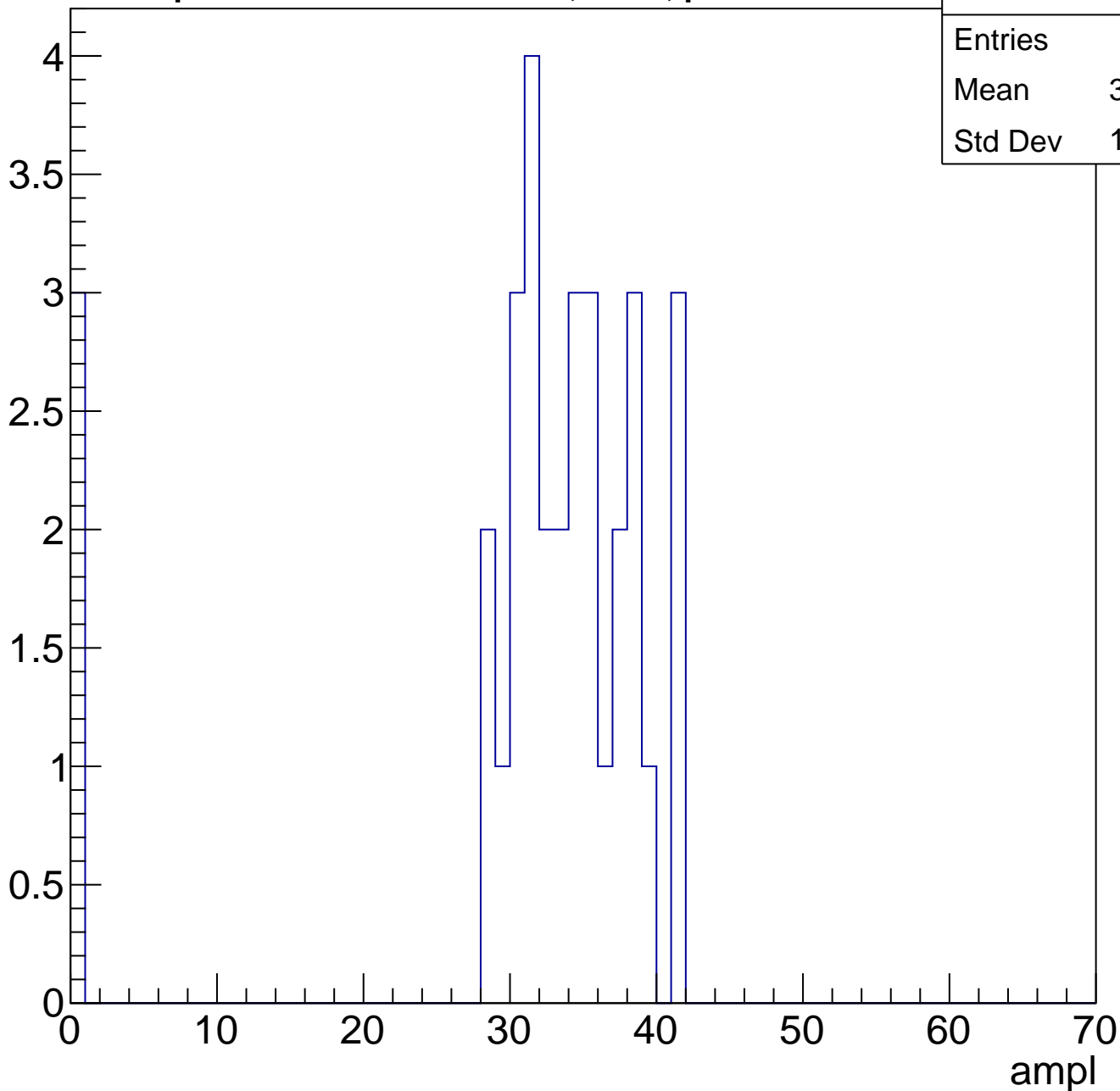


Entries	30
Mean	27.53
Std Dev	6.276

B1L103S, U14-ch89, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry



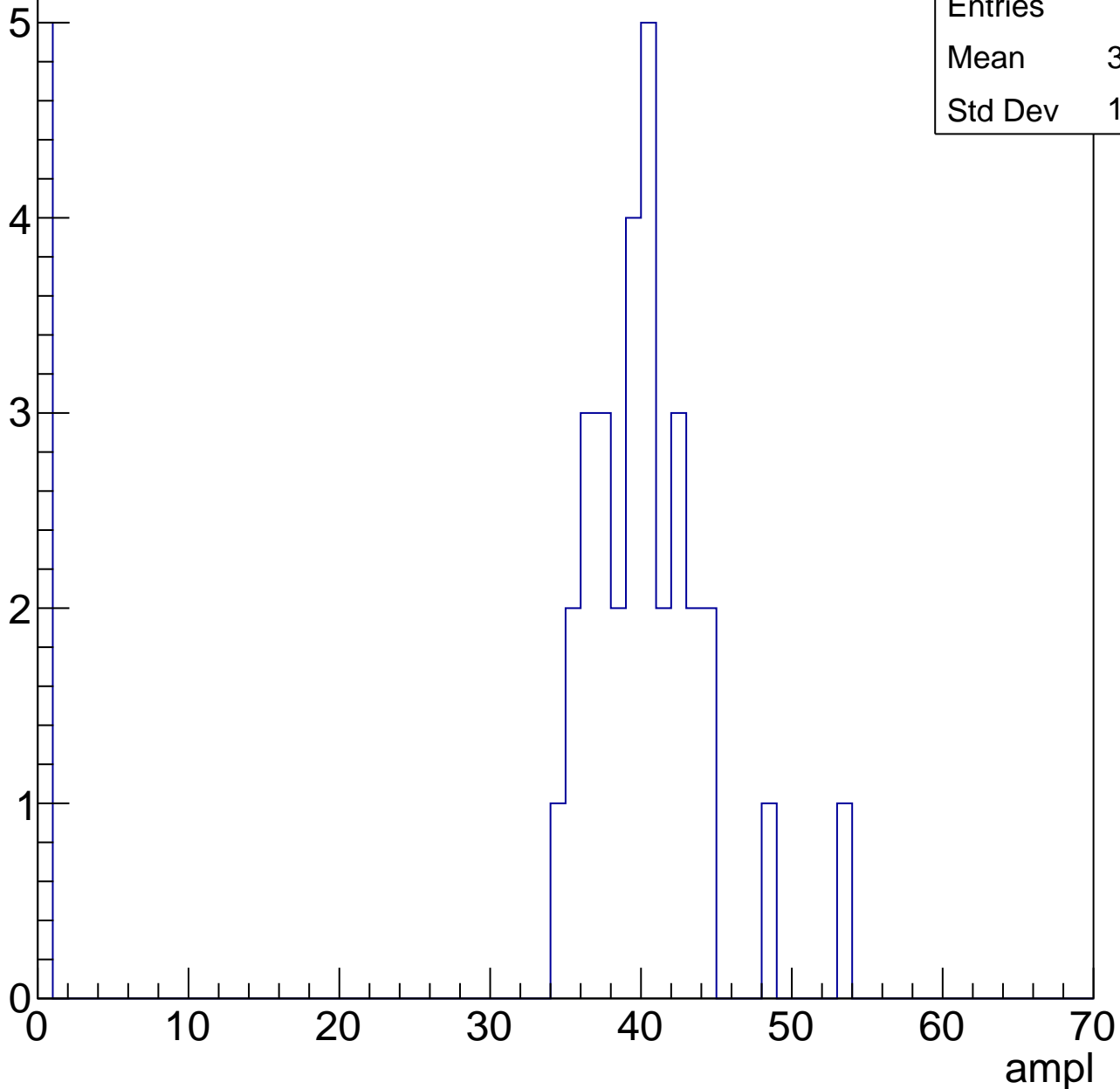
Entries	33
Mean	30.97
Std Dev	10.45

B1L103S, U14-ch89, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	36
Mean	34.39
Std Dev	14.28

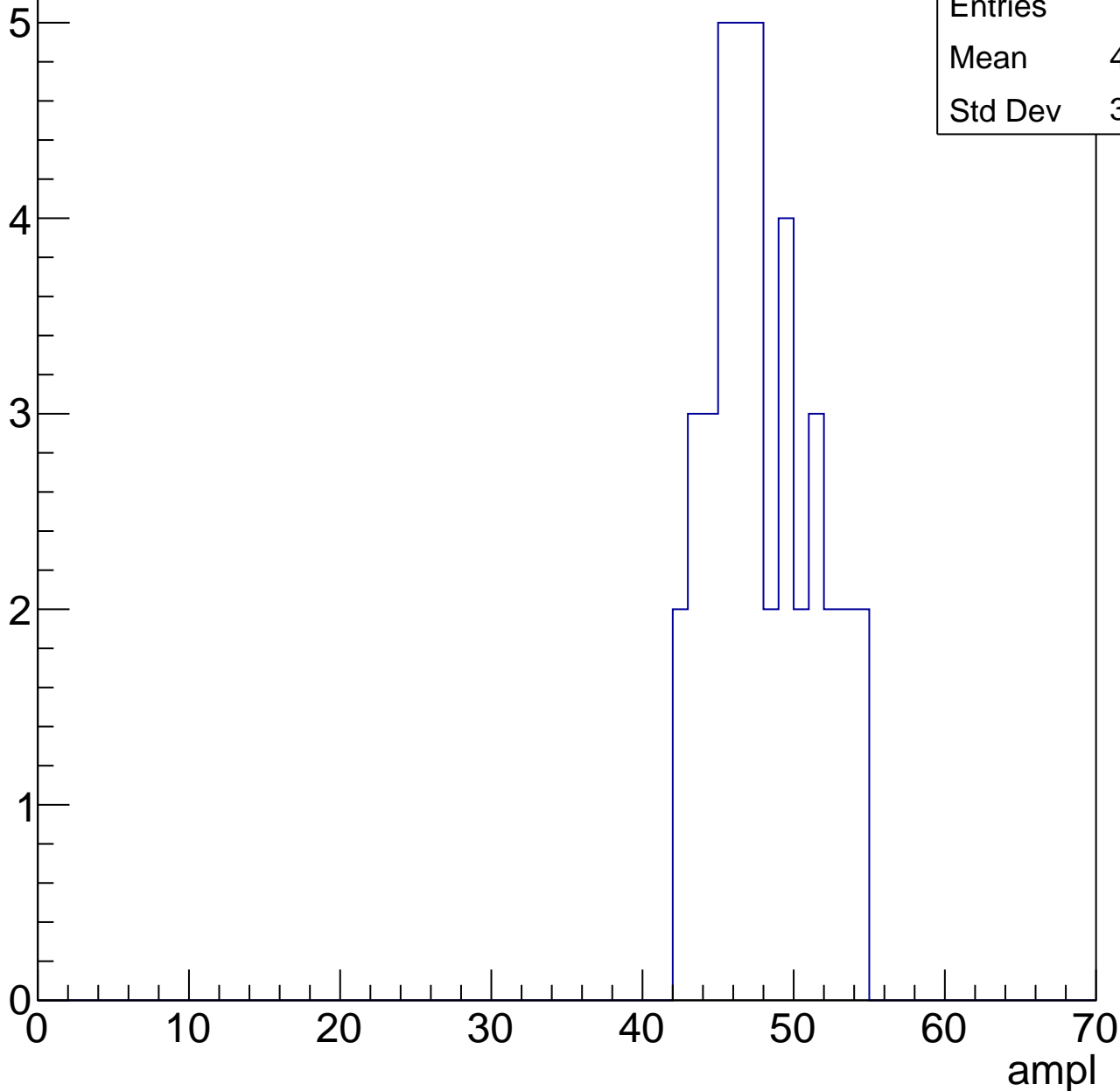


B1L103S, U14-ch89, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

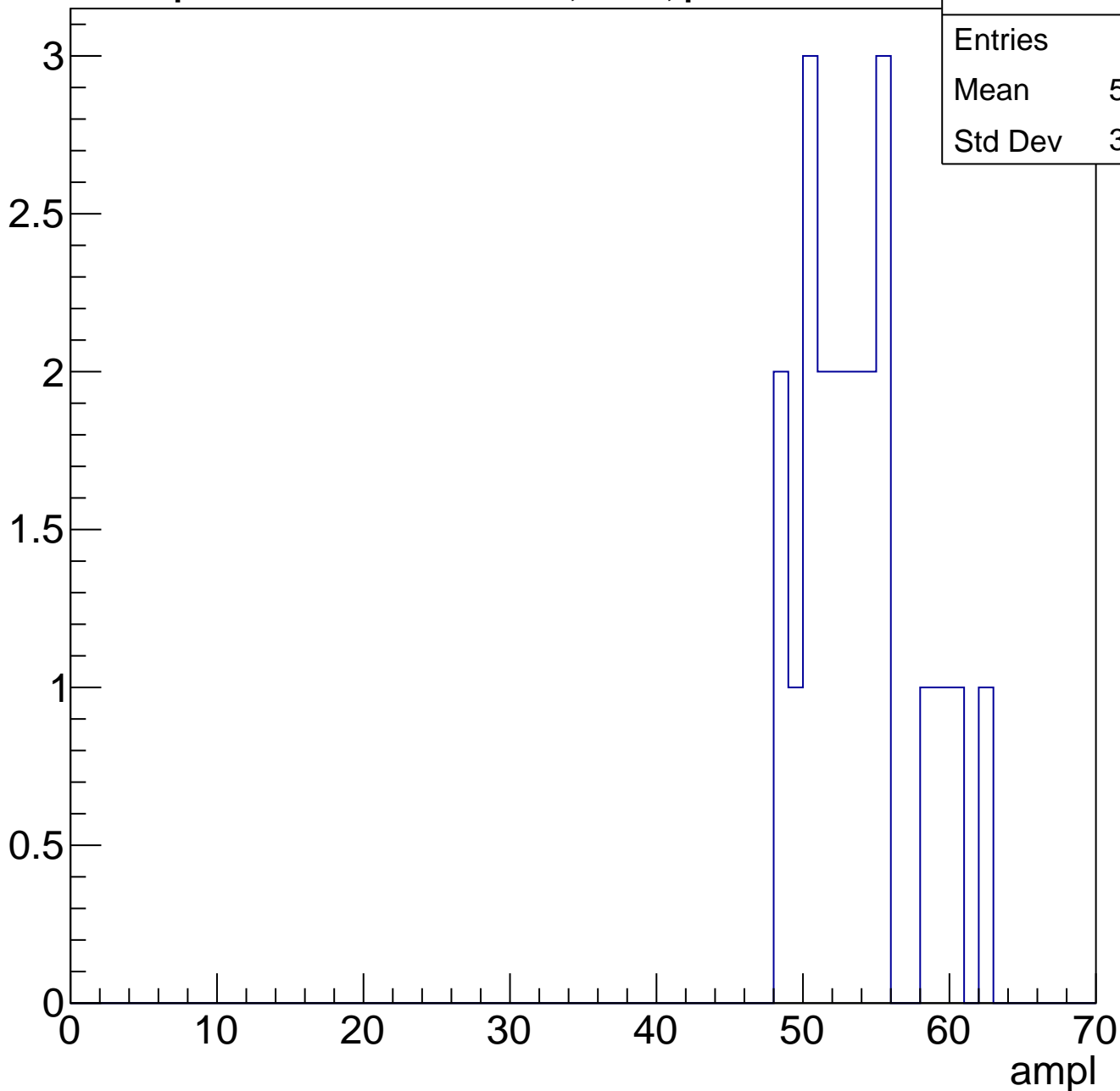
Entries	40
Mean	47.45
Std Dev	3.339



B1L103S, U14-ch89, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



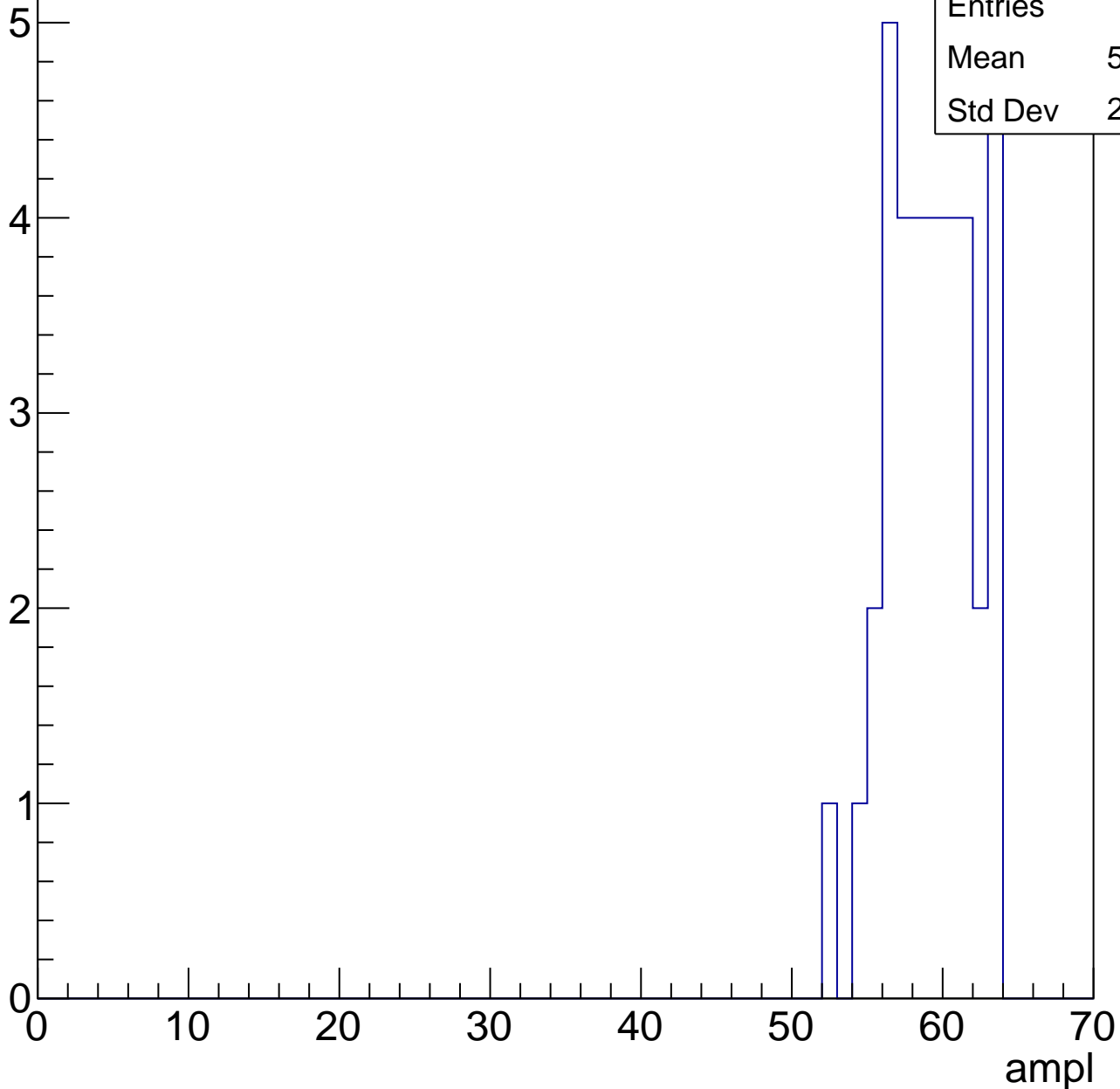
Entries	21
Mean	53.29
Std Dev	3.819

B1L103S, U14-ch89, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

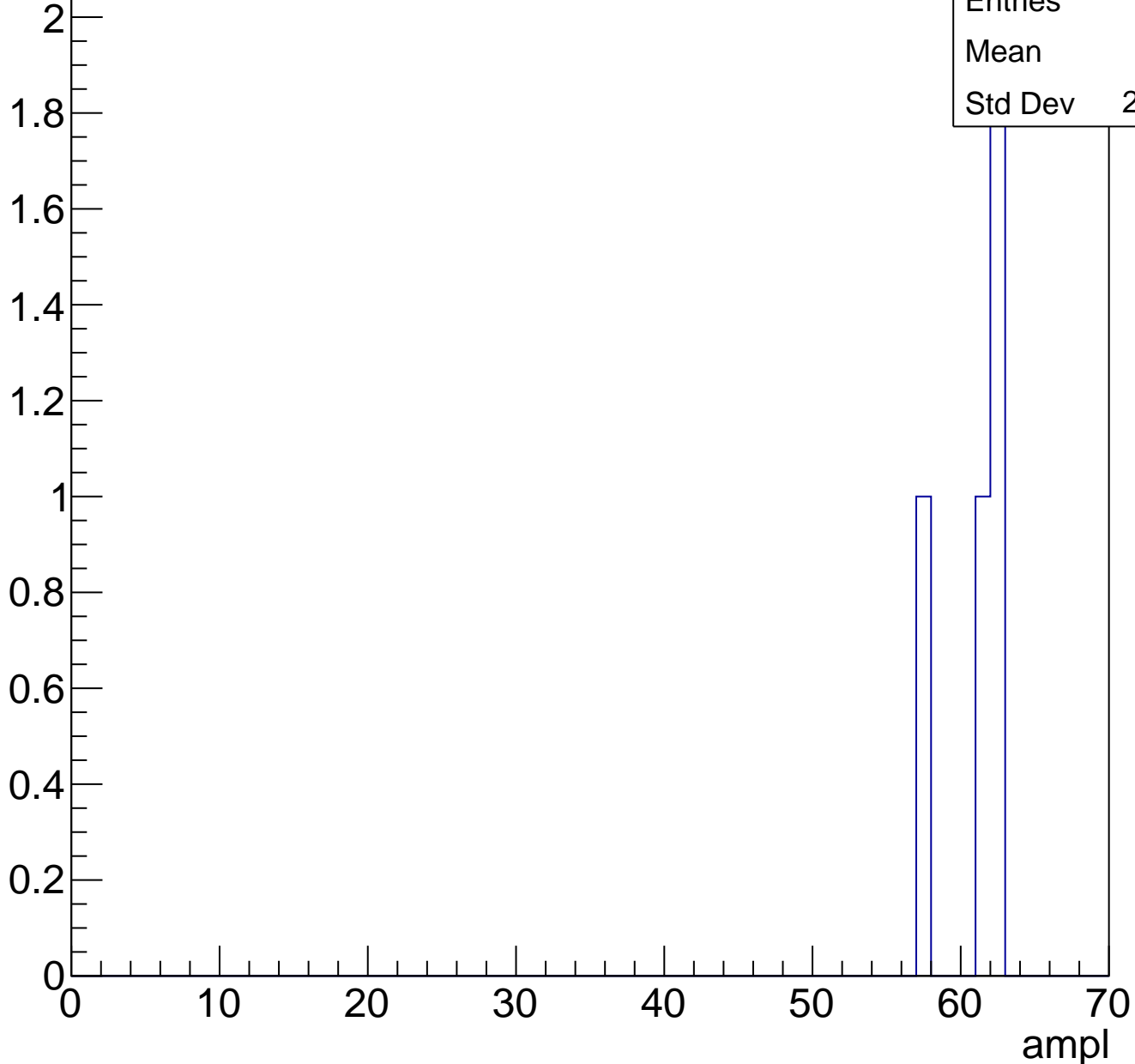
Entries	36
Mean	58.75
Std Dev	2.822



B1L103S, U14-ch89, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch89, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

Entries

11

Mean

0

Std Dev

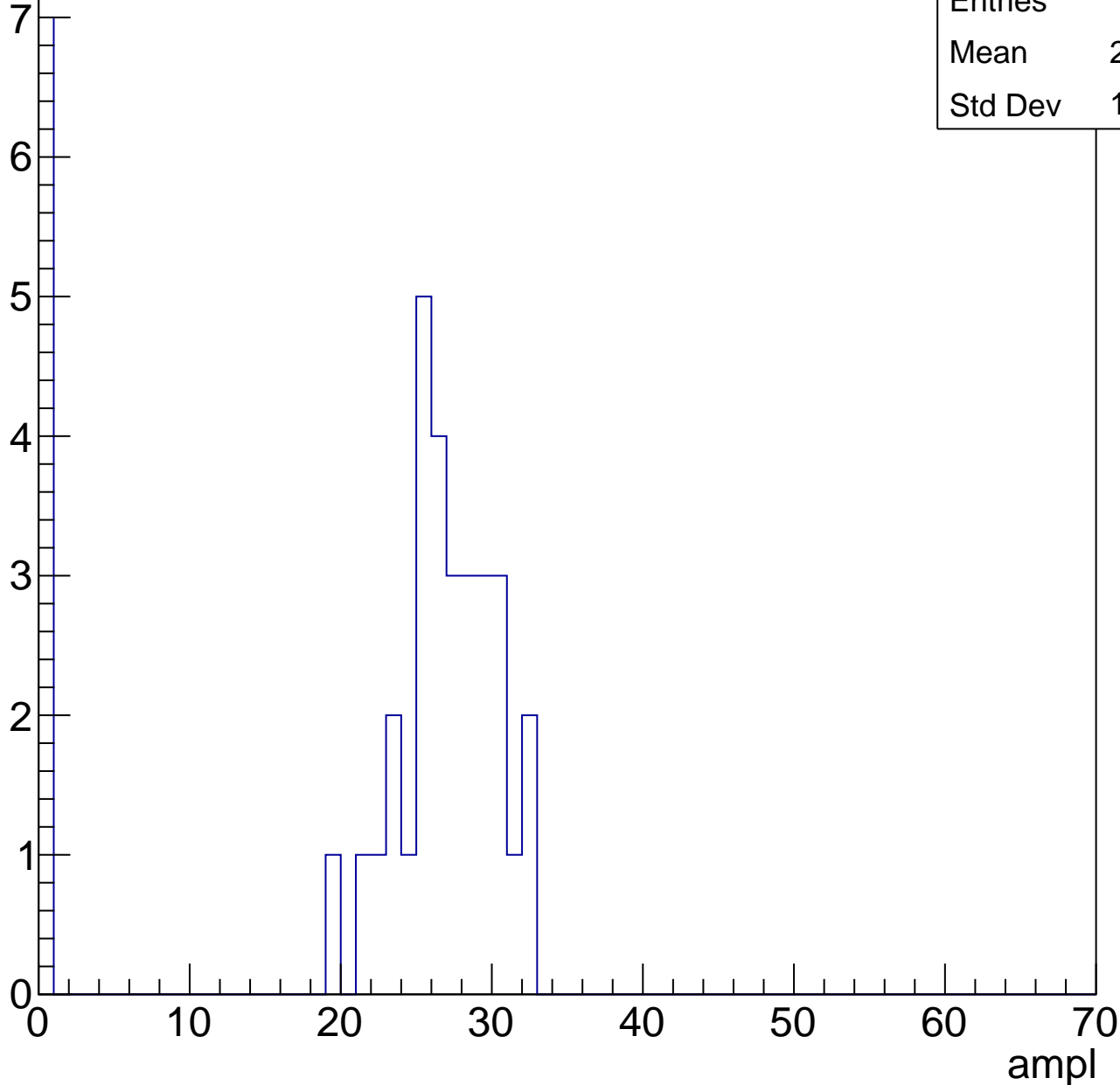
0

B1L103S, U14-ch90, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

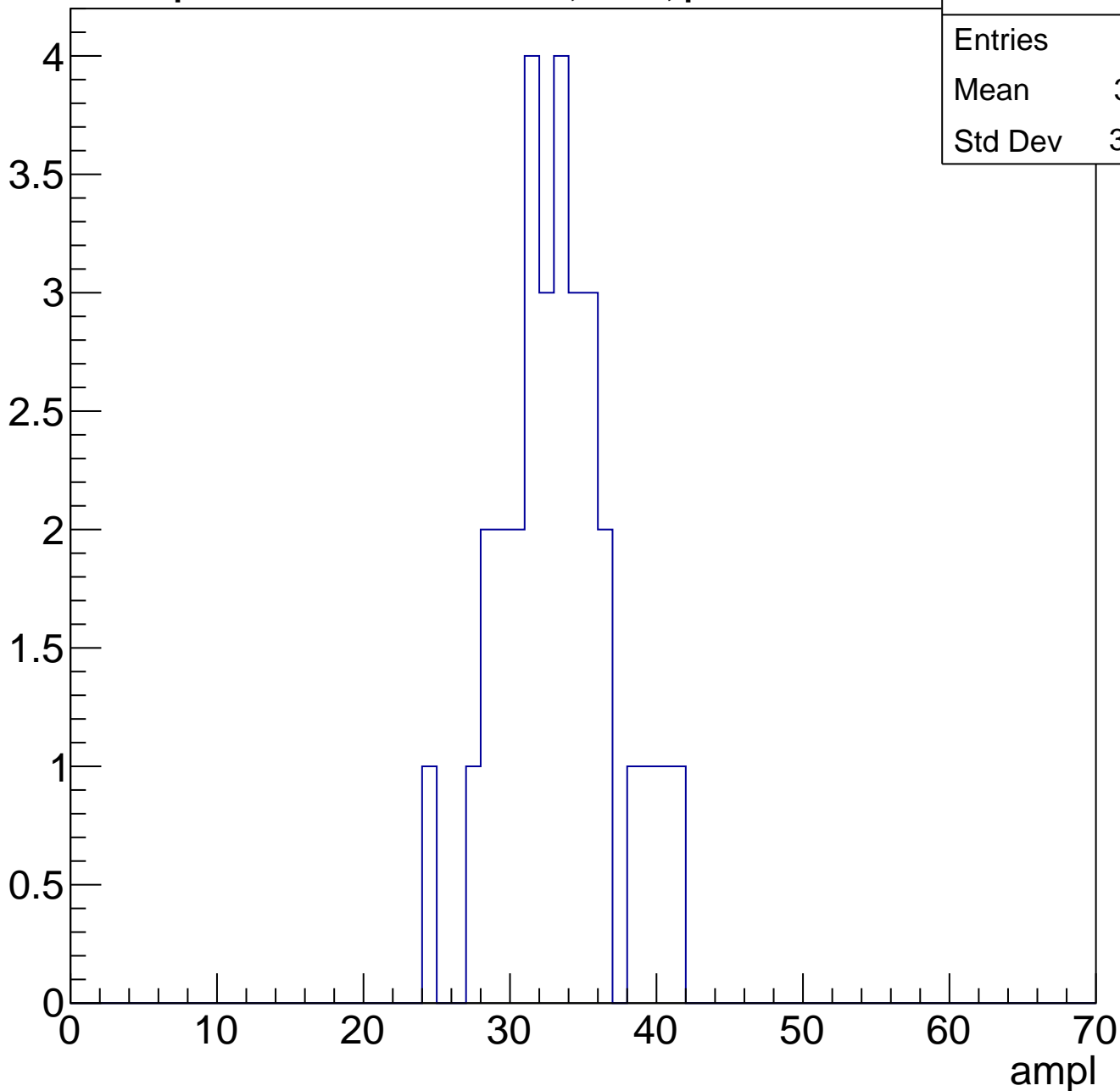
Entries	37
Mean	21.57
Std Dev	10.79



B1L103S, U14-ch90, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

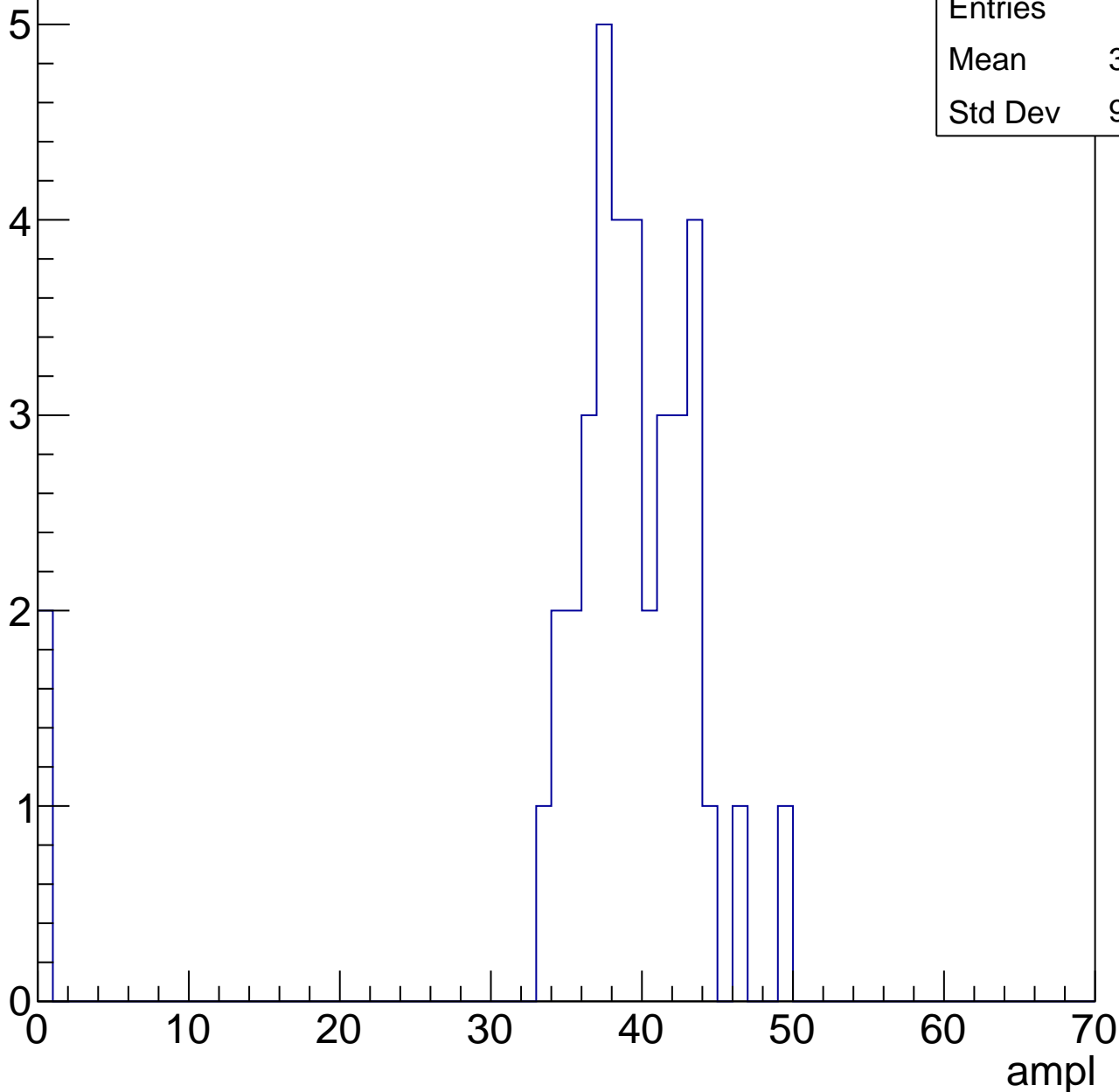


B1L103S, U14-ch90, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	38
Mean	37.16
Std Dev	9.405

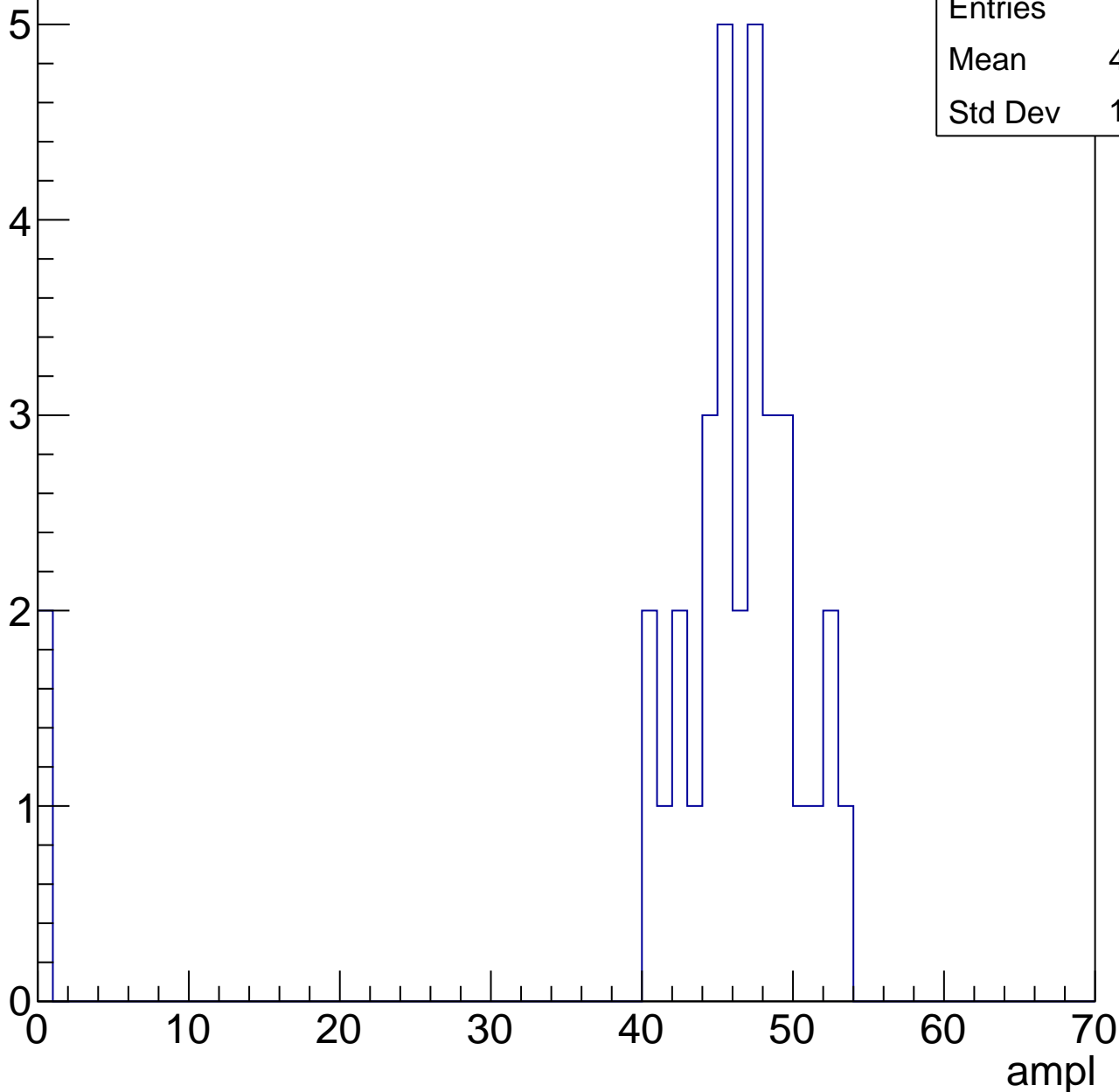


B1L103S, U14-ch90, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

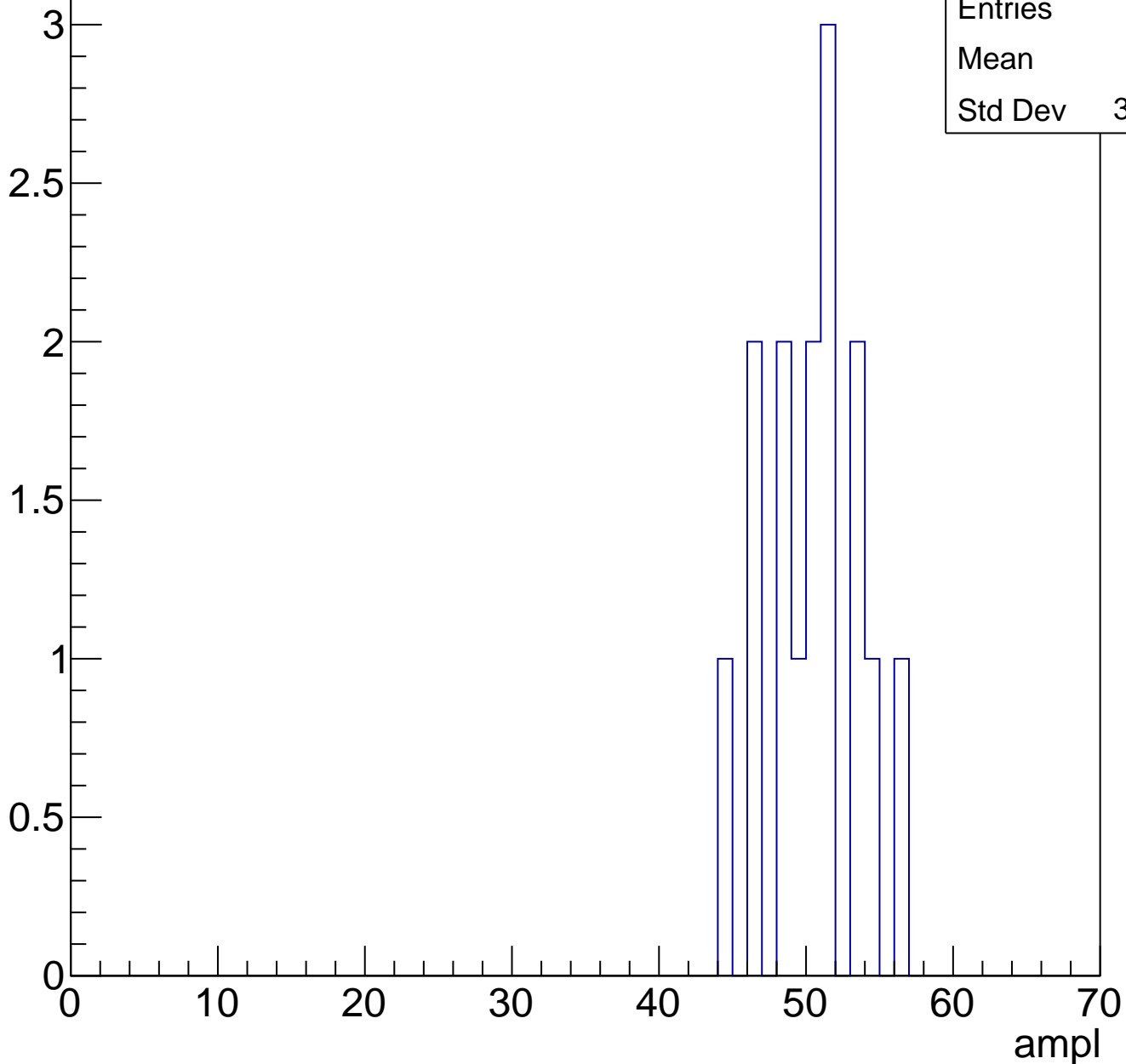
Entries	34
Mean	43.56
Std Dev	11.36



B1L103S, U14-ch90, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

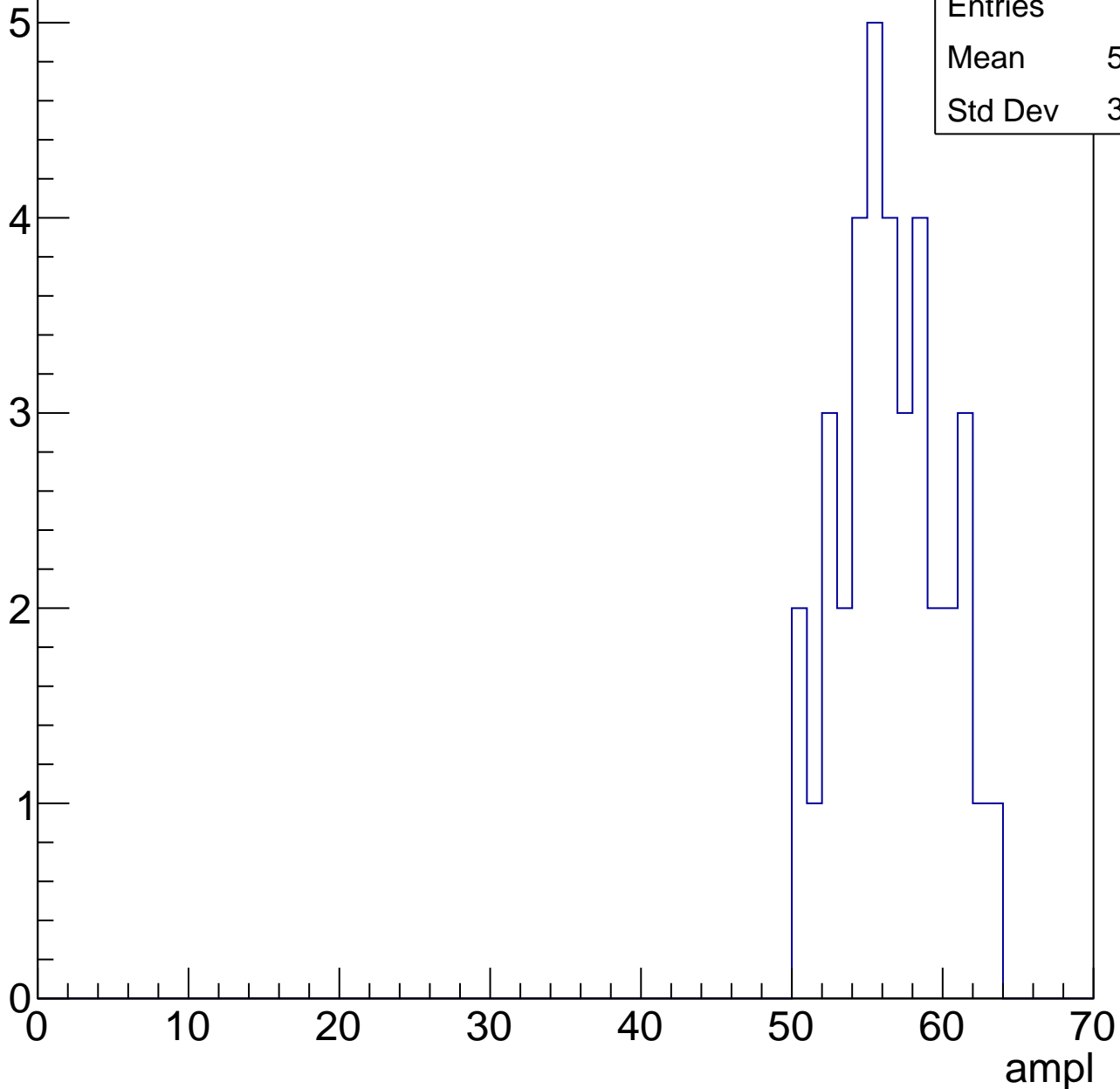


B1L103S, U14-ch90, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	37
Mean	56.14
Std Dev	3.338



B1L103S, U14-ch90, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

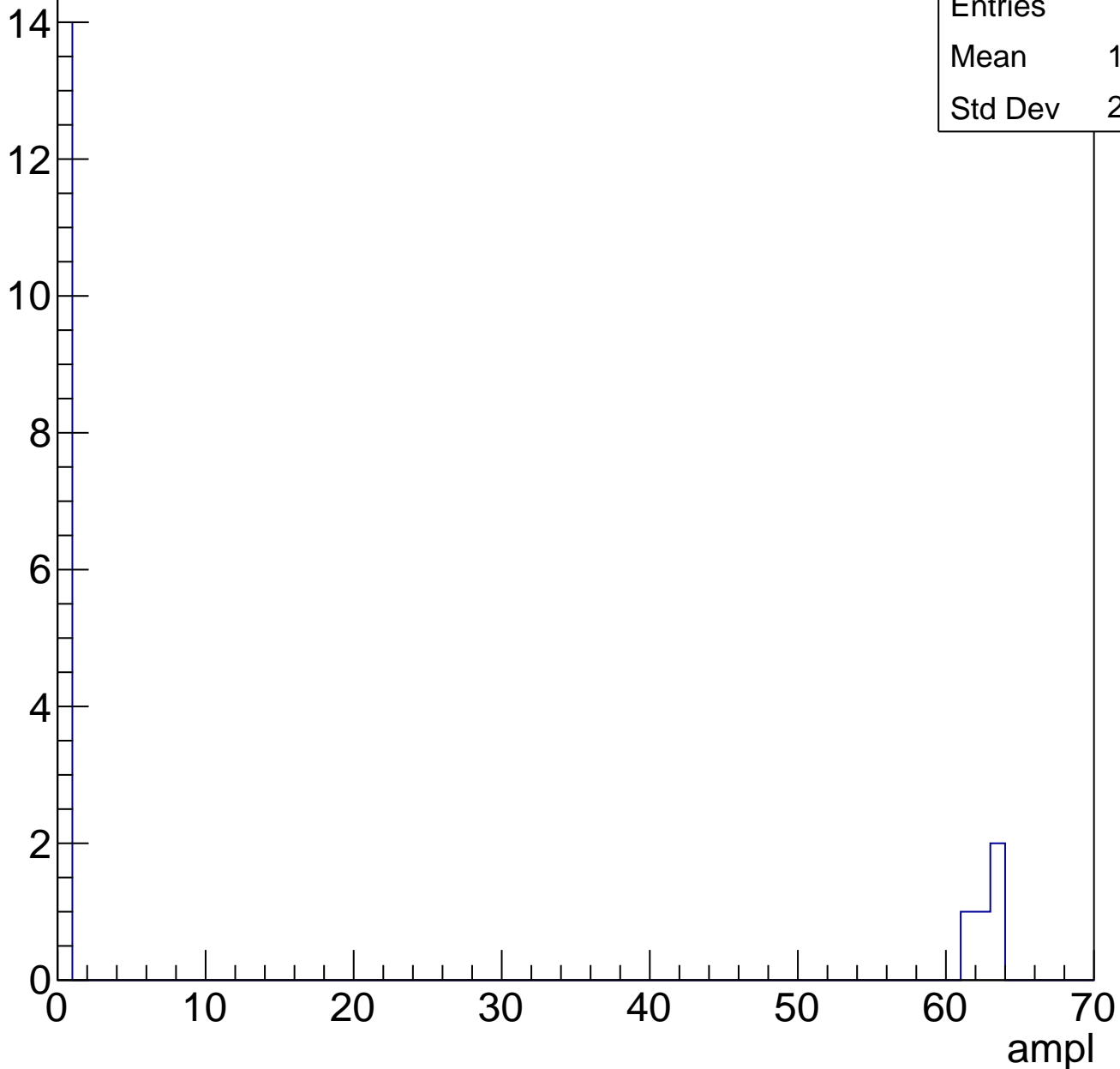
Entries	15
Mean	60.13
Std Dev	1.928

B1L103S, U14-ch90, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	18
Mean	13.83
Std Dev	25.88

Entry

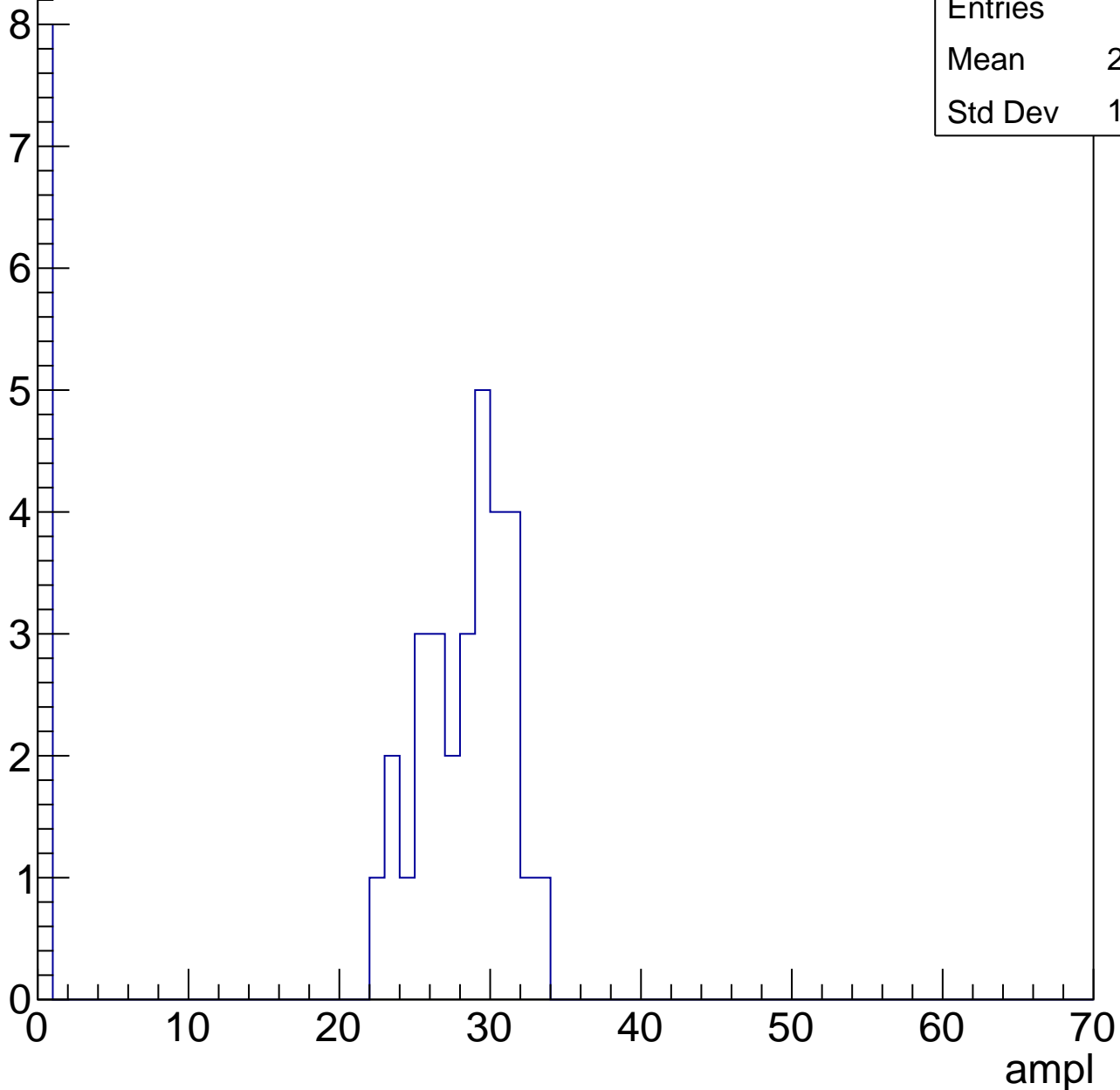


B1L103S, U14-ch91, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	38
Mean	22.03
Std Dev	11.65

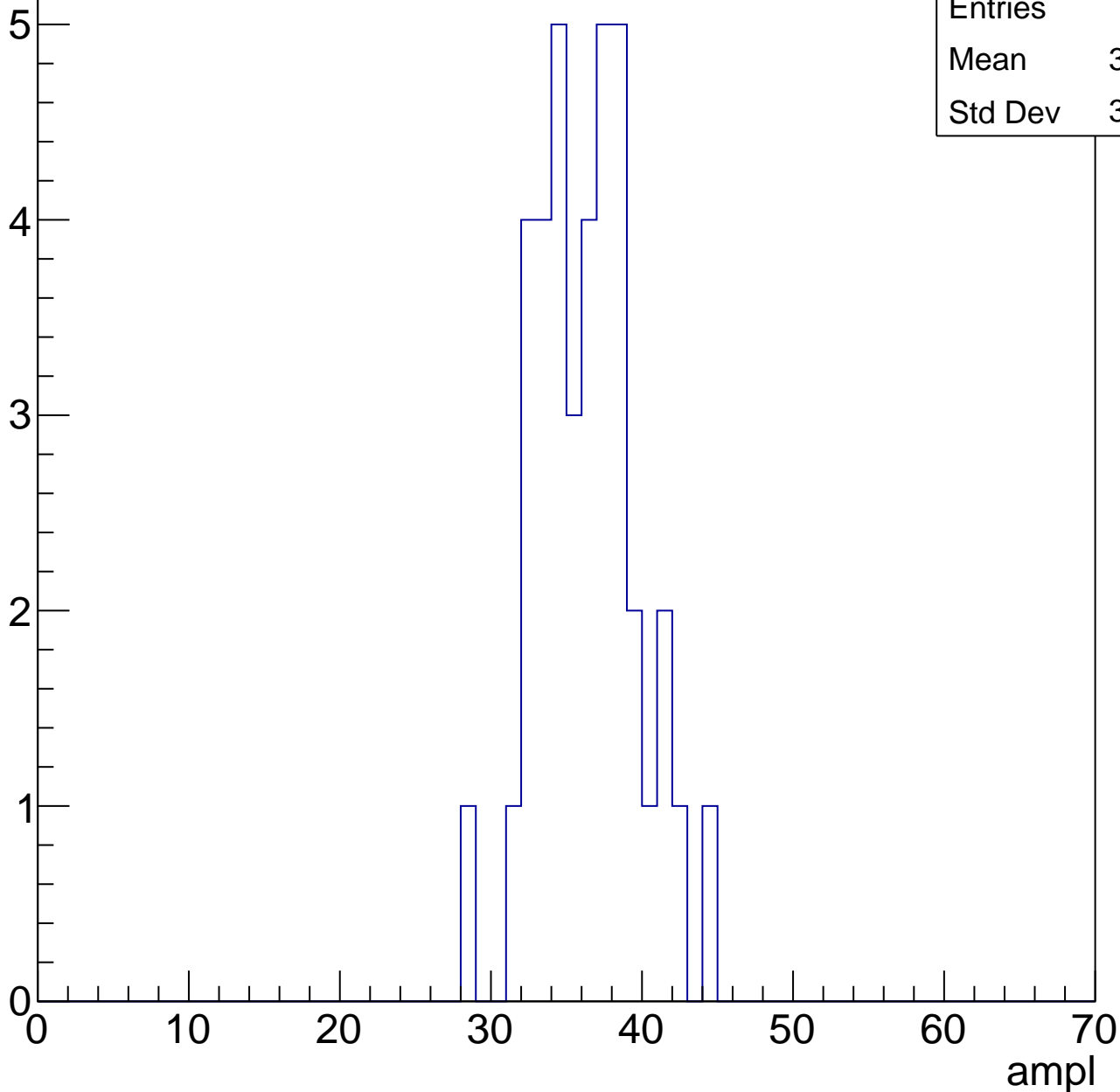


B1L103S, U14-ch91, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

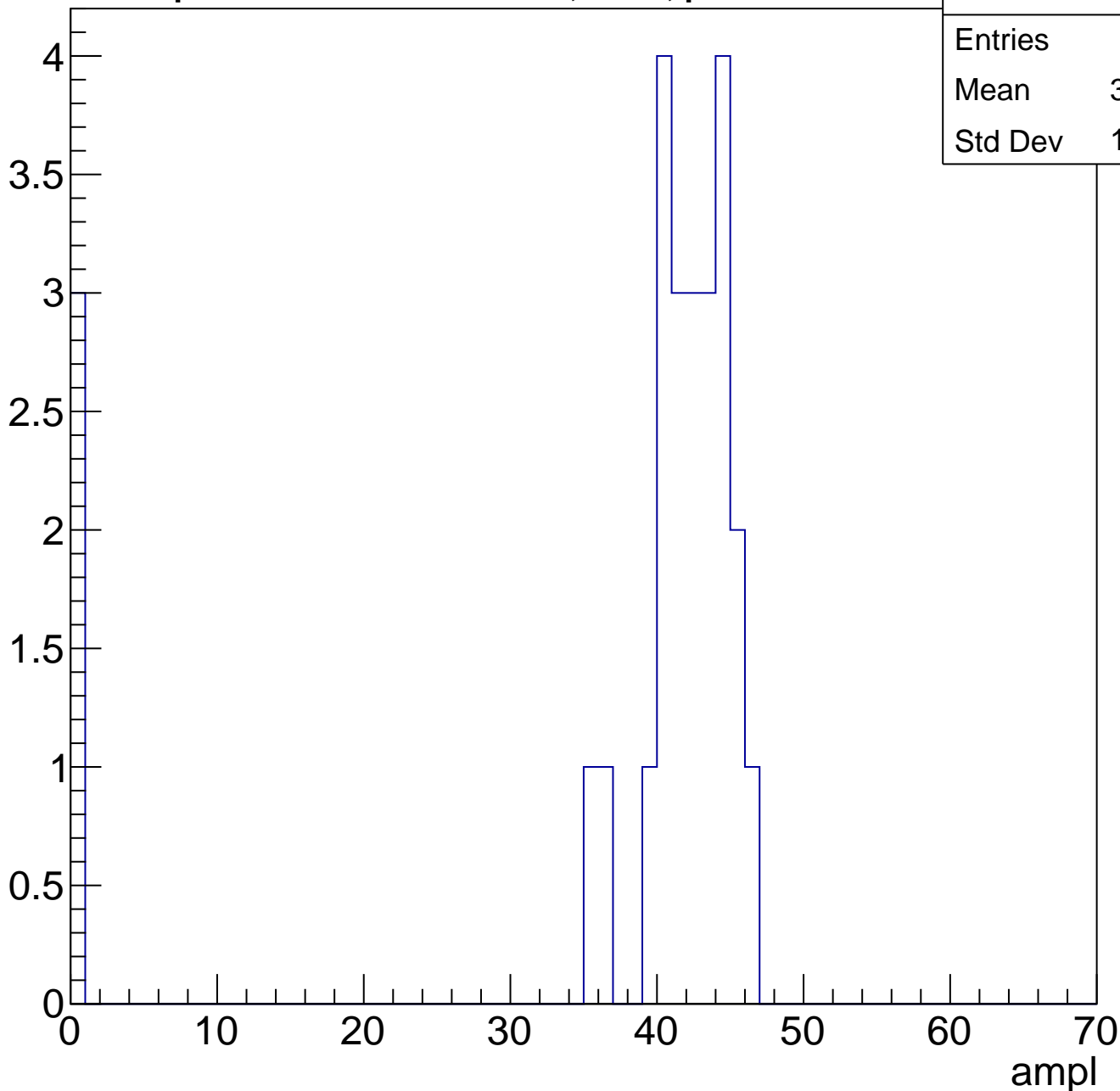
Entries	39
Mean	35.87
Std Dev	3.283



B1L103S, U14-ch91, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry



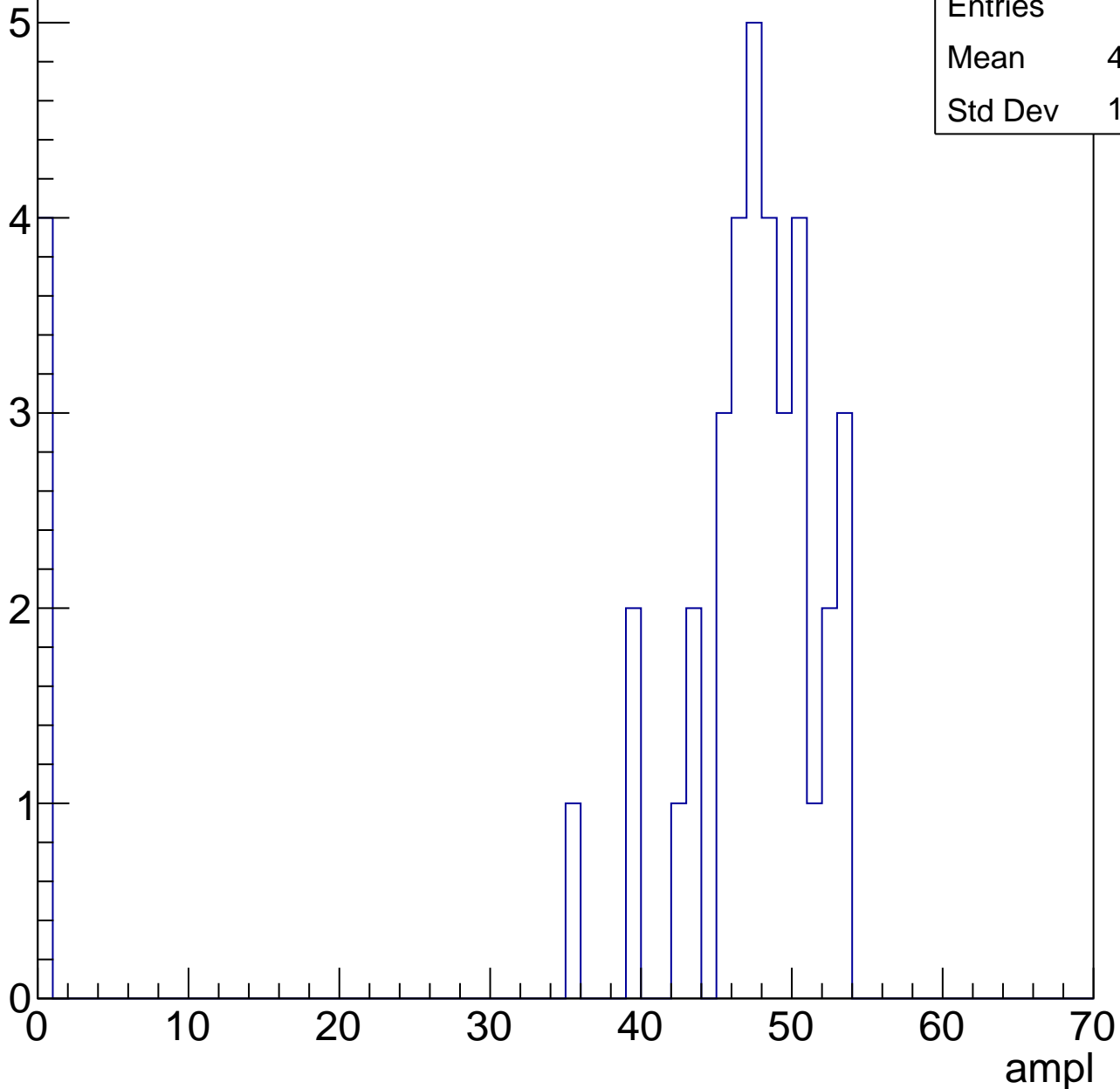
Entries	26
Mean	36.92
Std Dev	13.57

B1L103S, U14-ch91, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	42.26
Std Dev	14.79

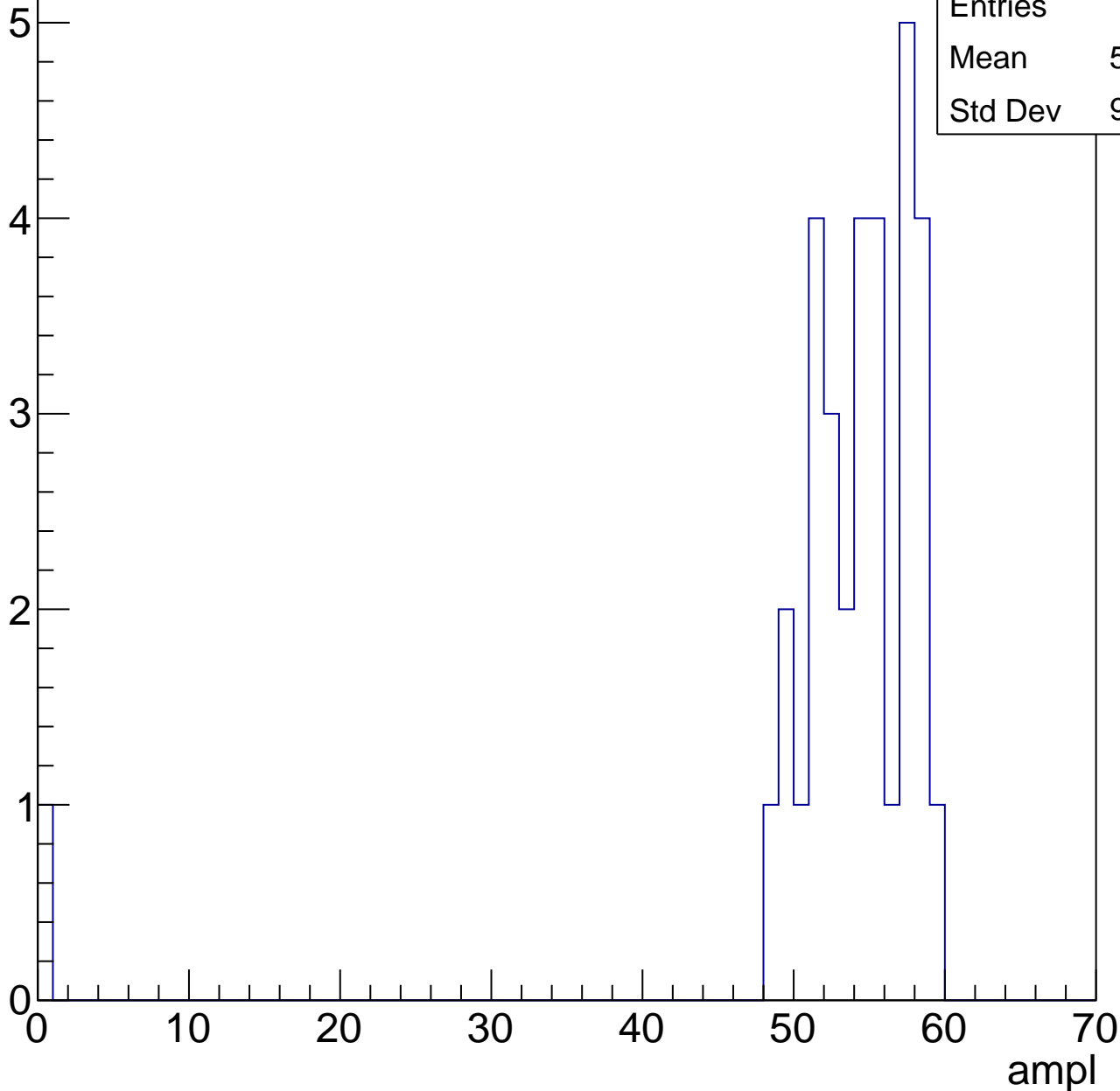


B1L103S, U14-ch91, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	33
Mean	52.42
Std Dev	9.736

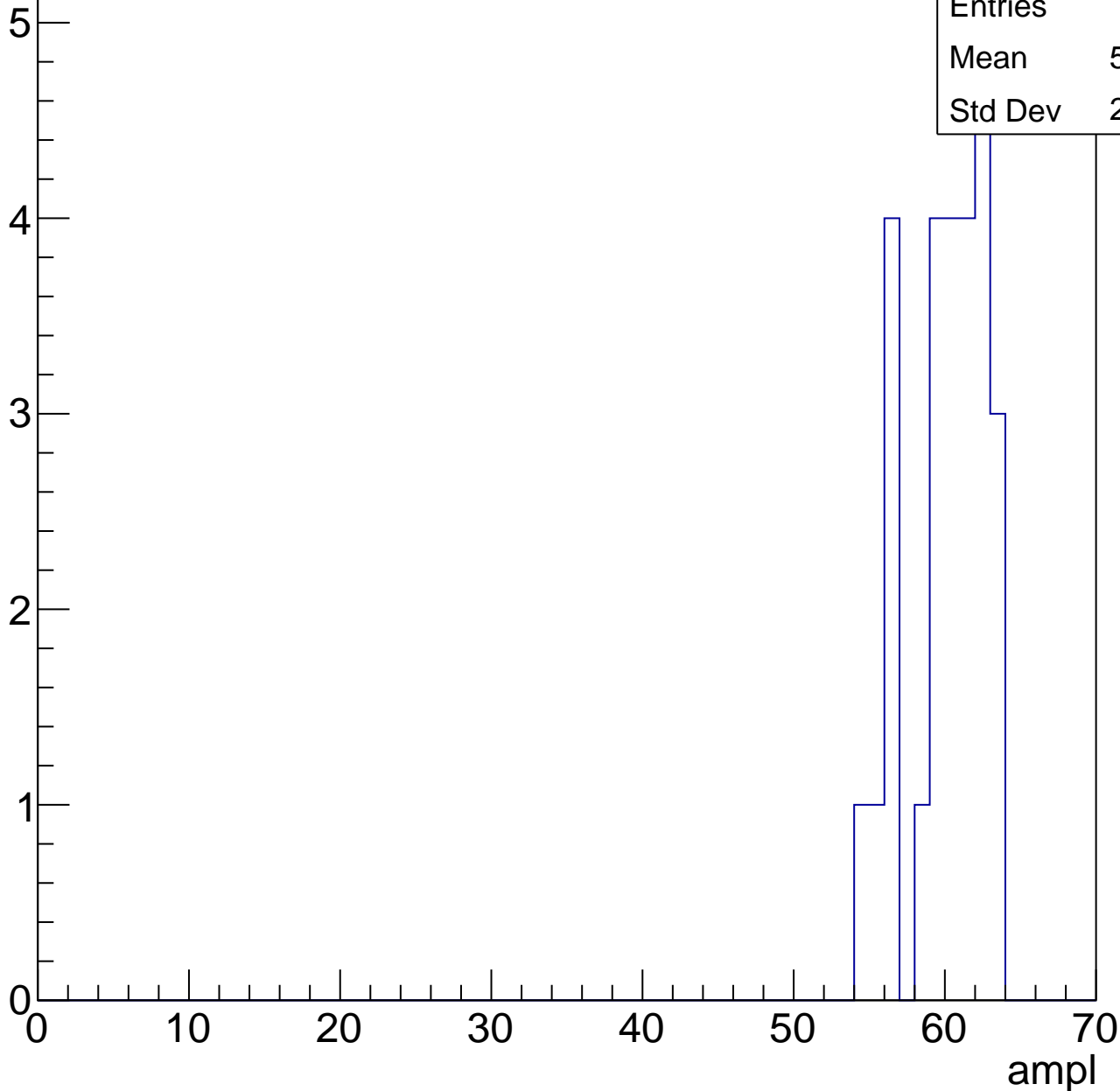


B1L103S, U14-ch91, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	27
Mean	59.63
Std Dev	2.584



B1L103S, U14-ch91, adc6

calib_packv5_041523_1651.root, FC#0, port C2

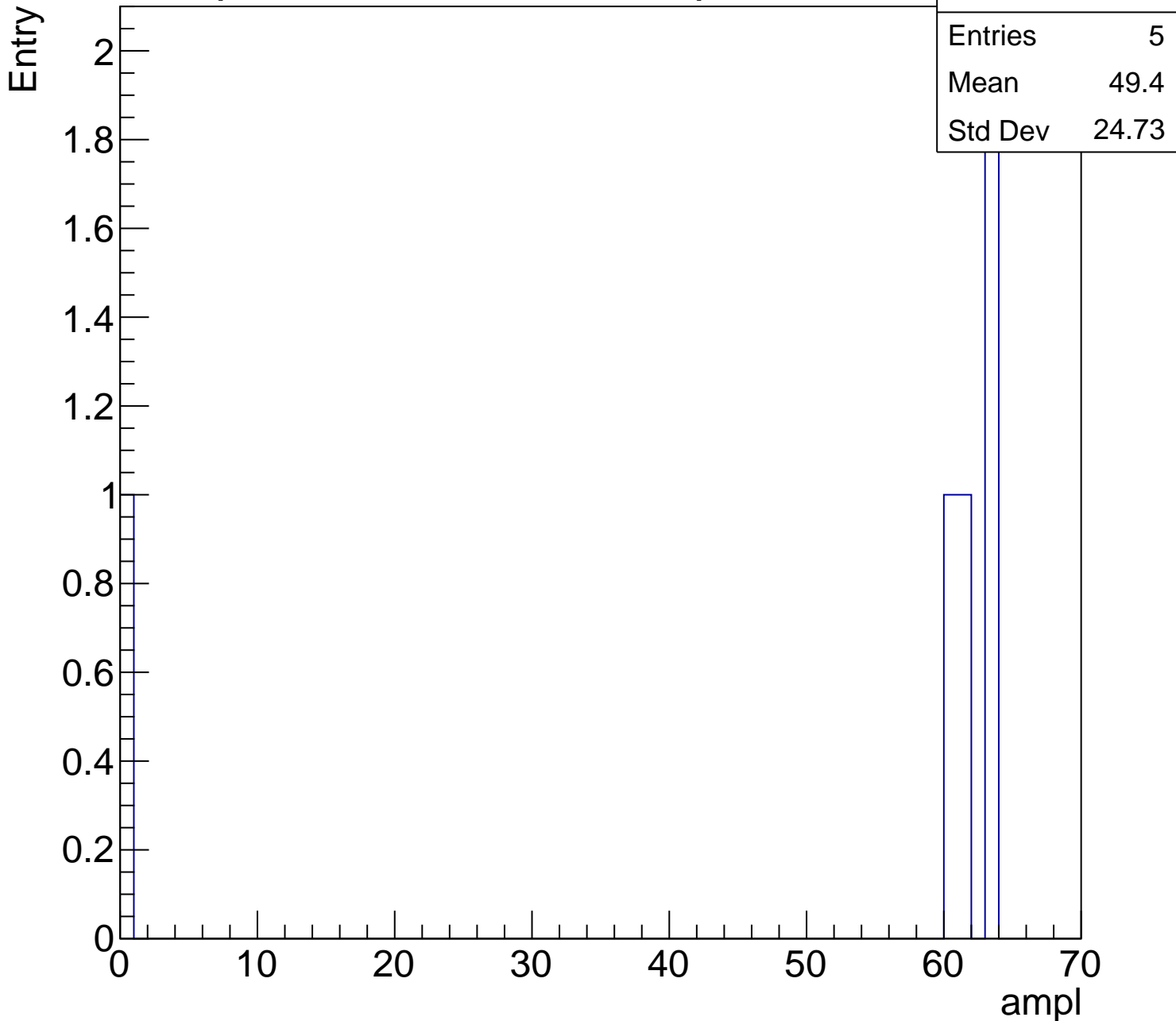
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	5
Mean	49.4
Std Dev	24.73

0 10 20 30 40 50 60 70

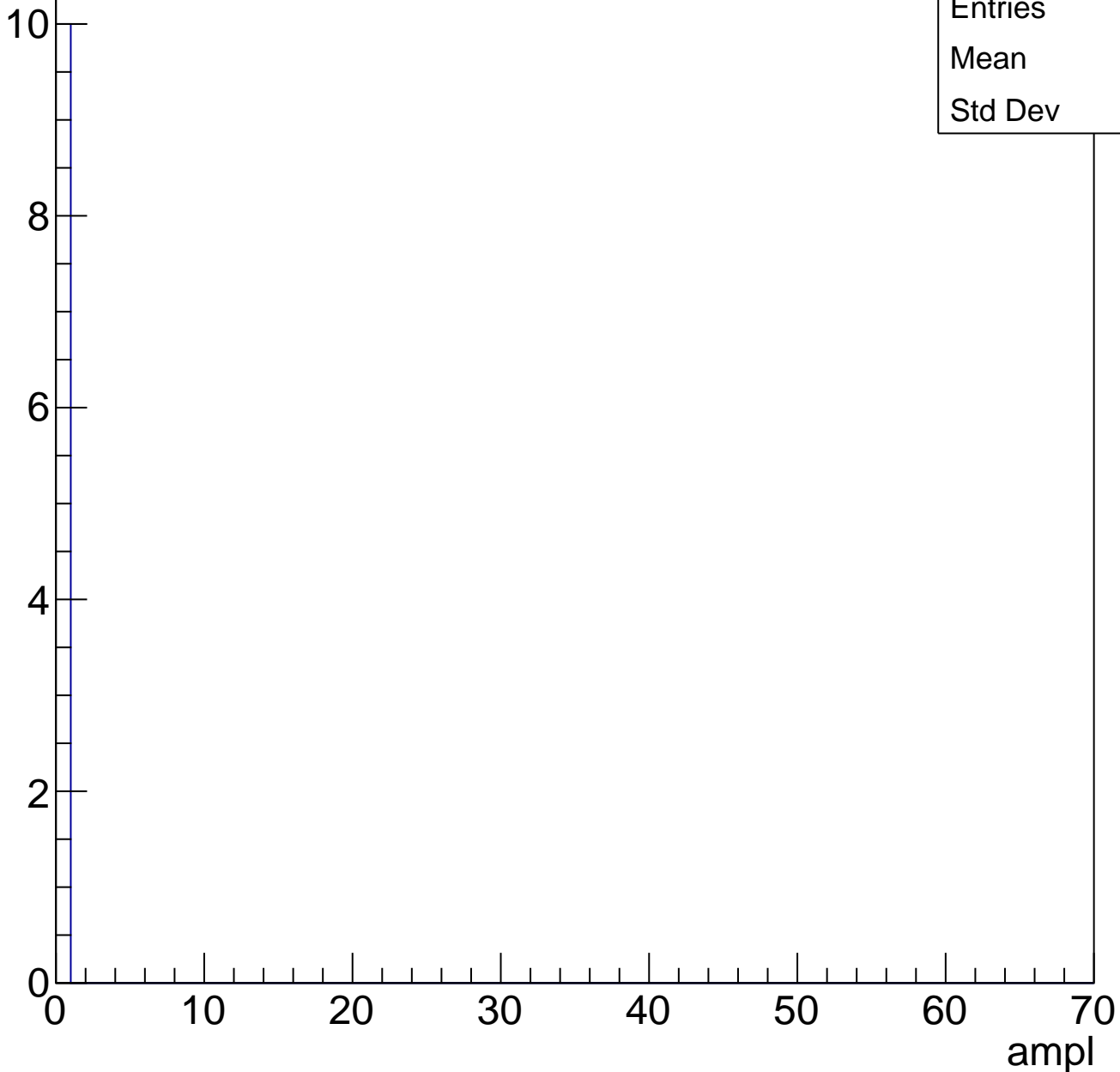
ampl



B1L103S, U14-ch91, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

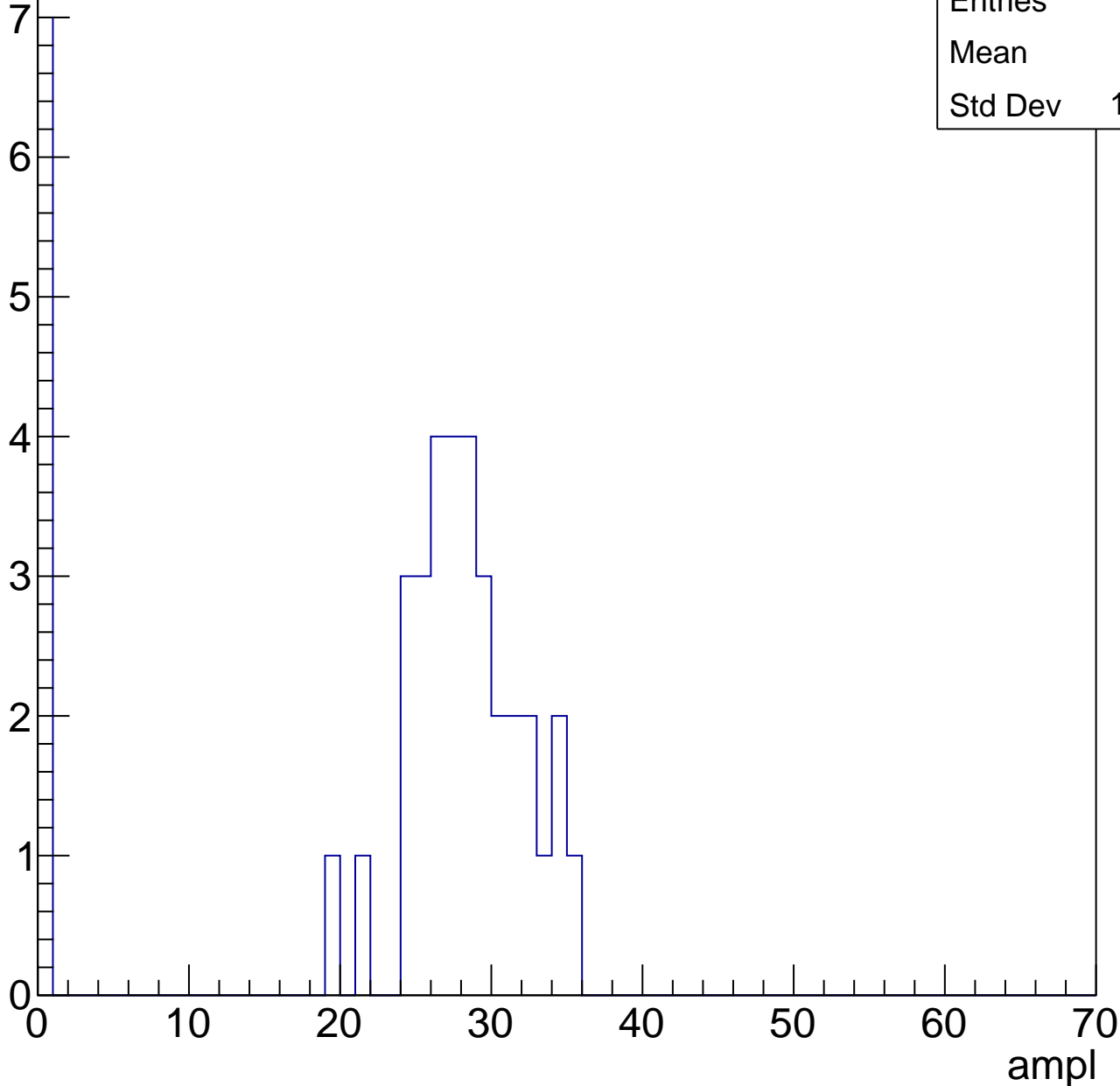


B1L103S, U14-ch92, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	23
Std Dev	11.09

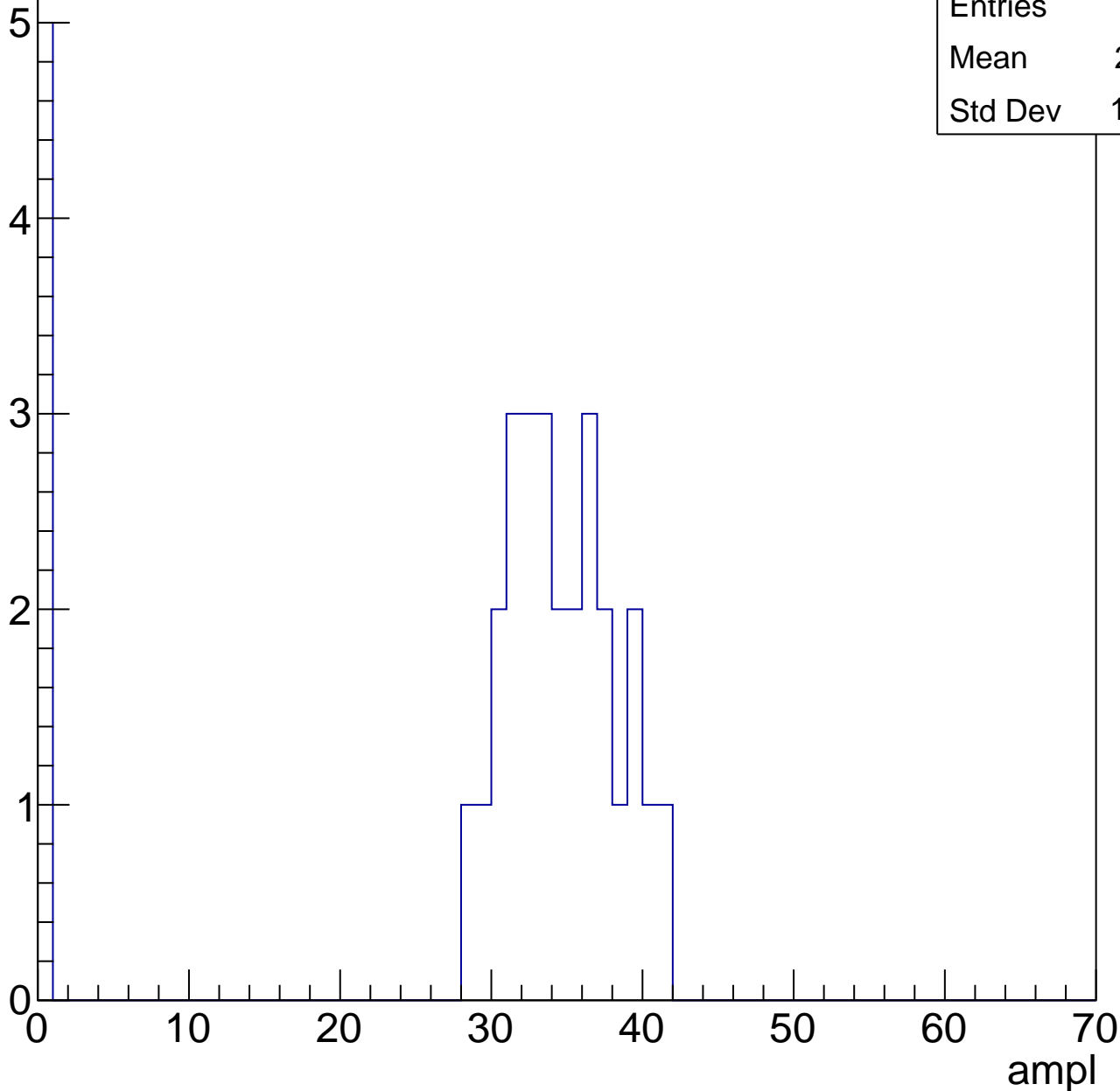


B1L103S, U14-ch92, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	32
Mean	28.81
Std Dev	12.79

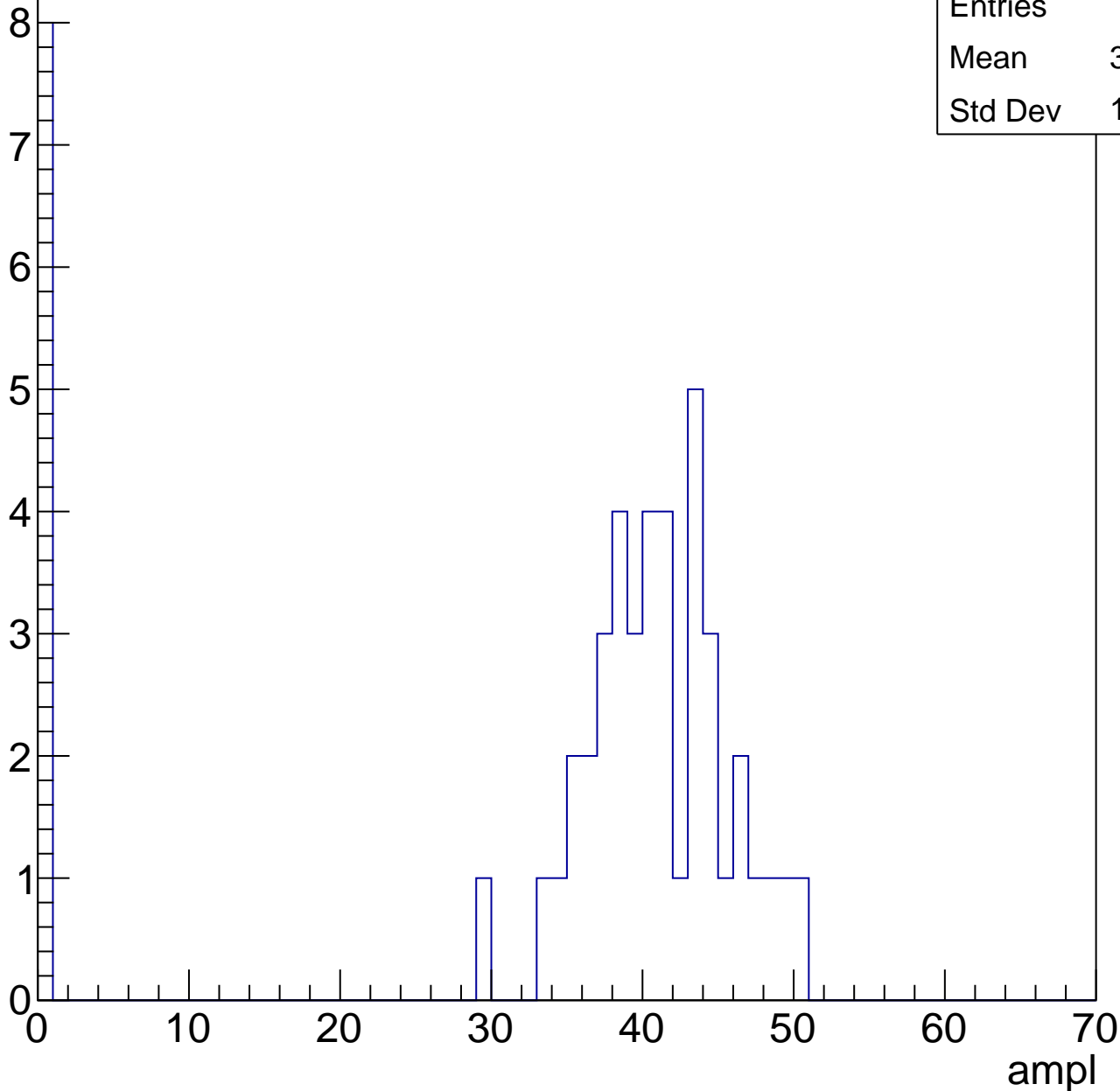


B1L103S, U14-ch92, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

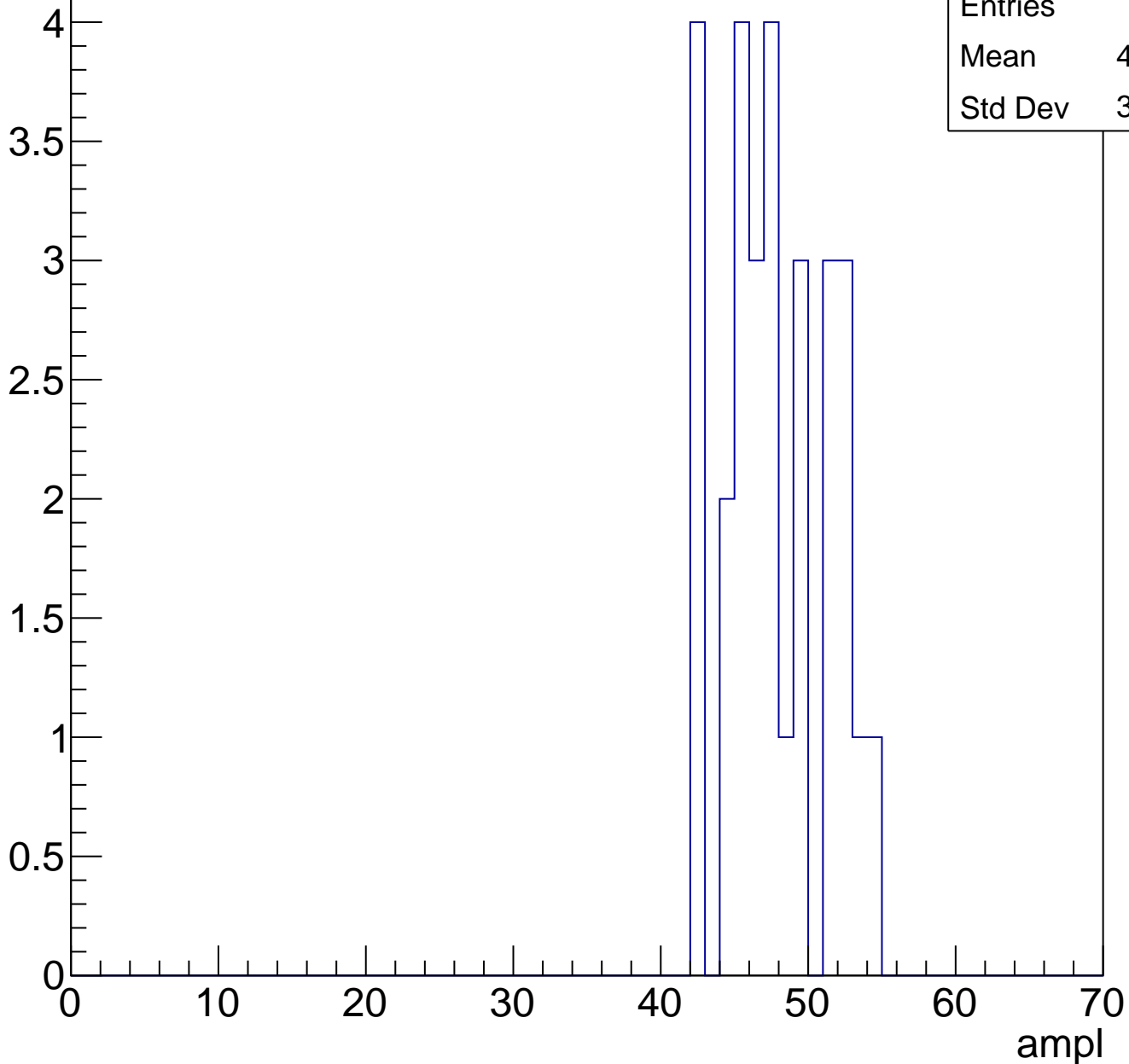
Entries	49
Mean	33.92
Std Dev	15.53



B1L103S, U14-ch92, adc3

calib_packv5_041523_1651.root, FC#0, port C2

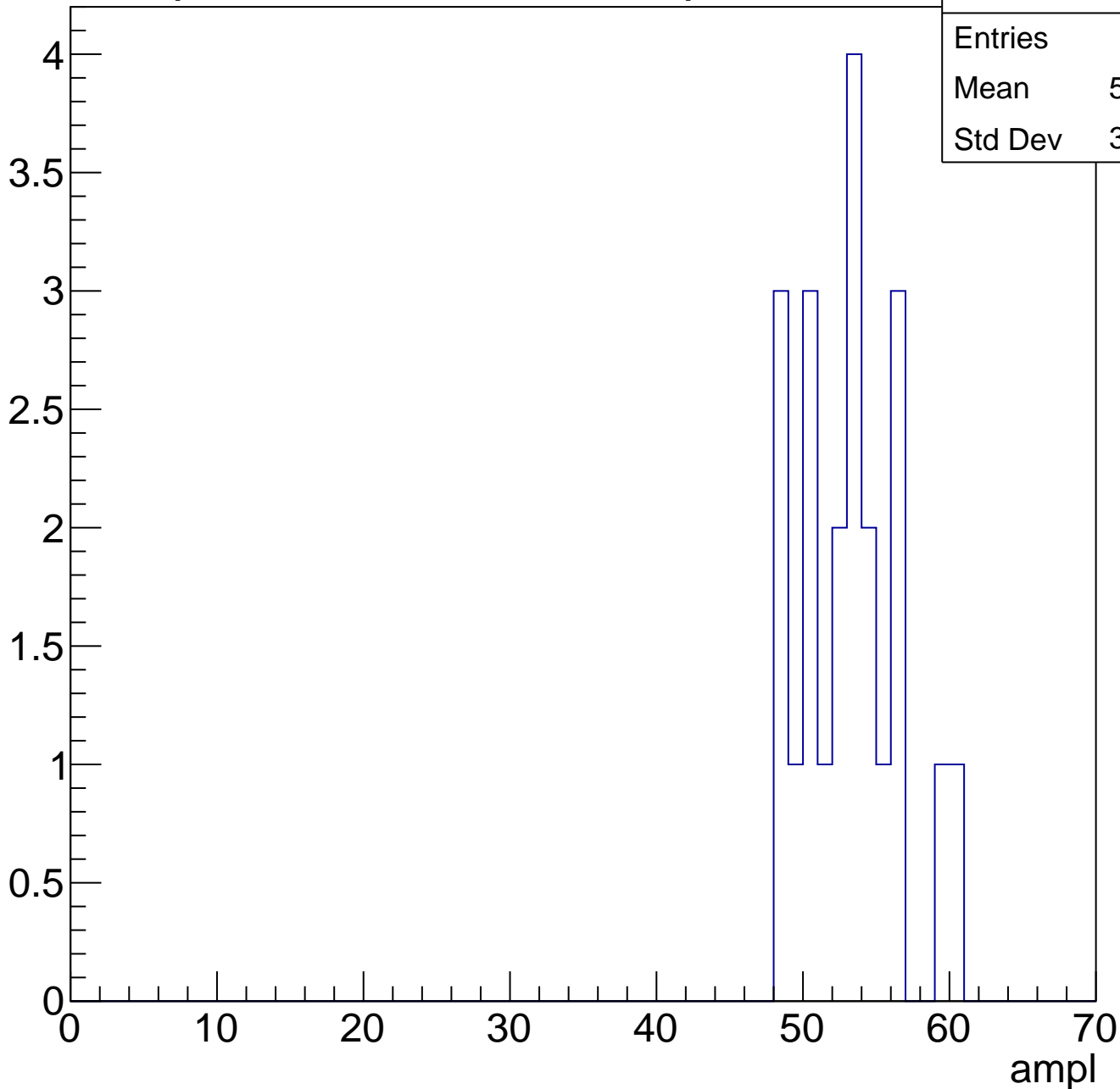
Entry



B1L103S, U14-ch92, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch92, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

5

4

3

2

1

0

Entries

27

Mean

57.15

Std Dev

2.915

0

10

20

30

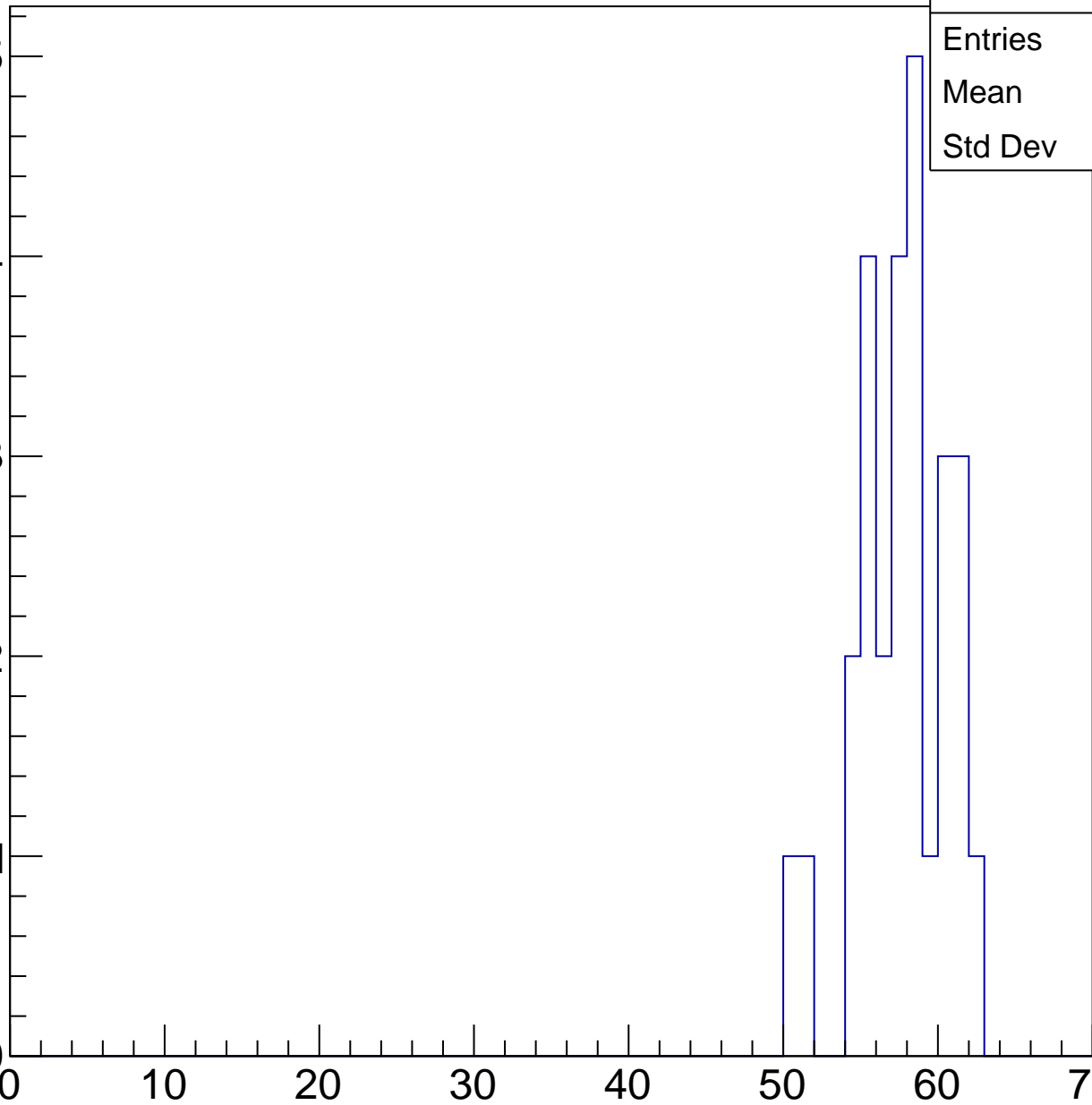
40

50

60

70

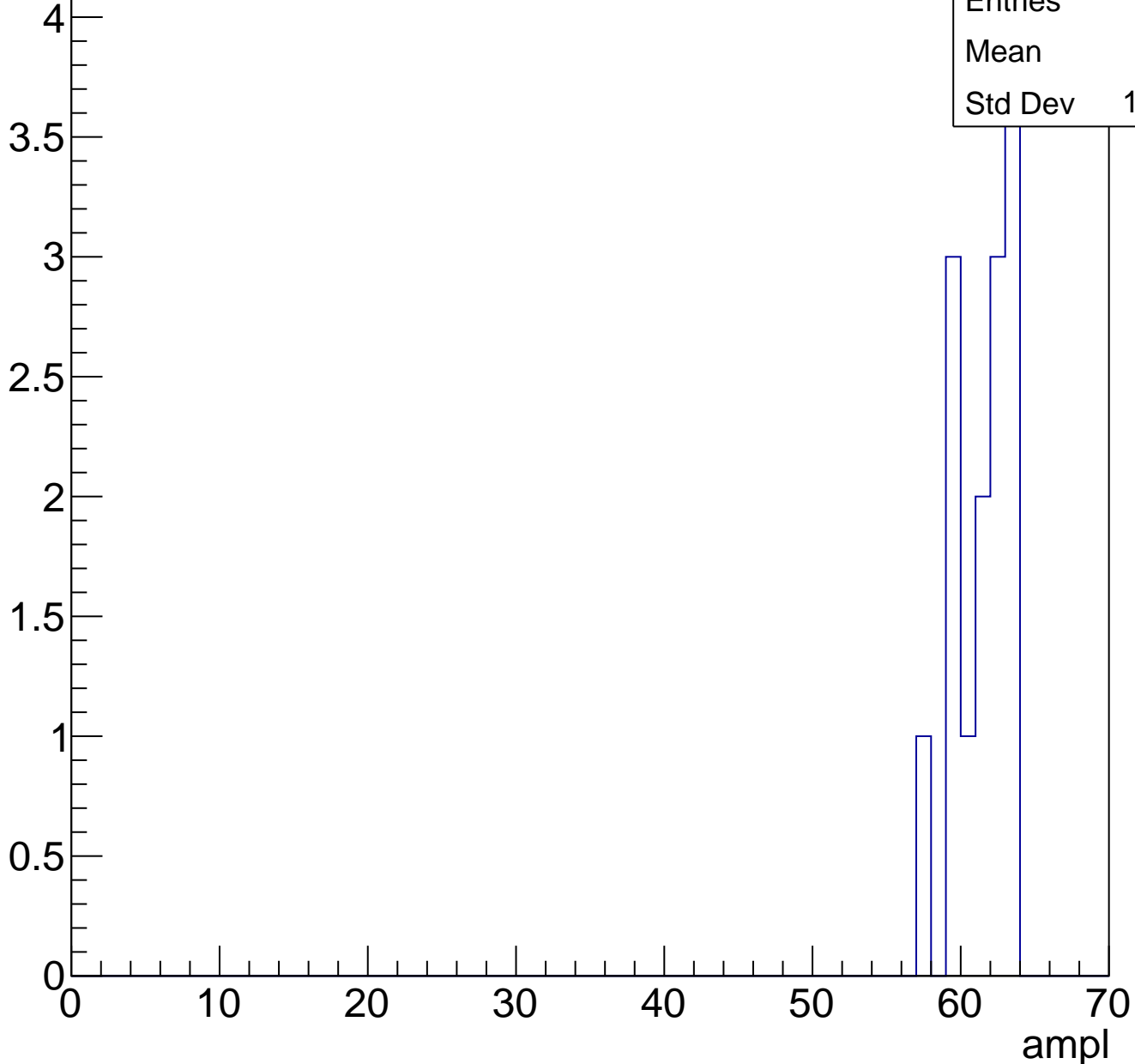
ampl



B1L103S, U14-ch92, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

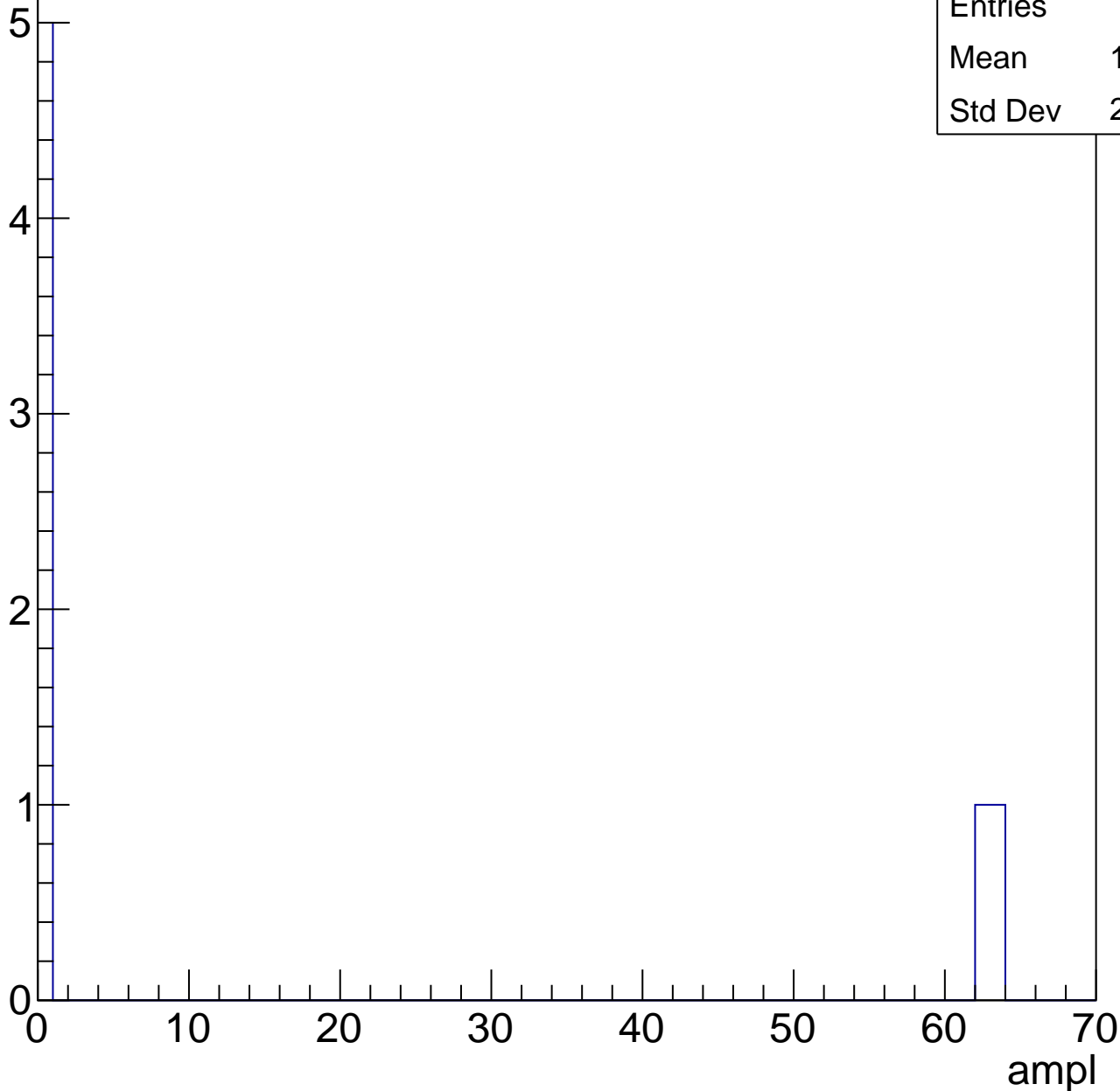


B1L103S, U14-ch92, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	7
Mean	17.86
Std Dev	28.24

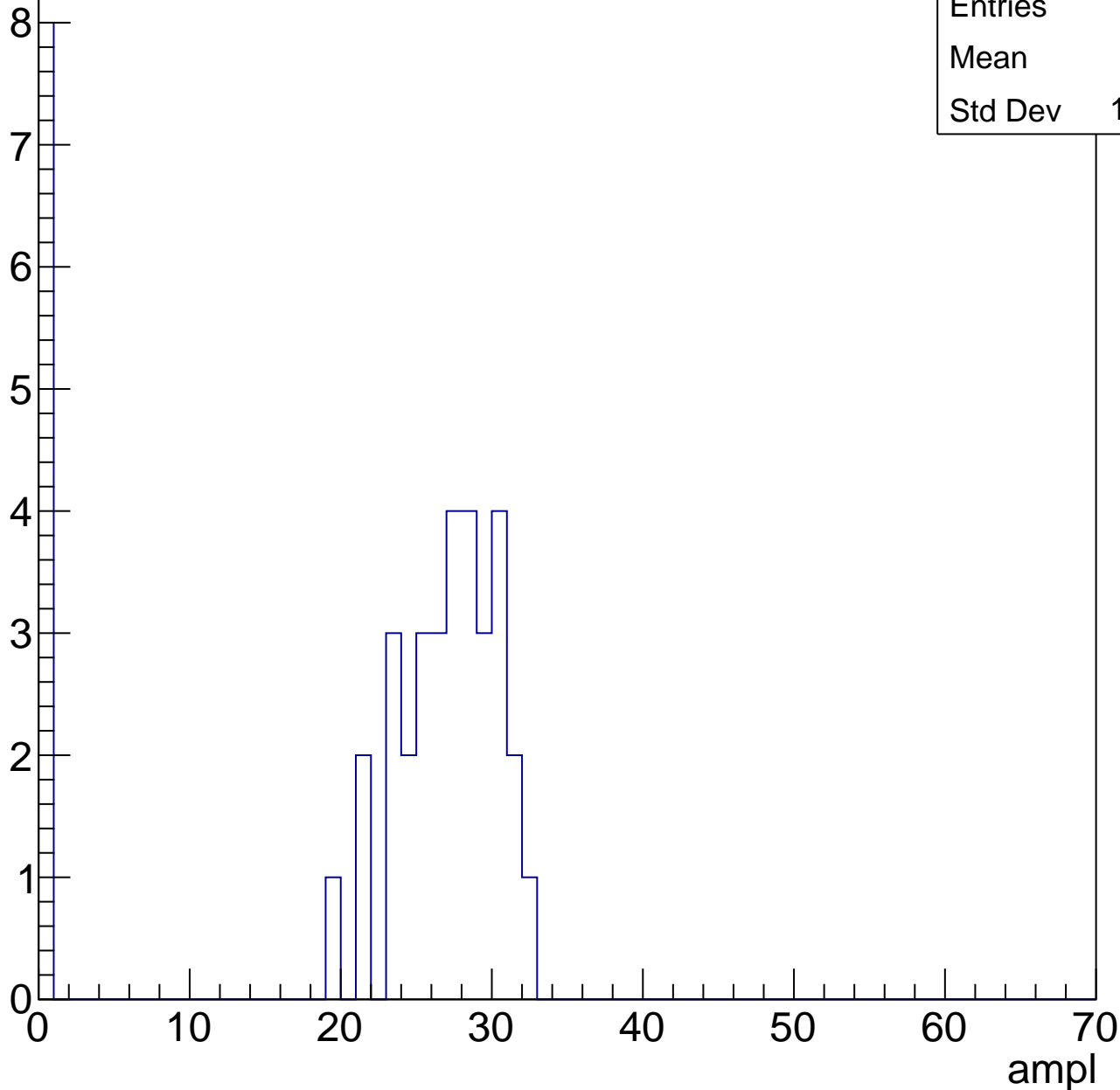


B1L103S, U14-ch93, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	21.3
Std Dev	11.02

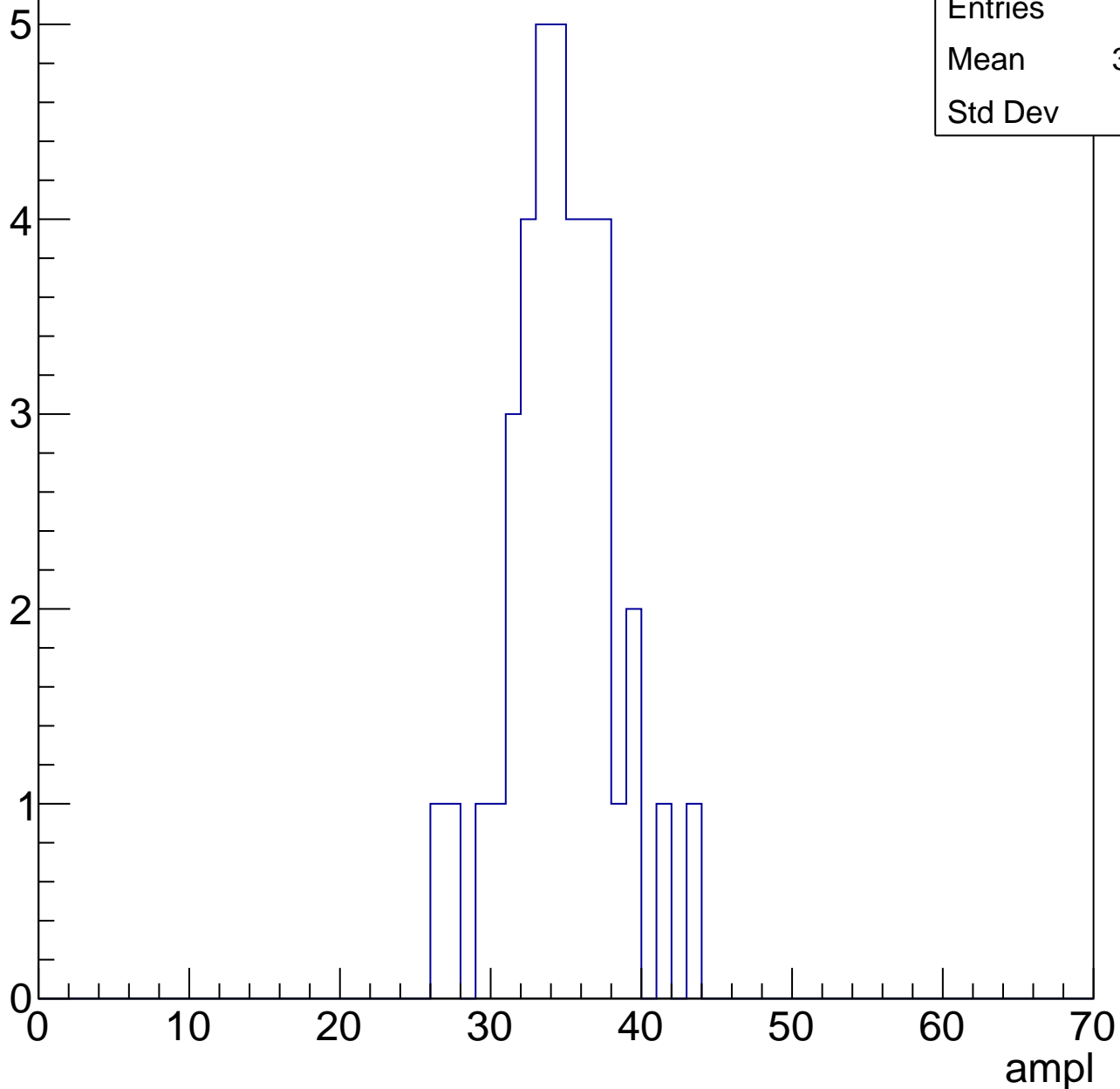


B1L103S, U14-ch93, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	38
Mean	34.21
Std Dev	3.45

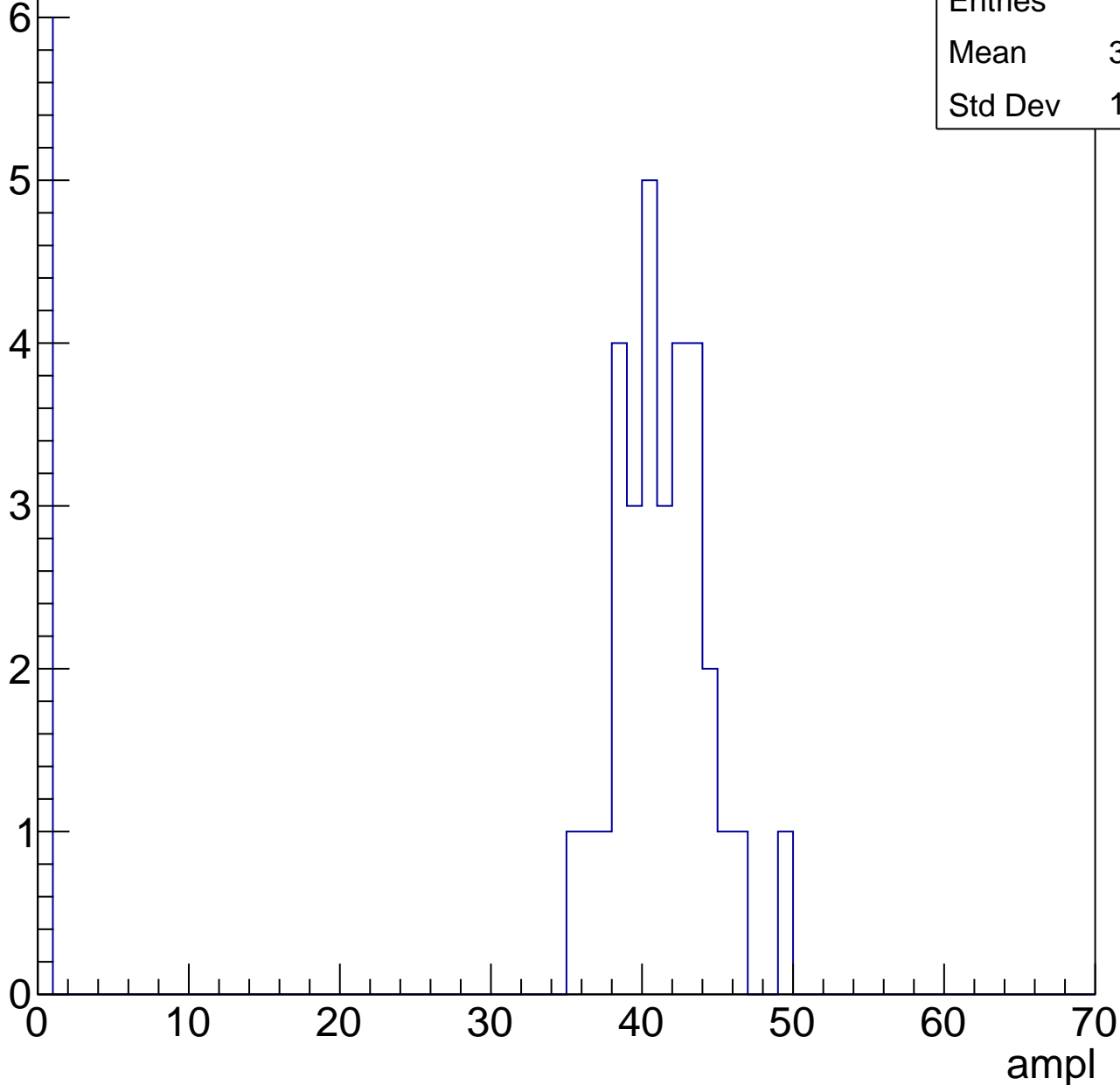


B1L103S, U14-ch93, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	37
Mean	34.27
Std Dev	15.32

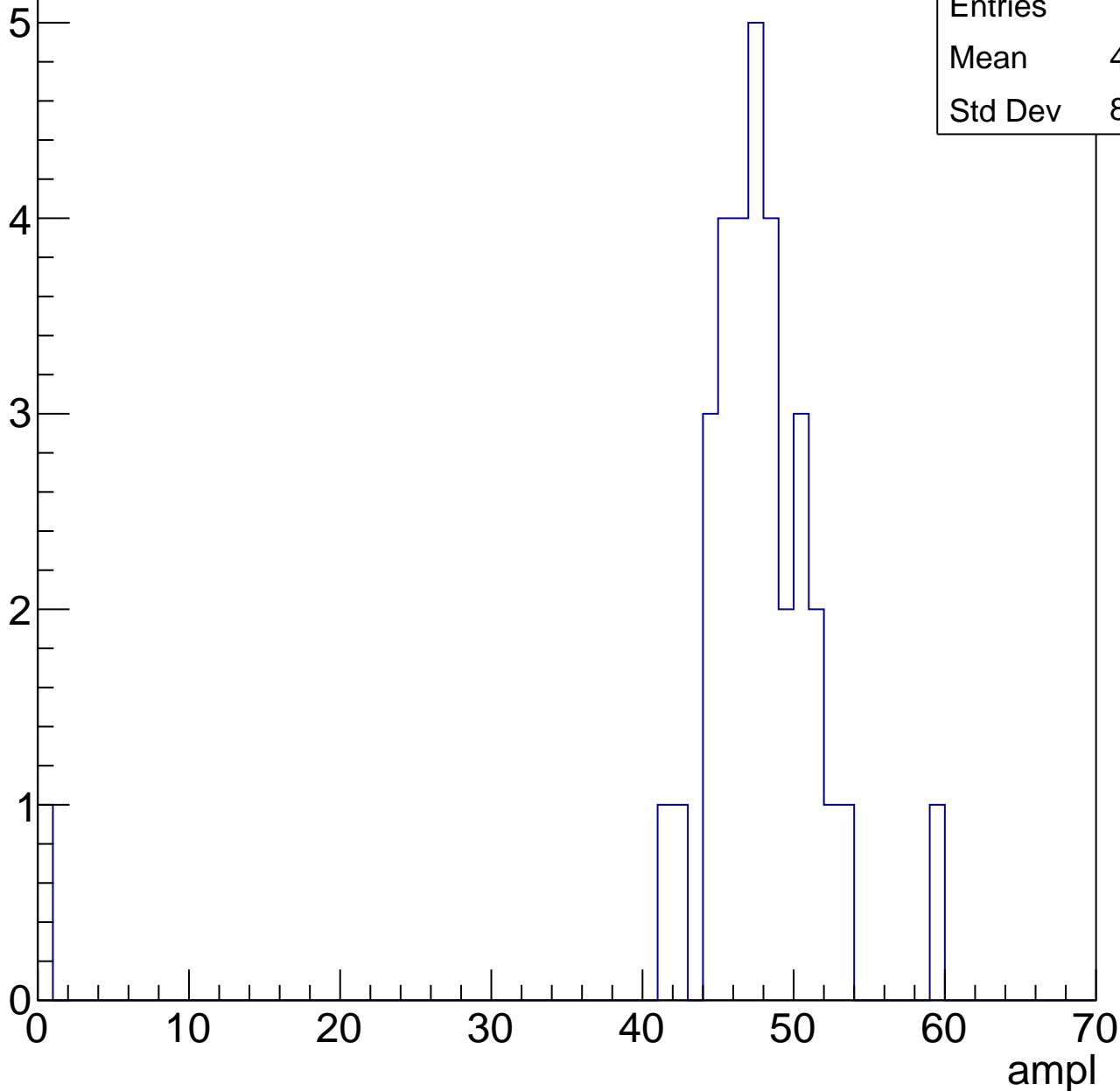


B1L103S, U14-ch93, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

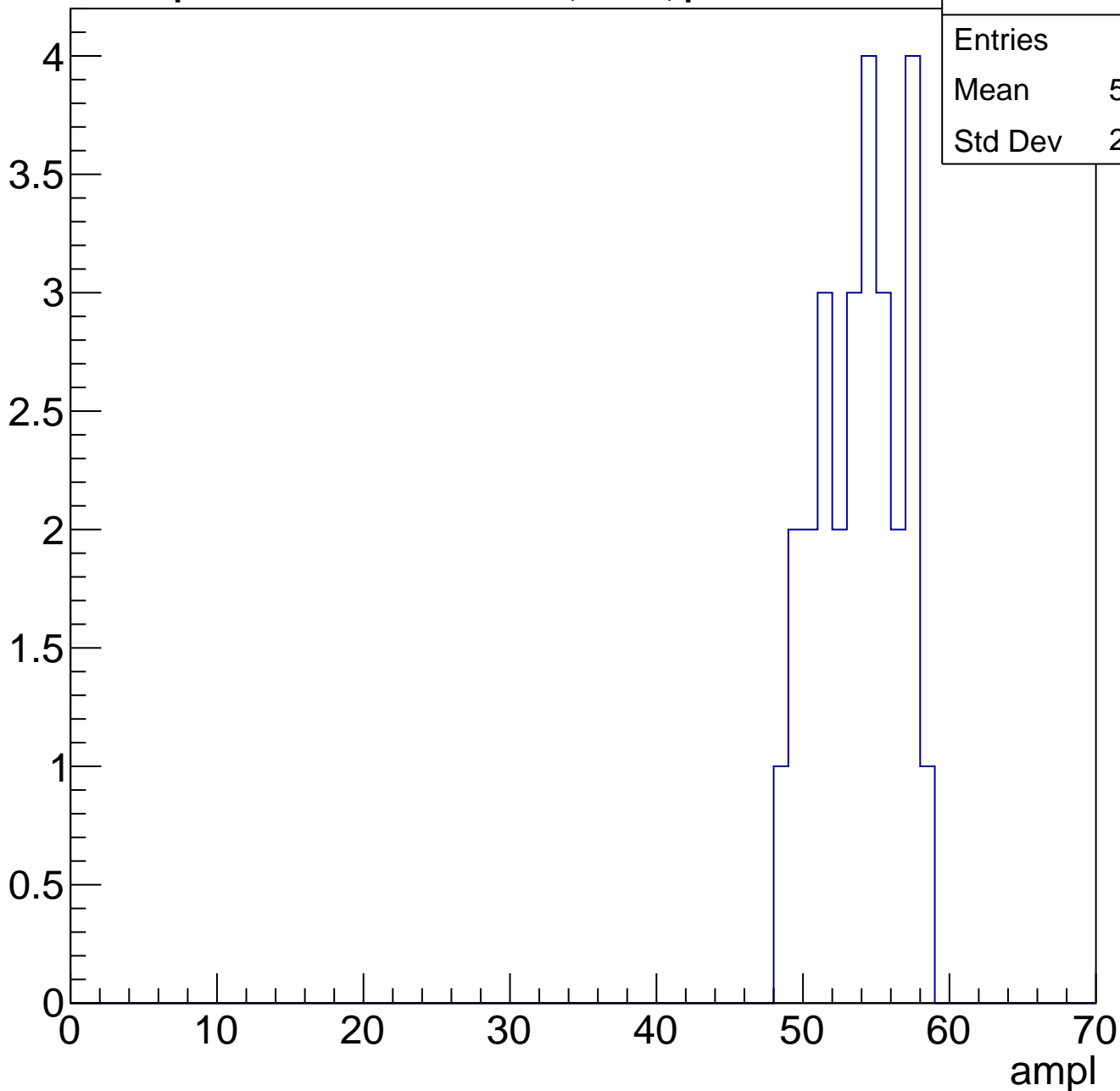
Entries	33
Mean	46.06
Std Dev	8.814



B1L103S, U14-ch93, adc4

calib_packv5_041523_1651.root, FC#0, port C2

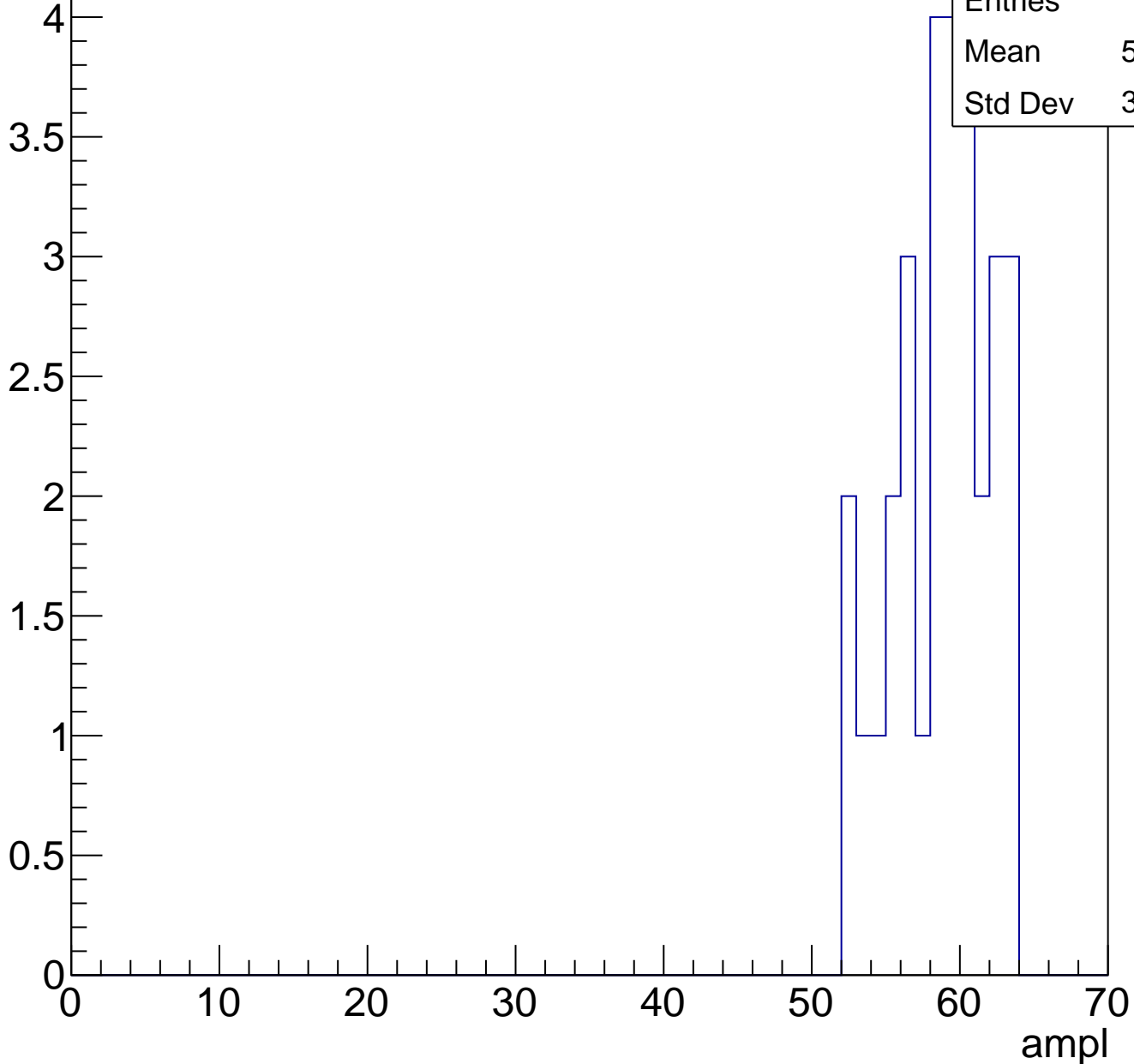
Entry



B1L103S, U14-ch93, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	30
Mean	58.37
Std Dev	3.167

B1L103S, U14-ch93, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

8

Mean

61.62

Std Dev

0.9922

B1L103S, U14-ch93, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

12

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

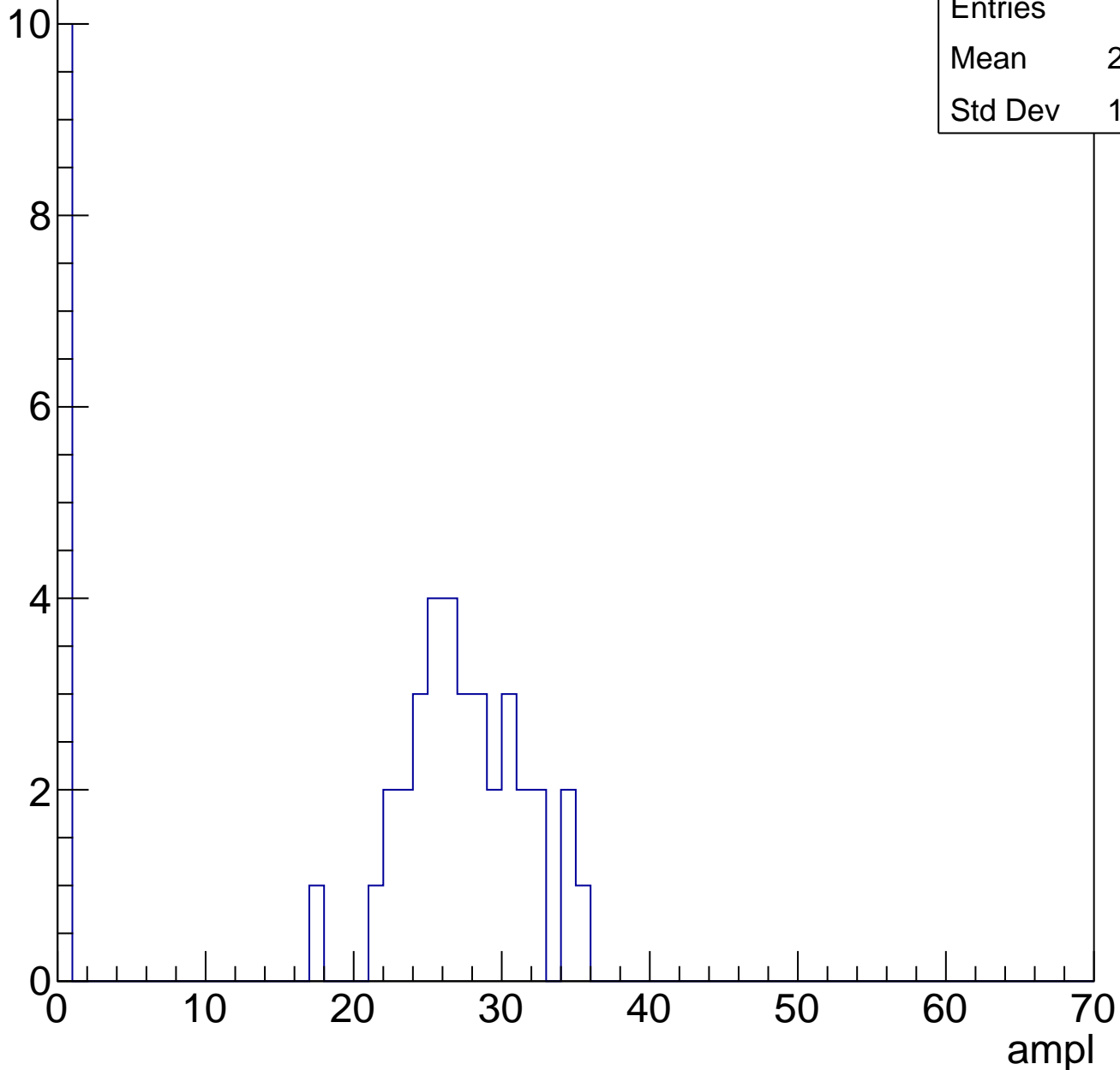
Entries	12
Mean	0
Std Dev	0

B1L103S, U14-ch94, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	45
Mean	21.02
Std Dev	11.77

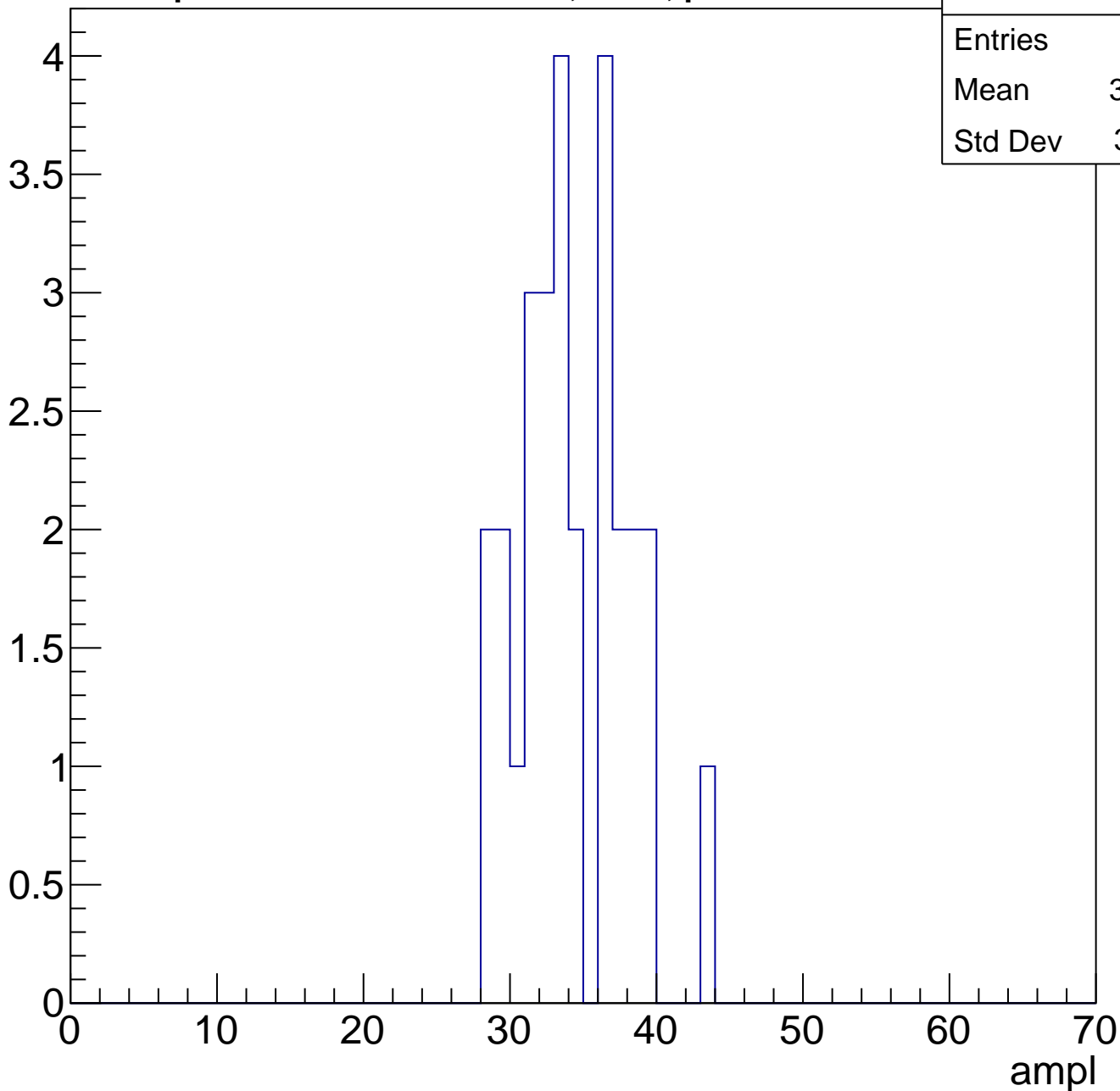
Entry



B1L103S, U14-ch94, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

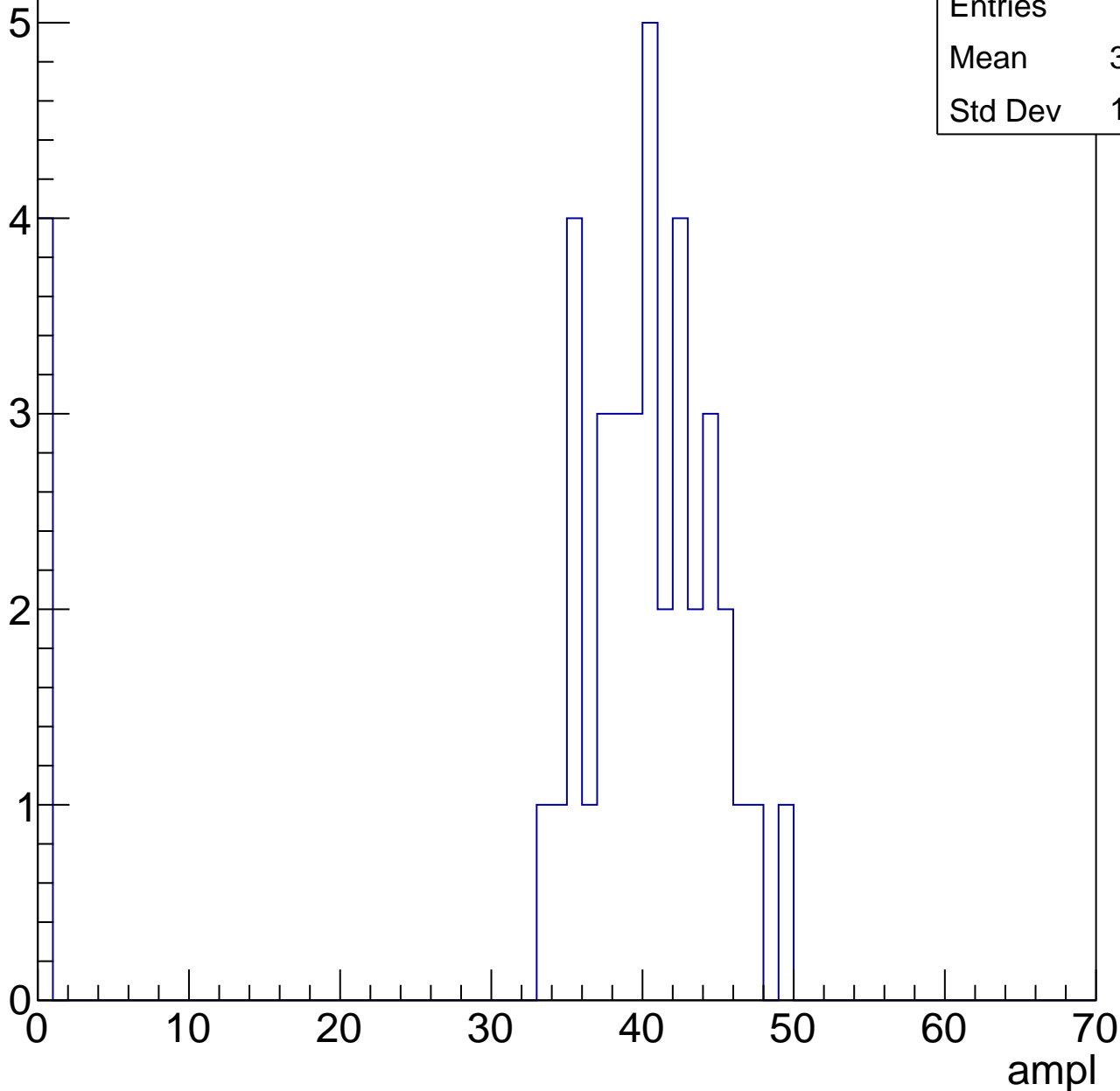


B1L103S, U14-ch94, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	41
Mean	36.22
Std Dev	12.45

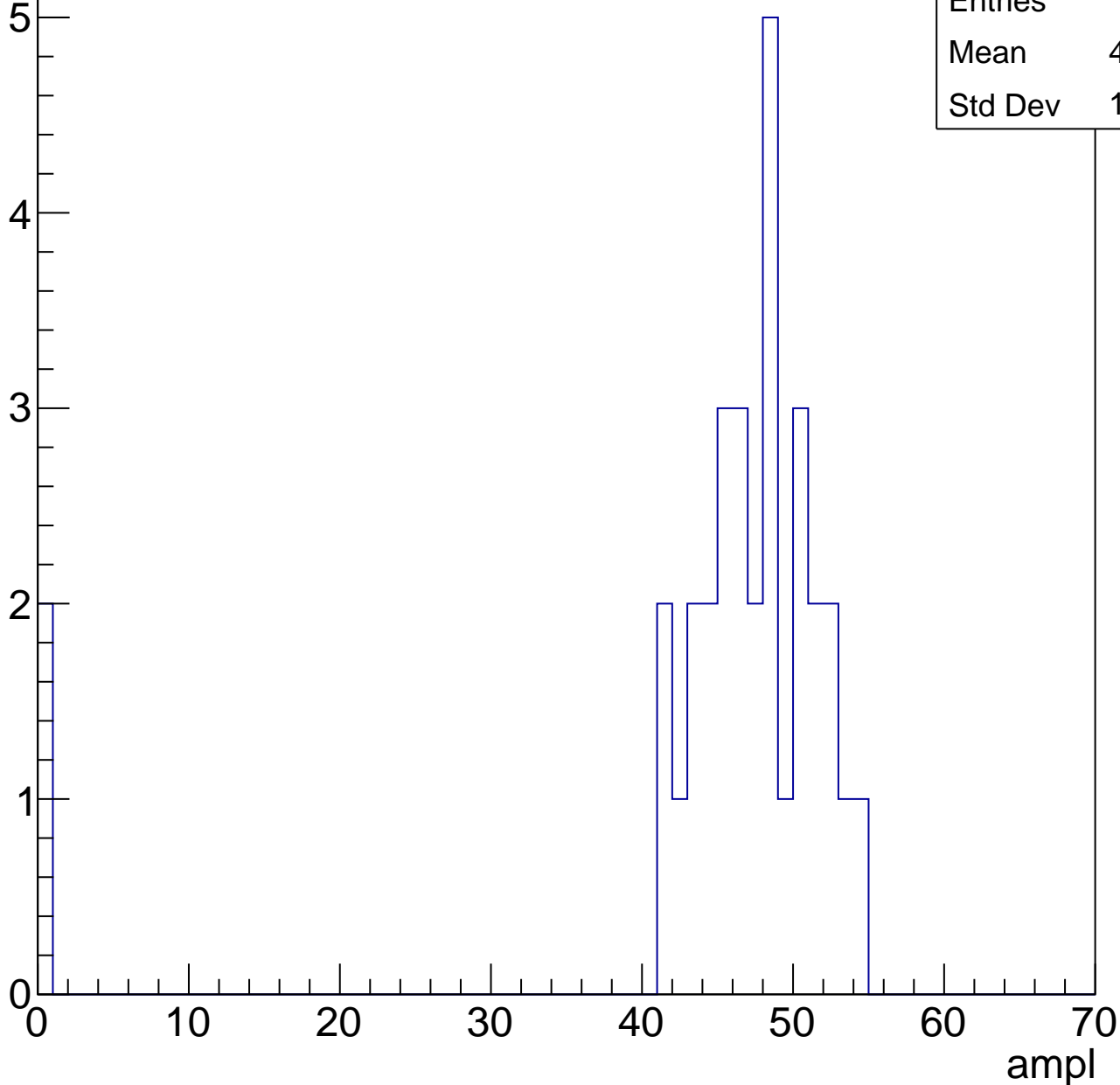


B1L103S, U14-ch94, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

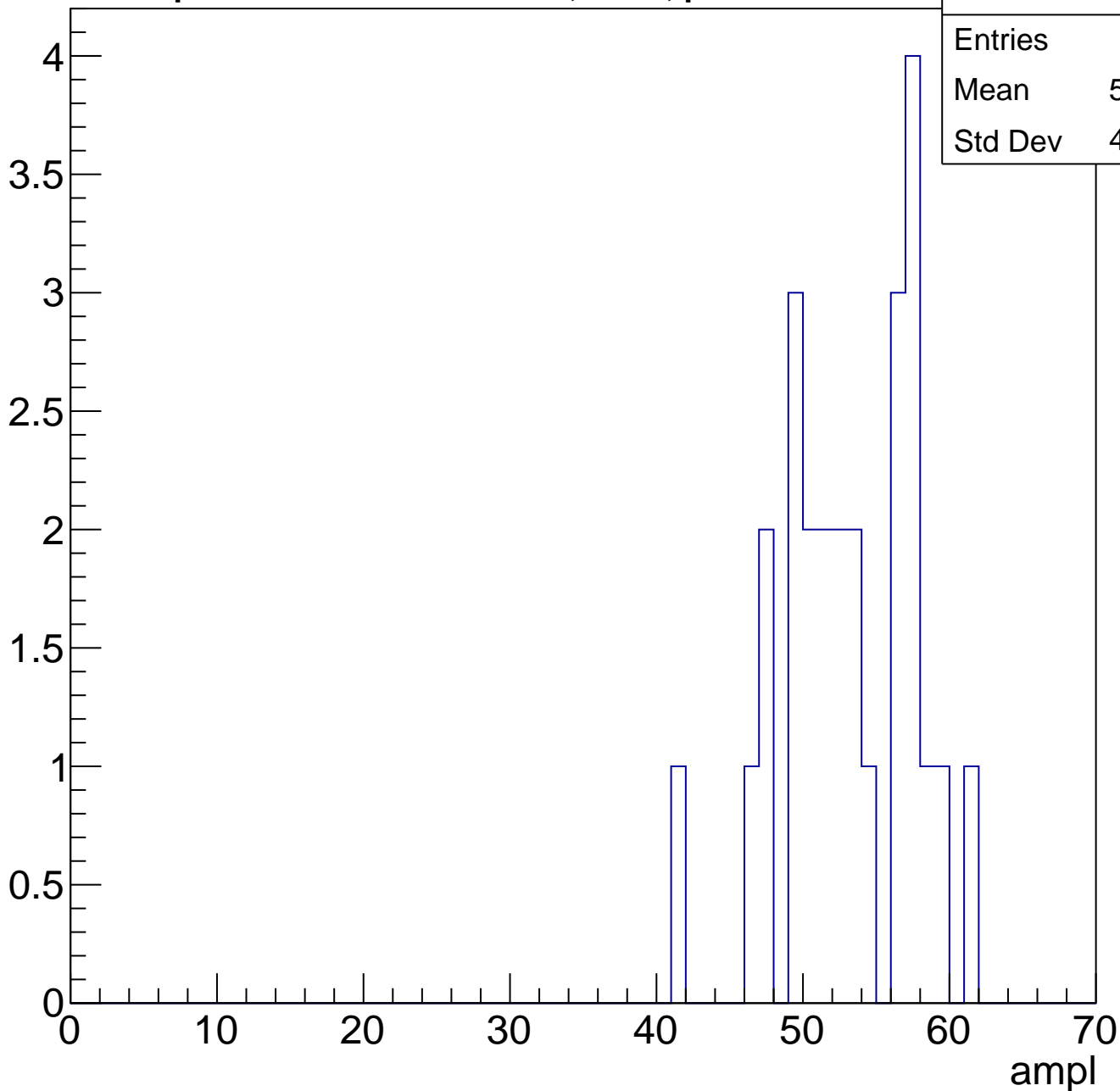
Entries	32
Mean	44.28
Std Dev	11.92



B1L103S, U14-ch94, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

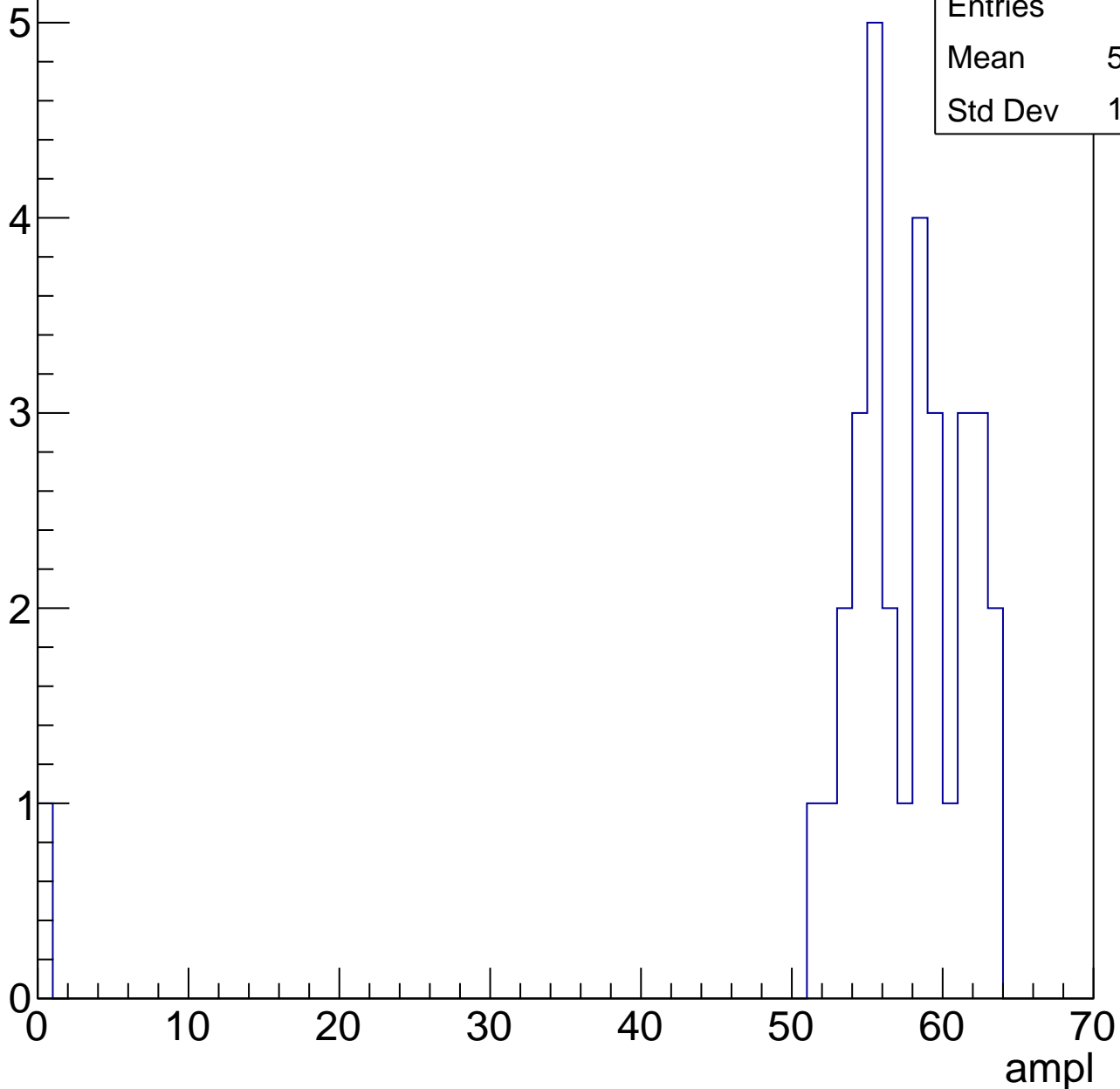


B1L103S, U14-ch94, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

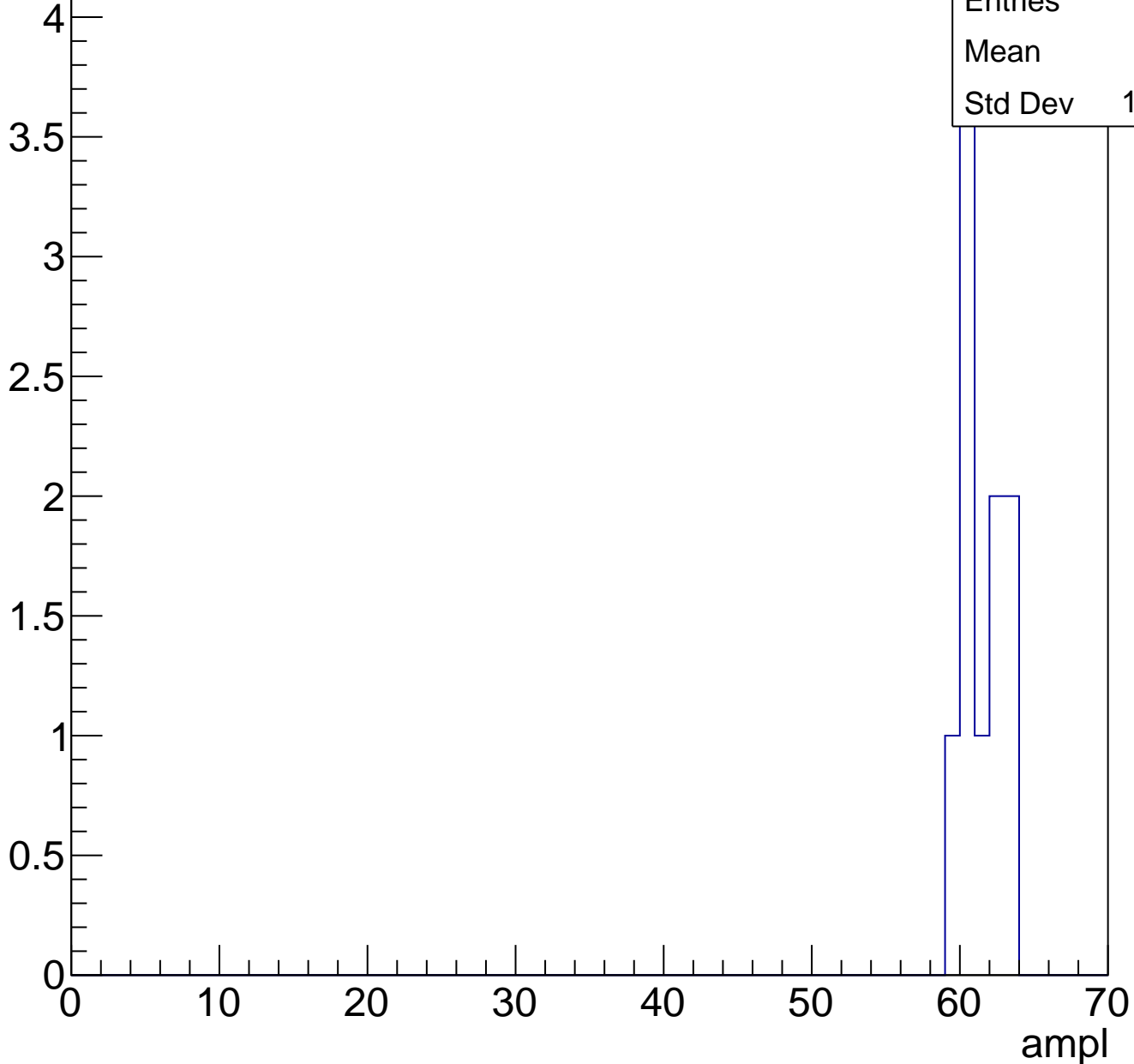
Entries	32
Mean	55.59
Std Dev	10.53



B1L103S, U14-ch94, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

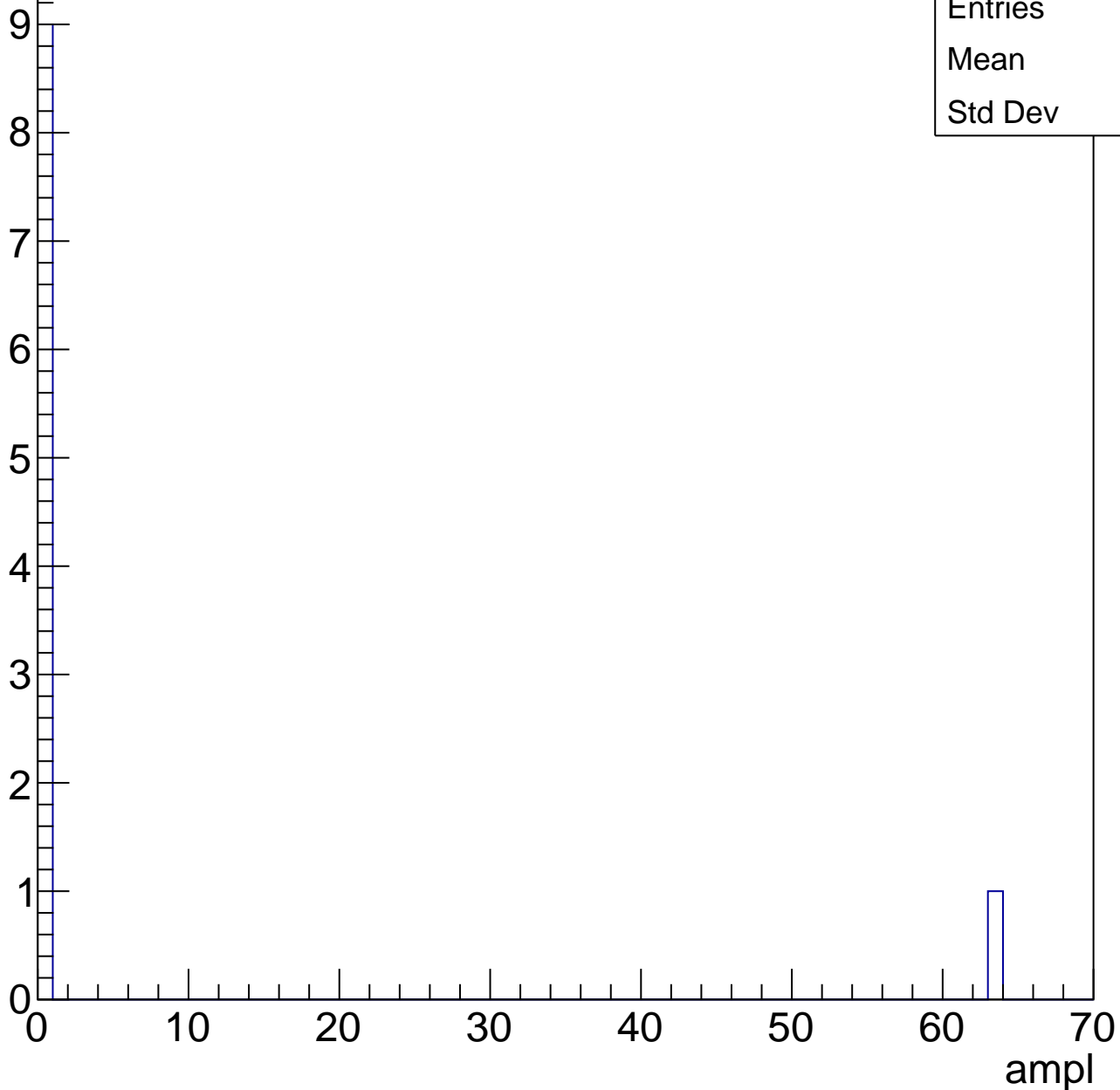


B1L103S, U14-ch94, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	10
Mean	6.3
Std Dev	18.9

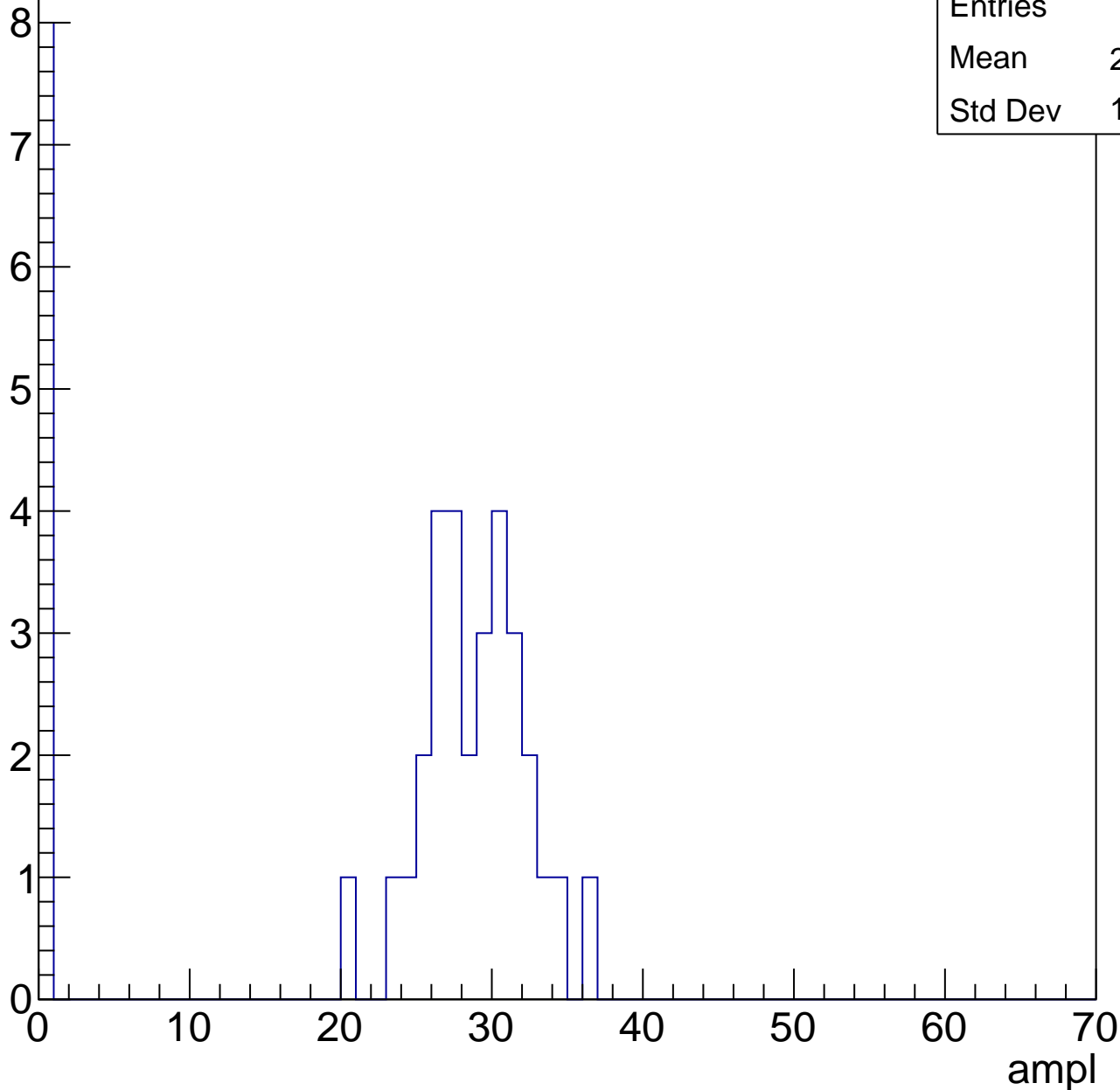


B1L103S, U14-ch95, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	38
Mean	22.42
Std Dev	11.96

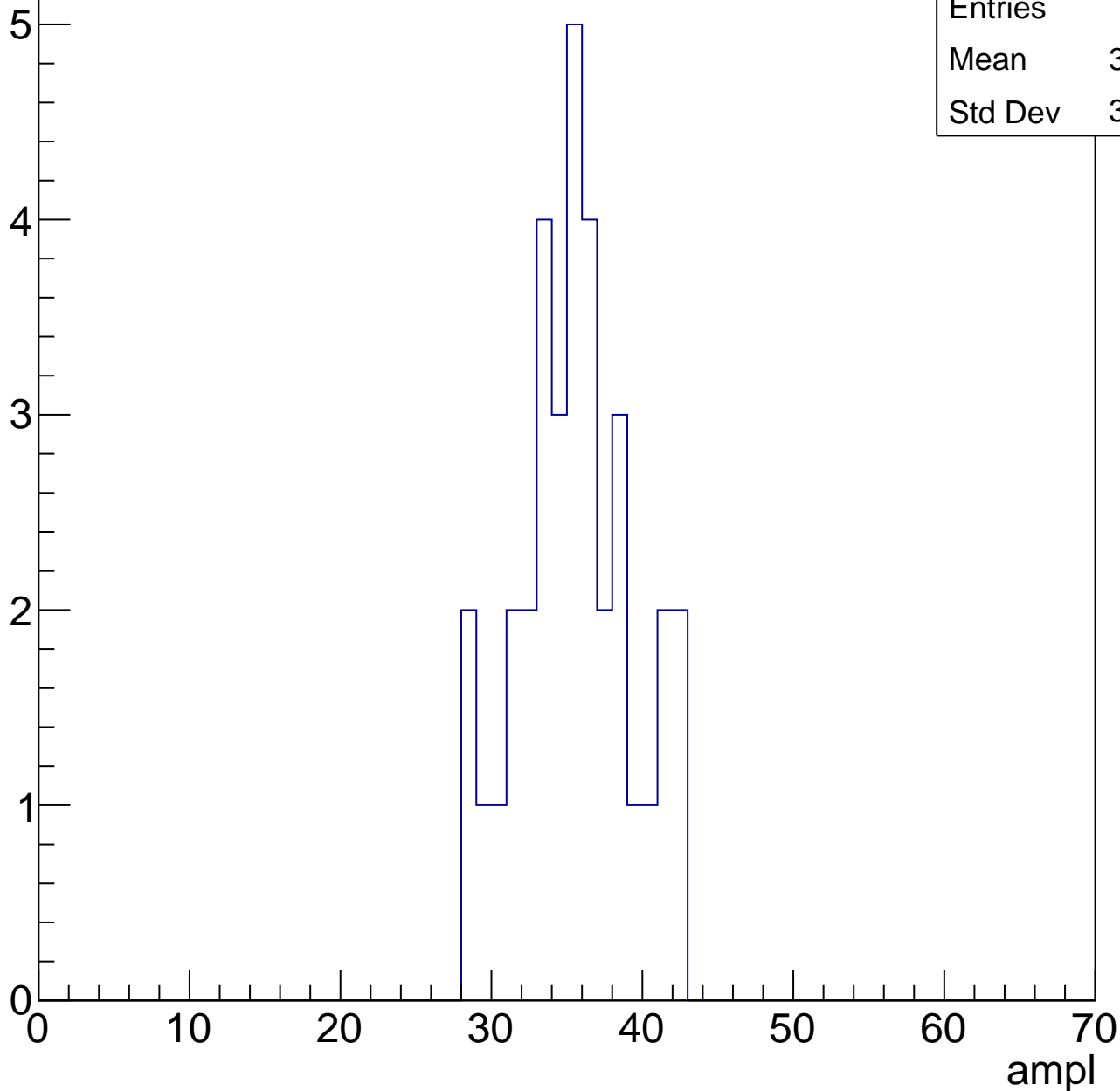


B1L103S, U14-ch95, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

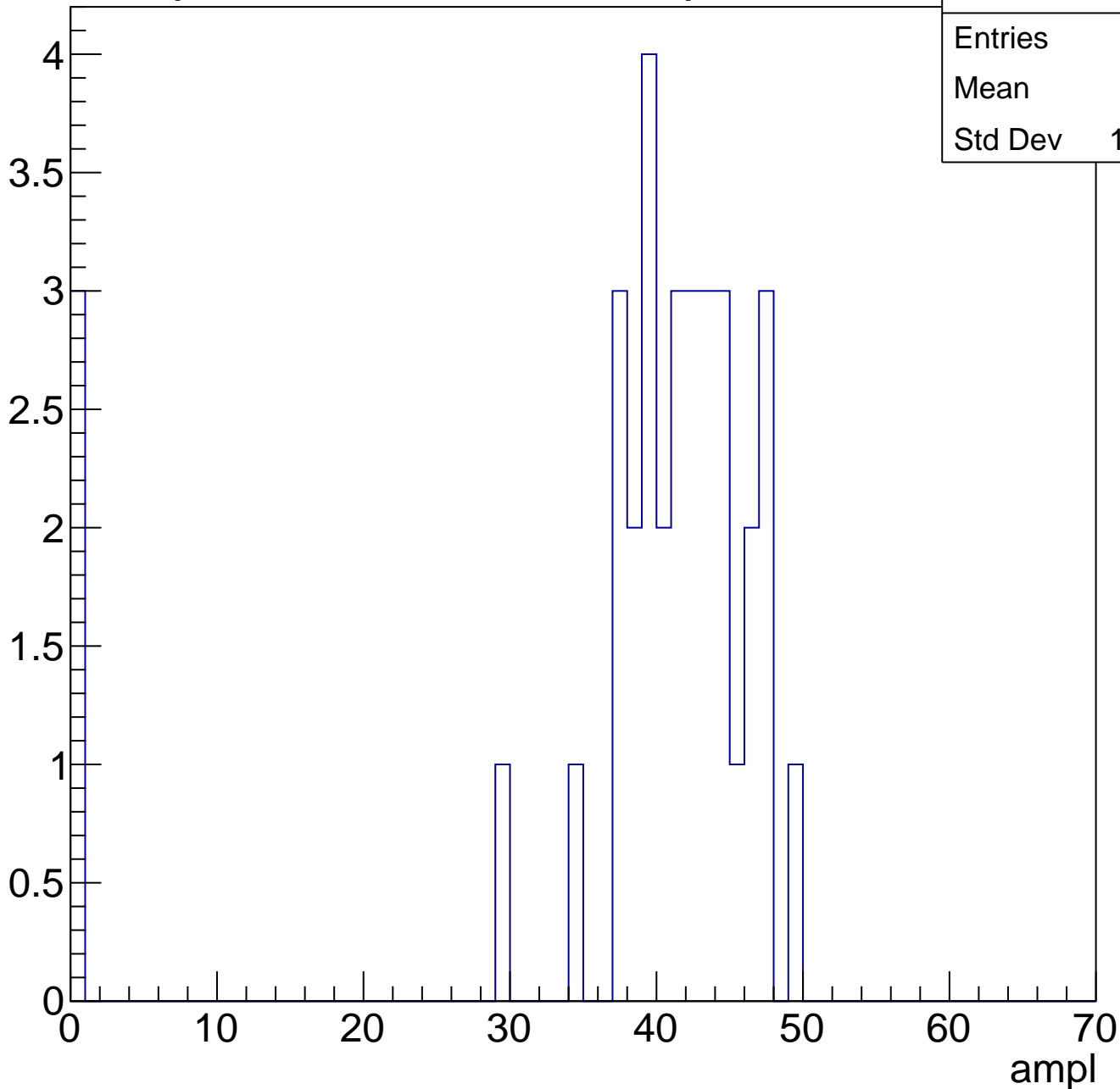
Entries	35
Mean	35.06
Std Dev	3.695



B1L103S, U14-ch95, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

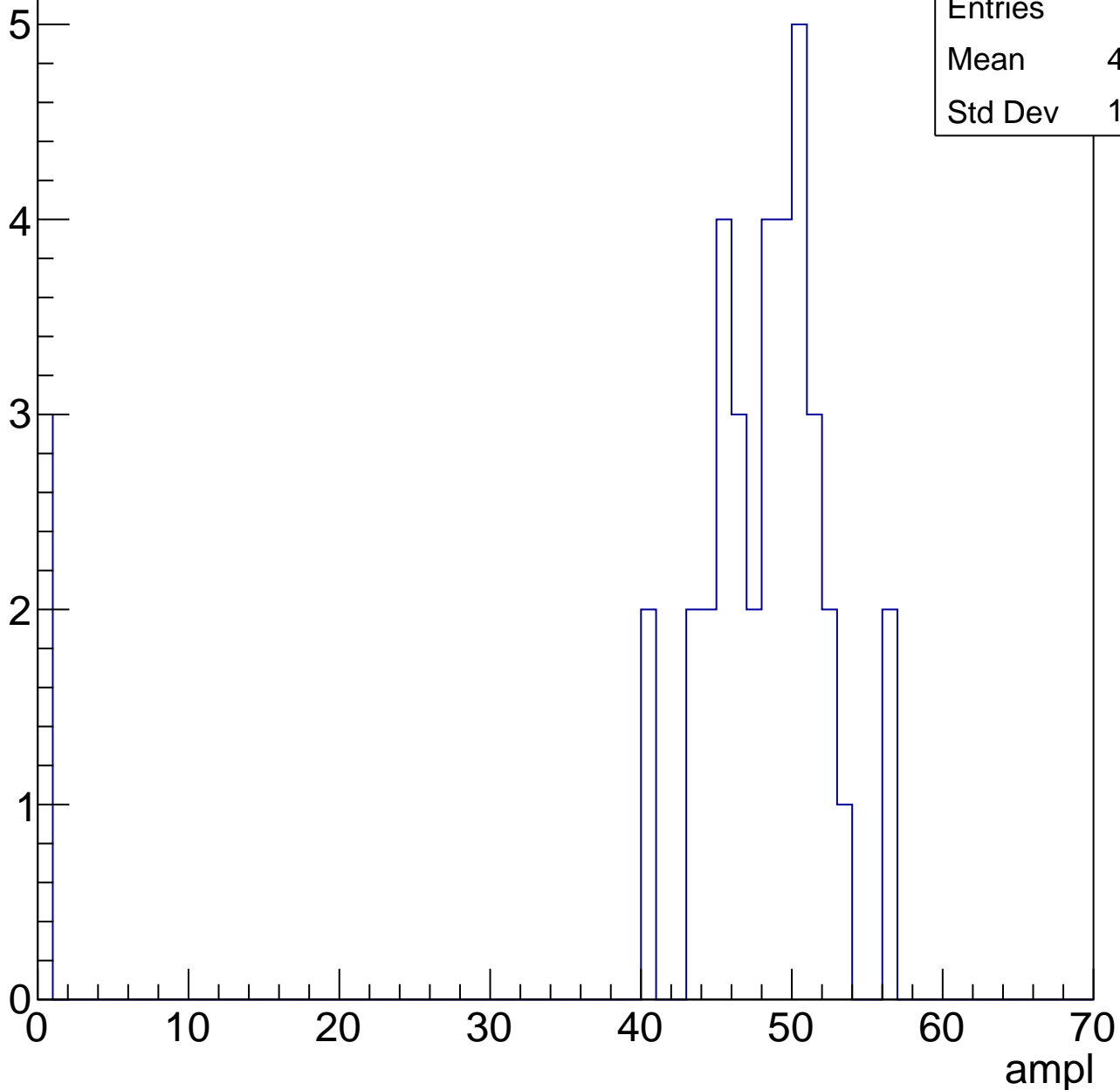


B1L103S, U14-ch95, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	44.26
Std Dev	13.26

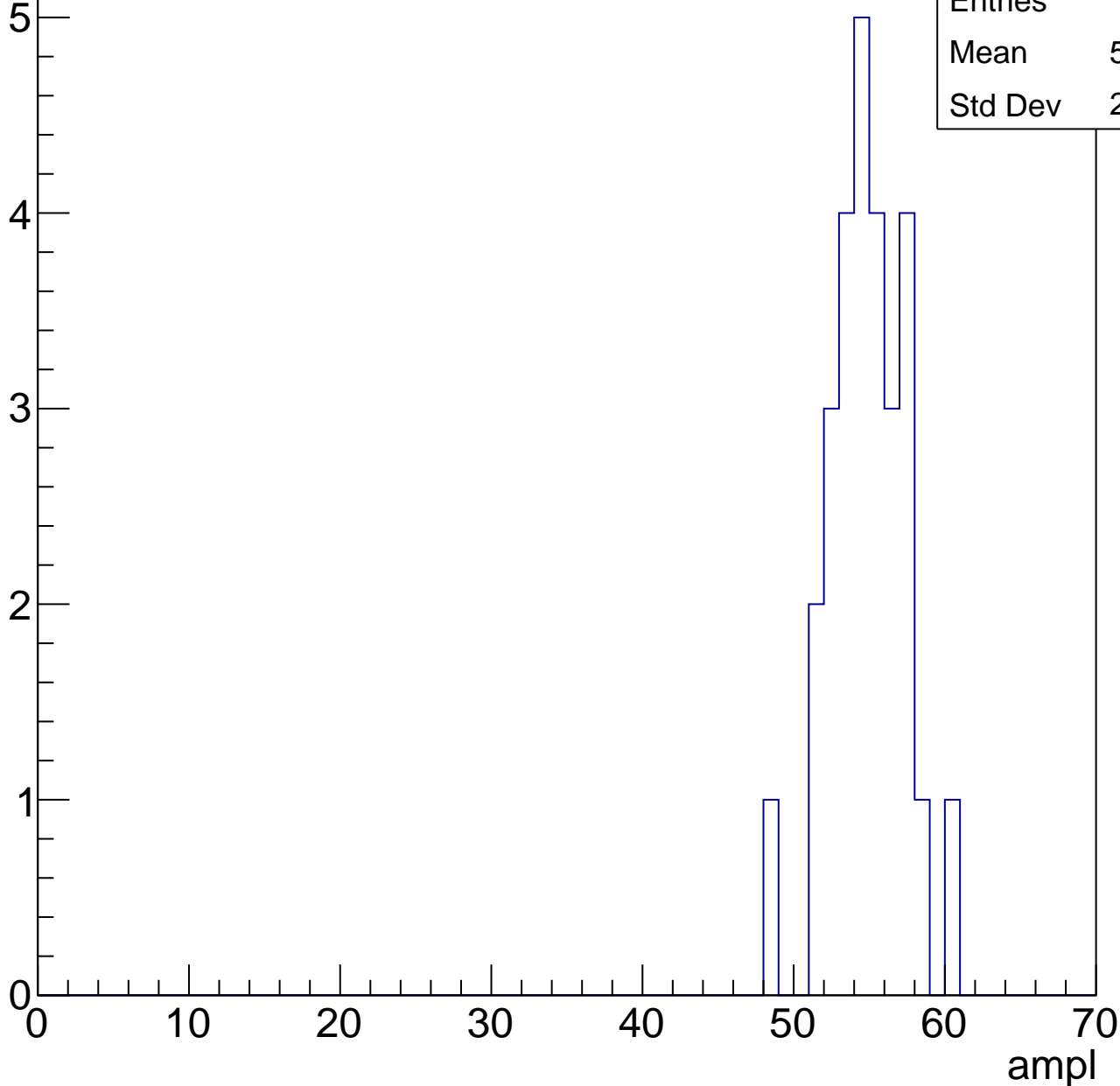


B1L103S, U14-ch95, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	28
Mean	54.36
Std Dev	2.467

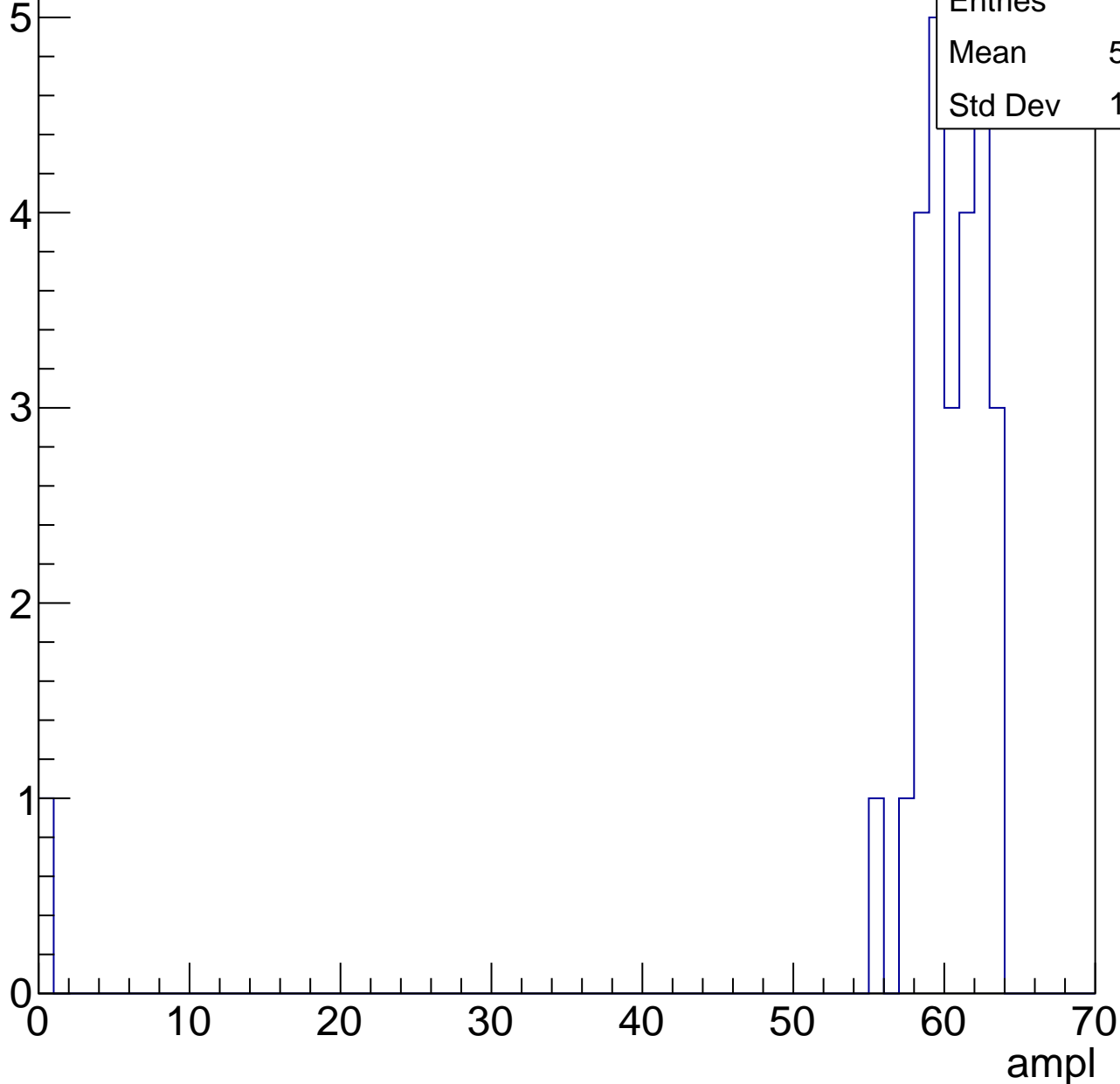


B1L103S, U14-ch95, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	27
Mean	57.85
Std Dev	11.52



B1L103S, U14-ch95, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch95, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

Entries

11

Mean

0

Std Dev

0

B1L103S, U14-ch96, adc0

calib_packv5_041523_1651.root, FC#0, port C2

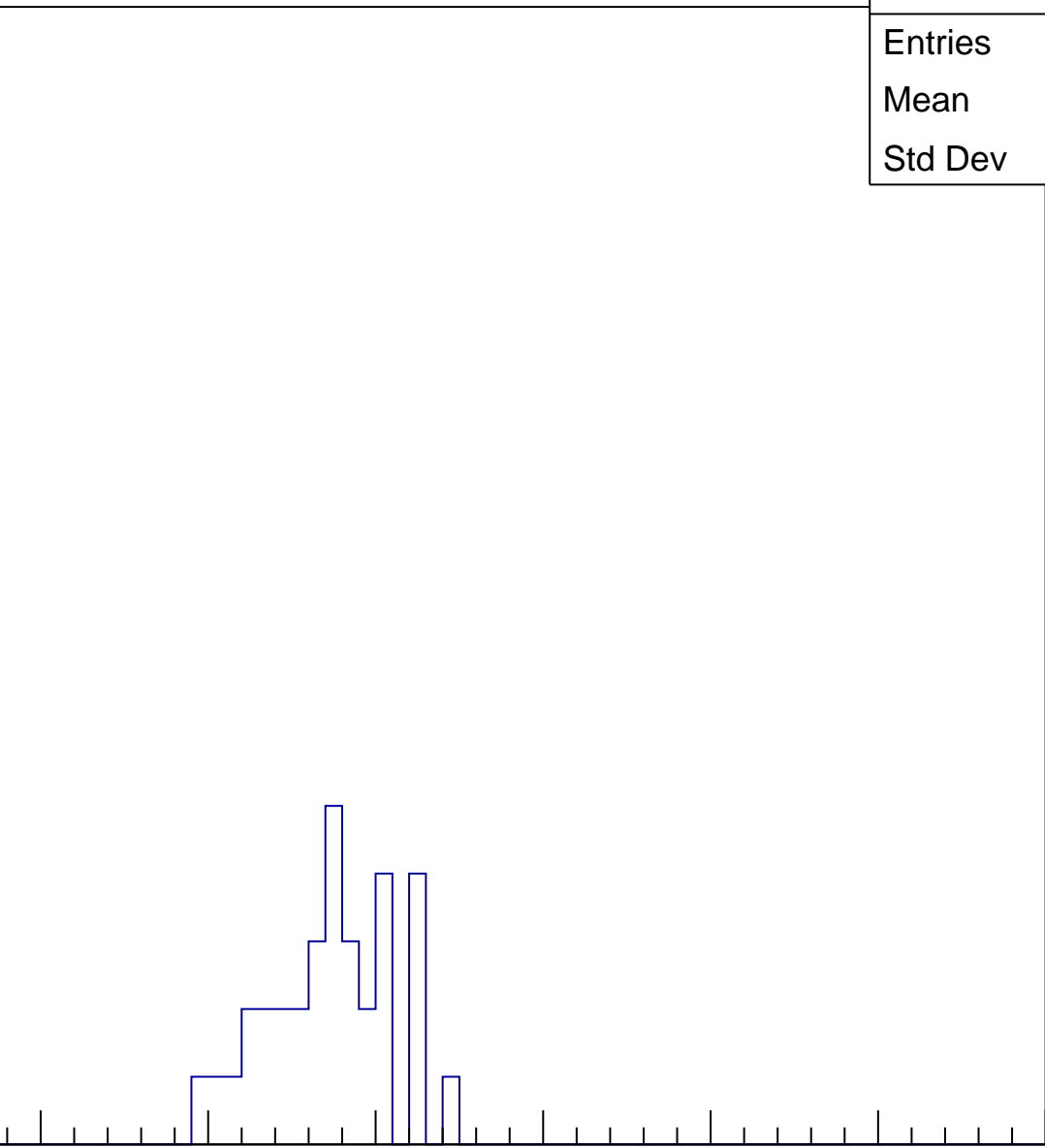
Entries	49
Mean	18.06
Std Dev	12.94

Entry

16
14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

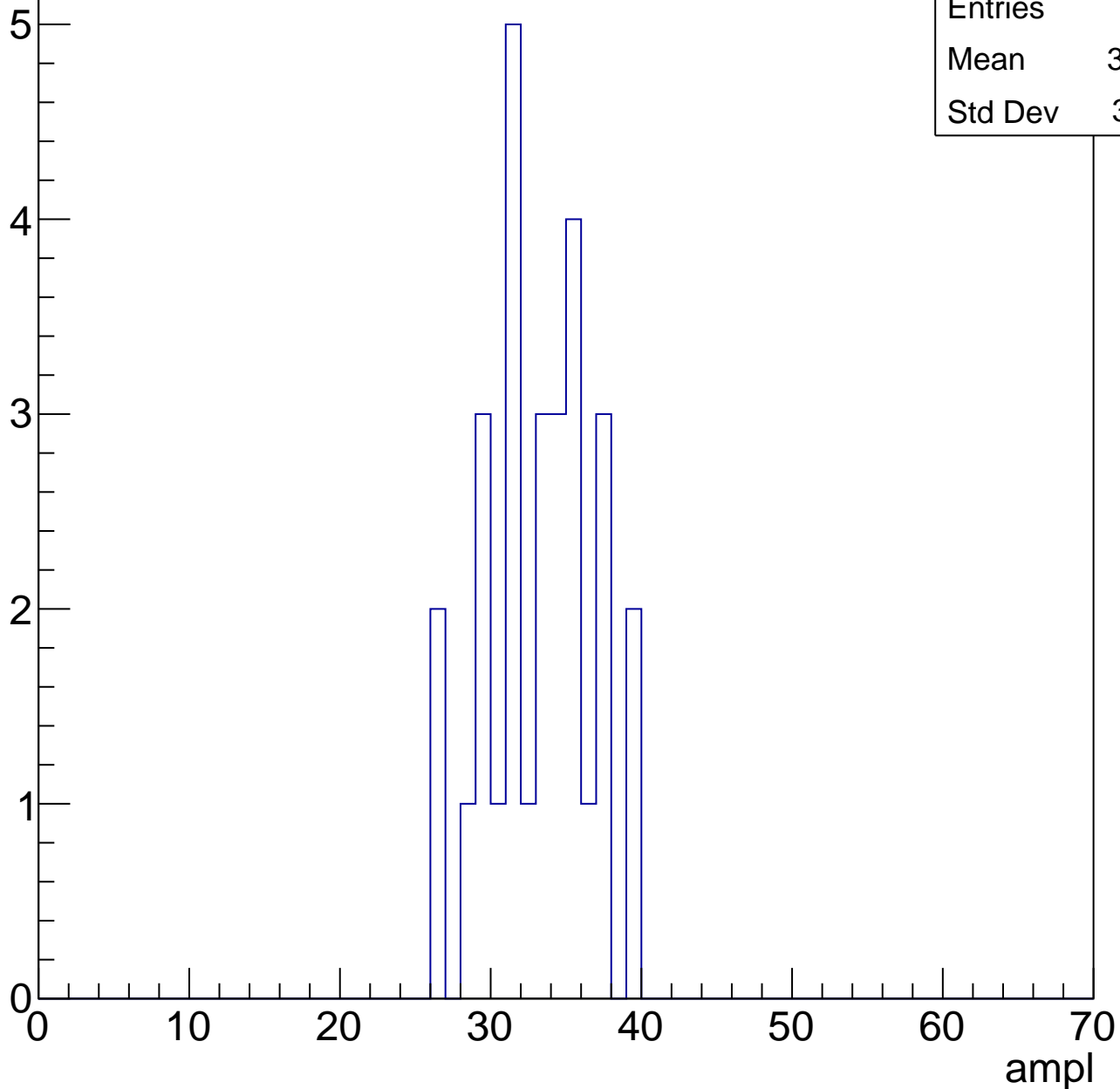


B1L103S, U14-ch96, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	29
Mean	32.76
Std Dev	3.461

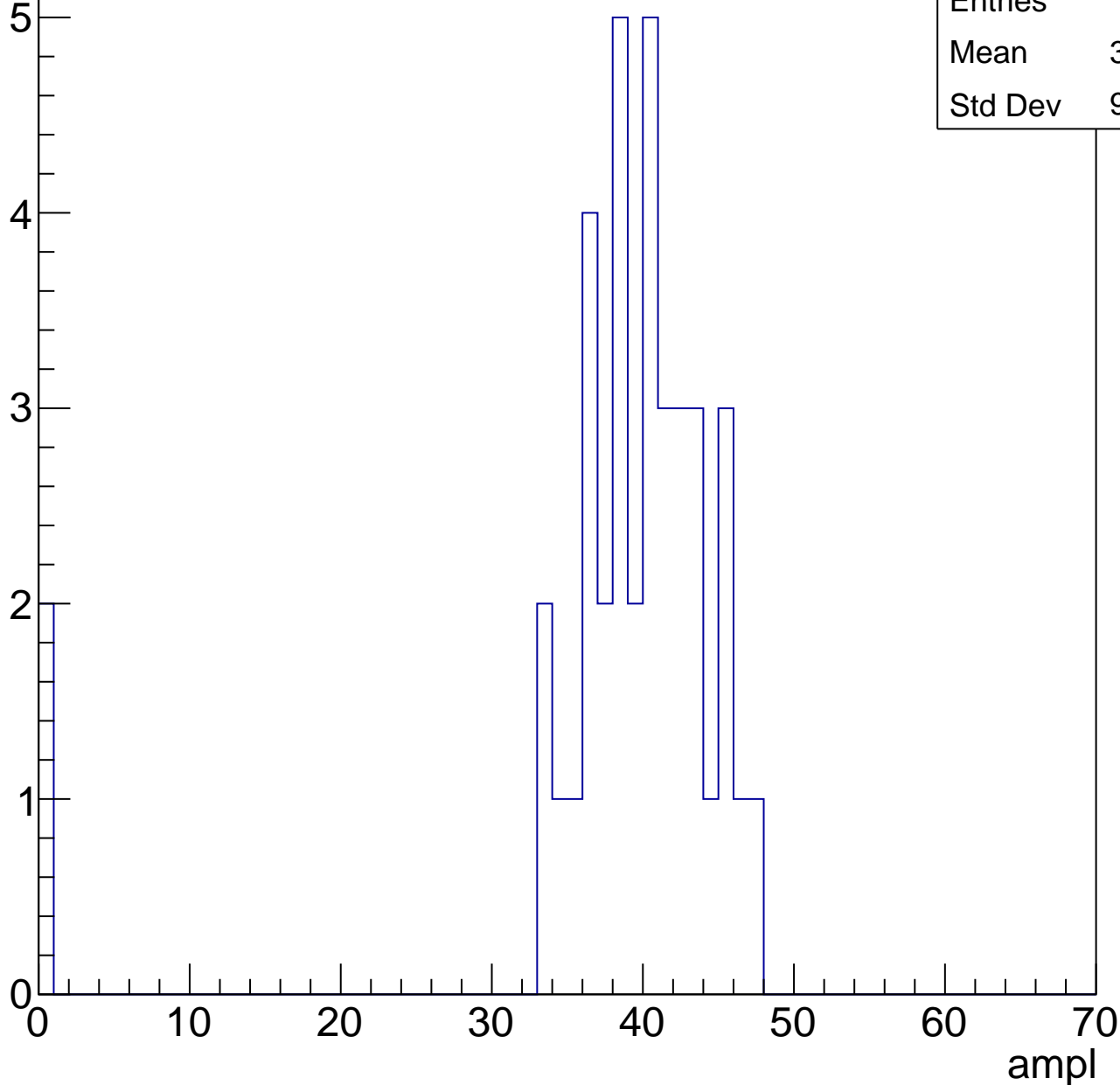


B1L103S, U14-ch96, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	37.72
Std Dev	9.443

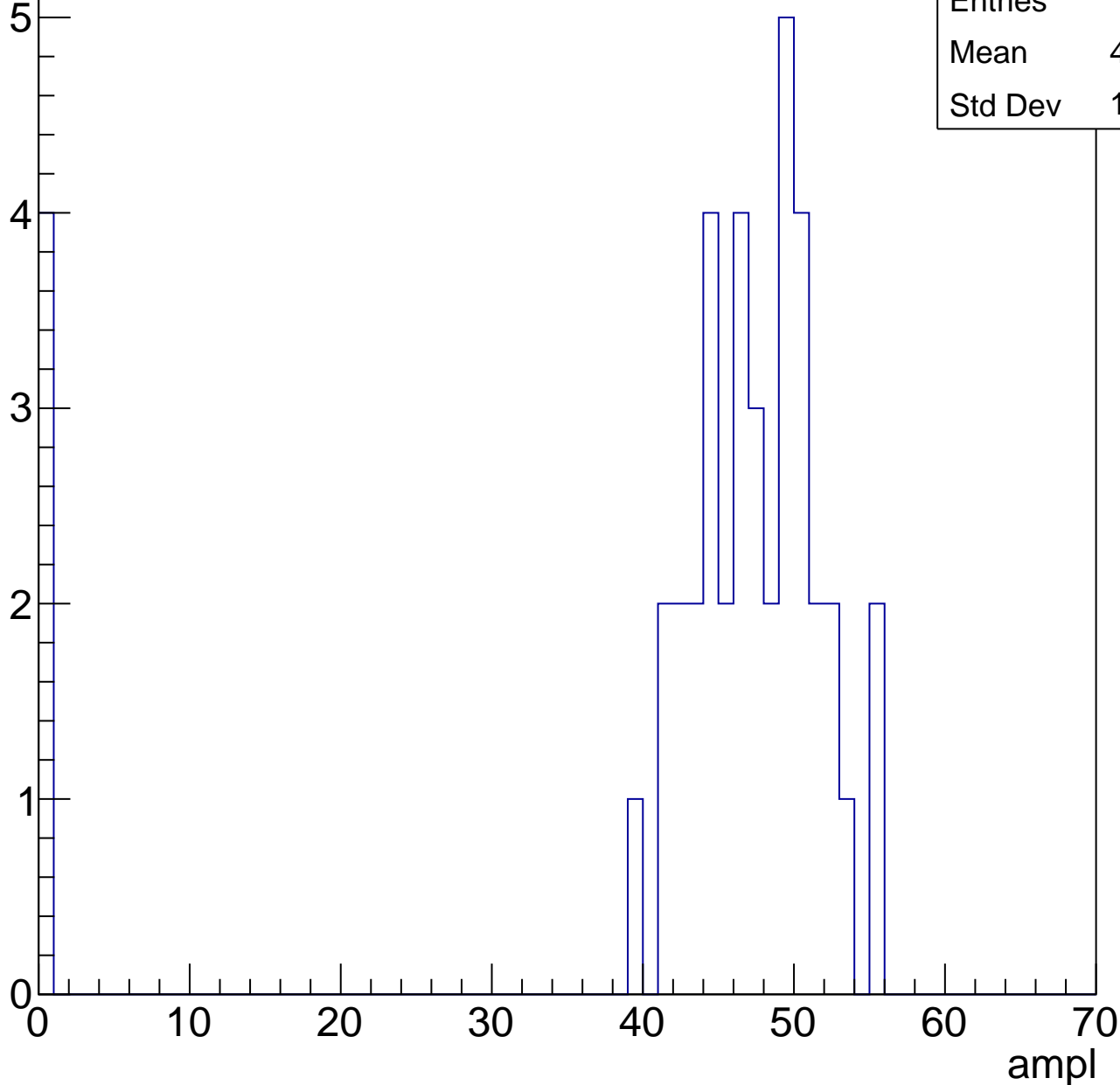


B1L103S, U14-ch96, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

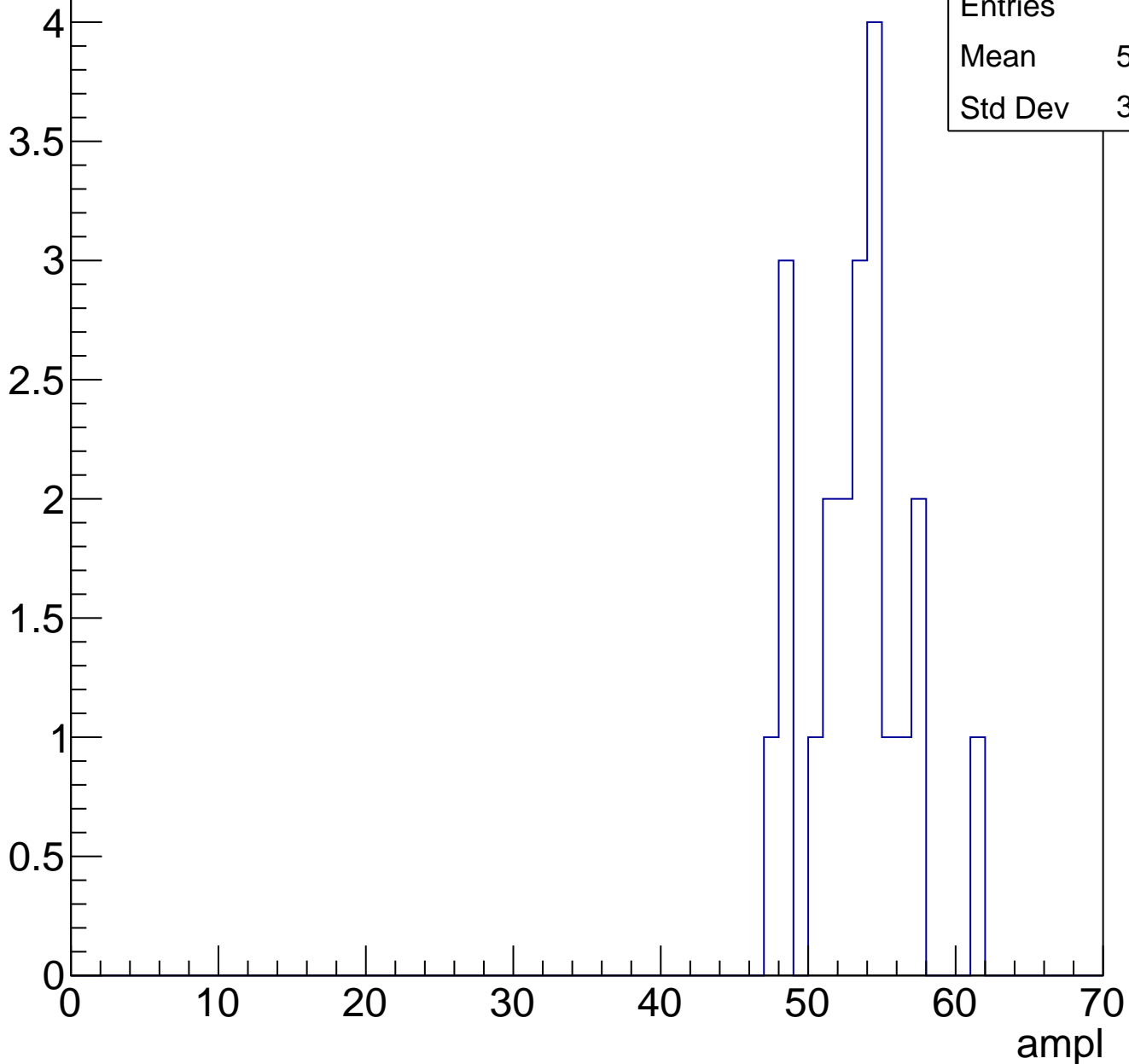
Entries	42
Mean	42.67
Std Dev	14.32



B1L103S, U14-ch96, adc4

calib_packv5_041523_1651.root, FC#0, port C2

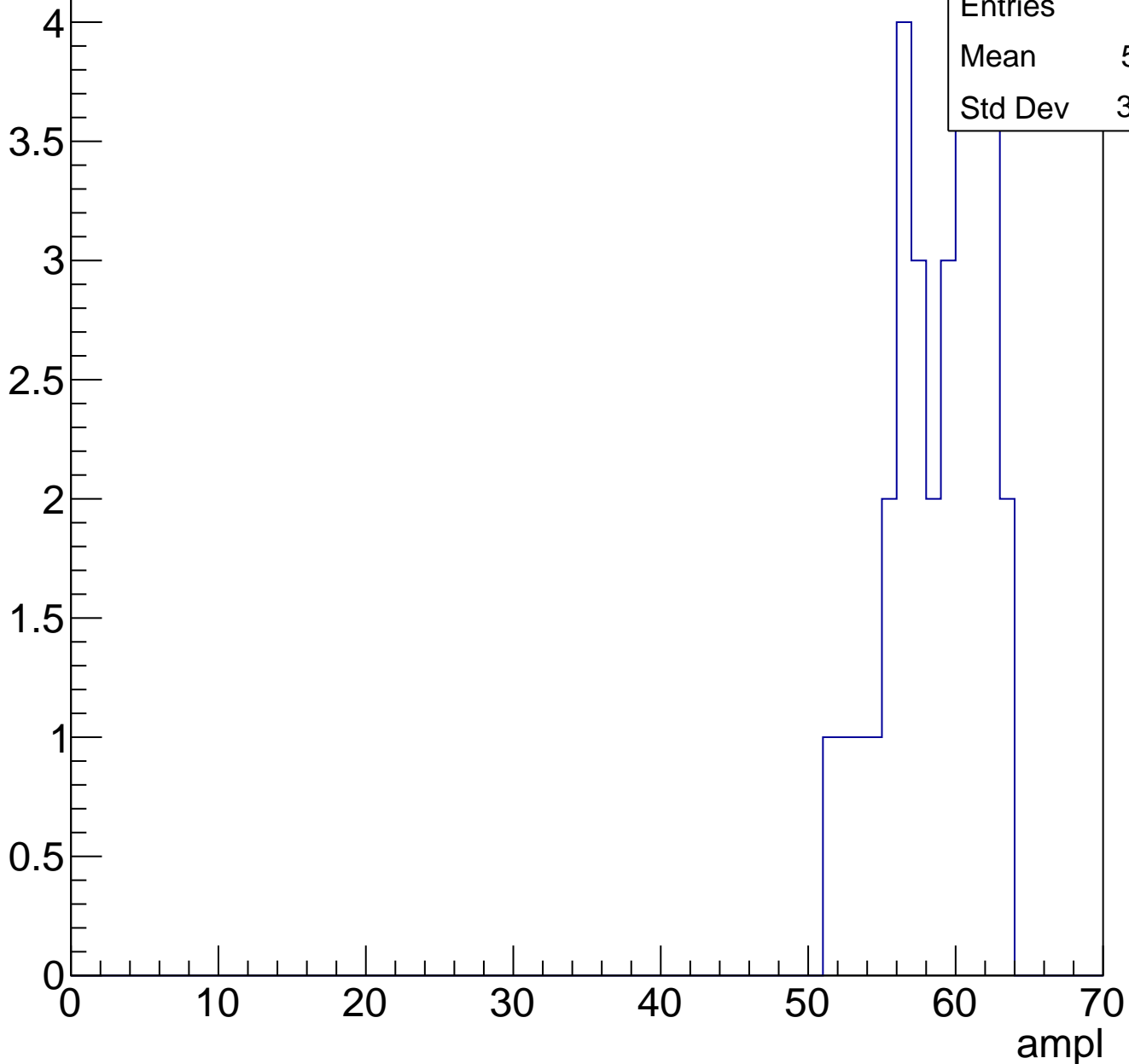
Entry



B1L103S, U14-ch96, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch96, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

3
2.5
2
1.5
1
0.5
0

Entries	10
Mean	60.3
Std Dev	2.1

ampl

B1L103S, U14-ch96, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	11
Mean	0
Std Dev	0

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

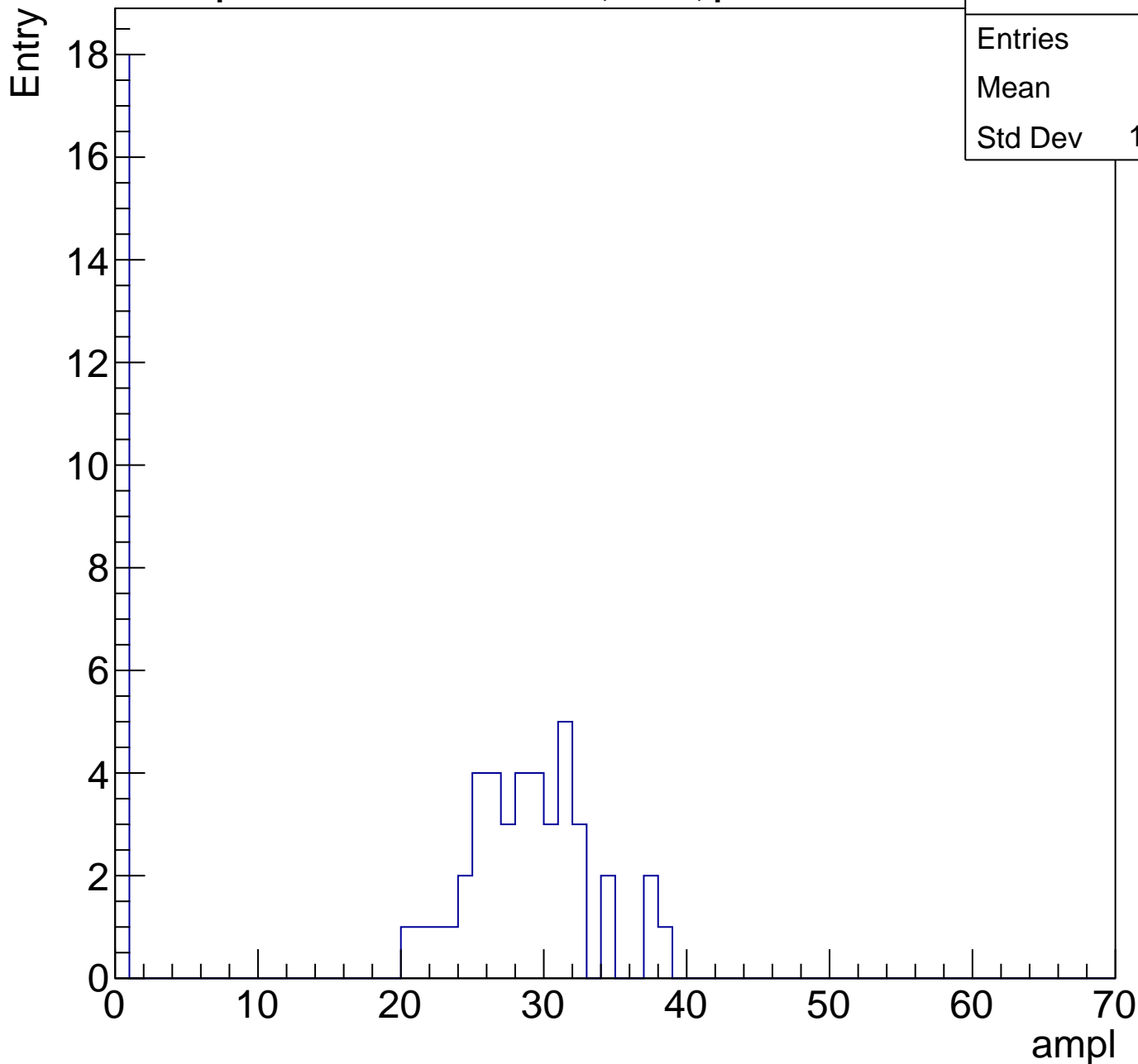
70

ampl

B1L103S, U14-ch97, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	59
Mean	19.8
Std Dev	13.56

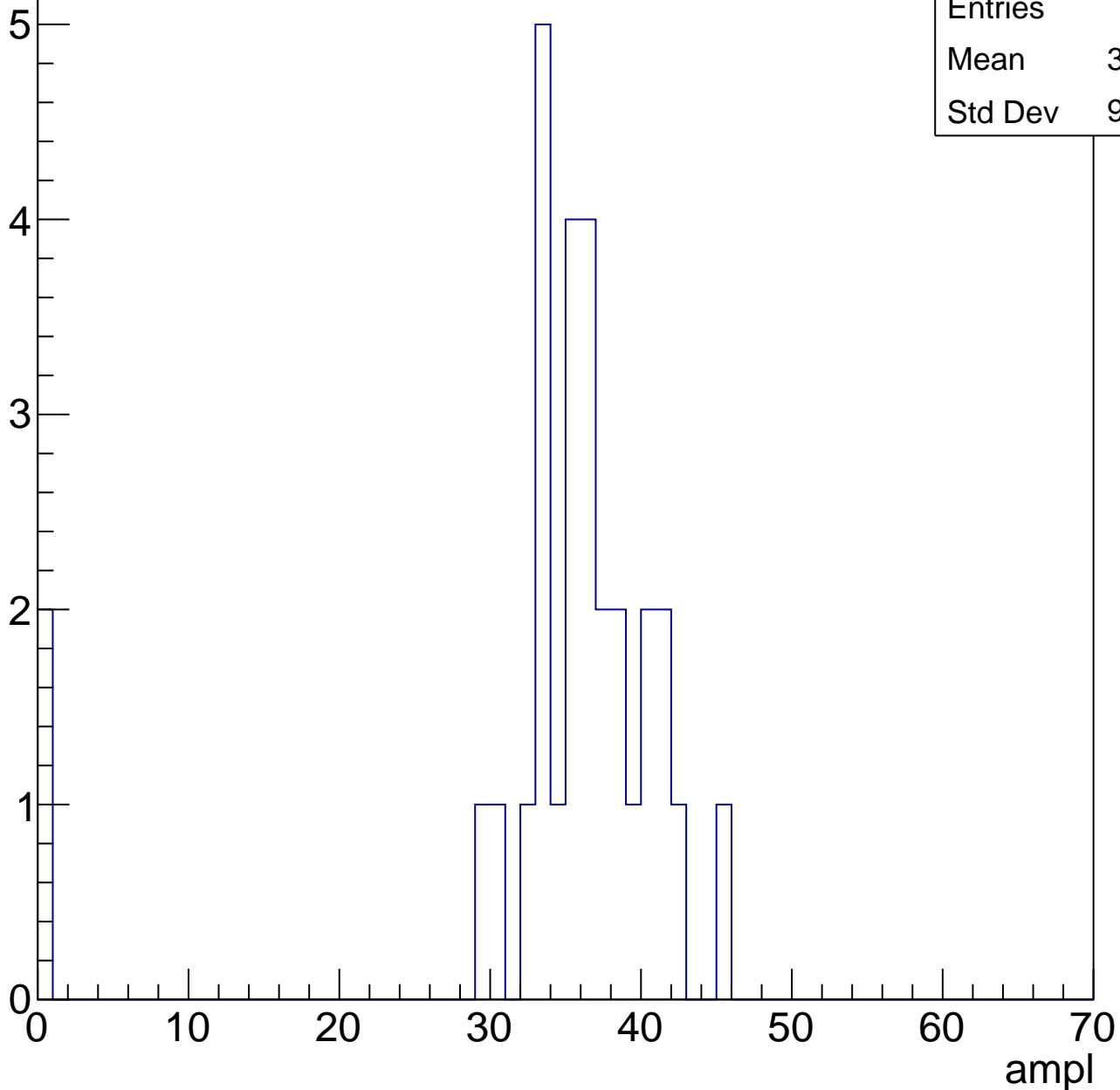


B1L103S, U14-ch97, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	30
Mean	33.73
Std Dev	9.678

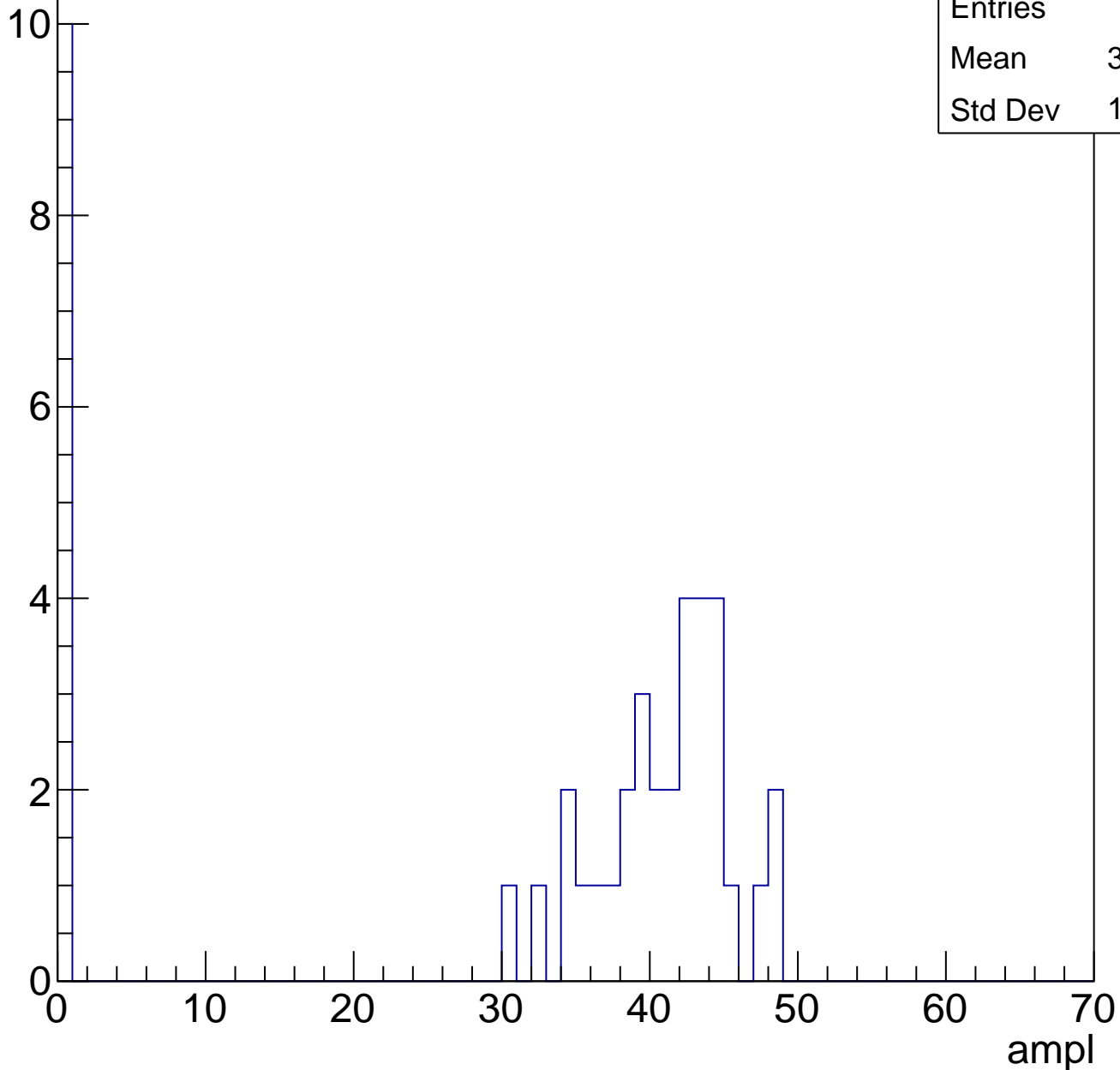


B1L103S, U14-ch97, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	42
Mean	30.88
Std Dev	17.68

Entry

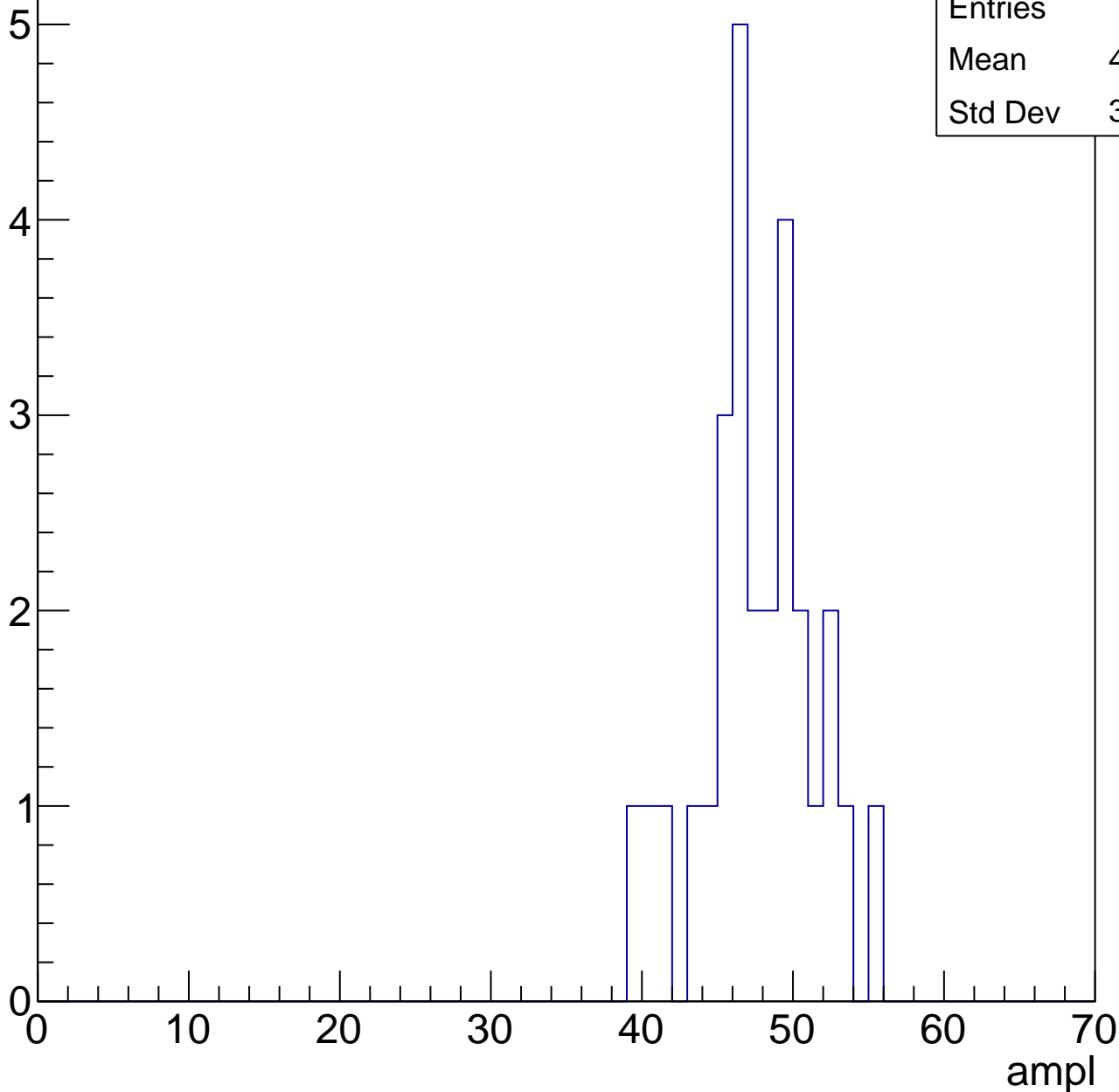


B1L103S, U14-ch97, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	28
Mean	47.18
Std Dev	3.742

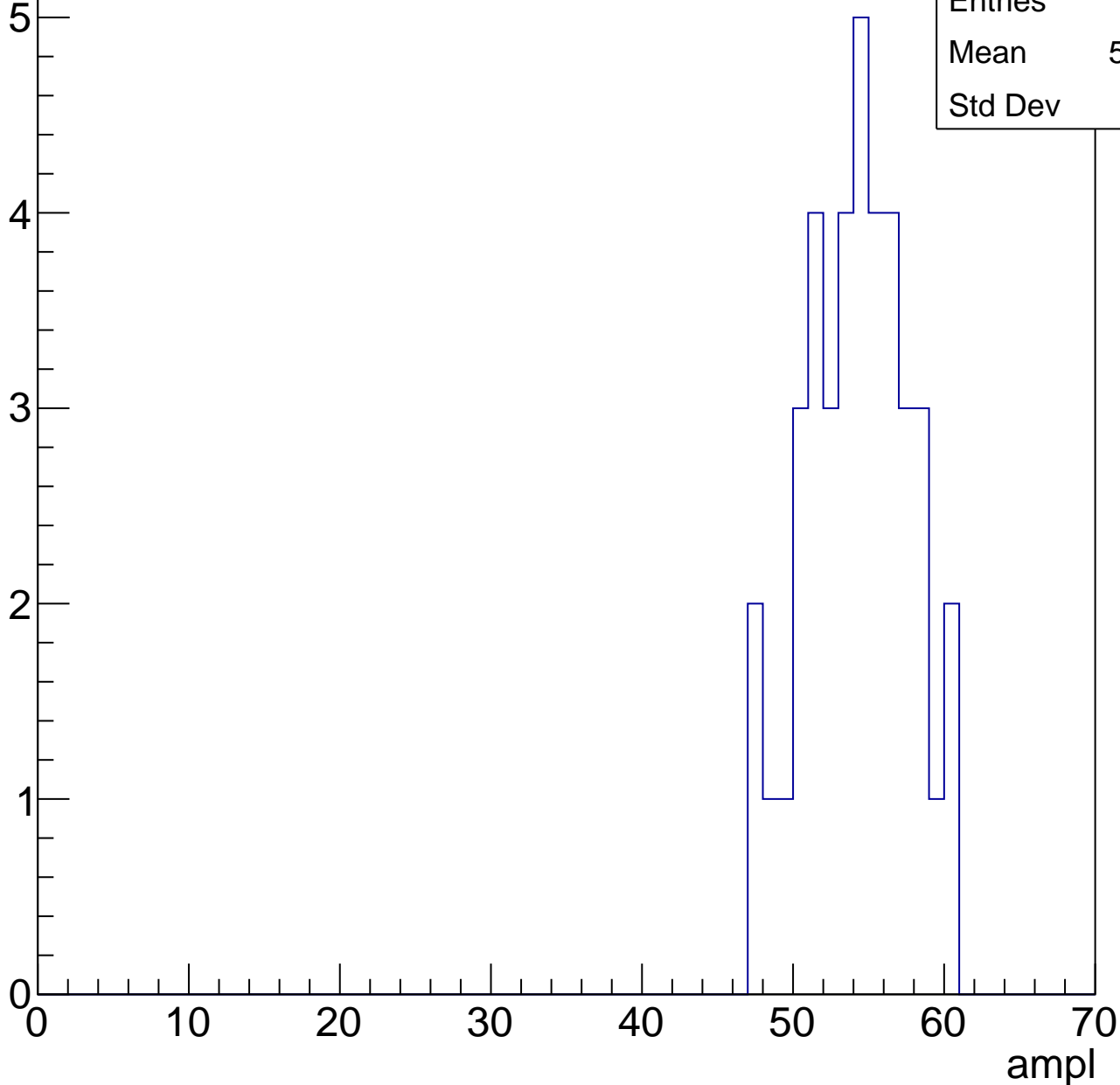


B1L103S, U14-ch97, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	53.77
Std Dev	3.35

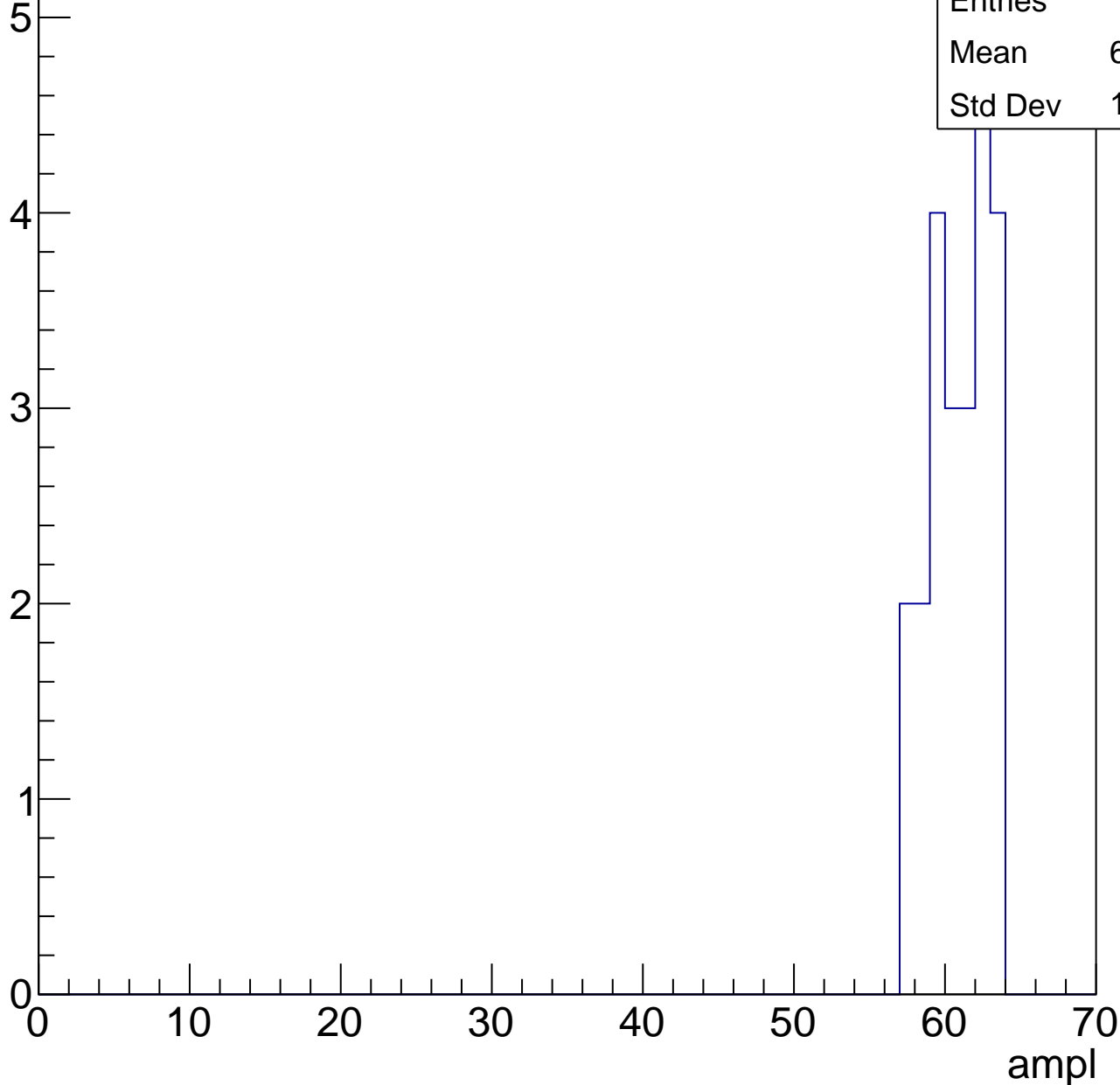


B1L103S, U14-ch97, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

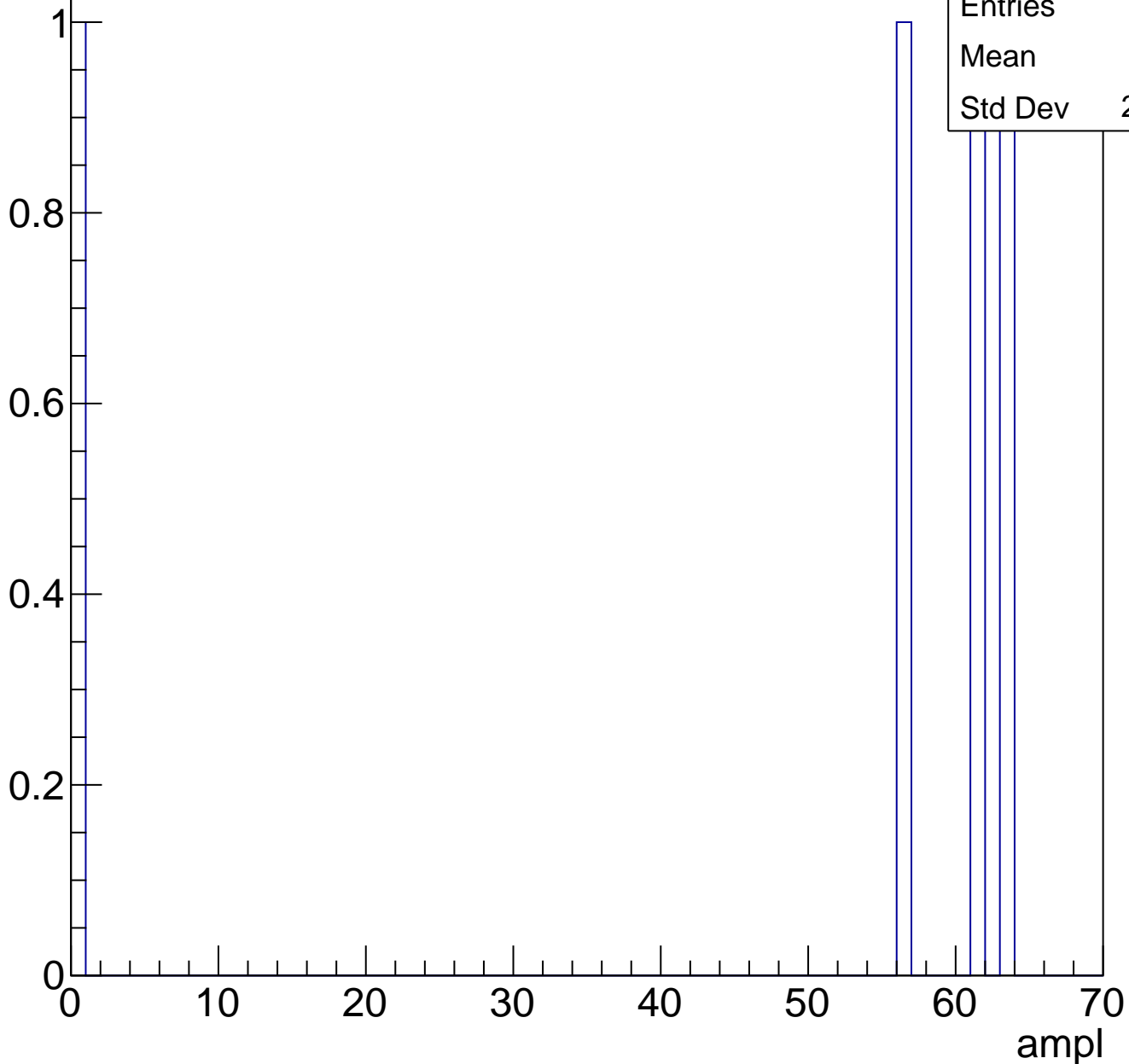
Entries	23
Mean	60.48
Std Dev	1.908



B1L103S, U14-ch97, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

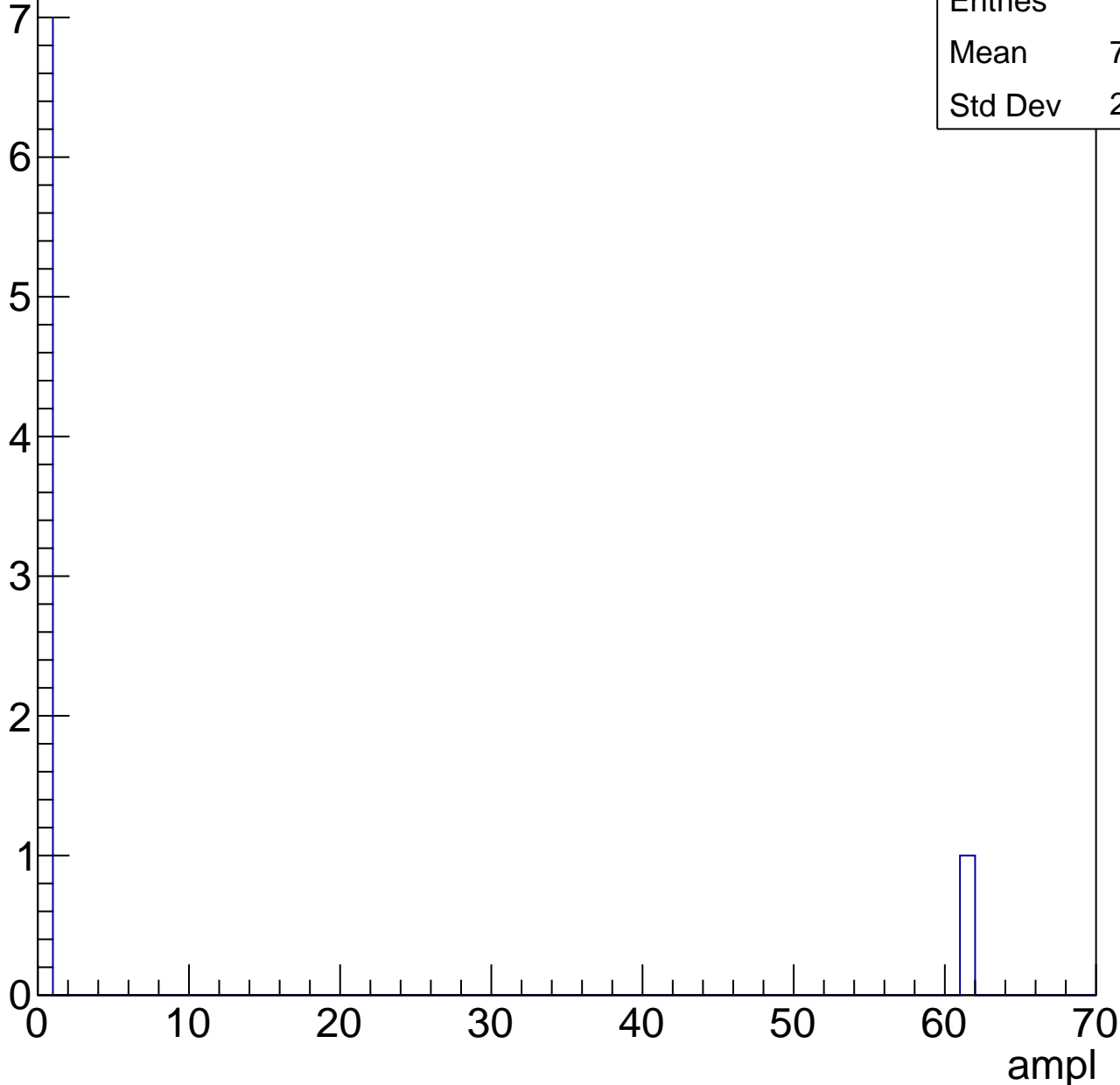


B1L103S, U14-ch97, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	8
Mean	7.625
Std Dev	20.17

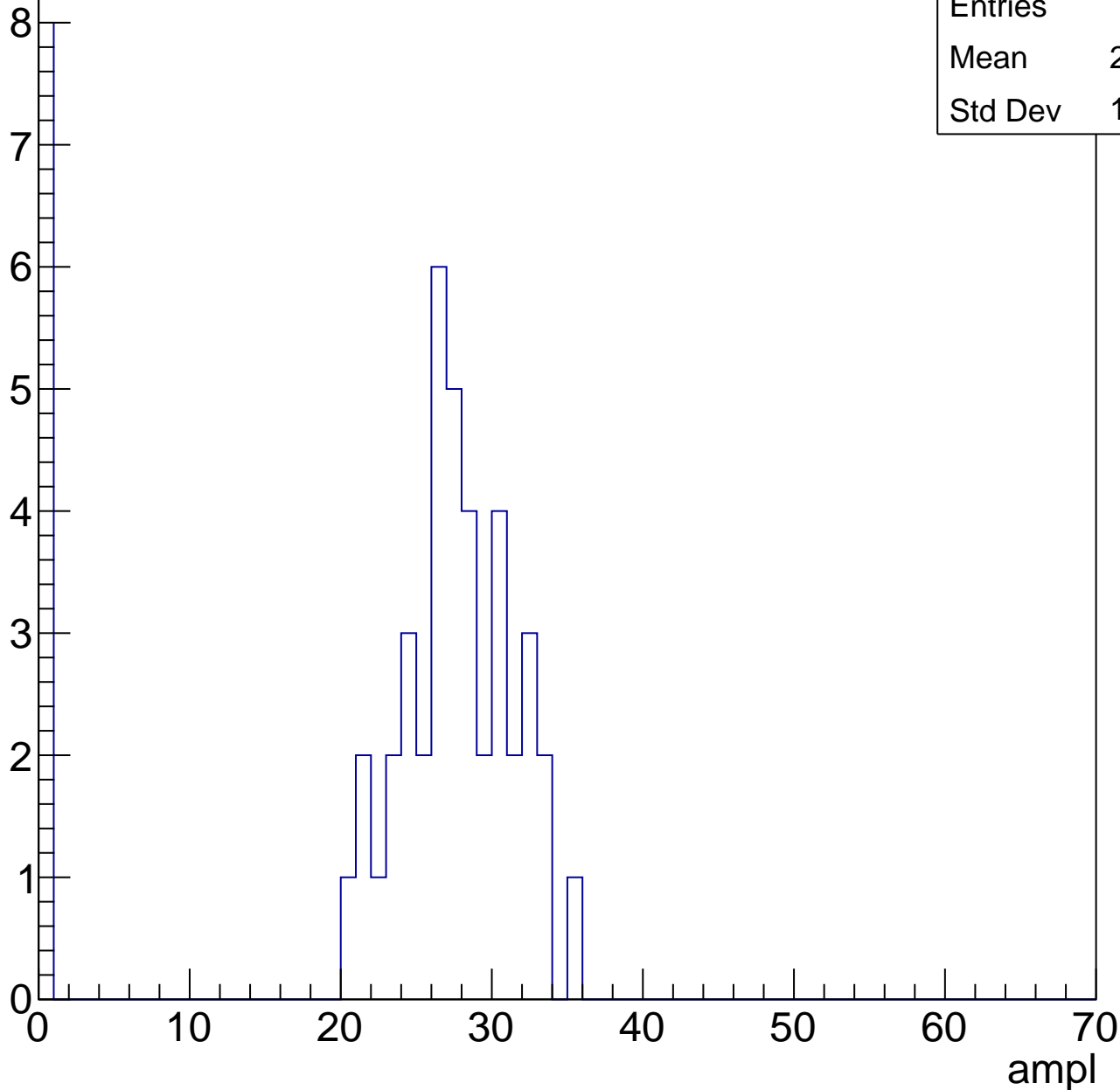


B1L103S, U14-ch98, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

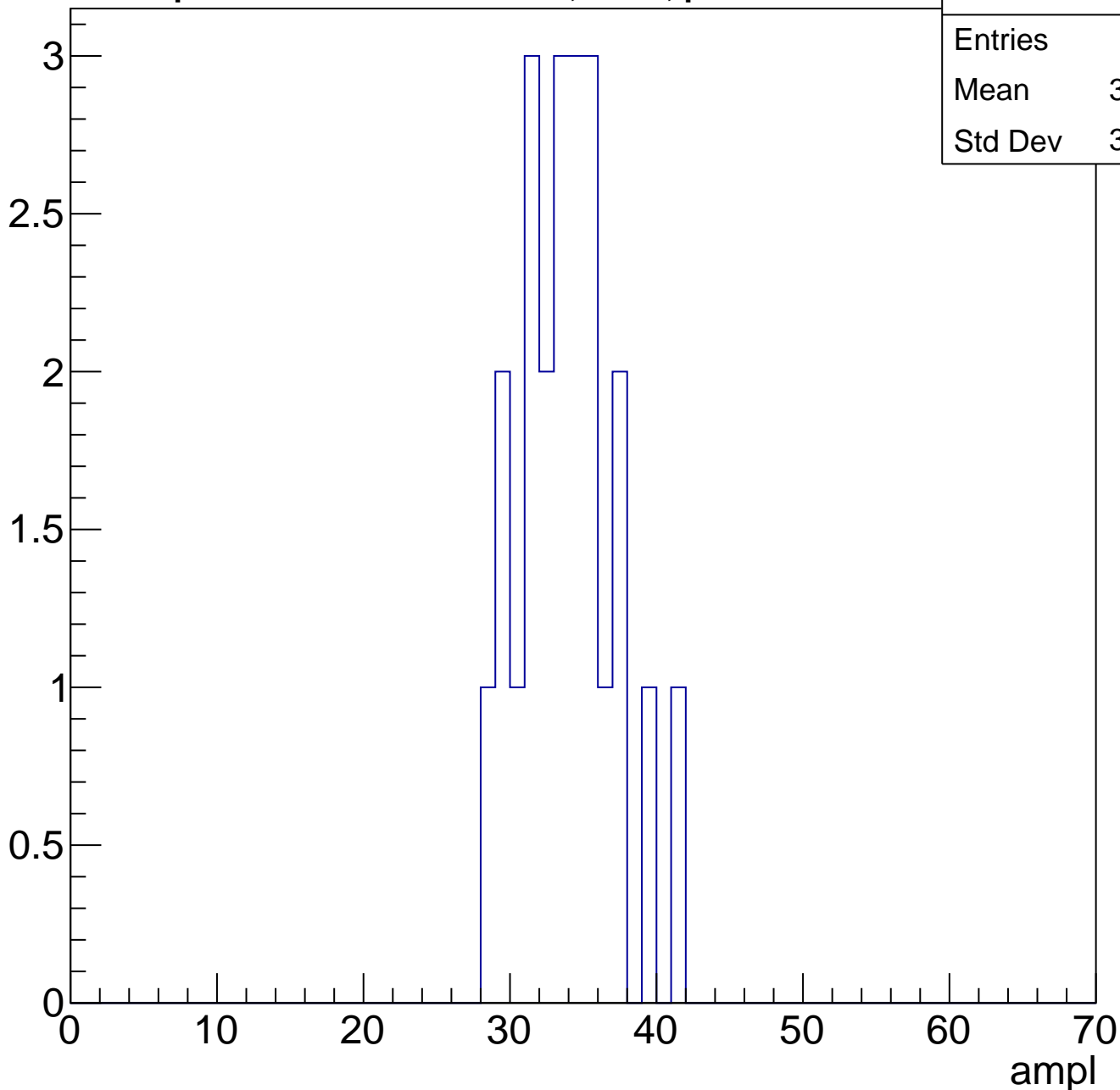
Entries	48
Mean	22.75
Std Dev	10.68



B1L103S, U14-ch98, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry



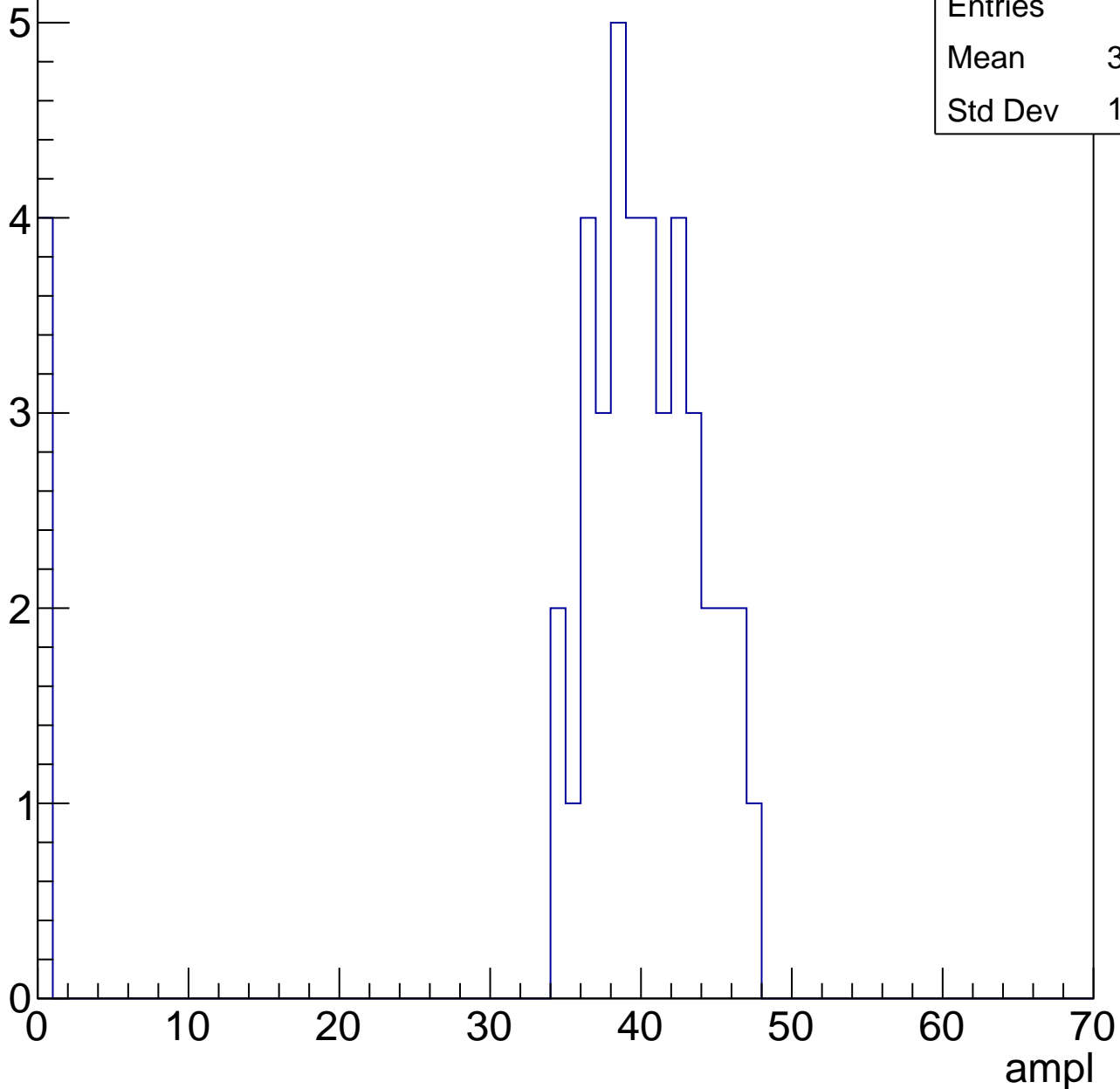
Entries	23
Mean	33.43
Std Dev	3.174

B1L103S, U14-ch98, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

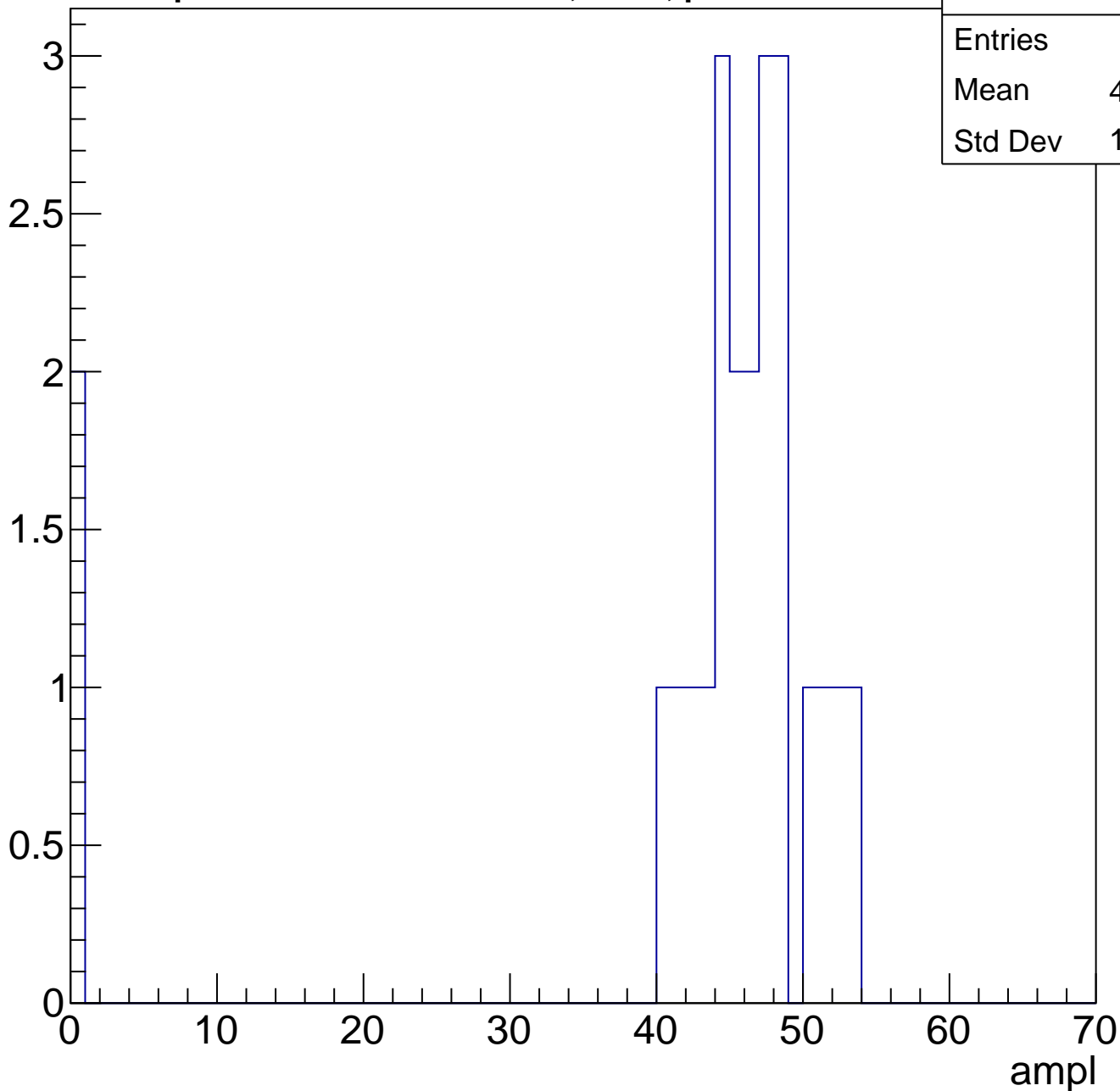
Entries	44
Mean	36.39
Std Dev	11.95



B1L103S, U14-ch98, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

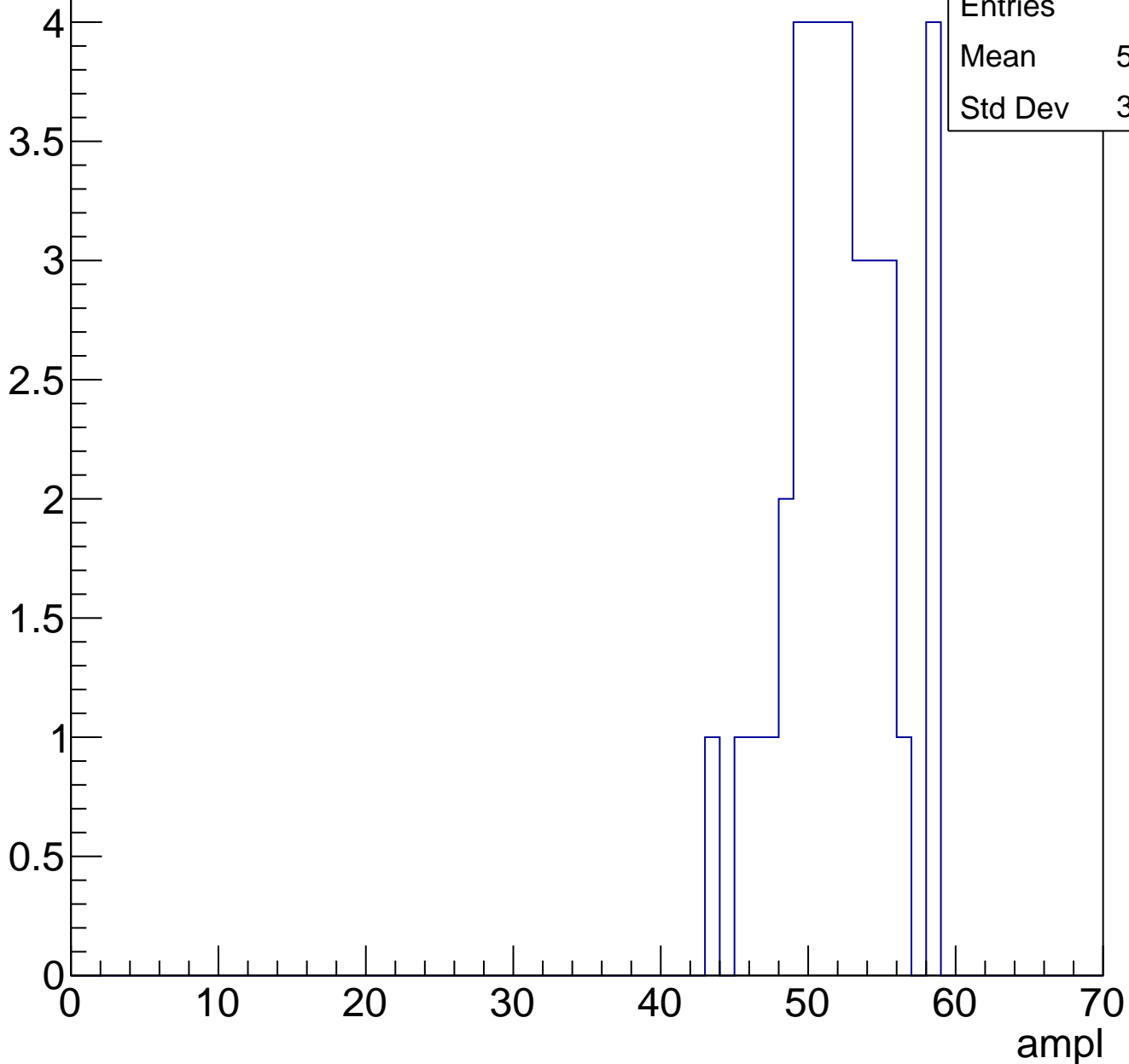


Entries	23
Mean	42.22
Std Dev	13.42

B1L103S, U14-ch98, adc4

calib_packv5_041523_1651.root, FC#0, port C2

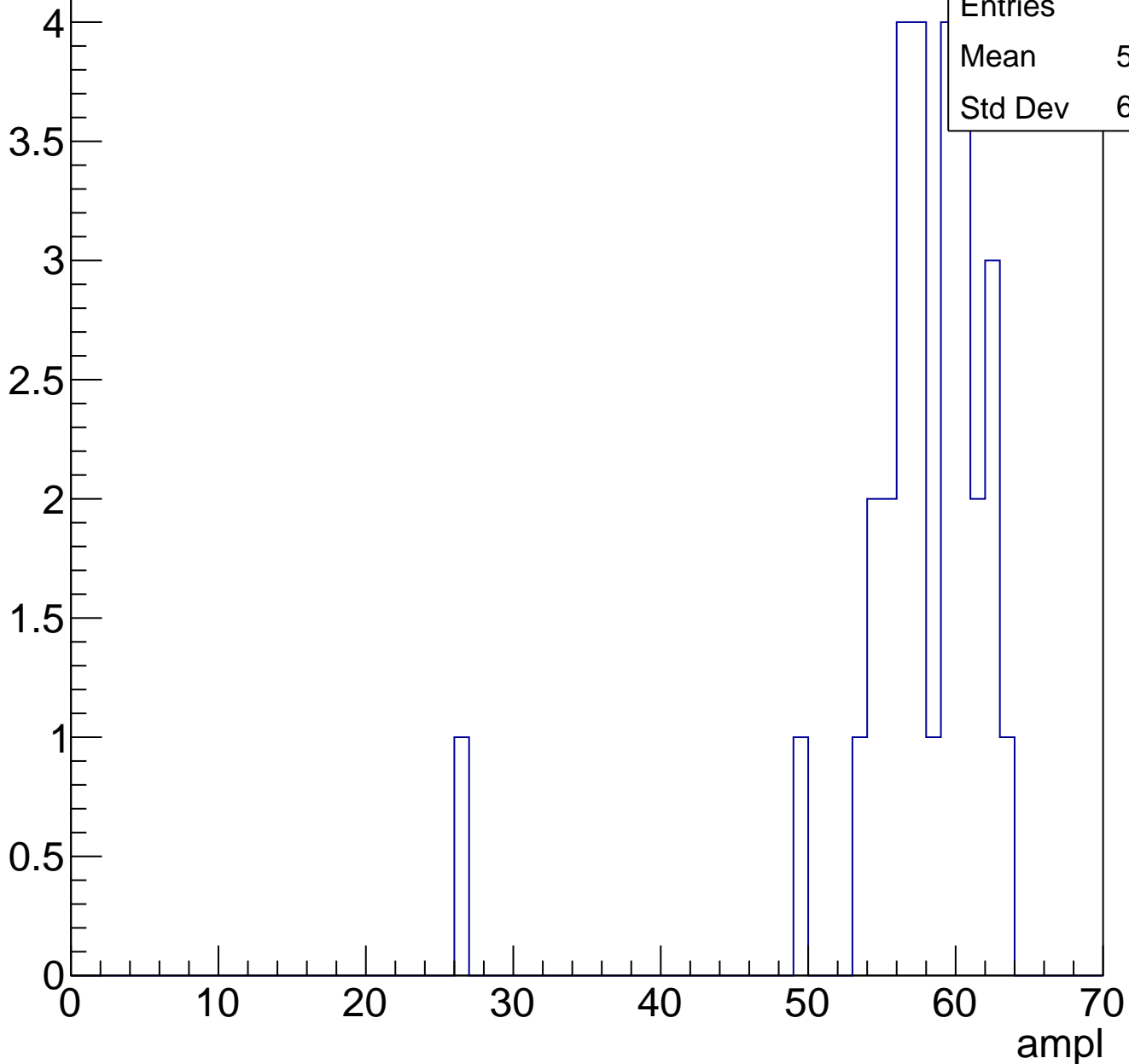
Entry



B1L103S, U14-ch98, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch98, adc6

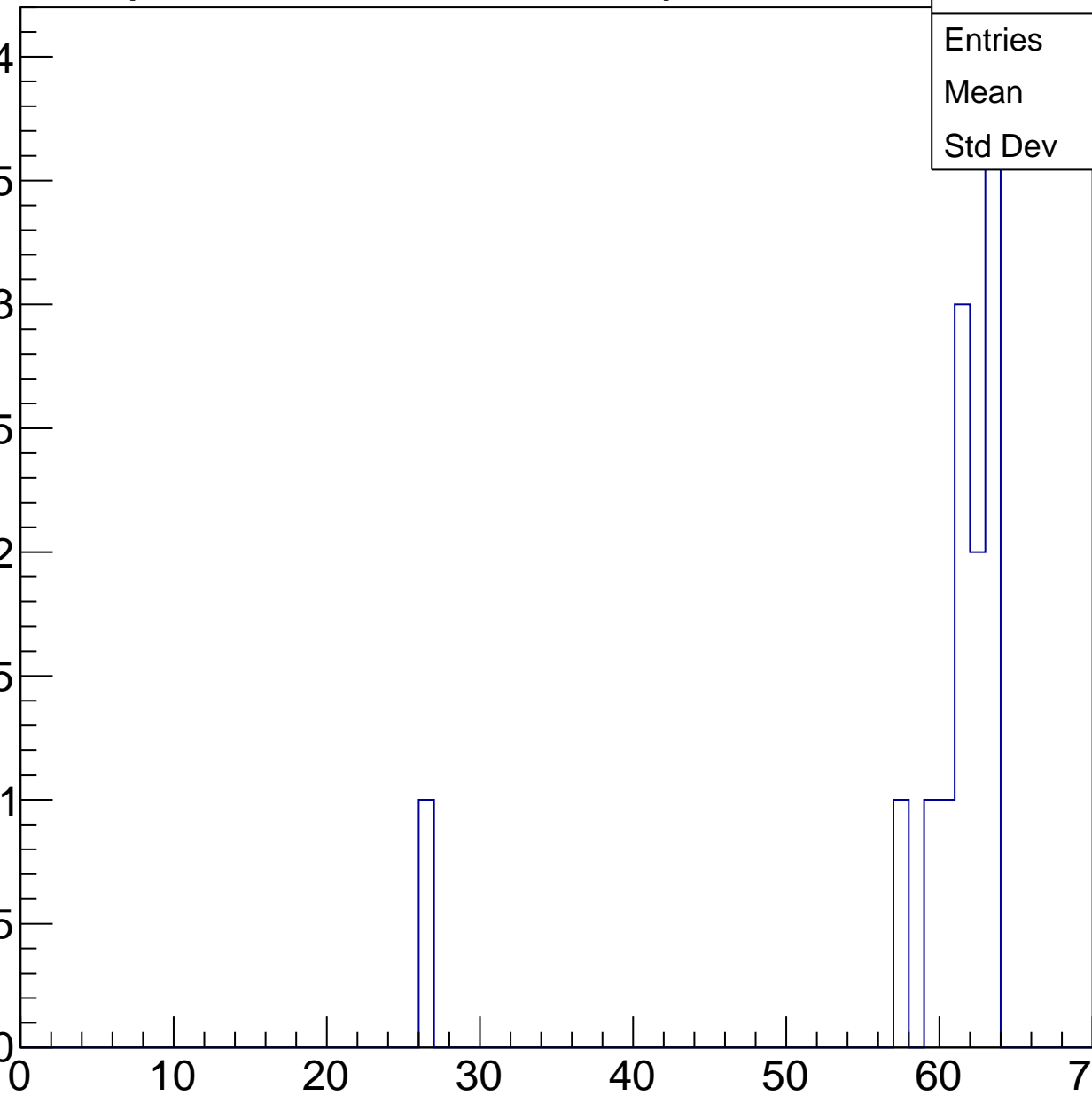
calib_packv5_041523_1651.root, FC#0, port C2

Entry

4
3.5
3
2.5
2
1.5
1
0.5
0

Entries	13
Mean	58.54
Std Dev	9.548

ampl



B1L103S, U14-ch98, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

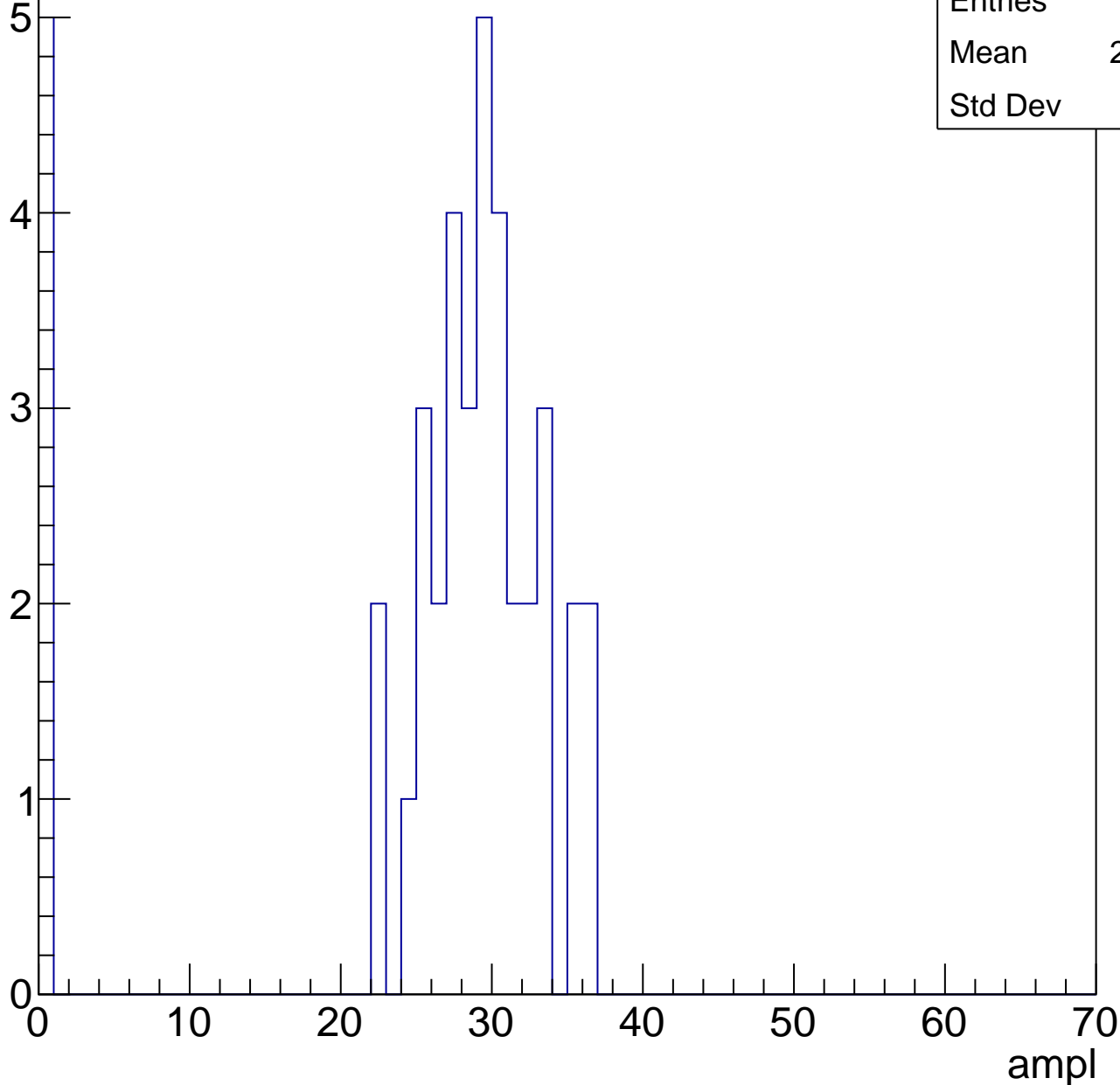
Entries	11
Mean	0
Std Dev	0

B1L103S, U14-ch99, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	25.48
Std Dev	10.2

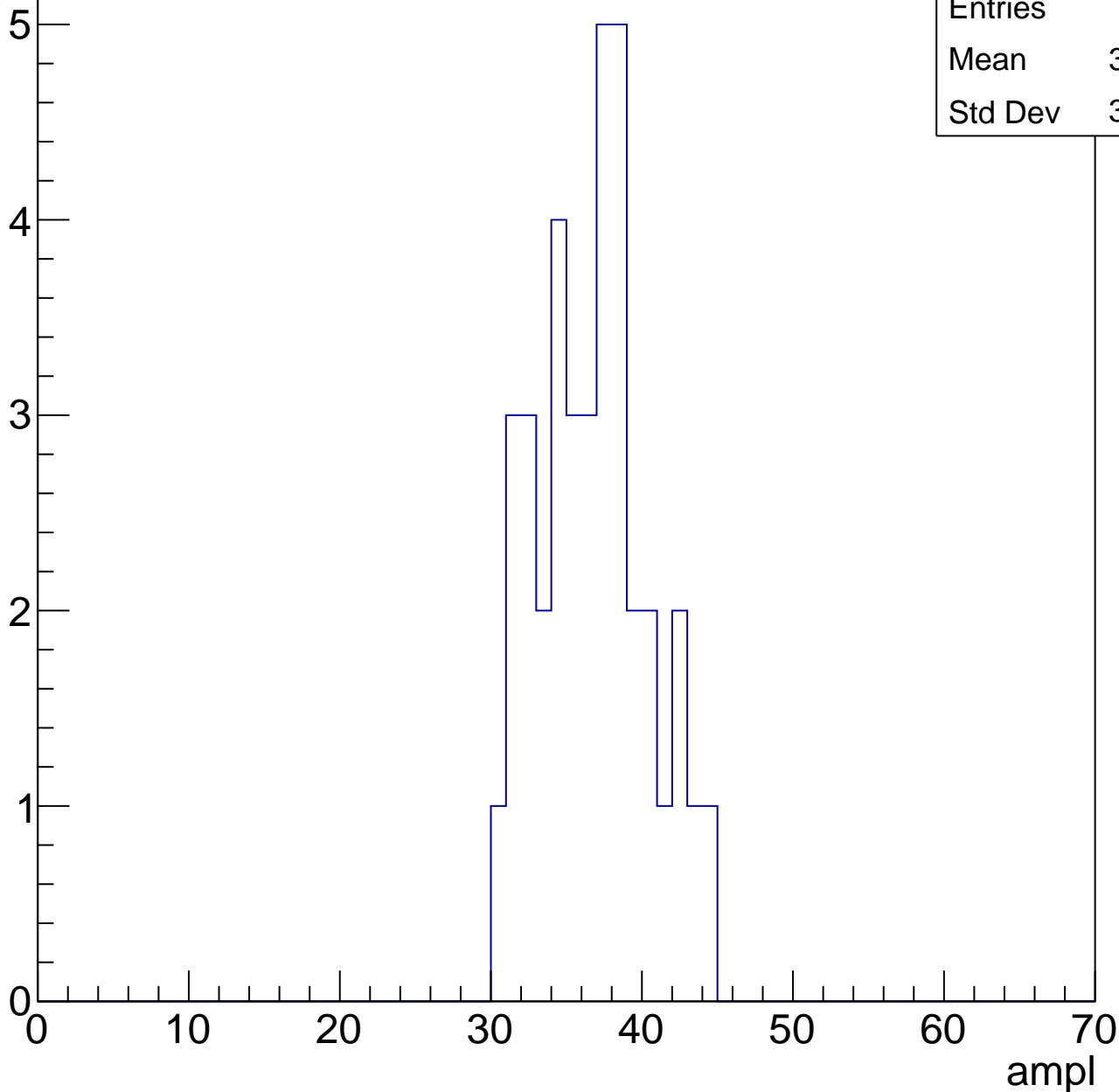


B1L103S, U14-ch99, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

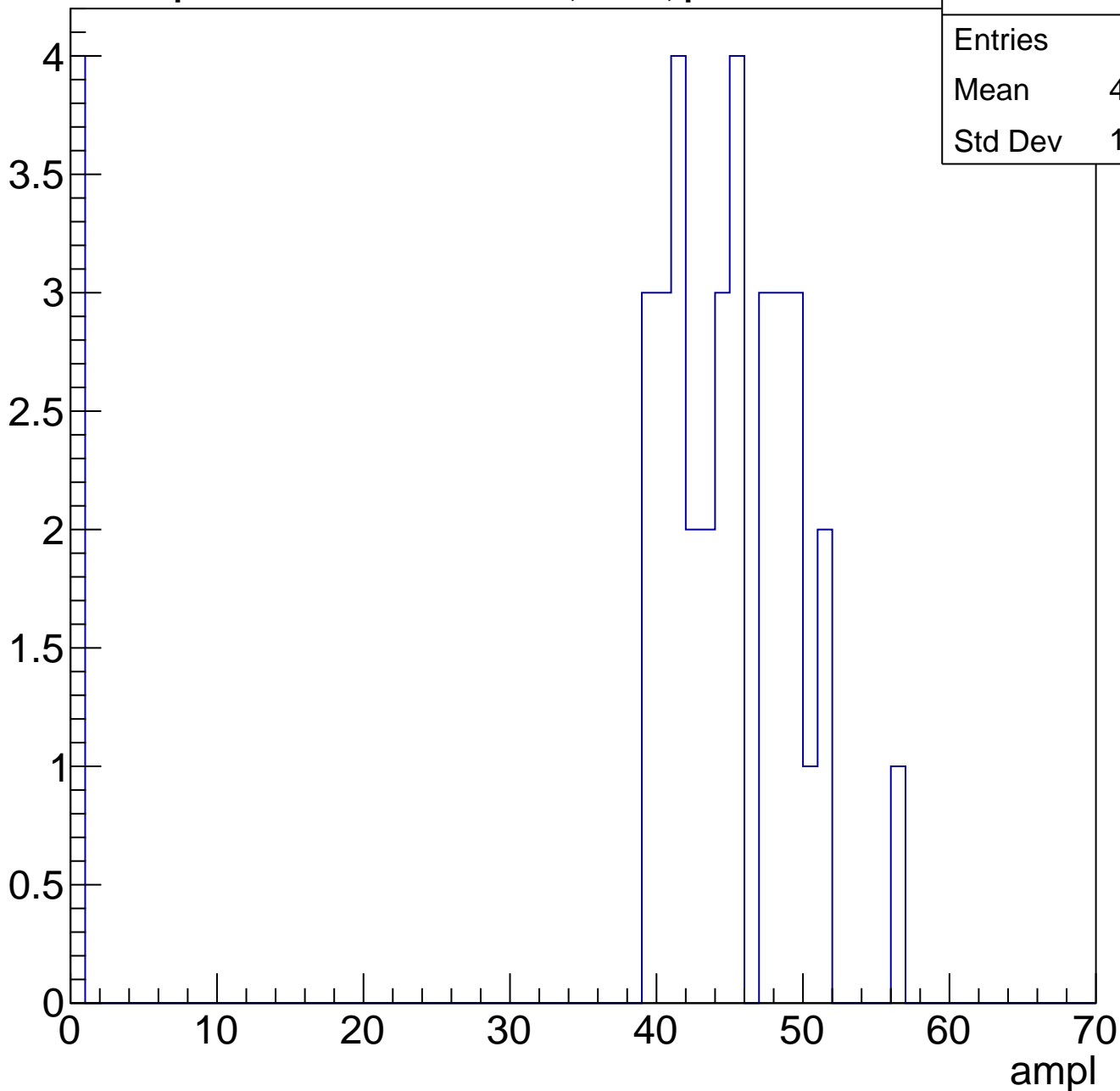
Entries	38
Mean	36.29
Std Dev	3.546



B1L103S, U14-ch99, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

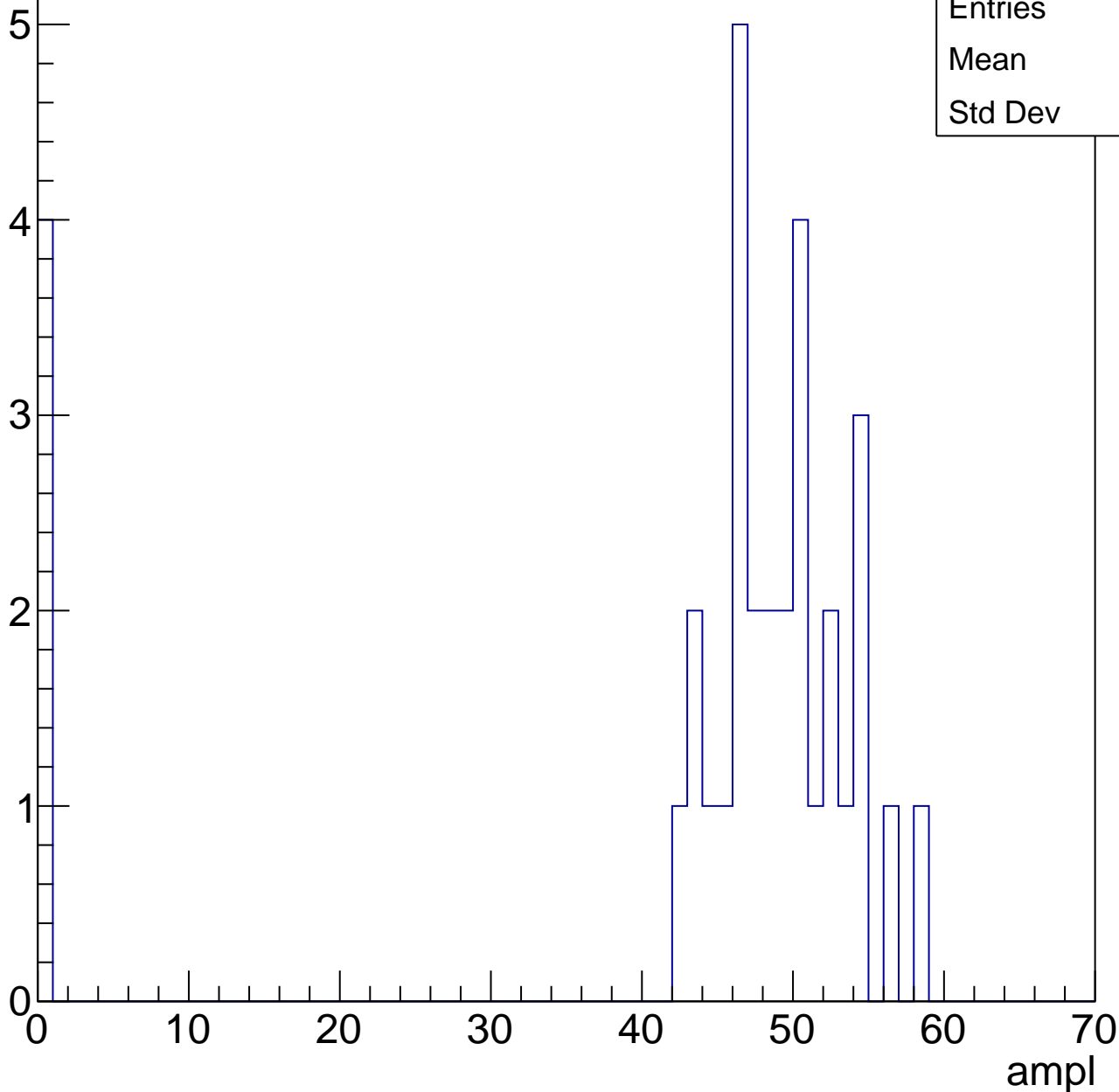


B1L103S, U14-ch99, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

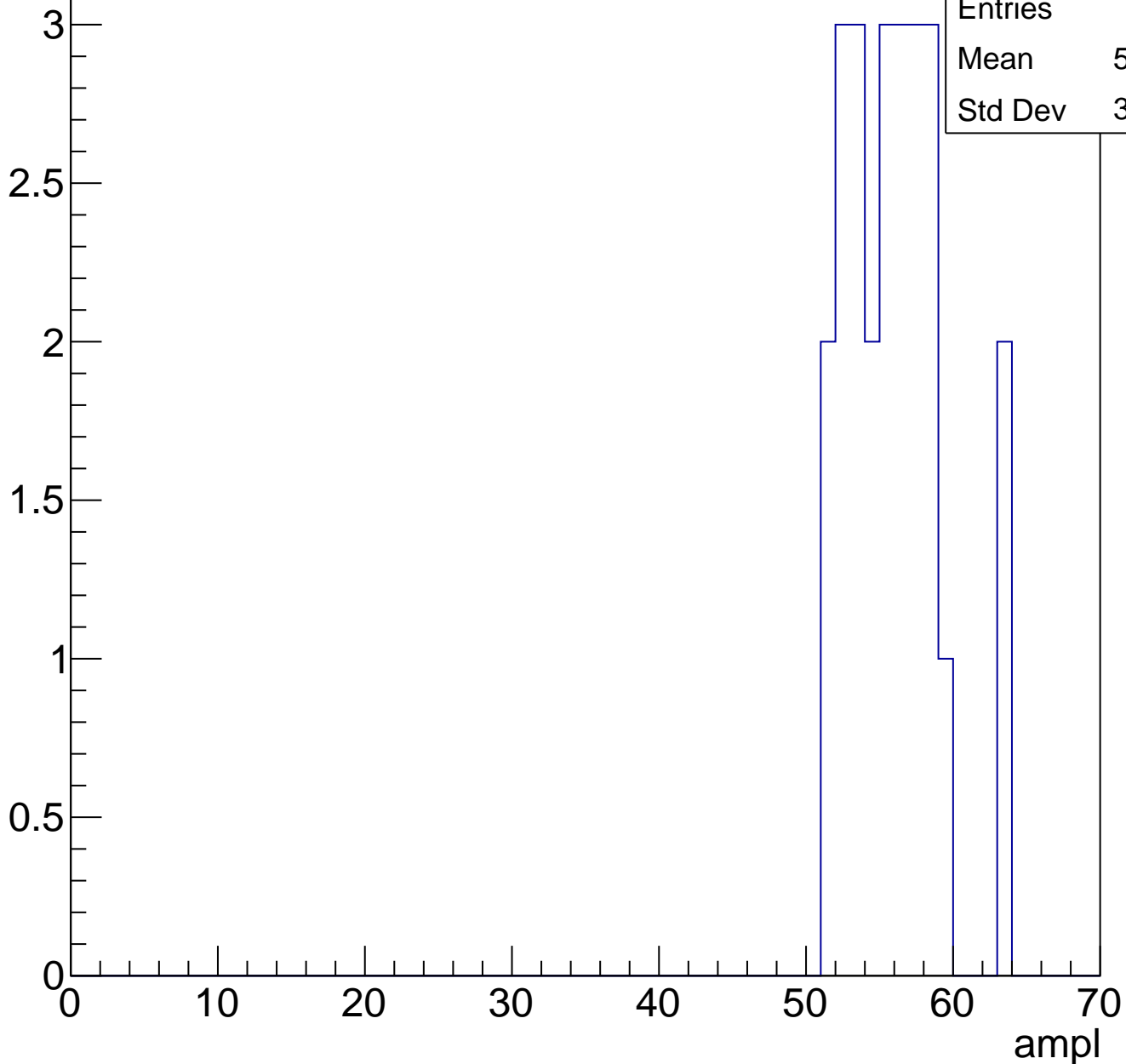
Entries	33
Mean	43
Std Dev	16.4



B1L103S, U14-ch99, adc4

calib_packv5_041523_1651.root, FC#0, port C2

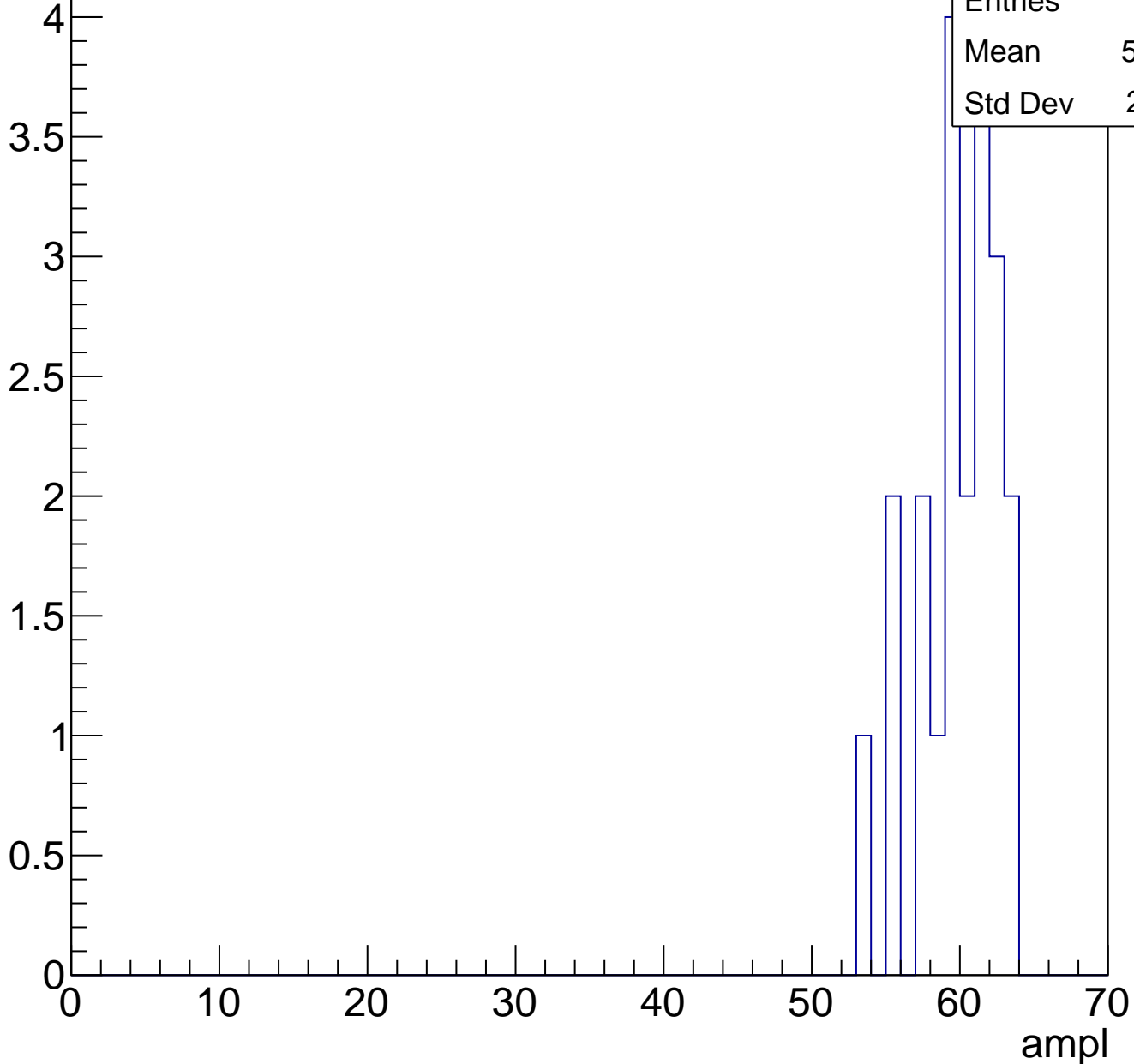
Entry



B1L103S, U14-ch99, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch99, adc6

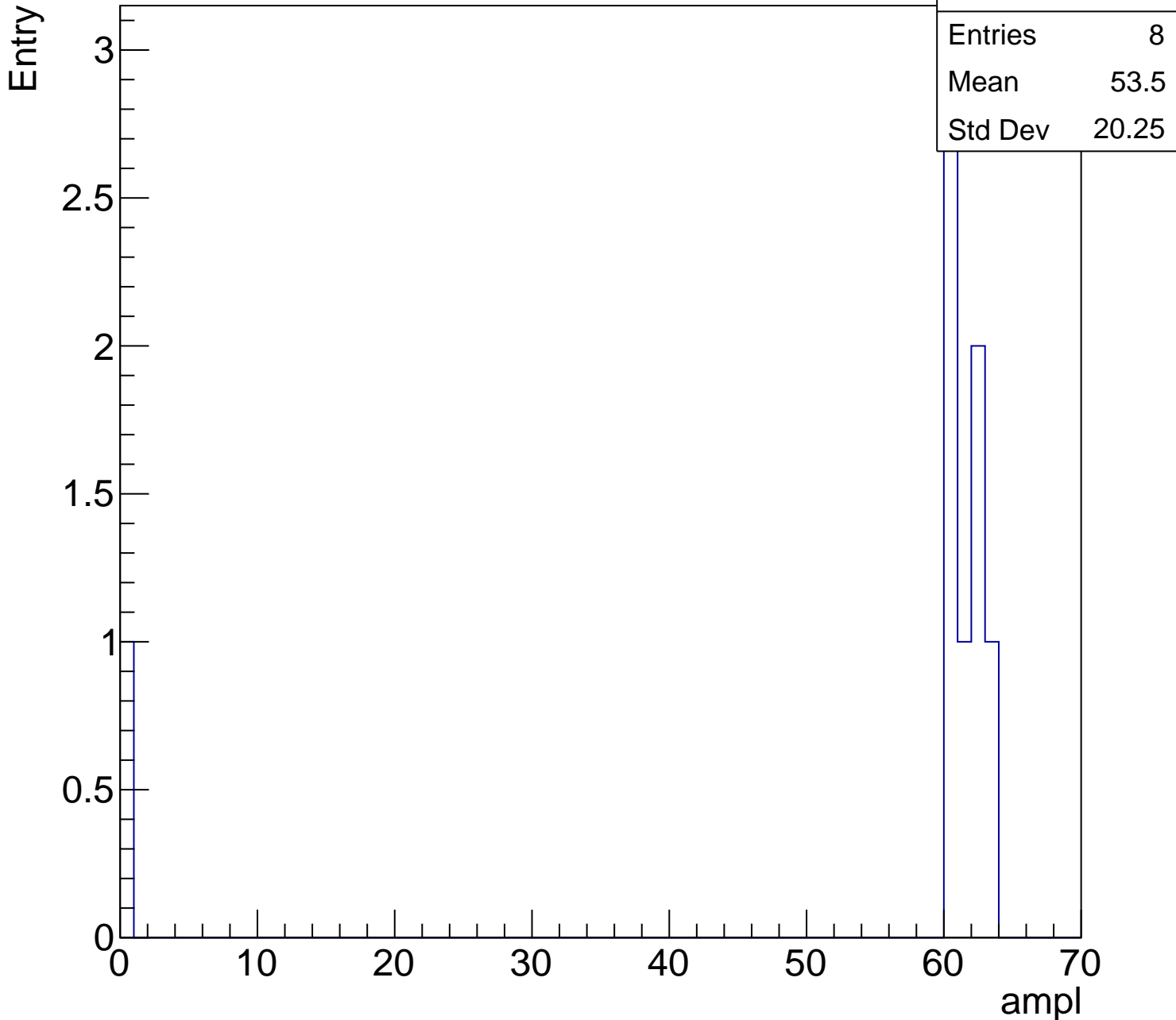
calib_packv5_041523_1651.root, FC#0, port C2

Entry

3
2.5
2
1.5
1
0.5
0

Entries	8
Mean	53.5
Std Dev	20.25

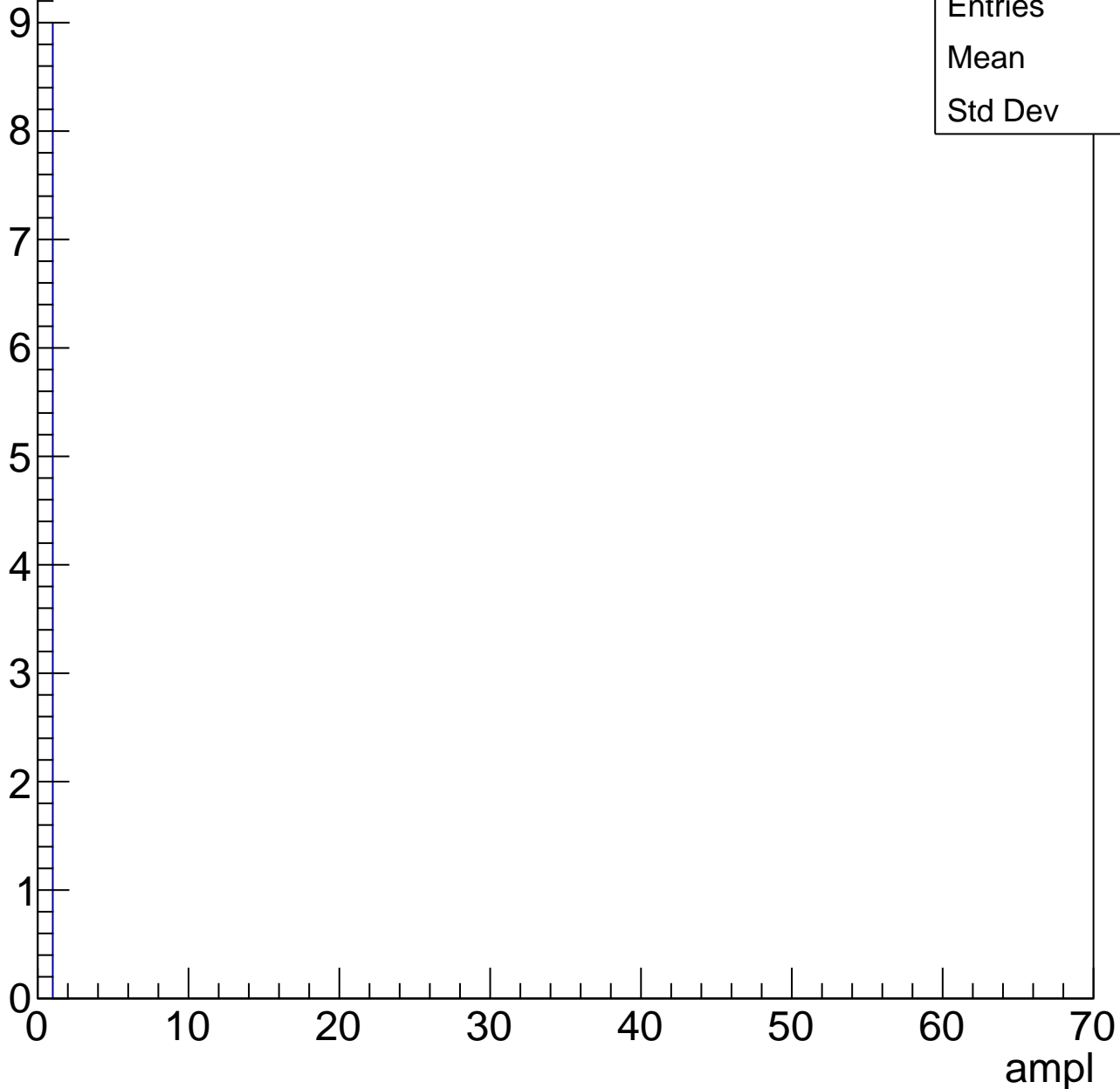
ampl



B1L103S, U14-ch99, adc7

calib_packv5_041523_1651.root, FC#0, port C2

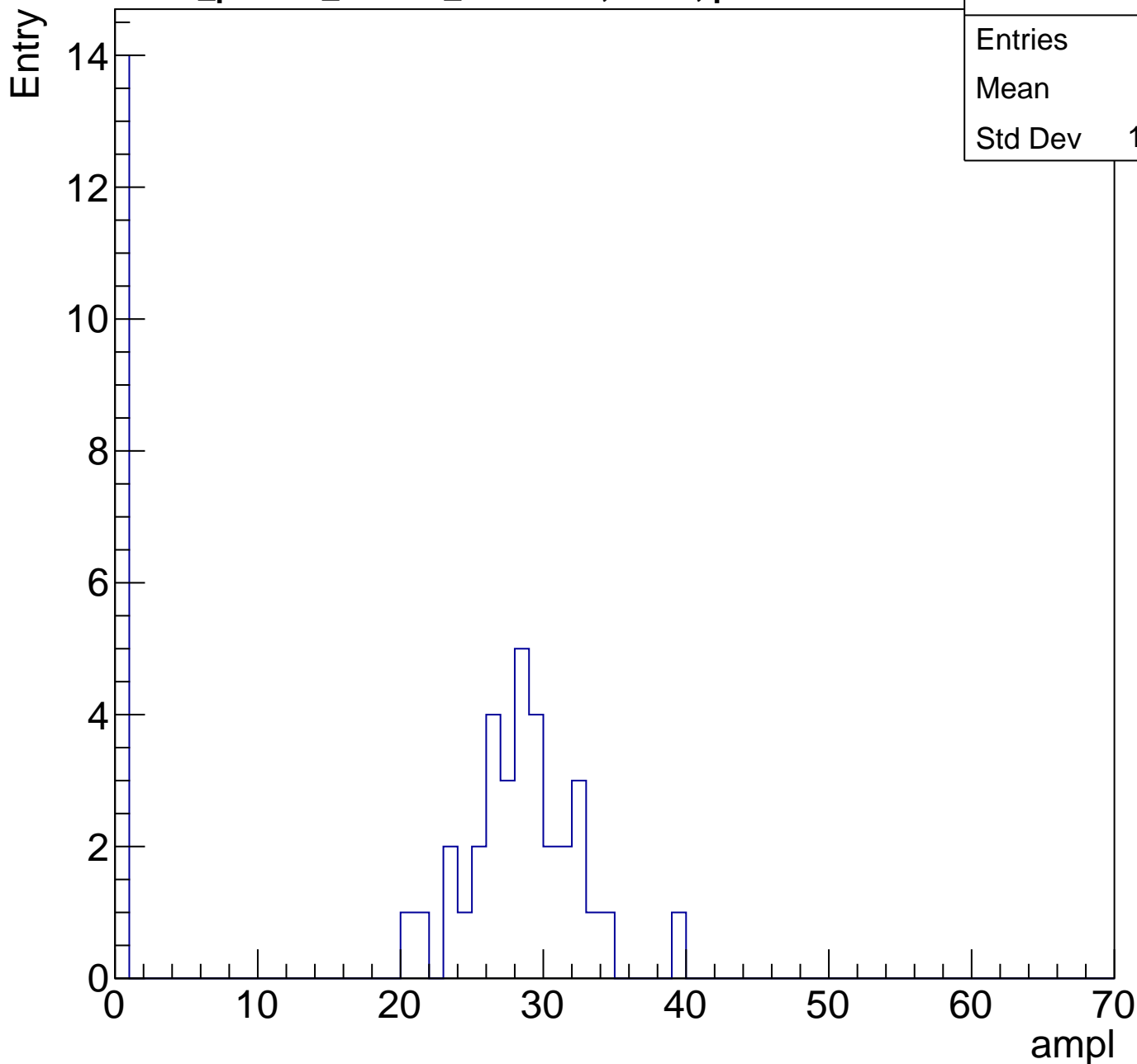
Entry



B1L103S, U14-ch100, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	47
Mean	19.7
Std Dev	13.22

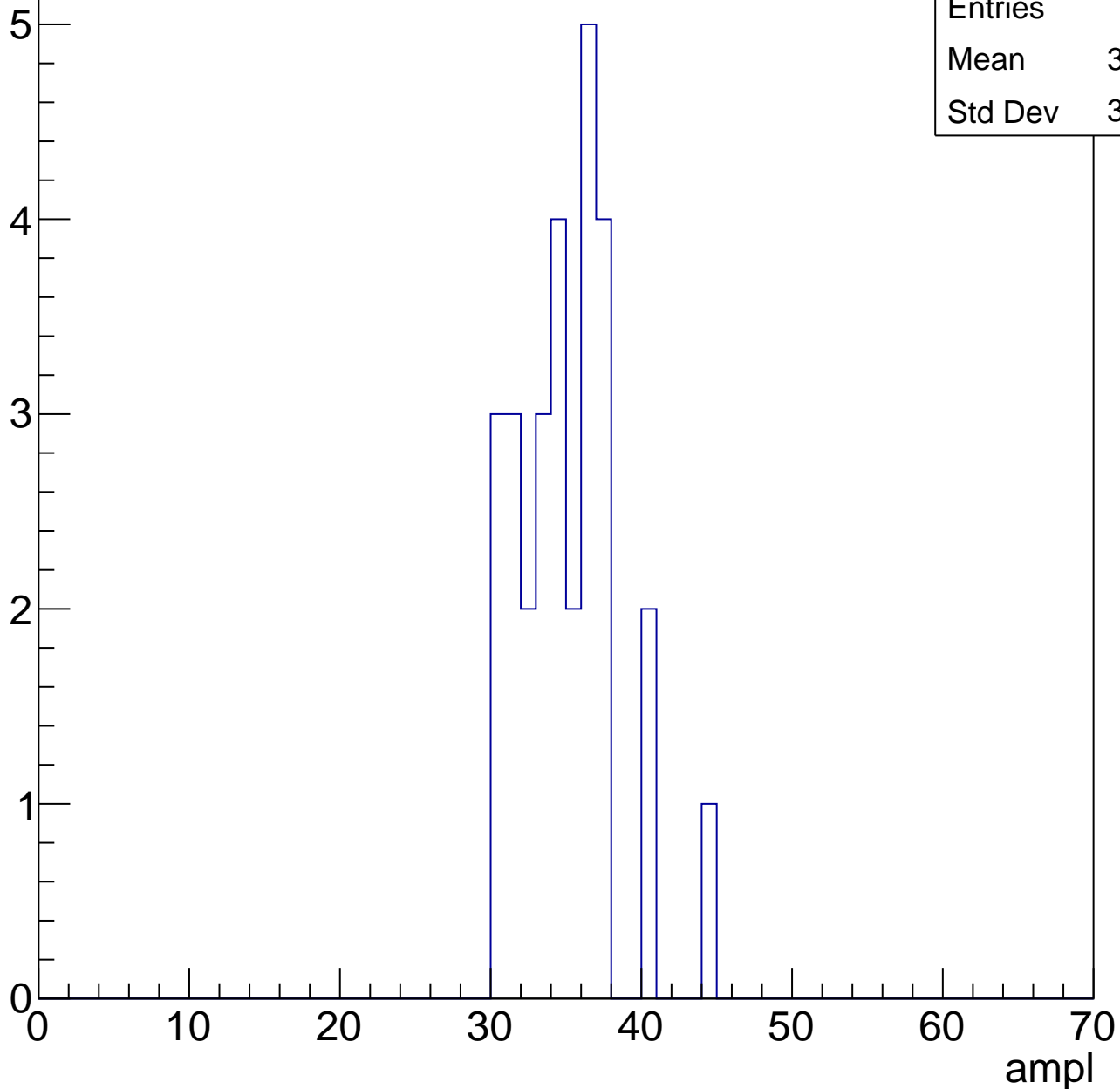


B1L103S, U14-ch100, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	29
Mean	34.62
Std Dev	3.242

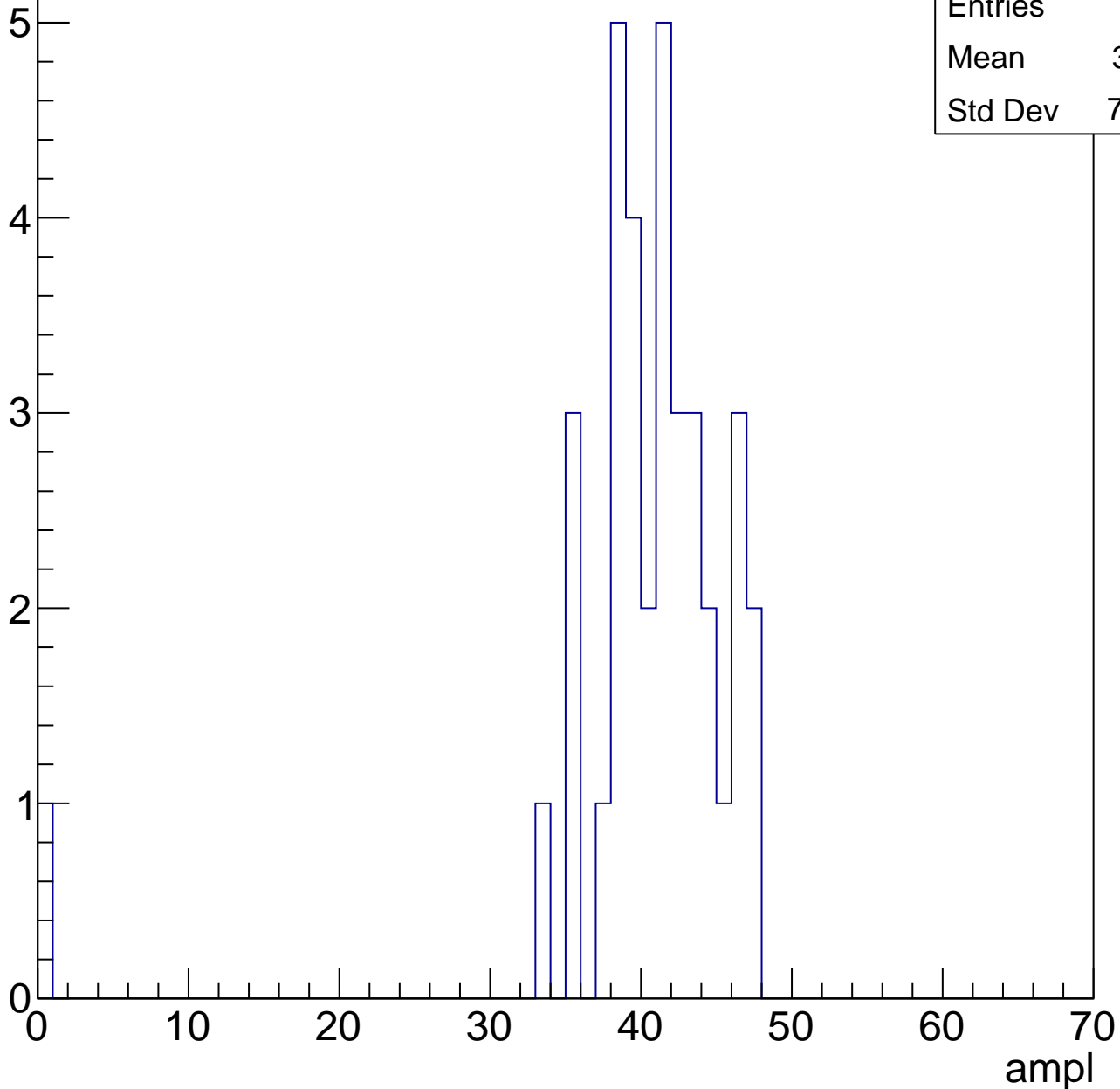


B1L103S, U14-ch100, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	36
Mean	39.61
Std Dev	7.562

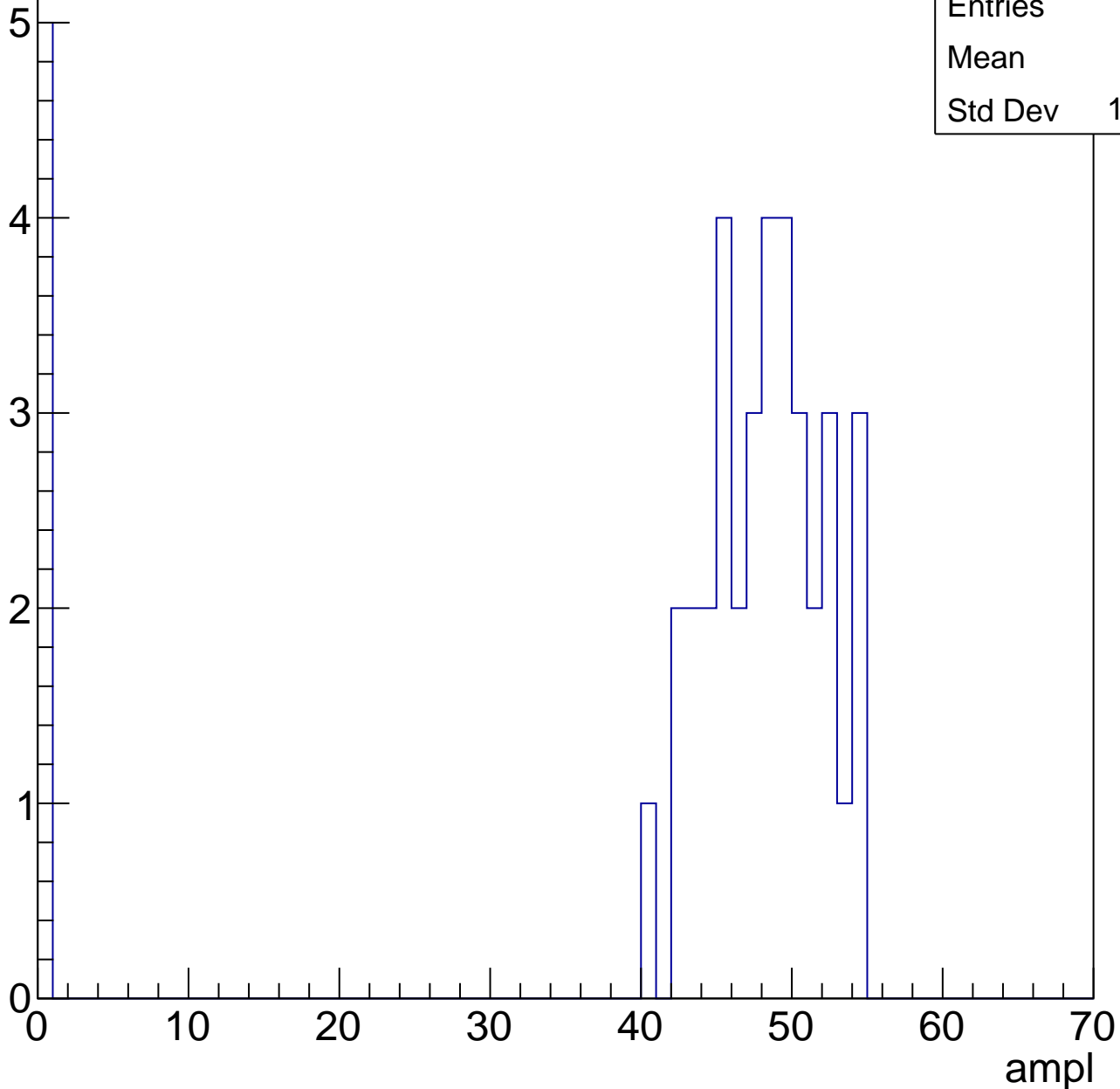


B1L103S, U14-ch100, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

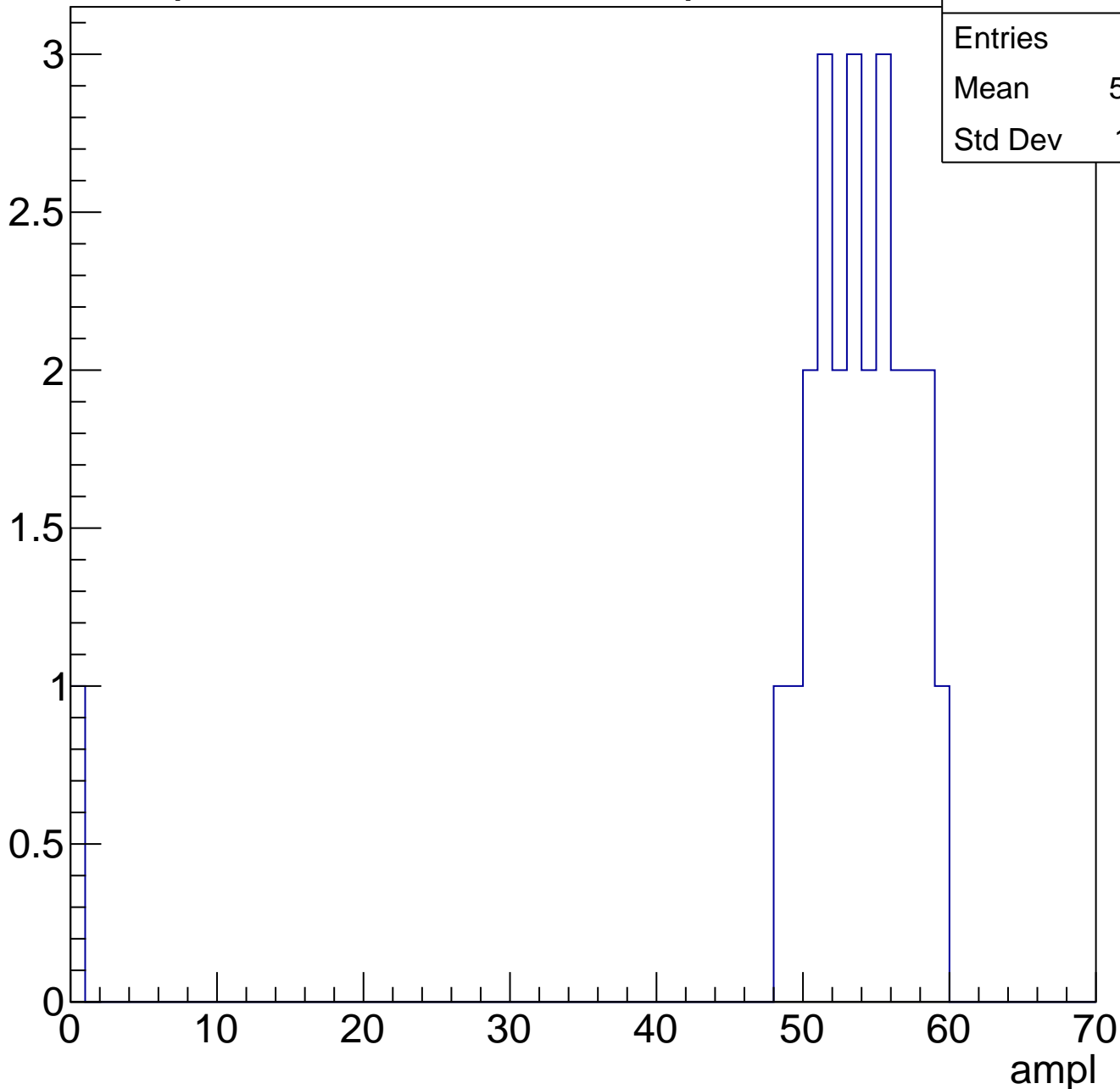
Entries	41
Mean	42
Std Dev	16.02



B1L103S, U14-ch100, adc4

calib_packv5_041523_1651.root, FC#0, port C2

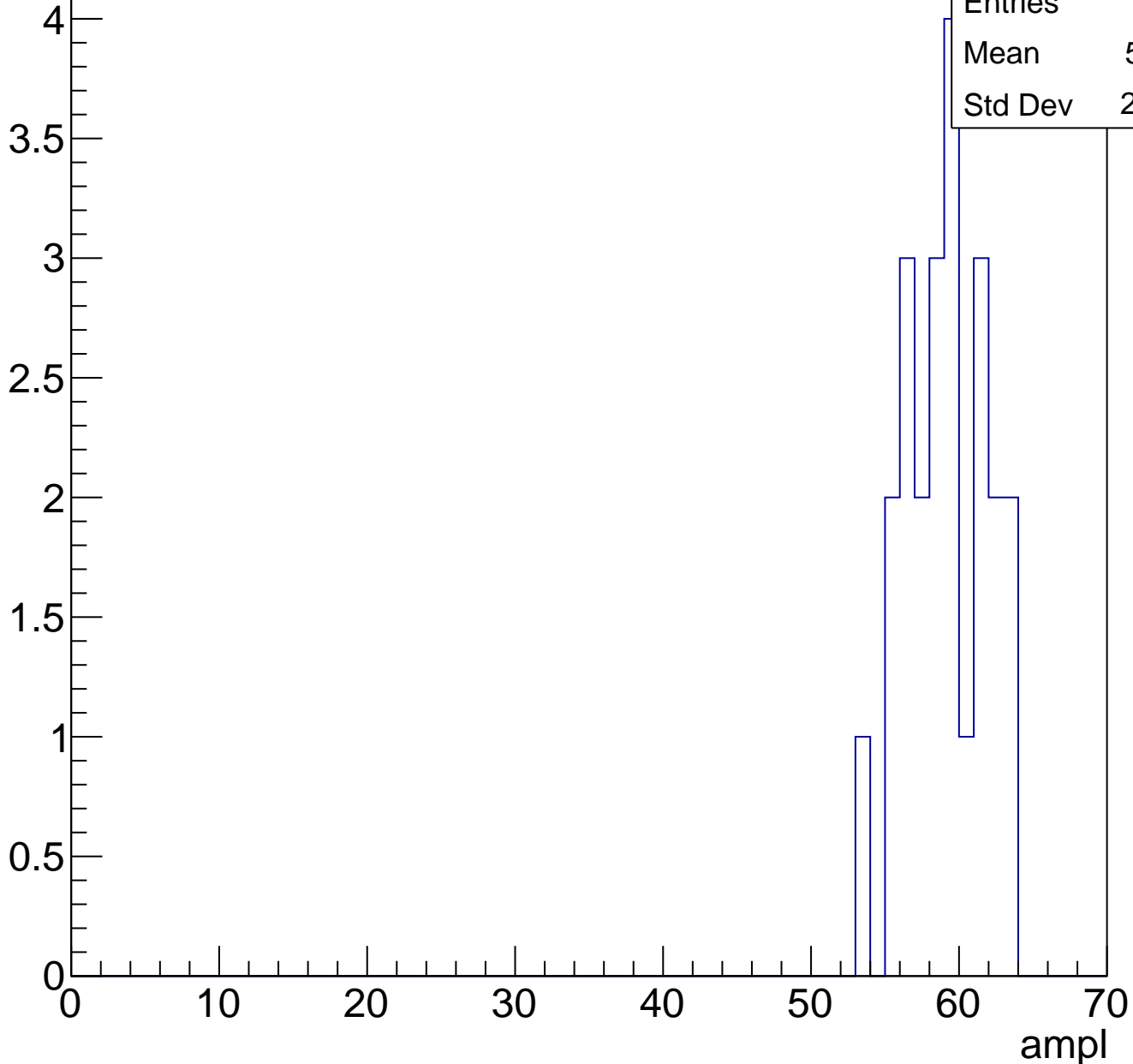
Entry



B1L103S, U14-ch100, adc5

calib_packv5_041523_1651.root, FC#0, port C2

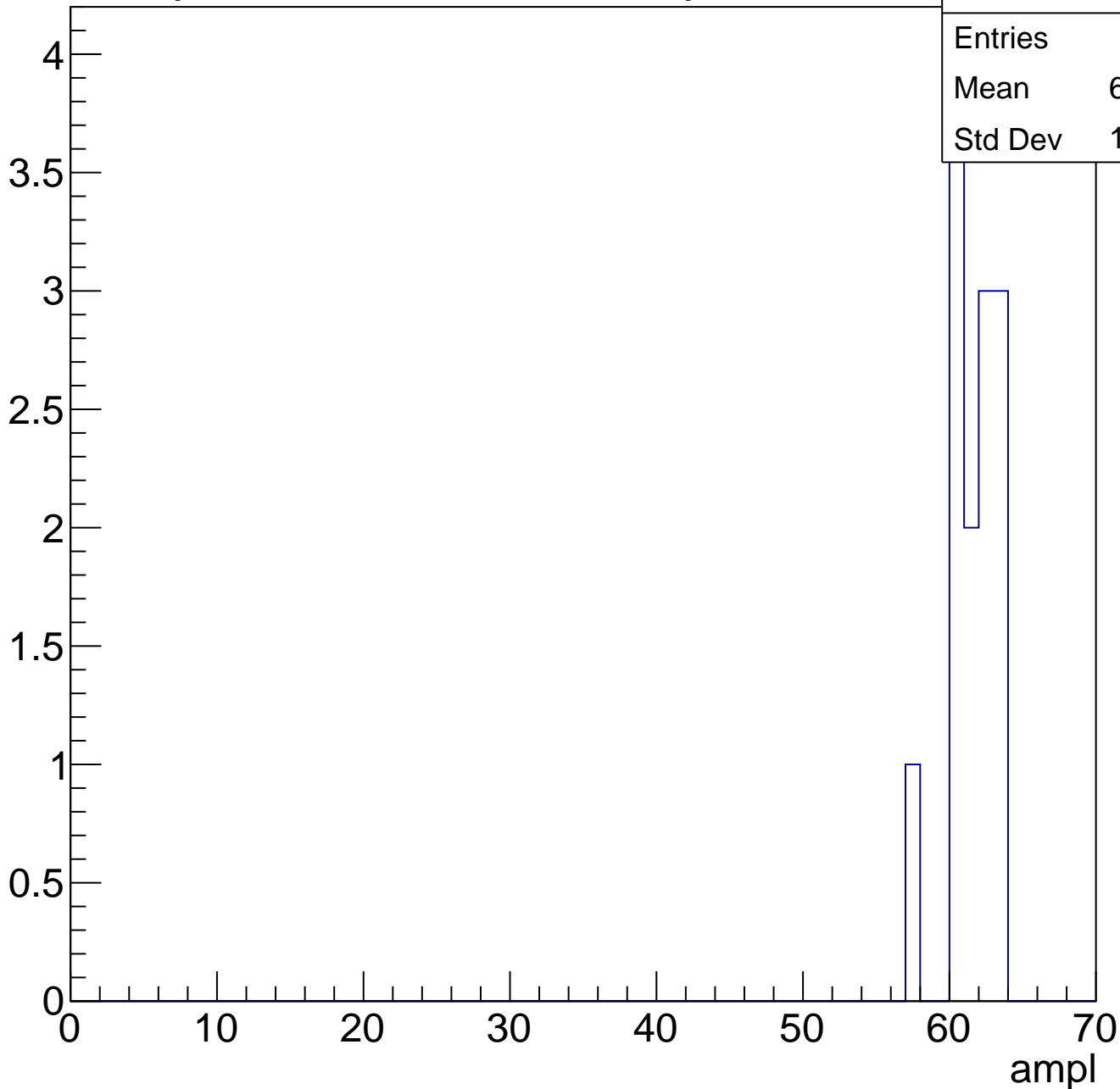
Entry



B1L103S, U14-ch100, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

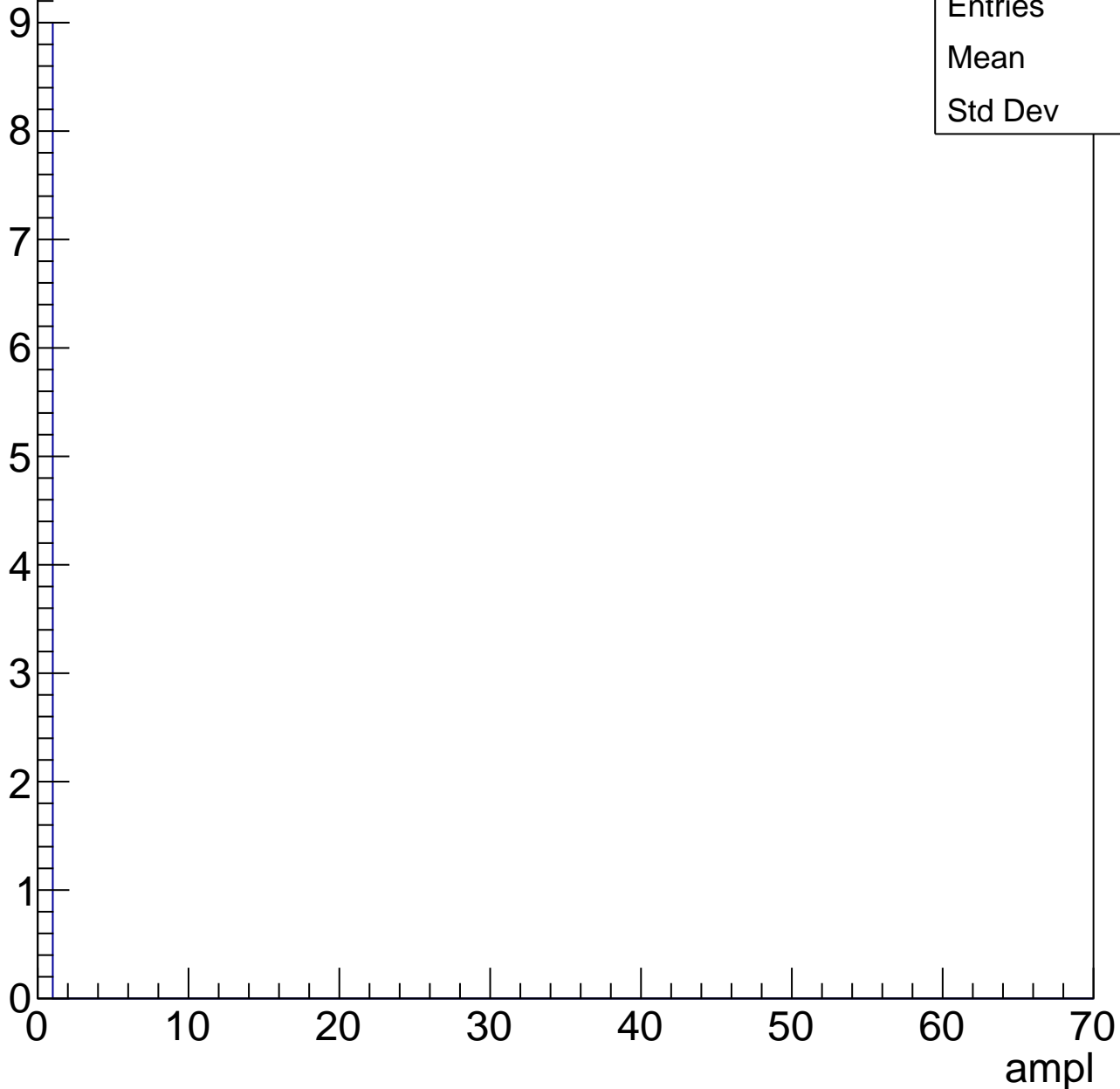


B1L103S, U14-ch100, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	9
Mean	0
Std Dev	0

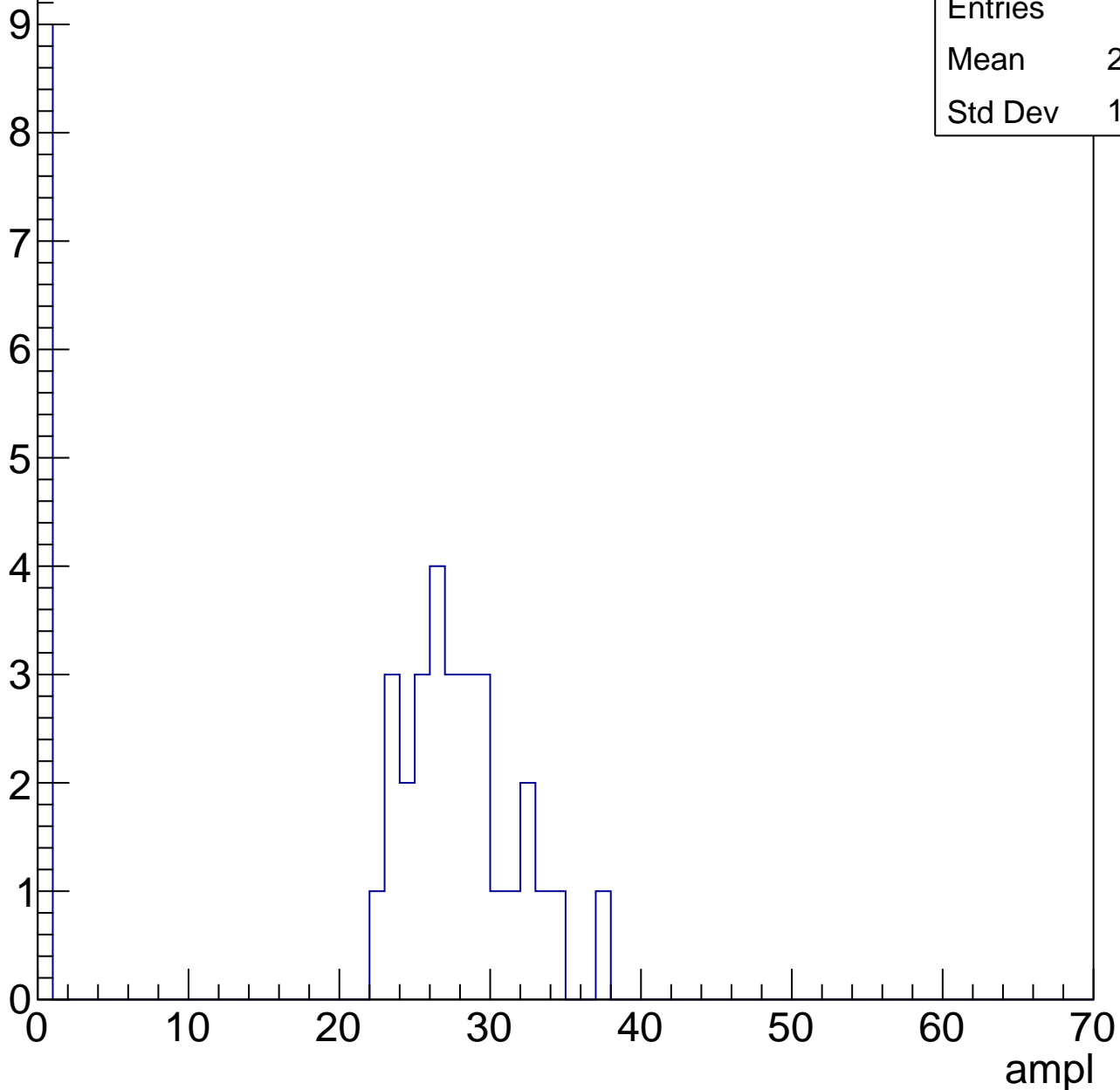


B1L103S, U14-ch101, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

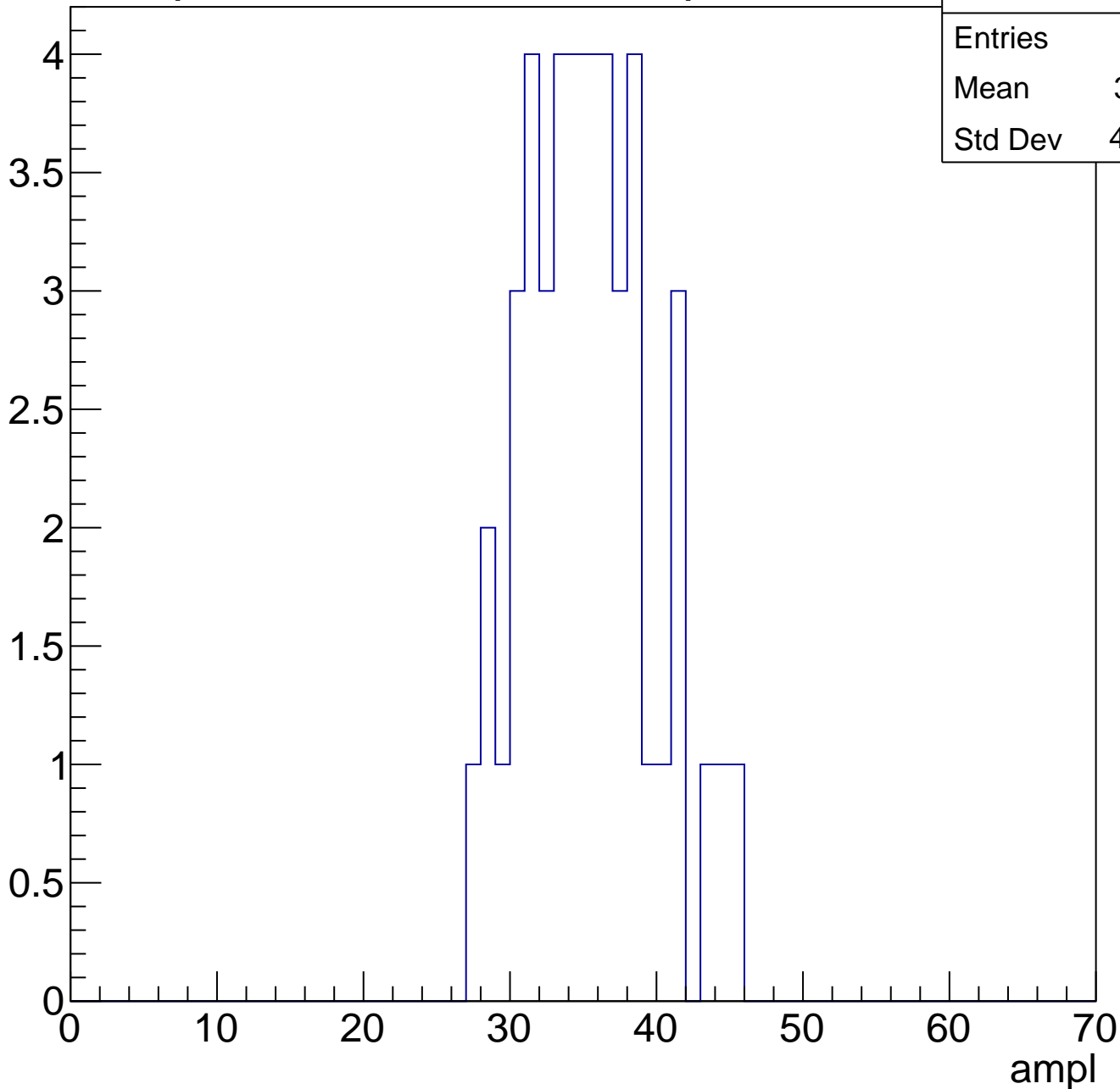
Entries	38
Mean	21.03
Std Dev	12.13



B1L103S, U14-ch101, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

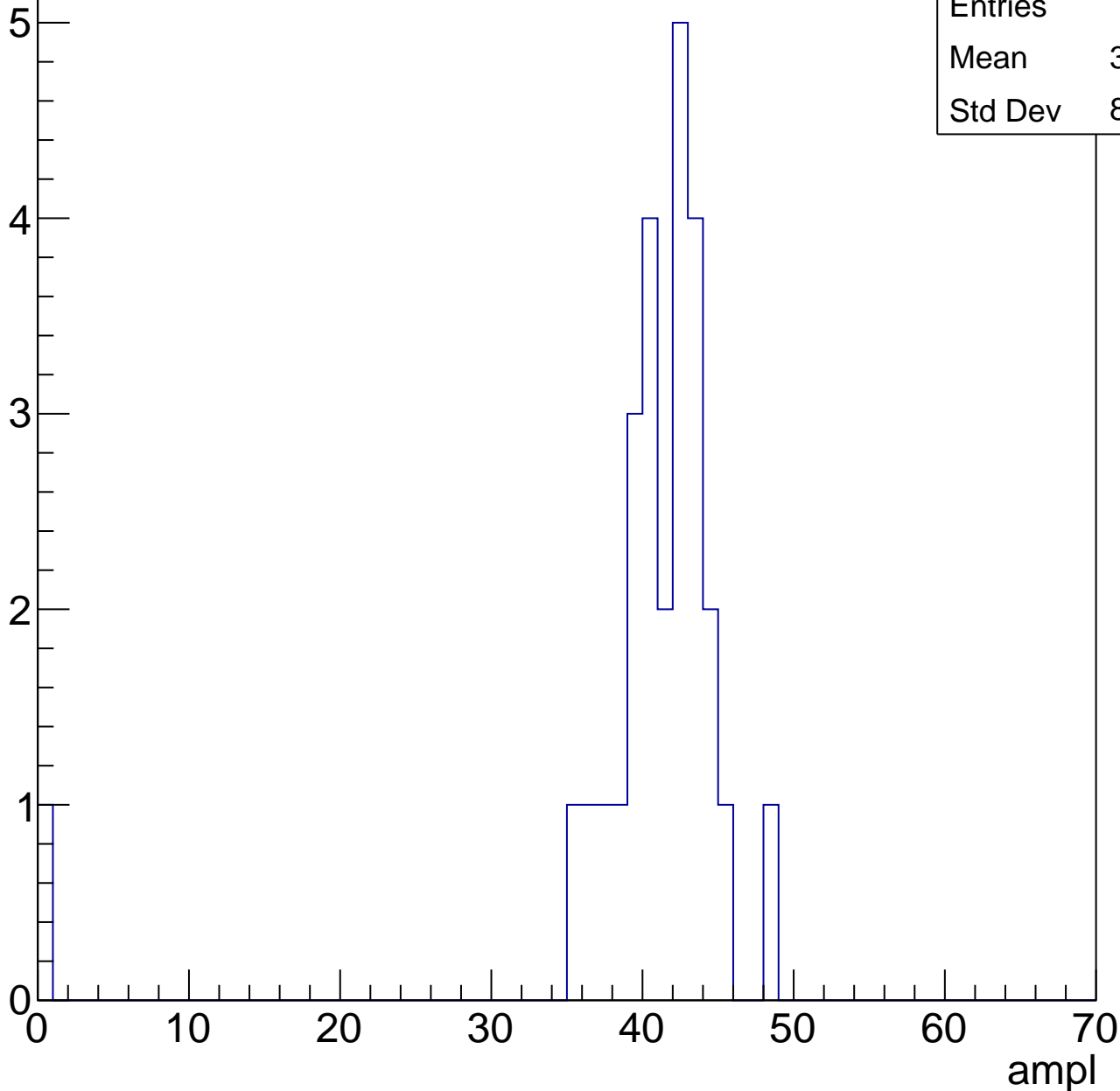


B1L103S, U14-ch101, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	27
Mean	39.56
Std Dev	8.234

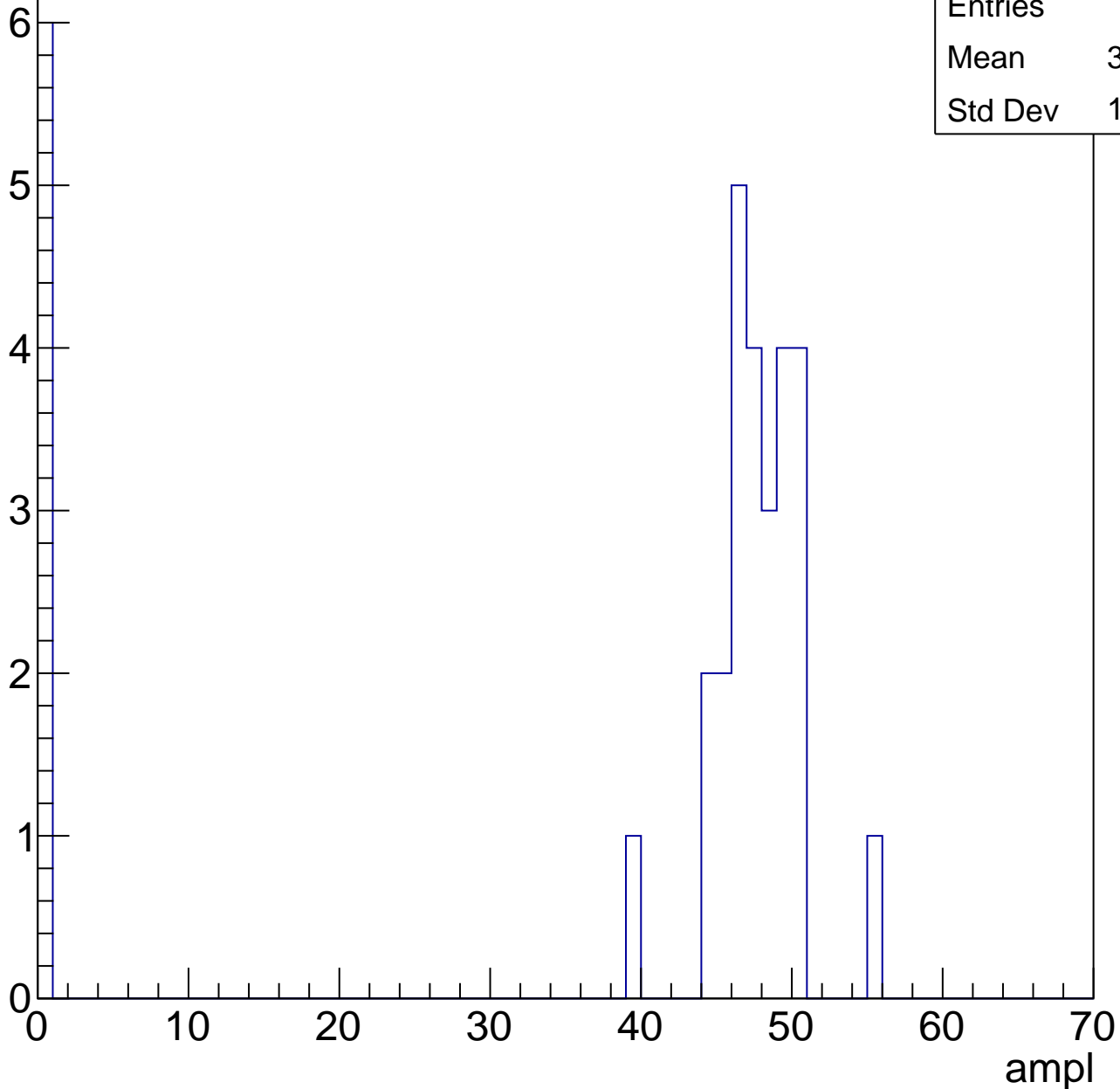


B1L103S, U14-ch101, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	32
Mean	38.44
Std Dev	18.64

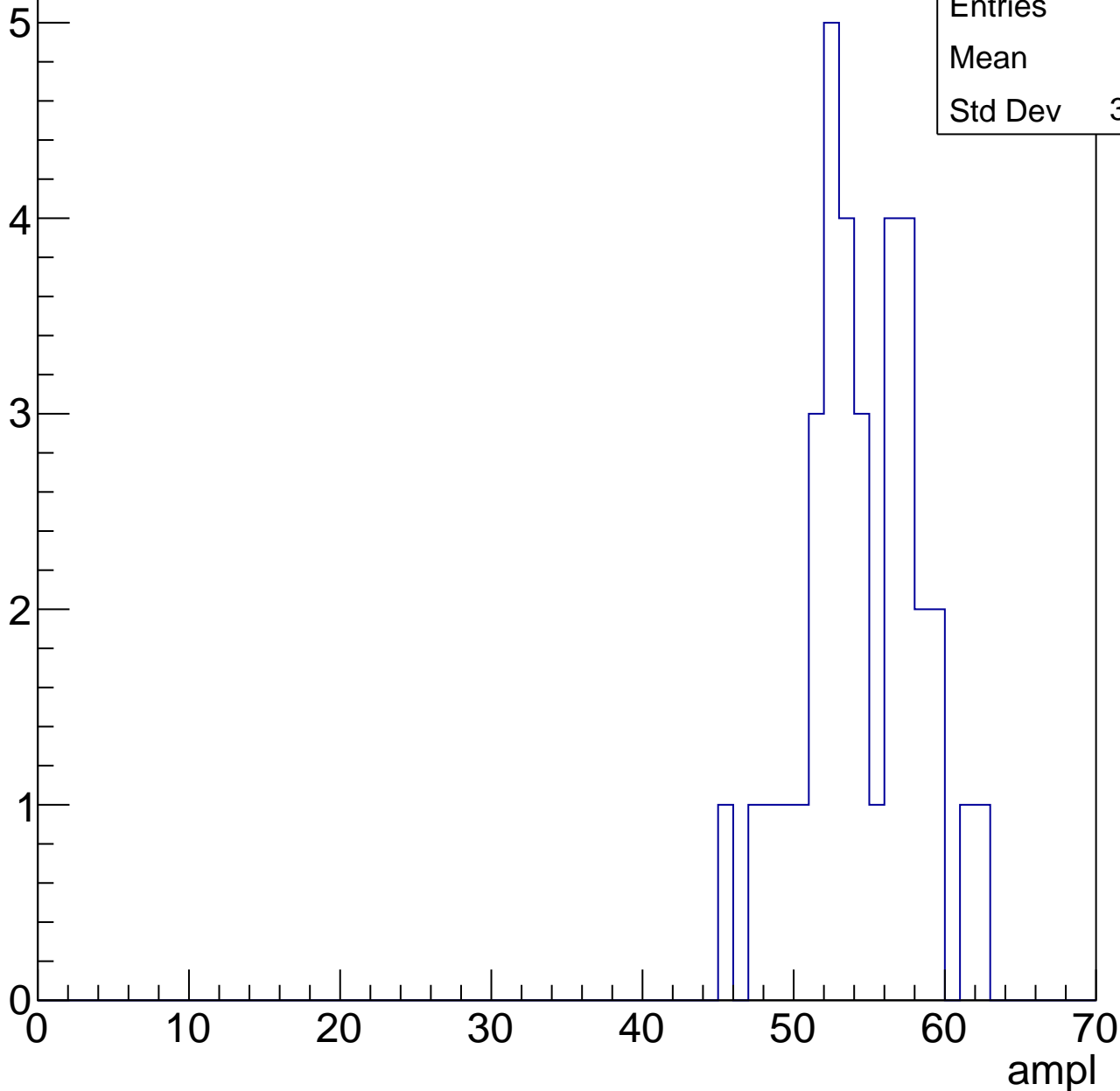


B1L103S, U14-ch101, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

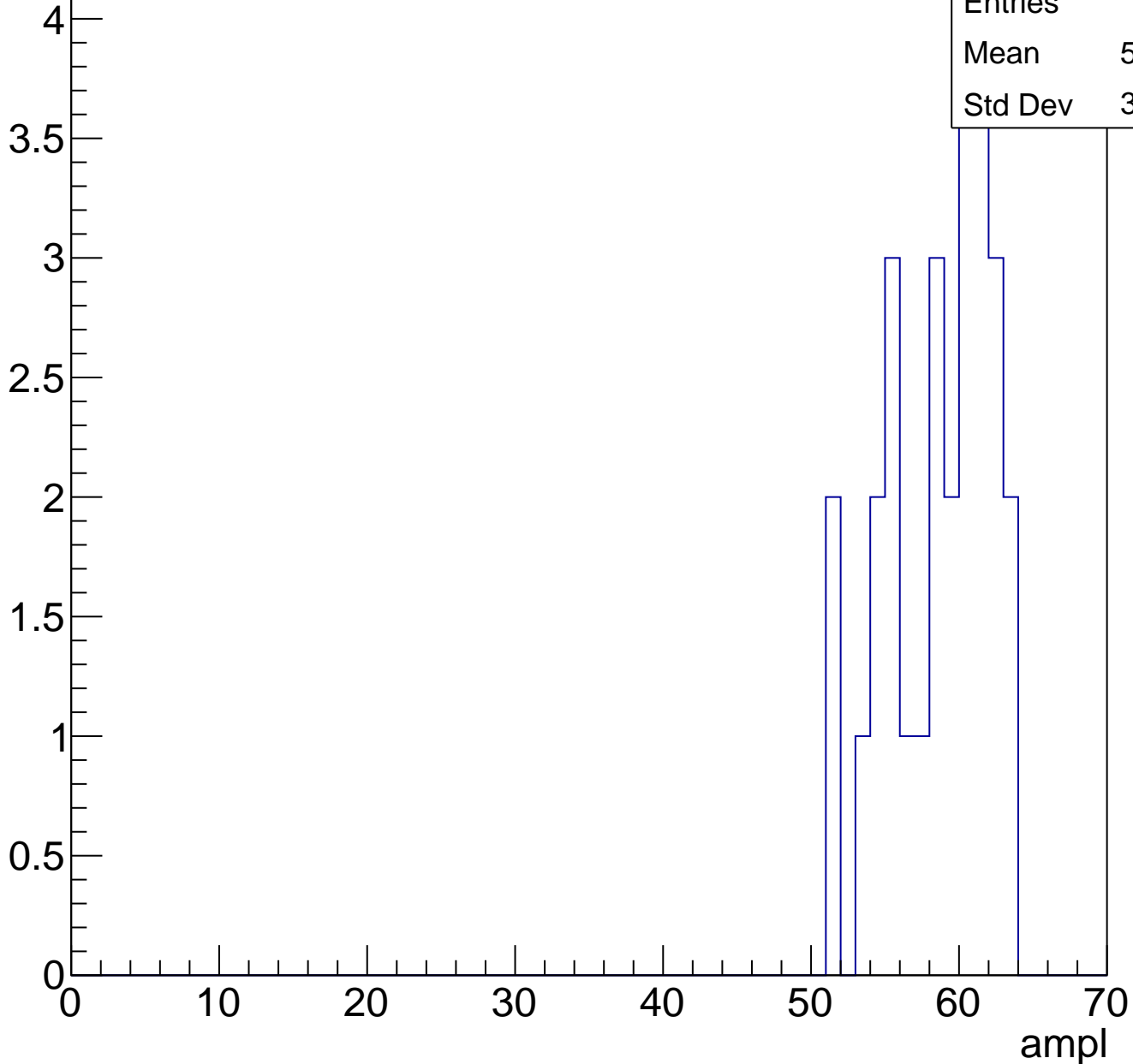
Entries	35
Mean	54
Std Dev	3.802



B1L103S, U14-ch101, adc5

calib_packv5_041523_1651.root, FC#0, port C2

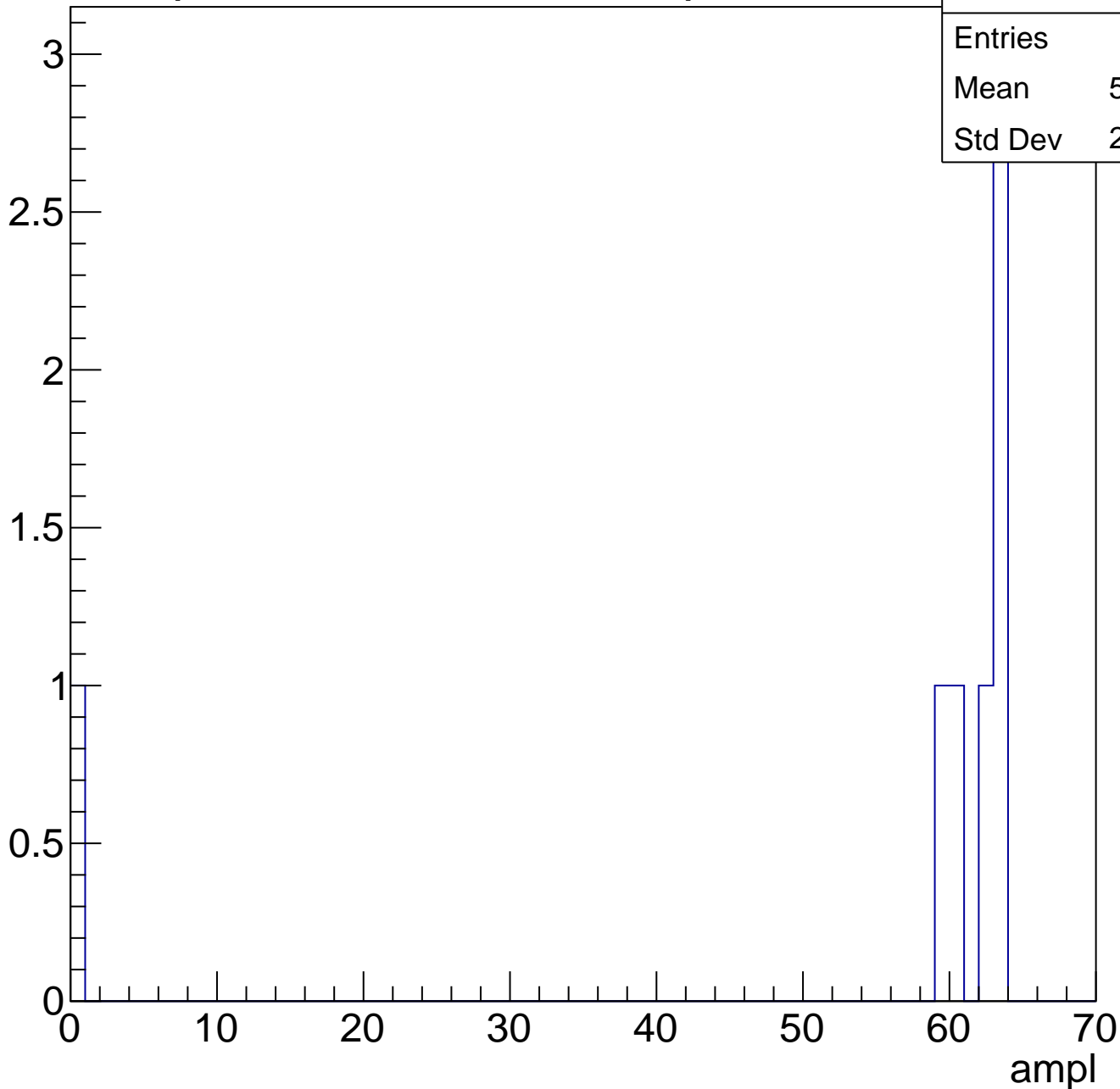
Entry



B1L103S, U14-ch101, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

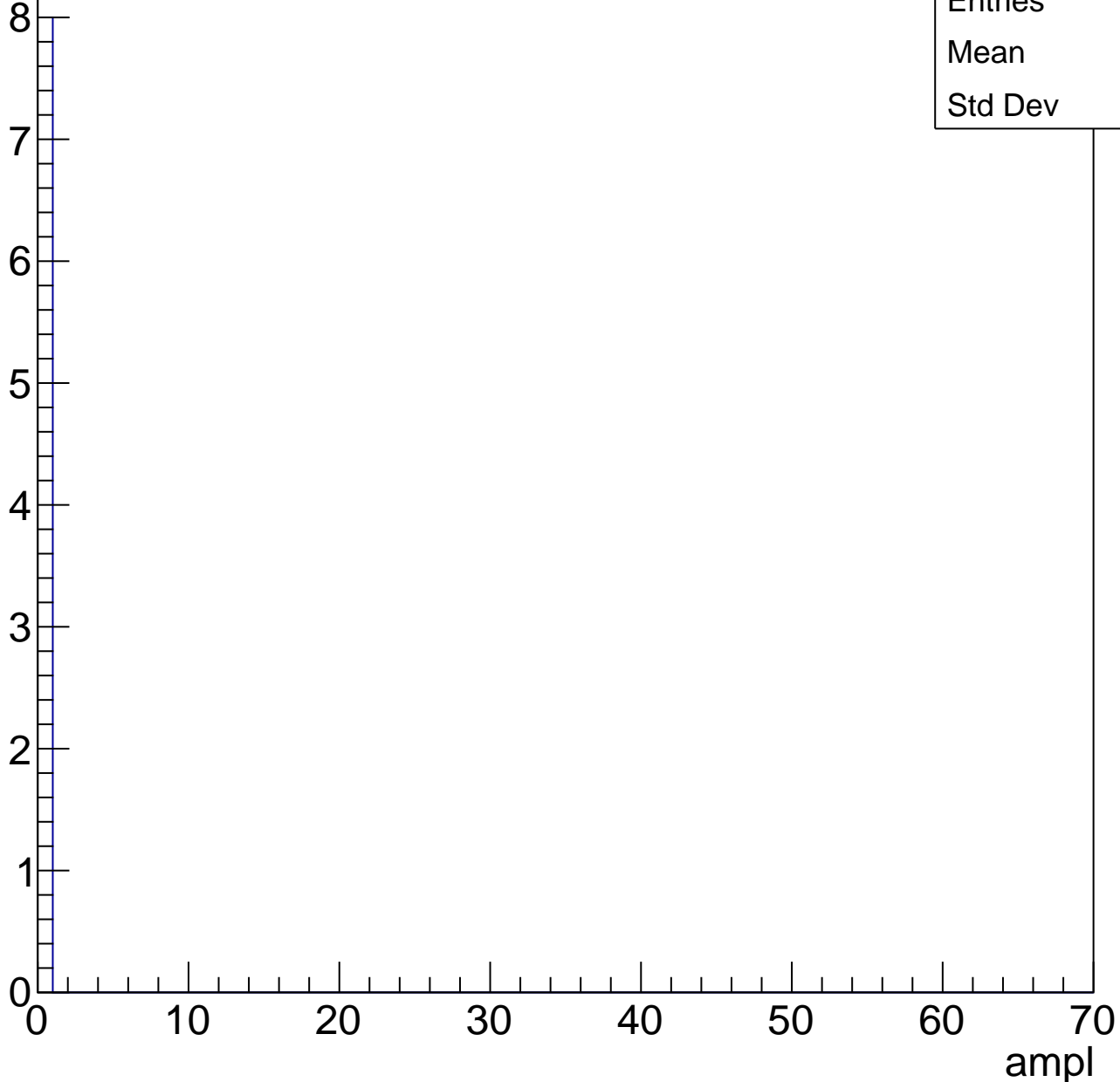


B1L103S, U14-ch101, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	8
Mean	0
Std Dev	0



B1L103S, U14-ch102, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	41
Mean	20.73
Std Dev	12.94

Entry

10

8

6

4

2

0

0

10

20

30

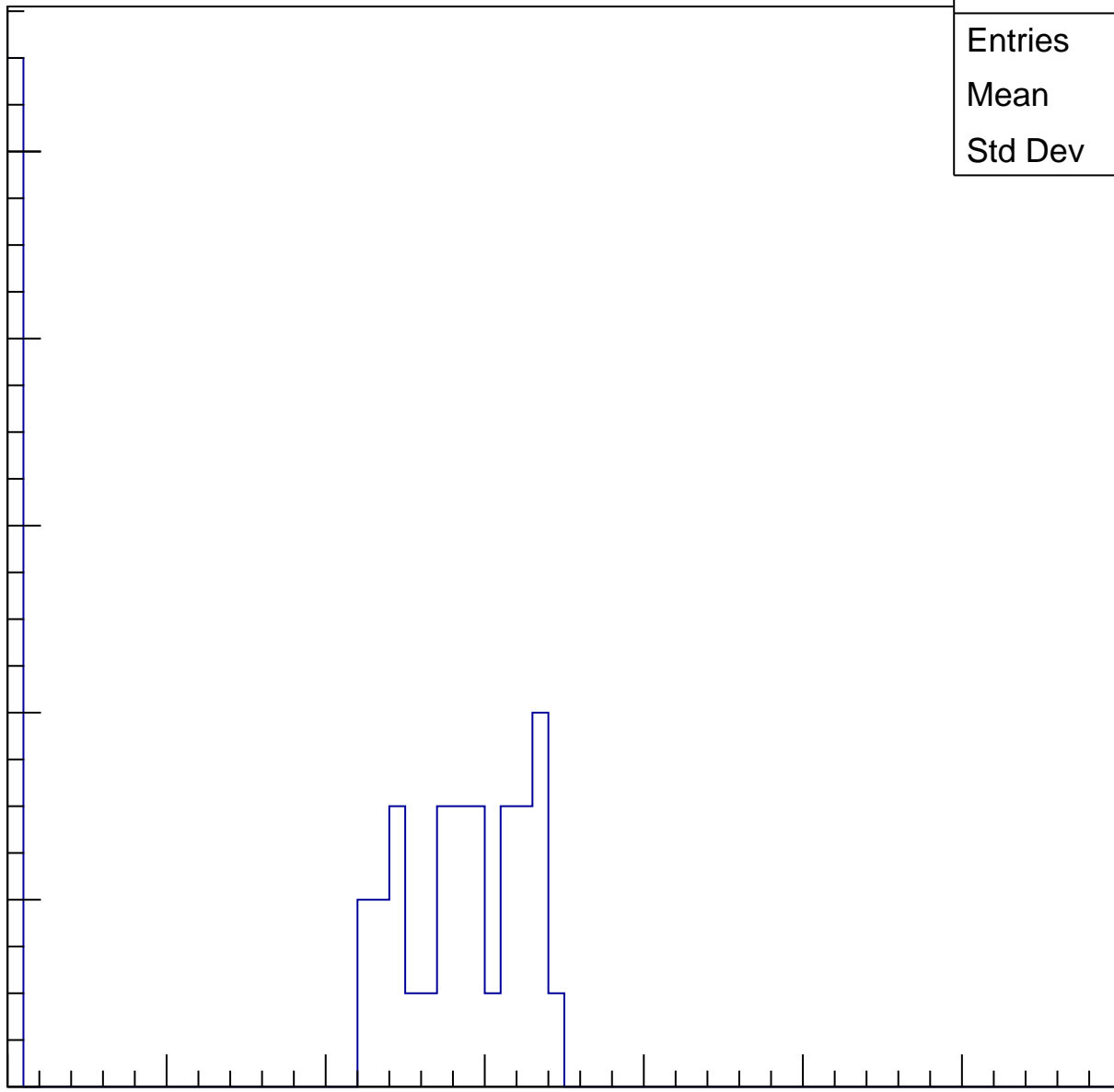
40

50

60

70

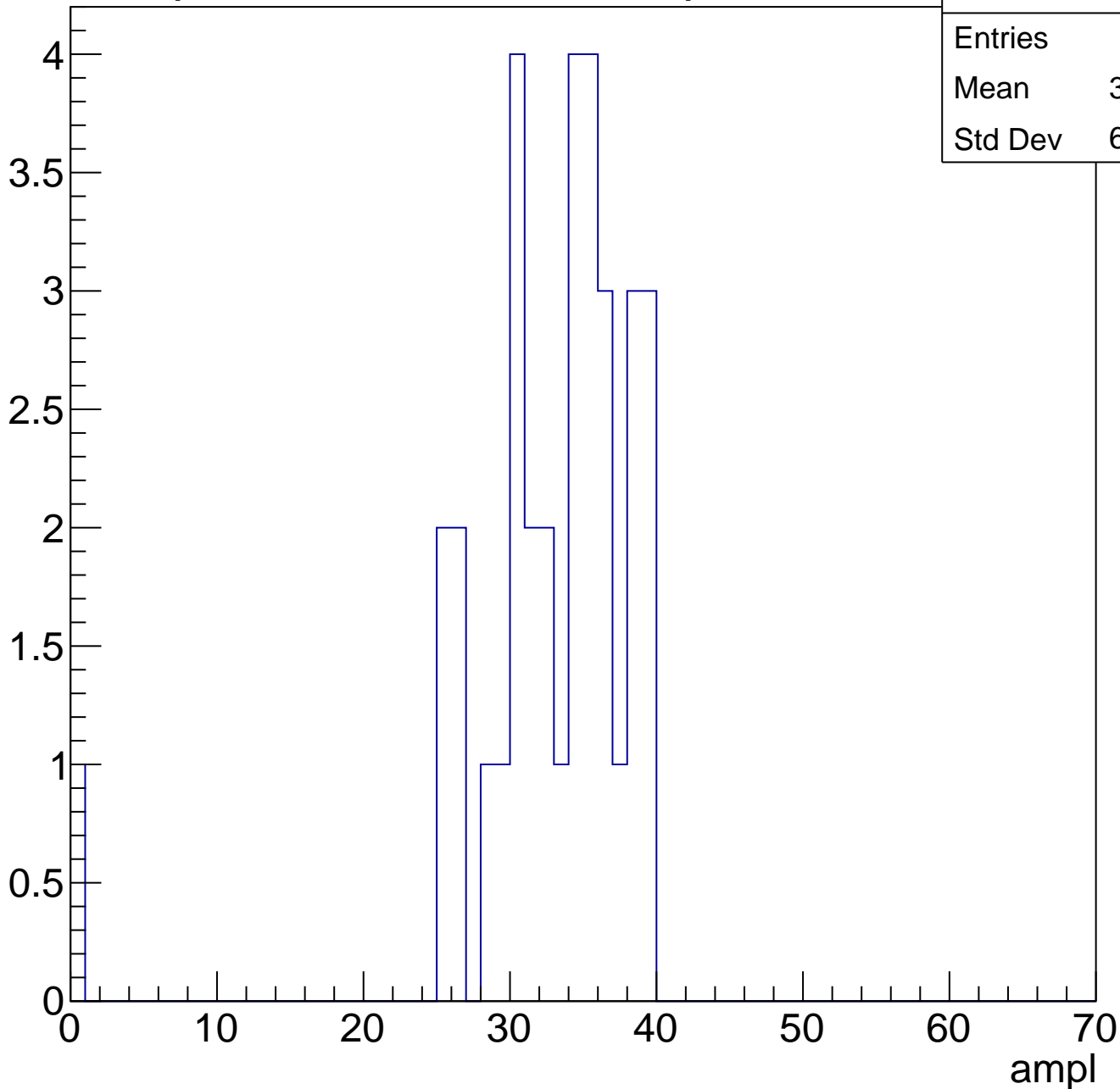
ampl



B1L103S, U14-ch102, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

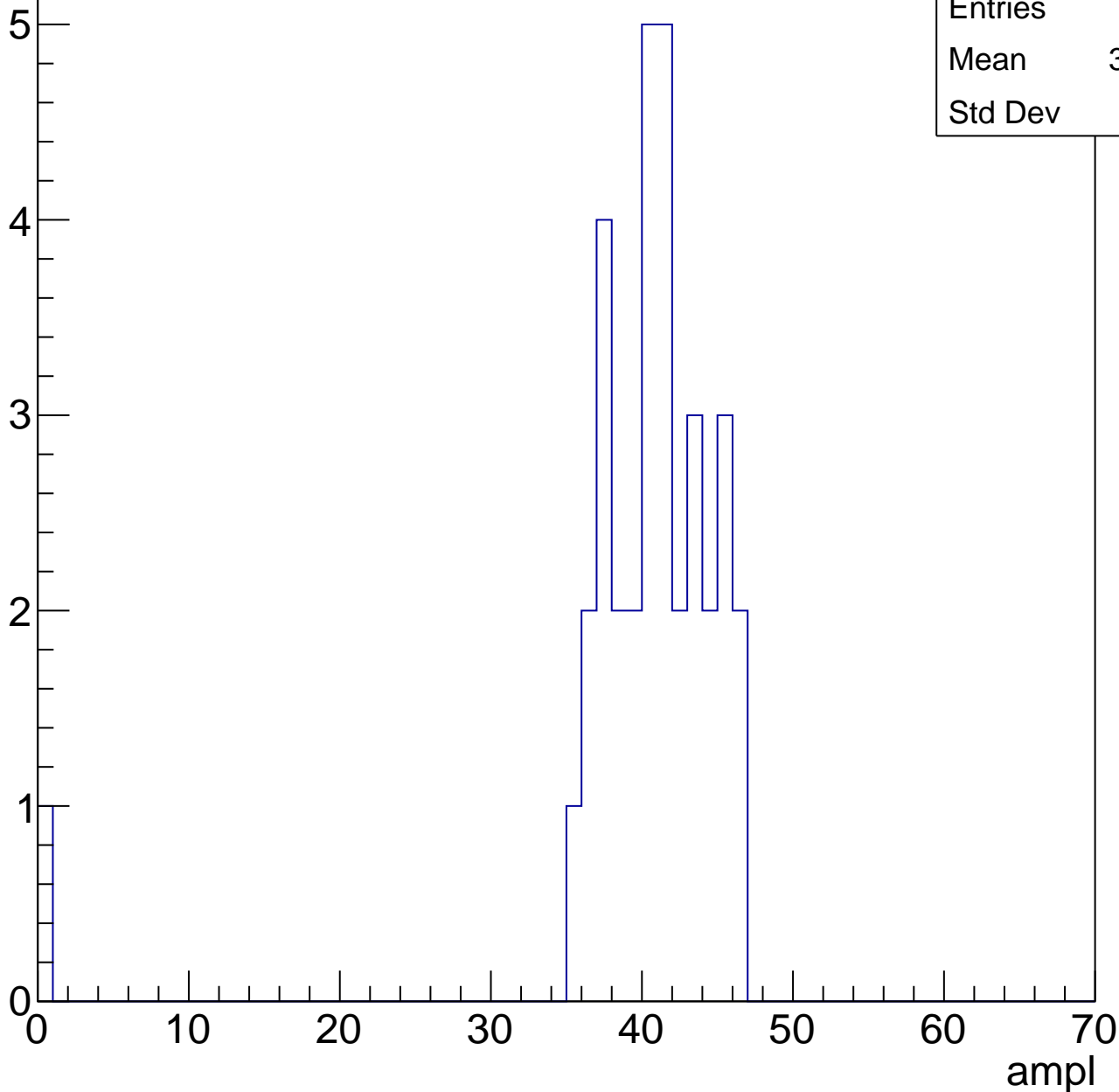


B1L103S, U14-ch102, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	34
Mean	39.47
Std Dev	7.5

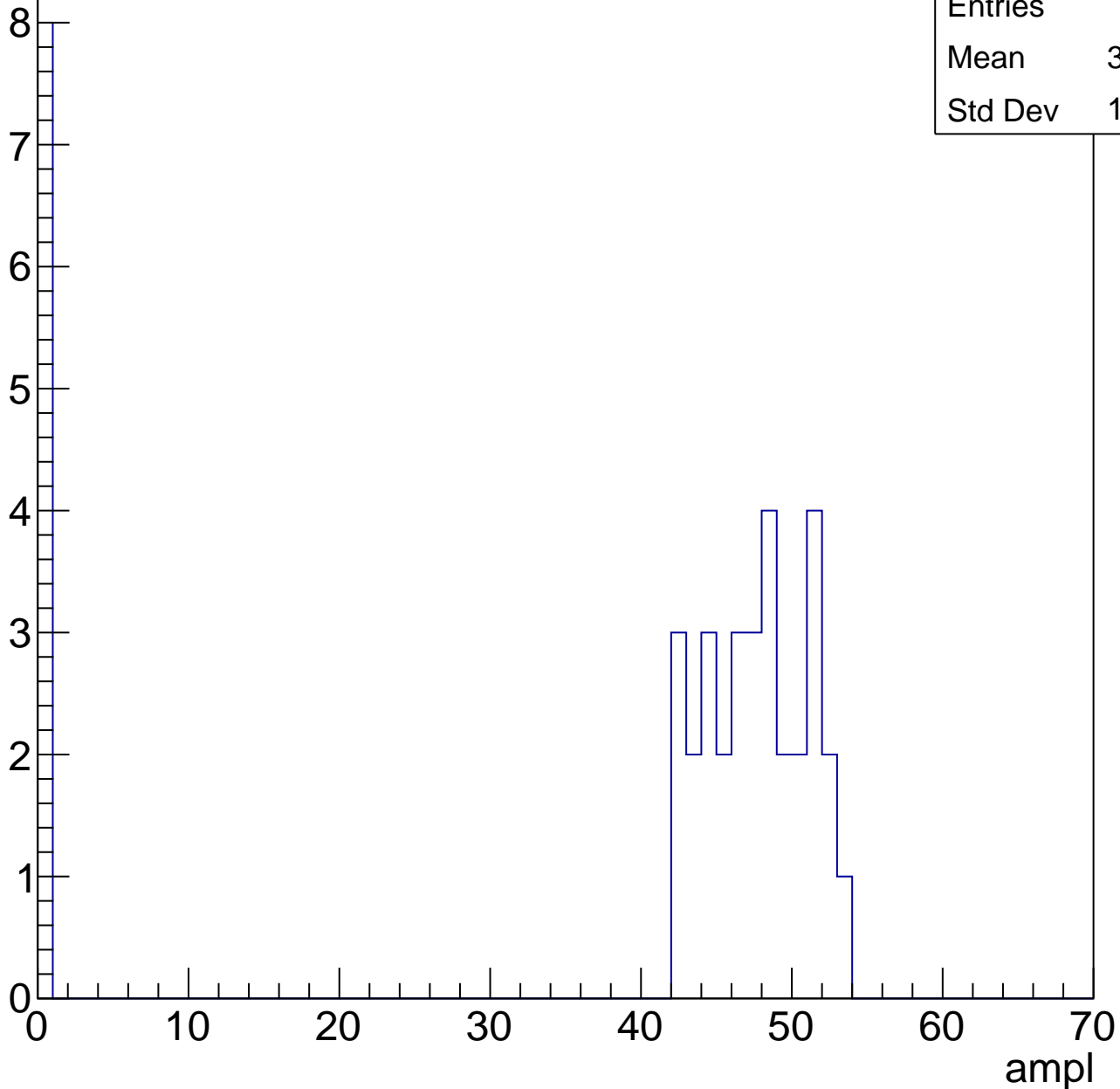


B1L103S, U14-ch102, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	37.54
Std Dev	19.29

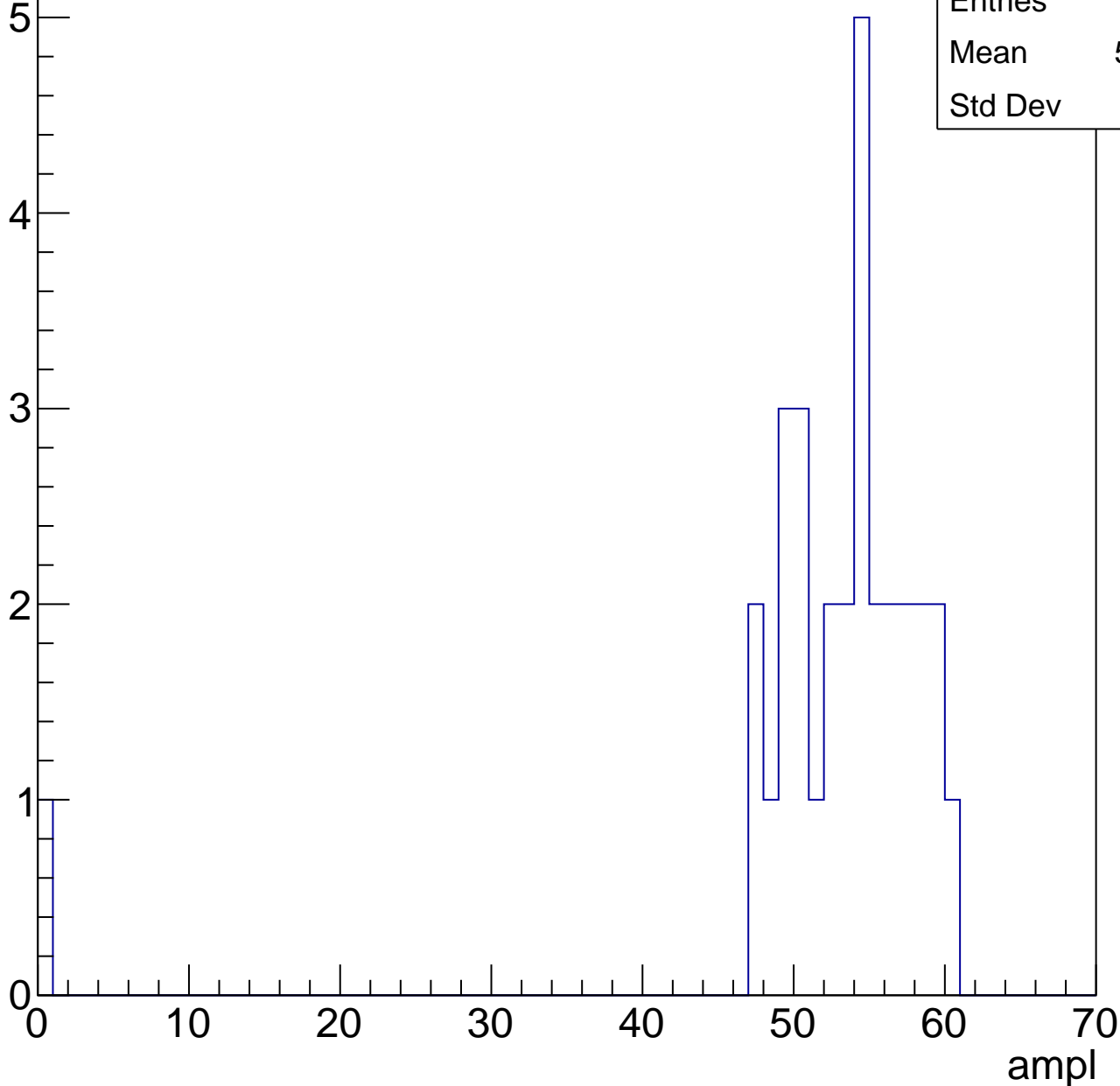


B1L103S, U14-ch102, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

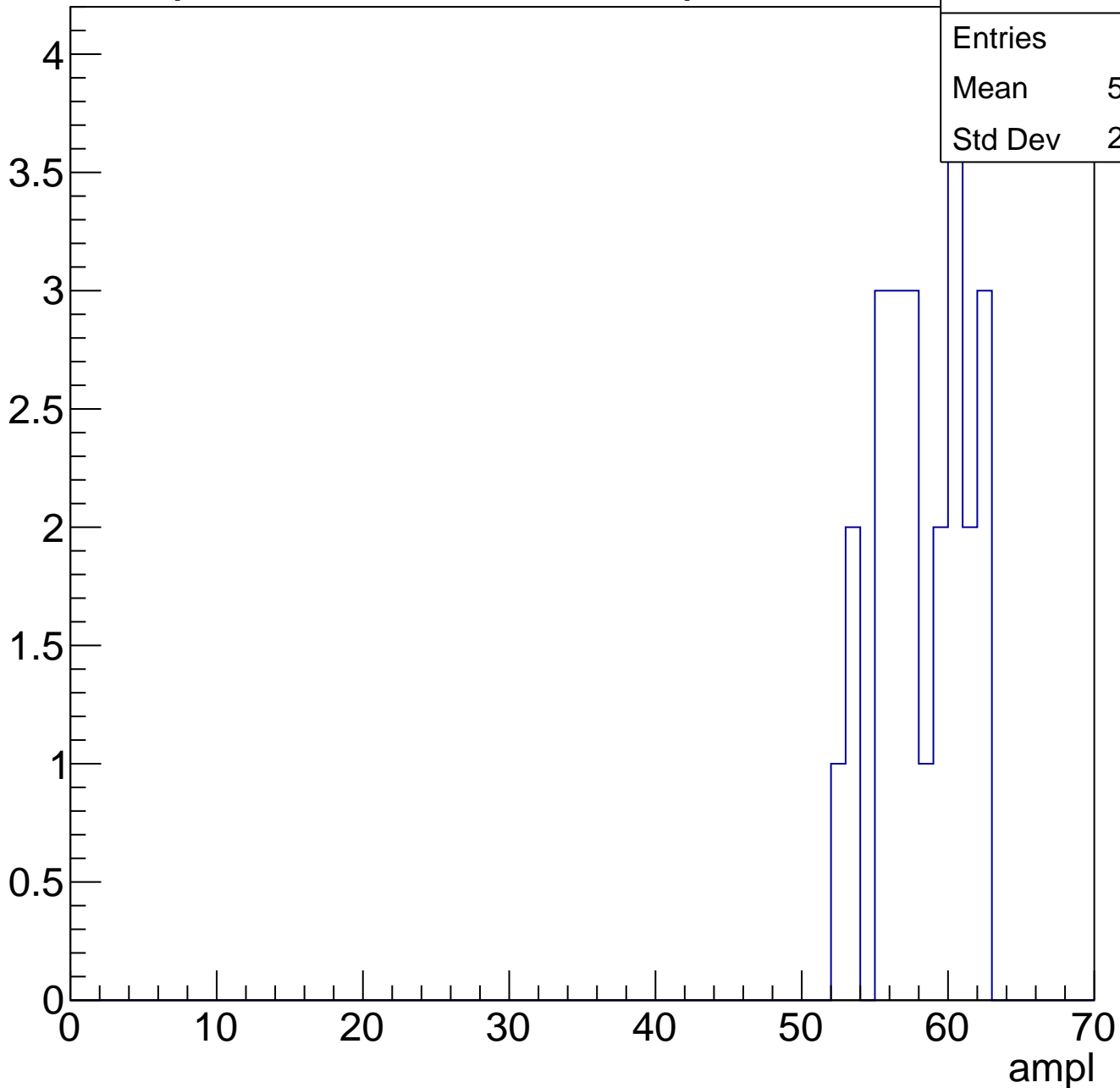
Entries	31
Mean	51.61
Std Dev	10.1



B1L103S, U14-ch102, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

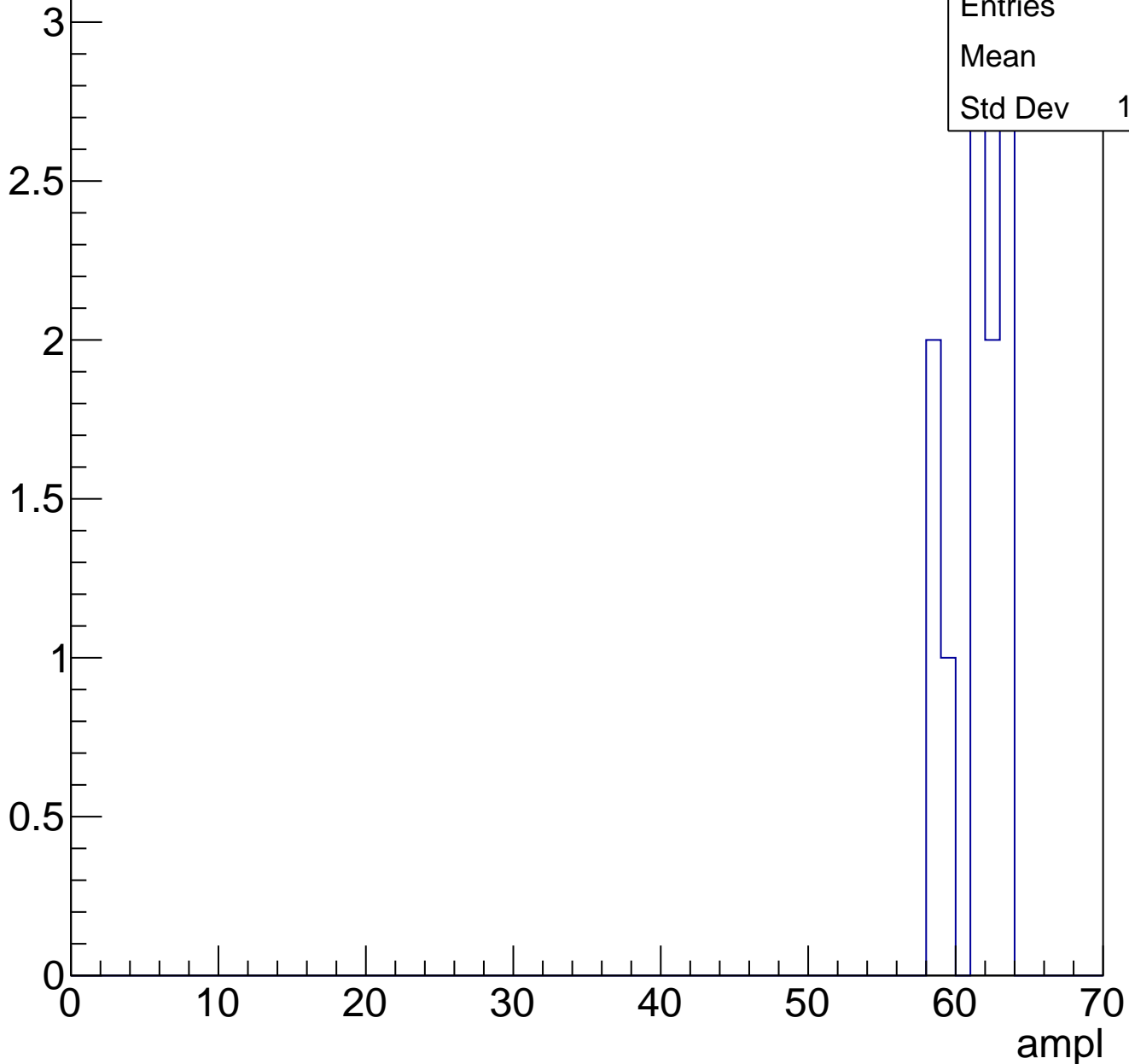


Entries	24
Mean	57.75
Std Dev	2.962

B1L103S, U14-ch102, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

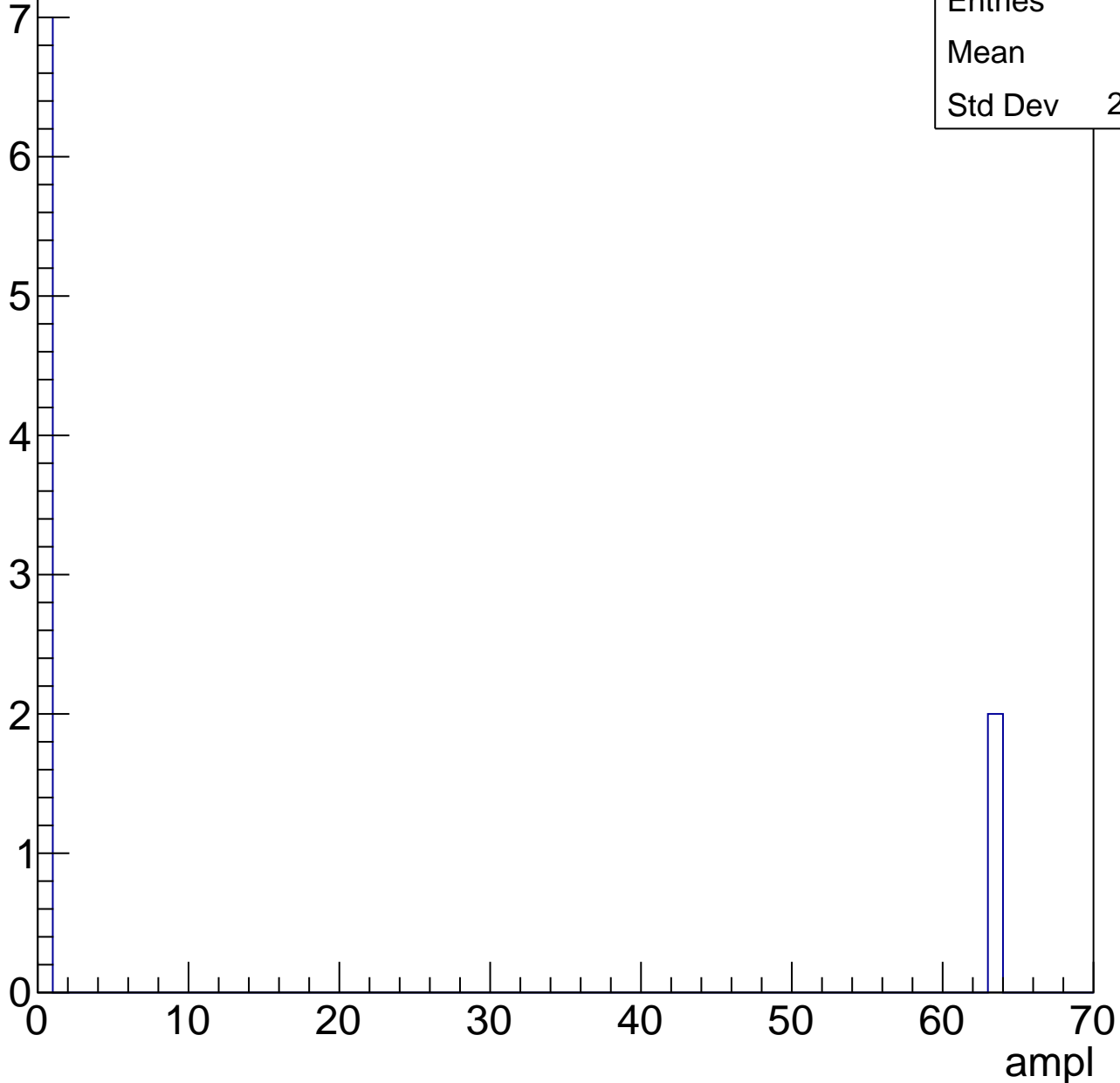


B1L103S, U14-ch102, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	9
Mean	14
Std Dev	26.19



B1L103S, U14-ch103, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	52
Mean	22.13
Std Dev	11.87

Entry

10

8

6

4

2

0

0

10

20

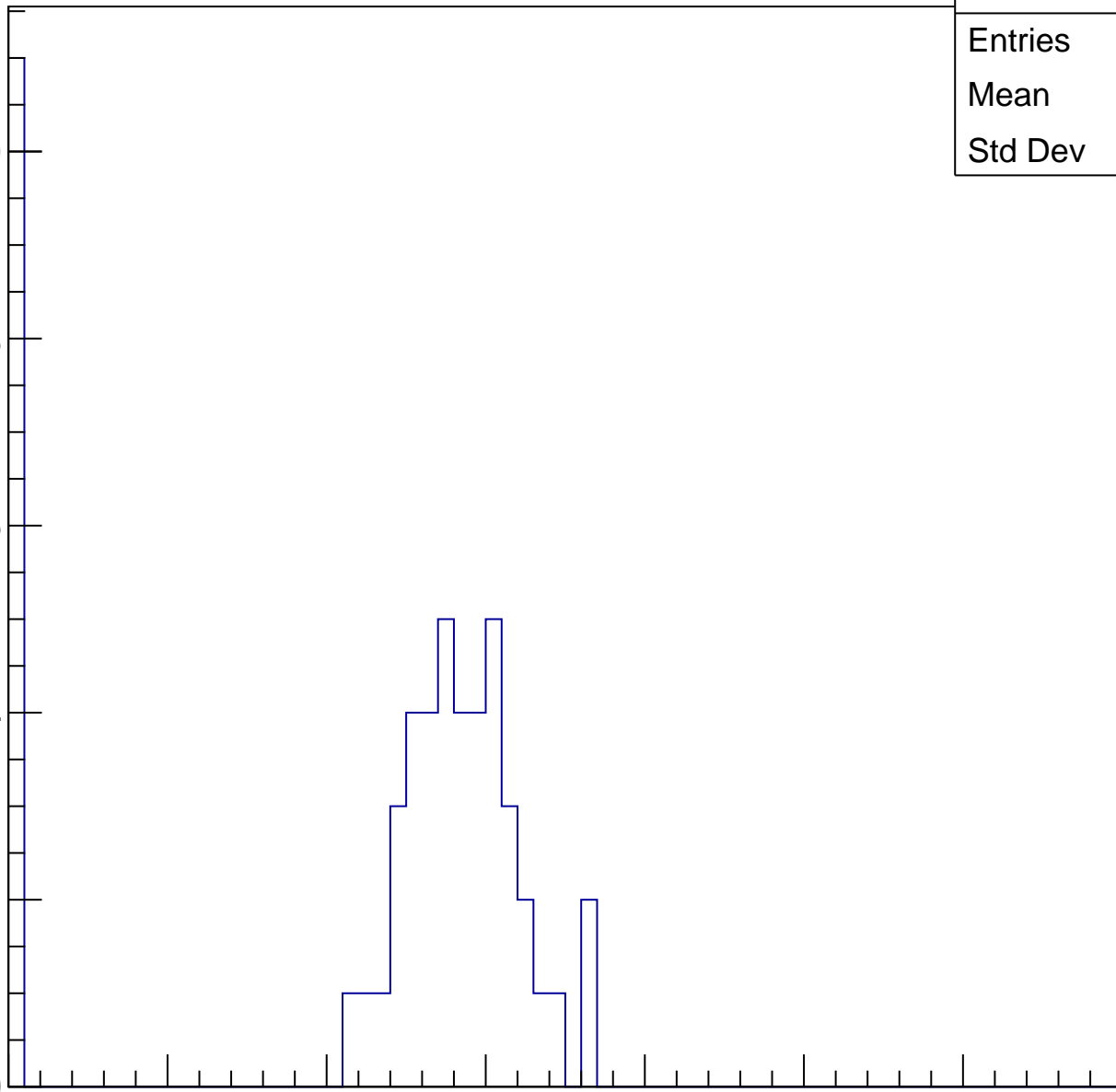
30

40

50

60

ampl

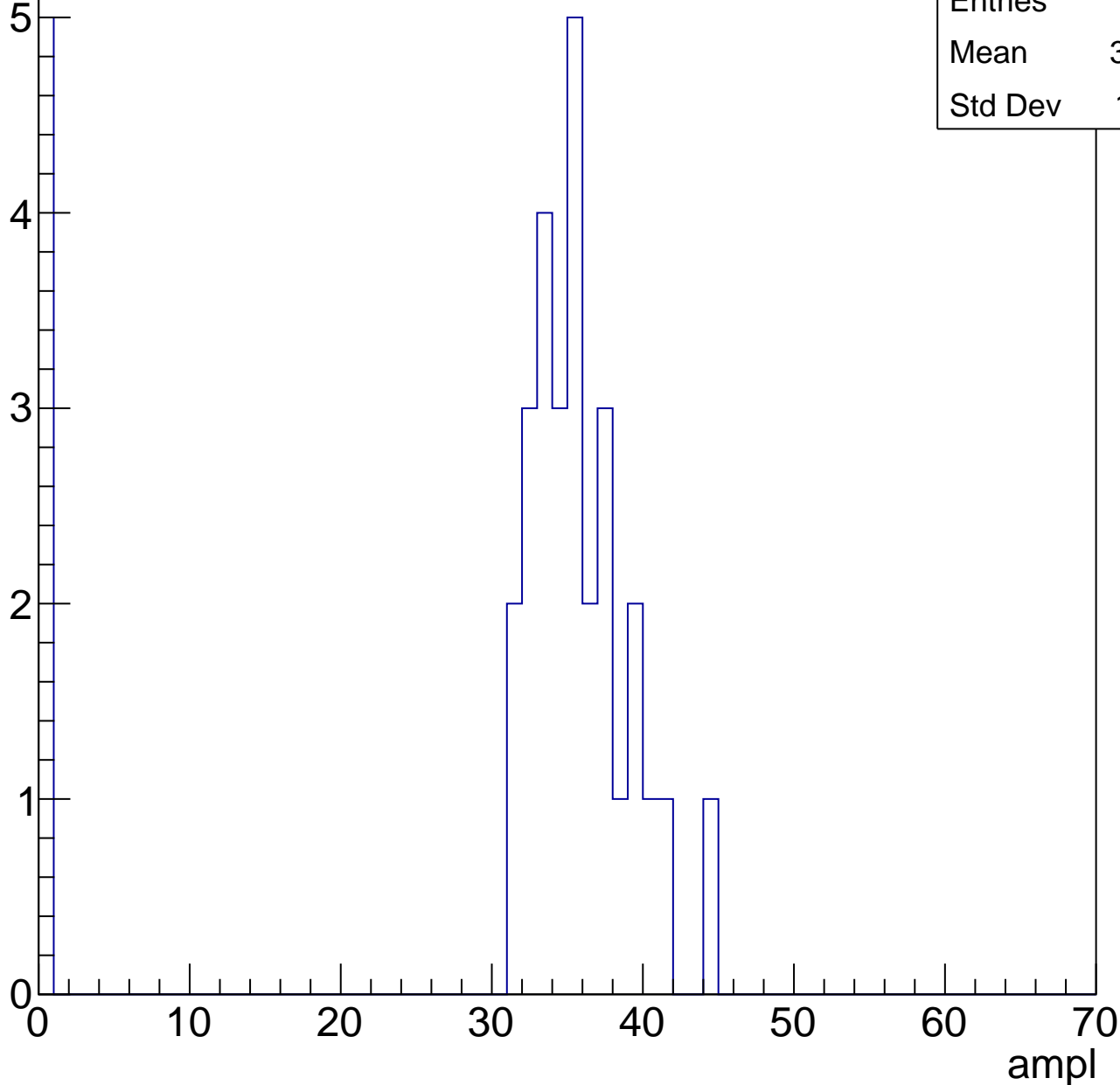


B1L103S, U14-ch103, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	33
Mean	30.03
Std Dev	13.01

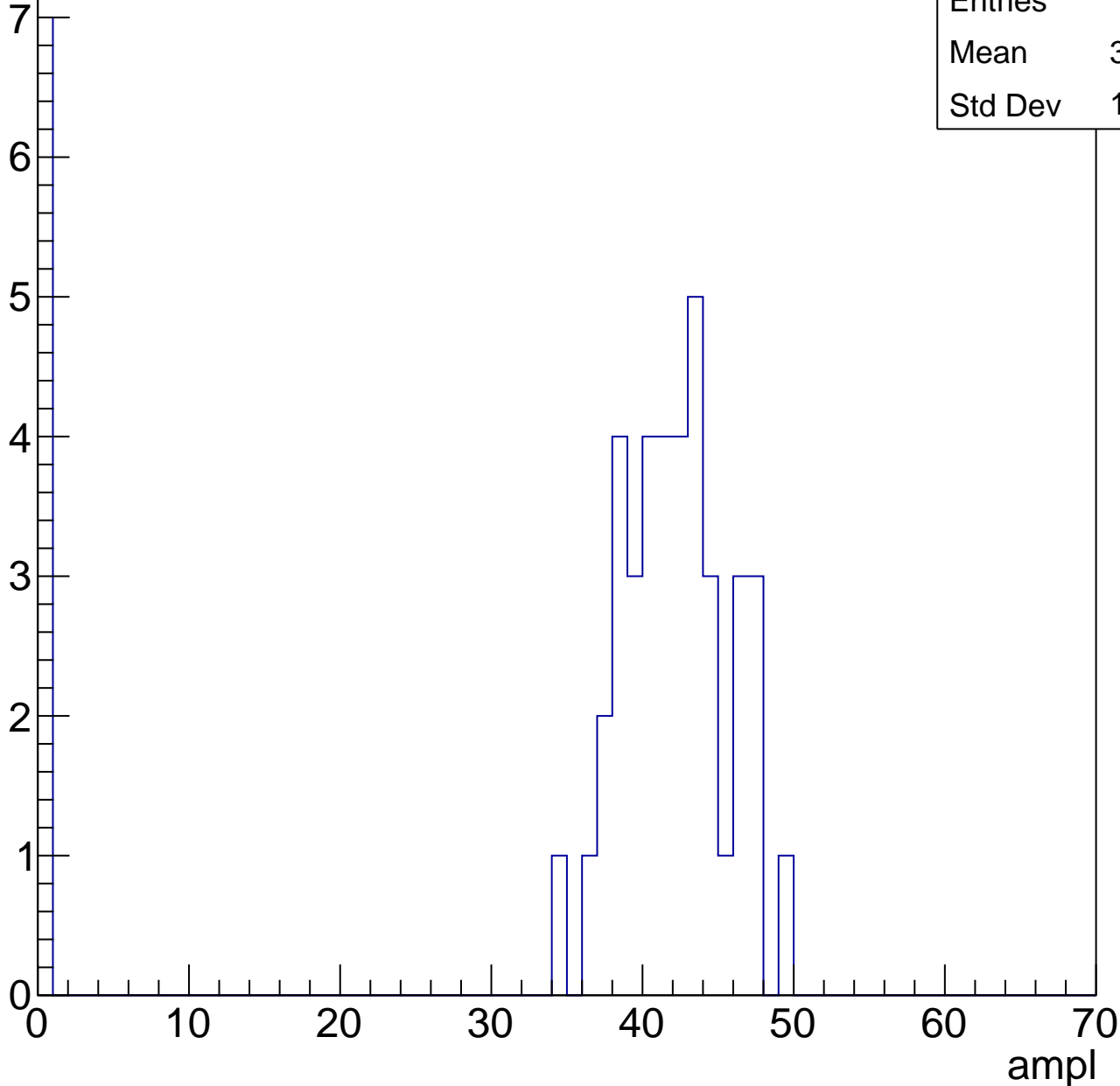


B1L103S, U14-ch103, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	46
Mean	35.33
Std Dev	15.29

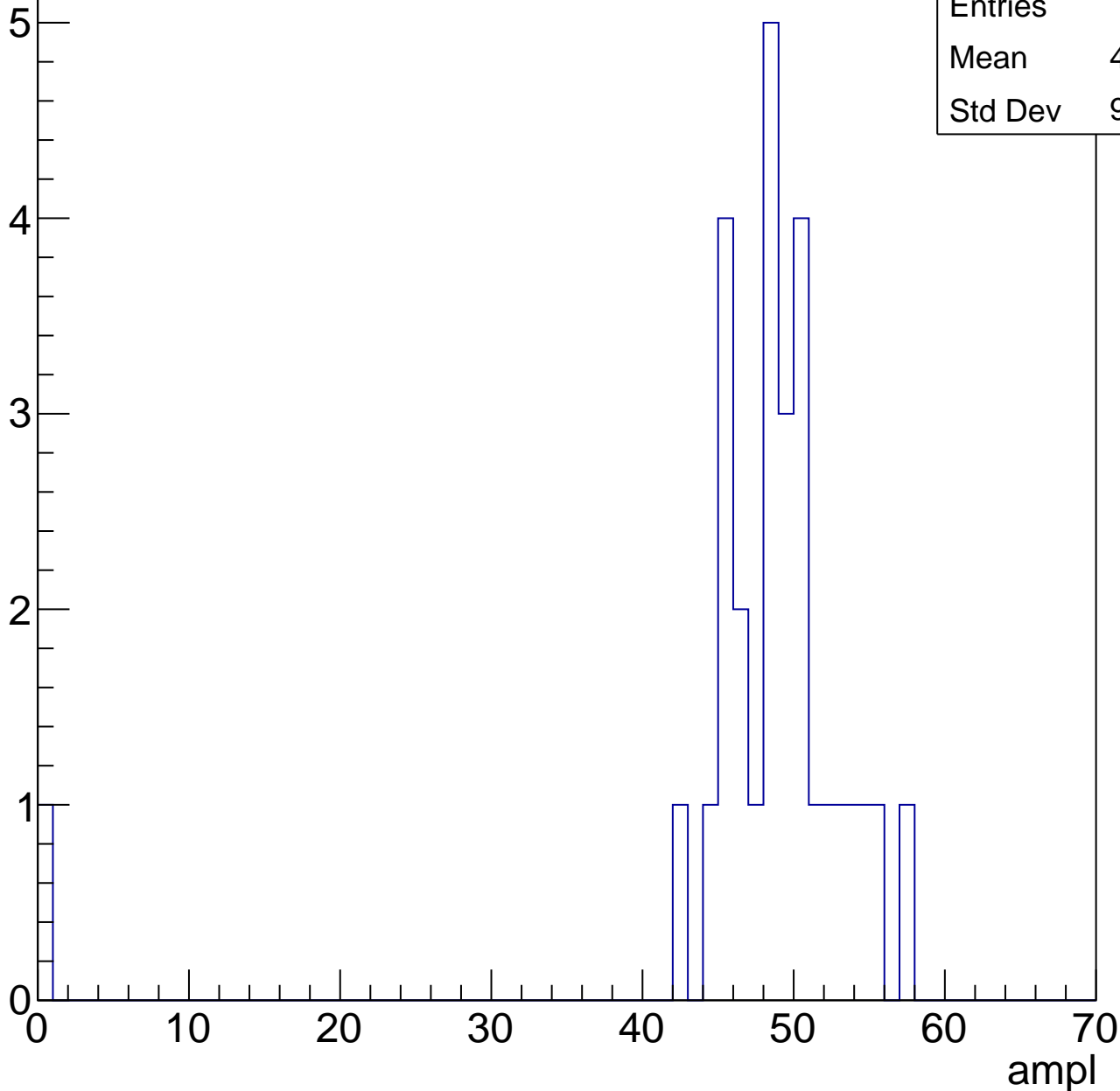


B1L103S, U14-ch103, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

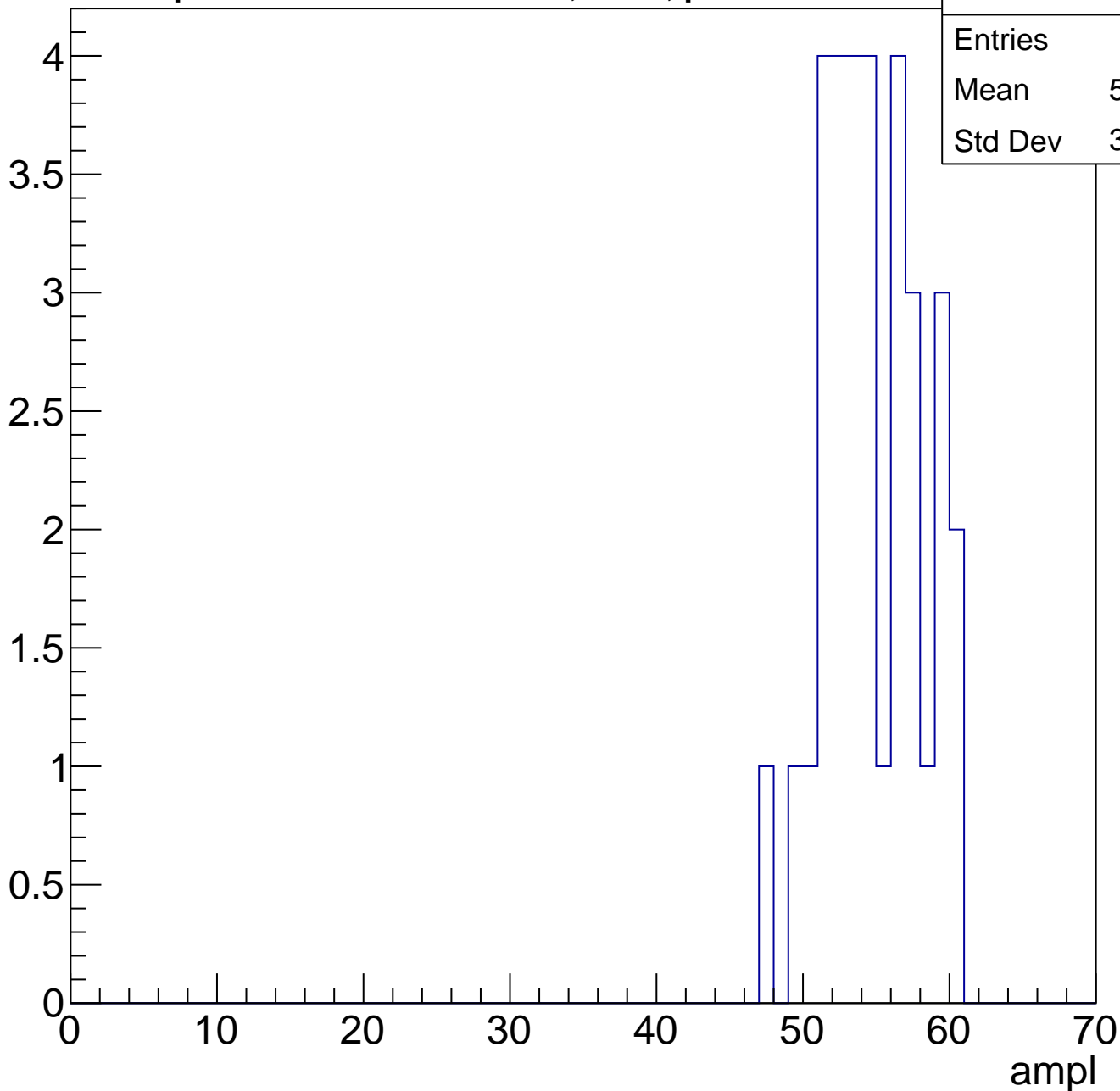
Entries	28
Mean	46.93
Std Dev	9.643



B1L103S, U14-ch103, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch103, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

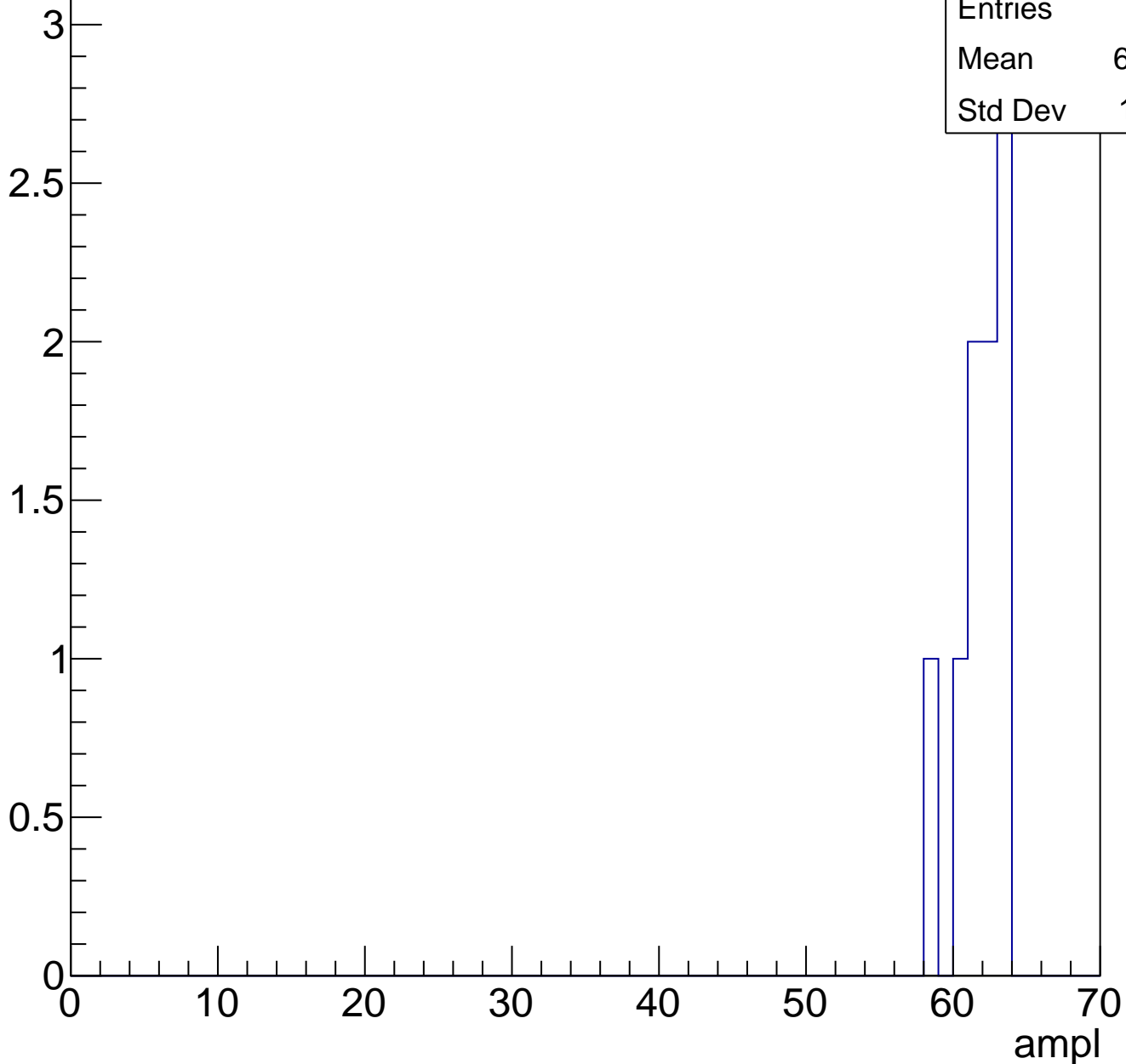
ampl

Entries	20
Mean	59.25
Std Dev	2.605

B1L103S, U14-ch103, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

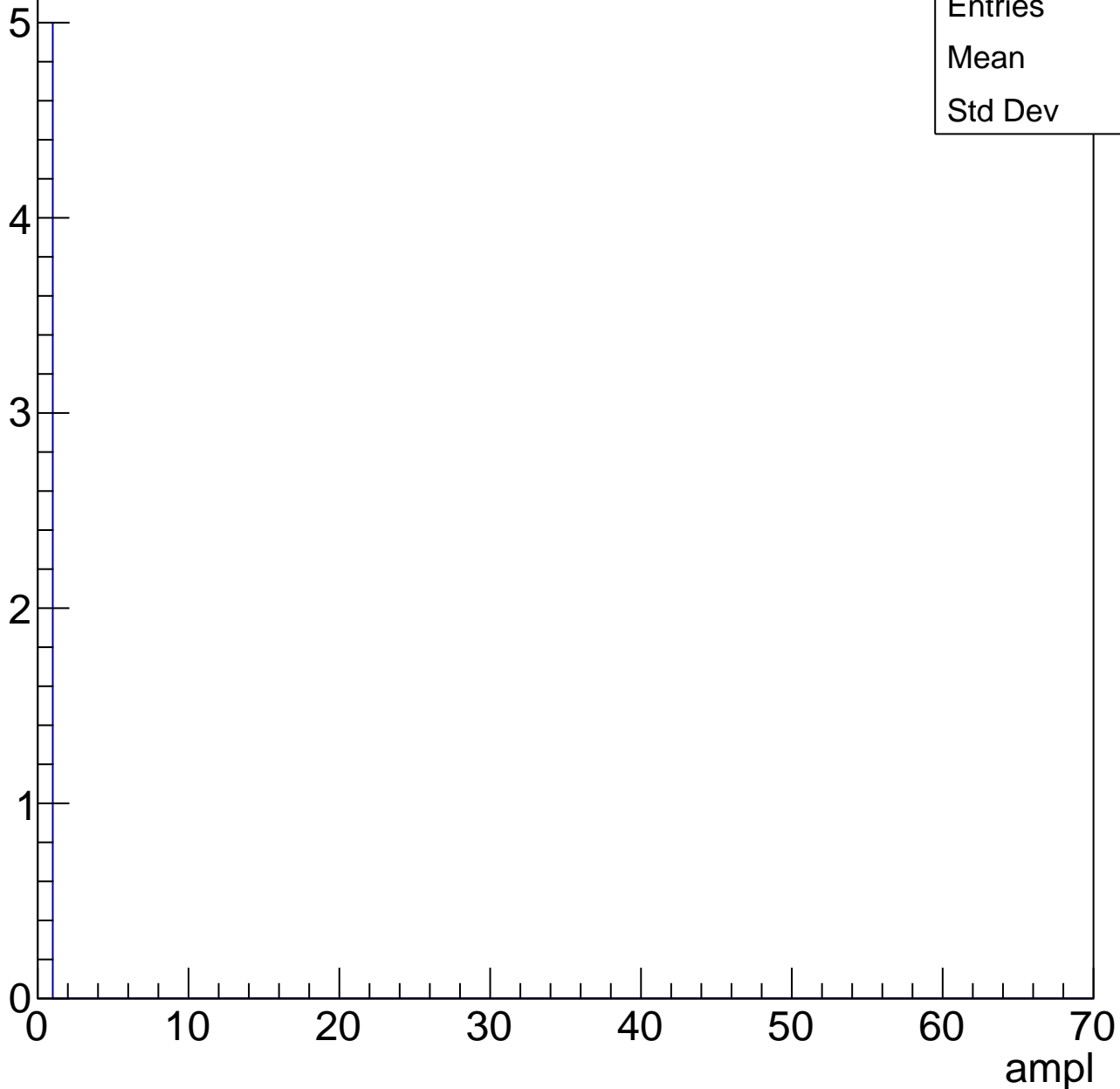


B1L103S, U14-ch103, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

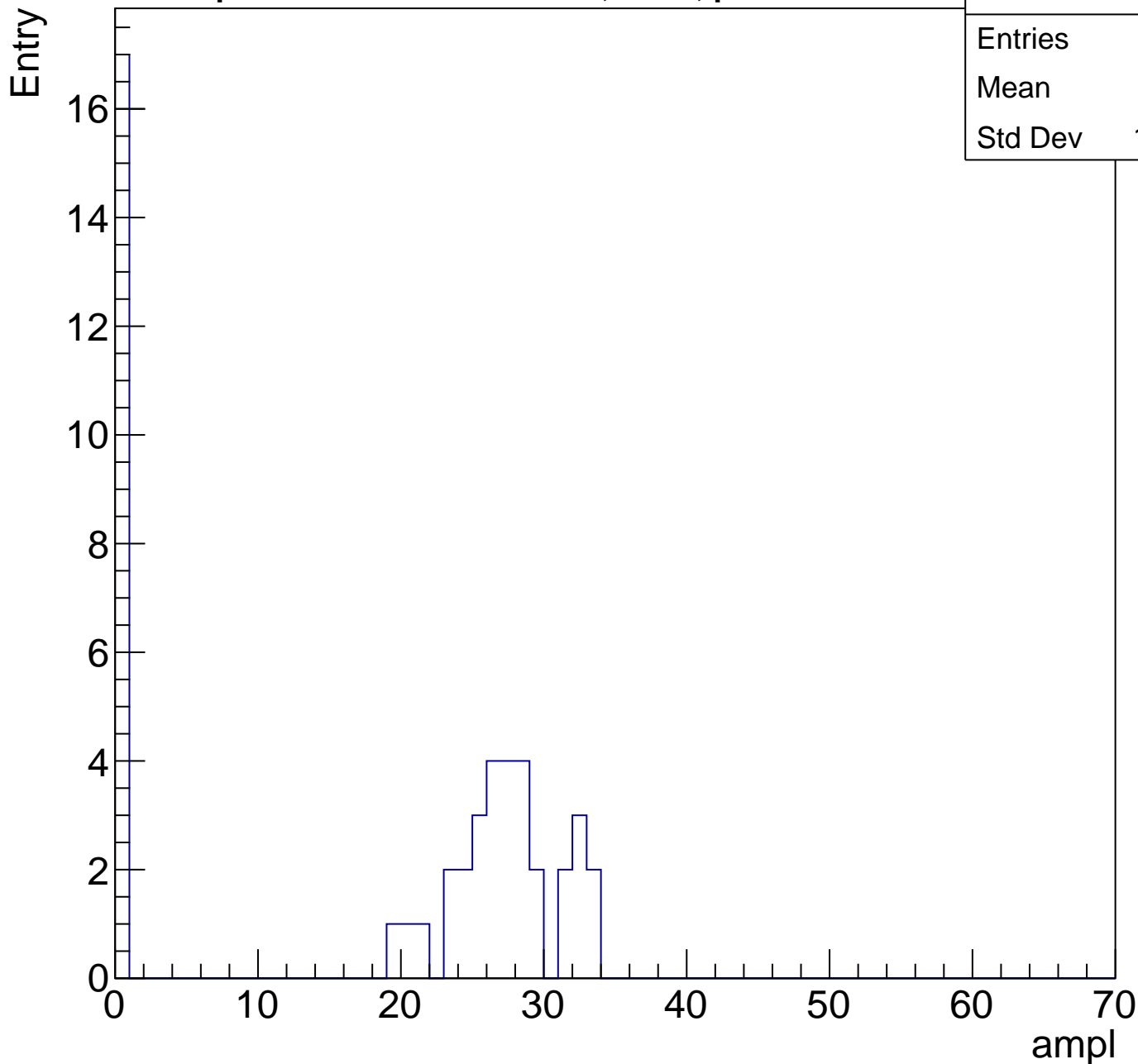
Entries	5
Mean	0
Std Dev	0



B1L103S, U14-ch104, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	48
Mean	17.4
Std Dev	13.21

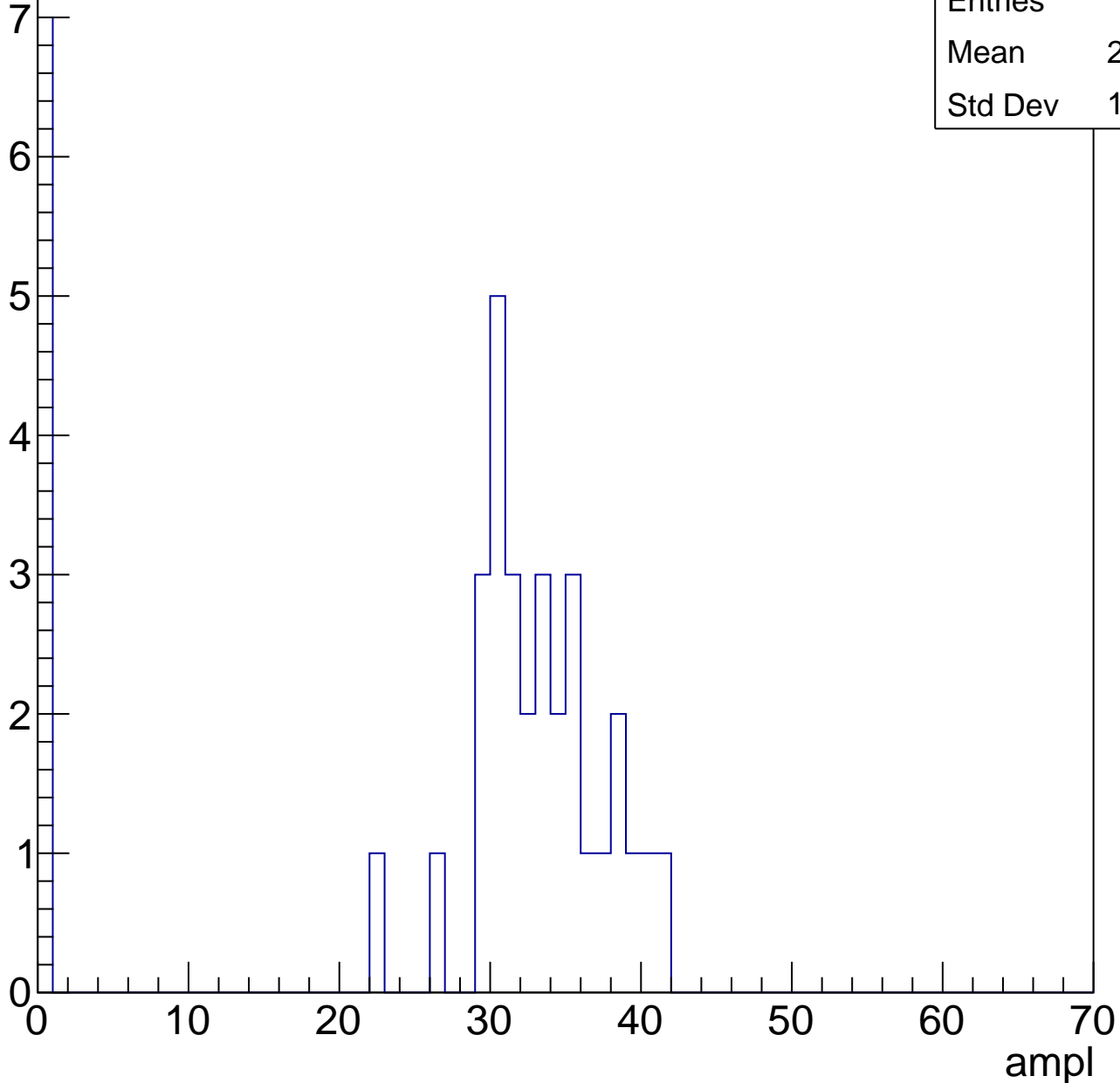


B1L103S, U14-ch104, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	37
Mean	26.57
Std Dev	13.36

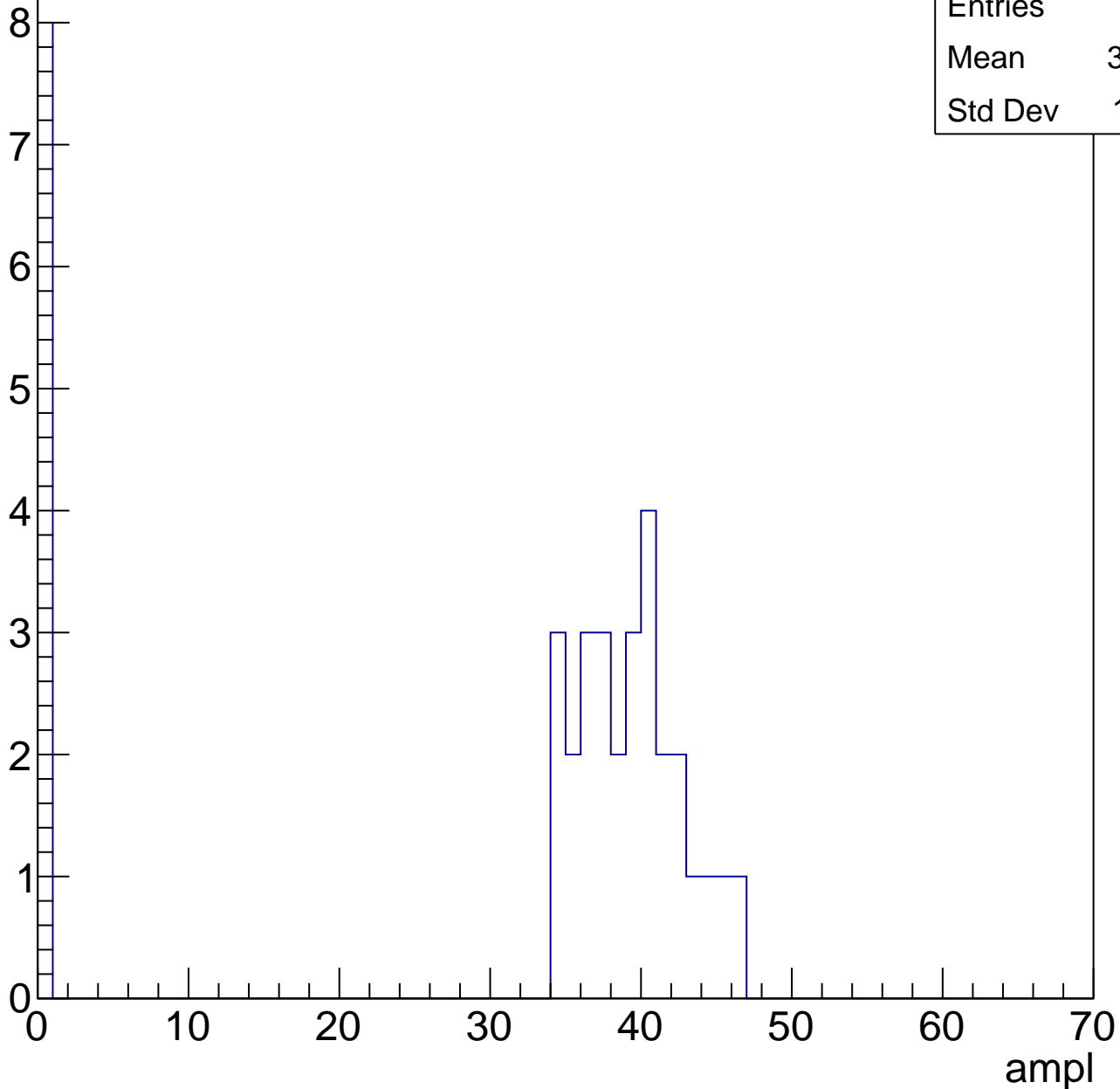


B1L103S, U14-ch104, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

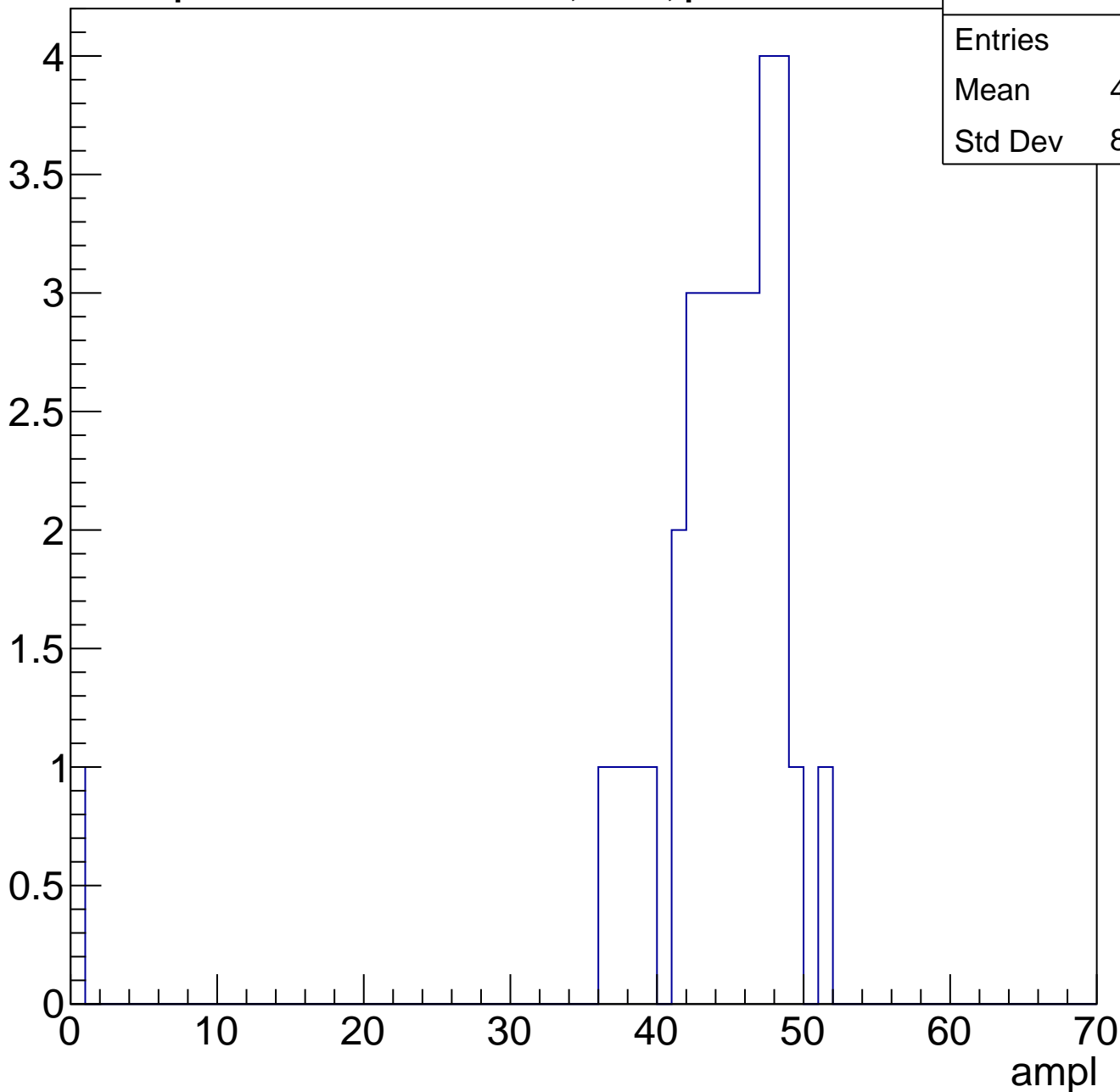
Entries	36
Mean	30.22
Std Dev	16.41



B1L103S, U14-ch104, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry



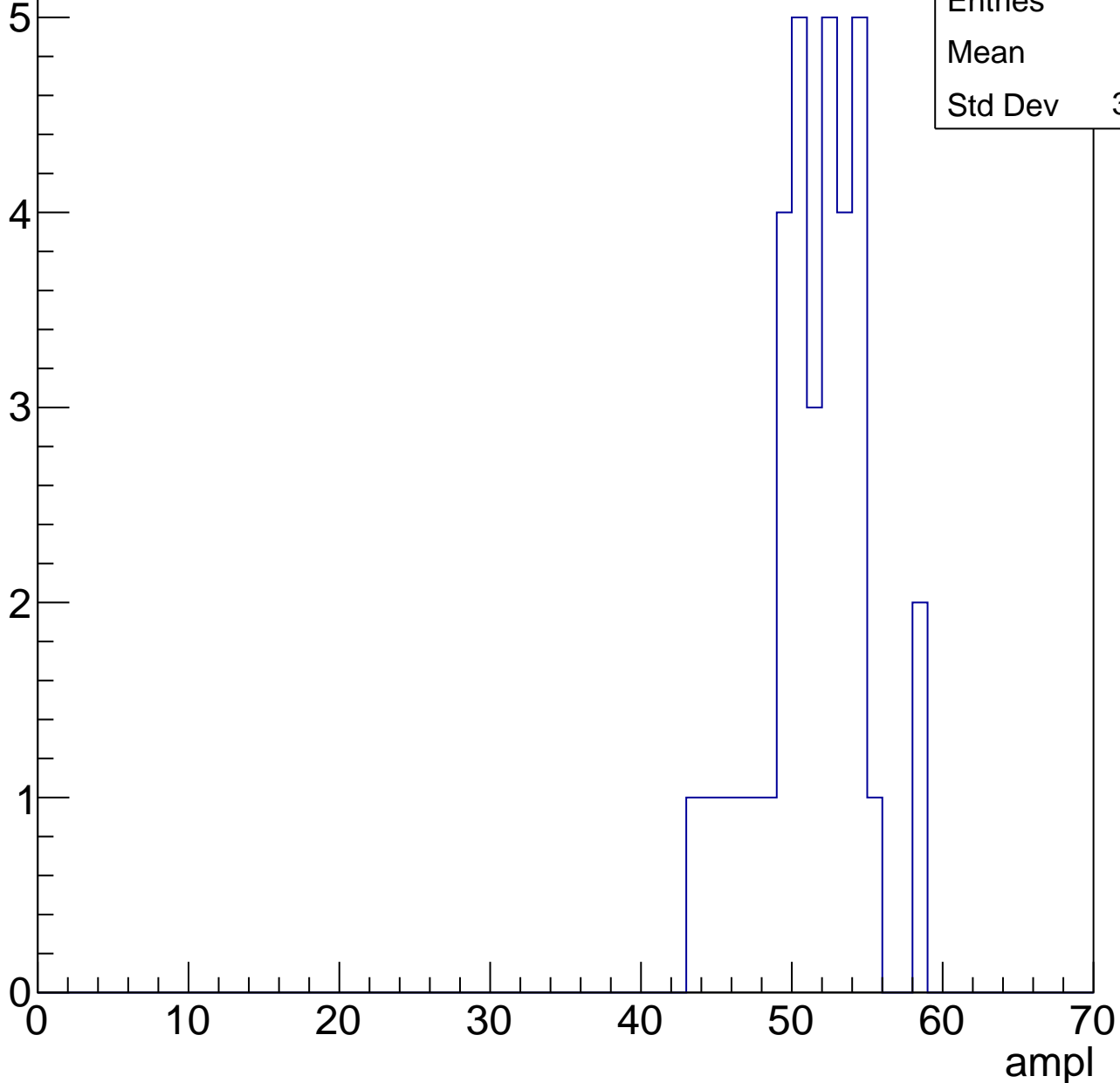
Entries	32
Mean	42.88
Std Dev	8.462

B1L103S, U14-ch104, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

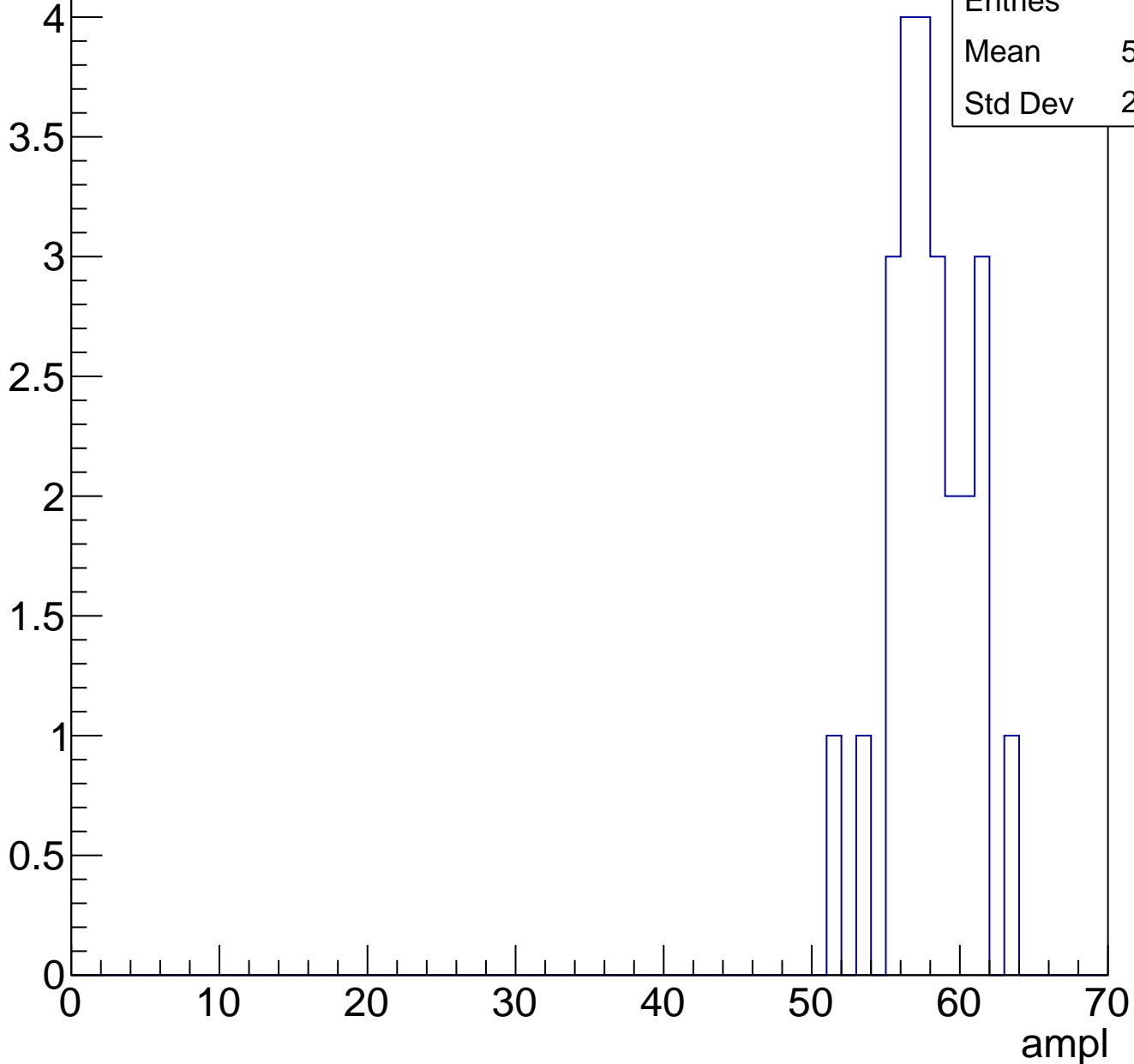
Entries	35
Mean	51
Std Dev	3.381



B1L103S, U14-ch104, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

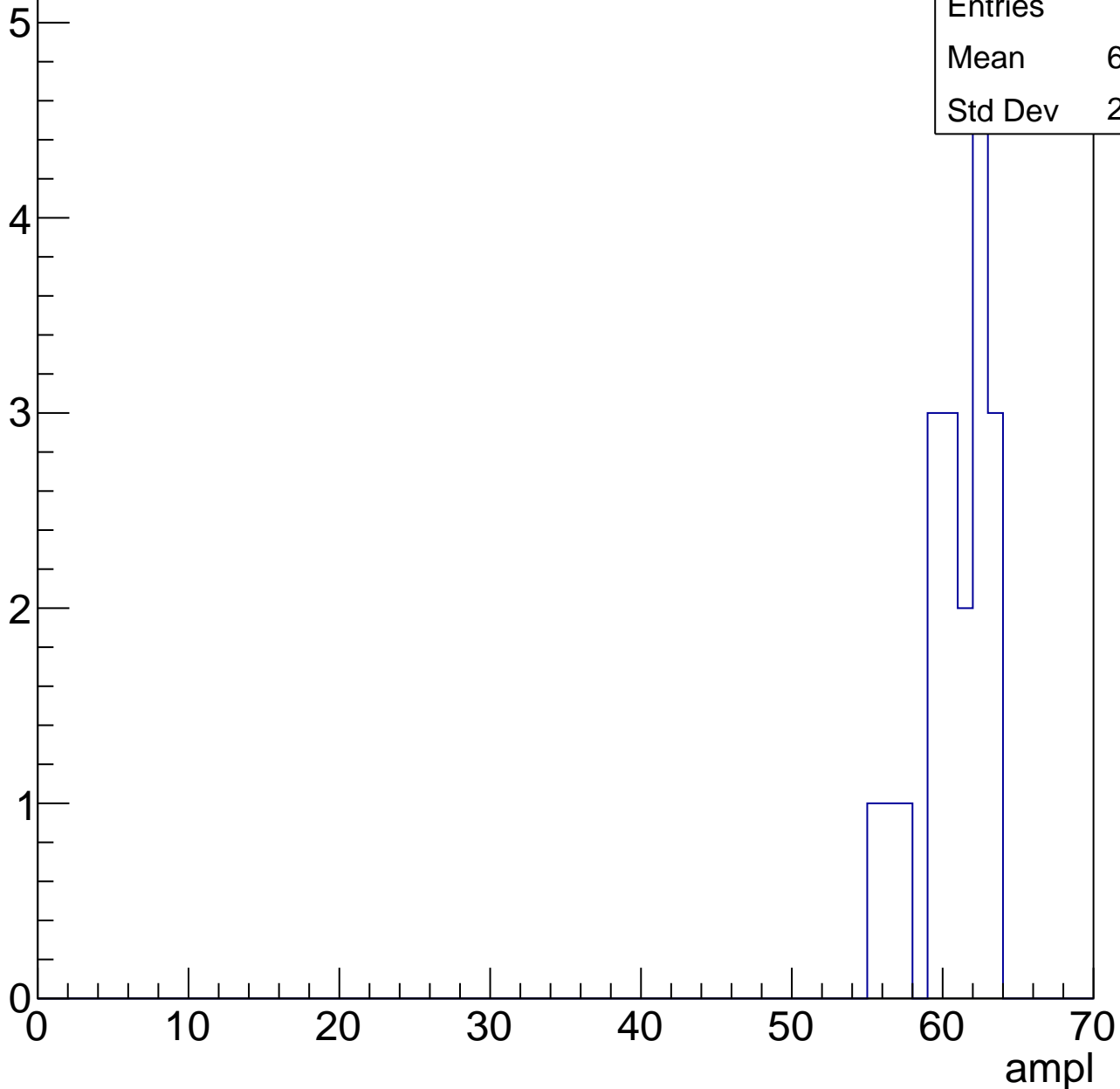


B1L103S, U14-ch104, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

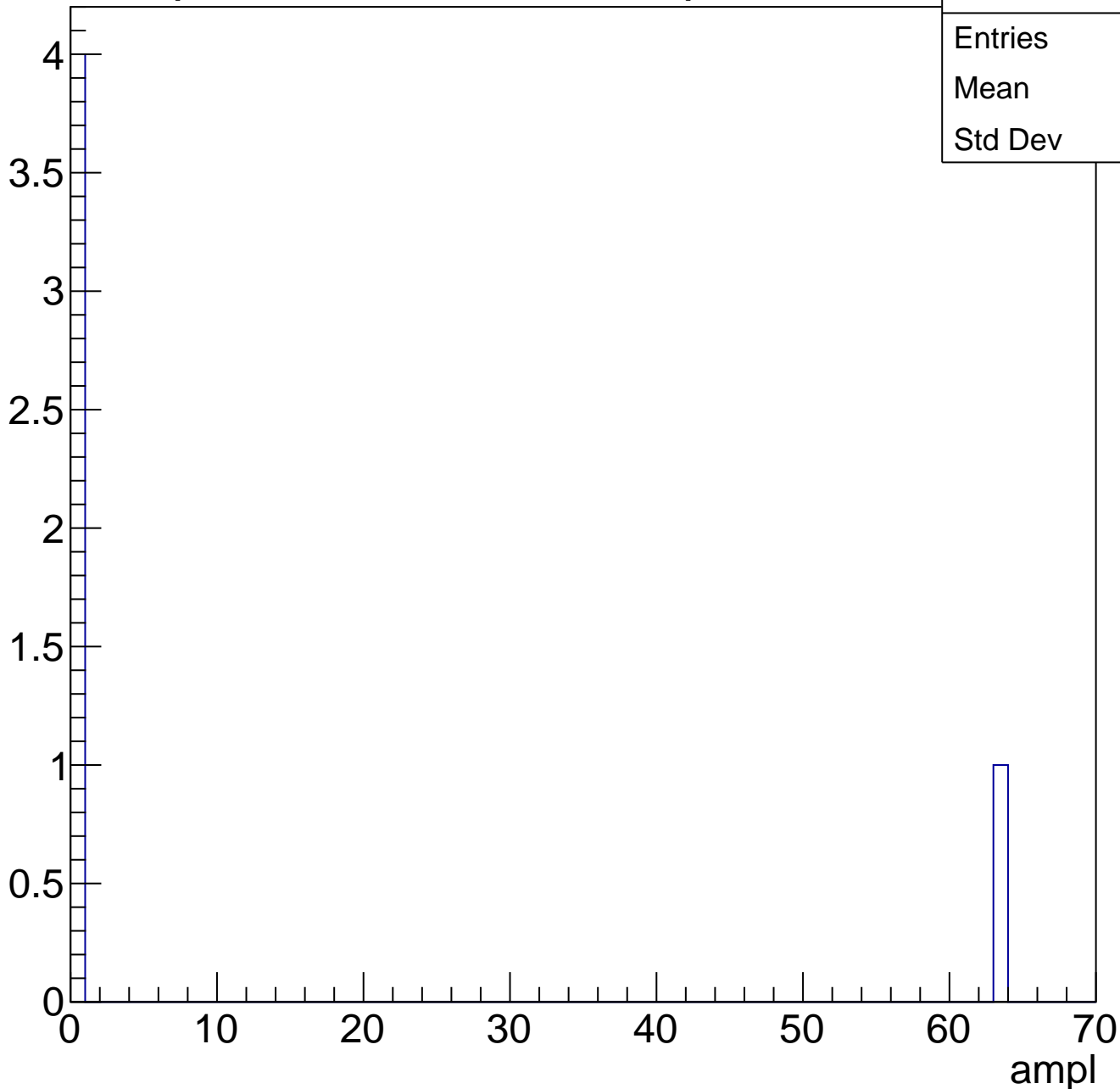
Entries	19
Mean	60.32
Std Dev	2.295



B1L103S, U14-ch104, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

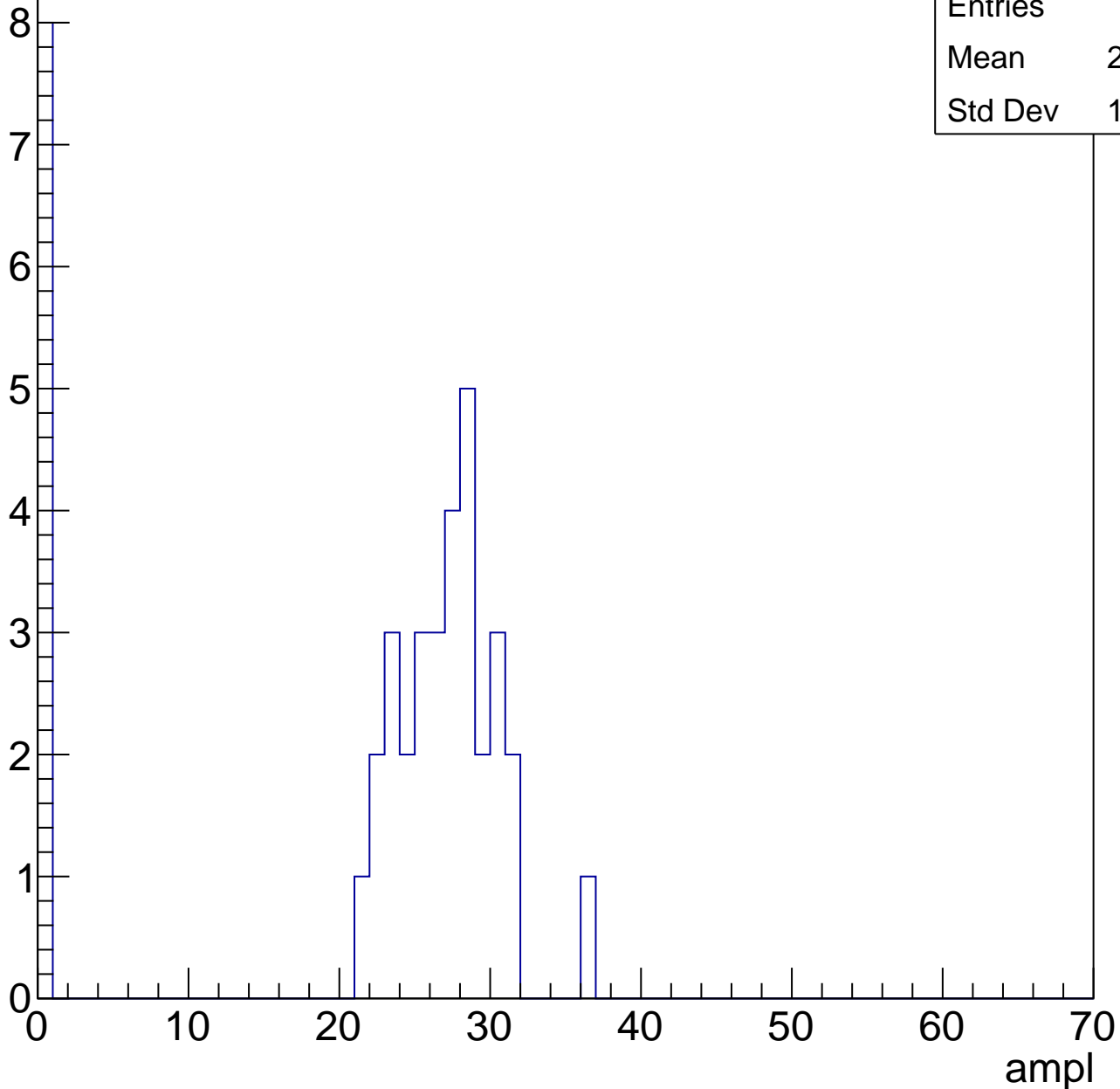


B1L103S, U14-ch105, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	21.26
Std Dev	11.17

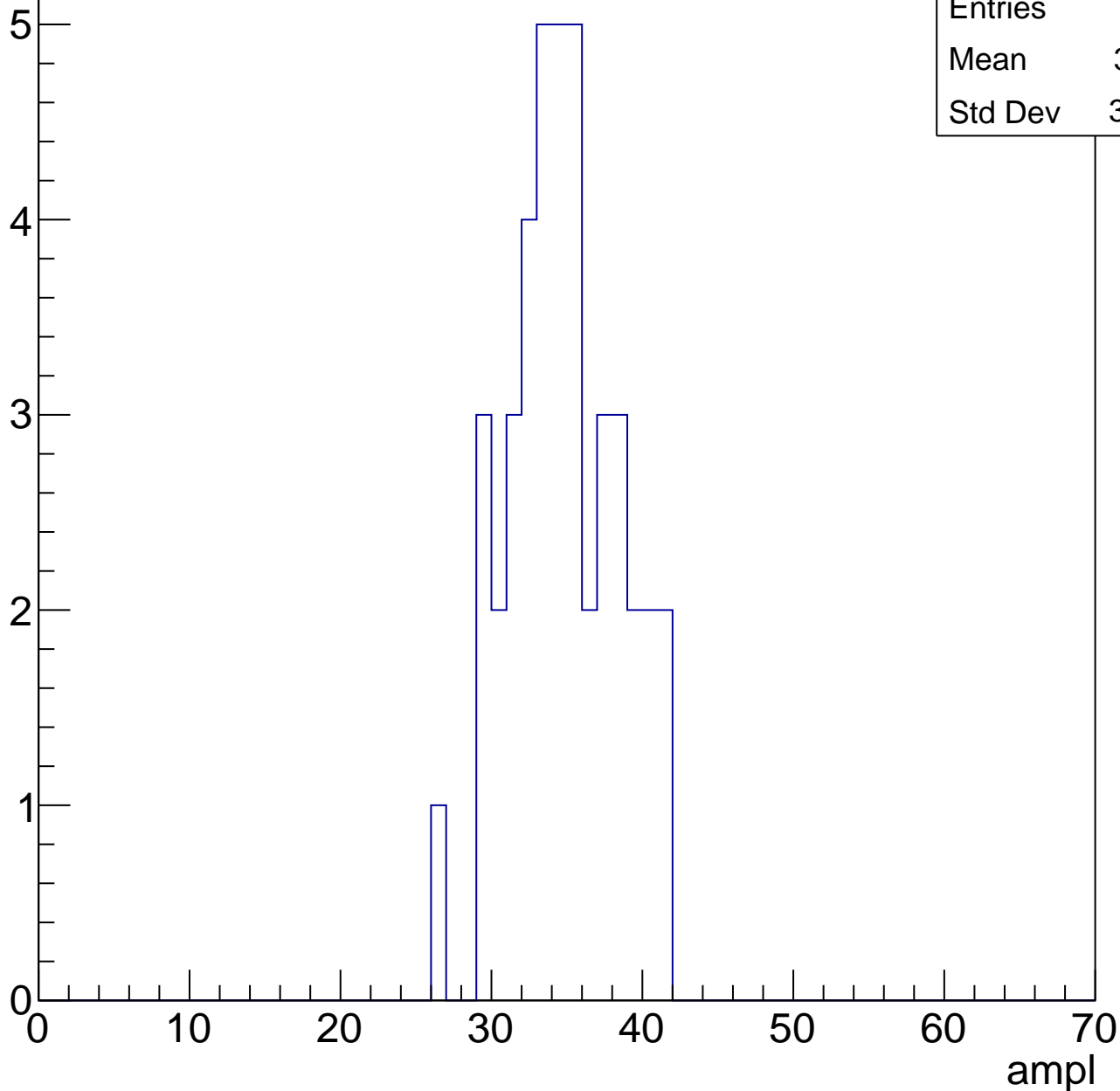


B1L103S, U14-ch105, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

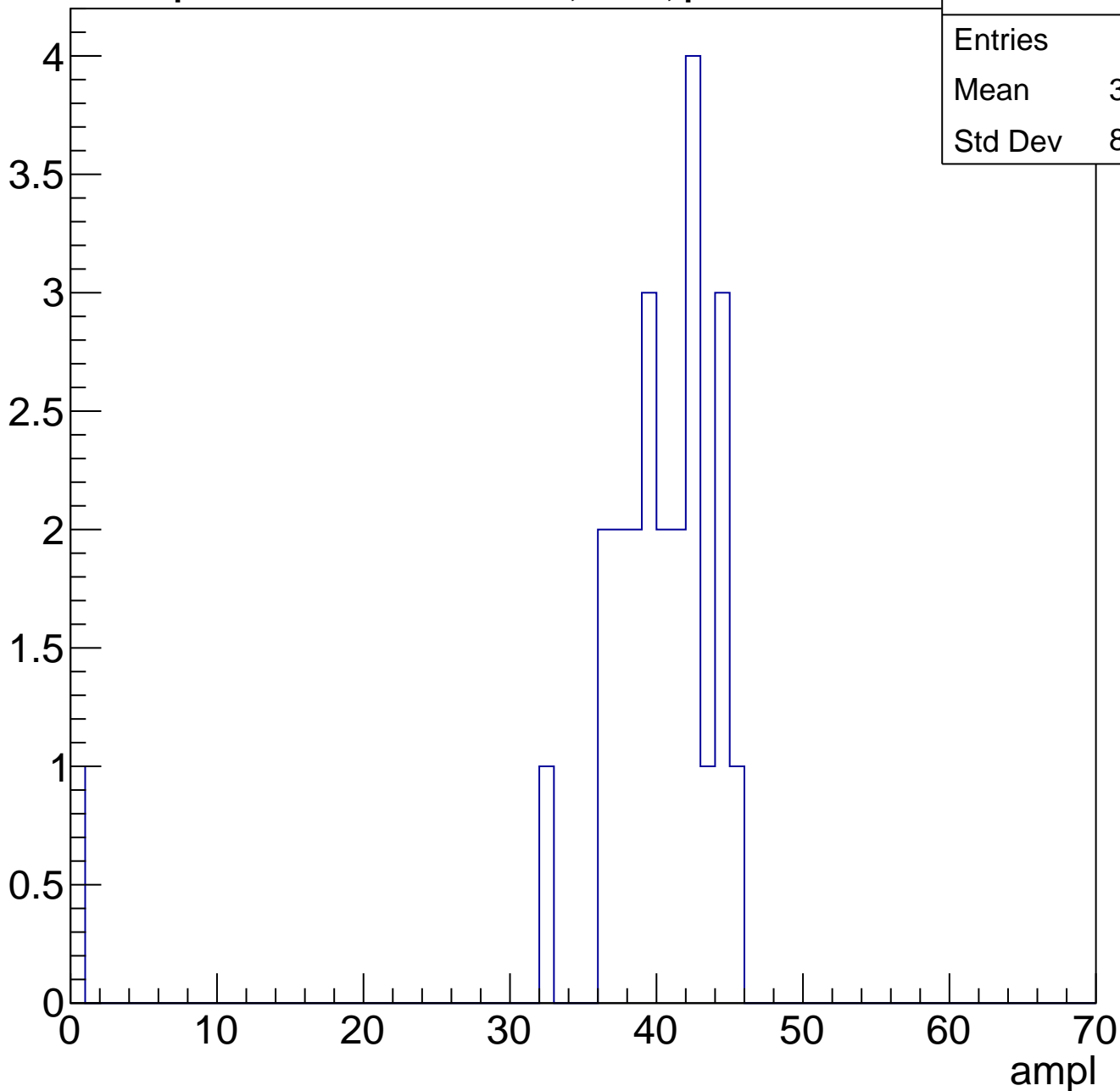
Entries	42
Mean	34.31
Std Dev	3.529



B1L103S, U14-ch105, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

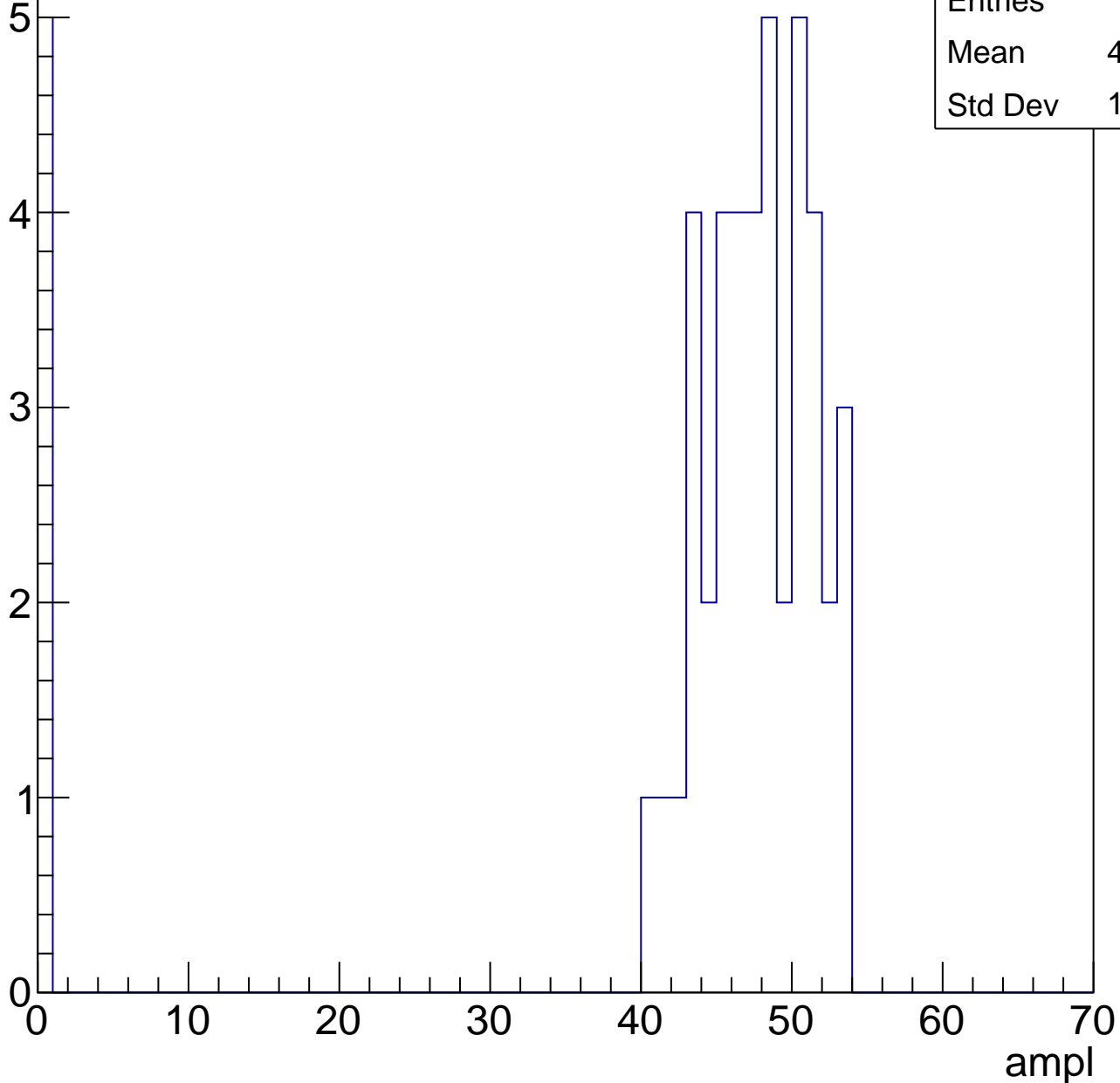


B1L103S, U14-ch105, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	47
Mean	42.34
Std Dev	14.96



B1L103S, U14-ch105, adc4

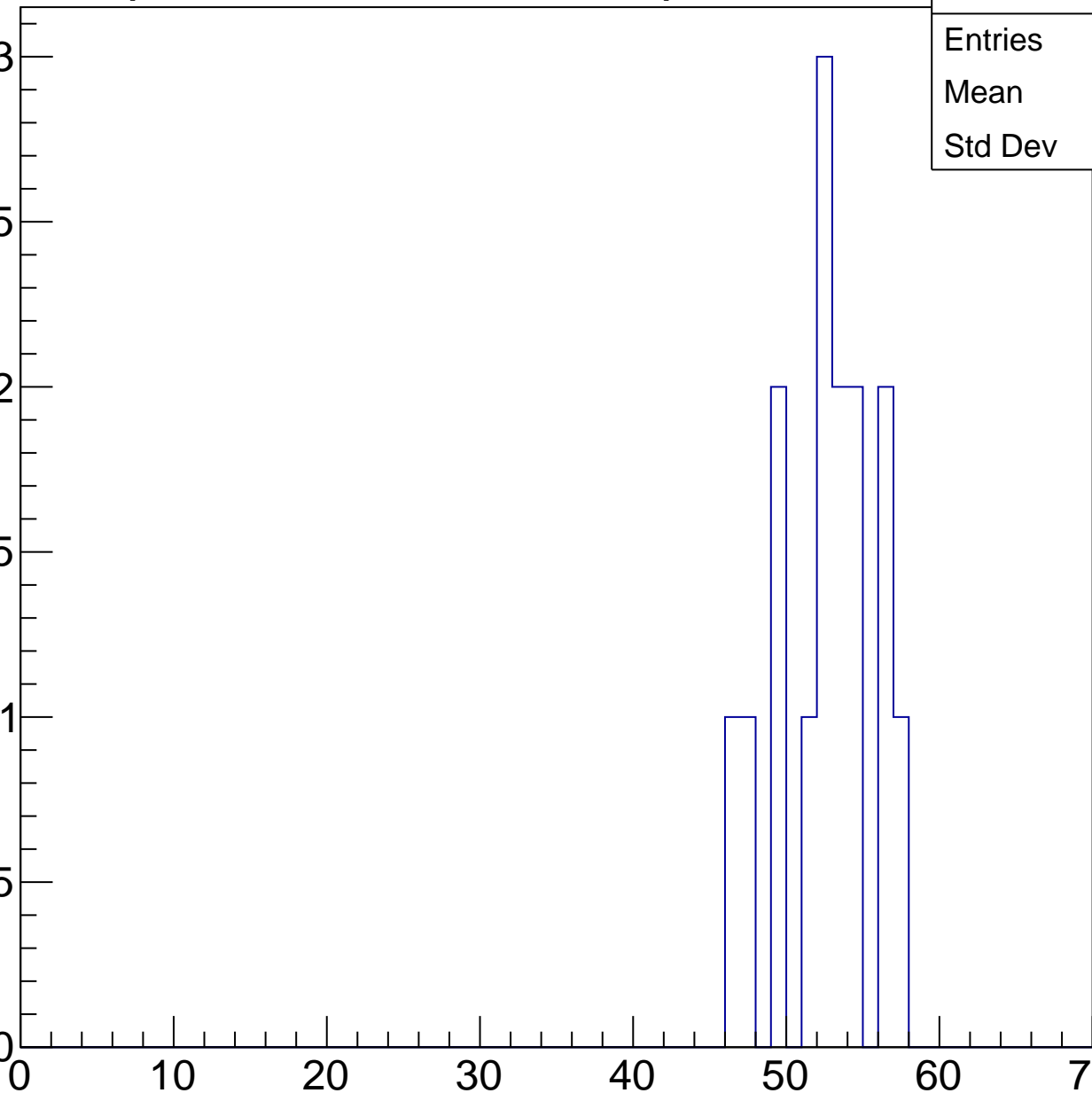
calib_packv5_041523_1651.root, FC#0, port C2

Entry

3
2.5
2
1.5
1
0.5
0

Entries	15
Mean	52.07
Std Dev	3.13

ampl

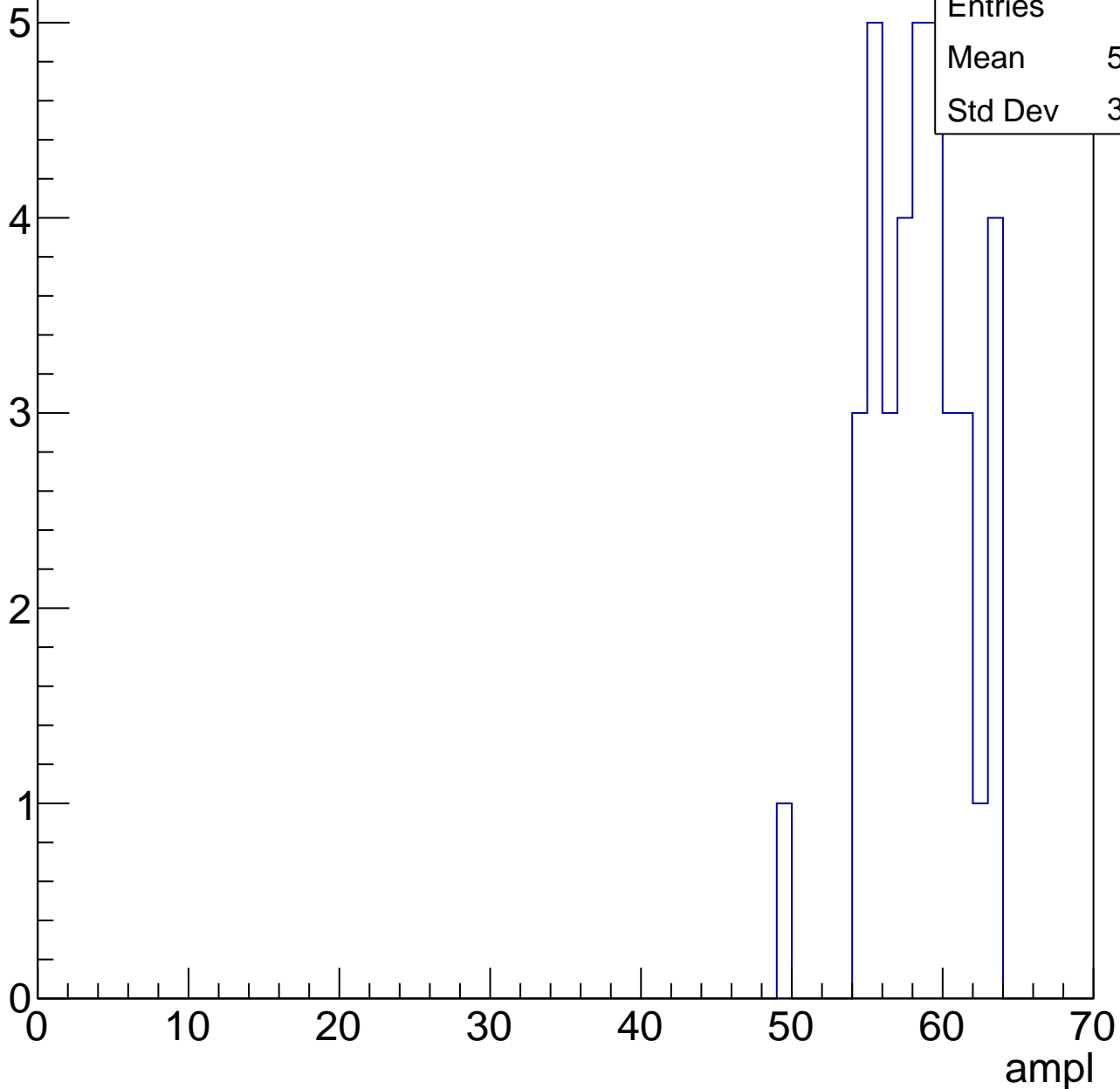


B1L103S, U14-ch105, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

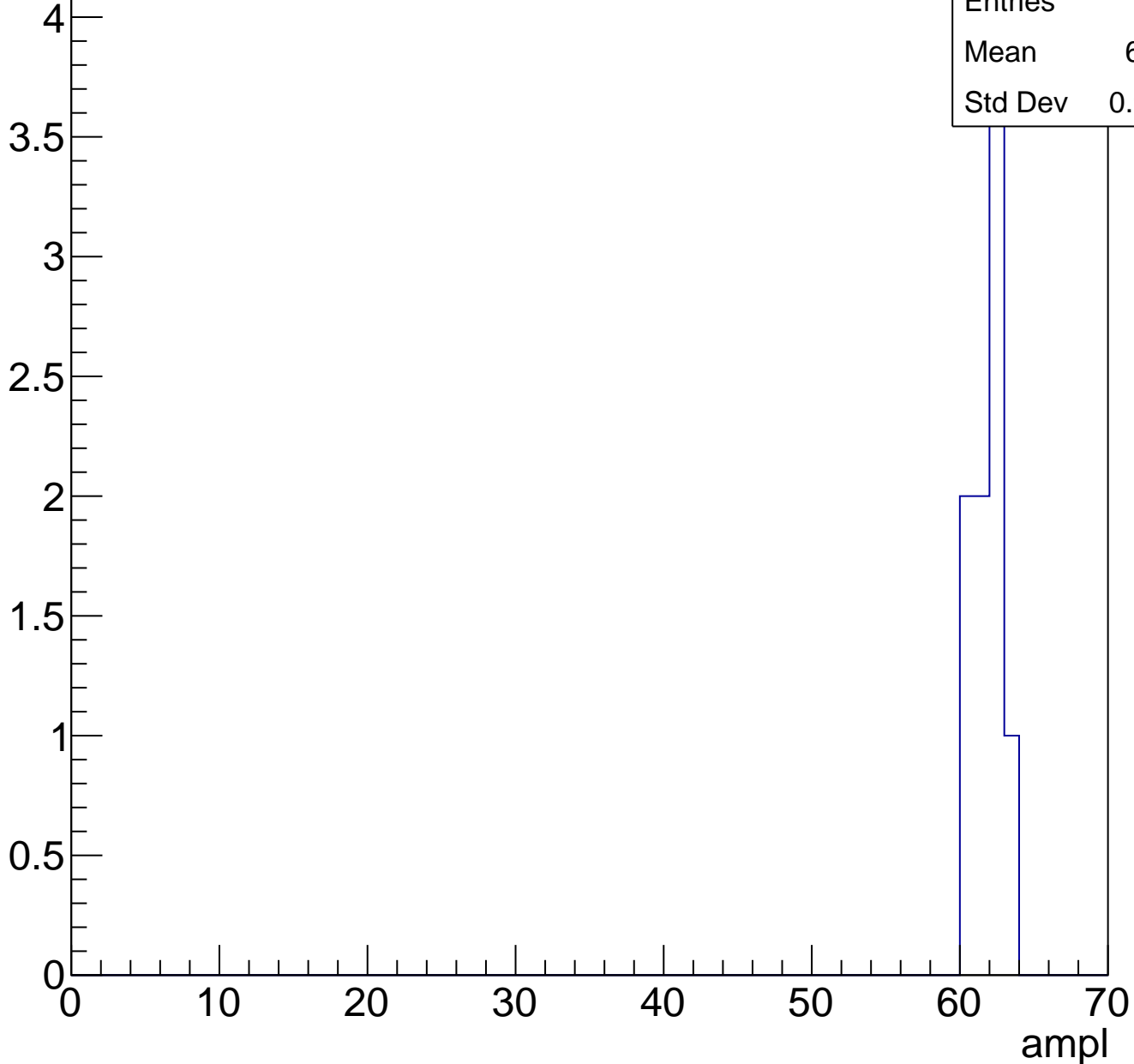
Entries	37
Mean	57.95
Std Dev	3.075



B1L103S, U14-ch105, adc6

calib_packv5_041523_1651.root, FC#0, port C2

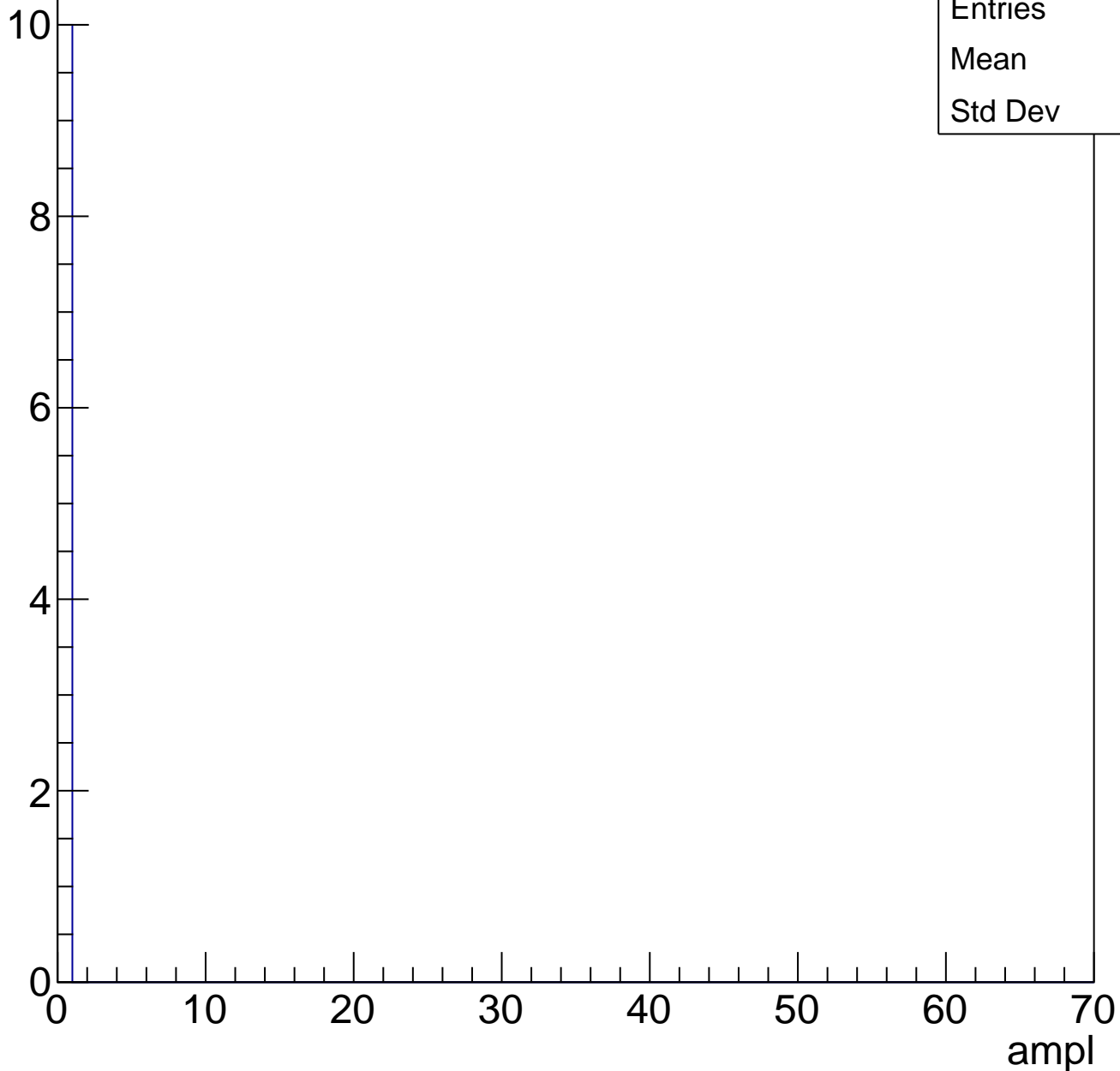
Entry



B1L103S, U14-ch105, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

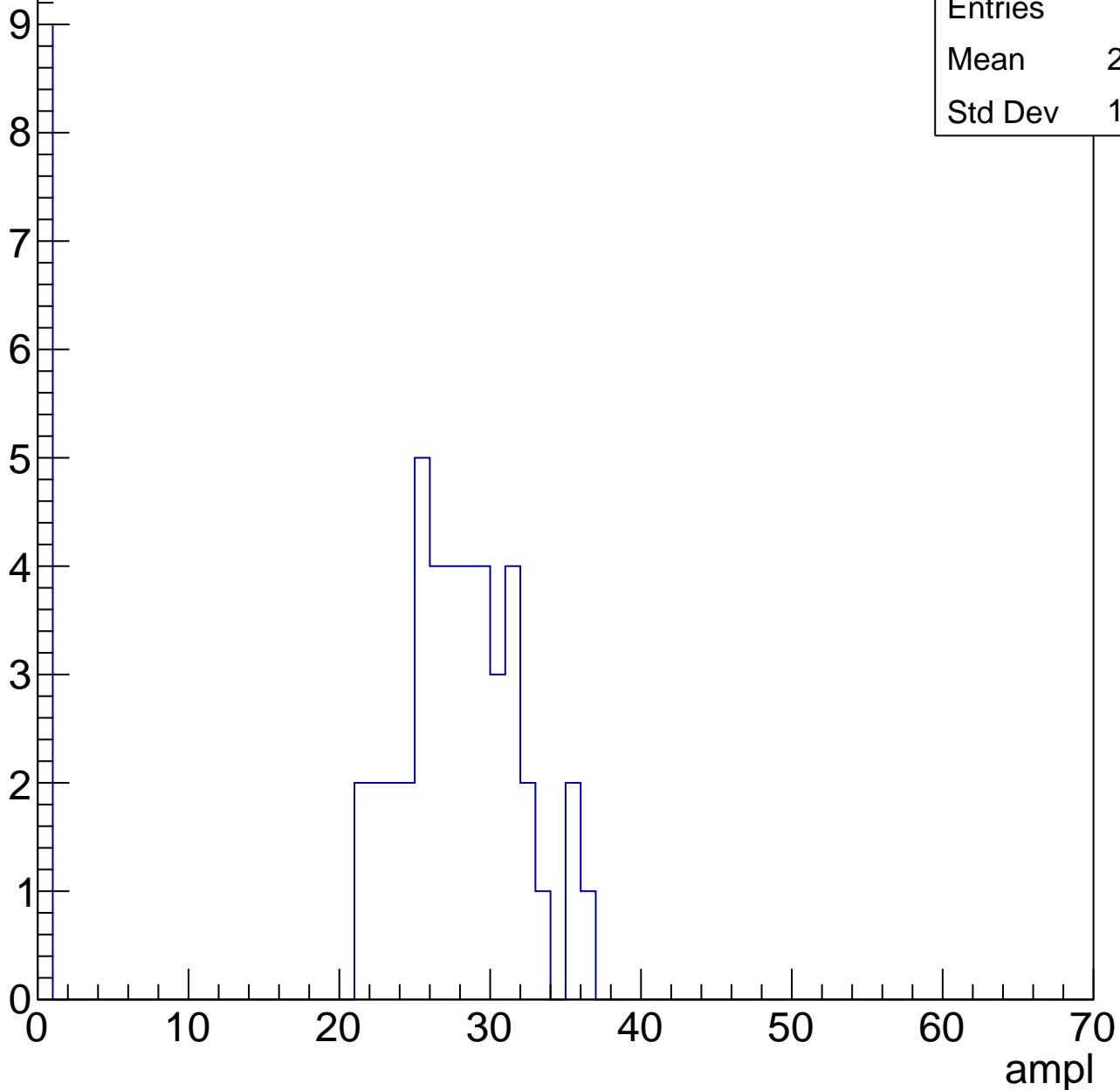


B1L103S, U14-ch106, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	22.78
Std Dev	11.08

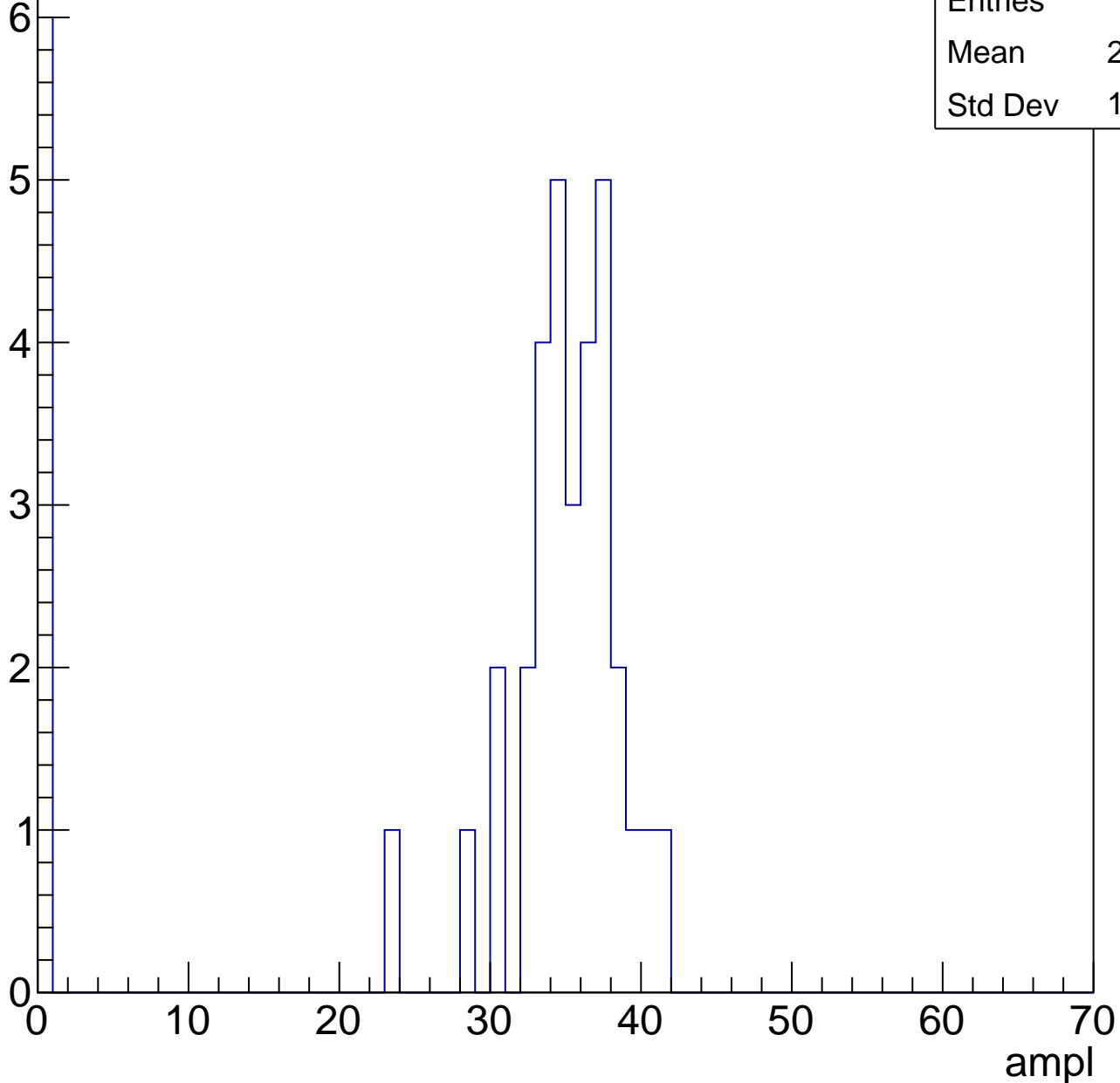


B1L103S, U14-ch106, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

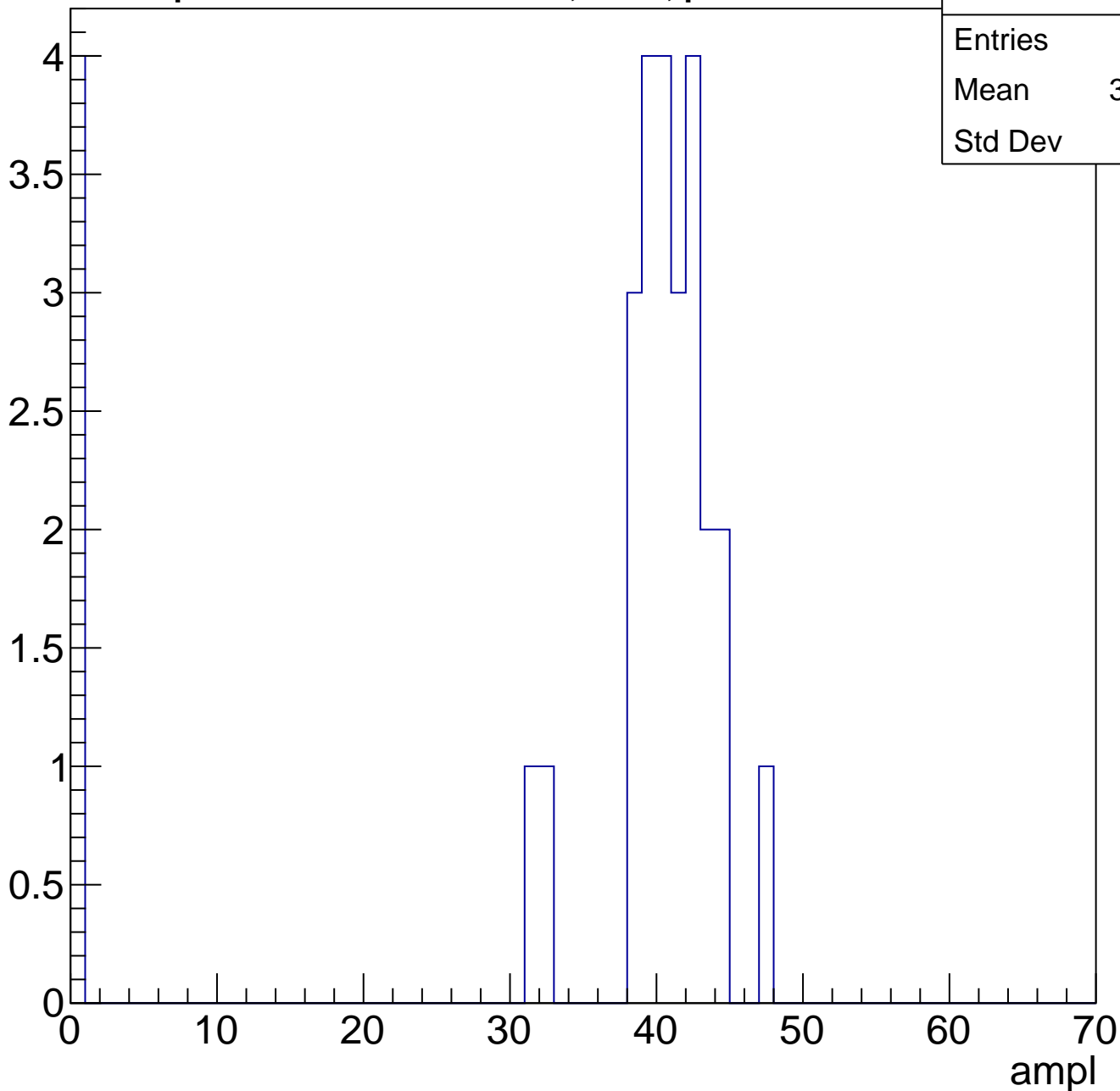
Entries	38
Mean	29.13
Std Dev	13.02



B1L103S, U14-ch106, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

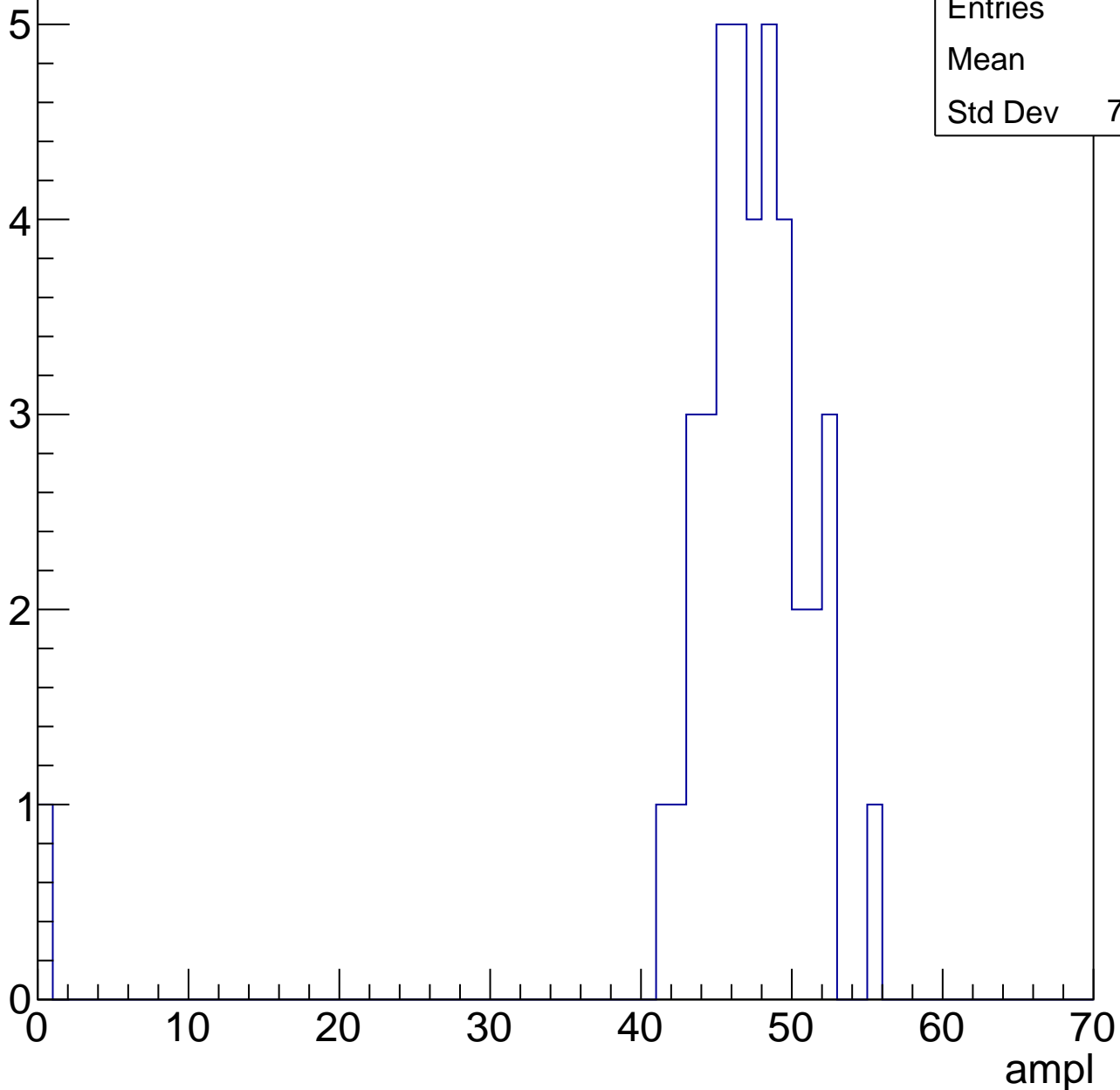


B1L103S, U14-ch106, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

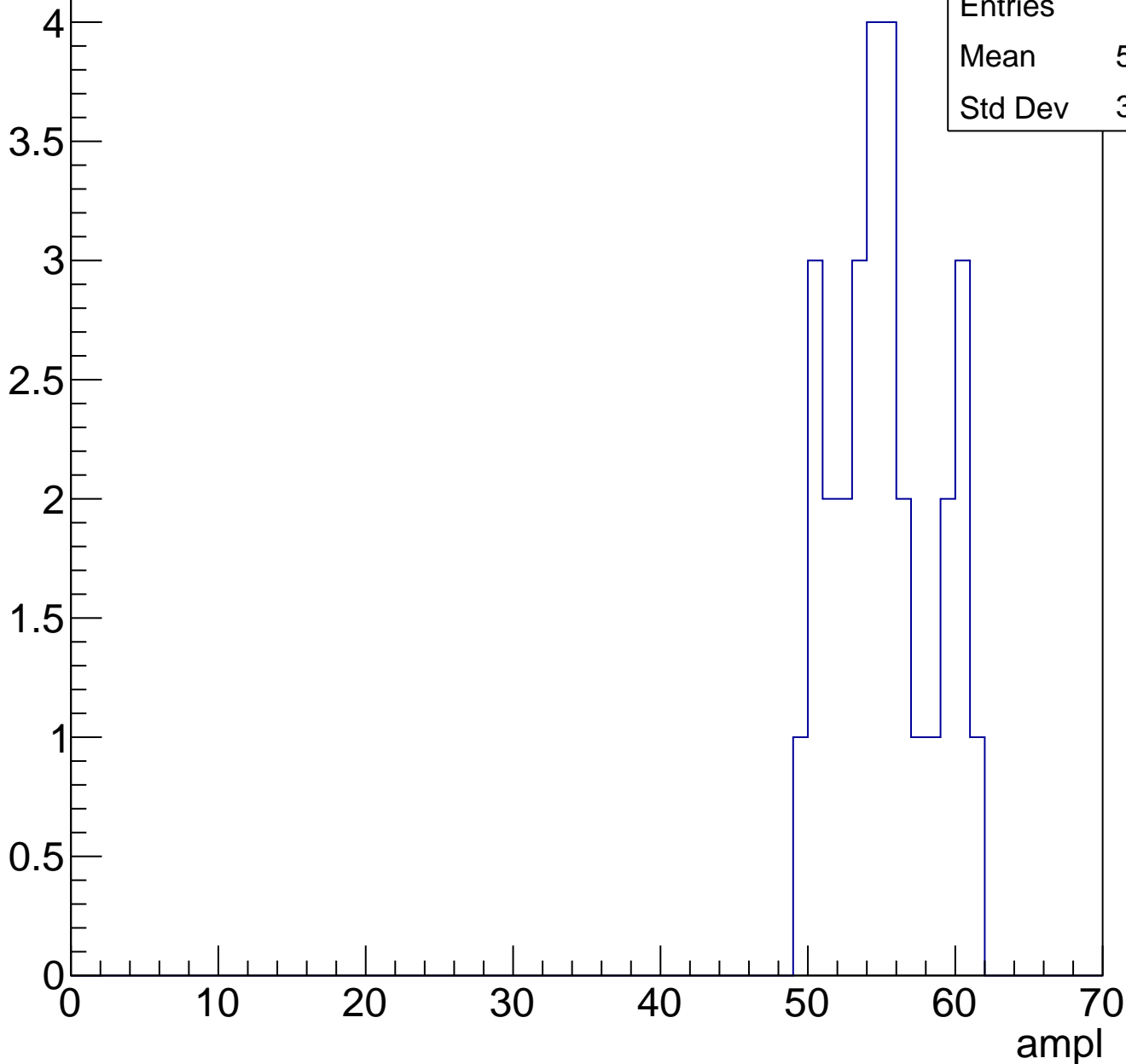
Entries	40
Mean	45.9
Std Dev	7.956



B1L103S, U14-ch106, adc4

calib_packv5_041523_1651.root, FC#0, port C2

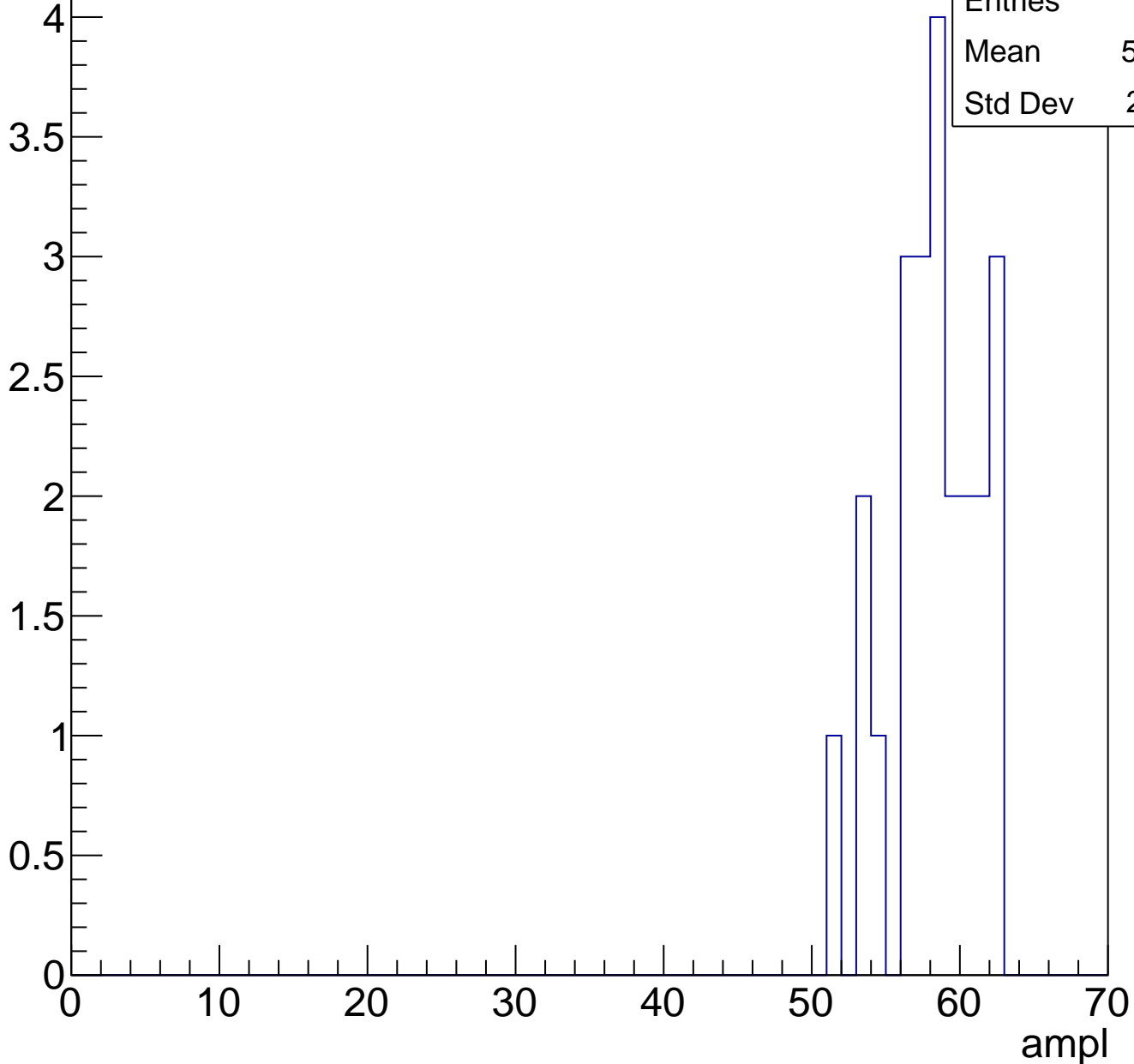
Entry



B1L103S, U14-ch106, adc5

calib_packv5_041523_1651.root, FC#0, port C2

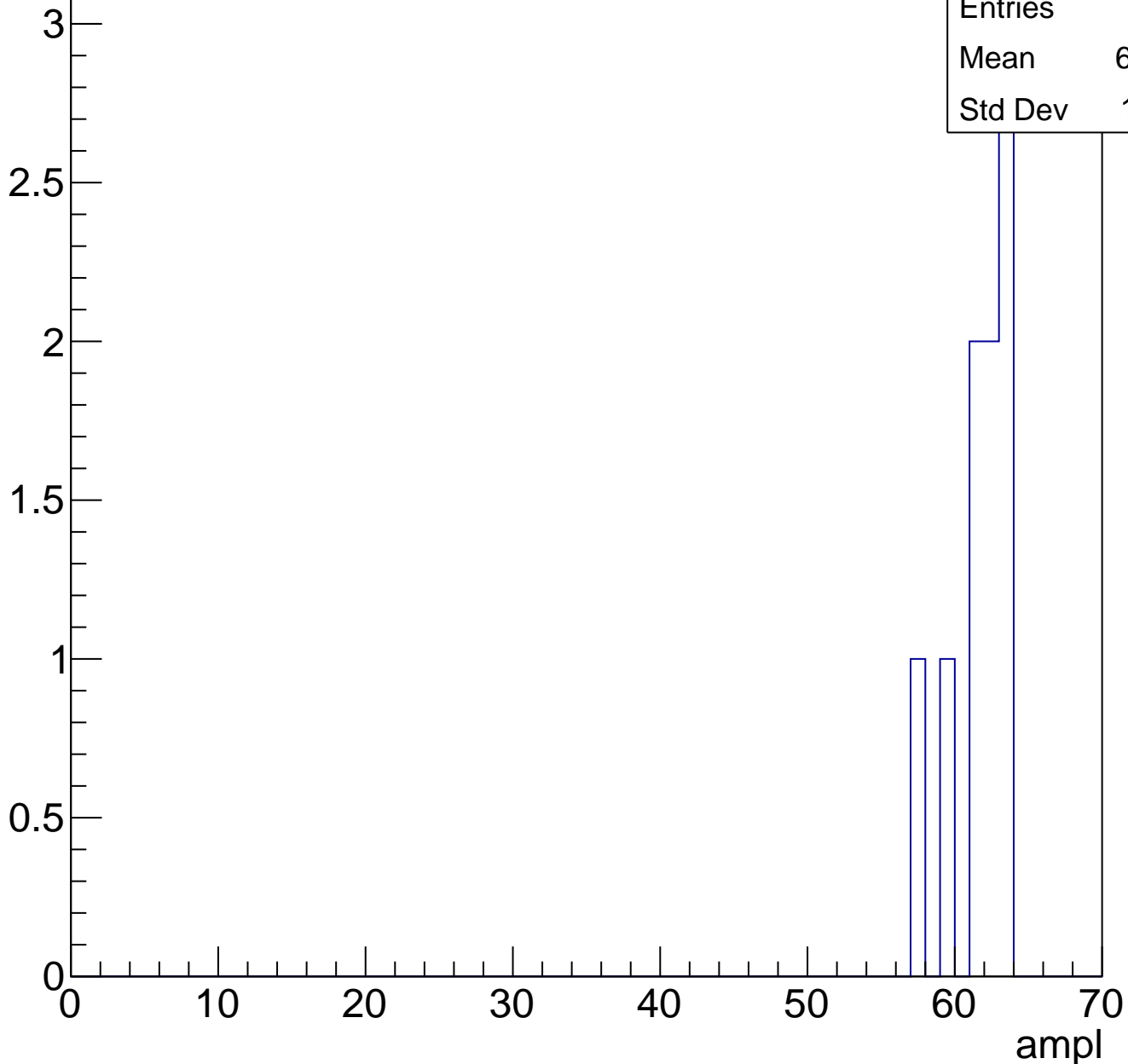
Entry



B1L103S, U14-ch106, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



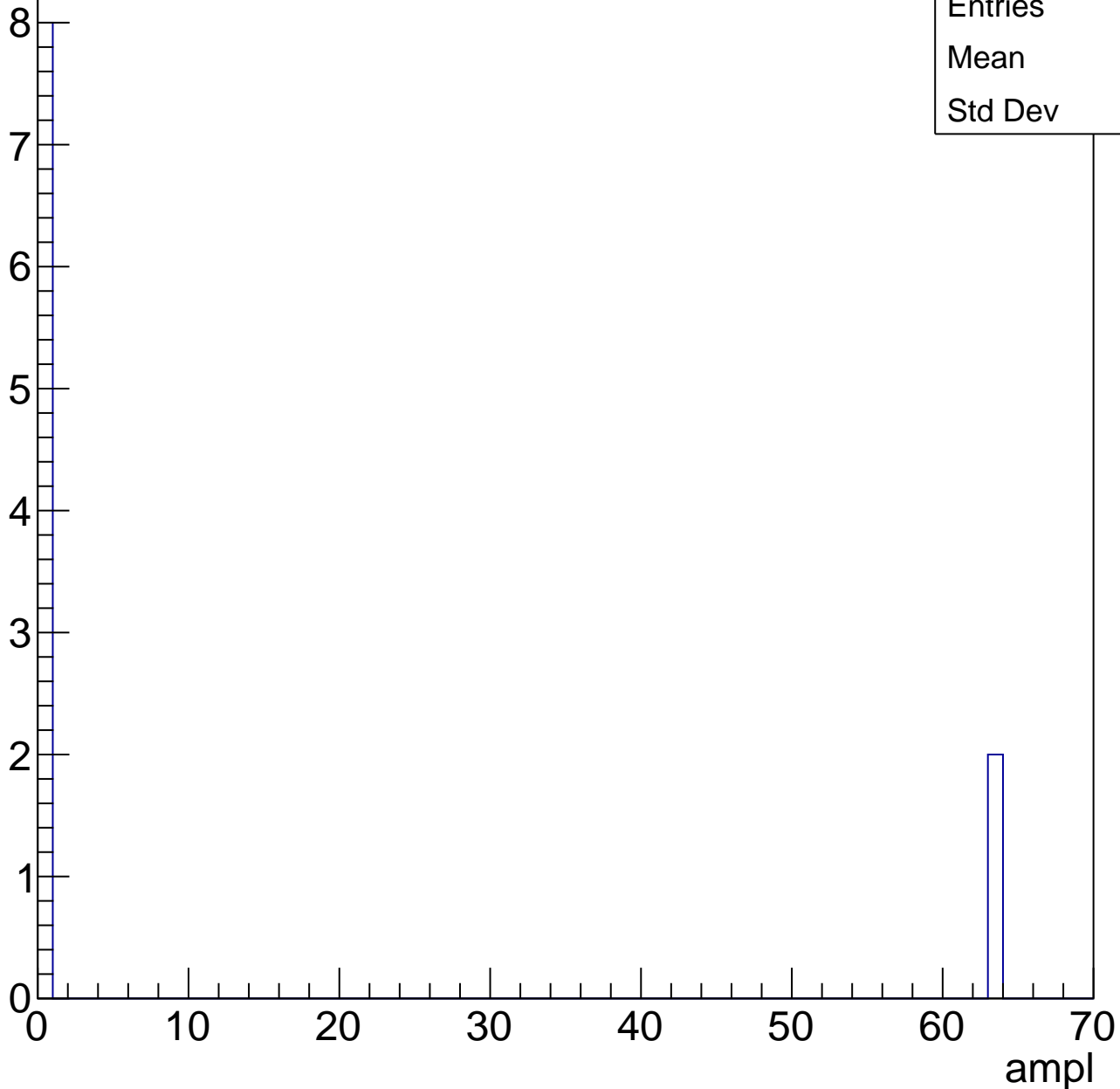
Entries	9
Mean	61.22
Std Dev	1.931

B1L103S, U14-ch106, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	10
Mean	12.6
Std Dev	25.2

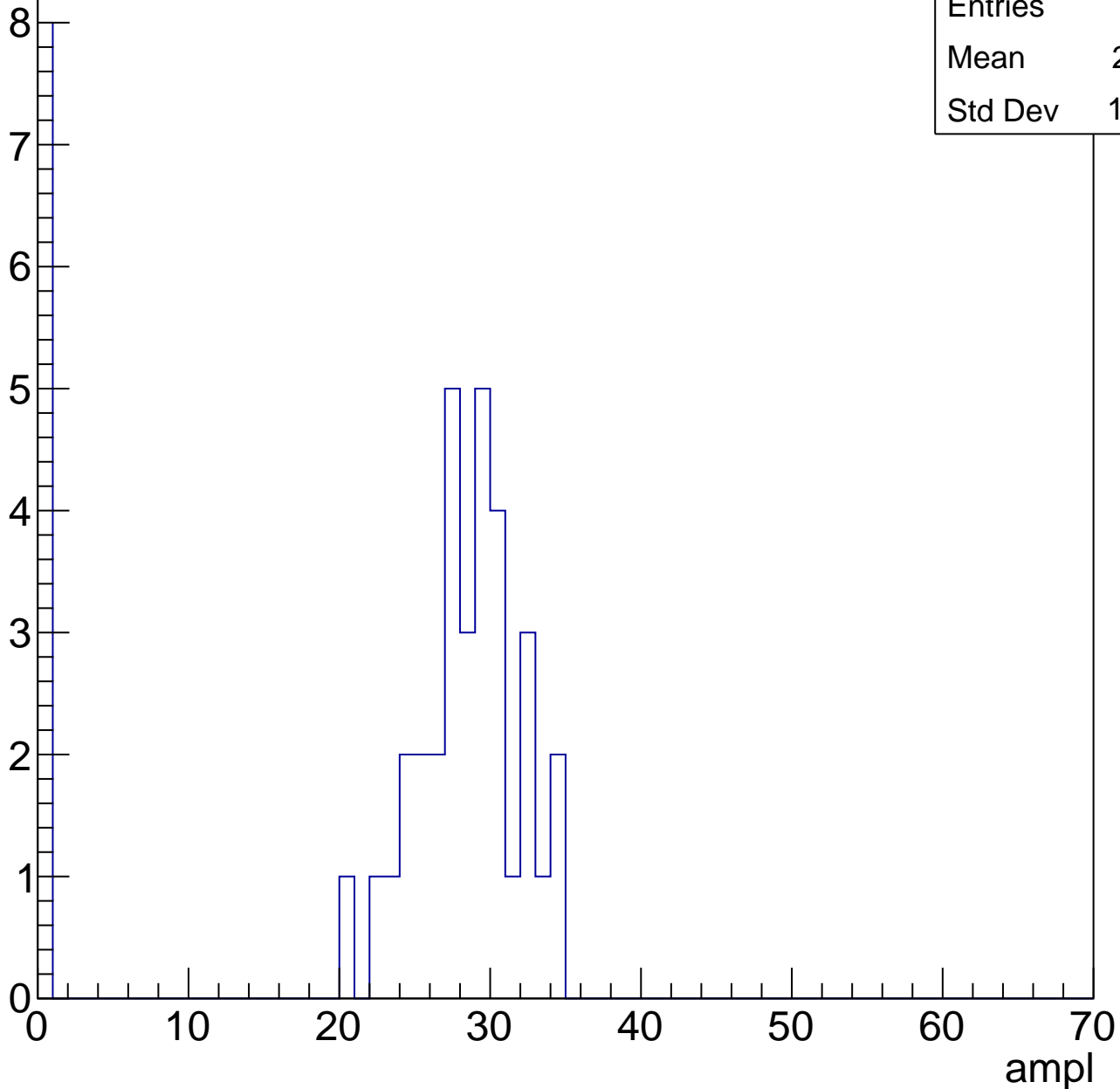


B1L103S, U14-ch107, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

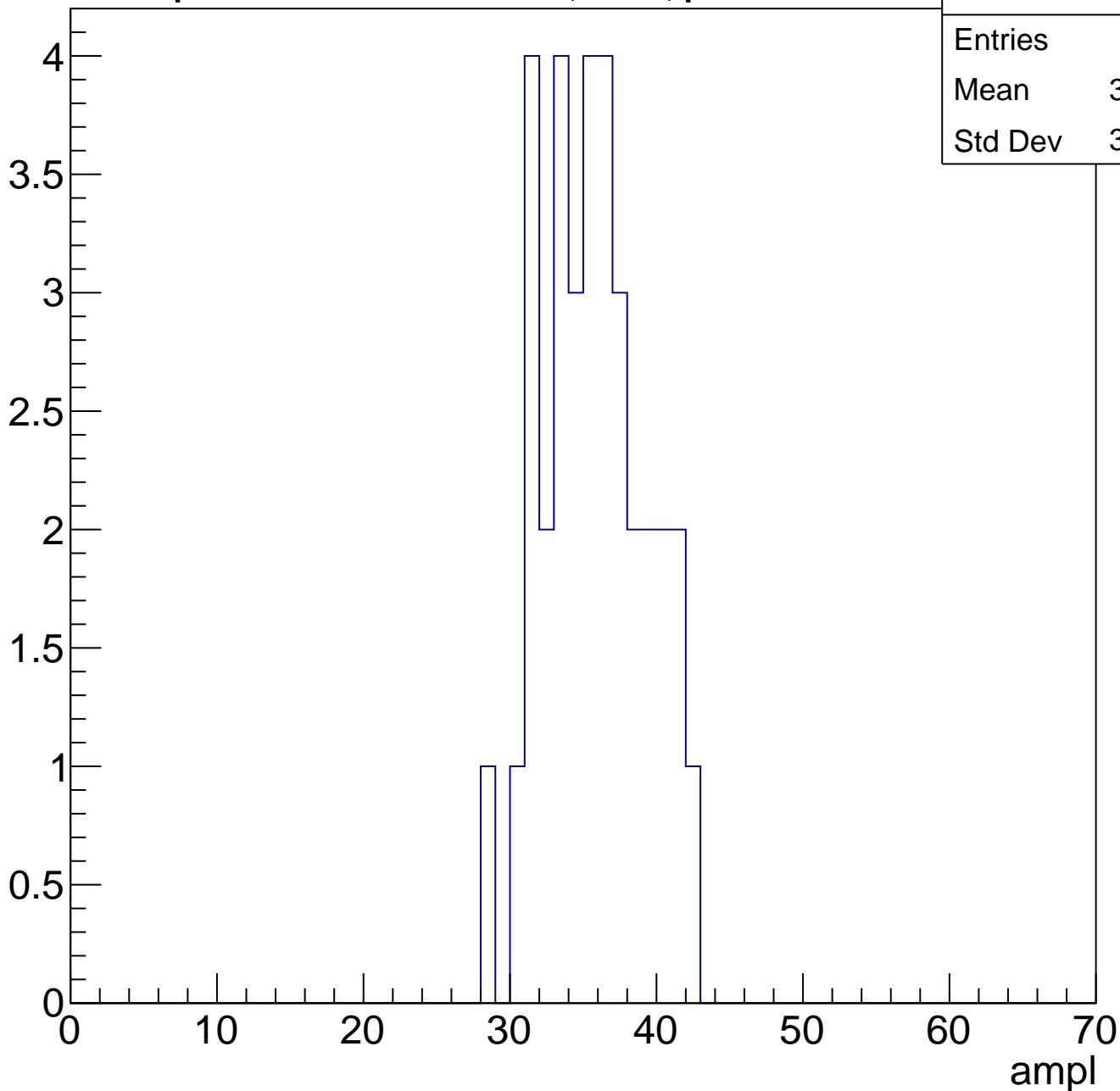
Entries	41
Mean	22.61
Std Dev	11.52



B1L103S, U14-ch107, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry



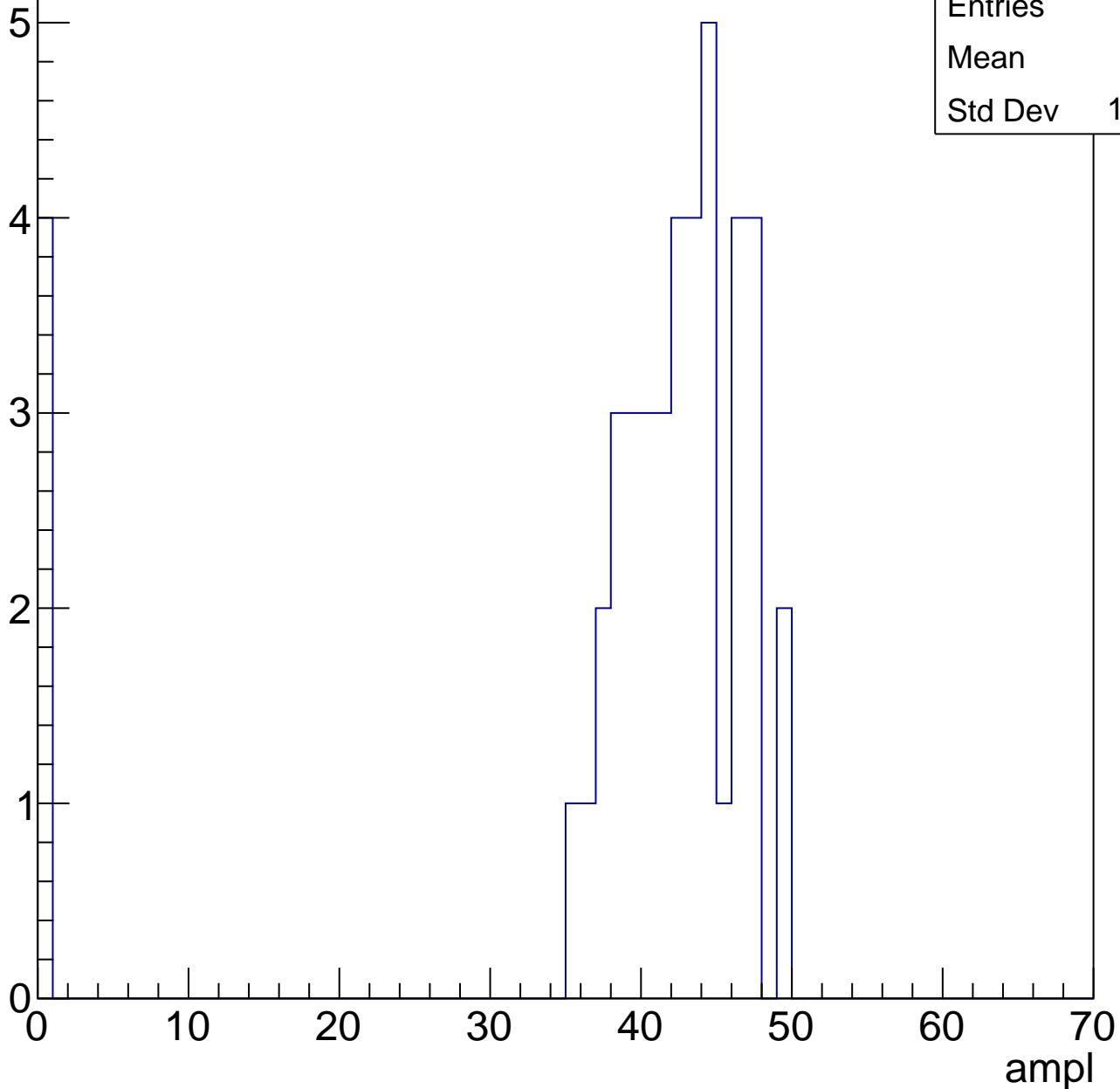
Entries	35
Mean	35.23
Std Dev	3.423

B1L103S, U14-ch107, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	44
Mean	38.5
Std Dev	12.65

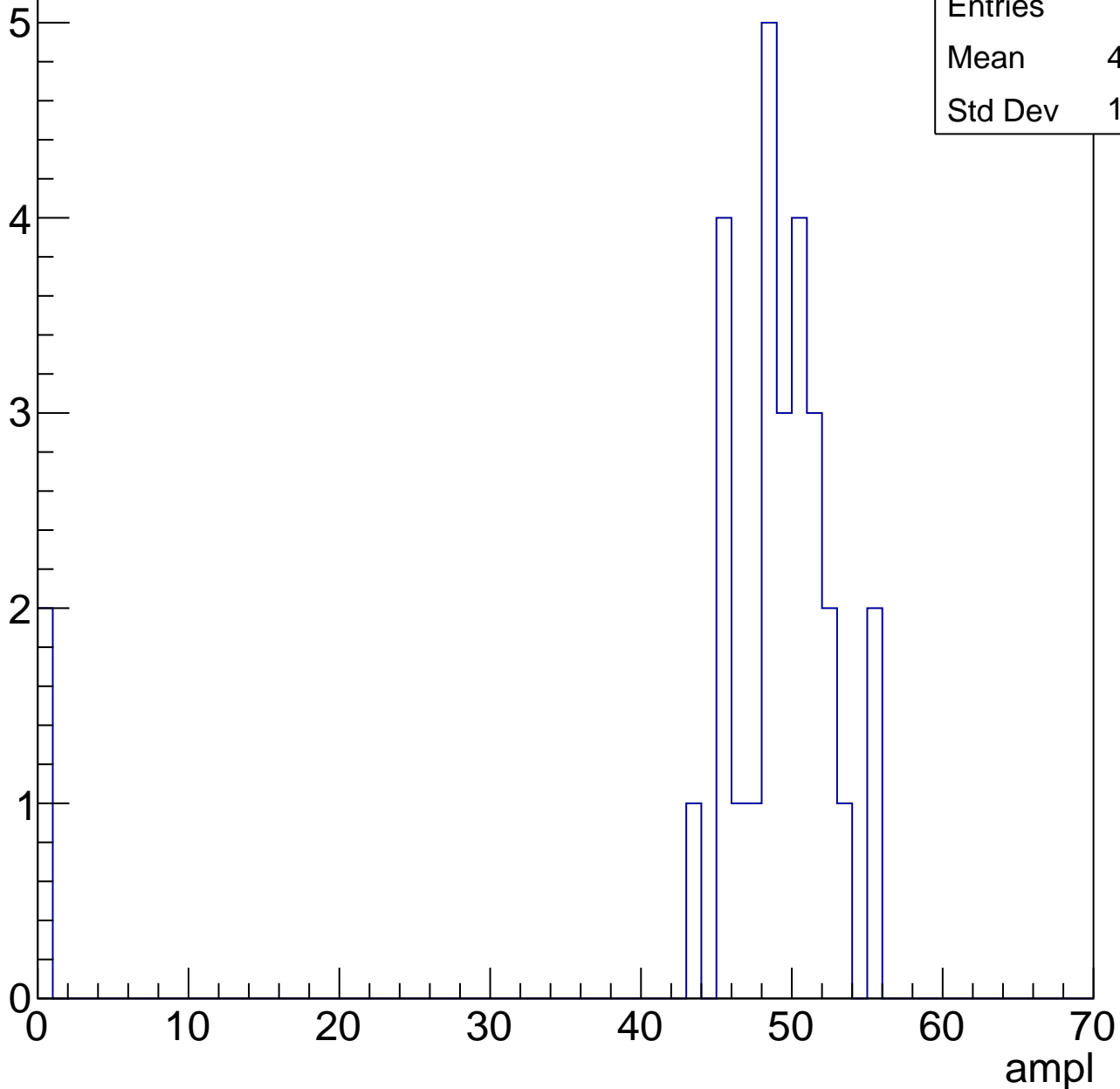


B1L103S, U14-ch107, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

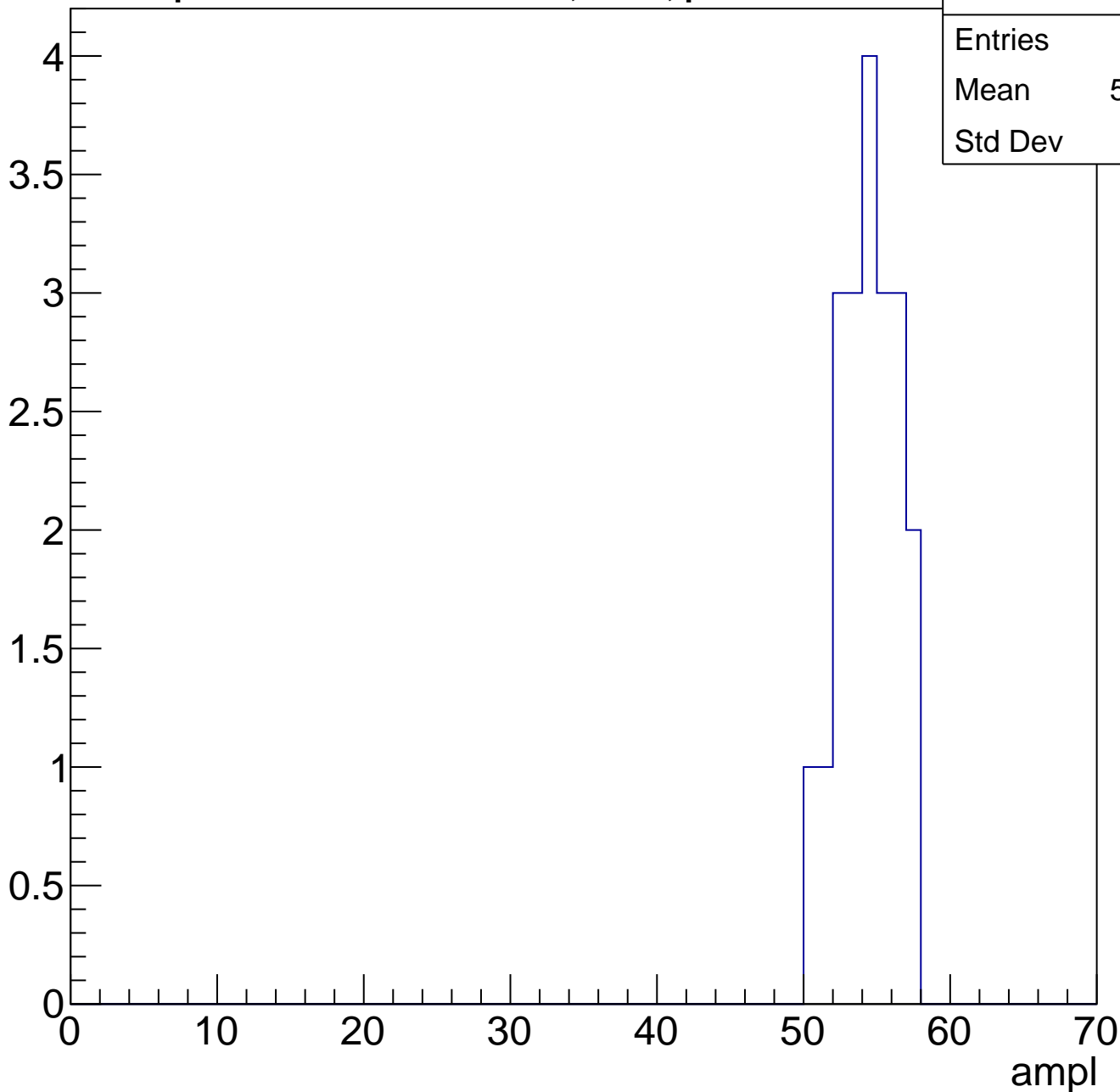
Entries	29
Mean	45.62
Std Dev	12.75



B1L103S, U14-ch107, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	20
Mean	53.95
Std Dev	1.91

B1L103S, U14-ch107, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

5

4

3

2

1

0

Entries

32

Mean

58.97

Std Dev

2.812

ampl

0

10

20

30

40

50

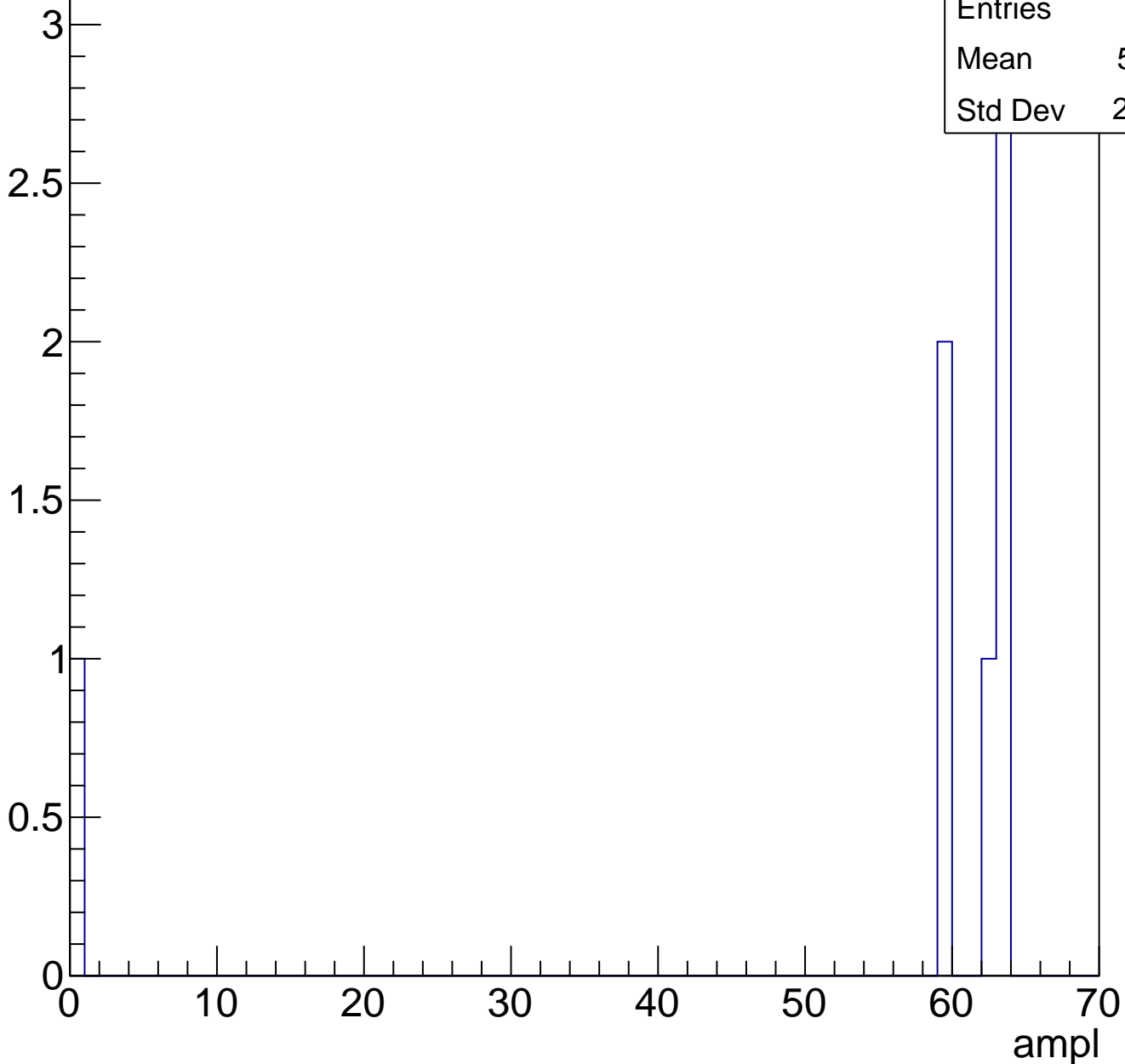
60

70

B1L103S, U14-ch107, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch107, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

12

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

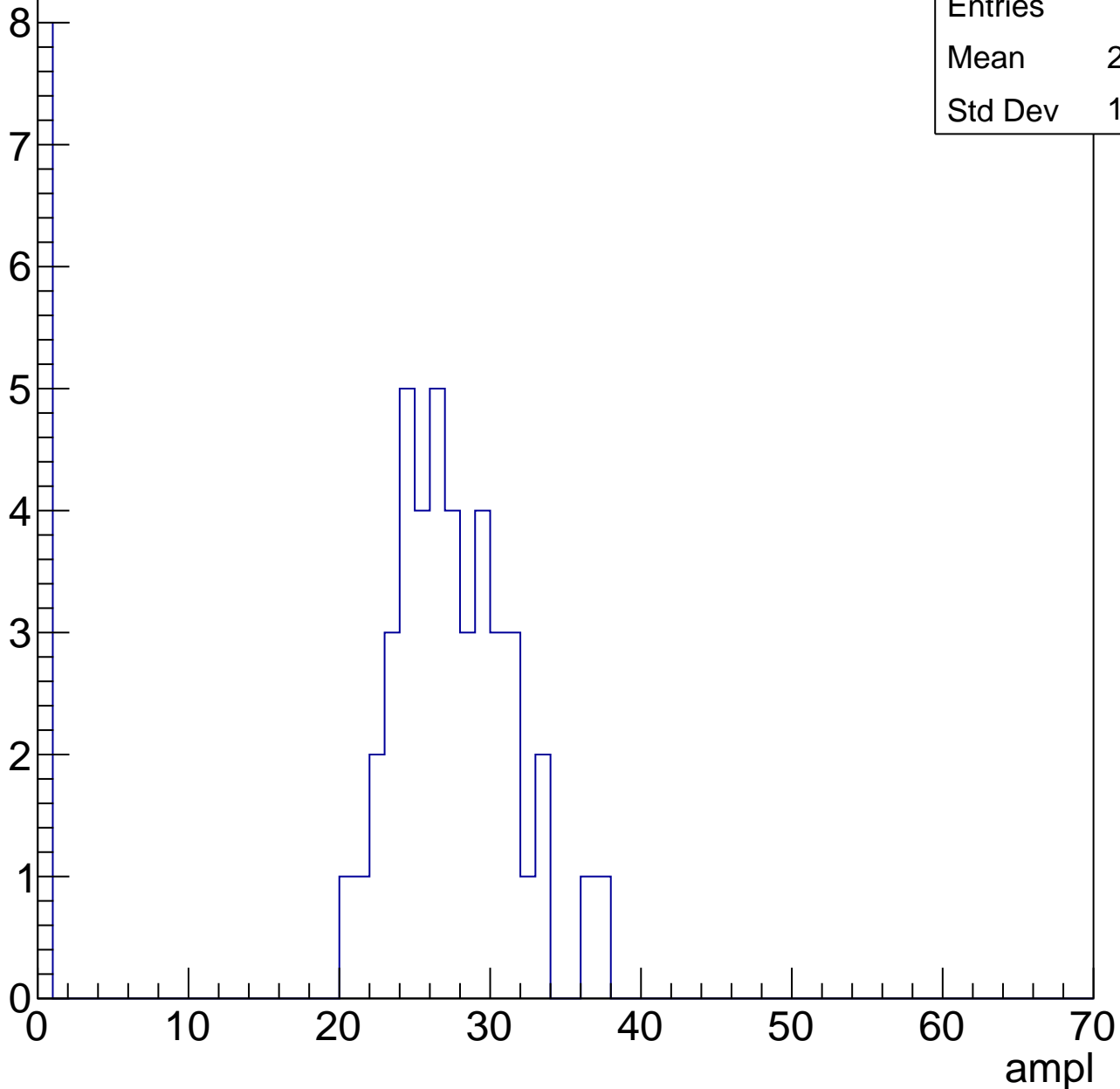
Entries	13
Mean	0
Std Dev	0

B1L103S, U14-ch108, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	22.86
Std Dev	10.46



B1L103S, U14-ch108, adc1

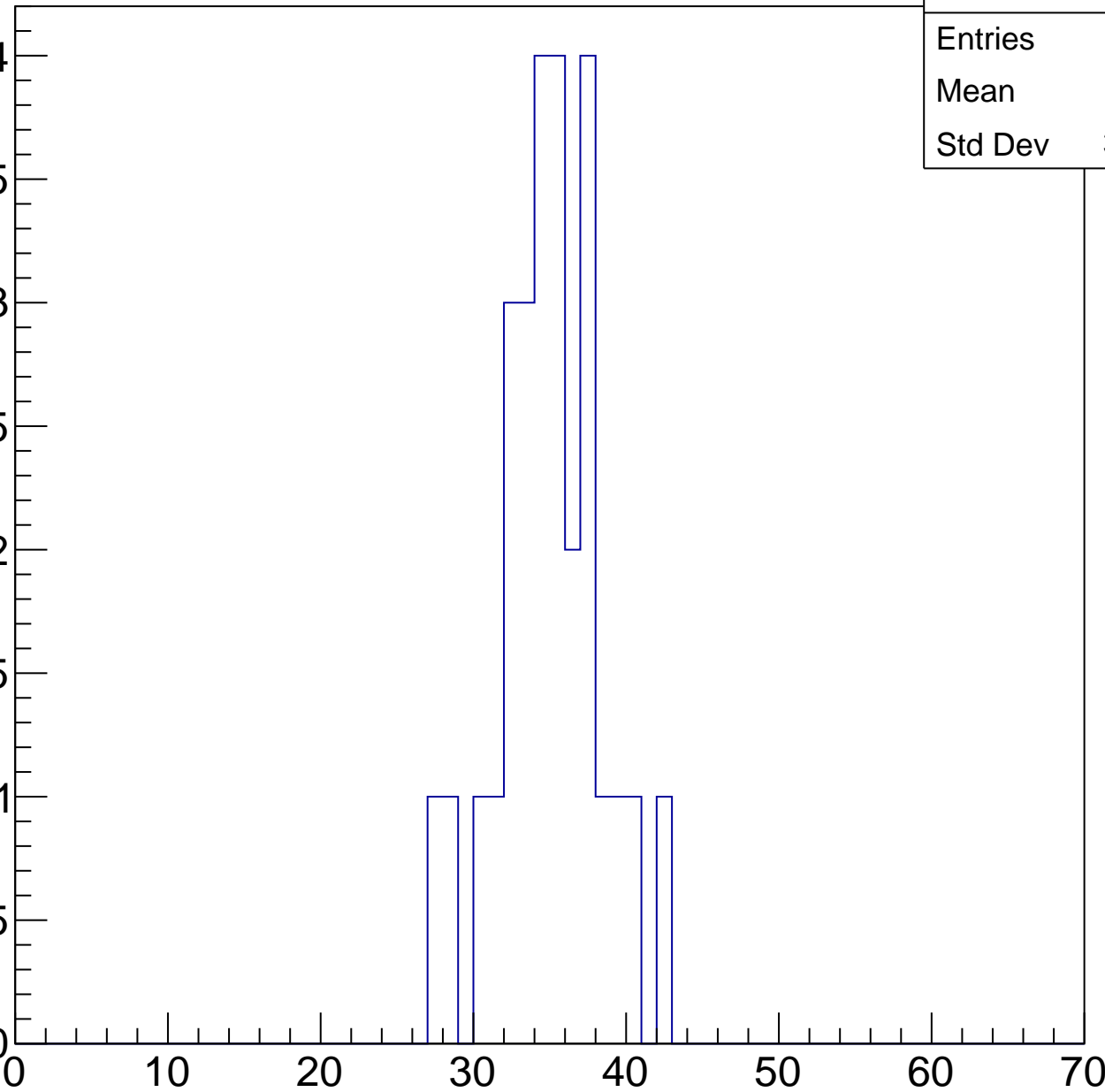
calib_packv5_041523_1651.root, FC#0, port C2

Entry

4
3.5
3
2.5
2
1.5
1
0.5
0

Entries	28
Mean	34.5
Std Dev	3.311

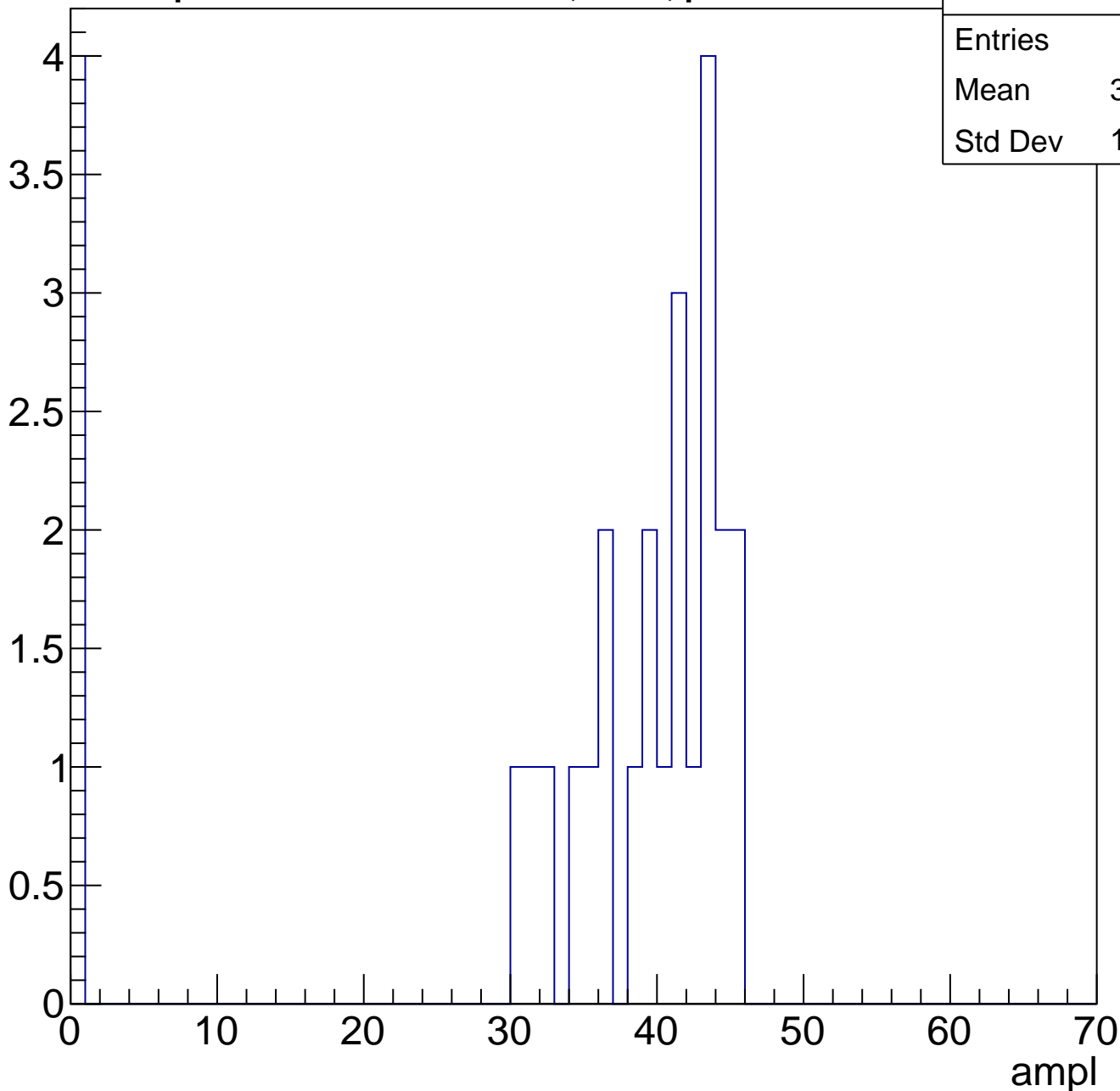
ampl



B1L103S, U14-ch108, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

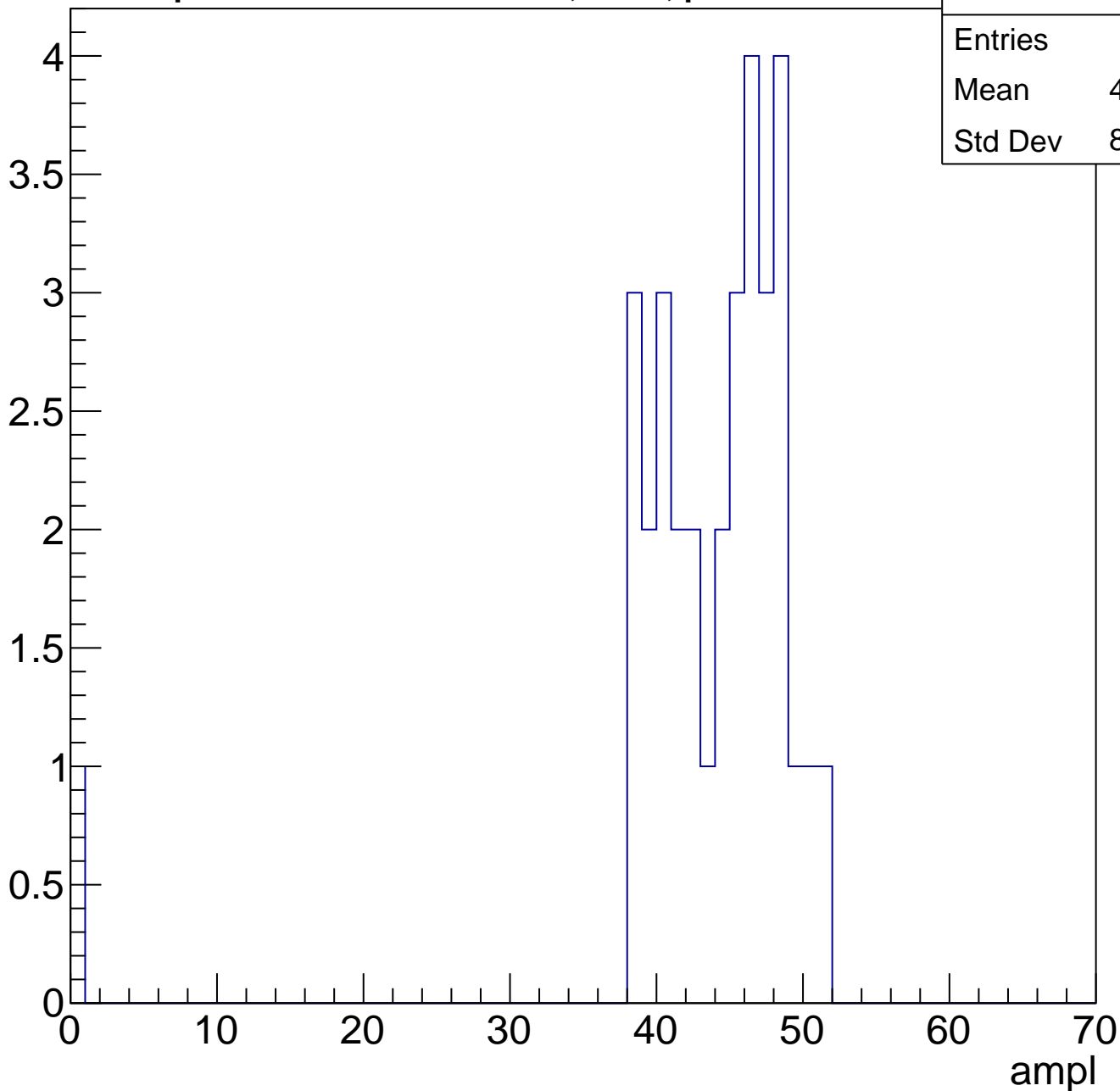


Entries	27
Mean	33.52
Std Dev	14.57

B1L103S, U14-ch108, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

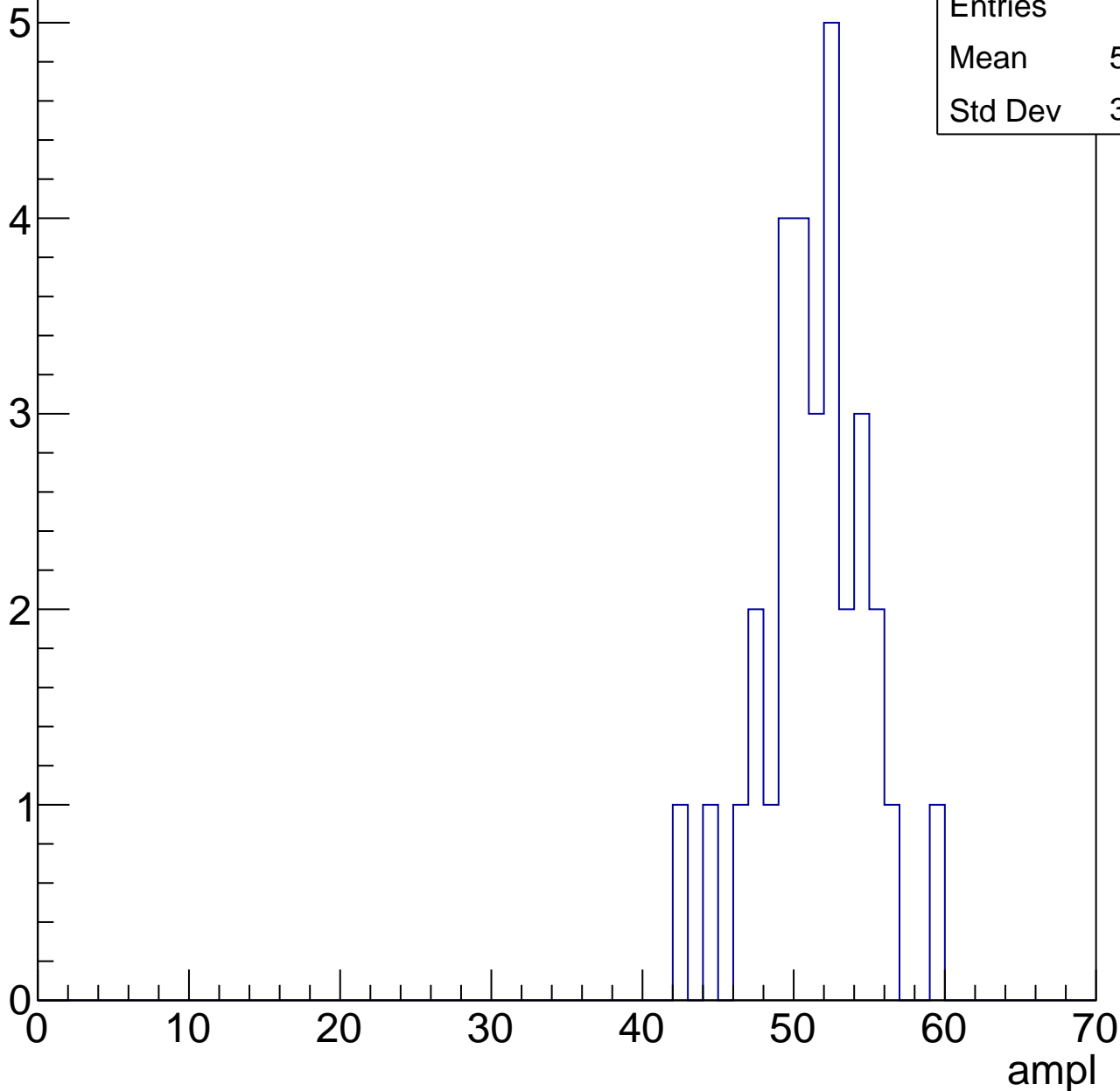


B1L103S, U14-ch108, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	31
Mean	50.84
Std Dev	3.484

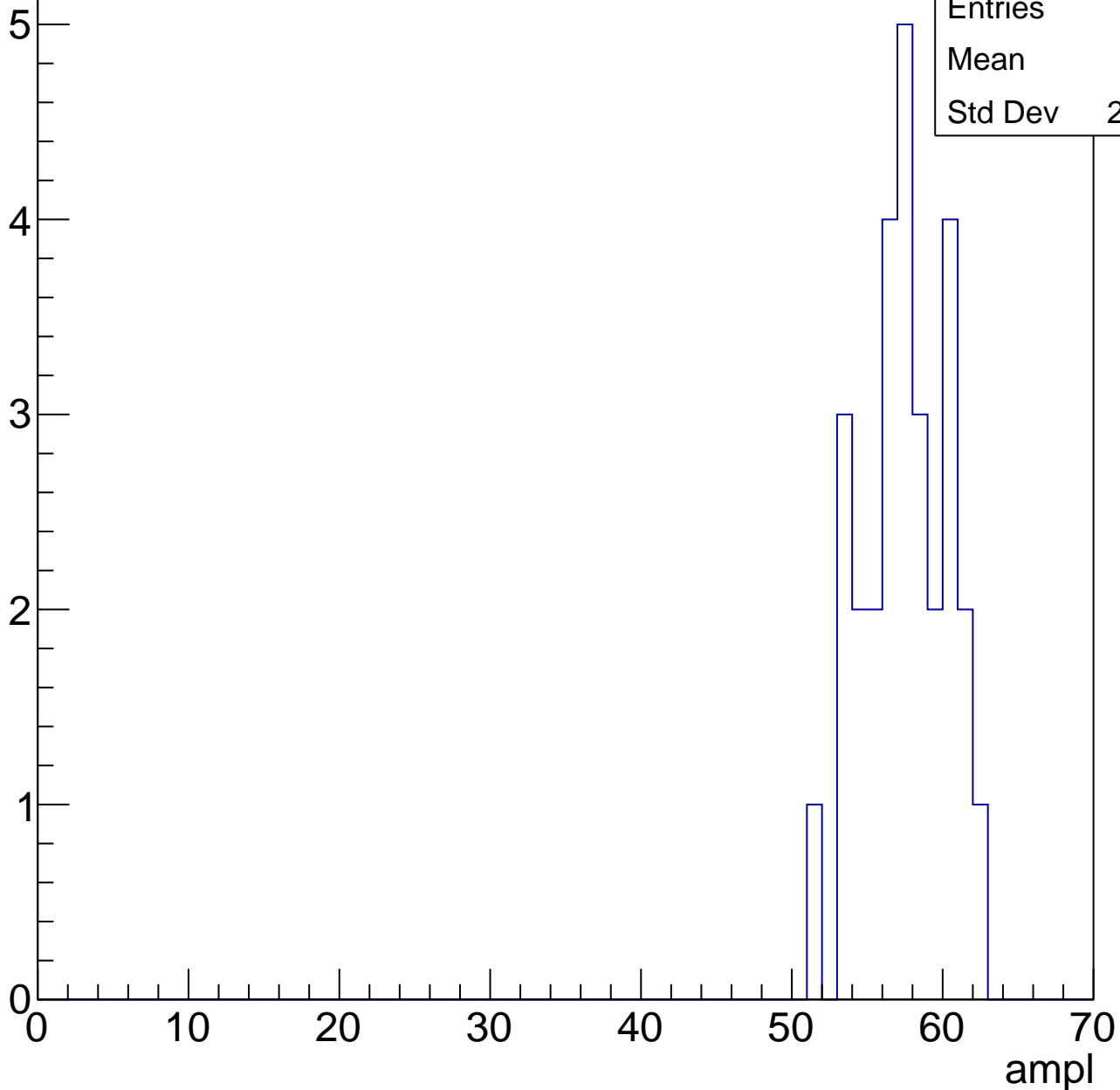


B1L103S, U14-ch108, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

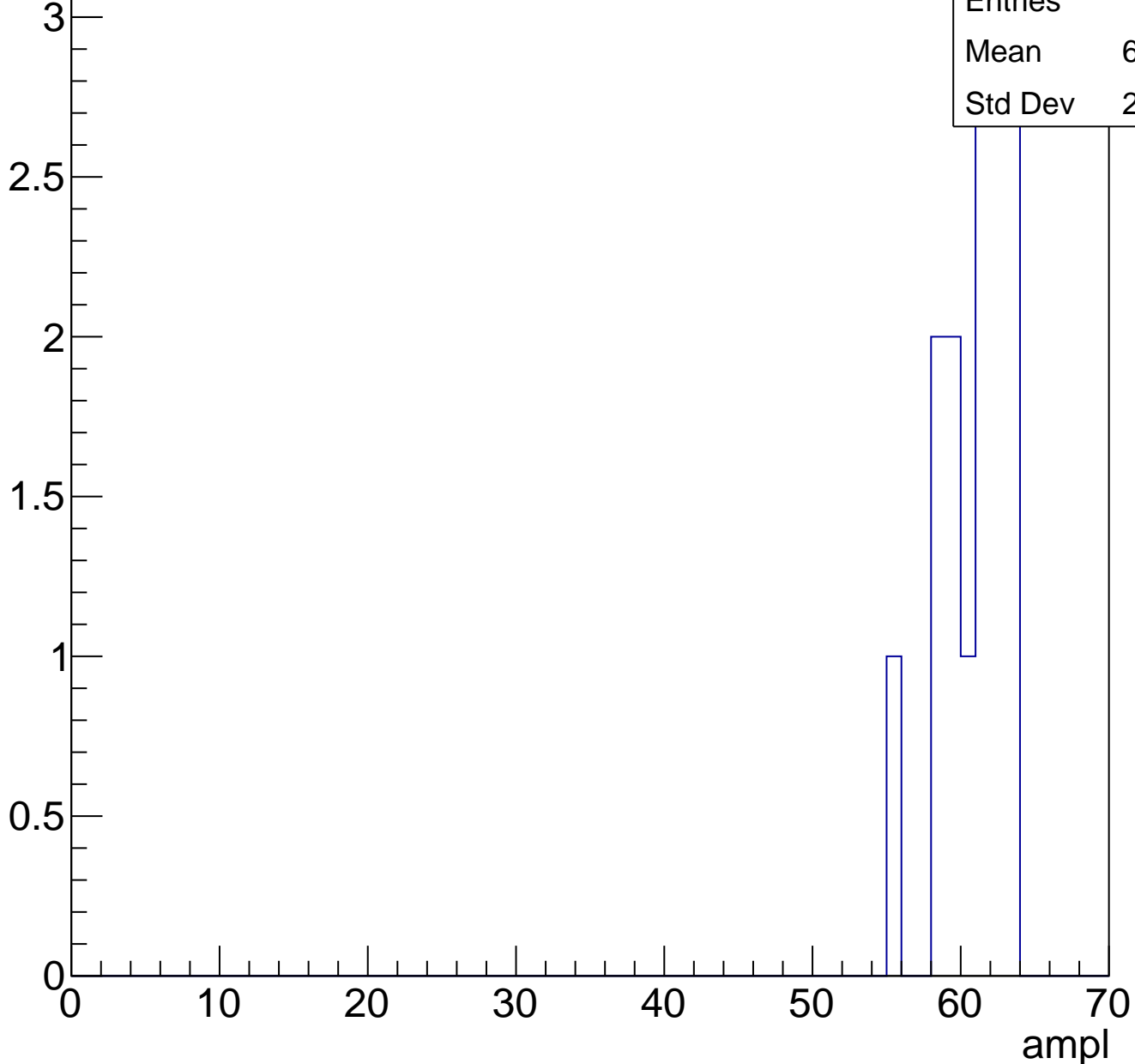
Entries	29
Mean	57
Std Dev	2.742



B1L103S, U14-ch108, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	15
Mean	60.47
Std Dev	2.217

B1L103S, U14-ch108, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	16
Mean	11.75
Std Dev	24.46

Entry

12

10

8

6

4

2

0

0

10

20

30

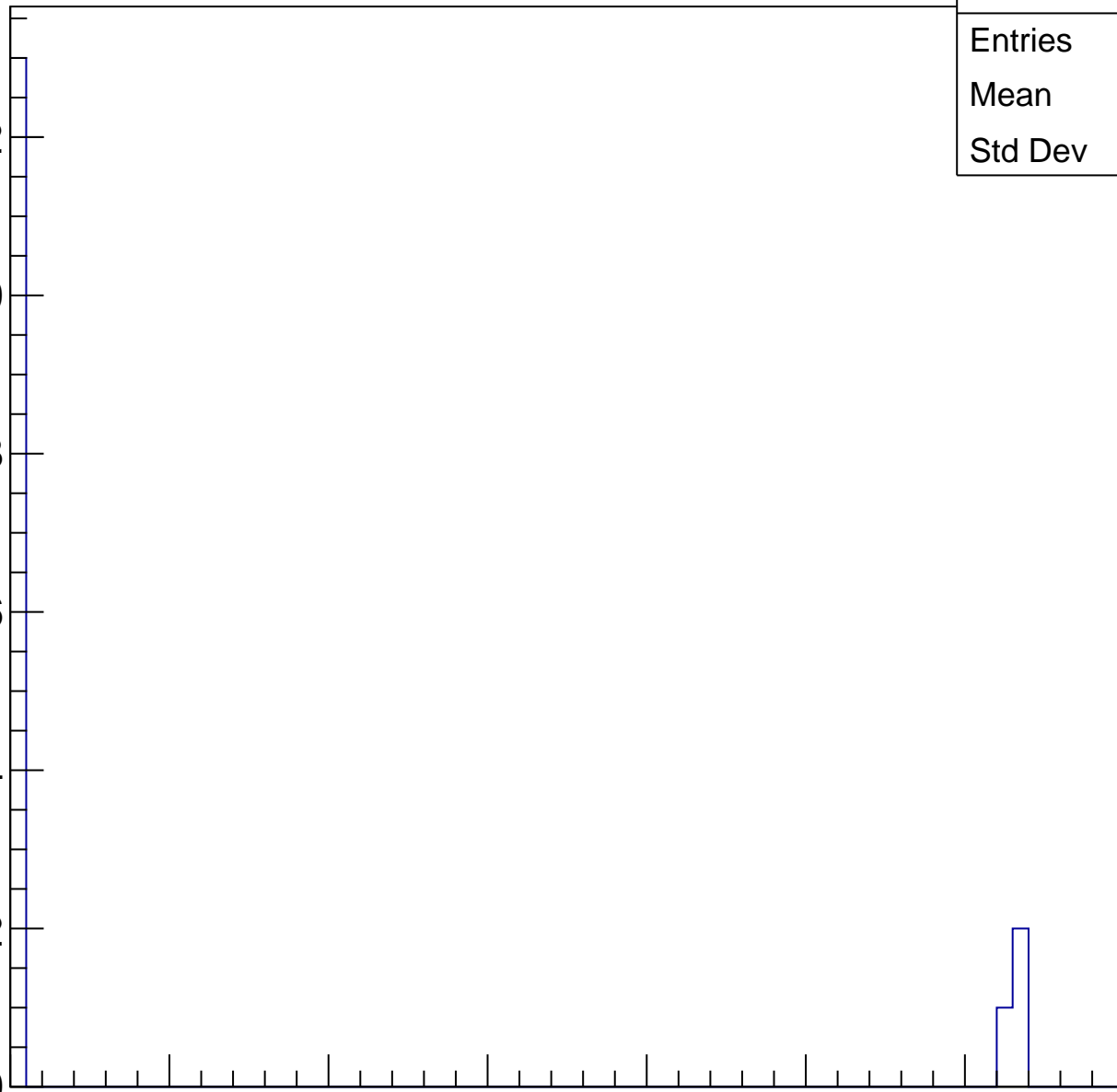
40

50

60

70

ampl

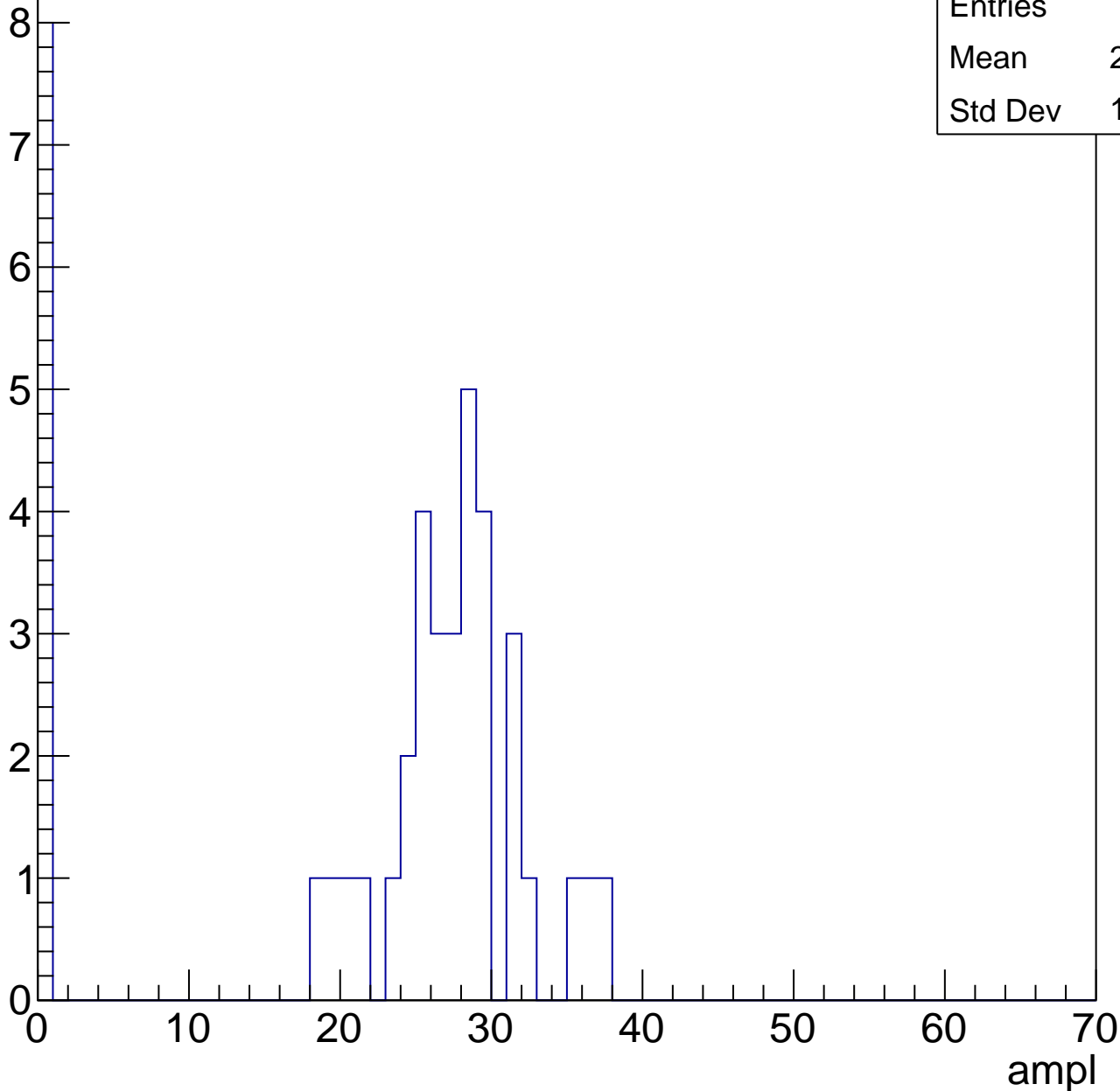


B1L103S, U14-ch109, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	41
Mean	21.88
Std Dev	11.45

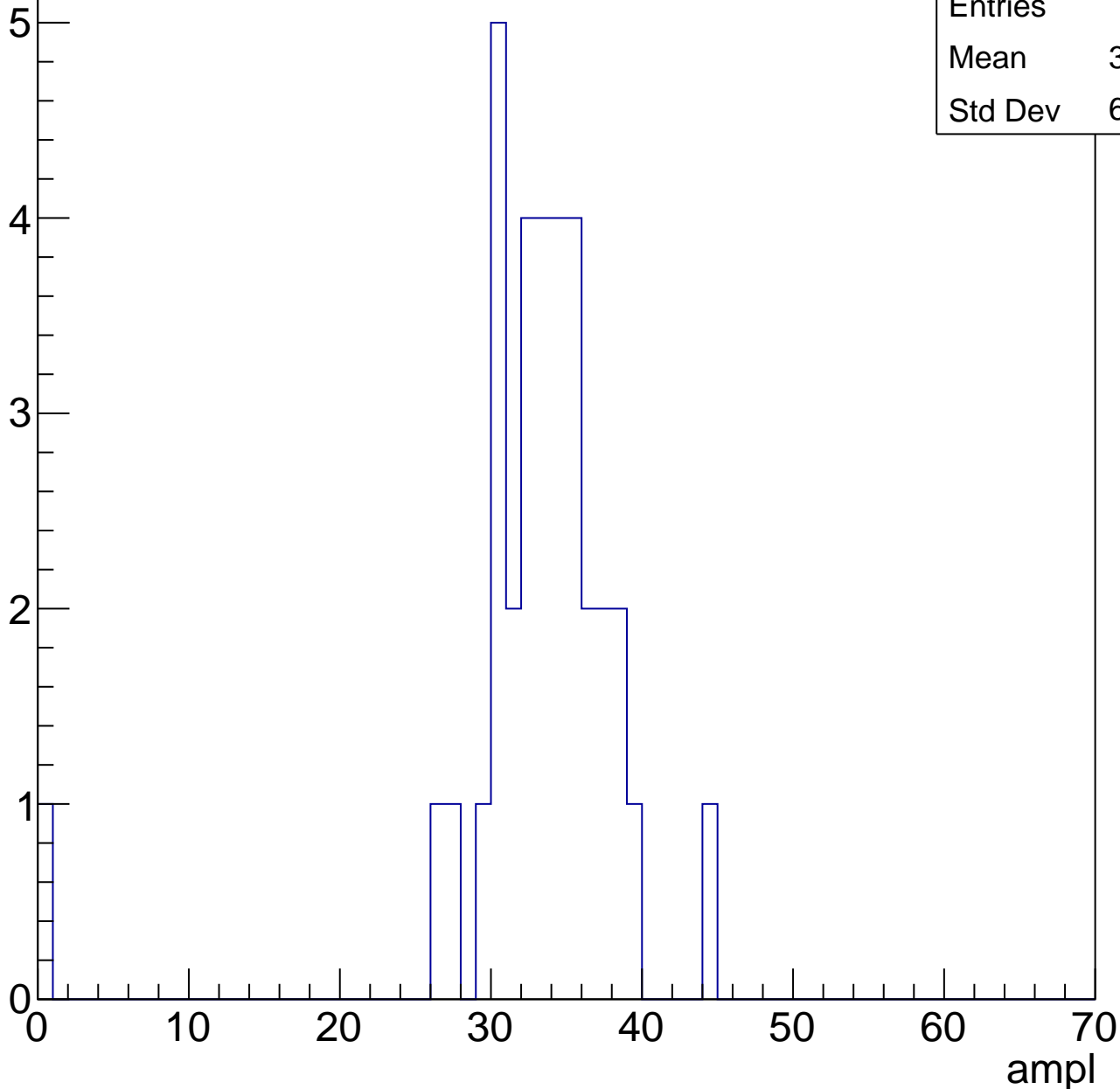


B1L103S, U14-ch109, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	35
Mean	32.43
Std Dev	6.574

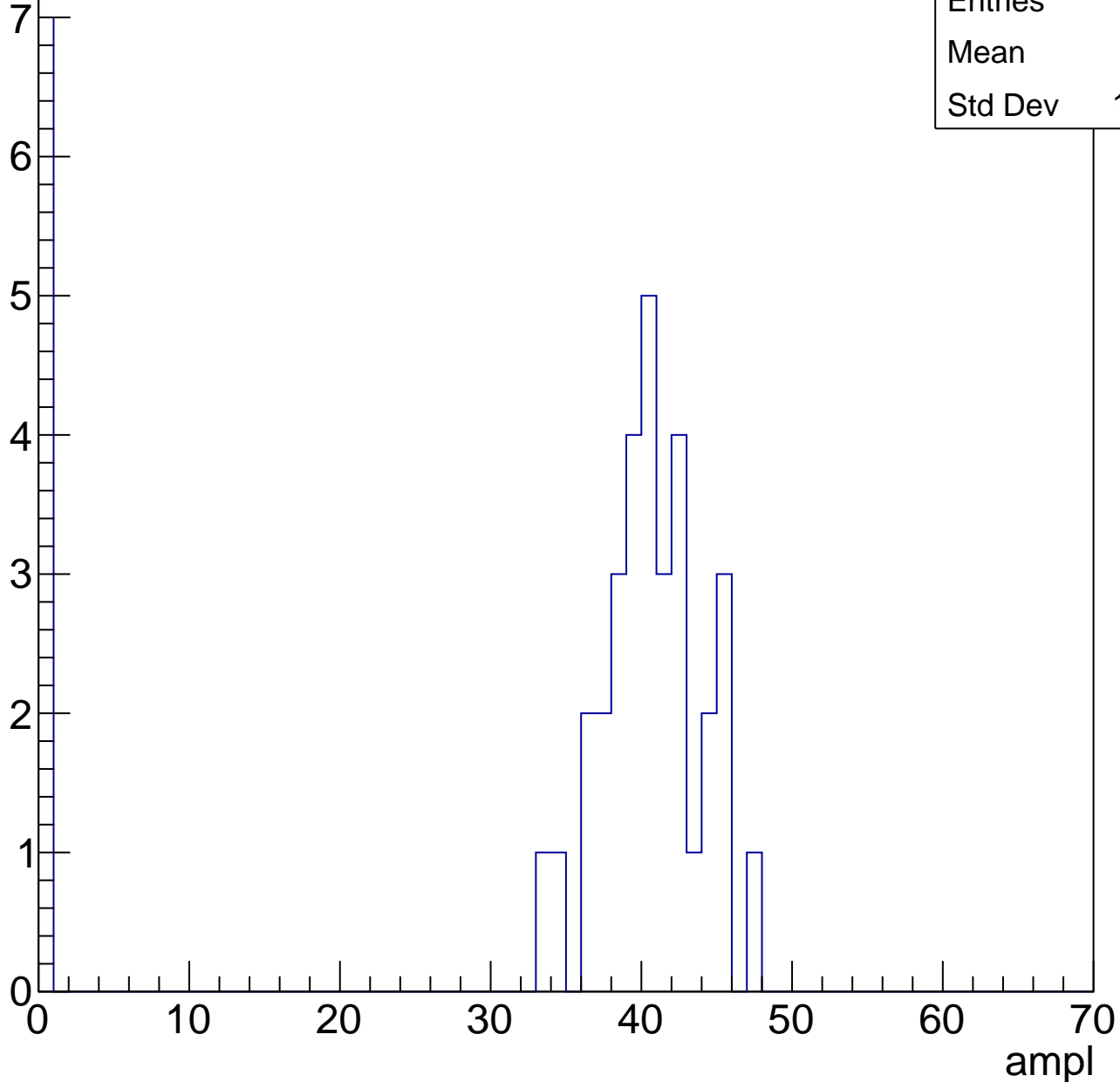


B1L103S, U14-ch109, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

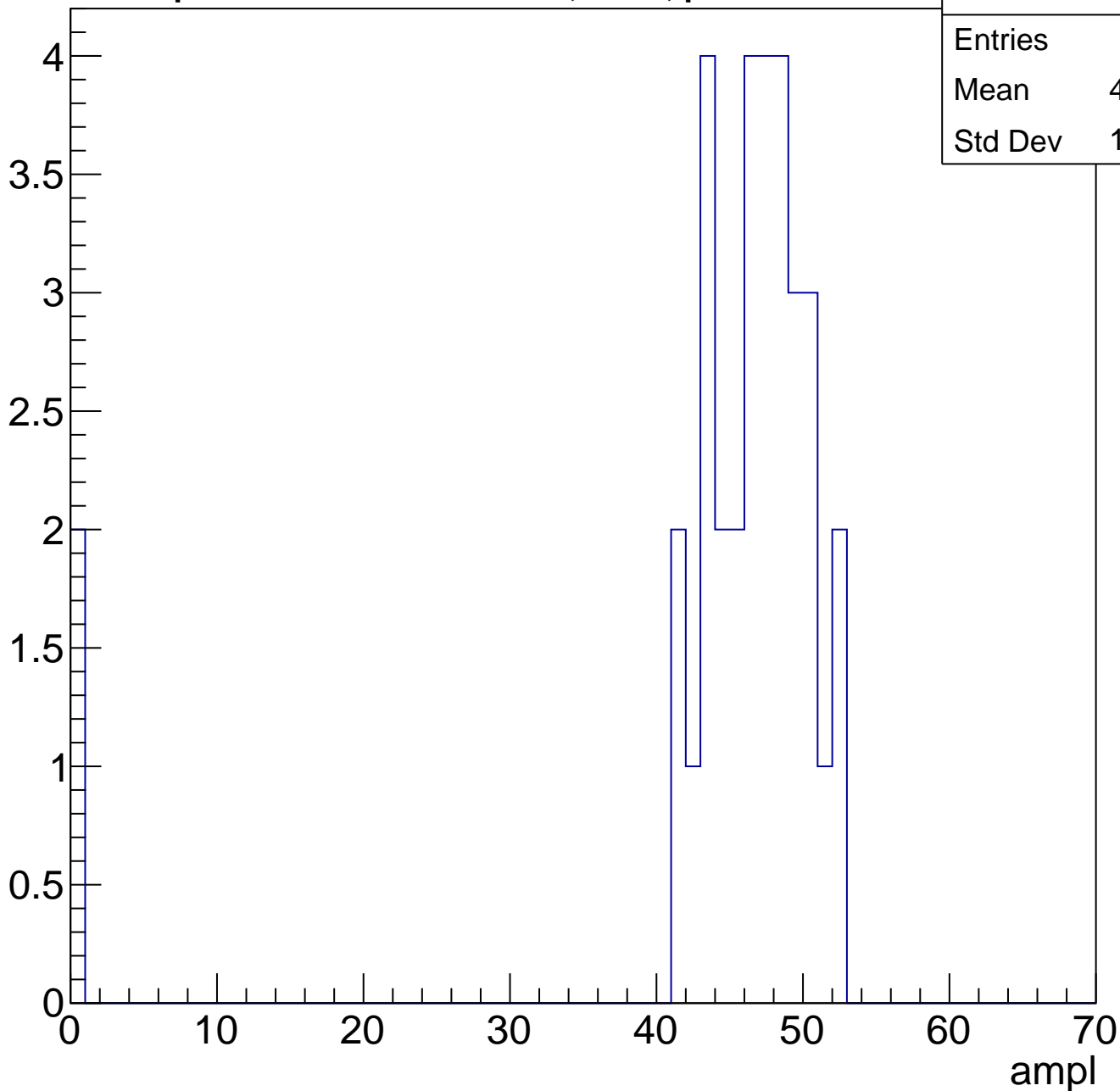
Entries	39
Mean	33
Std Dev	15.71



B1L103S, U14-ch109, adc3

calib_packv5_041523_1651.root, FC#0, port C2

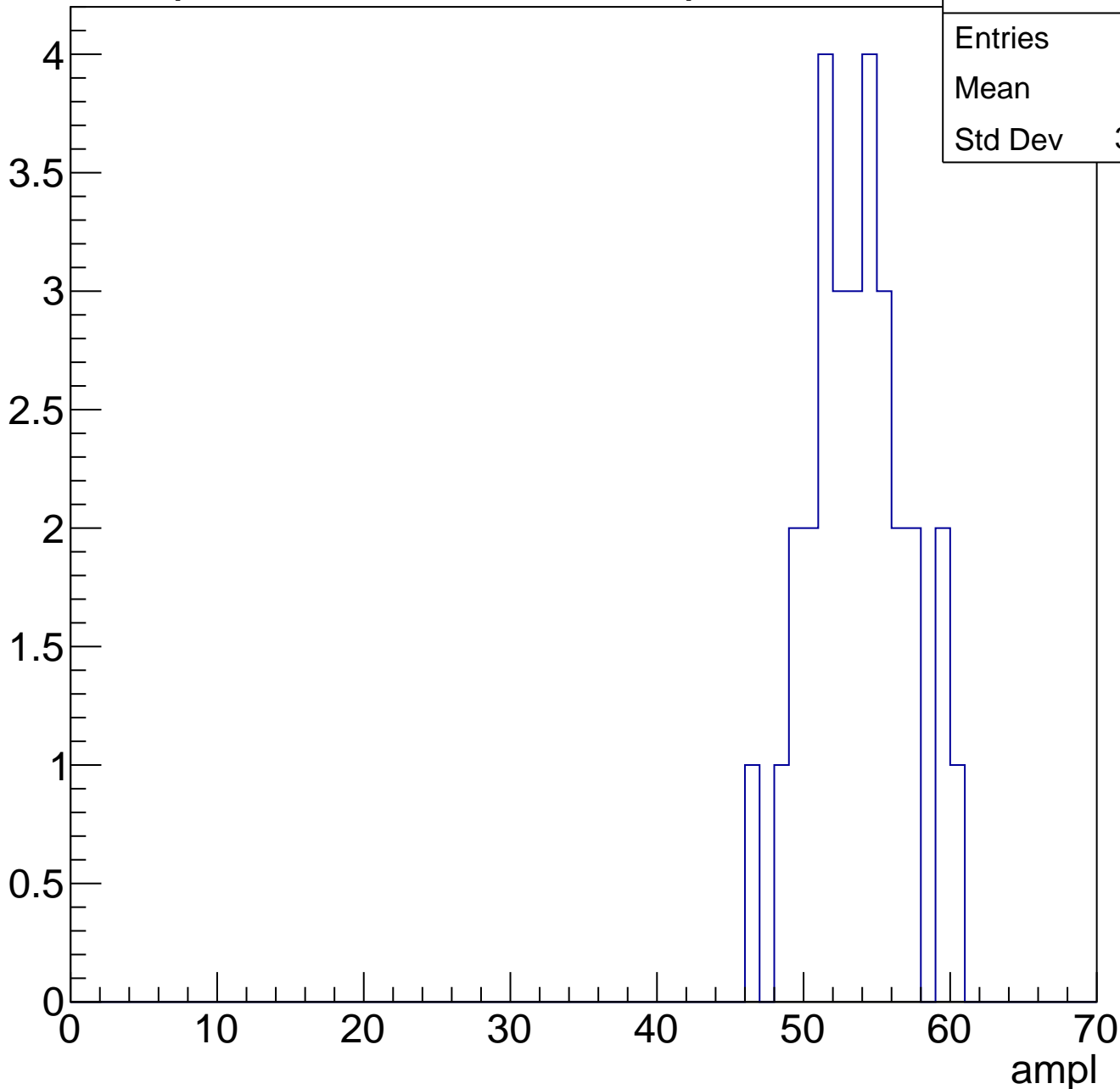
Entry



B1L103S, U14-ch109, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



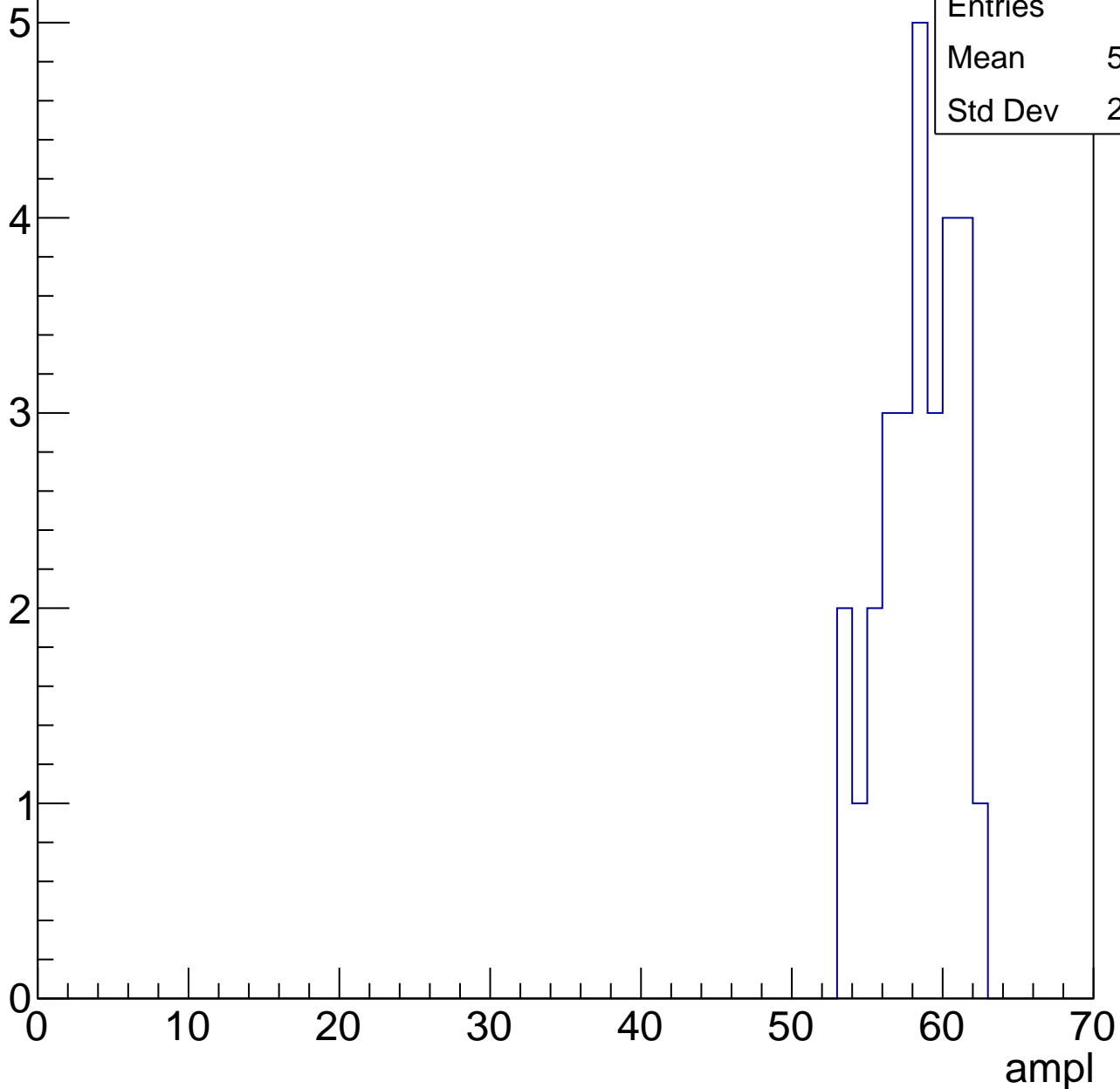
Entries	30
Mean	53.2
Std Dev	3.311

B1L103S, U14-ch109, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	28
Mean	57.93
Std Dev	2.463

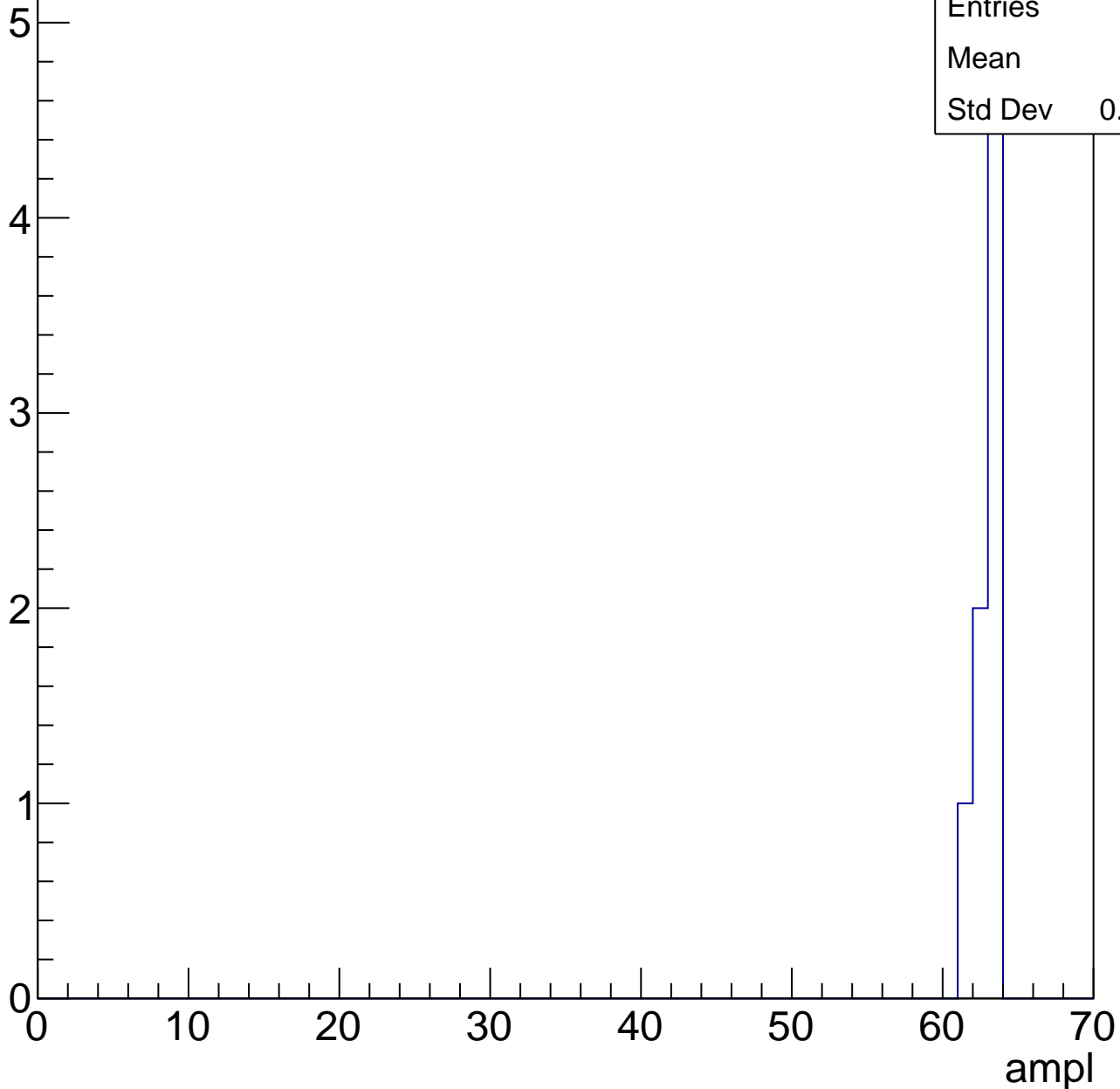


B1L103S, U14-ch109, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	8
Mean	62.5
Std Dev	0.7071

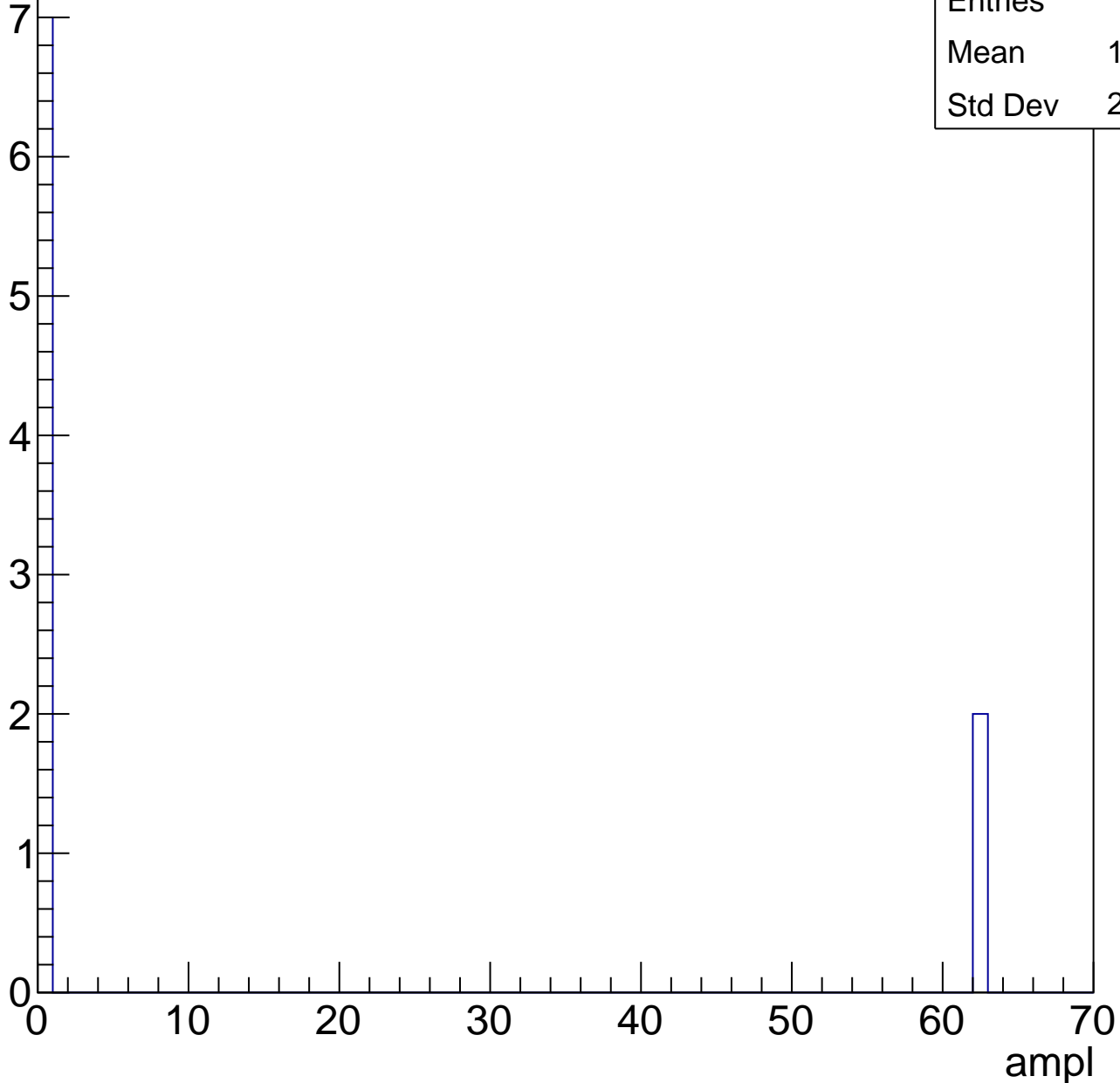


B1L103S, U14-ch109, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

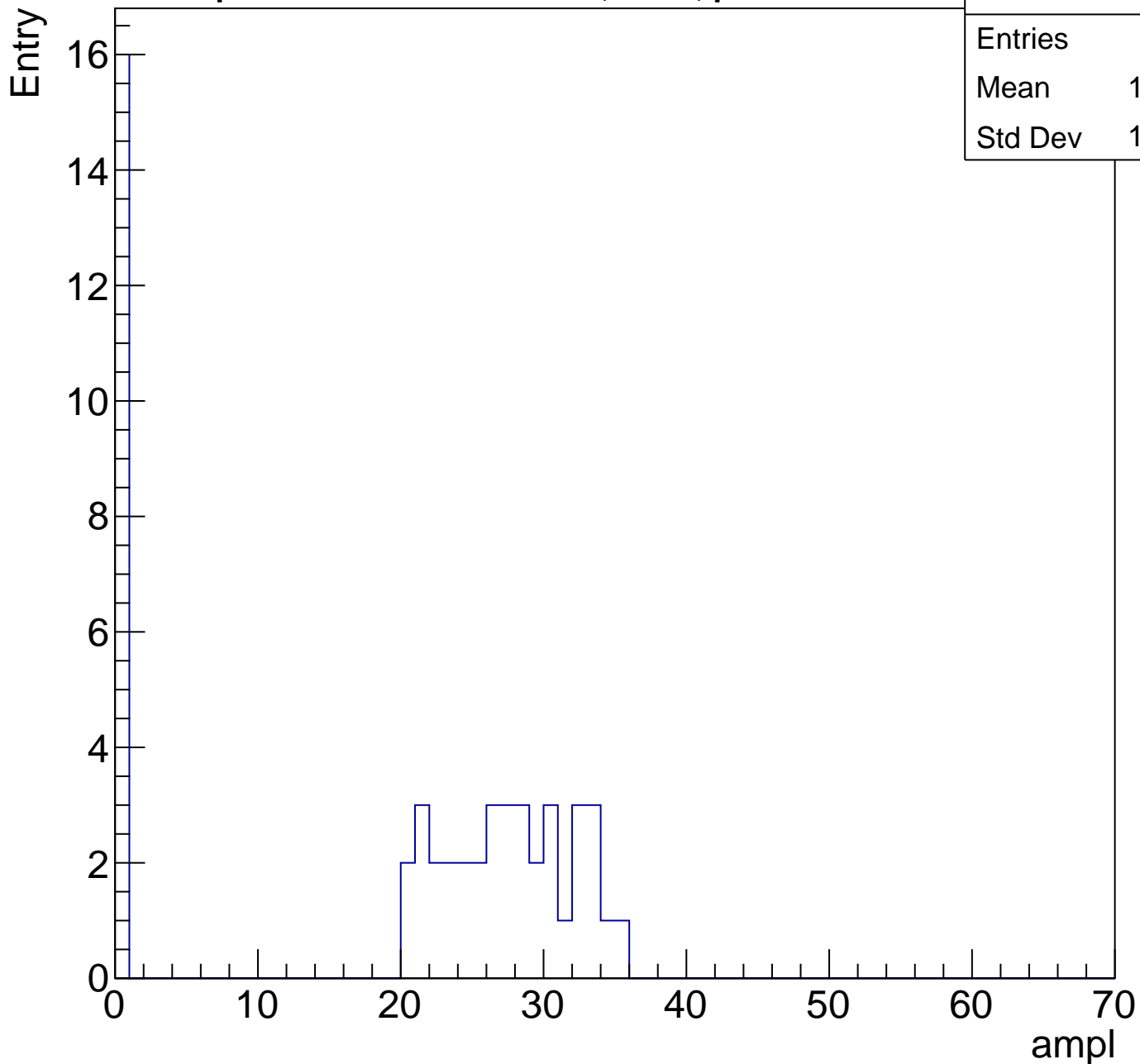
Entries	9
Mean	13.78
Std Dev	25.78



B1L103S, U14-ch110, adc0

calib_packv5_041523_1651.root, FC#0, port C2

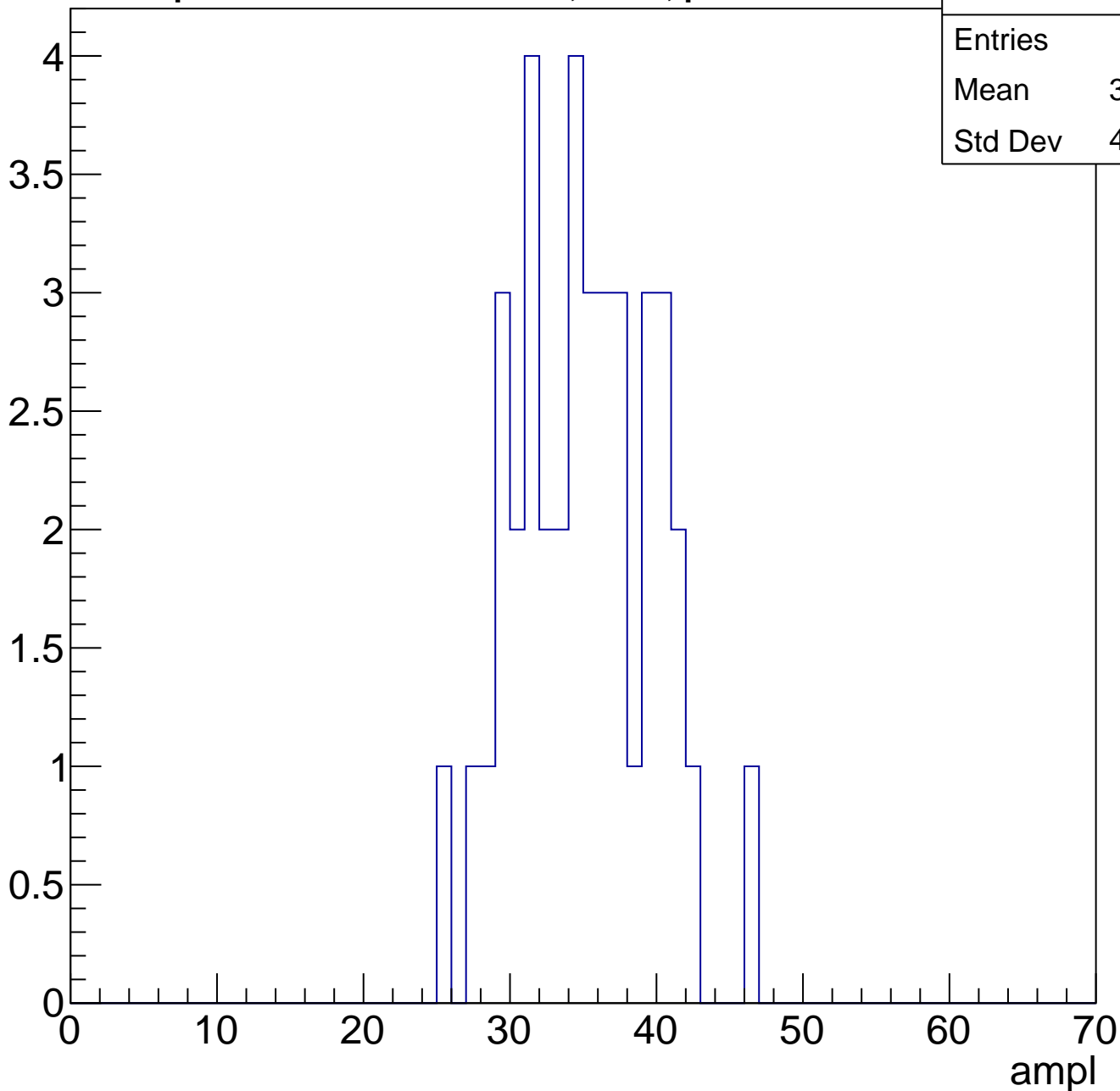
Entries	52
Mean	18.79
Std Dev	13.03



B1L103S, U14-ch110, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

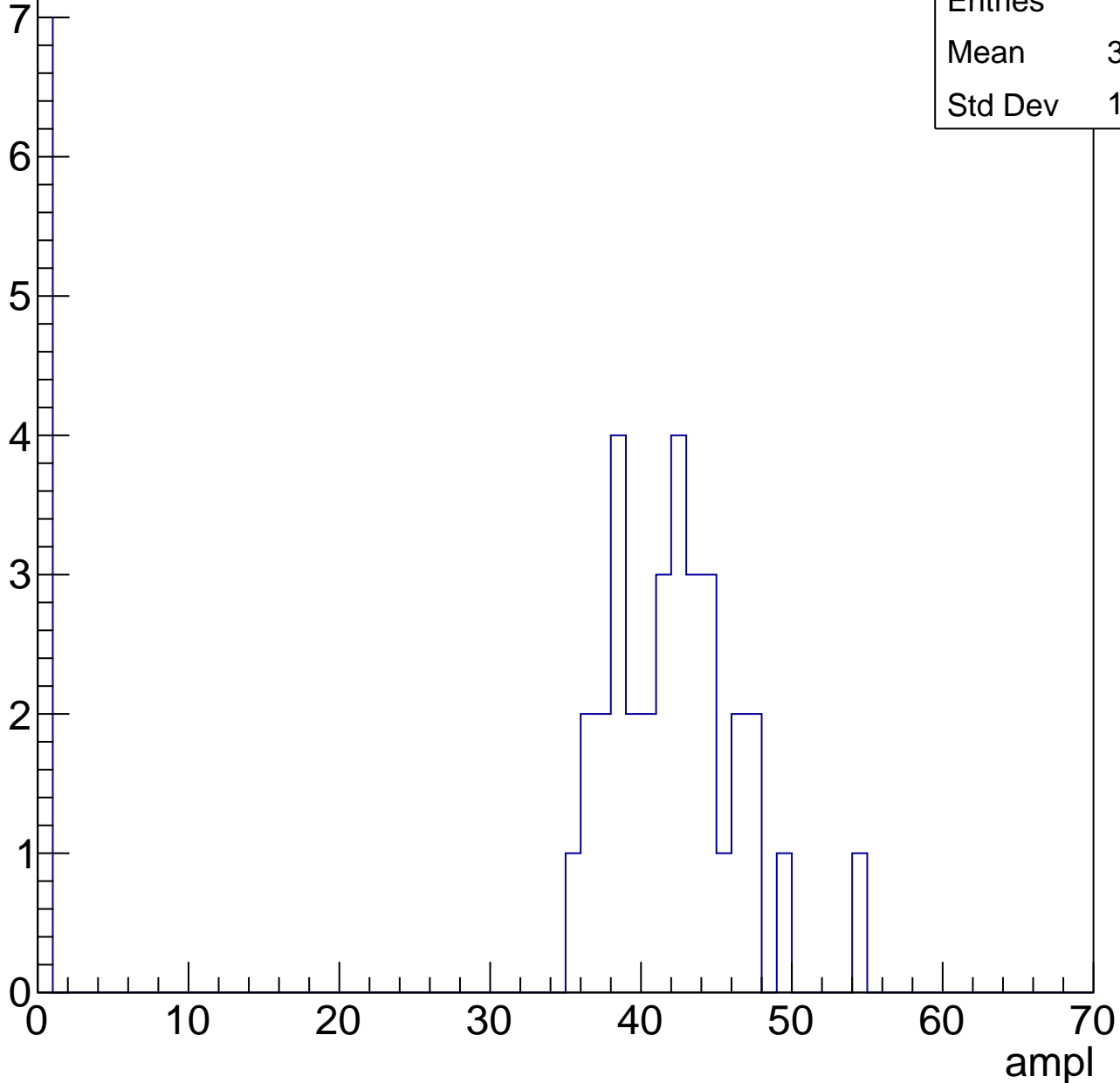


B1L103S, U14-ch110, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	34.42
Std Dev	16.29

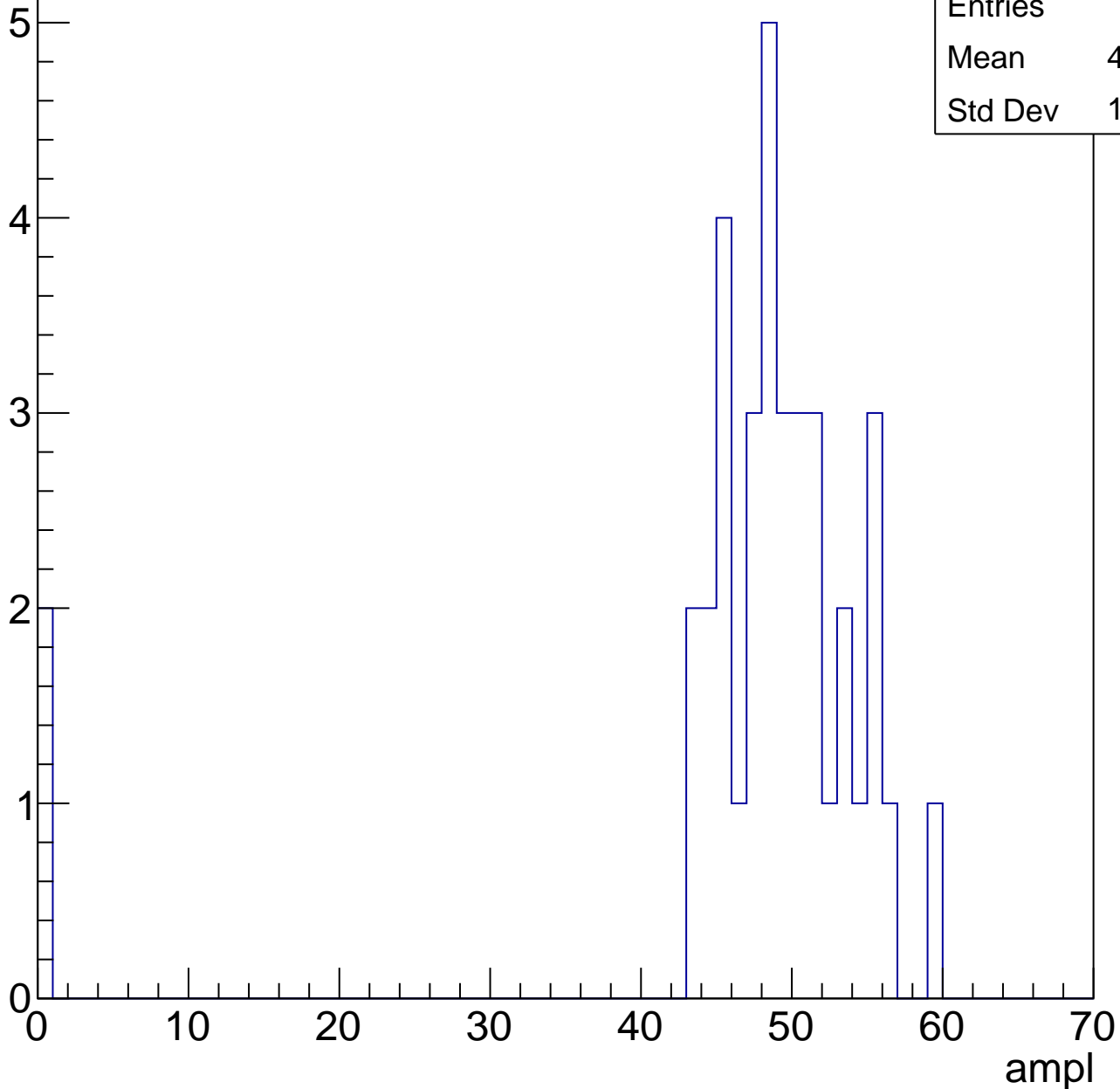


B1L103S, U14-ch110, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

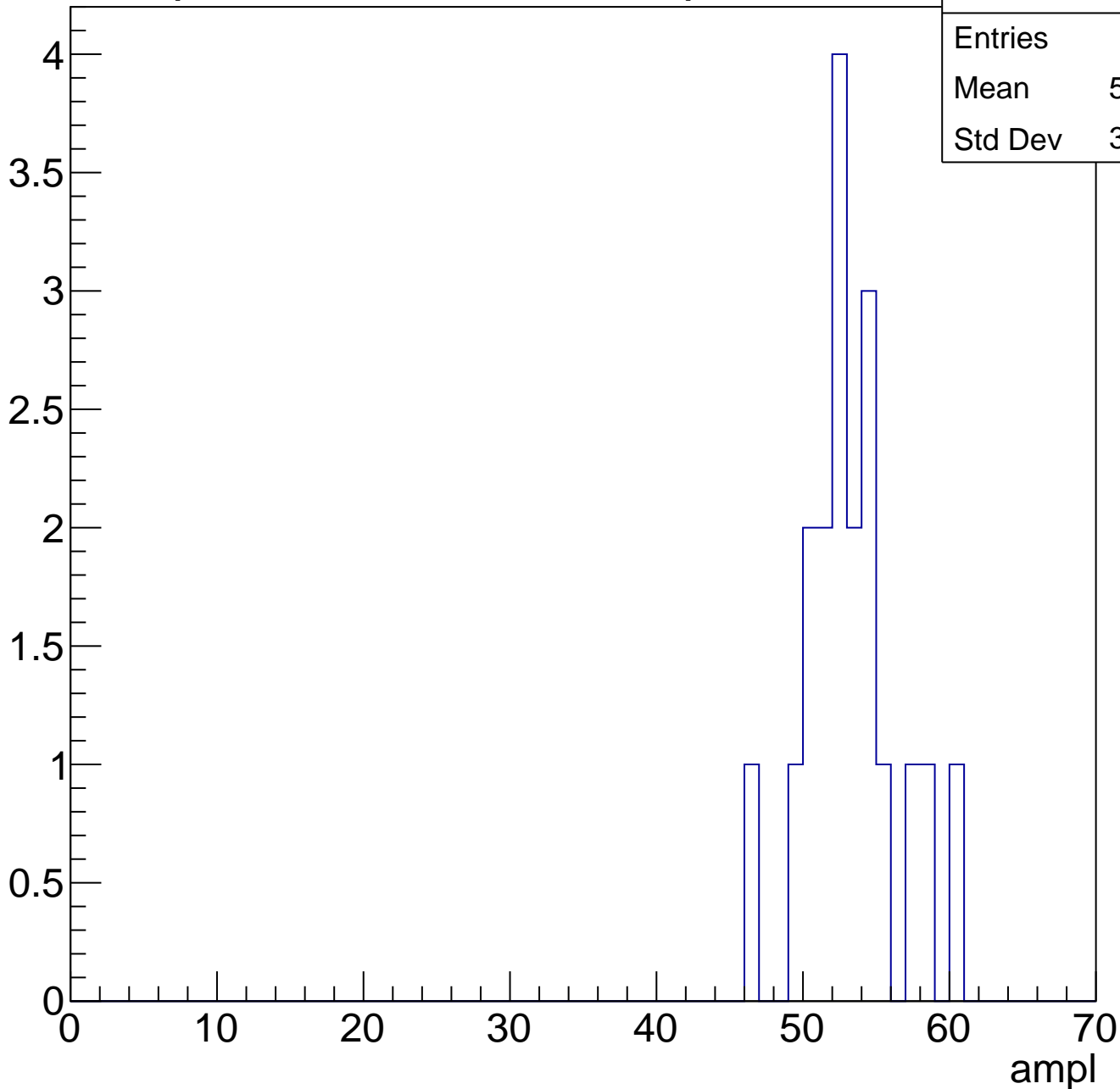
Entries	37
Mean	46.57
Std Dev	11.78



B1L103S, U14-ch110, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

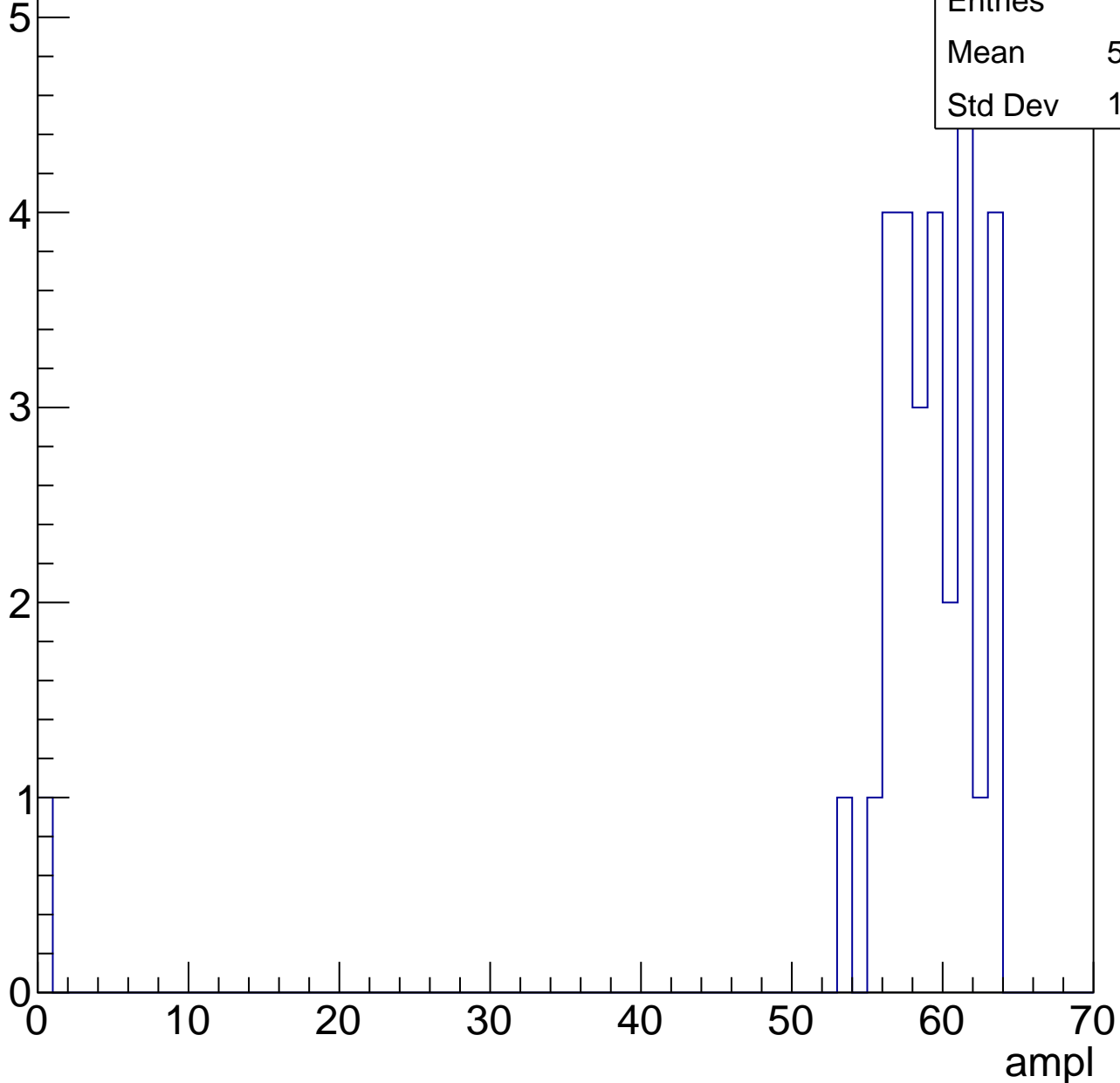


B1L103S, U14-ch110, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

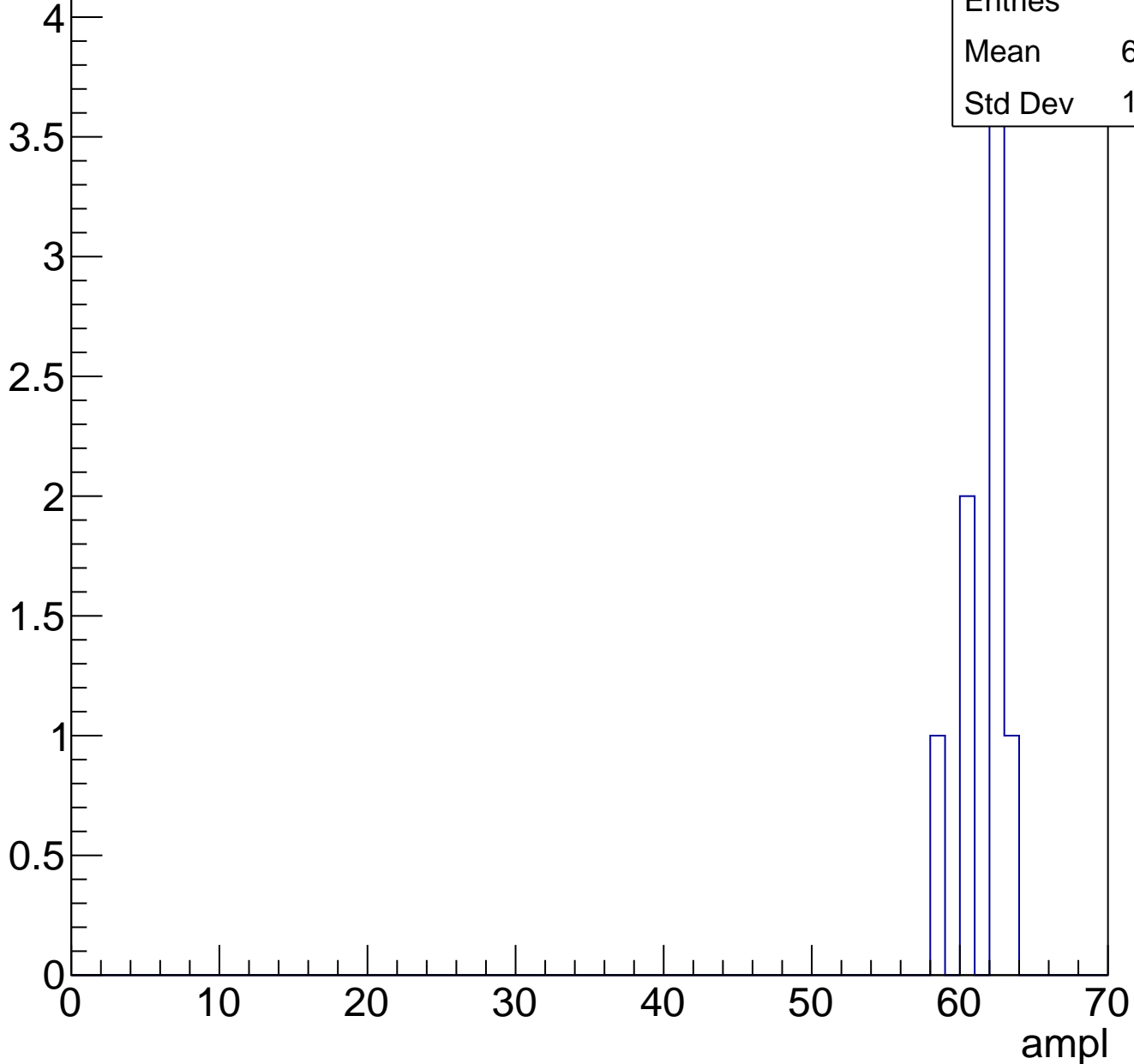
Entries	30
Mean	56.97
Std Dev	10.89



B1L103S, U14-ch110, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch110, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

Entries	10
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Mean	0
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Std Dev	0
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8

6

4

2

0

0

10

20

30

40

50

60

70

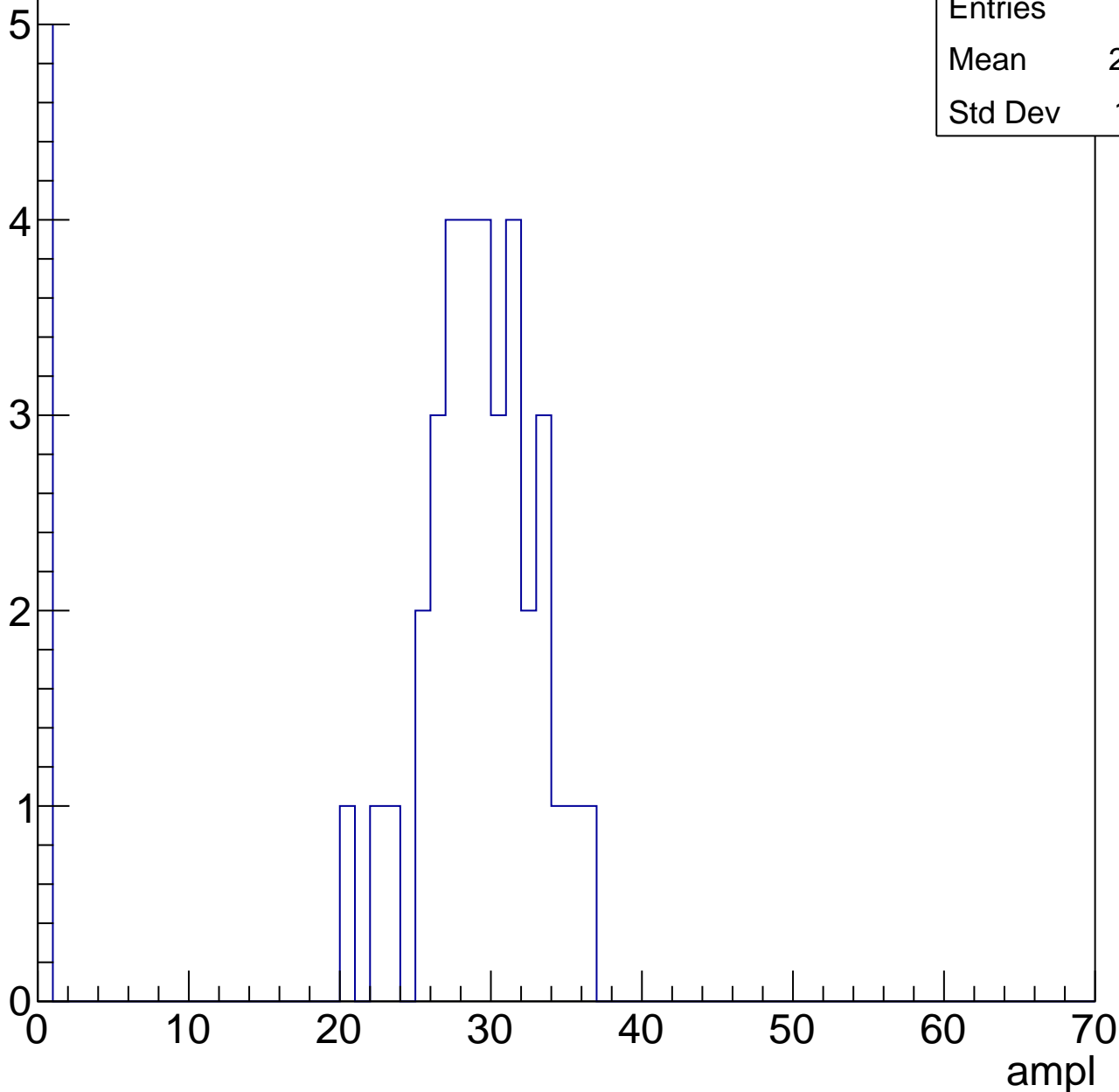
ampl

B1L103S, U14-ch111, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

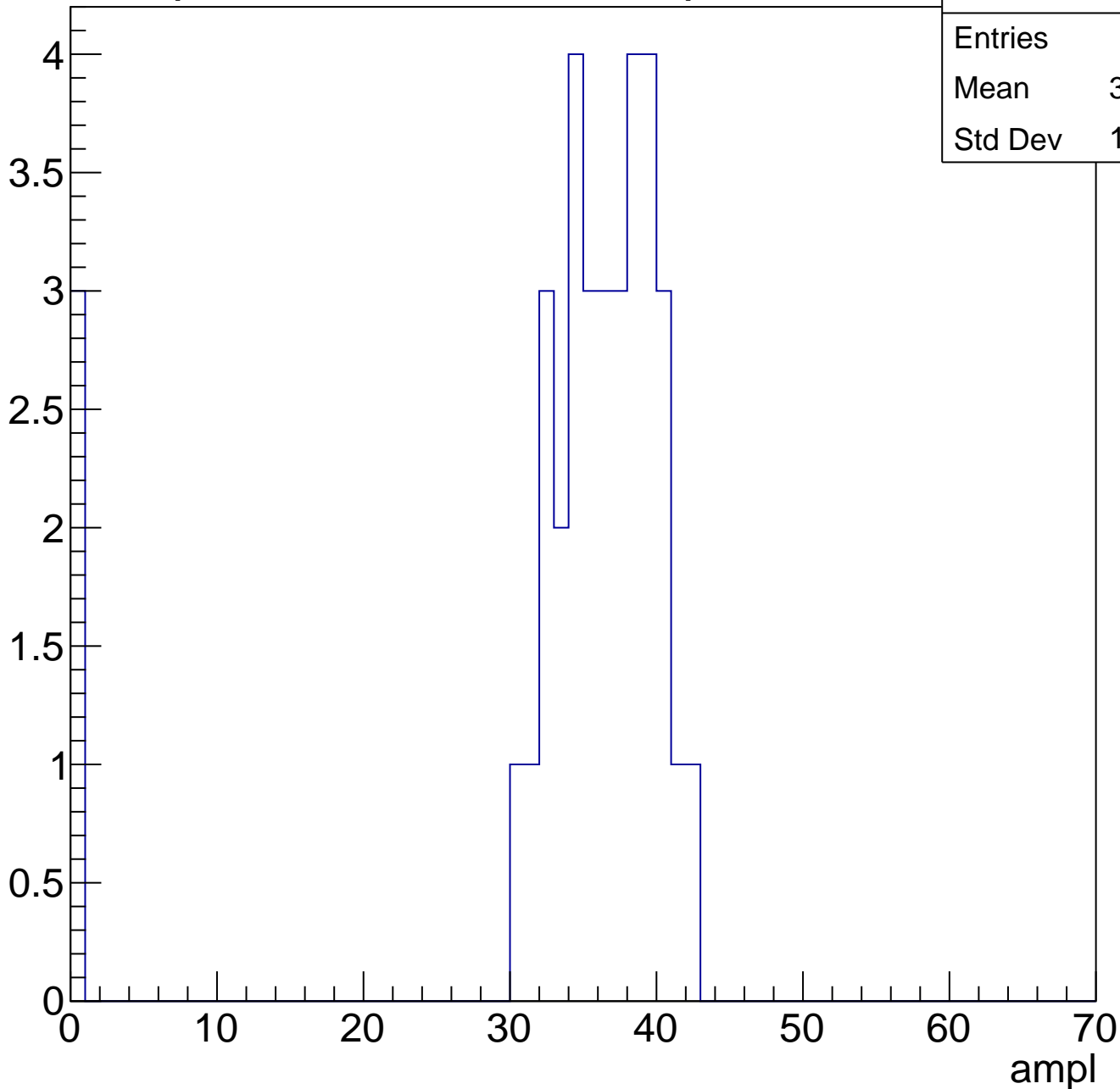
Entries	40
Mean	25.27
Std Dev	10.11



B1L103S, U14-ch111, adc1

calib_packv5_041523_1651.root, FC#0, port C2

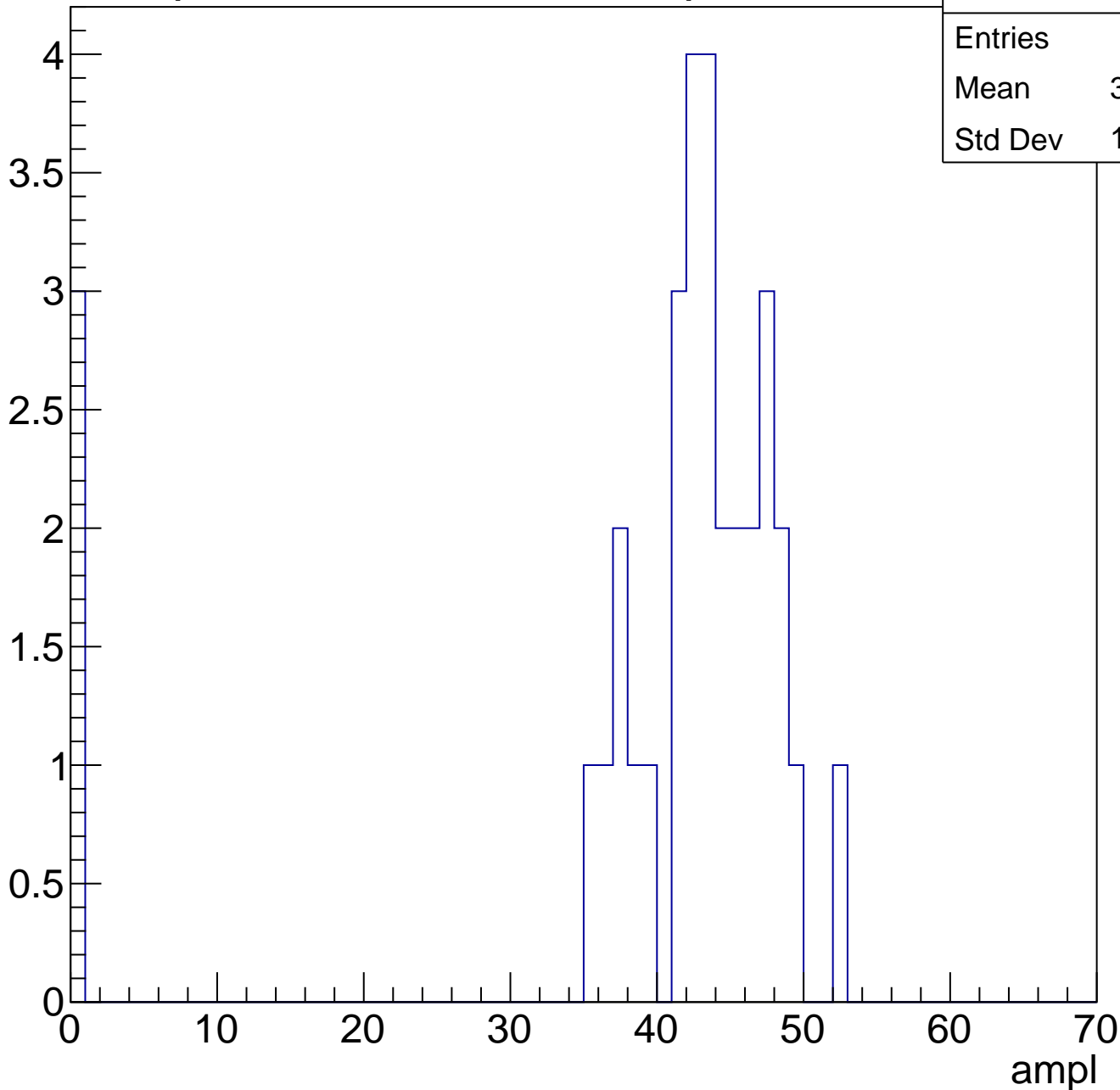
Entry



B1L103S, U14-ch111, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch111, adc3

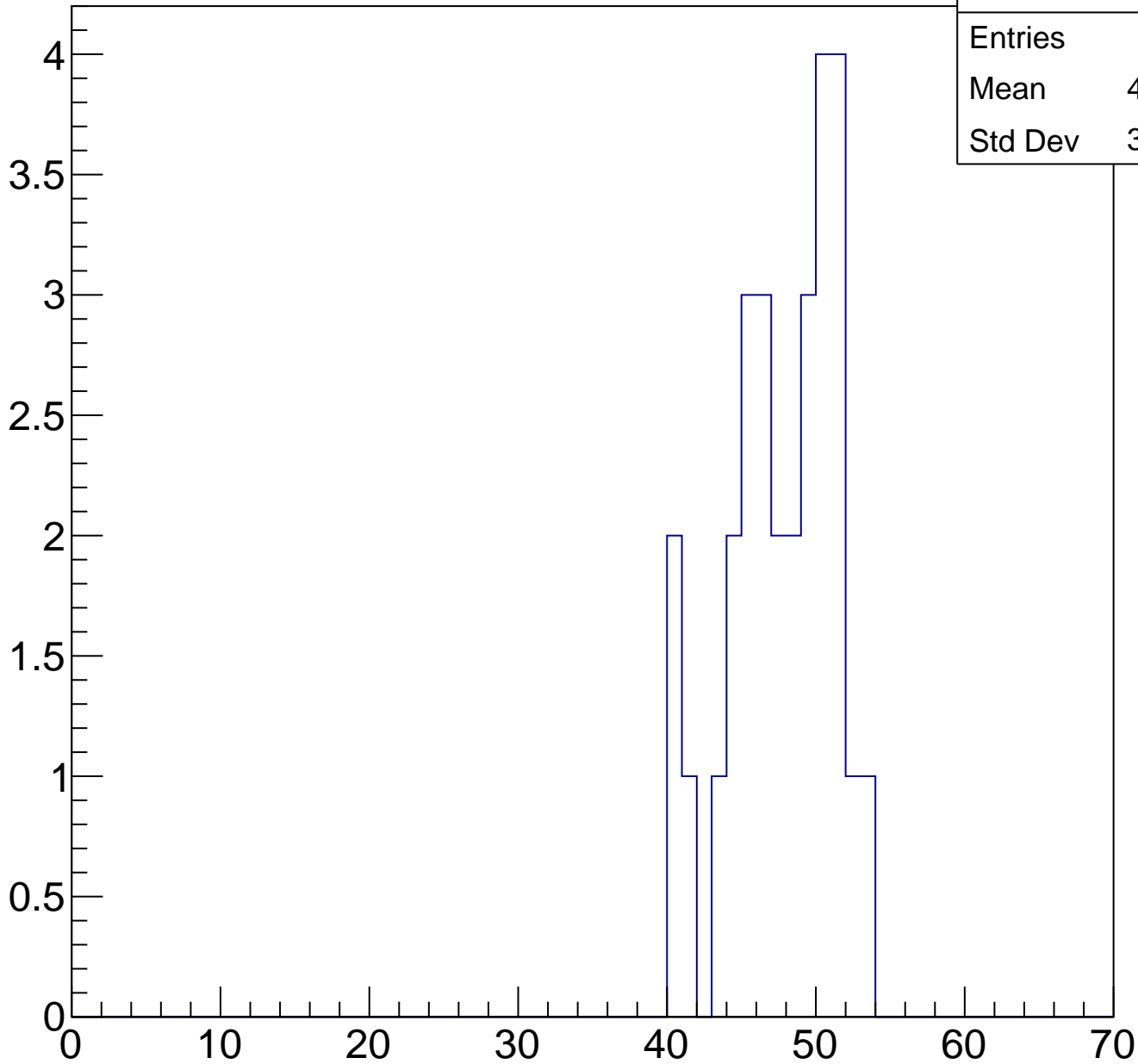
calib_packv5_041523_1651.root, FC#0, port C2

Entry

4
3.5
3
2.5
2
1.5
1
0.5
0

Entries	29
Mean	47.28
Std Dev	3.503

ampl

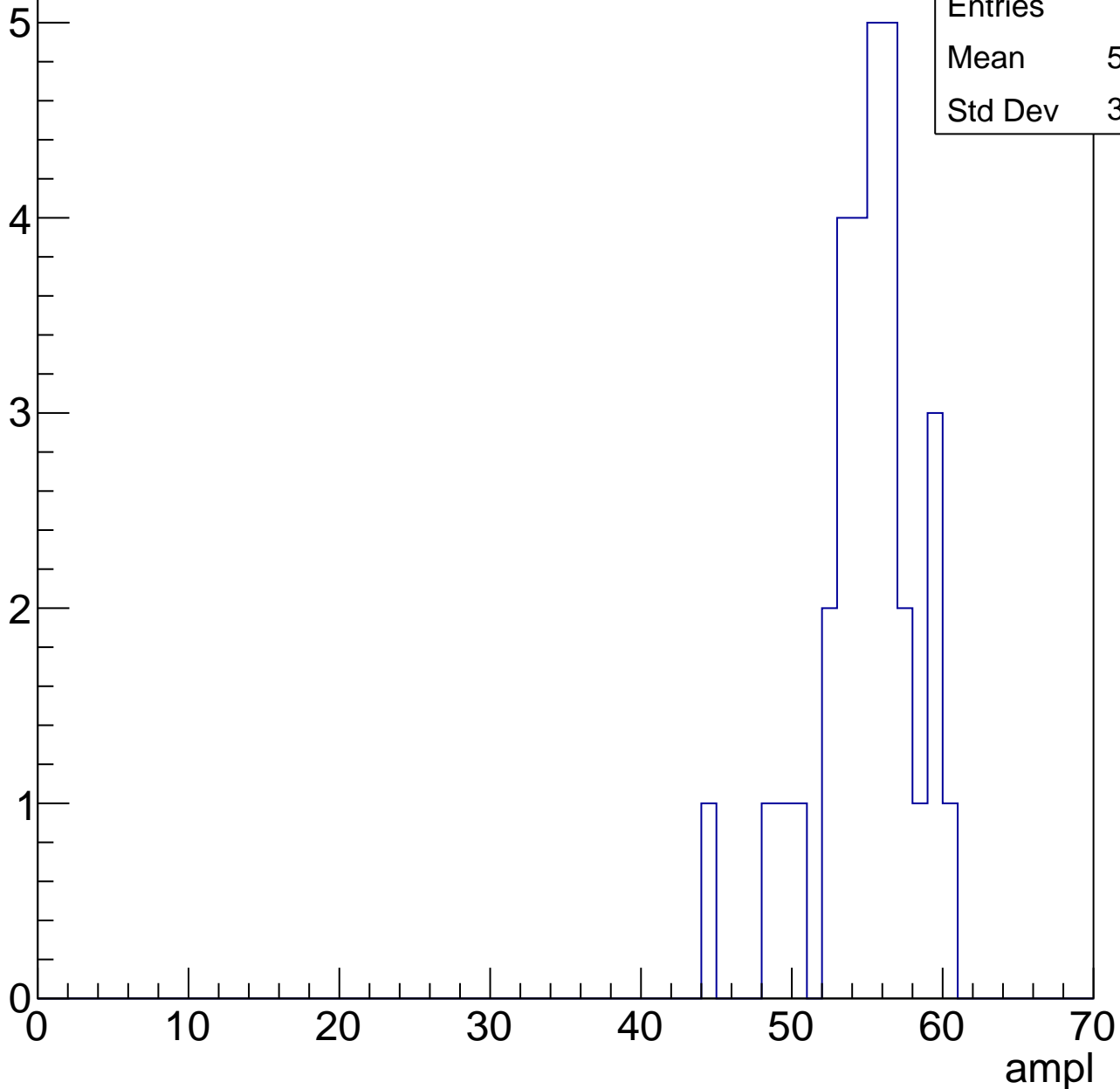


B1L103S, U14-ch111, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	31
Mean	54.42
Std Dev	3.377

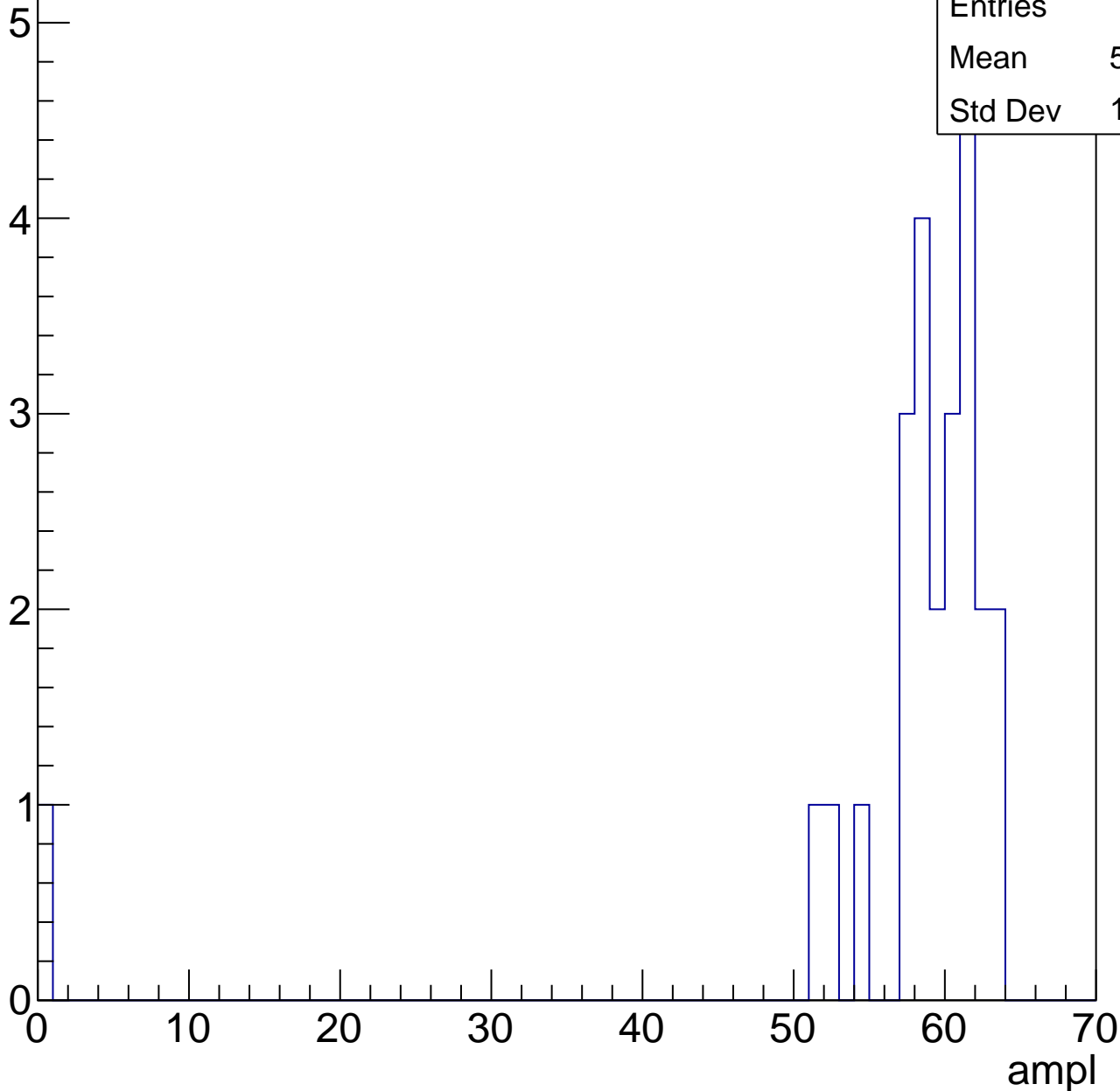


B1L103S, U14-ch111, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	25
Mean	56.52
Std Dev	11.92



B1L103S, U14-ch111, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

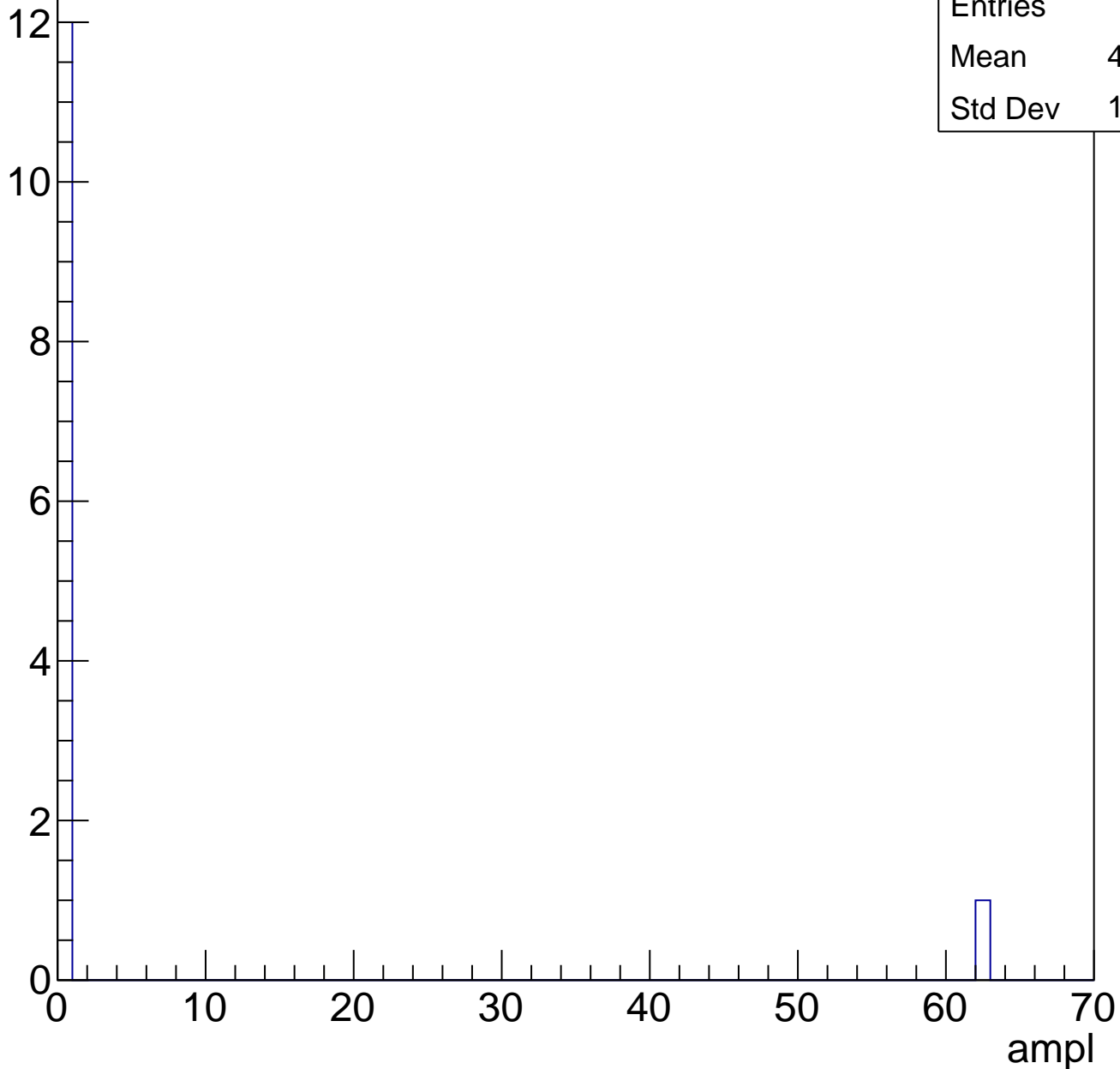


B1L103S, U14-ch111, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	13
Mean	4.769
Std Dev	16.52

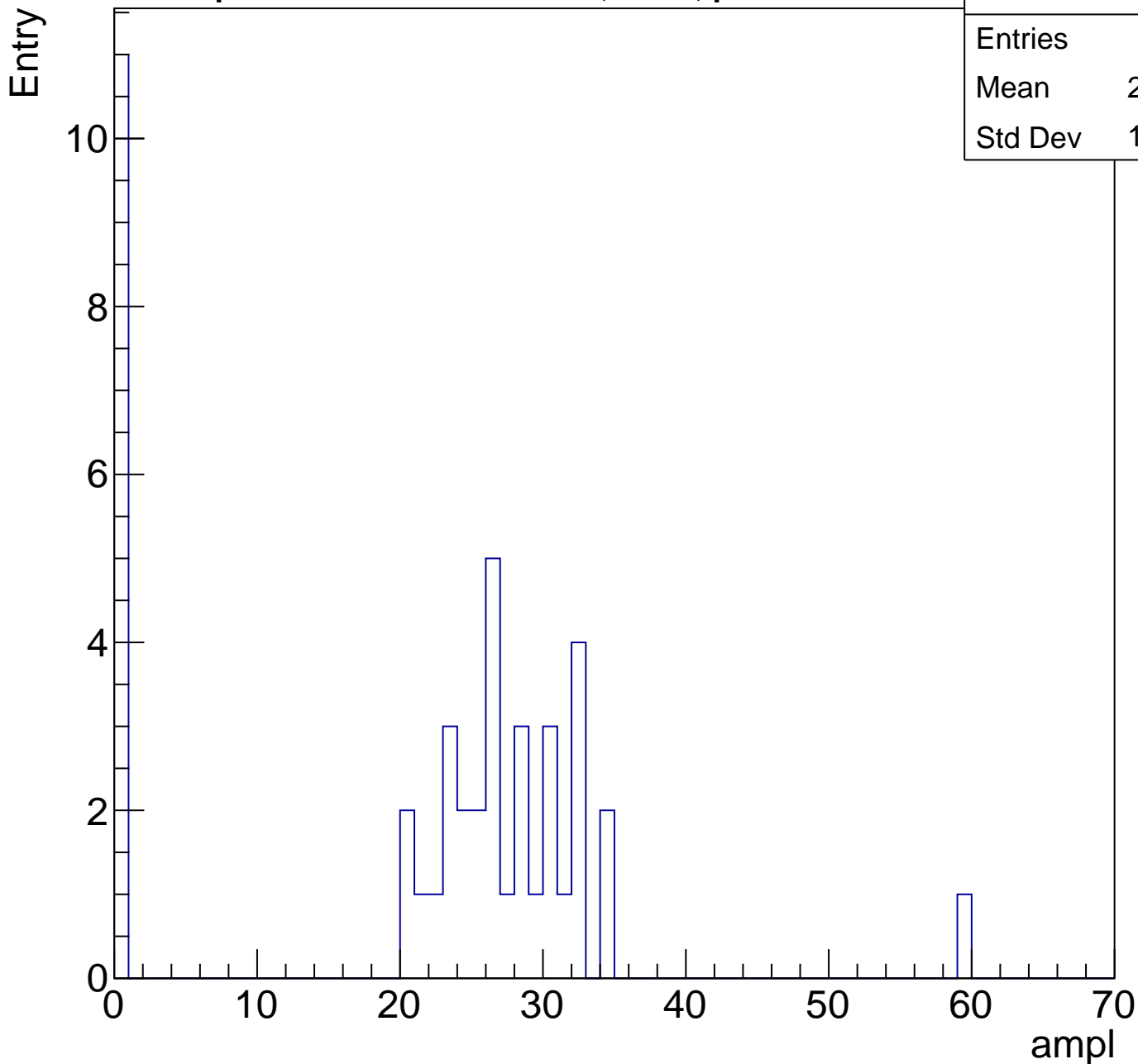
Entry



B1L103S, U14-ch112, adc0

calib_packv5_041523_1651.root, FC#0, port C2

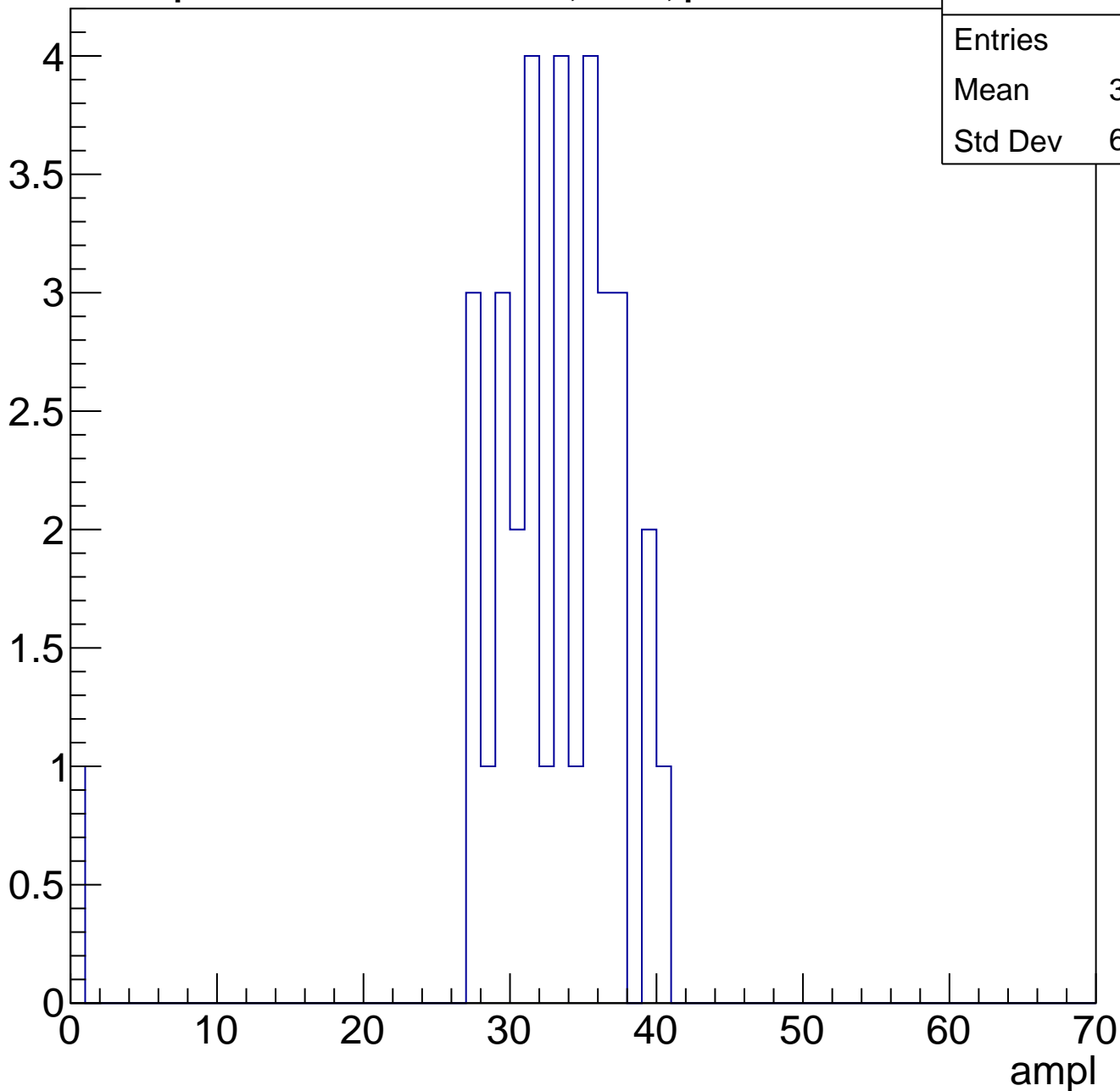
Entries	43
Mean	20.84
Std Dev	13.55



B1L103S, U14-ch112, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry



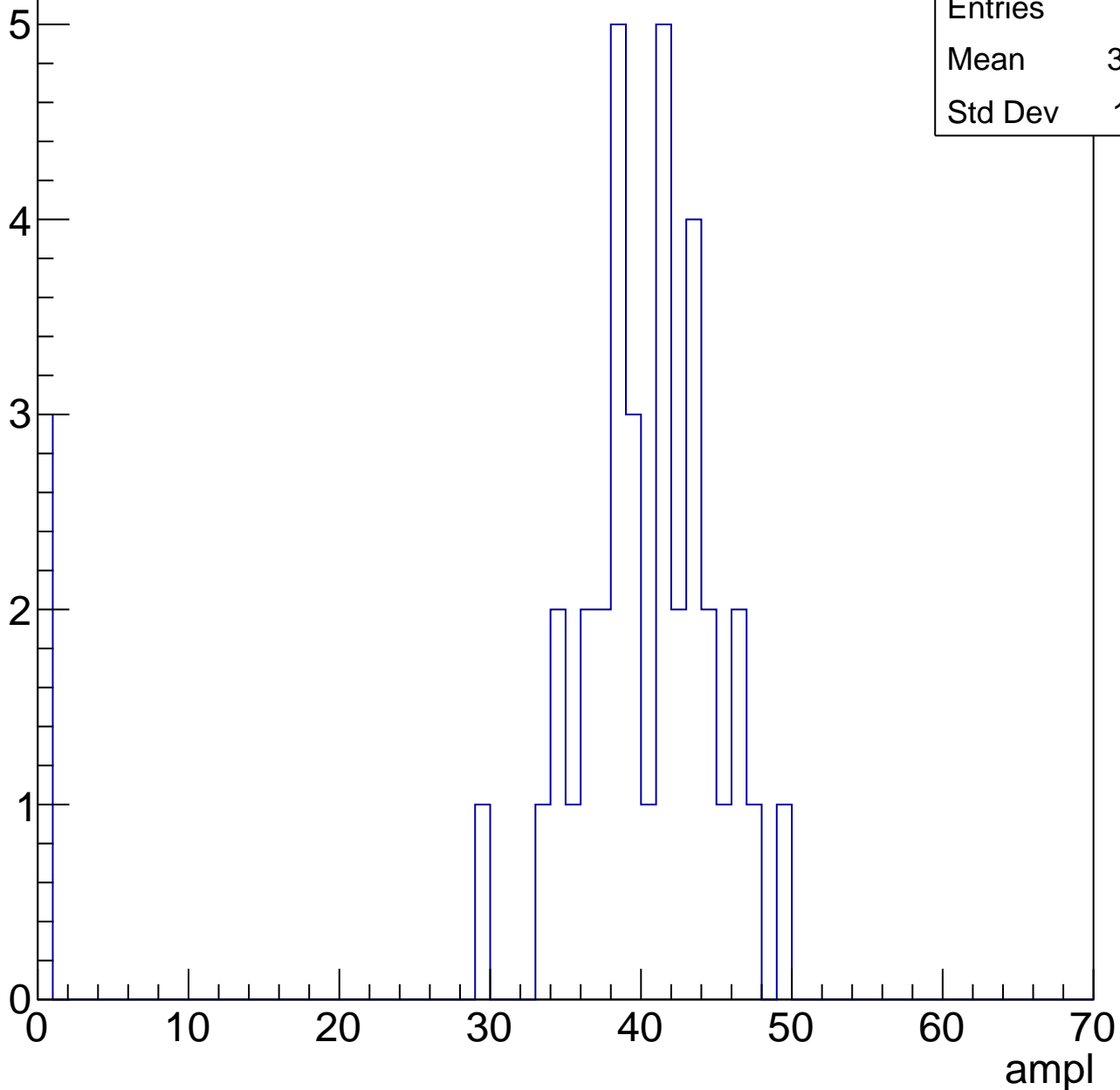
Entries	33
Mean	31.97
Std Dev	6.704

B1L103S, U14-ch112, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

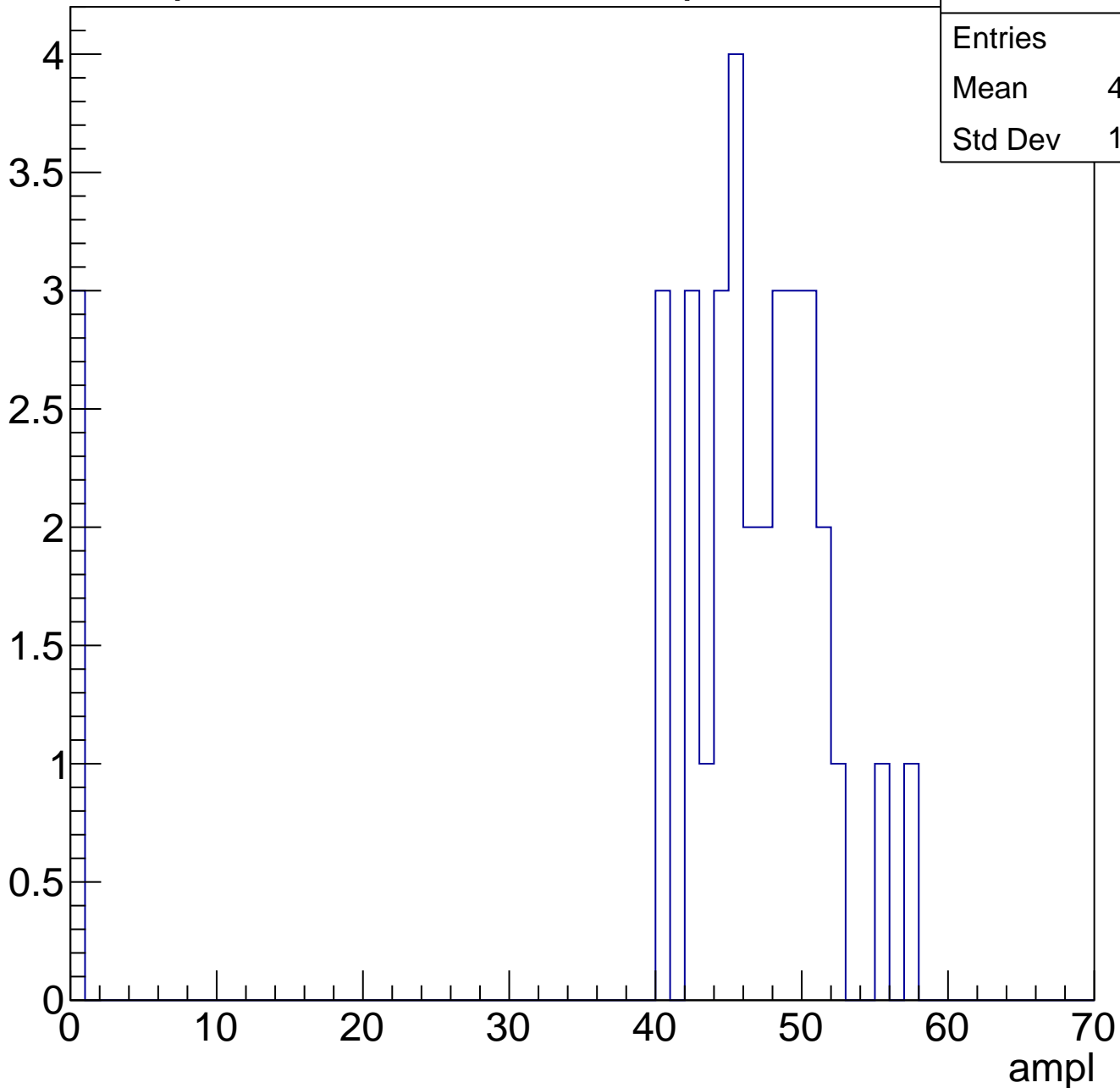
Entries	39
Mean	36.92
Std Dev	11.41



B1L103S, U14-ch112, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	35
Mean	42.69
Std Dev	13.65

B1L103S, U14-ch112, adc4

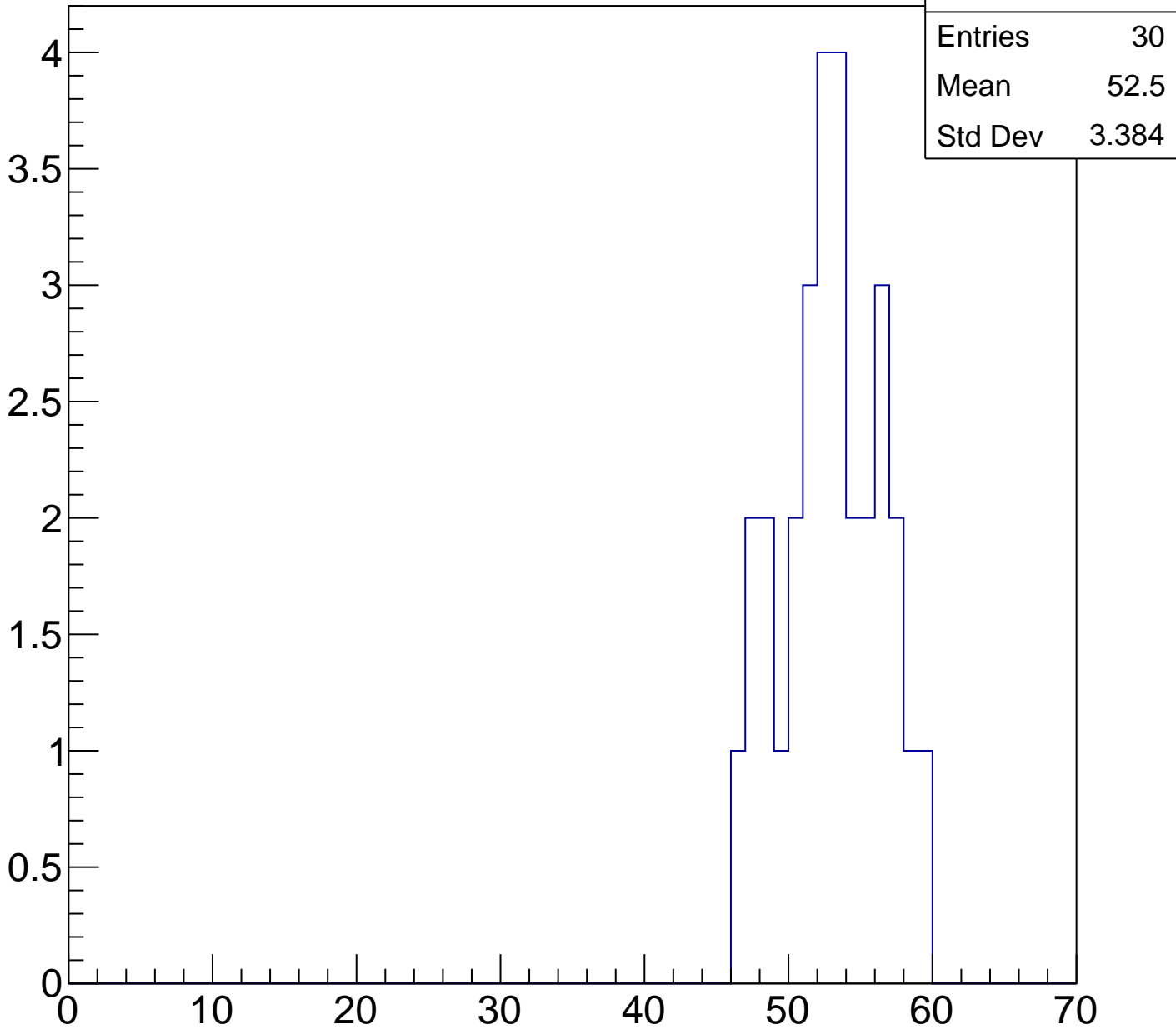
calib_packv5_041523_1651.root, FC#0, port C2

Entry

4
3.5
3
2.5
2
1.5
1
0.5
0

Entries	30
Mean	52.5
Std Dev	3.384

ampl

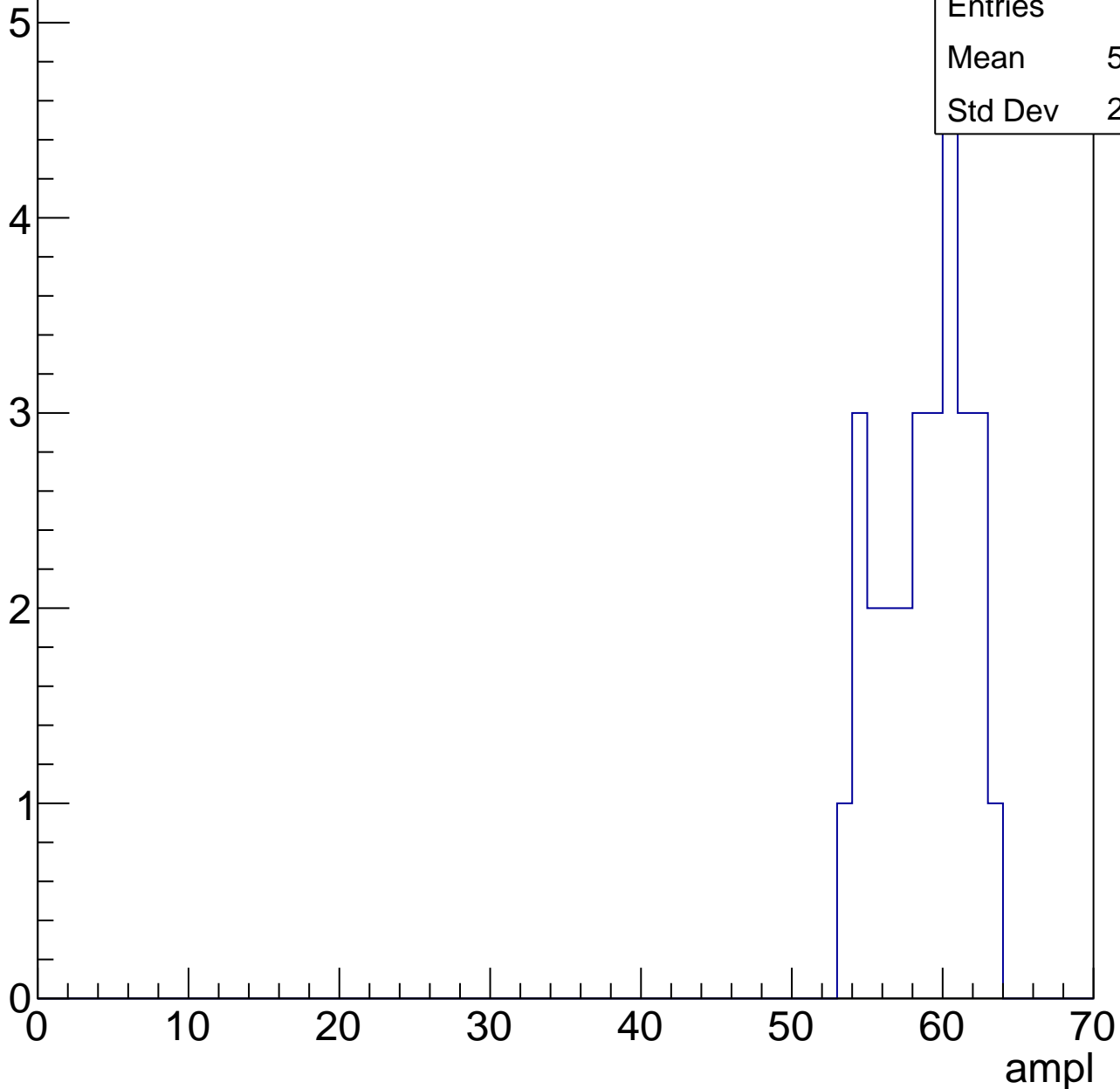


B1L103S, U14-ch112, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

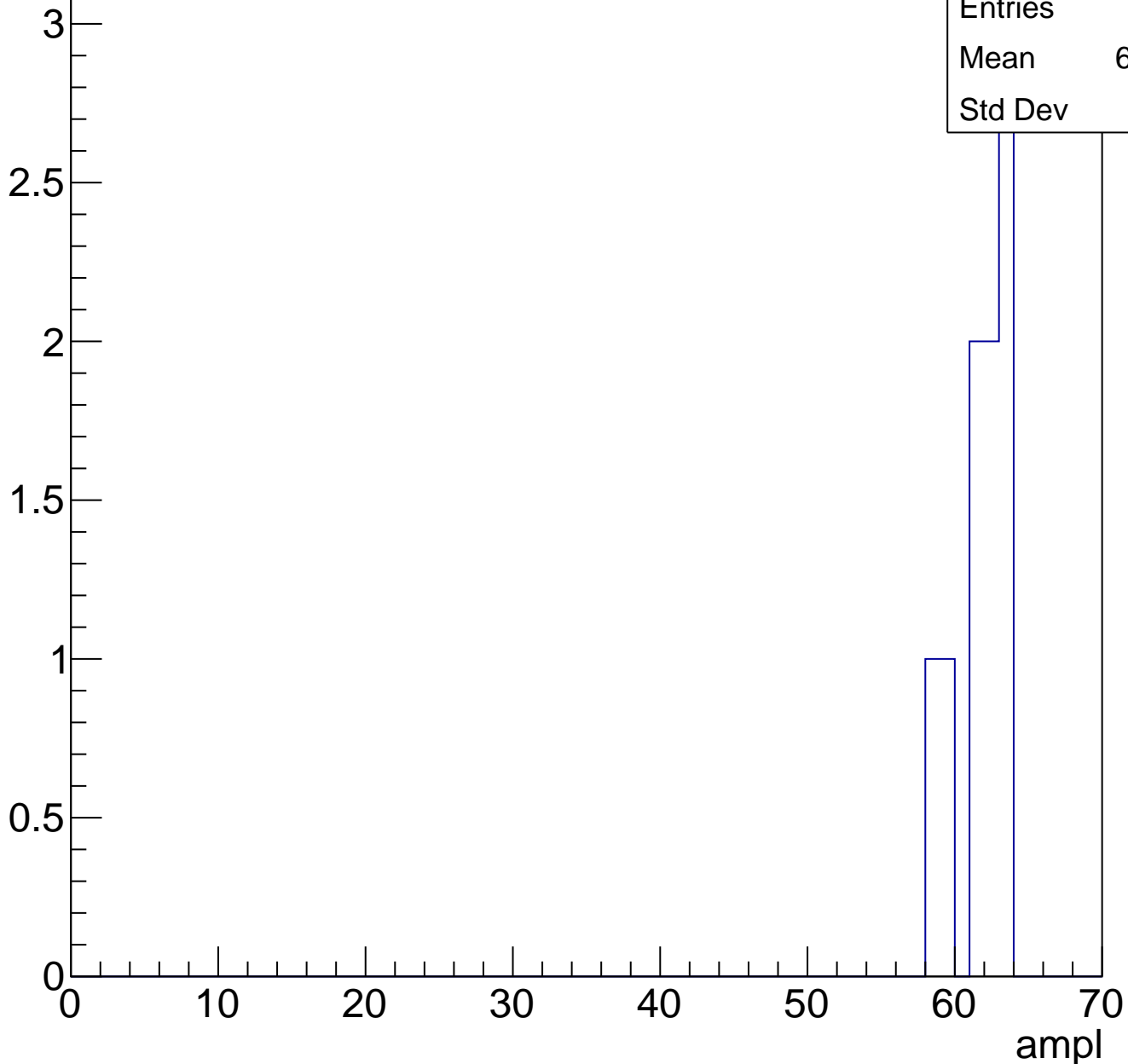
Entries	28
Mean	58.36
Std Dev	2.806



B1L103S, U14-ch112, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

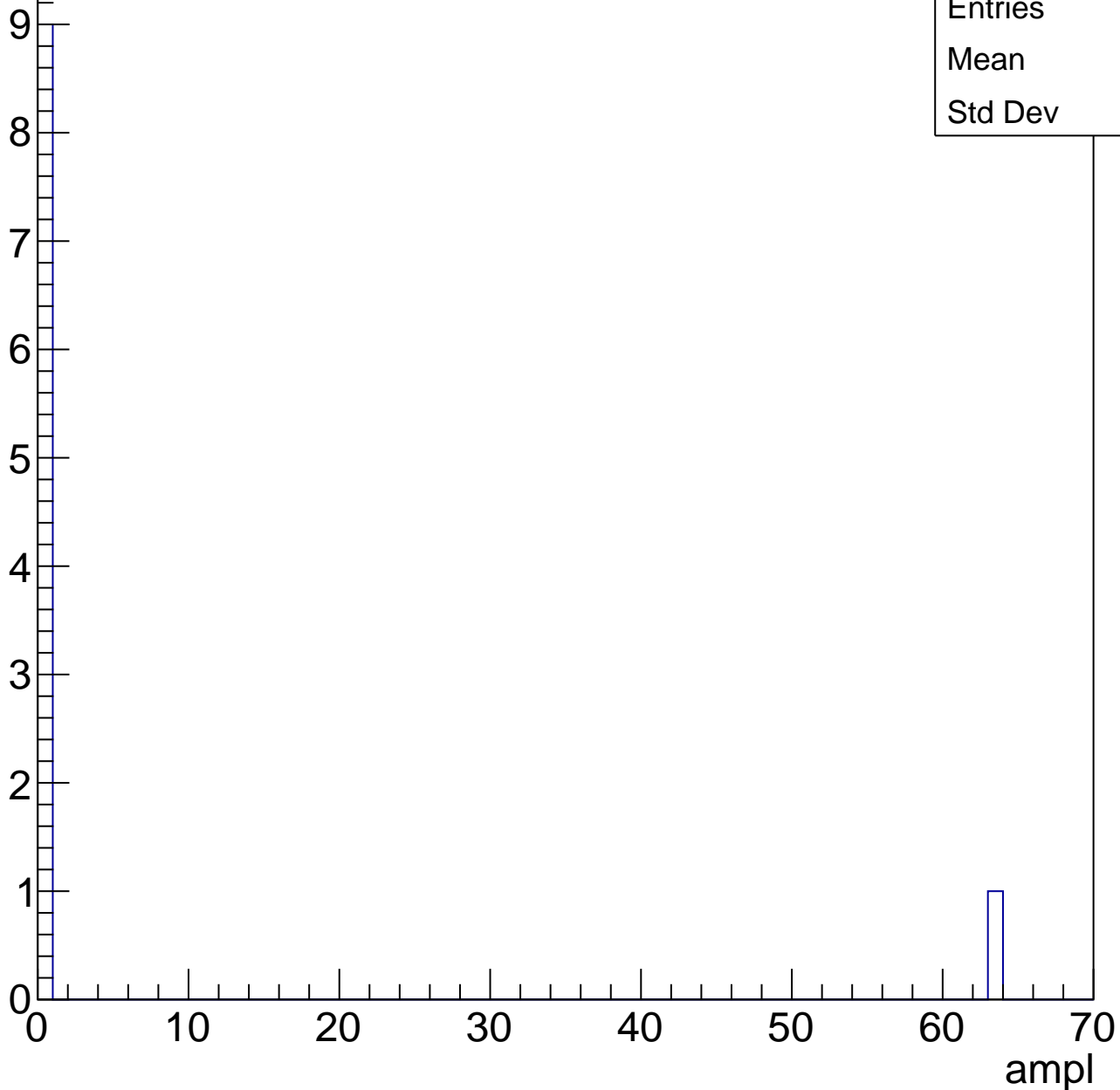


B1L103S, U14-ch112, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

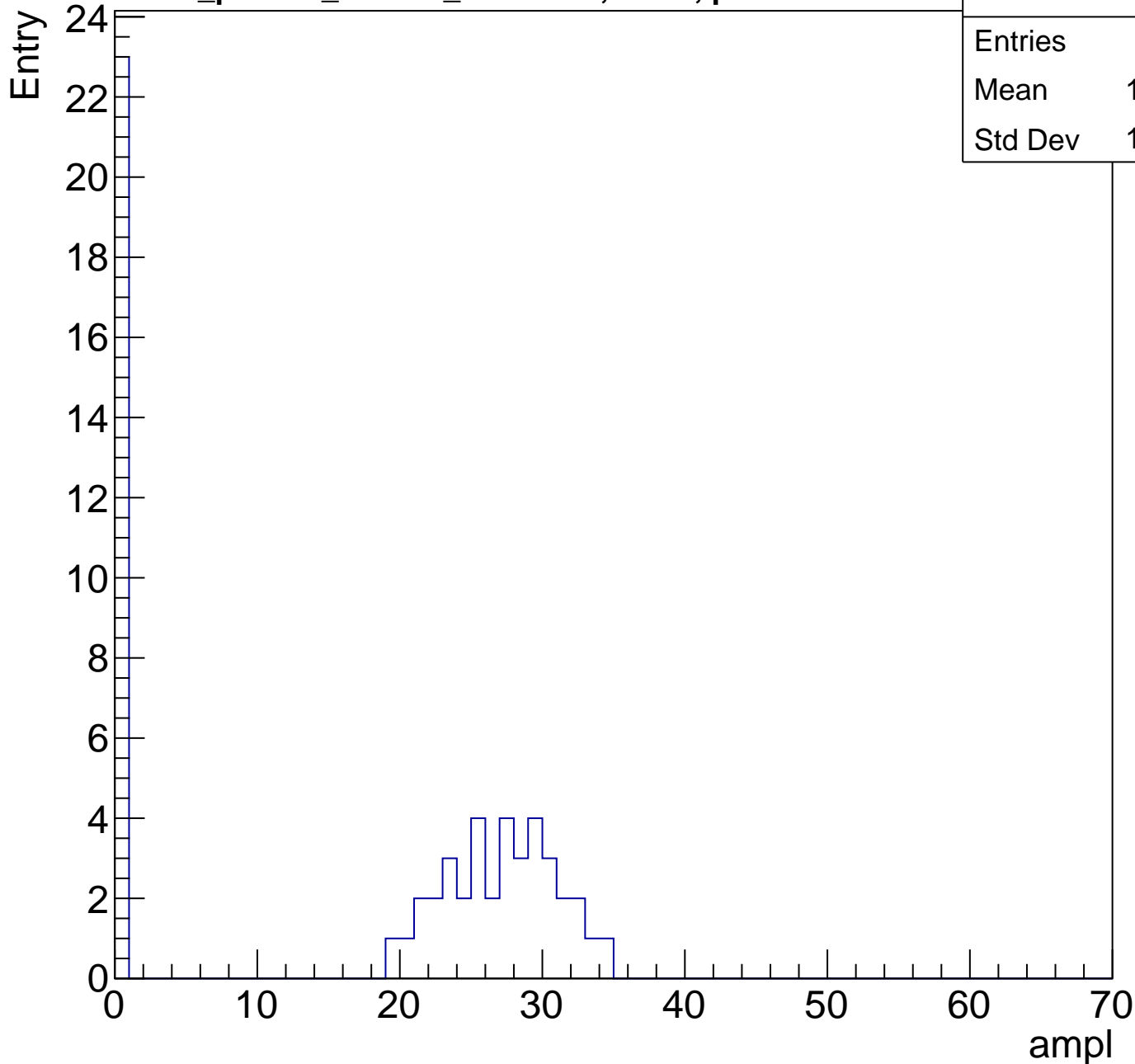
Entries	10
Mean	6.3
Std Dev	18.9



B1L103S, U14-ch113, adc0

calib_packv5_041523_1651.root, FC#0, port C2

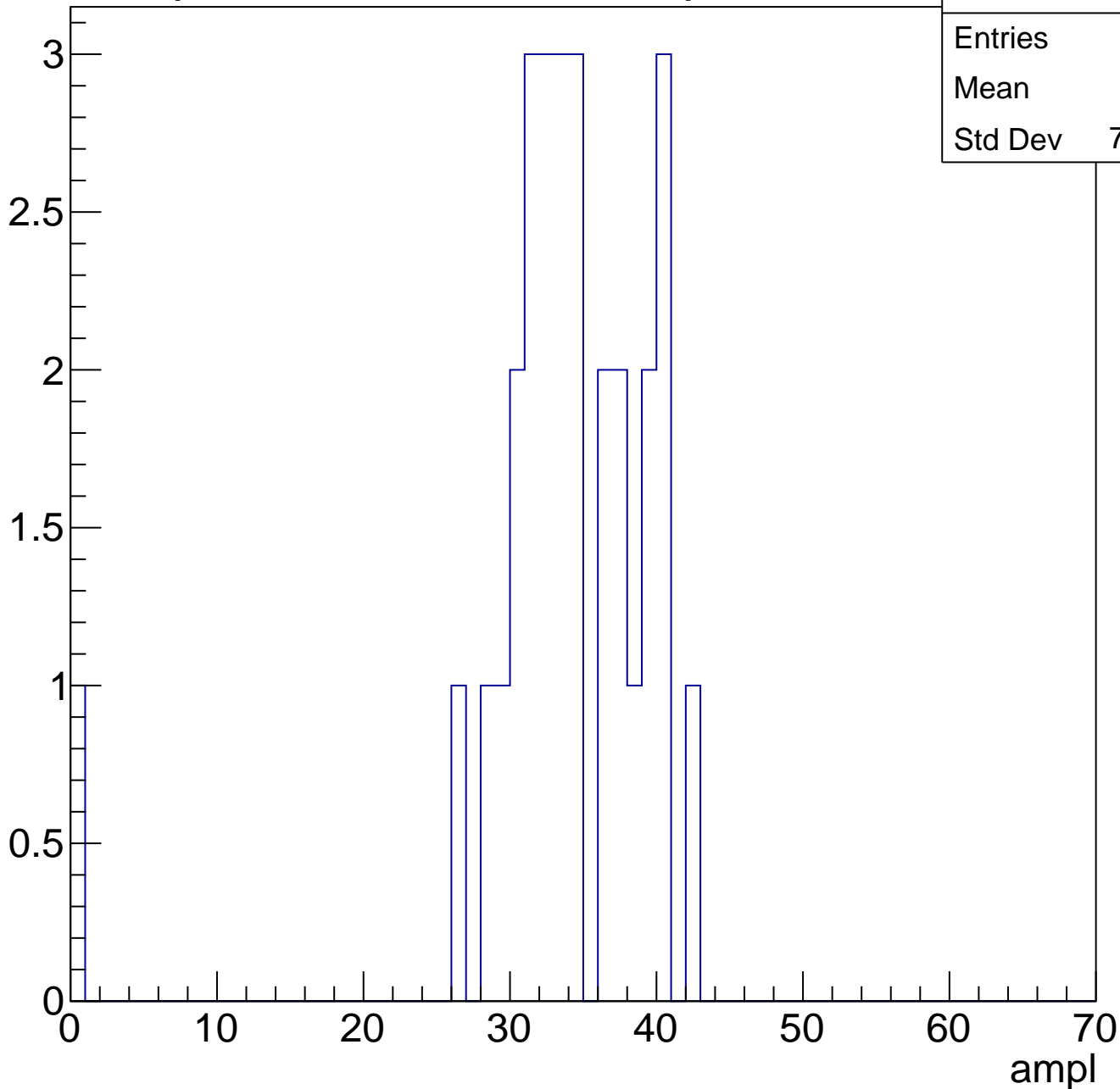
Entries	60
Mean	16.42
Std Dev	13.28



B1L103S, U14-ch113, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry



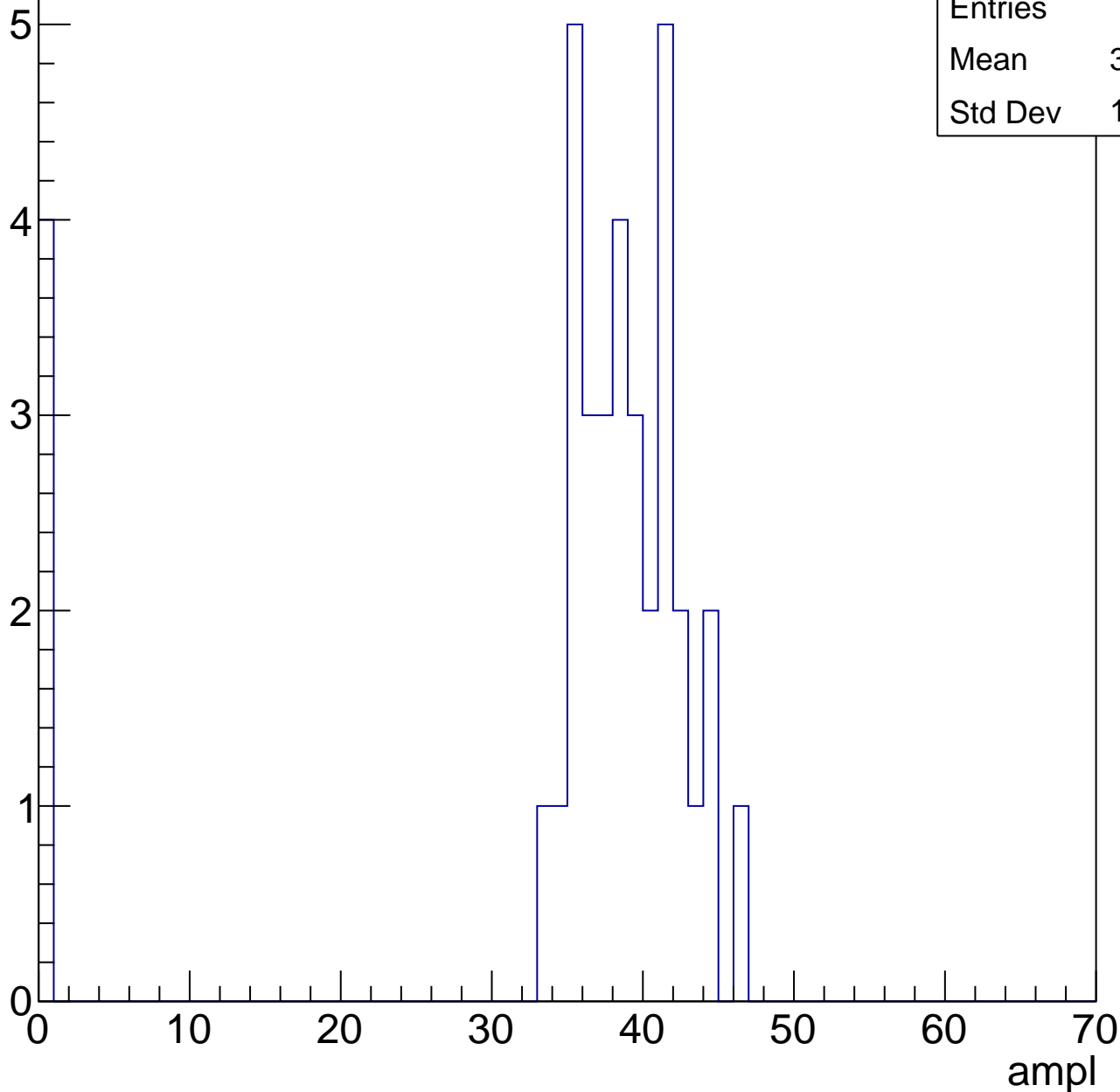
Entries	29
Mean	33
Std Dev	7.405

B1L103S, U14-ch113, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	37
Mean	34.49
Std Dev	12.38

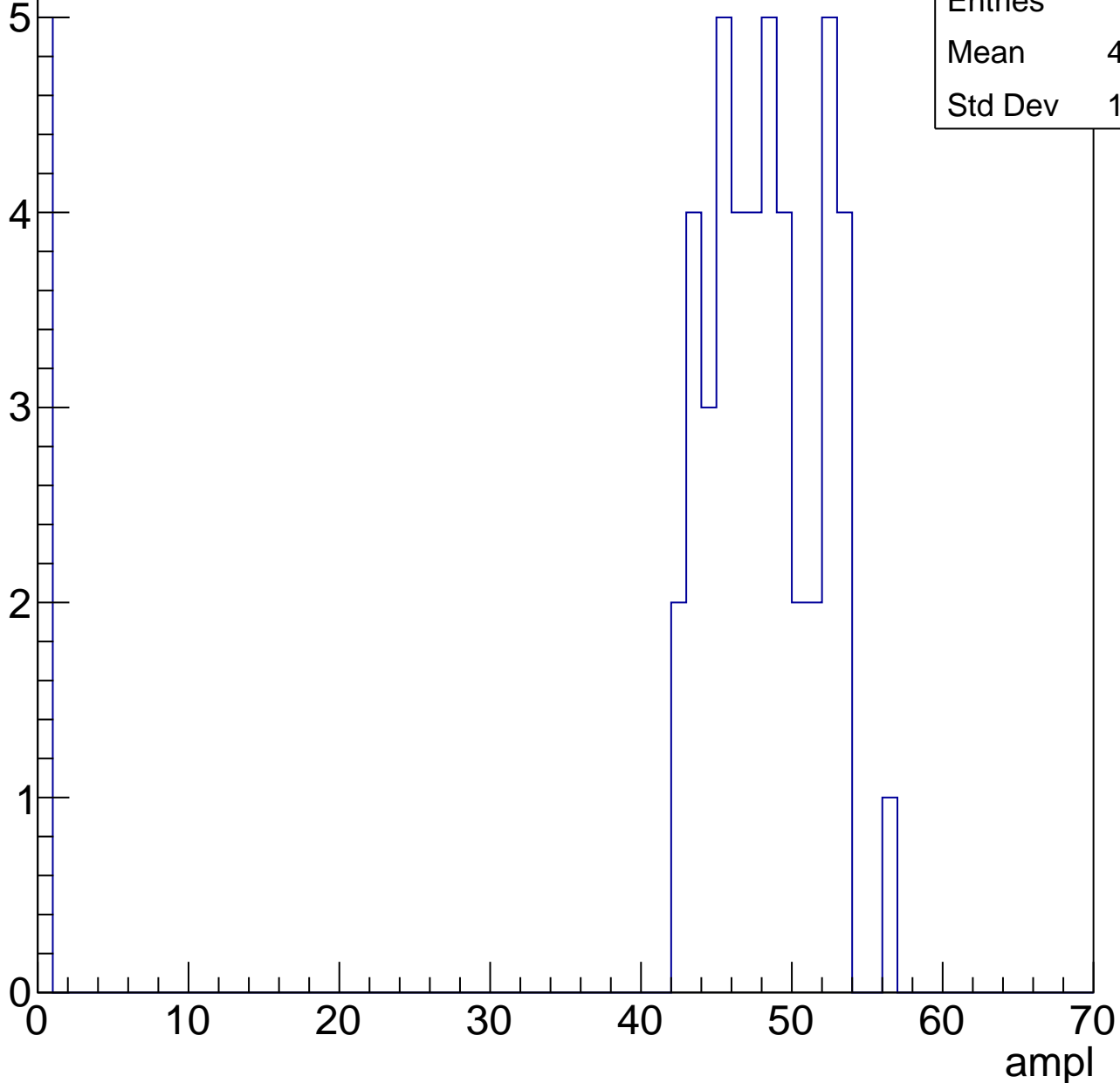


B1L103S, U14-ch113, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

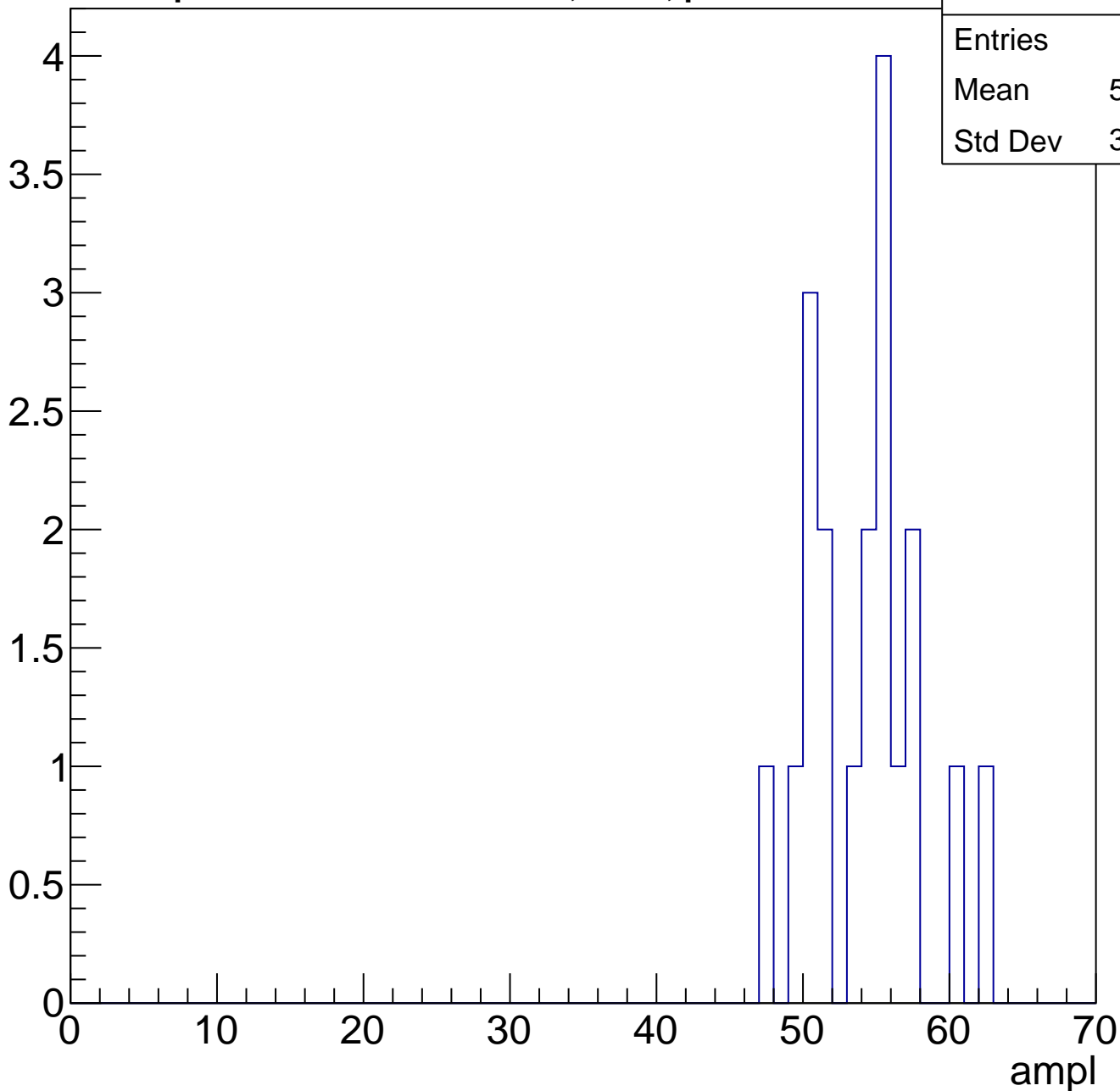
Entries	50
Mean	43.02
Std Dev	14.72



B1L103S, U14-ch113, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

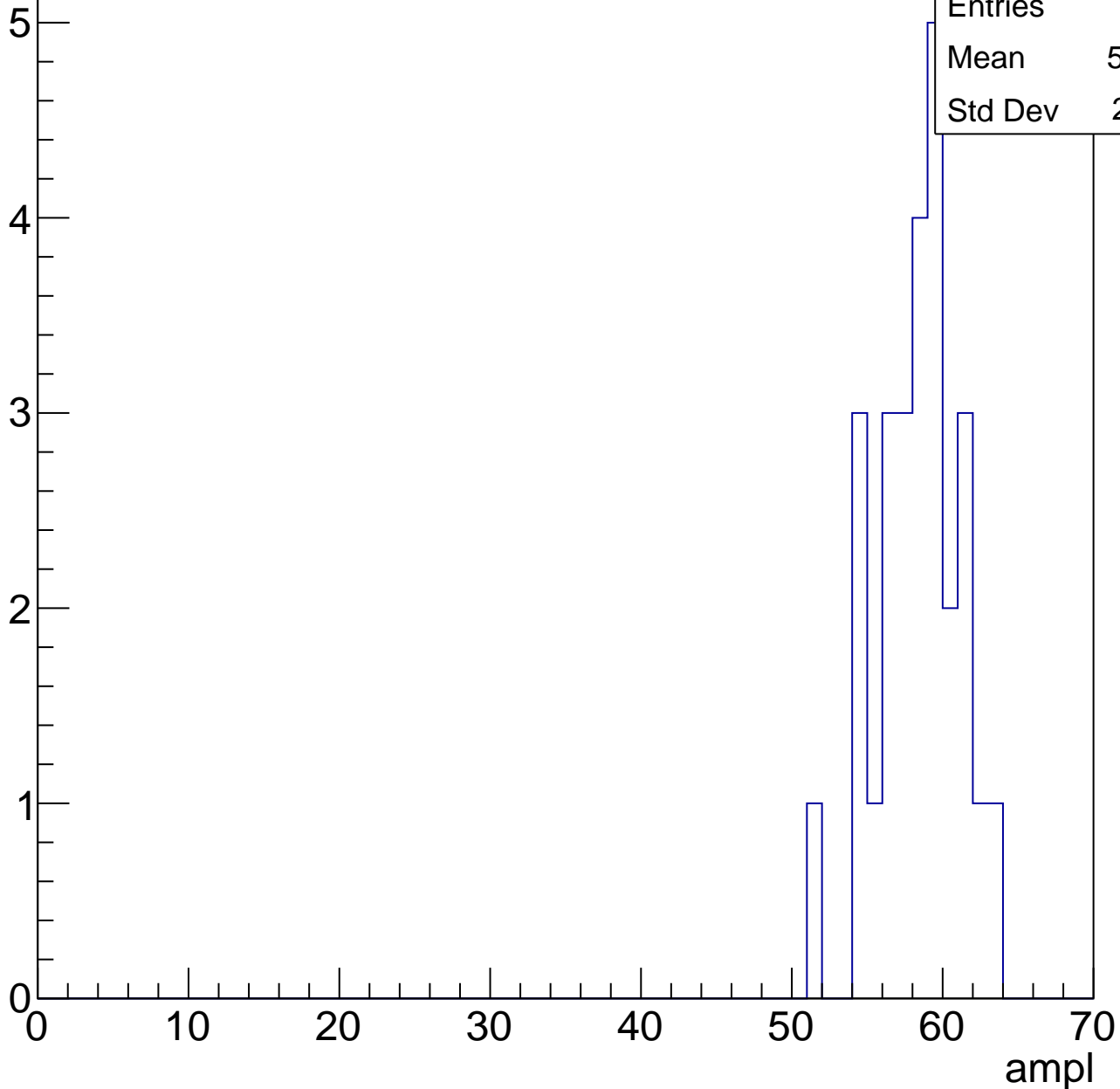


B1L103S, U14-ch113, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

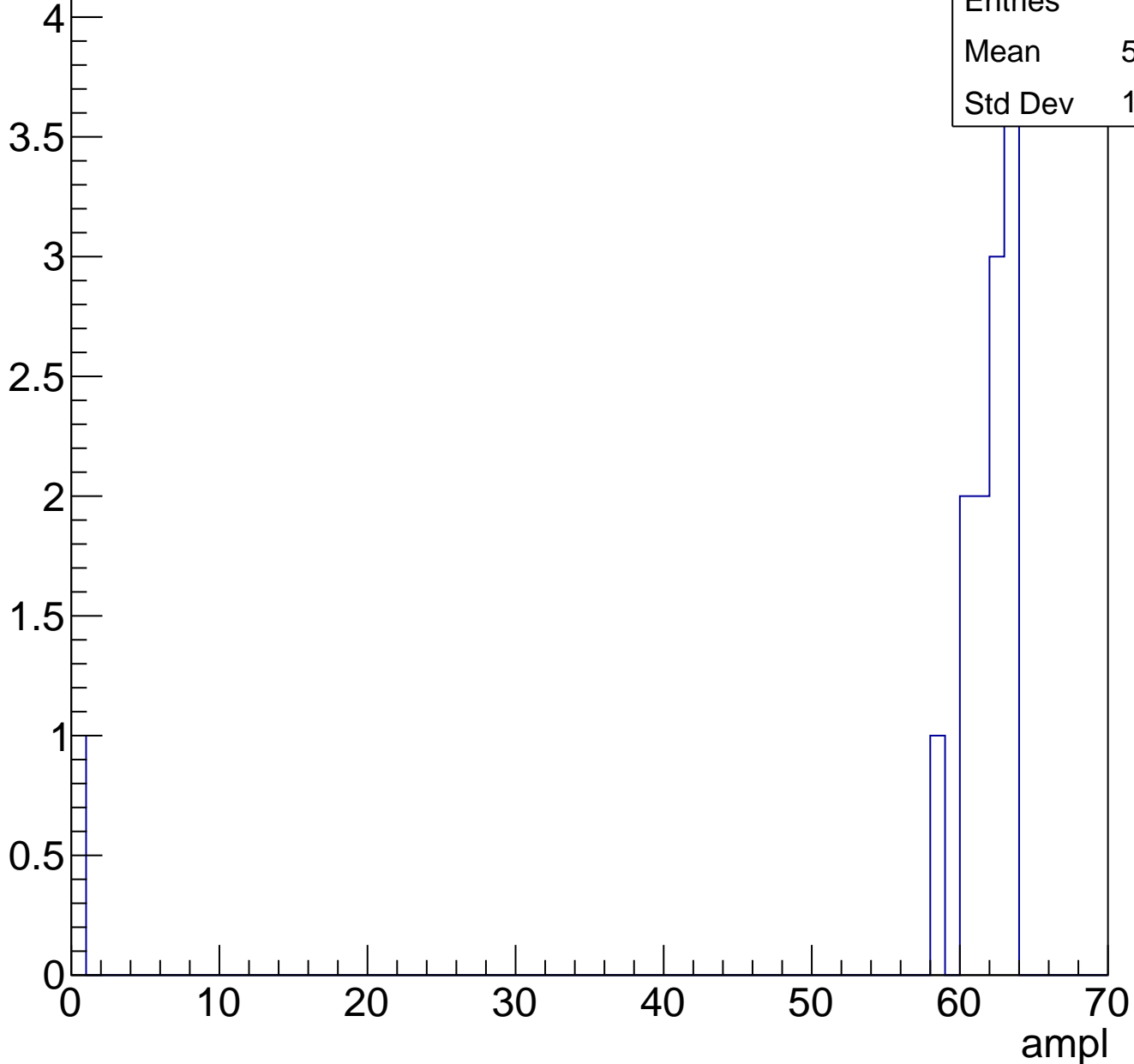
Entries	27
Mean	57.85
Std Dev	2.731



B1L103S, U14-ch113, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

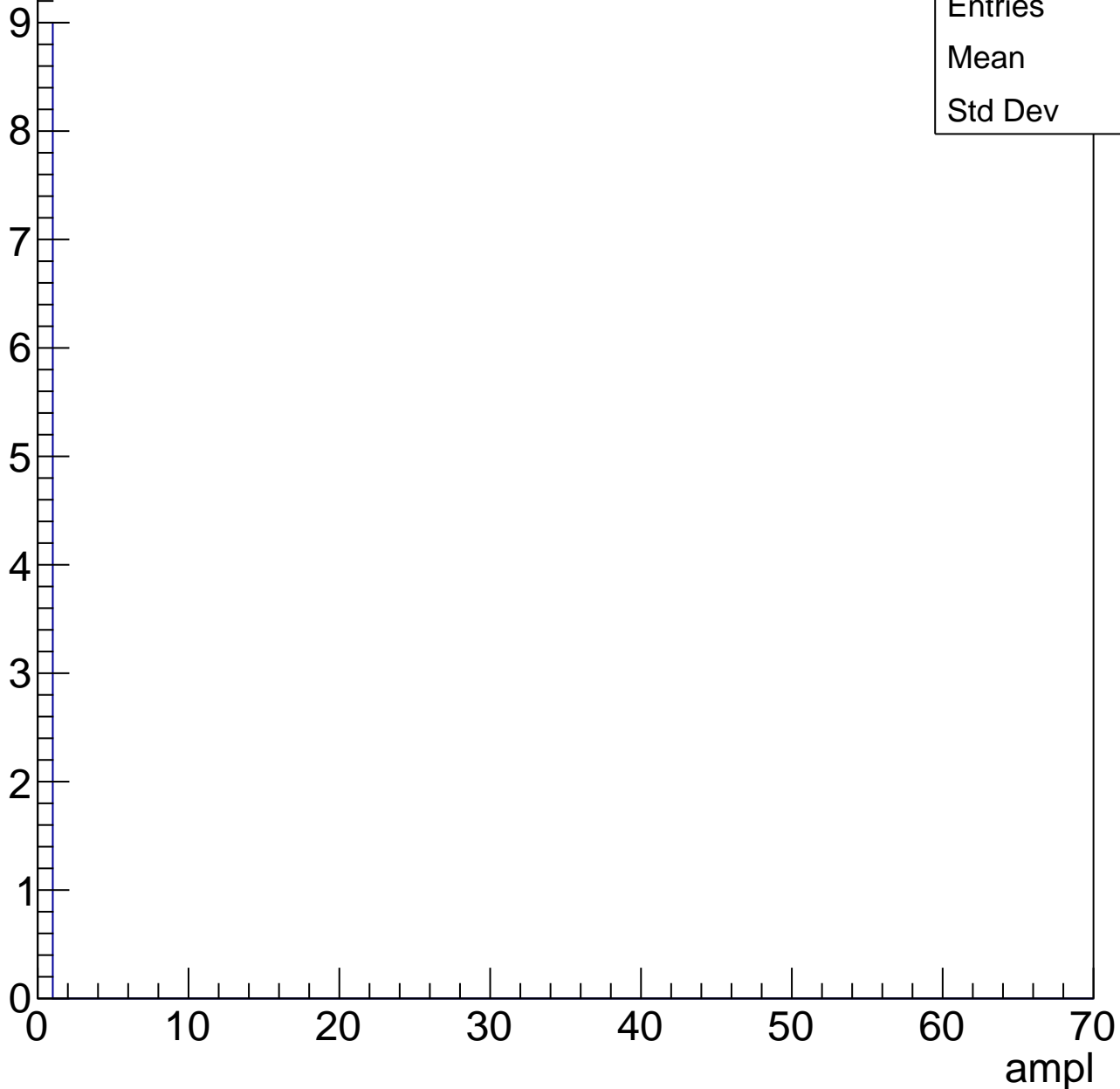


B1L103S, U14-ch113, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	9
Mean	0
Std Dev	0

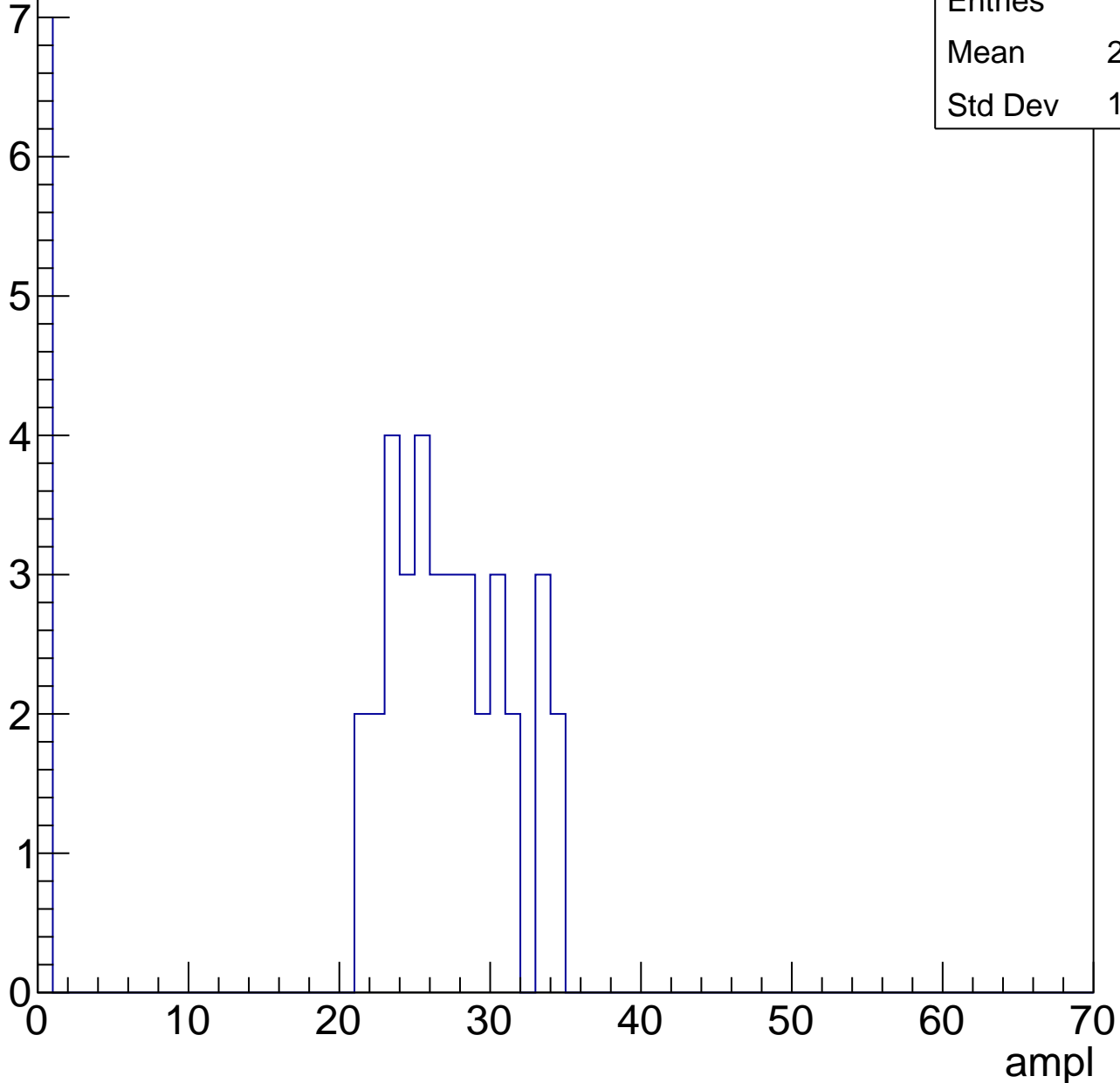


B1L103S, U14-ch114, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	43
Mean	22.56
Std Dev	10.52

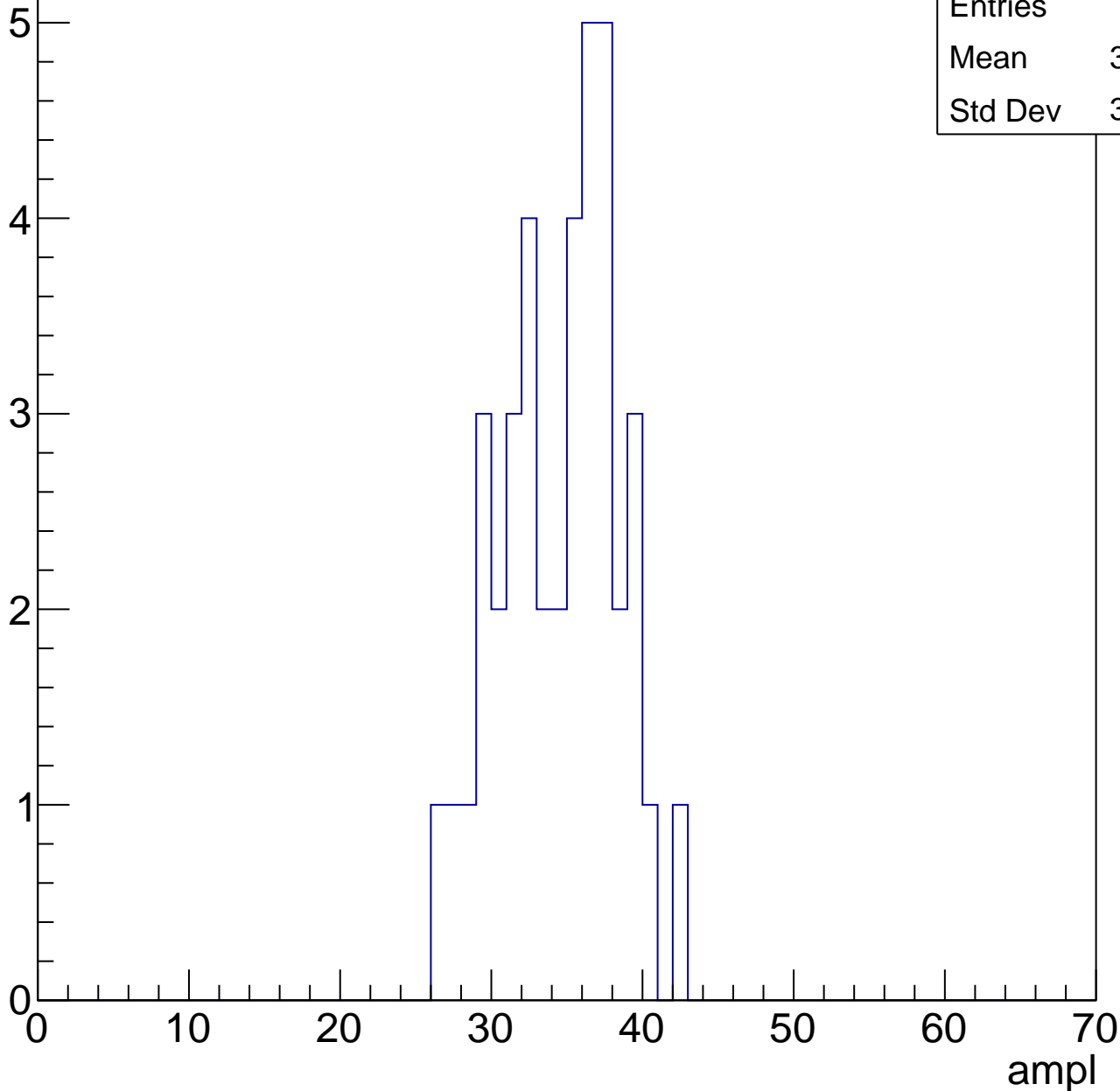


B1L103S, U14-ch114, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	34.08
Std Dev	3.797

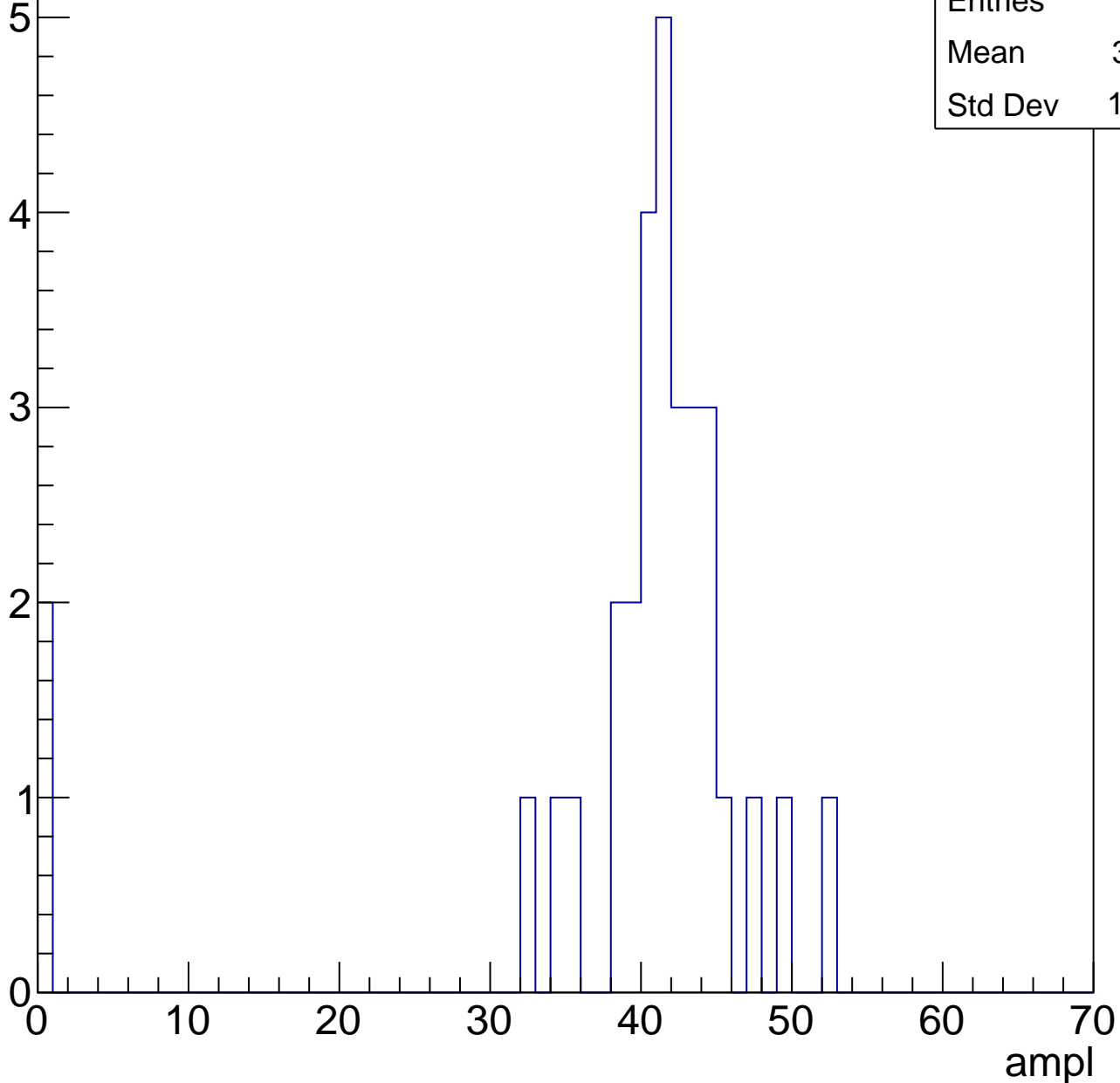


B1L103S, U14-ch114, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	31
Mean	38.71
Std Dev	10.89

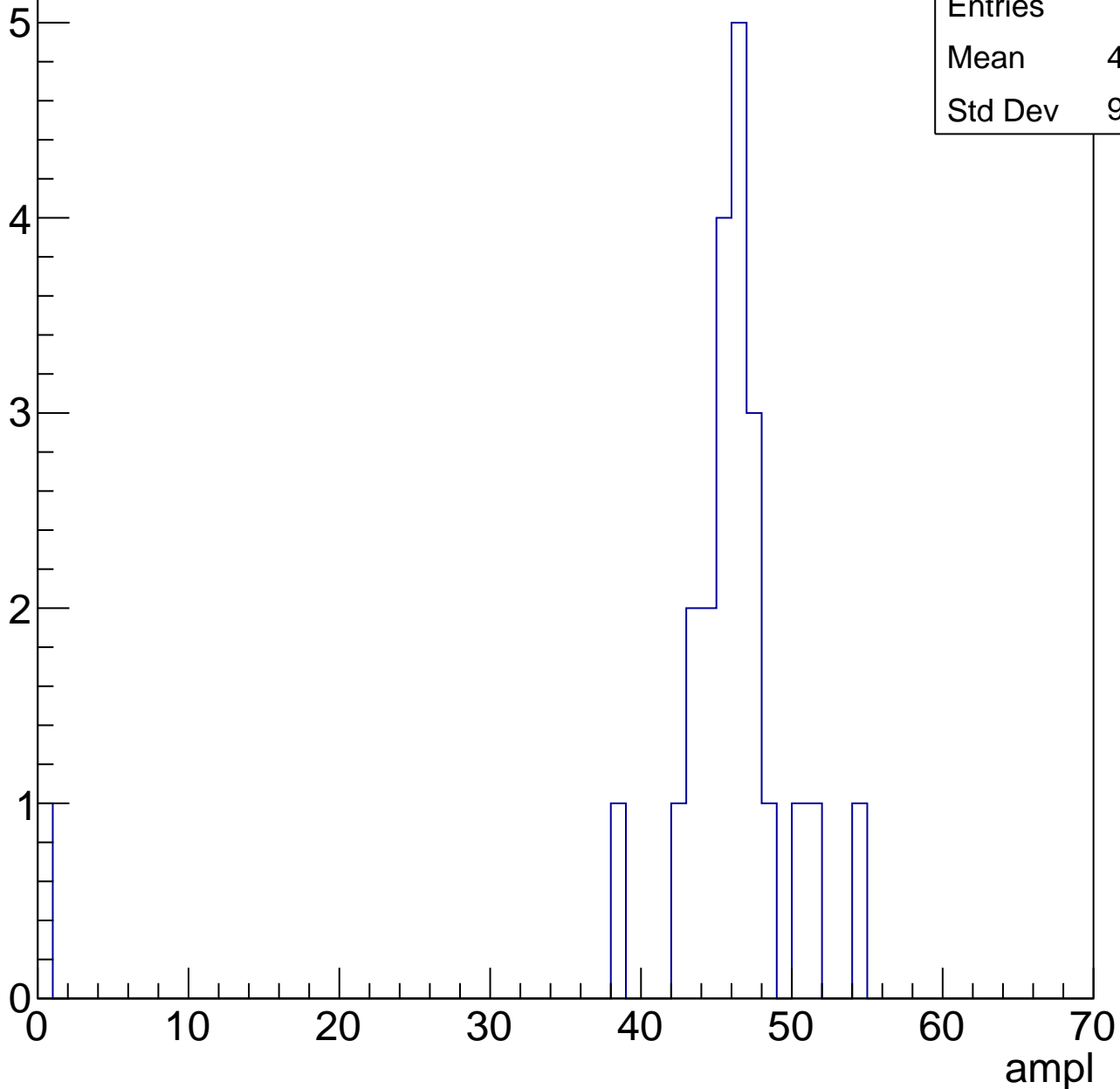


B1L103S, U14-ch114, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

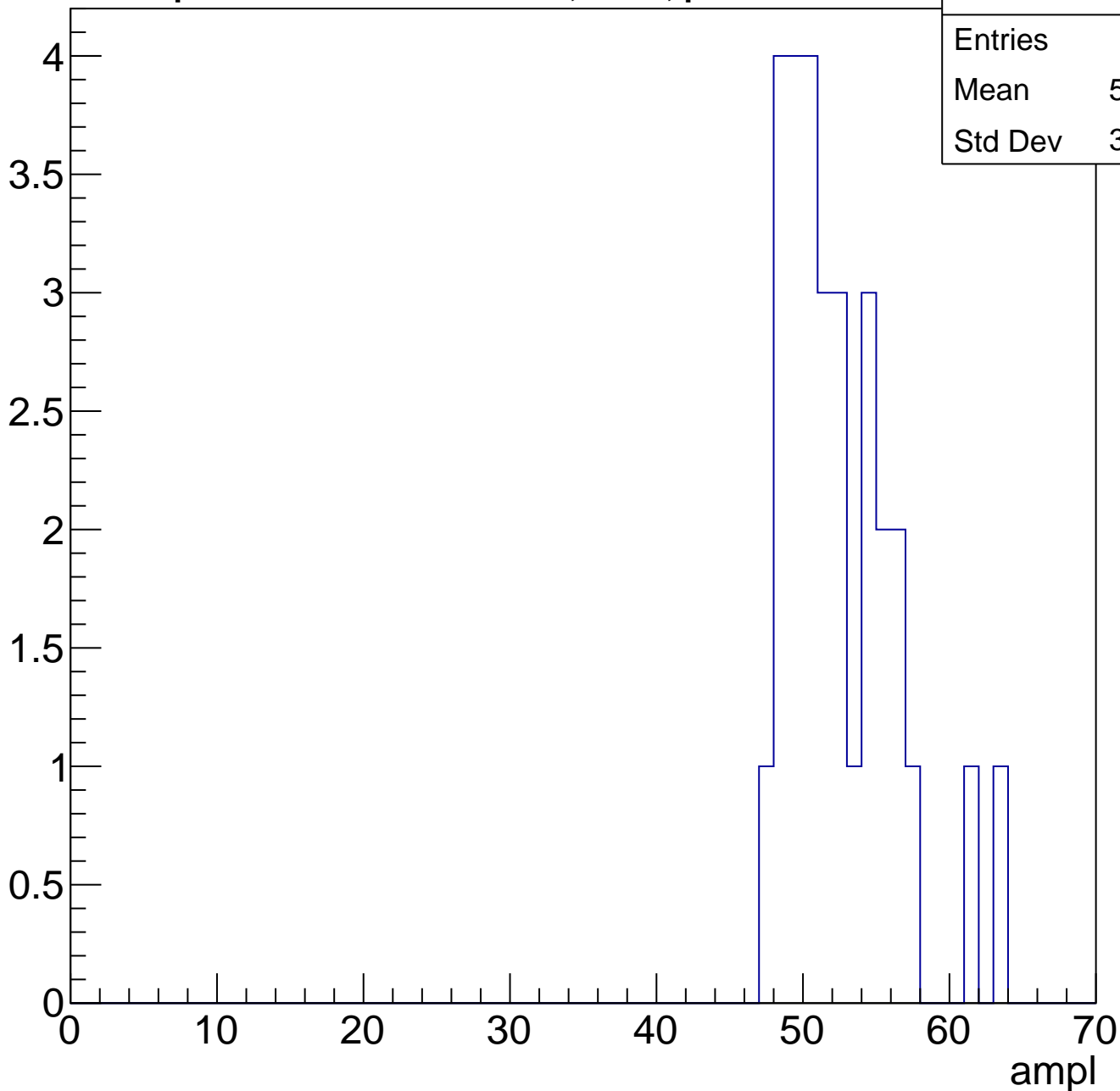
Entries	23
Mean	43.83
Std Dev	9.845



B1L103S, U14-ch114, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

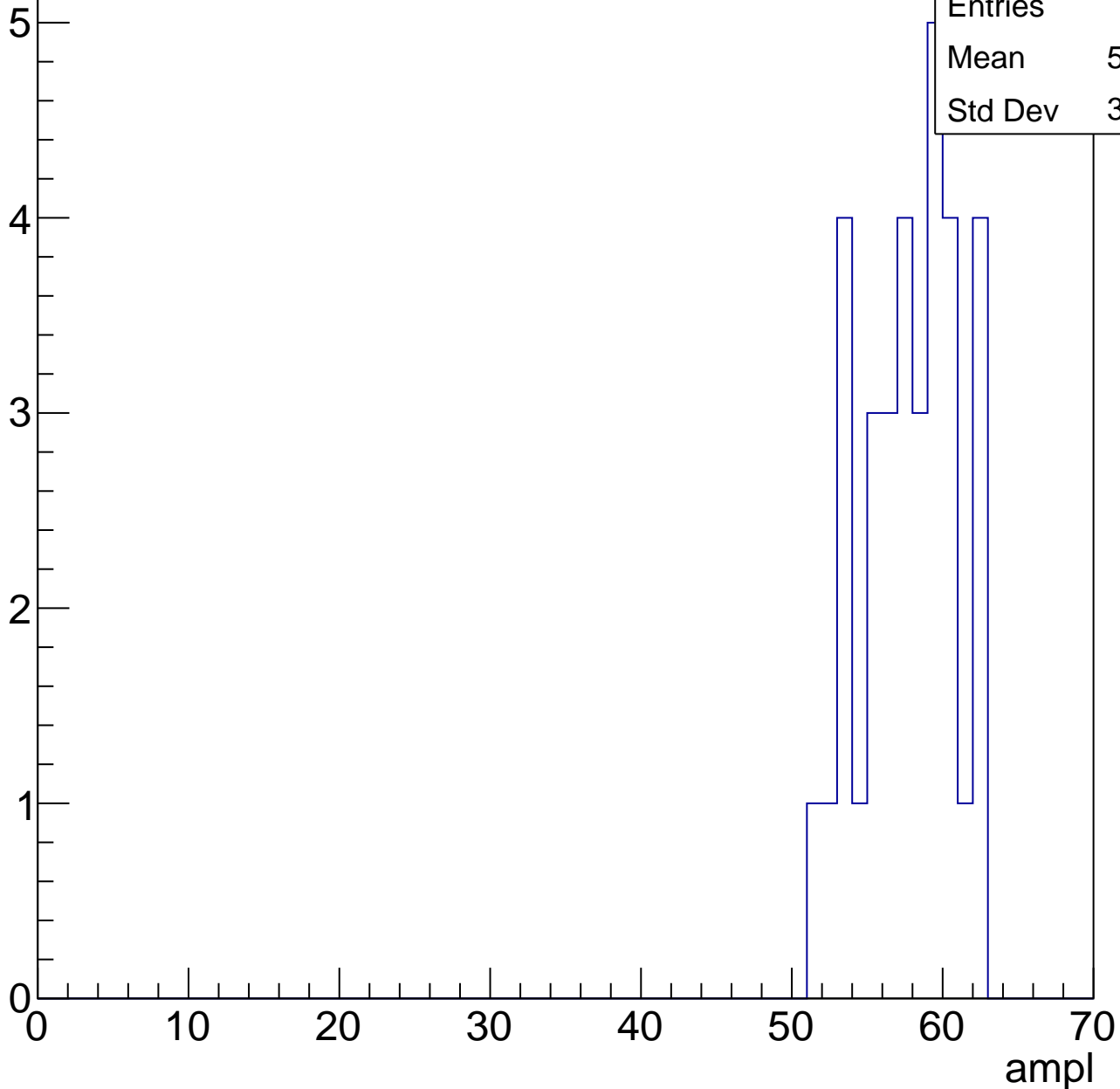


B1L103S, U14-ch114, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

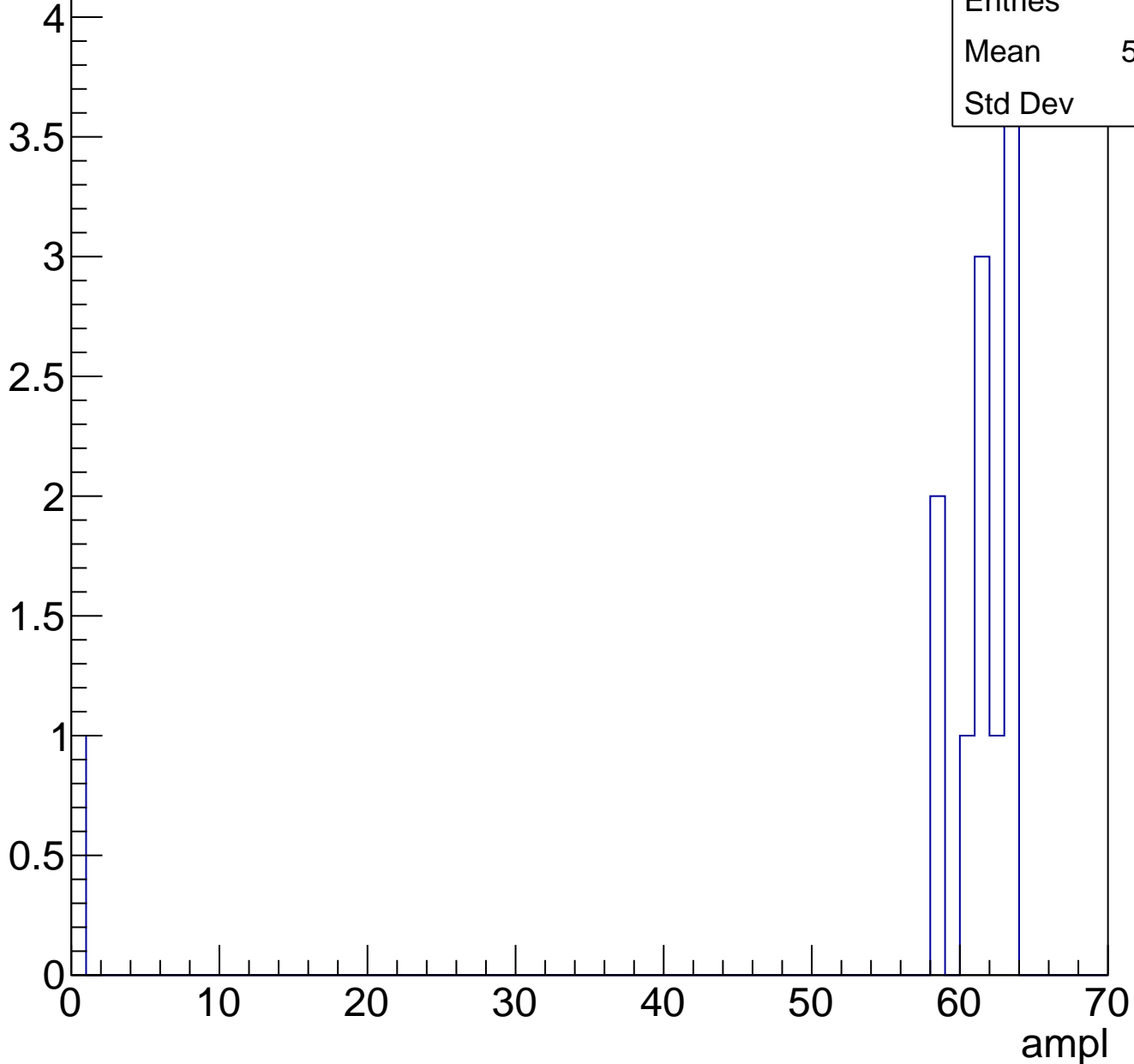
Entries	34
Mean	57.29
Std Dev	3.073



B1L103S, U14-ch114, adc6

calib_packv5_041523_1651.root, FC#0, port C2

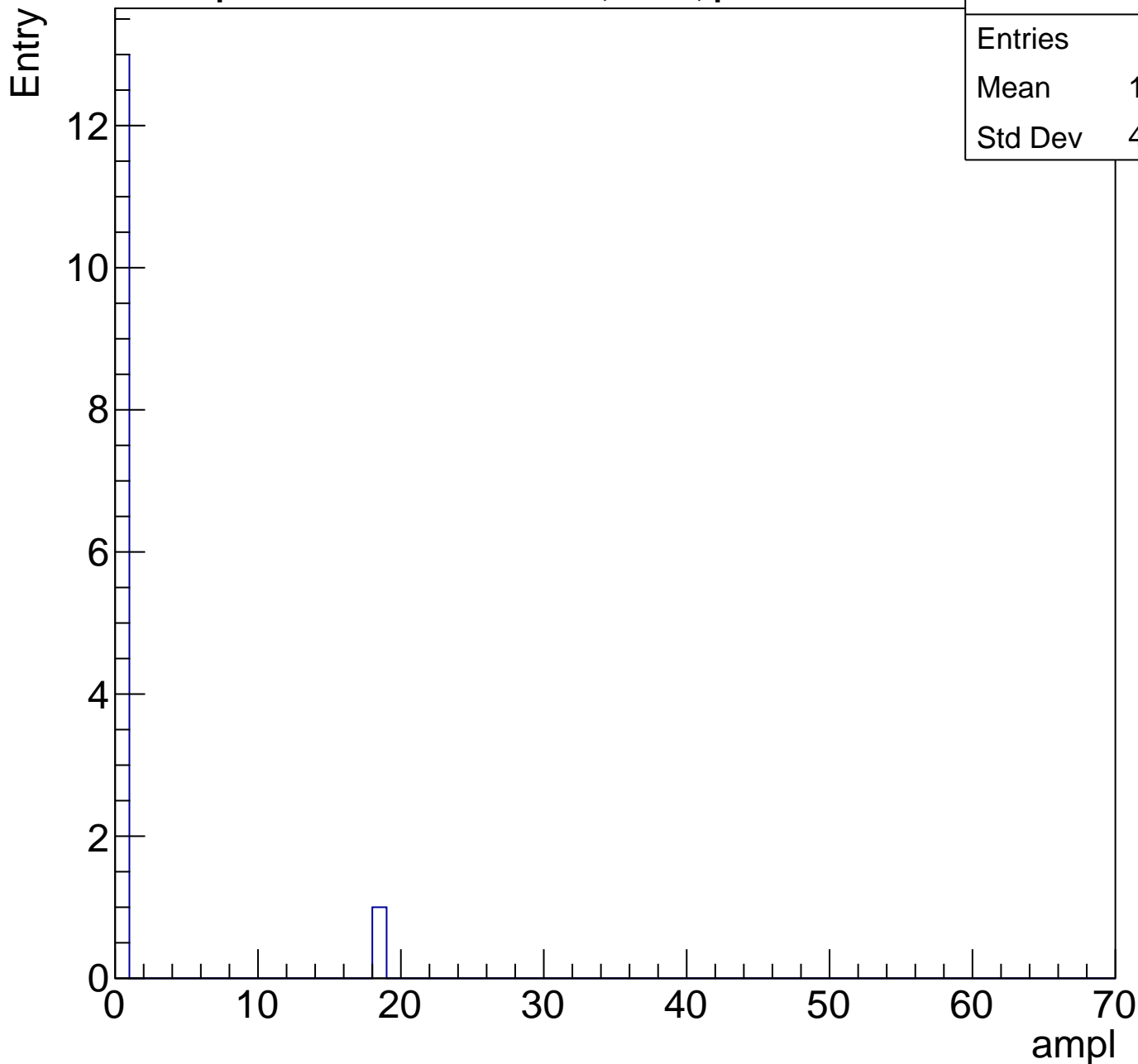
Entry



B1L103S, U14-ch114, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	14
Mean	1.286
Std Dev	4.636



B1L103S, U14-ch115, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	49
Mean	18.55
Std Dev	13.78

Entry

16
14
12
10
8
6
4
2
0

0

10

20

30

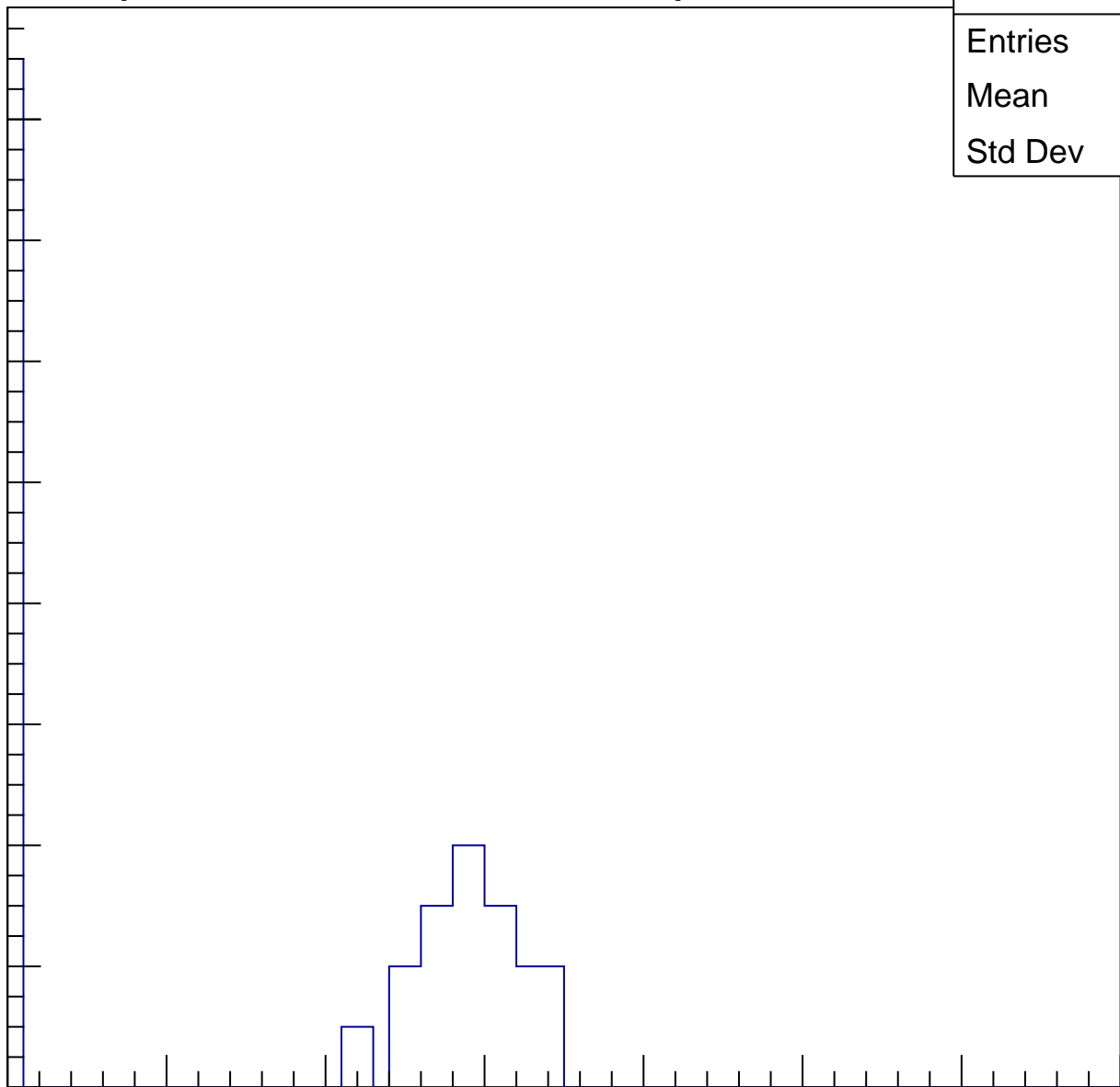
40

50

60

70

ampl

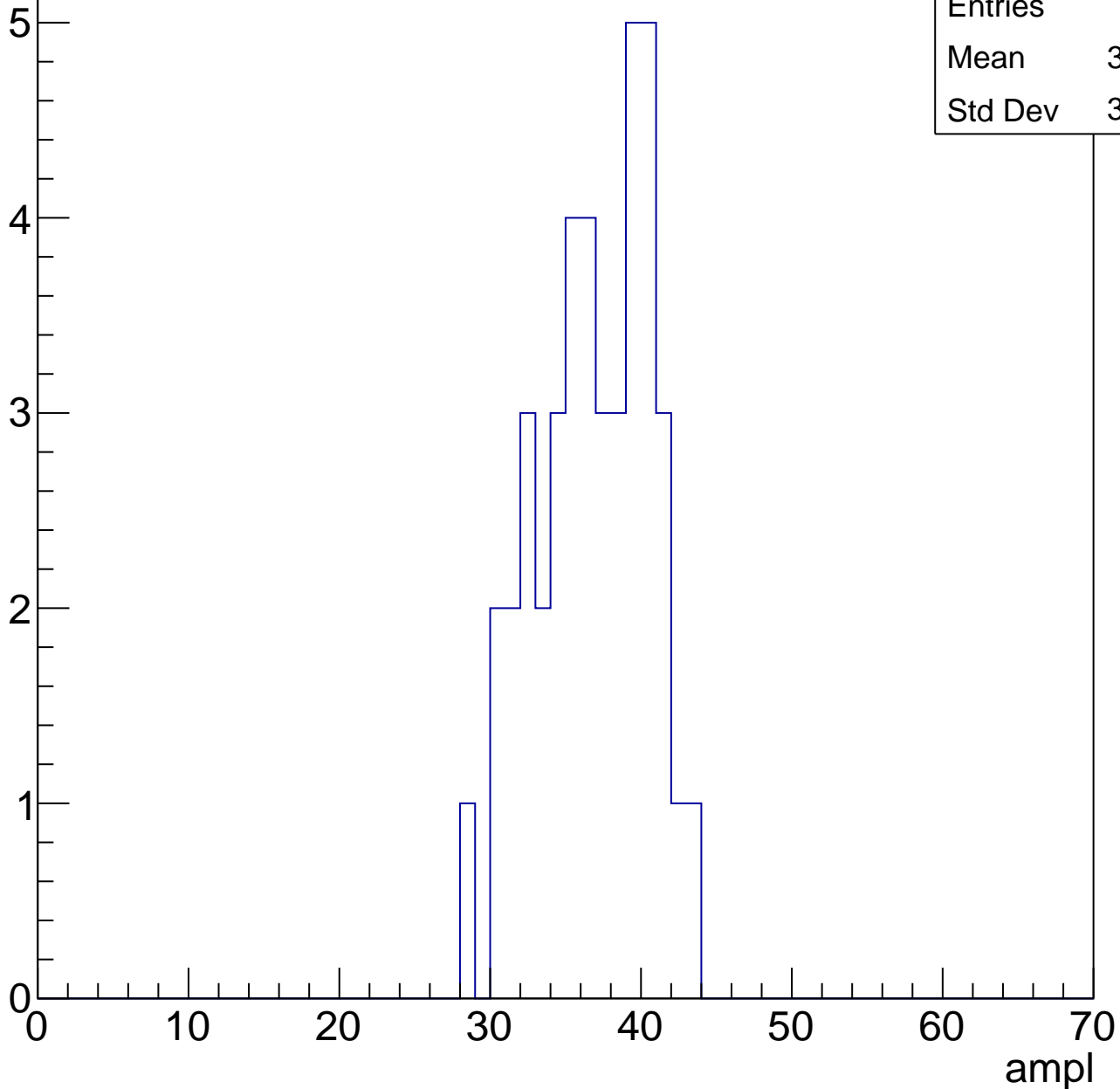


B1L103S, U14-ch115, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	42
Mean	36.33
Std Dev	3.662

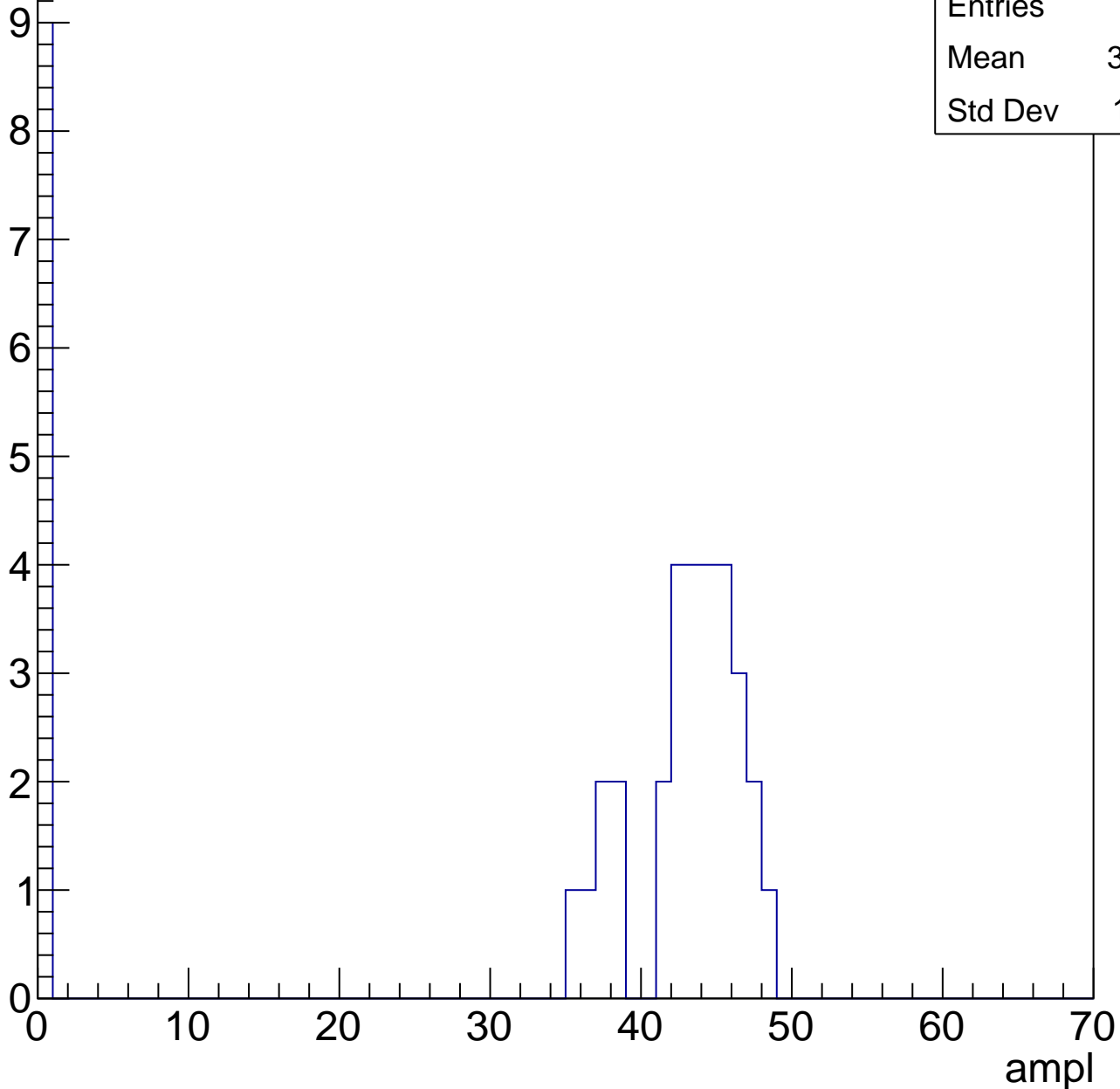


B1L103S, U14-ch115, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

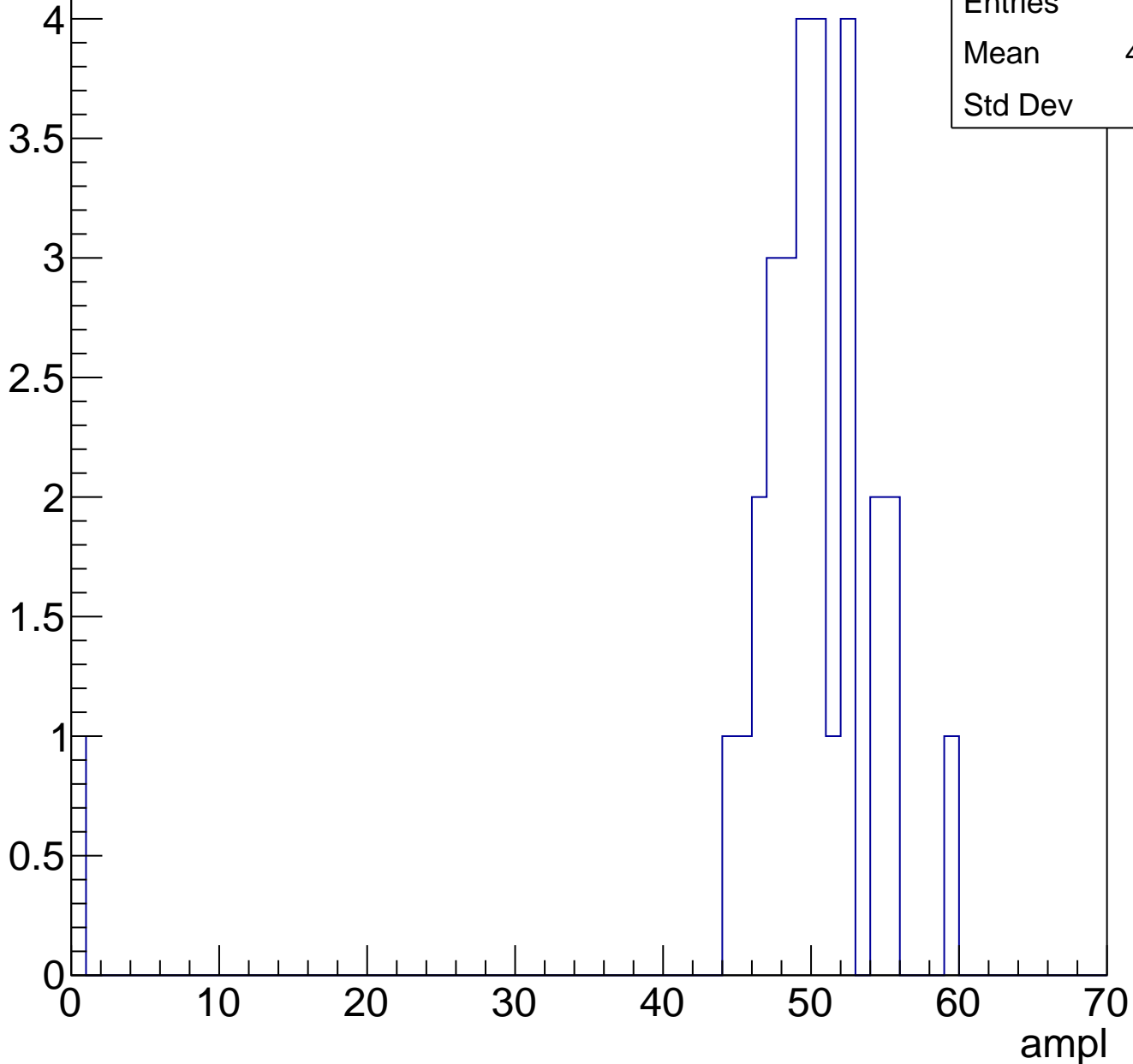
Entries	39
Mean	32.79
Std Dev	18.21



B1L103S, U14-ch115, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

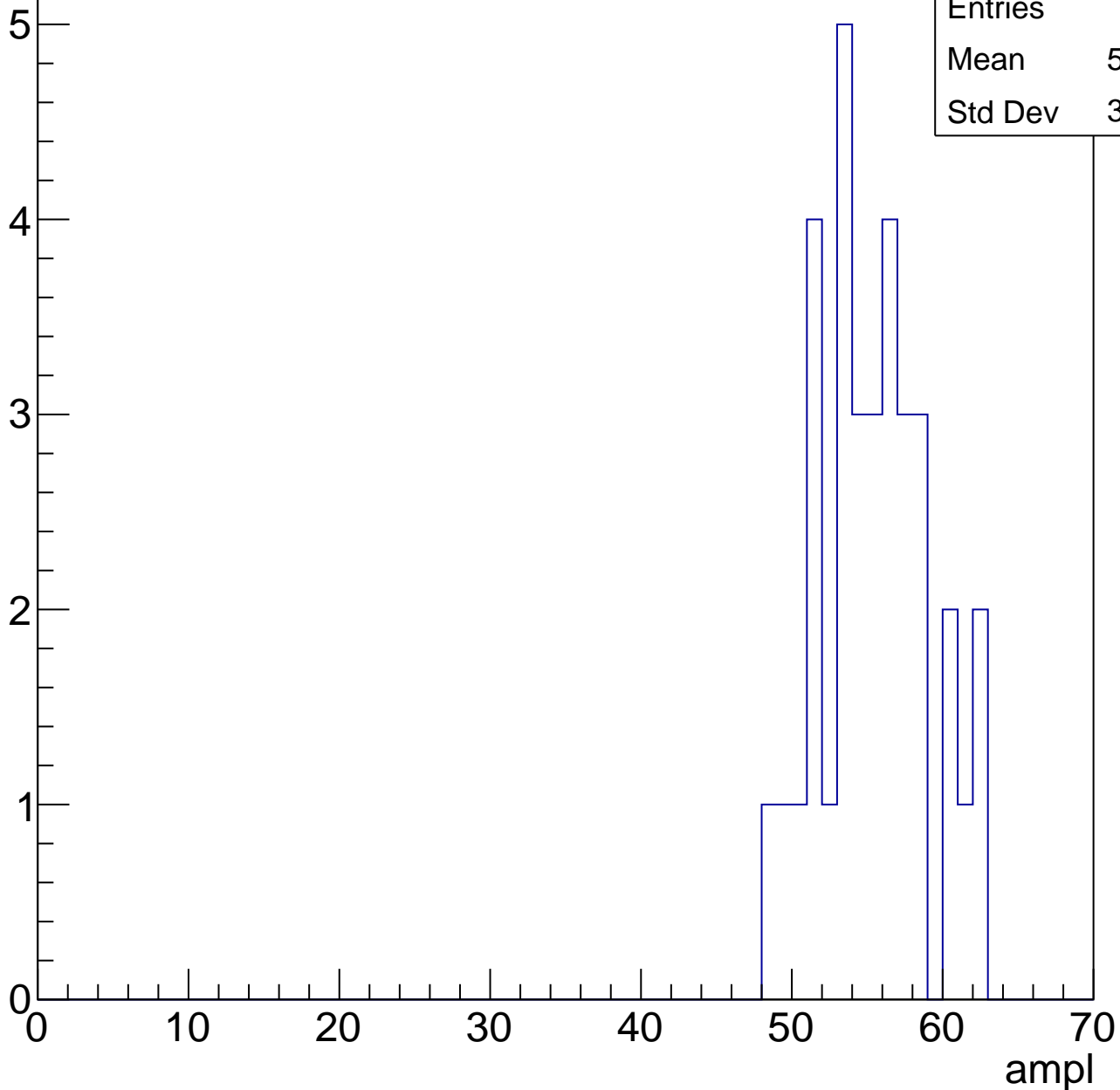


B1L103S, U14-ch115, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

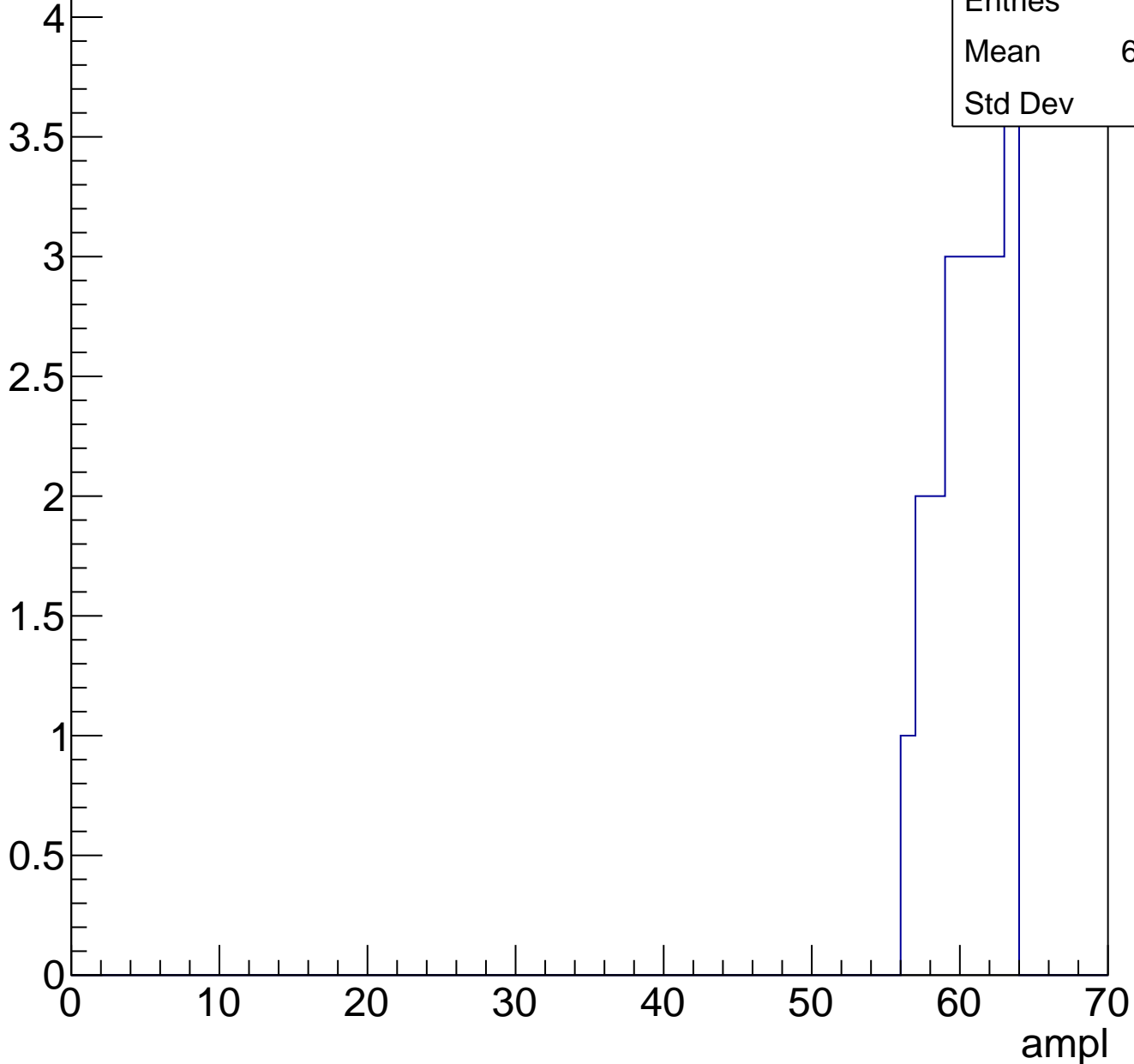
Entries	34
Mean	54.97
Std Dev	3.569



B1L103S, U14-ch115, adc5

calib_packv5_041523_1651.root, FC#0, port C2

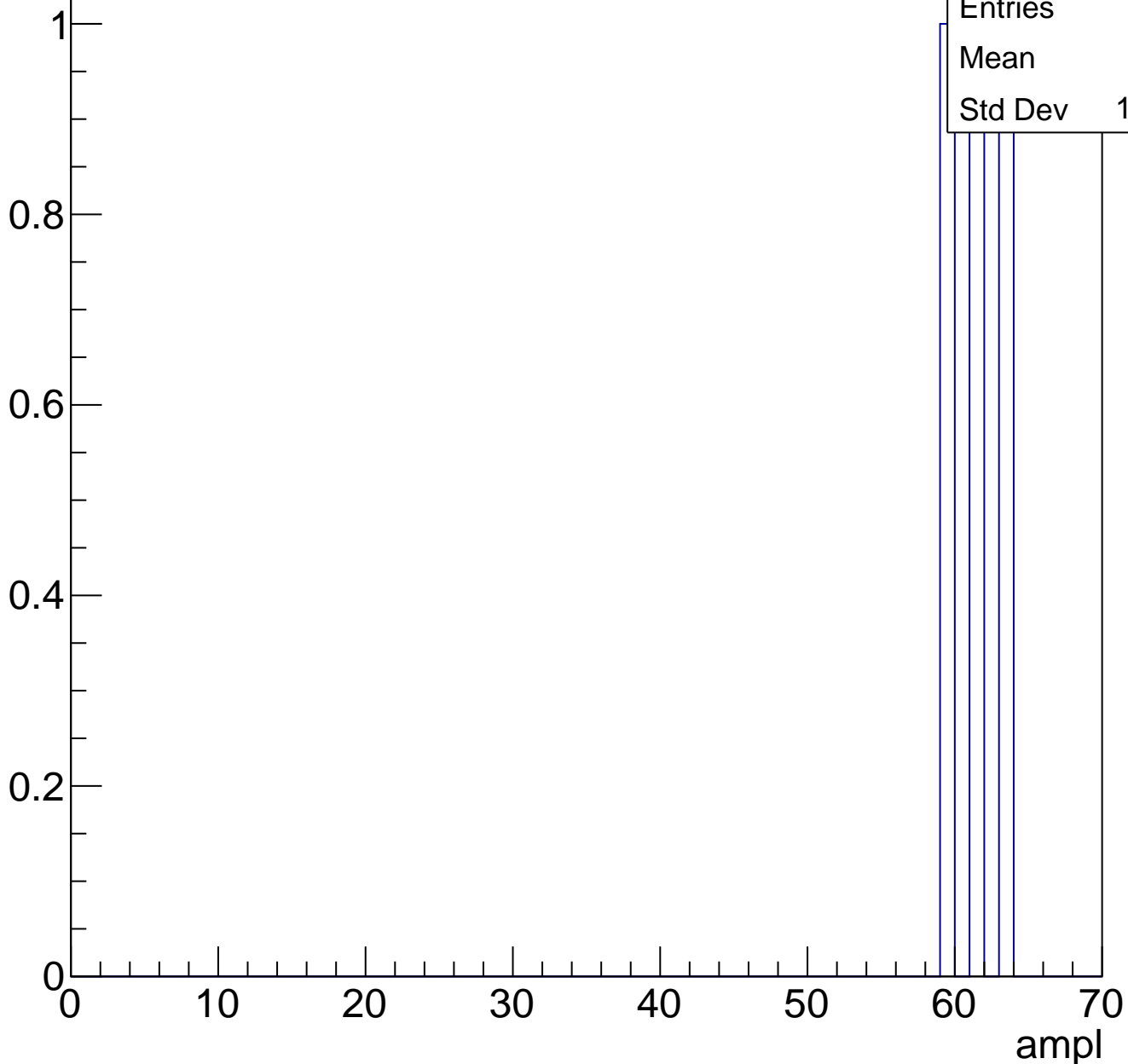
Entry



B1L103S, U14-ch115, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	3
Mean	61
Std Dev	1.633

B1L103S, U14-ch115, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

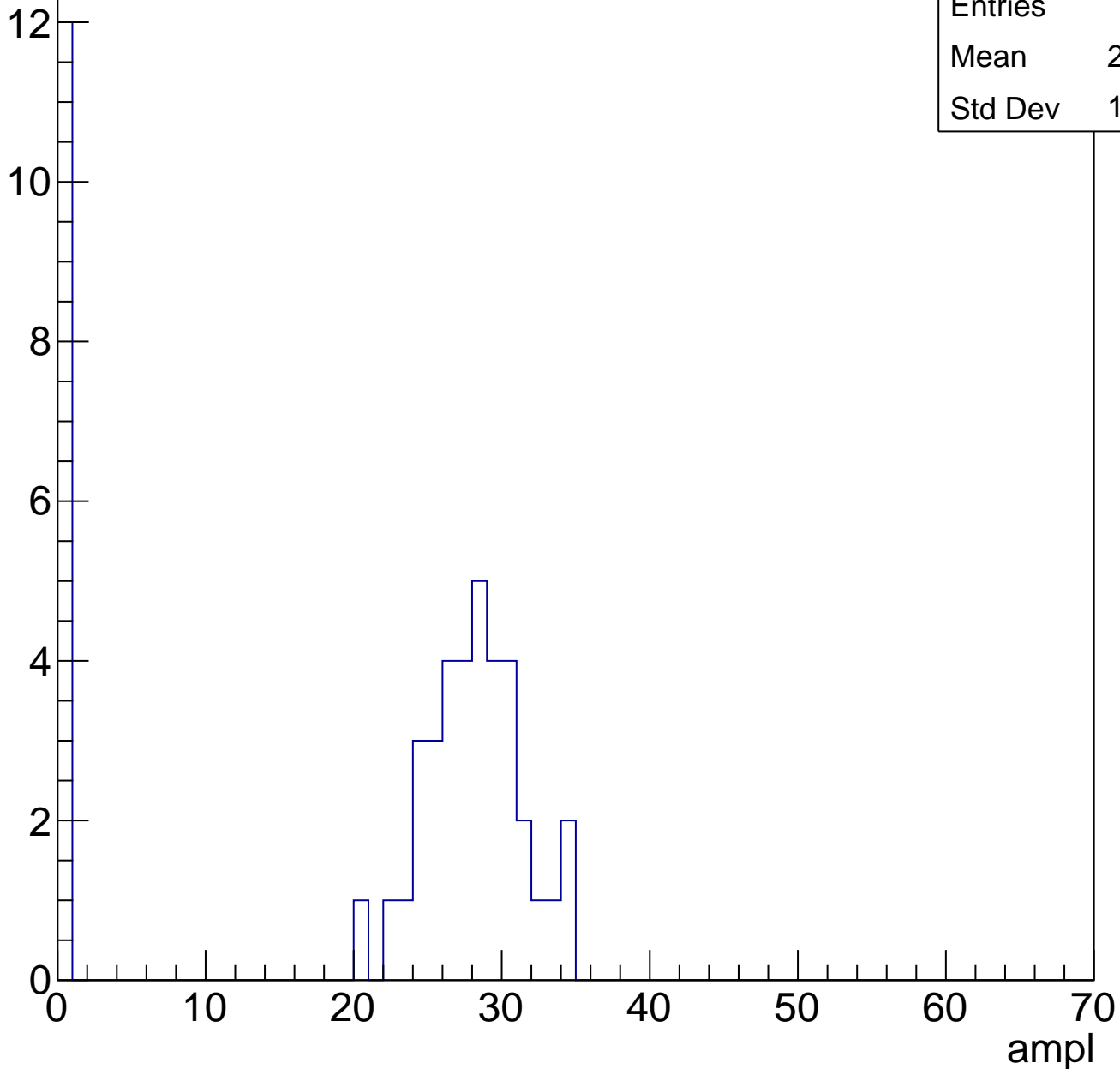
Entries	10
Mean	0
Std Dev	0

B1L103S, U14-ch116, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	48
Mean	20.73
Std Dev	12.28

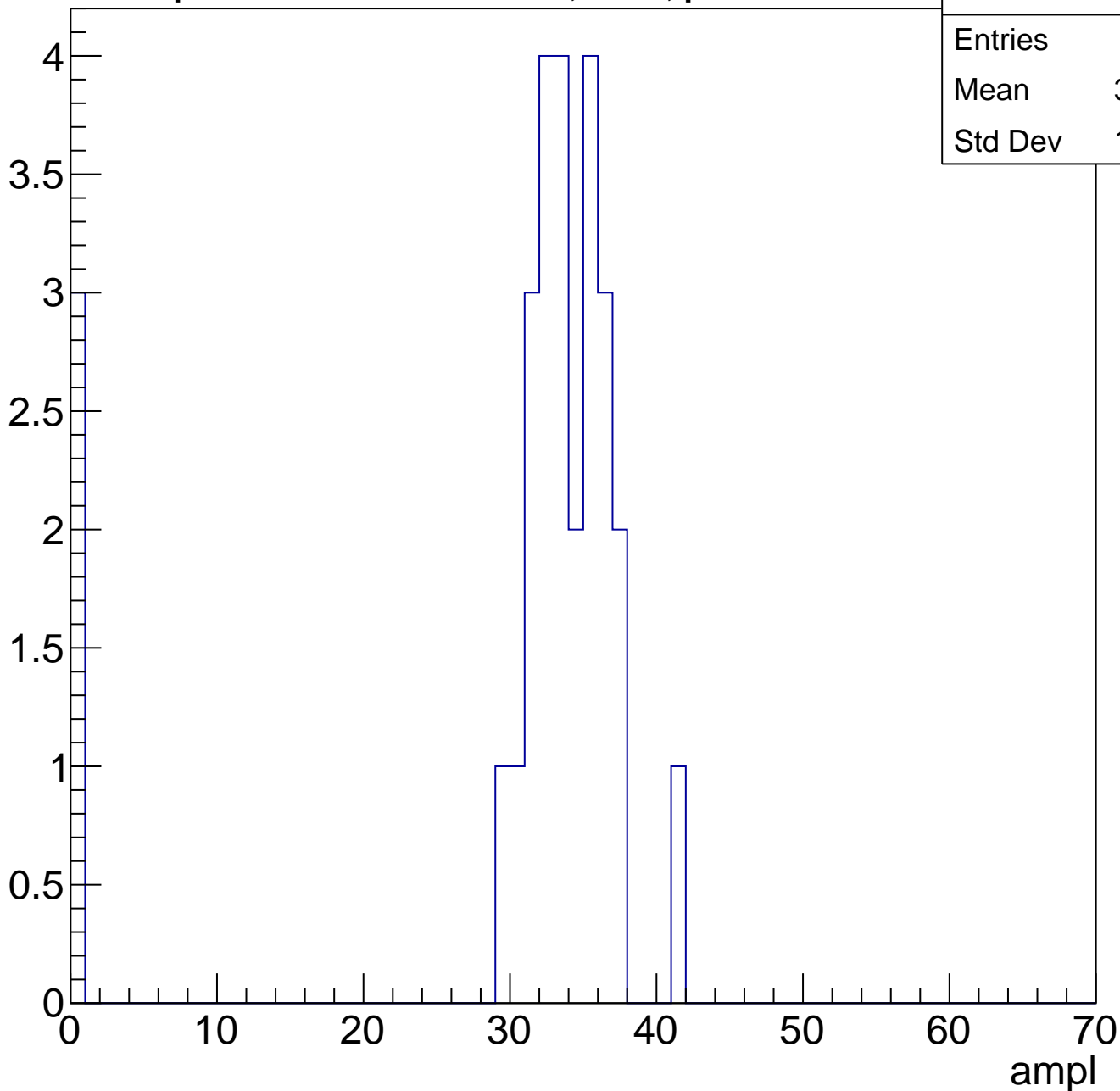
Entry



B1L103S, U14-ch116, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry



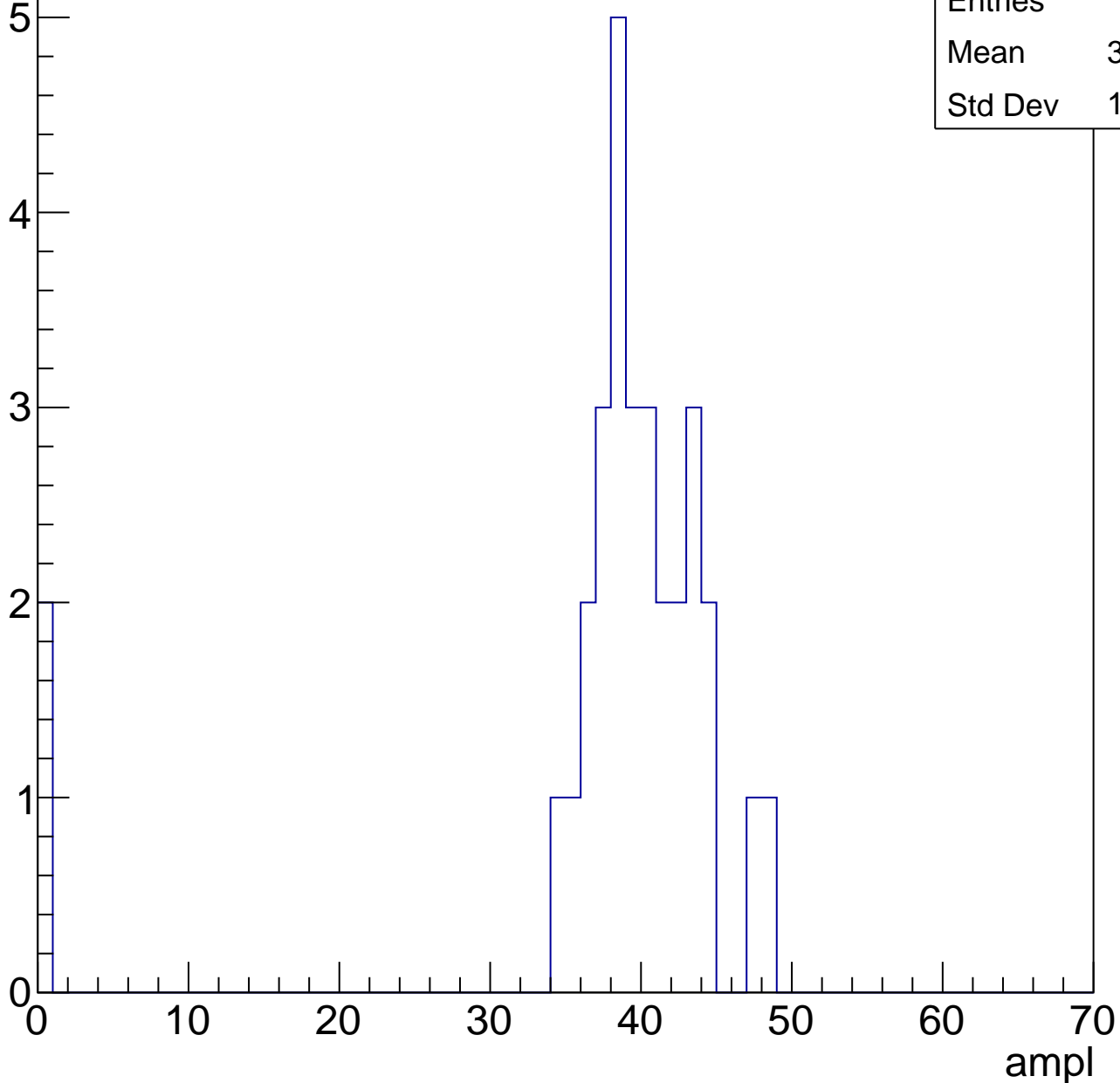
Entries	28
Mean	30.11
Std Dev	10.71

B1L103S, U14-ch116, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	31
Mean	37.32
Std Dev	10.32

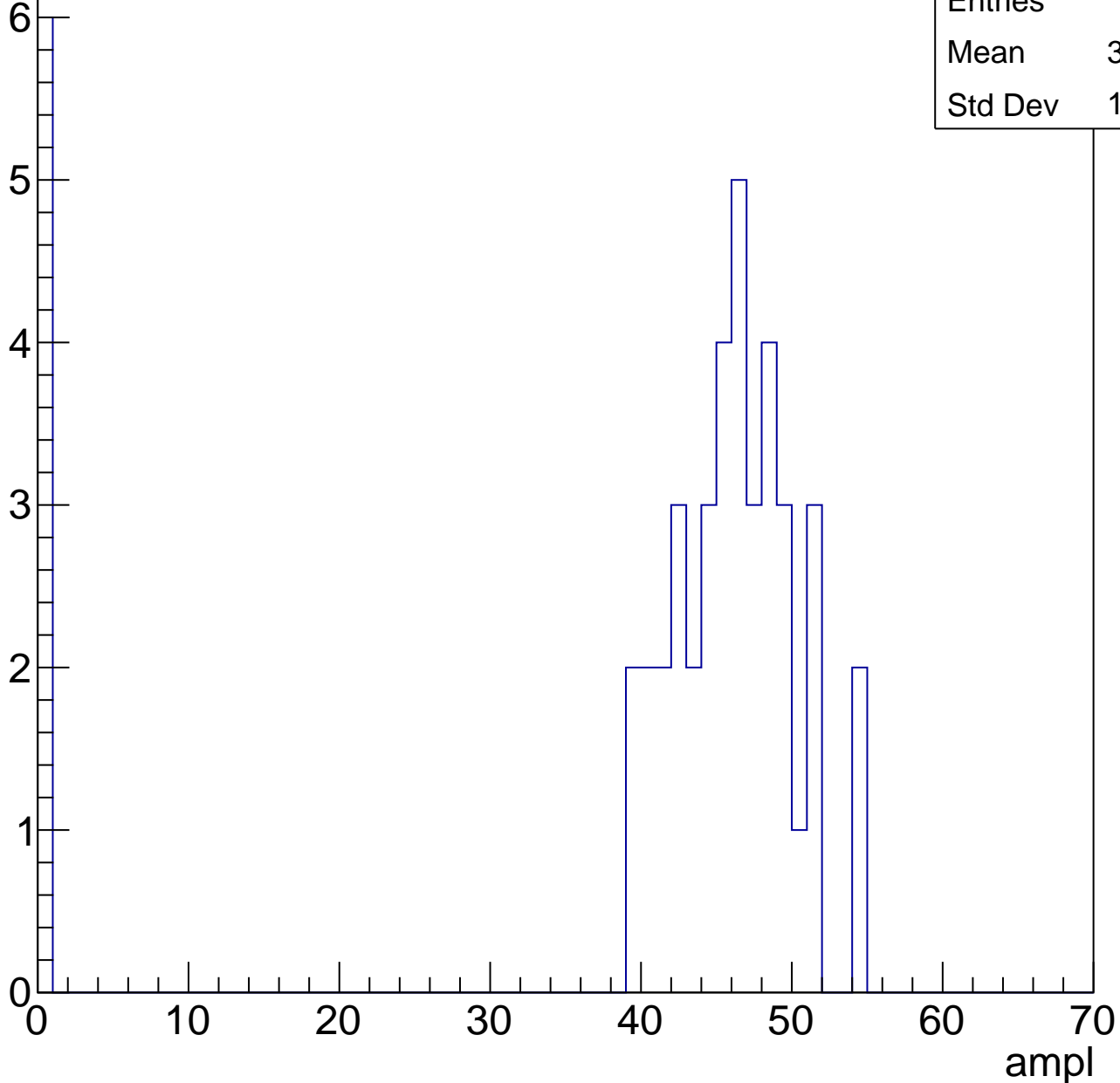


B1L103S, U14-ch116, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

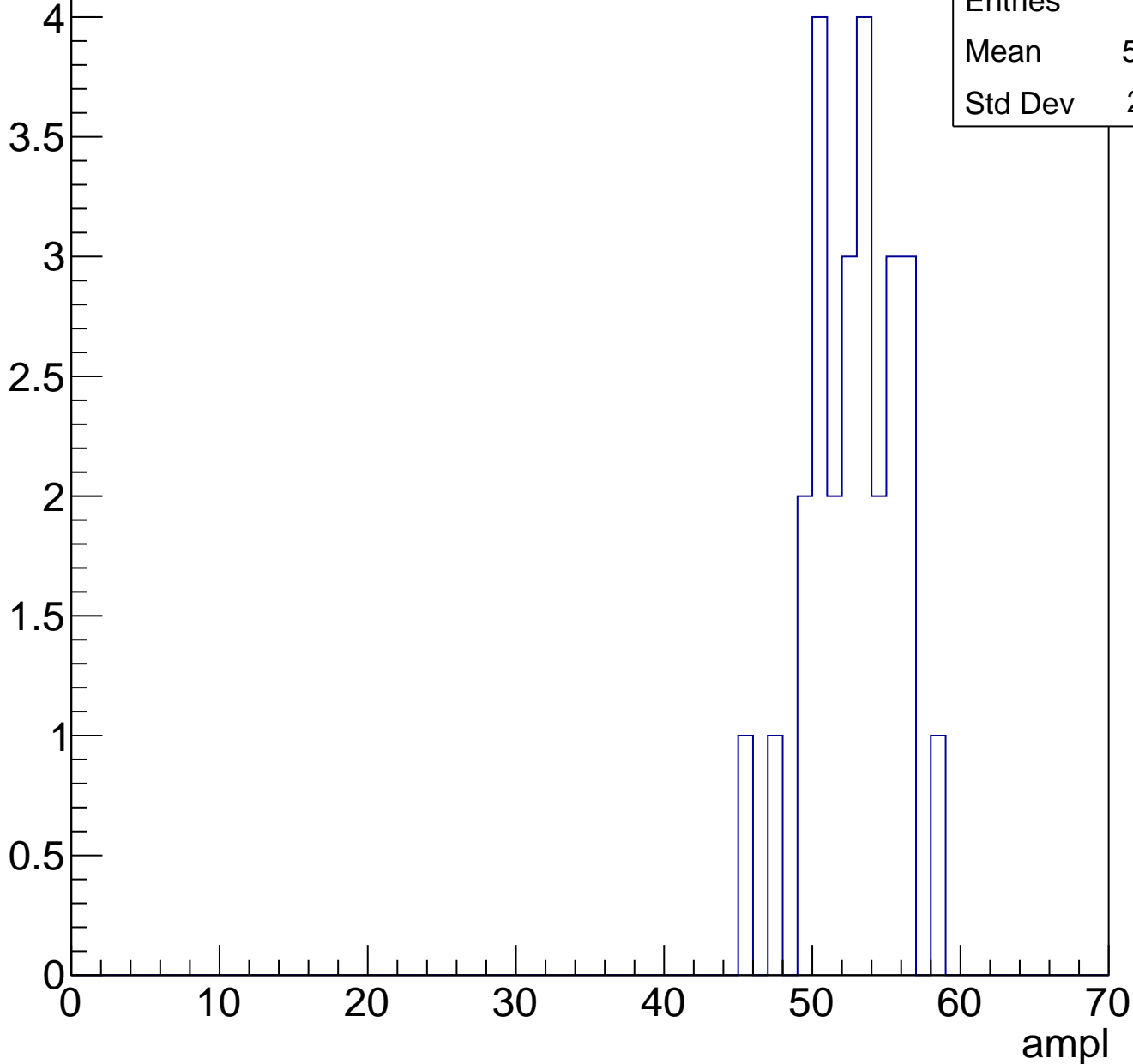
Entries	45
Mean	39.67
Std Dev	15.96



B1L103S, U14-ch116, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

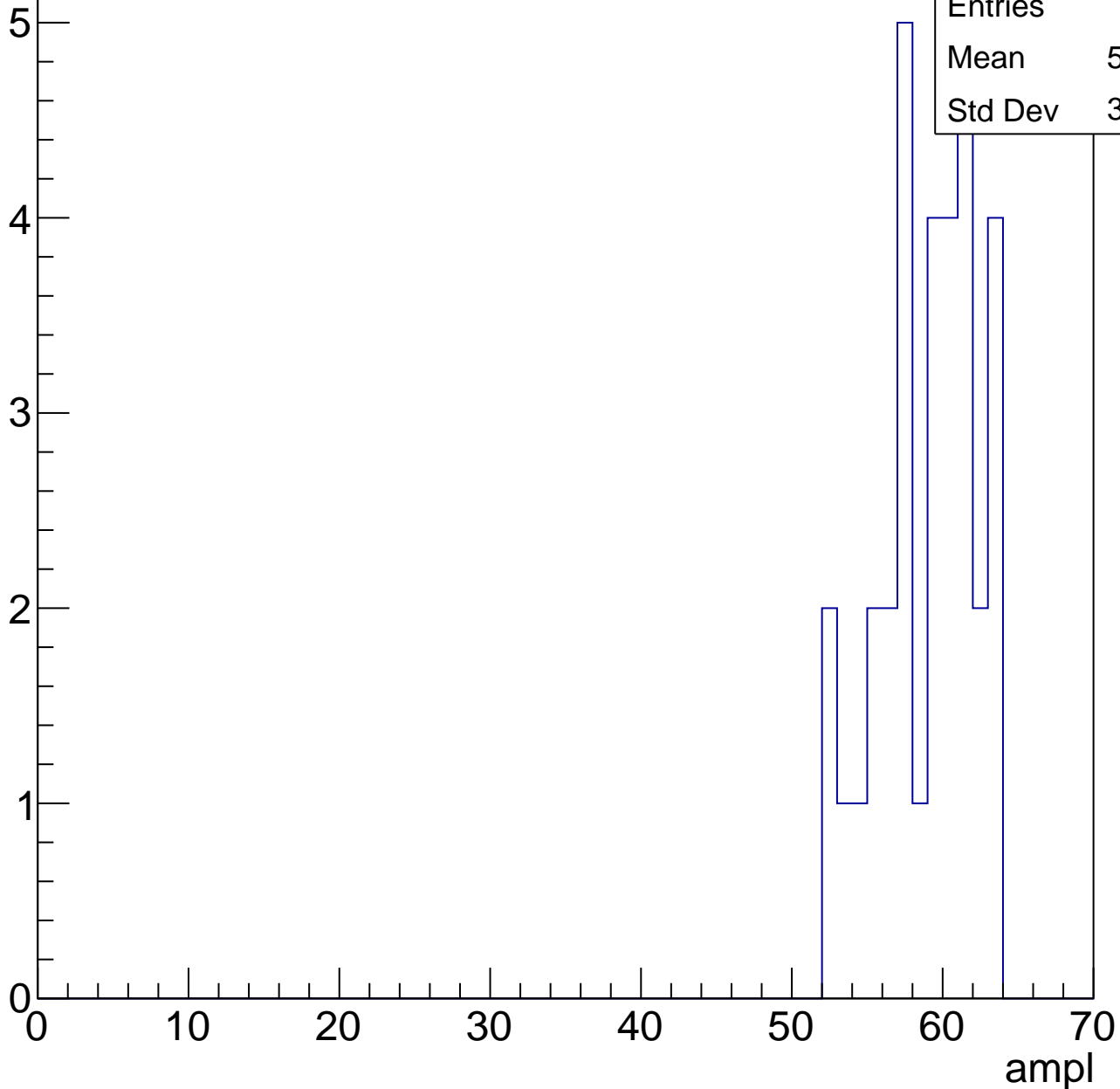


B1L103S, U14-ch116, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	33
Mean	58.58
Std Dev	3.163



B1L103S, U14-ch116, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

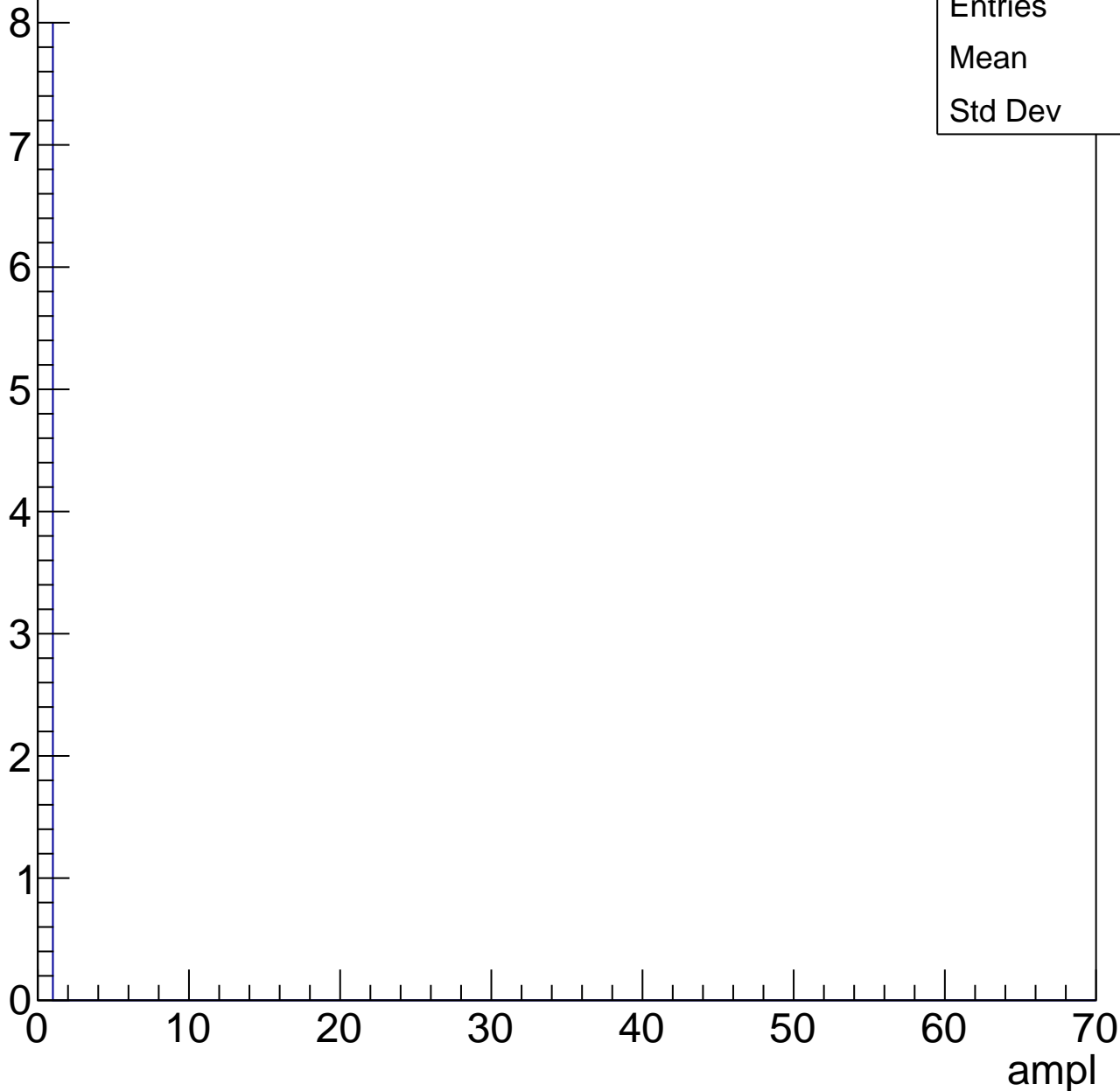
Entries	9
Mean	60.22
Std Dev	1.931

B1L103S, U14-ch116, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	8
Mean	0
Std Dev	0

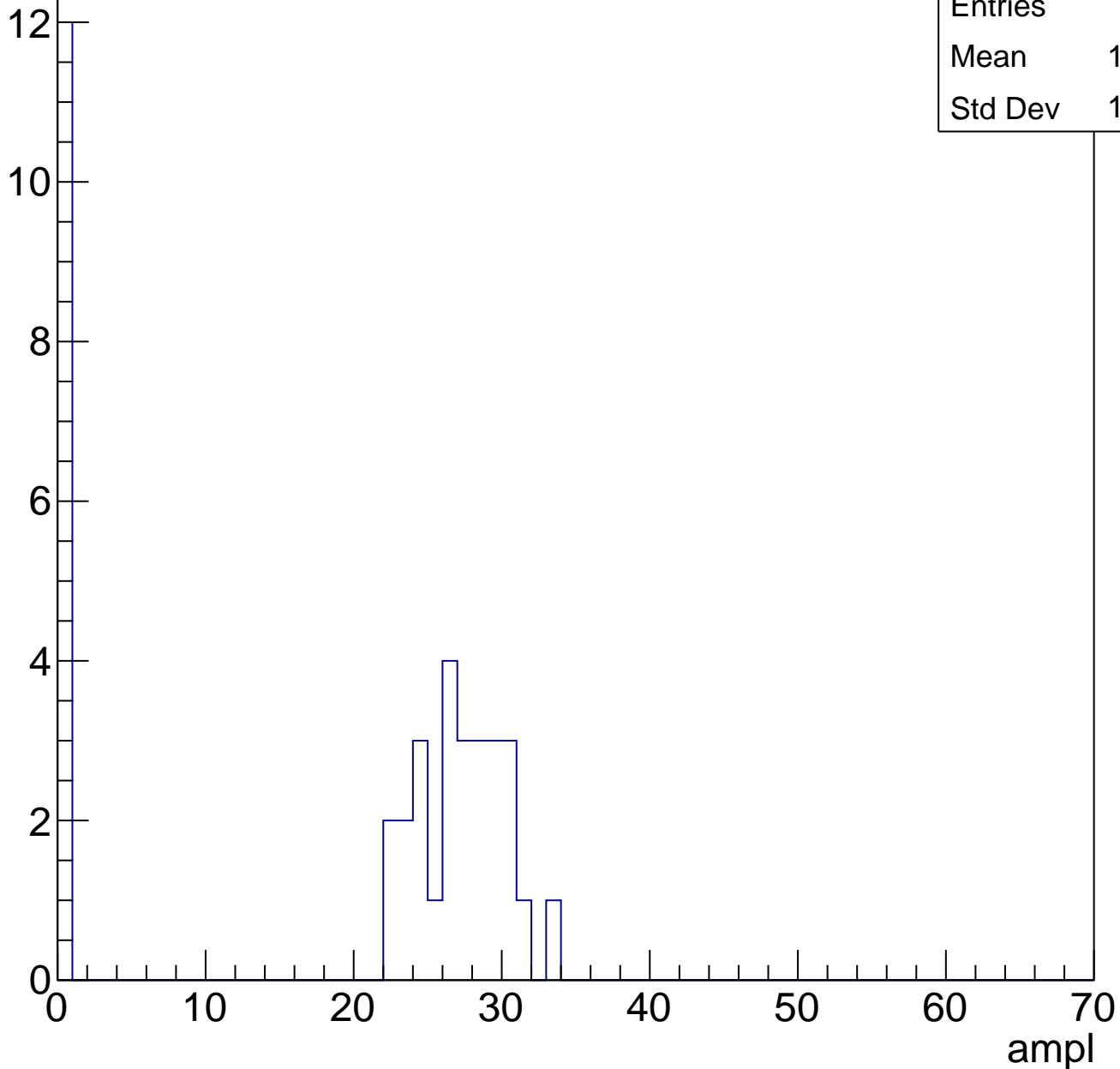


B1L103S, U14-ch117, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	38
Mean	18.34
Std Dev	12.68

Entry

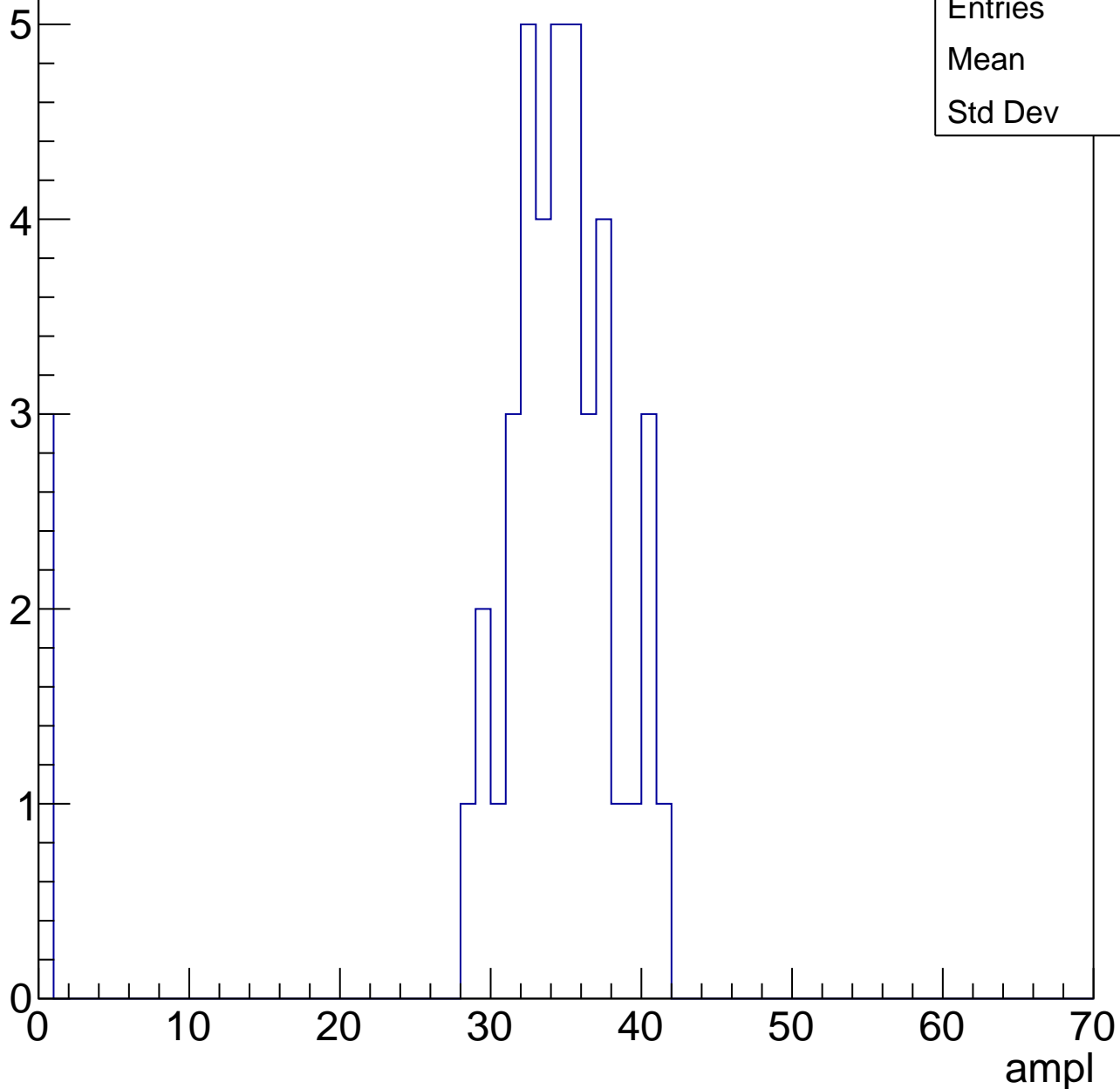


B1L103S, U14-ch117, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	42
Mean	31.9
Std Dev	9.37

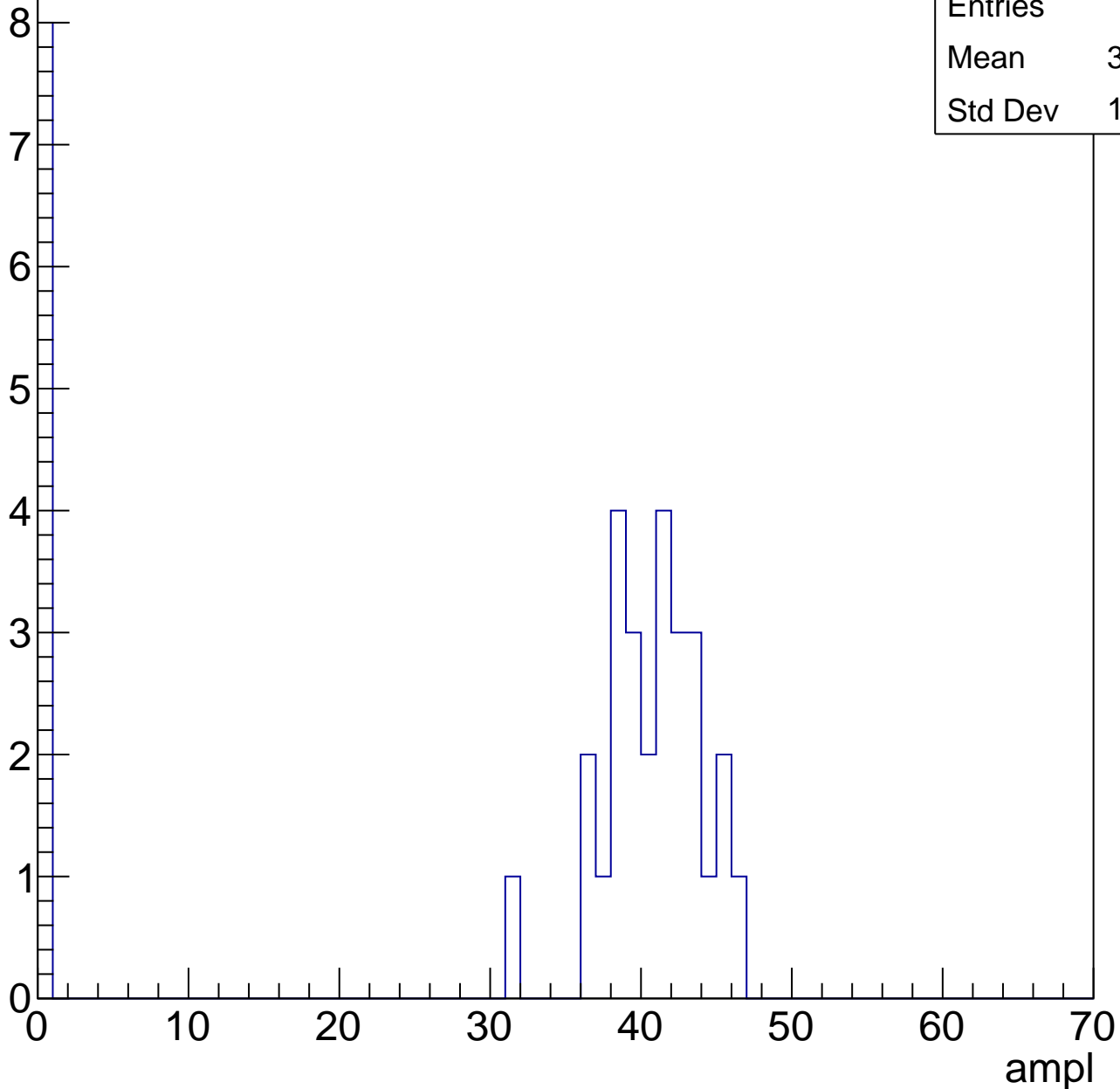


B1L103S, U14-ch117, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

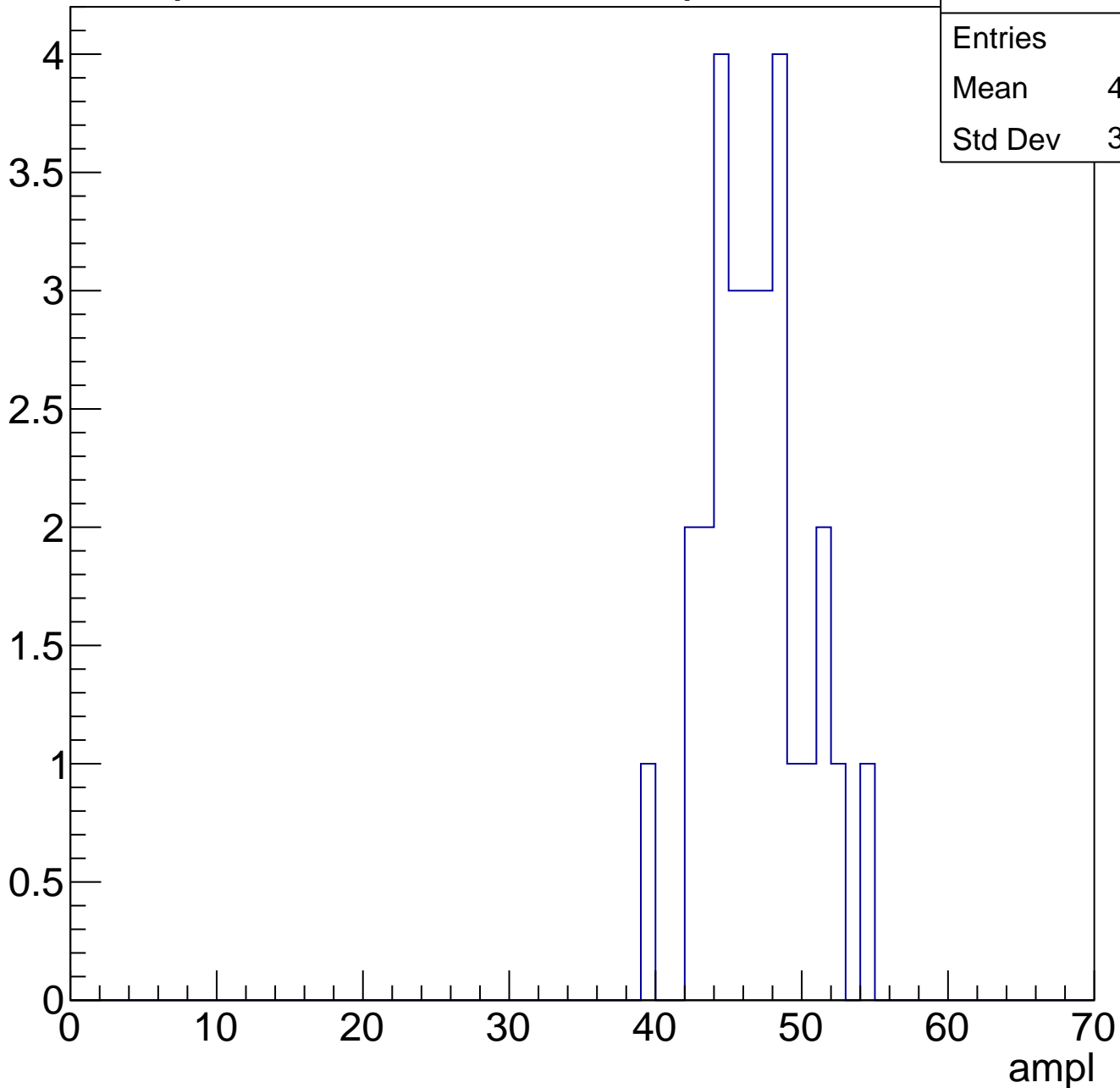
Entries	35
Mean	31.09
Std Dev	17.16



B1L103S, U14-ch117, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry



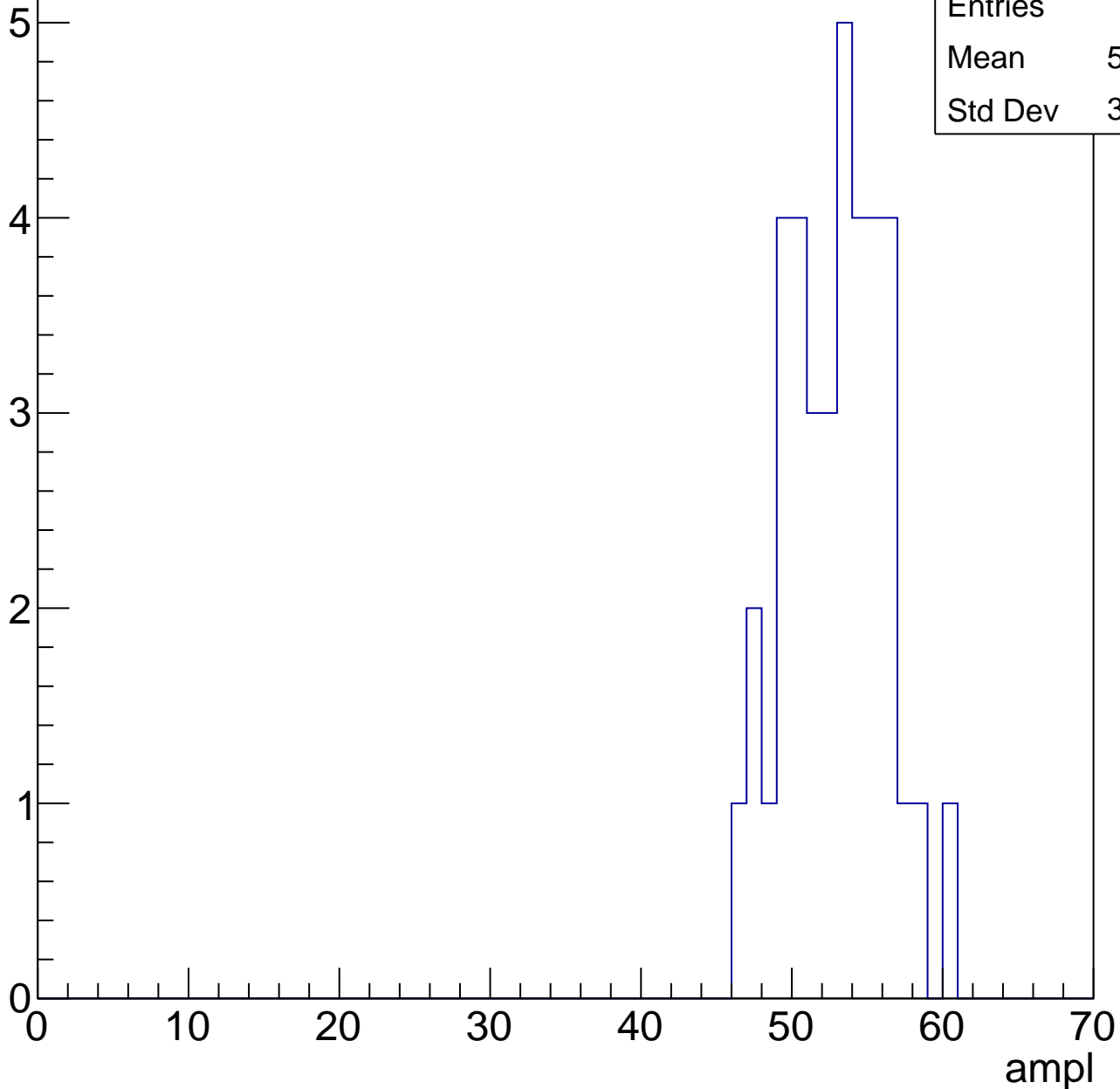
Entries	28
Mean	46.36
Std Dev	3.319

B1L103S, U14-ch117, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	38
Mean	52.45
Std Dev	3.226

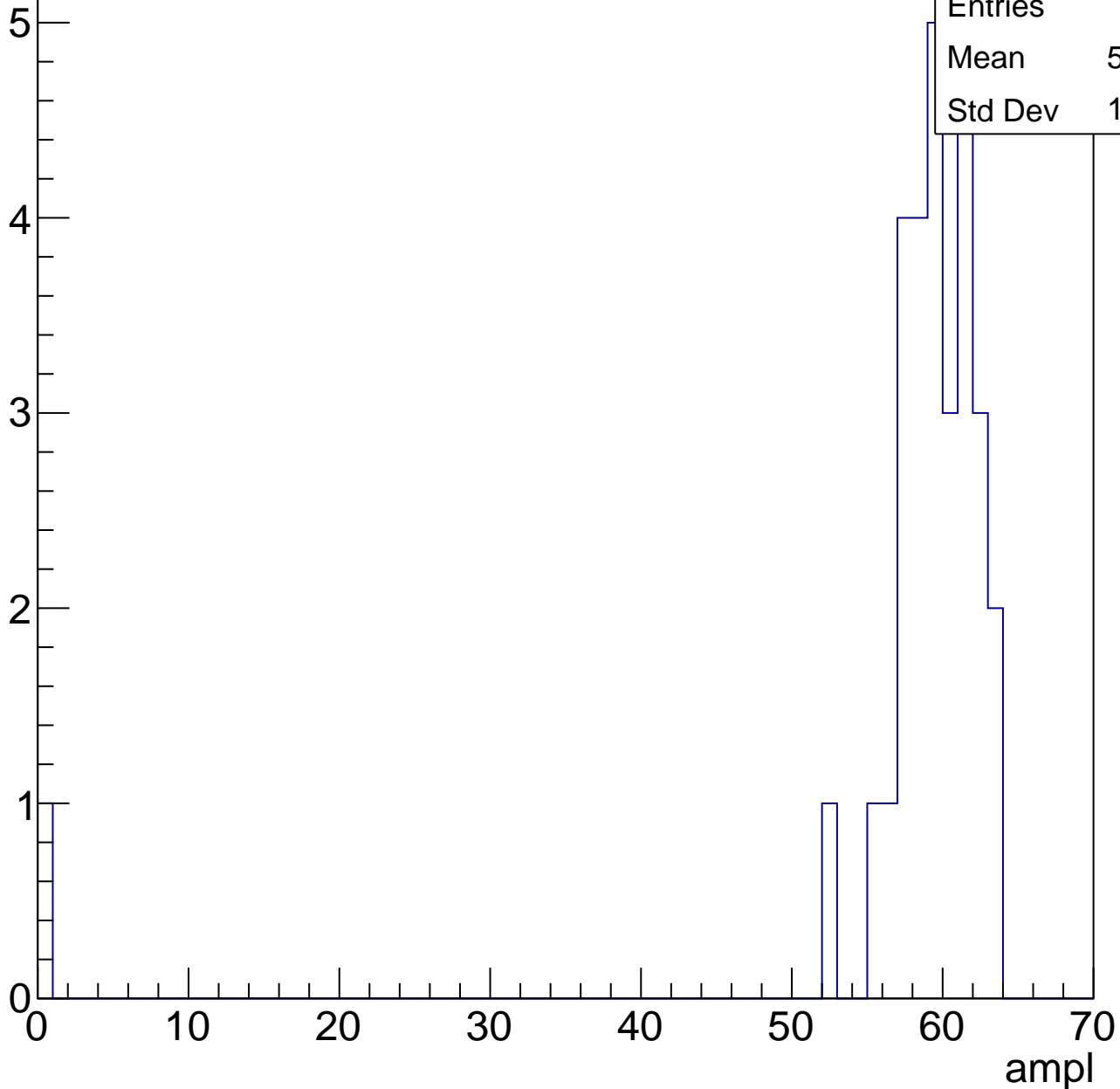


B1L103S, U14-ch117, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	30
Mean	57.17
Std Dev	10.89



B1L103S, U14-ch117, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

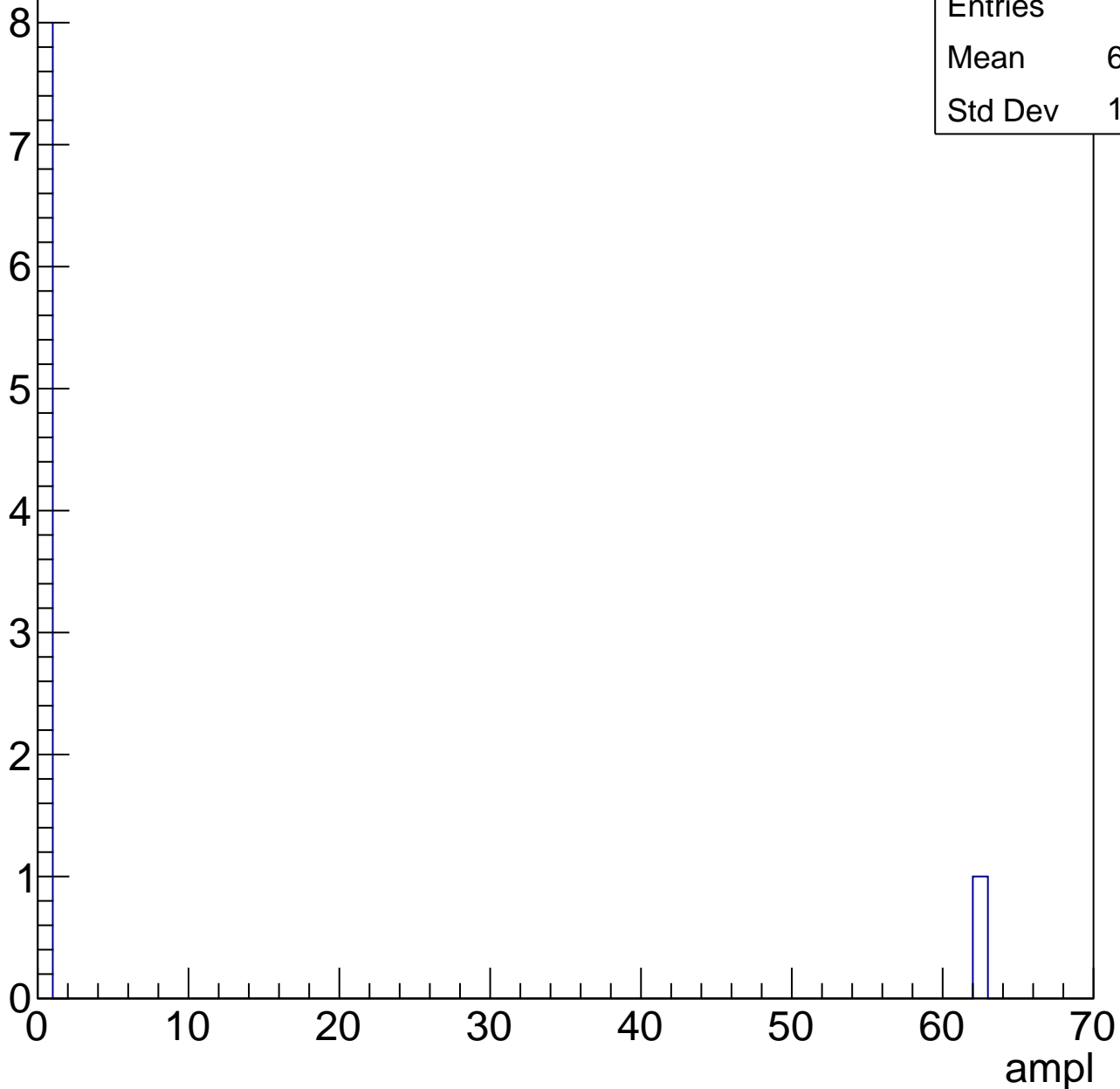


B1L103S, U14-ch117, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

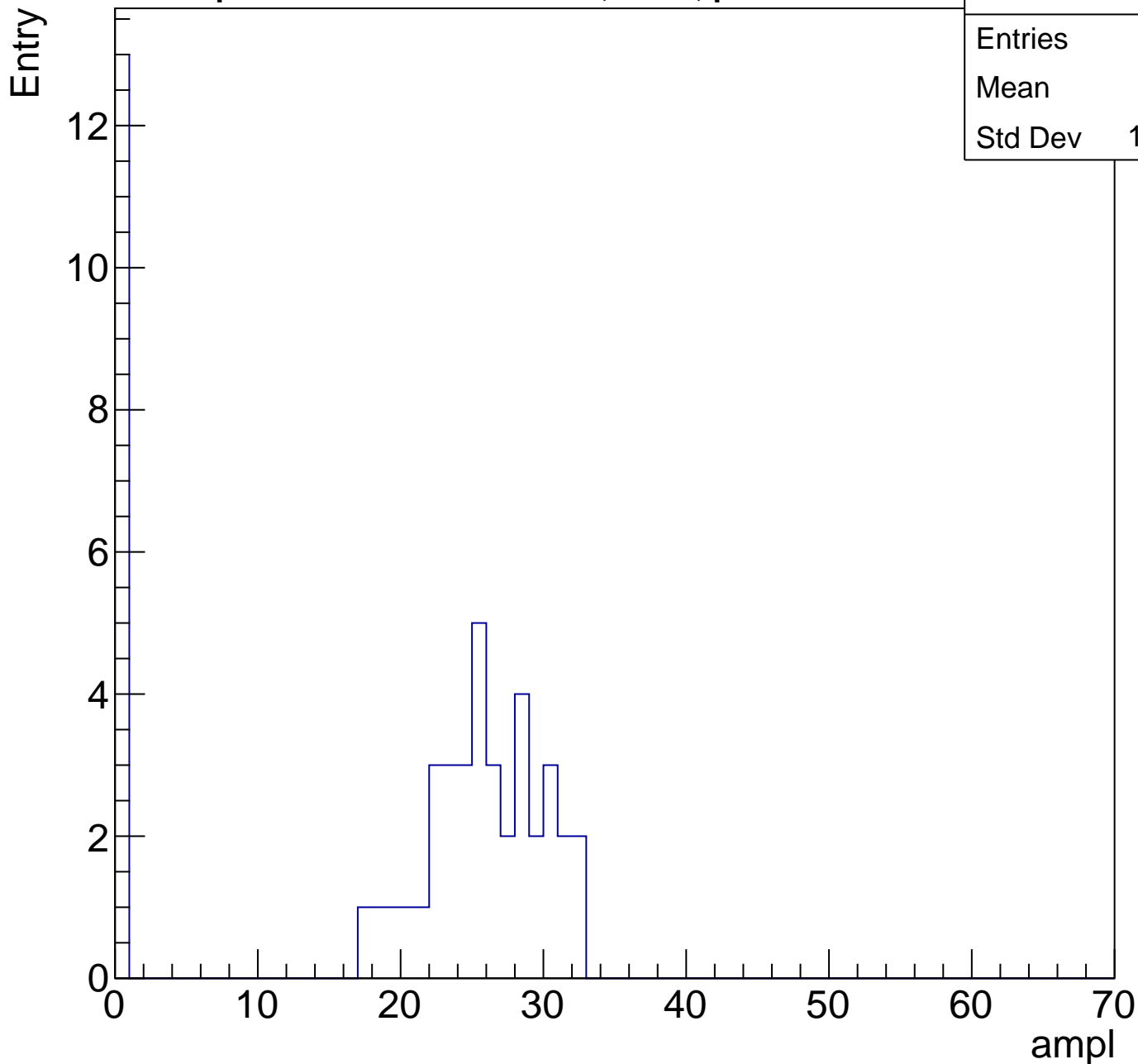
Entries	9
Mean	6.889
Std Dev	19.48



B1L103S, U14-ch118, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	50
Mean	18.9
Std Dev	11.68

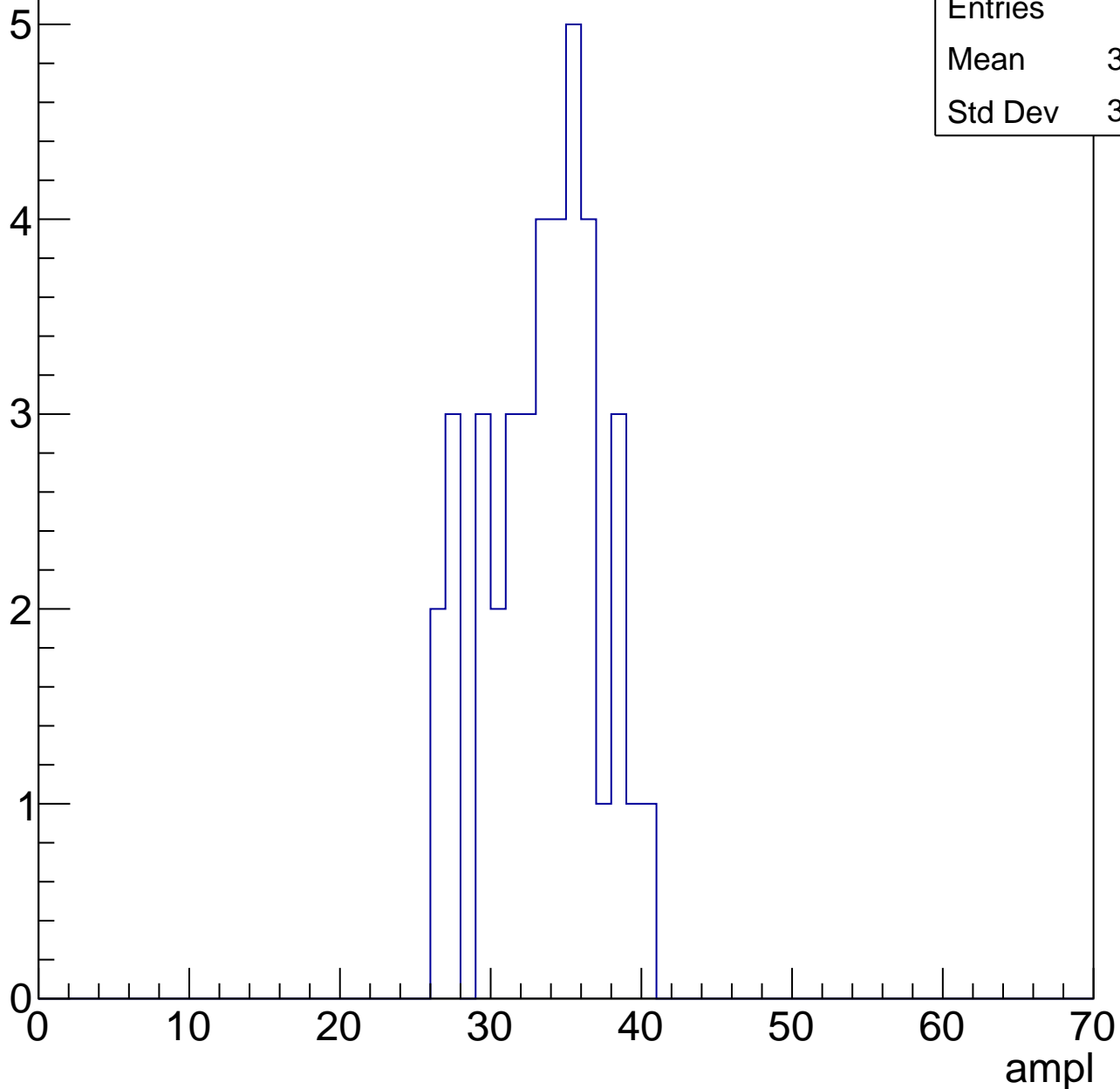


B1L103S, U14-ch118, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	32.97
Std Dev	3.662

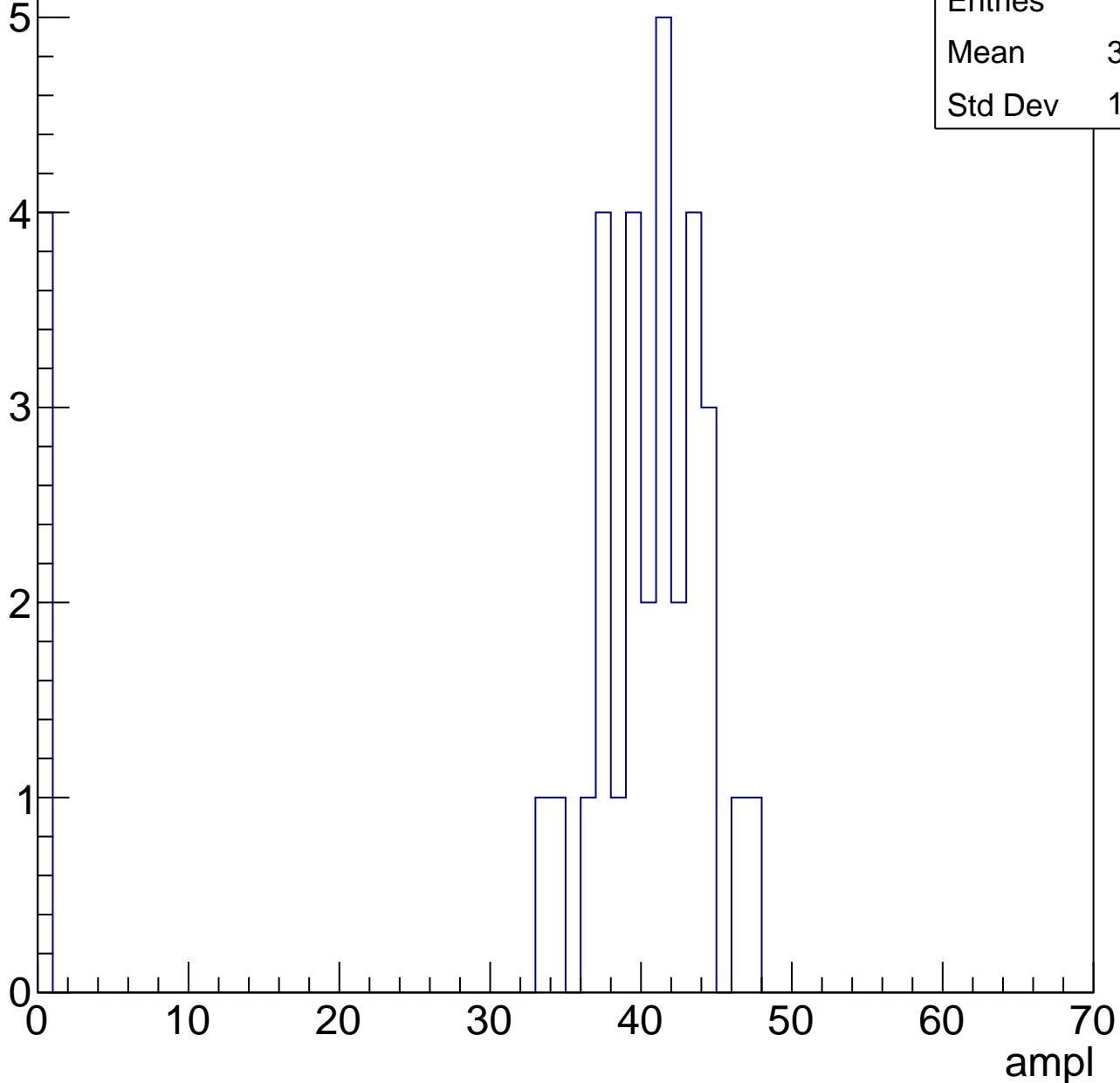


B1L103S, U14-ch118, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	34
Mean	35.62
Std Dev	13.37

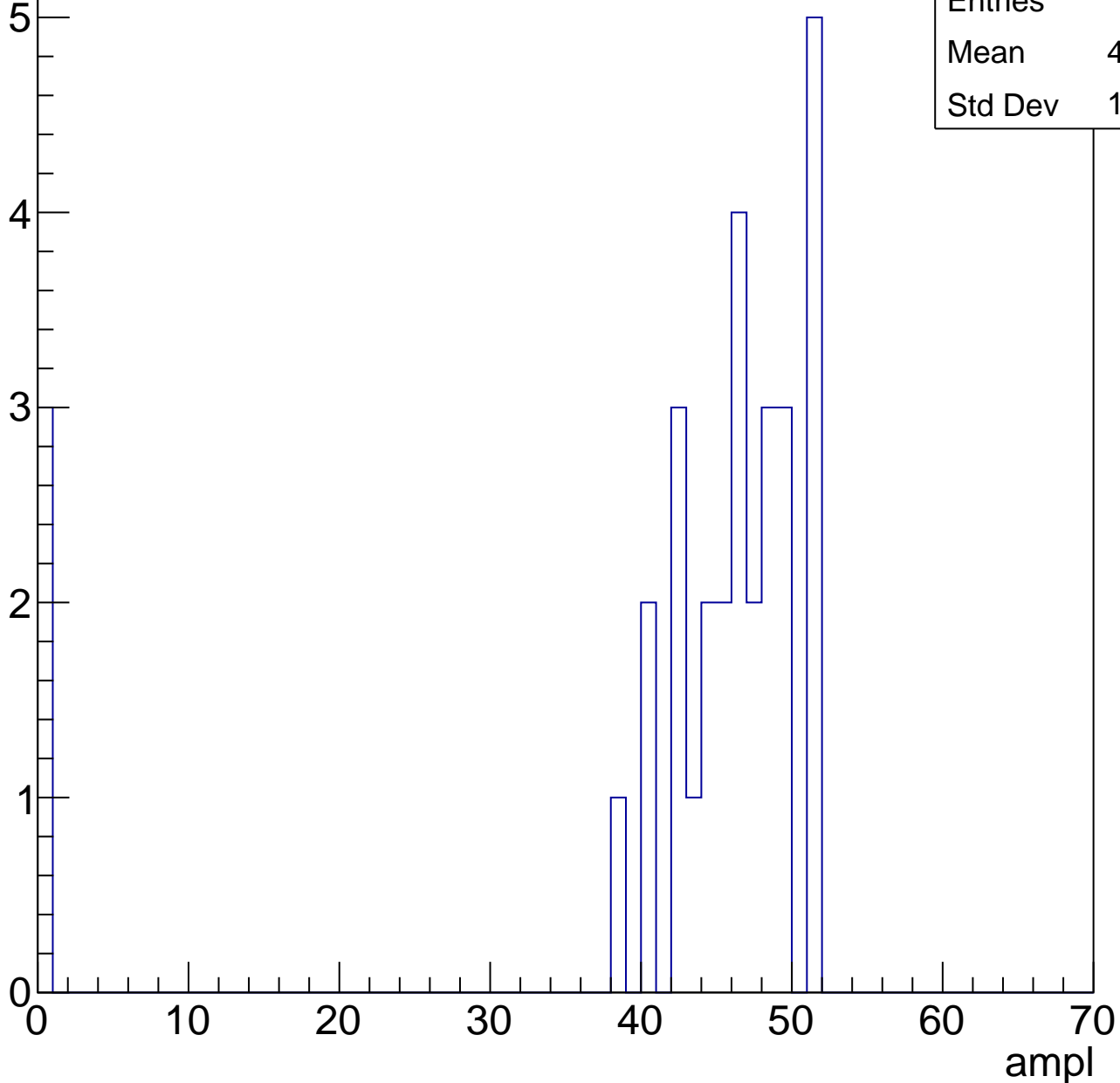


B1L103S, U14-ch118, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	31
Mean	41.58
Std Dev	14.04

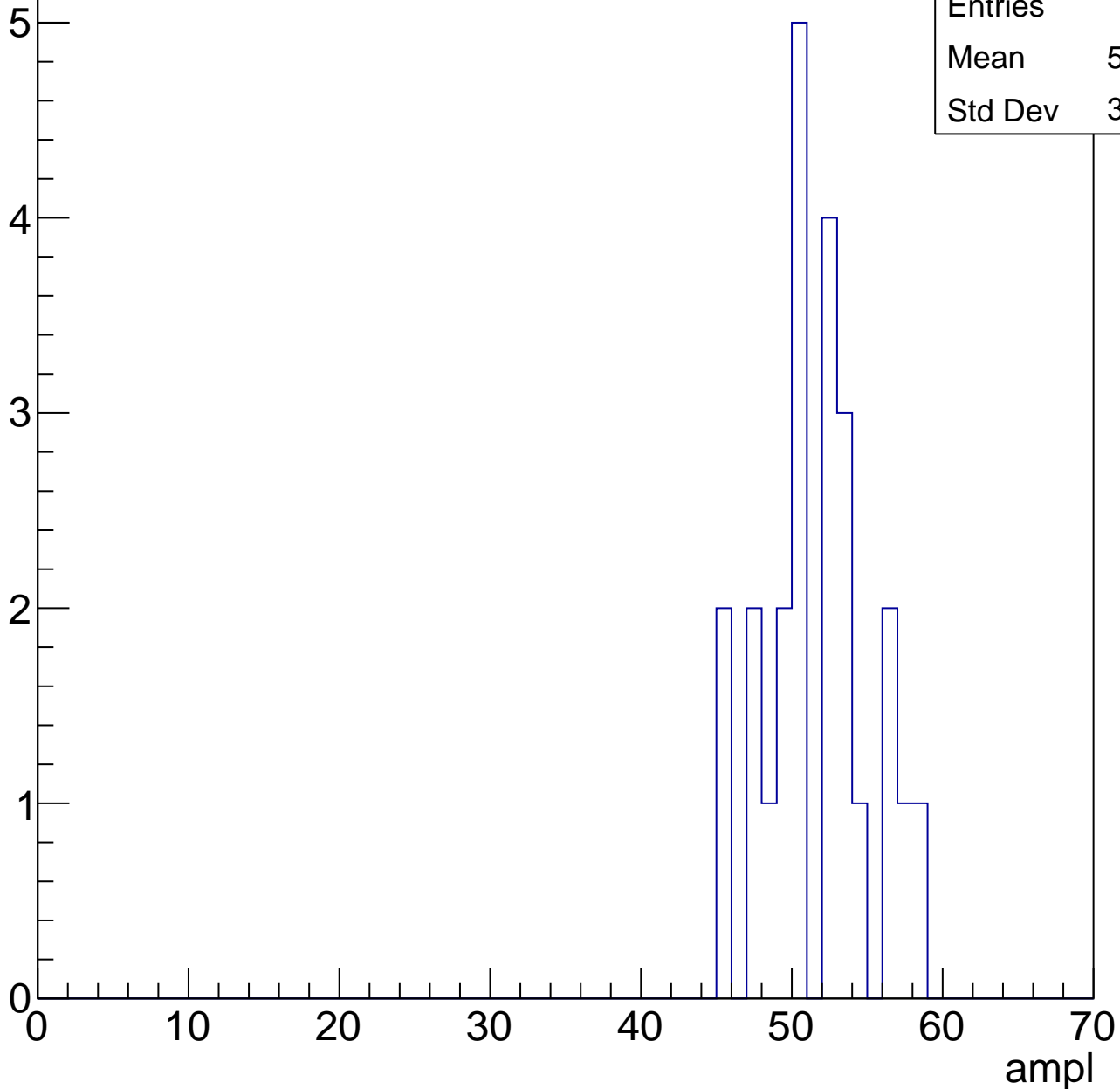


B1L103S, U14-ch118, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	24
Mean	51.17
Std Dev	3.448

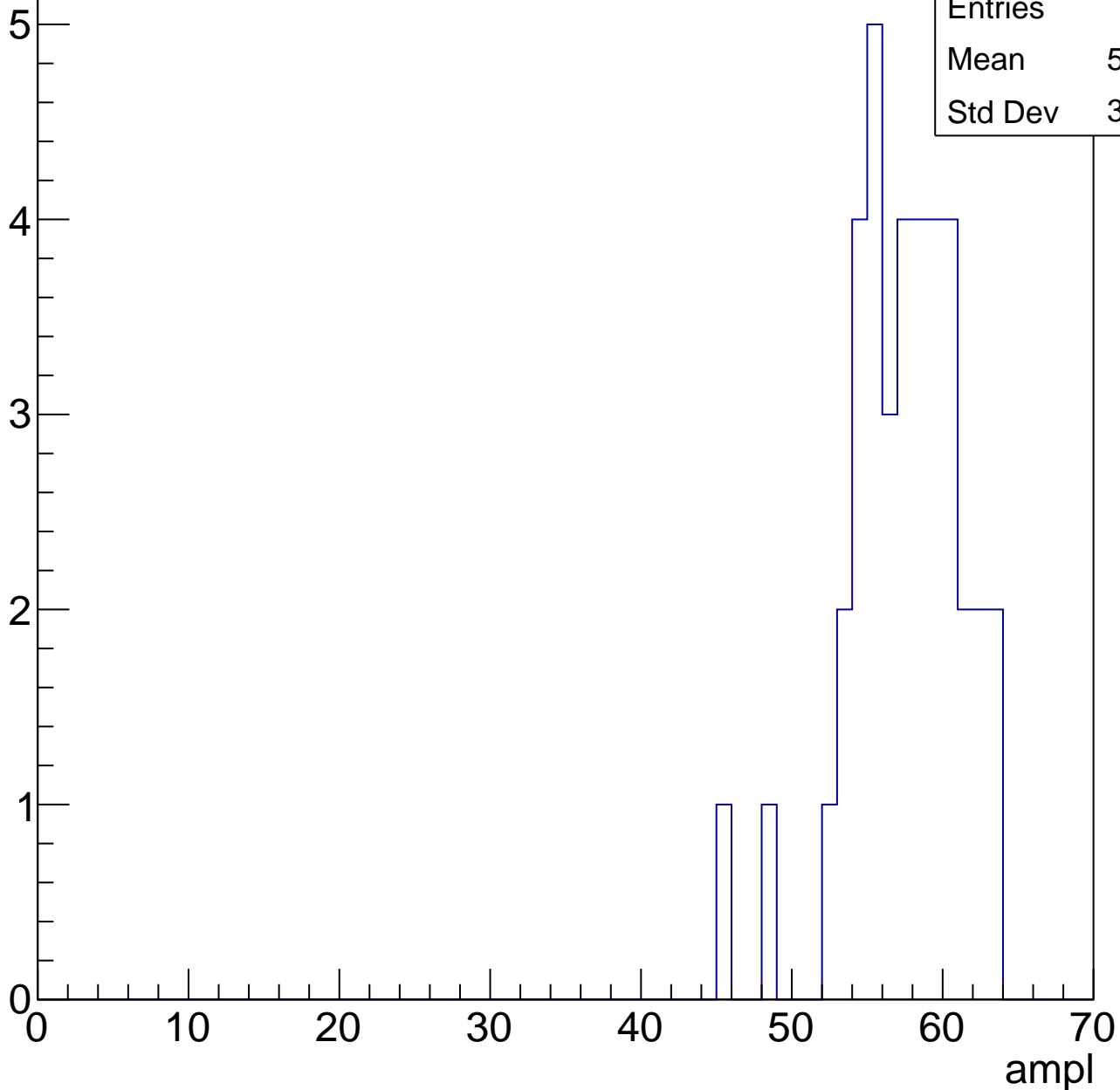


B1L103S, U14-ch118, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	56.87
Std Dev	3.757



B1L103S, U14-ch118, adc6

calib_packv5_041523_1651.root, FC#0, port C2

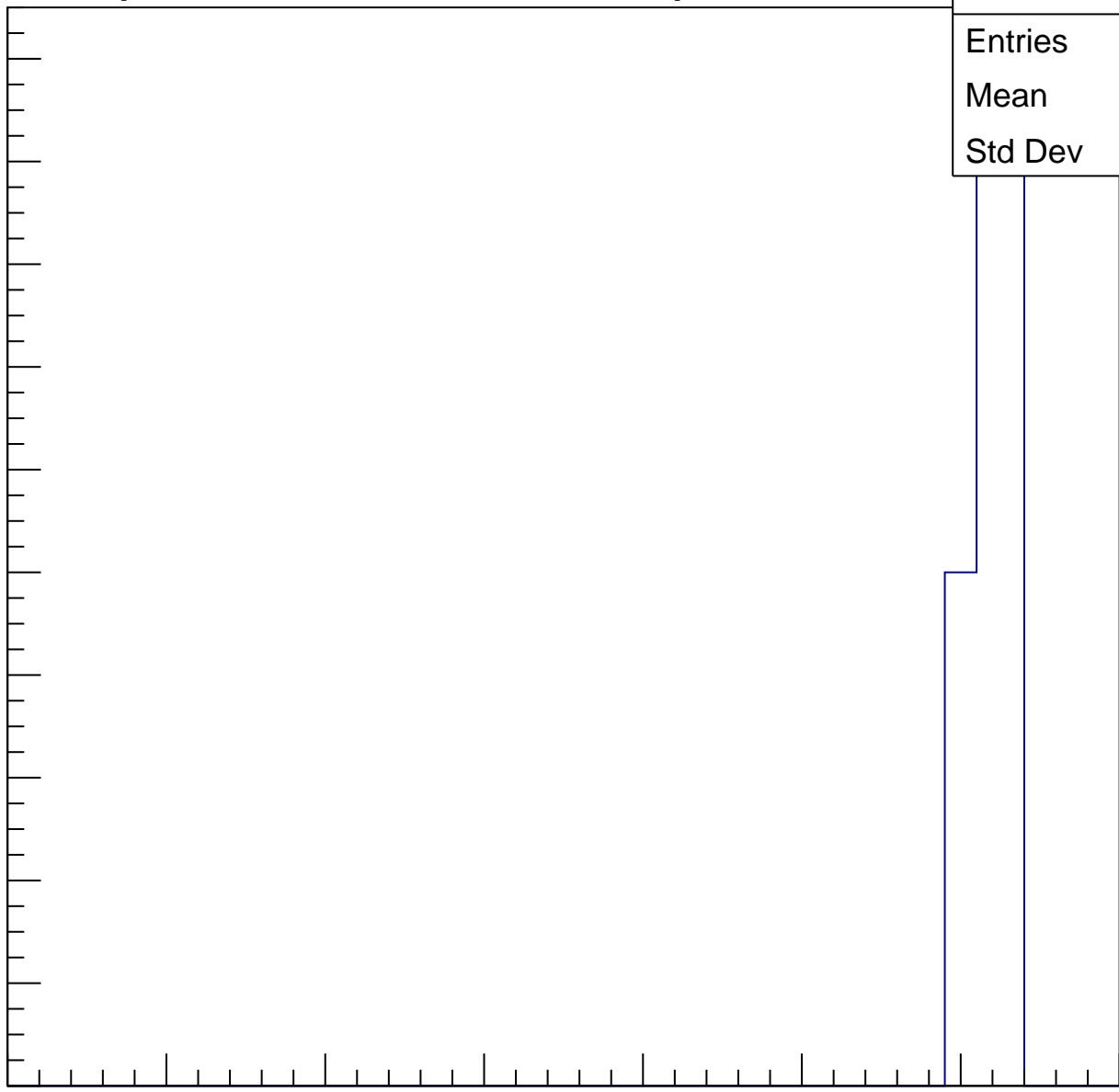
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	8
Mean	61.38
Std Dev	1.317

0 10 20 30 40 50 60 70

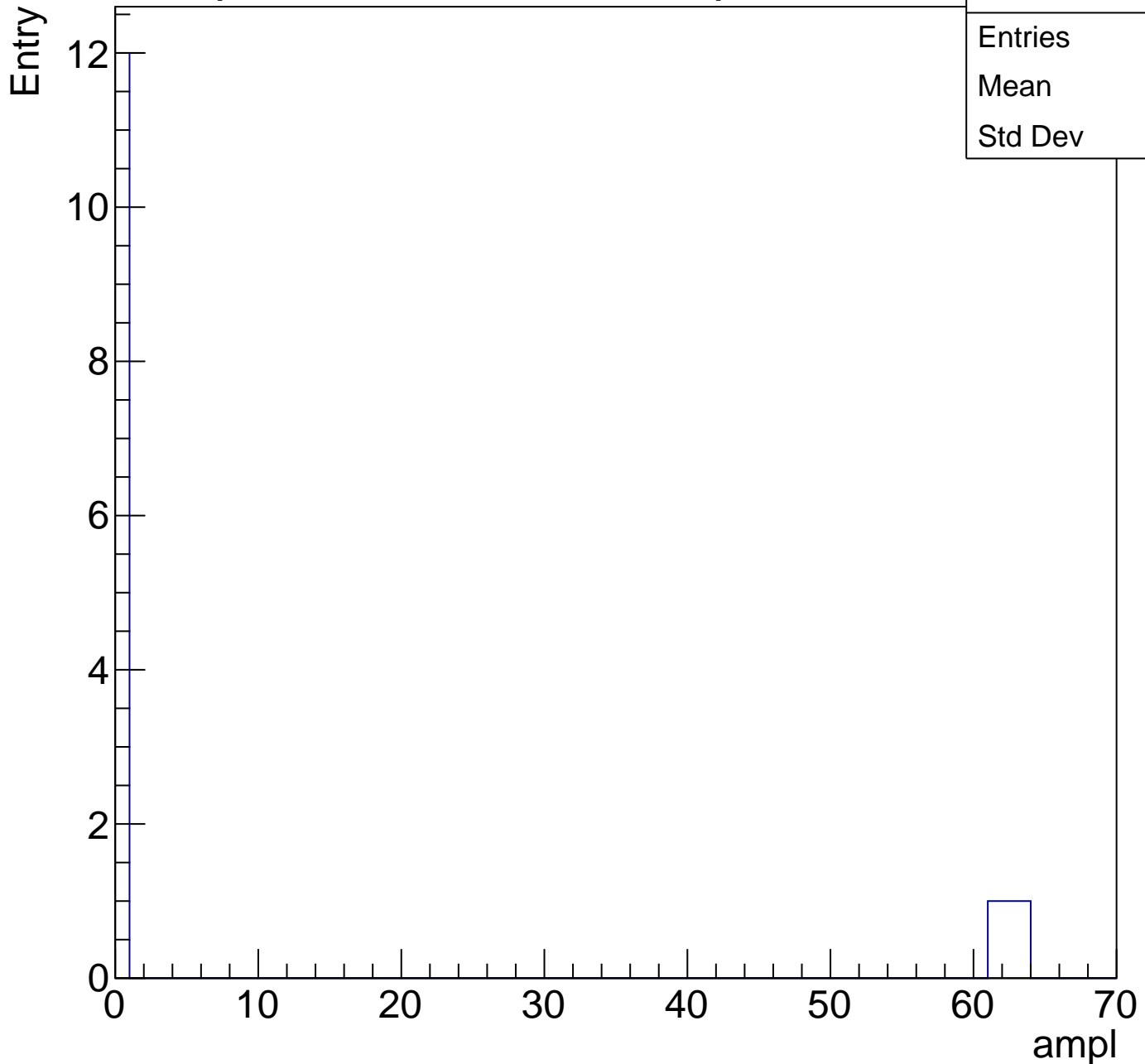
ampl



B1L103S, U14-ch118, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	15
Mean	12.4
Std Dev	24.8

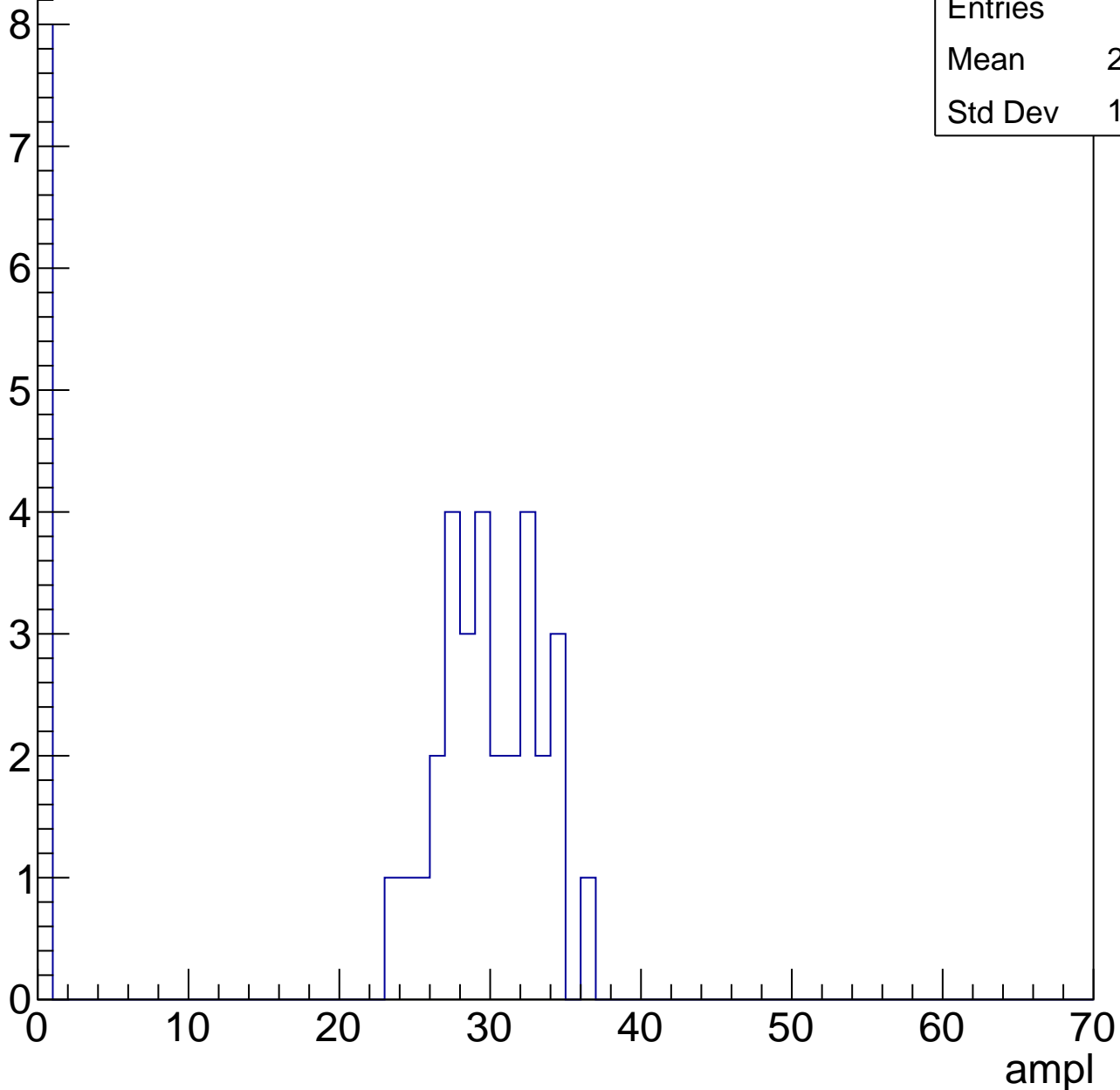


B1L103S, U14-ch119, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	38
Mean	23.32
Std Dev	12.37



B1L103S, U14-ch119, adc1

calib_packv5_041523_1651.root, FC#0, port C2

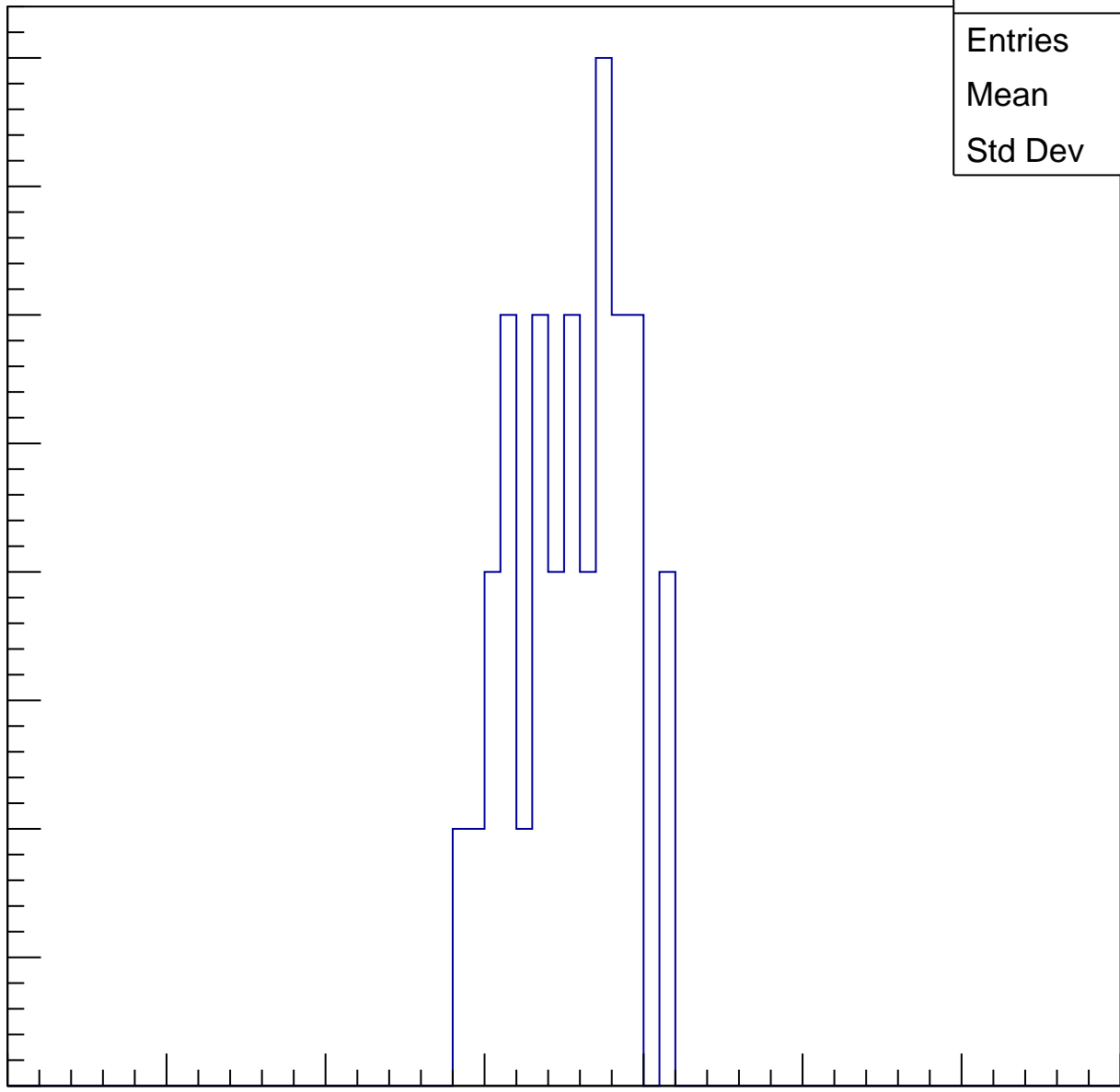
Entry

4
3.5
3
2.5
2
1.5
1
0.5
0

Entries	30
Mean	34.9
Std Dev	3.515

ampl

0 10 20 30 40 50 60 70

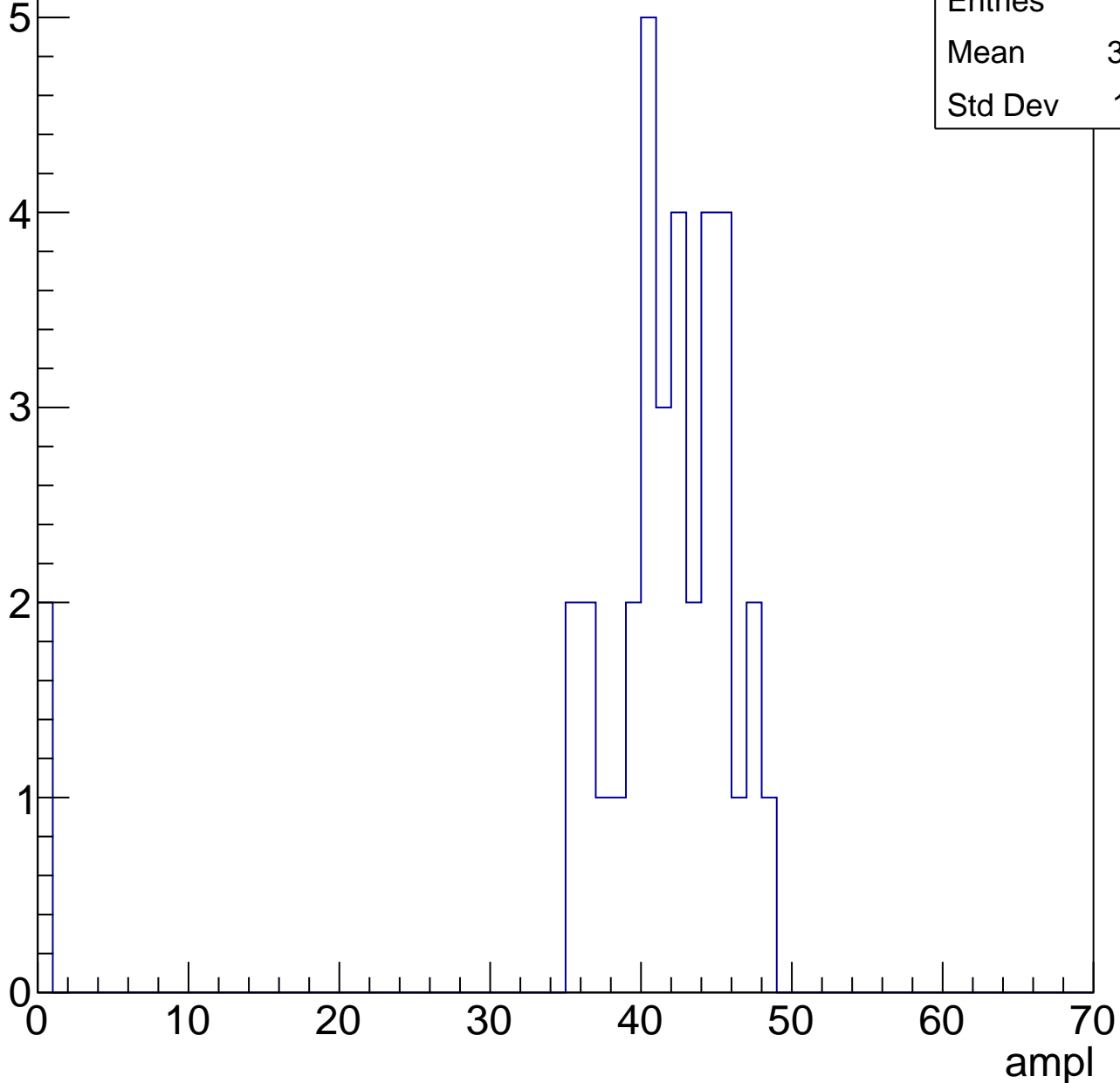


B1L103S, U14-ch119, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	36
Mean	39.33
Std Dev	10.11

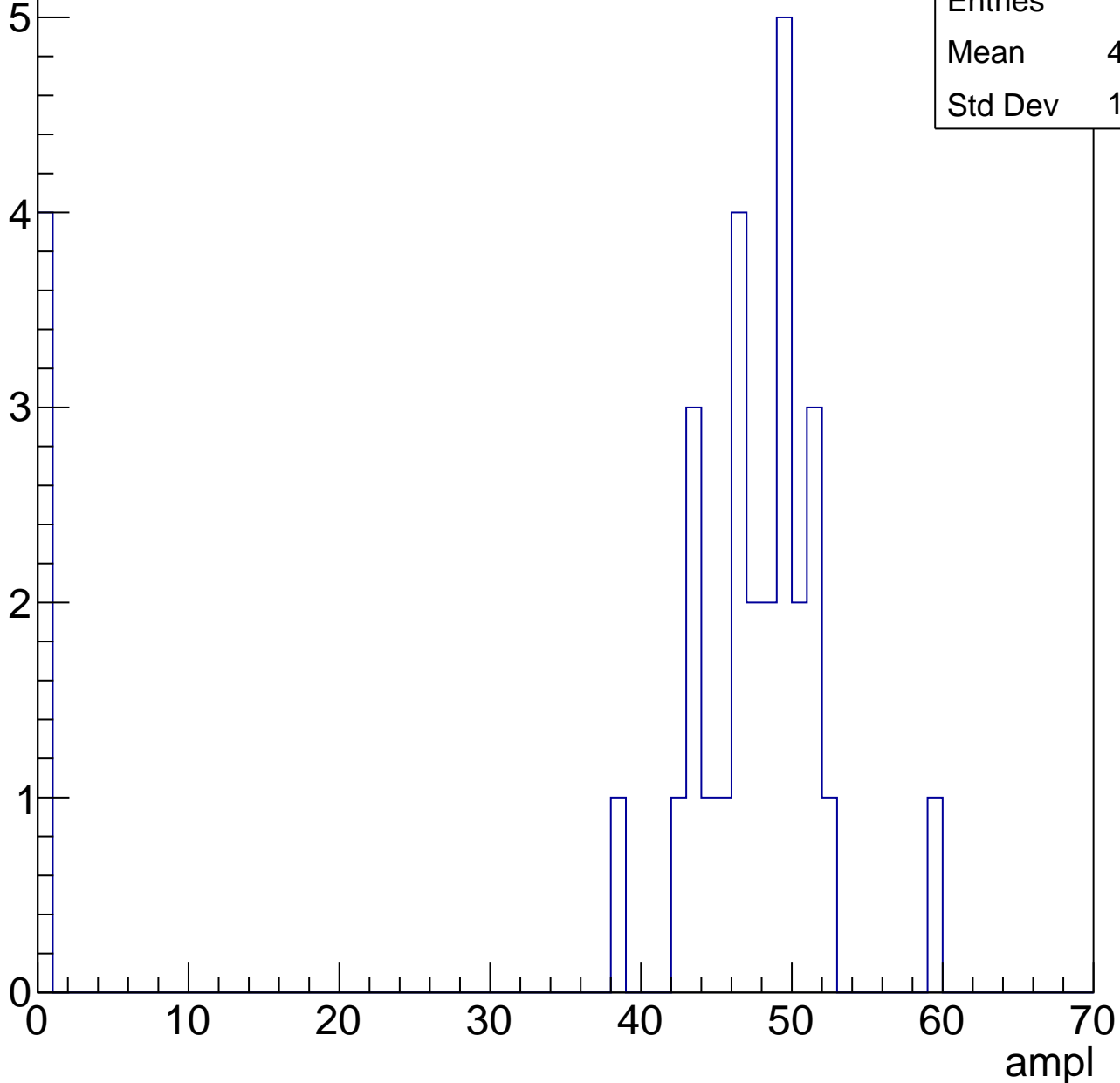


B1L103S, U14-ch119, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	31
Mean	41.32
Std Dev	16.33

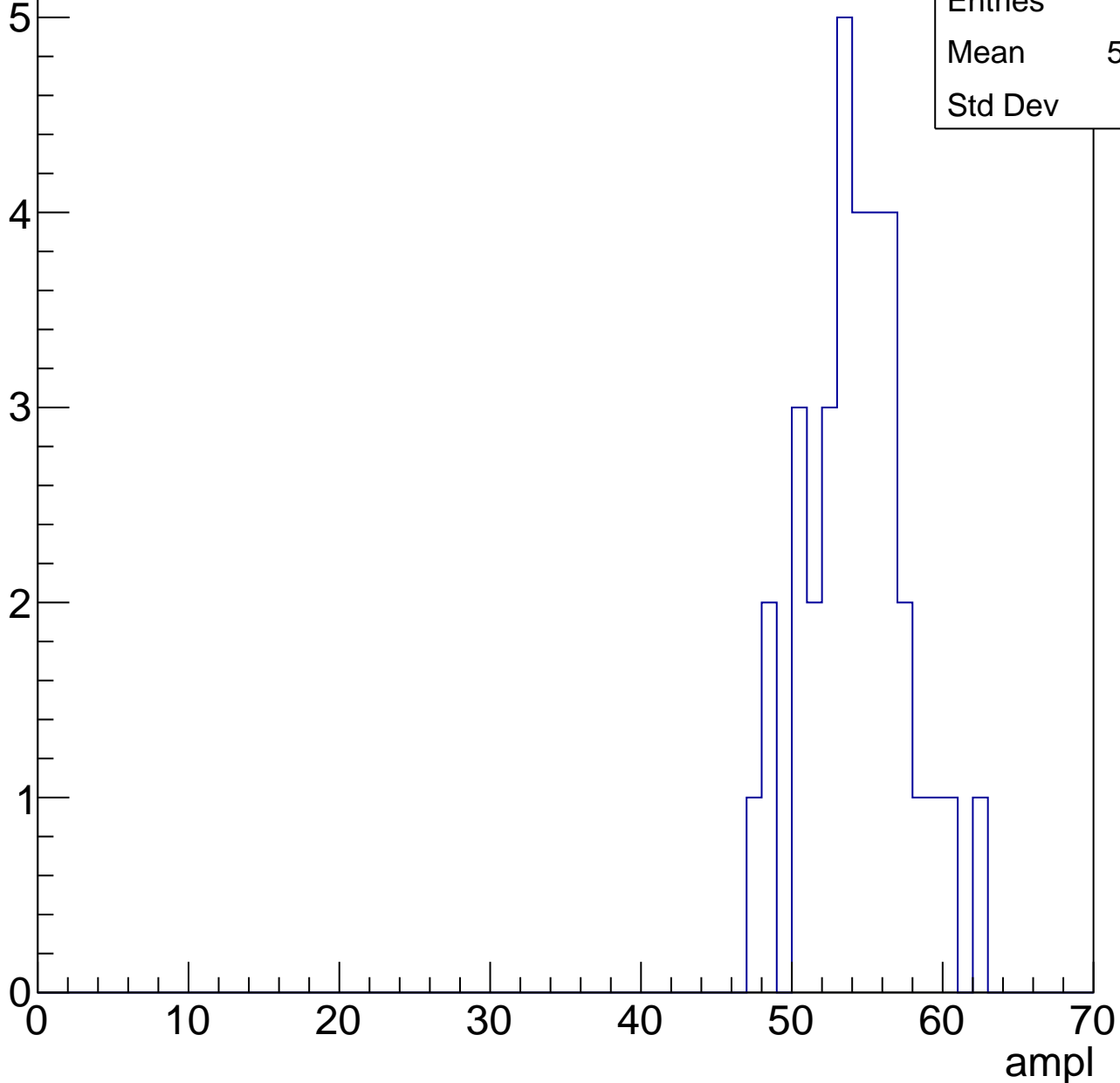


B1L103S, U14-ch119, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	34
Mean	53.79
Std Dev	3.35

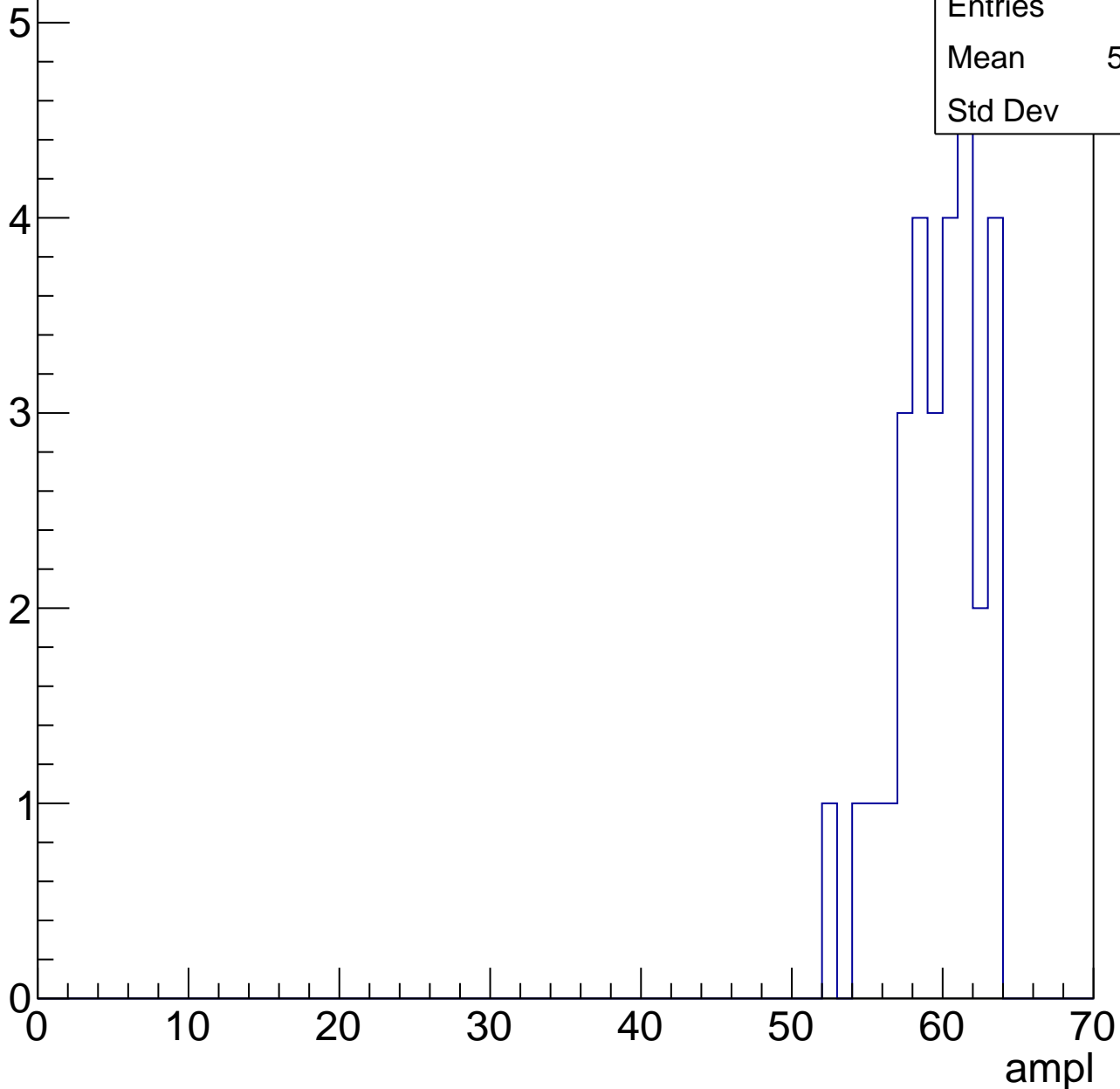


B1L103S, U14-ch119, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	29
Mean	59.24
Std Dev	2.75



B1L103S, U14-ch119, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	3
Mean	62.33
Std Dev	0.4714

ampl

B1L103S, U14-ch119, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

Entries	10
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Mean	0
------	---

Std Dev	0
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8

6

4

2

0

0

10

20

30

40

50

60

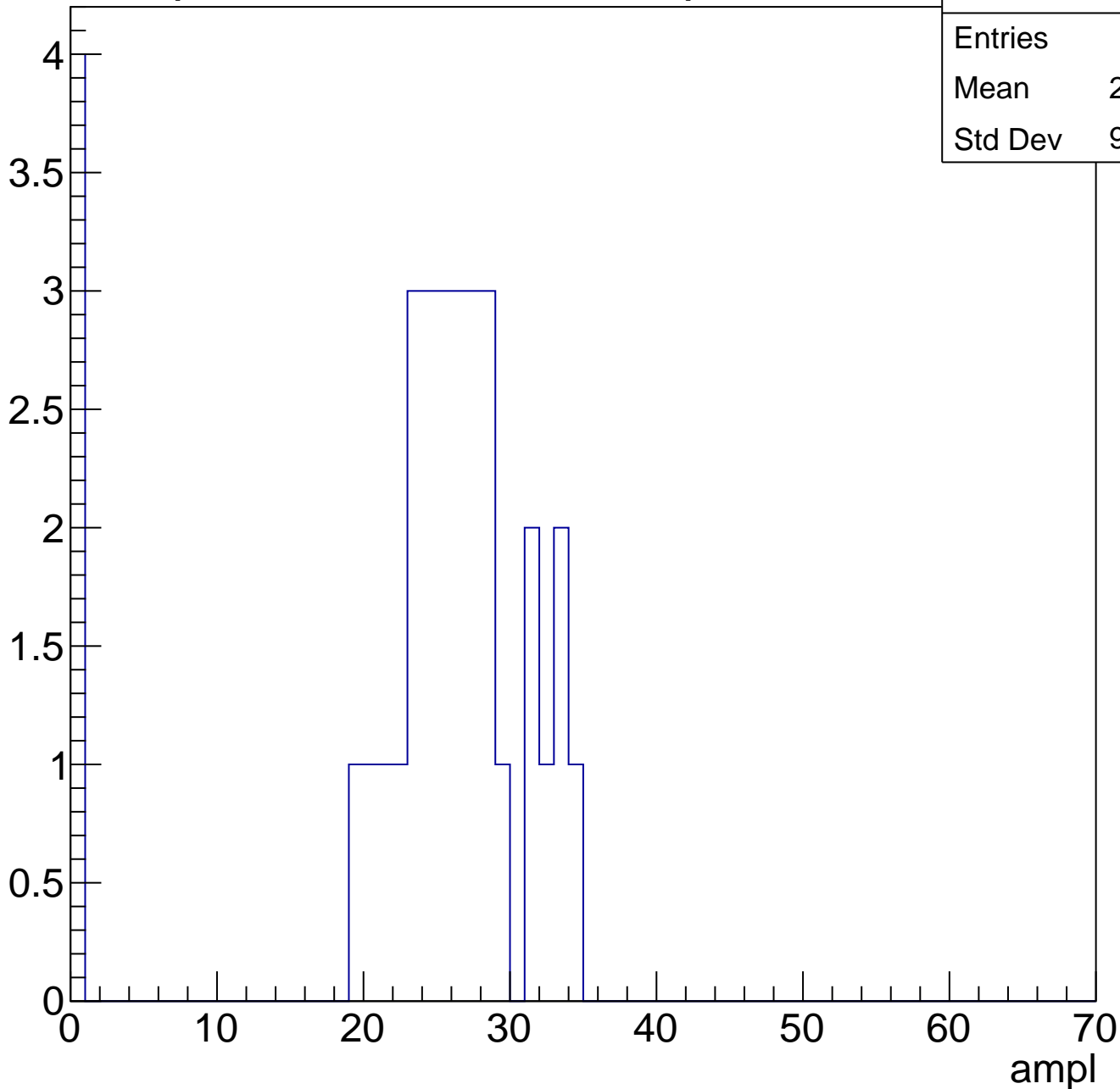
70

ampl

B1L103S, U14-ch120, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry



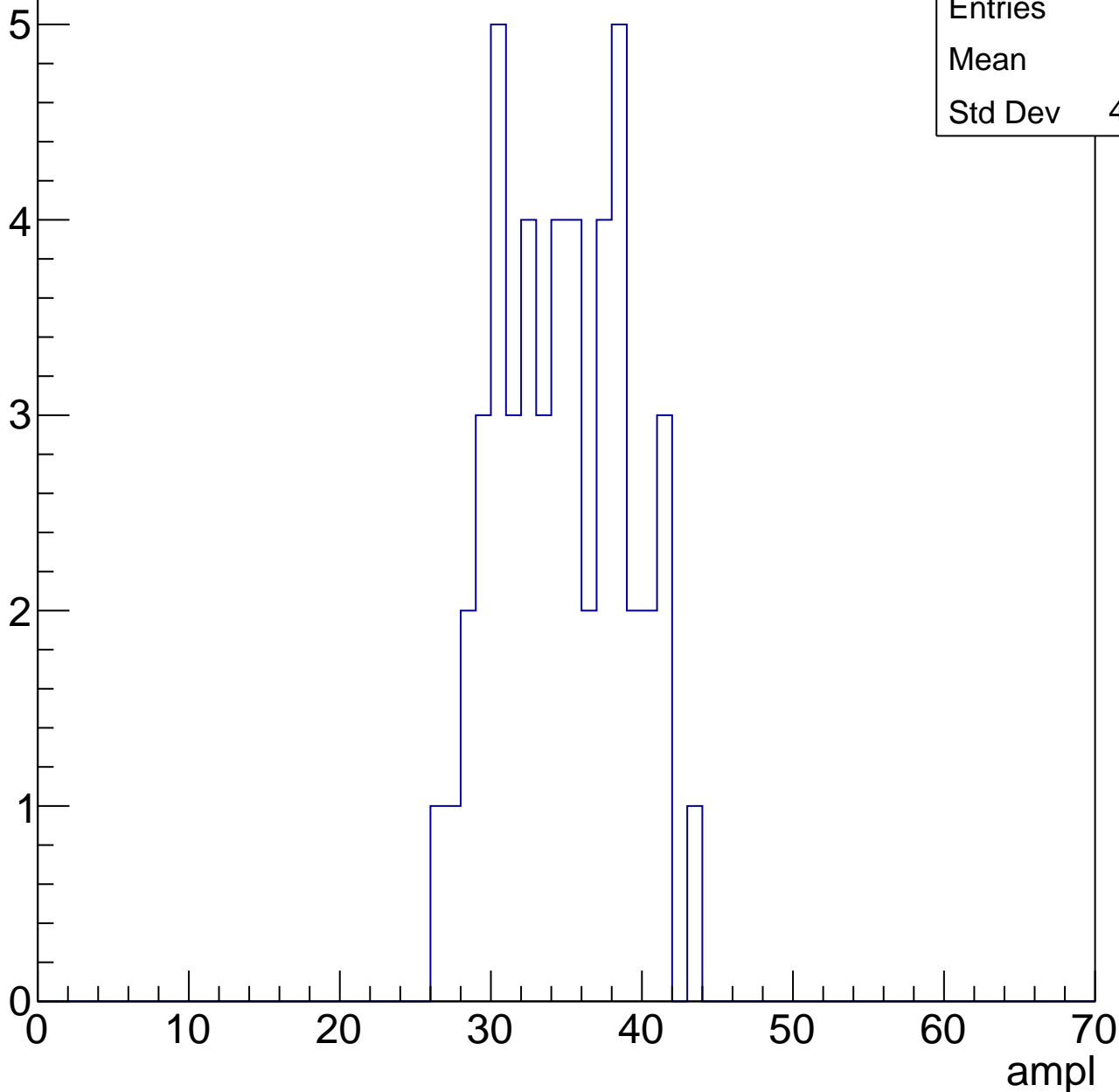
Entries	33
Mean	23.15
Std Dev	9.336

B1L103S, U14-ch120, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

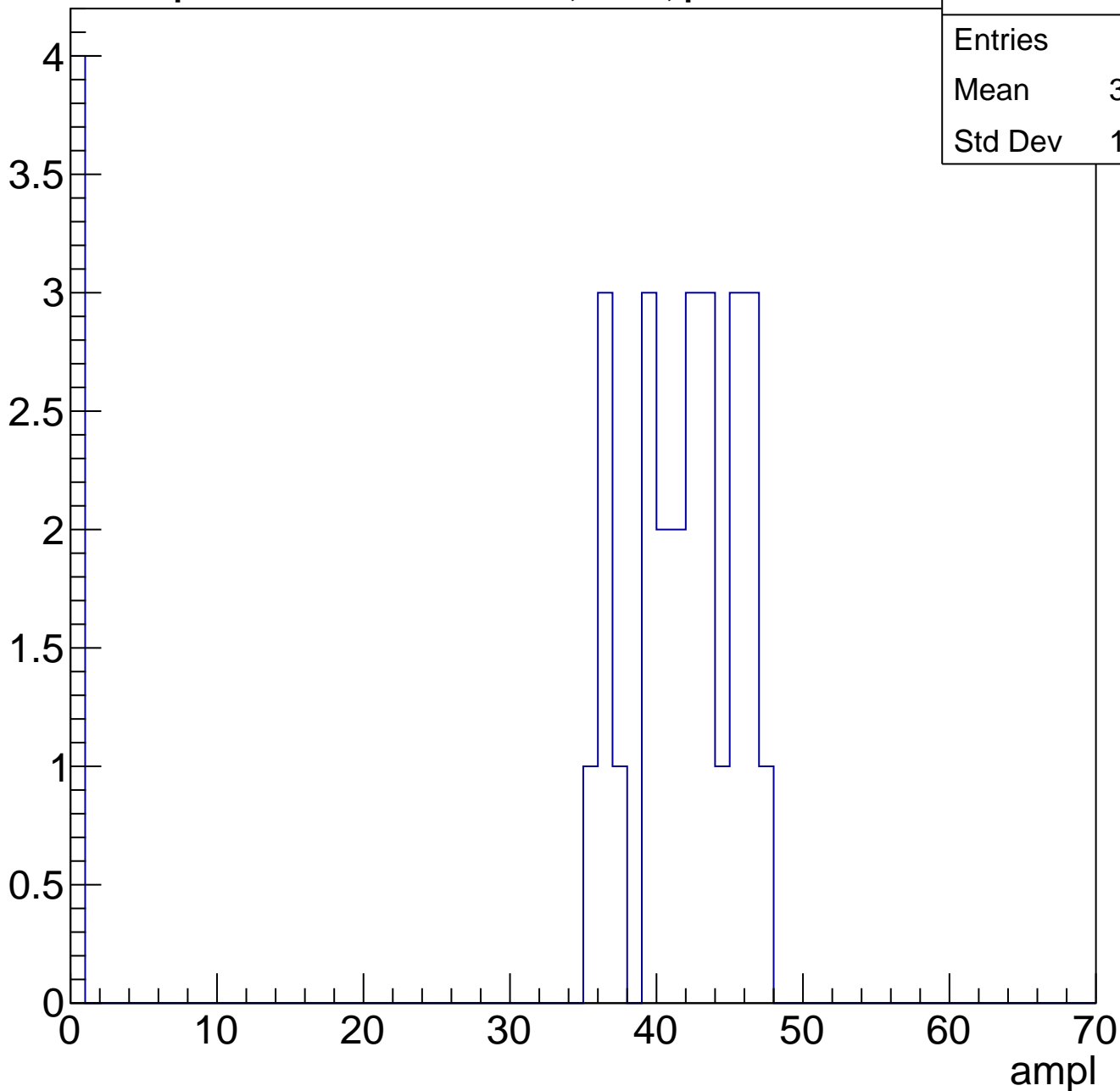
Entries	49
Mean	34.2
Std Dev	4.194



B1L103S, U14-ch120, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry



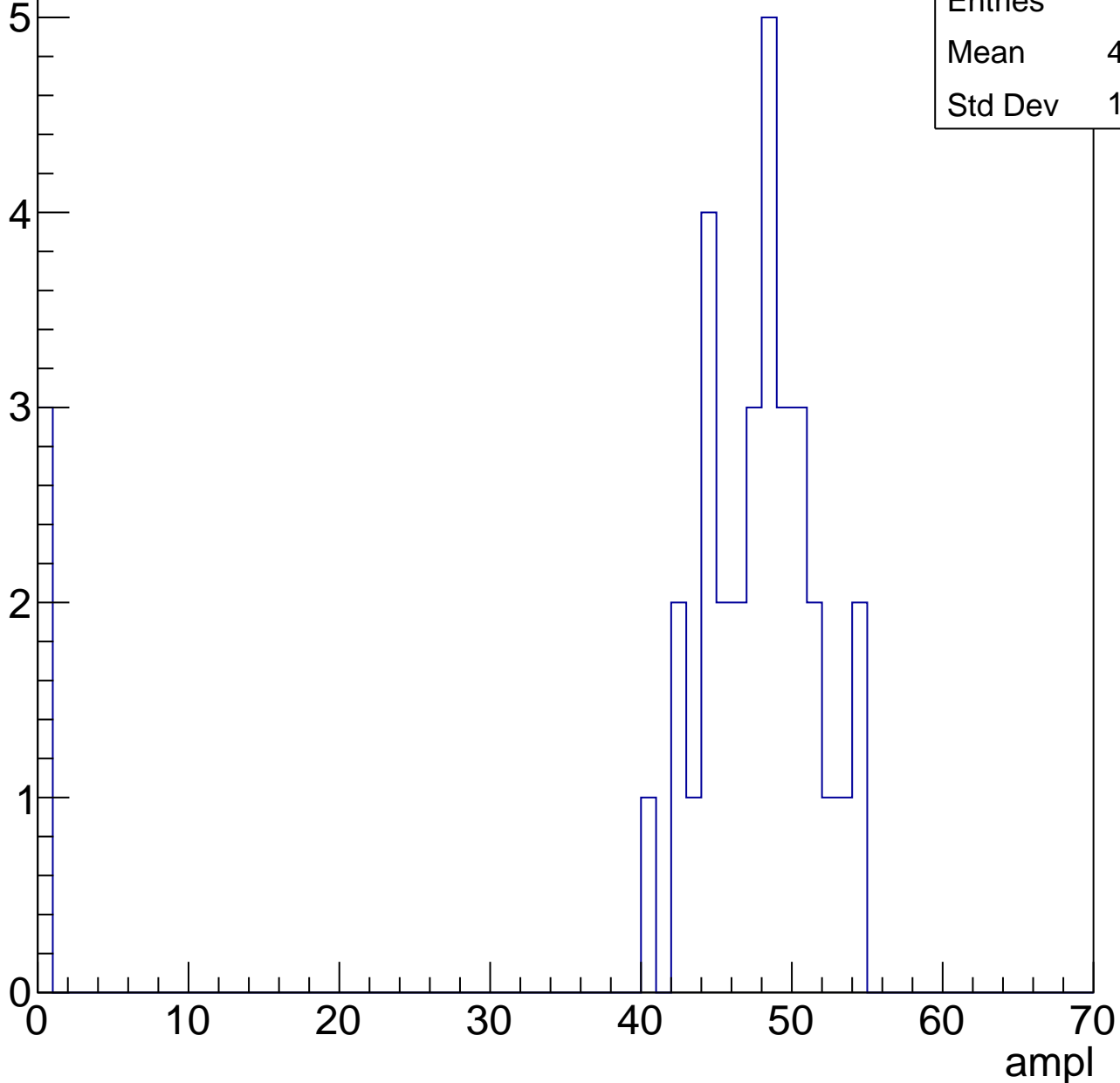
Entries	30
Mean	35.93
Std Dev	14.47

B1L103S, U14-ch120, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

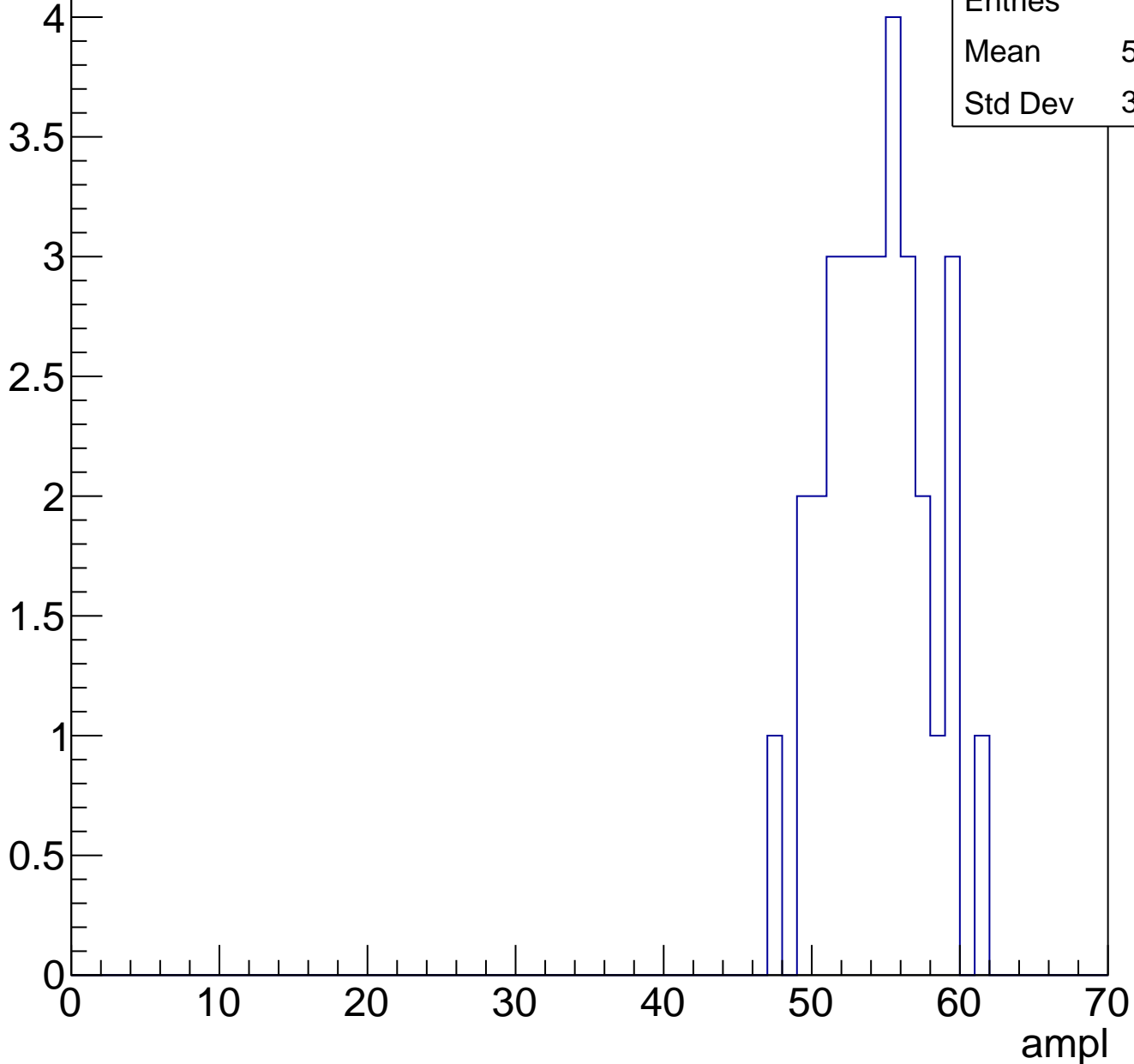
Entries	35
Mean	43.37
Std Dev	13.69



B1L103S, U14-ch120, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

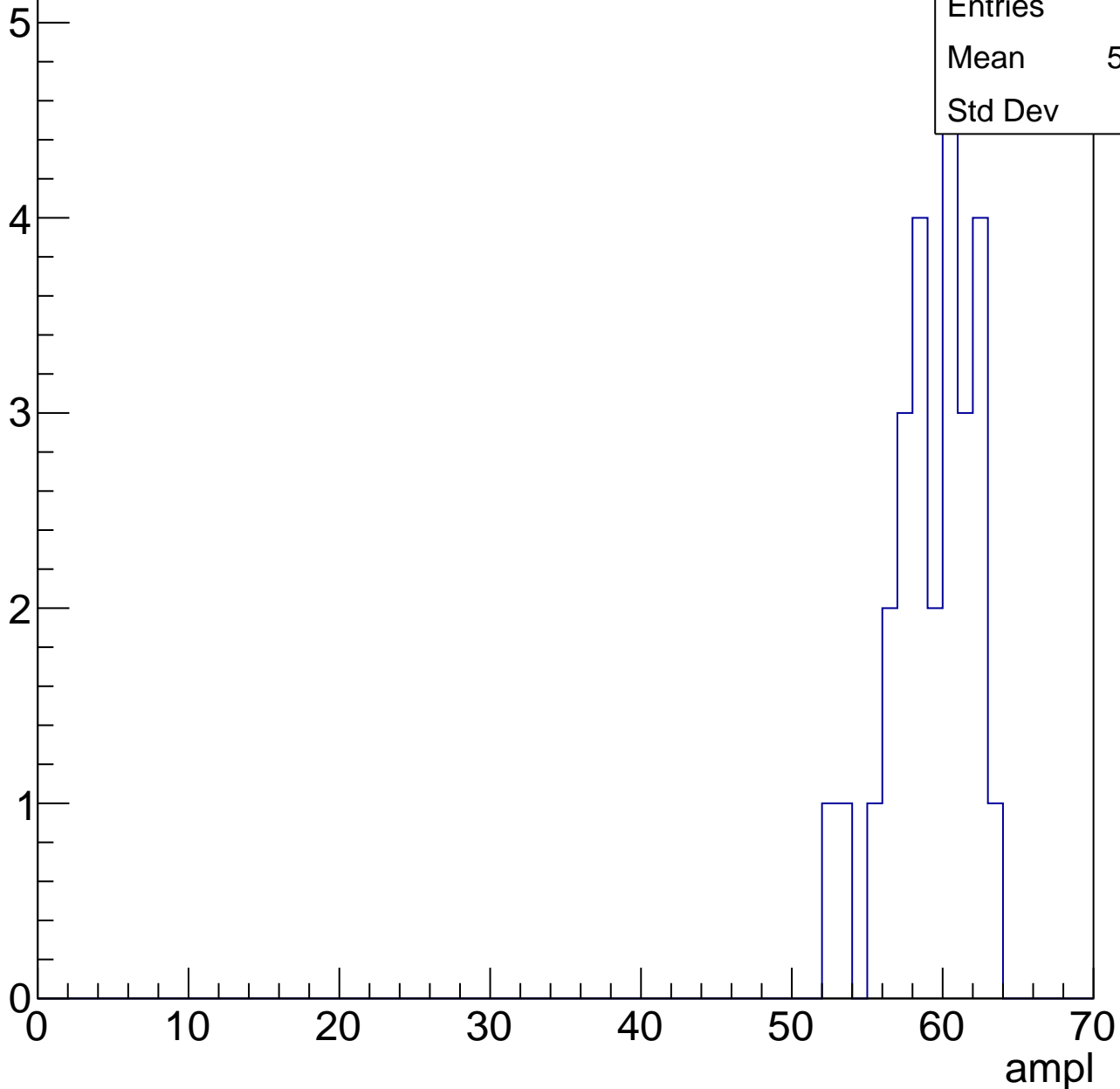


B1L103S, U14-ch120, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

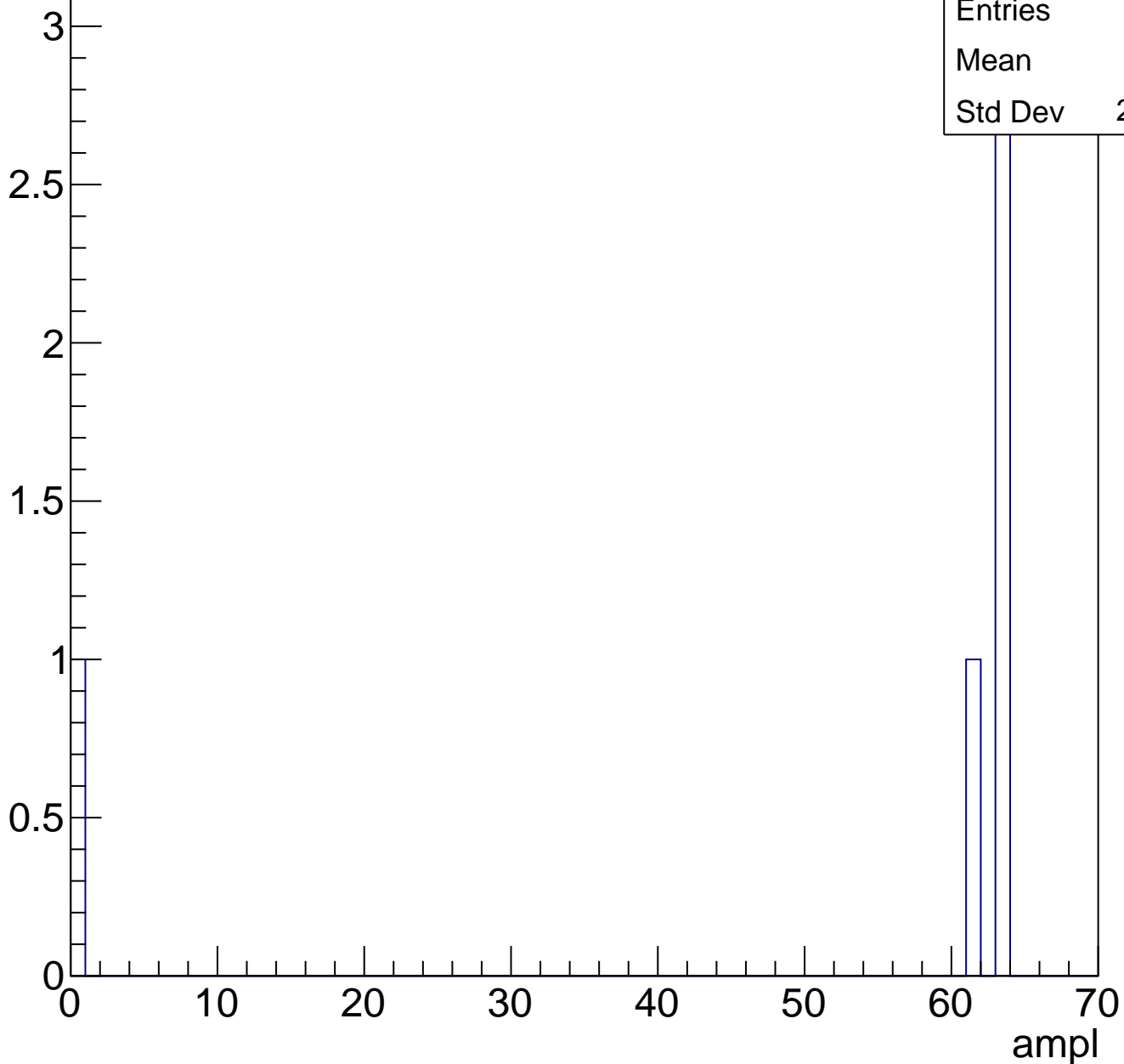
Entries	27
Mean	58.78
Std Dev	2.74



B1L103S, U14-ch120, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

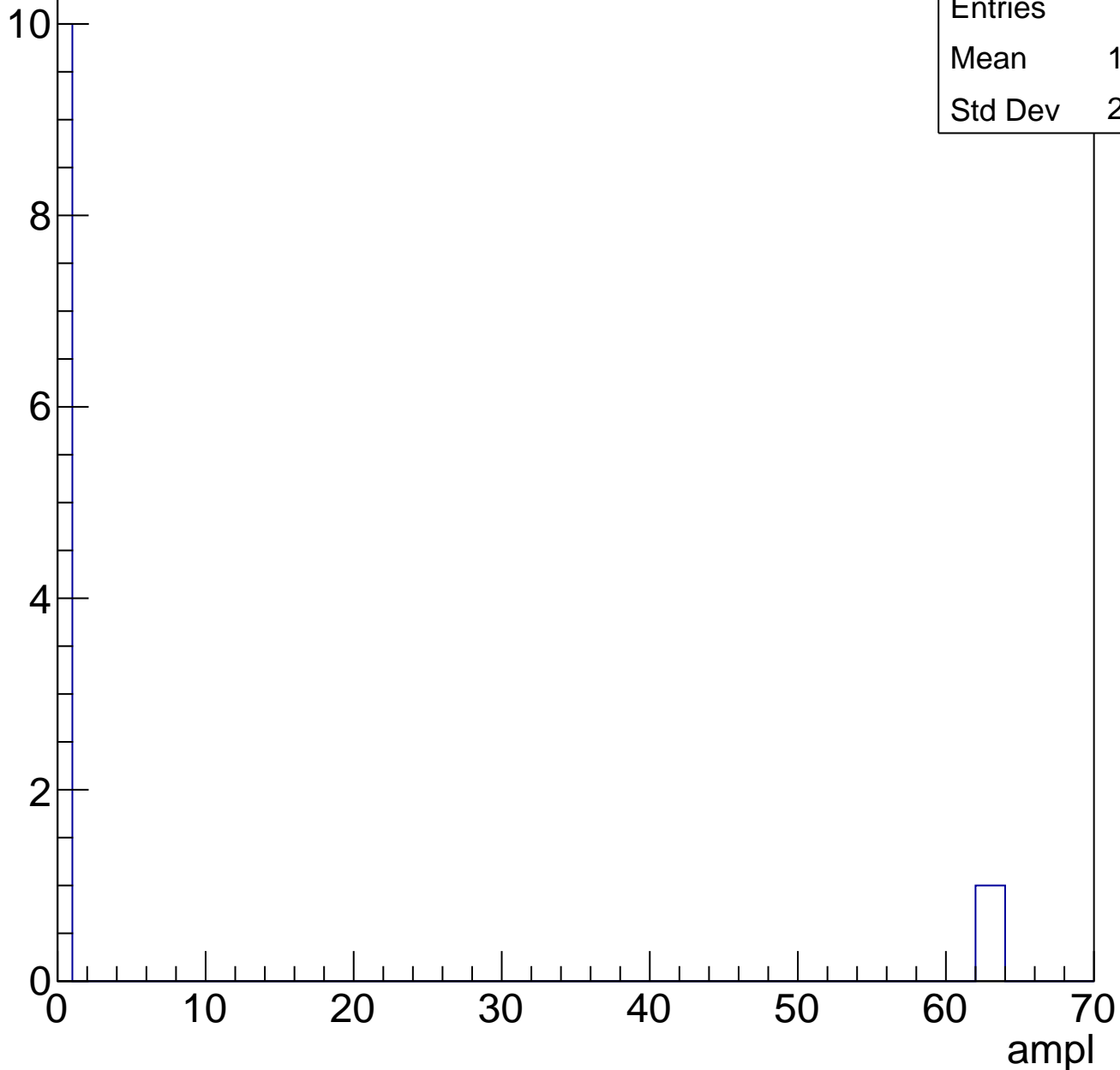


B1L103S, U14-ch120, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	12
Mean	10.42
Std Dev	23.29

Entry

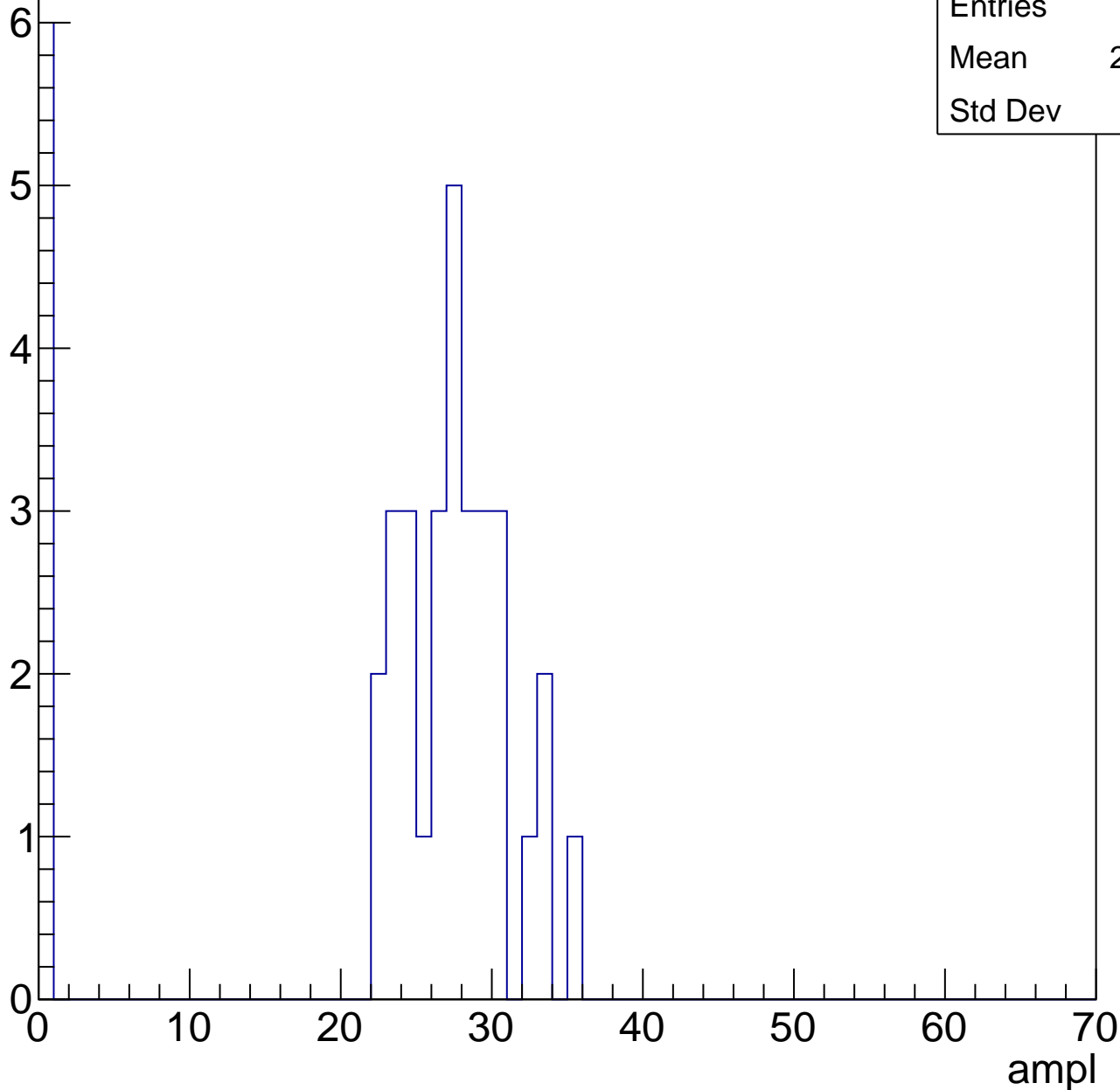


B1L103S, U14-ch121, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	36
Mean	22.69
Std Dev	10.6

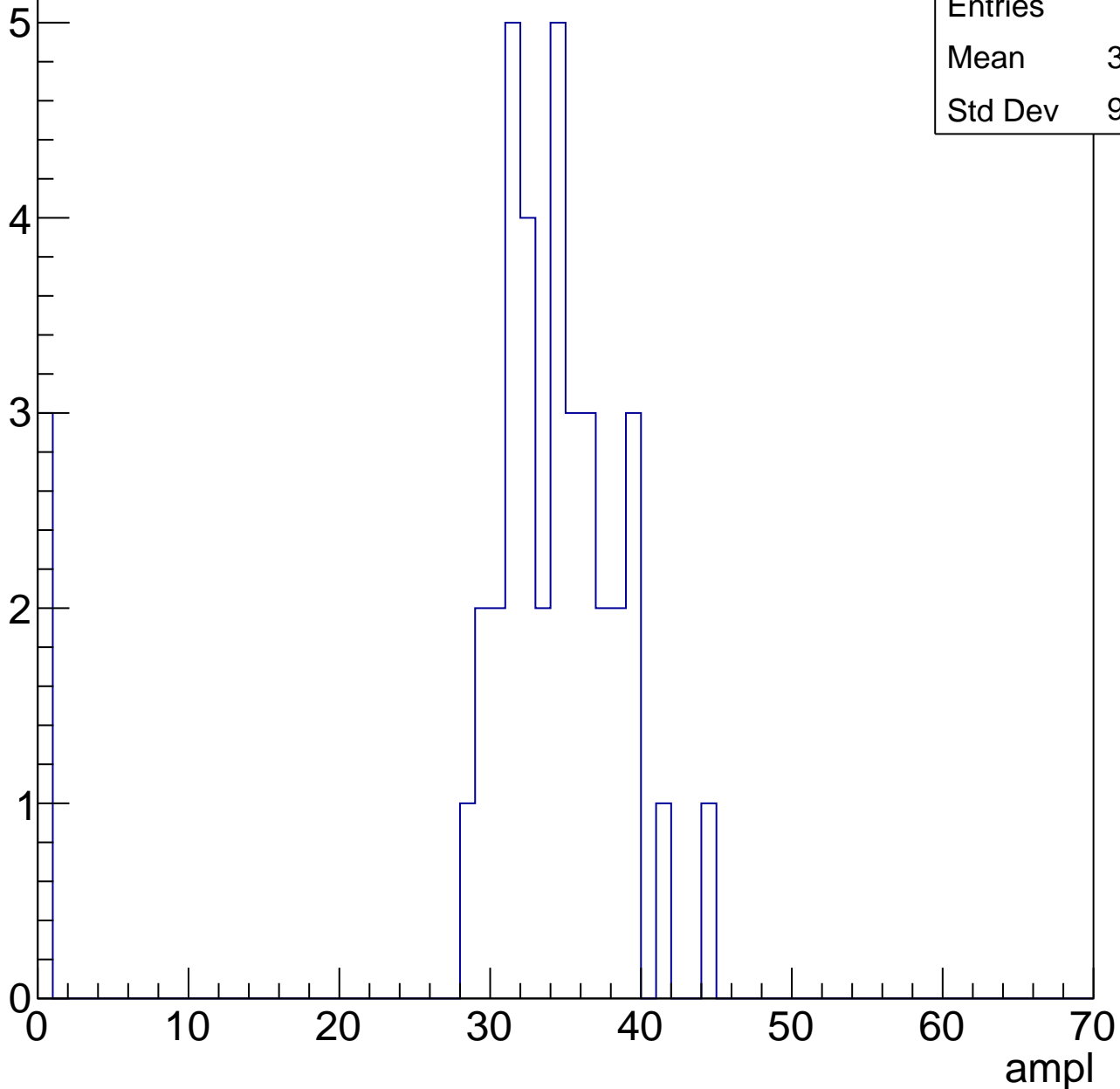


B1L103S, U14-ch121, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	31.54
Std Dev	9.742

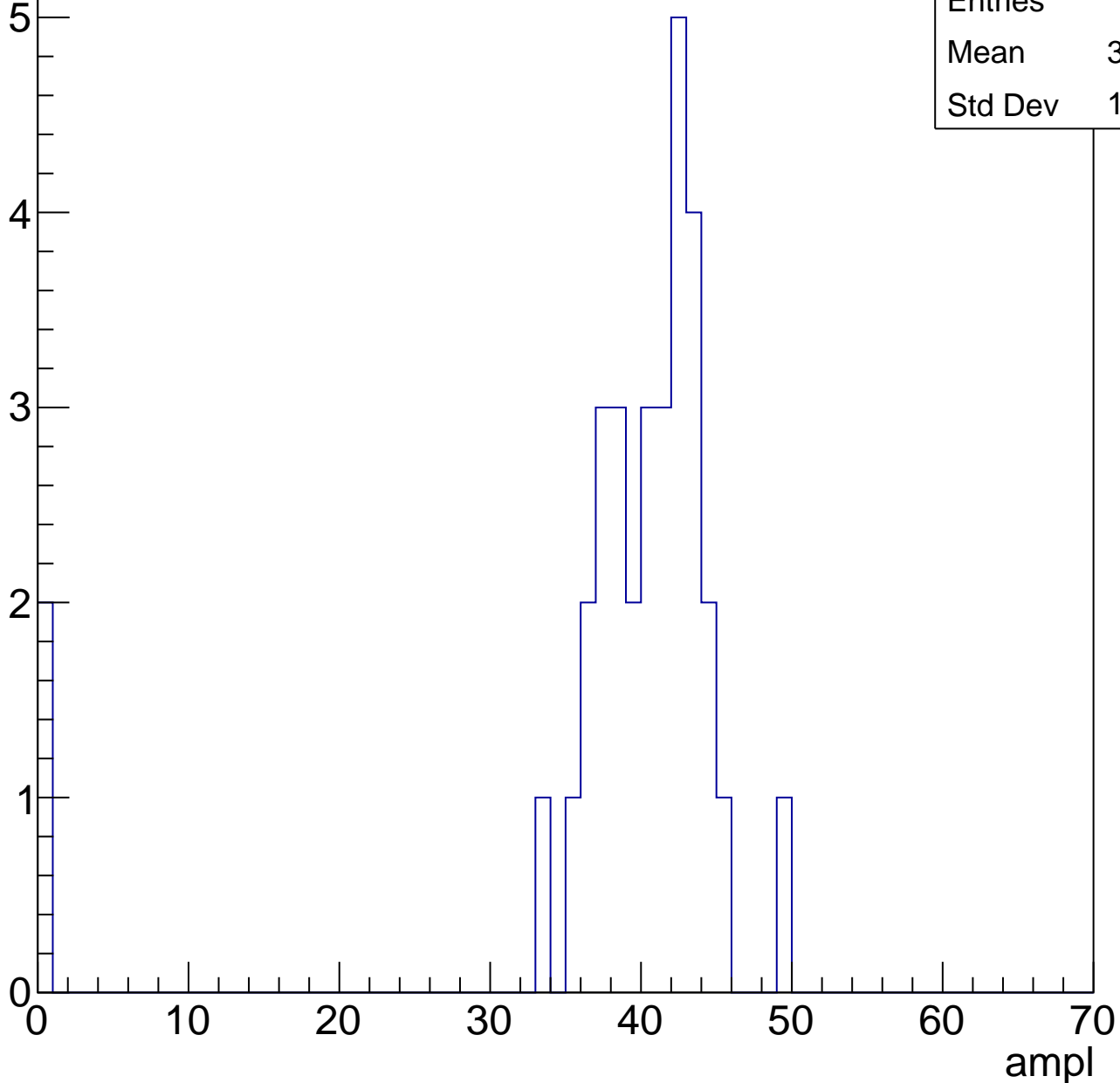


B1L103S, U14-ch121, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	33
Mean	37.88
Std Dev	10.14

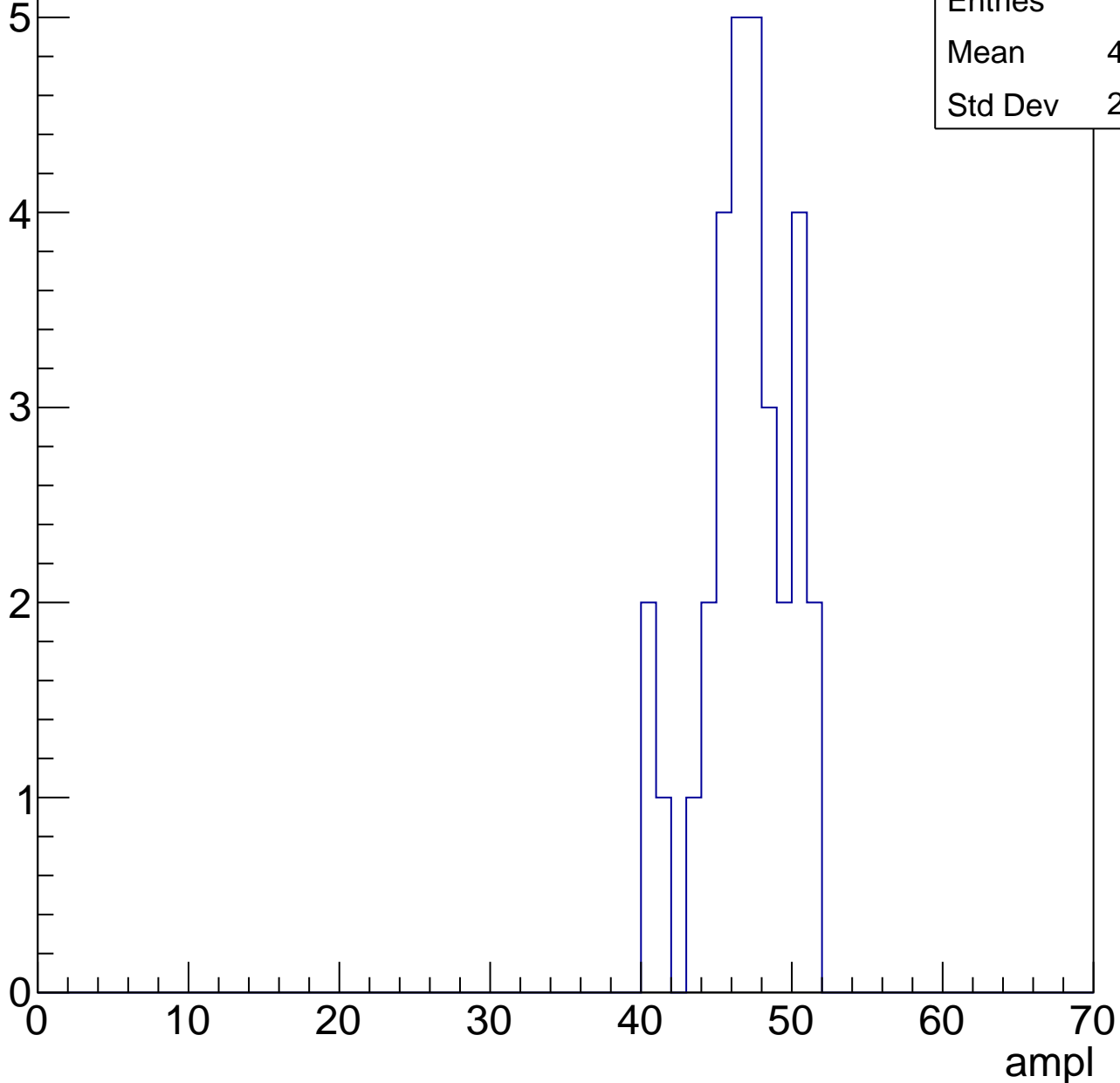


B1L103S, U14-ch121, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

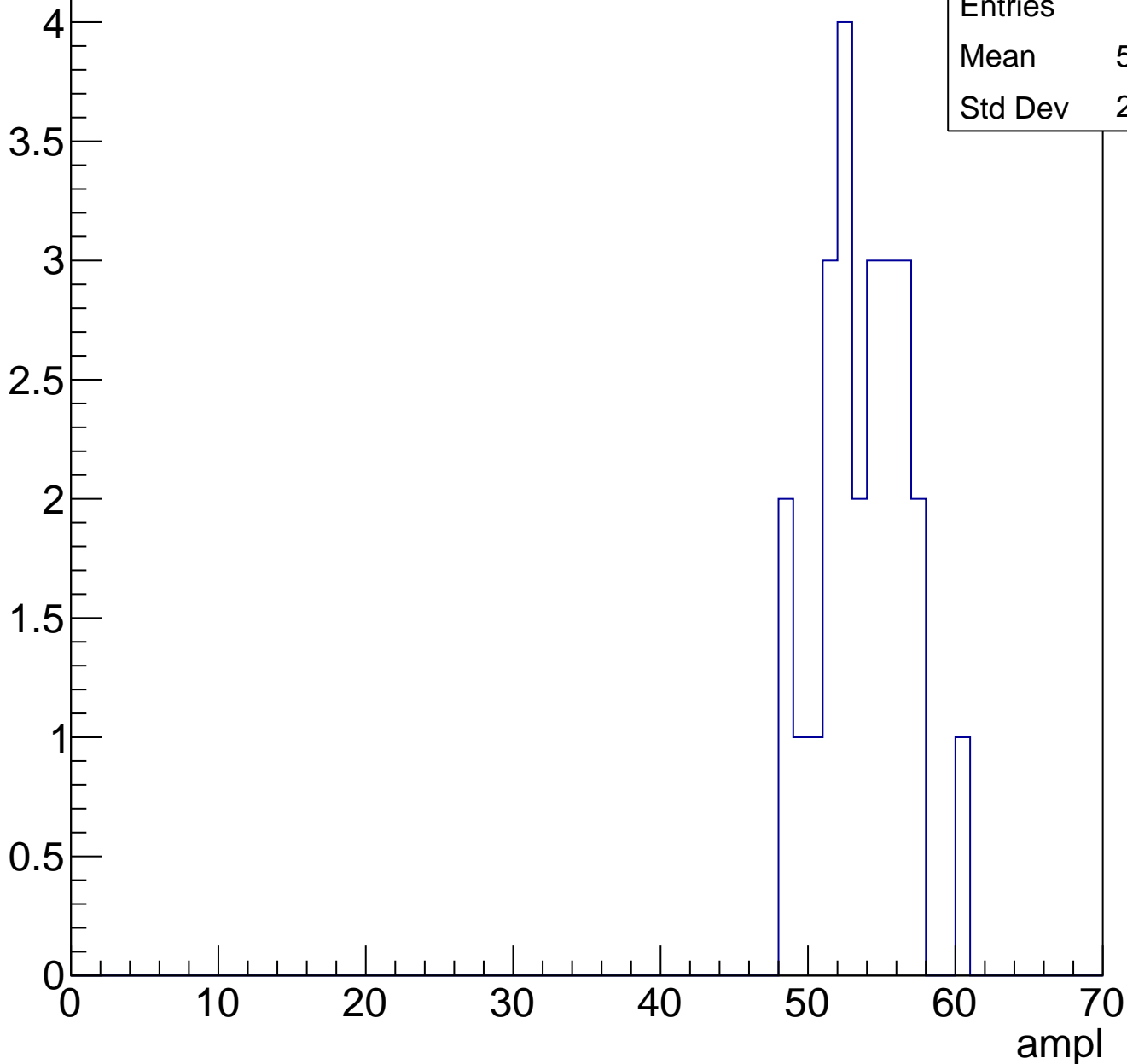
Entries	31
Mean	46.48
Std Dev	2.895



B1L103S, U14-ch121, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

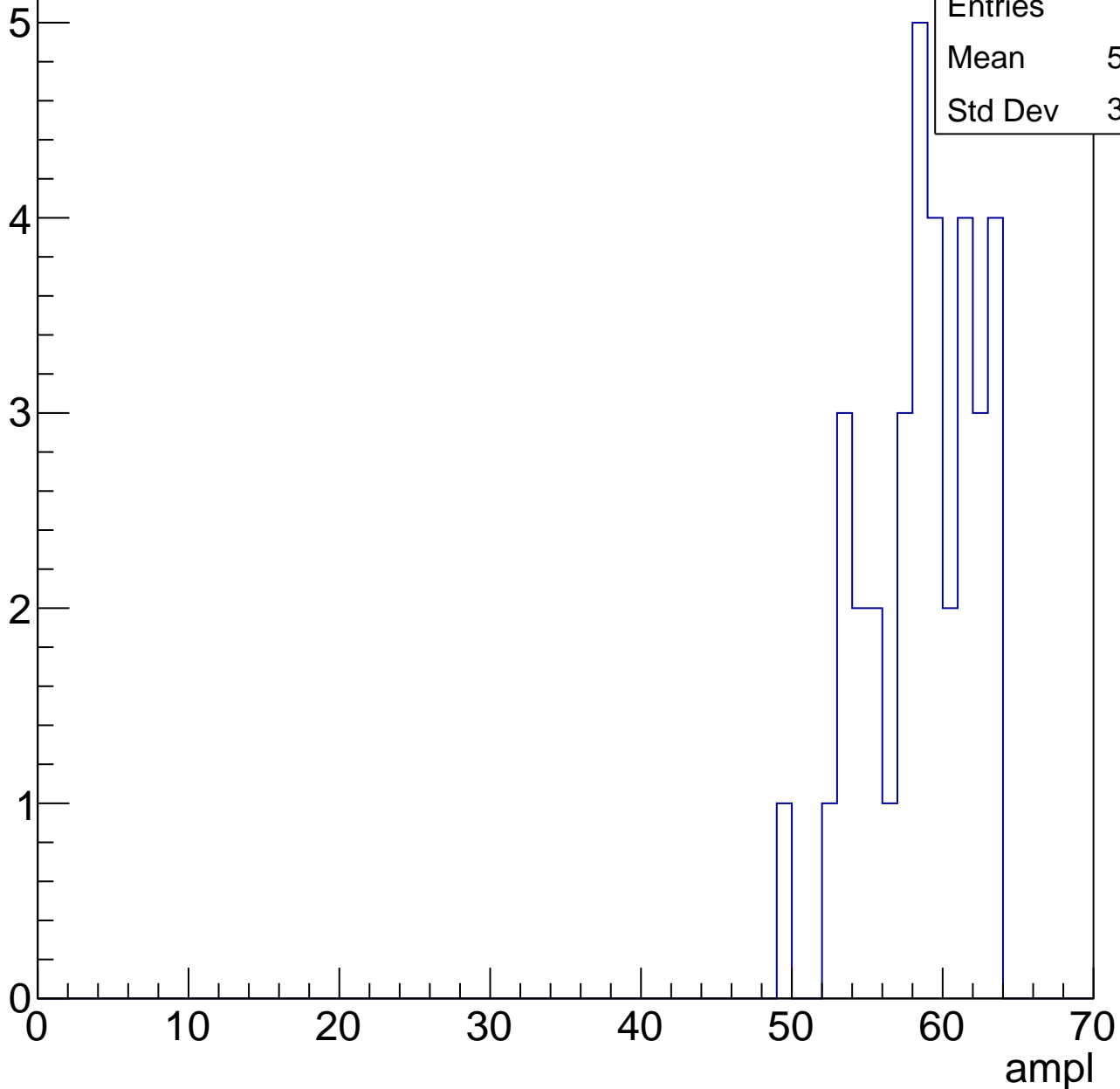


B1L103S, U14-ch121, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	35
Mean	58.09
Std Dev	3.565



B1L103S, U14-ch121, adc6

calib_packv5_041523_1651.root, FC#0, port C2

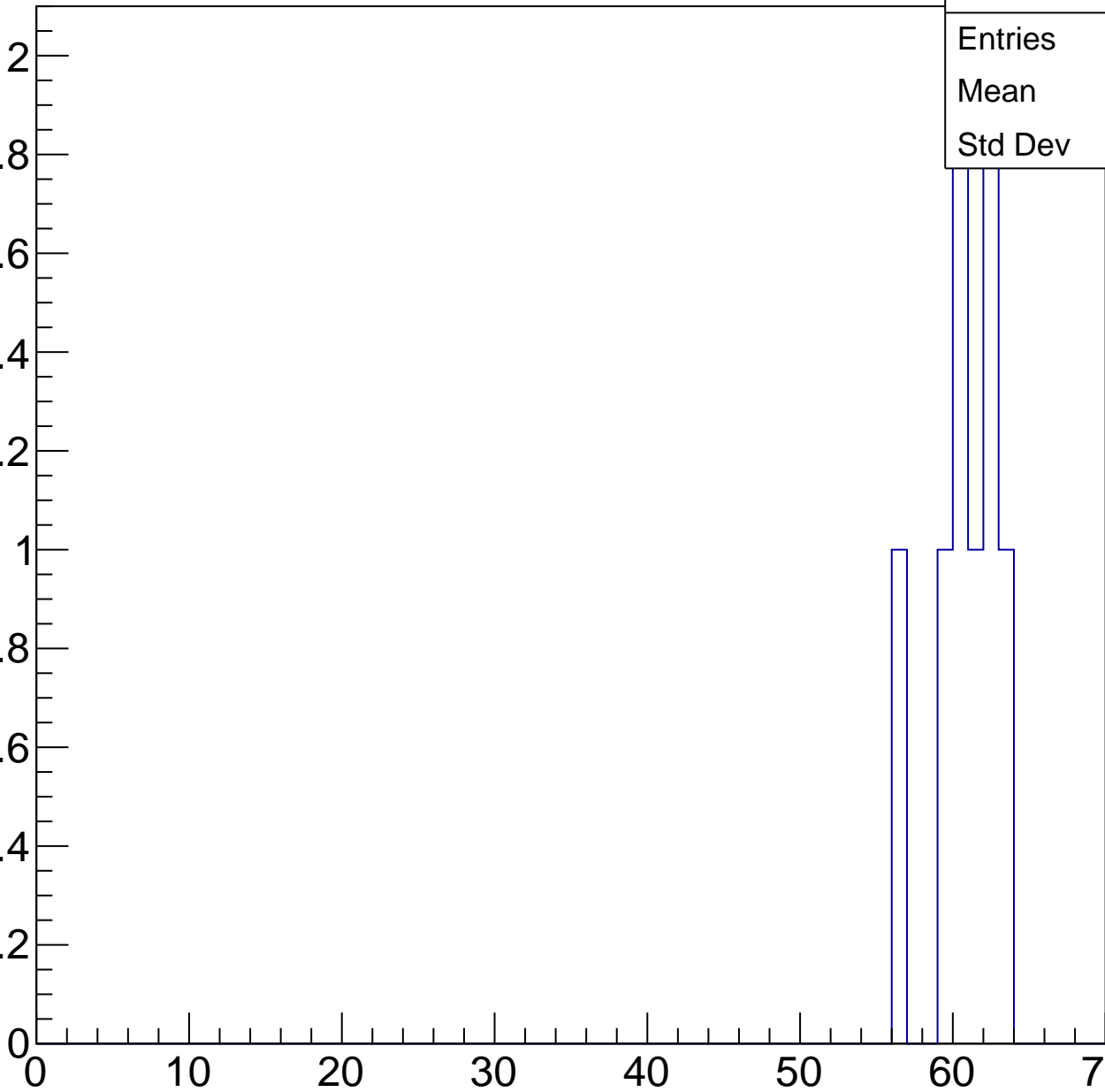
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	8
Mean	60.38
Std Dev	2.058

0 10 20 30 40 50 60 70

ampl



B1L103S, U14-ch121, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

Entries	10
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Mean	0
------	---

Std Dev	0
---------	---

8

6

4

2

0

0

10

20

30

40

50

60

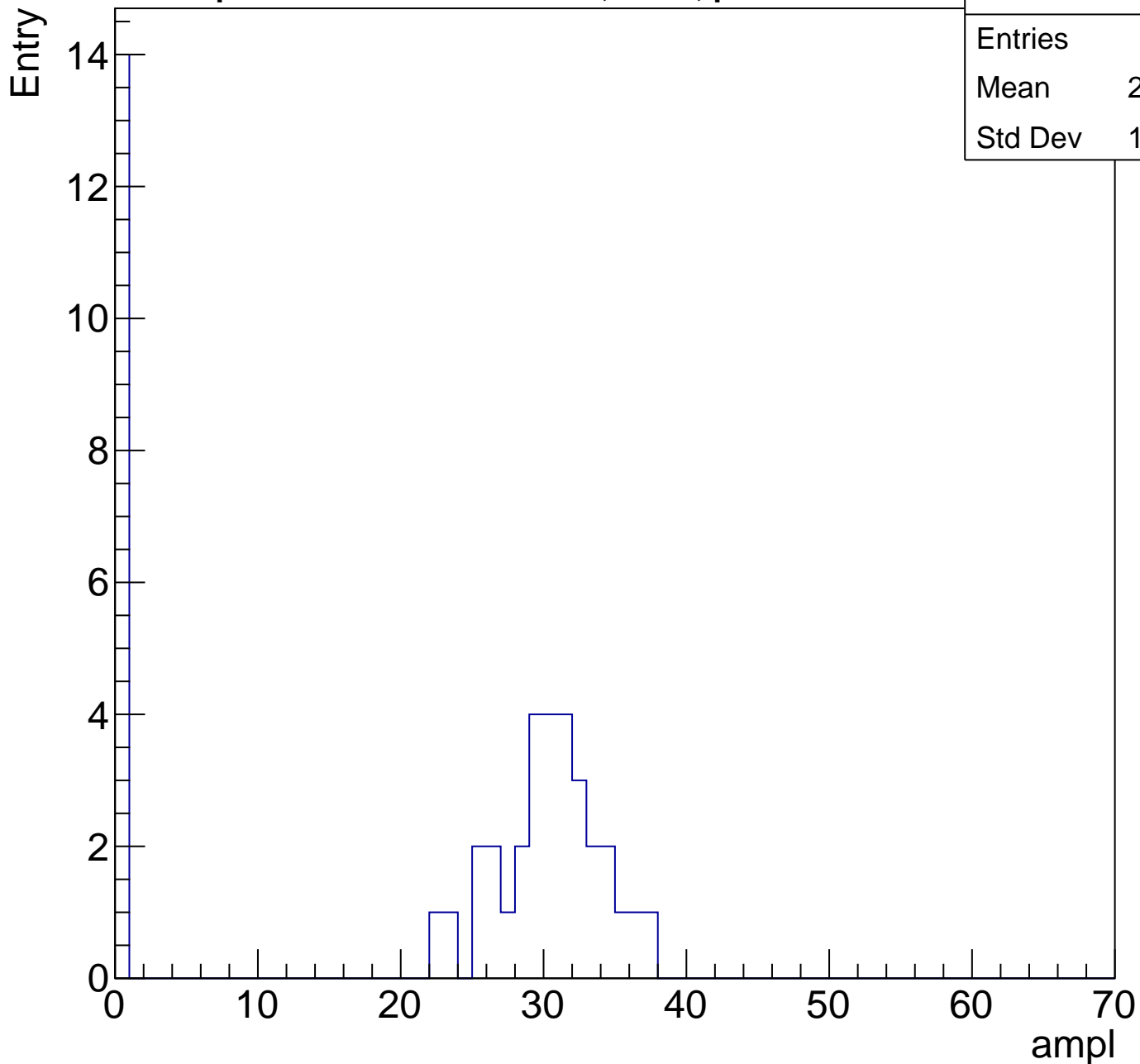
70

ampl

B1L103S, U14-ch122, adc0

calib_packv5_041523_1651.root, FC#0, port C2

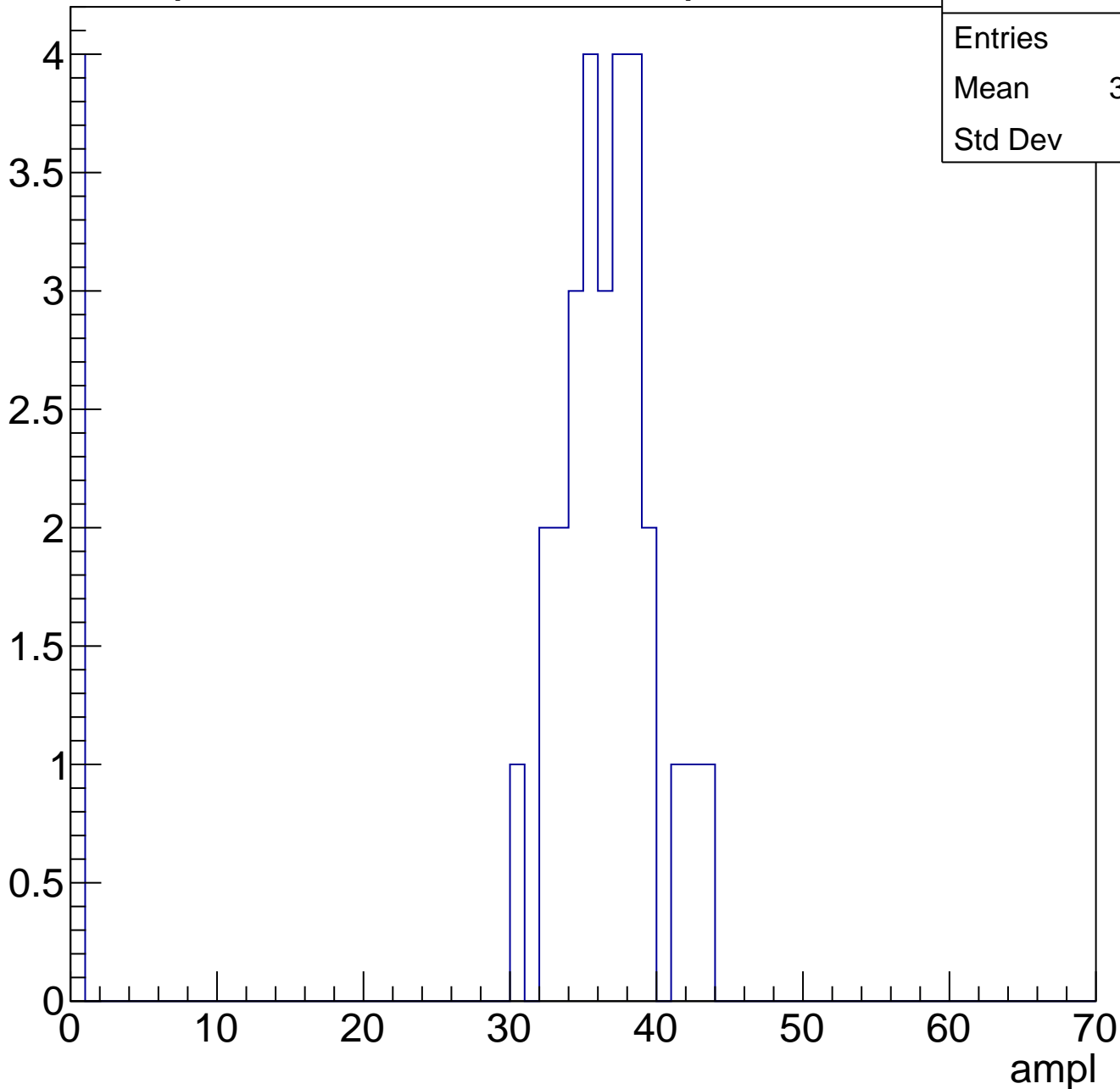
Entries	45
Mean	20.62
Std Dev	14.17



B1L103S, U14-ch122, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

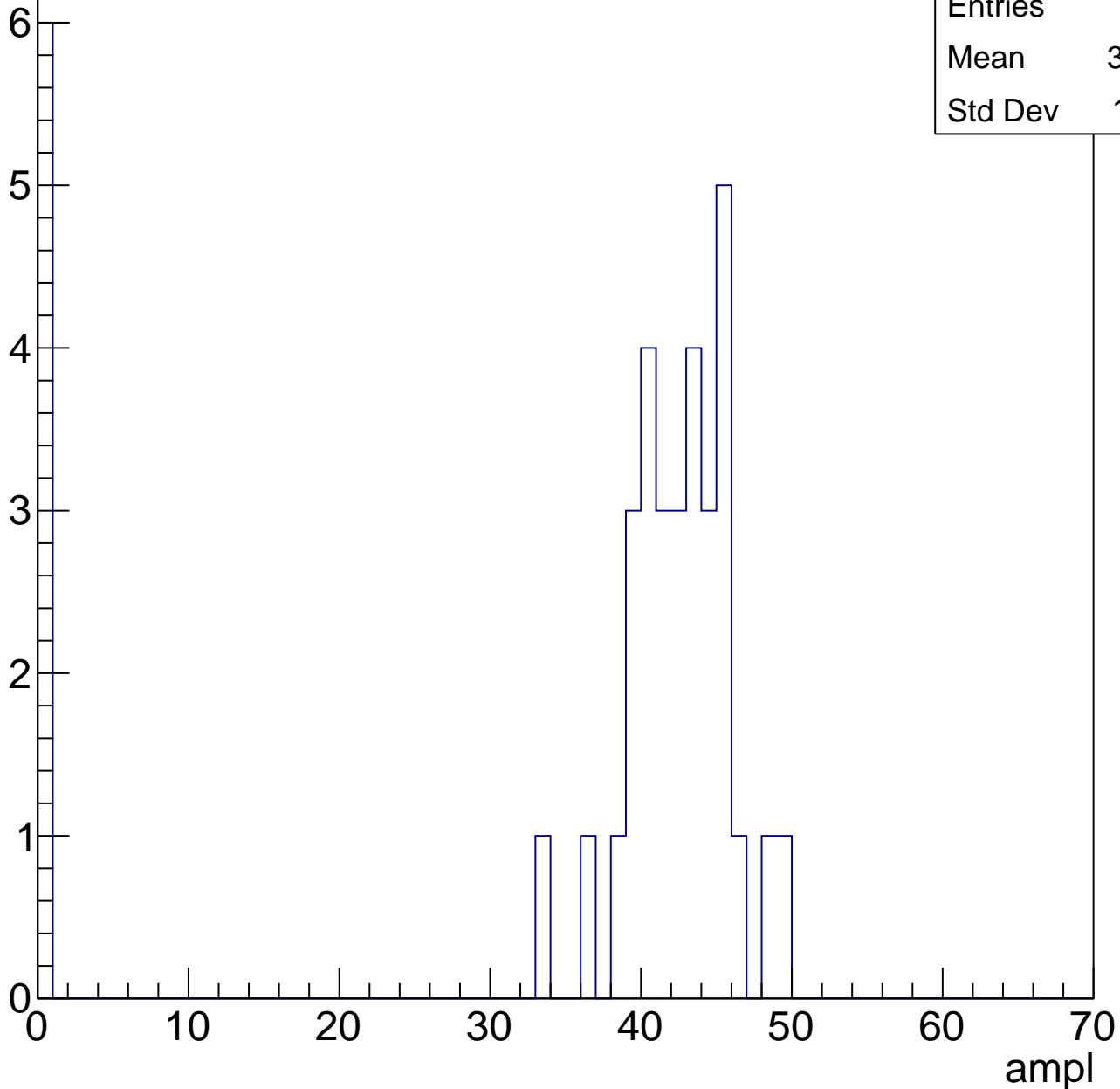


B1L103S, U14-ch122, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

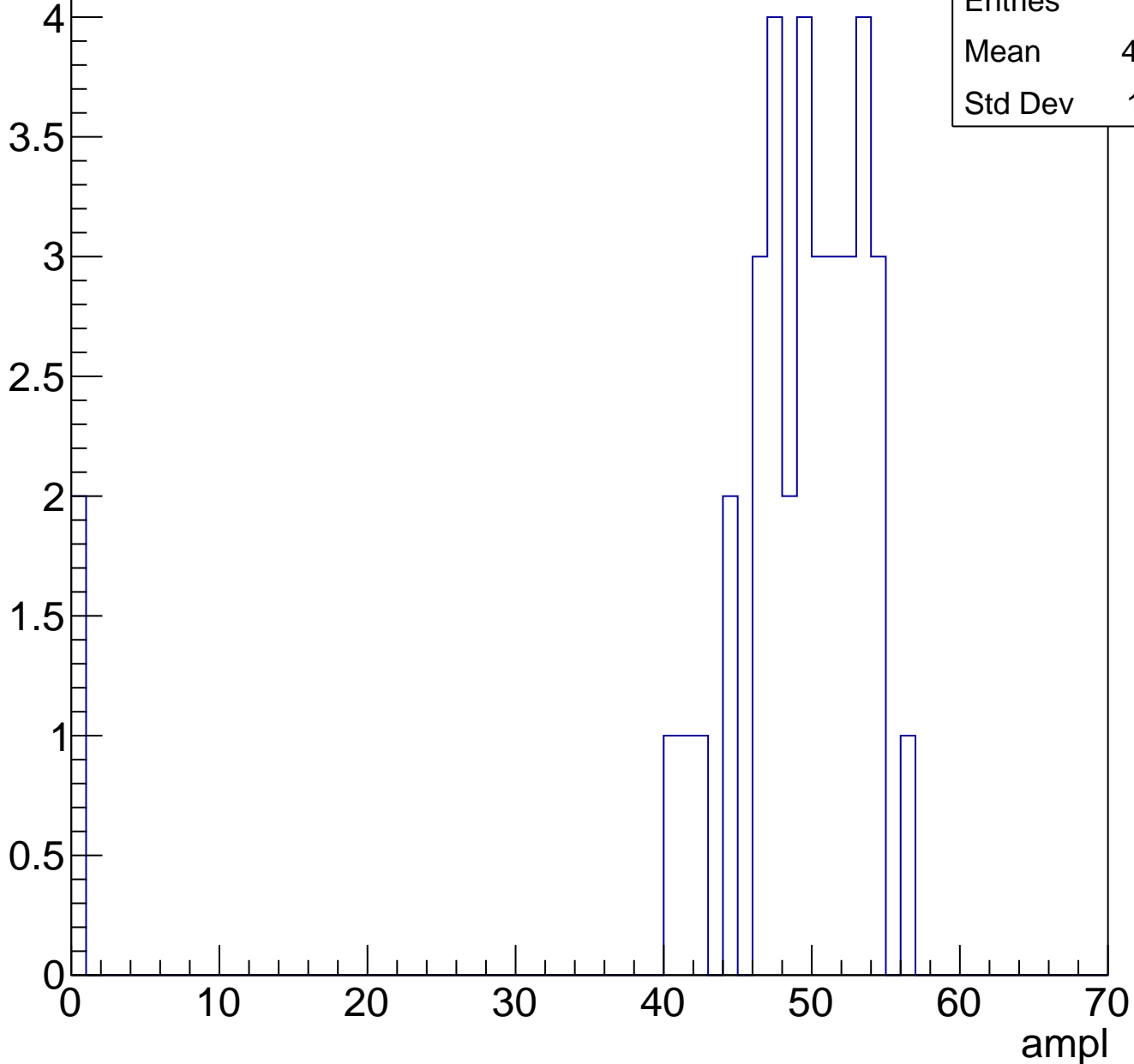
Entries	37
Mean	35.27
Std Dev	15.81



B1L103S, U14-ch122, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

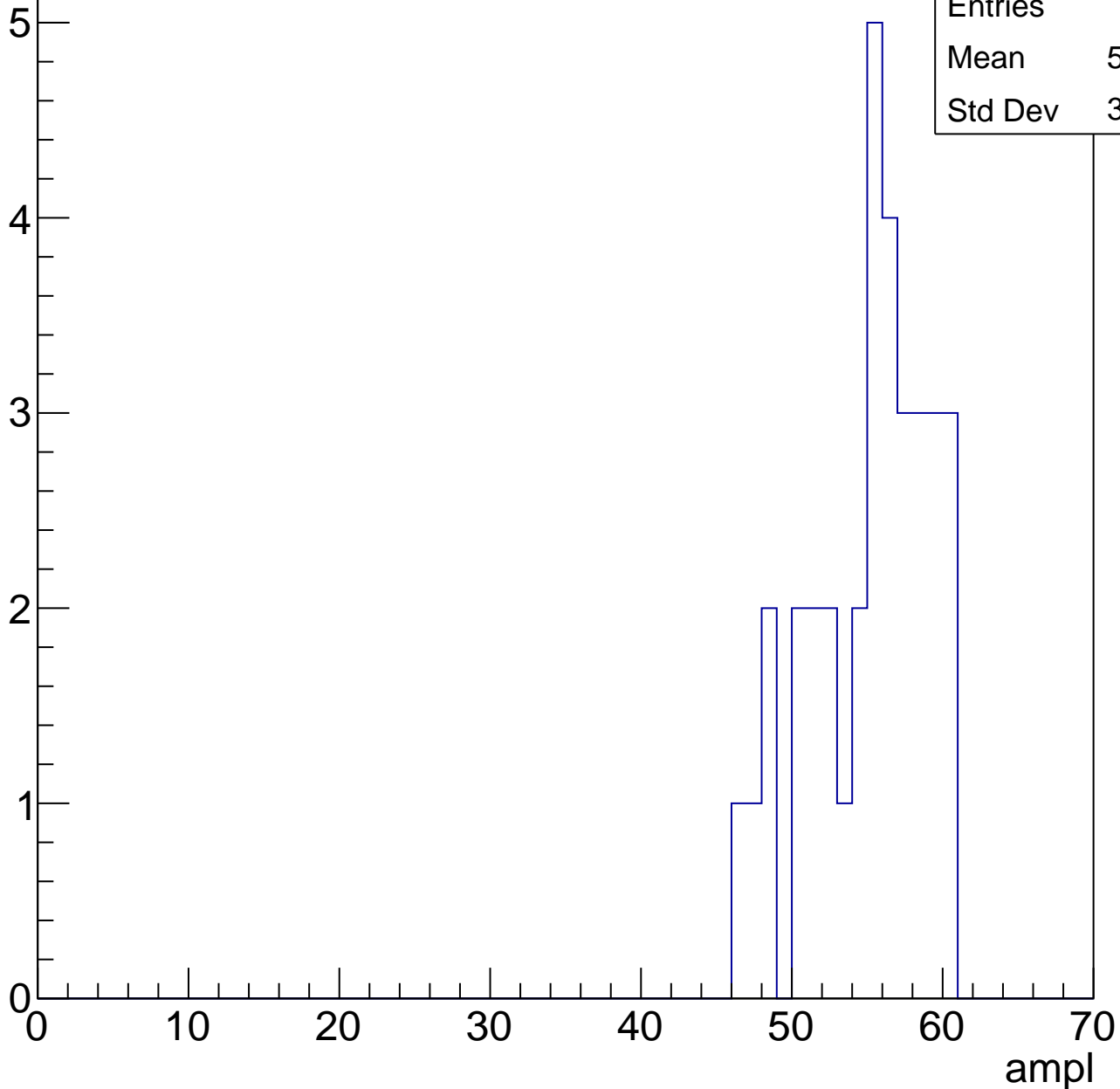


B1L103S, U14-ch122, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	34
Mean	54.62
Std Dev	3.873



B1L103S, U14-ch122, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

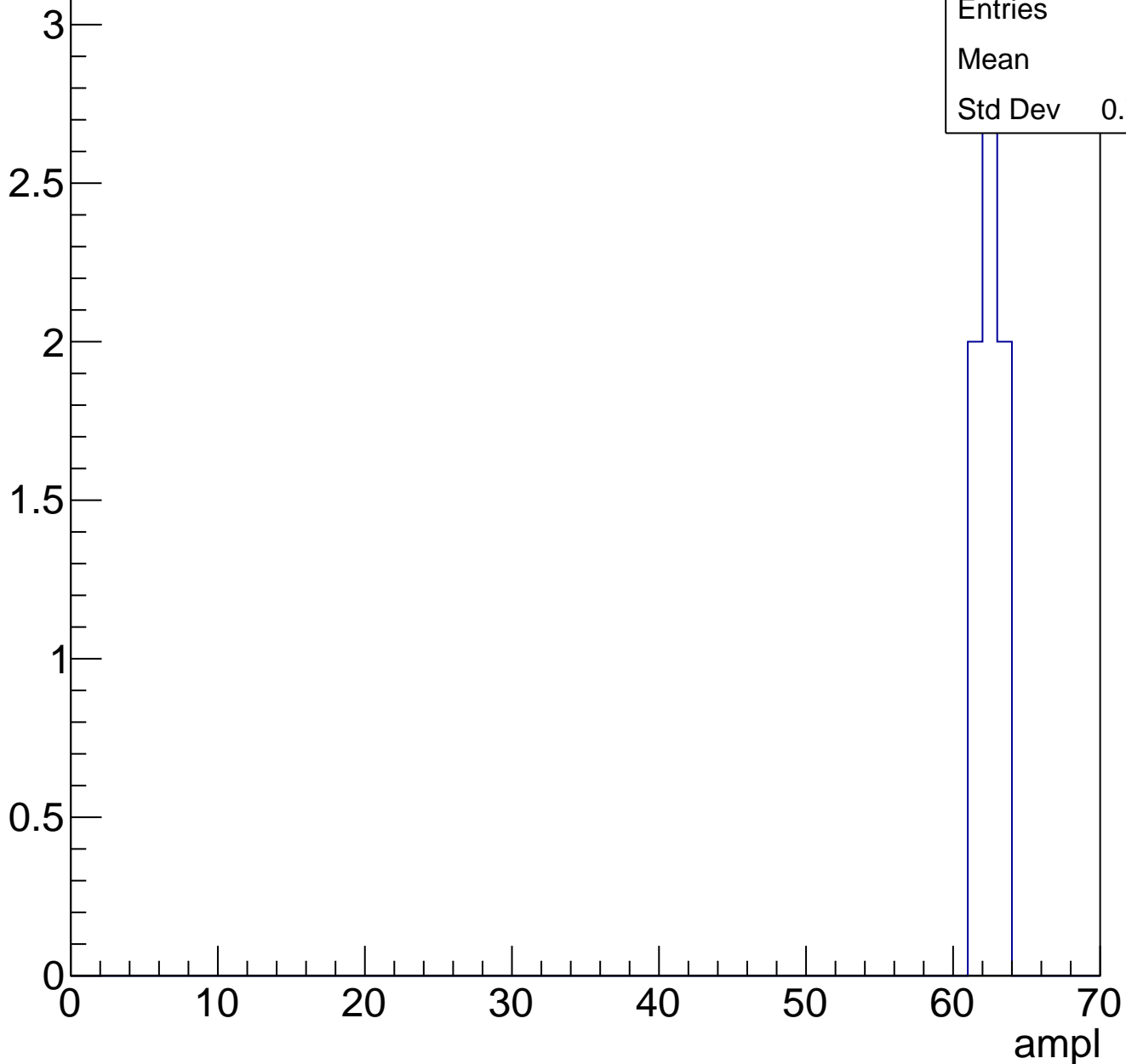
ampl

Entries	16
Mean	60.25
Std Dev	2.016

B1L103S, U14-ch122, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

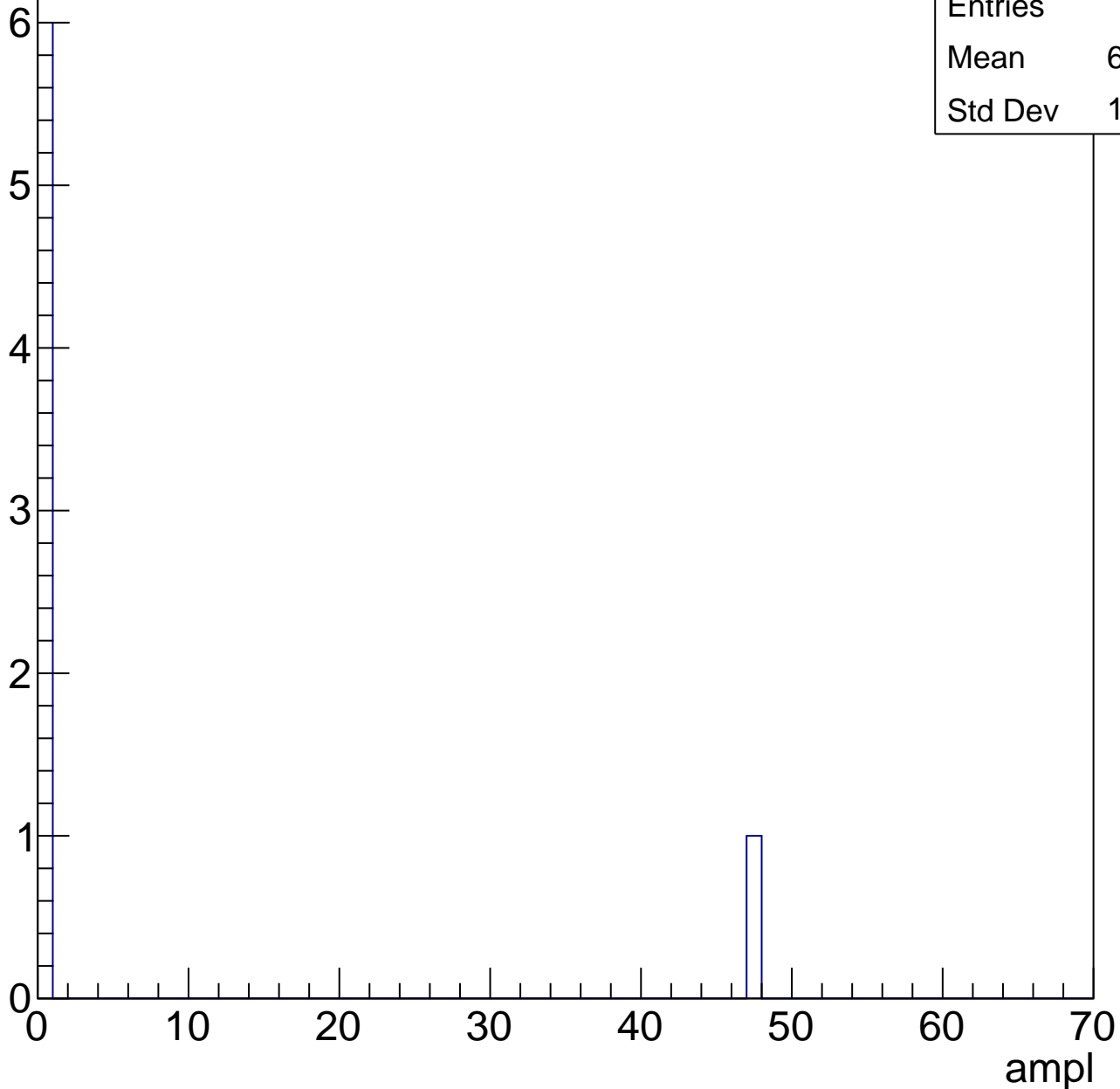


B1L103S, U14-ch122, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

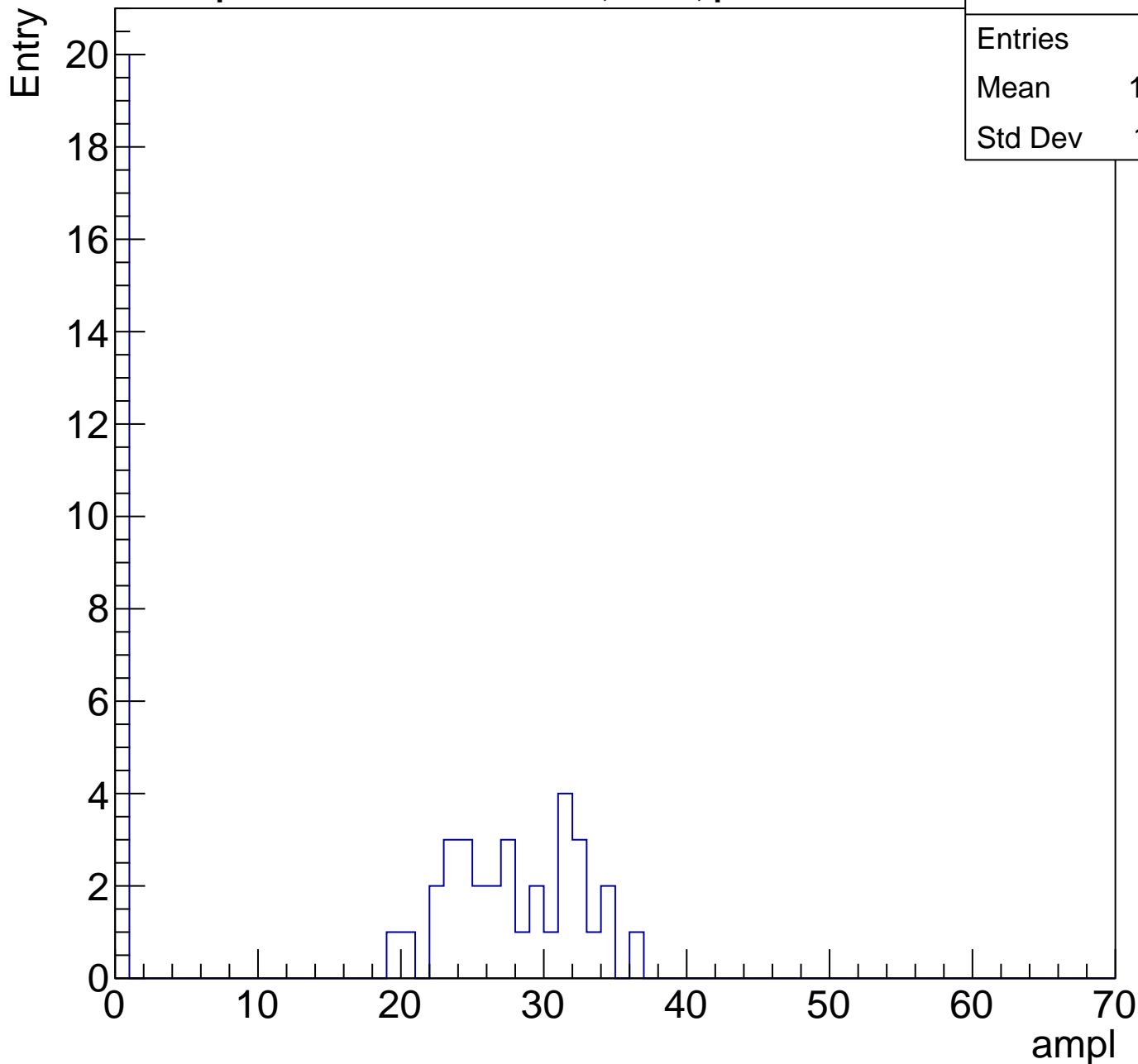
Entries	7
Mean	6.714
Std Dev	16.45



B1L103S, U14-ch123, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	52
Mean	16.92
Std Dev	13.81

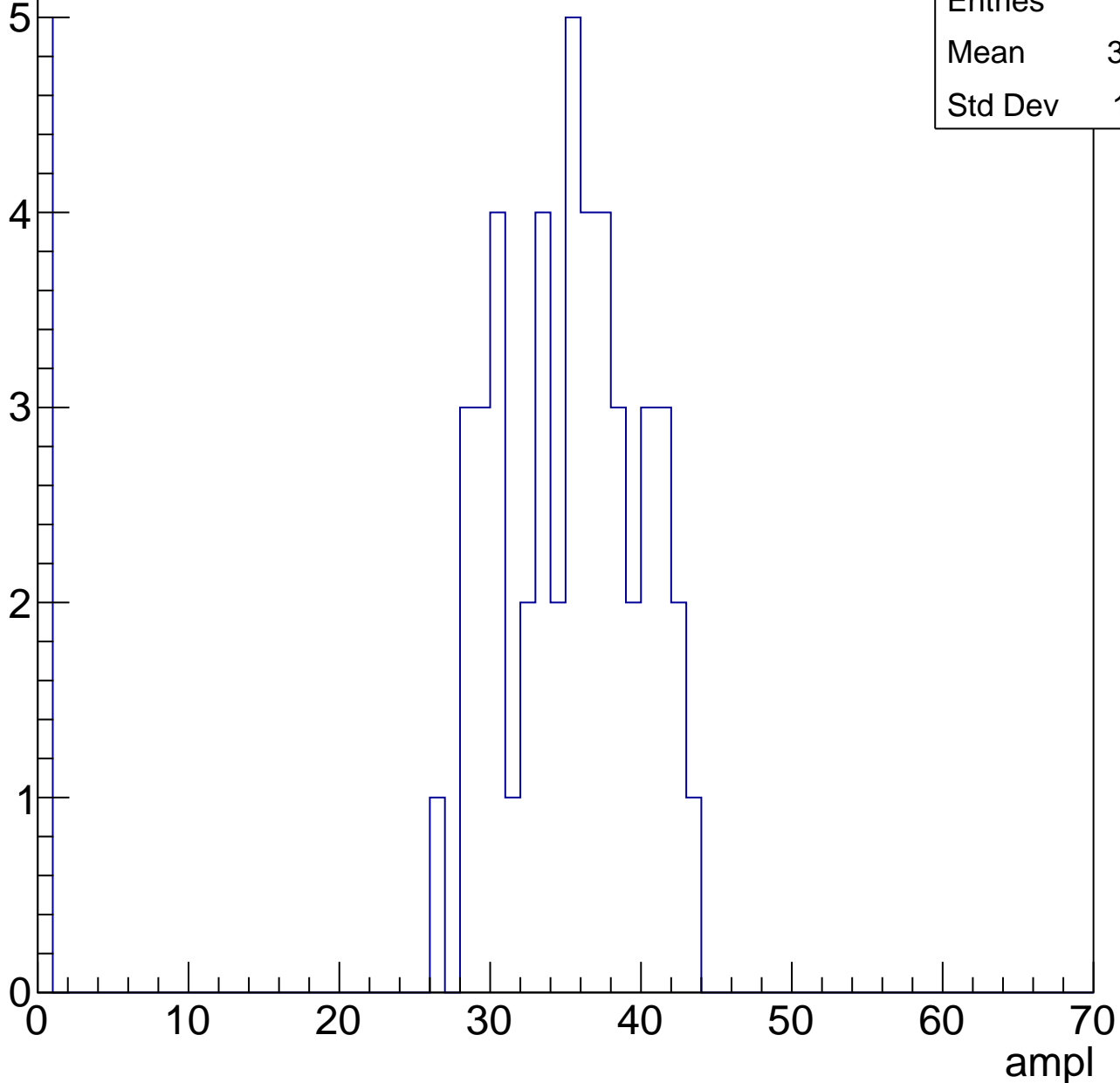


B1L103S, U14-ch123, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	31.56
Std Dev	11.11

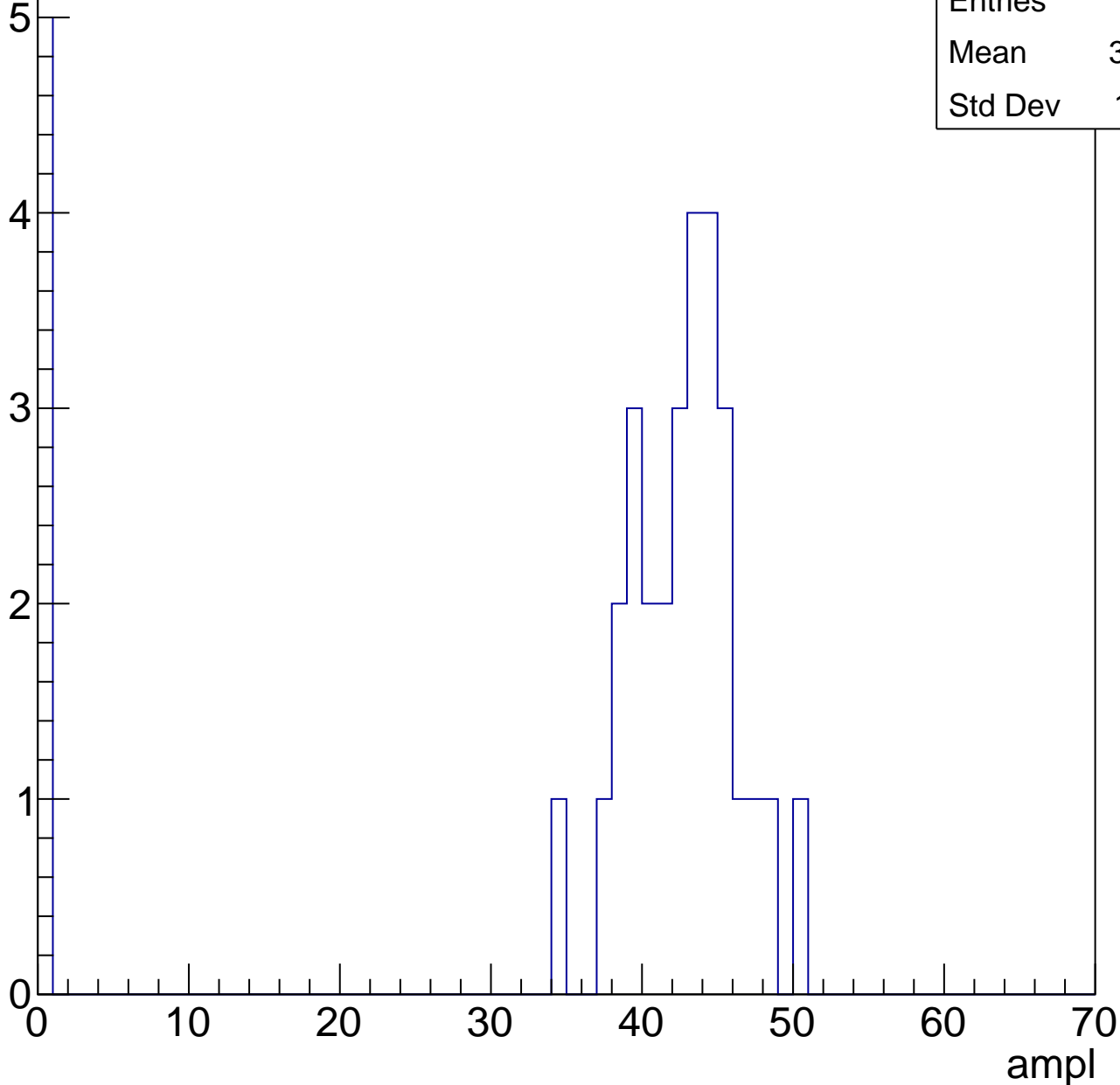


B1L103S, U14-ch123, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	34
Mean	36.06
Std Dev	15.31



B1L103S, U14-ch123, adc3

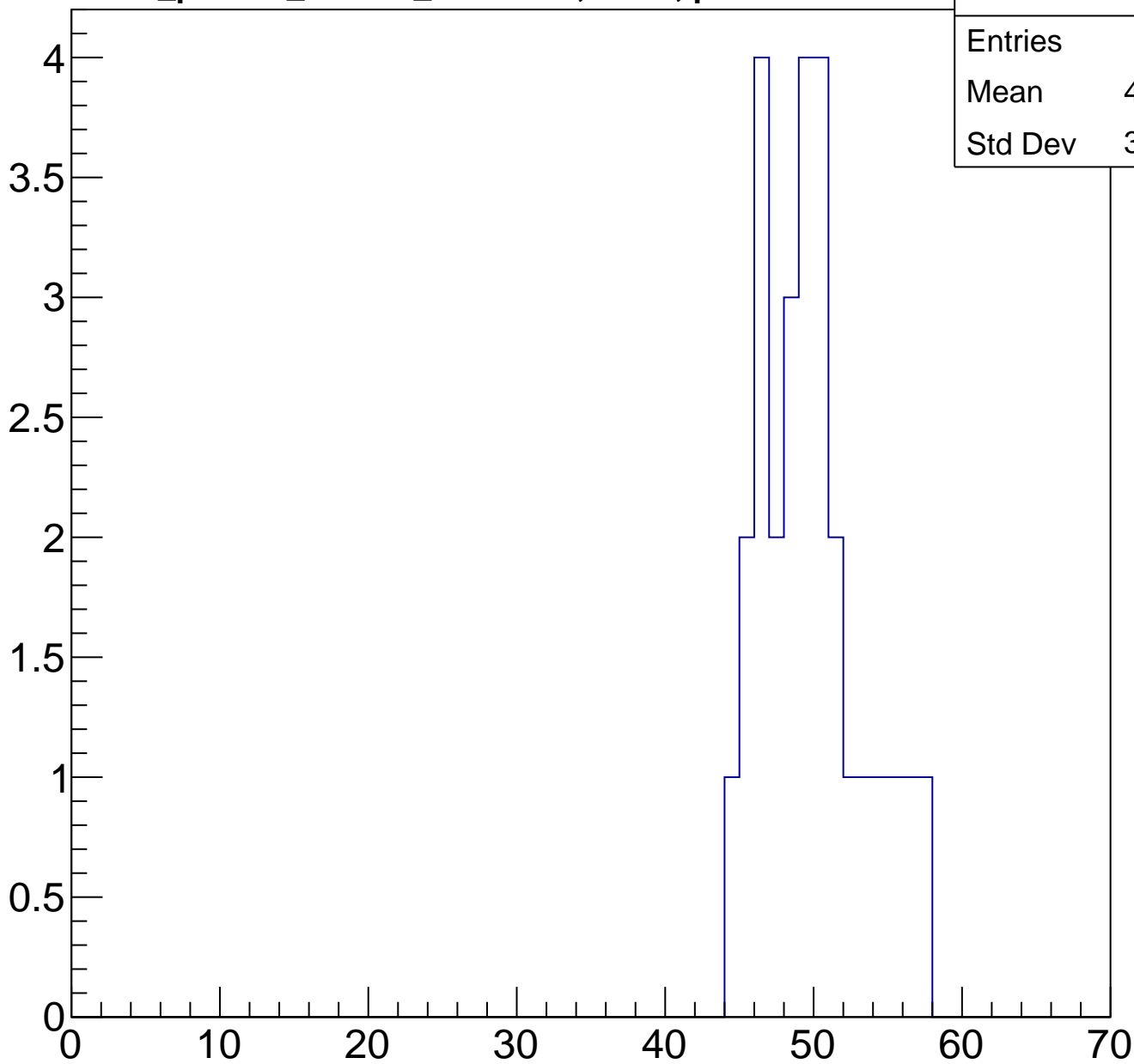
calib_packv5_041523_1651.root, FC#0, port C2

Entry

4
3.5
3
2.5
2
1.5
1
0.5
0

Entries	28
Mean	49.32
Std Dev	3.339

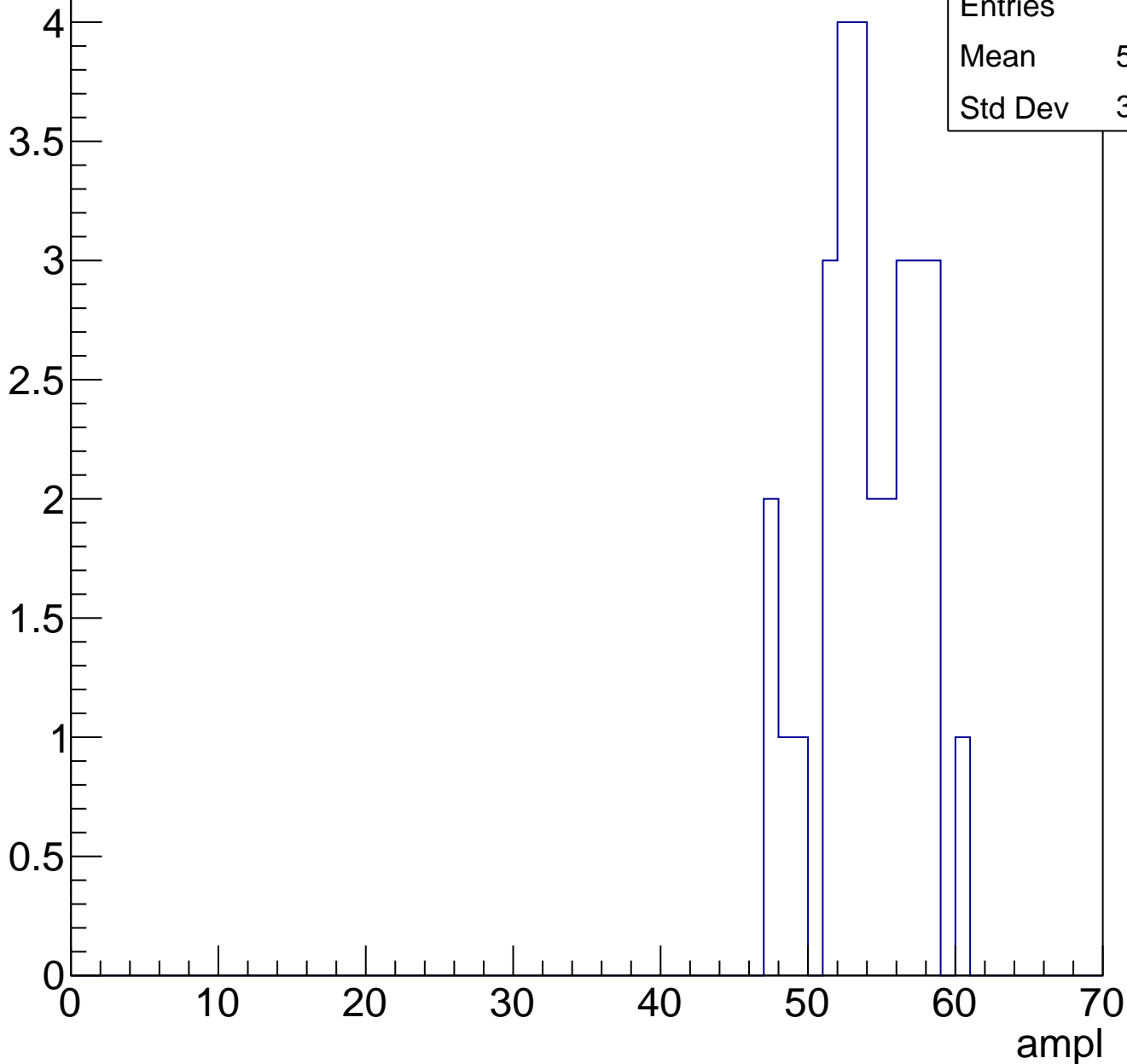
ampl



B1L103S, U14-ch123, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

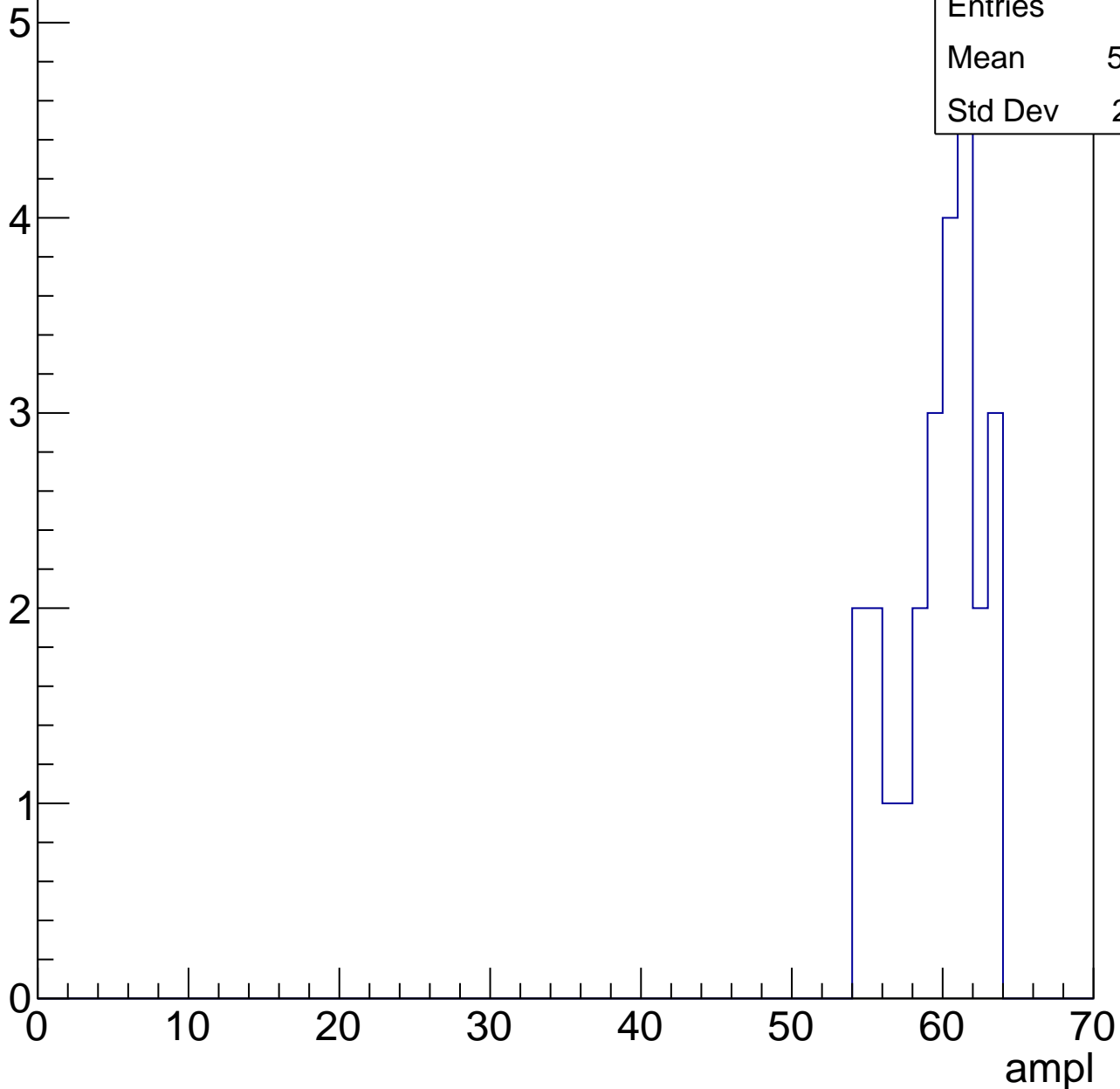


B1L103S, U14-ch123, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

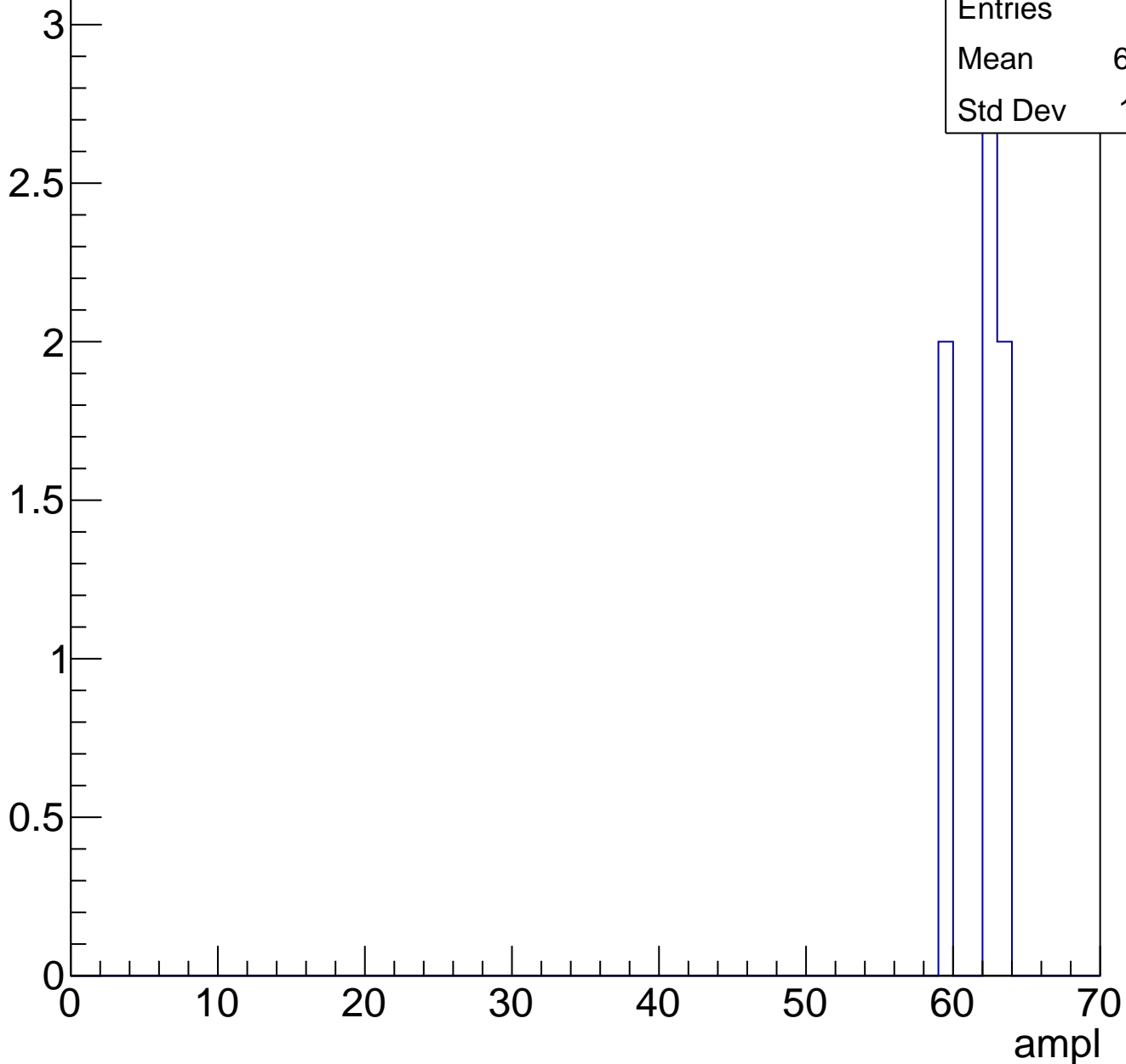
Entries	25
Mean	59.28
Std Dev	2.721



B1L103S, U14-ch123, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U14-ch123, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

Entries	10
---------	----

Mean	0
------	---

Std Dev	0
---------	---

8

6

4

2

0

0

10

20

30

40

50

60

70

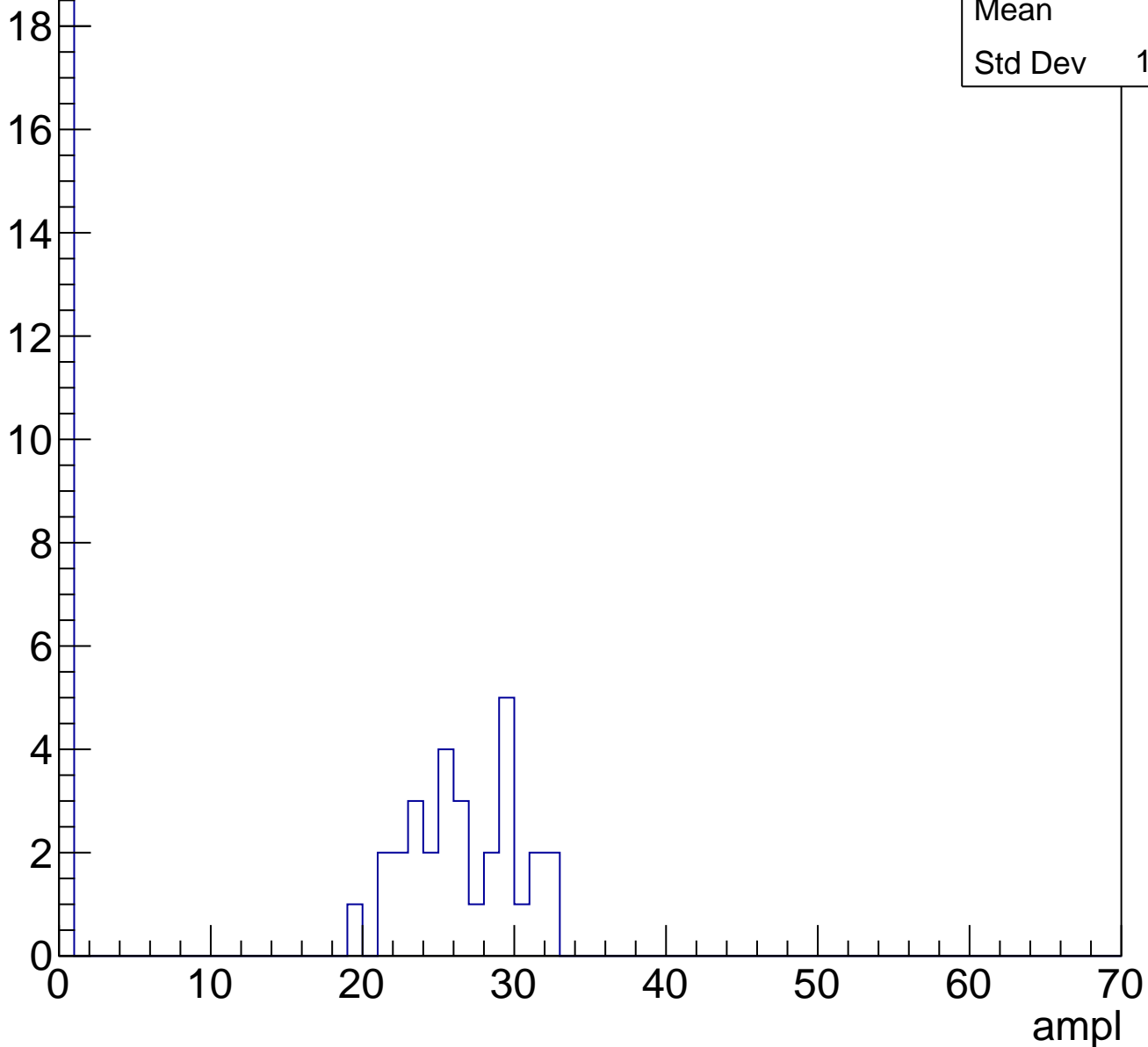
ampl

B1L103S, U14-ch124, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	49
Mean	16
Std Dev	13.02

Entry

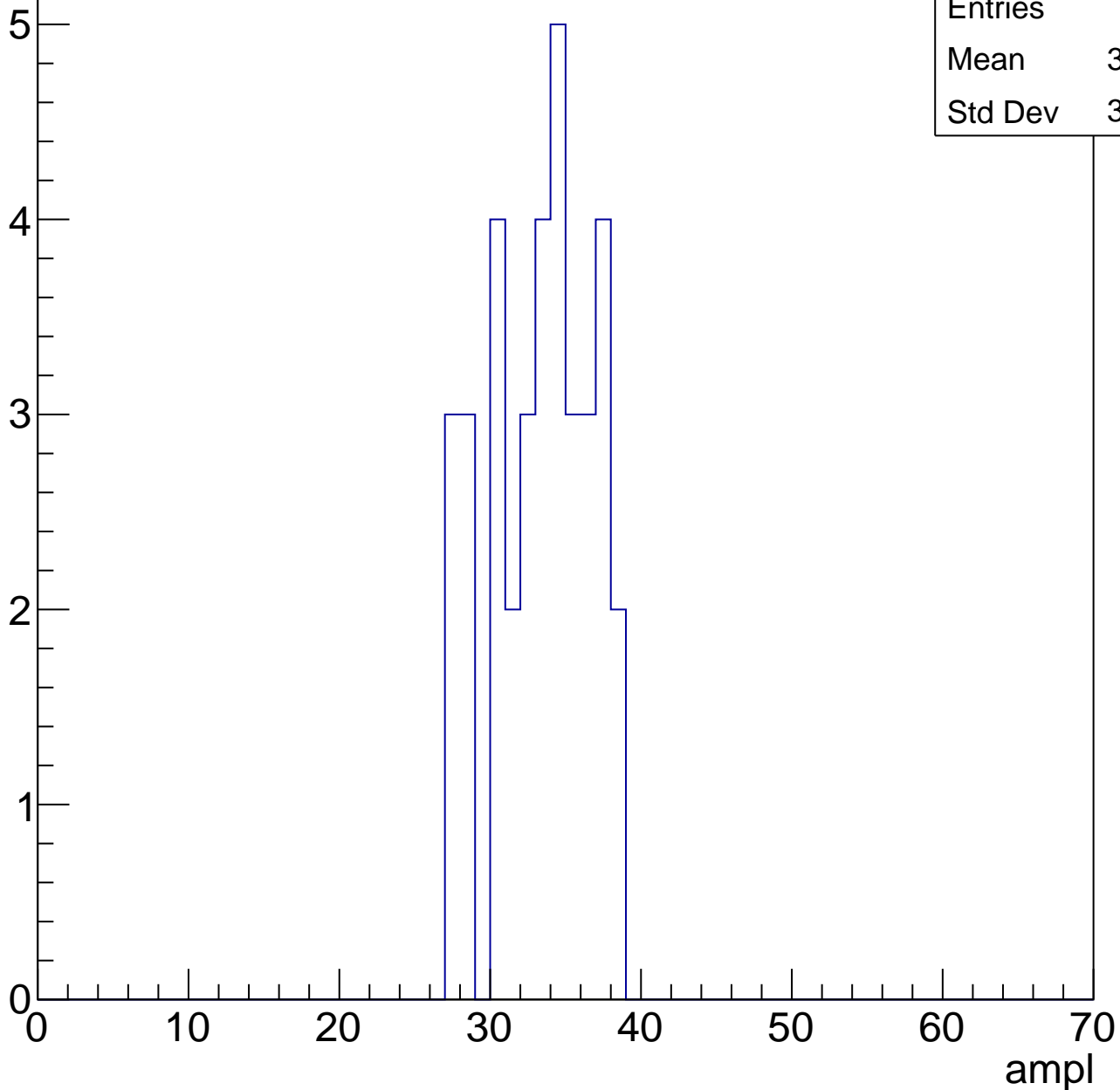


B1L103S, U14-ch124, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	36
Mean	32.83
Std Dev	3.279

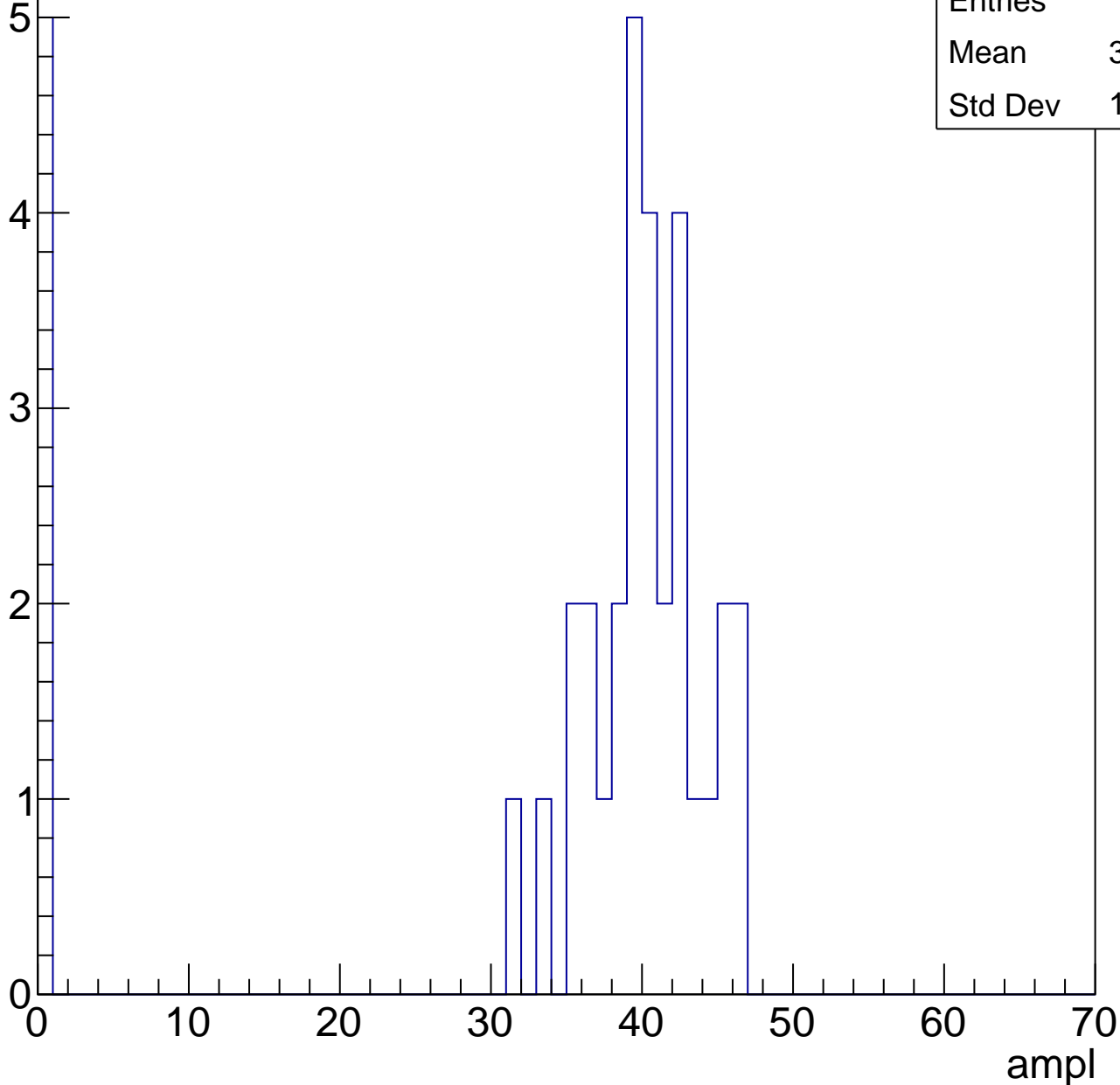


B1L103S, U14-ch124, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

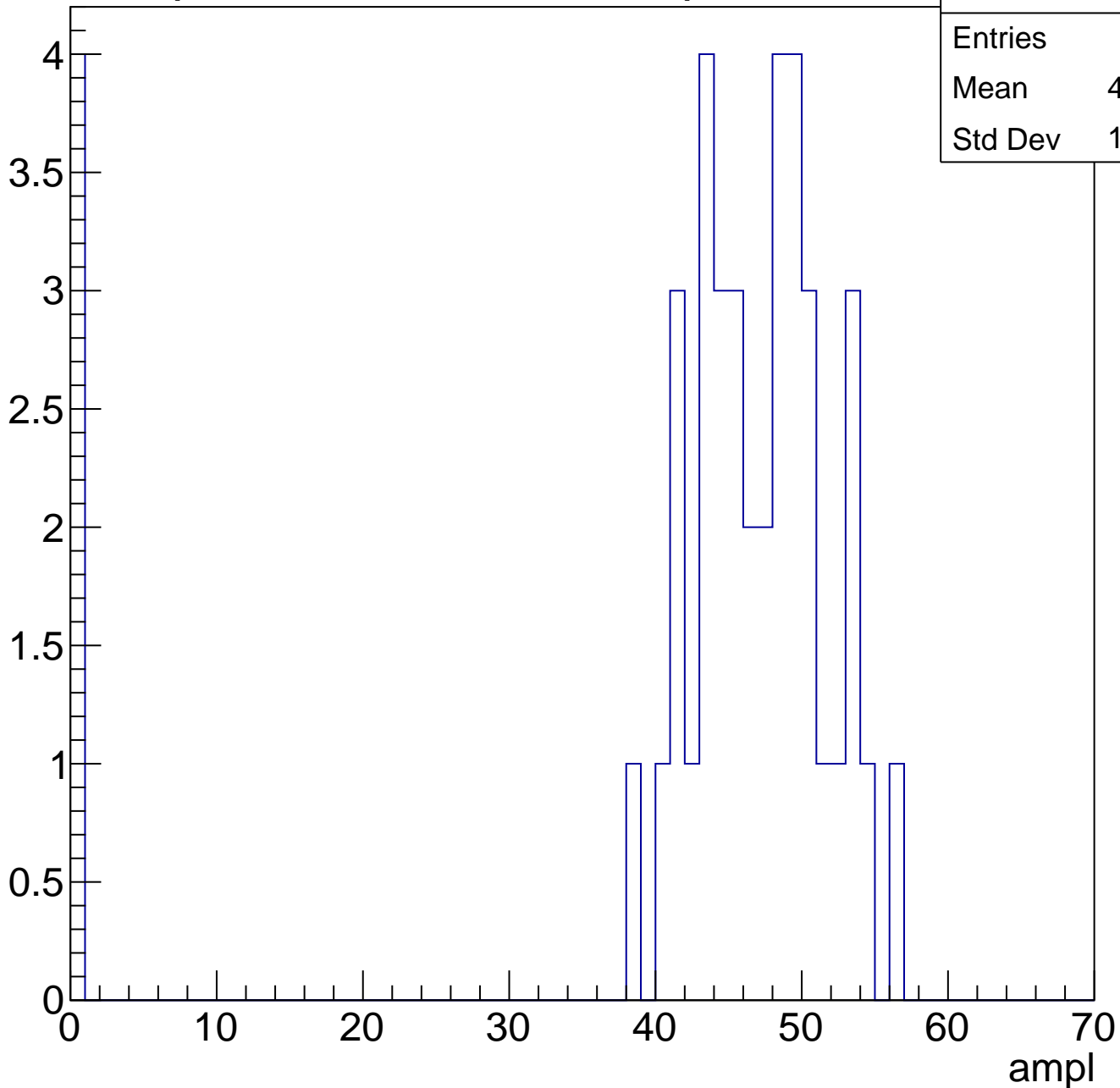
Entries	35
Mean	34.09
Std Dev	14.32



B1L103S, U14-ch124, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

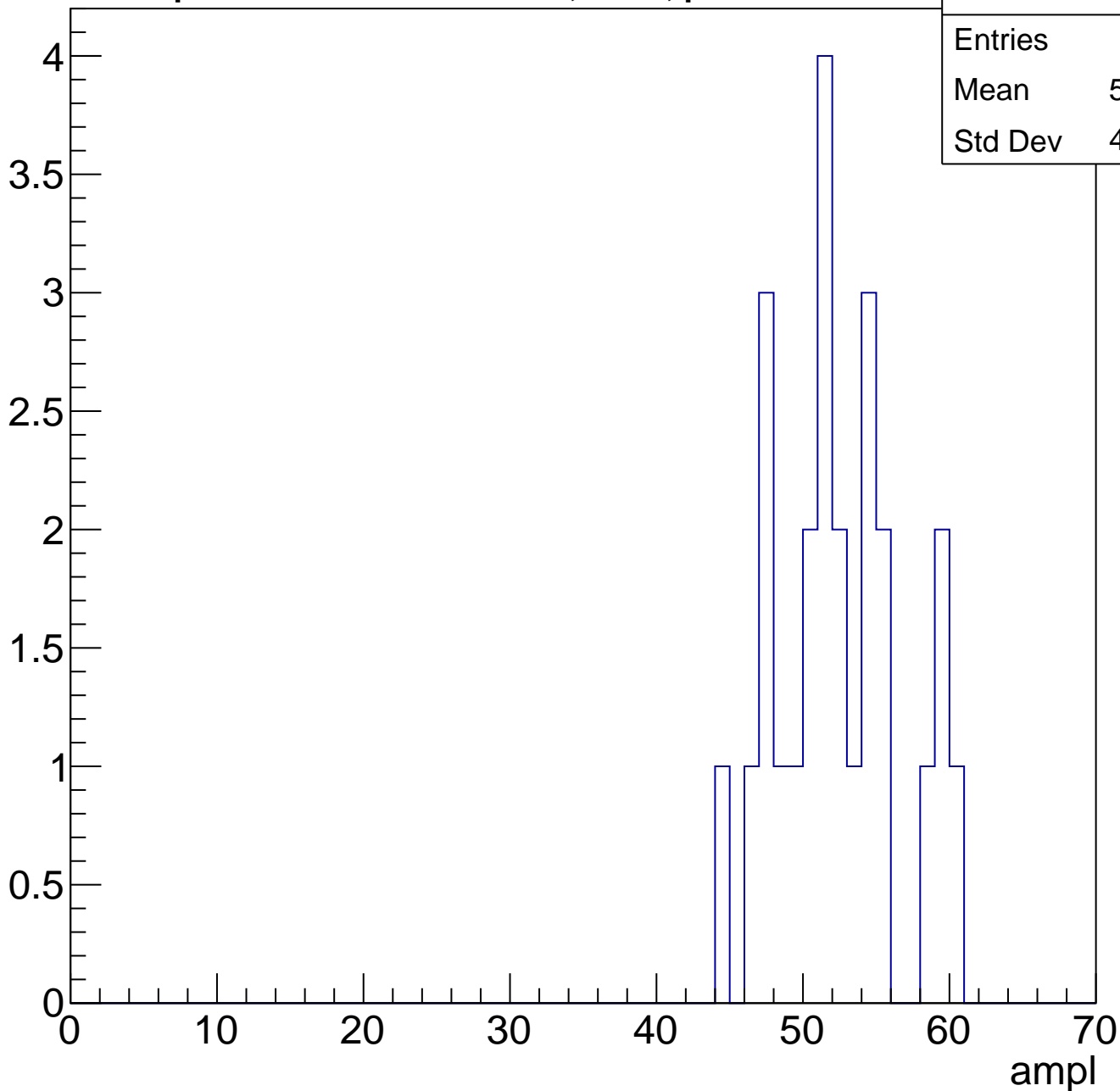


Entries	42
Mean	42.33
Std Dev	14.32

B1L103S, U14-ch124, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	25
Mean	51.88
Std Dev	4.198

B1L103S, U14-ch124, adc5

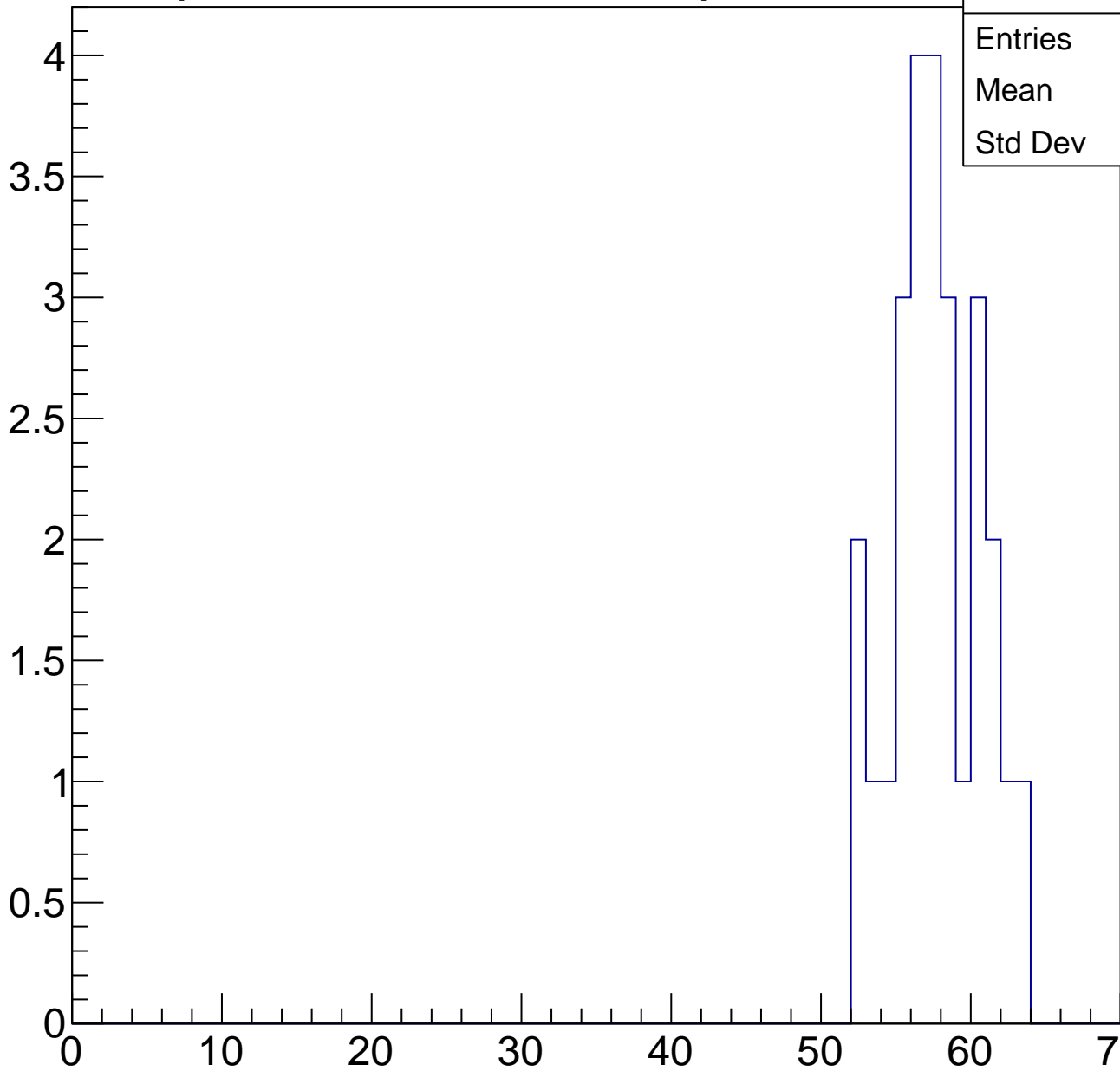
calib_packv5_041523_1651.root, FC#0, port C2

Entry

4
3.5
3
2.5
2
1.5
1
0.5
0

Entries	26
Mean	57.23
Std Dev	2.886

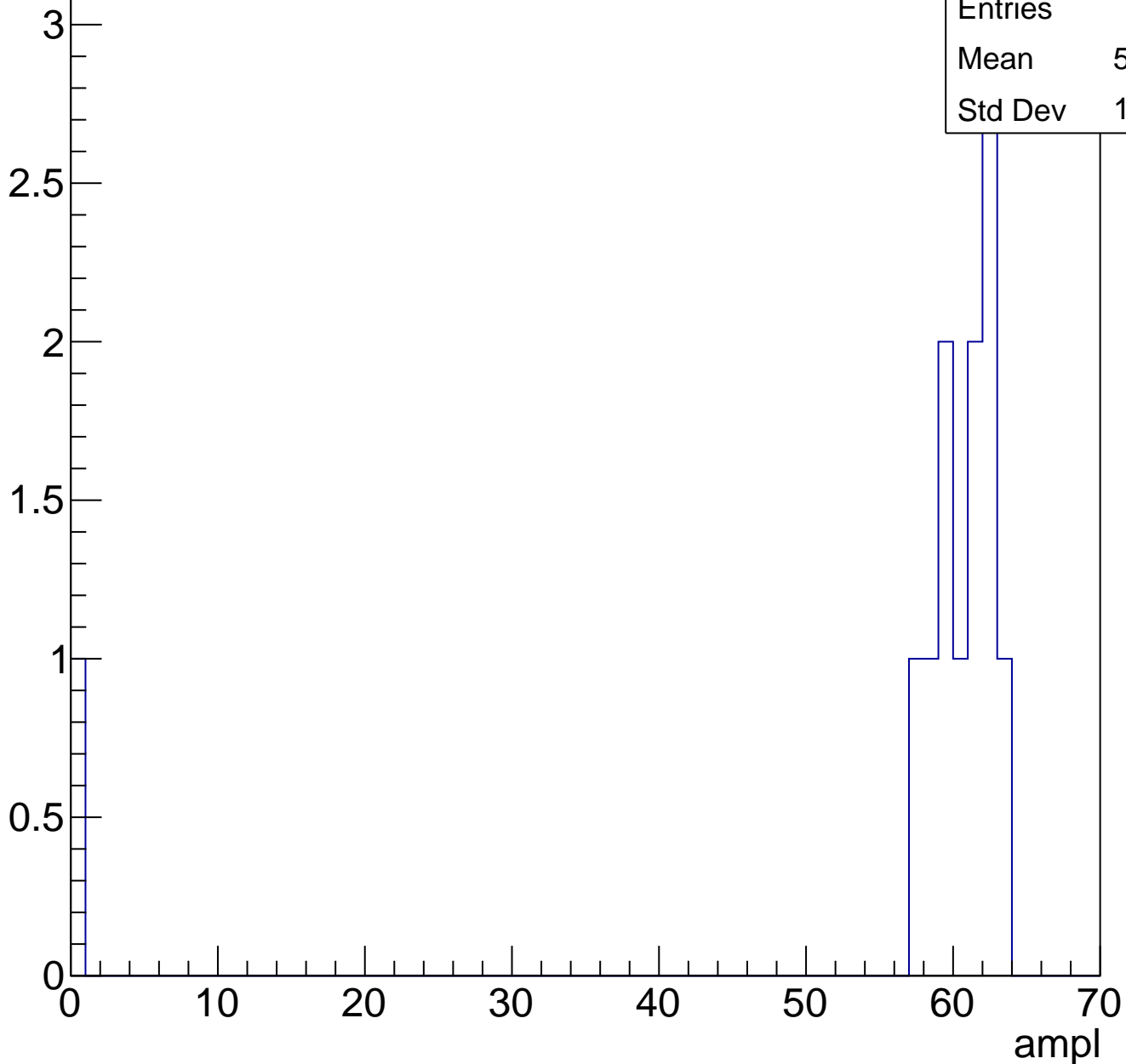
ampl



B1L103S, U14-ch124, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

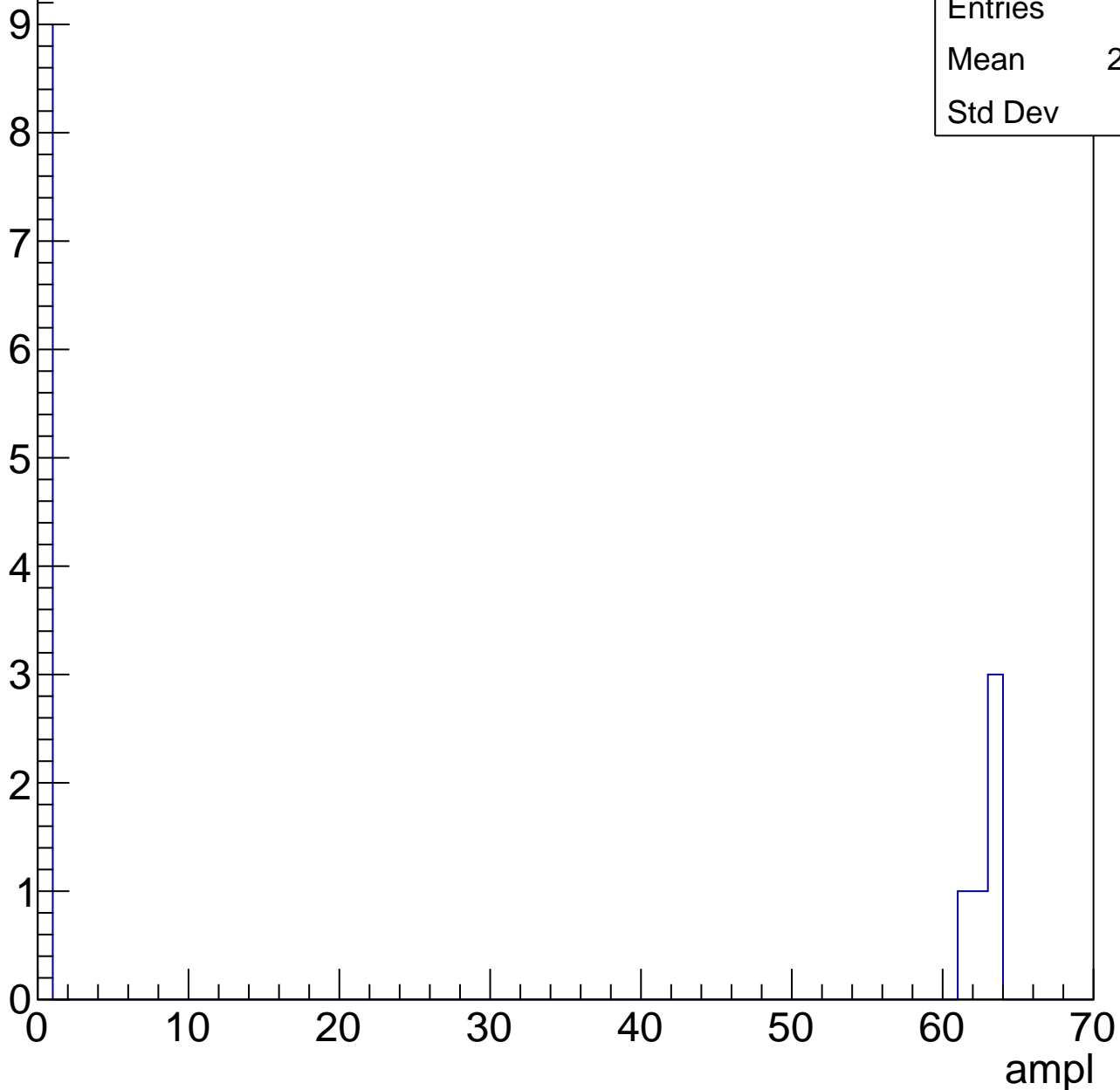


B1L103S, U14-ch124, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	14
Mean	22.29
Std Dev	29.9



B1L103S, U14-ch125, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	42
Mean	19.71
Std Dev	12.09

Entry

10

8

6

4

2

0

0

10

20

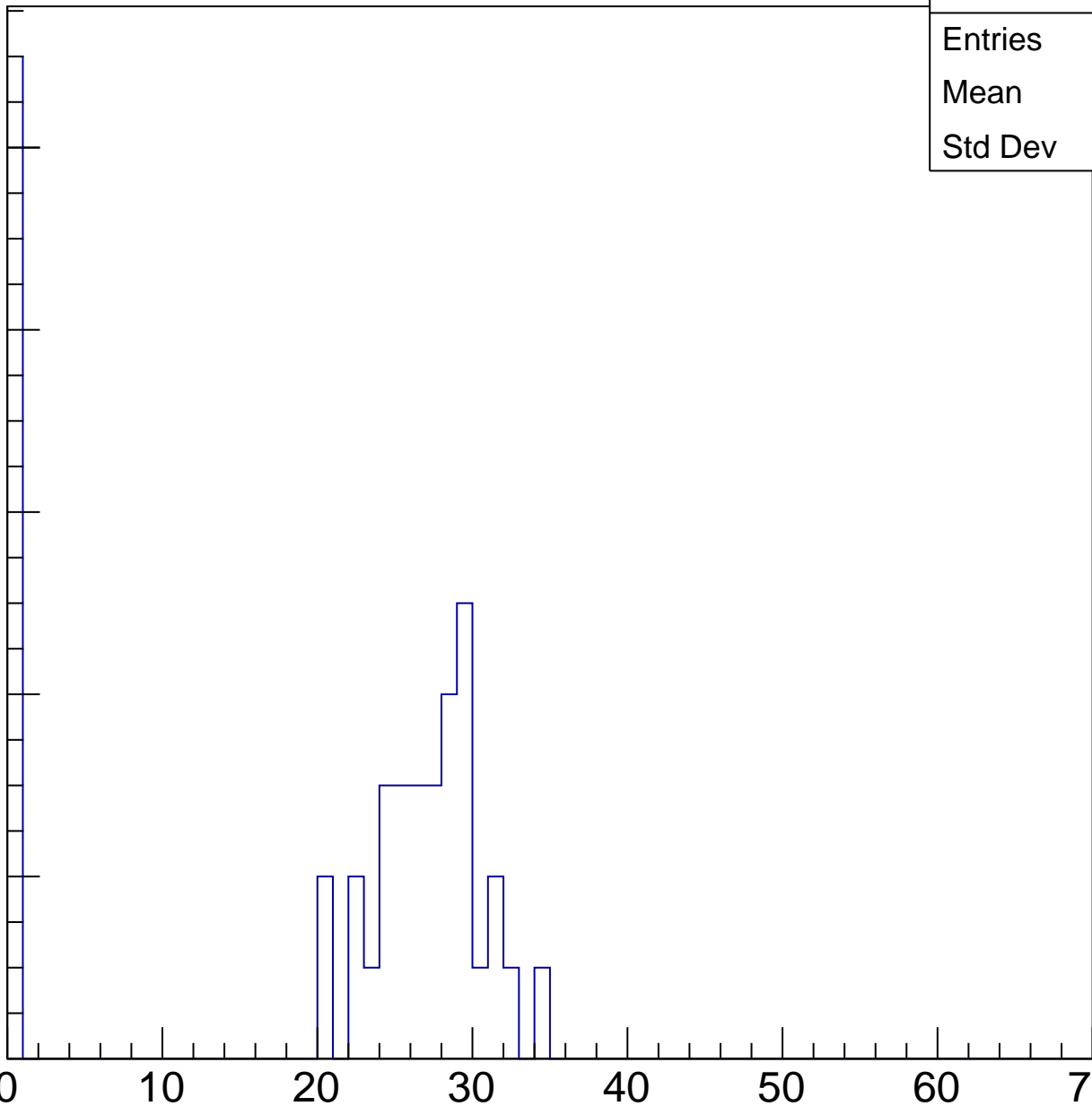
30

40

50

60

ampl

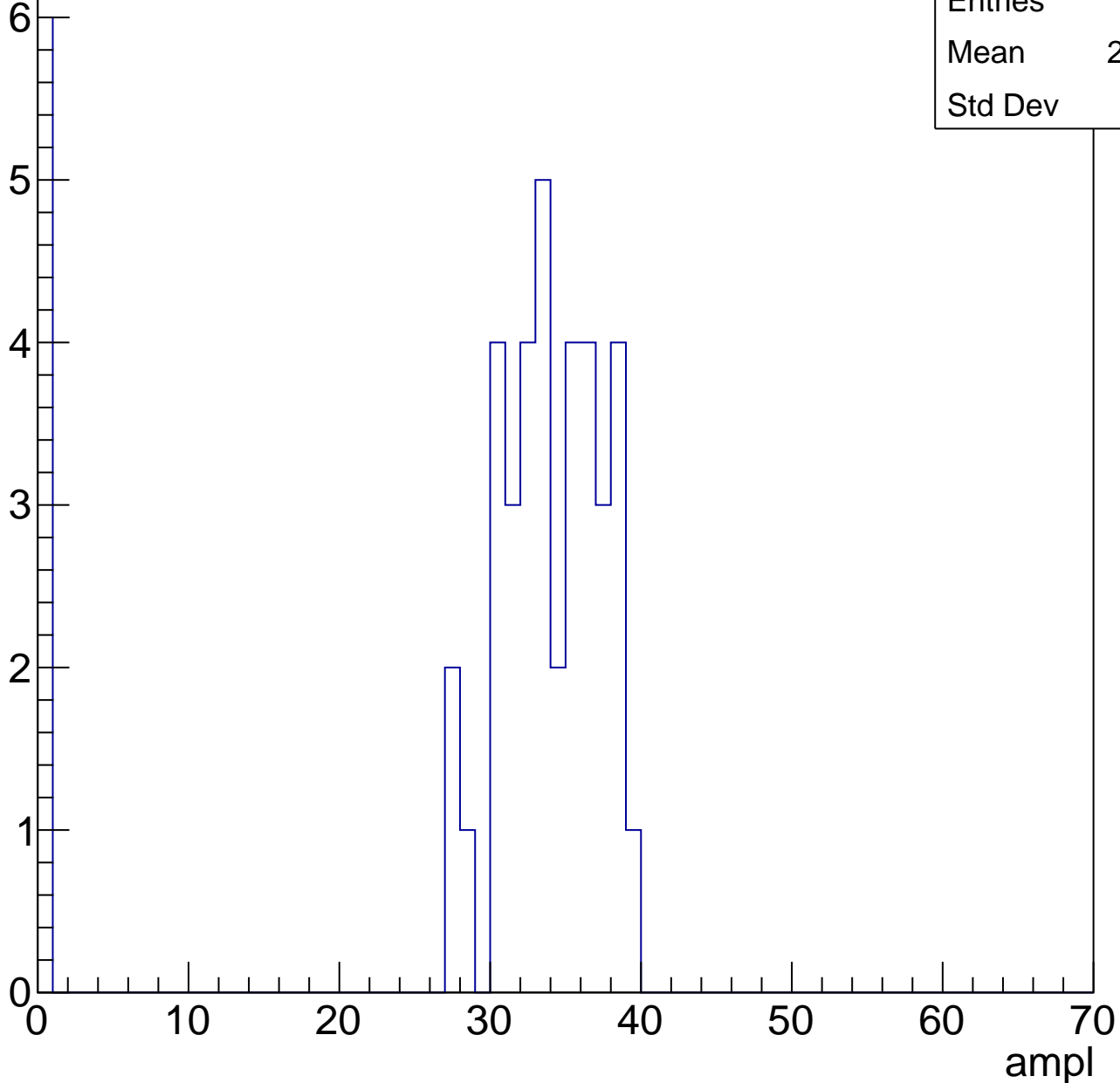


B1L103S, U14-ch125, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

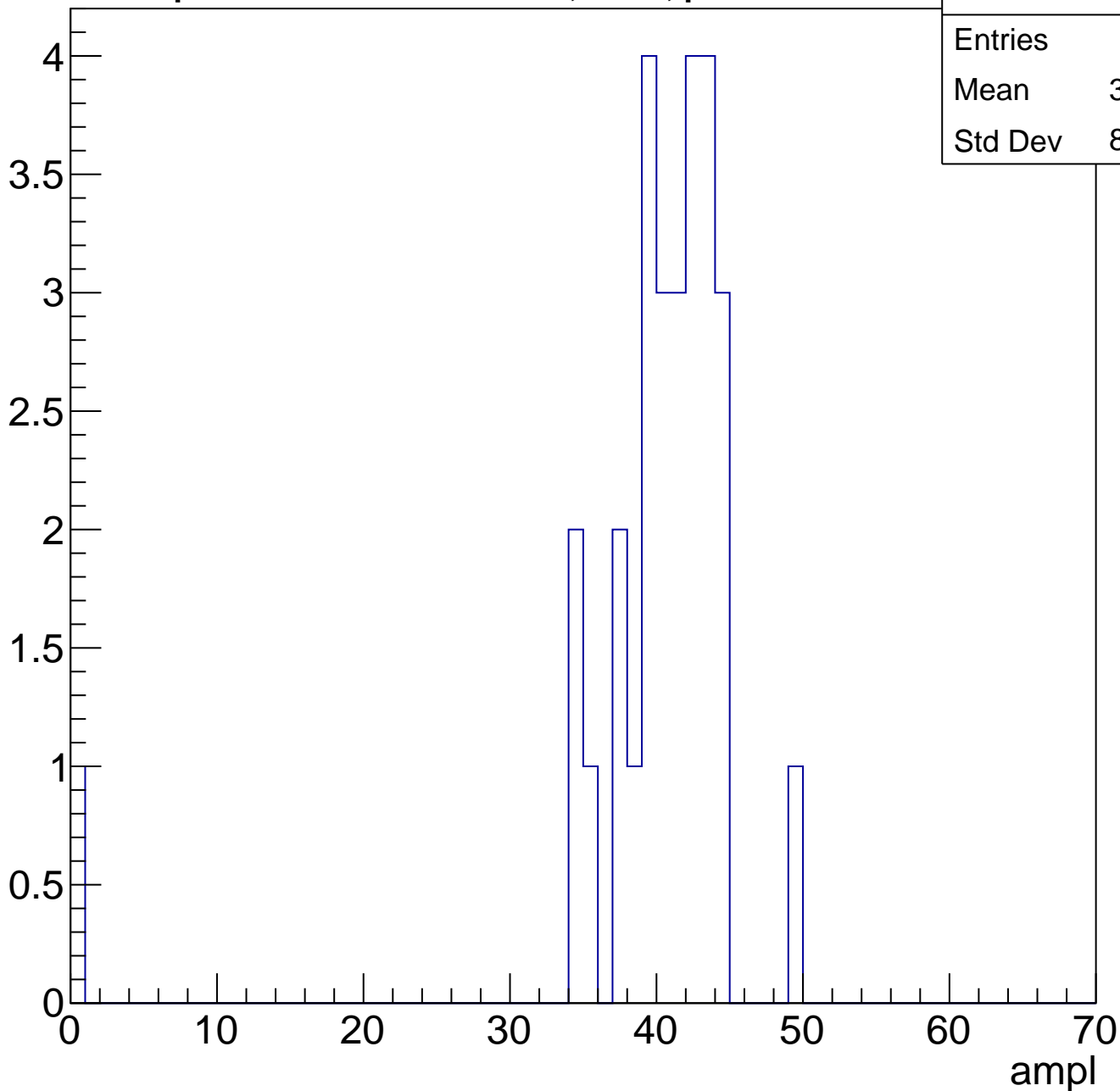
Entries	43
Mean	28.88
Std Dev	12



B1L103S, U14-ch125, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

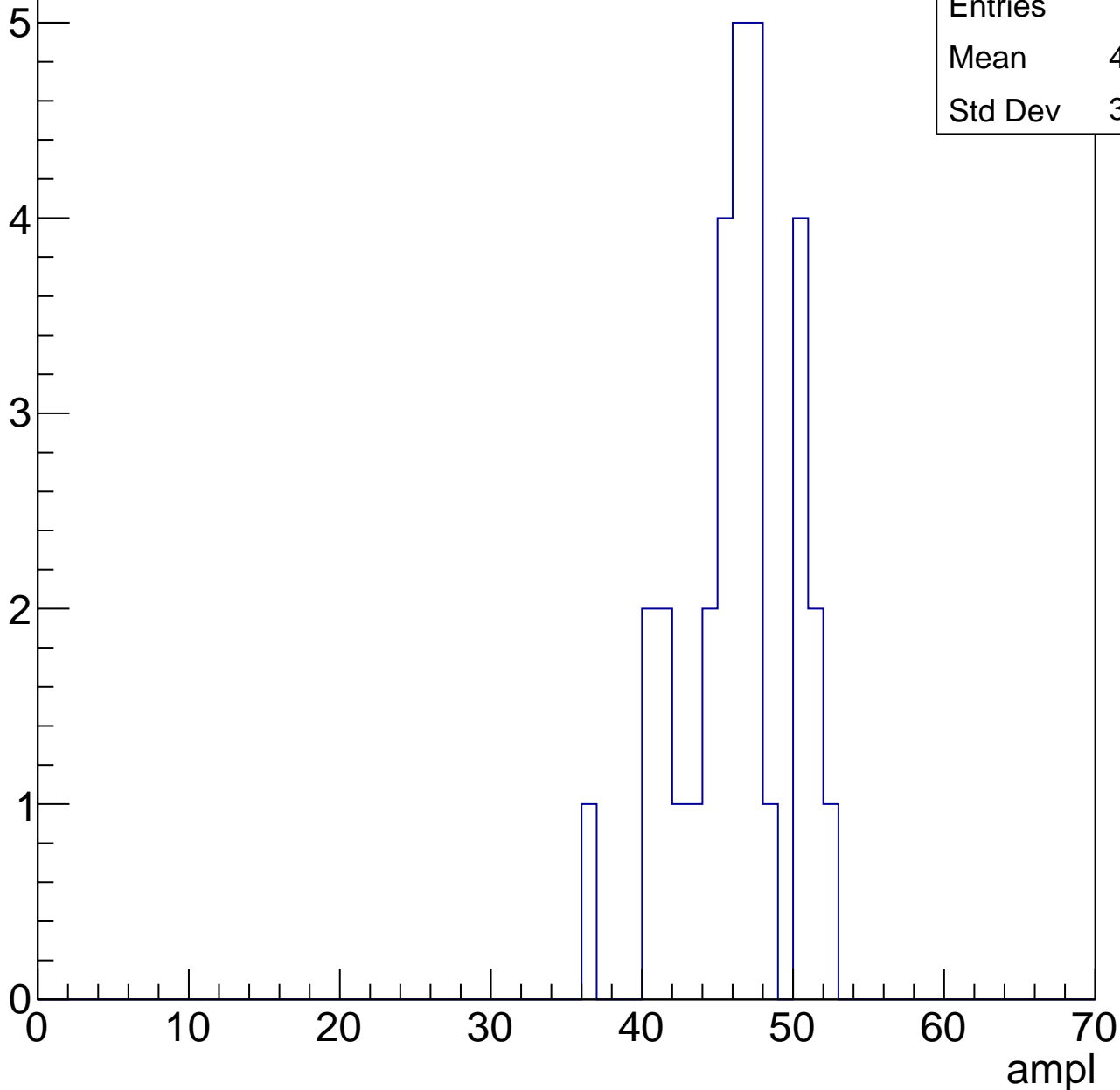


B1L103S, U14-ch125, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	31
Mean	45.74
Std Dev	3.663



B1L103S, U14-ch125, adc4

calib_packv5_041523_1651.root, FC#0, port C2

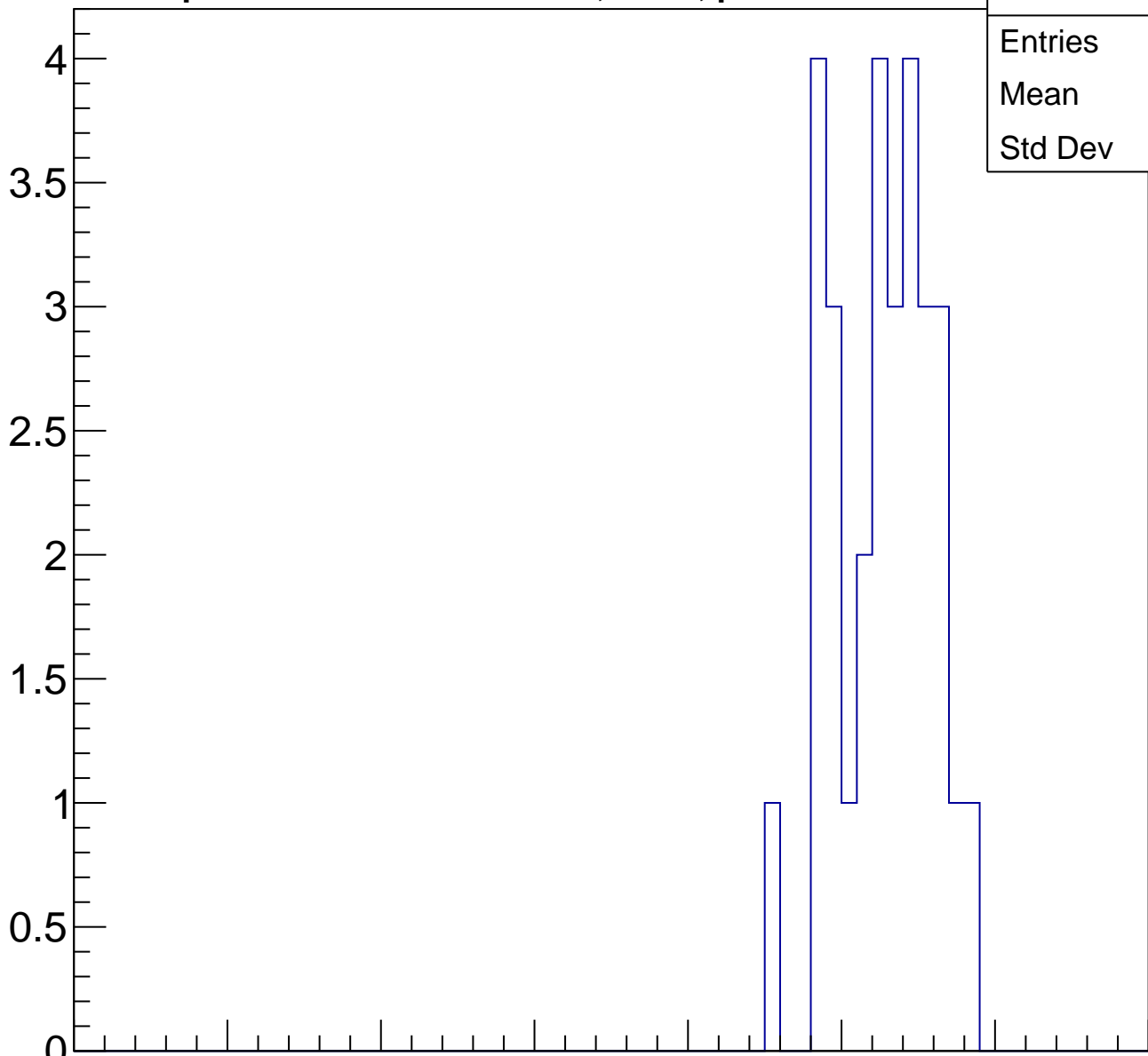
Entry

4
3.5
3
2.5
2
1.5
1
0.5
0

Entries	30
Mean	52.23
Std Dev	3.159

0 10 20 30 40 50 60 70

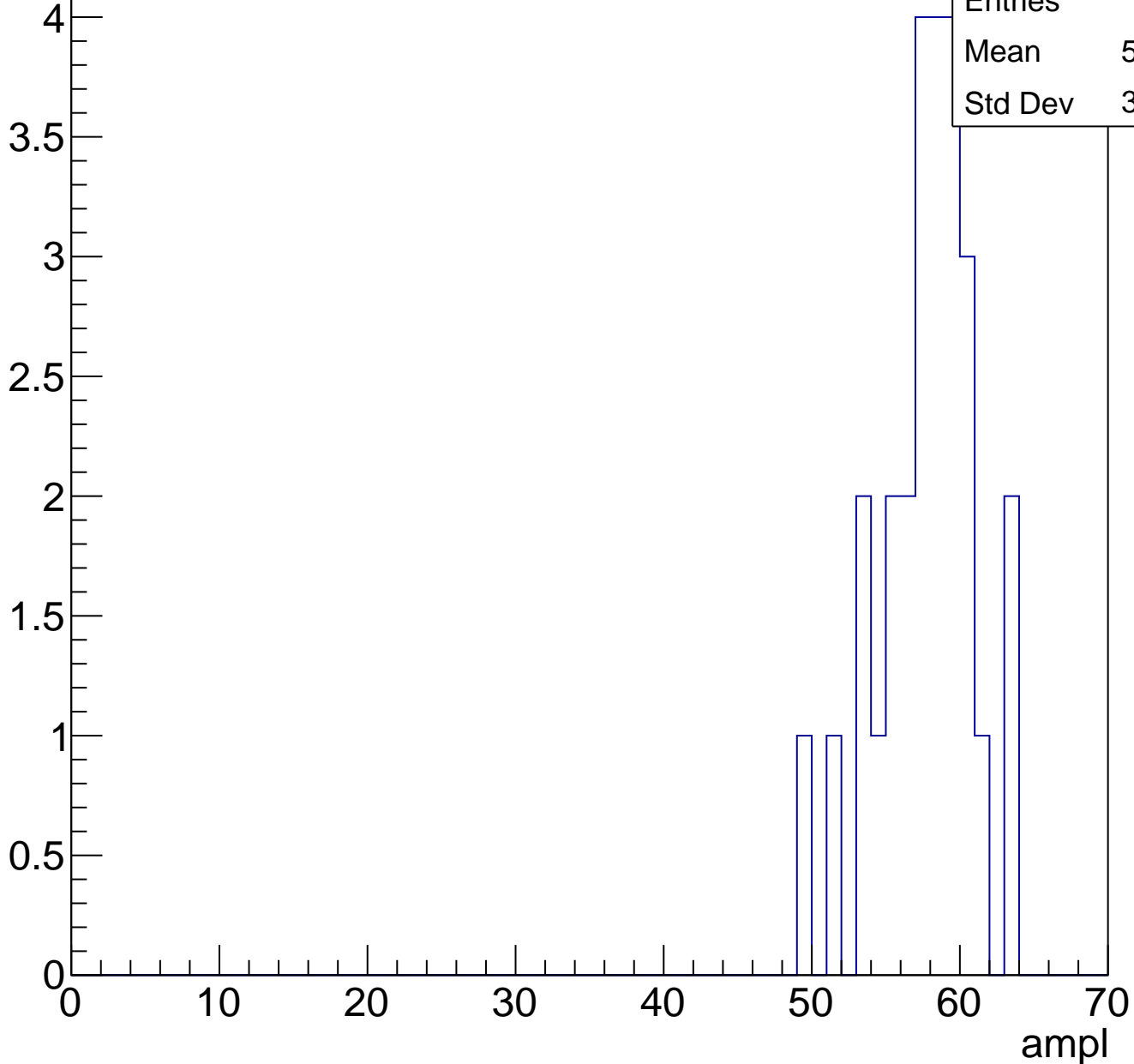
ampl



B1L103S, U14-ch125, adc5

calib_packv5_041523_1651.root, FC#0, port C2

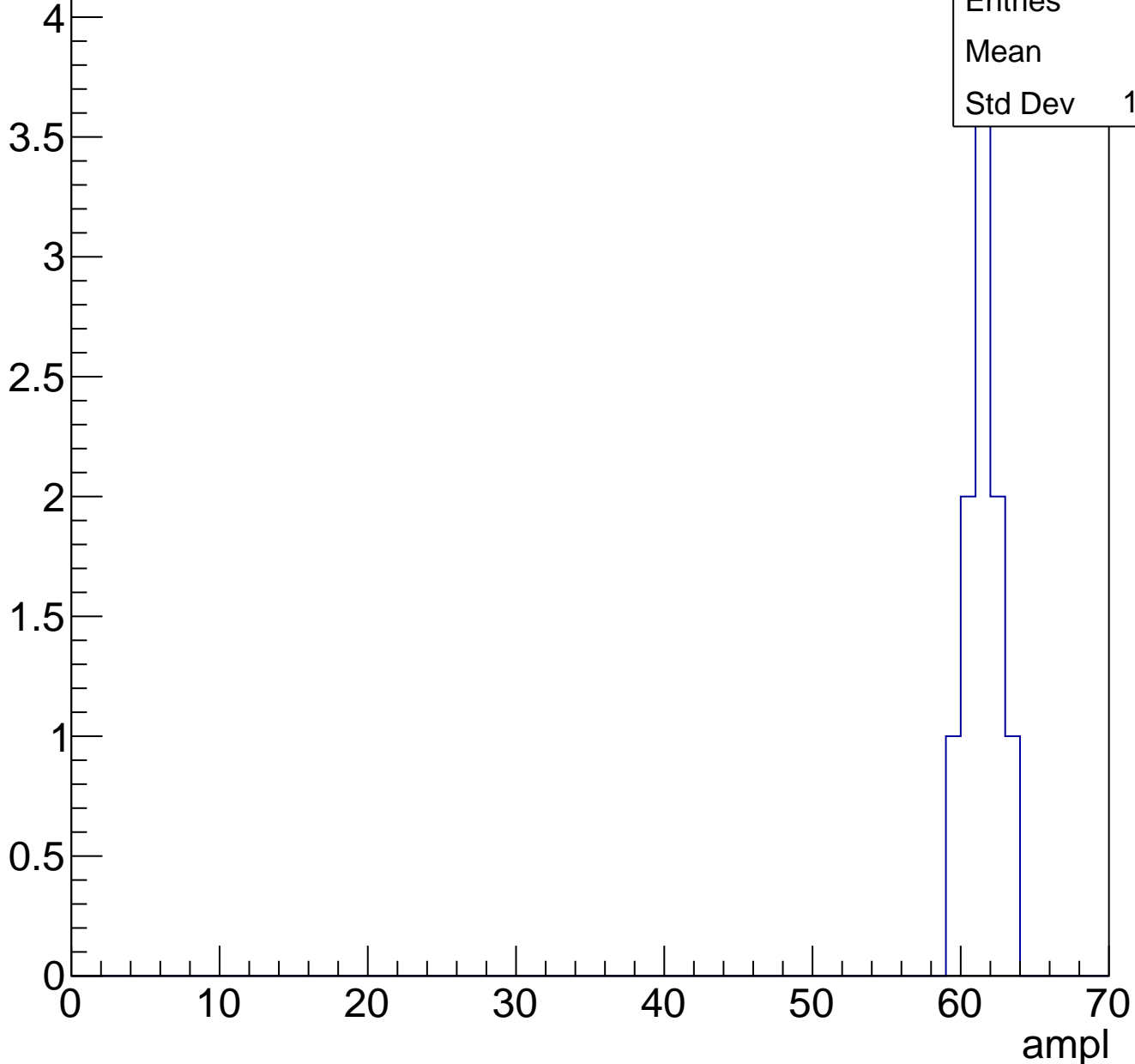
Entry



B1L103S, U14-ch125, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	10
Mean	61
Std Dev	1.095

B1L103S, U14-ch125, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	16
Mean	19.5
Std Dev	28.92

Entry

10

8

6

4

2

0

0

10

20

30

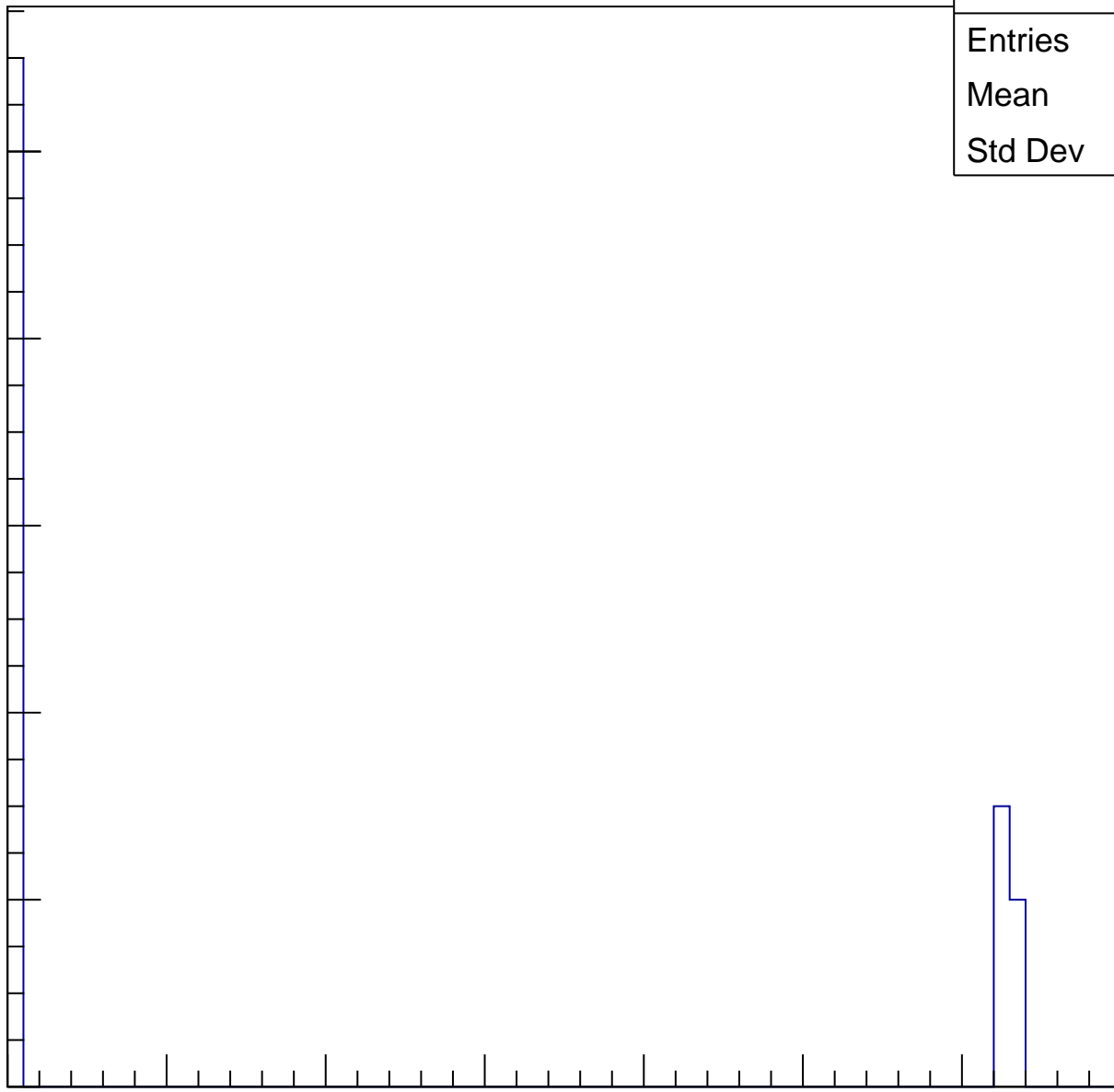
40

50

60

70

ampl



B1L103S, U14-ch126, adc0

calib_packv5_041523_1651.root, FC#0, port C2

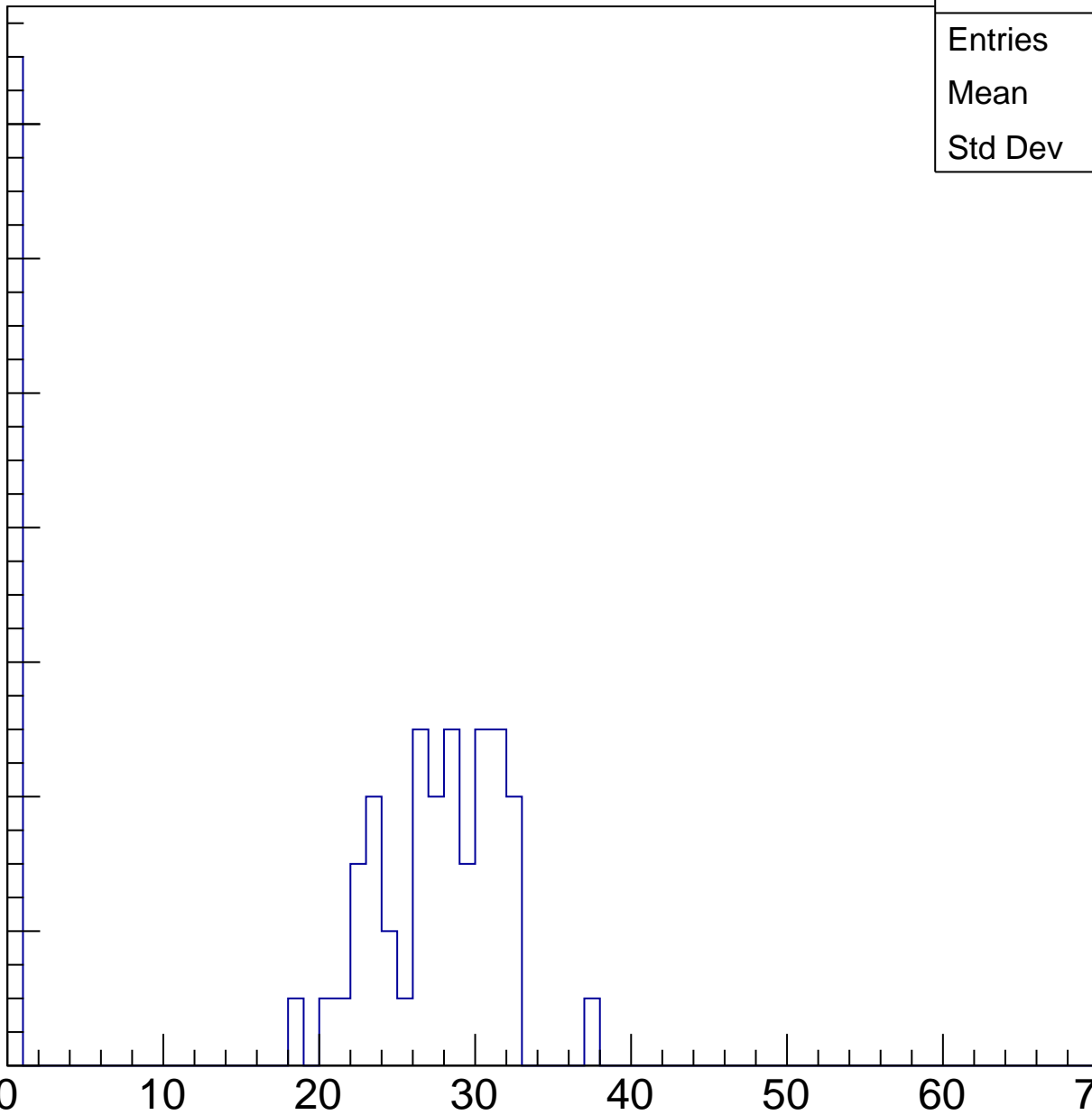
Entries	60
Mean	20.42
Std Dev	12.25

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

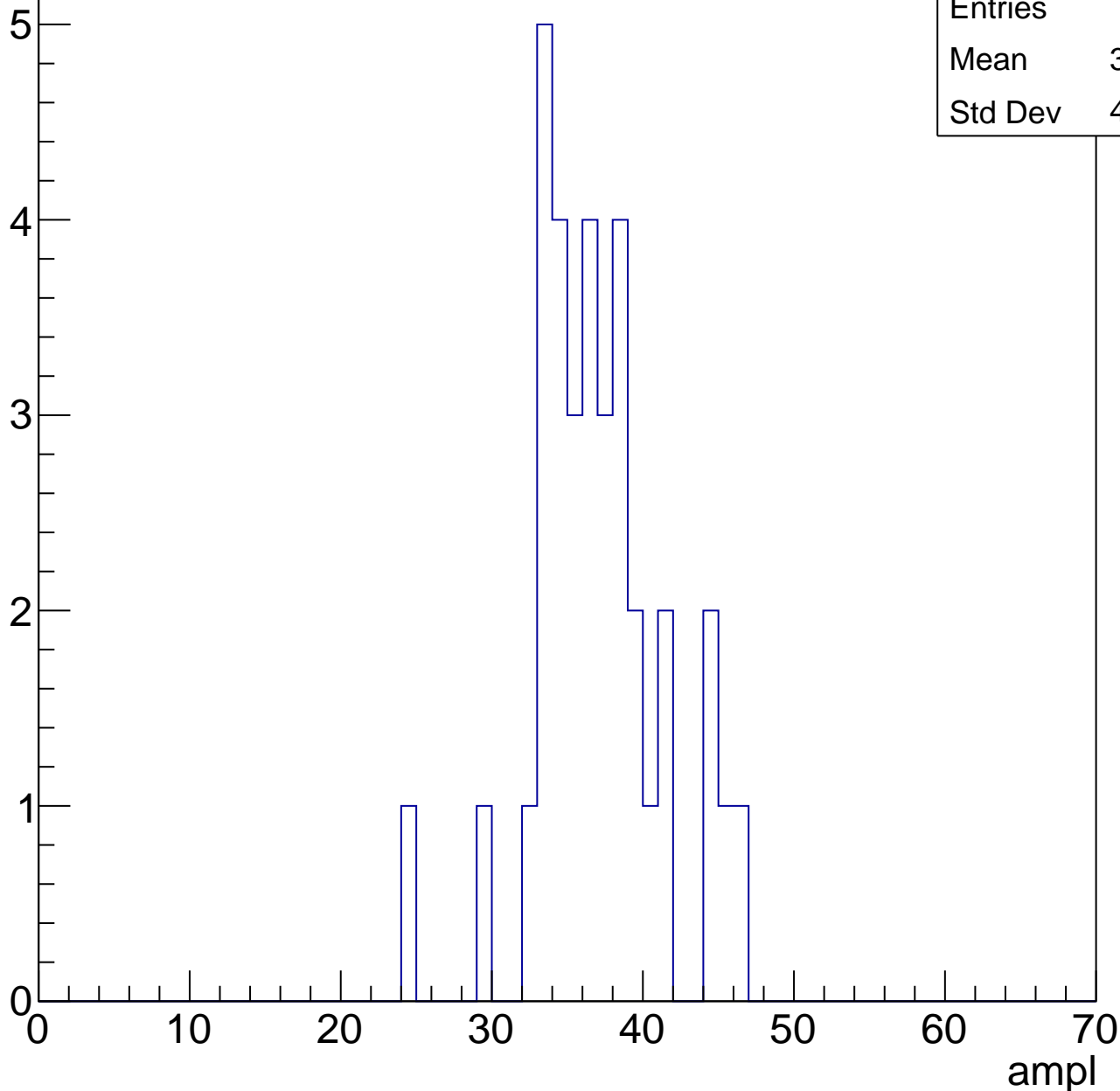


B1L103S, U14-ch126, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

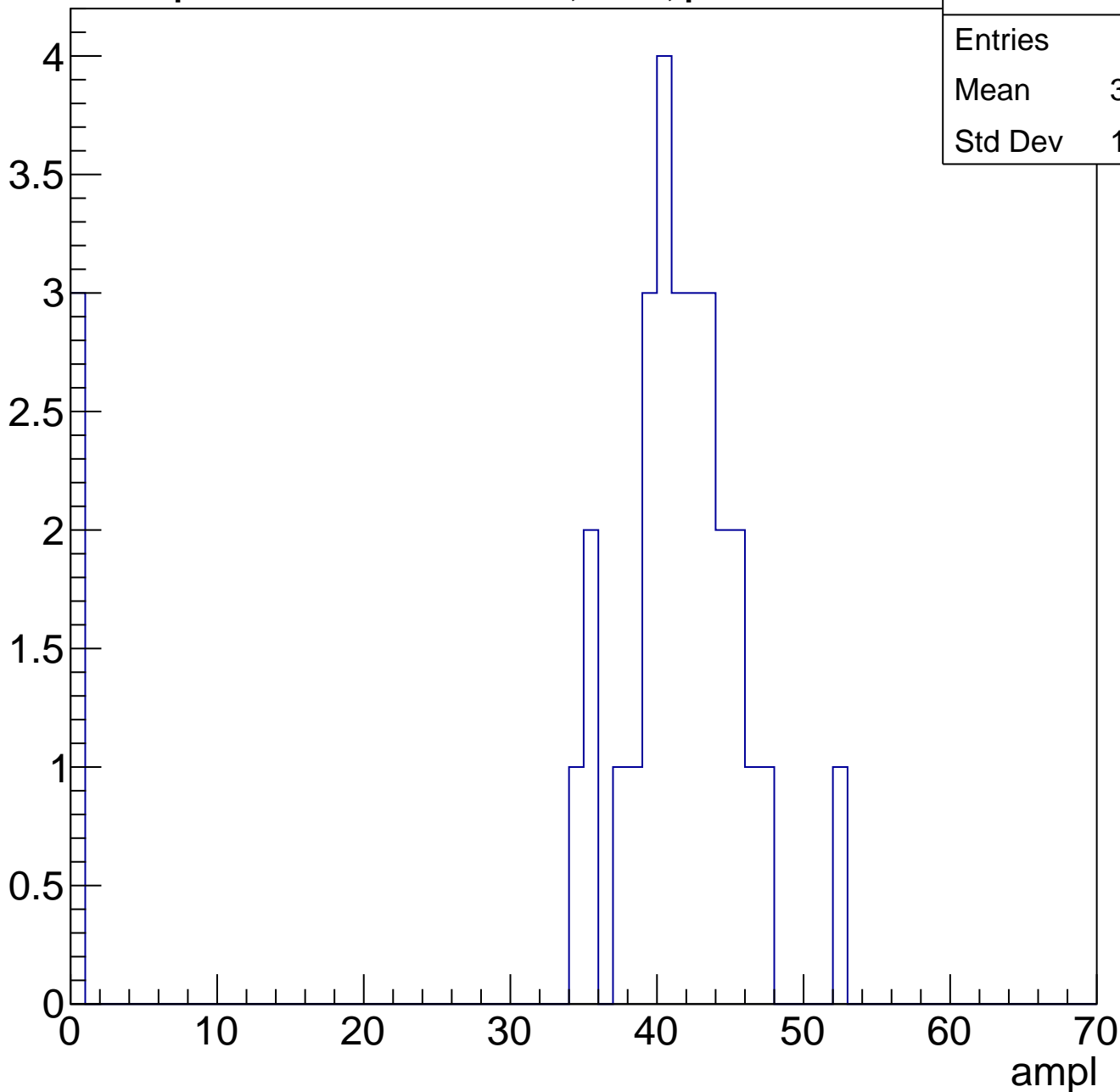
Entries	35
Mean	36.49
Std Dev	4.397



B1L103S, U14-ch126, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry



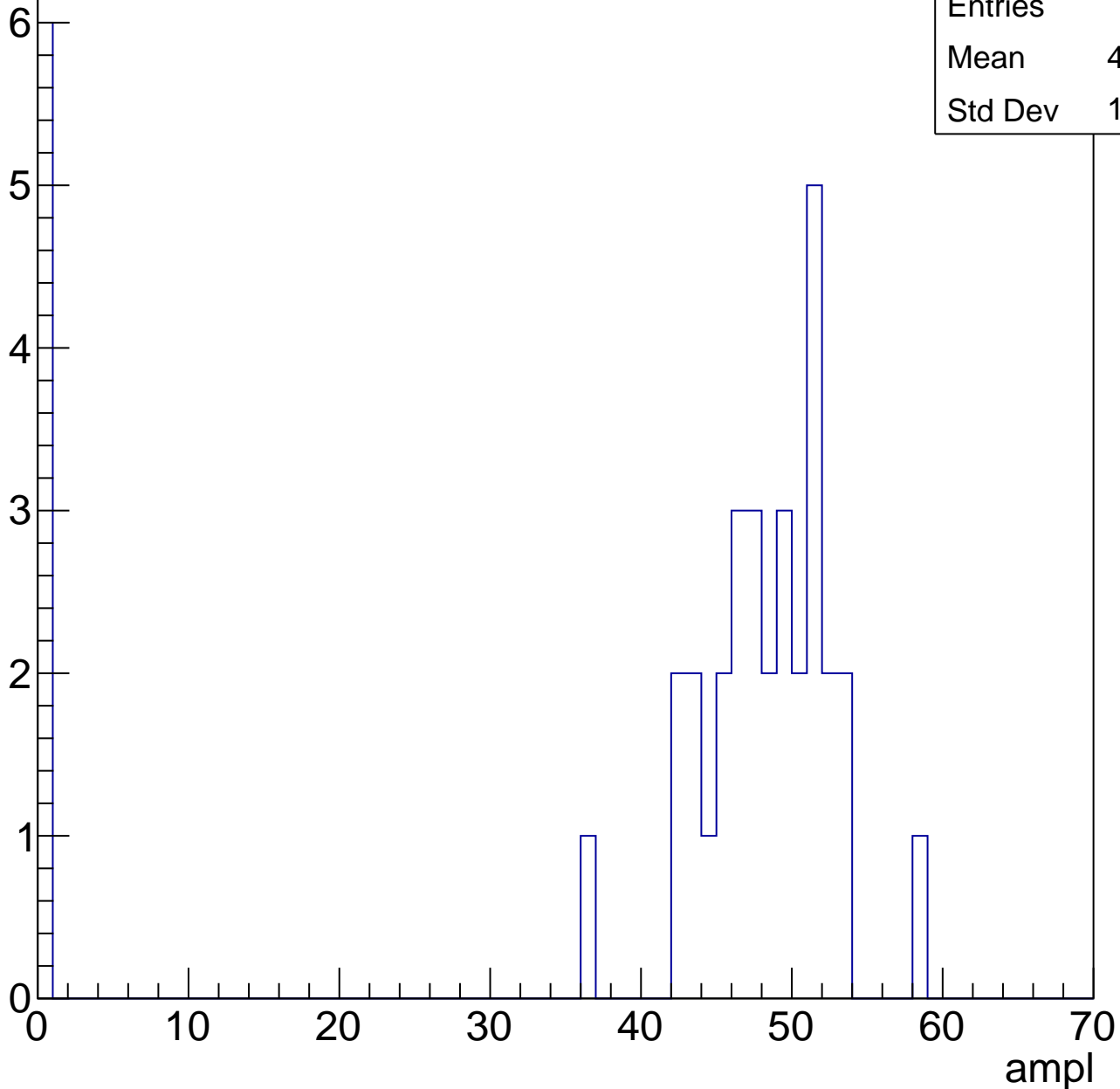
Entries	31
Mean	37.32
Std Dev	12.74

B1L103S, U14-ch126, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

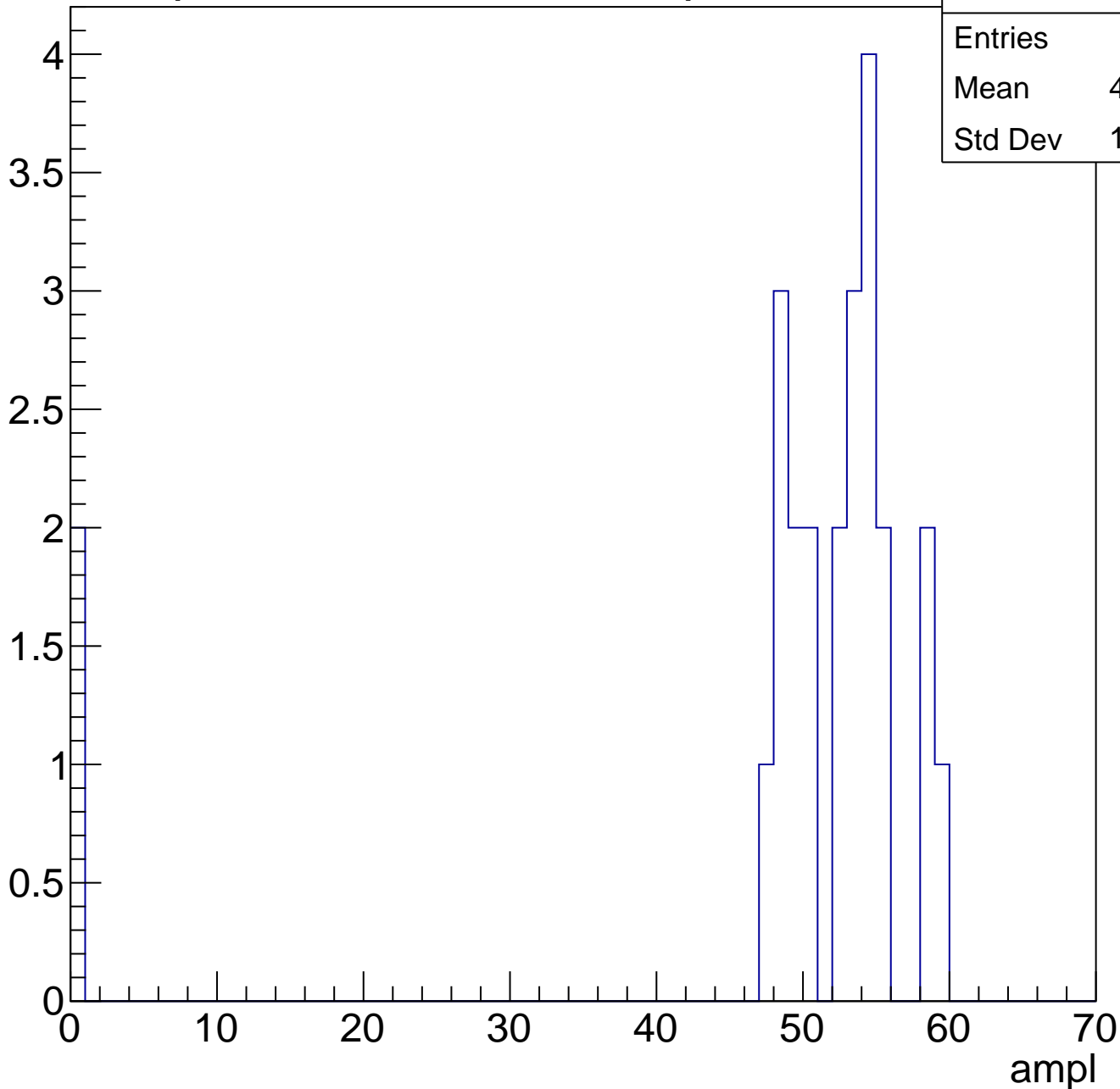
Entries	37
Mean	40.14
Std Dev	18.08



B1L103S, U14-ch126, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



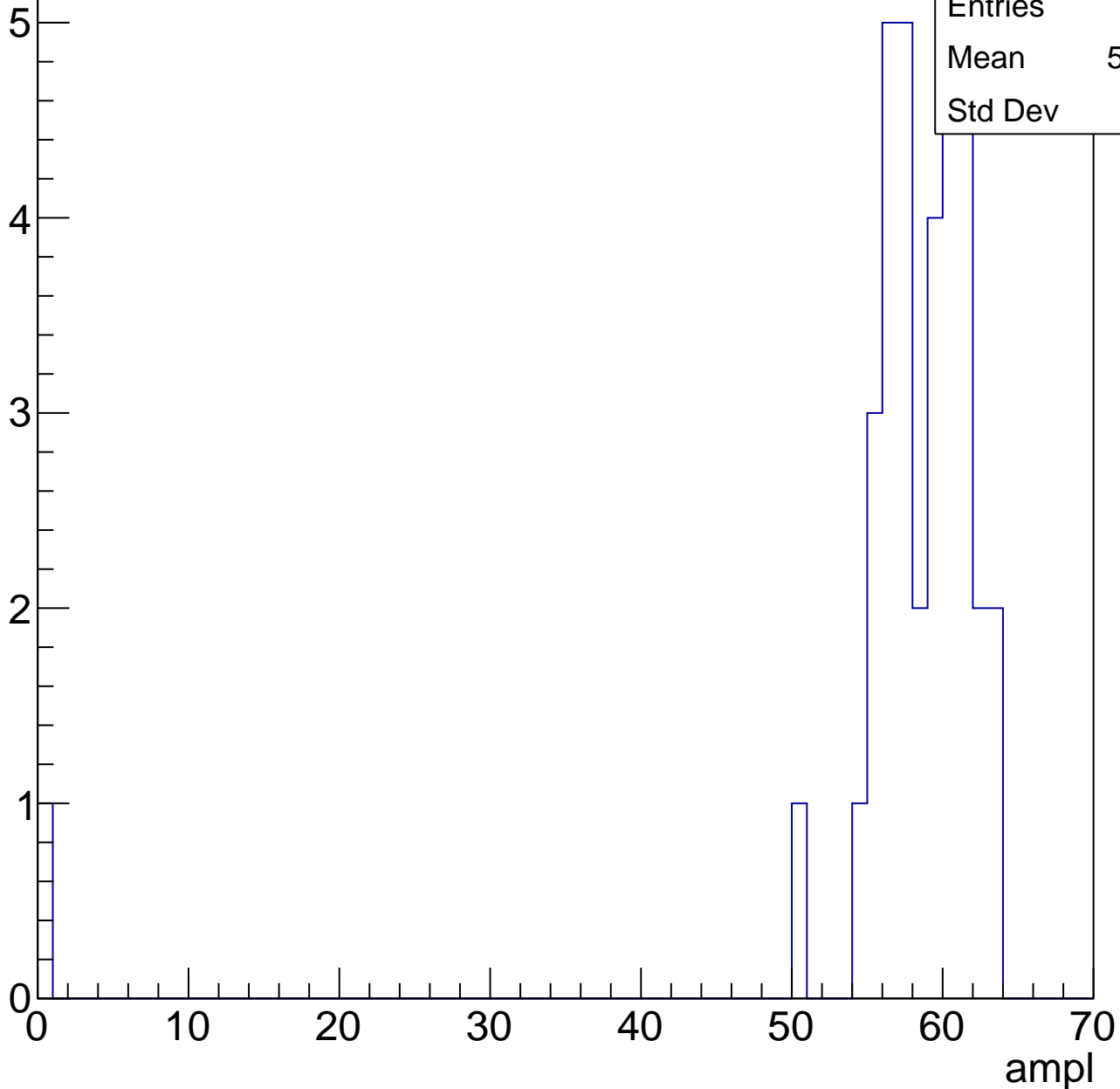
Entries	24
Mean	48.04
Std Dev	14.84

B1L103S, U14-ch126, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	36
Mean	56.69
Std Dev	9.98



B1L103S, U14-ch126, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

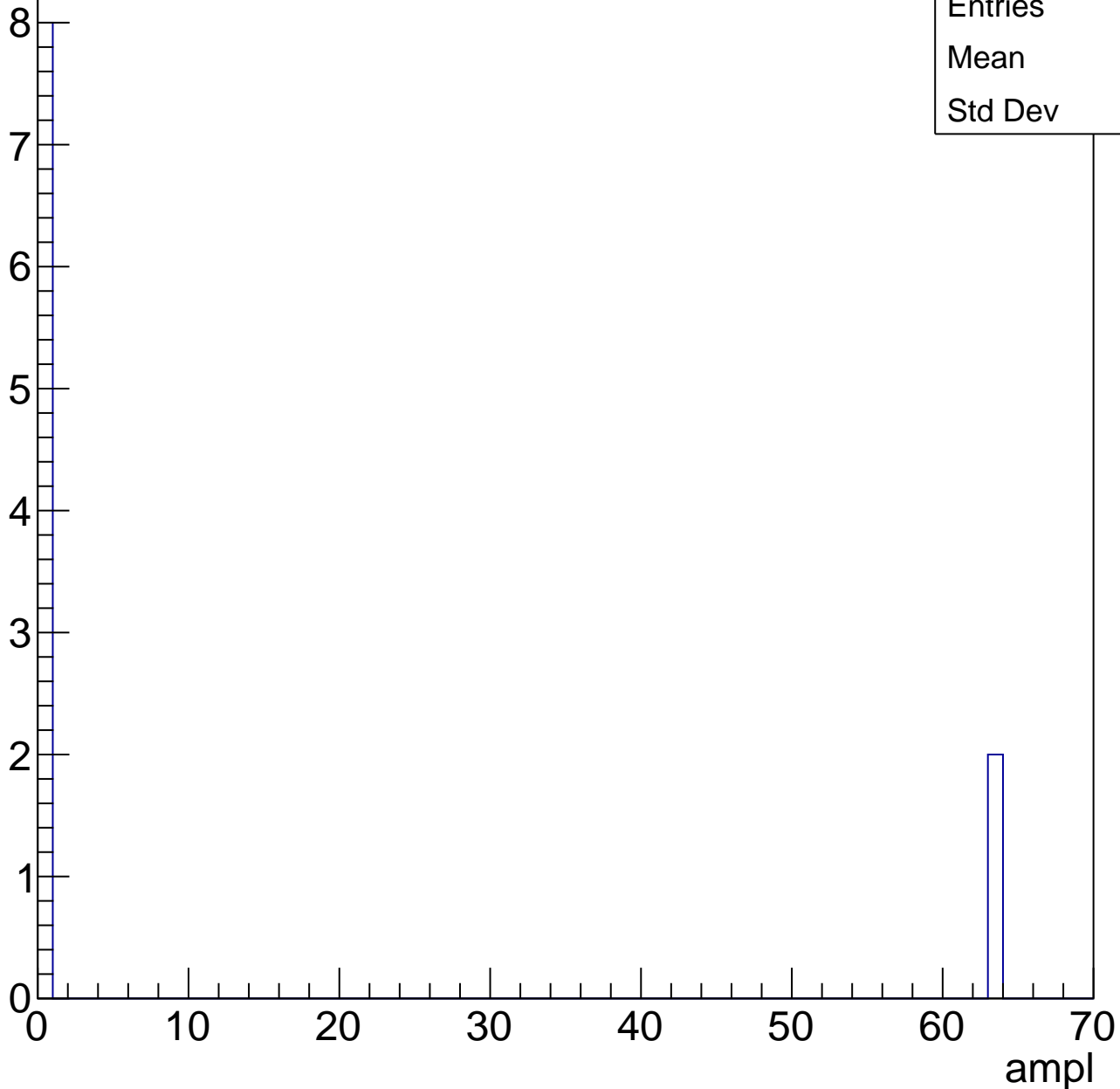


B1L103S, U14-ch126, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

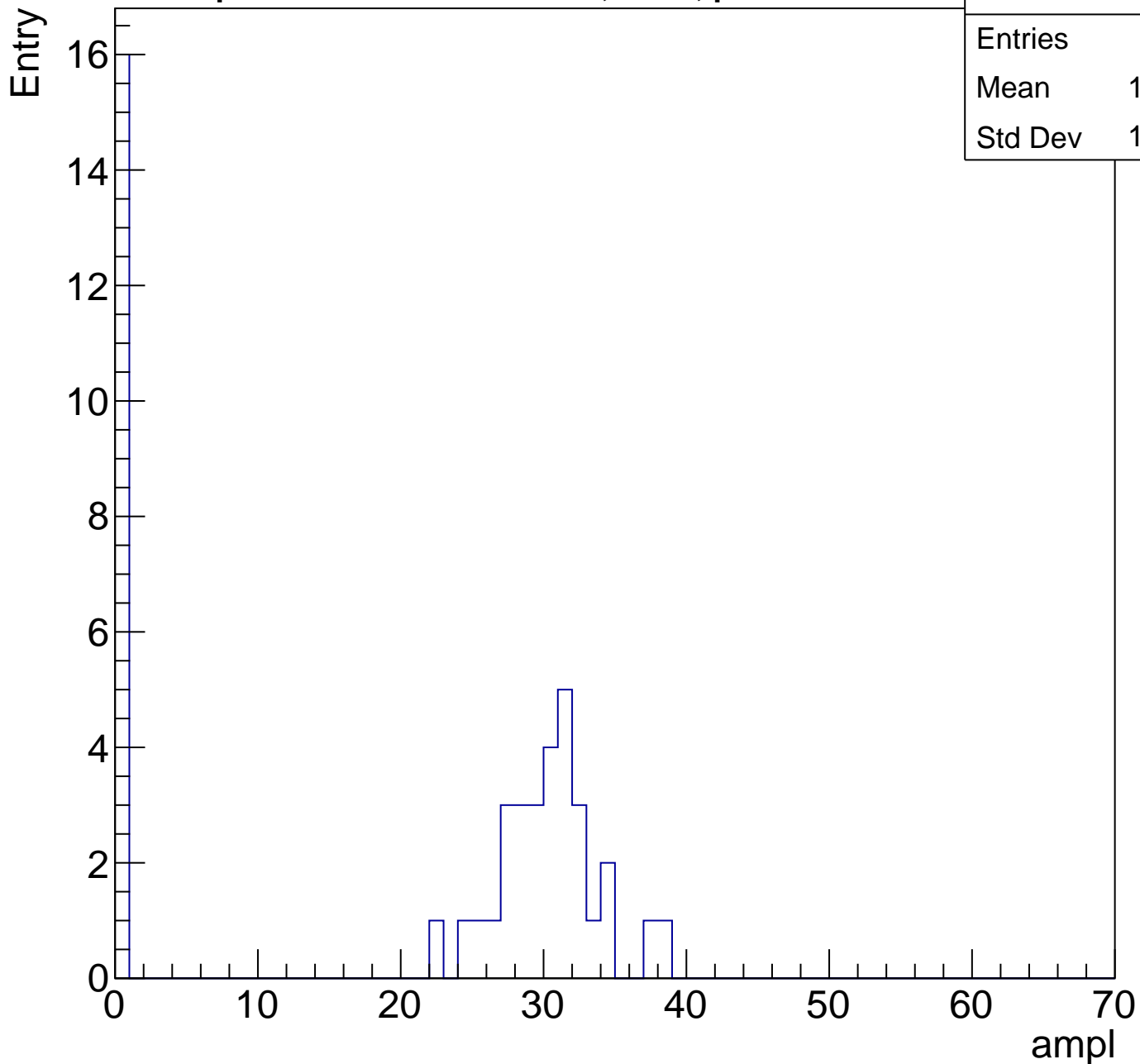
Entries	10
Mean	12.6
Std Dev	25.2



B1L103S, U14-ch127, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	46
Mean	19.48
Std Dev	14.49

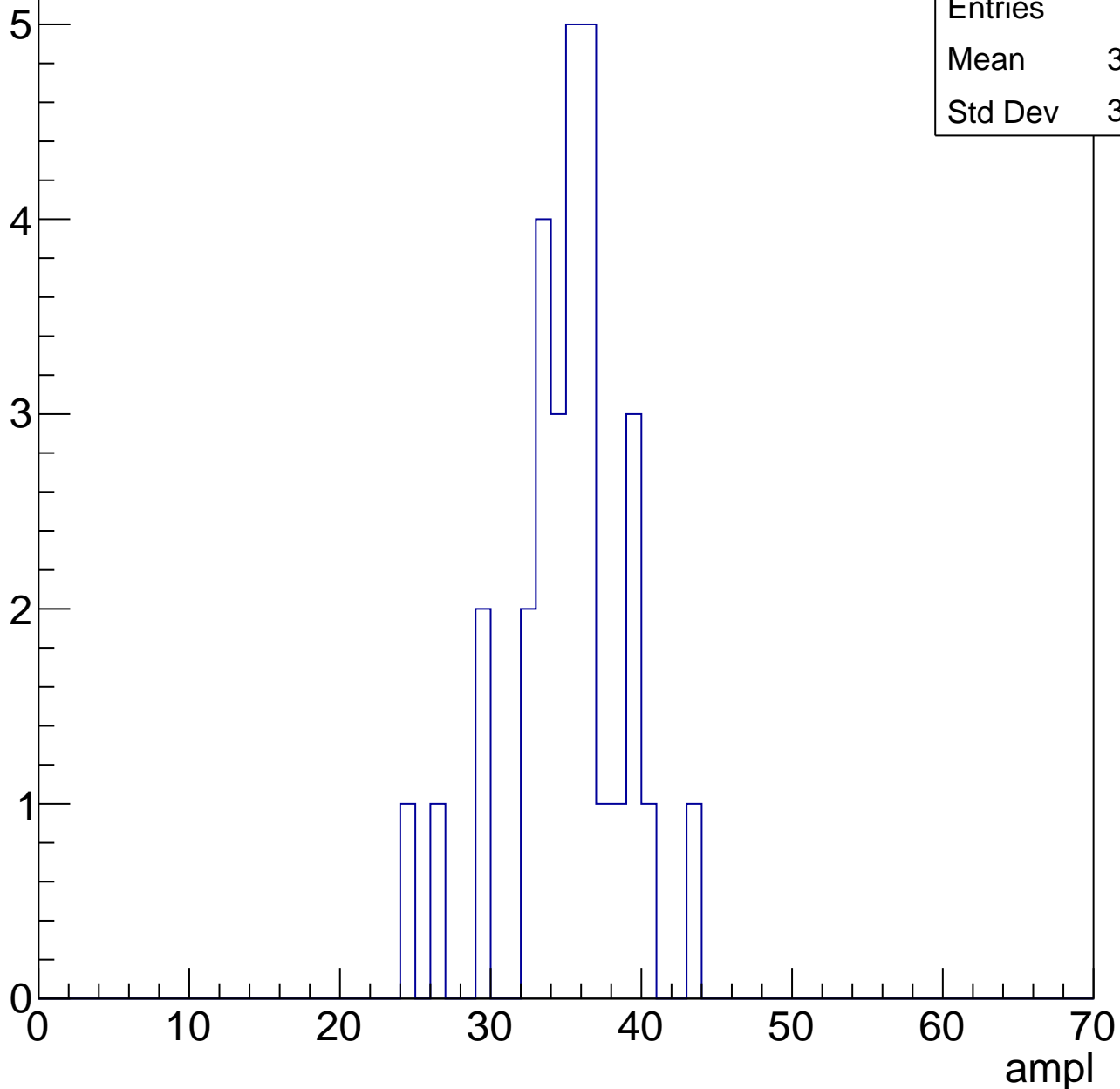


B1L103S, U14-ch127, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	30
Mean	34.53
Std Dev	3.914

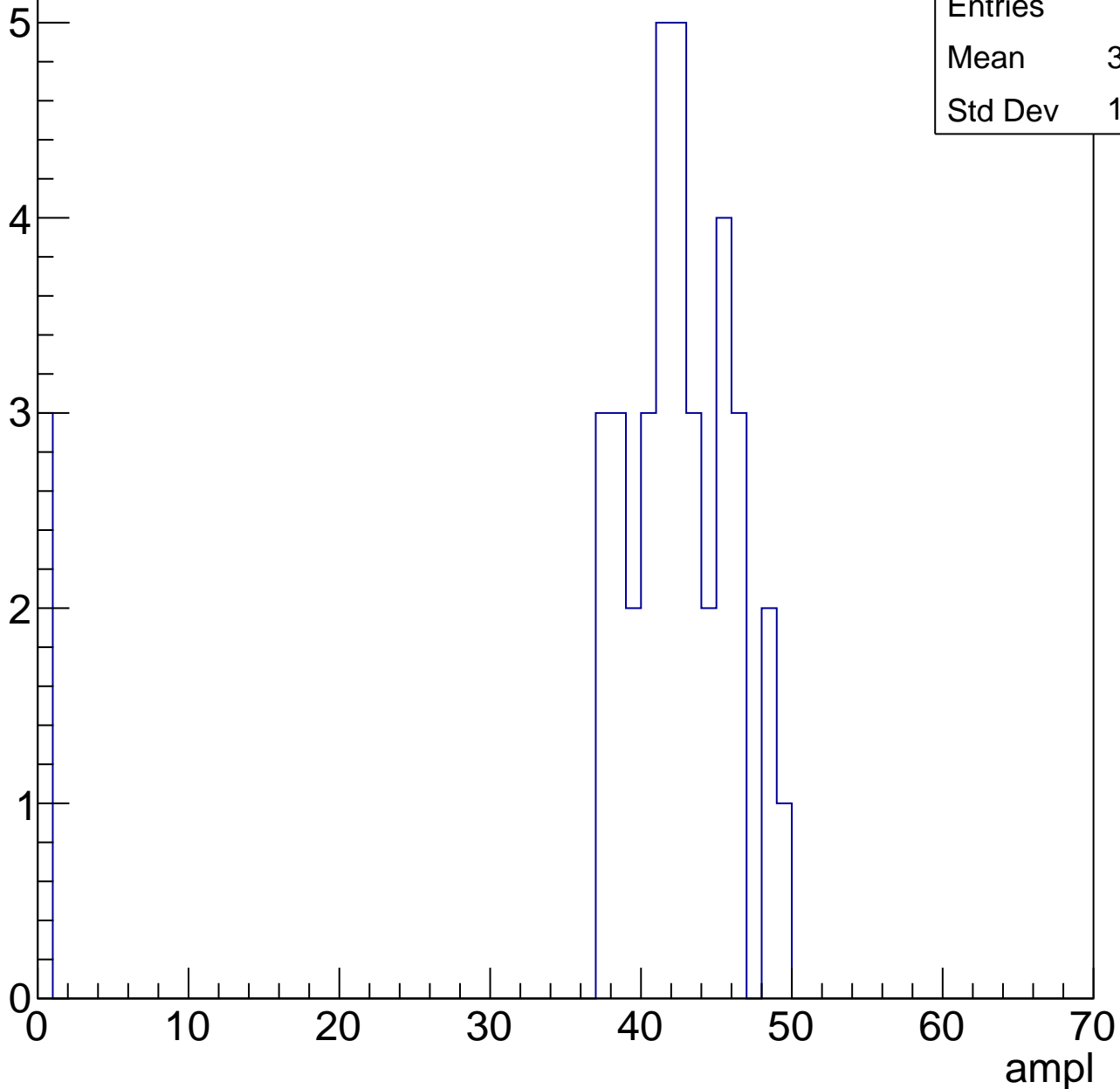


B1L103S, U14-ch127, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	38.92
Std Dev	11.65

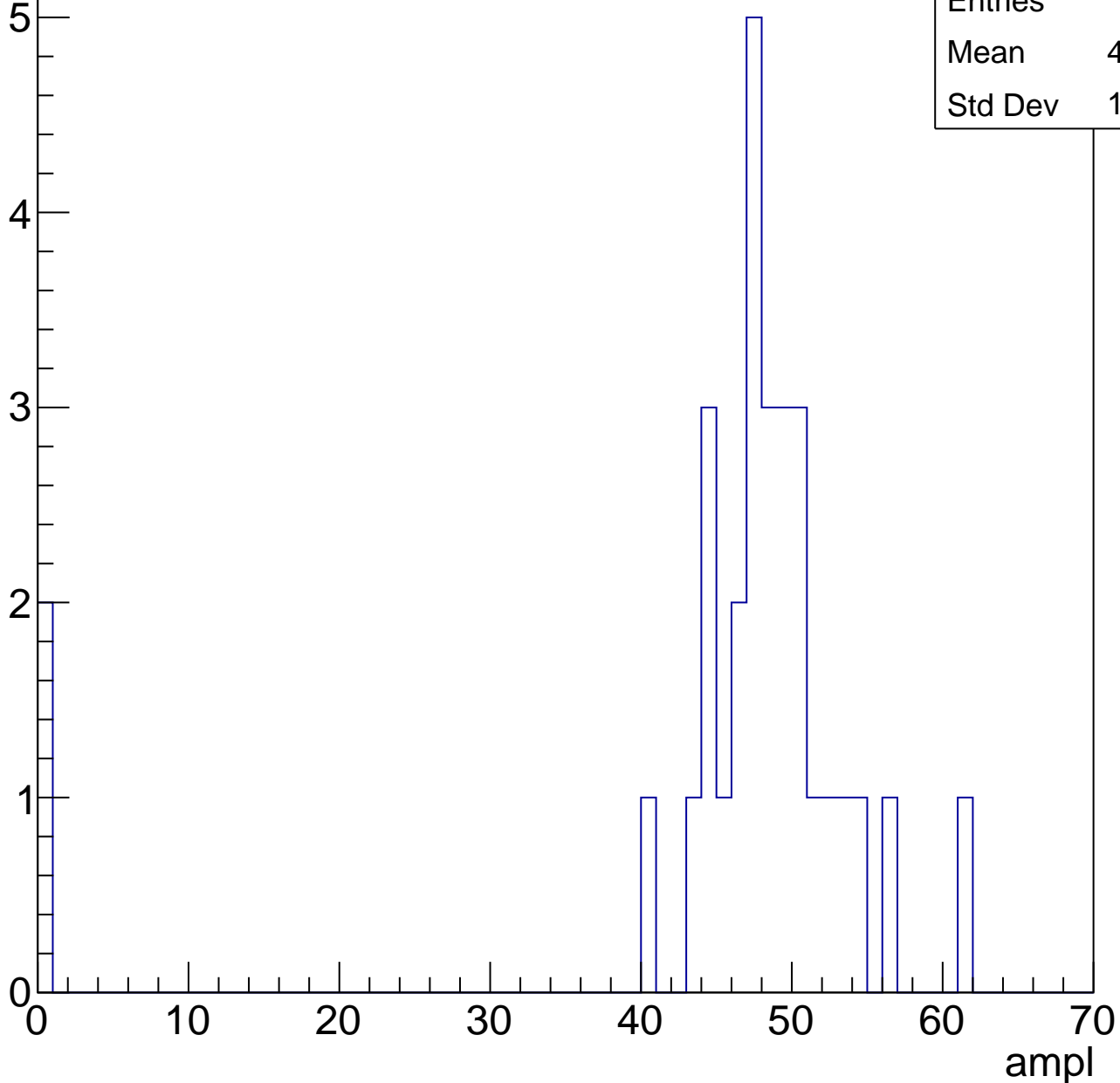


B1L103S, U14-ch127, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	30
Mean	45.17
Std Dev	12.73

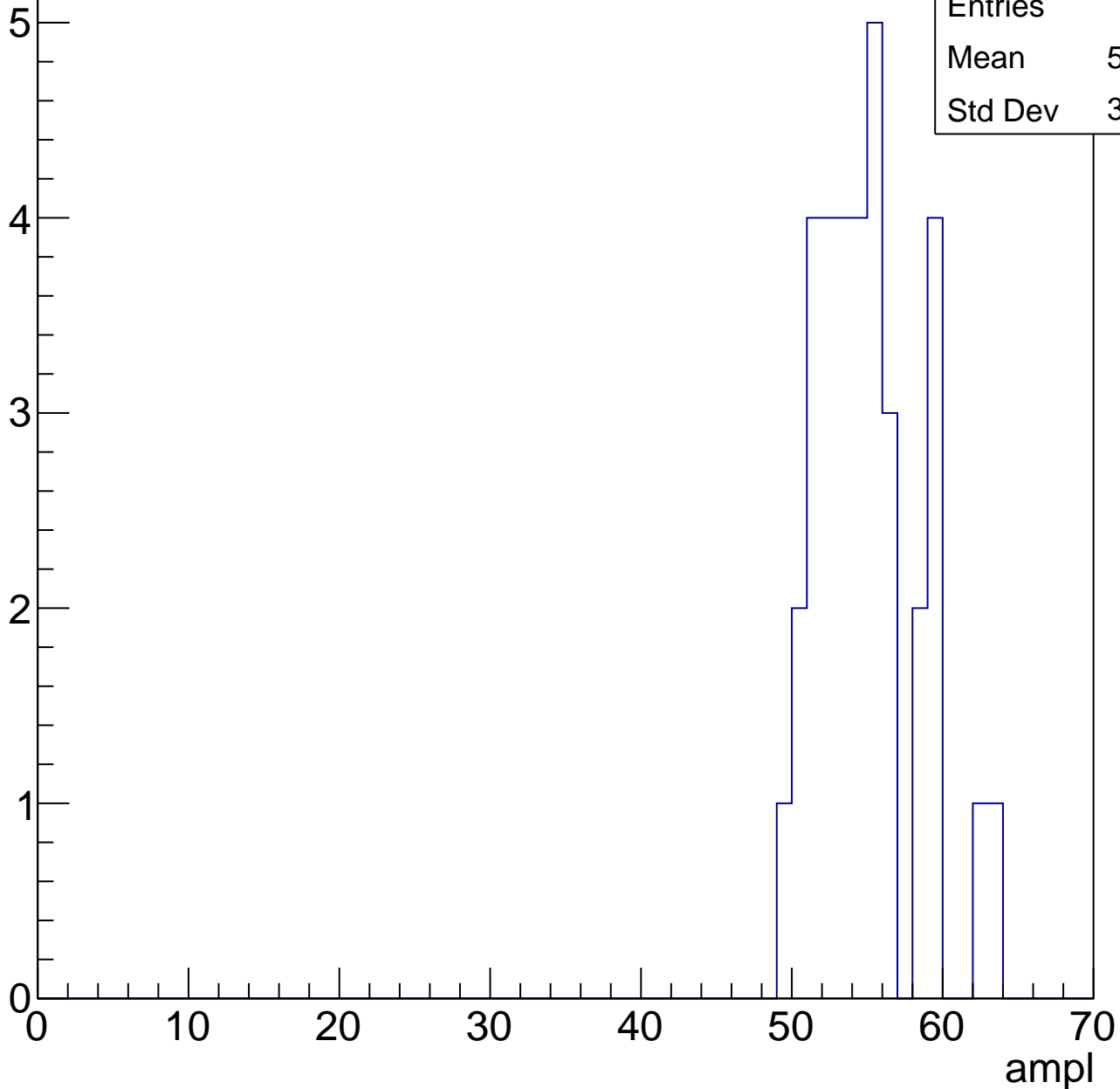


B1L103S, U14-ch127, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	35
Mean	54.54
Std Dev	3.367



B1L103S, U14-ch127, adc5

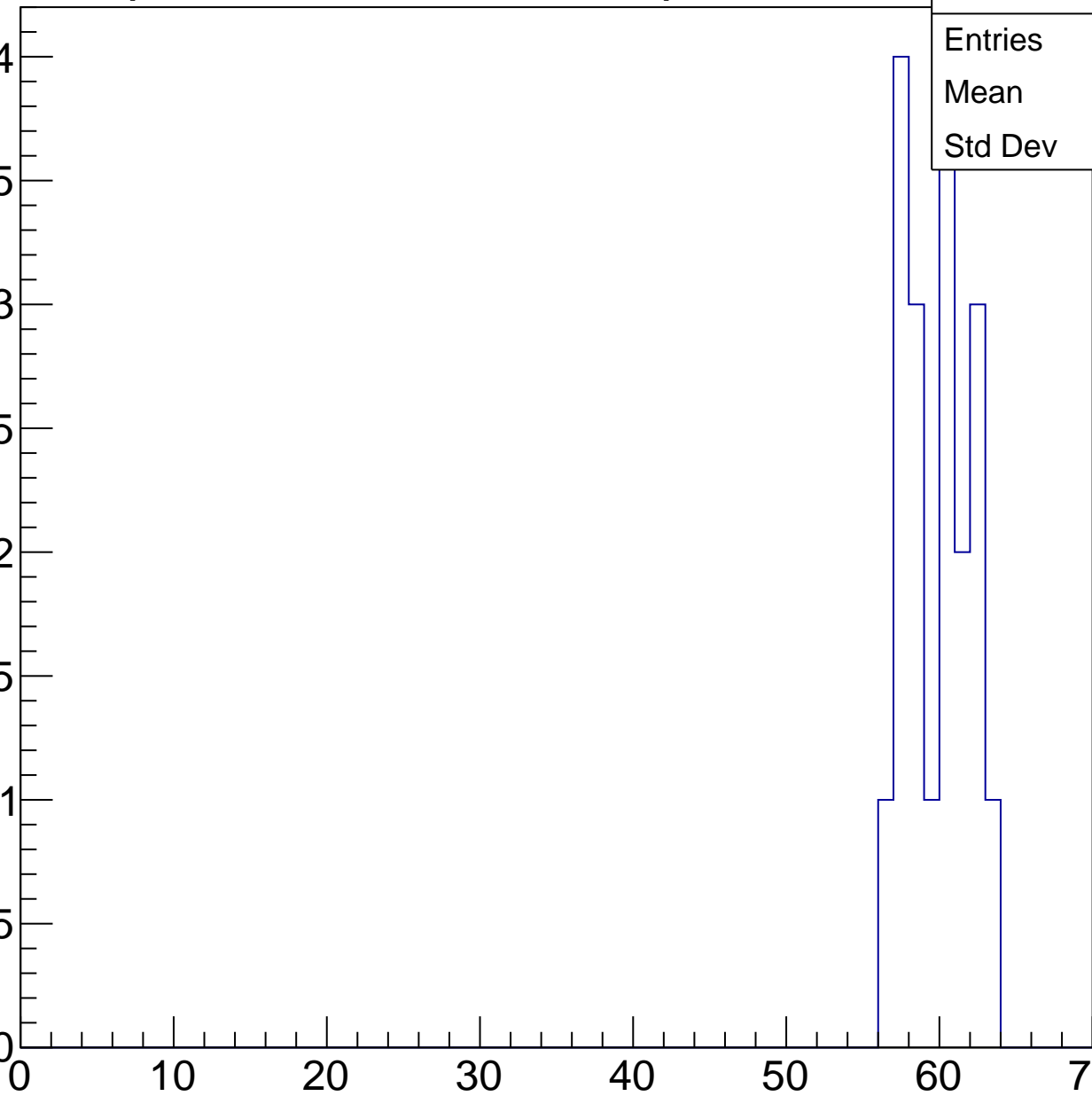
calib_packv5_041523_1651.root, FC#0, port C2

Entry

4
3.5
3
2.5
2
1.5
1
0.5
0

Entries	19
Mean	59.37
Std Dev	2.057

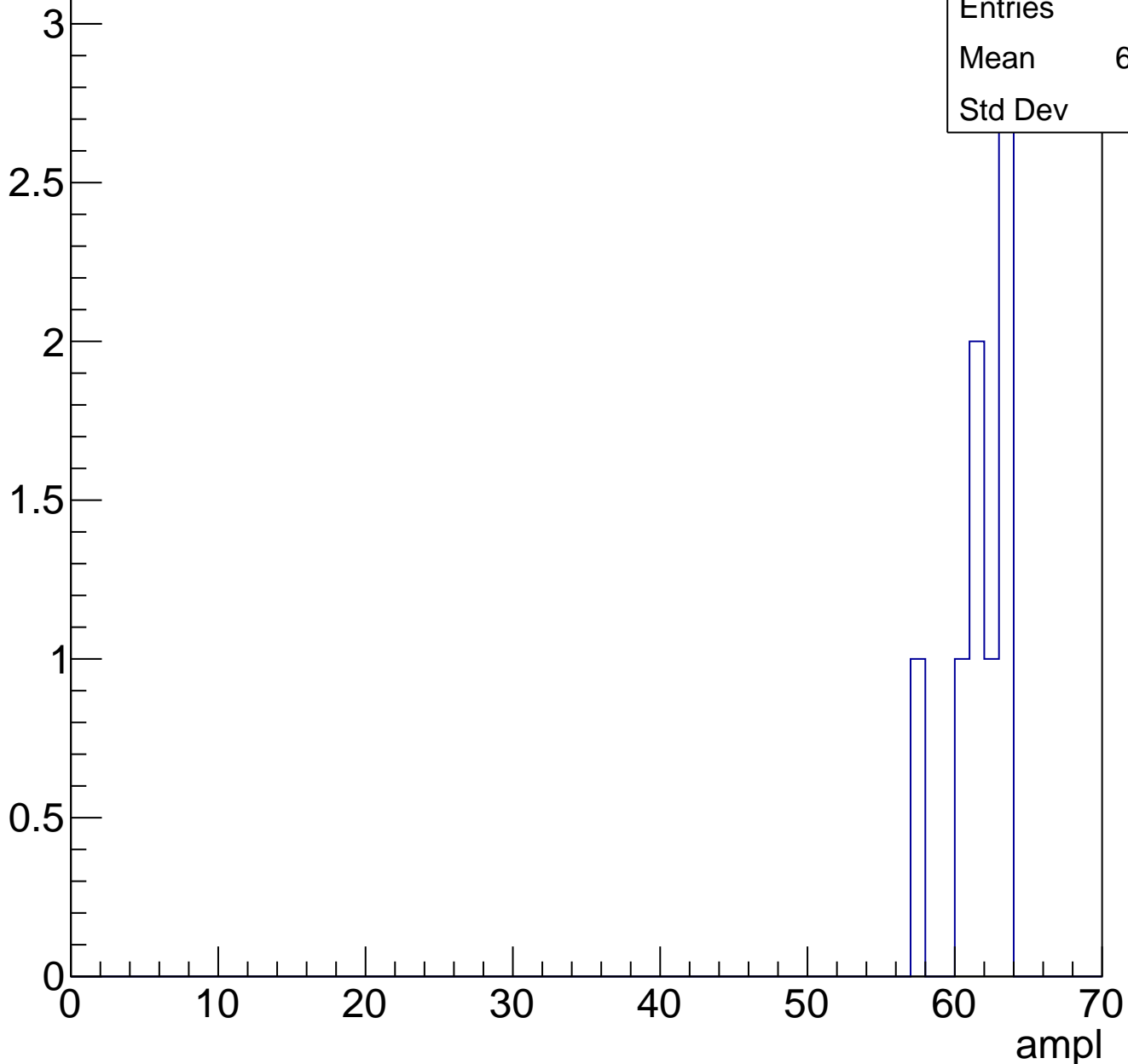
ampl



B1L103S, U14-ch127, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

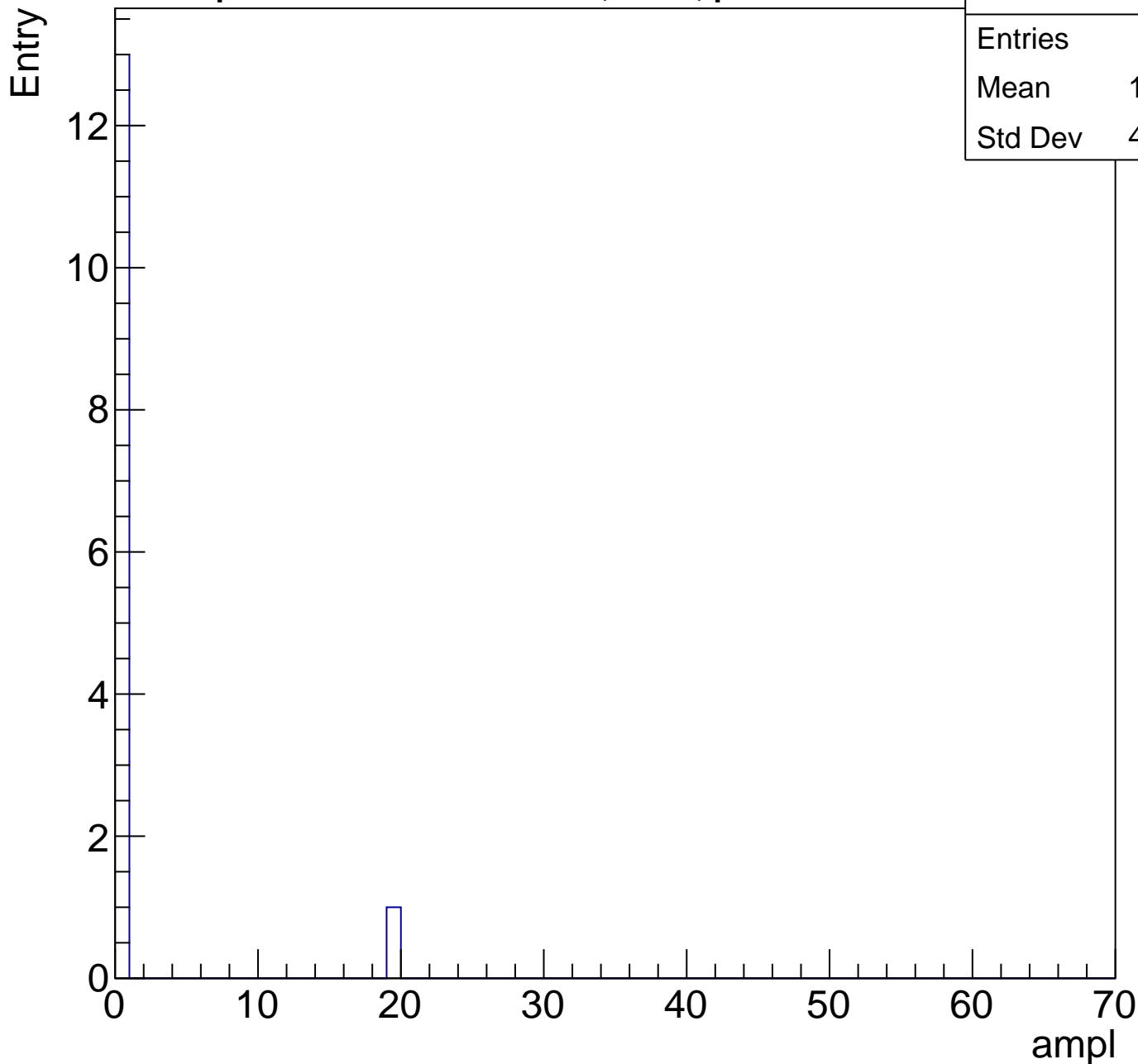


Entries	8
Mean	61.25
Std Dev	1.92

B1L103S, U14-ch127, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	14
Mean	1.357
Std Dev	4.893



B1L103S, U14-ch127, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	14
Mean	1.357
Std Dev	4.893

Entry

