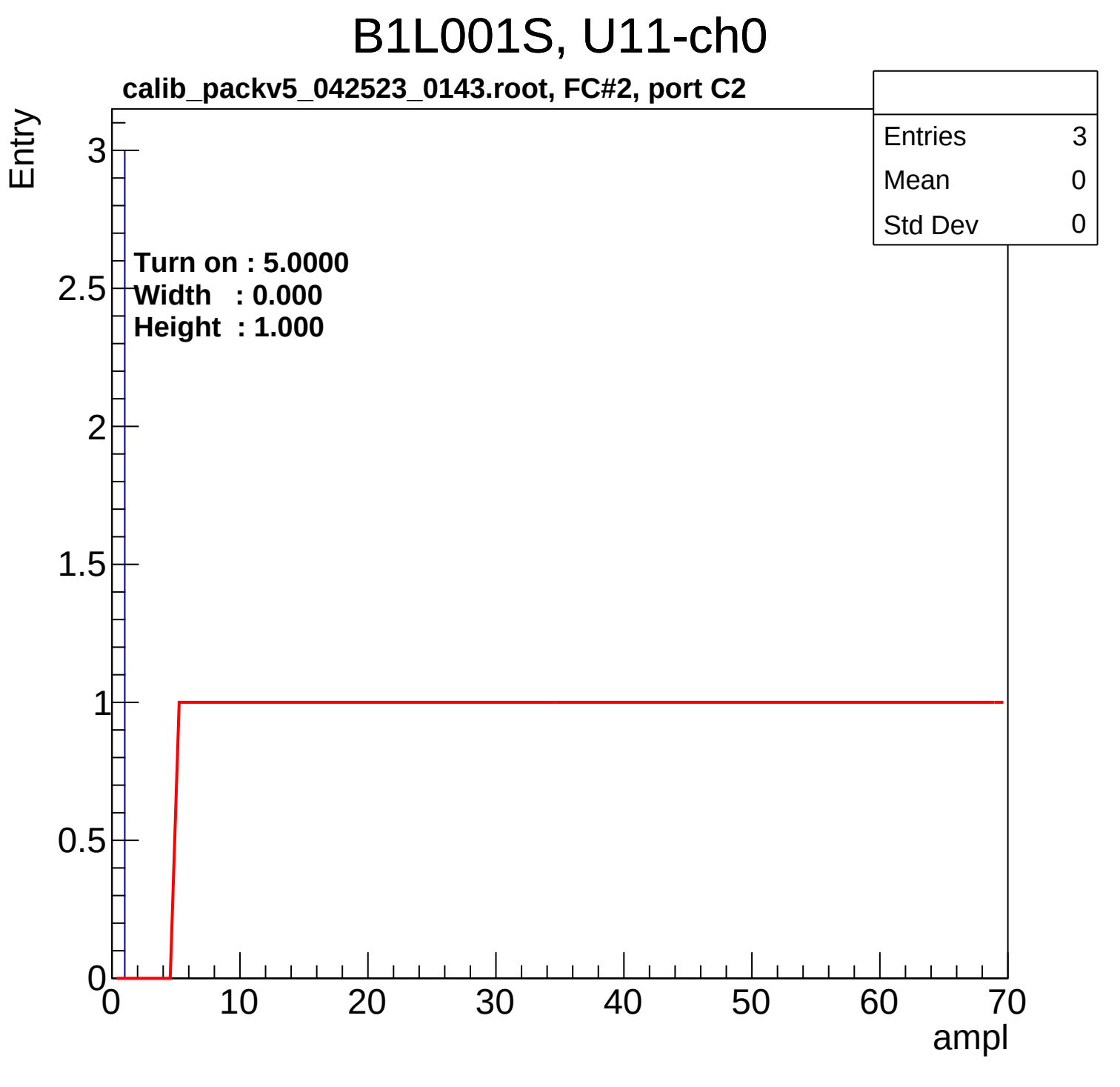
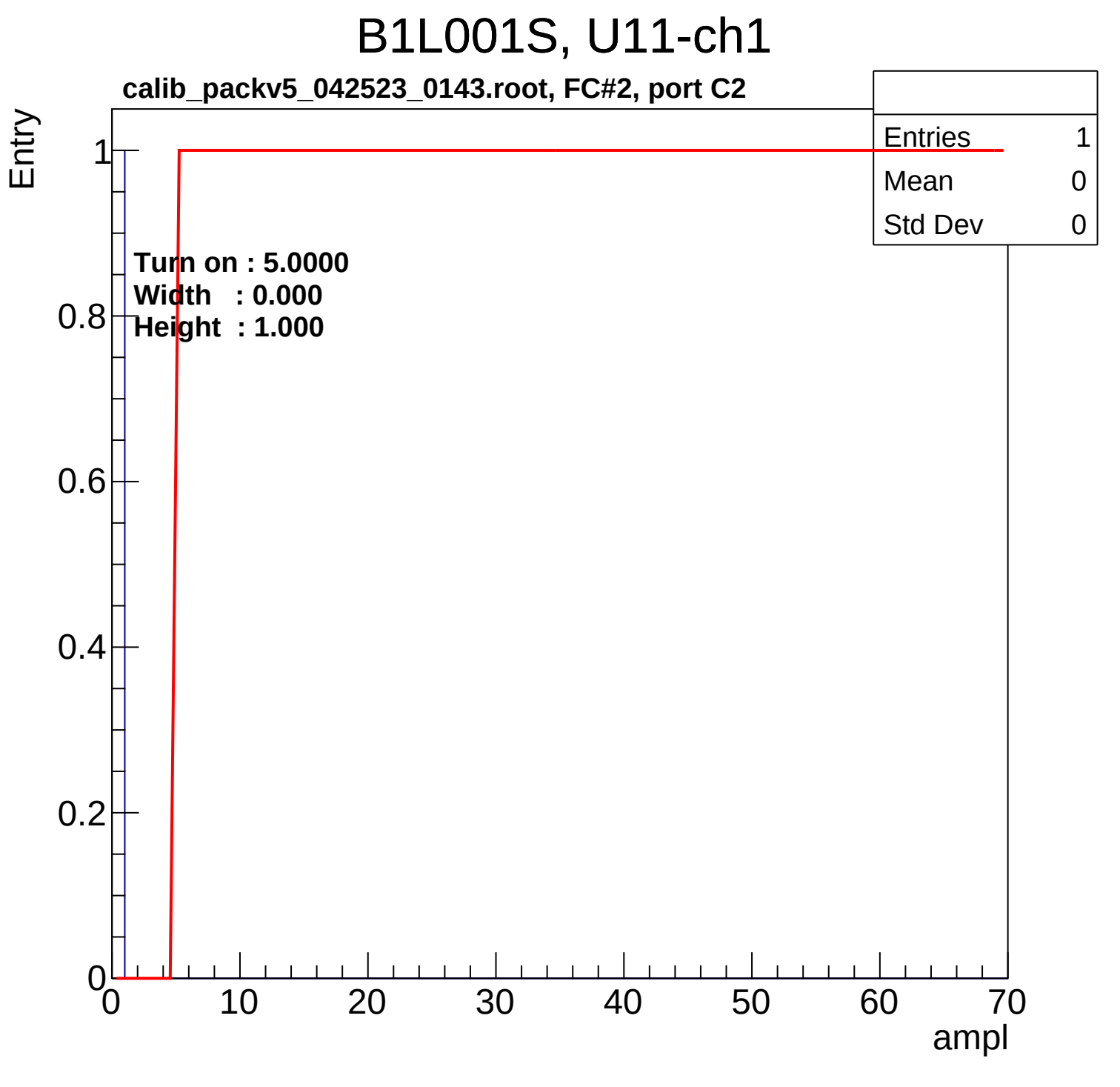
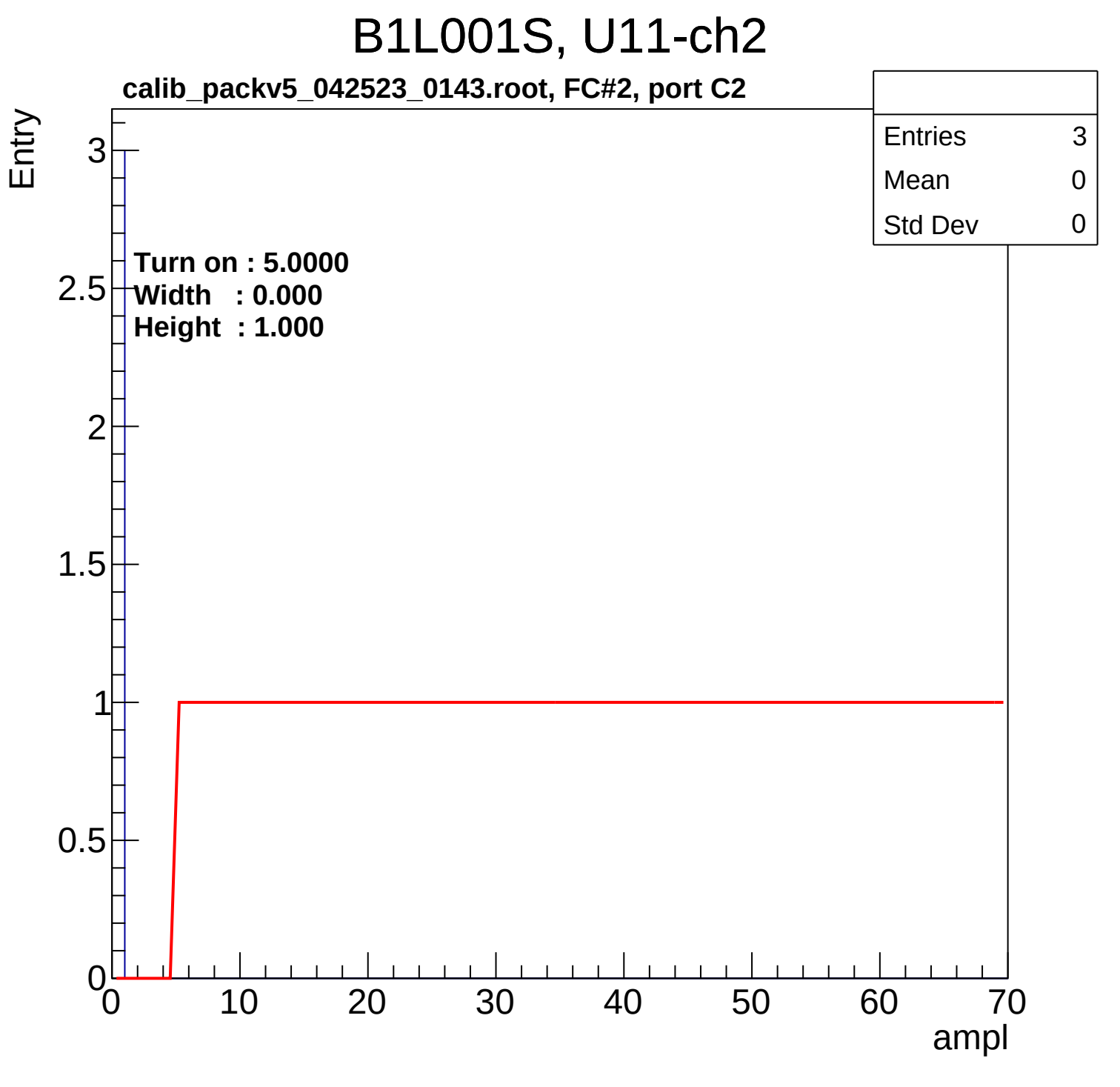
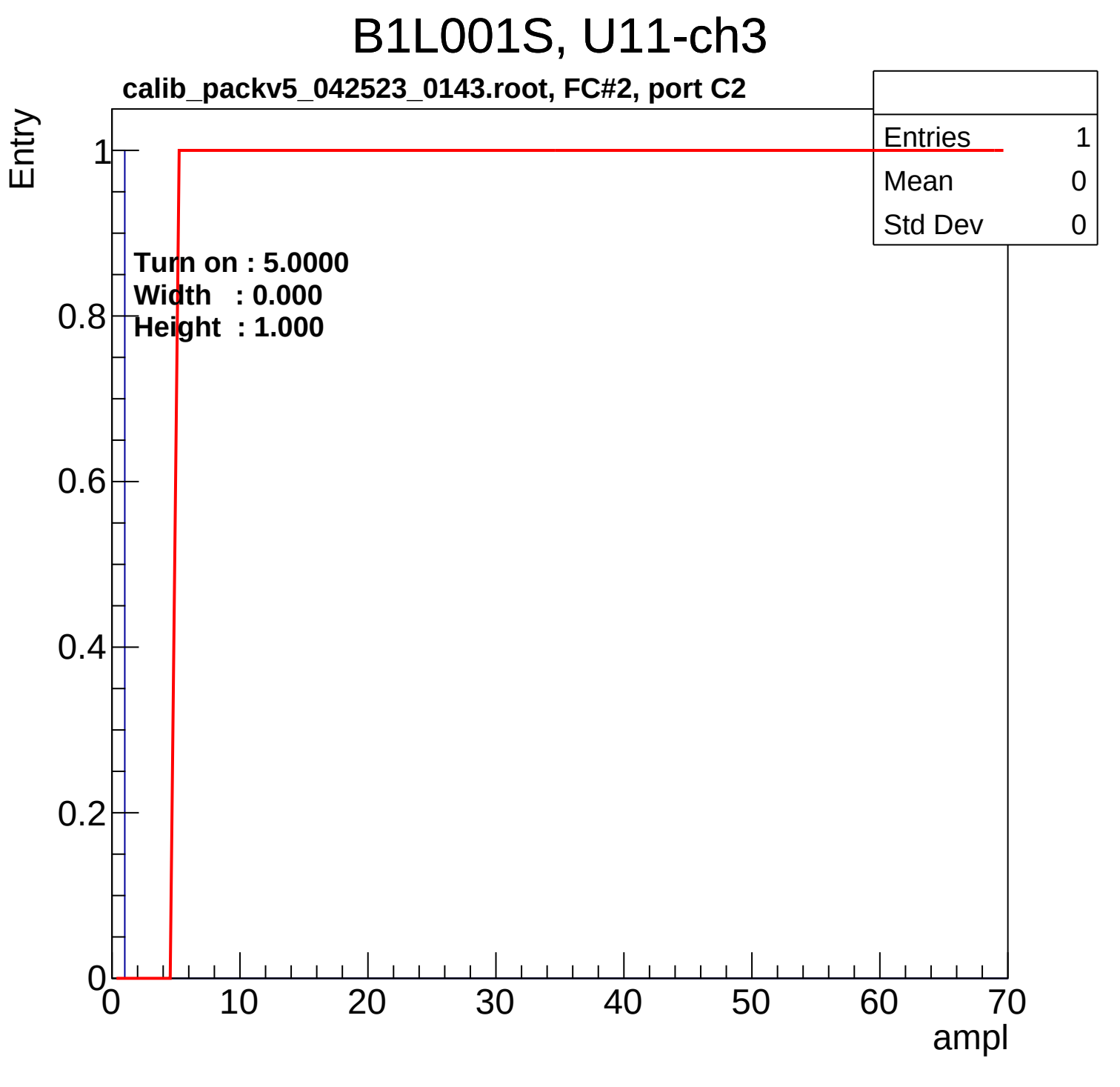
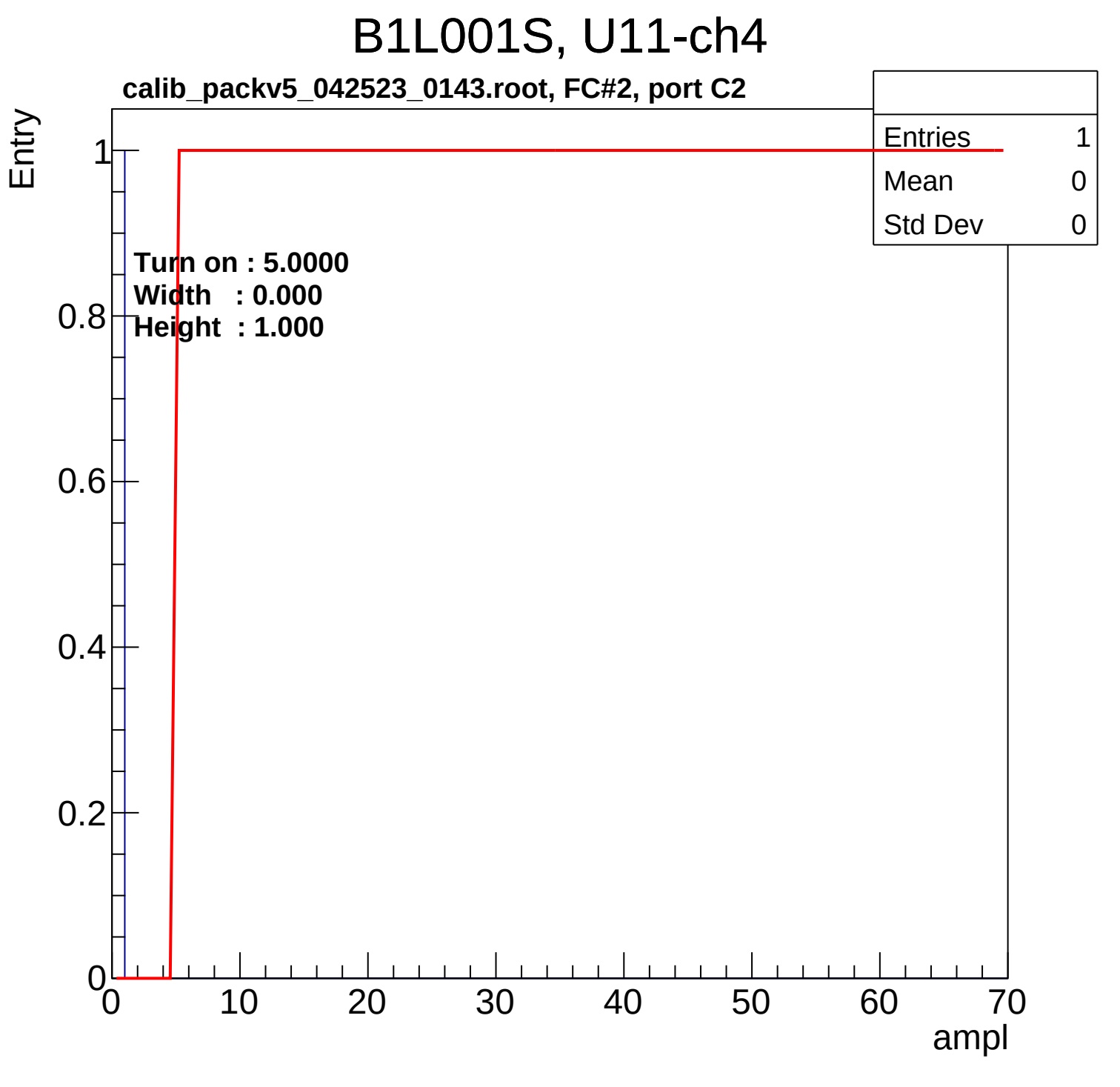
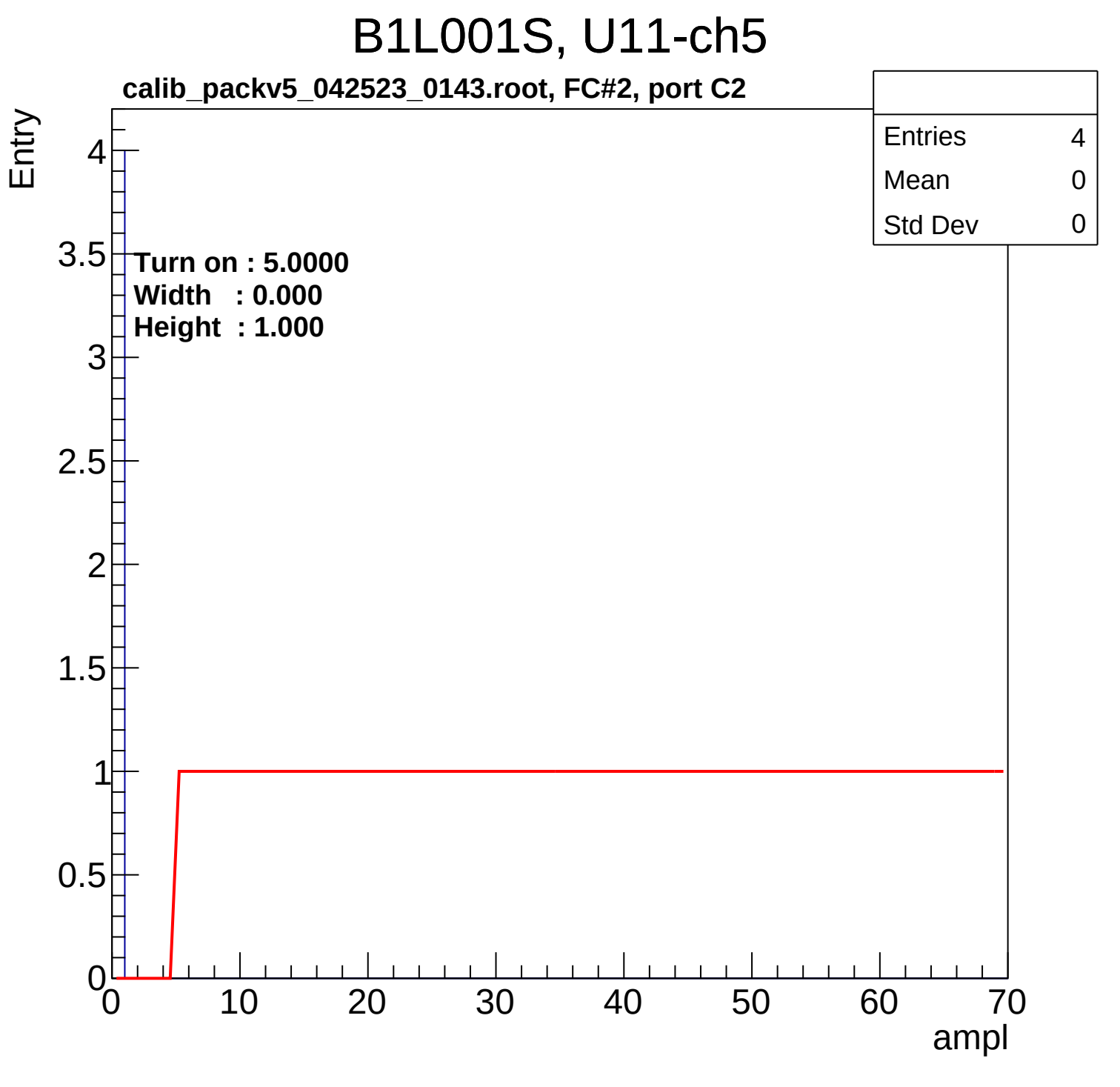

B1L001S, U11-ch0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

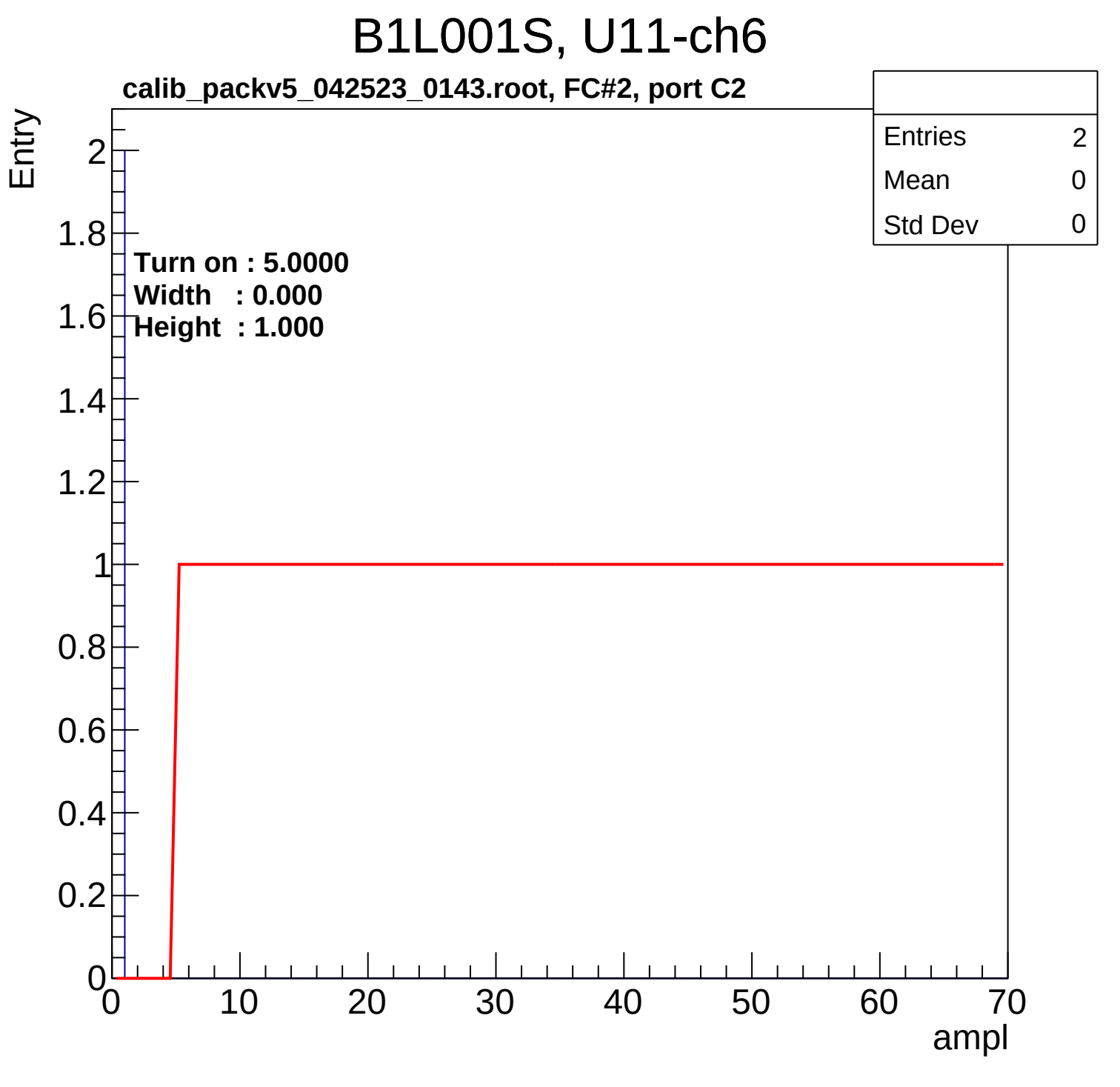

B1L001S, U11-ch1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

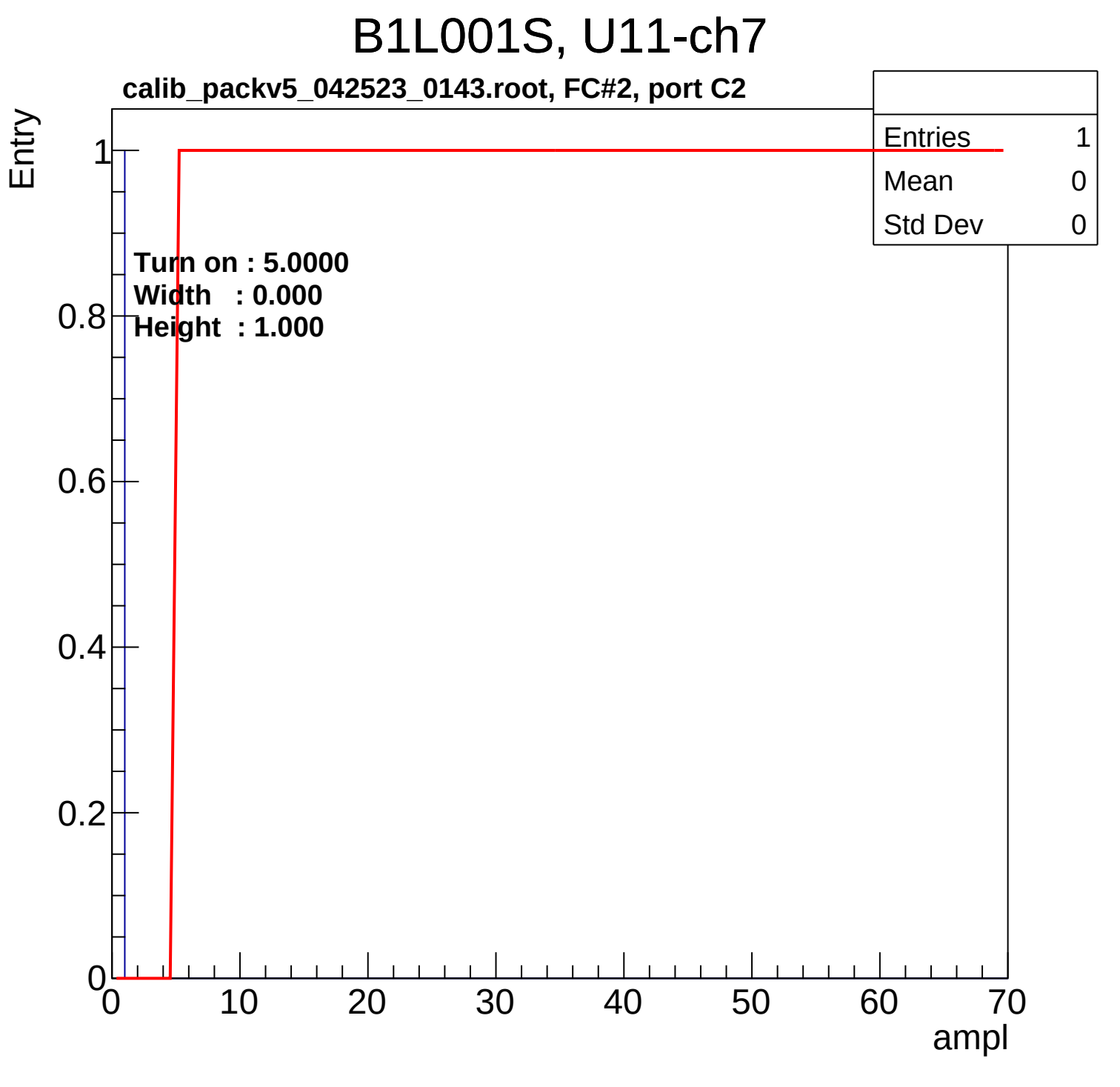

B1L001S, U11-ch2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

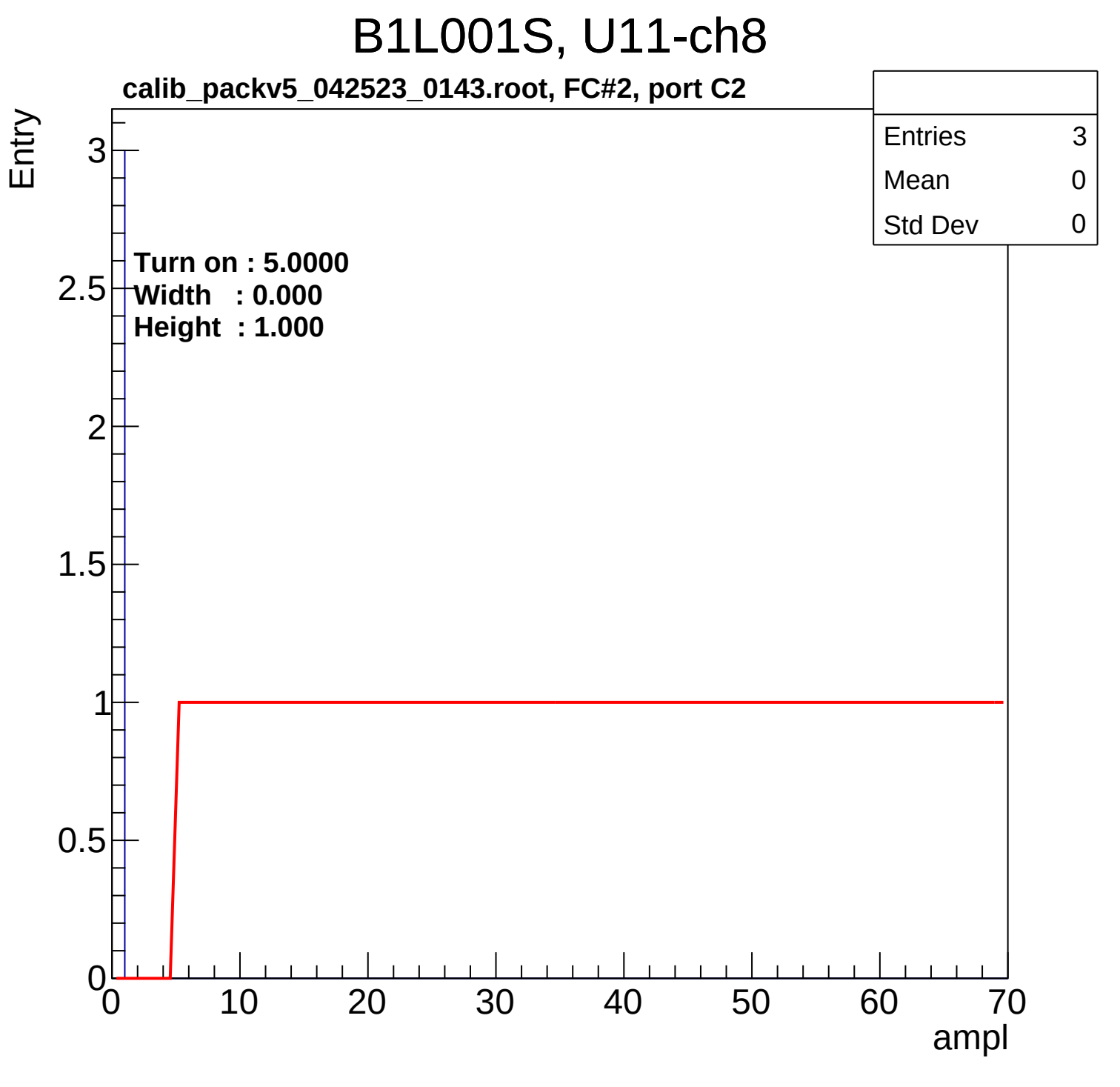

B1L001S, U11-ch3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

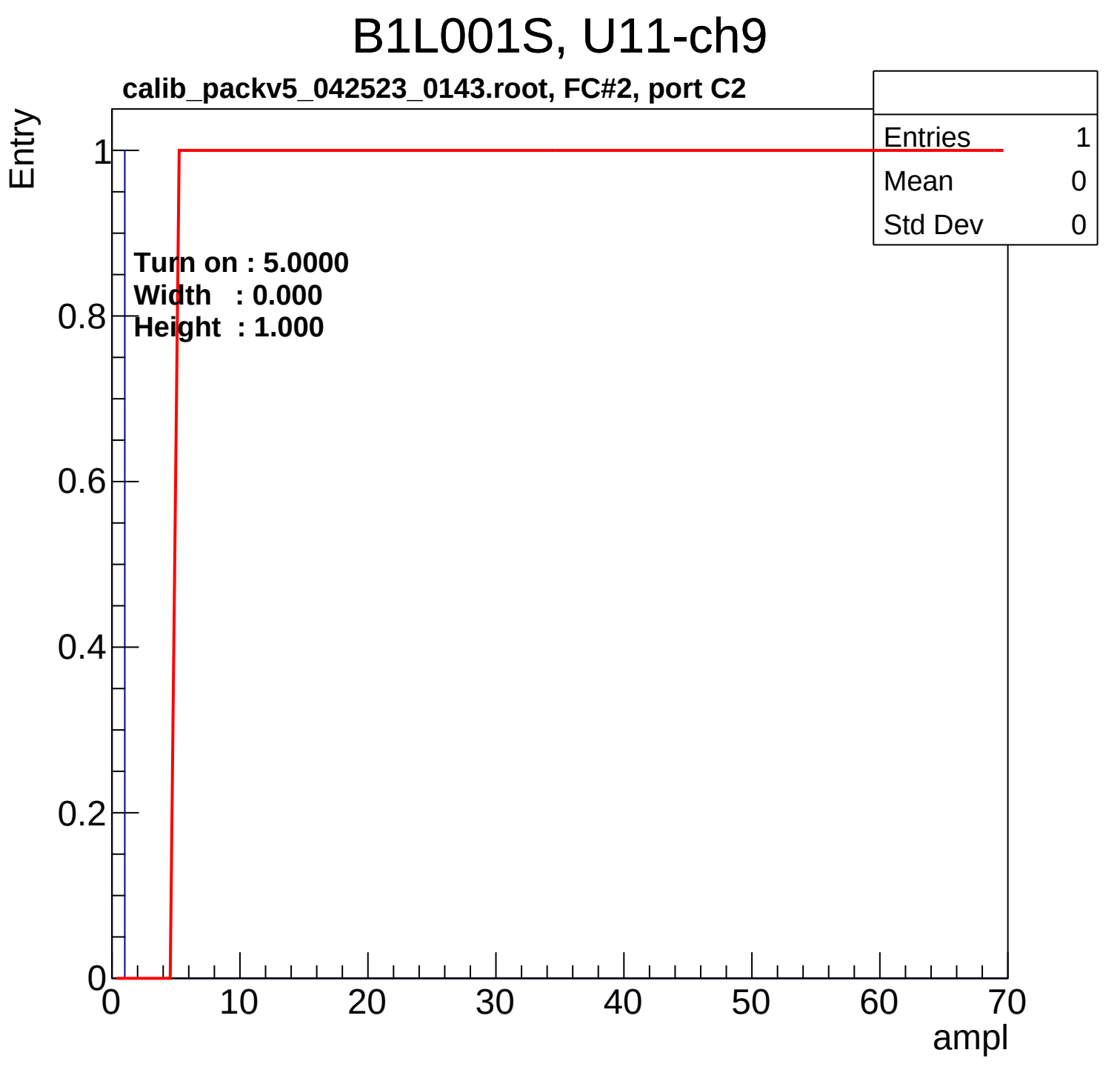

B1L001S, U11-ch4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

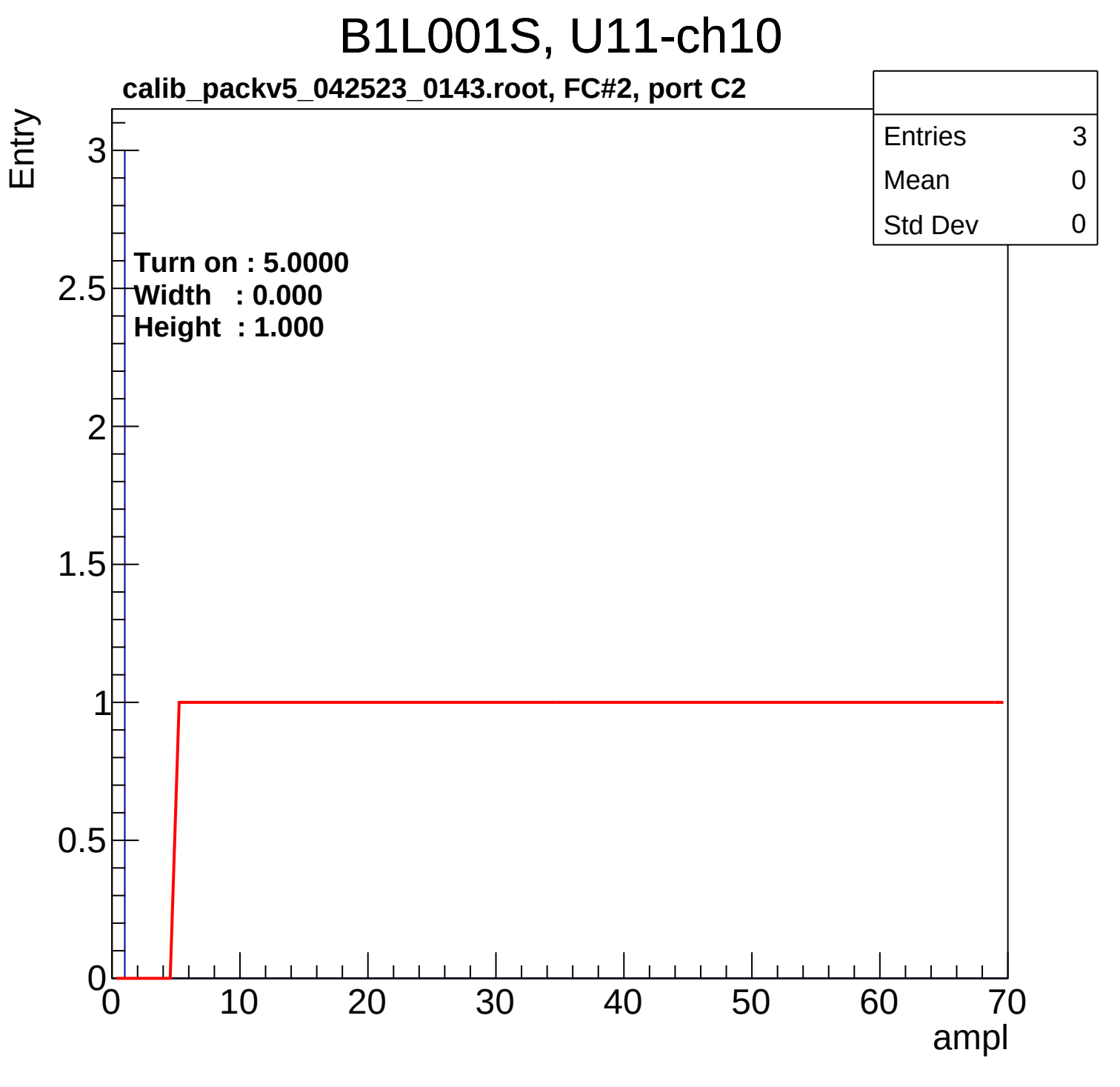

B1L001S, U11-ch5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

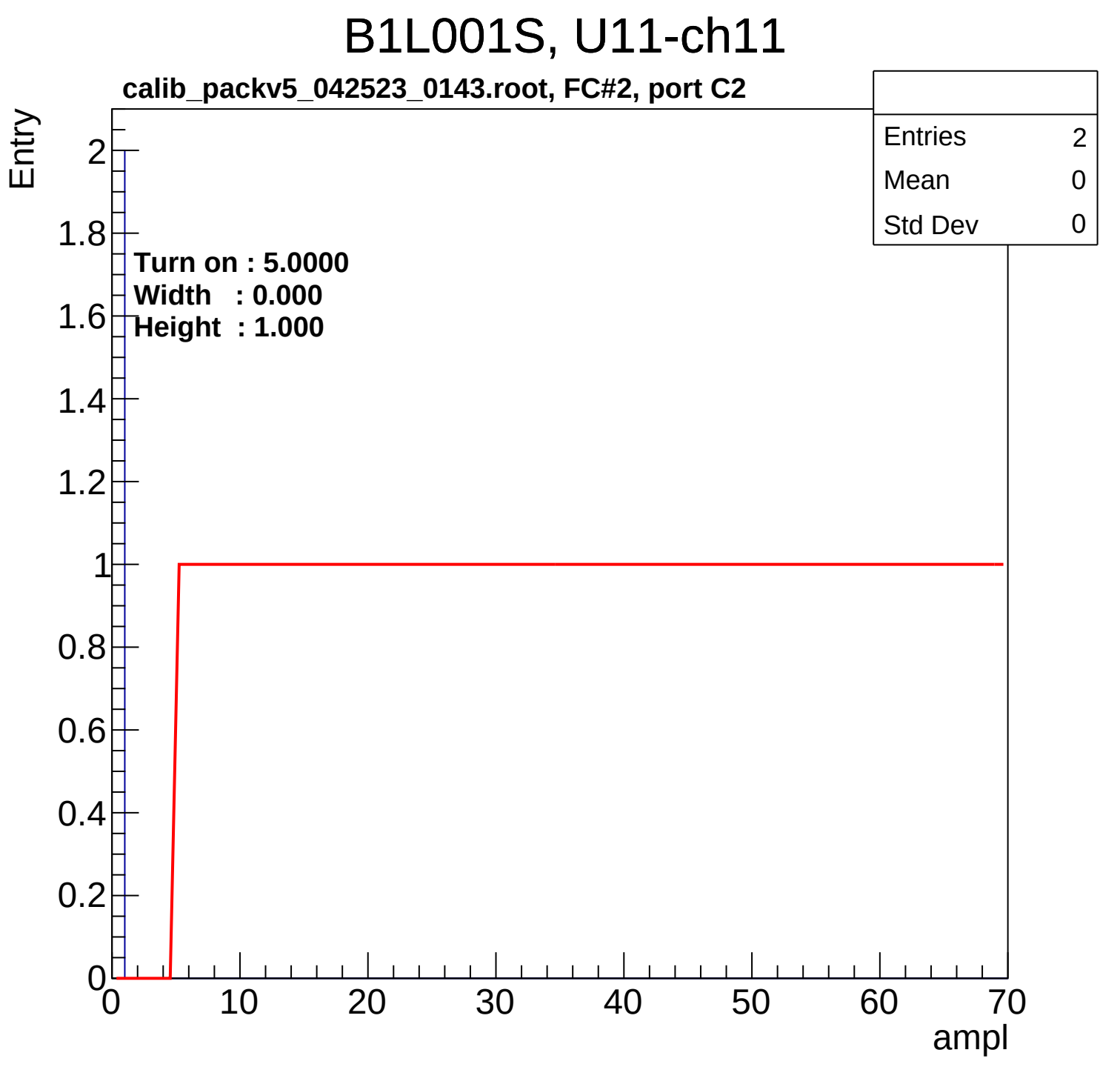

B1L001S, U11-ch6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

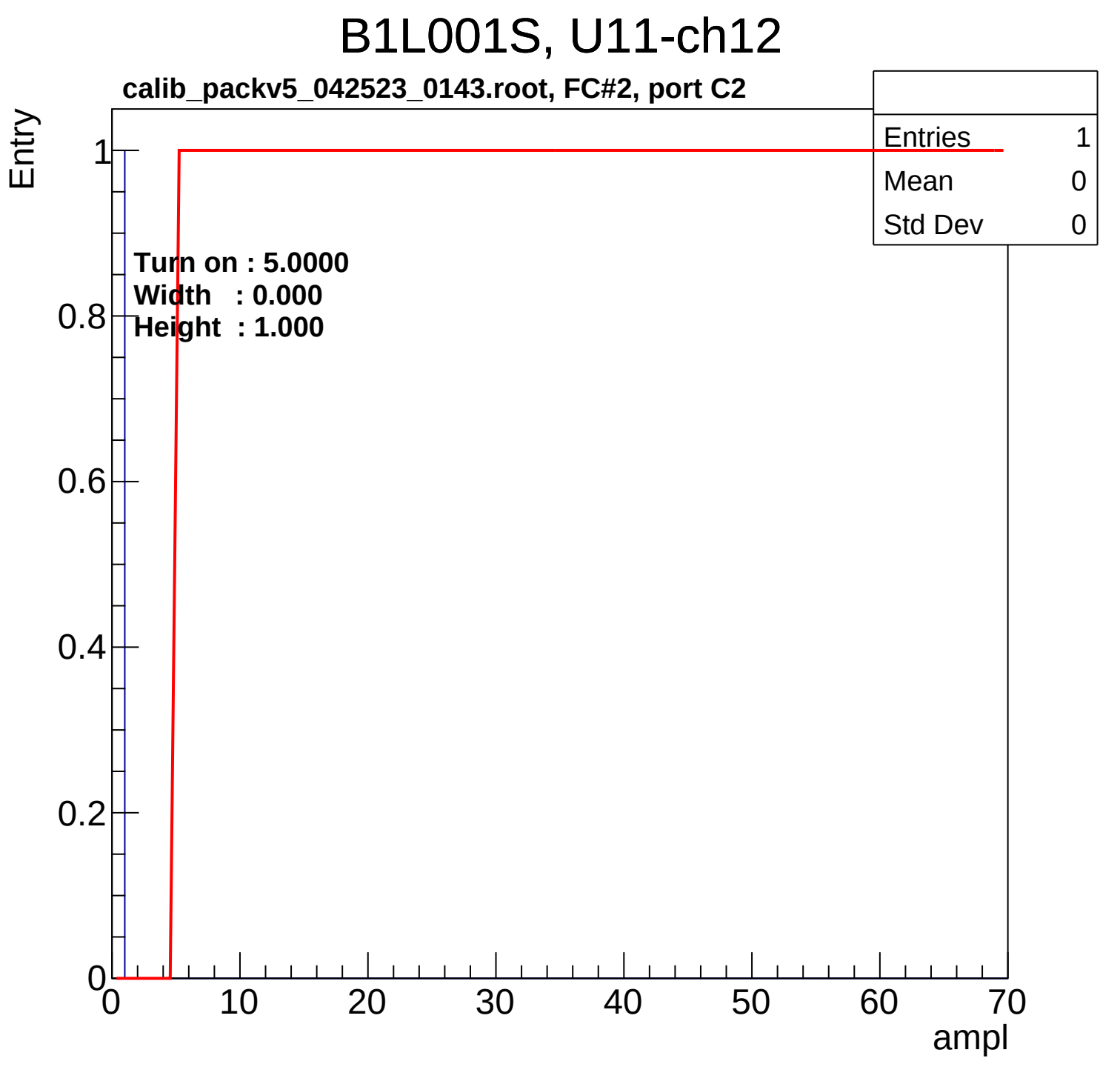

B1L001S, U11-ch7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

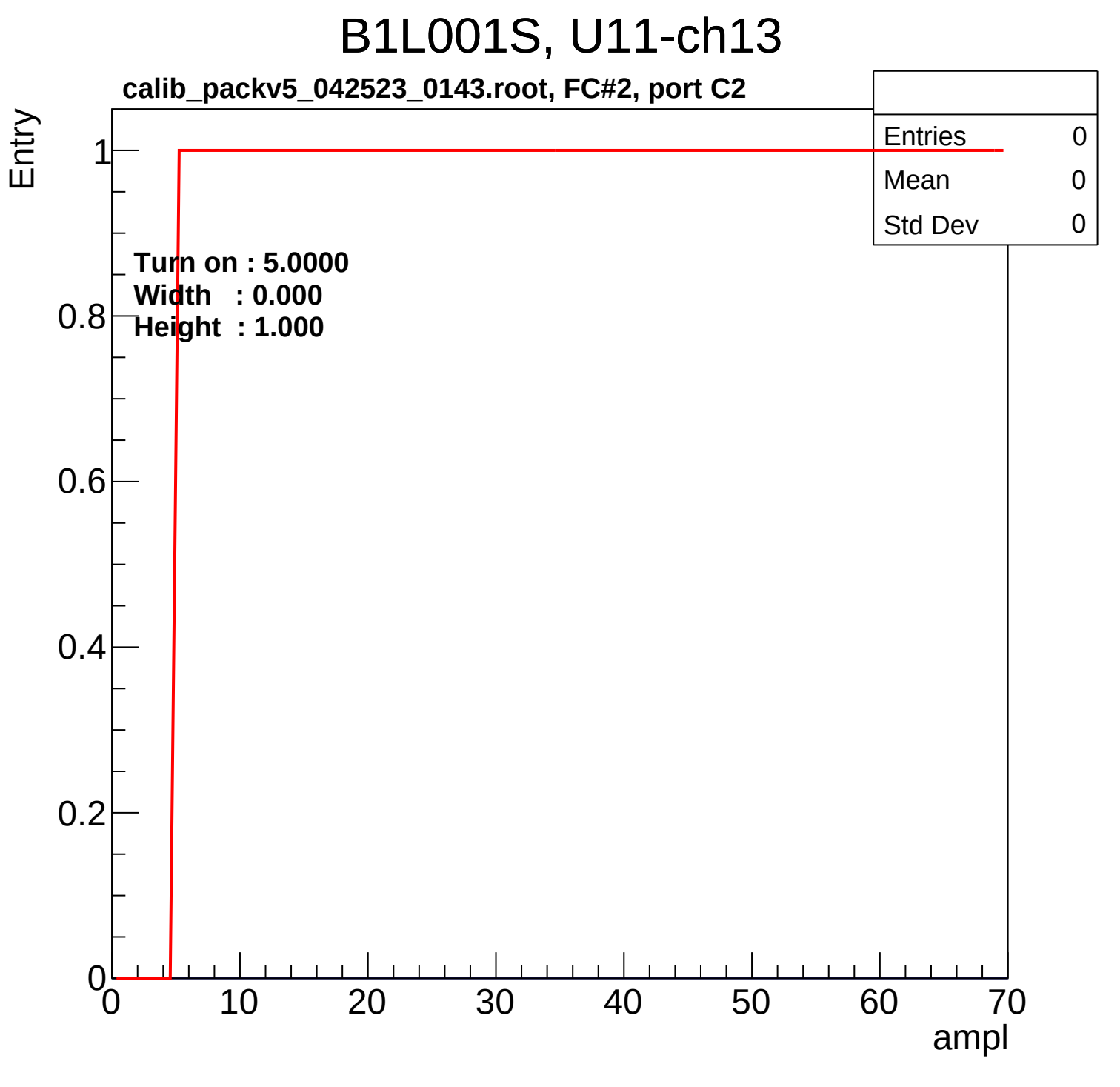

B1L001S, U11-ch8
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

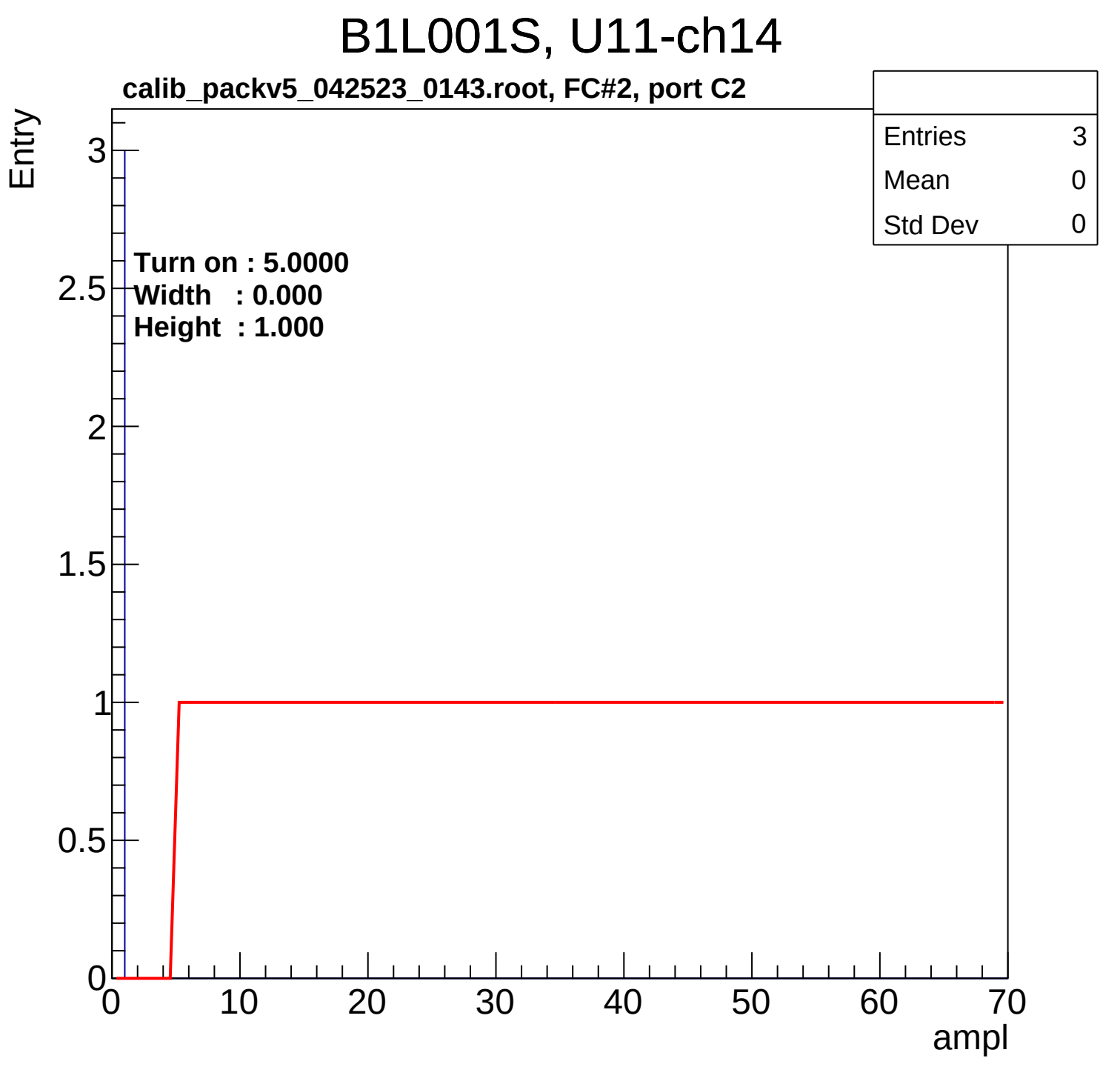

B1L001S, U11-ch9
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

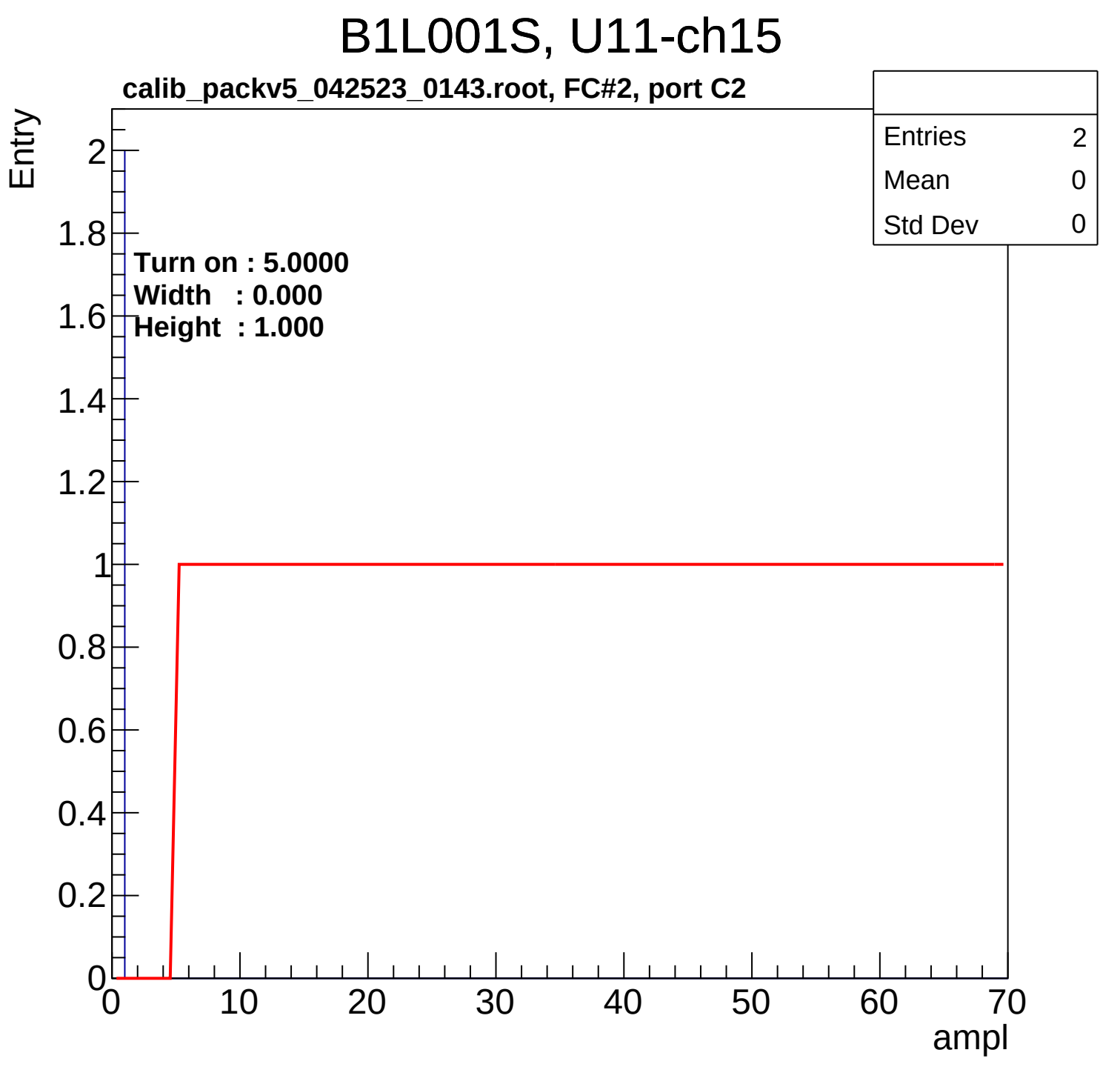

B1L001S, U11-ch10
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

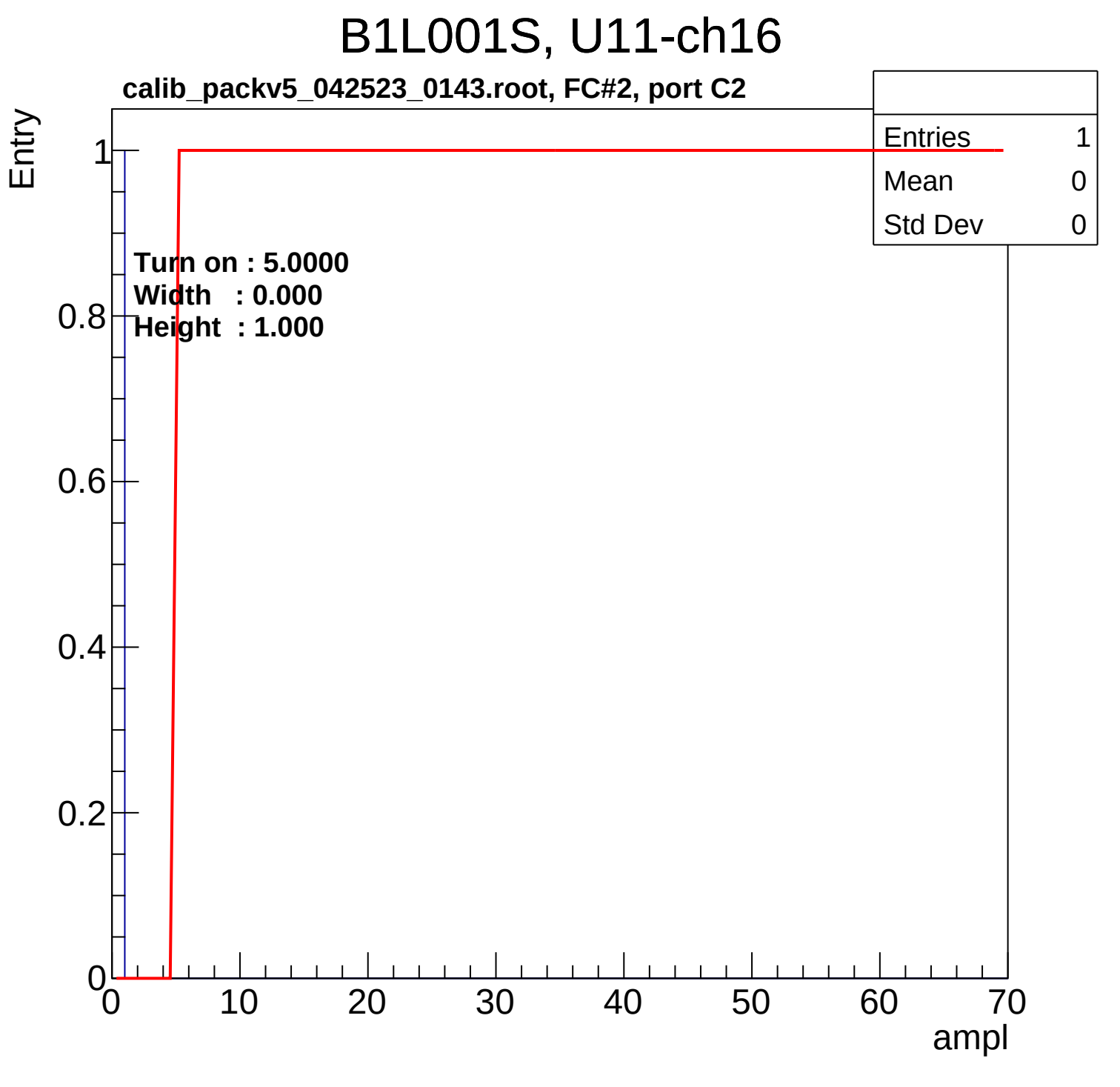

B1L001S, U11-ch11
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

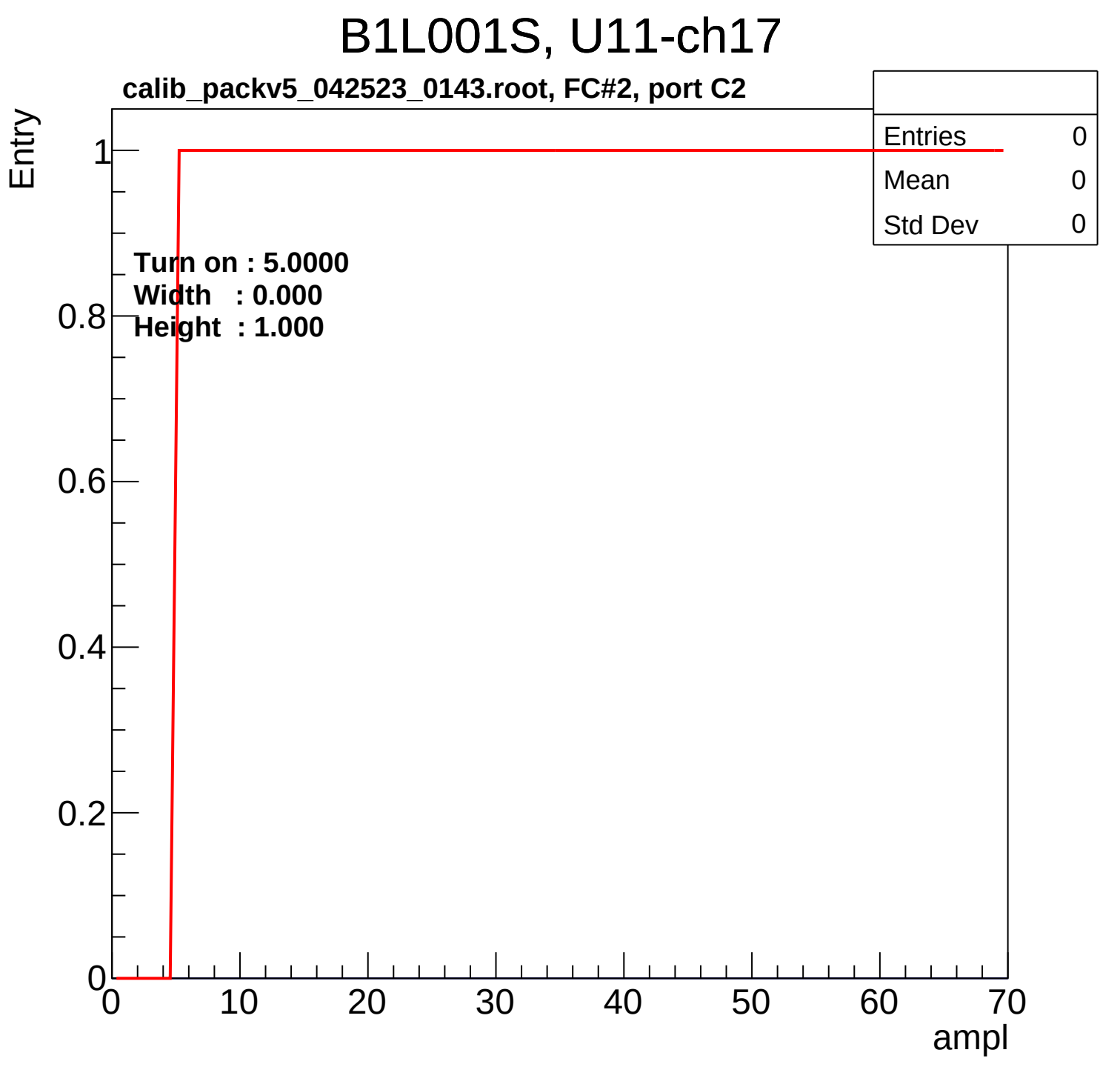

B1L001S, U11-ch12
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

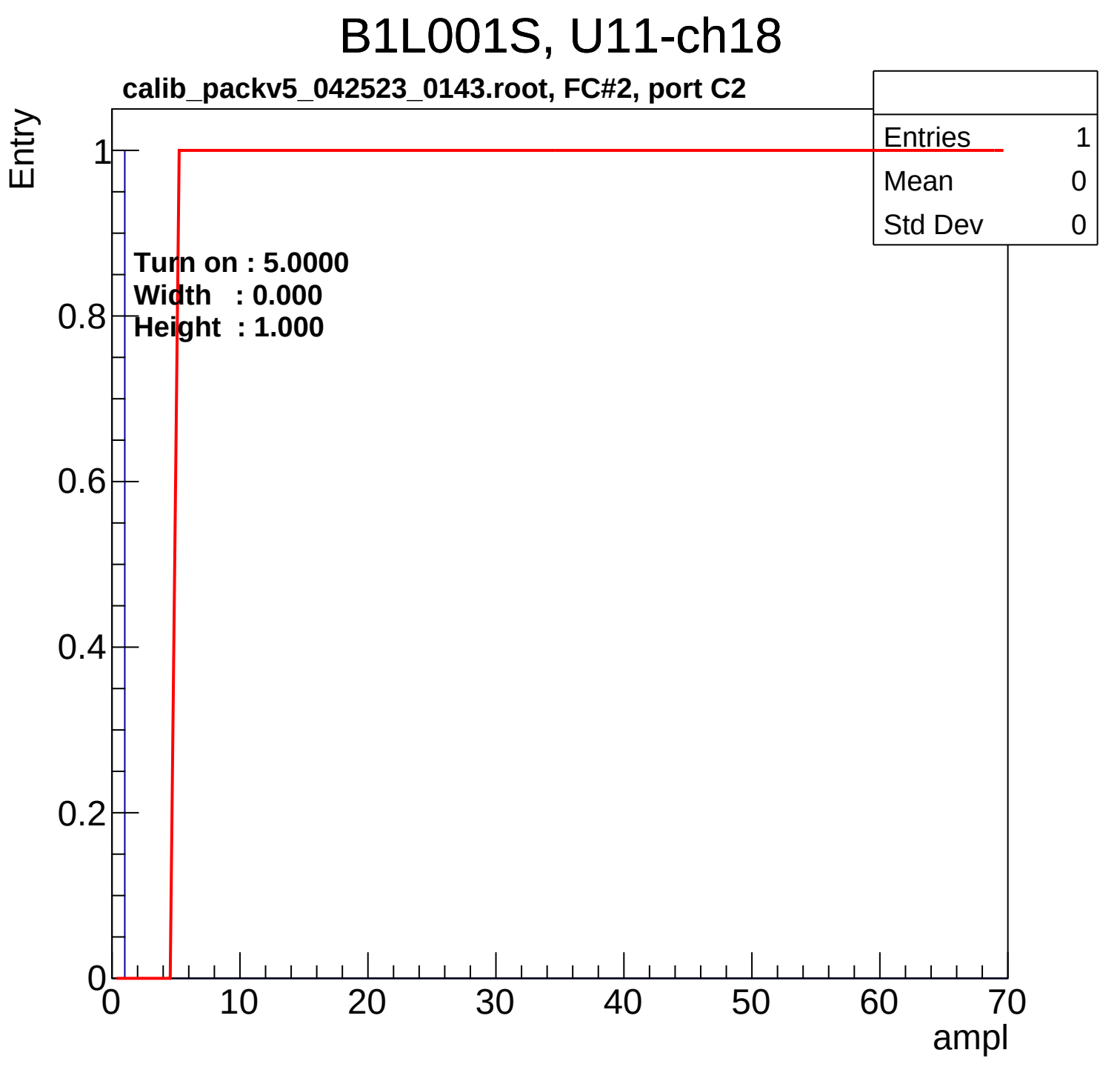

B1L001S, U11-ch13
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

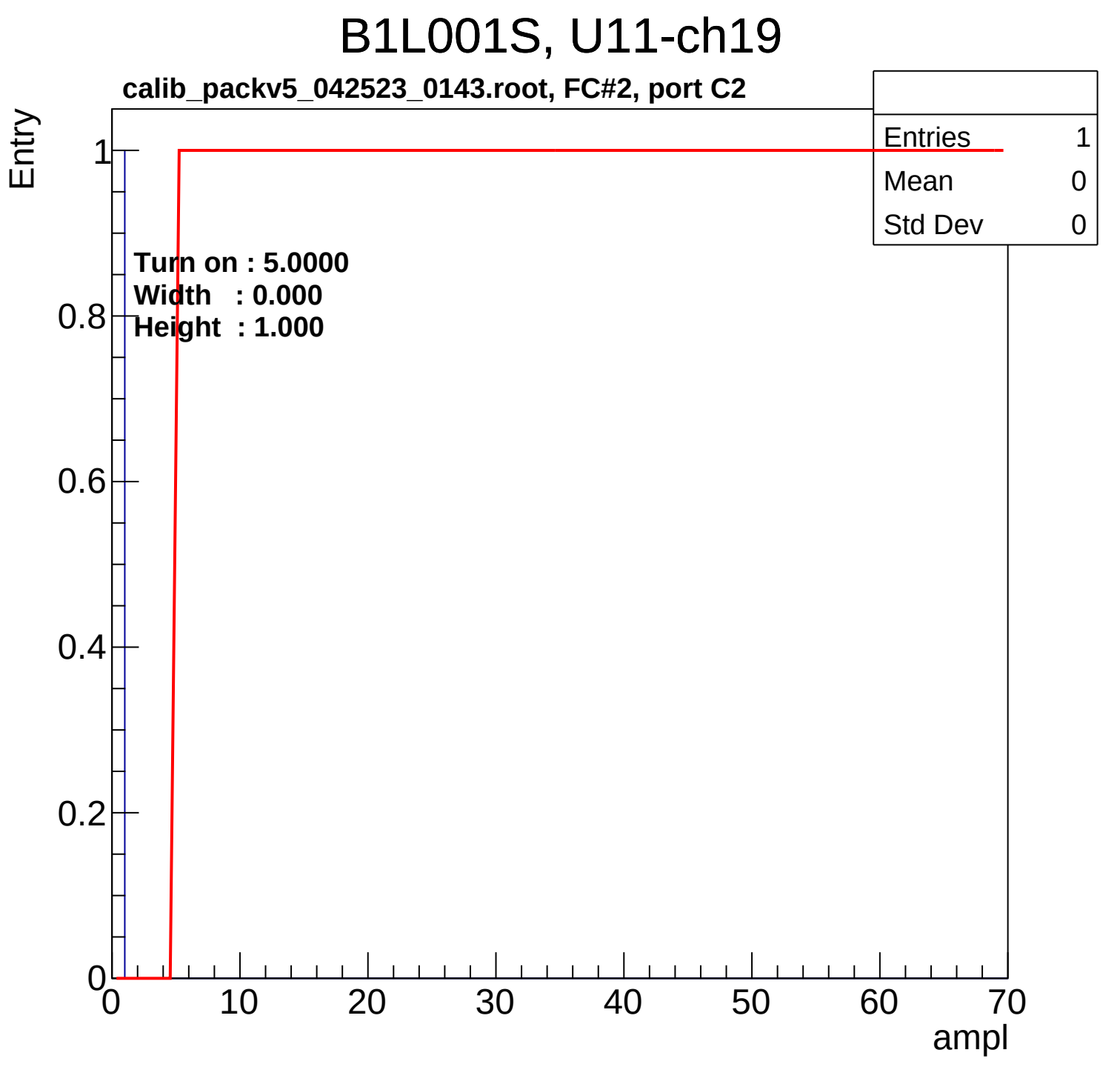

B1L001S, U11-ch14
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

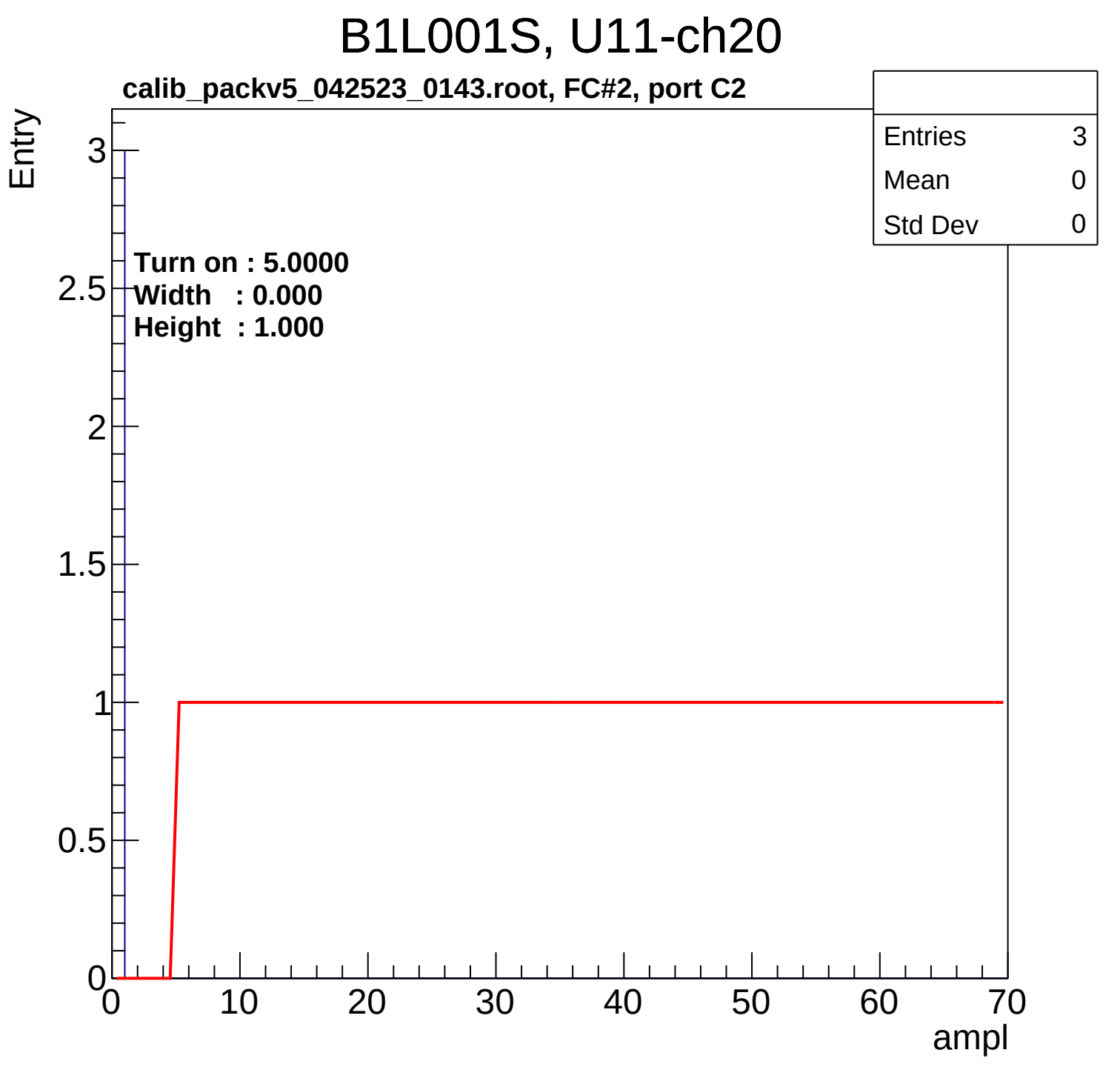

B1L001S, U11-ch15
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

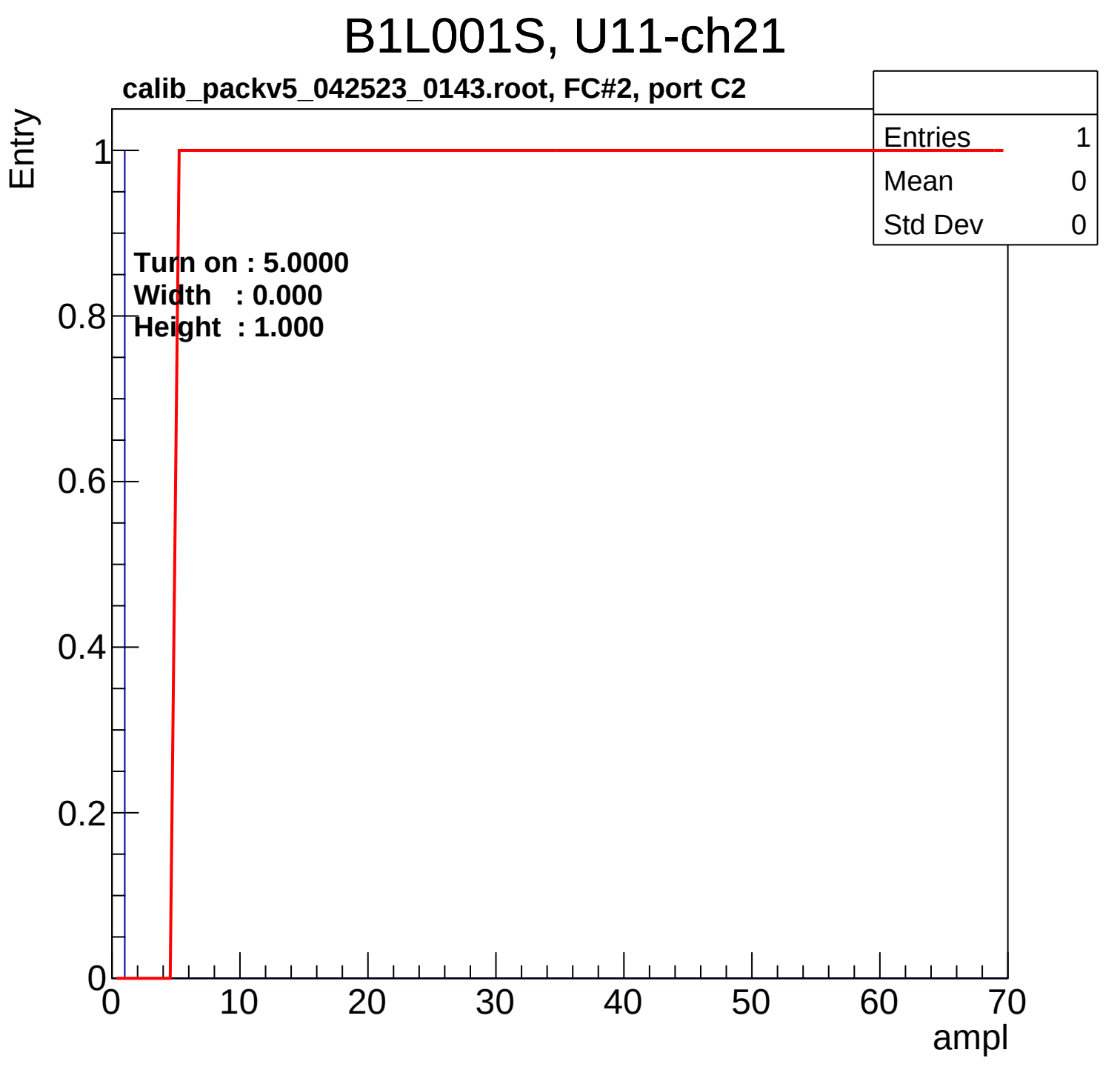

B1L001S, U11-ch16
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

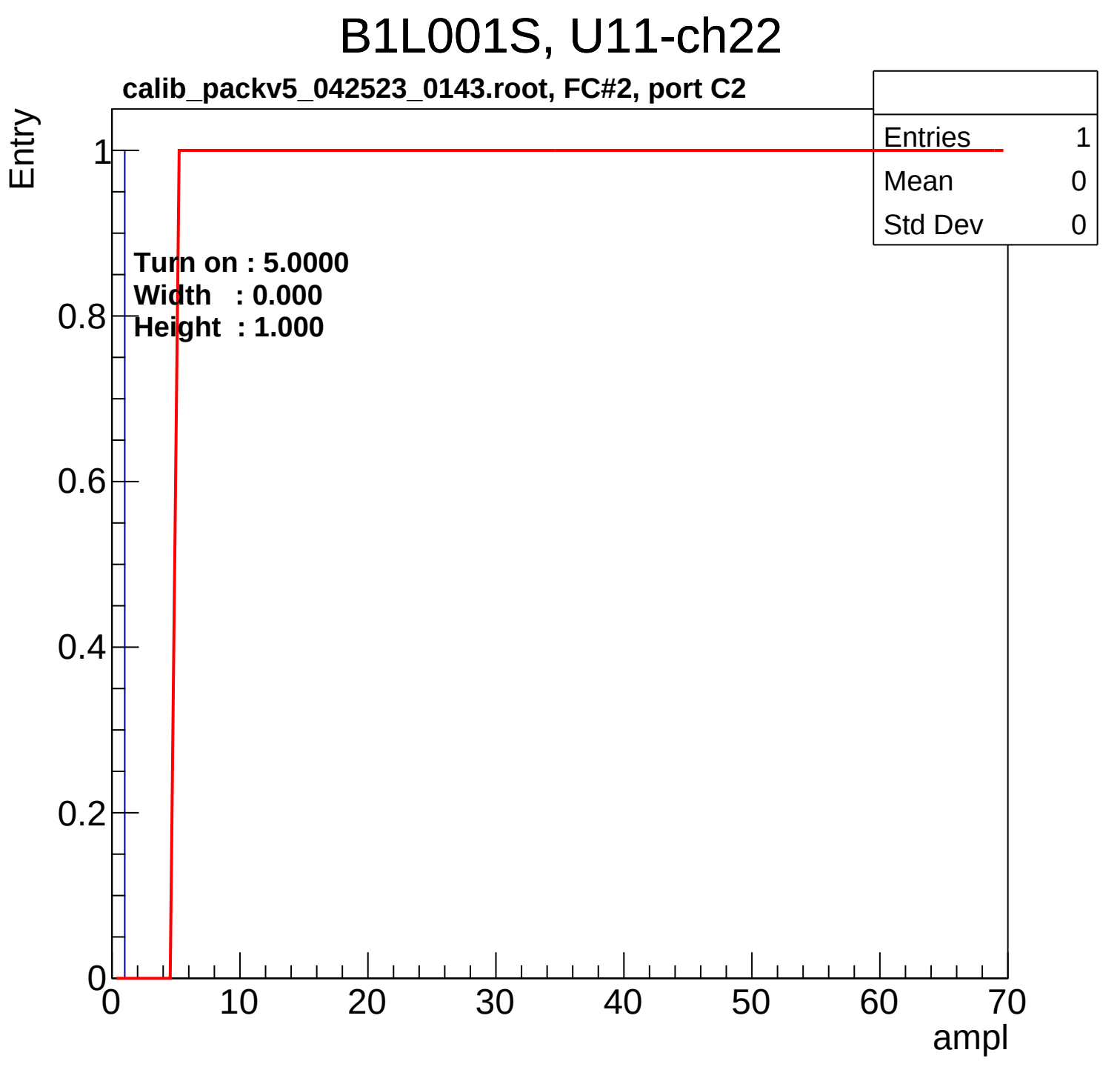

B1L001S, U11-ch17
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

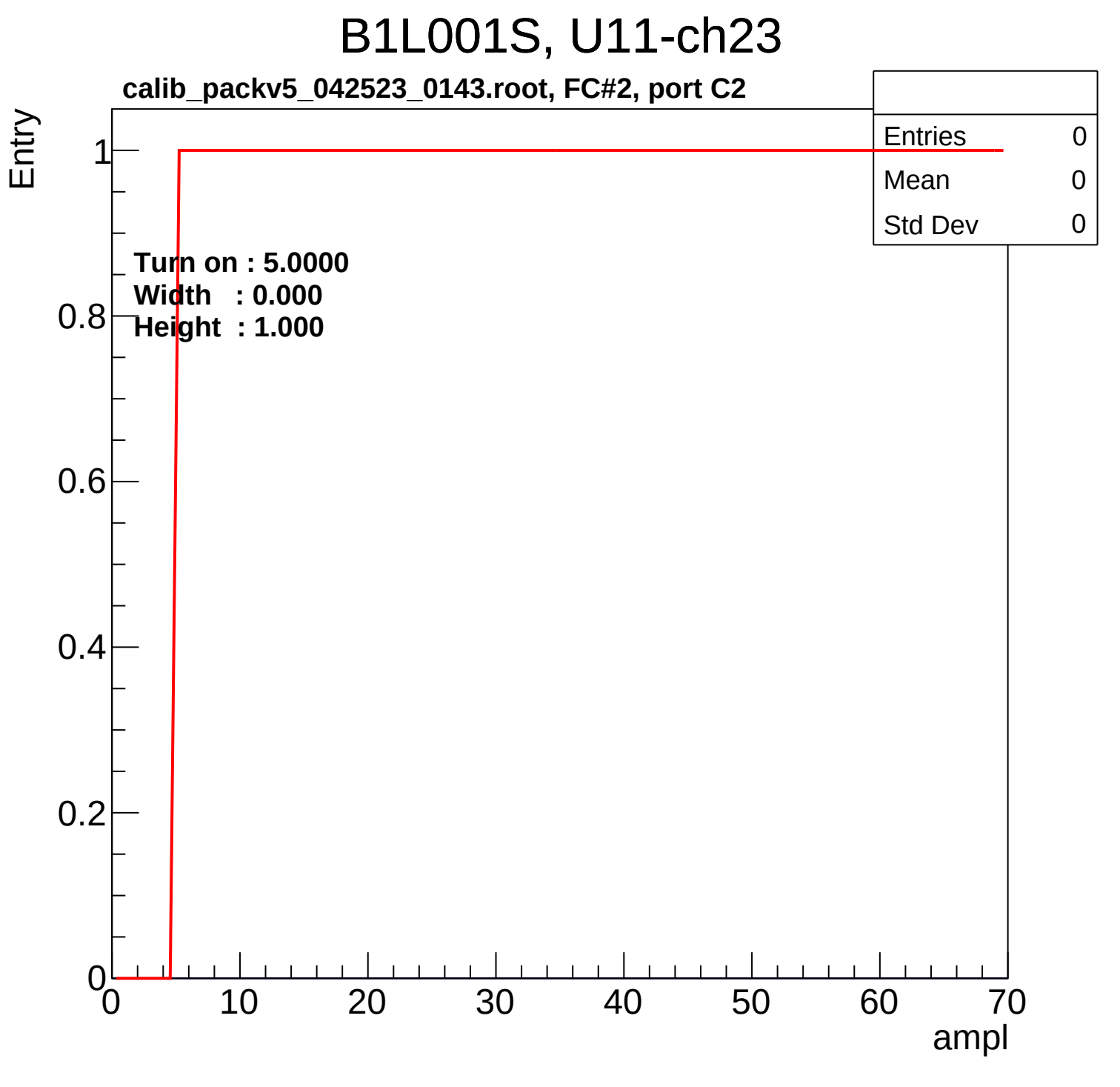

B1L001S, U11-ch18
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

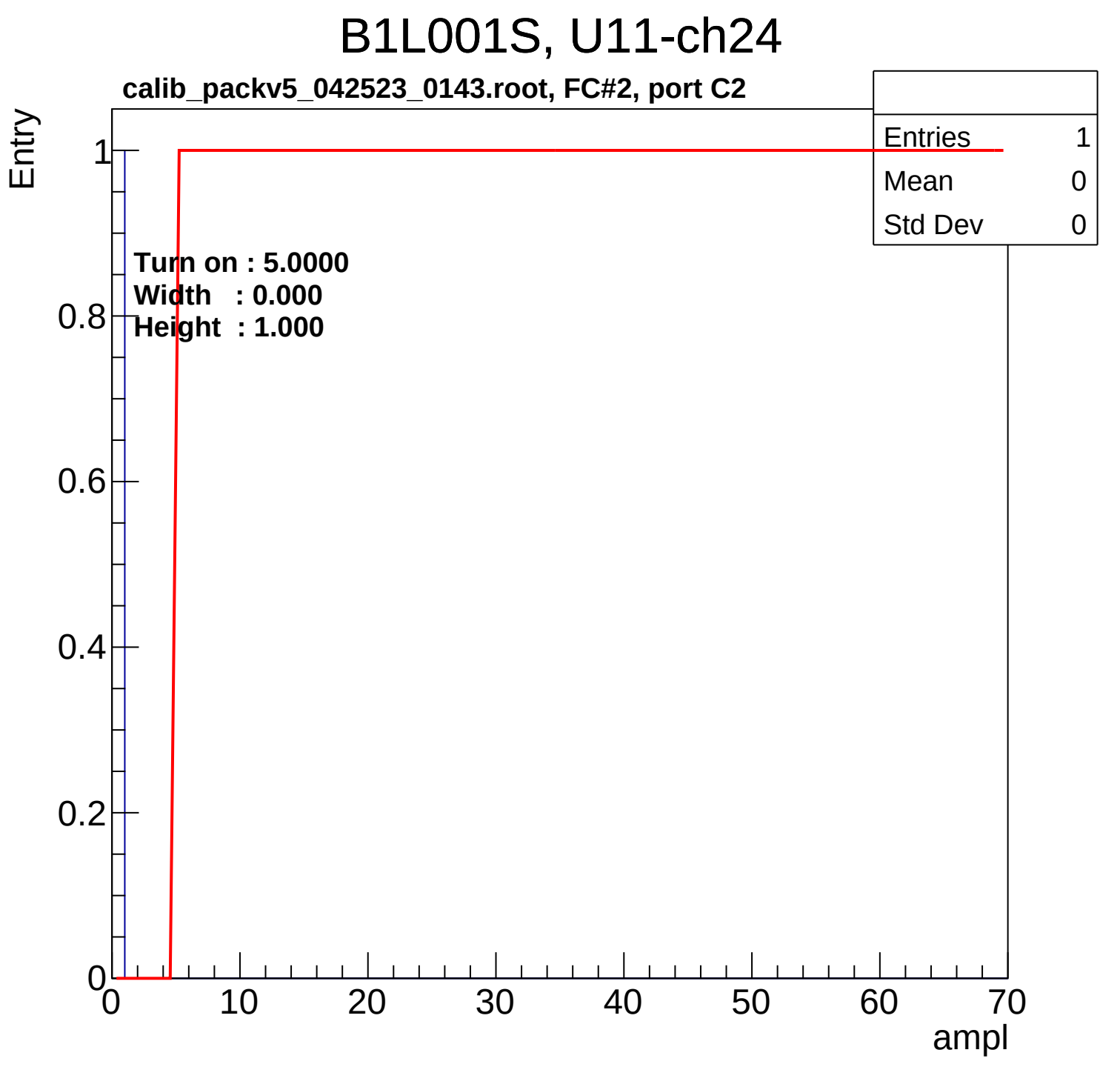

B1L001S, U11-ch19
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

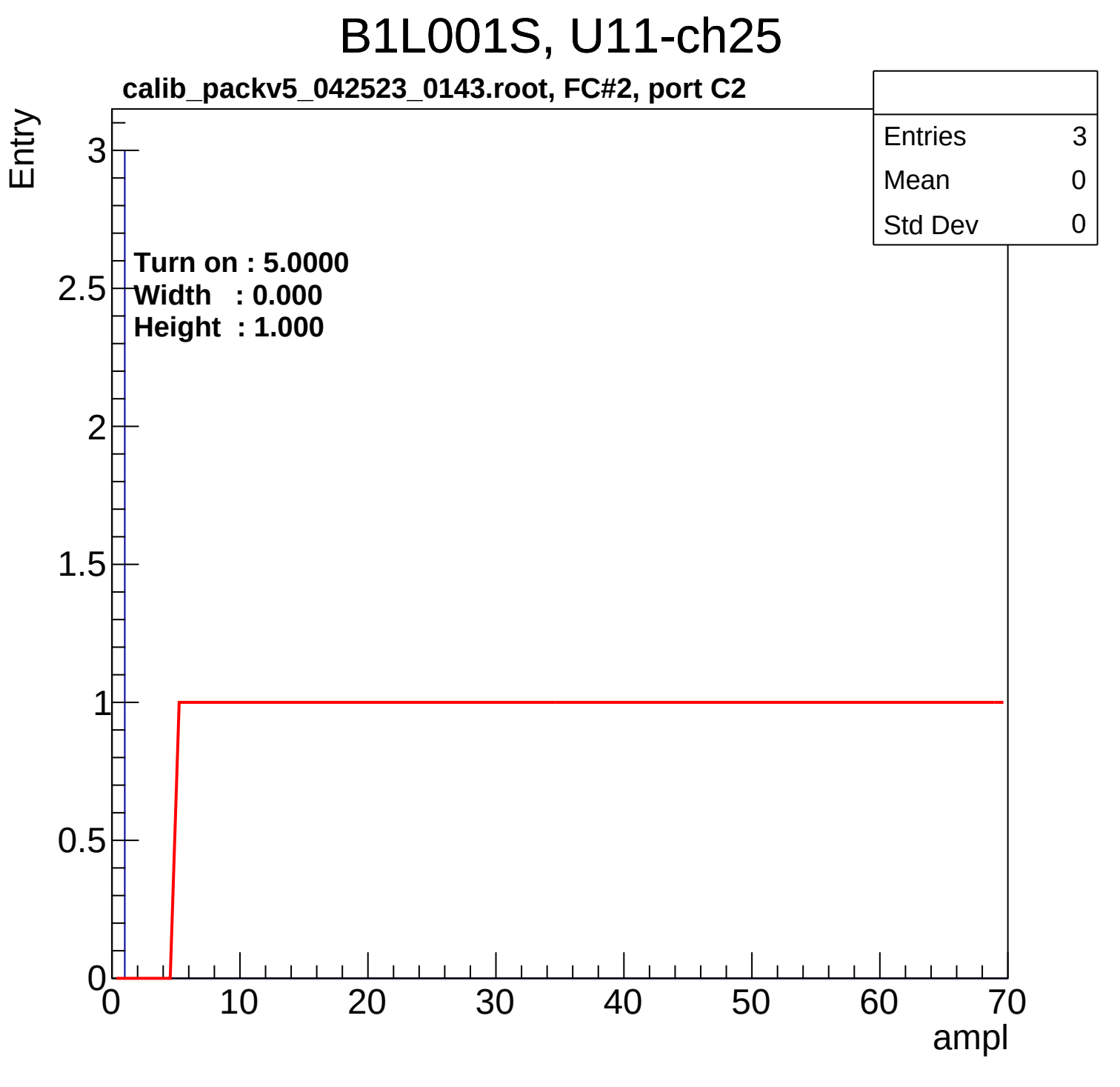

B1L001S, U11-ch20
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

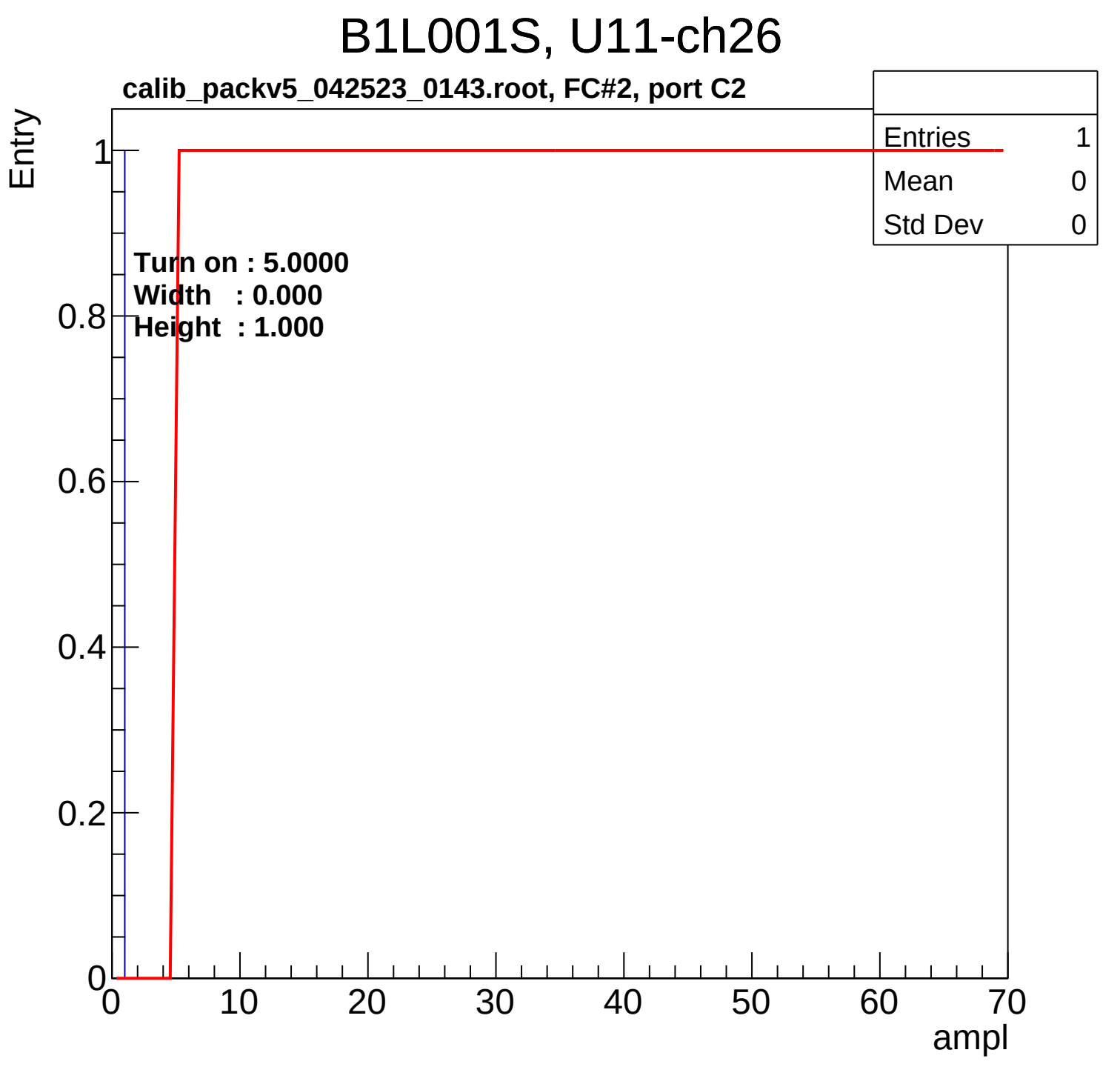

B1L001S, U11-ch21
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

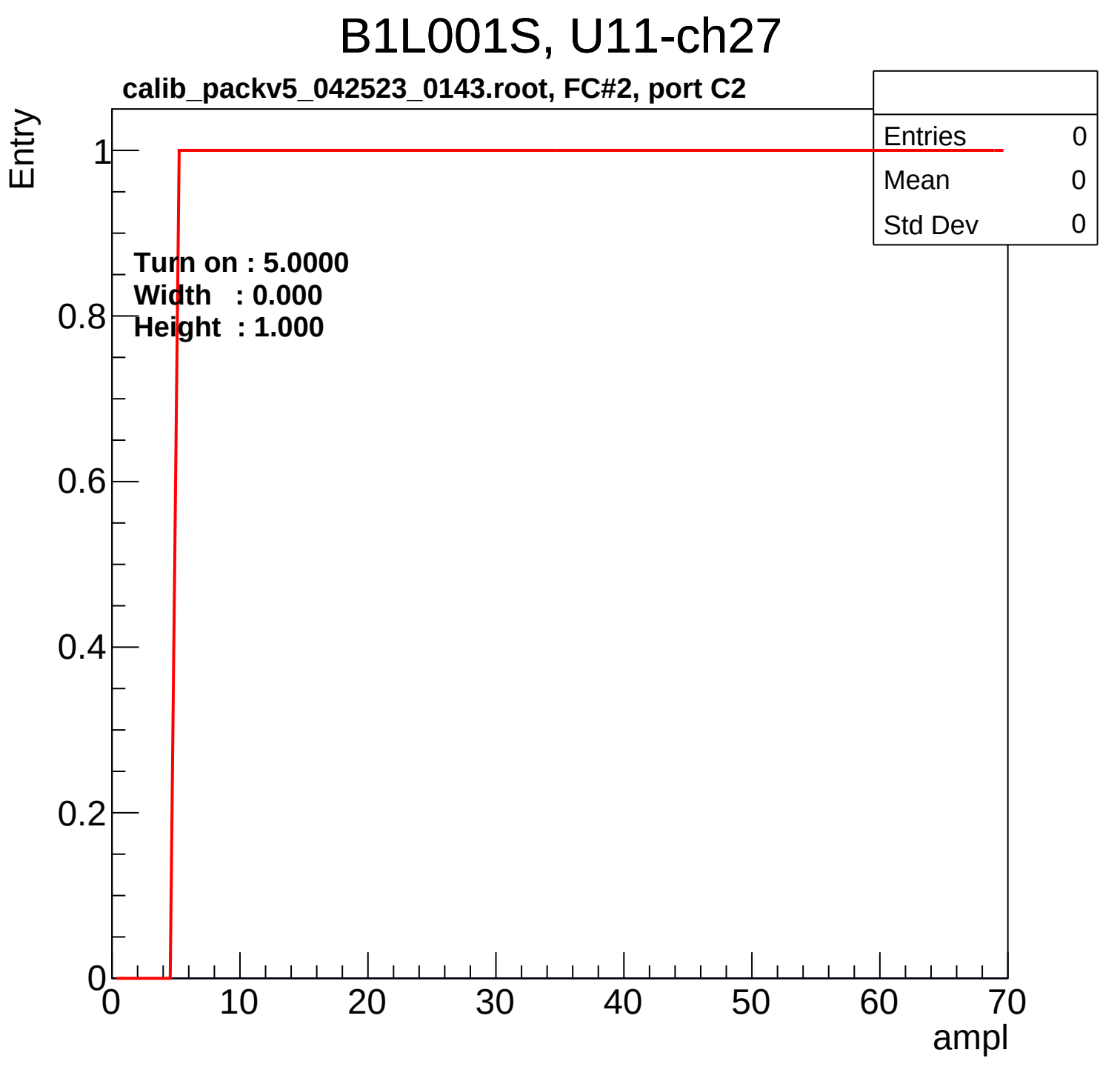

B1L001S, U11-ch22
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

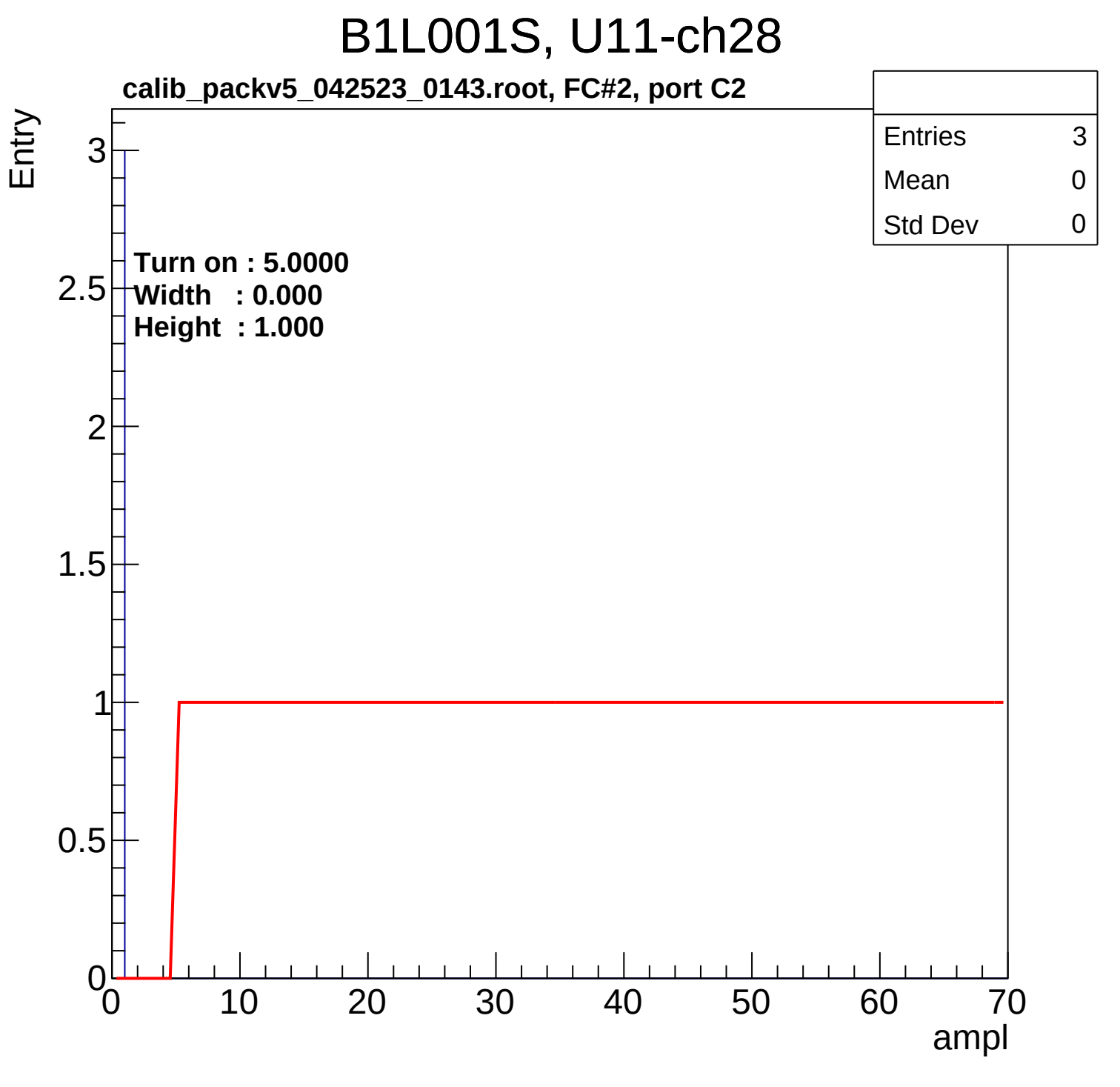

B1L001S, U11-ch23
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

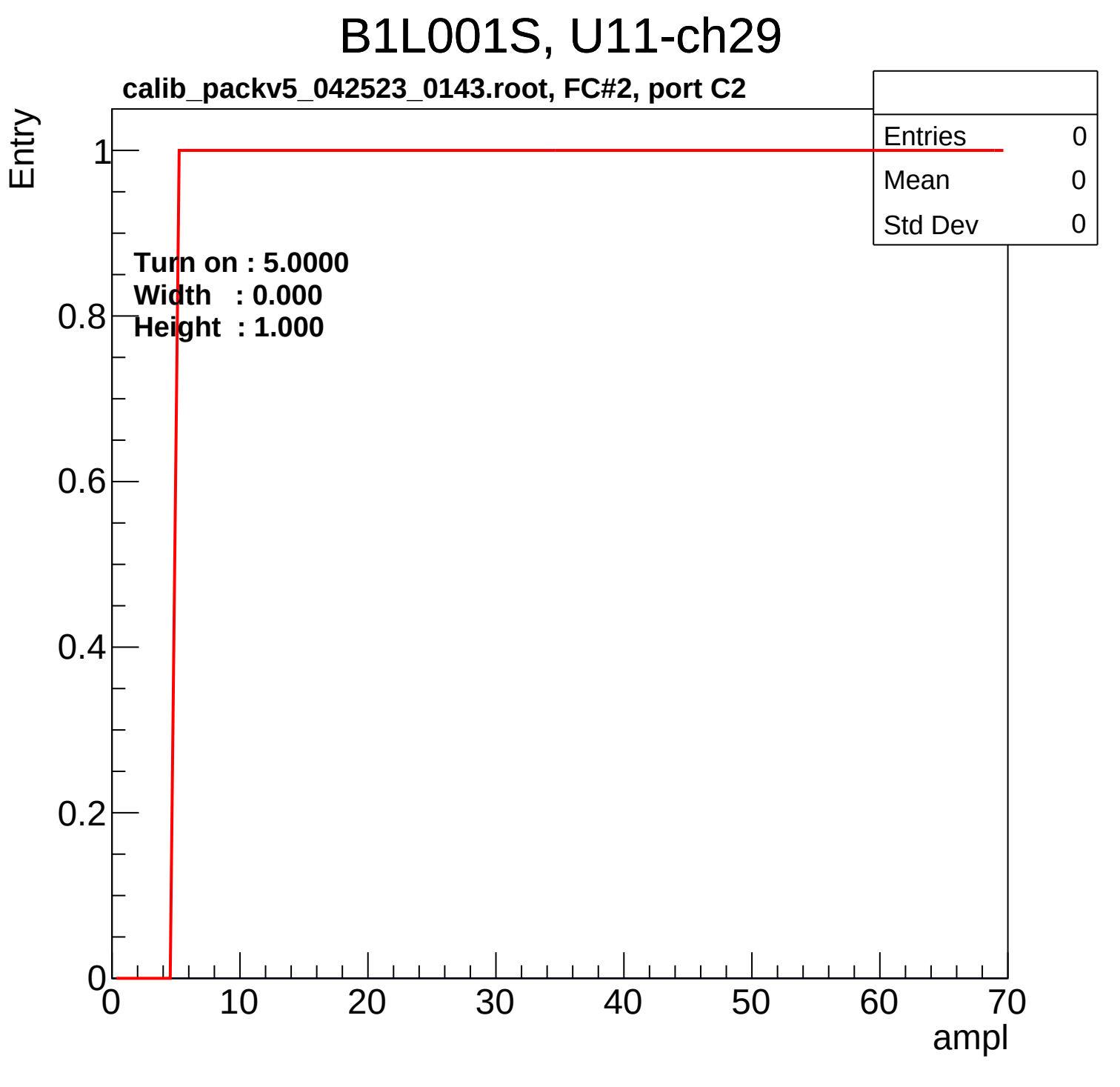

B1L001S, U11-ch24
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

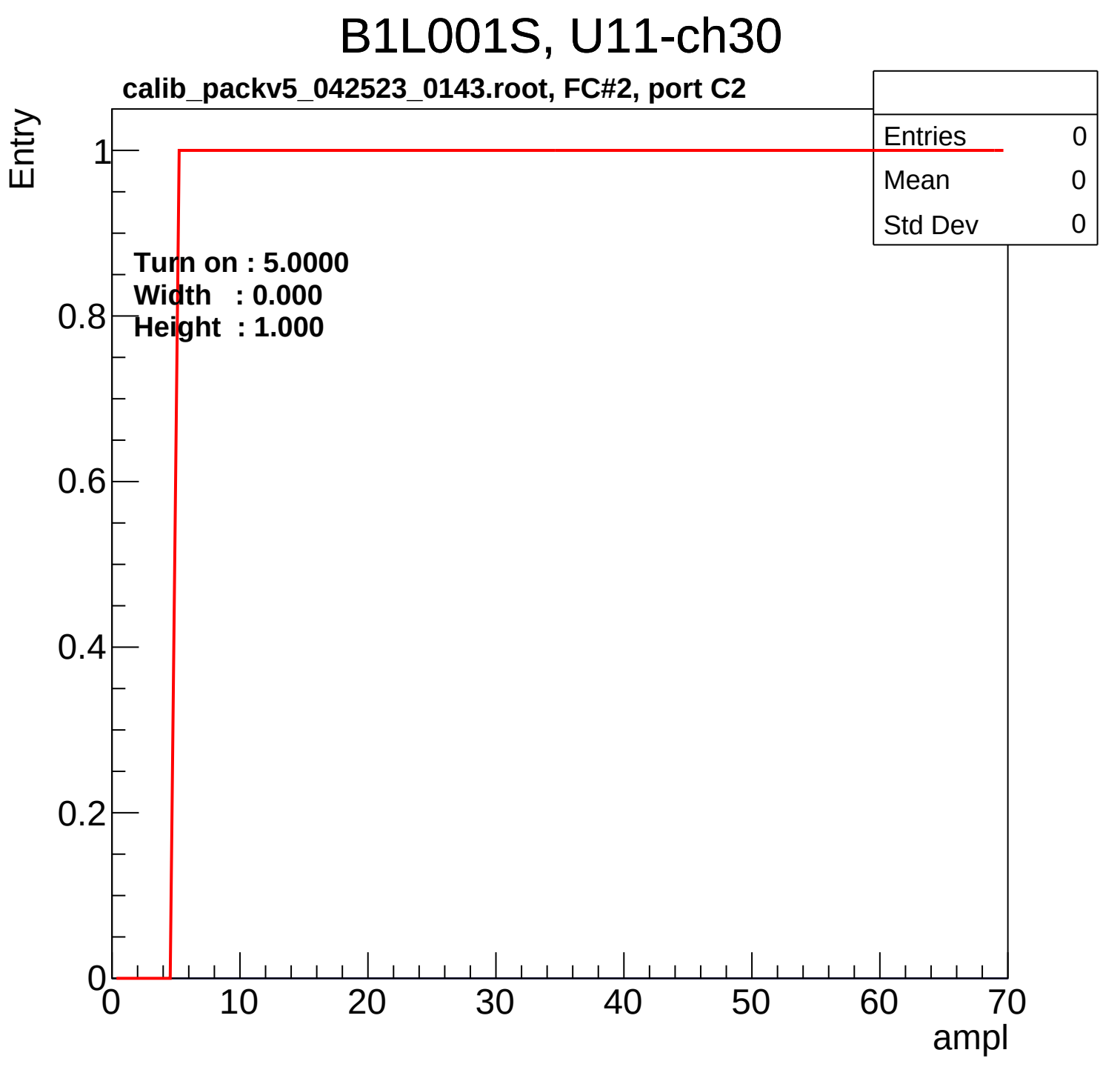

B1L001S, U11-ch25
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

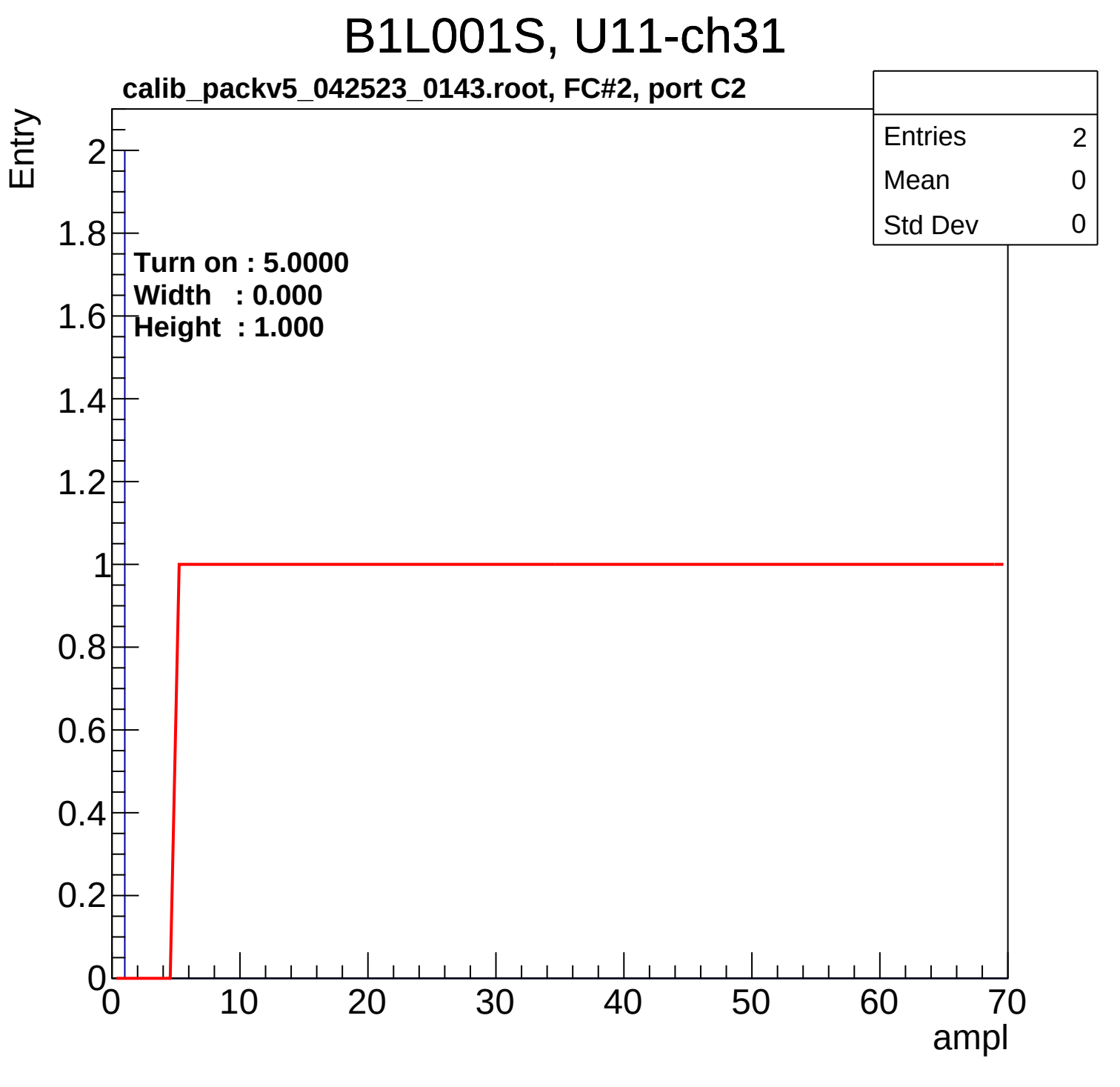

B1L001S, U11-ch26
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

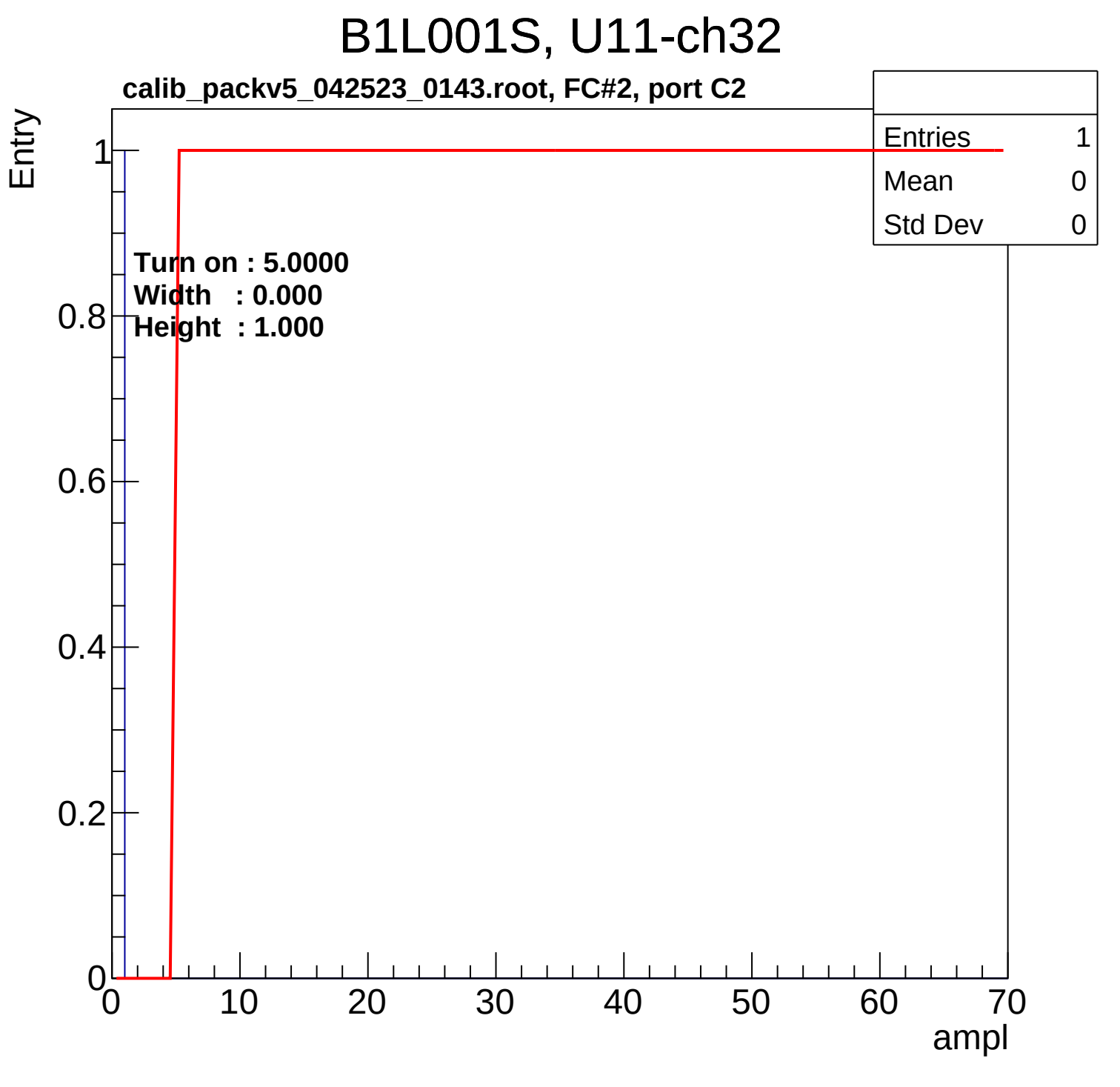

B1L001S, U11-ch27
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

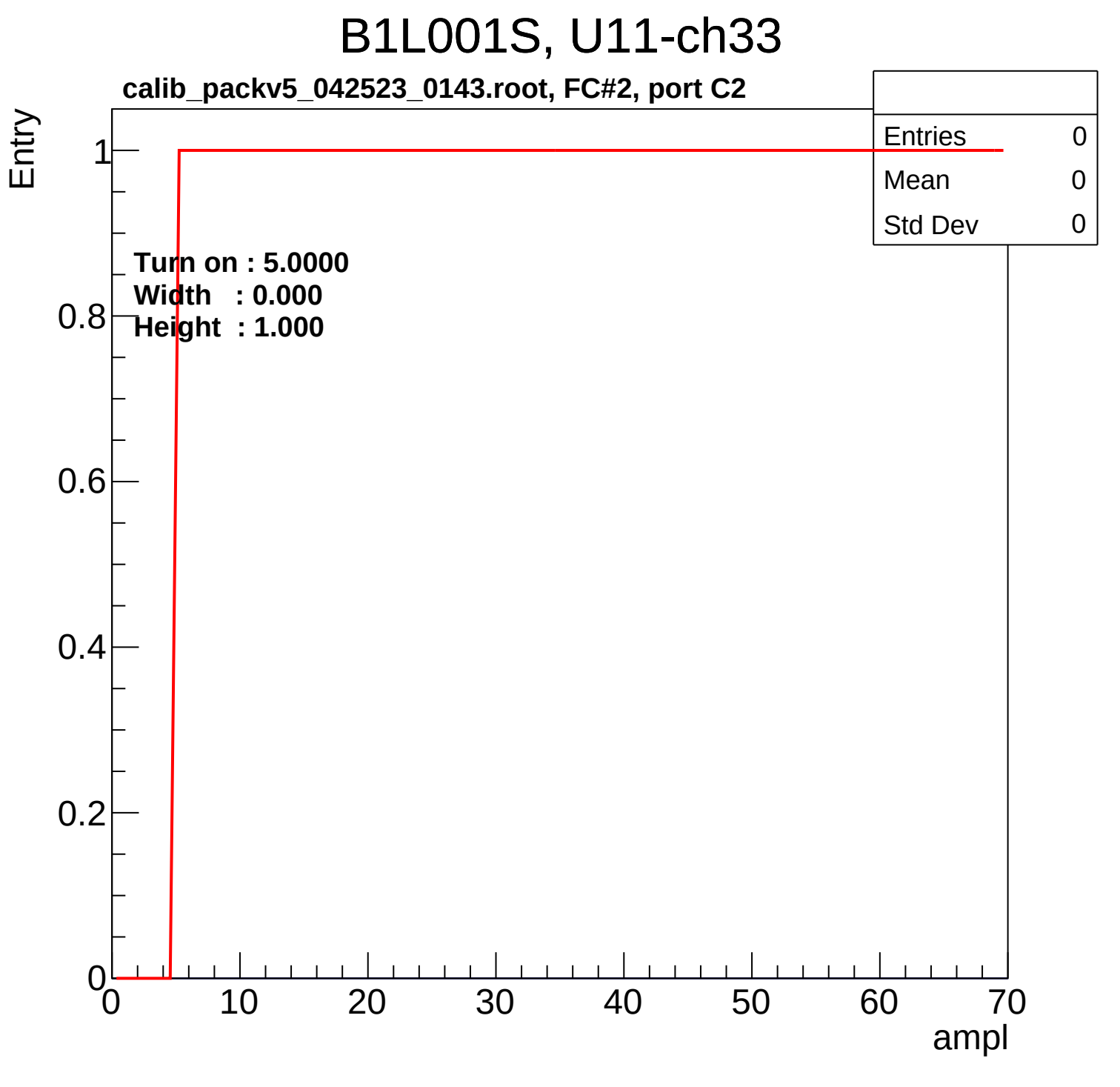

B1L001S, U11-ch28
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

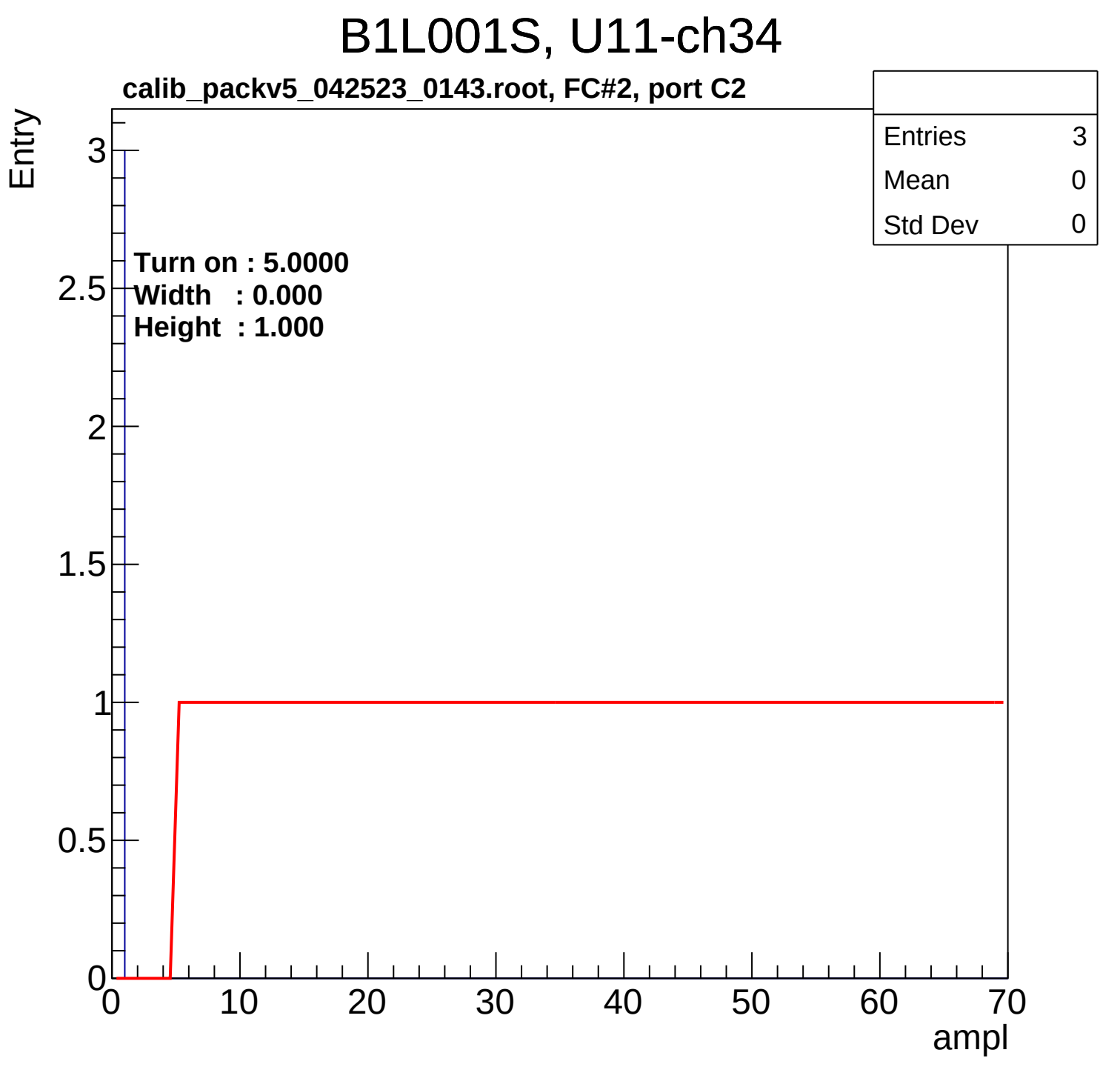

B1L001S, U11-ch29
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

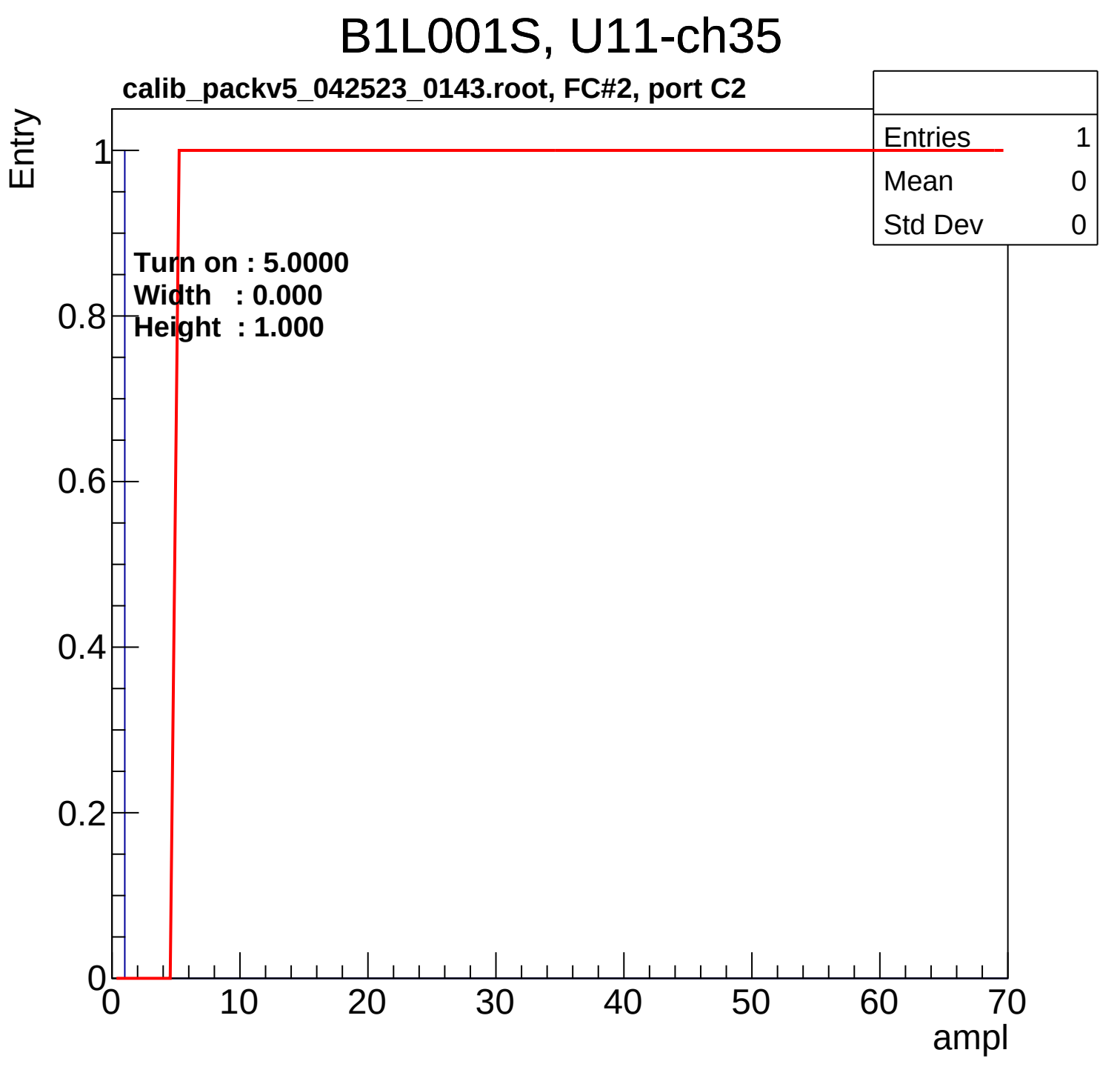

B1L001S, U11-ch30
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

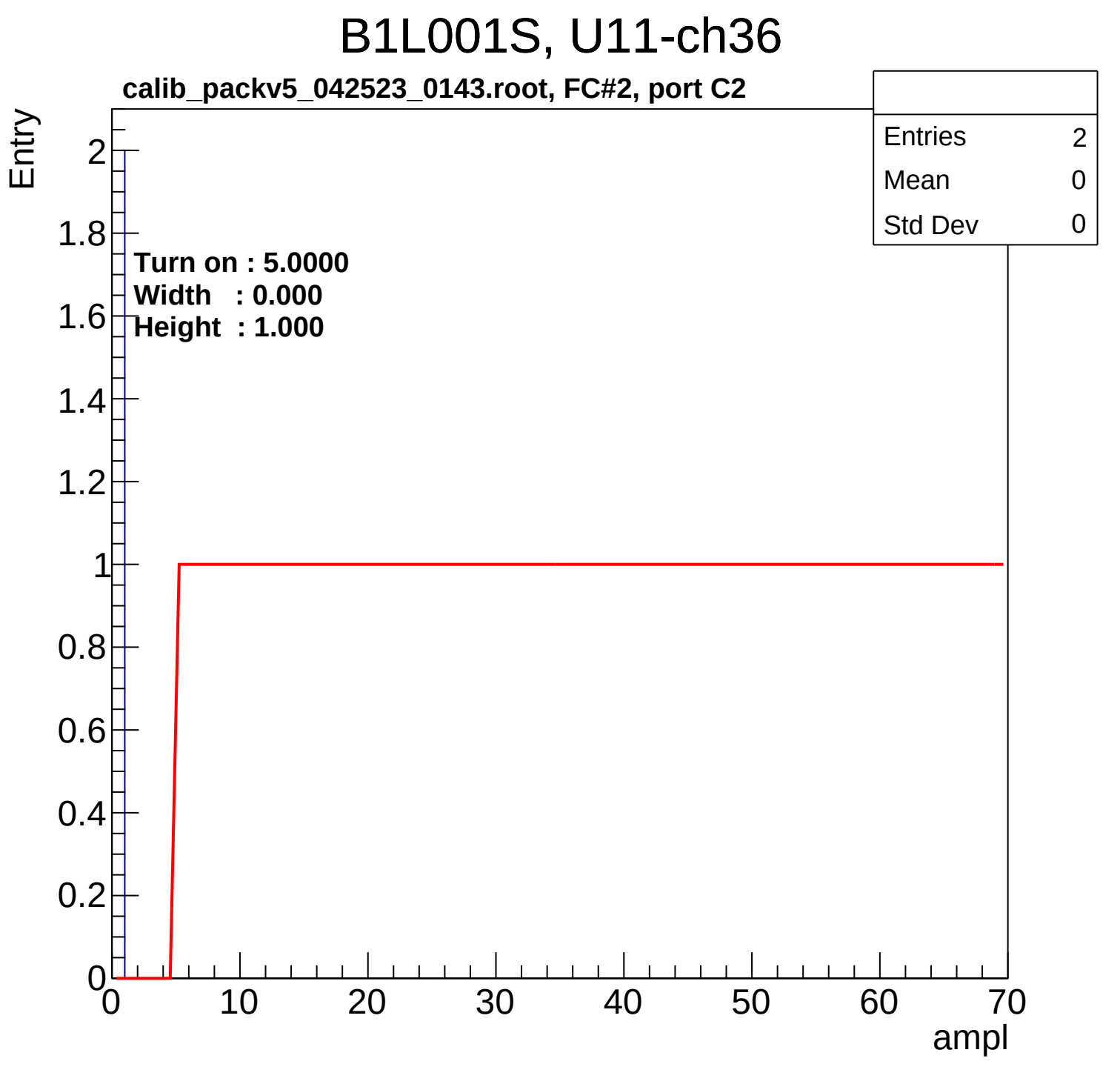

B1L001S, U11-ch31
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

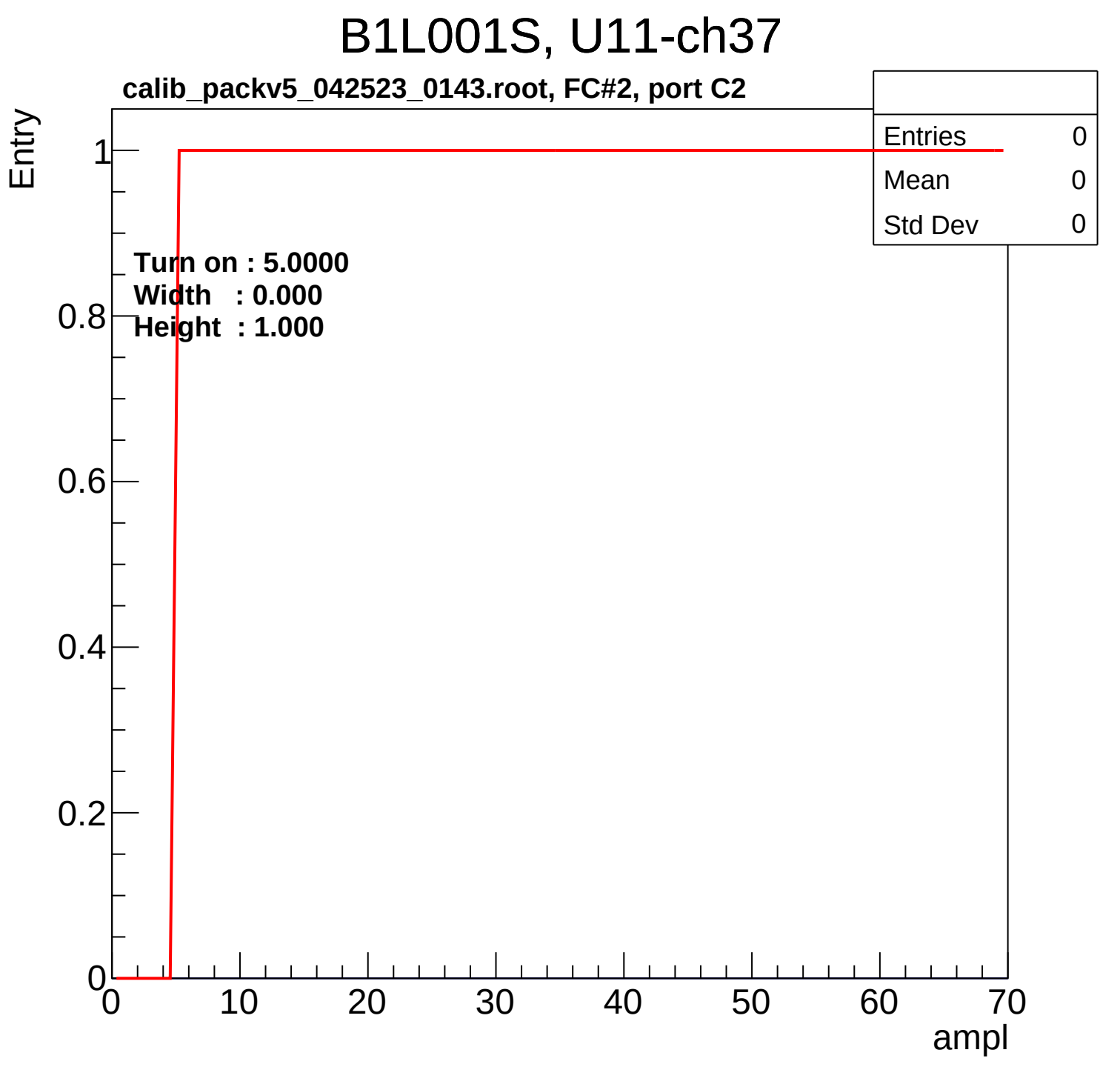

B1L001S, U11-ch32
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

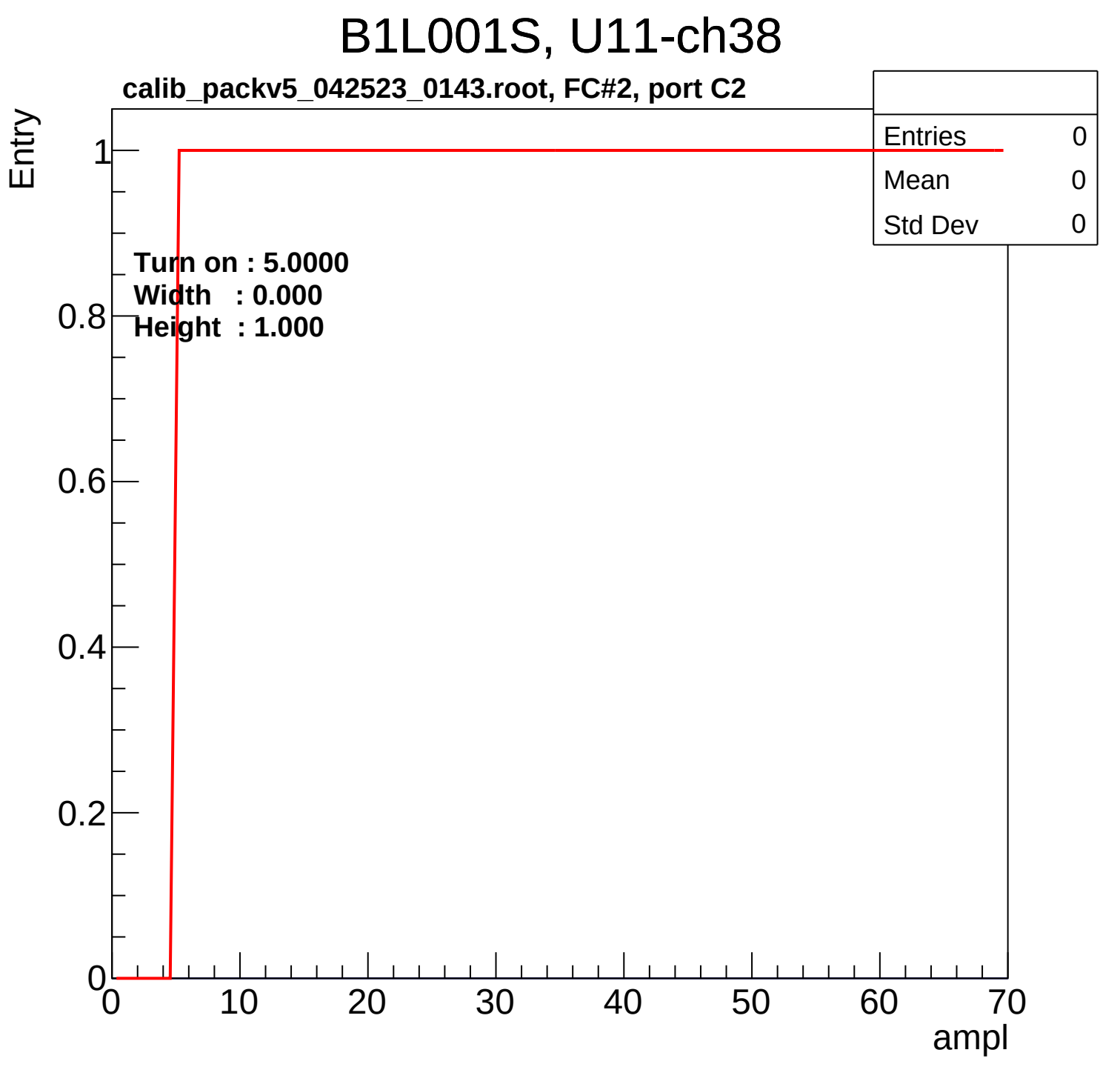

B1L001S, U11-ch33
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

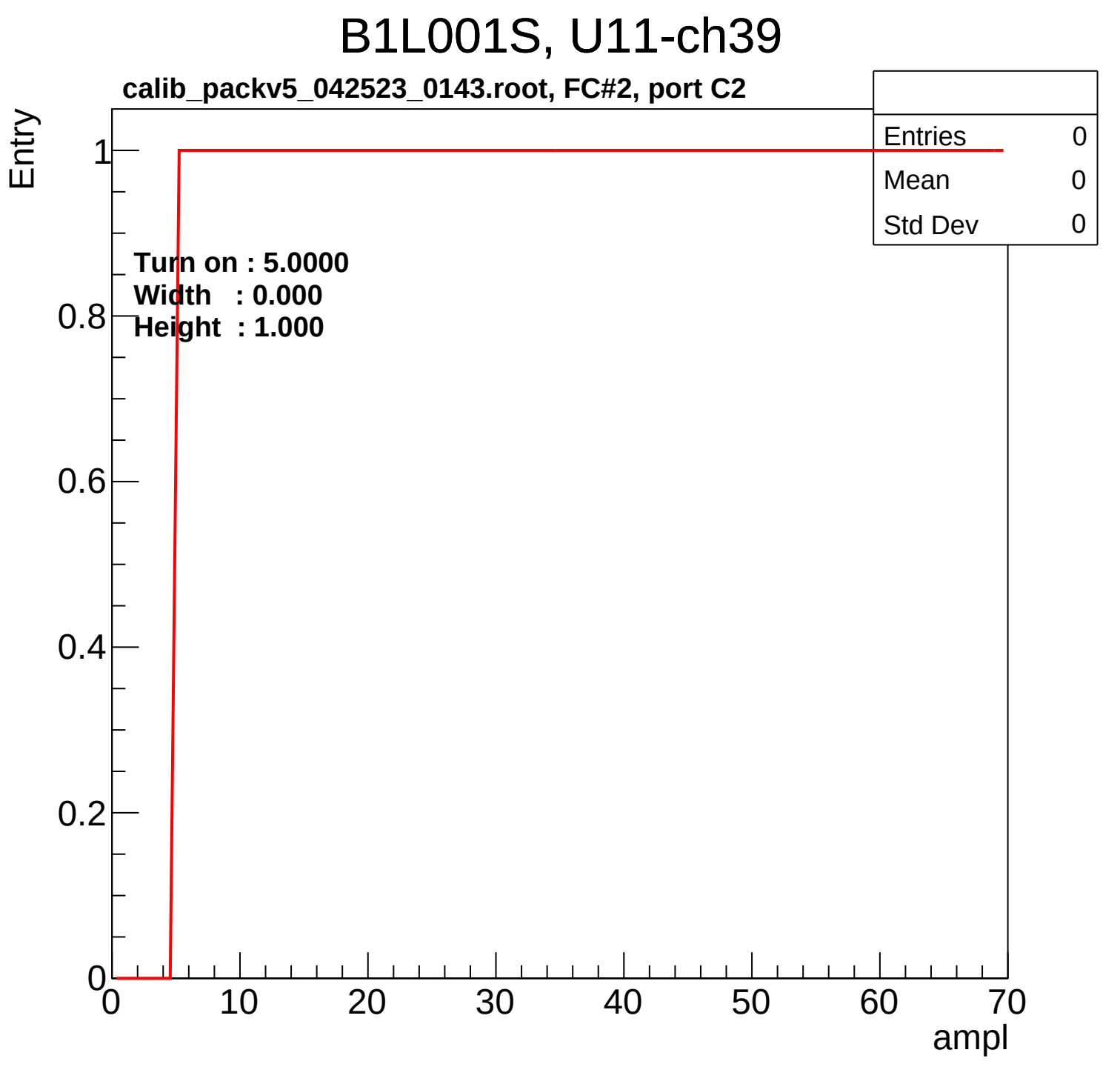

B1L001S, U11-ch34
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

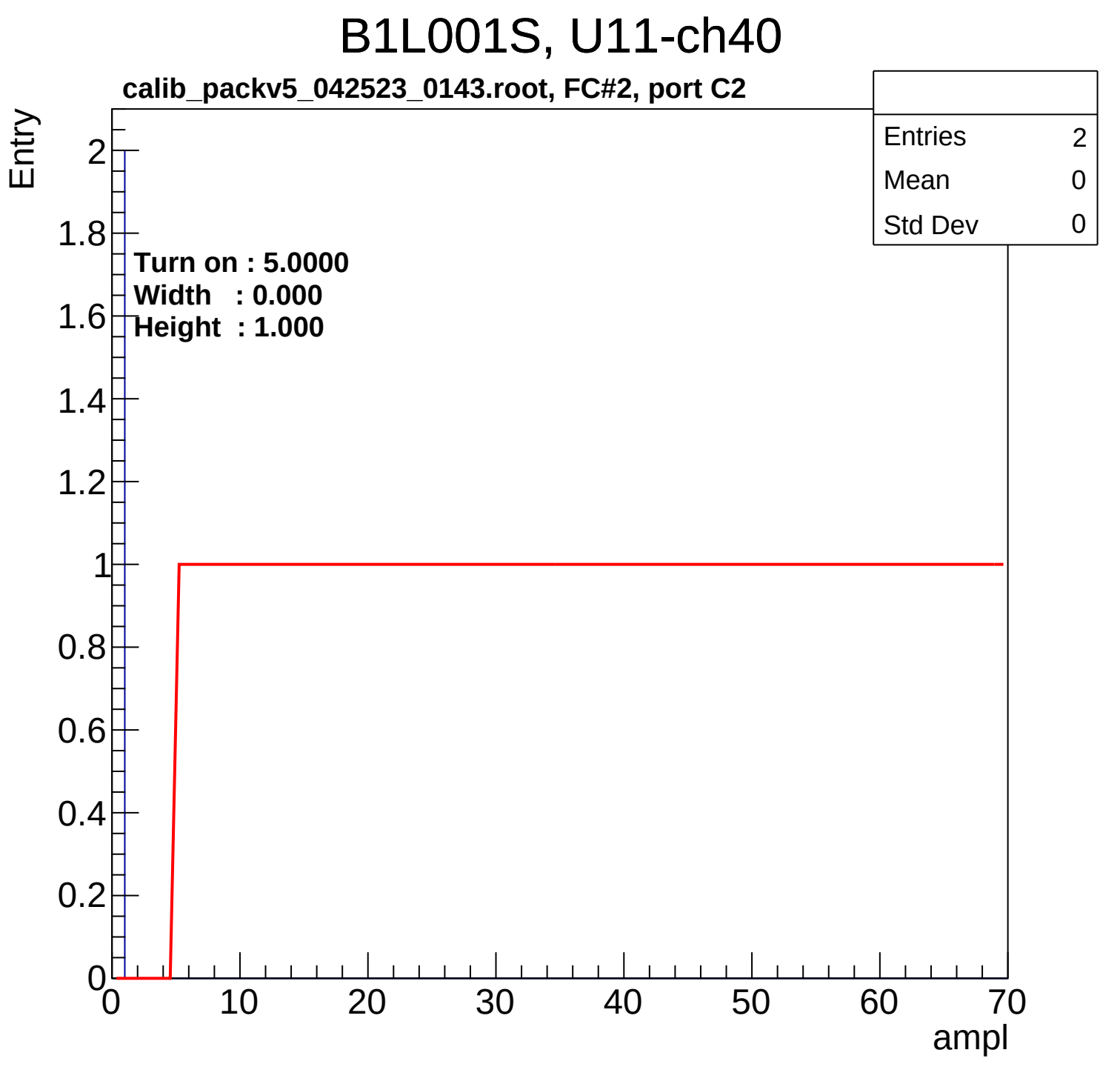

B1L001S, U11-ch35
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

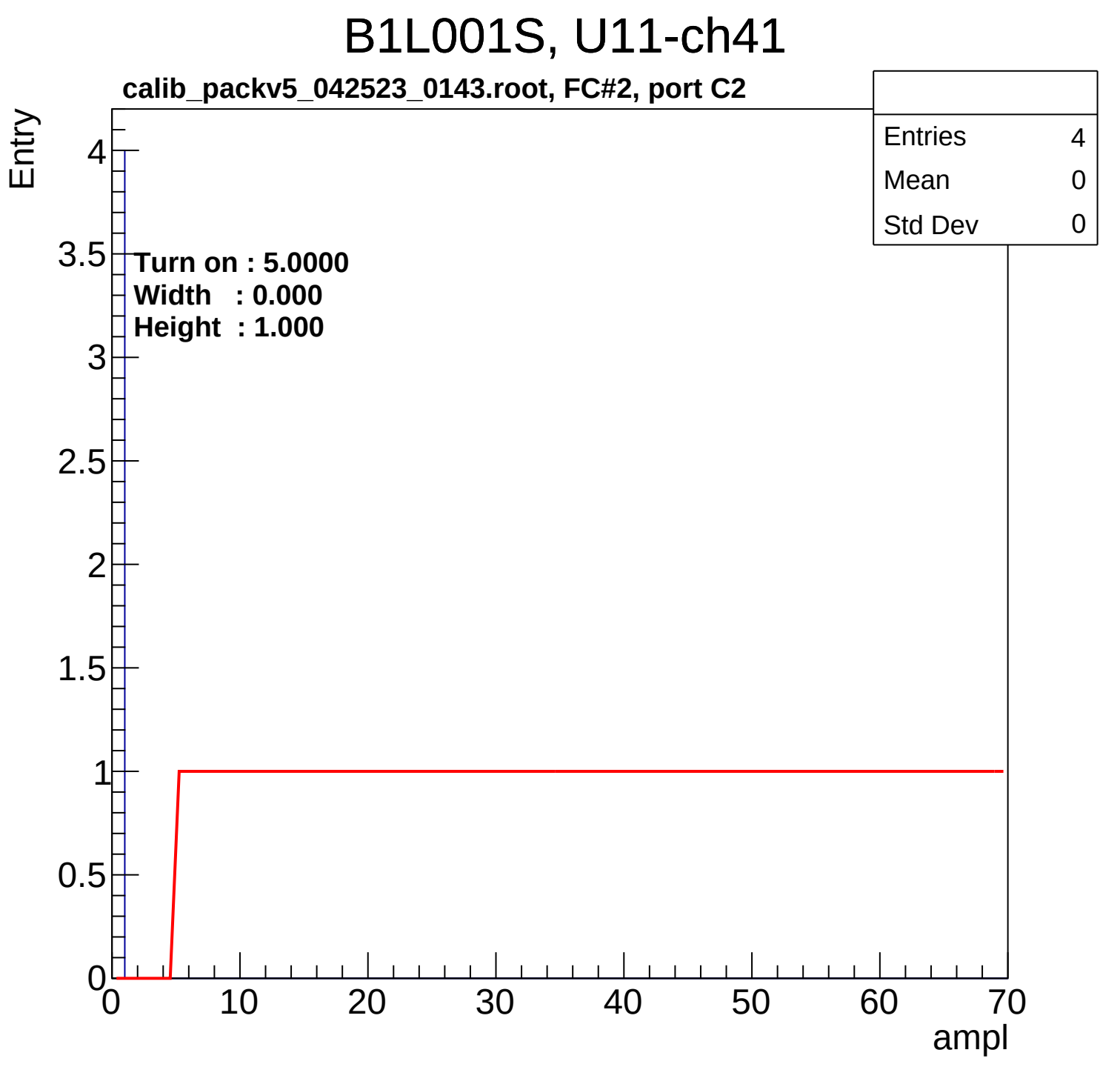

B1L001S, U11-ch36
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

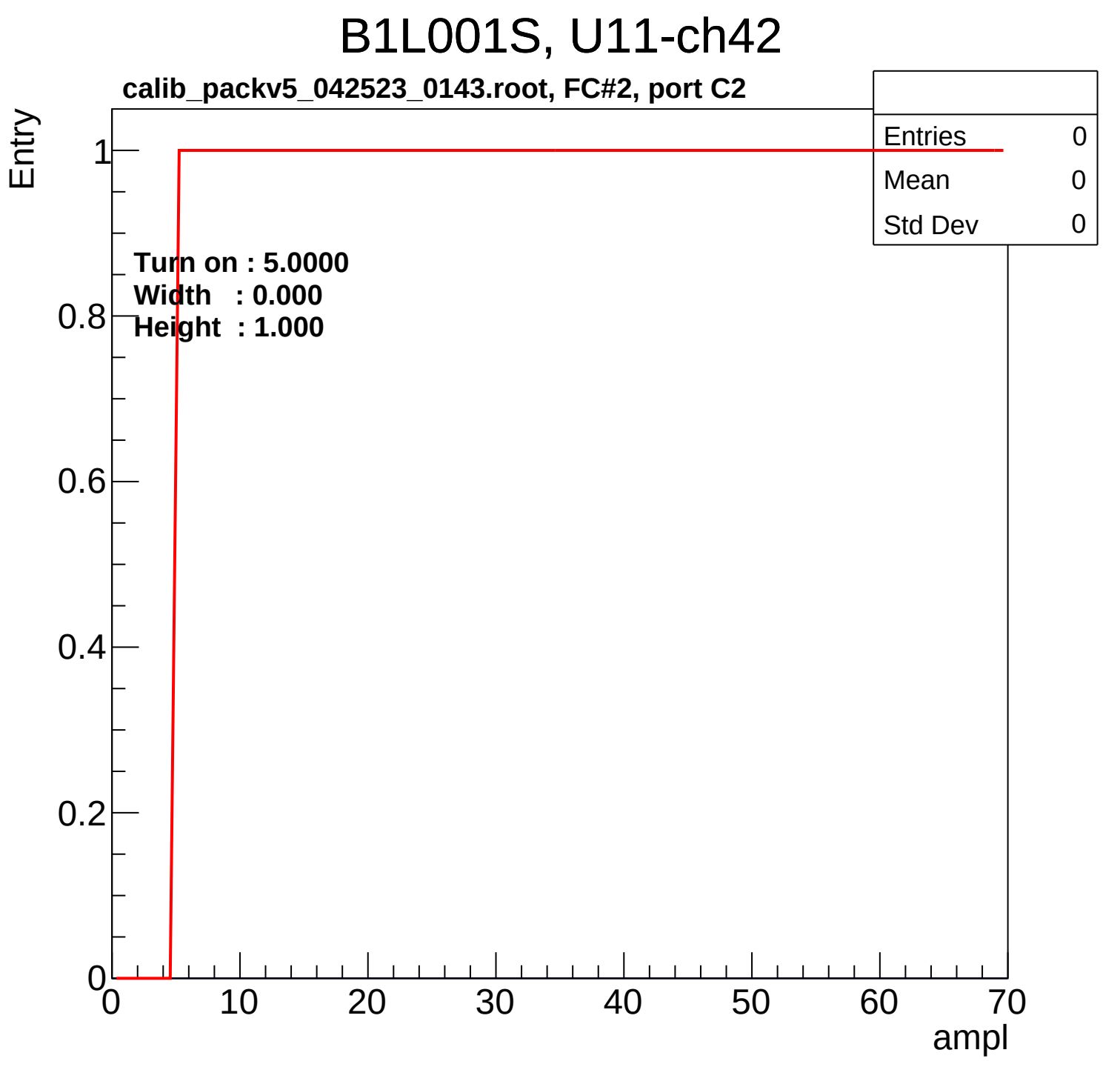

B1L001S, U11-ch37
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

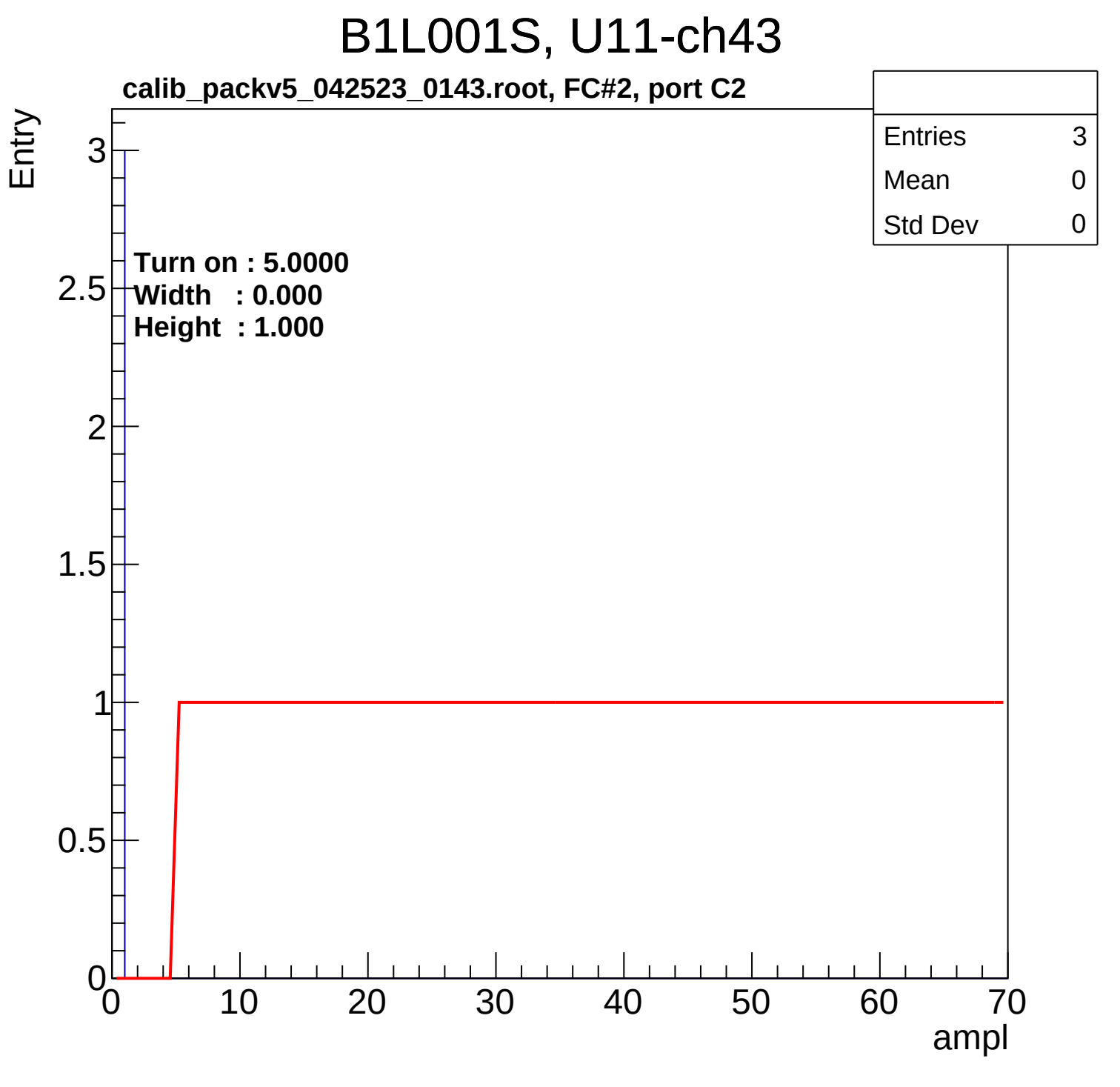

B1L001S, U11-ch38
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

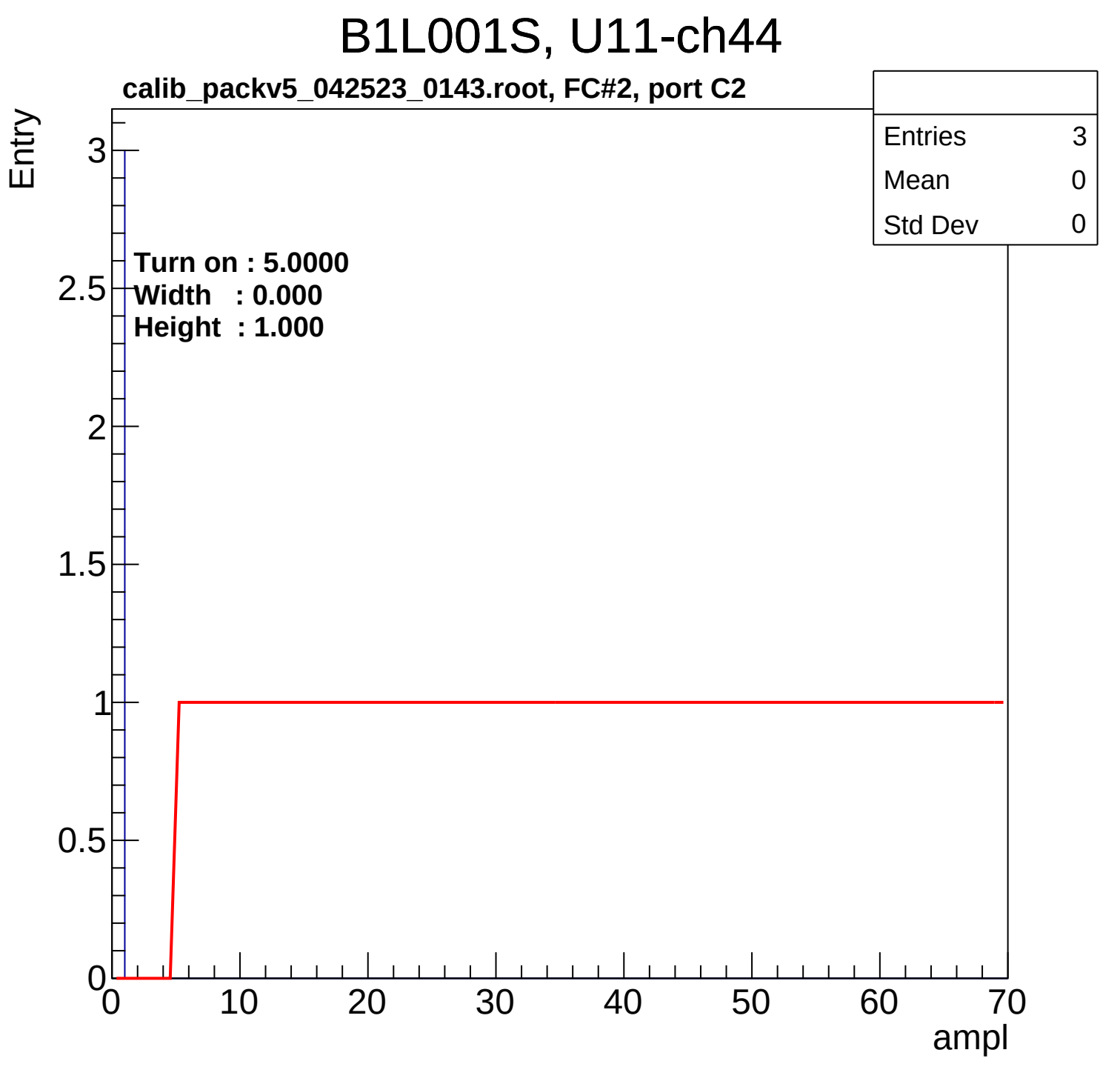

B1L001S, U11-ch39
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

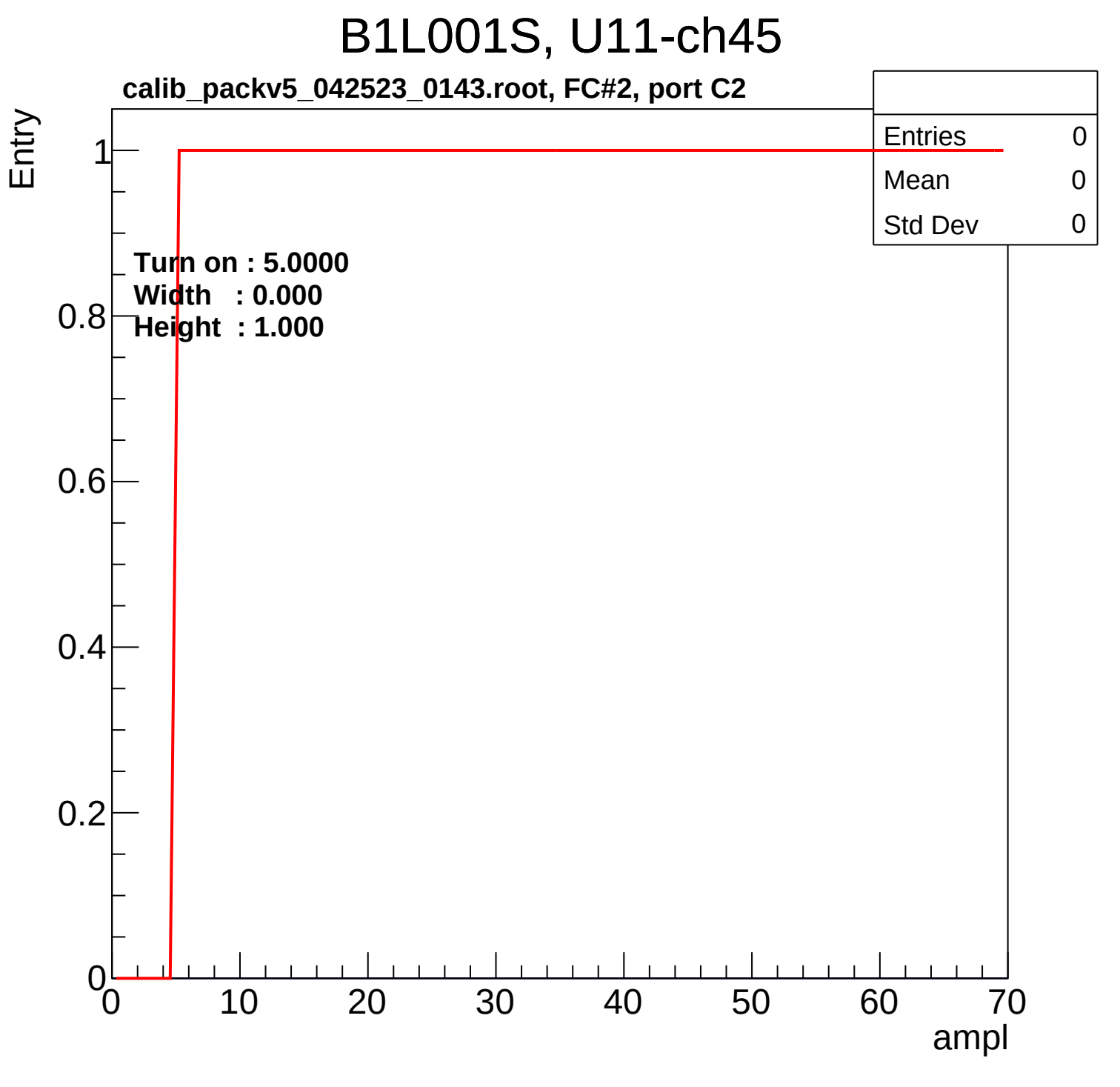

B1L001S, U11-ch40
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

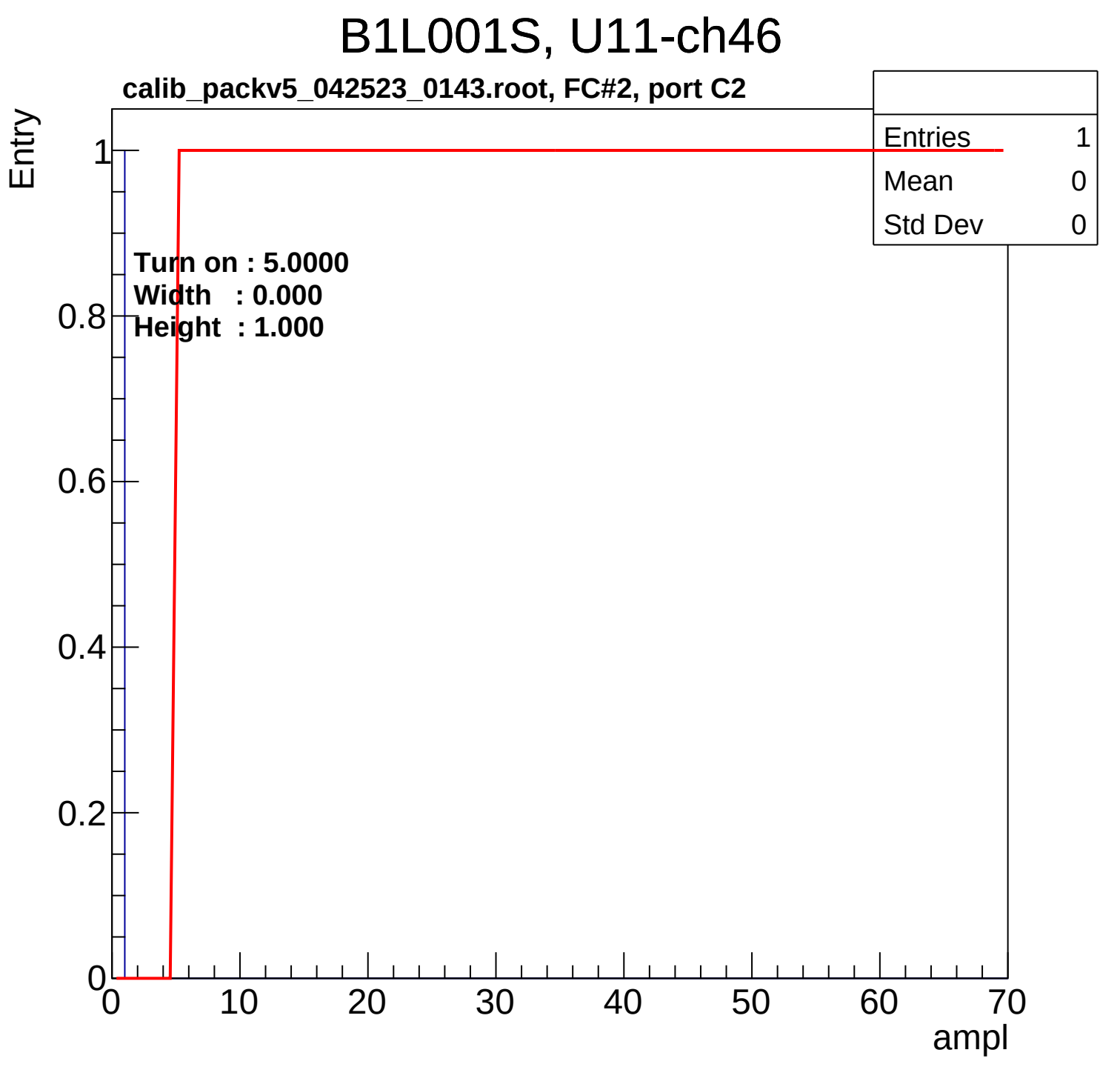

B1L001S, U11-ch41
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

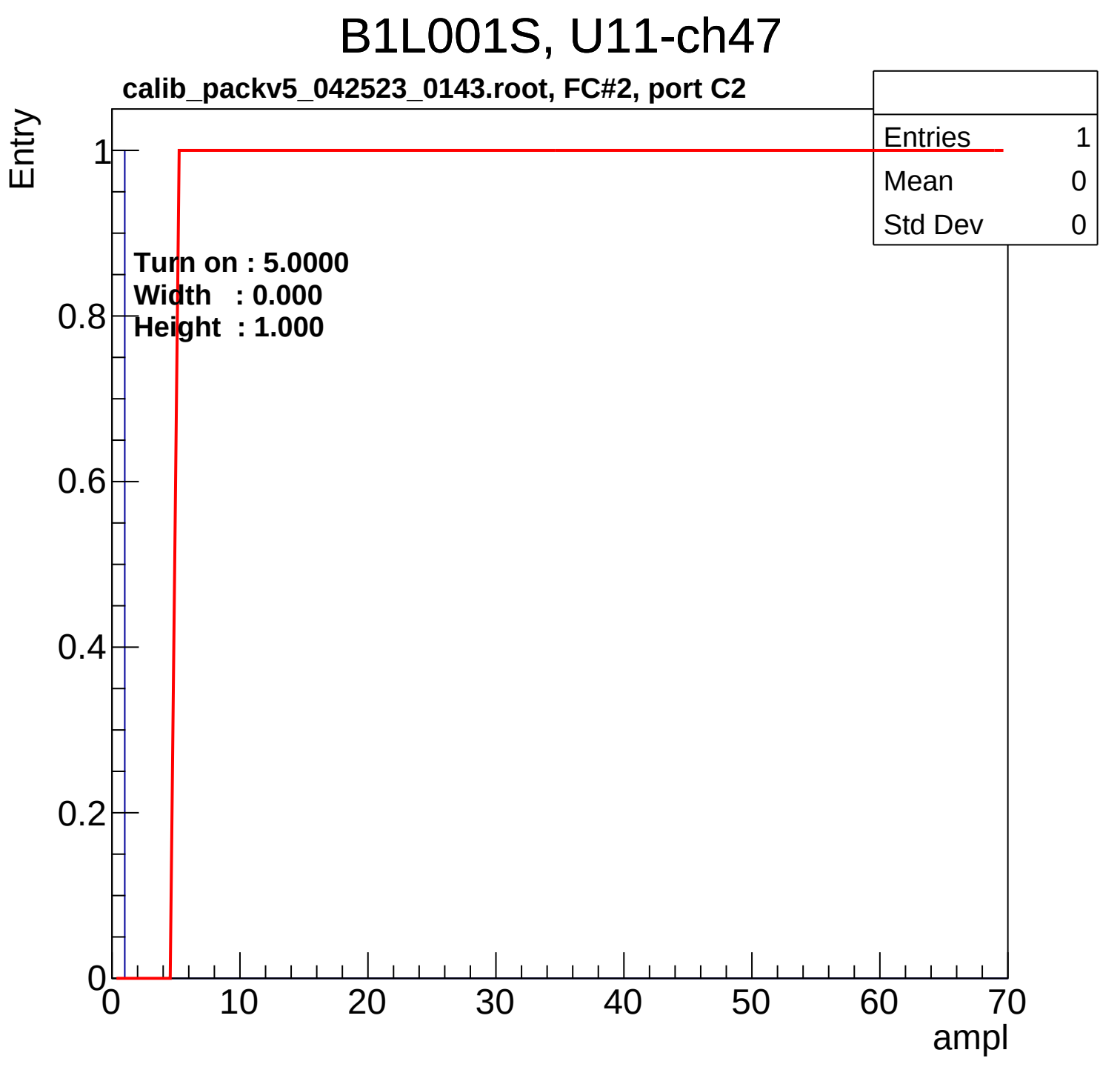

B1L001S, U11-ch42
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

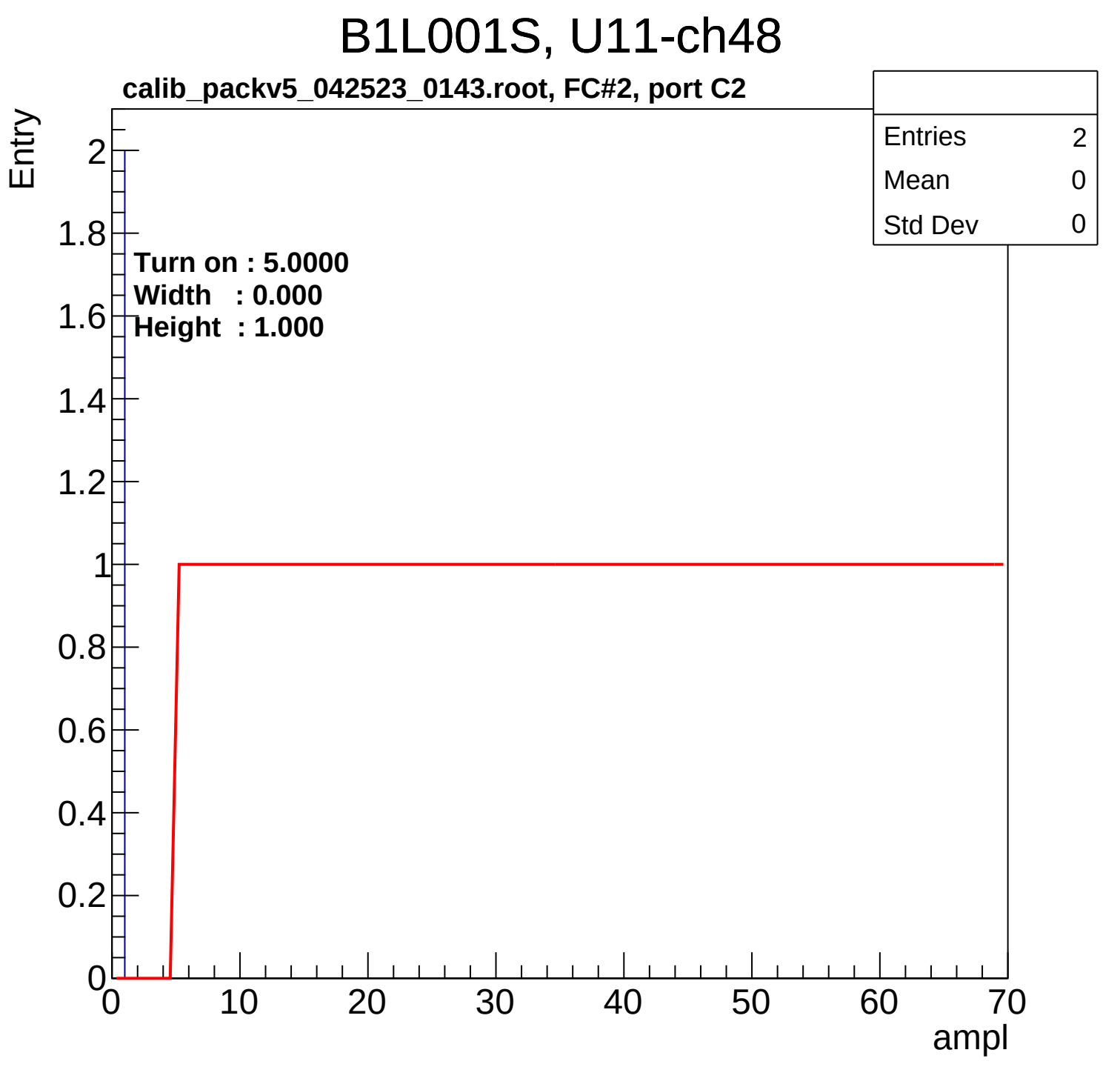

B1L001S, U11-ch43
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

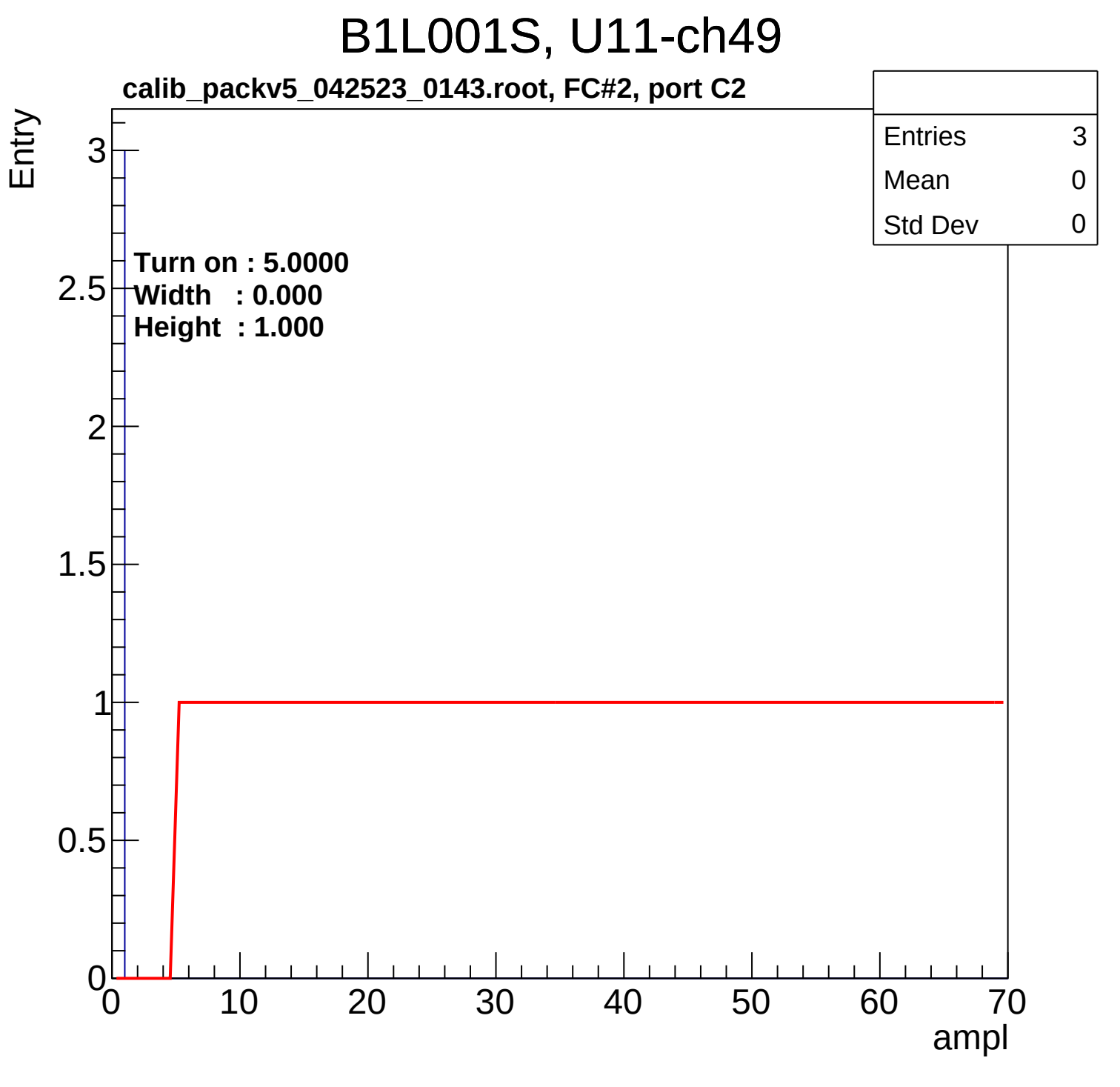

B1L001S, U11-ch44
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

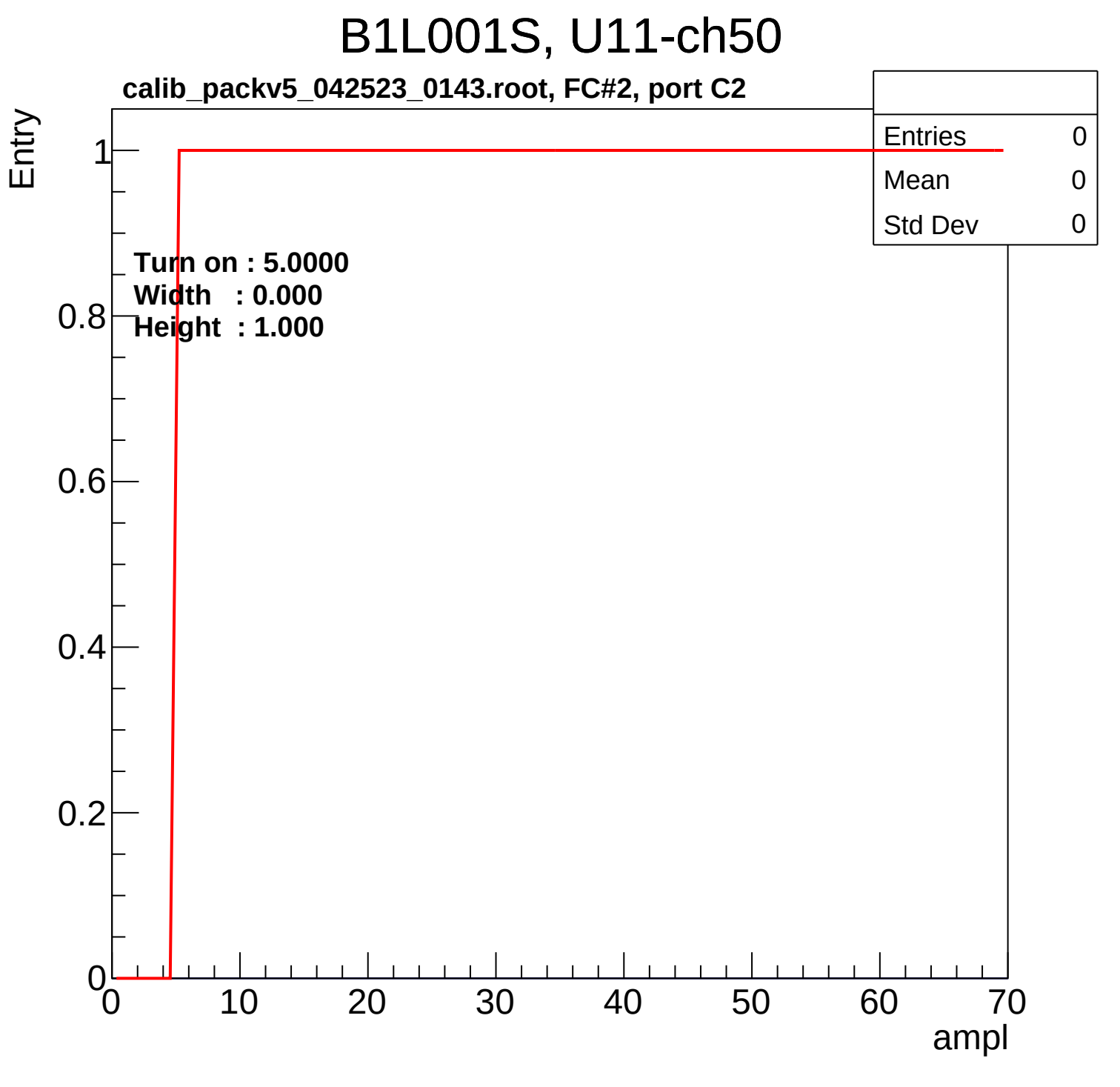

B1L001S, U11-ch45
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

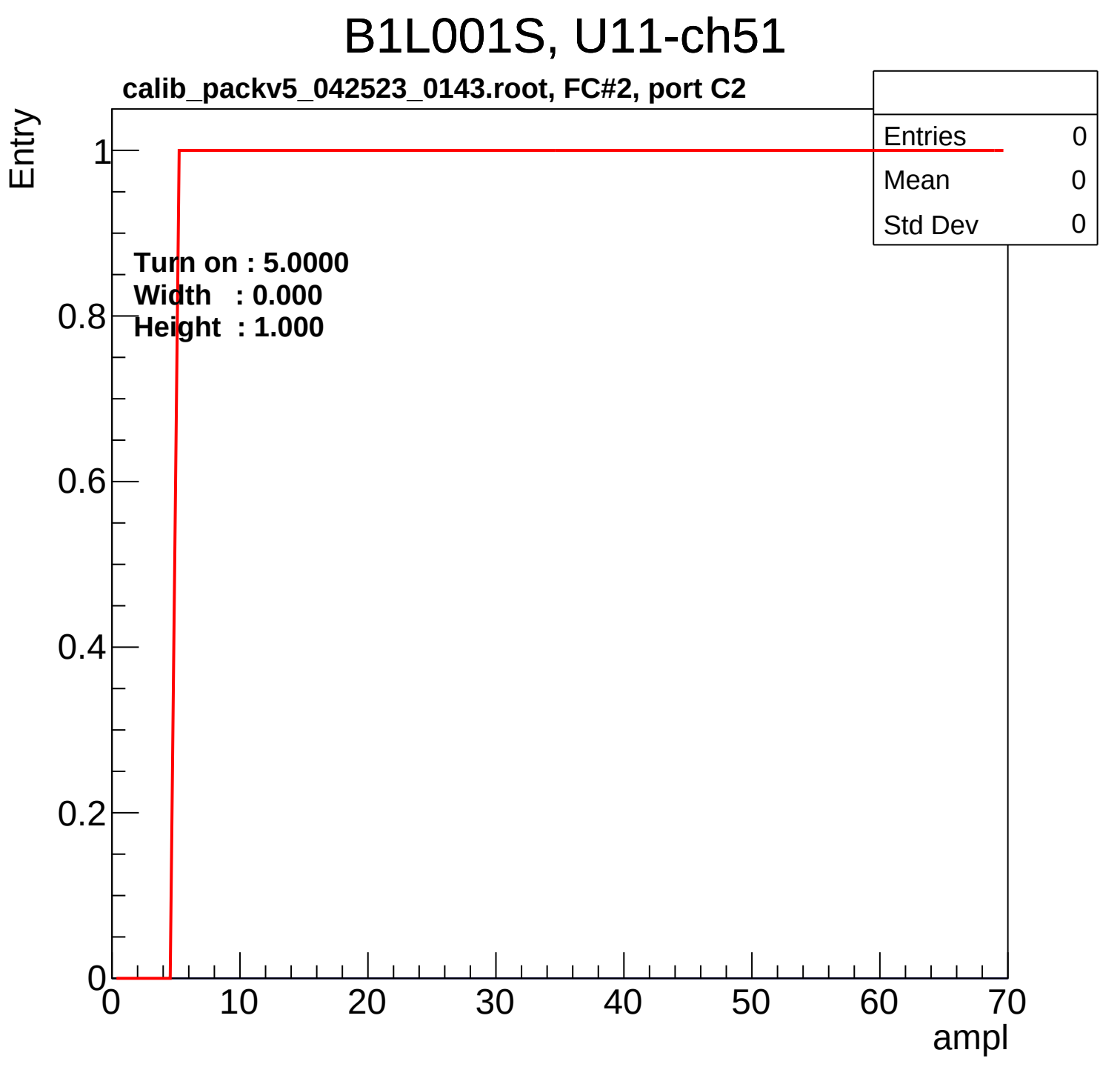

B1L001S, U11-ch46
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

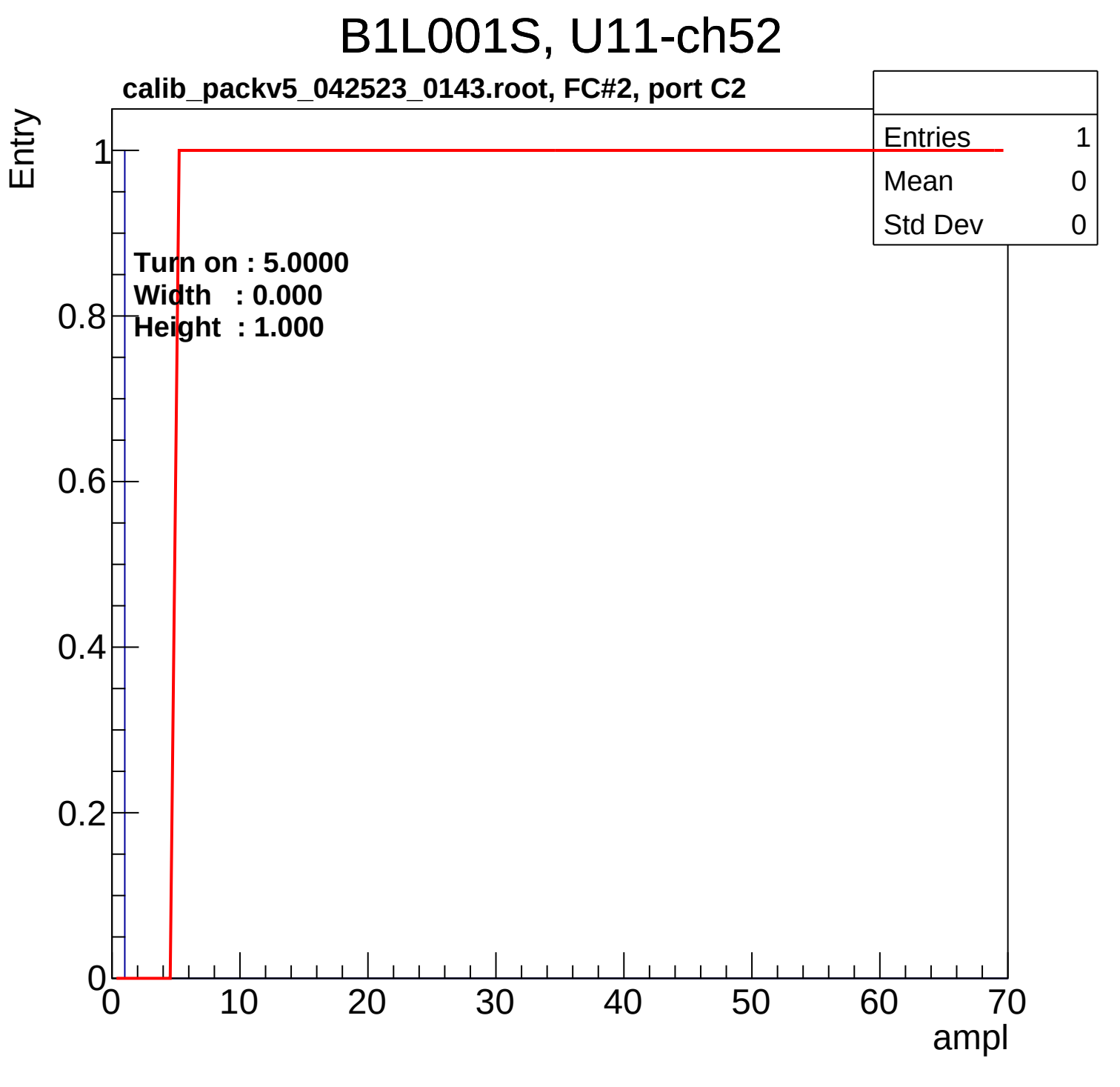

B1L001S, U11-ch47
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

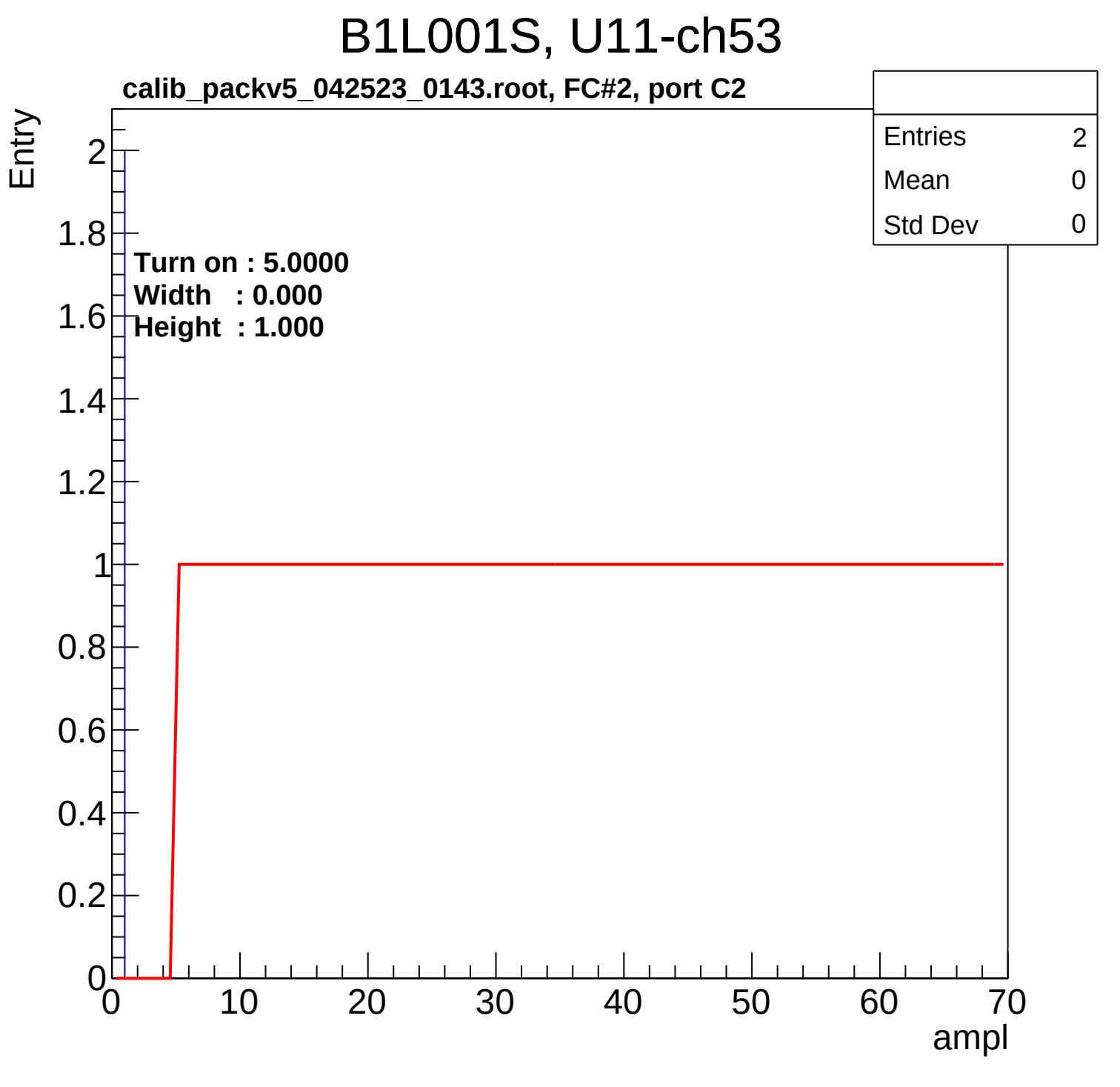

B1L001S, U11-ch48
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

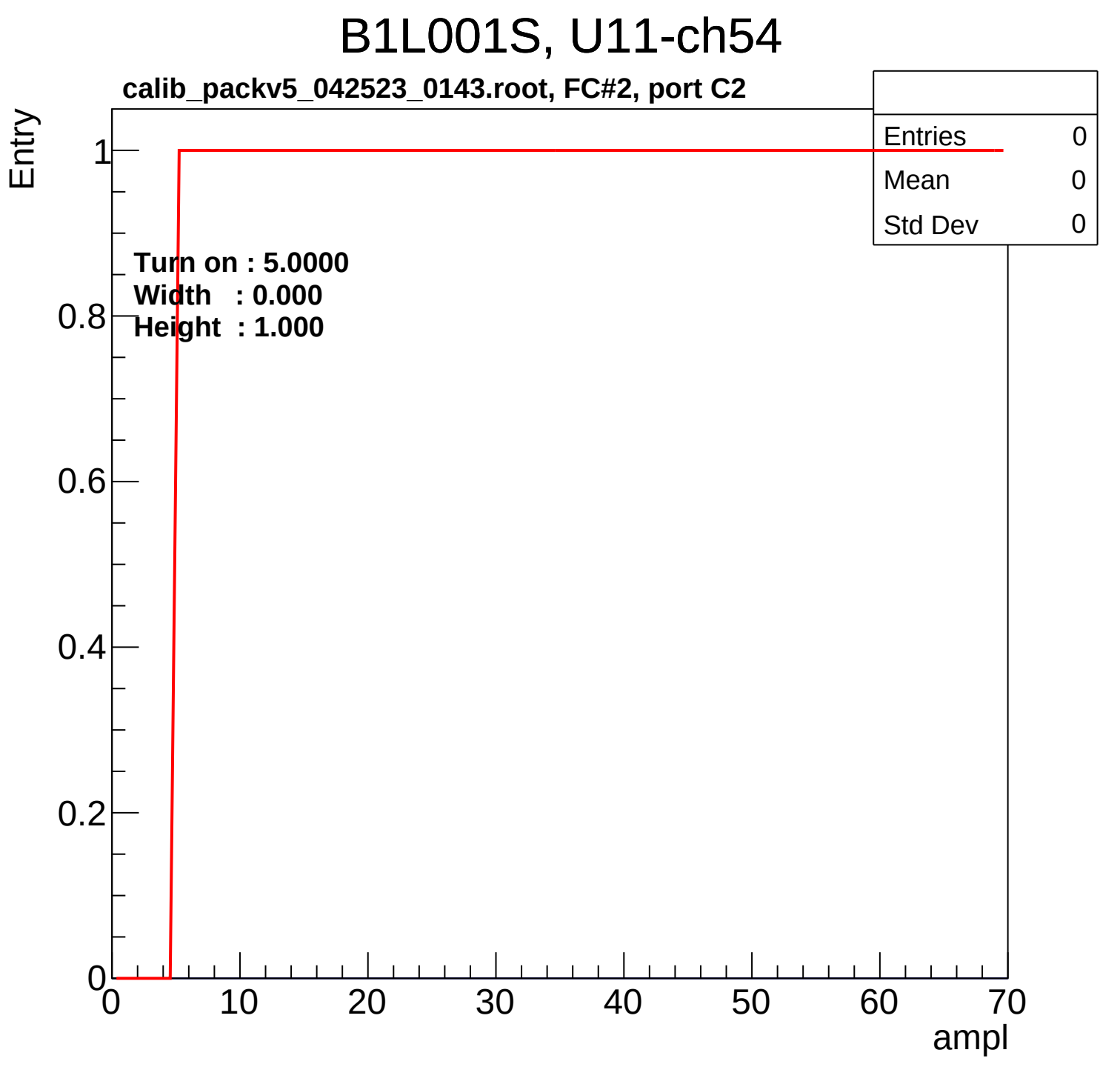

B1L001S, U11-ch49
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

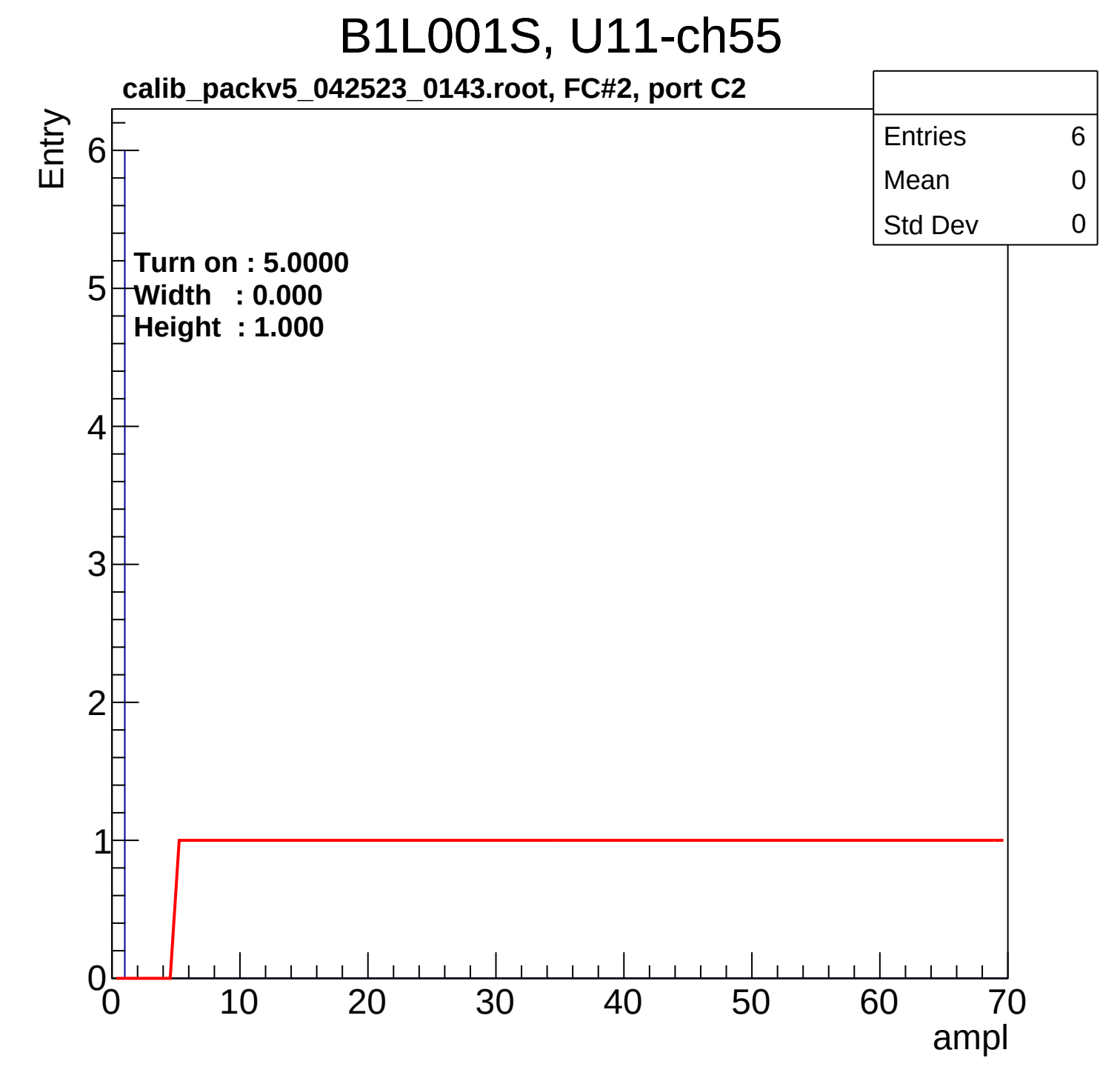

B1L001S, U11-ch50
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

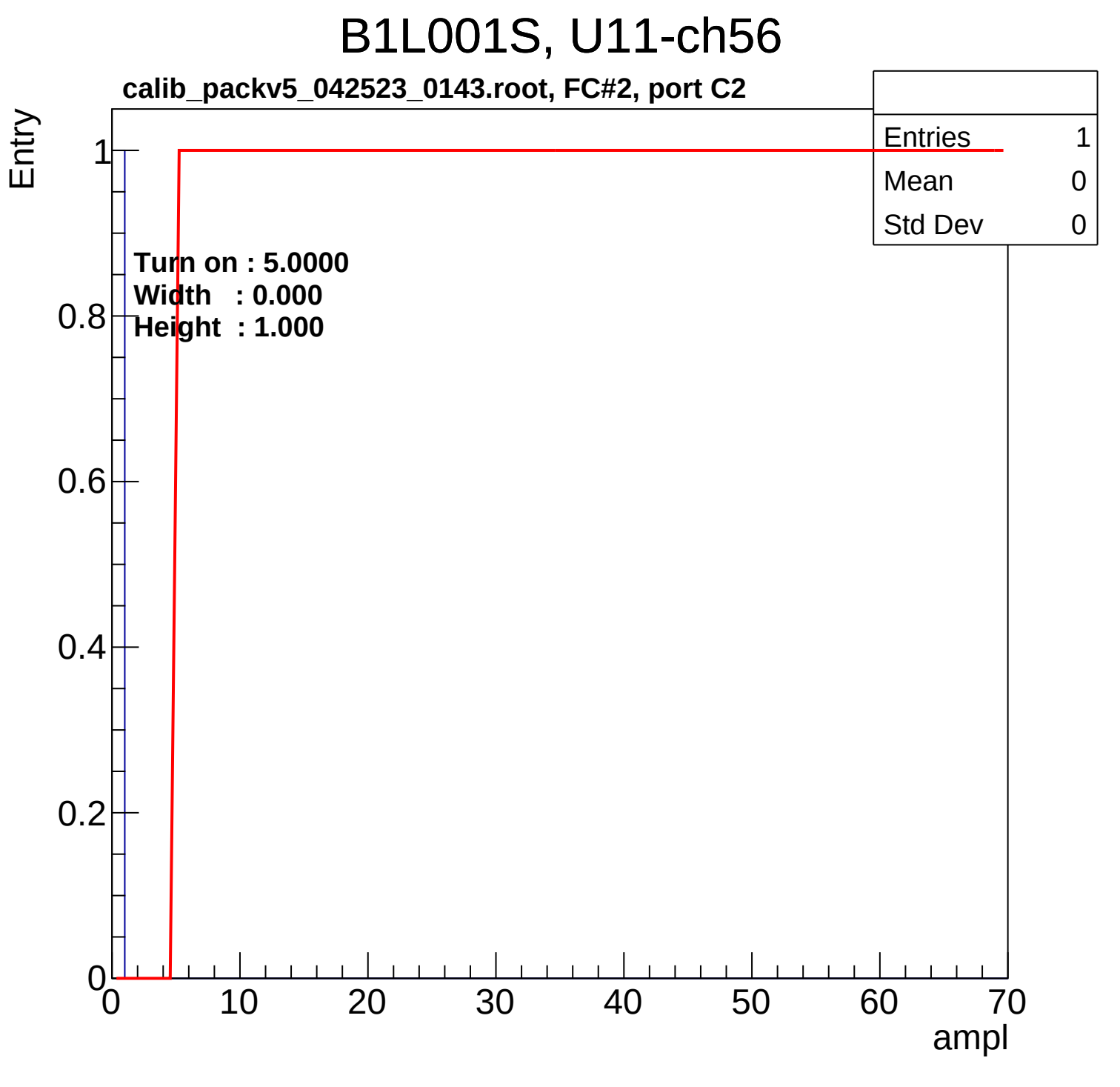

B1L001S, U11-ch51
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

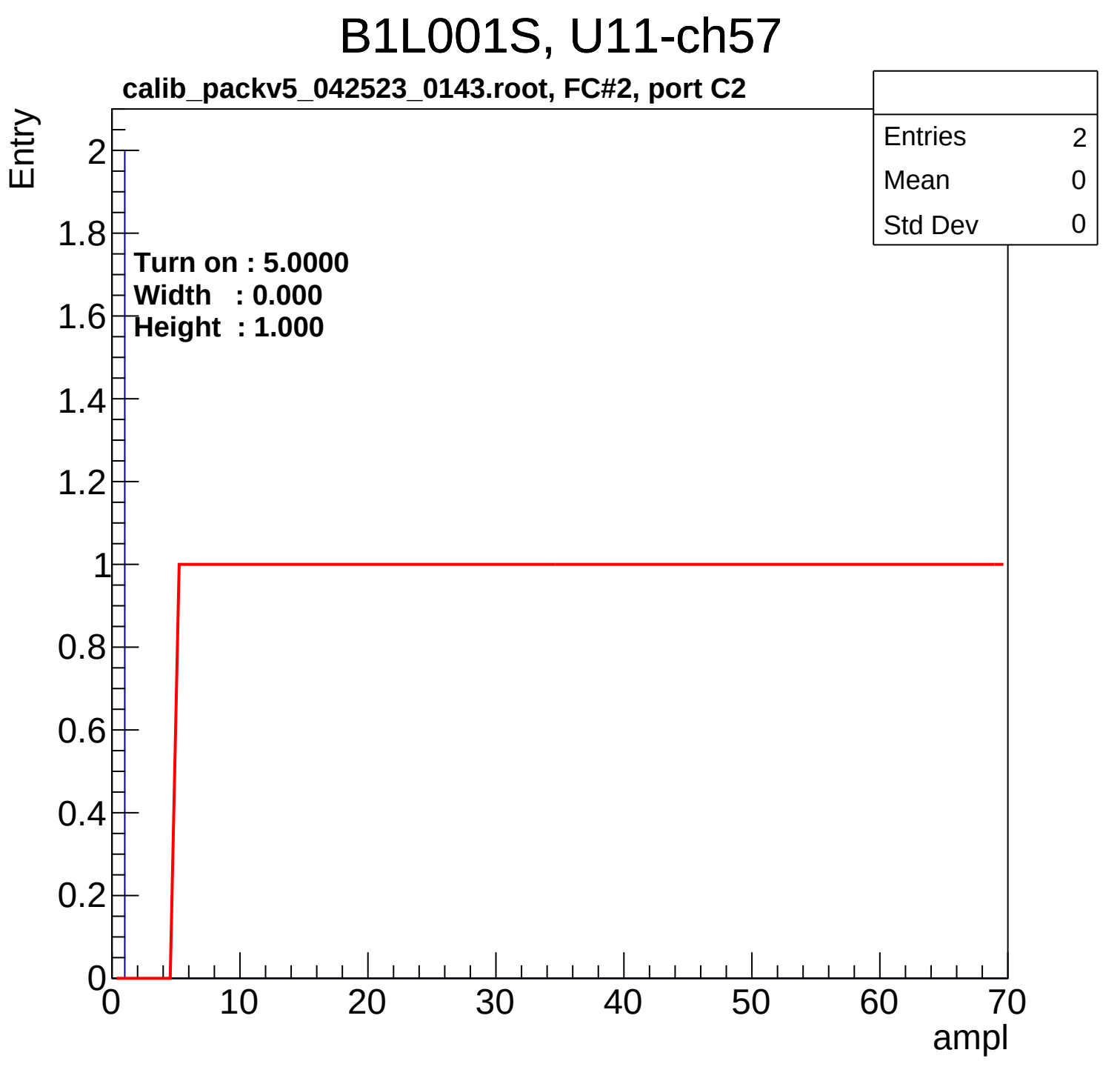

B1L001S, U11-ch52
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

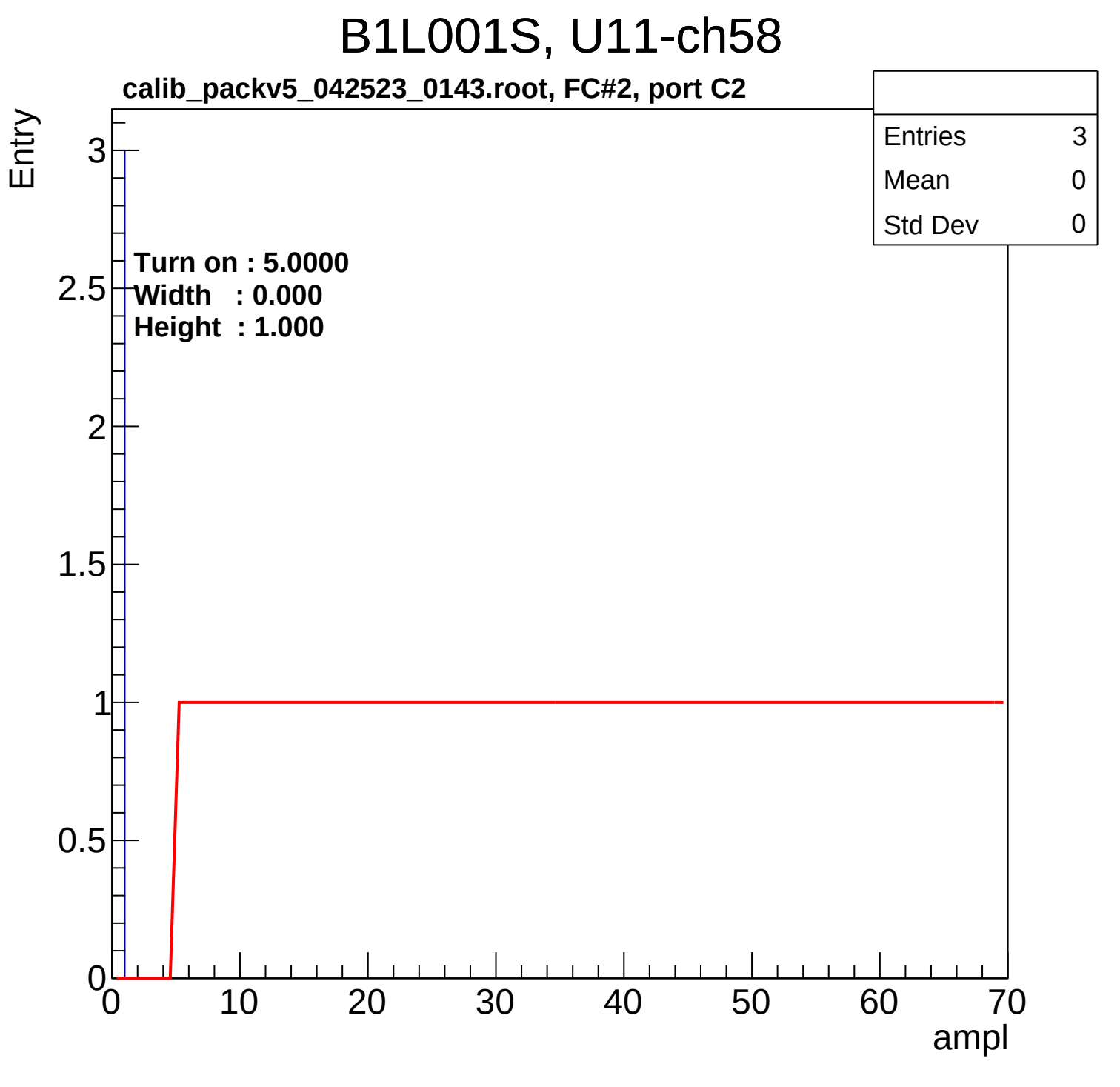

B1L001S, U11-ch53
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

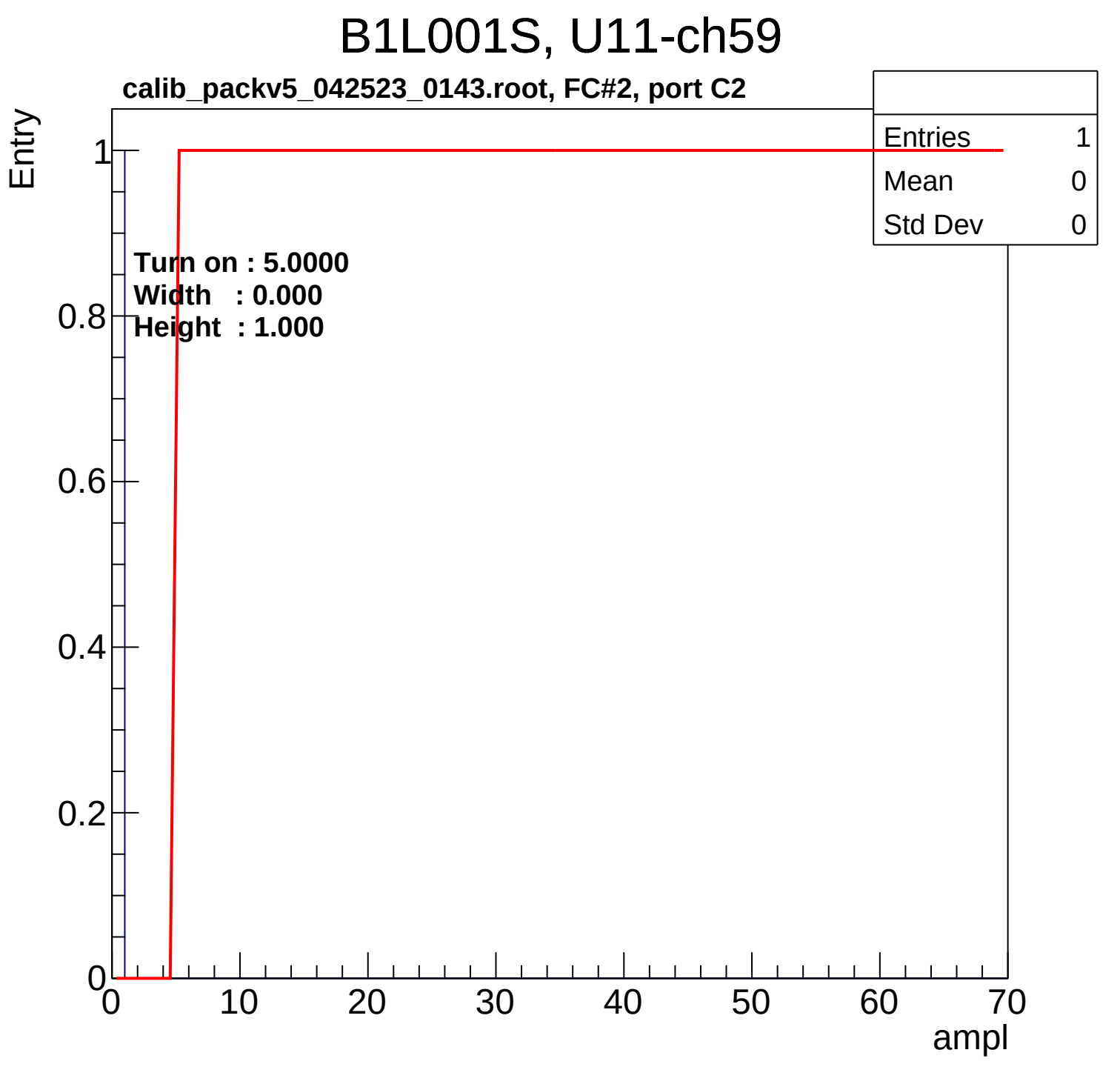

B1L001S, U11-ch54
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

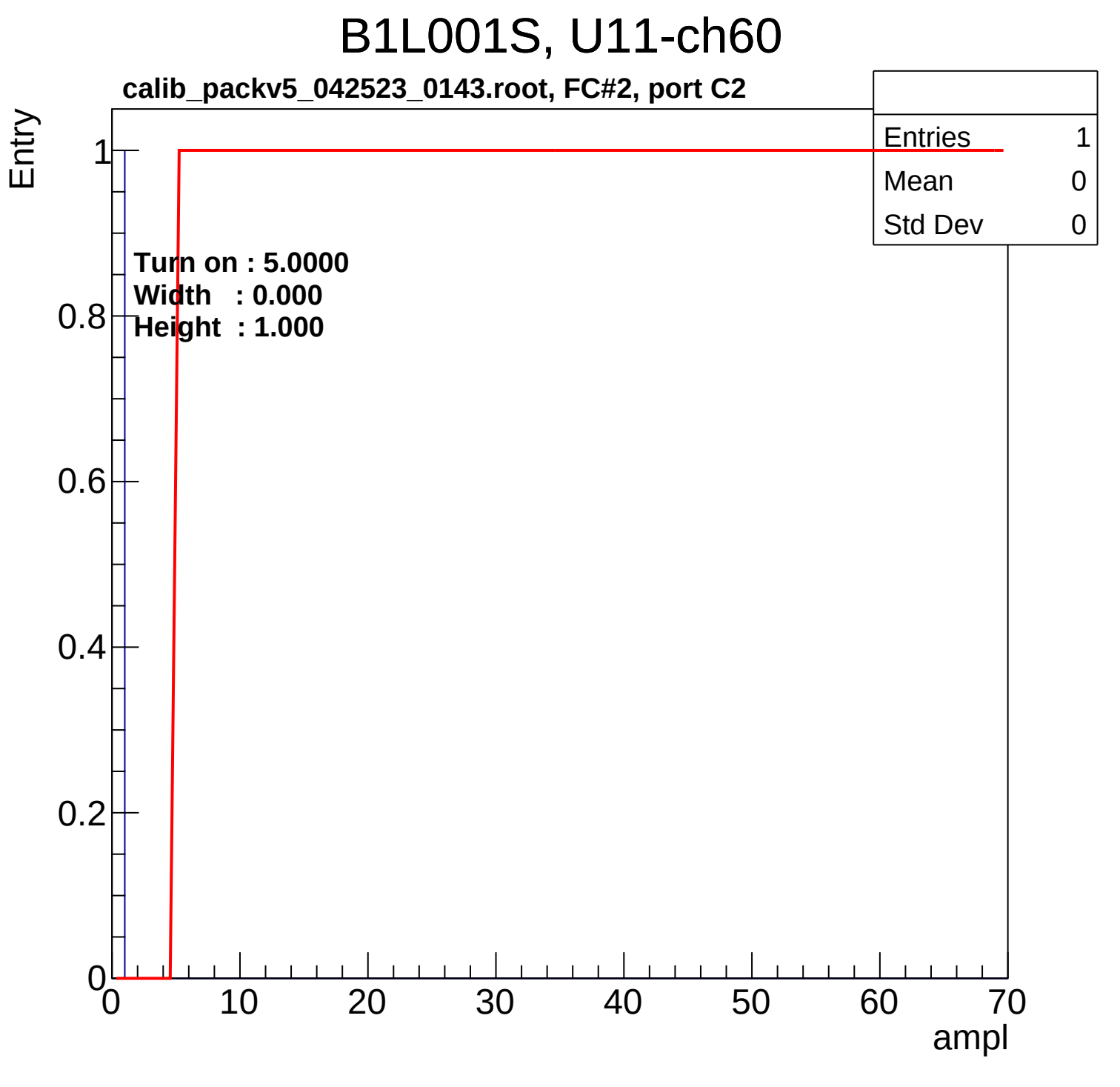

B1L001S, U11-ch55
calib_packv5_042523_0143.root, FC#2, port C2
Entries 6
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

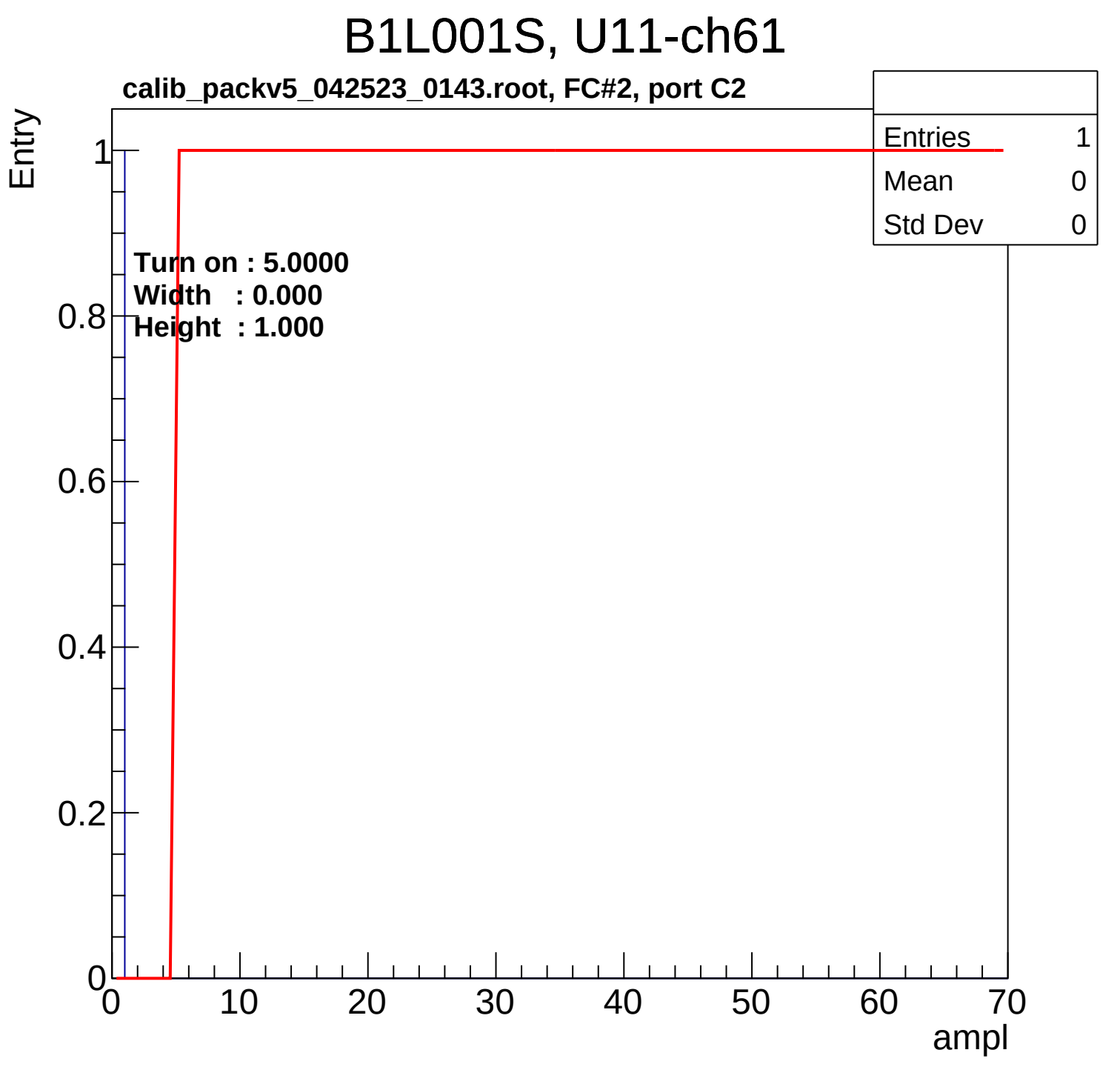

B1L001S, U11-ch56
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

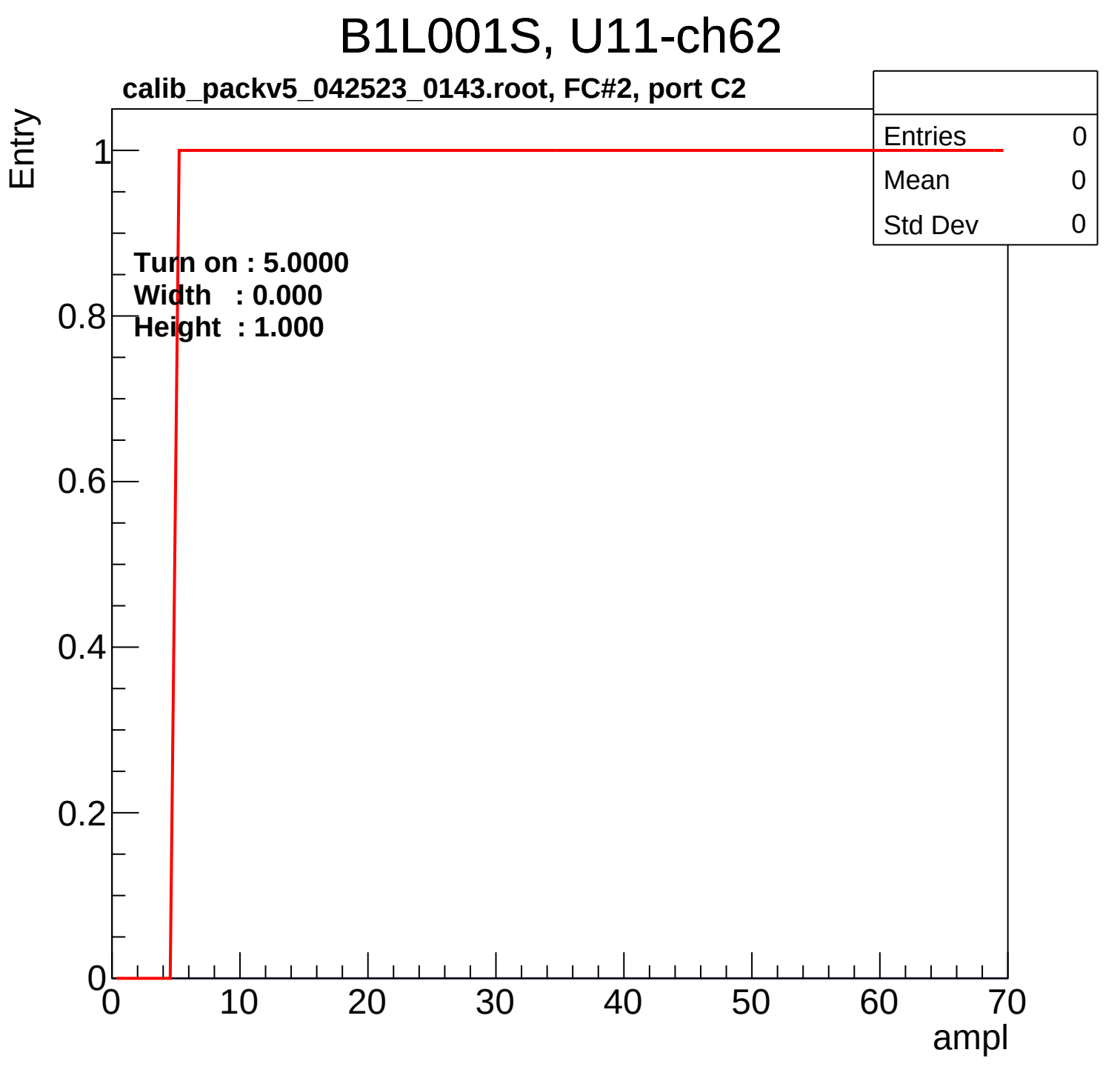

B1L001S, U11-ch57
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

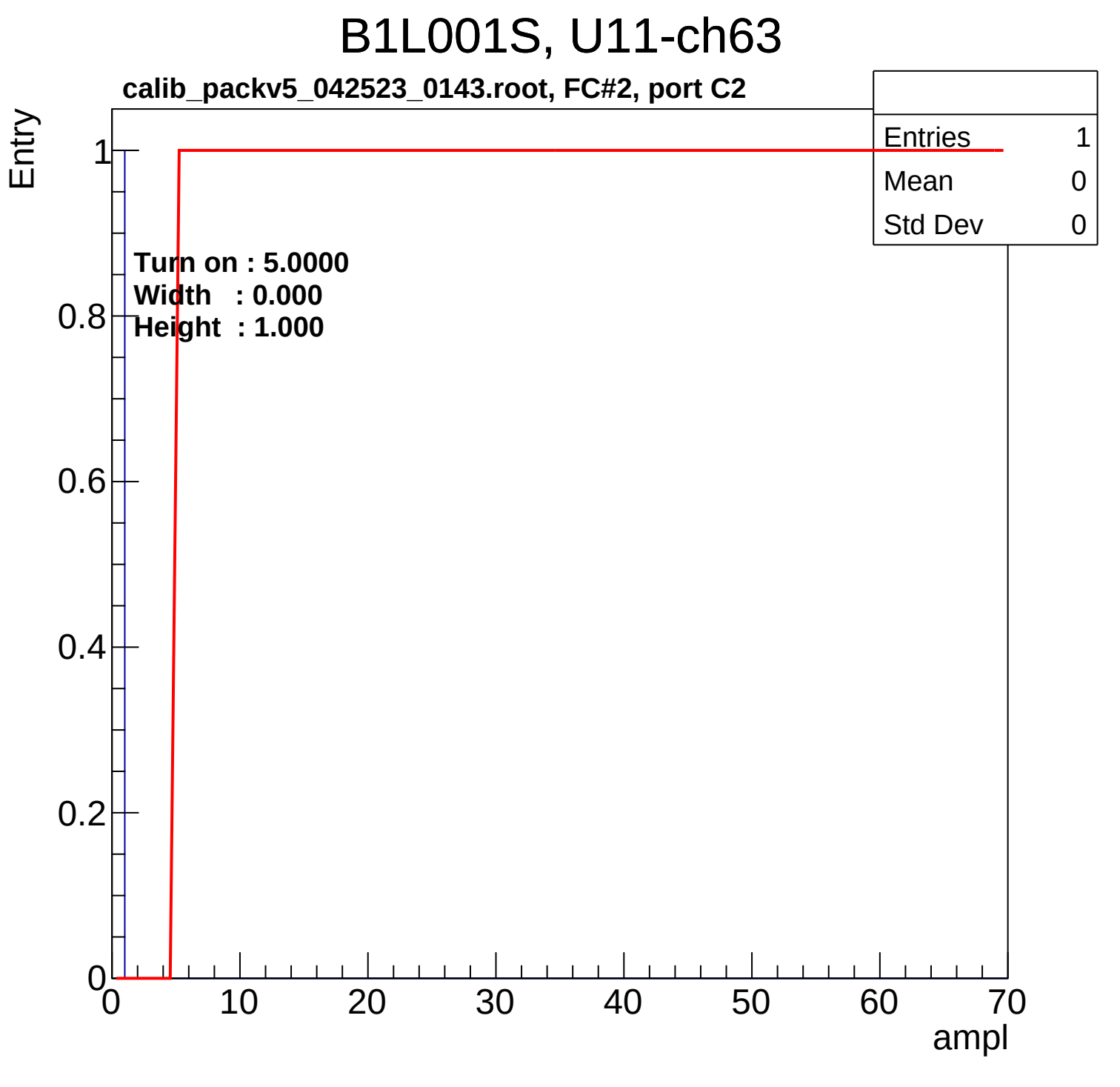

B1L001S, U11-ch58
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

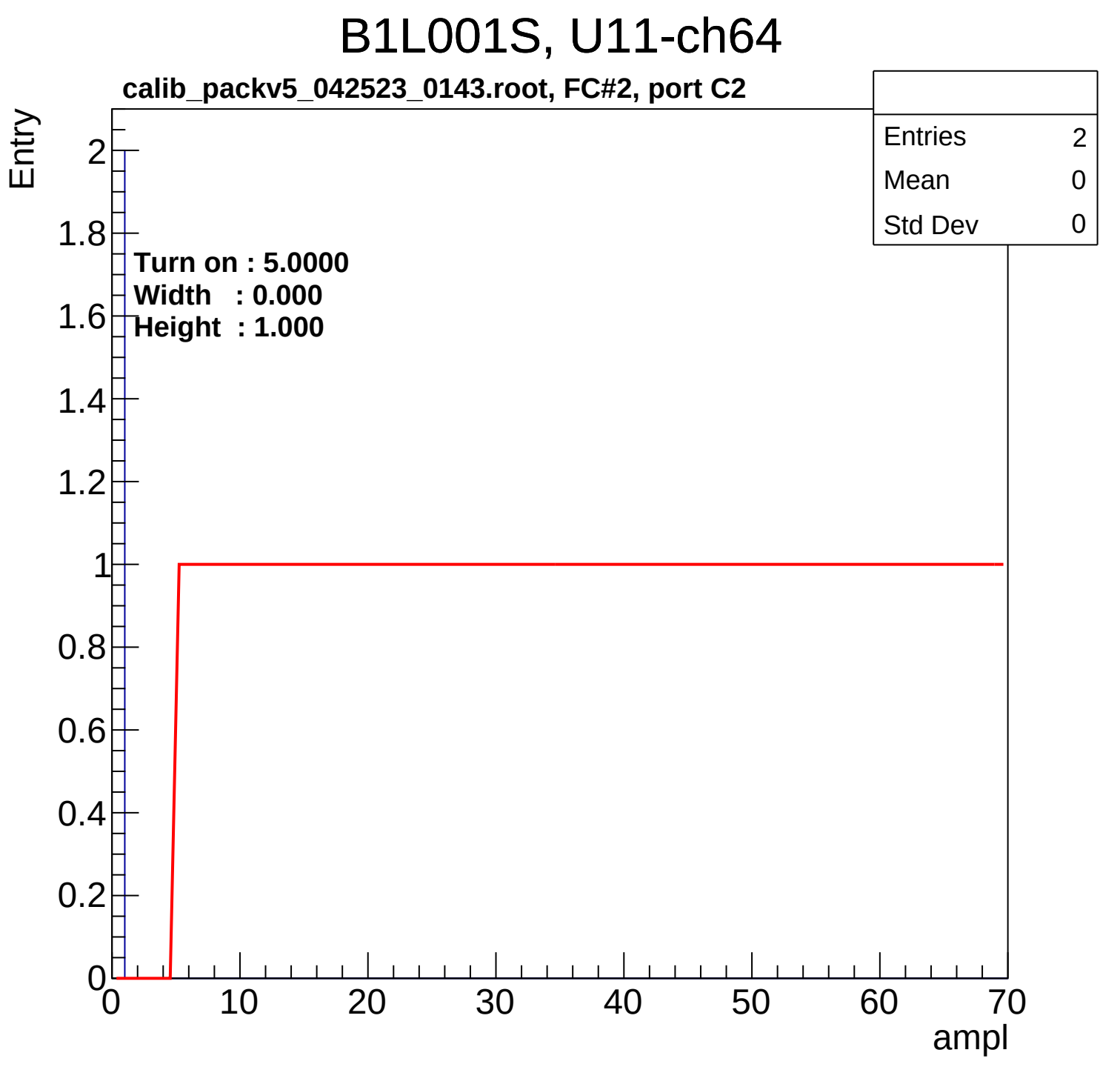

B1L001S, U11-ch59
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

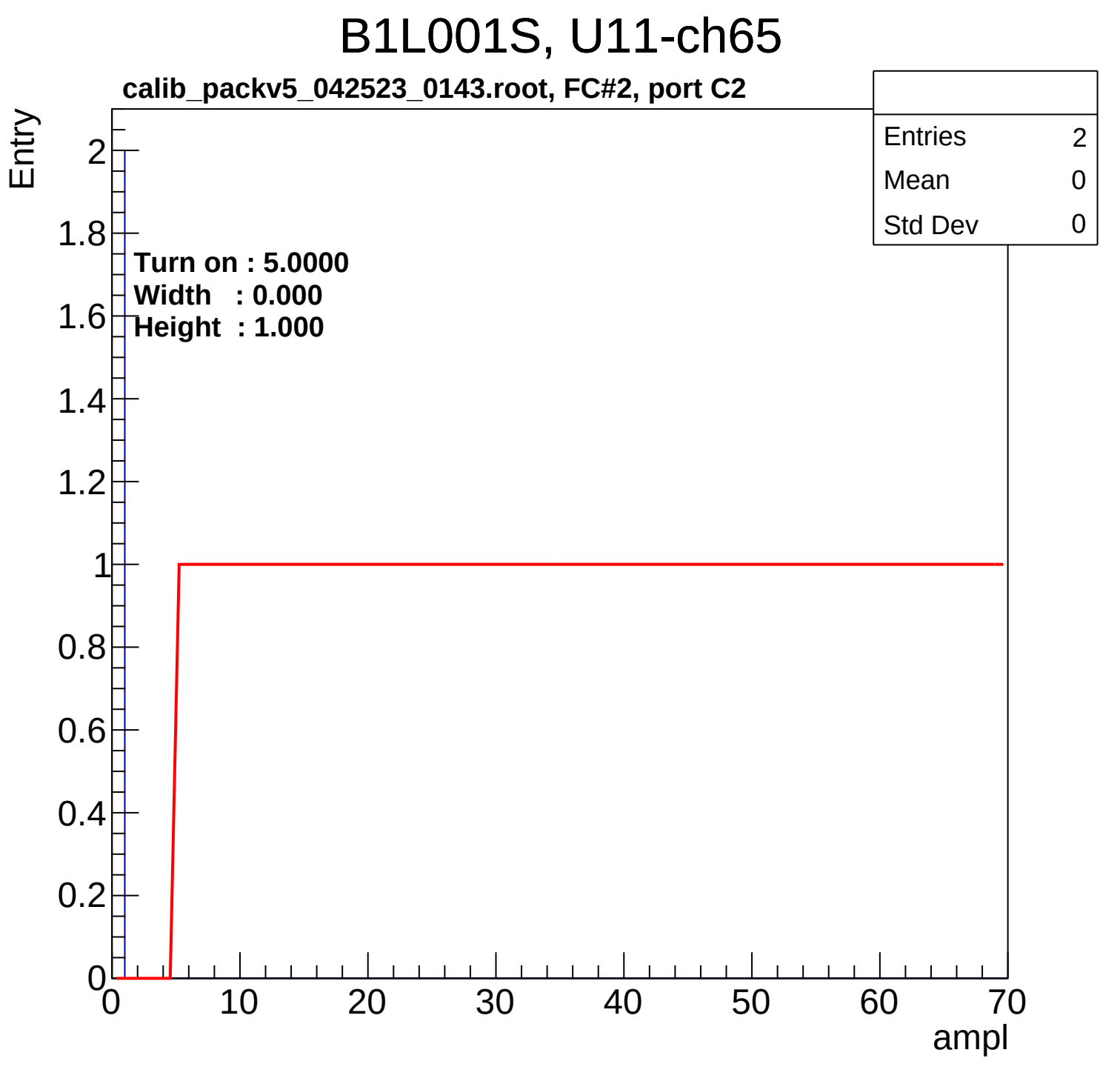

B1L001S, U11-ch60
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

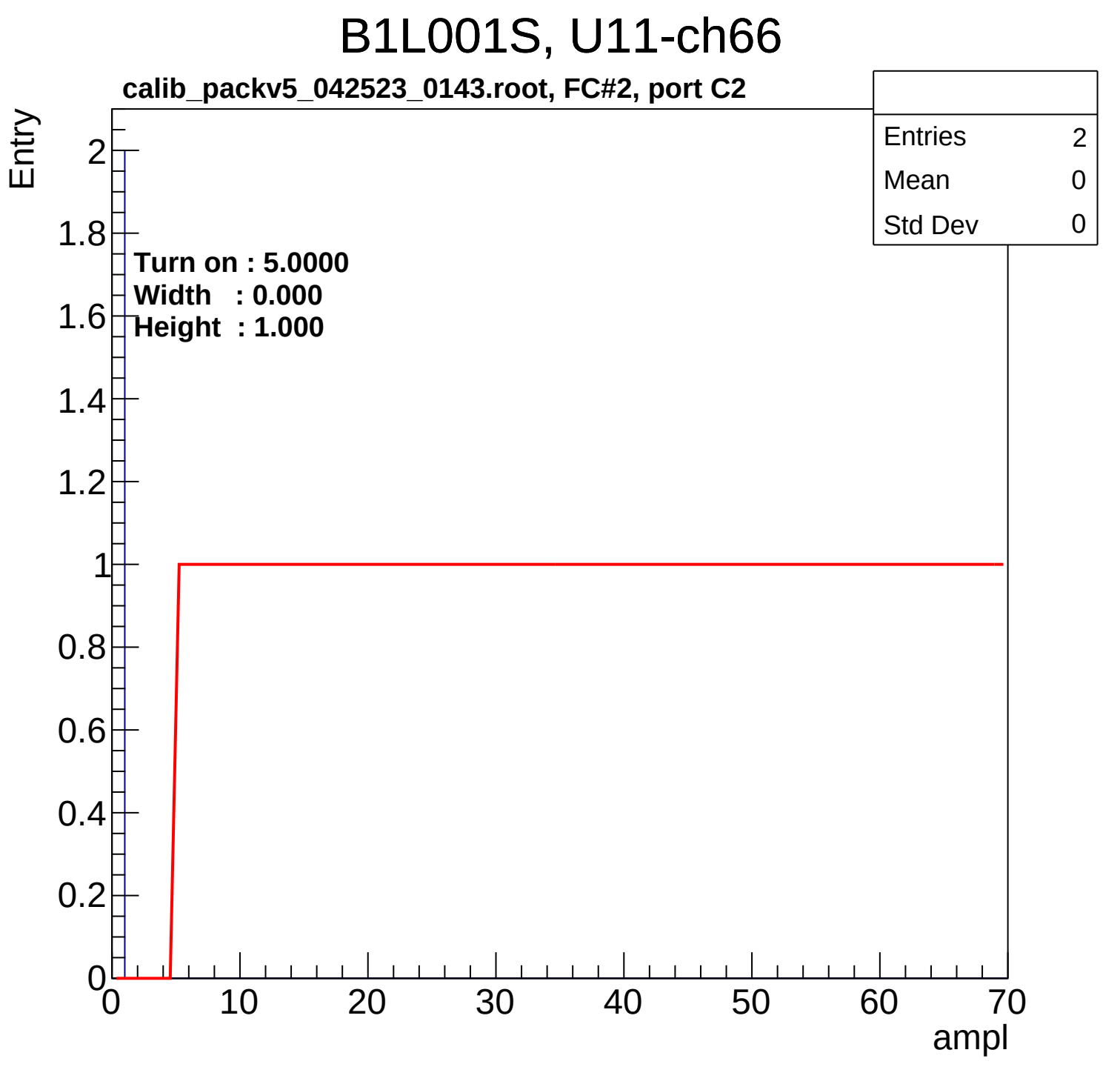

B1L001S, U11-ch61
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

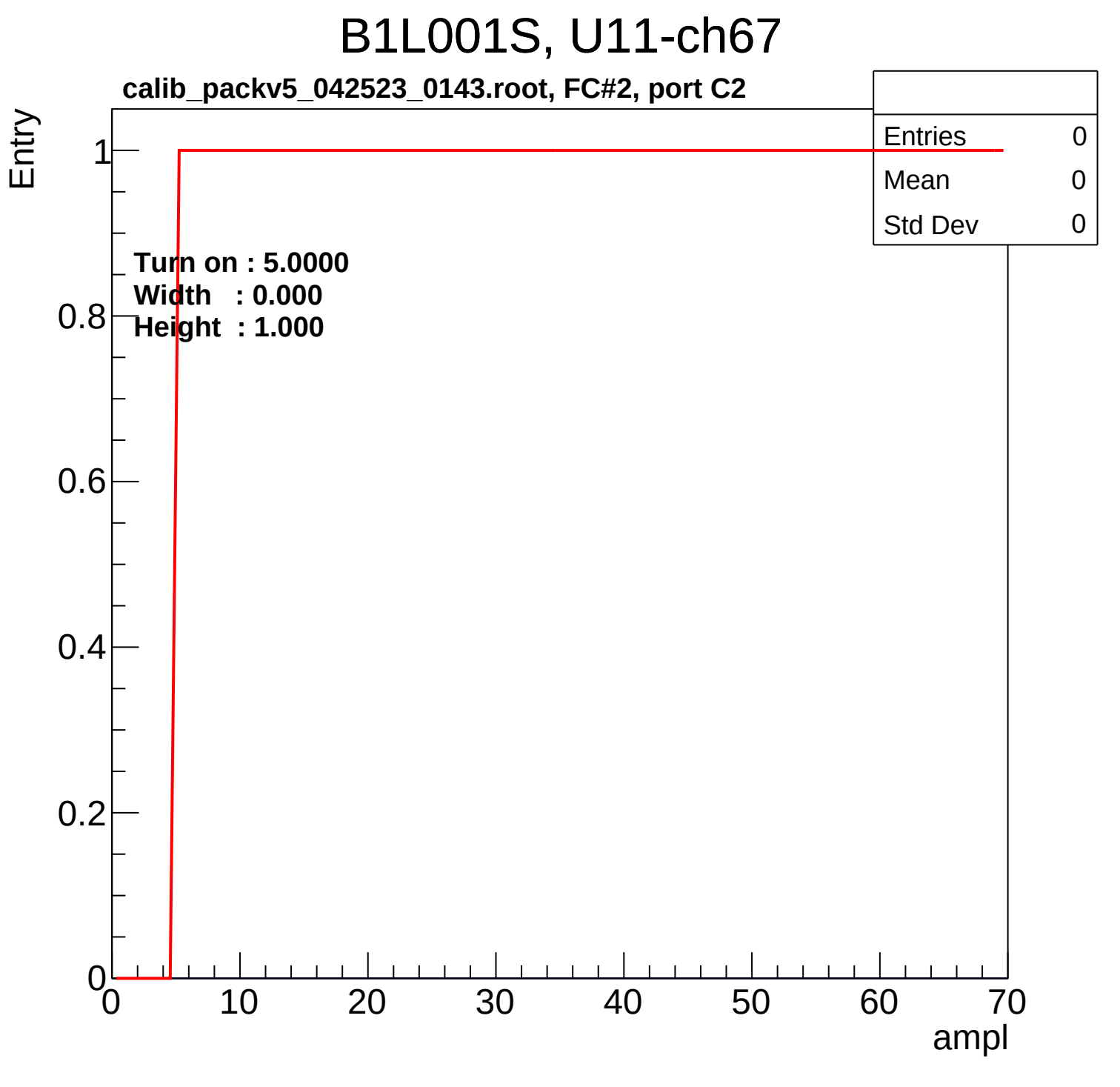

B1L001S, U11-ch62
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

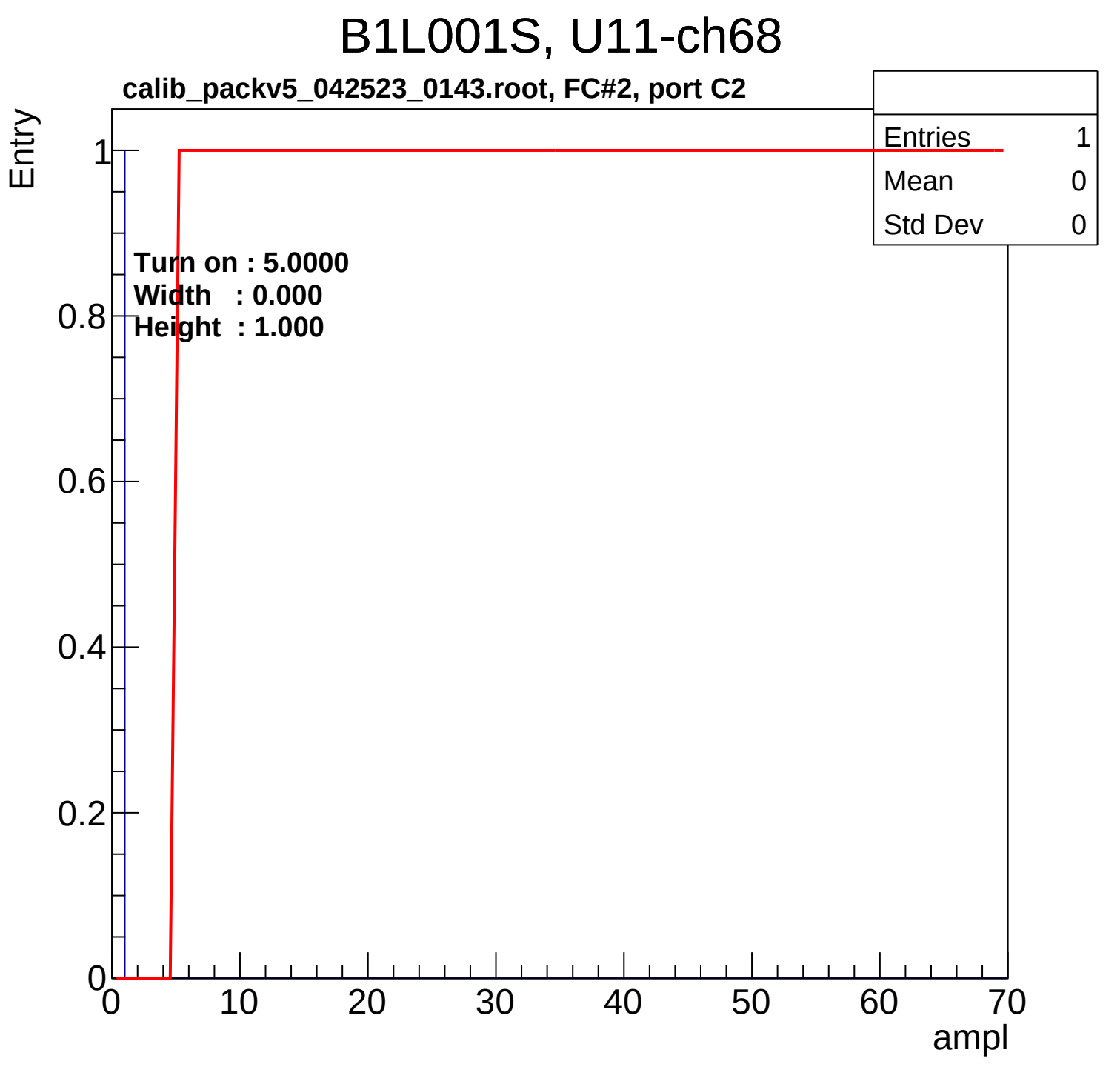

B1L001S, U11-ch63
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

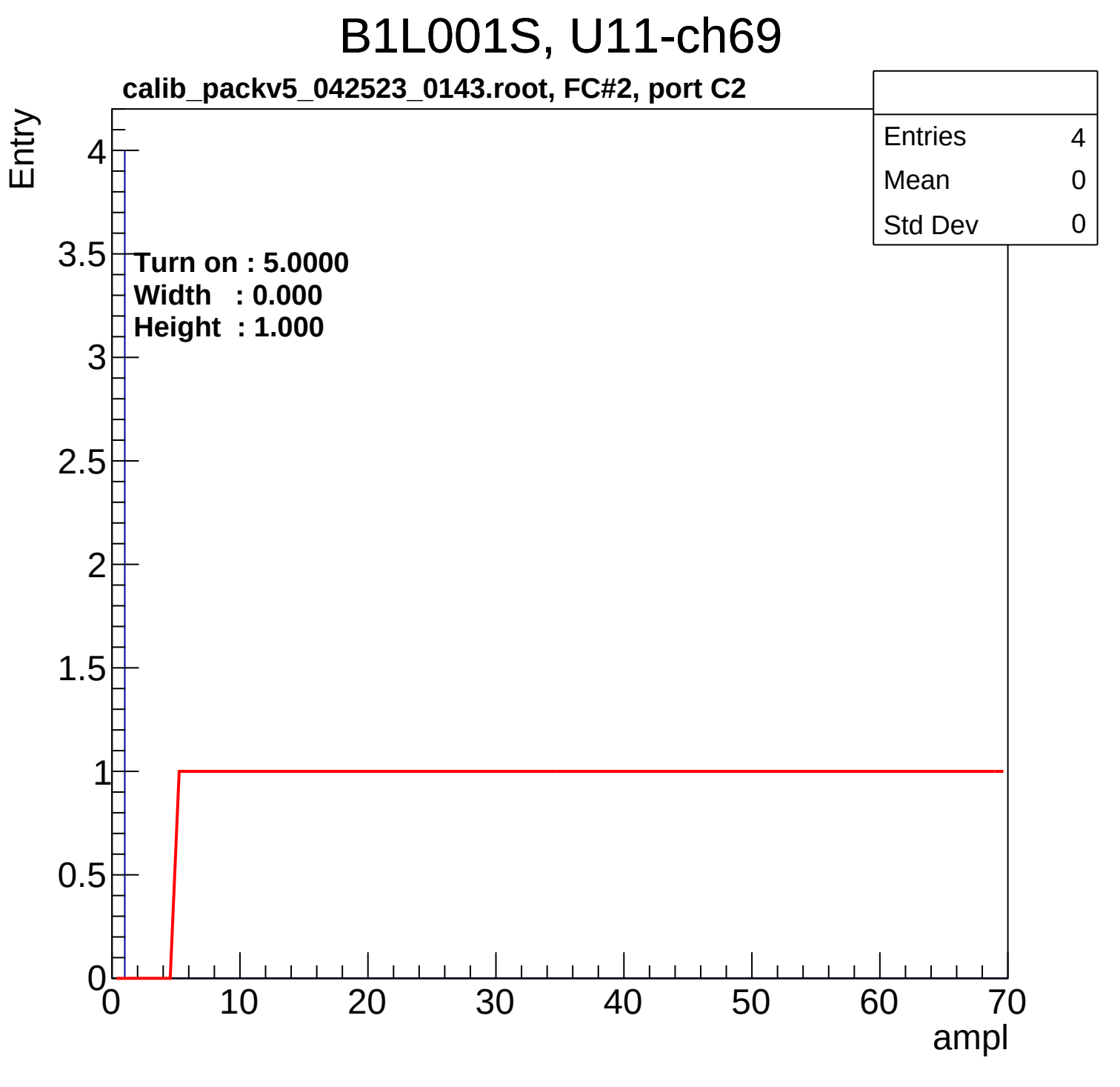

B1L001S, U11-ch64
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

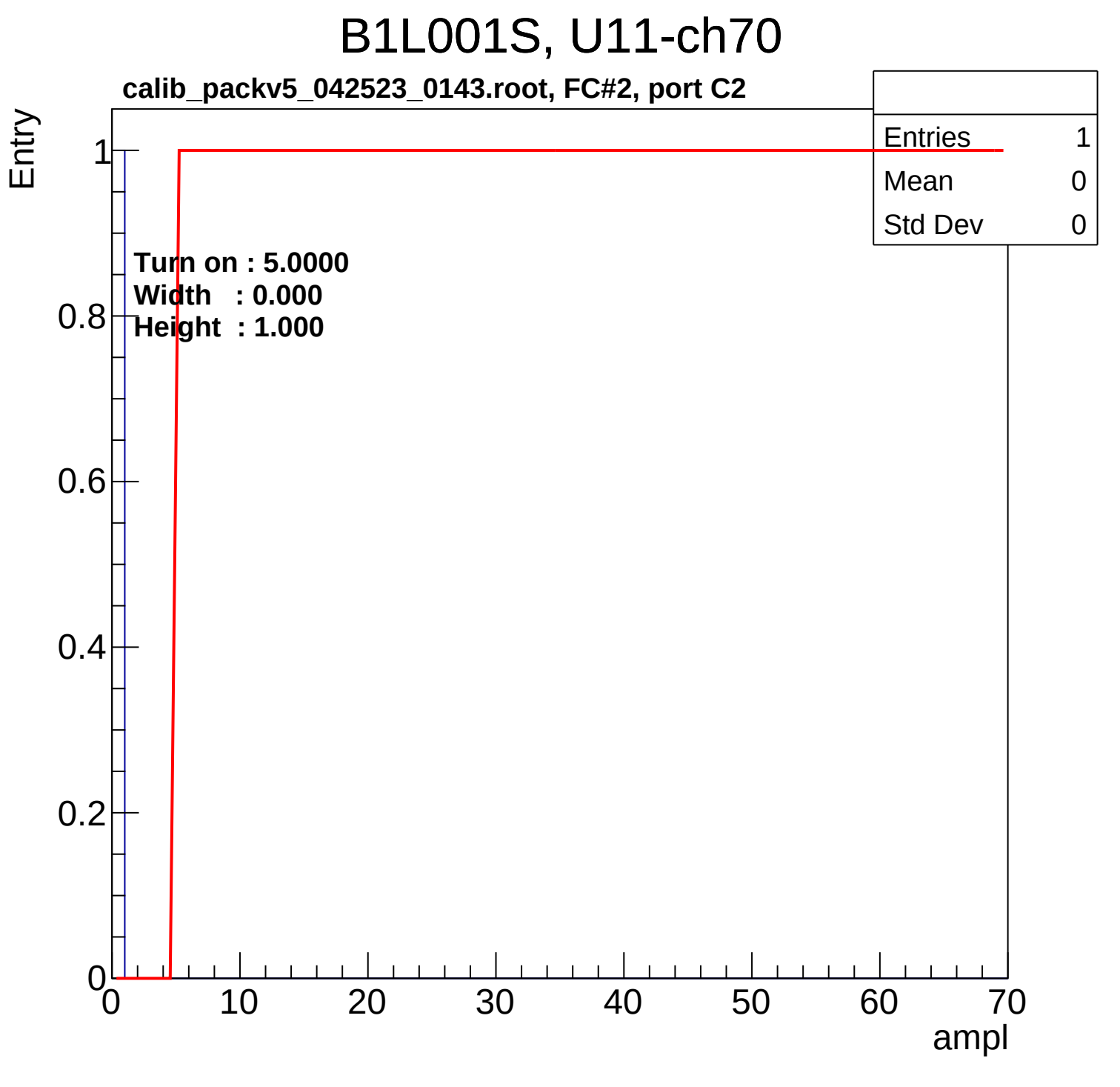

B1L001S, U11-ch65
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

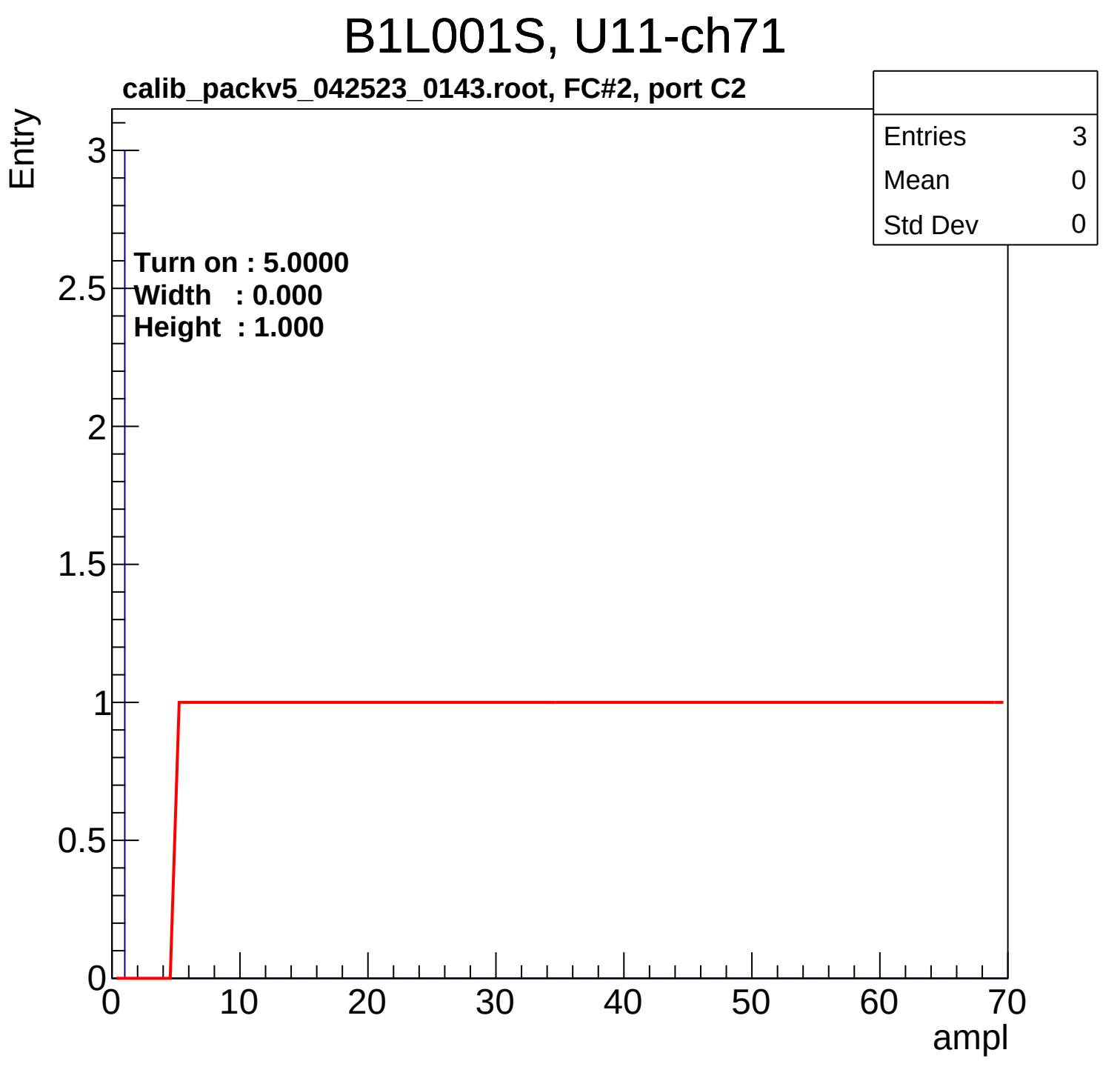

B1L001S, U11-ch66
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

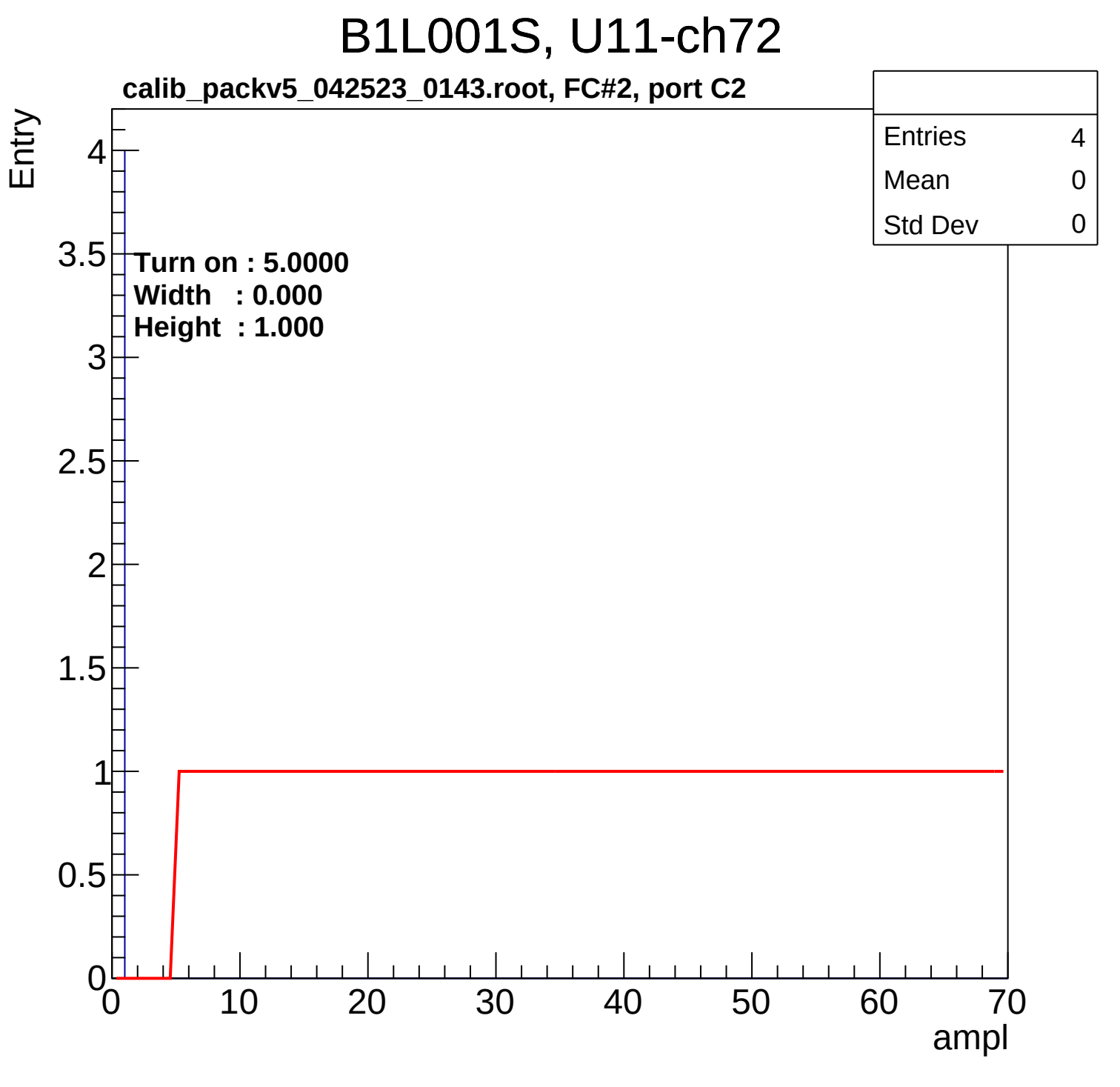

B1L001S, U11-ch67
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

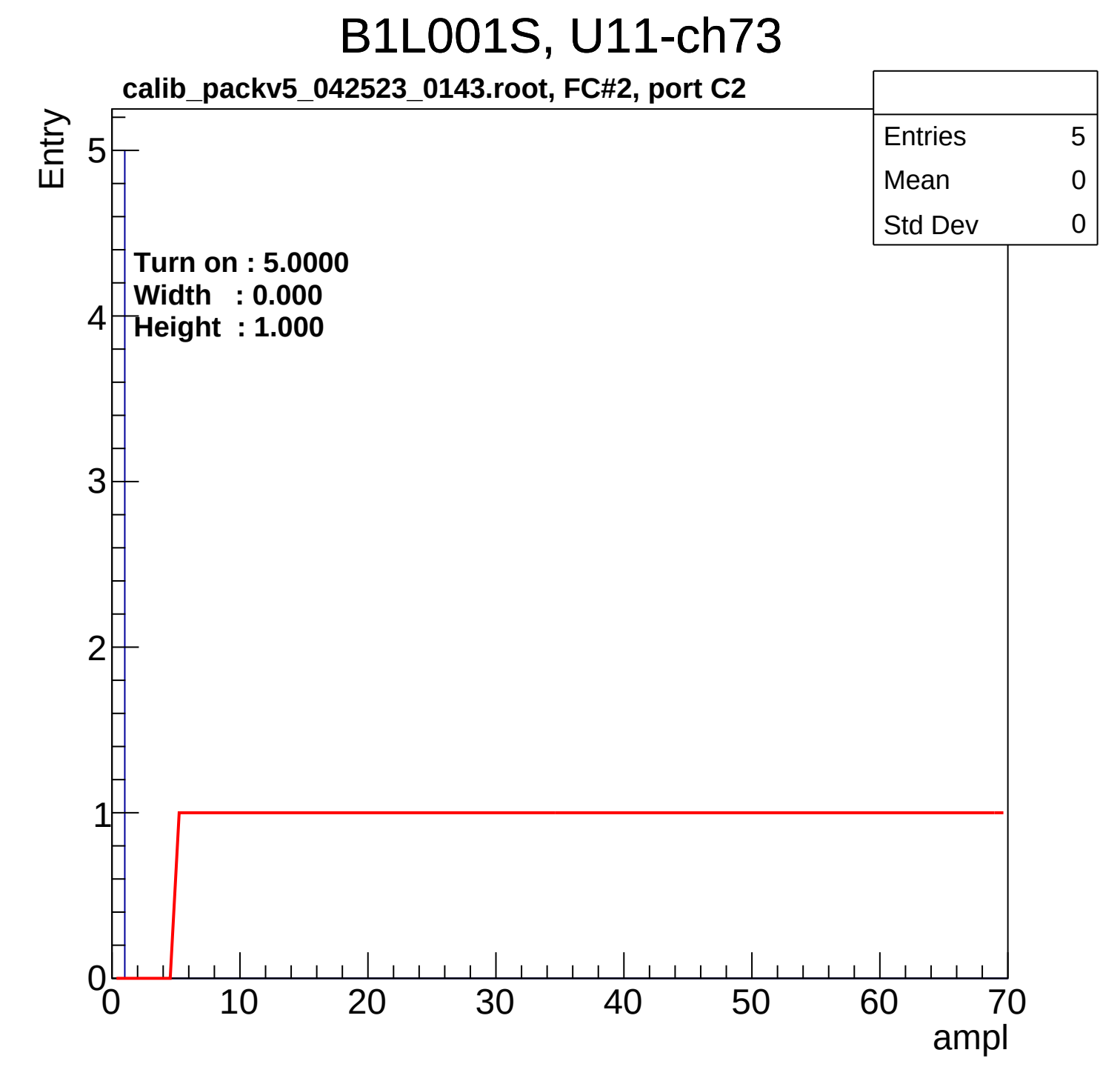

B1L001S, U11-ch68
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

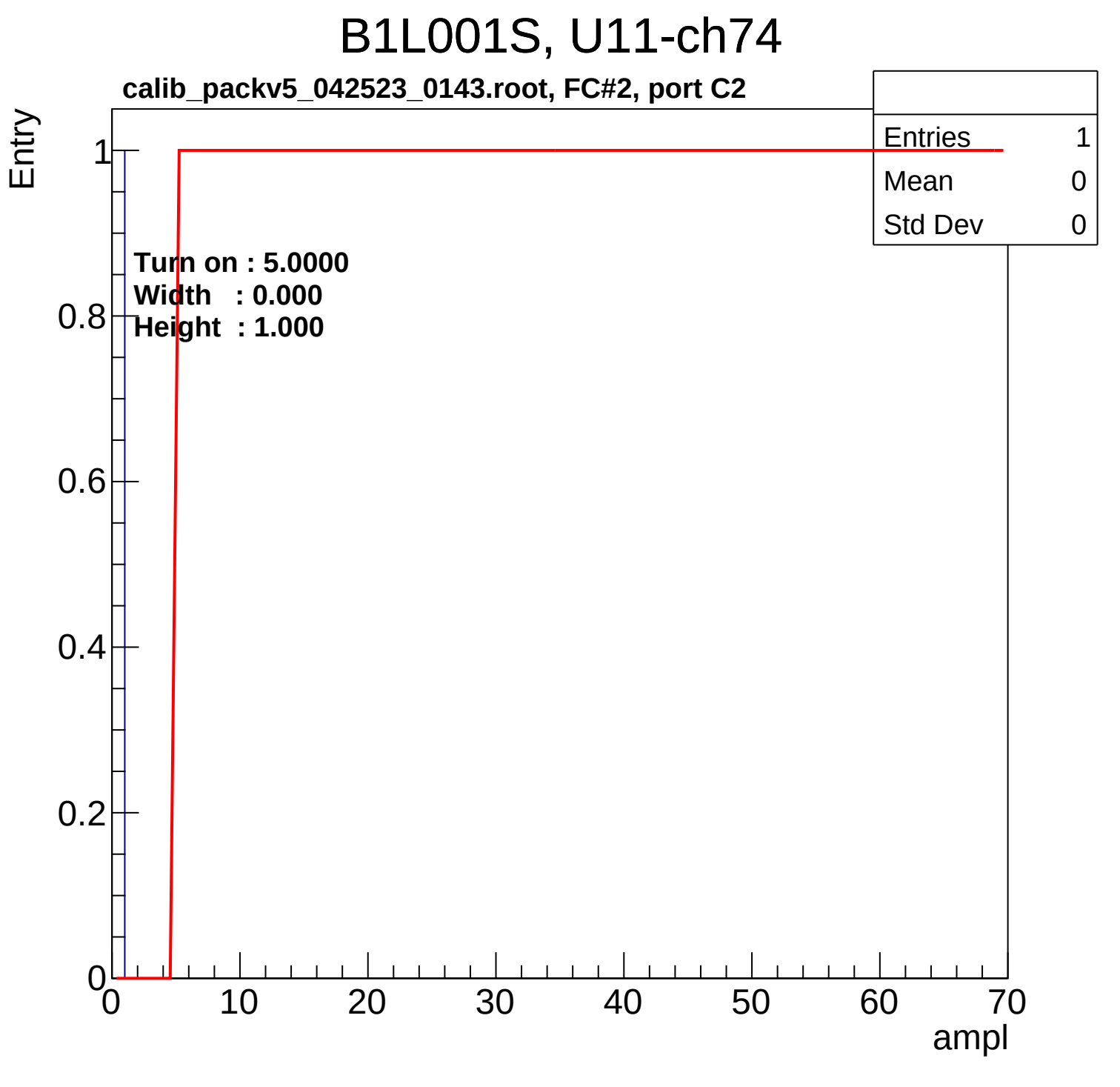

B1L001S, U11-ch69
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

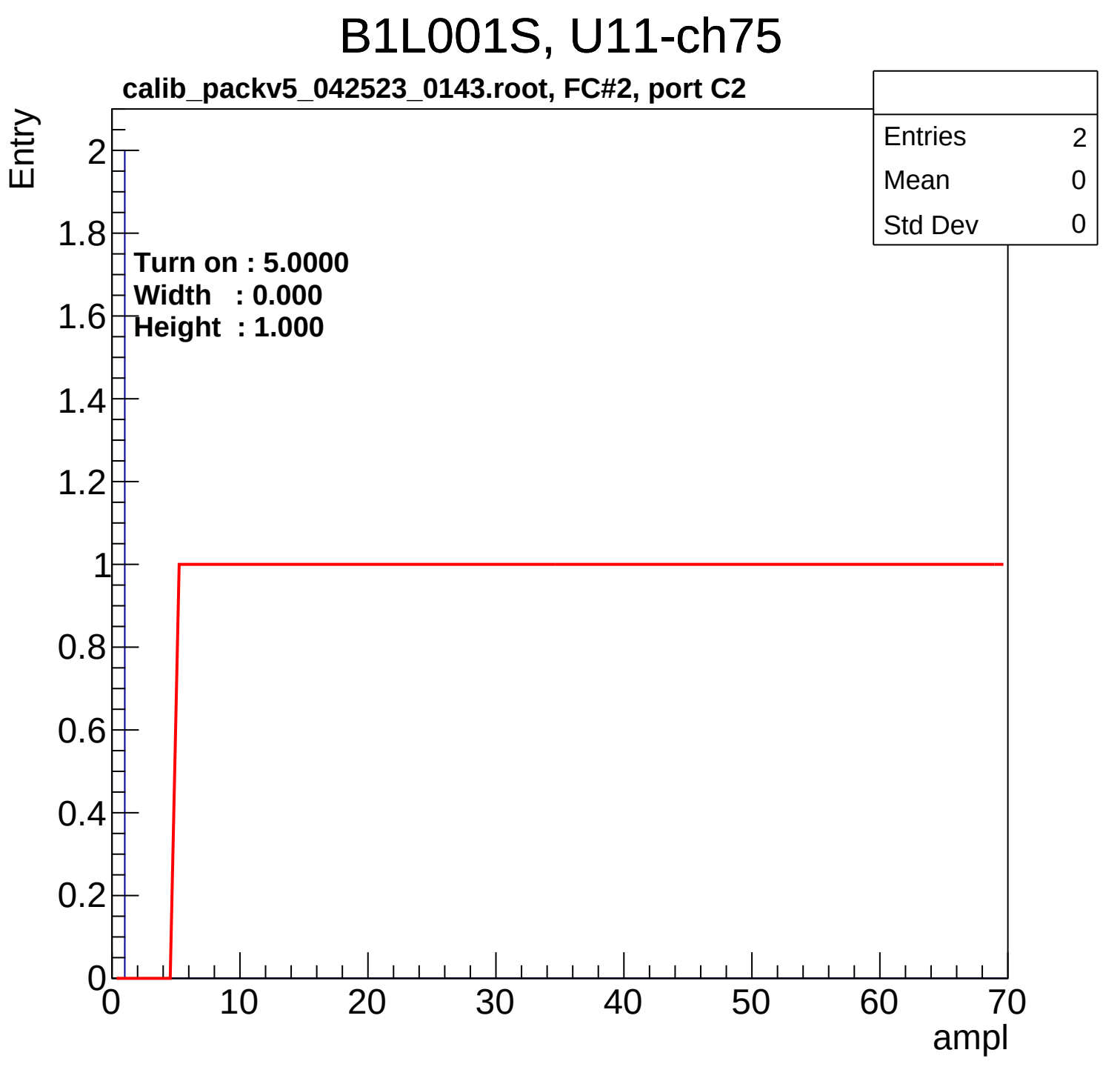

B1L001S, U11-ch70
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

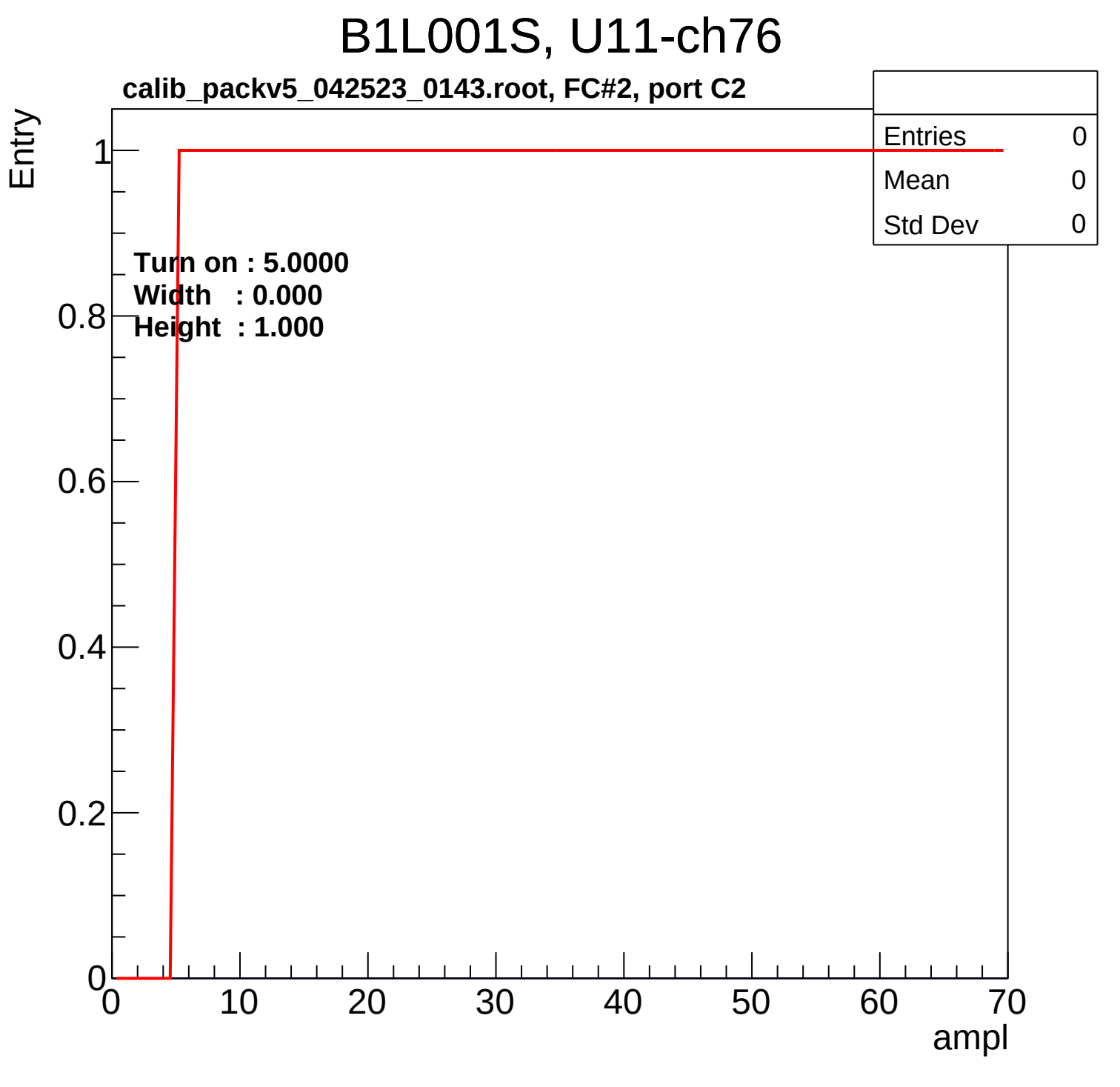

B1L001S, U11-ch71
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

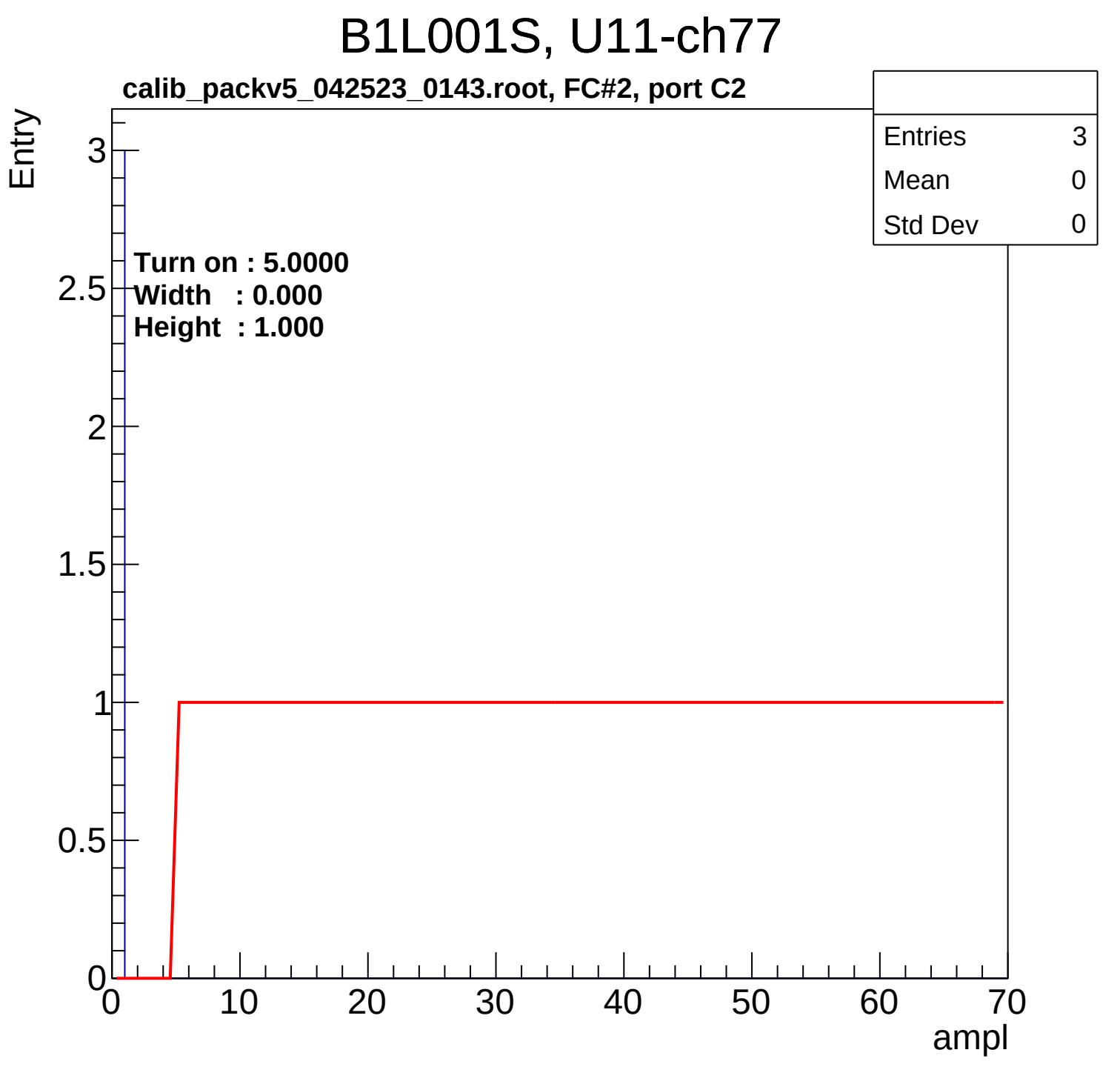

B1L001S, U11-ch72
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

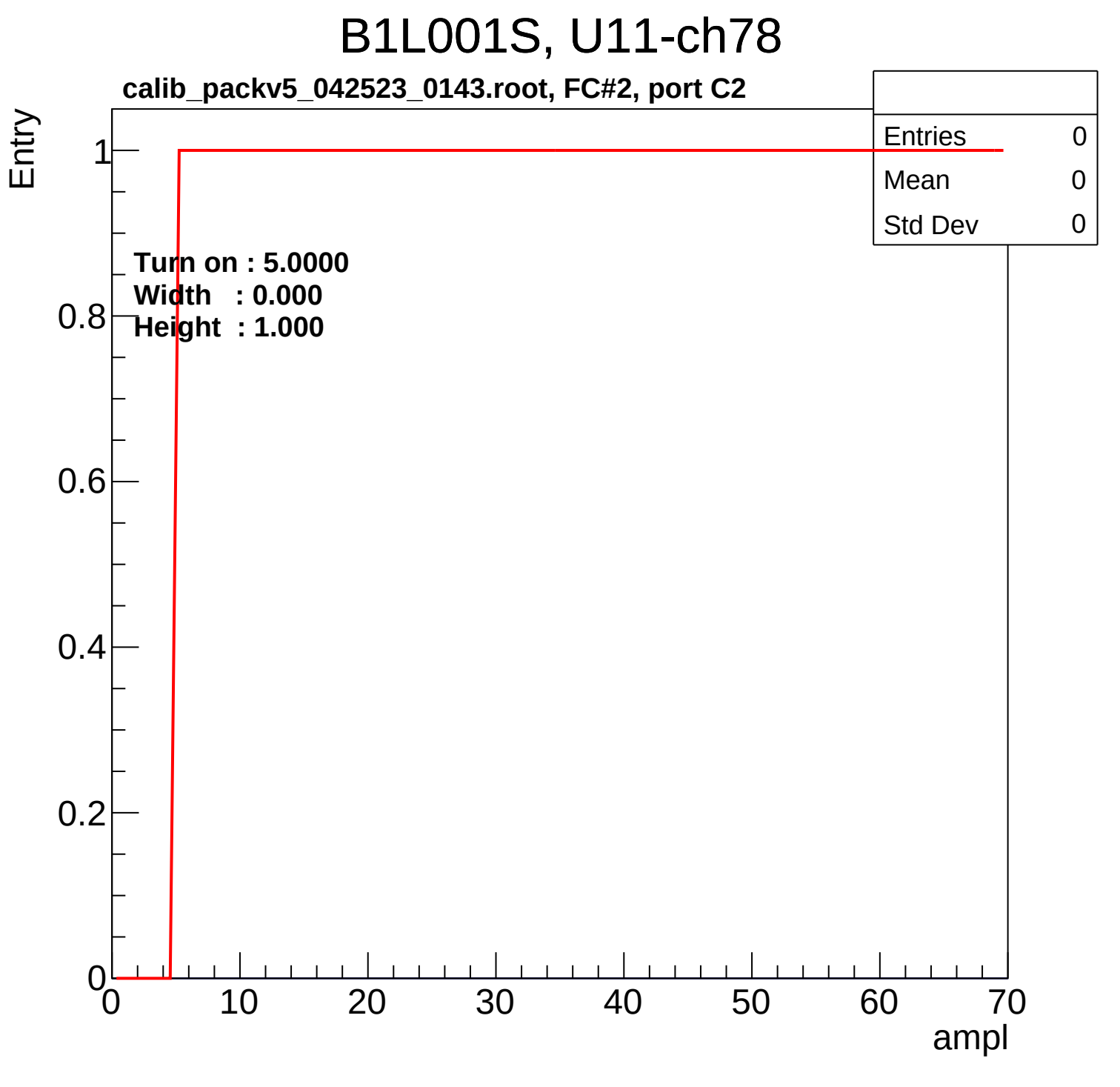

B1L001S, U11-ch73
calib_packv5_042523_0143.root, FC#2, port C2
Entries 5
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

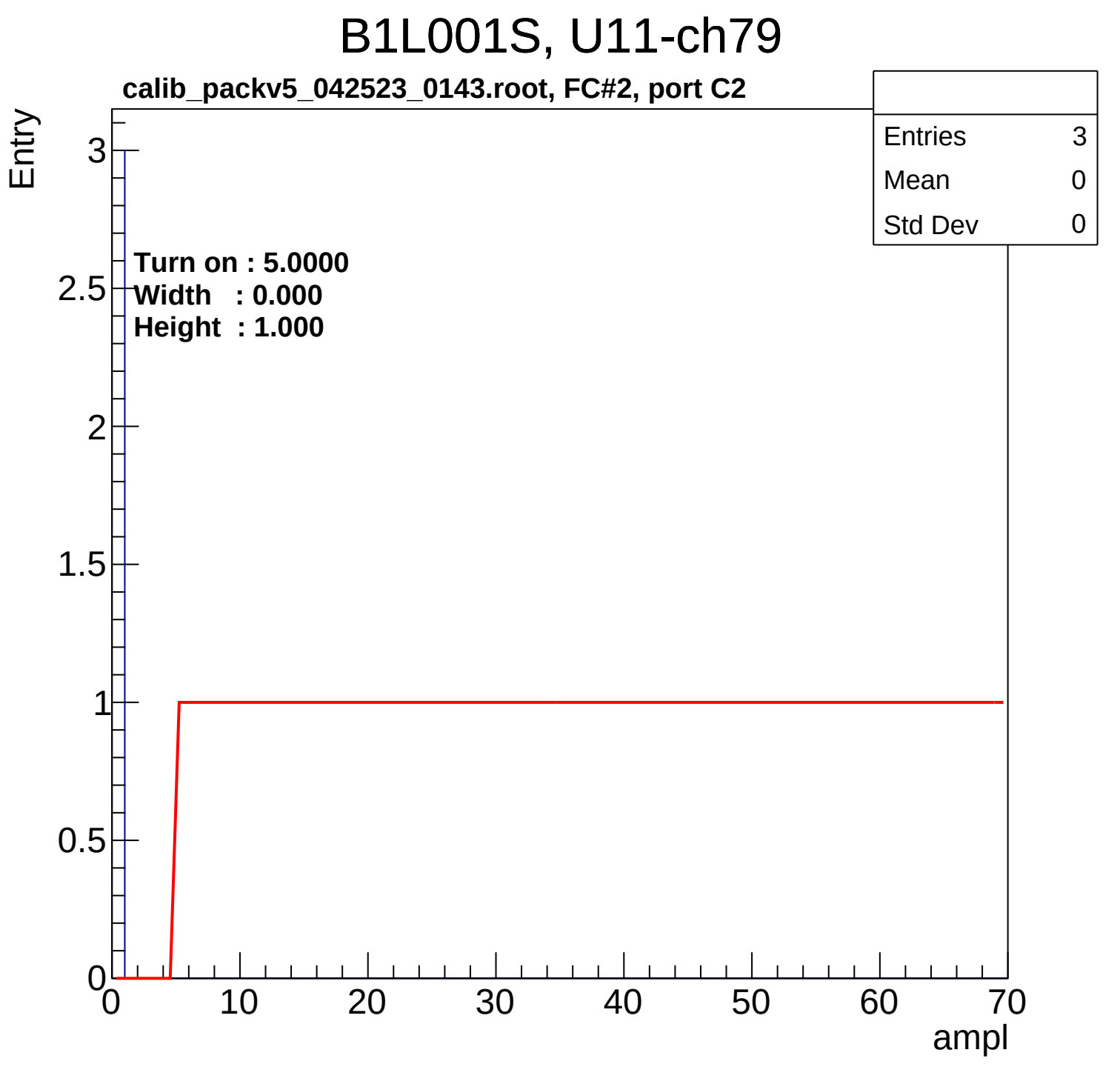

B1L001S, U11-ch74
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

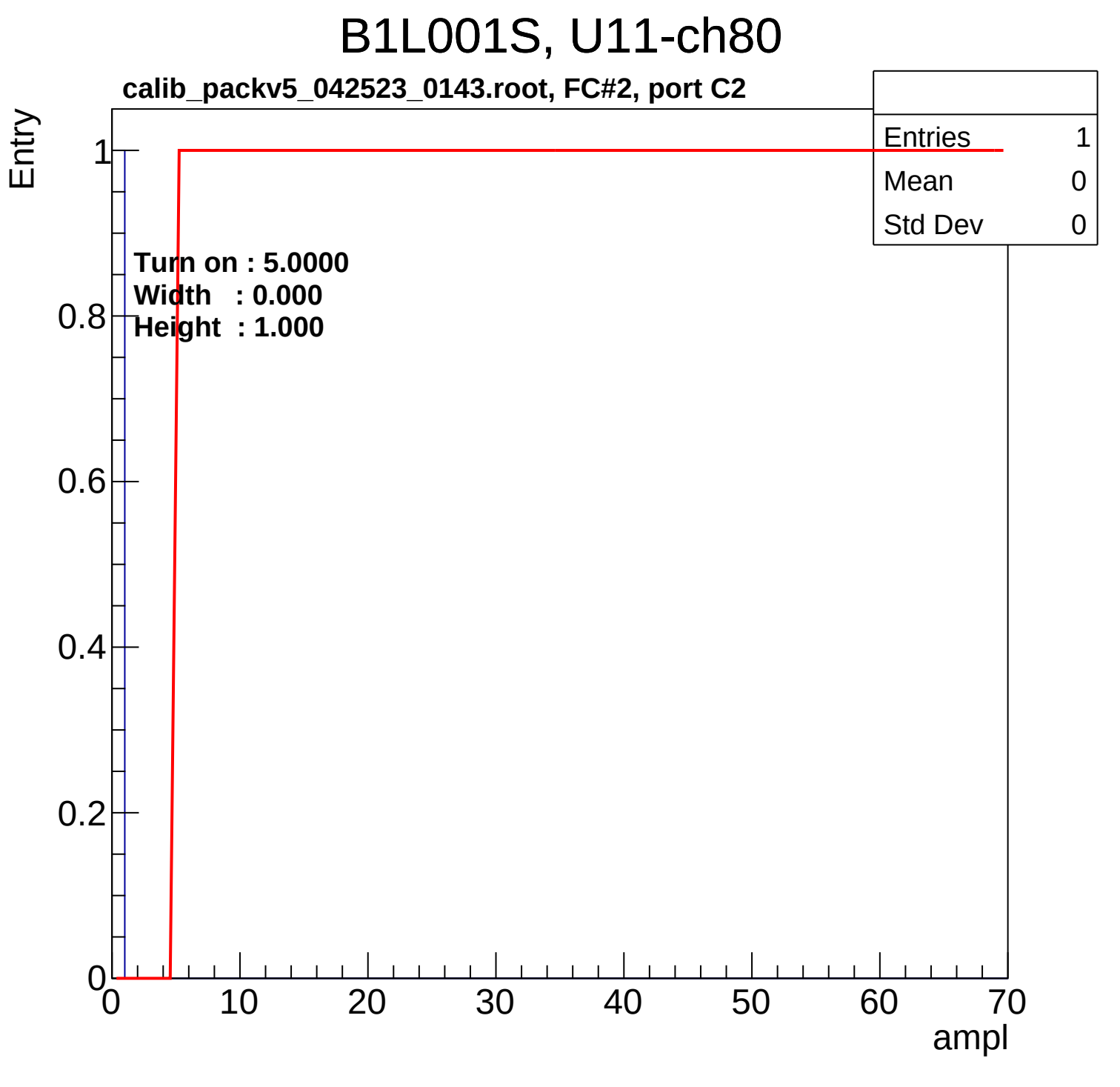

B1L001S, U11-ch75
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

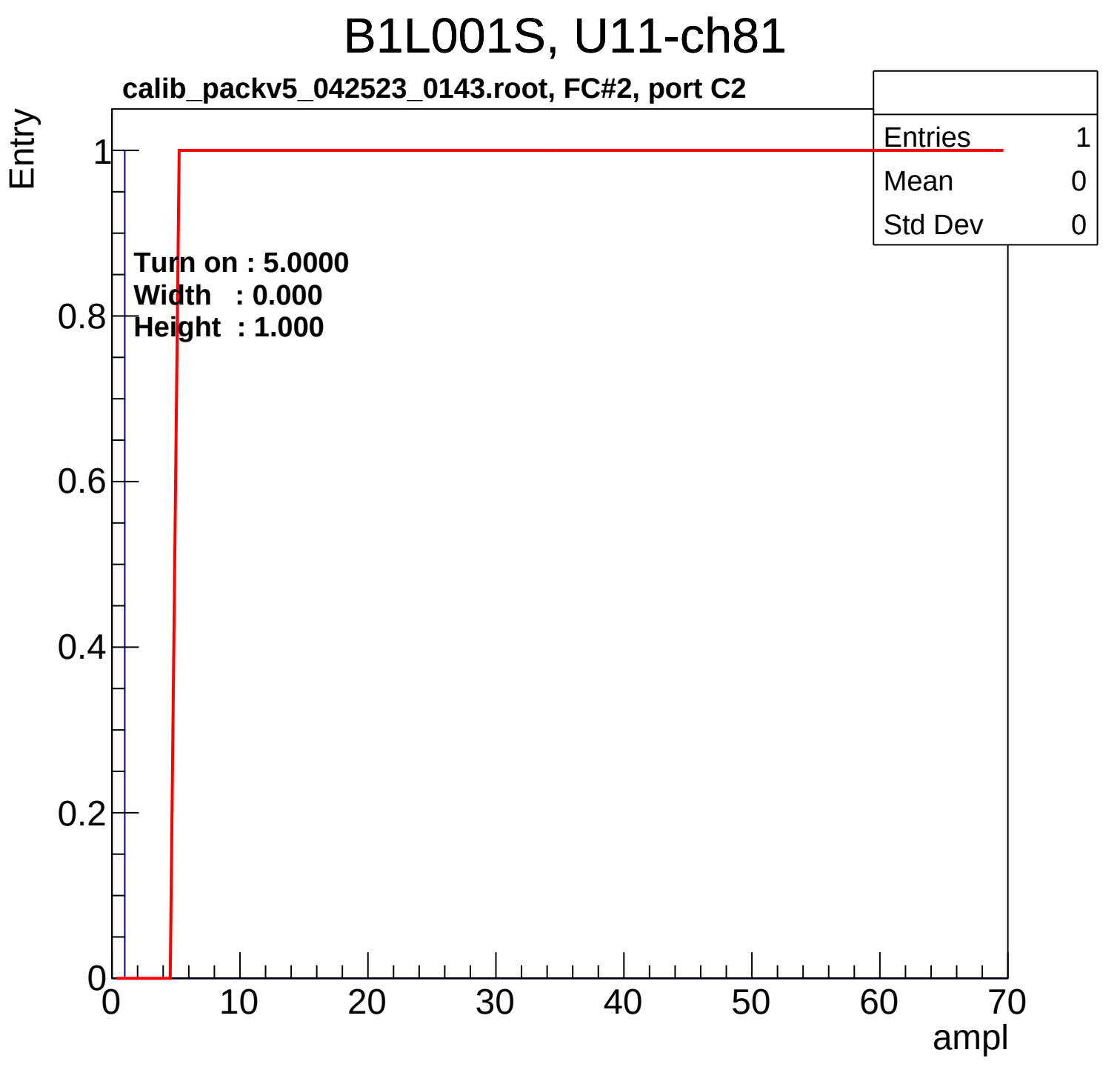

B1L001S, U11-ch76
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

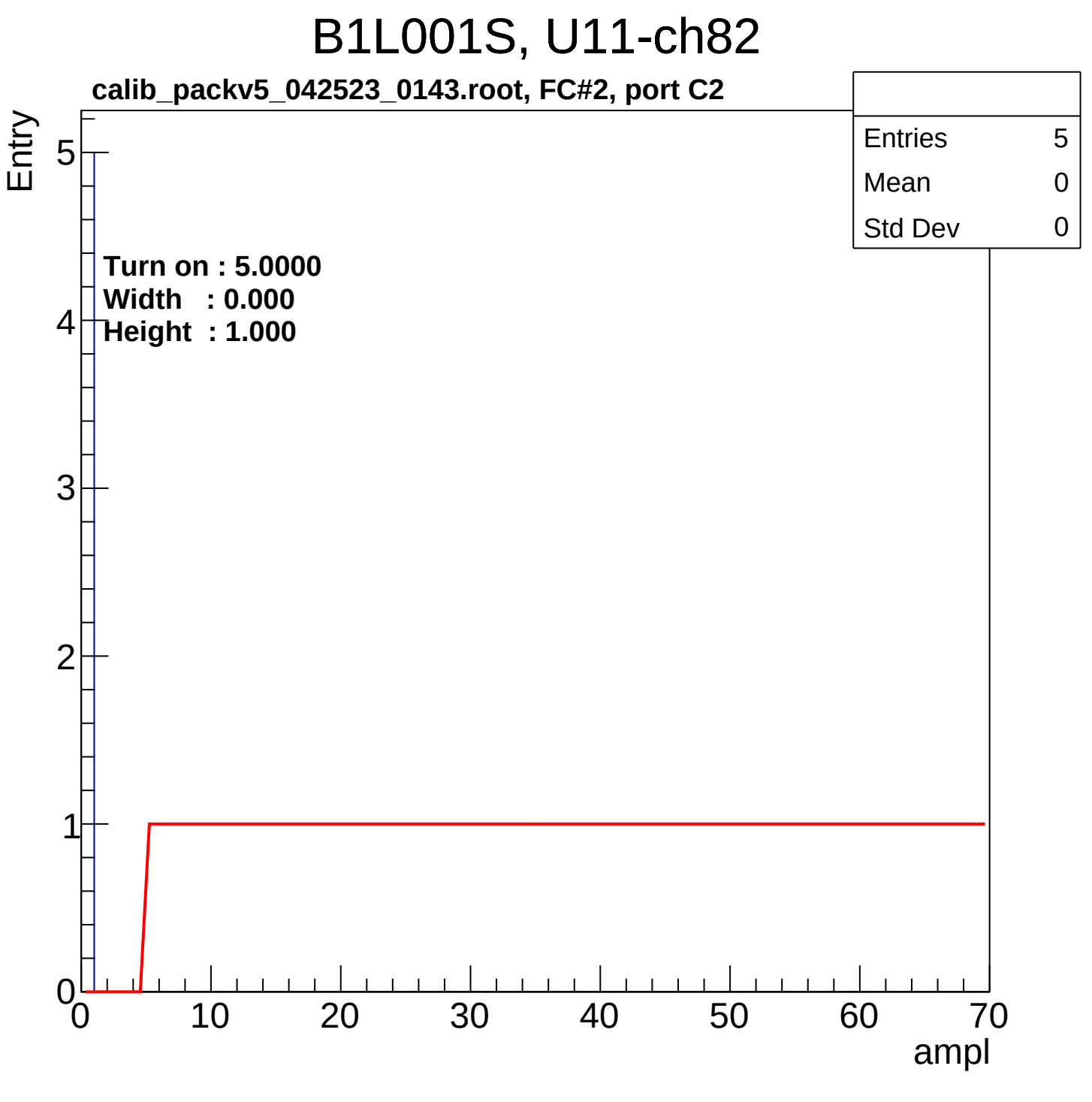

B1L001S, U11-ch77
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

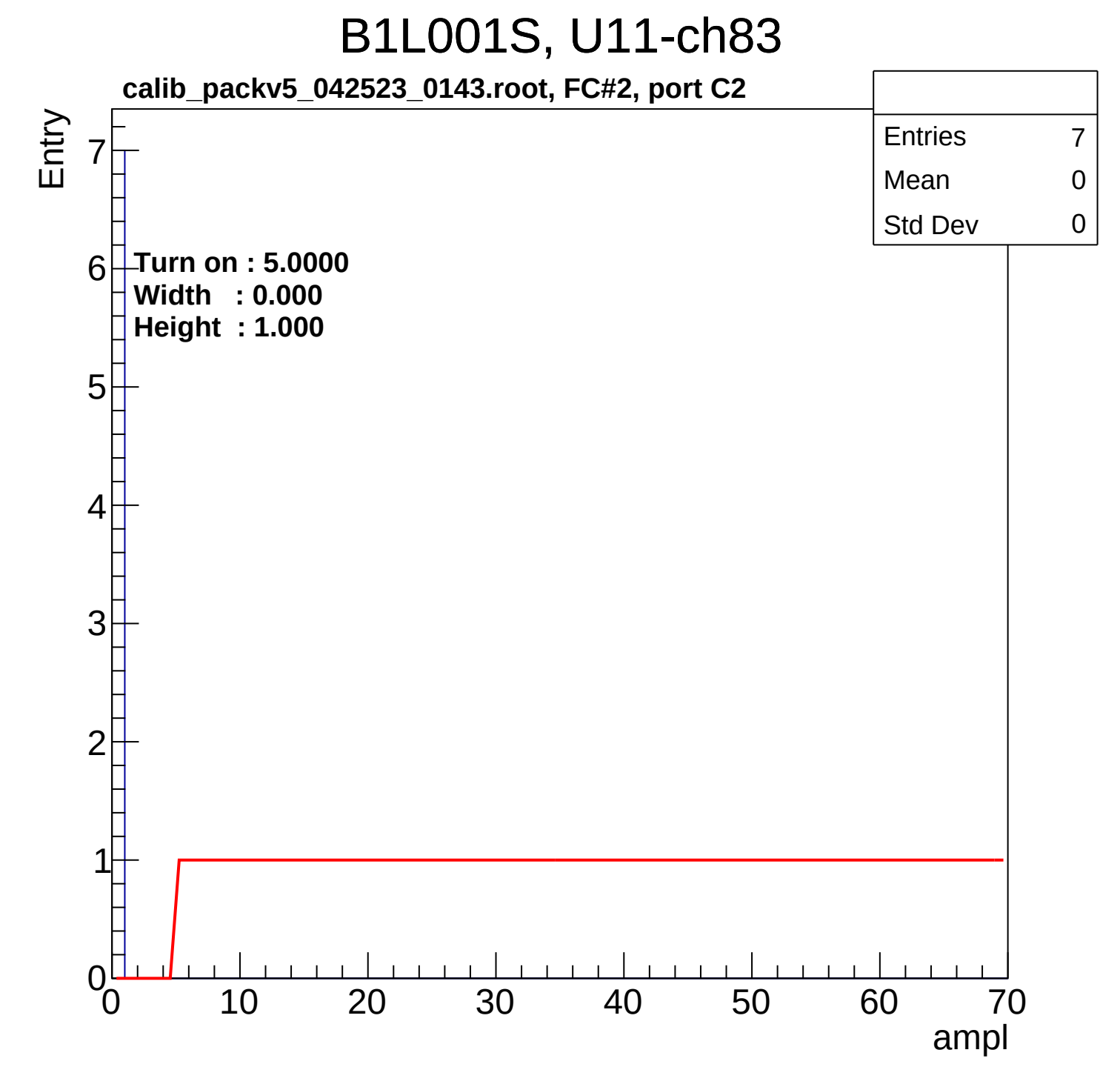

B1L001S, U11-ch78
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

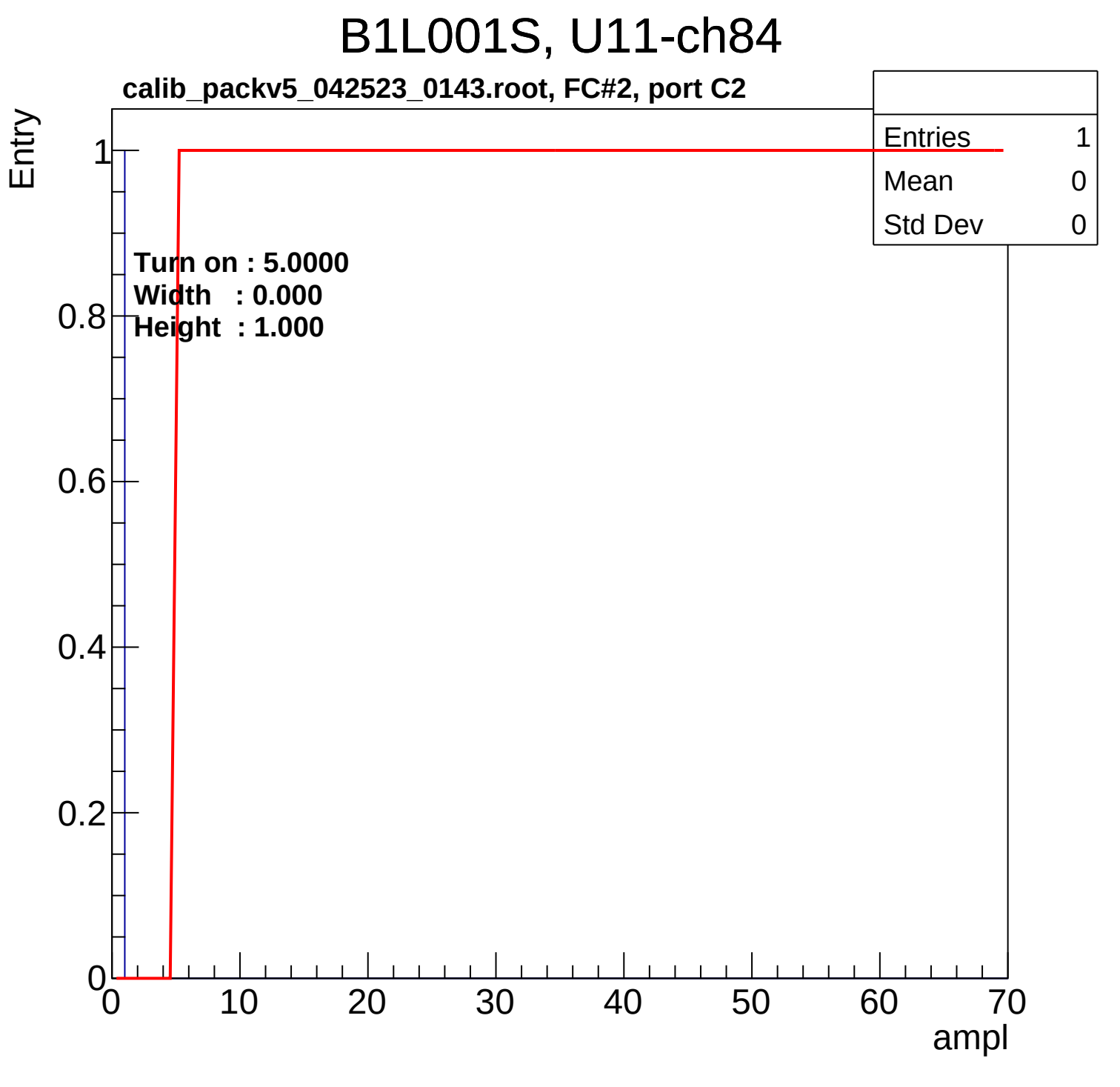

B1L001S, U11-ch79
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

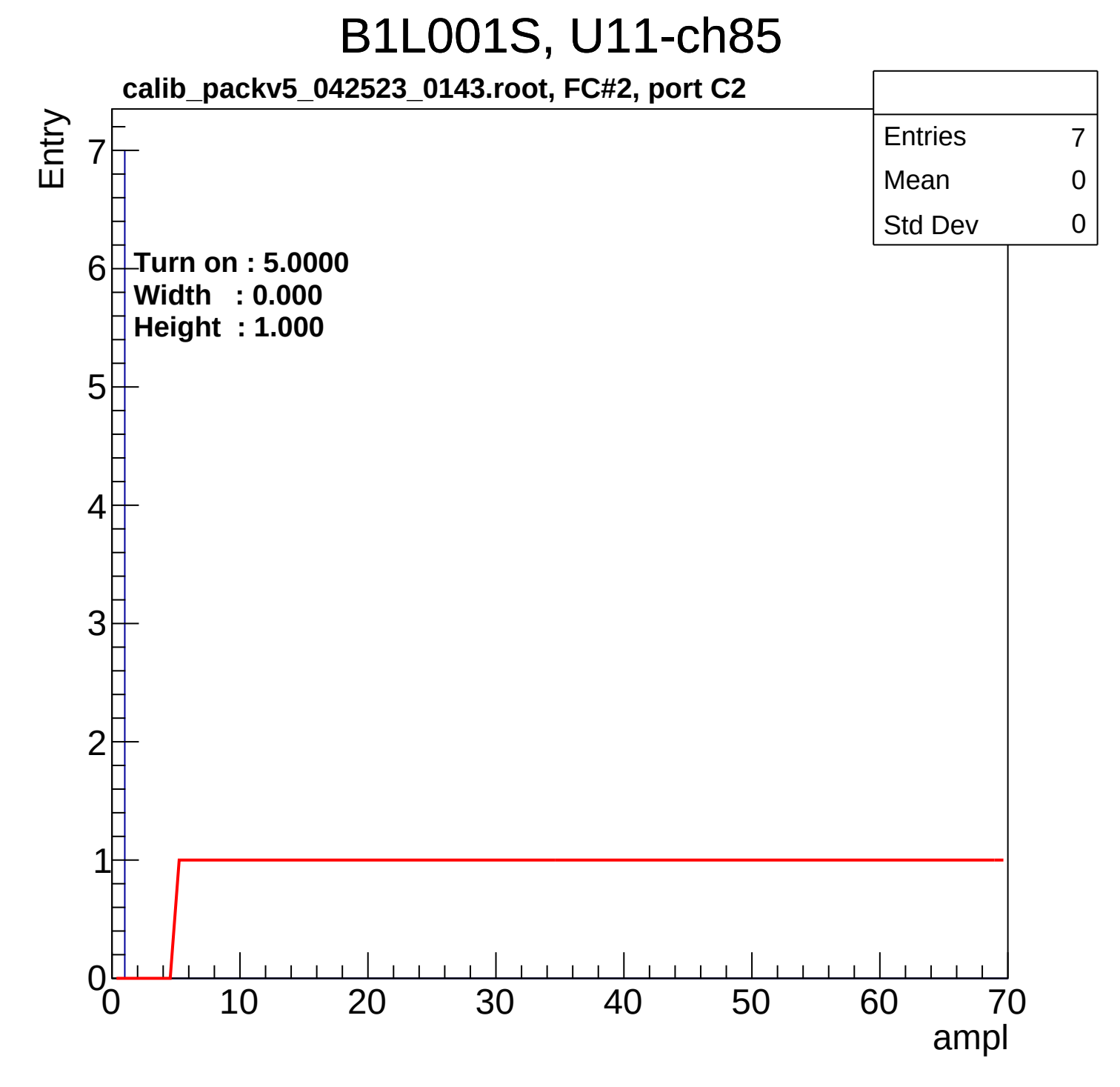

B1L001S, U11-ch80
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

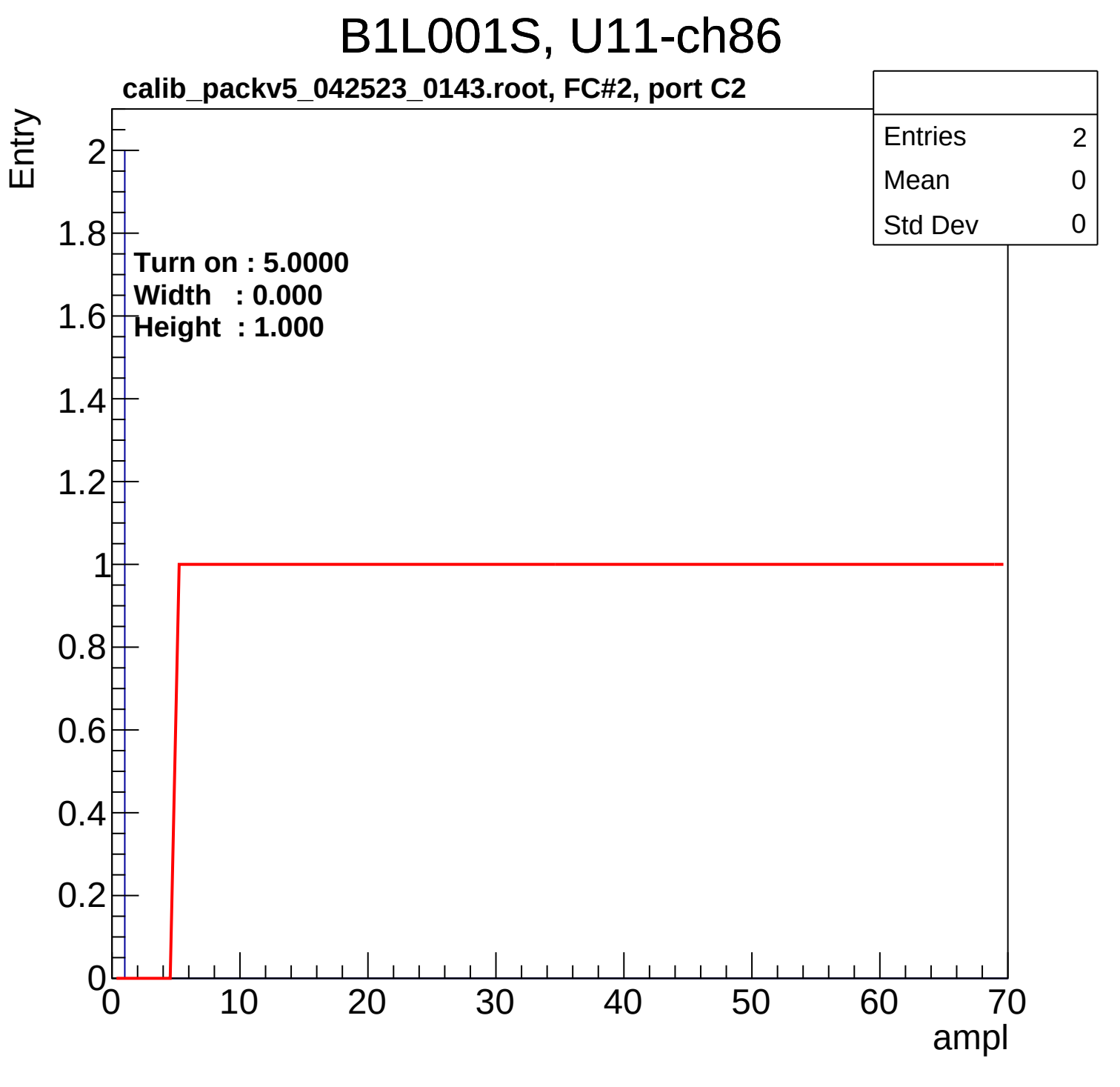

B1L001S, U11-ch81
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

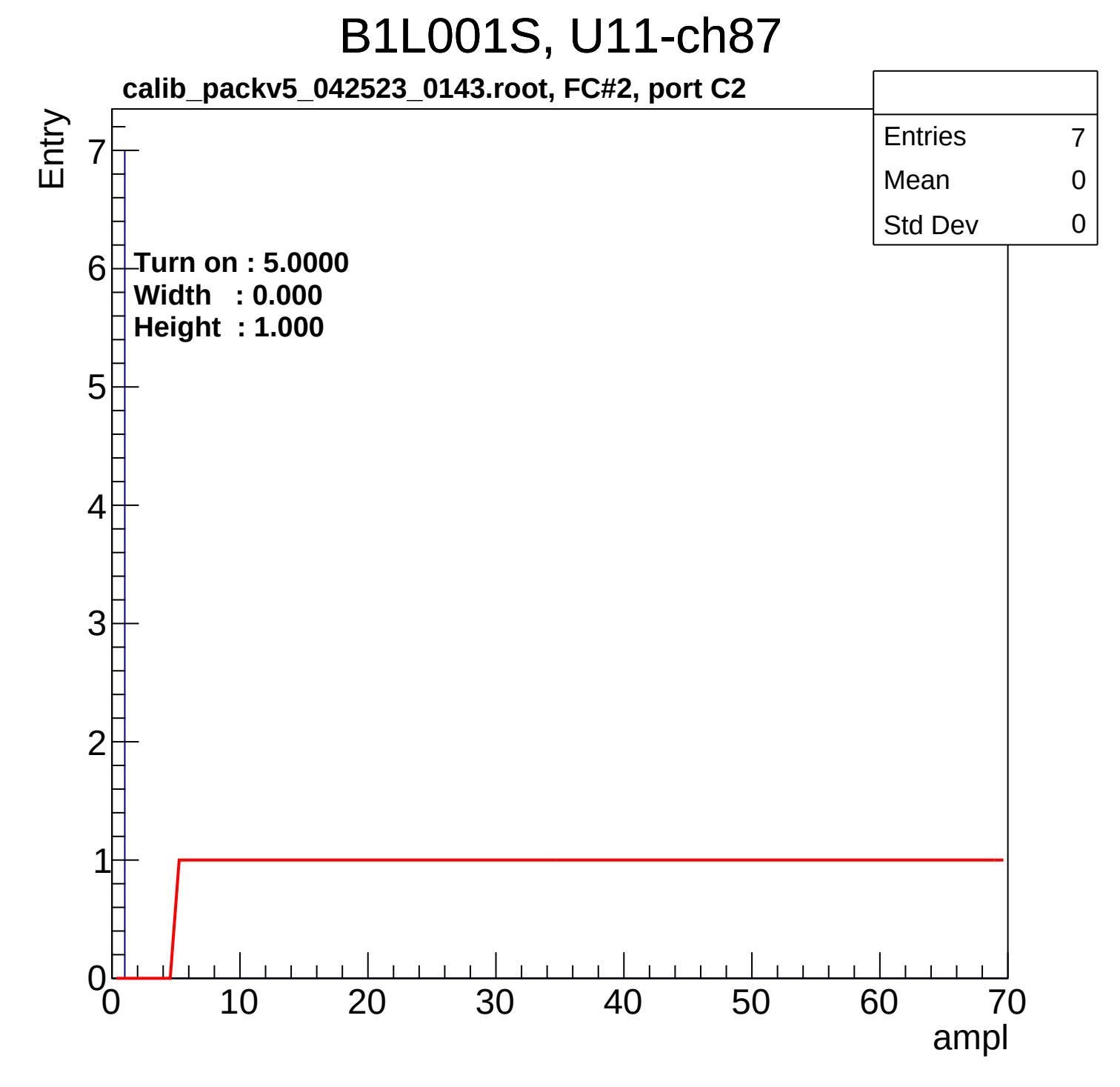

B1L001S, U11-ch82
calib_packv5_042523_0143.root, FC#2, port C2
Entries 5
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

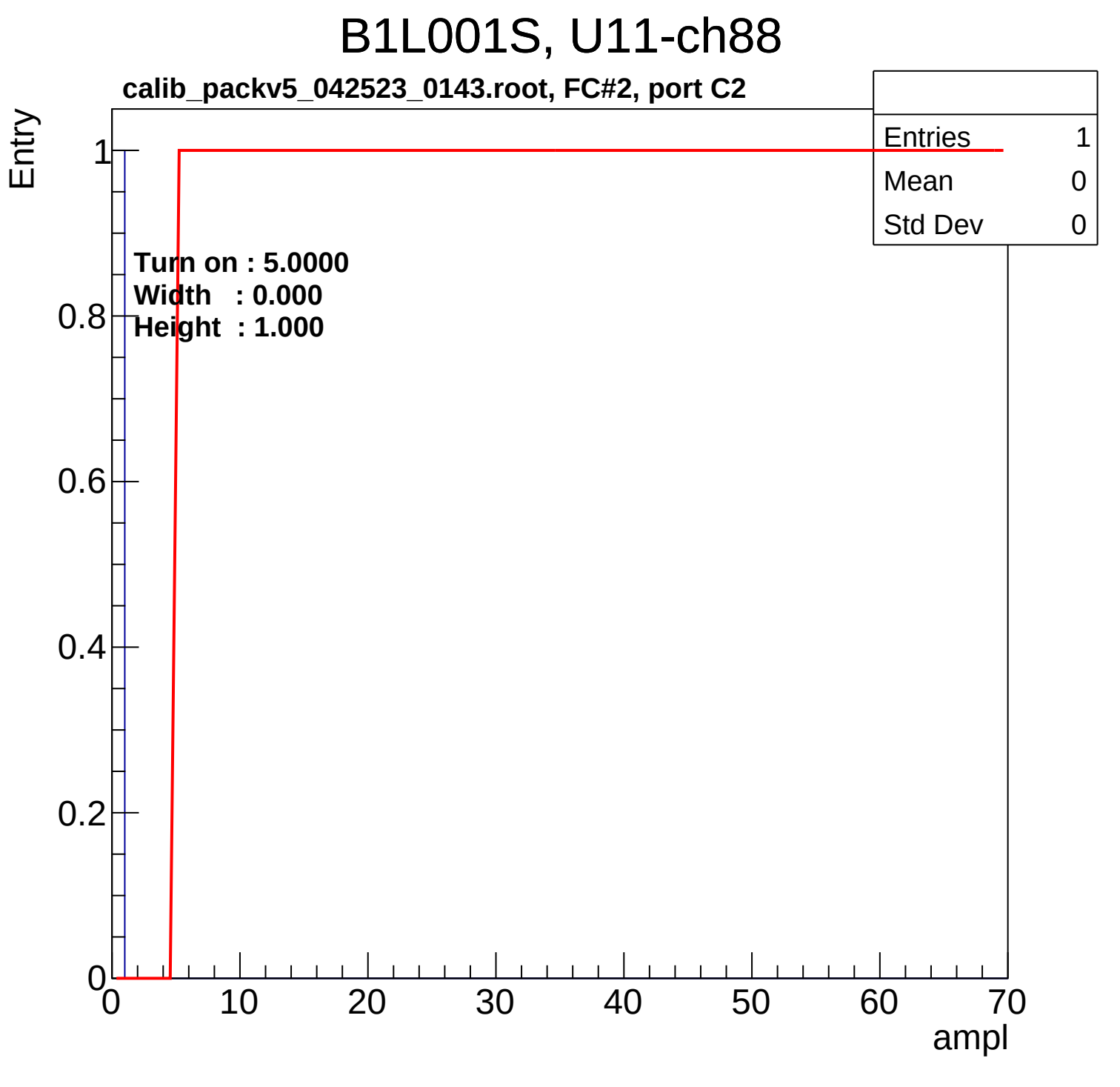

B1L001S, U11-ch83
calib_packv5_042523_0143.root, FC#2, port C2
Entries 7
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

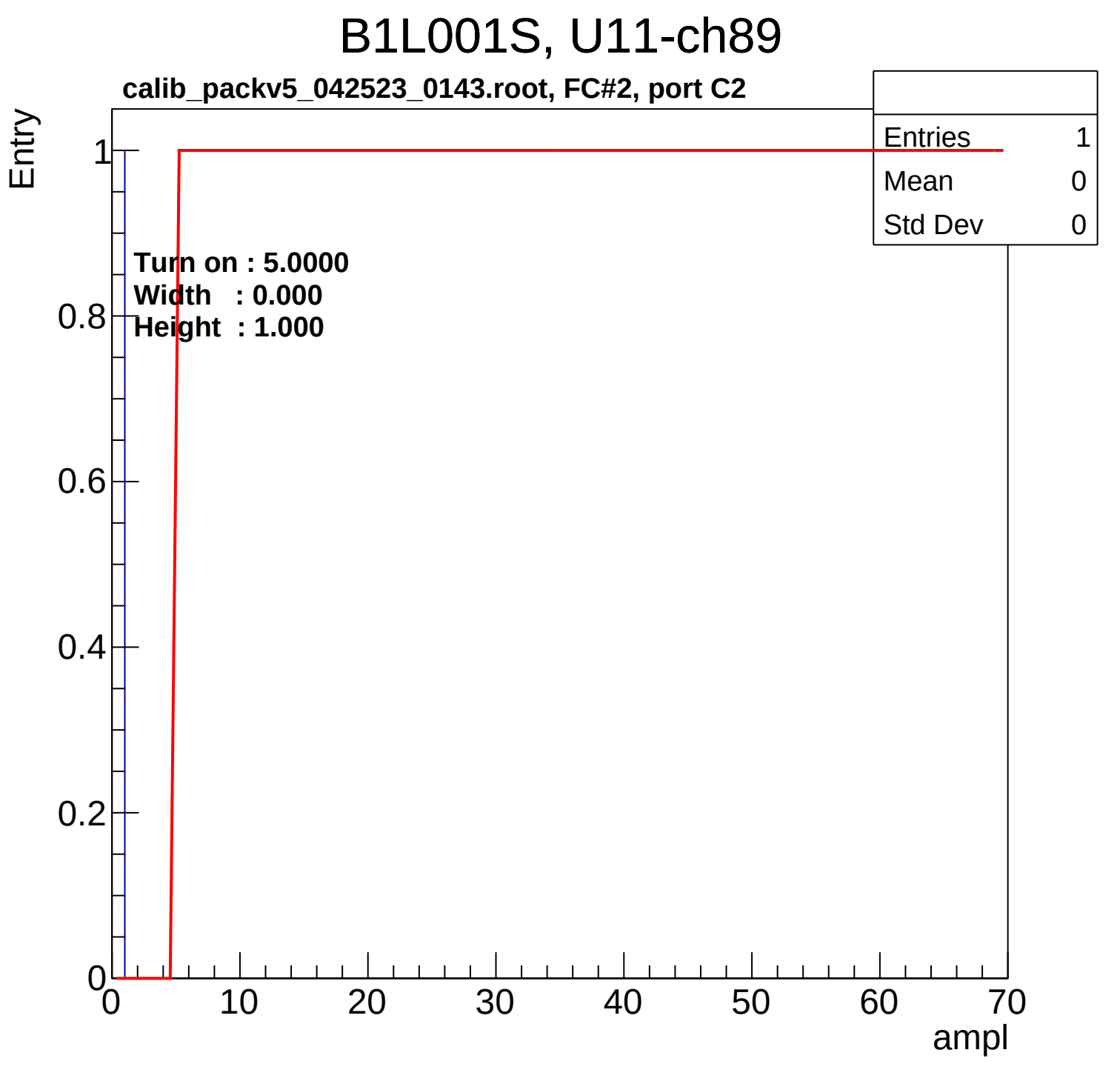

B1L001S, U11-ch84
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

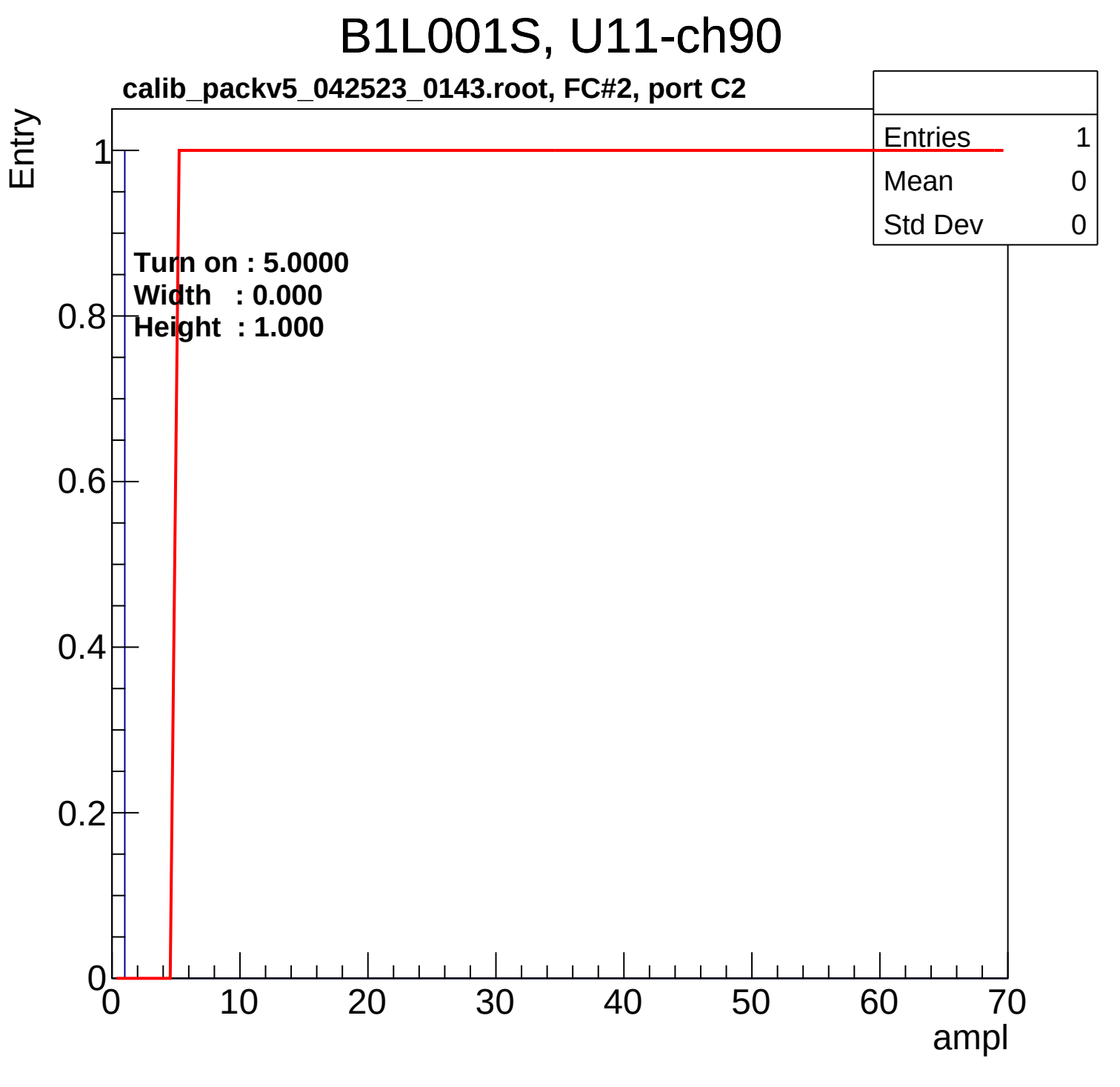

B1L001S, U11-ch85
calib_packv5_042523_0143.root, FC#2, port C2
Entries 7
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

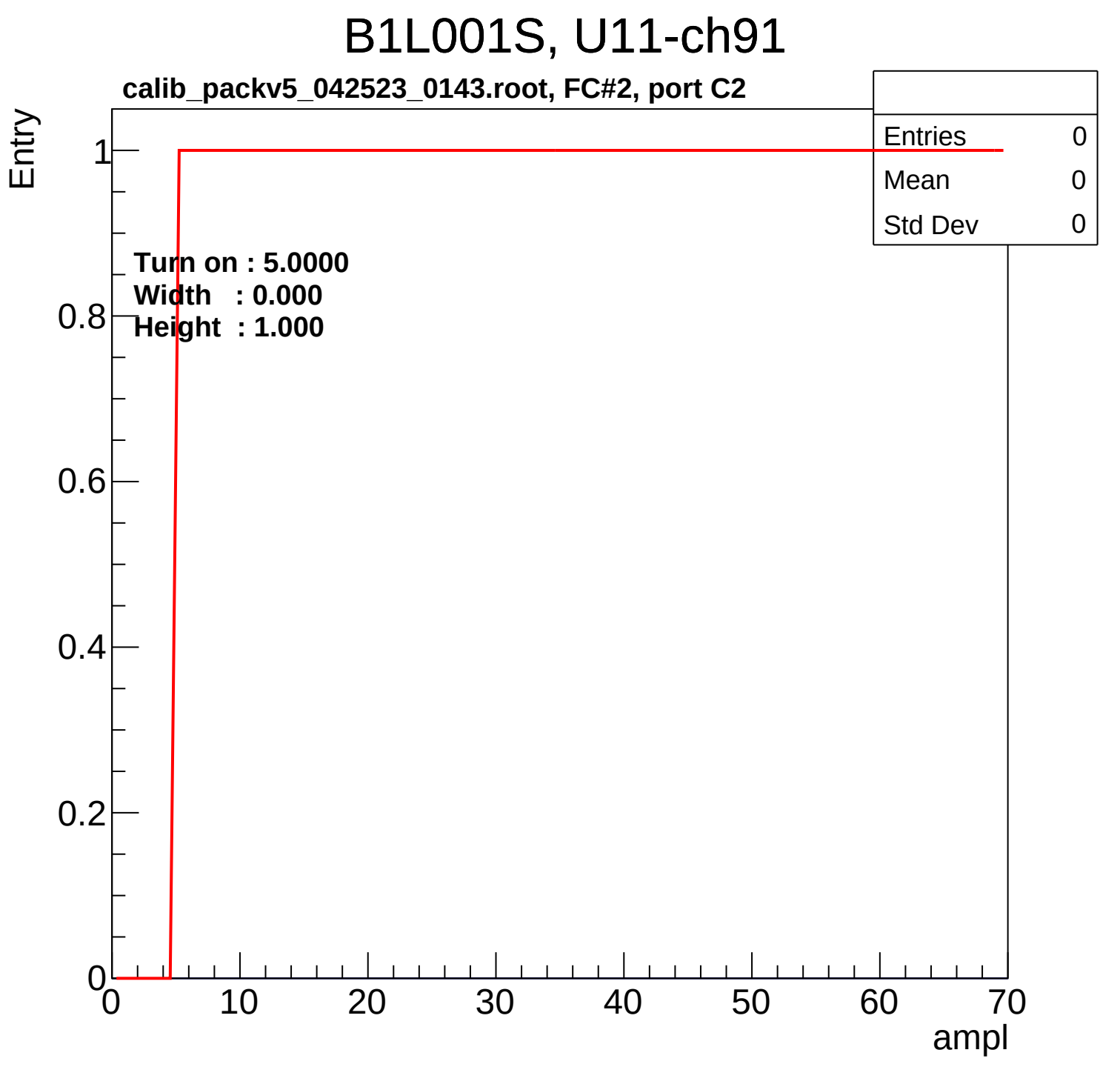

B1L001S, U11-ch86
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

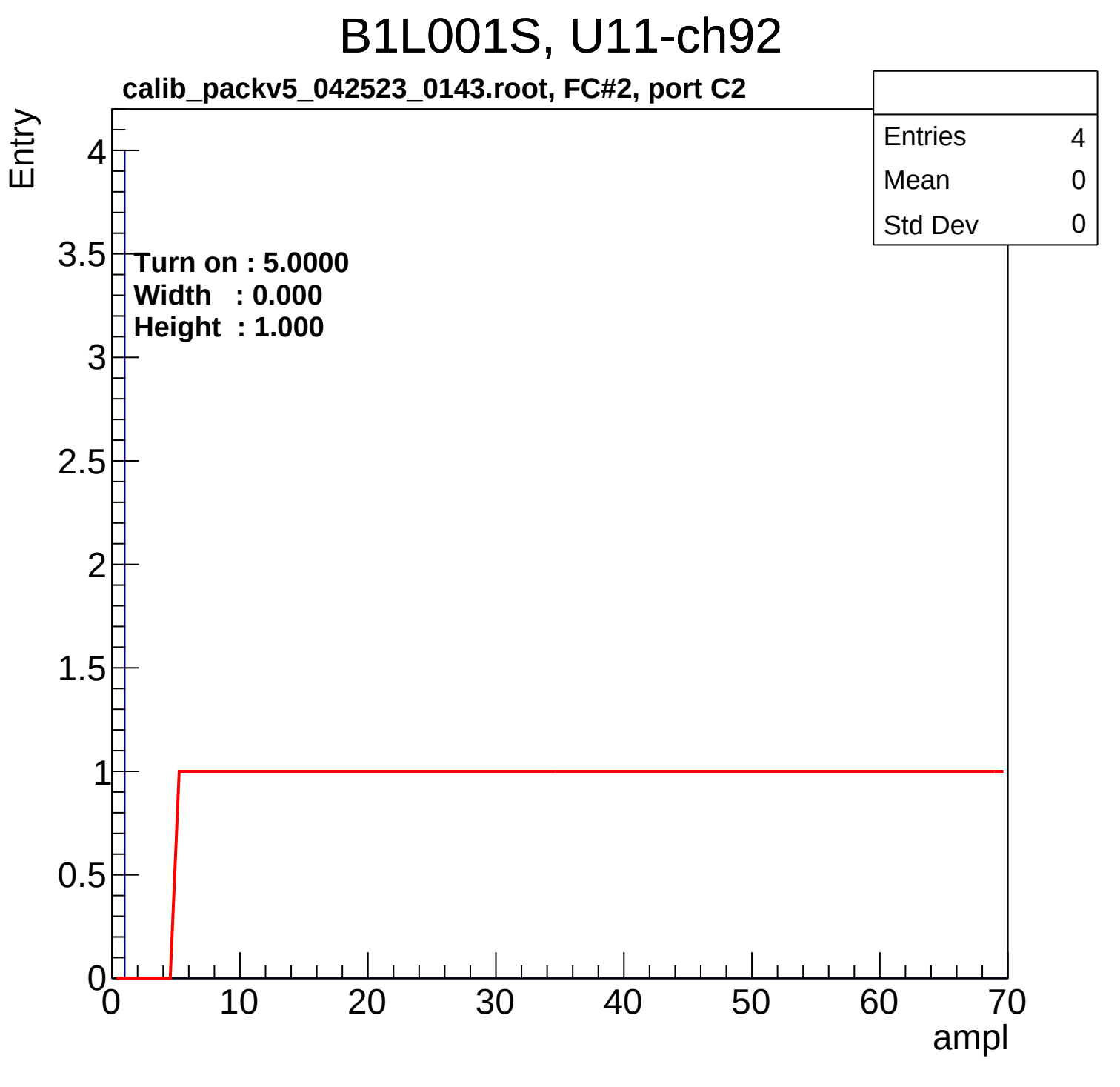

B1L001S, U11-ch87
calib_packv5_042523_0143.root, FC#2, port C2
Entries 7
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

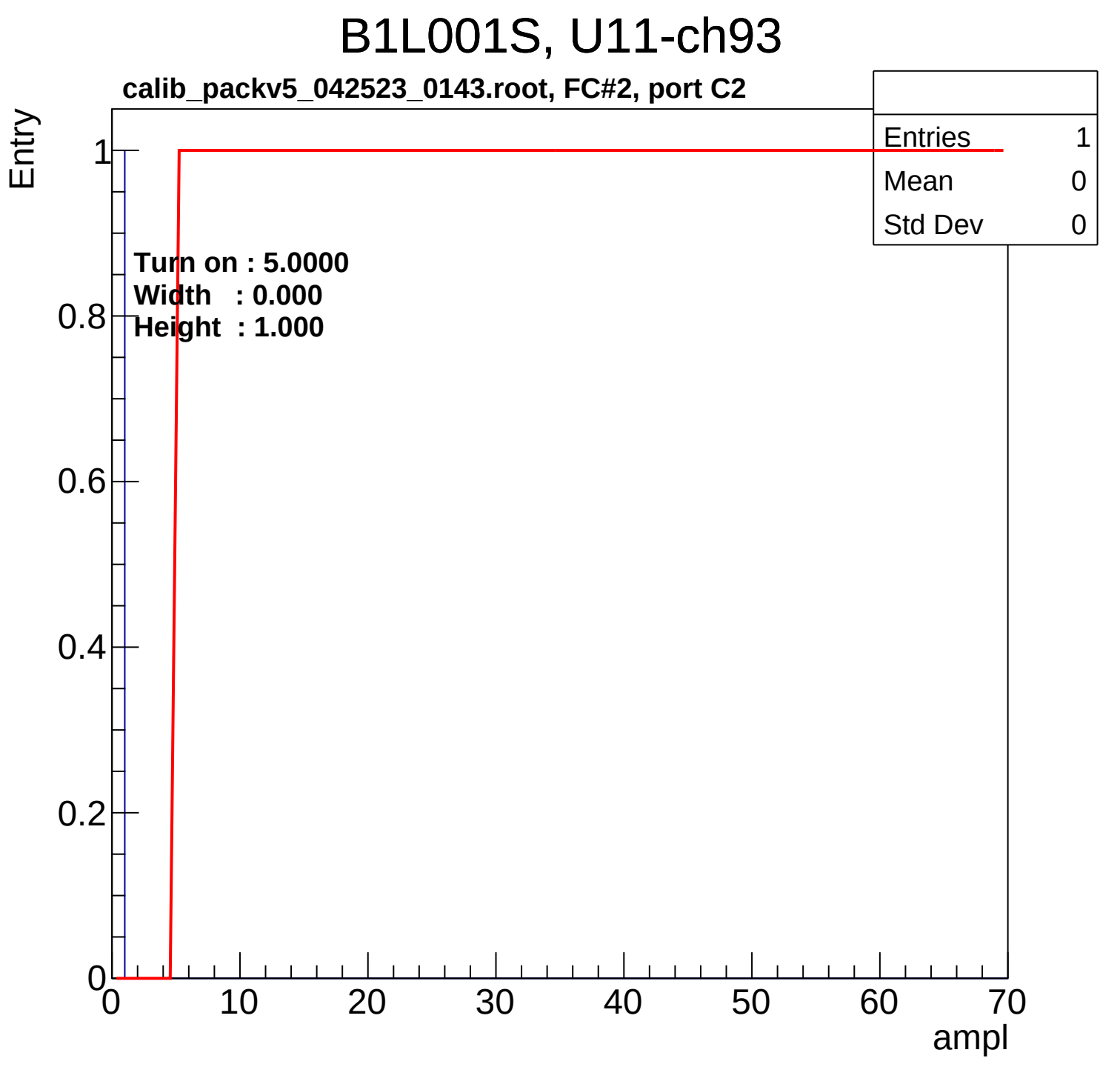

B1L001S, U11-ch88
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

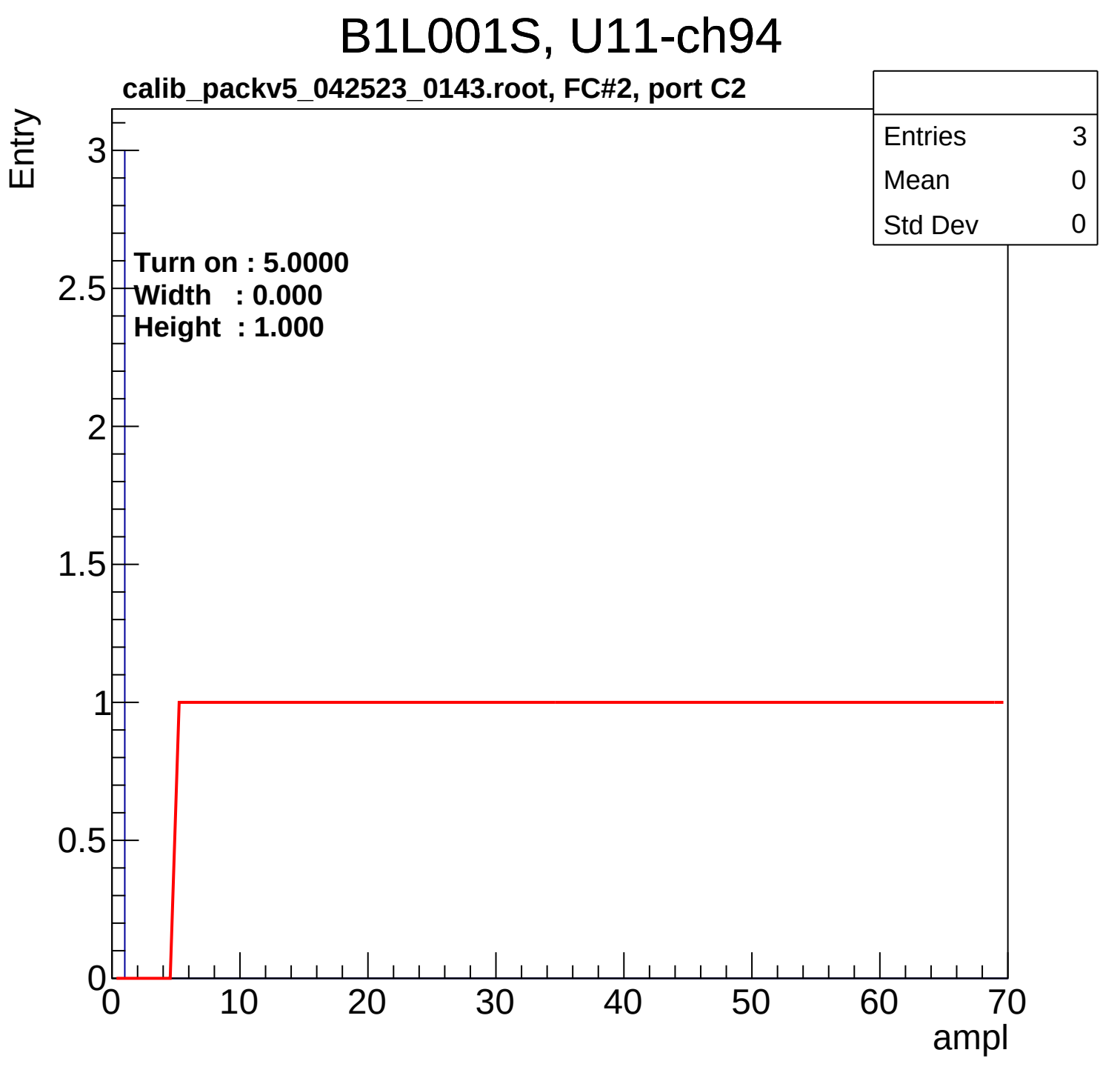

B1L001S, U11-ch89
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

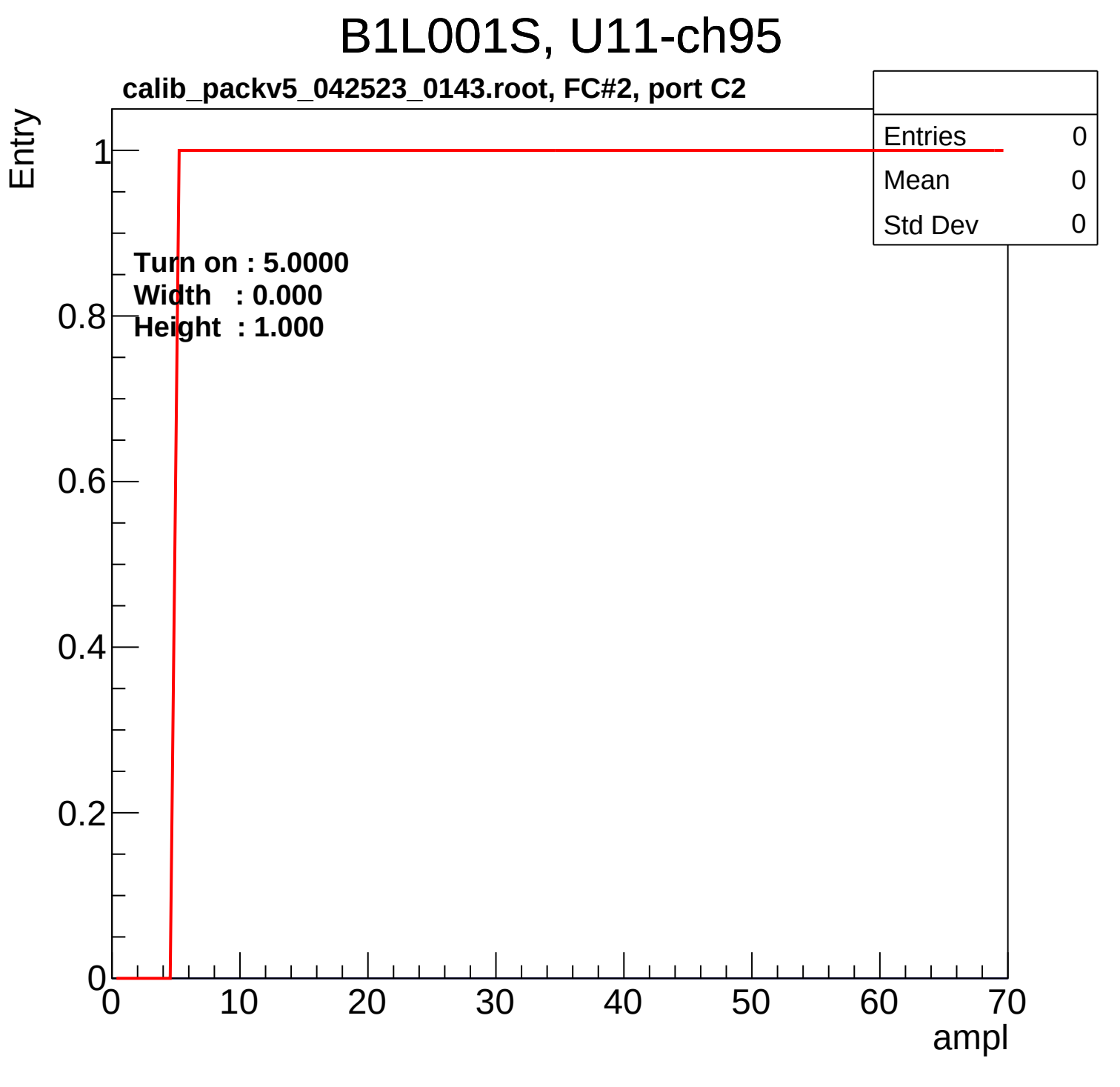

B1L001S, U11-ch90
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

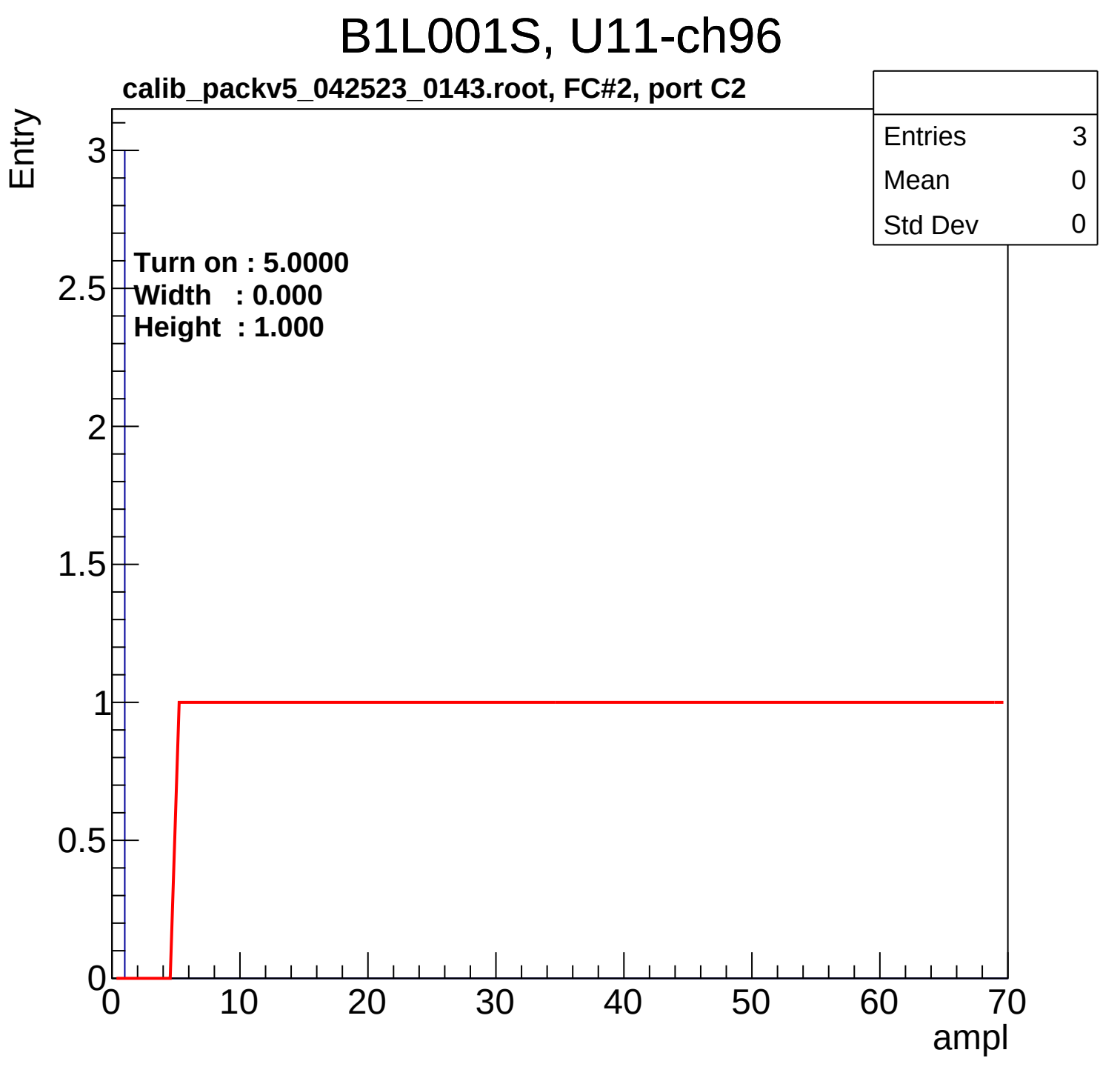

B1L001S, U11-ch91
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

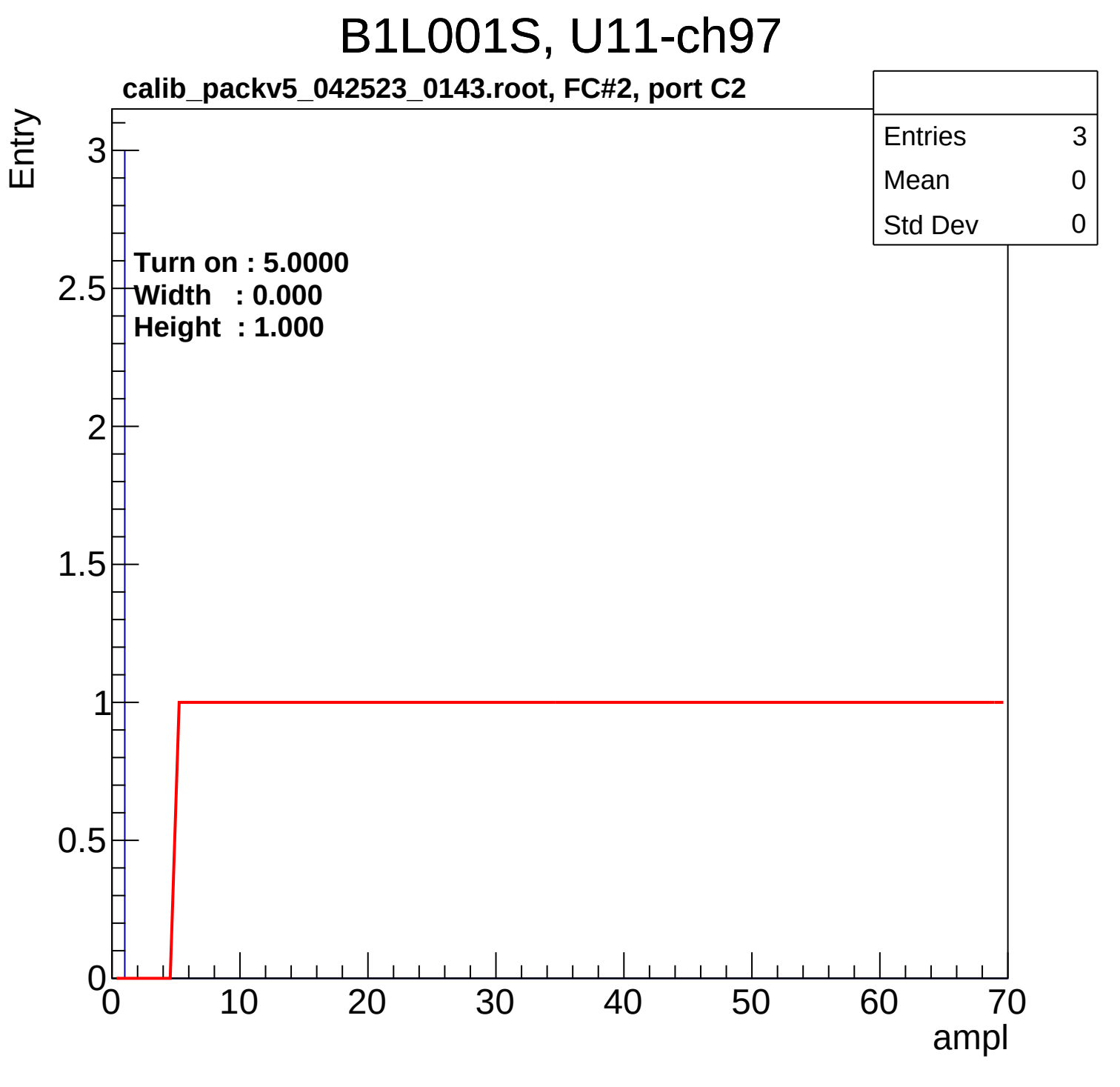

B1L001S, U11-ch92
calib_packv5_042523_0143.root, FC#2, port C2
Entries 4
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

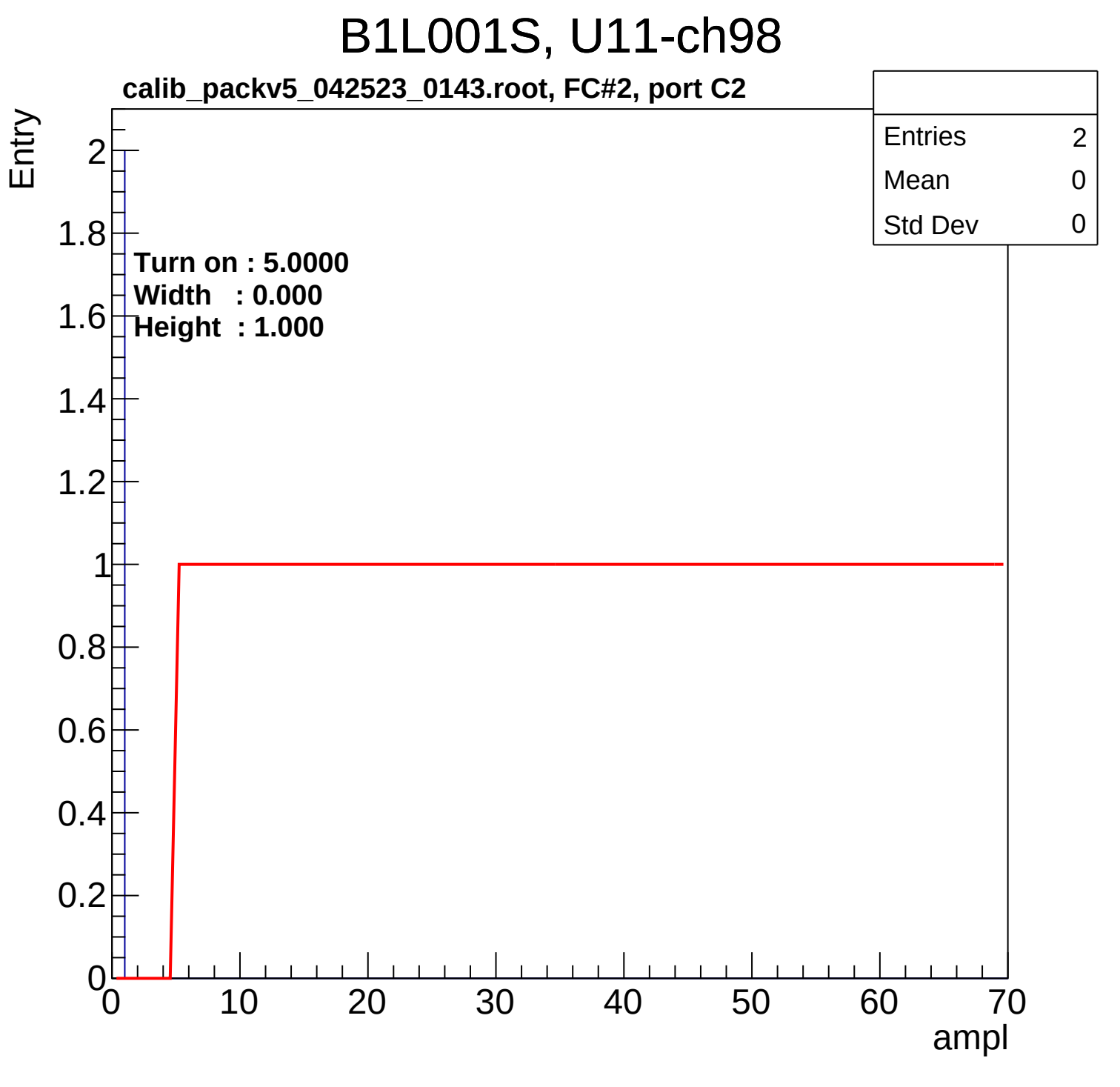

B1L001S, U11-ch93
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

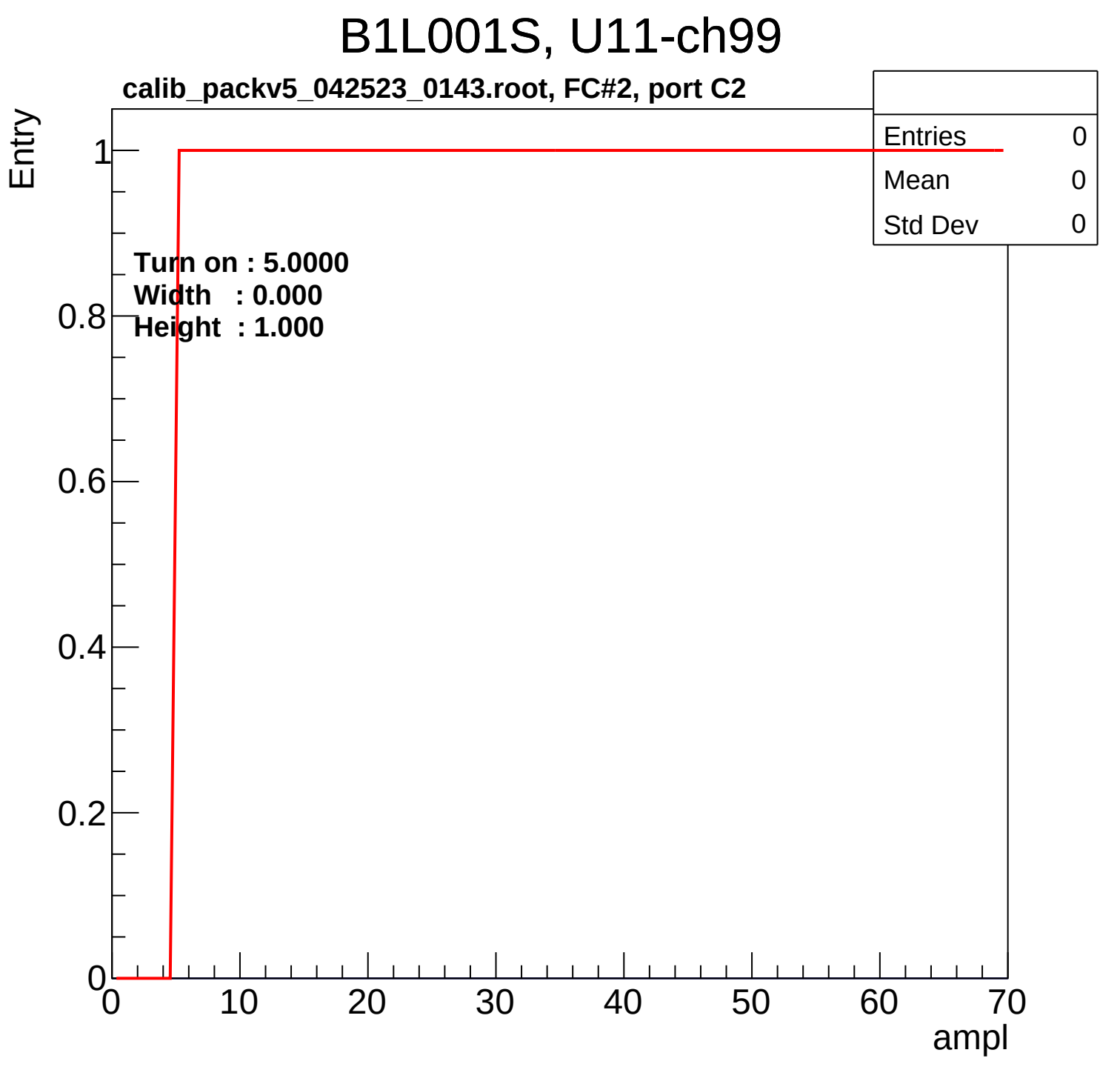

B1L001S, U11-ch94
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

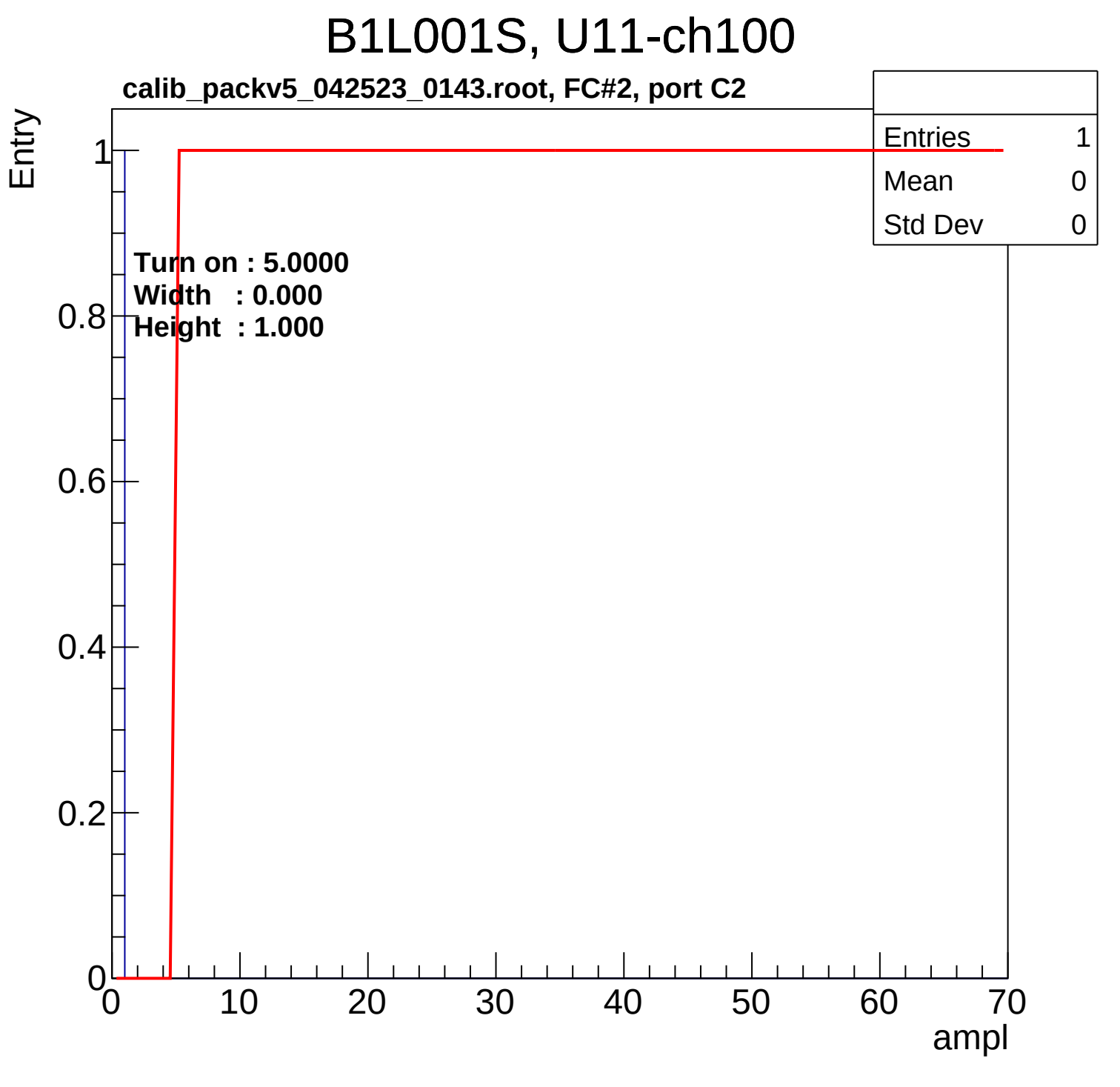

B1L001S, U11-ch95
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

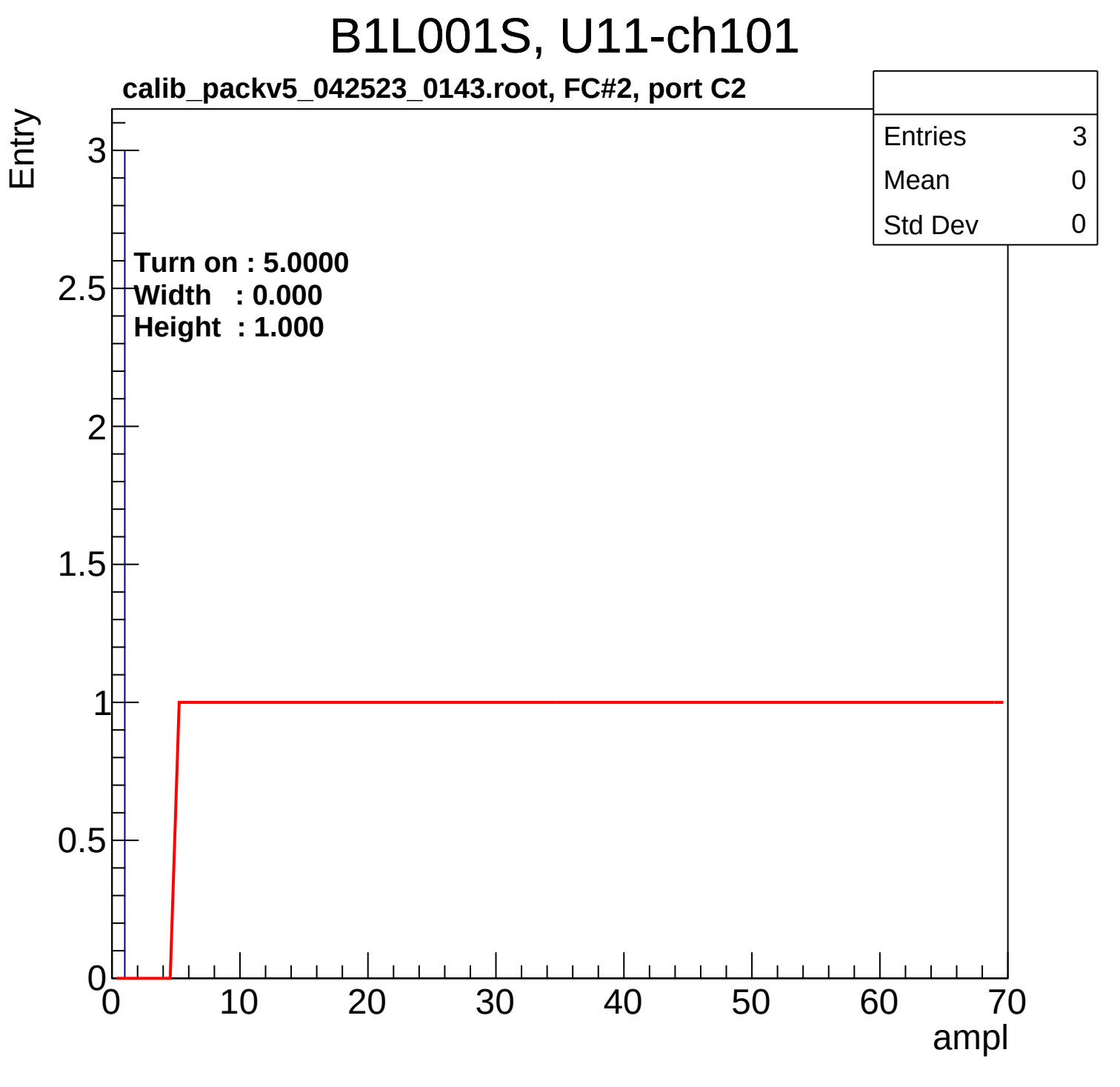

B1L001S, U11-ch96
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

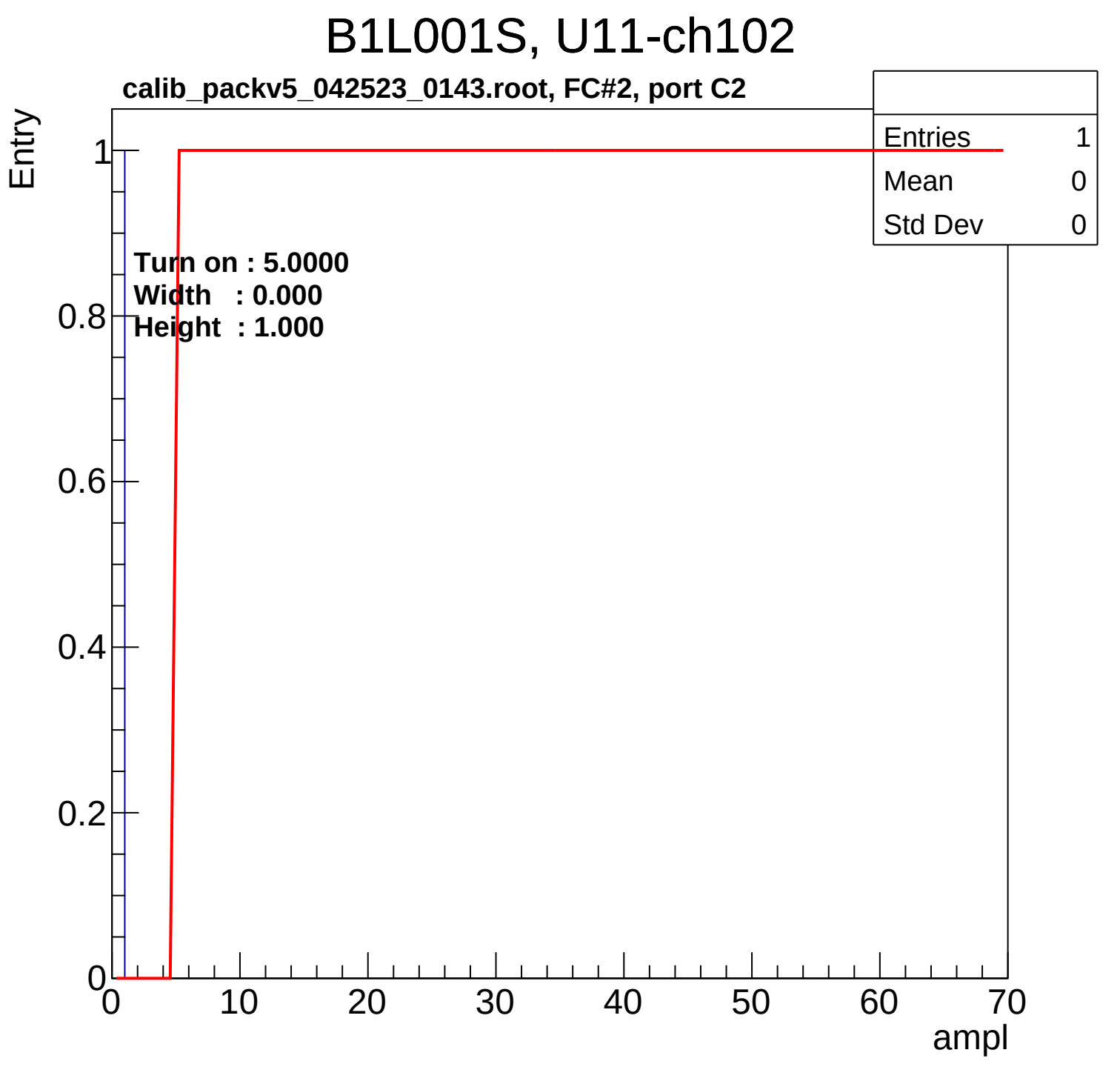

B1L001S, U11-ch97
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

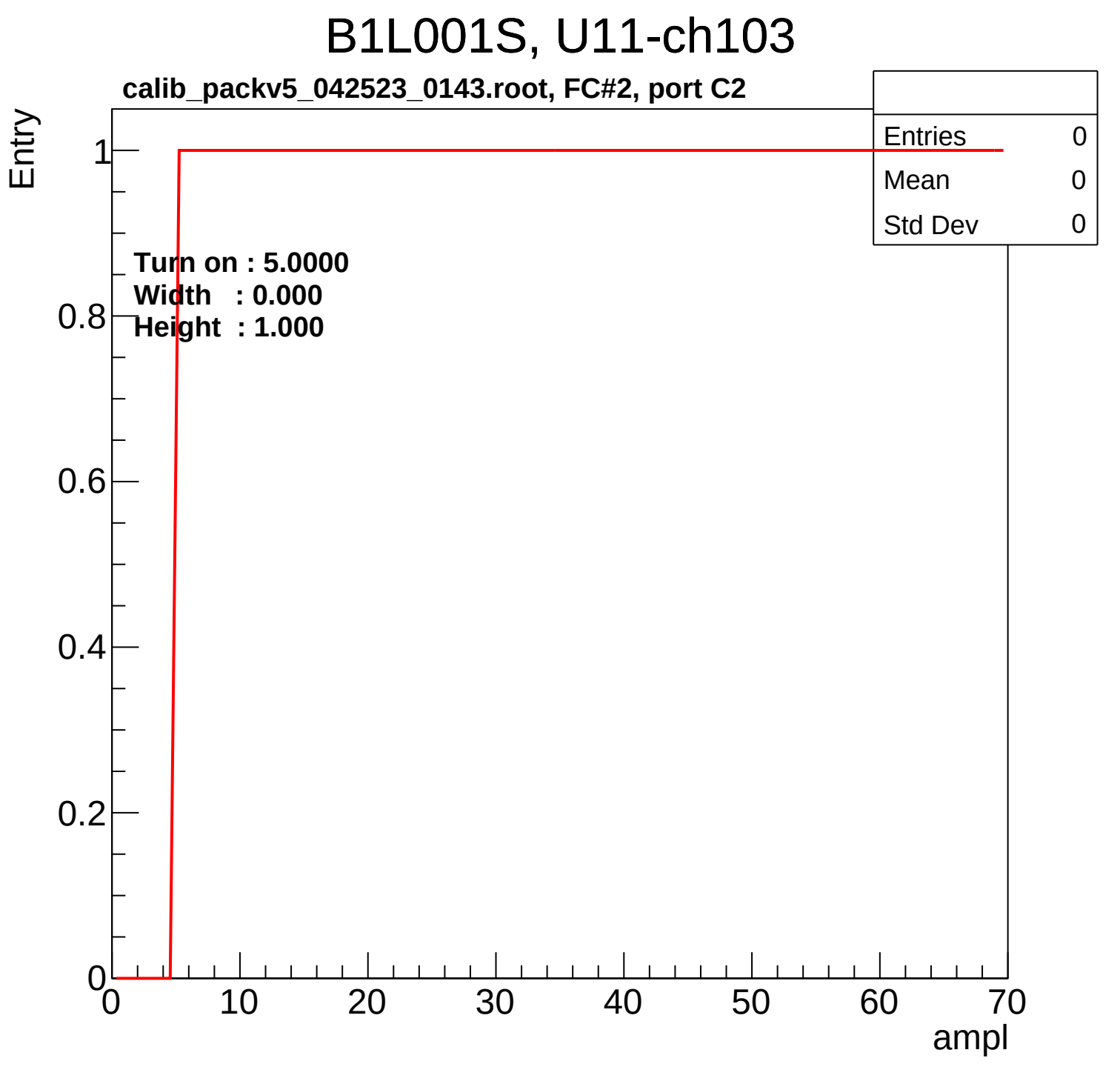

B1L001S, U11-ch98
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

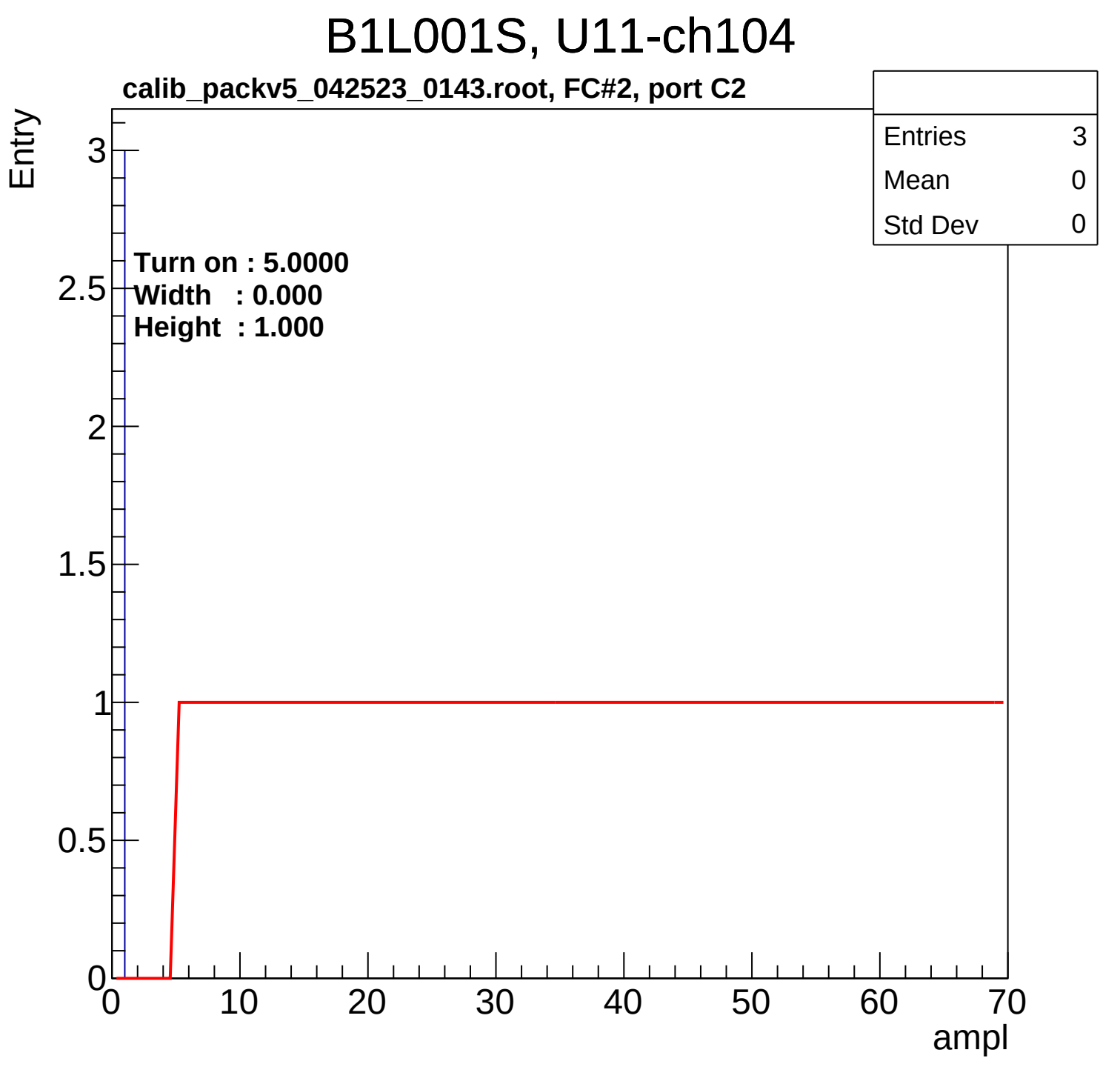

B1L001S, U11-ch99
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

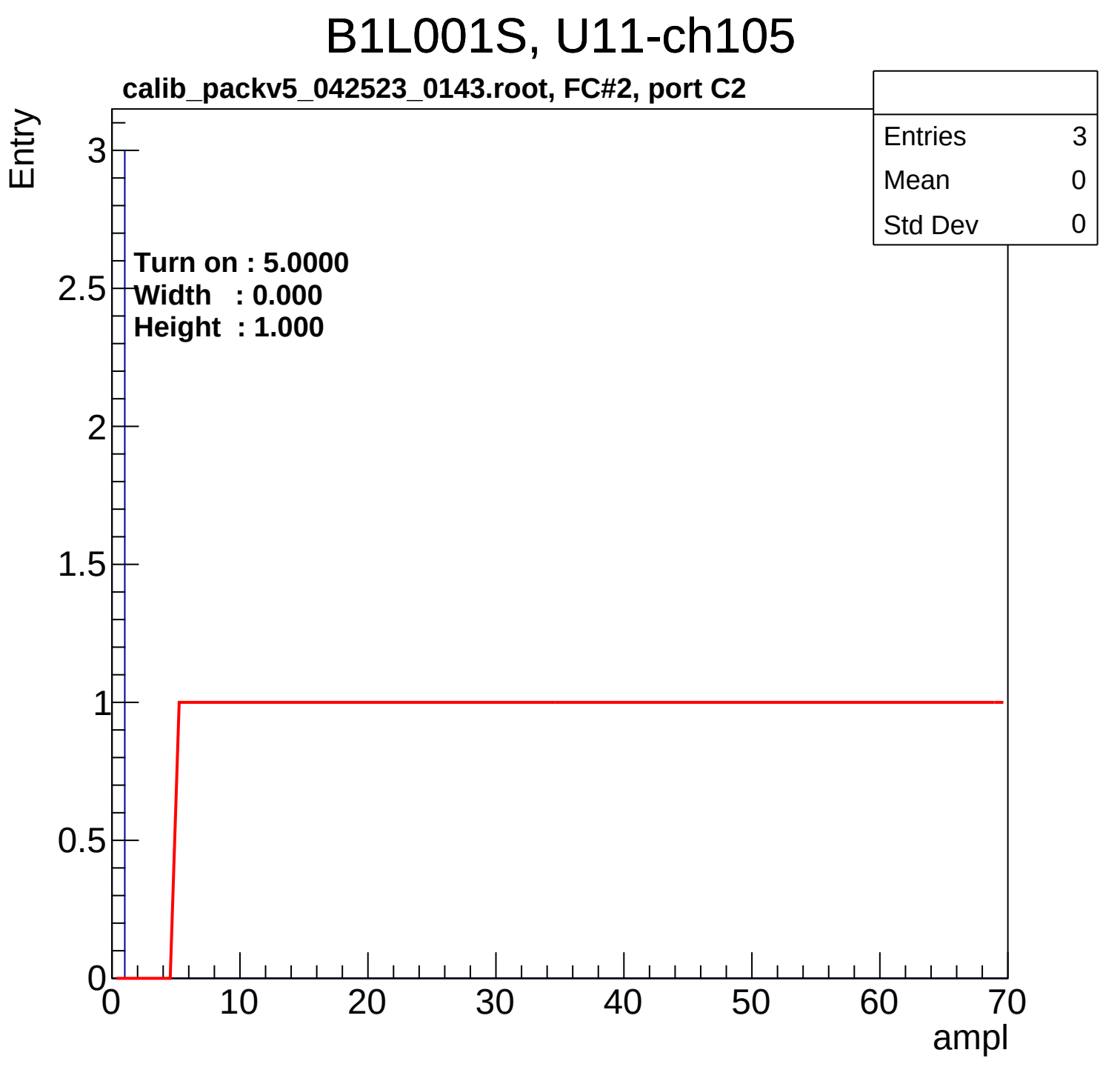

B1L001S, U11-ch100
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

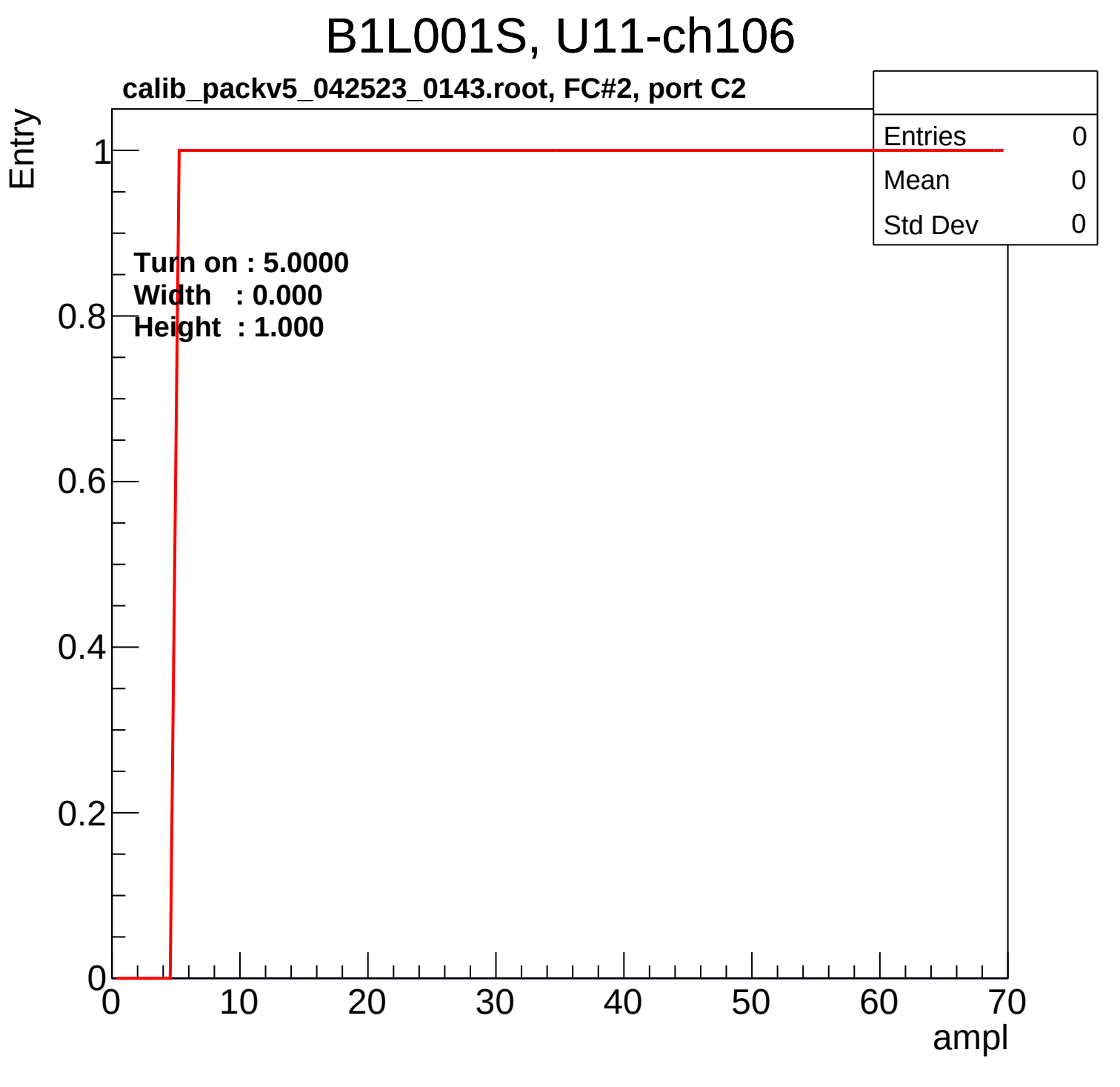

B1L001S, U11-ch101
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

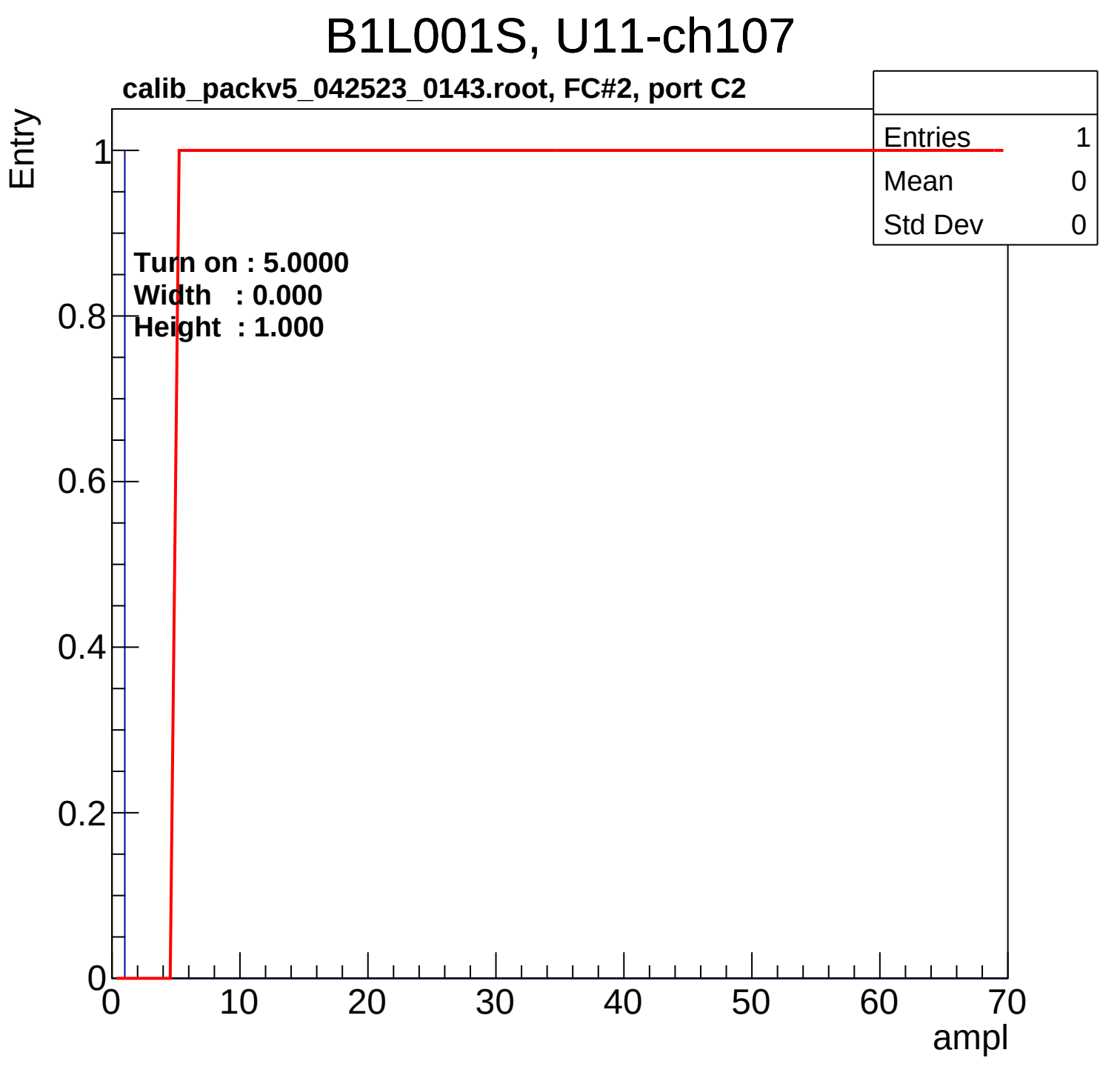

B1L001S, U11-ch102
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

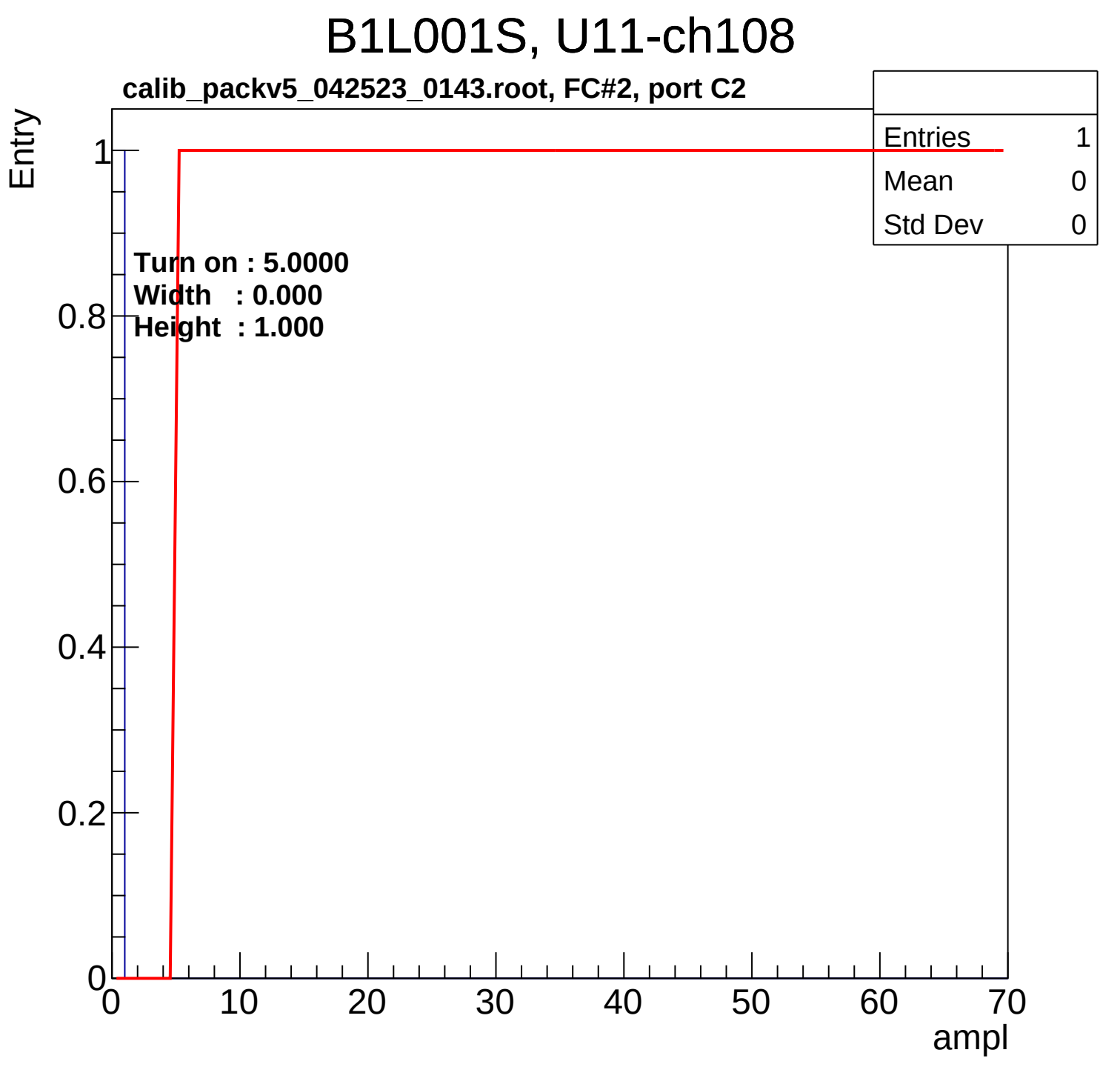

B1L001S, U11-ch103
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

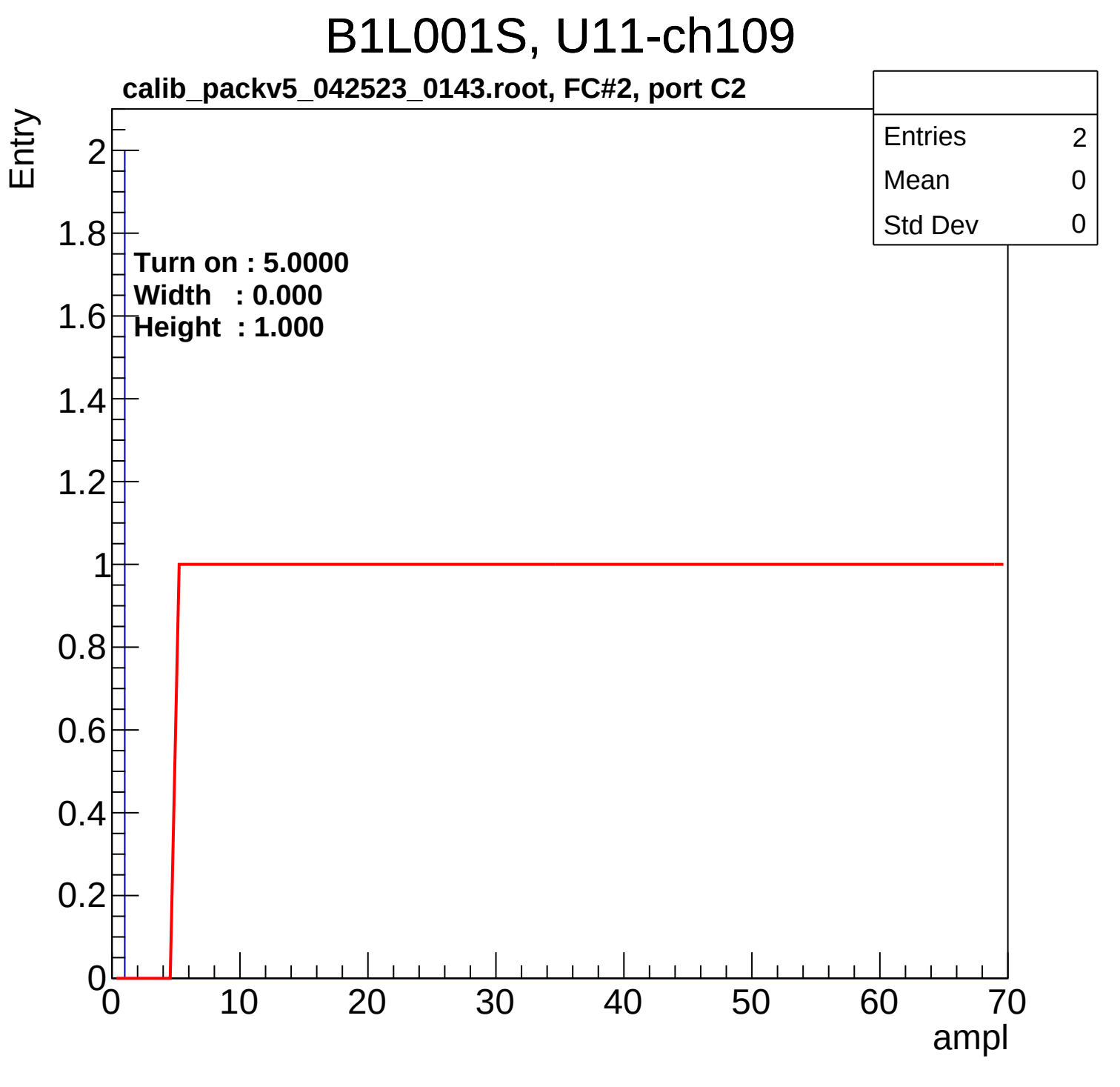

B1L001S, U11-ch104
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

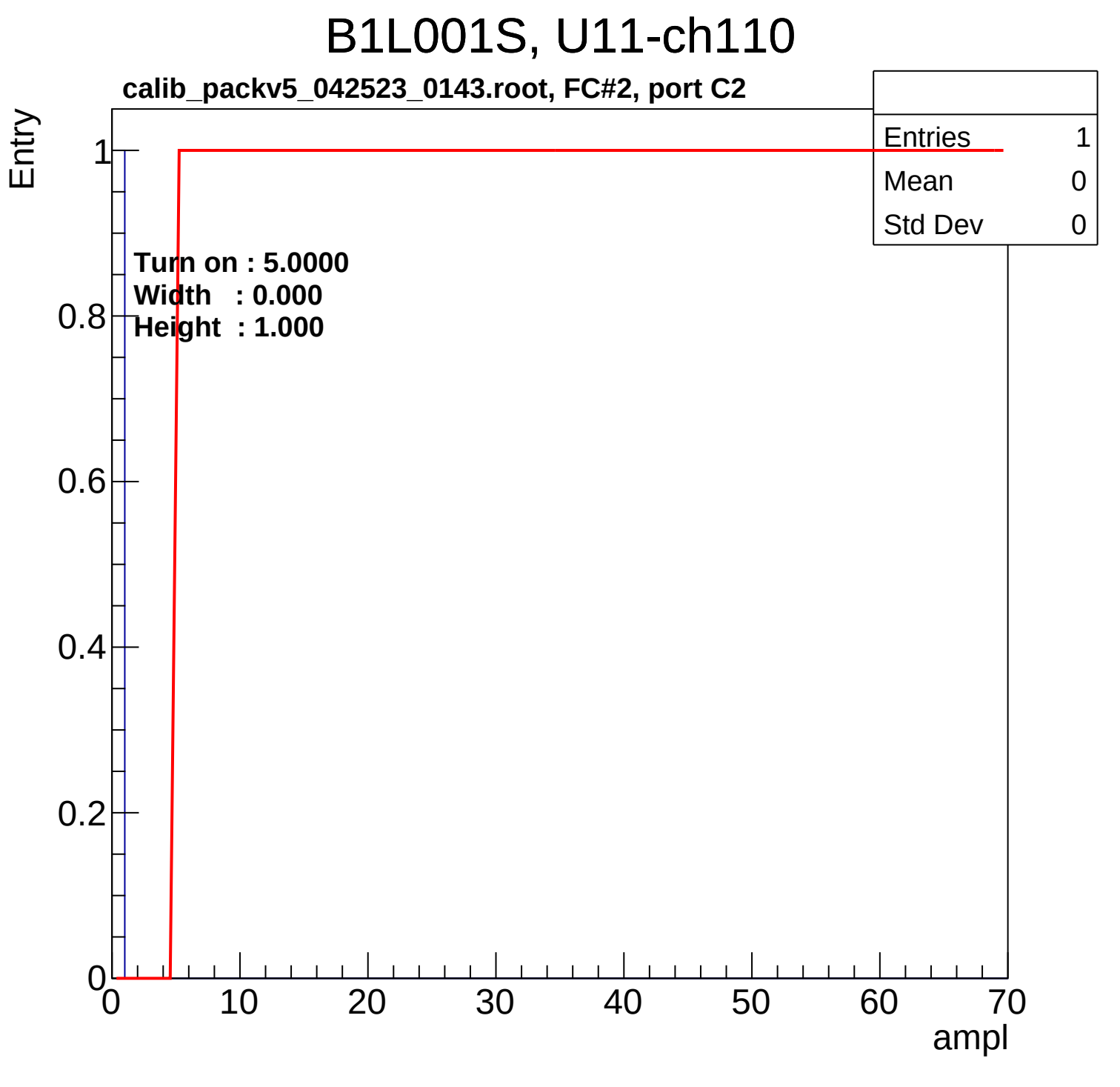

B1L001S, U11-ch105
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

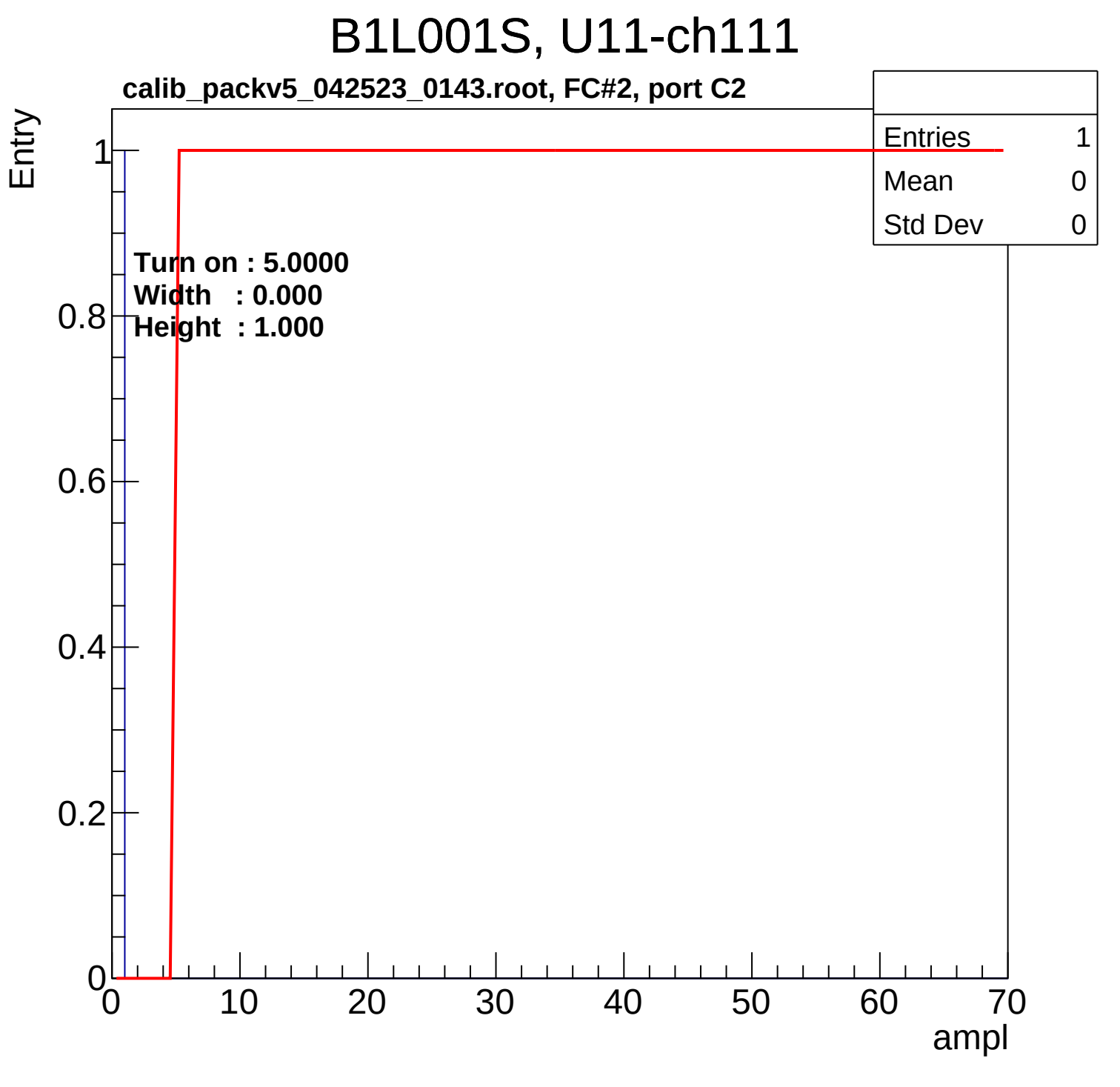

B1L001S, U11-ch106
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

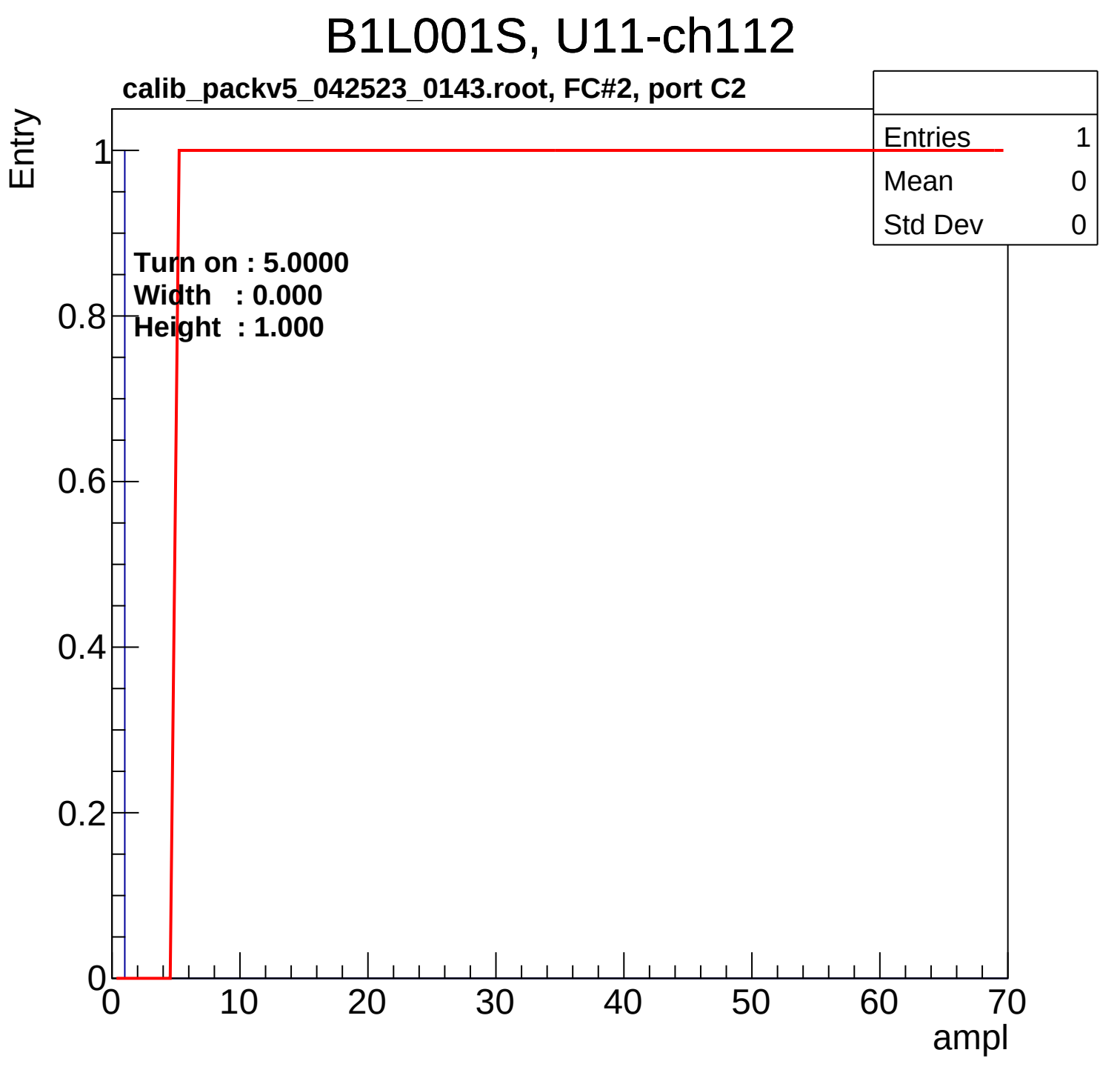

B1L001S, U11-ch107
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

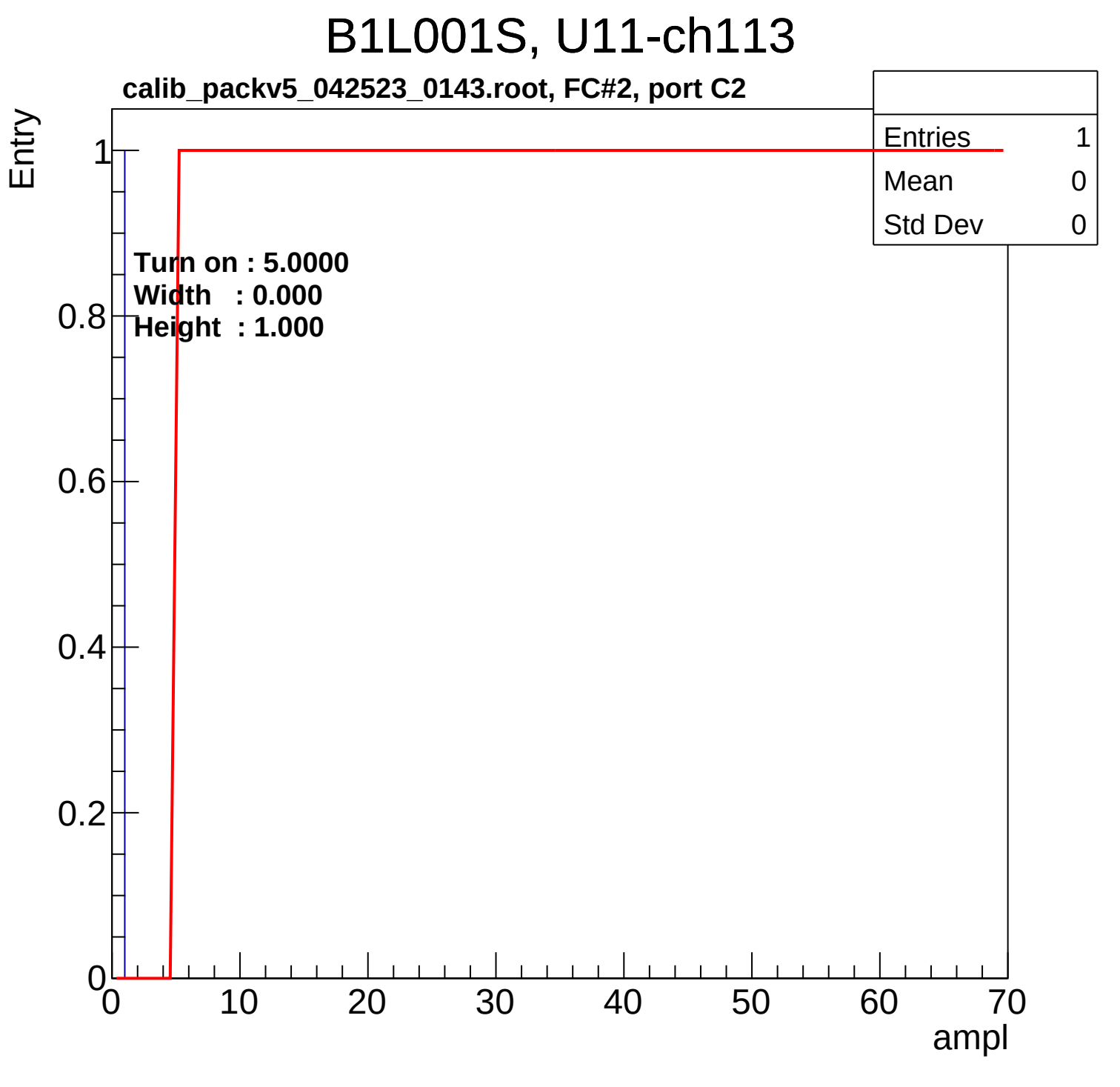

B1L001S, U11-ch108
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

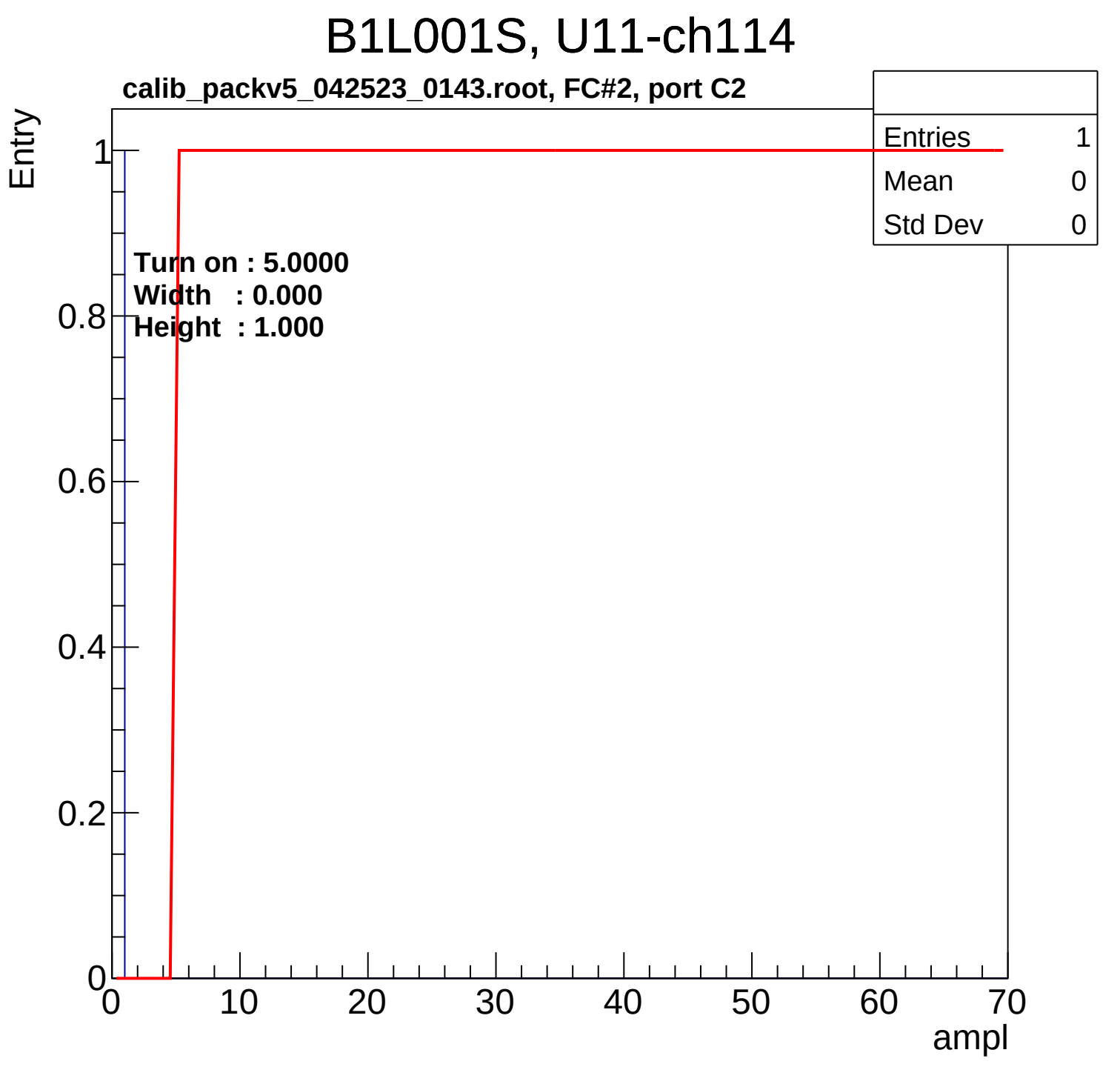

B1L001S, U11-ch109
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

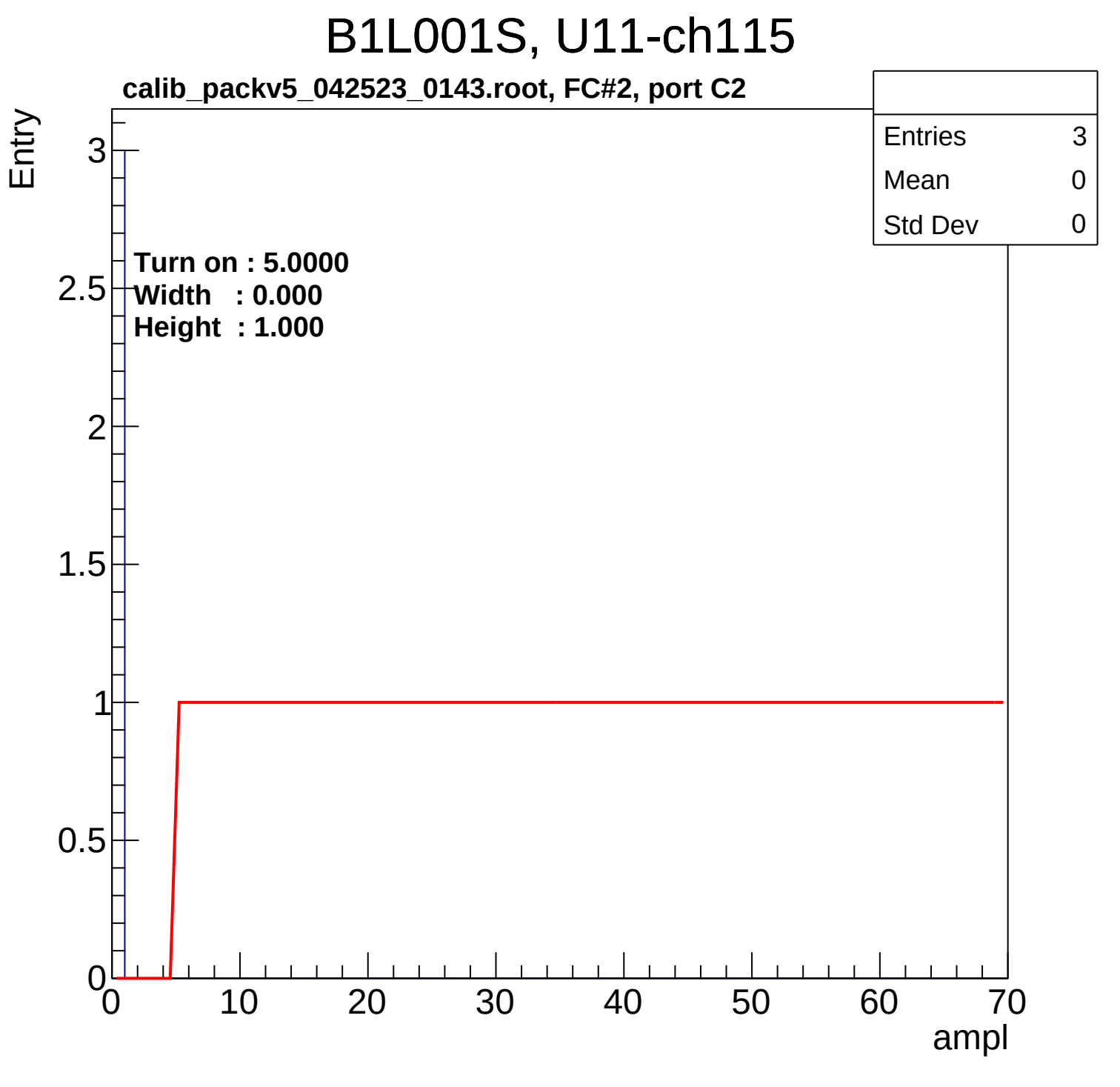

B1L001S, U11-ch110
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

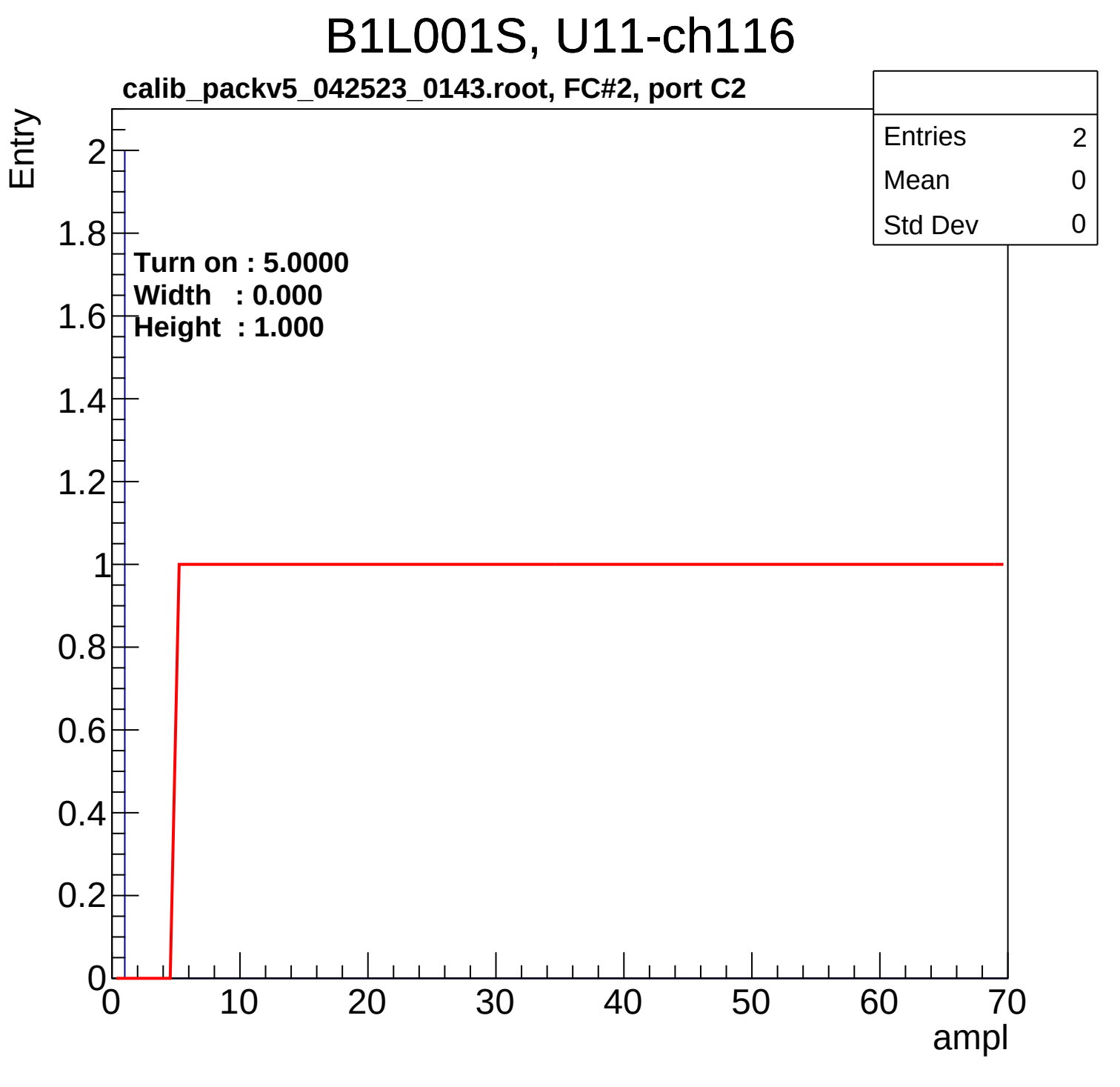

B1L001S, U11-ch111
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

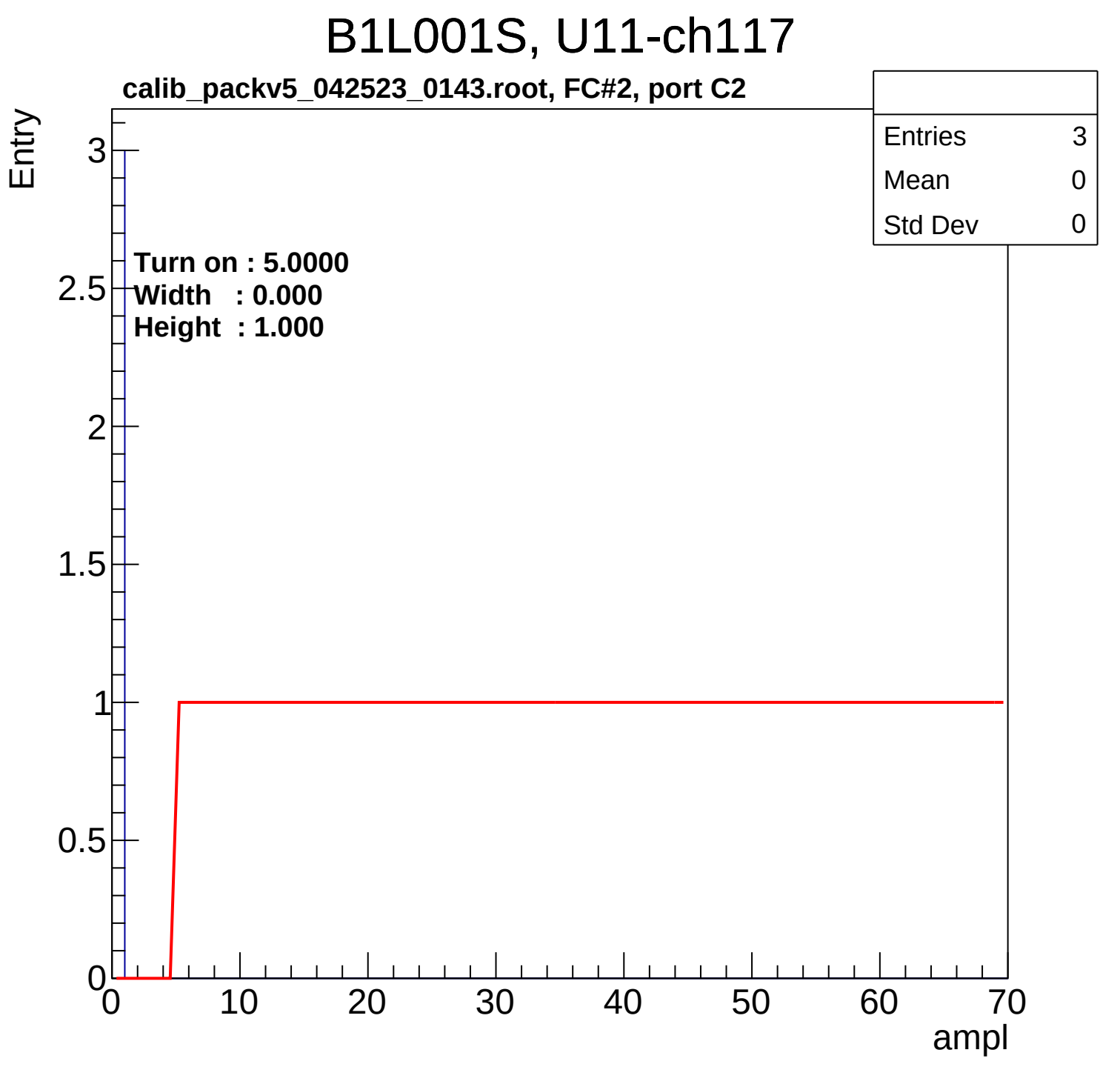

B1L001S, U11-ch112
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

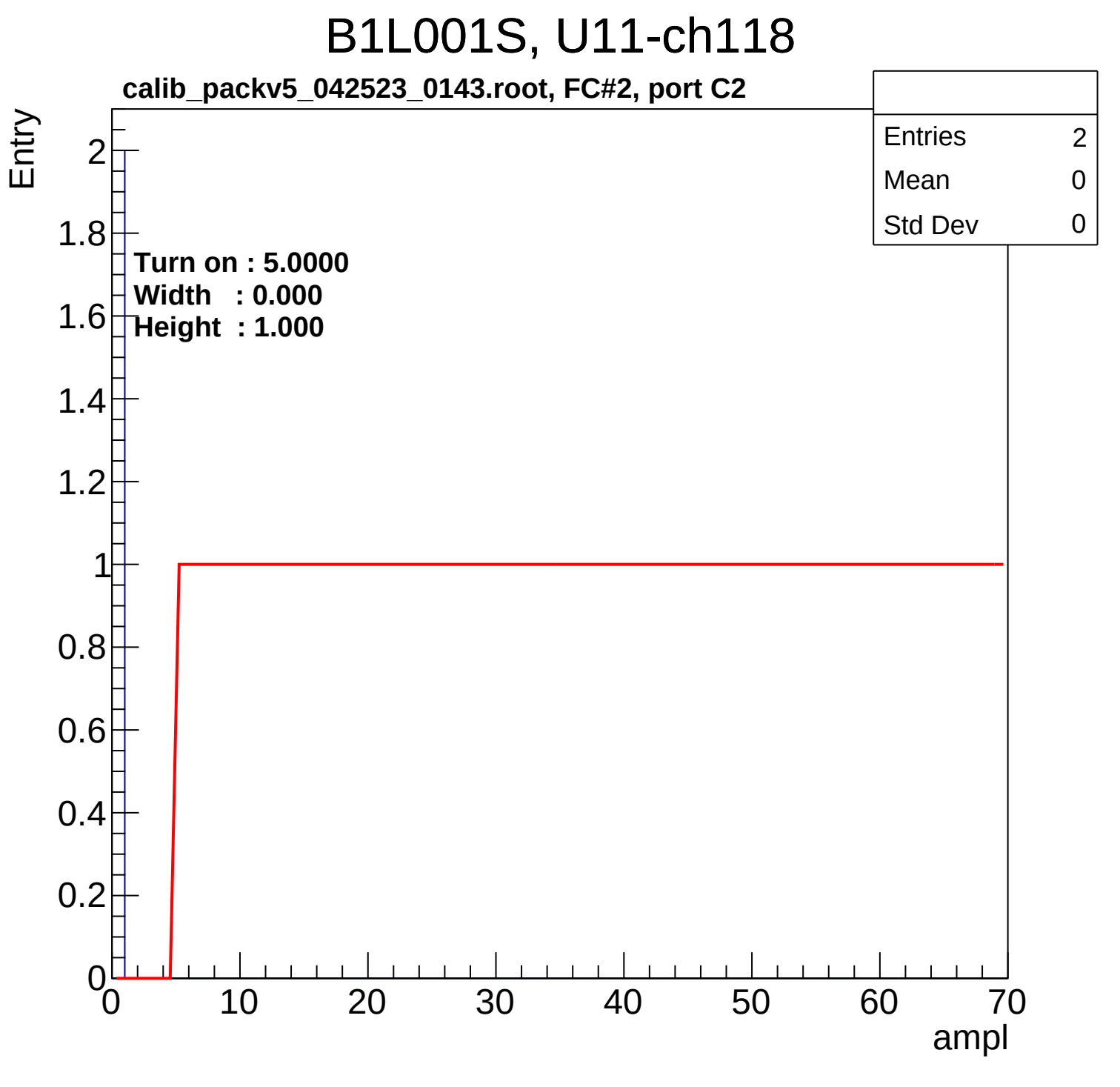

B1L001S, U11-ch113
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

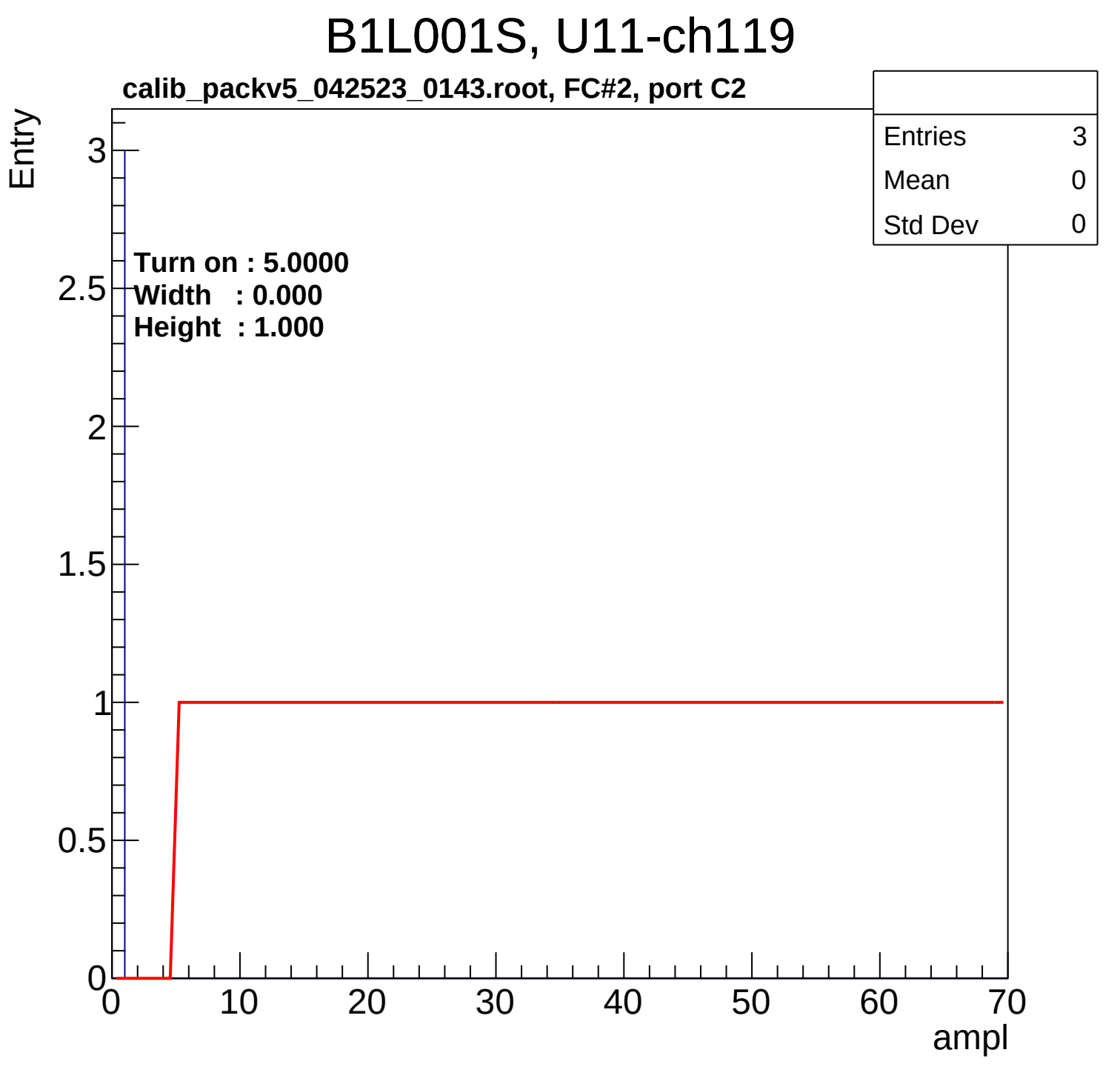

B1L001S, U11-ch114
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

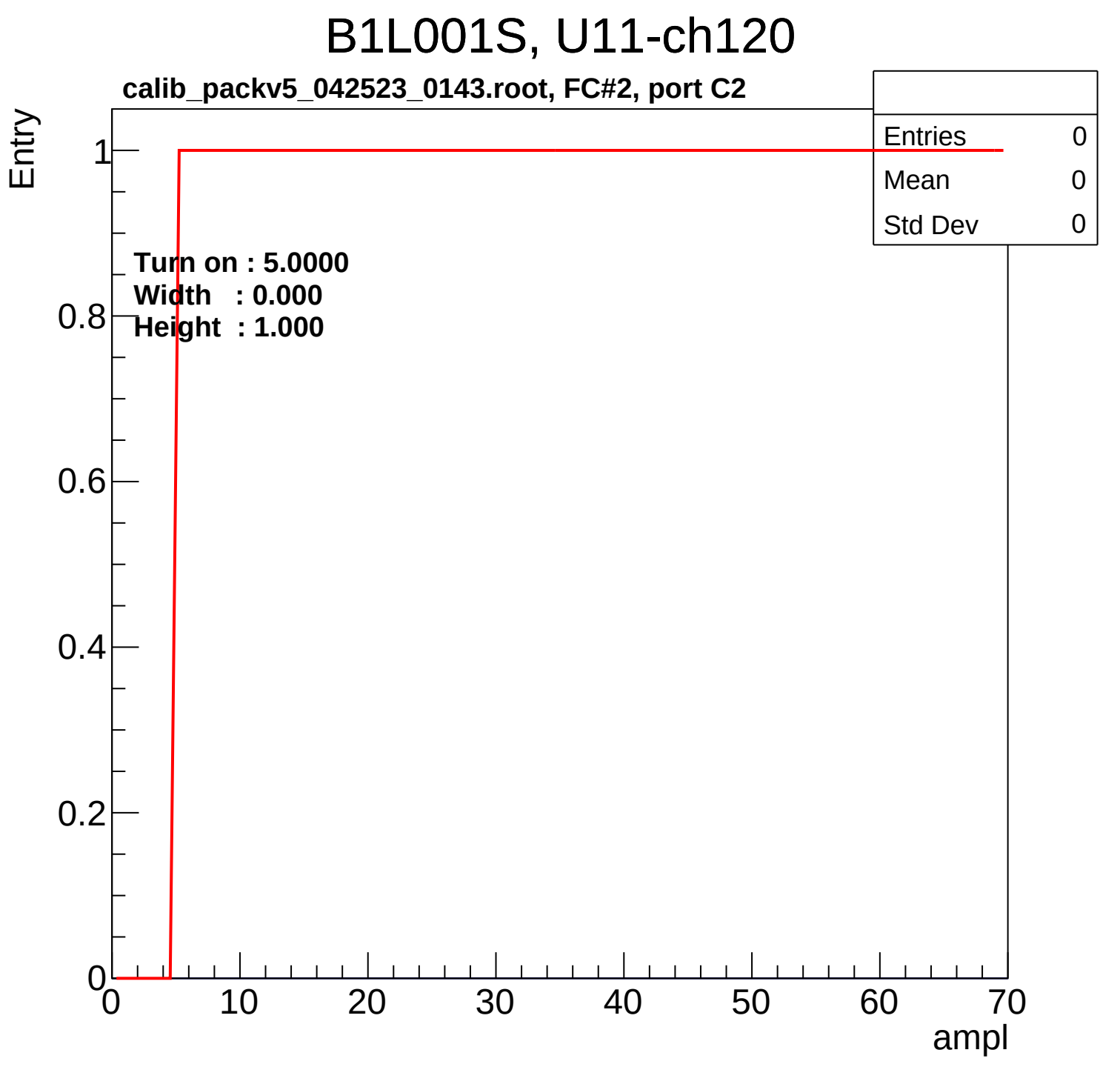

B1L001S, U11-ch115
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

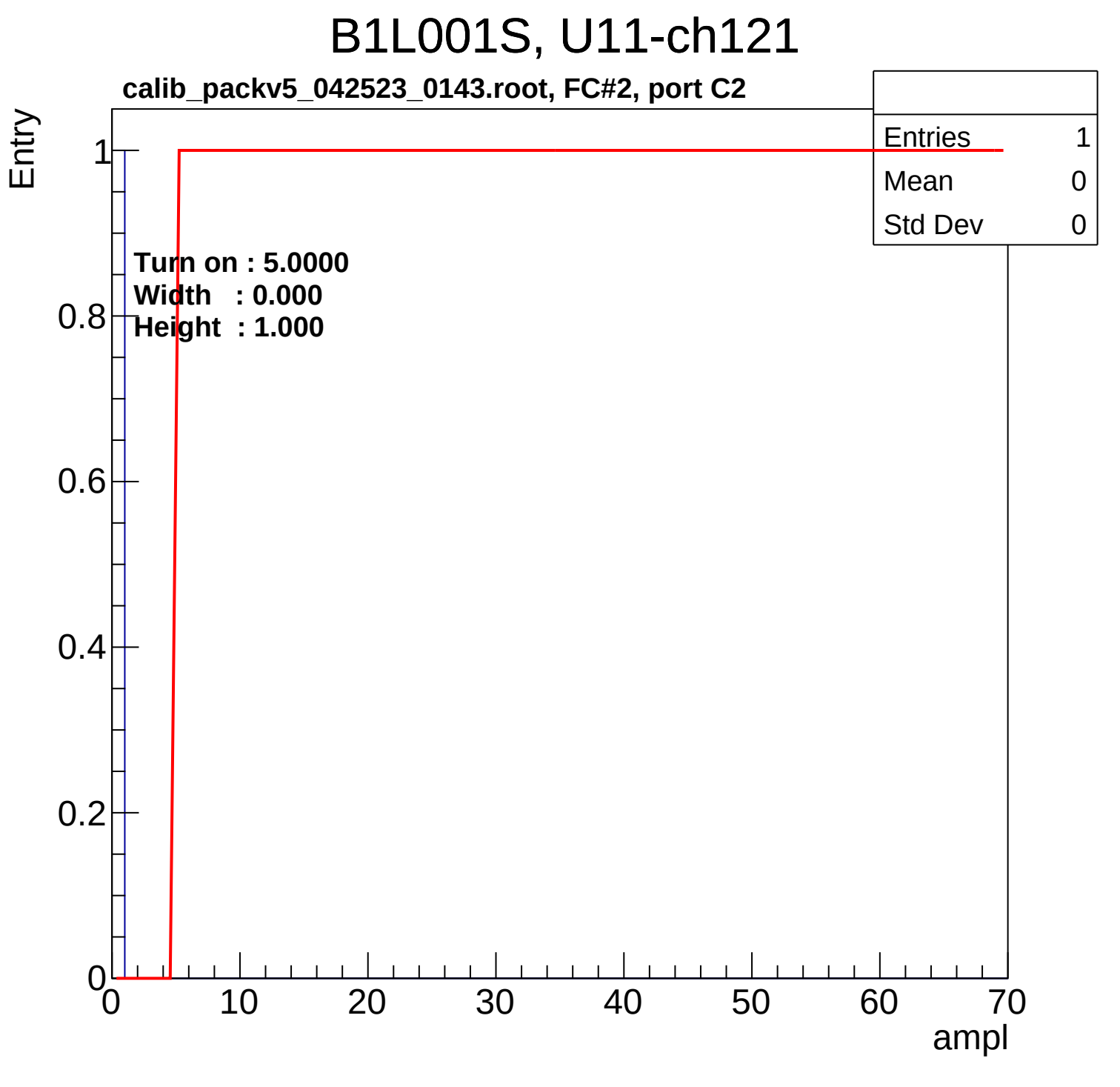

B1L001S, U11-ch116
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

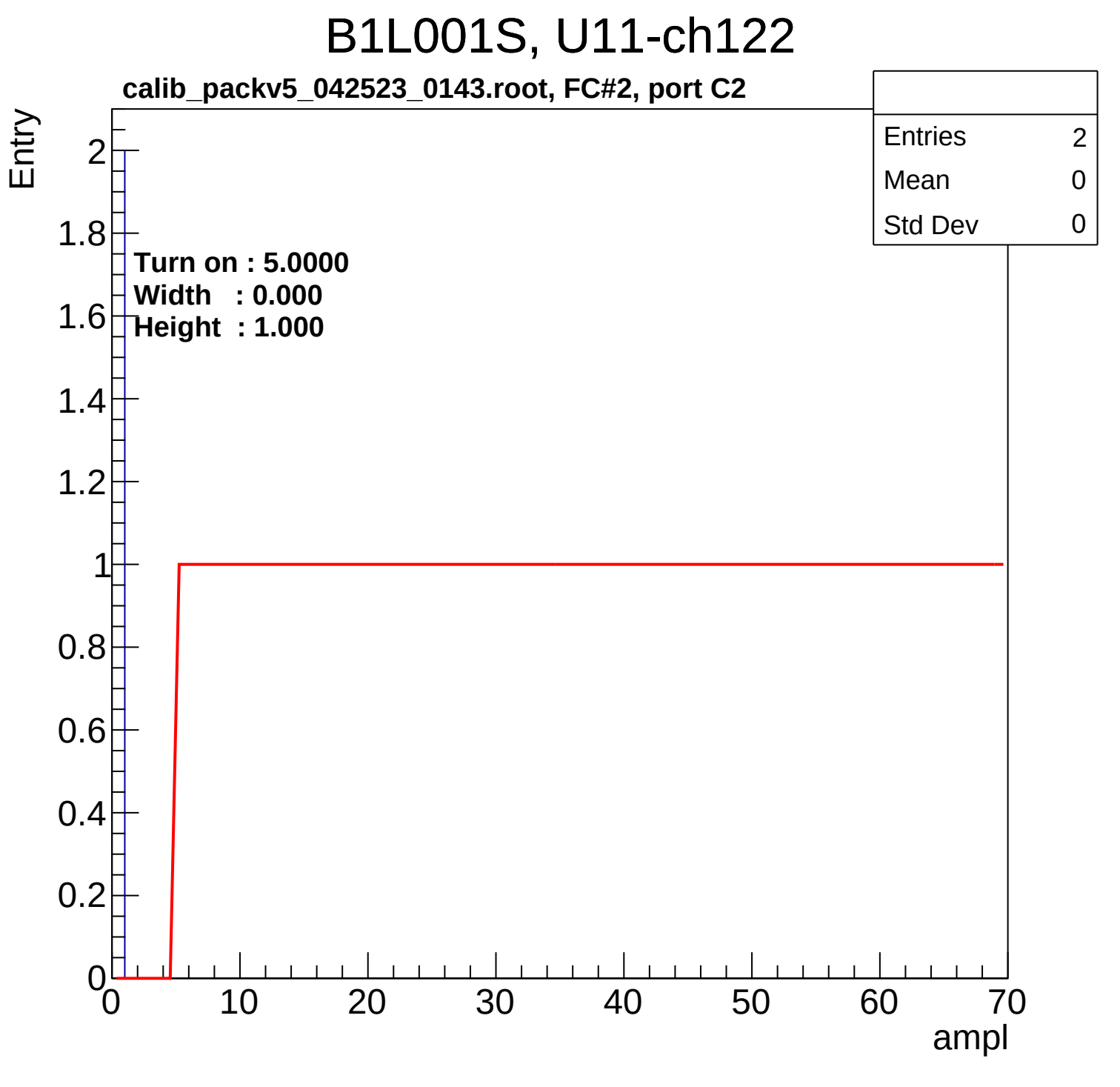

B1L001S, U11-ch117
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

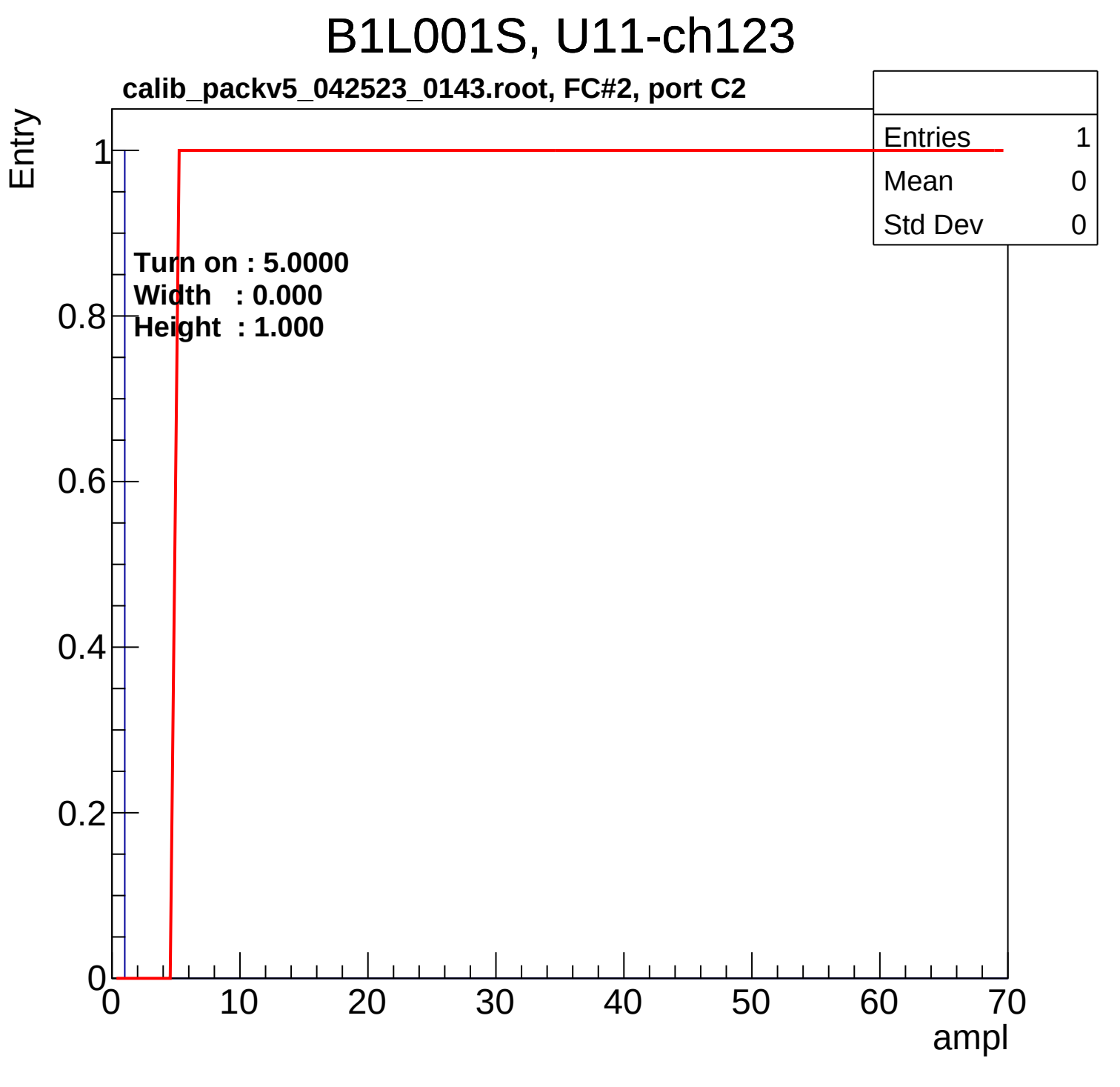

B1L001S, U11-ch118
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

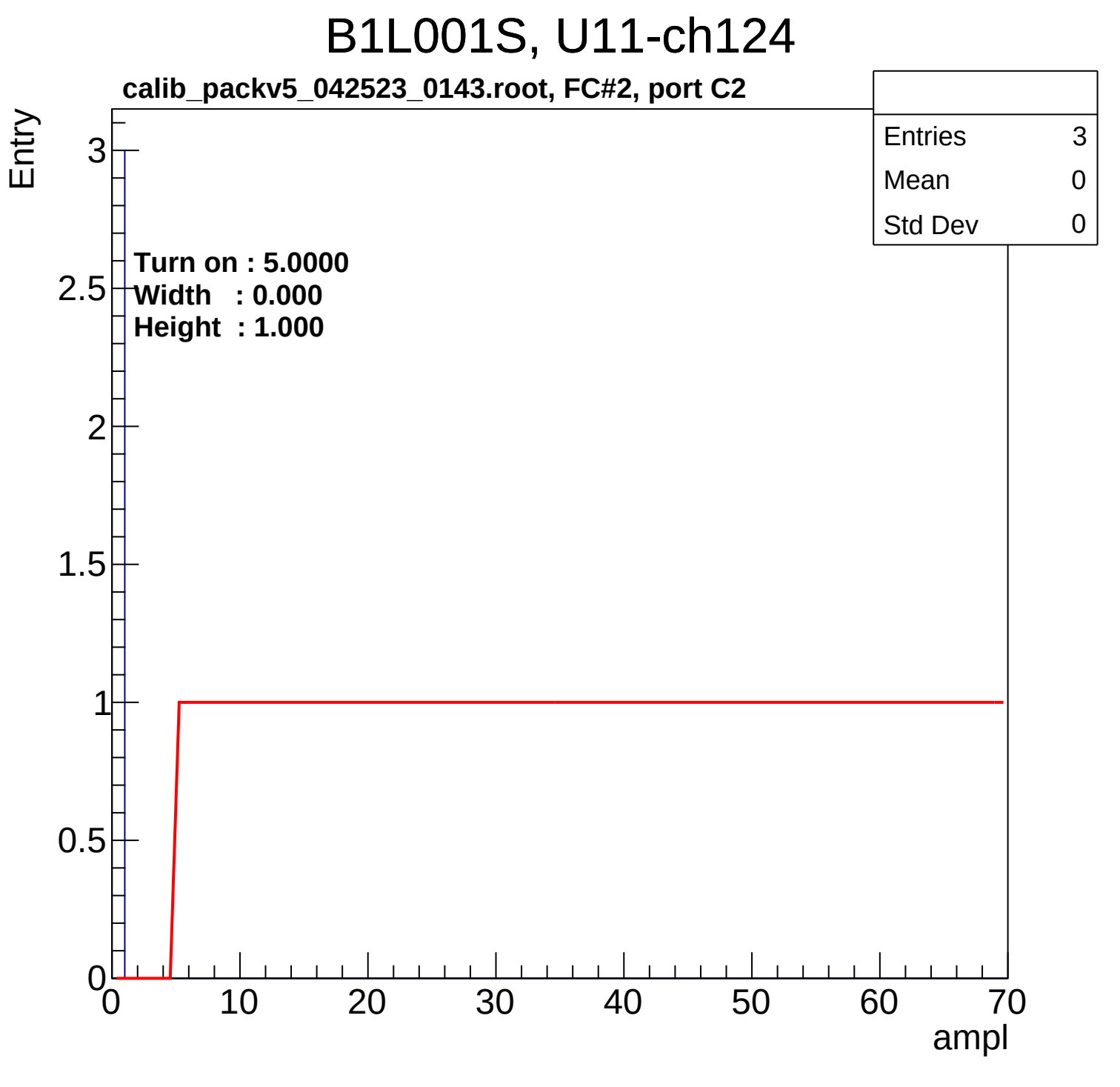

B1L001S, U11-ch119
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

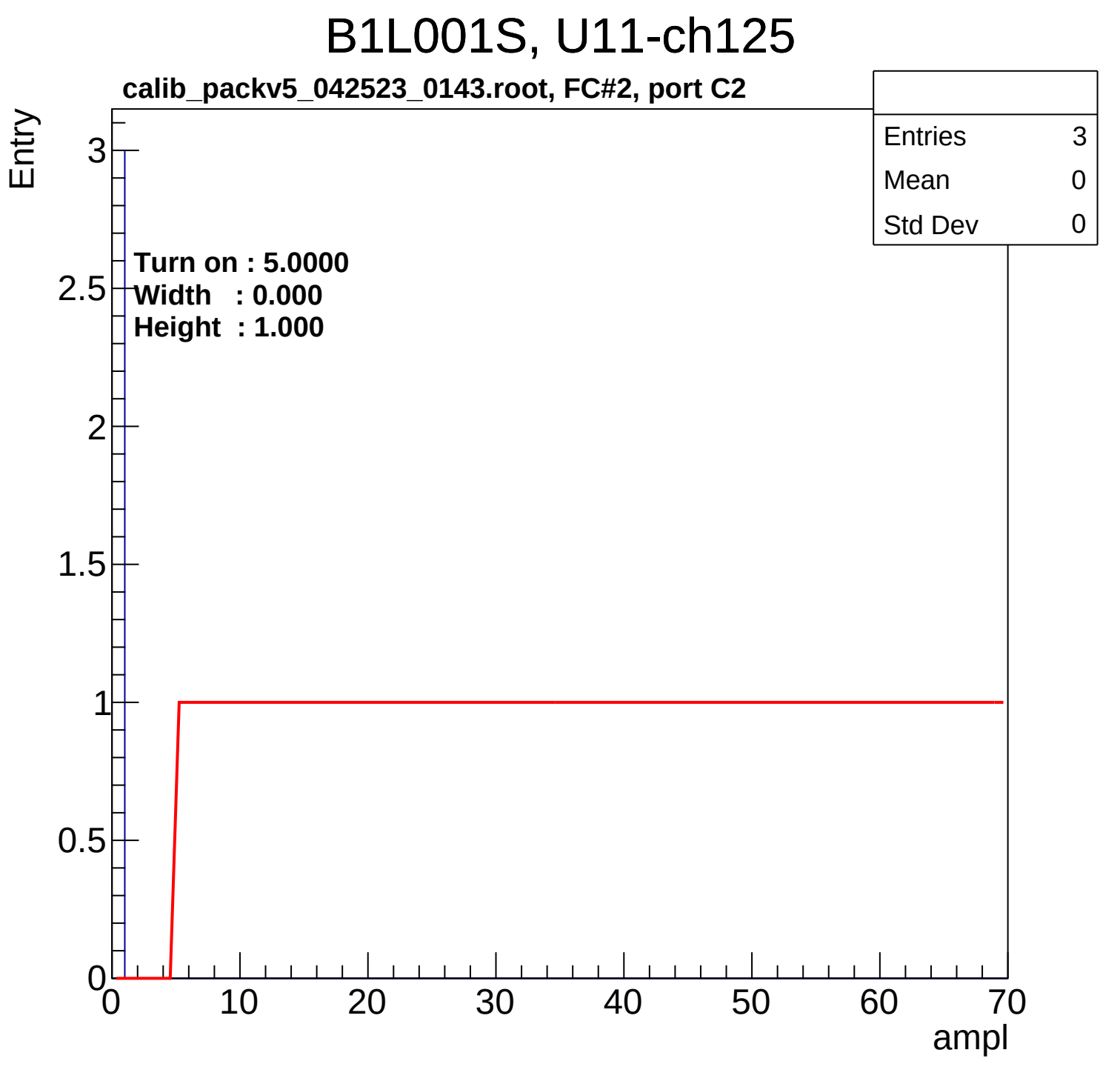

B1L001S, U11-ch120
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

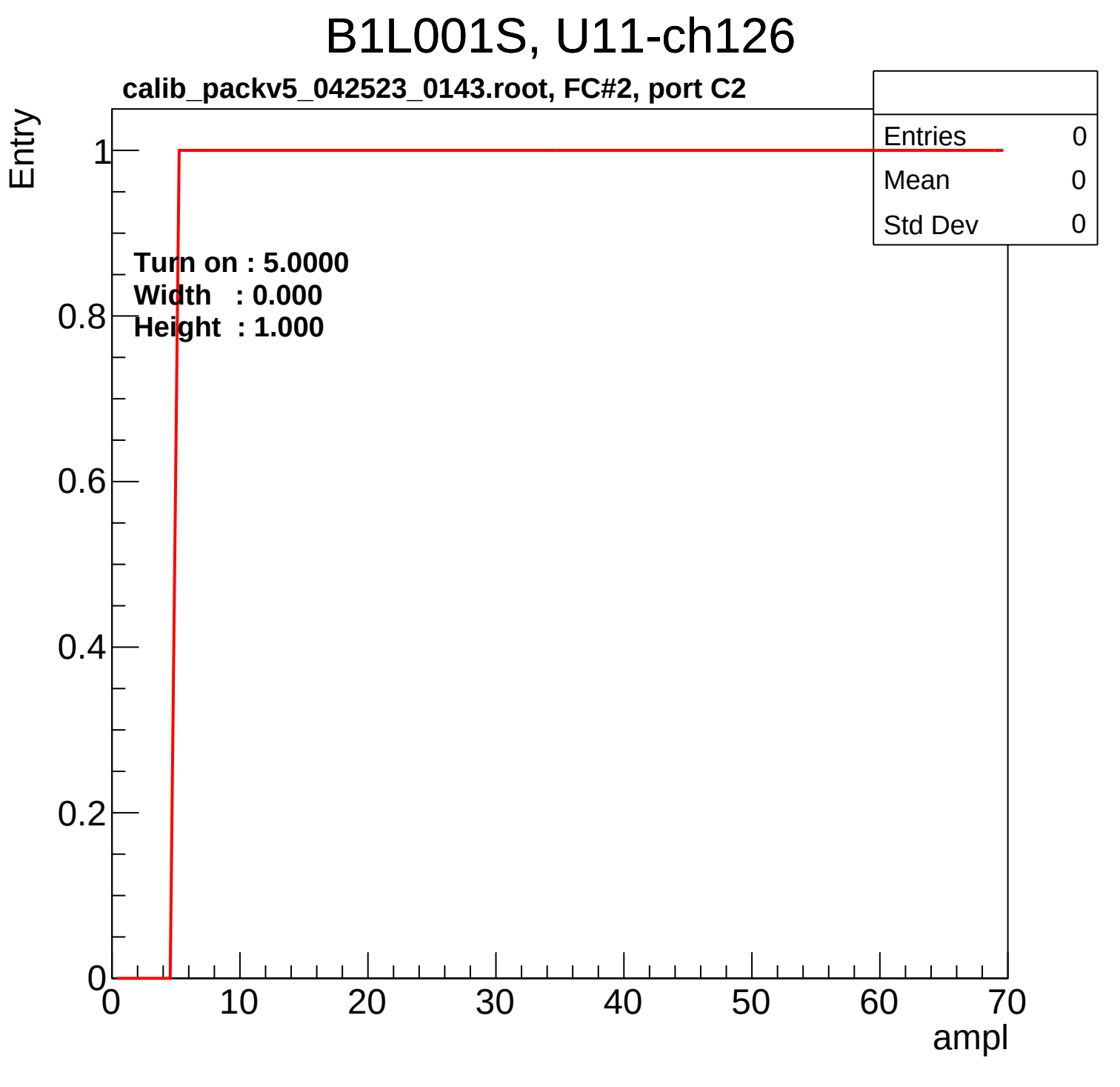

B1L001S, U11-ch121
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

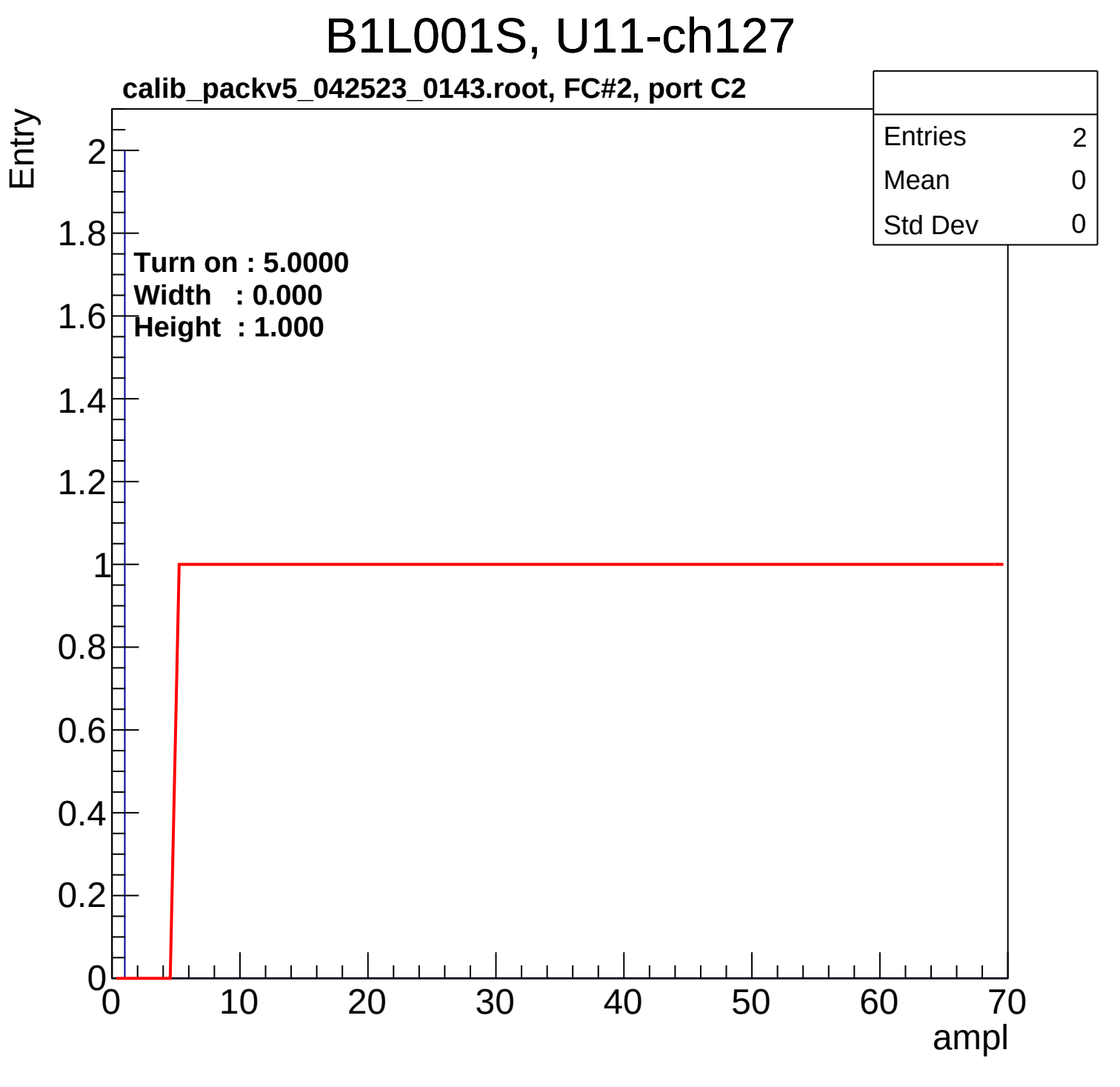

B1L001S, U11-ch122
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

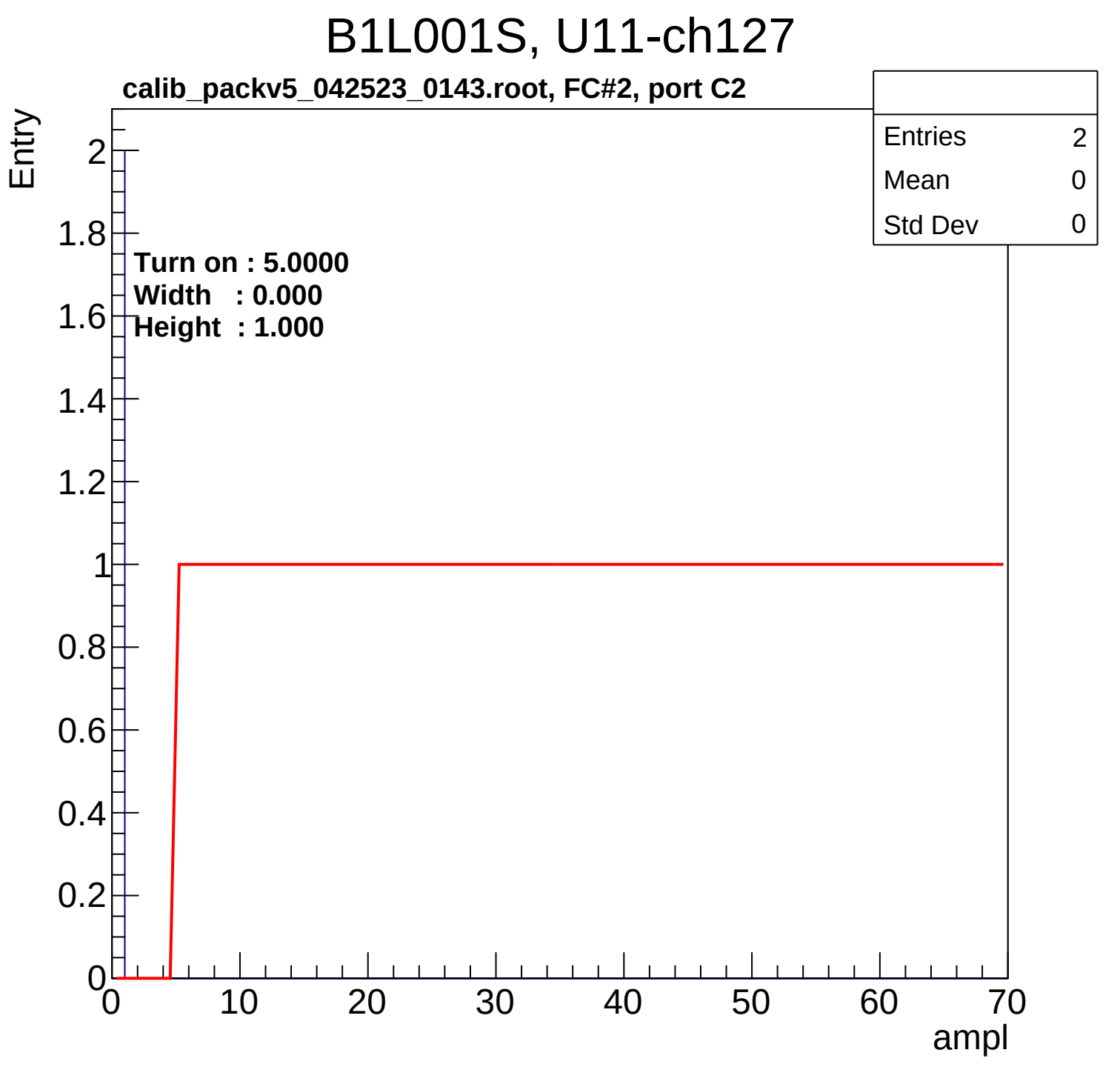

B1L001S, U11-ch123
calib_packv5_042523_0143.root, FC#2, port C2
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L001S, U11-ch124
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L001S, U11-ch125
calib_packv5_042523_0143.root, FC#2, port C2
Entries 3
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L001S, U11-ch126
calib_packv5_042523_0143.root, FC#2, port C2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L001S, U11-ch127
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L001S, U11-ch127
calib_packv5_042523_0143.root, FC#2, port C2
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70