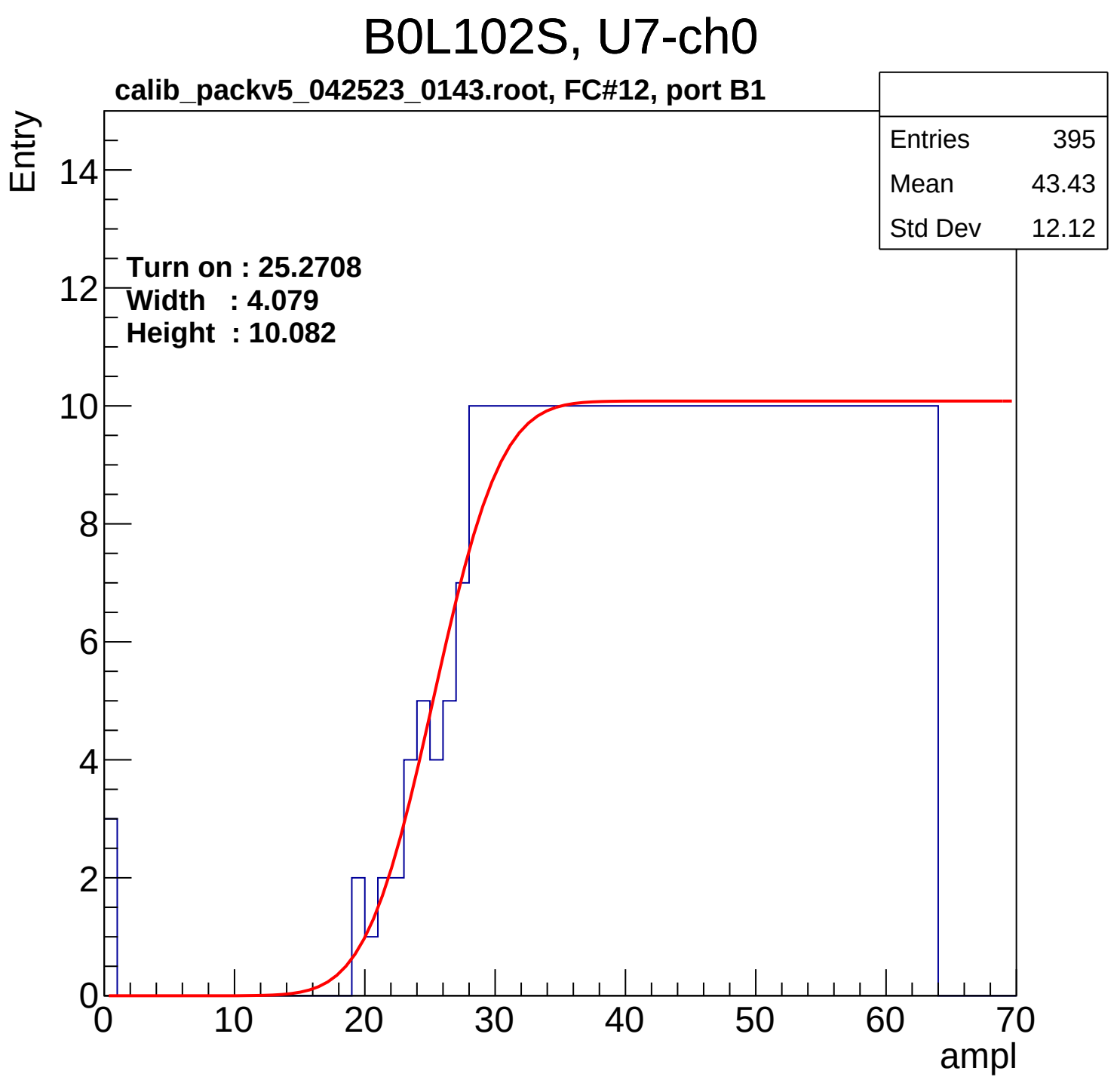
B0L102S, U7-ch0
calib_packv5_042523_0143.root, FC#12, port B1
Entries 395
Mean 43.43
Std Dev 12.12
Turn on : 25.2708
Width : 4.079
Height : 10.082
Entry
ampl
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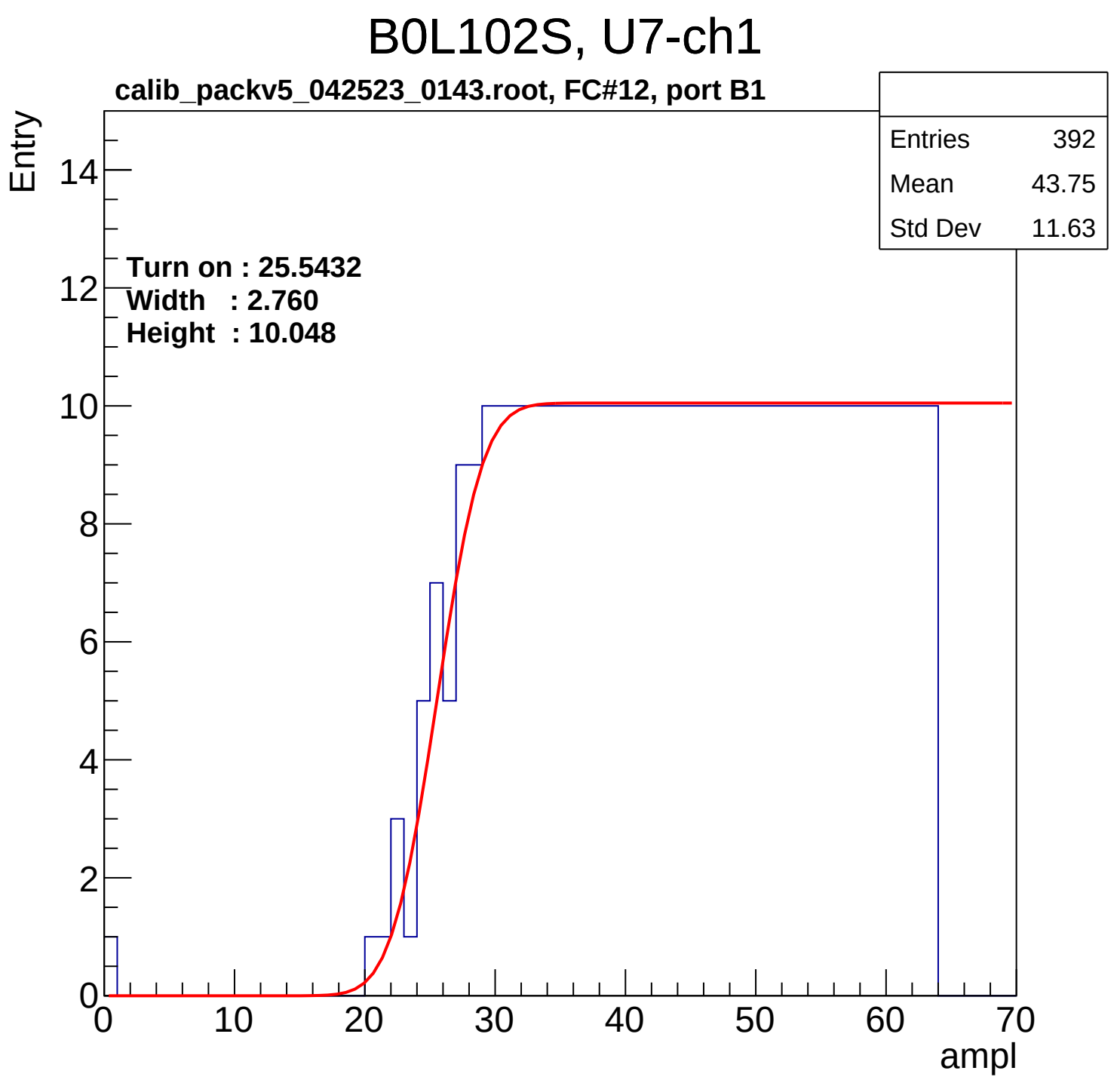
B0L102S, U7-ch1
calib_packv5_042523_0143.root, FC#12, port B1
Entries 392
Mean 43.75
Std Dev 11.63
Turn on : 25.5432
Width : 2.760
Height : 10.048
Entry
ampl
0
2
4
6
8
10
12
14
0
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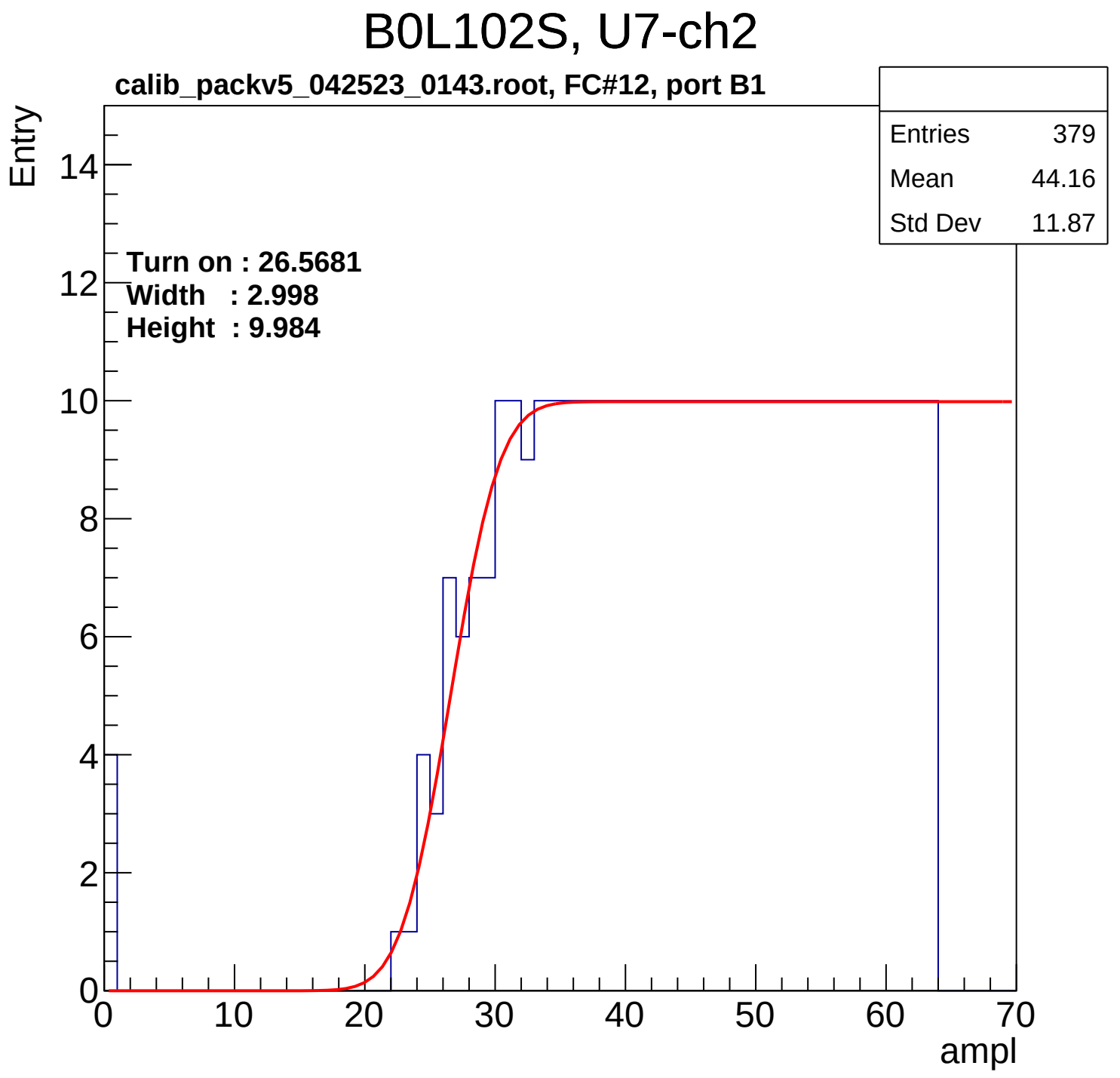
B0L102S, U7-ch2
calib_packv5_042523_0143.root, FC#12, port B1
Entries 379
Mean 44.16
Std Dev 11.87
Turn on : 26.5681
Width : 2.998
Height : 9.984
Entry
ampl
0
2
4
6
8
10
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0
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60
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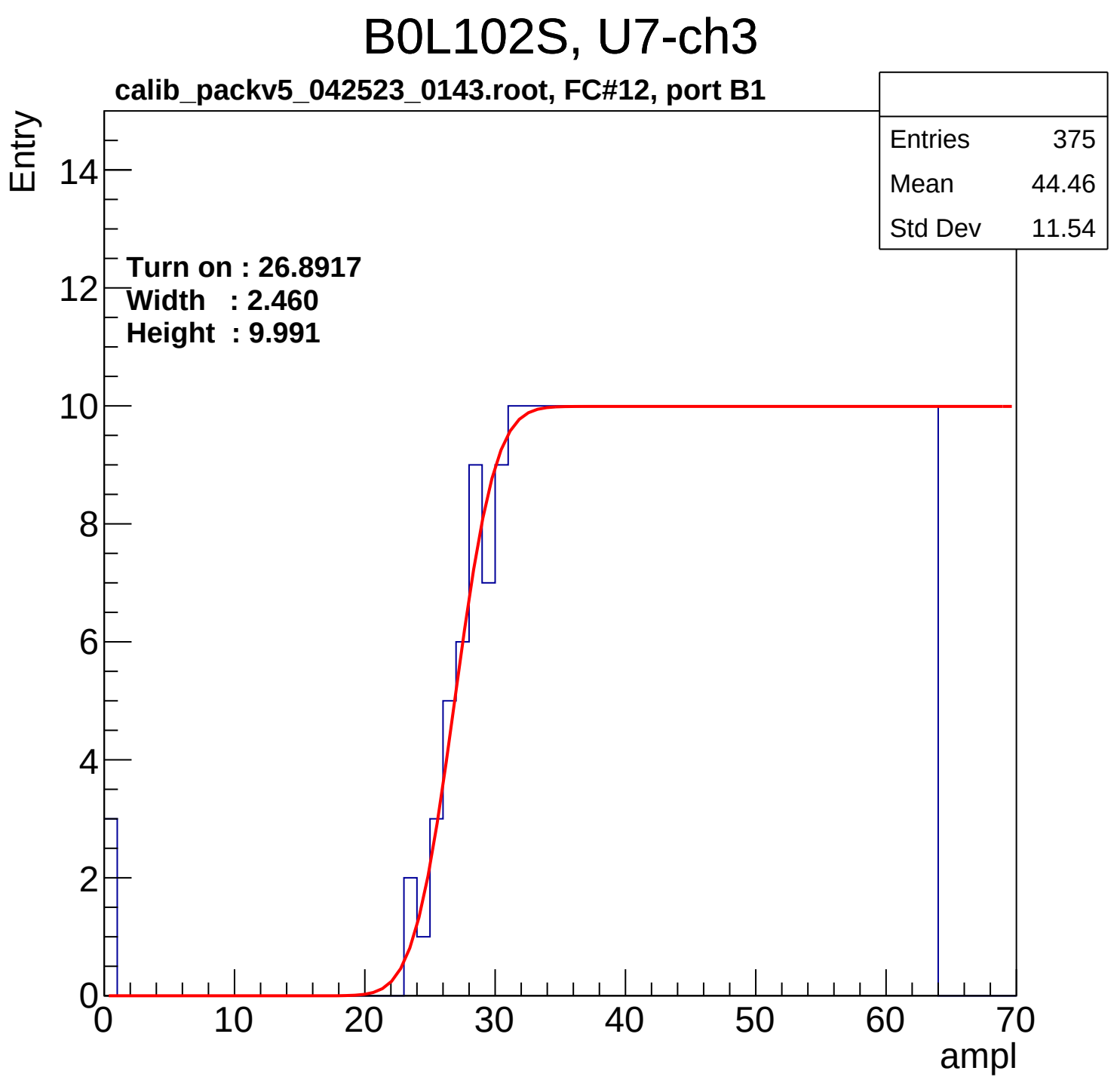
B0L102S, U7-ch3
calib_packv5_042523_0143.root, FC#12, port B1
Entries 375
Mean 44.46
Std Dev 11.54
Turn on : 26.8917
Width : 2.460
Height : 9.991
Entry
ampl
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2
4
6
8
10
12
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0
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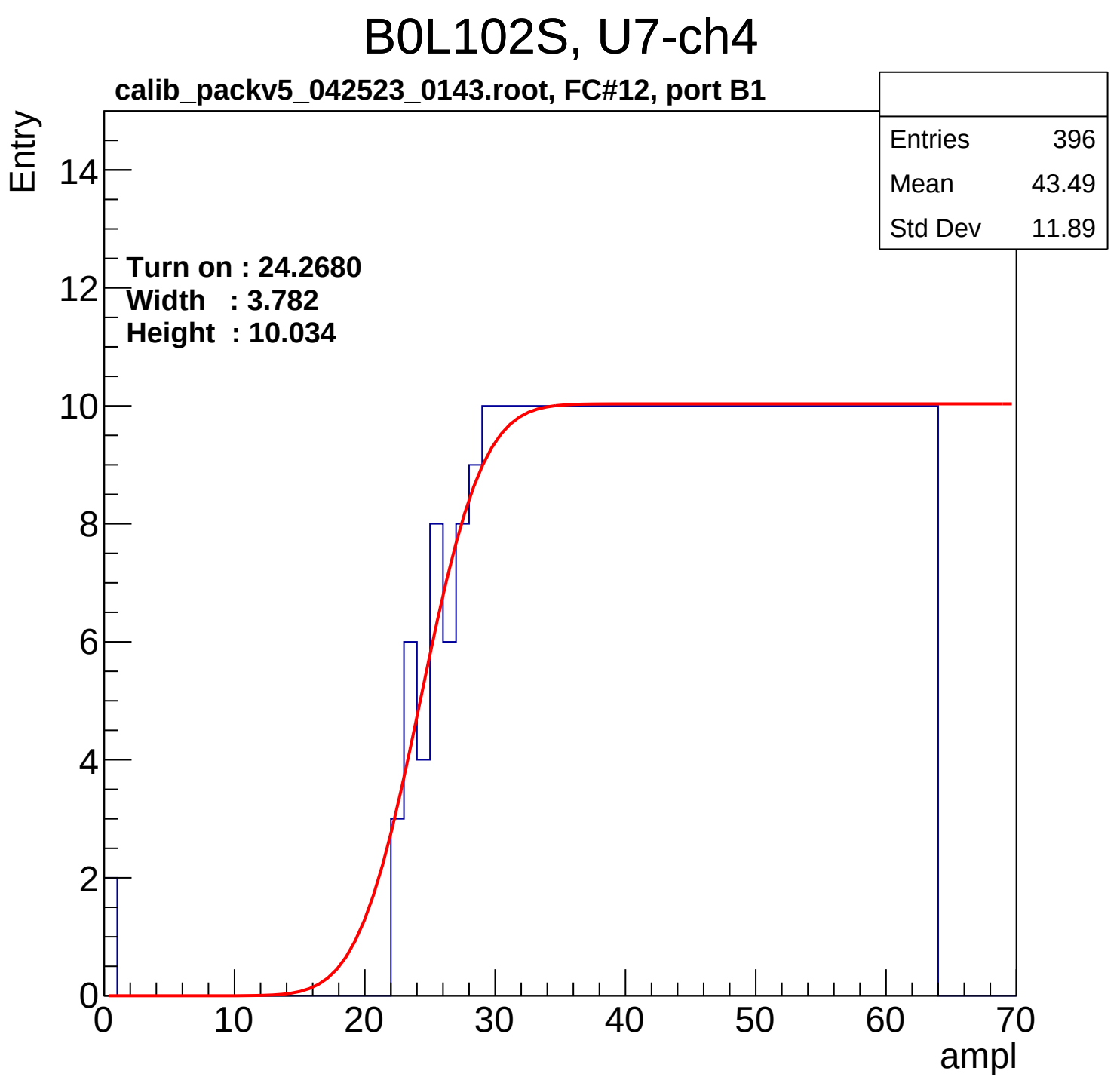
B0L102S, U7-ch4
calib_packv5_042523_0143.root, FC#12, port B1
Entries 396
Mean 43.49
Std Dev 11.89
Turn on : 24.2680
Width : 3.782
Height : 10.034
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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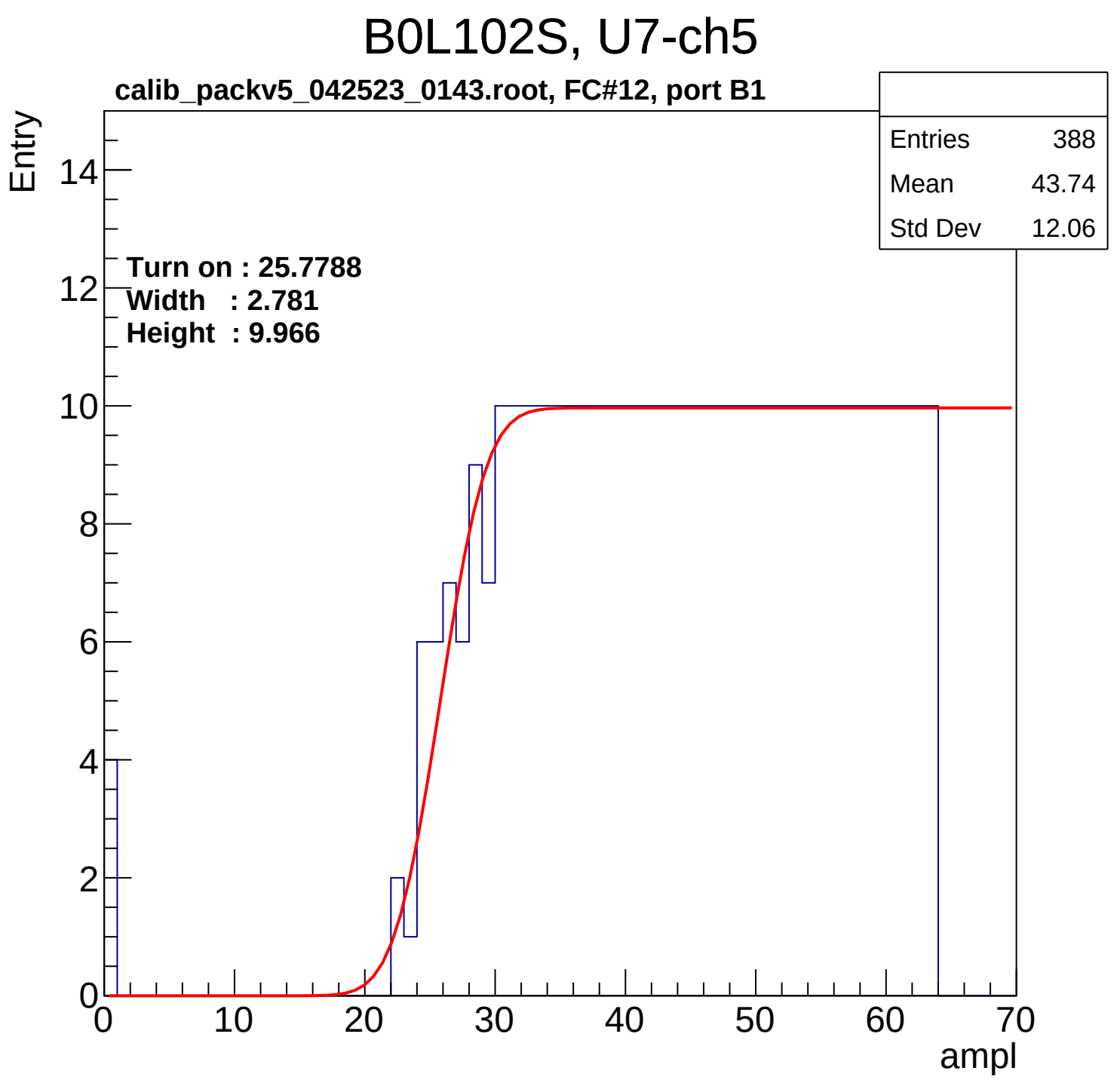
B0L102S, U7-ch5
calib_packv5_042523_0143.root, FC#12, port B1
Entries 388
Mean 43.74
Std Dev 12.06
Turn on : 25.7788
Width : 2.781
Height : 9.966
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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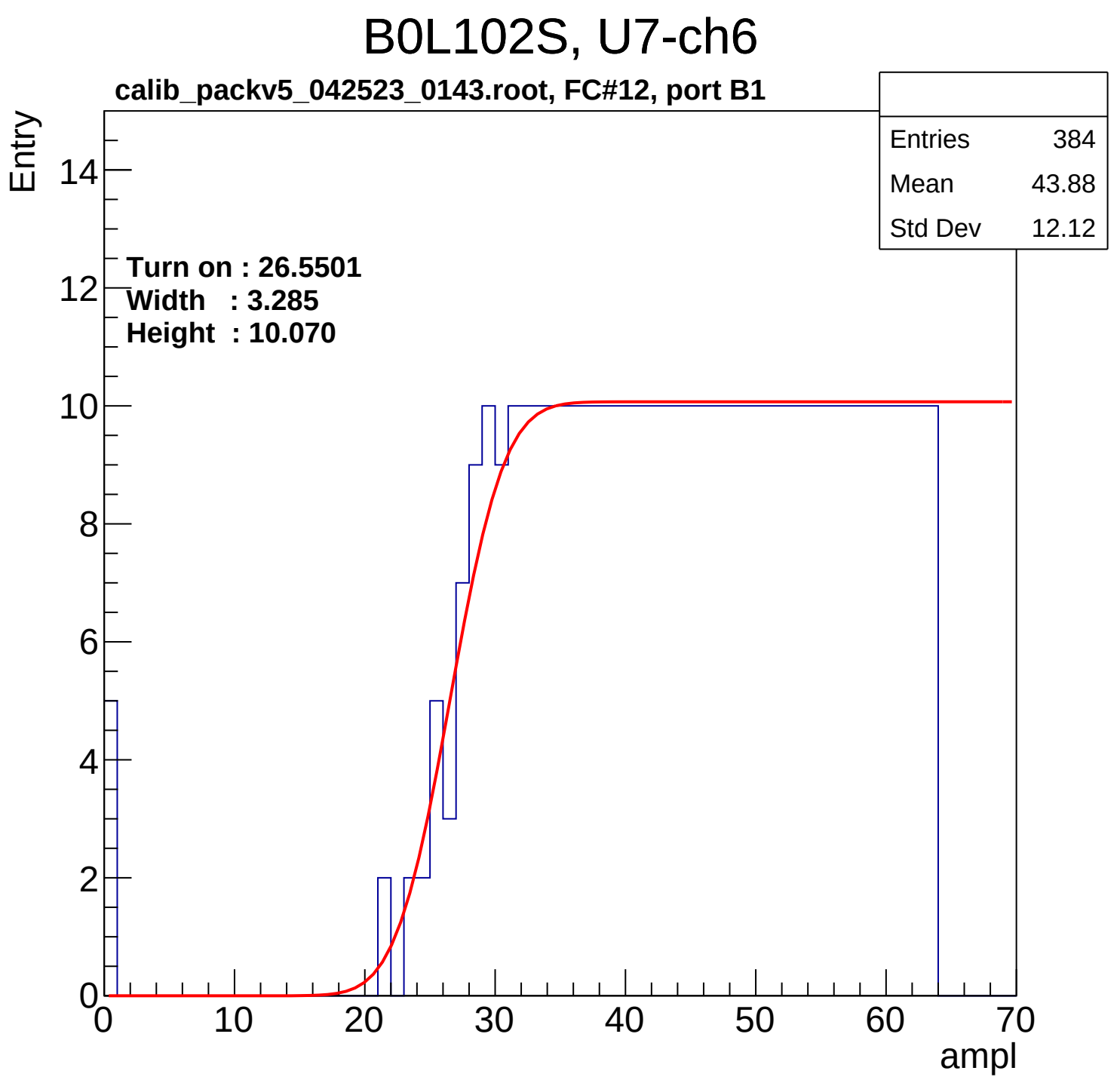
B0L102S, U7-ch6
calib_packv5_042523_0143.root, FC#12, port B1
Entries 384
Mean 43.88
Std Dev 12.12
Turn on : 26.5501
Width : 3.285
Height : 10.070
Entry
ampl
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2
4
6
8
10
12
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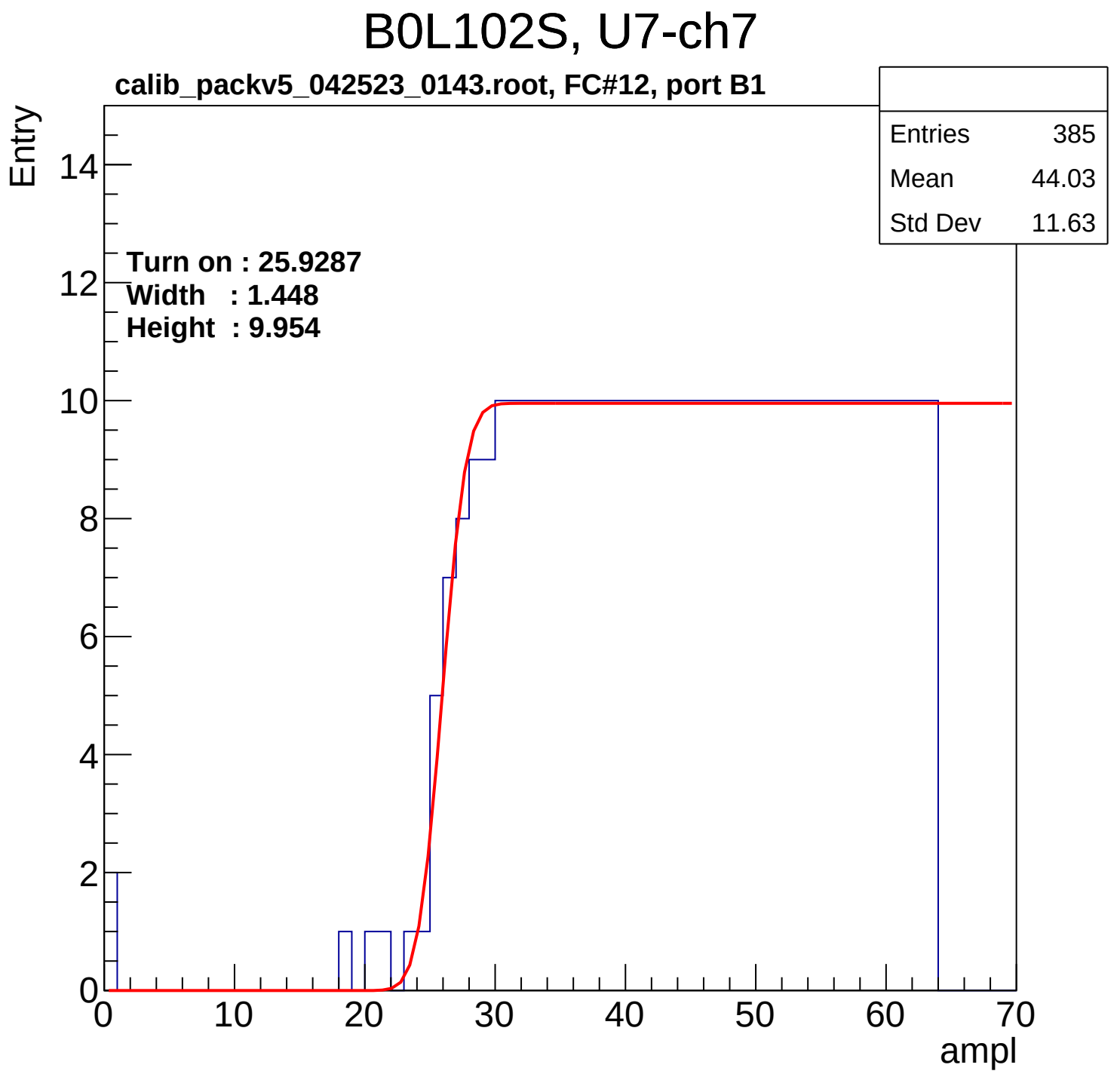
B0L102S, U7-ch7
calib_packv5_042523_0143.root, FC#12, port B1
Entries 385
Mean 44.03
Std Dev 11.63
Turn on : 25.9287
Width : 1.448
Height : 9.954
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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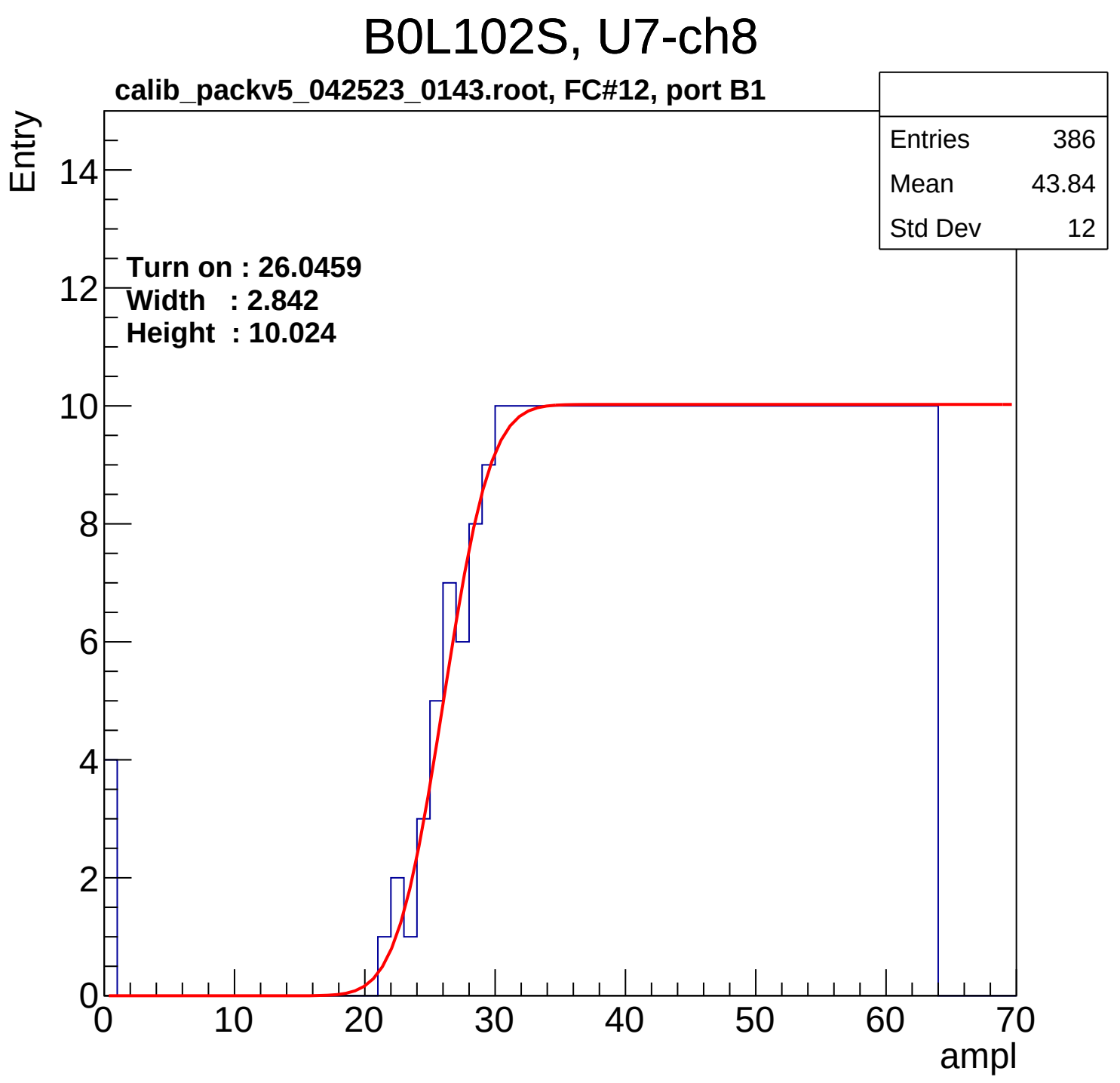
B0L102S, U7-ch8
calib_packv5_042523_0143.root, FC#12, port B1
Entries 386
Mean 43.84
Std Dev 12
Turn on : 26.0459
Width : 2.842
Height : 10.024
Entry
ampl
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2
4
6
8
10
12
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0
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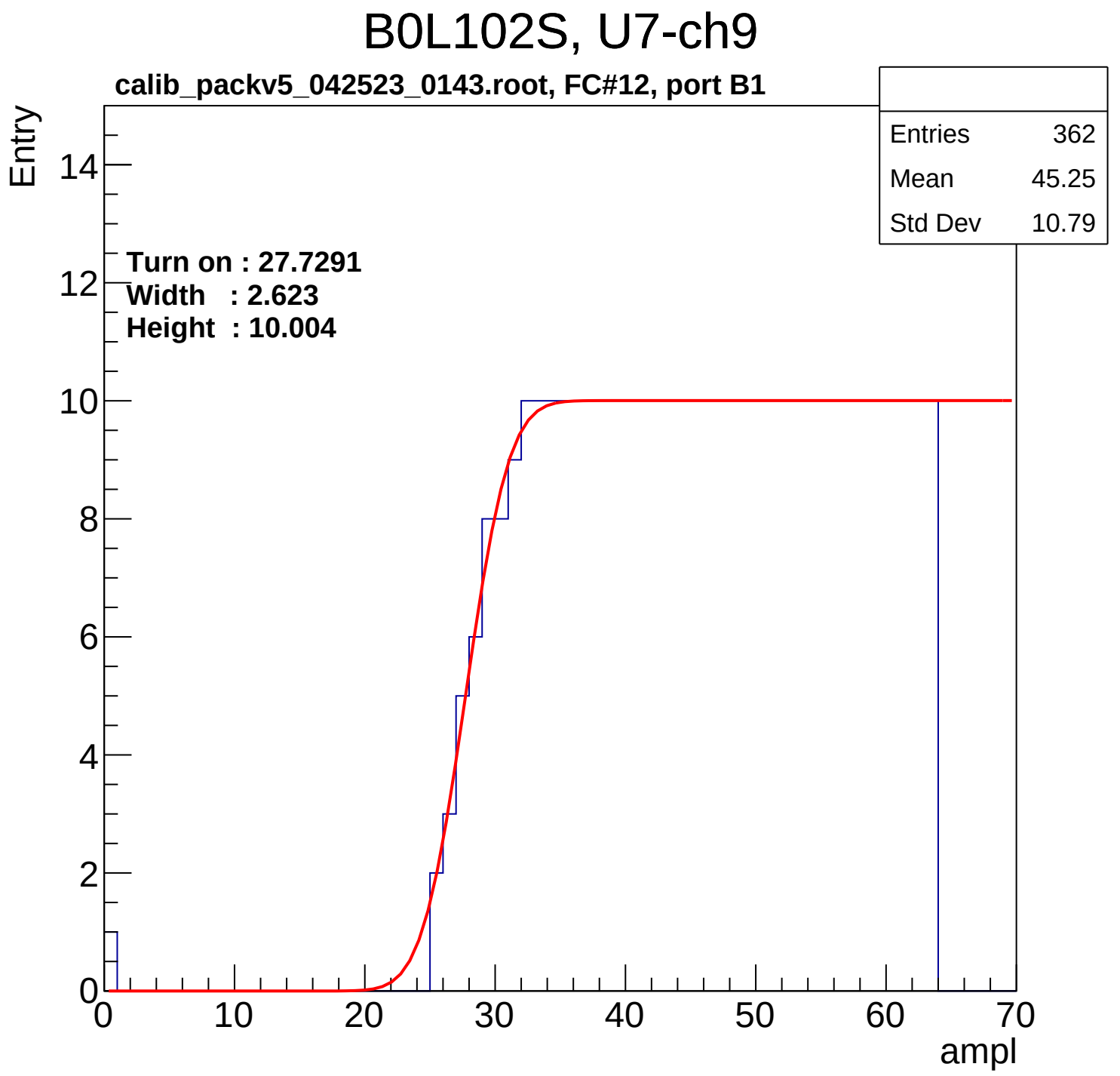
B0L102S, U7-ch9
calib_packv5_042523_0143.root, FC#12, port B1
Entries 362
Mean 45.25
Std Dev 10.79
Turn on : 27.7291
Width : 2.623
Height : 10.004
Entry
ampl
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4
6
8
10
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0
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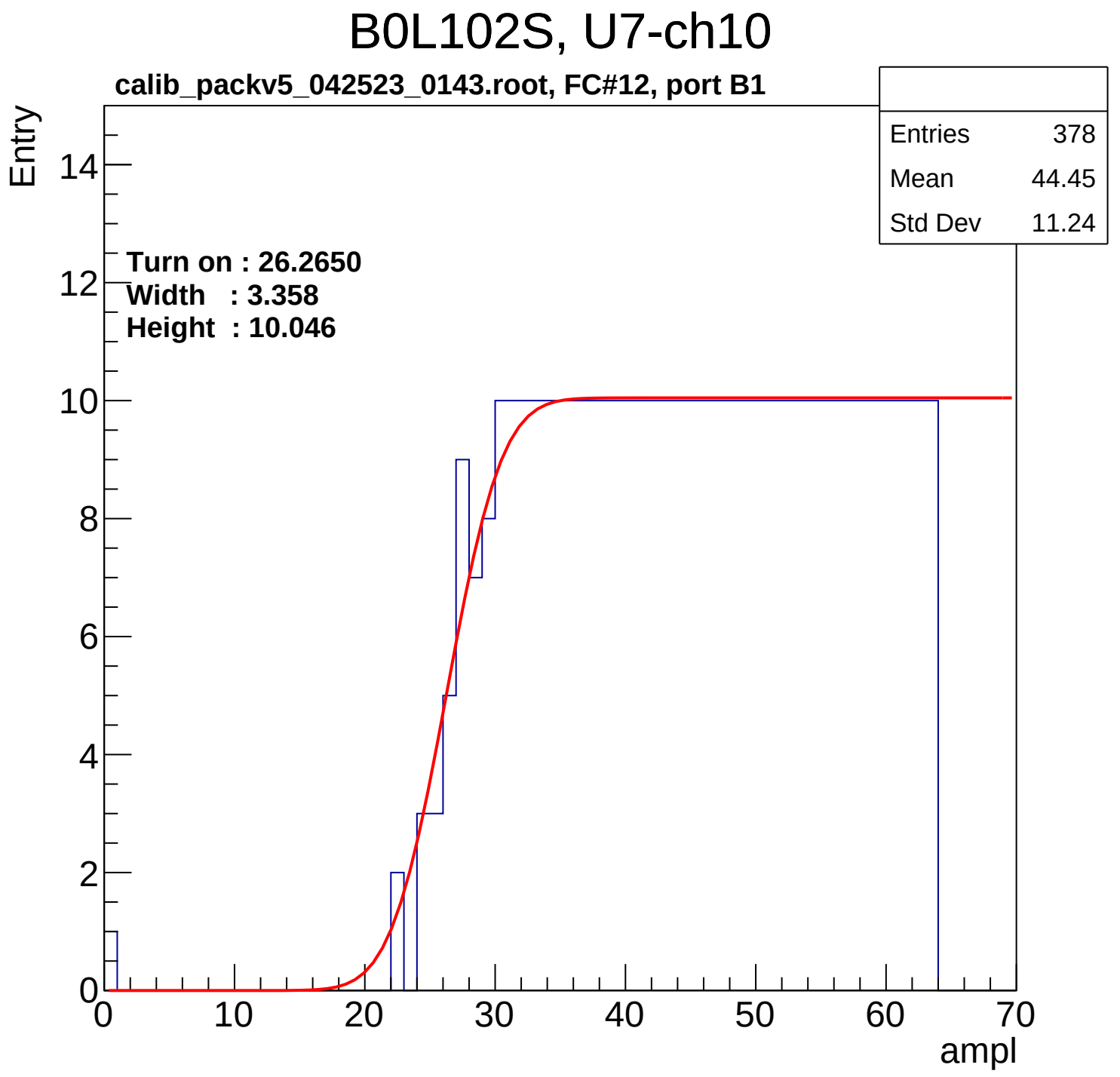
B0L102S, U7-ch10
calib_packv5_042523_0143.root, FC#12, port B1
Entries 378
Mean 44.45
Std Dev 11.24
Turn on : 26.2650
Width : 3.358
Height : 10.046
Entry
ampl
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6
8
10
12
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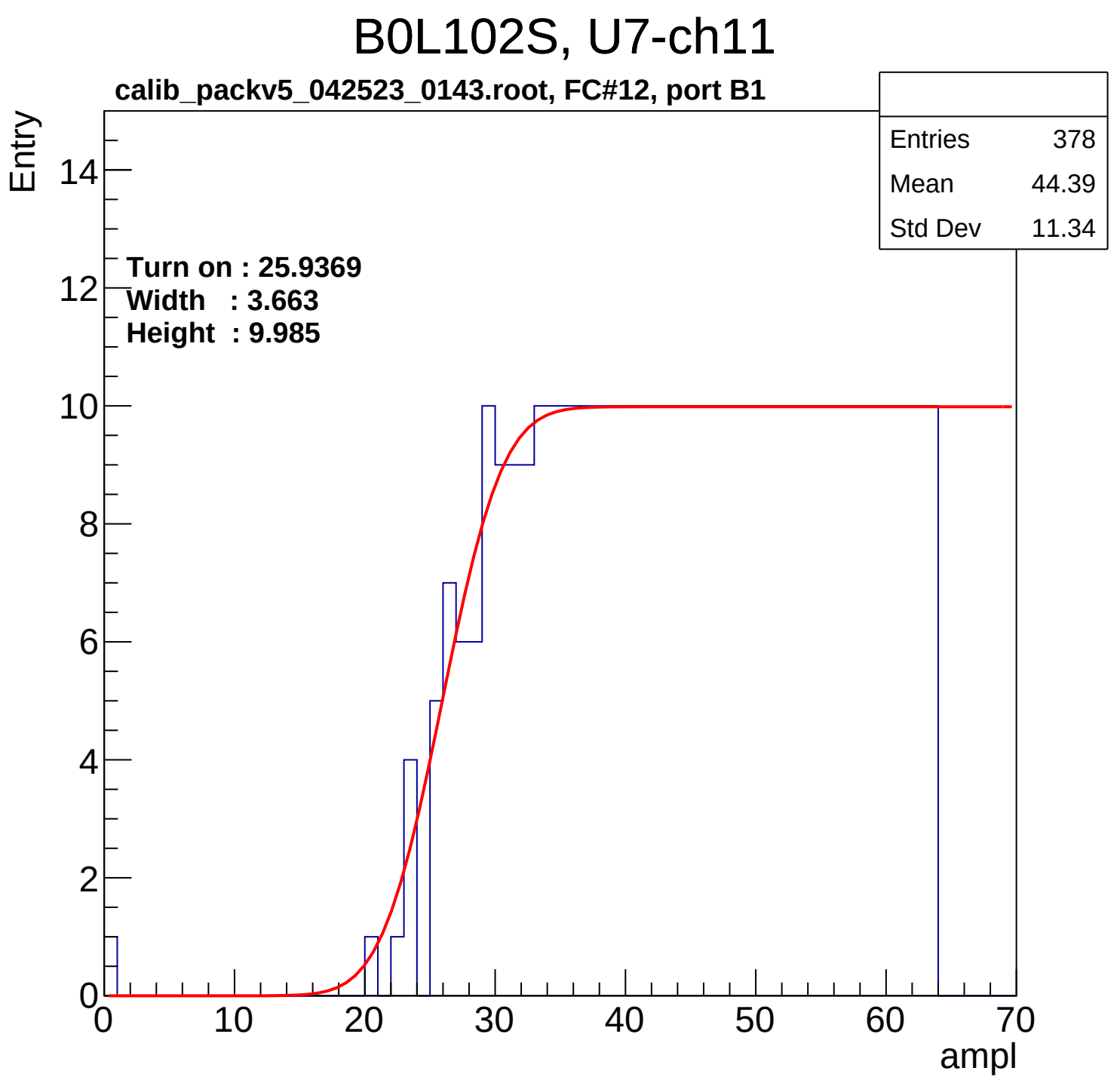
B0L102S, U7-ch11
calib_packv5_042523_0143.root, FC#12, port B1
Entries 378
Mean 44.39
Std Dev 11.34
Turn on : 25.9369
Width : 3.663
Height : 9.985
Entry
ampl
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4
6
8
10
12
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0
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60
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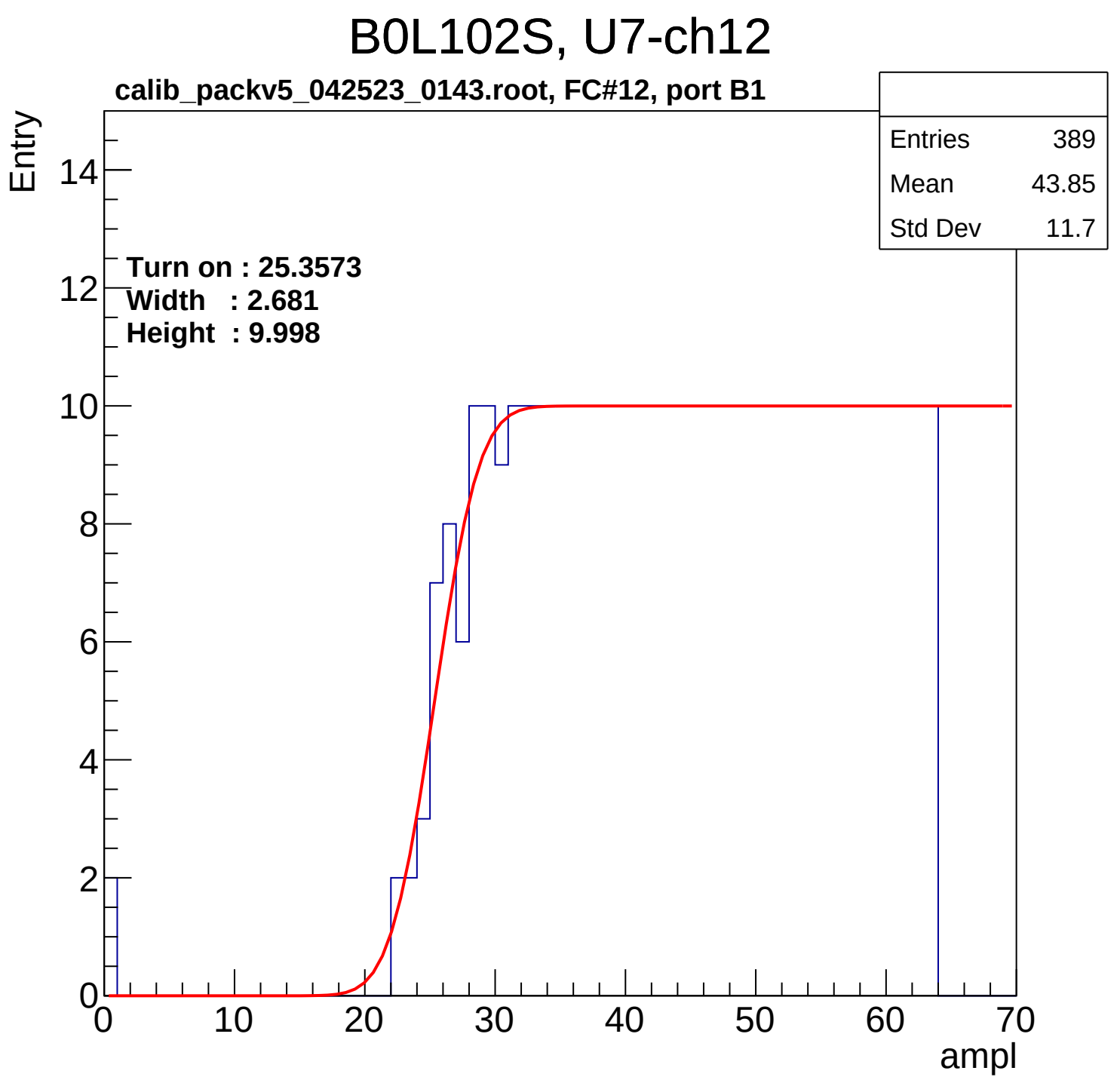
B0L102S, U7-ch12
calib_packv5_042523_0143.root, FC#12, port B1
Entries 389
Mean 43.85
Std Dev 11.7
Turn on : 25.3573
Width : 2.681
Height : 9.998
Entry
ampl
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2
4
6
8
10
12
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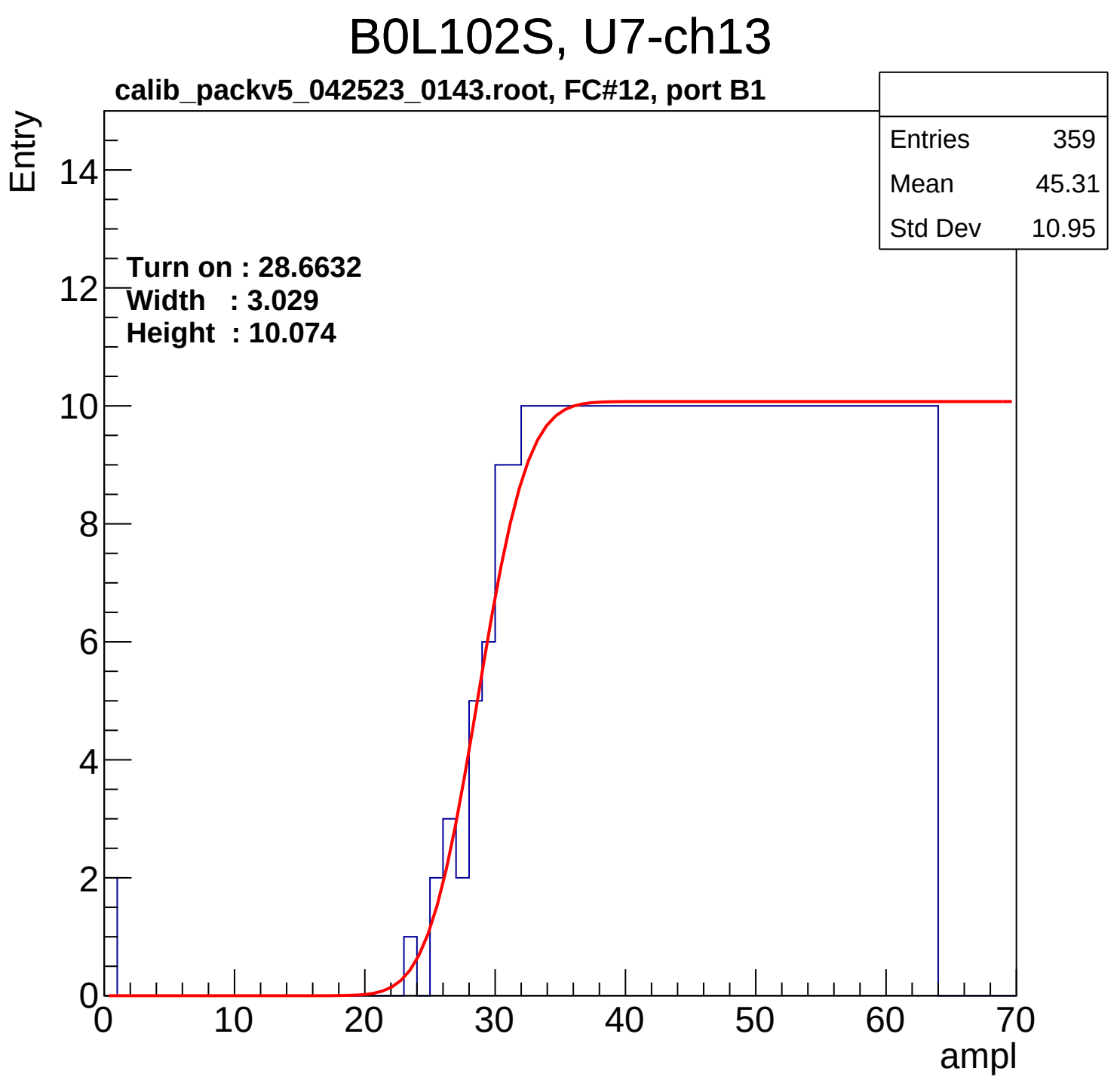
B0L102S, U7-ch13
calib_packv5_042523_0143.root, FC#12, port B1
Entries 359
Mean 45.31
Std Dev 10.95
Turn on : 28.6632
Width : 3.029
Height : 10.074
Entry
ampl
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6
8
10
12
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0
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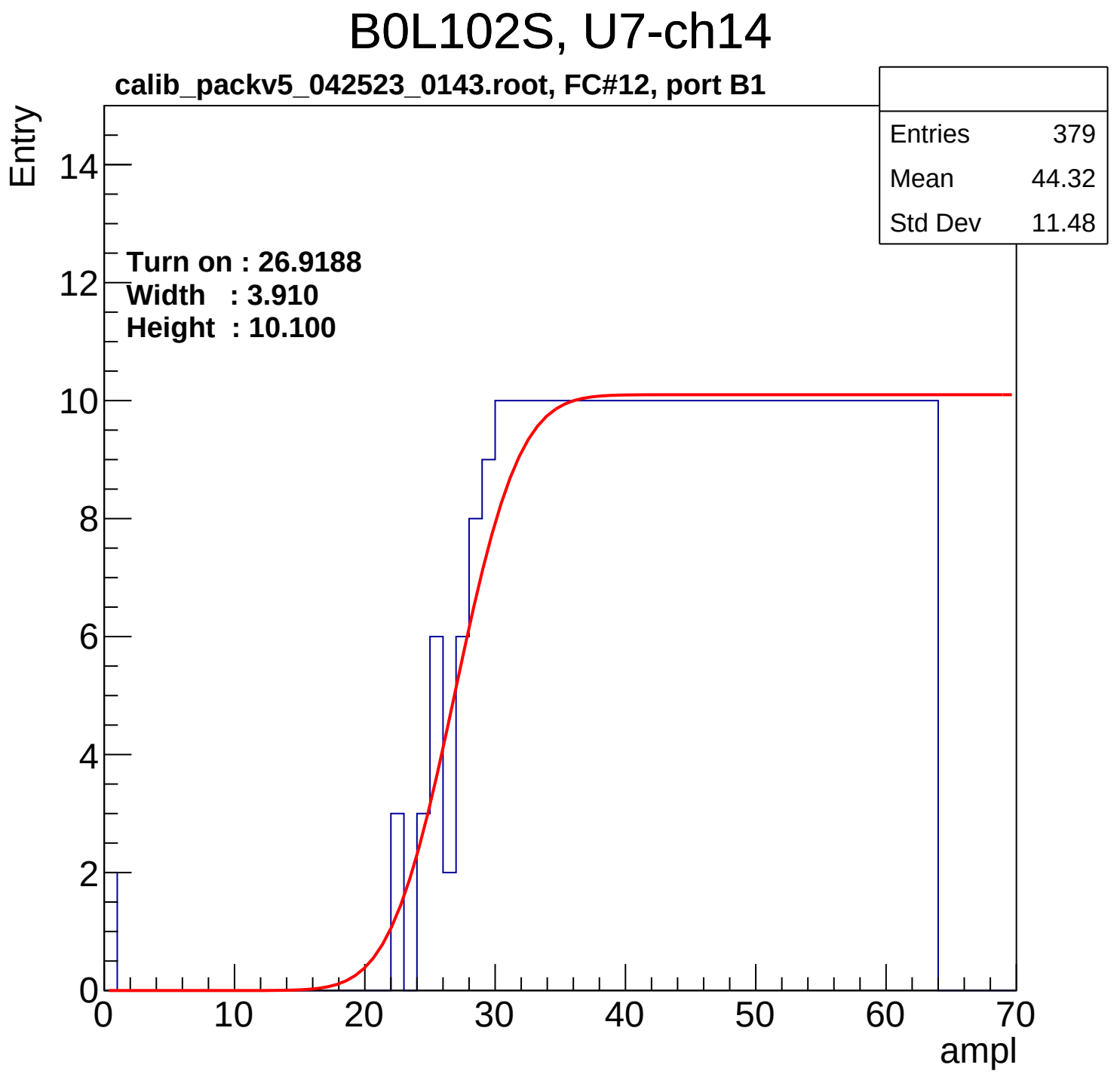
B0L102S, U7-ch14
calib_packv5_042523_0143.root, FC#12, port B1
Entries 379
Mean 44.32
Std Dev 11.48
Turn on : 26.9188
Width : 3.910
Height : 10.100
Entry
ampl
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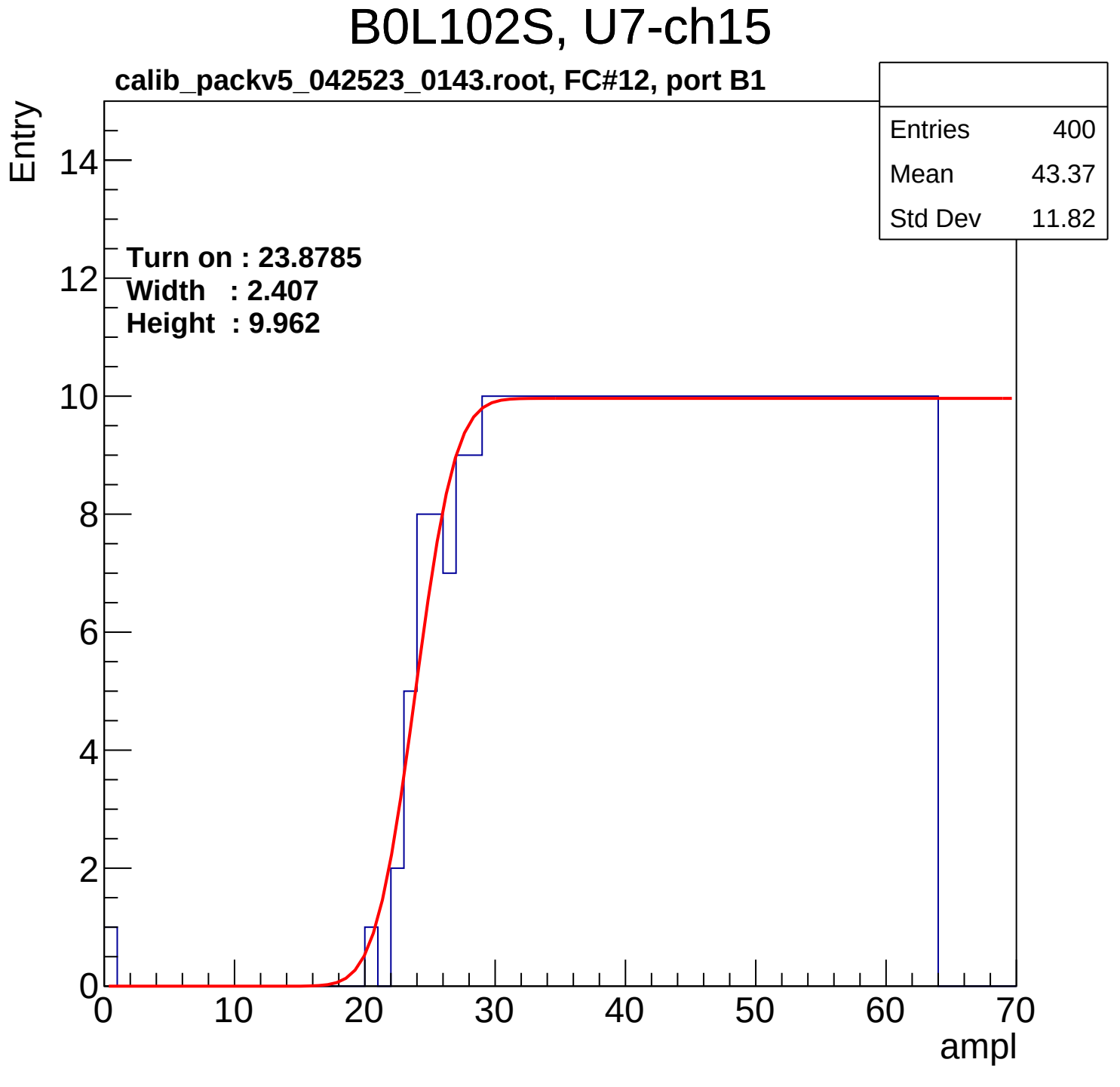
B0L102S, U7-ch15
calib_packv5_042523_0143.root, FC#12, port B1
Entries 400
Mean 43.37
Std Dev 11.82
Turn on : 23.8785
Width : 2.407
Height : 9.962
Entry
ampl
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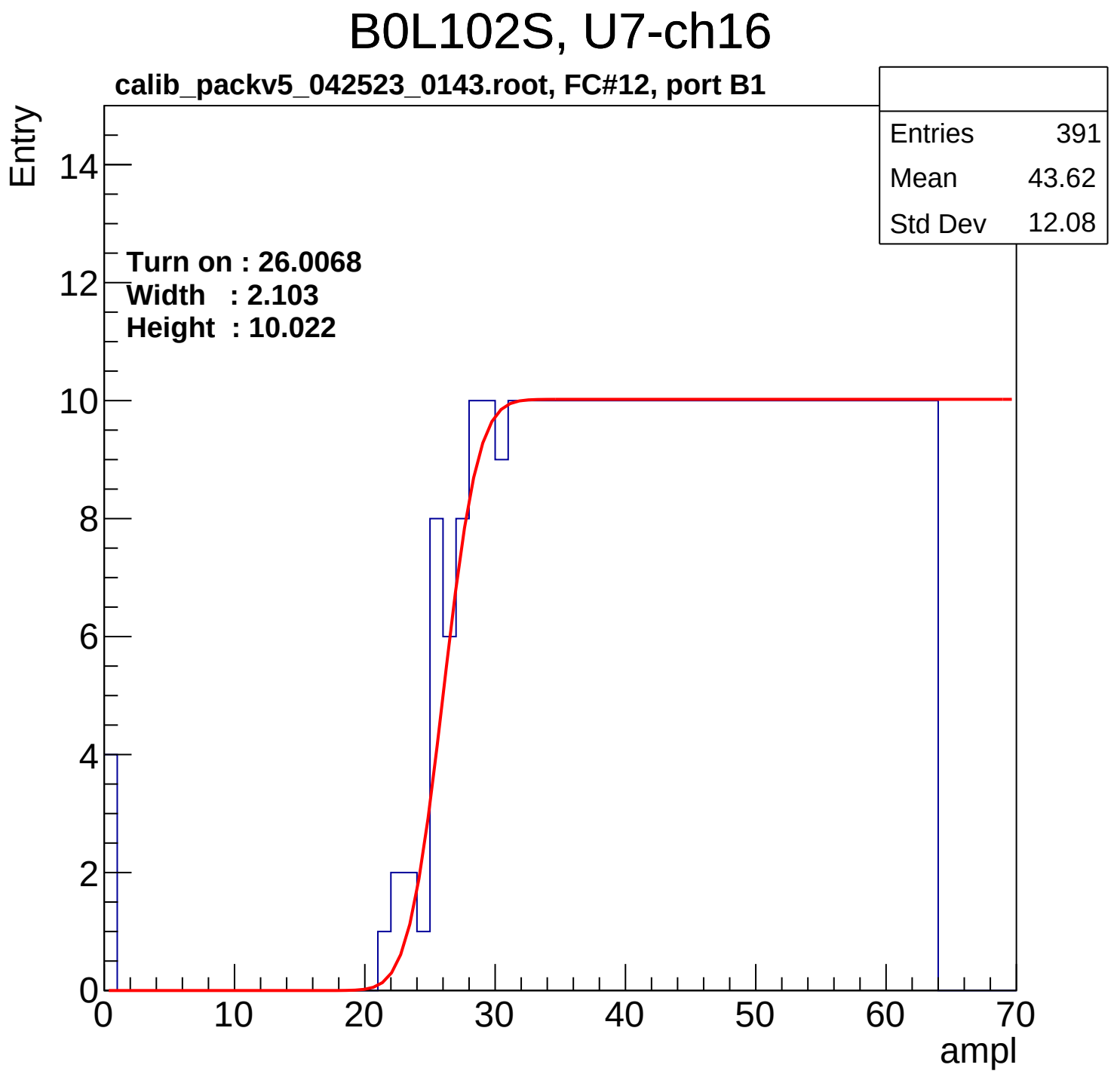
B0L102S, U7-ch16
calib_packv5_042523_0143.root, FC#12, port B1
Entries 391
Mean 43.62
Std Dev 12.08
Turn on : 26.0068
Width : 2.103
Height : 10.022
Entry
ampl
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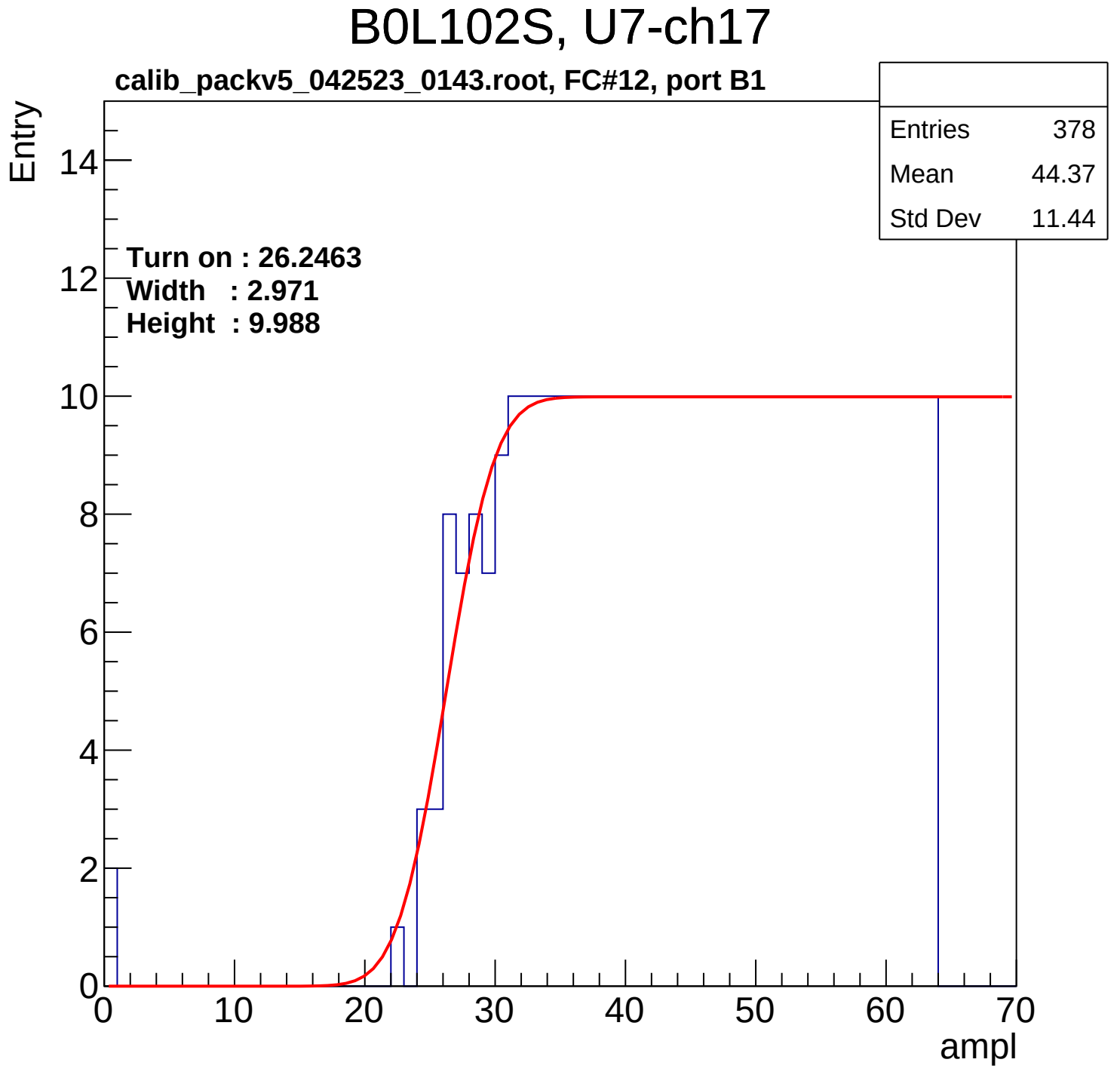
B0L102S, U7-ch17
calib_packv5_042523_0143.root, FC#12, port B1
Entries 378
Mean 44.37
Std Dev 11.44
Turn on : 26.2463
Width : 2.971
Height : 9.988
Entry
ampl
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2
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6
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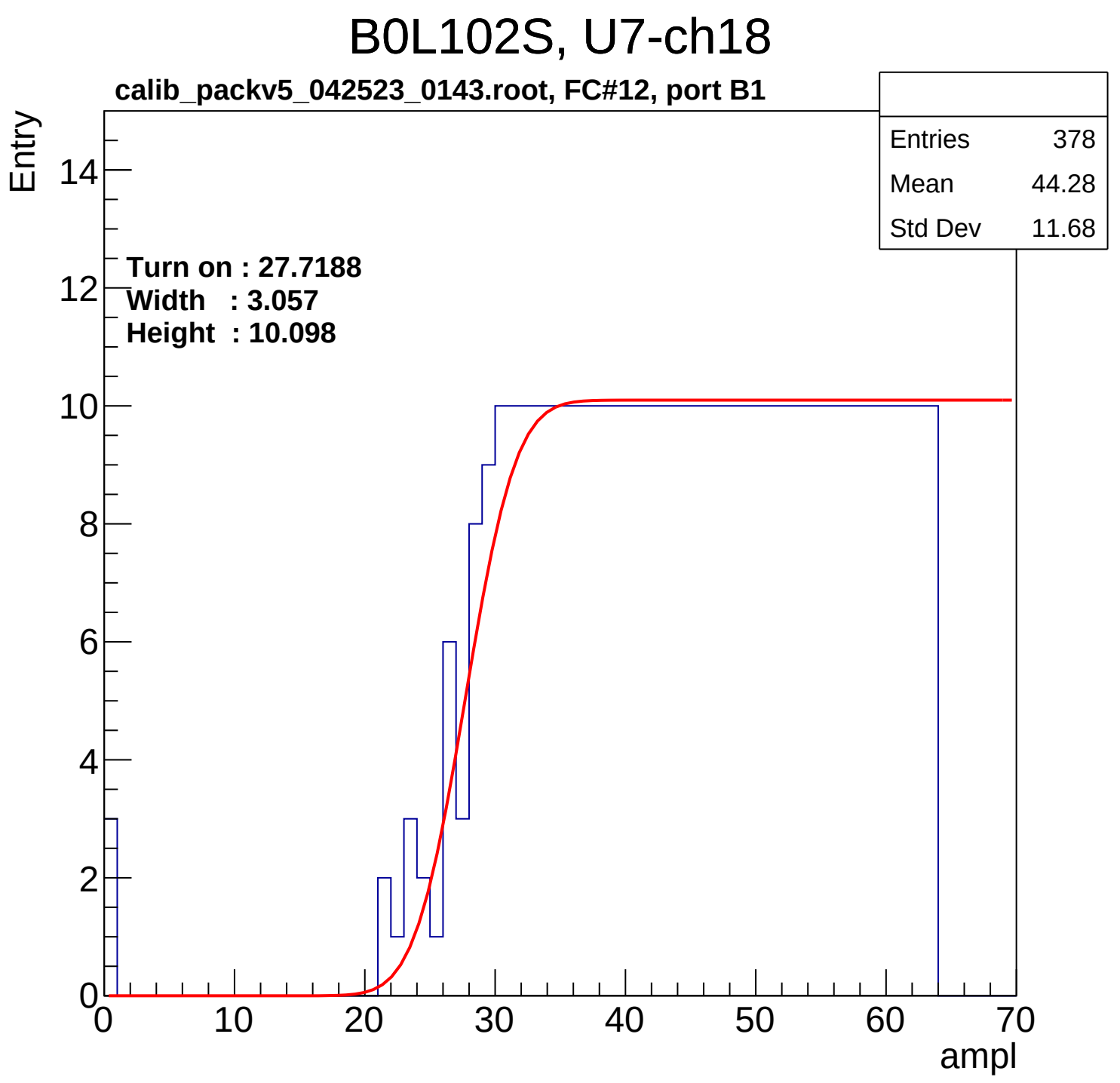
B0L102S, U7-ch18
calib_packv5_042523_0143.root, FC#12, port B1
Entries 378
Mean 44.28
Std Dev 11.68
Turn on : 27.7188
Width : 3.057
Height : 10.098
Entry
ampl
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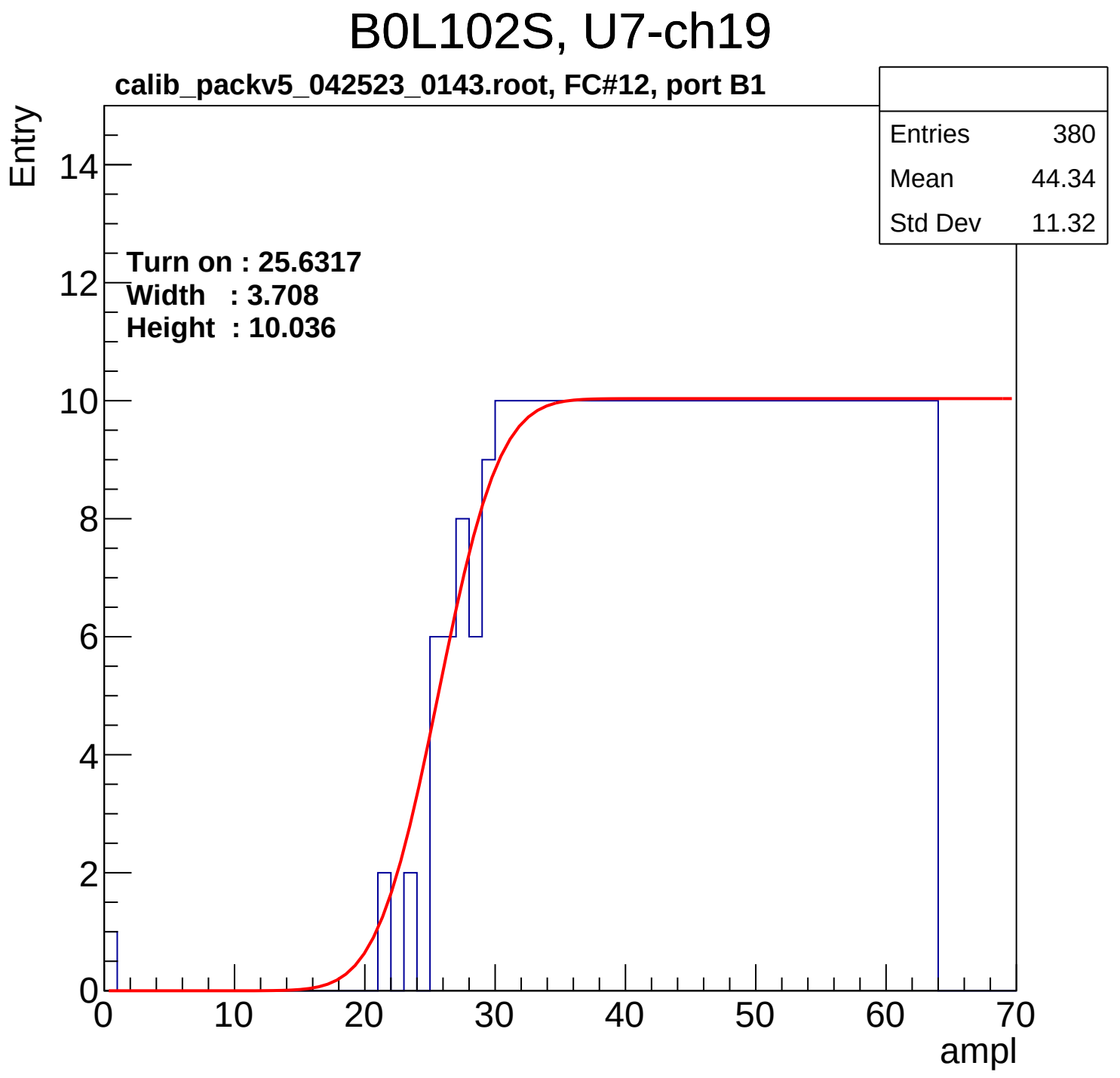
B0L102S, U7-ch19
calib_packv5_042523_0143.root, FC#12, port B1
Entries 380
Mean 44.34
Std Dev 11.32
Turn on : 25.6317
Width : 3.708
Height : 10.036
Entry
ampl
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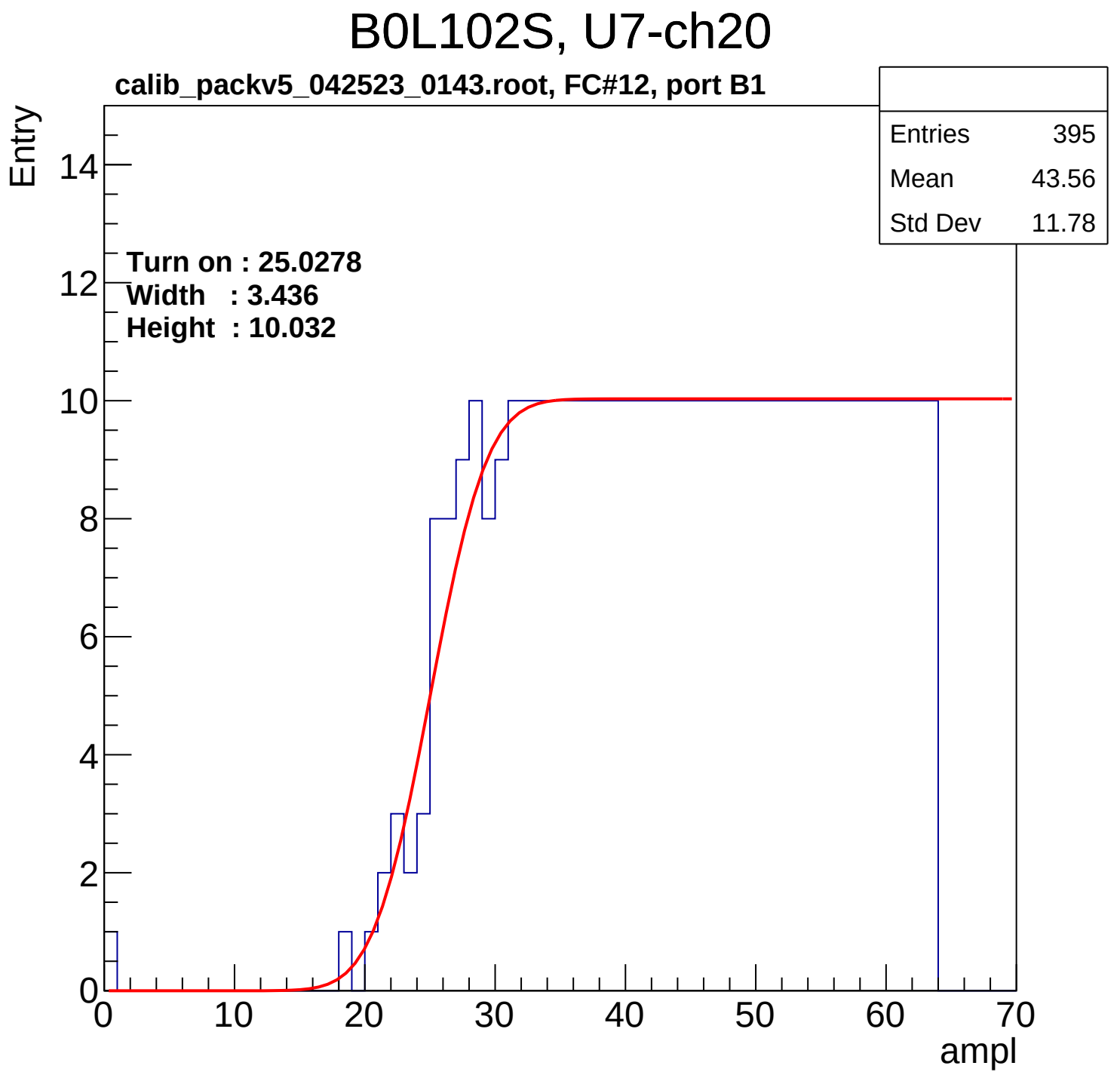
B0L102S, U7-ch20
calib_packv5_042523_0143.root, FC#12, port B1
Entries 395
Mean 43.56
Std Dev 11.78
Turn on : 25.0278
Width : 3.436
Height : 10.032
Entry
ampl
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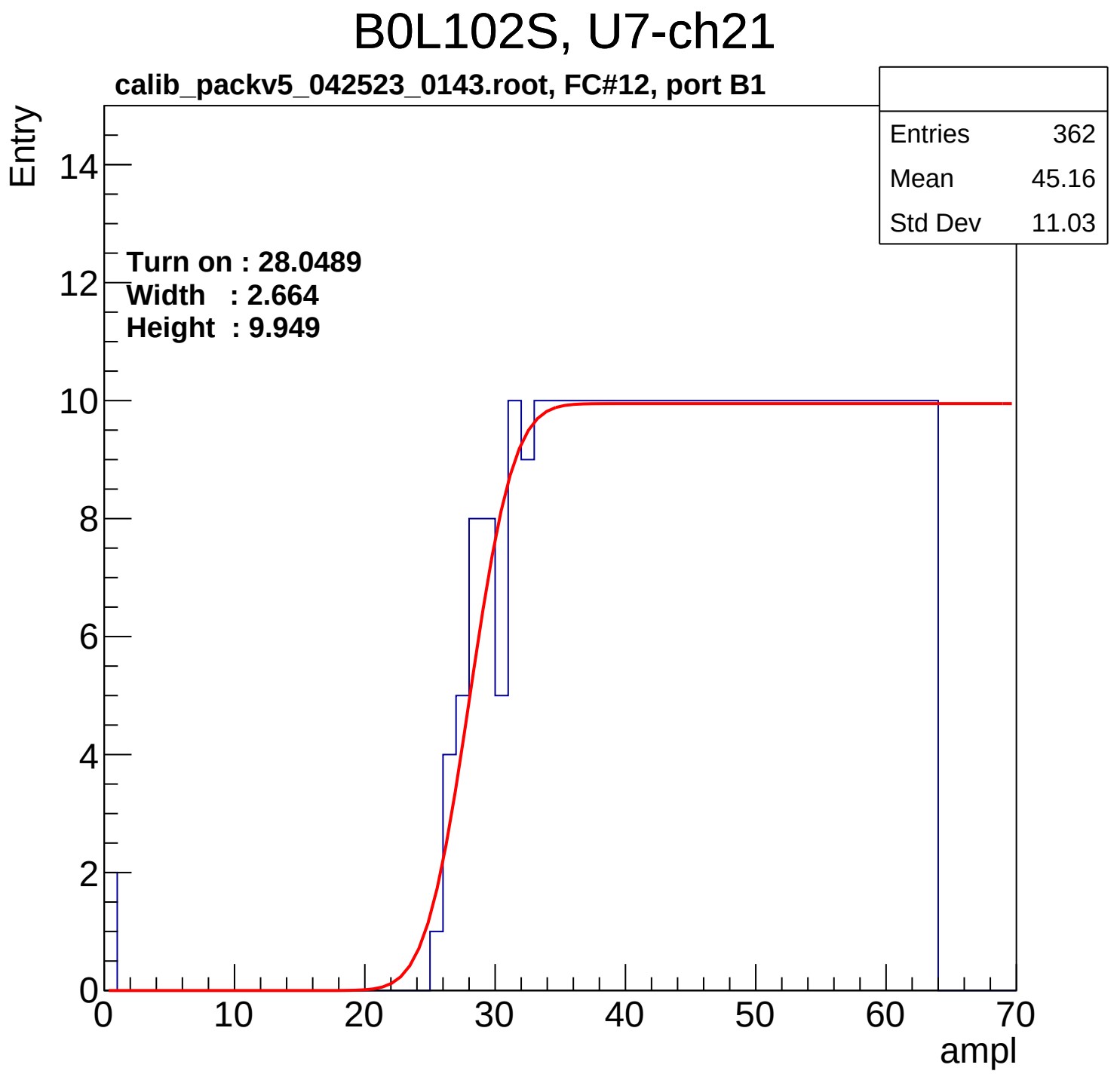
B0L102S, U7-ch21
calib_packv5_042523_0143.root, FC#12, port B1
Entries 362
Mean 45.16
Std Dev 11.03
Turn on : 28.0489
Width : 2.664
Height : 9.949
Entry
ampl
0
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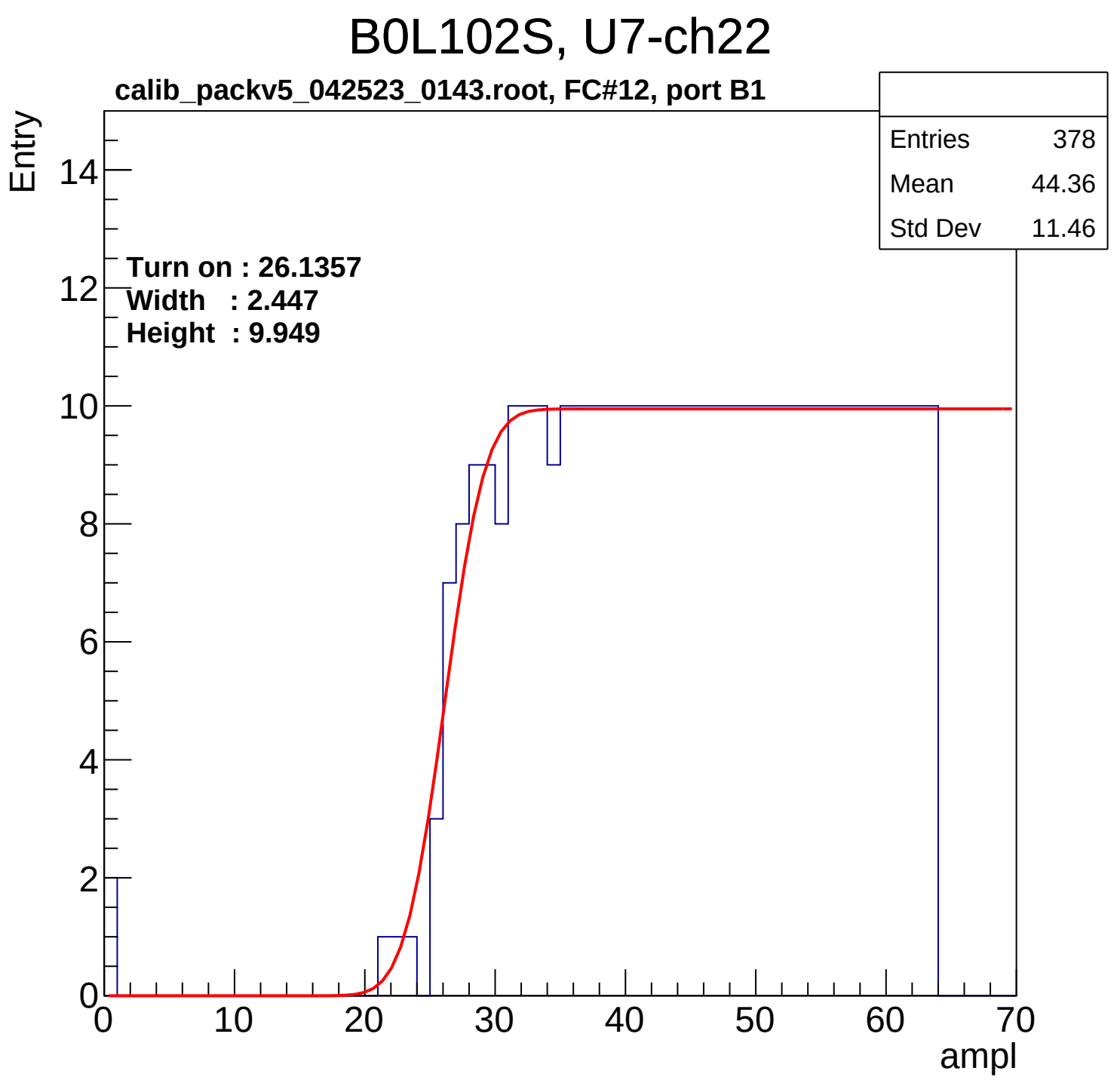
B0L102S, U7-ch22
calib_packv5_042523_0143.root, FC#12, port B1
Entries 378
Mean 44.36
Std Dev 11.46
Turn on : 26.1357
Width : 2.447
Height : 9.949
Entry
ampl
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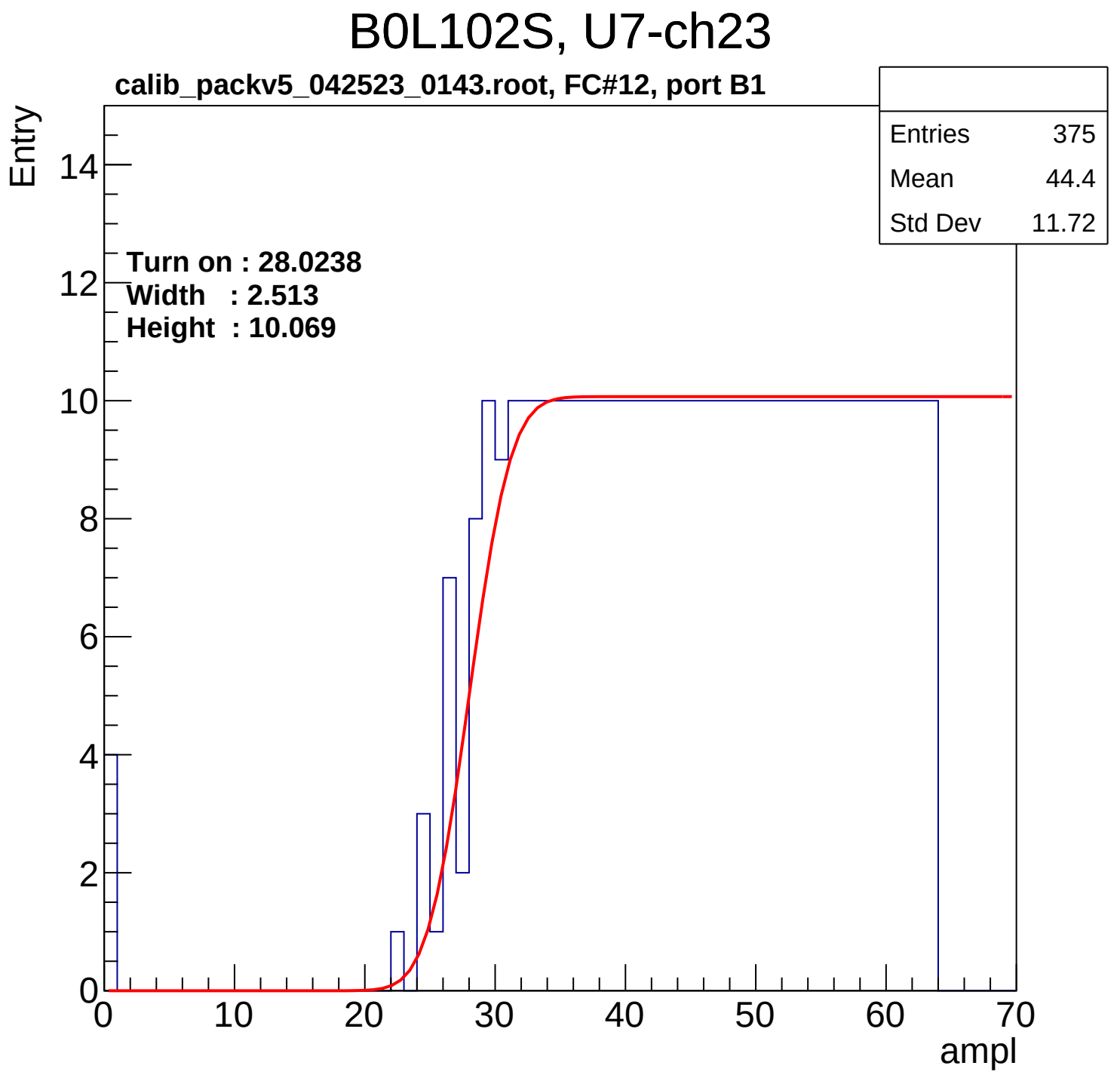
B0L102S, U7-ch23
calib_packv5_042523_0143.root, FC#12, port B1
Entries 375
Mean 44.4
Std Dev 11.72
Turn on : 28.0238
Width : 2.513
Height : 10.069
Entry
ampl
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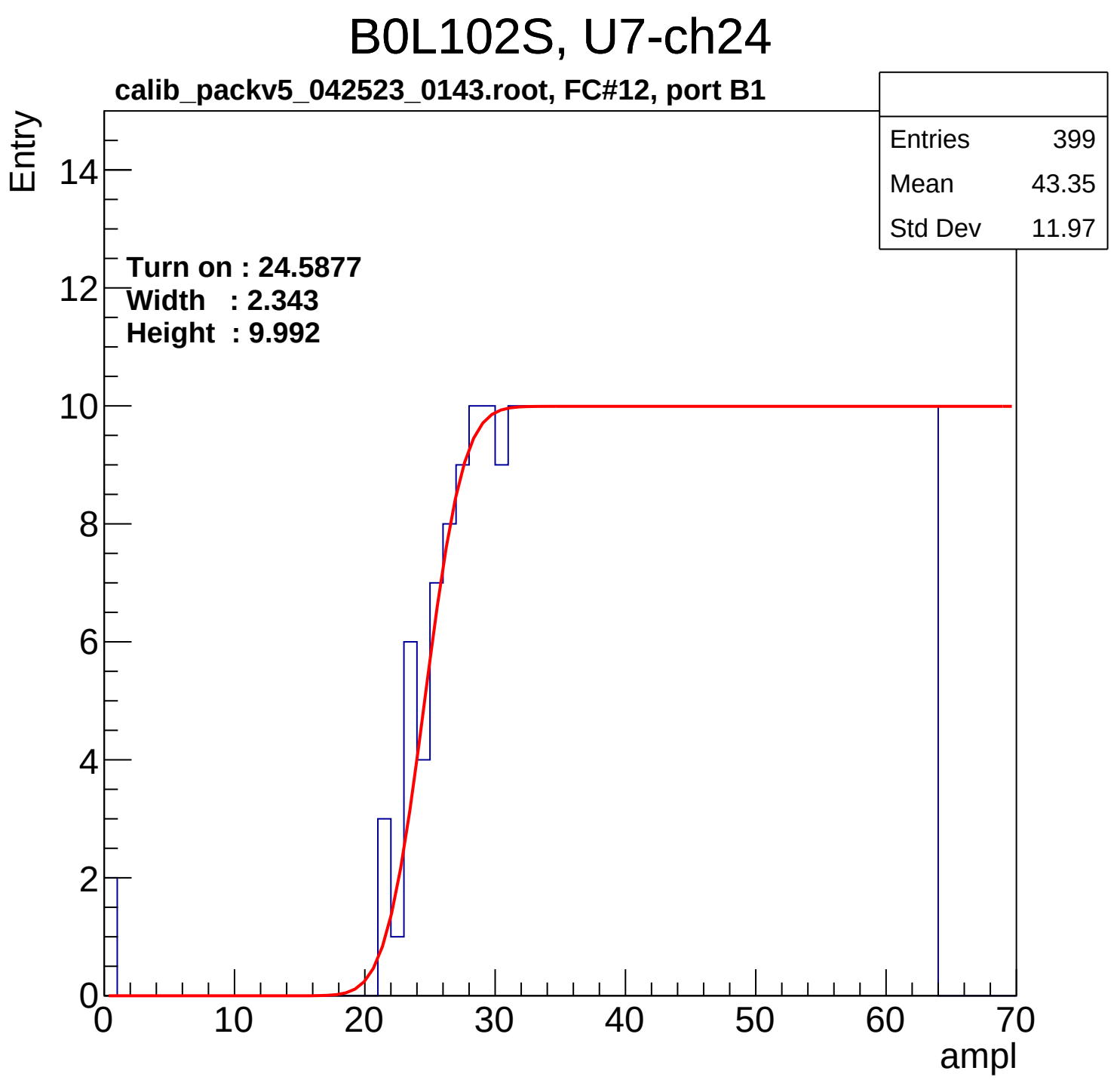
B0L102S, U7-ch24
calib_packv5_042523_0143.root, FC#12, port B1
Entries 399
Mean 43.35
Std Dev 11.97
Turn on : 24.5877
Width : 2.343
Height : 9.992
Entry
ampl
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6
8
10
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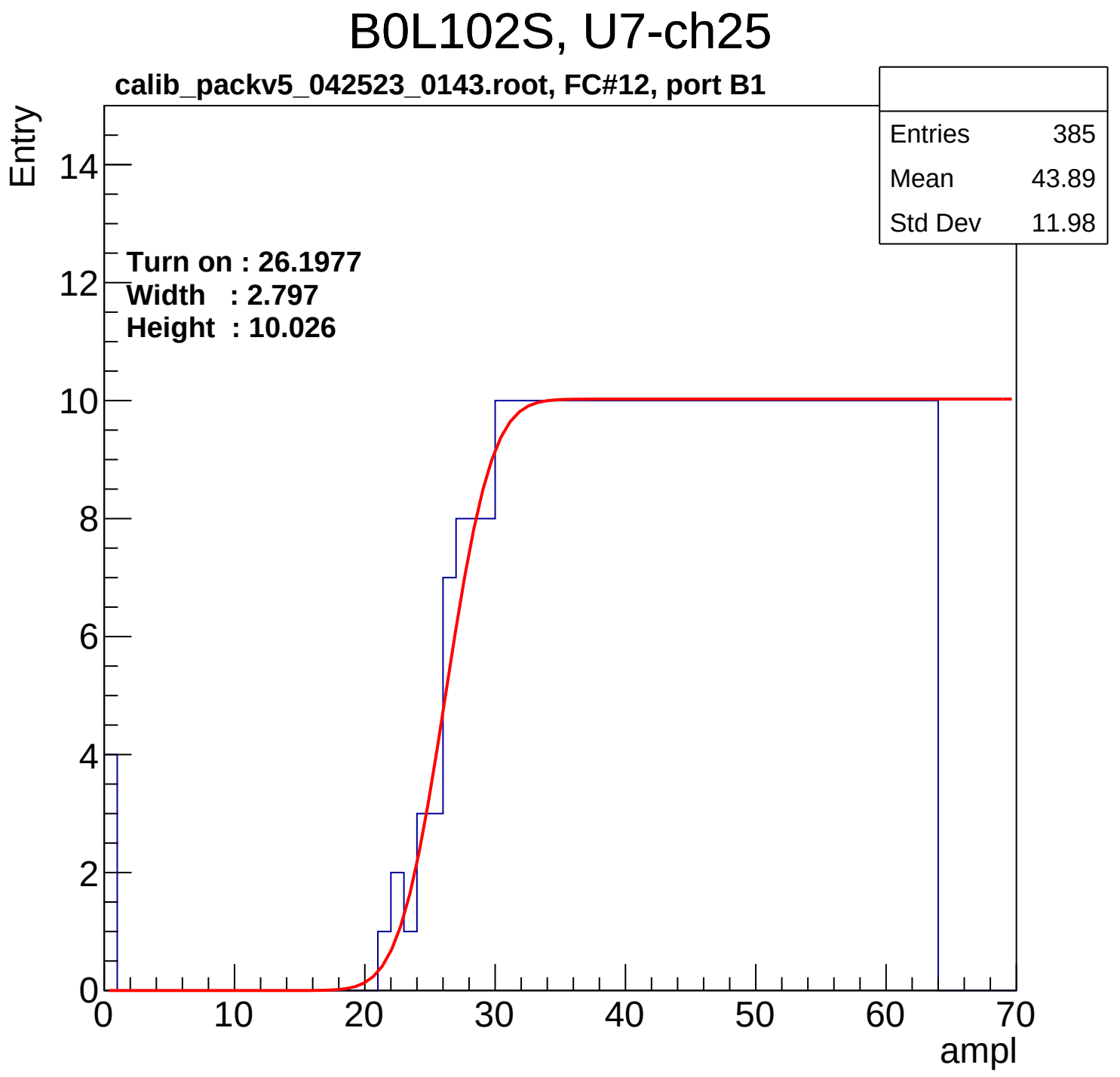
B0L102S, U7-ch25
calib_packv5_042523_0143.root, FC#12, port B1
Entries 385
Mean 43.89
Std Dev 11.98
Turn on : 26.1977
Width : 2.797
Height : 10.026
Entry
ampl
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6
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10
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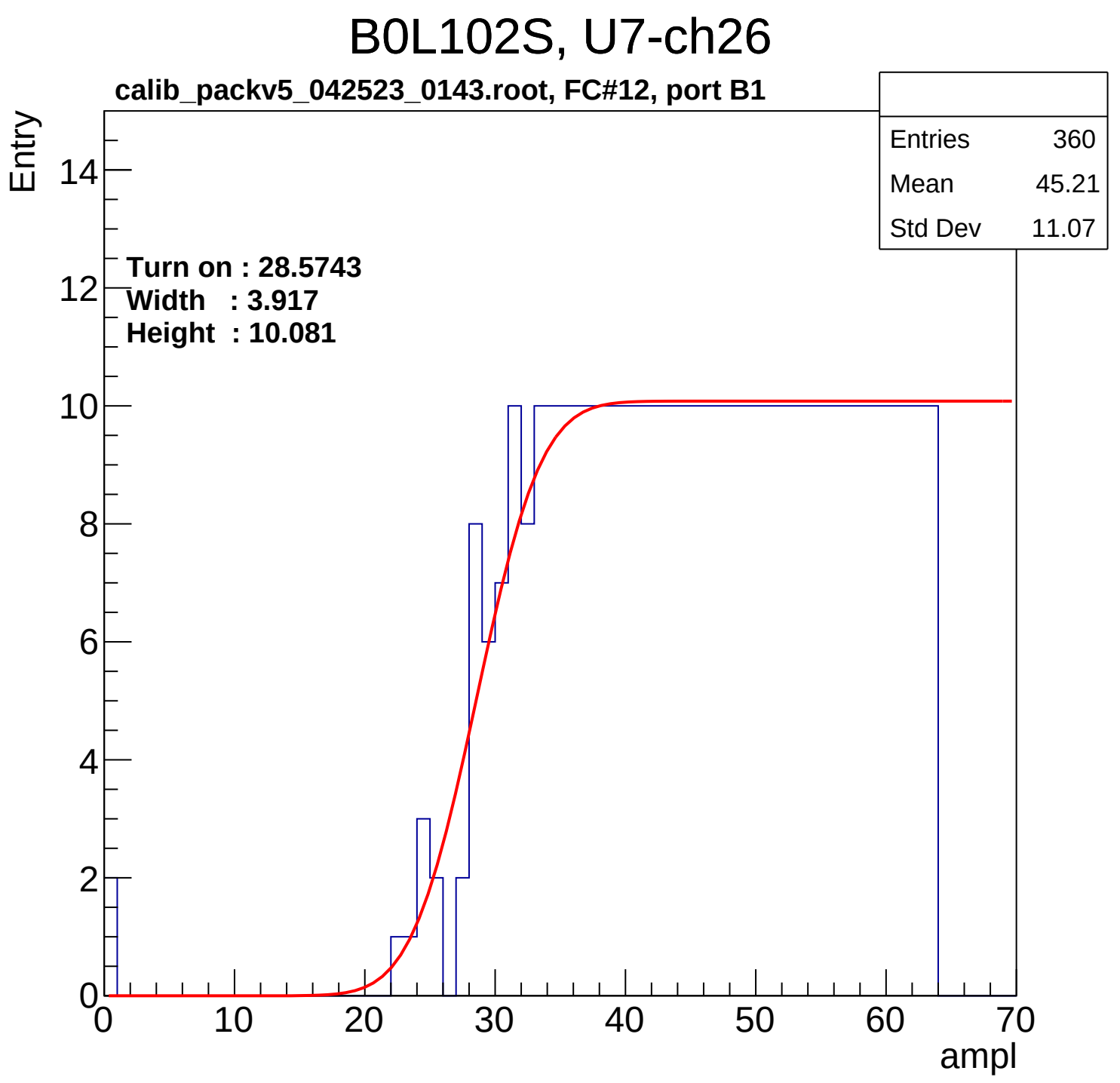
B0L102S, U7-ch26
calib_packv5_042523_0143.root, FC#12, port B1
Entries 360
Mean 45.21
Std Dev 11.07
Turn on : 28.5743
Width : 3.917
Height : 10.081
Entry
ampl
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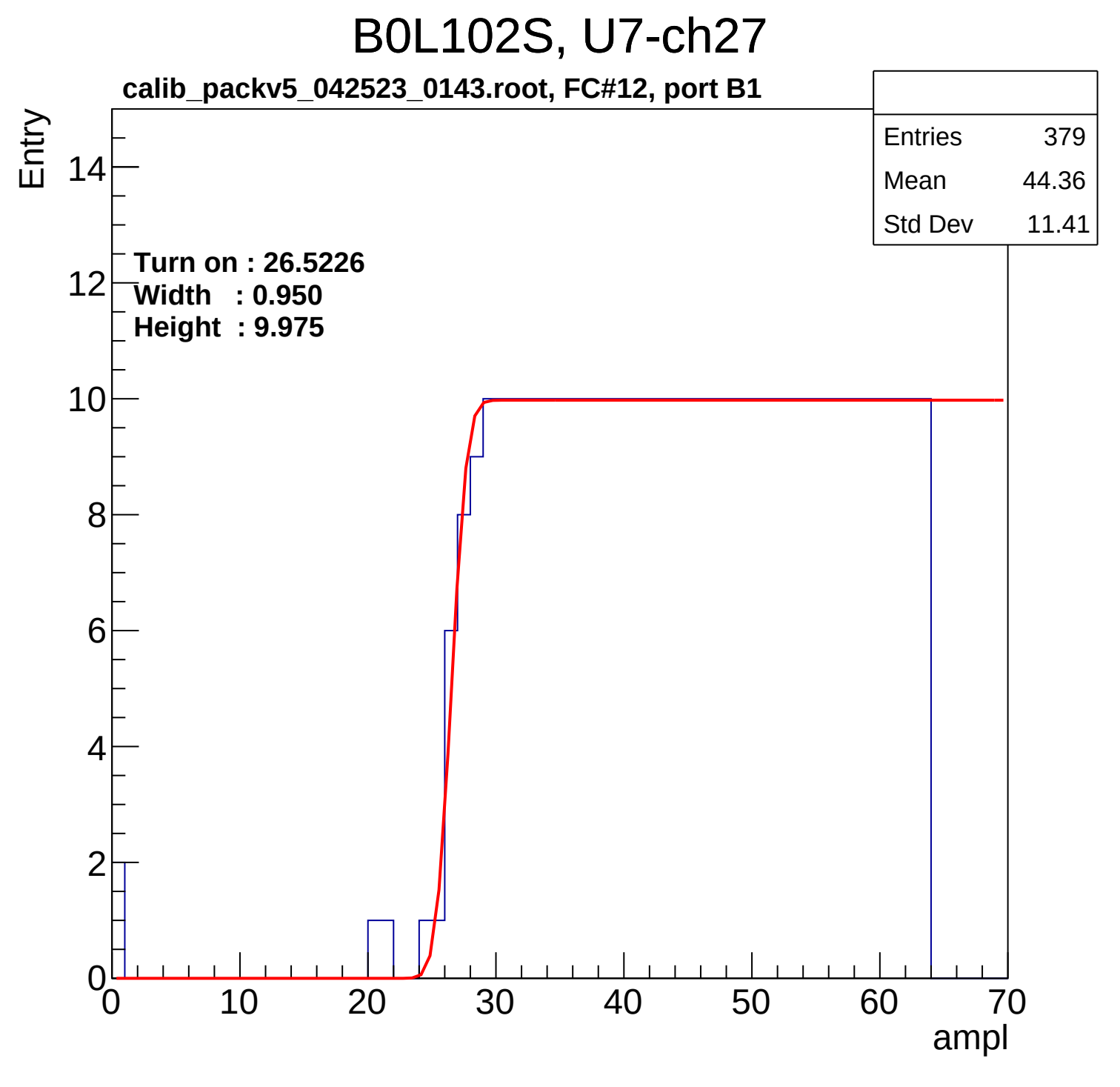
B0L102S, U7-ch27
calib_packv5_042523_0143.root, FC#12, port B1
Entries 379
Mean 44.36
Std Dev 11.41
Turn on : 26.5226
Width : 0.950
Height : 9.975
Entry
ampl
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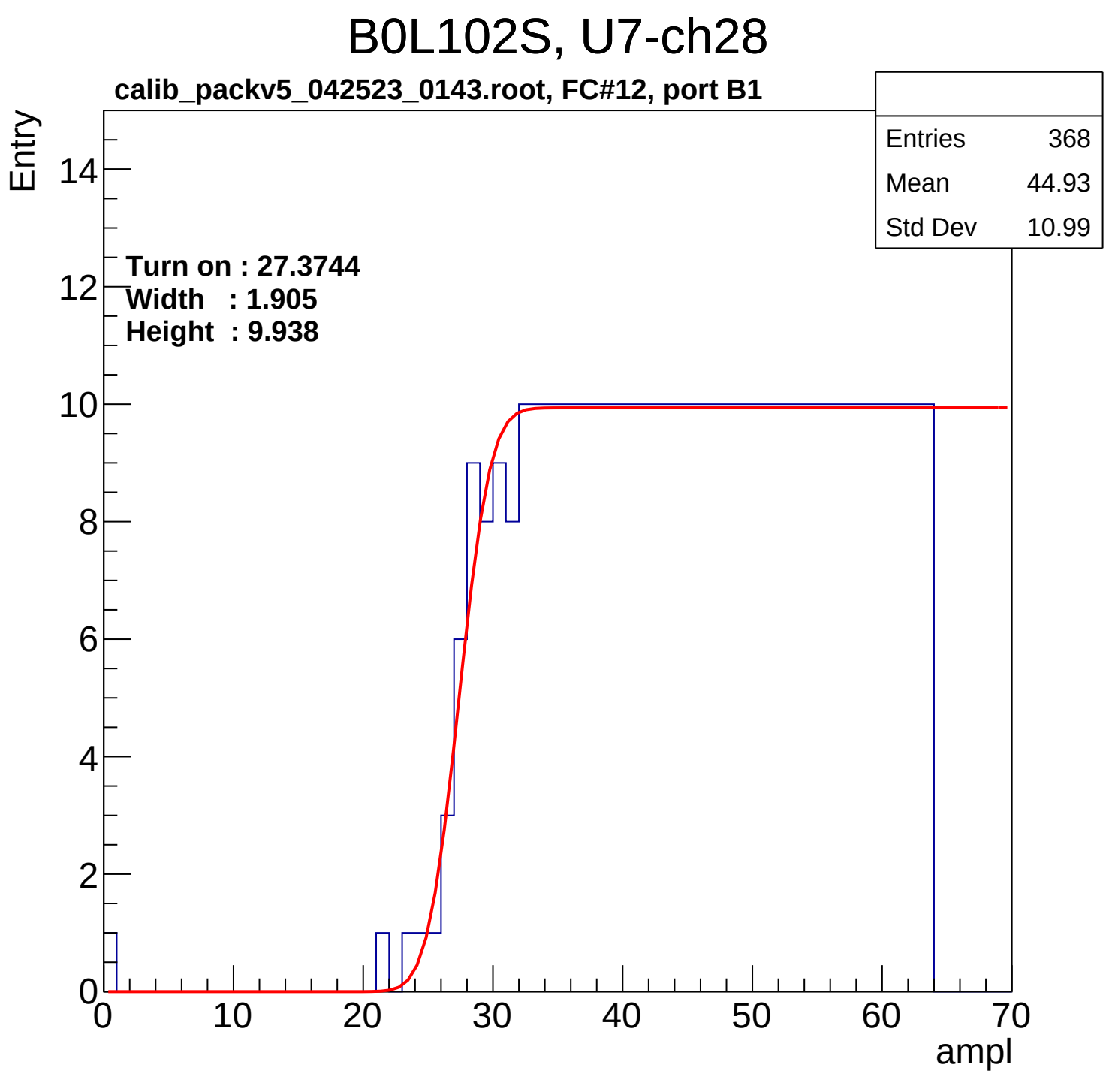
B0L102S, U7-ch28
calib_packv5_042523_0143.root, FC#12, port B1
Entries 368
Mean 44.93
Std Dev 10.99
Turn on : 27.3744
Width : 1.905
Height : 9.938
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
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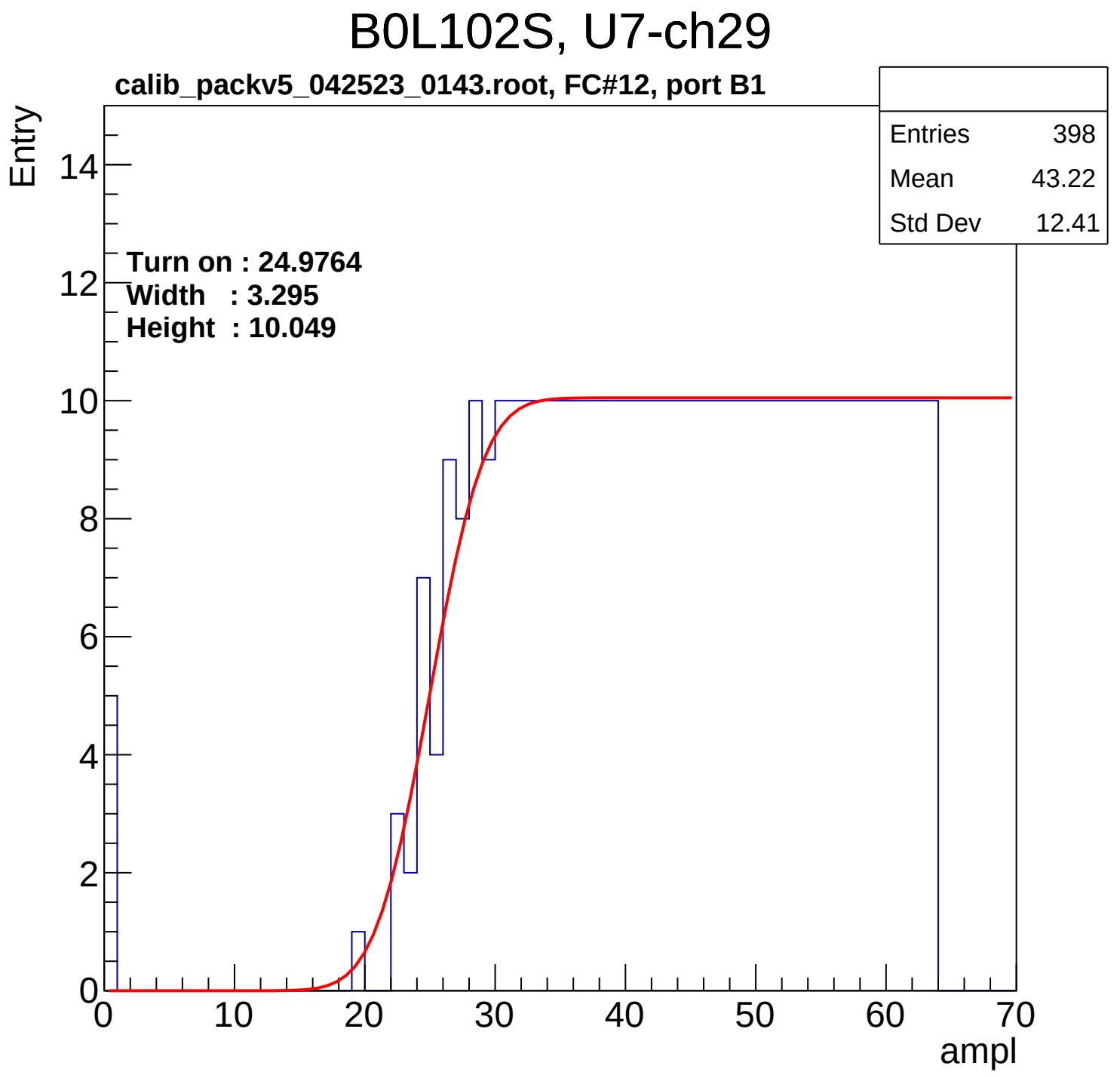
B0L102S, U7-ch29
calib_packv5_042523_0143.root, FC#12, port B1
Entries 398
Mean 43.22
Std Dev 12.41
Turn on : 24.9764
Width : 3.295
Height : 10.049
Entry
ampl
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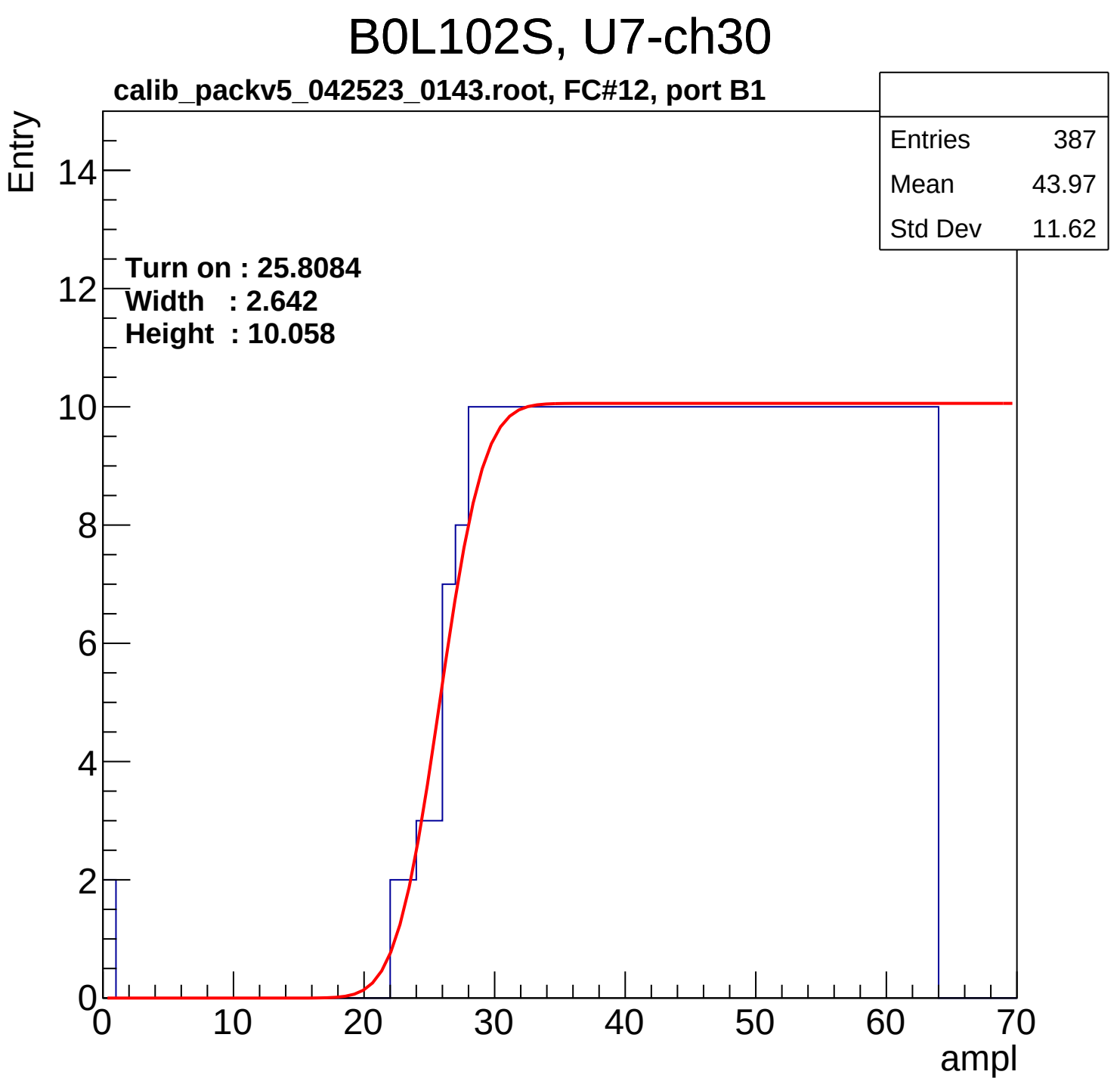
B0L102S, U7-ch30
calib_packv5_042523_0143.root, FC#12, port B1
Entries 387
Mean 43.97
Std Dev 11.62
Turn on : 25.8084
Width : 2.642
Height : 10.058
Entry
ampl
0
2
4
6
8
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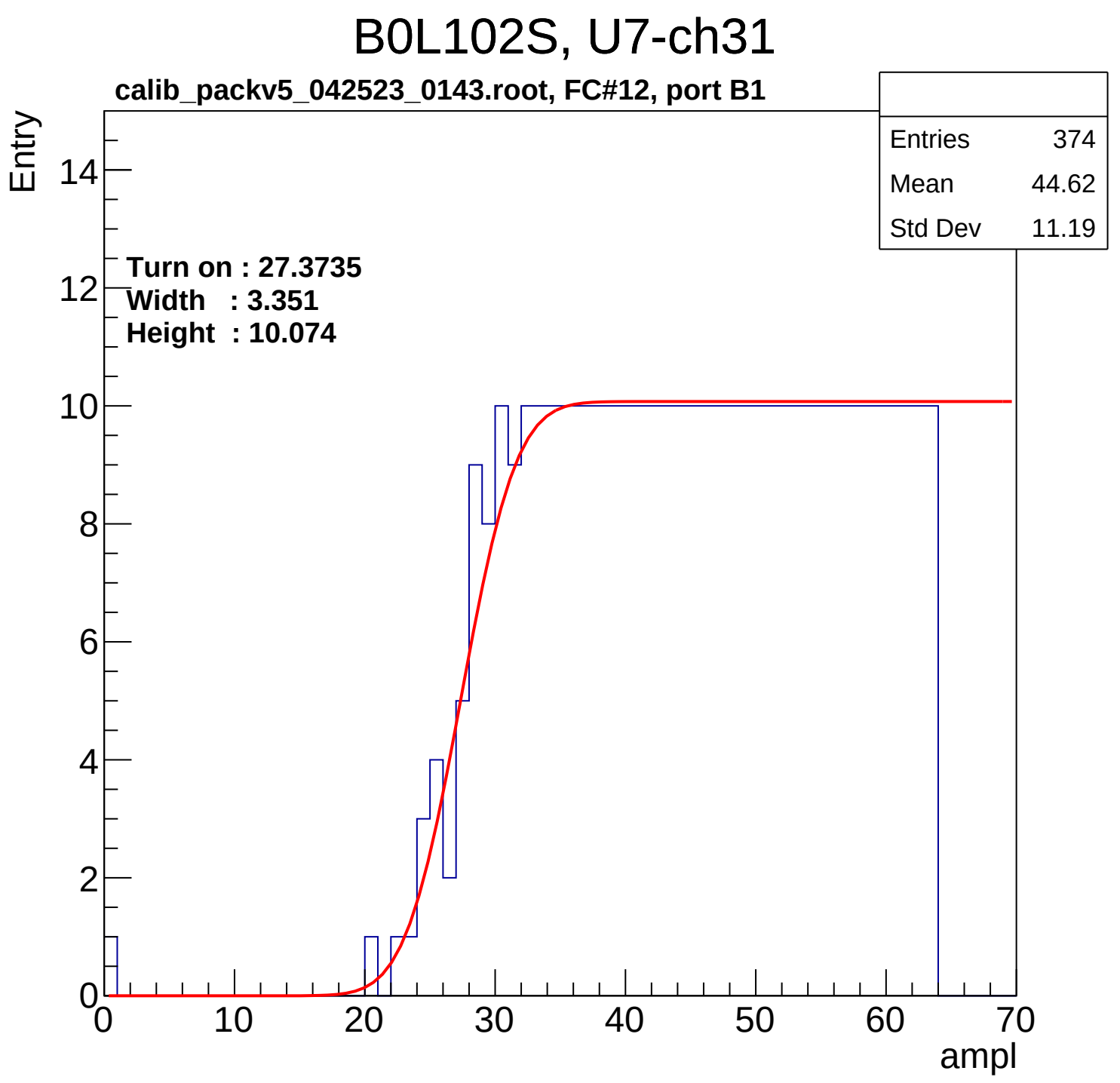
B0L102S, U7-ch31
calib_packv5_042523_0143.root, FC#12, port B1
Entries 374
Mean 44.62
Std Dev 11.19
Turn on : 27.3735
Width : 3.351
Height : 10.074
Entry
ampl
0
2
4
6
8
10
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0
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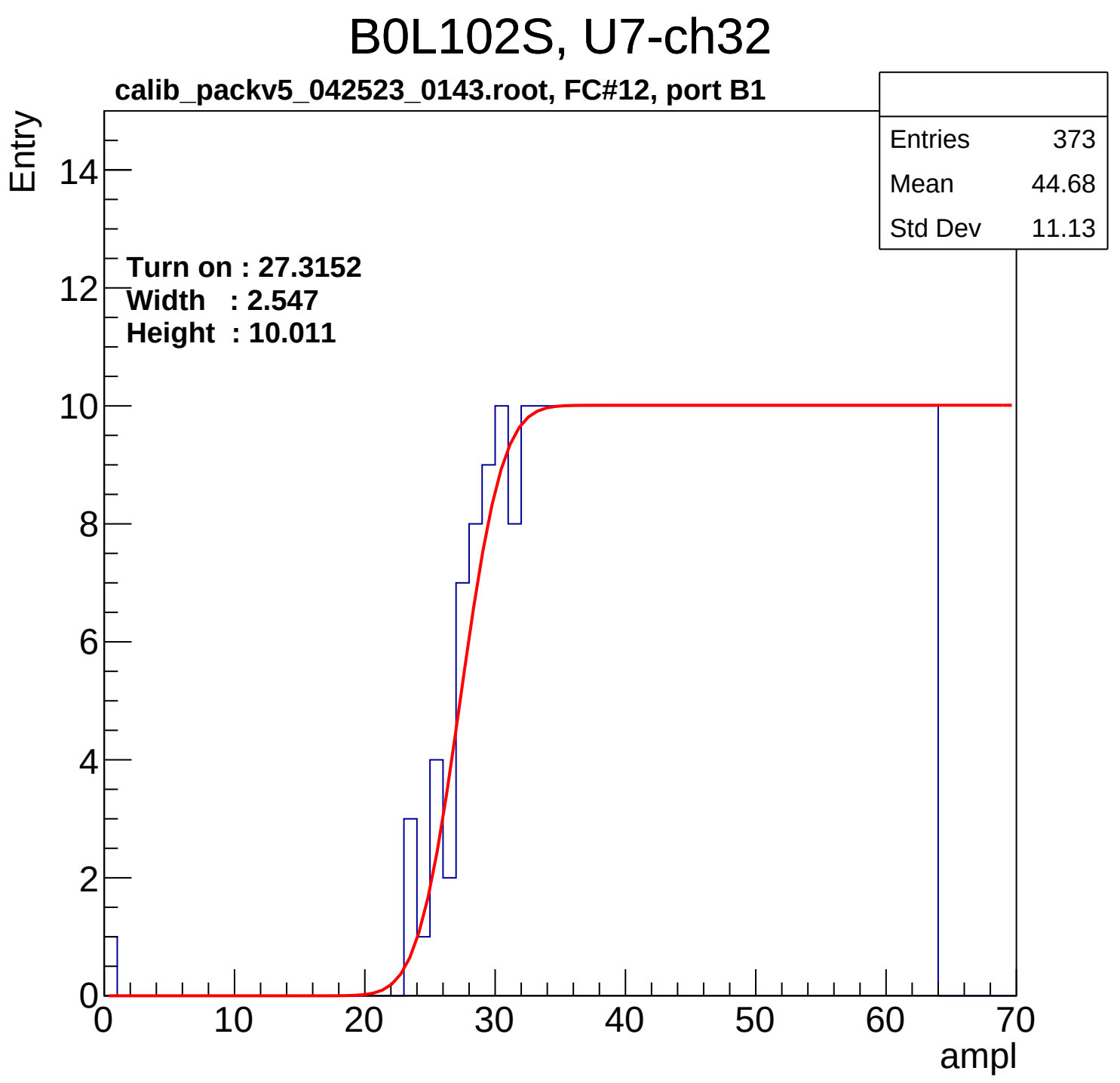
B0L102S, U7-ch32
calib_packv5_042523_0143.root, FC#12, port B1
Entries 373
Mean 44.68
Std Dev 11.13
Turn on : 27.3152
Width : 2.547
Height : 10.011
Entry
ampl
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2
4
6
8
10
12
14
0
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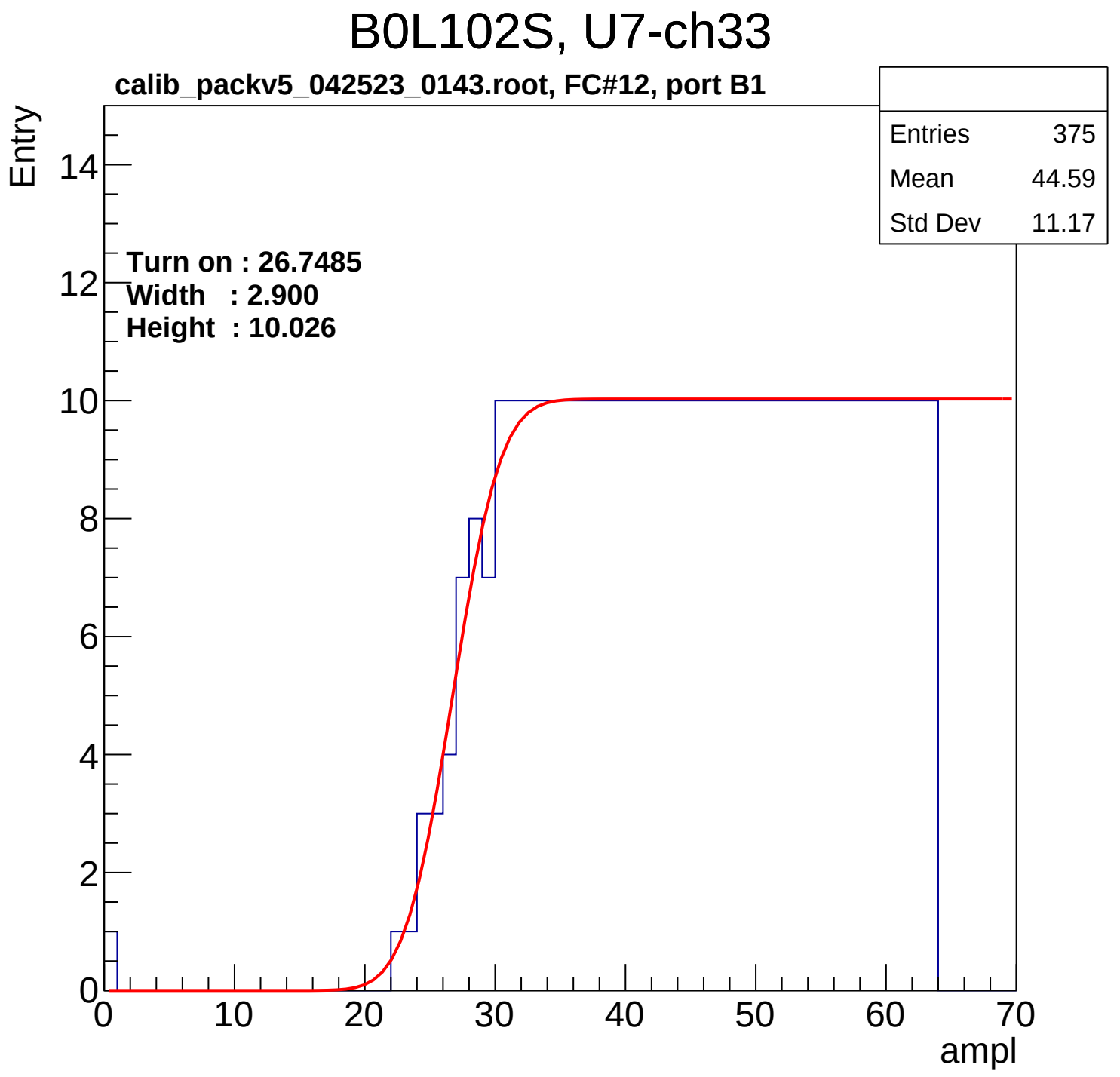
B0L102S, U7-ch33
calib_packv5_042523_0143.root, FC#12, port B1
Entries 375
Mean 44.59
Std Dev 11.17
Turn on : 26.7485
Width : 2.900
Height : 10.026
Entry
ampl
0
2
4
6
8
10
12
14
0
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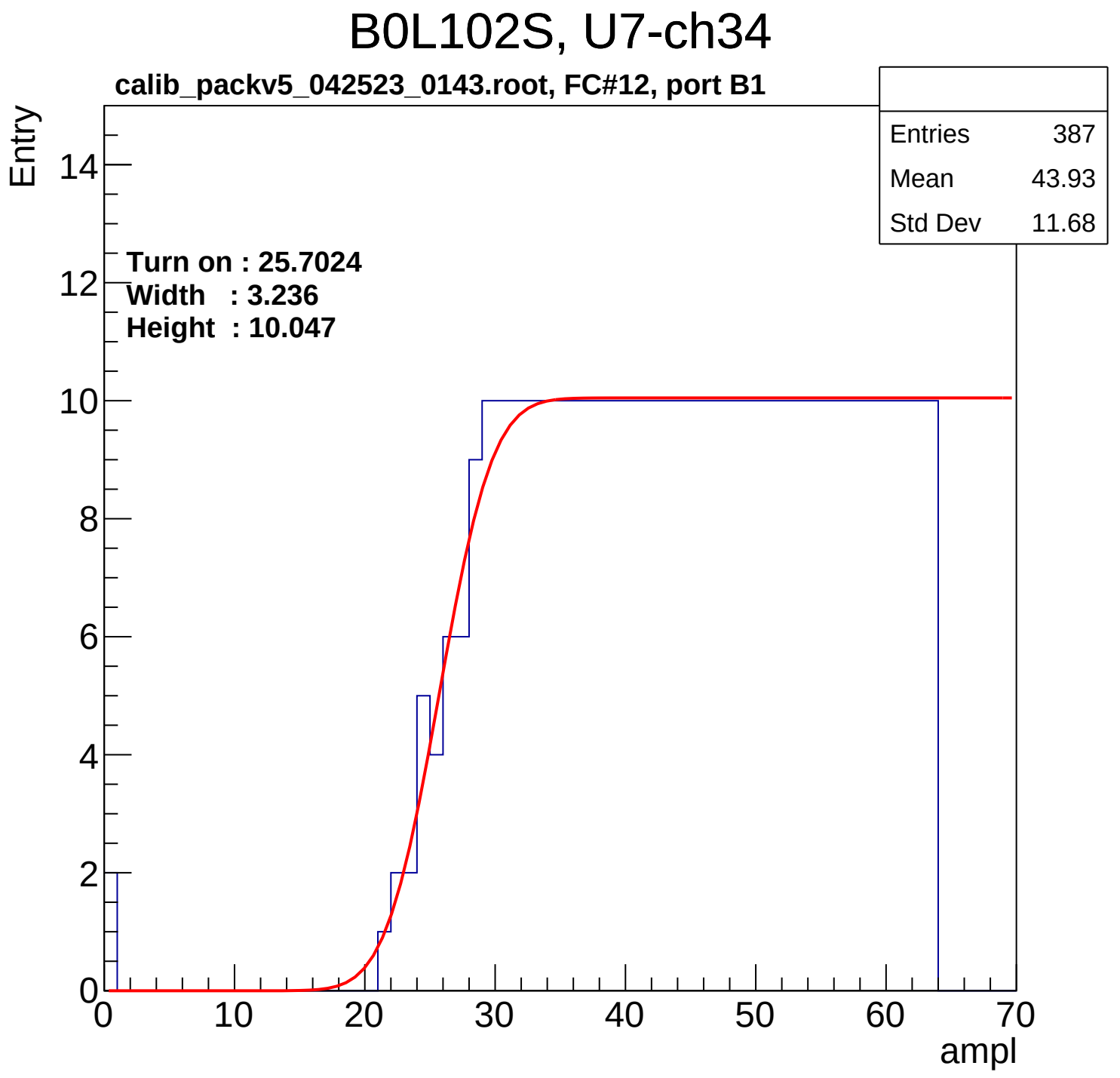
B0L102S, U7-ch34
calib_packv5_042523_0143.root, FC#12, port B1
Entries 387
Mean 43.93
Std Dev 11.68
Turn on : 25.7024
Width : 3.236
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
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40
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60
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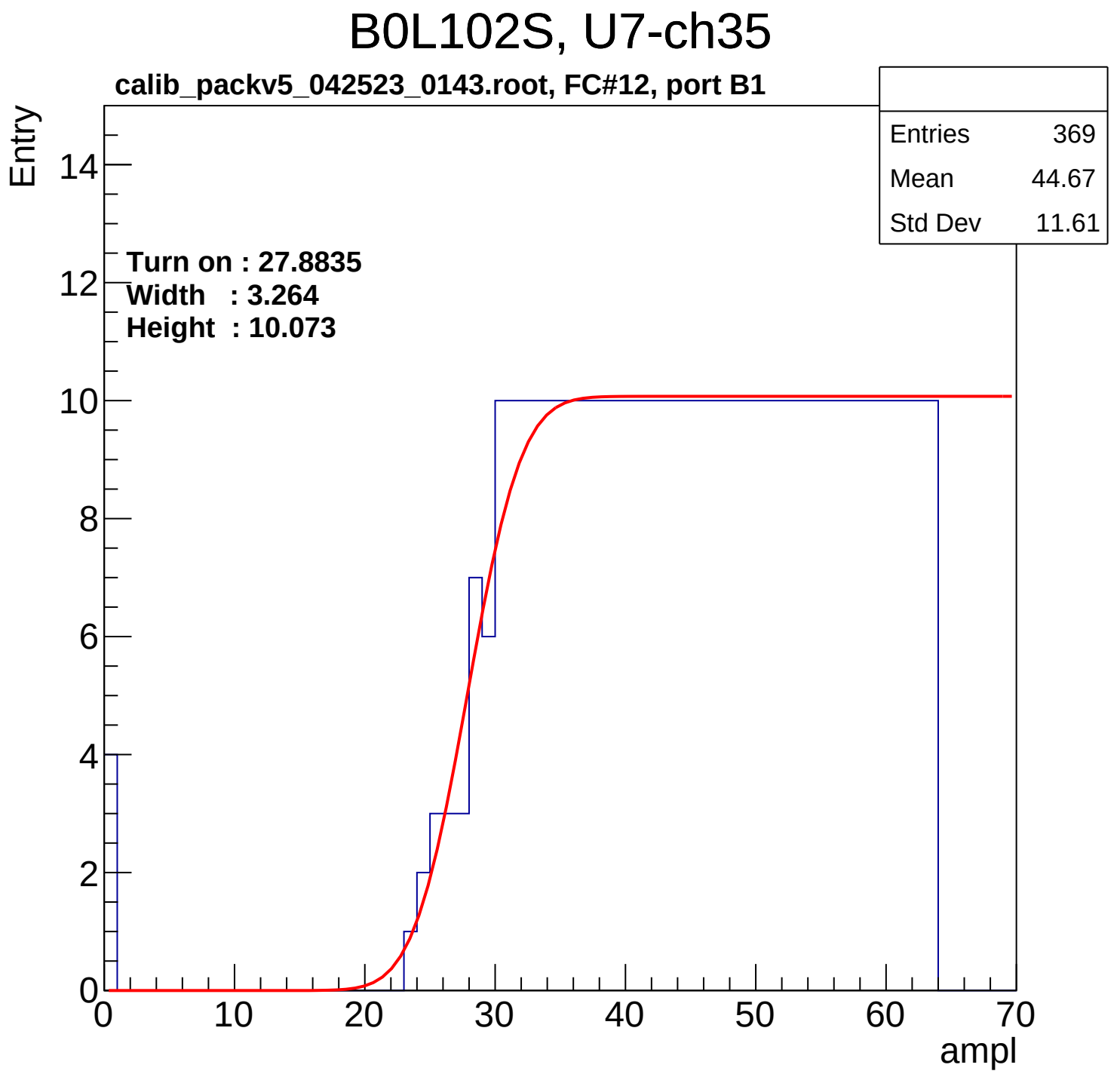
B0L102S, U7-ch35
calib_packv5_042523_0143.root, FC#12, port B1
Entries 369
Mean 44.67
Std Dev 11.61
Turn on : 27.8835
Width : 3.264
Height : 10.073
Entry
ampl
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2
4
6
8
10
12
14
0
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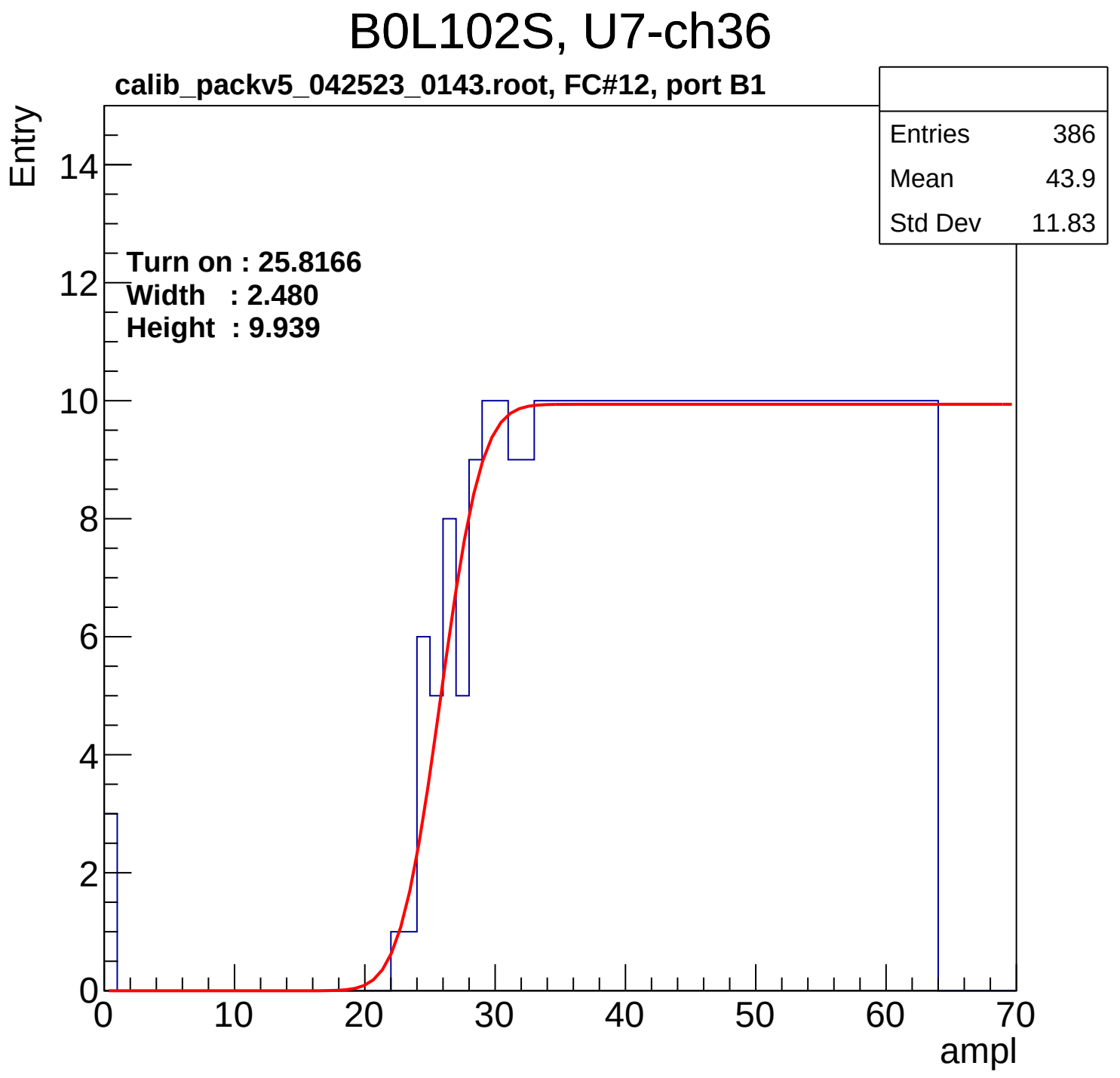
B0L102S, U7-ch36
calib_packv5_042523_0143.root, FC#12, port B1
Entries 386
Mean 43.9
Std Dev 11.83
Turn on : 25.8166
Width : 2.480
Height : 9.939
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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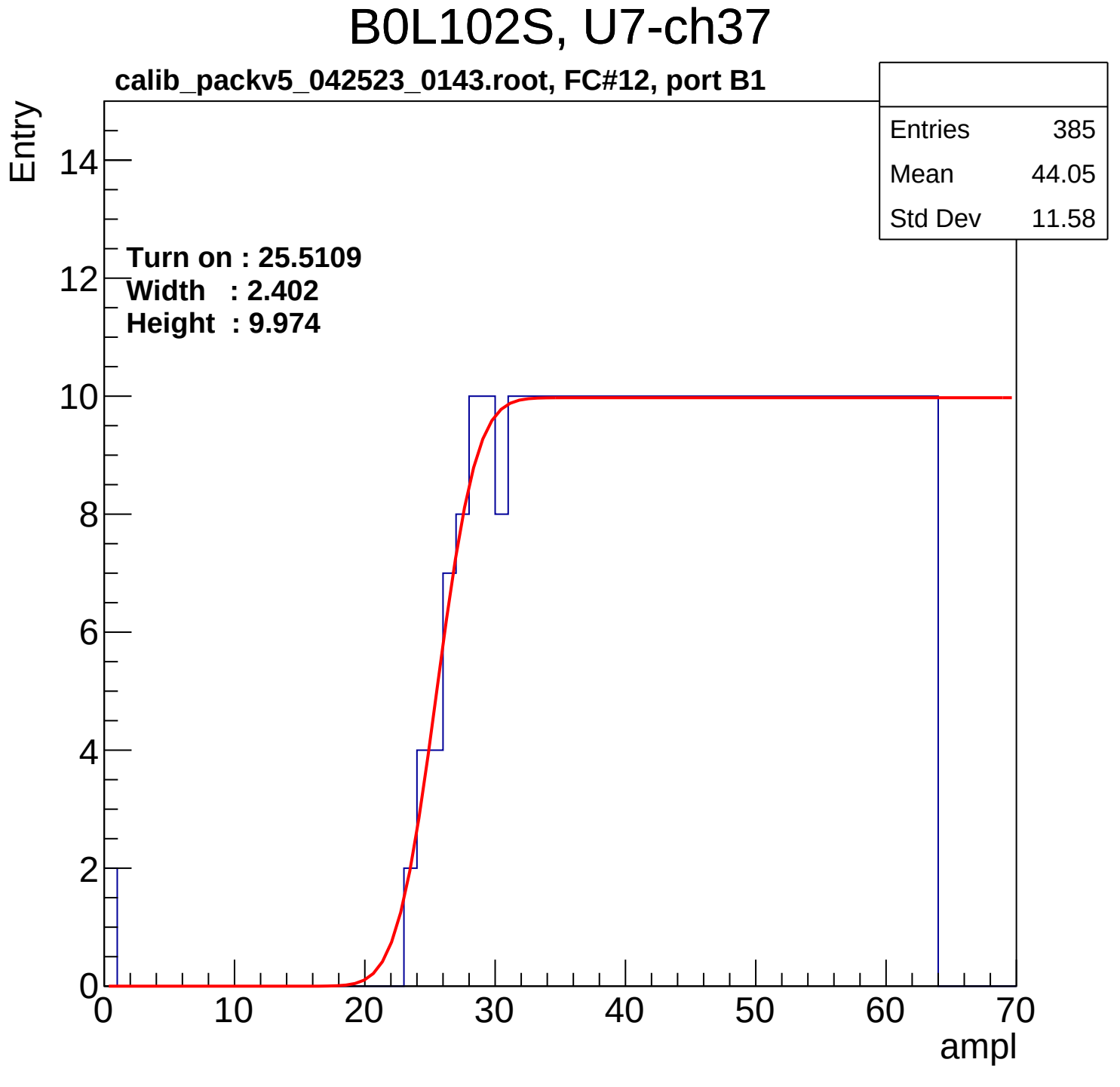
B0L102S, U7-ch37
calib_packv5_042523_0143.root, FC#12, port B1
Entries 385
Mean 44.05
Std Dev 11.58
Turn on : 25.5109
Width : 2.402
Height : 9.974
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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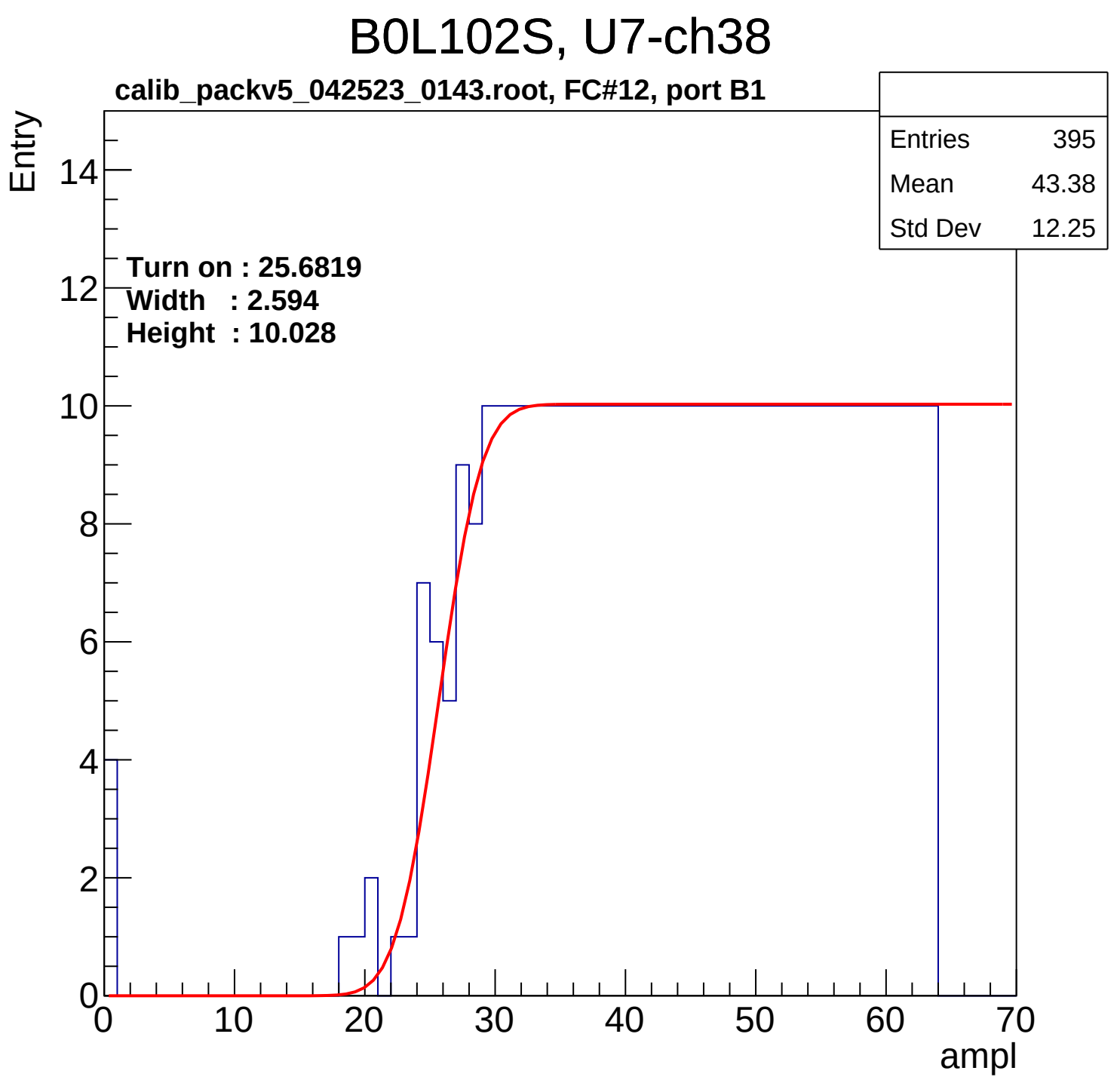
B0L102S, U7-ch38
calib_packv5_042523_0143.root, FC#12, port B1
Entries 395
Mean 43.38
Std Dev 12.25
Turn on : 25.6819
Width : 2.594
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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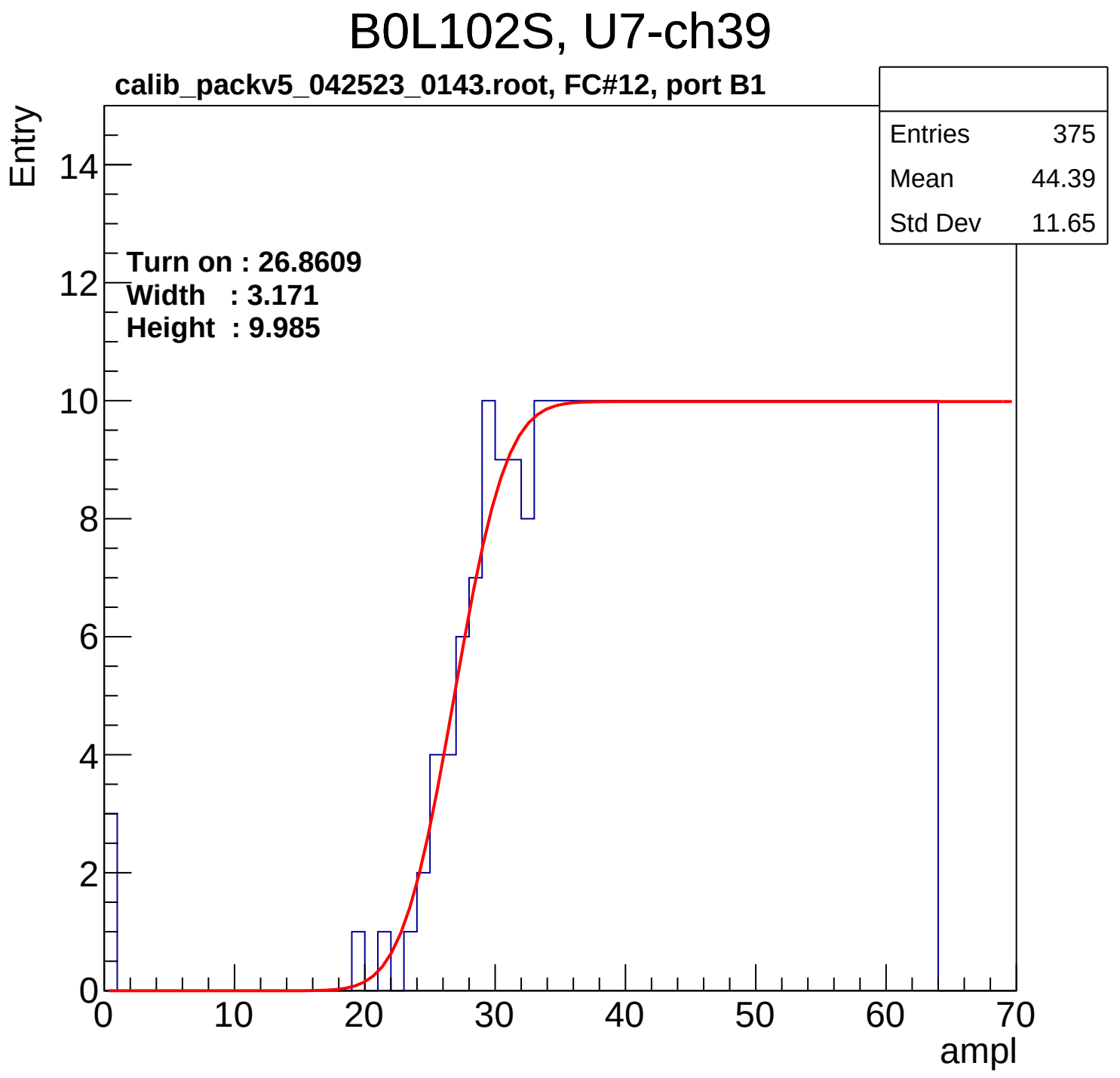
B0L102S, U7-ch39
calib_packv5_042523_0143.root, FC#12, port B1
Entries 375
Mean 44.39
Std Dev 11.65
Turn on : 26.8609
Width : 3.171
Height : 9.985
Entry
ampl
0
2
4
6
8
10
12
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0
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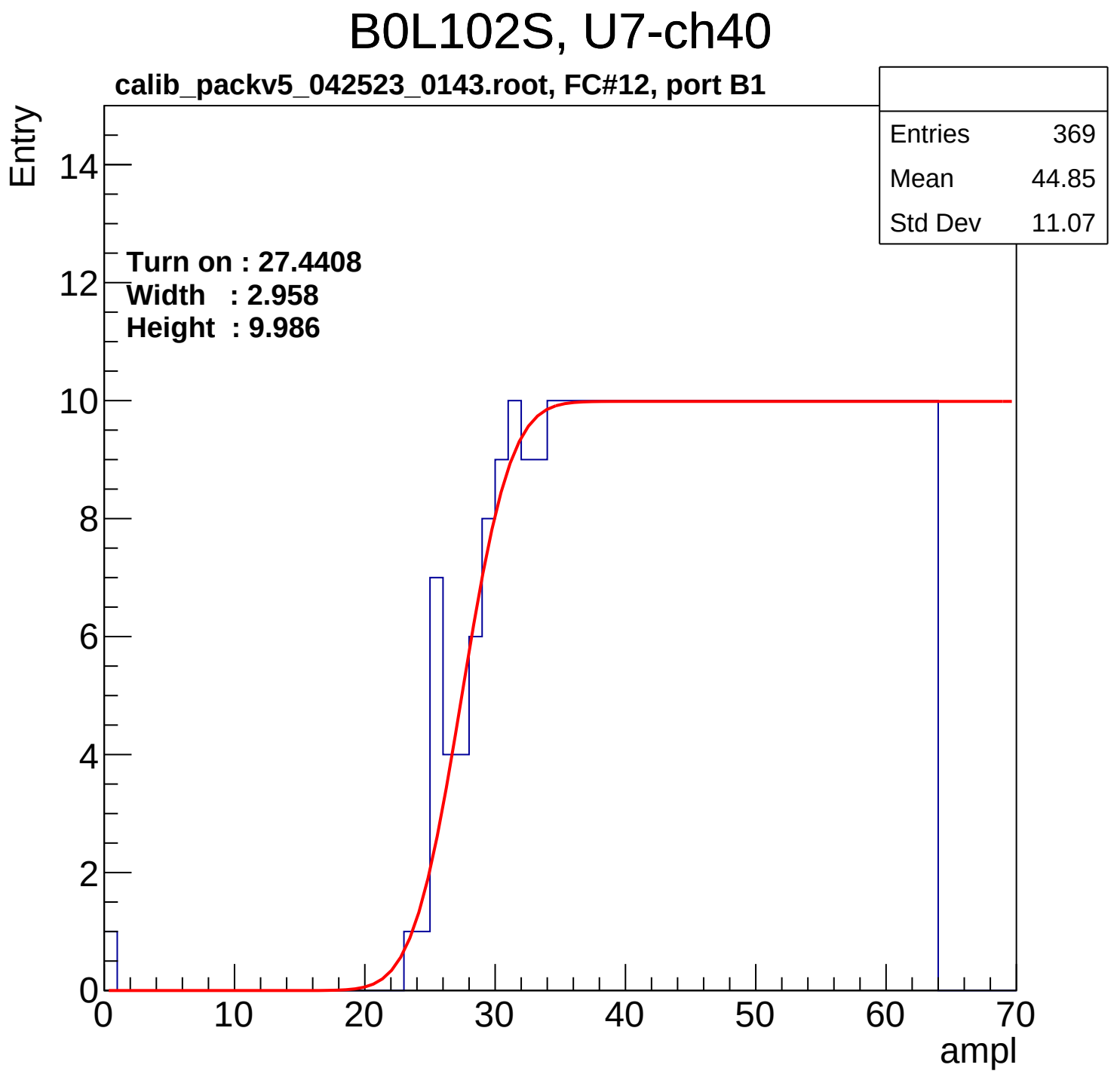
B0L102S, U7-ch40
calib_packv5_042523_0143.root, FC#12, port B1
Entries 369
Mean 44.85
Std Dev 11.07
Turn on : 27.4408
Width : 2.958
Height : 9.986
Entry
ampl
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6
8
10
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0
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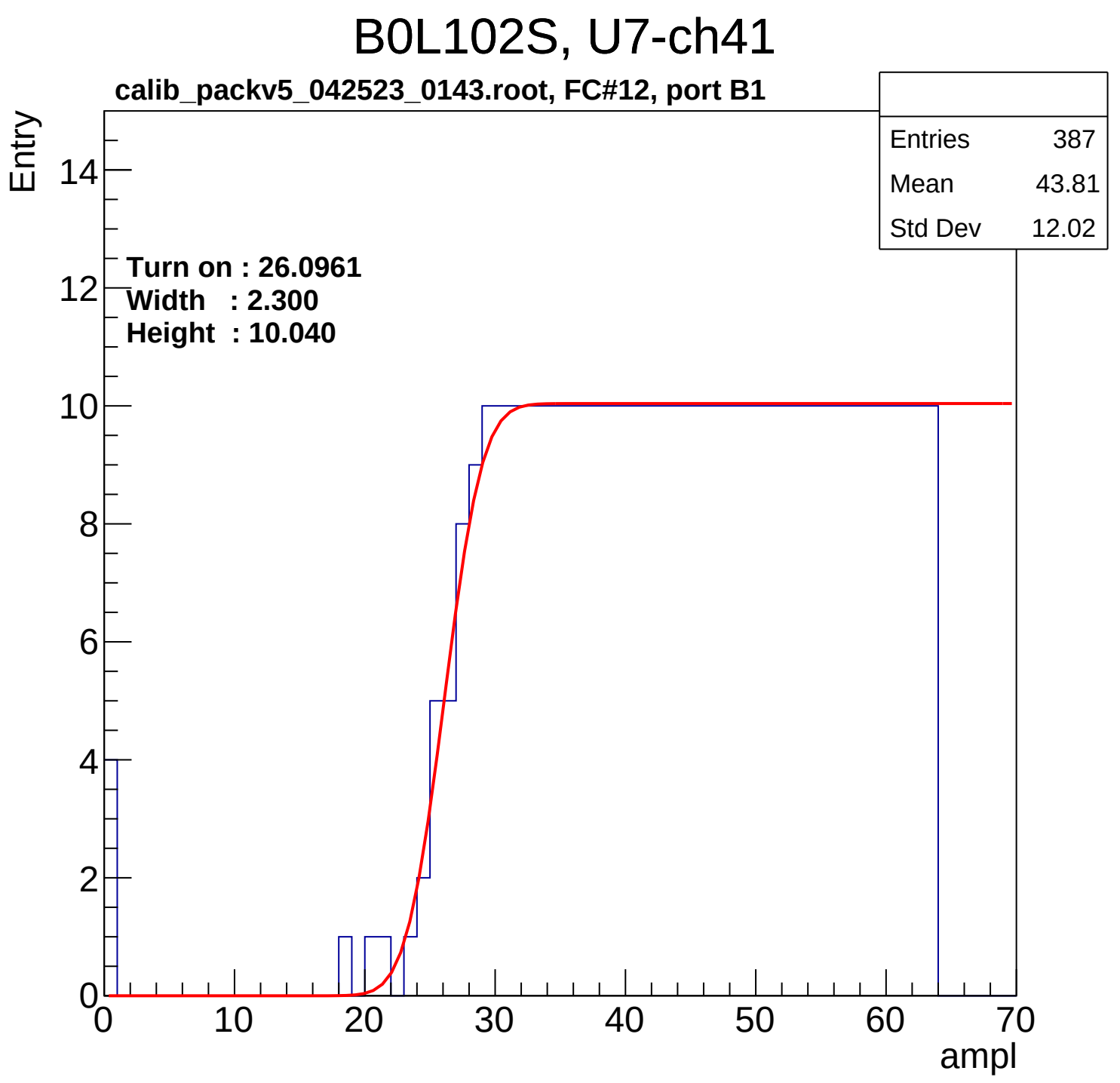
B0L102S, U7-ch41
calib_packv5_042523_0143.root, FC#12, port B1
Entries 387
Mean 43.81
Std Dev 12.02
Turn on : 26.0961
Width : 2.300
Height : 10.040
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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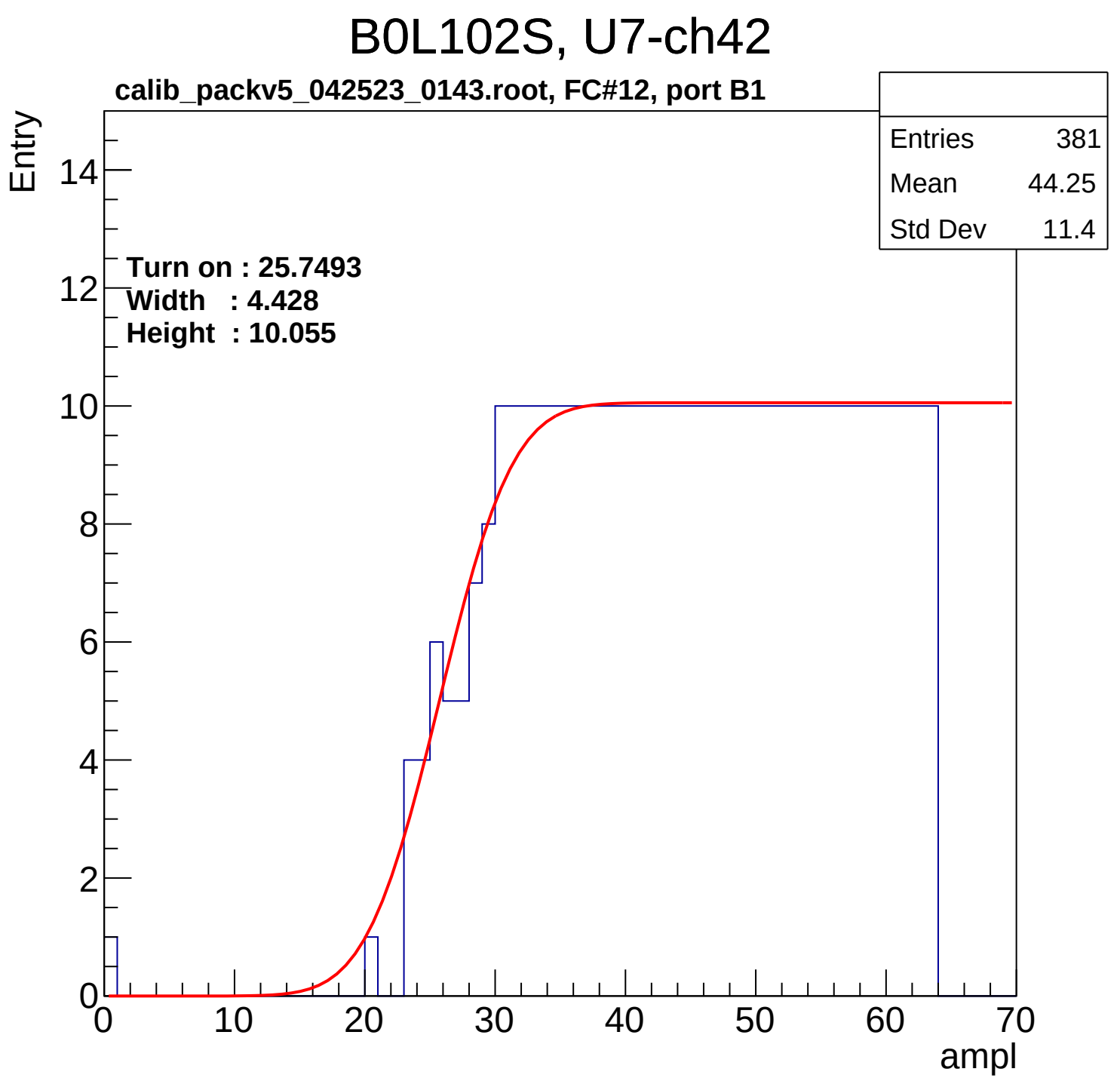
B0L102S, U7-ch42
calib_packv5_042523_0143.root, FC#12, port B1
Entries 381
Mean 44.25
Std Dev 11.4
Turn on : 25.7493
Width : 4.428
Height : 10.055
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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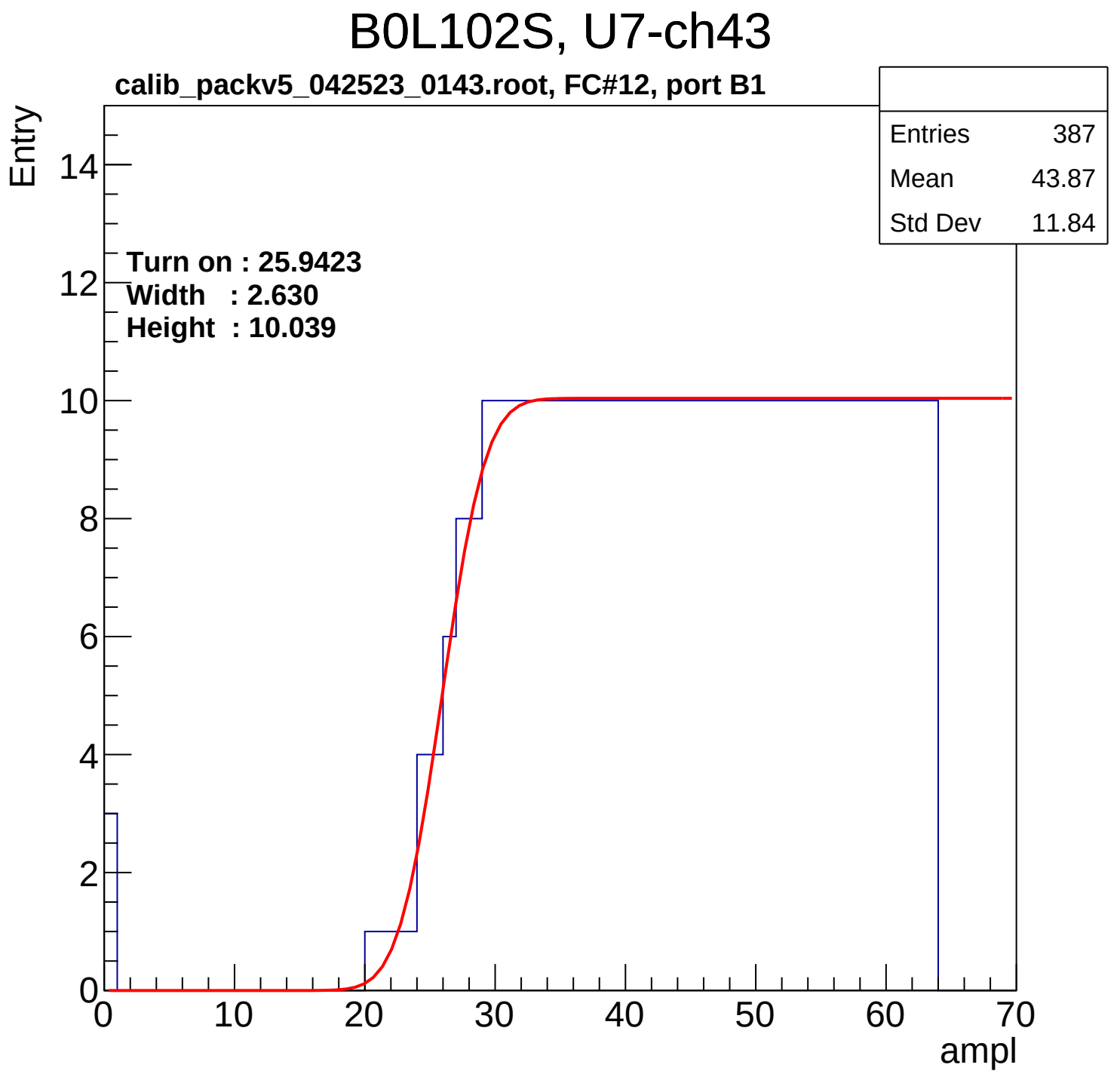
B0L102S, U7-ch43
calib_packv5_042523_0143.root, FC#12, port B1
Entries 387
Mean 43.87
Std Dev 11.84
Turn on : 25.9423
Width : 2.630
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
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0
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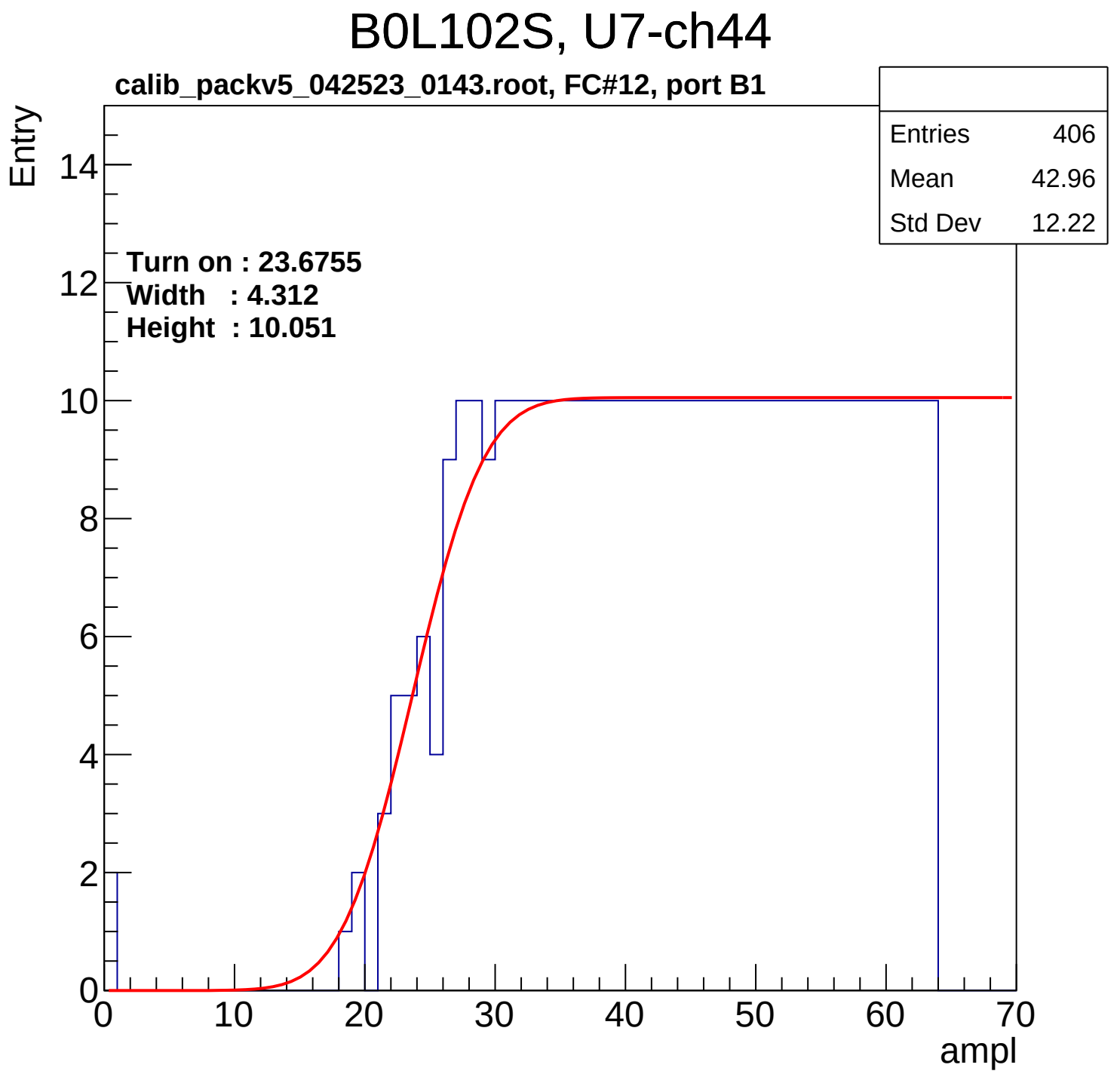
B0L102S, U7-ch44
calib_packv5_042523_0143.root, FC#12, port B1
Entries 406
Mean 42.96
Std Dev 12.22
Turn on : 23.6755
Width : 4.312
Height : 10.051
Entry
ampl
0
2
4
6
8
10
12
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0
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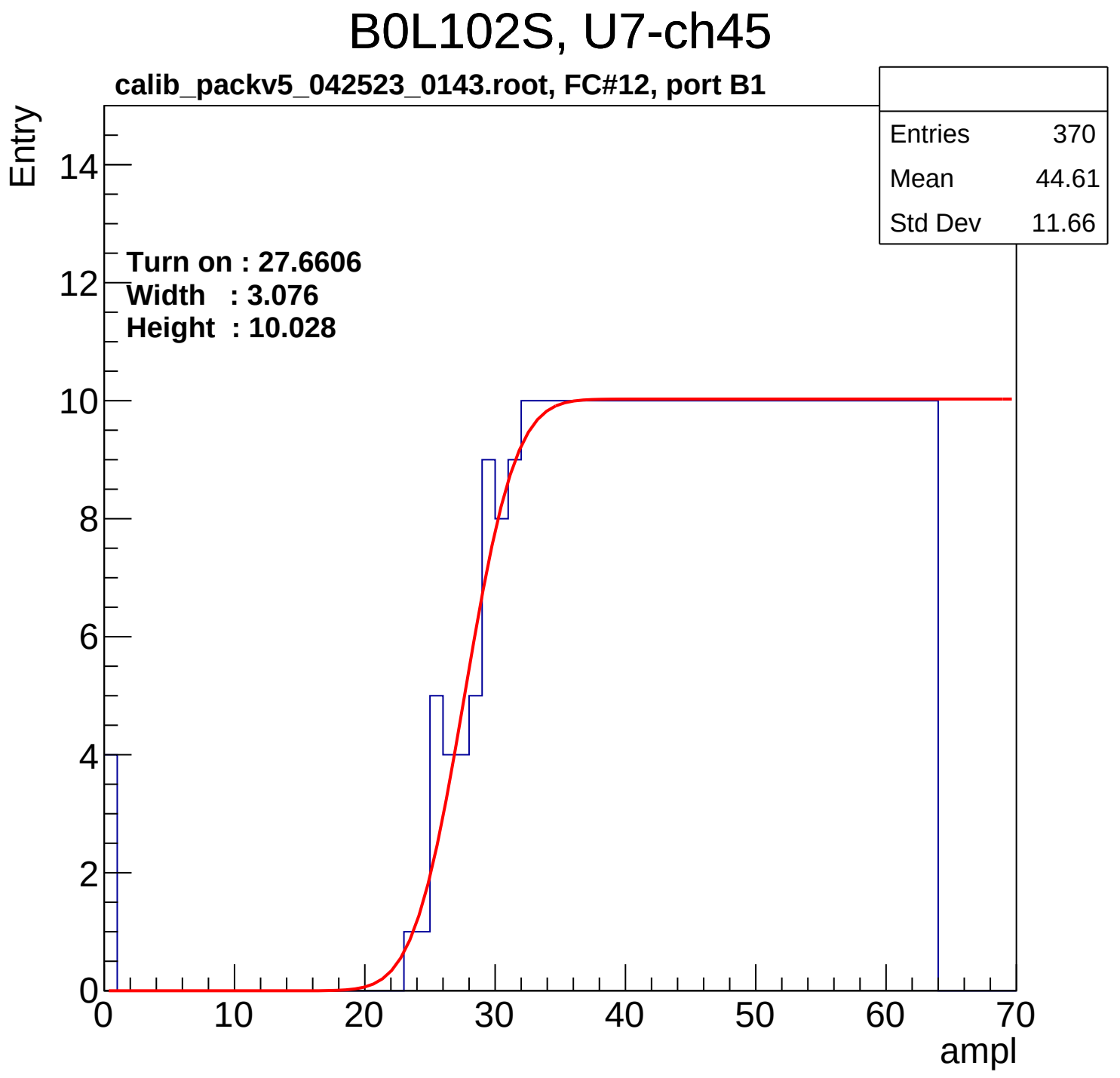
B0L102S, U7-ch45
calib_packv5_042523_0143.root, FC#12, port B1
Entries 370
Mean 44.61
Std Dev 11.66
Turn on : 27.6606
Width : 3.076
Height : 10.028
Entry
ampl
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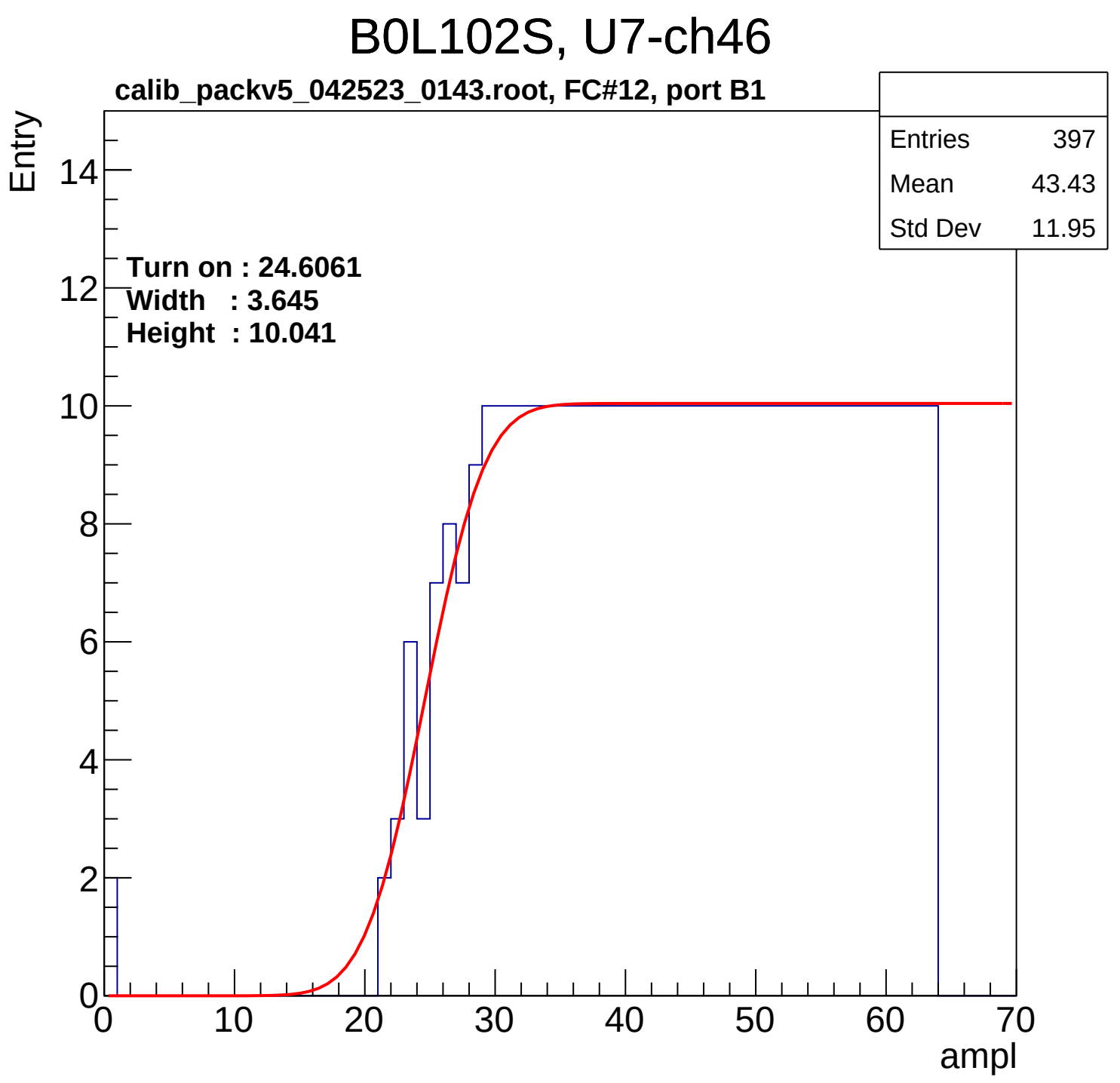
B0L102S, U7-ch46
calib_packv5_042523_0143.root, FC#12, port B1
Entries 397
Mean 43.43
Std Dev 11.95
Turn on : 24.6061
Width : 3.645
Height : 10.041
Entry
ampl
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4
6
8
10
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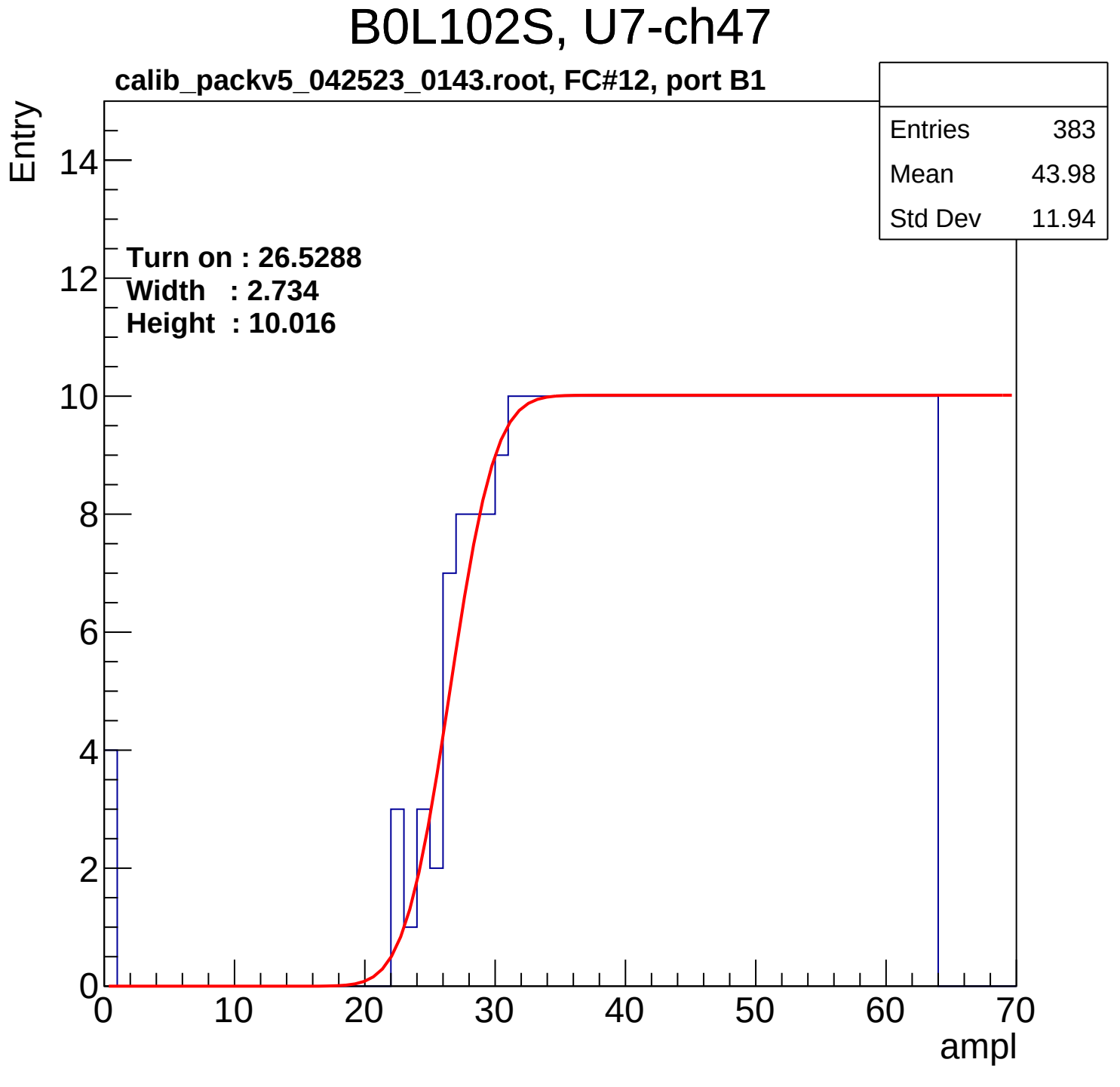
B0L102S, U7-ch47
calib_packv5_042523_0143.root, FC#12, port B1
Entries 383
Mean 43.98
Std Dev 11.94
Turn on : 26.5288
Width : 2.734
Height : 10.016
Entry
ampl
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4
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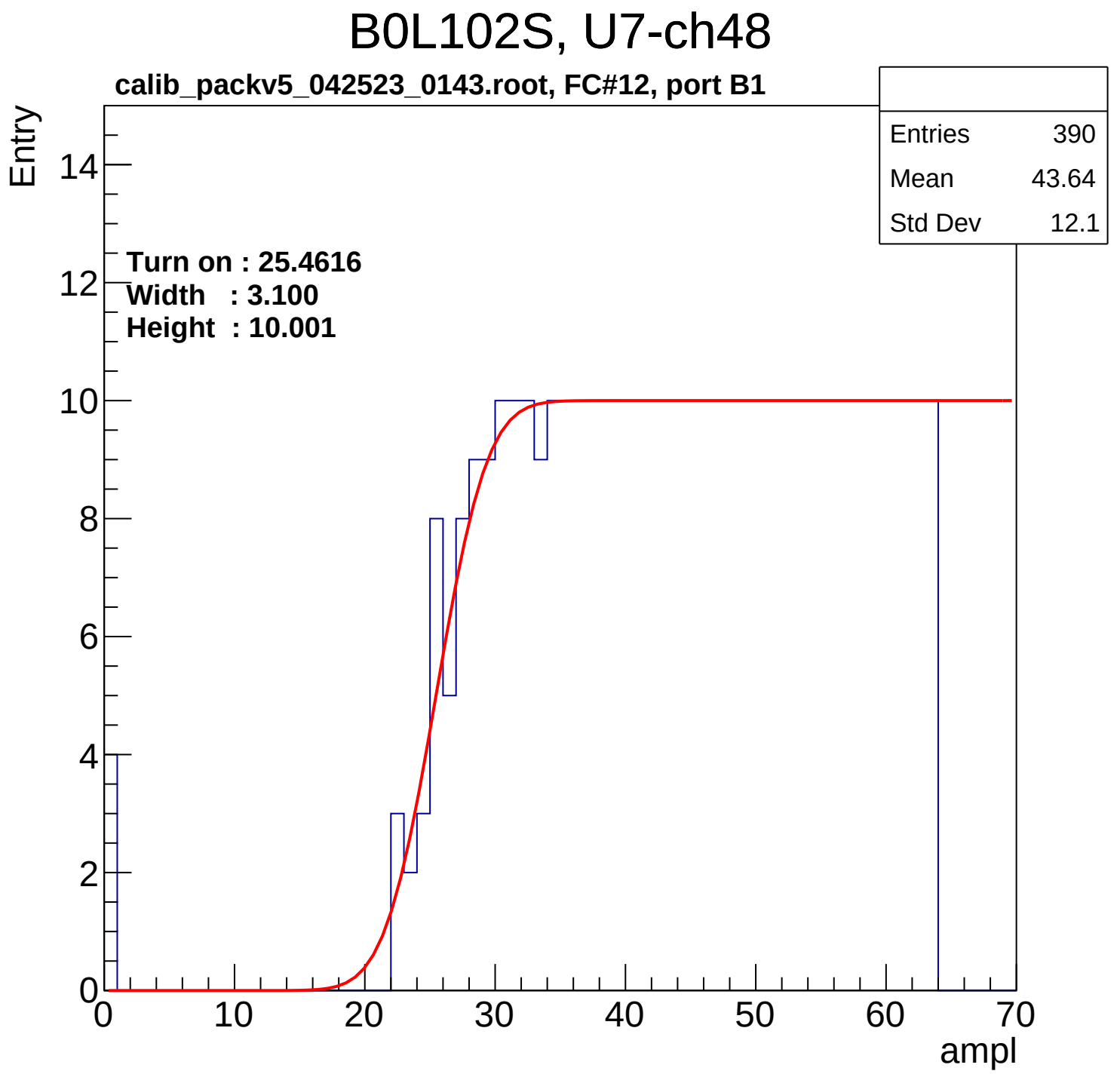
B0L102S, U7-ch48
calib_packv5_042523_0143.root, FC#12, port B1
Entries 390
Mean 43.64
Std Dev 12.1
Turn on : 25.4616
Width : 3.100
Height : 10.001
Entry
ampl
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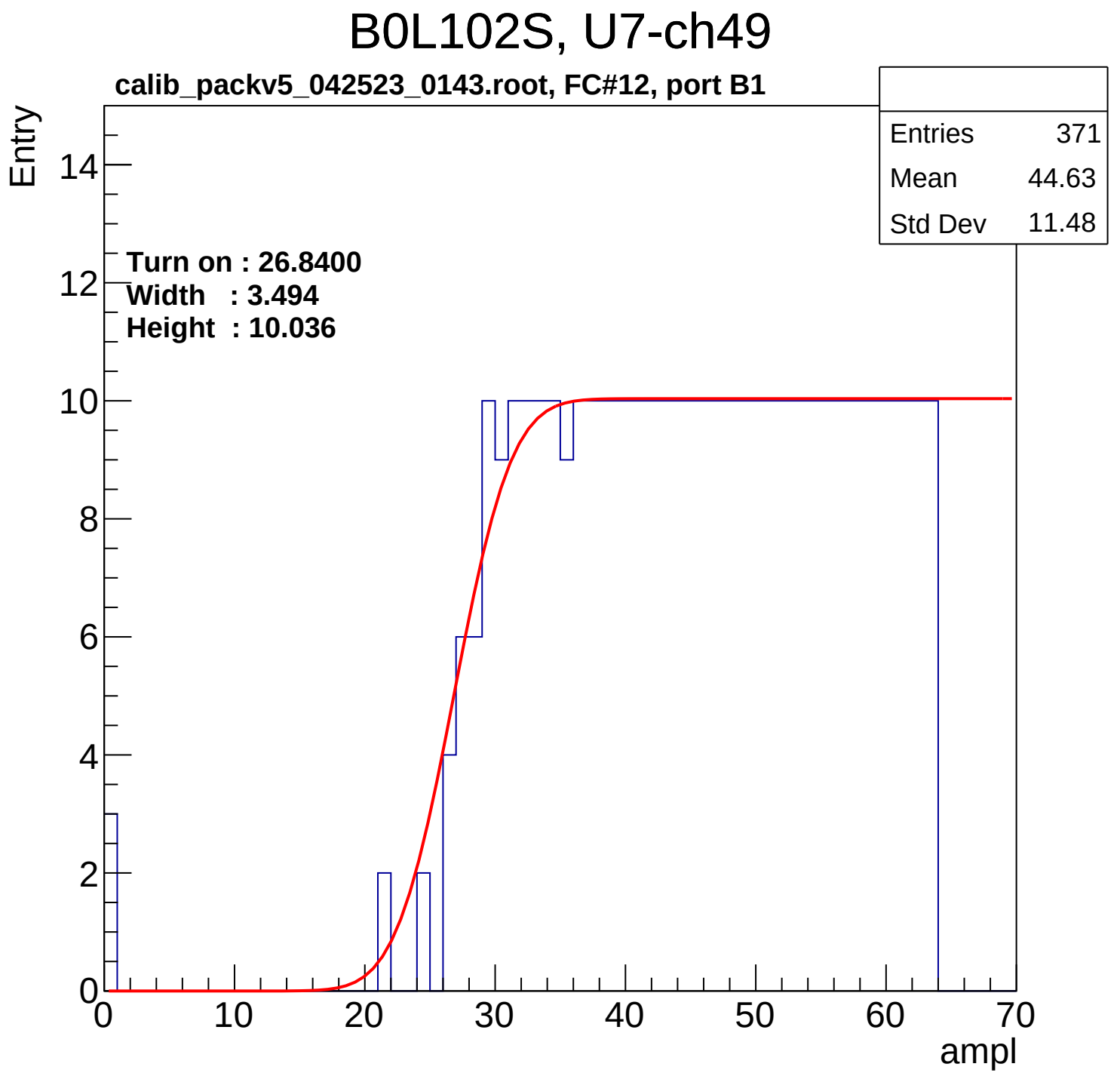
B0L102S, U7-ch49
calib_packv5_042523_0143.root, FC#12, port B1
Entries 371
Mean 44.63
Std Dev 11.48
Turn on : 26.8400
Width : 3.494
Height : 10.036
Entry
ampl
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2
4
6
8
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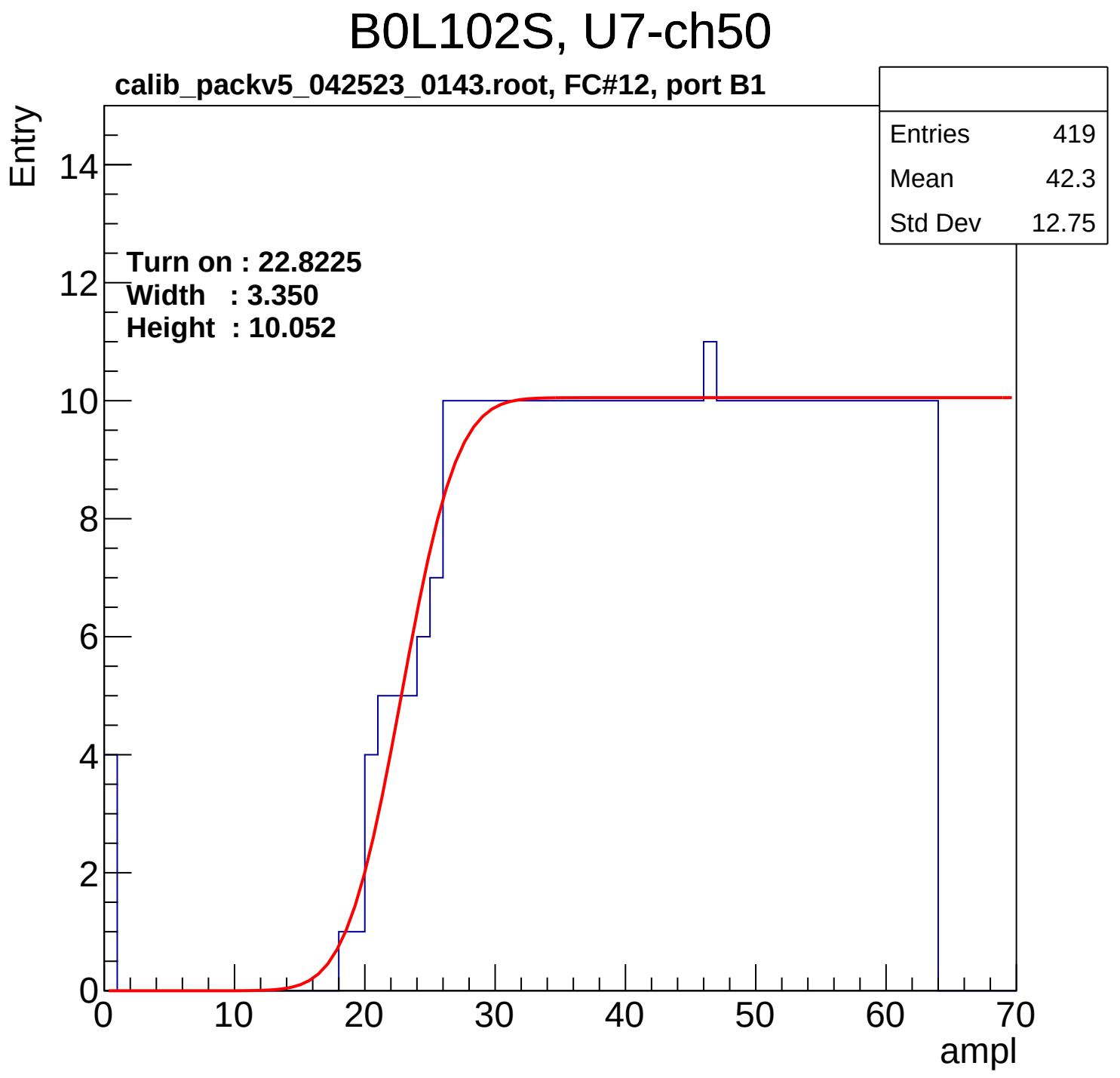
B0L102S, U7-ch50
calib_packv5_042523_0143.root, FC#12, port B1
Entries 419
Mean 42.3
Std Dev 12.75
Turn on : 22.8225
Width : 3.350
Height : 10.052
Entry
ampl
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8
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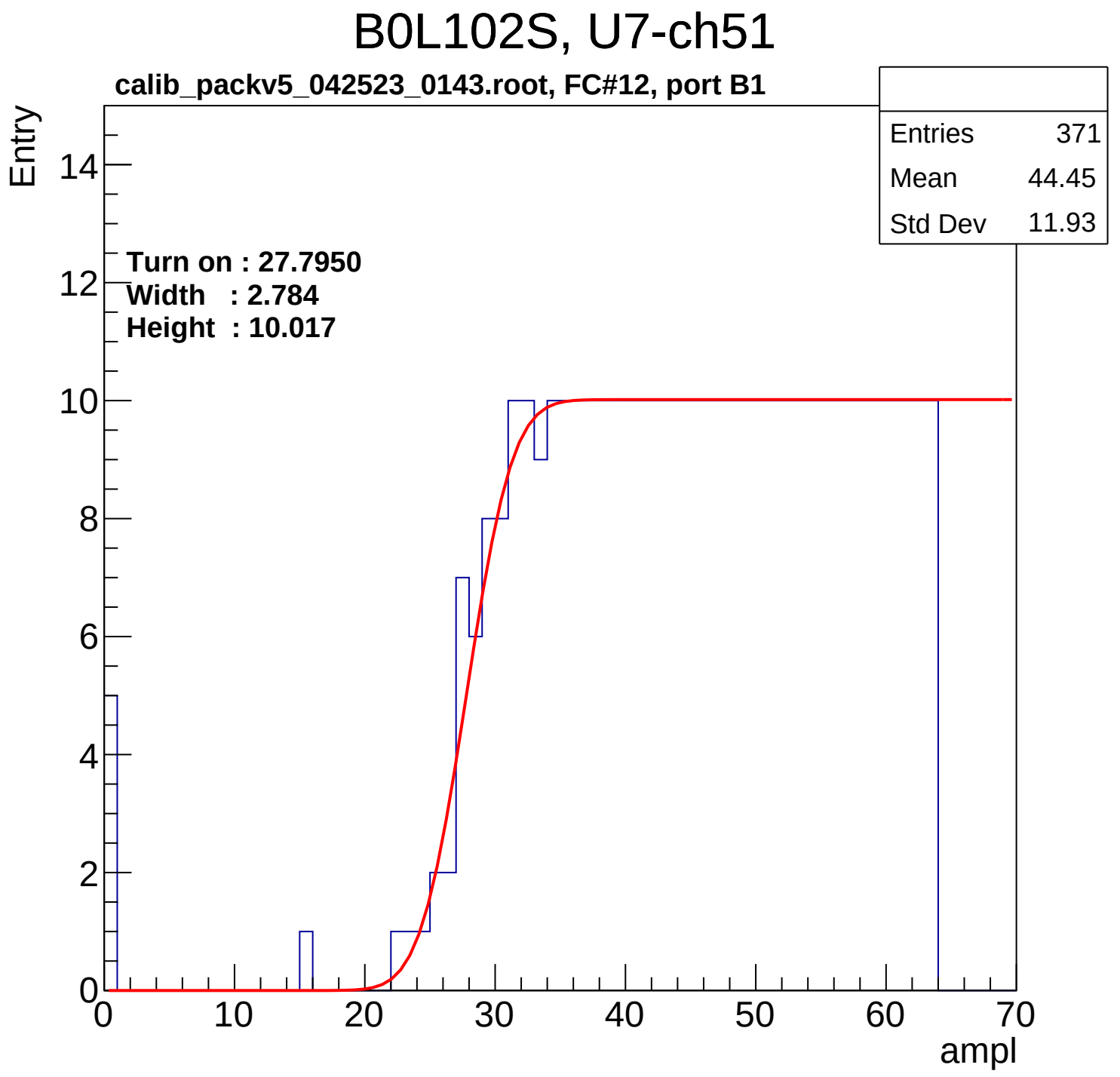
B0L102S, U7-ch51
calib_packv5_042523_0143.root, FC#12, port B1
Entries 371
Mean 44.45
Std Dev 11.93
Turn on : 27.7950
Width : 2.784
Height : 10.017
Entry
ampl
0
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8
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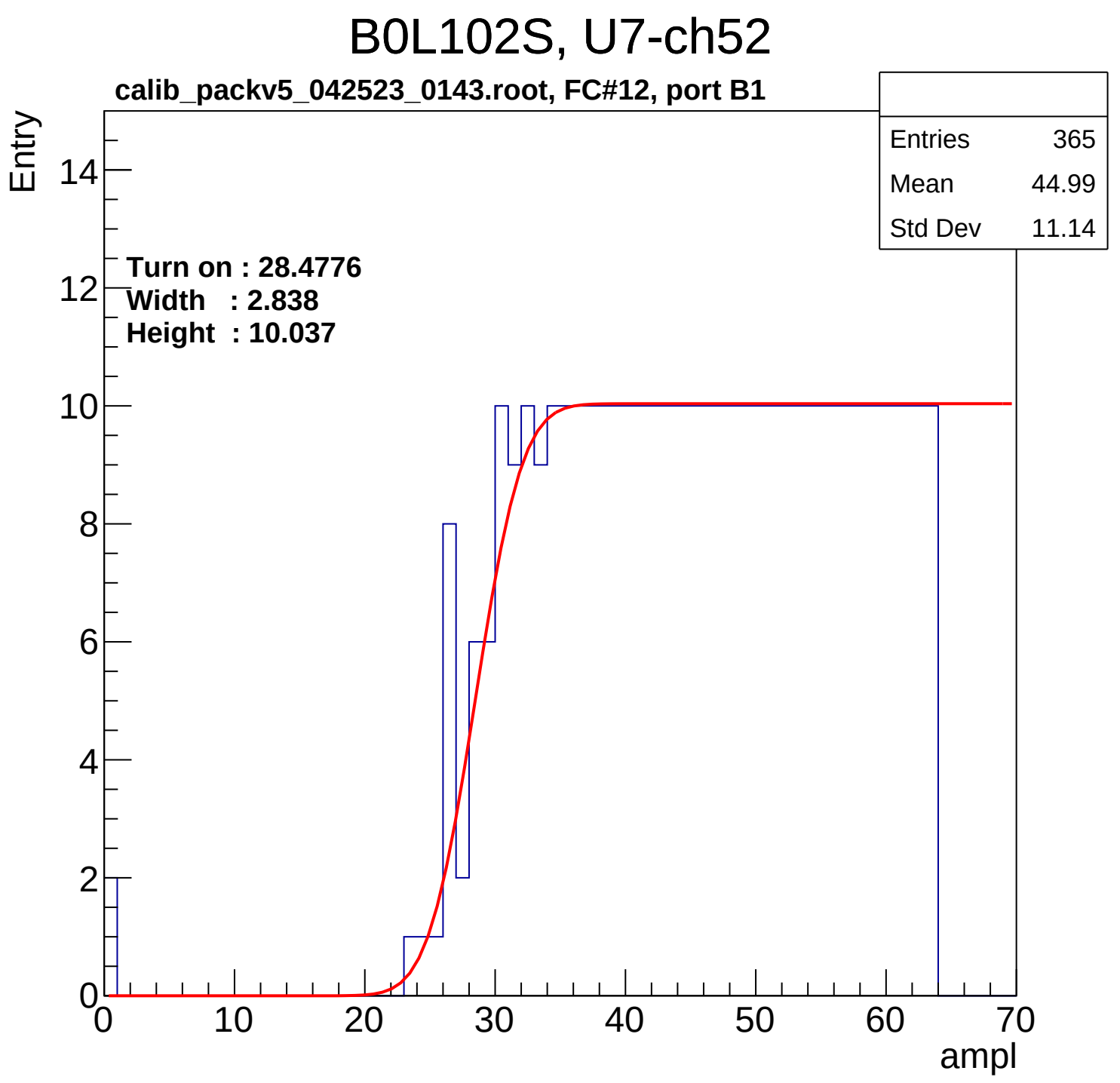
B0L102S, U7-ch52
calib_packv5_042523_0143.root, FC#12, port B1
Entries 365
Mean 44.99
Std Dev 11.14
Turn on : 28.4776
Width : 2.838
Height : 10.037
Entry
ampl
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8
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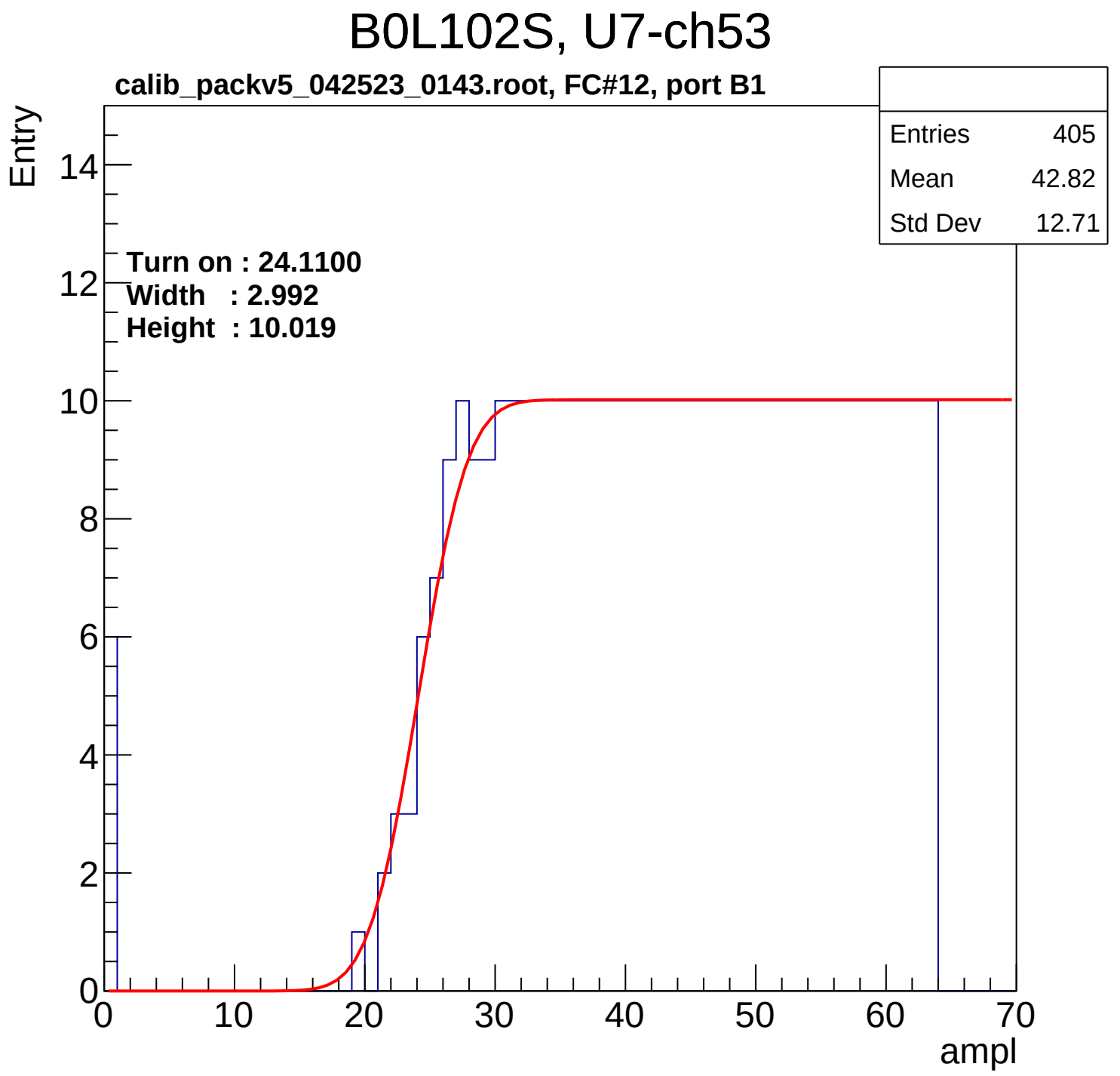
B0L102S, U7-ch53
calib_packv5_042523_0143.root, FC#12, port B1
Entries 405
Mean 42.82
Std Dev 12.71
Turn on : 24.1100
Width : 2.992
Height : 10.019
Entry
ampl
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4
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8
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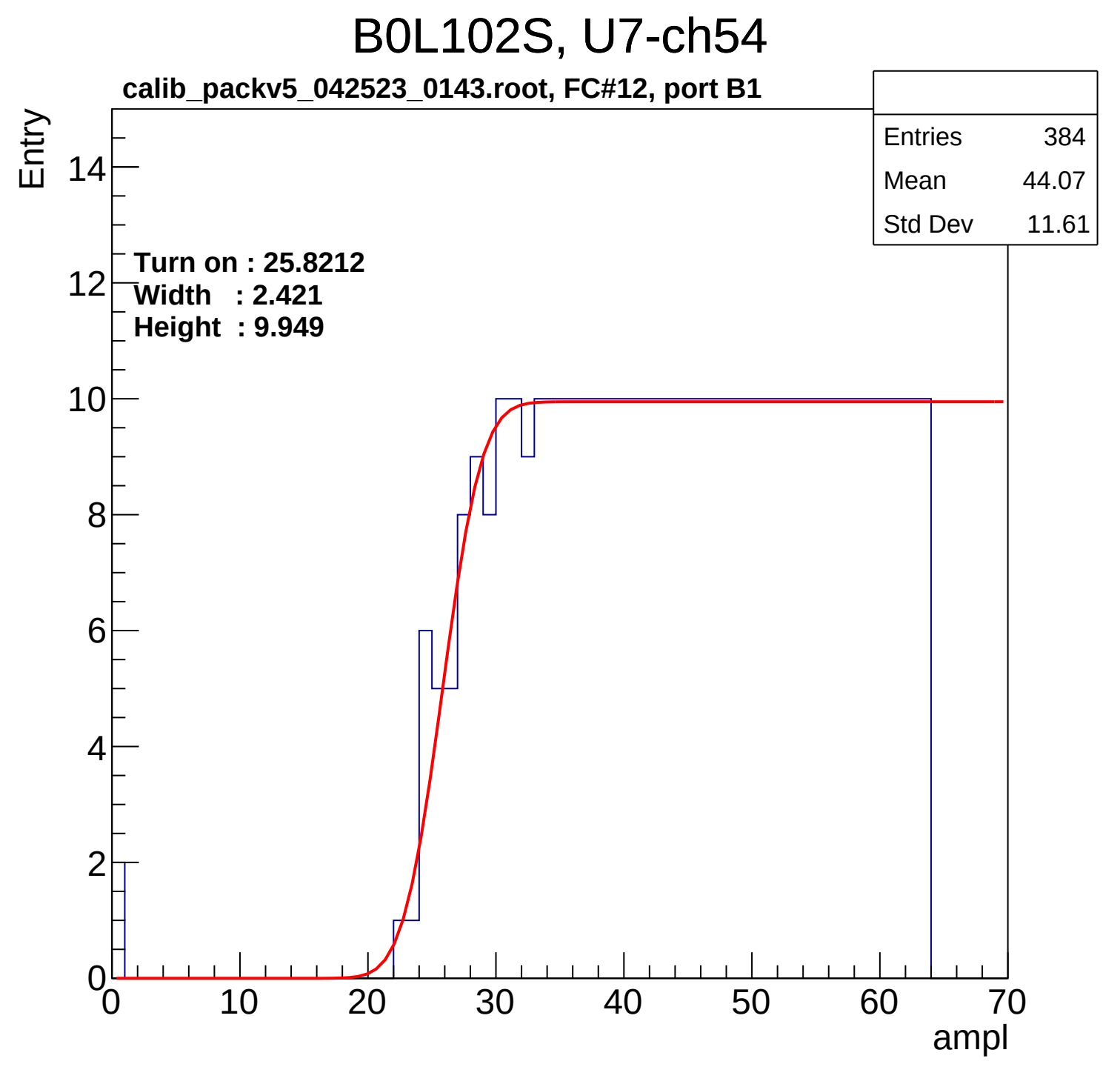
B0L102S, U7-ch54
calib_packv5_042523_0143.root, FC#12, port B1
Entries 384
Mean 44.07
Std Dev 11.61
Turn on : 25.8212
Width : 2.421
Height : 9.949
Entry
ampl
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4
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8
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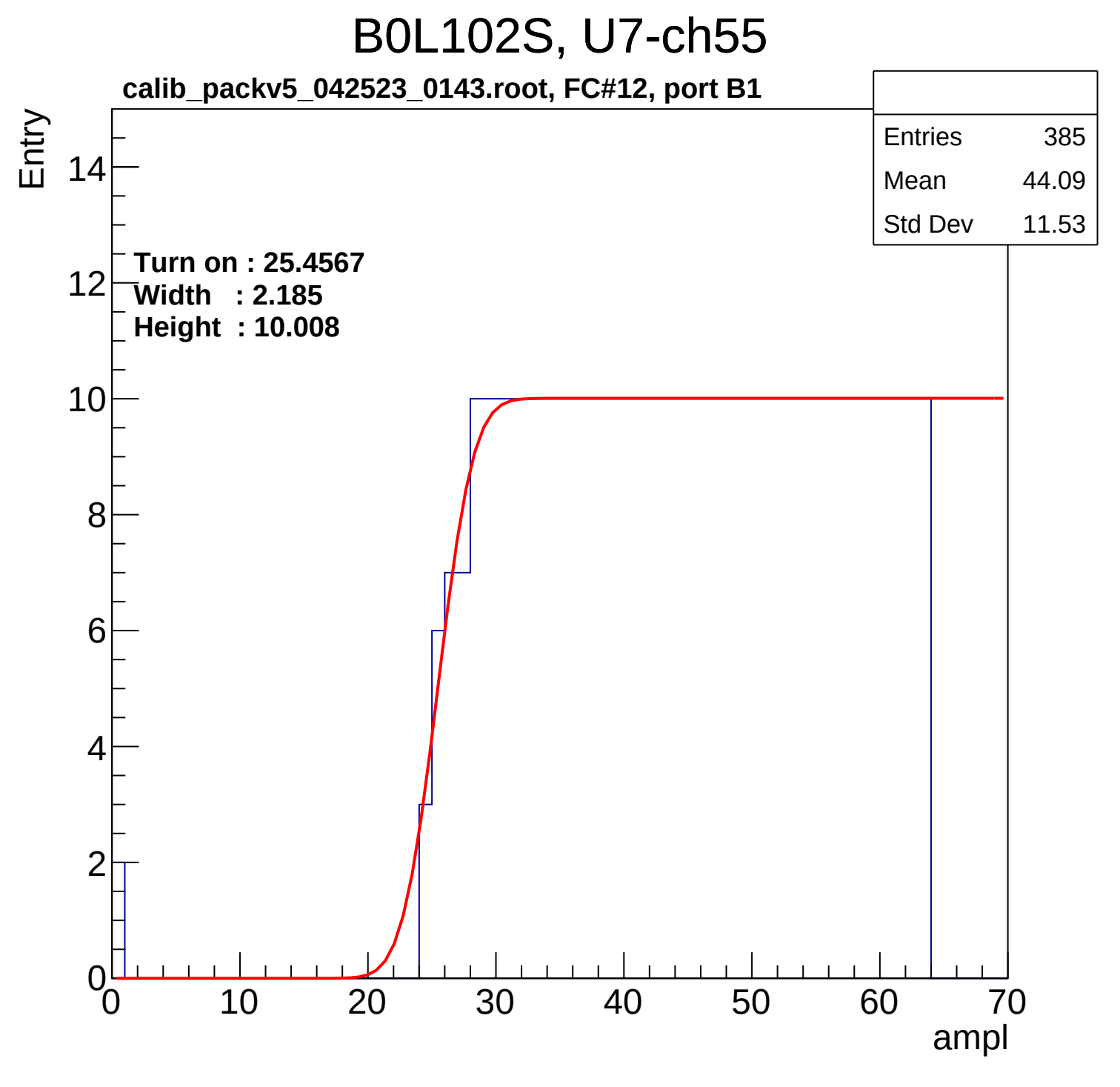
B0L102S, U7-ch55
calib_packv5_042523_0143.root, FC#12, port B1
Entries 385
Mean 44.09
Std Dev 11.53
Turn on : 25.4567
Width : 2.185
Height : 10.008
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ampl
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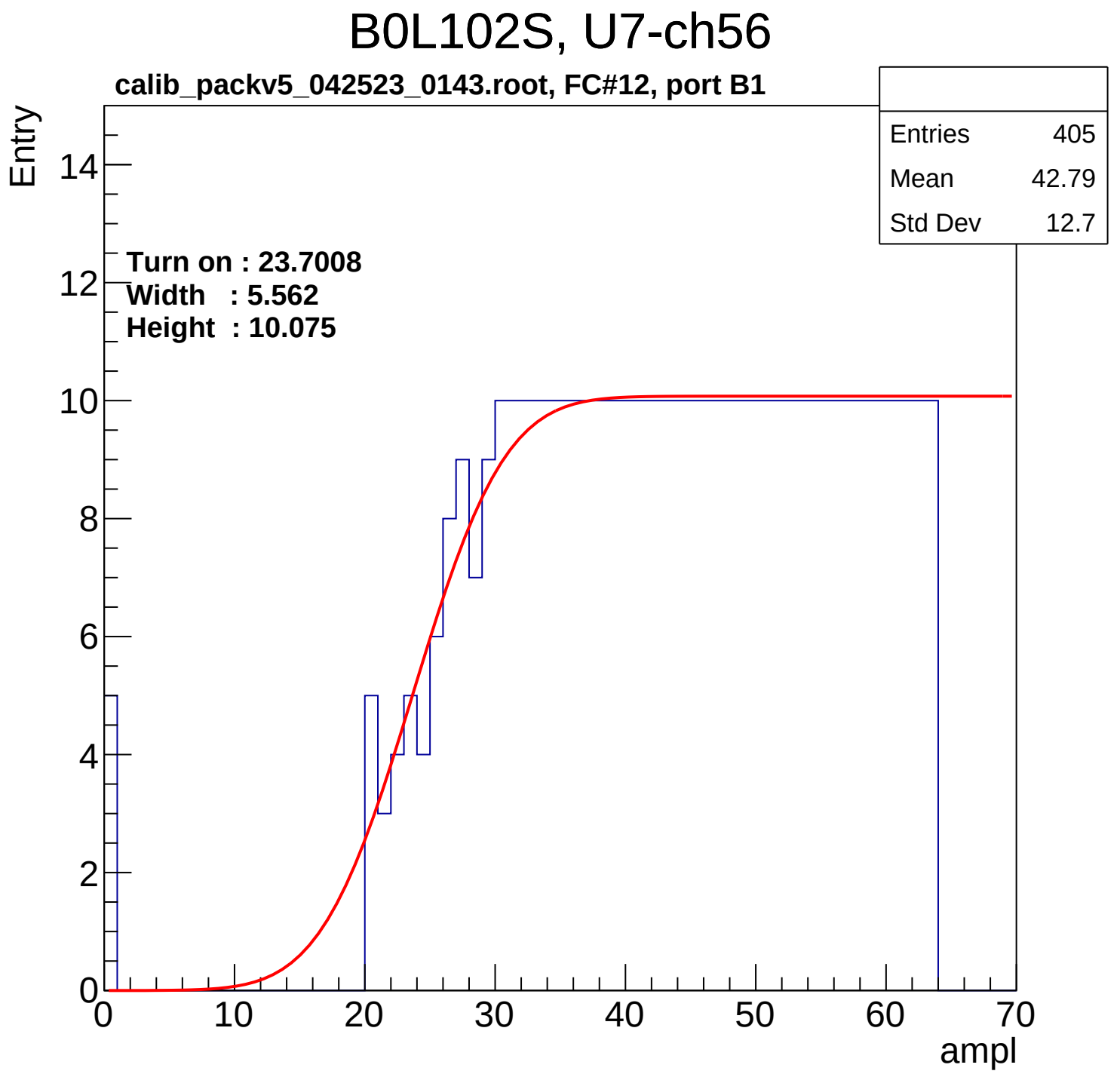
B0L102S, U7-ch56
calib_packv5_042523_0143.root, FC#12, port B1
Entries 405
Mean 42.79
Std Dev 12.7
Turn on : 23.7008
Width : 5.562
Height : 10.075
Entry
ampl
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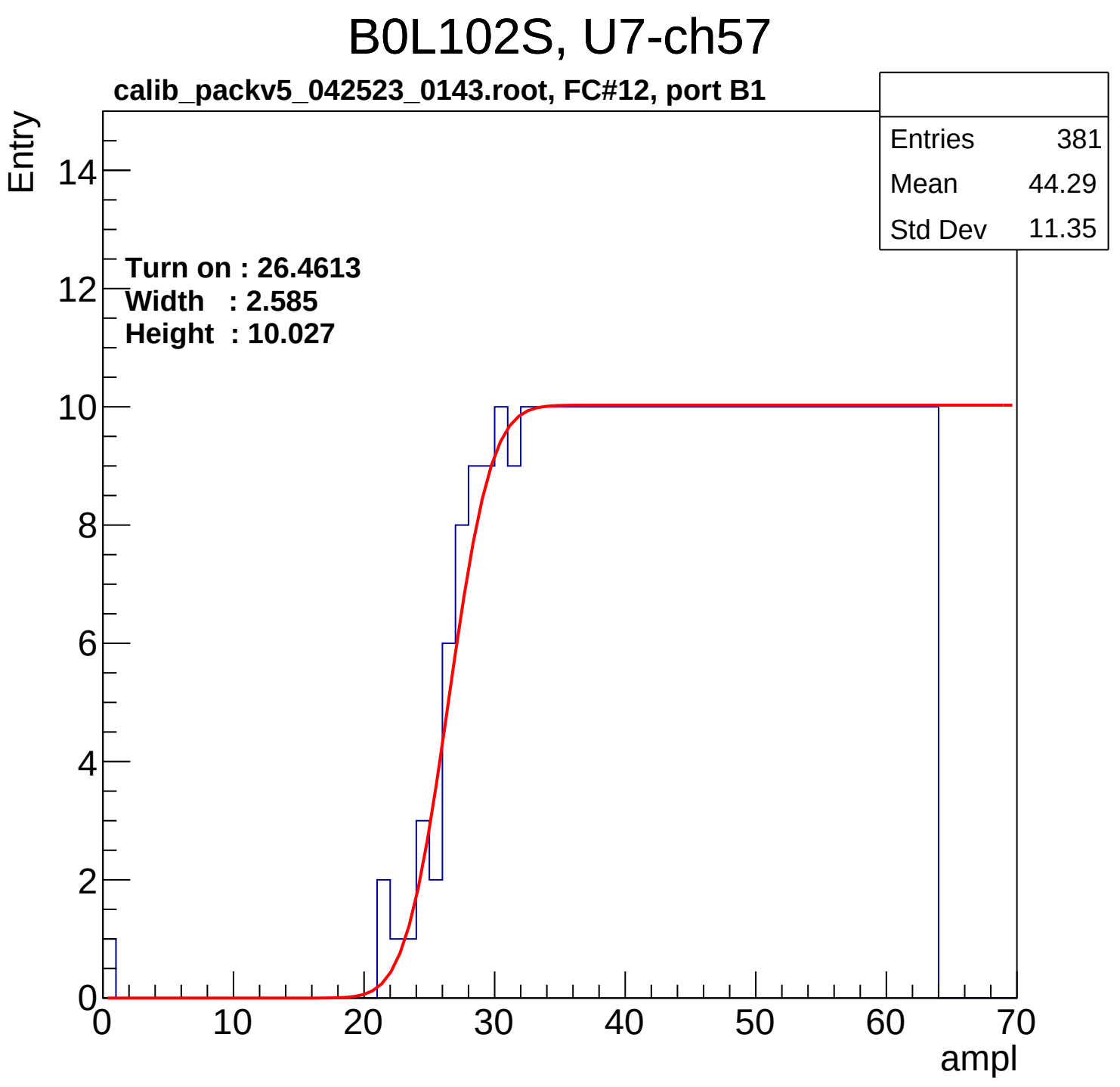
B0L102S, U7-ch57
calib_packv5_042523_0143.root, FC#12, port B1
Entries 381
Mean 44.29
Std Dev 11.35
Turn on : 26.4613
Width : 2.585
Height : 10.027
Entry
ampl
0
2
4
6
8
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12
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20
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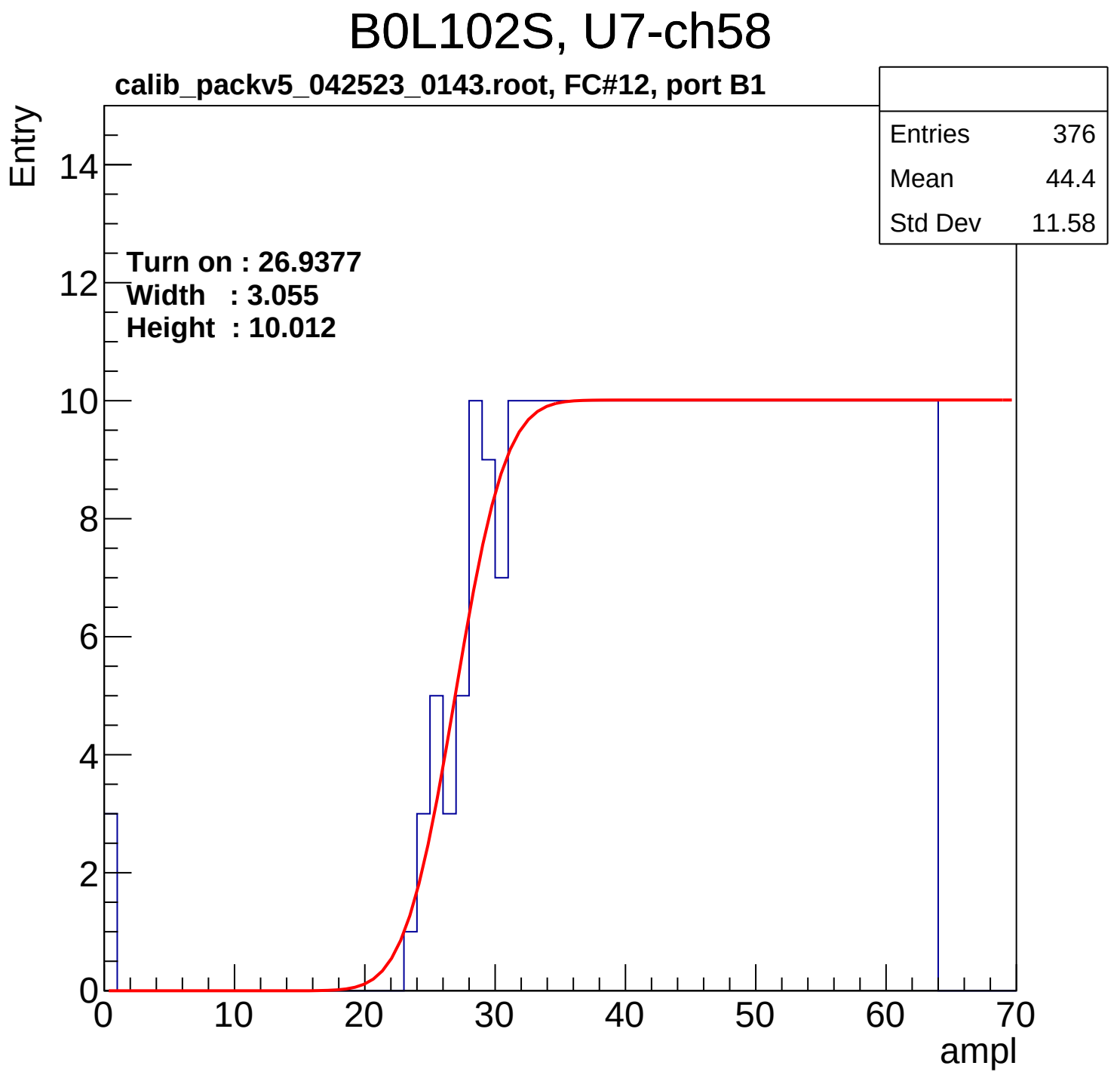
B0L102S, U7-ch58
calib_packv5_042523_0143.root, FC#12, port B1
Entries 376
Mean 44.4
Std Dev 11.58
Turn on : 26.9377
Width : 3.055
Height : 10.012
Entry
ampl
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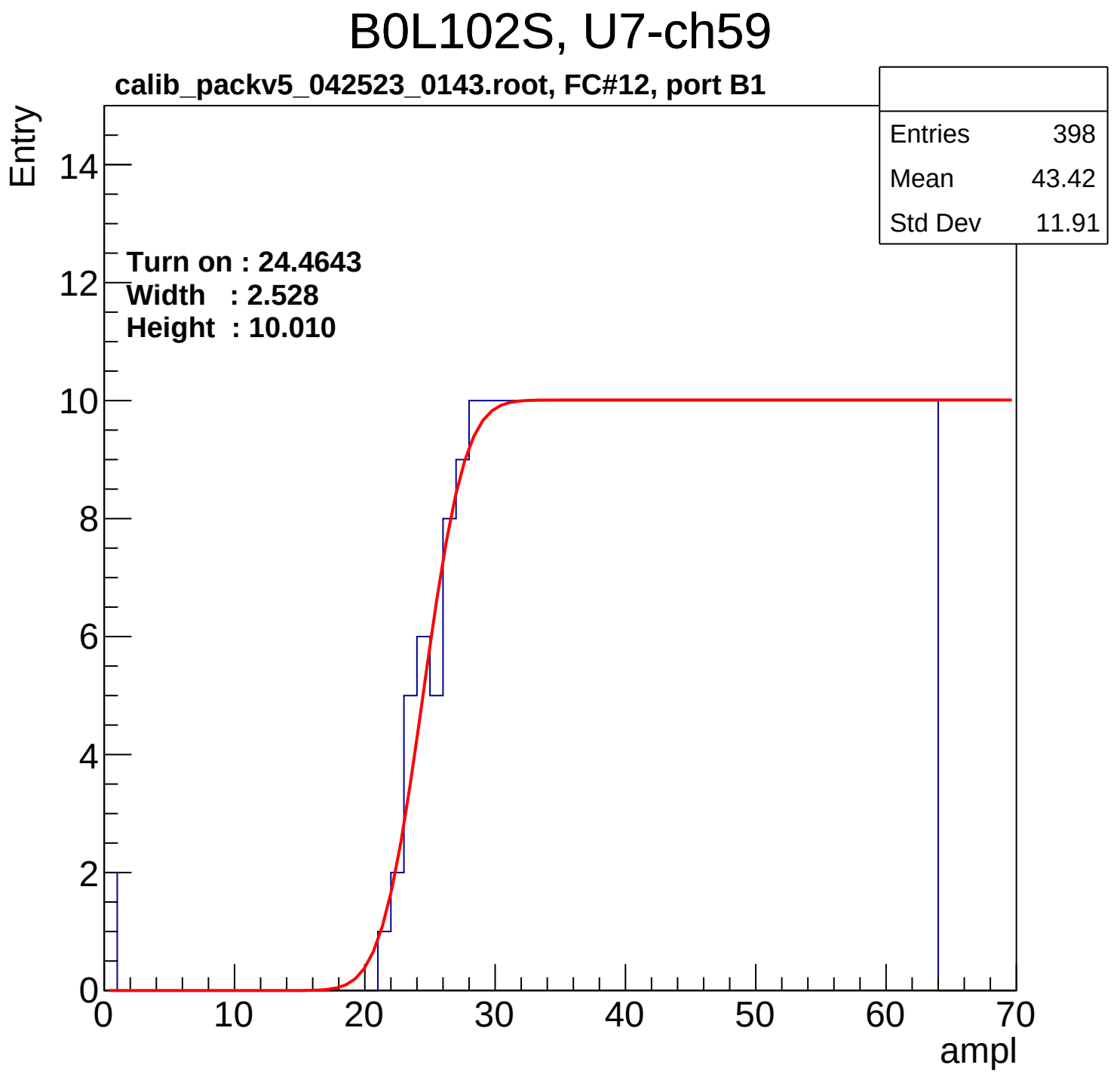
B0L102S, U7-ch59
calib_packv5_042523_0143.root, FC#12, port B1
Entries 398
Mean 43.42
Std Dev 11.91
Turn on : 24.4643
Width : 2.528
Height : 10.010
Entry
ampl
0
2
4
6
8
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0
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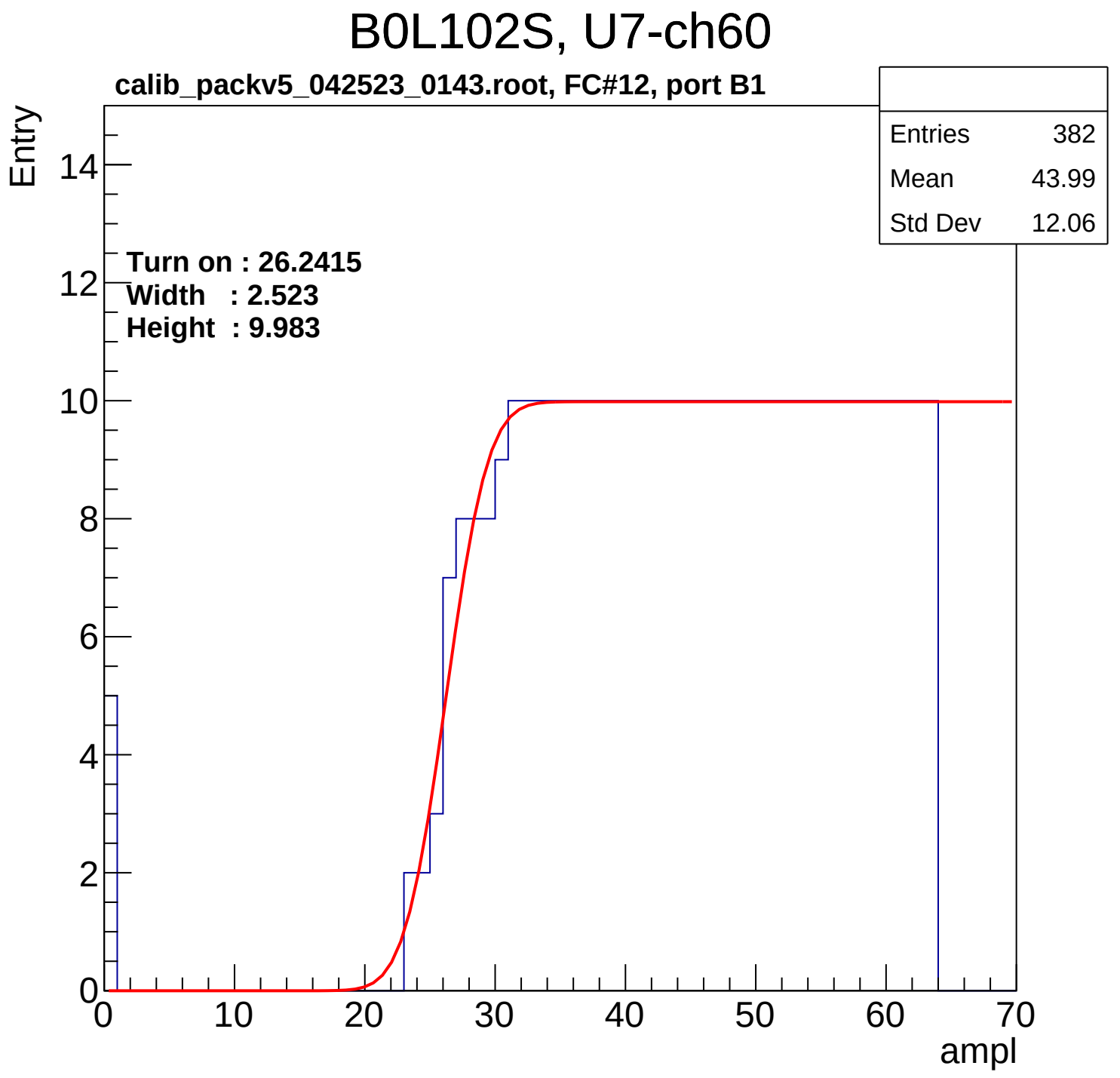
B0L102S, U7-ch60
calib_packv5_042523_0143.root, FC#12, port B1
Entries 382
Mean 43.99
Std Dev 12.06
Turn on : 26.2415
Width : 2.523
Height : 9.983
Entry
ampl
0
2
4
6
8
10
12
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0
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40
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60
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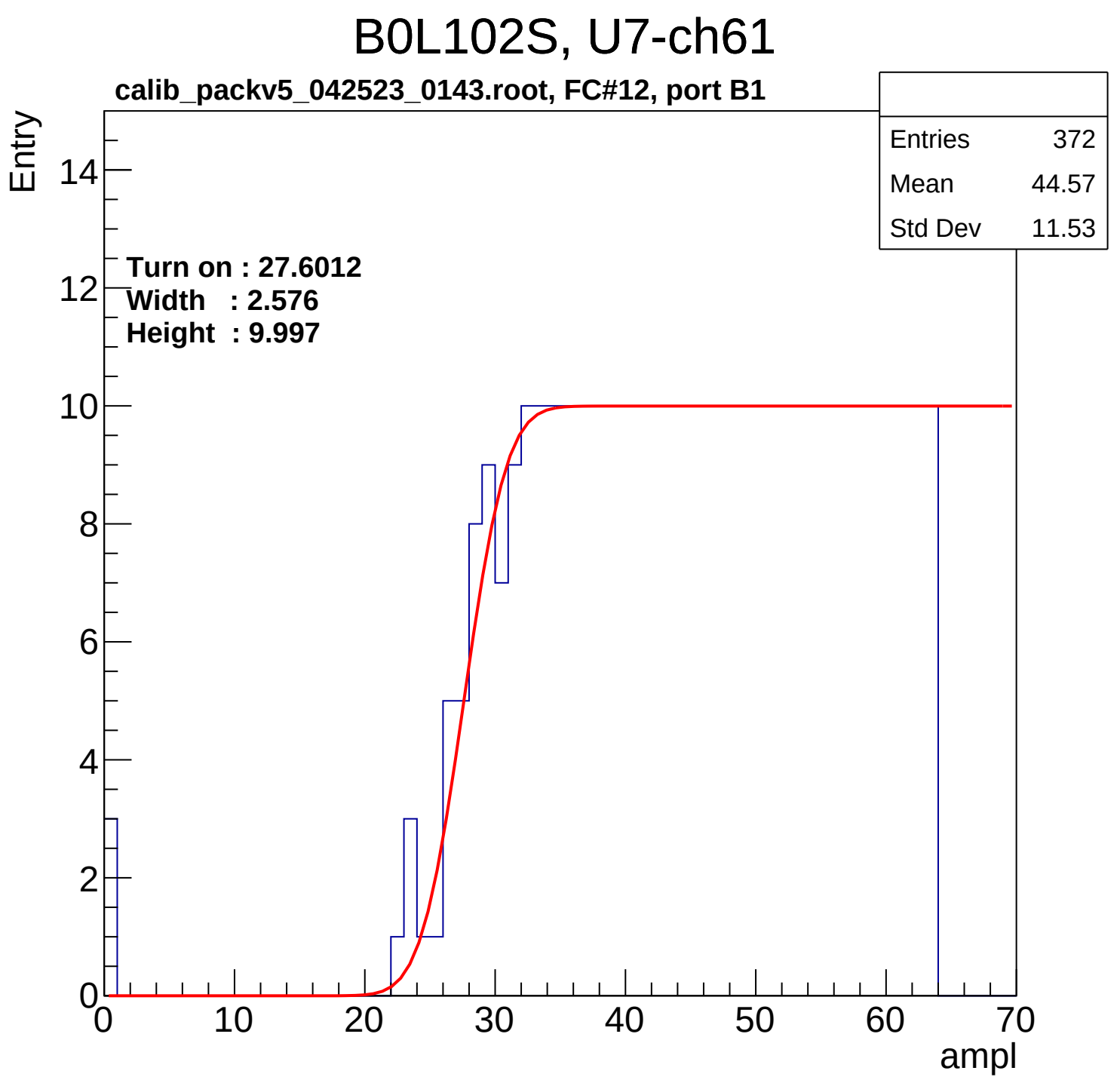
B0L102S, U7-ch61
calib_packv5_042523_0143.root, FC#12, port B1
Entries 372
Mean 44.57
Std Dev 11.53
Turn on : 27.6012
Width : 2.576
Height : 9.997
Entry
ampl
0
2
4
6
8
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0
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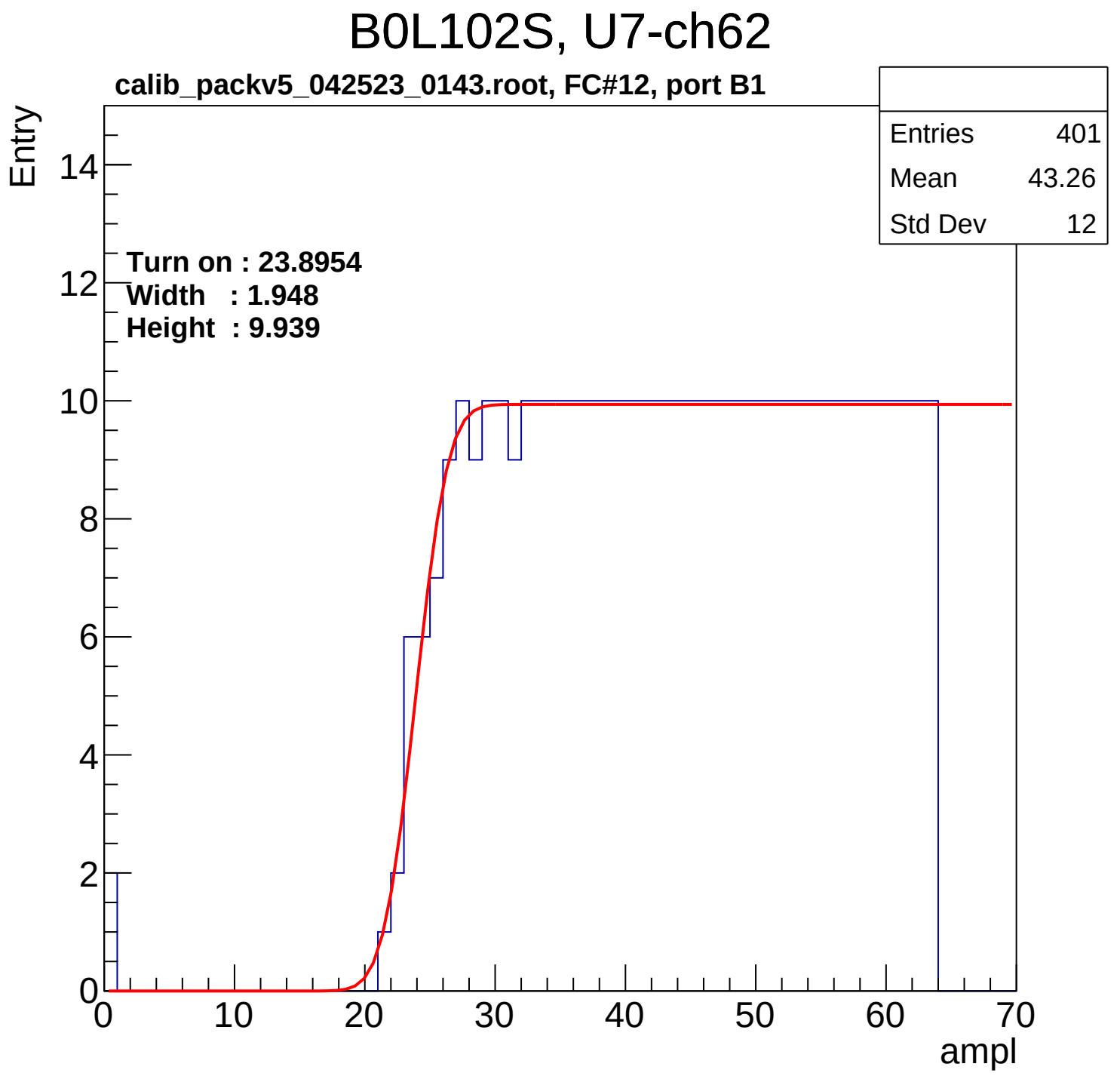
B0L102S, U7-ch62
calib_packv5_042523_0143.root, FC#12, port B1
Entries 401
Mean 43.26
Std Dev 12
Turn on : 23.8954
Width : 1.948
Height : 9.939
Entry
ampl
0
2
4
6
8
10
12
14
0
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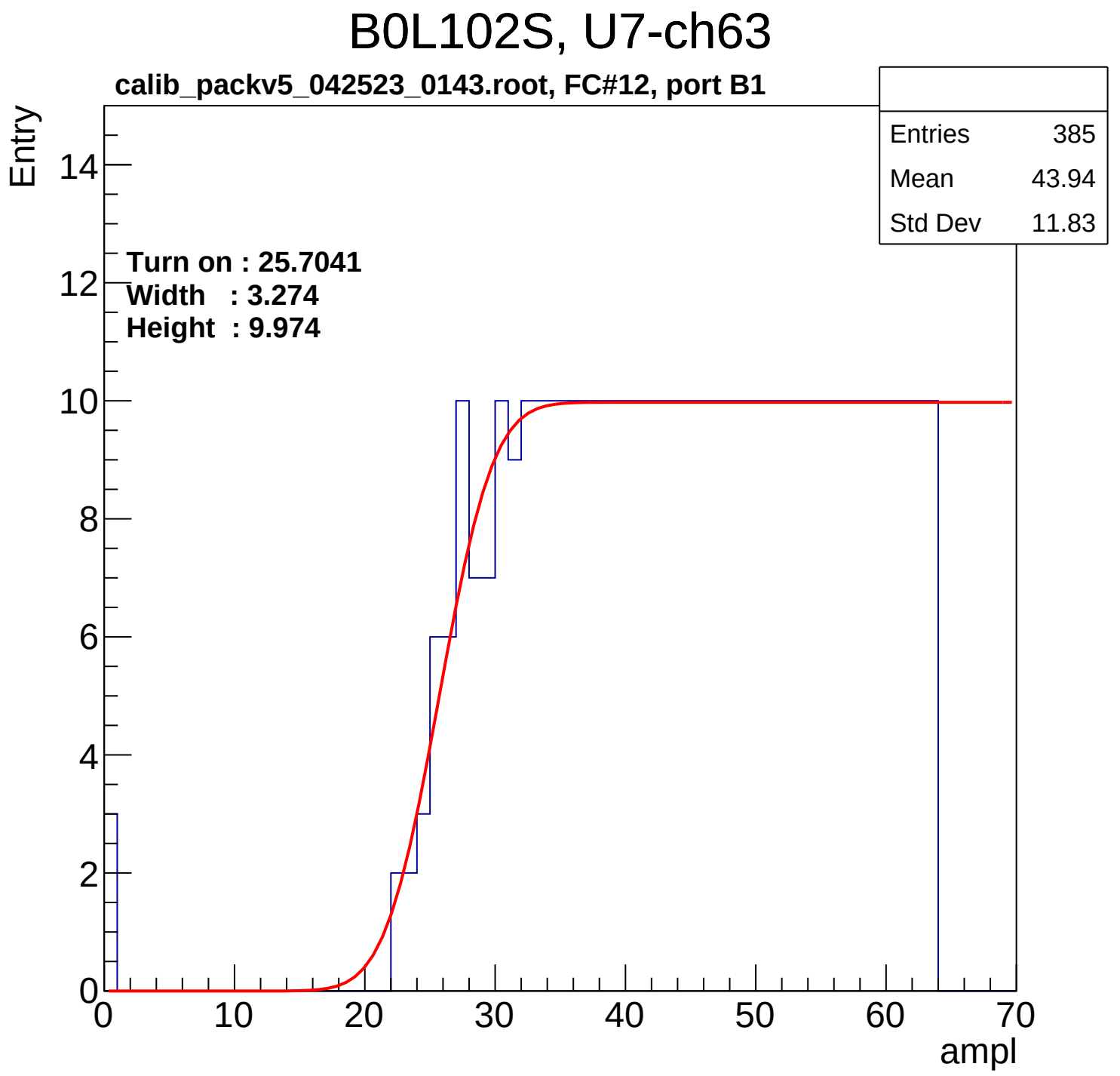
B0L102S, U7-ch63
calib_packv5_042523_0143.root, FC#12, port B1
Entries 385
Mean 43.94
Std Dev 11.83
Turn on : 25.7041
Width : 3.274
Height : 9.974
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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60
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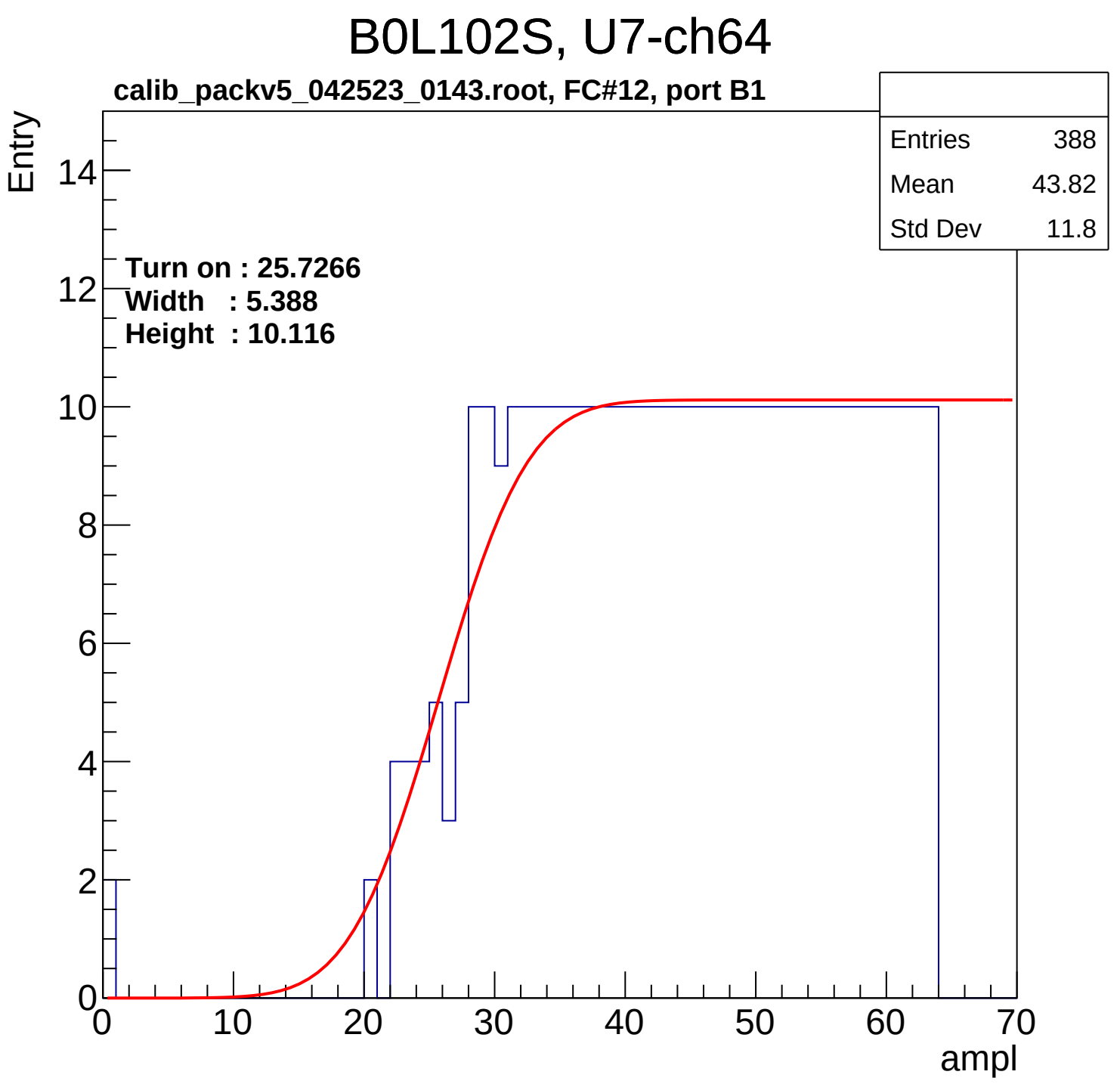
B0L102S, U7-ch64
calib_packv5_042523_0143.root, FC#12, port B1
Entries 388
Mean 43.82
Std Dev 11.8
Turn on : 25.7266
Width : 5.388
Height : 10.116
Entry
ampl
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4
6
8
10
12
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0
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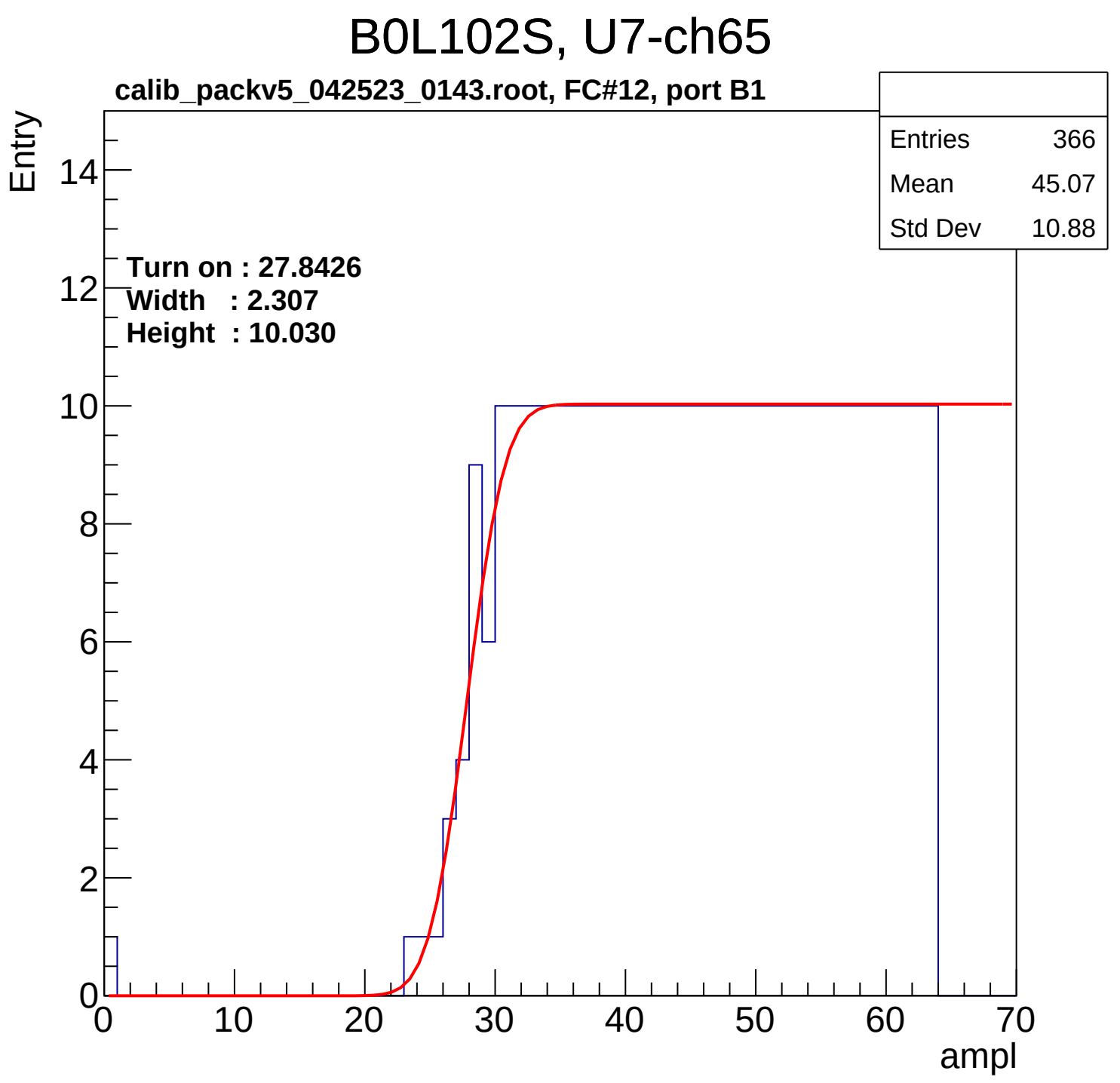
B0L102S, U7-ch65
calib_packv5_042523_0143.root, FC#12, port B1
Entries 366
Mean 45.07
Std Dev 10.88
Turn on : 27.8426
Width : 2.307
Height : 10.030
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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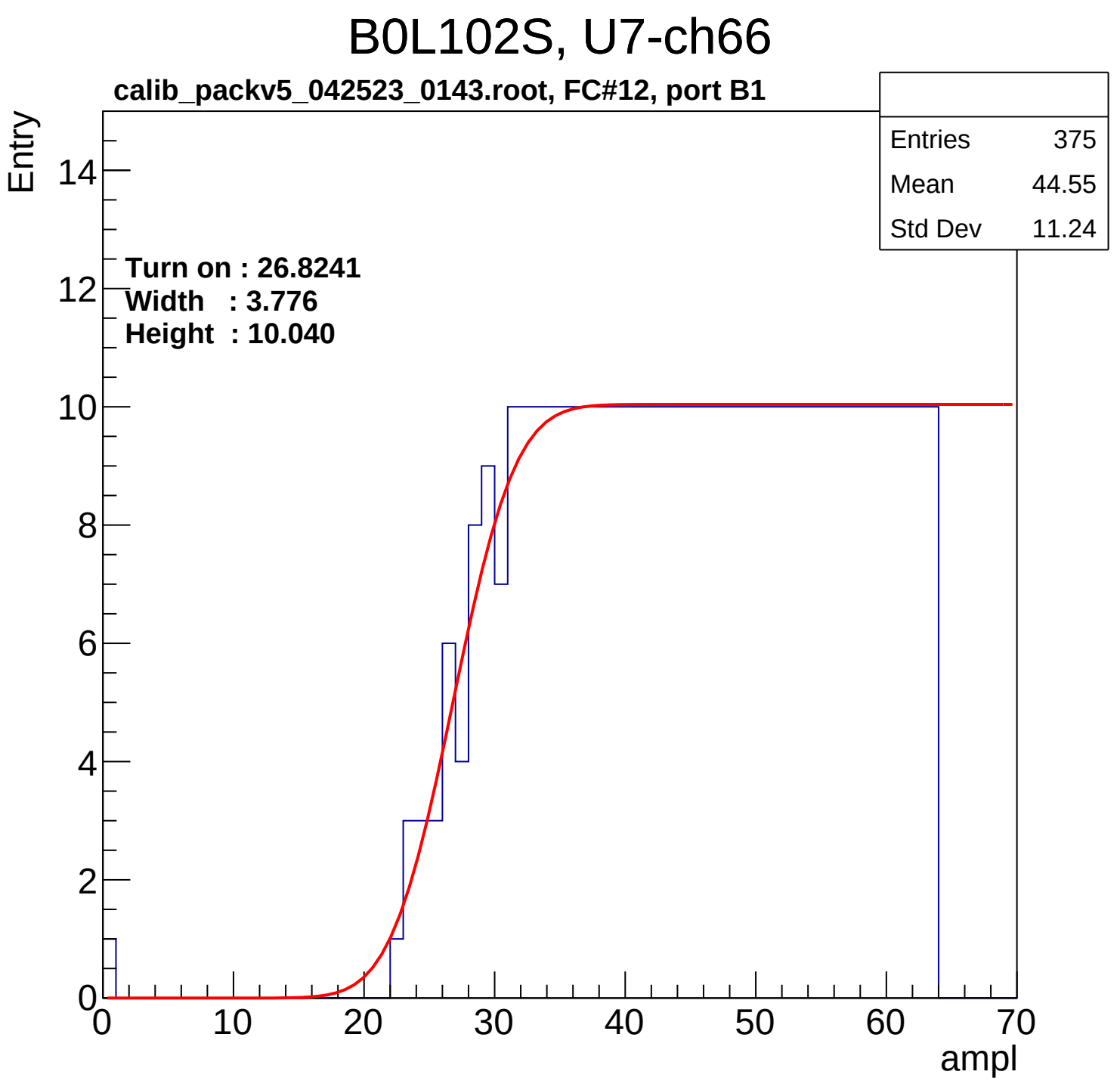
40
50
60
70


B0L102S, U7-ch66
calib_packv5_042523_0143.root, FC#12, port B1
Entries 375
Mean 44.55
Std Dev 11.24
Turn on : 26.8241
Width : 3.776
Height : 10.040
Entry
ampl
0
2
4
6
8
10
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0
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60
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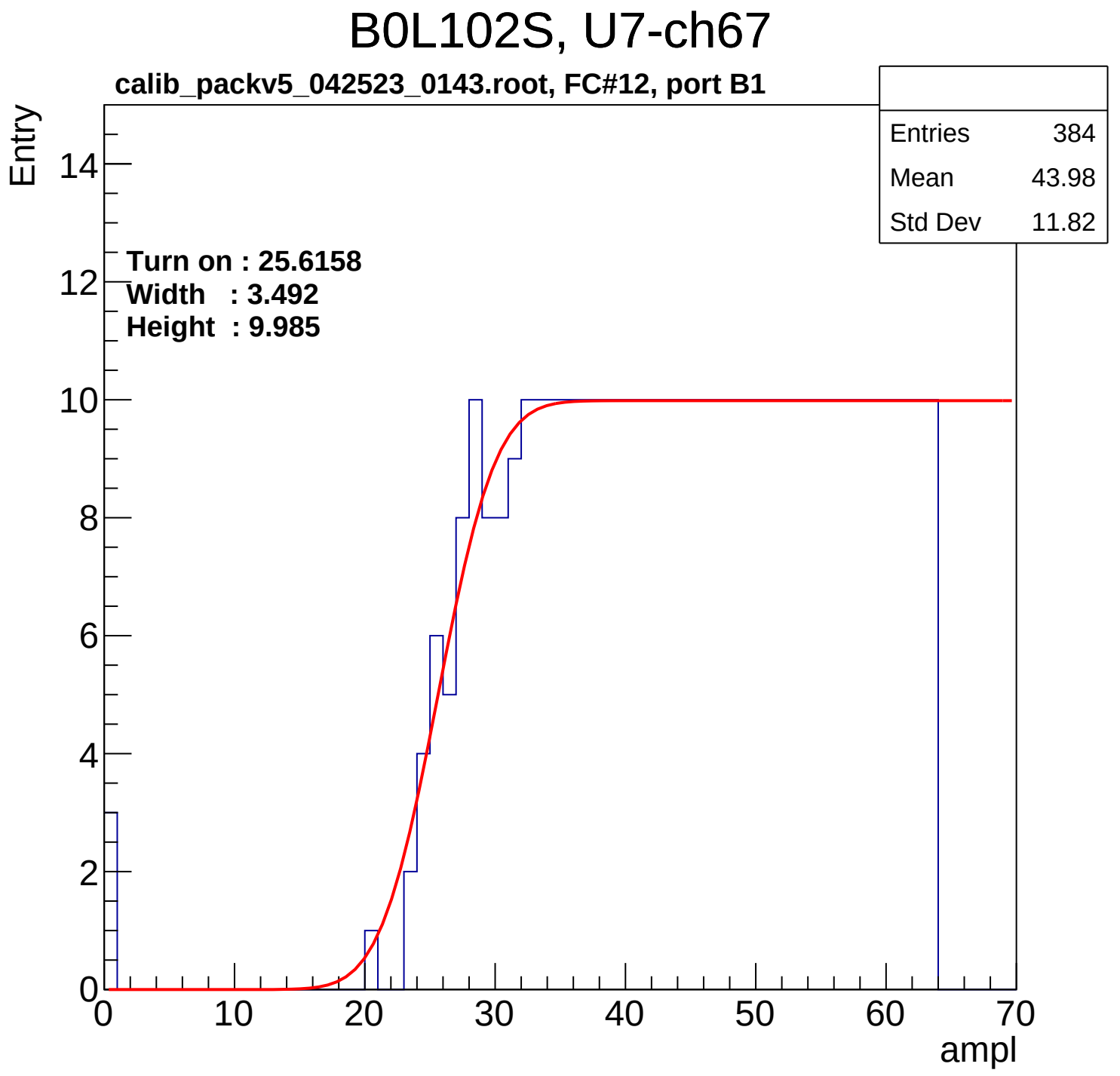
B0L102S, U7-ch67
calib_packv5_042523_0143.root, FC#12, port B1
Entries 384
Mean 43.98
Std Dev 11.82
Turn on : 25.6158
Width : 3.492
Height : 9.985
Entry
ampl
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2
4
6
8
10
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0
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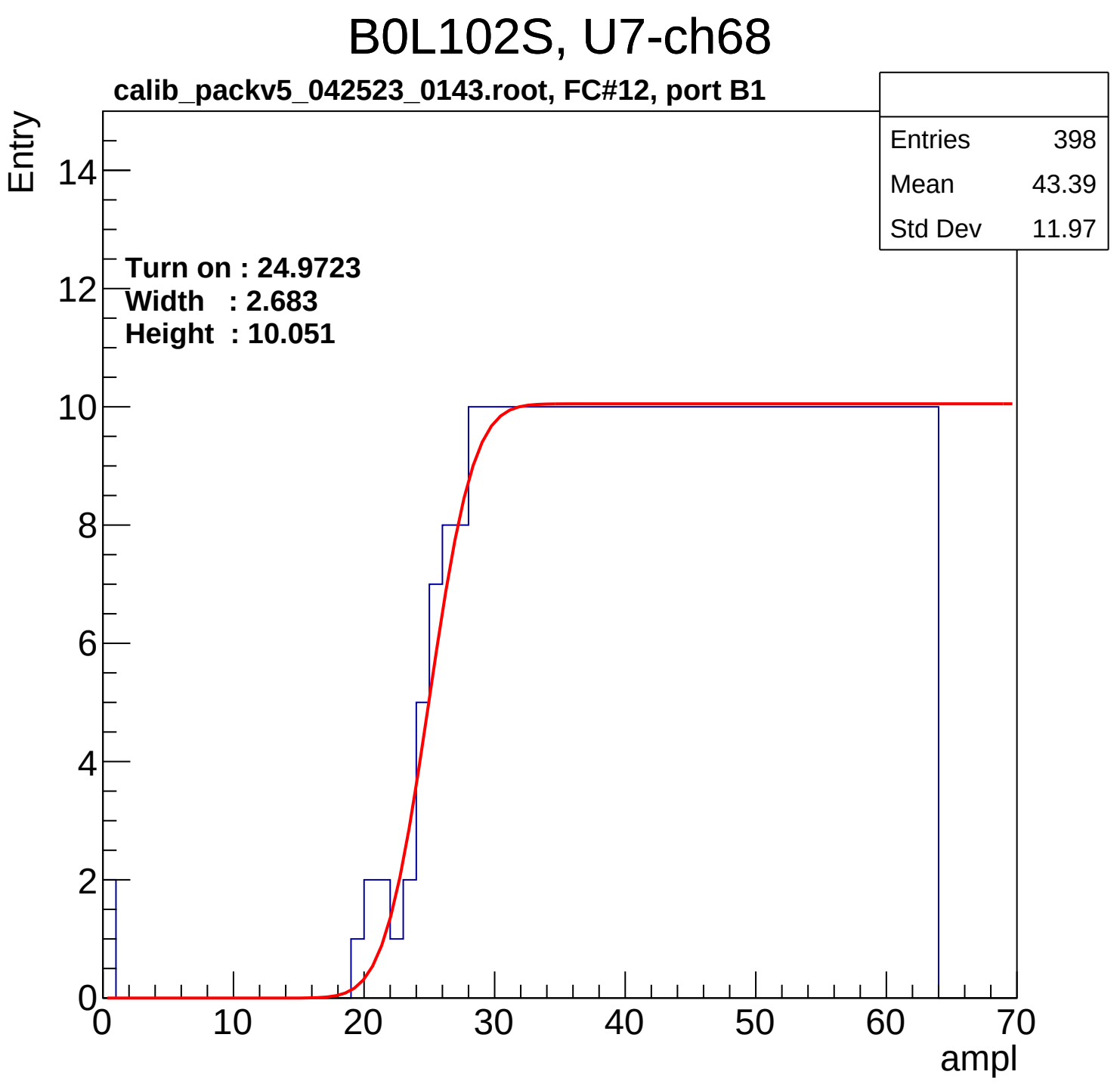
B0L102S, U7-ch68
calib_packv5_042523_0143.root, FC#12, port B1
Entries 398
Mean 43.39
Std Dev 11.97
Turn on : 24.9723
Width : 2.683
Height : 10.051
Entry
ampl
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2
4
6
8
10
12
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60
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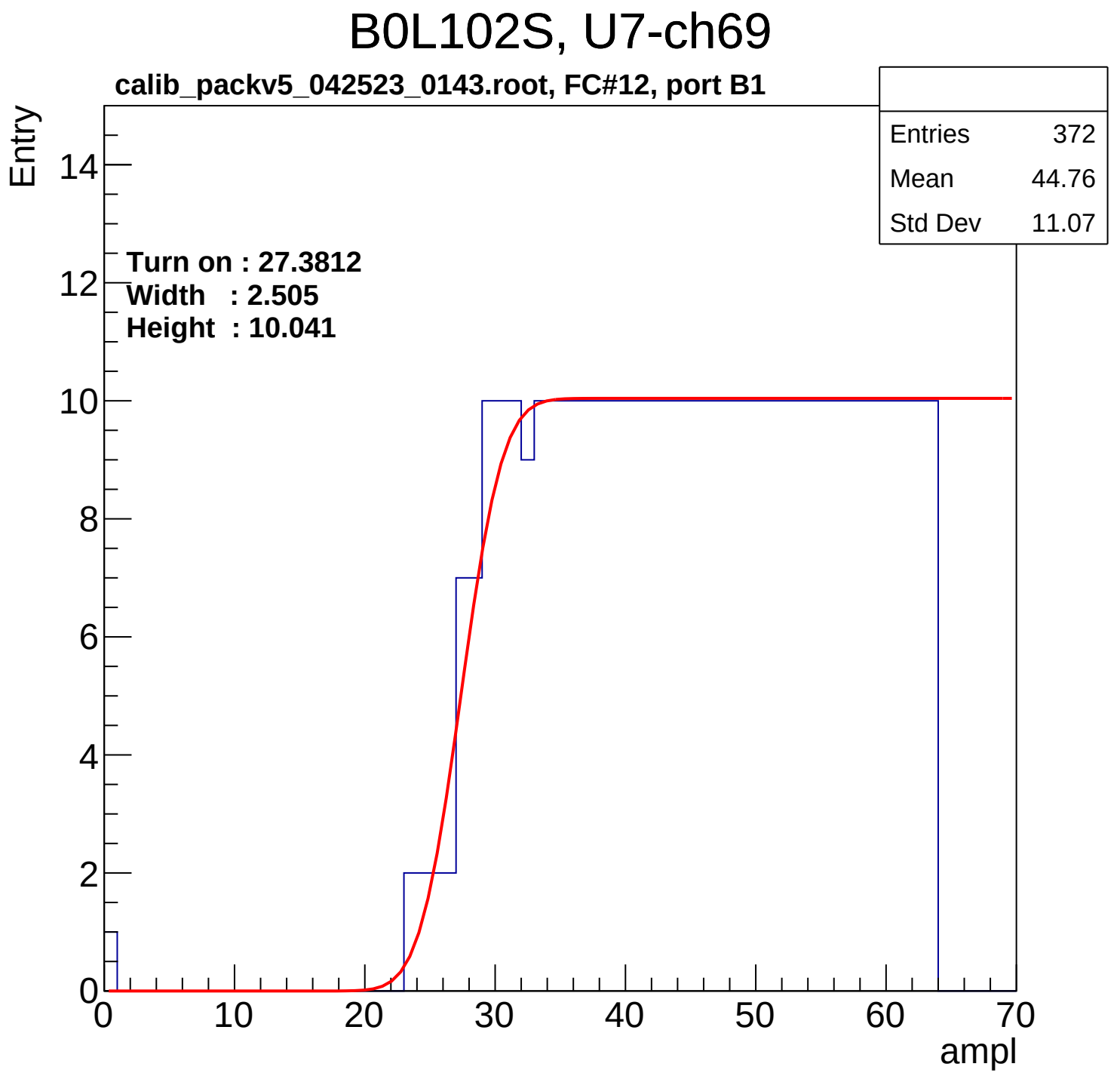
B0L102S, U7-ch69
calib_packv5_042523_0143.root, FC#12, port B1
Entries 372
Mean 44.76
Std Dev 11.07
Turn on : 27.3812
Width : 2.505
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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60
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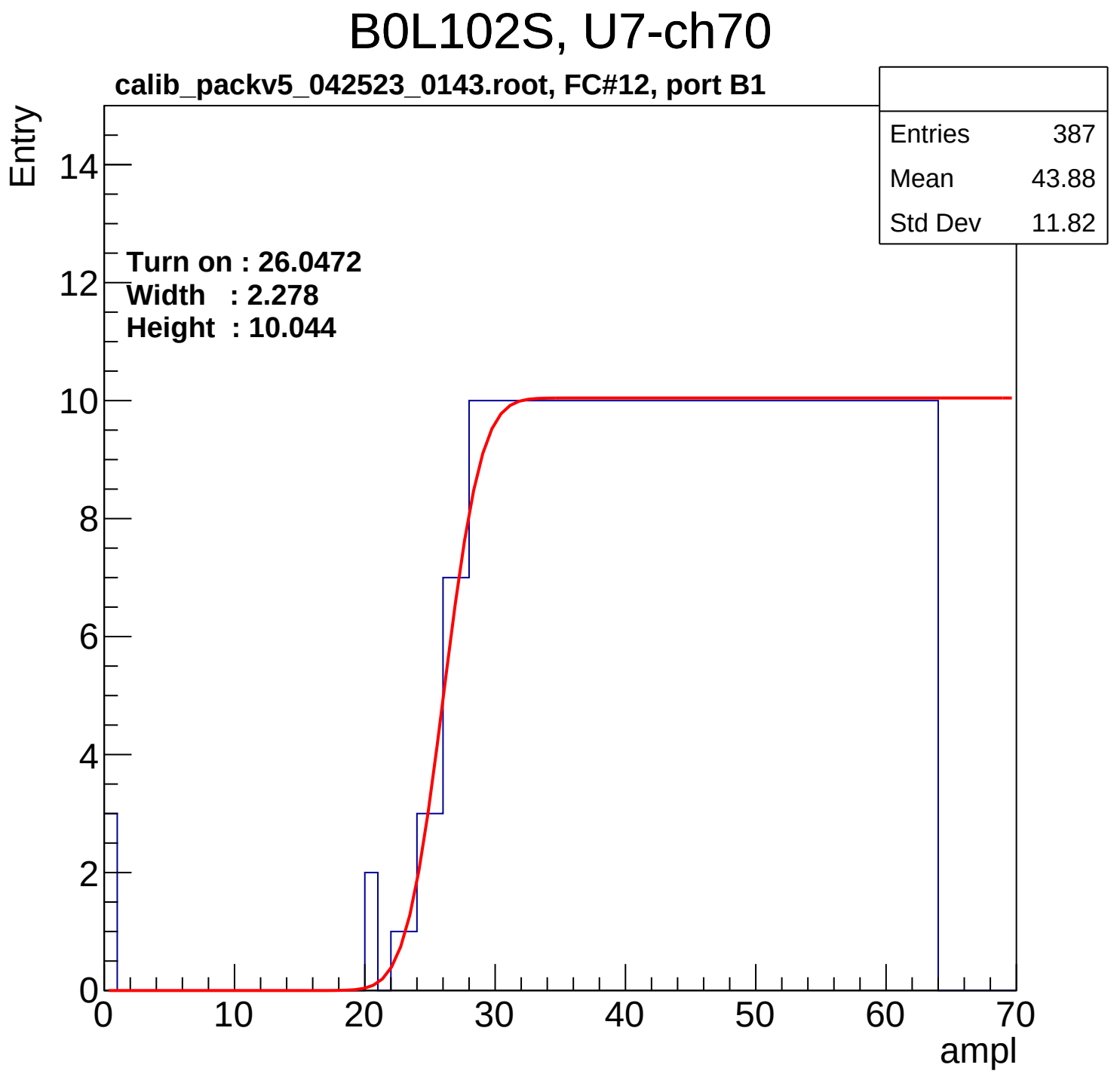
B0L102S, U7-ch70
calib_packv5_042523_0143.root, FC#12, port B1
Entries 387
Mean 43.88
Std Dev 11.82
Turn on : 26.0472
Width : 2.278
Height : 10.044
Entry
ampl
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2
4
6
8
10
12
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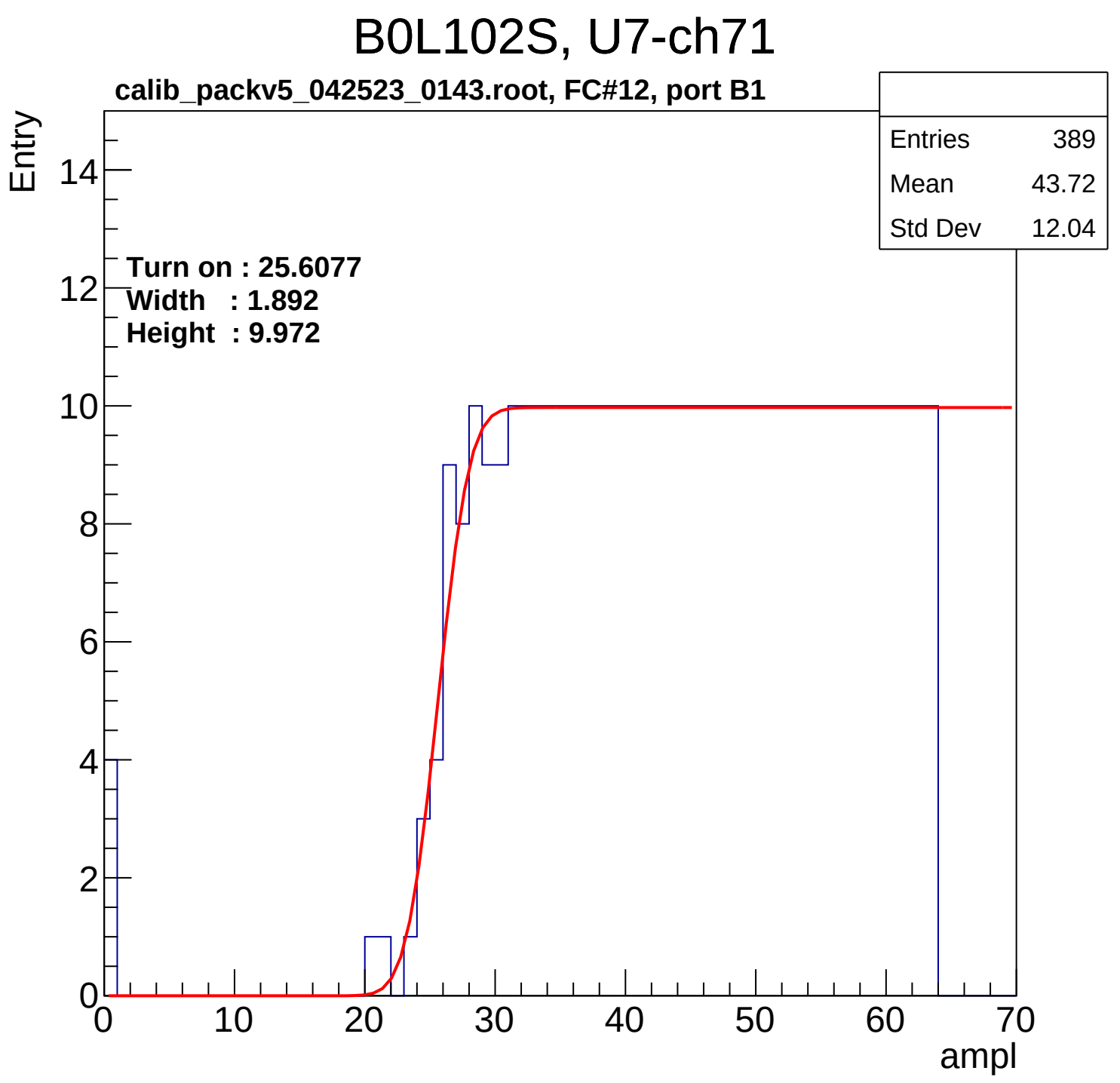
B0L102S, U7-ch71
calib_packv5_042523_0143.root, FC#12, port B1
Entries 389
Mean 43.72
Std Dev 12.04
Turn on : 25.6077
Width : 1.892
Height : 9.972
Entry
ampl
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2
4
6
8
10
12
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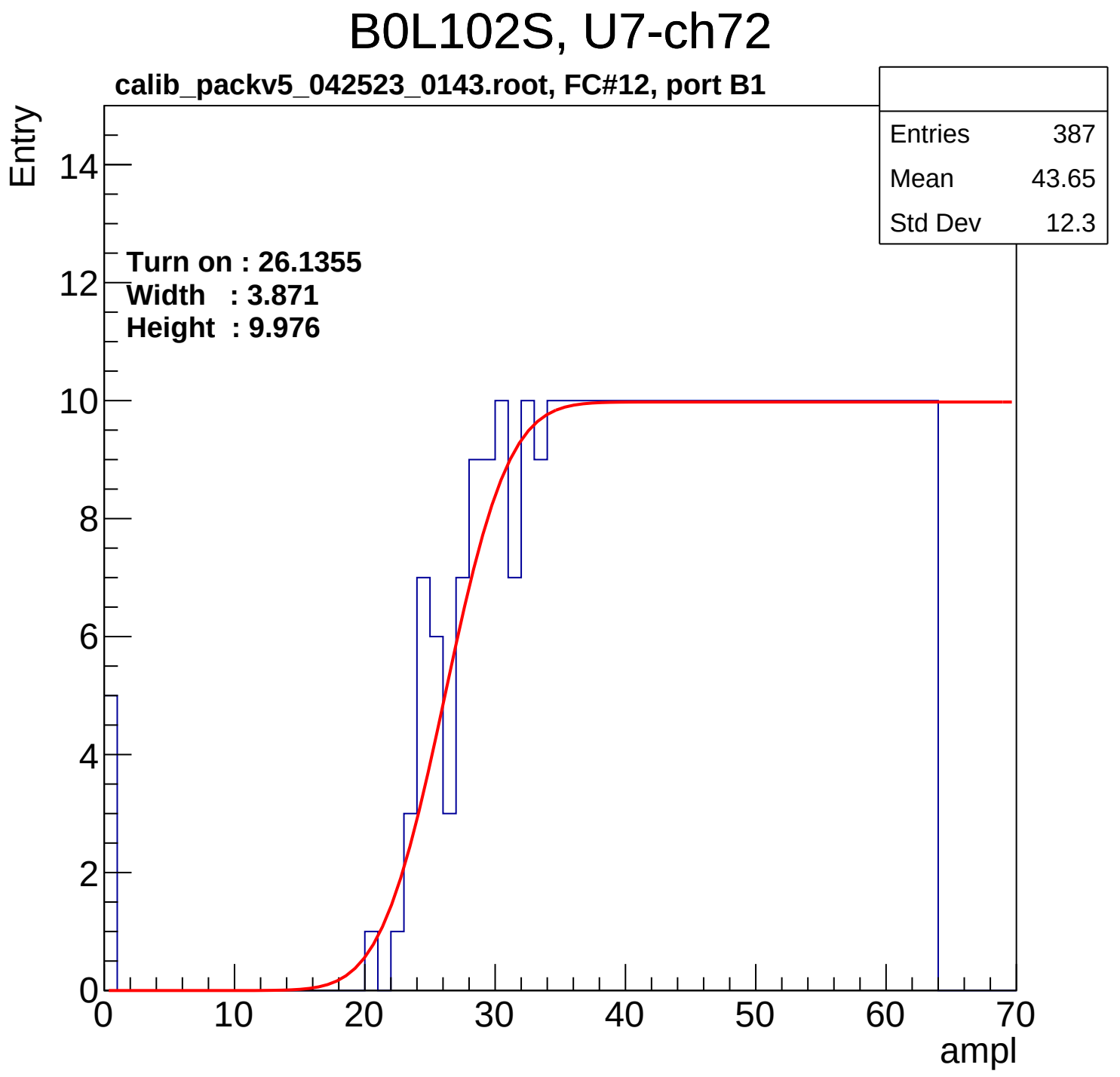
B0L102S, U7-ch72
calib_packv5_042523_0143.root, FC#12, port B1
Entries 387
Mean 43.65
Std Dev 12.3
Turn on : 26.1355
Width : 3.871
Height : 9.976
Entry
ampl
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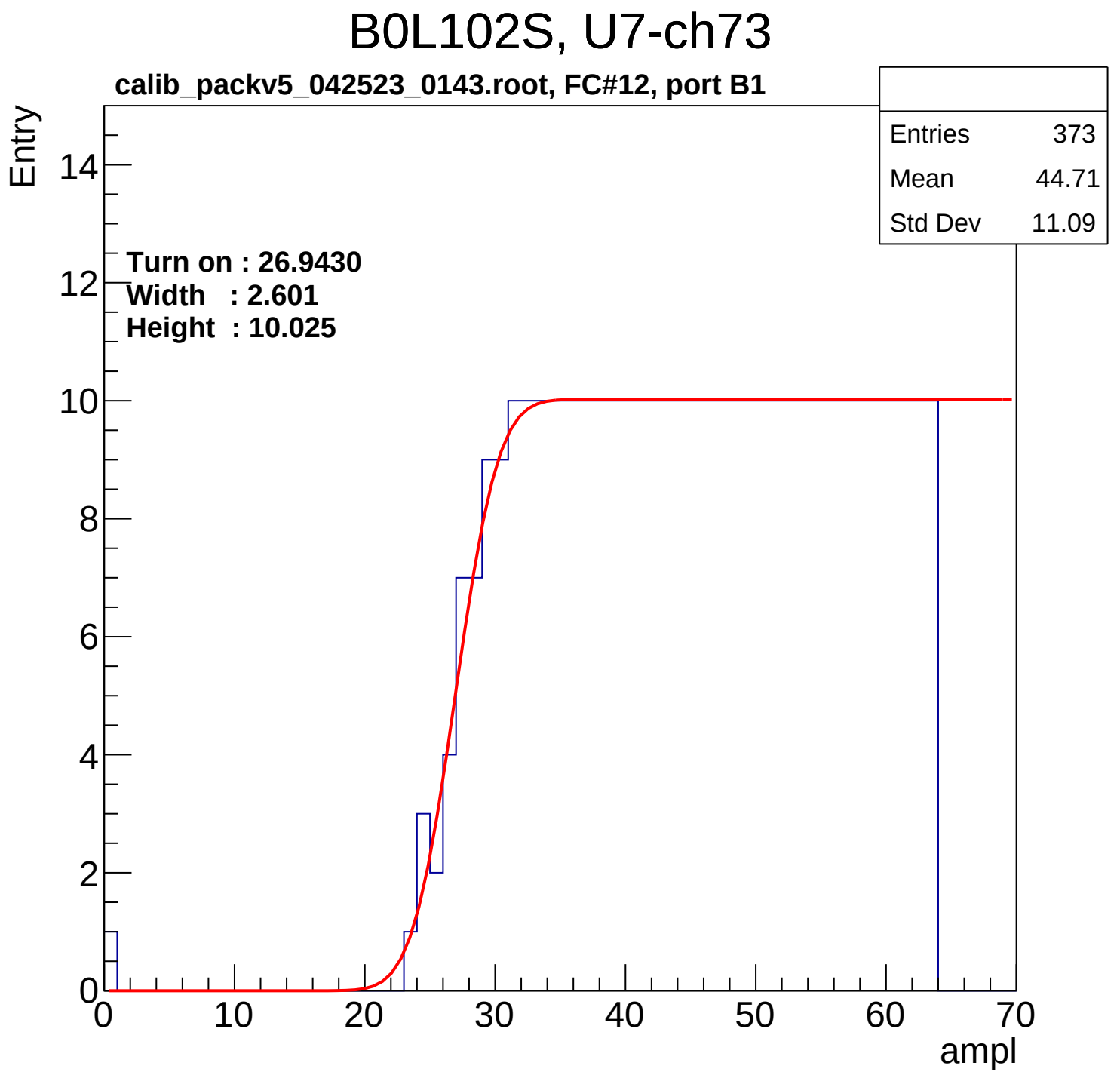
B0L102S, U7-ch73
calib_packv5_042523_0143.root, FC#12, port B1
Entries 373
Mean 44.71
Std Dev 11.09
Turn on : 26.9430
Width : 2.601
Height : 10.025
Entry
ampl
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6
8
10
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0
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60
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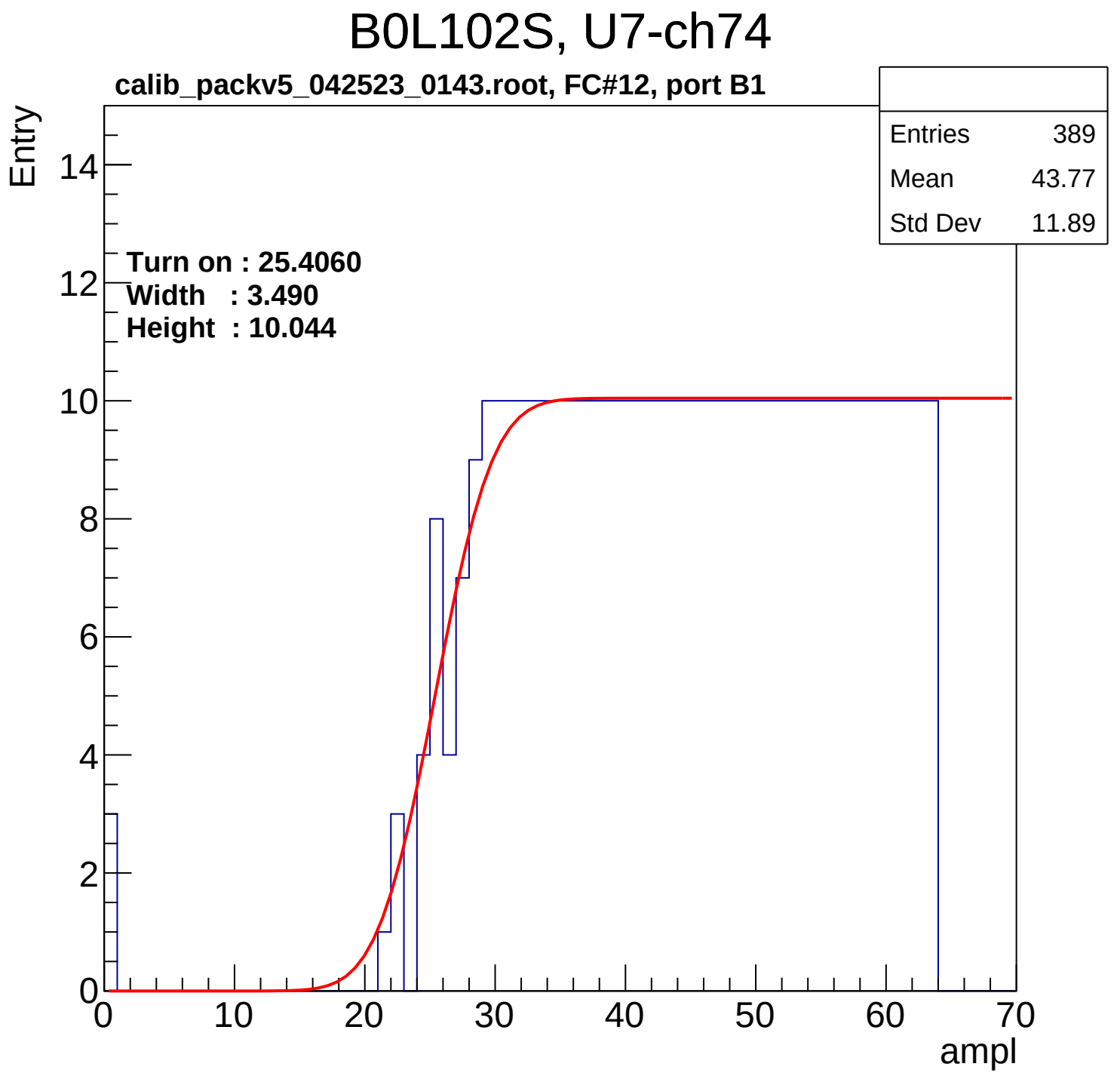
B0L102S, U7-ch74
calib_packv5_042523_0143.root, FC#12, port B1
Entries 389
Mean 43.77
Std Dev 11.89
Turn on : 25.4060
Width : 3.490
Height : 10.044
Entry
ampl
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8
10
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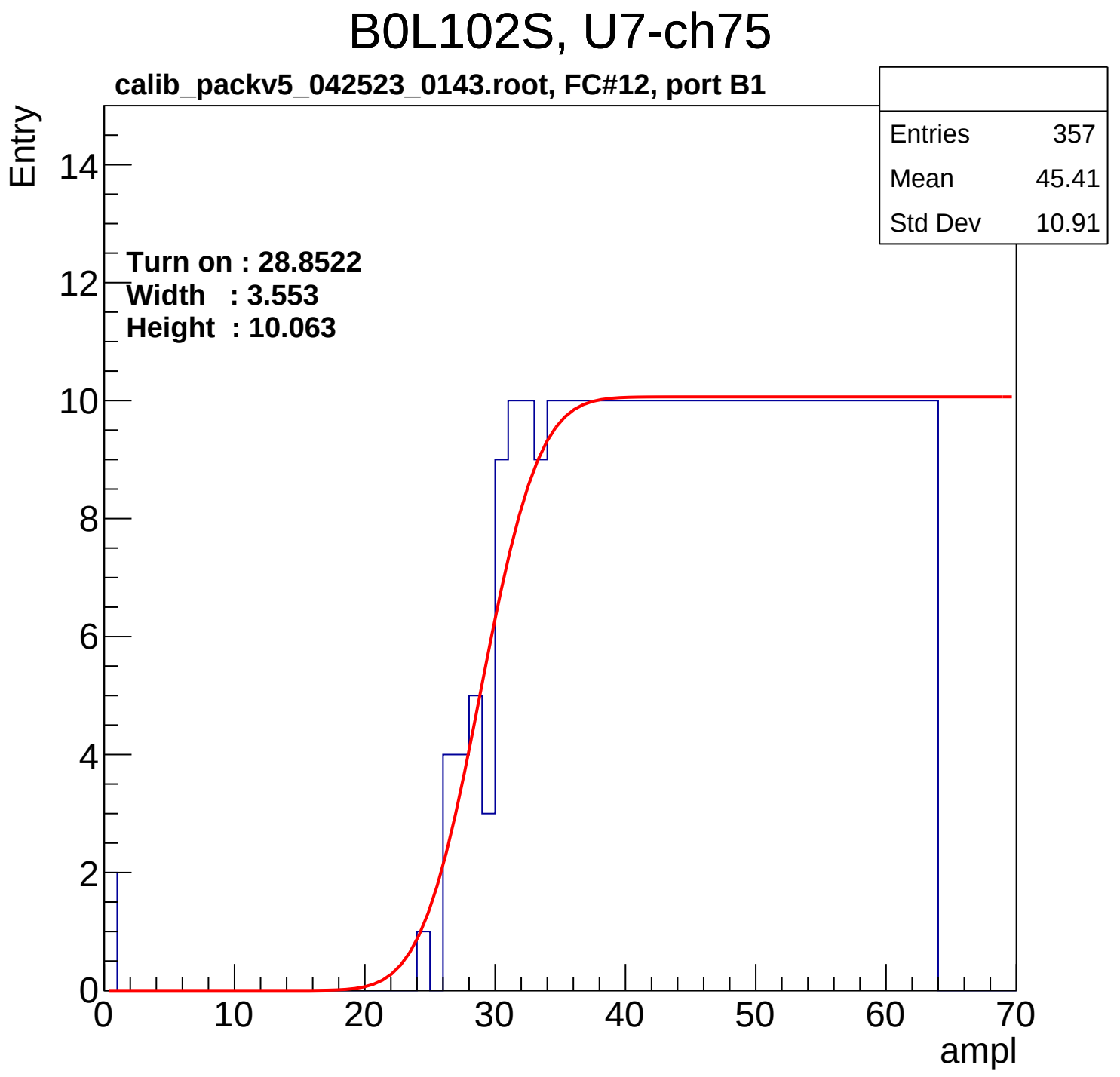
B0L102S, U7-ch75
calib_packv5_042523_0143.root, FC#12, port B1
Entries 357
Mean 45.41
Std Dev 10.91
Turn on : 28.8522
Width : 3.553
Height : 10.063
Entry
ampl
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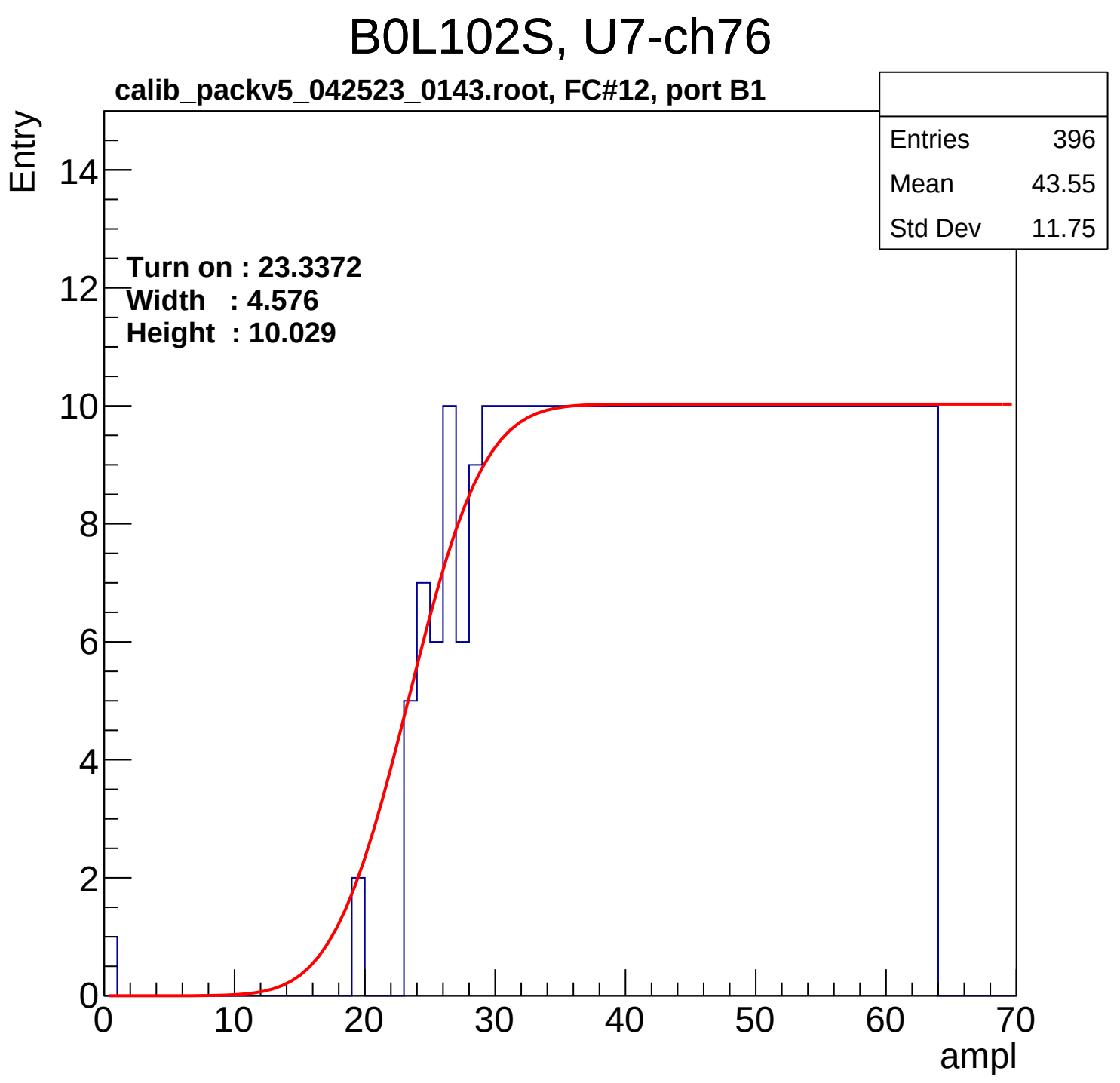
B0L102S, U7-ch76
calib_packv5_042523_0143.root, FC#12, port B1
Entries 396
Mean 43.55
Std Dev 11.75
Turn on : 23.3372
Width : 4.576
Height : 10.029
Entry
ampl
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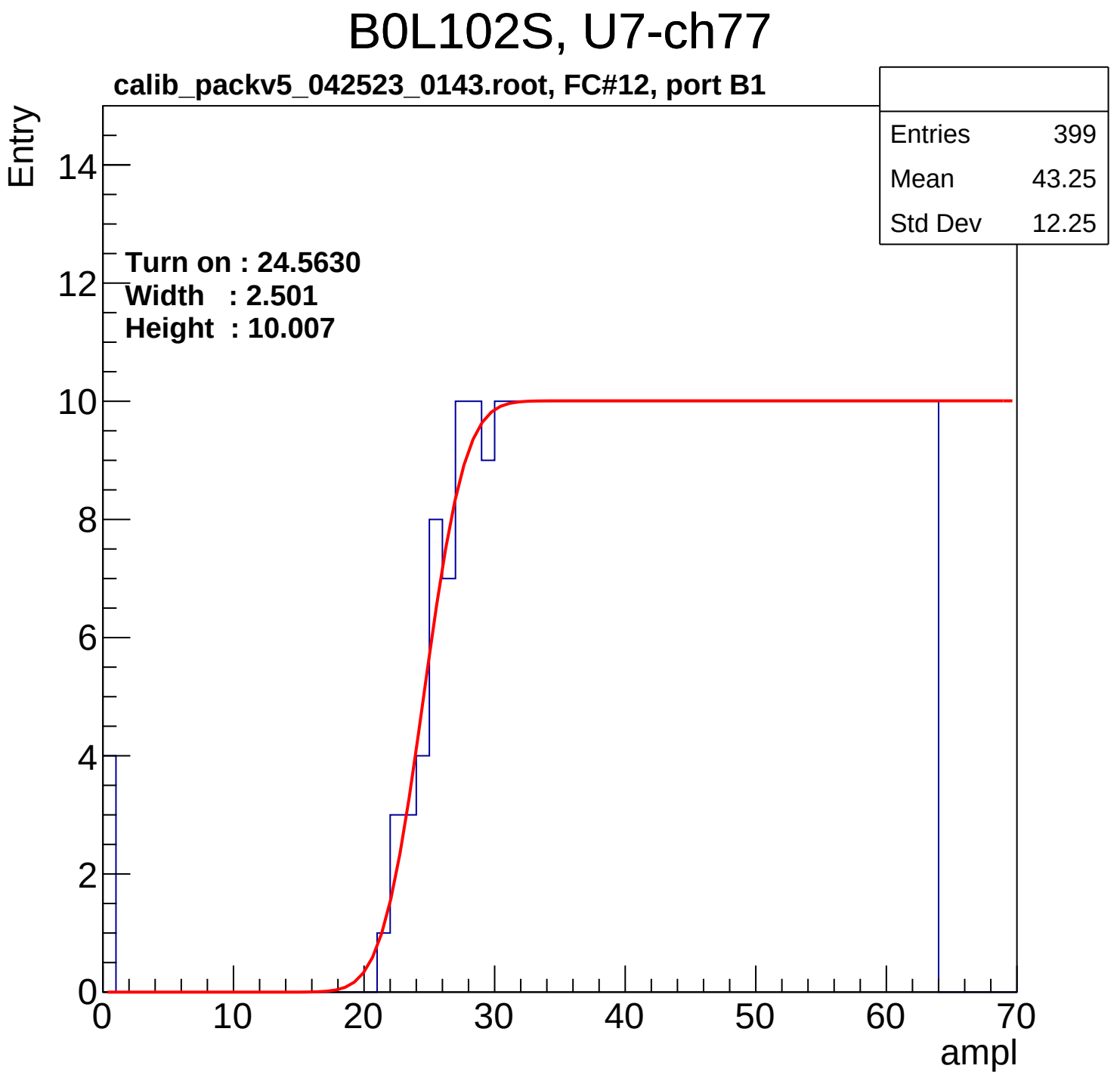
B0L102S, U7-ch77
calib_packv5_042523_0143.root, FC#12, port B1
Entries 399
Mean 43.25
Std Dev 12.25
Turn on : 24.5630
Width : 2.501
Height : 10.007
Entry
ampl
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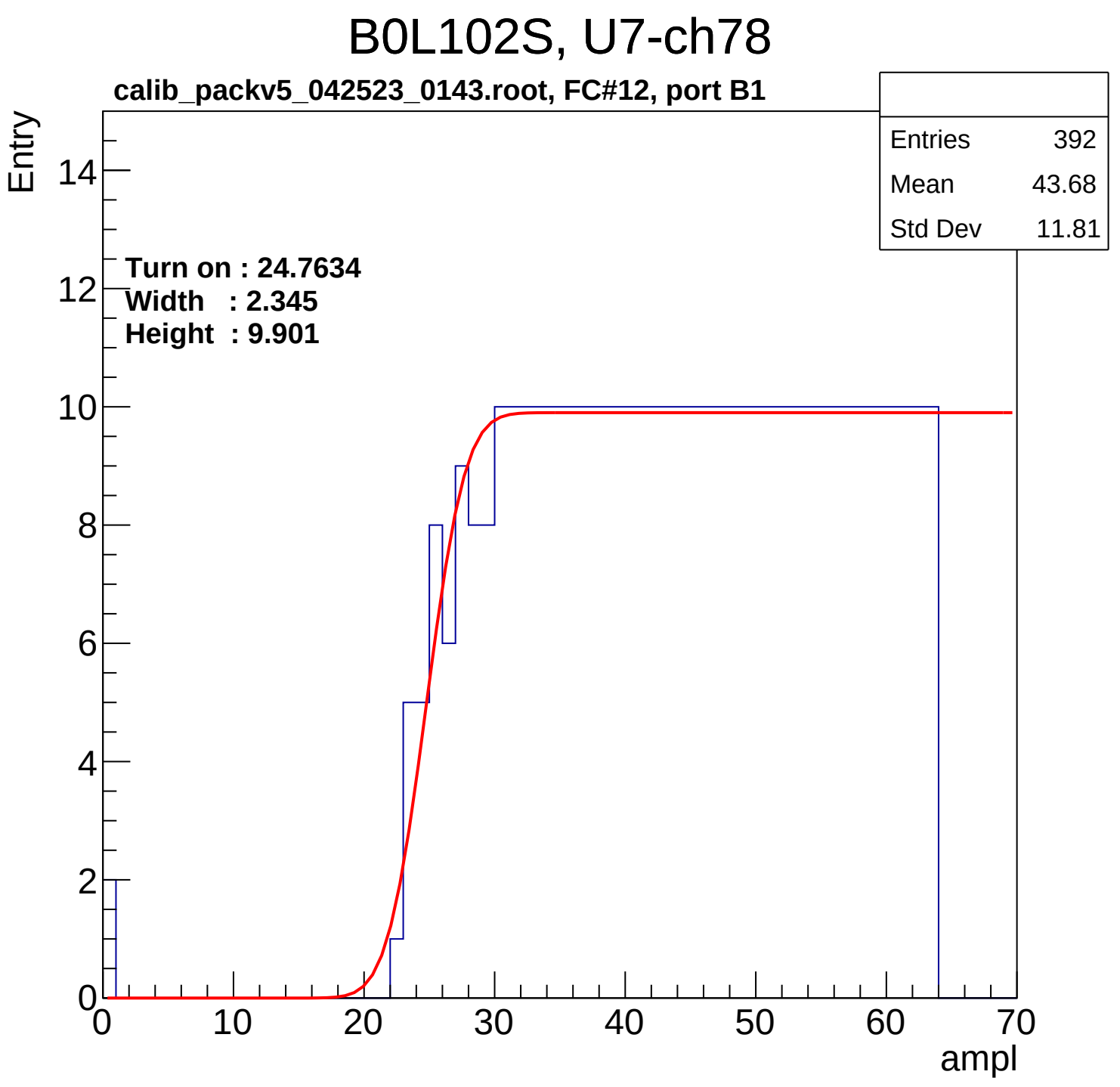
B0L102S, U7-ch78
calib_packv5_042523_0143.root, FC#12, port B1
Entries 392
Mean 43.68
Std Dev 11.81
Turn on : 24.7634
Width : 2.345
Height : 9.901
Entry
ampl
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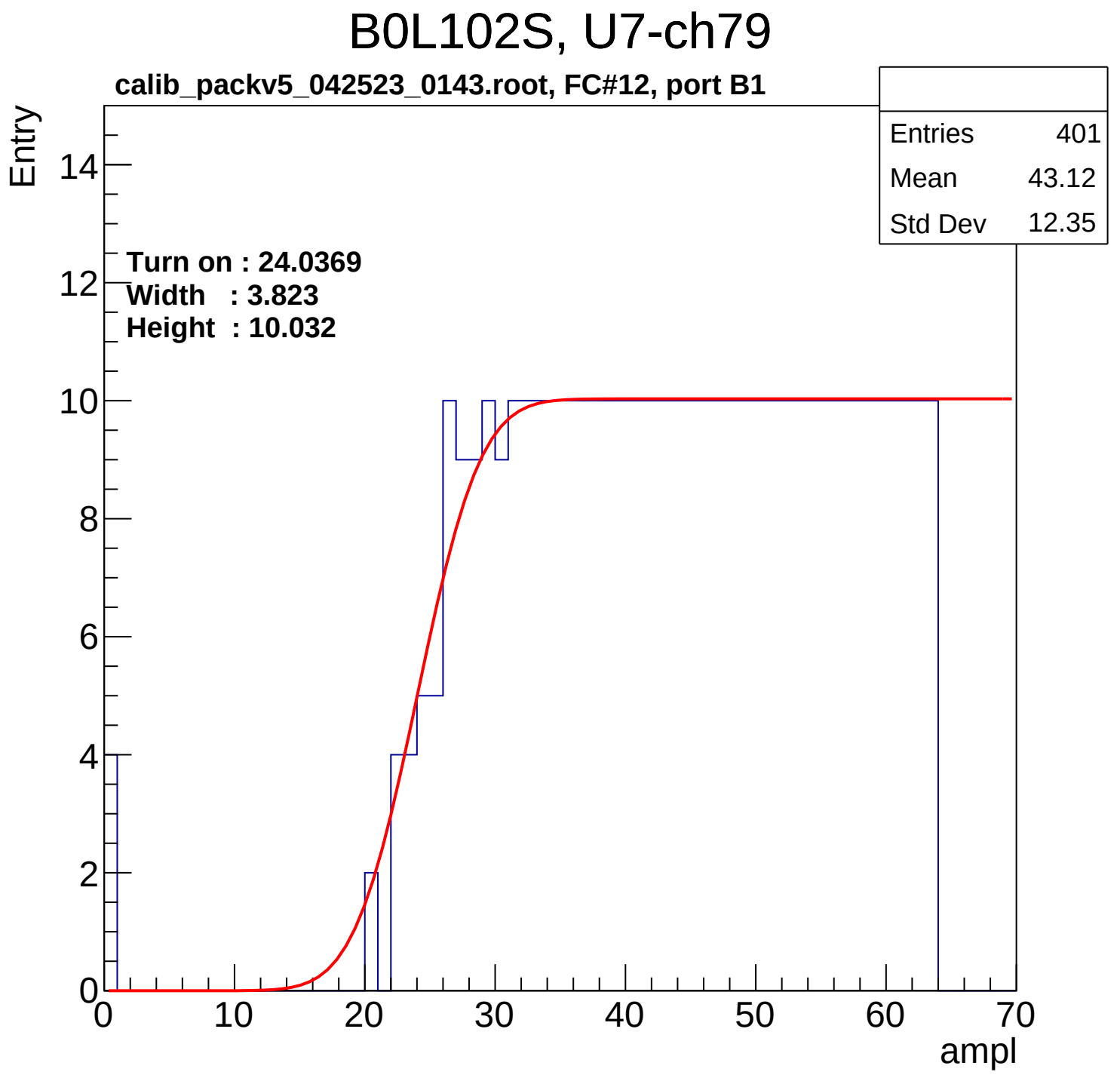
B0L102S, U7-ch79
calib_packv5_042523_0143.root, FC#12, port B1
Entries 401
Mean 43.12
Std Dev 12.35
Turn on : 24.0369
Width : 3.823
Height : 10.032
Entry
ampl
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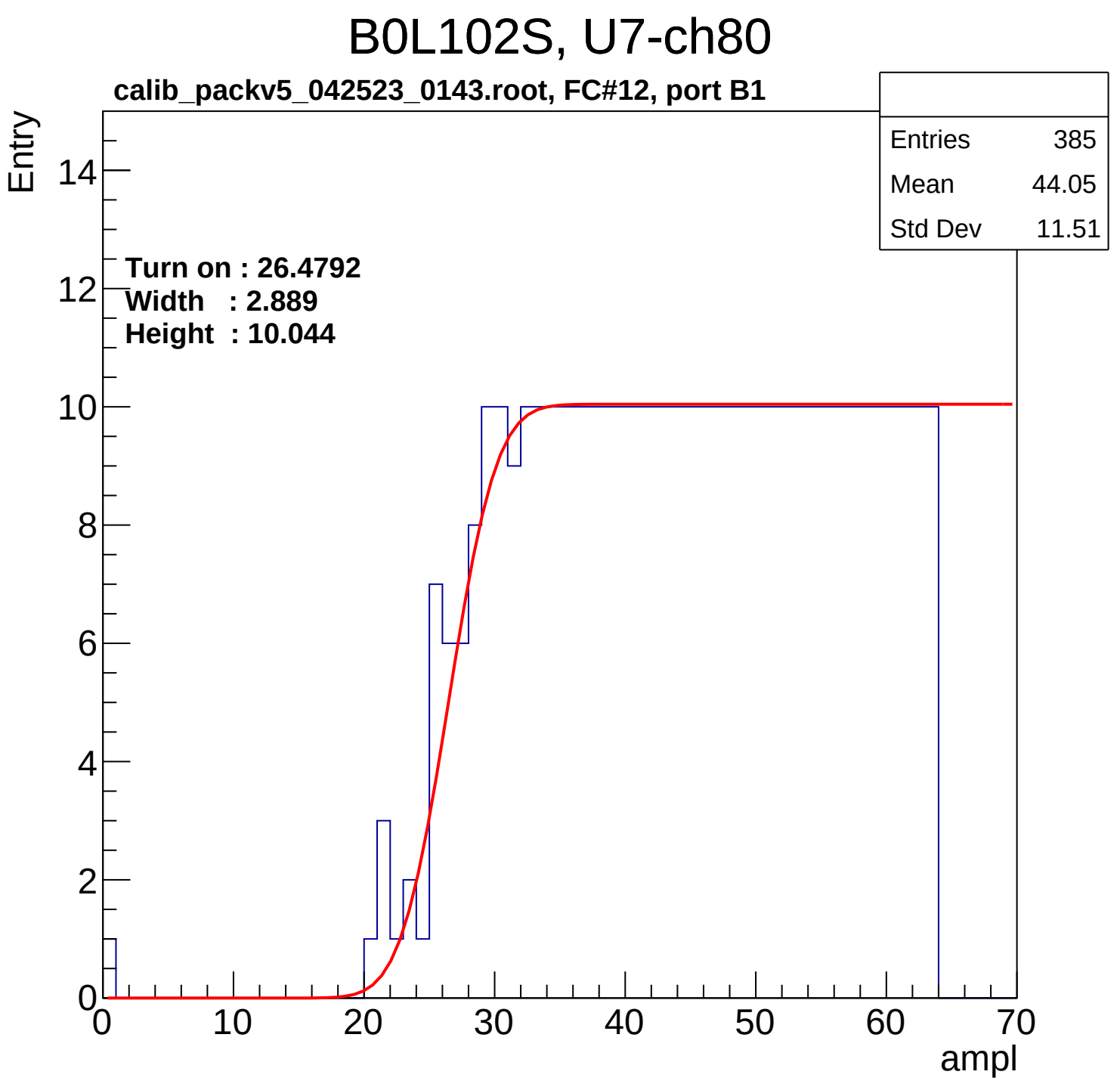
B0L102S, U7-ch80
calib_packv5_042523_0143.root, FC#12, port B1
Entries 385
Mean 44.05
Std Dev 11.51
Turn on : 26.4792
Width : 2.889
Height : 10.044
Entry
ampl
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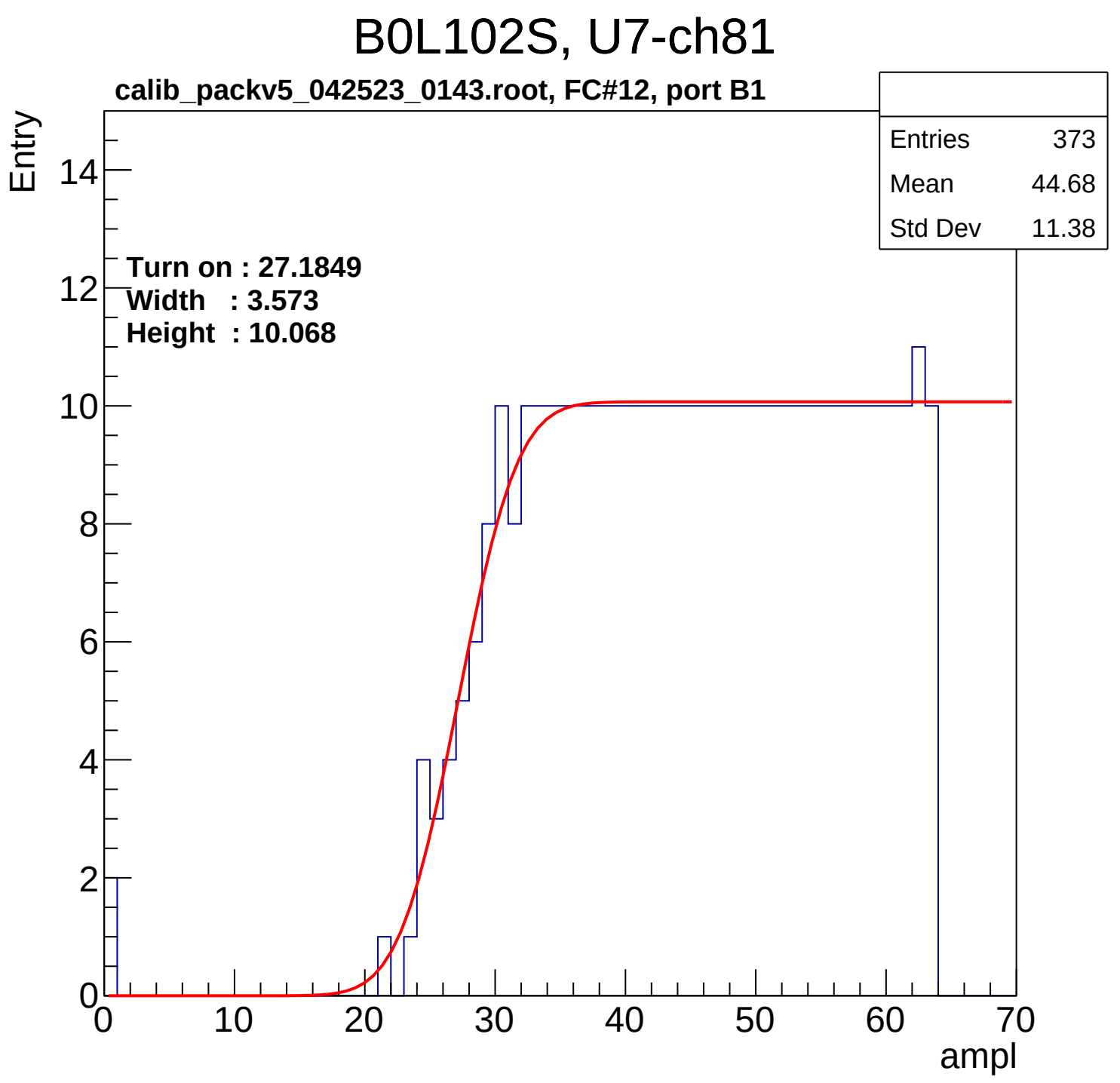
B0L102S, U7-ch81
calib_packv5_042523_0143.root, FC#12, port B1
Entries 373
Mean 44.68
Std Dev 11.38
Turn on : 27.1849
Width : 3.573
Height : 10.068
Entry
ampl
0
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4
6
8
10
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0
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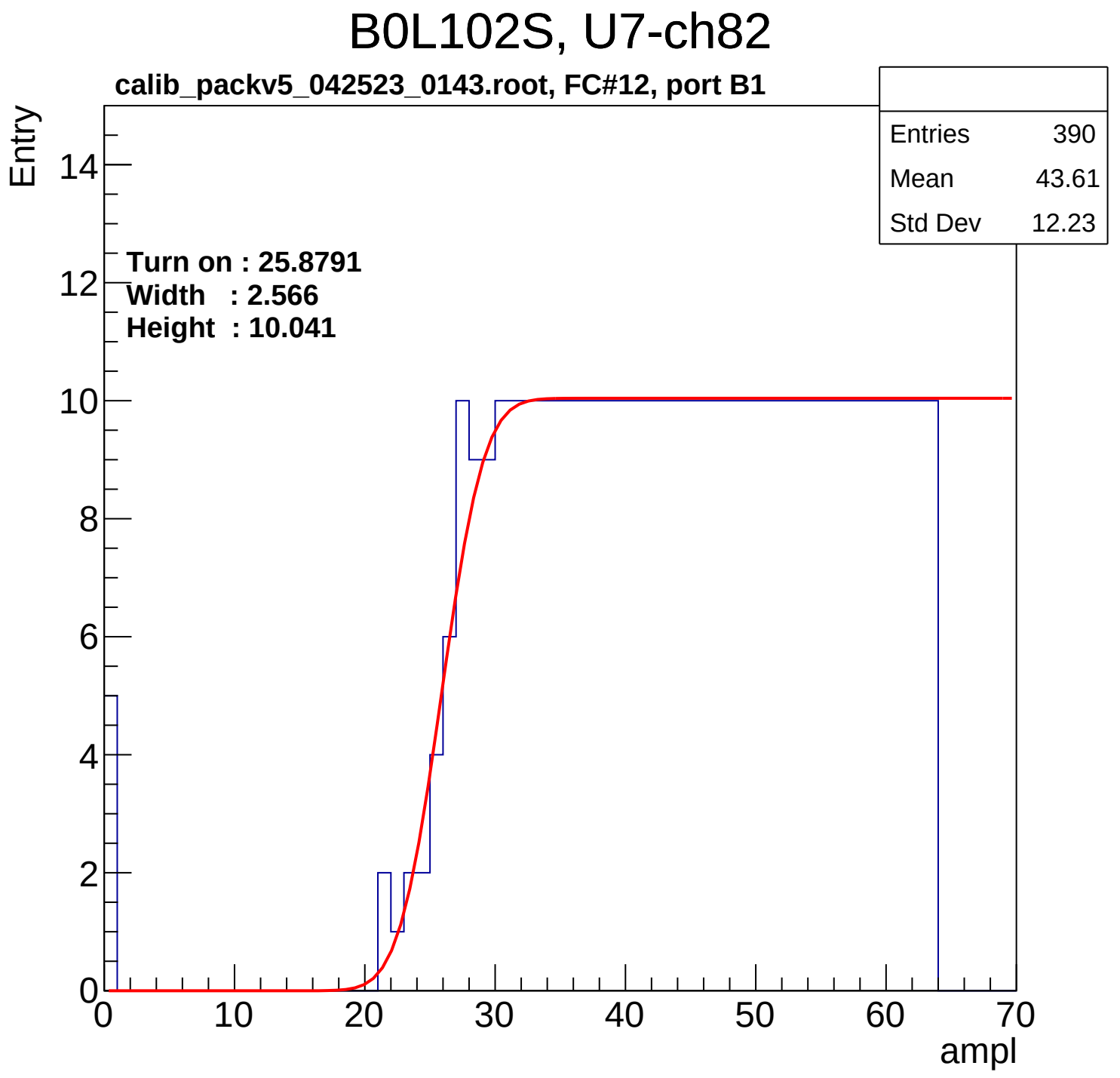
B0L102S, U7-ch82
calib_packv5_042523_0143.root, FC#12, port B1
Entries 390
Mean 43.61
Std Dev 12.23
Turn on : 25.8791
Width : 2.566
Height : 10.041
Entry
ampl
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8
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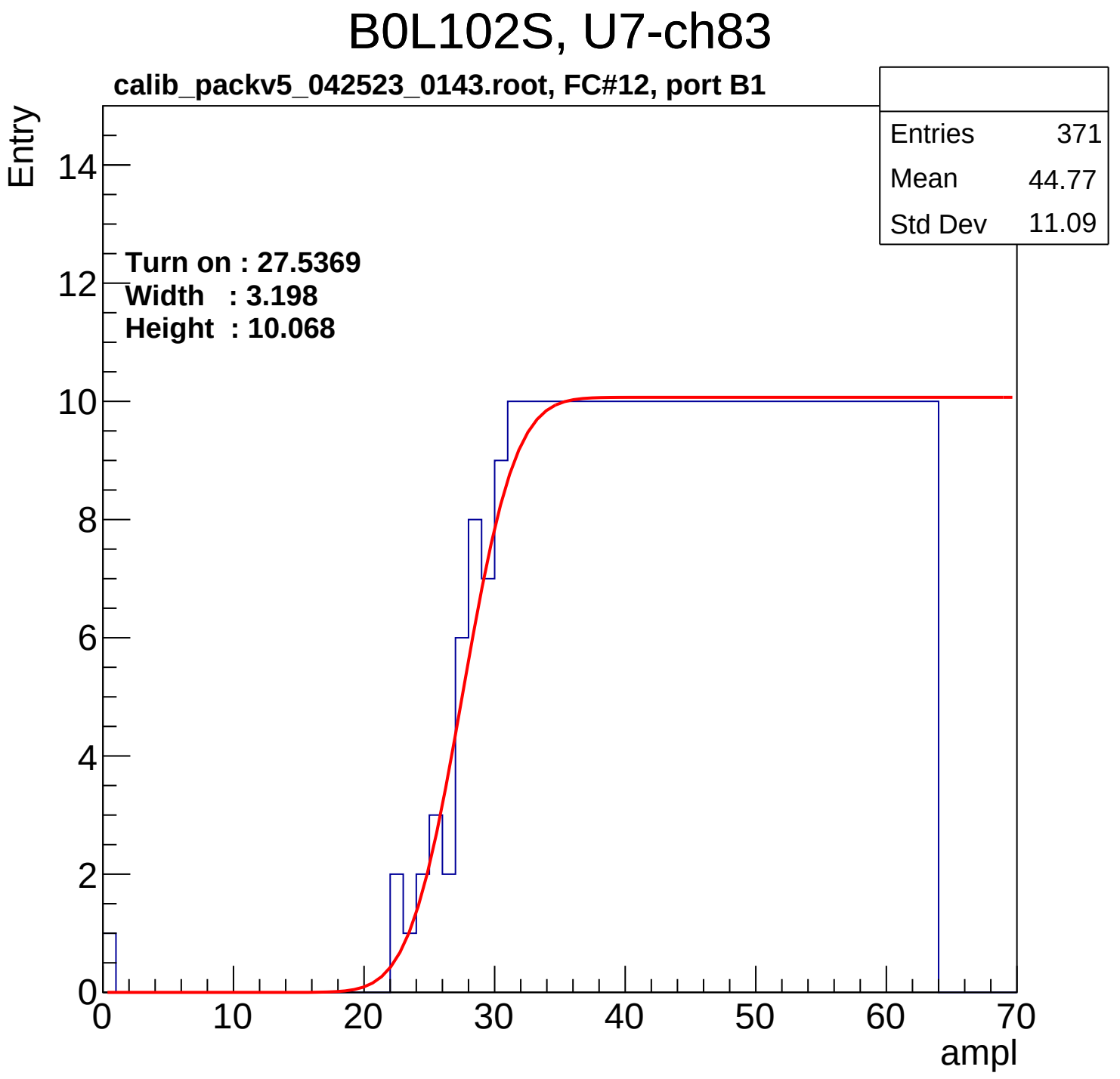
B0L102S, U7-ch83
calib_packv5_042523_0143.root, FC#12, port B1
Entries 371
Mean 44.77
Std Dev 11.09
Turn on : 27.5369
Width : 3.198
Height : 10.068
Entry
ampl
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6
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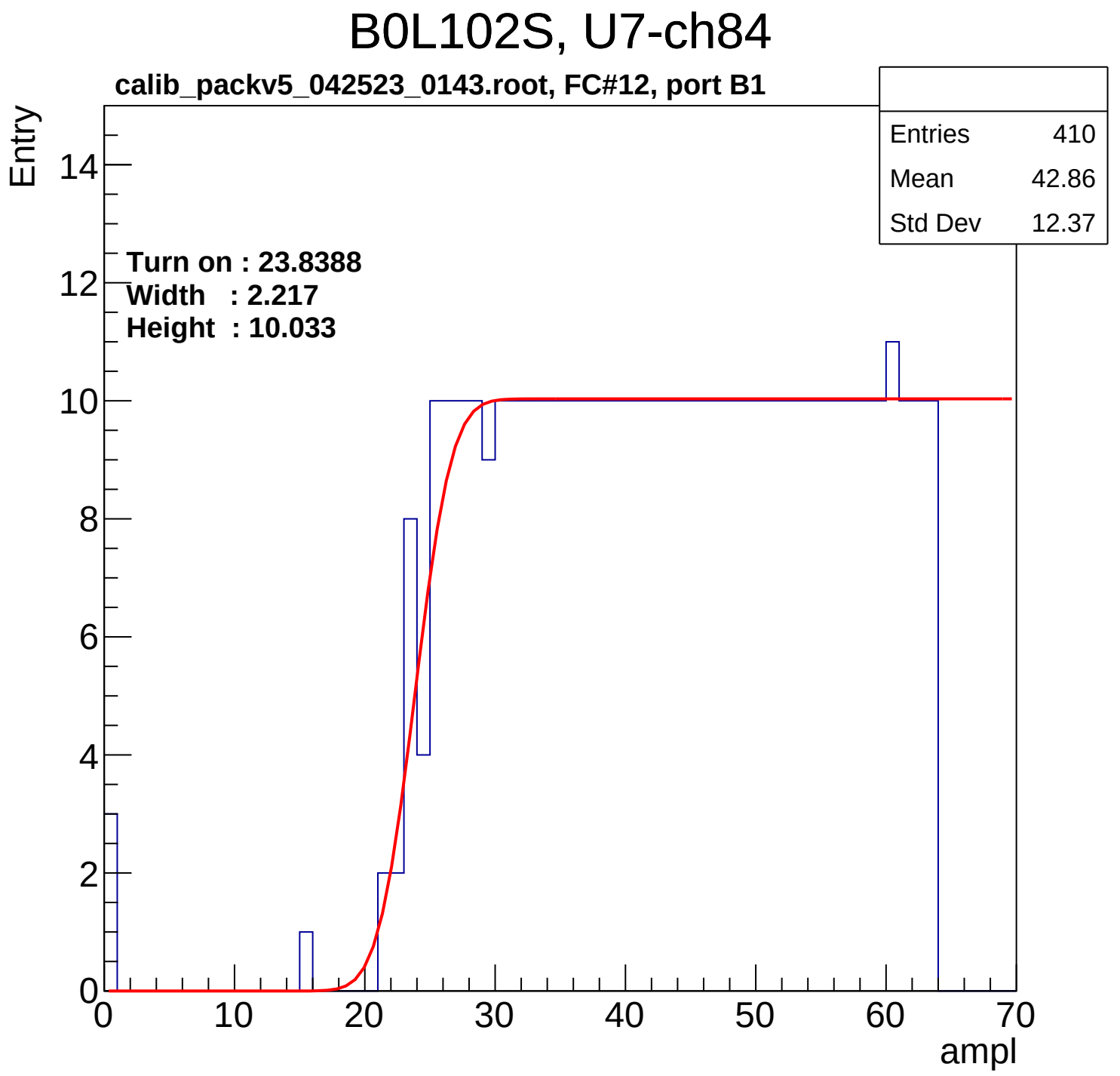
B0L102S, U7-ch84
calib_packv5_042523_0143.root, FC#12, port B1
Entries 410
Mean 42.86
Std Dev 12.37
Turn on : 23.8388
Width : 2.217
Height : 10.033
Entry
ampl
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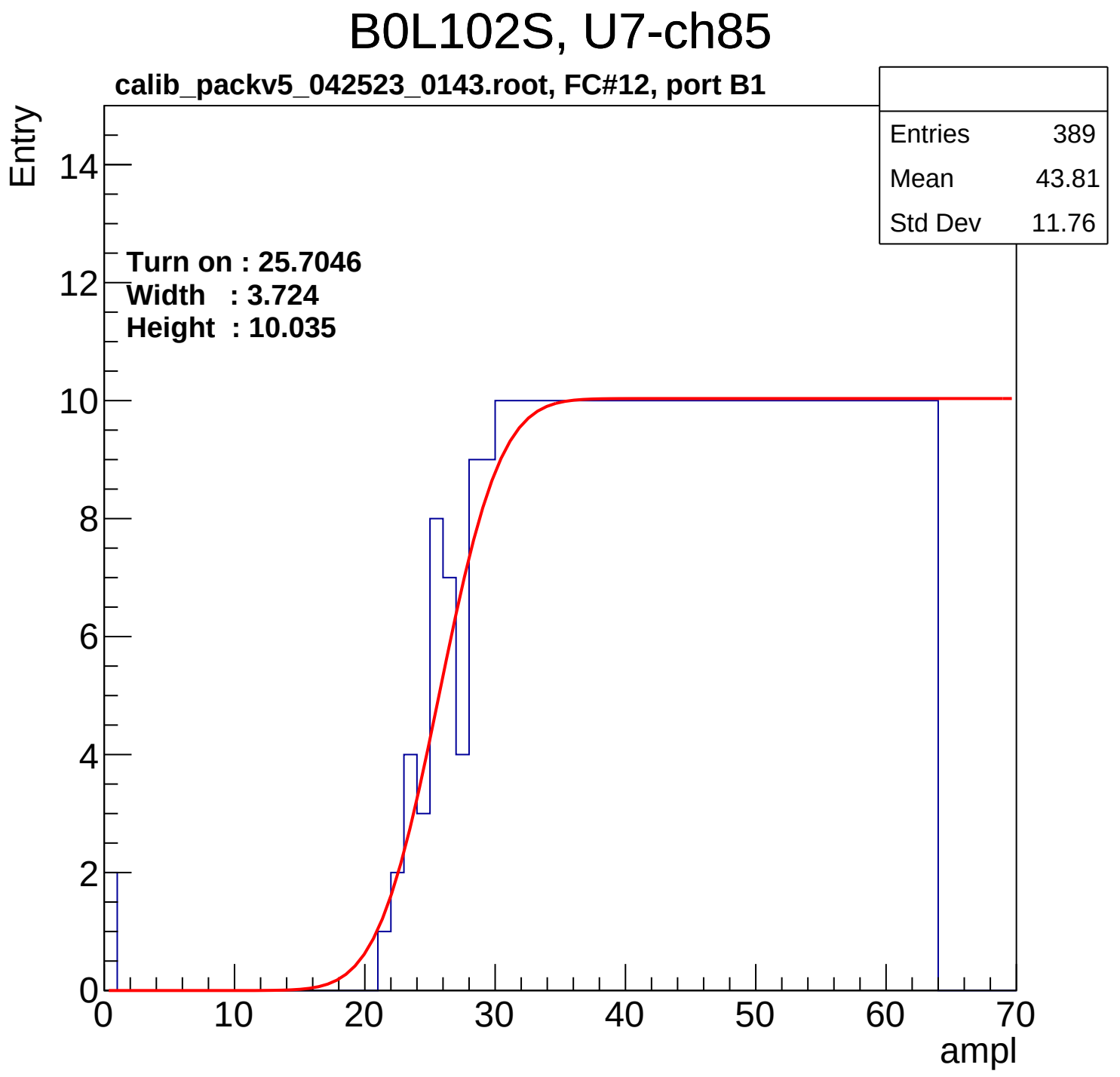
B0L102S, U7-ch85
calib_packv5_042523_0143.root, FC#12, port B1
Entries 389
Mean 43.81
Std Dev 11.76
Turn on : 25.7046
Width : 3.724
Height : 10.035
Entry
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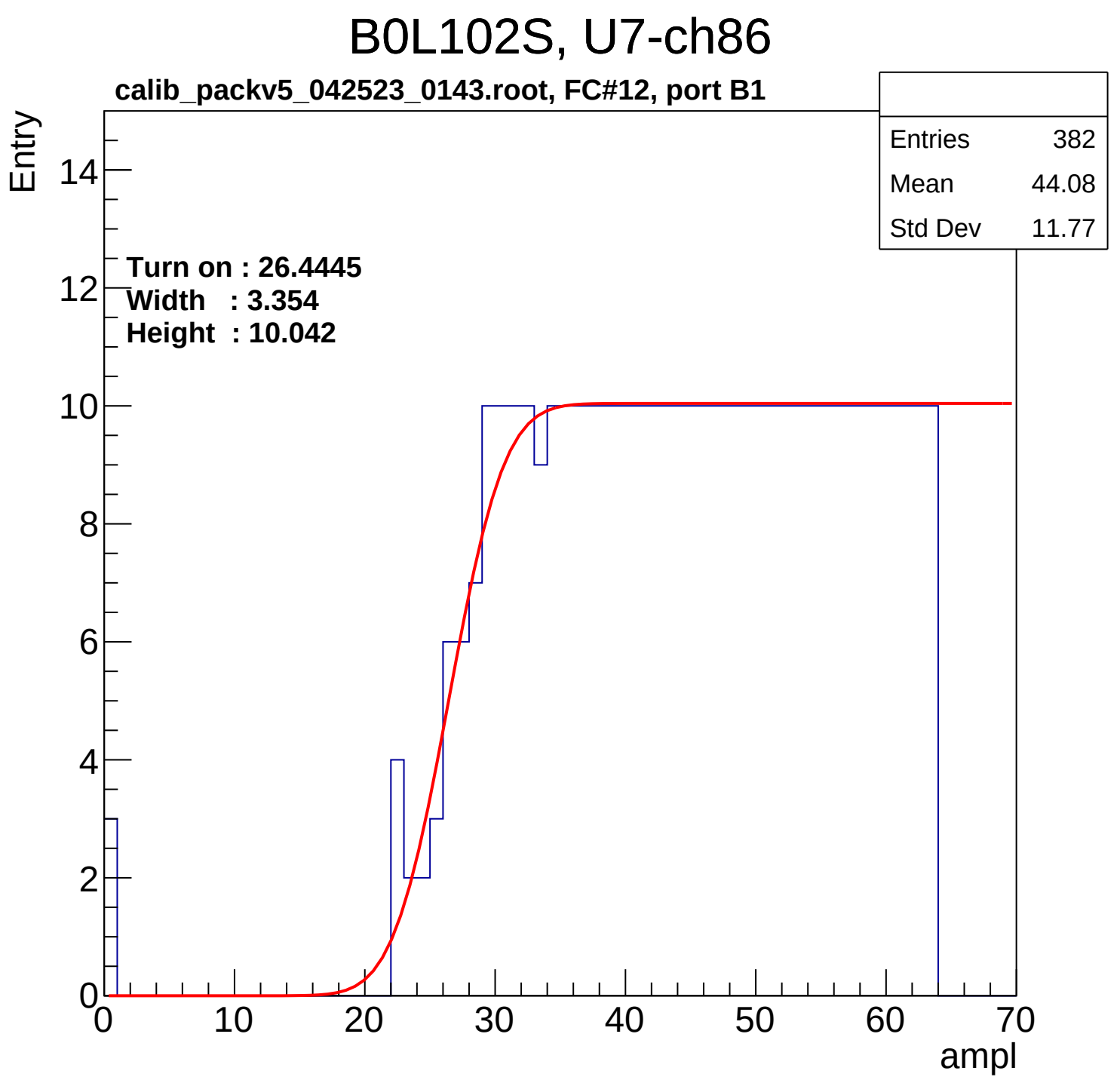
B0L102S, U7-ch86
calib_packv5_042523_0143.root, FC#12, port B1
Entries 382
Mean 44.08
Std Dev 11.77
Turn on : 26.4445
Width : 3.354
Height : 10.042
Entry
ampl
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4
6
8
10
12
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10
20
30
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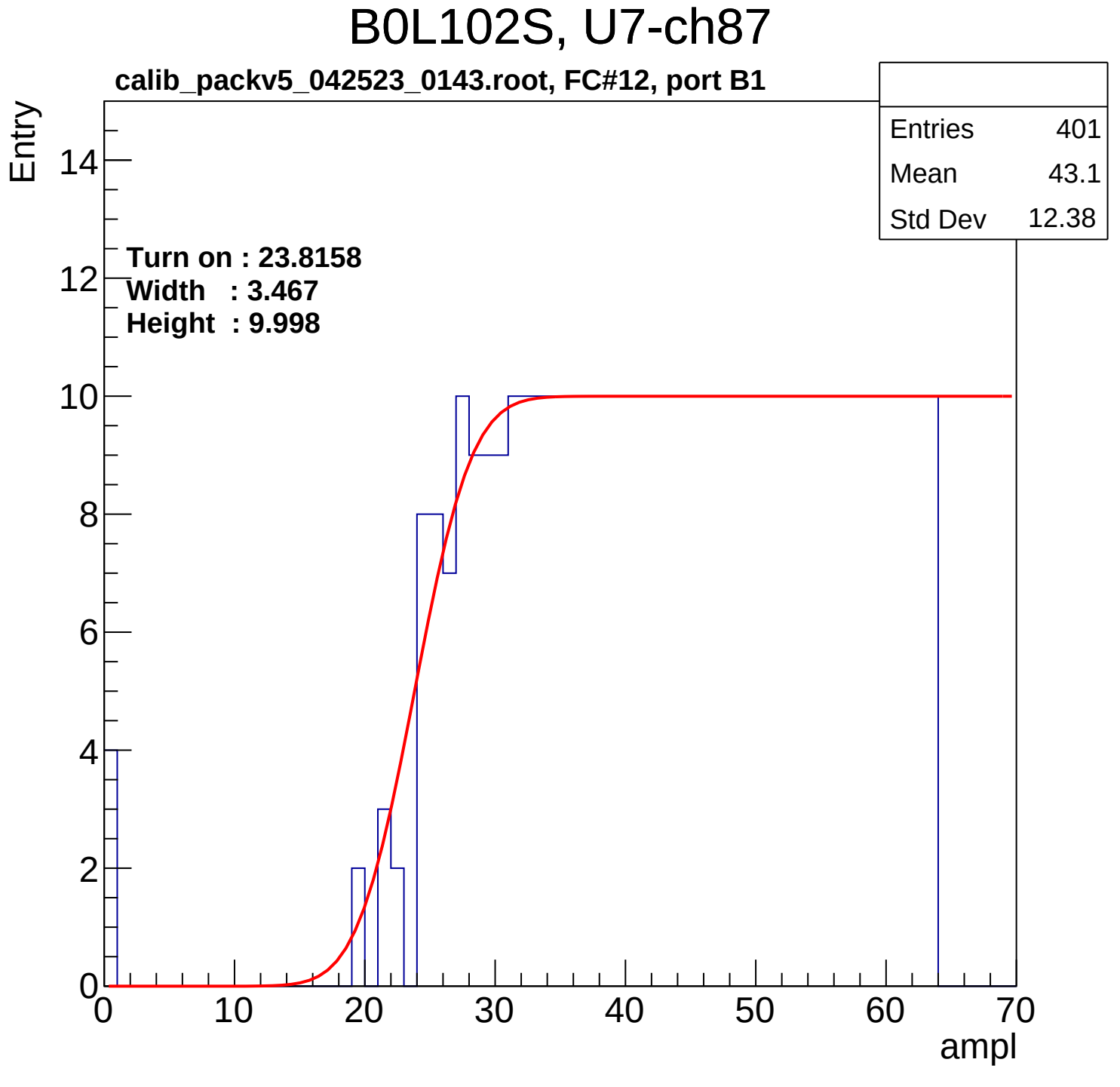
B0L102S, U7-ch87
calib_packv5_042523_0143.root, FC#12, port B1
Entries 401
Mean 43.1
Std Dev 12.38
Turn on : 23.8158
Width : 3.467
Height : 9.998
Entry
ampl
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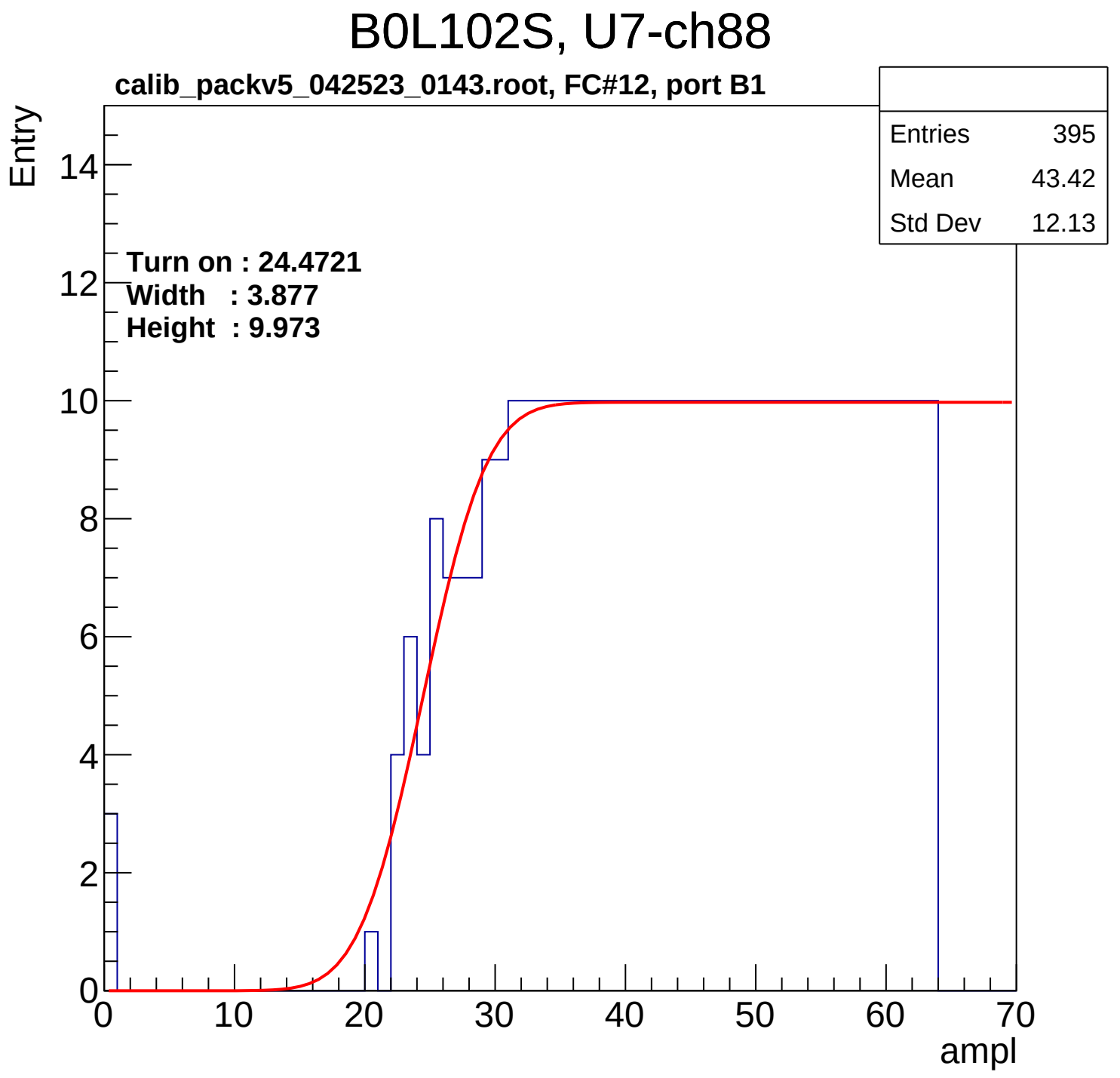
B0L102S, U7-ch88
calib_packv5_042523_0143.root, FC#12, port B1
Entries 395
Mean 43.42
Std Dev 12.13
Turn on : 24.4721
Width : 3.877
Height : 9.973
Entry
ampl
0
2
4
6
8
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0
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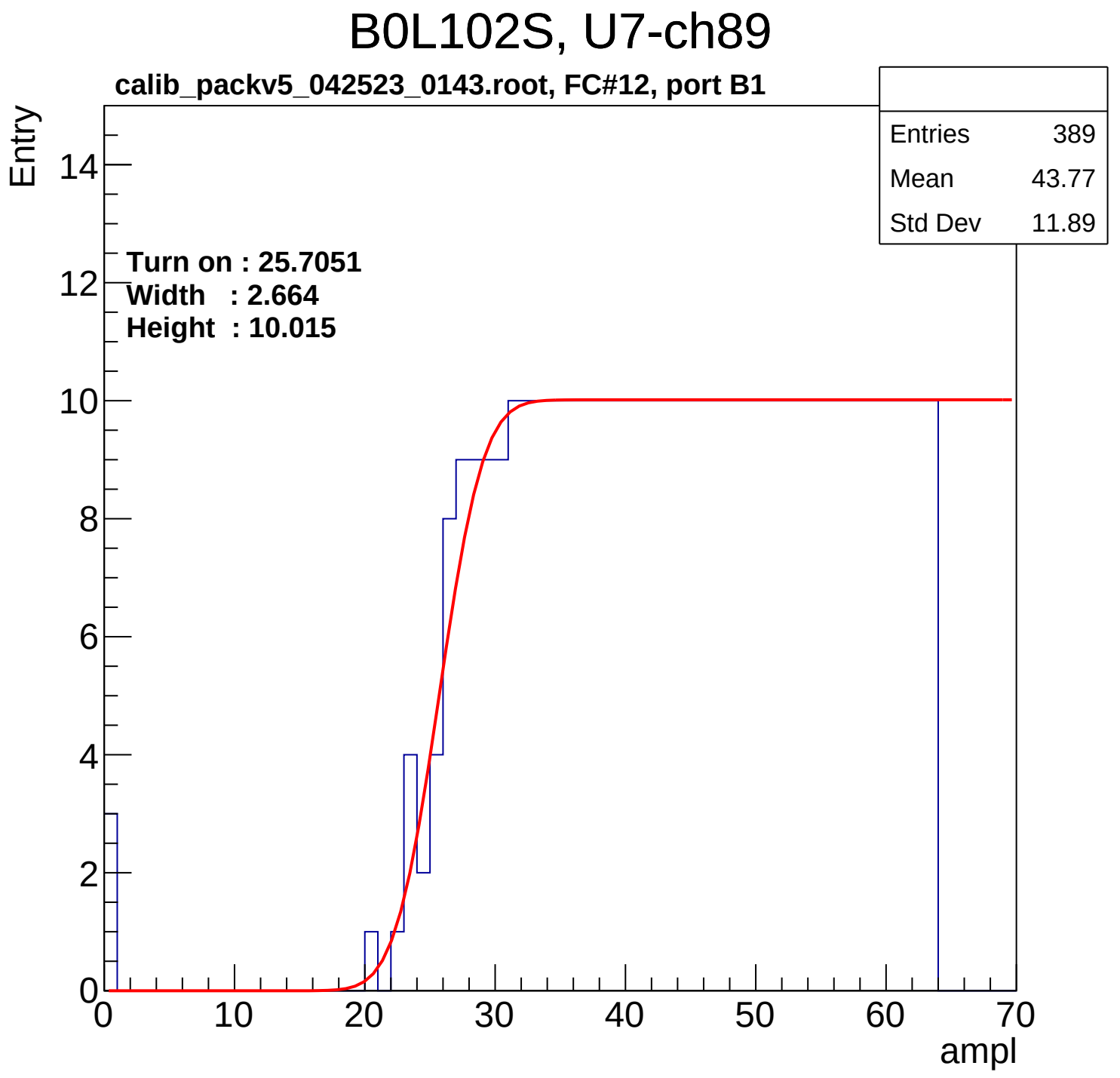
B0L102S, U7-ch89
calib_packv5_042523_0143.root, FC#12, port B1
Entries 389
Mean 43.77
Std Dev 11.89
Turn on : 25.7051
Width : 2.664
Height : 10.015
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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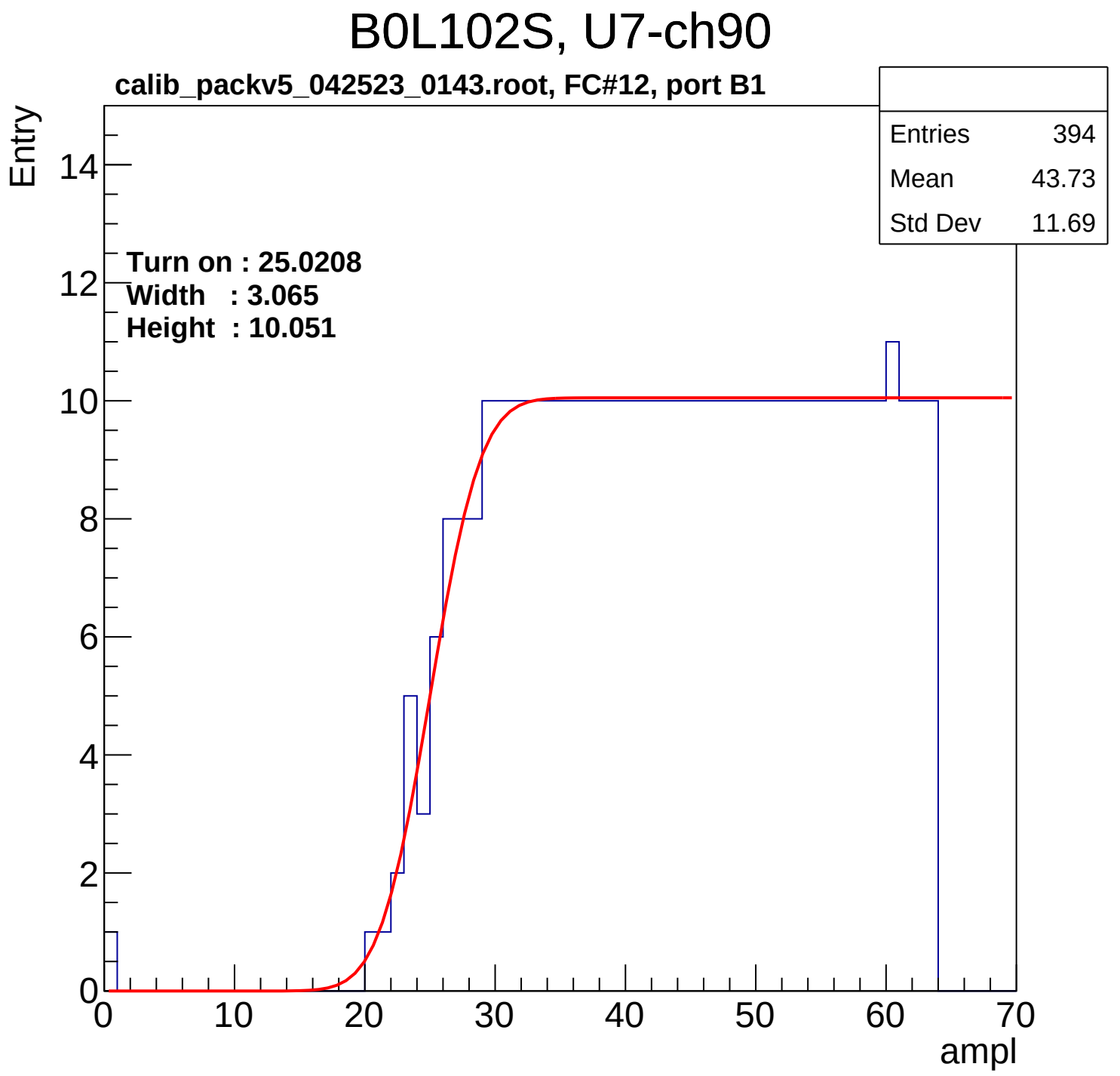
B0L102S, U7-ch90
calib_packv5_042523_0143.root, FC#12, port B1
Entries 394
Mean 43.73
Std Dev 11.69
Turn on : 25.0208
Width : 3.065
Height : 10.051
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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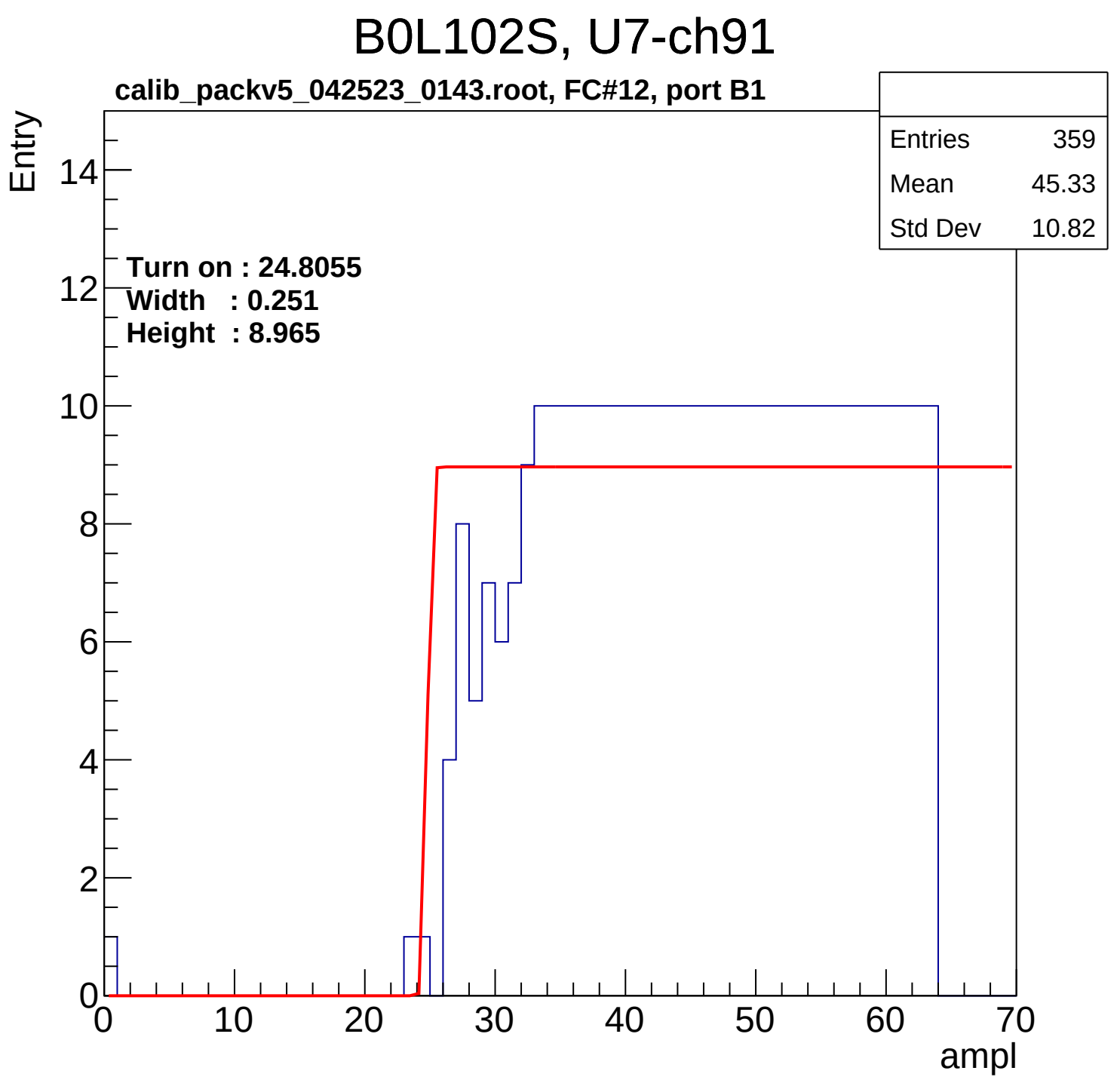
B0L102S, U7-ch91
calib_packv5_042523_0143.root, FC#12, port B1
Entries 359
Mean 45.33
Std Dev 10.82
Turn on : 24.8055
Width : 0.251
Height : 8.965
Entry
ampl
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2
4
6
8
10
12
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0
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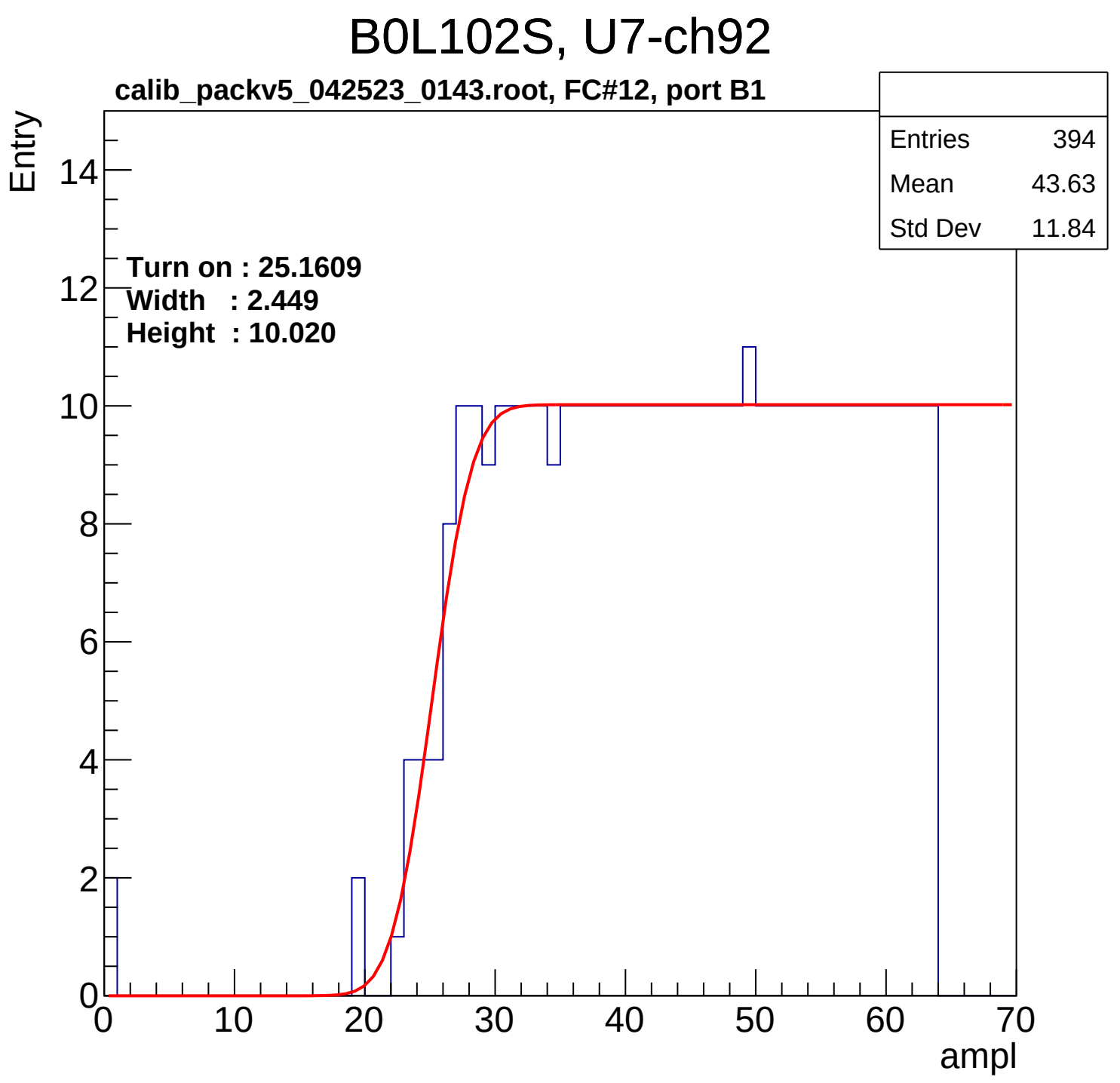
B0L102S, U7-ch92
calib_packv5_042523_0143.root, FC#12, port B1
Entries 394
Mean 43.63
Std Dev 11.84
Turn on : 25.1609
Width : 2.449
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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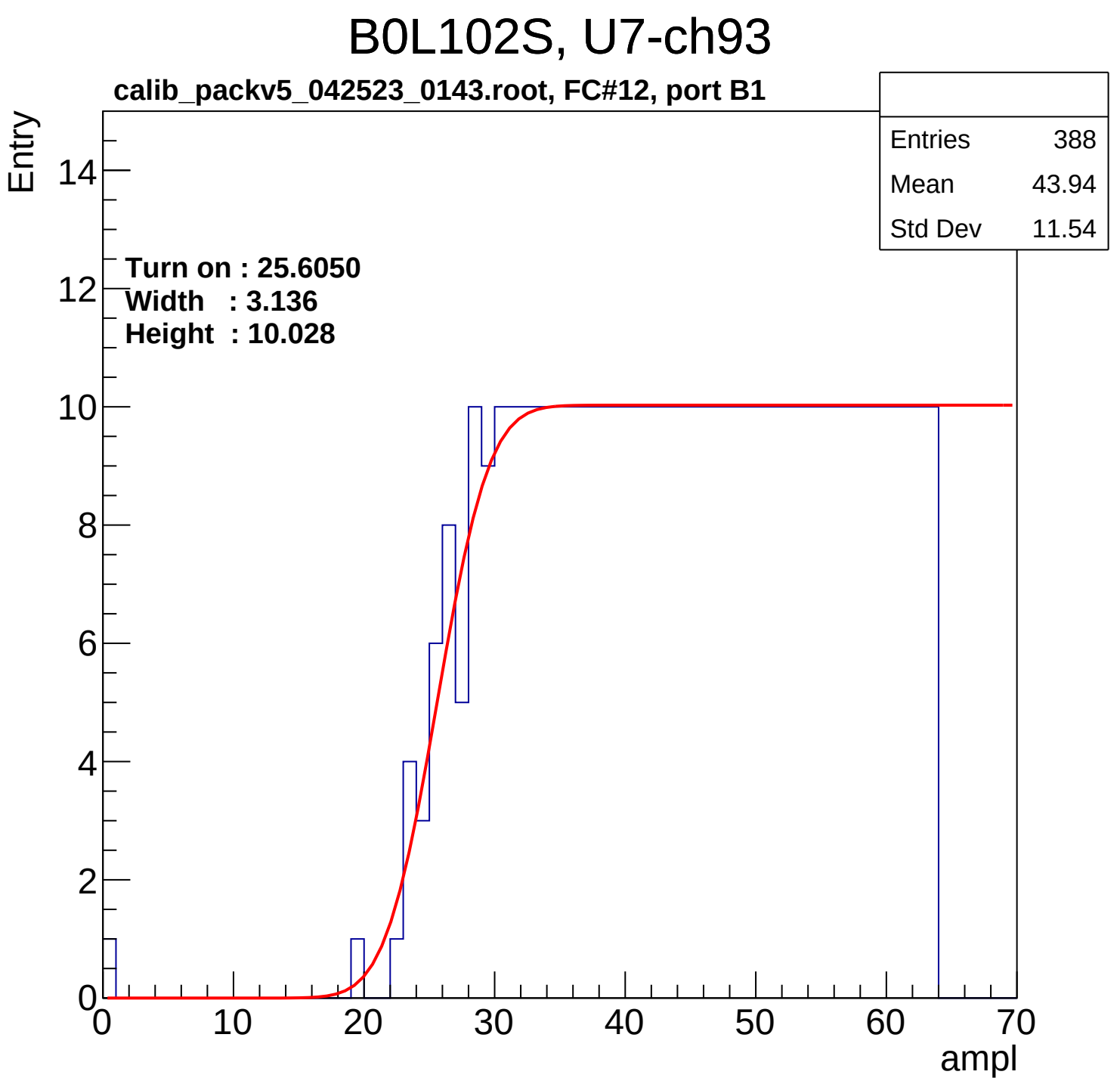
B0L102S, U7-ch93
calib_packv5_042523_0143.root, FC#12, port B1
Entries 388
Mean 43.94
Std Dev 11.54
Turn on : 25.6050
Width : 3.136
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
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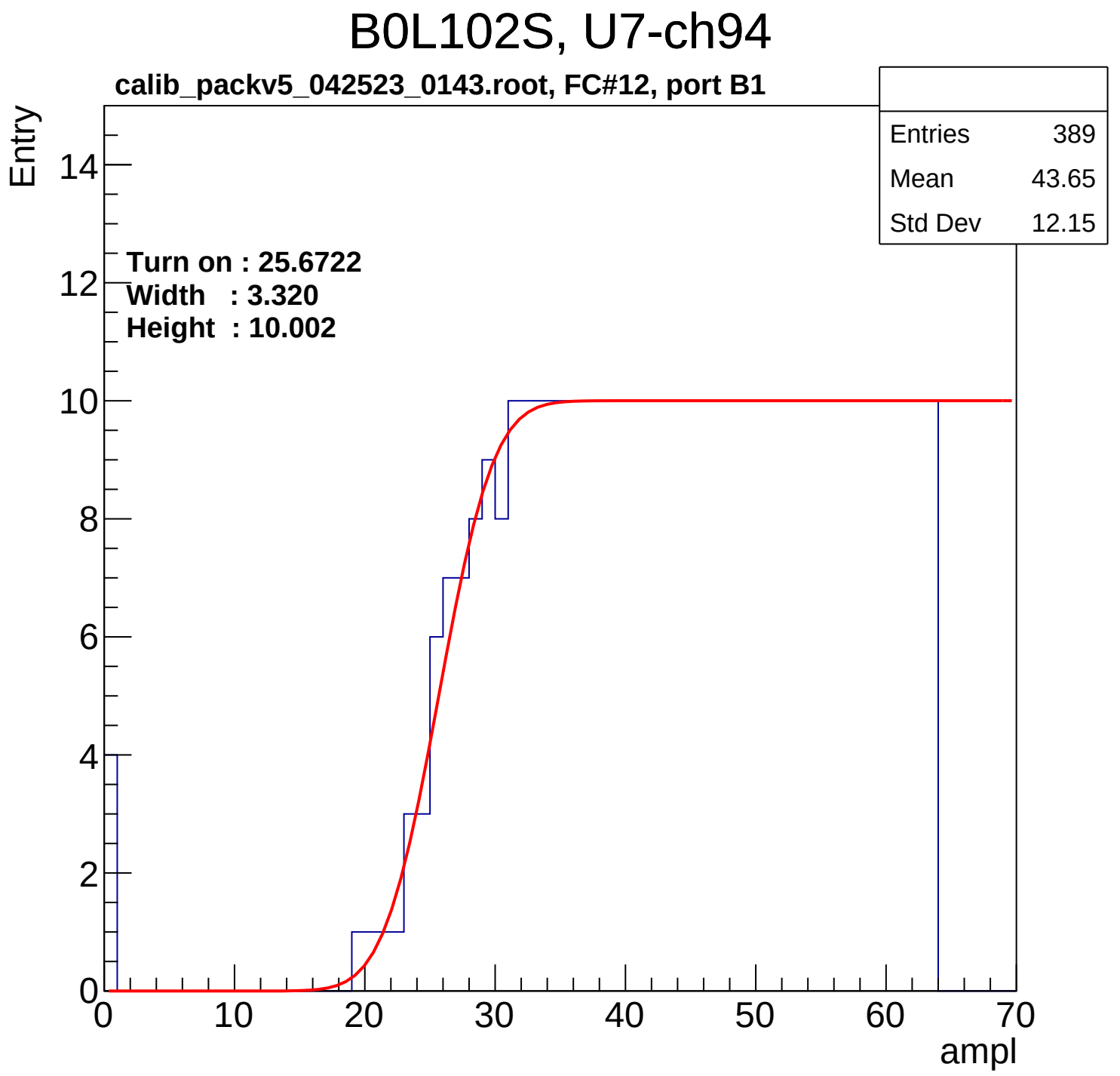
B0L102S, U7-ch94
calib_packv5_042523_0143.root, FC#12, port B1
Entries 389
Mean 43.65
Std Dev 12.15
Turn on : 25.6722
Width : 3.320
Height : 10.002
Entry
ampl
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2
4
6
8
10
12
14
0
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40
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60
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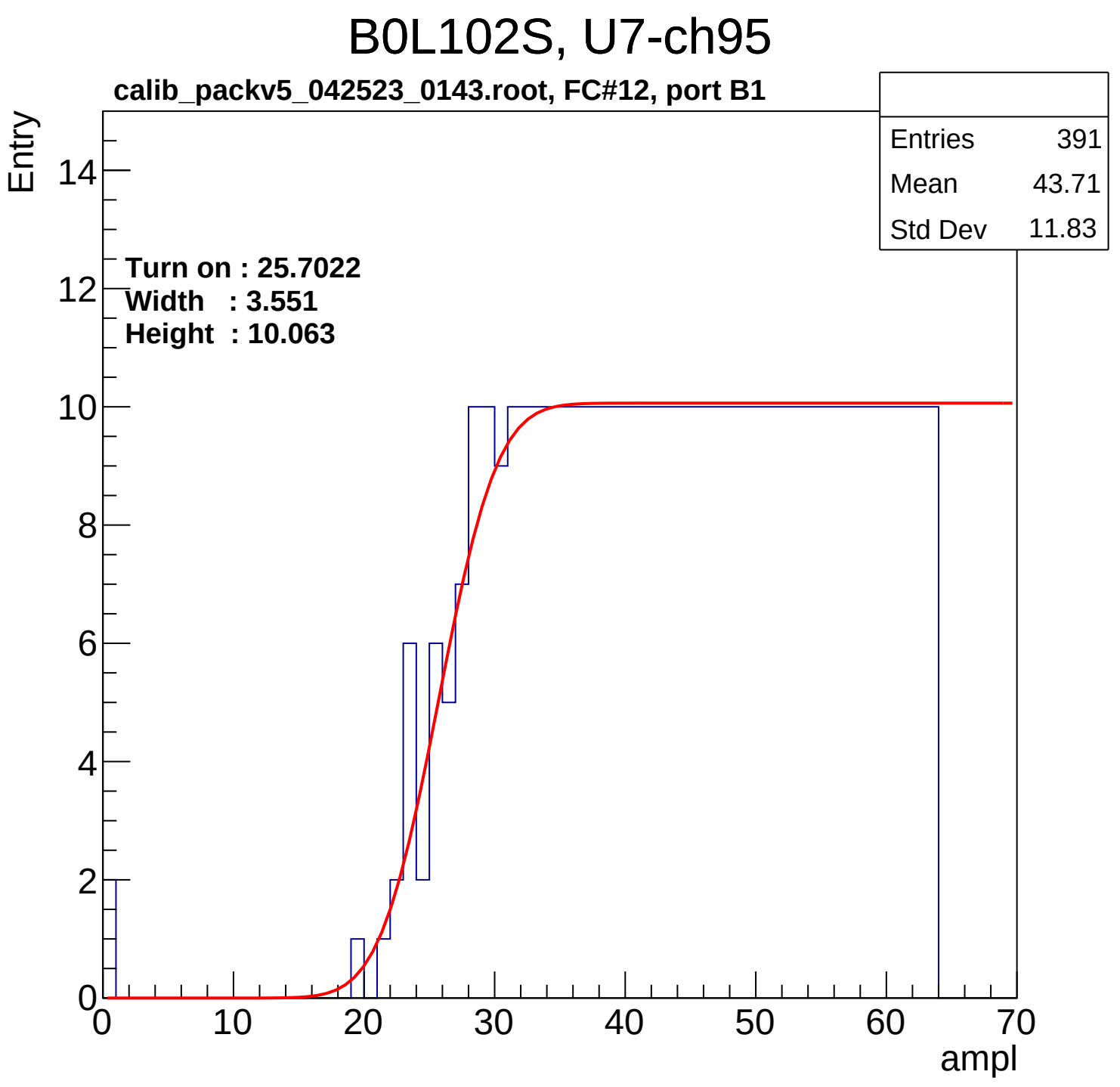
B0L102S, U7-ch95
calib_packv5_042523_0143.root, FC#12, port B1
Entries 391
Mean 43.71
Std Dev 11.83
Turn on : 25.7022
Width : 3.551
Height : 10.063
Entry
ampl
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2
4
6
8
10
12
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0
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60
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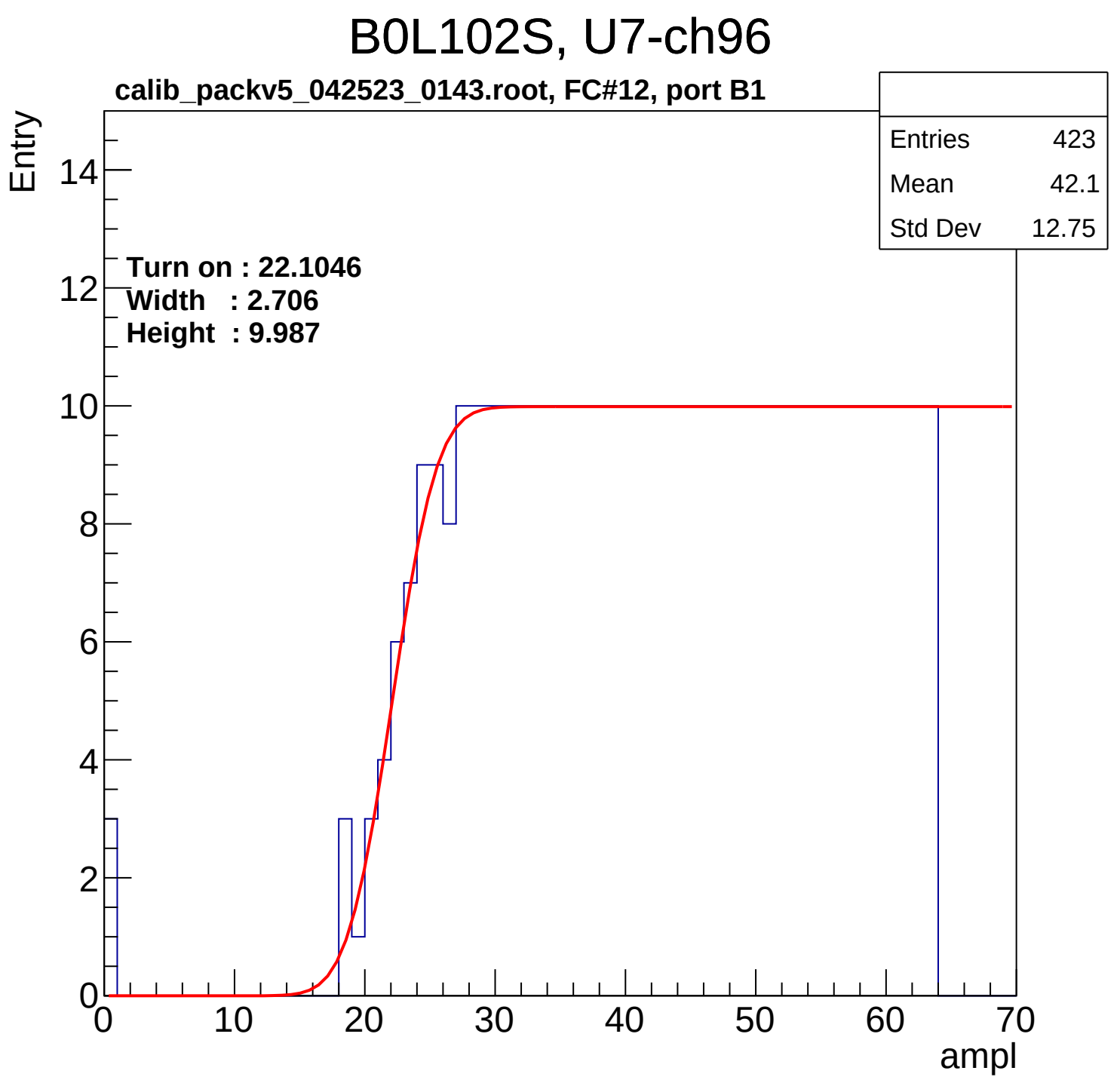
B0L102S, U7-ch96
calib_packv5_042523_0143.root, FC#12, port B1
Entries 423
Mean 42.1
Std Dev 12.75
Turn on : 22.1046
Width : 2.706
Height : 9.987
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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60
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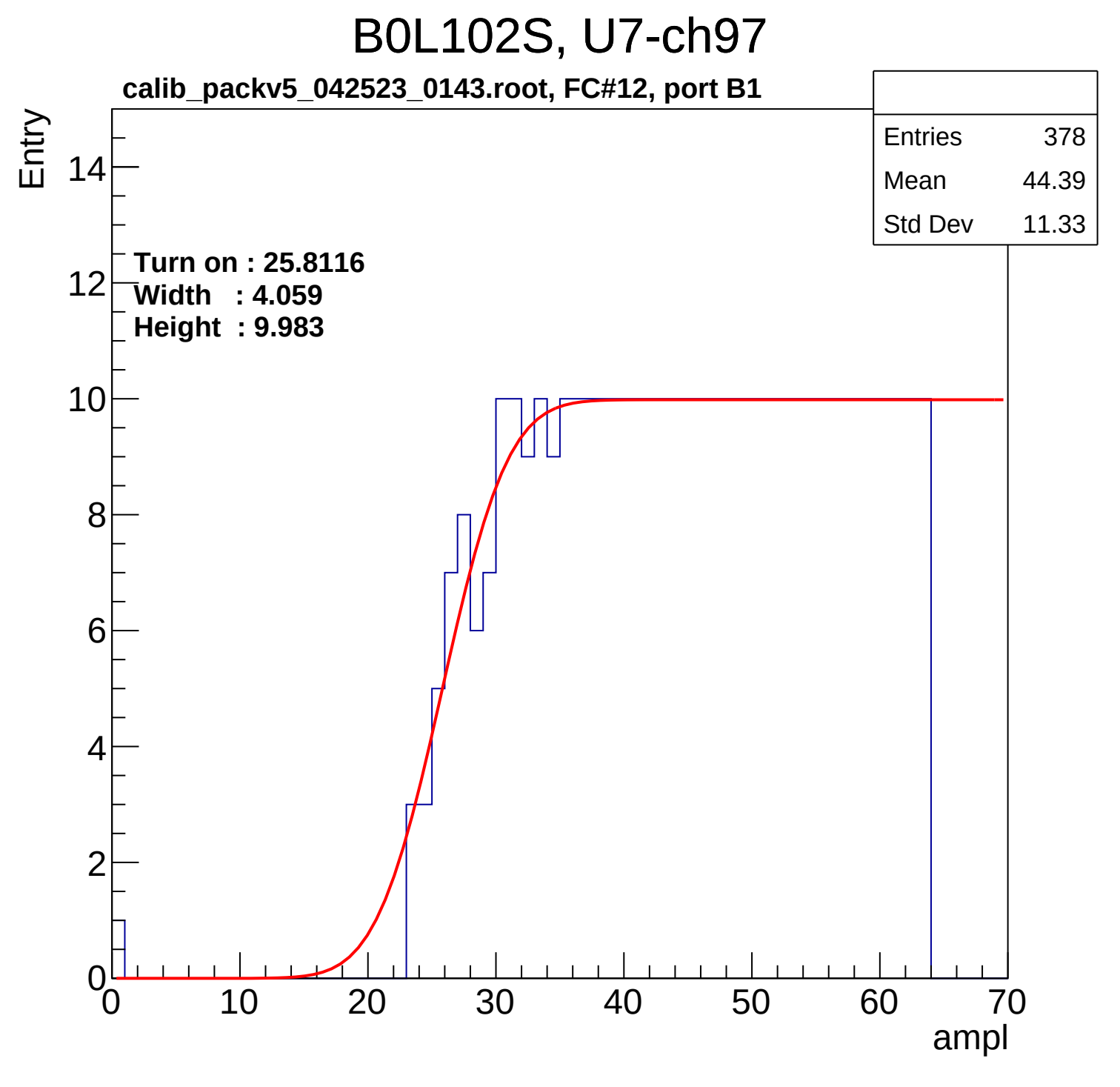
B0L102S, U7-ch97
calib_packv5_042523_0143.root, FC#12, port B1
Entries 378
Mean 44.39
Std Dev 11.33
Turn on : 25.8116
Width : 4.059
Height : 9.983
Entry
ampl
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4
6
8
10
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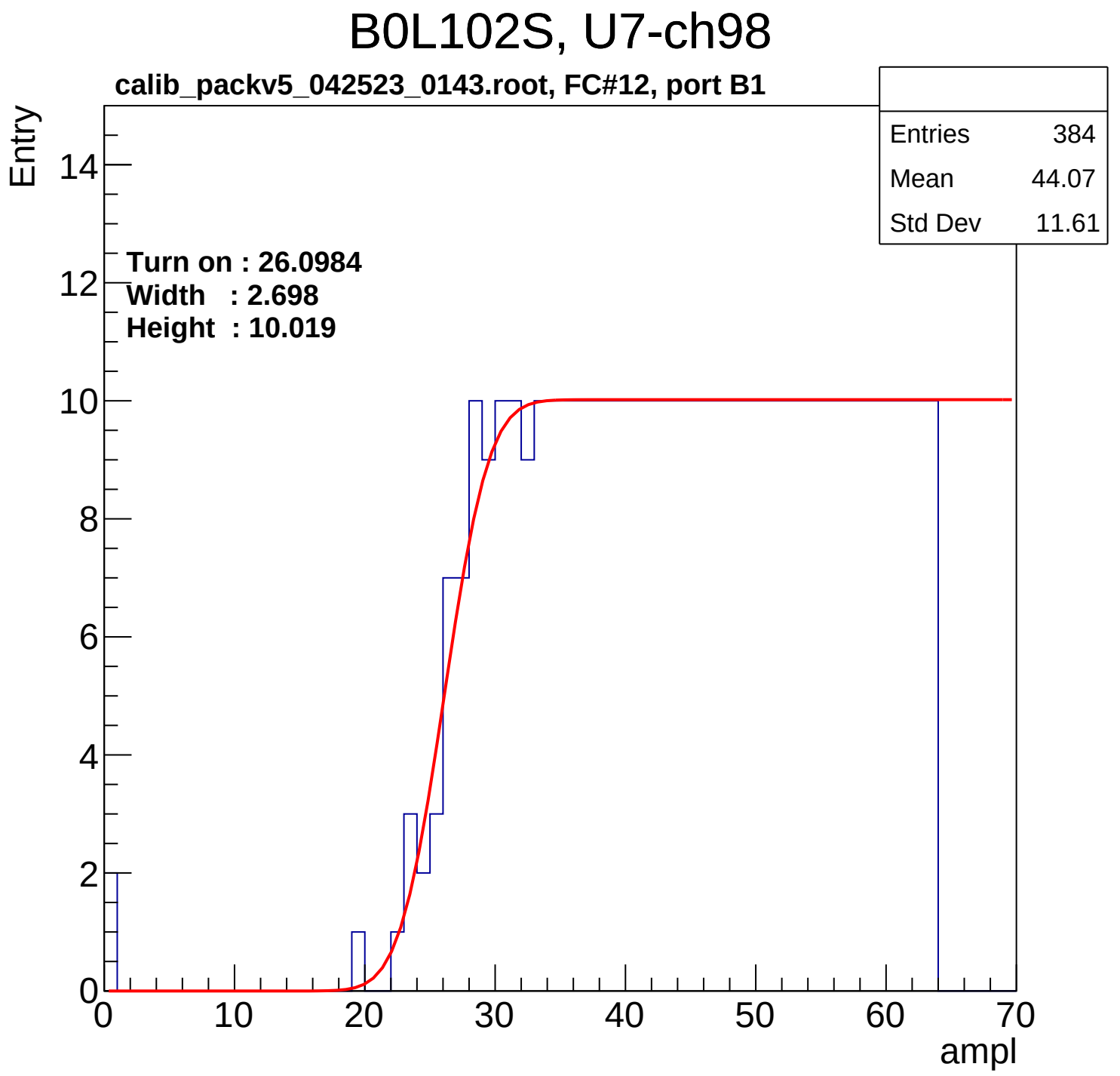
B0L102S, U7-ch98
calib_packv5_042523_0143.root, FC#12, port B1
Entries 384
Mean 44.07
Std Dev 11.61
Turn on : 26.0984
Width : 2.698
Height : 10.019
Entry
ampl
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4
6
8
10
12
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0
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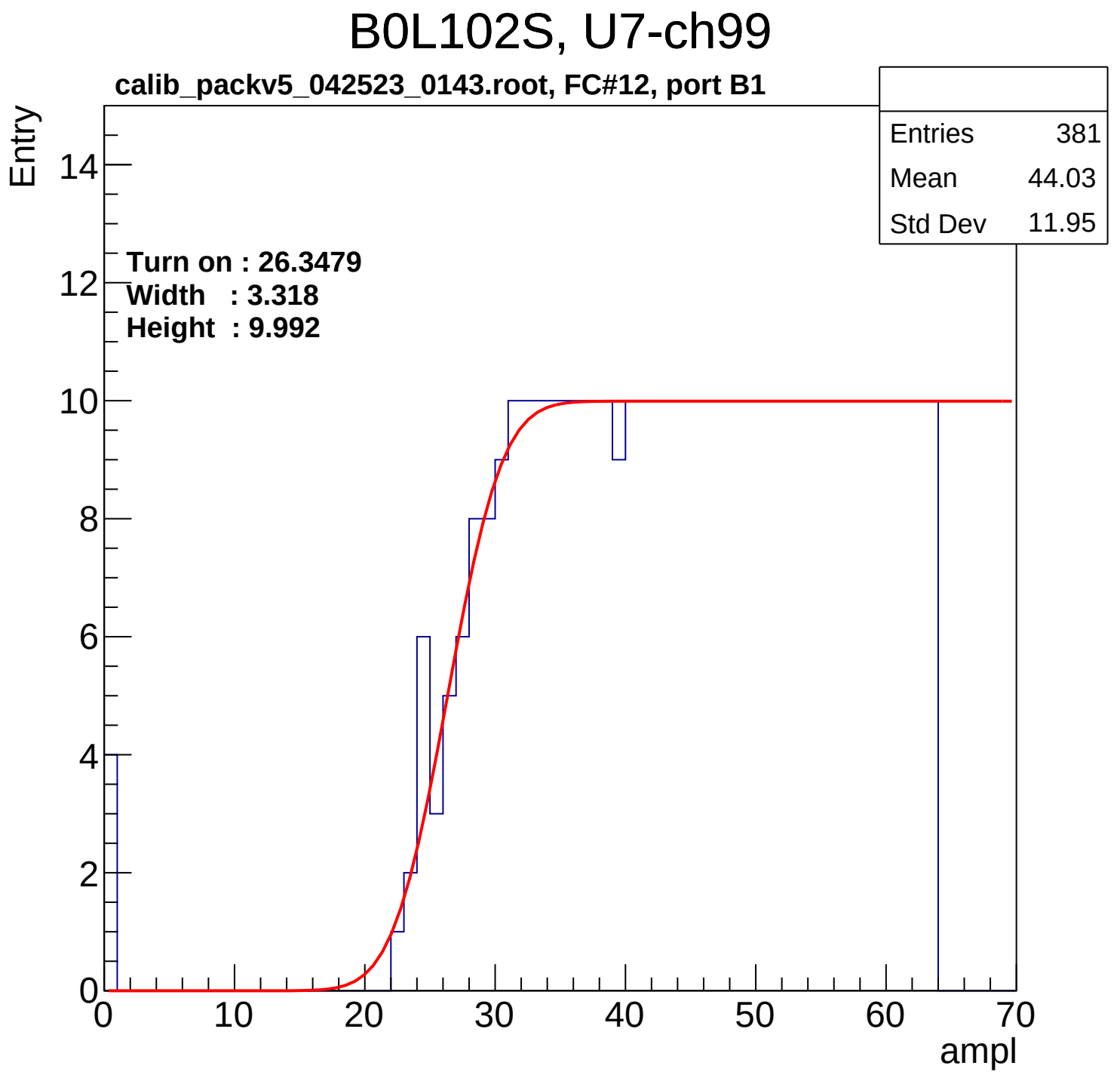
B0L102S, U7-ch99
calib_packv5_042523_0143.root, FC#12, port B1
Entries 381
Mean 44.03
Std Dev 11.95
Turn on : 26.3479
Width : 3.318
Height : 9.992
Entry
ampl
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6
8
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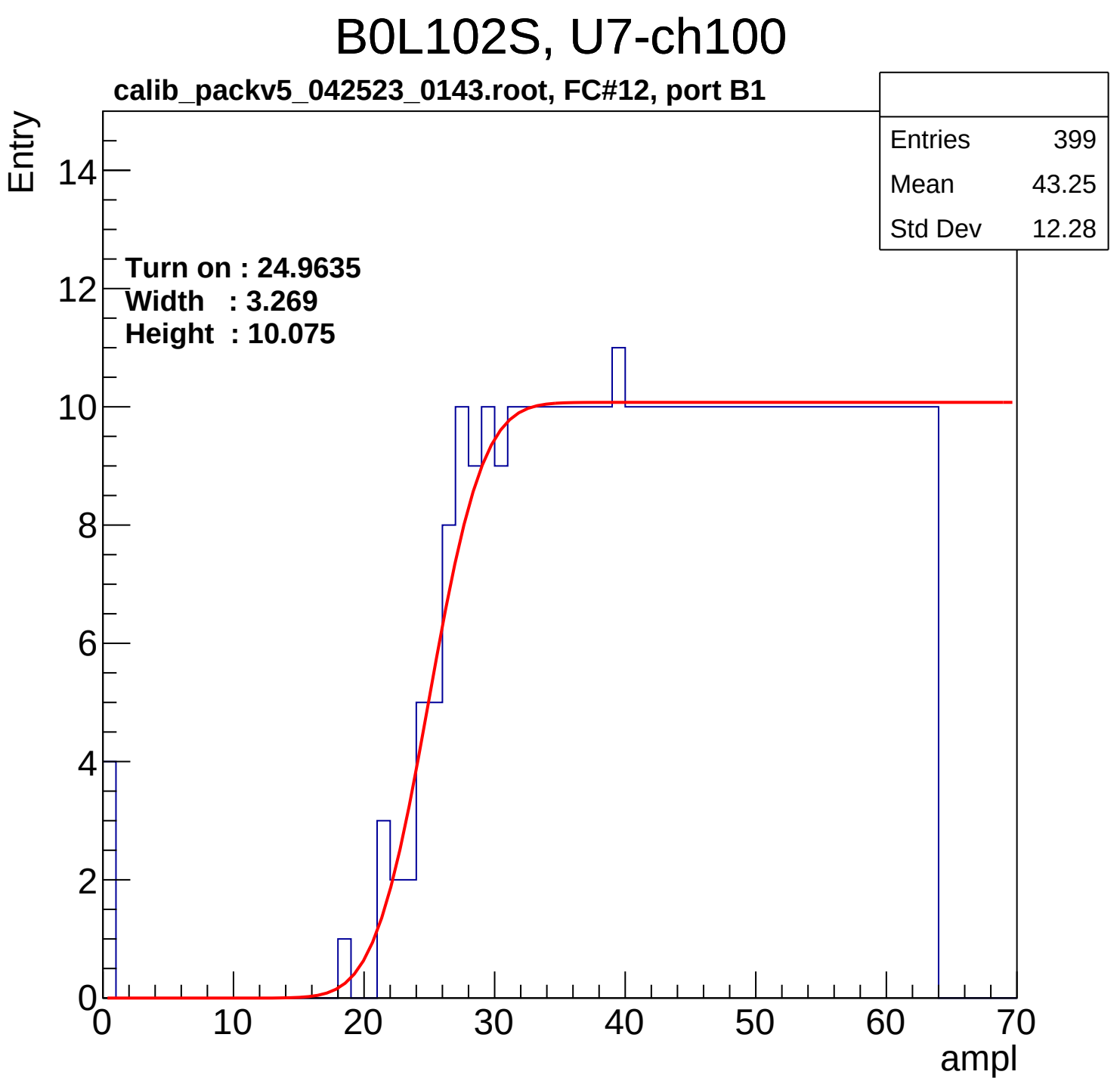
B0L102S, U7-ch100
calib_packv5_042523_0143.root, FC#12, port B1
Entries 399
Mean 43.25
Std Dev 12.28
Turn on : 24.9635
Width : 3.269
Height : 10.075
Entry
ampl
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6
8
10
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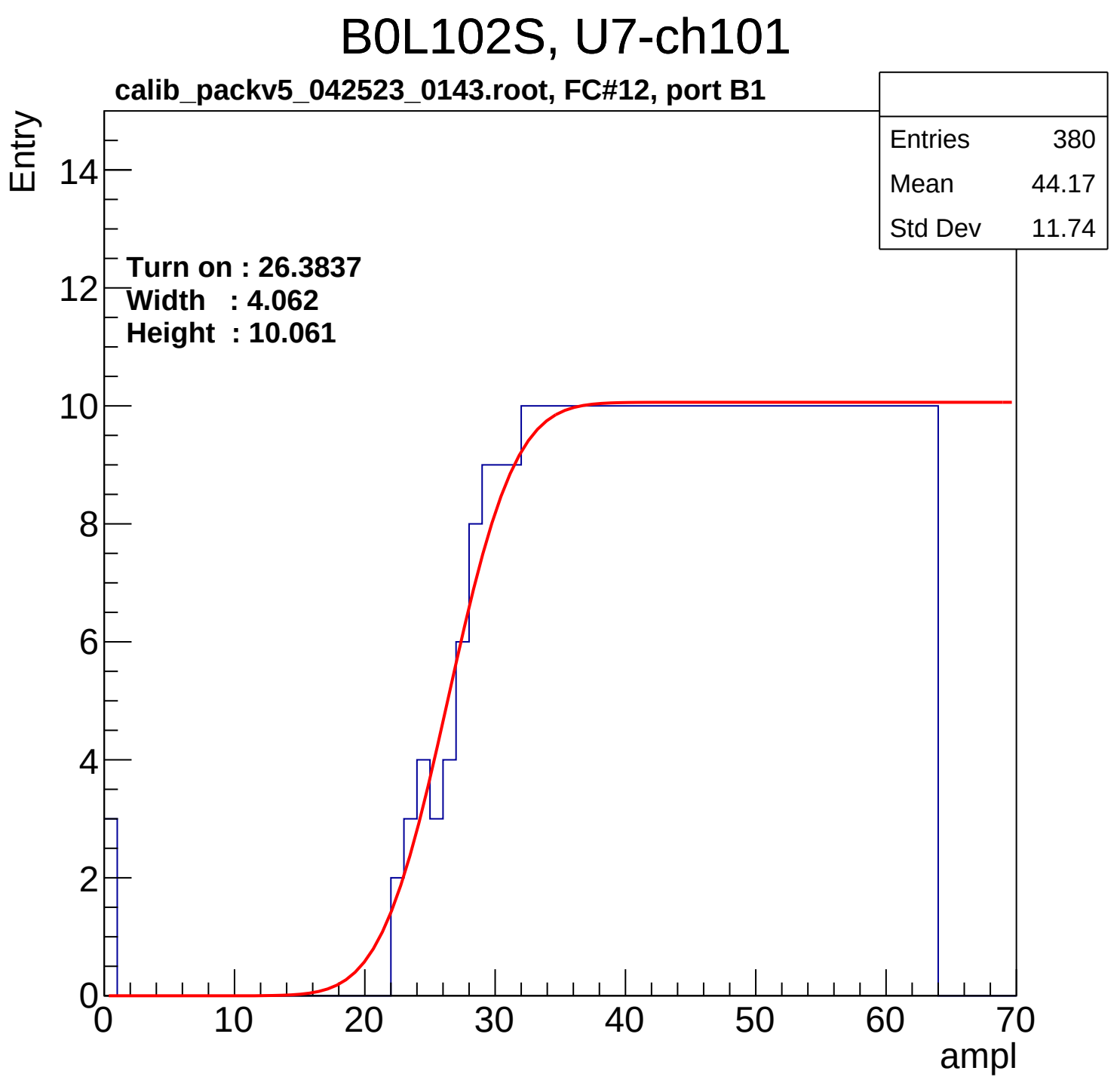
B0L102S, U7-ch101
calib_packv5_042523_0143.root, FC#12, port B1
Entries 380
Mean 44.17
Std Dev 11.74
Turn on : 26.3837
Width : 4.062
Height : 10.061
Entry
ampl
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6
8
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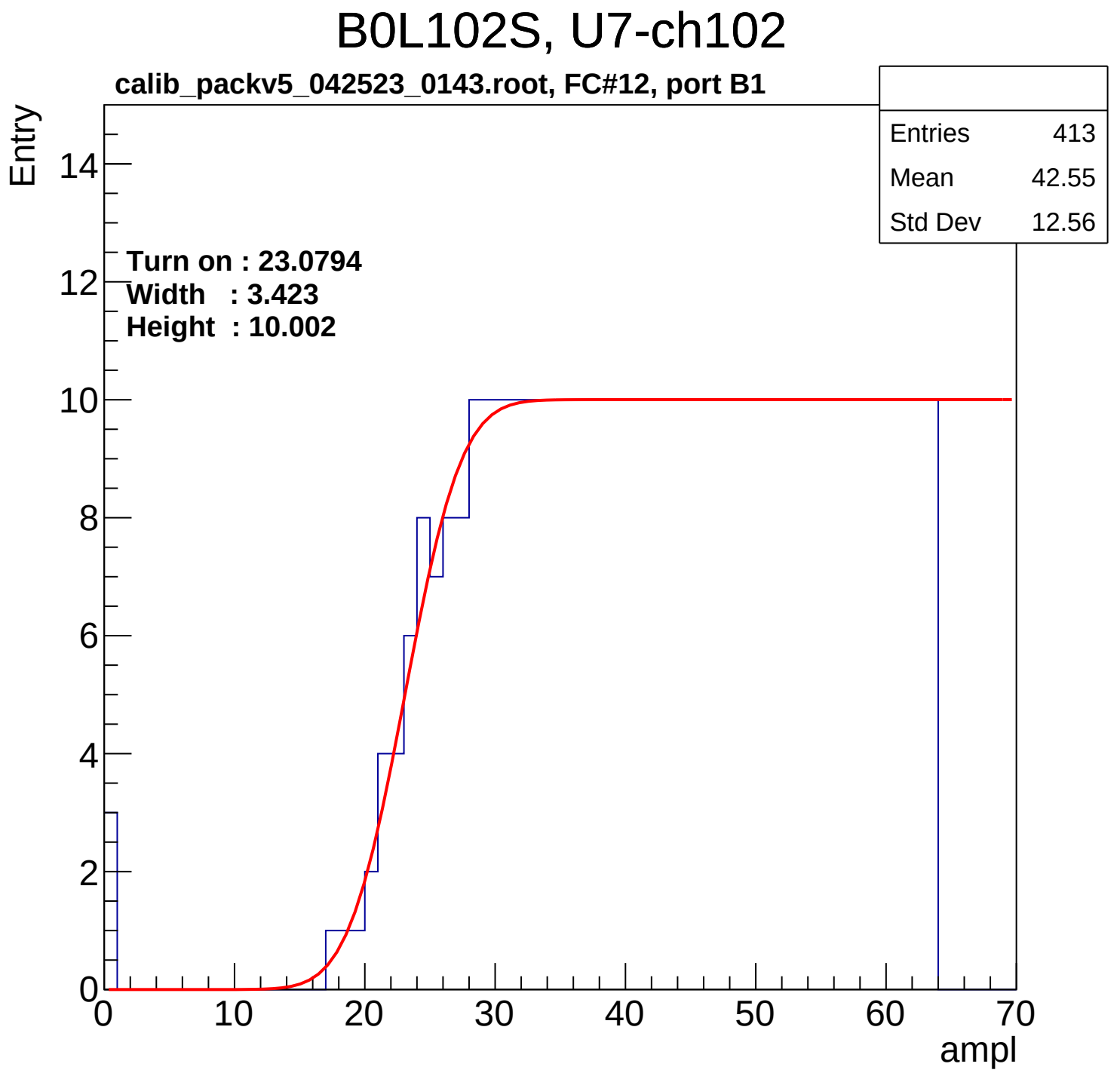
B0L102S, U7-ch102
calib_packv5_042523_0143.root, FC#12, port B1
Entries 413
Mean 42.55
Std Dev 12.56
Turn on : 23.0794
Width : 3.423
Height : 10.002
Entry
ampl
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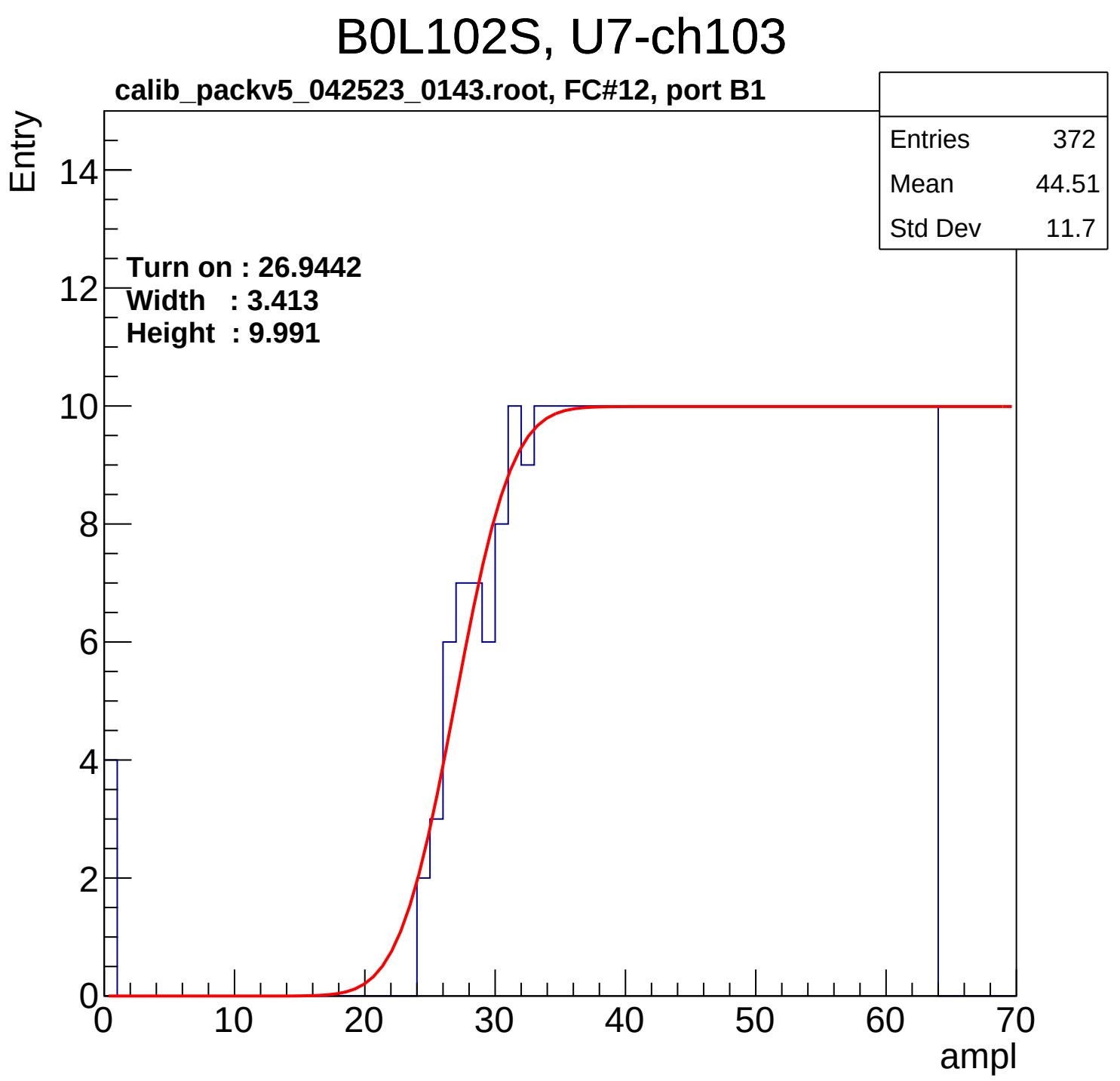
B0L102S, U7-ch103
calib_packv5_042523_0143.root, FC#12, port B1
Entries 372
Mean 44.51
Std Dev 11.7
Turn on : 26.9442
Width : 3.413
Height : 9.991
Entry
ampl
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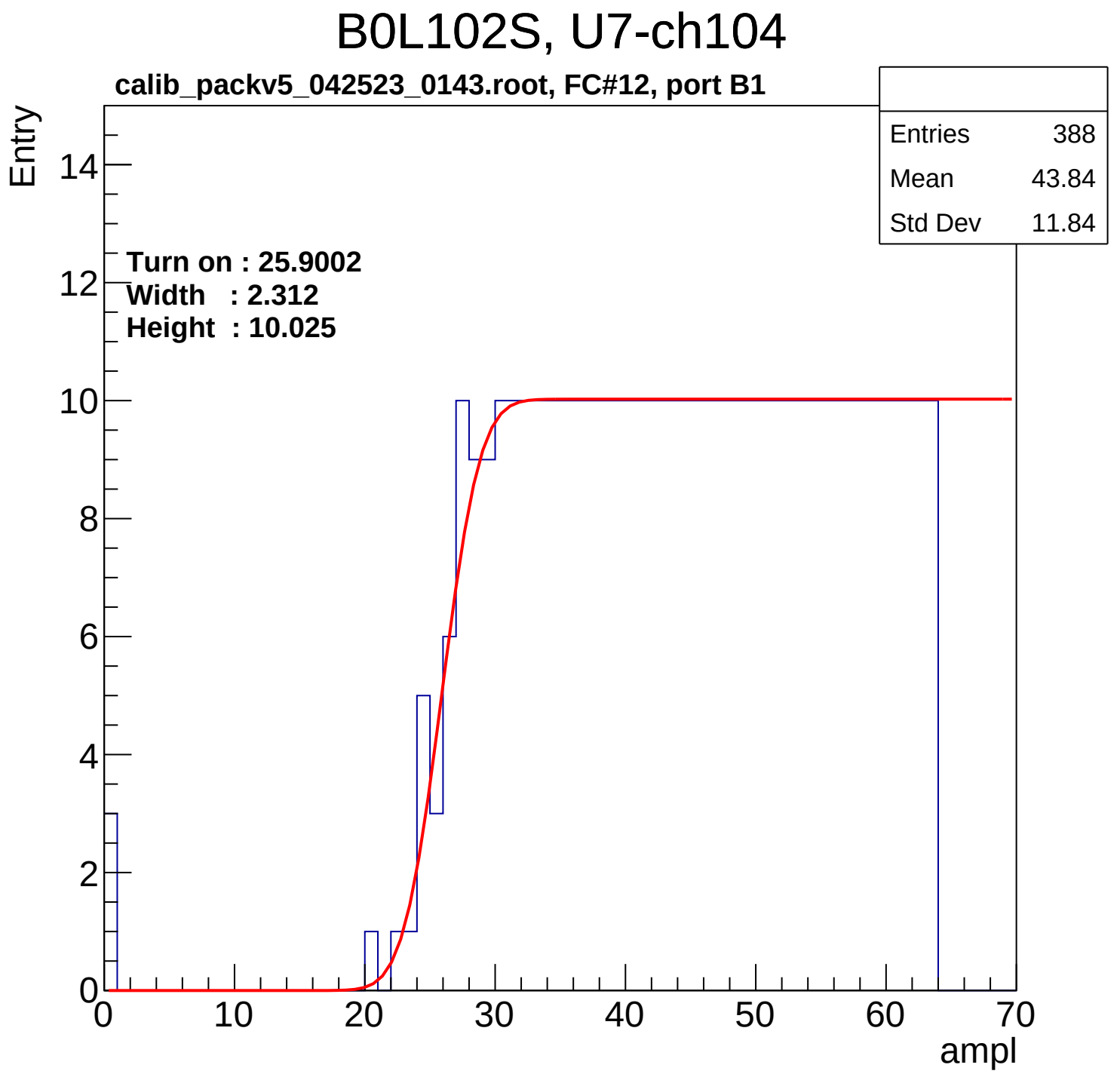
B0L102S, U7-ch104
calib_packv5_042523_0143.root, FC#12, port B1
Entries 388
Mean 43.84
Std Dev 11.84
Turn on : 25.9002
Width : 2.312
Height : 10.025
Entry
ampl
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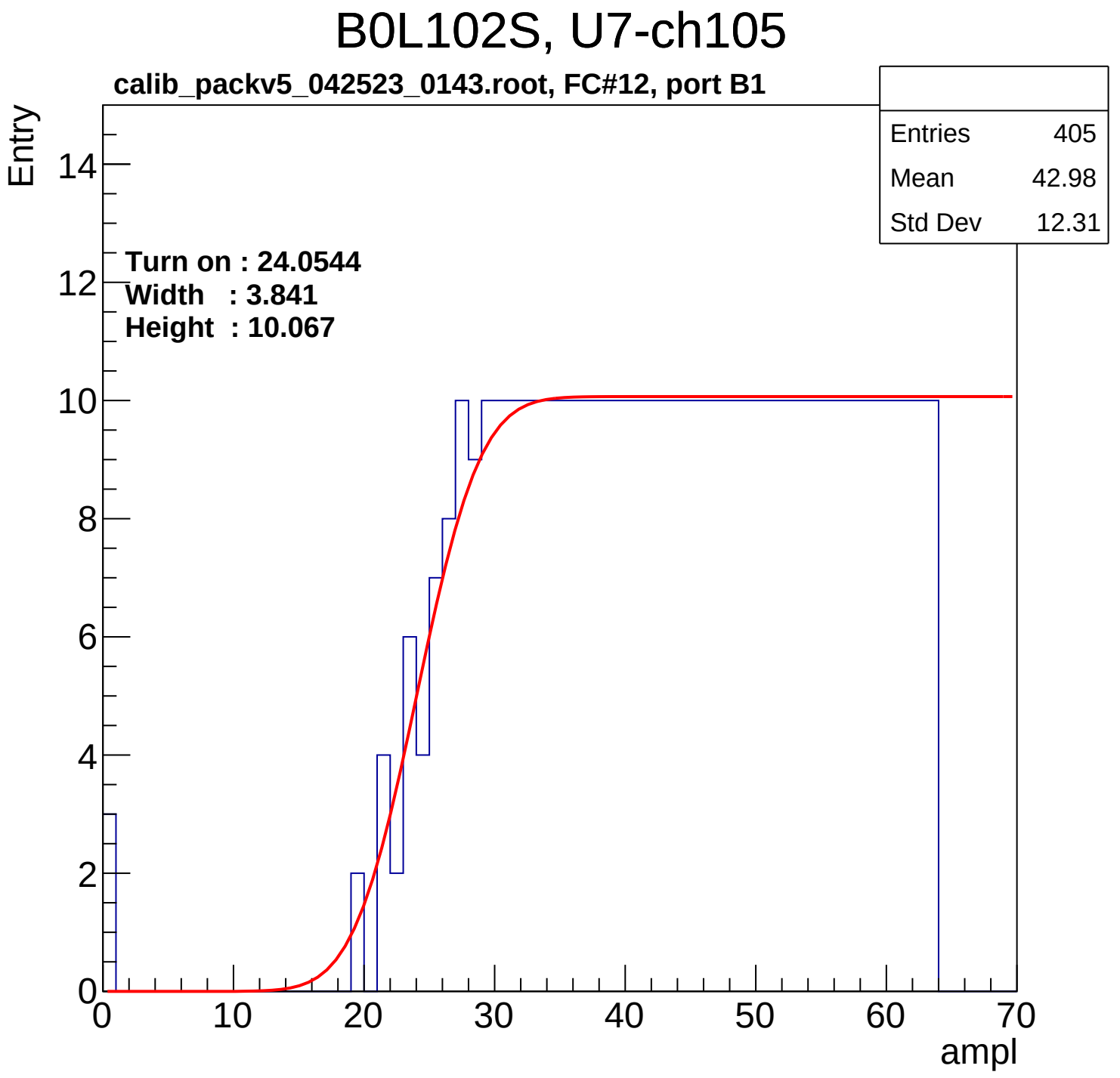
B0L102S, U7-ch105
calib_packv5_042523_0143.root, FC#12, port B1
Entries 405
Mean 42.98
Std Dev 12.31
Turn on : 24.0544
Width : 3.841
Height : 10.067
Entry
ampl
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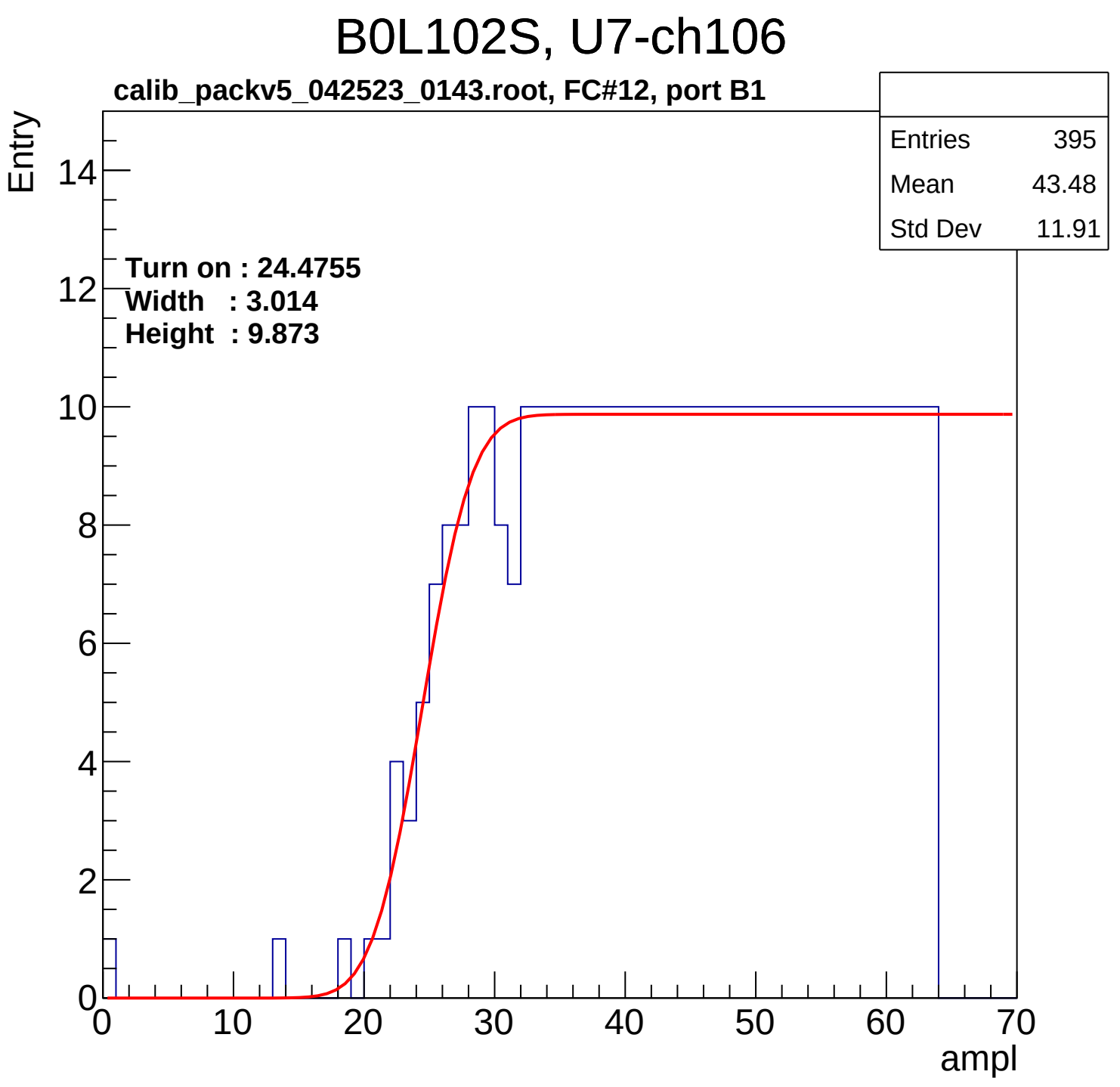
B0L102S, U7-ch106
calib_packv5_042523_0143.root, FC#12, port B1
Entries 395
Mean 43.48
Std Dev 11.91
Turn on : 24.4755
Width : 3.014
Height : 9.873
Entry
ampl
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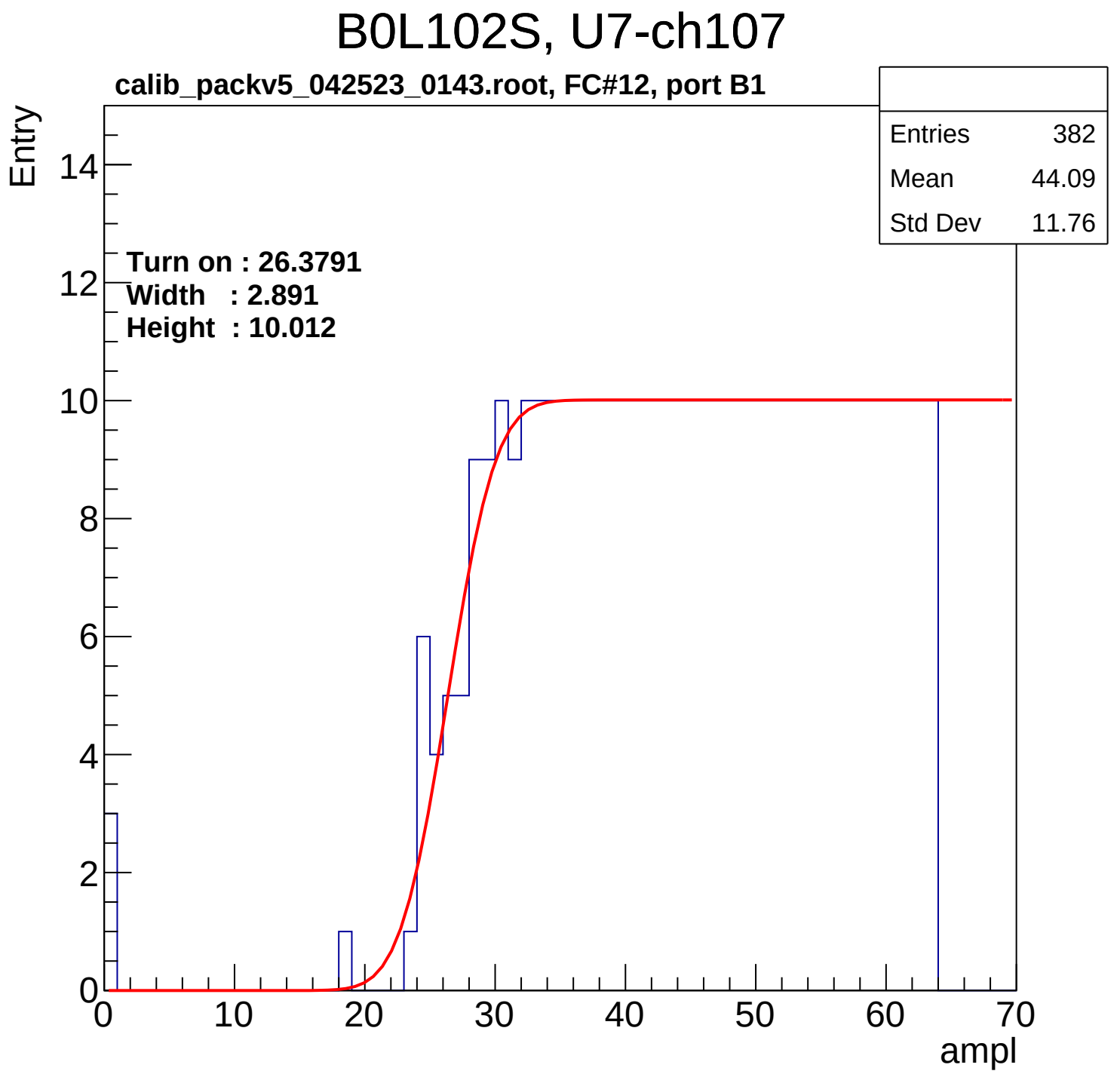
B0L102S, U7-ch107
calib_packv5_042523_0143.root, FC#12, port B1
Entries 382
Mean 44.09
Std Dev 11.76
Turn on : 26.3791
Width : 2.891
Height : 10.012
Entry
ampl
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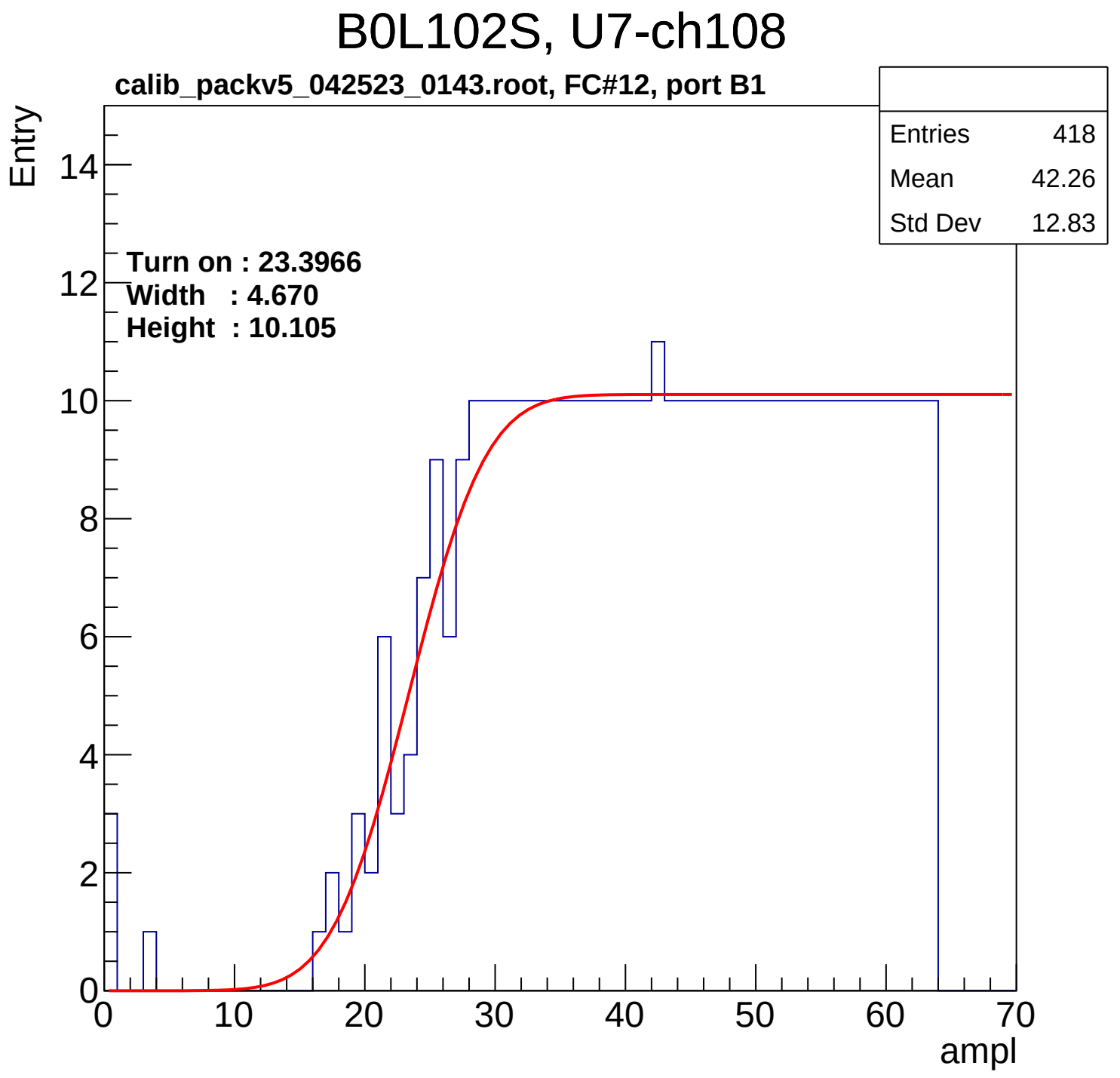
B0L102S, U7-ch108
calib_packv5_042523_0143.root, FC#12, port B1
Entries 418
Mean 42.26
Std Dev 12.83
Turn on : 23.3966
Width : 4.670
Height : 10.105
Entry
ampl
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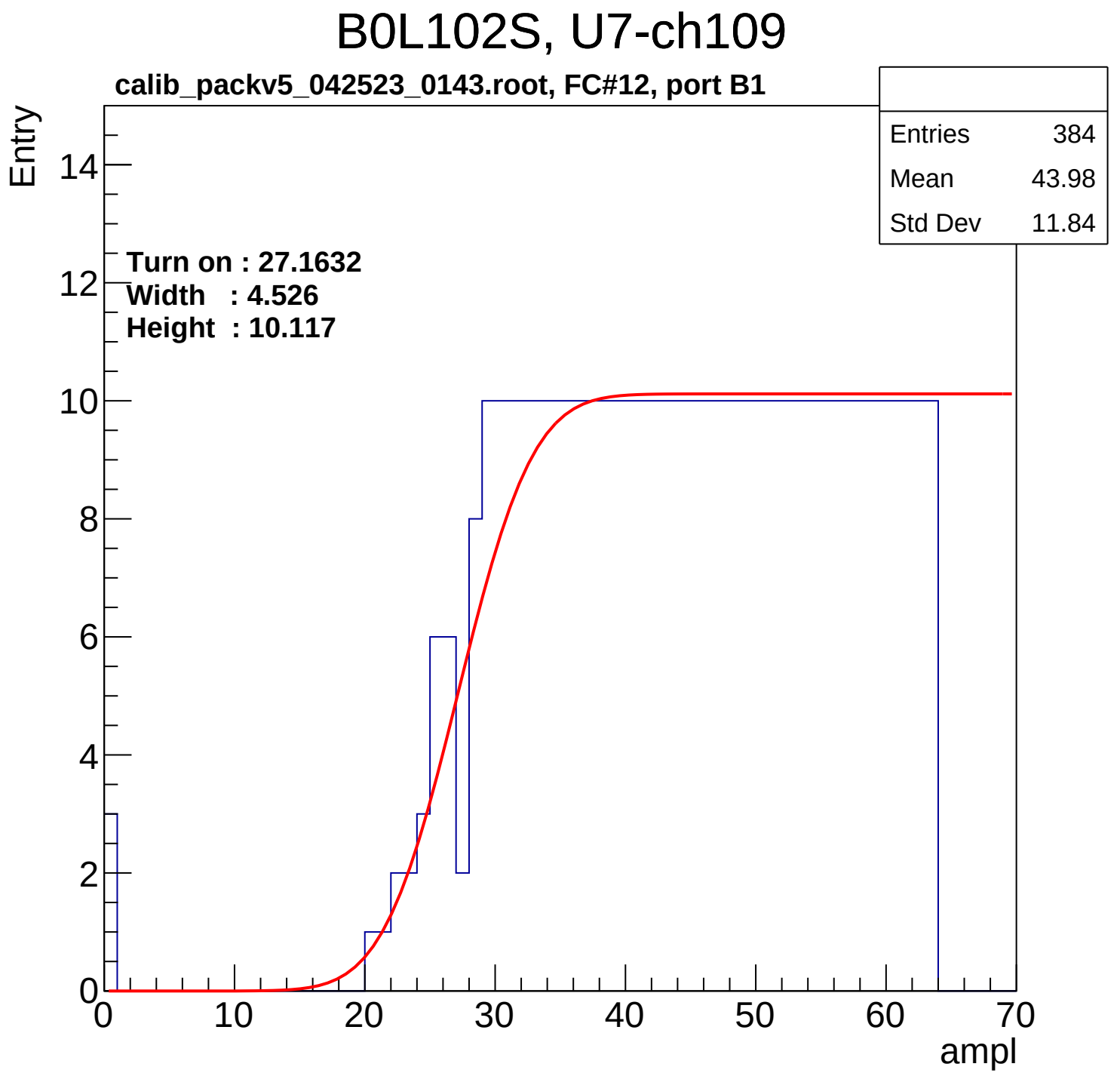
B0L102S, U7-ch109
calib_packv5_042523_0143.root, FC#12, port B1
Entries 384
Mean 43.98
Std Dev 11.84
Turn on : 27.1632
Width : 4.526
Height : 10.117
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ampl
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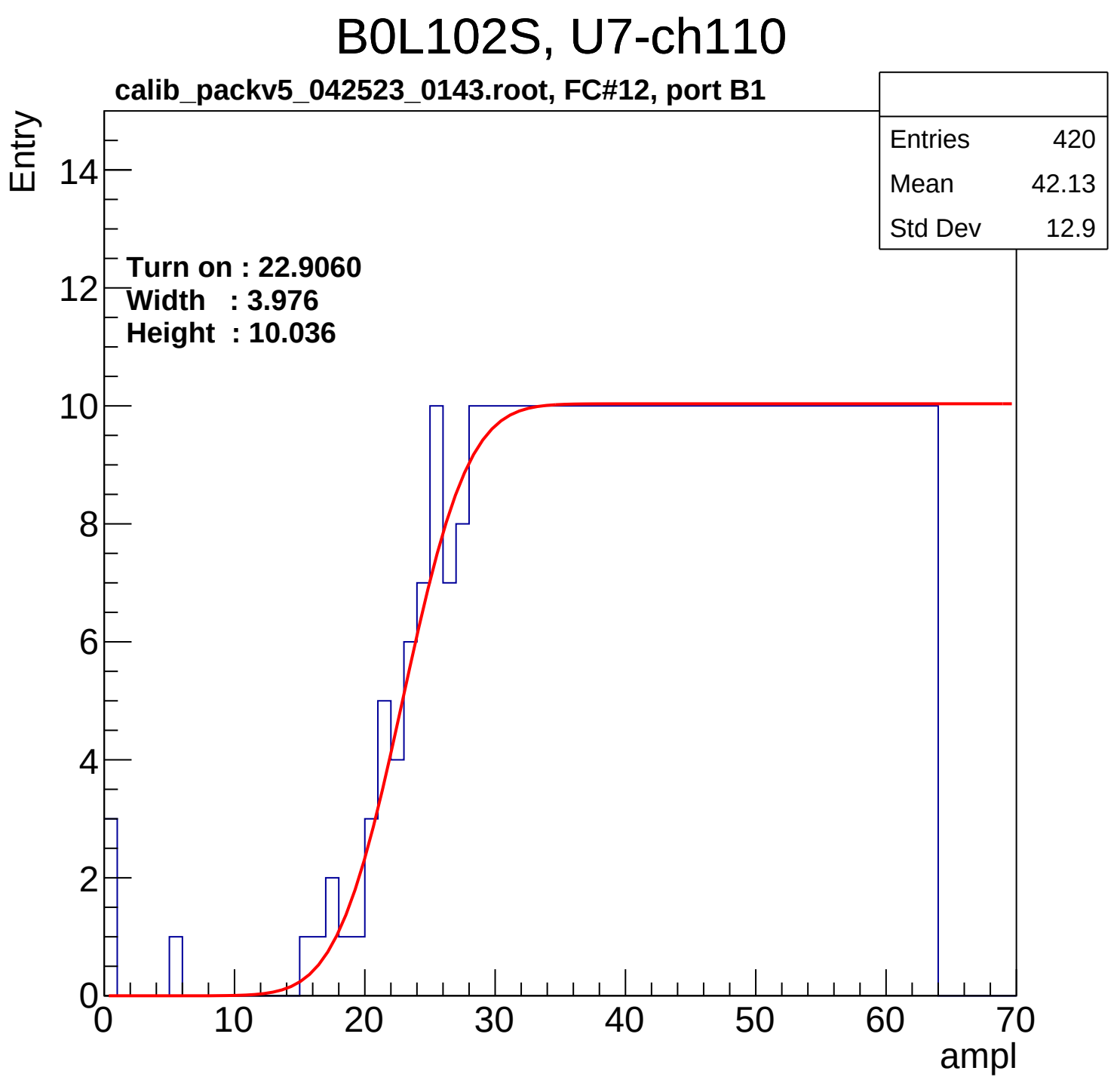
B0L102S, U7-ch110
calib_packv5_042523_0143.root, FC#12, port B1
Entries 420
Mean 42.13
Std Dev 12.9
Turn on : 22.9060
Width : 3.976
Height : 10.036
Entry
ampl
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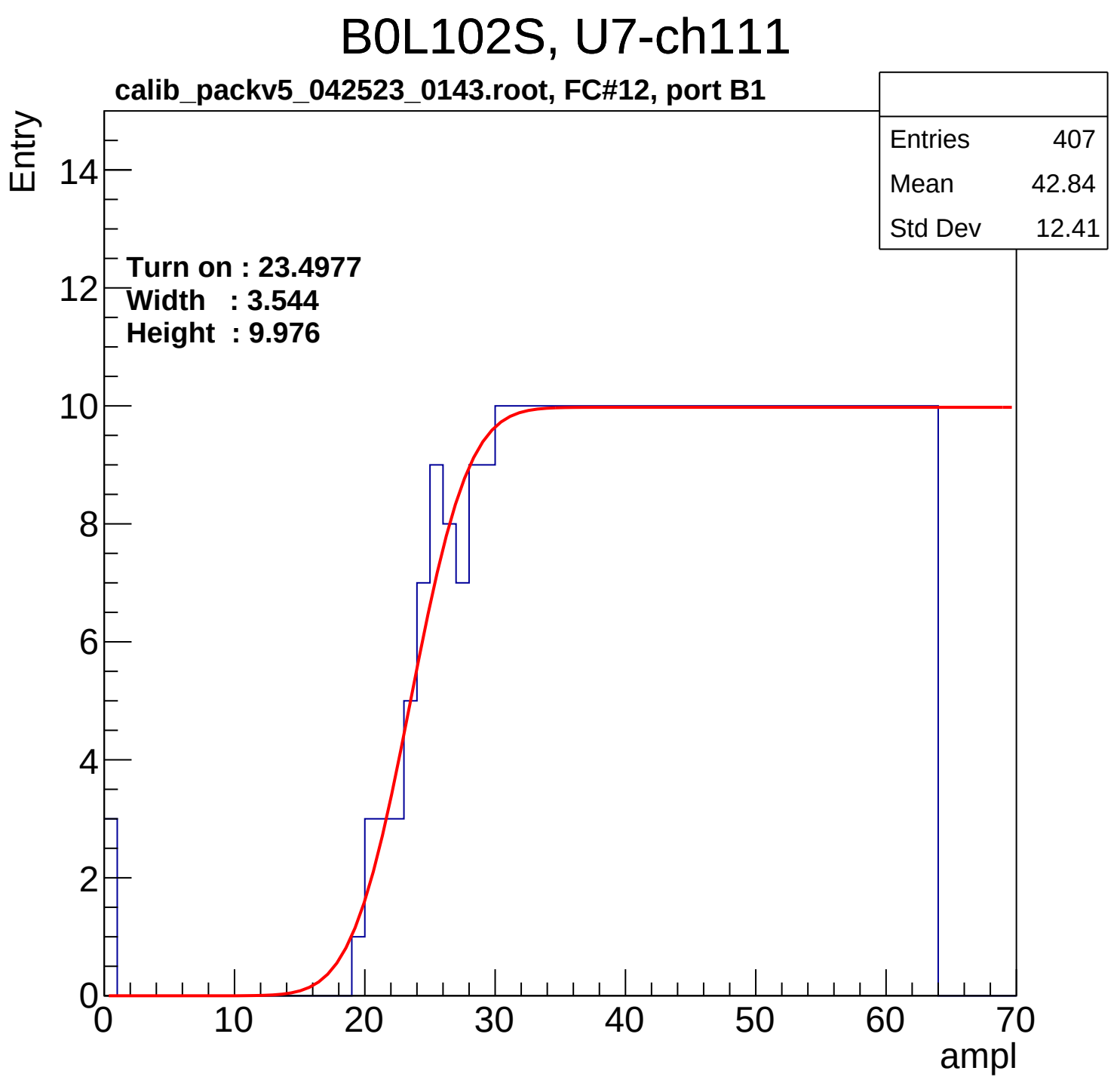
B0L102S, U7-ch111
calib_packv5_042523_0143.root, FC#12, port B1
Entries 407
Mean 42.84
Std Dev 12.41
Turn on : 23.4977
Width : 3.544
Height : 9.976
Entry
ampl
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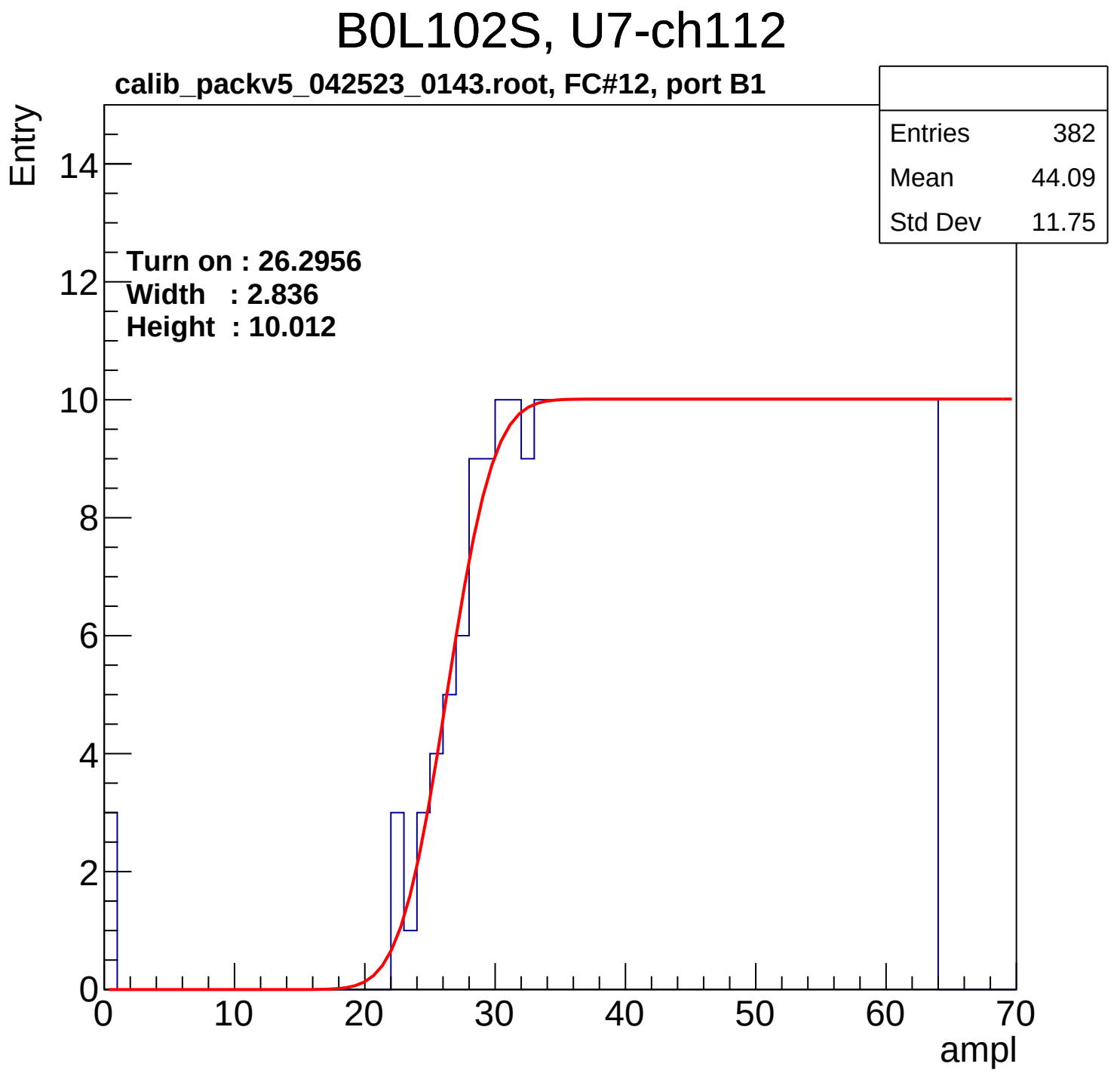
B0L102S, U7-ch112
calib_packv5_042523_0143.root, FC#12, port B1
Entries 382
Mean 44.09
Std Dev 11.75
Turn on : 26.2956
Width : 2.836
Height : 10.012
Entry
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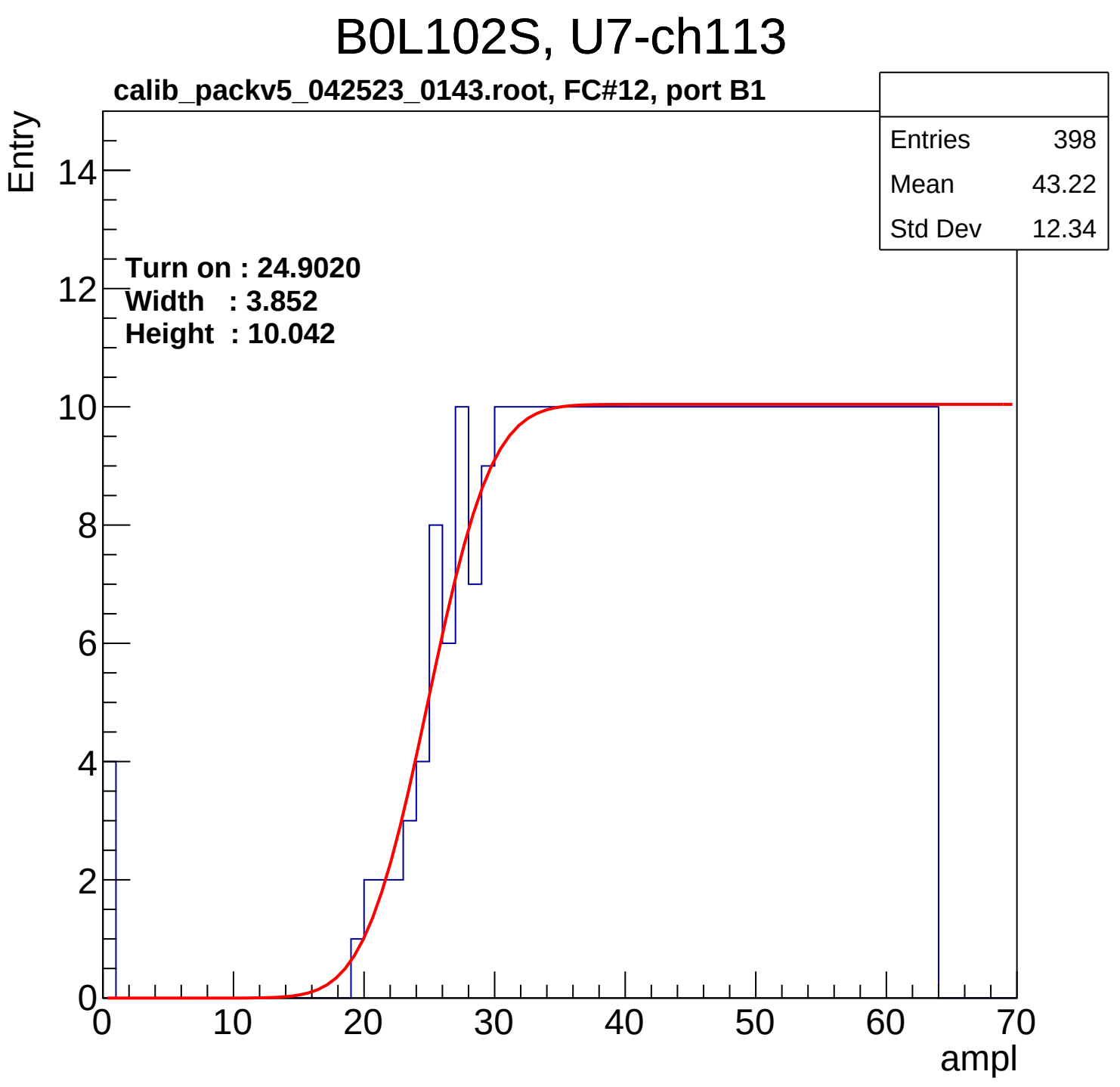
B0L102S, U7-ch113
calib_packv5_042523_0143.root, FC#12, port B1
Entries 398
Mean 43.22
Std Dev 12.34
Turn on : 24.9020
Width : 3.852
Height : 10.042
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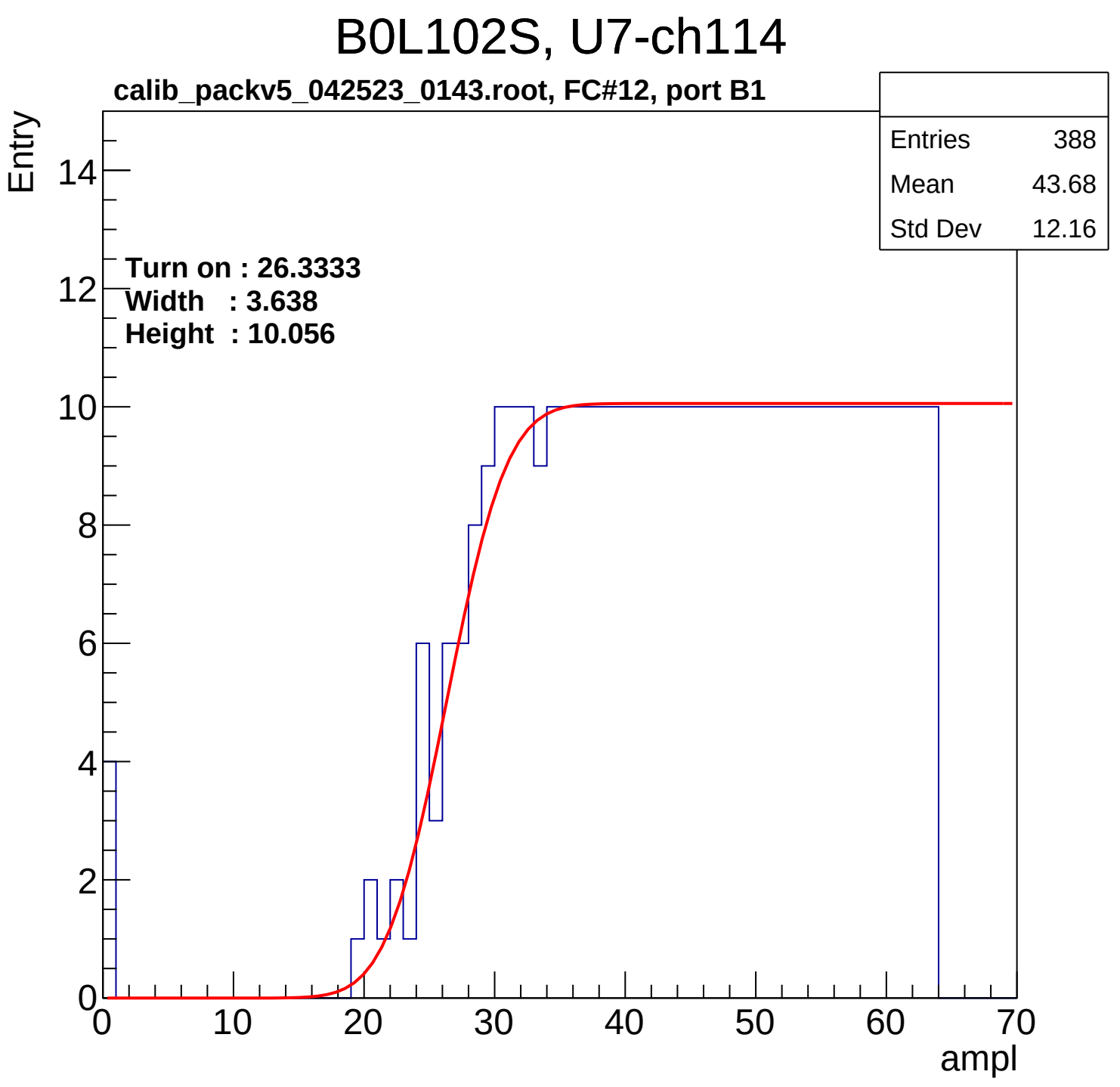
B0L102S, U7-ch114
calib_packv5_042523_0143.root, FC#12, port B1
Entries 388
Mean 43.68
Std Dev 12.16
Turn on : 26.3333
Width : 3.638
Height : 10.056
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ampl
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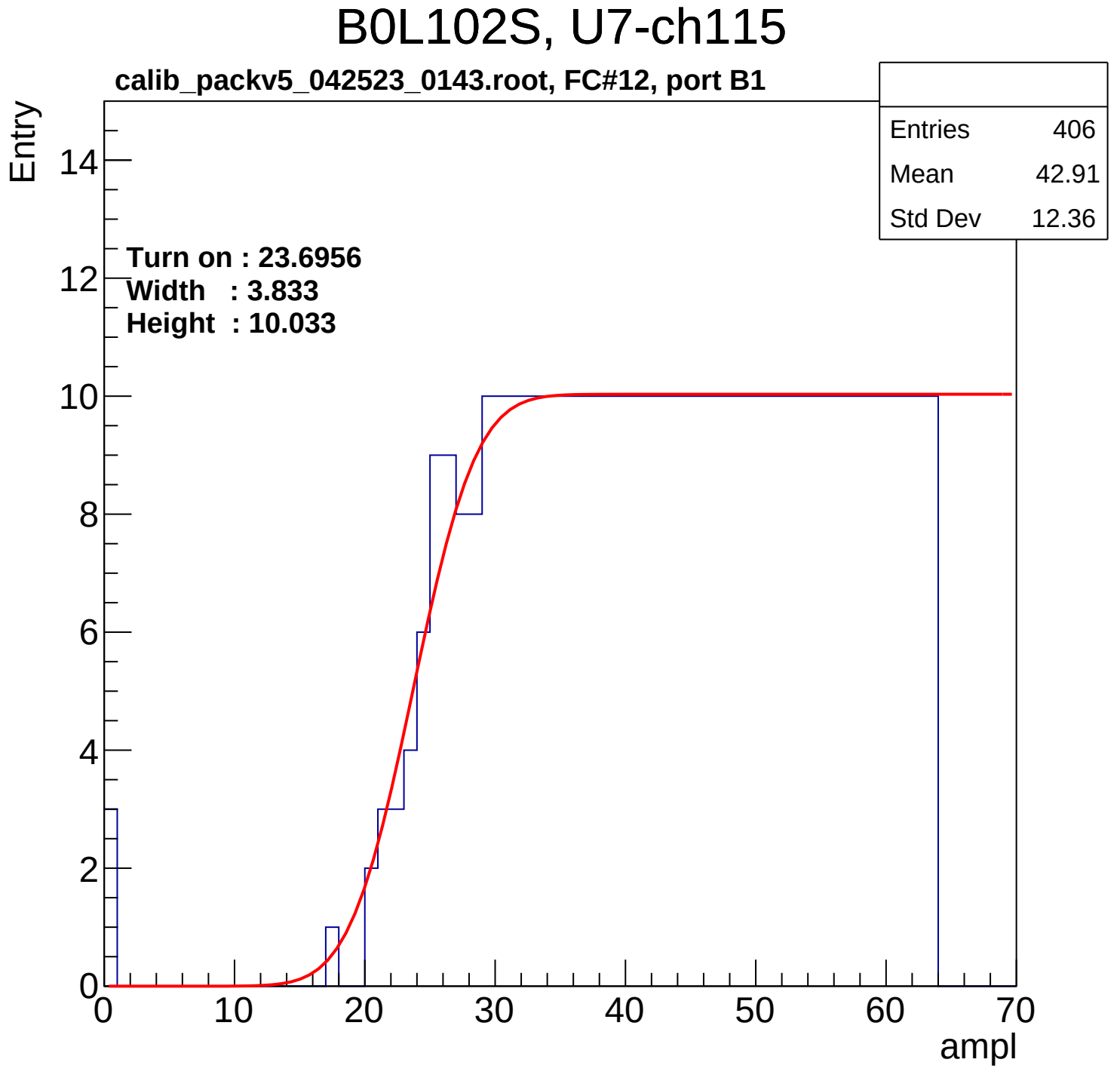
B0L102S, U7-ch115
calib_packv5_042523_0143.root, FC#12, port B1
Entries 406
Mean 42.91
Std Dev 12.36
Turn on : 23.6956
Width : 3.833
Height : 10.033
Entry
ampl
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4
6
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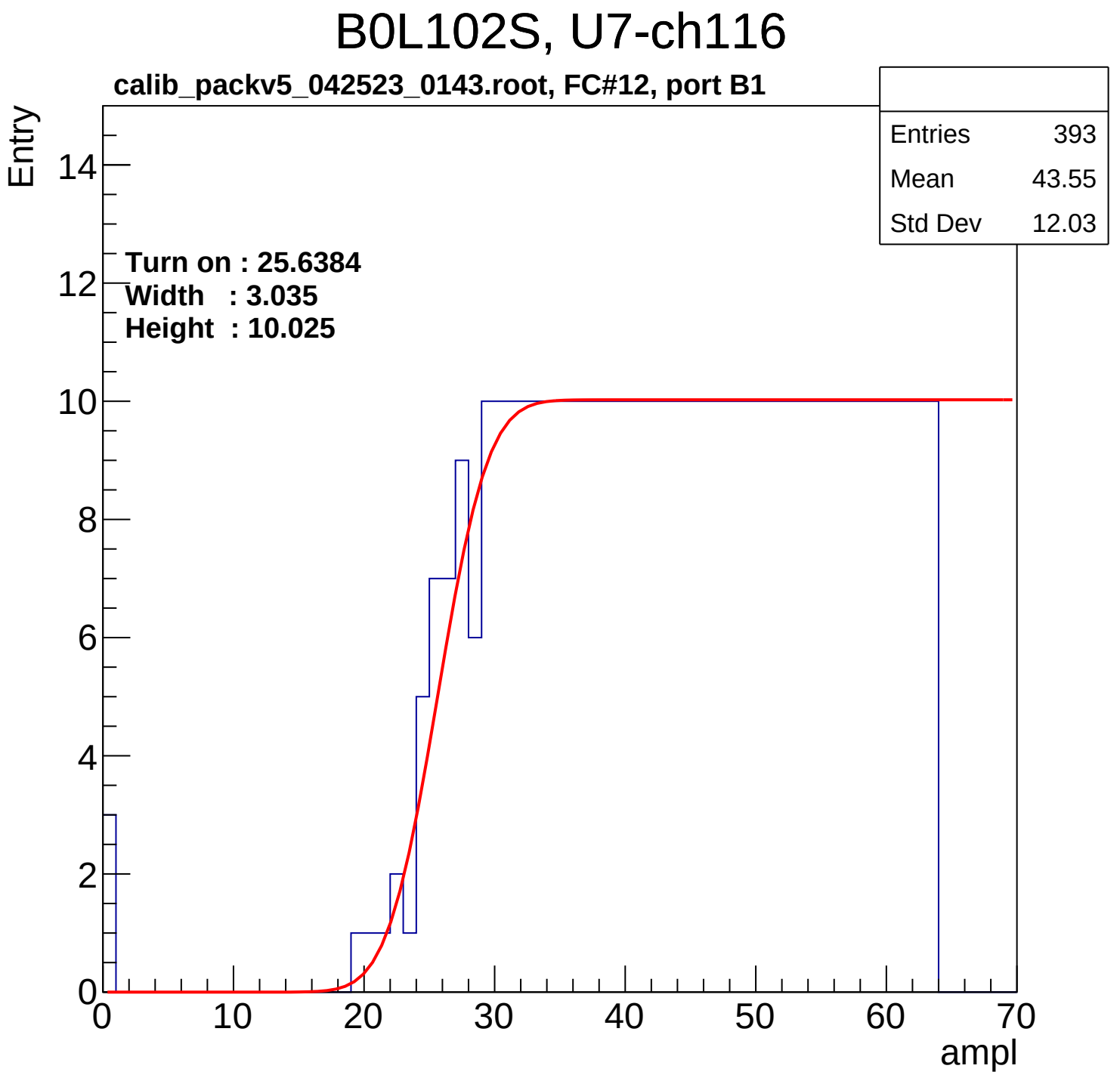
B0L102S, U7-ch116
calib_packv5_042523_0143.root, FC#12, port B1
Entries 393
Mean 43.55
Std Dev 12.03
Turn on : 25.6384
Width : 3.035
Height : 10.025
Entry
ampl
0
2
4
6
8
10
12
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0
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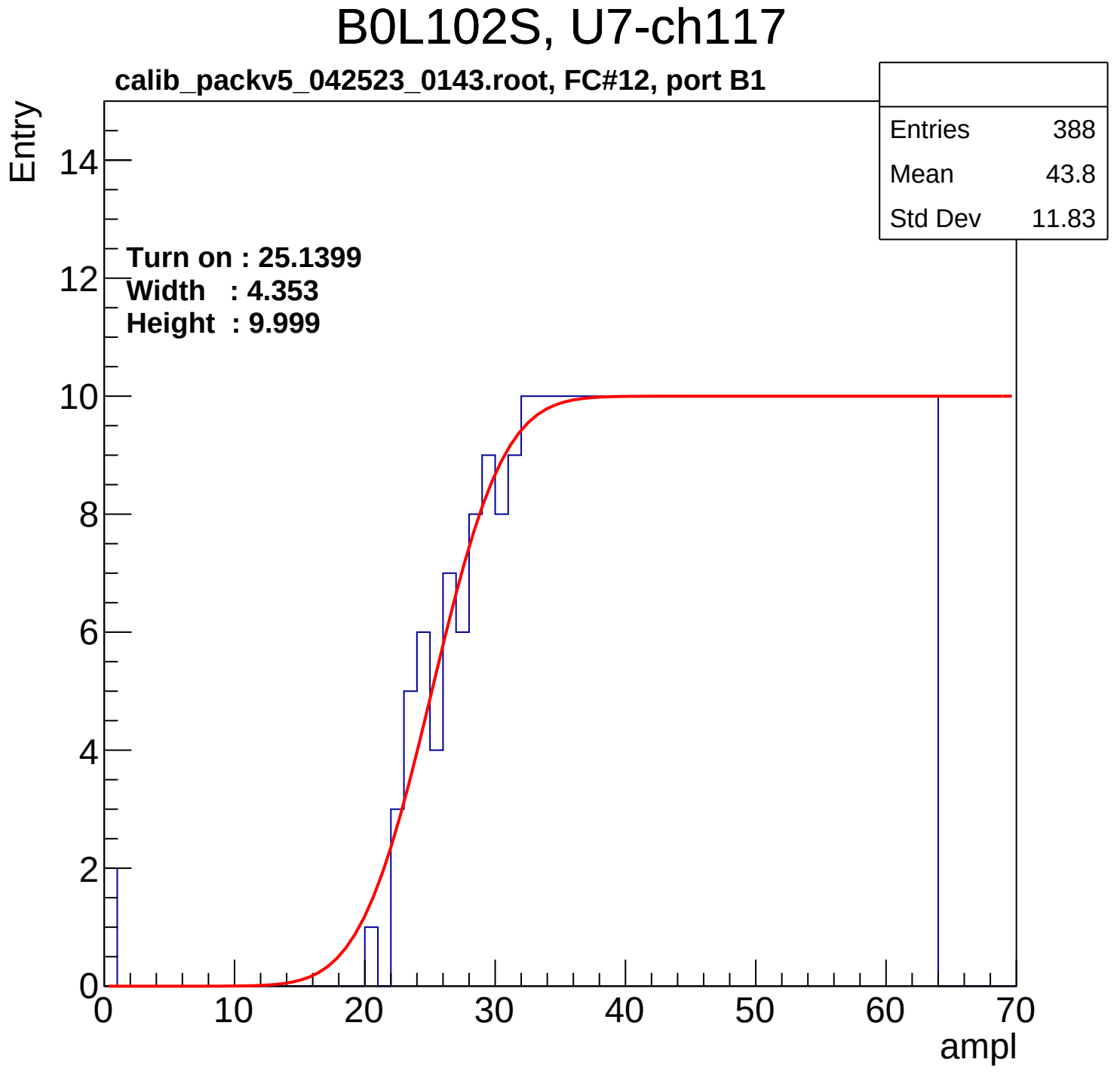
B0L102S, U7-ch117
calib_packv5_042523_0143.root, FC#12, port B1
Entries 388
Mean 43.8
Std Dev 11.83
Turn on : 25.1399
Width : 4.353
Height : 9.999
Entry
ampl
0
2
4
6
8
10
12
14
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10
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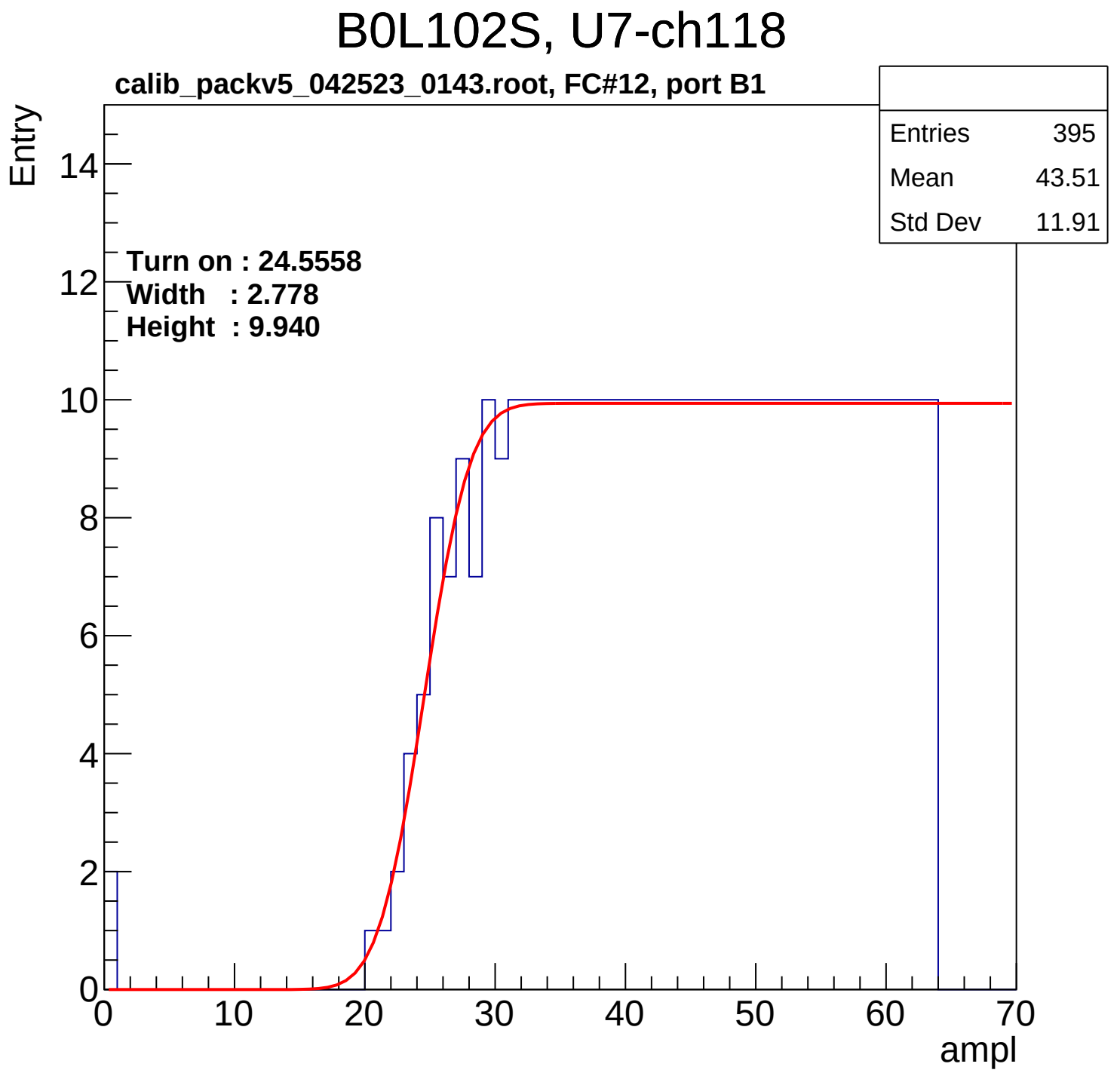
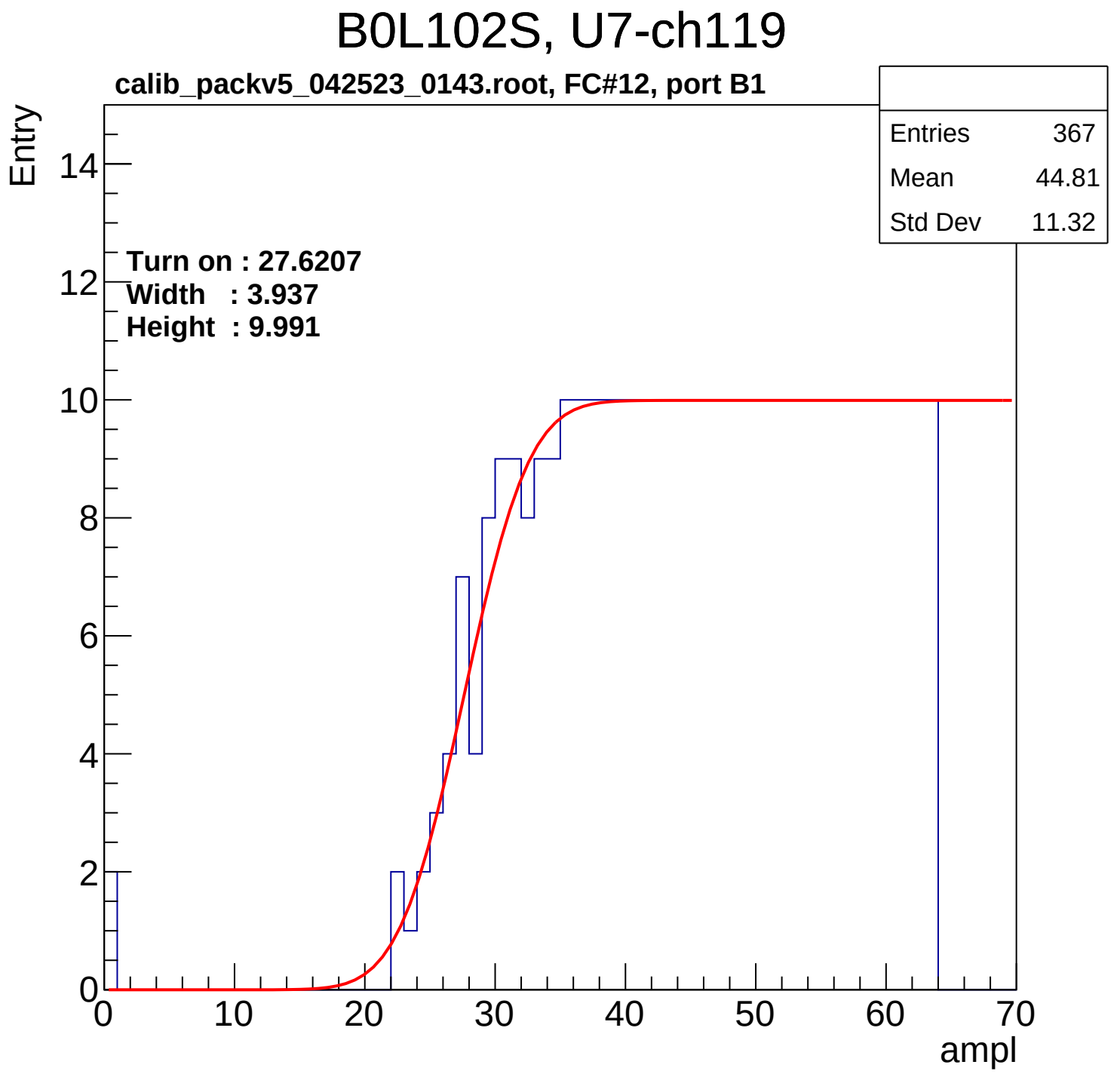
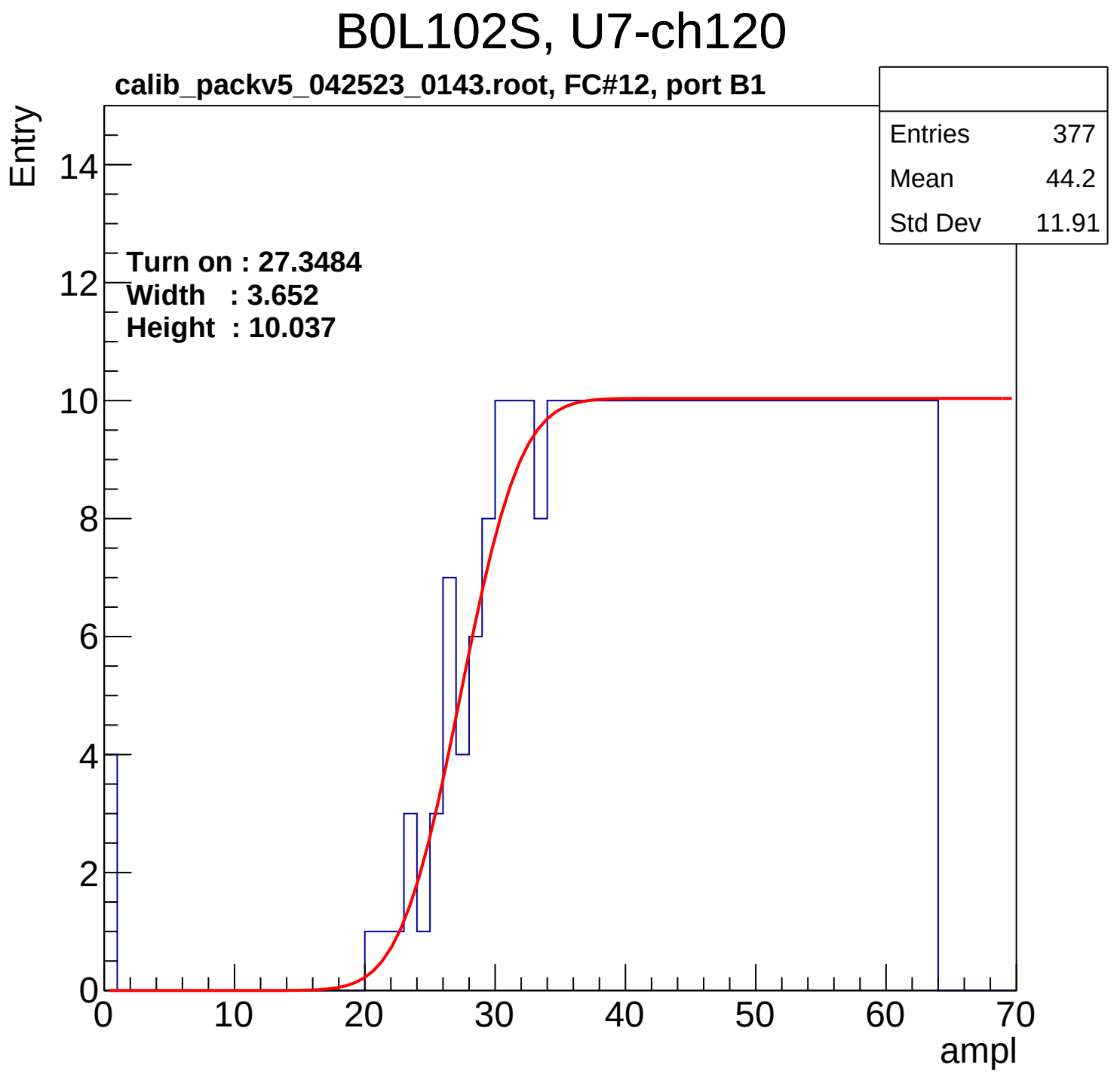
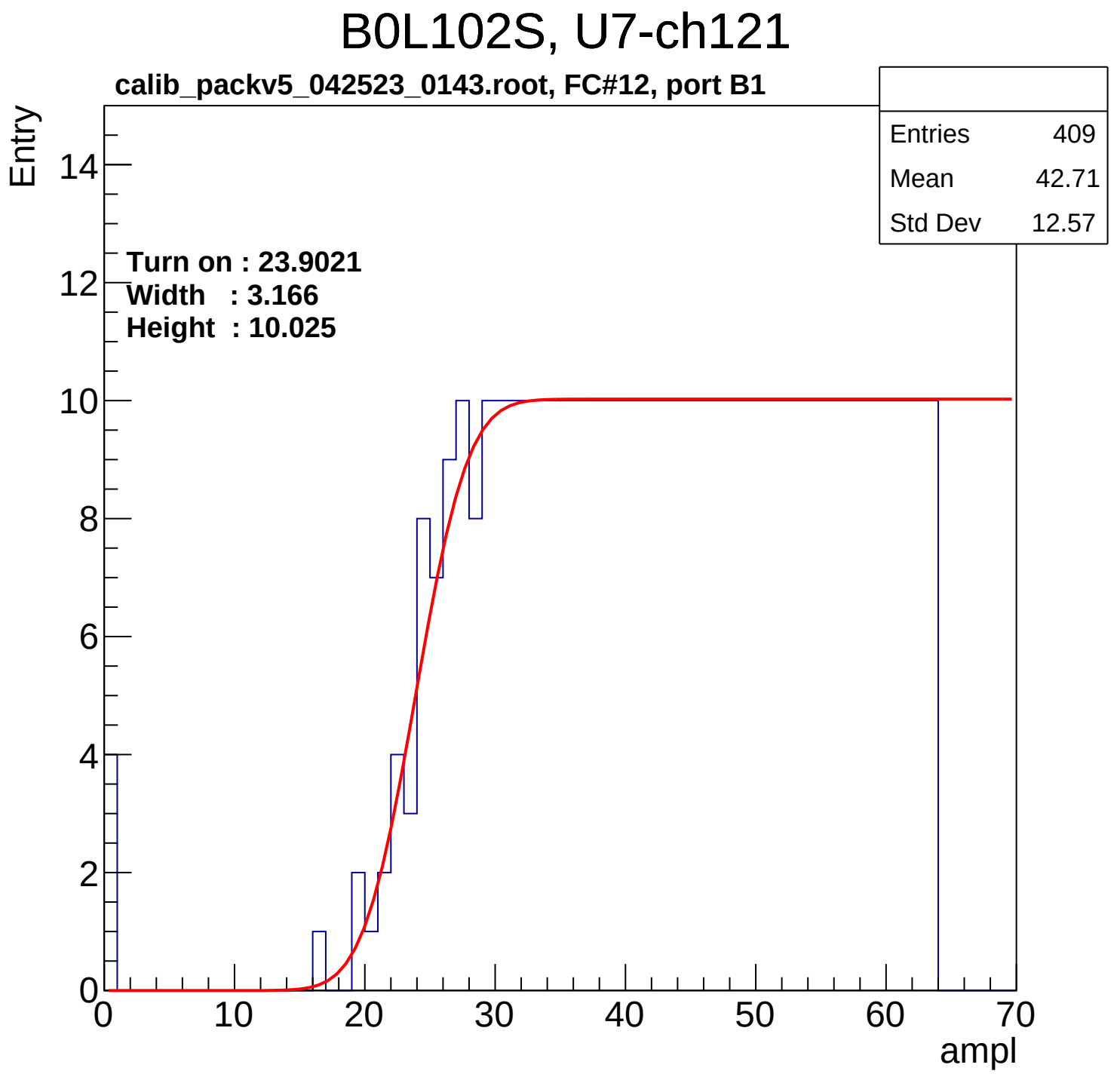
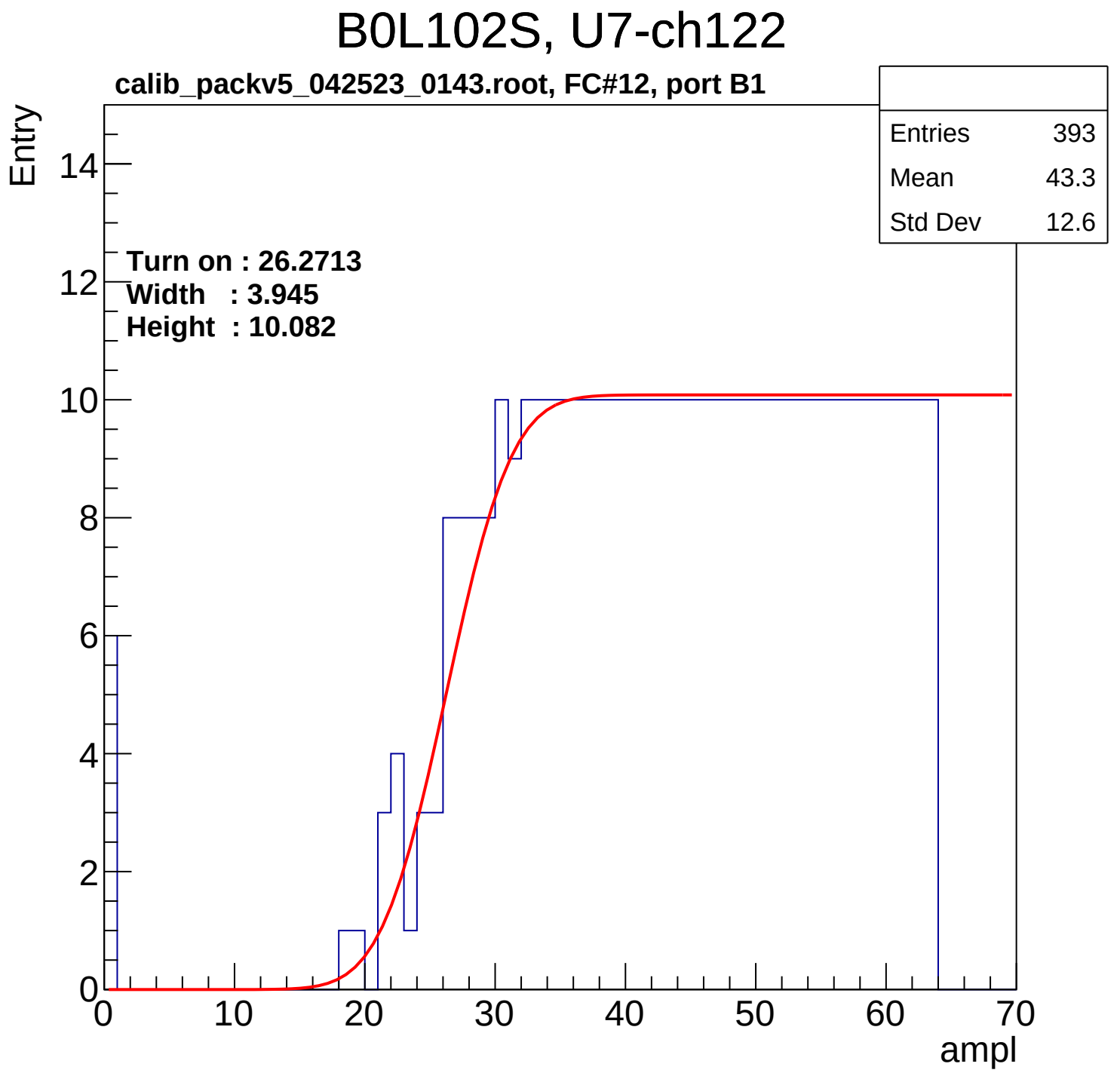

B0L102S, U7-ch118
calib_packv5_042523_0143.root, FC#12, port B1
Entries 395
Mean 43.51
Std Dev 11.91
Turn on : 24.5558
Width : 2.778
Height : 9.940
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L102S, U7-ch119
calib_packv5_042523_0143.root, FC#12, port B1
Entries 367
Mean 44.81
Std Dev 11.32
Turn on : 27.6207
Width : 3.937
Height : 9.991
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L102S, U7-ch120
calib_packv5_042523_0143.root, FC#12, port B1
Entries 377
Mean 44.2
Std Dev 11.91
Turn on : 27.3484
Width : 3.652
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L102S, U7-ch121
calib_packv5_042523_0143.root, FC#12, port B1
Entries 409
Mean 42.71
Std Dev 12.57
Turn on : 23.9021
Width : 3.166
Height : 10.025
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L102S, U7-ch122
calib_packv5_042523_0143.root, FC#12, port B1
Entries 393
Mean 43.3
Std Dev 12.6
Turn on : 26.2713
Width : 3.945
Height : 10.082
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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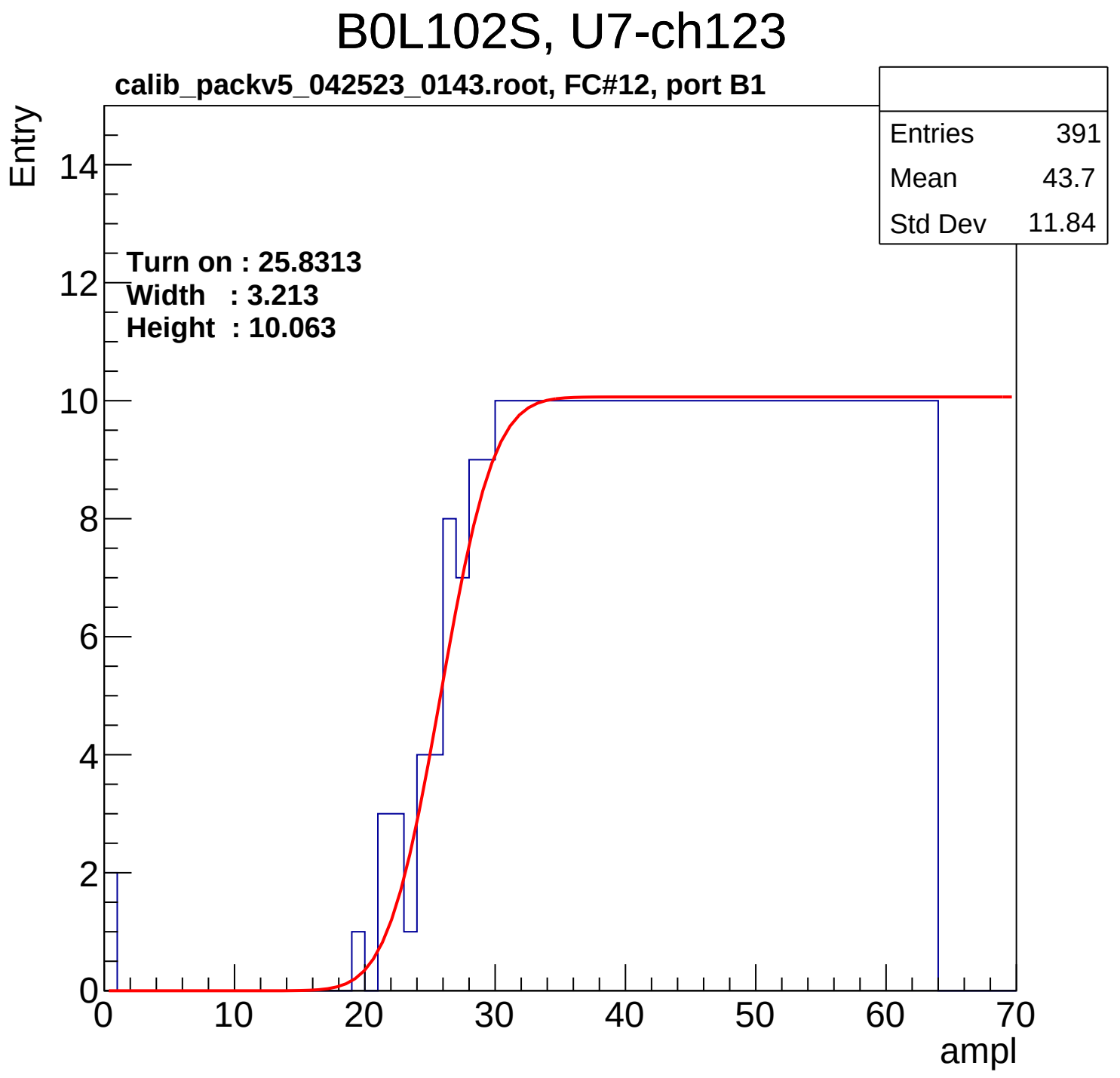
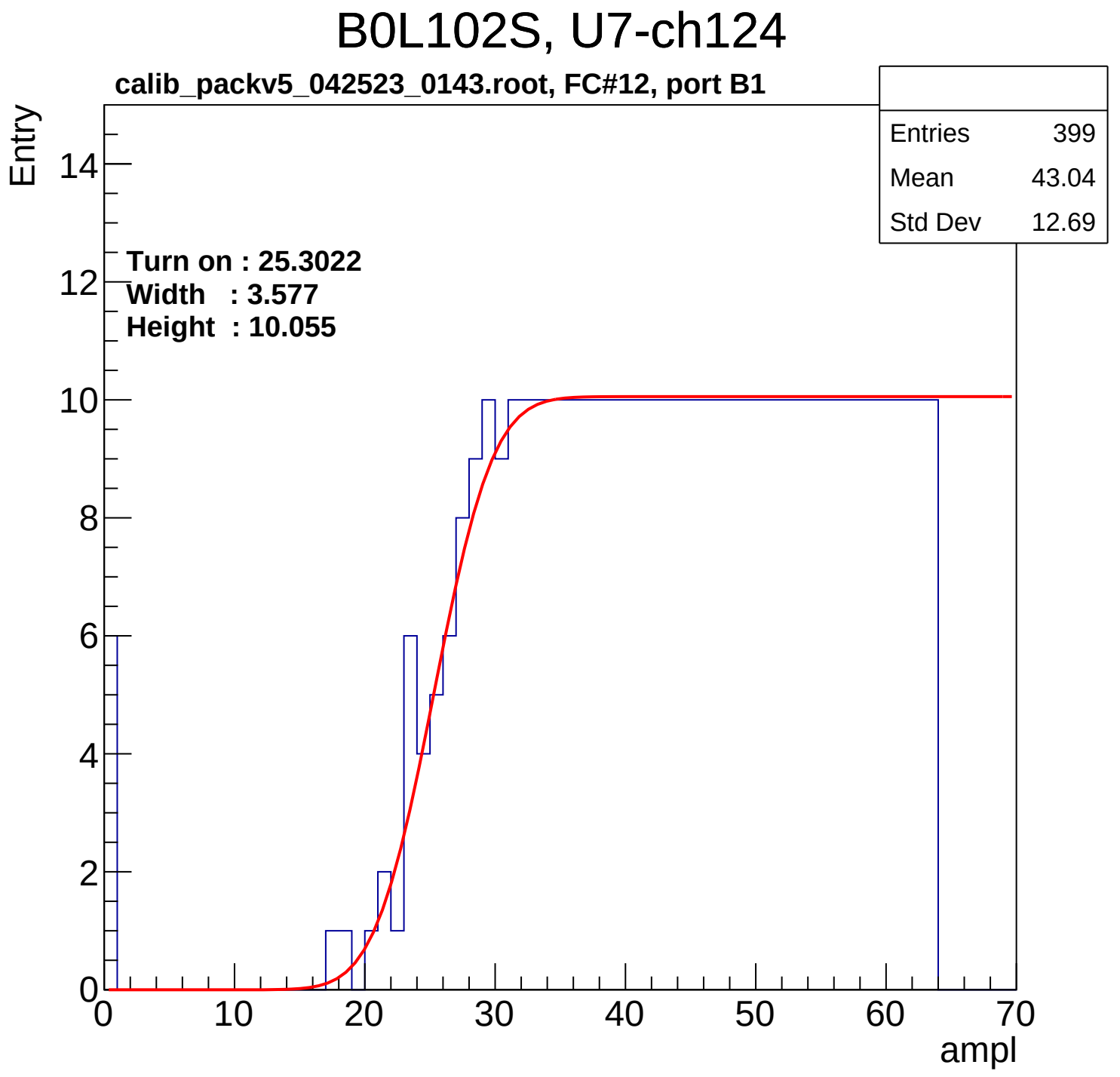

B0L102S, U7-ch123
calib_packv5_042523_0143.root, FC#12, port B1
Entries 391
Mean 43.7
Std Dev 11.84
Turn on : 25.8313
Width : 3.213
Height : 10.063
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L102S, U7-ch124
calib_packv5_042523_0143.root, FC#12, port B1
Entries 399
Mean 43.04
Std Dev 12.69
Turn on : 25.3022
Width : 3.577
Height : 10.055
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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40
50
60
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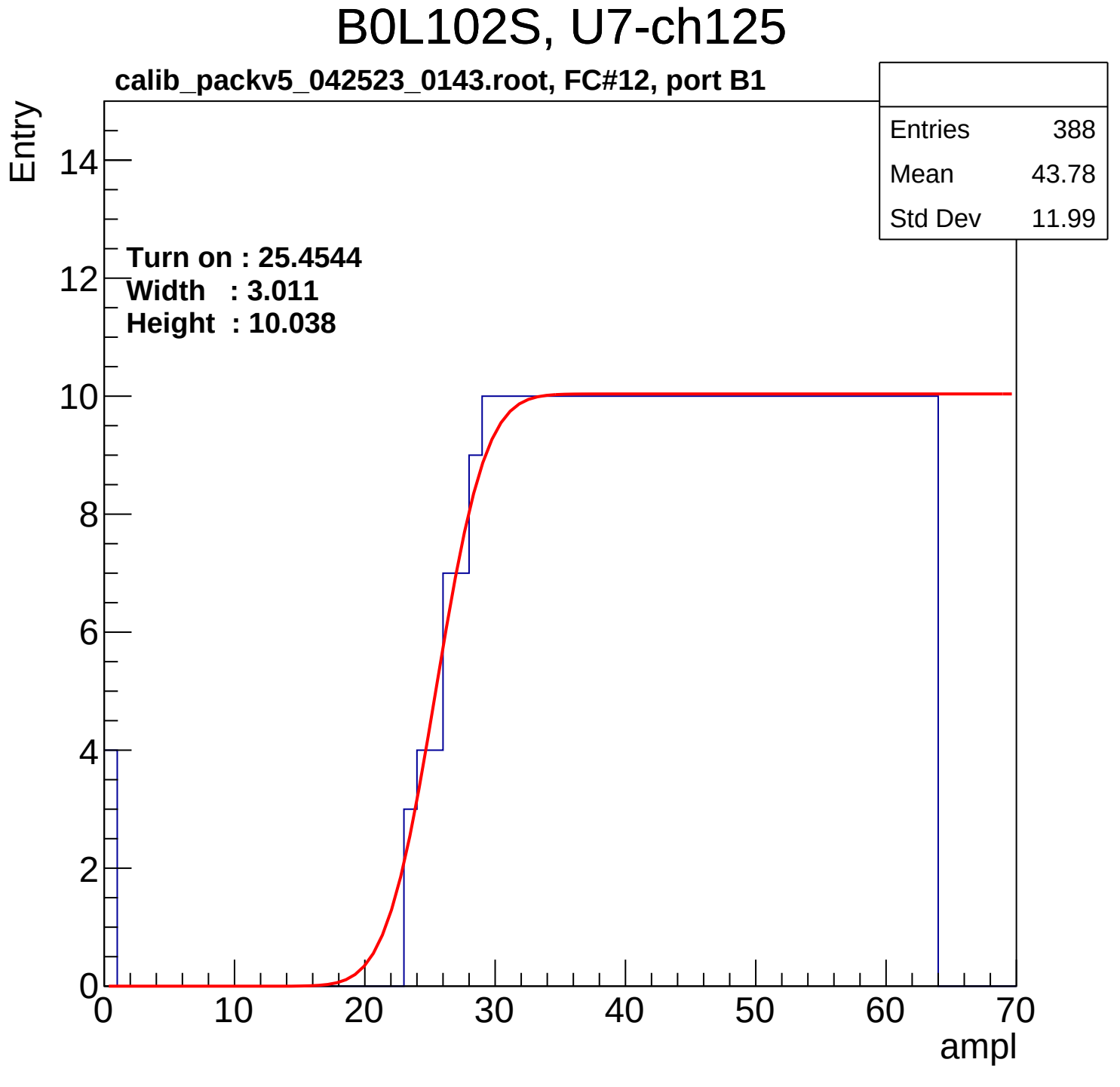
B0L102S, U7-ch125
calib_packv5_042523_0143.root, FC#12, port B1
Entries 388
Mean 43.78
Std Dev 11.99
Turn on : 25.4544
Width : 3.011
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
14
0
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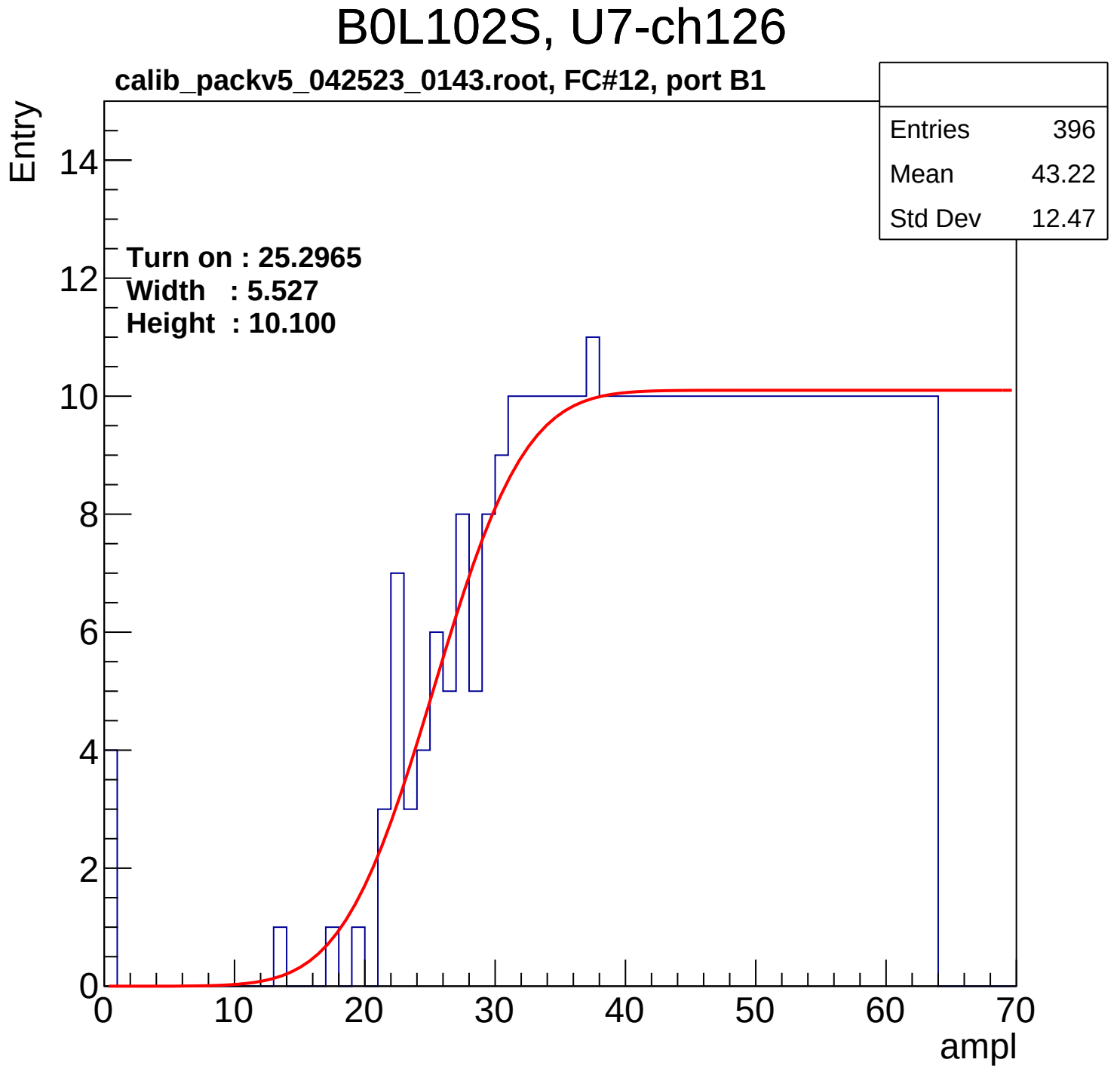
20
30
40
50
60
70


B0L102S, U7-ch126
calib_packv5_042523_0143.root, FC#12, port B1
Entries 396
Mean 43.22
Std Dev 12.47
Turn on : 25.2965
Width : 5.527
Height : 10.100
Entry
ampl
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2
4
6
8
10
12
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0
10
20
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60
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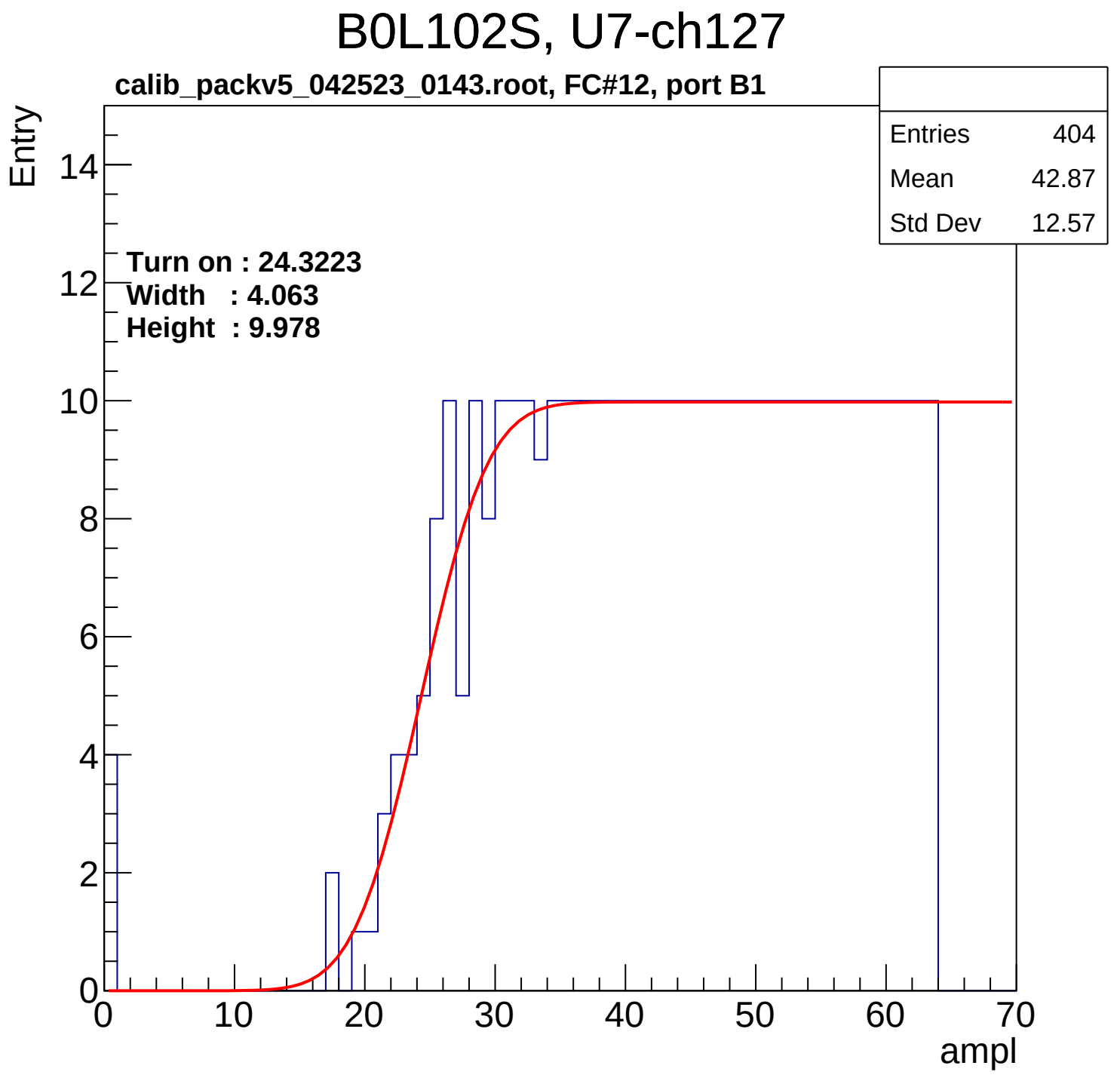
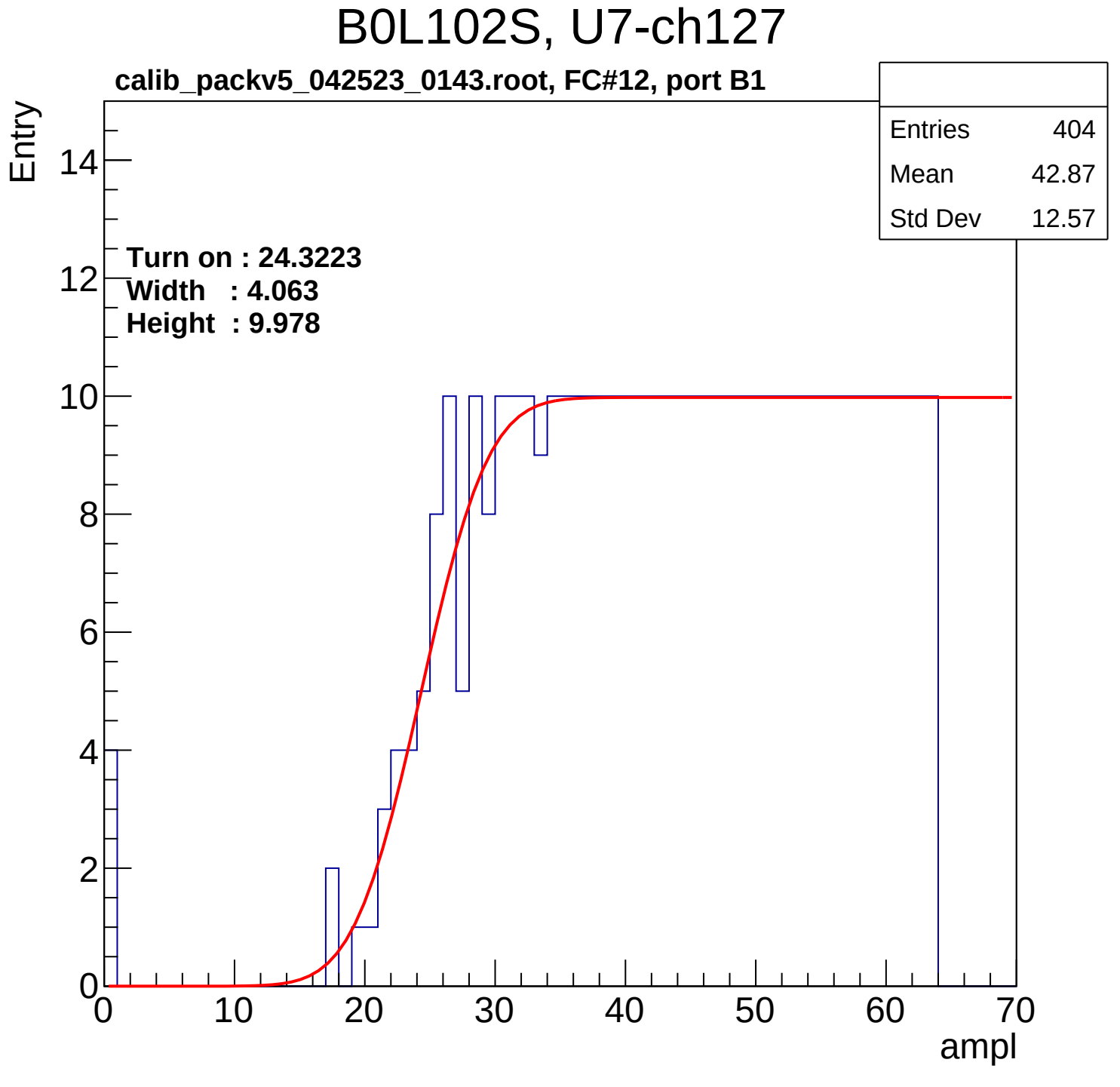

B0L102S, U7-ch127
calib_packv5_042523_0143.root, FC#12, port B1
Entries 404
Mean 42.87
Std Dev 12.57
Turn on : 24.3223
Width : 4.063
Height : 9.978
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L102S, U7-ch127
calib_packv5_042523_0143.root, FC#12, port B1
Entries 404
Mean 42.87
Std Dev 12.57
Turn on : 24.3223
Width : 4.063
Height : 9.978
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70