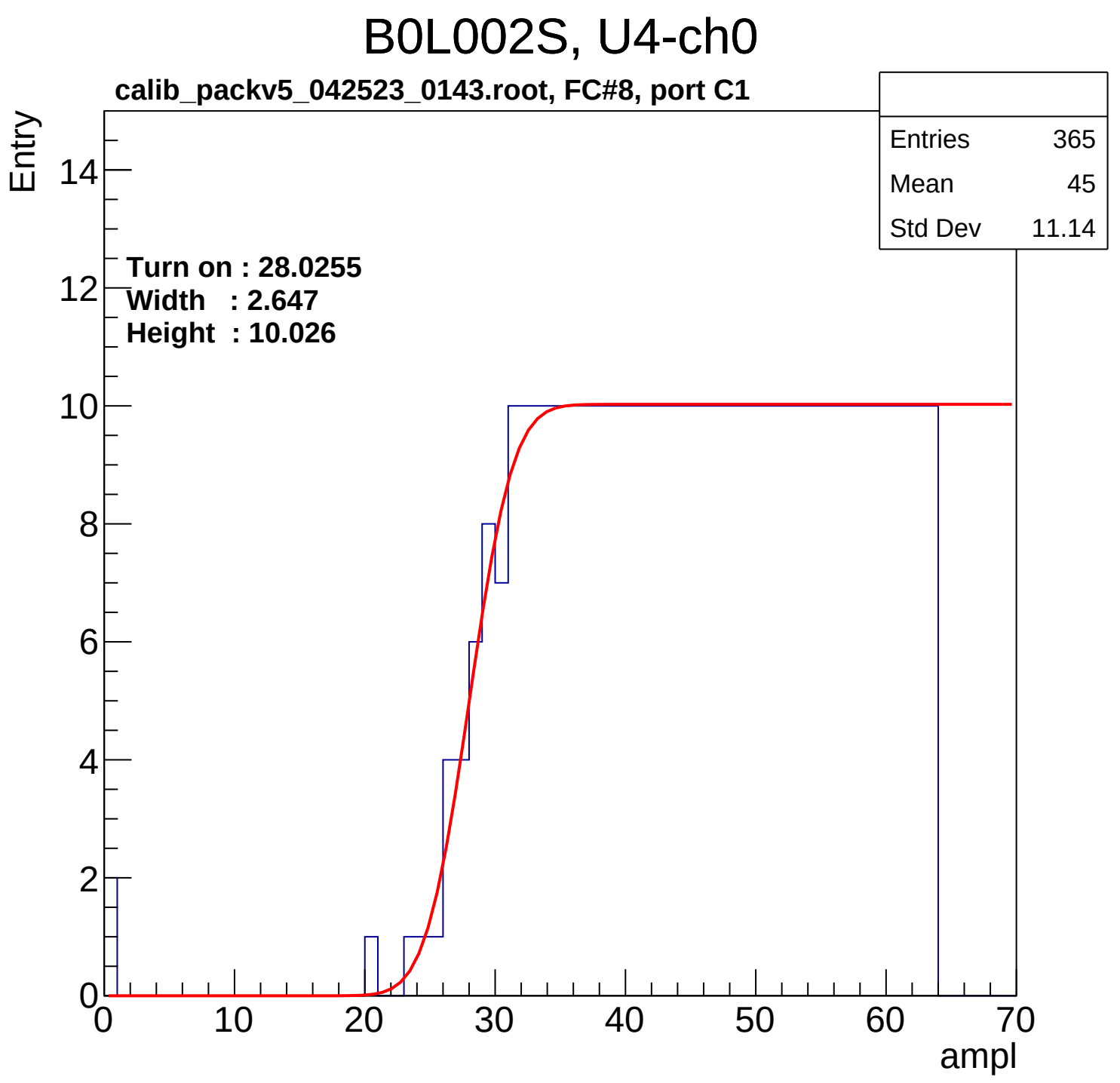
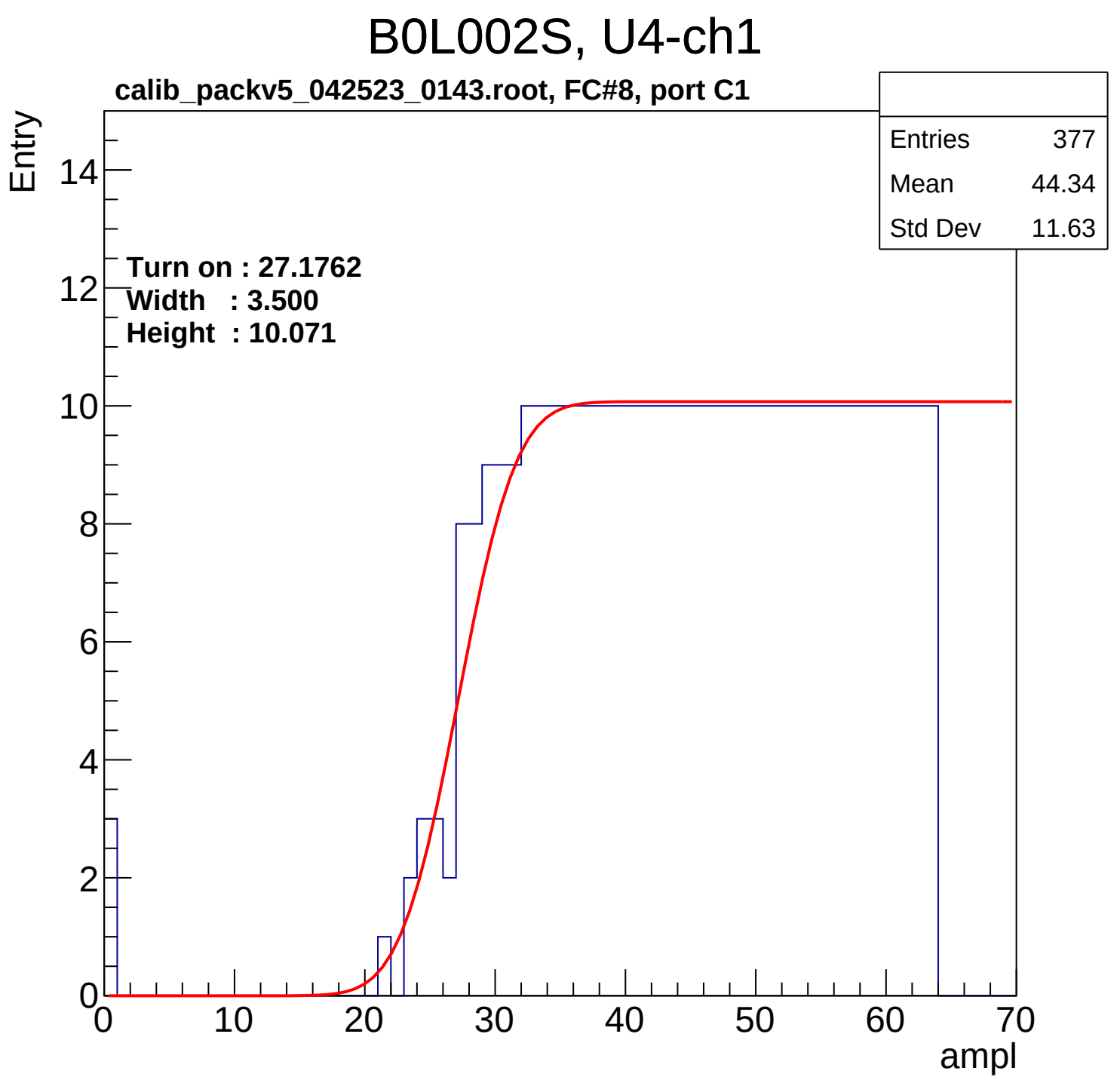
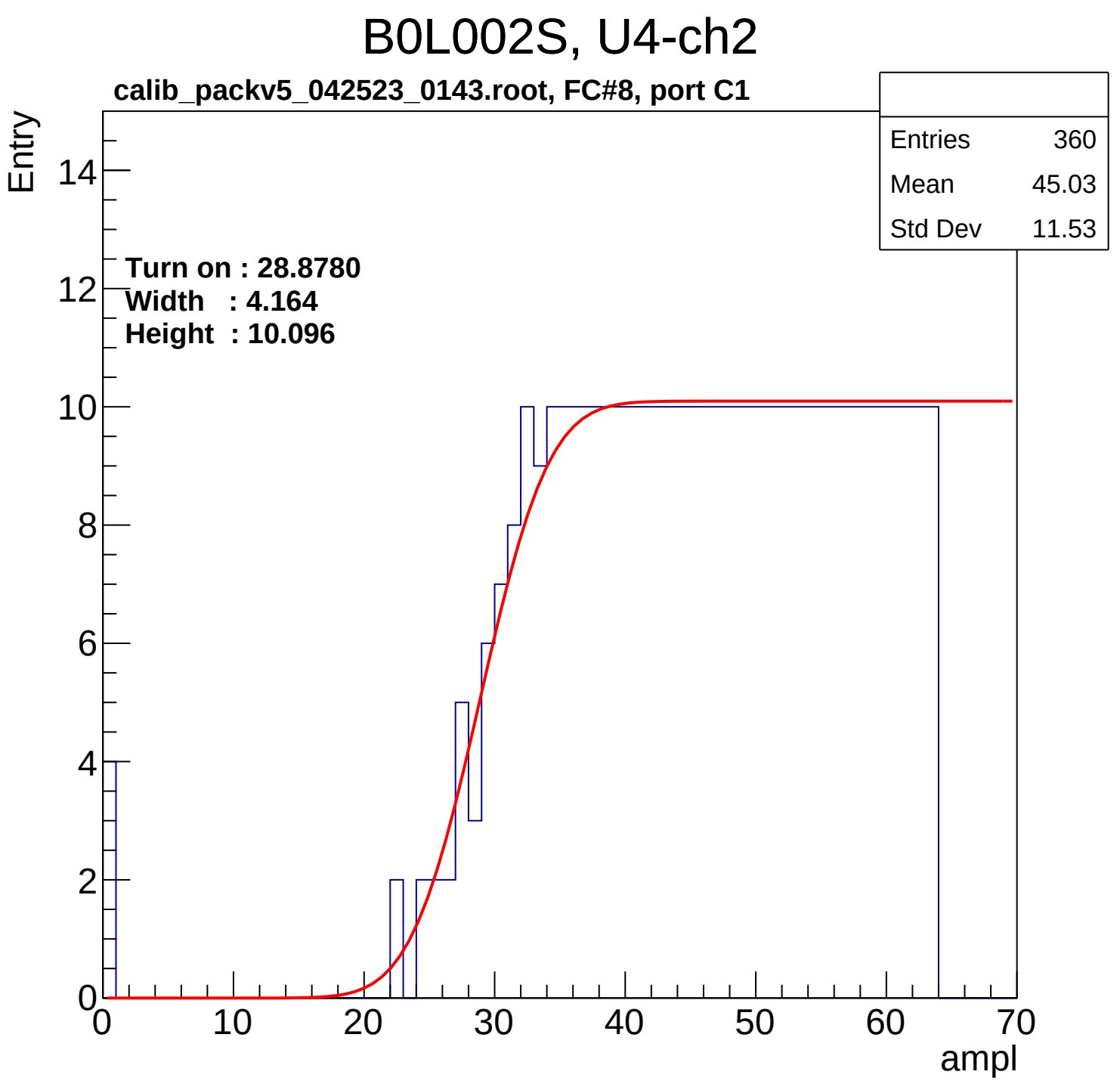
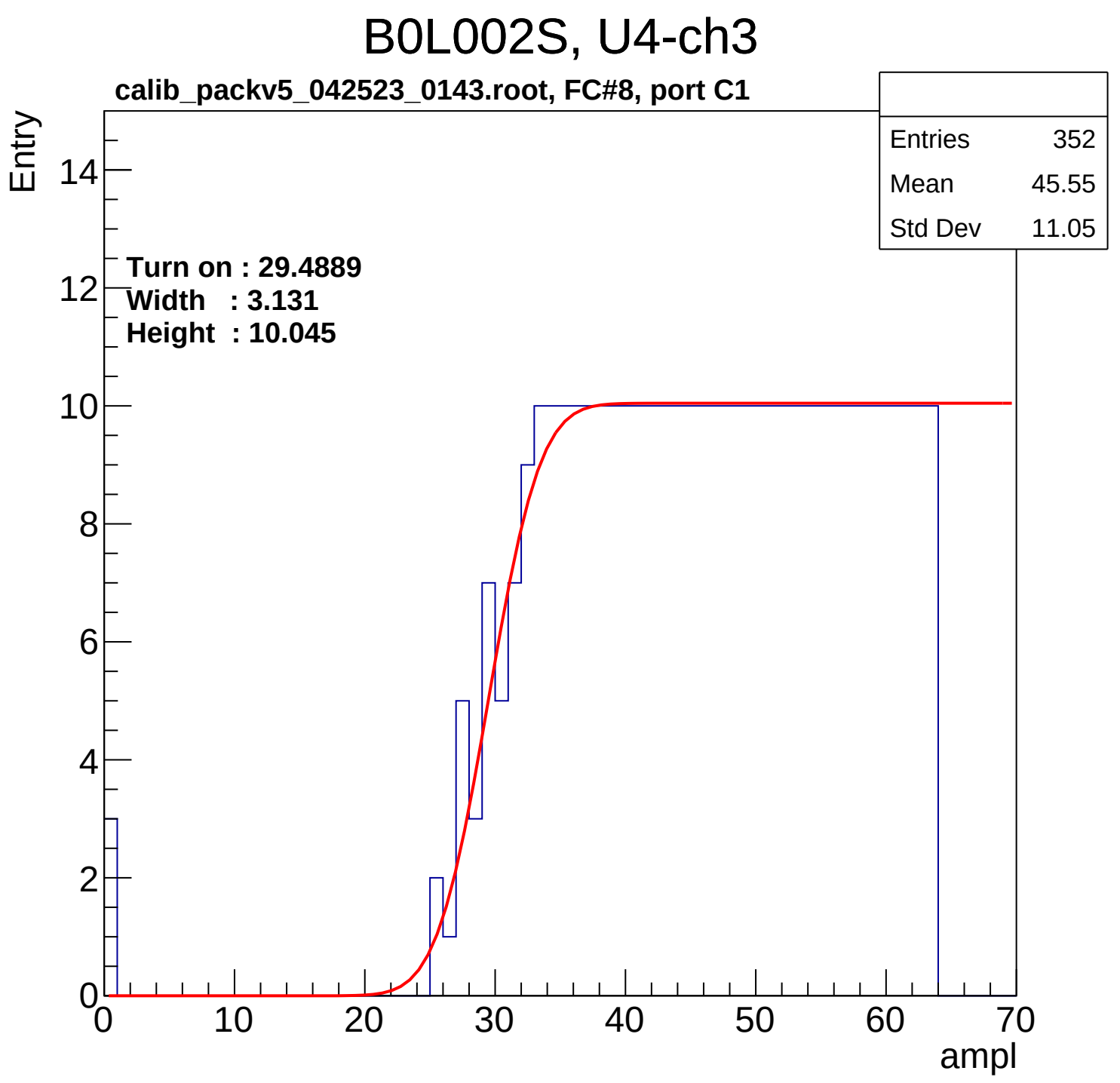
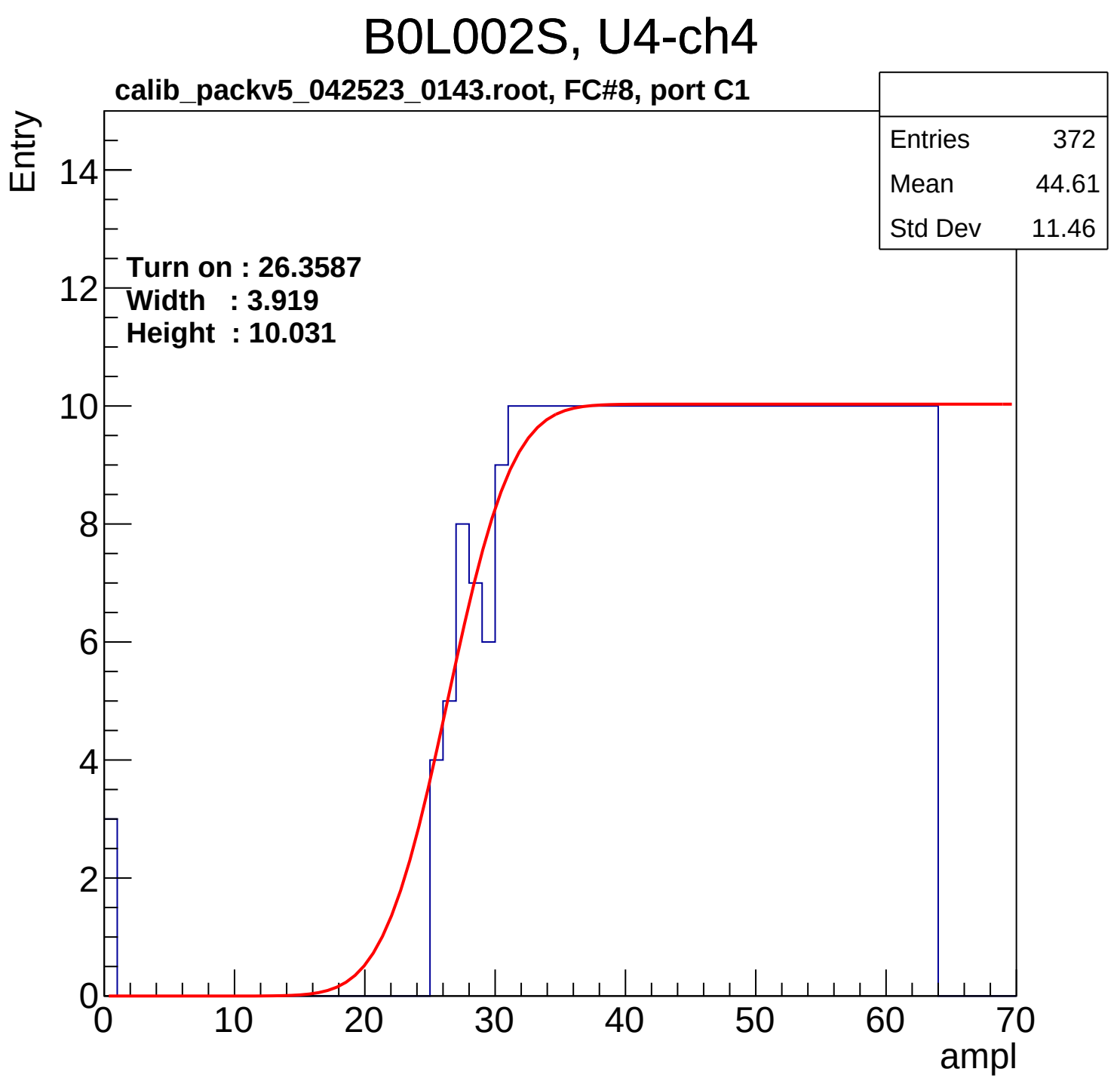
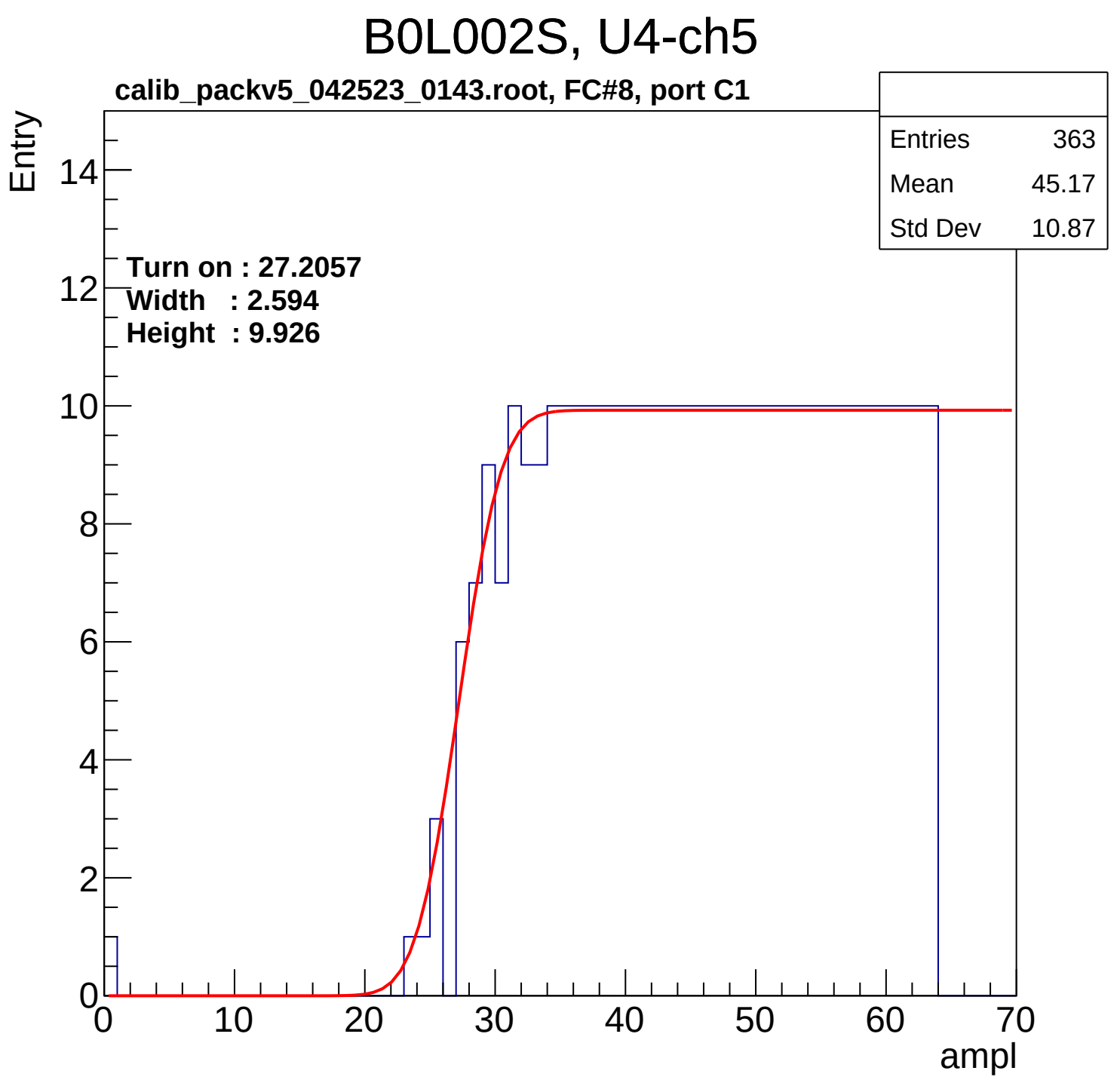

B0L002S, U4-ch0
calib_packv5_042523_0143.root, FC#8, port C1
Entries 365
Mean 45
Std Dev 11.14
Turn on : 28.0255
Width : 2.647
Height : 10.026
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

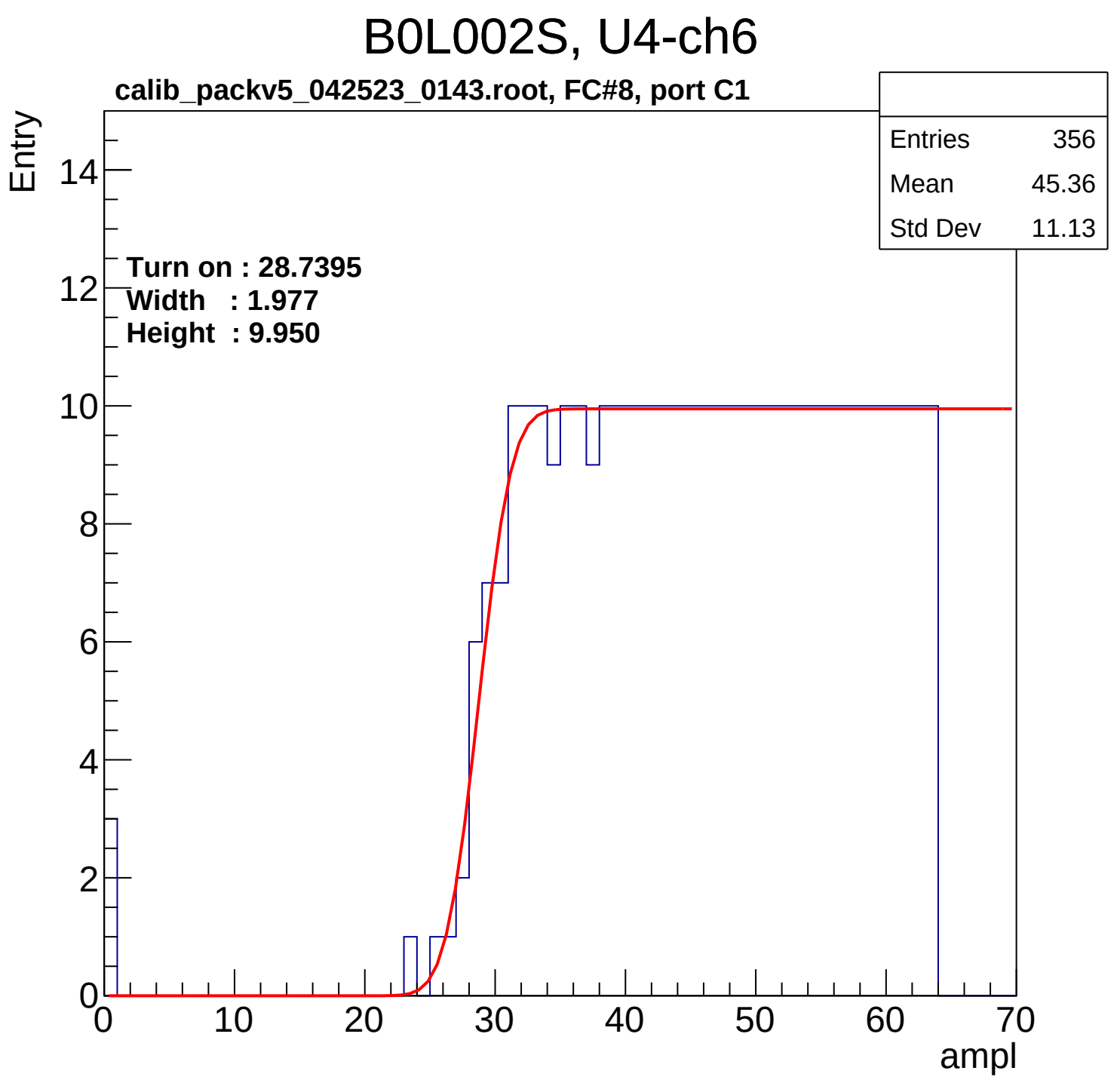

B0L002S, U4-ch1
calib_packv5_042523_0143.root, FC#8, port C1
Entries 377
Mean 44.34
Std Dev 11.63
Turn on : 27.1762
Width : 3.500
Height : 10.071
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

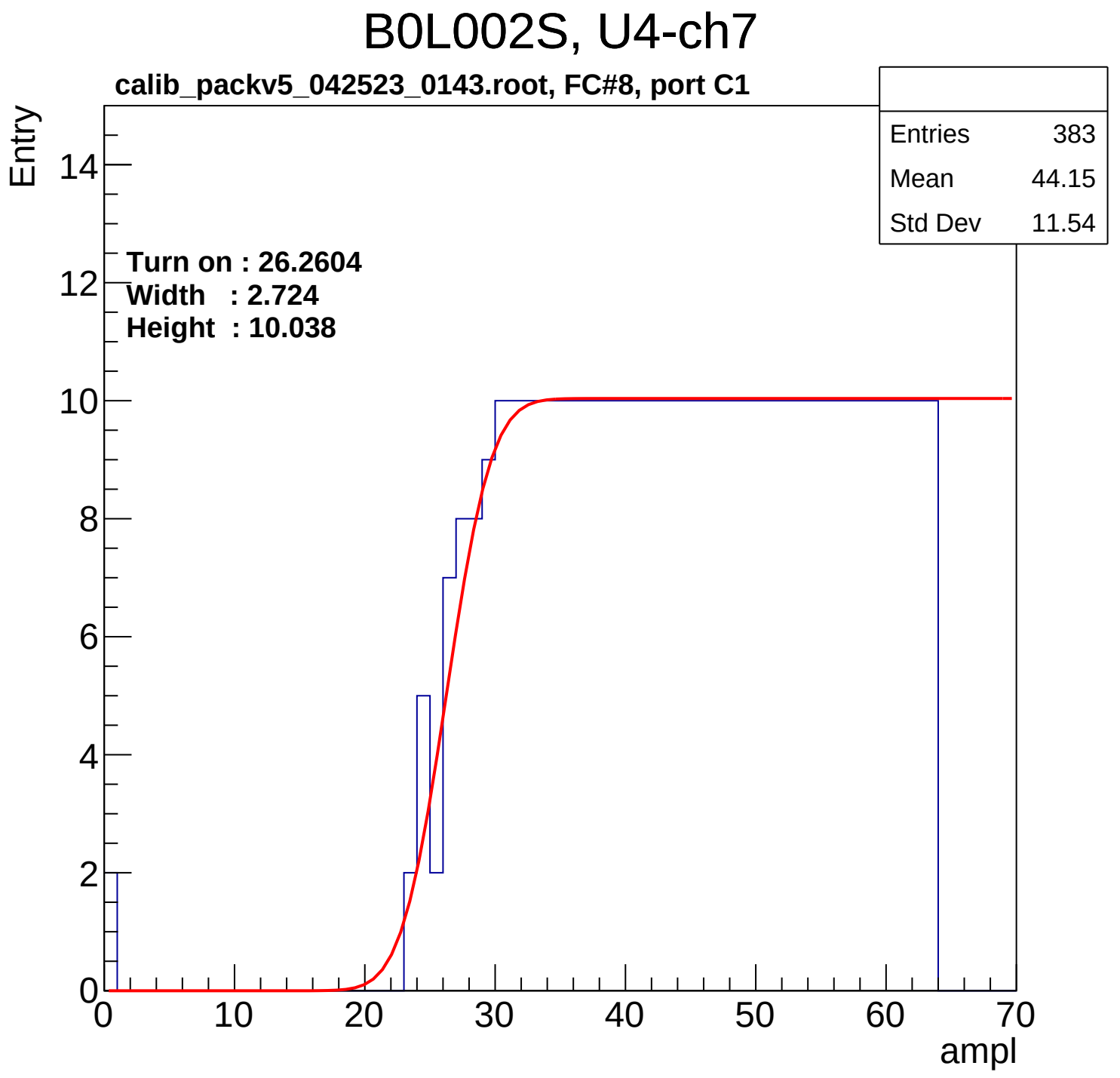

B0L002S, U4-ch2
calib_packv5_042523_0143.root, FC#8, port C1
Entries 360
Mean 45.03
Std Dev 11.53
Turn on : 28.8780
Width : 4.164
Height : 10.096
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

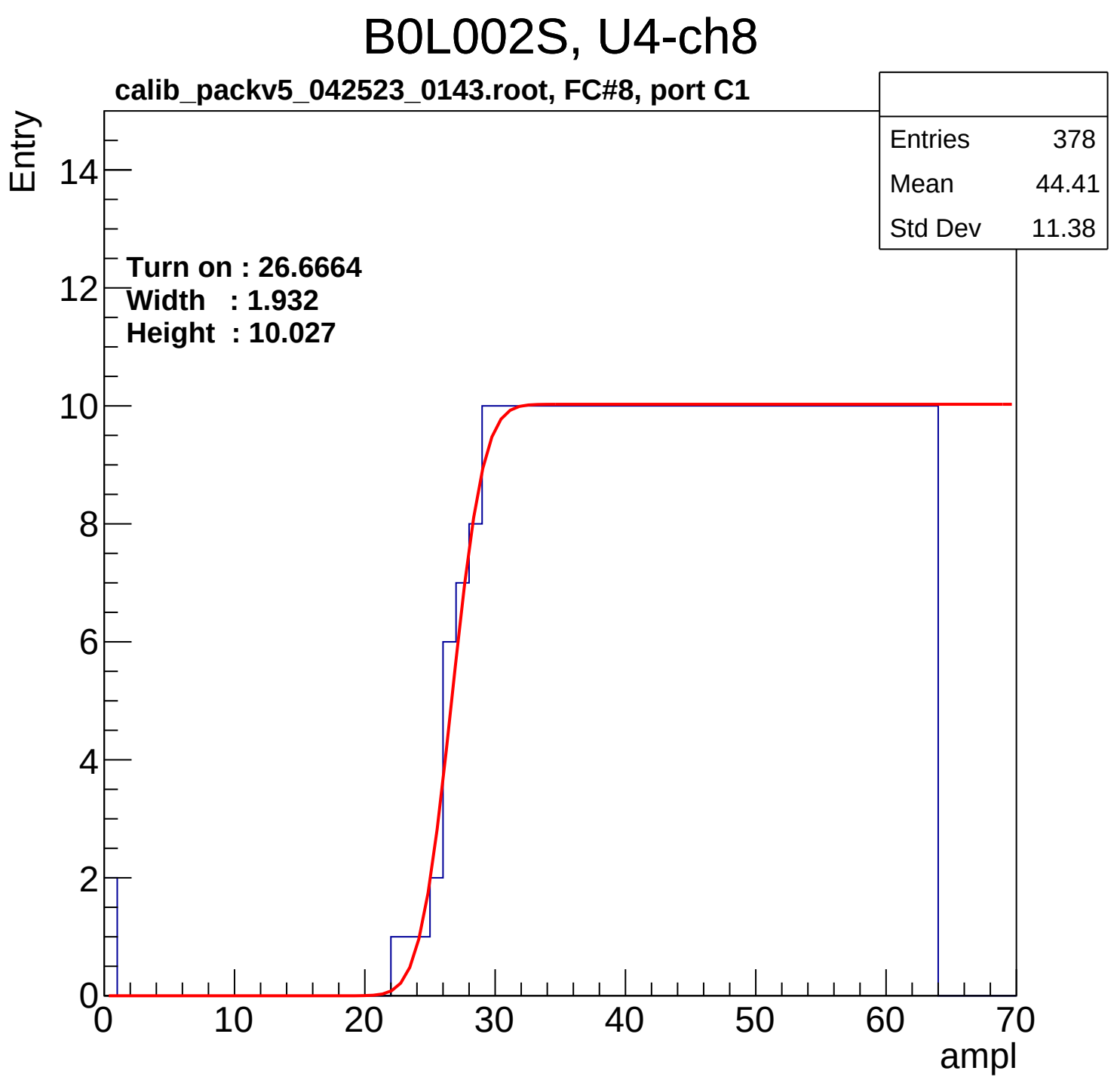

B0L002S, U4-ch3
calib_packv5_042523_0143.root, FC#8, port C1
Entries 352
Mean 45.55
Std Dev 11.05
Turn on : 29.4889
Width : 3.131
Height : 10.045
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

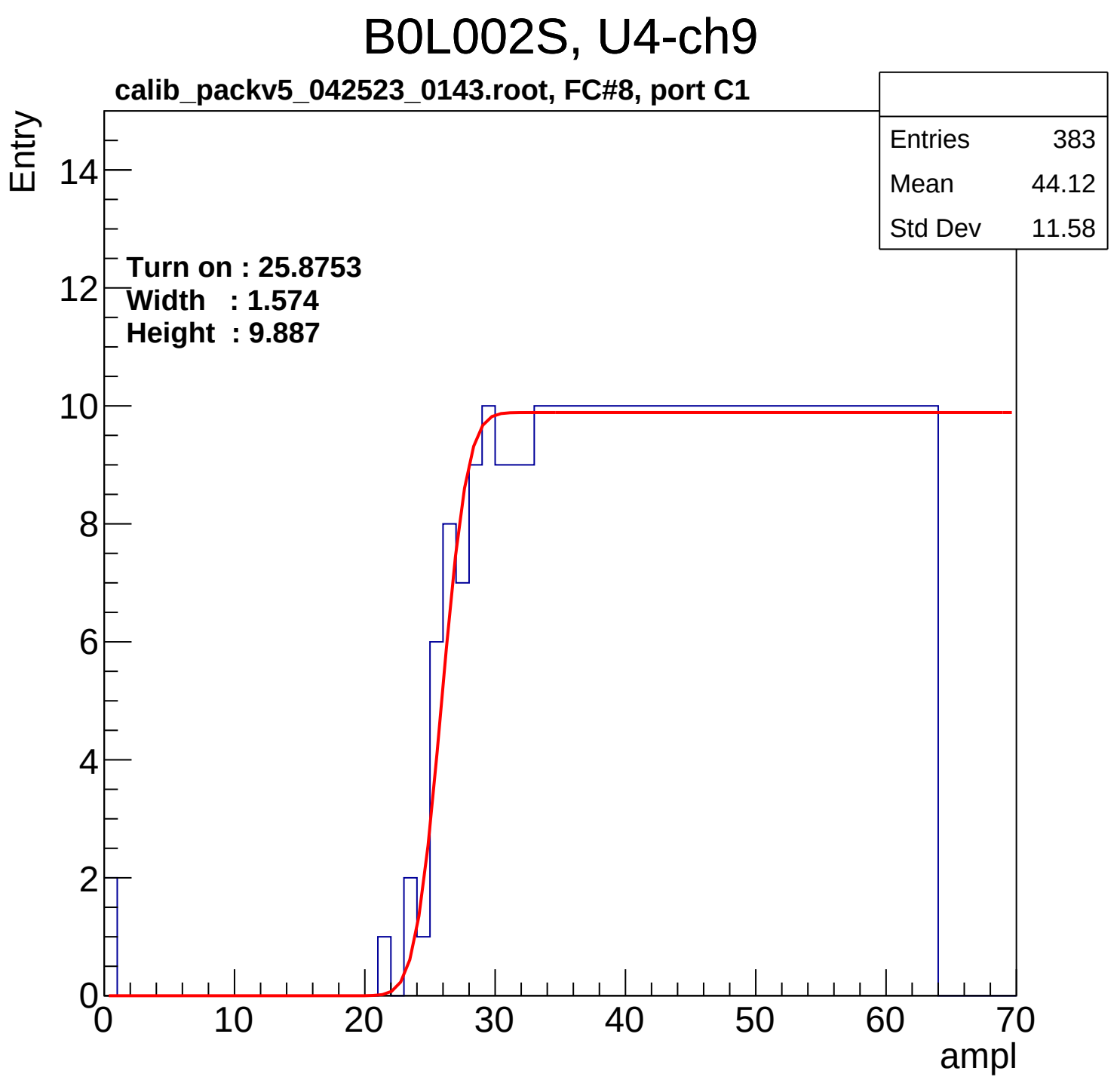

B0L002S, U4-ch4
calib_packv5_042523_0143.root, FC#8, port C1
Entries 372
Mean 44.61
Std Dev 11.46
Turn on : 26.3587
Width : 3.919
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

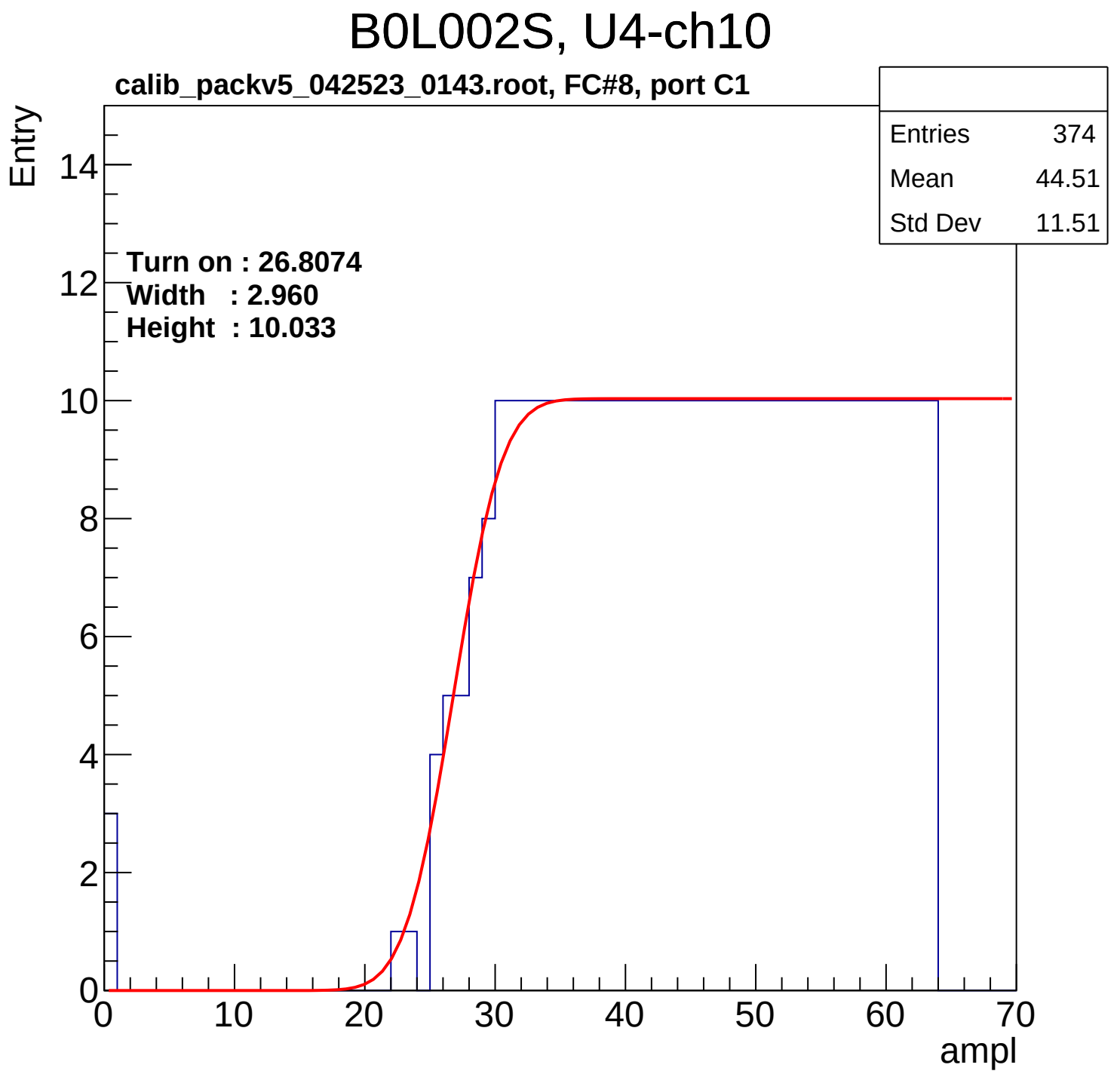

B0L002S, U4-ch5
calib_packv5_042523_0143.root, FC#8, port C1
Entries 363
Mean 45.17
Std Dev 10.87
Turn on : 27.2057
Width : 2.594
Height : 9.926
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

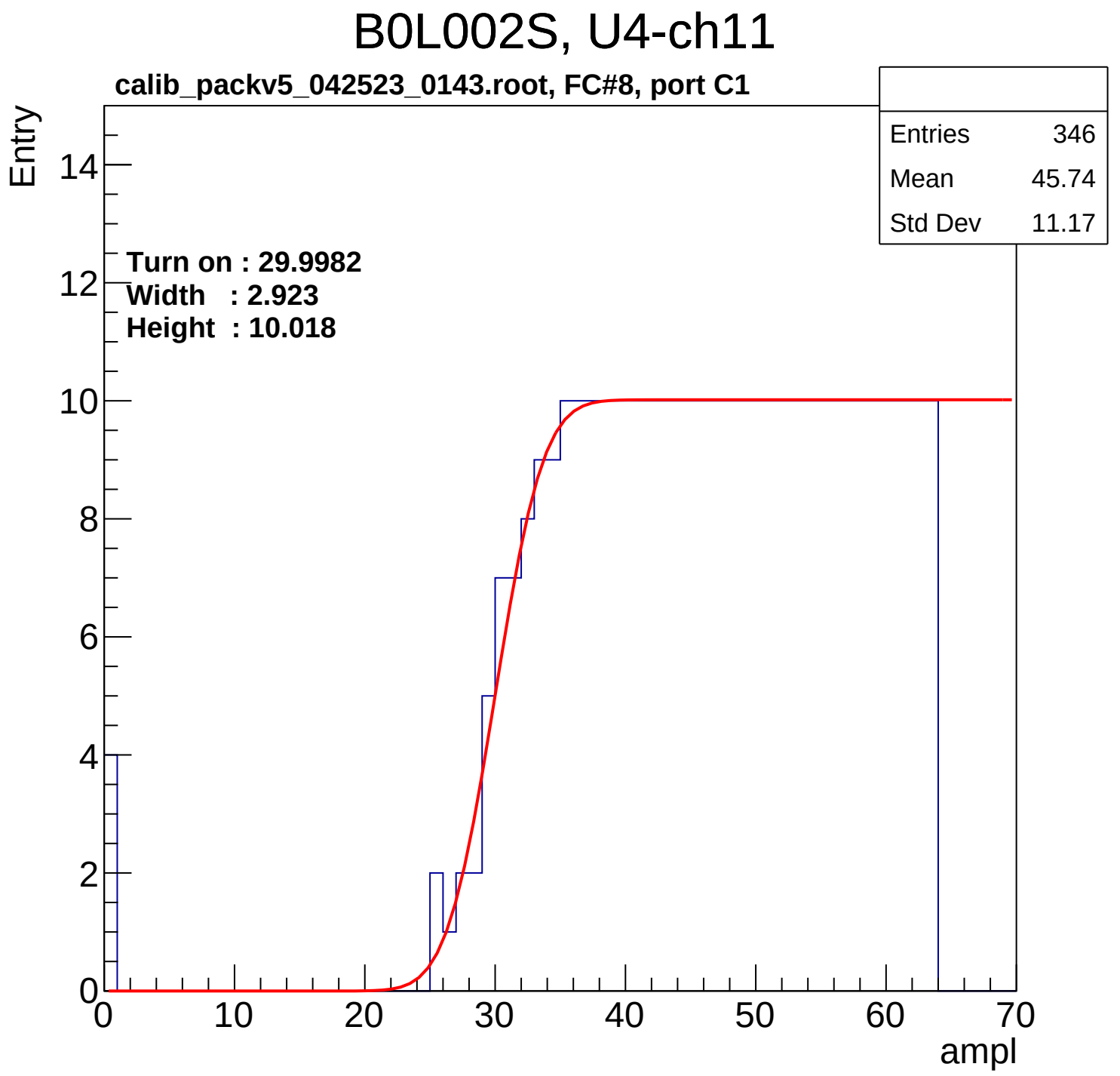

B0L002S, U4-ch6
calib_packv5_042523_0143.root, FC#8, port C1
Entries 356
Mean 45.36
Std Dev 11.13
Turn on : 28.7395
Width : 1.977
Height : 9.950
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

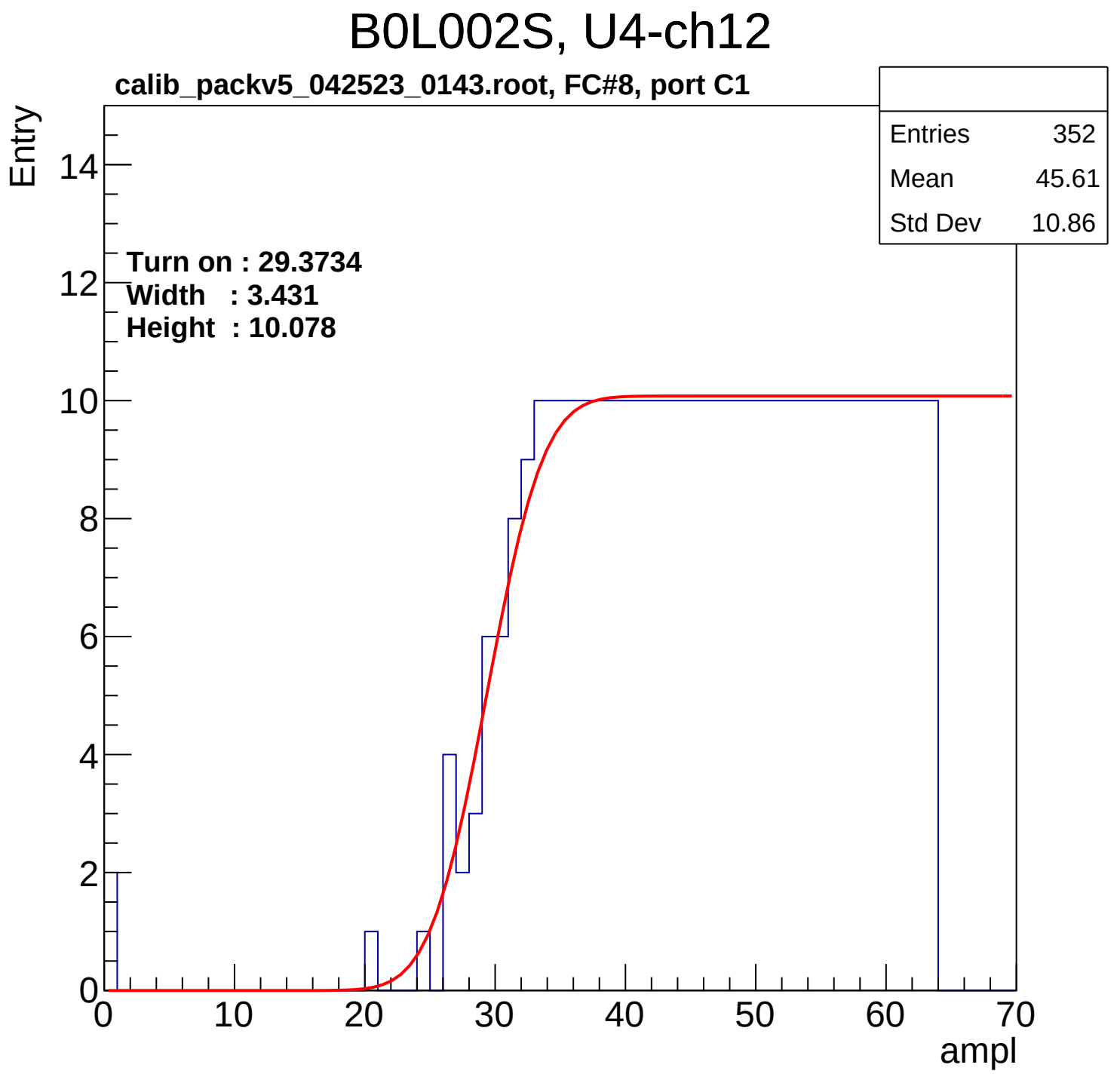

B0L002S, U4-ch7
calib_packv5_042523_0143.root, FC#8, port C1
Entries 383
Mean 44.15
Std Dev 11.54
Turn on : 26.2604
Width : 2.724
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

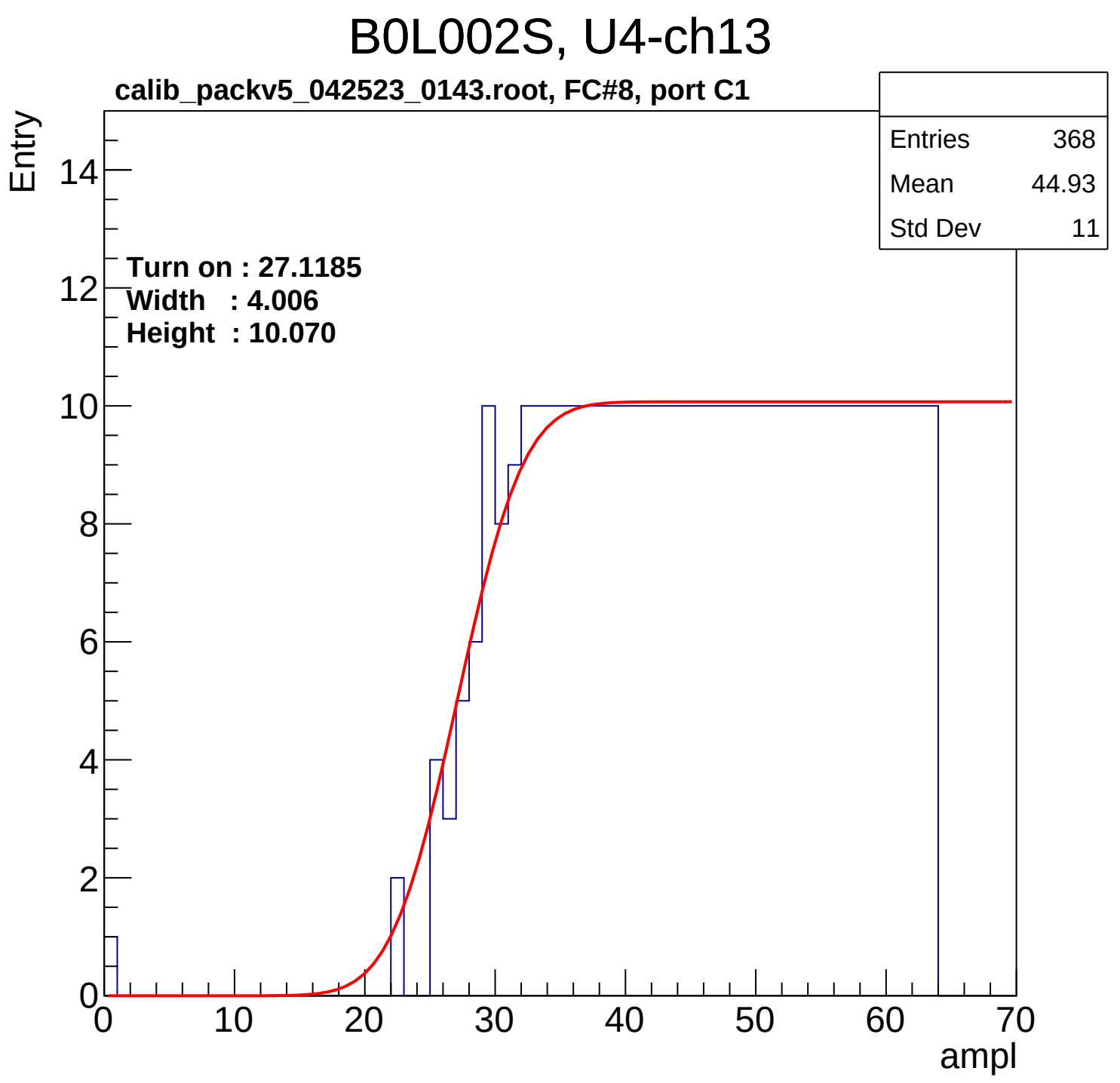

B0L002S, U4-ch8
calib_packv5_042523_0143.root, FC#8, port C1
Entries 378
Mean 44.41
Std Dev 11.38
Turn on : 26.6664
Width : 1.932
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

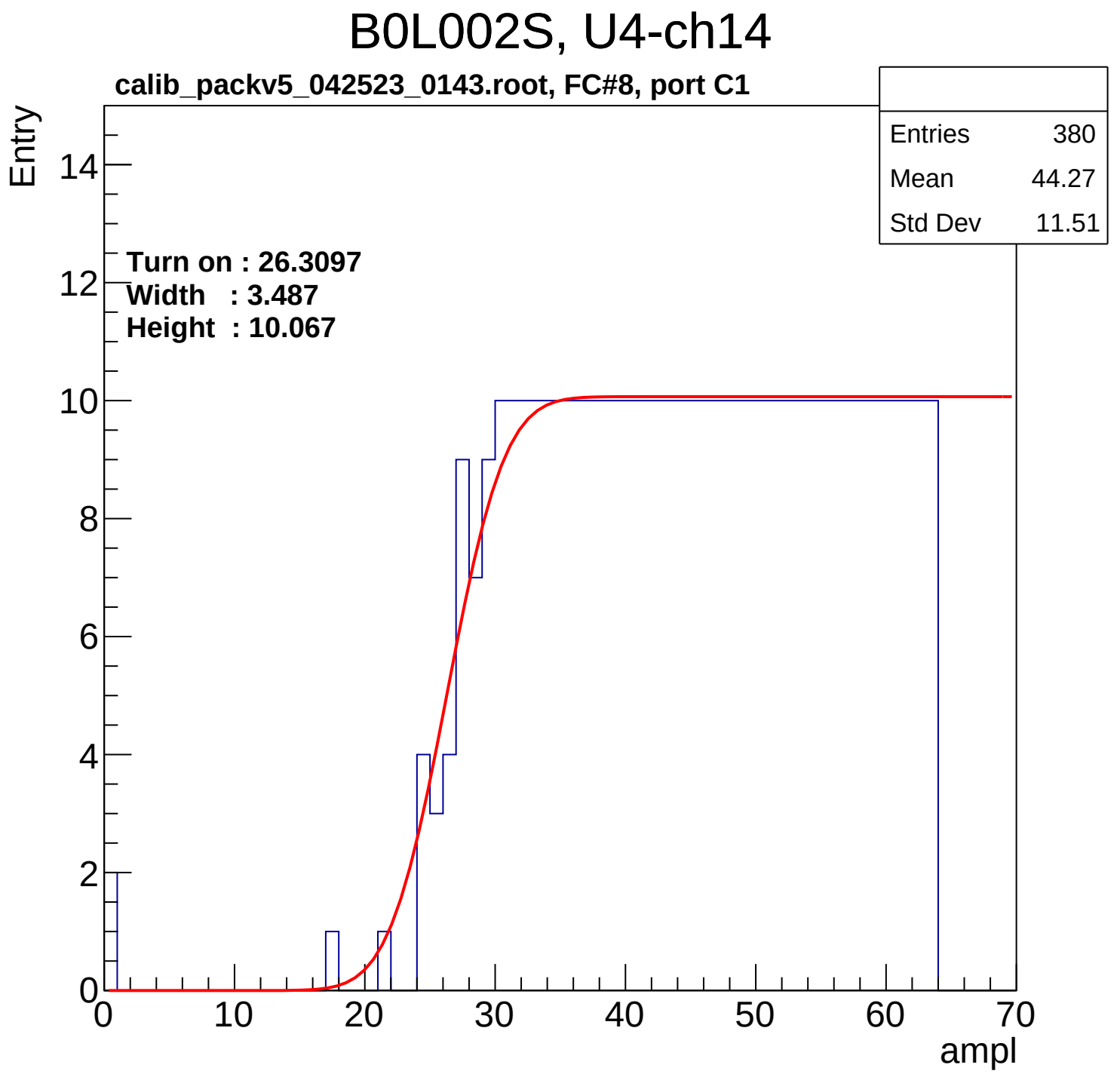

B0L002S, U4-ch9
calib_packv5_042523_0143.root, FC#8, port C1
Entries 383
Mean 44.12
Std Dev 11.58
Turn on : 25.8753
Width : 1.574
Height : 9.887
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

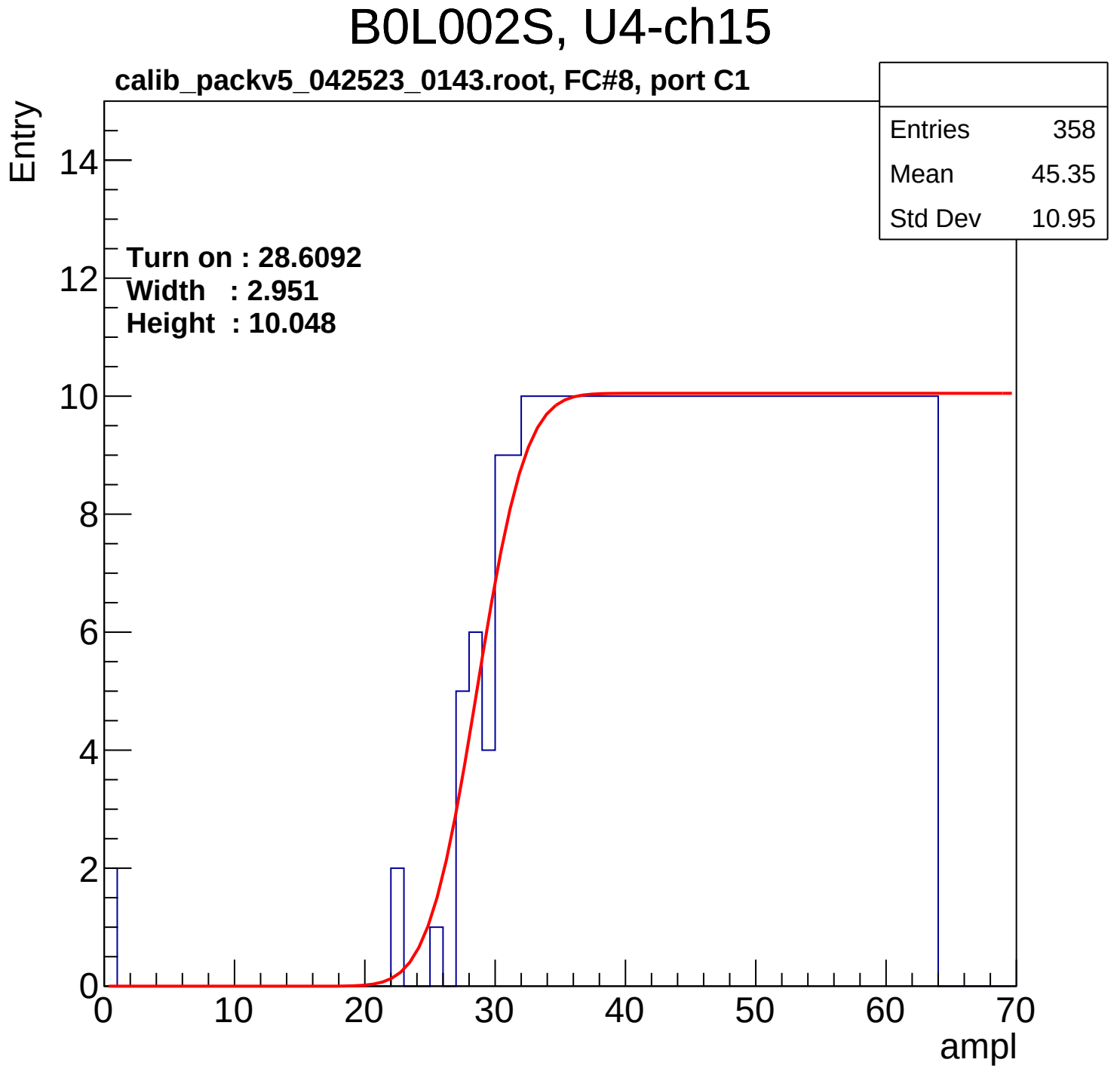

B0L002S, U4-ch10
calib_packv5_042523_0143.root, FC#8, port C1
Entries 374
Mean 44.51
Std Dev 11.51
Turn on : 26.8074
Width : 2.960
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

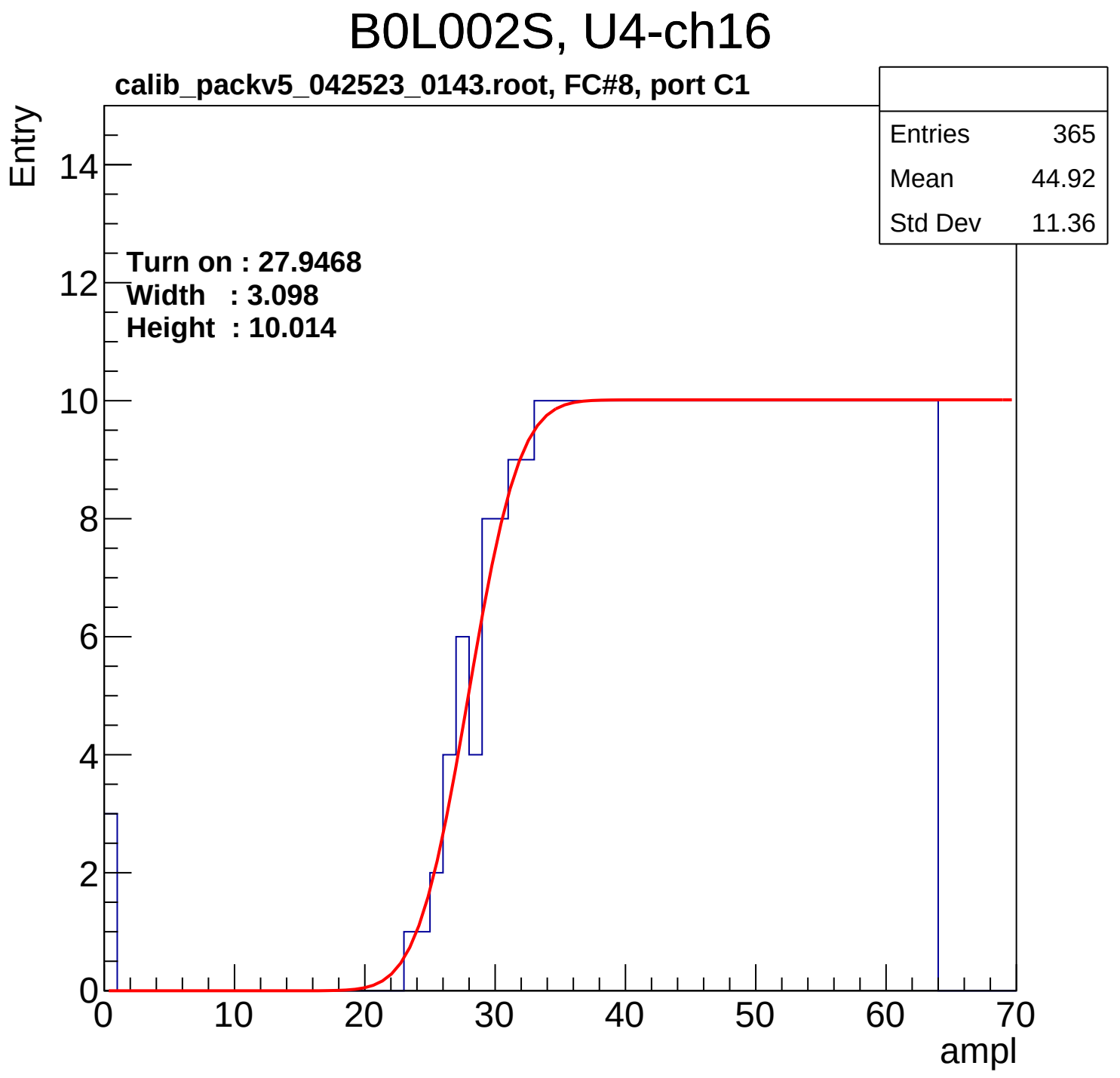

B0L002S, U4-ch11
calib_packv5_042523_0143.root, FC#8, port C1
Entries 346
Mean 45.74
Std Dev 11.17
Turn on : 29.9982
Width : 2.923
Height : 10.018
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

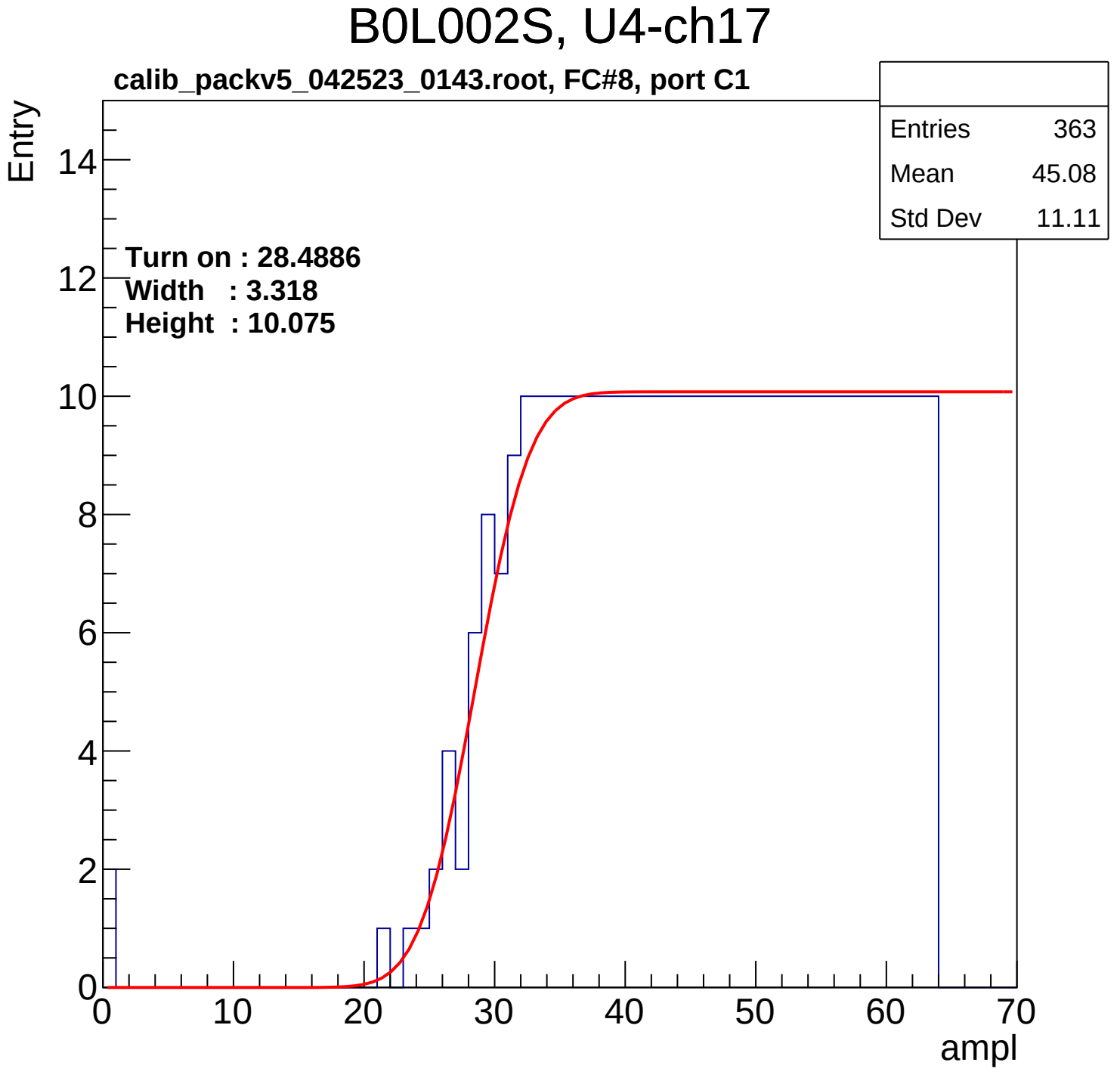

B0L002S, U4-ch12
calib_packv5_042523_0143.root, FC#8, port C1
Entries 352
Mean 45.61
Std Dev 10.86
Turn on : 29.3734
Width : 3.431
Height : 10.078
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

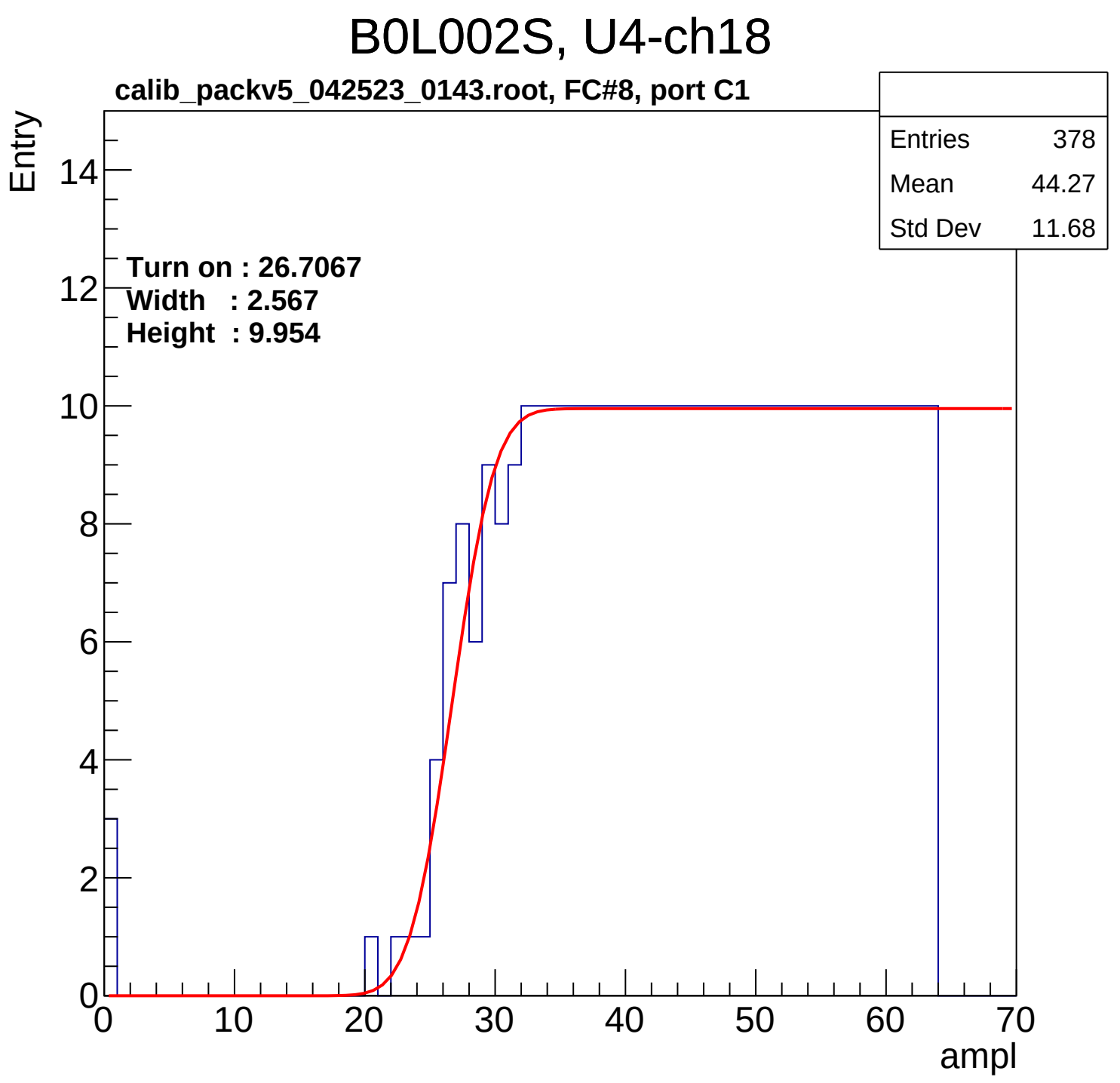

B0L002S, U4-ch13
calib_packv5_042523_0143.root, FC#8, port C1
Entries 368
Mean 44.93
Std Dev 11
Turn on : 27.1185
Width : 4.006
Height : 10.070
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

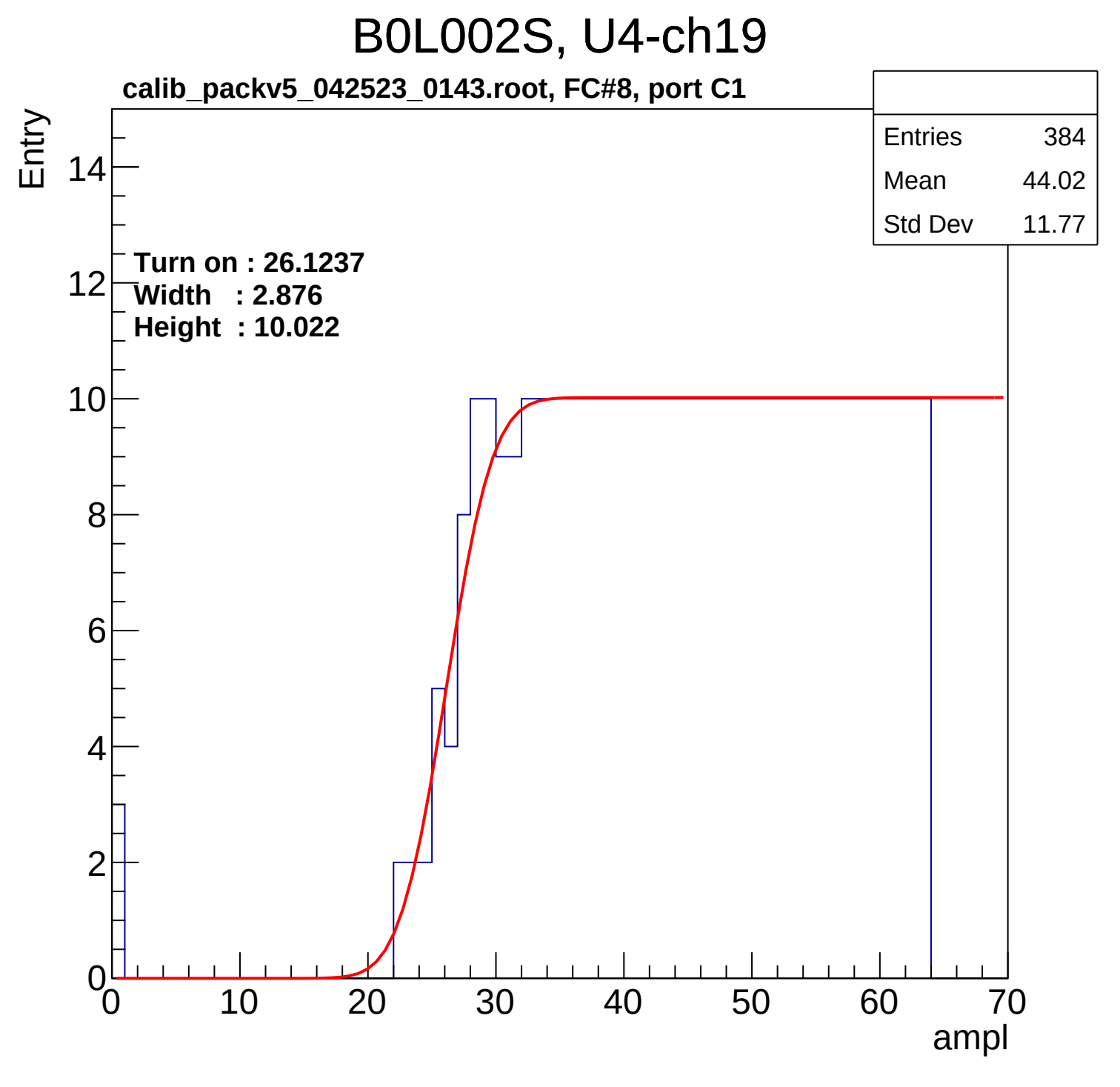

B0L002S, U4-ch14
calib_packv5_042523_0143.root, FC#8, port C1
Entries 380
Mean 44.27
Std Dev 11.51
Turn on : 26.3097
Width : 3.487
Height : 10.067
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

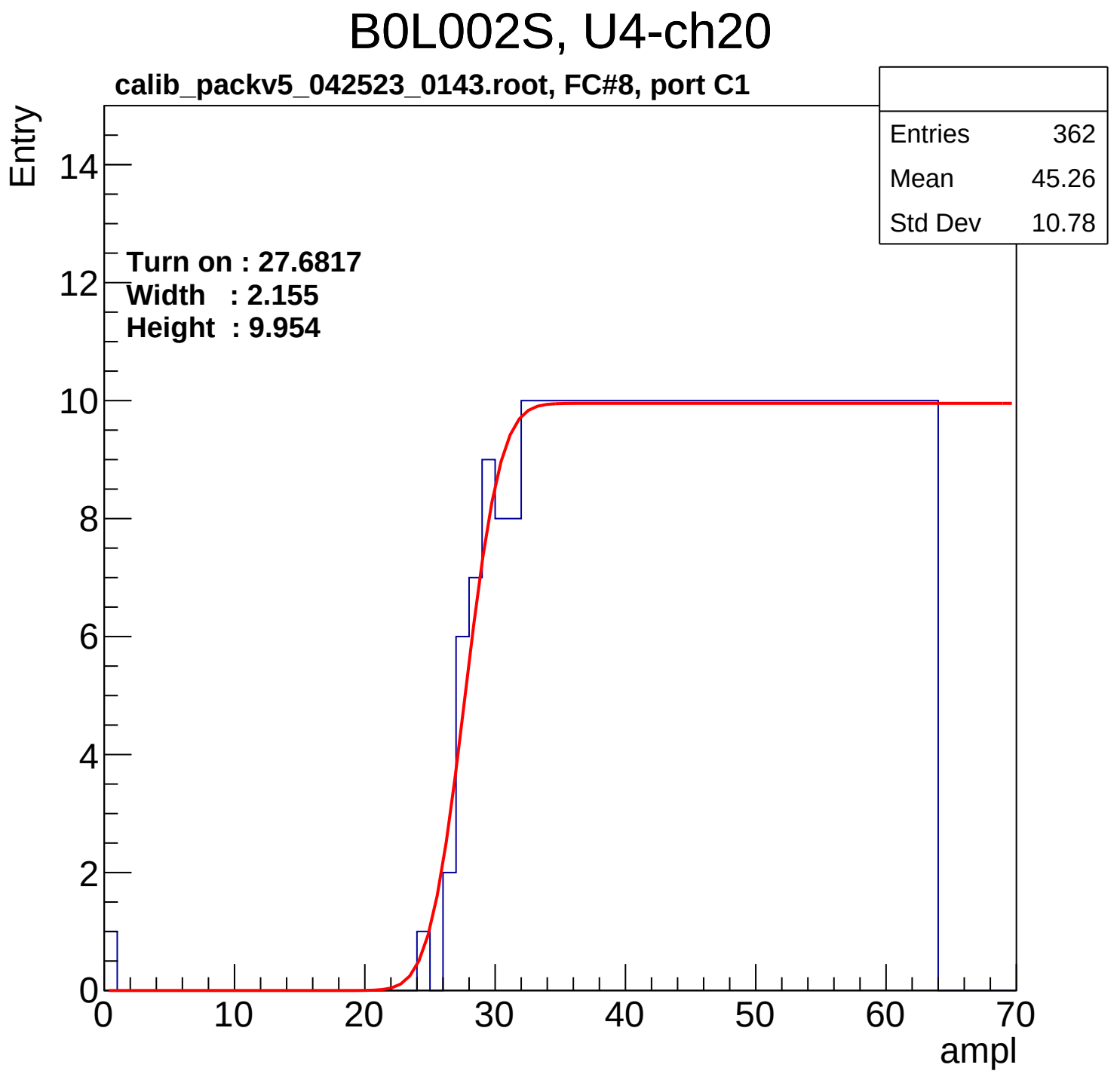

B0L002S, U4-ch15
calib_packv5_042523_0143.root, FC#8, port C1
Entries 358
Mean 45.35
Std Dev 10.95
Turn on : 28.6092
Width : 2.951
Height : 10.048
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

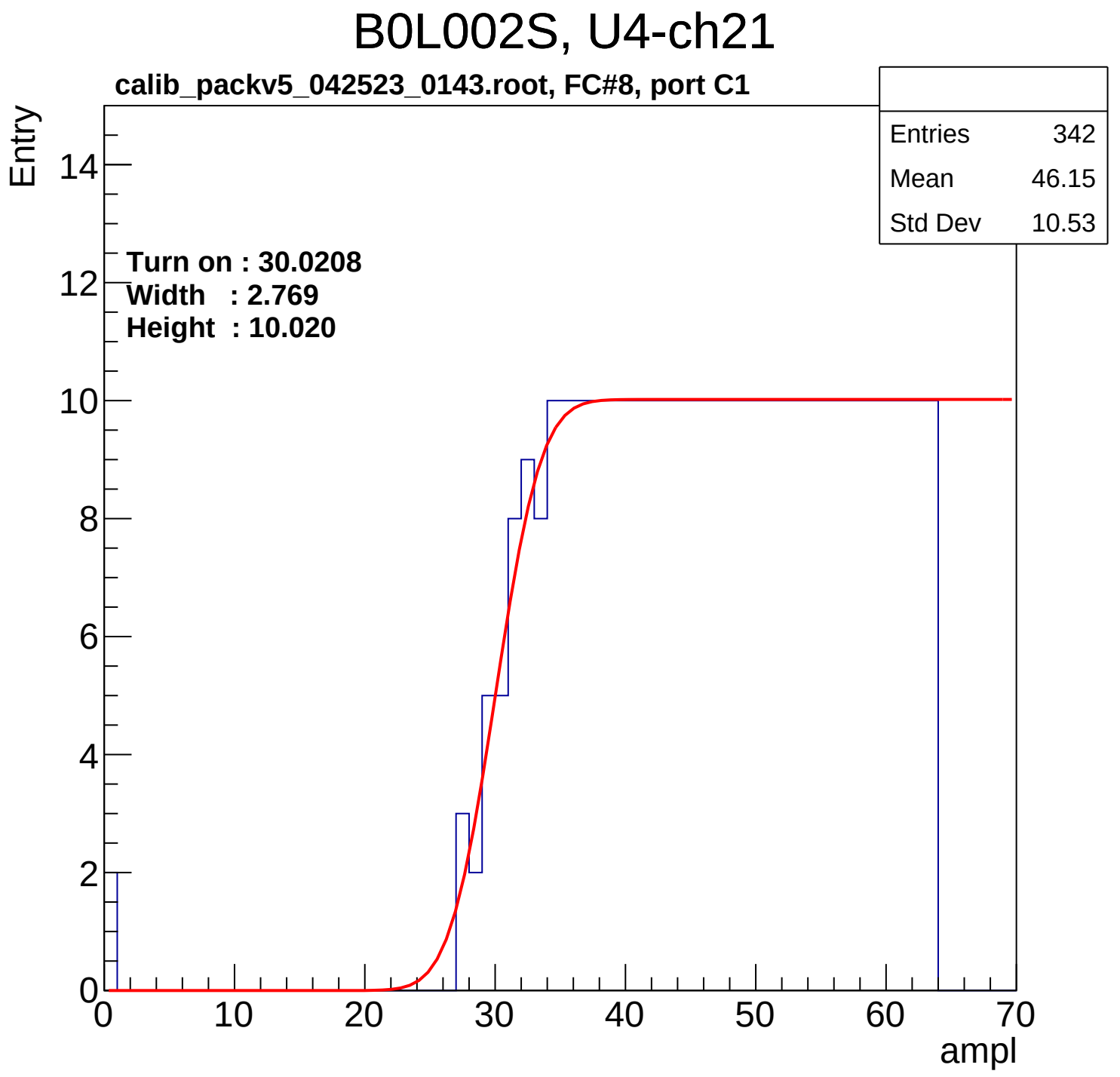

B0L002S, U4-ch16
calib_packv5_042523_0143.root, FC#8, port C1
Entries 365
Mean 44.92
Std Dev 11.36
Turn on : 27.9468
Width : 3.098
Height : 10.014
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

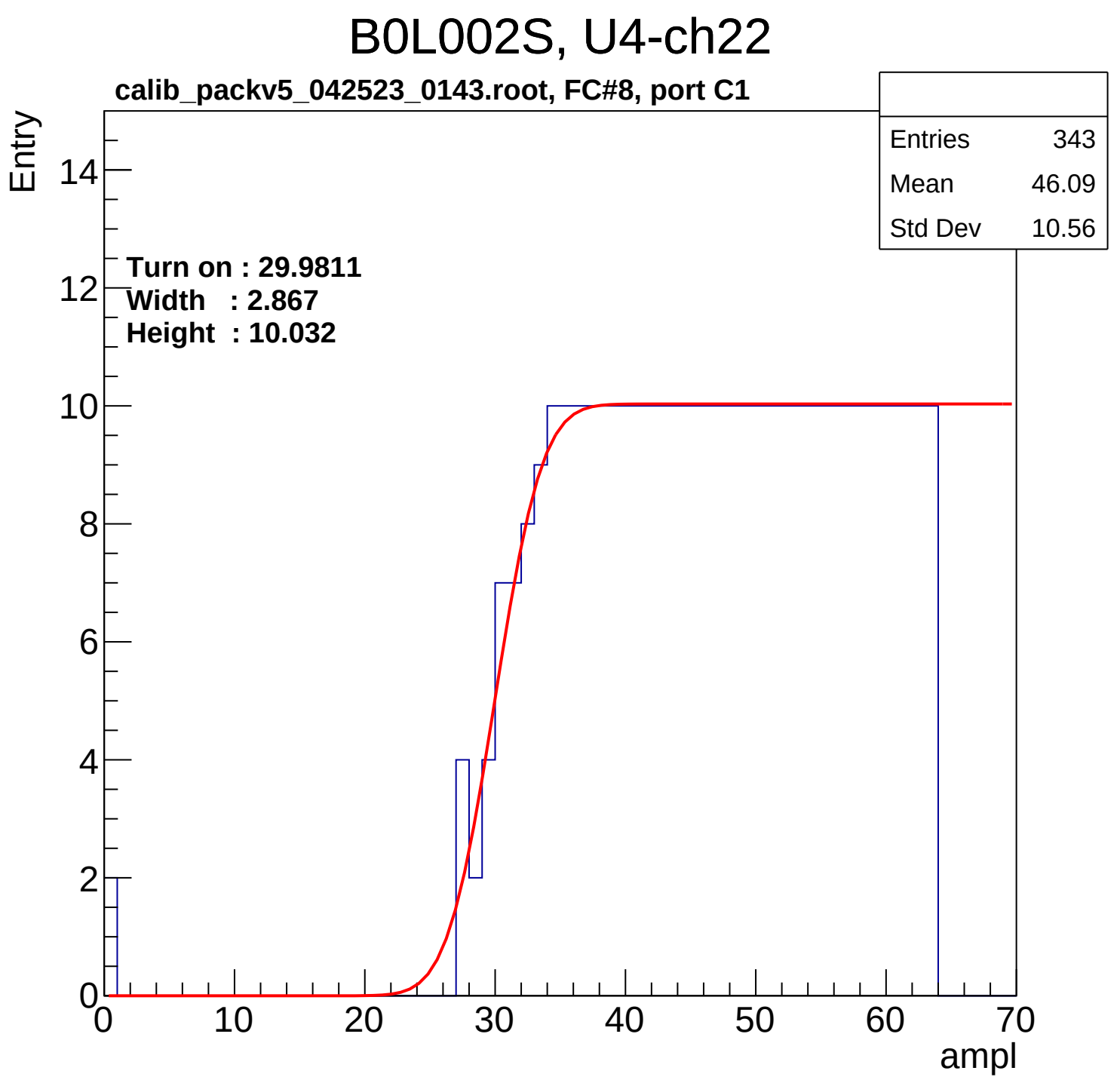

B0L002S, U4-ch17
calib_packv5_042523_0143.root, FC#8, port C1
Entries 363
Mean 45.08
Std Dev 11.11
Turn on : 28.4886
Width : 3.318
Height : 10.075
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

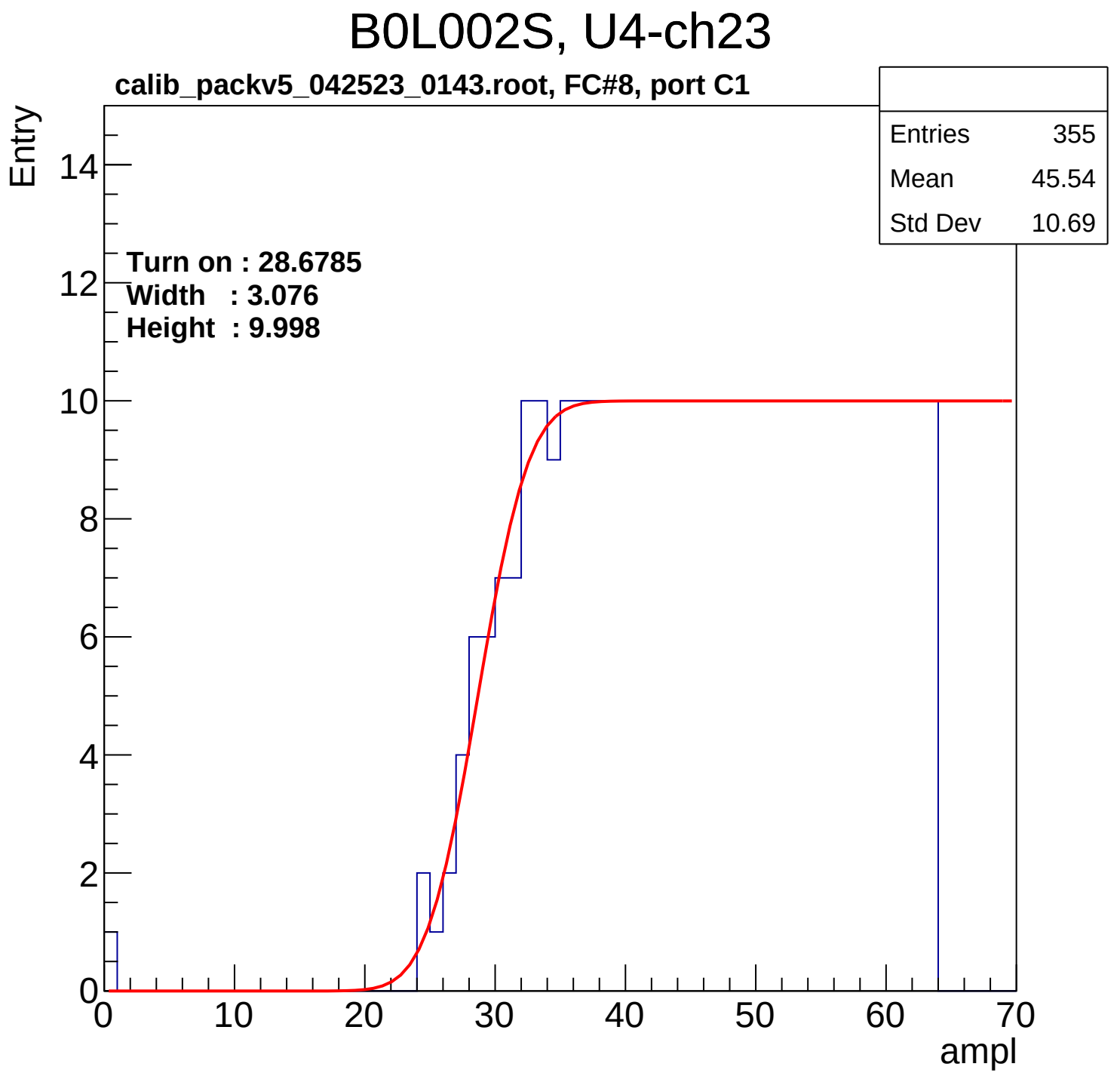

B0L002S, U4-ch18
calib_packv5_042523_0143.root, FC#8, port C1
Entries 378
Mean 44.27
Std Dev 11.68
Turn on : 26.7067
Width : 2.567
Height : 9.954
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

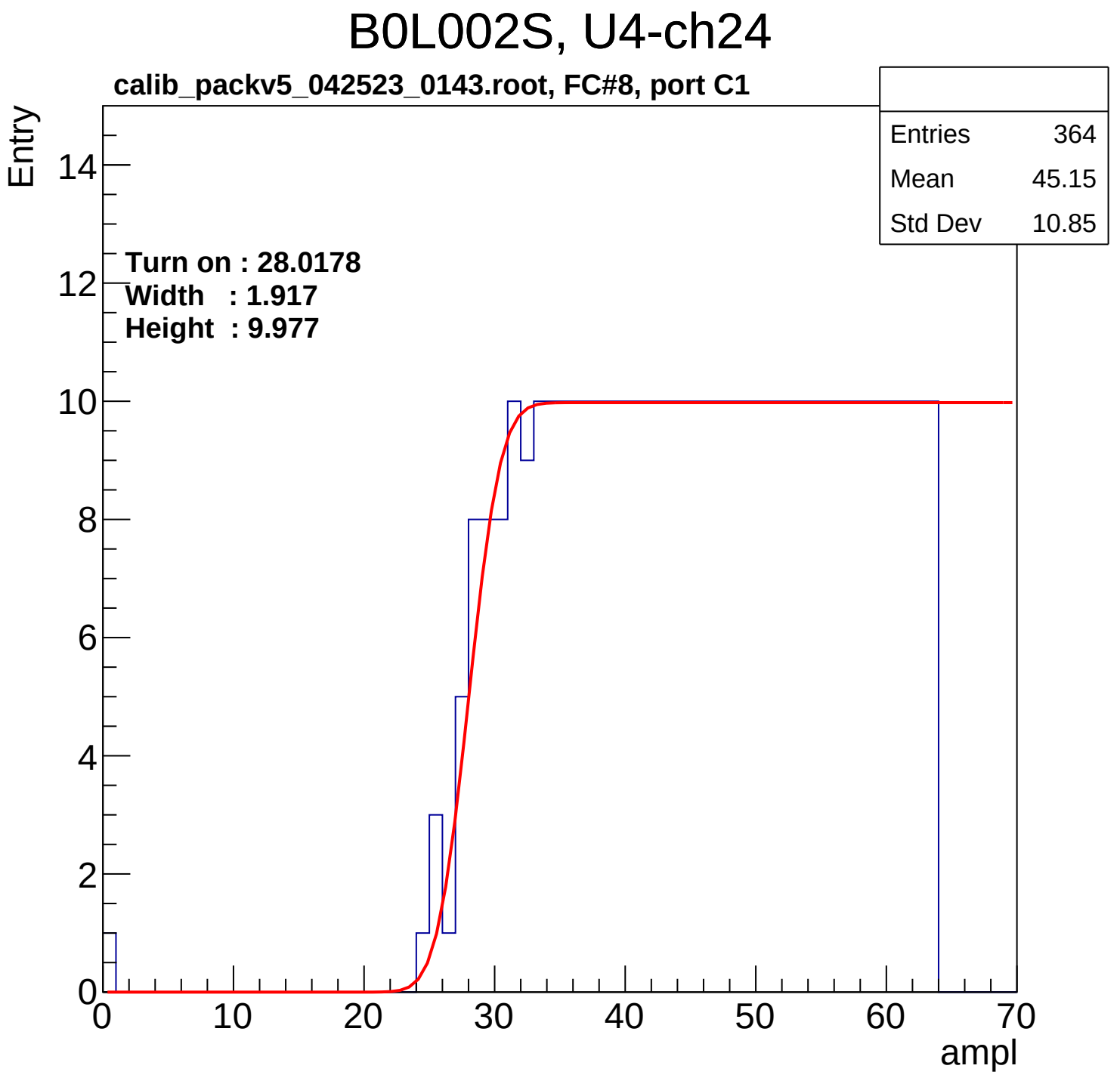

B0L002S, U4-ch19
calib_packv5_042523_0143.root, FC#8, port C1
Entries 384
Mean 44.02
Std Dev 11.77
Turn on : 26.1237
Width : 2.876
Height : 10.022
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

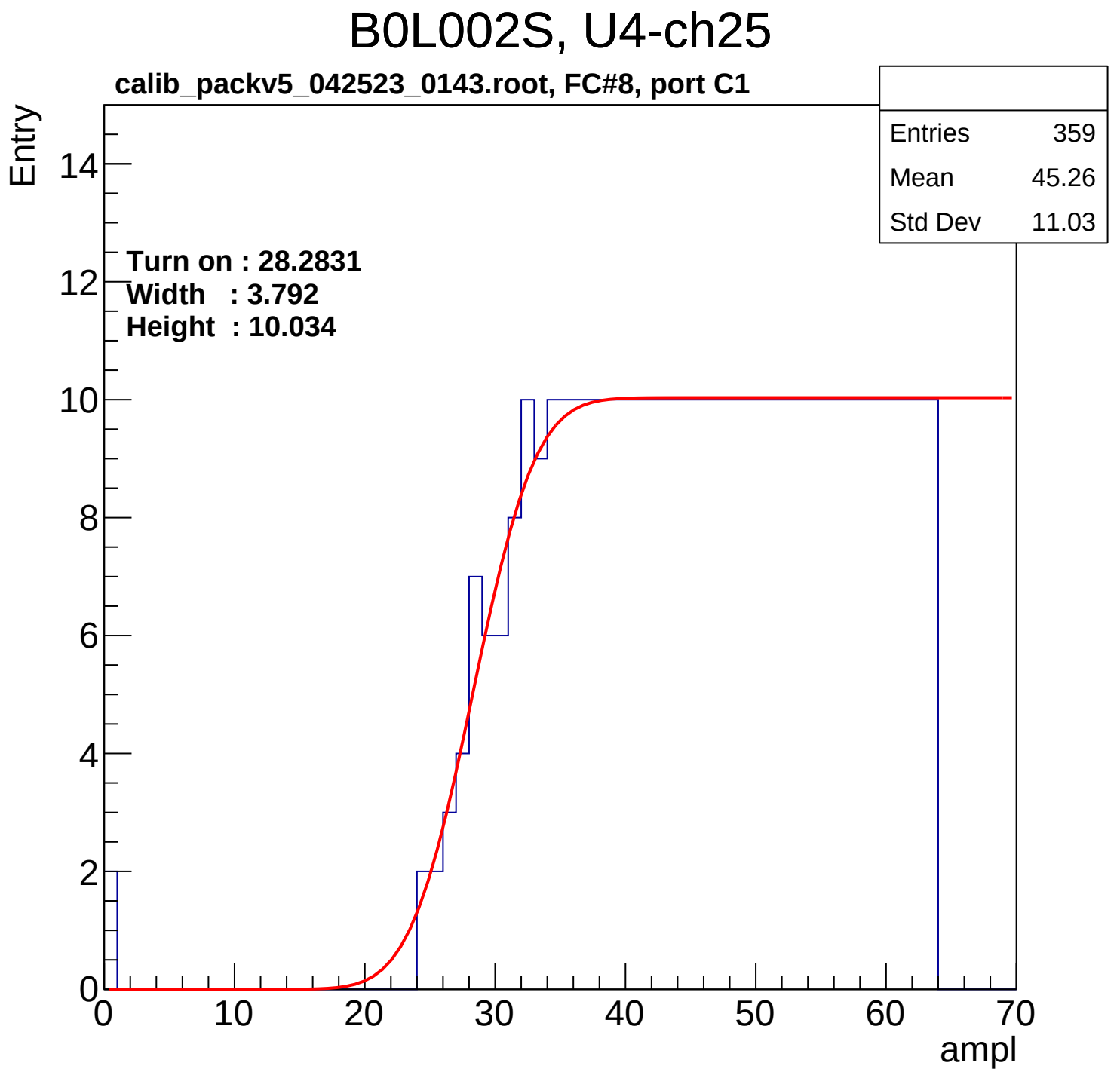

B0L002S, U4-ch20
calib_packv5_042523_0143.root, FC#8, port C1
Entries 362
Mean 45.26
Std Dev 10.78
Turn on : 27.6817
Width : 2.155
Height : 9.954
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

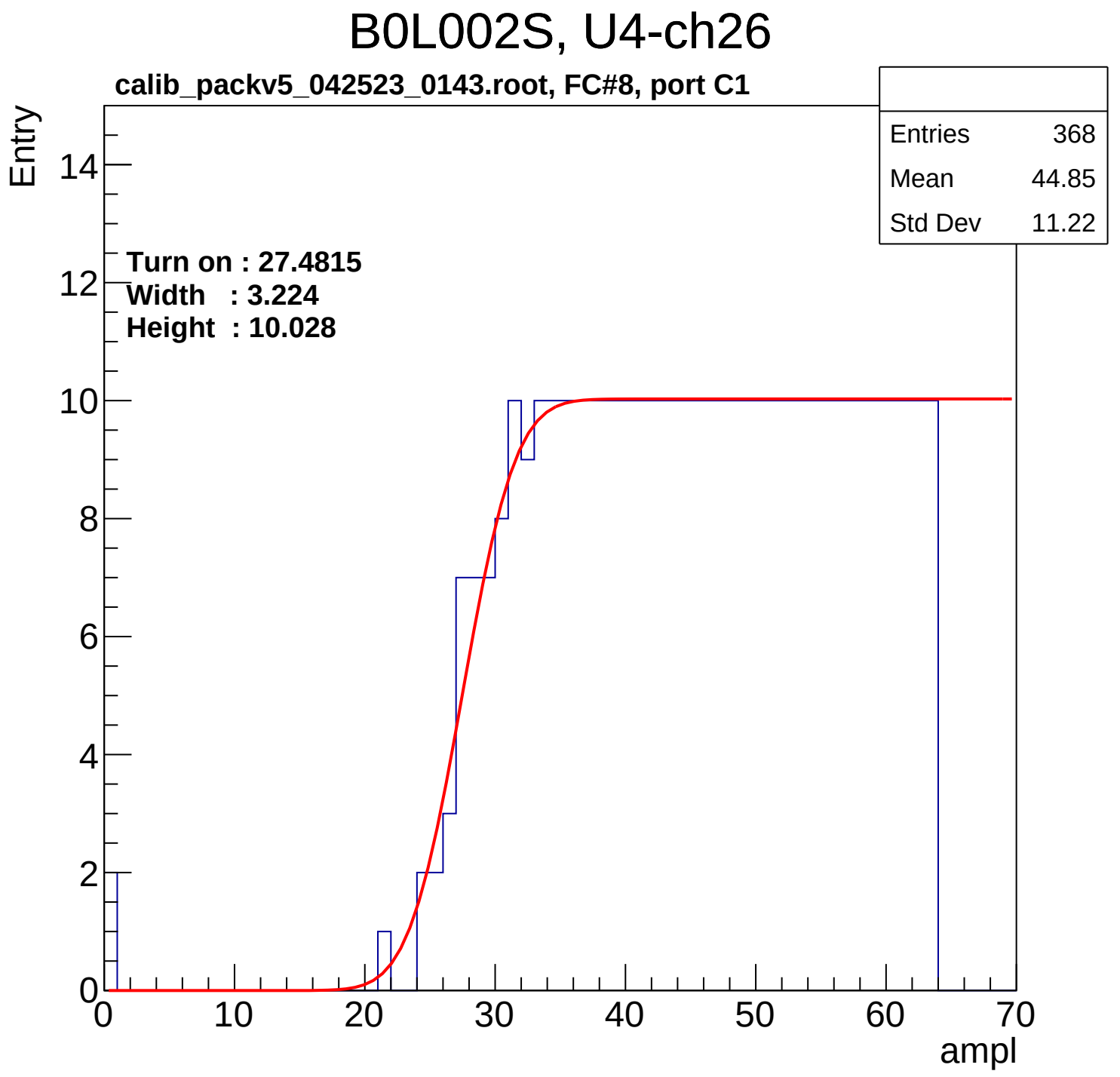

B0L002S, U4-ch21
calib_packv5_042523_0143.root, FC#8, port C1
Entries 342
Mean 46.15
Std Dev 10.53
Turn on : 30.0208
Width : 2.769
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

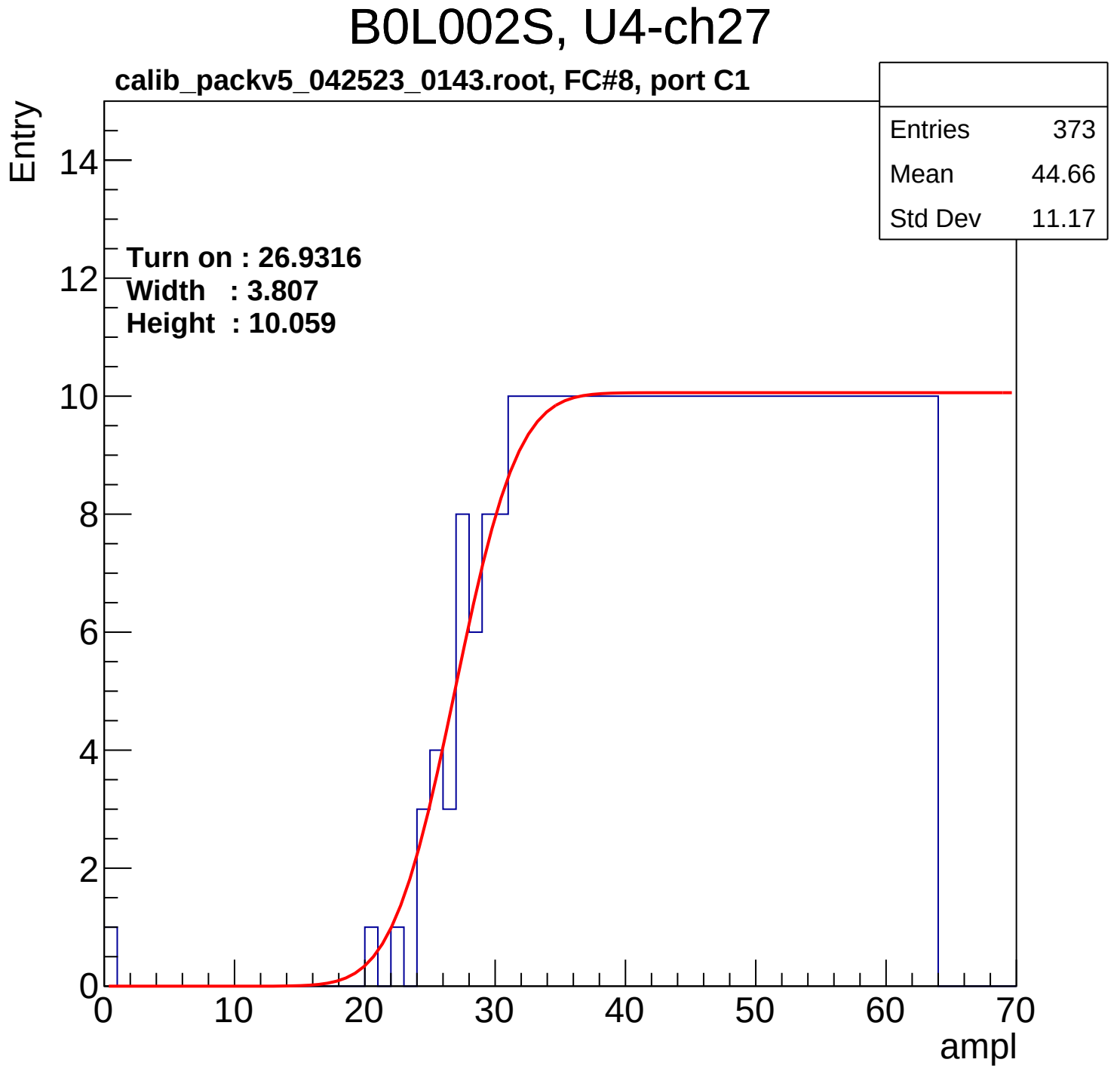

B0L002S, U4-ch22
calib_packv5_042523_0143.root, FC#8, port C1
Entries 343
Mean 46.09
Std Dev 10.56
Turn on : 29.9811
Width : 2.867
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

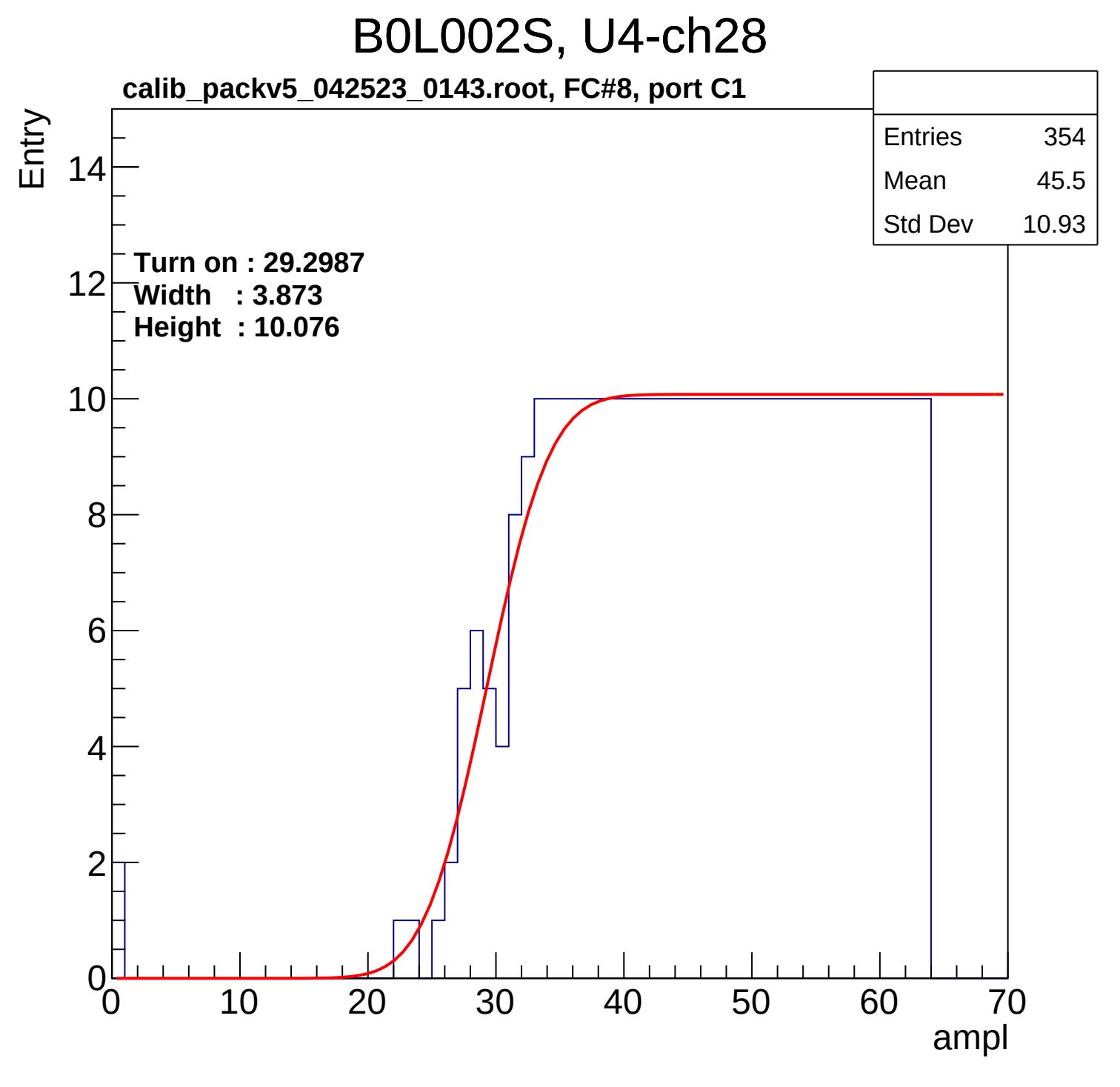

B0L002S, U4-ch23
calib_packv5_042523_0143.root, FC#8, port C1
Entries 355
Mean 45.54
Std Dev 10.69
Turn on : 28.6785
Width : 3.076
Height : 9.998
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

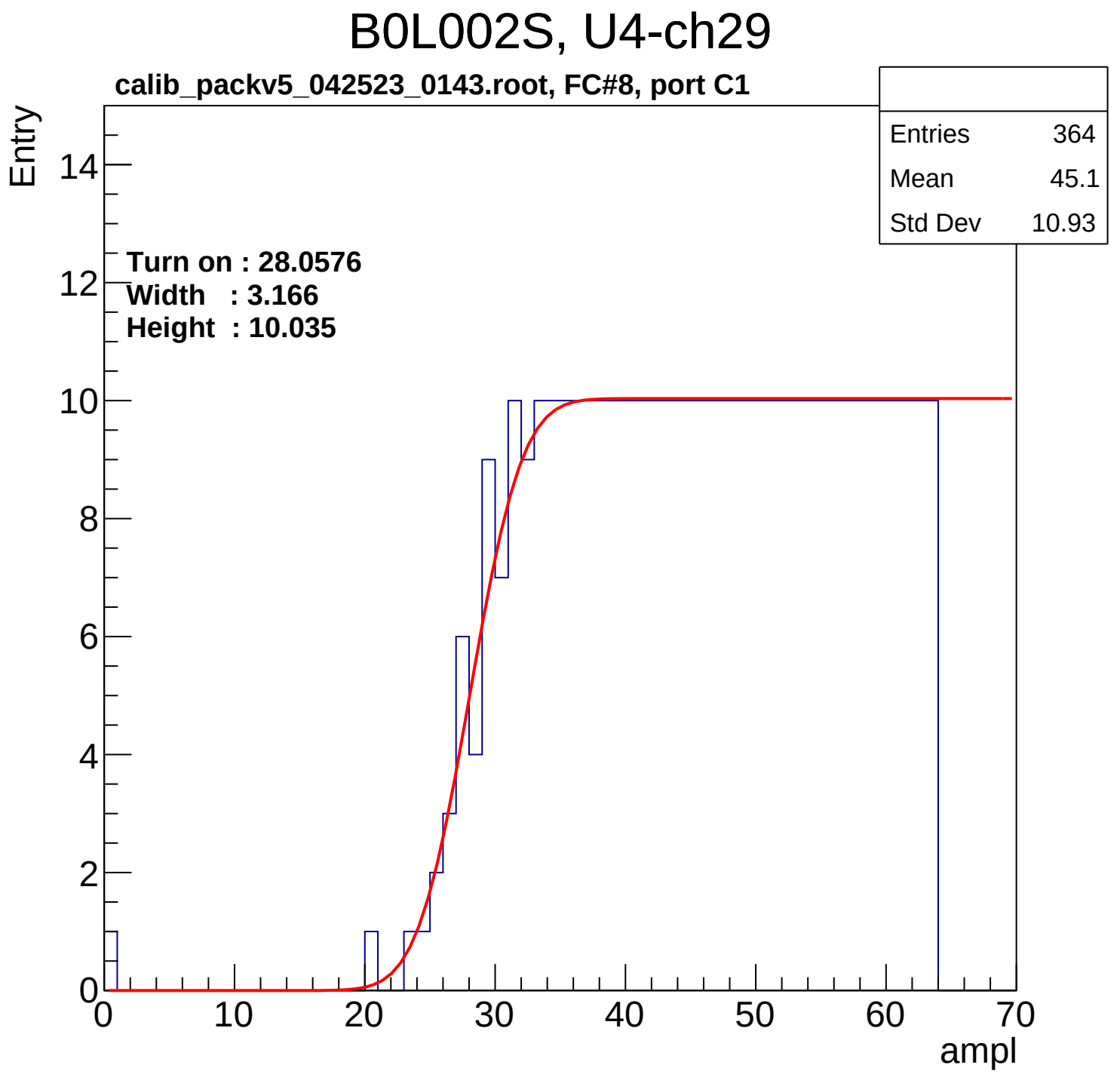

B0L002S, U4-ch24
calib_packv5_042523_0143.root, FC#8, port C1
Entries 364
Mean 45.15
Std Dev 10.85
Turn on : 28.0178
Width : 1.917
Height : 9.977
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

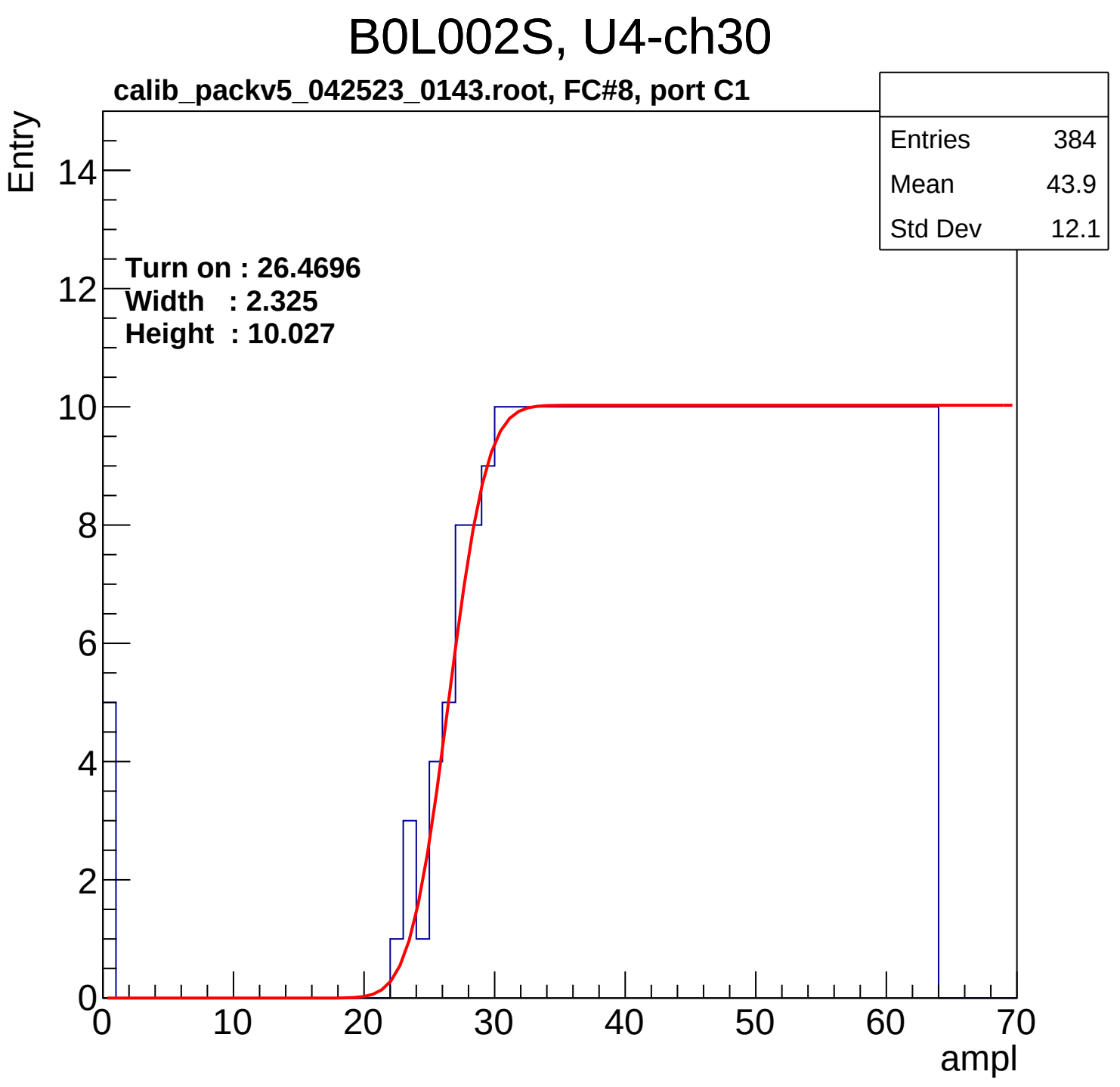

B0L002S, U4-ch25
calib_packv5_042523_0143.root, FC#8, port C1
Entries 359
Mean 45.26
Std Dev 11.03
Turn on : 28.2831
Width : 3.792
Height : 10.034
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

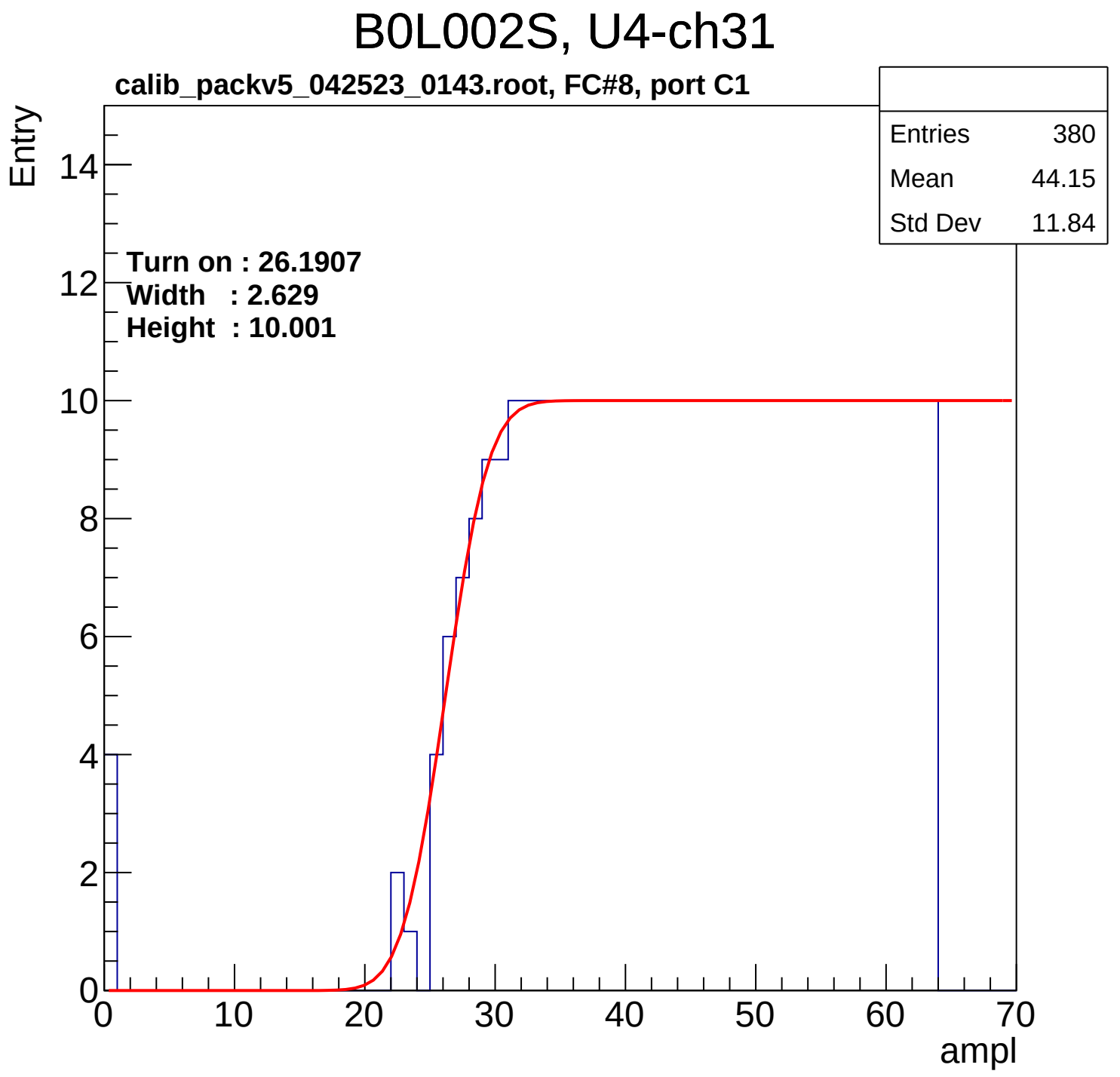

B0L002S, U4-ch26
calib_packv5_042523_0143.root, FC#8, port C1
Entries 368
Mean 44.85
Std Dev 11.22
Turn on : 27.4815
Width : 3.224
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

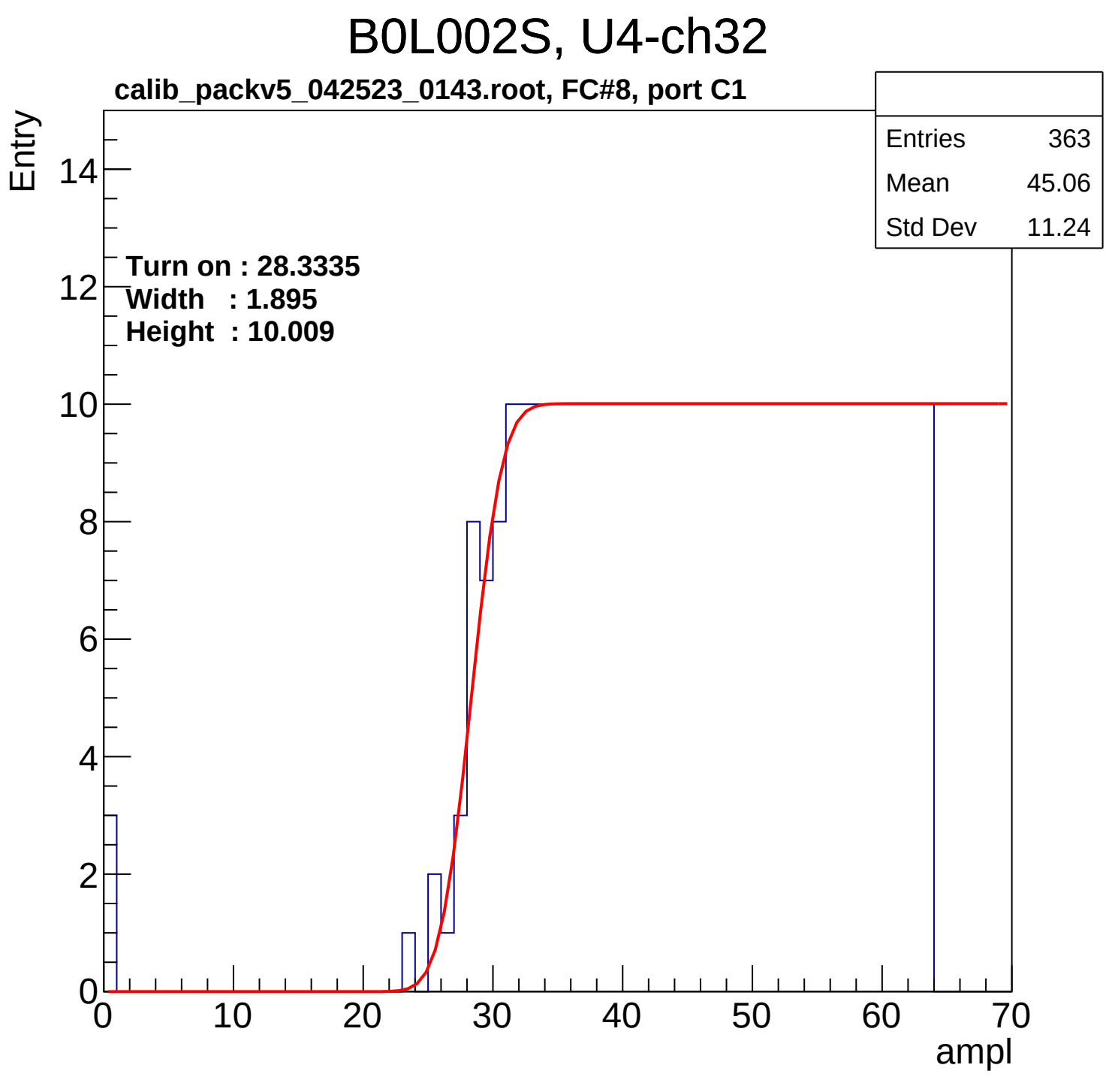

B0L002S, U4-ch27
calib_packv5_042523_0143.root, FC#8, port C1
Entries 373
Mean 44.66
Std Dev 11.17
Turn on : 26.9316
Width : 3.807
Height : 10.059
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

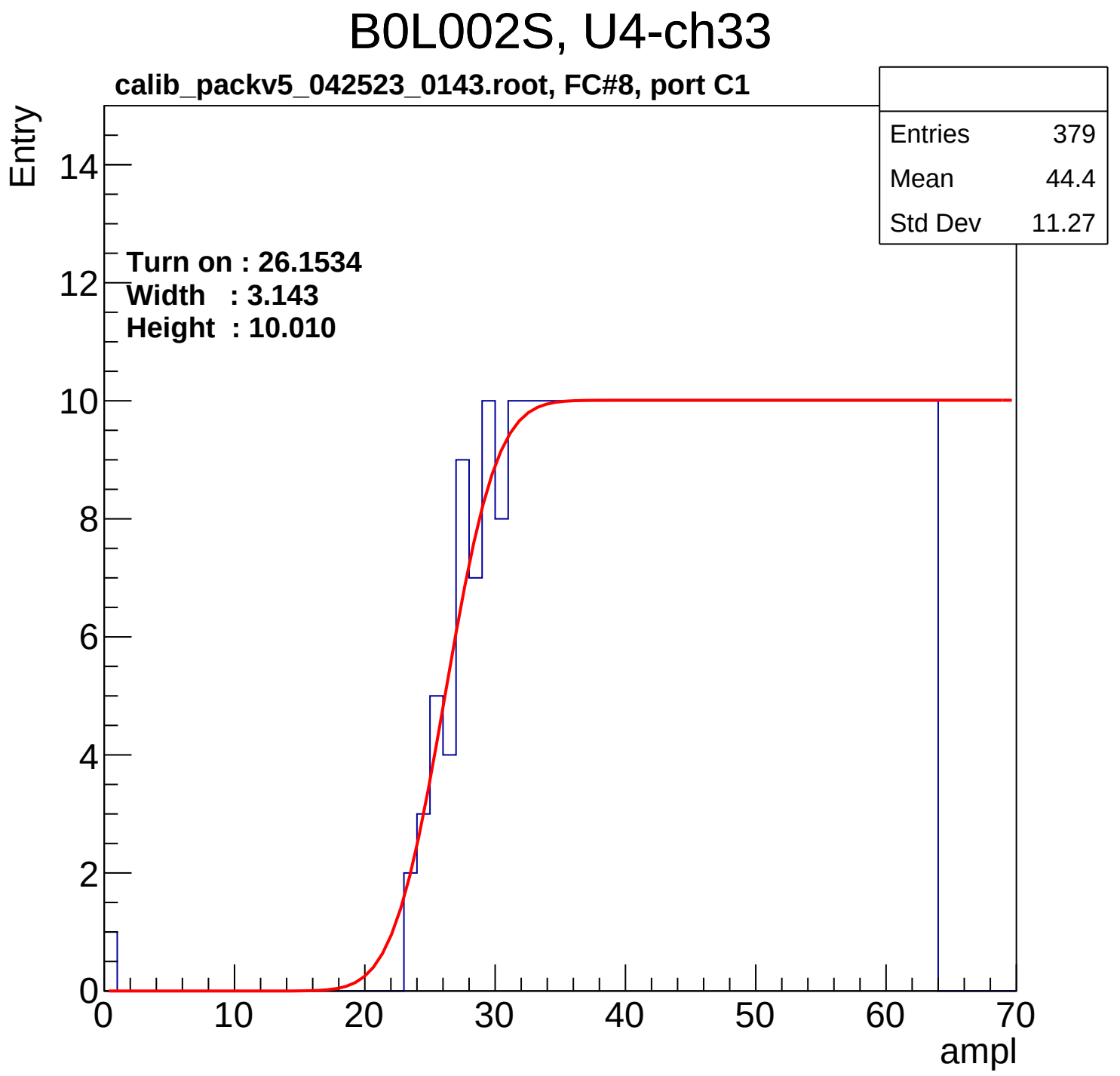

B0L002S, U4-ch28
calib_packv5_042523_0143.root, FC#8, port C1
Entries 354
Mean 45.5
Std Dev 10.93
Turn on : 29.2987
Width : 3.873
Height : 10.076
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

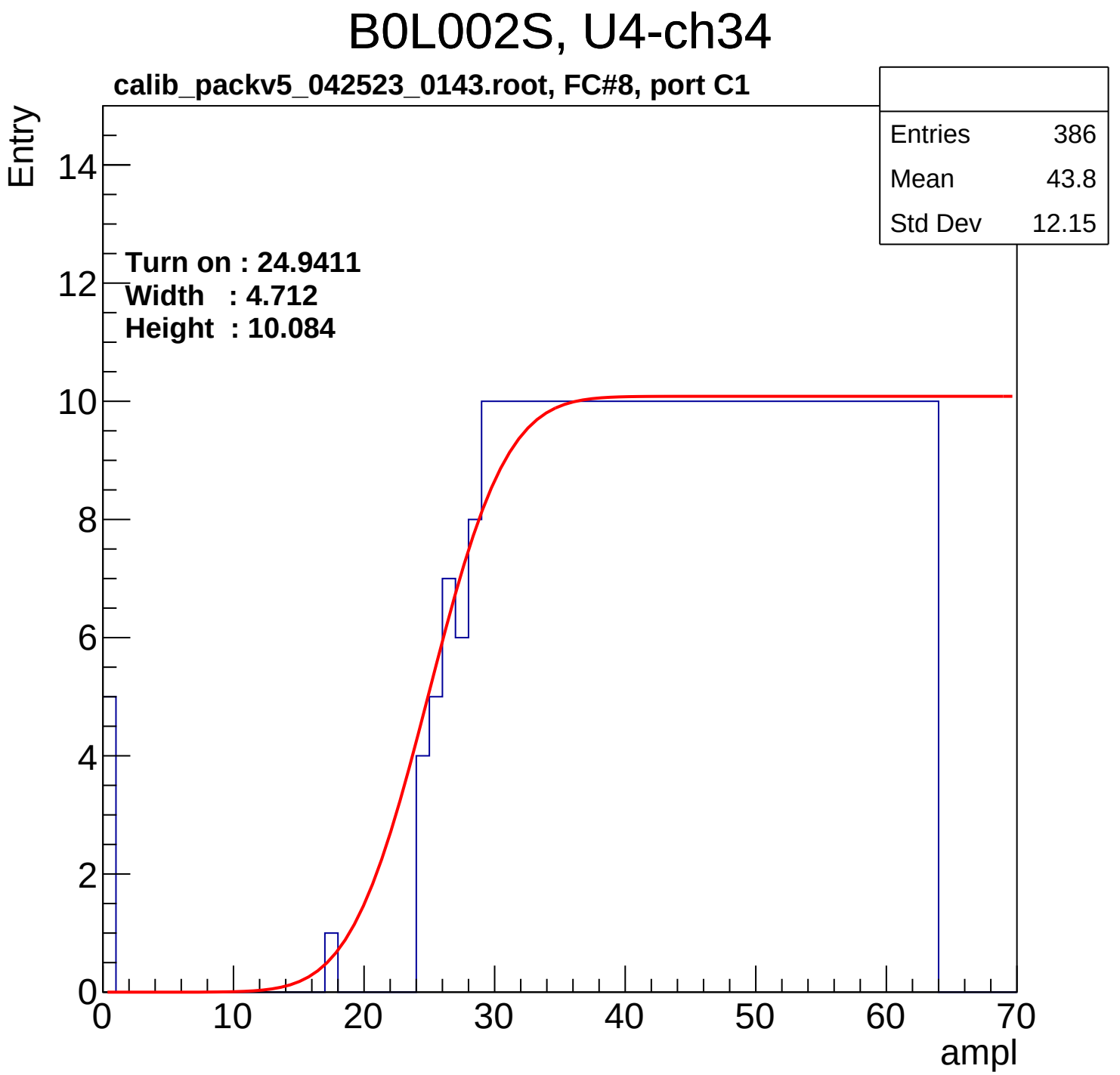

B0L002S, U4-ch29
calib_packv5_042523_0143.root, FC#8, port C1
Entries 364
Mean 45.1
Std Dev 10.93
Turn on : 28.0576
Width : 3.166
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

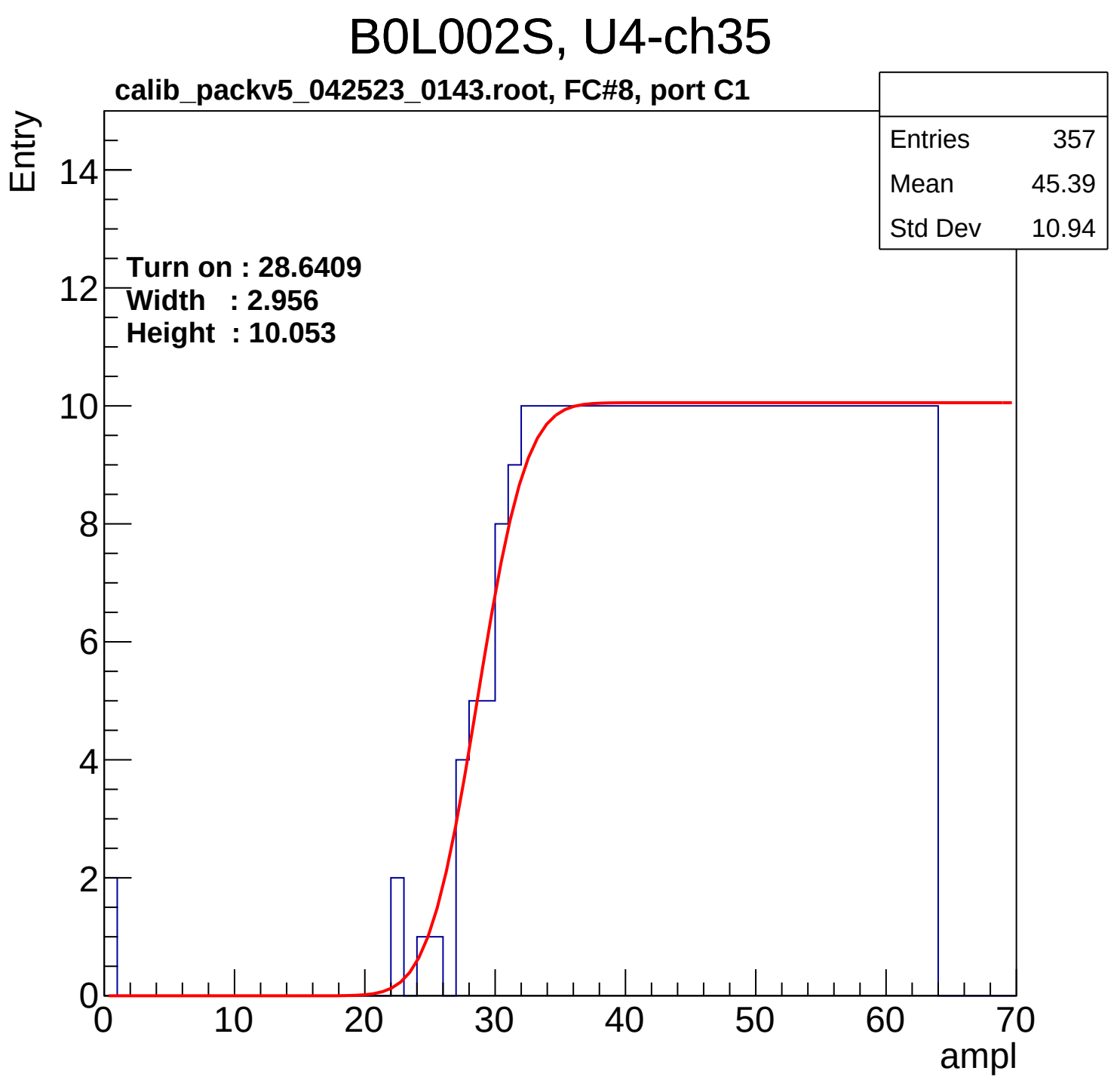

B0L002S, U4-ch30
calib_packv5_042523_0143.root, FC#8, port C1
Entries 384
Mean 43.9
Std Dev 12.1
Turn on : 26.4696
Width : 2.325
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

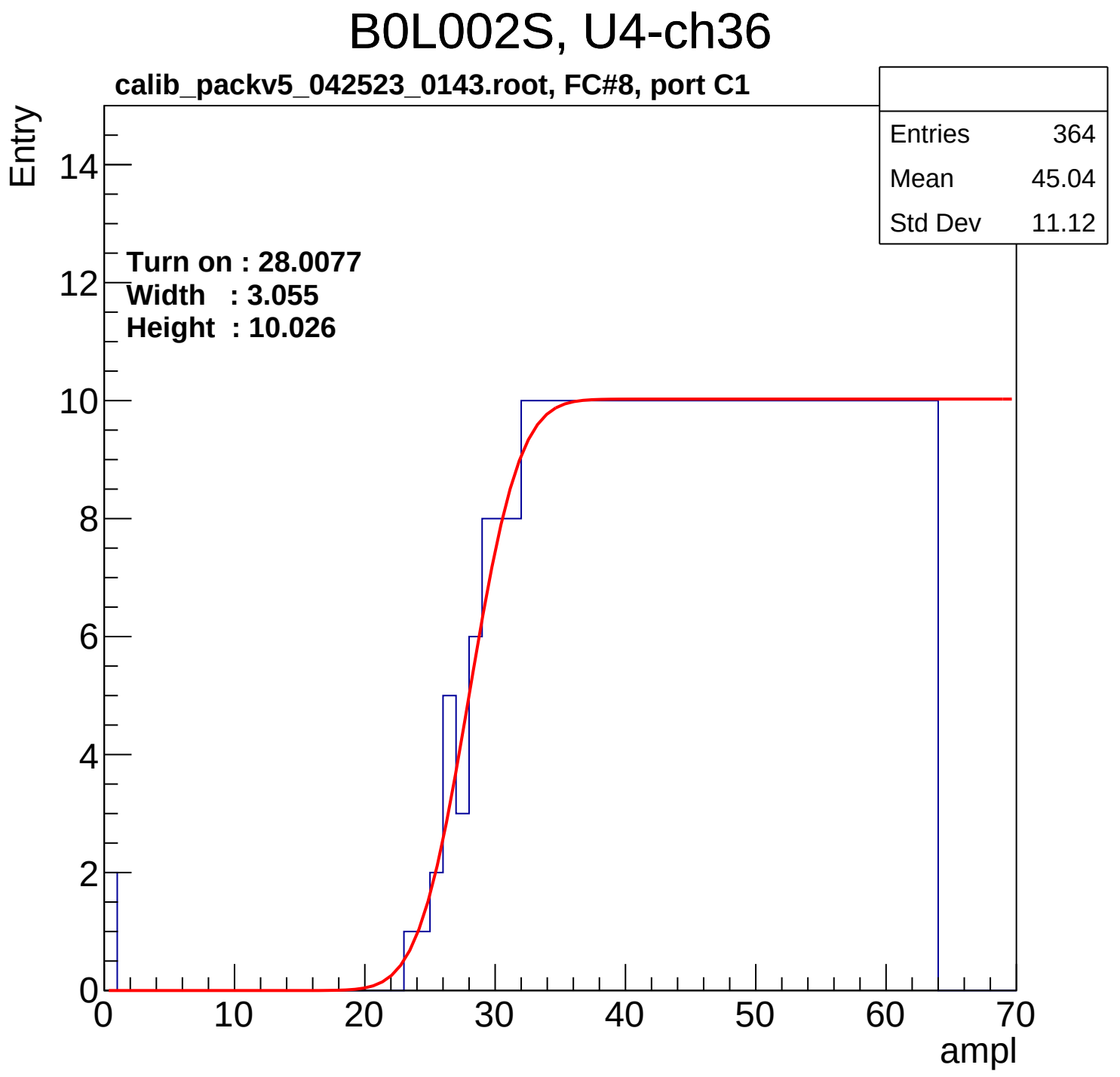

B0L002S, U4-ch31
calib_packv5_042523_0143.root, FC#8, port C1
Entries 380
Mean 44.15
Std Dev 11.84
Turn on : 26.1907
Width : 2.629
Height : 10.001
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

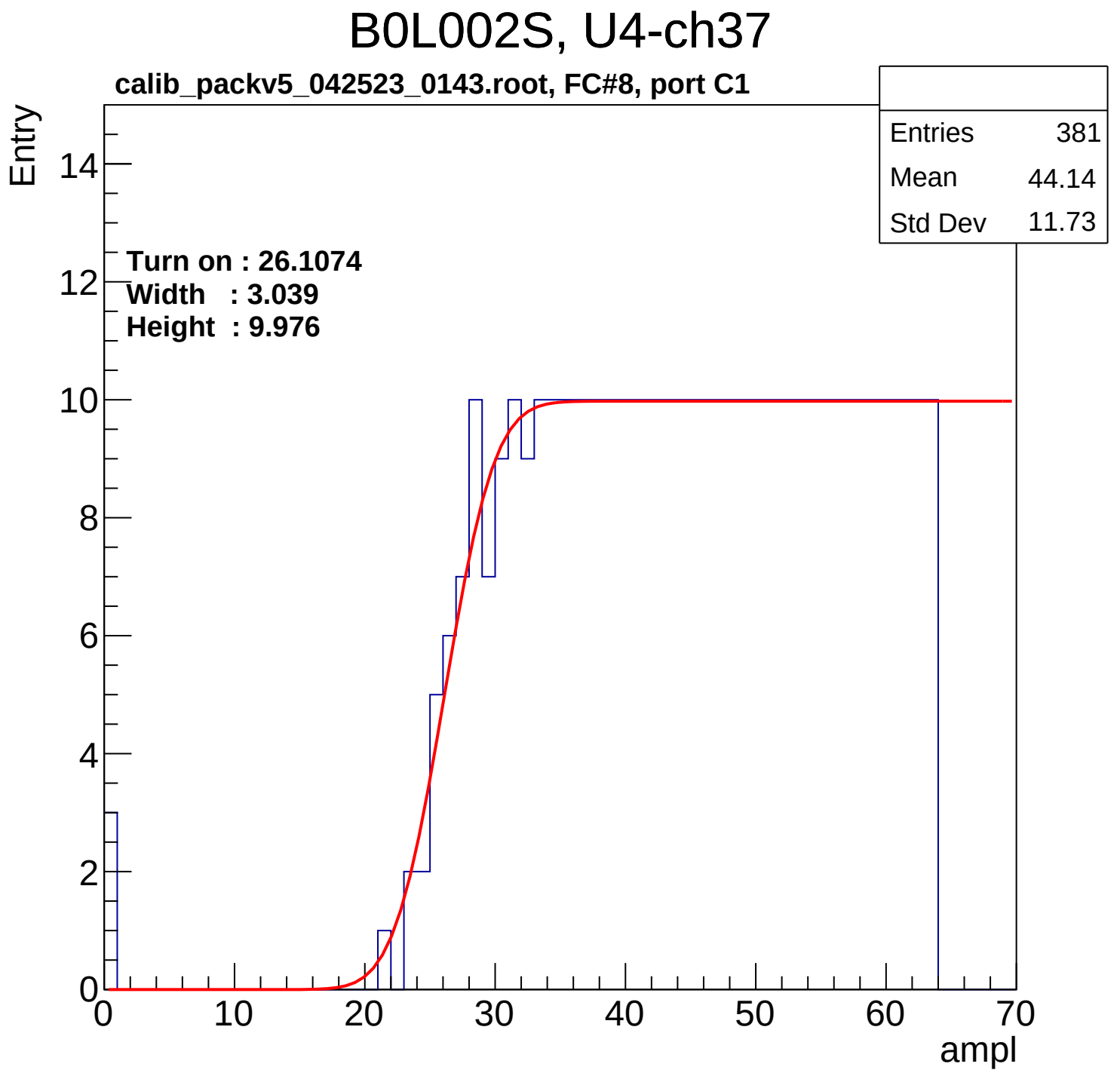

B0L002S, U4-ch32
calib_packv5_042523_0143.root, FC#8, port C1
Entries 363
Mean 45.06
Std Dev 11.24
Turn on : 28.3335
Width : 1.895
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

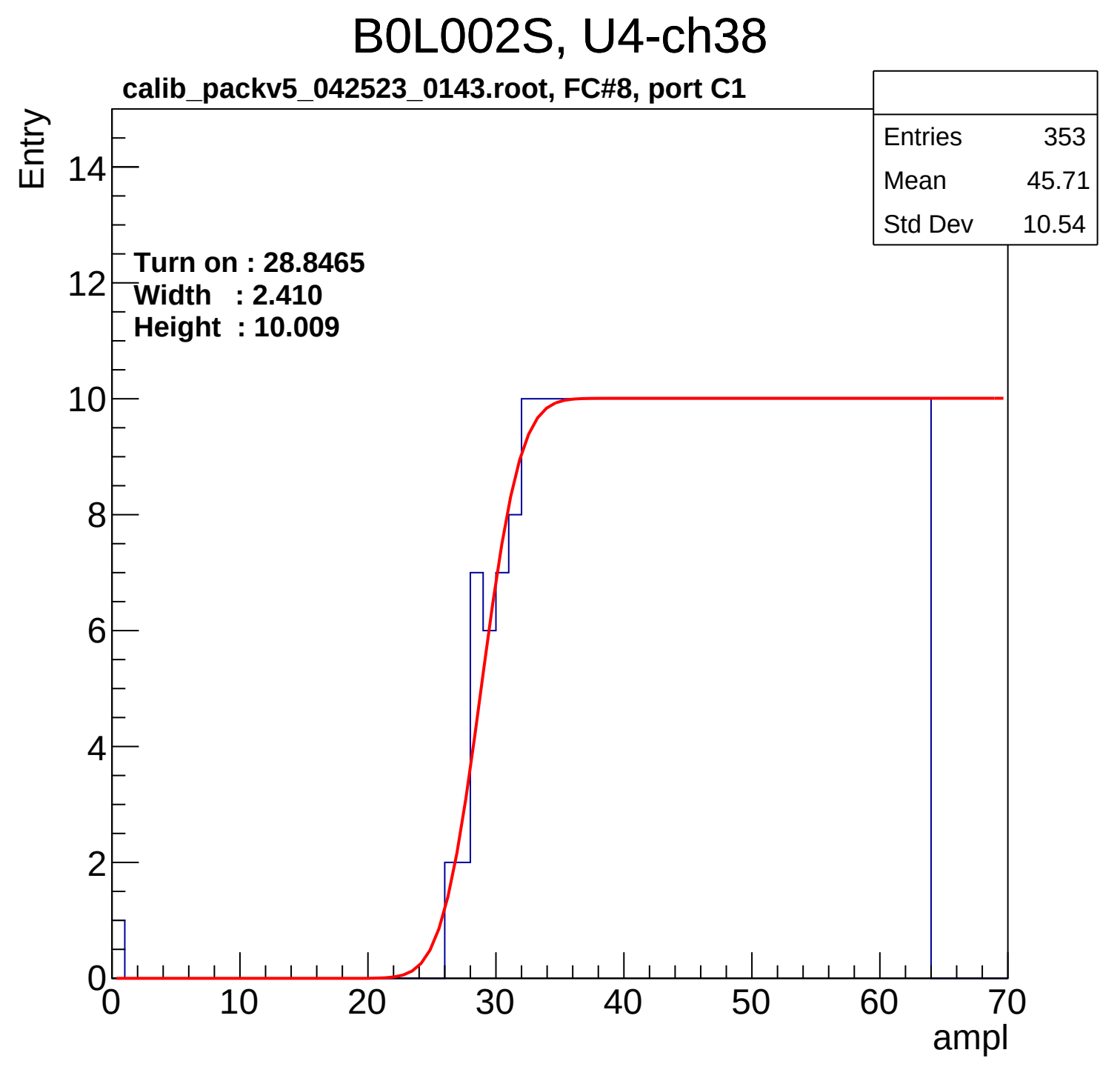

B0L002S, U4-ch33
calib_packv5_042523_0143.root, FC#8, port C1
Entries 379
Mean 44.4
Std Dev 11.27
Turn on : 26.1534
Width : 3.143
Height : 10.010
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

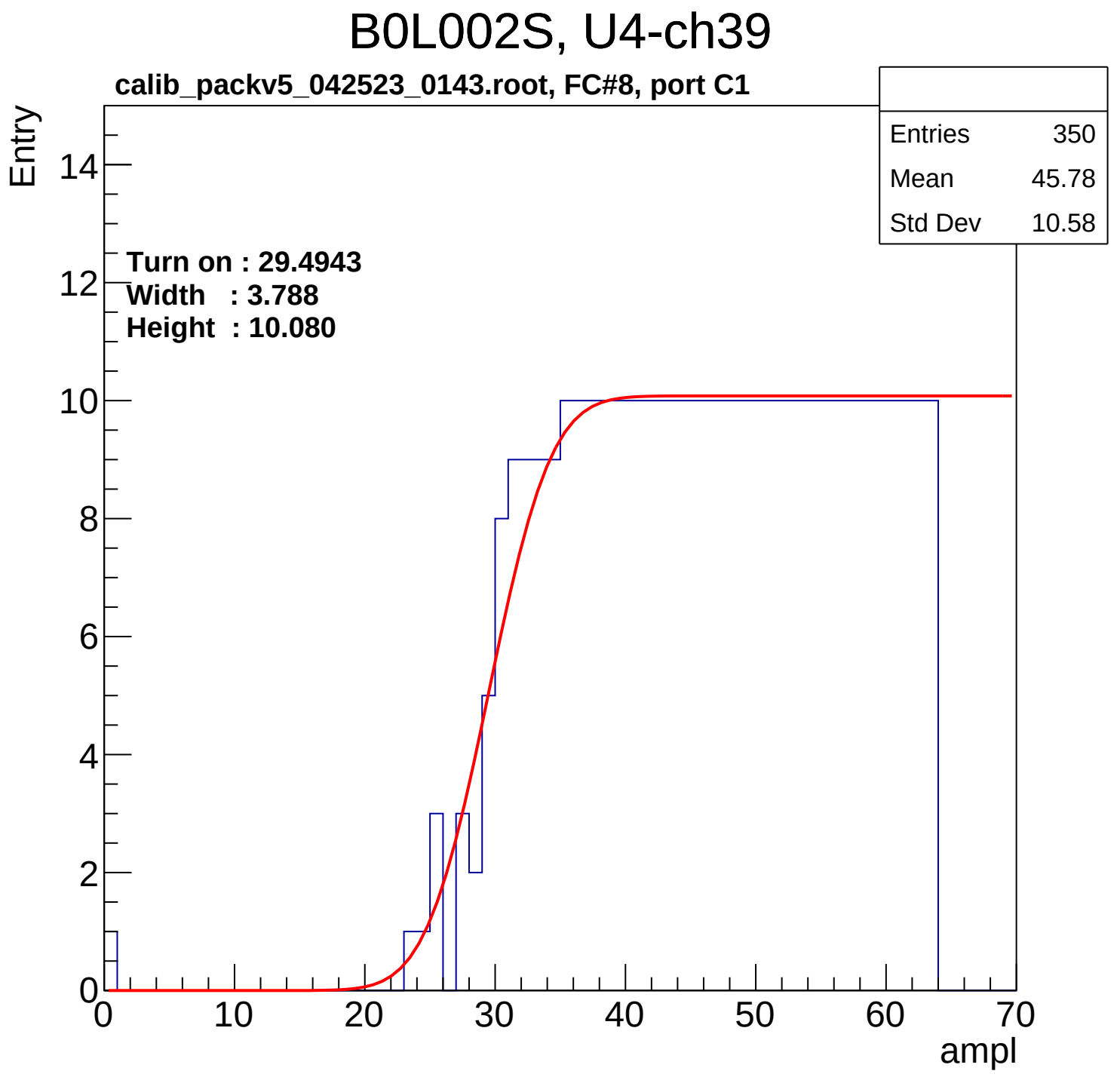

B0L002S, U4-ch34
calib_packv5_042523_0143.root, FC#8, port C1
Entries 386
Mean 43.8
Std Dev 12.15
Turn on : 24.9411
Width : 4.712
Height : 10.084
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

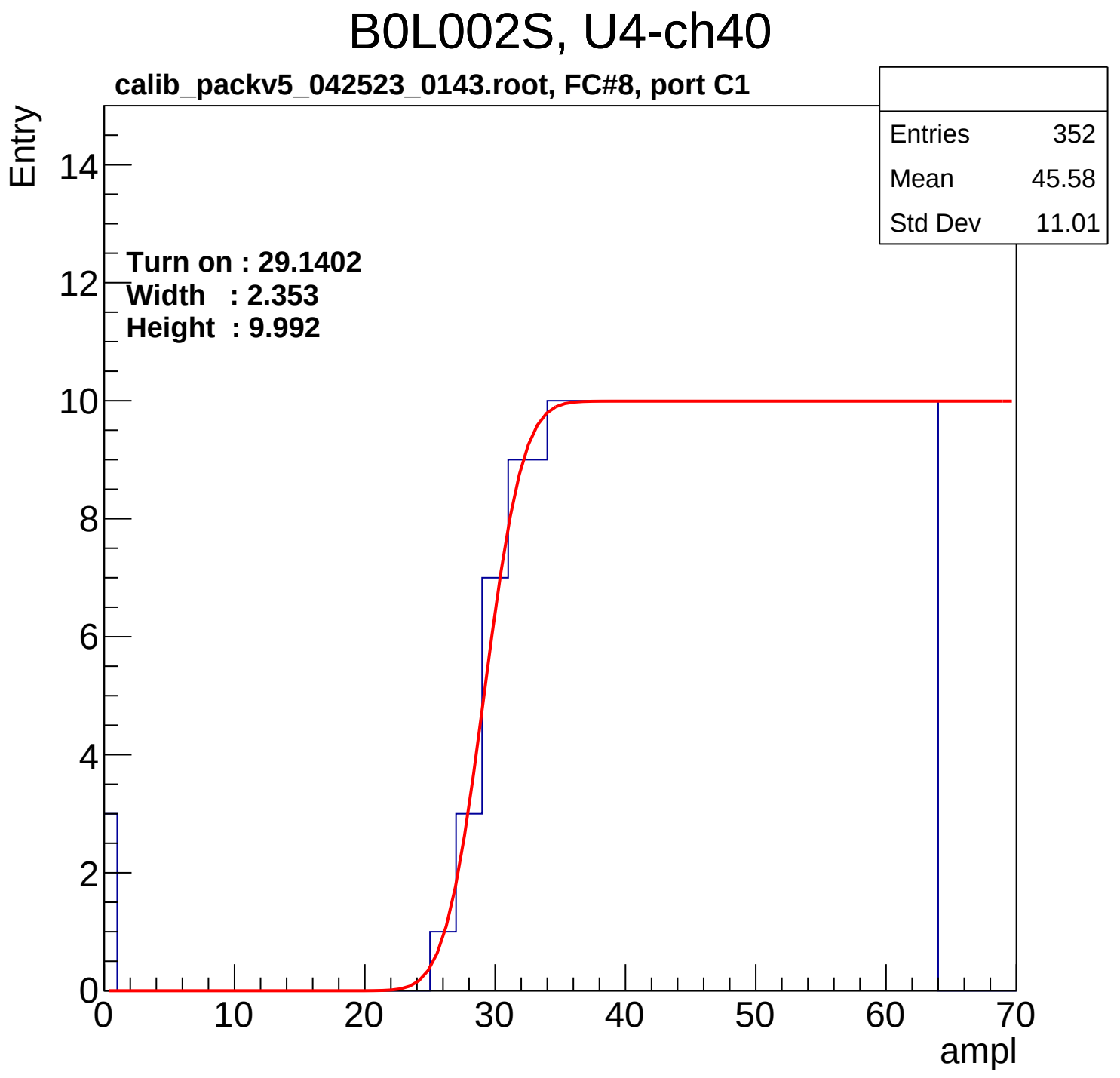

B0L002S, U4-ch35
calib_packv5_042523_0143.root, FC#8, port C1
Entries 357
Mean 45.39
Std Dev 10.94
Turn on : 28.6409
Width : 2.956
Height : 10.053
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

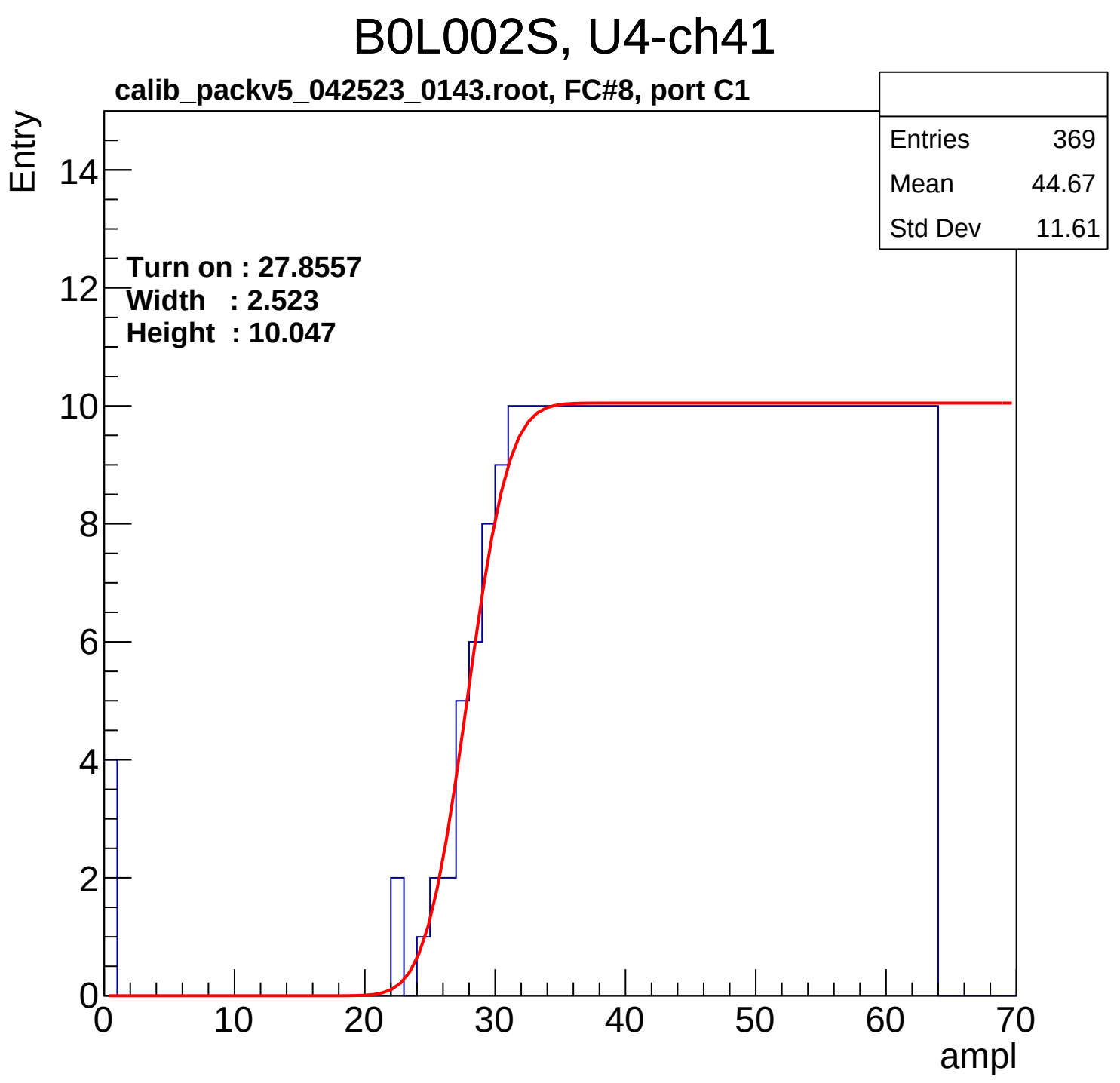

B0L002S, U4-ch36
calib_packv5_042523_0143.root, FC#8, port C1
Entries 364
Mean 45.04
Std Dev 11.12
Turn on : 28.0077
Width : 3.055
Height : 10.026
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

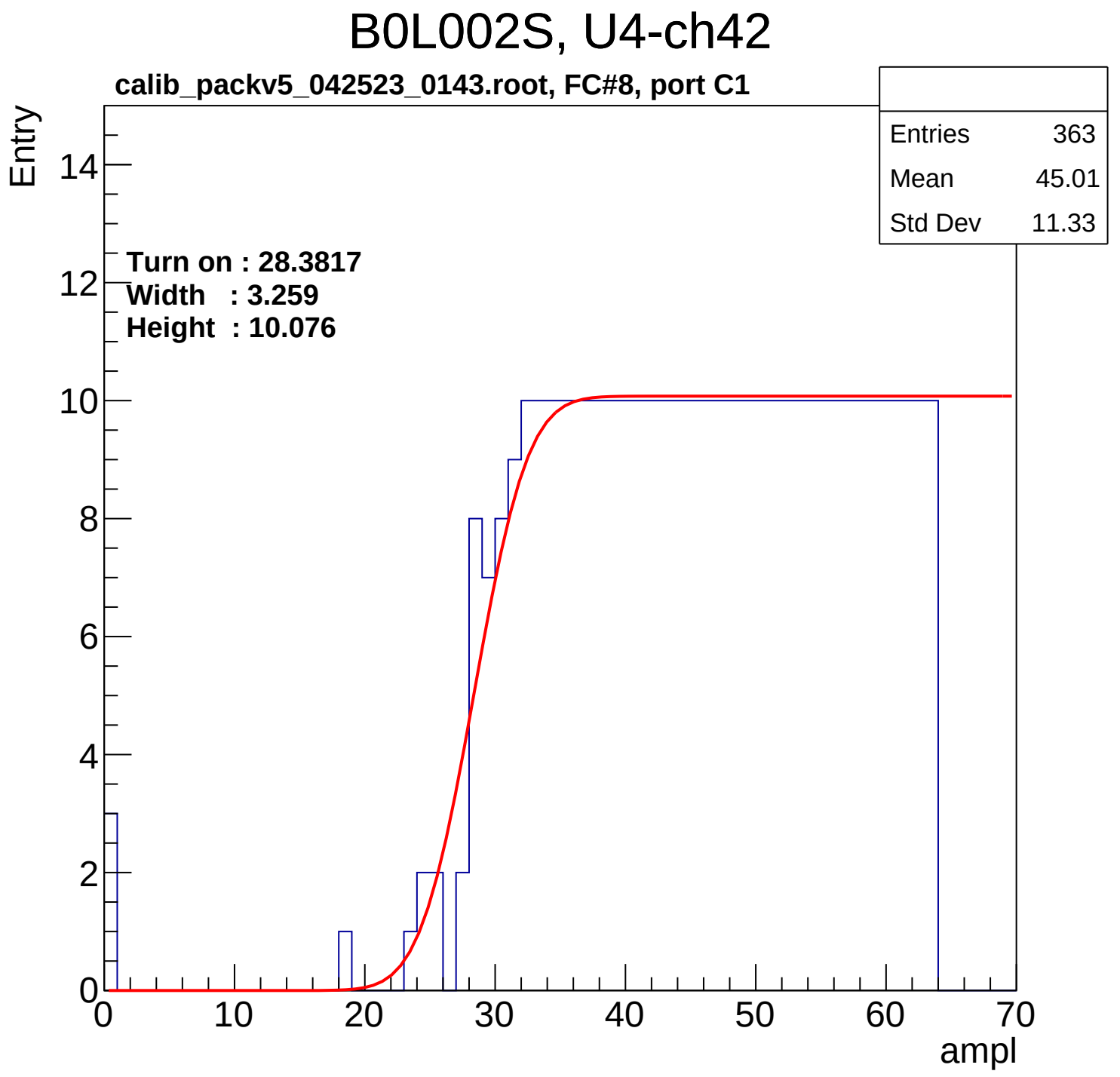

B0L002S, U4-ch37
calib_packv5_042523_0143.root, FC#8, port C1
Entries 381
Mean 44.14
Std Dev 11.73
Turn on : 26.1074
Width : 3.039
Height : 9.976
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

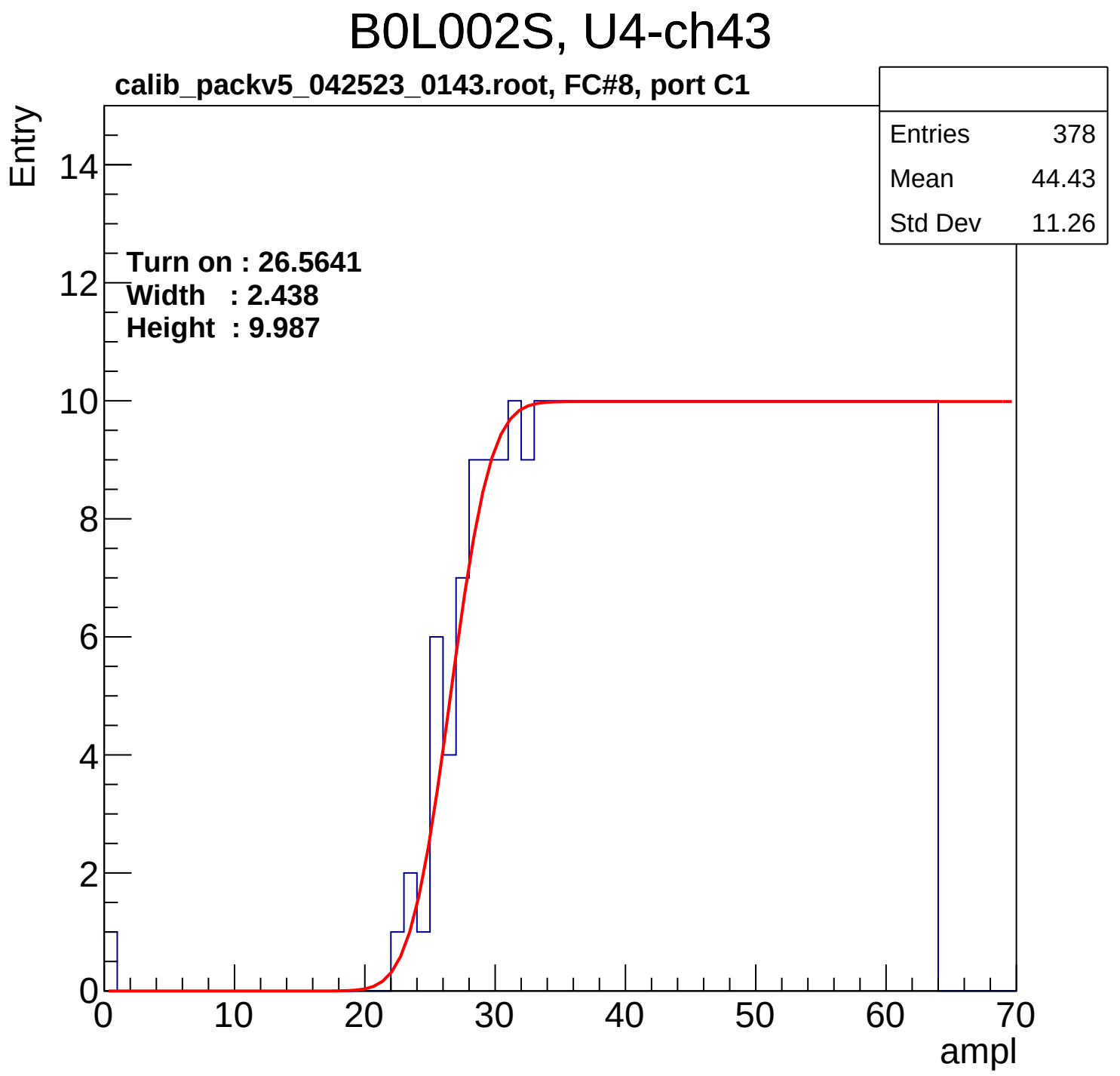

B0L002S, U4-ch38
calib_packv5_042523_0143.root, FC#8, port C1
Entries 353
Mean 45.71
Std Dev 10.54
Turn on : 28.8465
Width : 2.410
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

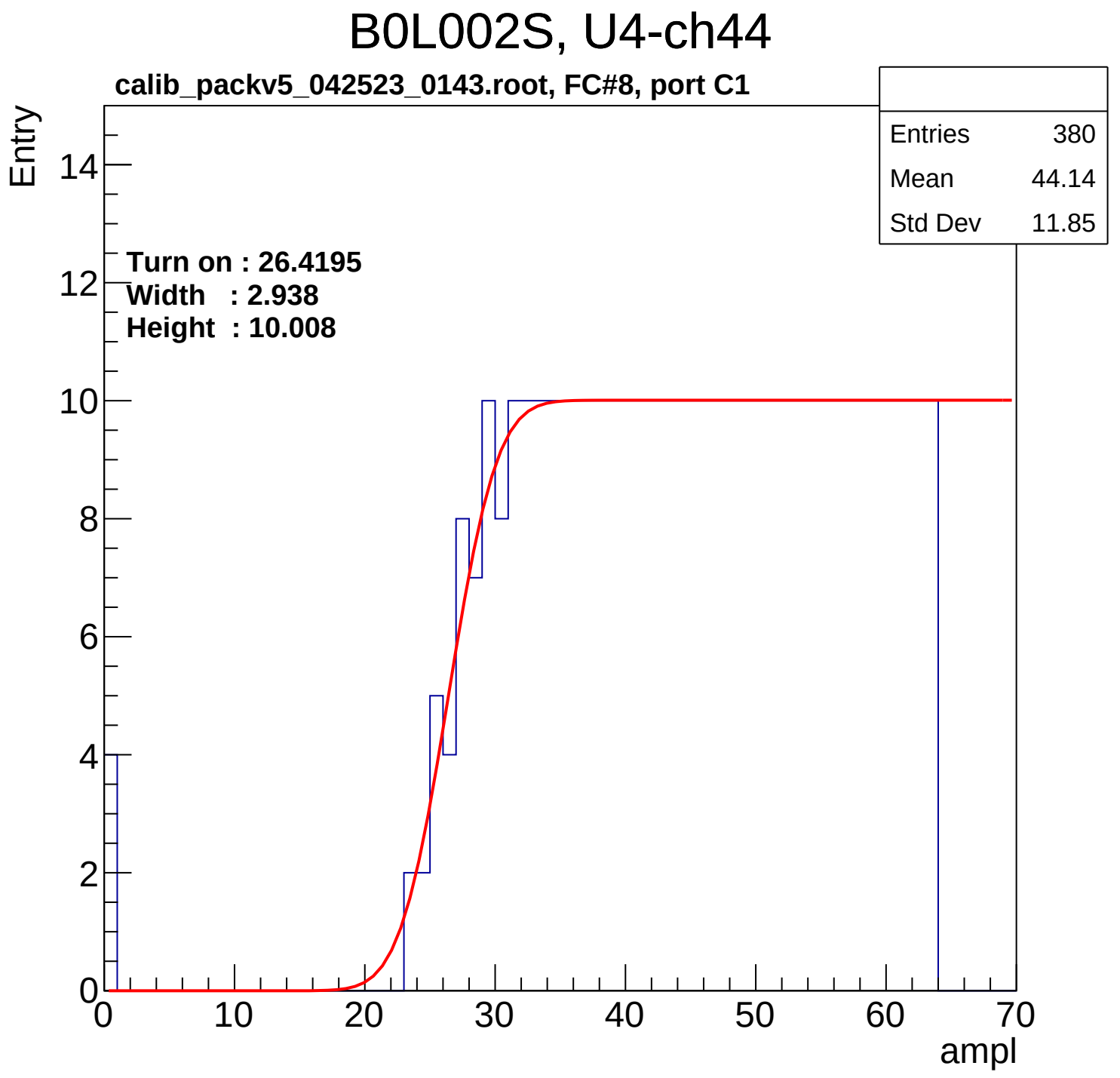

B0L002S, U4-ch39
calib_packv5_042523_0143.root, FC#8, port C1
Entries 350
Mean 45.78
Std Dev 10.58
Turn on : 29.4943
Width : 3.788
Height : 10.080
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

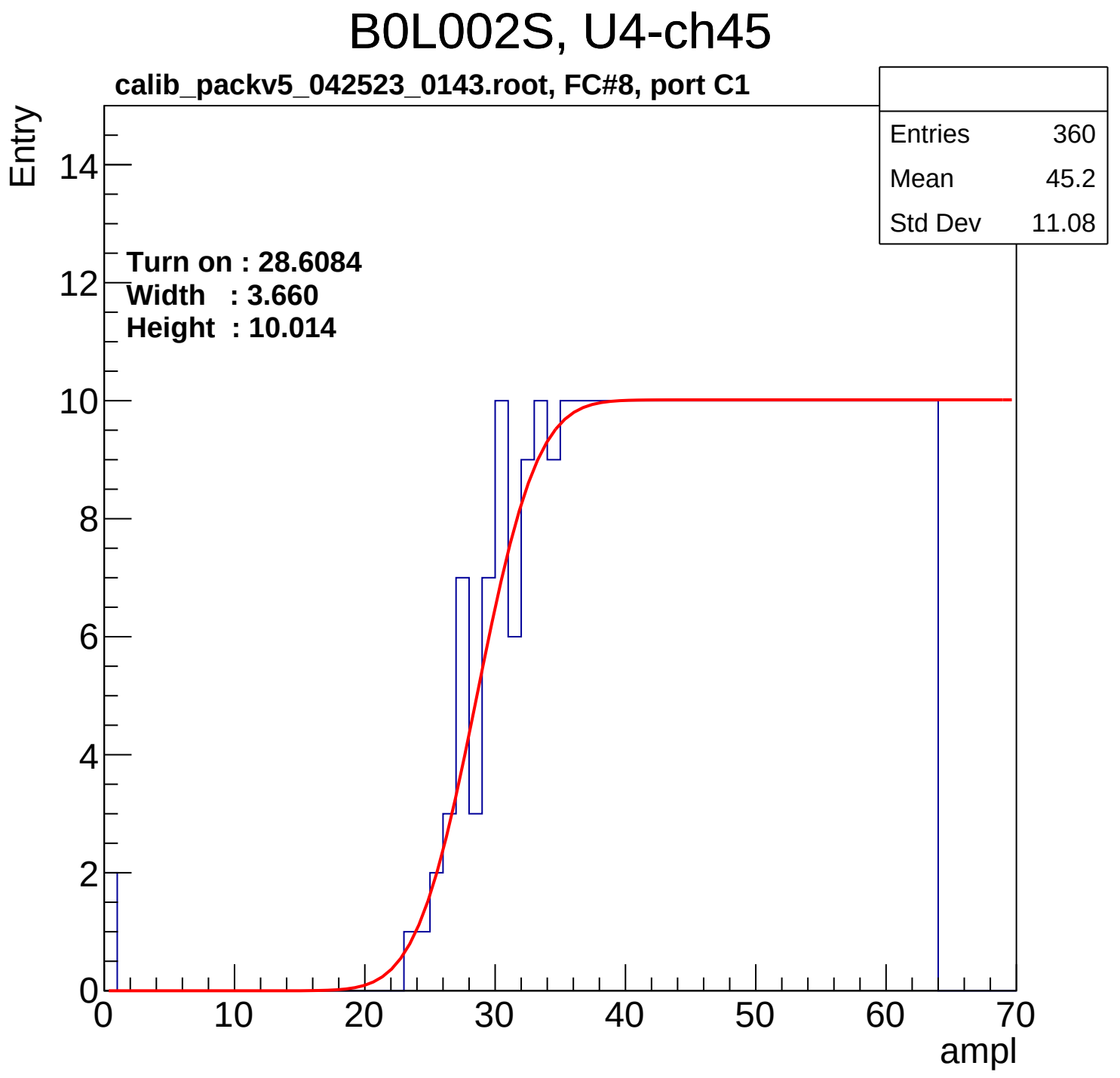

B0L002S, U4-ch40
calib_packv5_042523_0143.root, FC#8, port C1
Entries 352
Mean 45.58
Std Dev 11.01
Turn on : 29.1402
Width : 2.353
Height : 9.992
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

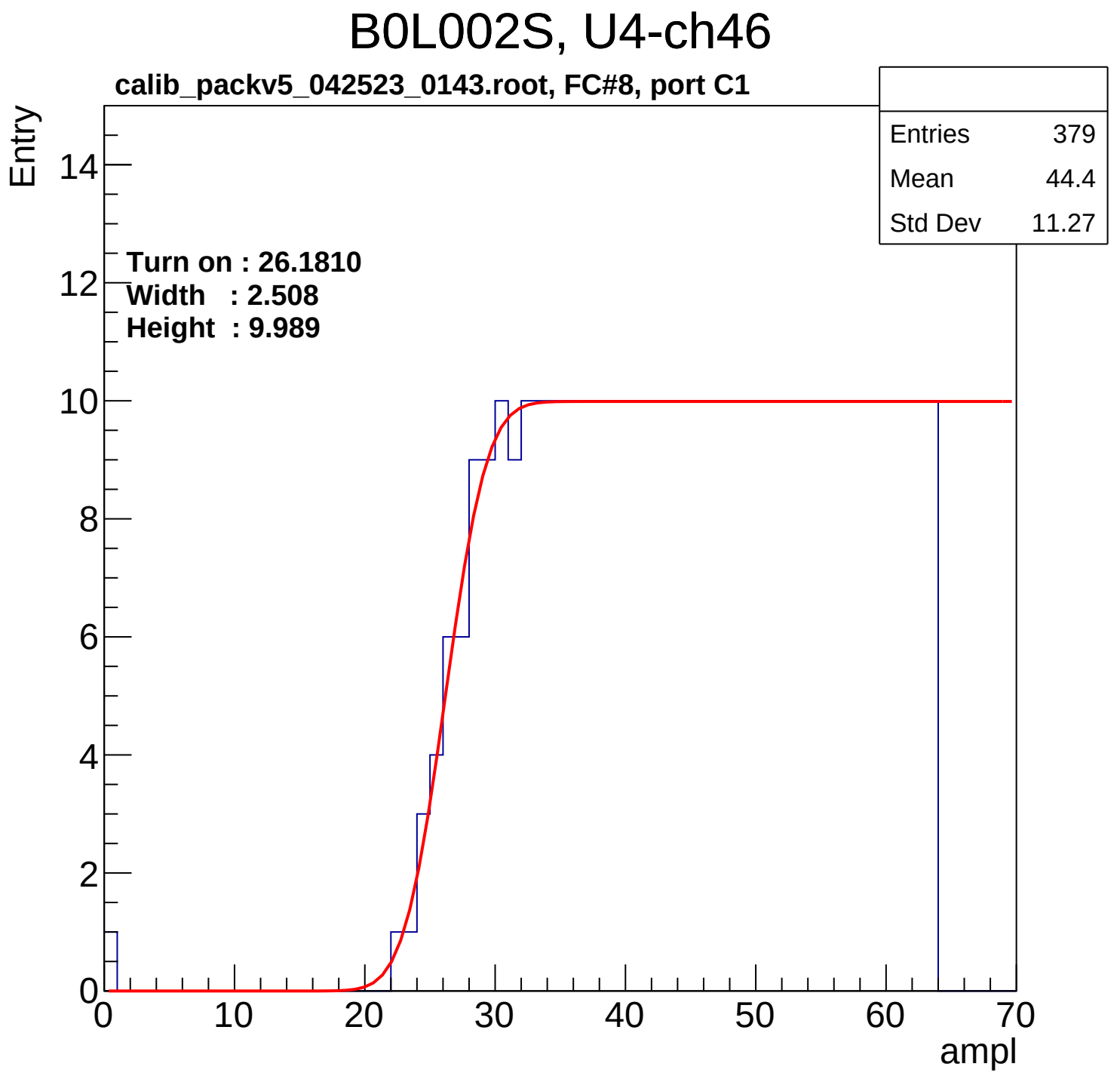

B0L002S, U4-ch41
calib_packv5_042523_0143.root, FC#8, port C1
Entries 369
Mean 44.67
Std Dev 11.61
Turn on : 27.8557
Width : 2.523
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

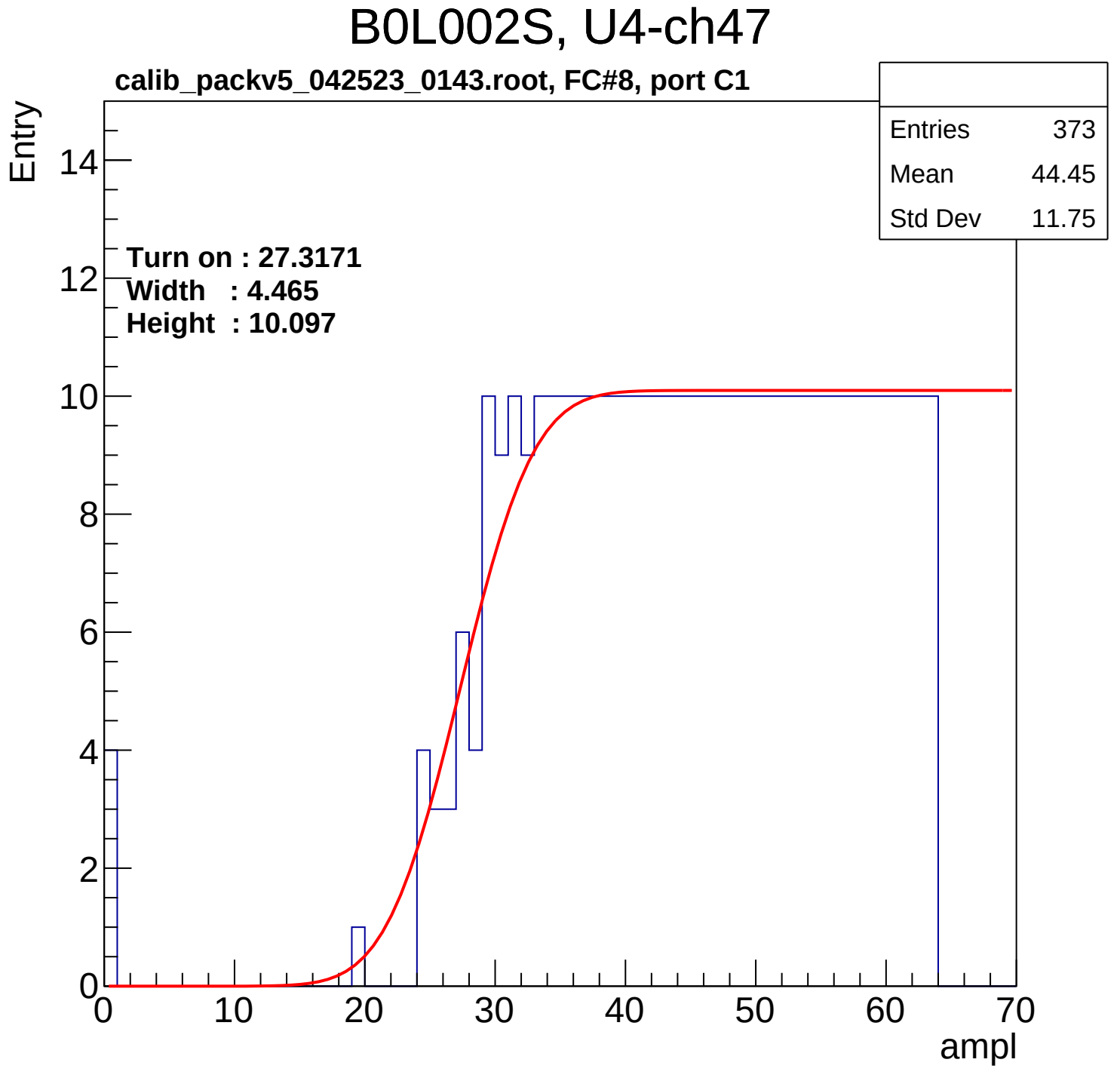

B0L002S, U4-ch42
calib_packv5_042523_0143.root, FC#8, port C1
Entries 363
Mean 45.01
Std Dev 11.33
Turn on : 28.3817
Width : 3.259
Height : 10.076
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

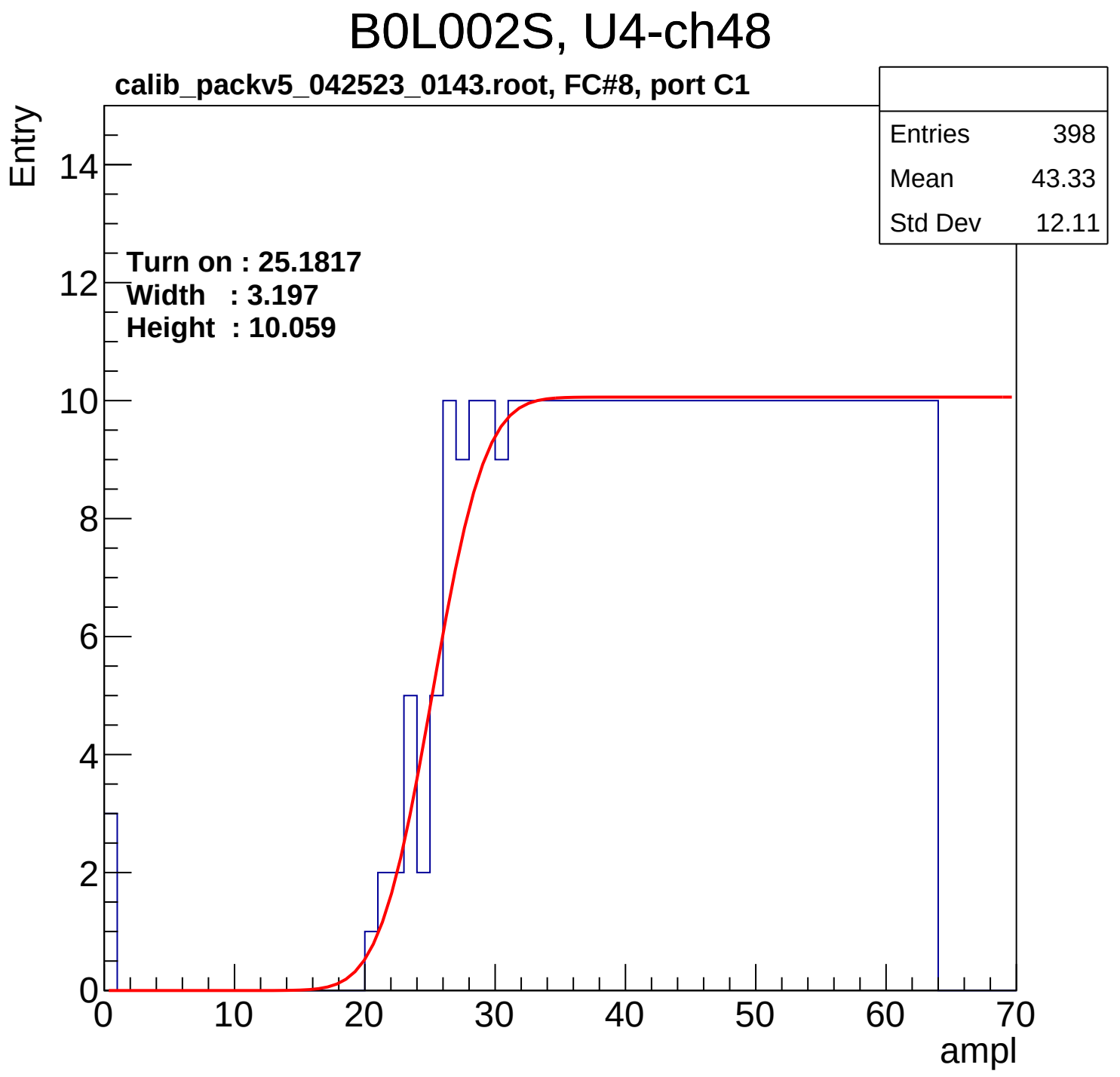

B0L002S, U4-ch43
calib_packv5_042523_0143.root, FC#8, port C1
Entries 378
Mean 44.43
Std Dev 11.26
Turn on : 26.5641
Width : 2.438
Height : 9.987
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

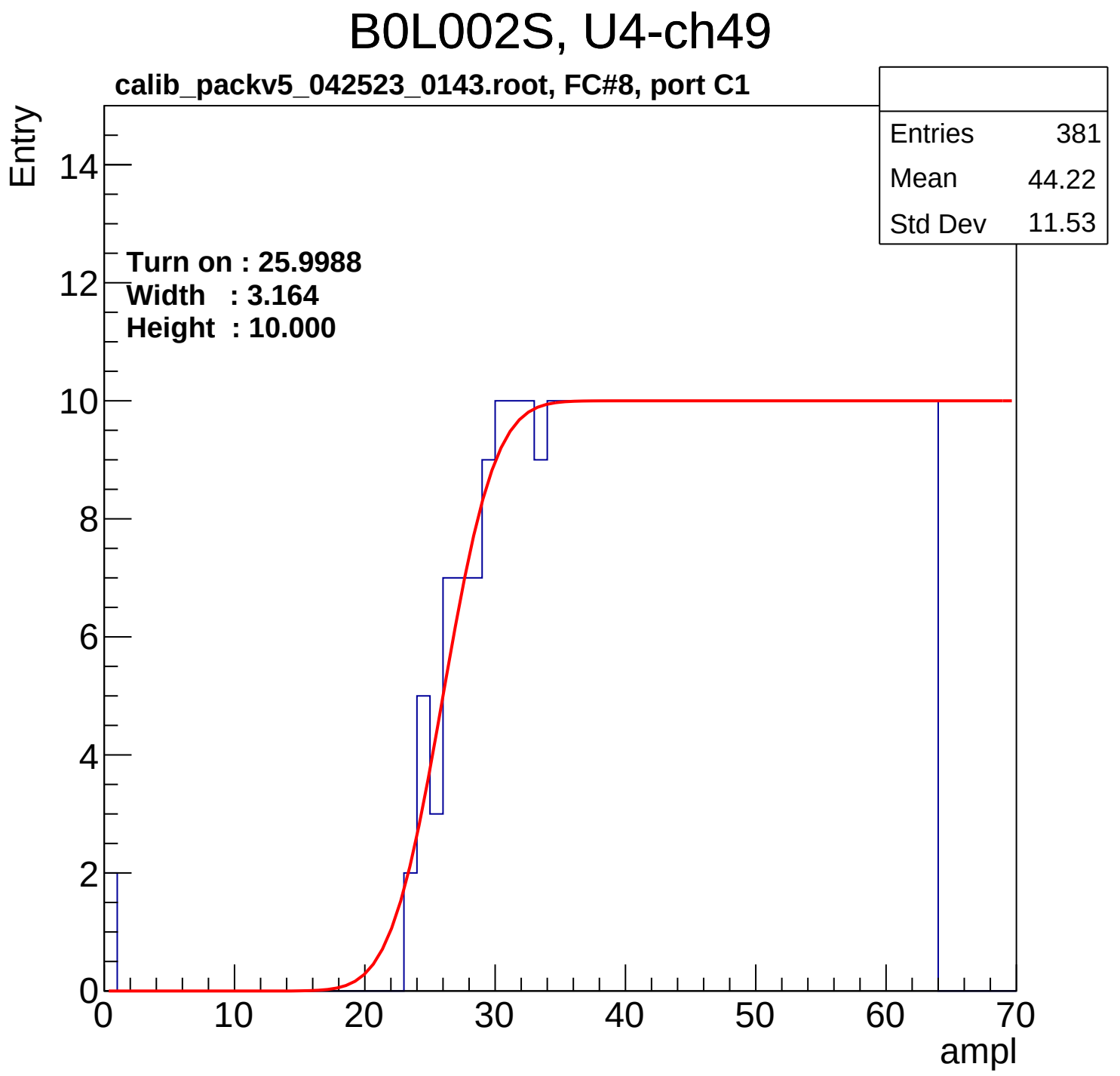

B0L002S, U4-ch44
calib_packv5_042523_0143.root, FC#8, port C1
Entries 380
Mean 44.14
Std Dev 11.85
Turn on : 26.4195
Width : 2.938
Height : 10.008
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

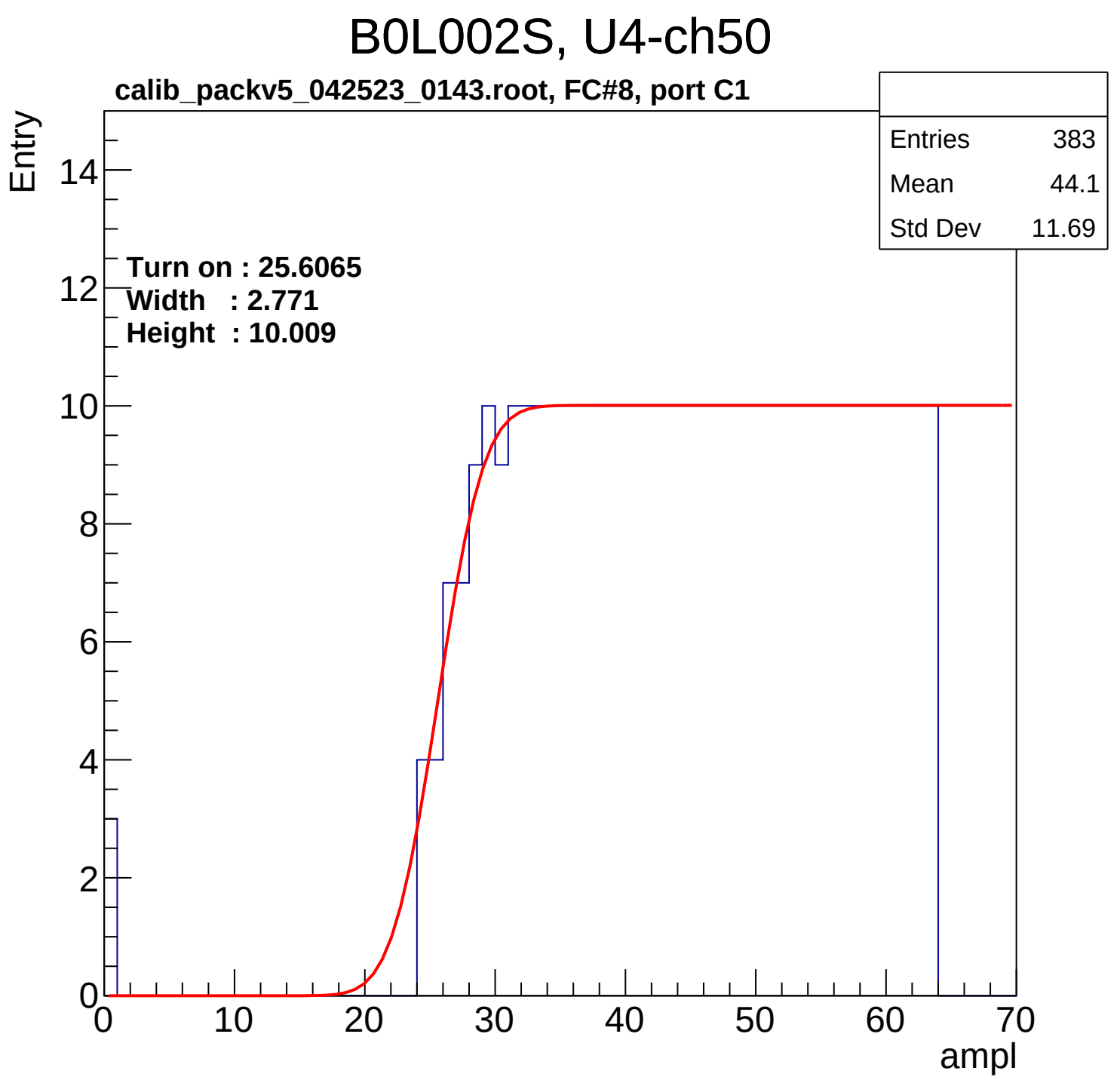

B0L002S, U4-ch45
calib_packv5_042523_0143.root, FC#8, port C1
Entries 360
Mean 45.2
Std Dev 11.08
Turn on : 28.6084
Width : 3.660
Height : 10.014
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

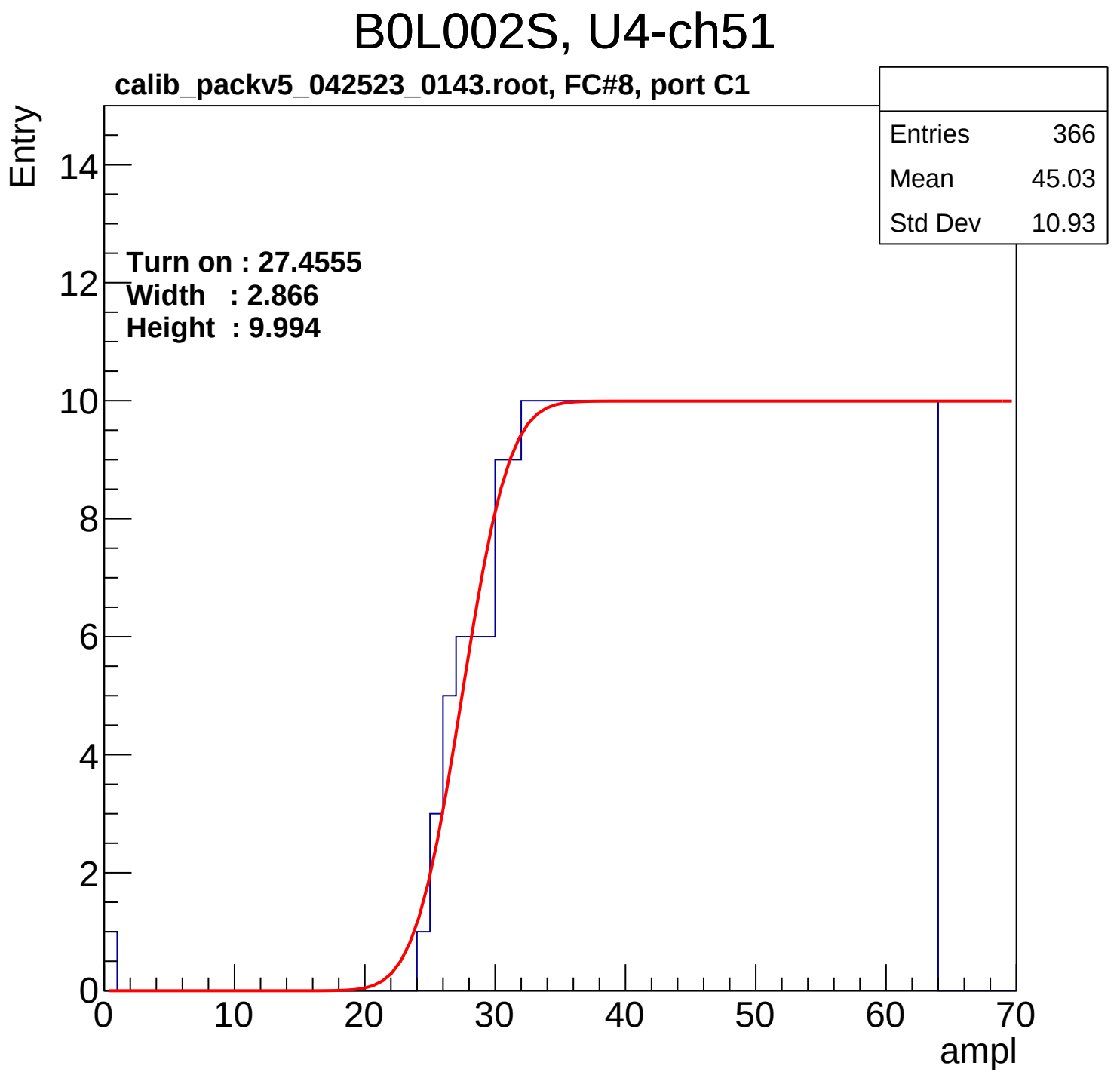

B0L002S, U4-ch46
calib_packv5_042523_0143.root, FC#8, port C1
Entries 379
Mean 44.4
Std Dev 11.27
Turn on : 26.1810
Width : 2.508
Height : 9.989
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

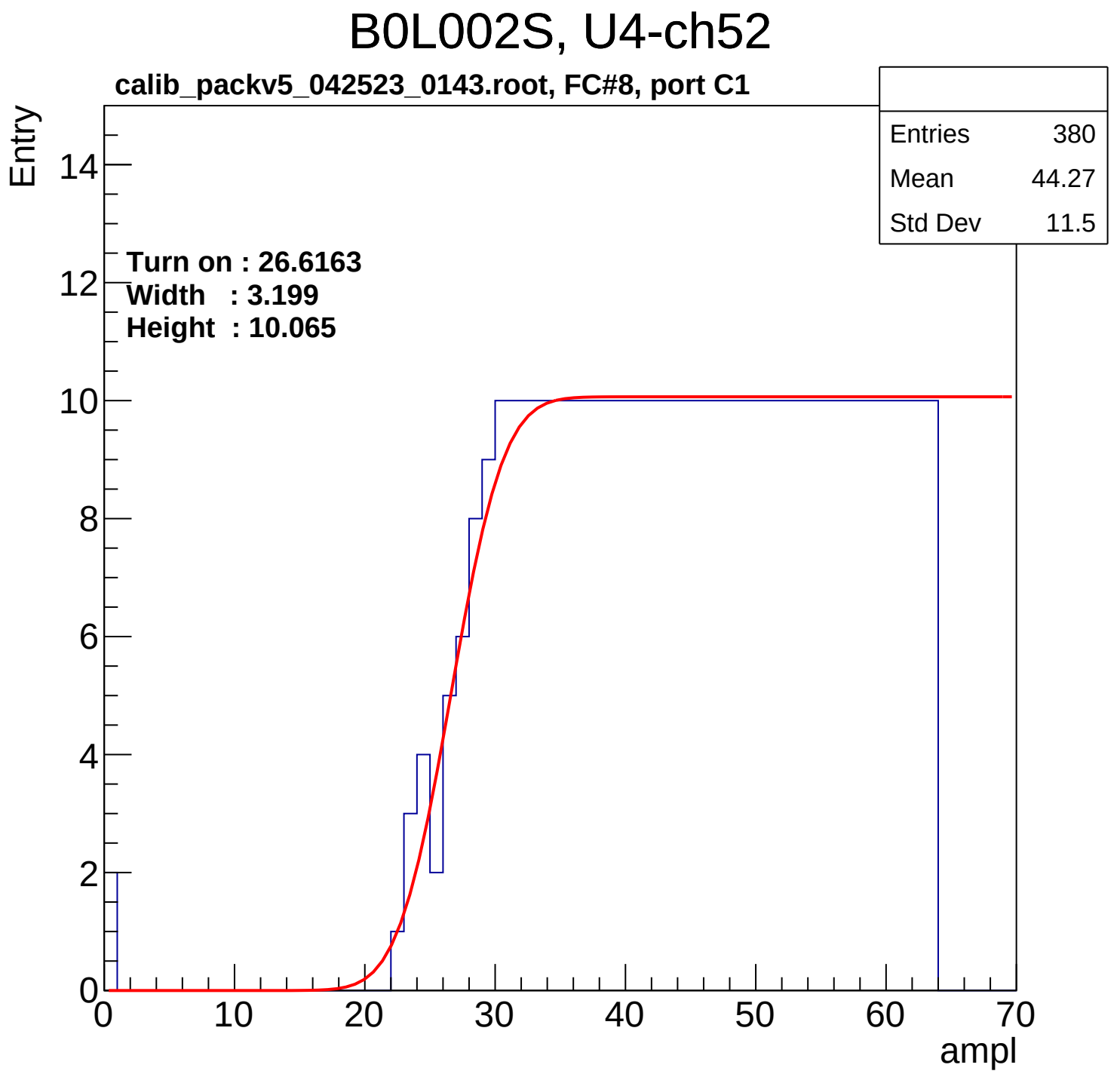

B0L002S, U4-ch47
calib_packv5_042523_0143.root, FC#8, port C1
Entries 373
Mean 44.45
Std Dev 11.75
Turn on : 27.3171
Width : 4.465
Height : 10.097
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

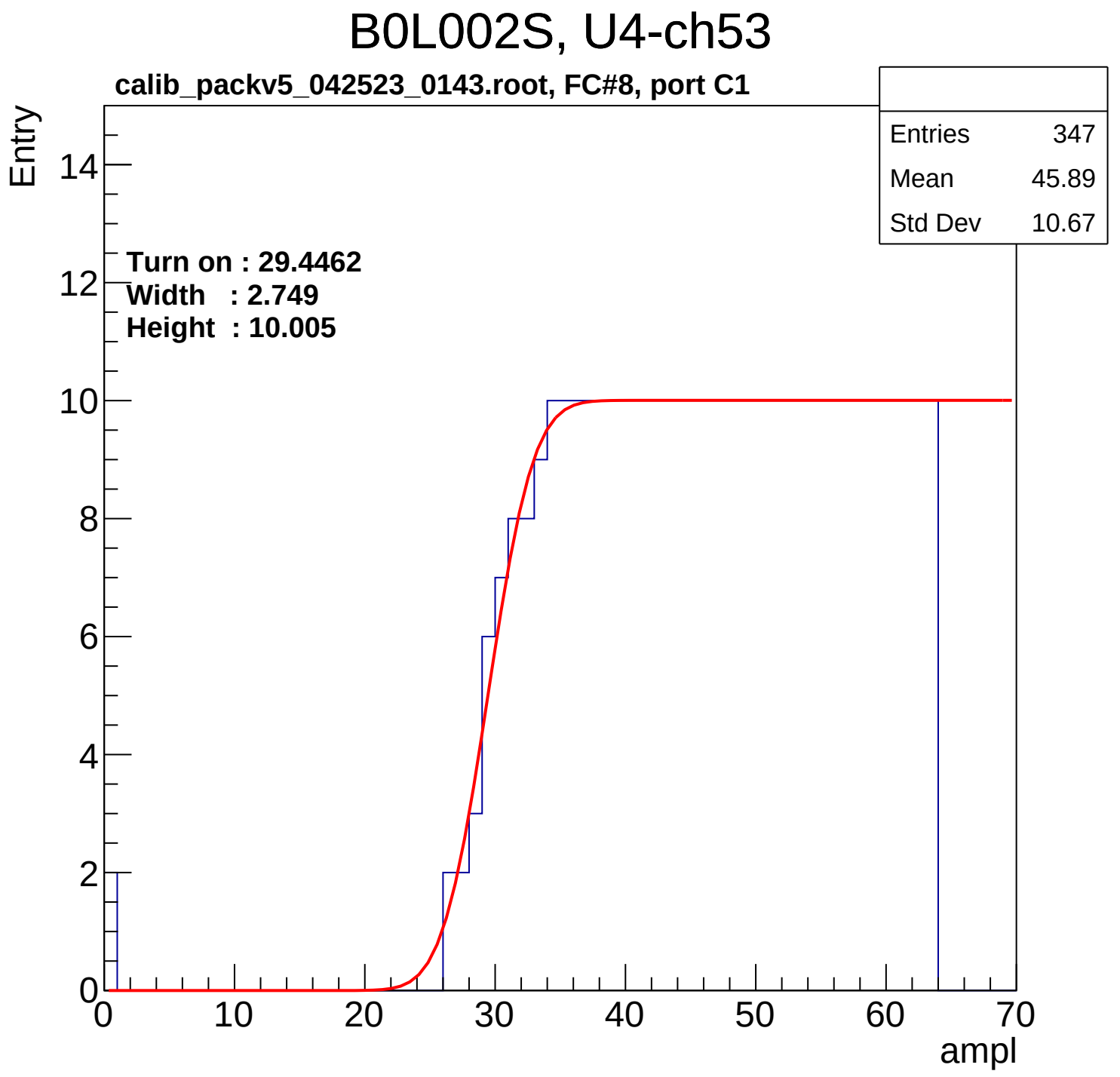

B0L002S, U4-ch48
calib_packv5_042523_0143.root, FC#8, port C1
Entries 398
Mean 43.33
Std Dev 12.11
Turn on : 25.1817
Width : 3.197
Height : 10.059
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

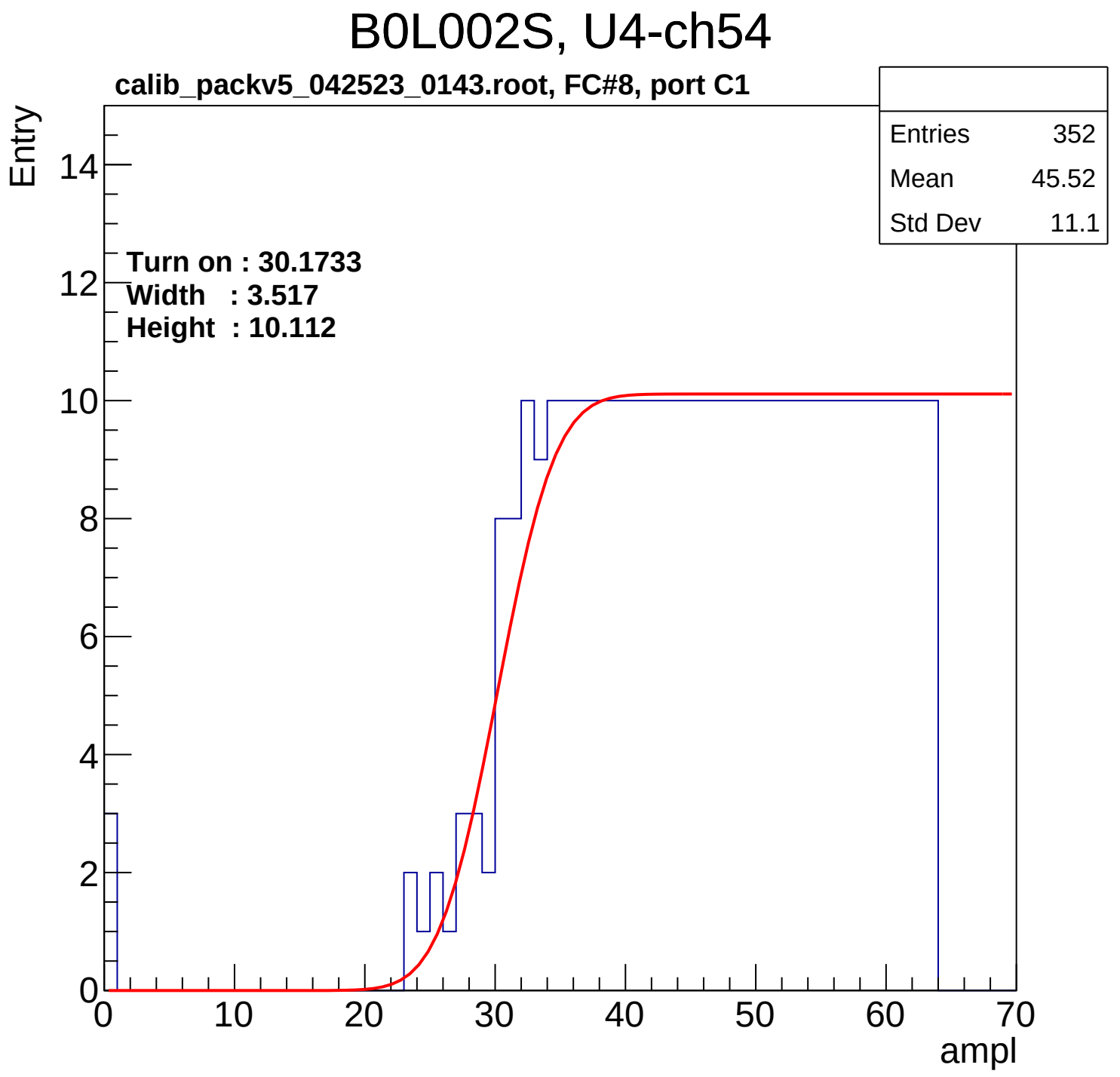

B0L002S, U4-ch49
calib_packv5_042523_0143.root, FC#8, port C1
Entries 381
Mean 44.22
Std Dev 11.53
Turn on : 25.9988
Width : 3.164
Height : 10.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

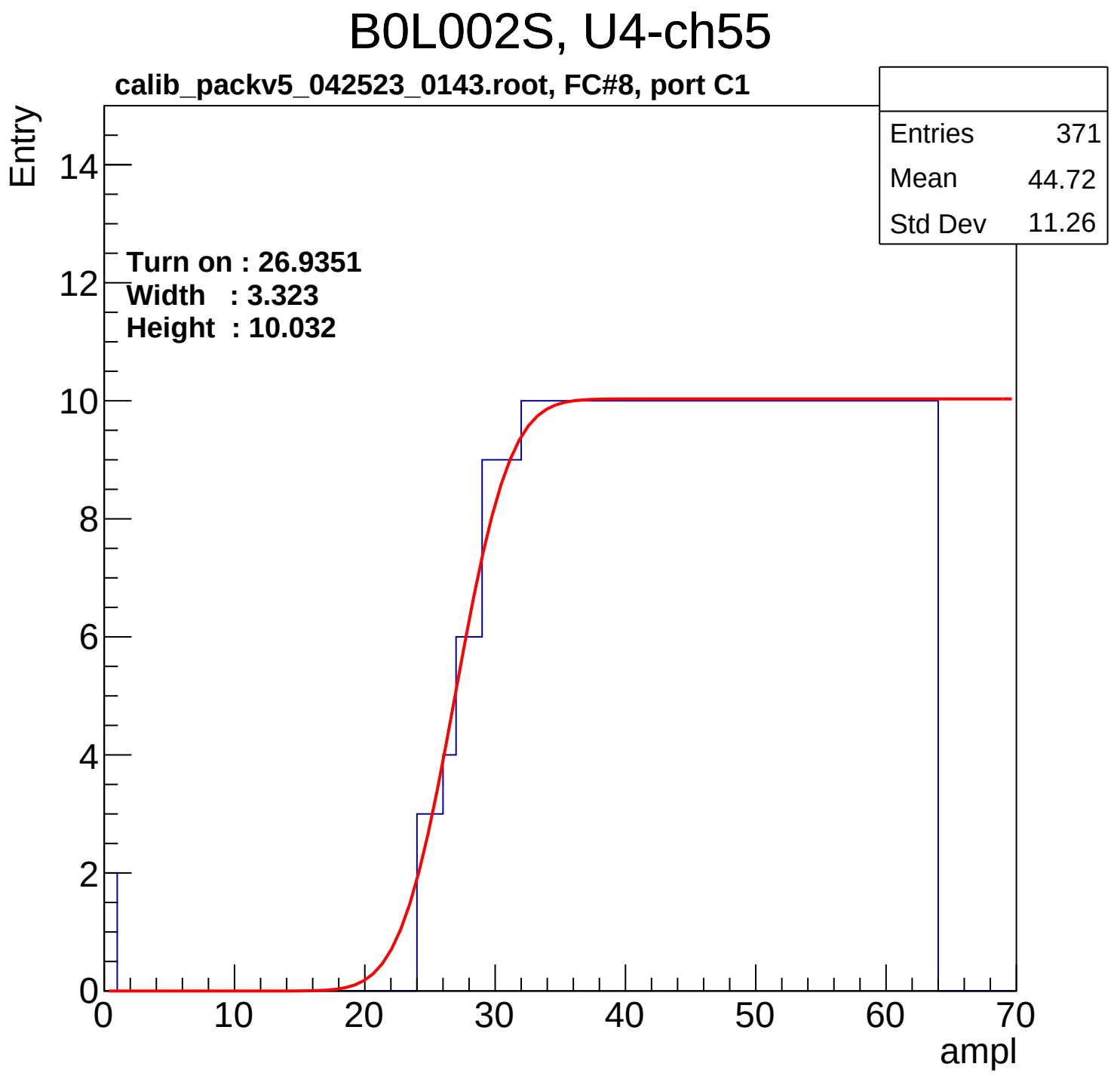

B0L002S, U4-ch50
calib_packv5_042523_0143.root, FC#8, port C1
Entries 383
Mean 44.1
Std Dev 11.69
Turn on : 25.6065
Width : 2.771
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

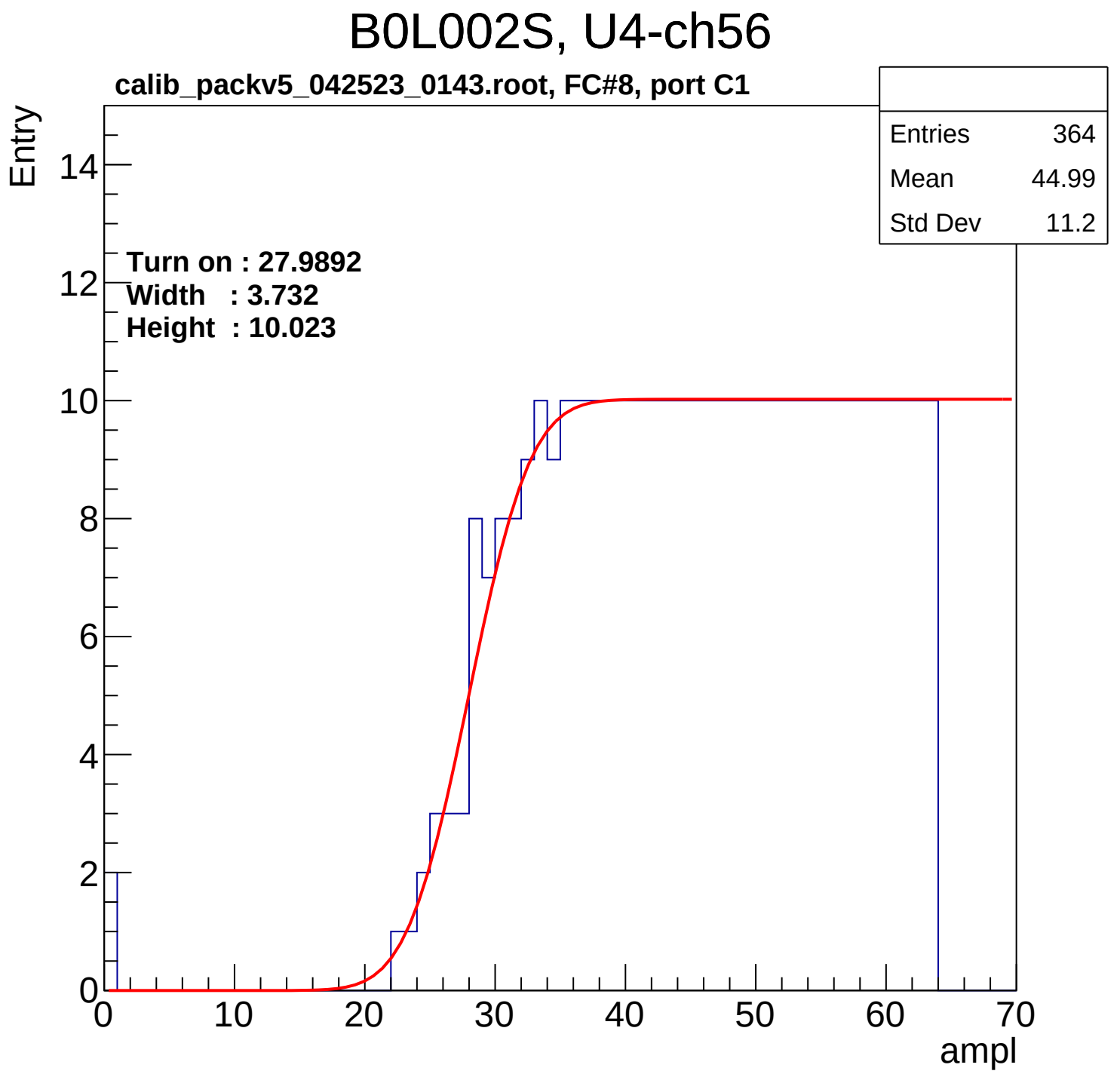

B0L002S, U4-ch51
calib_packv5_042523_0143.root, FC#8, port C1
Entries 366
Mean 45.03
Std Dev 10.93
Turn on : 27.4555
Width : 2.866
Height : 9.994
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

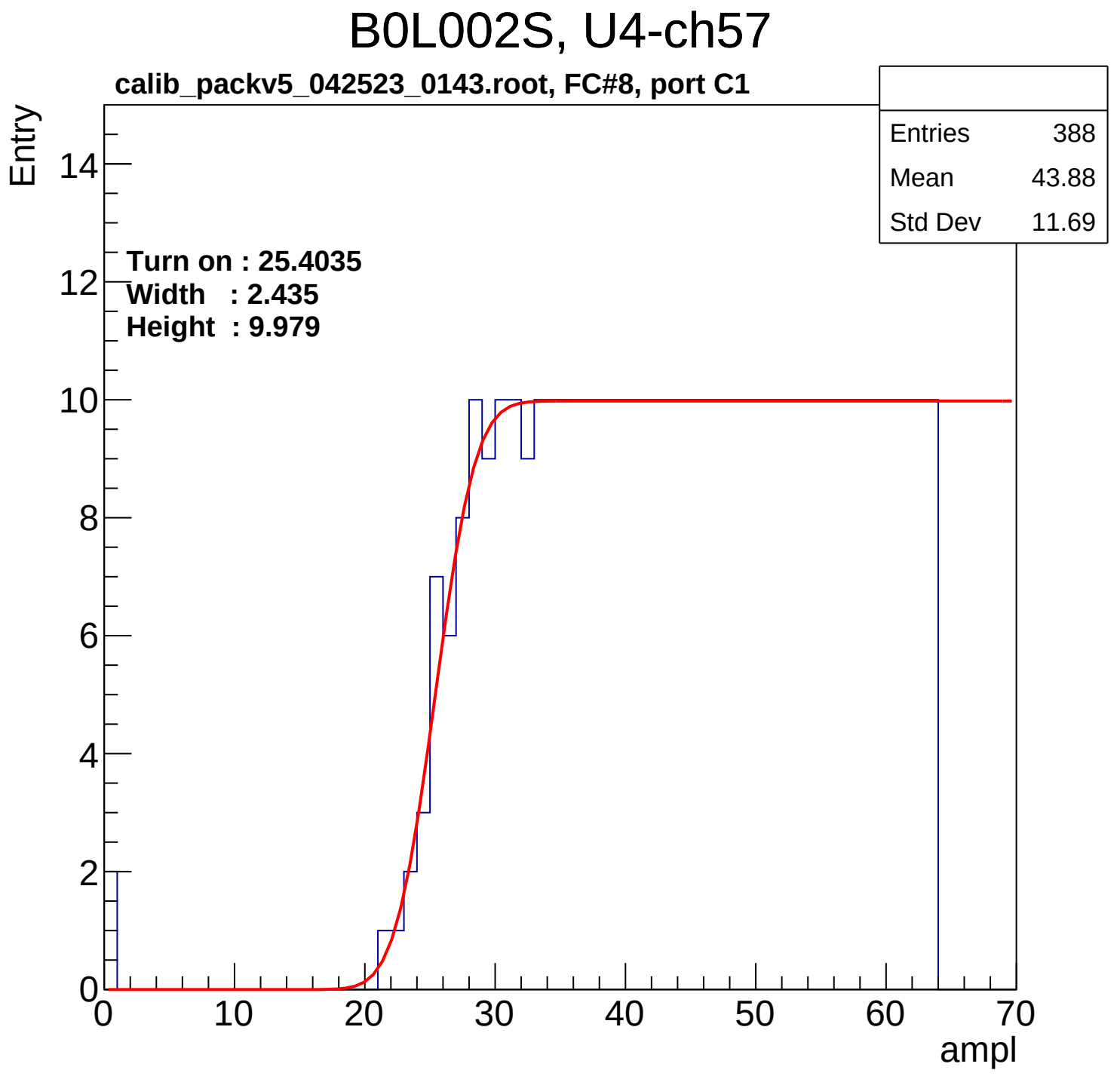

B0L002S, U4-ch52
calib_packv5_042523_0143.root, FC#8, port C1
Entries 380
Mean 44.27
Std Dev 11.5
Turn on : 26.6163
Width : 3.199
Height : 10.065
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

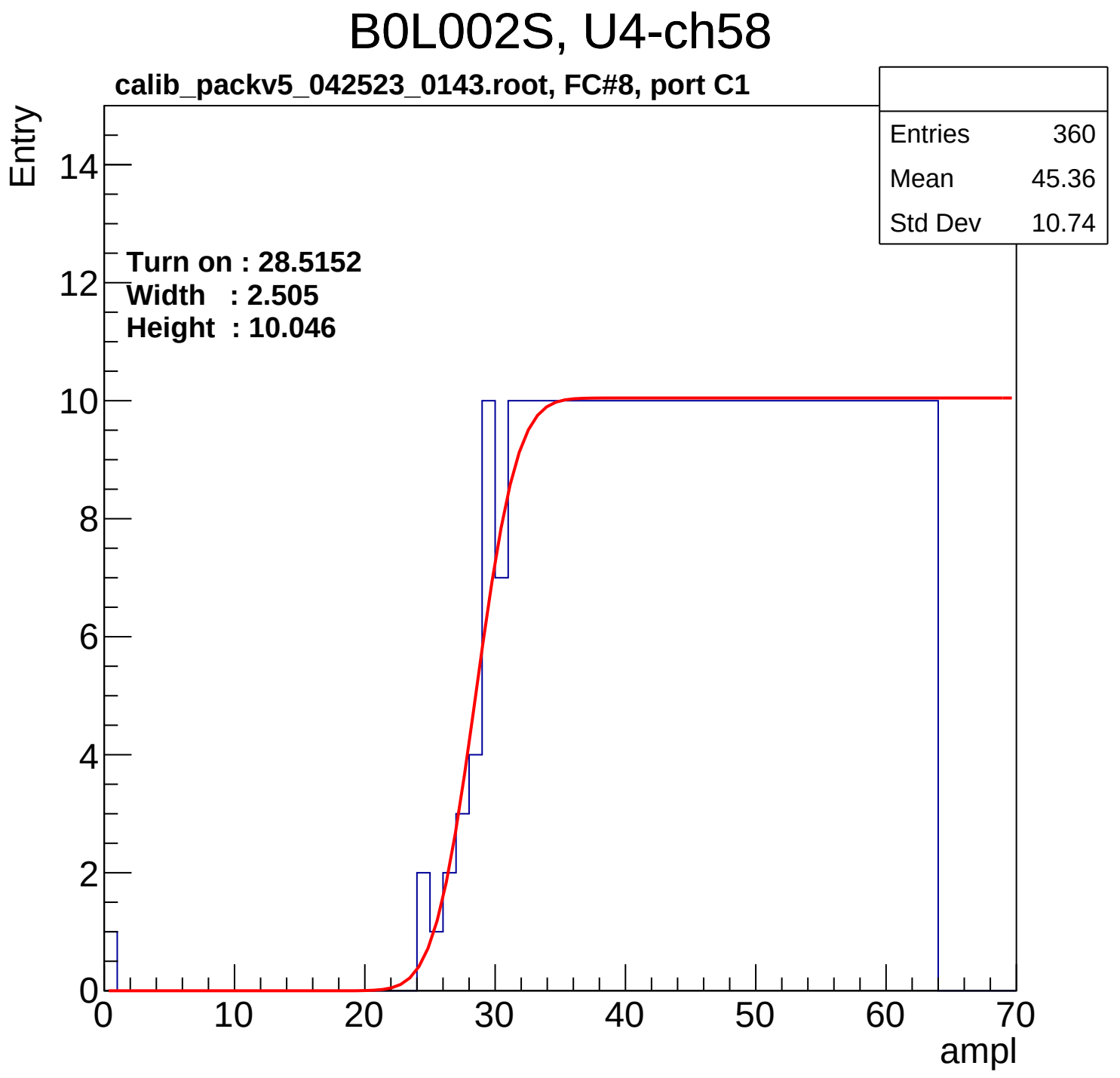

B0L002S, U4-ch53
calib_packv5_042523_0143.root, FC#8, port C1
Entries 347
Mean 45.89
Std Dev 10.67
Turn on : 29.4462
Width : 2.749
Height : 10.005
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

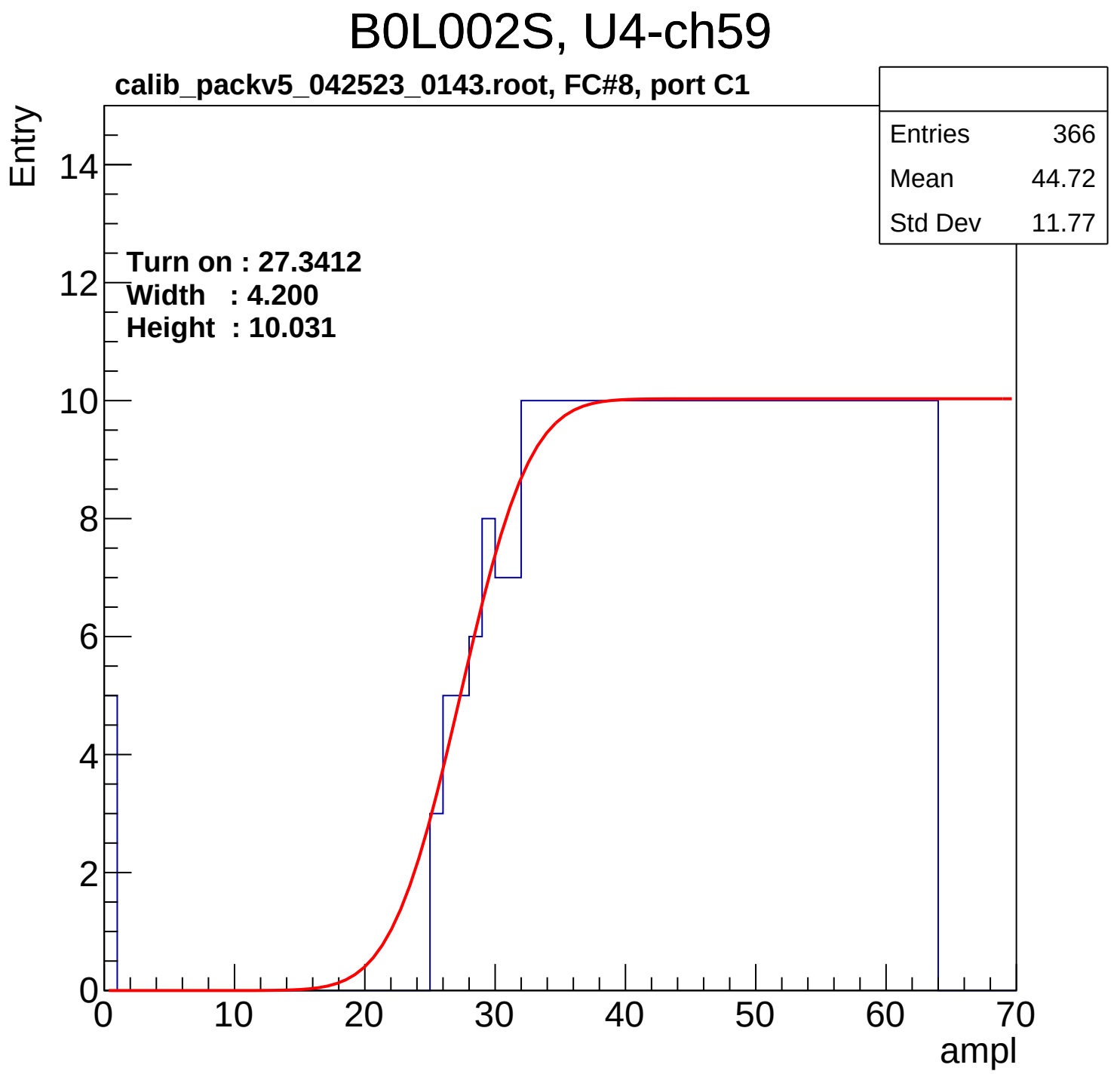

B0L002S, U4-ch54
calib_packv5_042523_0143.root, FC#8, port C1
Entries 352
Mean 45.52
Std Dev 11.1
Turn on : 30.1733
Width : 3.517
Height : 10.112
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

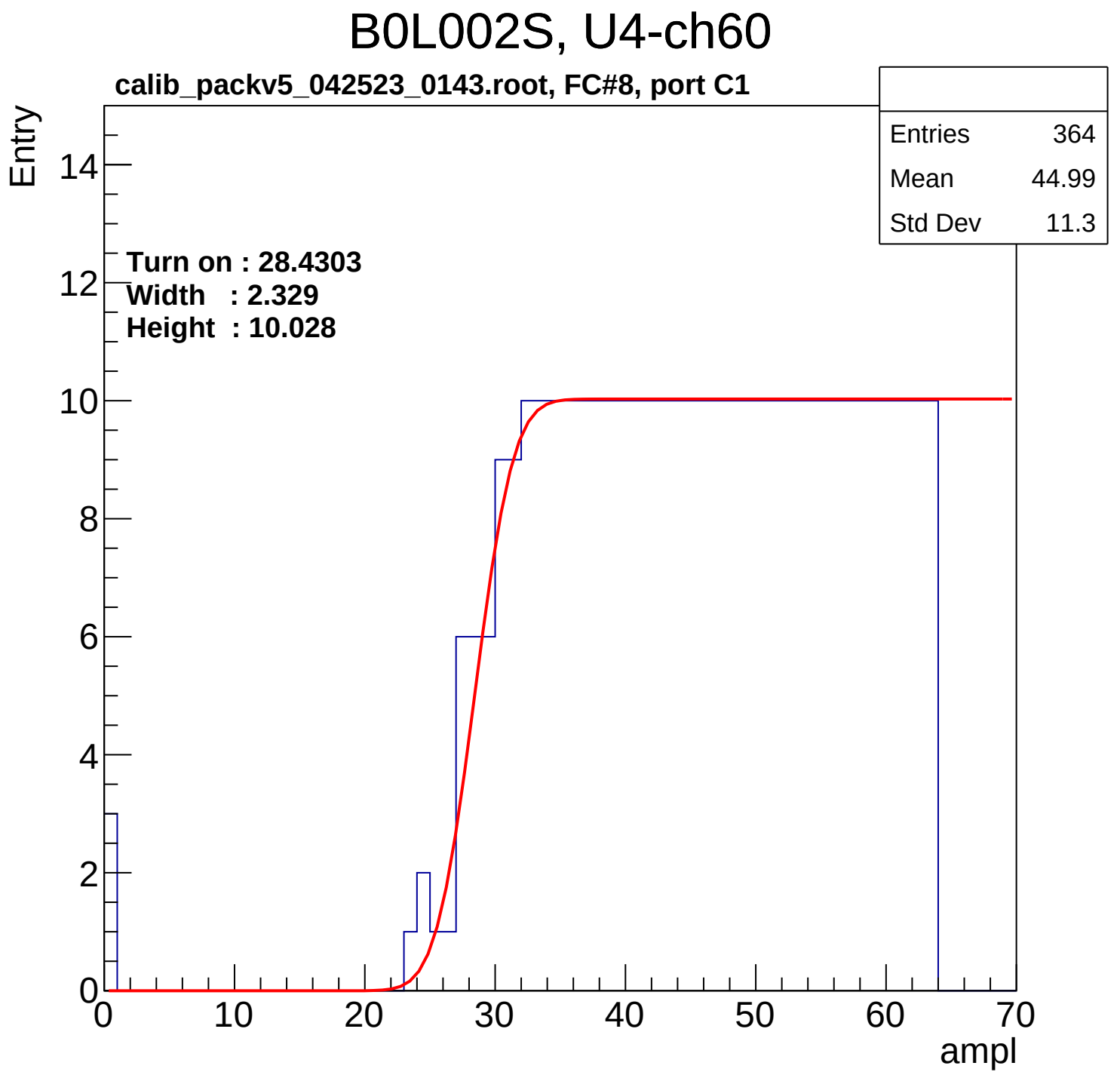

B0L002S, U4-ch55
calib_packv5_042523_0143.root, FC#8, port C1
Entries 371
Mean 44.72
Std Dev 11.26
Turn on : 26.9351
Width : 3.323
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

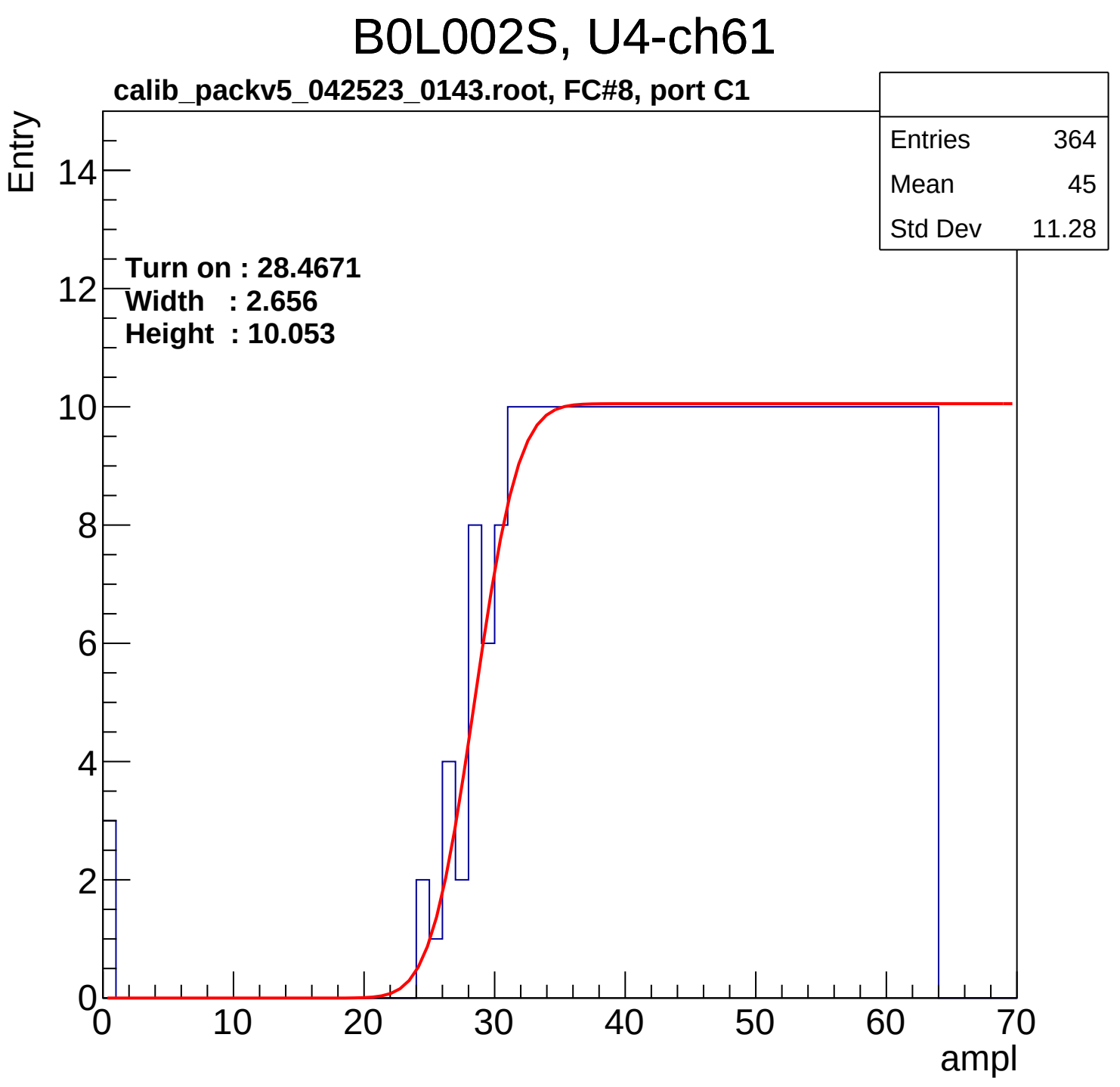

B0L002S, U4-ch56
calib_packv5_042523_0143.root, FC#8, port C1
Entries 364
Mean 44.99
Std Dev 11.2
Turn on : 27.9892
Width : 3.732
Height : 10.023
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

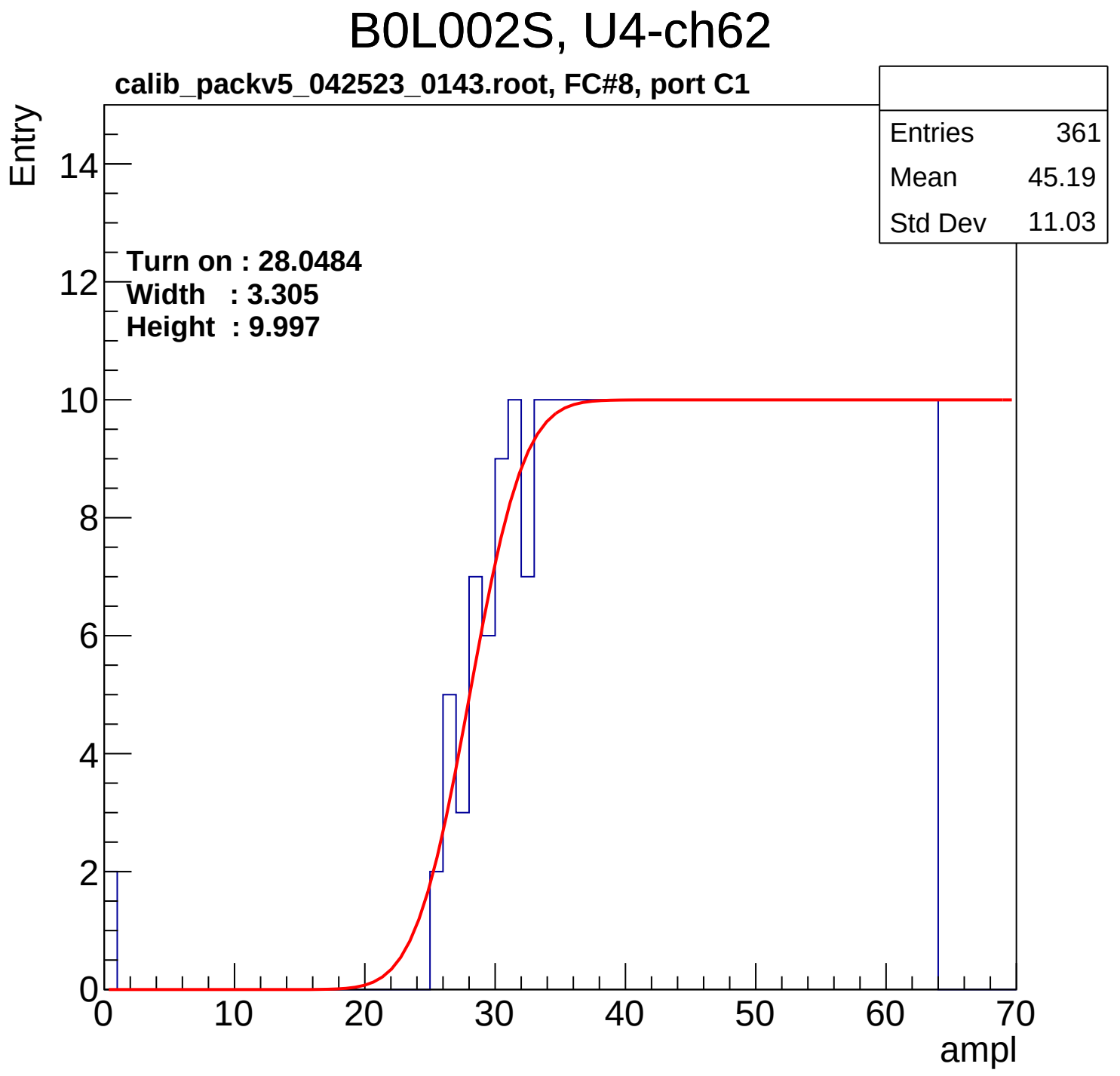

B0L002S, U4-ch57
calib_packv5_042523_0143.root, FC#8, port C1
Entries 388
Mean 43.88
Std Dev 11.69
Turn on : 25.4035
Width : 2.435
Height : 9.979
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

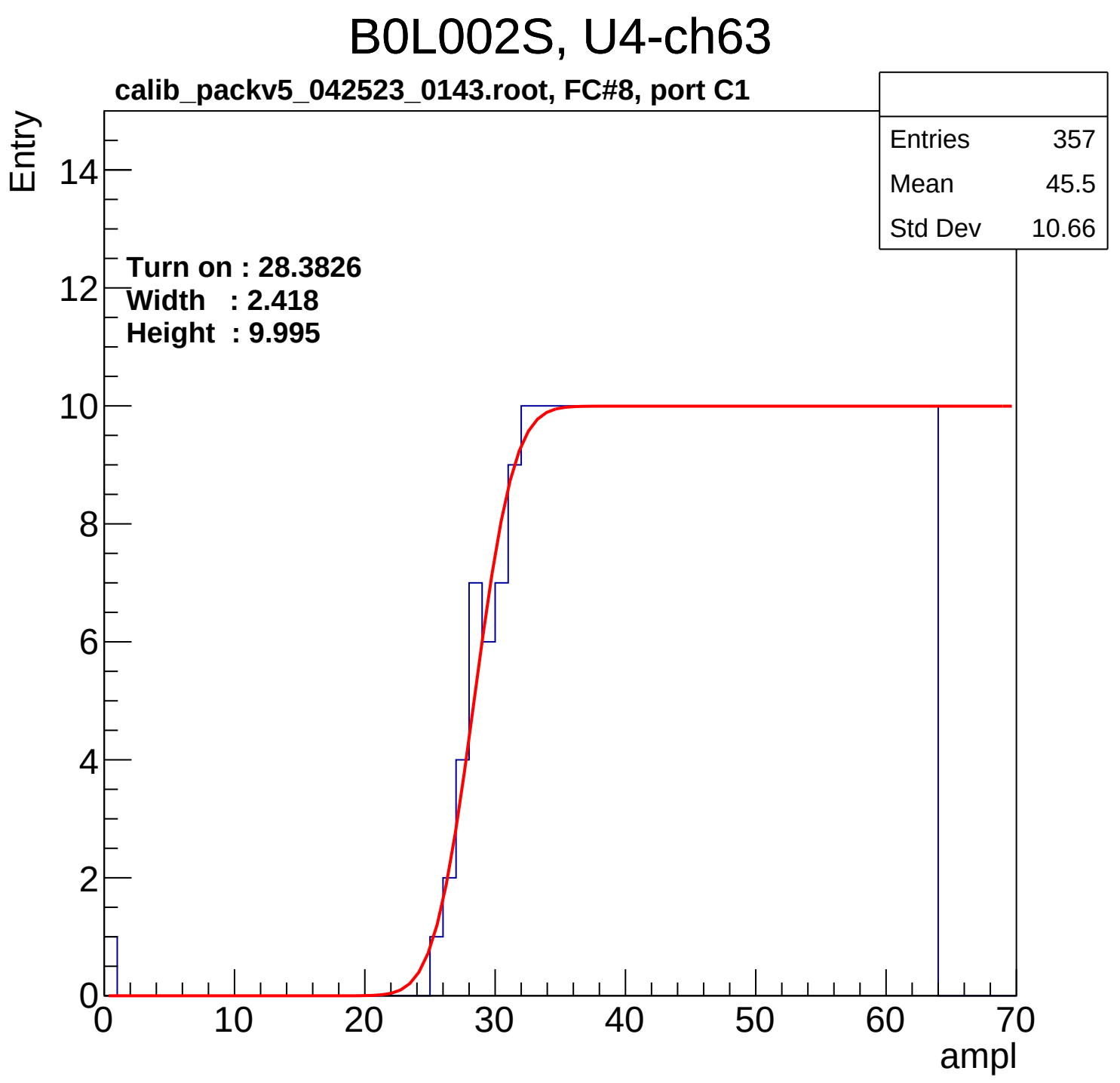

B0L002S, U4-ch58
calib_packv5_042523_0143.root, FC#8, port C1
Entries 360
Mean 45.36
Std Dev 10.74
Turn on : 28.5152
Width : 2.505
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

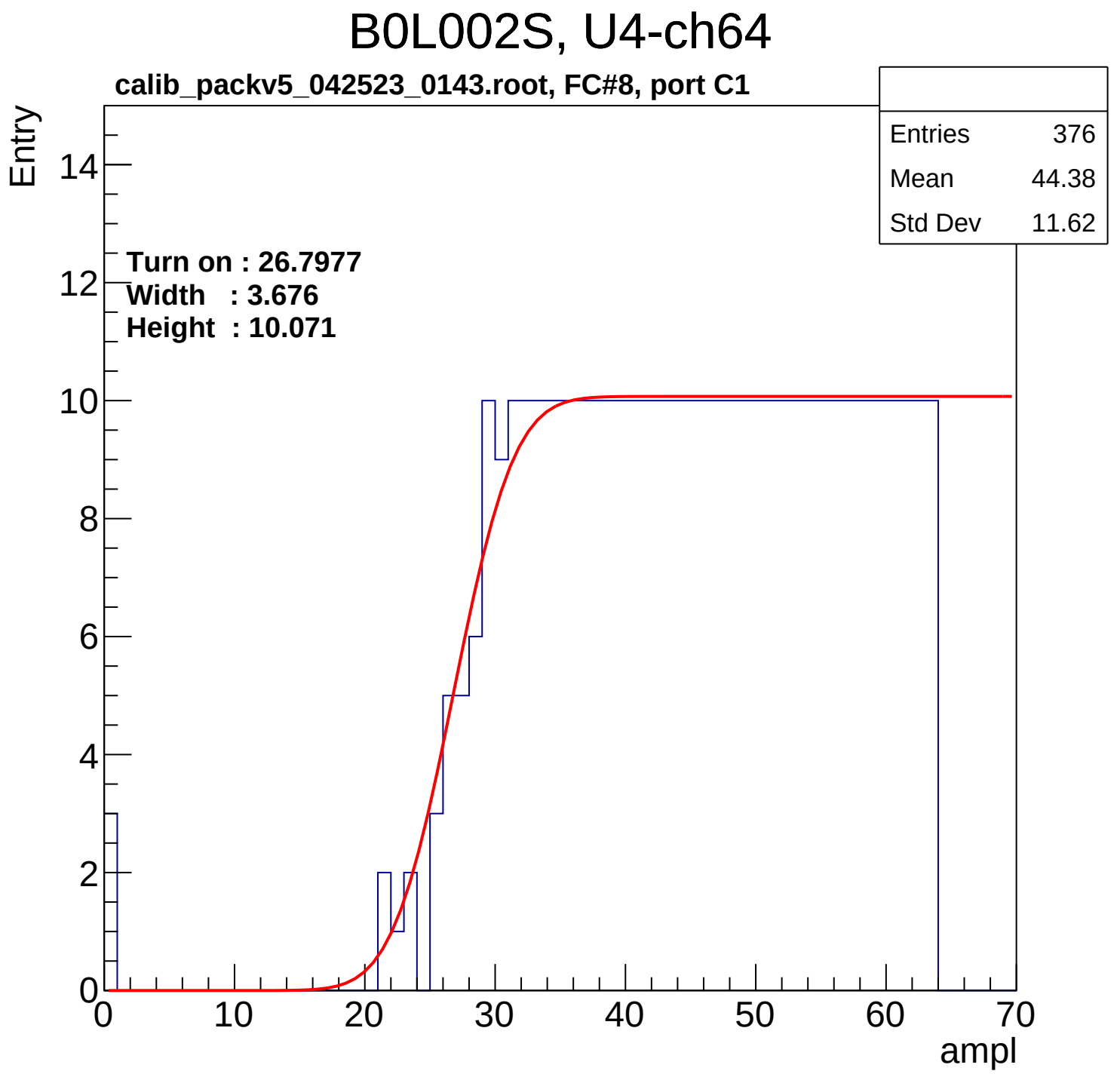

B0L002S, U4-ch59
calib_packv5_042523_0143.root, FC#8, port C1
Entries 366
Mean 44.72
Std Dev 11.77
Turn on : 27.3412
Width : 4.200
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

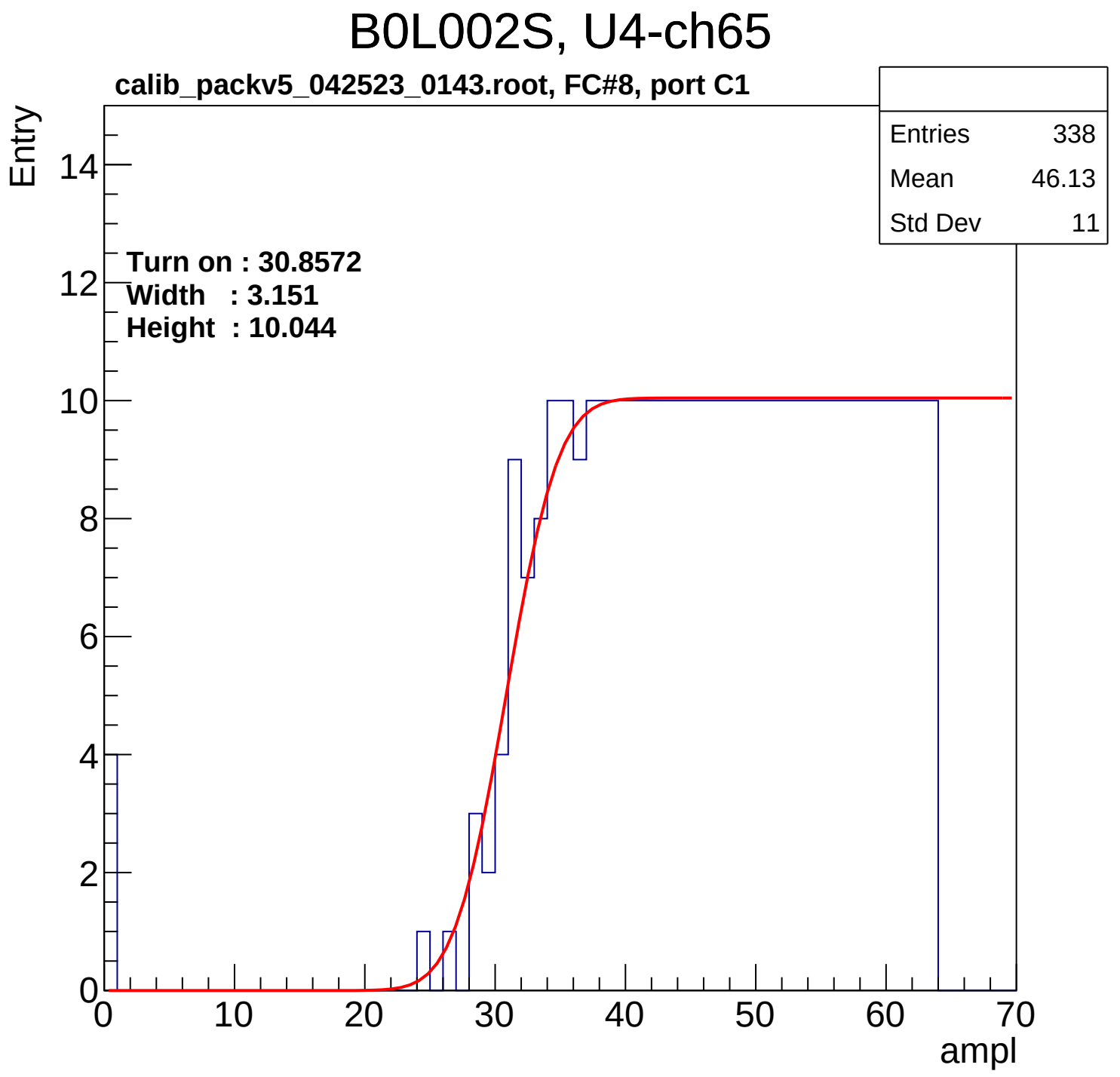

B0L002S, U4-ch60
calib_packv5_042523_0143.root, FC#8, port C1
Entries 364
Mean 44.99
Std Dev 11.3
Turn on : 28.4303
Width : 2.329
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

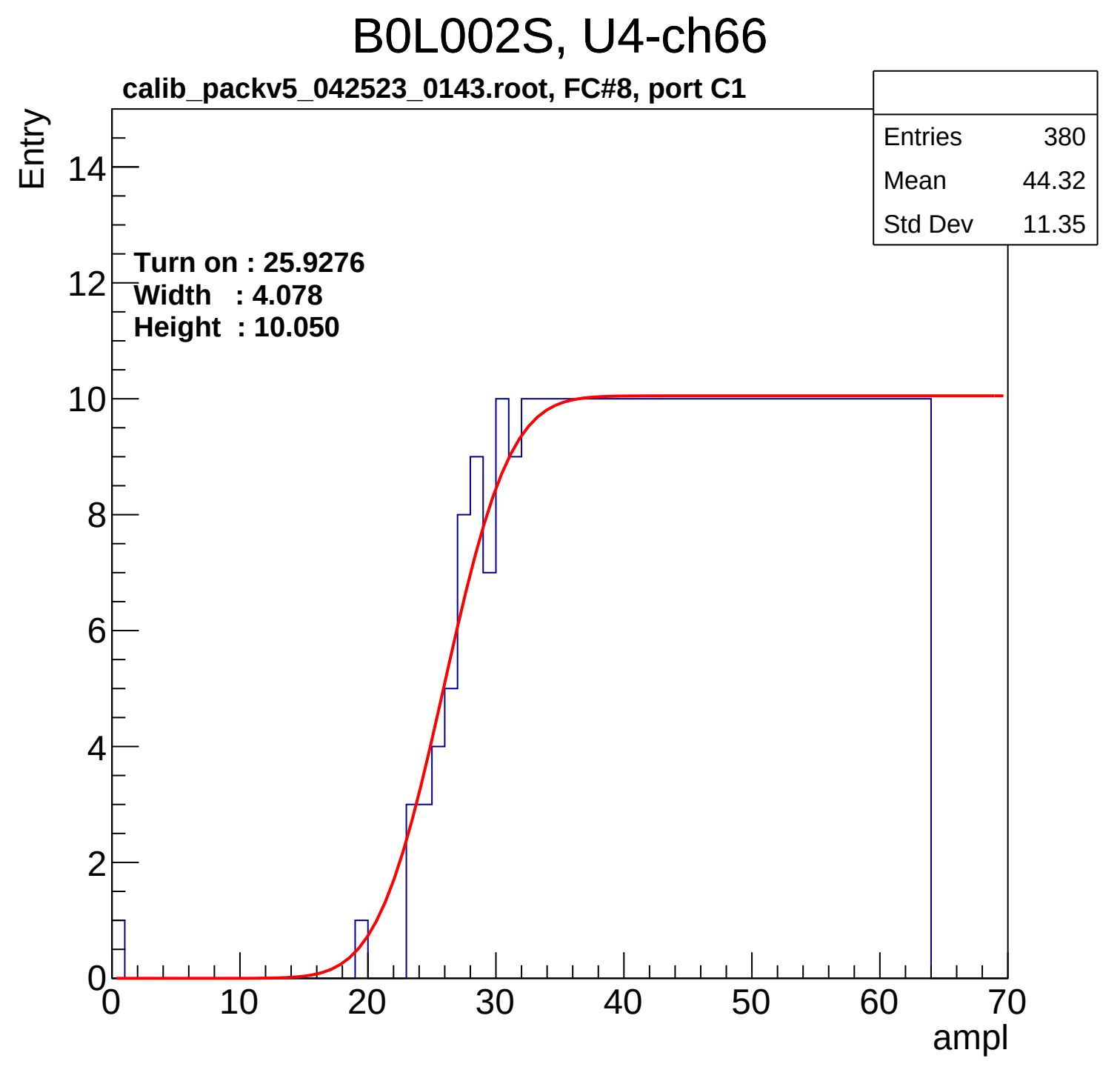

B0L002S, U4-ch61
calib_packv5_042523_0143.root, FC#8, port C1
Entries 364
Mean 45
Std Dev 11.28
Turn on : 28.4671
Width : 2.656
Height : 10.053
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

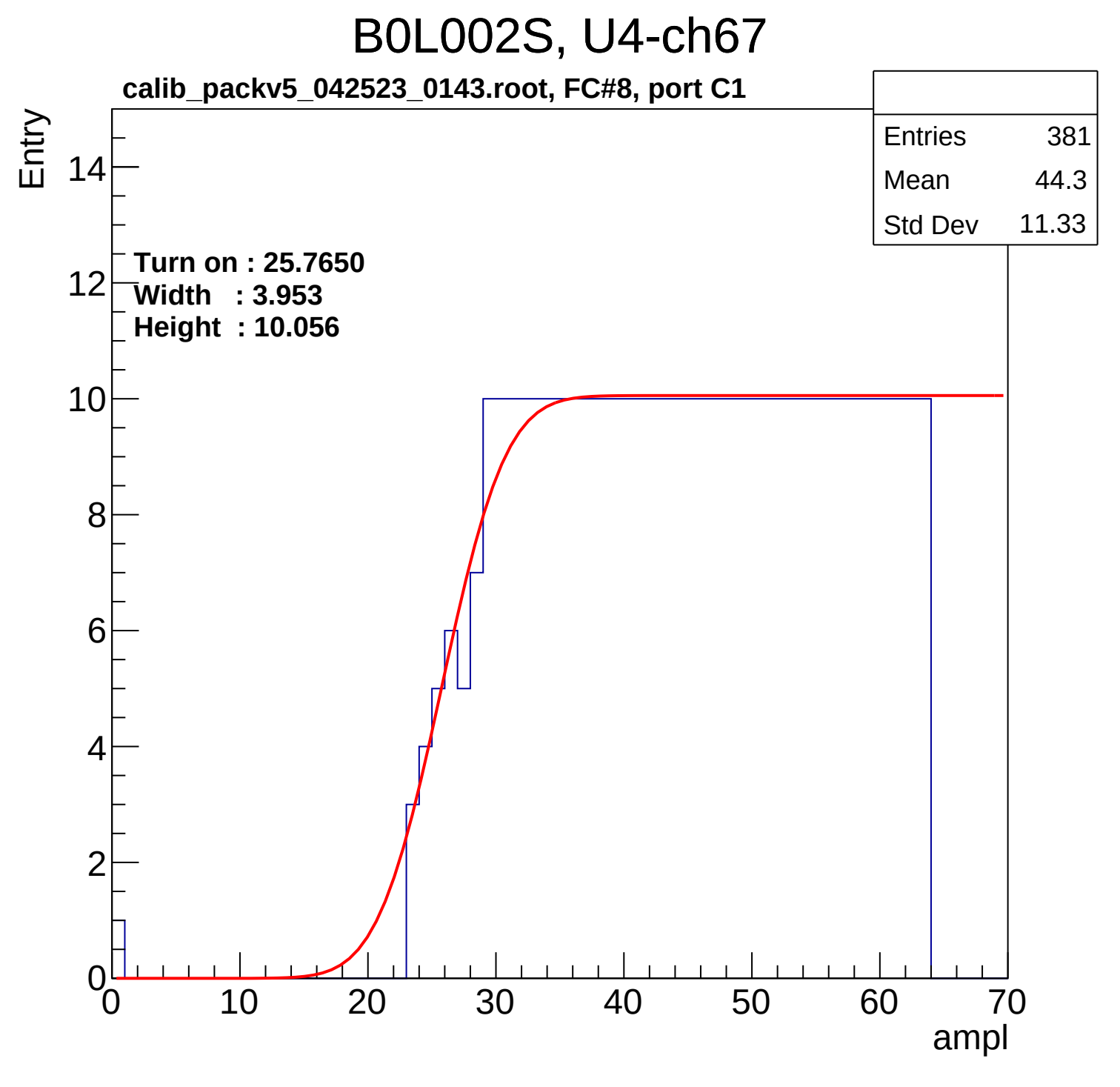

B0L002S, U4-ch62
calib_packv5_042523_0143.root, FC#8, port C1
Entries 361
Mean 45.19
Std Dev 11.03
Turn on : 28.0484
Width : 3.305
Height : 9.997
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

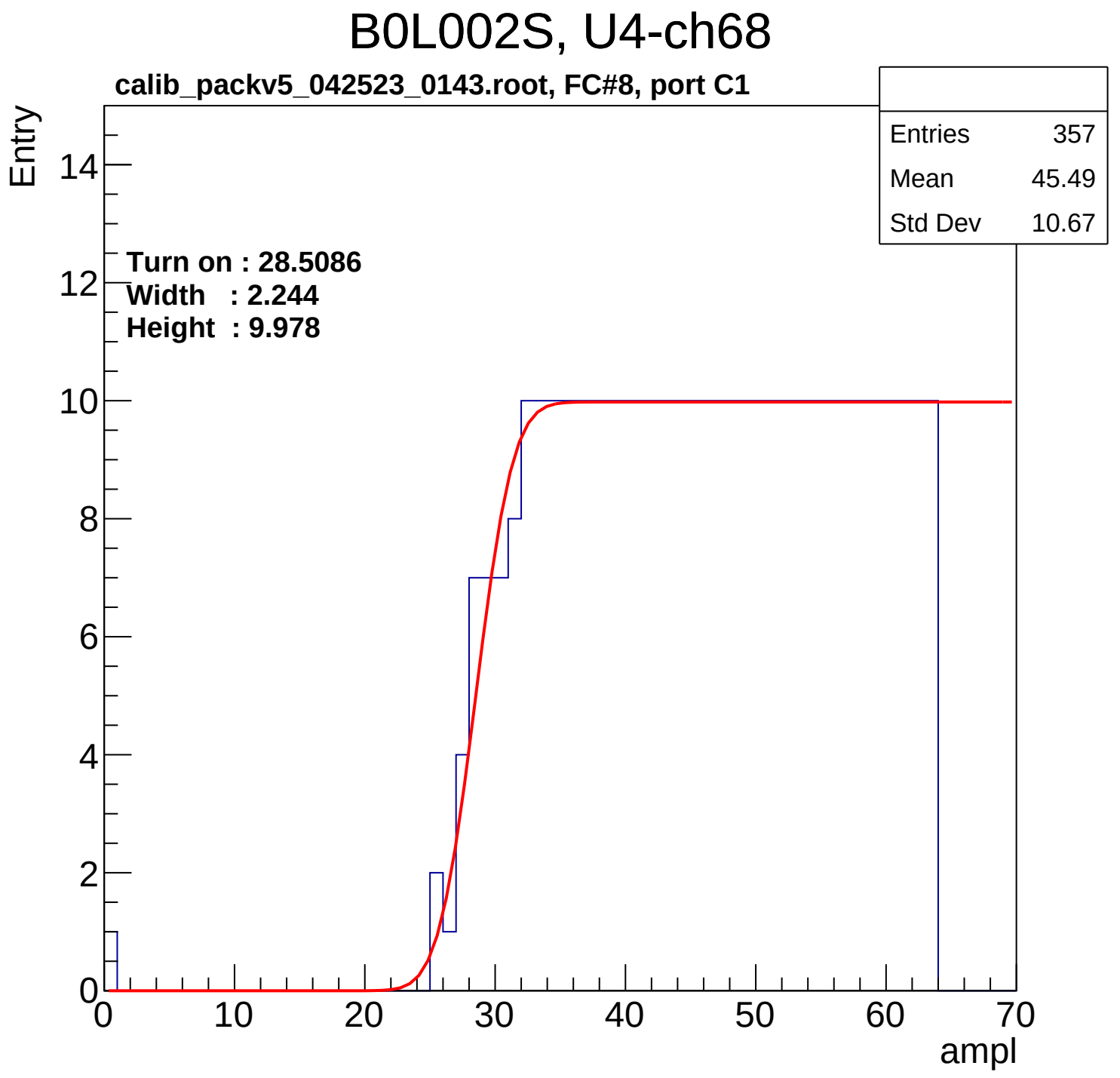

B0L002S, U4-ch63
calib_packv5_042523_0143.root, FC#8, port C1
Entries 357
Mean 45.5
Std Dev 10.66
Turn on : 28.3826
Width : 2.418
Height : 9.995
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

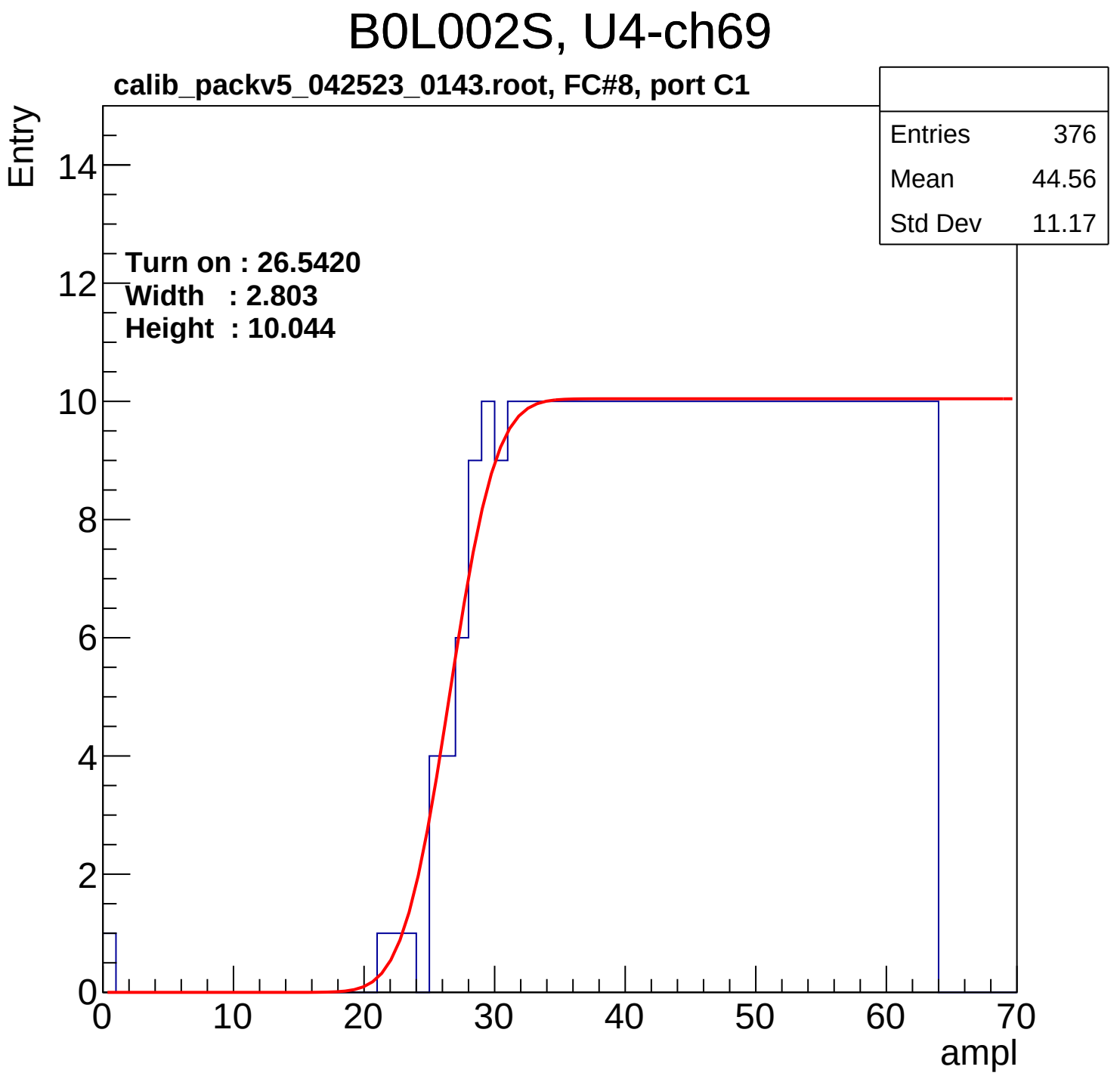

B0L002S, U4-ch64
calib_packv5_042523_0143.root, FC#8, port C1
Entries 376
Mean 44.38
Std Dev 11.62
Turn on : 26.7977
Width : 3.676
Height : 10.071
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

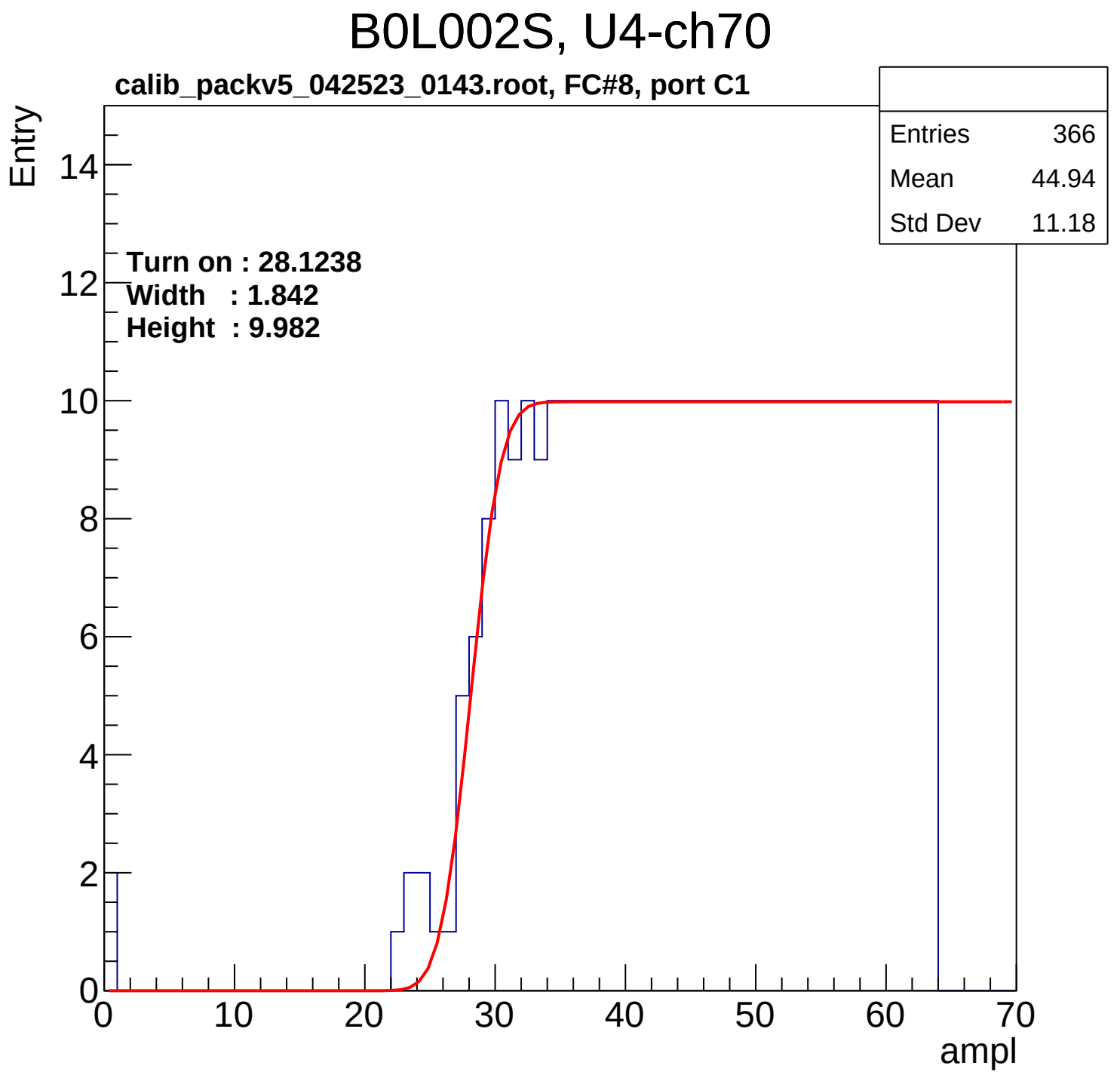

B0L002S, U4-ch65
calib_packv5_042523_0143.root, FC#8, port C1
Entries 338
Mean 46.13
Std Dev 11
Turn on : 30.8572
Width : 3.151
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

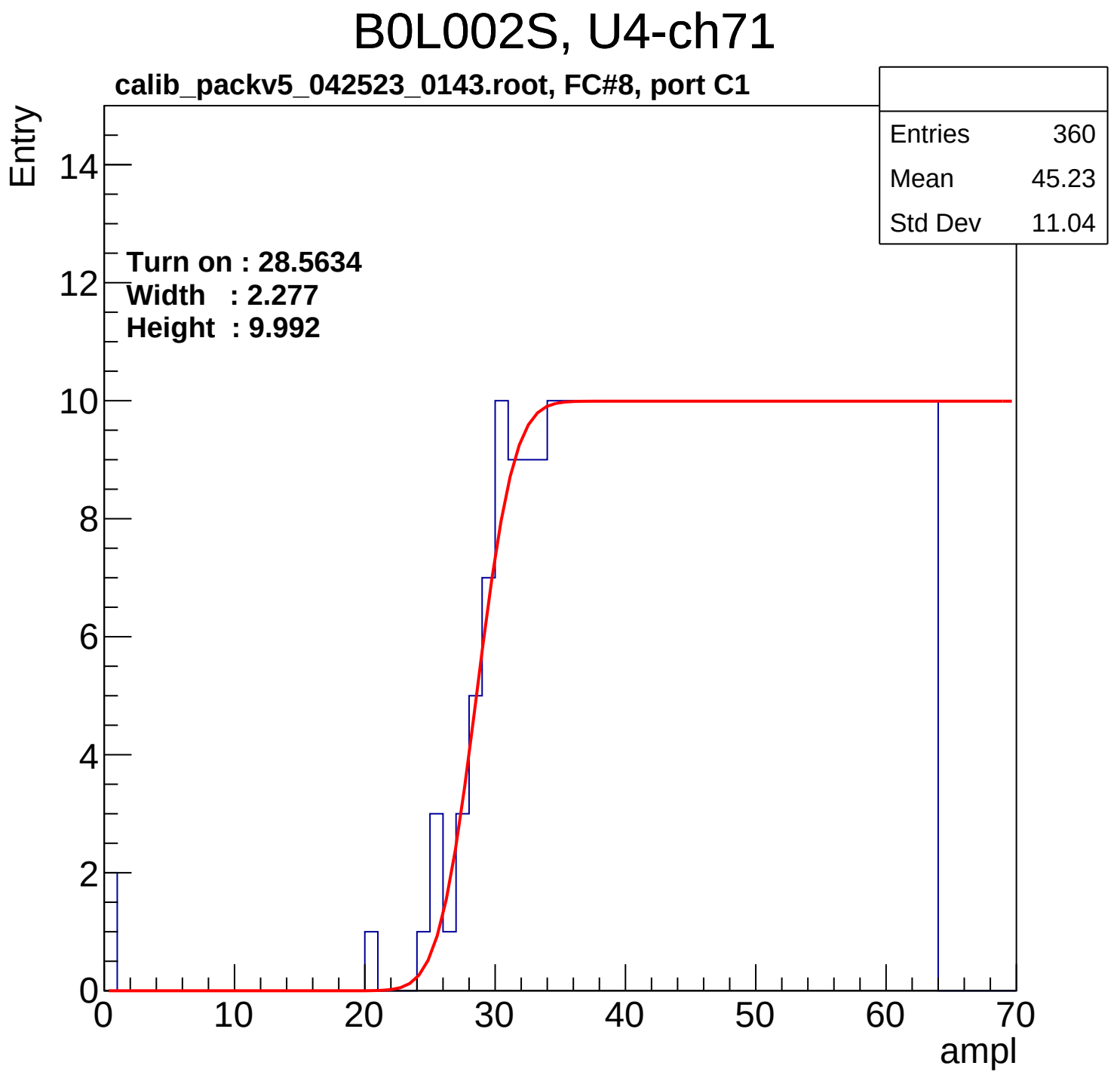

B0L002S, U4-ch66
calib_packv5_042523_0143.root, FC#8, port C1
Entries 380
Mean 44.32
Std Dev 11.35
Turn on : 25.9276
Width : 4.078
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

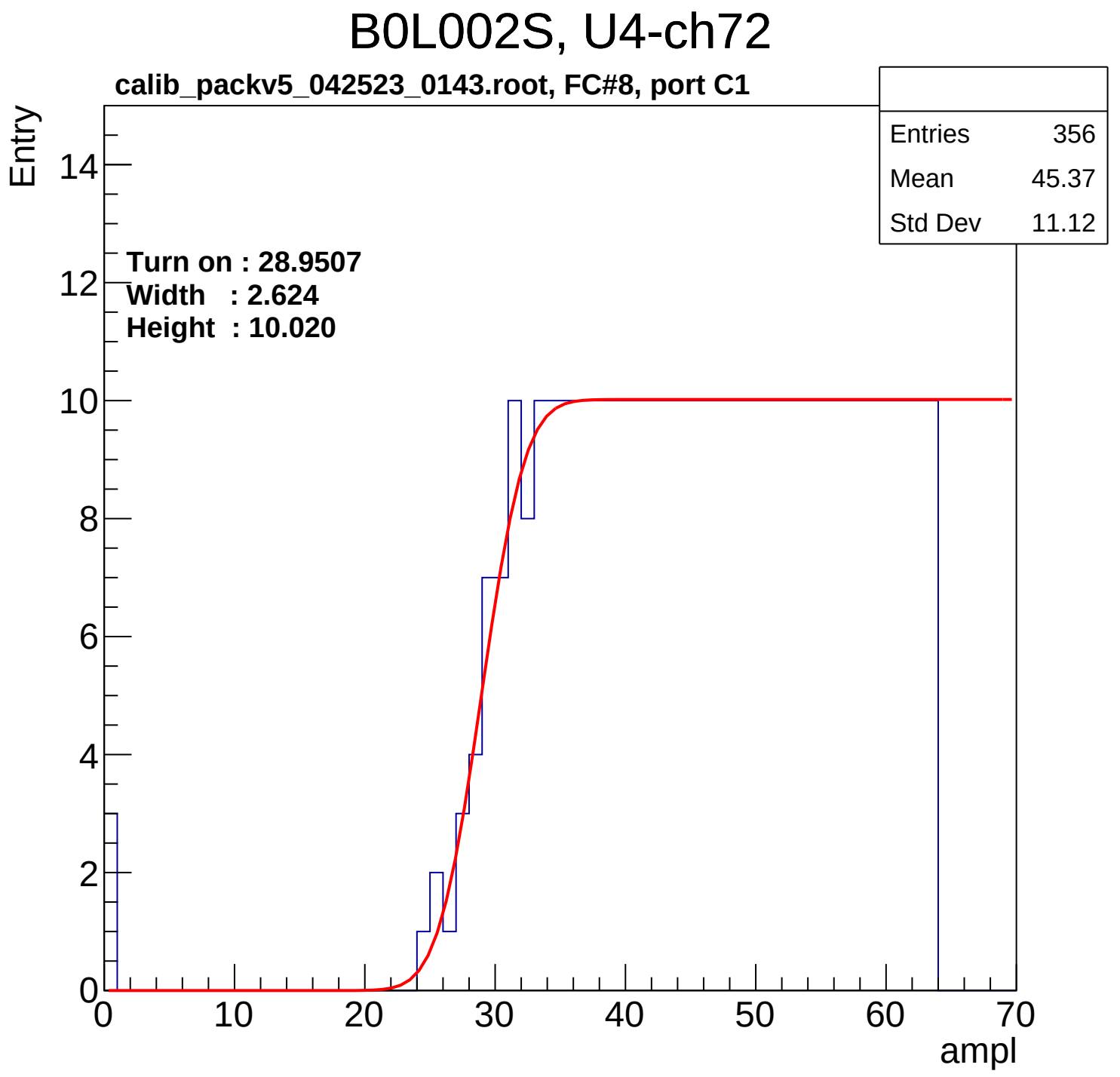

B0L002S, U4-ch67
calib_packv5_042523_0143.root, FC#8, port C1
Entries 381
Mean 44.3
Std Dev 11.33
Turn on : 25.7650
Width : 3.953
Height : 10.056
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

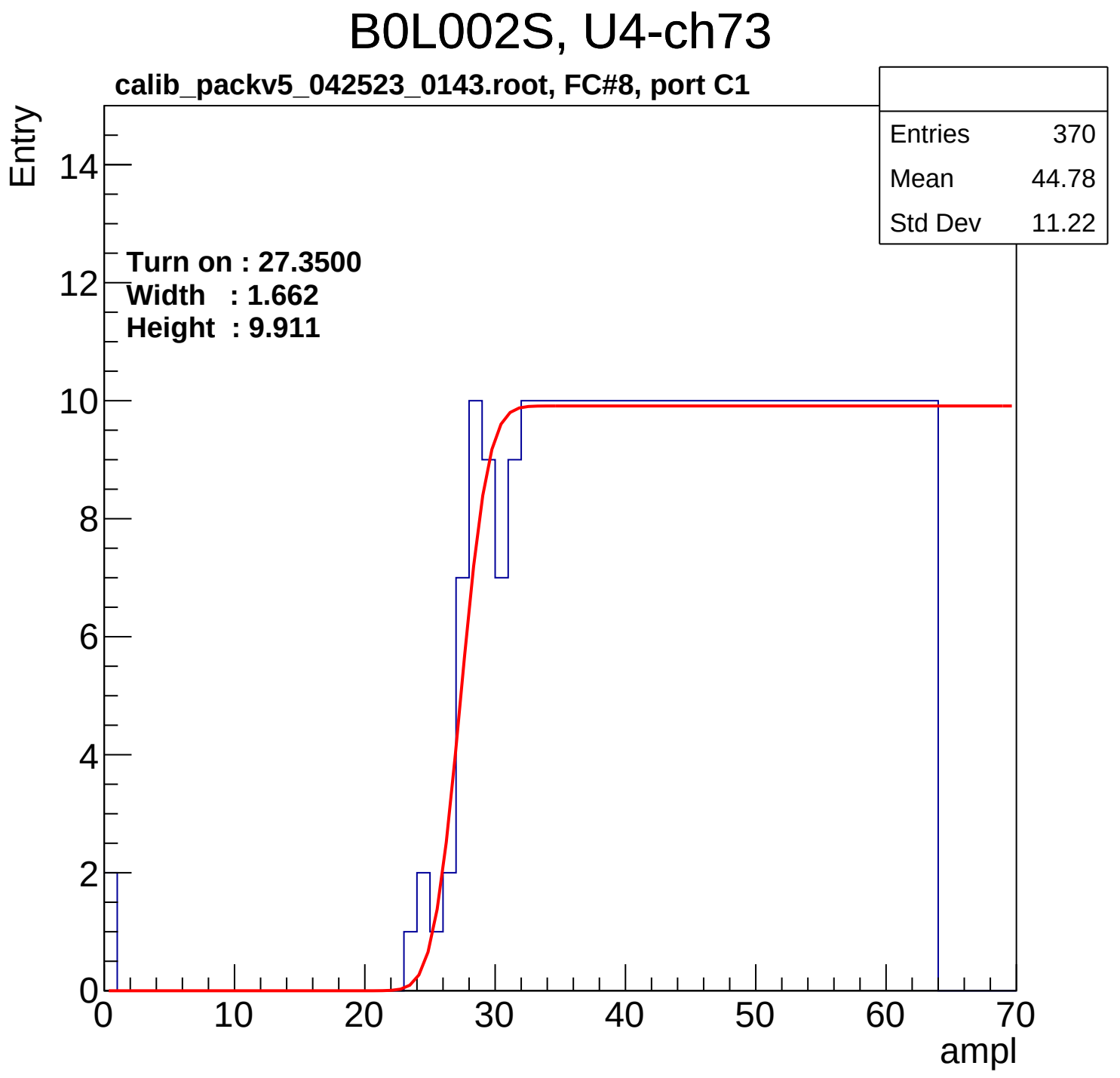

B0L002S, U4-ch68
calib_packv5_042523_0143.root, FC#8, port C1
Entries 357
Mean 45.49
Std Dev 10.67
Turn on : 28.5086
Width : 2.244
Height : 9.978
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

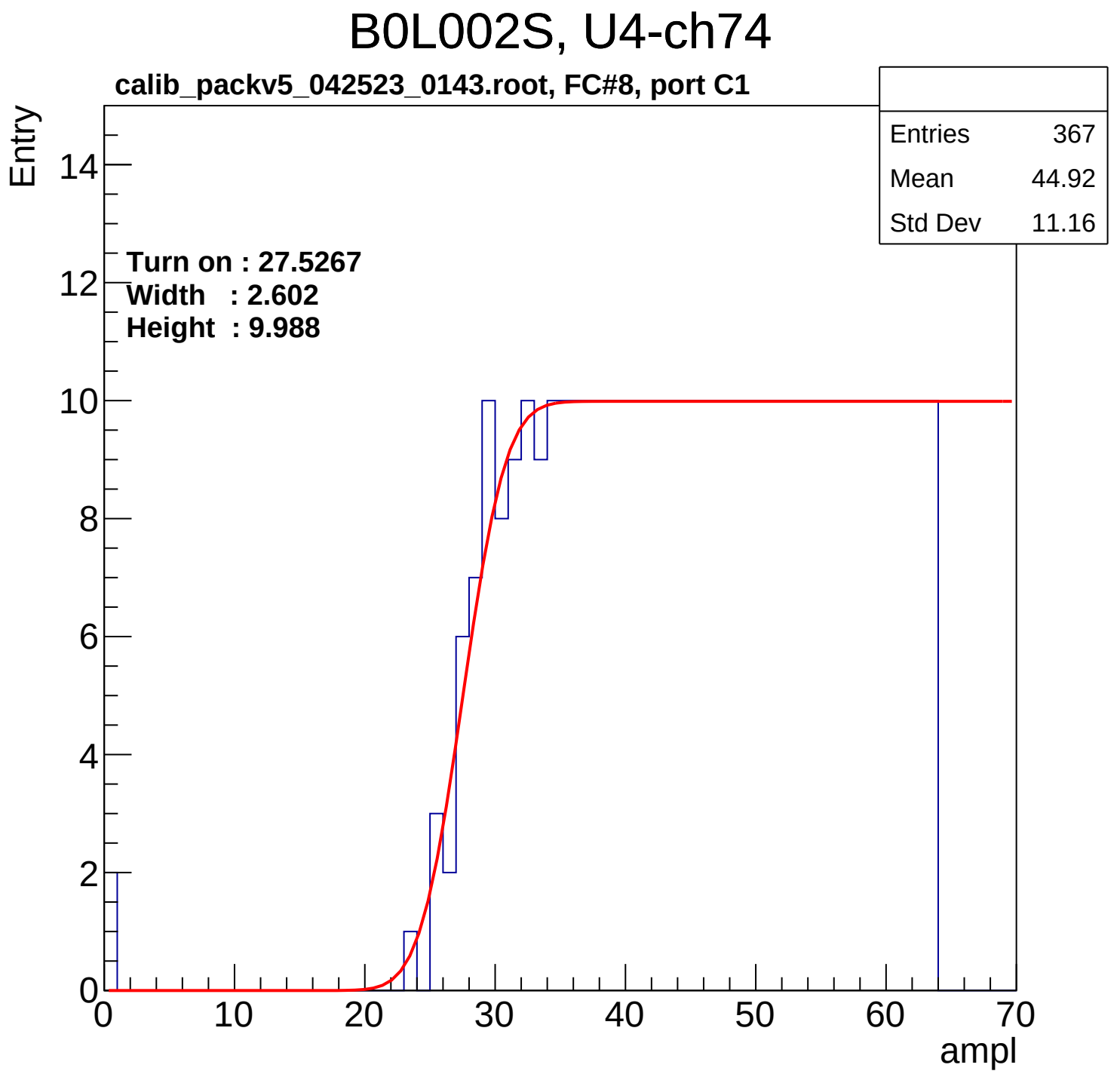

B0L002S, U4-ch69
calib_packv5_042523_0143.root, FC#8, port C1
Entries 376
Mean 44.56
Std Dev 11.17
Turn on : 26.5420
Width : 2.803
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

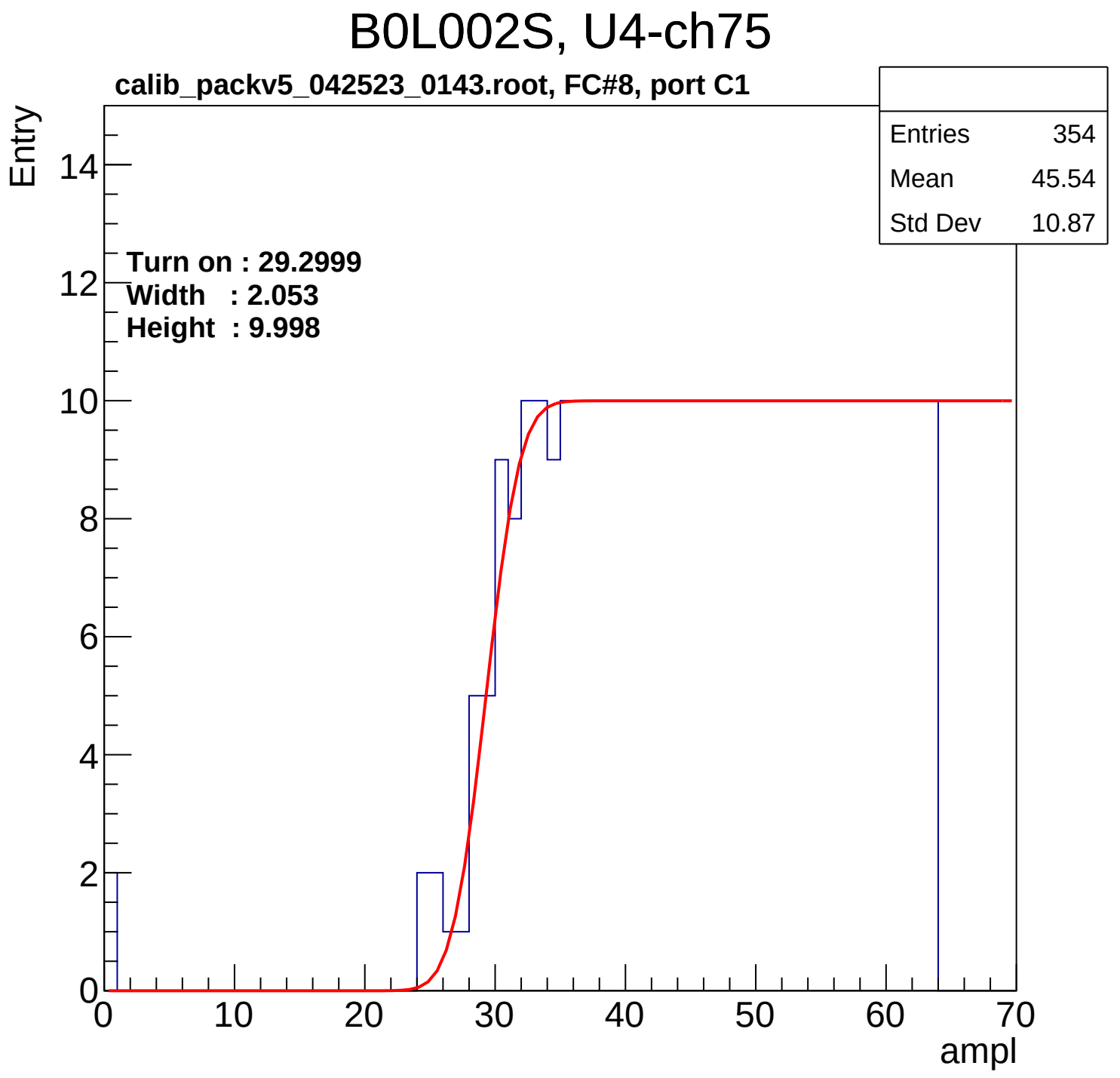

B0L002S, U4-ch70
calib_packv5_042523_0143.root, FC#8, port C1
Entries 366
Mean 44.94
Std Dev 11.18
Turn on : 28.1238
Width : 1.842
Height : 9.982
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

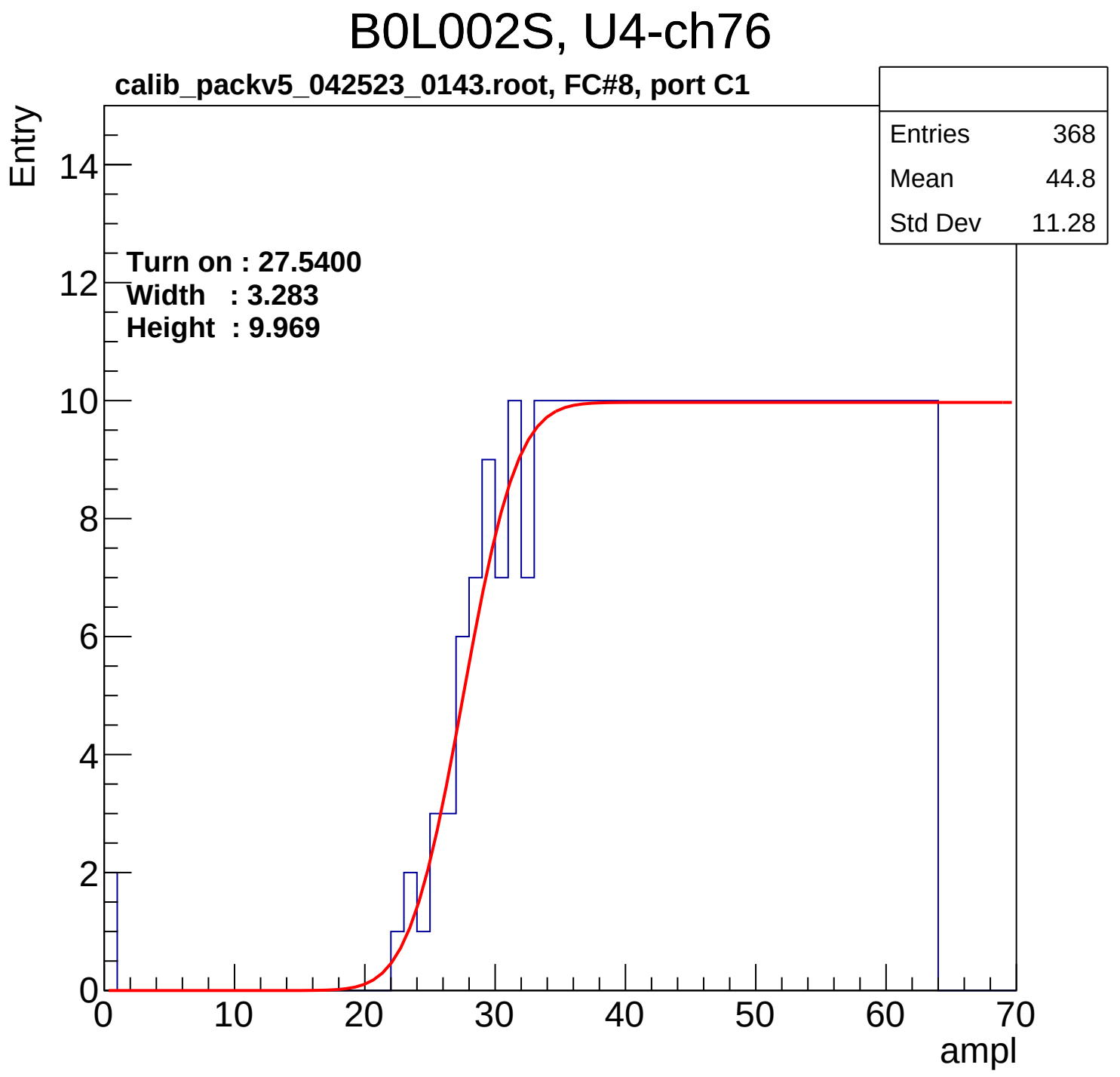

B0L002S, U4-ch71
calib_packv5_042523_0143.root, FC#8, port C1
Entries 360
Mean 45.23
Std Dev 11.04
Turn on : 28.5634
Width : 2.277
Height : 9.992
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

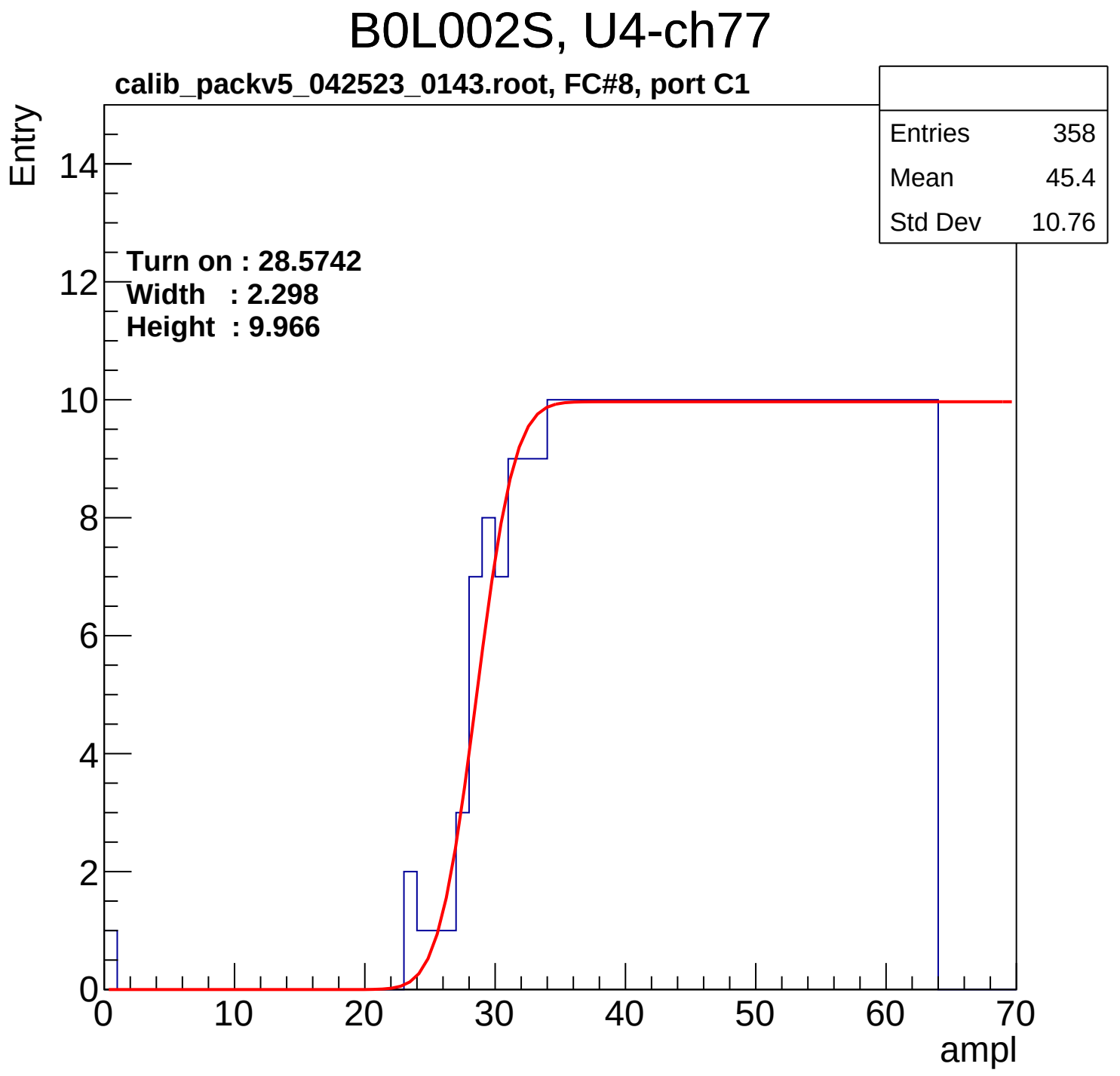

B0L002S, U4-ch72
calib_packv5_042523_0143.root, FC#8, port C1
Entries 356
Mean 45.37
Std Dev 11.12
Turn on : 28.9507
Width : 2.624
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

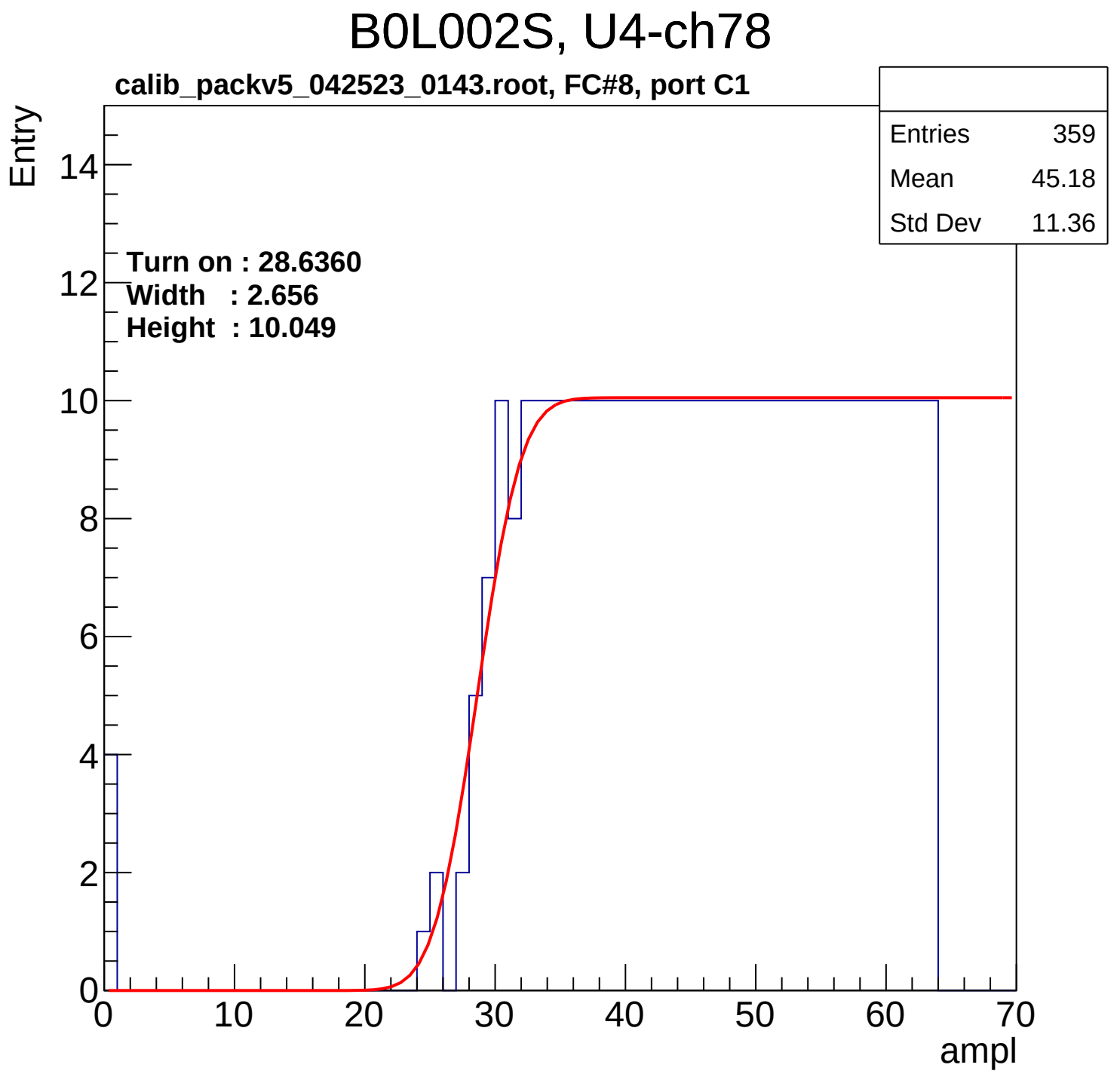

B0L002S, U4-ch73
calib_packv5_042523_0143.root, FC#8, port C1
Entries 370
Mean 44.78
Std Dev 11.22
Turn on : 27.3500
Width : 1.662
Height : 9.911
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

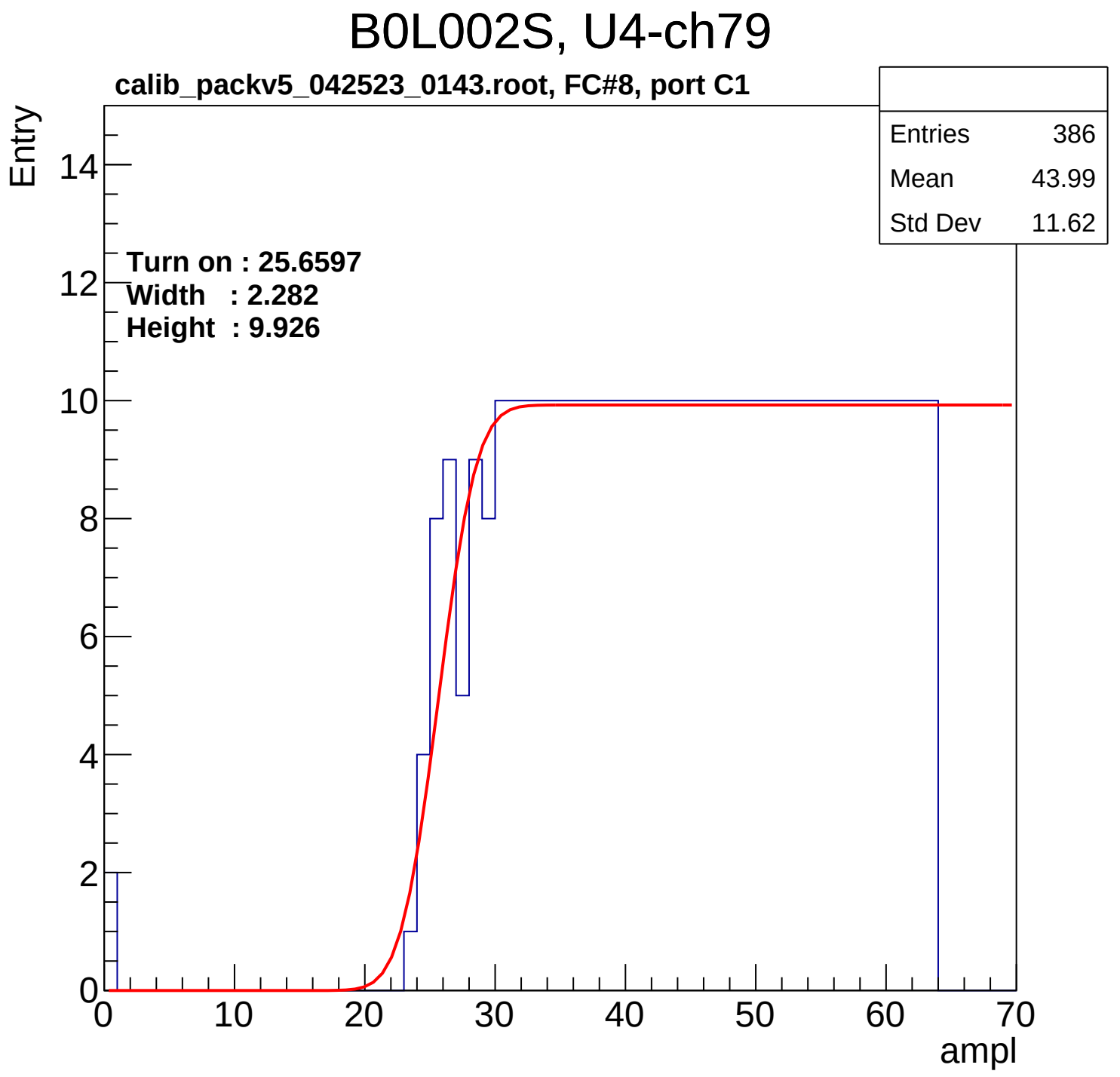

B0L002S, U4-ch74
calib_packv5_042523_0143.root, FC#8, port C1
Entries 367
Mean 44.92
Std Dev 11.16
Turn on : 27.5267
Width : 2.602
Height : 9.988
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

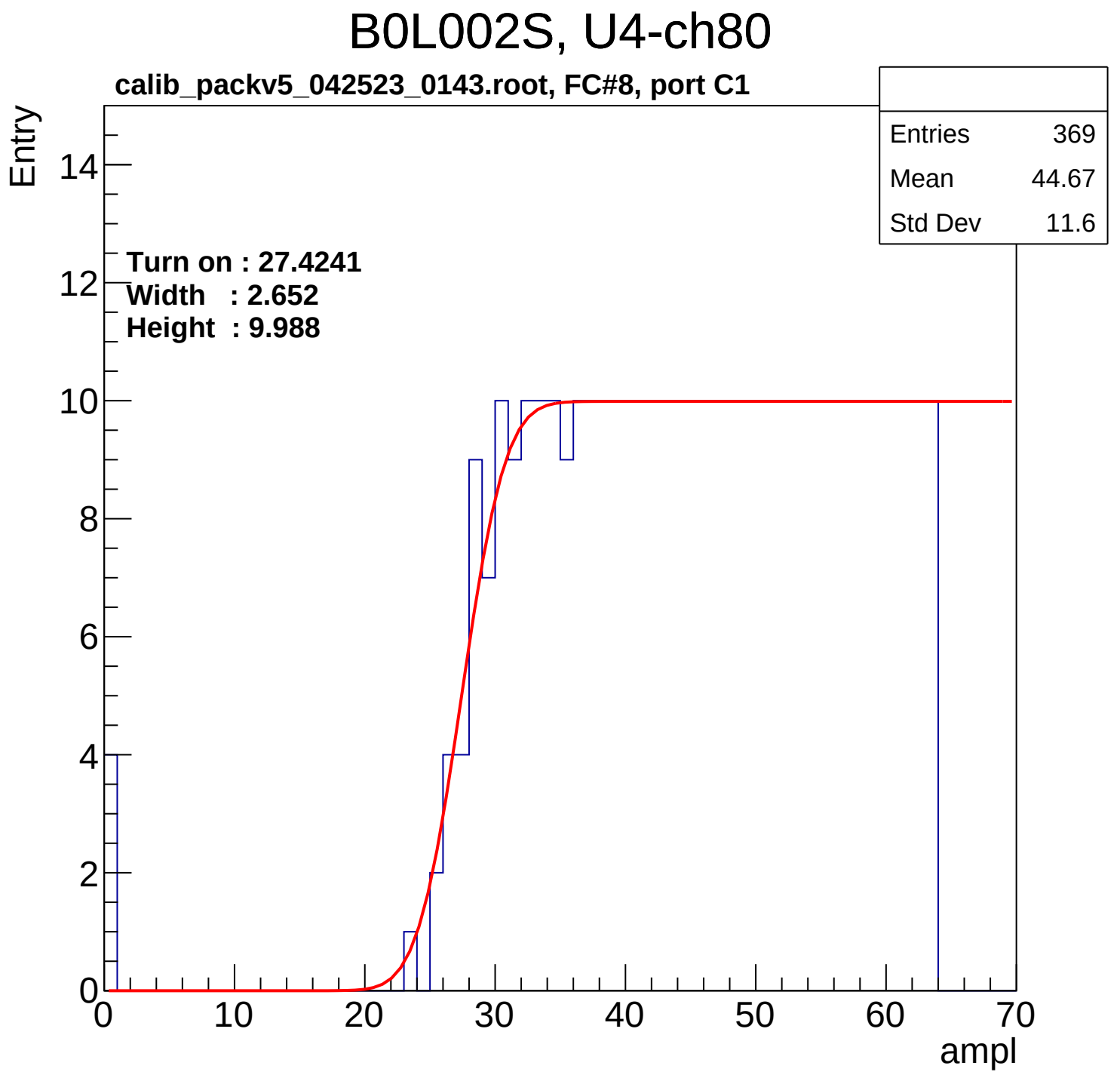

B0L002S, U4-ch75
calib_packv5_042523_0143.root, FC#8, port C1
Entries 354
Mean 45.54
Std Dev 10.87
Turn on : 29.2999
Width : 2.053
Height : 9.998
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

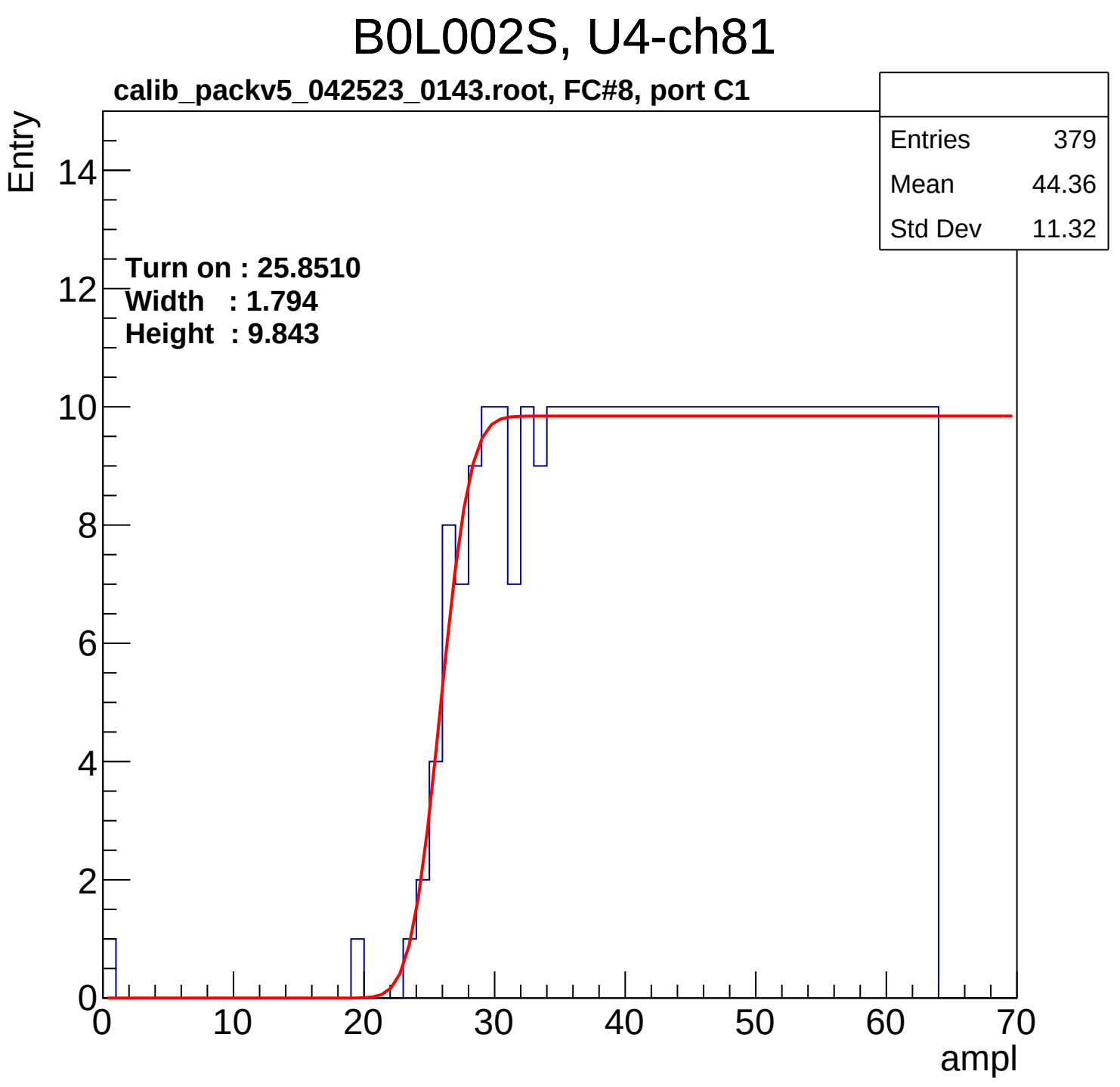

B0L002S, U4-ch76
calib_packv5_042523_0143.root, FC#8, port C1
Entries 368
Mean 44.8
Std Dev 11.28
Turn on : 27.5400
Width : 3.283
Height : 9.969
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

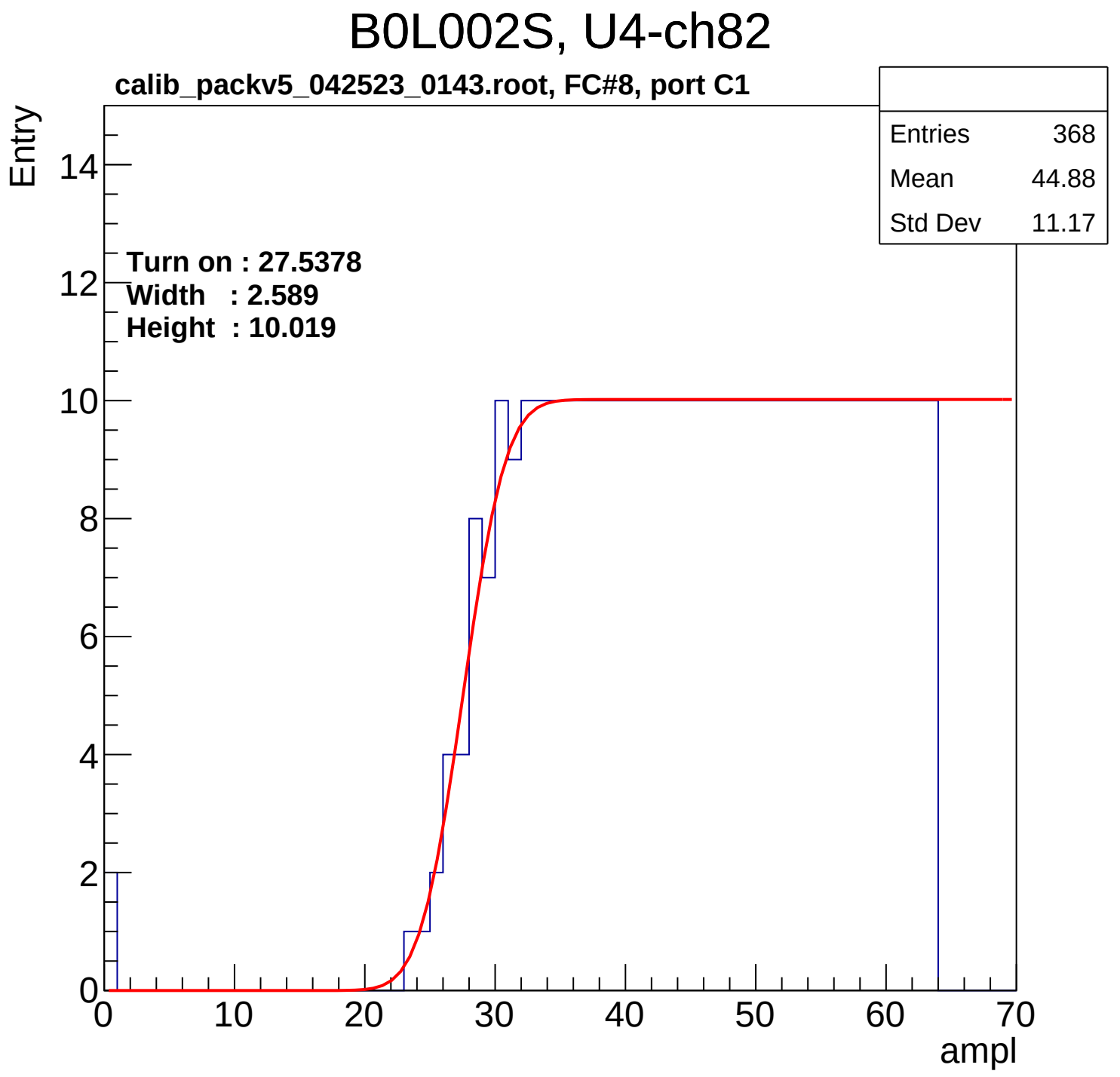

B0L002S, U4-ch77
calib_packv5_042523_0143.root, FC#8, port C1
Entries 358
Mean 45.4
Std Dev 10.76
Turn on : 28.5742
Width : 2.298
Height : 9.966
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

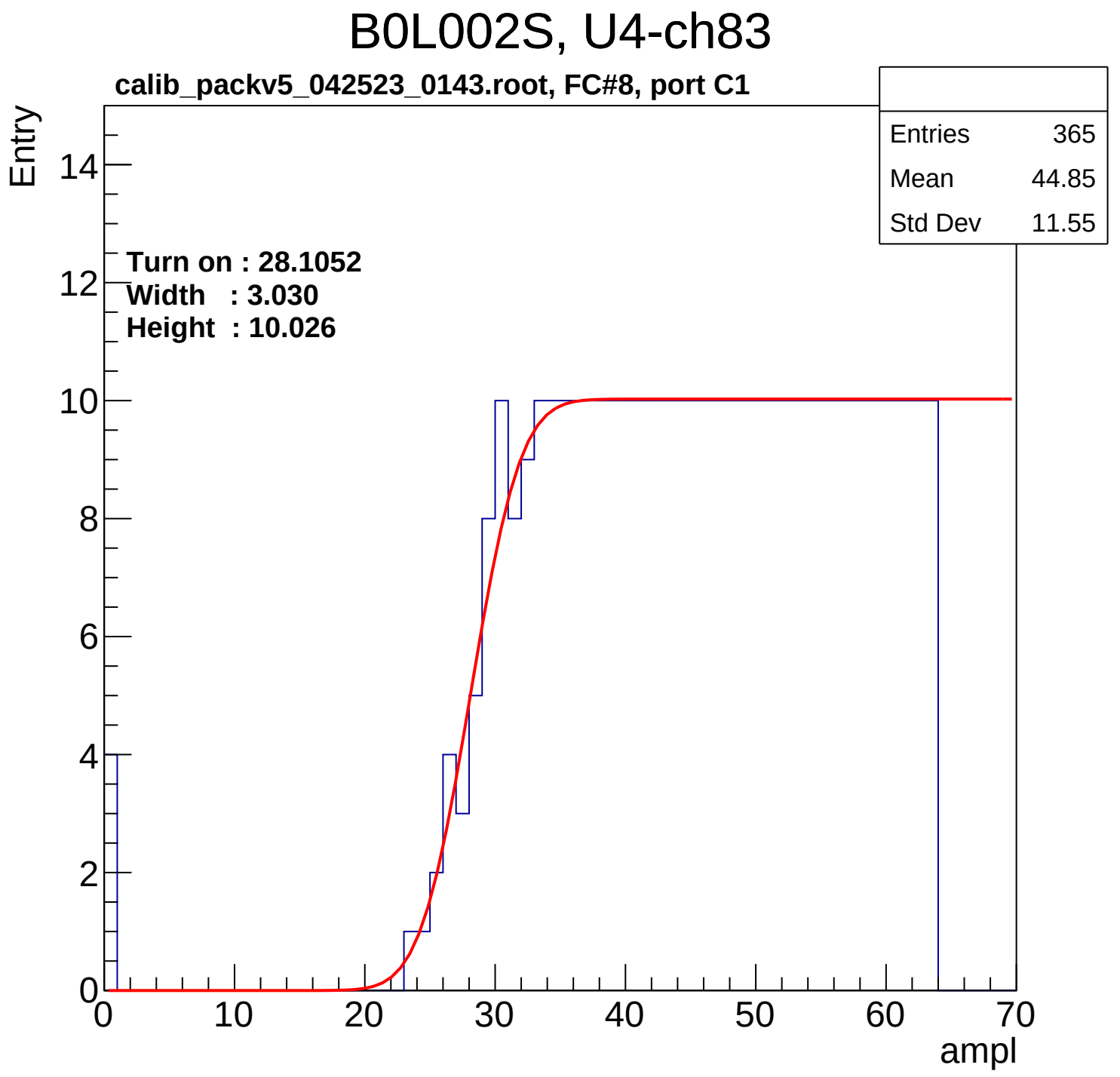

B0L002S, U4-ch78
calib_packv5_042523_0143.root, FC#8, port C1
Entries 359
Mean 45.18
Std Dev 11.36
Turn on : 28.6360
Width : 2.656
Height : 10.049
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

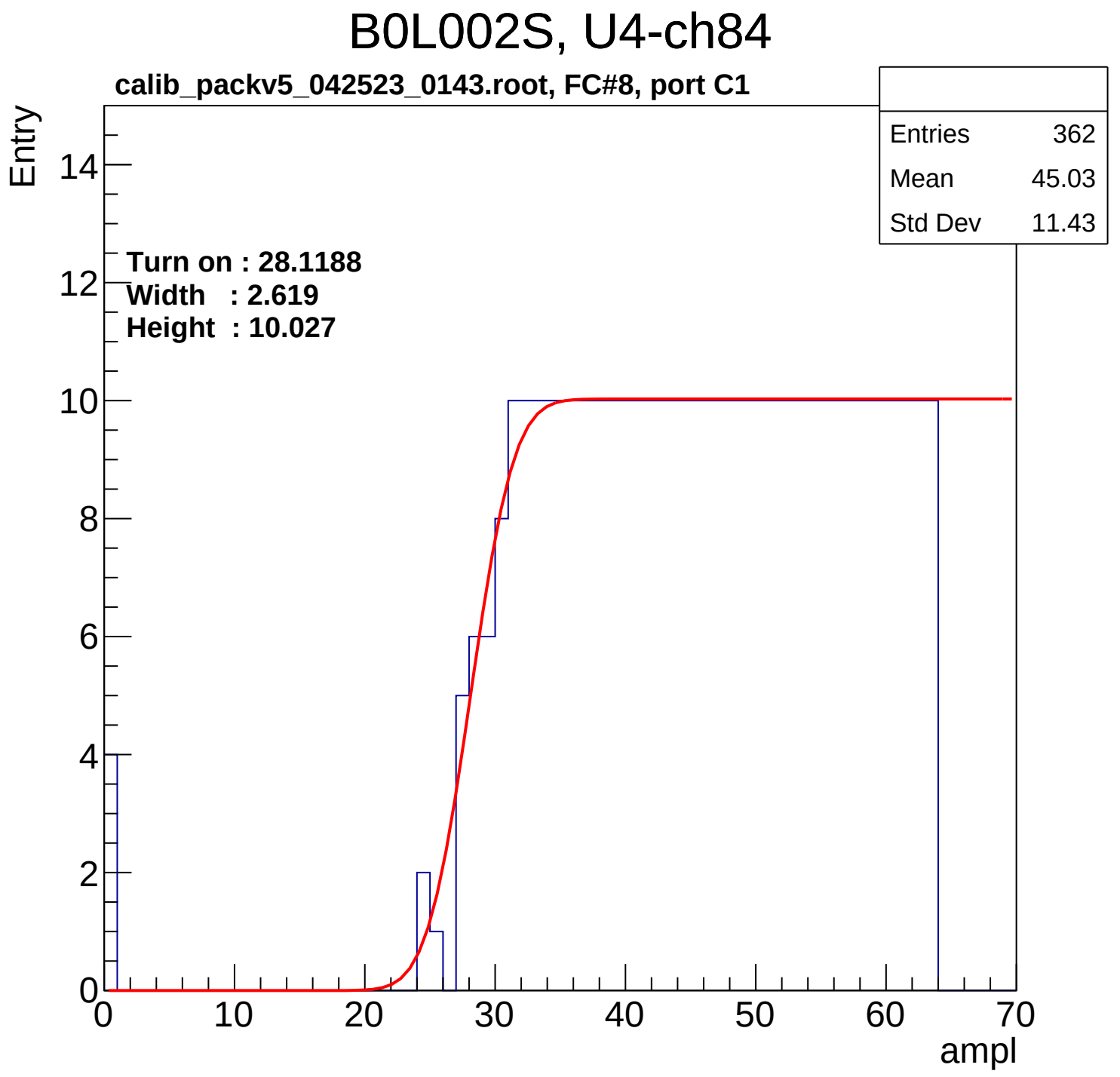

B0L002S, U4-ch79
calib_packv5_042523_0143.root, FC#8, port C1
Entries 386
Mean 43.99
Std Dev 11.62
Turn on : 25.6597
Width : 2.282
Height : 9.926
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

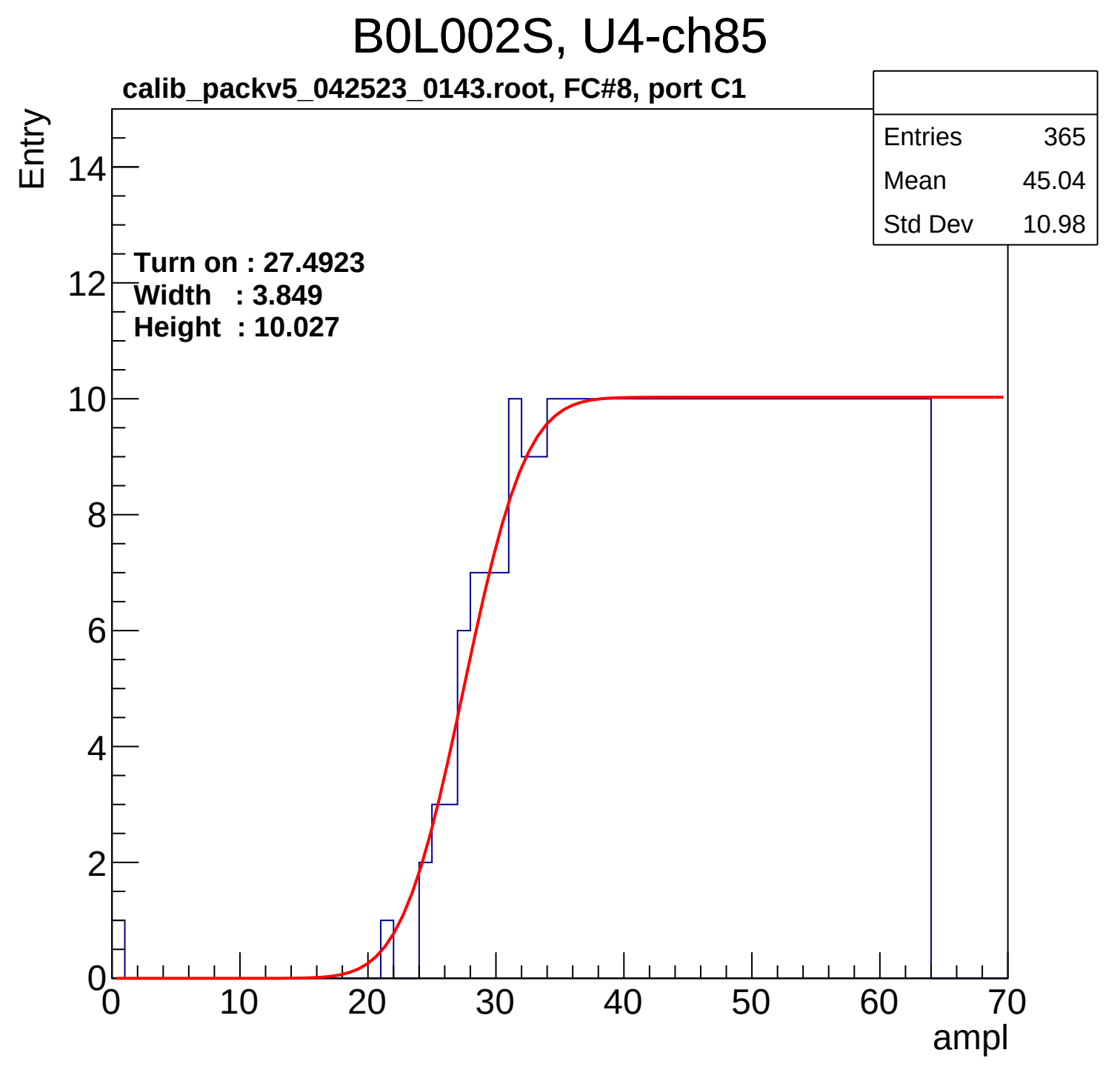

B0L002S, U4-ch80
calib_packv5_042523_0143.root, FC#8, port C1
Entries 369
Mean 44.67
Std Dev 11.6
Turn on : 27.4241
Width : 2.652
Height : 9.988
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

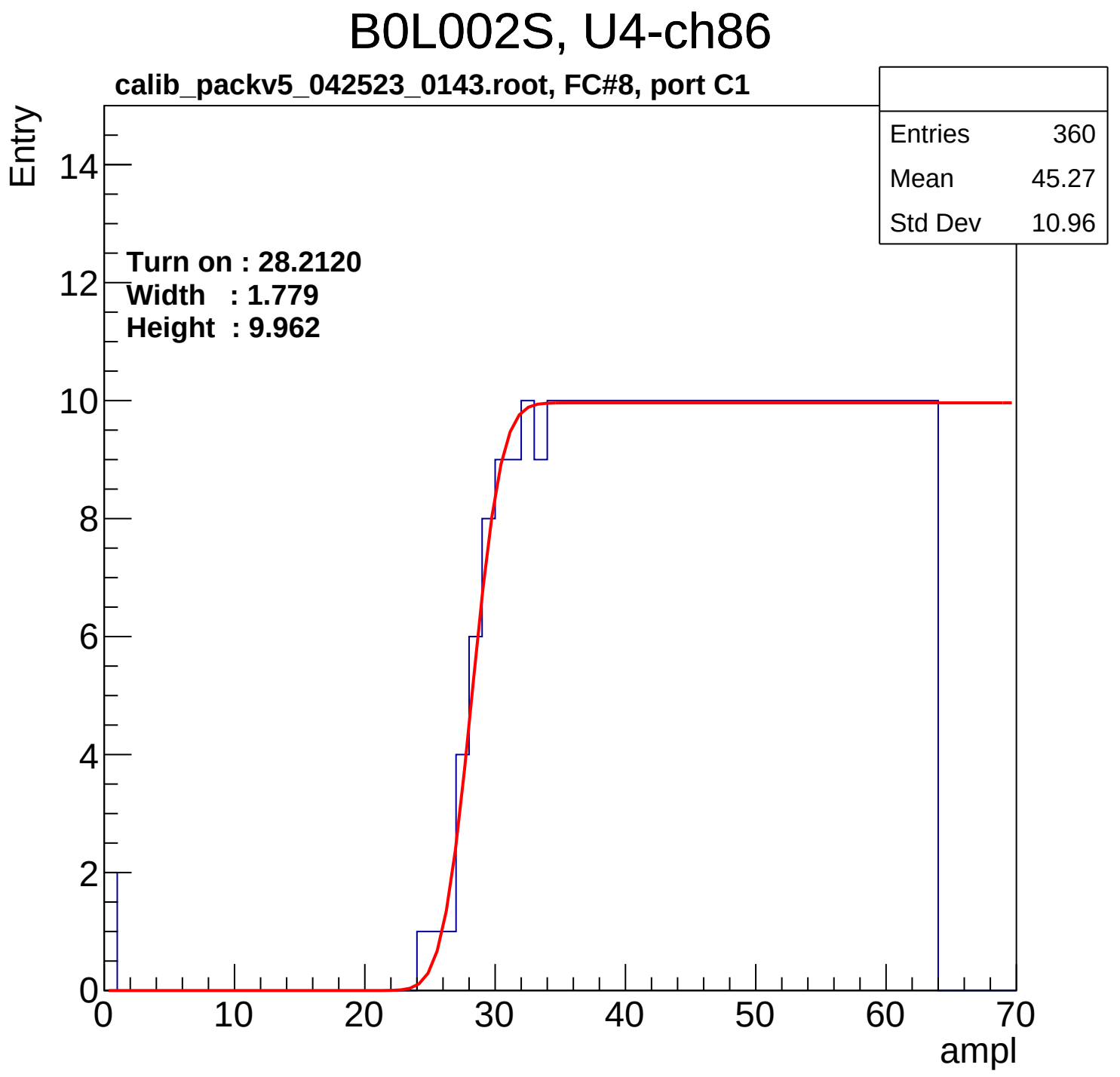

B0L002S, U4-ch81
calib_packv5_042523_0143.root, FC#8, port C1
Entries 379
Mean 44.36
Std Dev 11.32
Turn on : 25.8510
Width : 1.794
Height : 9.843
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

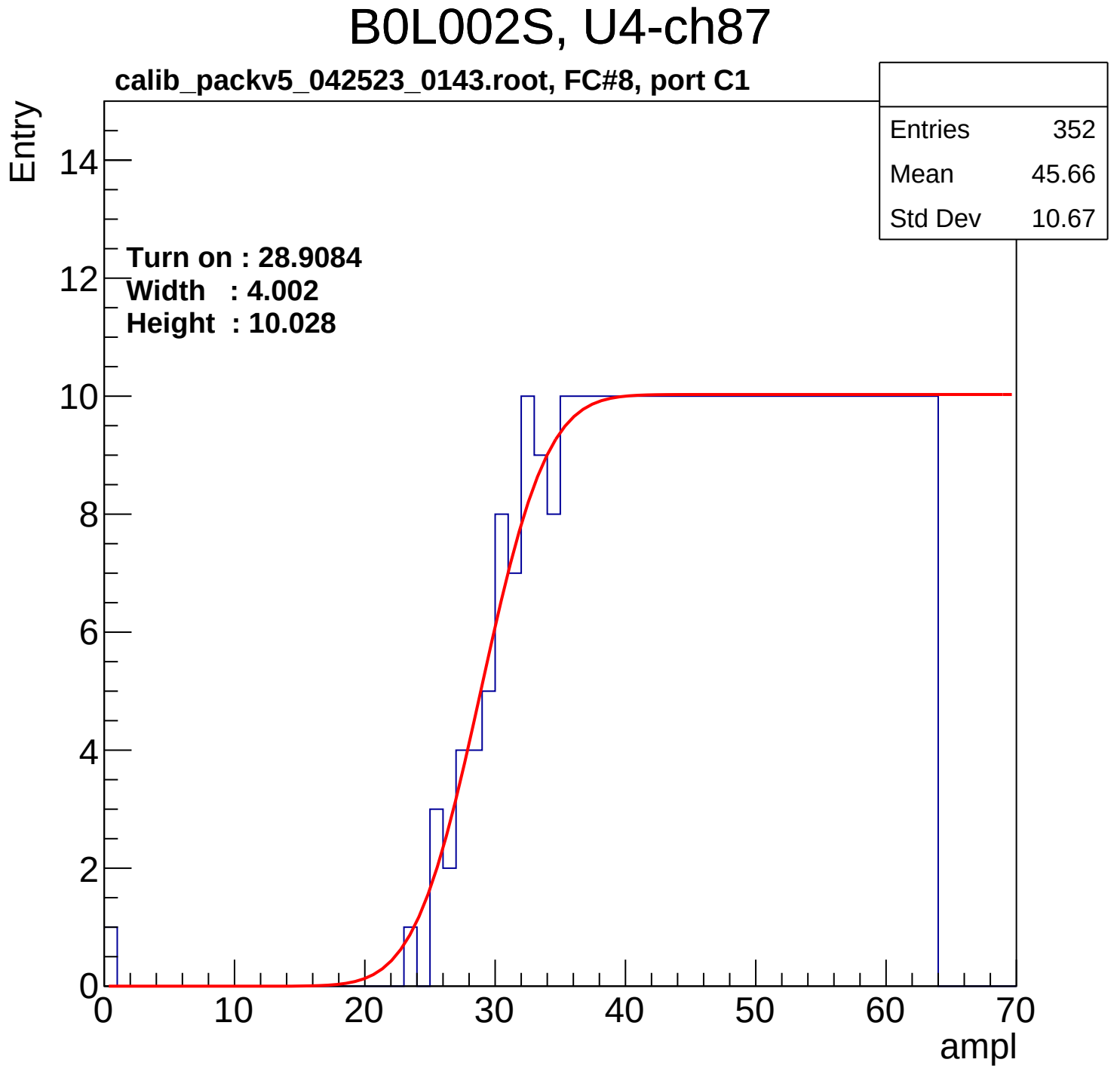

B0L002S, U4-ch82
calib_packv5_042523_0143.root, FC#8, port C1
Entries 368
Mean 44.88
Std Dev 11.17
Turn on : 27.5378
Width : 2.589
Height : 10.019
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

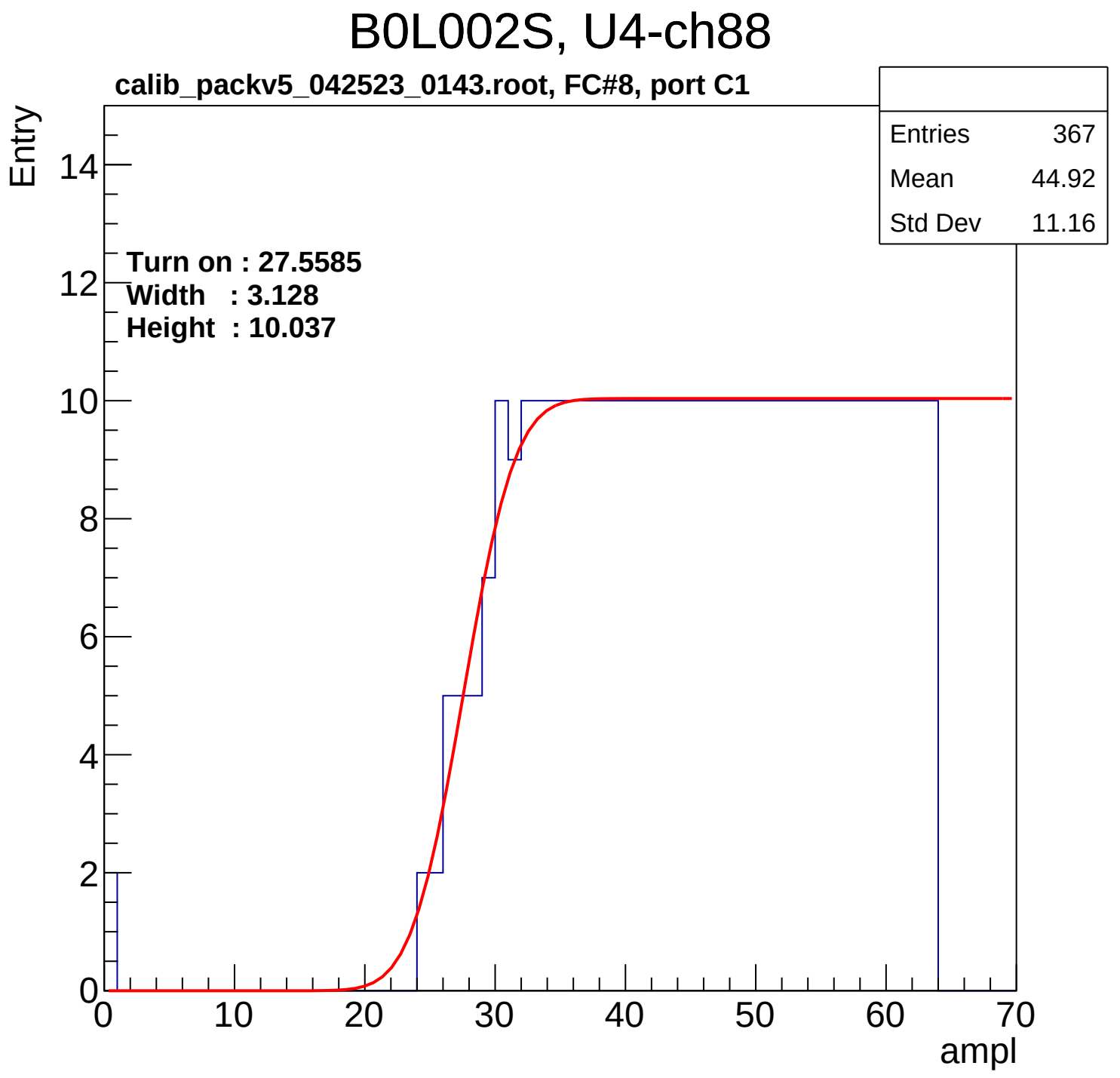

B0L002S, U4-ch83
calib_packv5_042523_0143.root, FC#8, port C1
Entries 365
Mean 44.85
Std Dev 11.55
Turn on : 28.1052
Width : 3.030
Height : 10.026
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

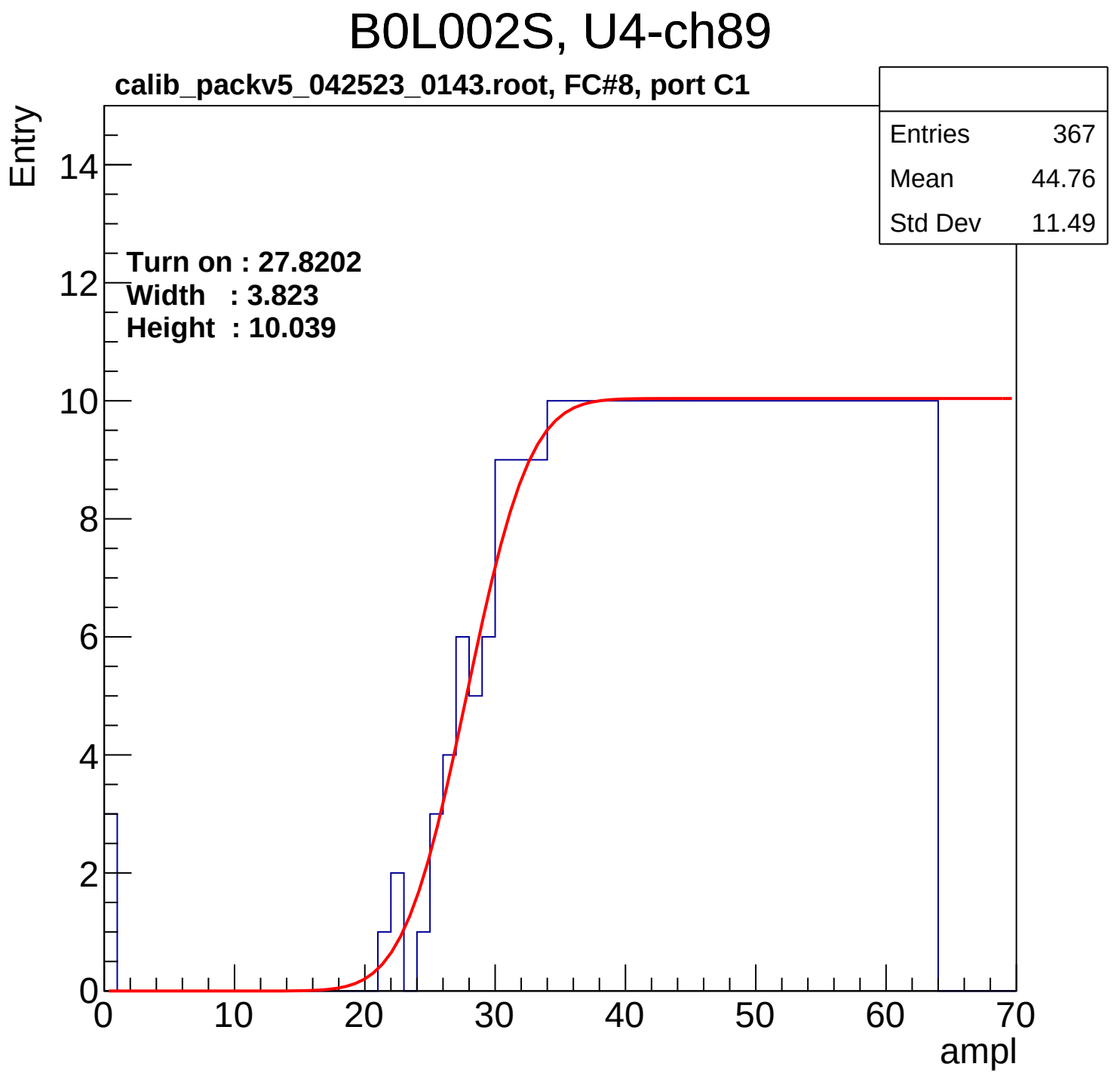

B0L002S, U4-ch84
calib_packv5_042523_0143.root, FC#8, port C1
Entries 362
Mean 45.03
Std Dev 11.43
Turn on : 28.1188
Width : 2.619
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

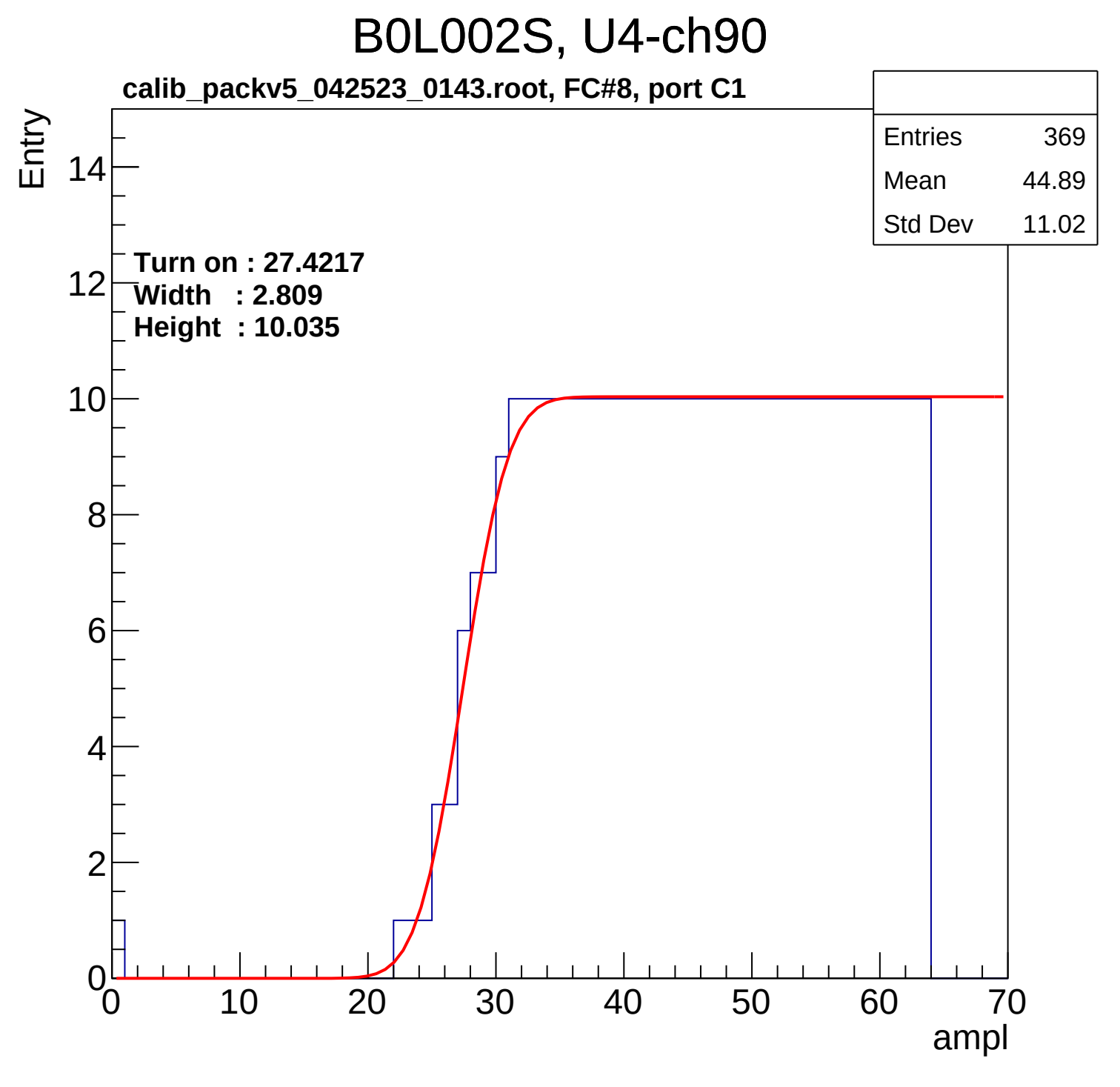

B0L002S, U4-ch85
calib_packv5_042523_0143.root, FC#8, port C1
Entries 365
Mean 45.04
Std Dev 10.98
Turn on : 27.4923
Width : 3.849
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

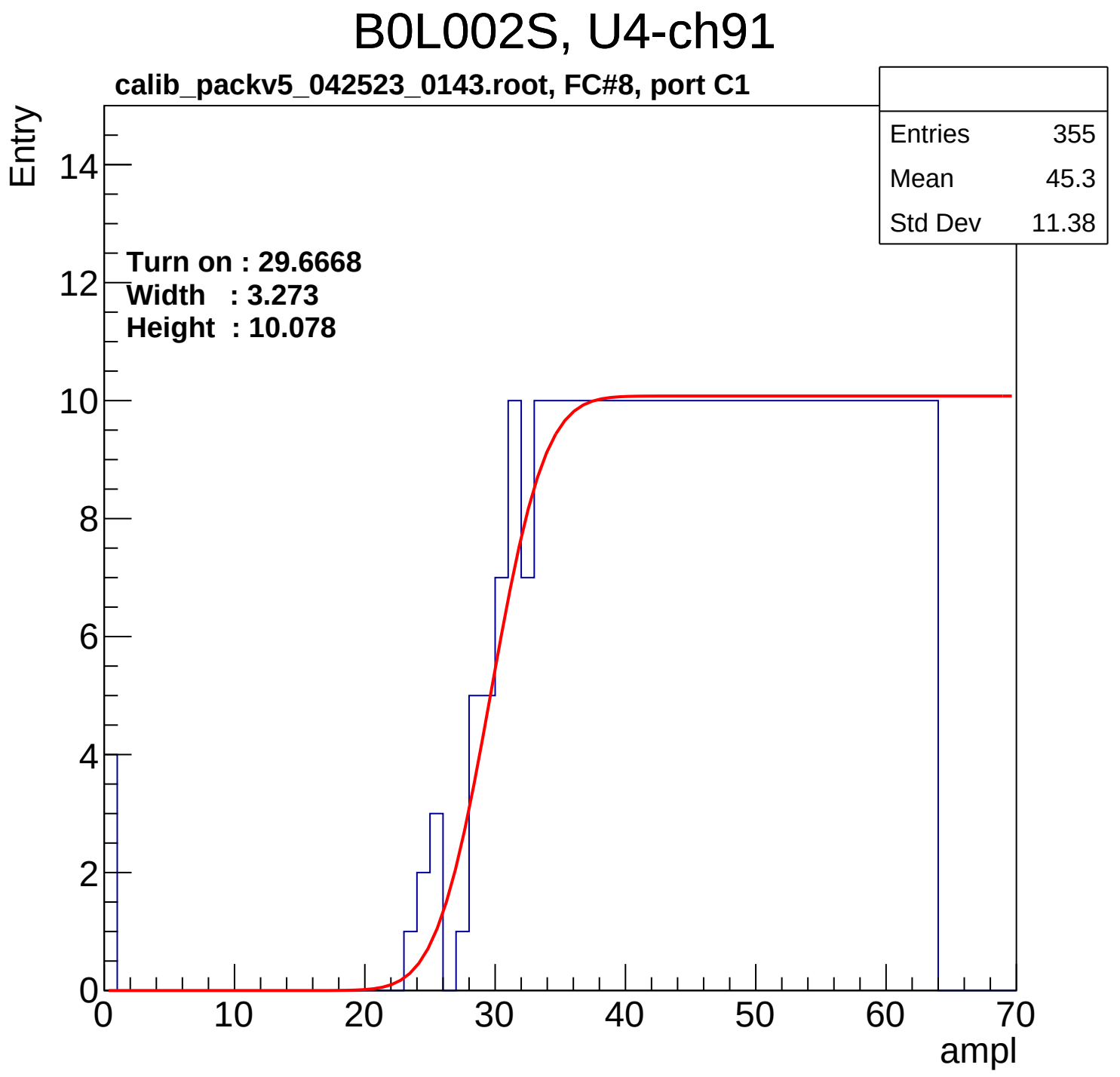

B0L002S, U4-ch86
calib_packv5_042523_0143.root, FC#8, port C1
Entries 360
Mean 45.27
Std Dev 10.96
Turn on : 28.2120
Width : 1.779
Height : 9.962
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

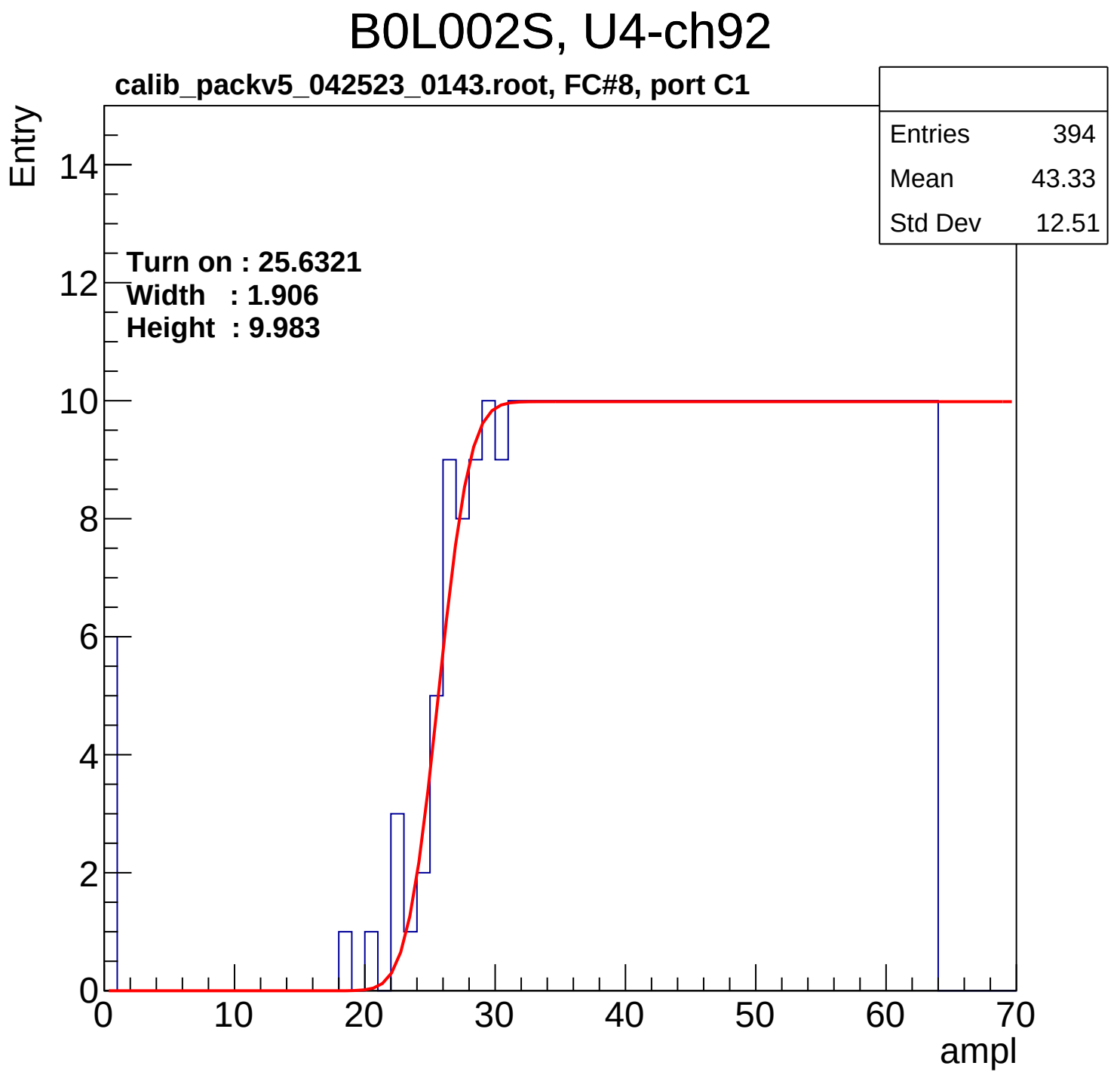

B0L002S, U4-ch87
calib_packv5_042523_0143.root, FC#8, port C1
Entries 352
Mean 45.66
Std Dev 10.67
Turn on : 28.9084
Width : 4.002
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

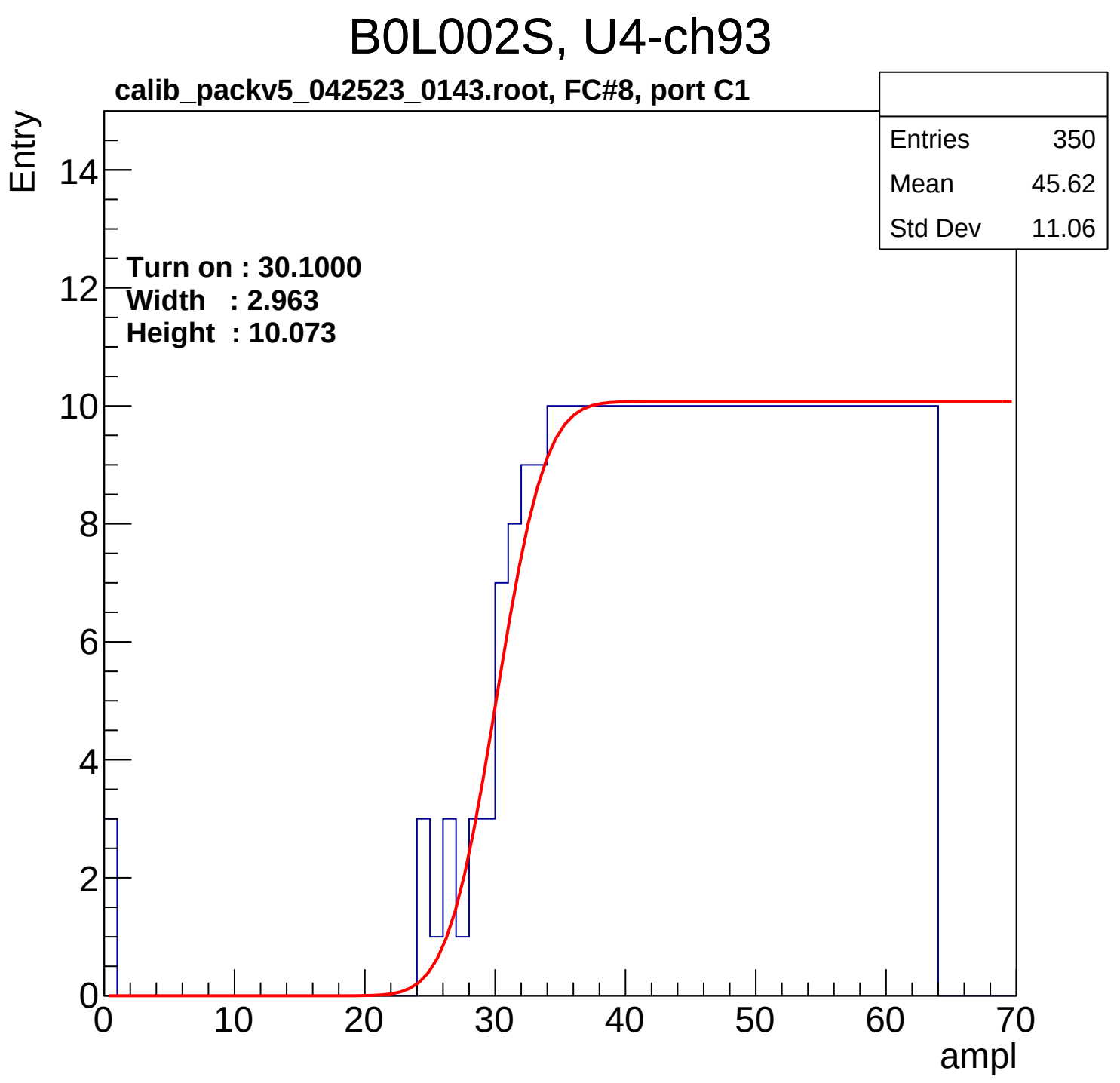

B0L002S, U4-ch88
calib_packv5_042523_0143.root, FC#8, port C1
Entries 367
Mean 44.92
Std Dev 11.16
Turn on : 27.5585
Width : 3.128
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

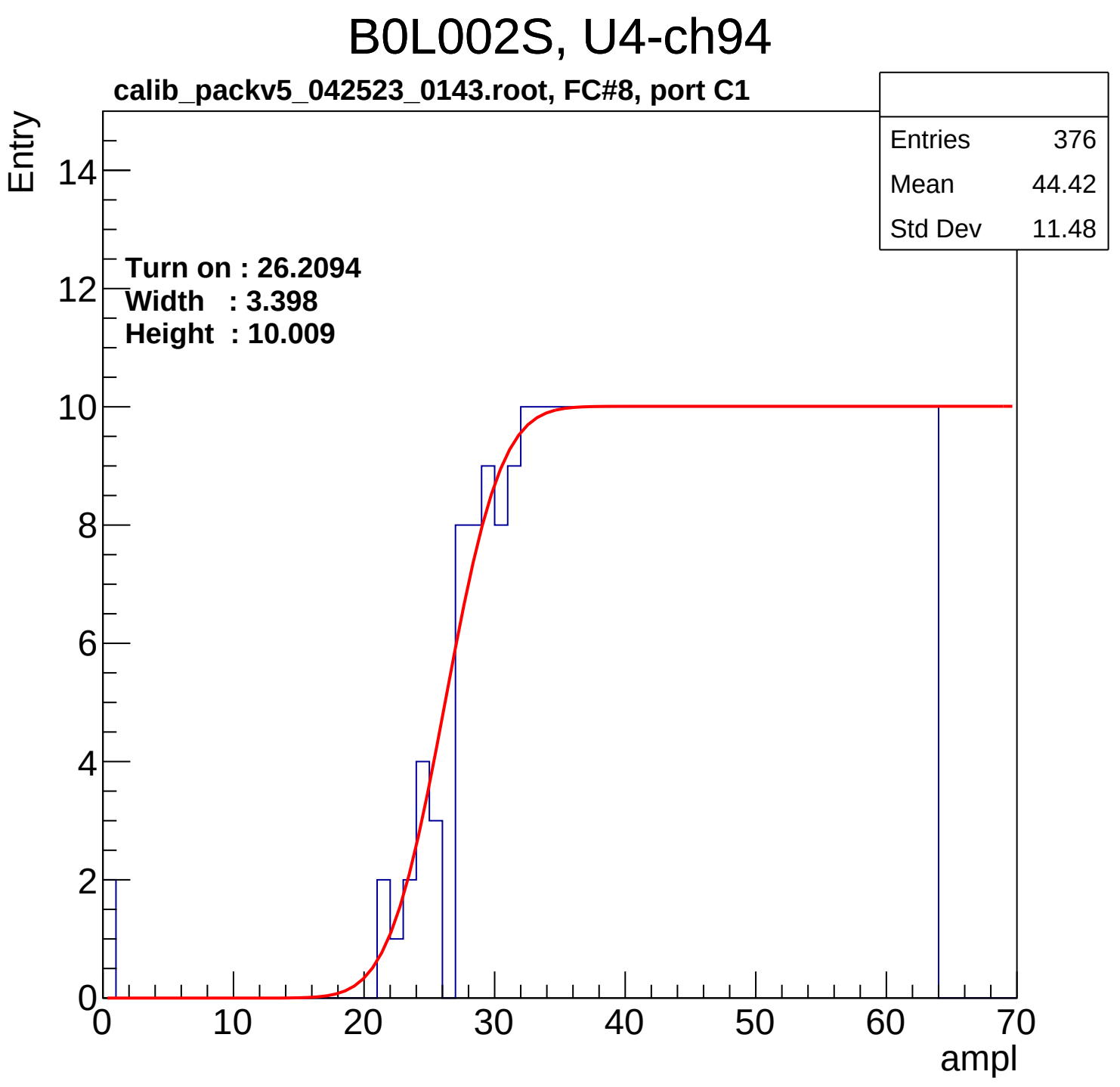

B0L002S, U4-ch89
calib_packv5_042523_0143.root, FC#8, port C1
Entries 367
Mean 44.76
Std Dev 11.49
Turn on : 27.8202
Width : 3.823
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

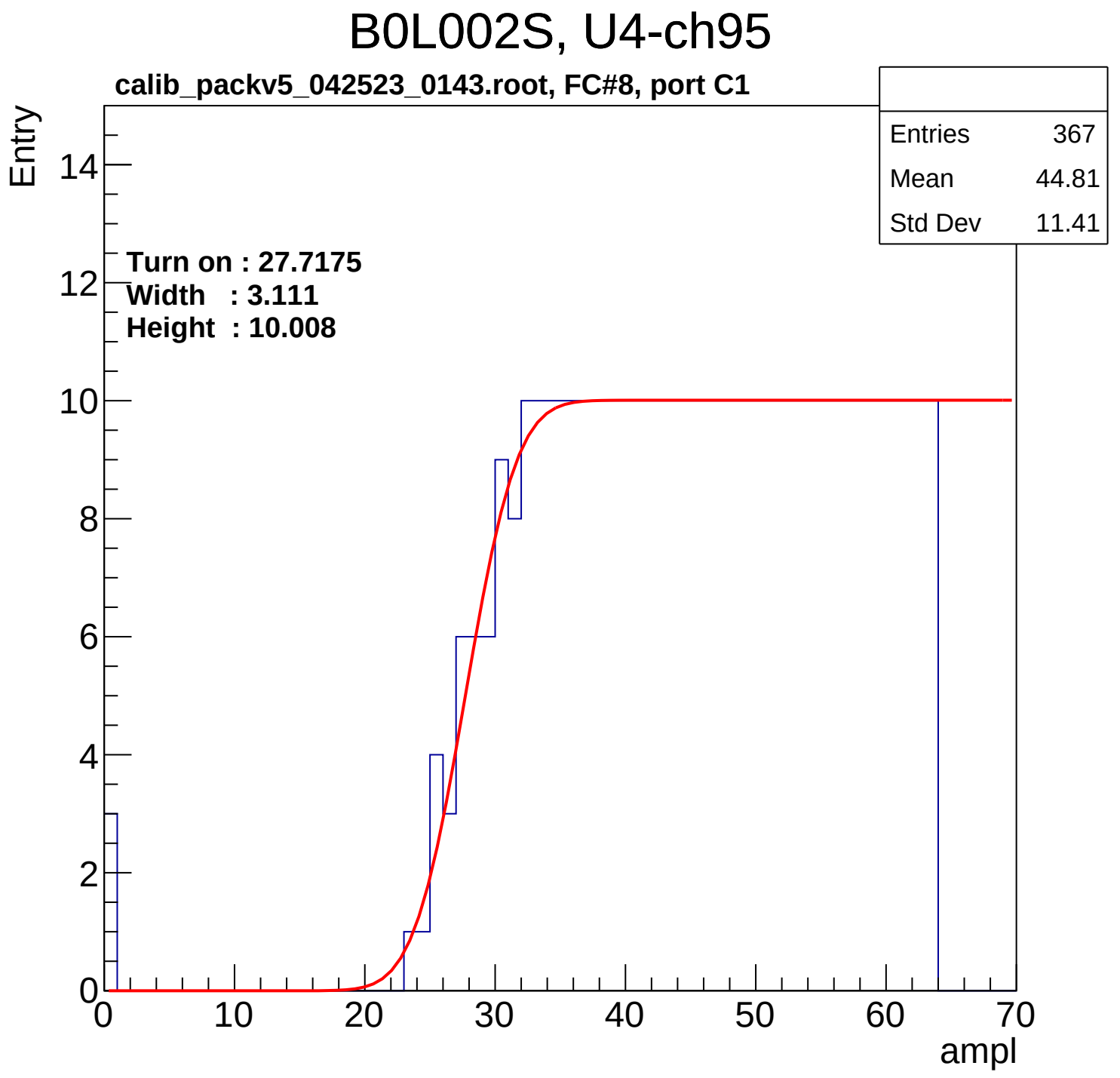

B0L002S, U4-ch90
calib_packv5_042523_0143.root, FC#8, port C1
Entries 369
Mean 44.89
Std Dev 11.02
Turn on : 27.4217
Width : 2.809
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

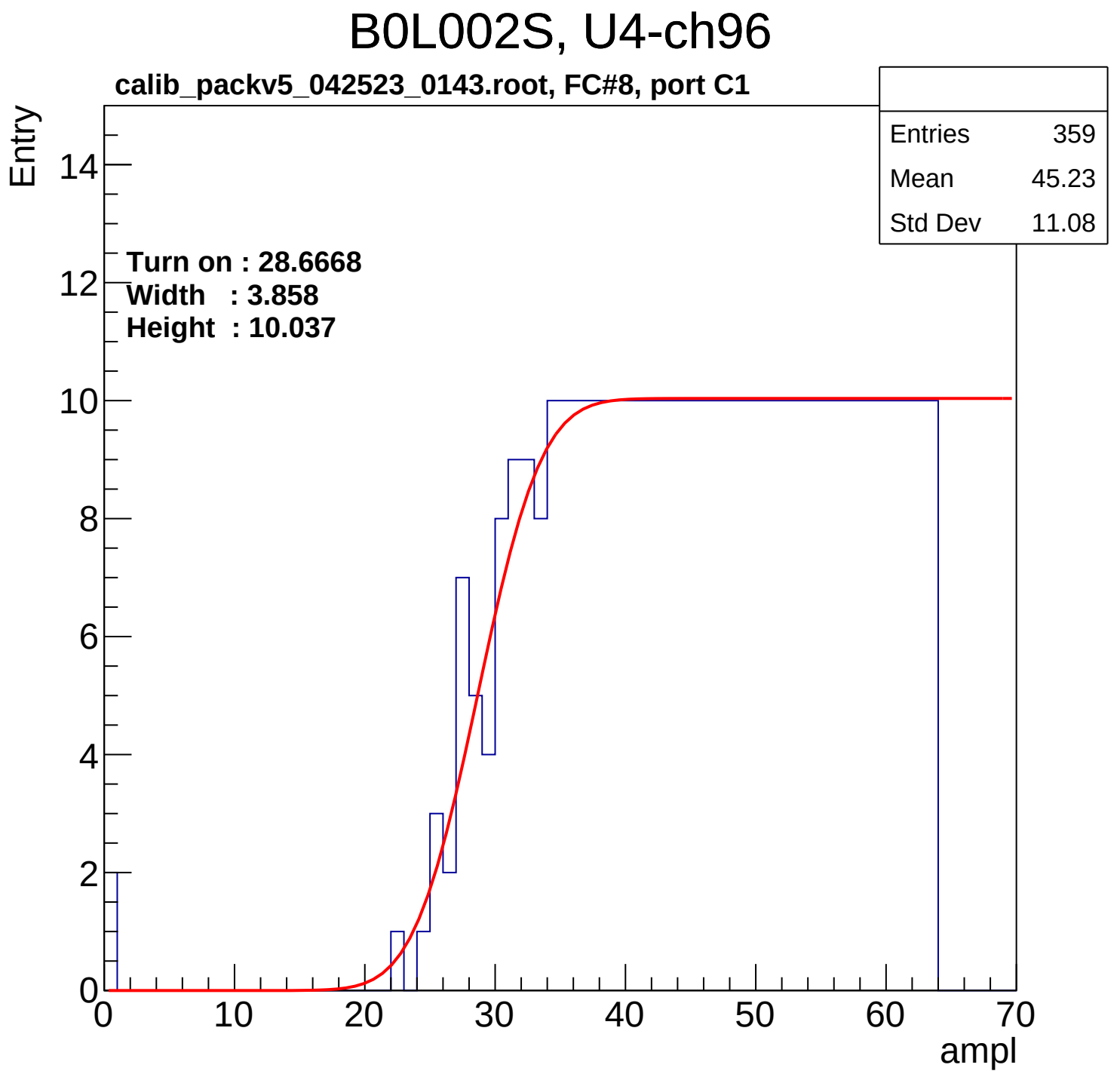

B0L002S, U4-ch91
calib_packv5_042523_0143.root, FC#8, port C1
Entries 355
Mean 45.3
Std Dev 11.38
Turn on : 29.6668
Width : 3.273
Height : 10.078
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

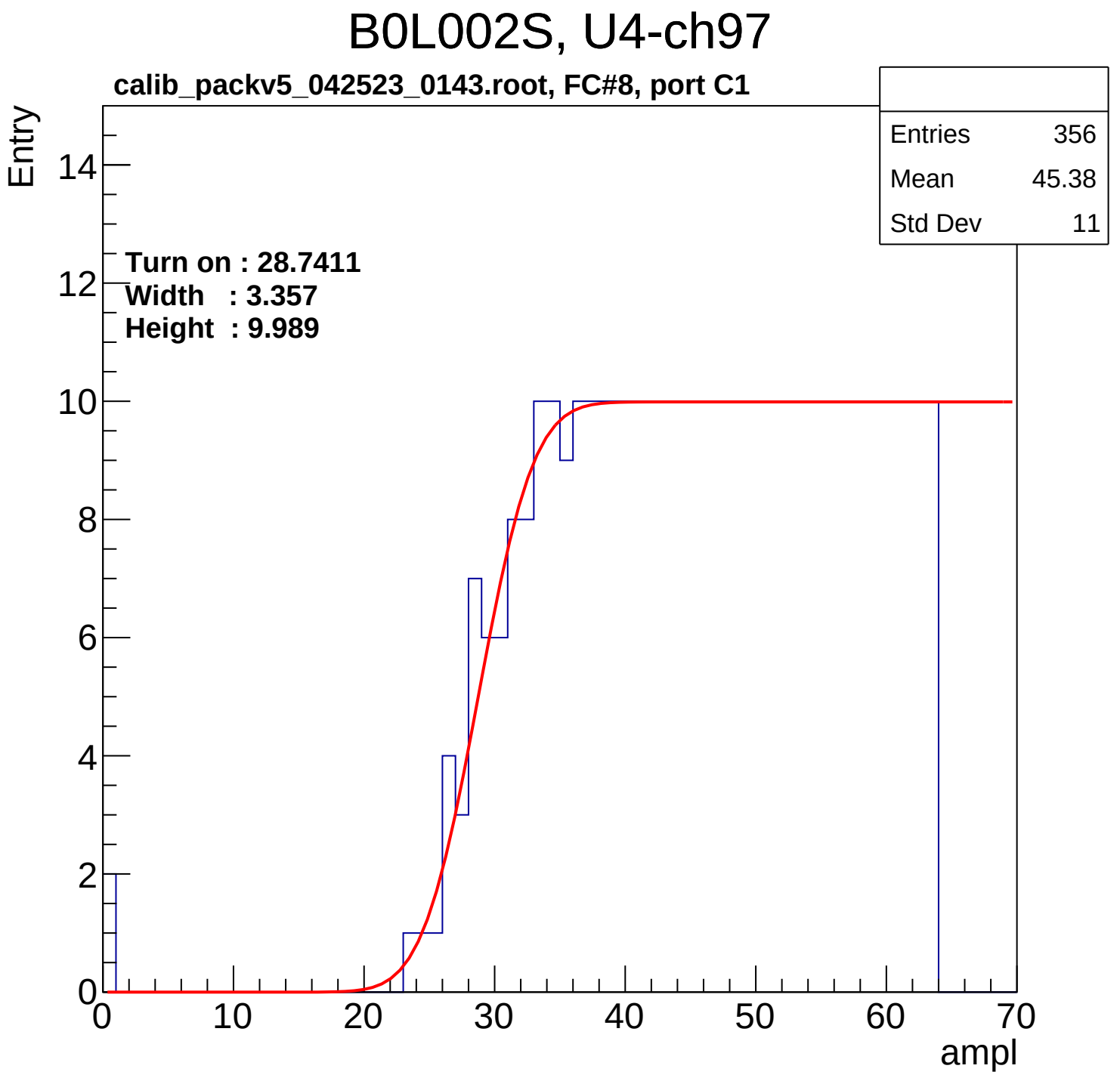

B0L002S, U4-ch92
calib_packv5_042523_0143.root, FC#8, port C1
Entries 394
Mean 43.33
Std Dev 12.51
Turn on : 25.6321
Width : 1.906
Height : 9.983
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

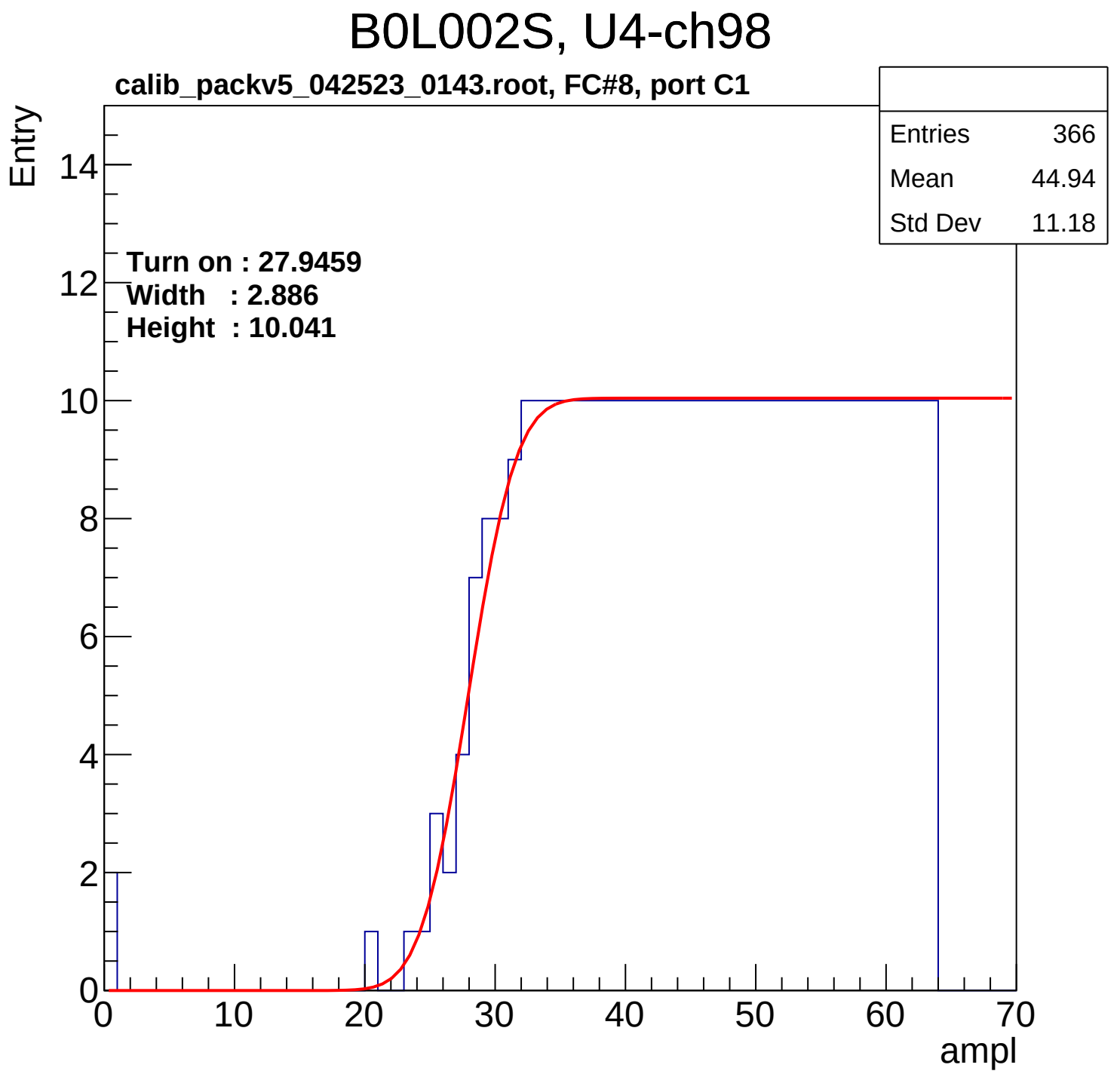

B0L002S, U4-ch93
calib_packv5_042523_0143.root, FC#8, port C1
Entries 350
Mean 45.62
Std Dev 11.06
Turn on : 30.1000
Width : 2.963
Height : 10.073
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

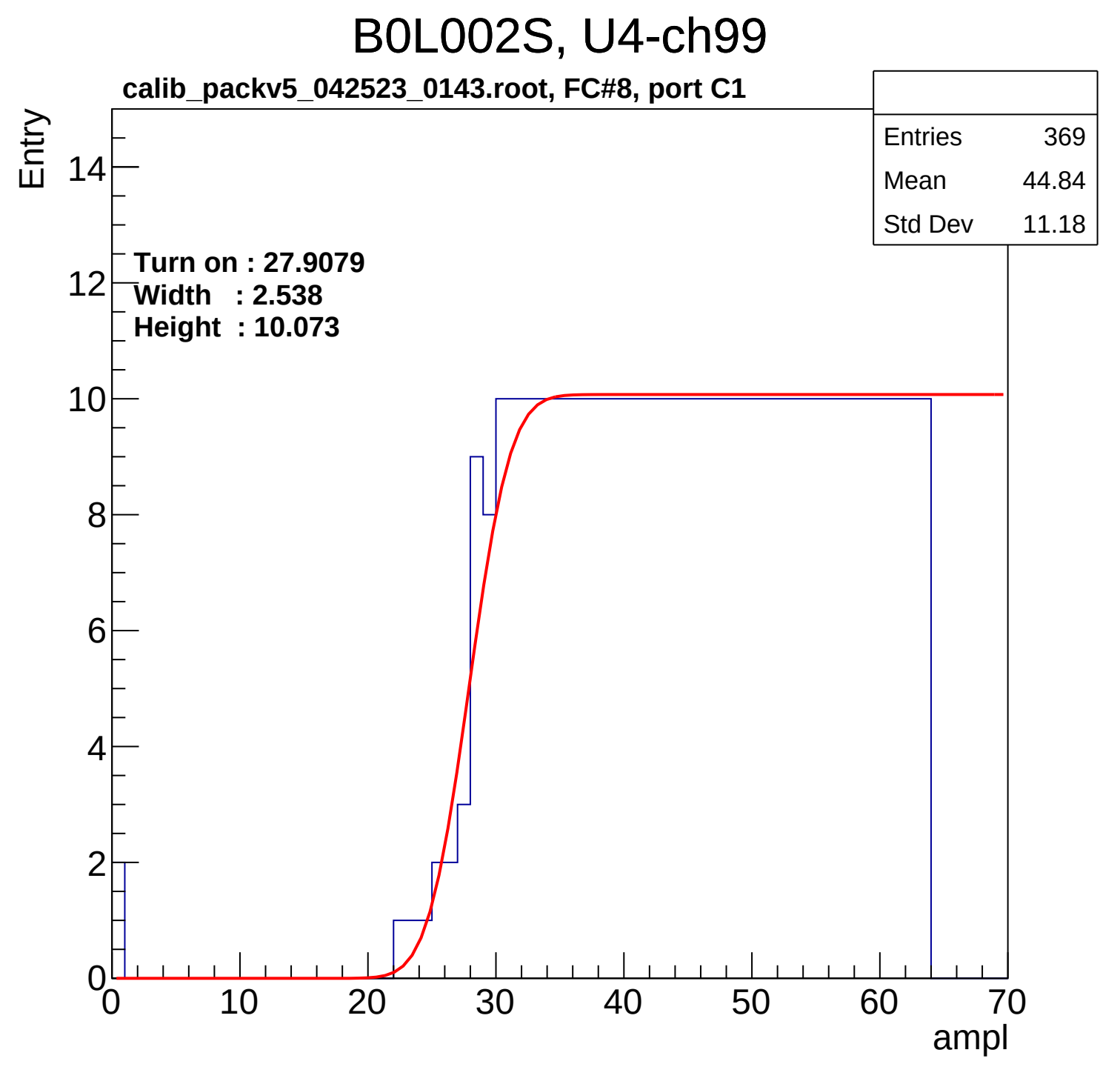

B0L002S, U4-ch94
calib_packv5_042523_0143.root, FC#8, port C1
Entries 376
Mean 44.42
Std Dev 11.48
Turn on : 26.2094
Width : 3.398
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

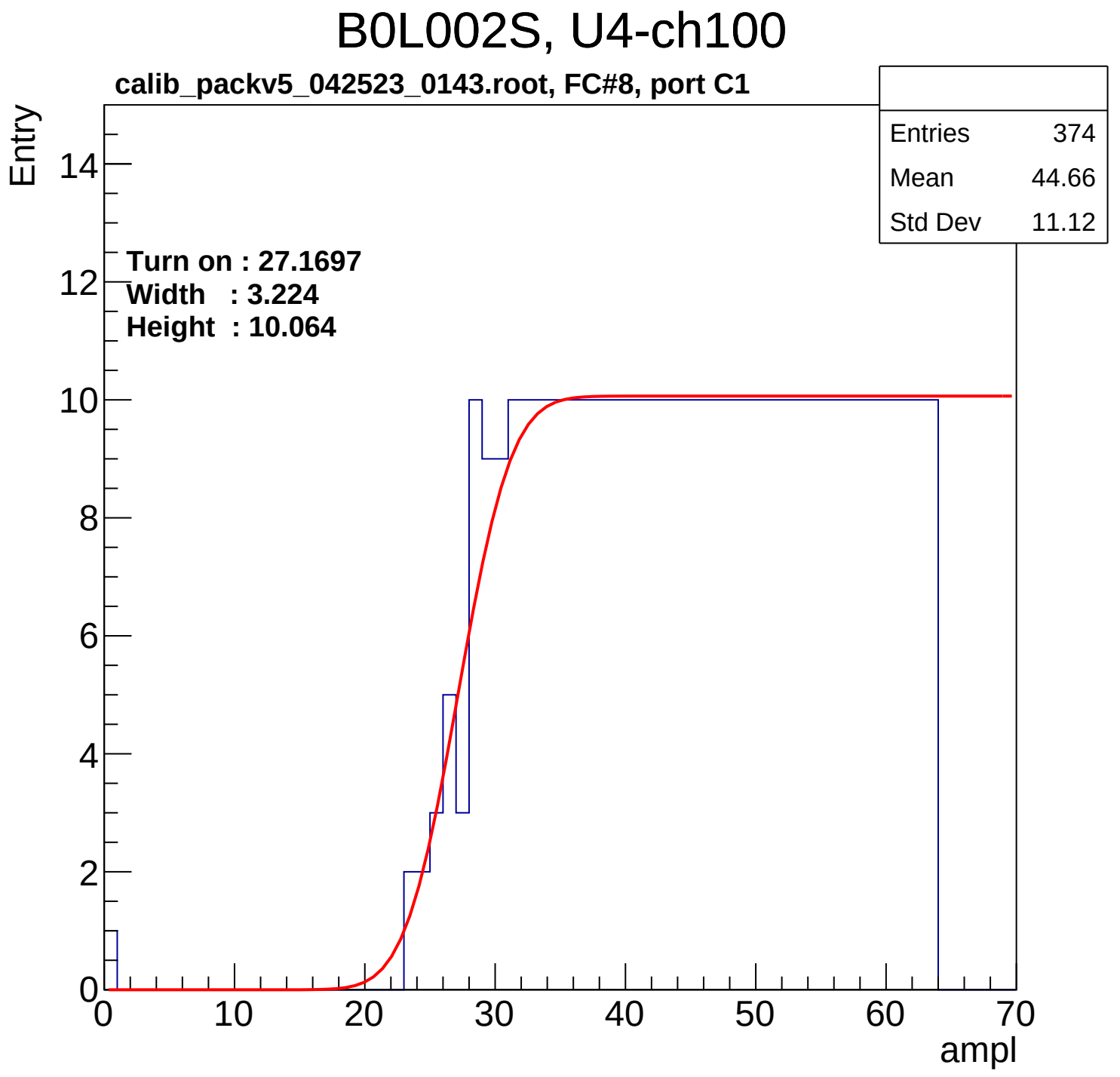

B0L002S, U4-ch95
calib_packv5_042523_0143.root, FC#8, port C1
Entries 367
Mean 44.81
Std Dev 11.41
Turn on : 27.7175
Width : 3.111
Height : 10.008
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

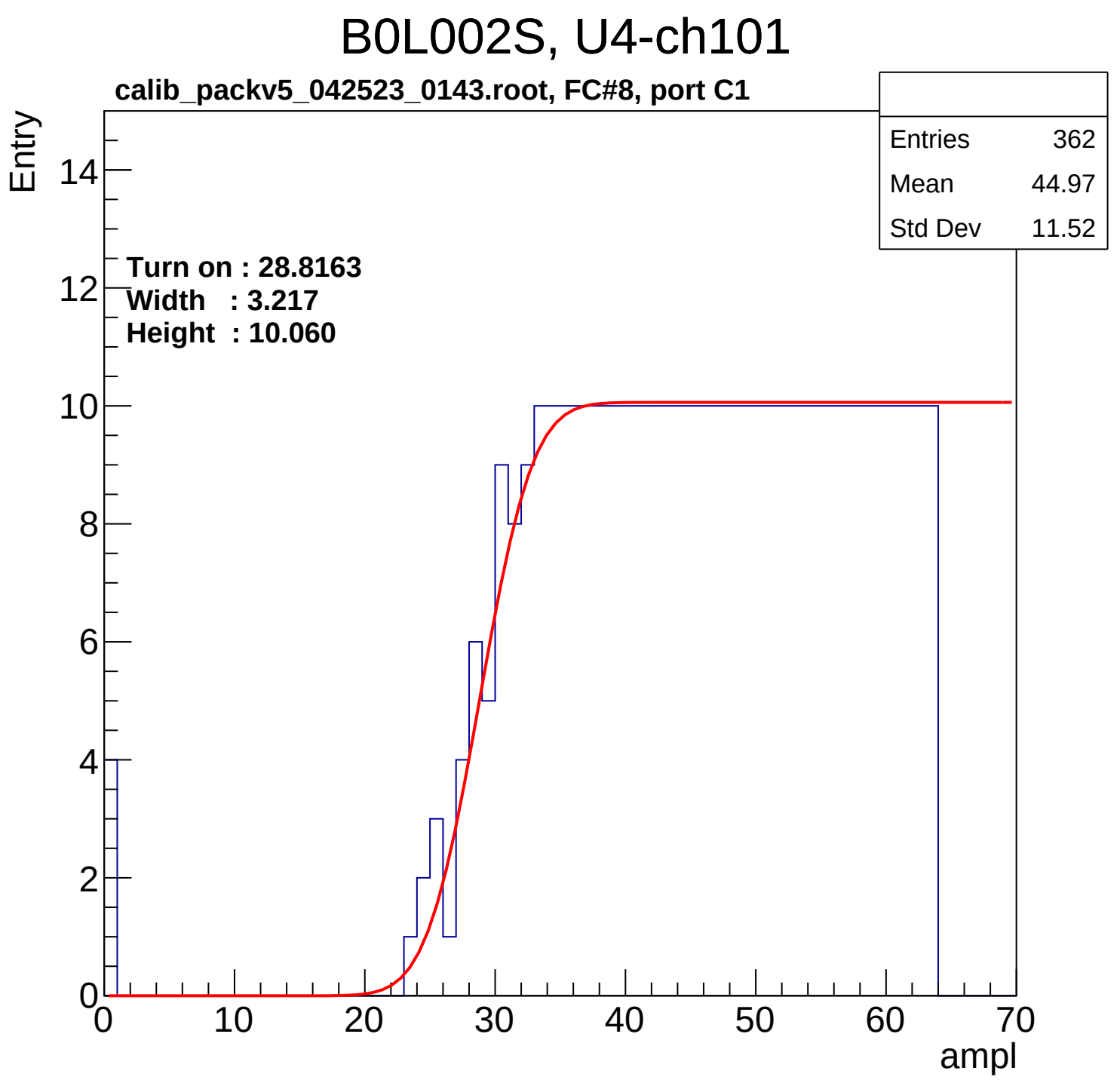

B0L002S, U4-ch96
calib_packv5_042523_0143.root, FC#8, port C1
Entries 359
Mean 45.23
Std Dev 11.08
Turn on : 28.6668
Width : 3.858
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

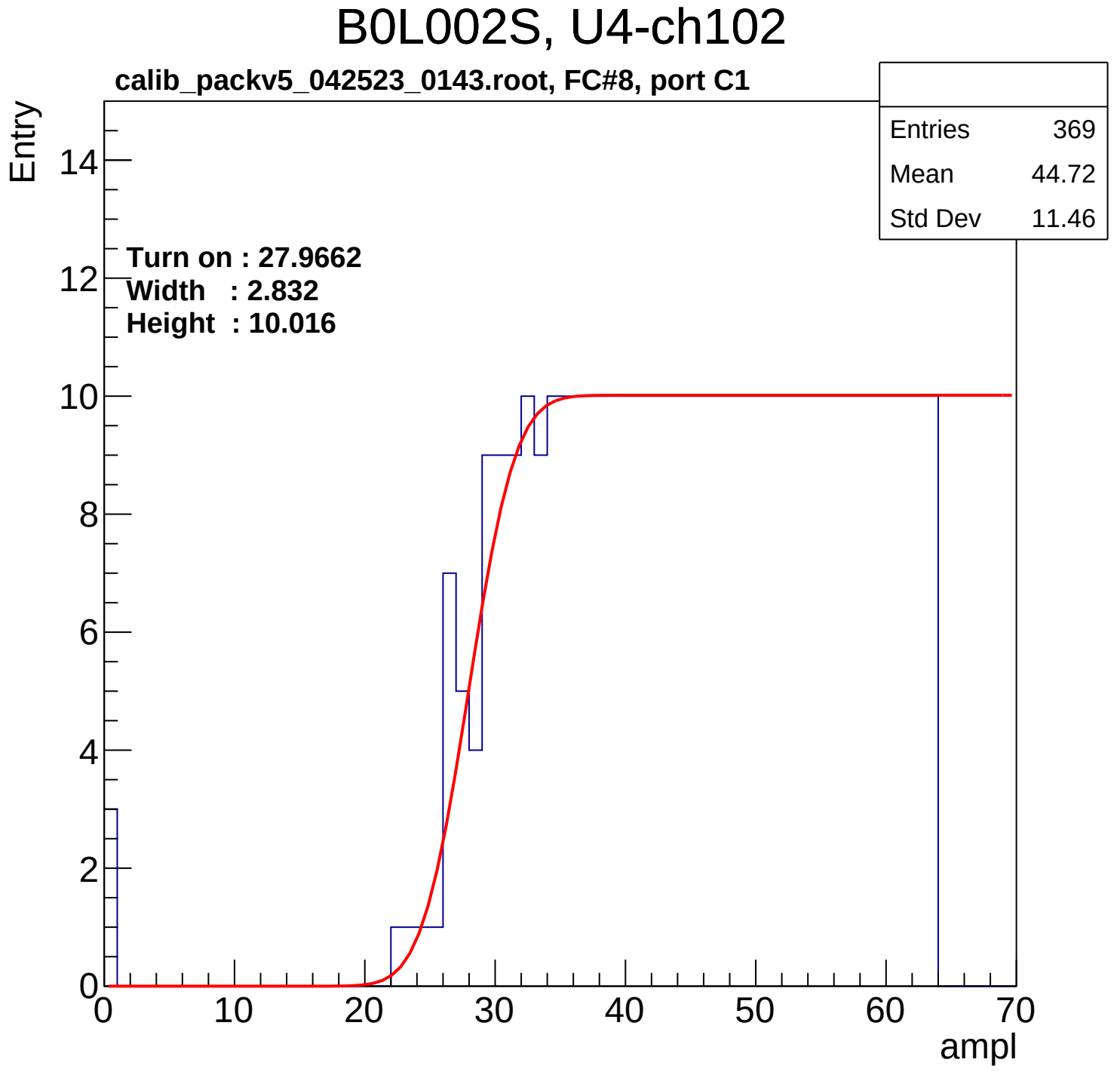

B0L002S, U4-ch97
calib_packv5_042523_0143.root, FC#8, port C1
Entries 356
Mean 45.38
Std Dev 11
Turn on : 28.7411
Width : 3.357
Height : 9.989
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

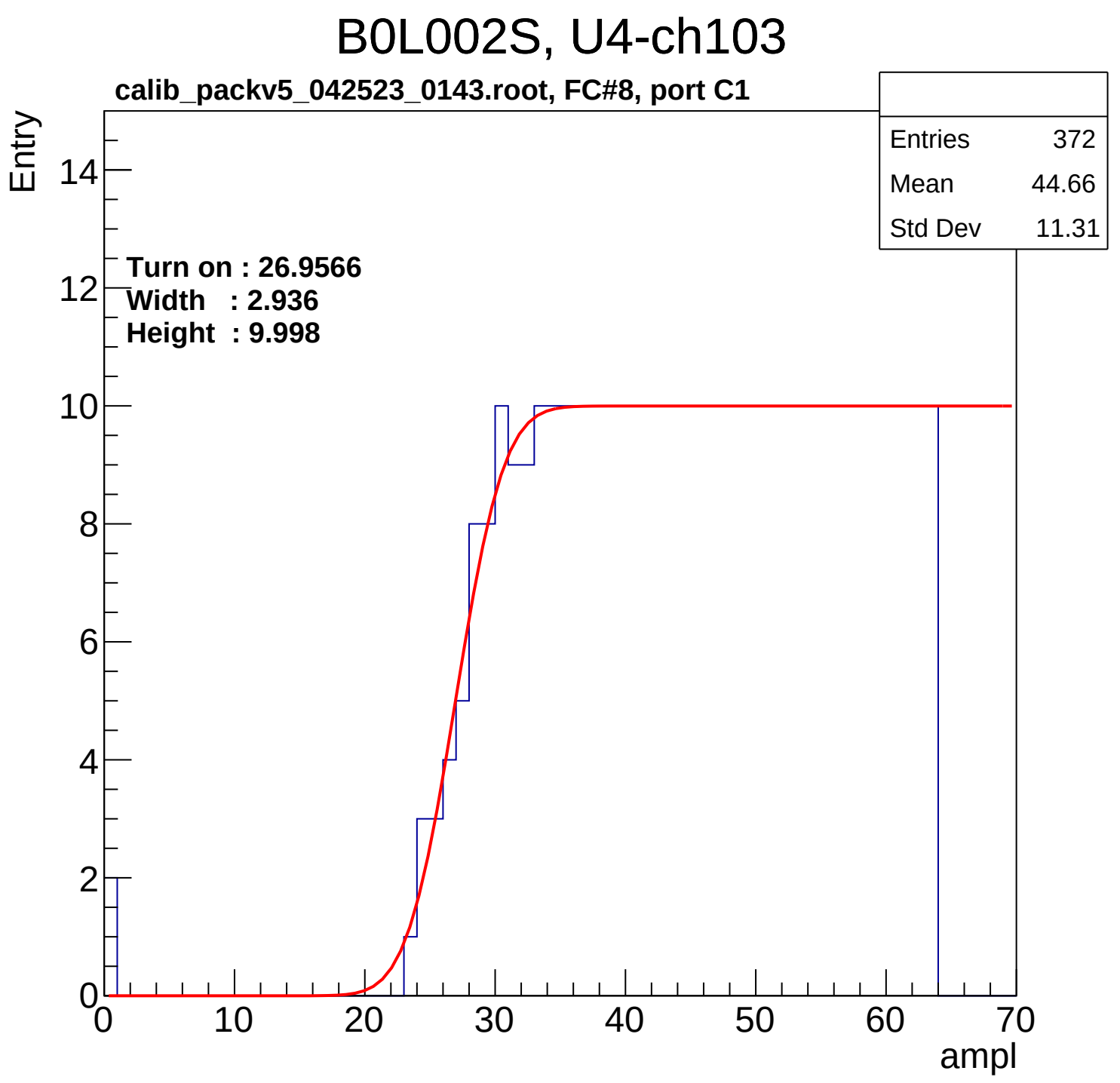

B0L002S, U4-ch98
calib_packv5_042523_0143.root, FC#8, port C1
Entries 366
Mean 44.94
Std Dev 11.18
Turn on : 27.9459
Width : 2.886
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

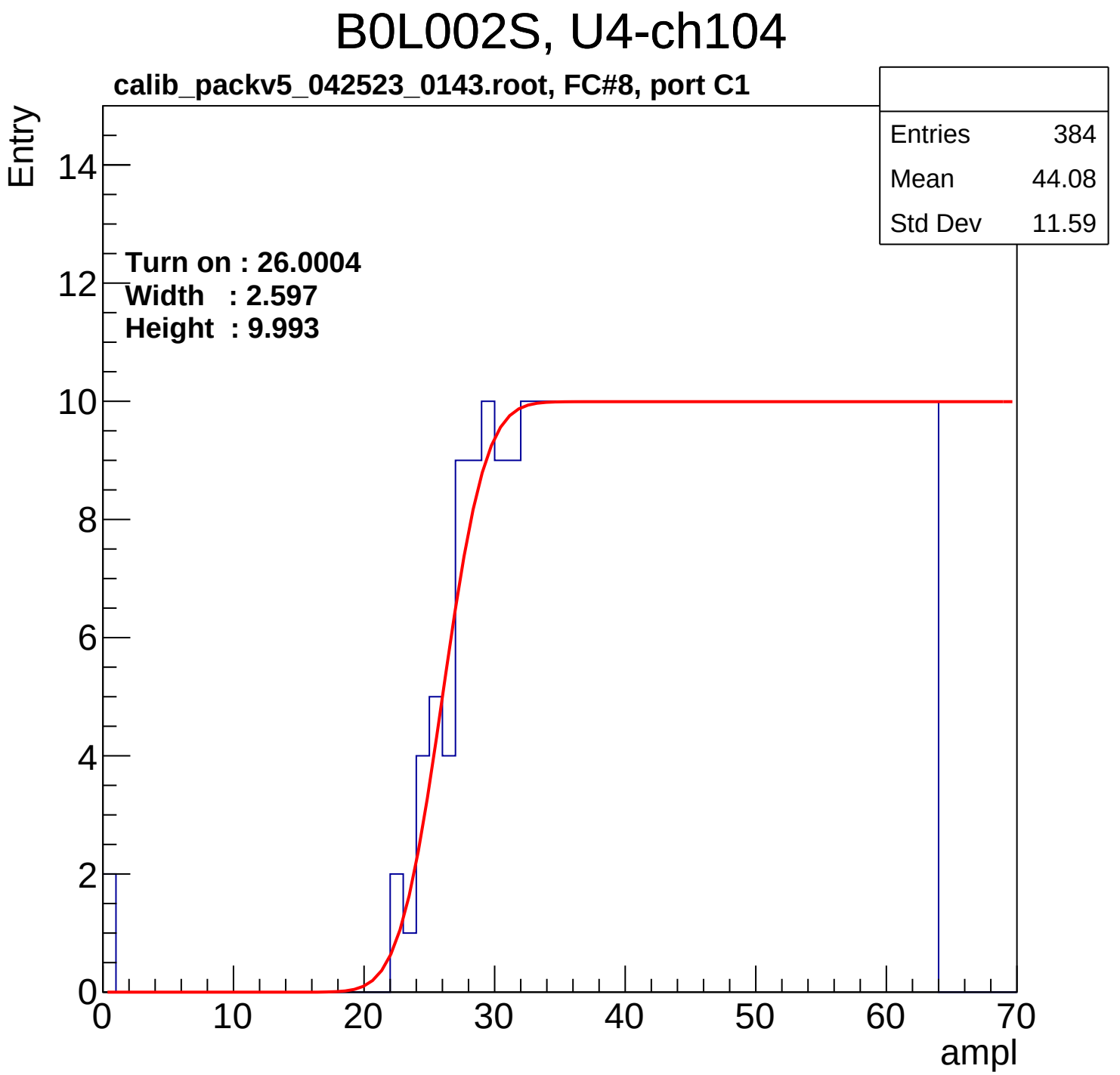

B0L002S, U4-ch99
calib_packv5_042523_0143.root, FC#8, port C1
Entries 369
Mean 44.84
Std Dev 11.18
Turn on : 27.9079
Width : 2.538
Height : 10.073
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

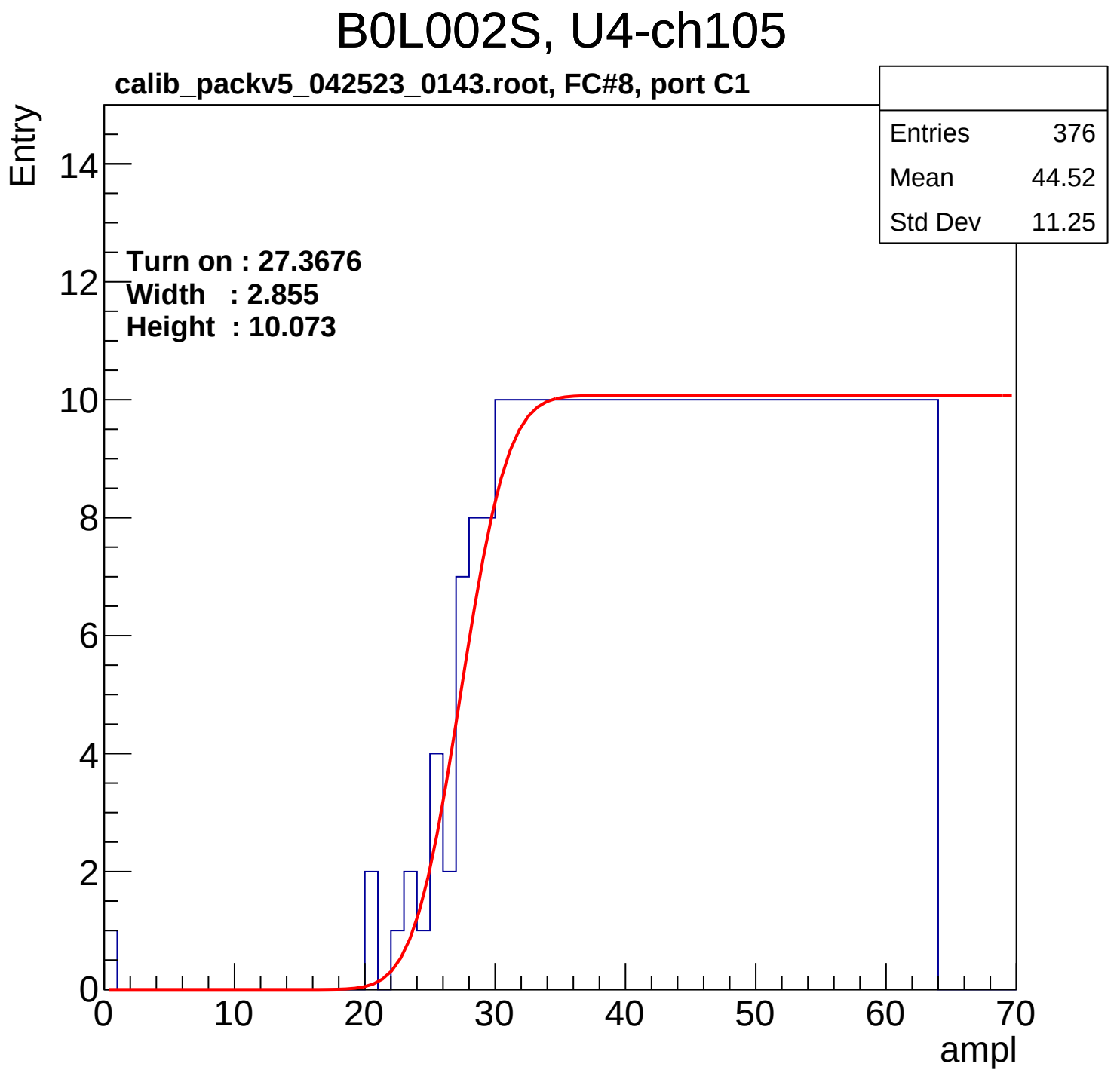

B0L002S, U4-ch100
calib_packv5_042523_0143.root, FC#8, port C1
Entries 374
Mean 44.66
Std Dev 11.12
Turn on : 27.1697
Width : 3.224
Height : 10.064
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

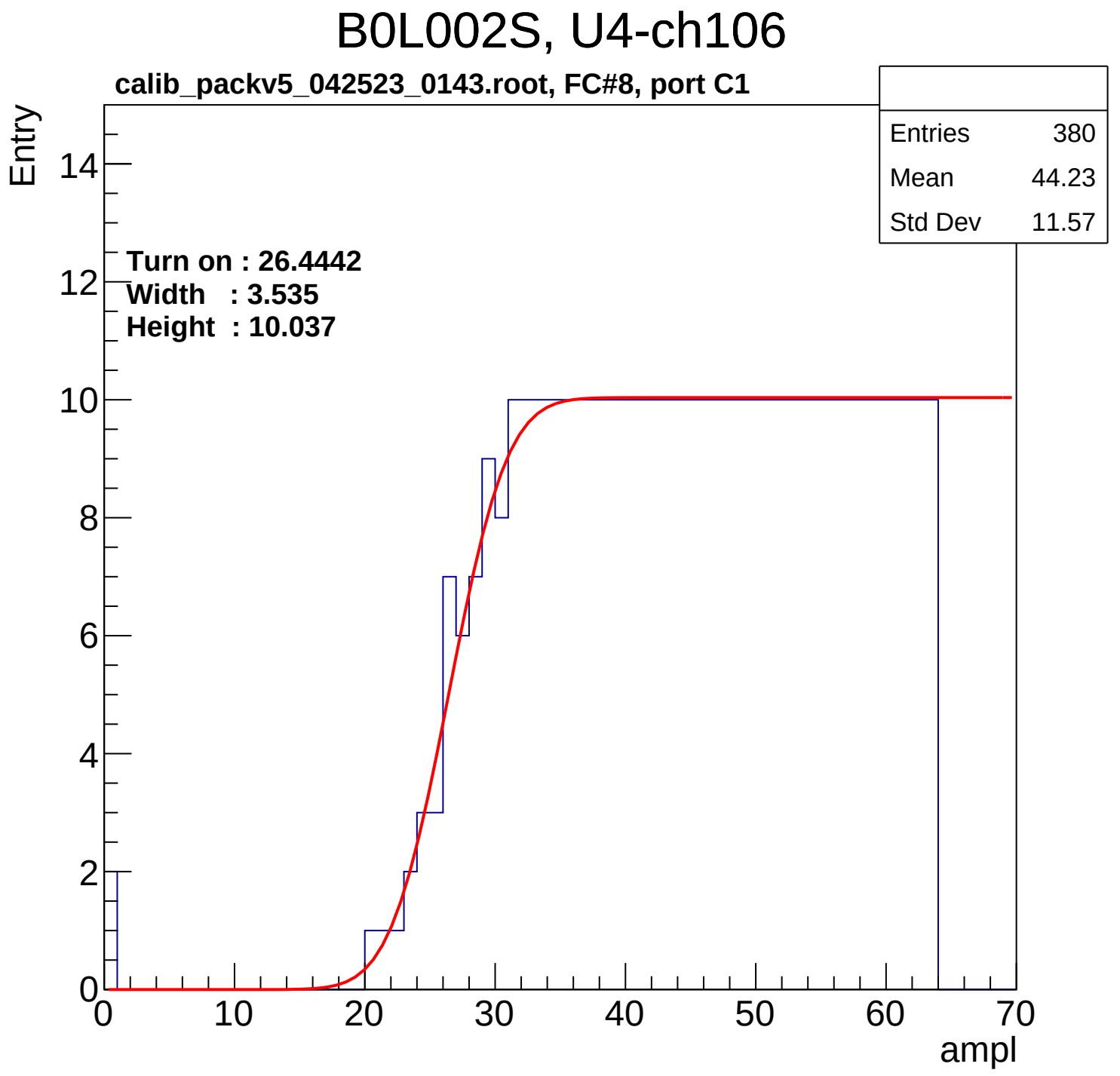

B0L002S, U4-ch101
calib_packv5_042523_0143.root, FC#8, port C1
Entries 362
Mean 44.97
Std Dev 11.52
Turn on : 28.8163
Width : 3.217
Height : 10.060
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

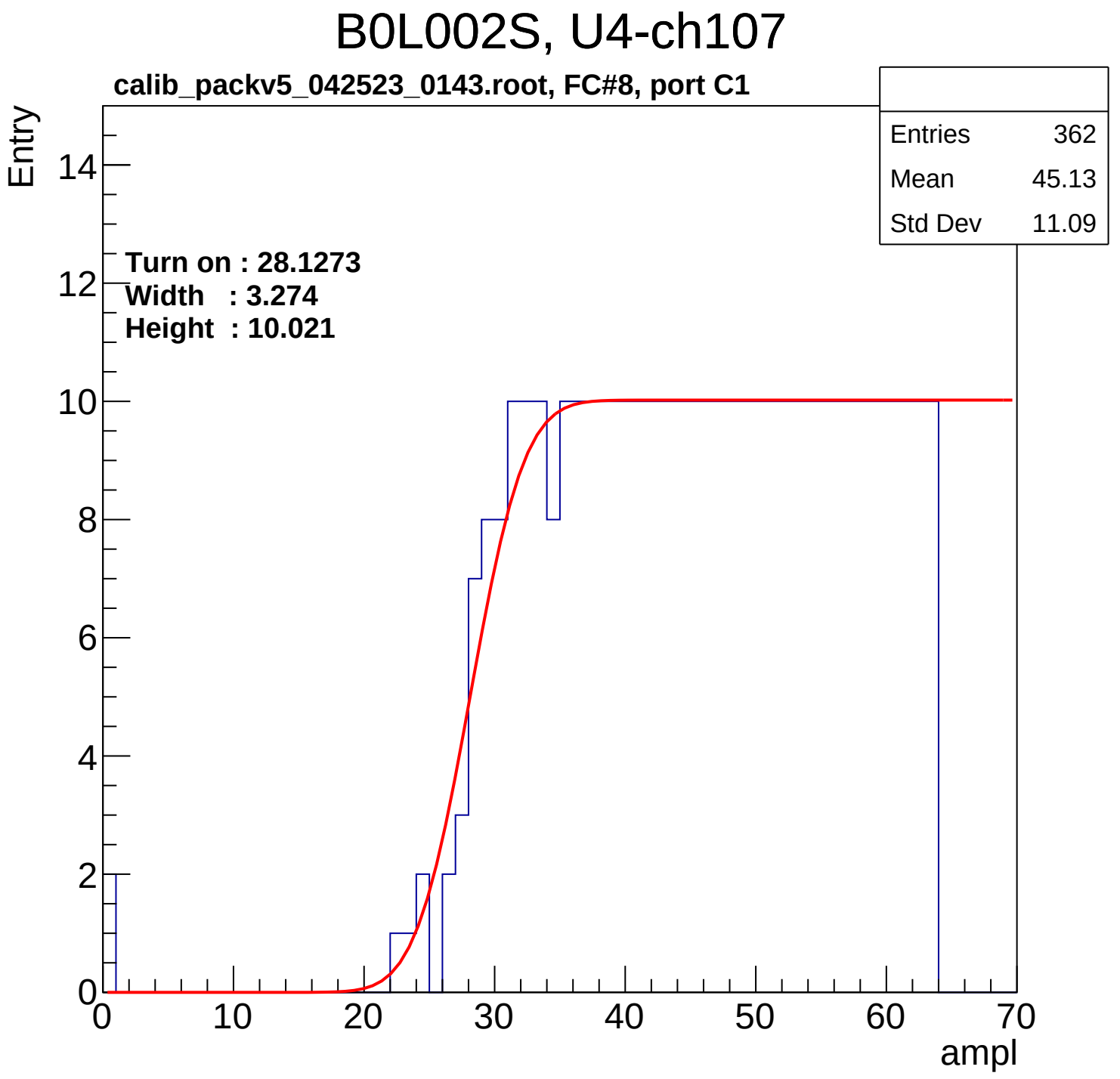

B0L002S, U4-ch102
calib_packv5_042523_0143.root, FC#8, port C1
Entries 369
Mean 44.72
Std Dev 11.46
Turn on : 27.9662
Width : 2.832
Height : 10.016
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

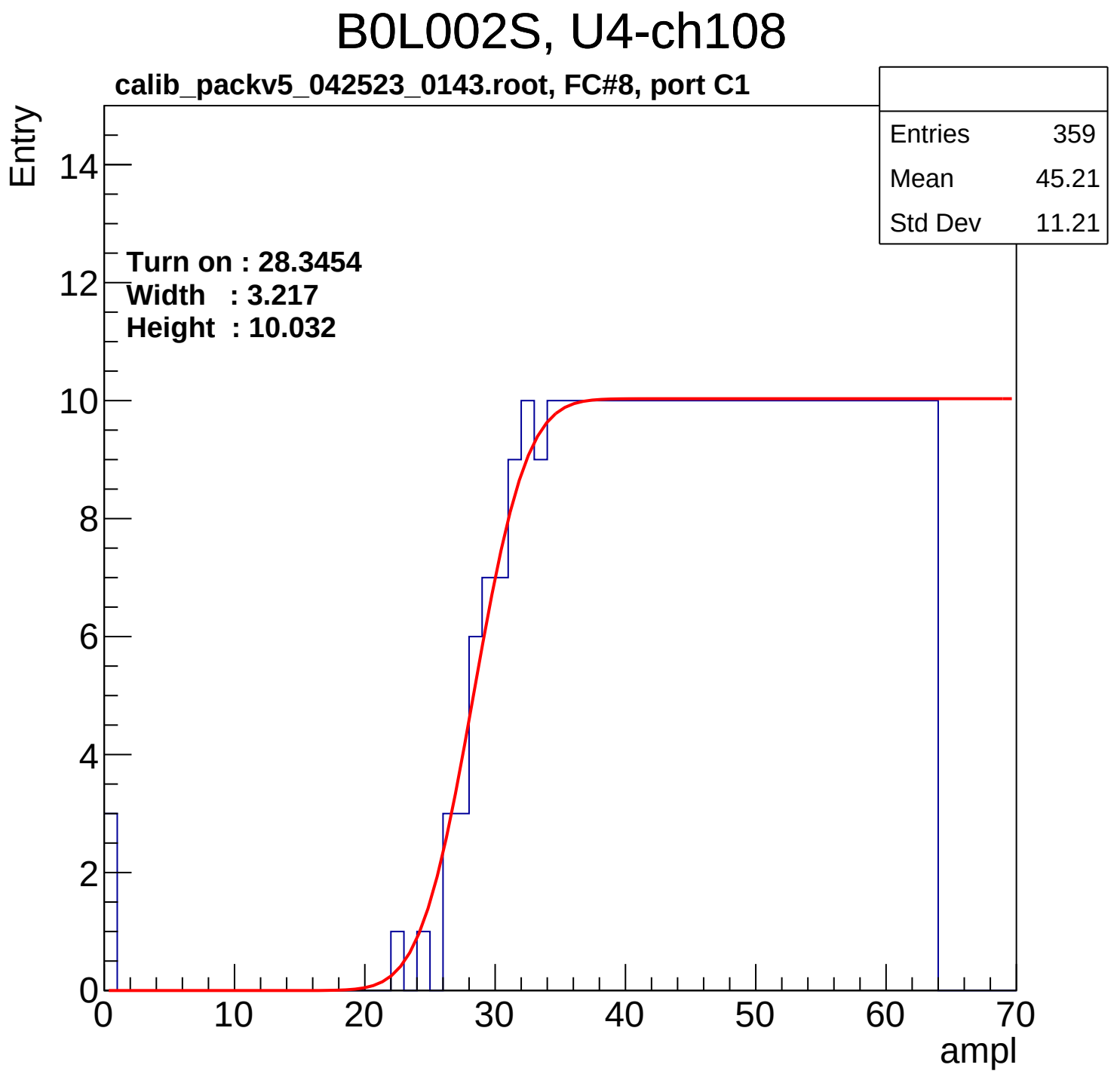

B0L002S, U4-ch103
calib_packv5_042523_0143.root, FC#8, port C1
Entries 372
Mean 44.66
Std Dev 11.31
Turn on : 26.9566
Width : 2.936
Height : 9.998
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

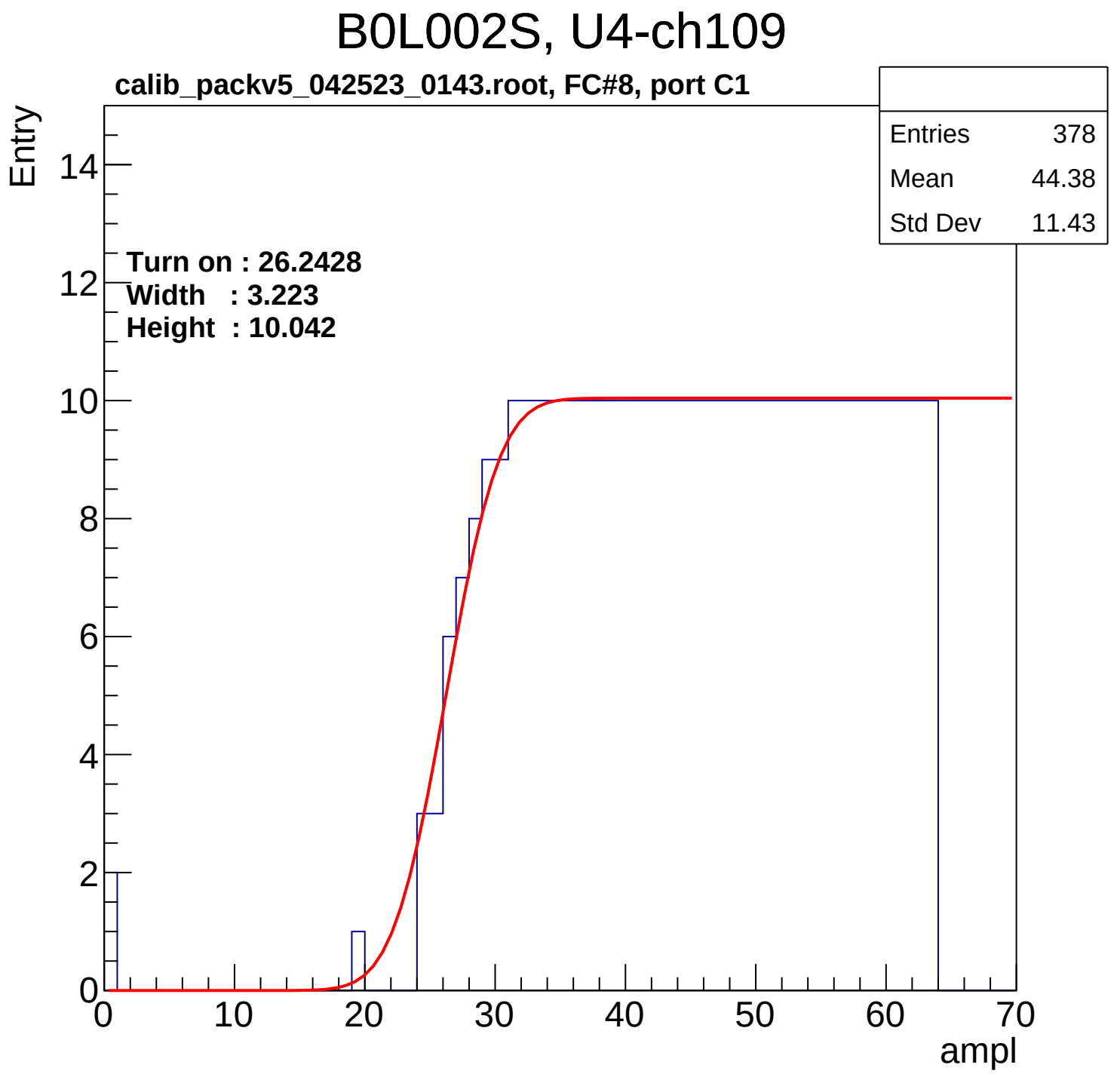

B0L002S, U4-ch104
calib_packv5_042523_0143.root, FC#8, port C1
Entries 384
Mean 44.08
Std Dev 11.59
Turn on : 26.0004
Width : 2.597
Height : 9.993
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

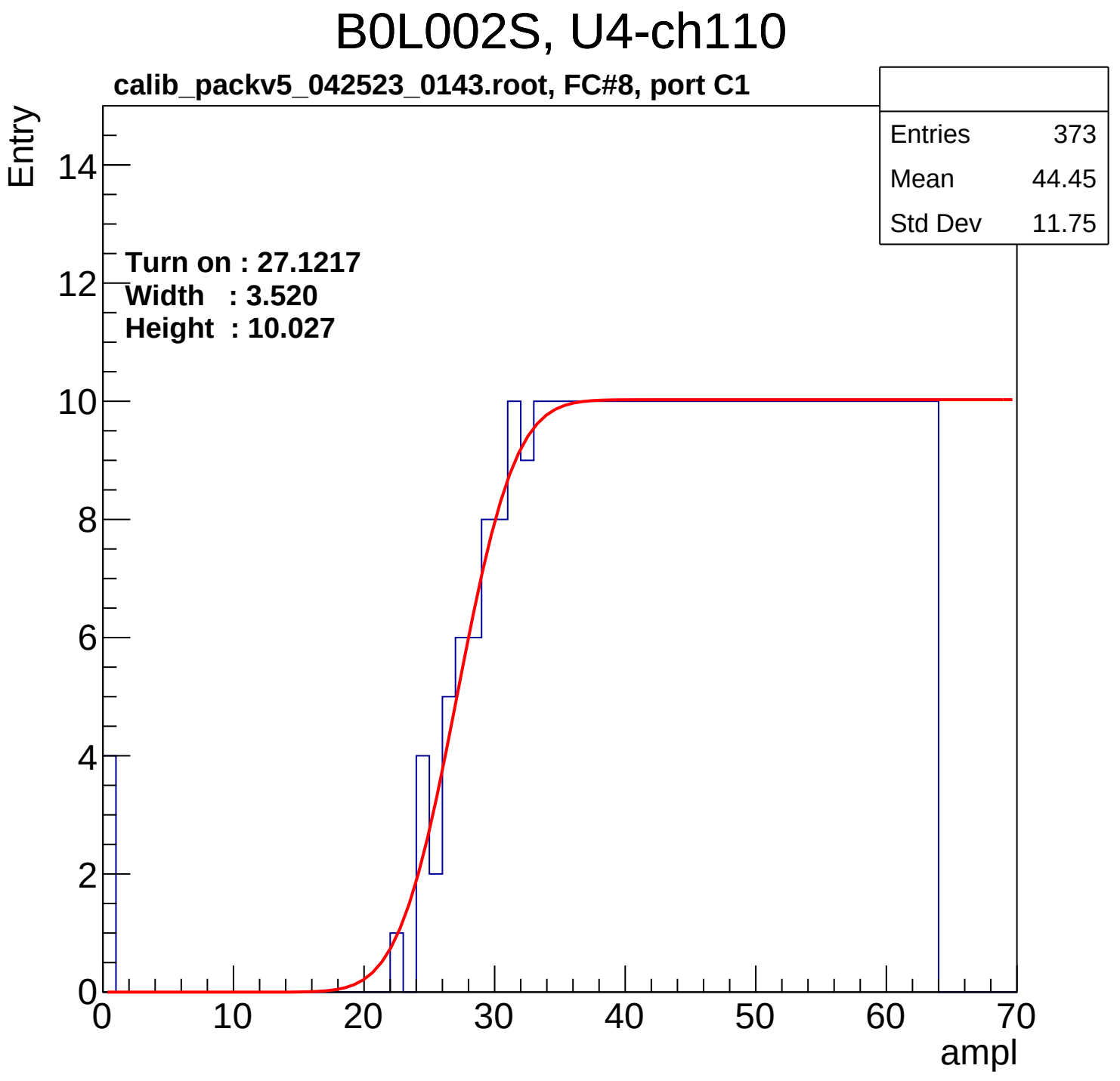

B0L002S, U4-ch105
calib_packv5_042523_0143.root, FC#8, port C1
Entries 376
Mean 44.52
Std Dev 11.25
Turn on : 27.3676
Width : 2.855
Height : 10.073
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

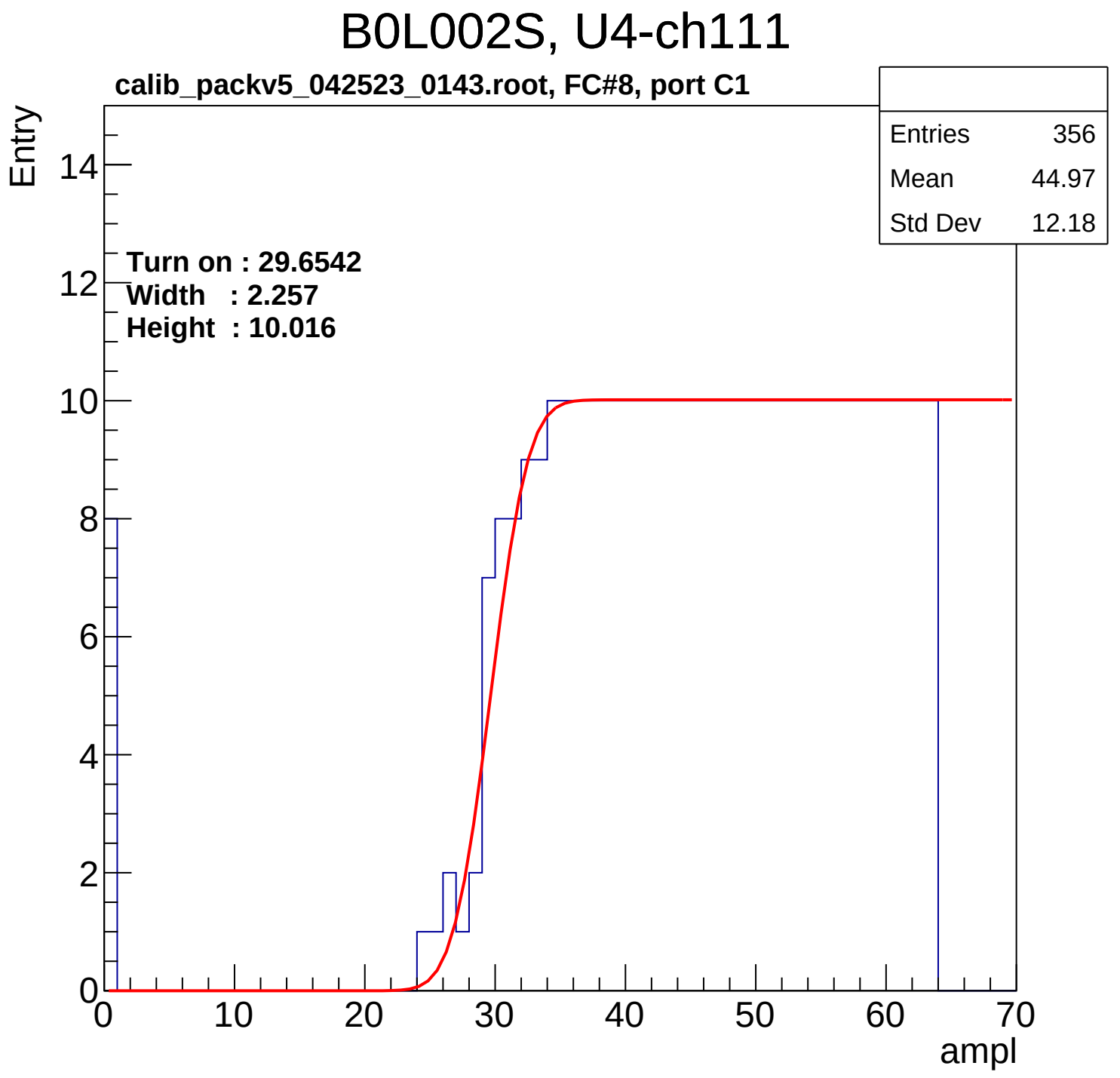

B0L002S, U4-ch106
calib_packv5_042523_0143.root, FC#8, port C1
Entries 380
Mean 44.23
Std Dev 11.57
Turn on : 26.4442
Width : 3.535
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

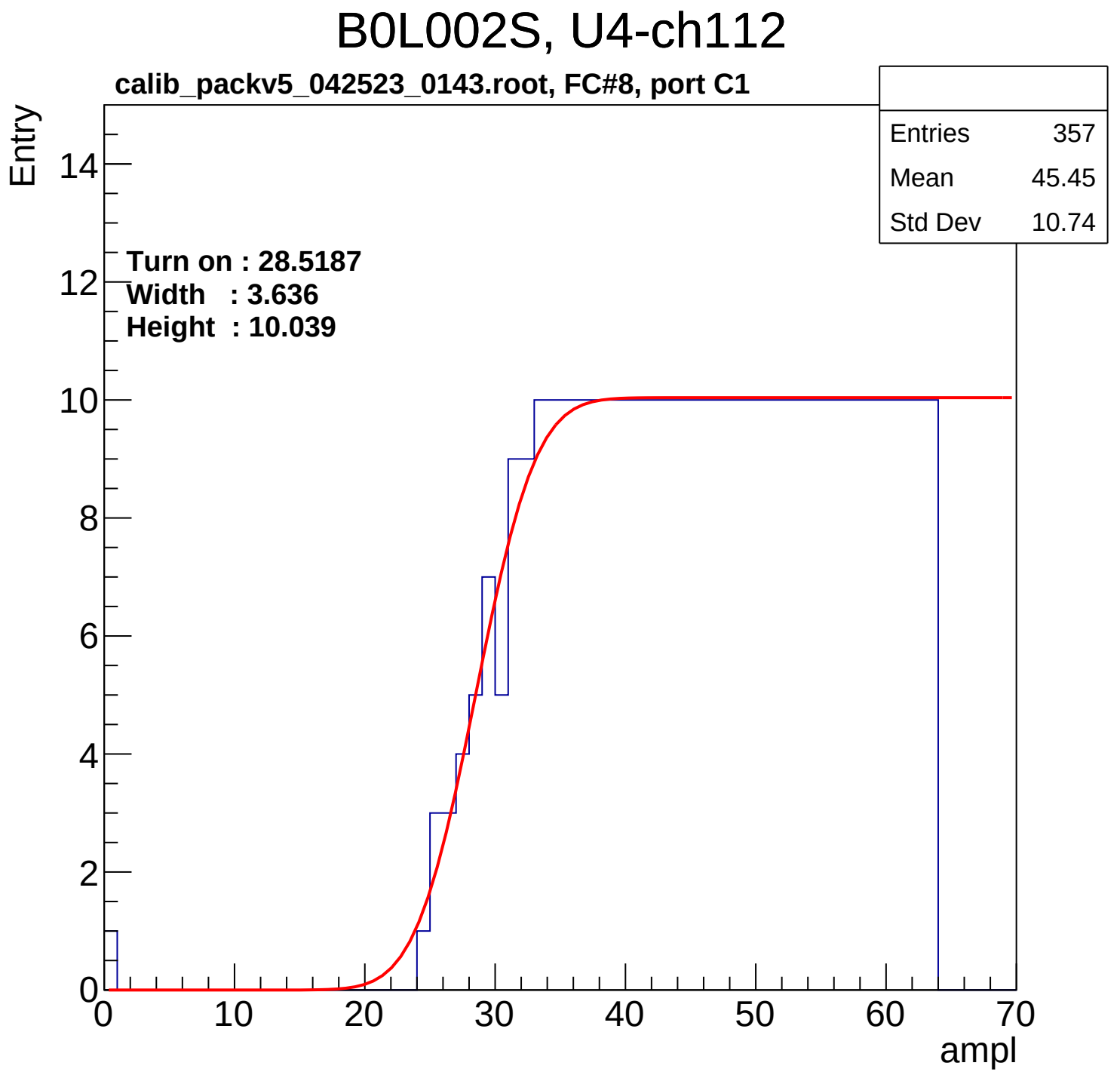

B0L002S, U4-ch107
calib_packv5_042523_0143.root, FC#8, port C1
Entries 362
Mean 45.13
Std Dev 11.09
Turn on : 28.1273
Width : 3.274
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

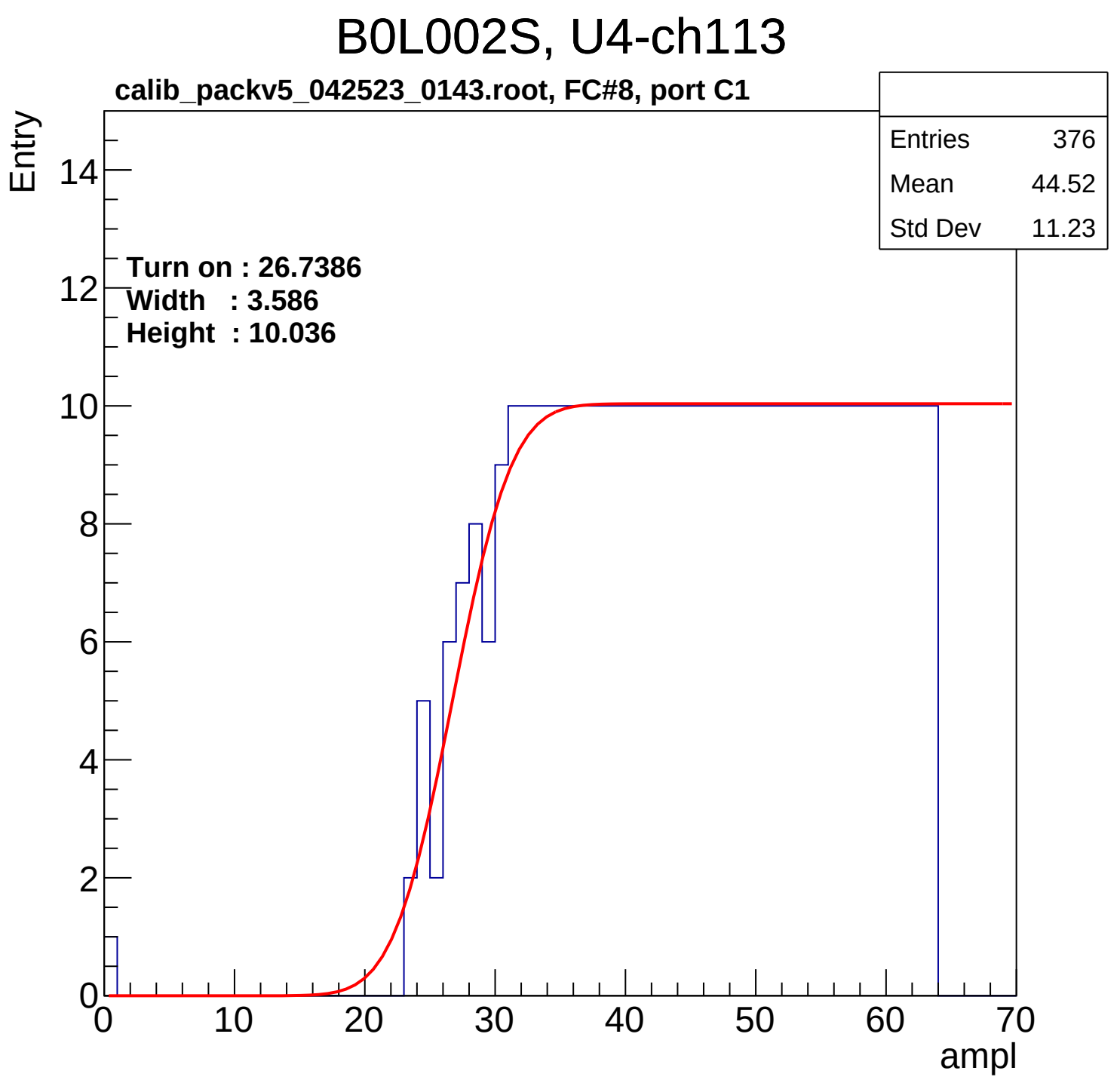

B0L002S, U4-ch108
calib_packv5_042523_0143.root, FC#8, port C1
Entries 359
Mean 45.21
Std Dev 11.21
Turn on : 28.3454
Width : 3.217
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

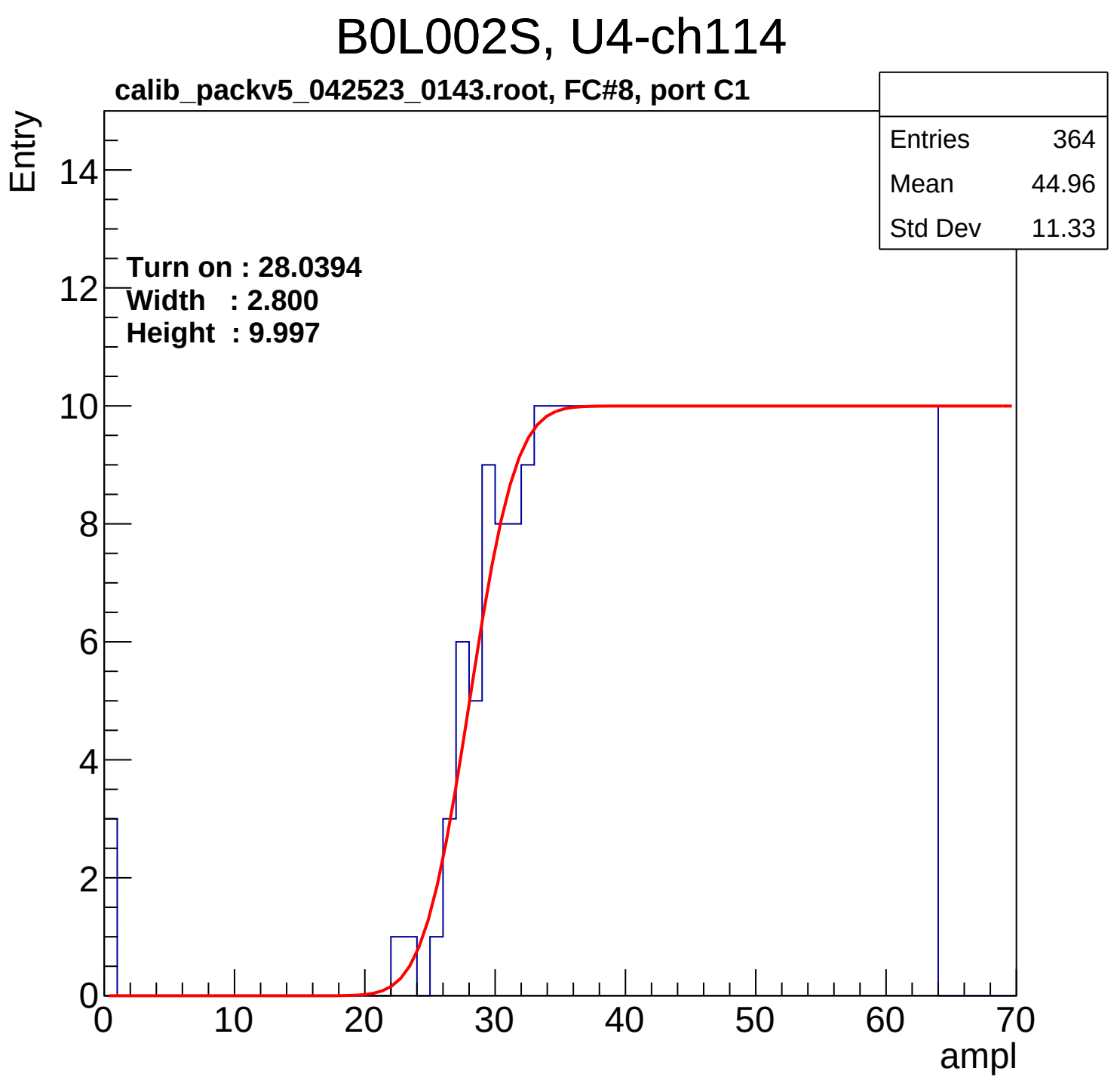

B0L002S, U4-ch109
calib_packv5_042523_0143.root, FC#8, port C1
Entries 378
Mean 44.38
Std Dev 11.43
Turn on : 26.2428
Width : 3.223
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

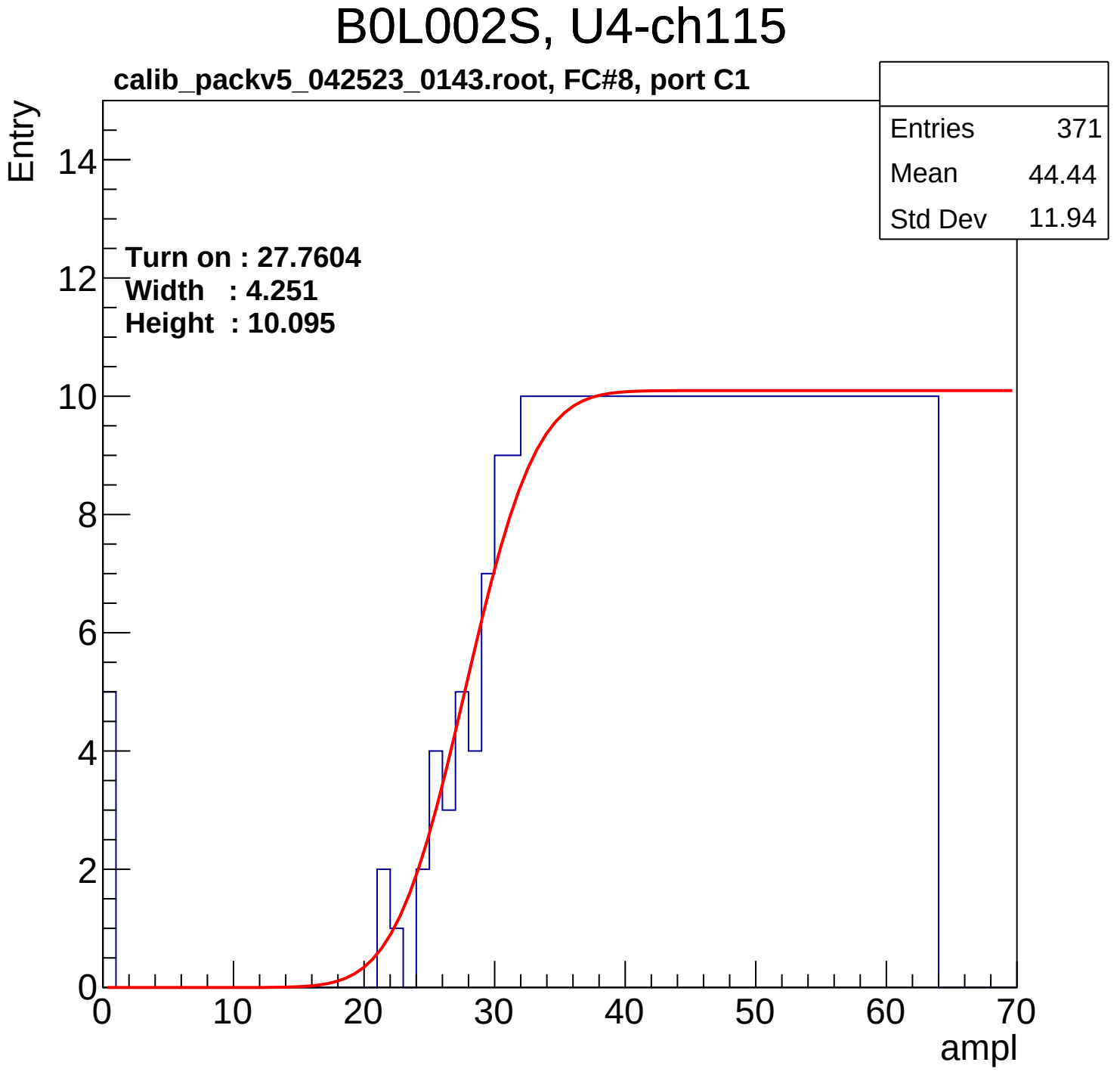

B0L002S, U4-ch110
calib_packv5_042523_0143.root, FC#8, port C1
Entries 373
Mean 44.45
Std Dev 11.75
Turn on : 27.1217
Width : 3.520
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

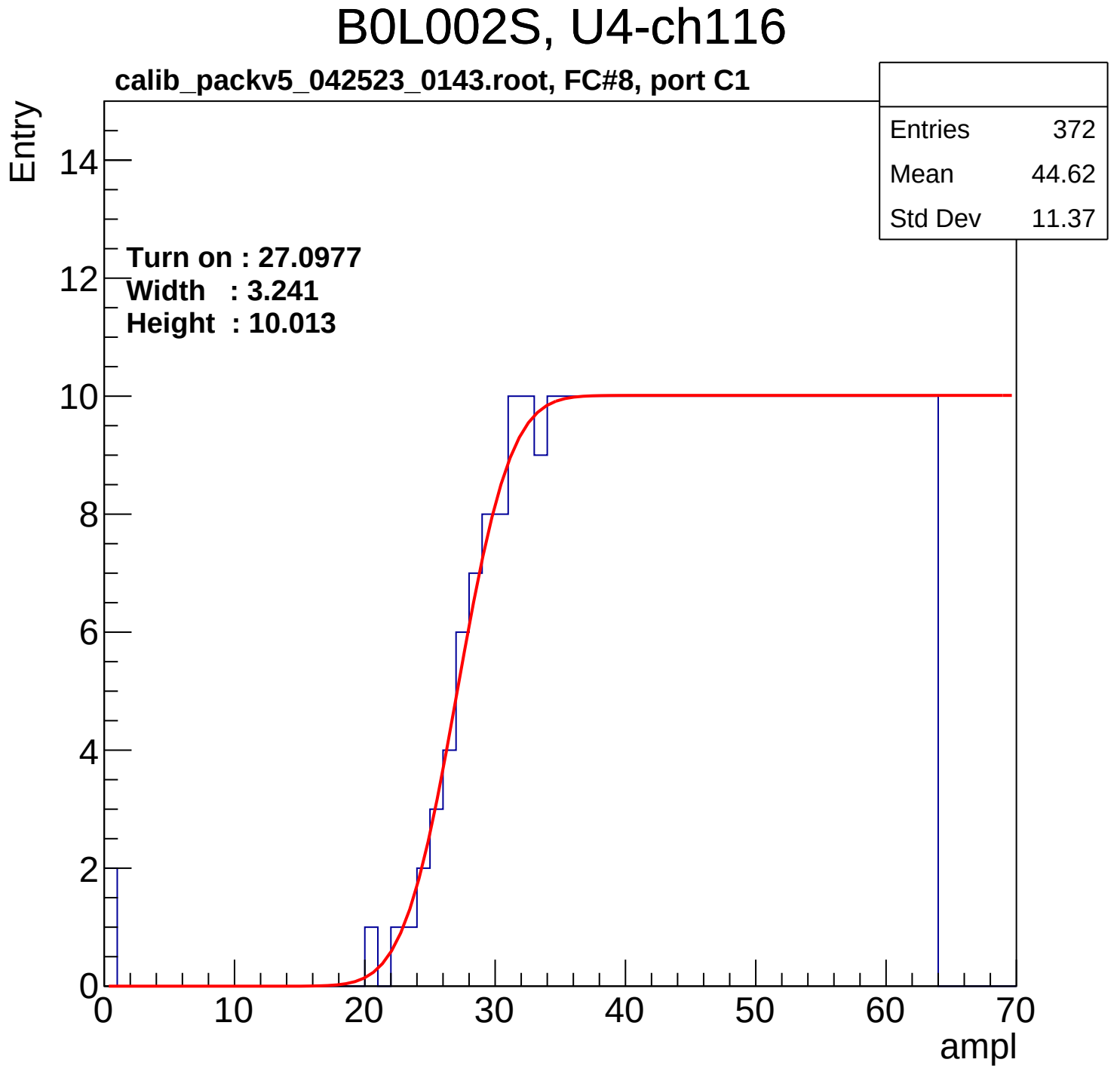

B0L002S, U4-ch111
calib_packv5_042523_0143.root, FC#8, port C1
Entries 356
Mean 44.97
Std Dev 12.18
Turn on : 29.6542
Width : 2.257
Height : 10.016
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

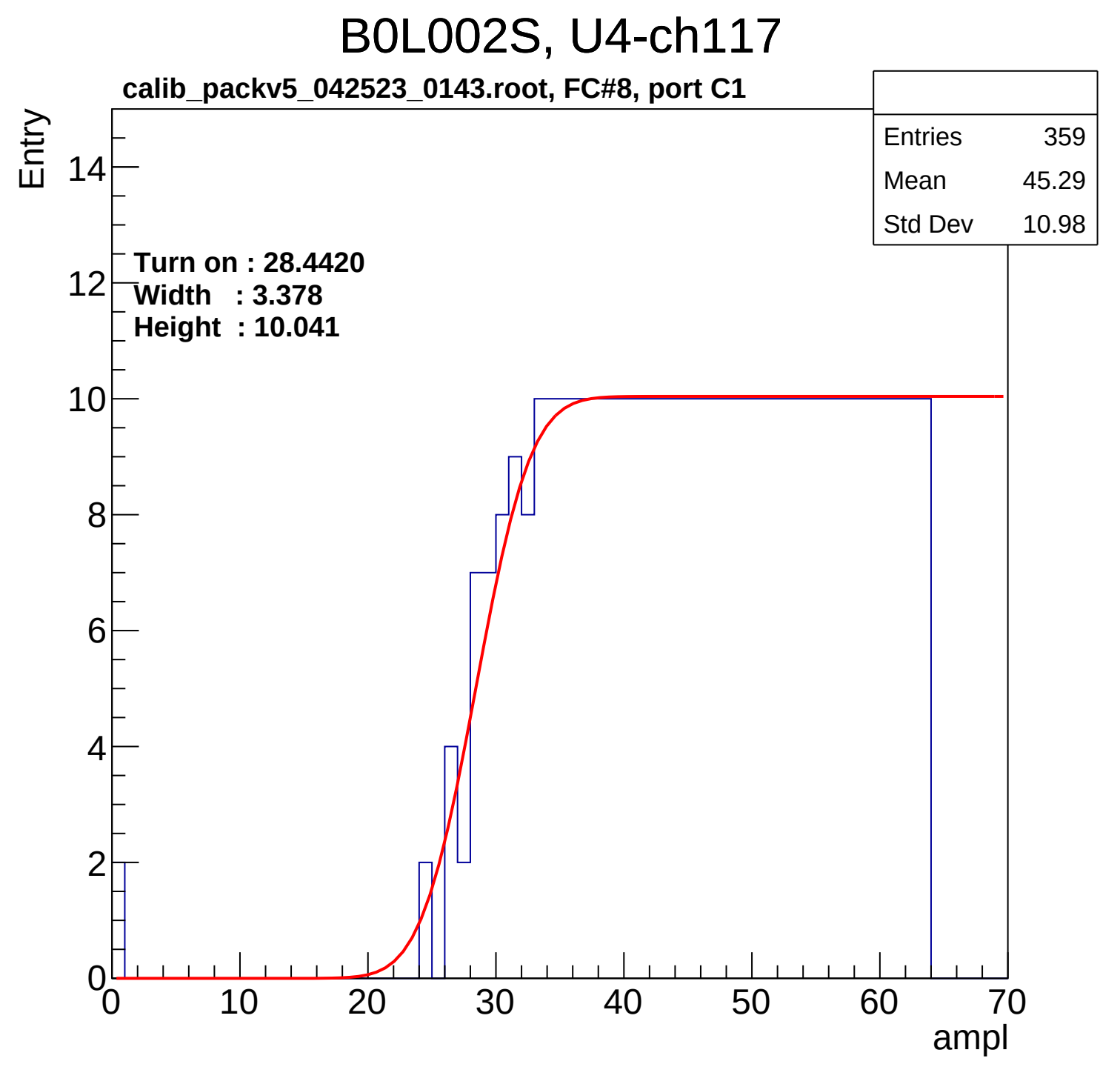

B0L002S, U4-ch112
calib_packv5_042523_0143.root, FC#8, port C1
Entries 357
Mean 45.45
Std Dev 10.74
Turn on : 28.5187
Width : 3.636
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

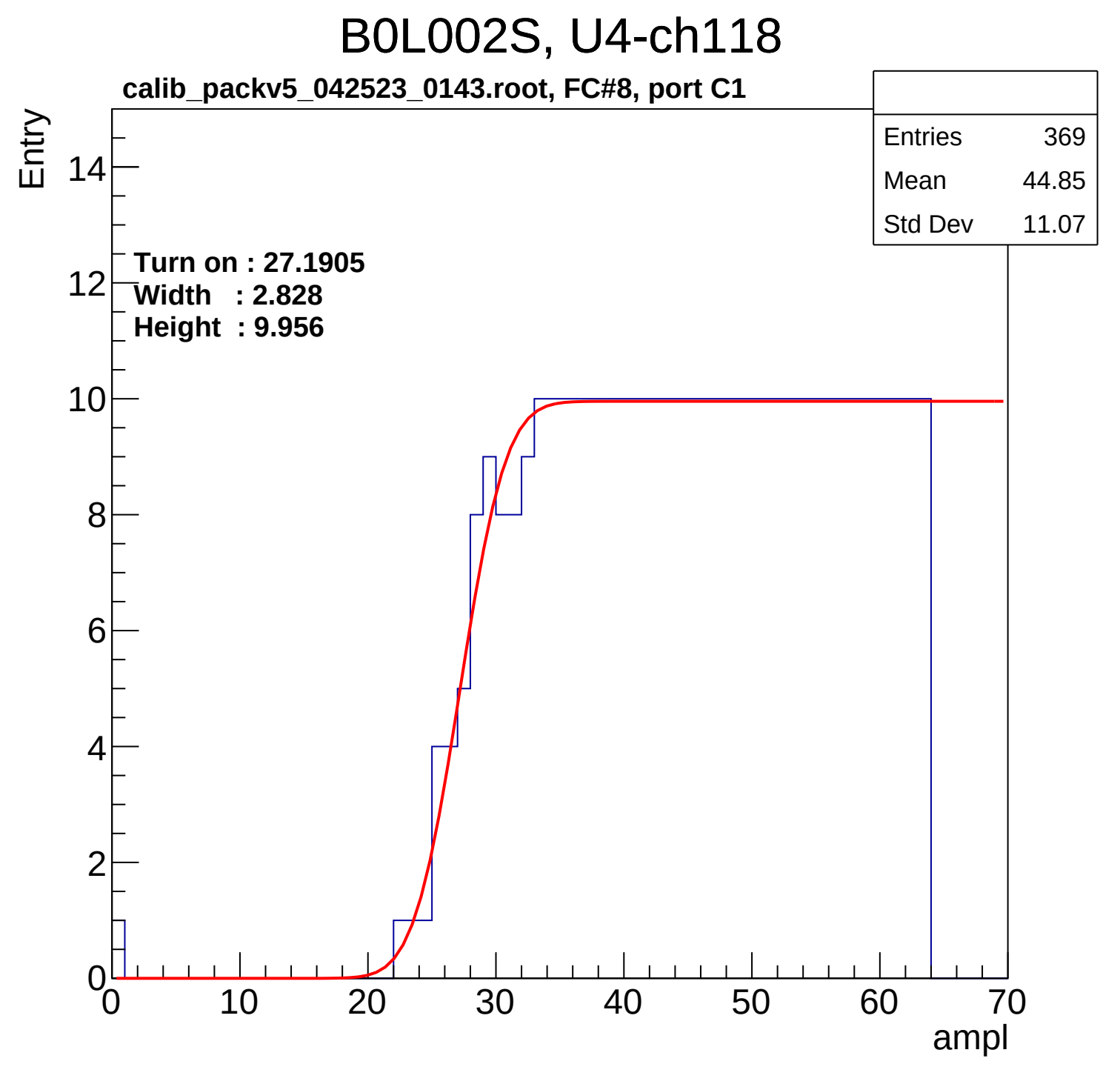

B0L002S, U4-ch113
calib_packv5_042523_0143.root, FC#8, port C1
Entries 376
Mean 44.52
Std Dev 11.23
Turn on : 26.7386
Width : 3.586
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

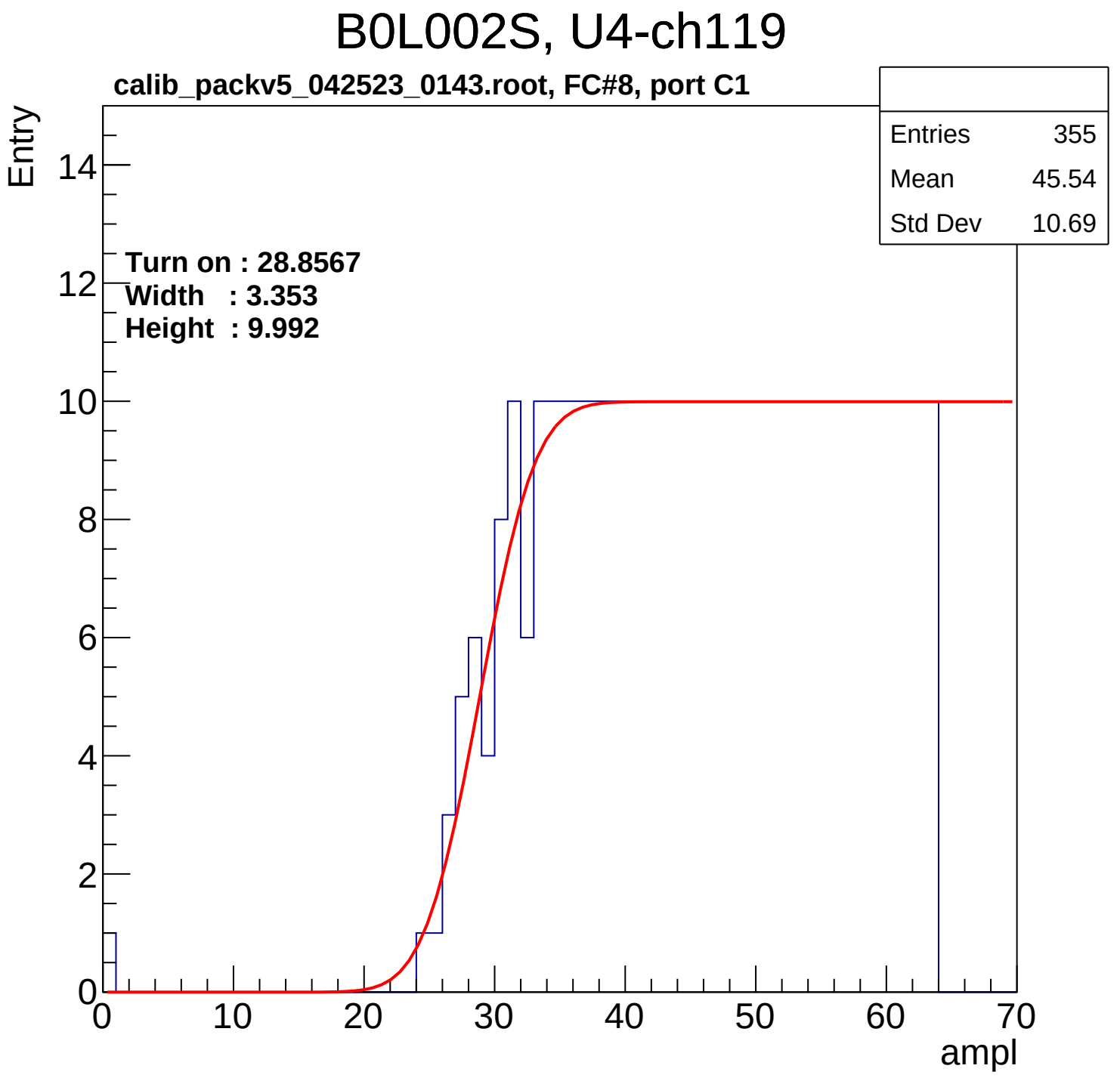

B0L002S, U4-ch114
calib_packv5_042523_0143.root, FC#8, port C1
Entries 364
Mean 44.96
Std Dev 11.33
Turn on : 28.0394
Width : 2.800
Height : 9.997
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

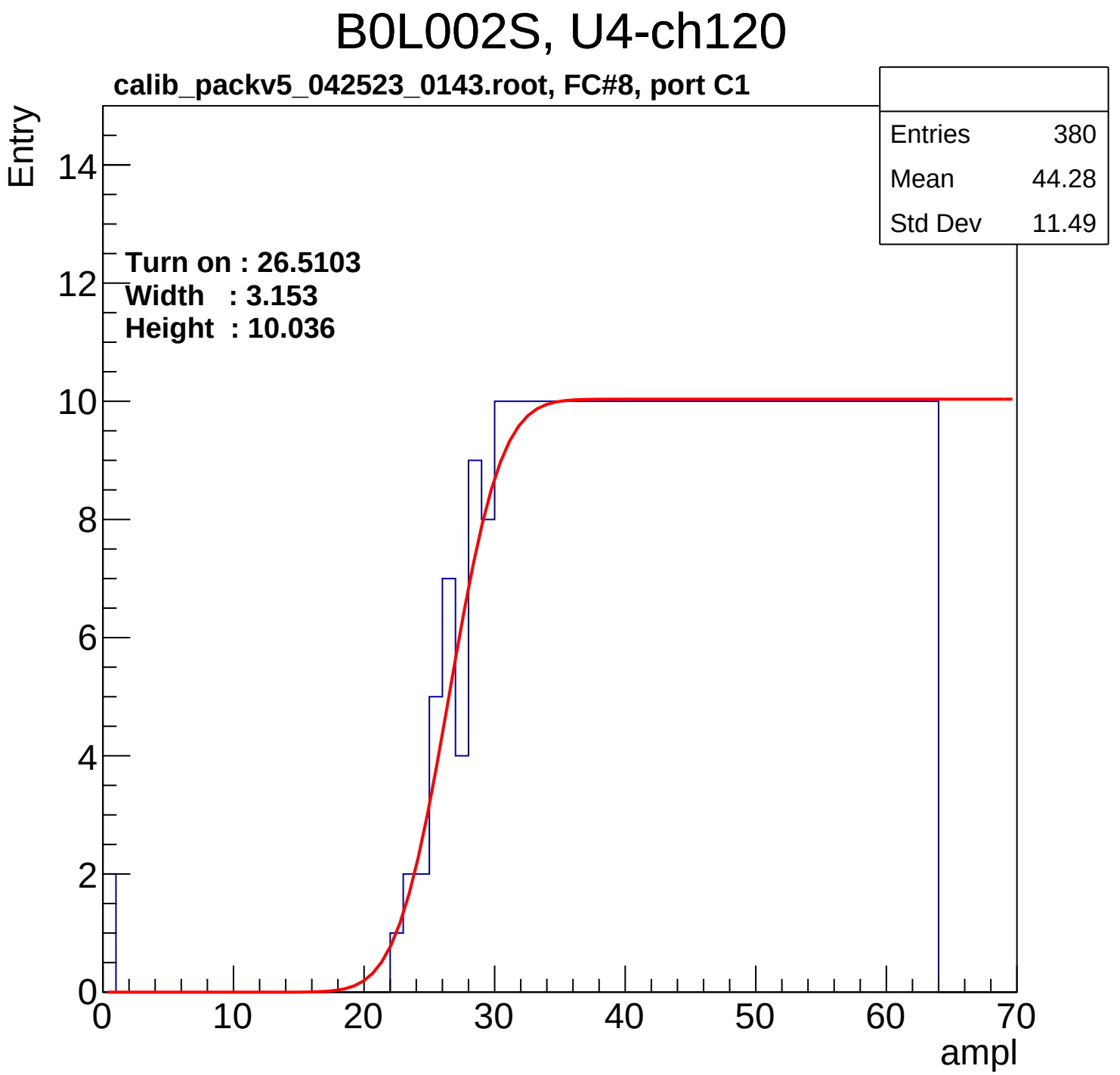

B0L002S, U4-ch115
calib_packv5_042523_0143.root, FC#8, port C1
Entries 371
Mean 44.44
Std Dev 11.94
Turn on : 27.7604
Width : 4.251
Height : 10.095
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

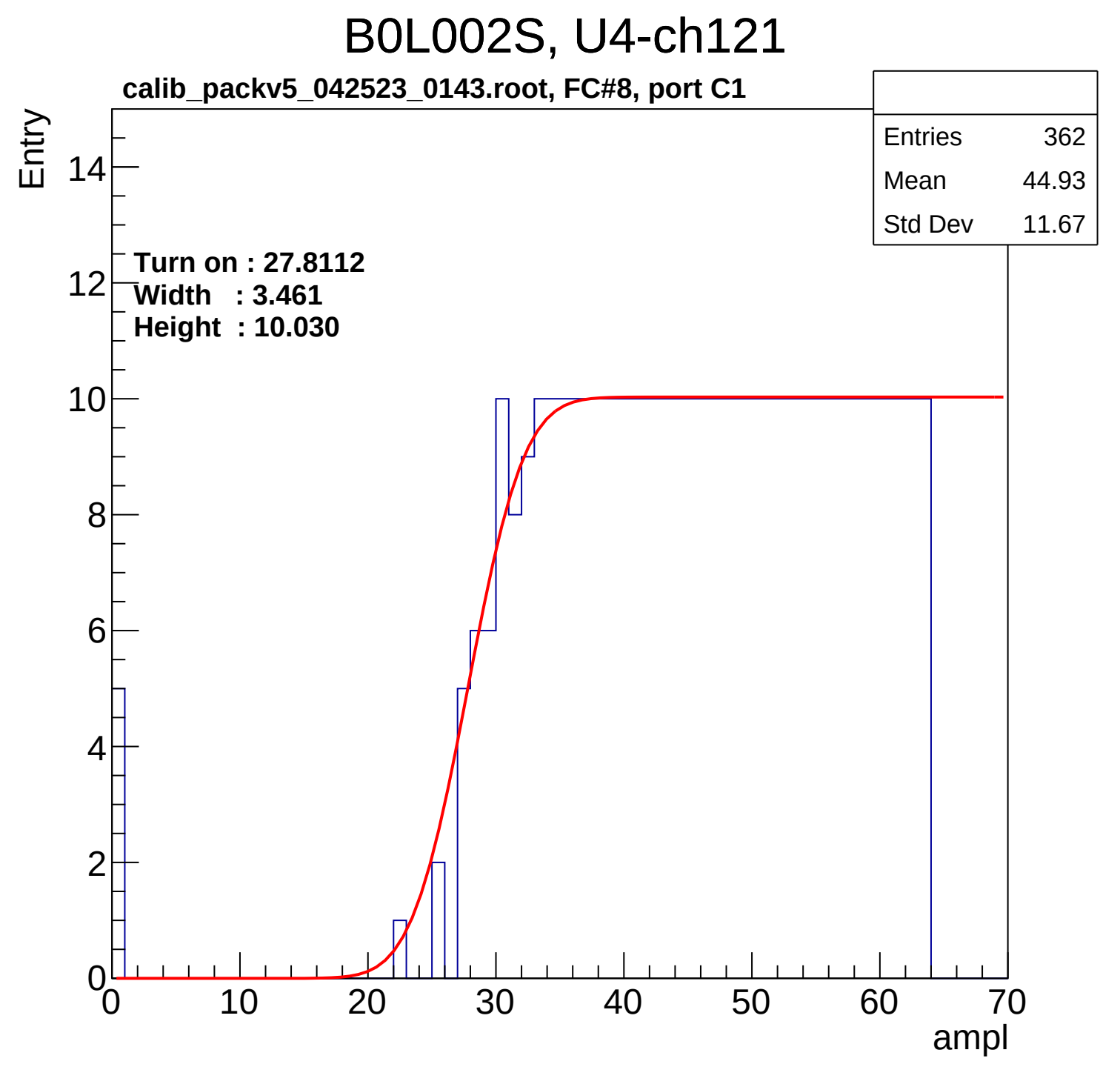

B0L002S, U4-ch116
calib_packv5_042523_0143.root, FC#8, port C1
Entries 372
Mean 44.62
Std Dev 11.37
Turn on : 27.0977
Width : 3.241
Height : 10.013
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

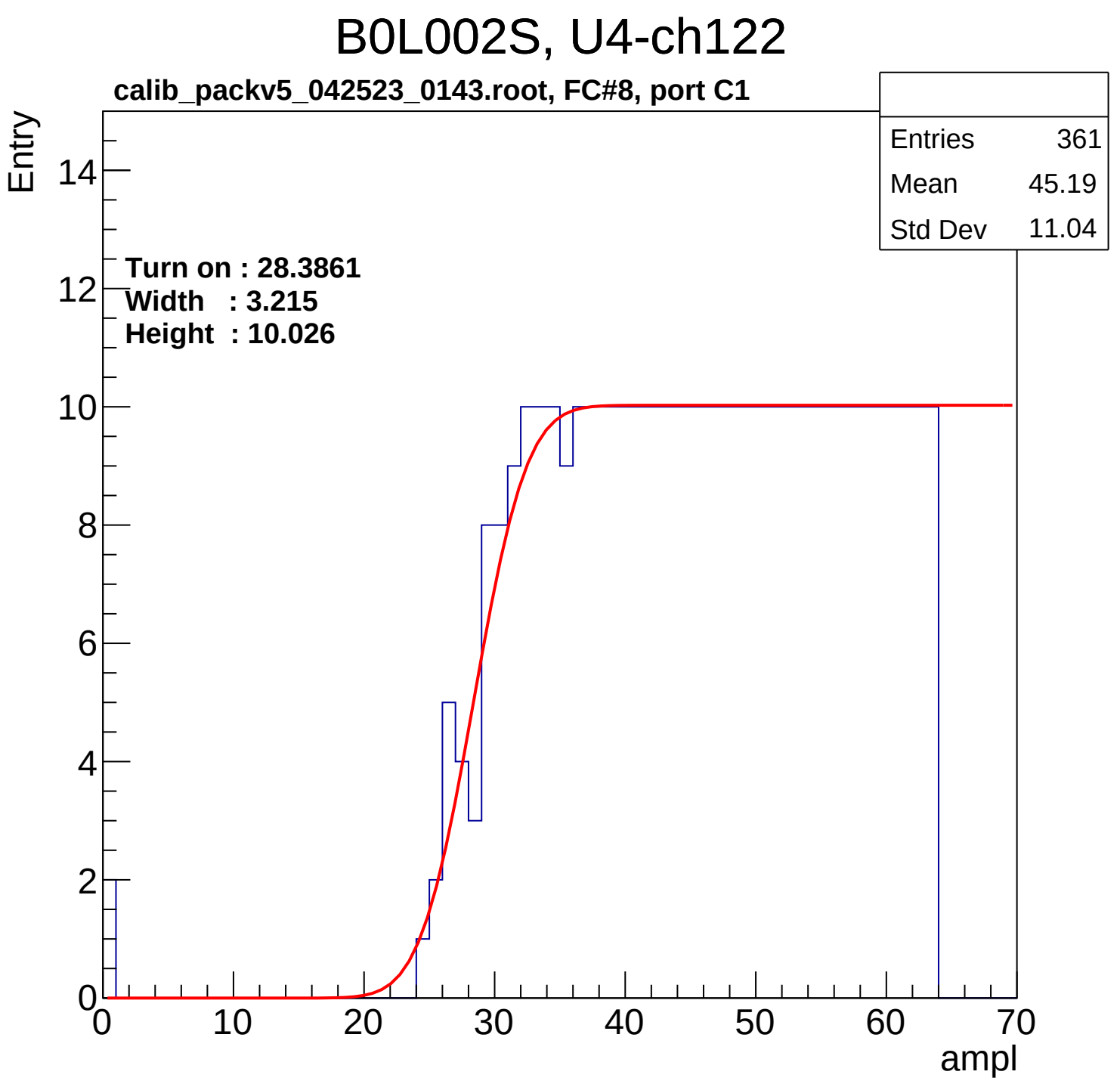

B0L002S, U4-ch117
calib_packv5_042523_0143.root, FC#8, port C1
Entries 359
Mean 45.29
Std Dev 10.98
Turn on : 28.4420
Width : 3.378
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

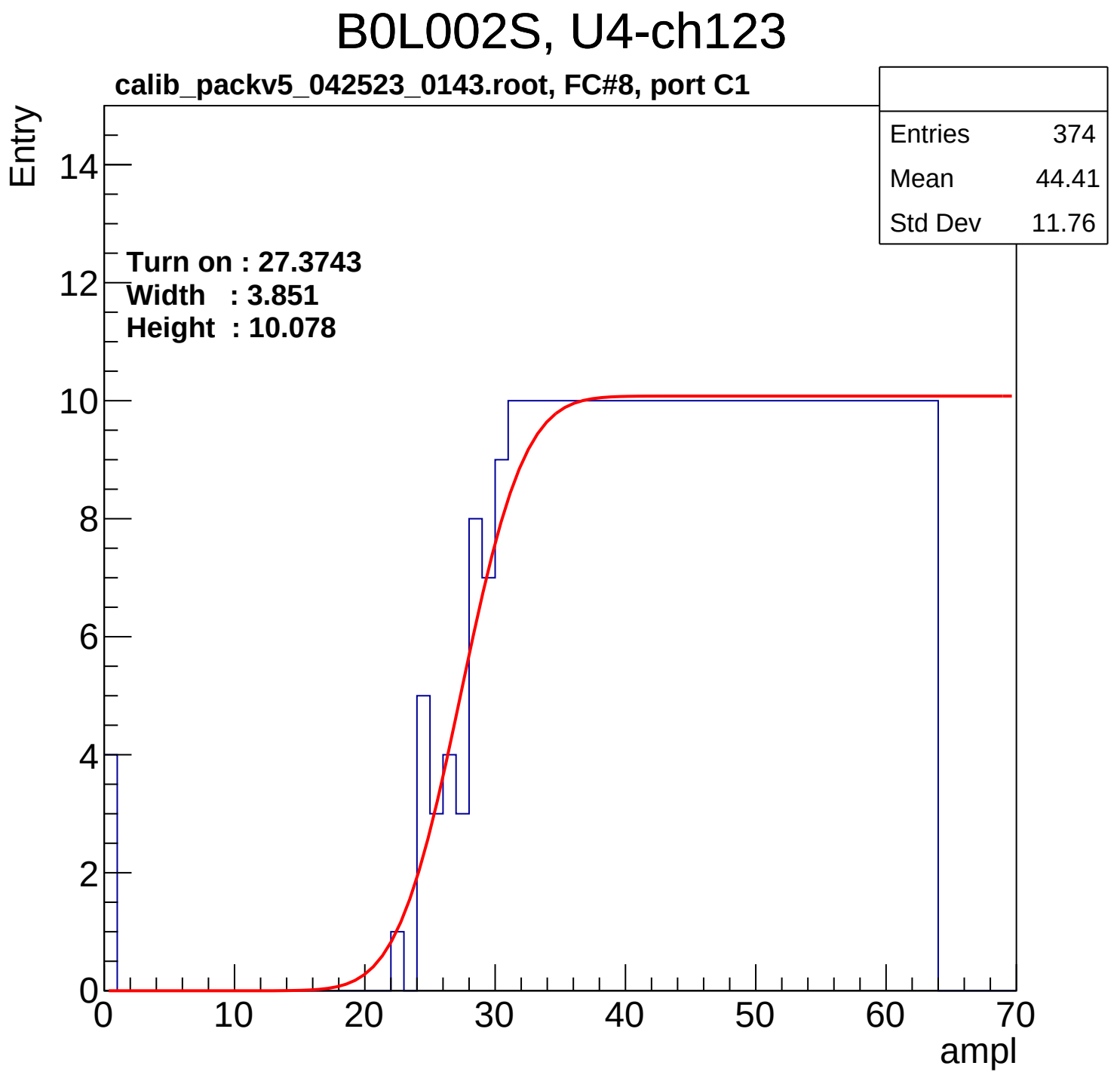

B0L002S, U4-ch118
calib_packv5_042523_0143.root, FC#8, port C1
Entries 369
Mean 44.85
Std Dev 11.07
Turn on : 27.1905
Width : 2.828
Height : 9.956
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

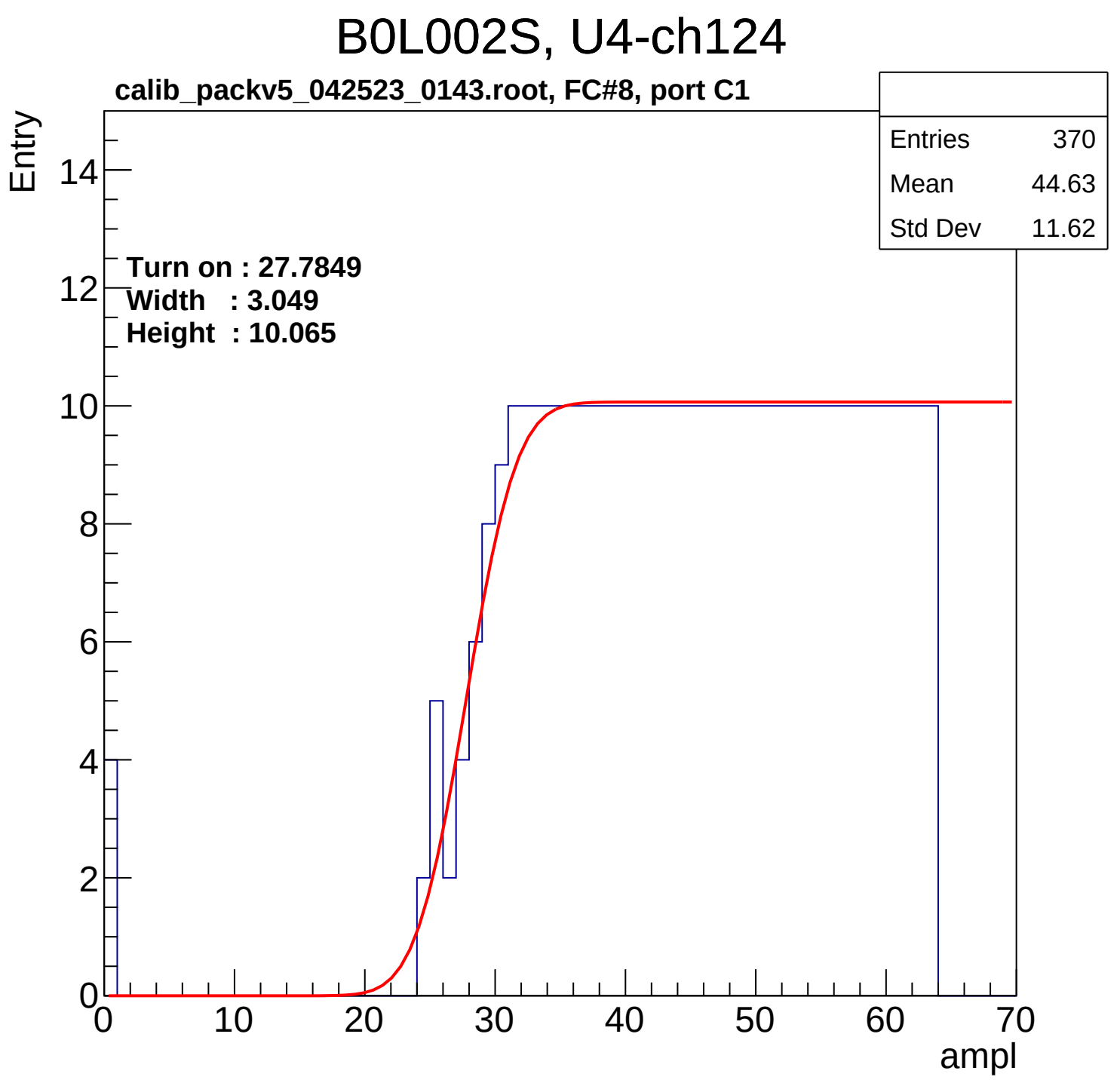

B0L002S, U4-ch119
calib_packv5_042523_0143.root, FC#8, port C1
Entries 355
Mean 45.54
Std Dev 10.69
Turn on : 28.8567
Width : 3.353
Height : 9.992
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

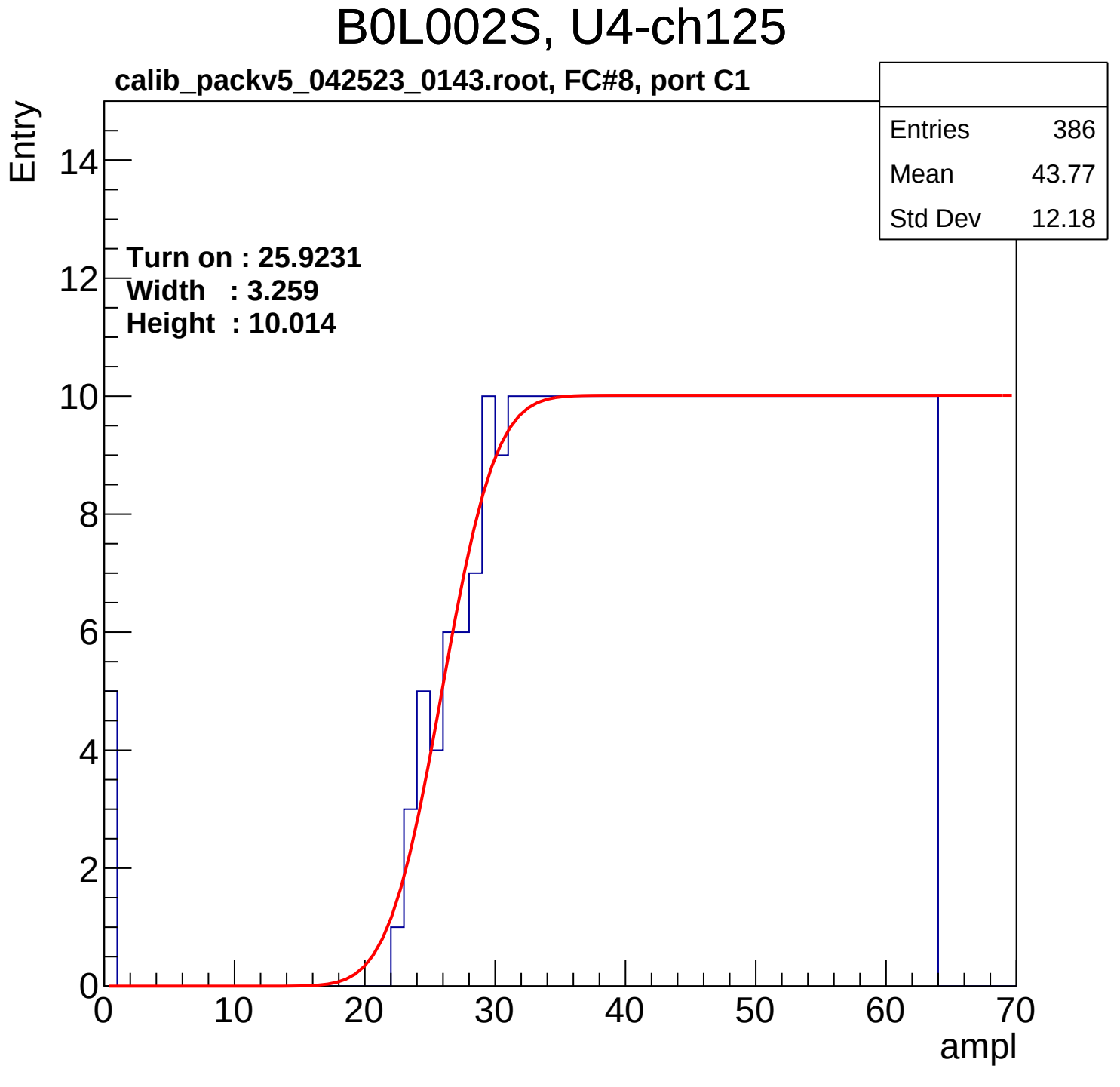

B0L002S, U4-ch120
calib_packv5_042523_0143.root, FC#8, port C1
Entries 380
Mean 44.28
Std Dev 11.49
Turn on : 26.5103
Width : 3.153
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

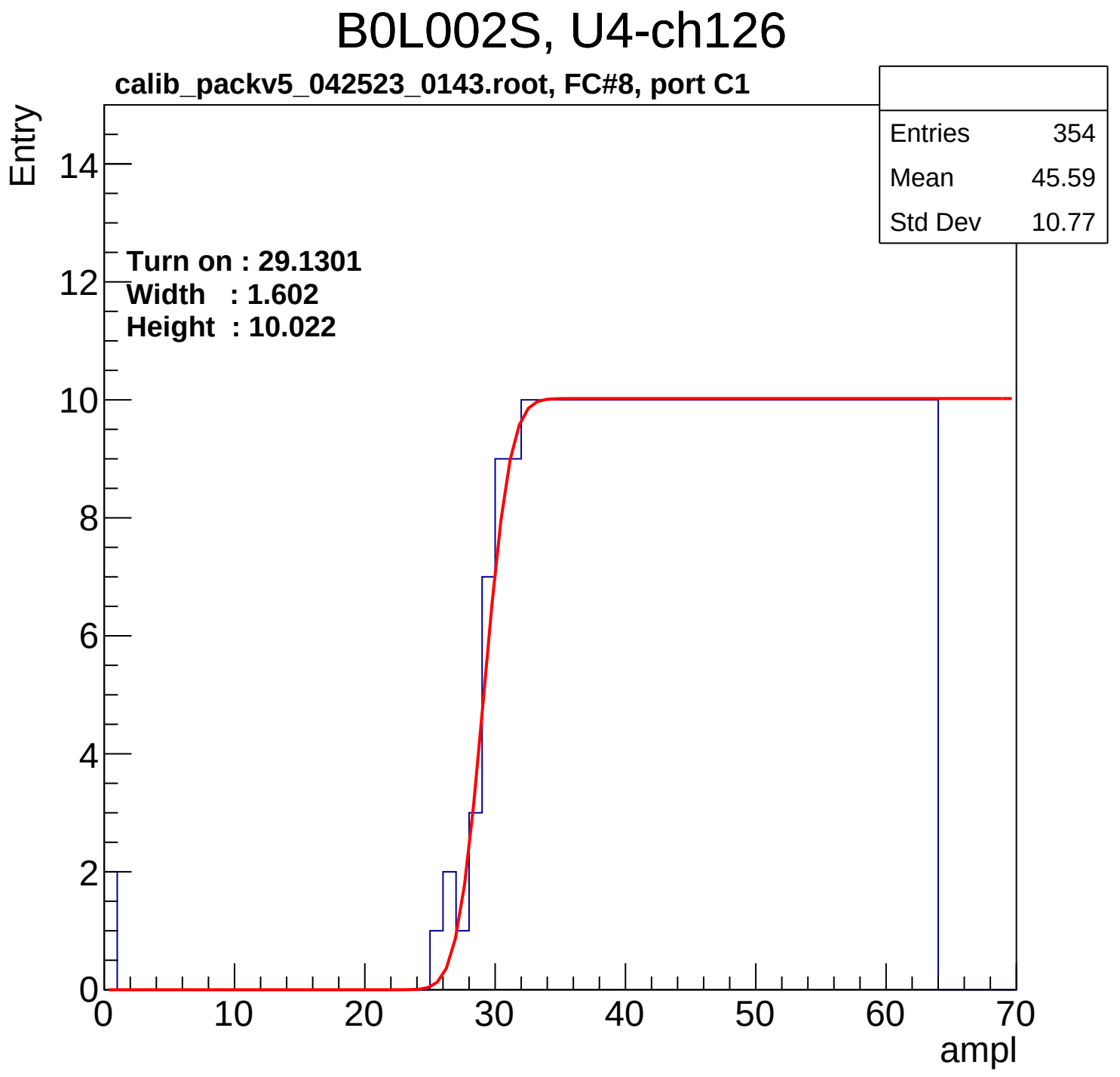

B0L002S, U4-ch121
calib_packv5_042523_0143.root, FC#8, port C1
Entries 362
Mean 44.93
Std Dev 11.67
Turn on : 27.8112
Width : 3.461
Height : 10.030
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

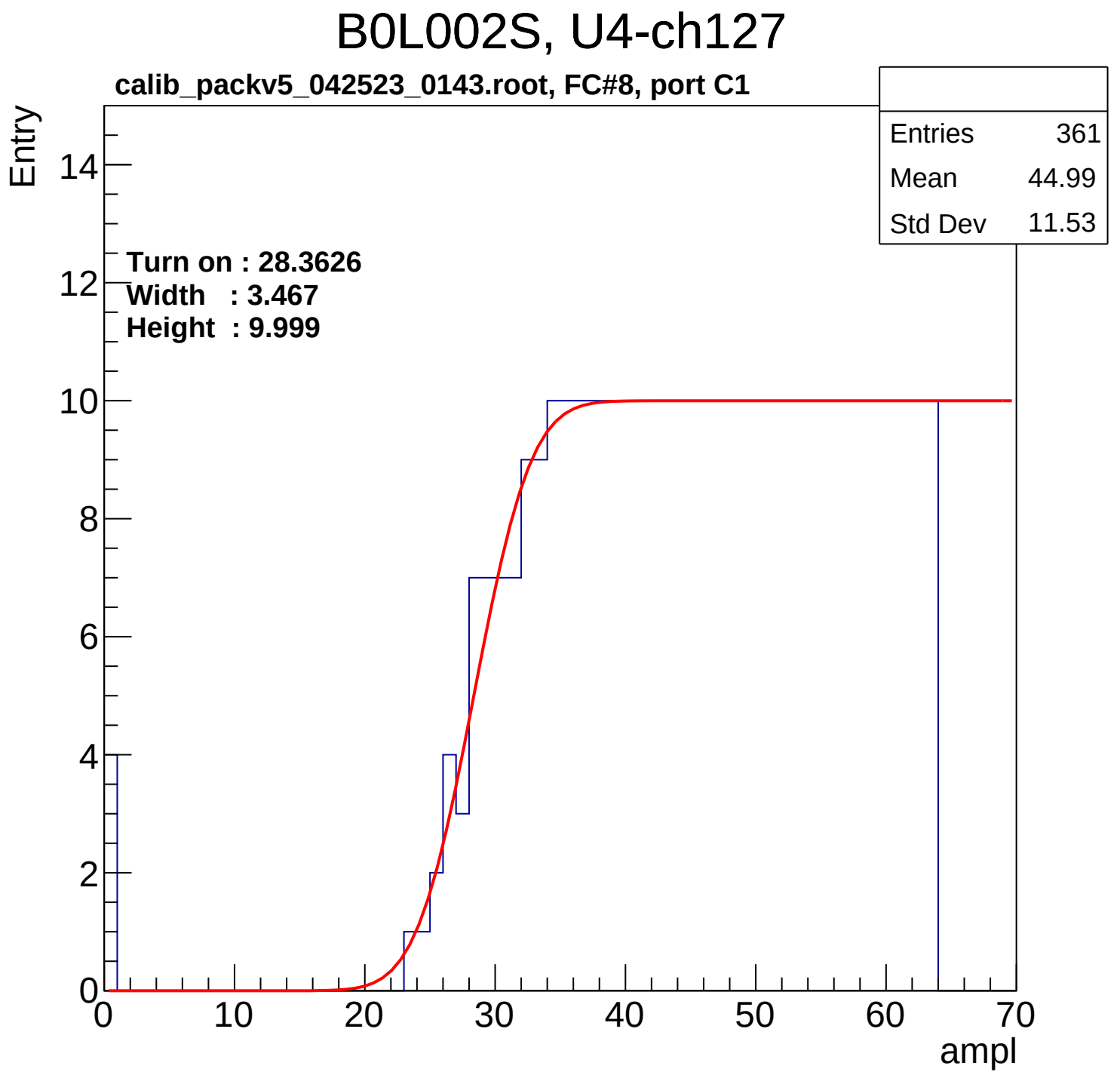

B0L002S, U4-ch122
calib_packv5_042523_0143.root, FC#8, port C1
Entries 361
Mean 45.19
Std Dev 11.04
Turn on : 28.3861
Width : 3.215
Height : 10.026
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

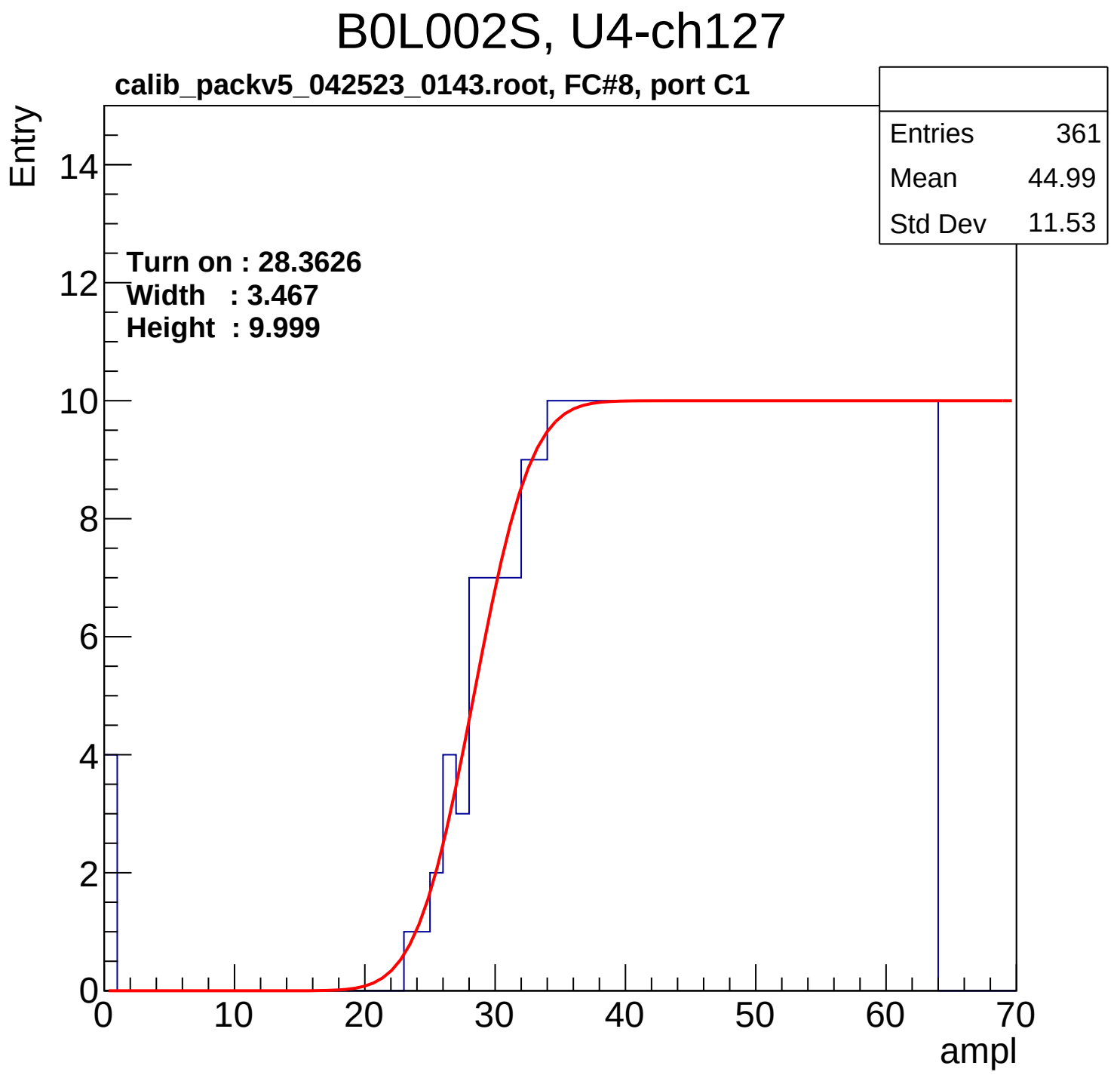

B0L002S, U4-ch123
calib_packv5_042523_0143.root, FC#8, port C1
Entries 374
Mean 44.41
Std Dev 11.76
Turn on : 27.3743
Width : 3.851
Height : 10.078
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L002S, U4-ch124
calib_packv5_042523_0143.root, FC#8, port C1
Entries 370
Mean 44.63
Std Dev 11.62
Turn on : 27.7849
Width : 3.049
Height : 10.065
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L002S, U4-ch125
calib_packv5_042523_0143.root, FC#8, port C1
Entries 386
Mean 43.77
Std Dev 12.18
Turn on : 25.9231
Width : 3.259
Height : 10.014
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L002S, U4-ch126
calib_packv5_042523_0143.root, FC#8, port C1
Entries 354
Mean 45.59
Std Dev 10.77
Turn on : 29.1301
Width : 1.602
Height : 10.022
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L002S, U4-ch127
calib_packv5_042523_0143.root, FC#8, port C1
Entries 361
Mean 44.99
Std Dev 11.53
Turn on : 28.3626
Width : 3.467
Height : 9.999
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L002S, U4-ch127
calib_packv5_042523_0143.root, FC#8, port C1
Entries 361
Mean 44.99
Std Dev 11.53
Turn on : 28.3626
Width : 3.467
Height : 9.999
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70