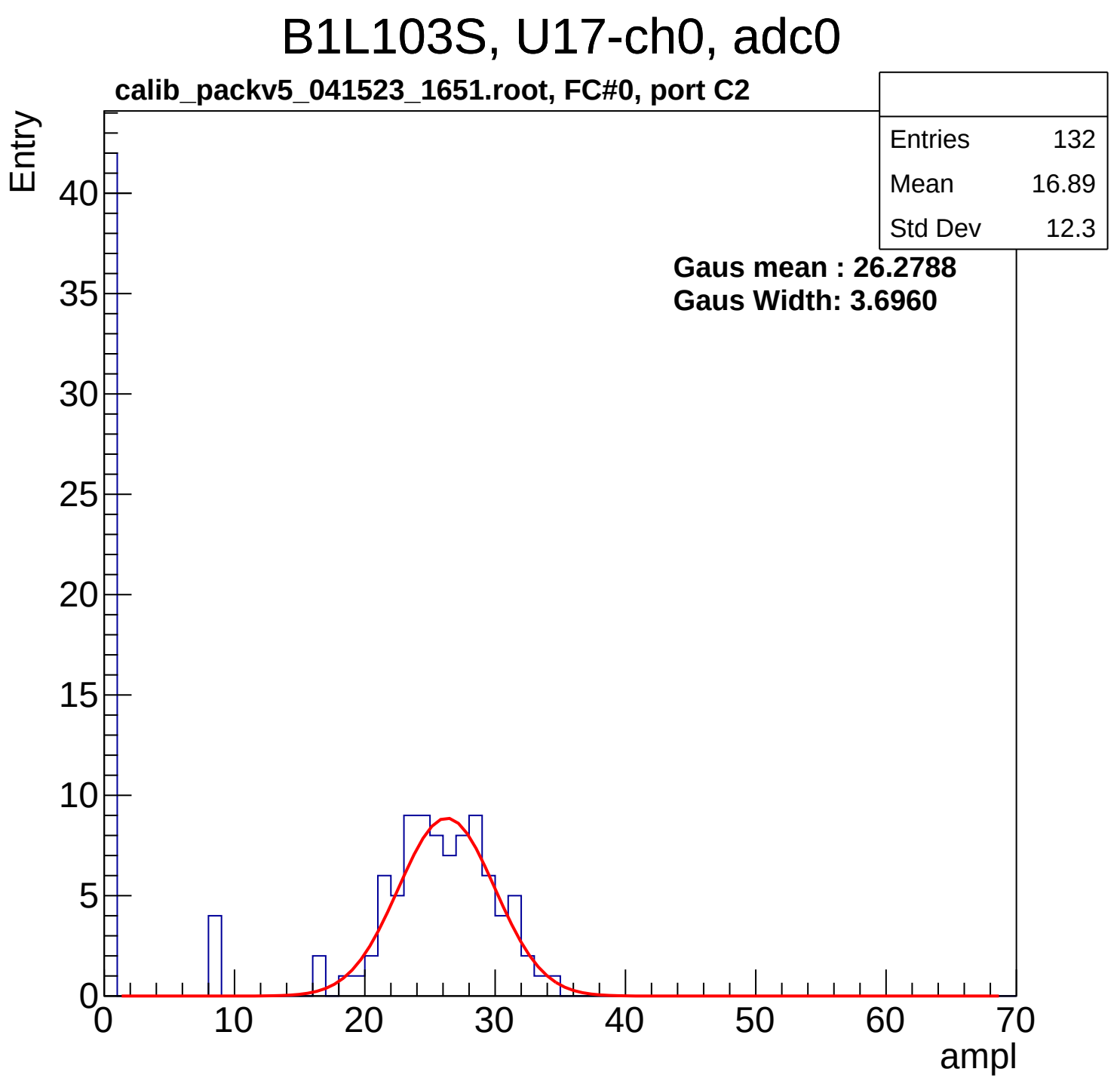
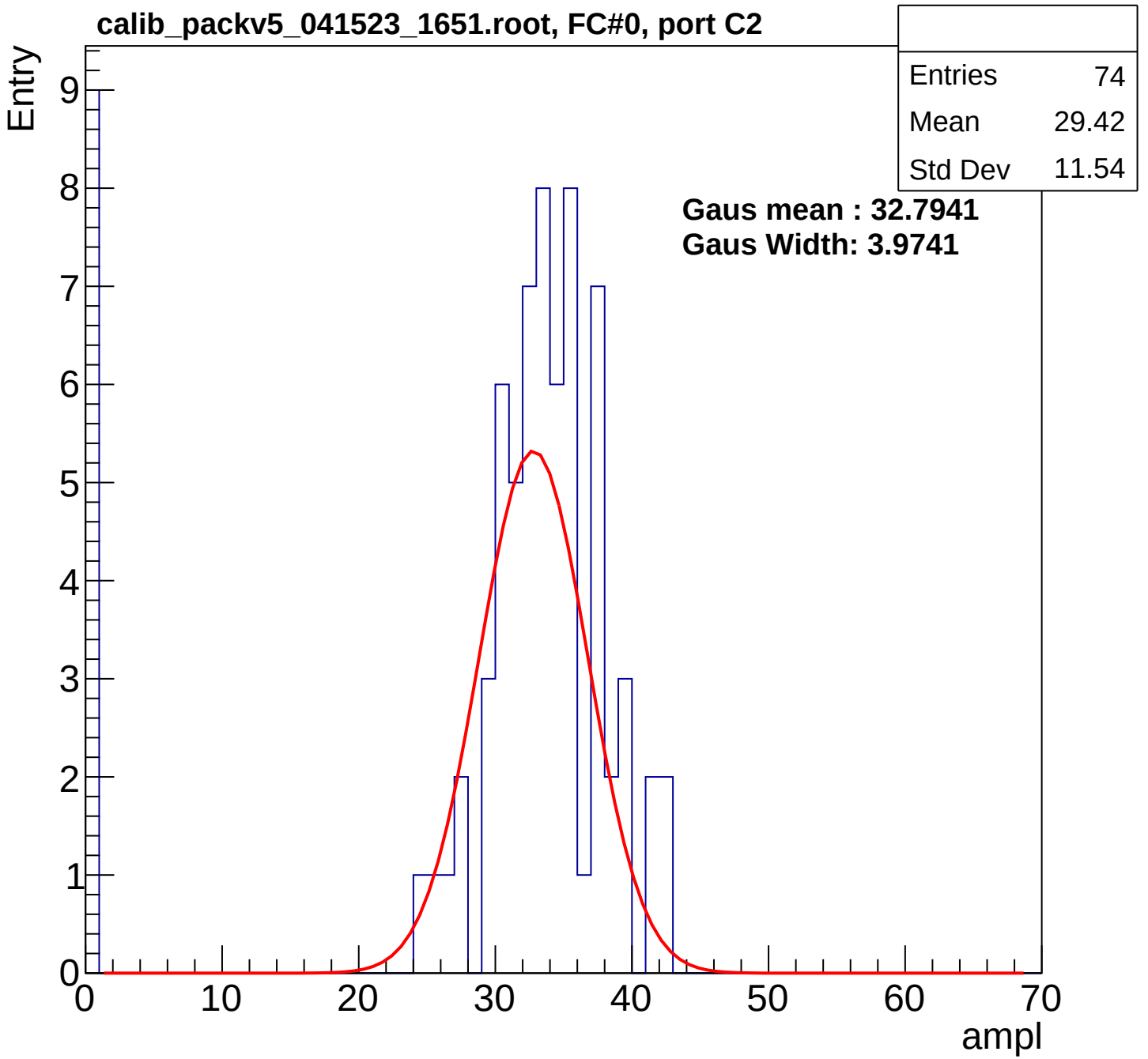
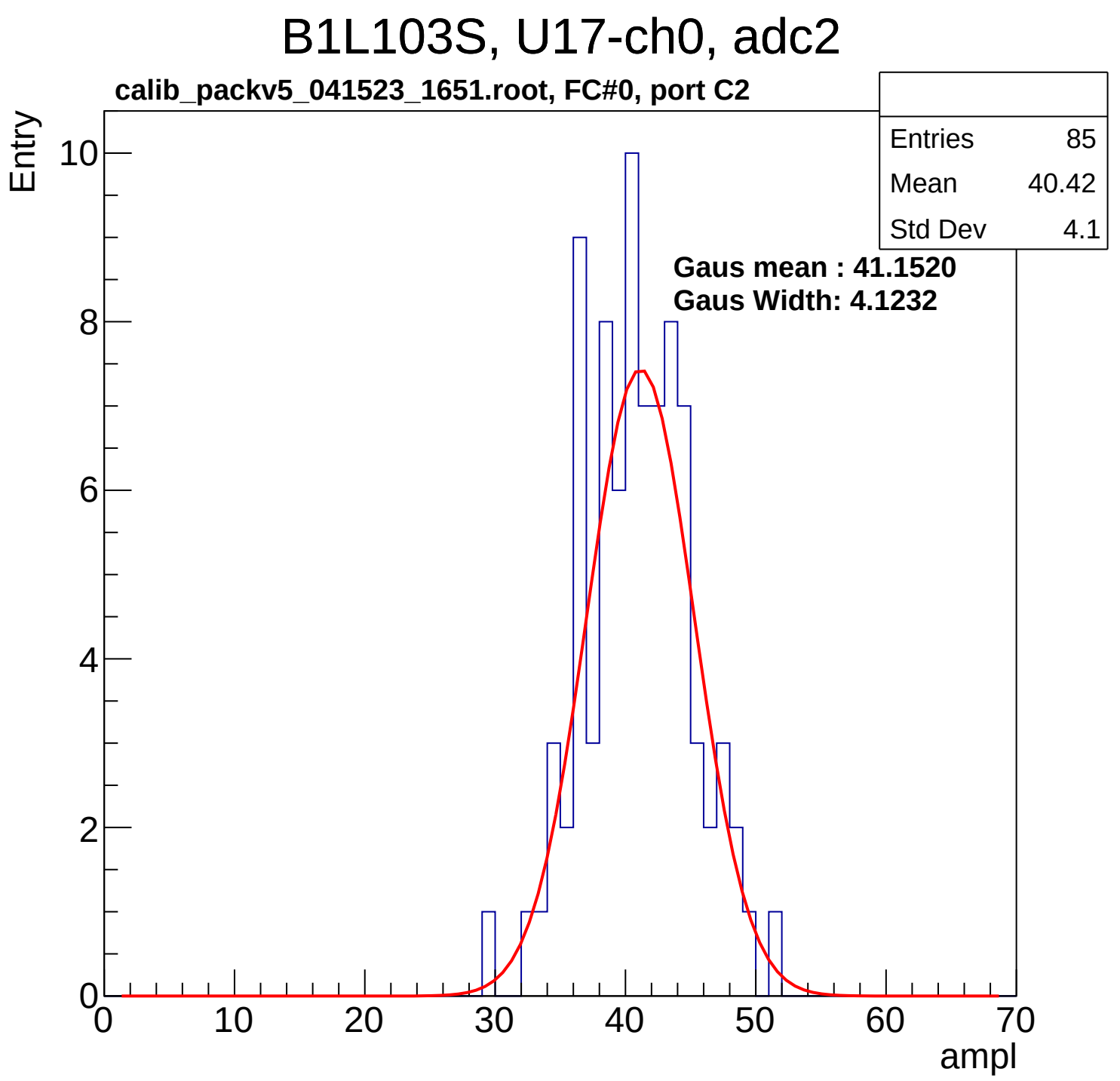
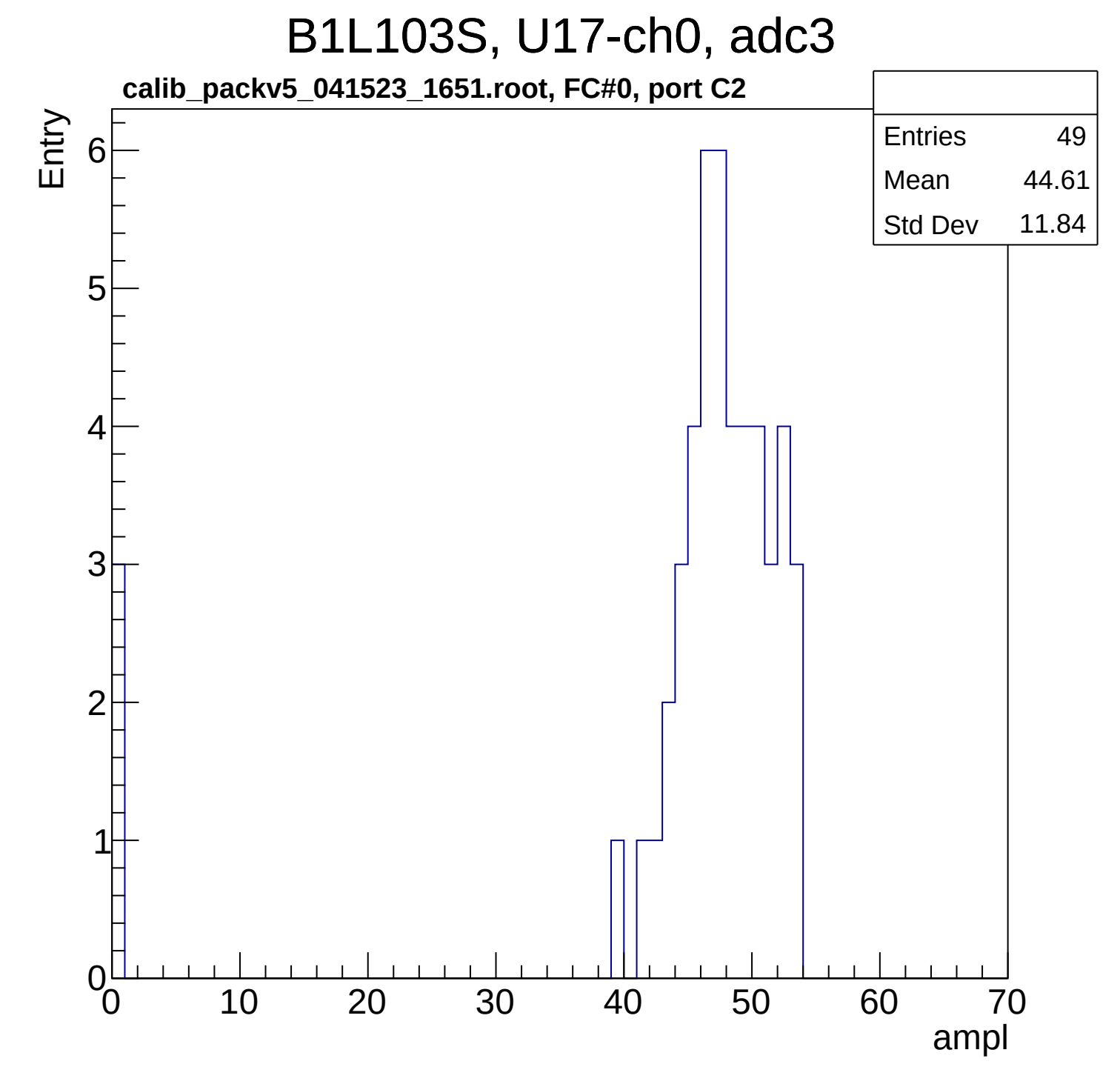
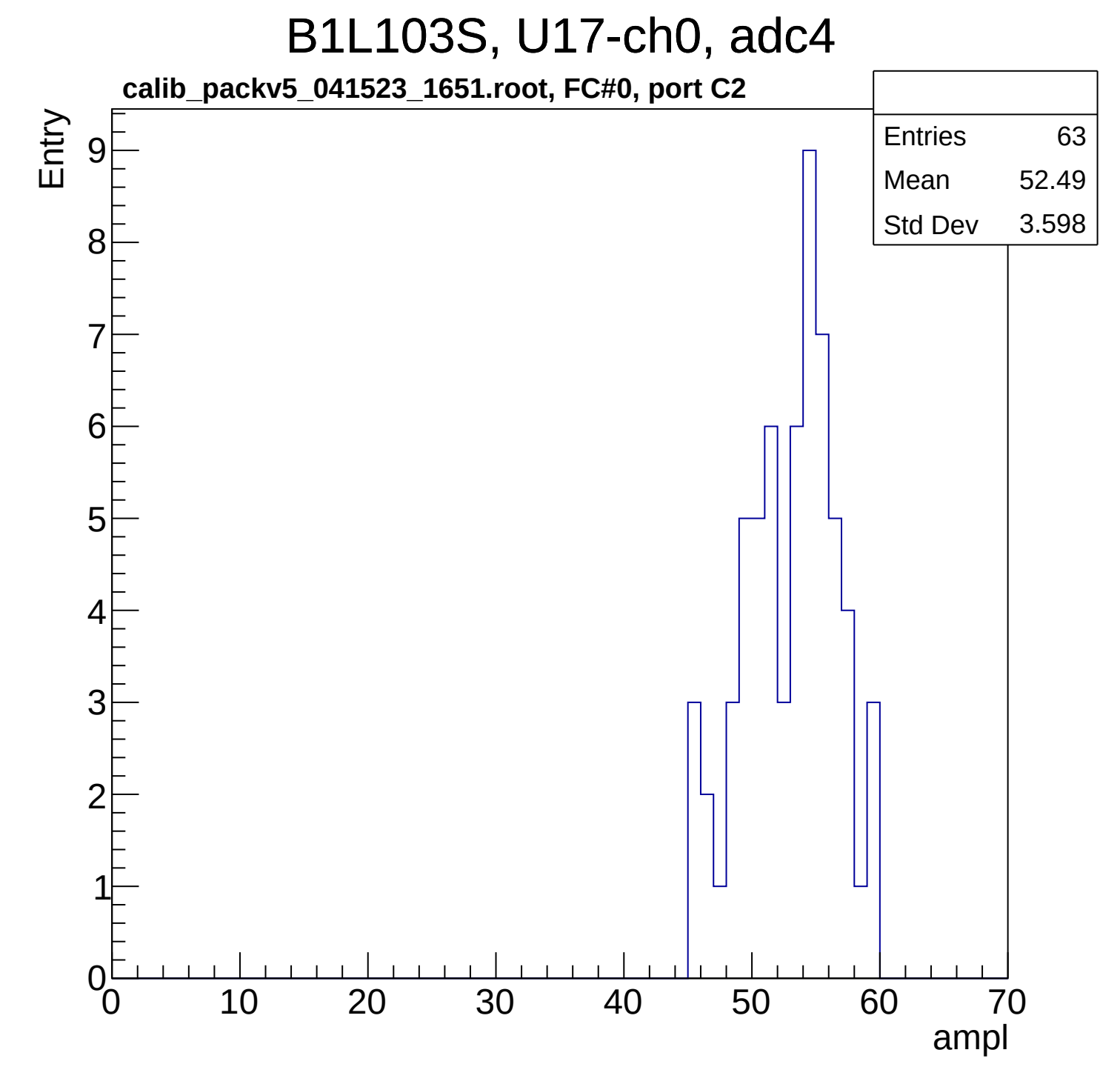
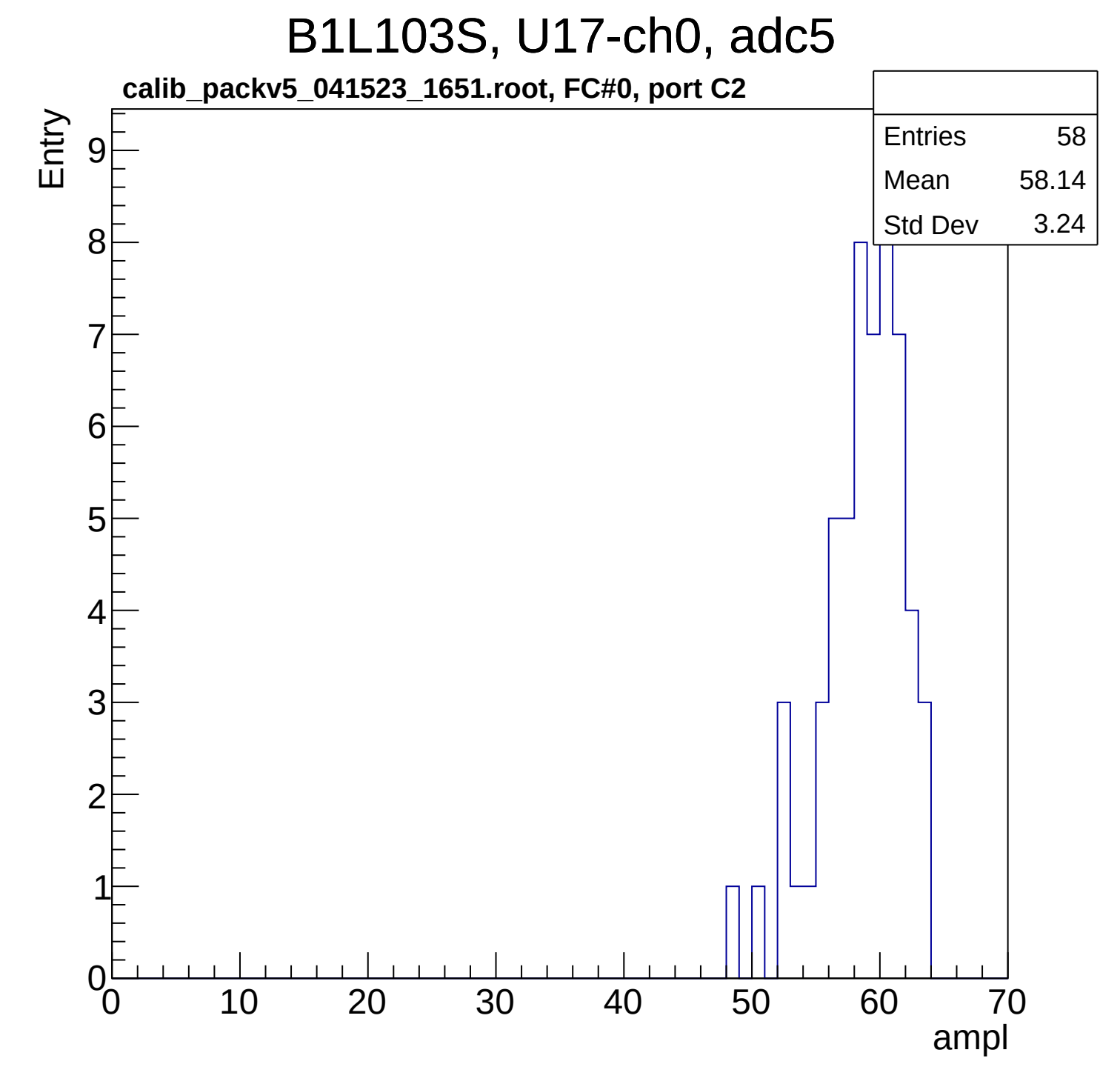

B1L103S, U17-ch0, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 132
Mean 16.89
Std Dev 12.3
Gaus mean : 26.2788
Gaus Width: 3.6960
Entry
ampl
0
5
10
15
20
25
30
35
40
0
10
20
30
40
50
60
70

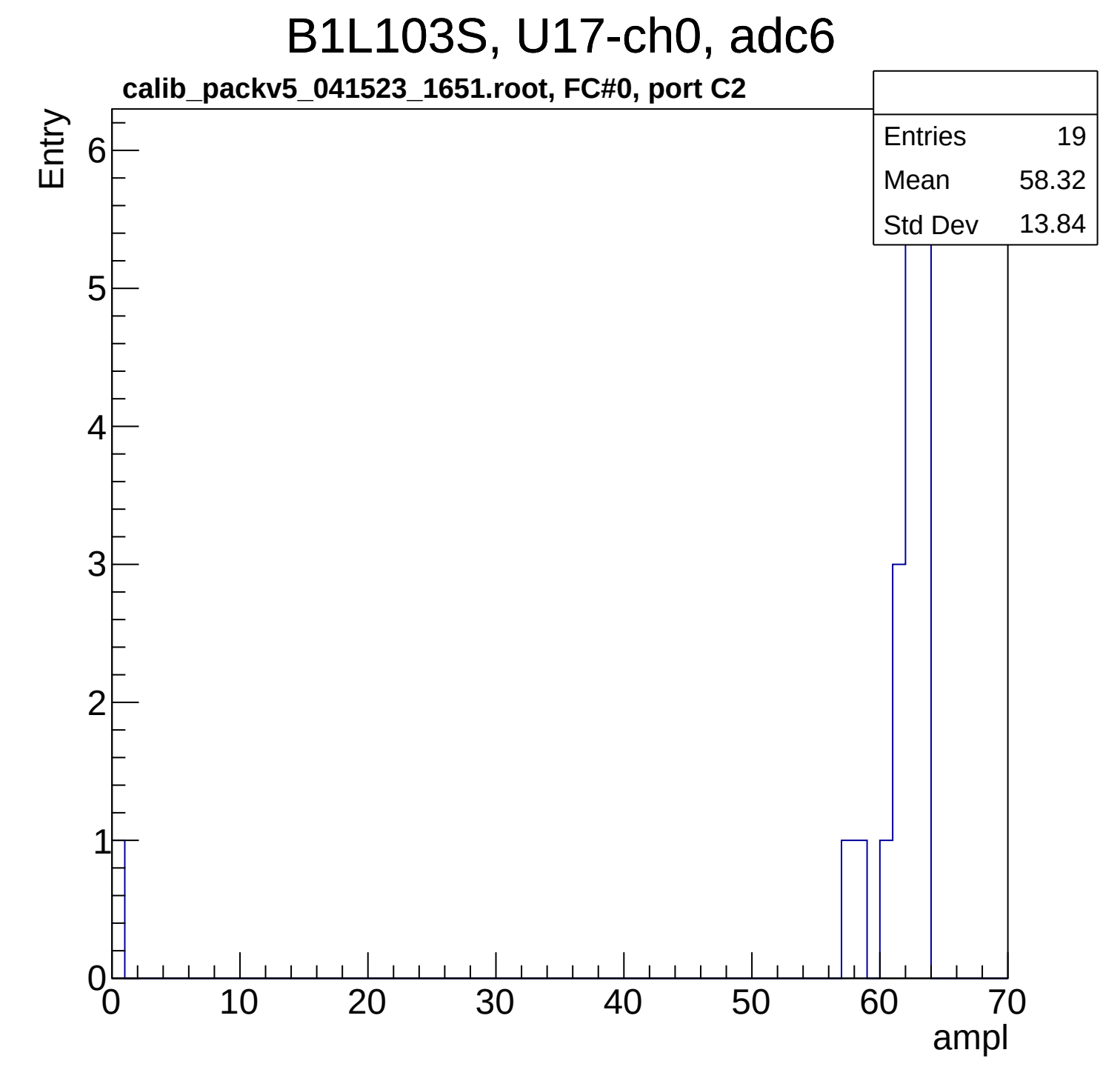

B1L103S, U17-ch0, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 29.42
Std Dev 11.54
Gaus mean : 32.7941
Gaus Width: 3.9741
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

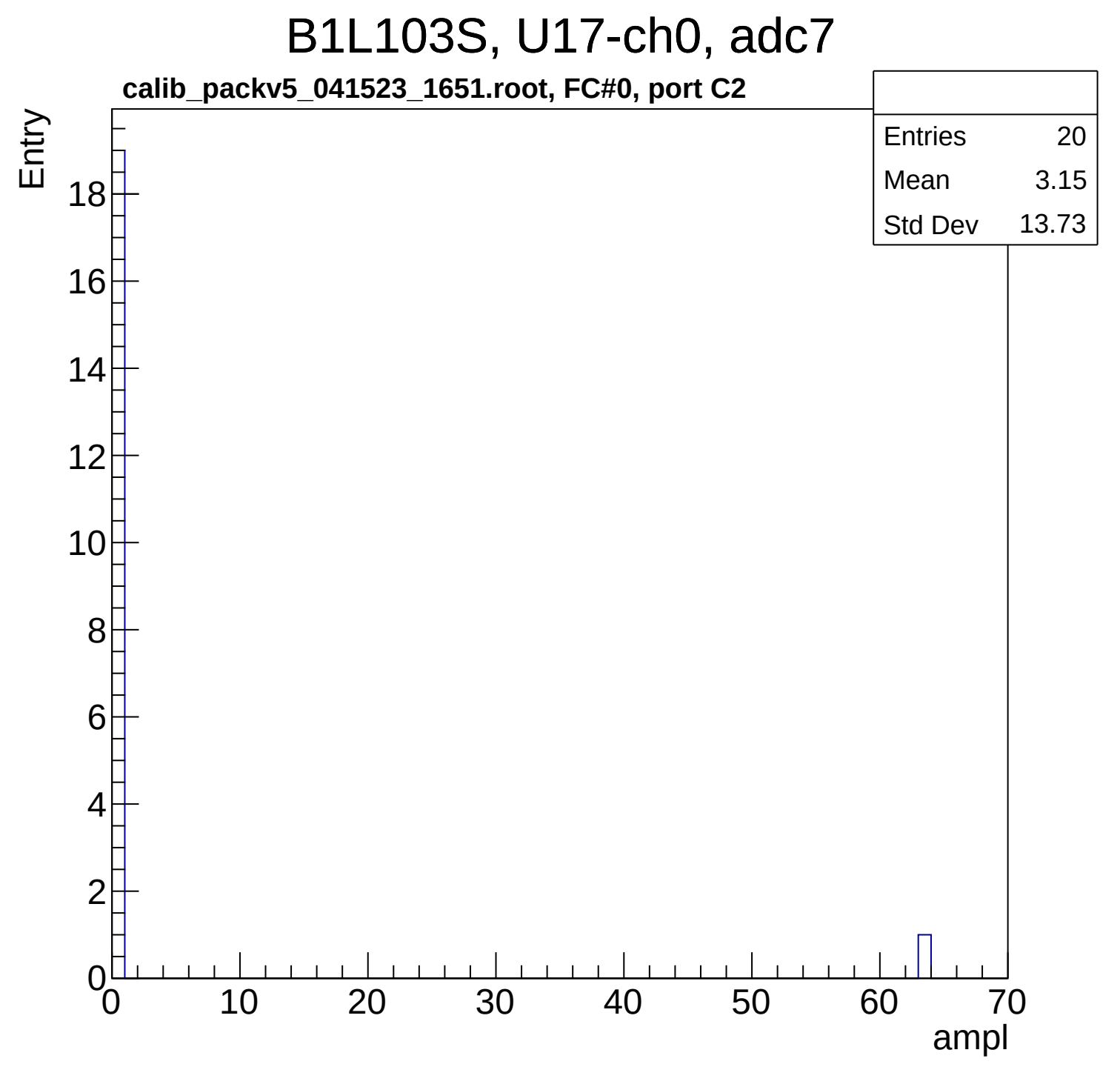

B1L103S, U17-ch0, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 40.42
Std Dev 4.1
Gaus mean : 41.1520
Gaus Width: 4.1232
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

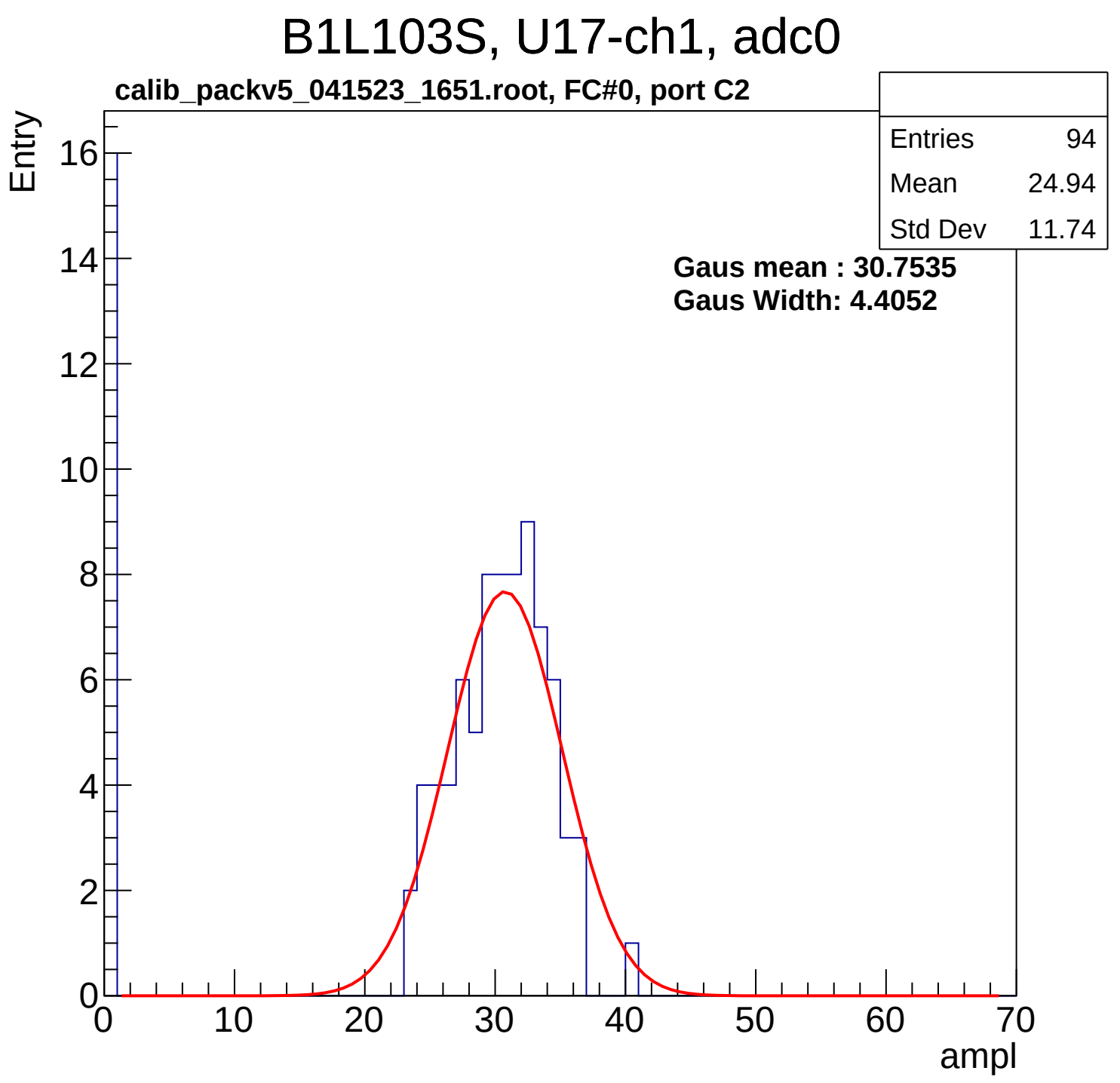

B1L103S, U17-ch0, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 44.61
Std Dev 11.84
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

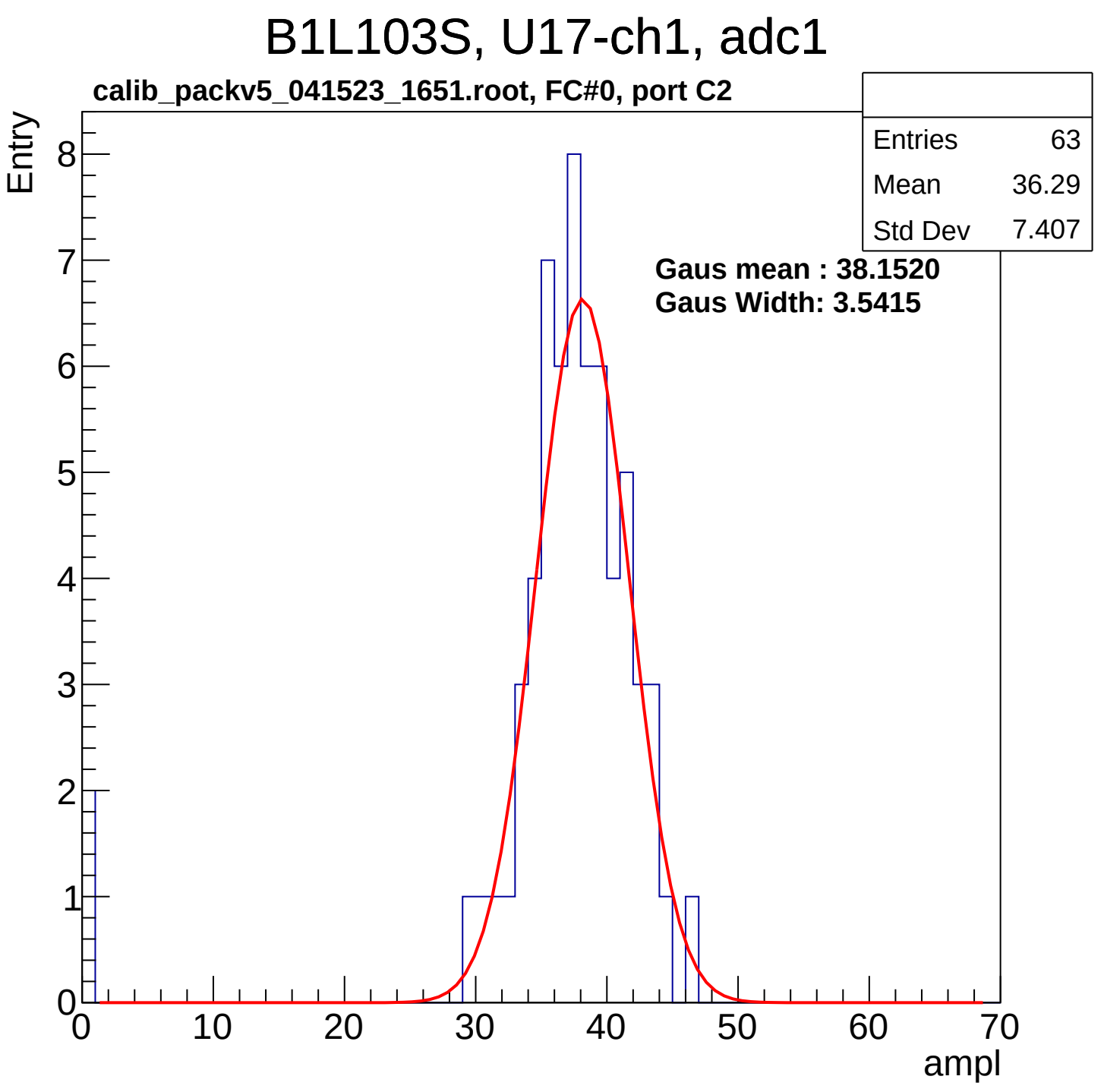

B1L103S, U17-ch0, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 52.49
Std Dev 3.598
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

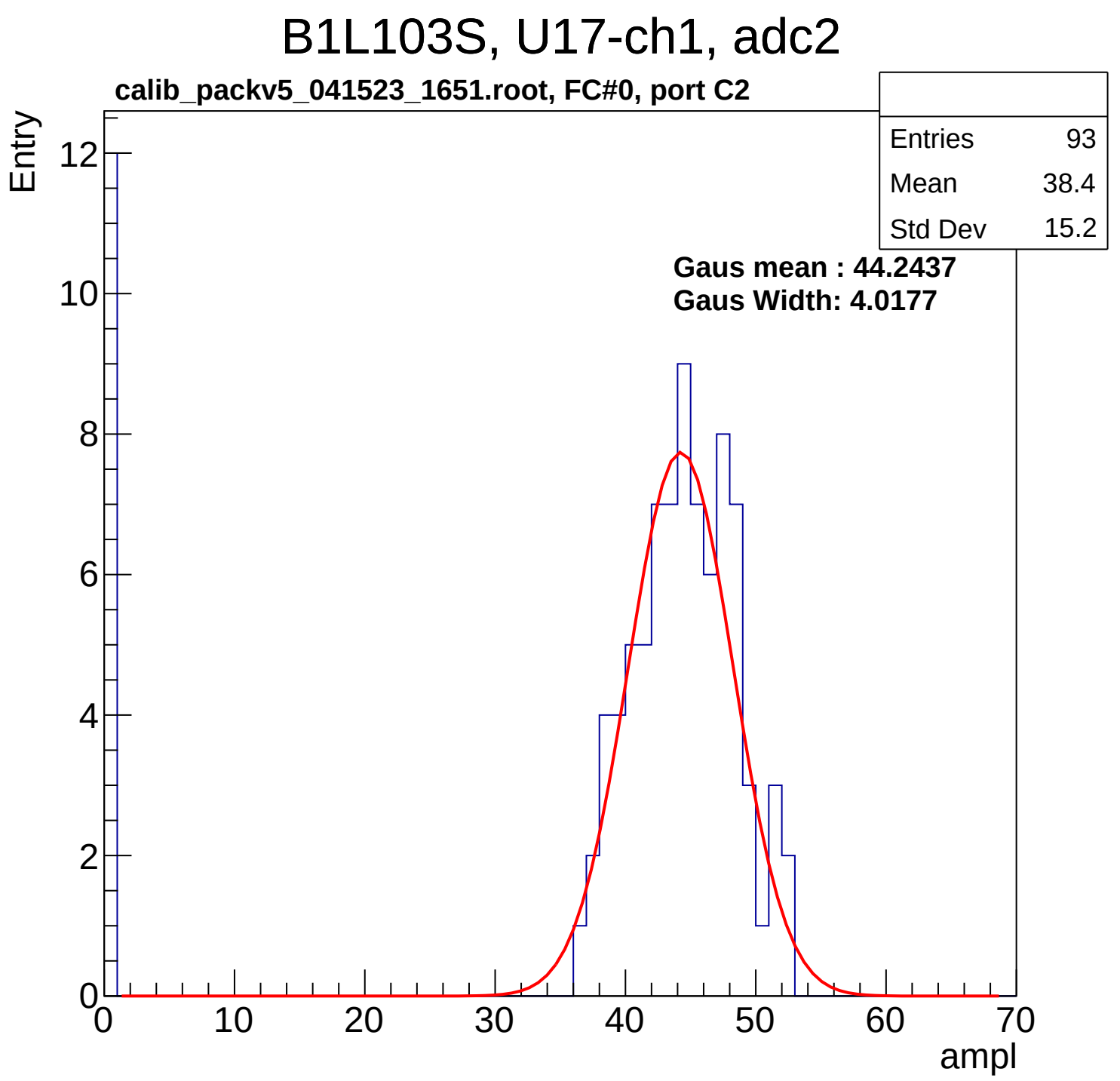

B1L103S, U17-ch0, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.14
Std Dev 3.24
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

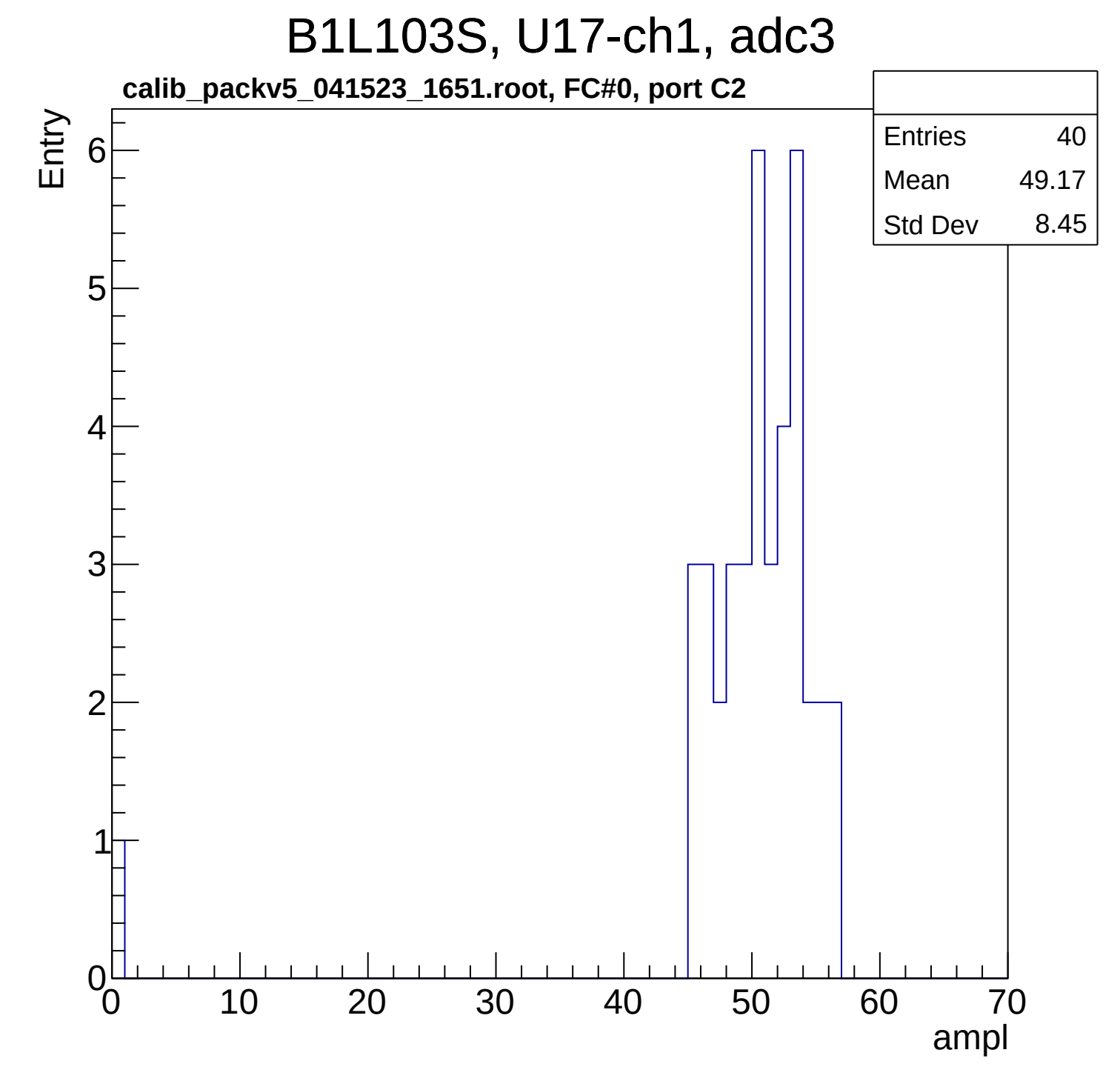

B1L103S, U17-ch0, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 58.32
Std Dev 13.84
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

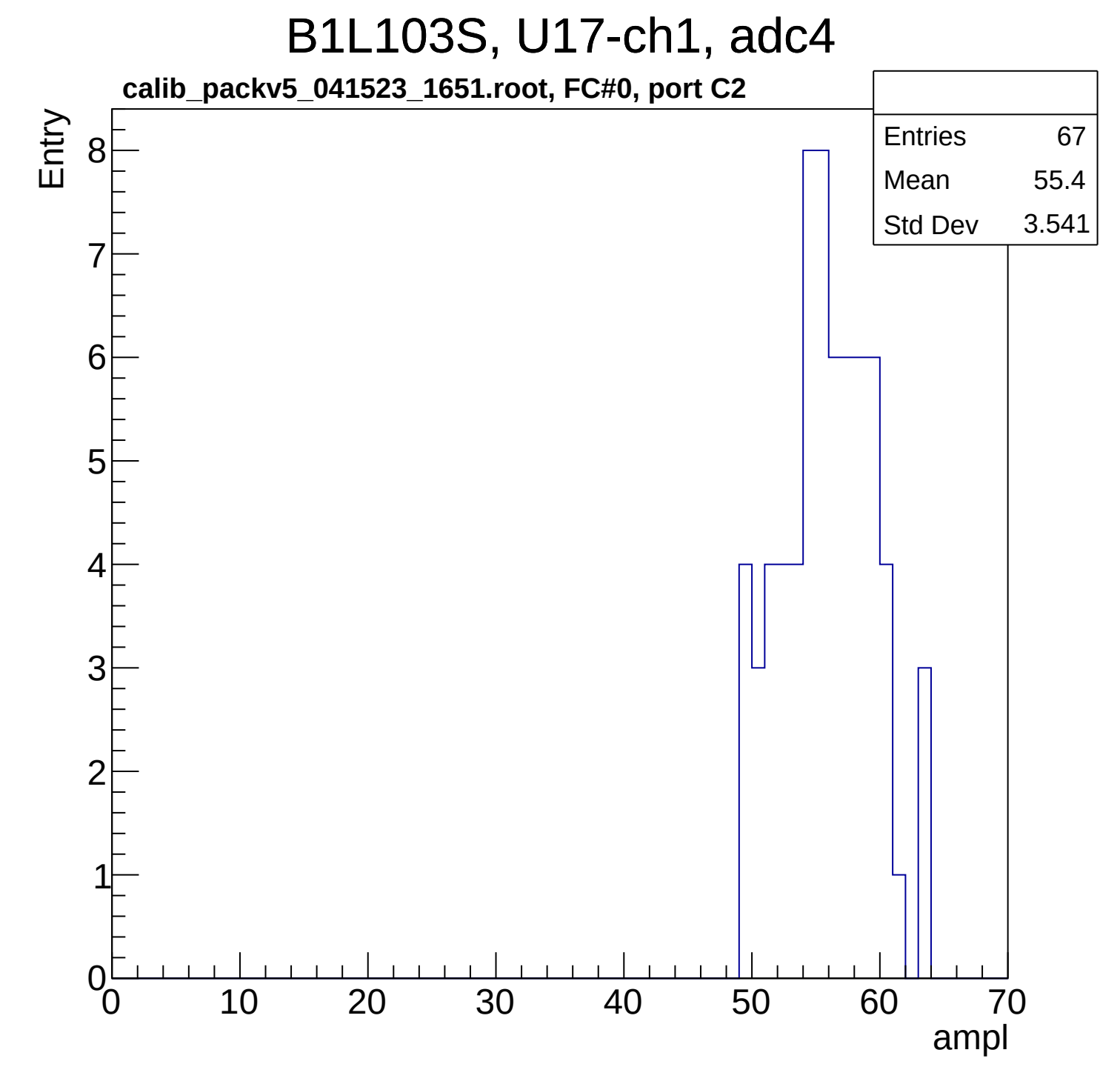

B1L103S, U17-ch0, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

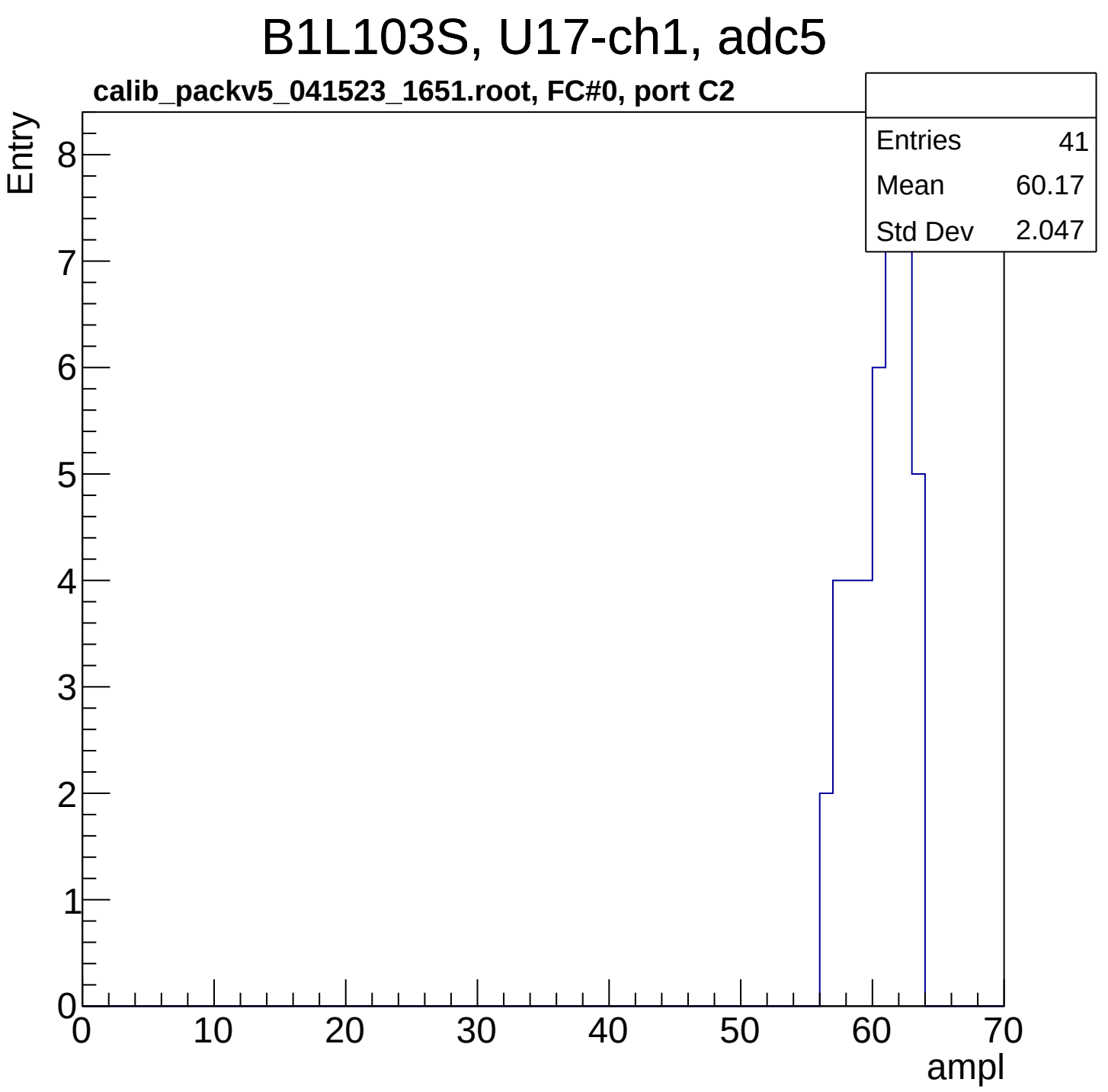

B1L103S, U17-ch1, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 24.94
Std Dev 11.74
Gaus mean : 30.7535
Gaus Width: 4.4052
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

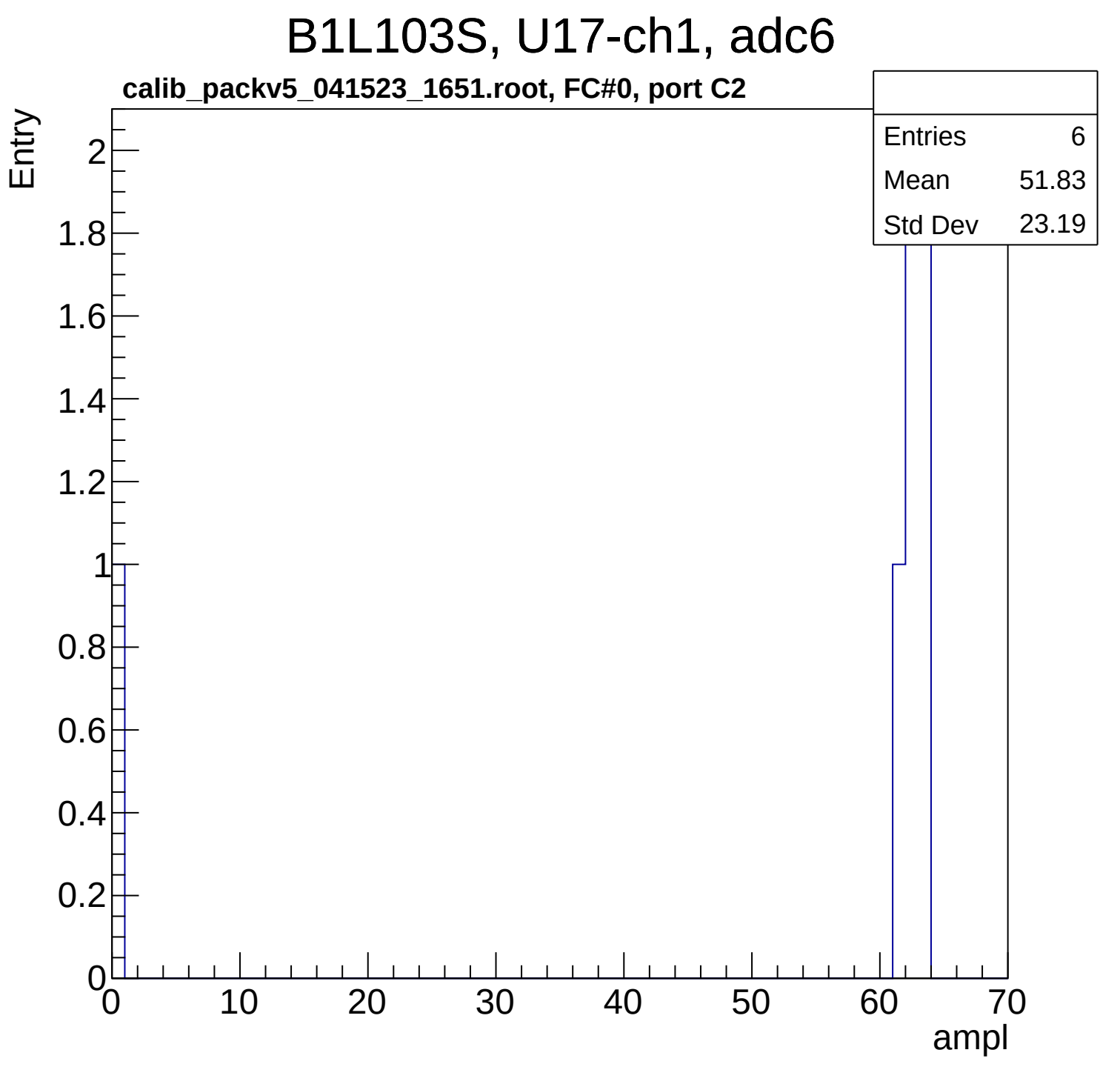

B1L103S, U17-ch1, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 36.29
Std Dev 7.407
Gaus mean : 38.1520
Gaus Width: 3.5415
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

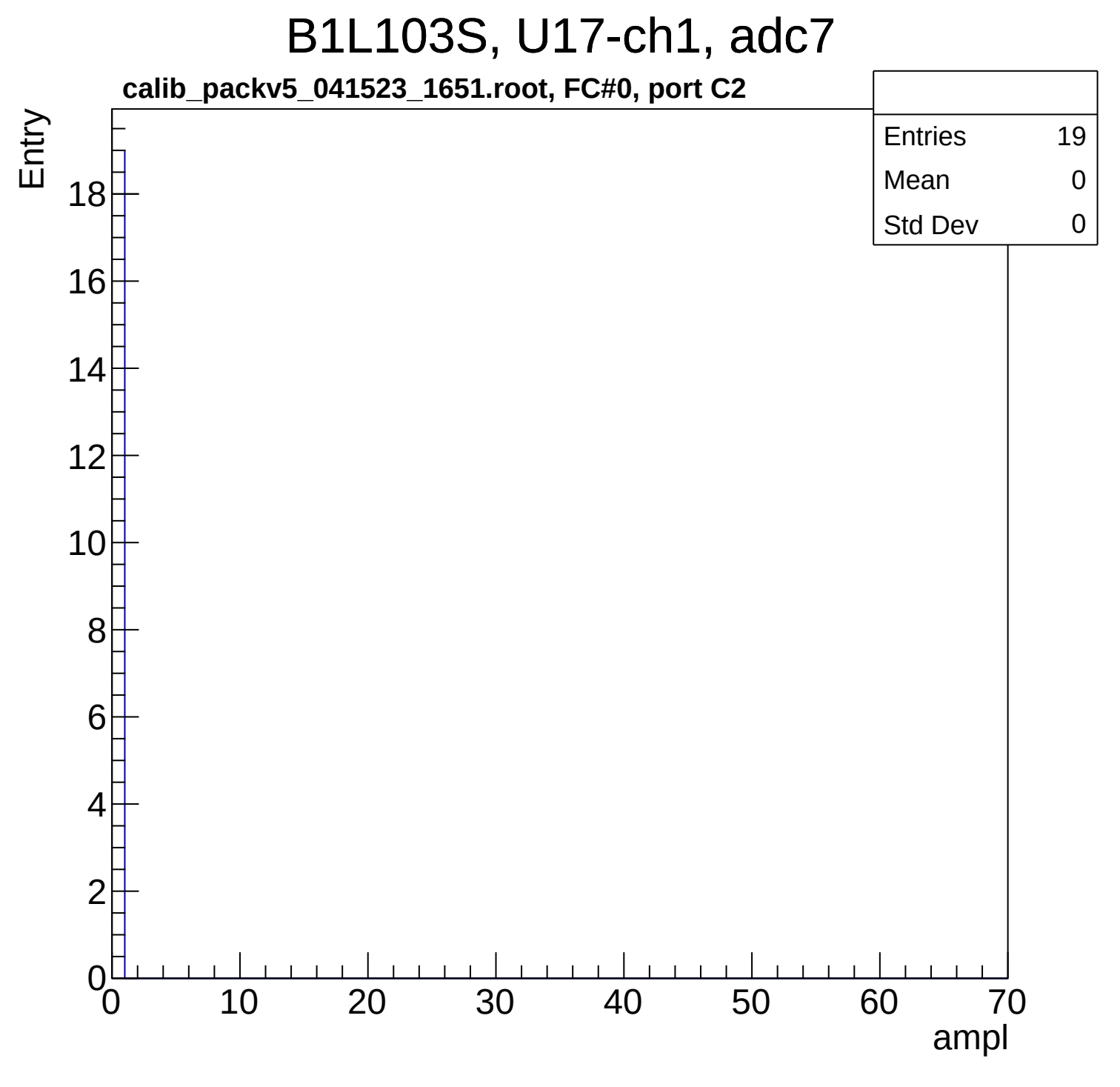

B1L103S, U17-ch1, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 38.4
Std Dev 15.2
Gaus mean : 44.2437
Gaus Width: 4.0177
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

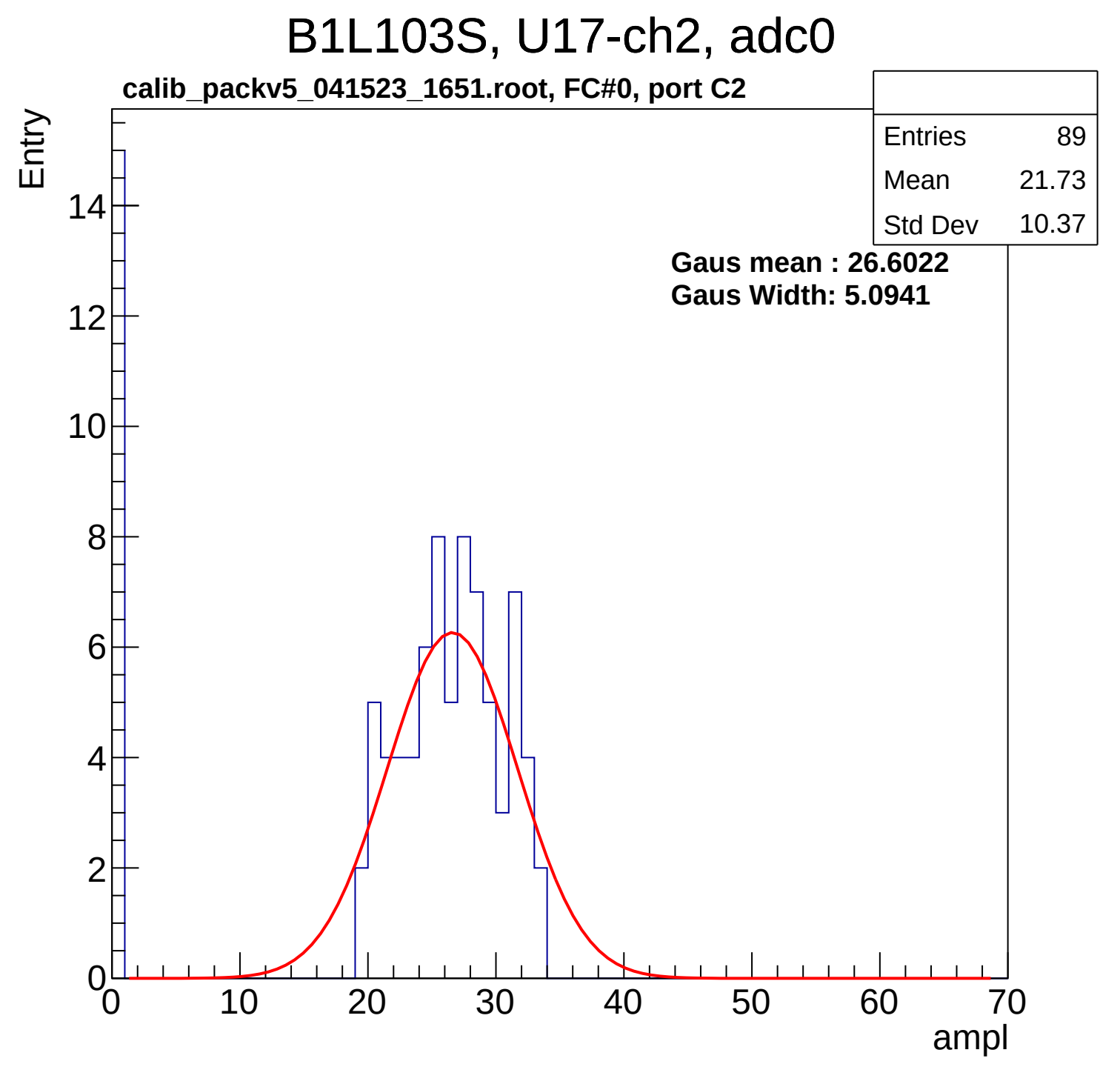

B1L103S, U17-ch1, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 49.17
Std Dev 8.45
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

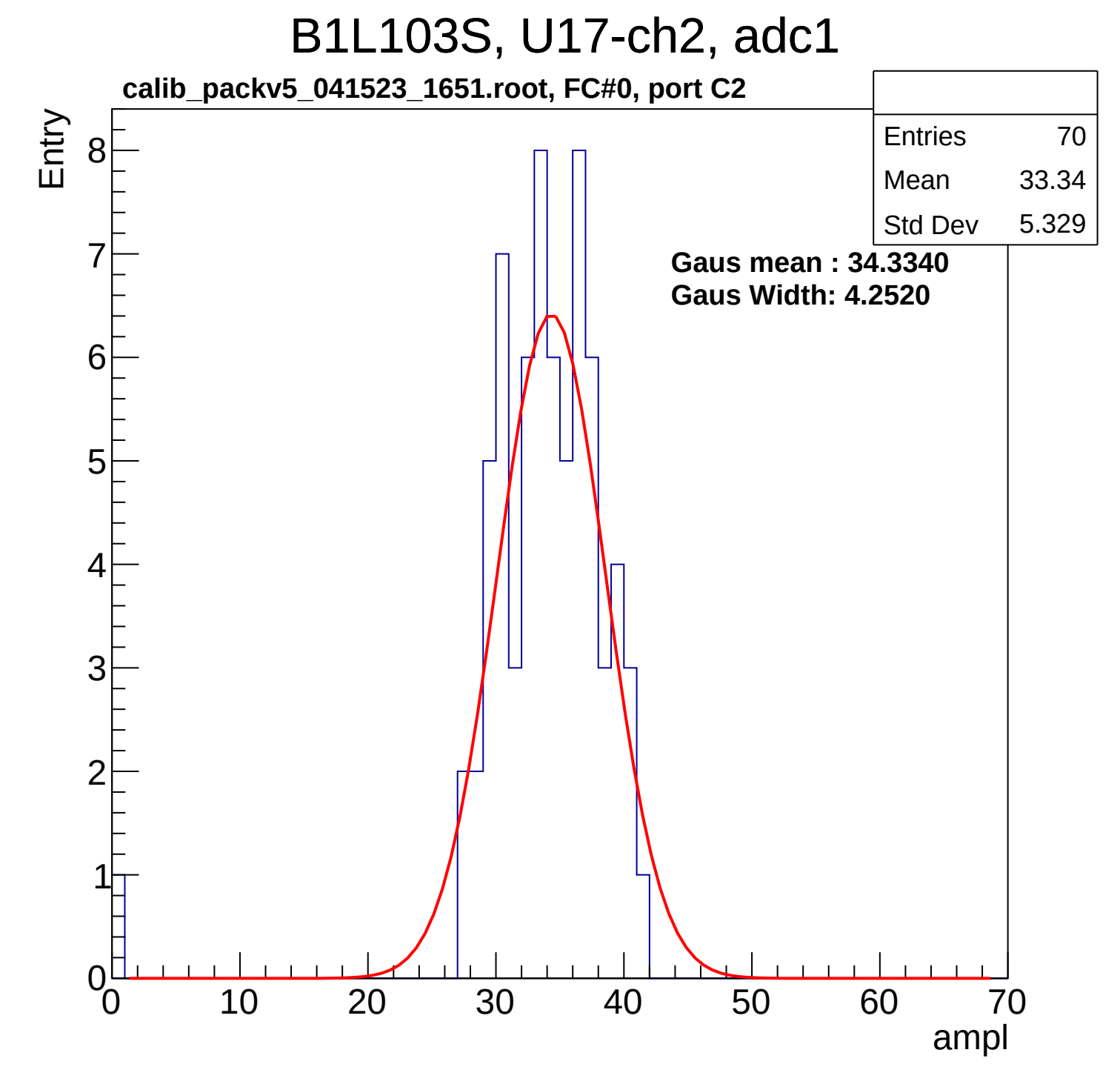

B1L103S, U17-ch1, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 55.4
Std Dev 3.541
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

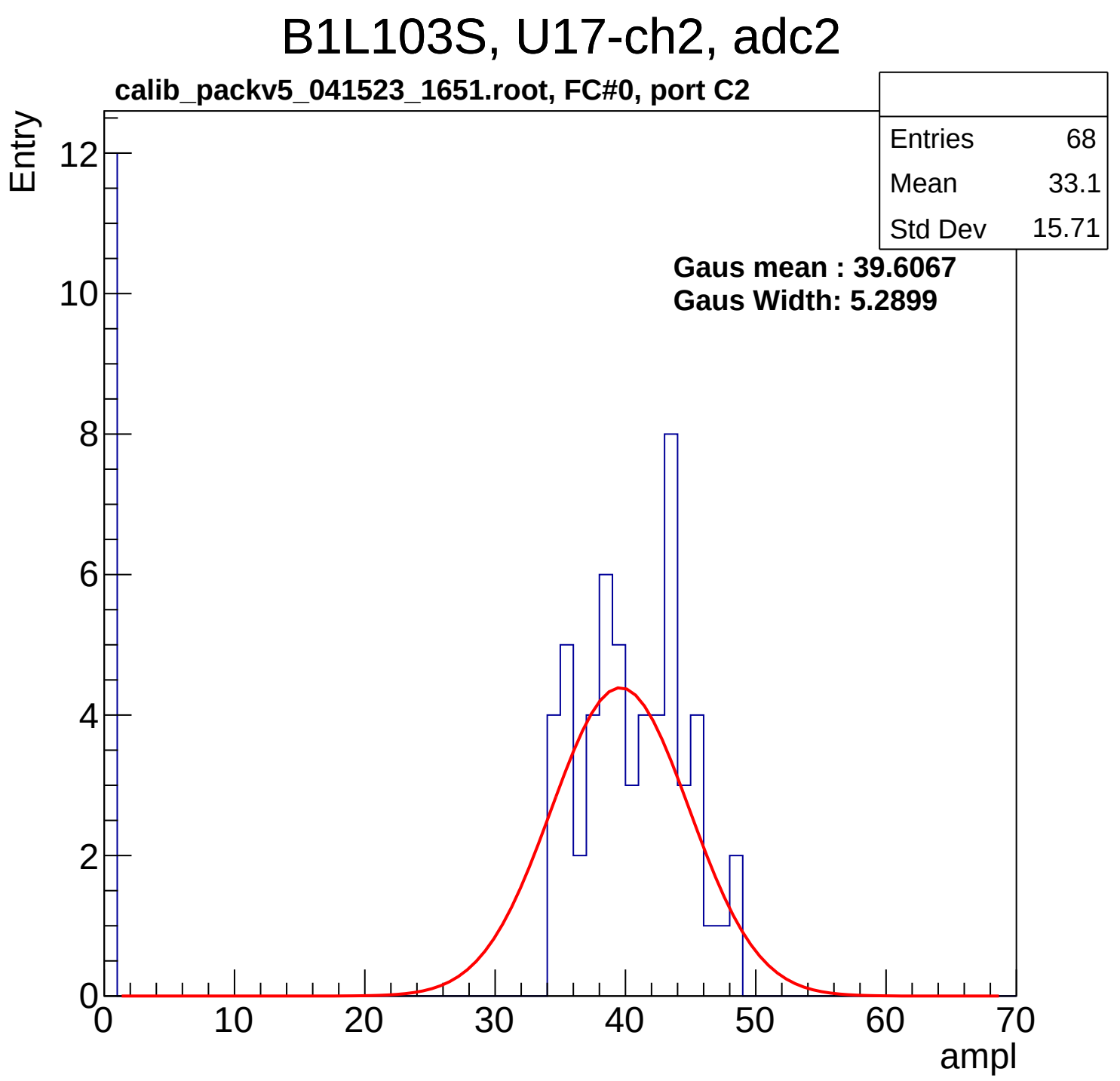

B1L103S, U17-ch1, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 60.17
Std Dev 2.047
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

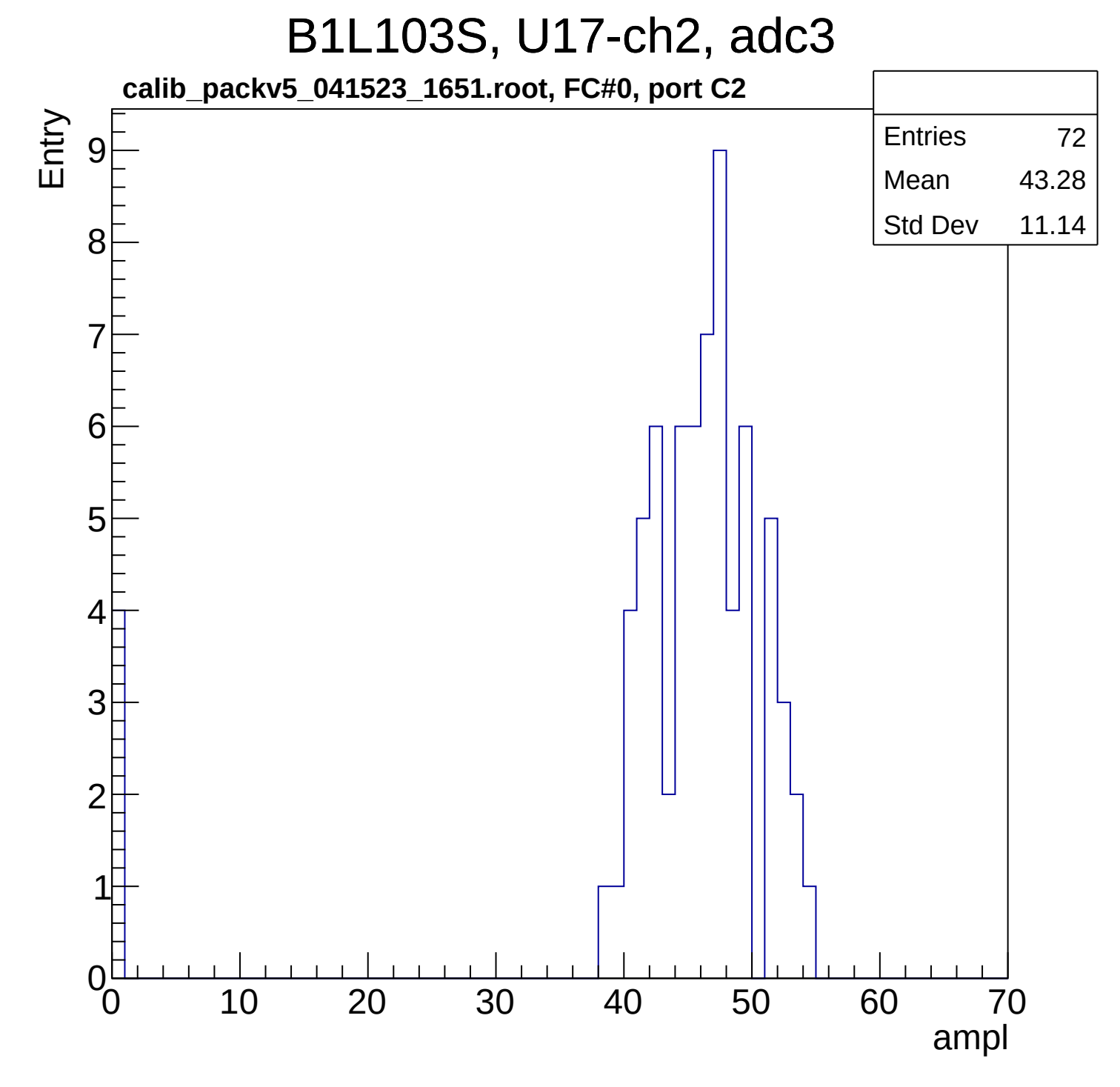

B1L103S, U17-ch1, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 51.83
Std Dev 23.19
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

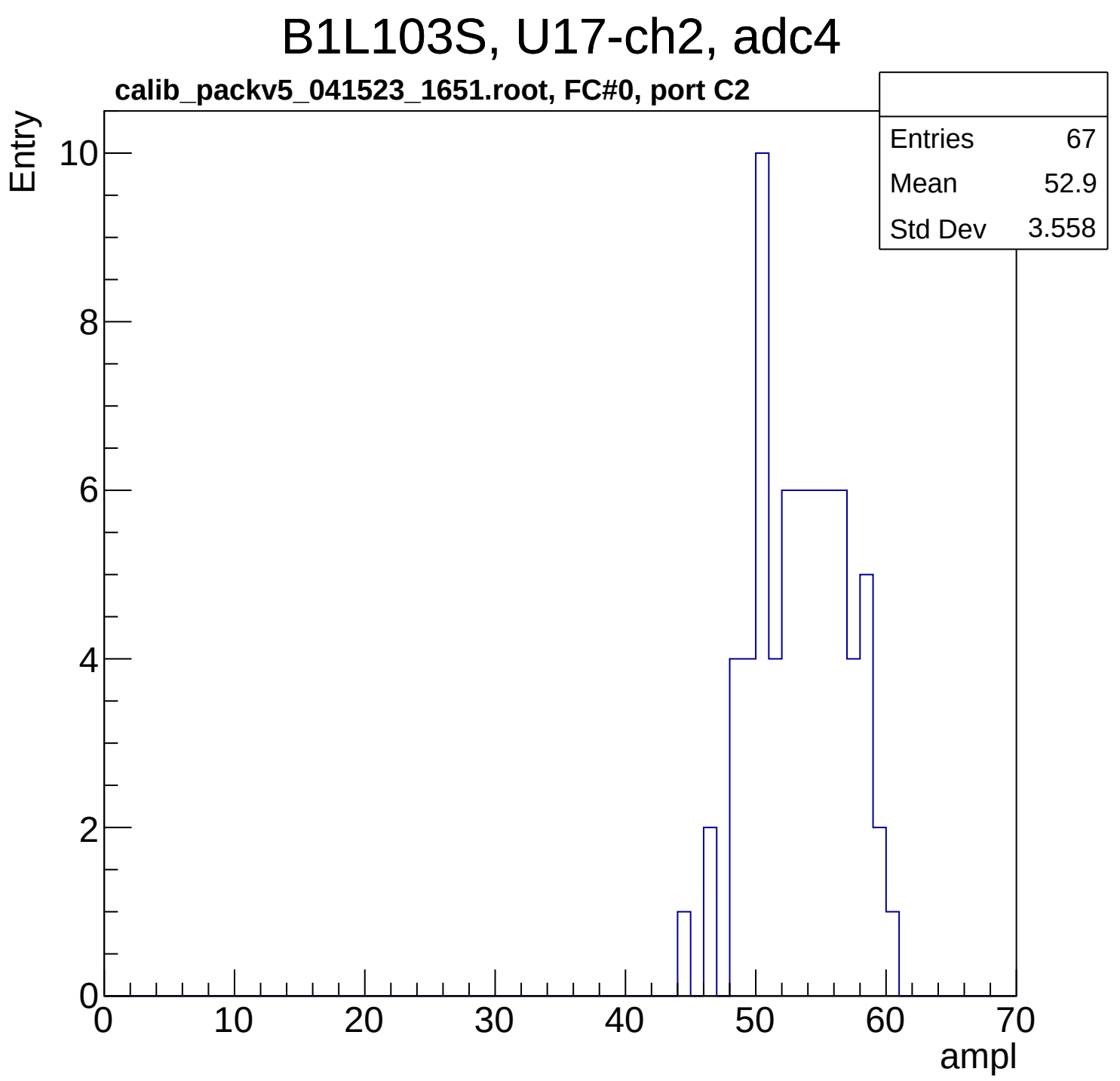

B1L103S, U17-ch1, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

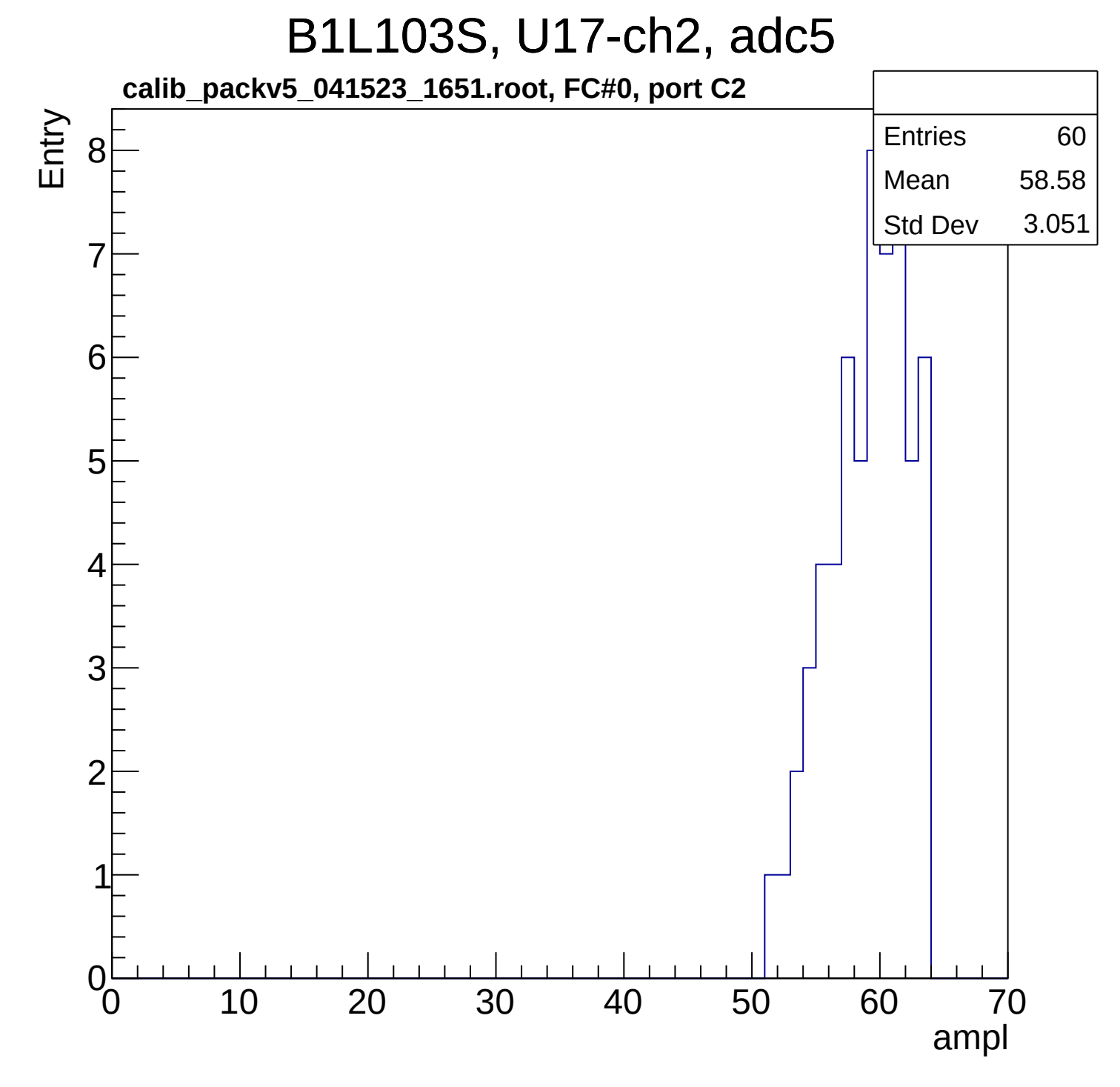

B1L103S, U17-ch2, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 21.73
Std Dev 10.37
Gaus mean : 26.6022
Gaus Width: 5.0941
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

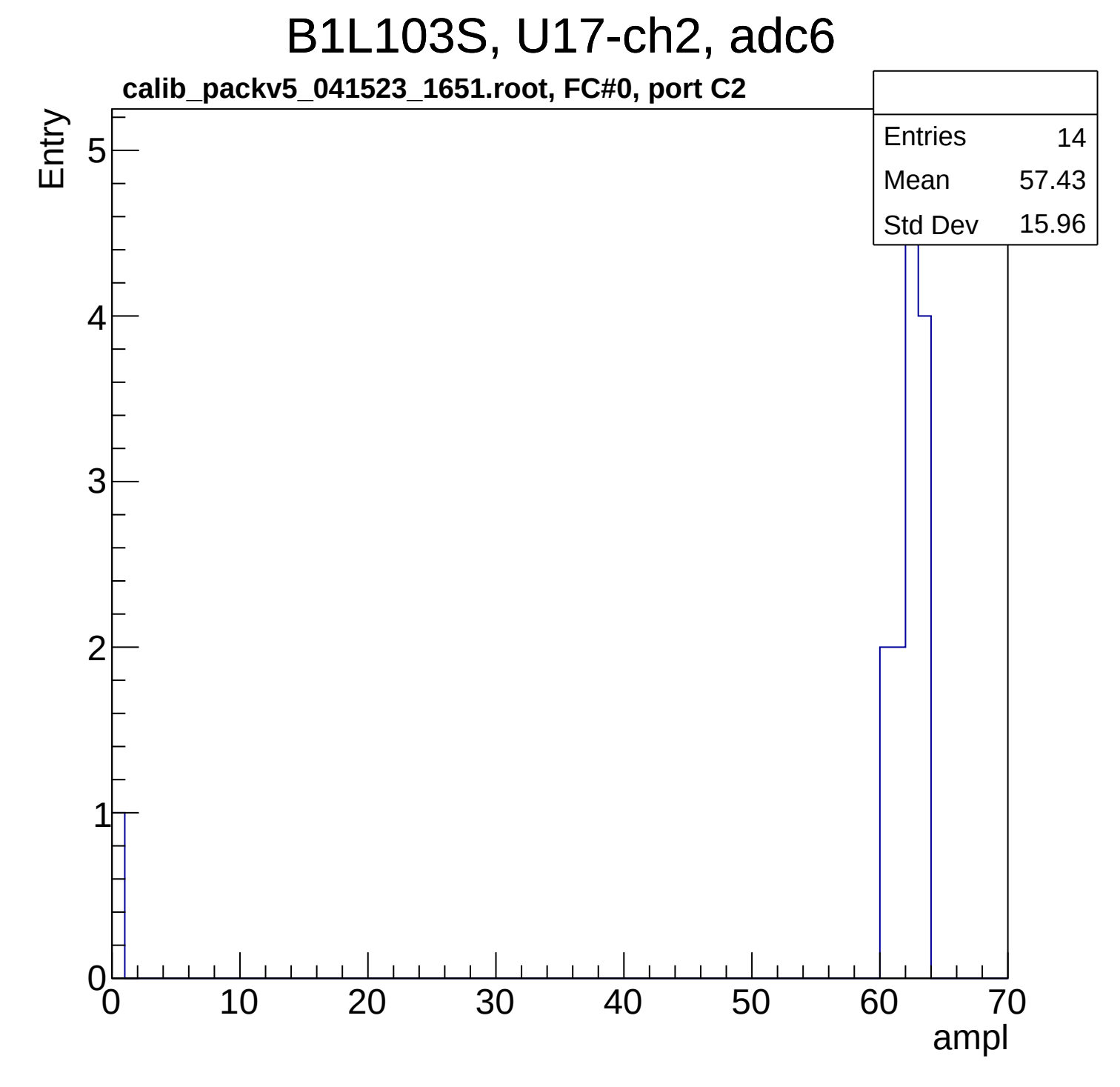

B1L103S, U17-ch2, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 33.34
Std Dev 5.329
Gaus mean : 34.3340
Gaus Width: 4.2520
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

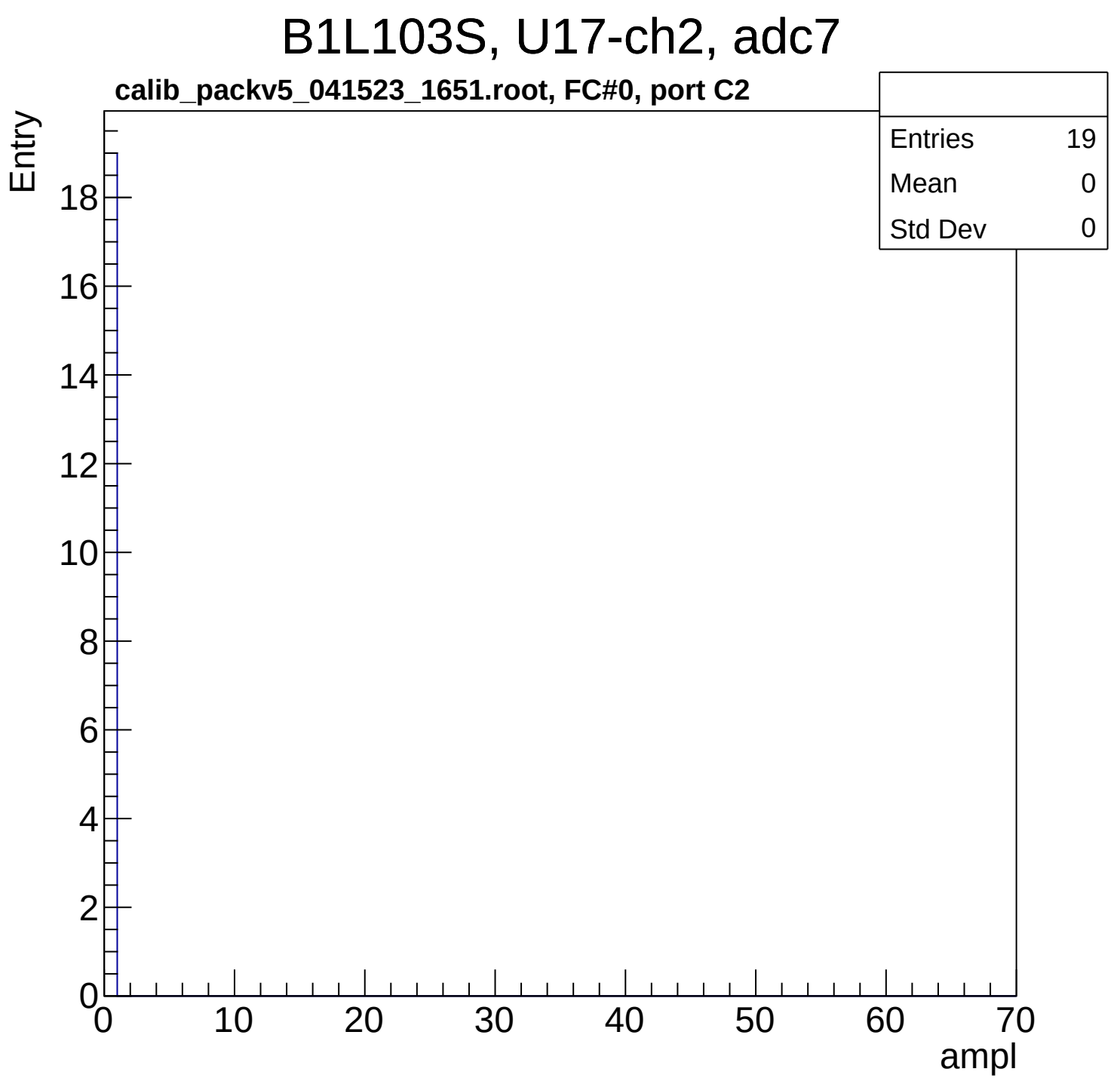

B1L103S, U17-ch2, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 33.1
Std Dev 15.71
Gaus mean : 39.6067
Gaus Width: 5.2899
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

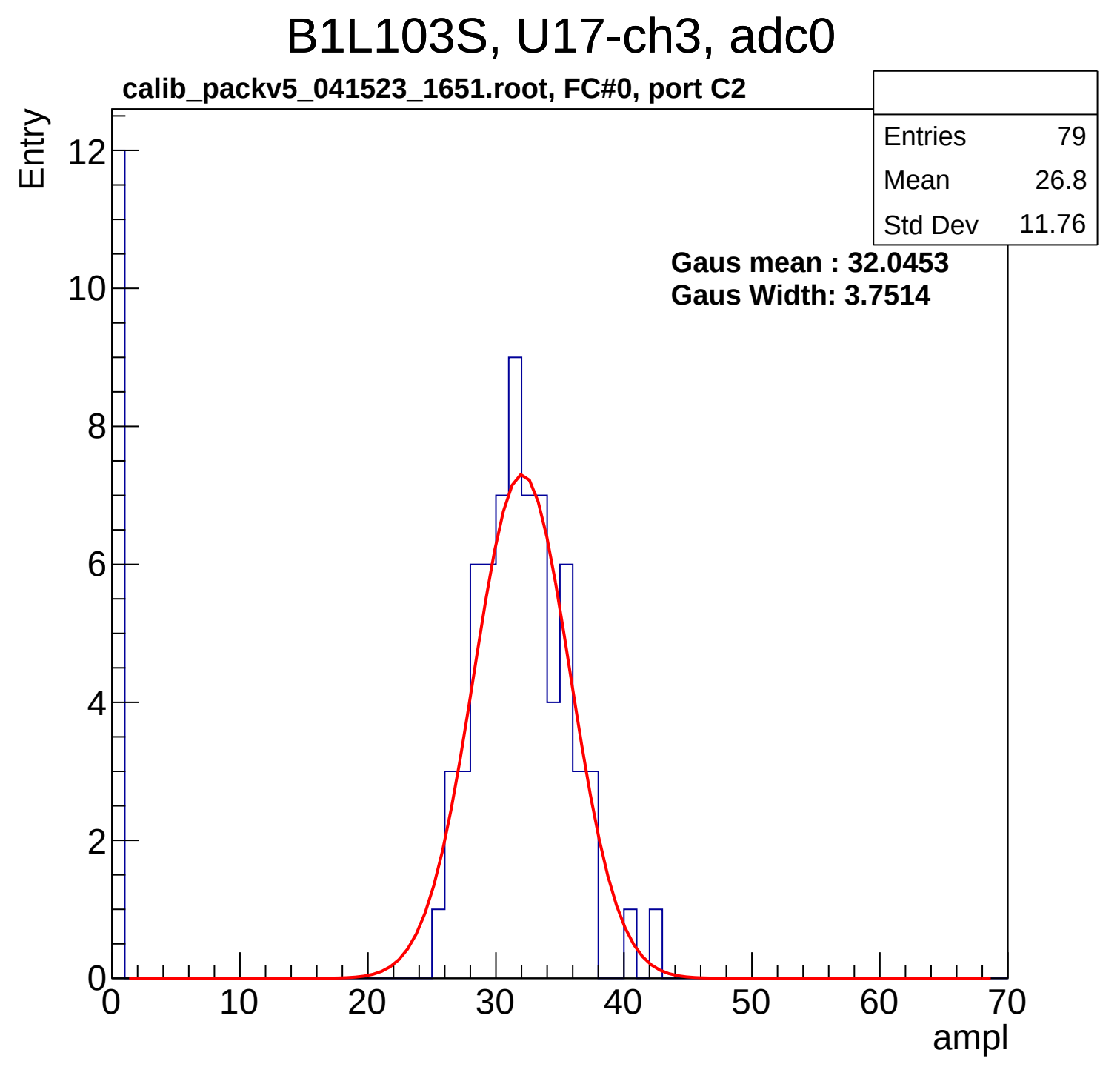

B1L103S, U17-ch2, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 43.28
Std Dev 11.14
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

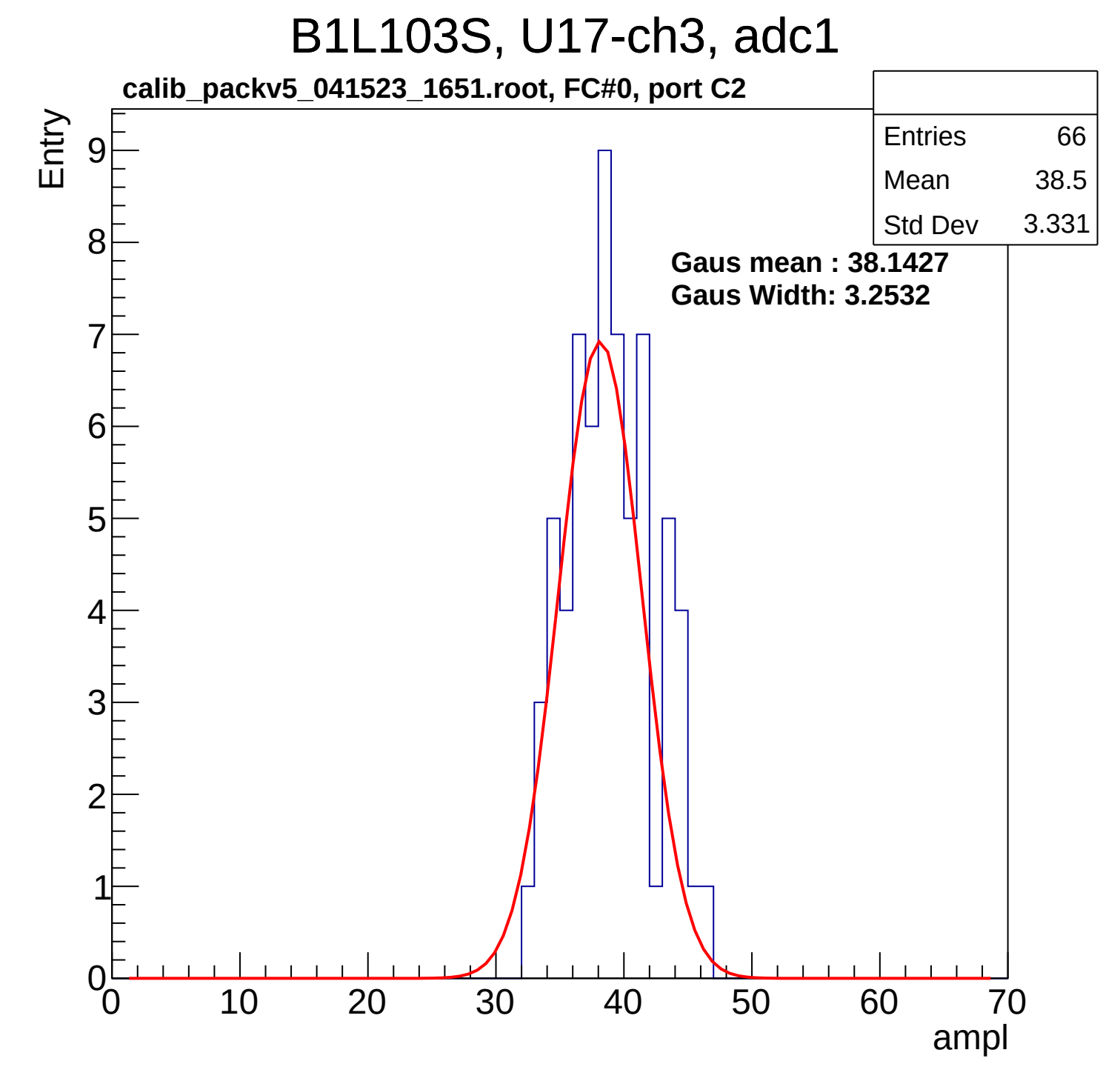

B1L103S, U17-ch2, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 52.9
Std Dev 3.558
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

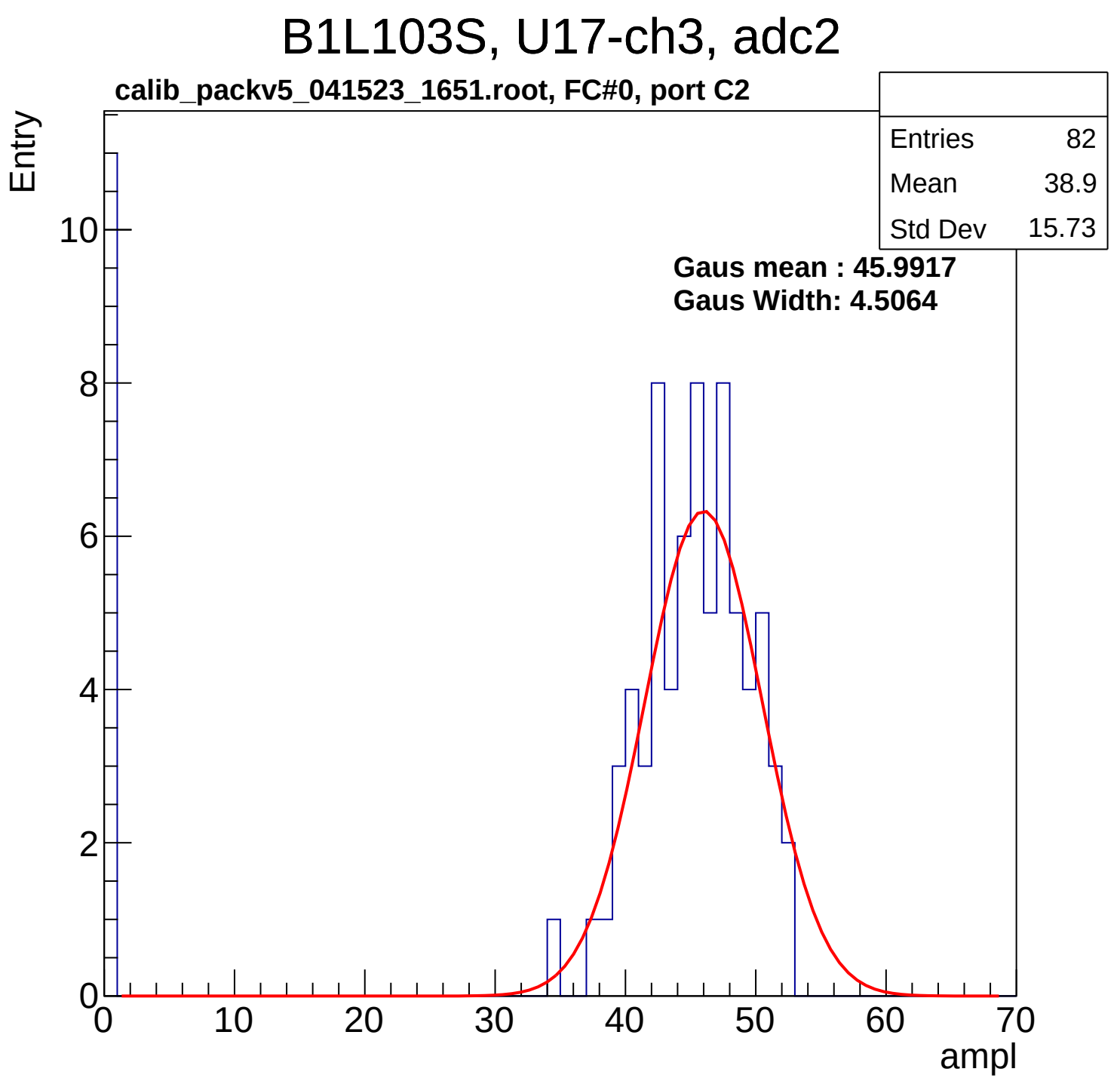

B1L103S, U17-ch2, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 58.58
Std Dev 3.051
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

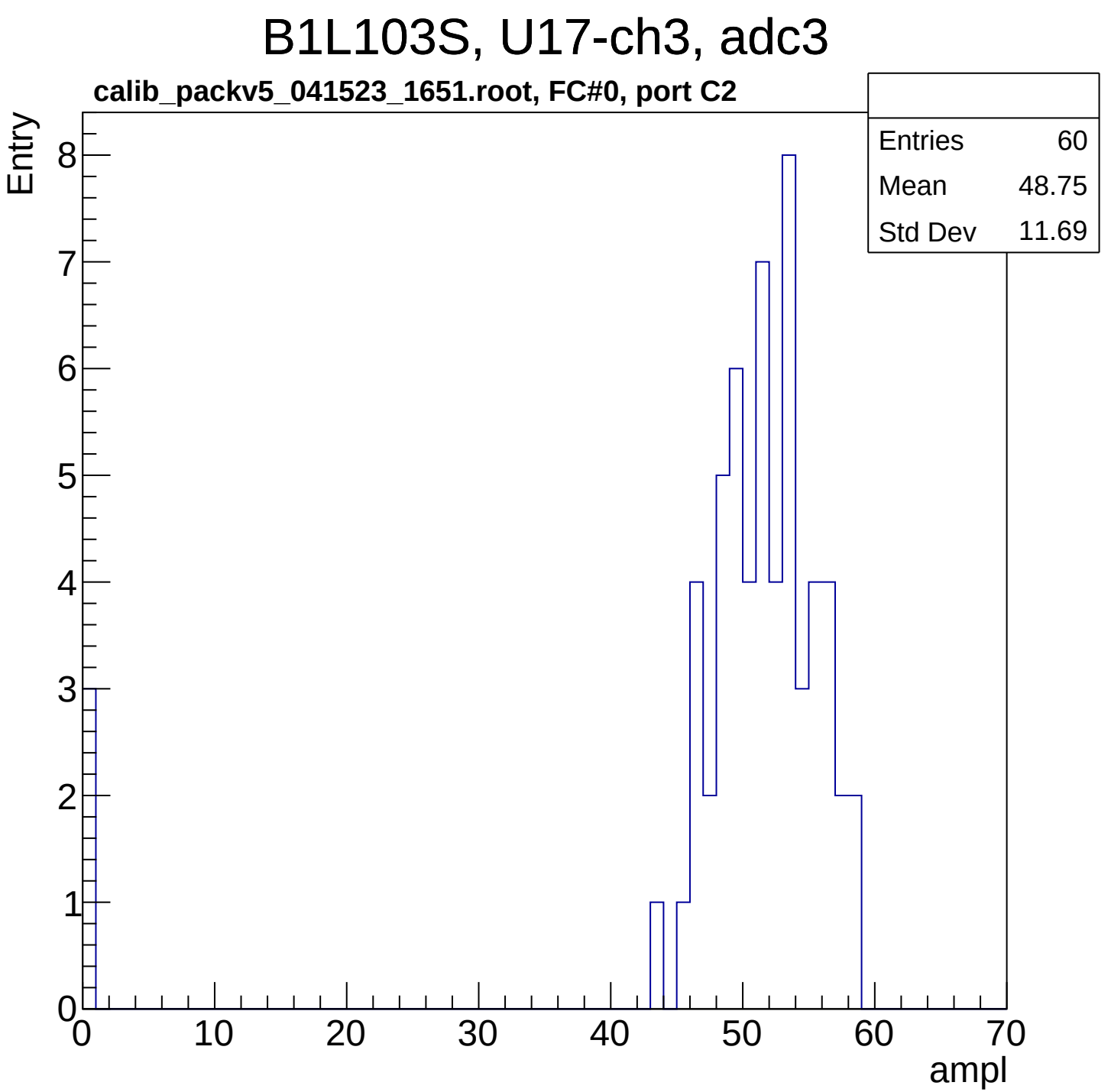

B1L103S, U17-ch2, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 57.43
Std Dev 15.96
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

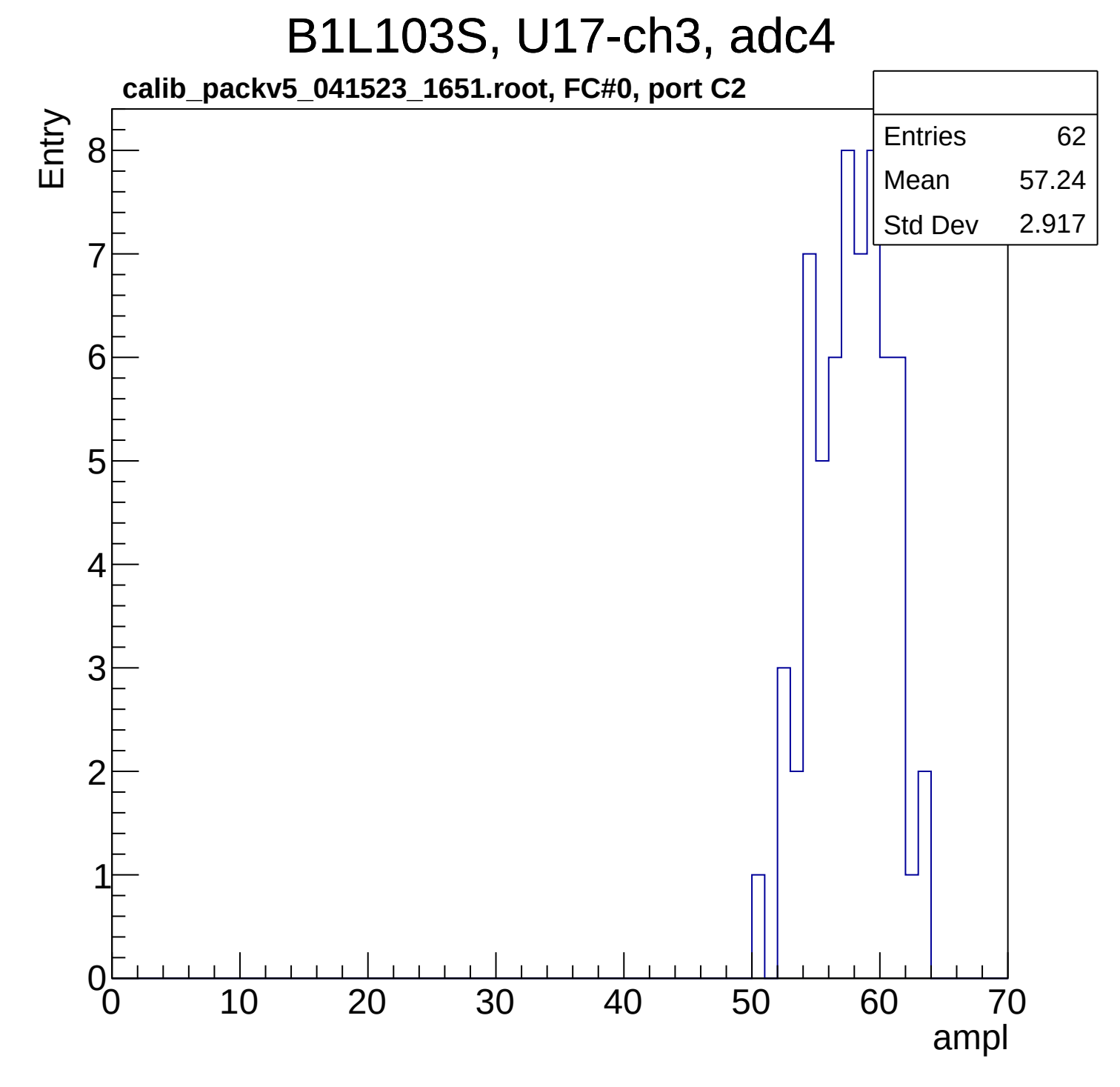

B1L103S, U17-ch2, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

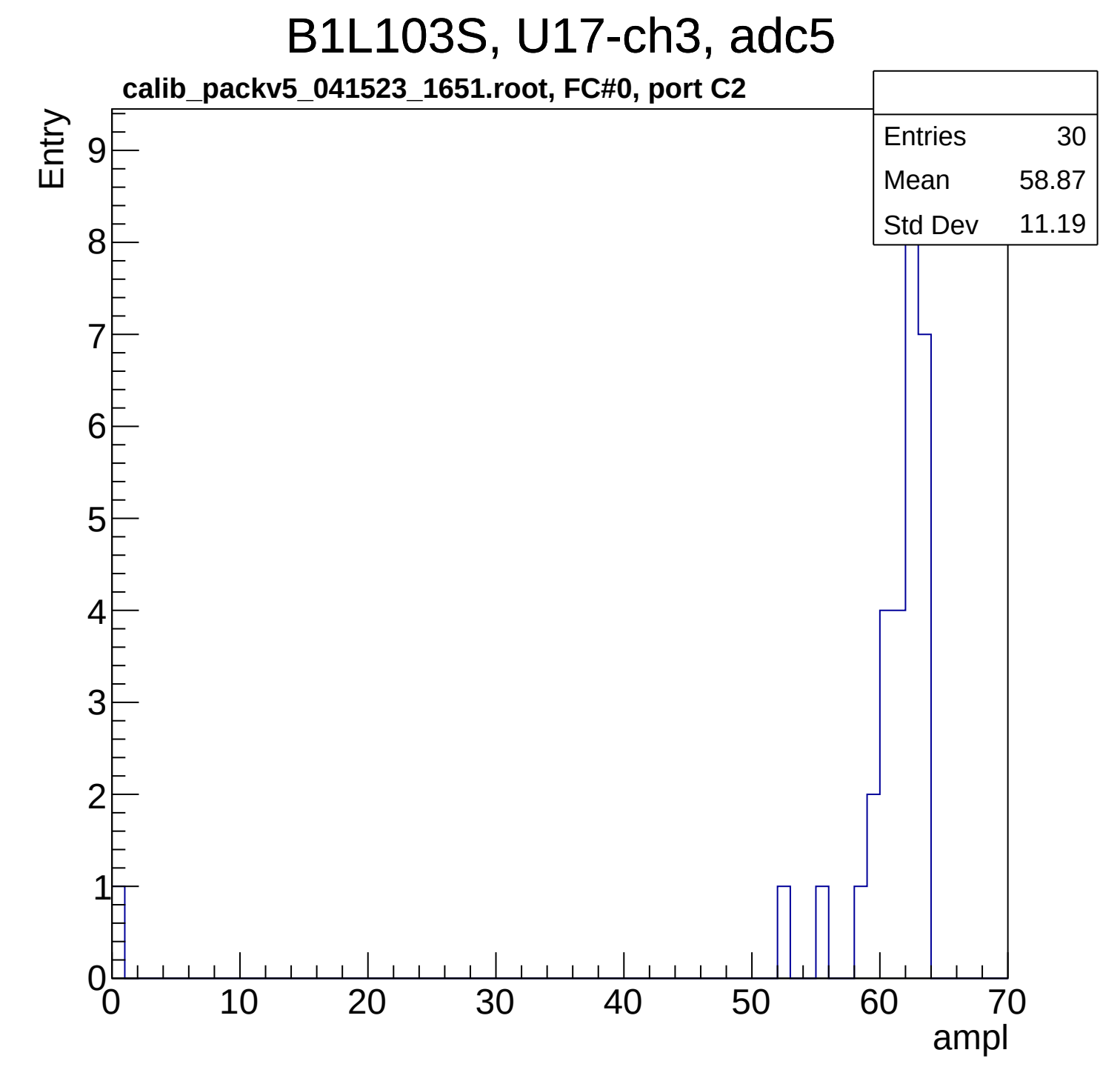

B1L103S, U17-ch3, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 26.8
Std Dev 11.76
Gaus mean : 32.0453
Gaus Width: 3.7514
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

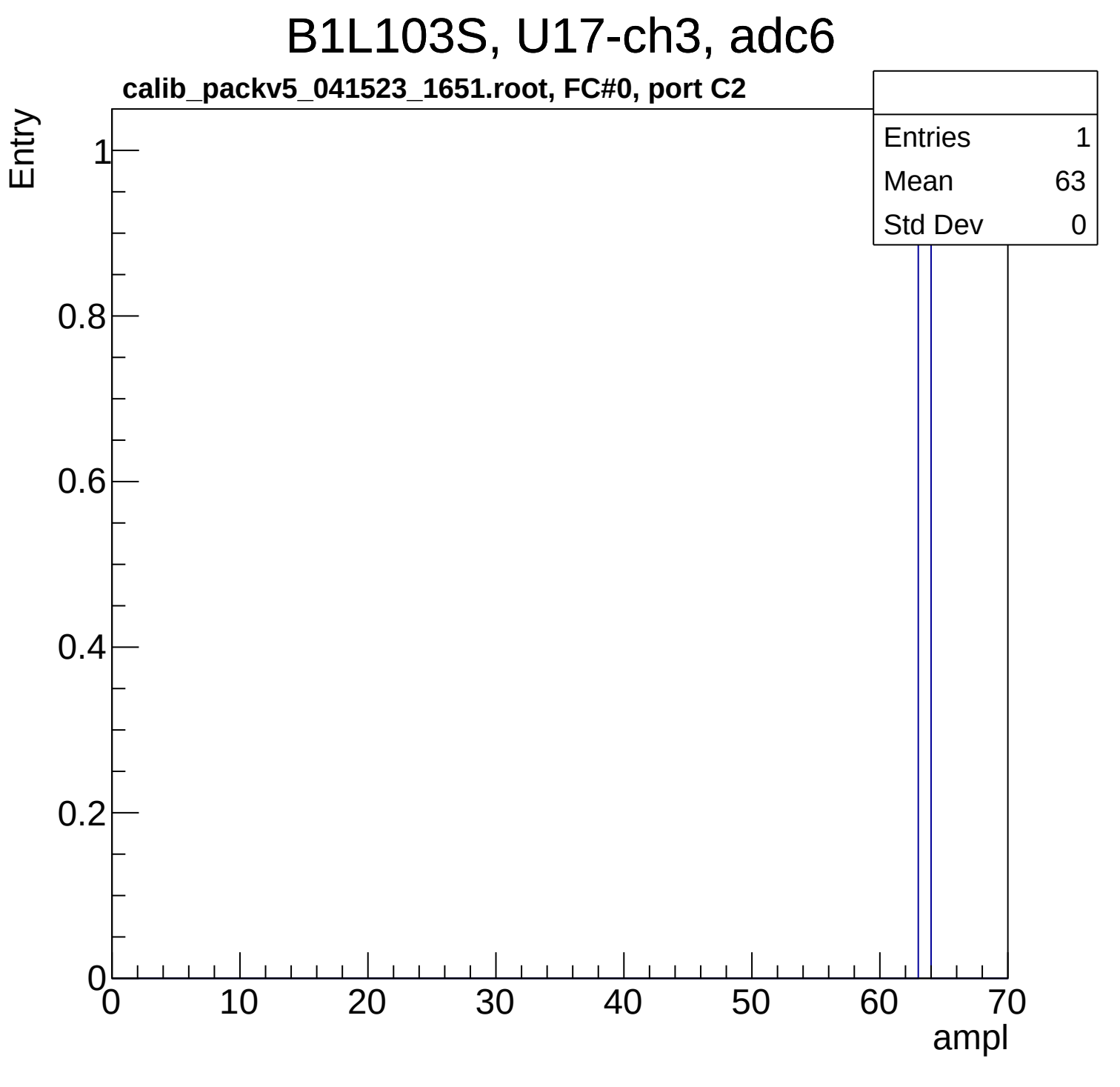

B1L103S, U17-ch3, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 38.5
Std Dev 3.331
Gaus mean : 38.1427
Gaus Width: 3.2532
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

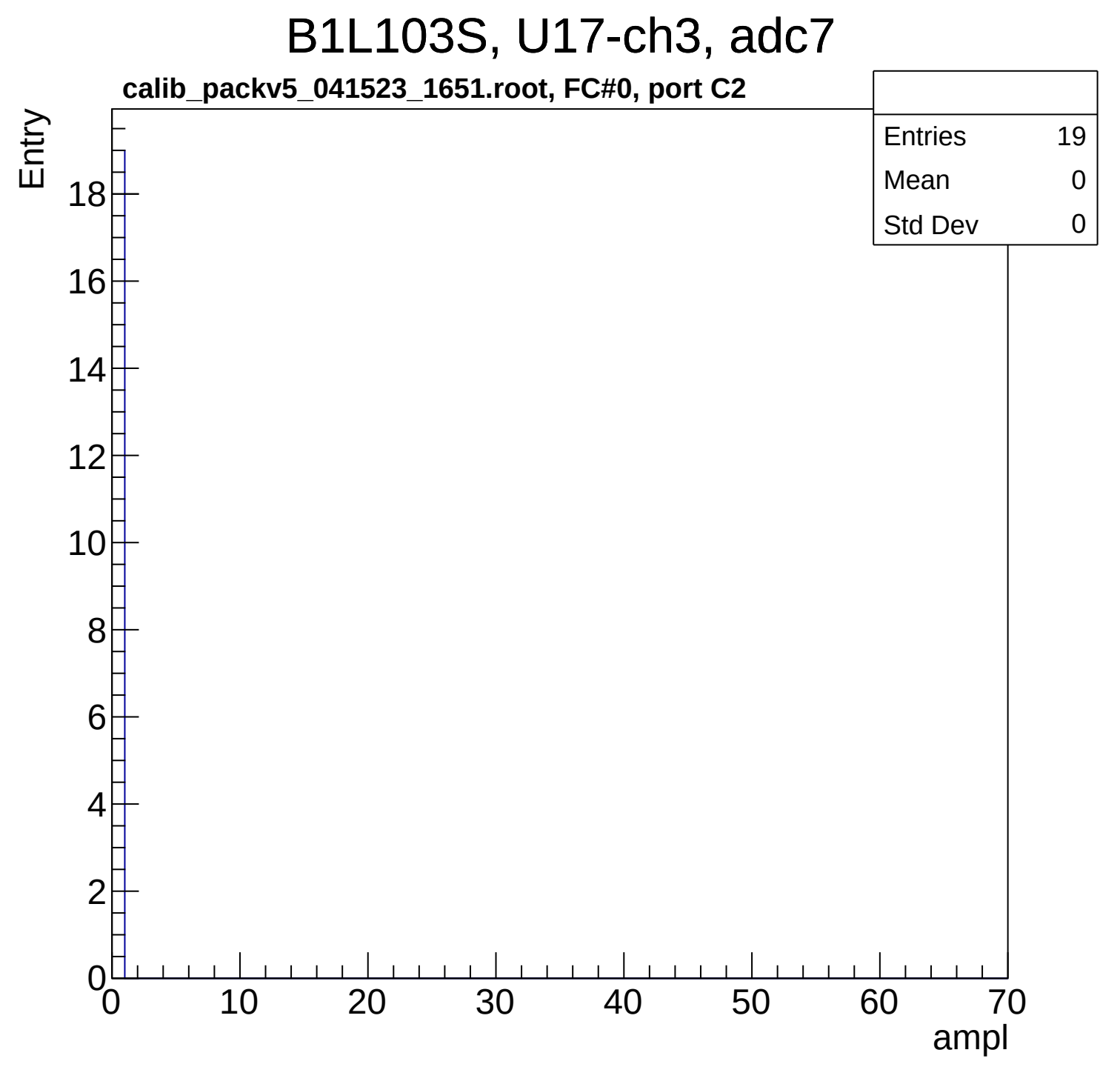

B1L103S, U17-ch3, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 38.9
Std Dev 15.73
Gaus mean : 45.9917
Gaus Width: 4.5064
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

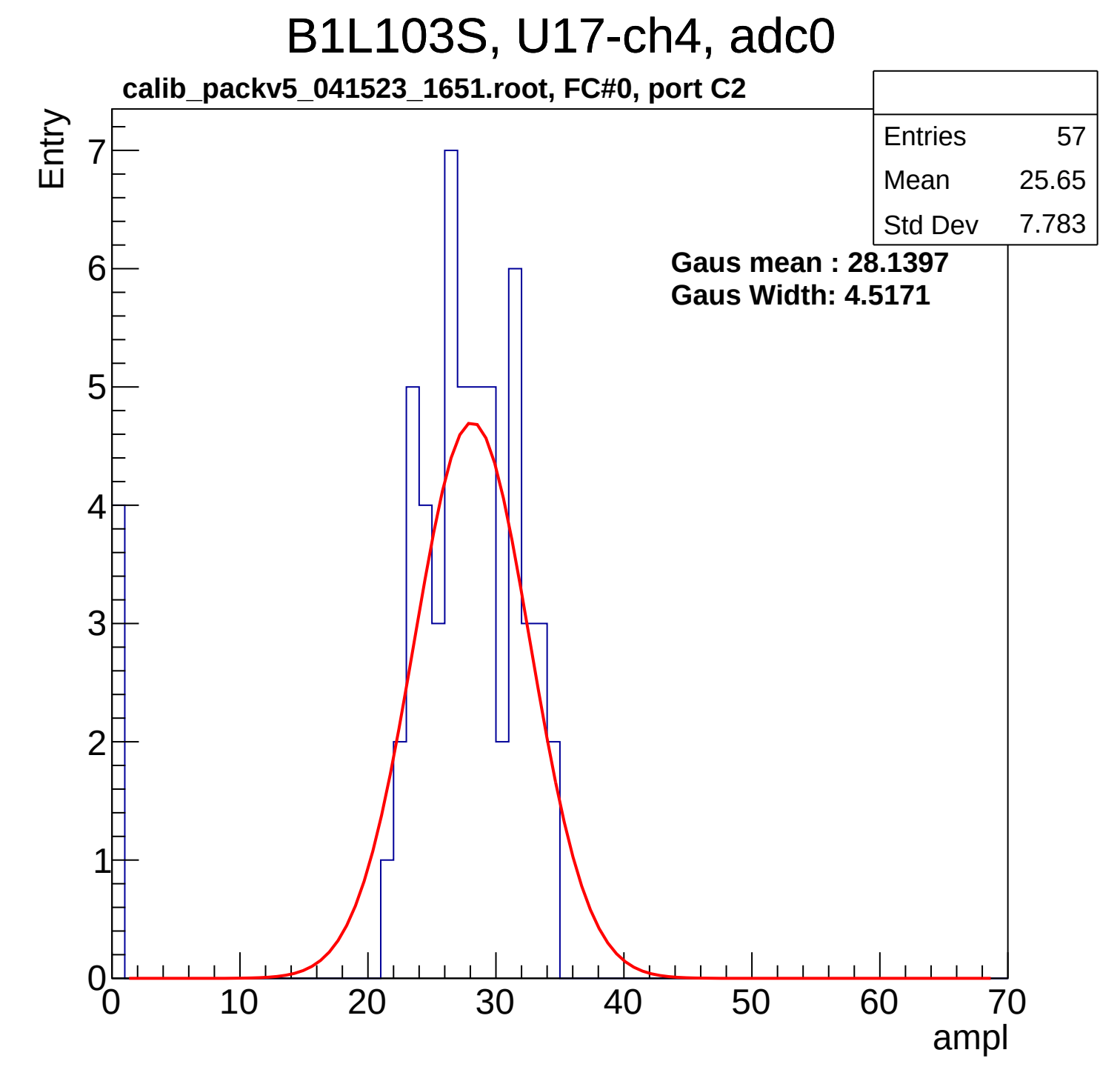

B1L103S, U17-ch3, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 48.75
Std Dev 11.69
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

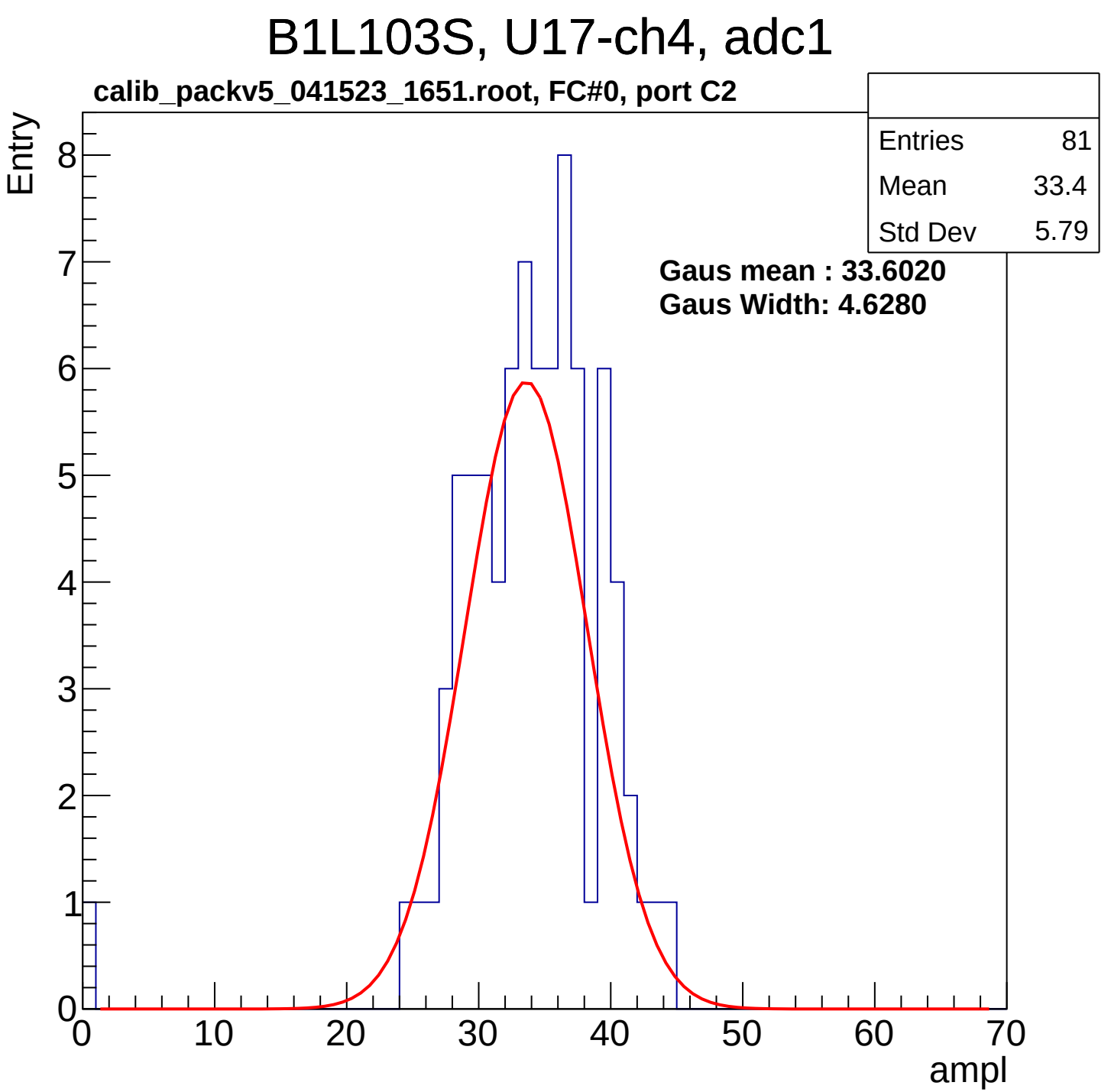

B1L103S, U17-ch3, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 57.24
Std Dev 2.917
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

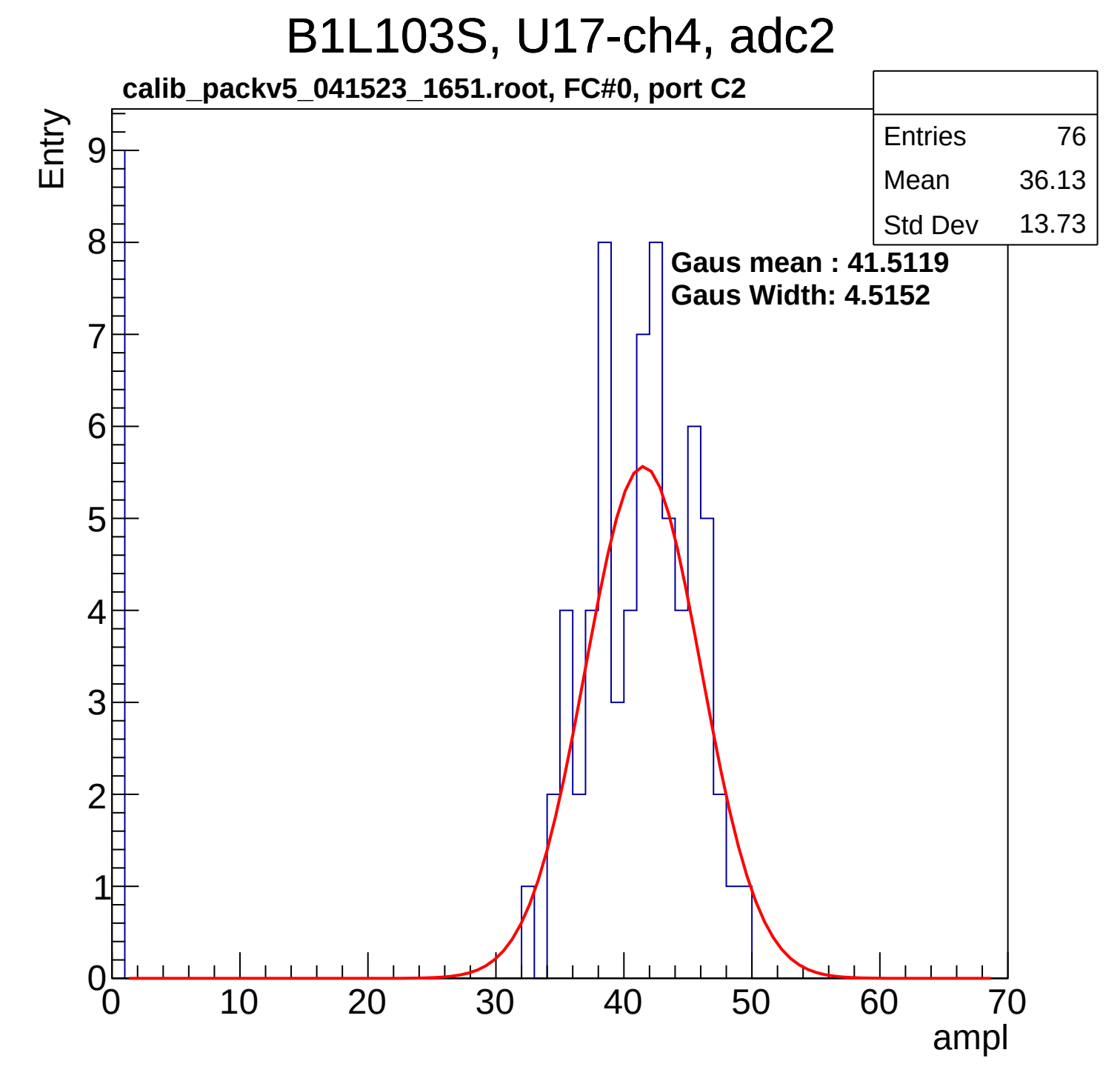

B1L103S, U17-ch3, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 58.87
Std Dev 11.19
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

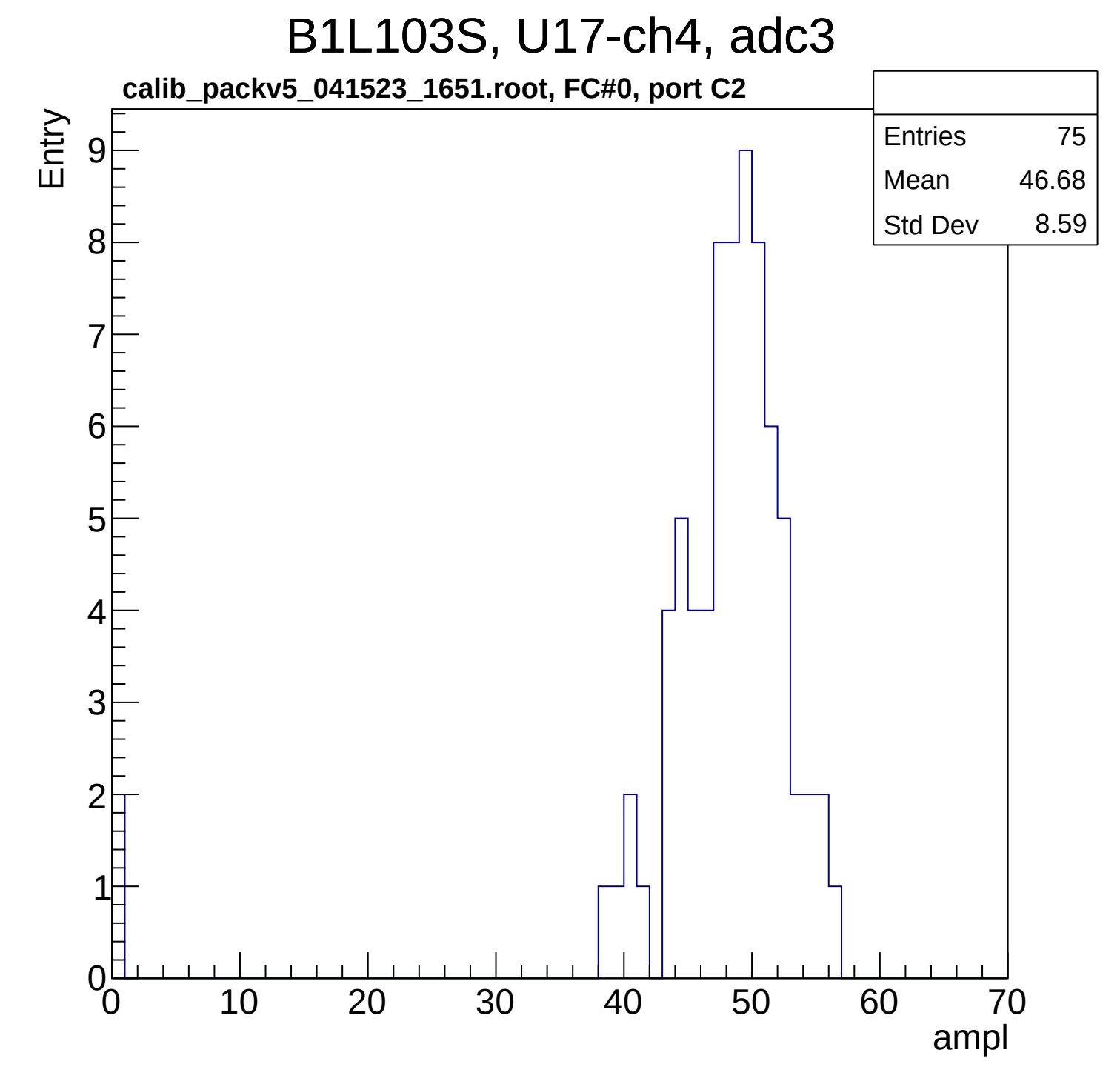

B1L103S, U17-ch3, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

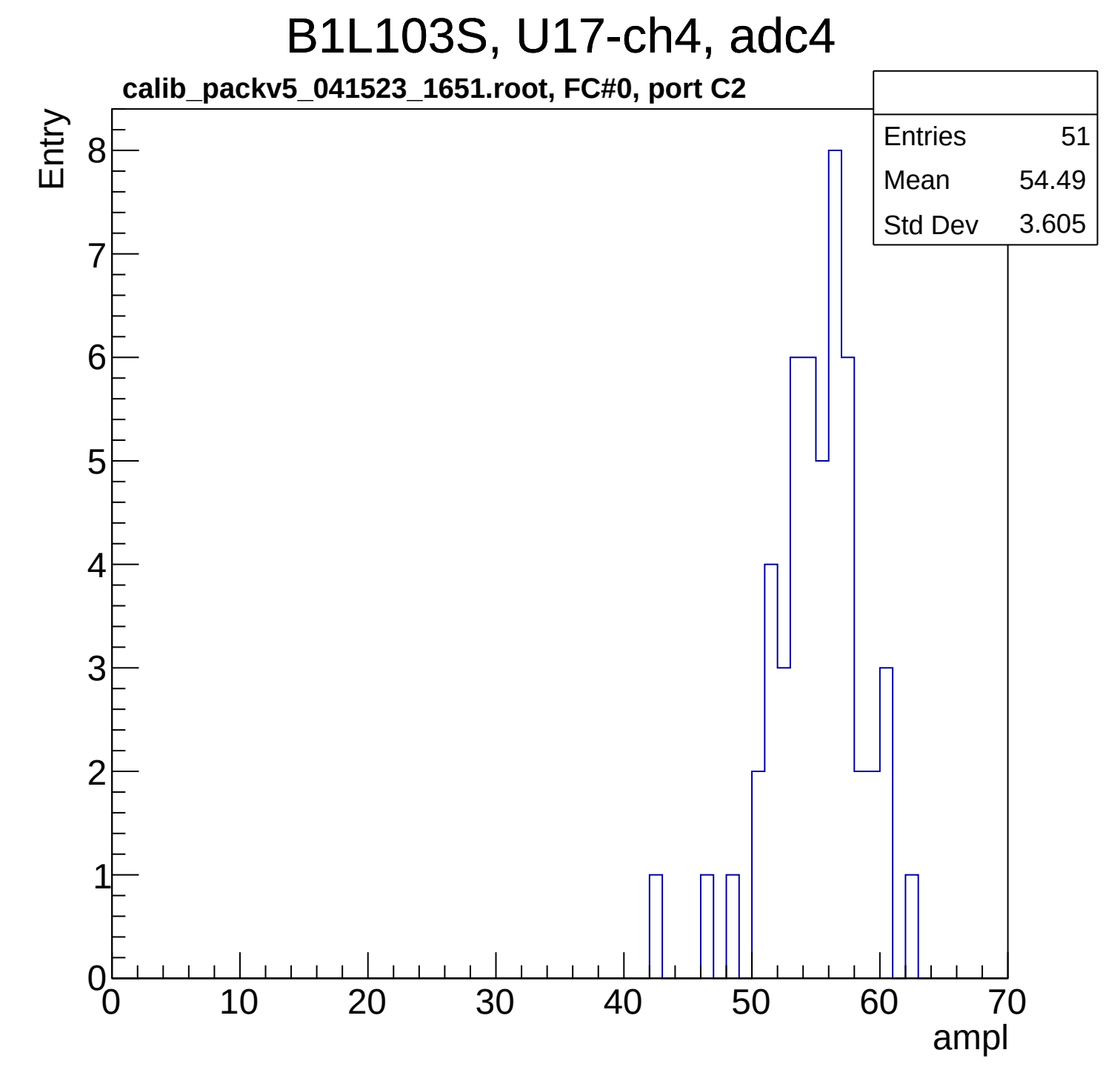

B1L103S, U17-ch3, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

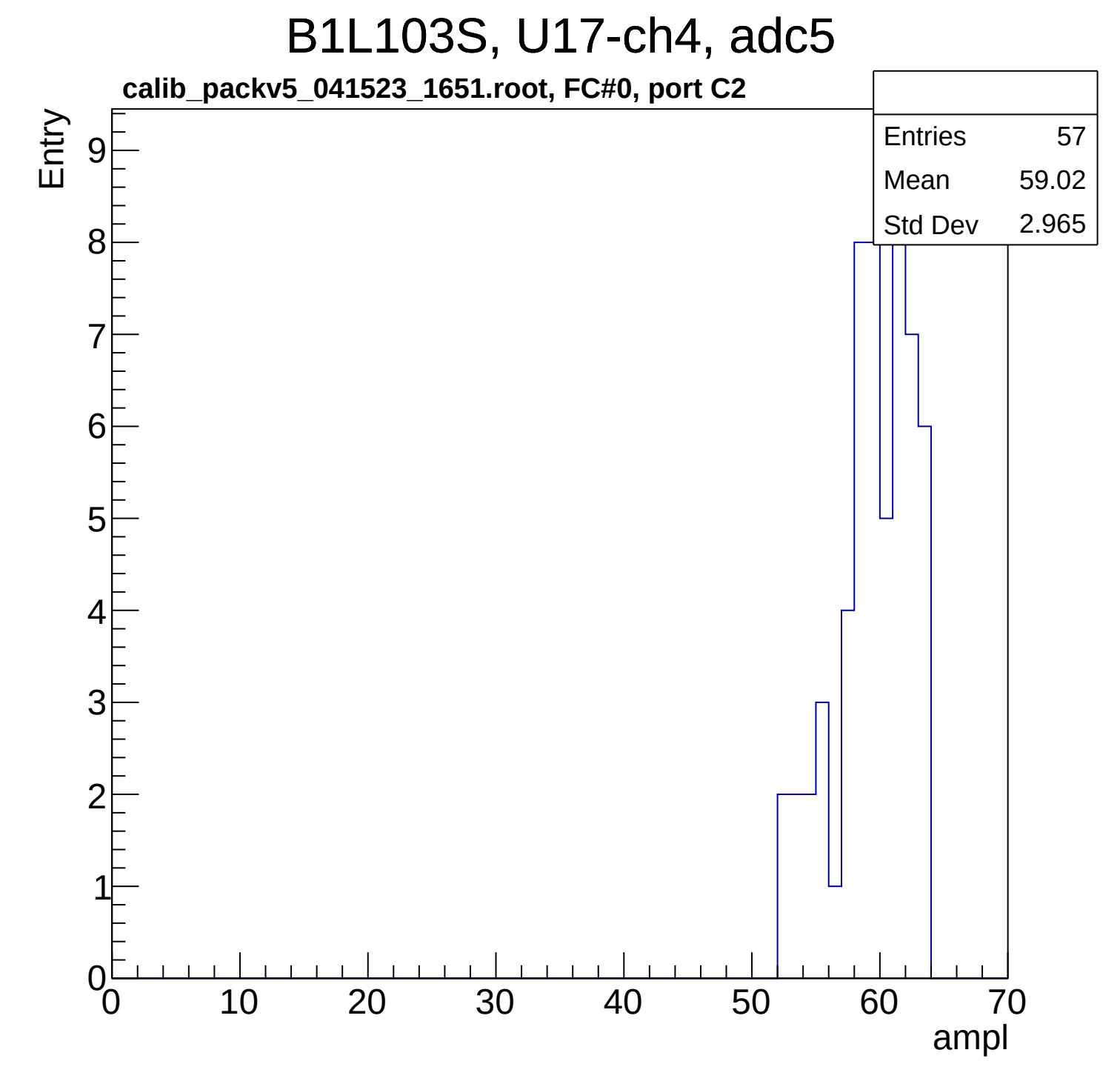

B1L103S, U17-ch4, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 25.65
Std Dev 7.783
Gaus mean : 28.1397
Gaus Width: 4.5171
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

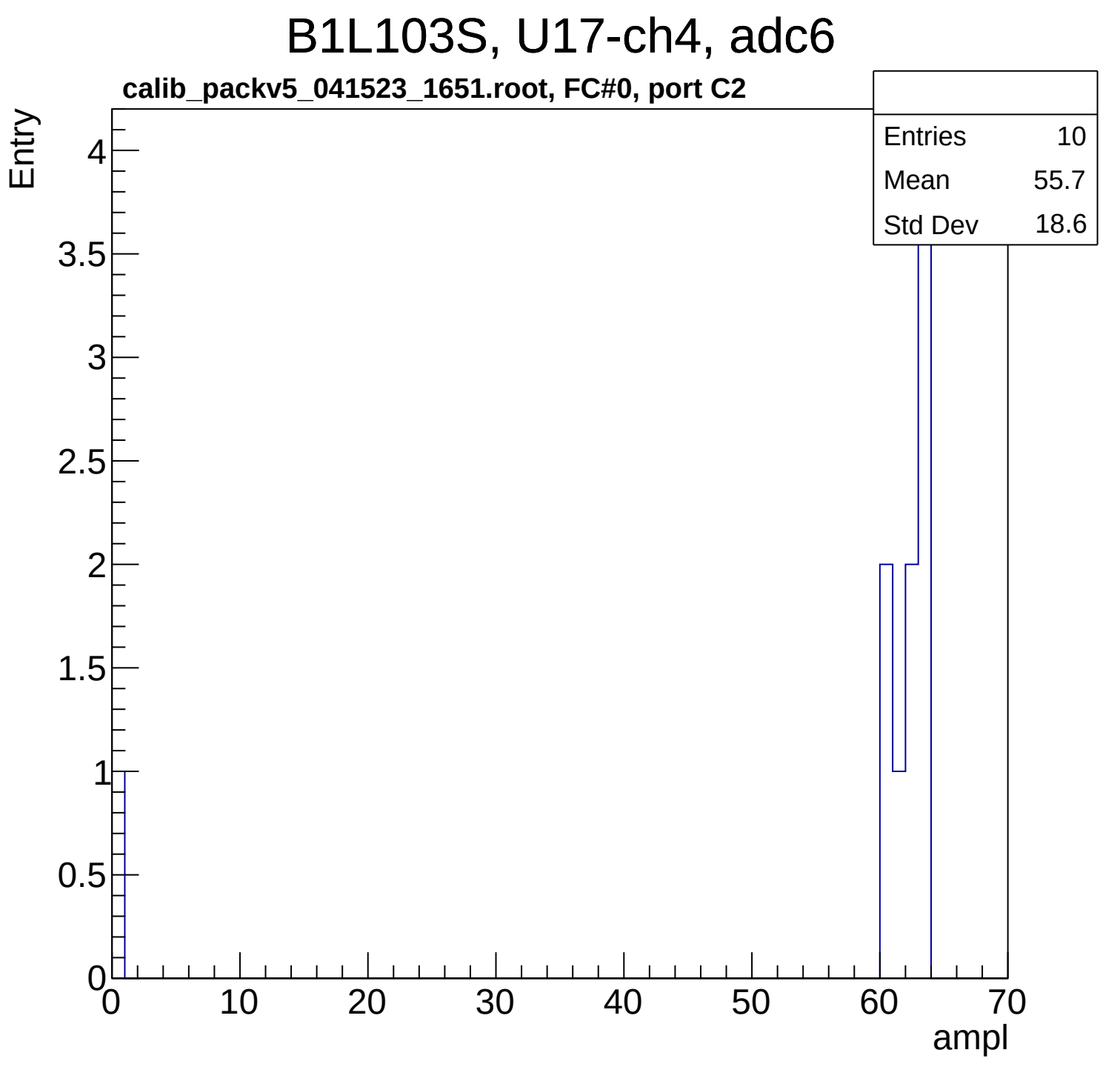

B1L103S, U17-ch4, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 33.4
Std Dev 5.79
Gaus mean : 33.6020
Gaus Width: 4.6280
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

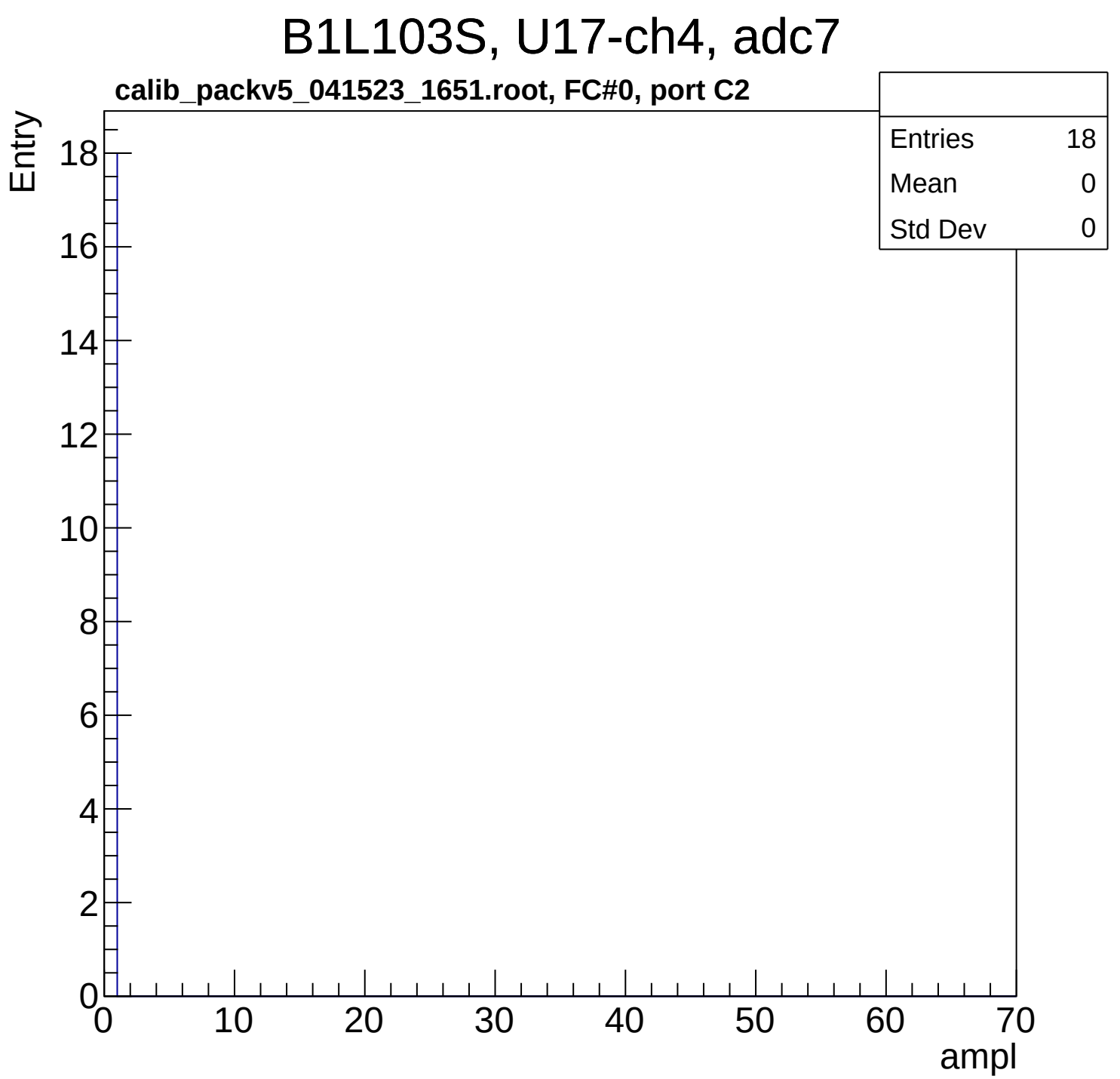

B1L103S, U17-ch4, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 36.13
Std Dev 13.73
Gaus mean : 41.5119
Gaus Width: 4.5152
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

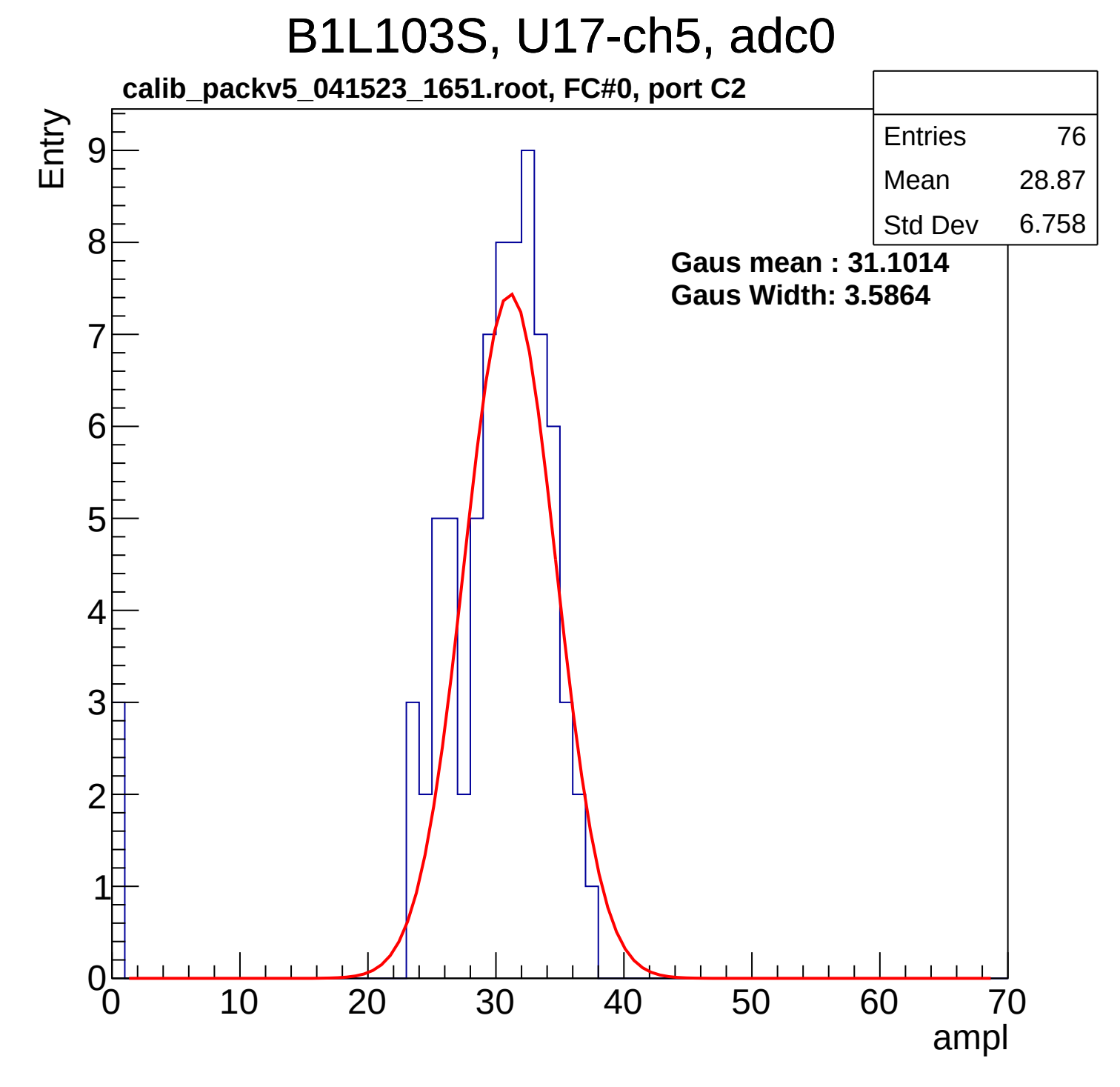

B1L103S, U17-ch4, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 46.68
Std Dev 8.59
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

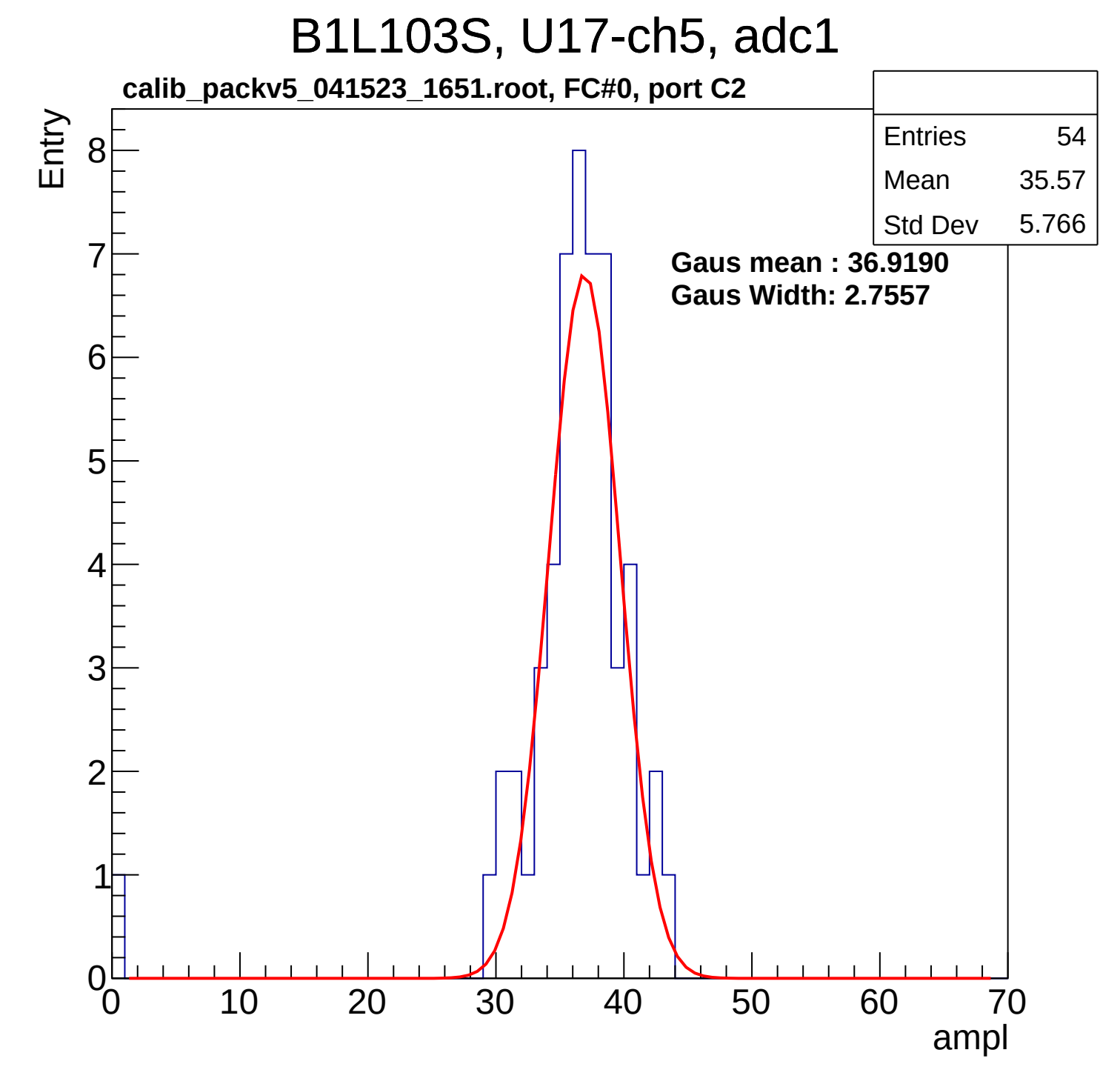

B1L103S, U17-ch4, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 54.49
Std Dev 3.605
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

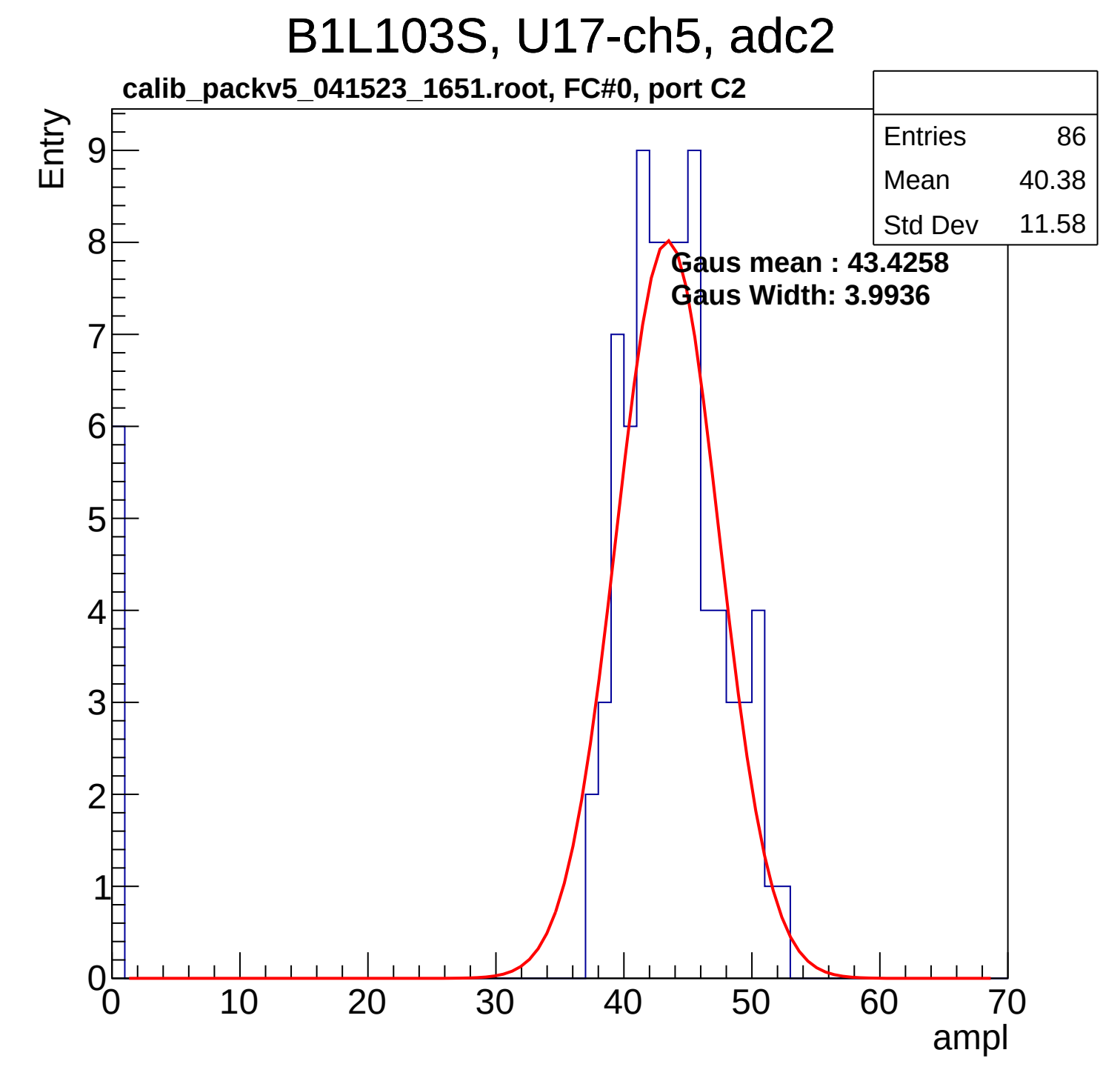

B1L103S, U17-ch4, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 59.02
Std Dev 2.965
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

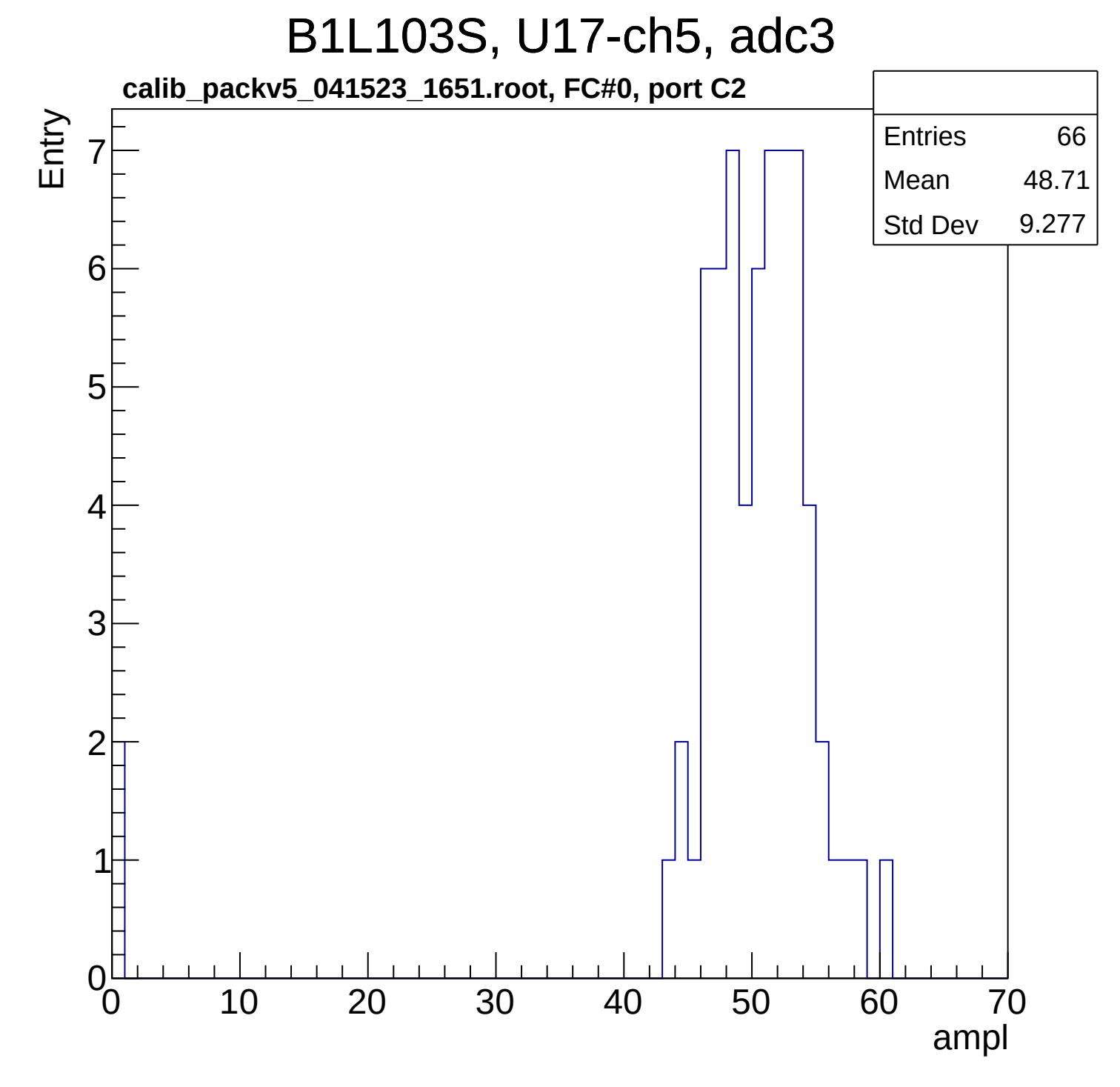

B1L103S, U17-ch4, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.7
Std Dev 18.6
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

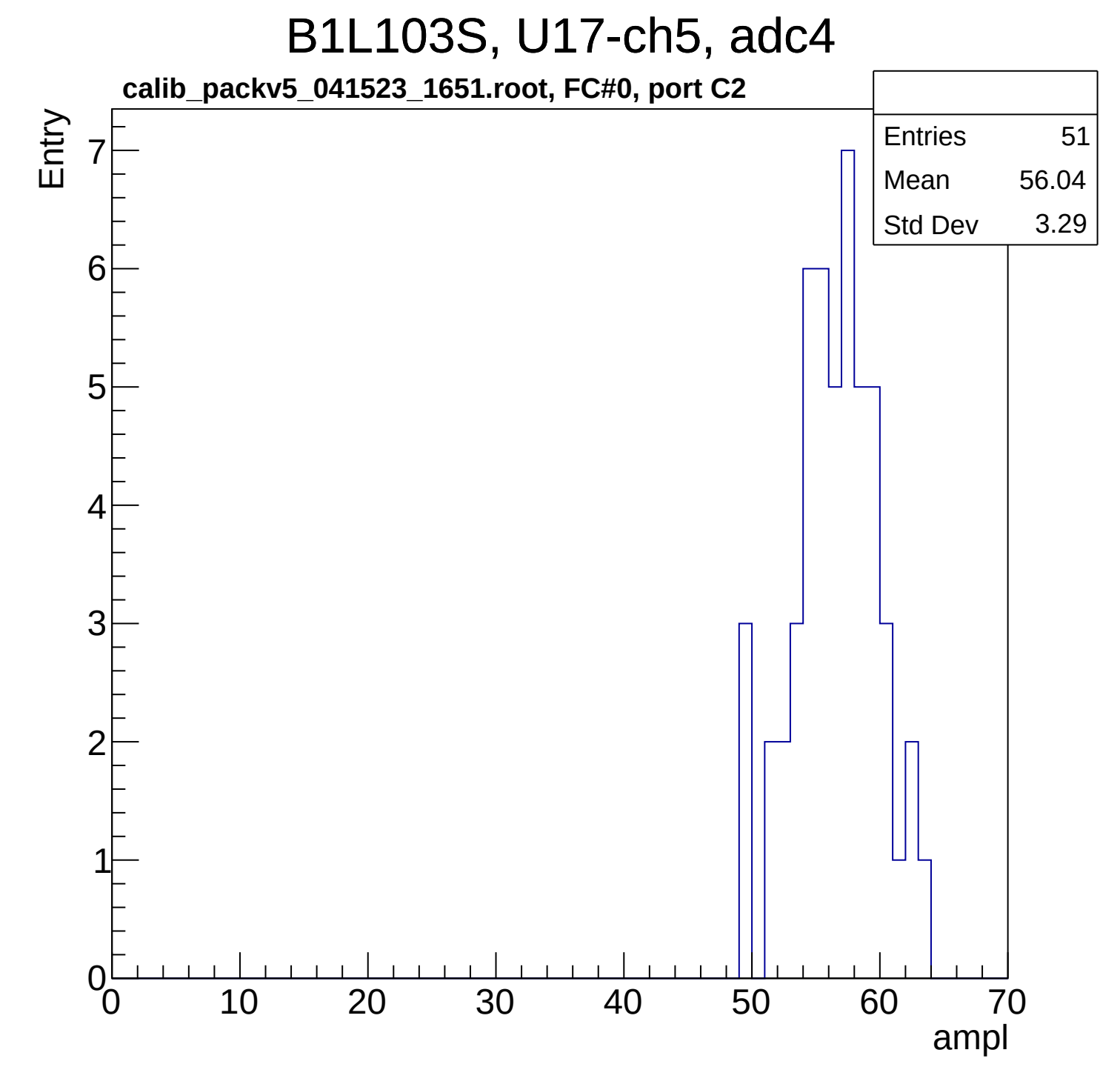

B1L103S, U17-ch4, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

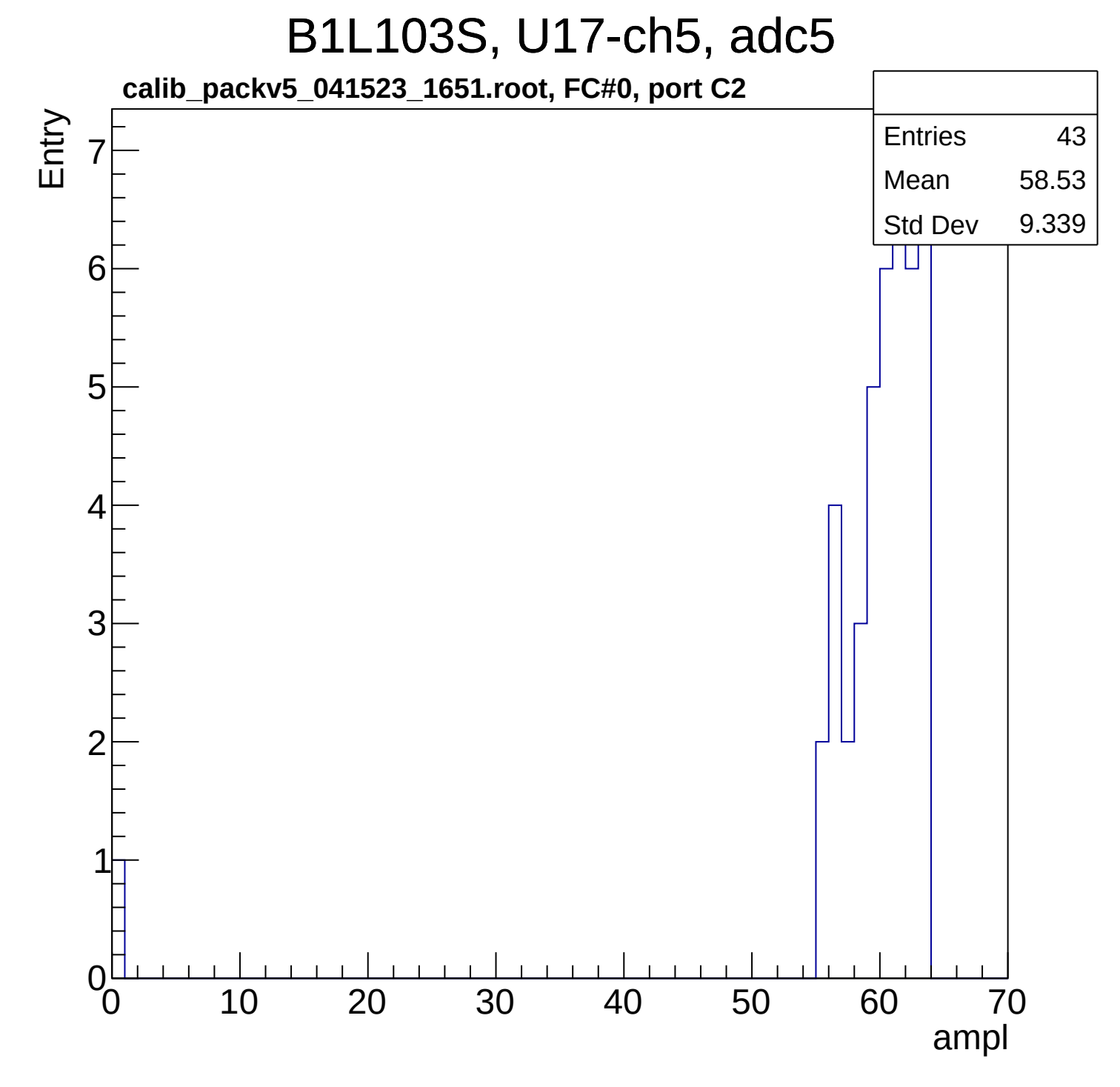

B1L103S, U17-ch5, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 28.87
Std Dev 6.758
Gaus mean : 31.1014
Gaus Width: 3.5864
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

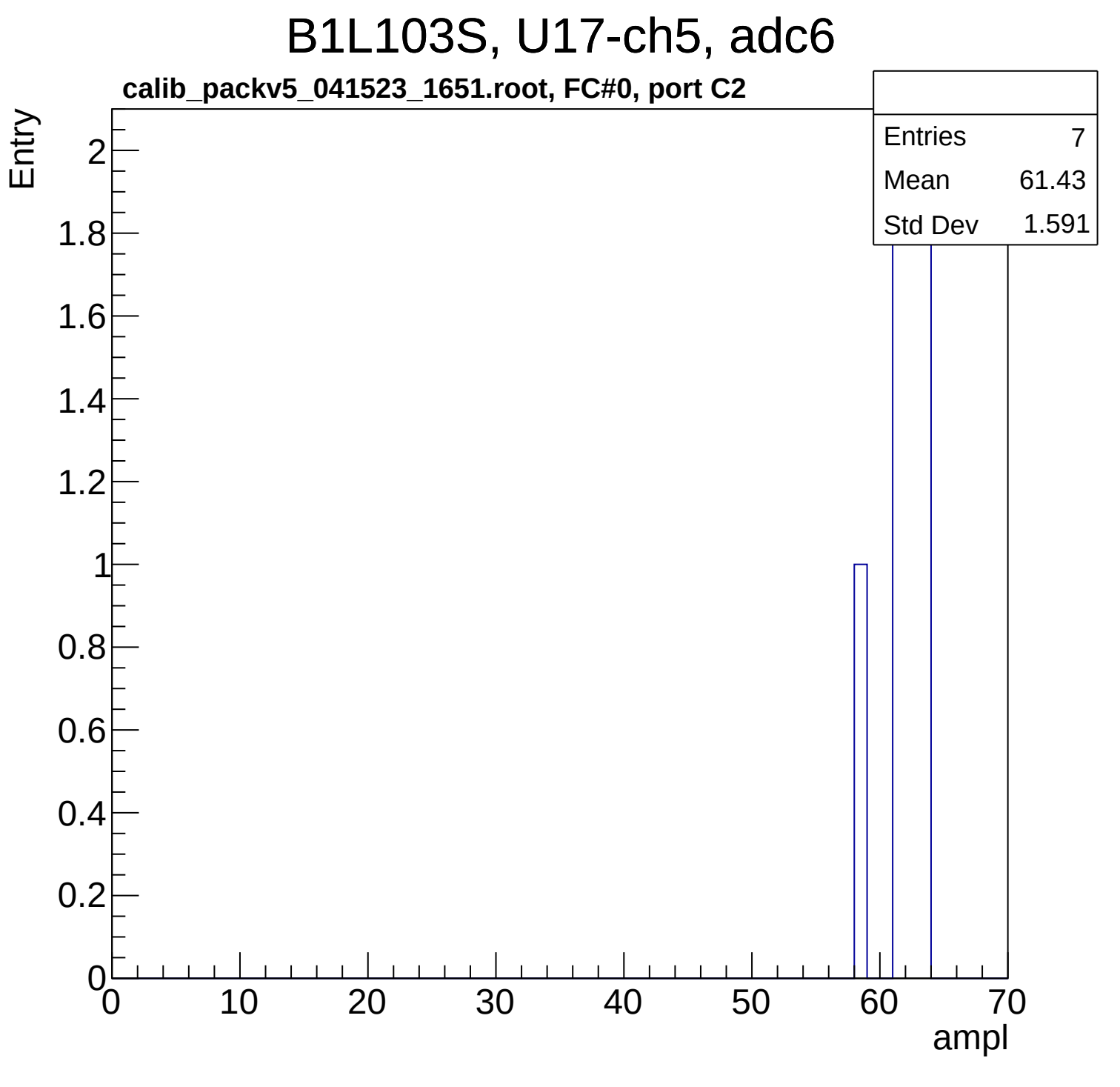

B1L103S, U17-ch5, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 35.57
Std Dev 5.766
Gaus mean : 36.9190
Gaus Width: 2.7557
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

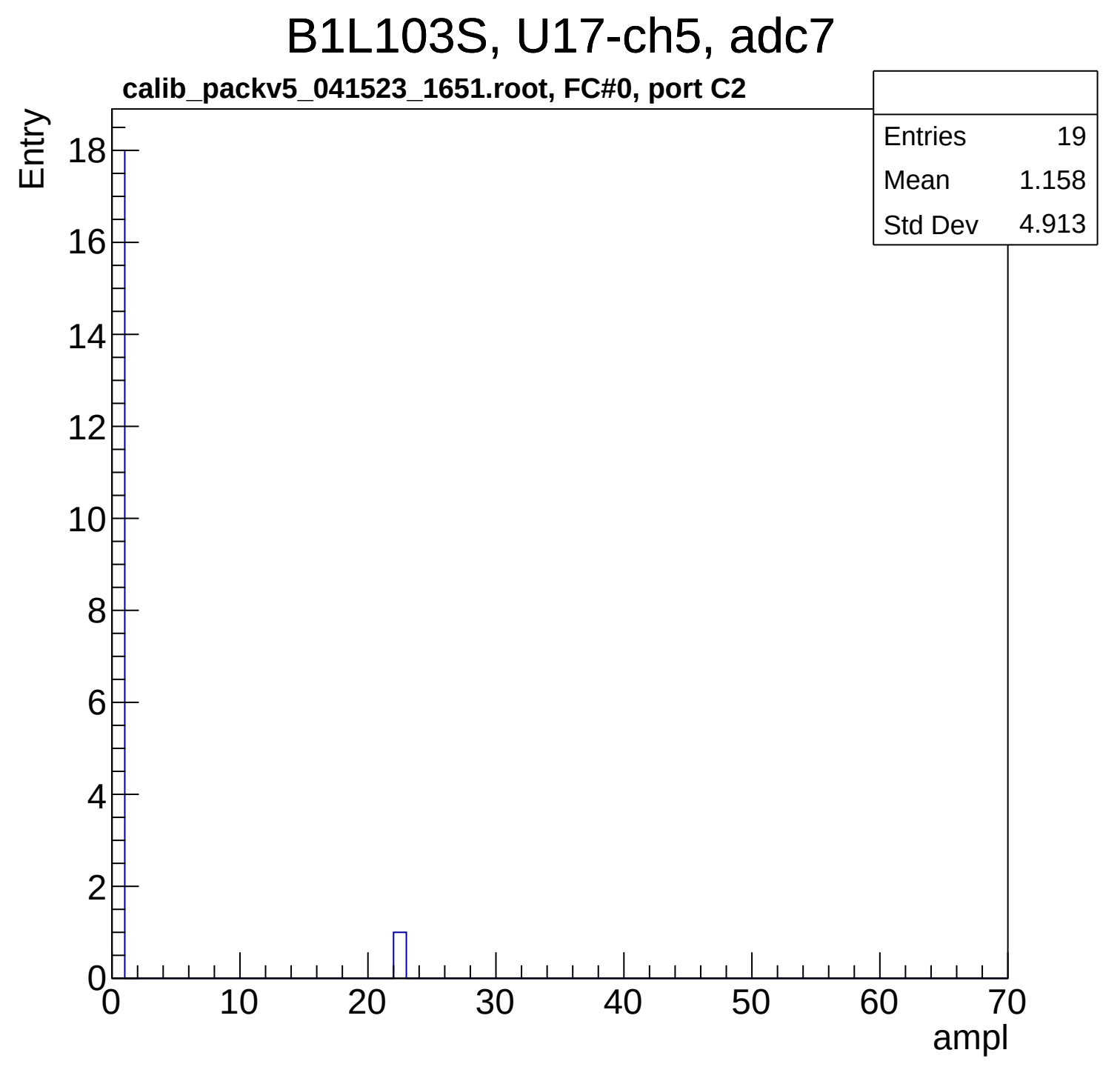

B1L103S, U17-ch5, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 40.38
Std Dev 11.58
Gaus mean : 43.4258
Gaus Width: 3.9936
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

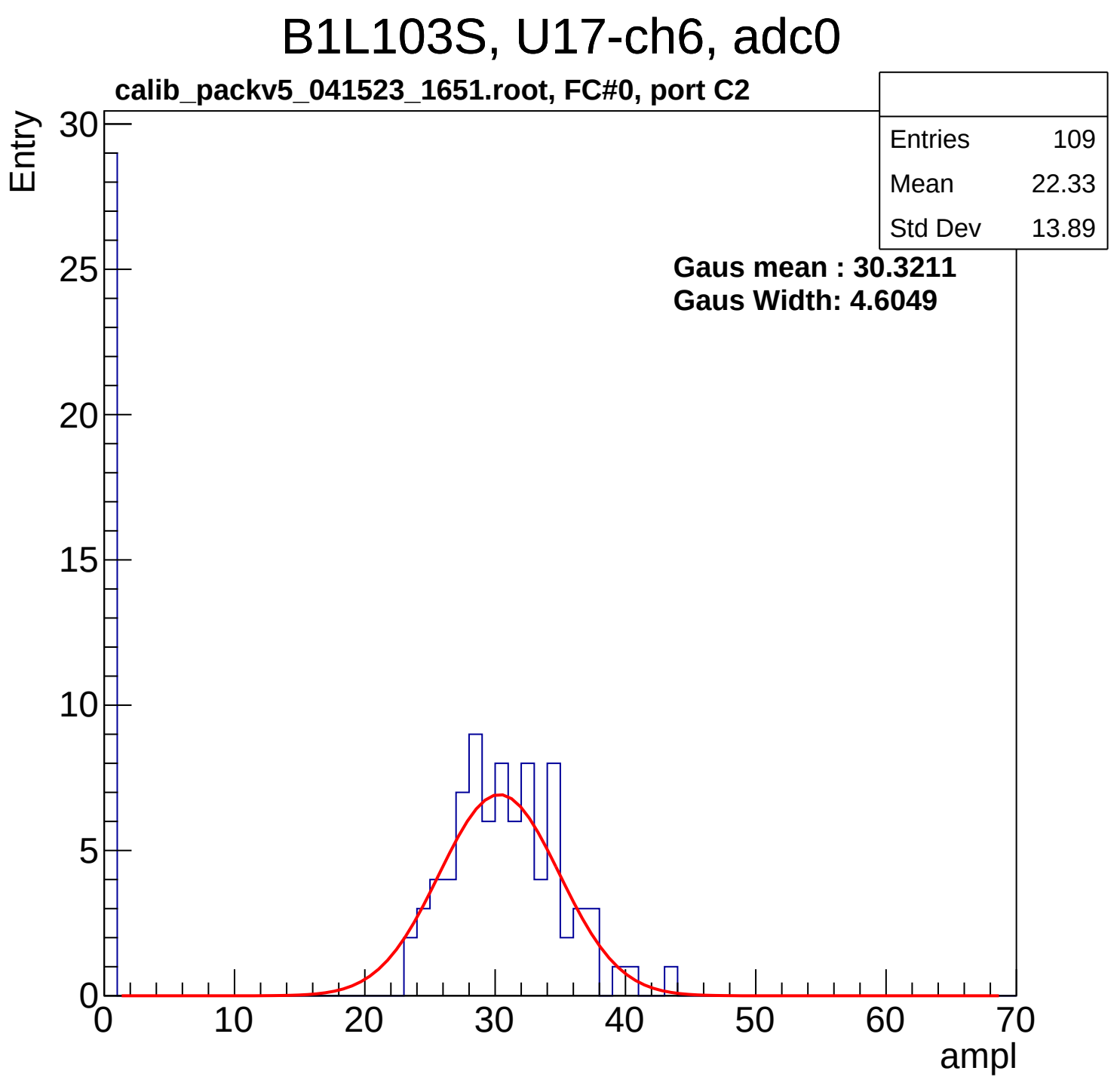

B1L103S, U17-ch5, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 48.71
Std Dev 9.277
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

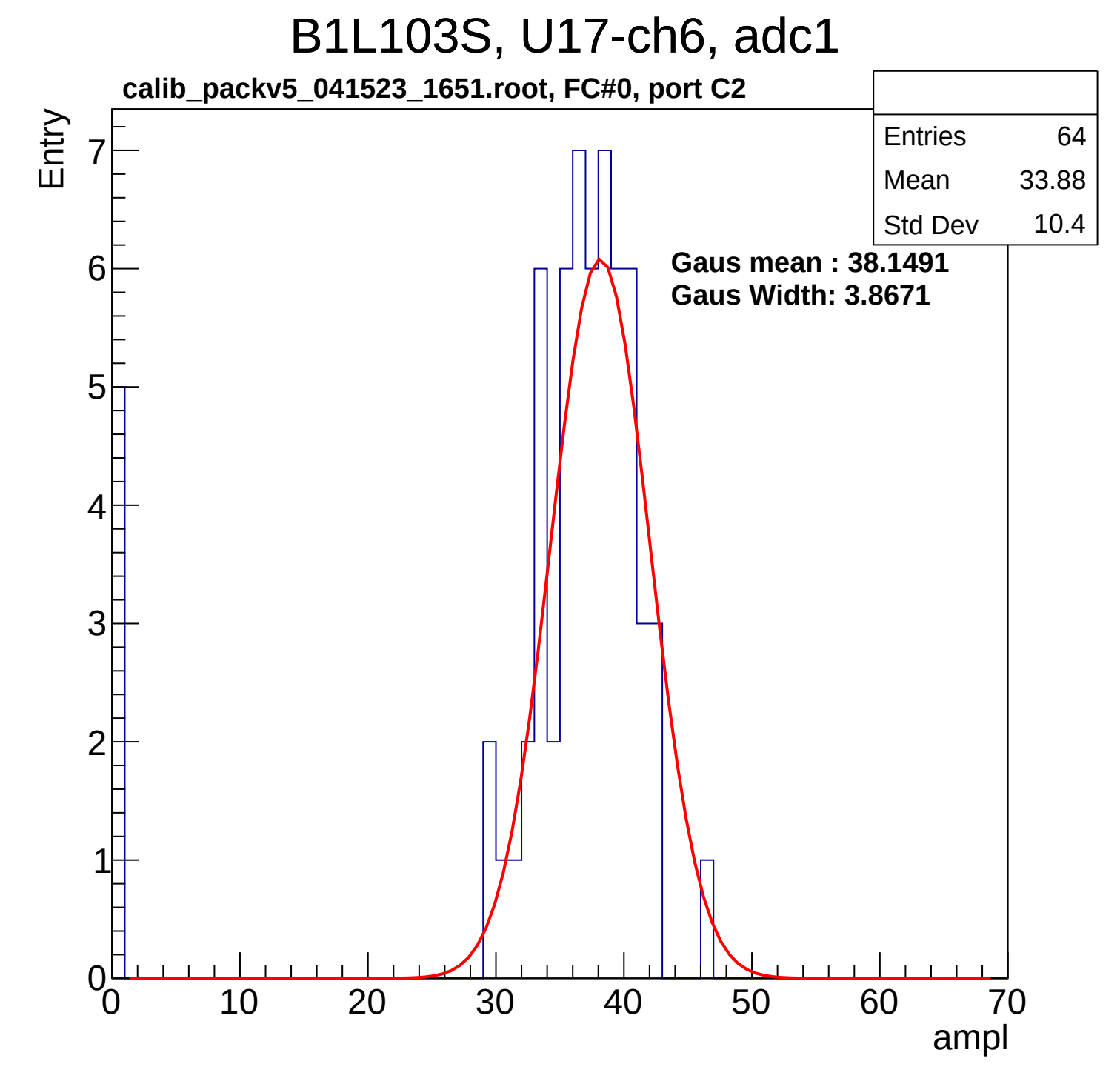

B1L103S, U17-ch5, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 56.04
Std Dev 3.29
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

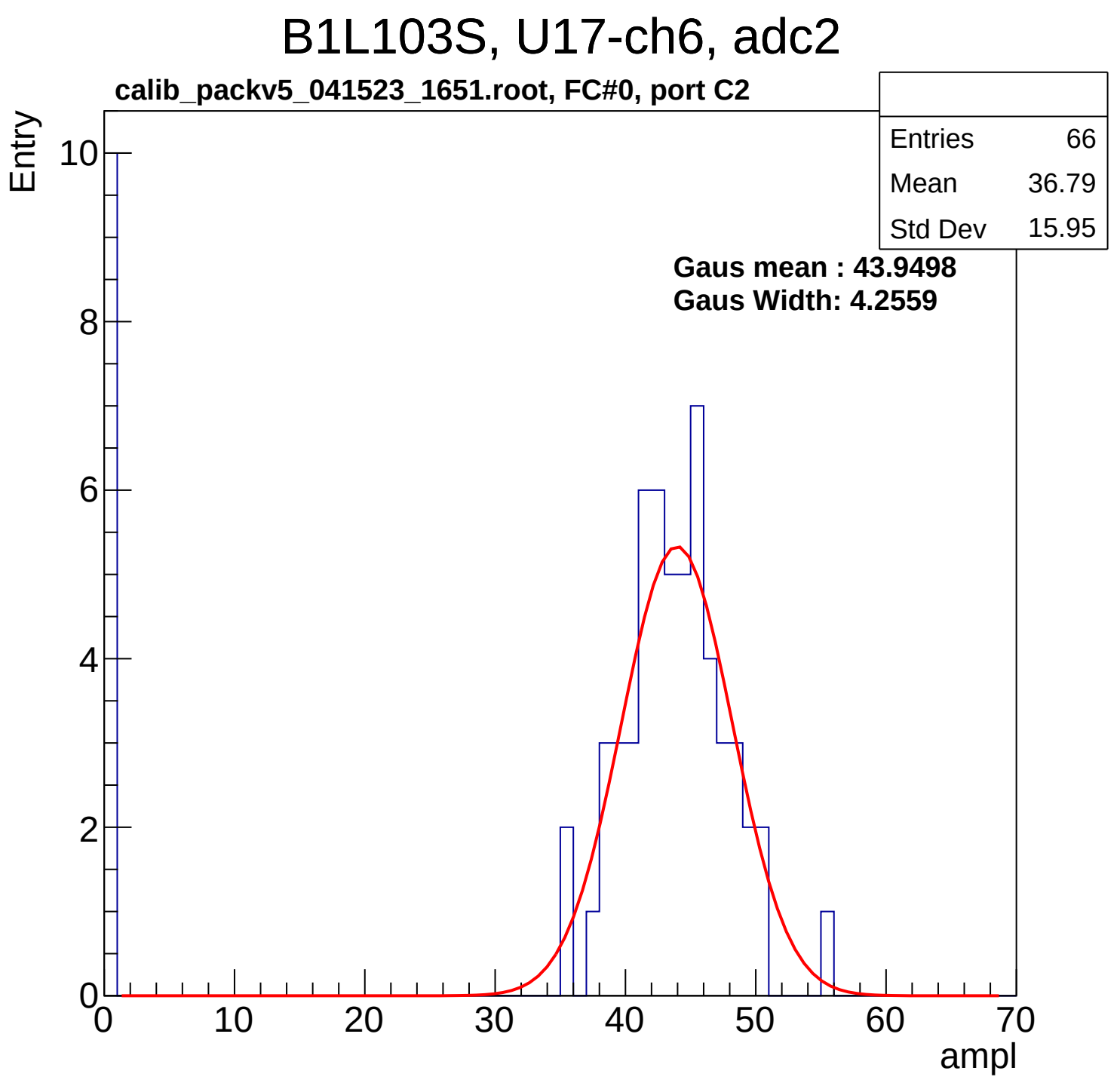

B1L103S, U17-ch5, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 58.53
Std Dev 9.339
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

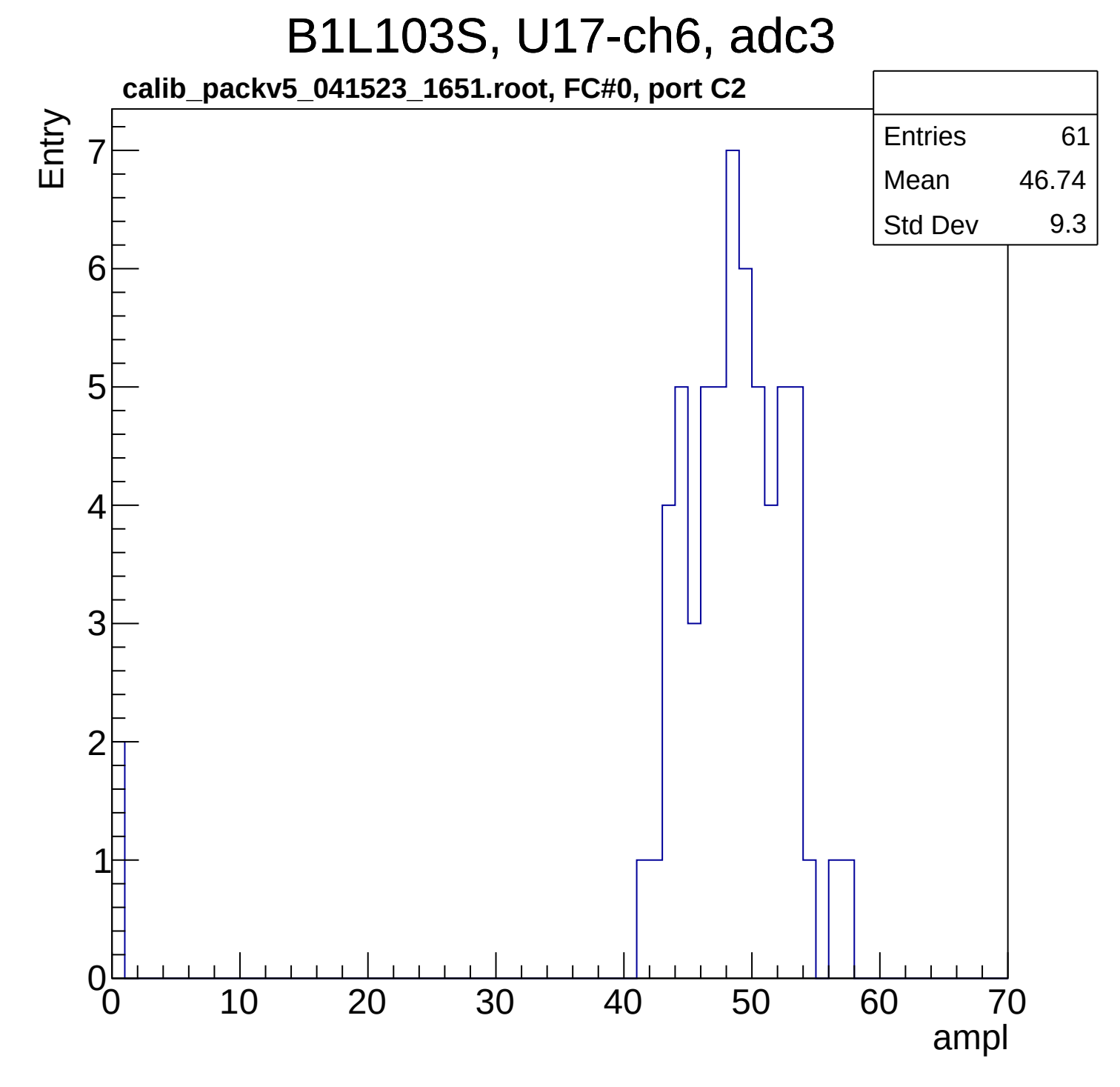

B1L103S, U17-ch5, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.43
Std Dev 1.591
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

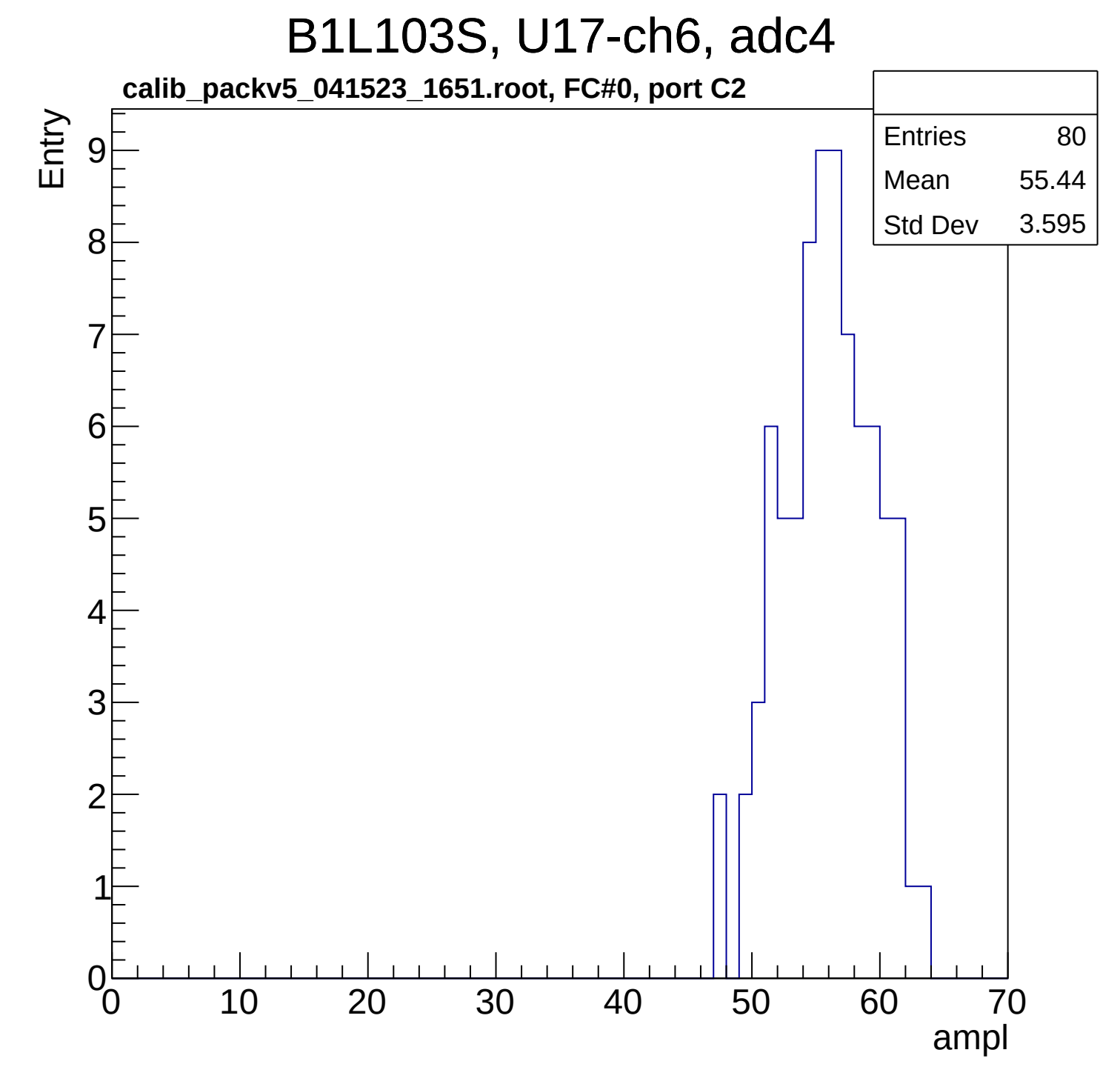

B1L103S, U17-ch5, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

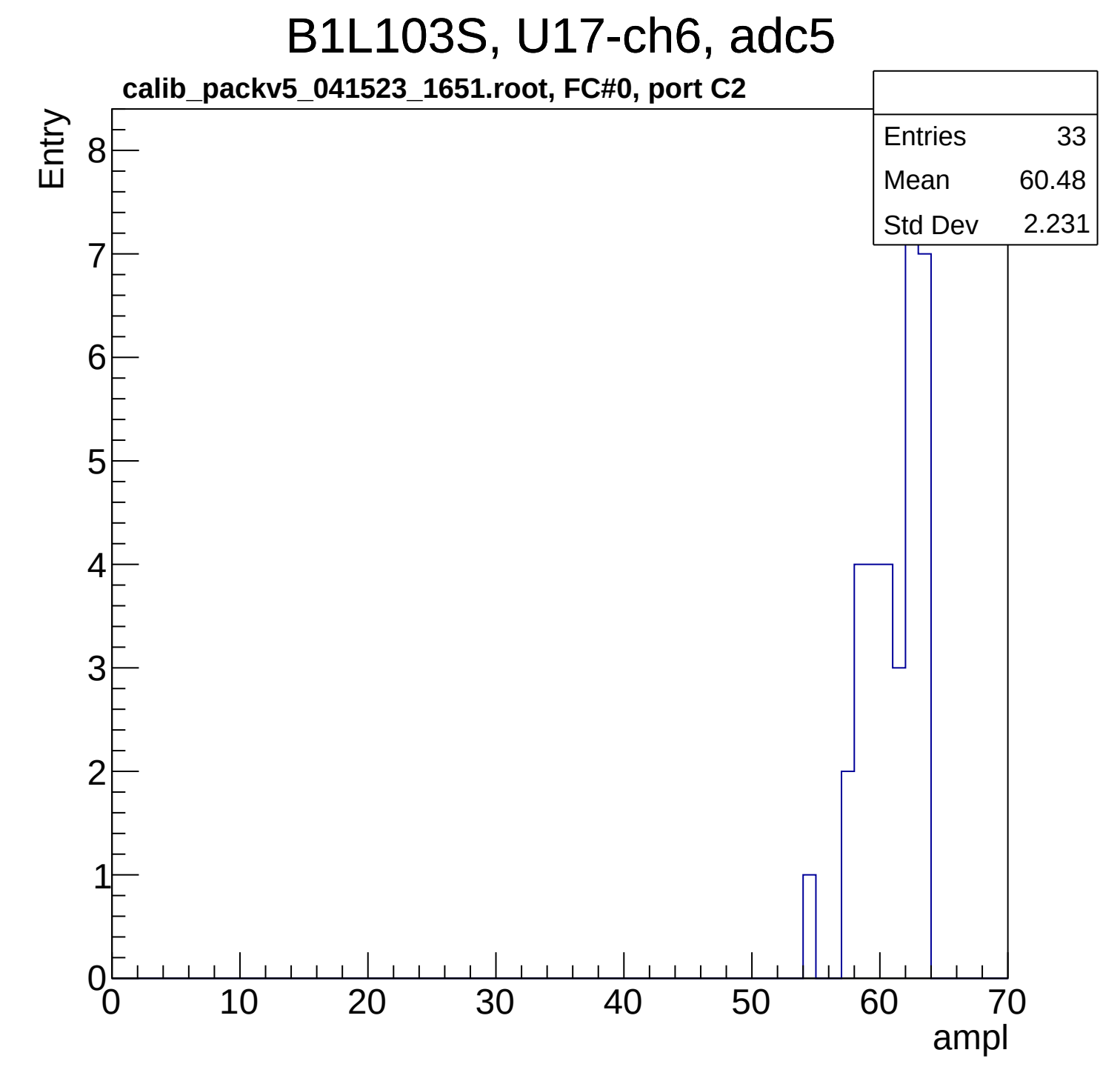

B1L103S, U17-ch6, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 109
Mean 22.33
Std Dev 13.89
Gaus mean : 30.3211
Gaus Width: 4.6049
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70

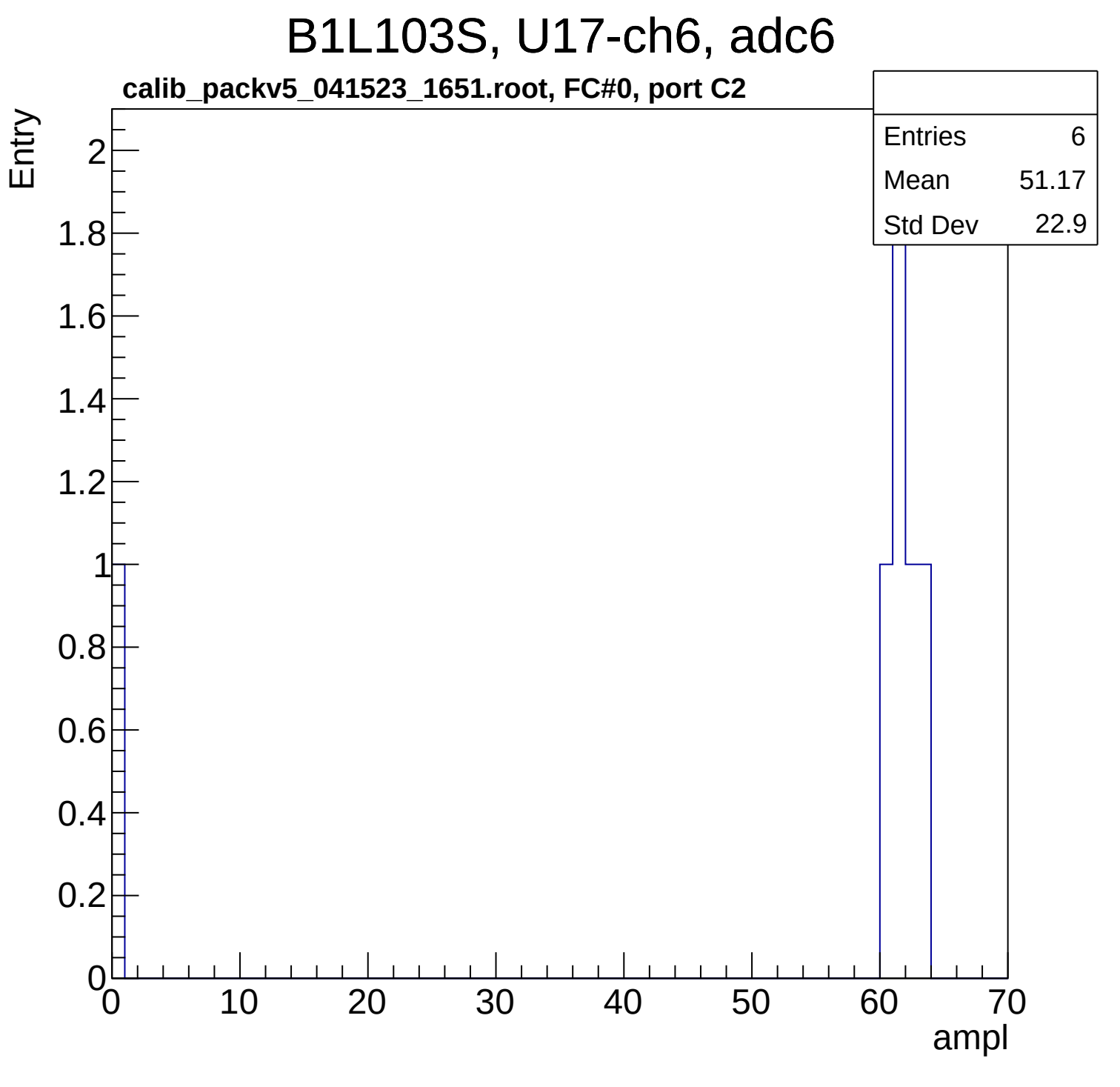

B1L103S, U17-ch6, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 33.88
Std Dev 10.4
Gaus mean : 38.1491
Gaus Width: 3.8671
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

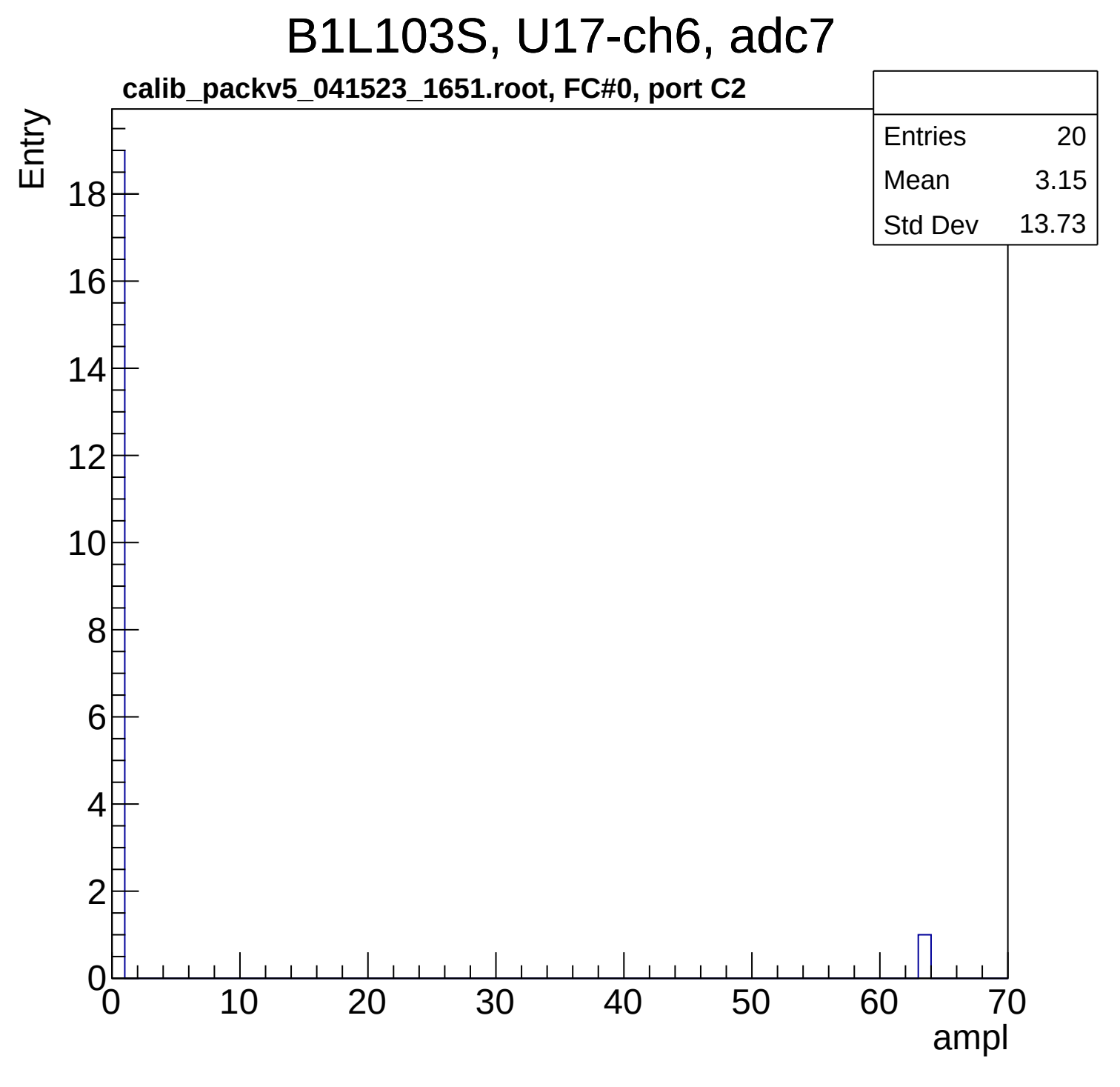

B1L103S, U17-ch6, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 36.79
Std Dev 15.95
Gaus mean : 43.9498
Gaus Width: 4.2559
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

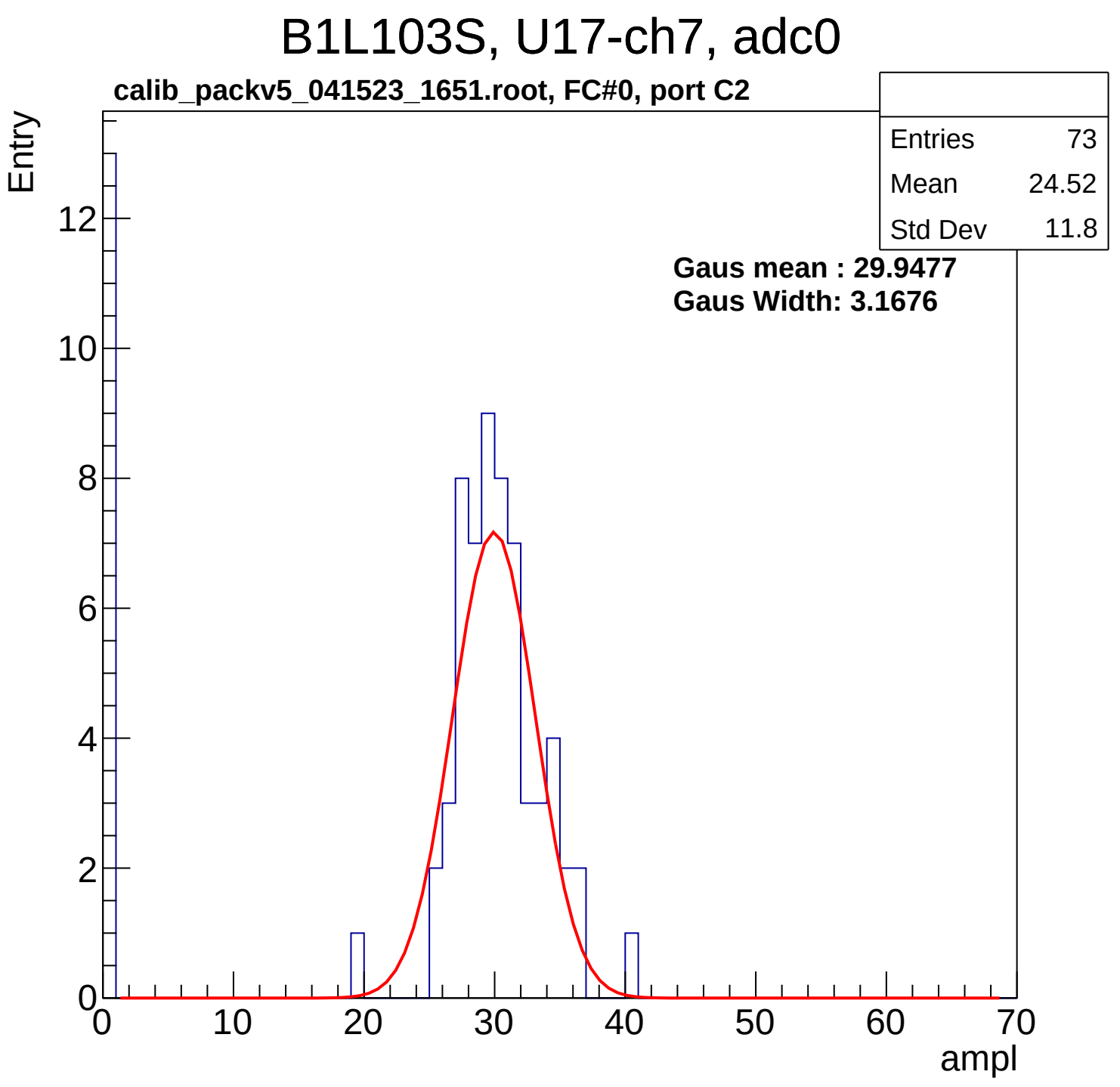

B1L103S, U17-ch6, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 46.74
Std Dev 9.3
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

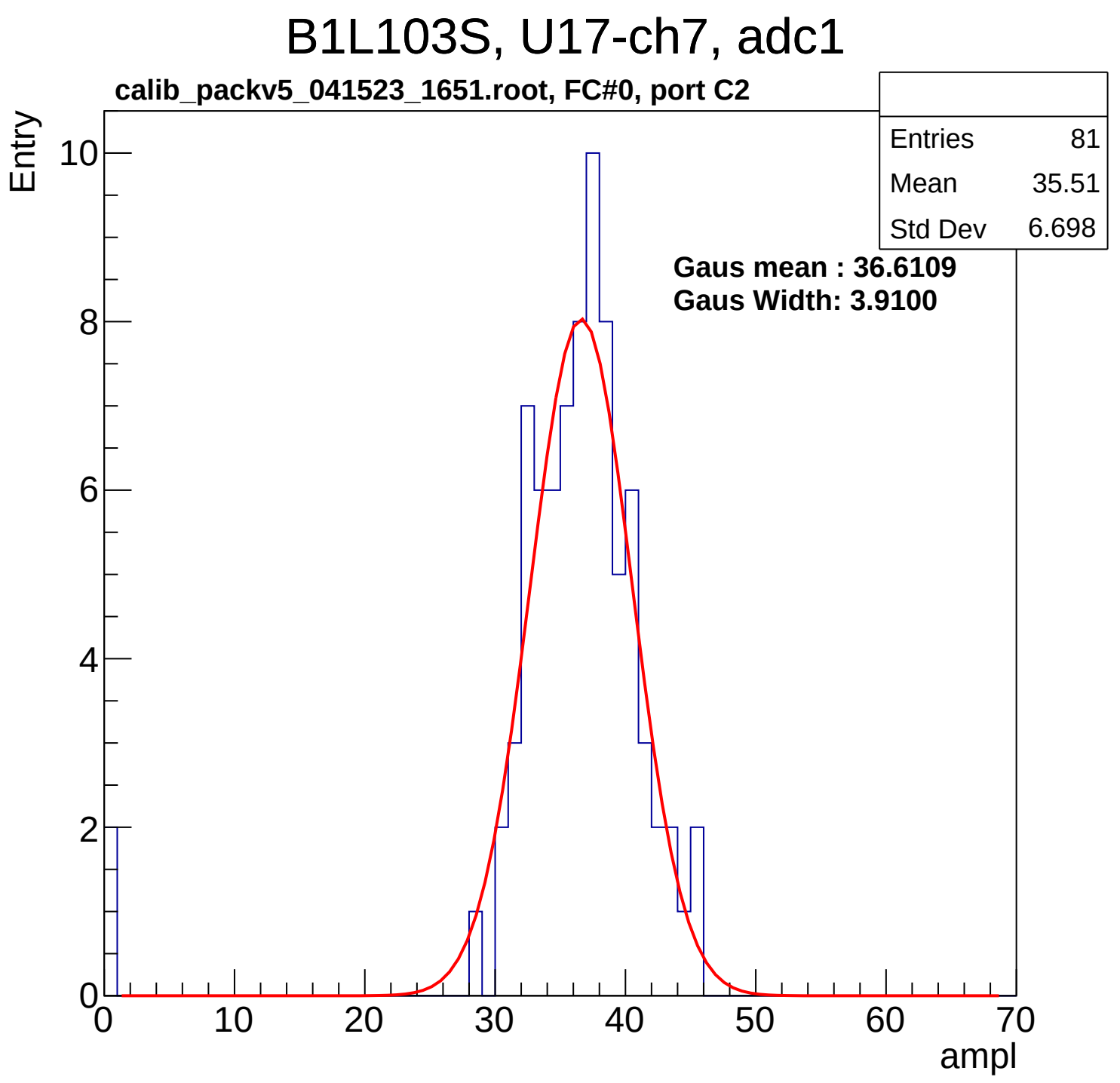

B1L103S, U17-ch6, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 55.44
Std Dev 3.595
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

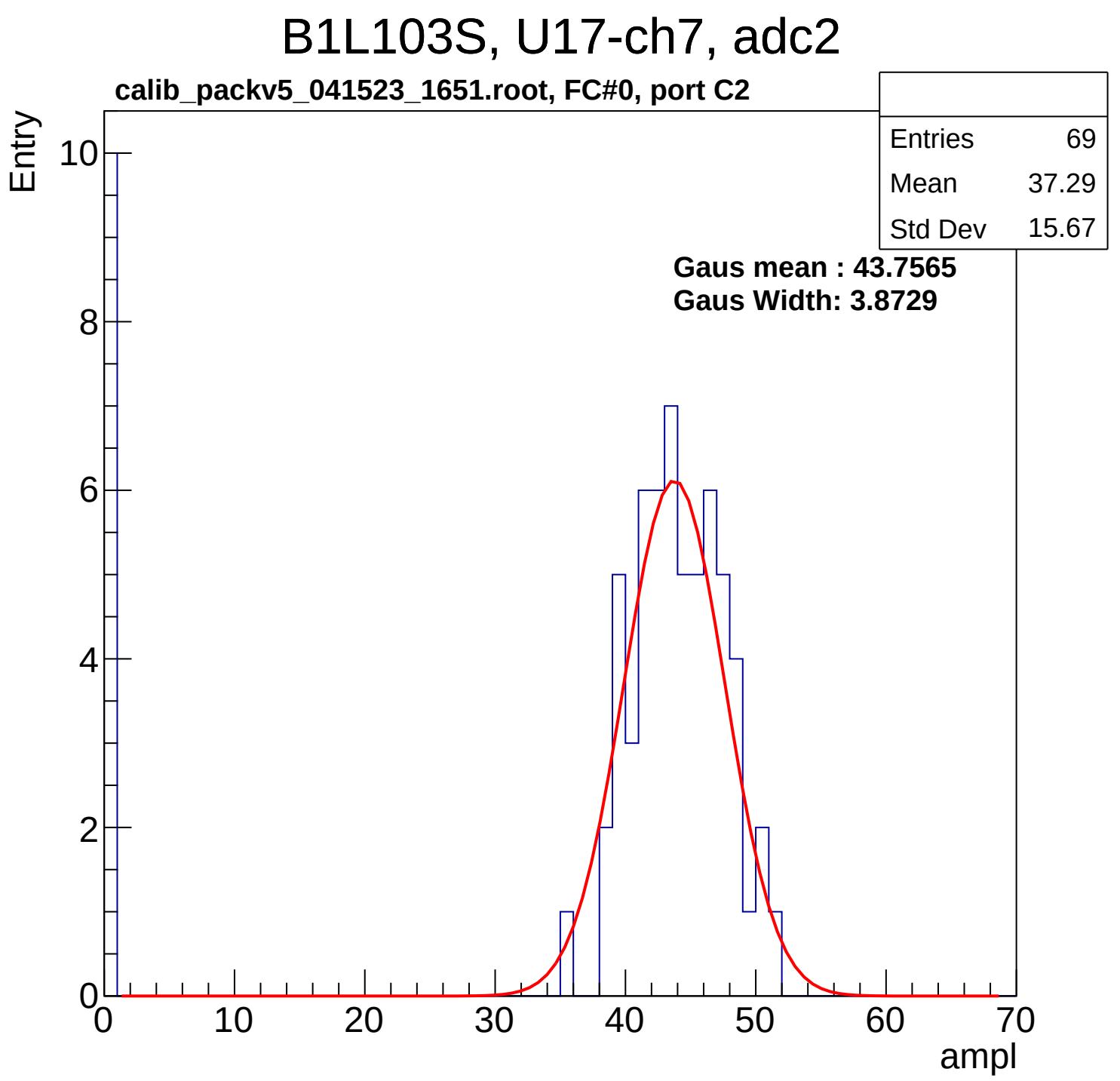

B1L103S, U17-ch6, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 60.48
Std Dev 2.231
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

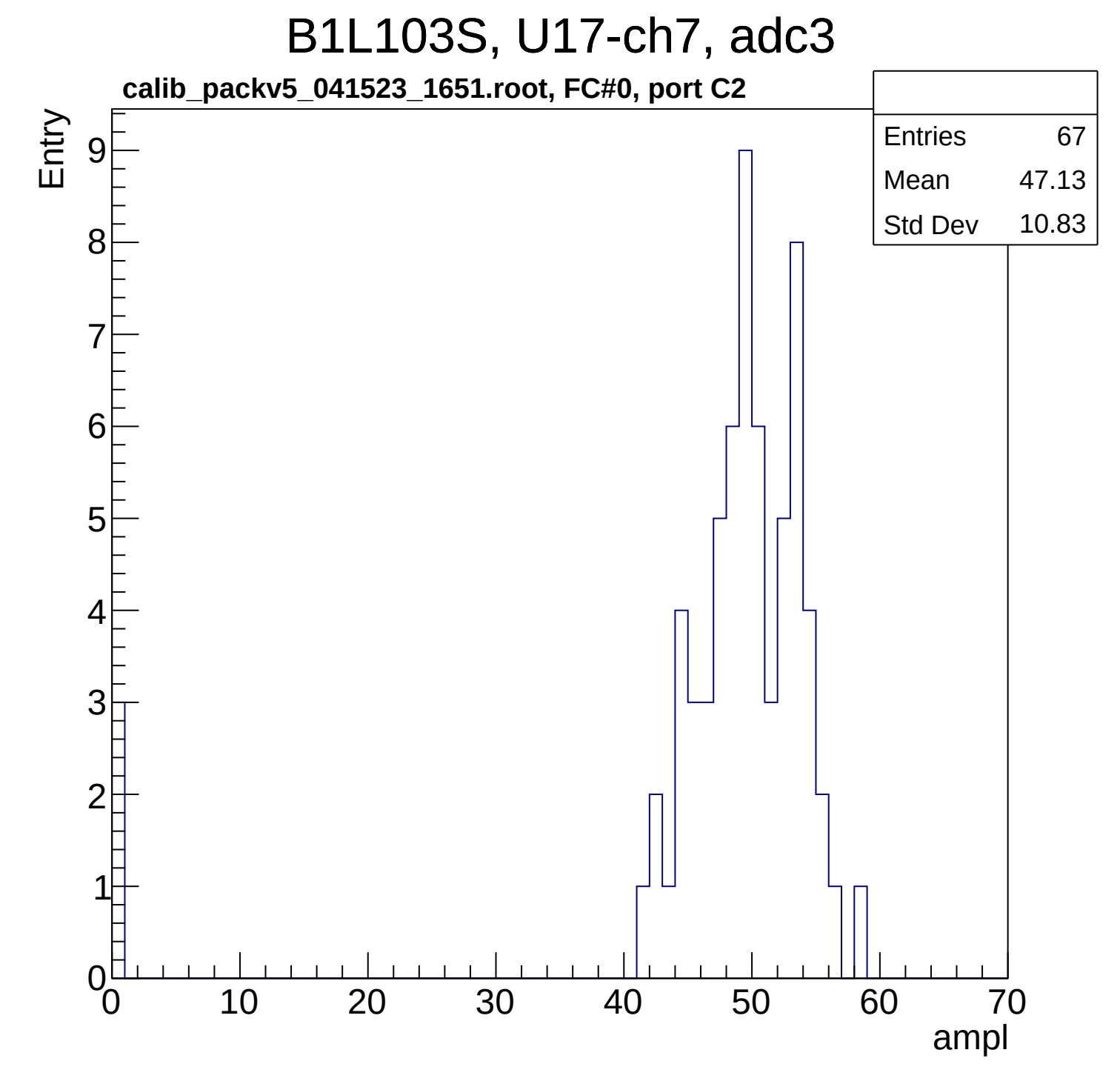

B1L103S, U17-ch6, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 51.17
Std Dev 22.9
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

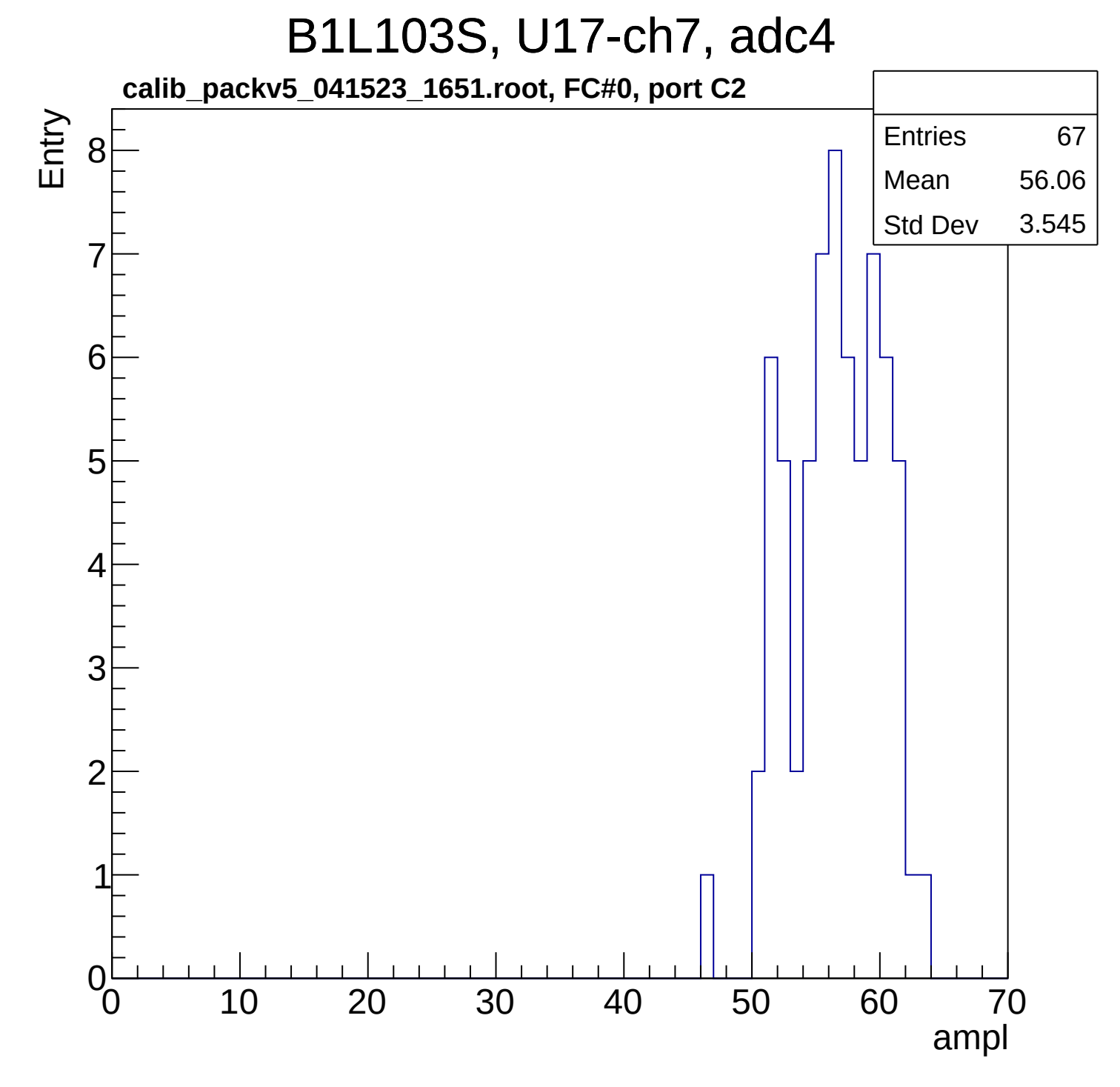

B1L103S, U17-ch6, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

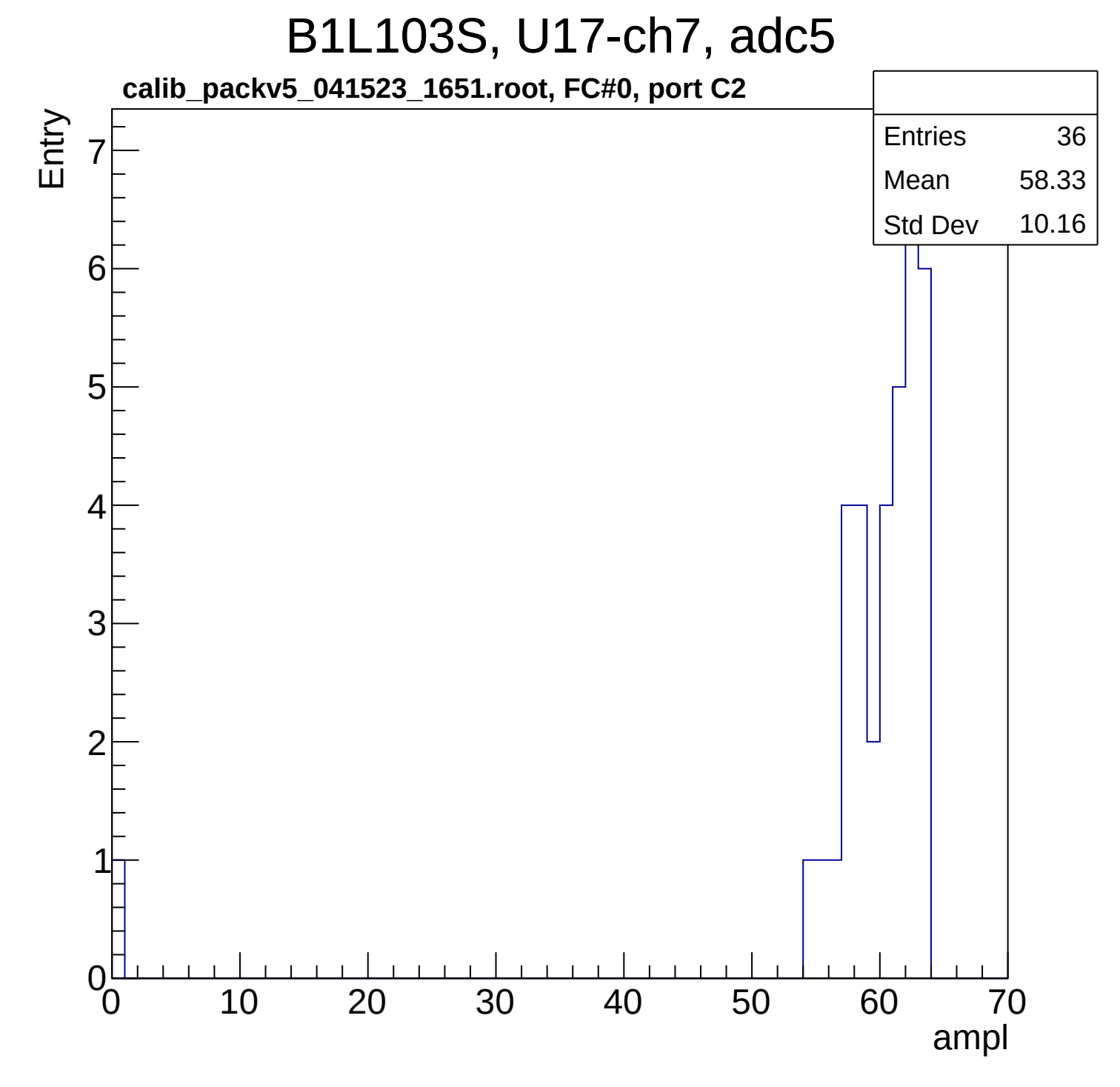

B1L103S, U17-ch7, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 24.52
Std Dev 11.8
Gaus mean : 29.9477
Gaus Width: 3.1676
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

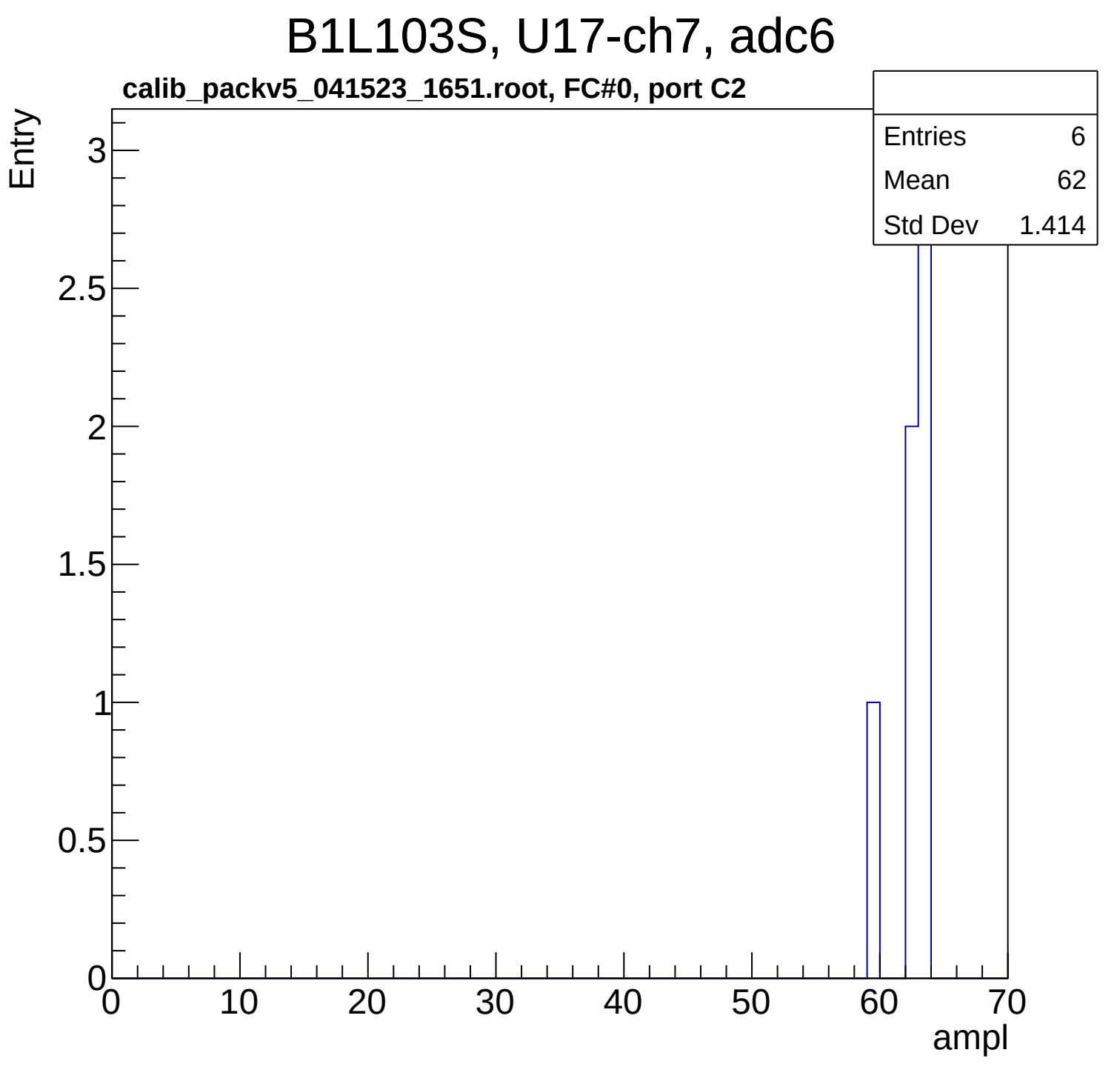

B1L103S, U17-ch7, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 35.51
Std Dev 6.698
Gaus mean : 36.6109
Gaus Width: 3.9100
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

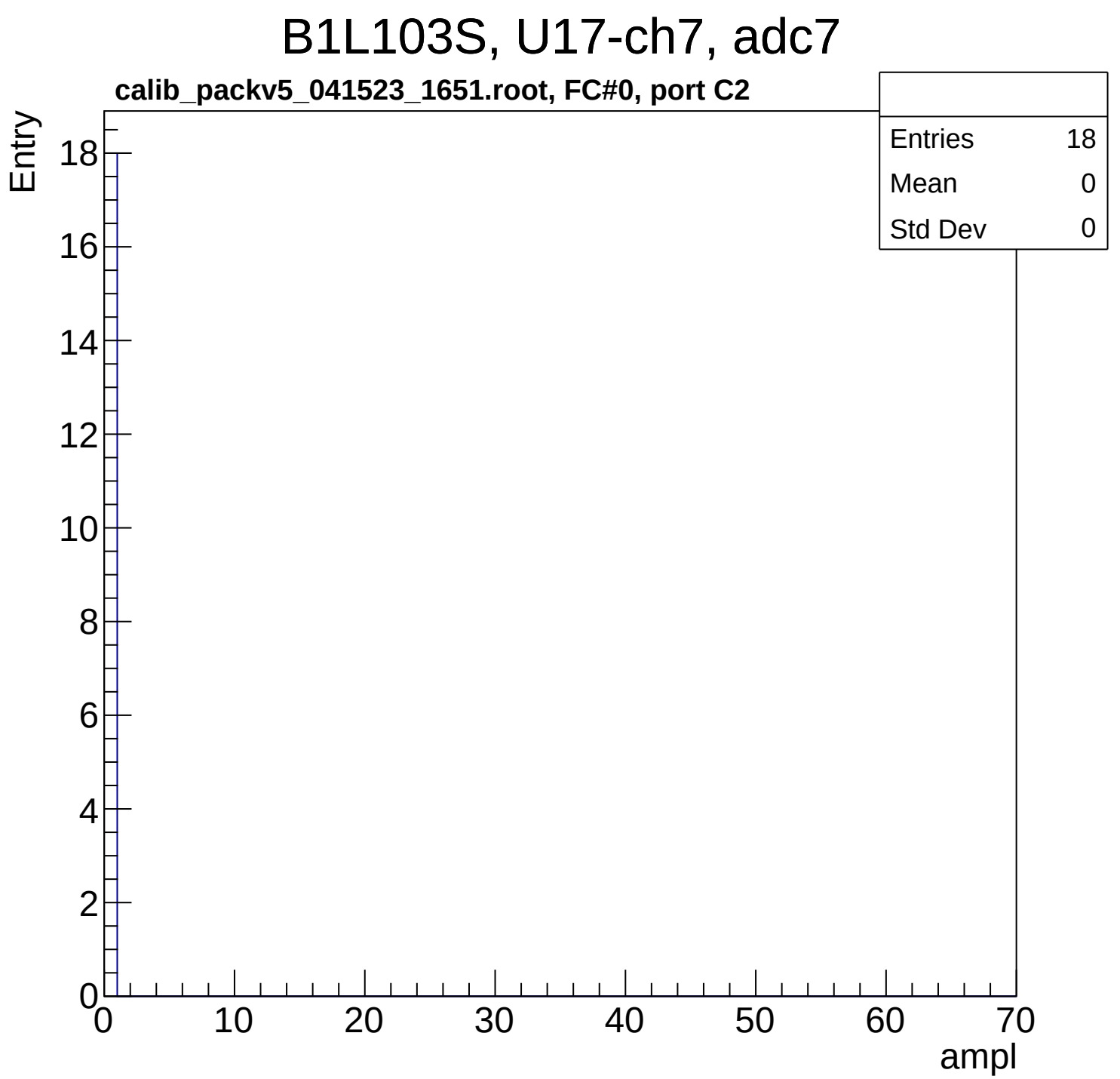

B1L103S, U17-ch7, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 37.29
Std Dev 15.67
Gaus mean : 43.7565
Gaus Width: 3.8729
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

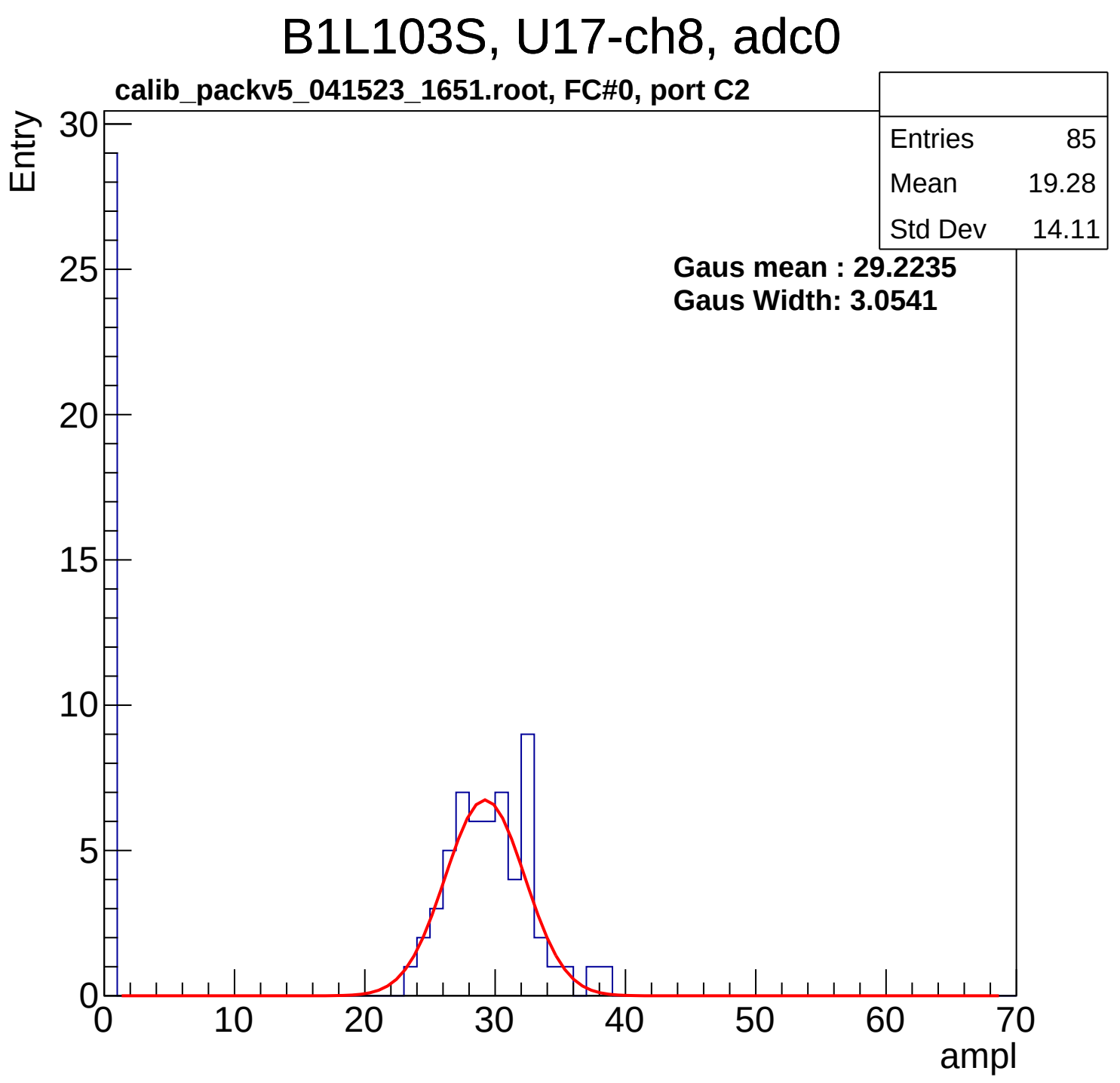

B1L103S, U17-ch7, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 47.13
Std Dev 10.83
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

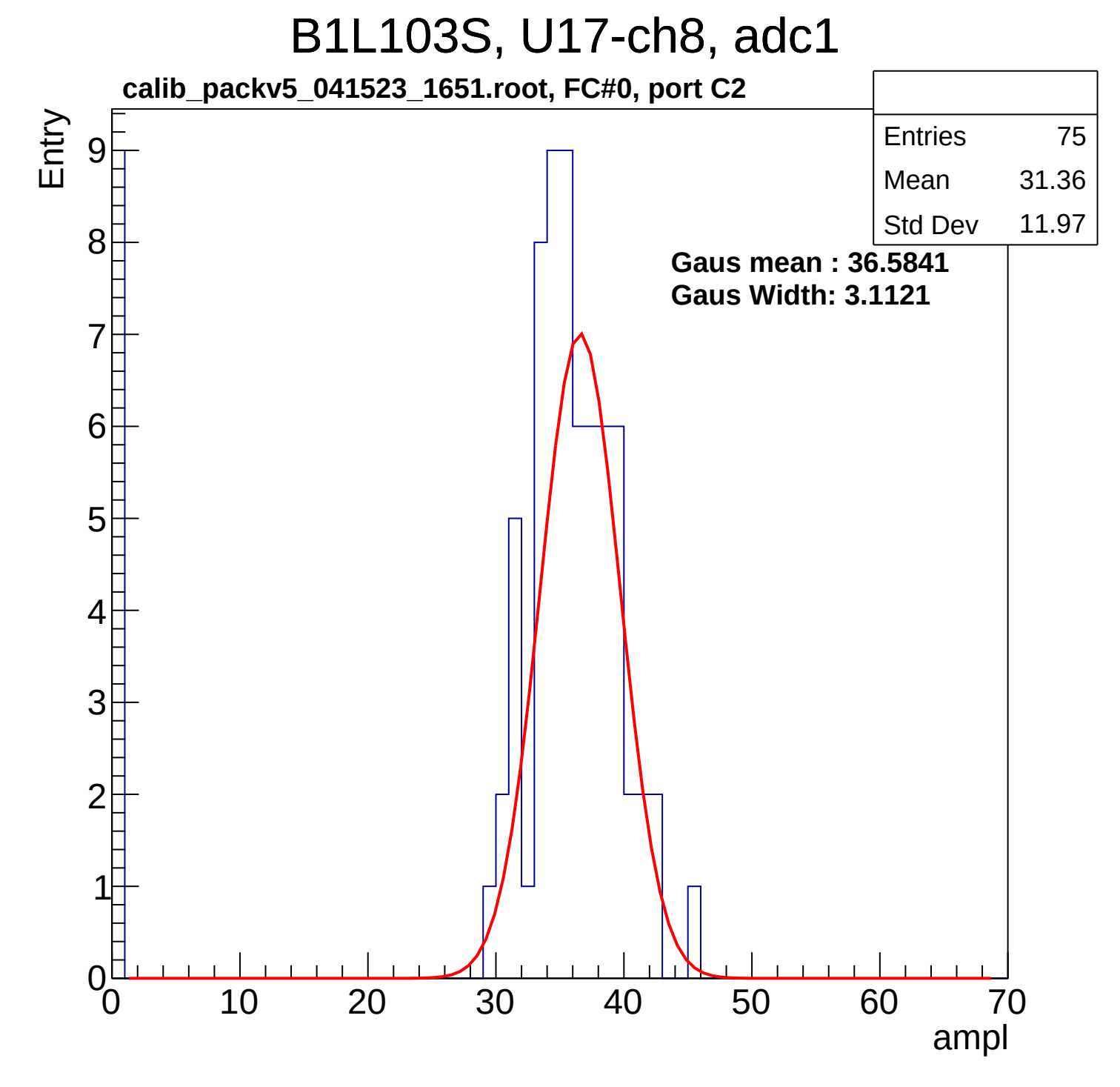

B1L103S, U17-ch7, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 56.06
Std Dev 3.545
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

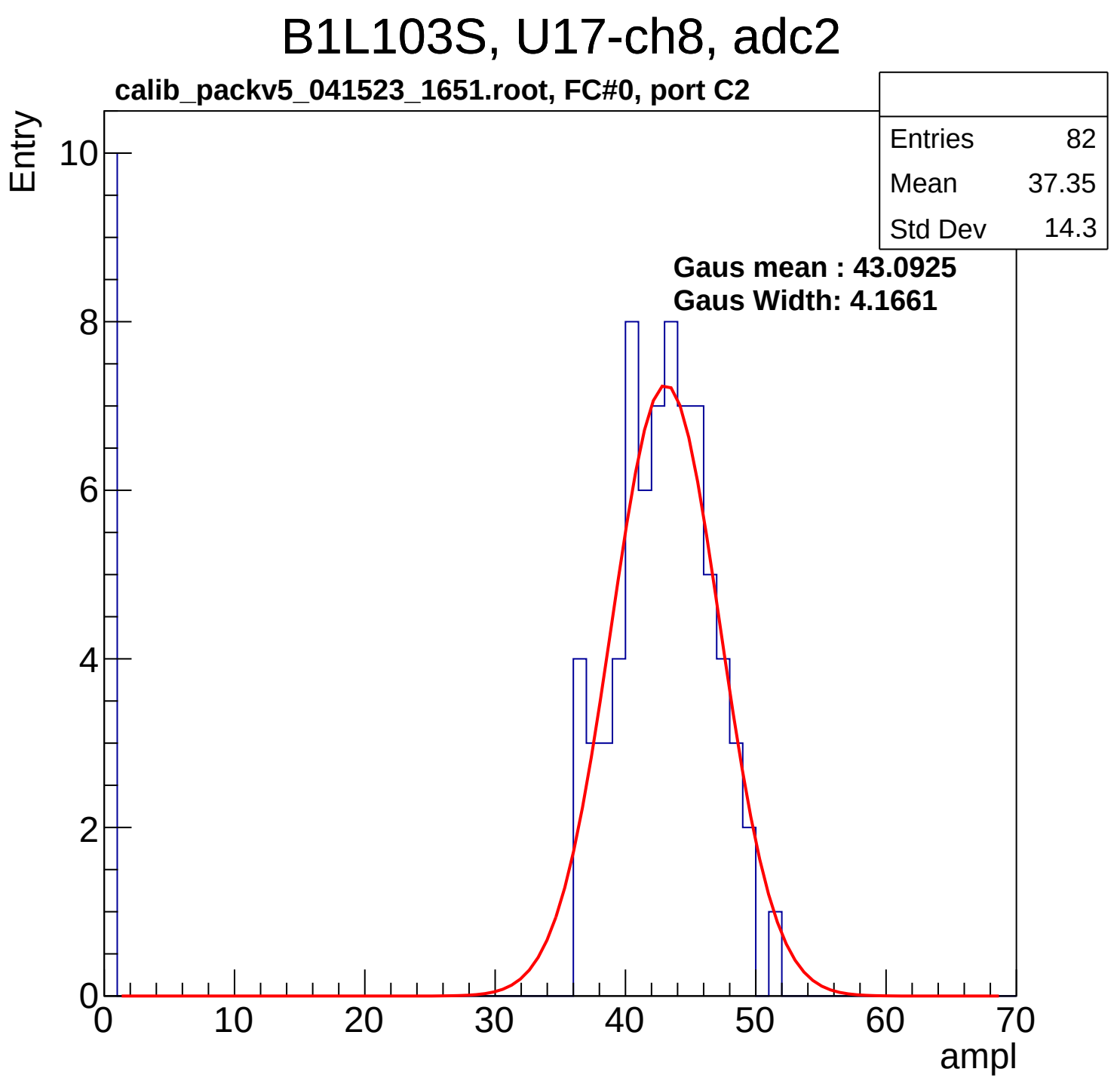

B1L103S, U17-ch7, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 58.33
Std Dev 10.16
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

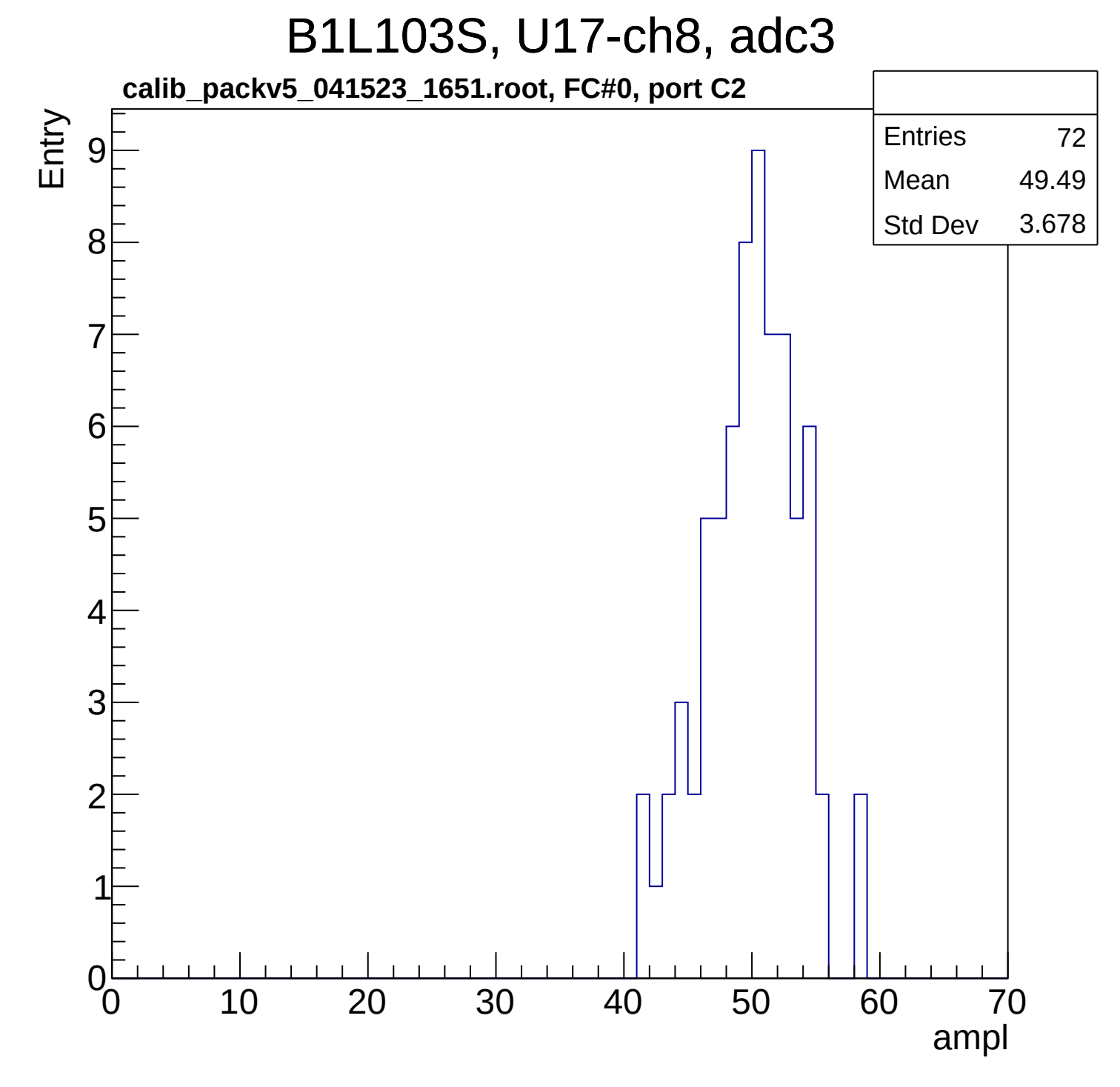

B1L103S, U17-ch7, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62
Std Dev 1.414
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

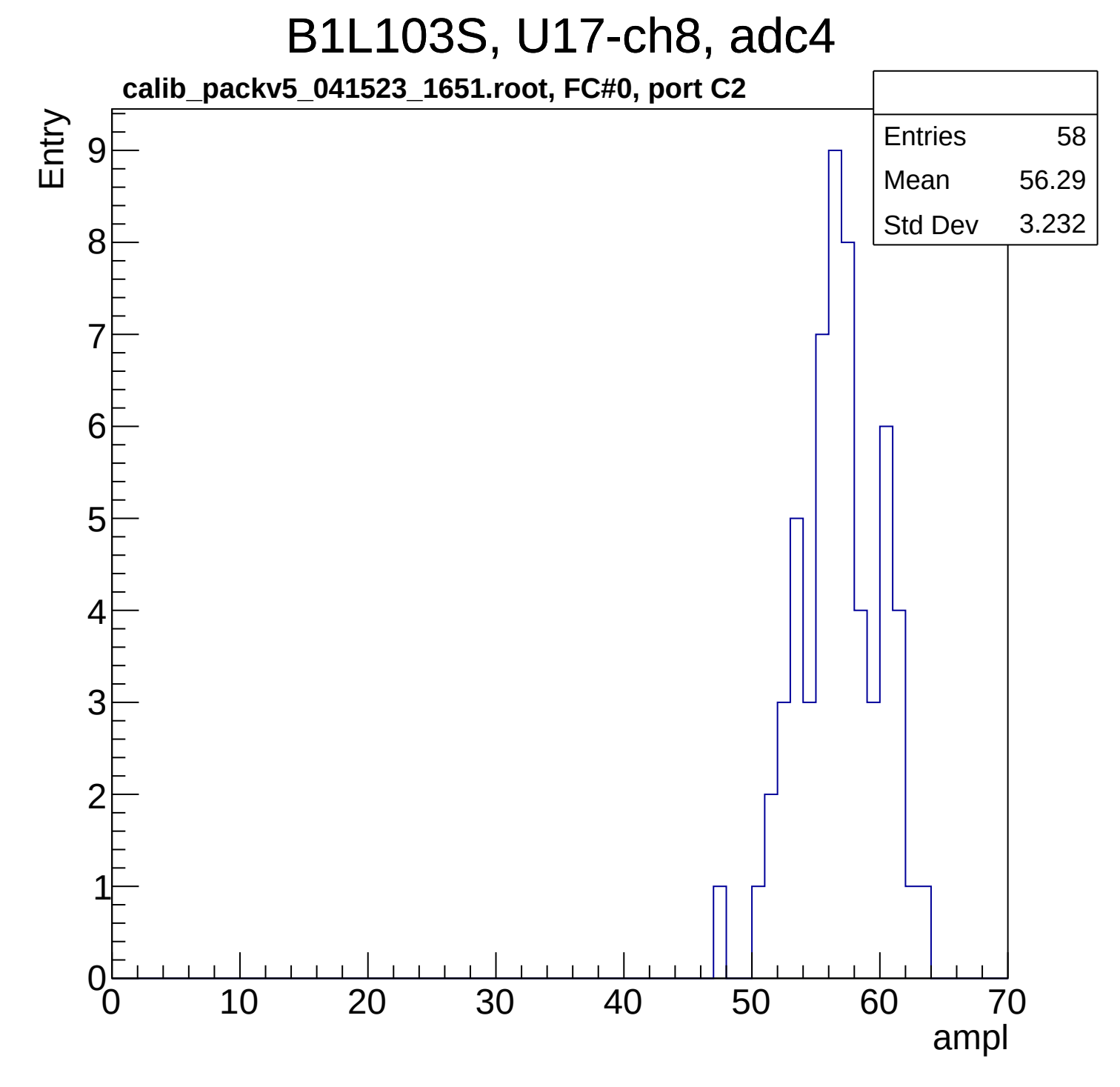

B1L103S, U17-ch7, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

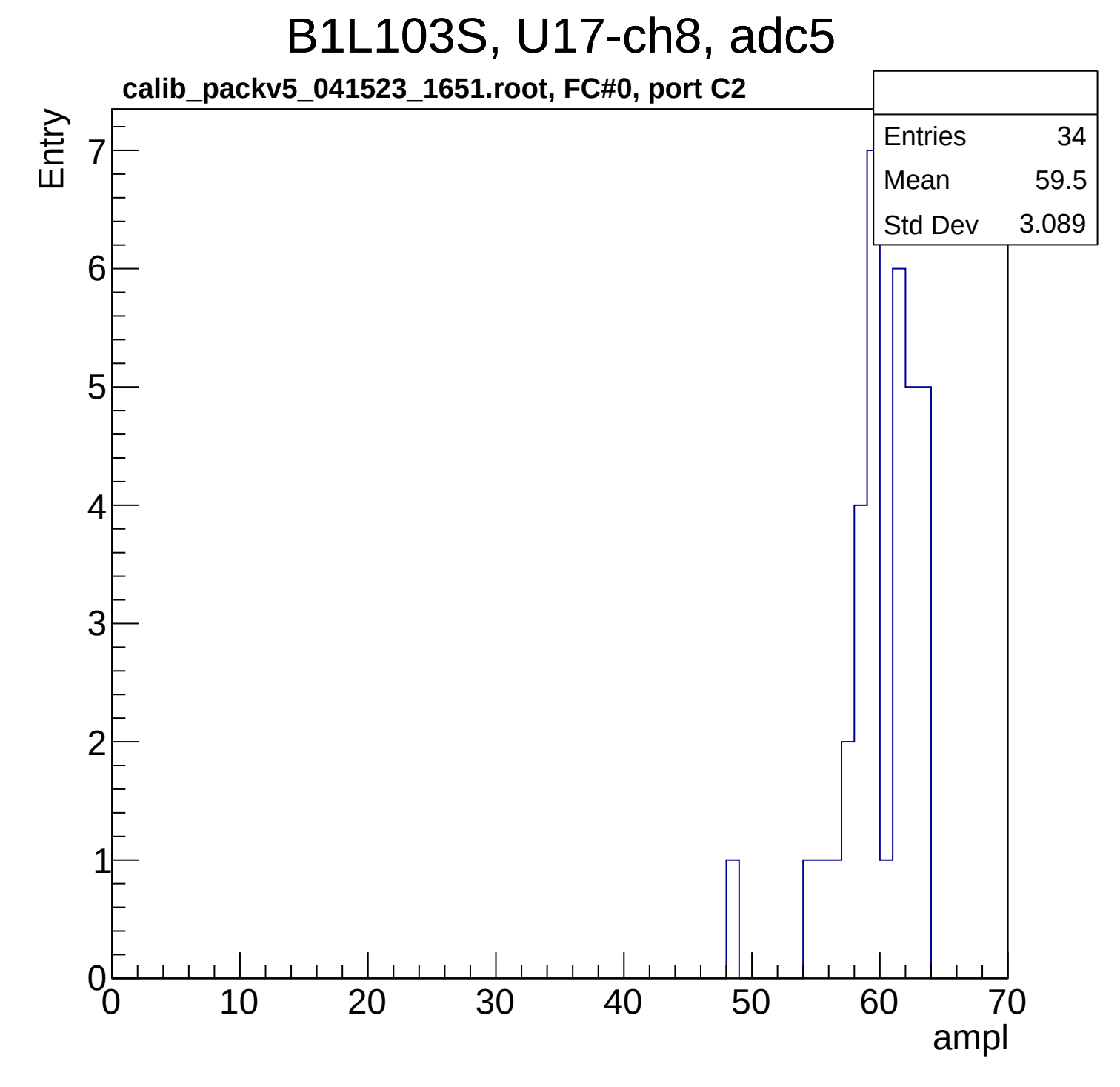

B1L103S, U17-ch8, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 19.28
Std Dev 14.11
Gaus mean : 29.2235
Gaus Width: 3.0541
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70

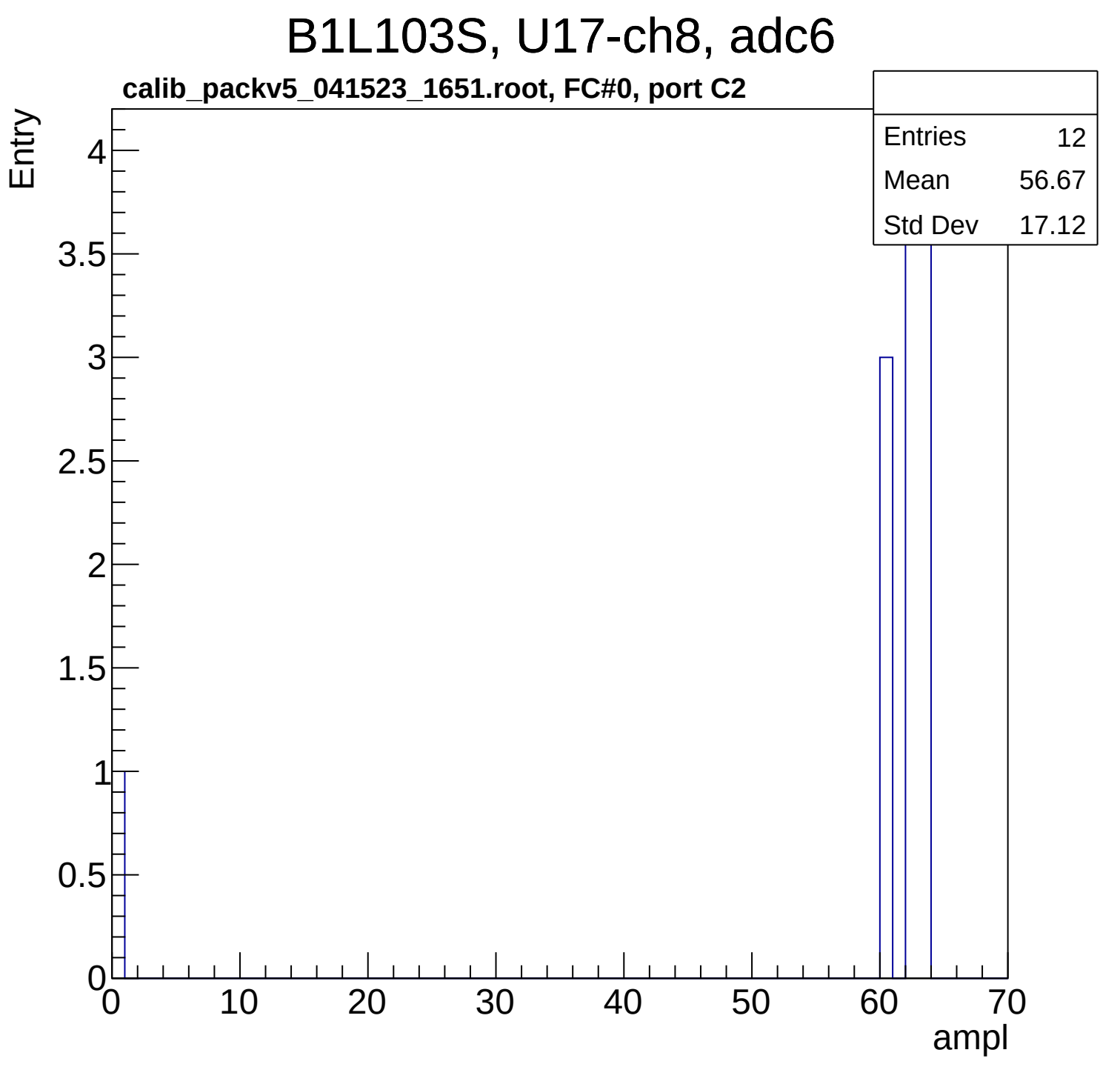

B1L103S, U17-ch8, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 31.36
Std Dev 11.97
Gaus mean : 36.5841
Gaus Width: 3.1121
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

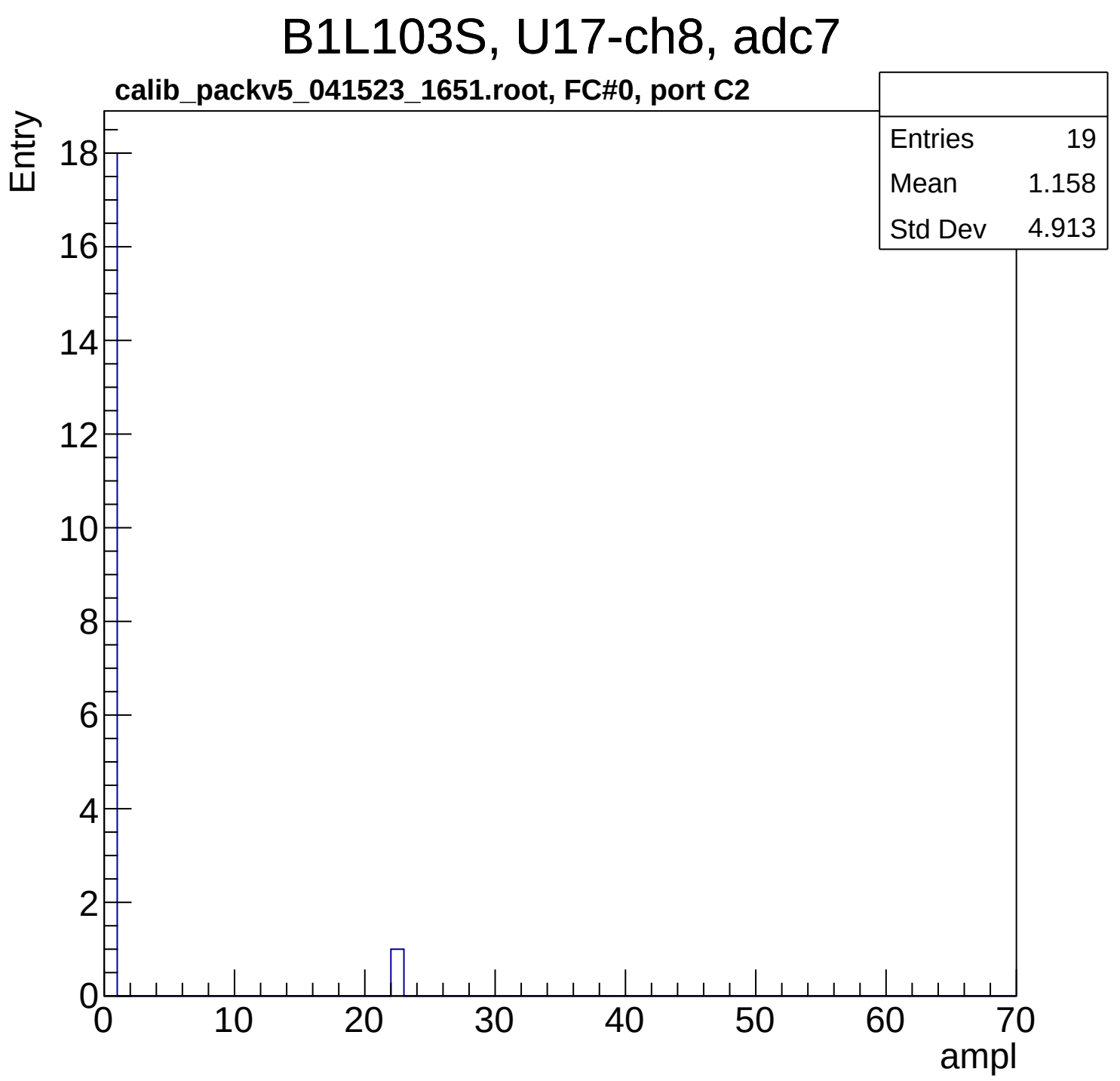

B1L103S, U17-ch8, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 37.35
Std Dev 14.3
Gaus mean : 43.0925
Gaus Width: 4.1661
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

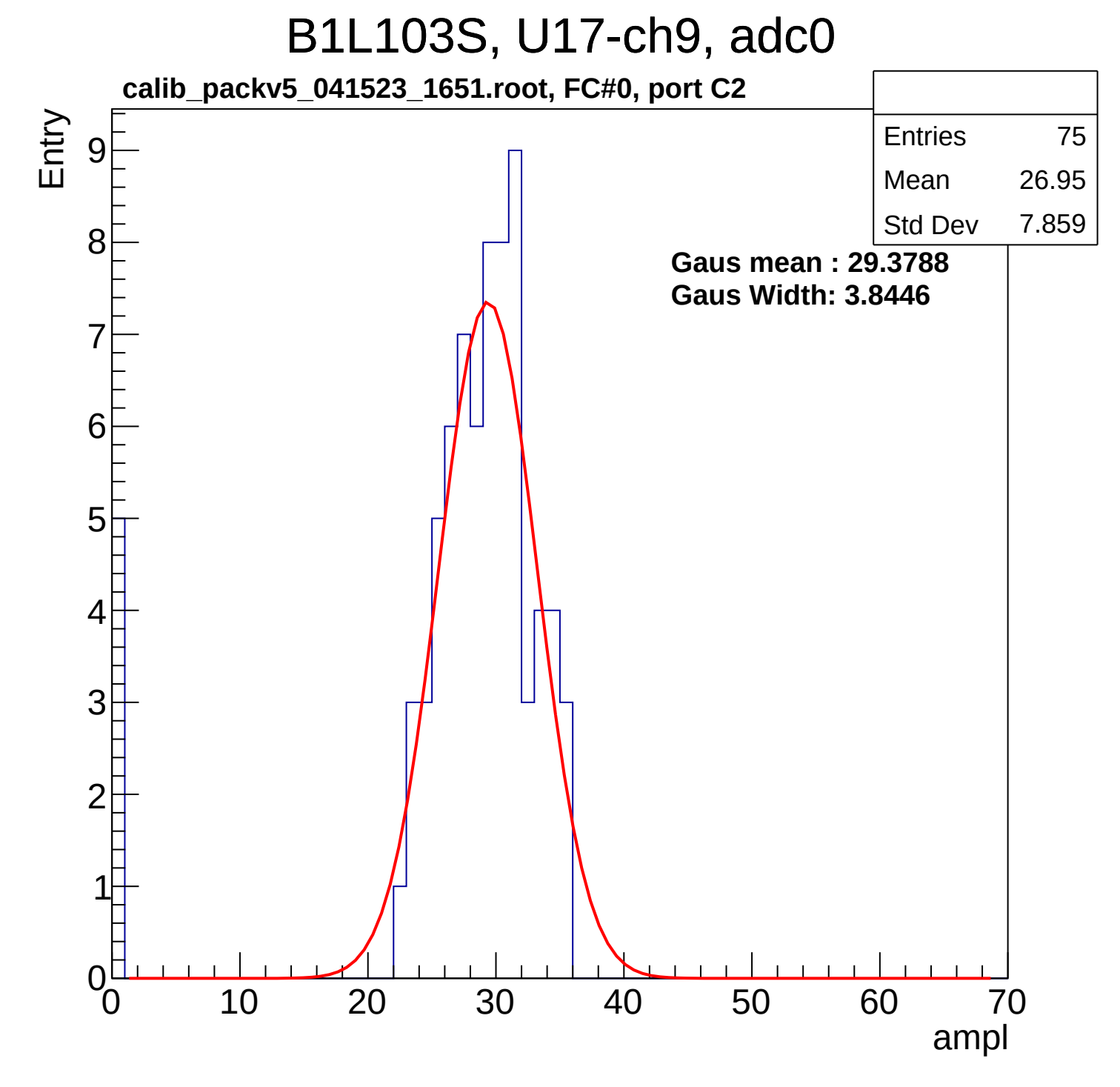

B1L103S, U17-ch8, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 49.49
Std Dev 3.678
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

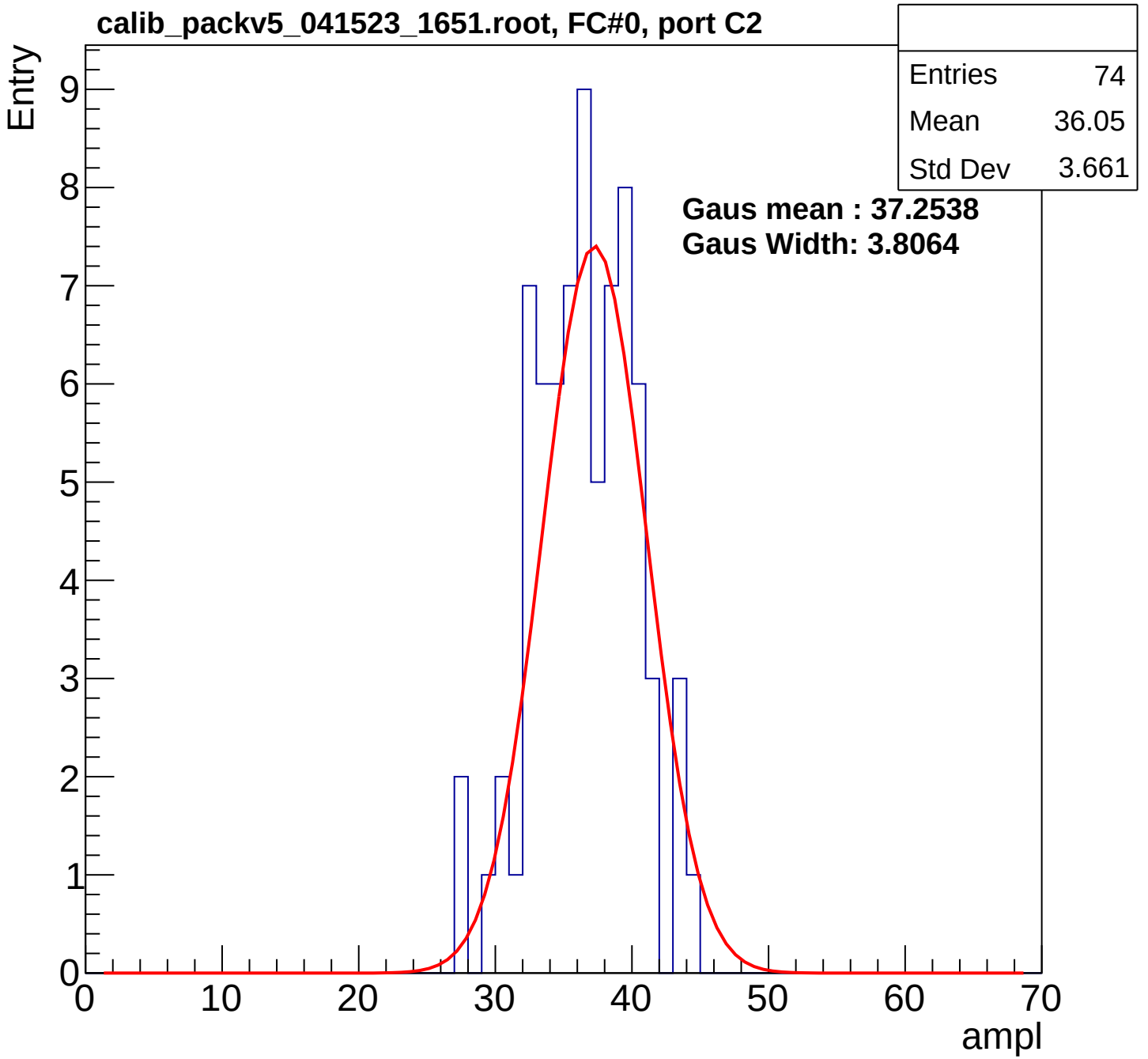

B1L103S, U17-ch8, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 56.29
Std Dev 3.232
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

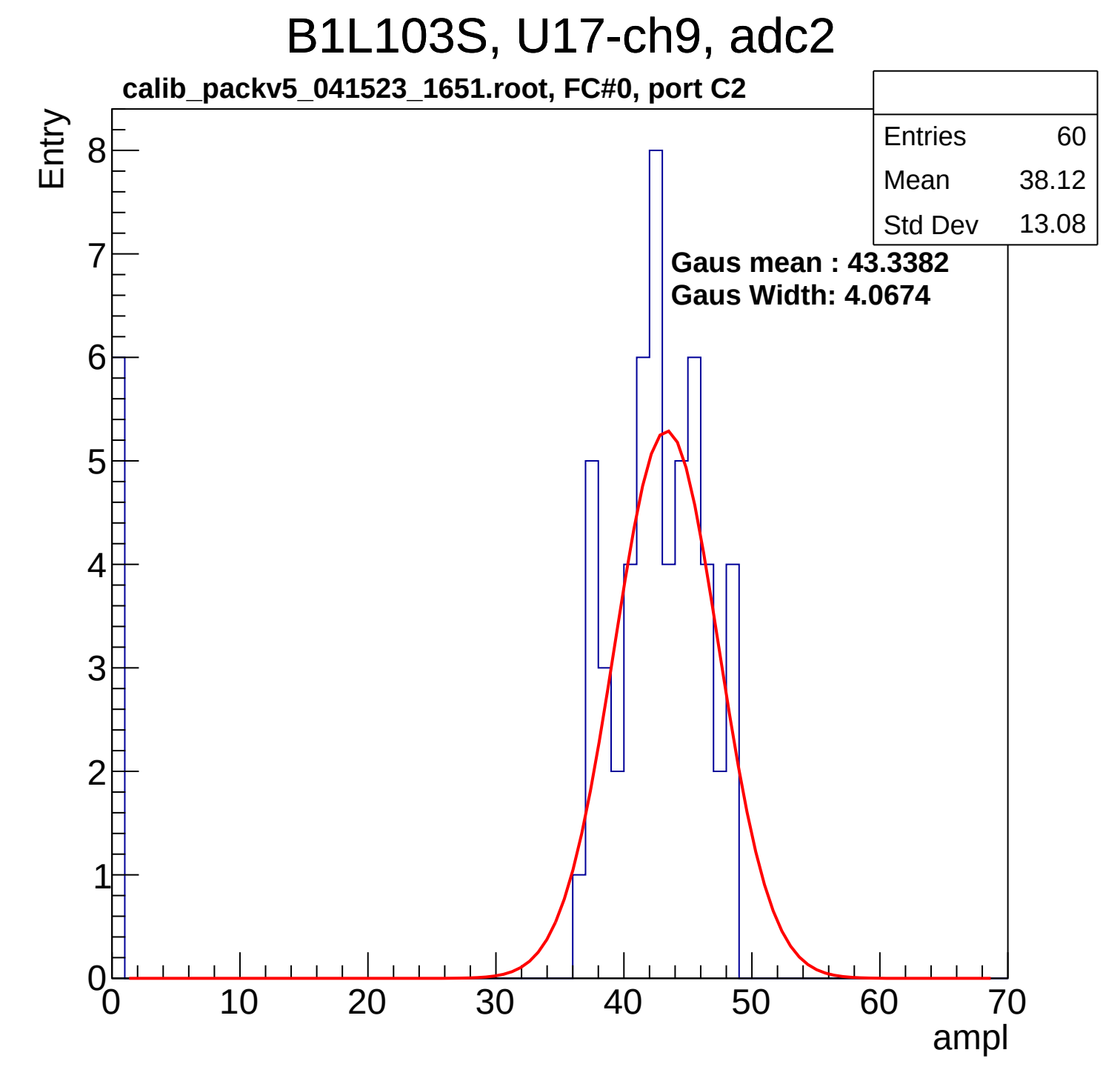

B1L103S, U17-ch8, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 59.5
Std Dev 3.089
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

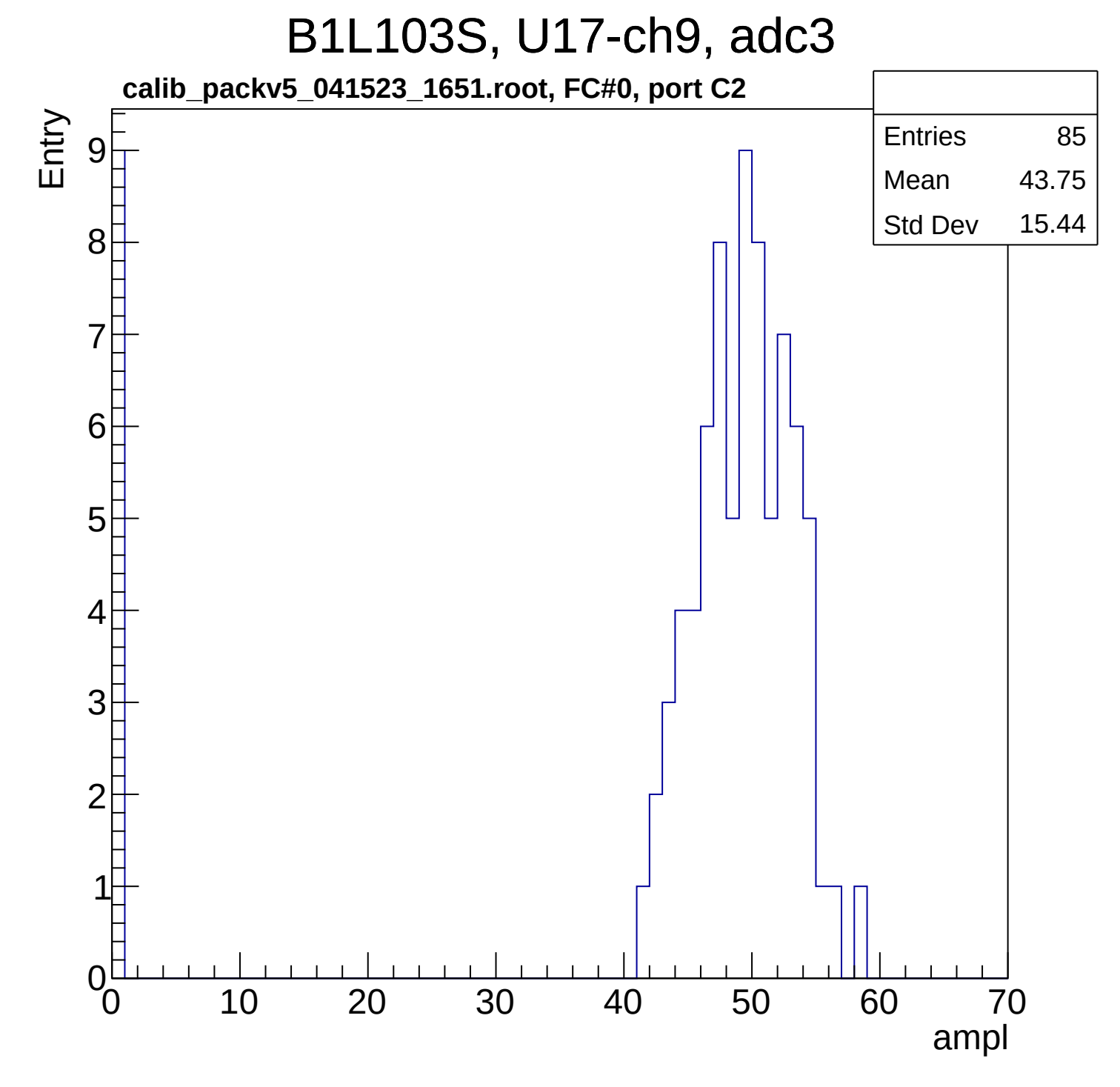

B1L103S, U17-ch8, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.67
Std Dev 17.12
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

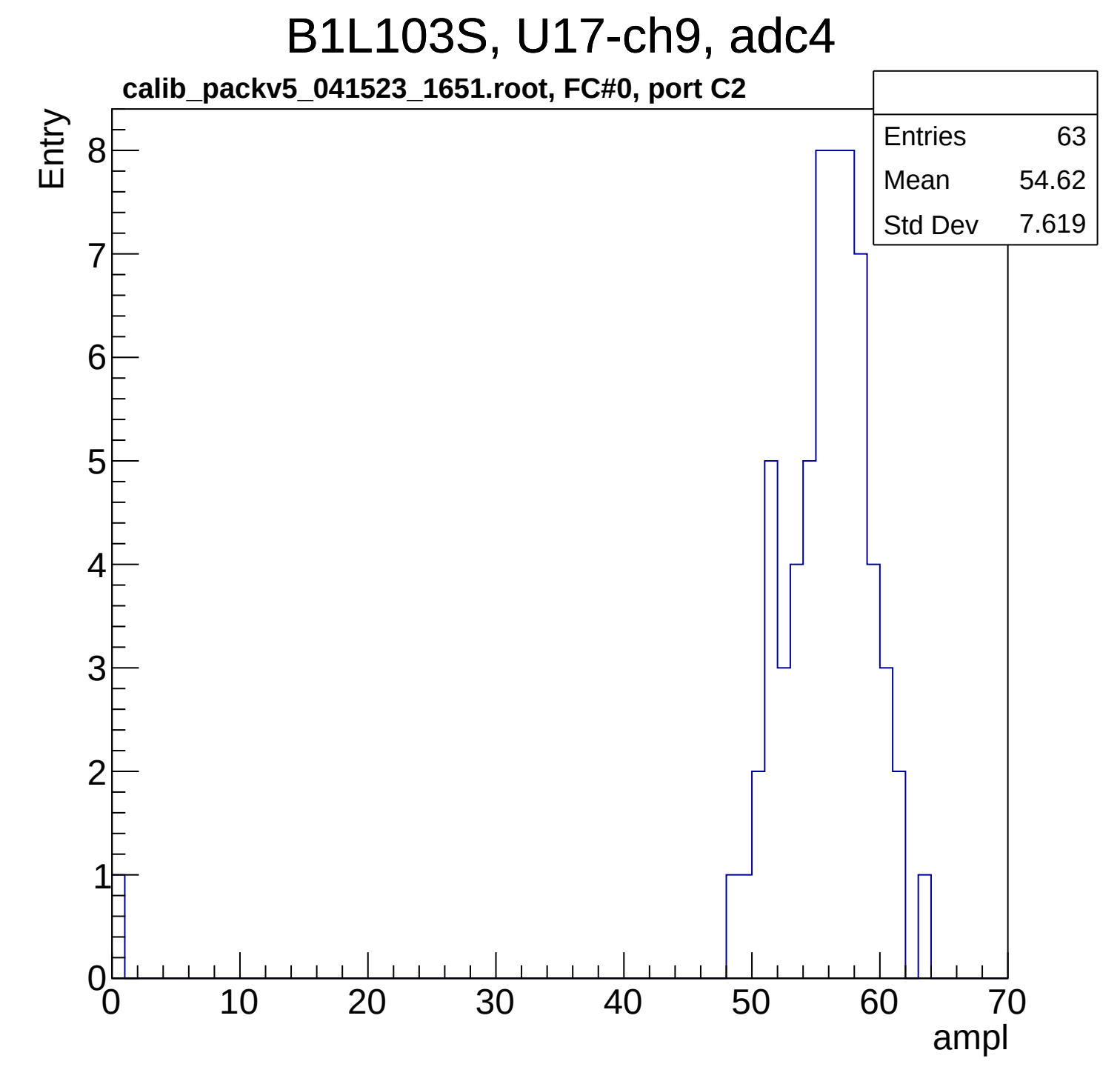

B1L103S, U17-ch8, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

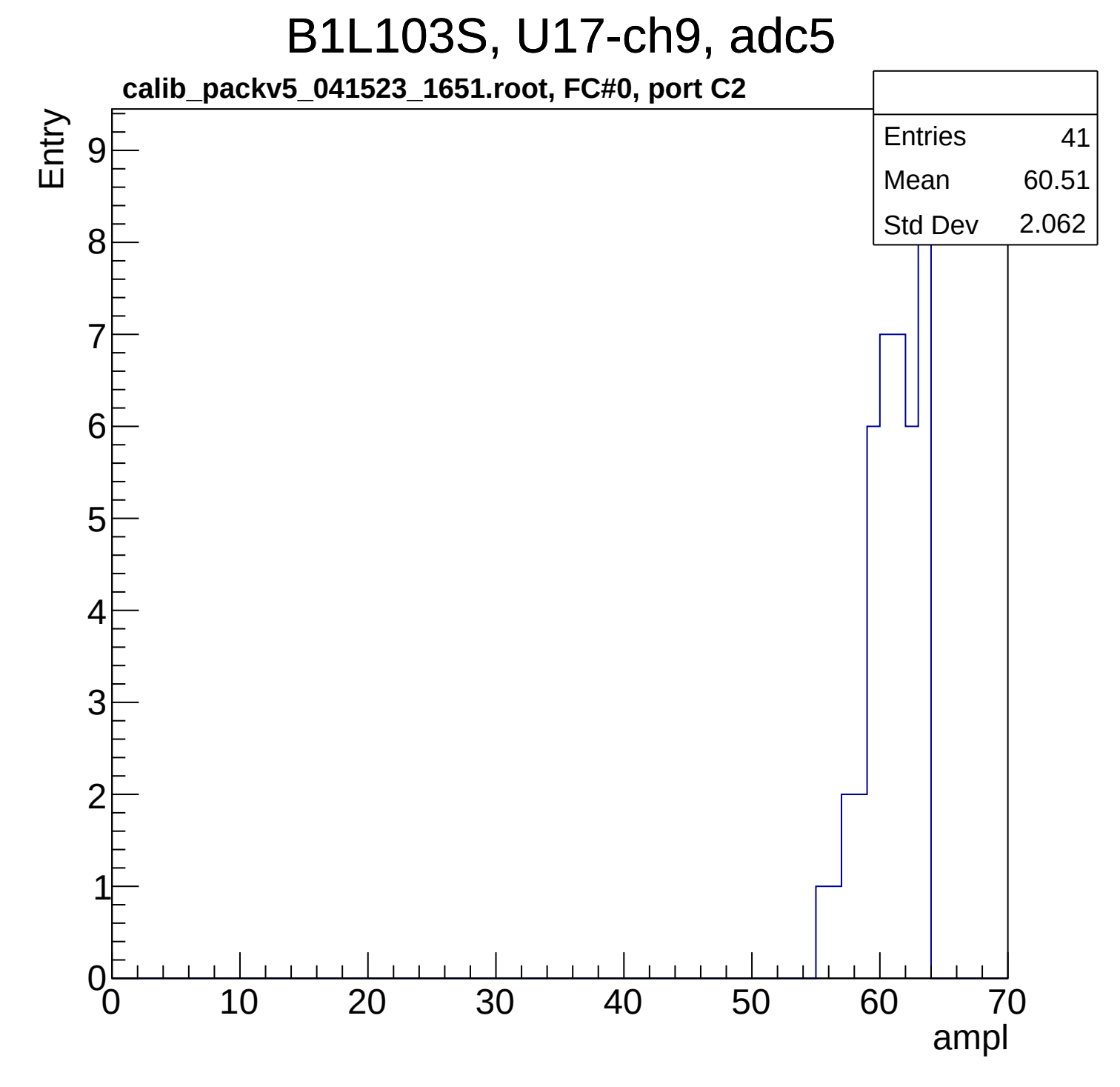

B1L103S, U17-ch9, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 26.95
Std Dev 7.859
Gaus mean : 29.3788
Gaus Width: 3.8446
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

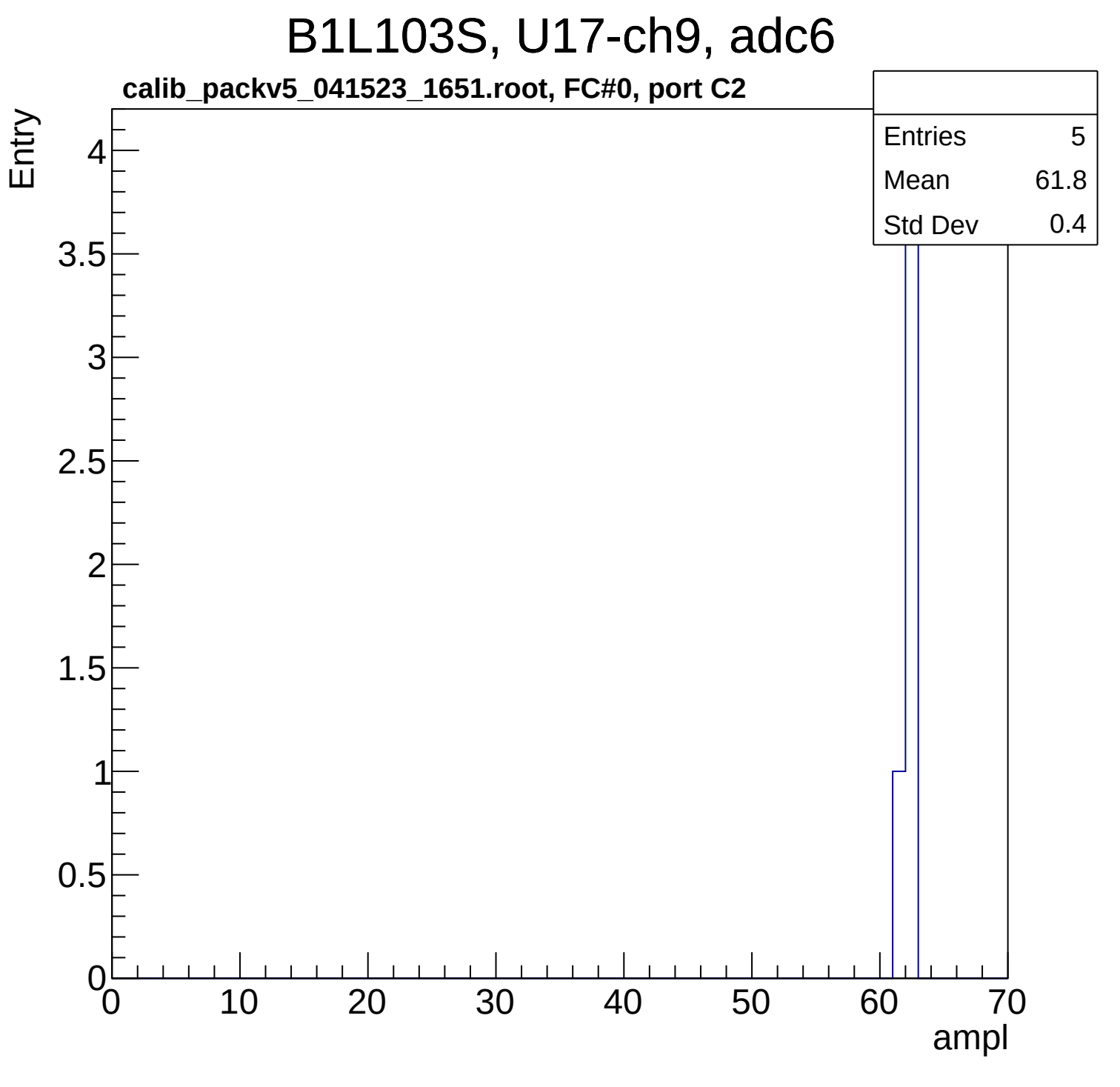

B1L103S, U17-ch9, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 36.05
Std Dev 3.661
Gaus mean : 37.2538
Gaus Width: 3.8064
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

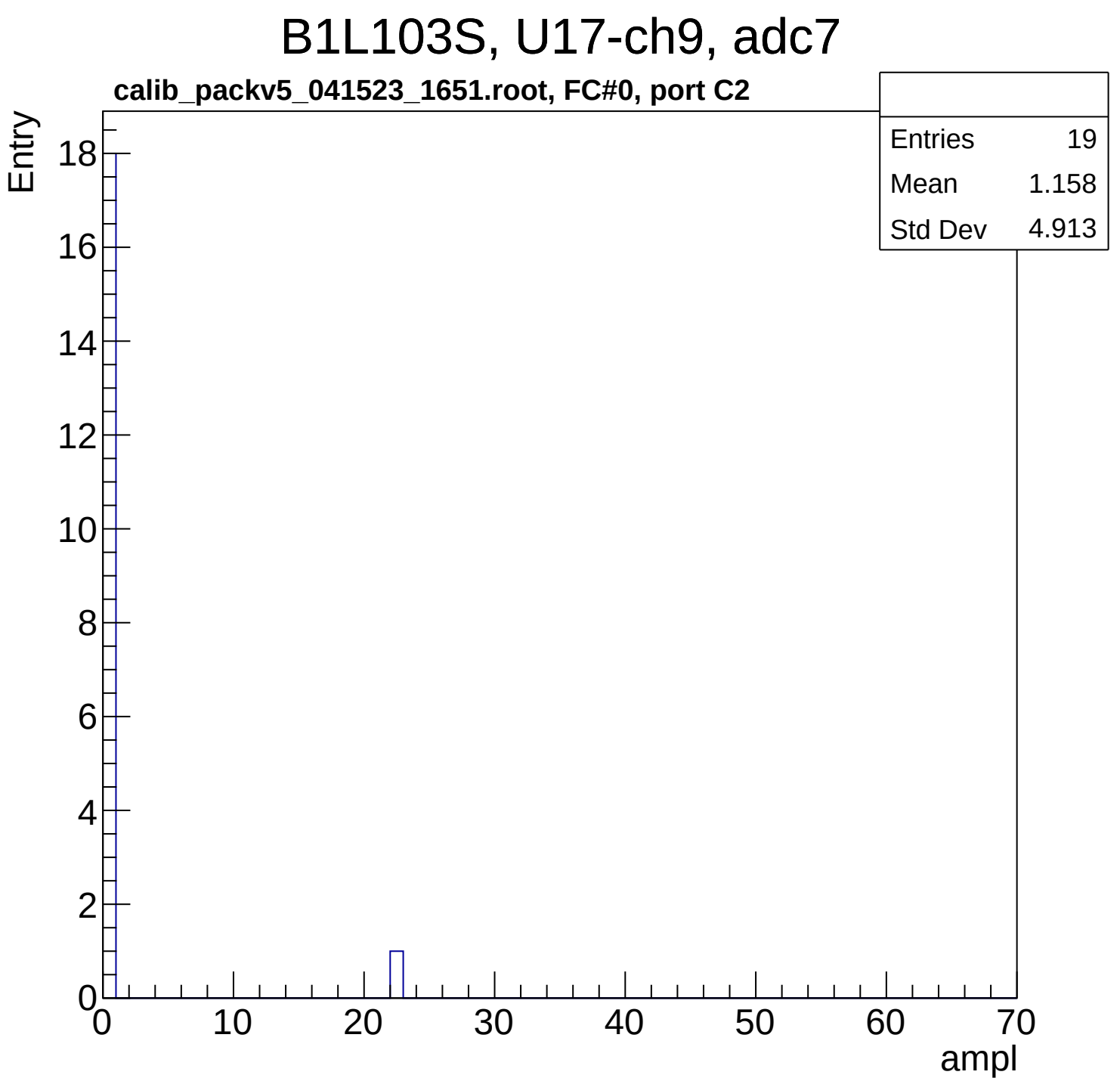

B1L103S, U17-ch9, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 38.12
Std Dev 13.08
Gaus mean : 43.3382
Gaus Width: 4.0674
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

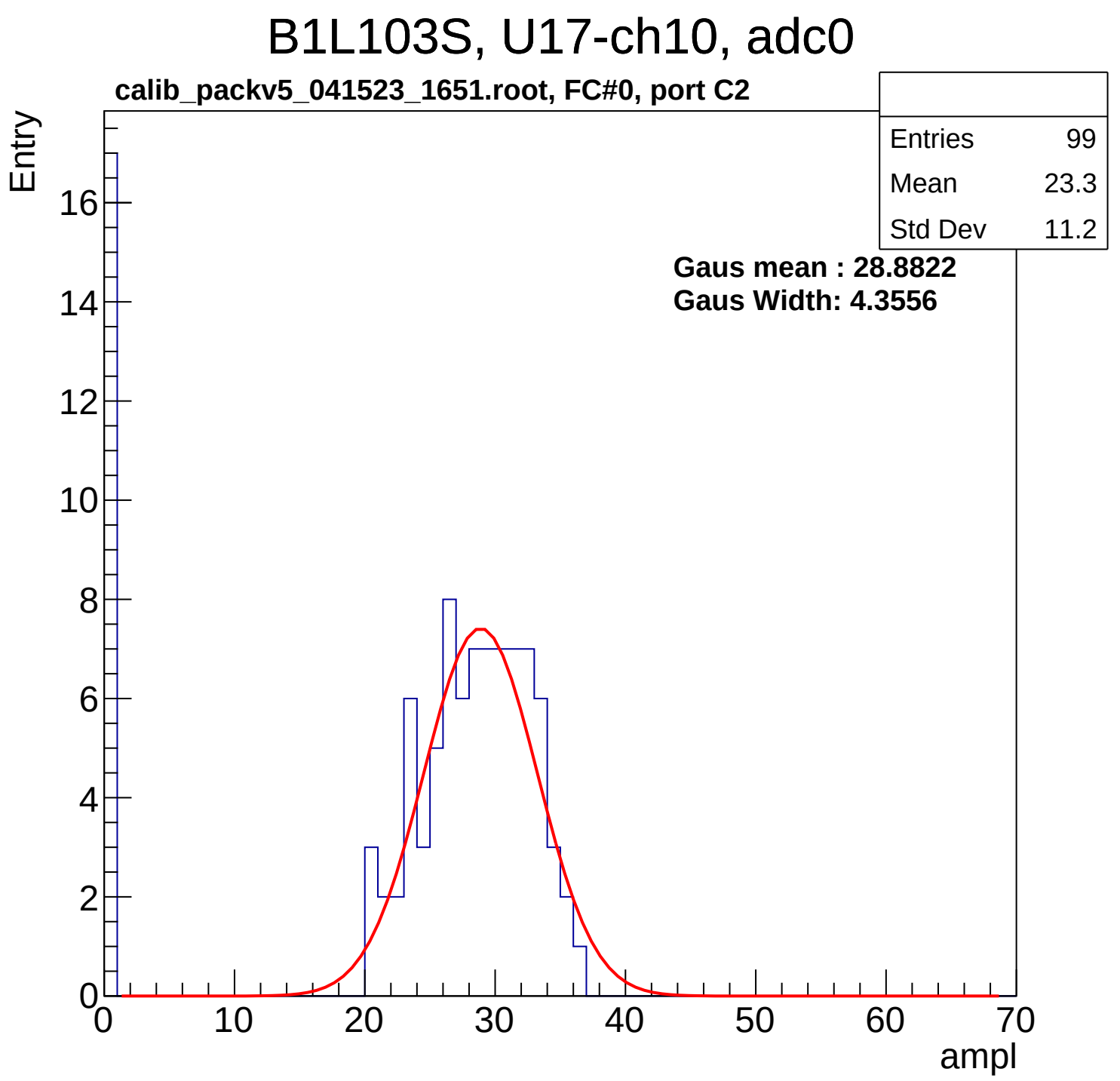

B1L103S, U17-ch9, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 43.75
Std Dev 15.44
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

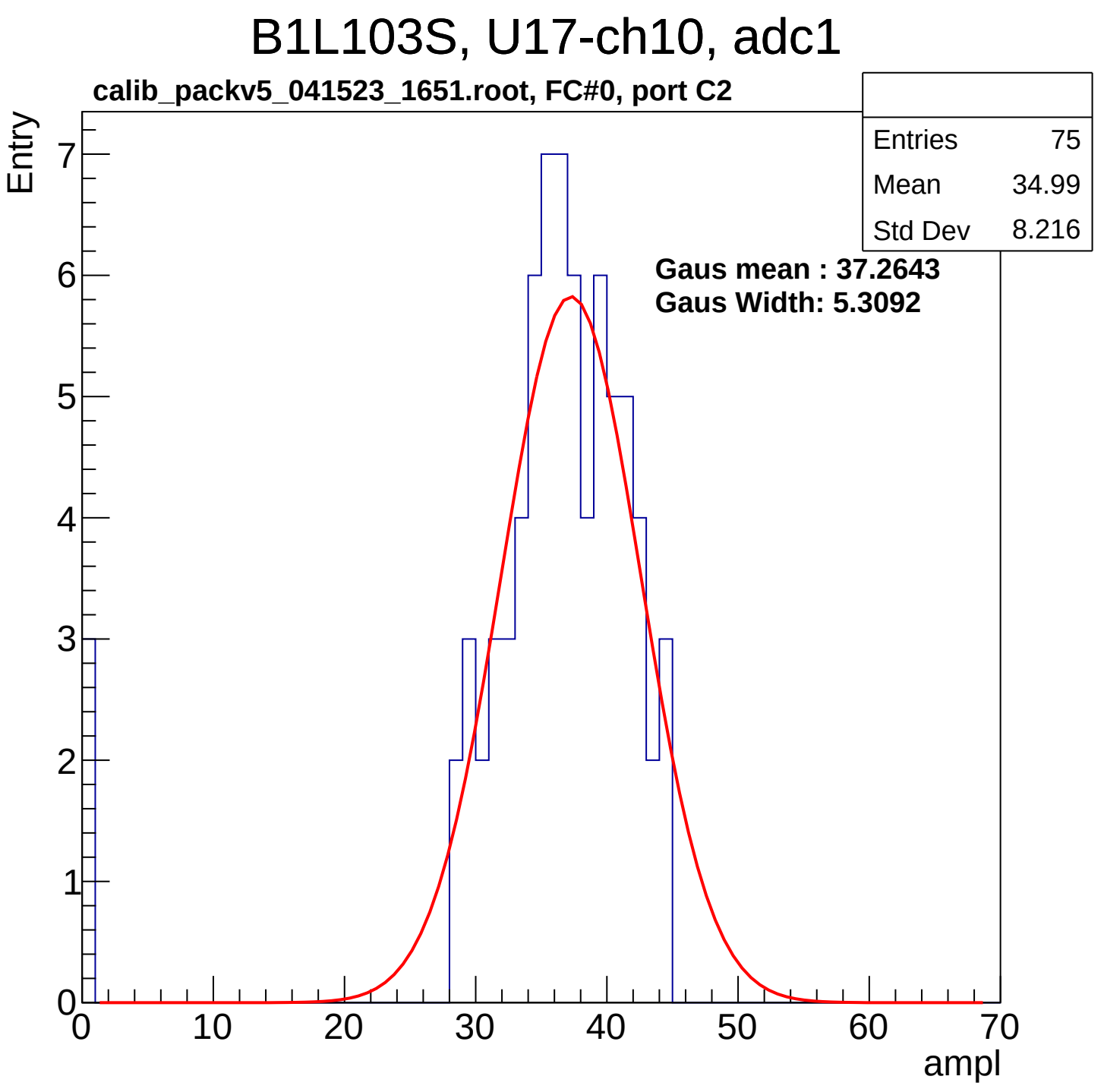

B1L103S, U17-ch9, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 54.62
Std Dev 7.619
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

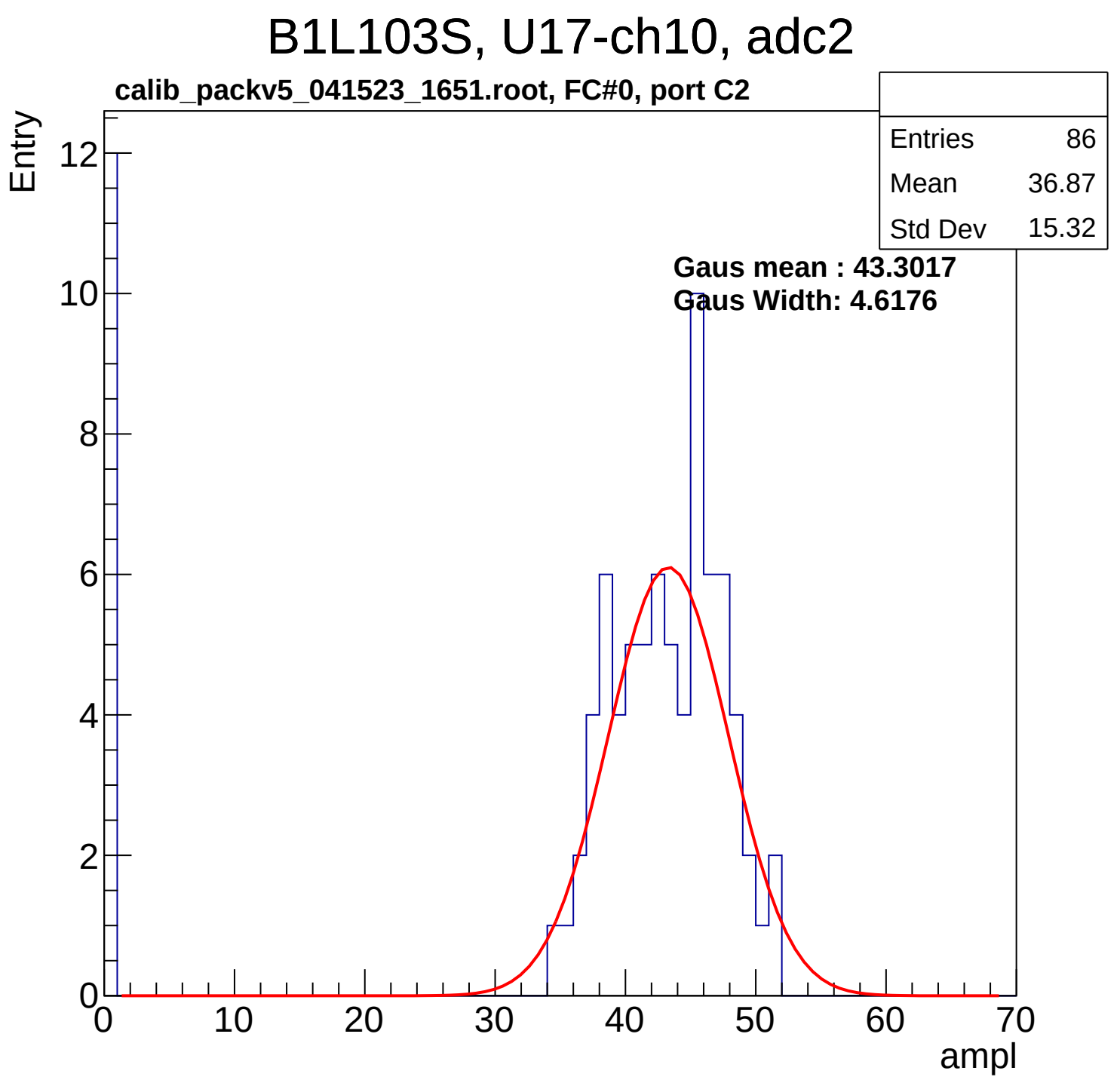

B1L103S, U17-ch9, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 60.51
Std Dev 2.062
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

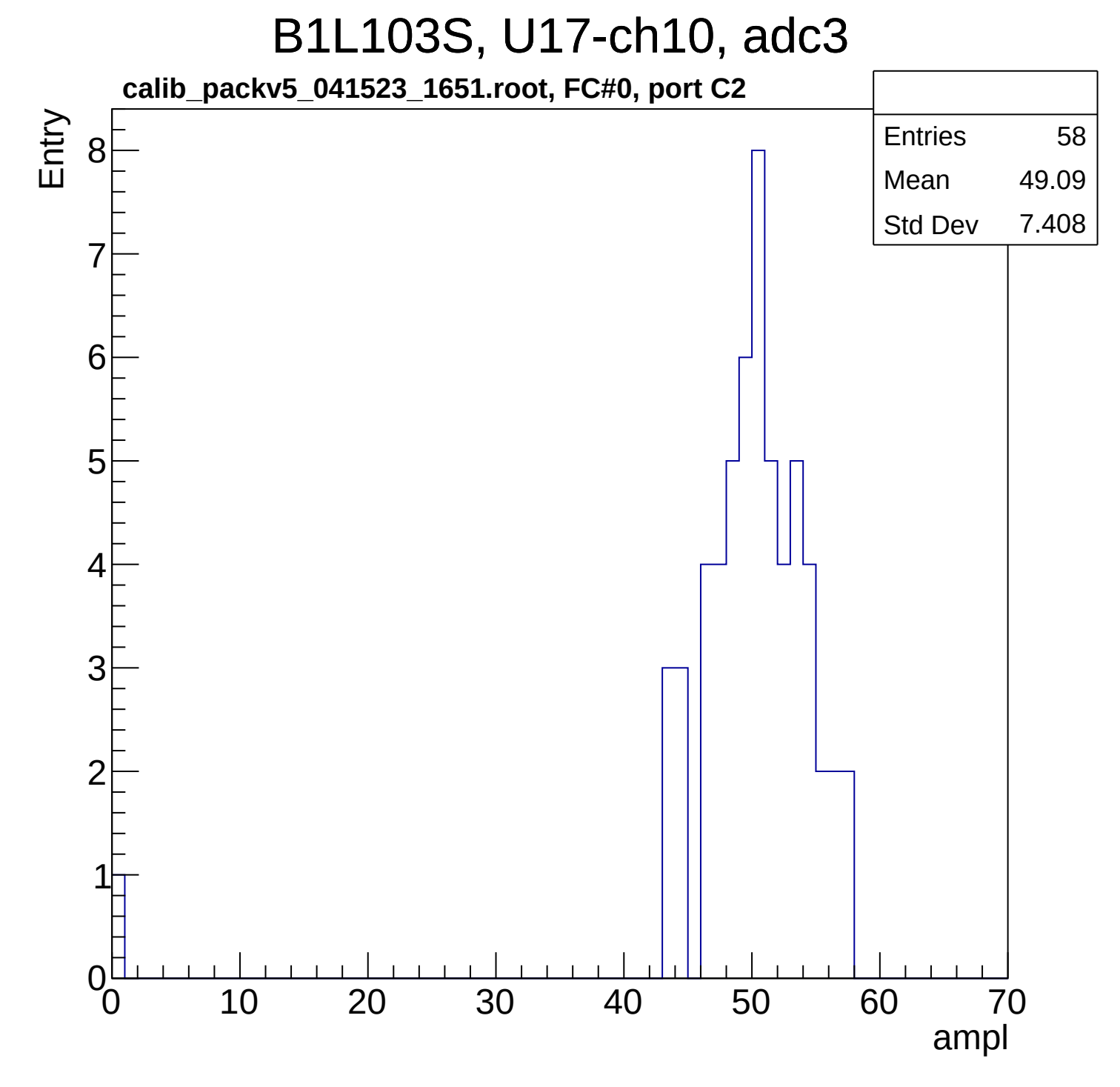

B1L103S, U17-ch9, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.8
Std Dev 0.4
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

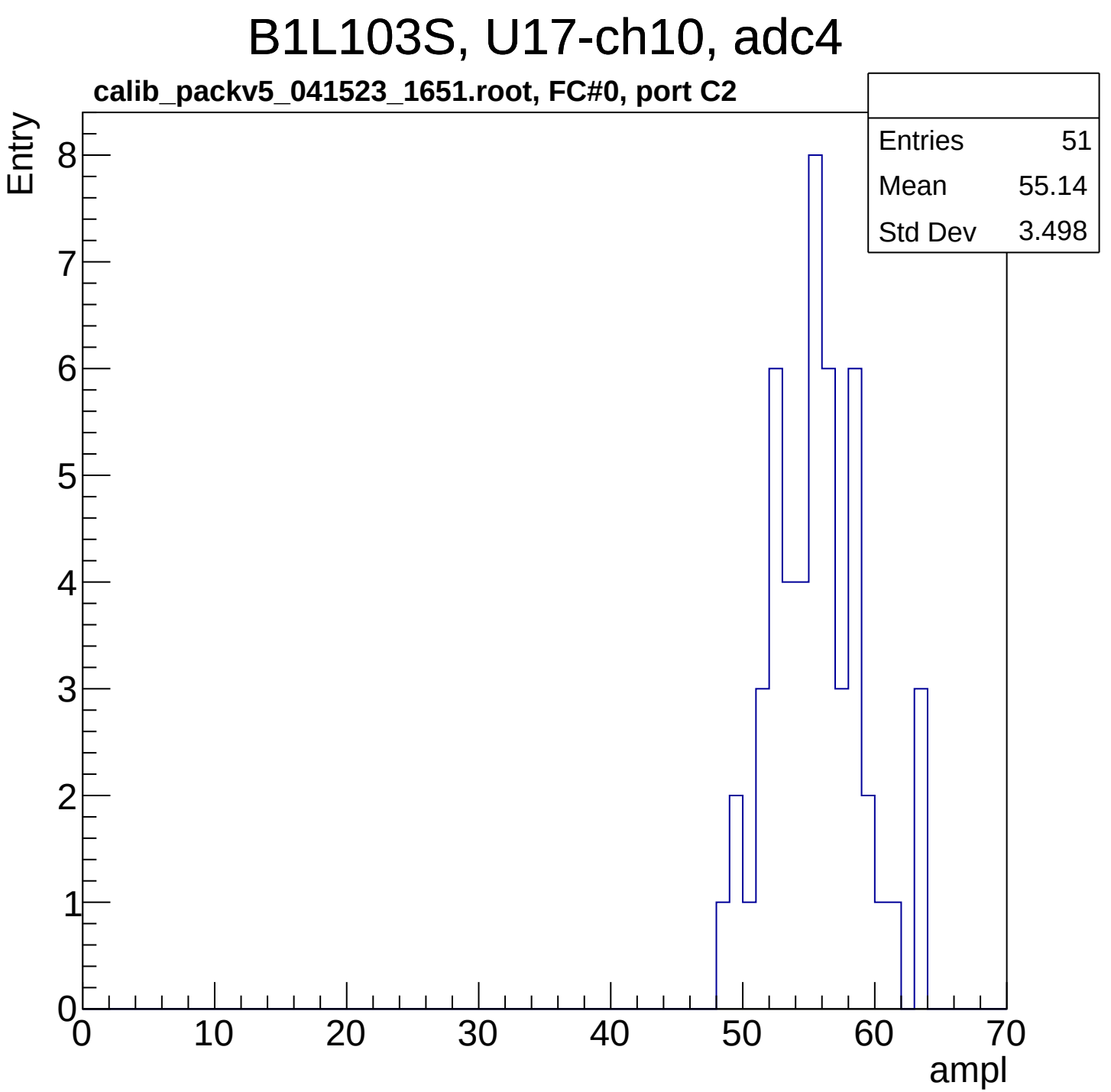

B1L103S, U17-ch9, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

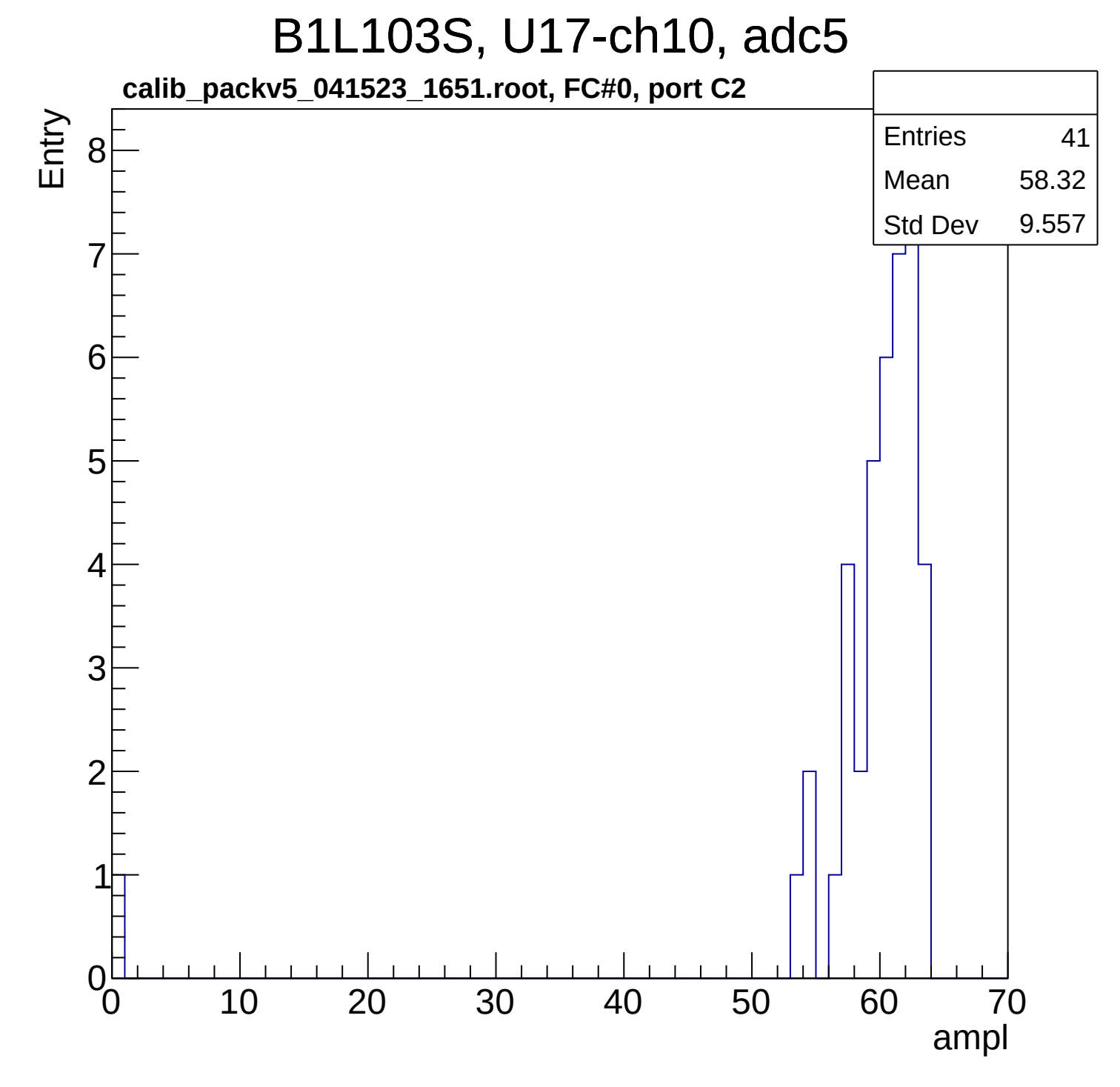

B1L103S, U17-ch10, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 23.3
Std Dev 11.2
Gaus mean : 28.8822
Gaus Width: 4.3556
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

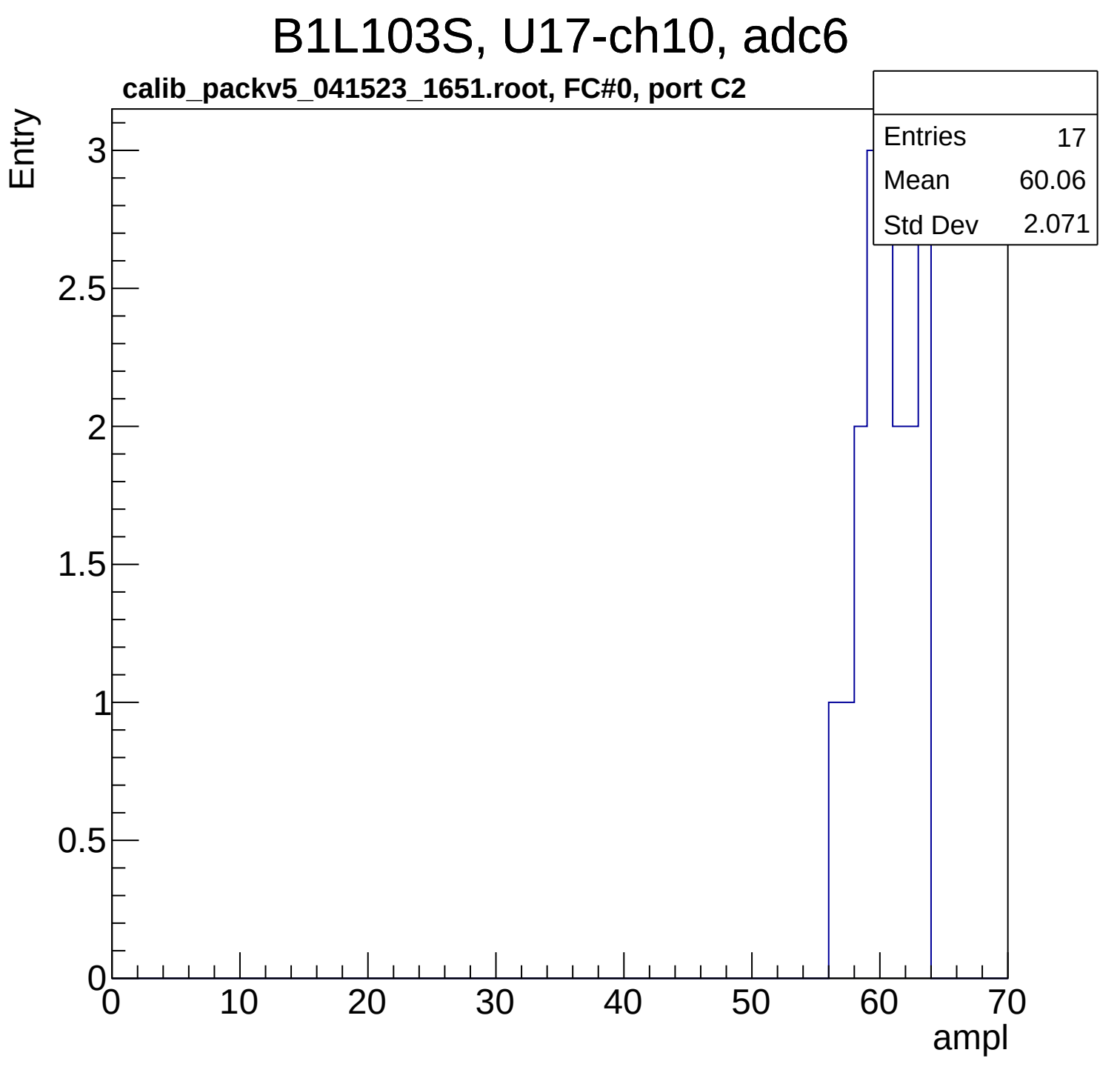

B1L103S, U17-ch10, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 34.99
Std Dev 8.216
Gaus mean : 37.2643
Gaus Width: 5.3092
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

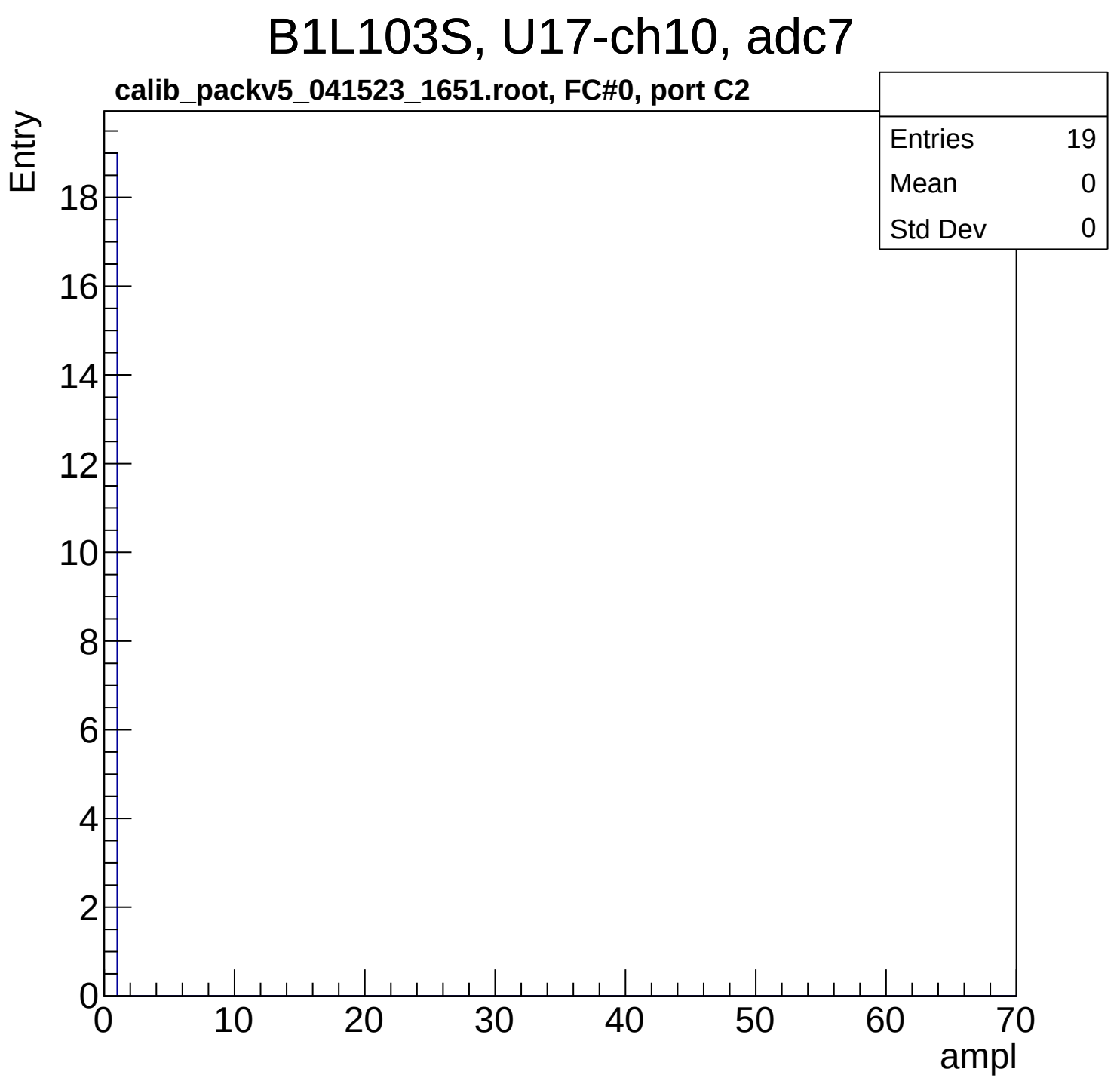

B1L103S, U17-ch10, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 36.87
Std Dev 15.32
Gaus mean : 43.3017
Gaus Width: 4.6176
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

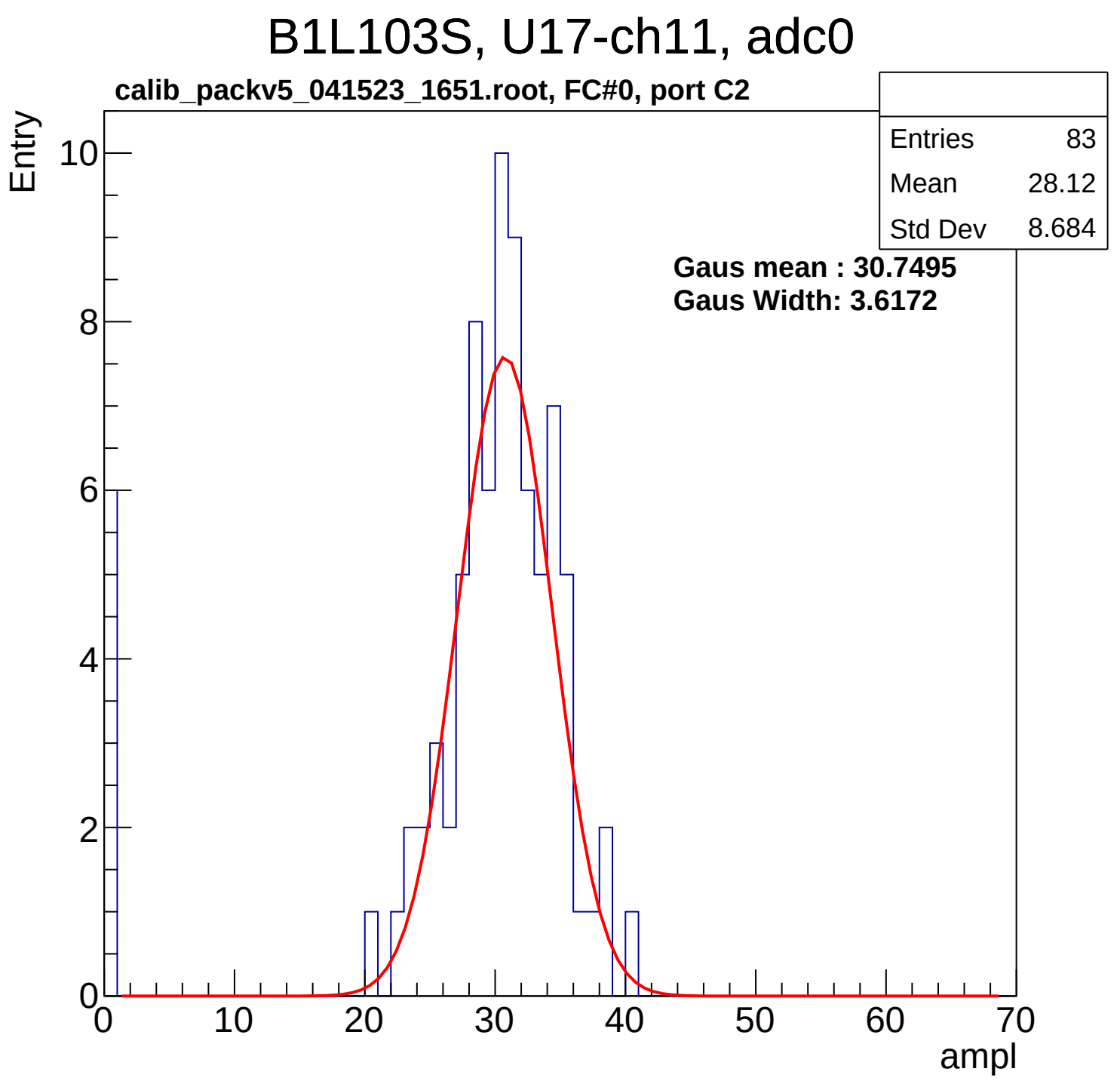

B1L103S, U17-ch10, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 49.09
Std Dev 7.408
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

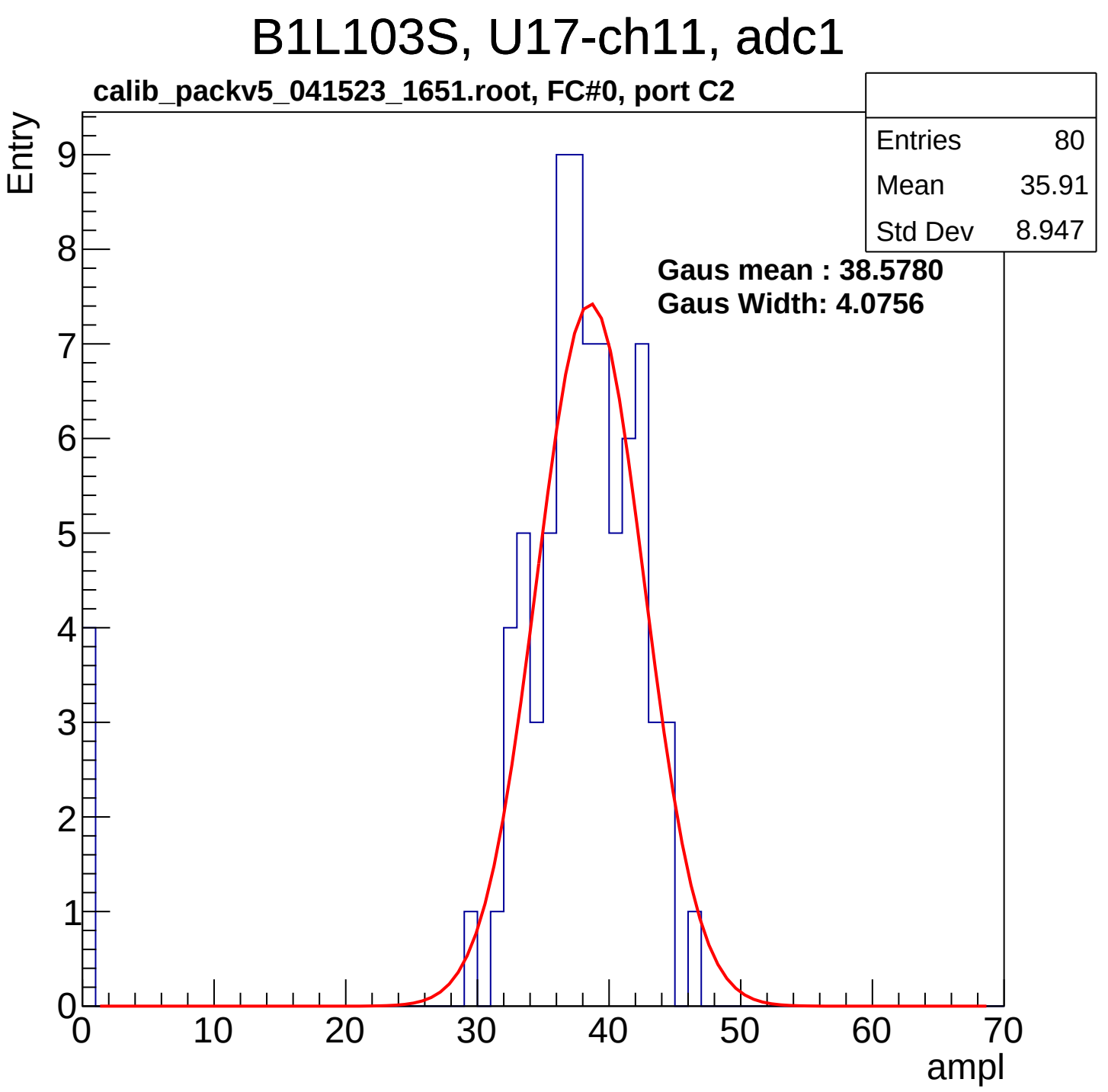

B1L103S, U17-ch10, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 55.14
Std Dev 3.498
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

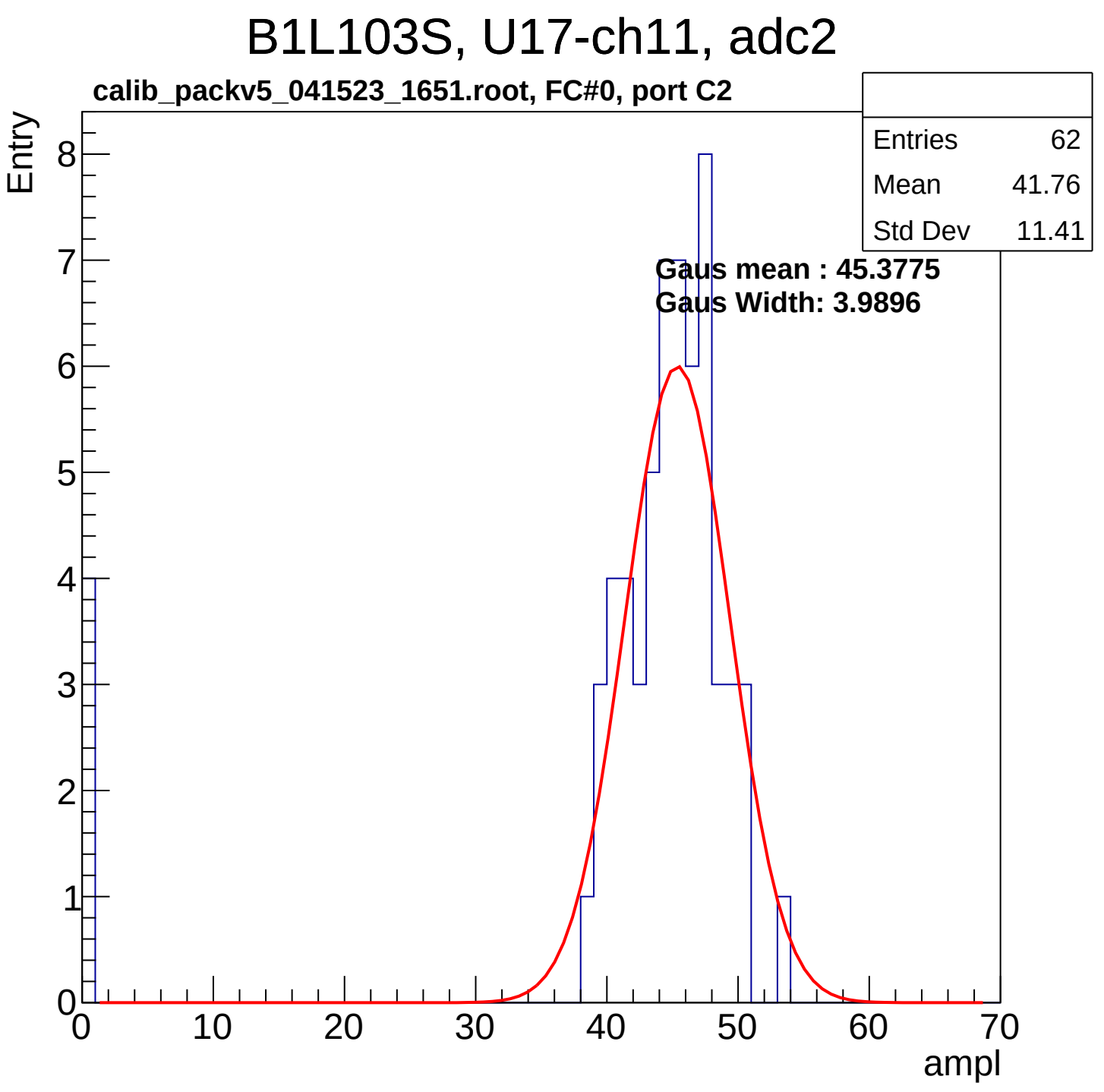

B1L103S, U17-ch10, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 58.32
Std Dev 9.557
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

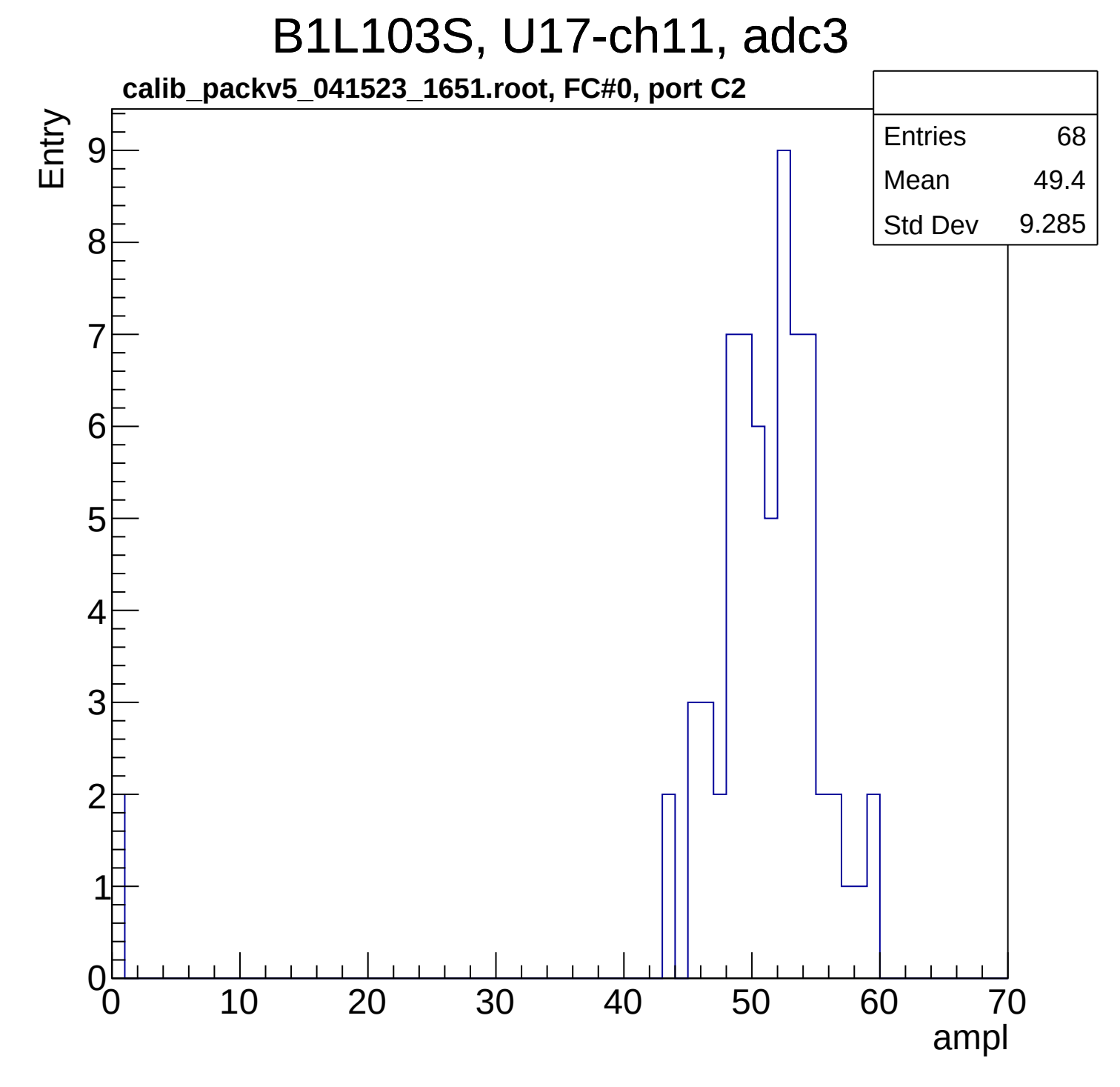

B1L103S, U17-ch10, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 60.06
Std Dev 2.071
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

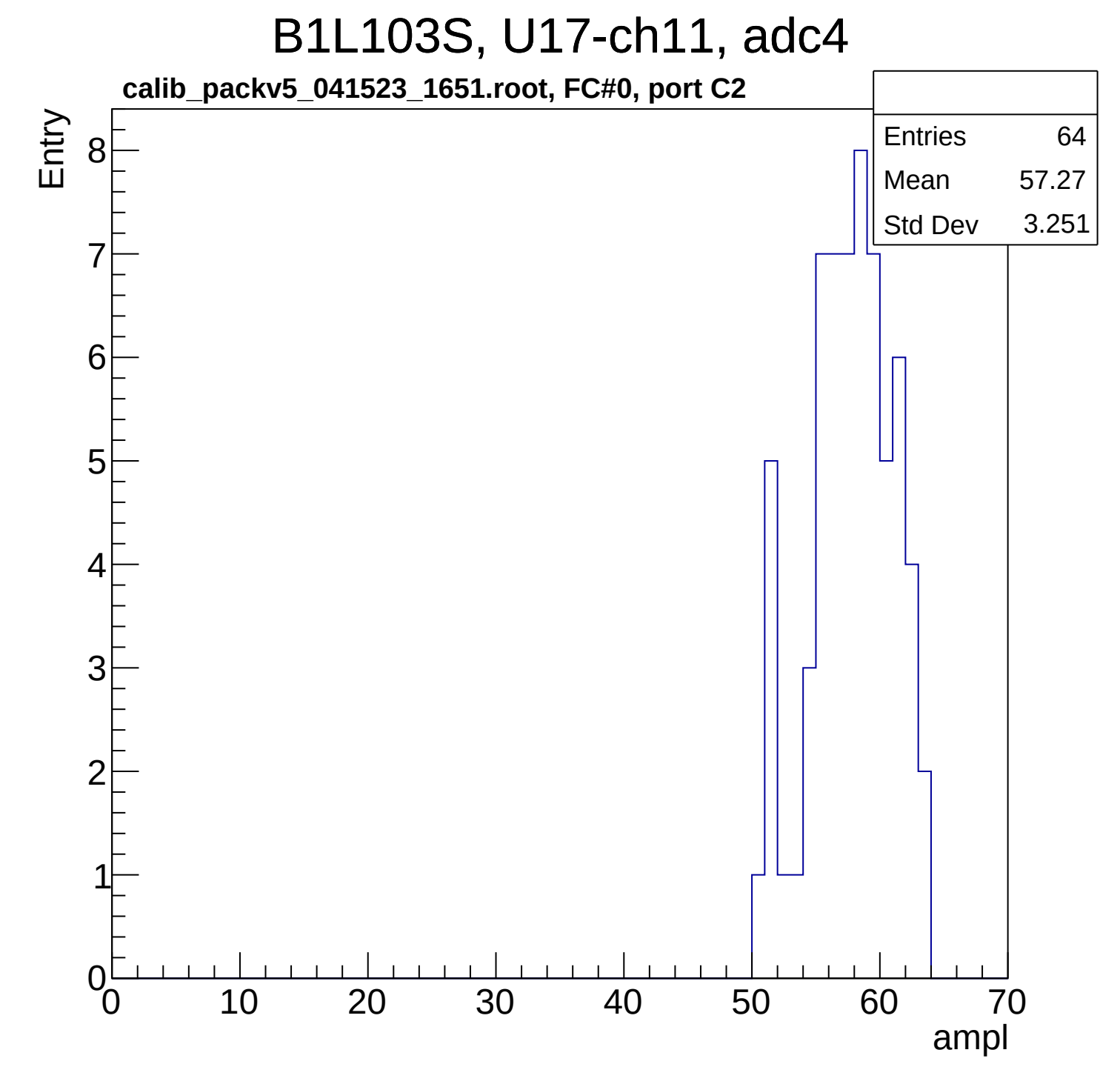

B1L103S, U17-ch10, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

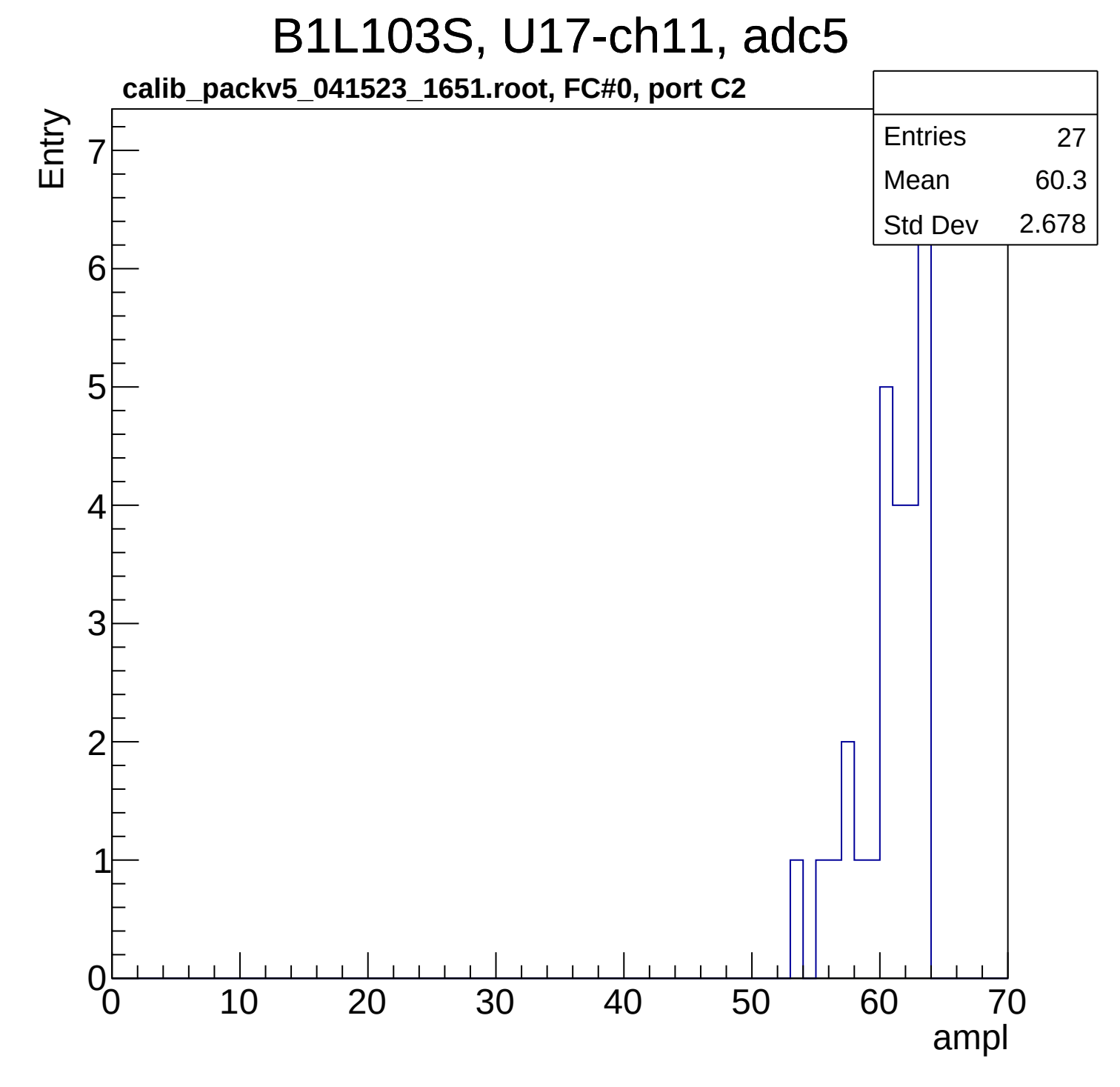

B1L103S, U17-ch11, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 28.12
Std Dev 8.684
Gaus mean : 30.7495
Gaus Width: 3.6172
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

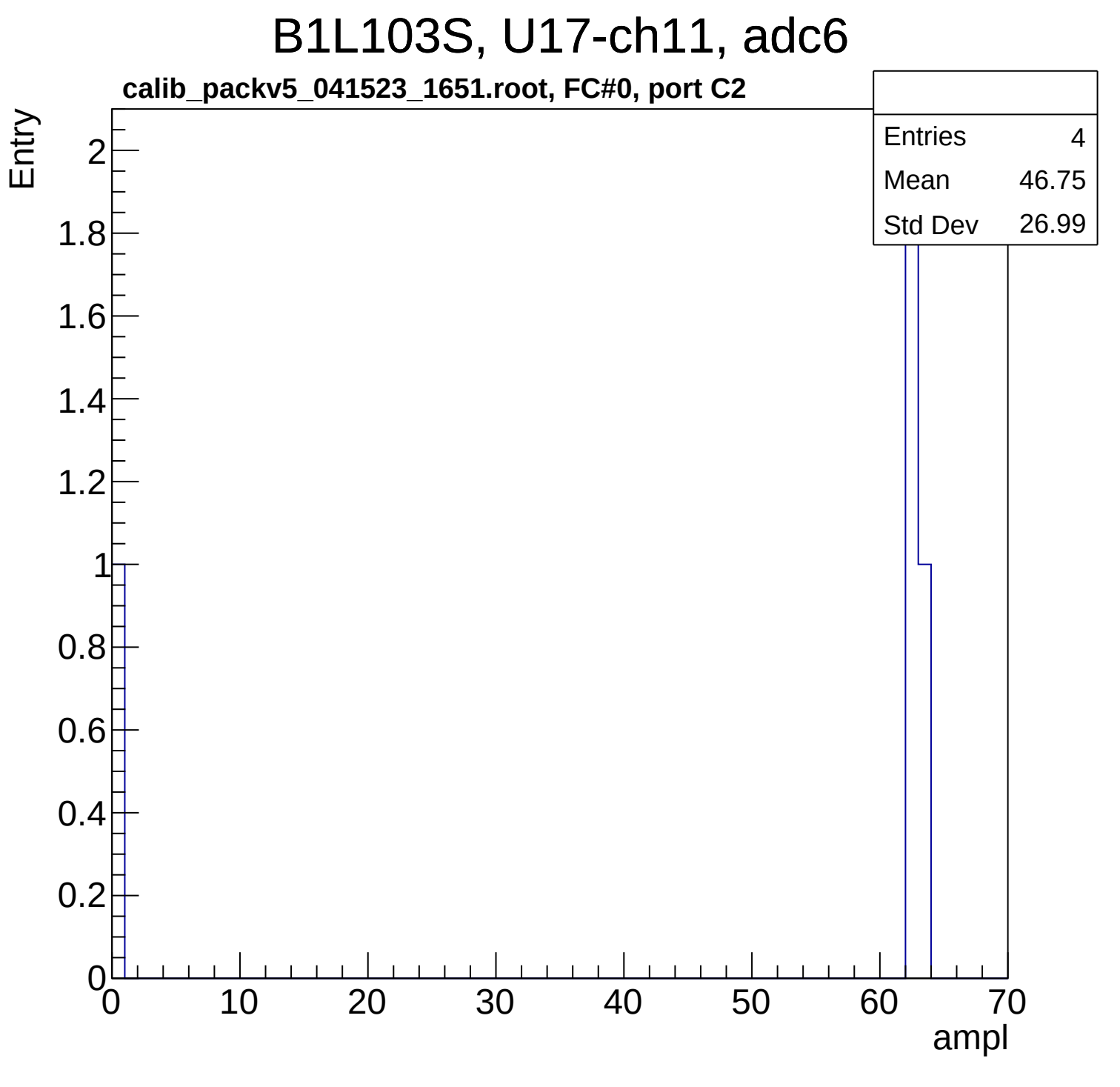

B1L103S, U17-ch11, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 35.91
Std Dev 8.947
Gaus mean : 38.5780
Gaus Width: 4.0756
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

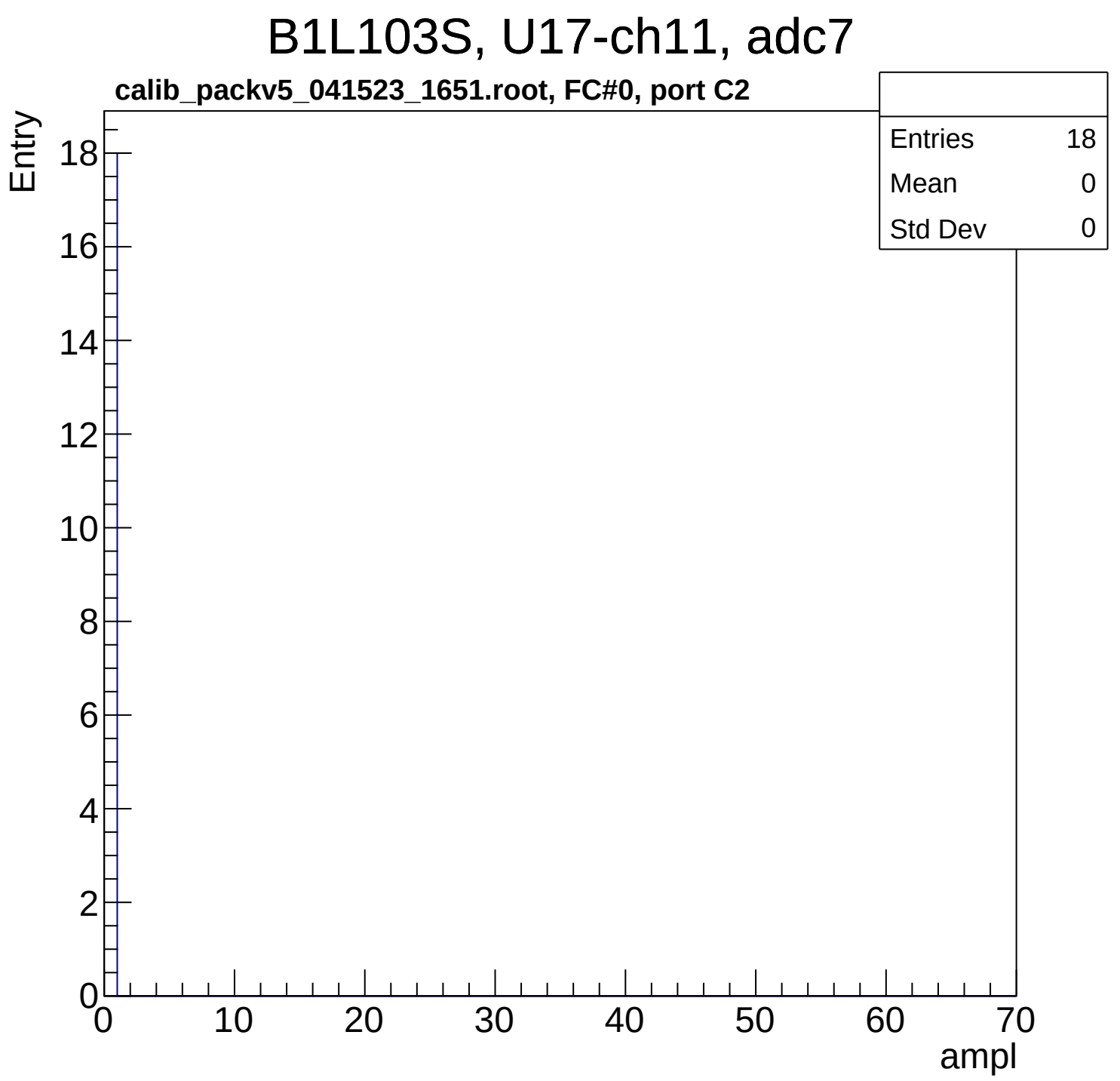

B1L103S, U17-ch11, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 41.76
Std Dev 11.41
Gaus mean : 45.3775
Gaus Width: 3.9896
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

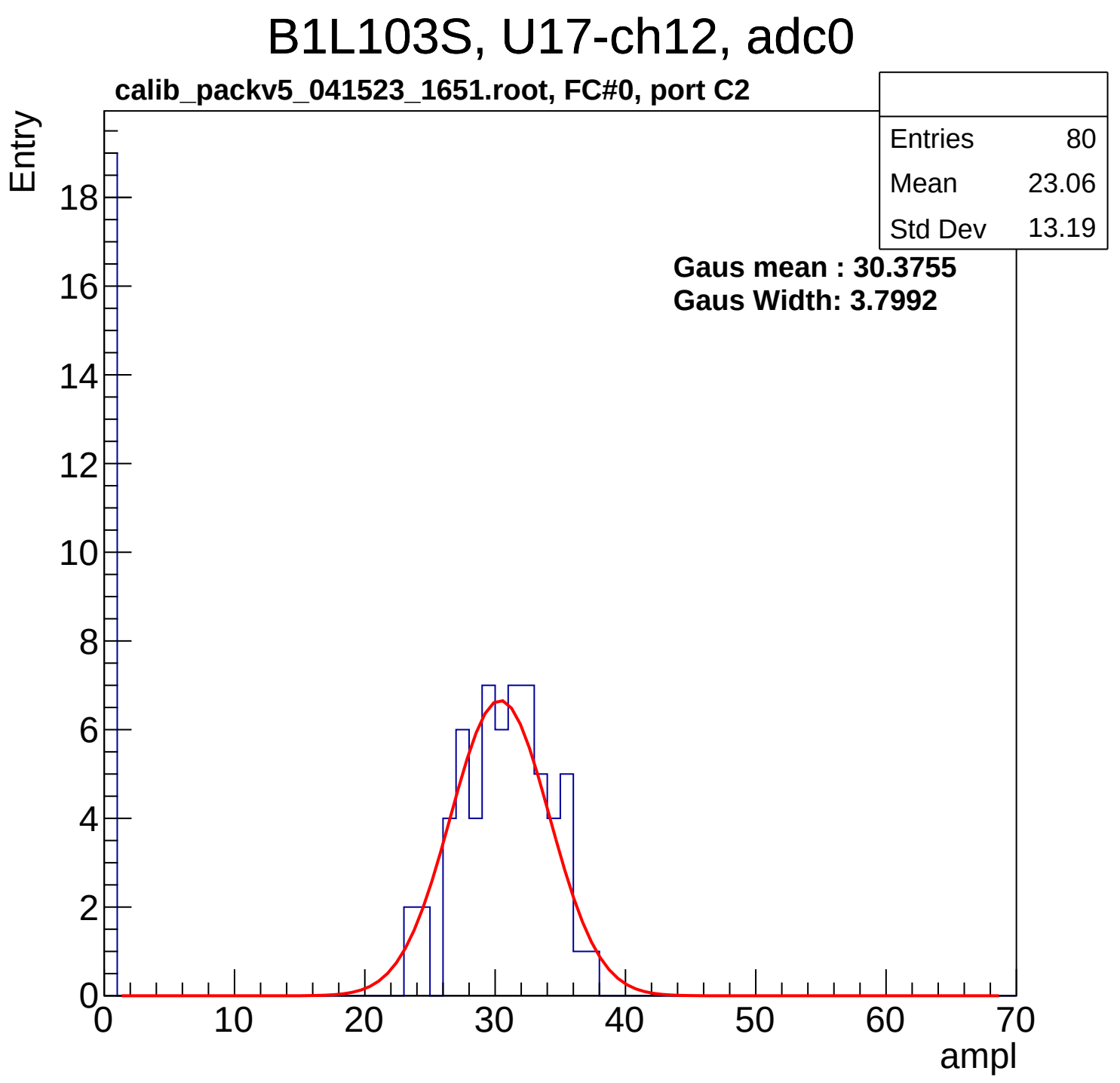

B1L103S, U17-ch11, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 49.4
Std Dev 9.285
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

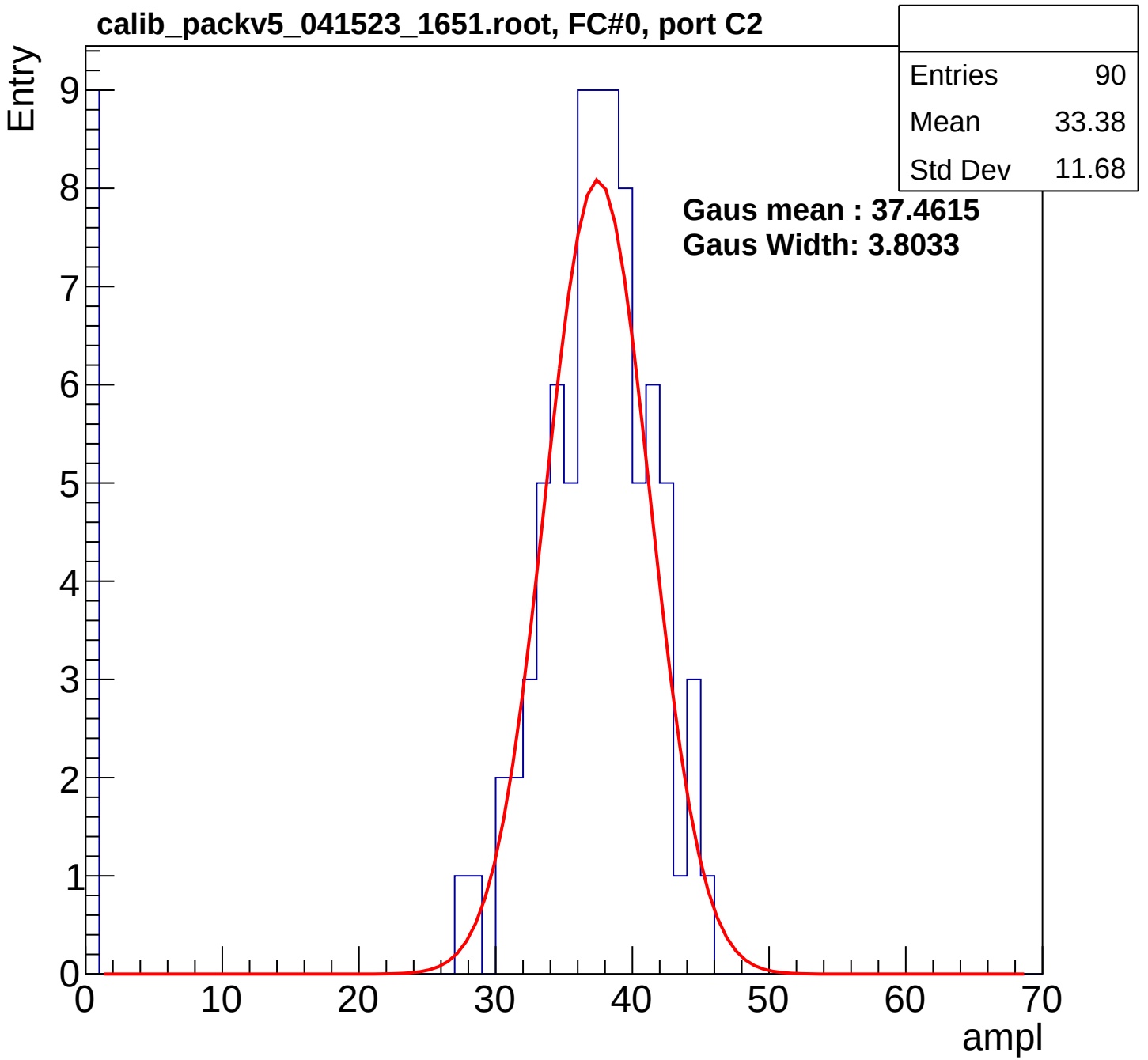

B1L103S, U17-ch11, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 57.27
Std Dev 3.251
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

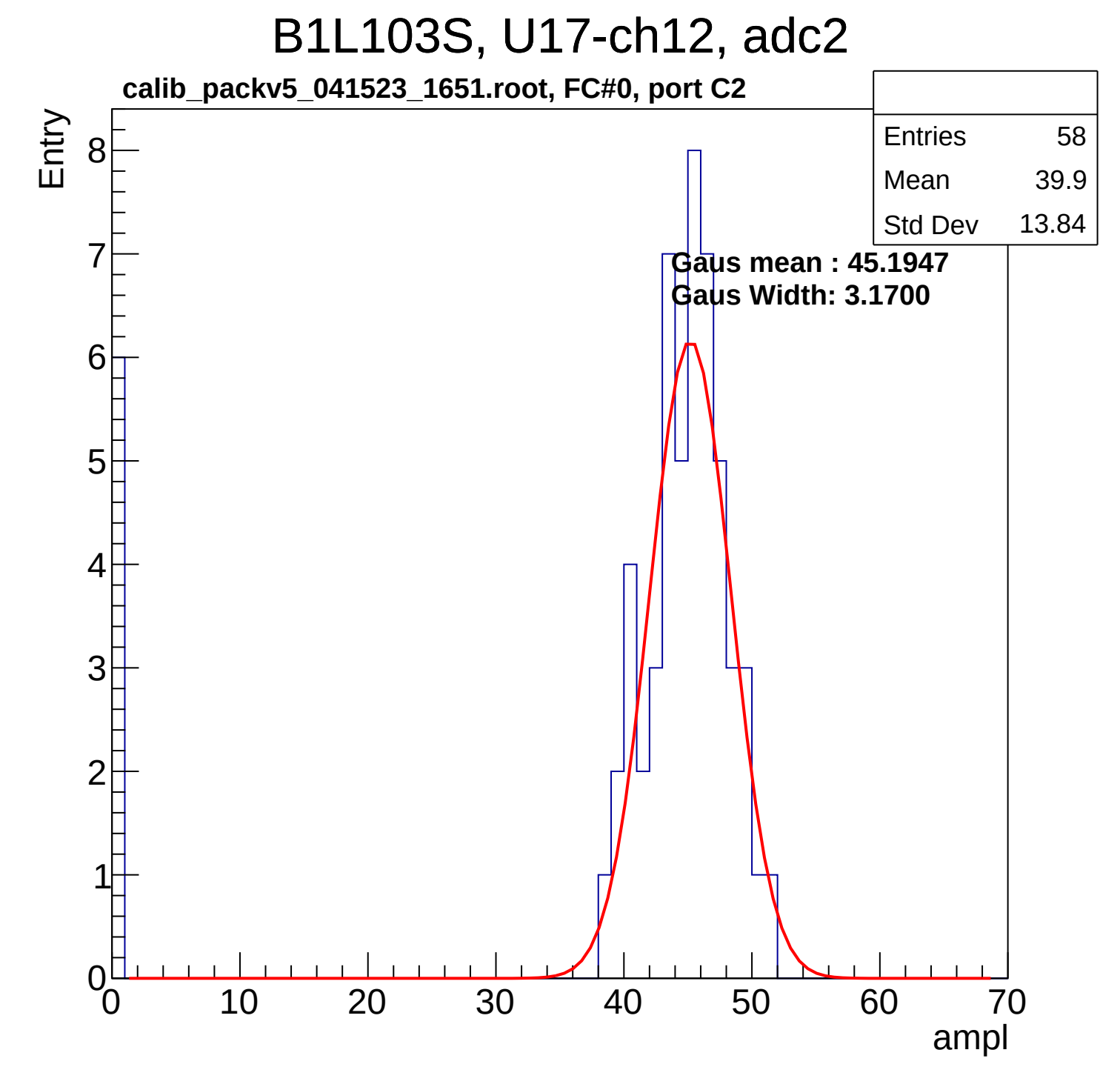

B1L103S, U17-ch11, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 60.3
Std Dev 2.678
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

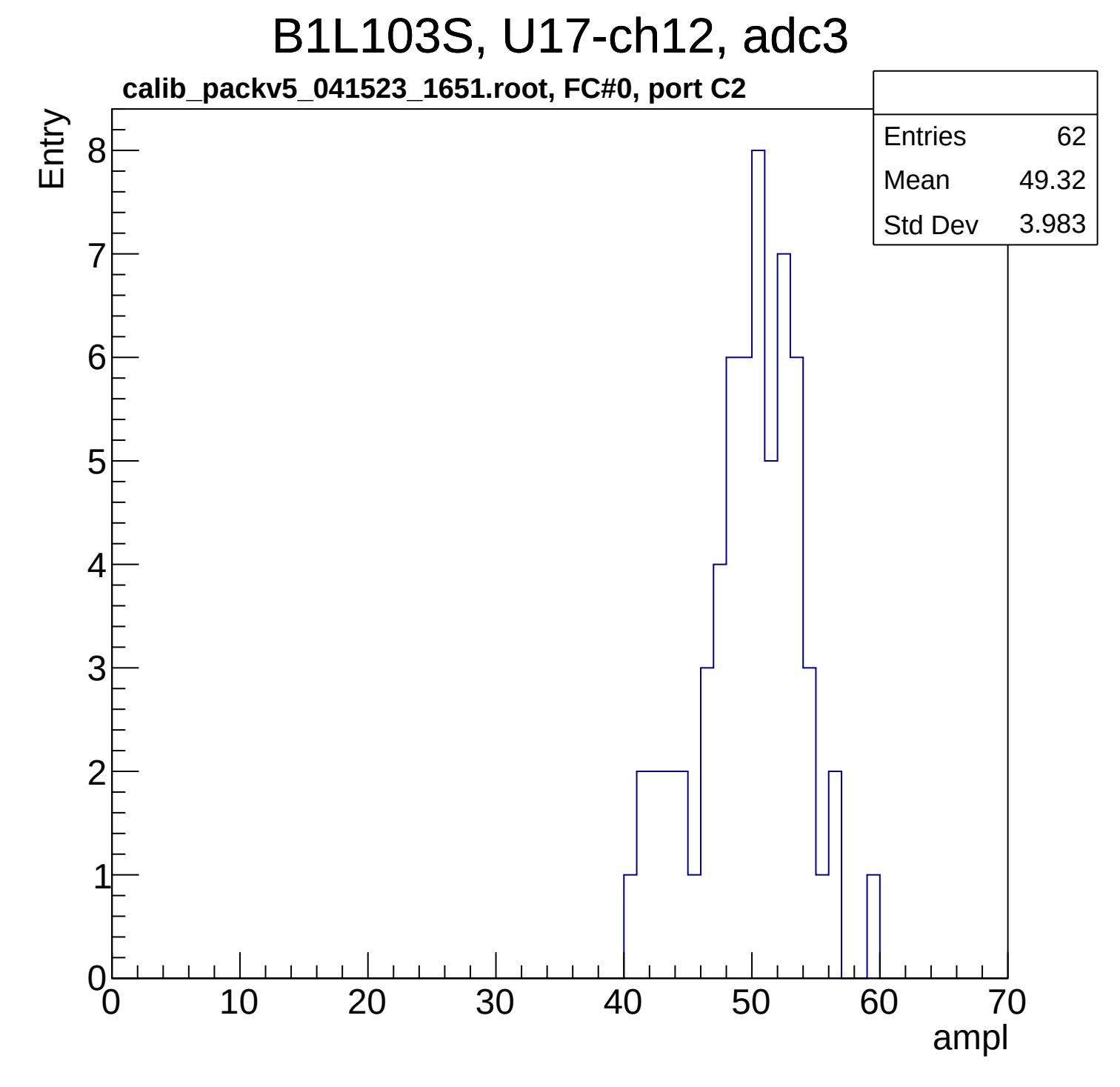

B1L103S, U17-ch11, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 46.75
Std Dev 26.99
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

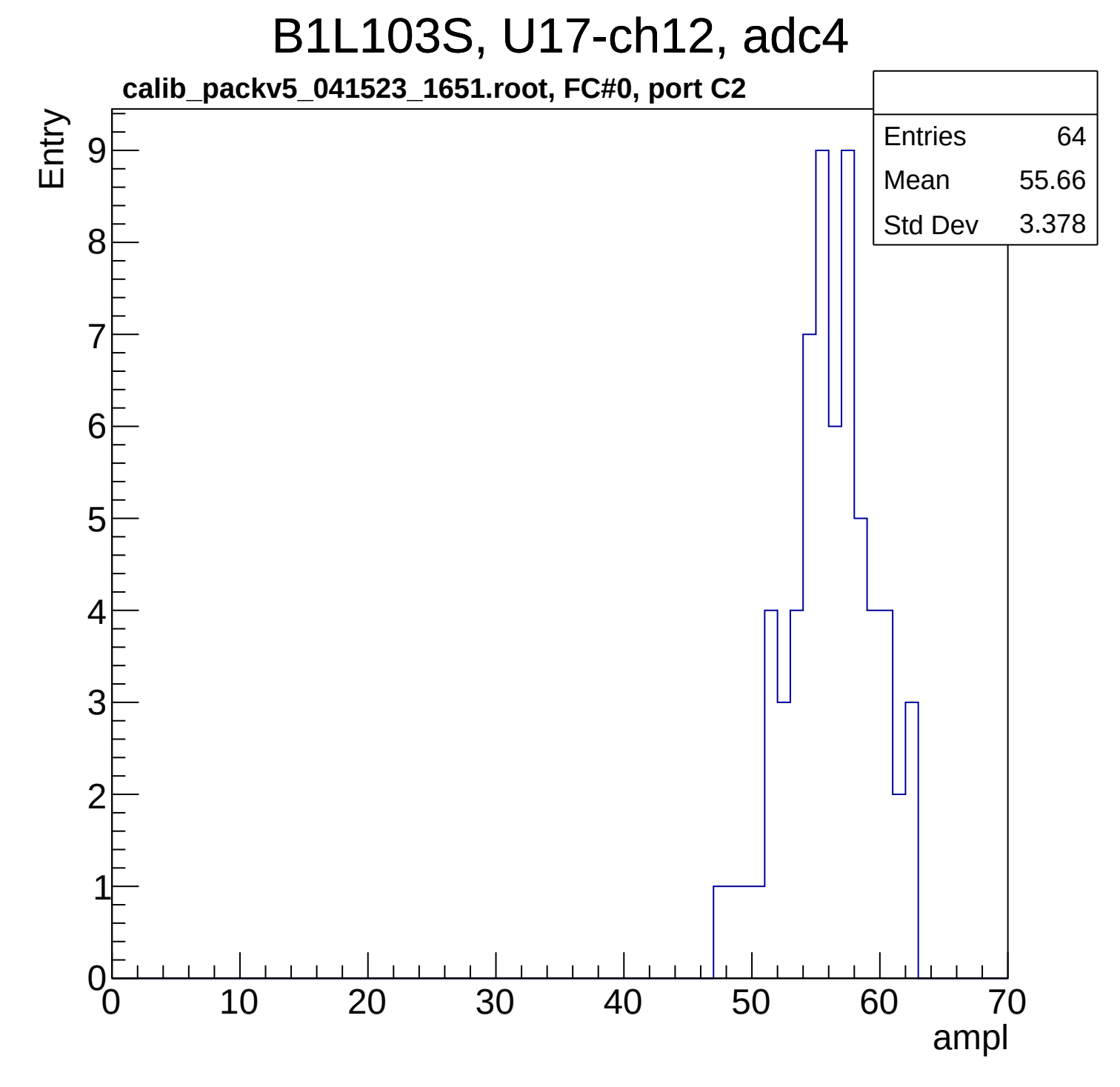

B1L103S, U17-ch11, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

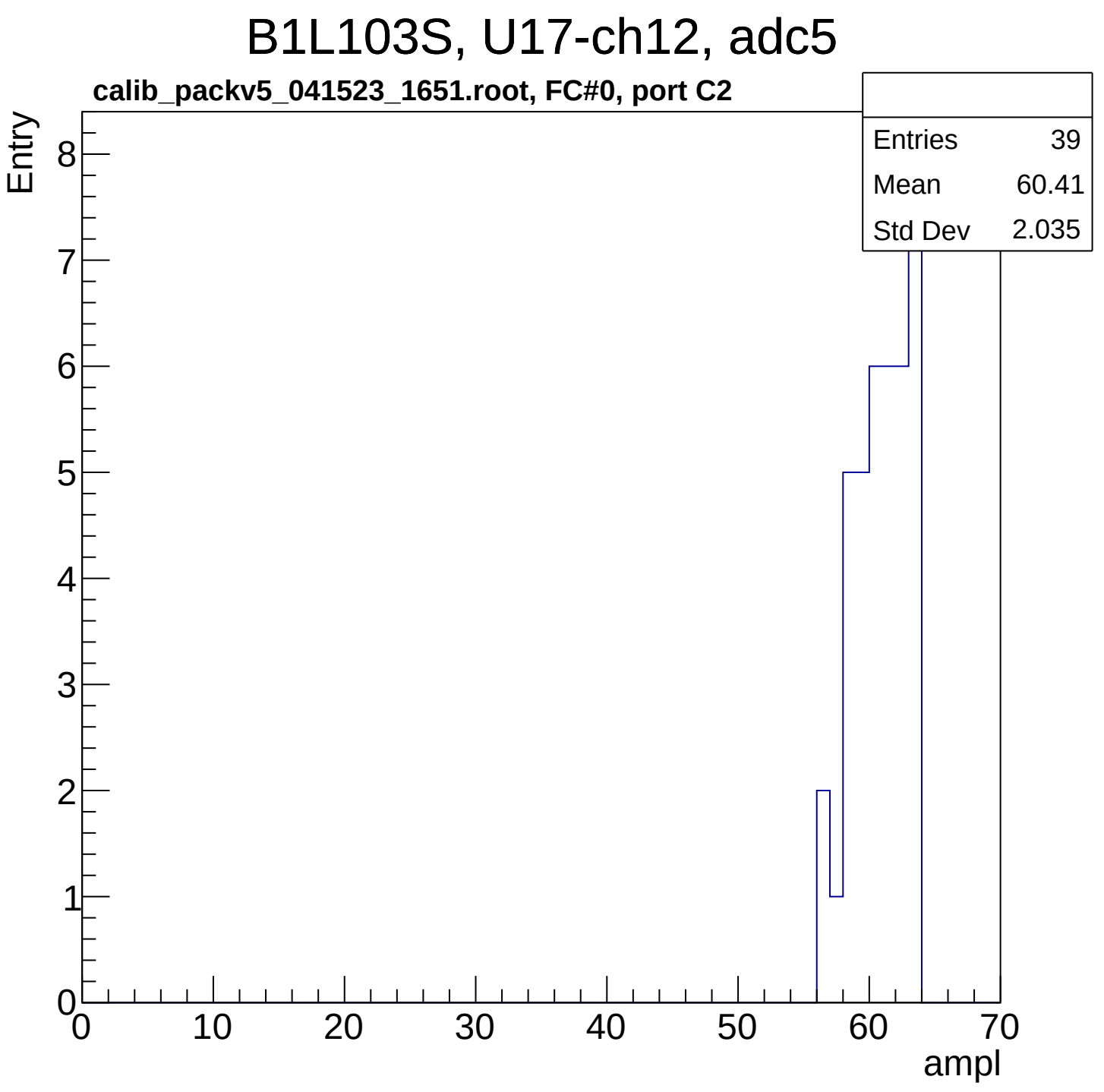

B1L103S, U17-ch12, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 23.06
Std Dev 13.19
Gaus mean : 30.3755
Gaus Width: 3.7992
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

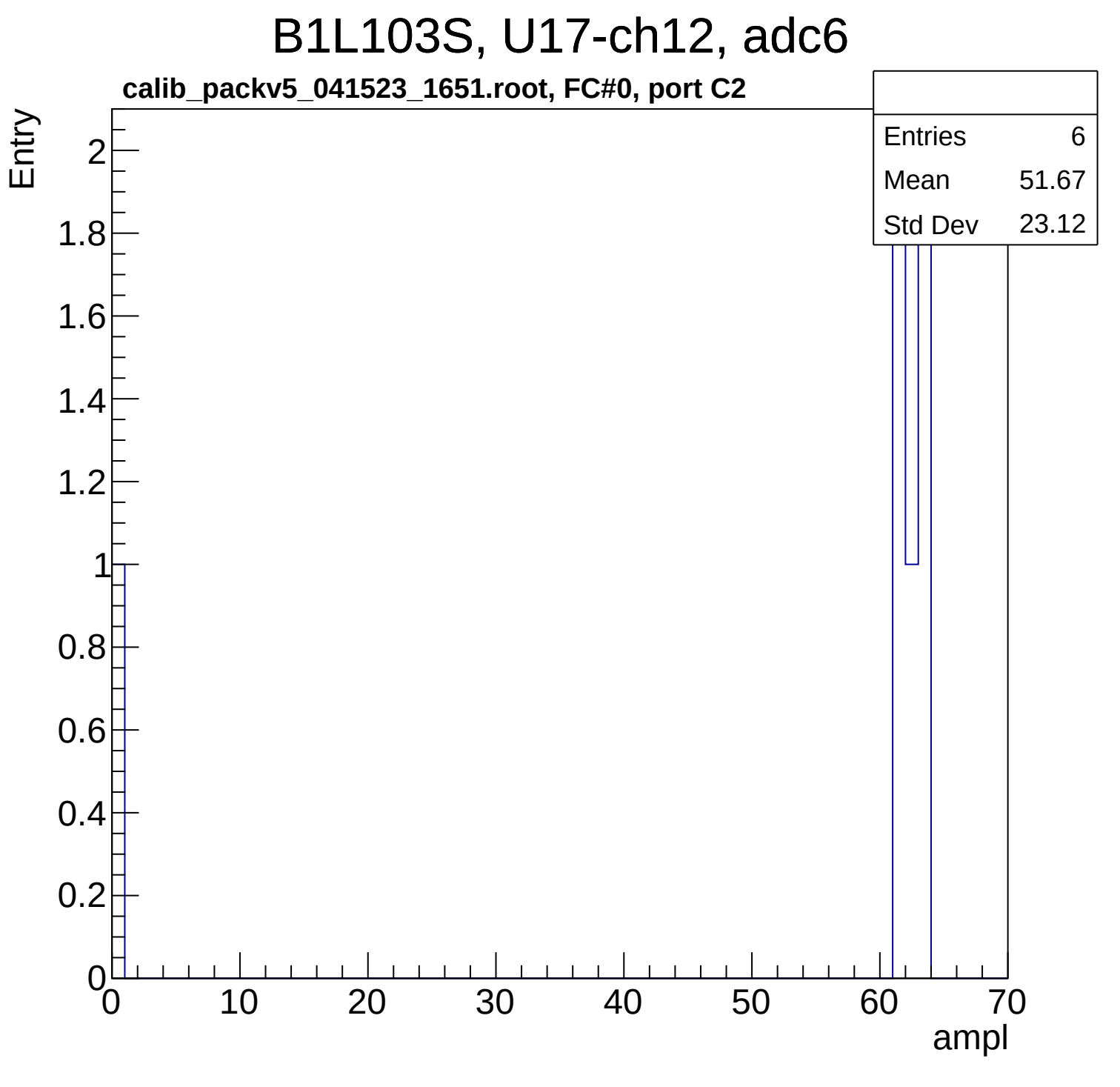

B1L103S, U17-ch12, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 33.38
Std Dev 11.68
Gaus mean : 37.4615
Gaus Width: 3.8033
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

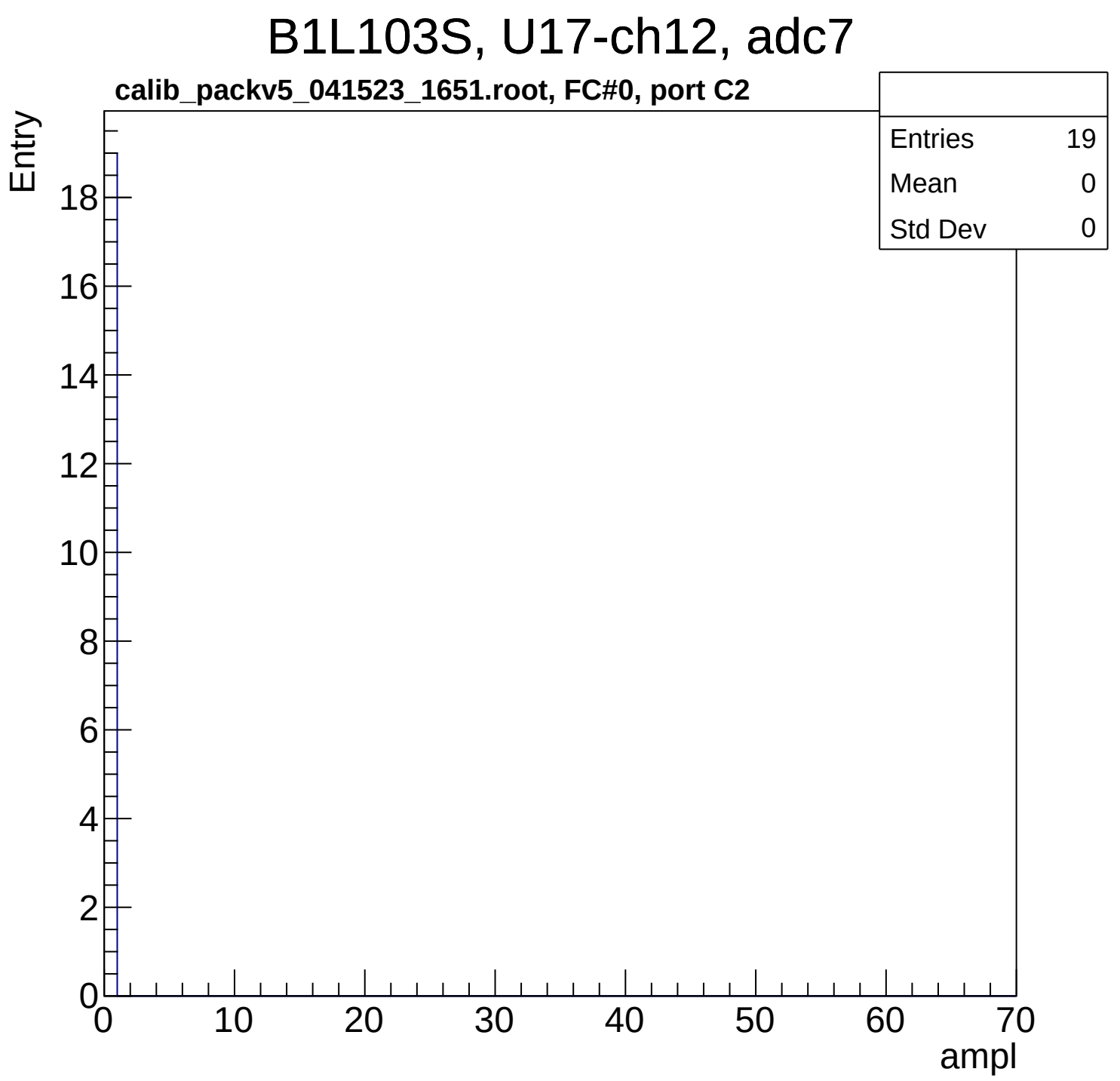

B1L103S, U17-ch12, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 39.9
Std Dev 13.84
Gaus mean : 45.1947
Gaus Width: 3.1700
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

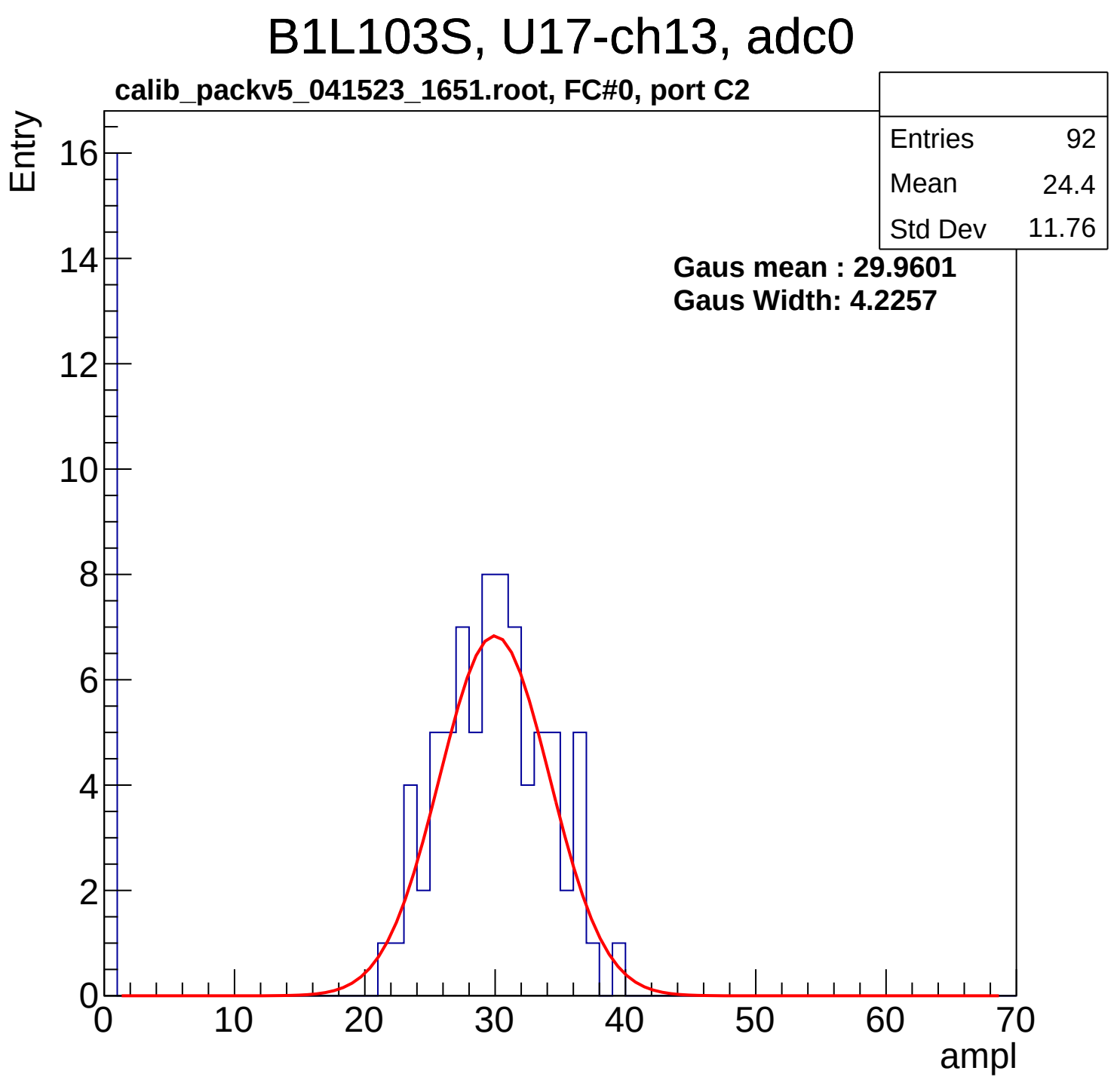

B1L103S, U17-ch12, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 49.32
Std Dev 3.983
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

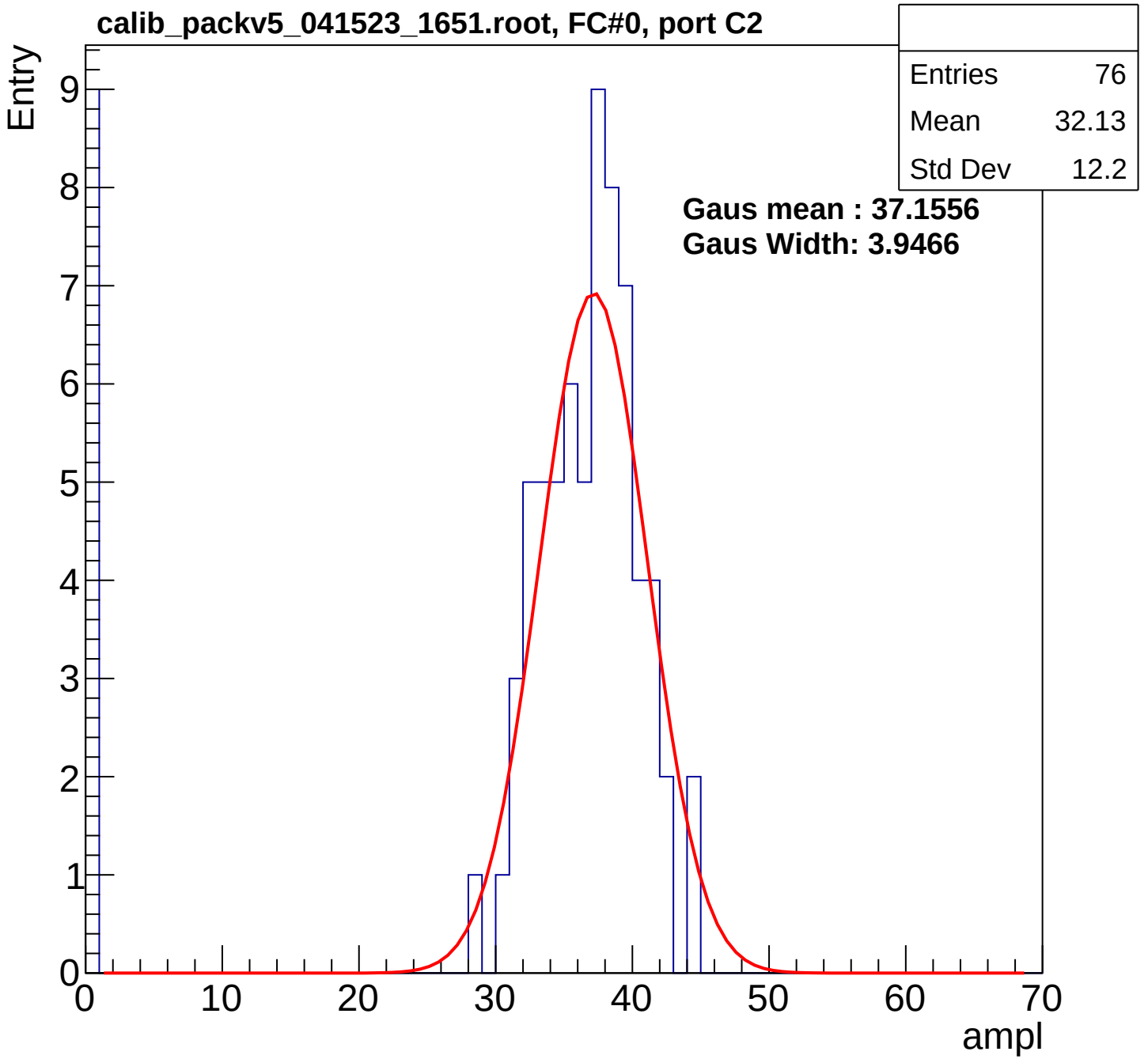

B1L103S, U17-ch12, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 55.66
Std Dev 3.378
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

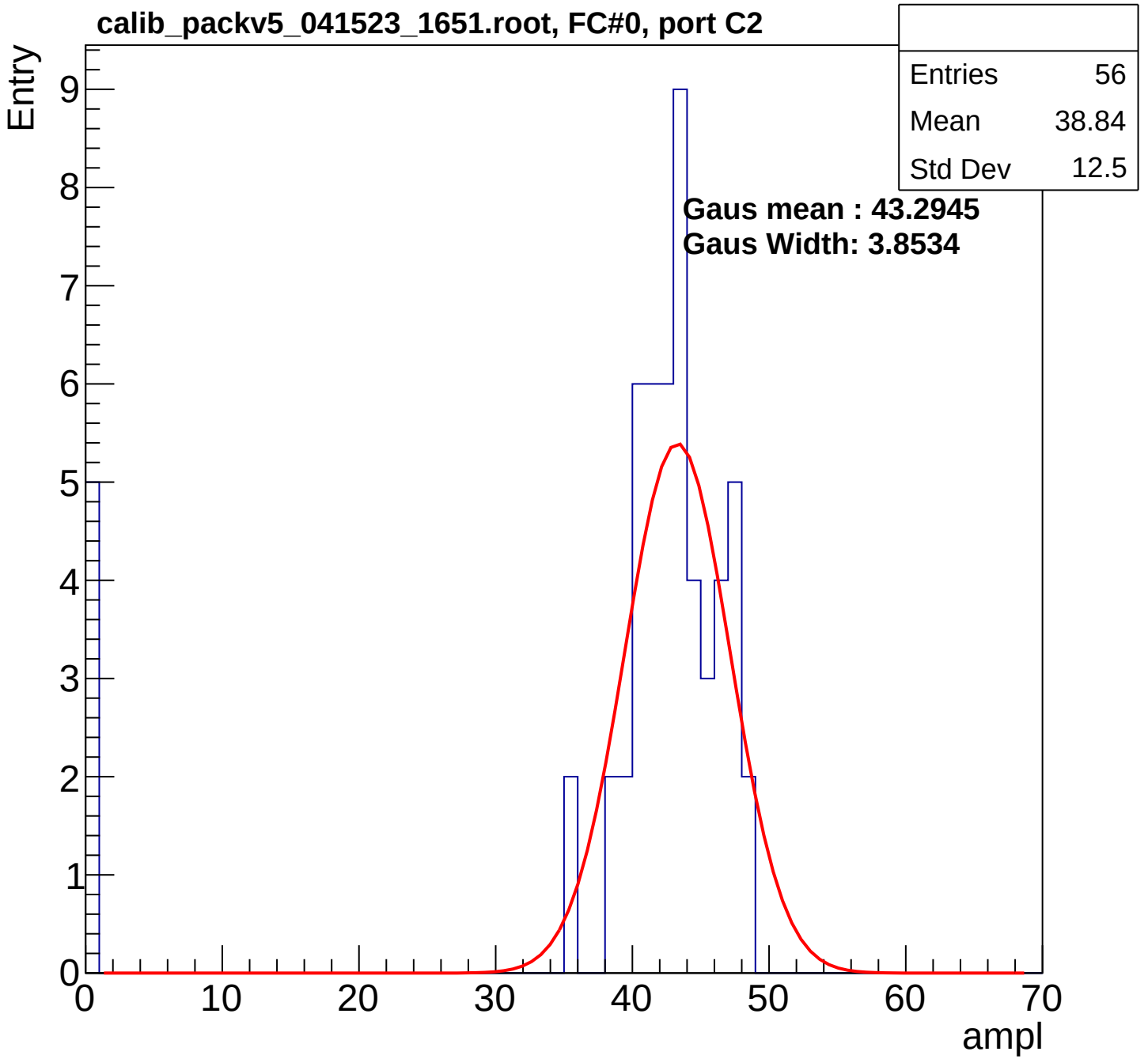

B1L103S, U17-ch12, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 60.41
Std Dev 2.035
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

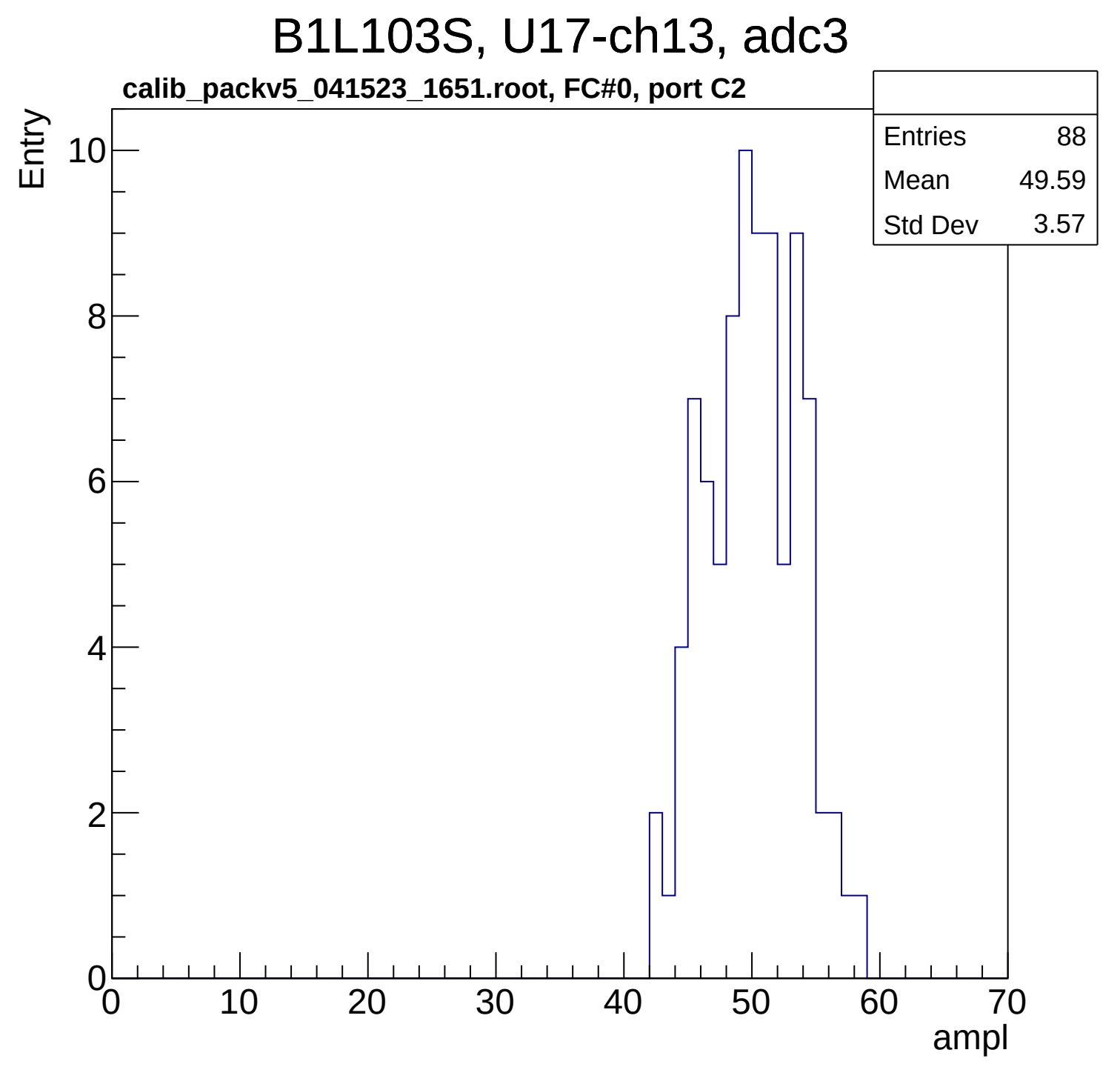

B1L103S, U17-ch12, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 51.67
Std Dev 23.12
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

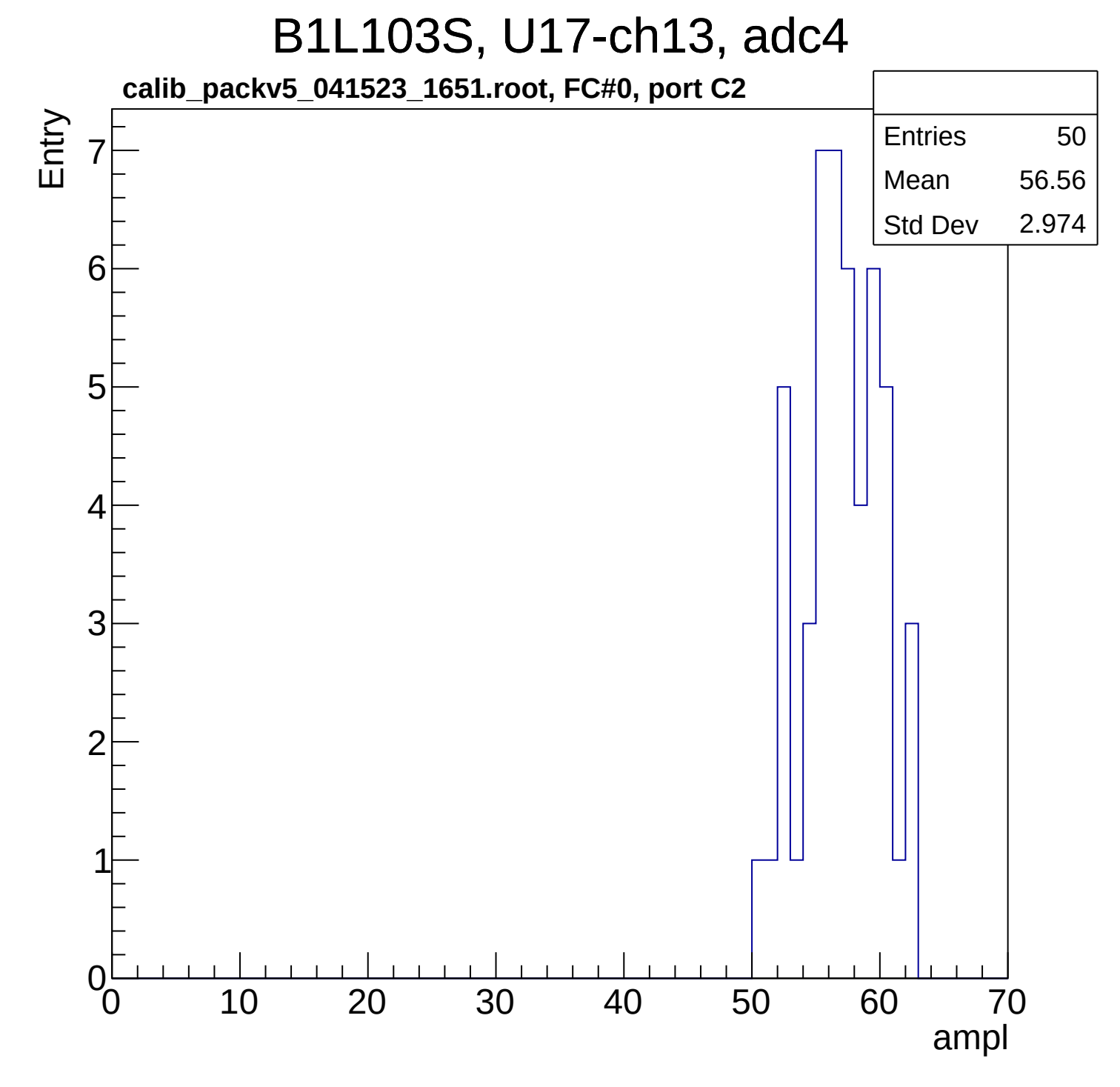

B1L103S, U17-ch12, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

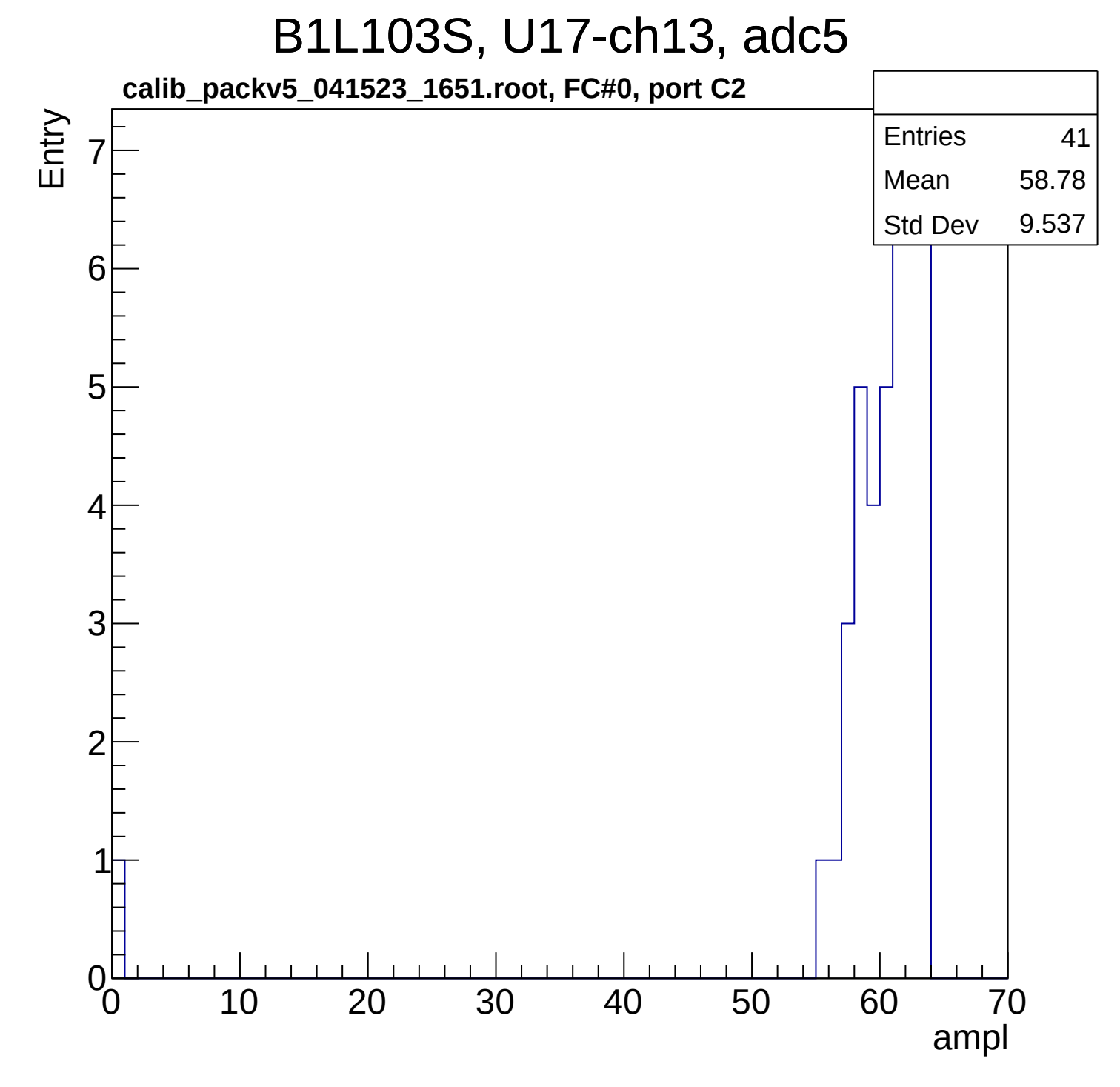

B1L103S, U17-ch13, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 24.4
Std Dev 11.76
Gaus mean : 29.9601
Gaus Width: 4.2257
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

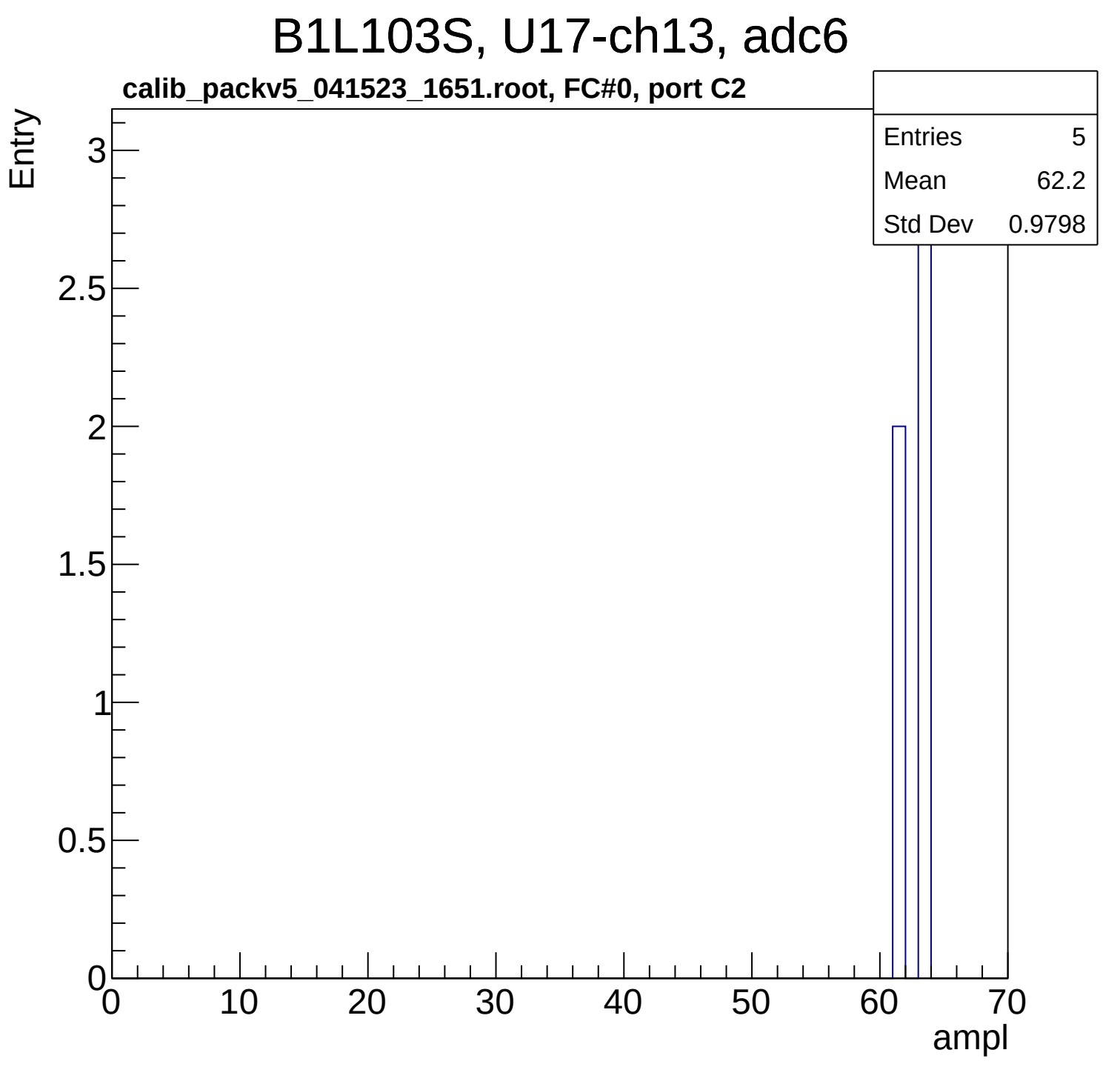

B1L103S, U17-ch13, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 32.13
Std Dev 12.2
Gaus mean : 37.1556
Gaus Width: 3.9466
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

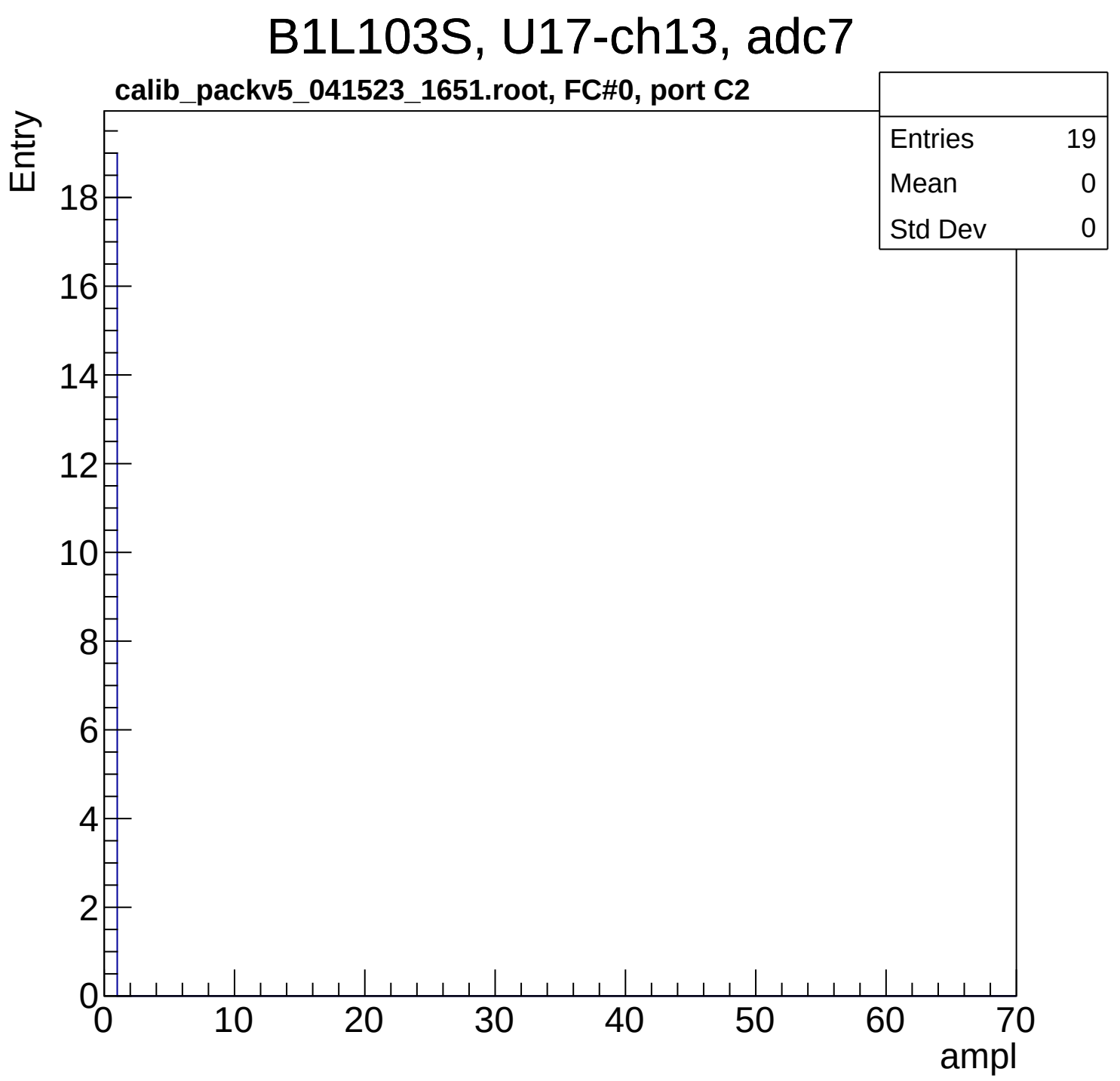

B1L103S, U17-ch13, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 38.84
Std Dev 12.5
Gaus mean : 43.2945
Gaus Width: 3.8534
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

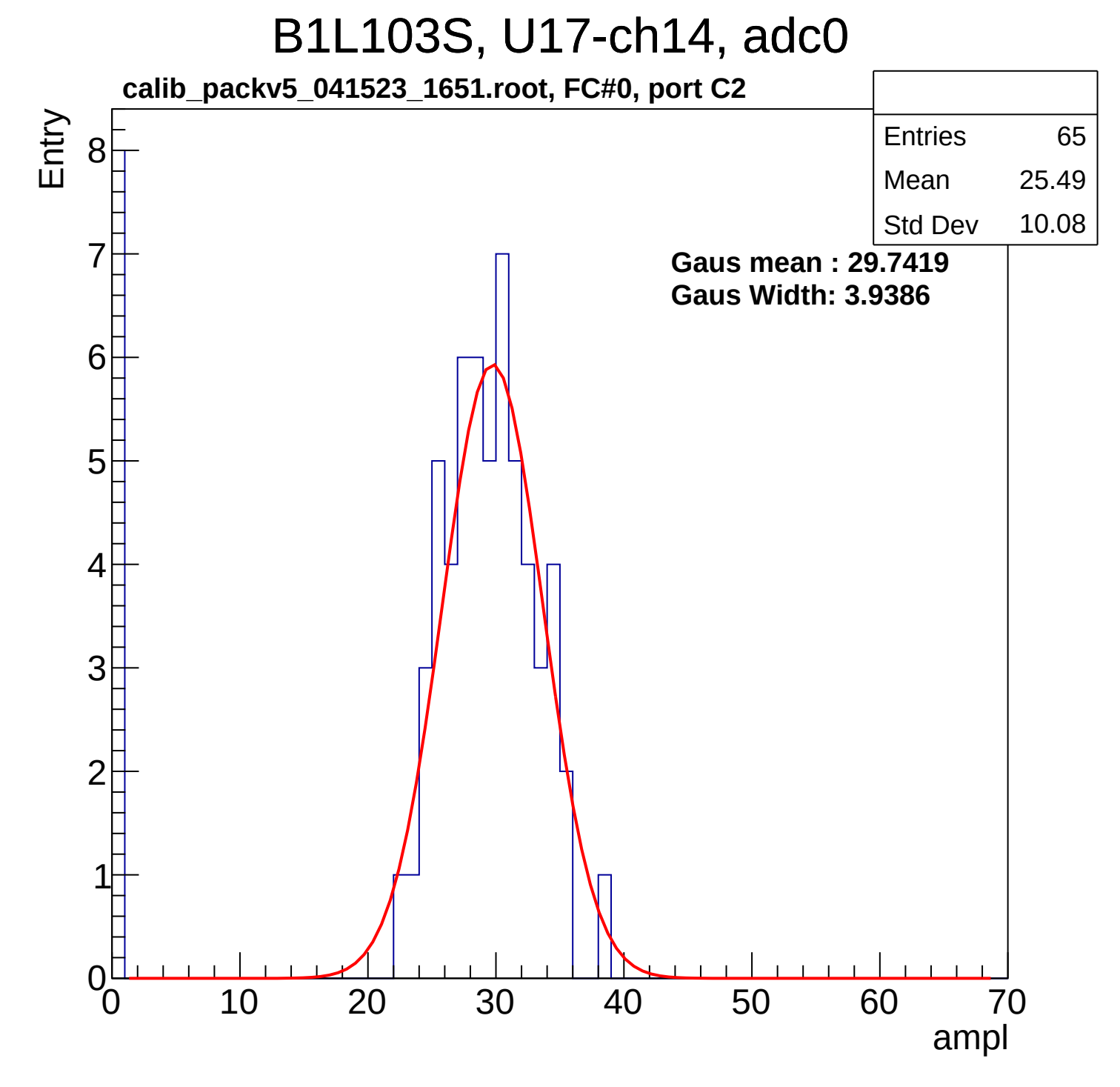

B1L103S, U17-ch13, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 49.59
Std Dev 3.57
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

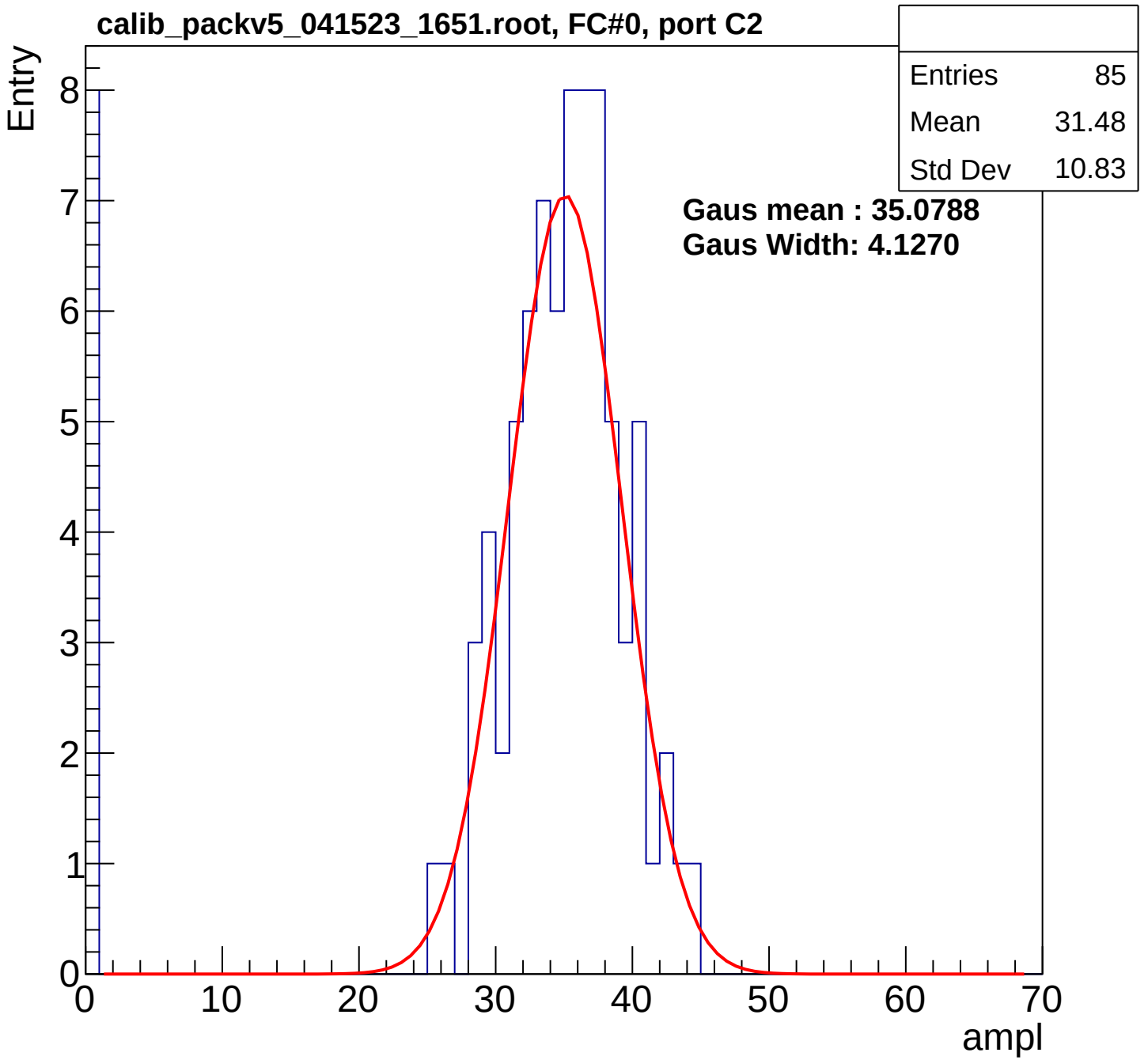

B1L103S, U17-ch13, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 56.56
Std Dev 2.974
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

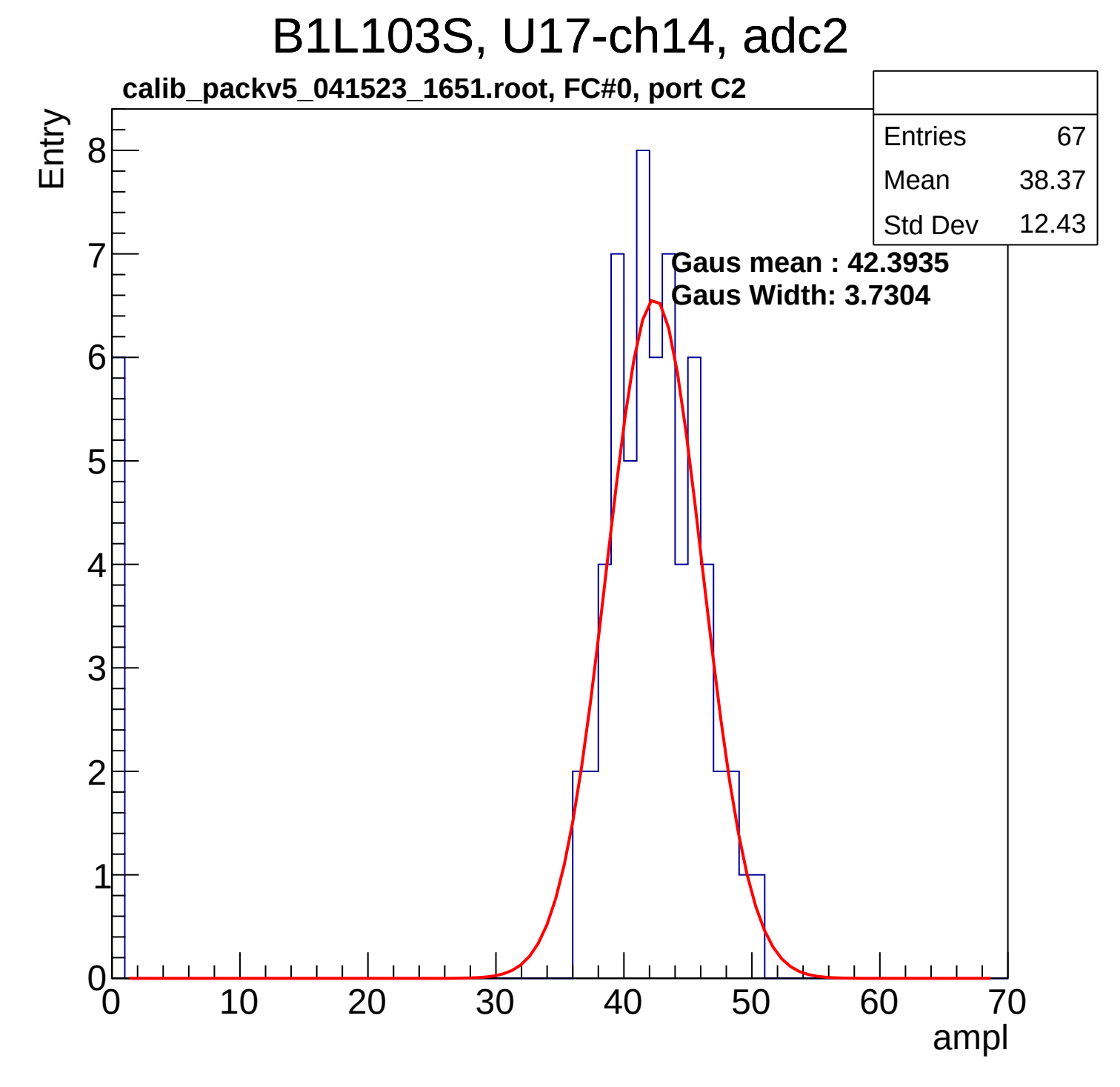

B1L103S, U17-ch13, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 58.78
Std Dev 9.537
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

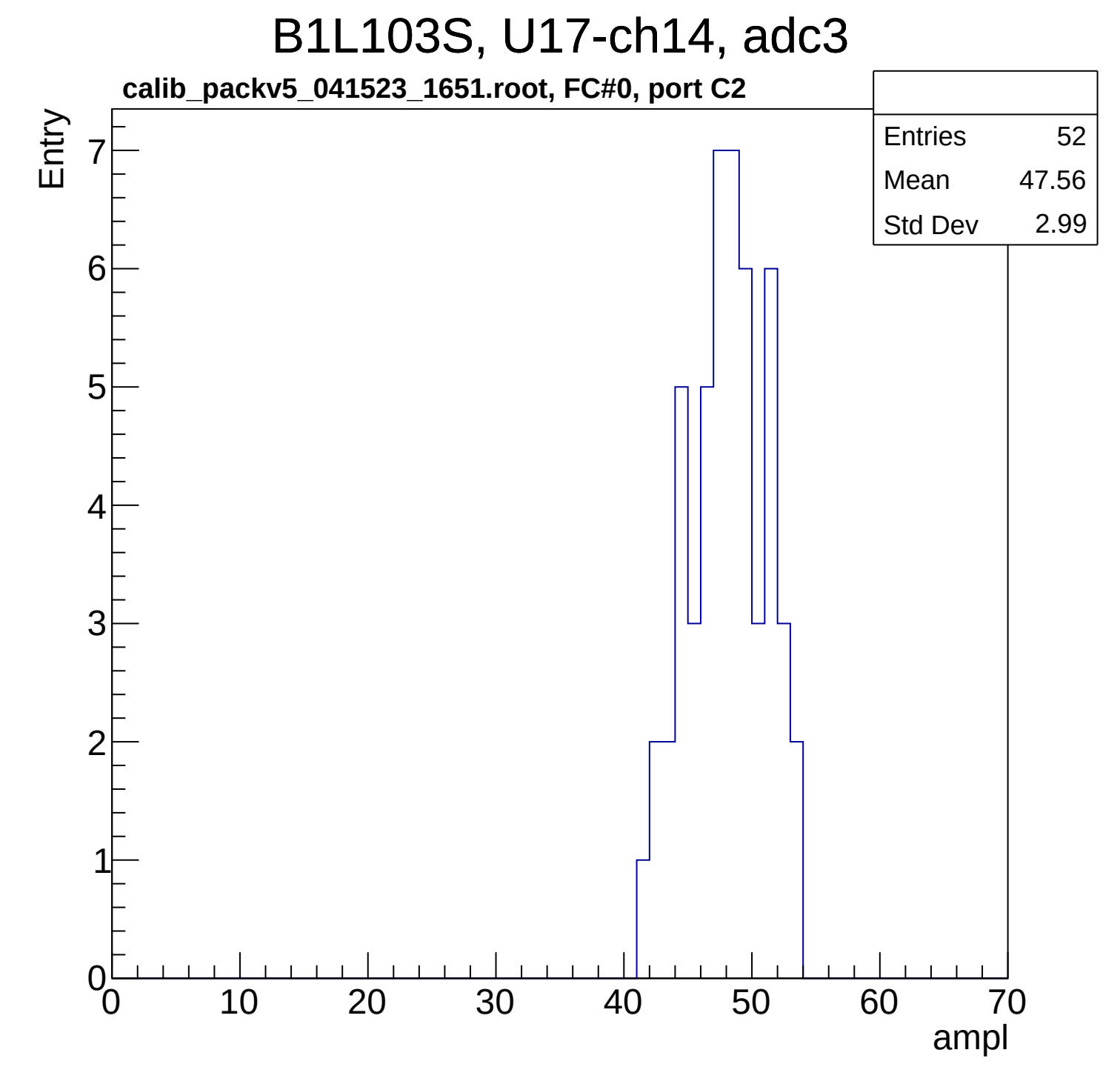

B1L103S, U17-ch13, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.2
Std Dev 0.9798
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

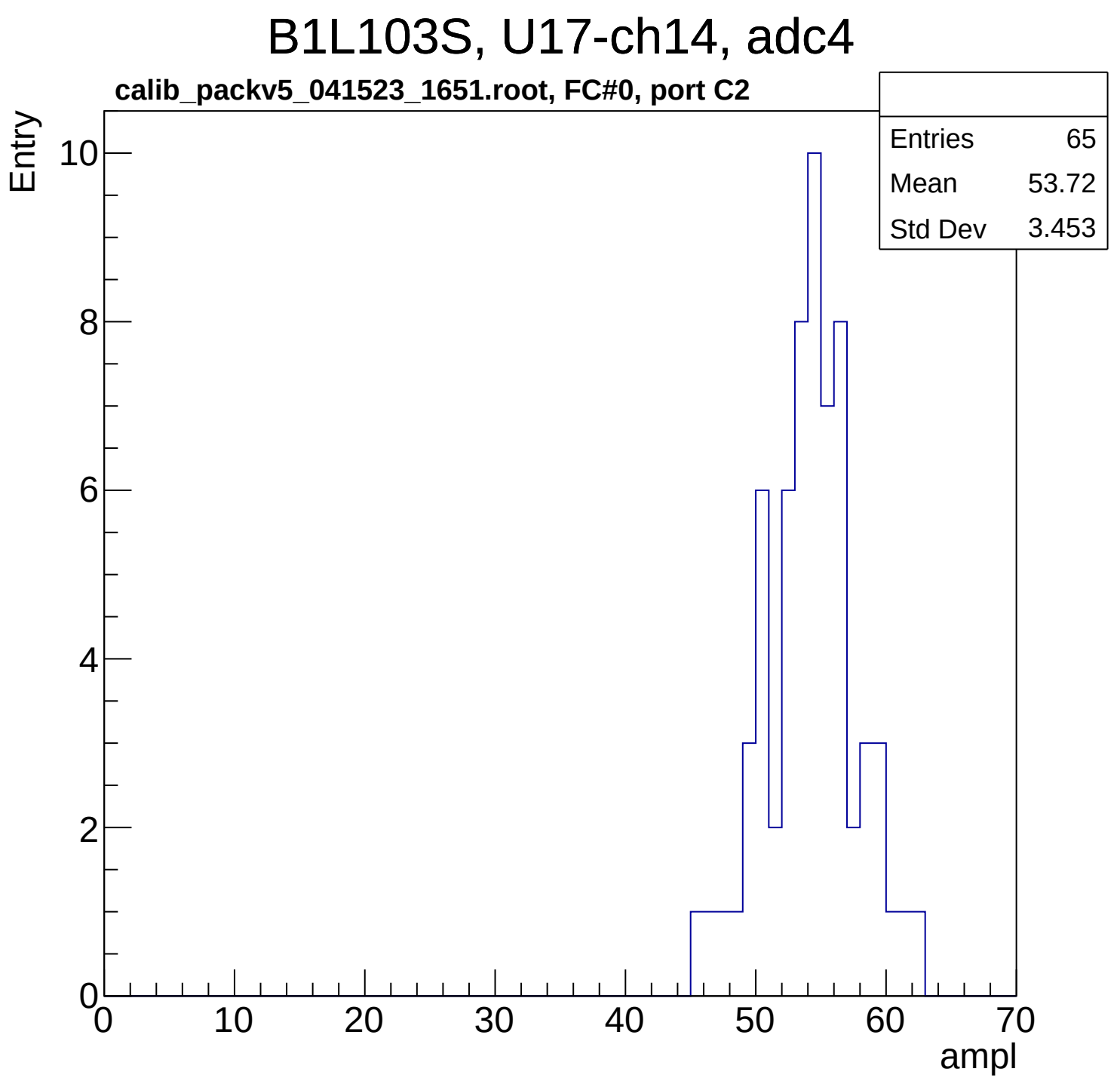

B1L103S, U17-ch13, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

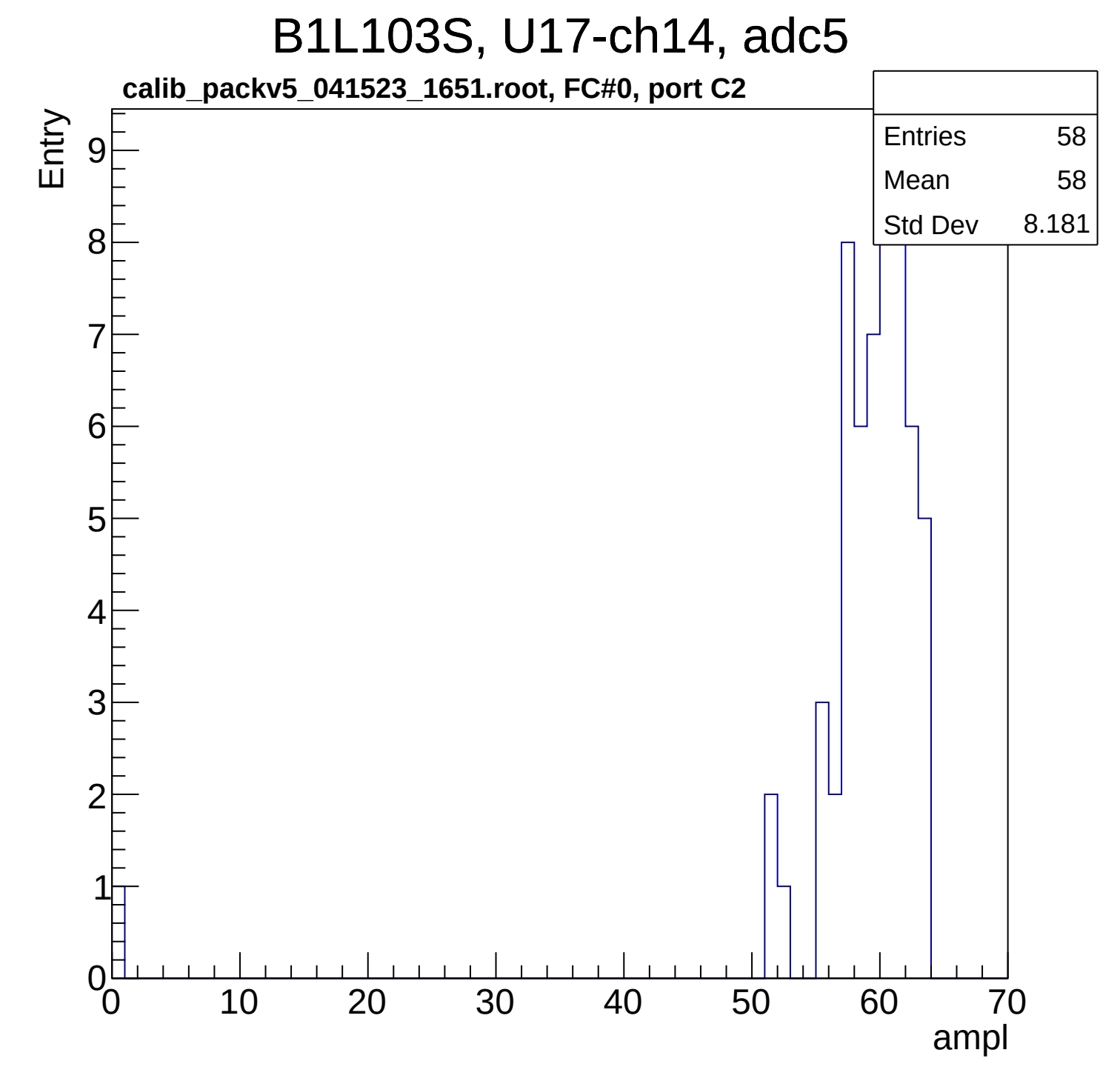

B1L103S, U17-ch14, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 25.49
Std Dev 10.08
Gaus mean : 29.7419
Gaus Width: 3.9386
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

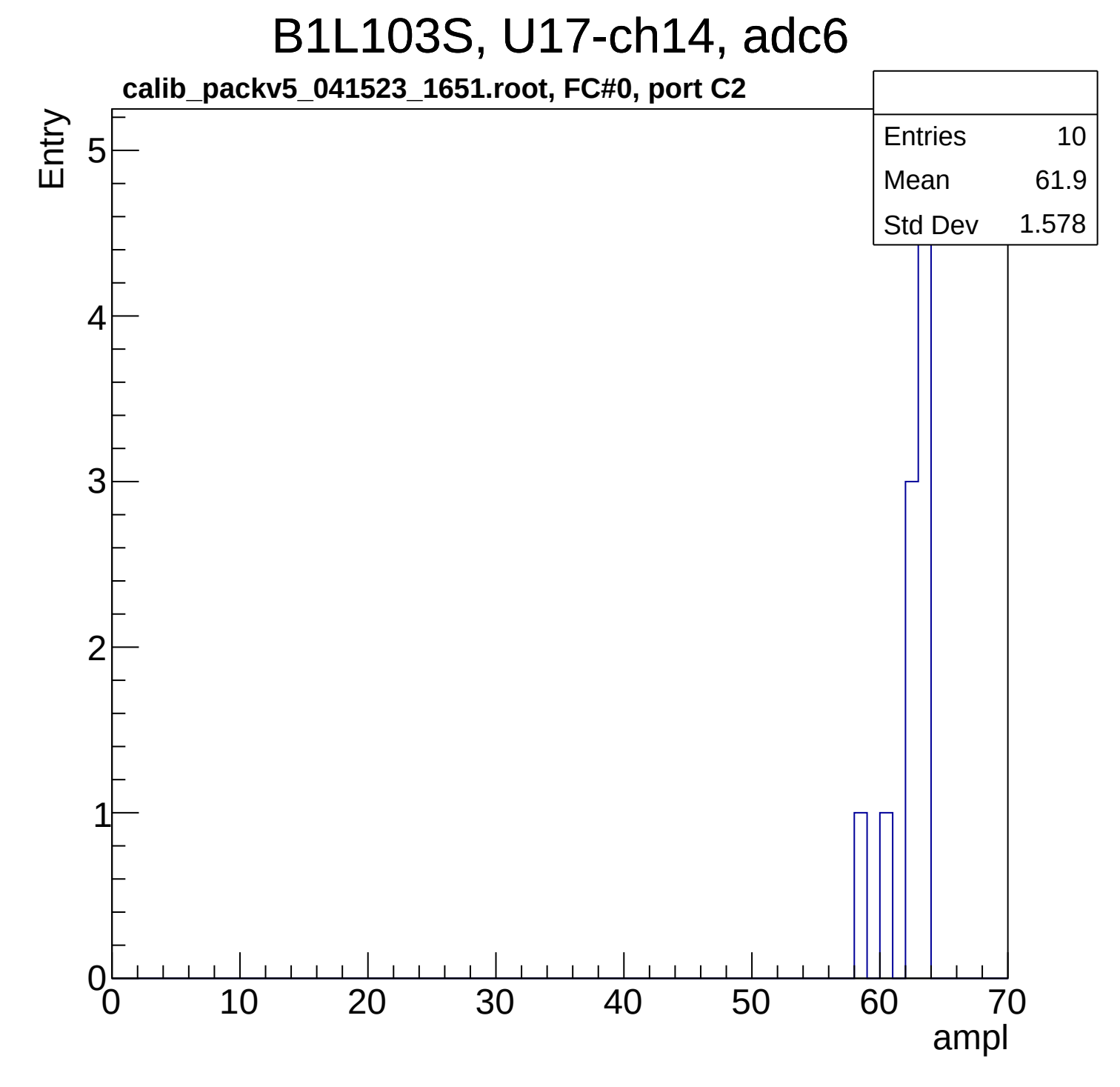

B1L103S, U17-ch14, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 31.48
Std Dev 10.83
Gaus mean : 35.0788
Gaus Width: 4.1270
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

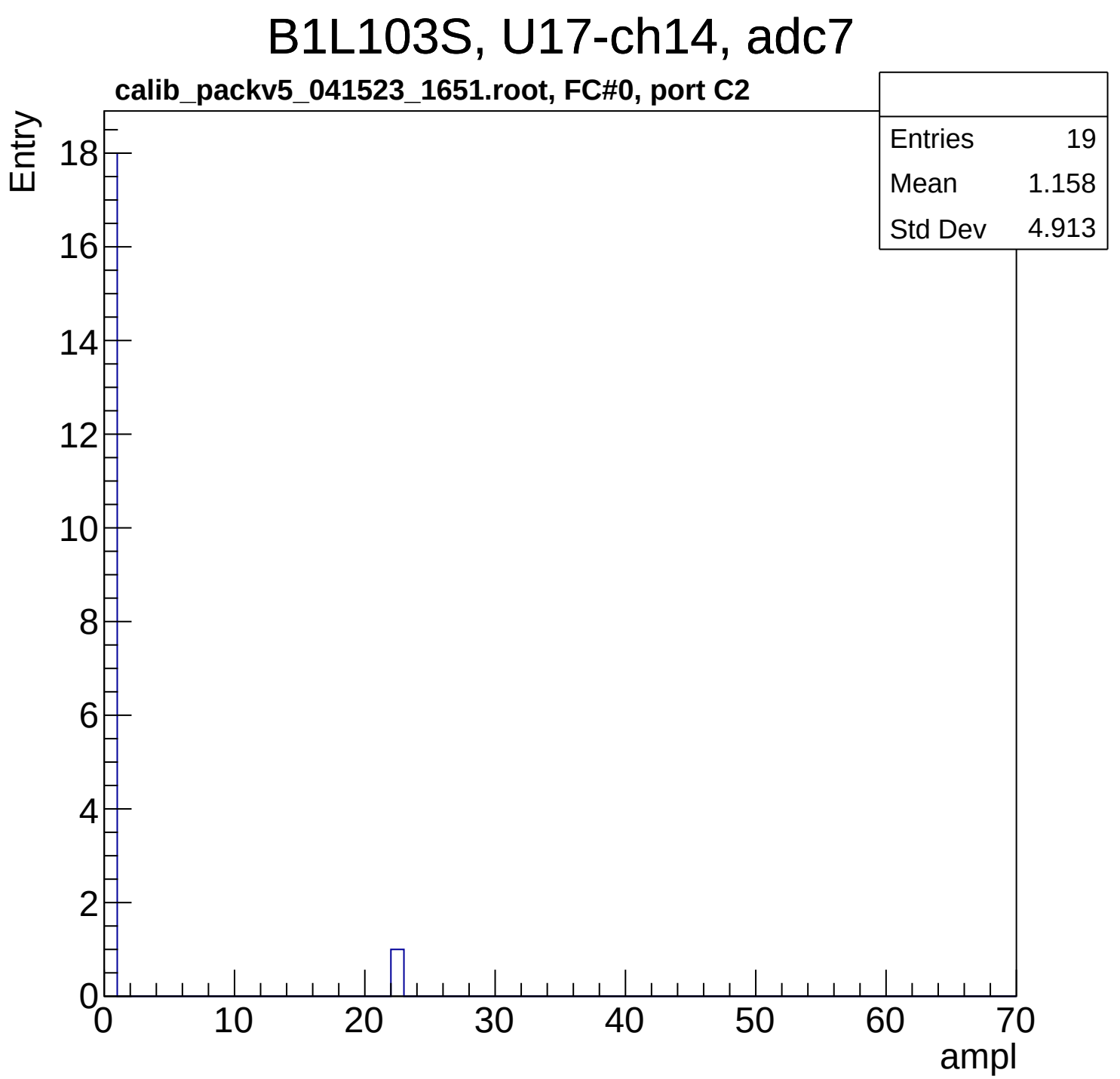

B1L103S, U17-ch14, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 38.37
Std Dev 12.43
Gaus mean : 42.3935
Gaus Width: 3.7304
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

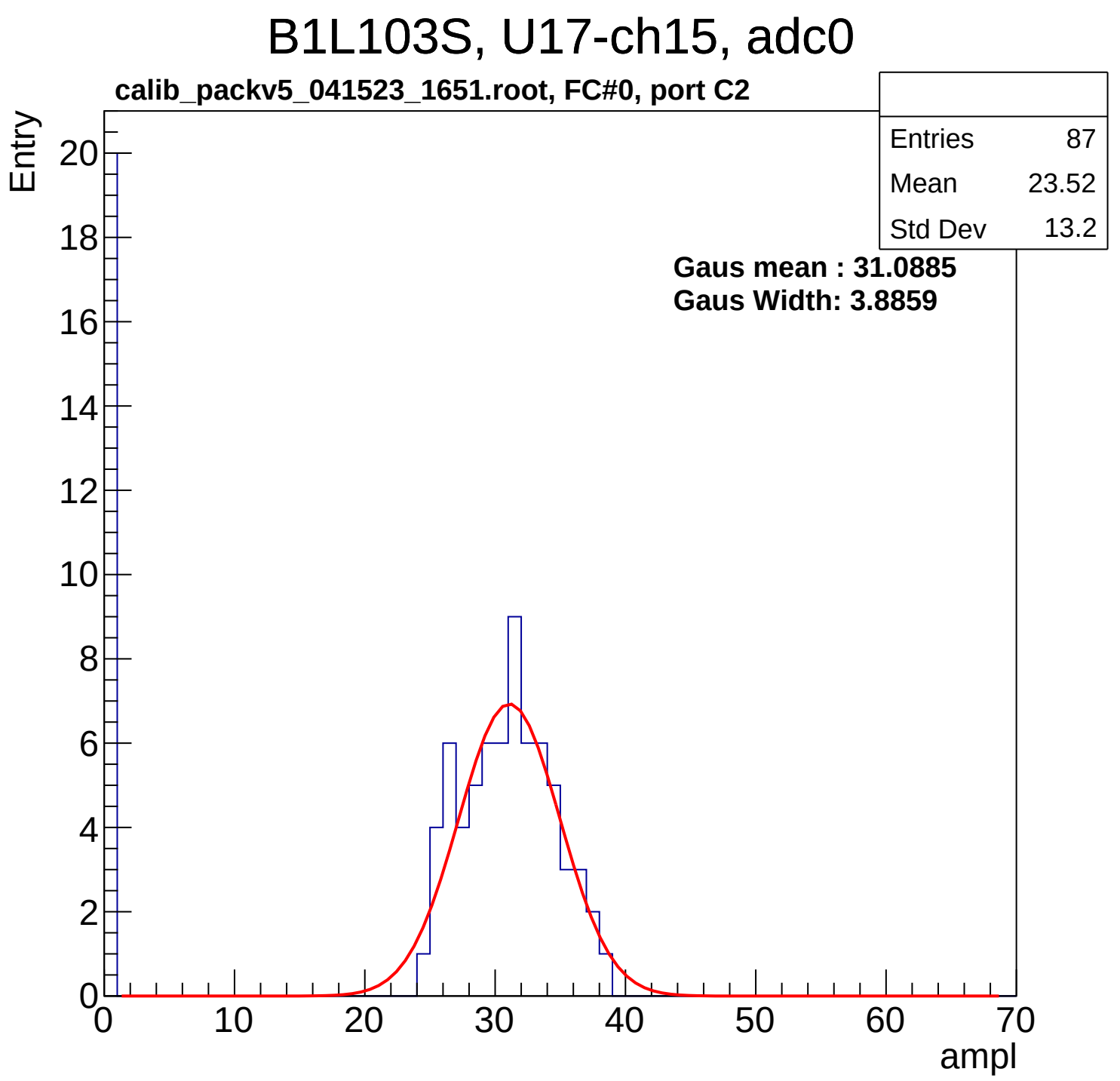

B1L103S, U17-ch14, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 47.56
Std Dev 2.99
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

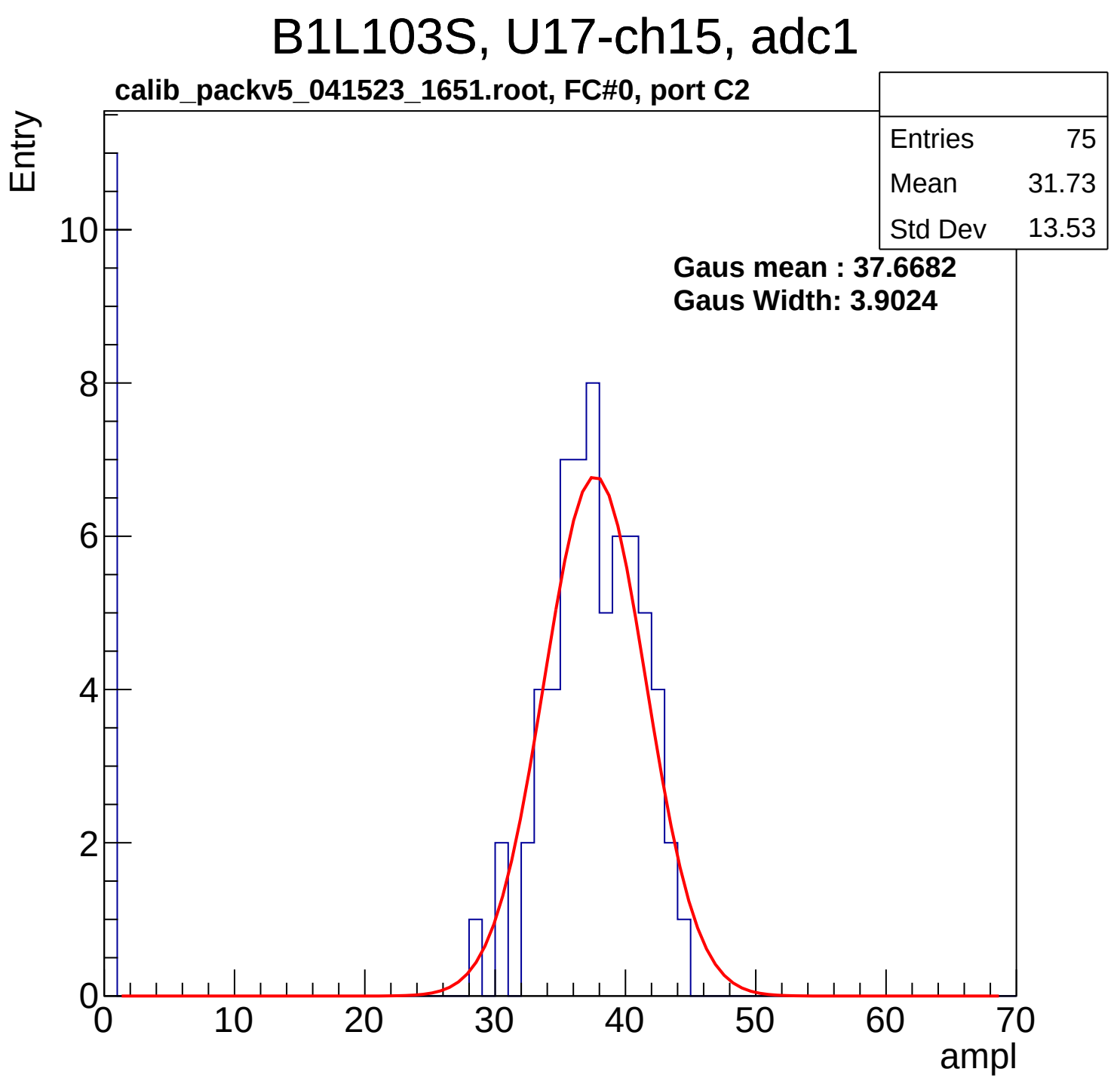

B1L103S, U17-ch14, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 53.72
Std Dev 3.453
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

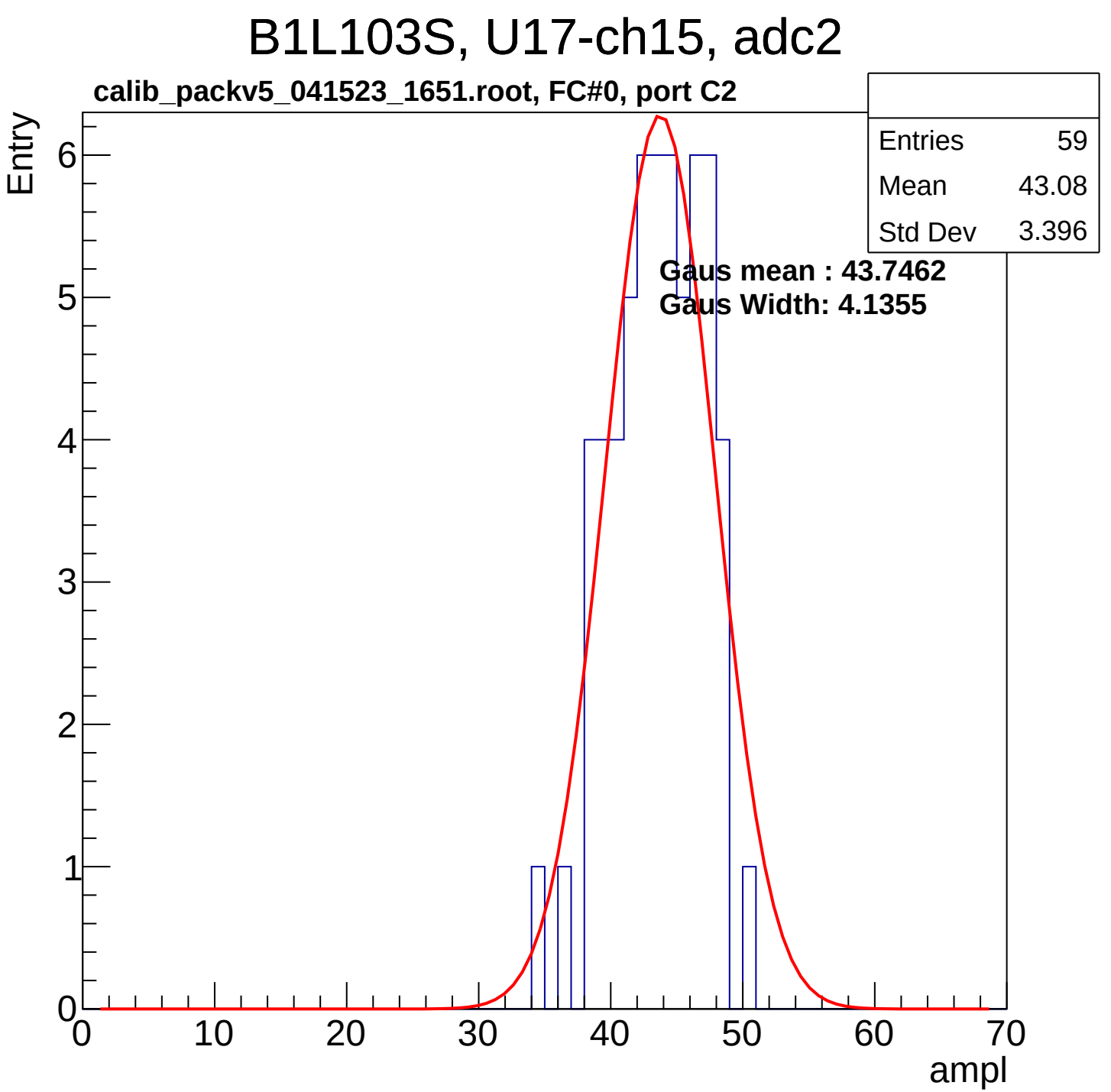

B1L103S, U17-ch14, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58
Std Dev 8.181
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

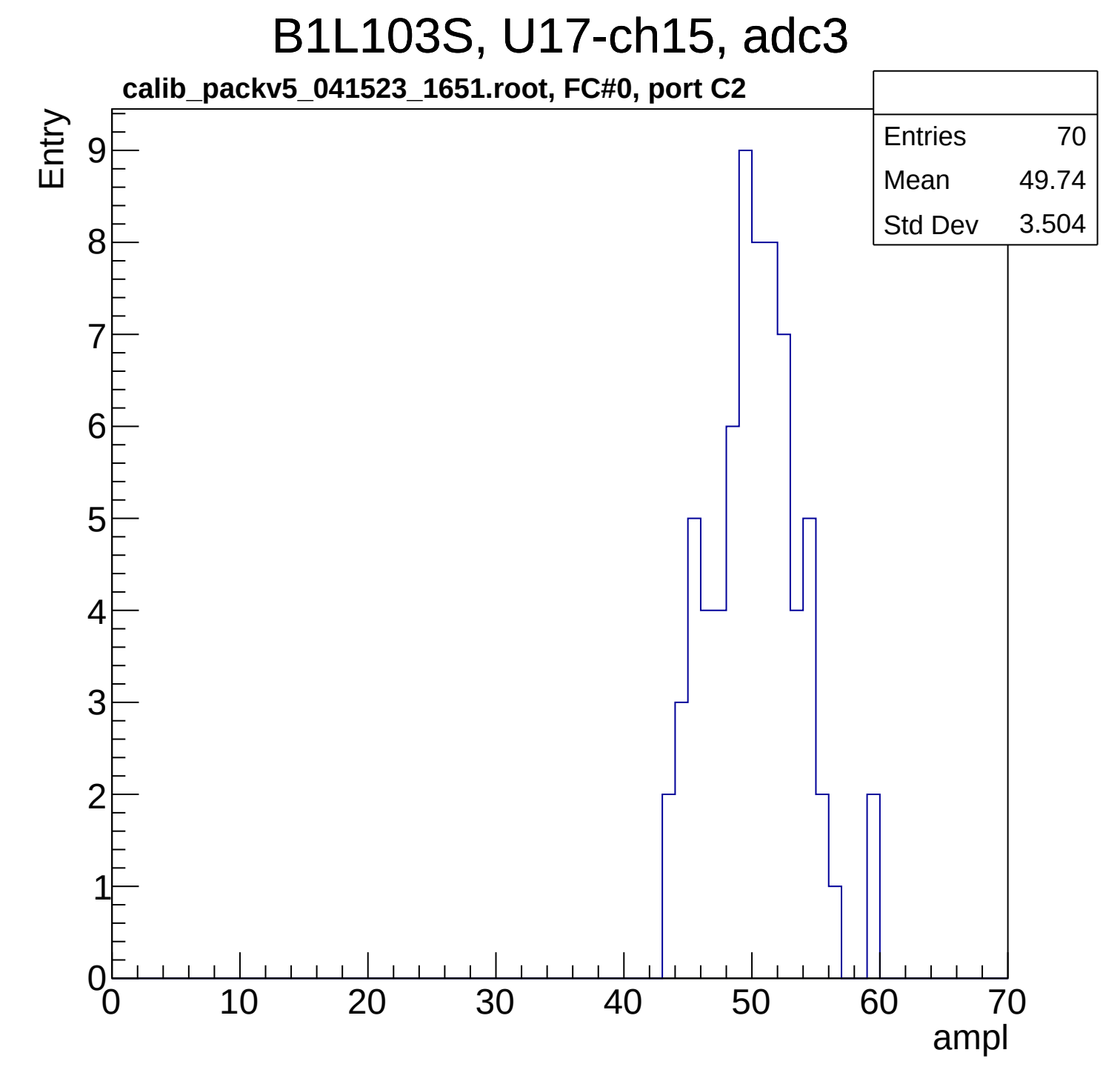

B1L103S, U17-ch14, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.9
Std Dev 1.578
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

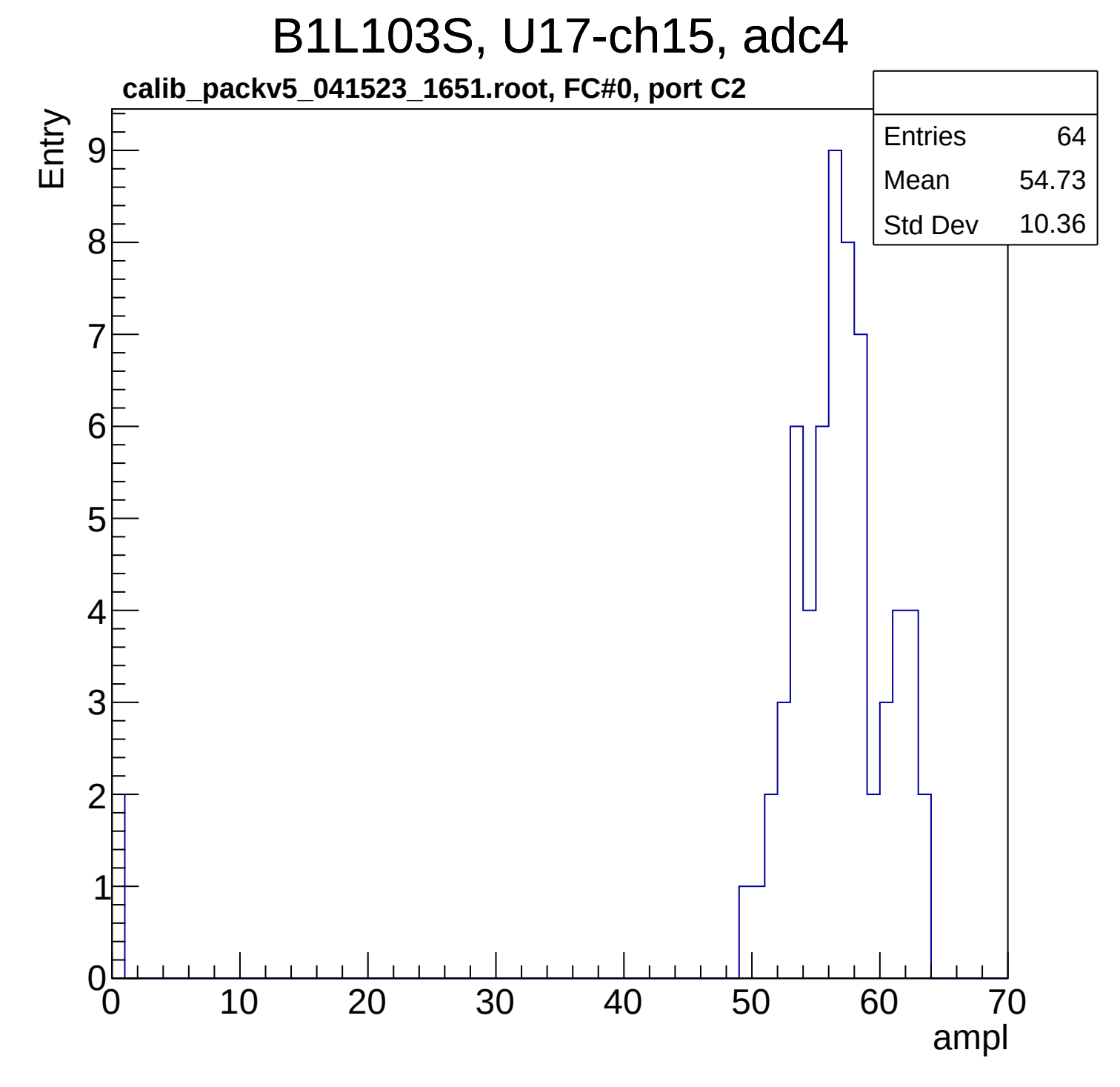

B1L103S, U17-ch14, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

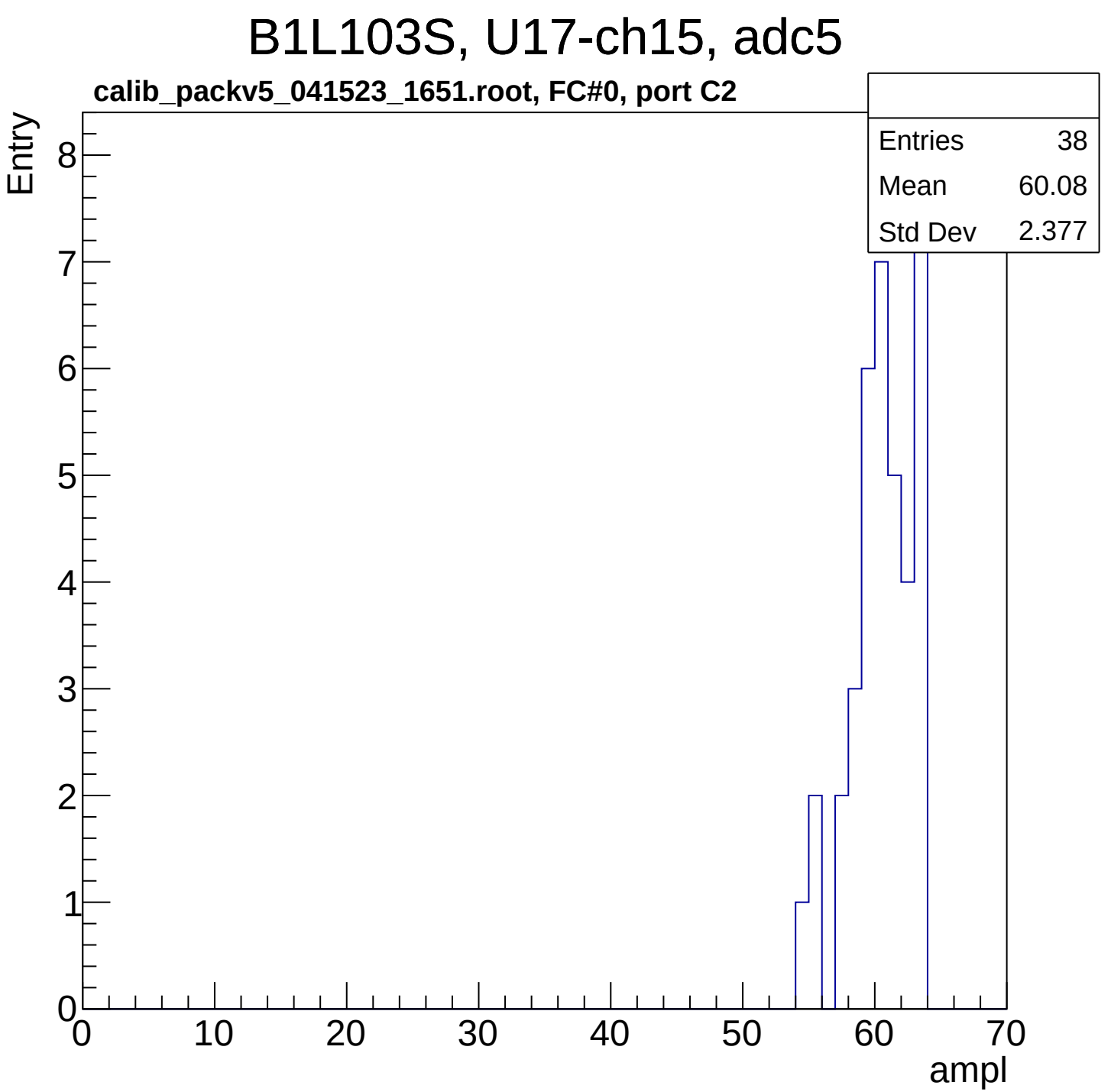

B1L103S, U17-ch15, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 23.52
Std Dev 13.2
Gaus mean : 31.0885
Gaus Width: 3.8859
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

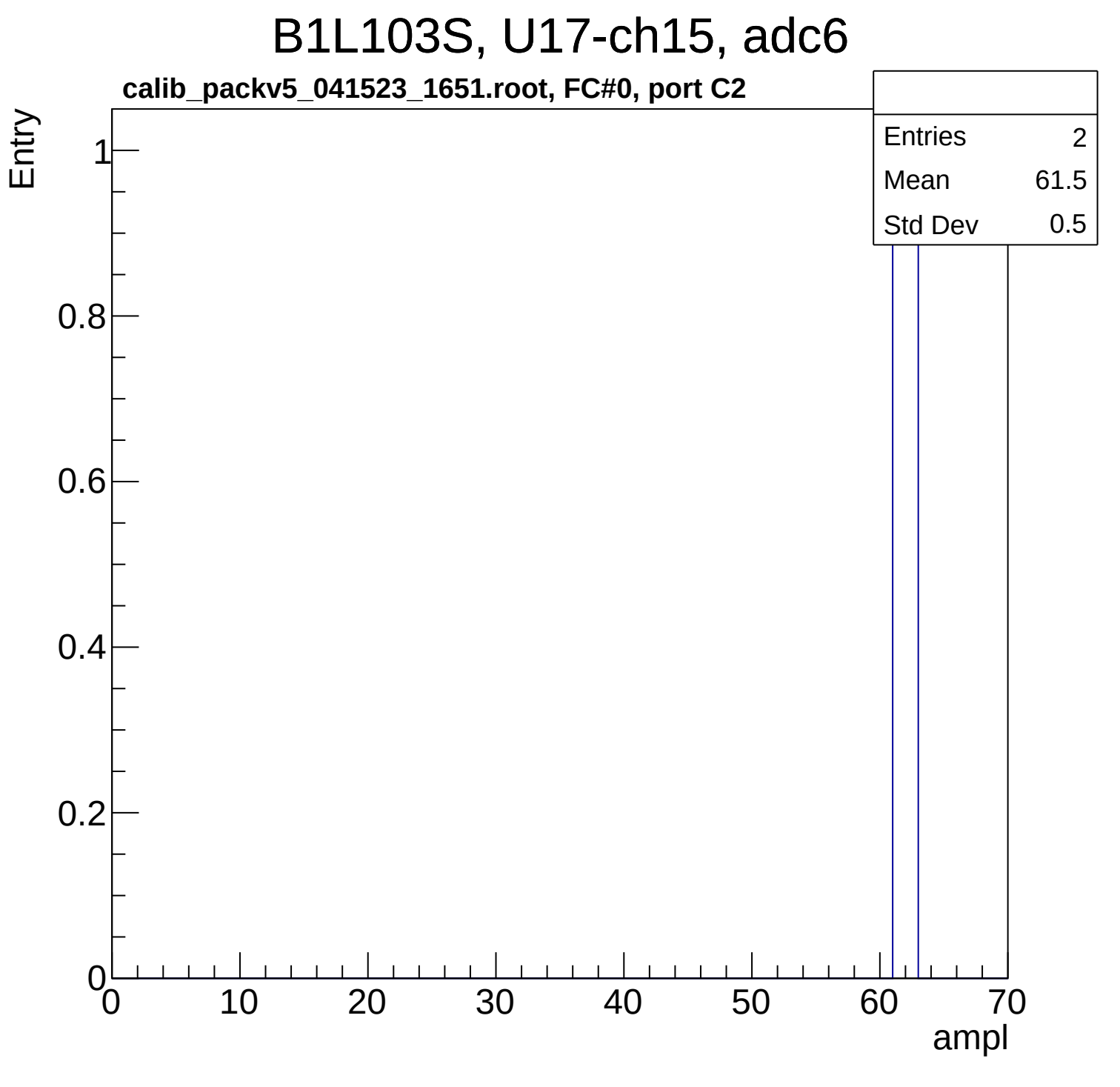

B1L103S, U17-ch15, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 31.73
Std Dev 13.53
Gaus mean : 37.6682
Gaus Width: 3.9024
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

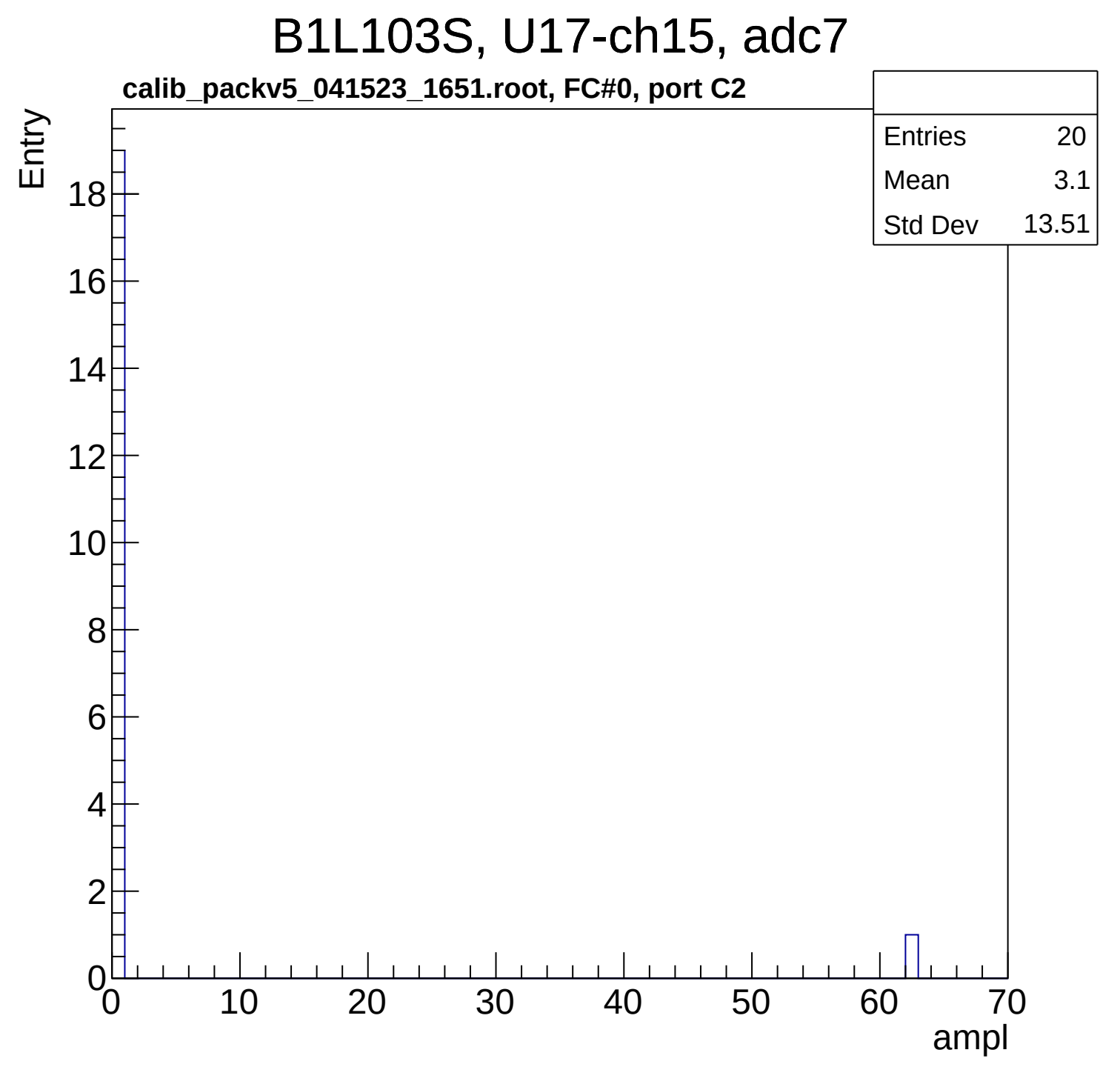

B1L103S, U17-ch15, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 43.08
Std Dev 3.396
Gaus mean : 43.7462
Gaus Width: 4.1355
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

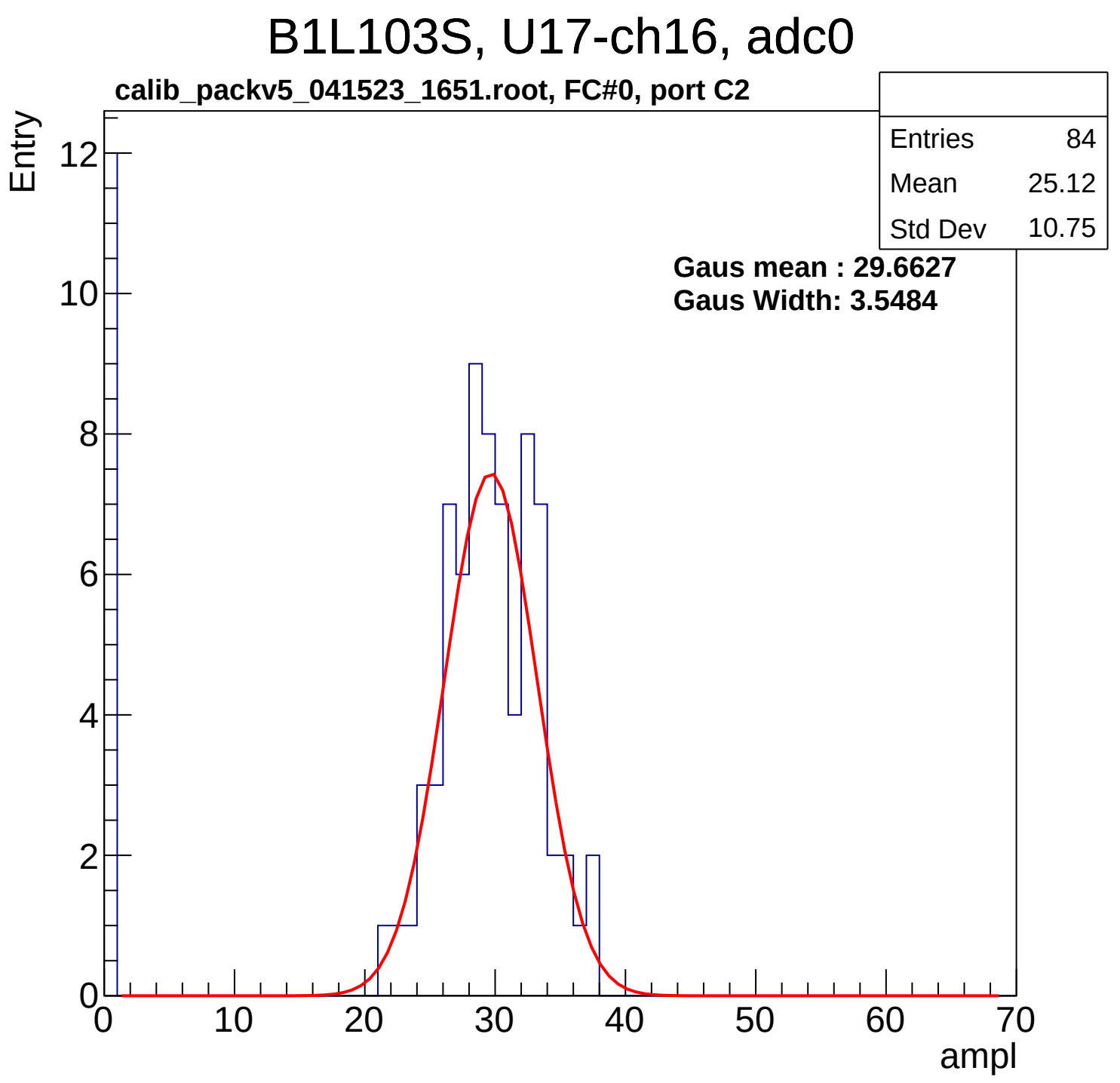

B1L103S, U17-ch15, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 49.74
Std Dev 3.504
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

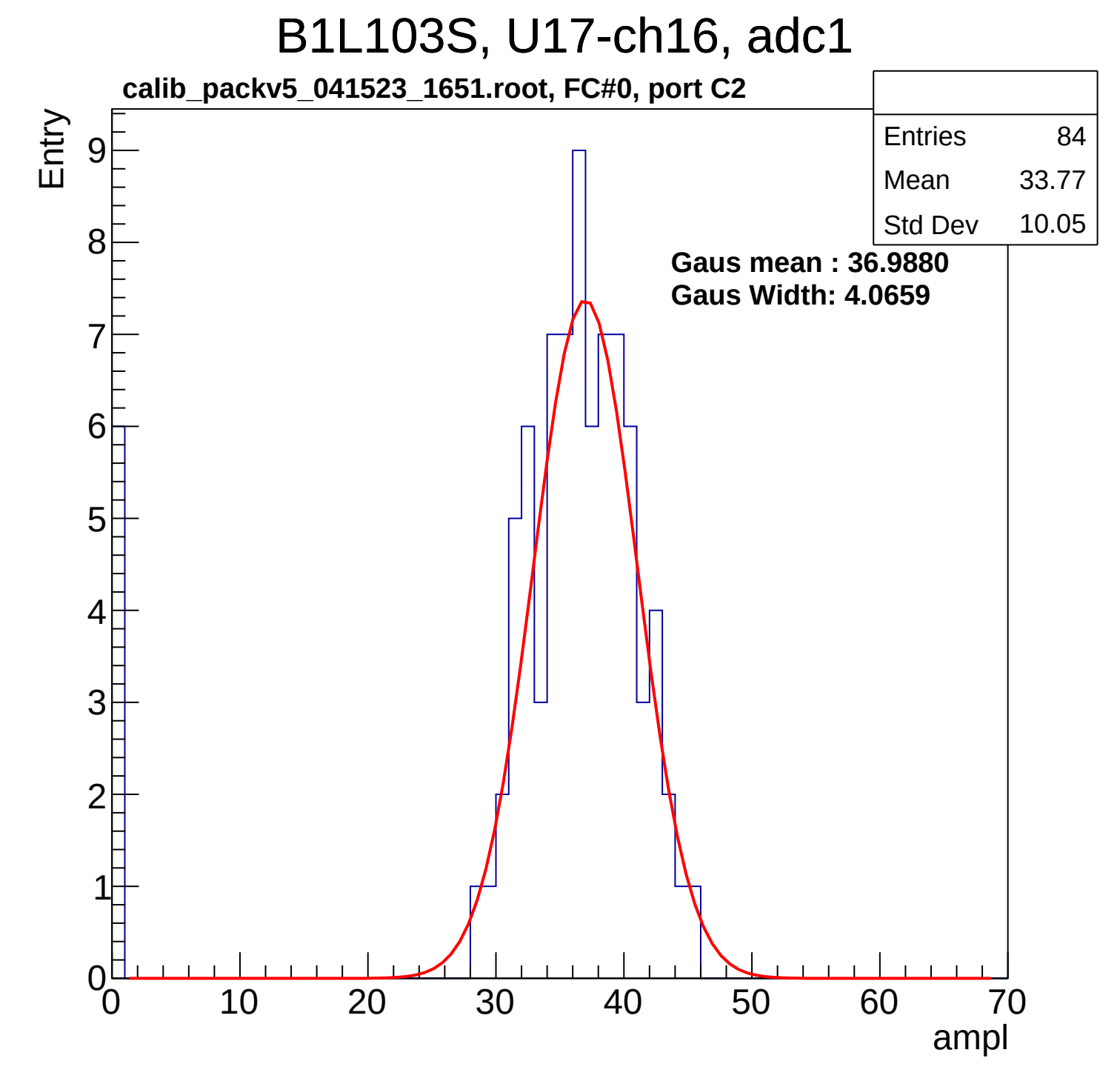

B1L103S, U17-ch15, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 54.73
Std Dev 10.36
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

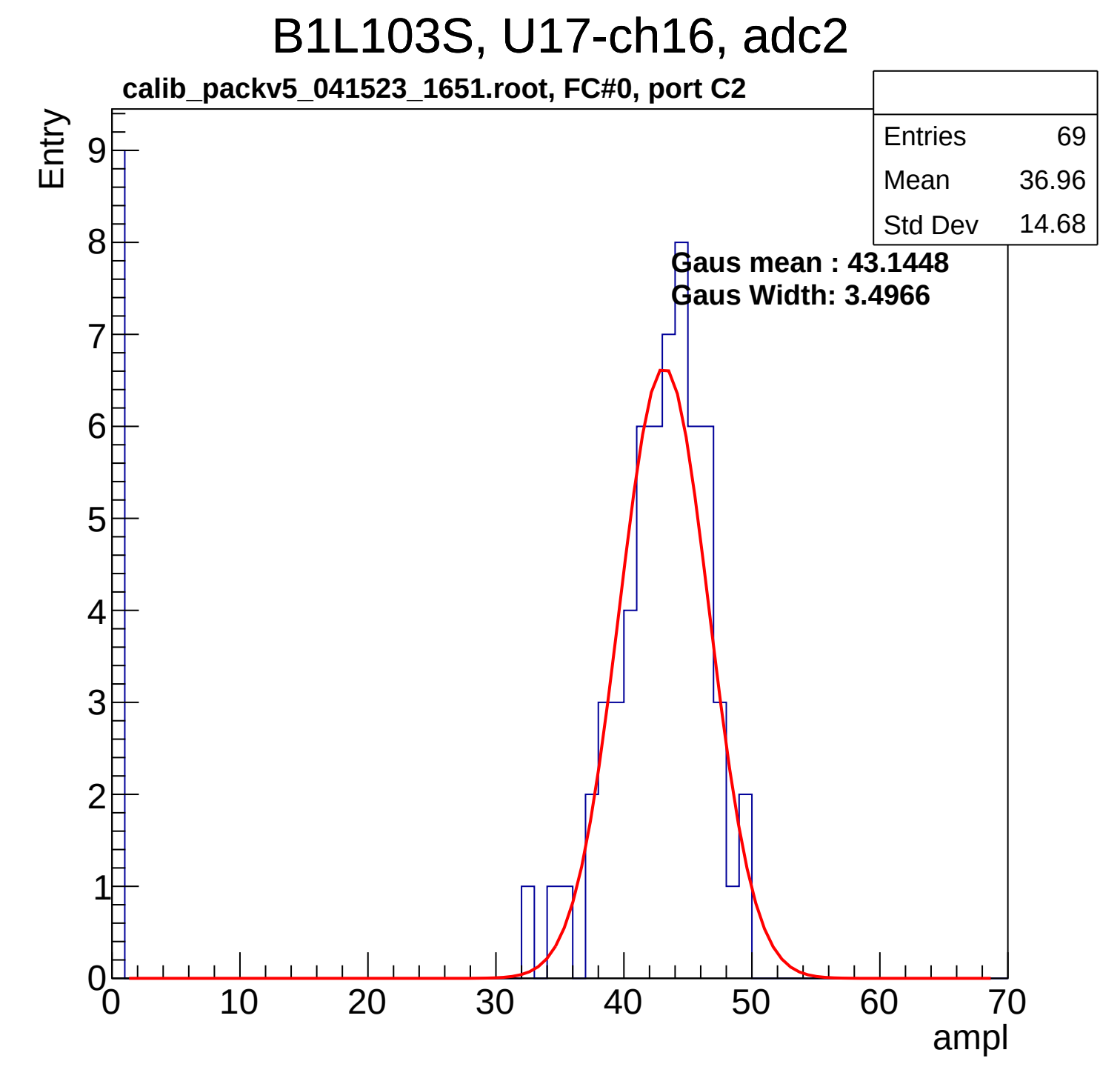

B1L103S, U17-ch15, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 60.08
Std Dev 2.377
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

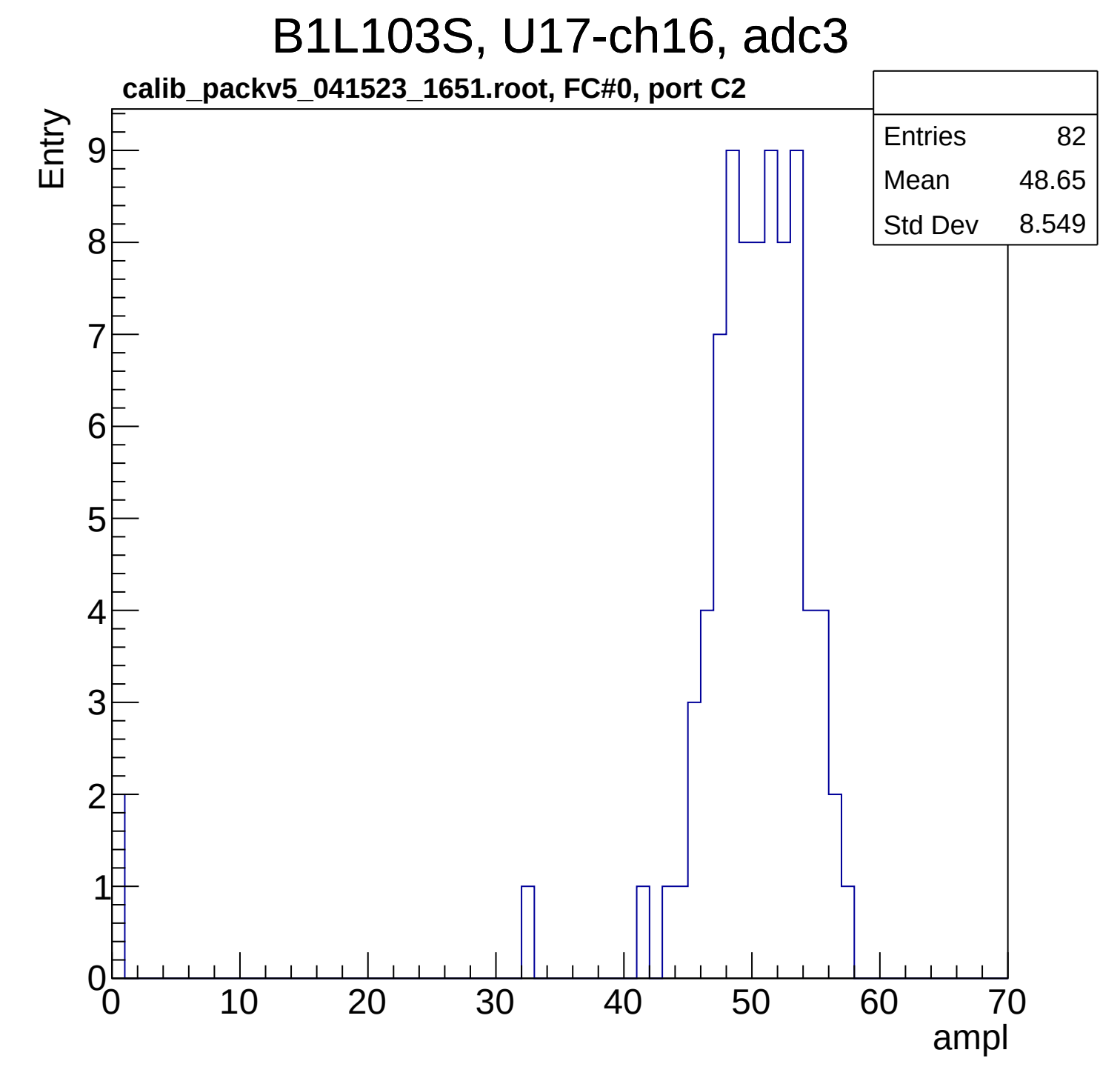

B1L103S, U17-ch15, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 61.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

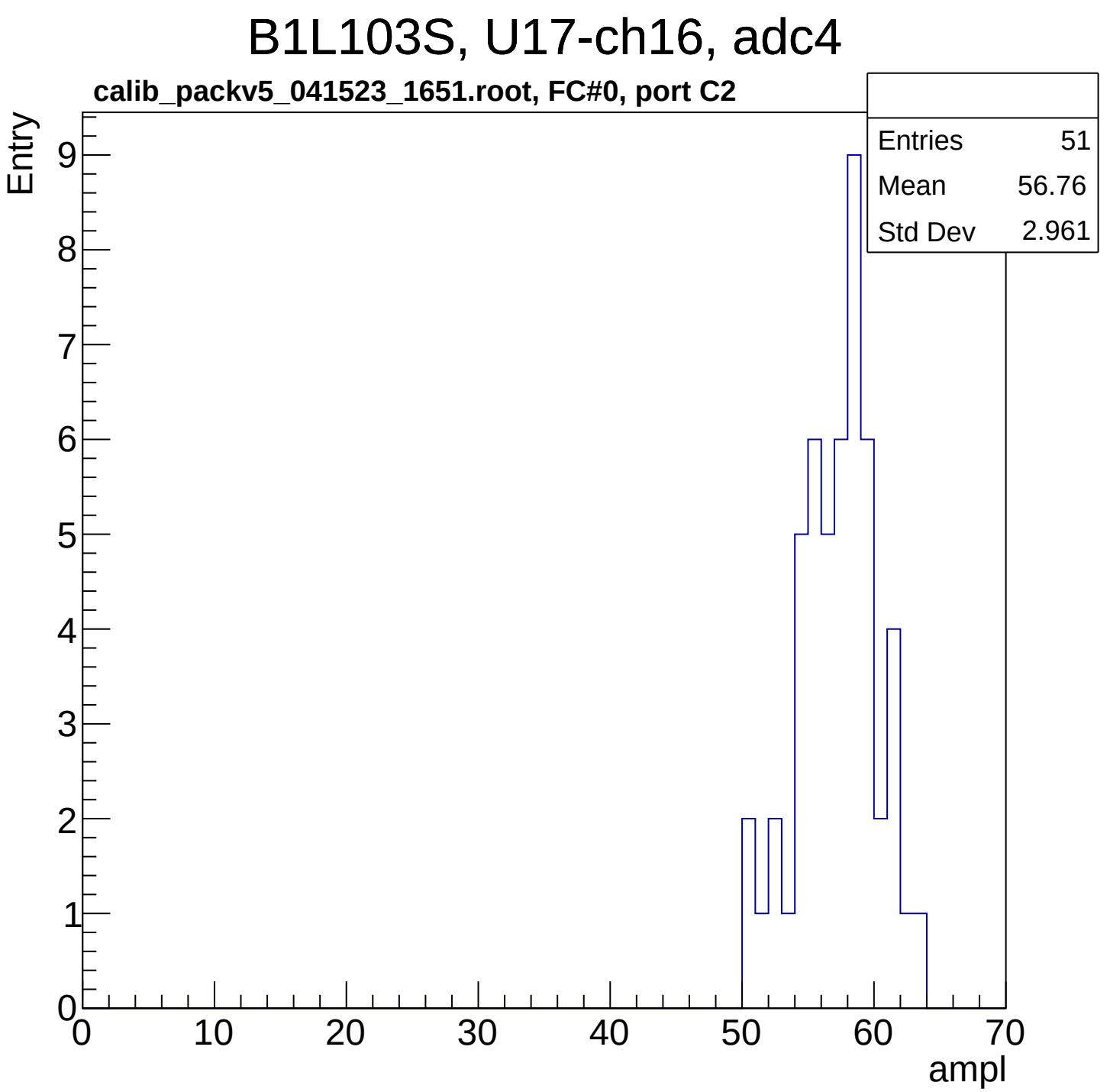

B1L103S, U17-ch15, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

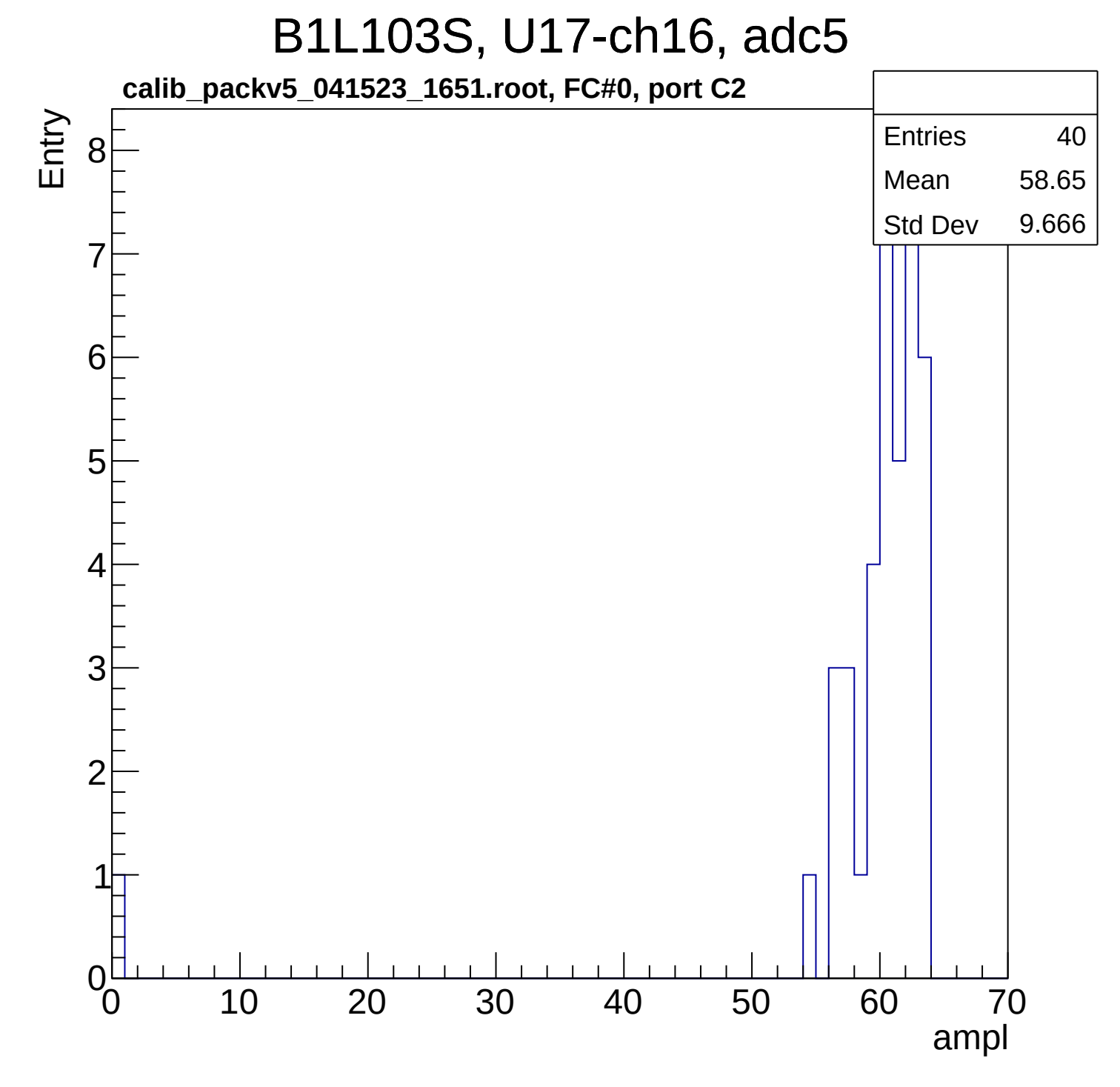

B1L103S, U17-ch16, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 25.12
Std Dev 10.75
Gaus mean : 29.6627
Gaus Width: 3.5484
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

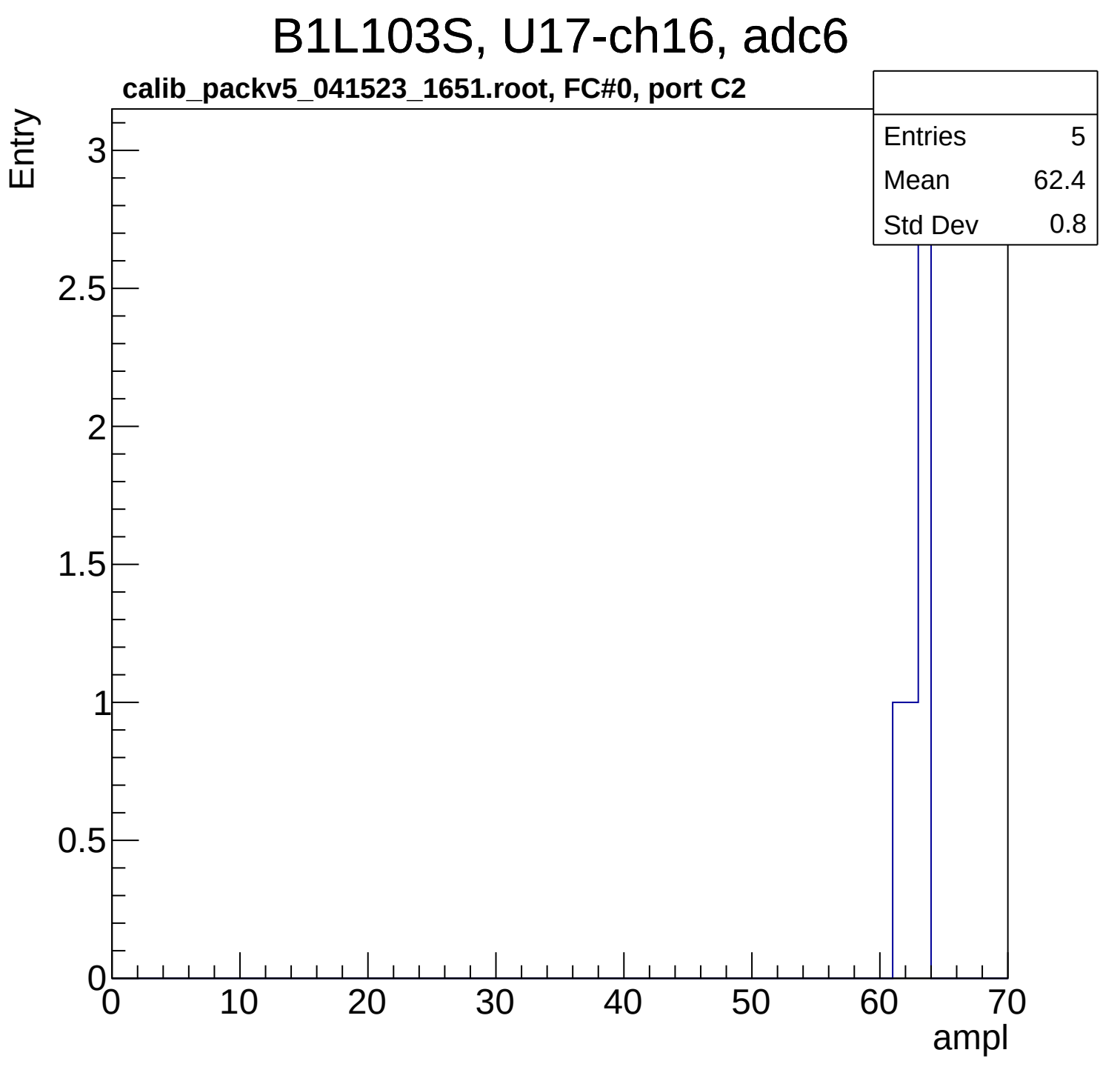

B1L103S, U17-ch16, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 33.77
Std Dev 10.05
Gaus mean : 36.9880
Gaus Width: 4.0659
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

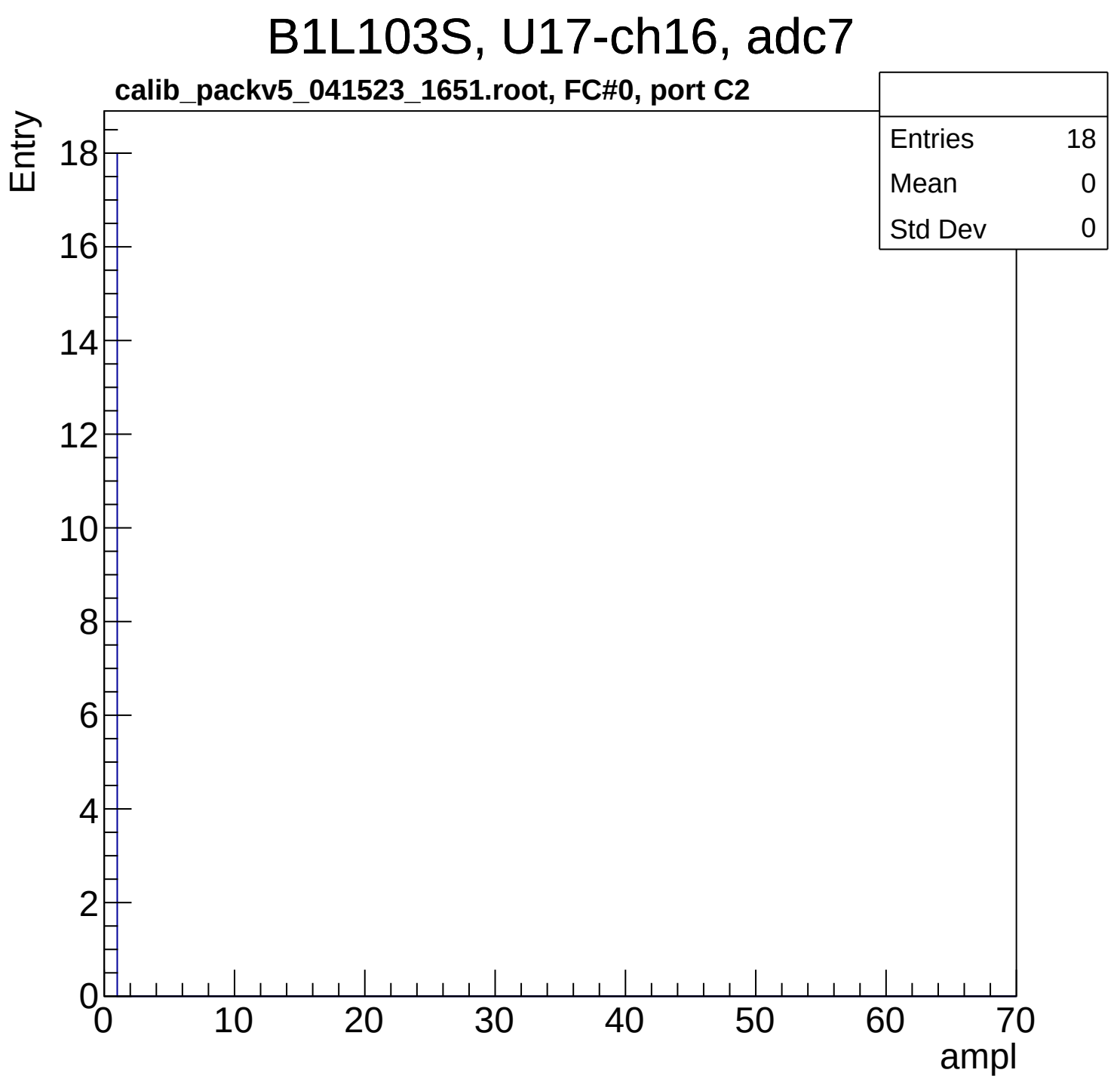

B1L103S, U17-ch16, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 36.96
Std Dev 14.68
Gaus mean : 43.1448
Gaus Width: 3.4966
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

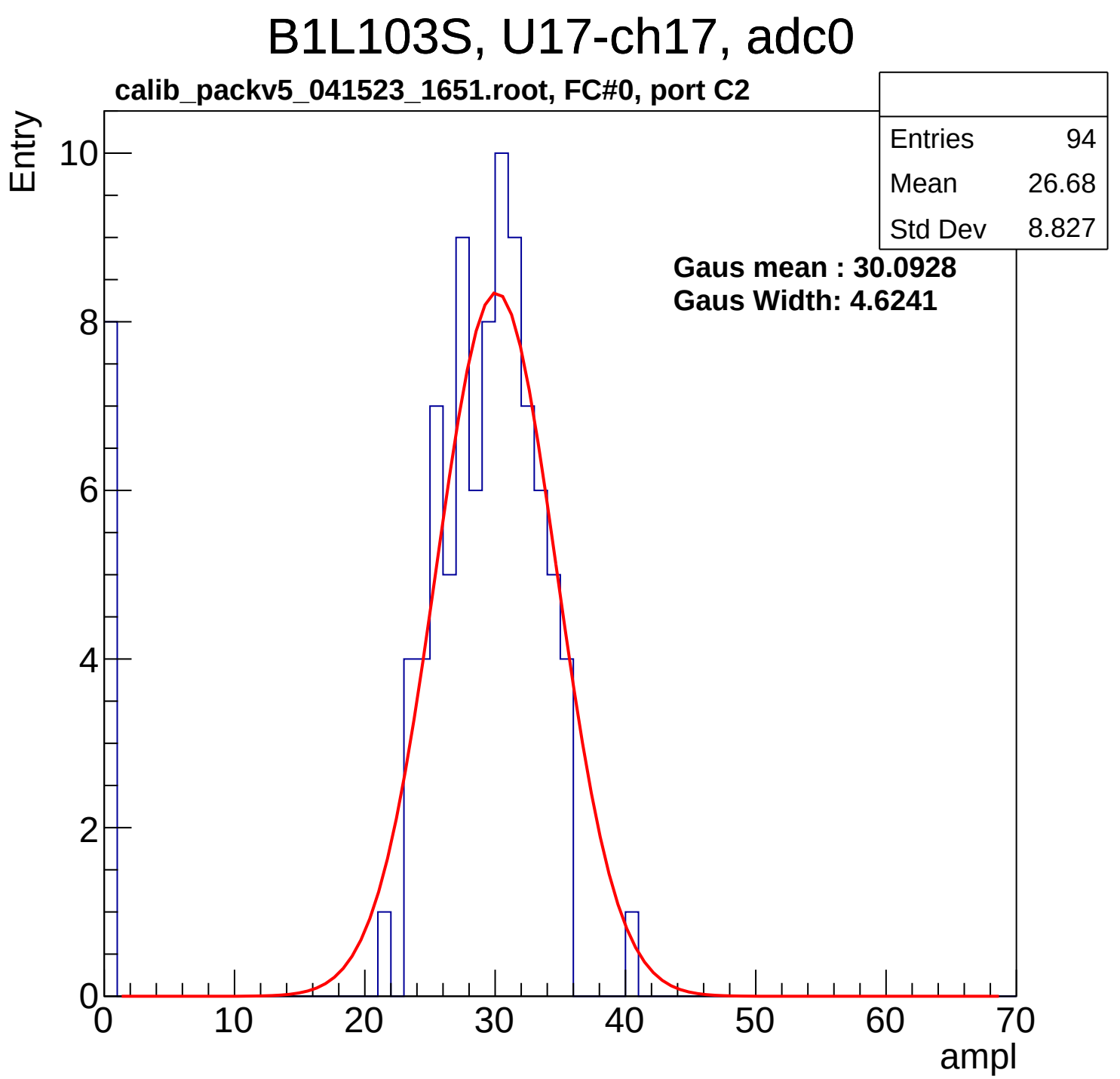

B1L103S, U17-ch16, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 48.65
Std Dev 8.549
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

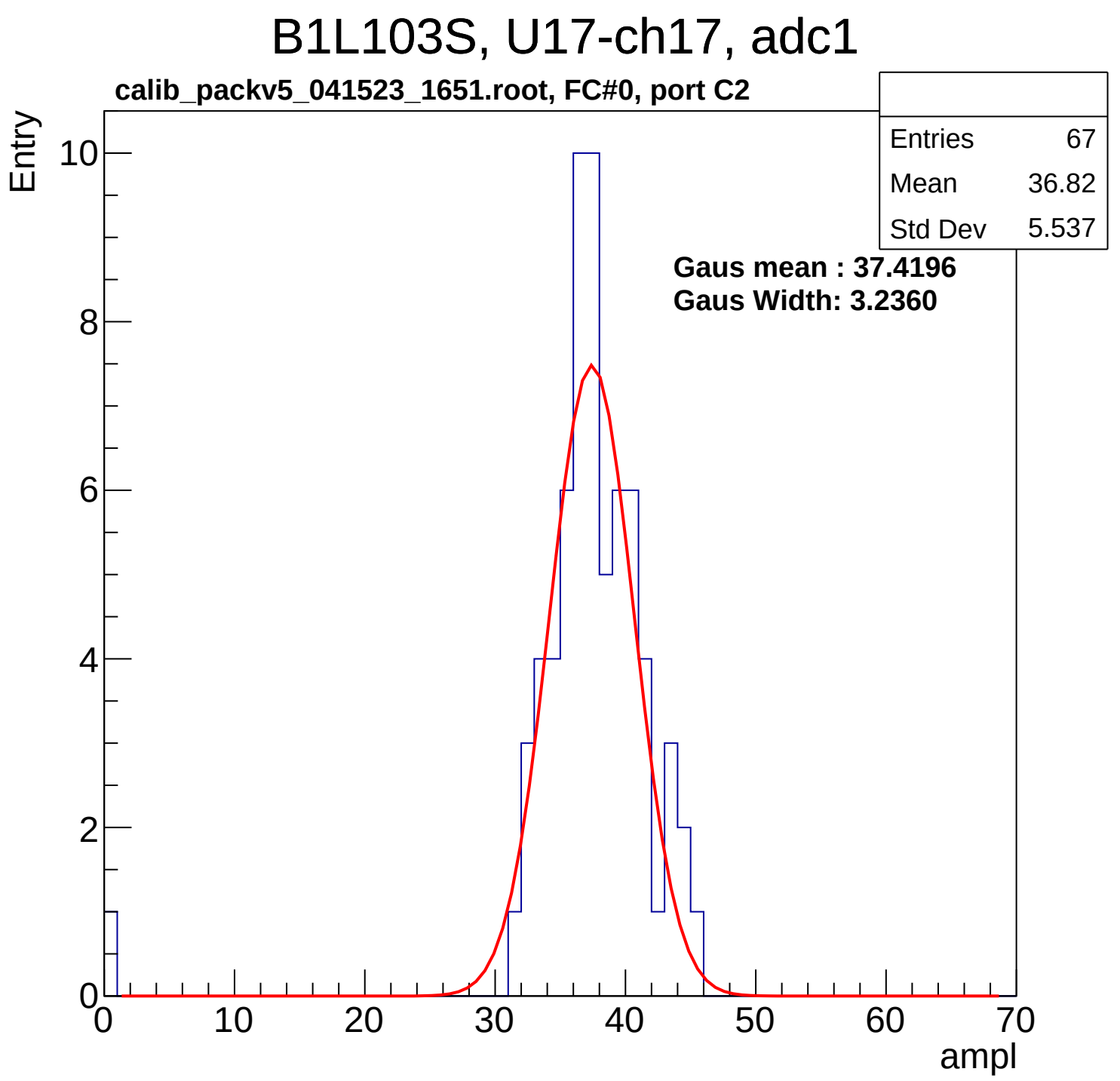

B1L103S, U17-ch16, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 56.76
Std Dev 2.961
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

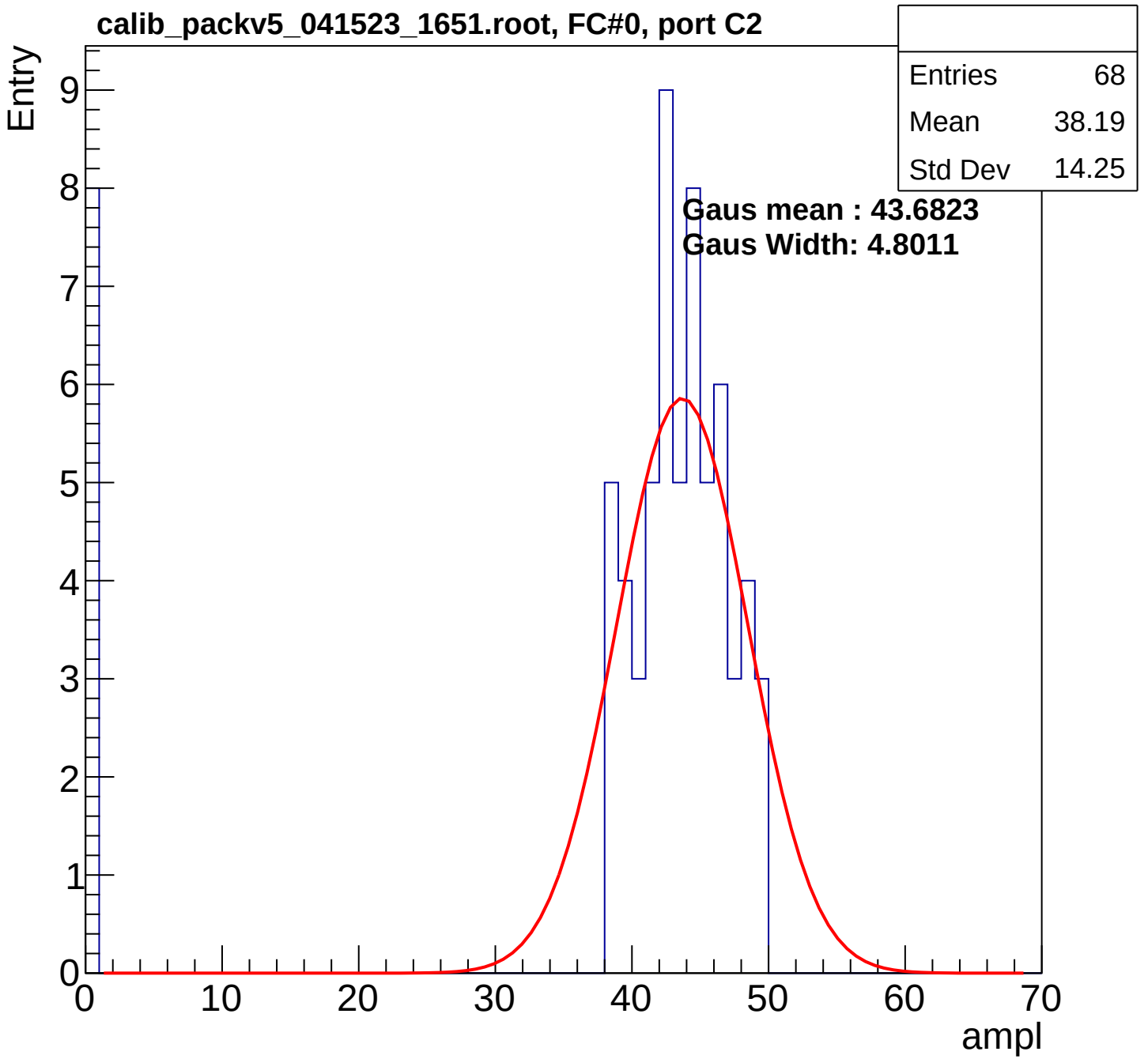

B1L103S, U17-ch16, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 58.65
Std Dev 9.666
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

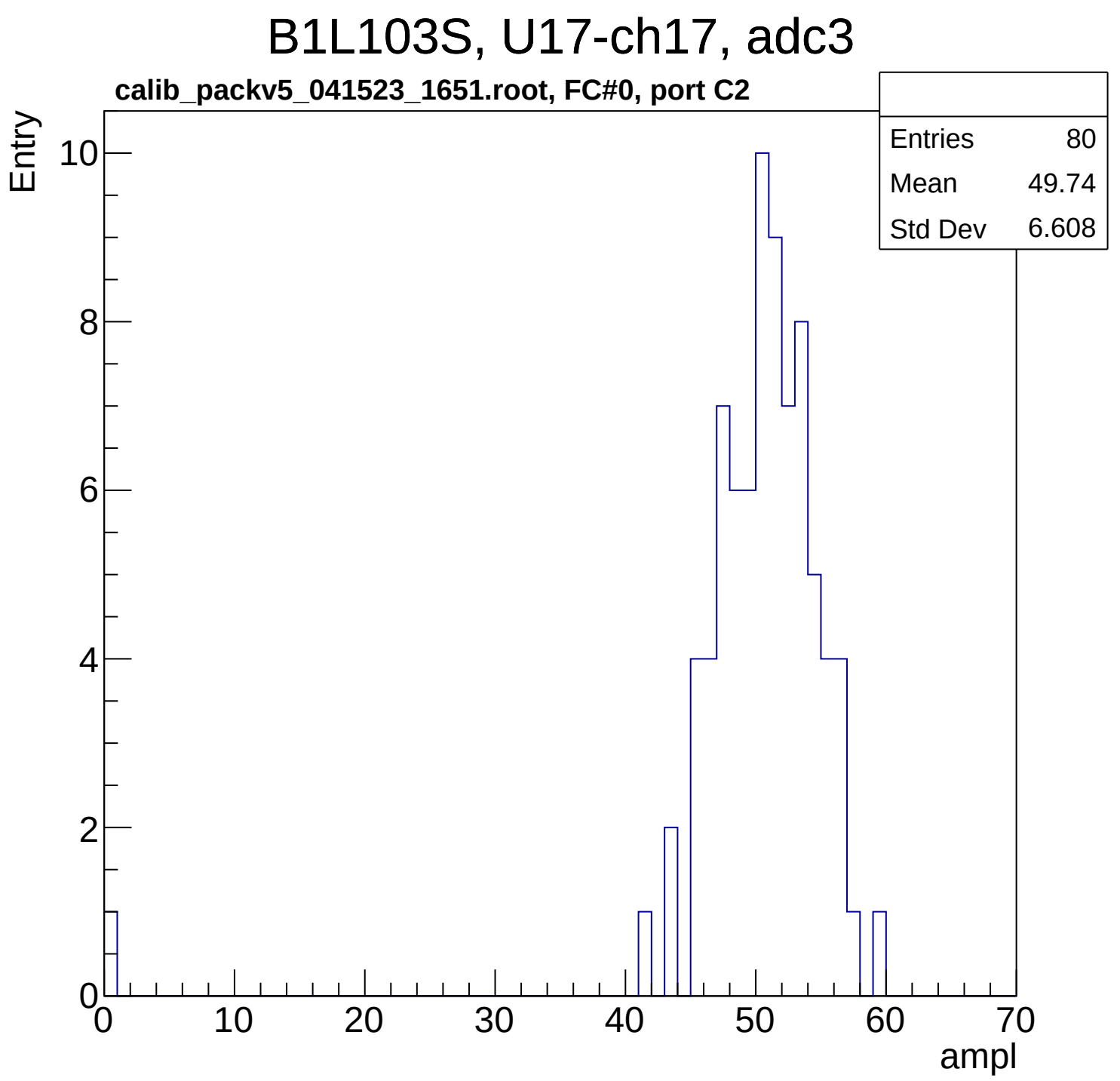

B1L103S, U17-ch16, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.4
Std Dev 0.8
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

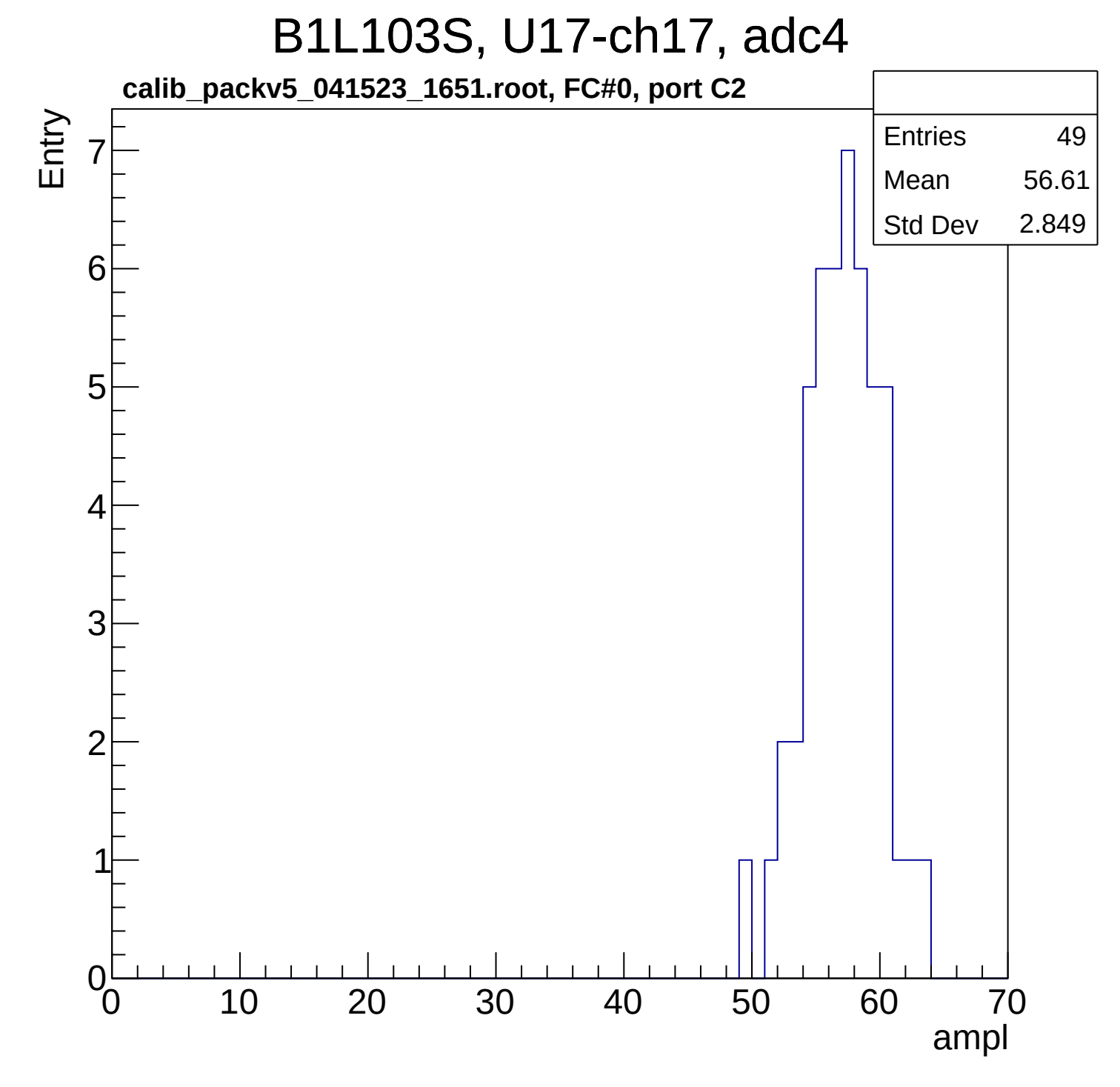

B1L103S, U17-ch16, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

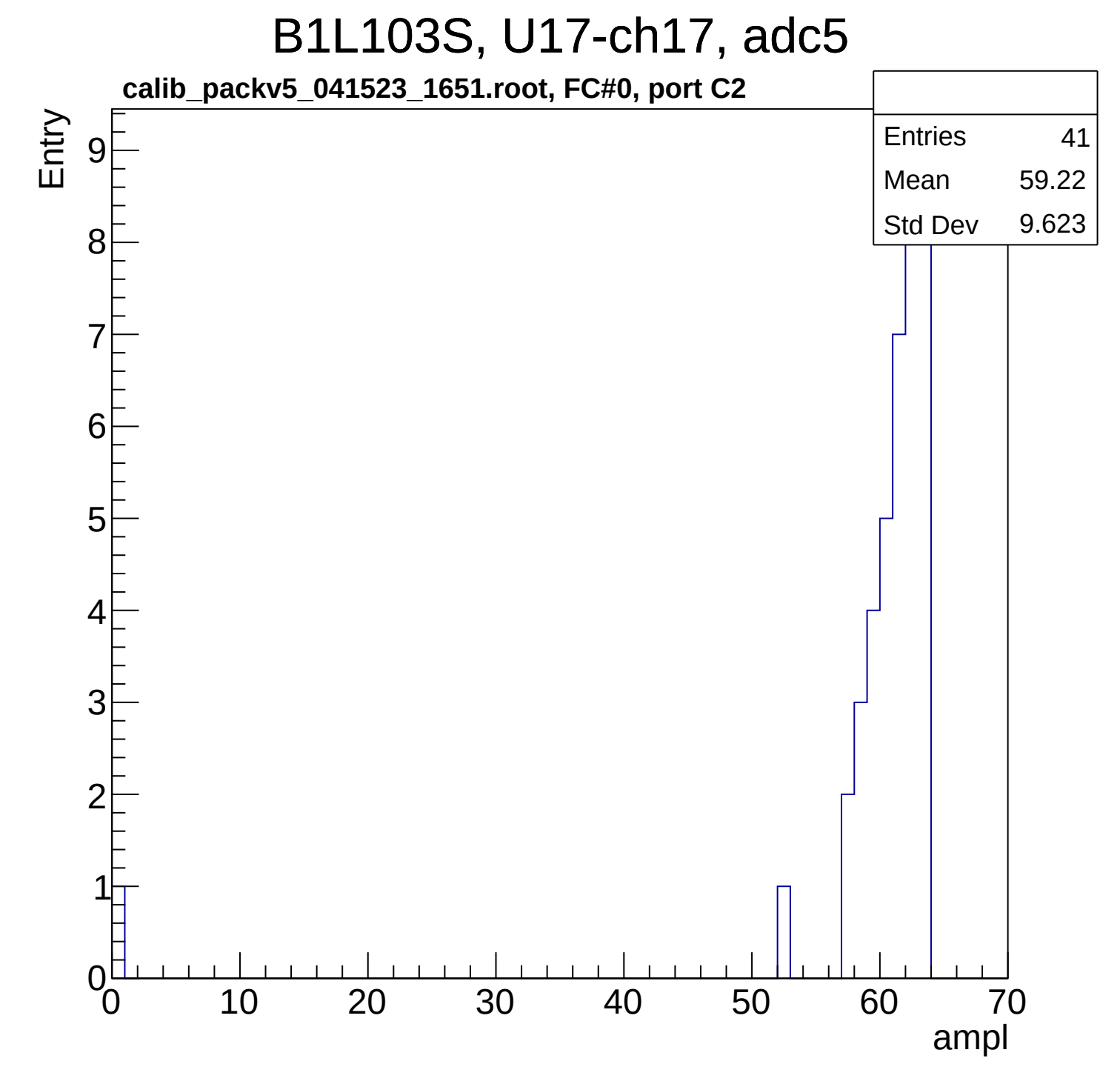

B1L103S, U17-ch17, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 26.68
Std Dev 8.827
Gaus mean : 30.0928
Gaus Width: 4.6241
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

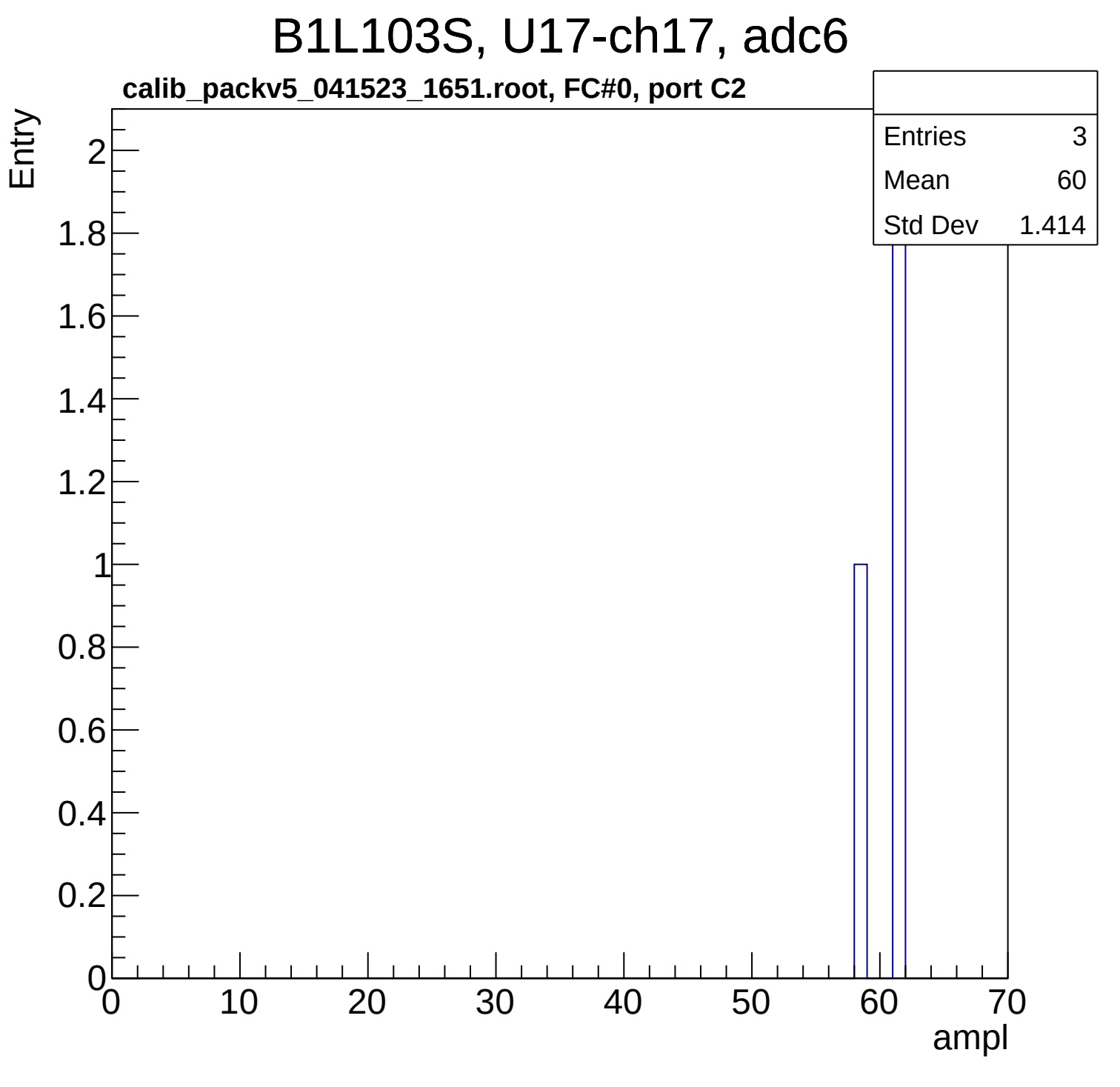

B1L103S, U17-ch17, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 36.82
Std Dev 5.537
Gaus mean : 37.4196
Gaus Width: 3.2360
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

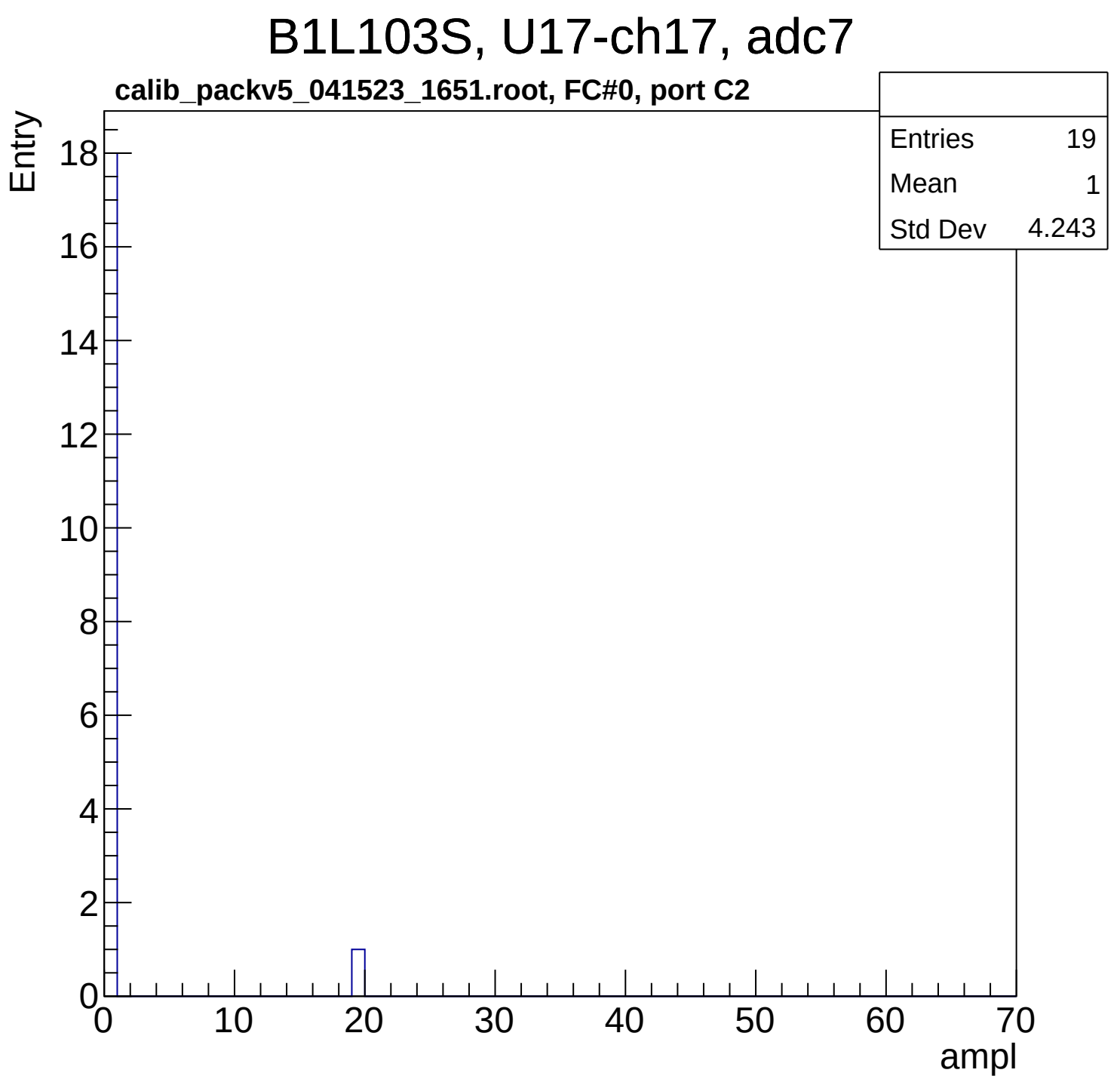

B1L103S, U17-ch17, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 38.19
Std Dev 14.25
Gaus mean : 43.6823
Gaus Width: 4.8011
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

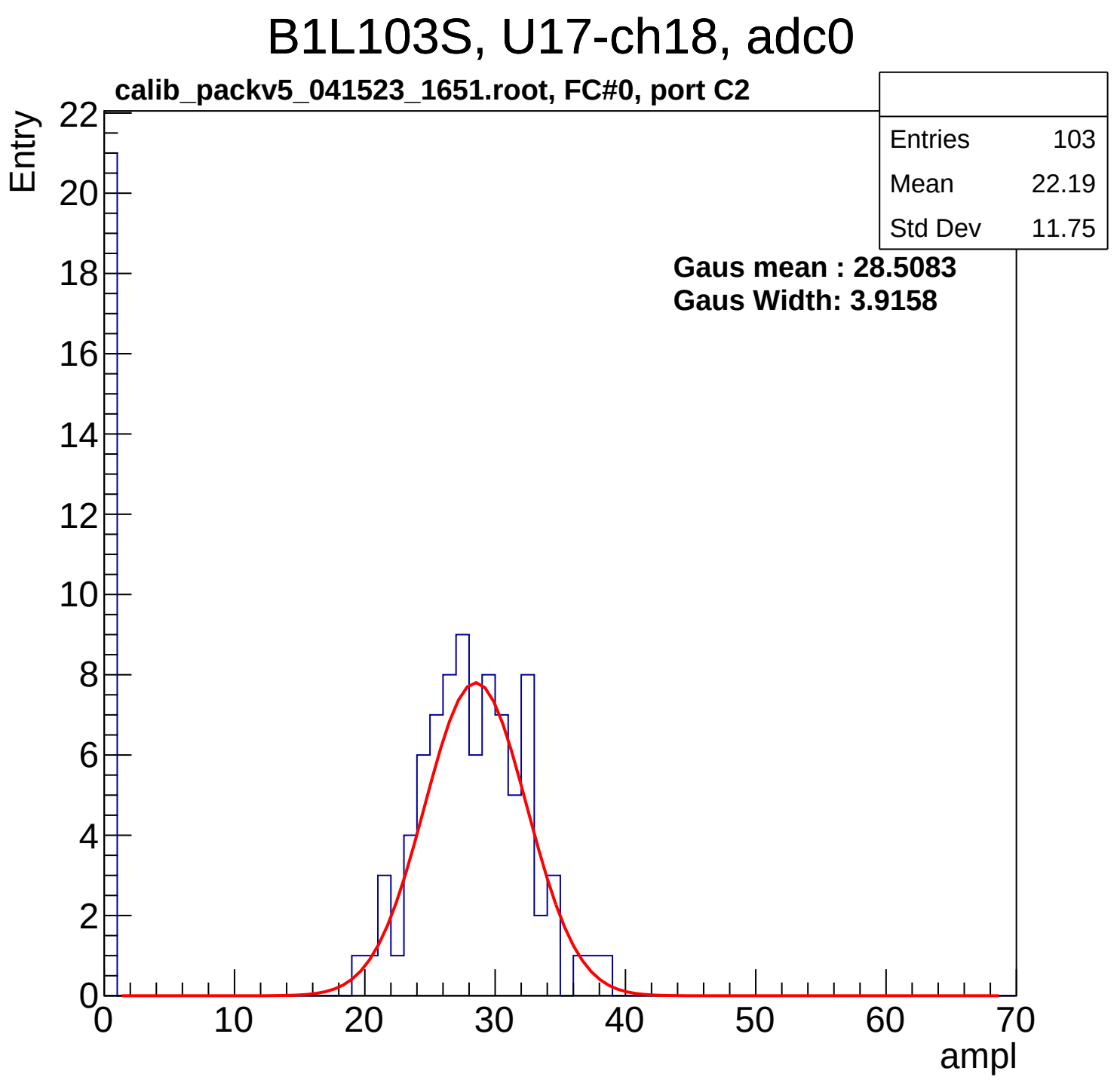

B1L103S, U17-ch17, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 49.74
Std Dev 6.608
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

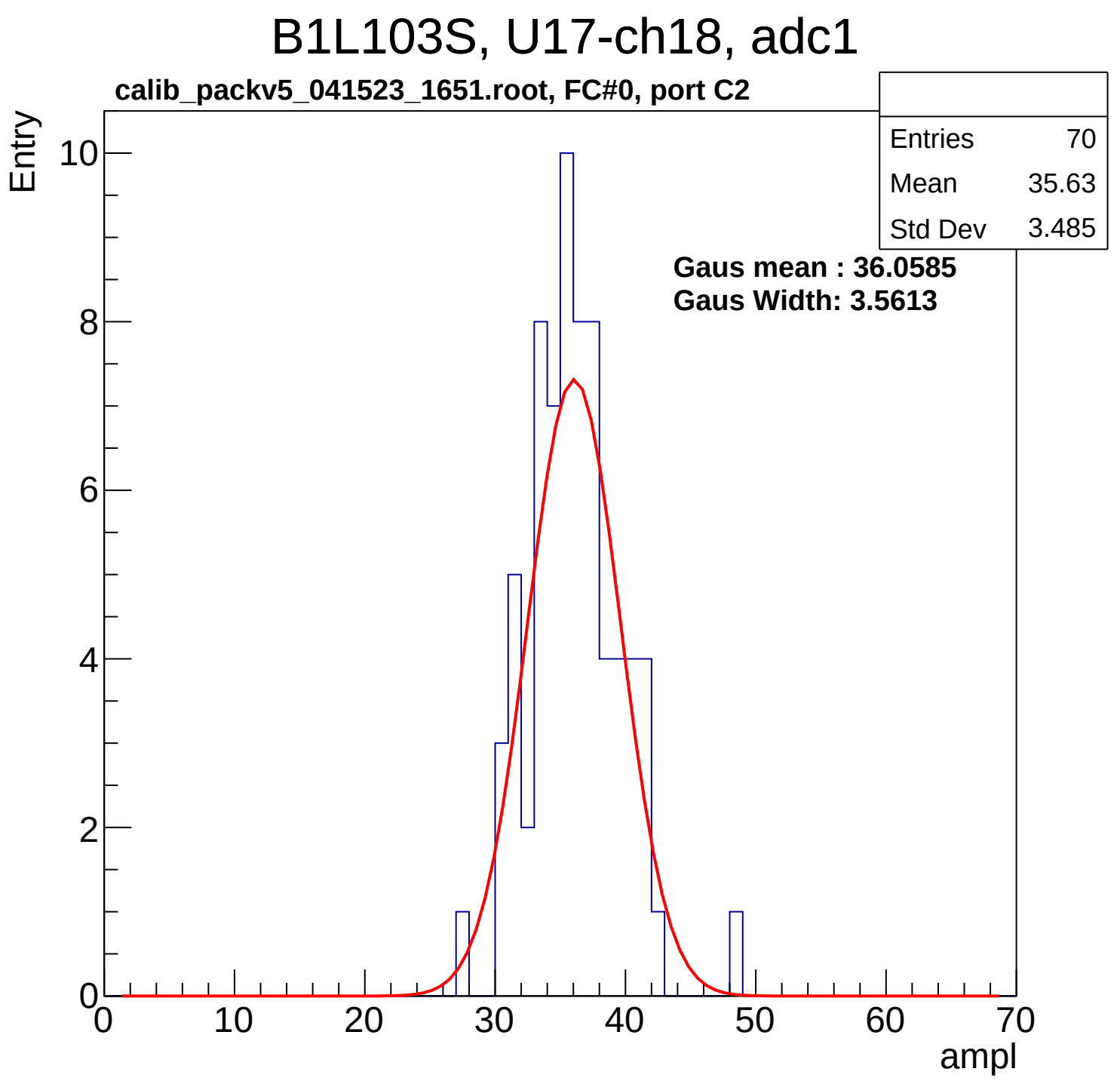

B1L103S, U17-ch17, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 56.61
Std Dev 2.849
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

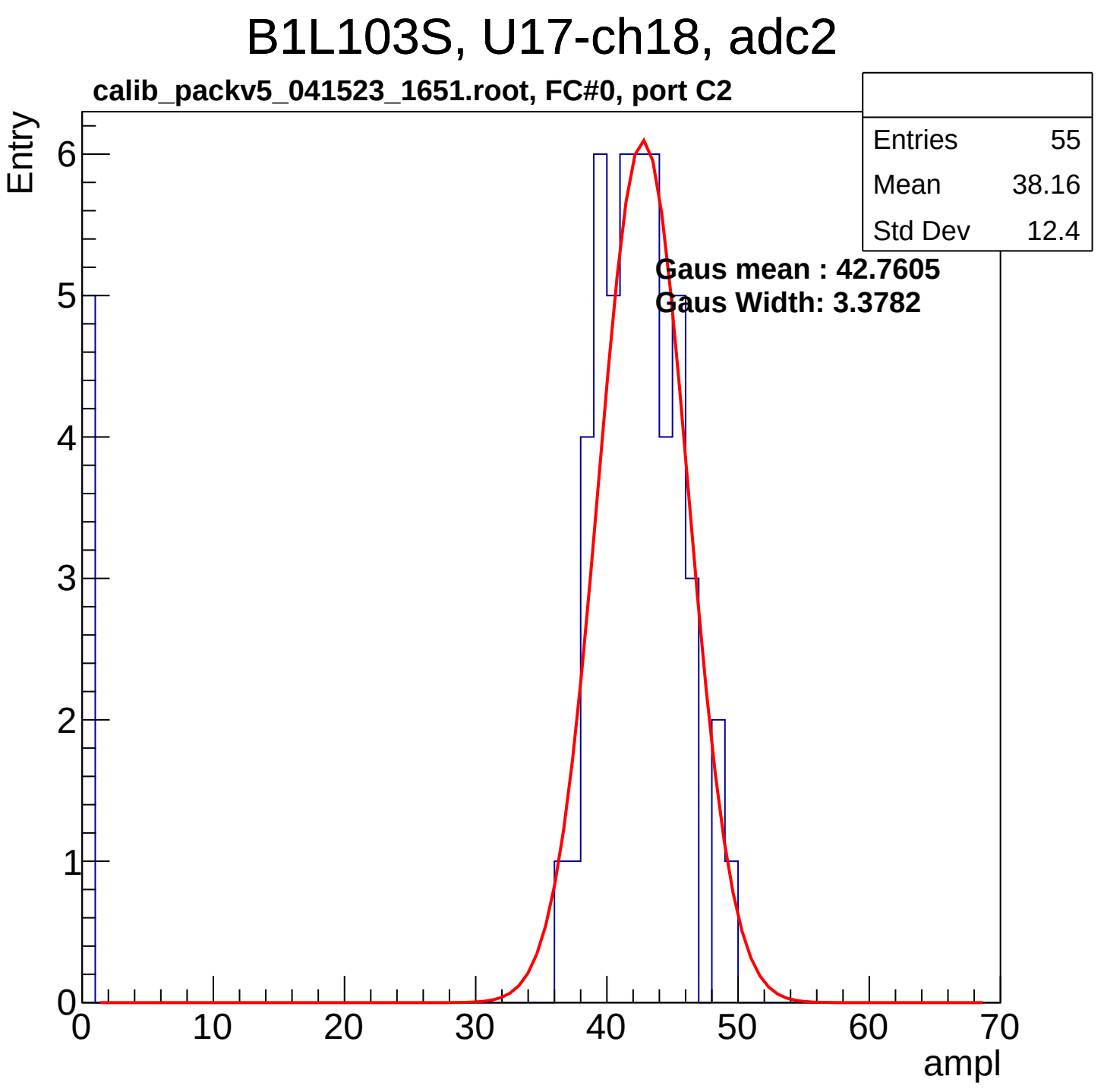

B1L103S, U17-ch17, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 59.22
Std Dev 9.623
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

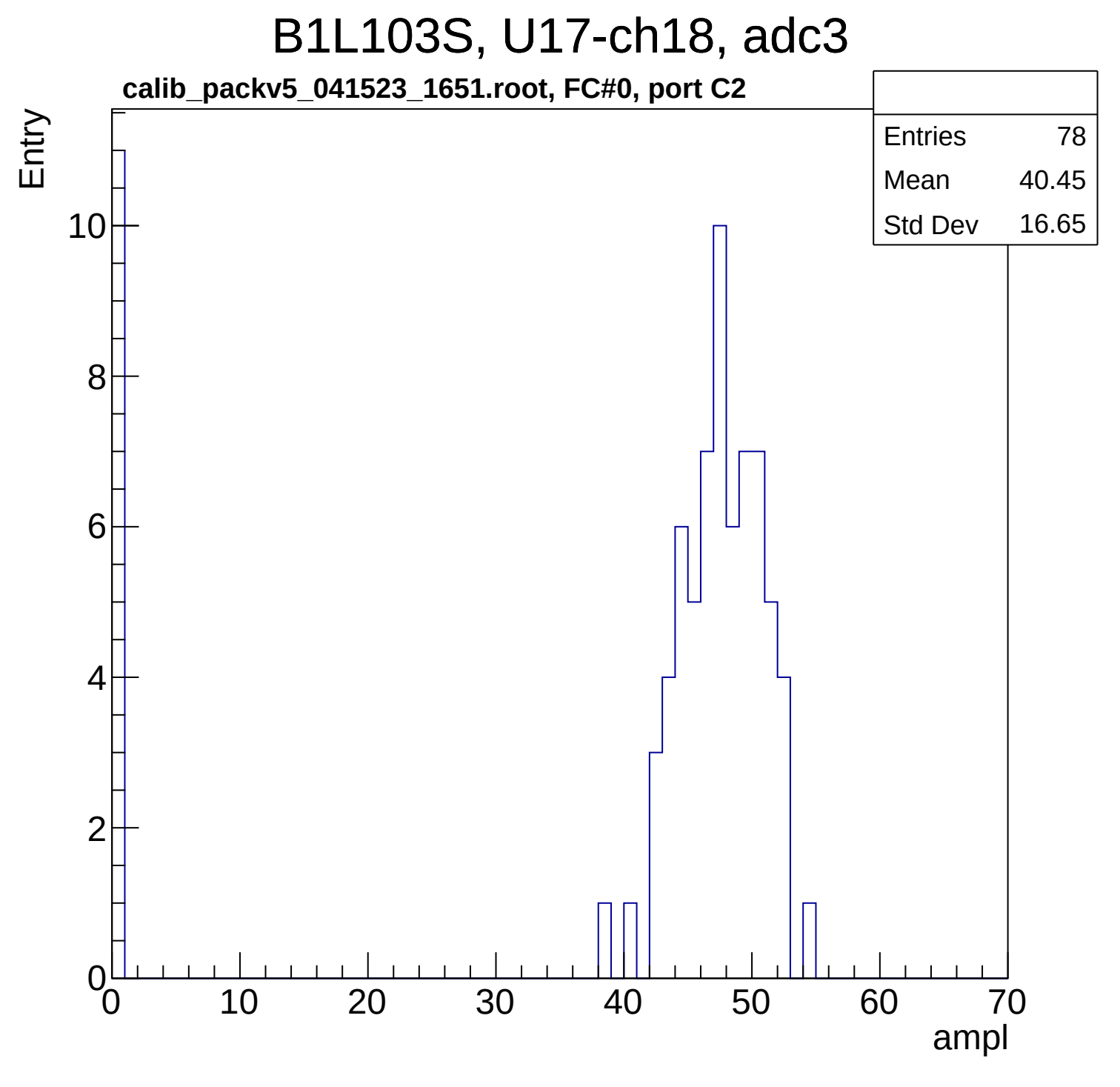

B1L103S, U17-ch17, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 60
Std Dev 1.414
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

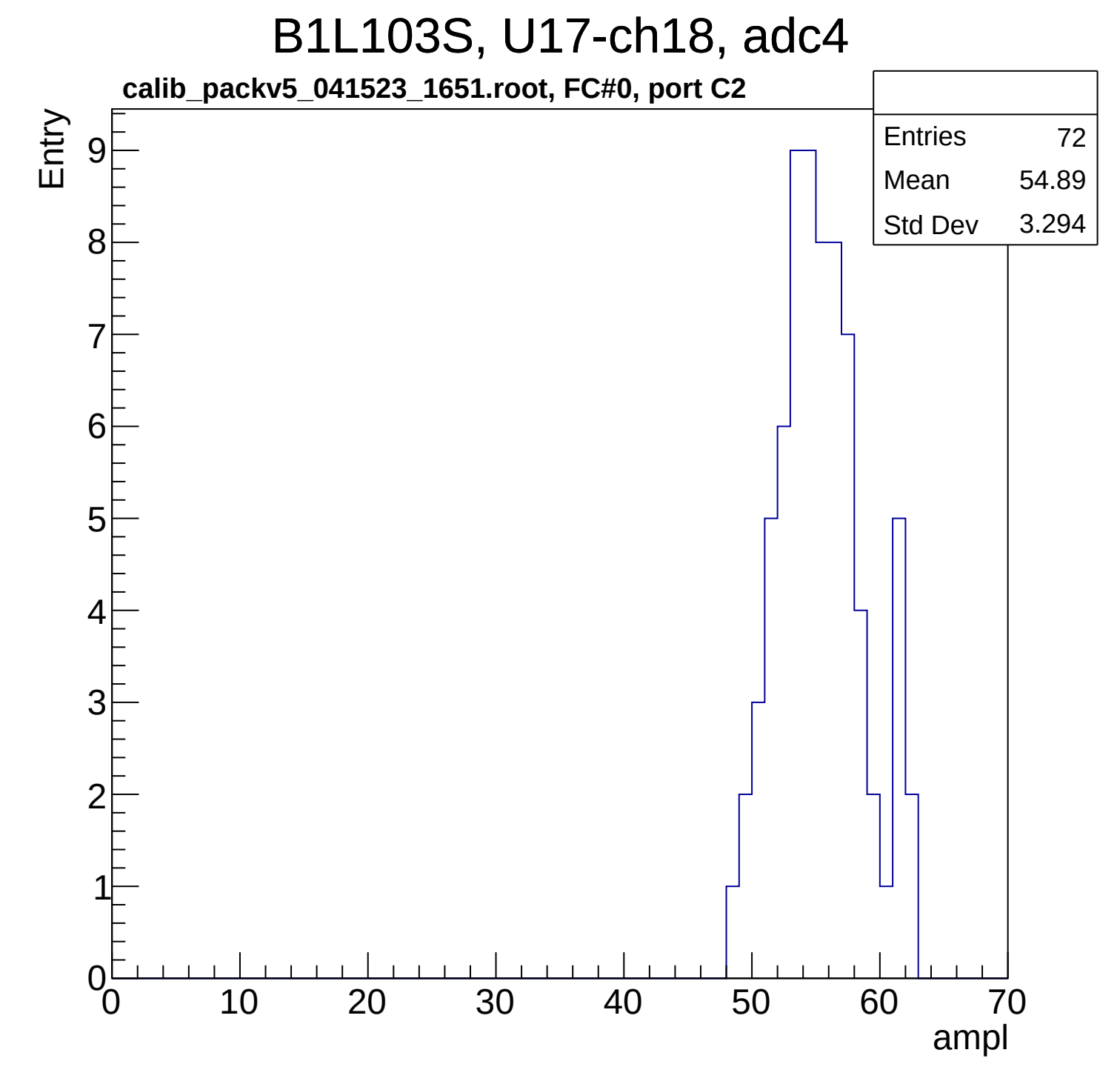

B1L103S, U17-ch17, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1
Std Dev 4.243
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

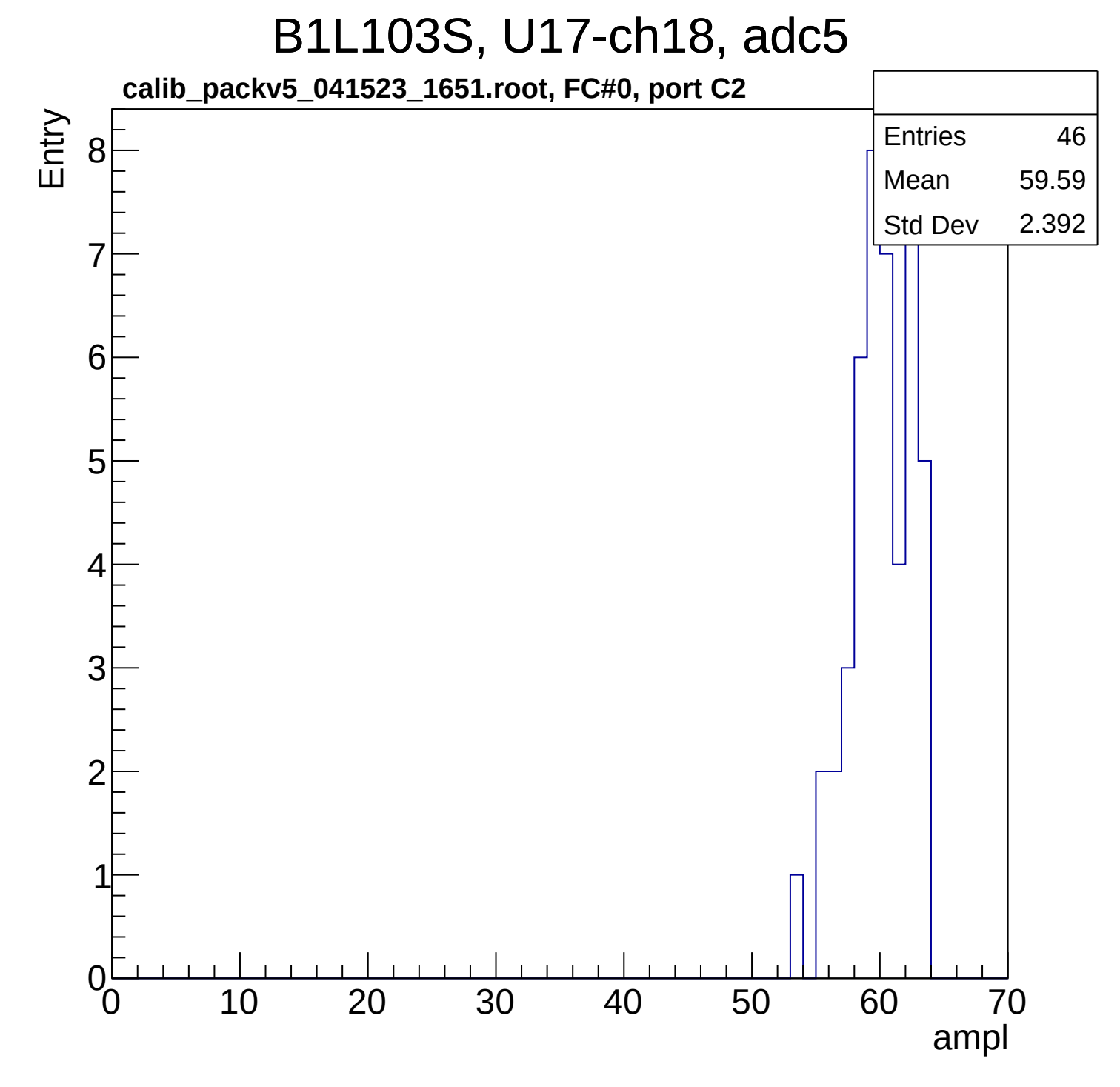

B1L103S, U17-ch18, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 22.19
Std Dev 11.75
Gaus mean : 28.5083
Gaus Width: 3.9158
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70

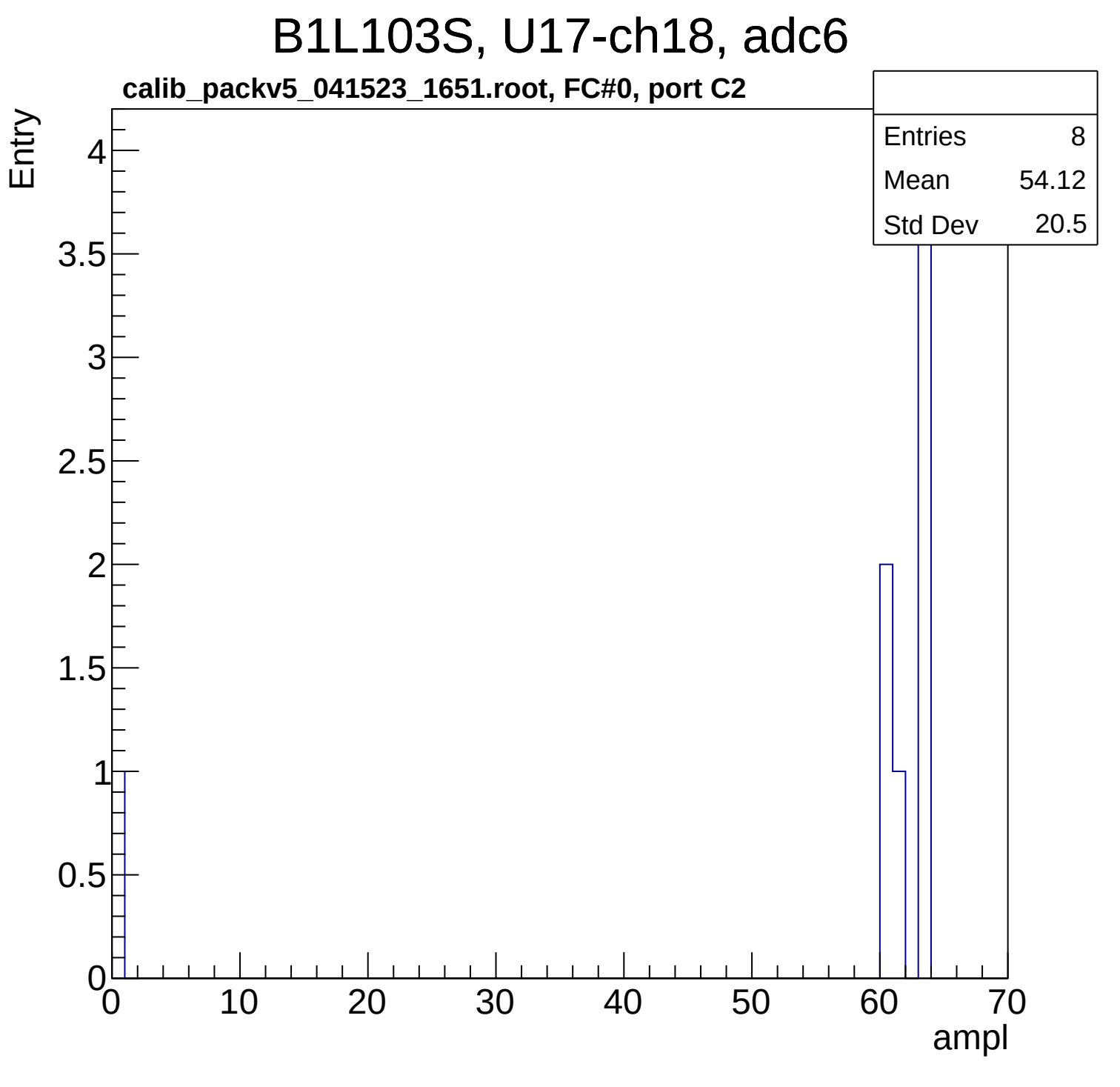

B1L103S, U17-ch18, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 35.63
Std Dev 3.485
Gaus mean : 36.0585
Gaus Width: 3.5613
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

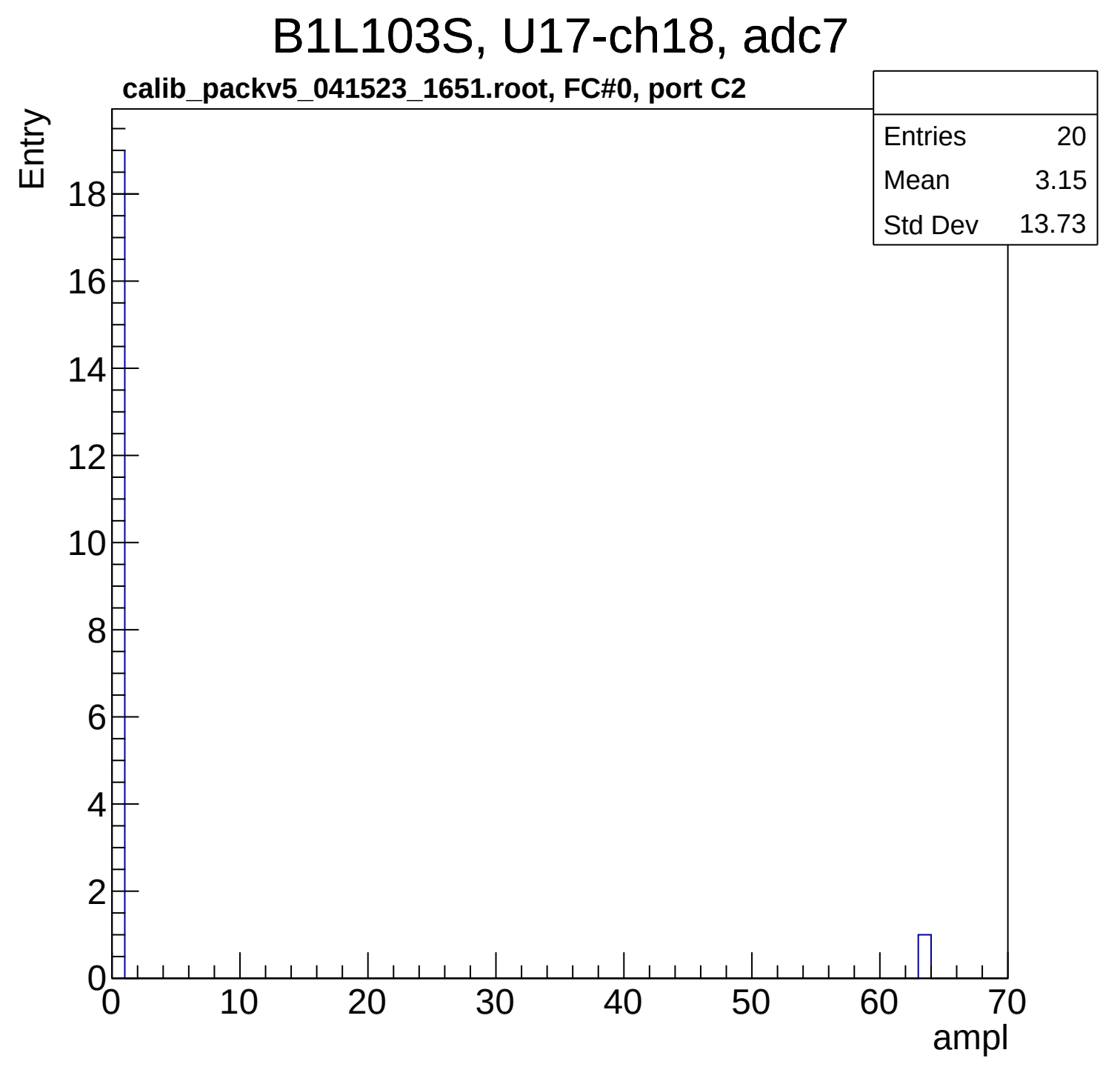

B1L103S, U17-ch18, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 38.16
Std Dev 12.4
Gaus mean : 42.7605
Gaus Width: 3.3782
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

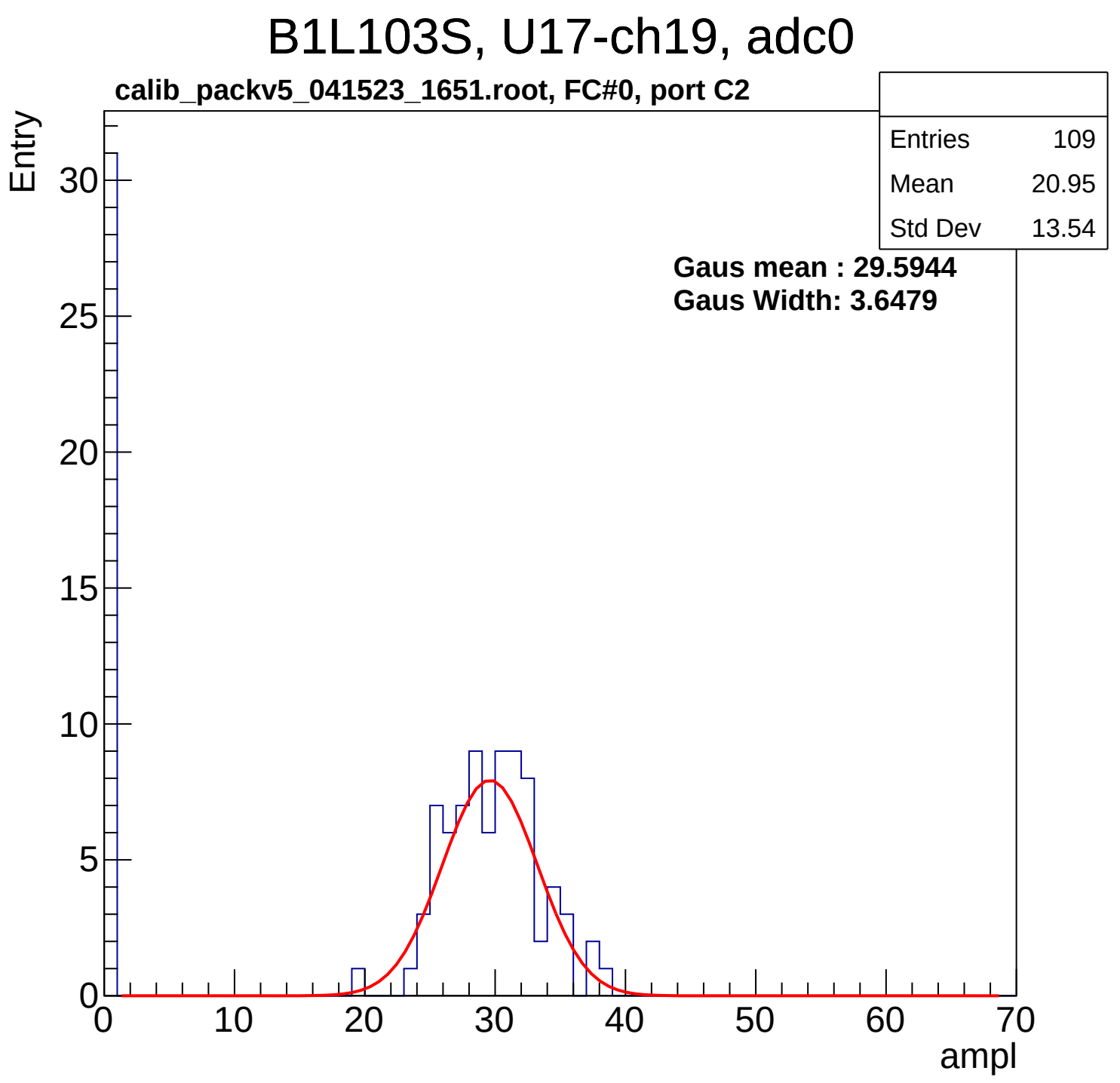

B1L103S, U17-ch18, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 40.45
Std Dev 16.65
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

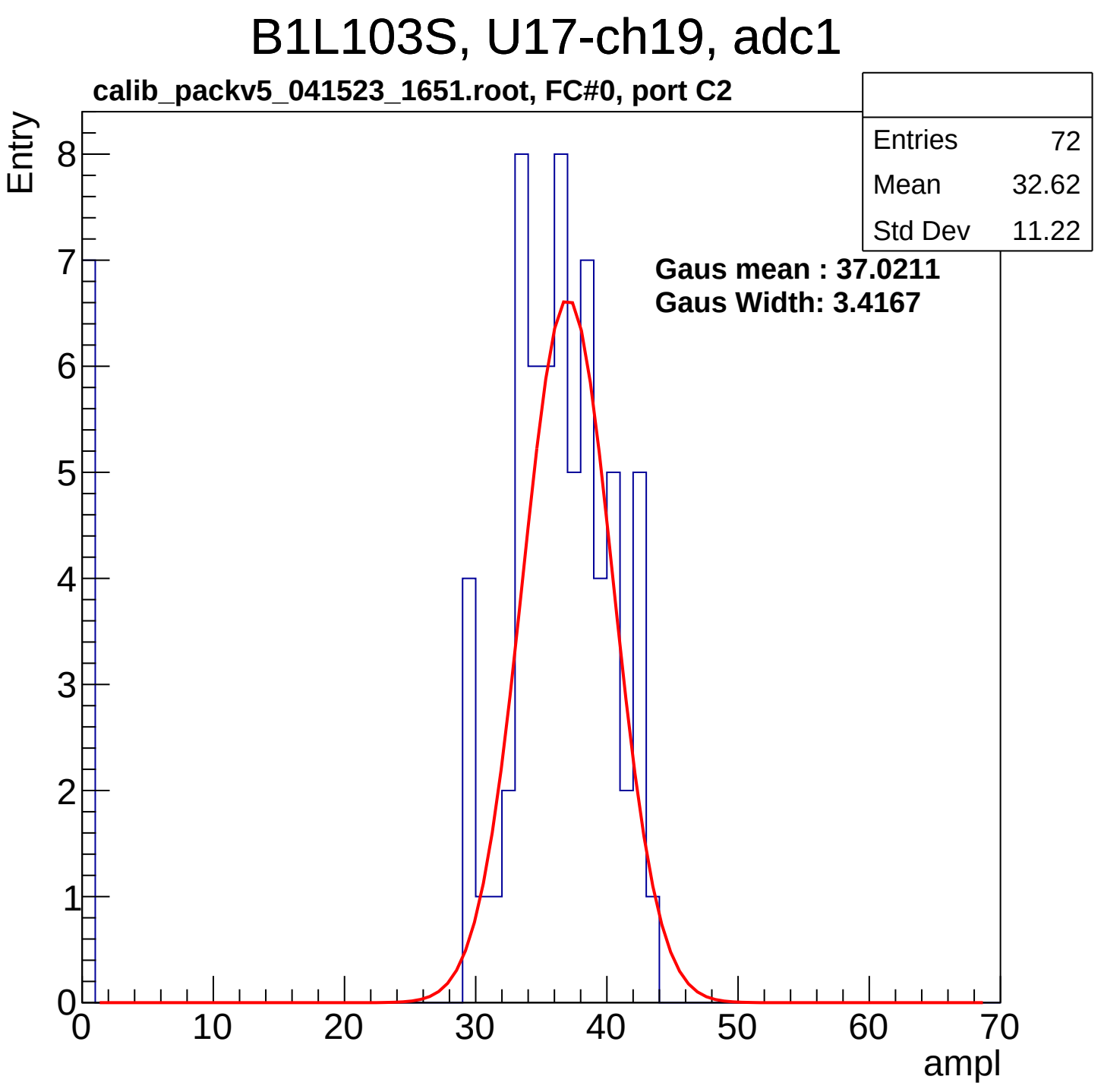

B1L103S, U17-ch18, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 54.89
Std Dev 3.294
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

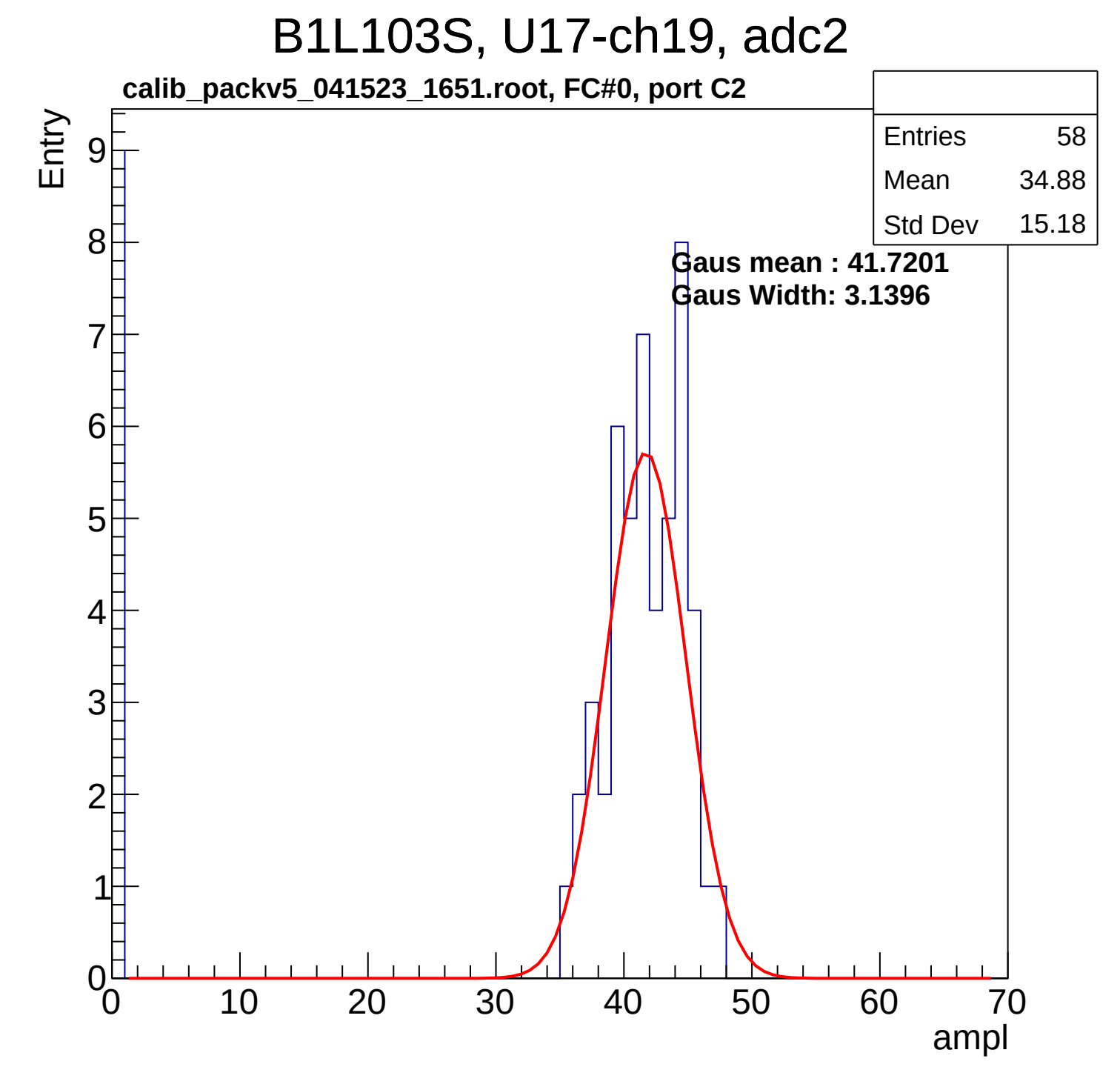

B1L103S, U17-ch18, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 59.59
Std Dev 2.392
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

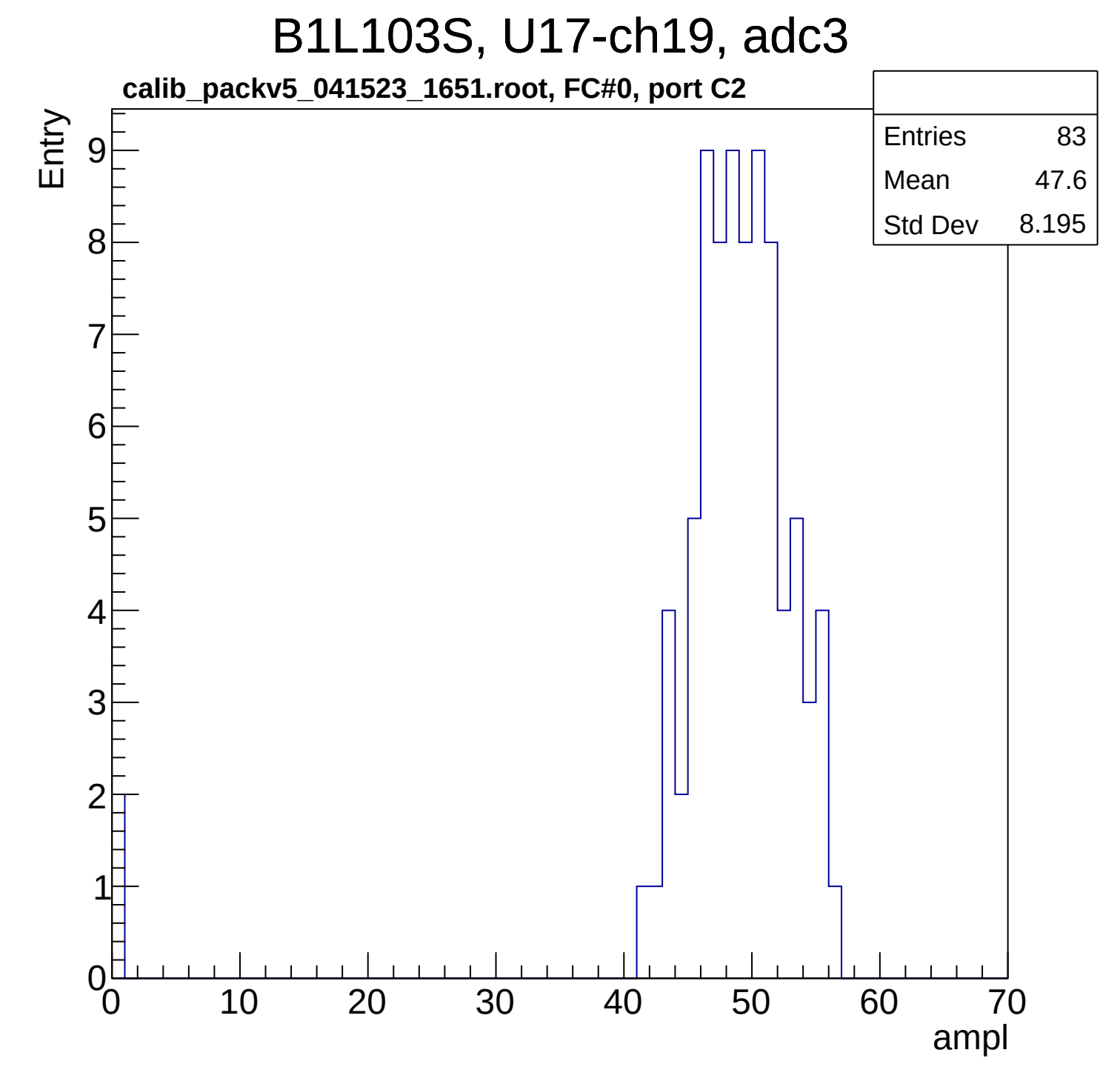

B1L103S, U17-ch18, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 54.12
Std Dev 20.5
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

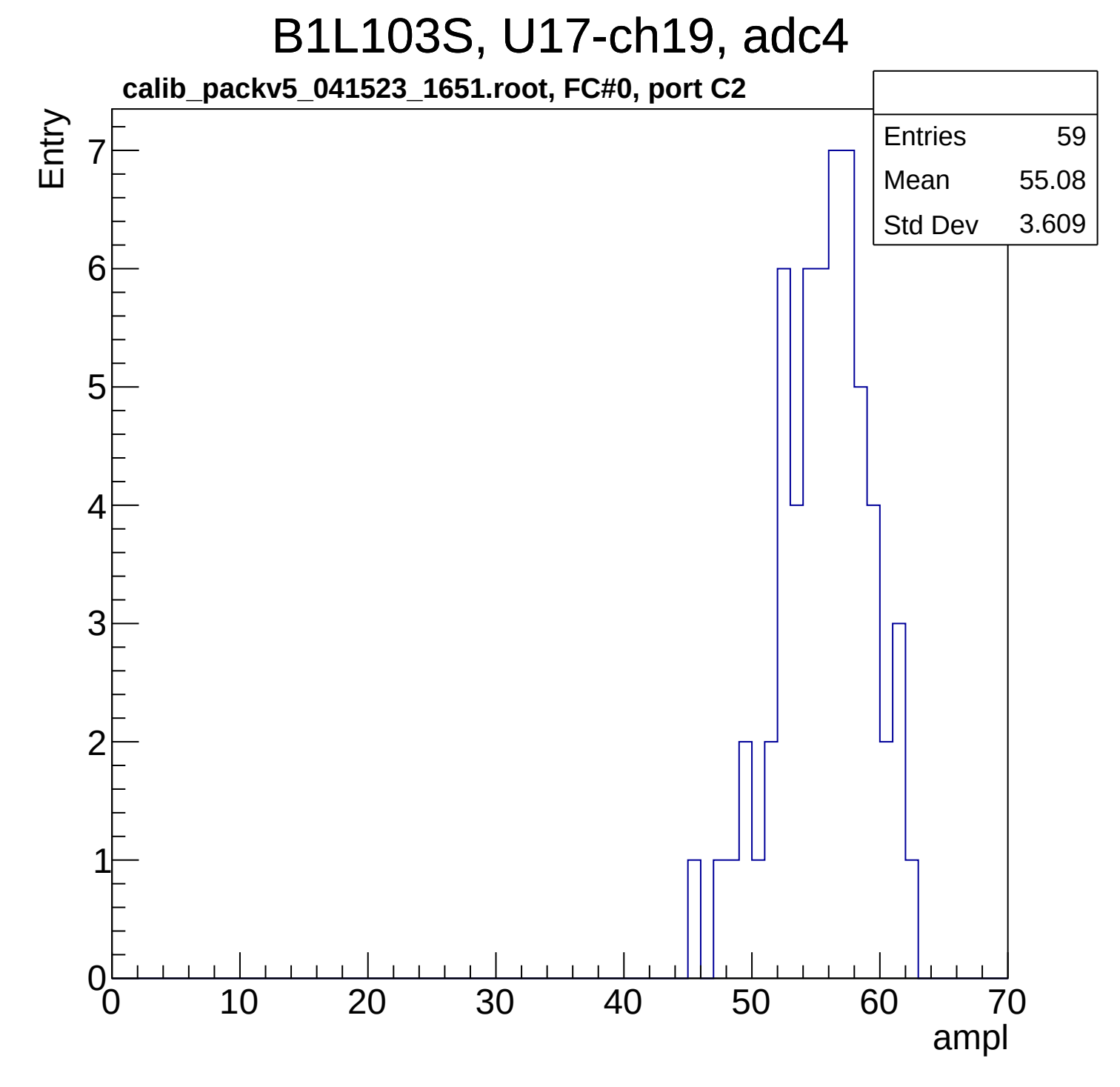

B1L103S, U17-ch18, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

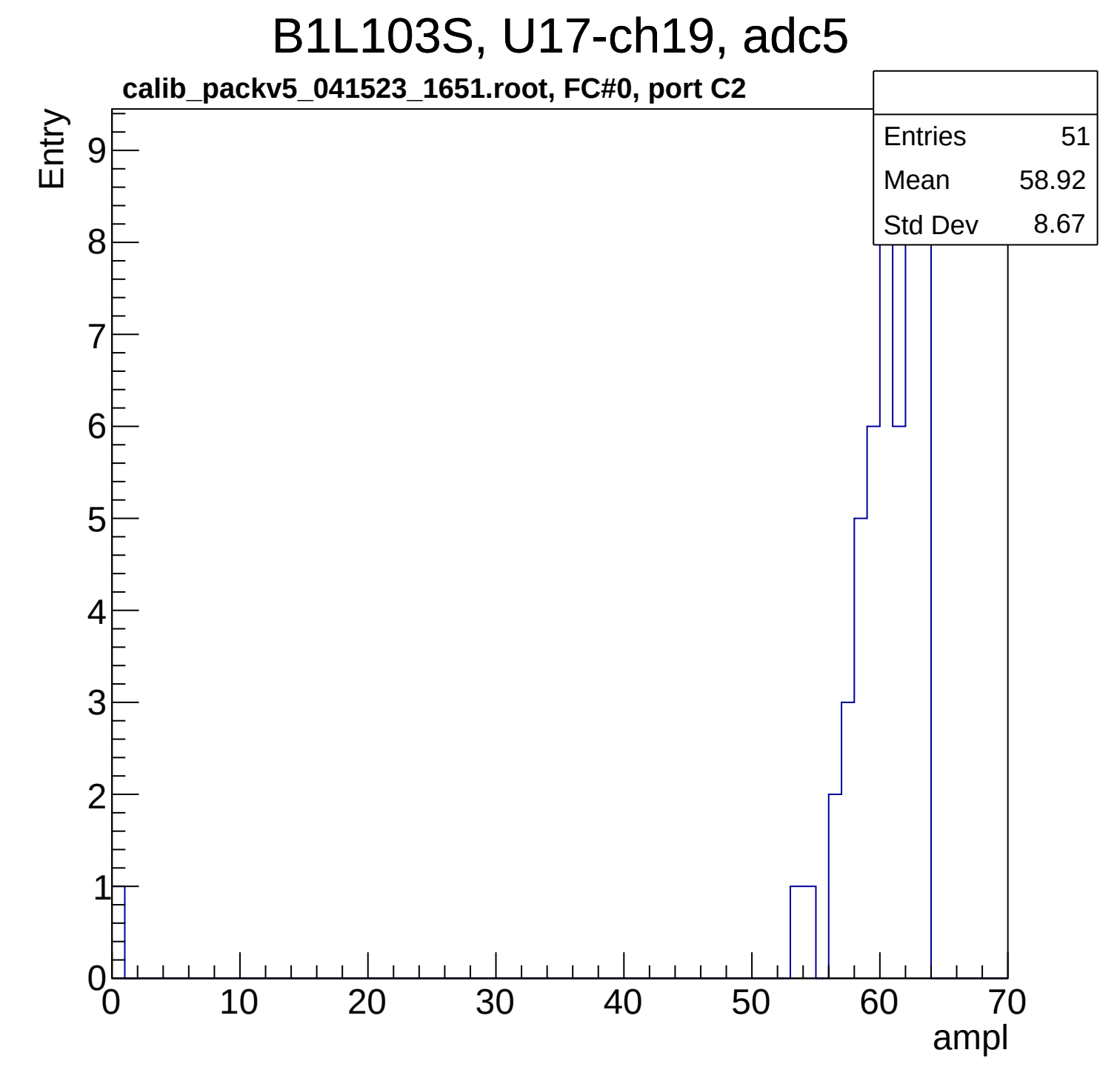

B1L103S, U17-ch19, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 109
Mean 20.95
Std Dev 13.54
Gaus mean : 29.5944
Gaus Width: 3.6479
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70

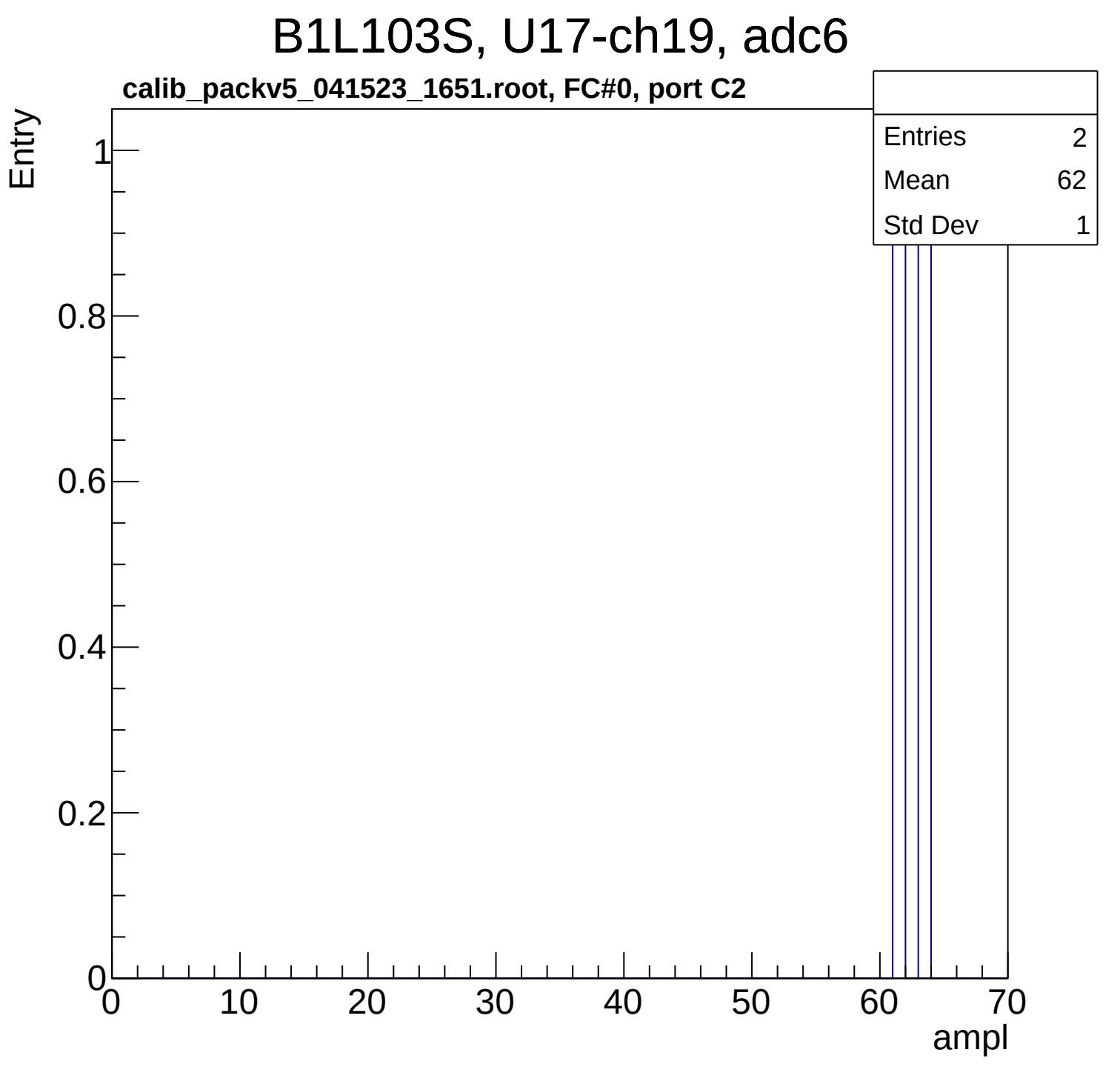

B1L103S, U17-ch19, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 32.62
Std Dev 11.22
Gaus mean : 37.0211
Gaus Width: 3.4167
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

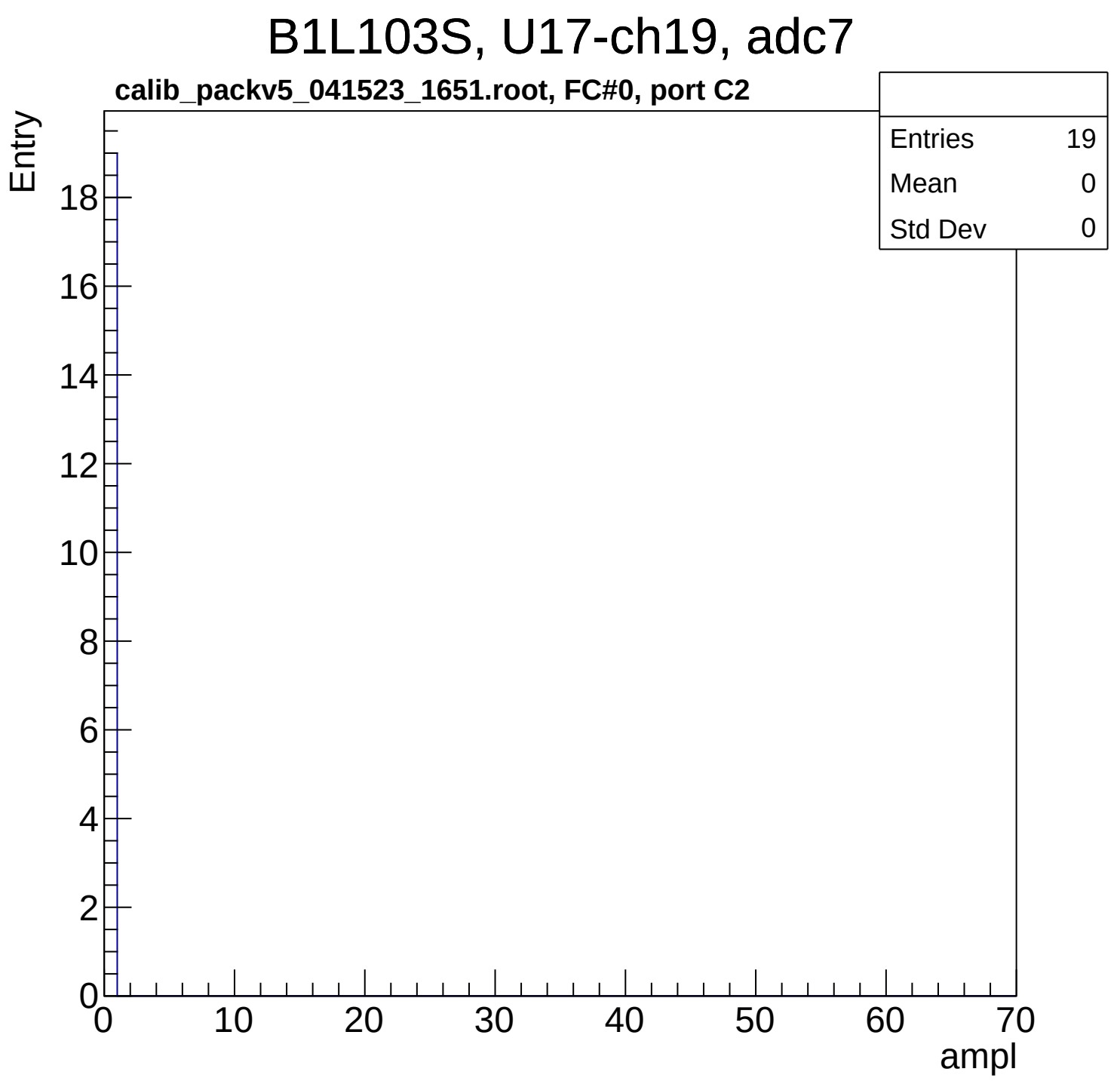

B1L103S, U17-ch19, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 34.88
Std Dev 15.18
Gaus mean : 41.7201
Gaus Width: 3.1396
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

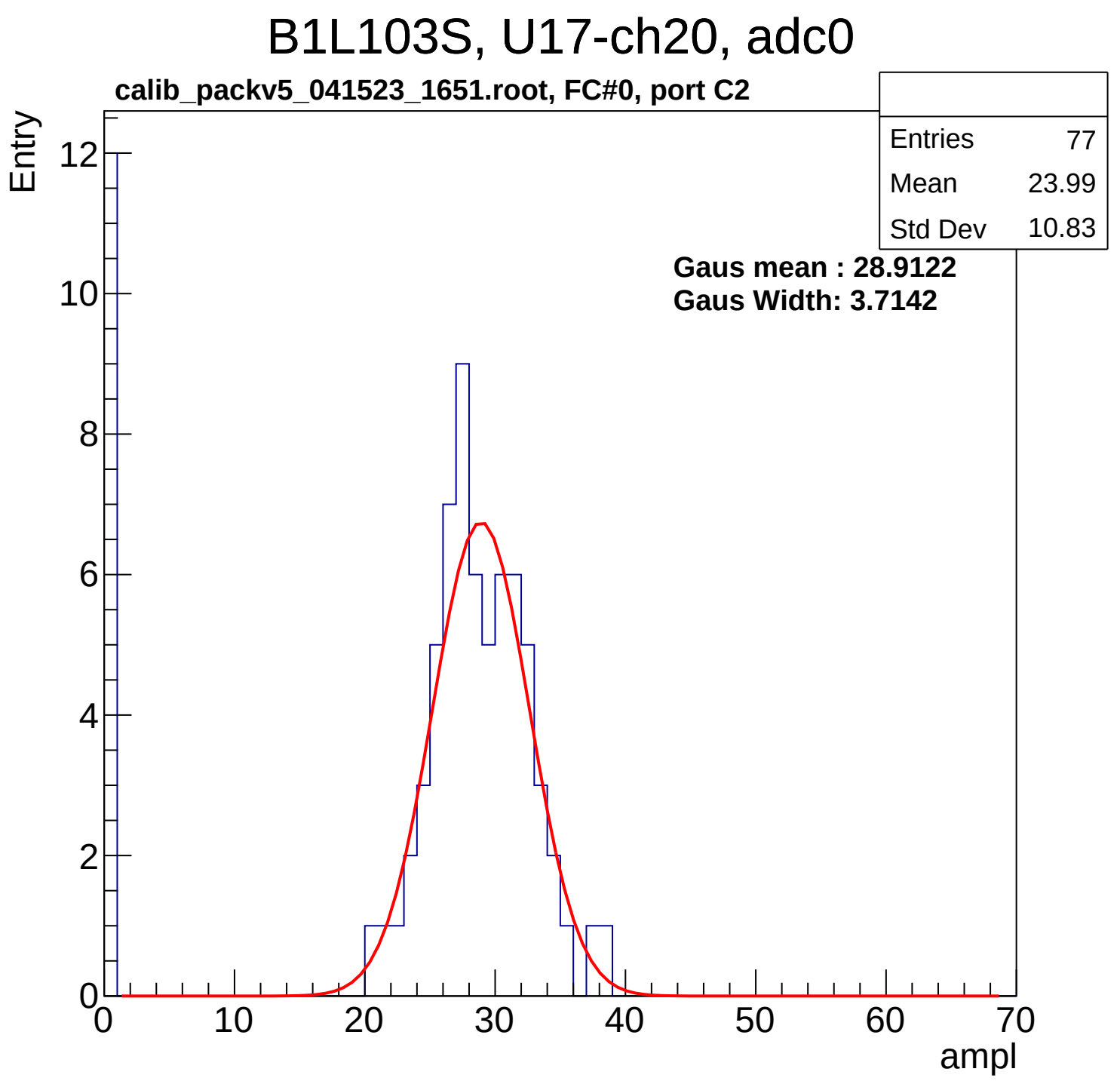

B1L103S, U17-ch19, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 47.6
Std Dev 8.195
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

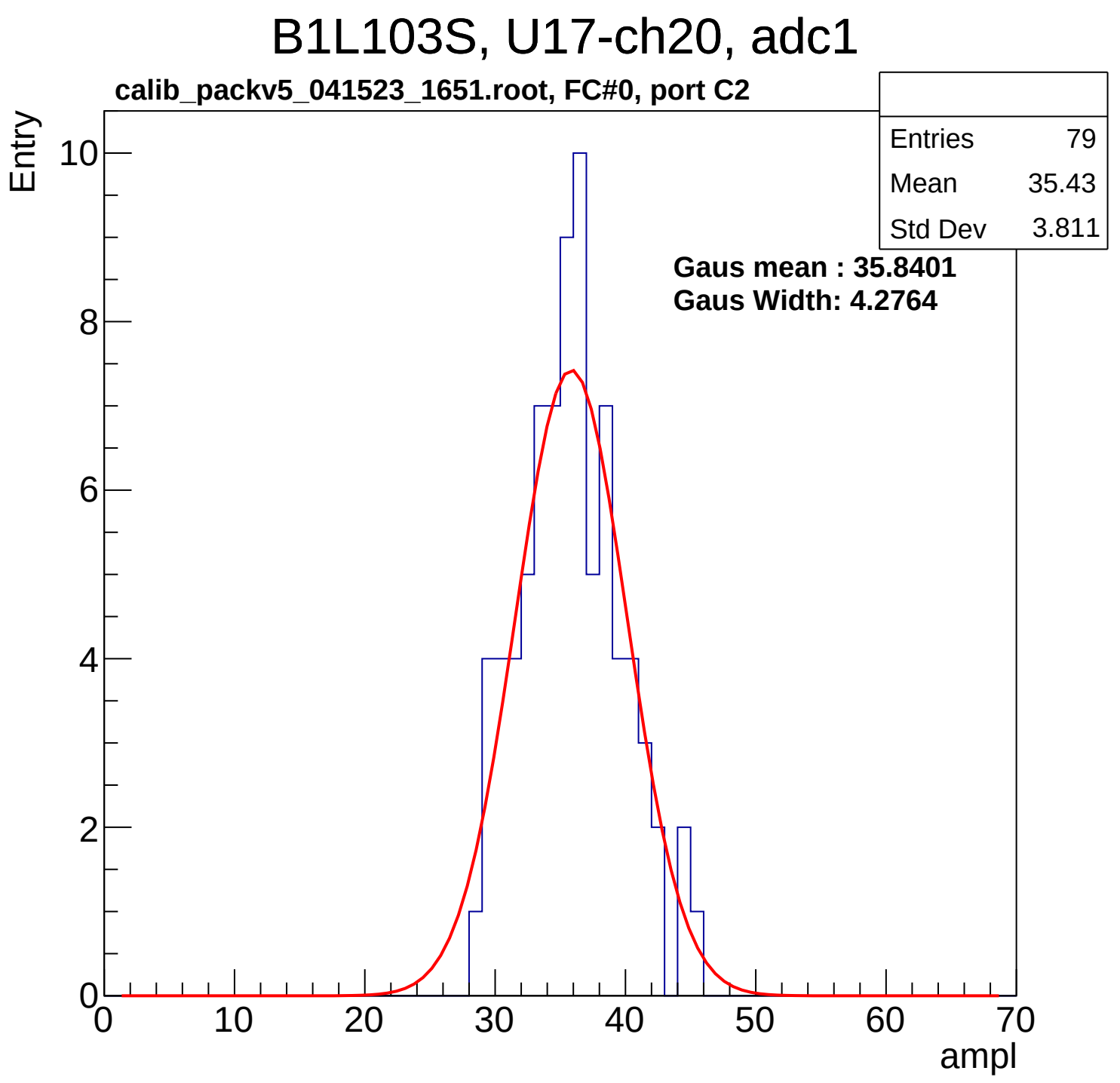

B1L103S, U17-ch19, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 55.08
Std Dev 3.609
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

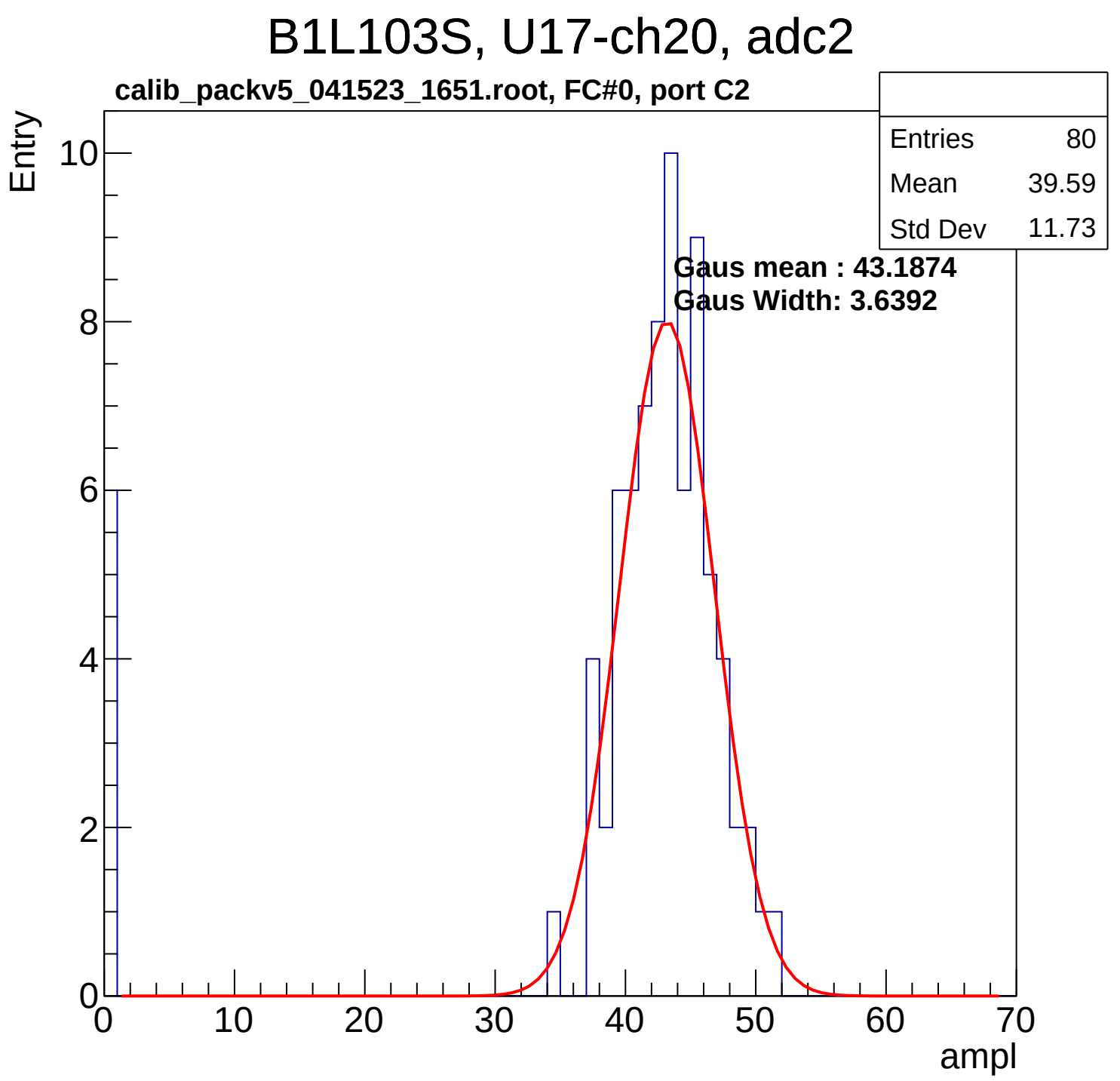

B1L103S, U17-ch19, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.92
Std Dev 8.67
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

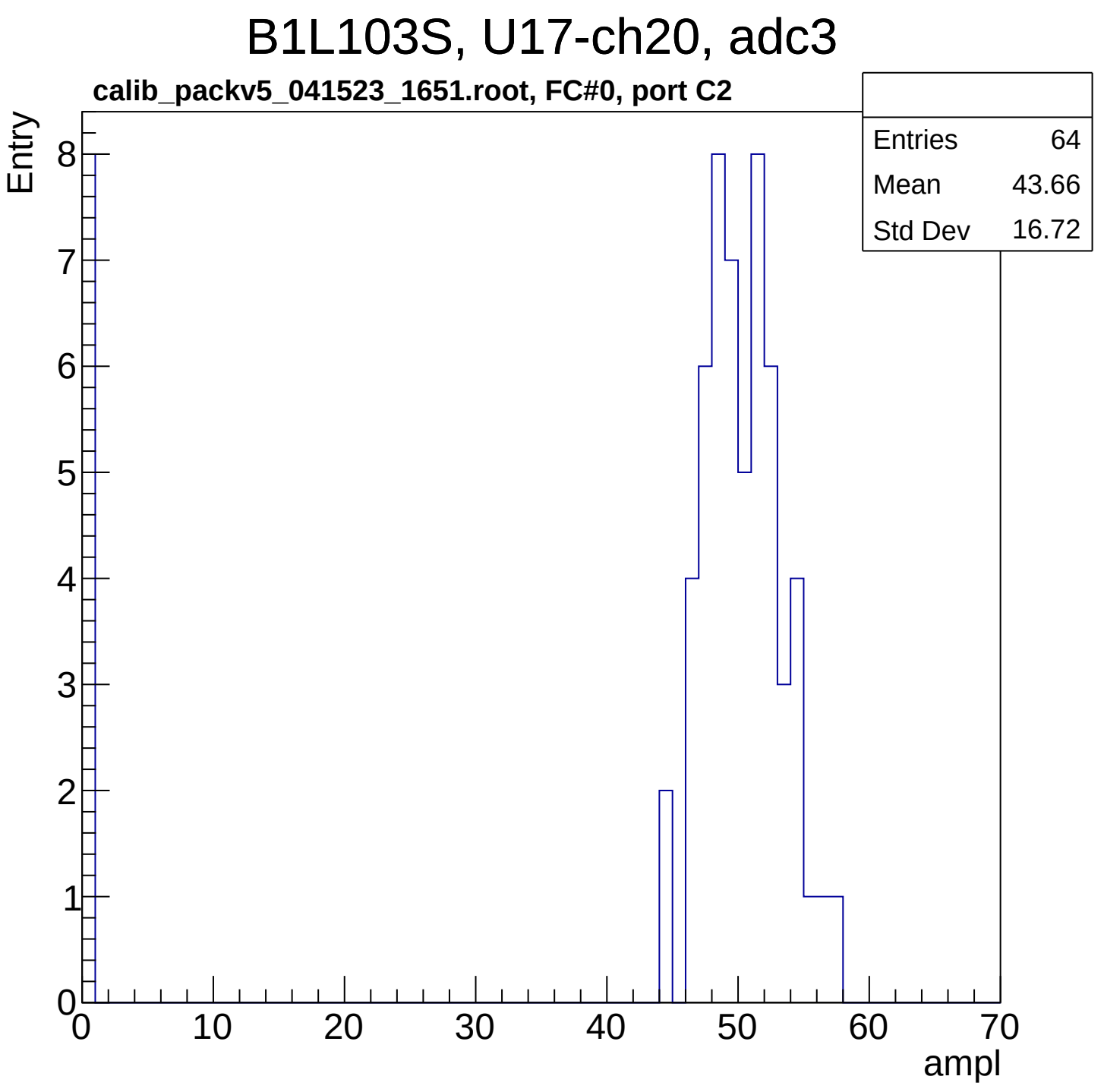

B1L103S, U17-ch19, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62
Std Dev 1
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

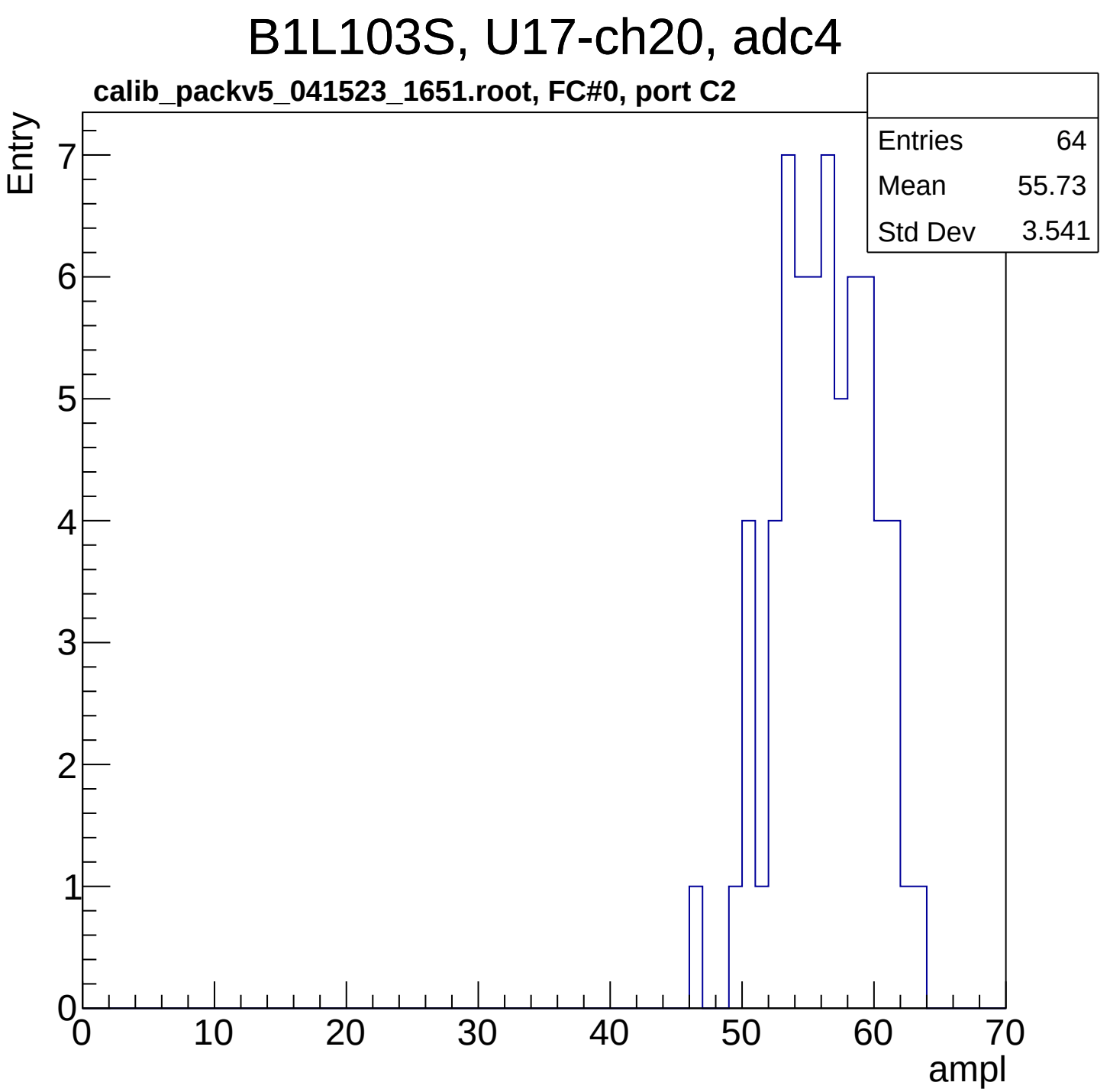

B1L103S, U17-ch19, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

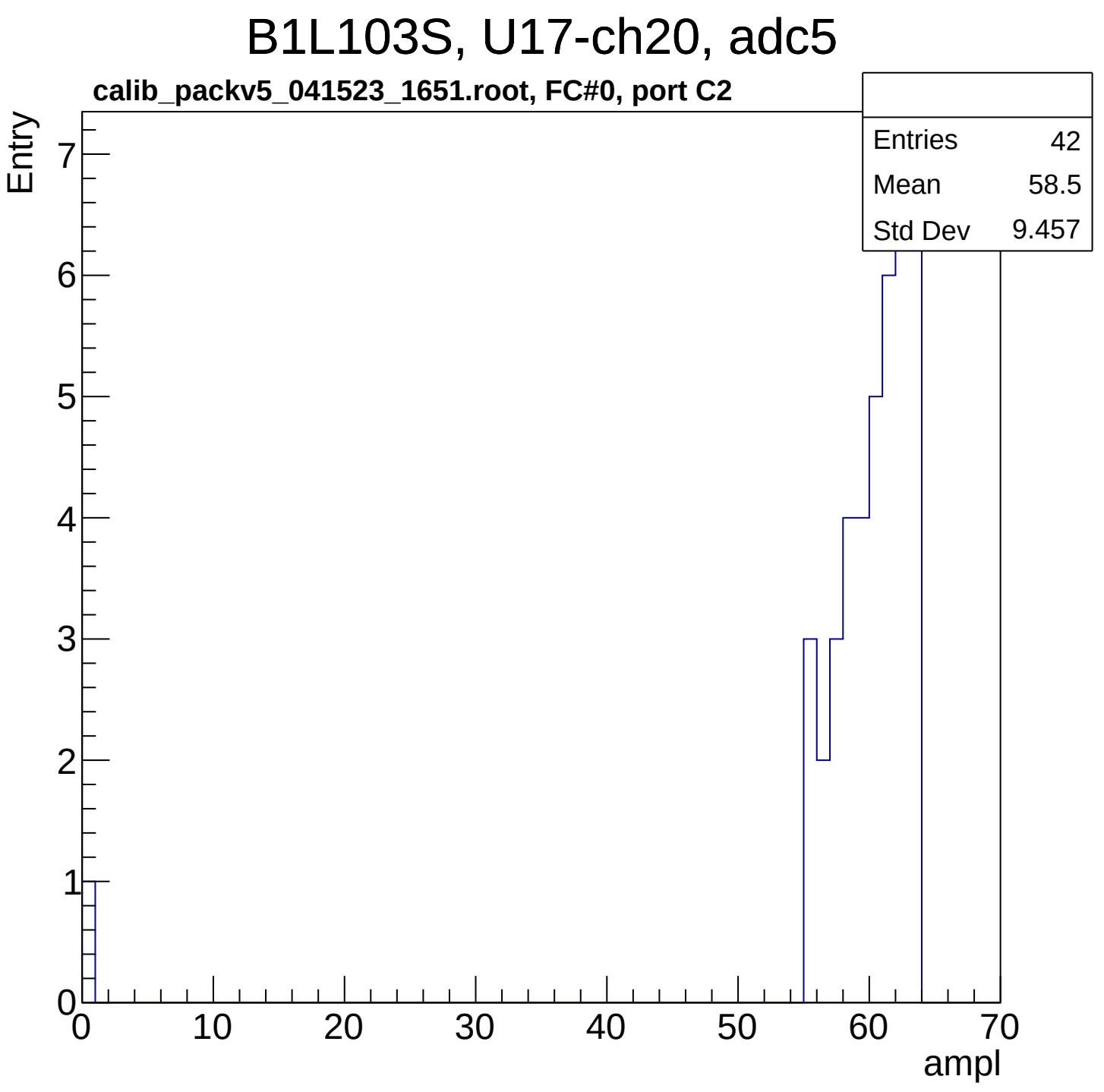

B1L103S, U17-ch20, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 23.99
Std Dev 10.83
Gaus mean : 28.9122
Gaus Width: 3.7142
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

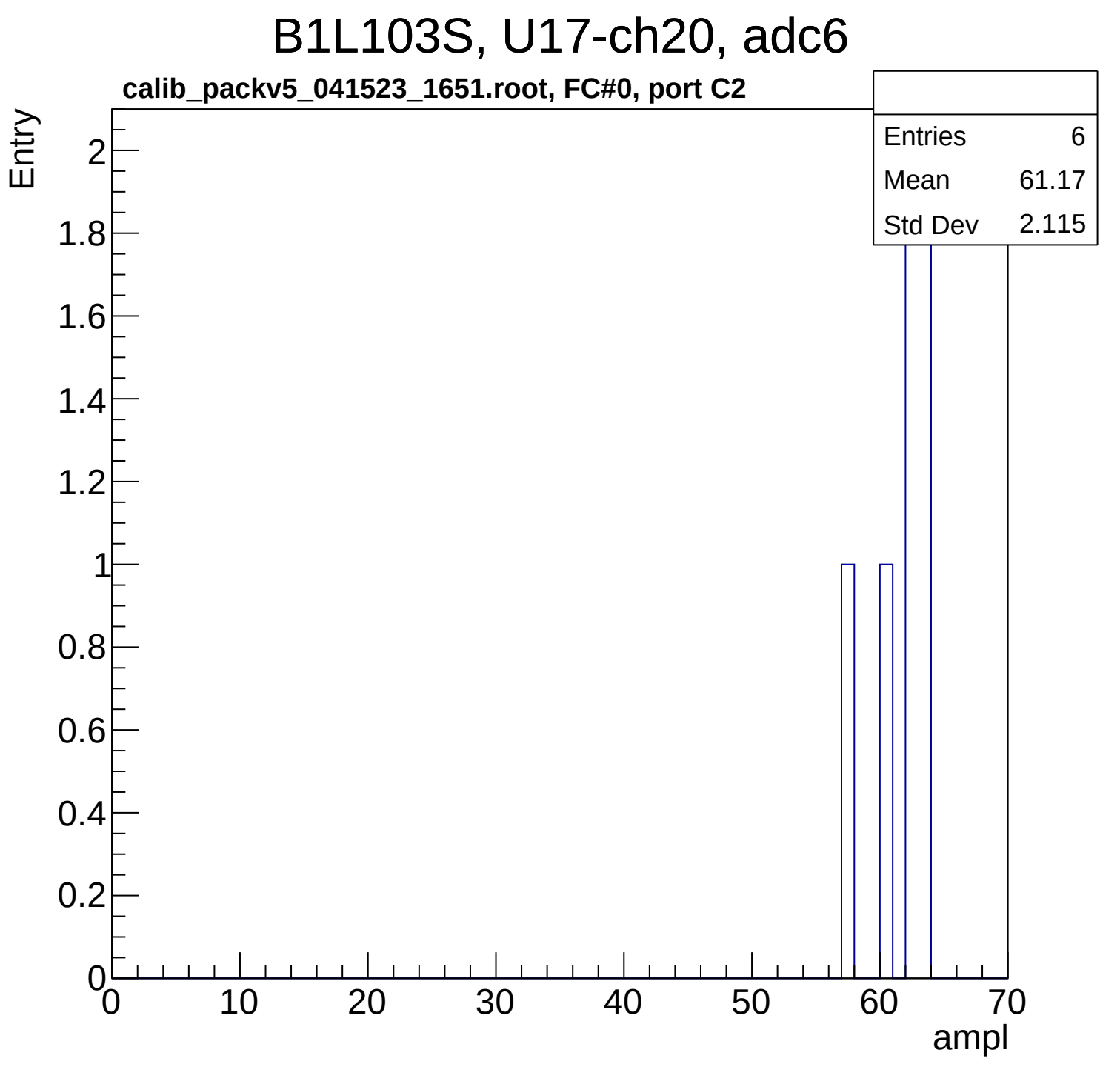

B1L103S, U17-ch20, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 35.43
Std Dev 3.811
Gaus mean : 35.8401
Gaus Width: 4.2764
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

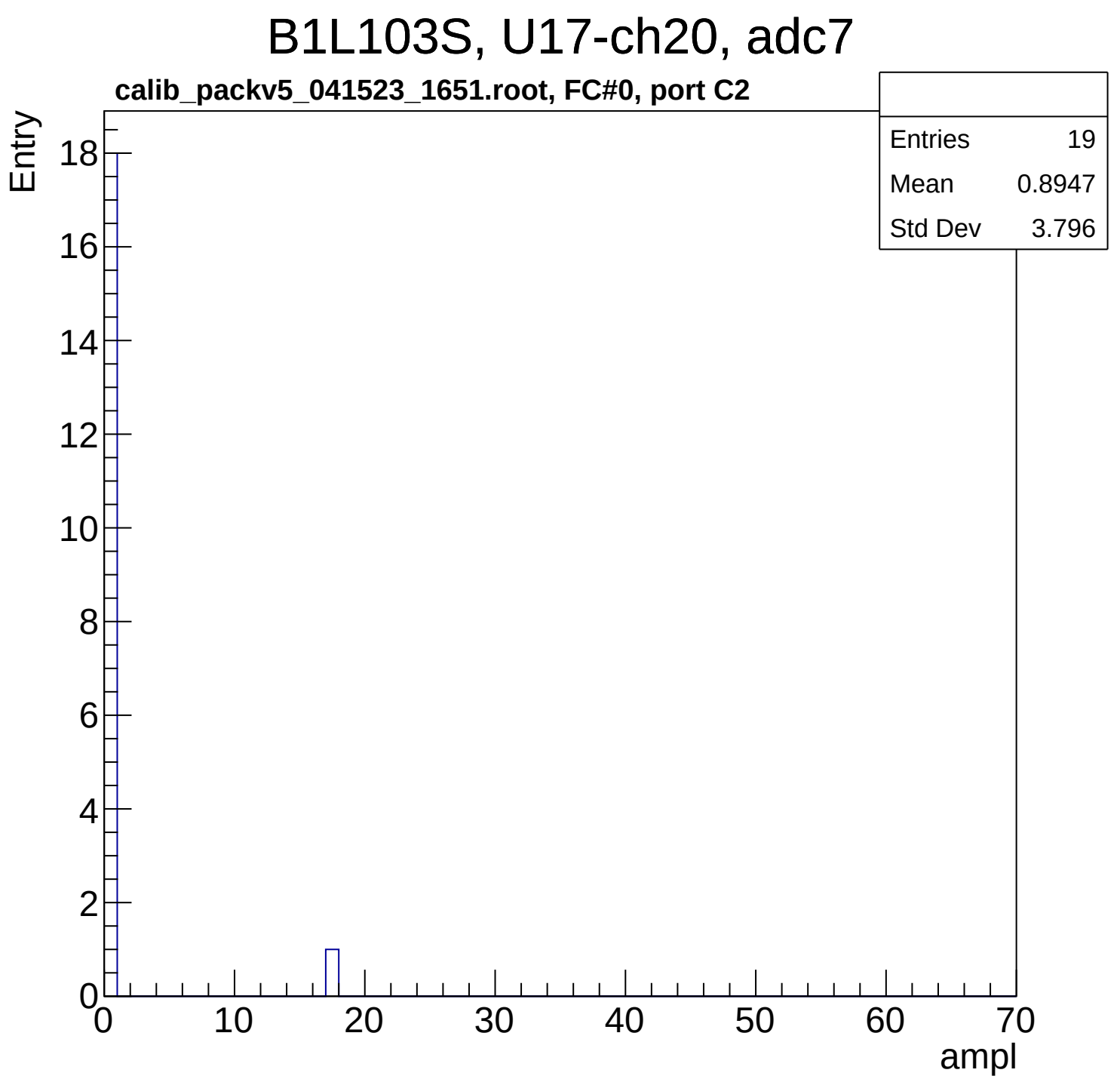

B1L103S, U17-ch20, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 39.59
Std Dev 11.73
Gaus mean : 43.1874
Gaus Width: 3.6392
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

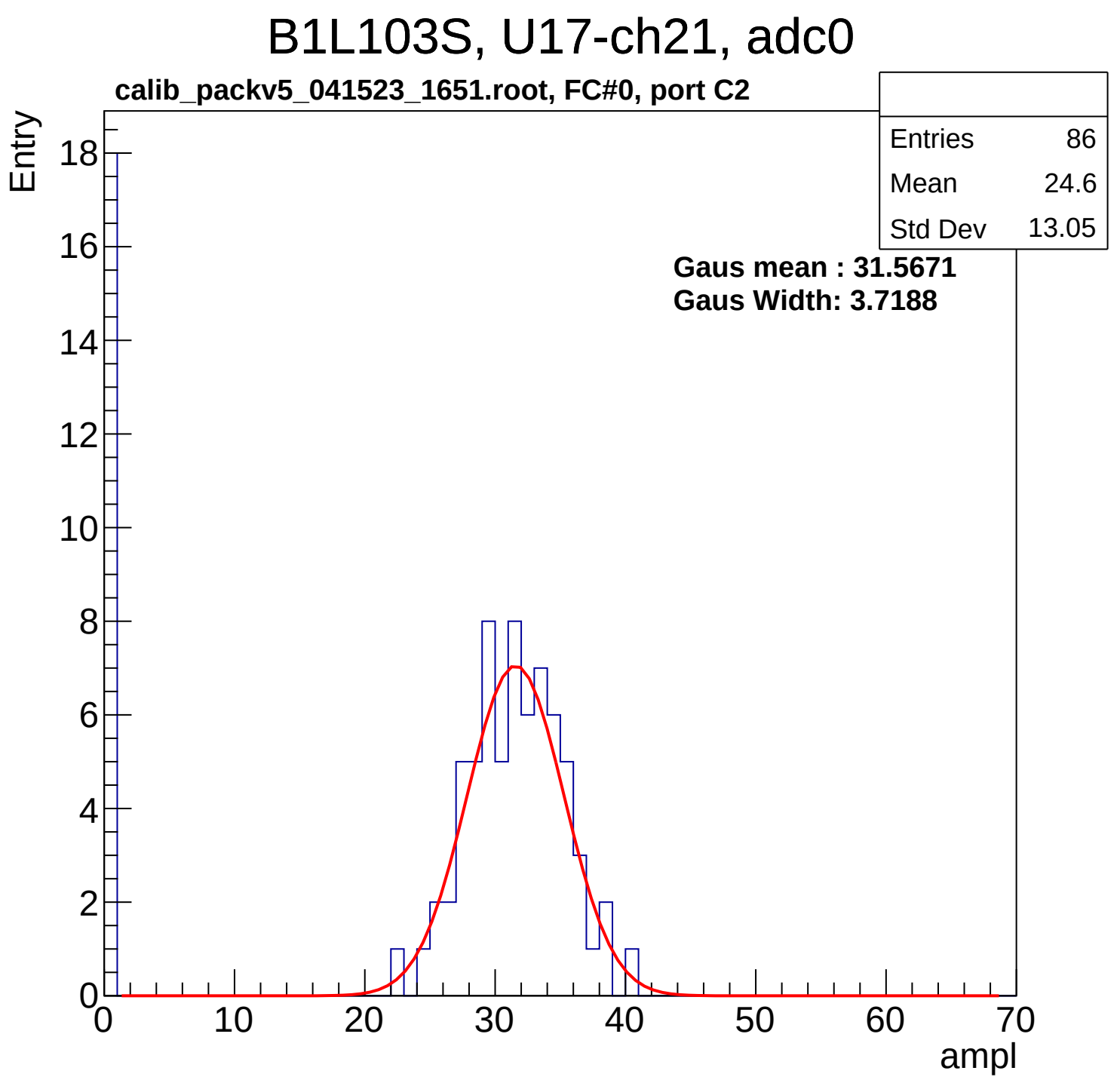

B1L103S, U17-ch20, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 43.66
Std Dev 16.72
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

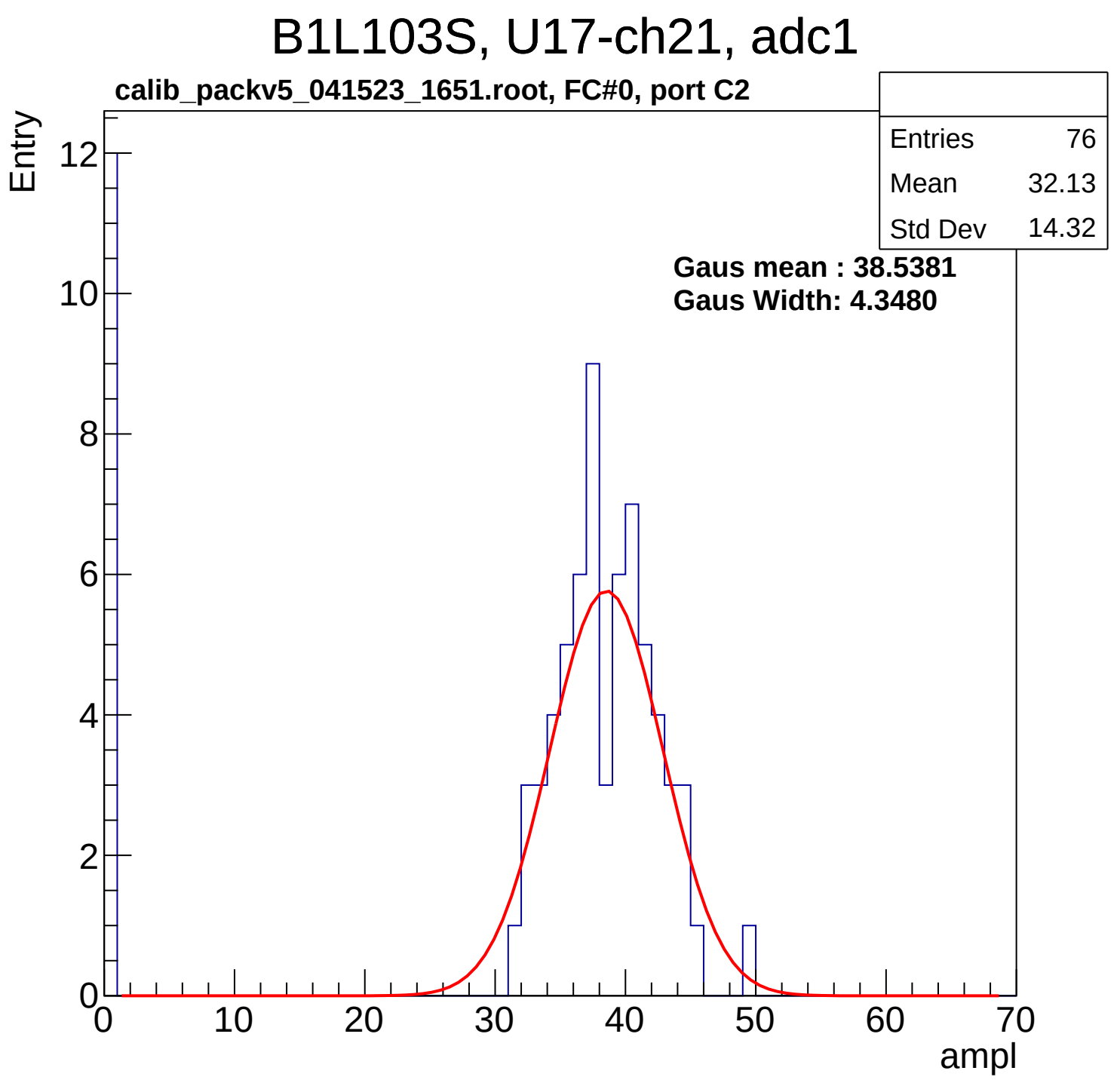

B1L103S, U17-ch20, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 55.73
Std Dev 3.541
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

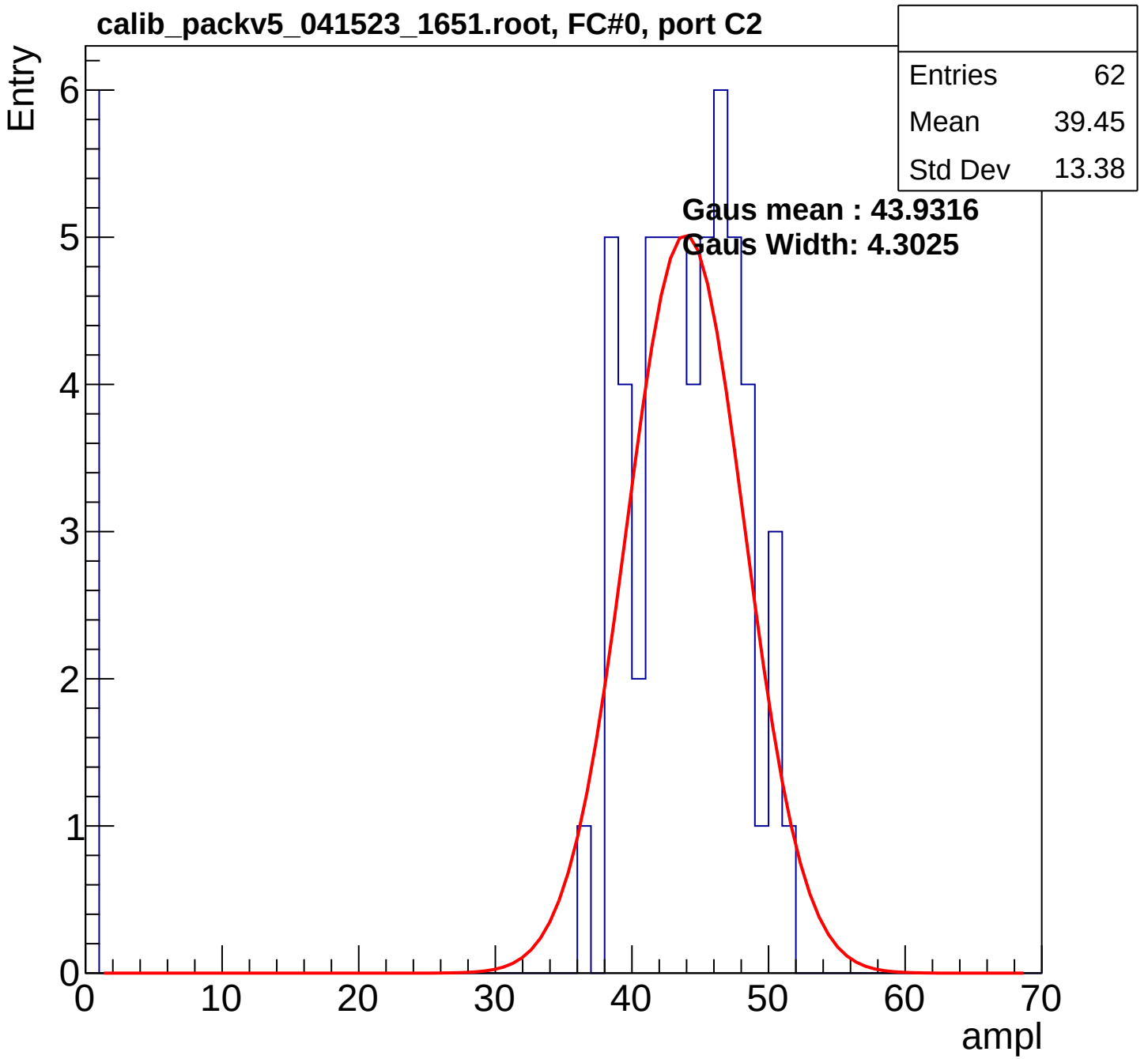

B1L103S, U17-ch20, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 58.5
Std Dev 9.457
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

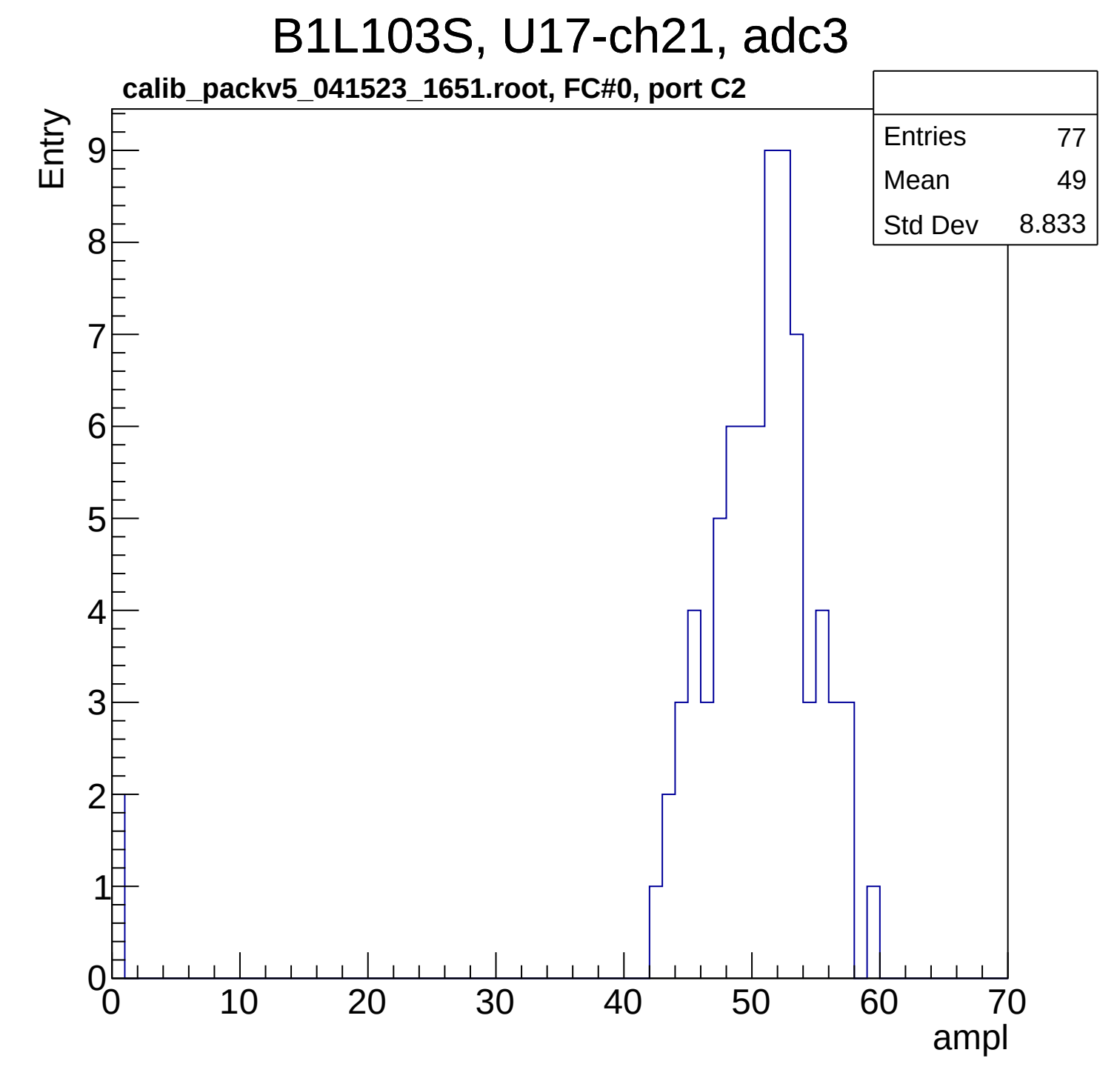

B1L103S, U17-ch20, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.17
Std Dev 2.115
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

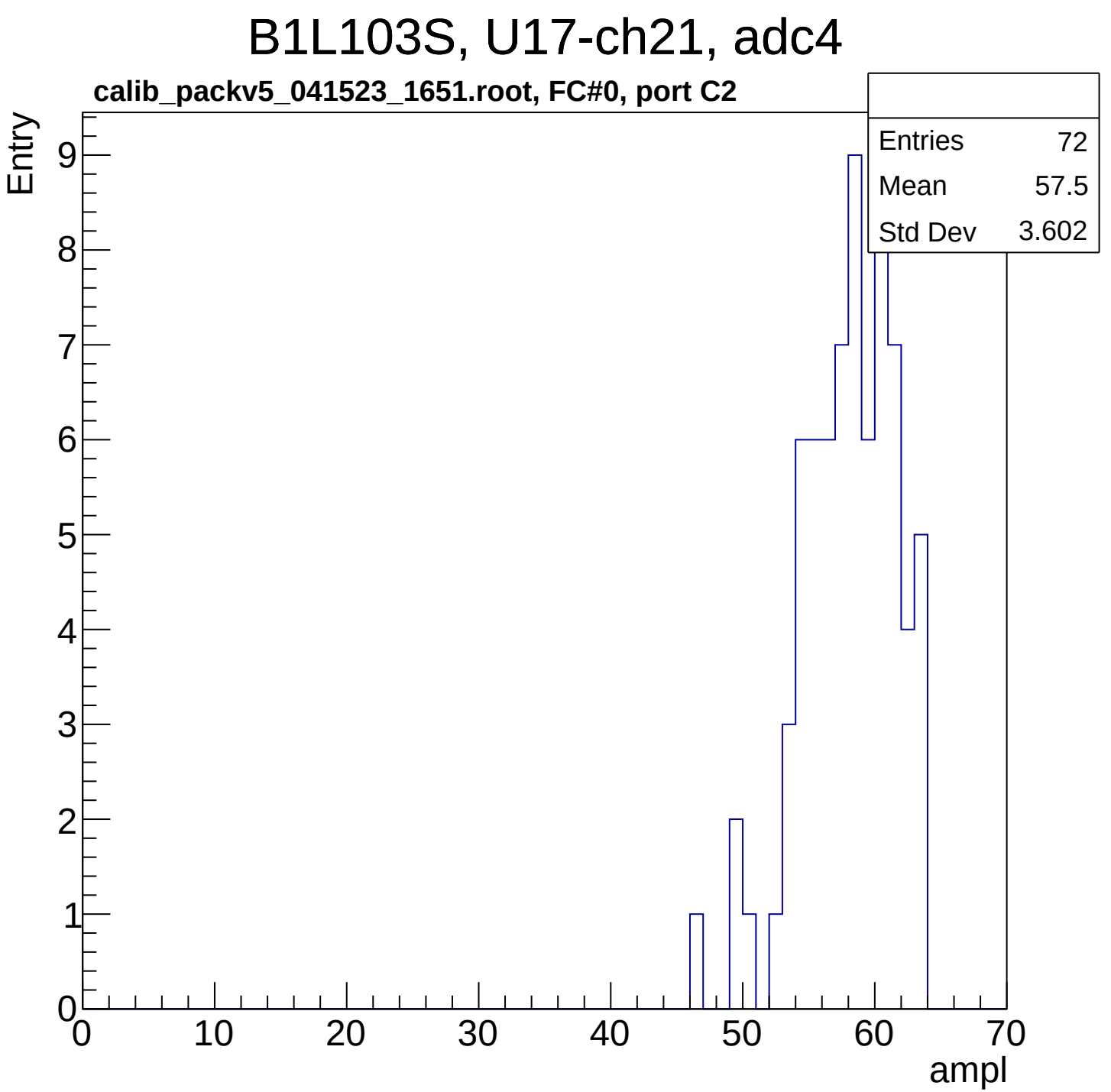

B1L103S, U17-ch20, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0.8947
Std Dev 3.796
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

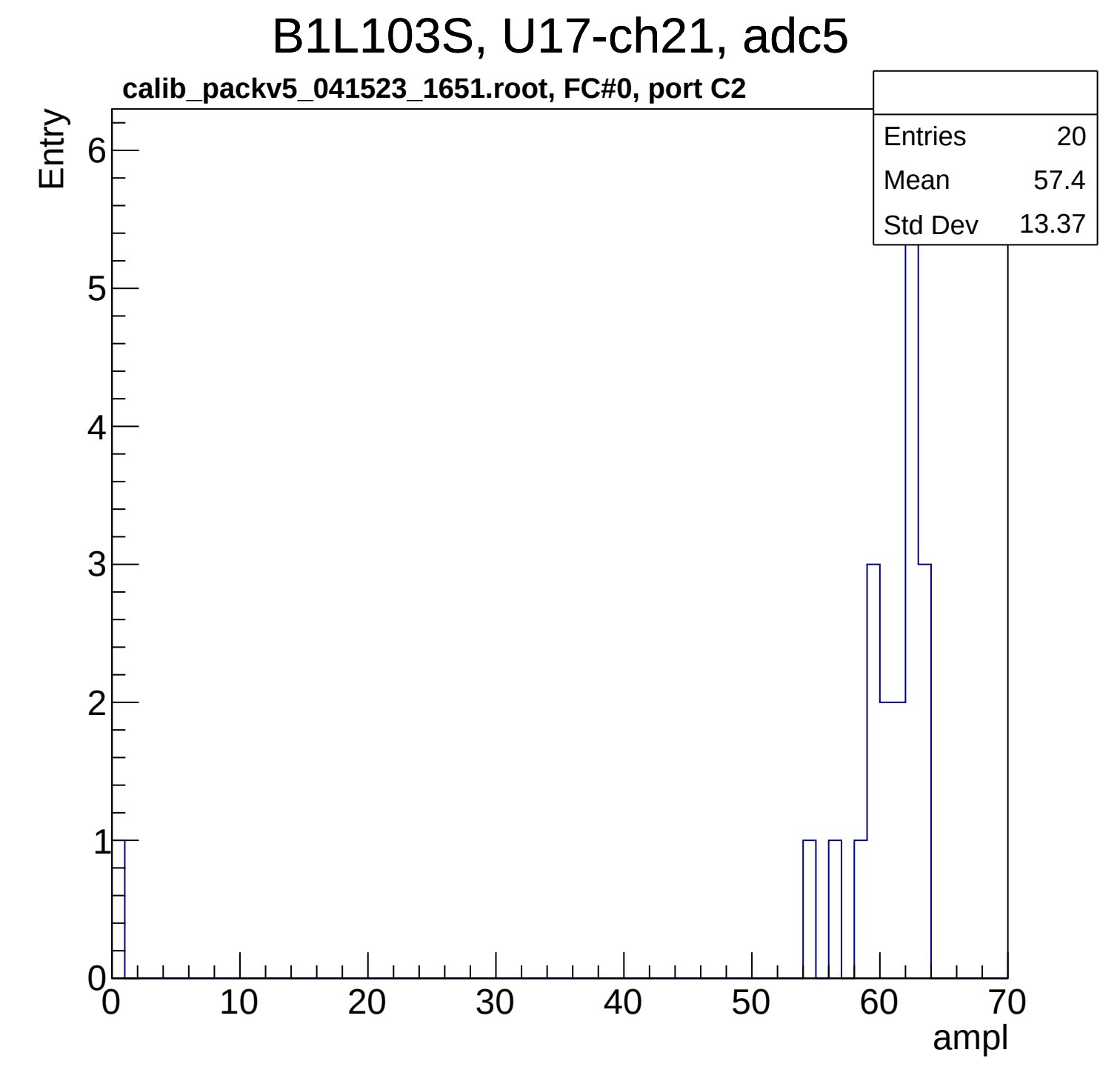

B1L103S, U17-ch21, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 24.6
Std Dev 13.05
Gaus mean : 31.5671
Gaus Width: 3.7188
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

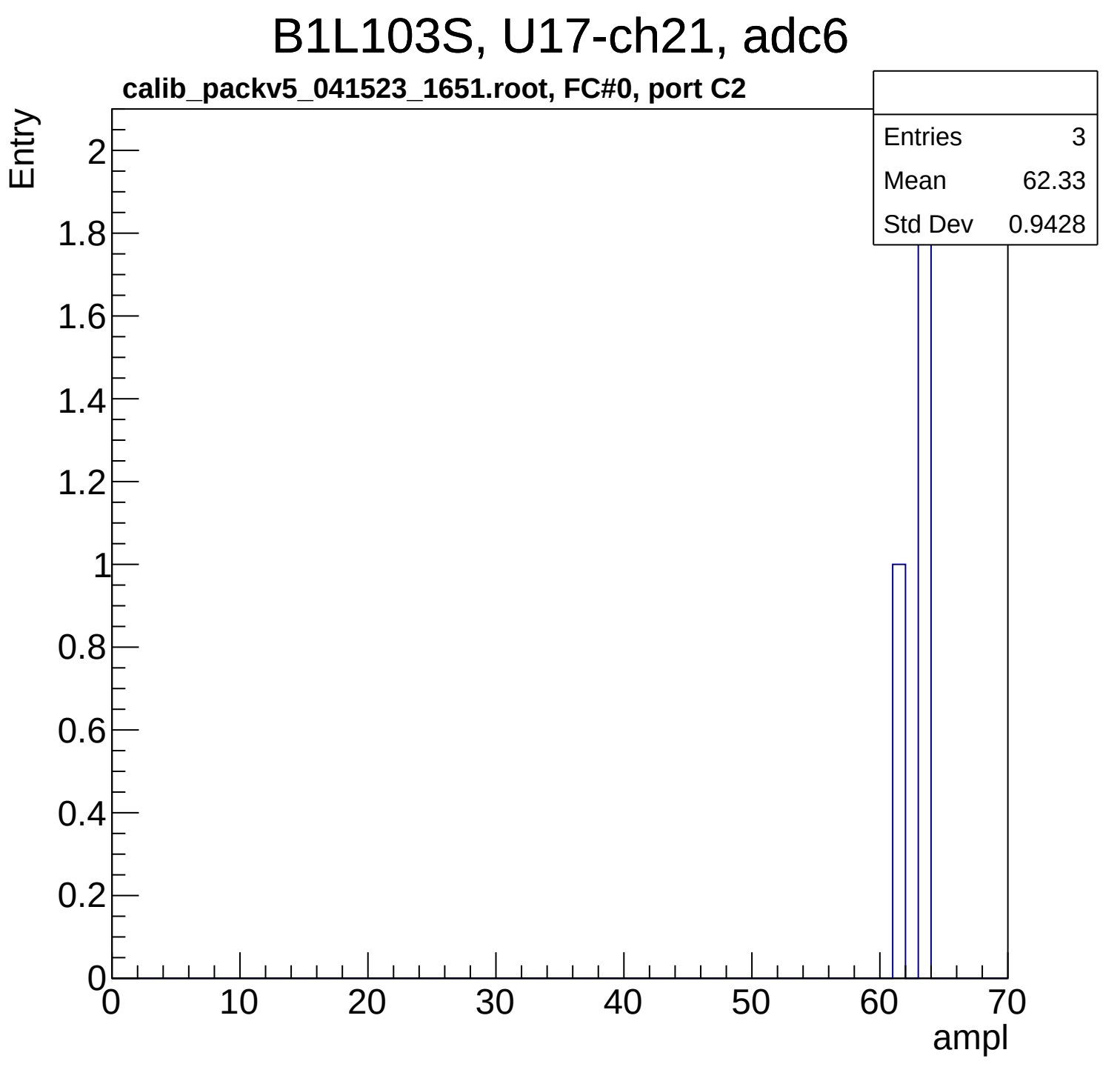

B1L103S, U17-ch21, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 32.13
Std Dev 14.32
Gaus mean : 38.5381
Gaus Width: 4.3480
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

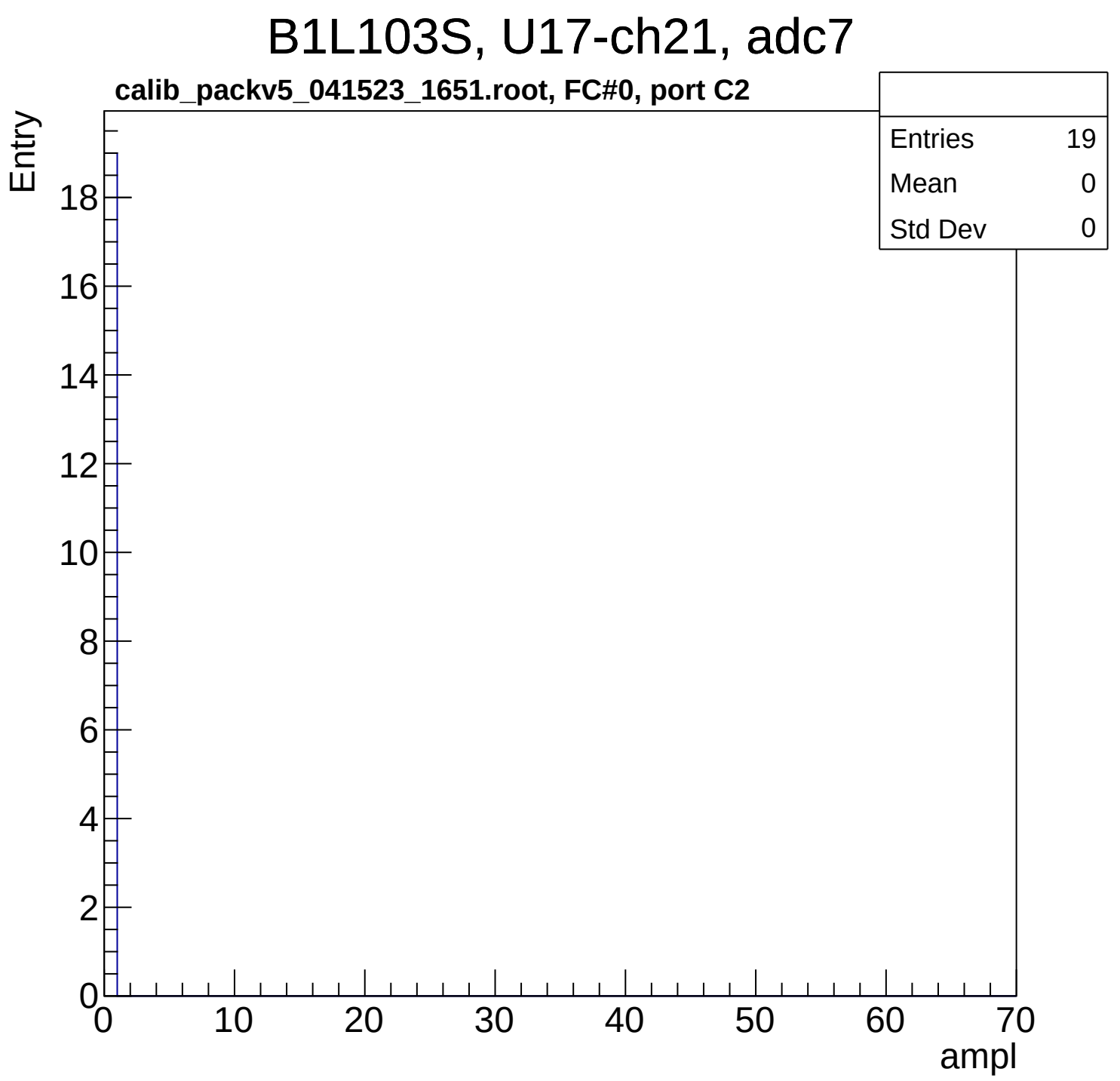

B1L103S, U17-ch21, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 39.45
Std Dev 13.38
Gaus mean : 43.9316
Gaus Width: 4.3025
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

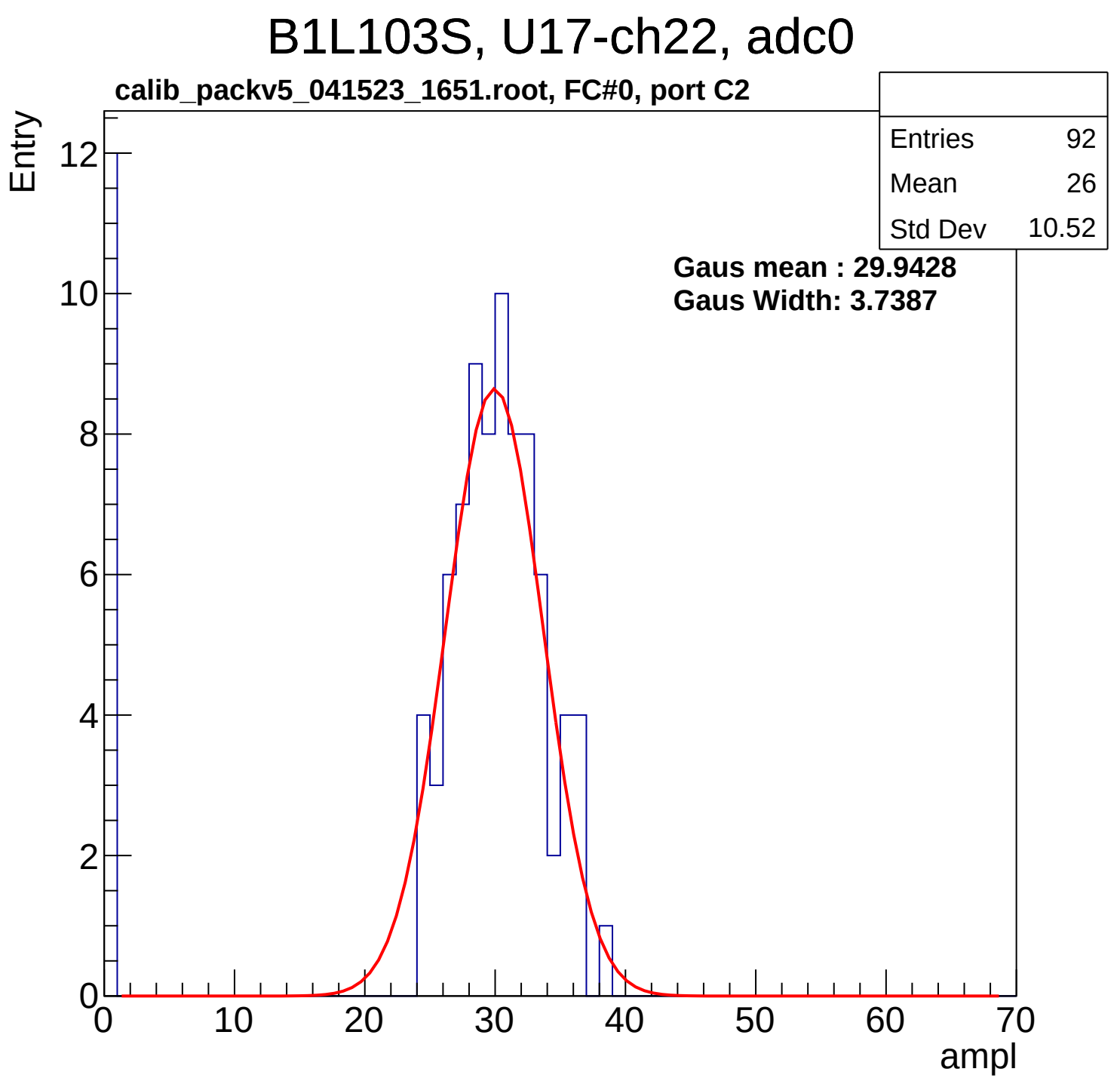

B1L103S, U17-ch21, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 49
Std Dev 8.833
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

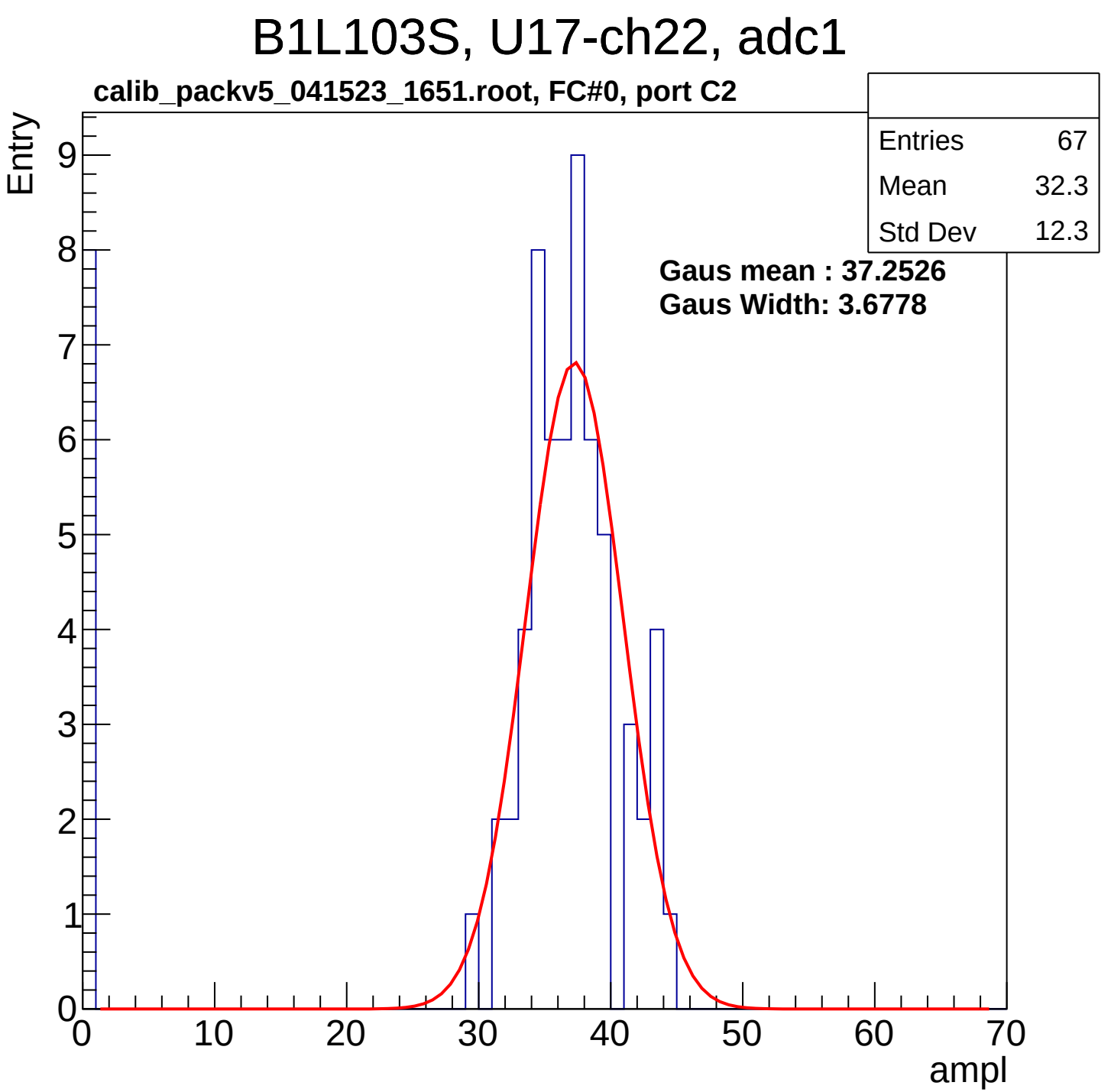

B1L103S, U17-ch21, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 57.5
Std Dev 3.602
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

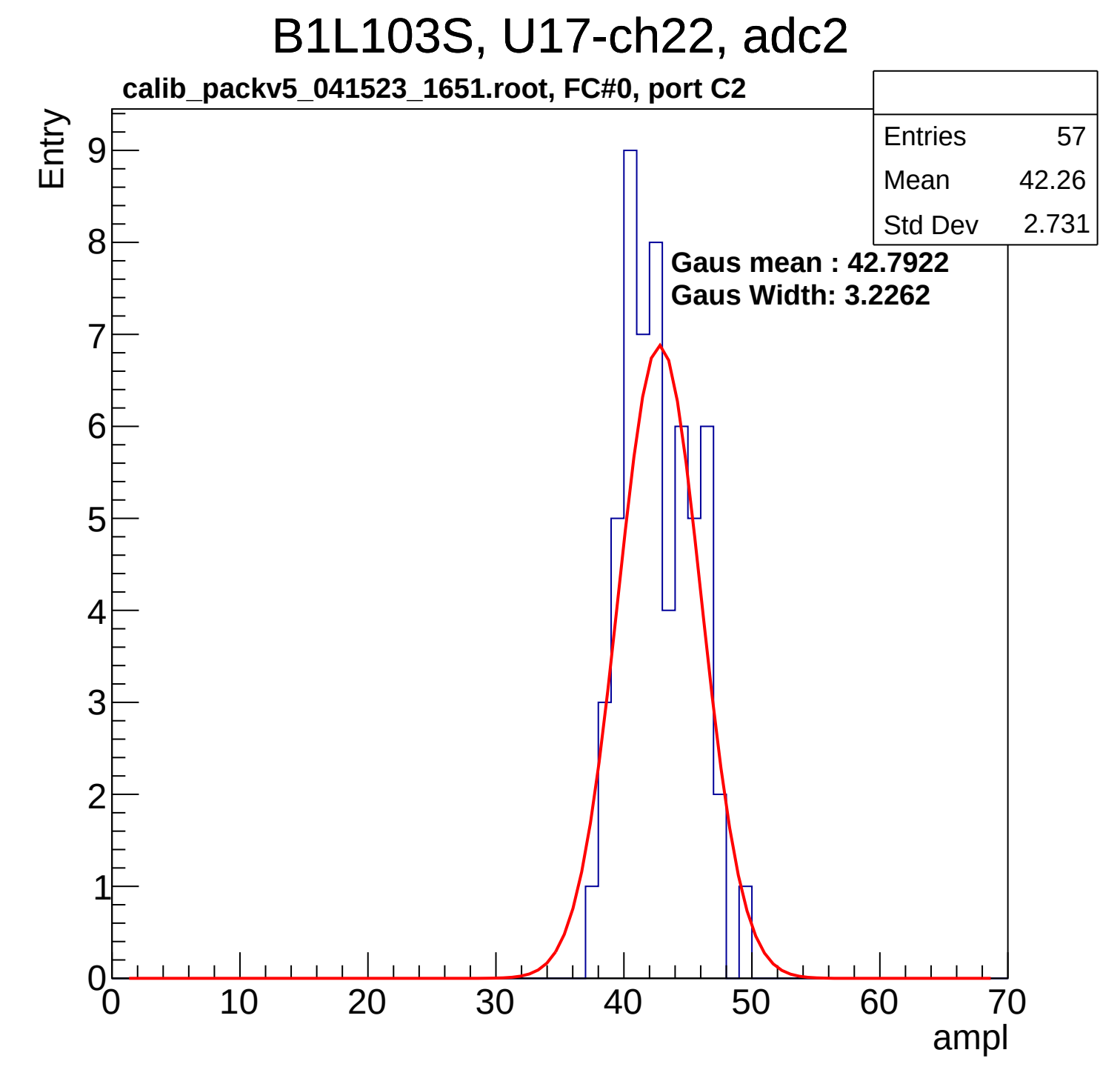

B1L103S, U17-ch21, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 57.4
Std Dev 13.37
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

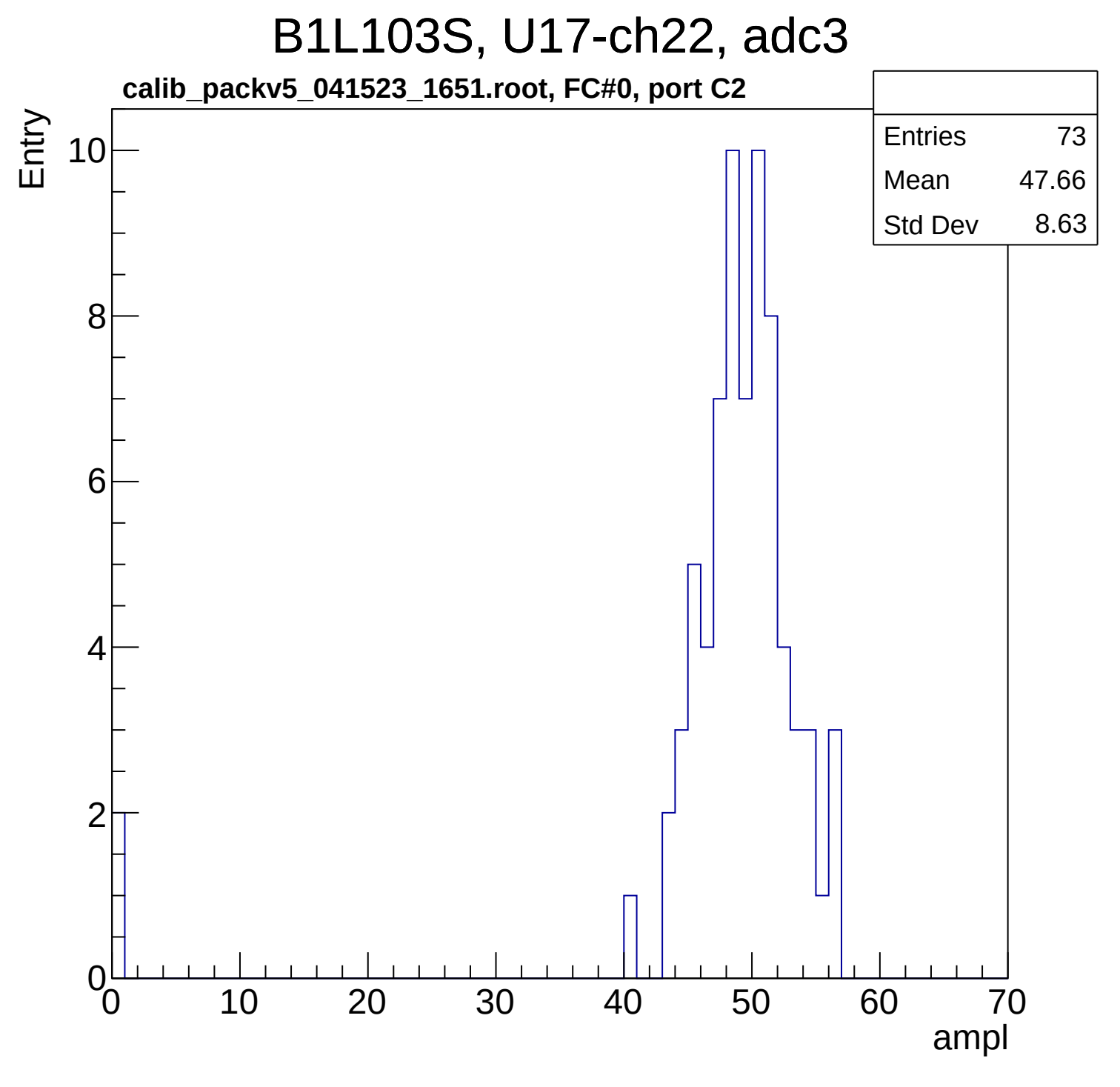

B1L103S, U17-ch21, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.33
Std Dev 0.9428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

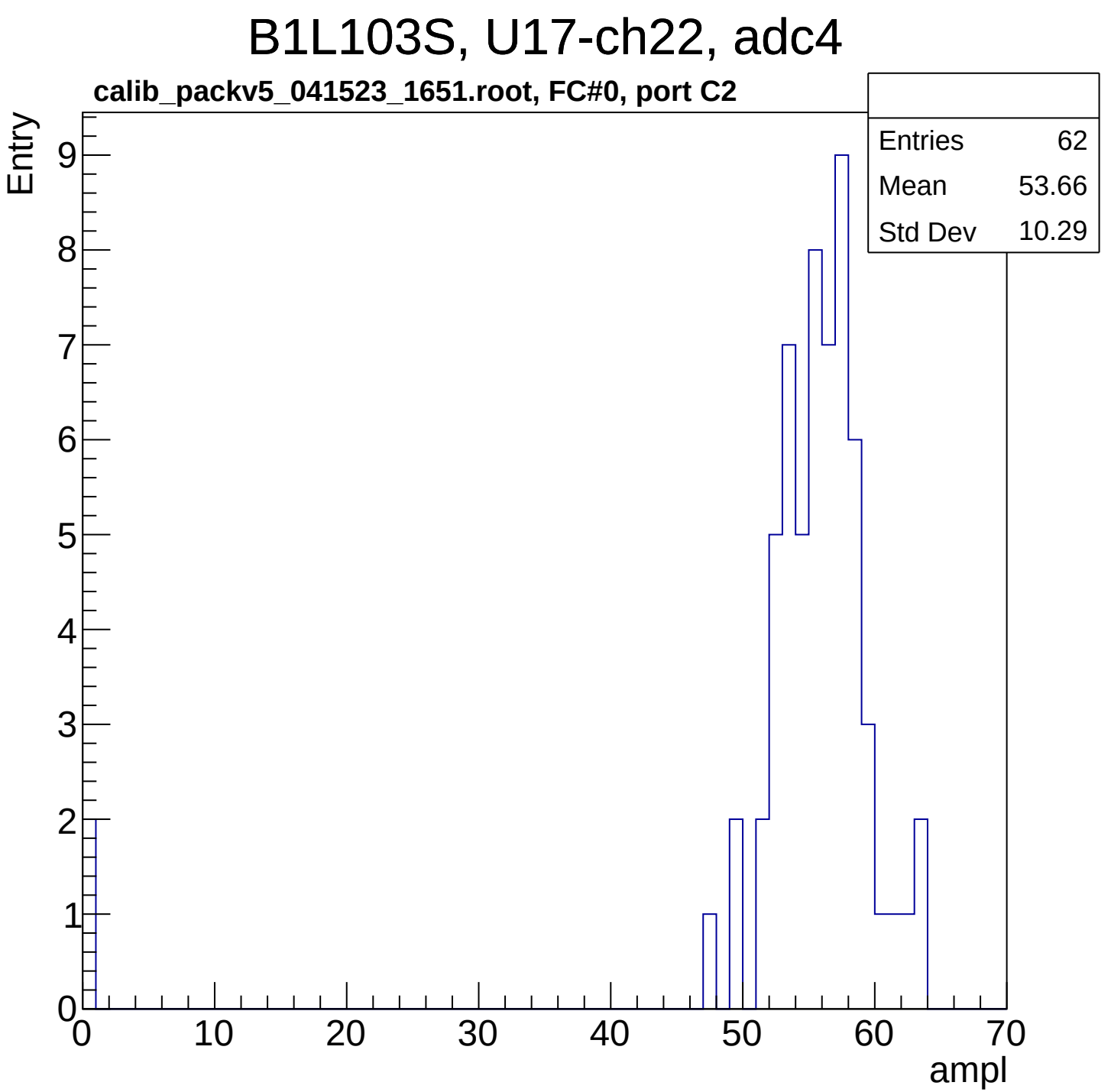

B1L103S, U17-ch21, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

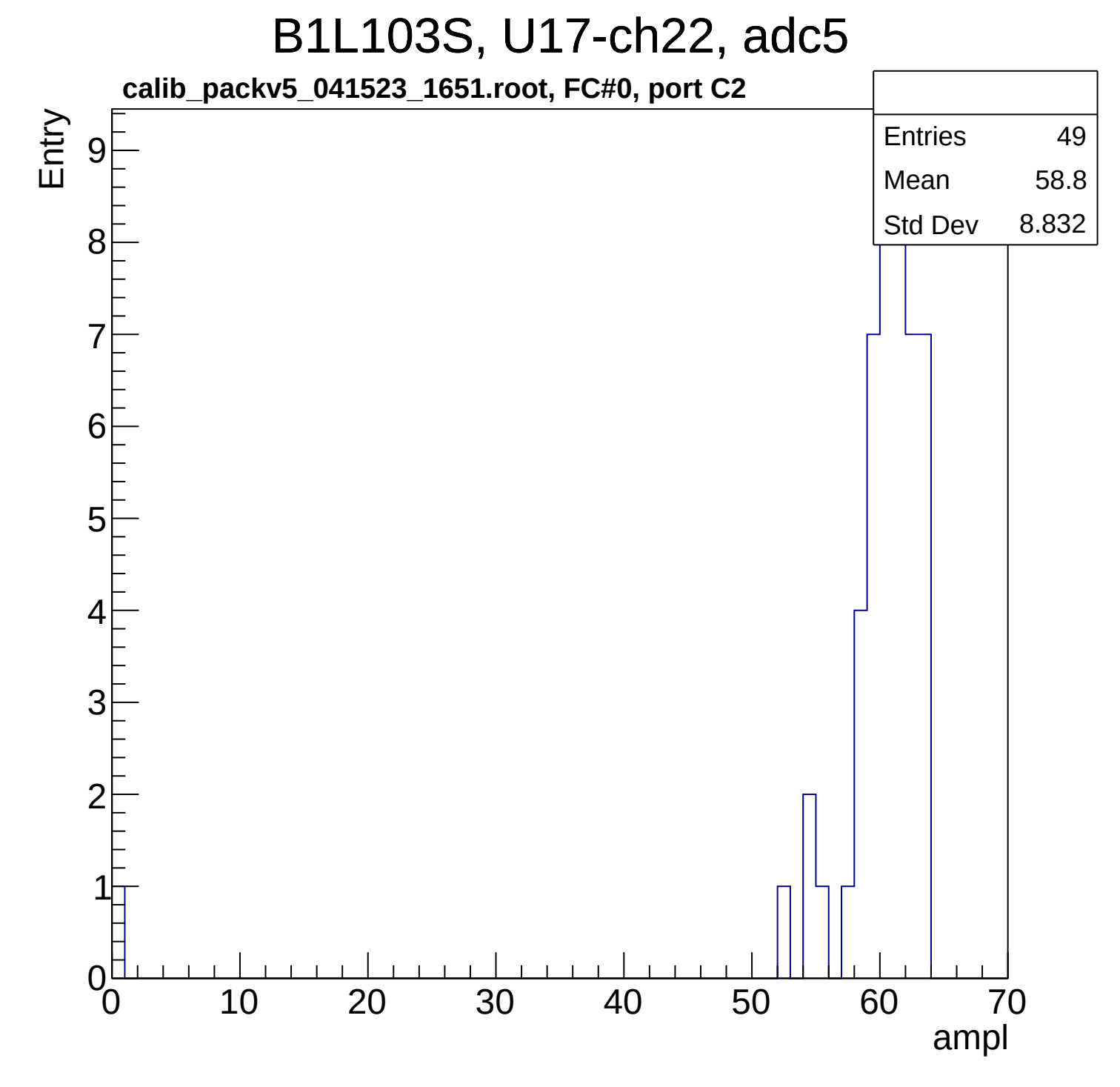

B1L103S, U17-ch22, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 26
Std Dev 10.52
Gaus mean : 29.9428
Gaus Width: 3.7387
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

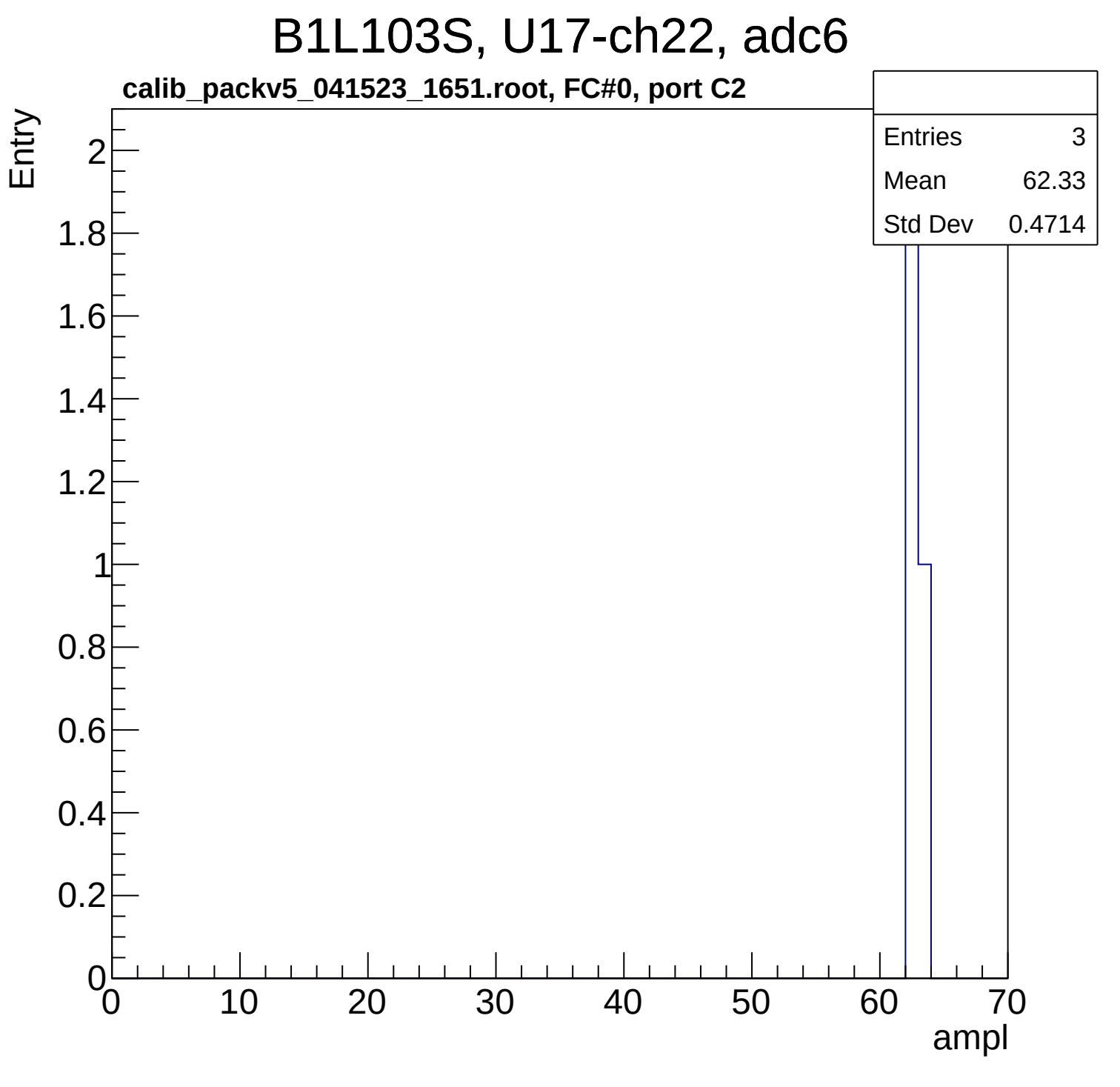

B1L103S, U17-ch22, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 32.3
Std Dev 12.3
Gaus mean : 37.2526
Gaus Width: 3.6778
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

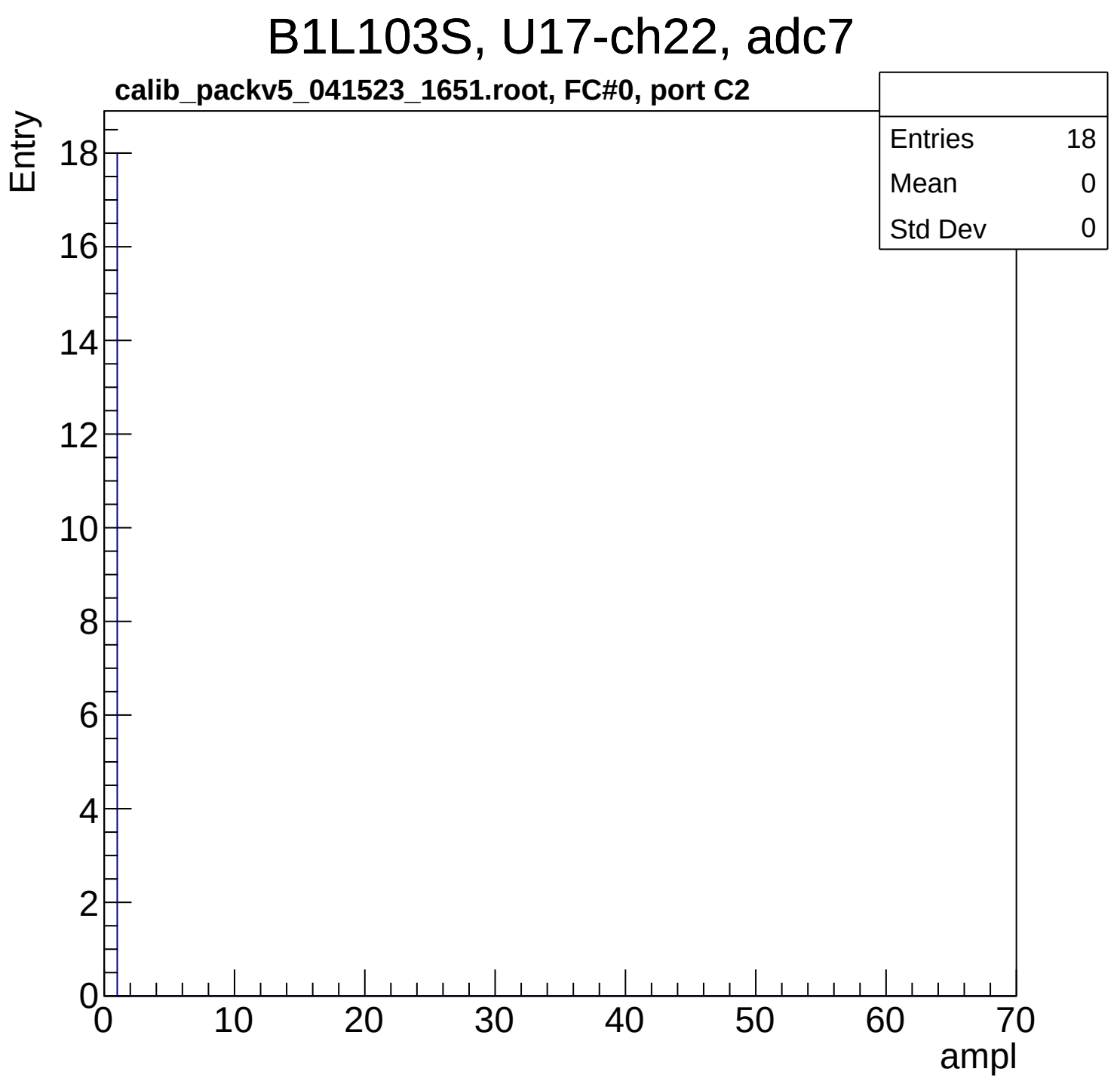

B1L103S, U17-ch22, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 42.26
Std Dev 2.731
Gaus mean : 42.7922
Gaus Width: 3.2262
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

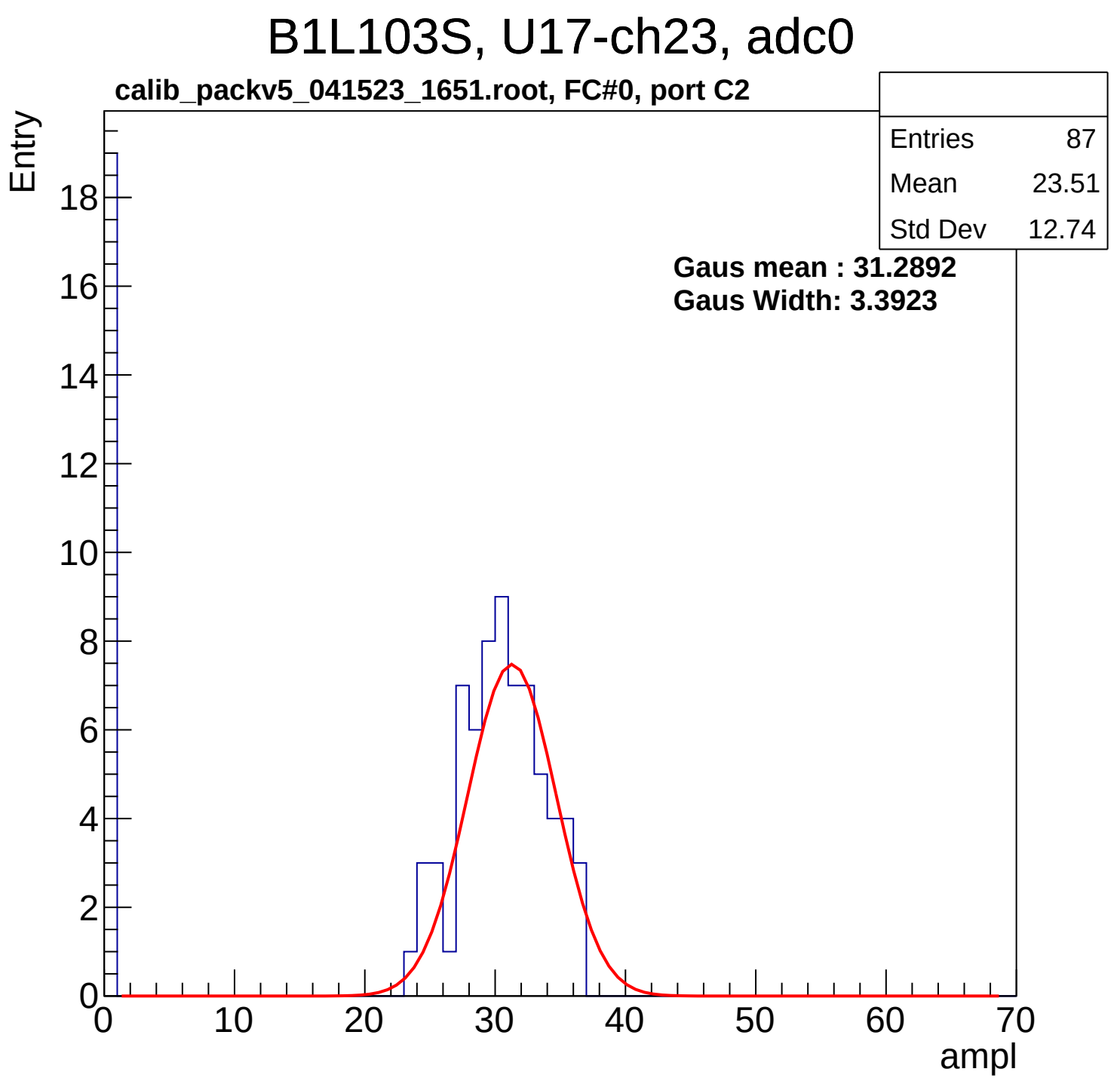

B1L103S, U17-ch22, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 47.66
Std Dev 8.63
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

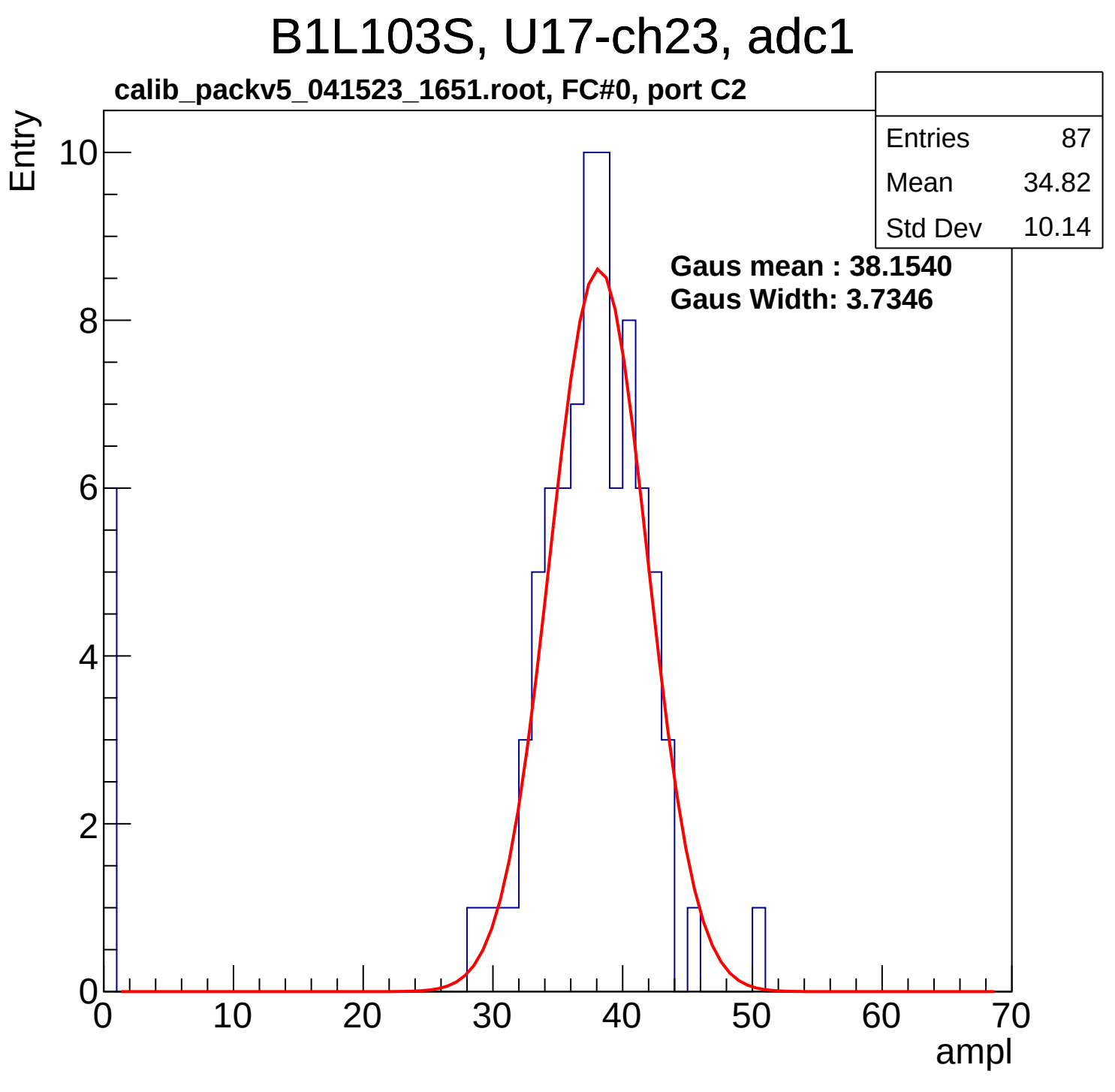

B1L103S, U17-ch22, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 53.66
Std Dev 10.29
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

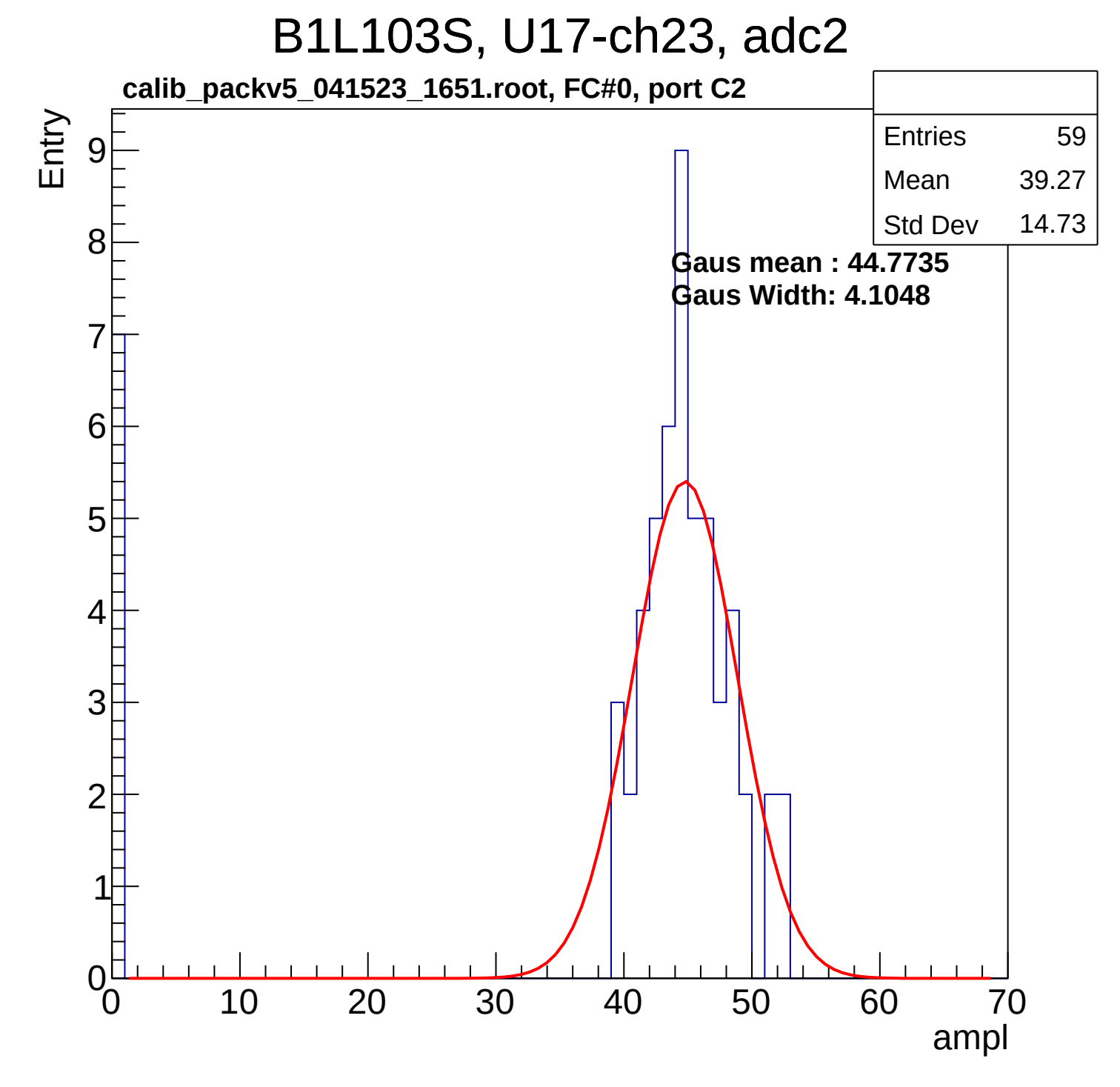

B1L103S, U17-ch22, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.8
Std Dev 8.832
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

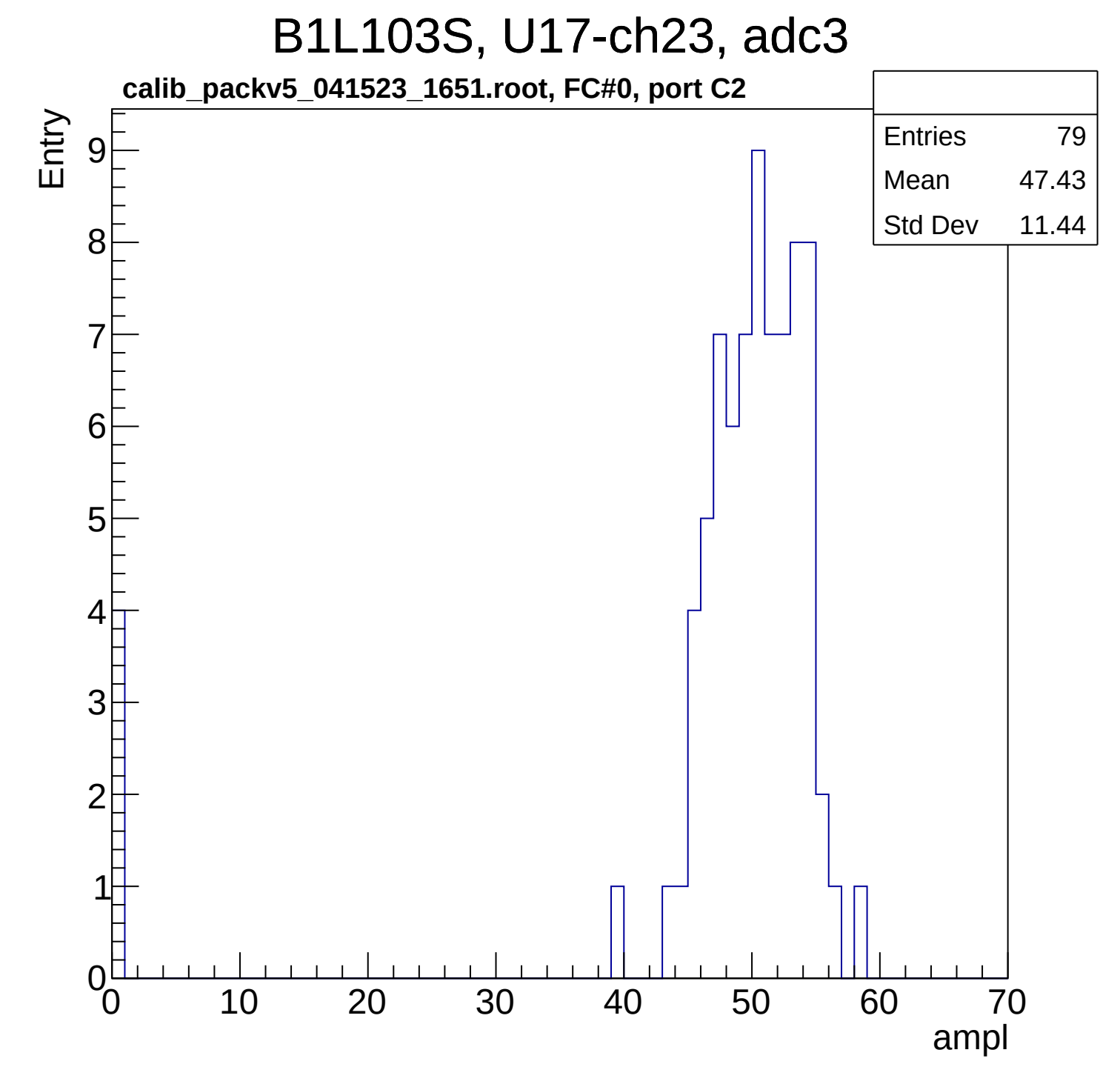

B1L103S, U17-ch22, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

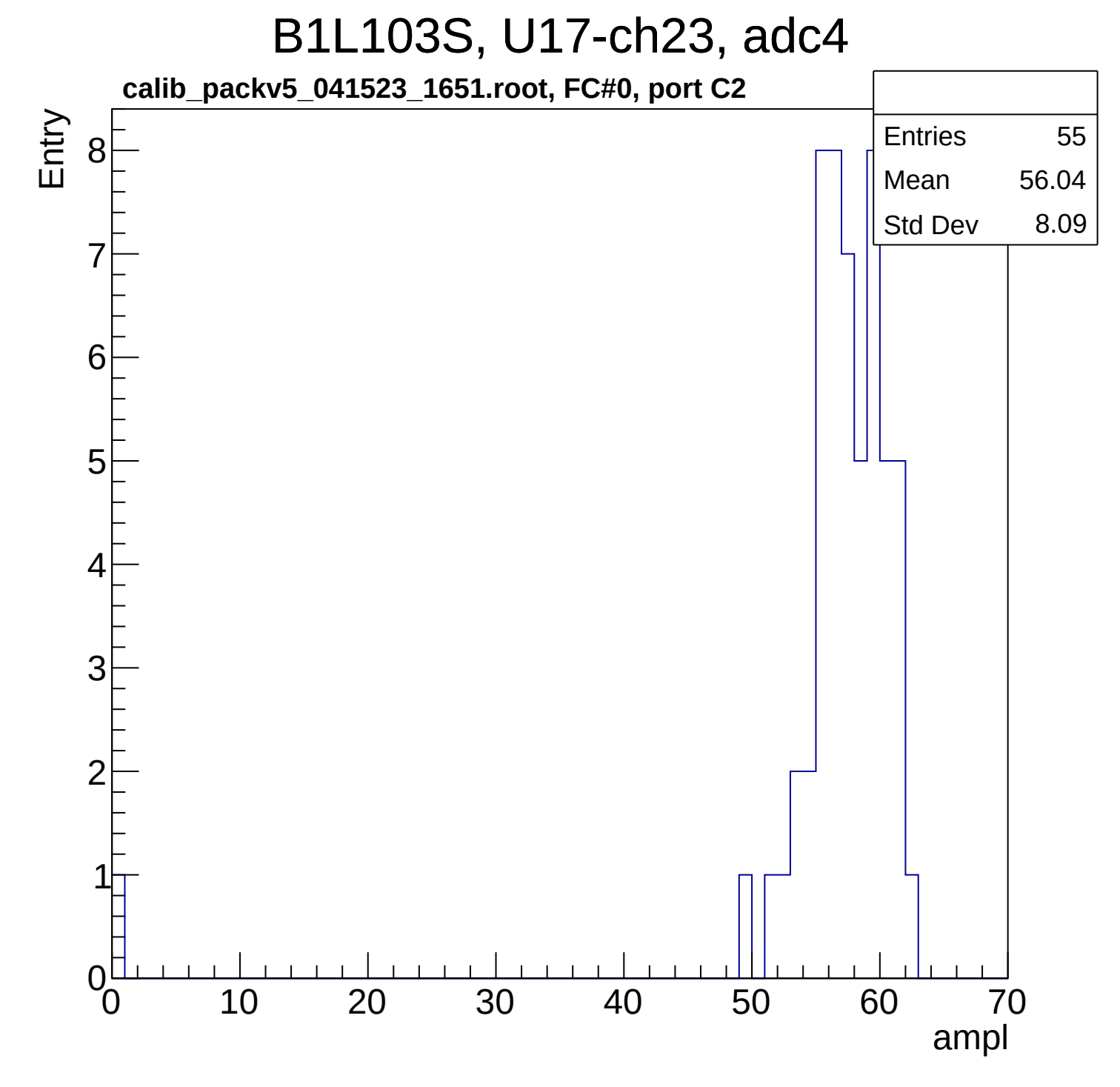

B1L103S, U17-ch22, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

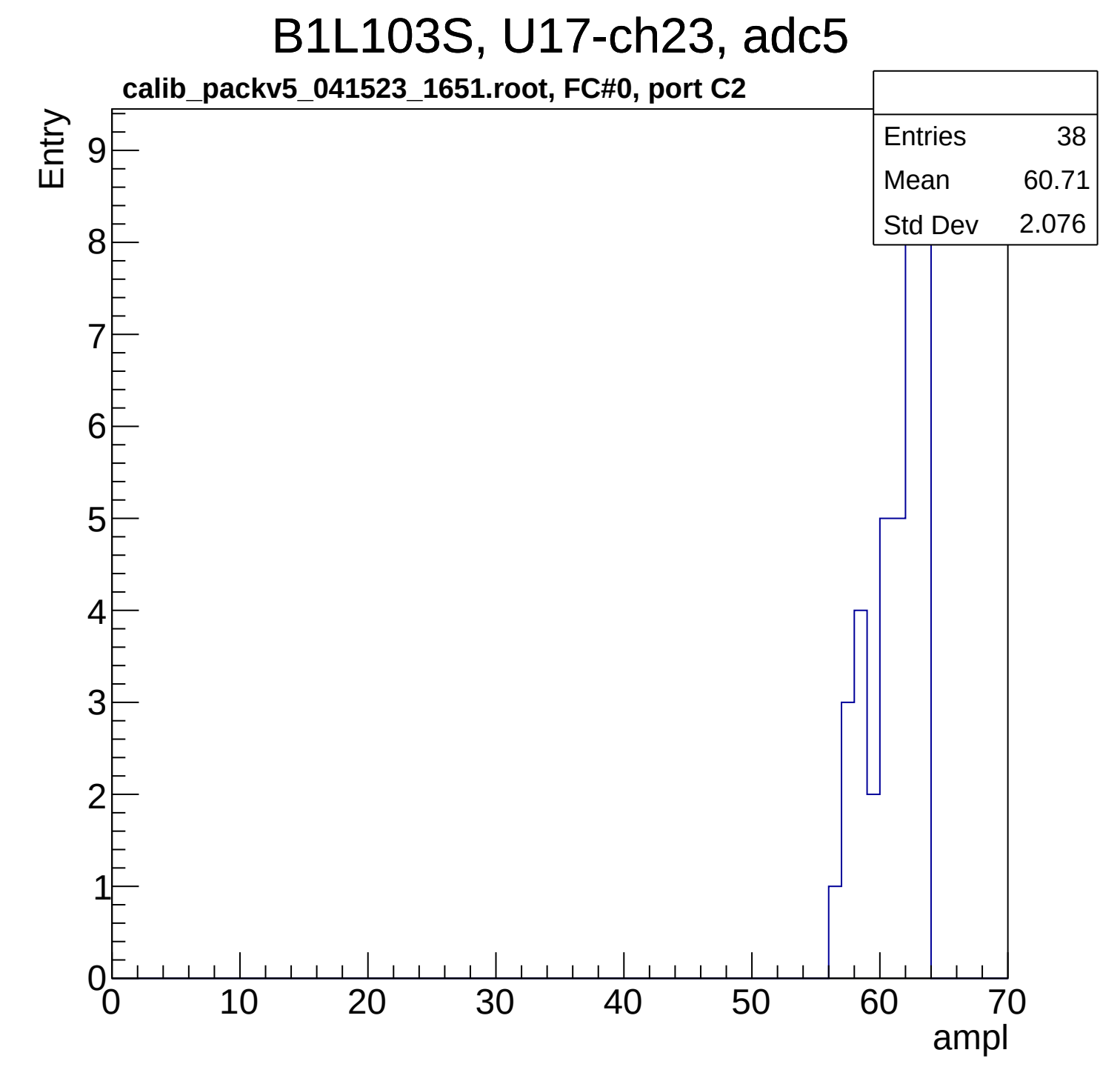

B1L103S, U17-ch23, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 23.51
Std Dev 12.74
Gaus mean : 31.2892
Gaus Width: 3.3923
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

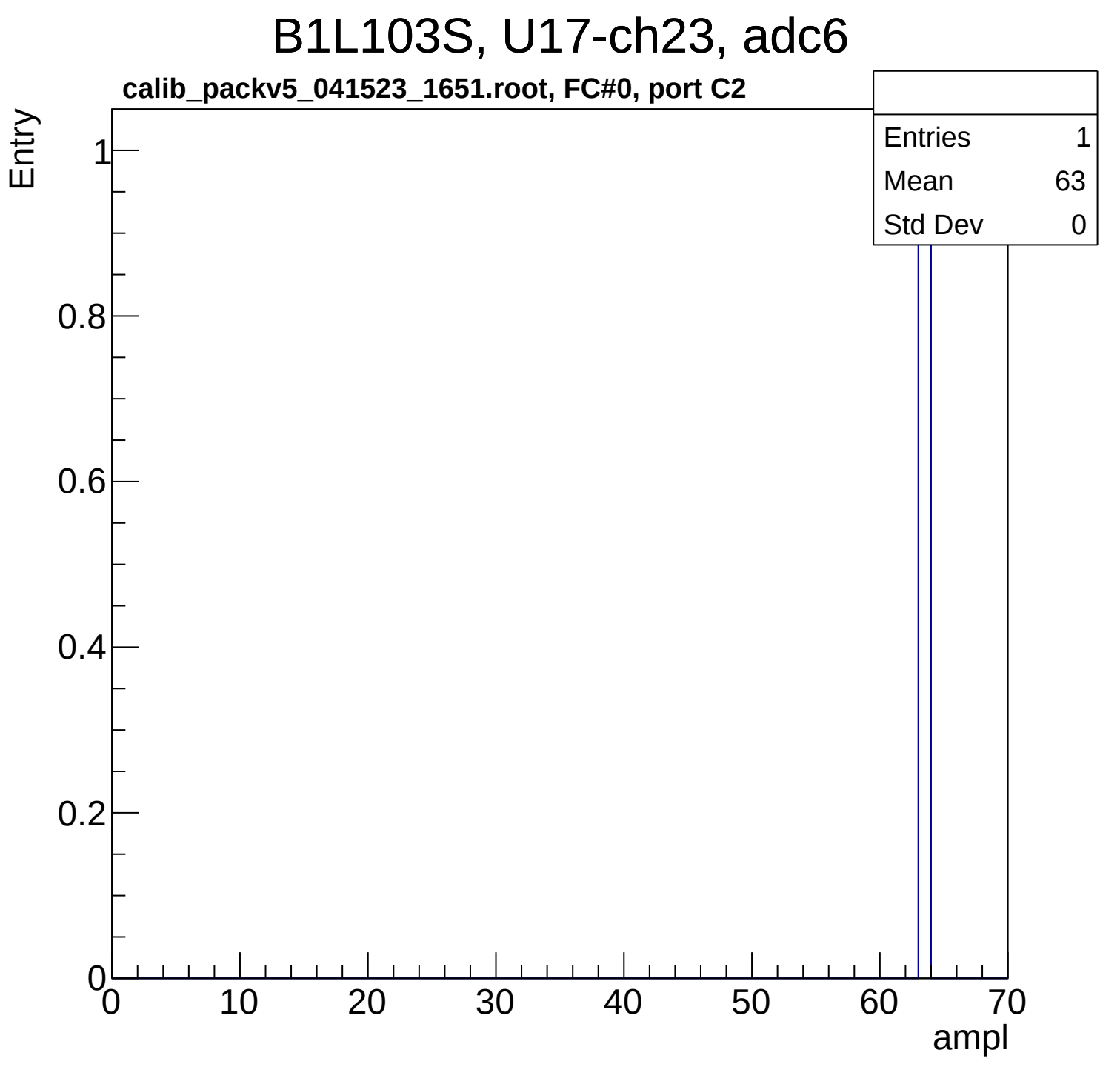

B1L103S, U17-ch23, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 34.82
Std Dev 10.14
Gaus mean : 38.1540
Gaus Width: 3.7346
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

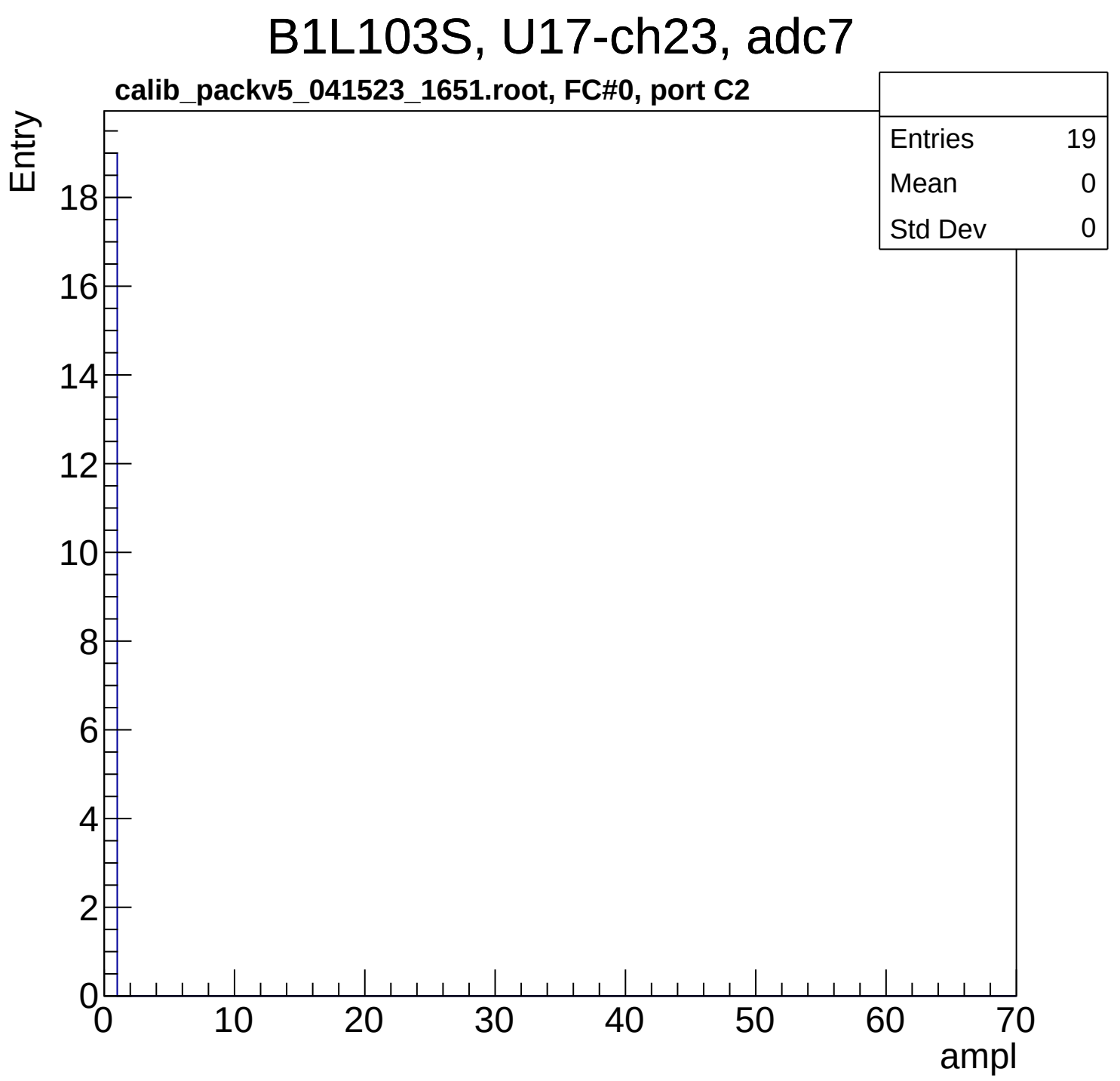

B1L103S, U17-ch23, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 39.27
Std Dev 14.73
Gaus mean : 44.7735
Gaus Width: 4.1048
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

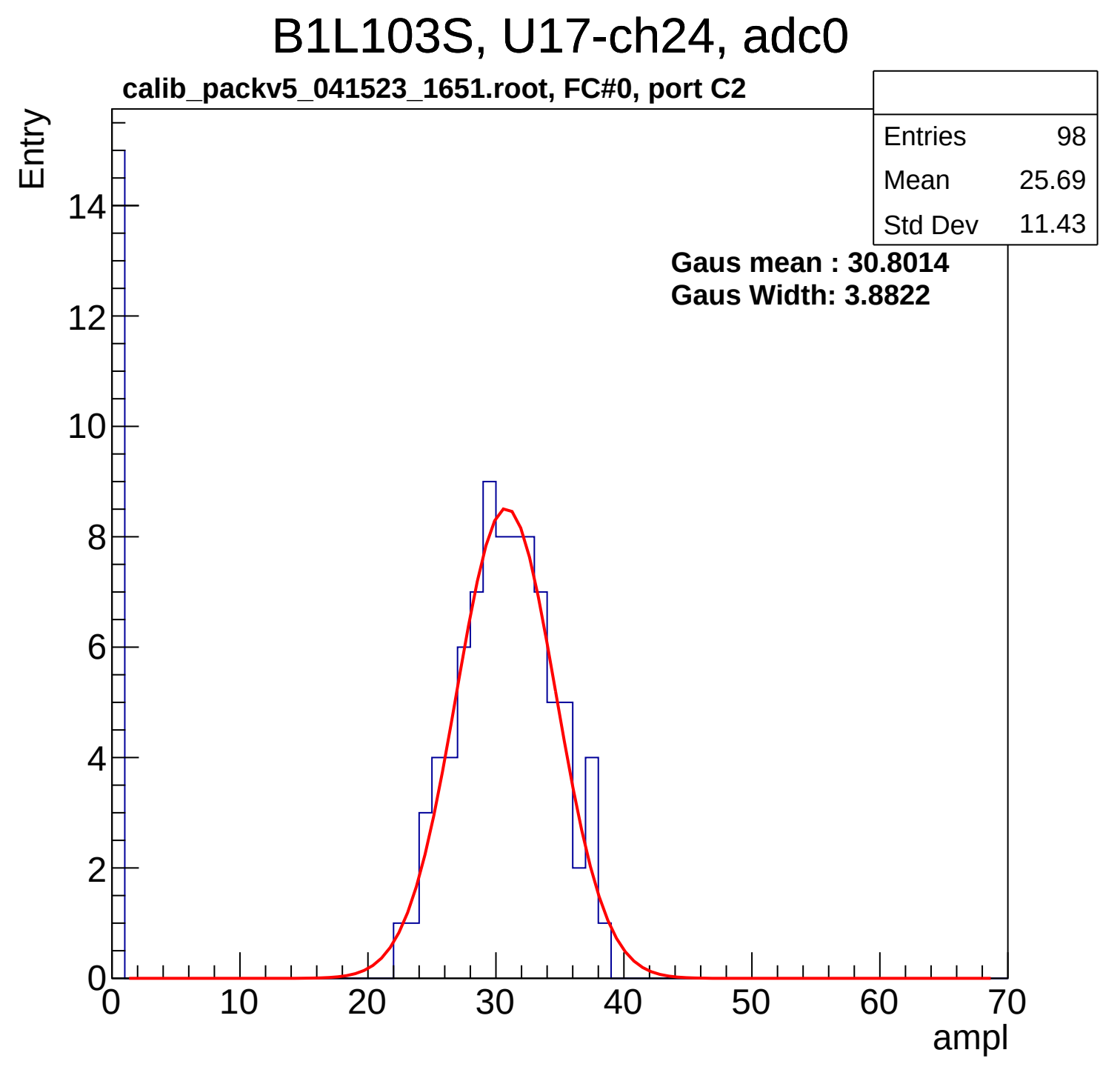

B1L103S, U17-ch23, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 47.43
Std Dev 11.44
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

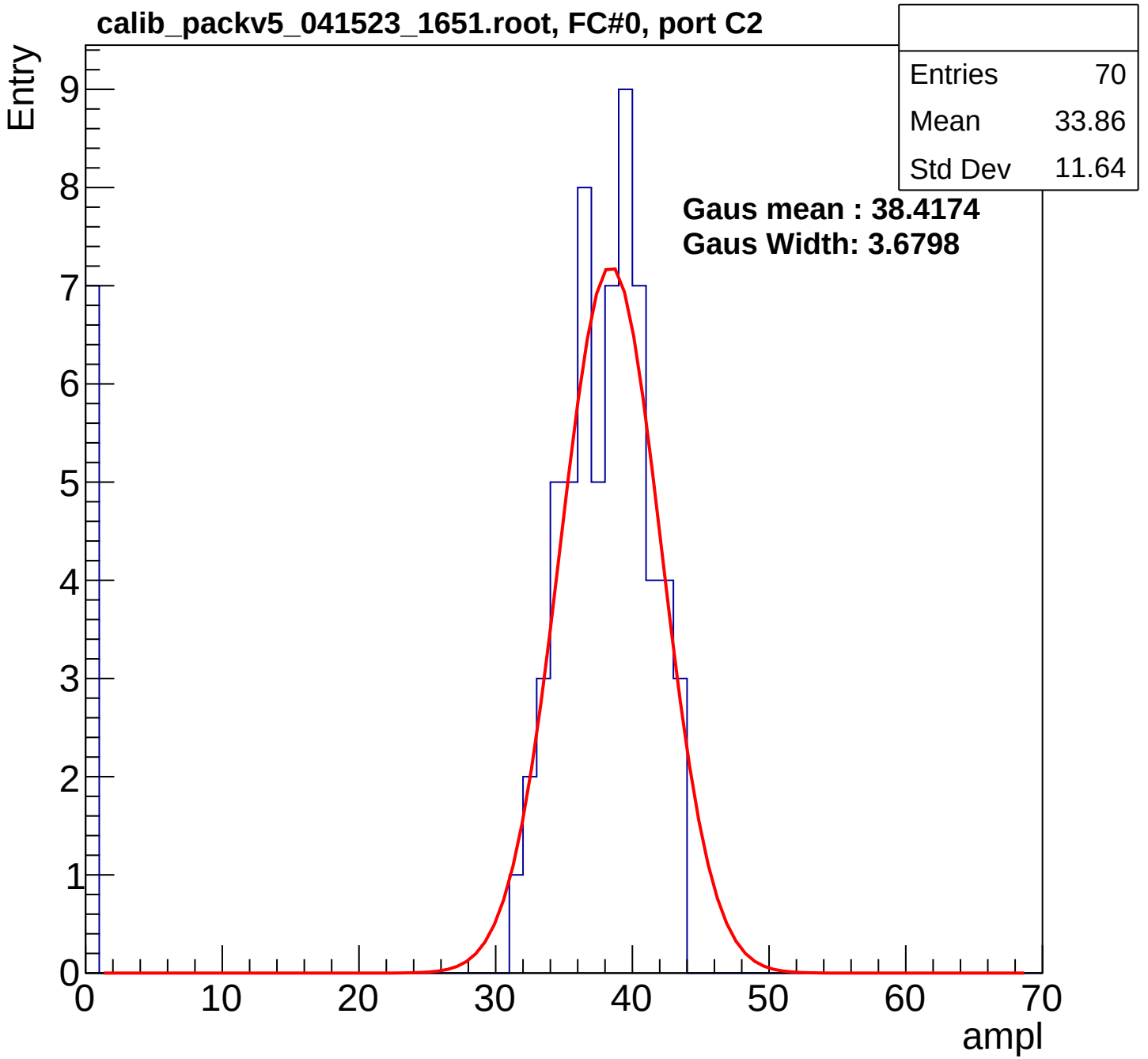

B1L103S, U17-ch23, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 56.04
Std Dev 8.09
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

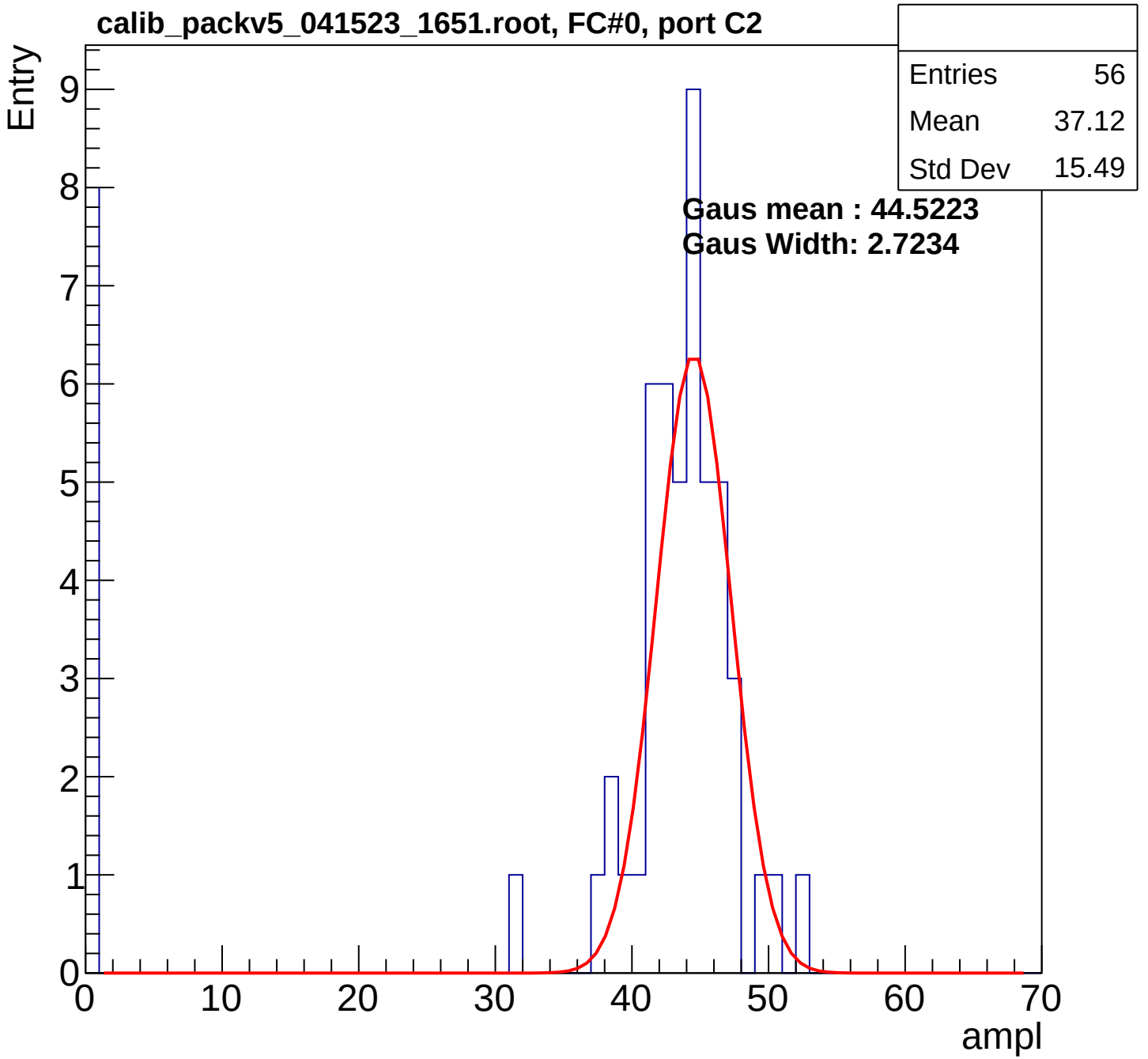

B1L103S, U17-ch23, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 60.71
Std Dev 2.076
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

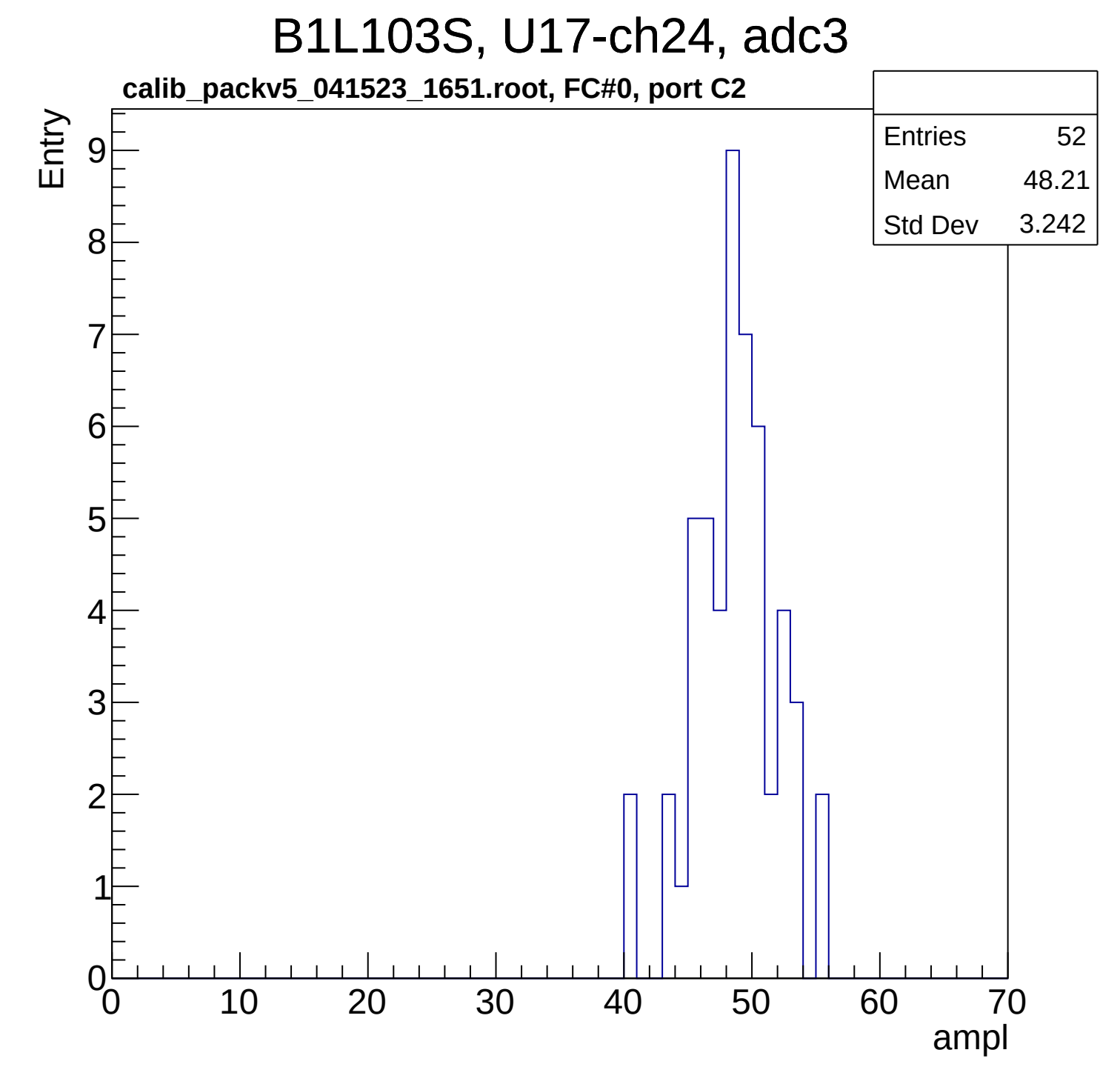

B1L103S, U17-ch23, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

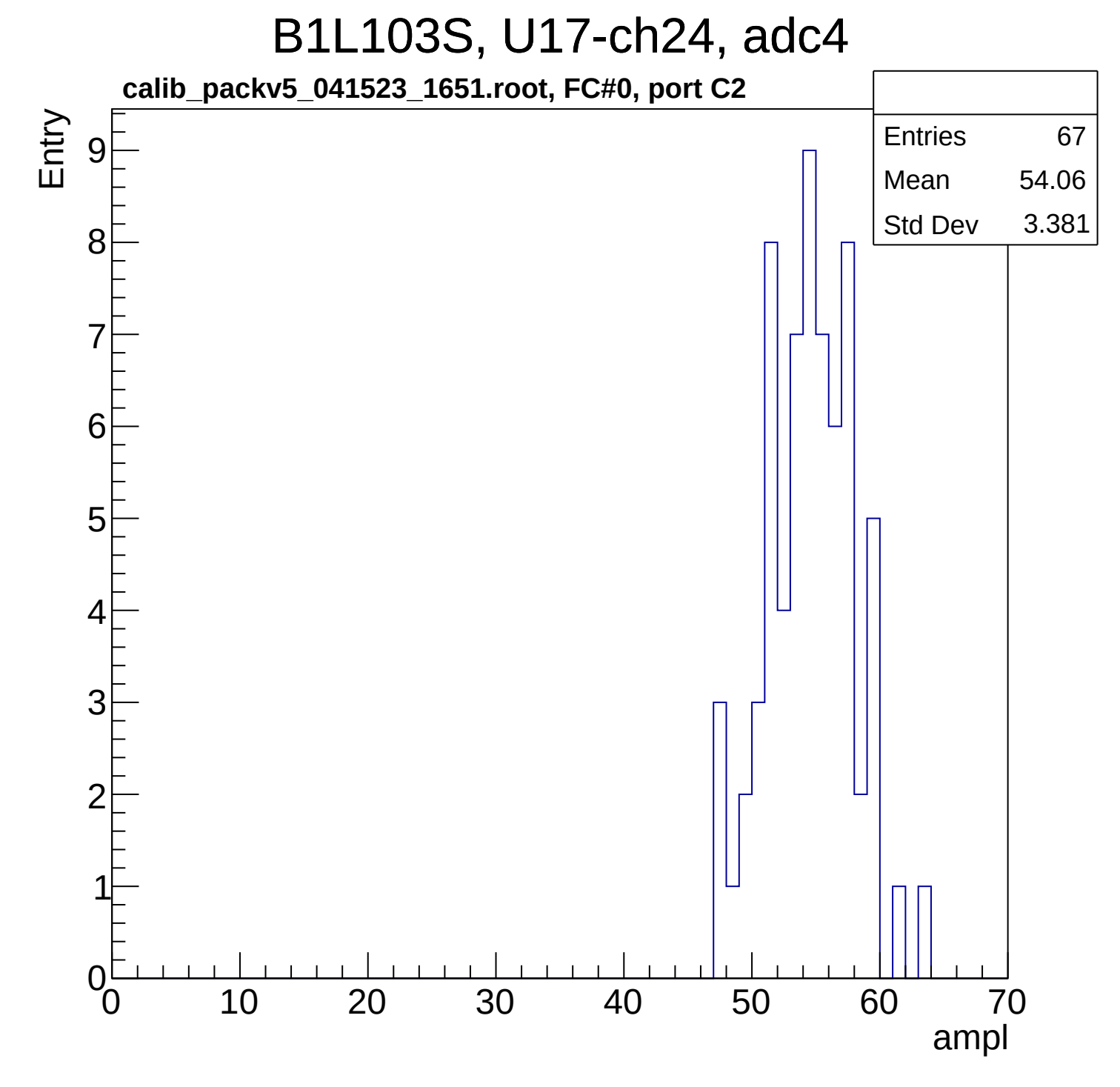

B1L103S, U17-ch23, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

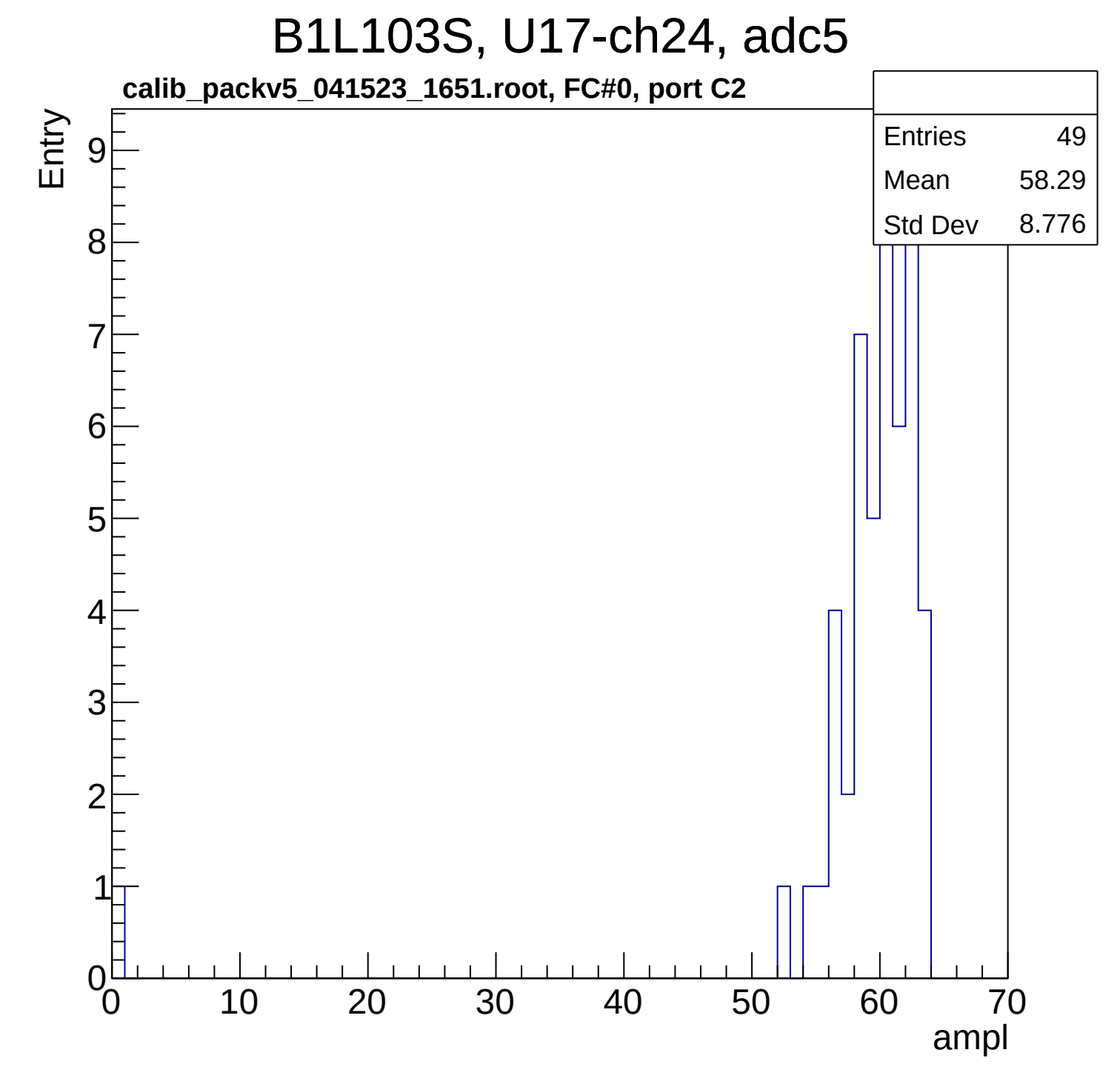

B1L103S, U17-ch24, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 25.69
Std Dev 11.43
Gaus mean : 30.8014
Gaus Width: 3.8822
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

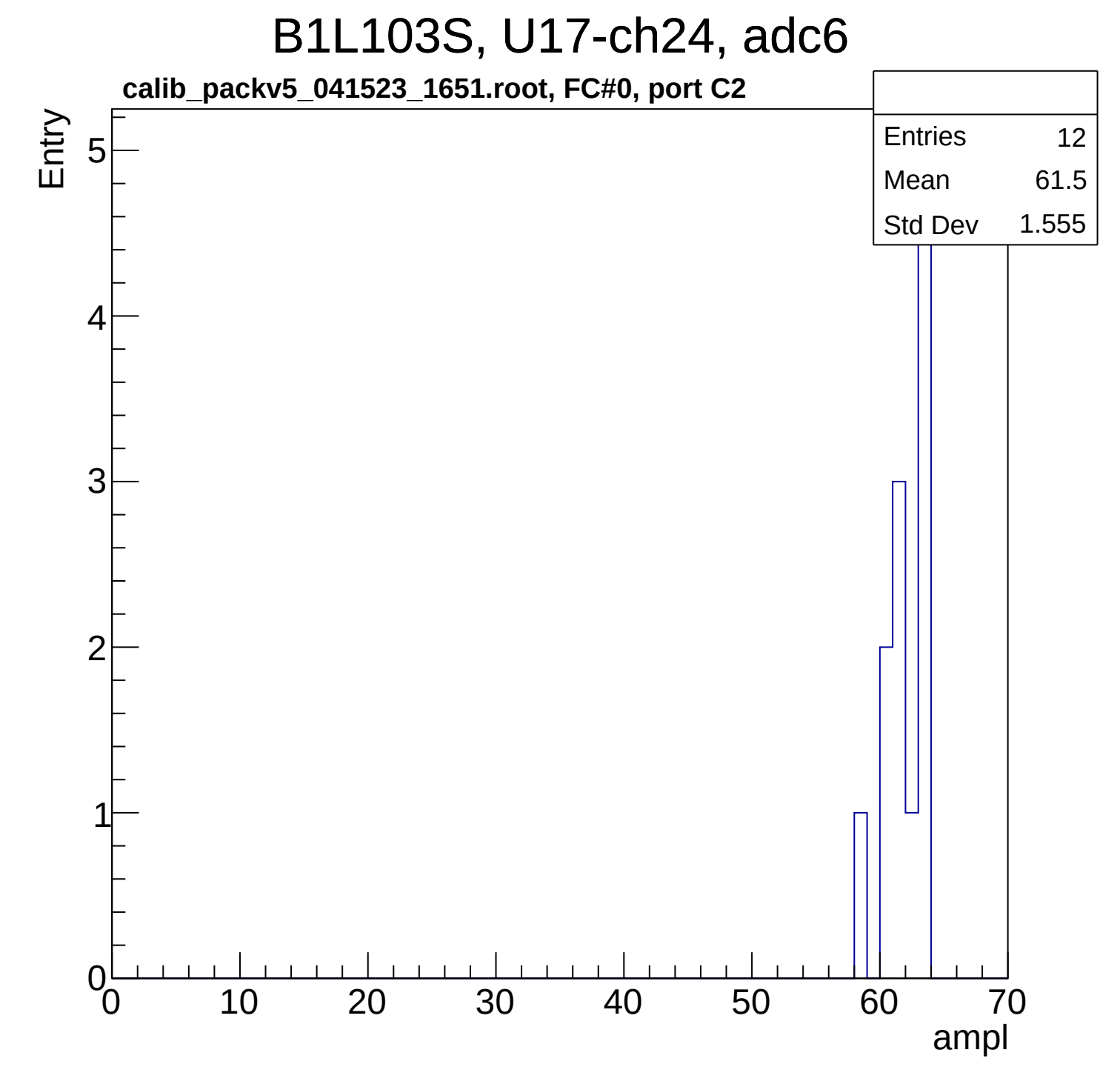

B1L103S, U17-ch24, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 33.86
Std Dev 11.64
Gaus mean : 38.4174
Gaus Width: 3.6798
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

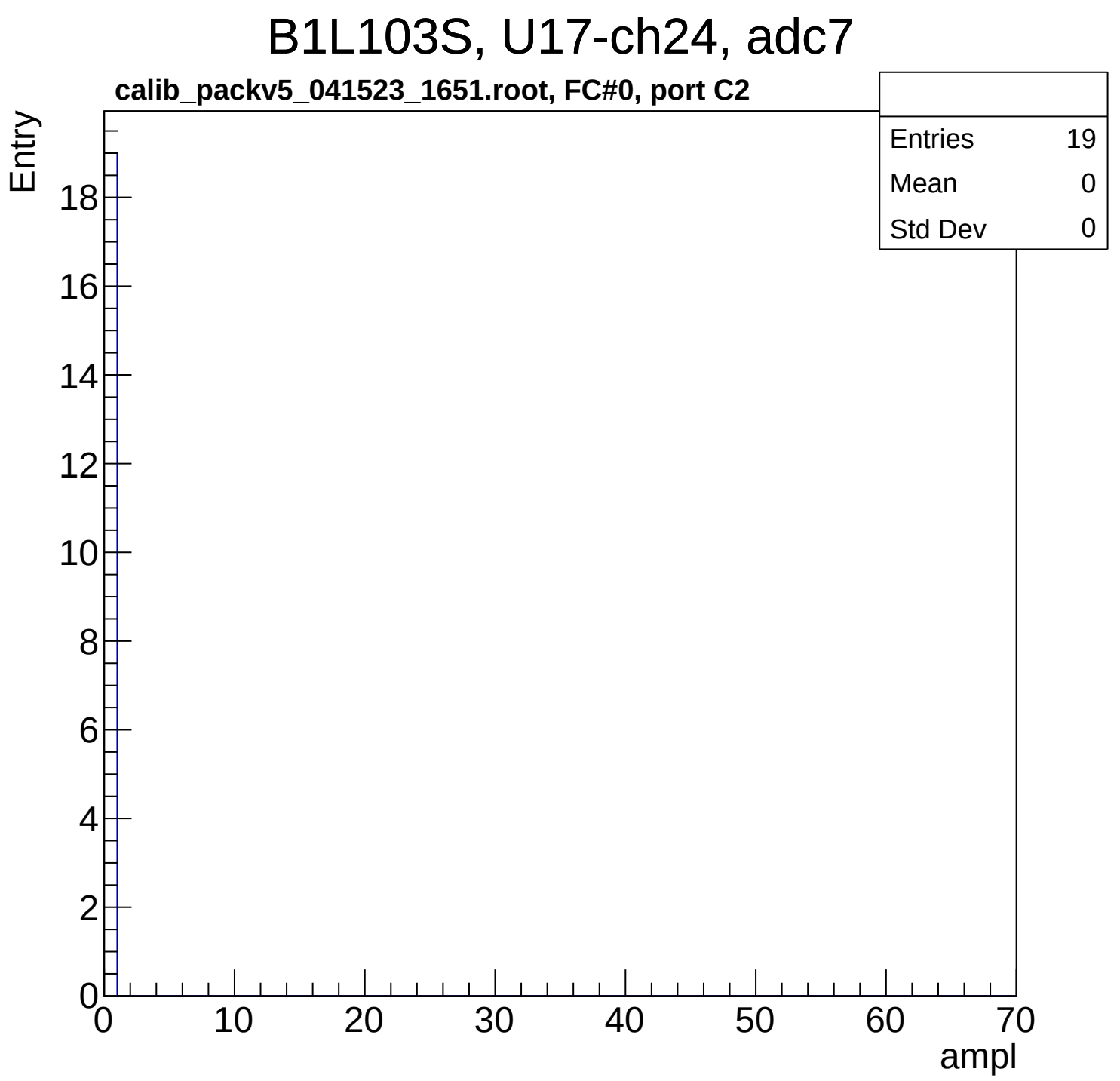

B1L103S, U17-ch24, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 37.12
Std Dev 15.49
Gaus mean : 44.5223
Gaus Width: 2.7234
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

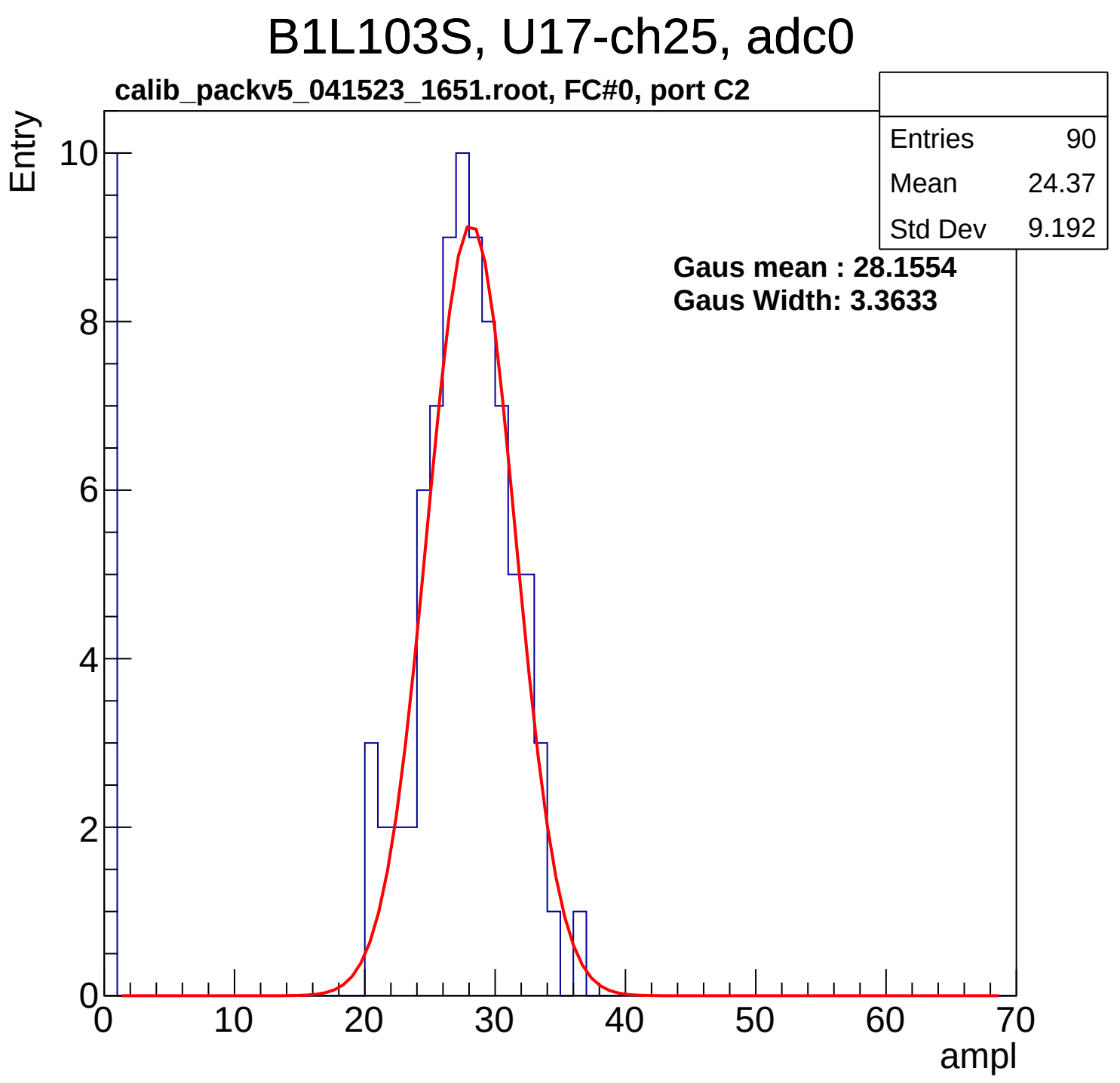

B1L103S, U17-ch24, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 48.21
Std Dev 3.242
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

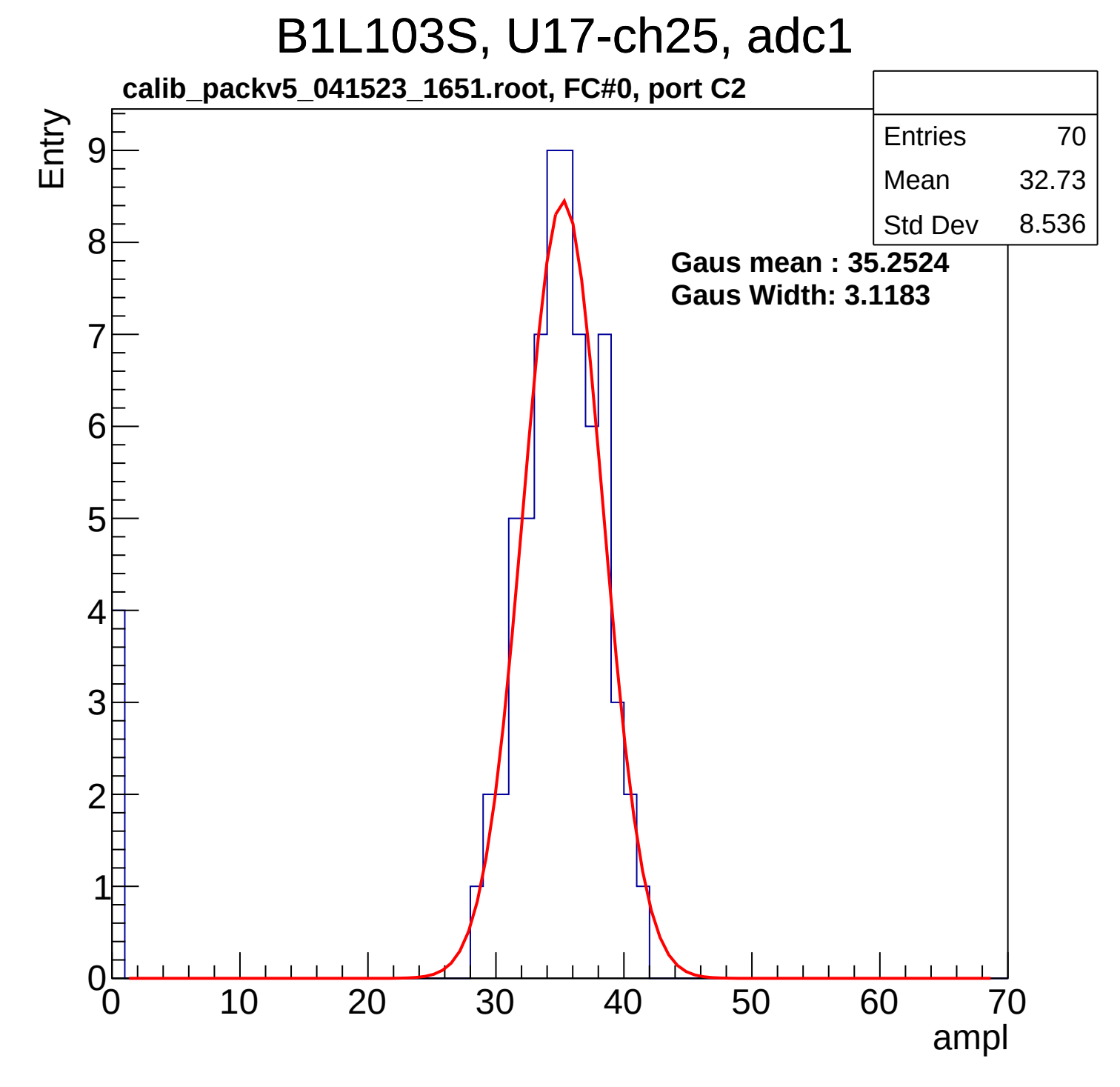

B1L103S, U17-ch24, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 54.06
Std Dev 3.381
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

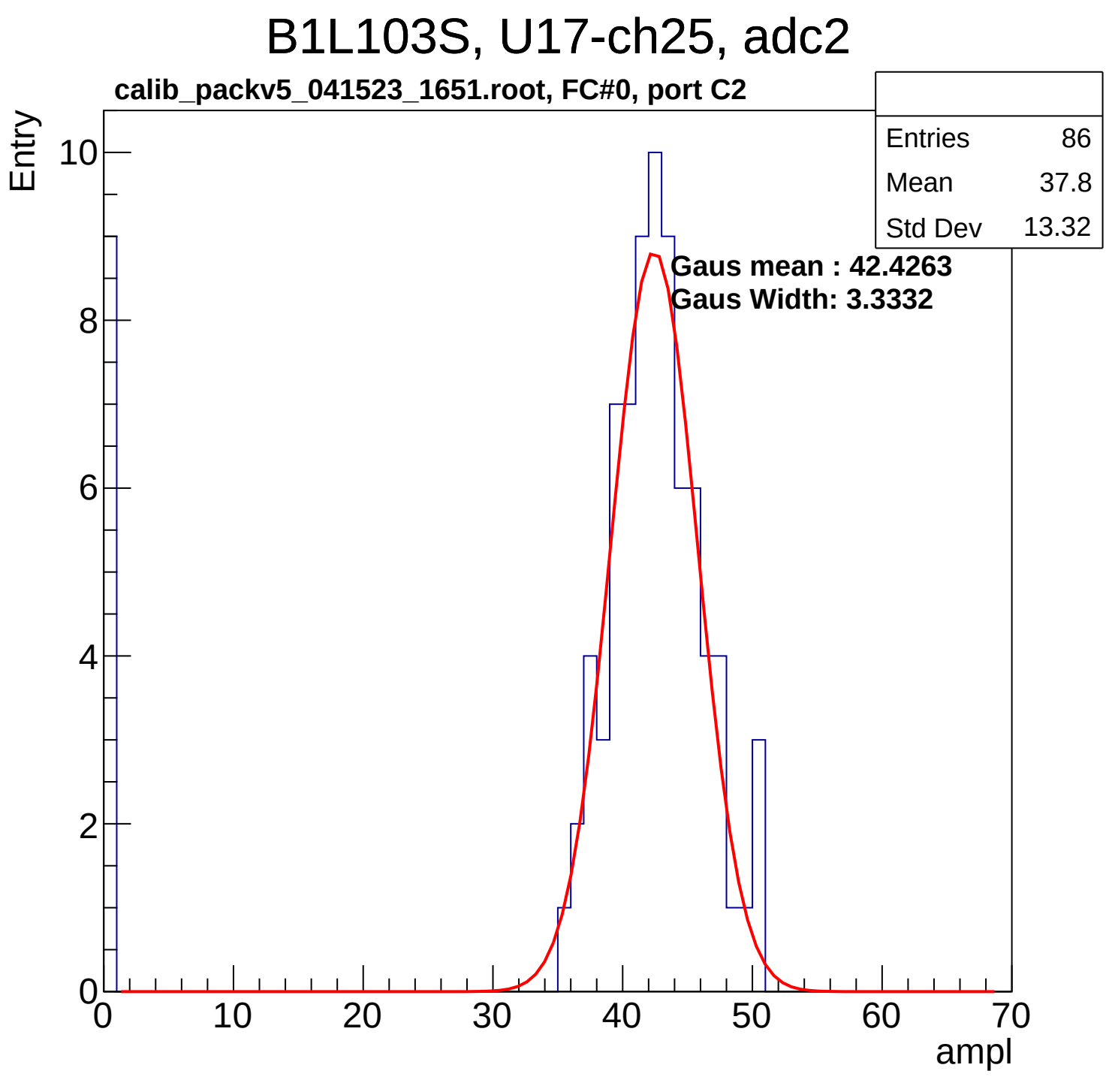

B1L103S, U17-ch24, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.29
Std Dev 8.776
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

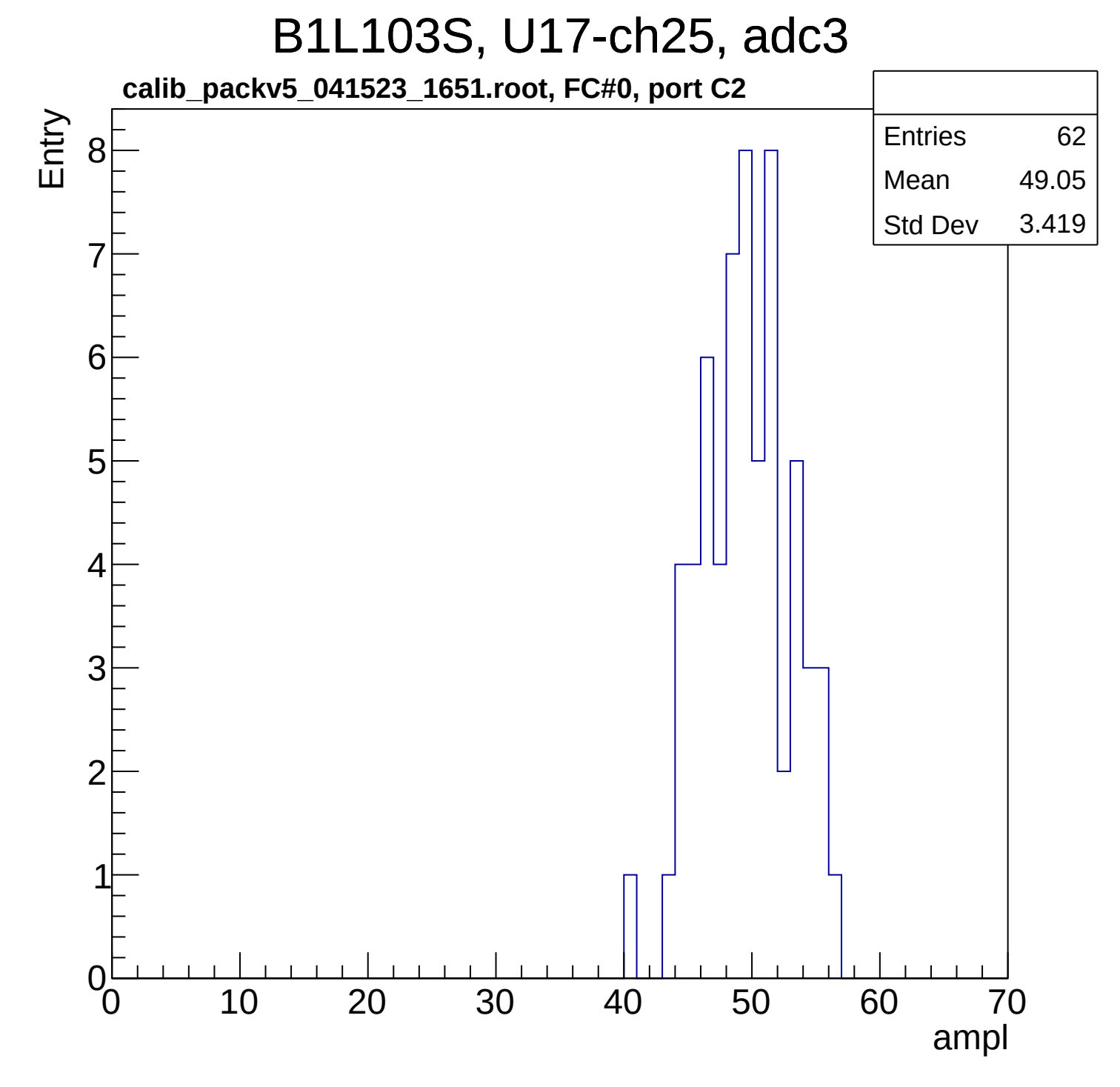

B1L103S, U17-ch24, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.5
Std Dev 1.555
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

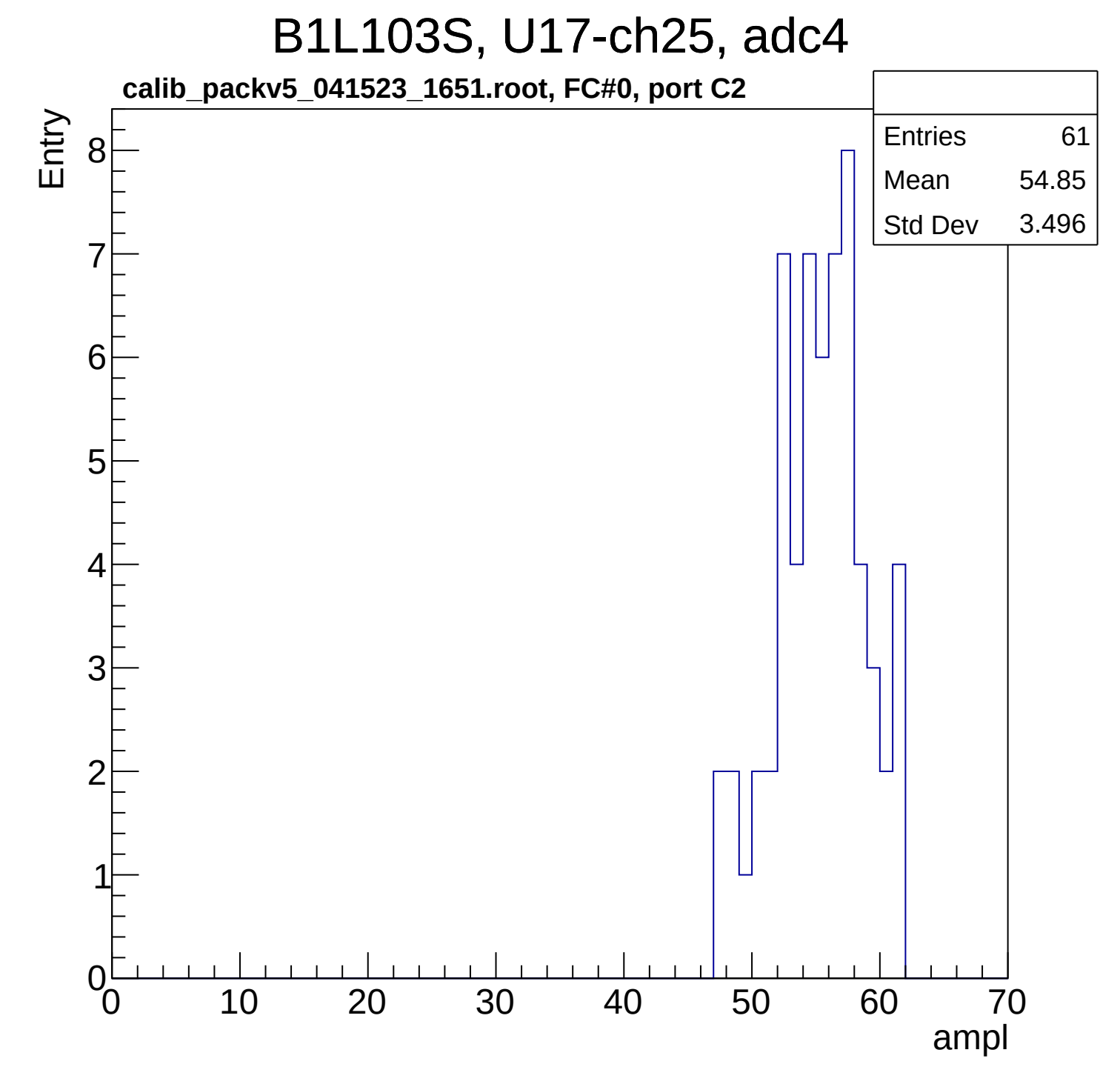

B1L103S, U17-ch24, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

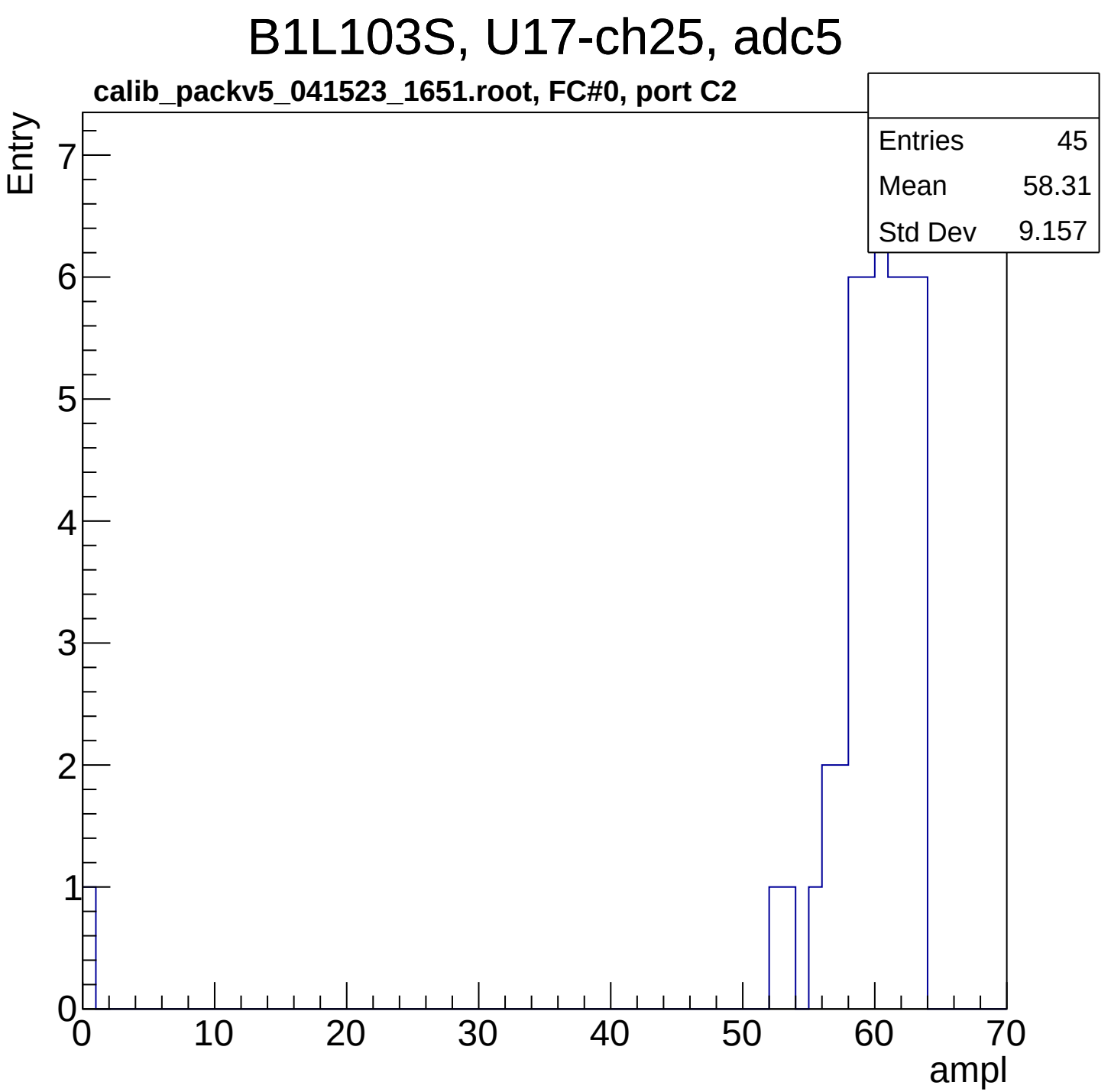

B1L103S, U17-ch25, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 24.37
Std Dev 9.192
Gaus mean : 28.1554
Gaus Width: 3.3633
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

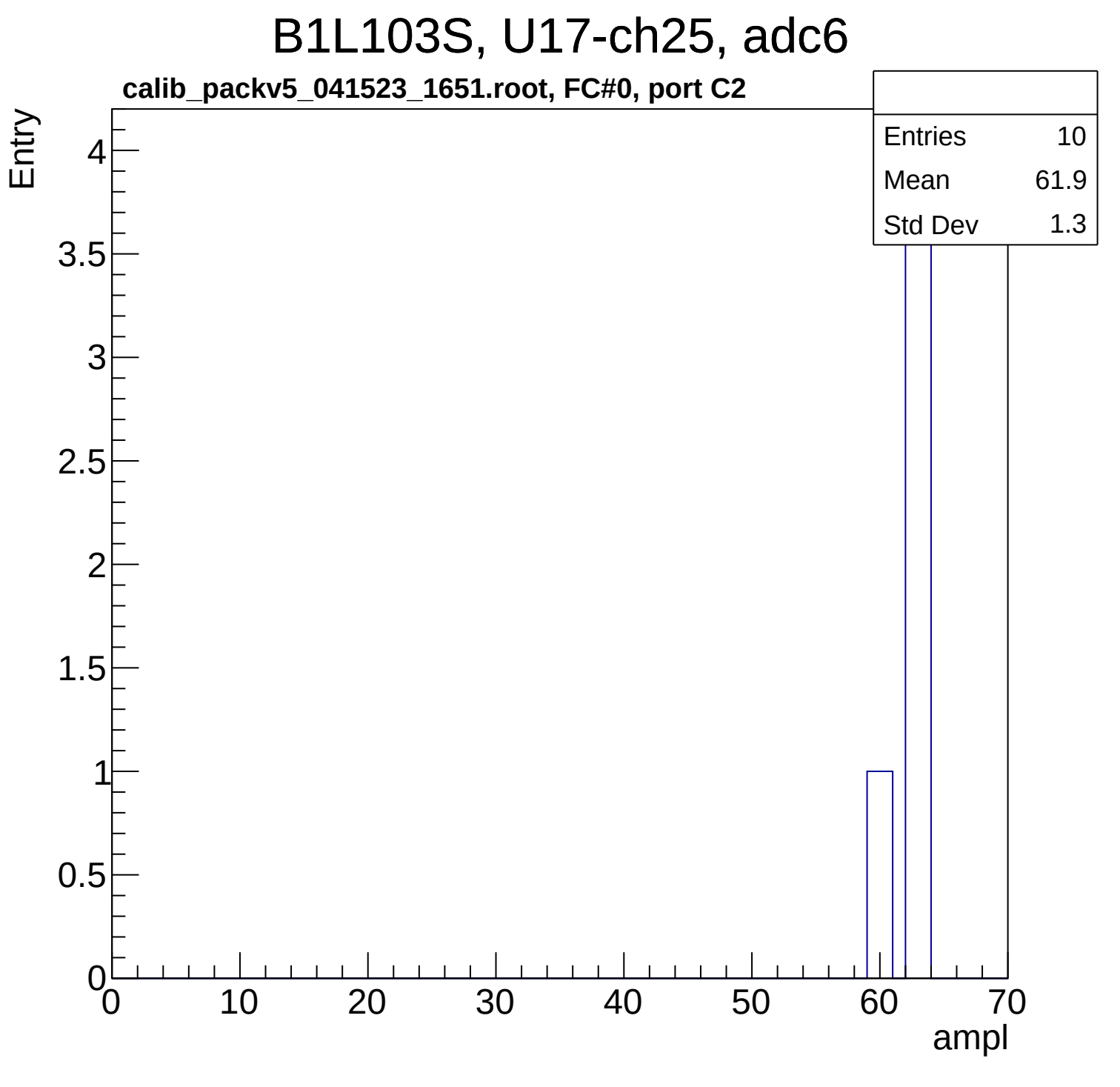

B1L103S, U17-ch25, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 32.73
Std Dev 8.536
Gaus mean : 35.2524
Gaus Width: 3.1183
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

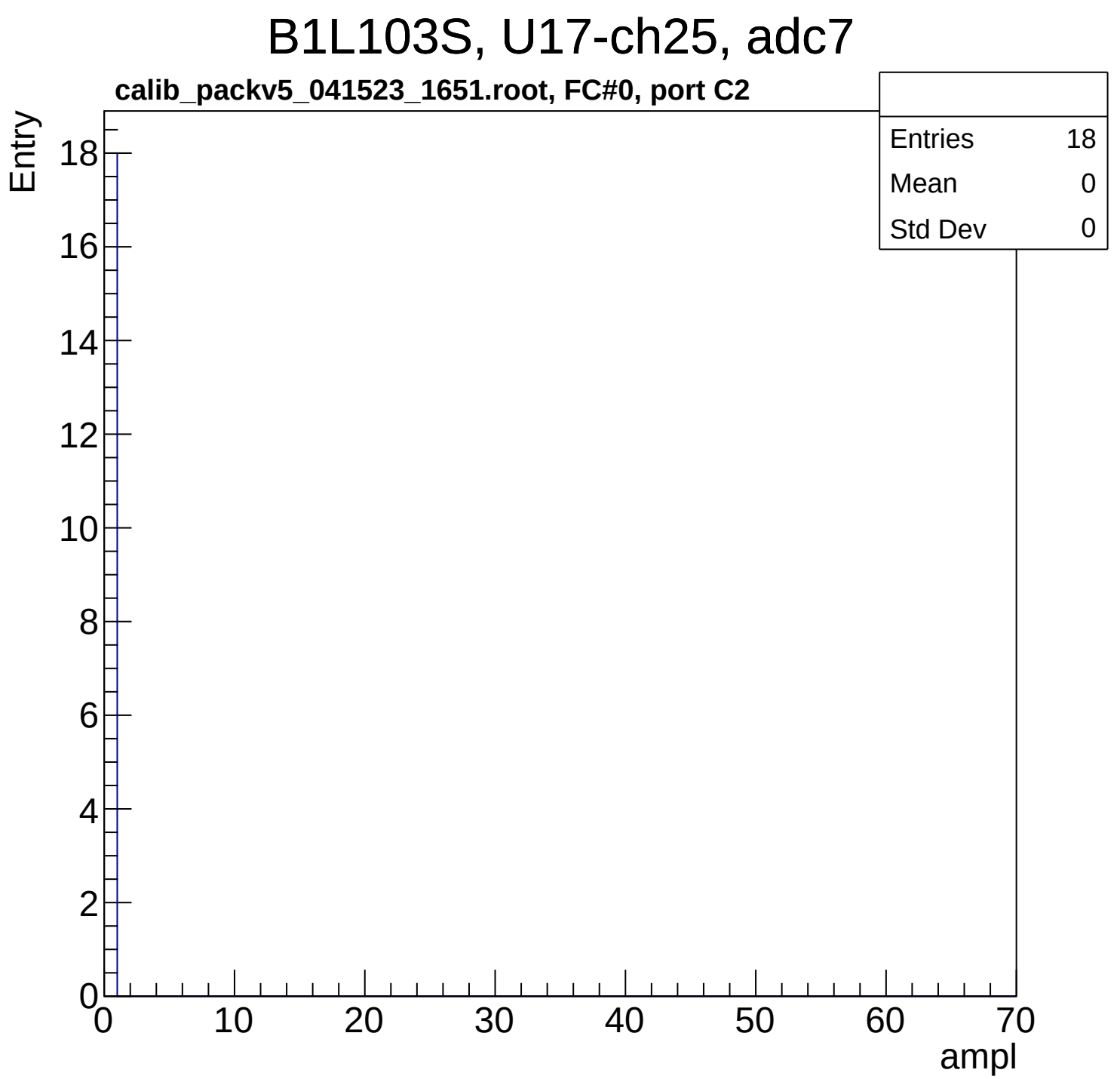

B1L103S, U17-ch25, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 37.8
Std Dev 13.32
Gaus mean : 42.4263
Gaus Width: 3.3332
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

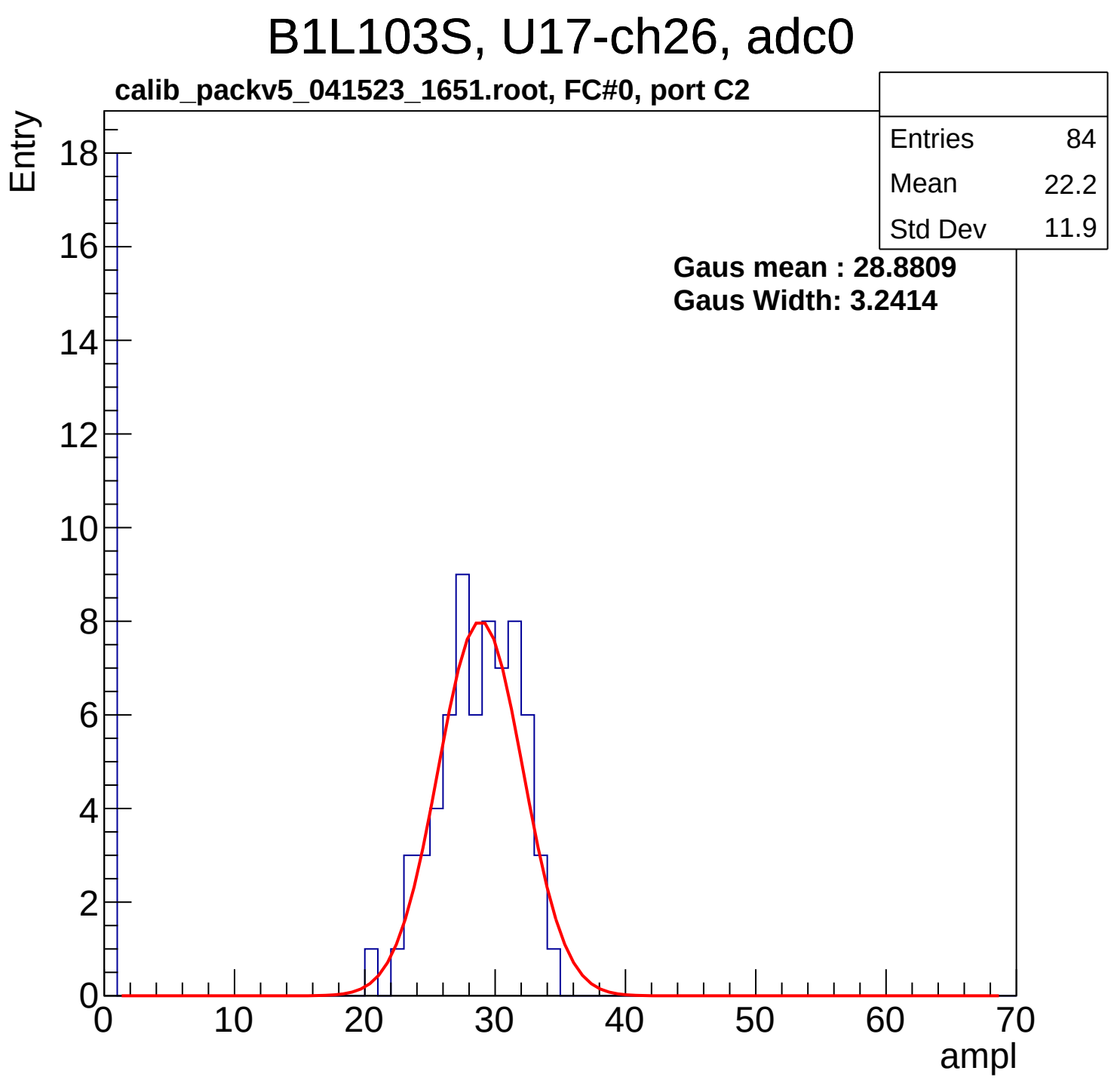

B1L103S, U17-ch25, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 49.05
Std Dev 3.419
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

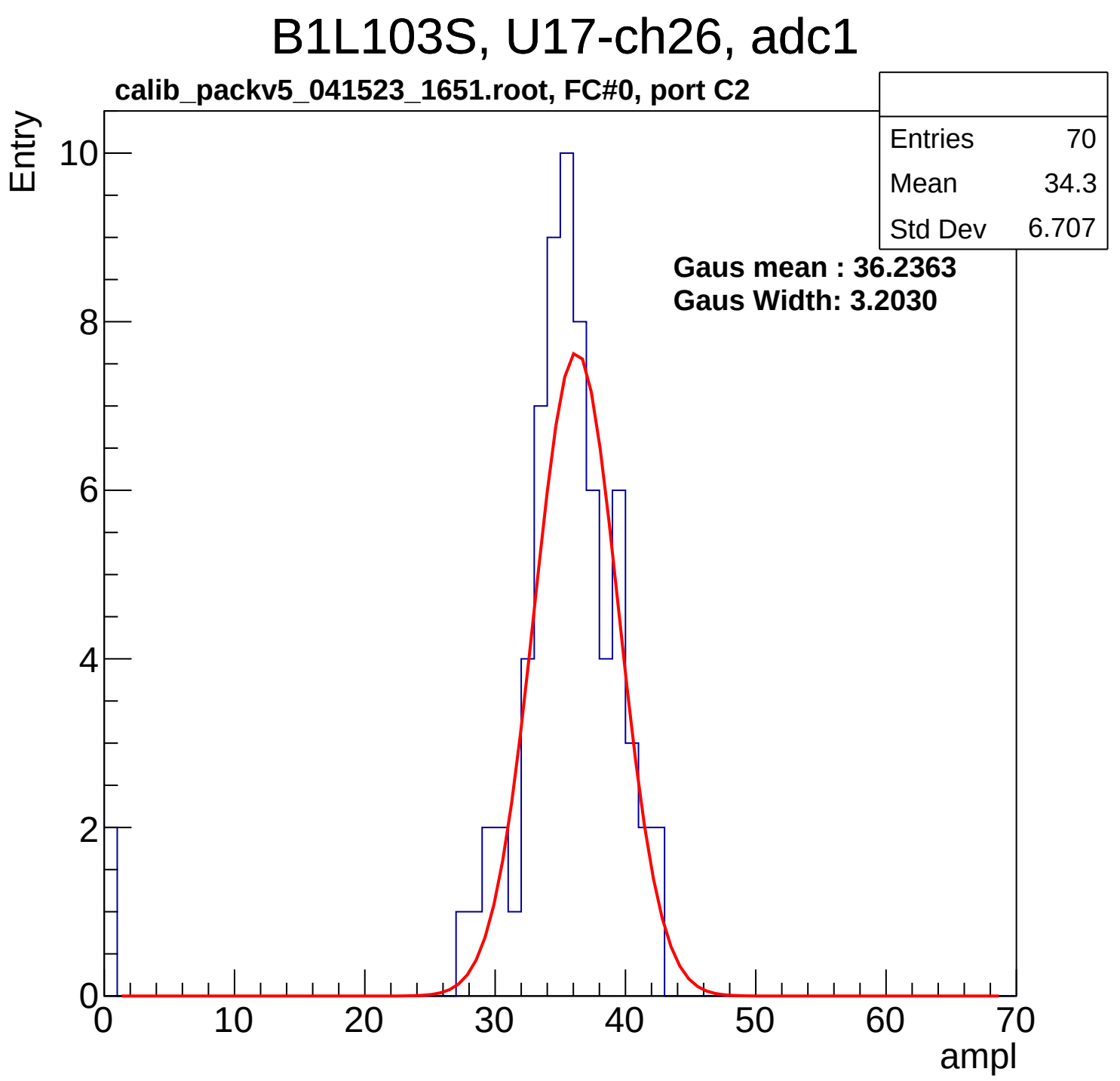

B1L103S, U17-ch25, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 54.85
Std Dev 3.496
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

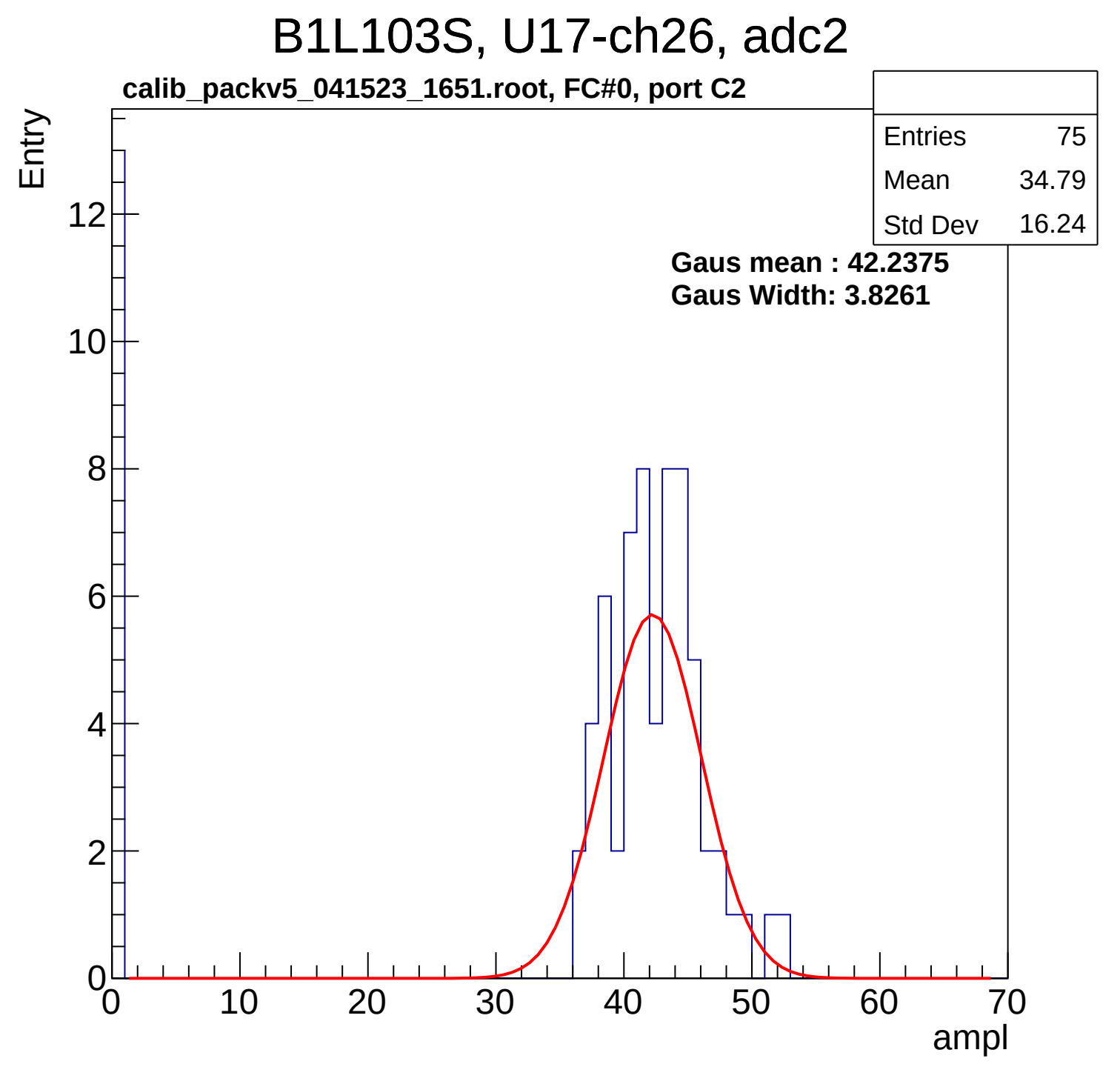

B1L103S, U17-ch25, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.31
Std Dev 9.157
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

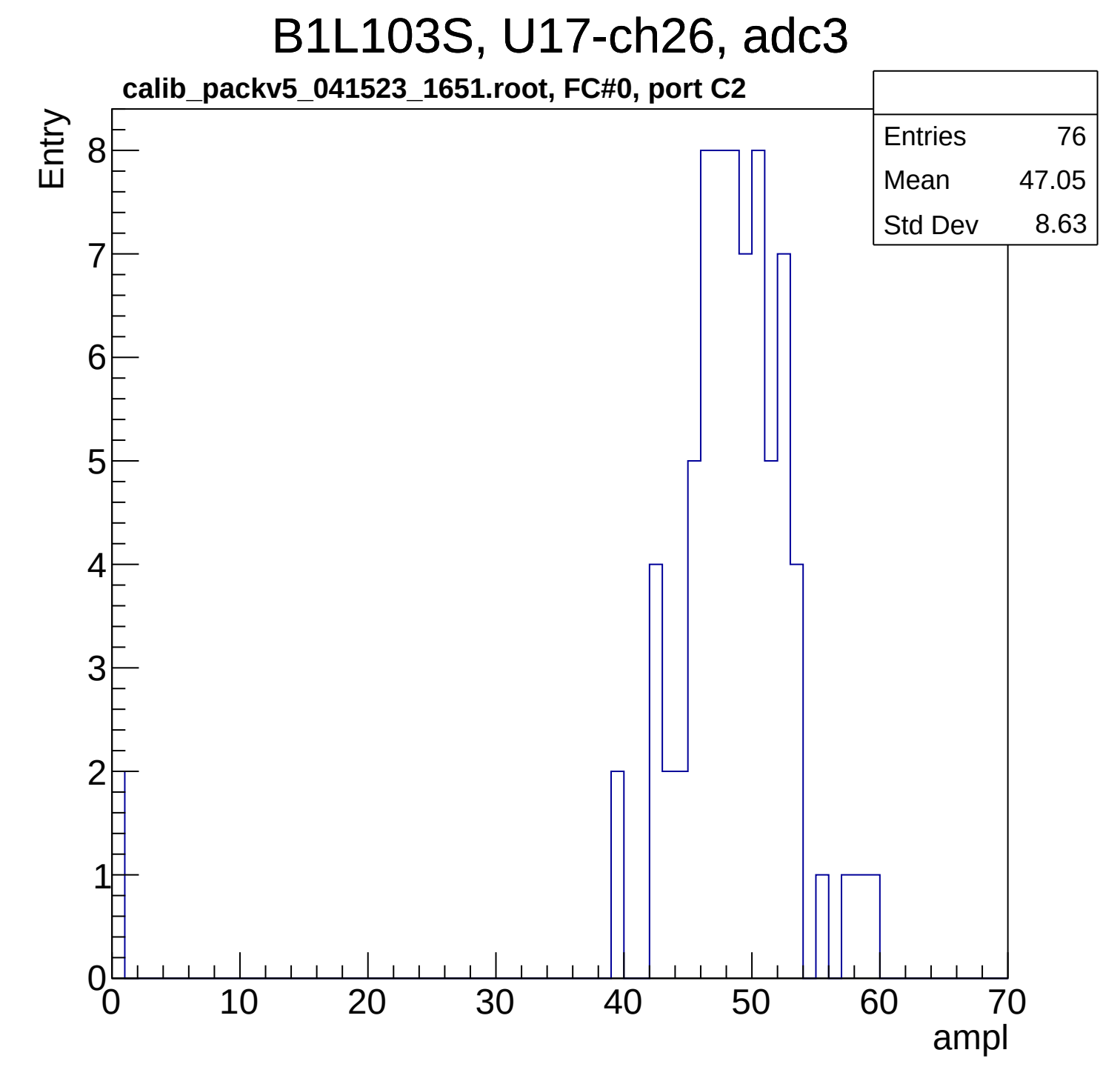

B1L103S, U17-ch25, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.9
Std Dev 1.3
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

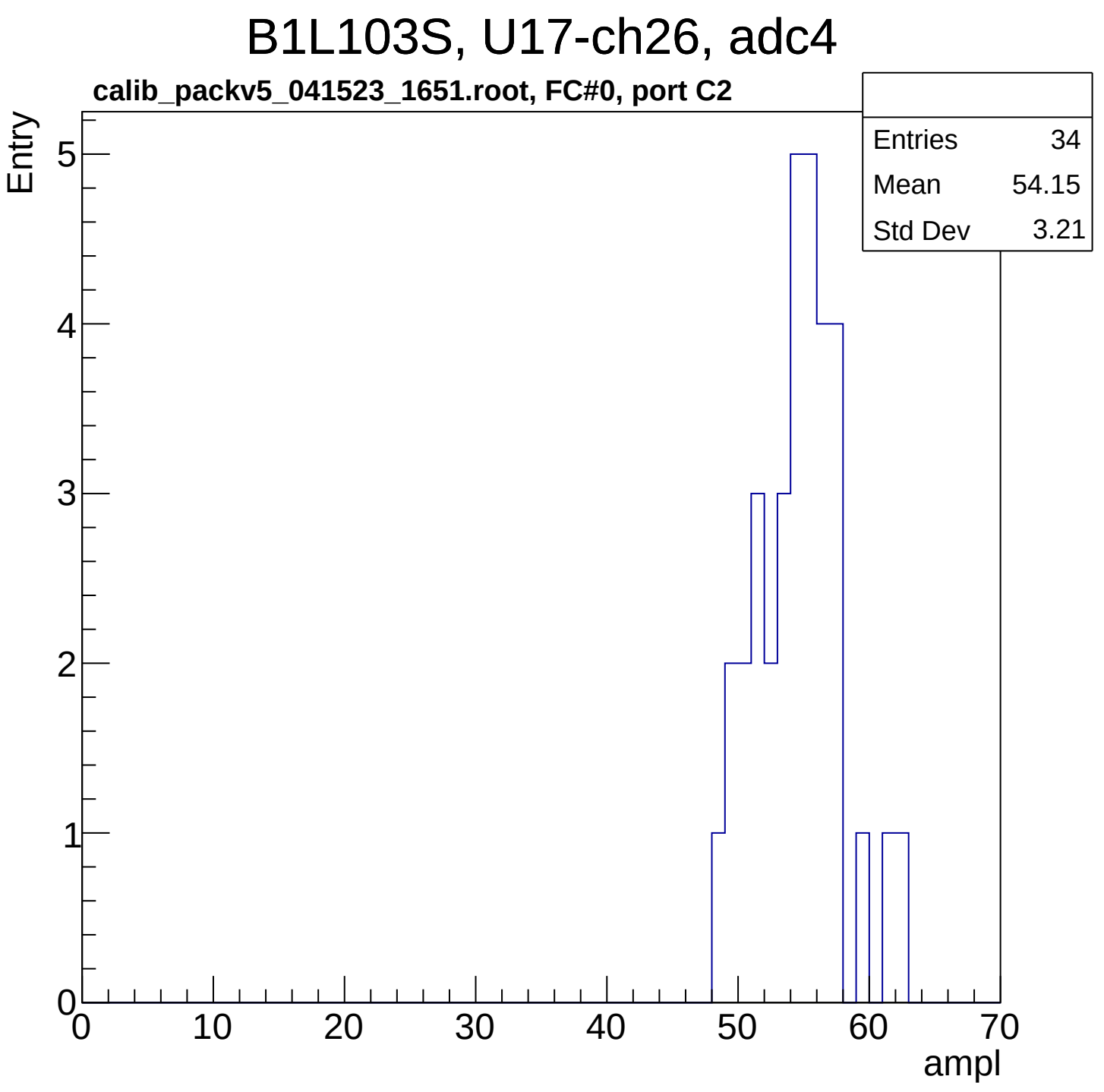

B1L103S, U17-ch25, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

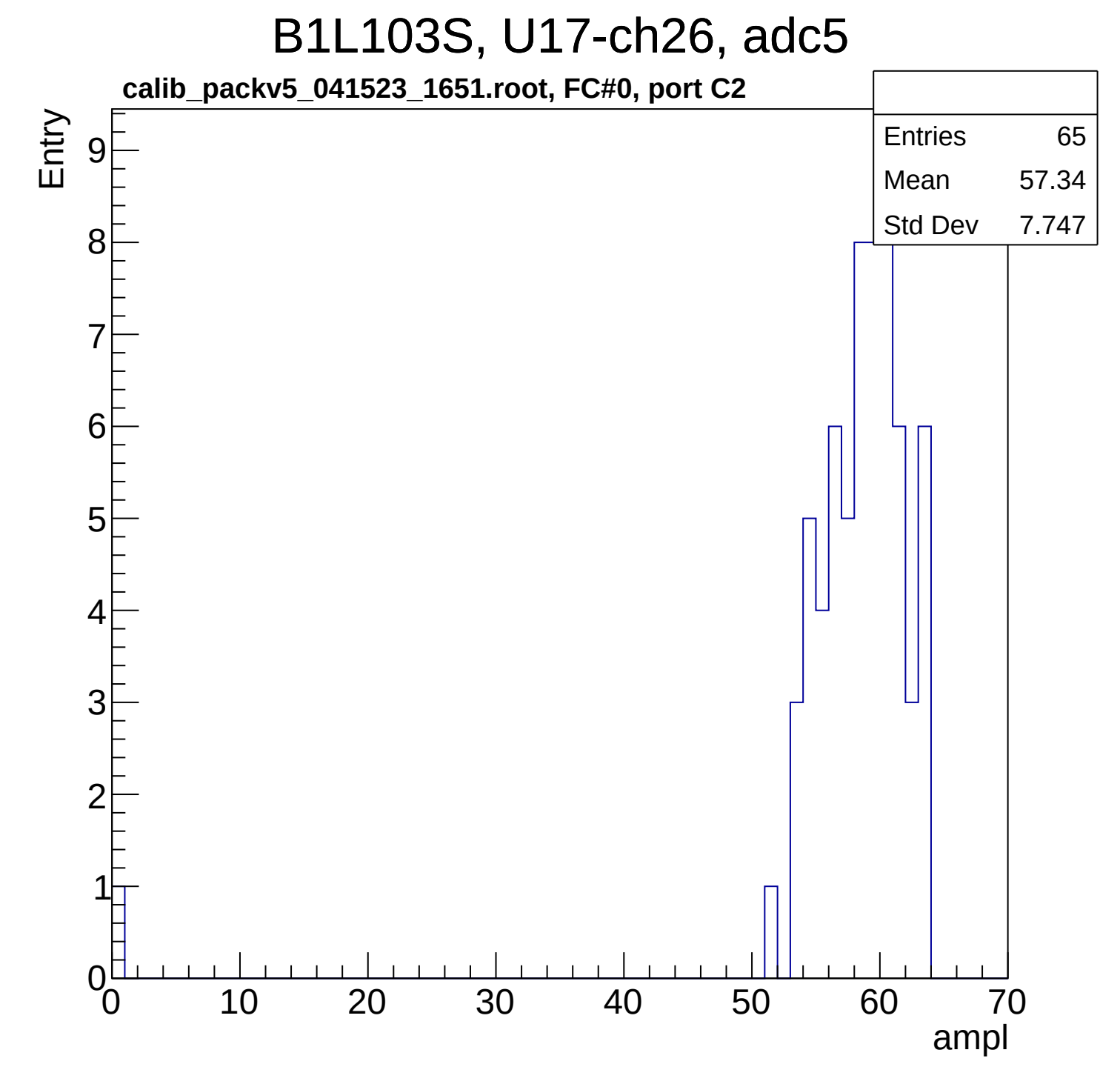

B1L103S, U17-ch26, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 22.2
Std Dev 11.9
Gaus mean : 28.8809
Gaus Width: 3.2414
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

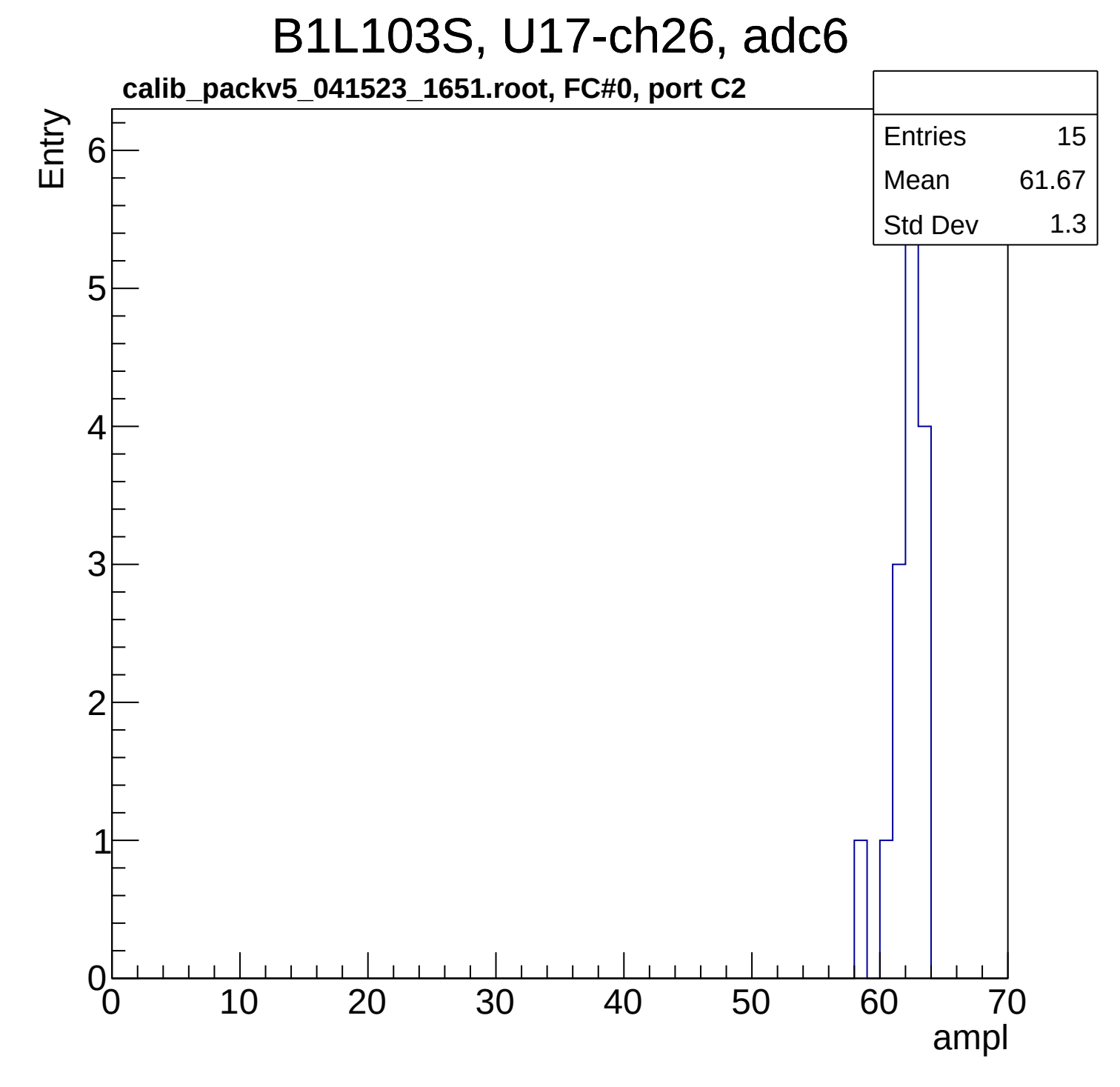

B1L103S, U17-ch26, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 34.3
Std Dev 6.707
Gaus mean : 36.2363
Gaus Width: 3.2030
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

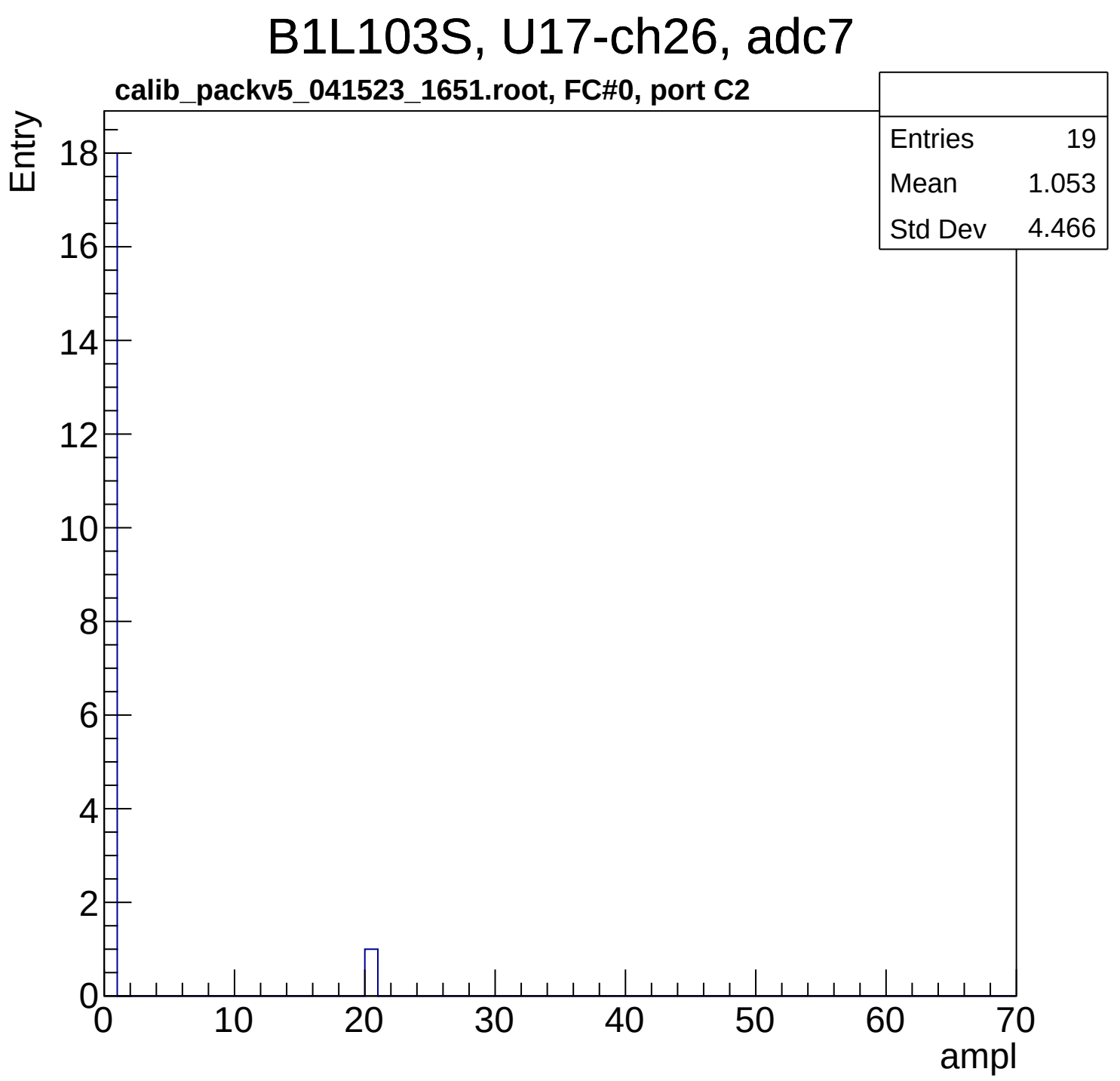

B1L103S, U17-ch26, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 34.79
Std Dev 16.24
Gaus mean : 42.2375
Gaus Width: 3.8261
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

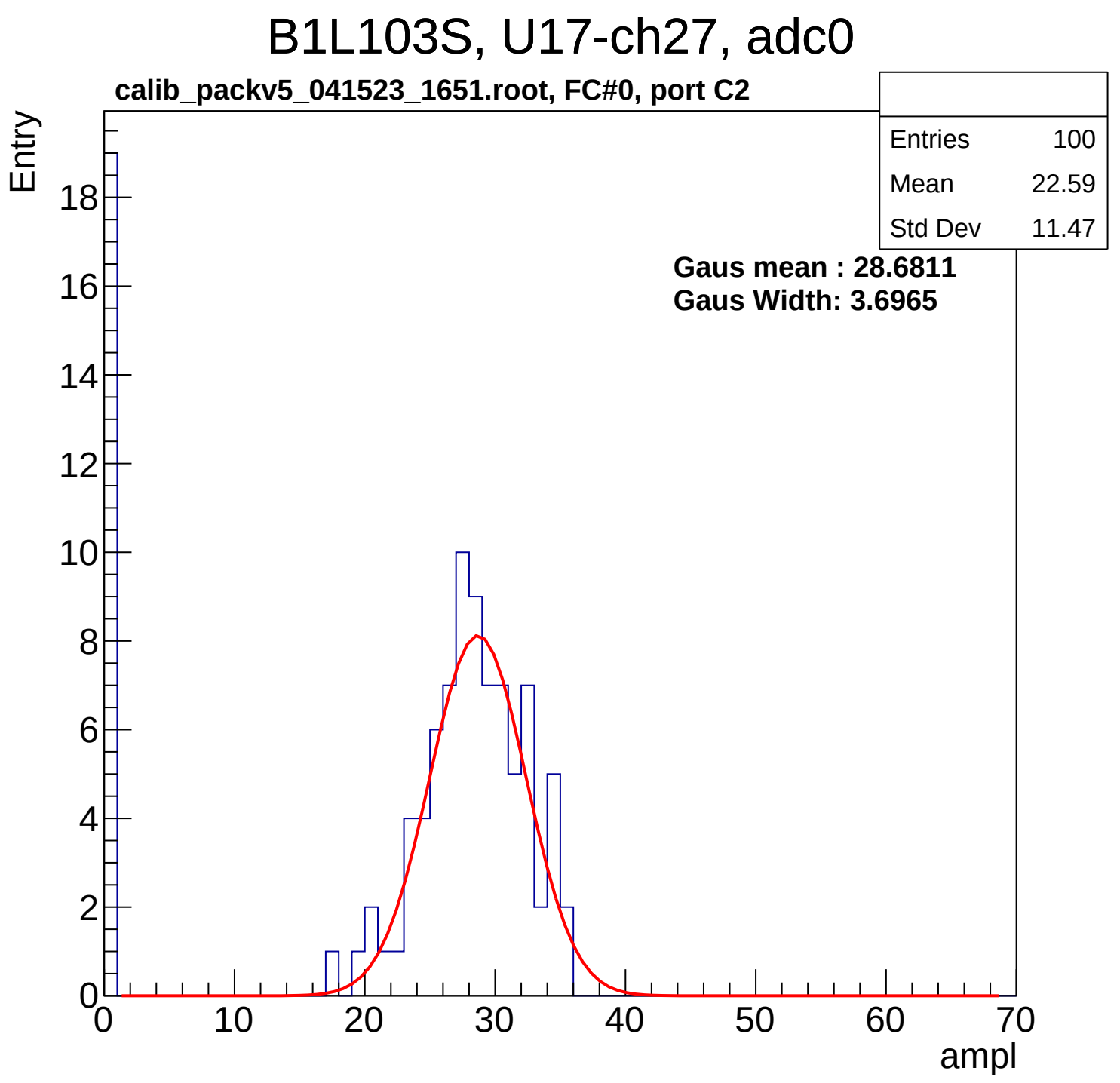

B1L103S, U17-ch26, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 47.05
Std Dev 8.63
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

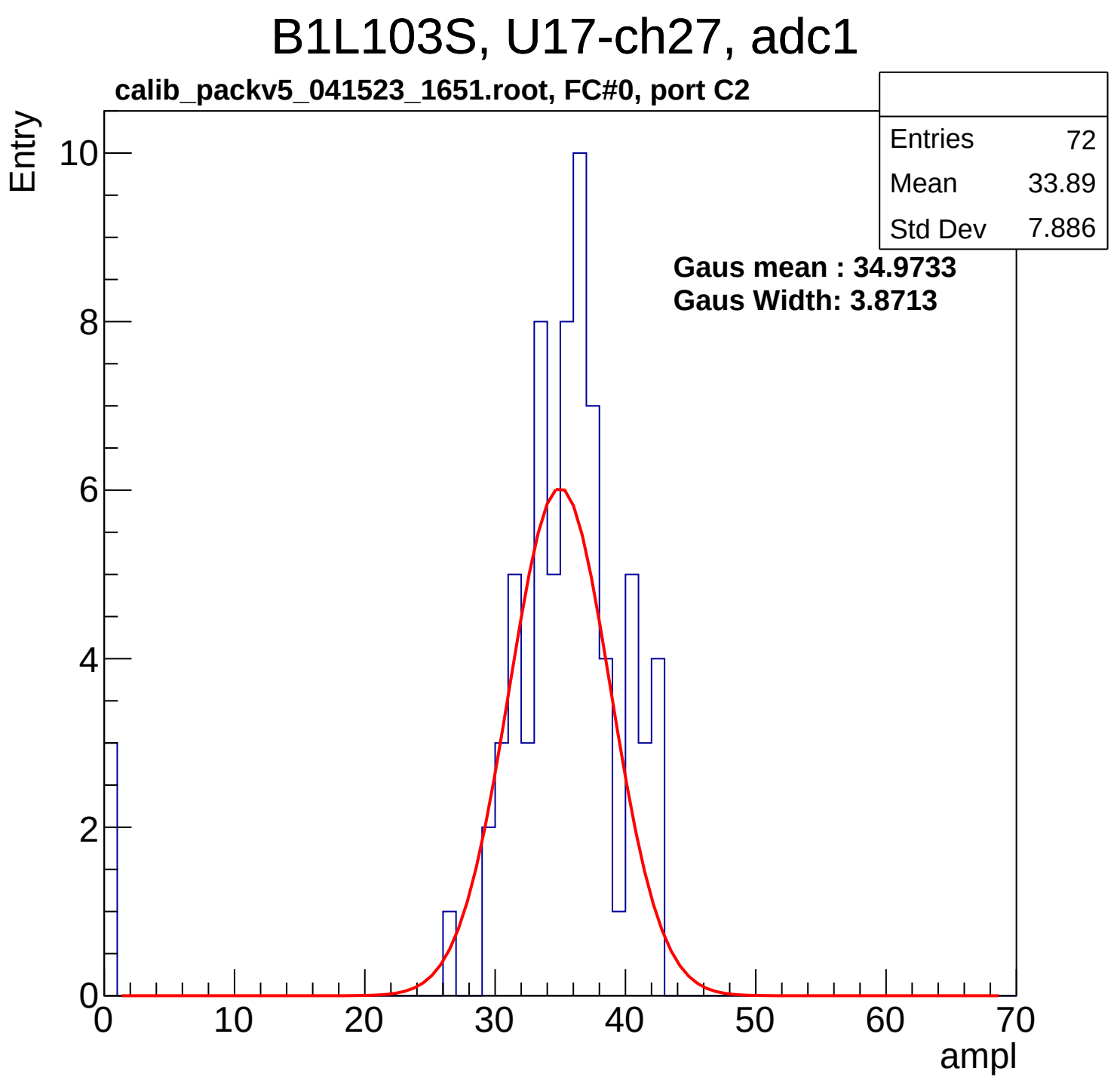

B1L103S, U17-ch26, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 54.15
Std Dev 3.21
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

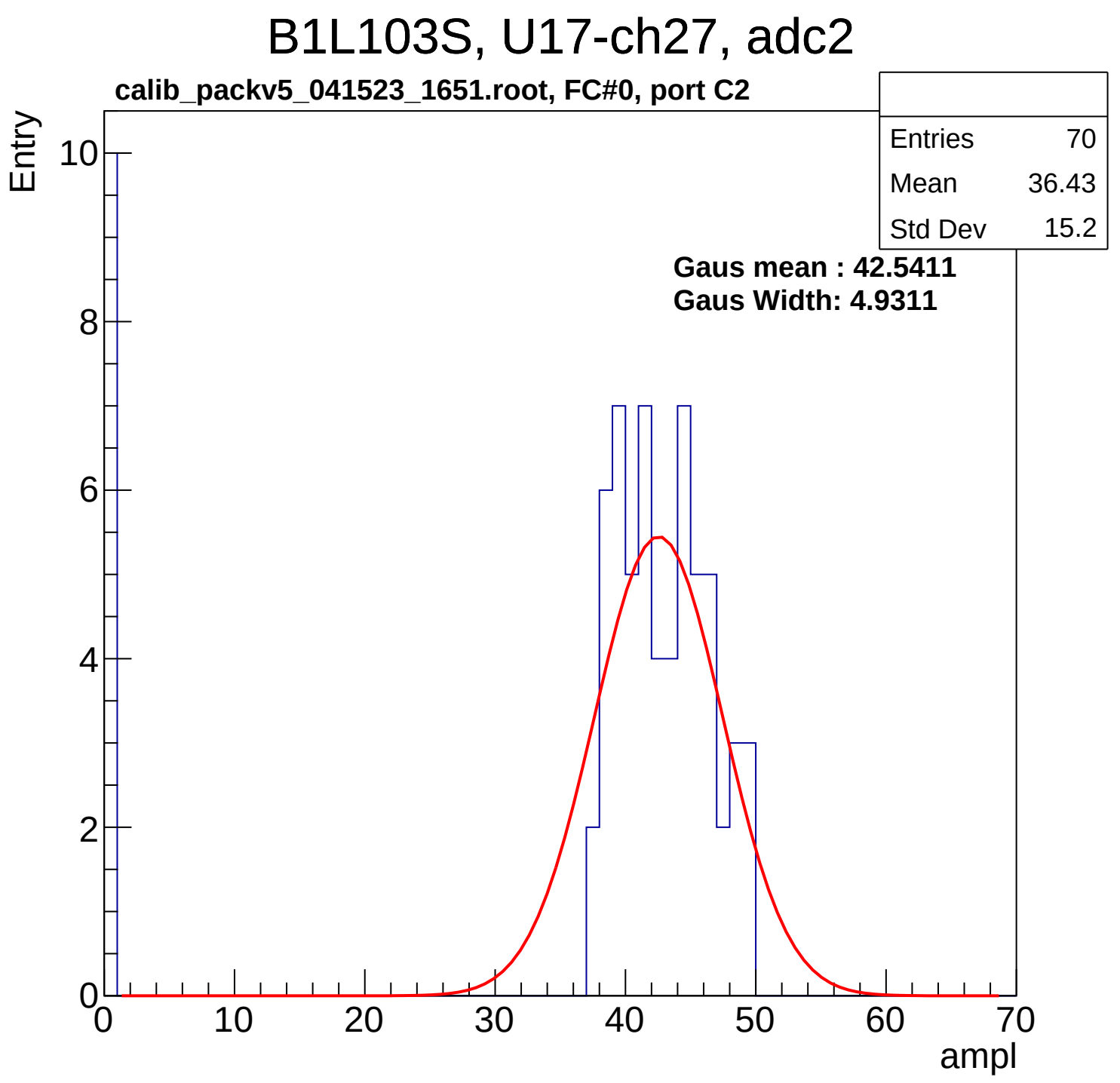

B1L103S, U17-ch26, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 57.34
Std Dev 7.747
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

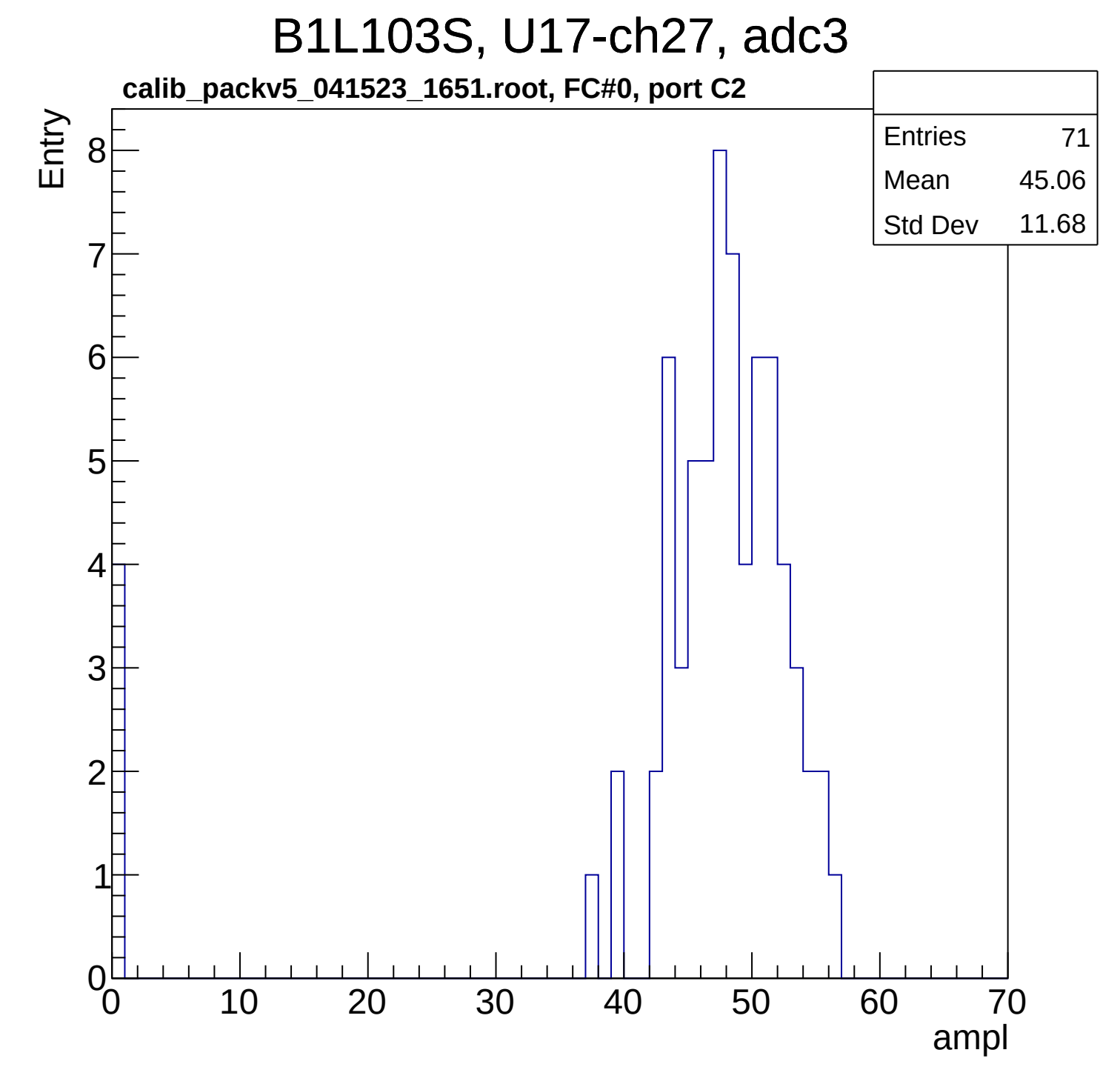

B1L103S, U17-ch26, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.67
Std Dev 1.3
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

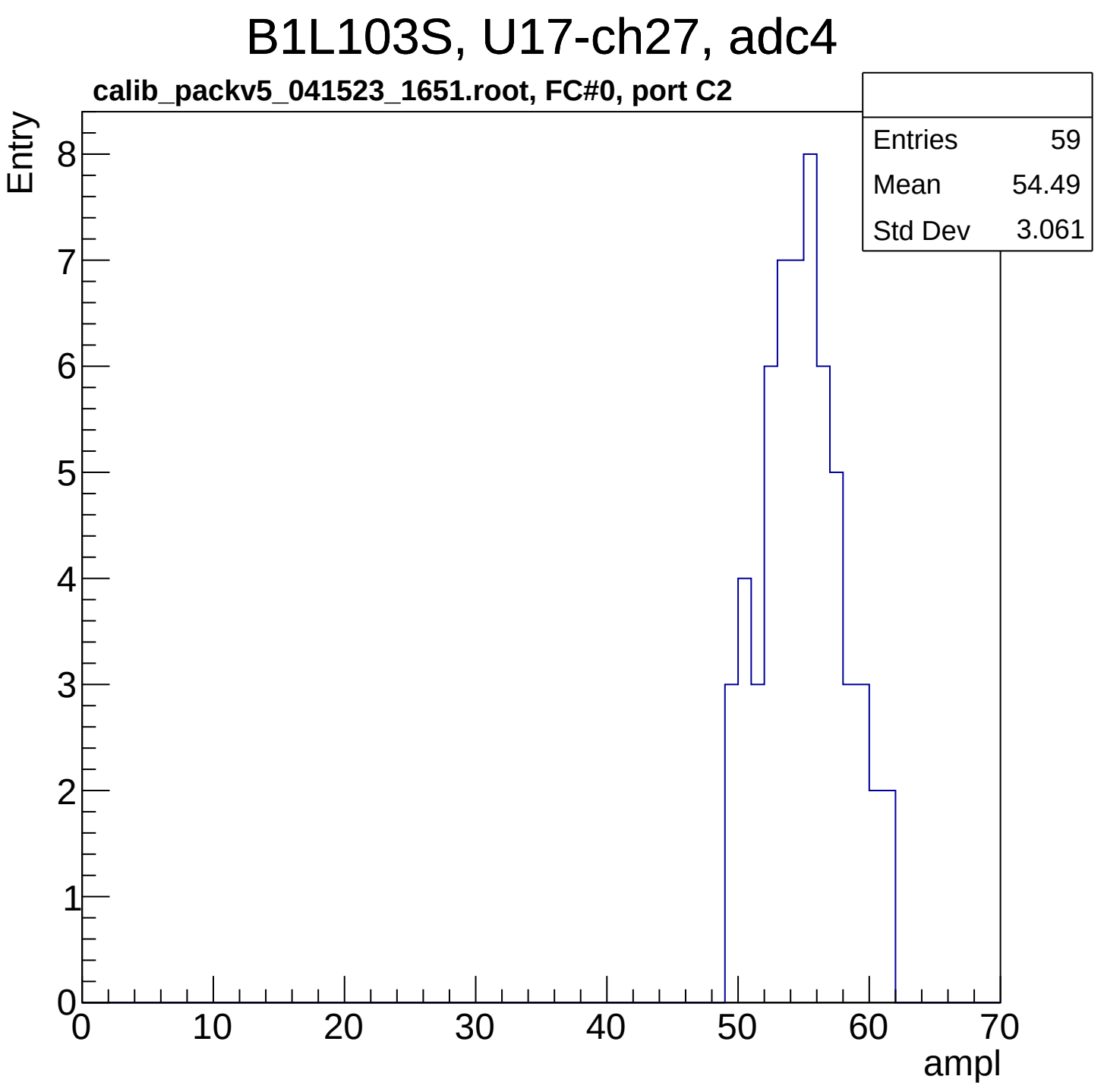

B1L103S, U17-ch26, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.053
Std Dev 4.466
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

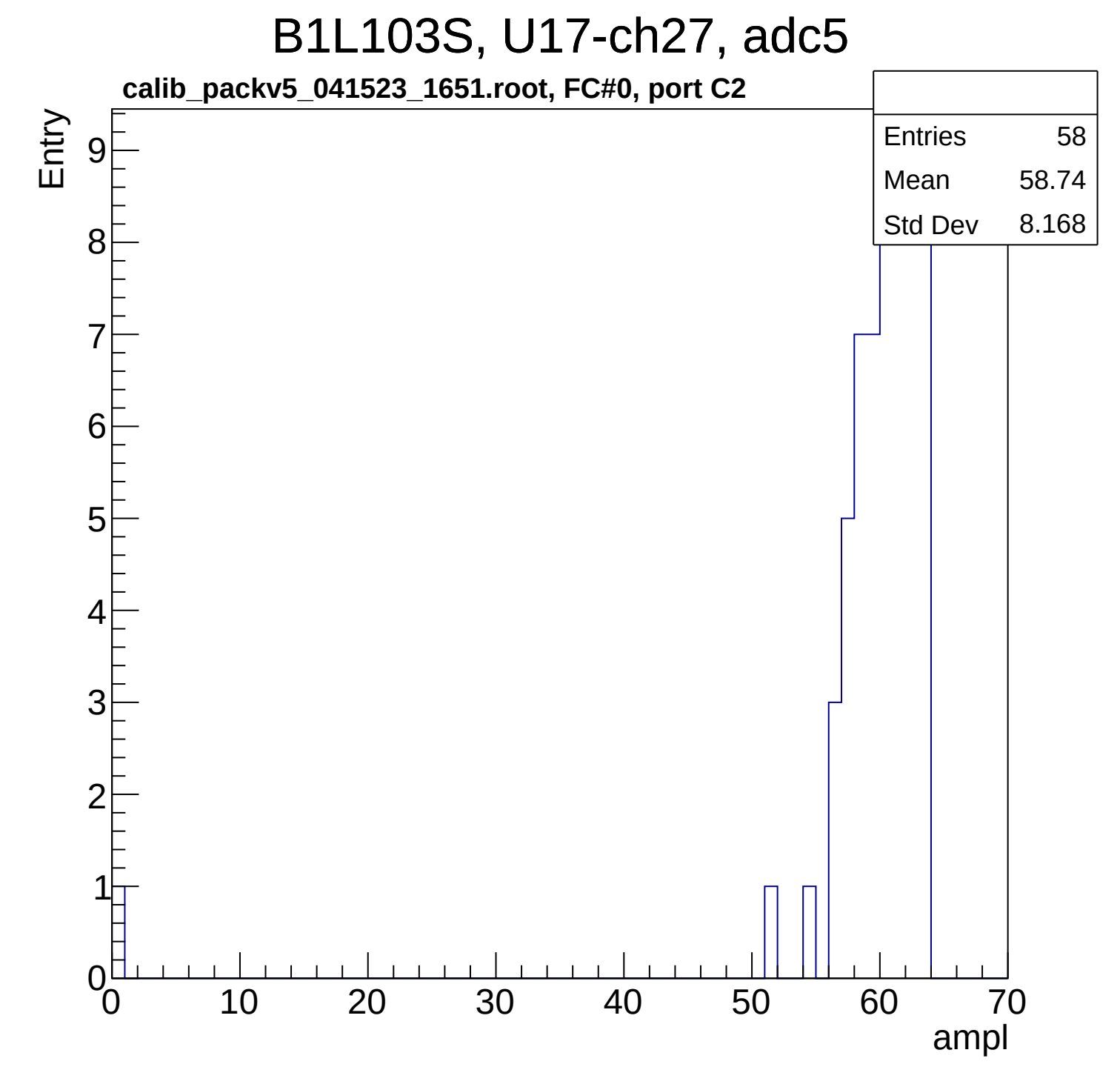

B1L103S, U17-ch27, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 22.59
Std Dev 11.47
Gaus mean : 28.6811
Gaus Width: 3.6965
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

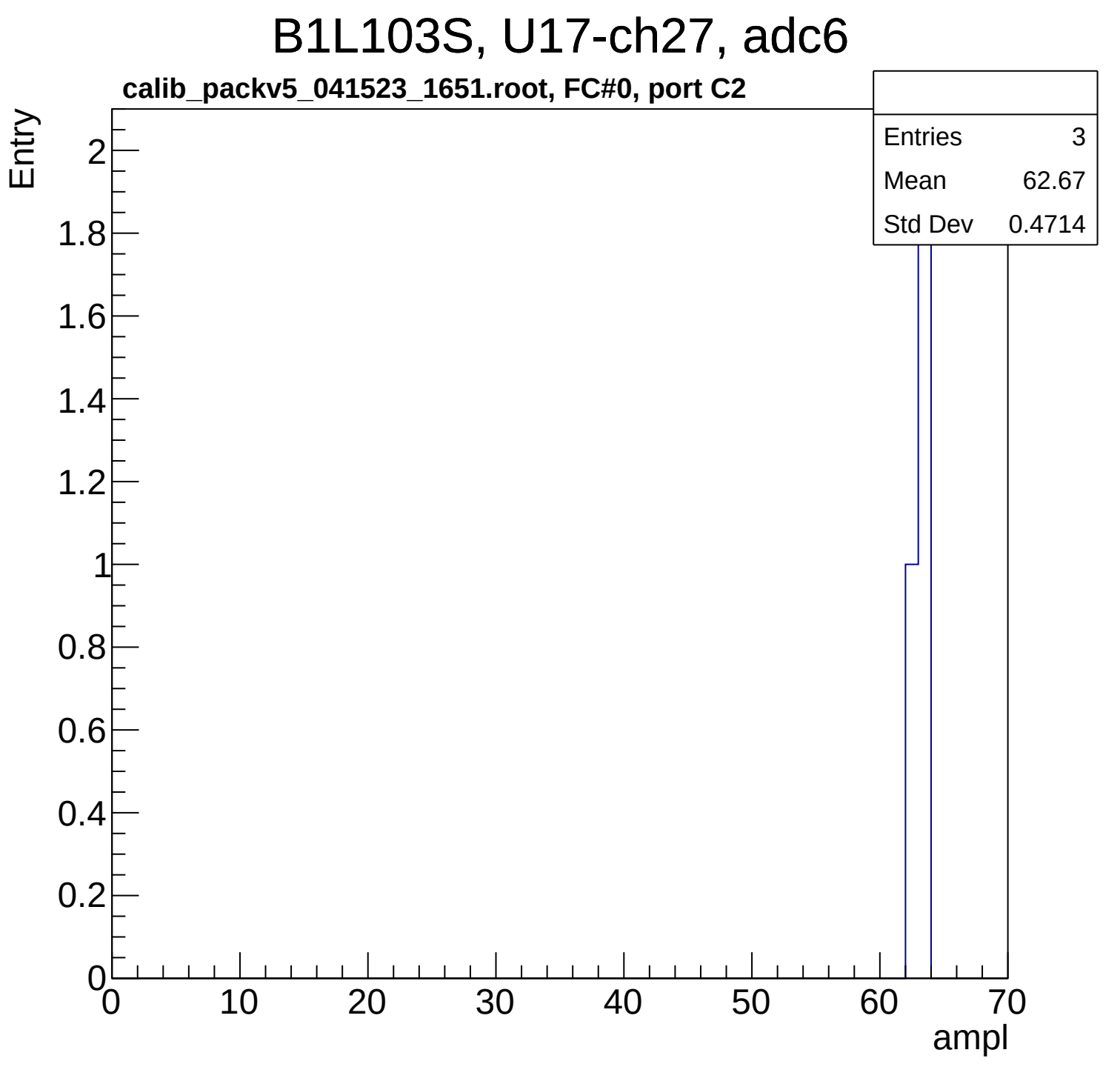

B1L103S, U17-ch27, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 33.89
Std Dev 7.886
Gaus mean : 34.9733
Gaus Width: 3.8713
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

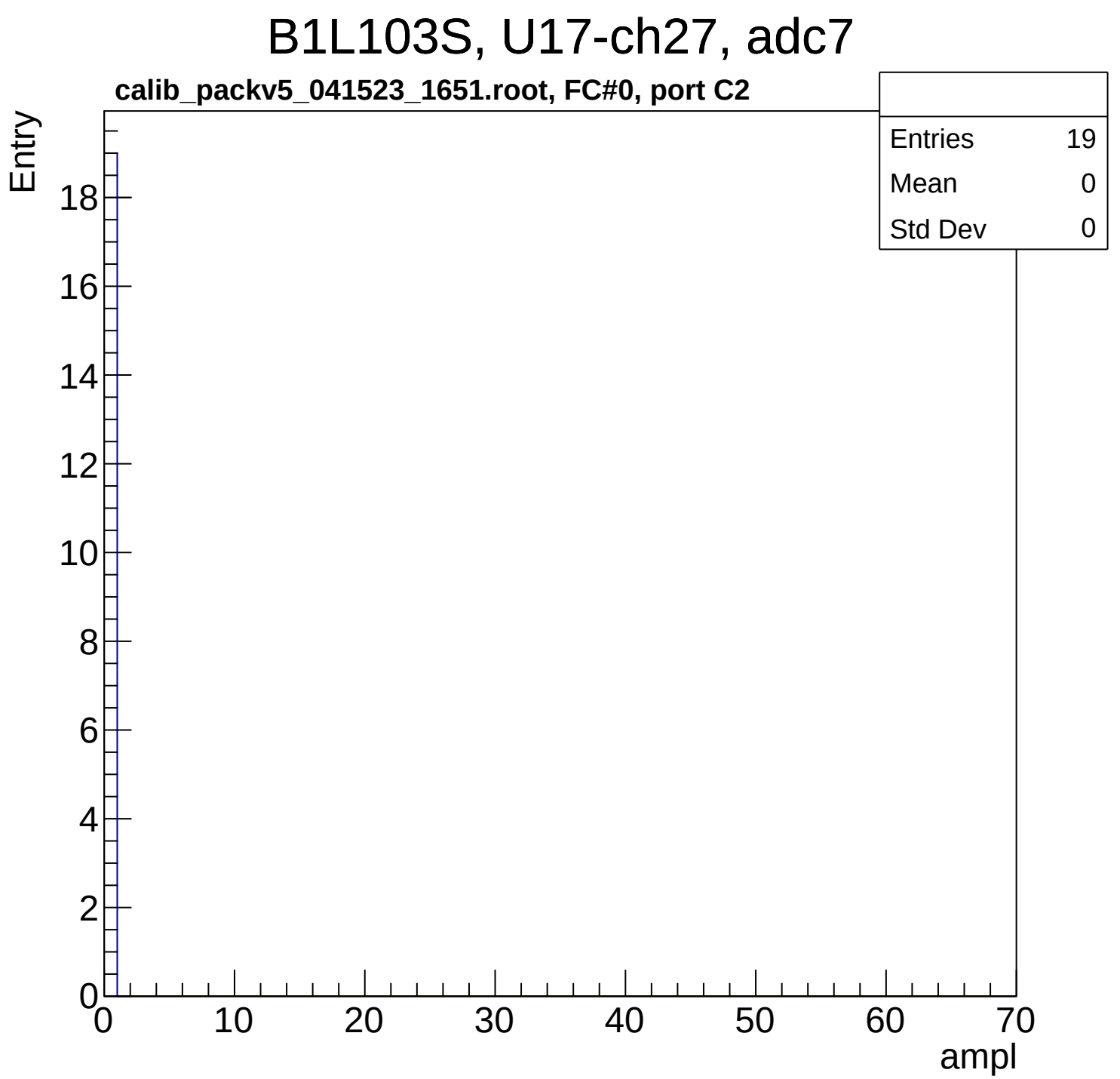

B1L103S, U17-ch27, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 36.43
Std Dev 15.2
Gaus mean : 42.5411
Gaus Width: 4.9311
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

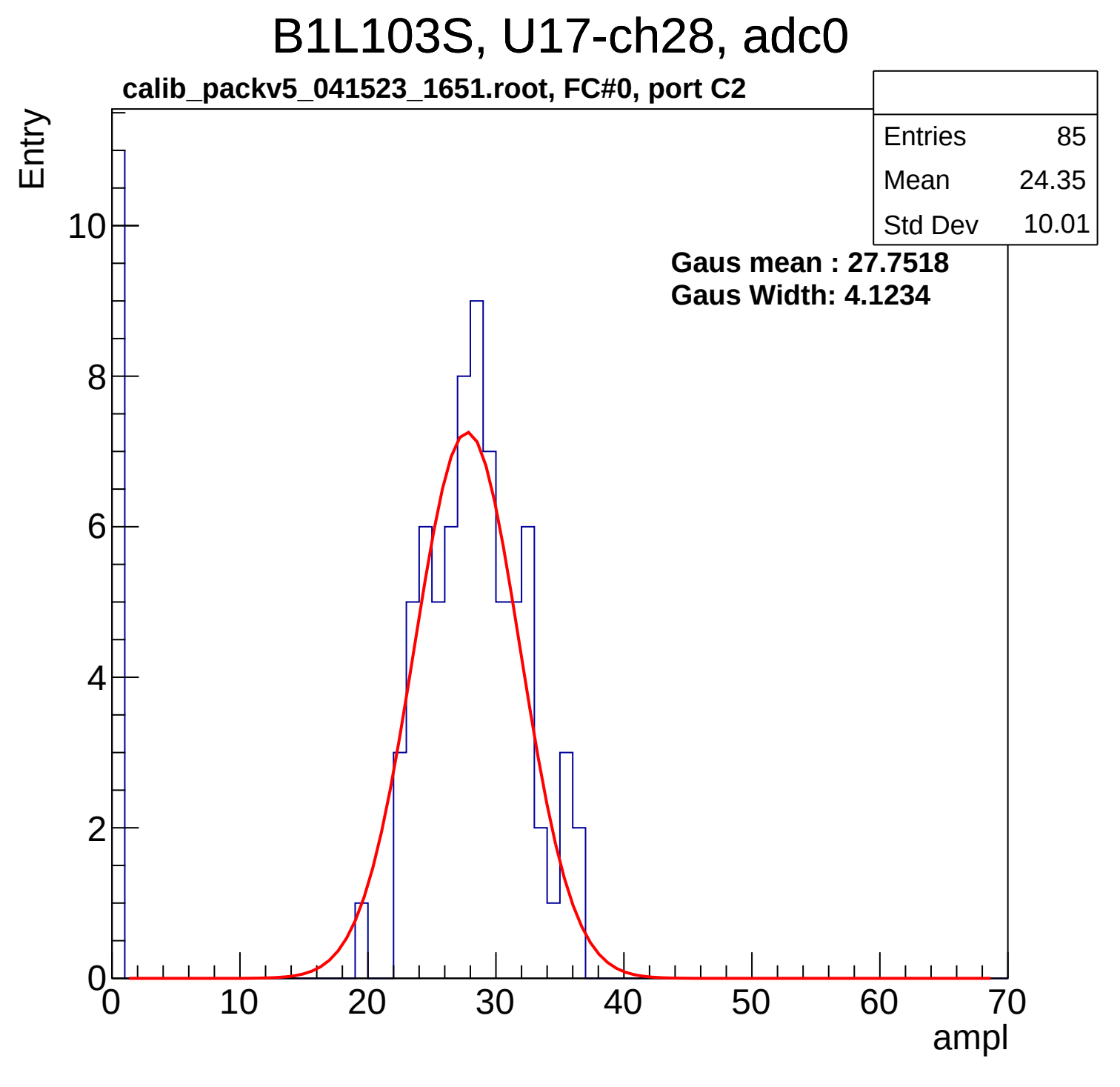

B1L103S, U17-ch27, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 45.06
Std Dev 11.68
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

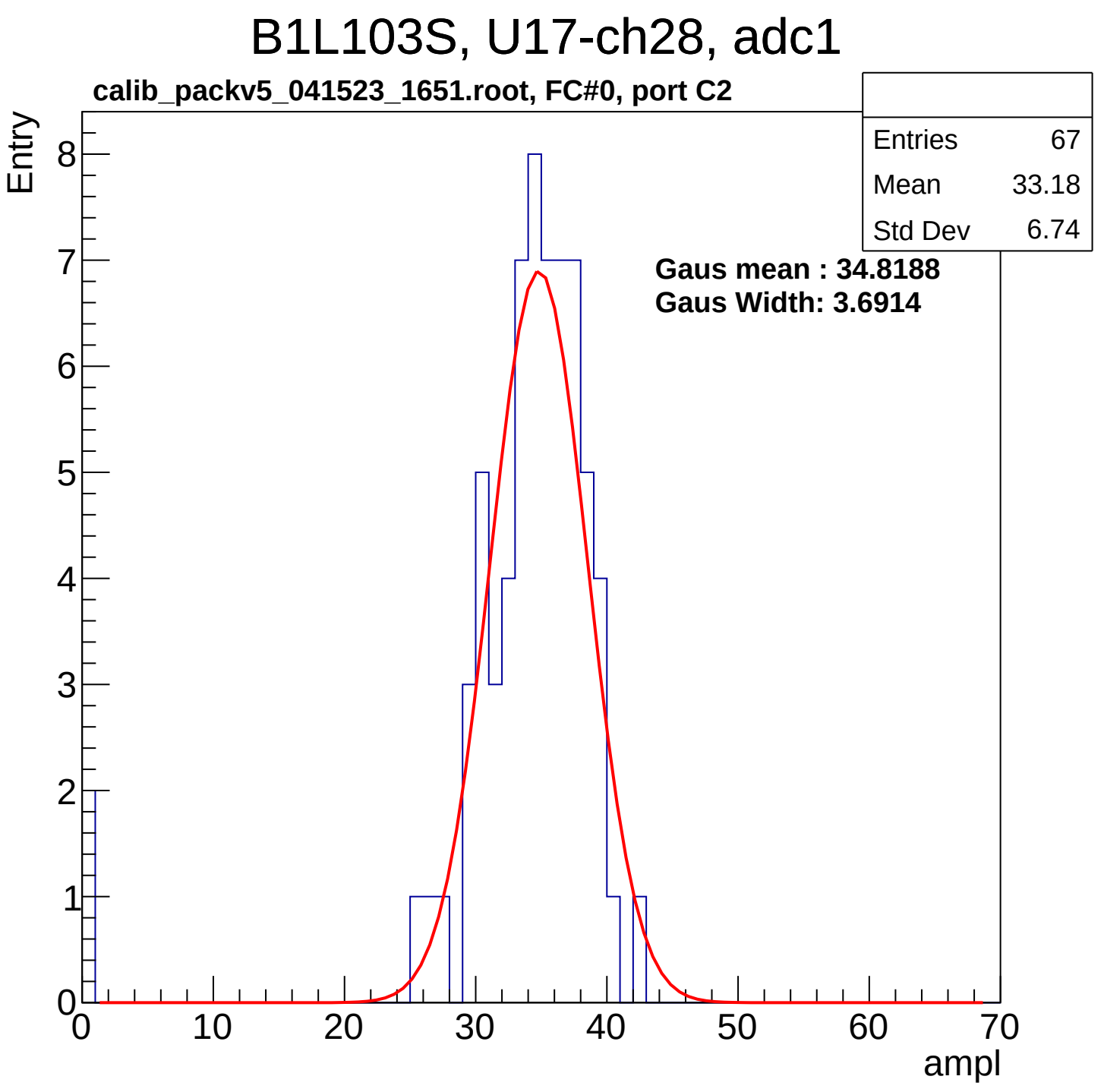

B1L103S, U17-ch27, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.49
Std Dev 3.061
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

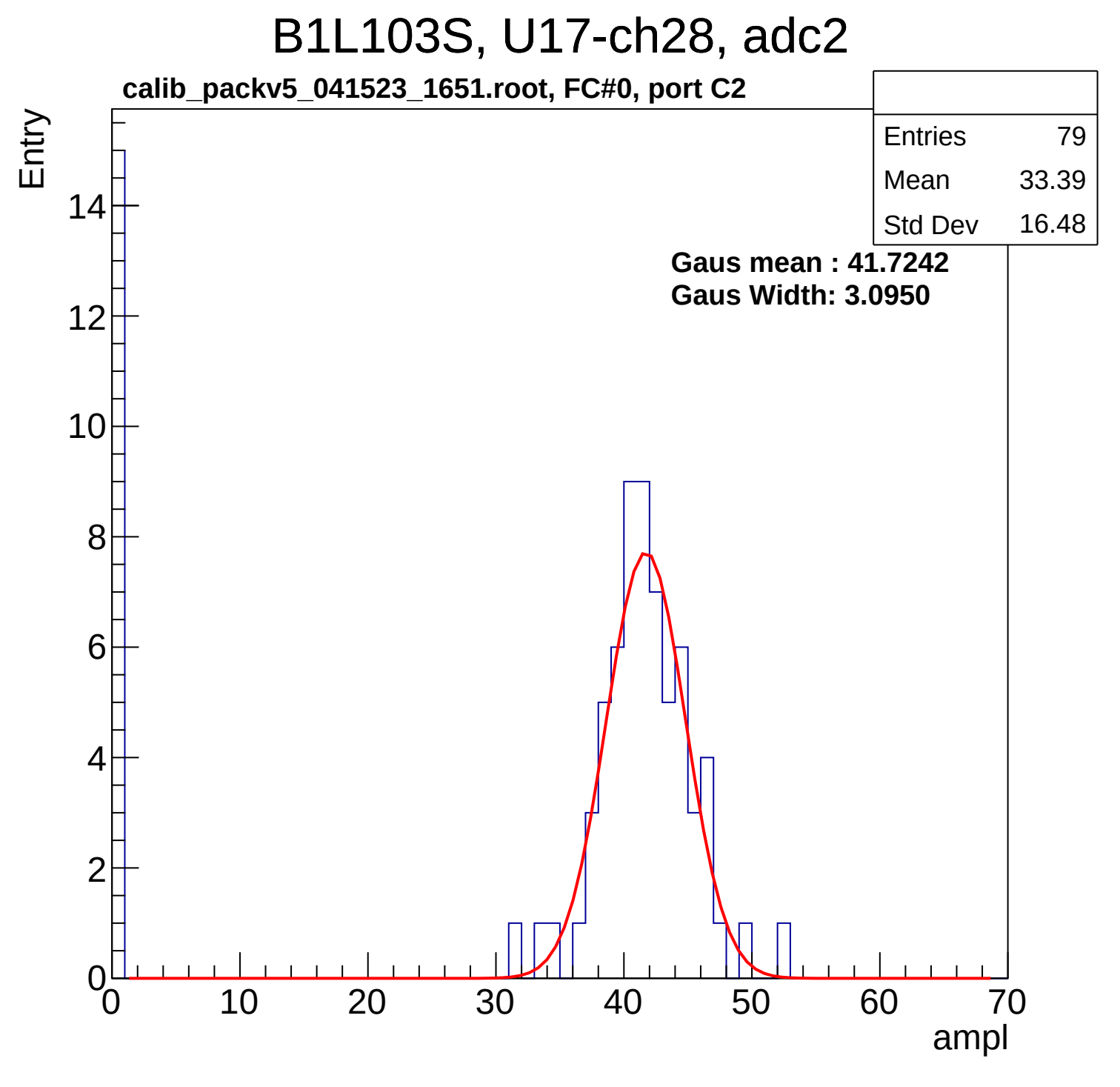

B1L103S, U17-ch27, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.74
Std Dev 8.168
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

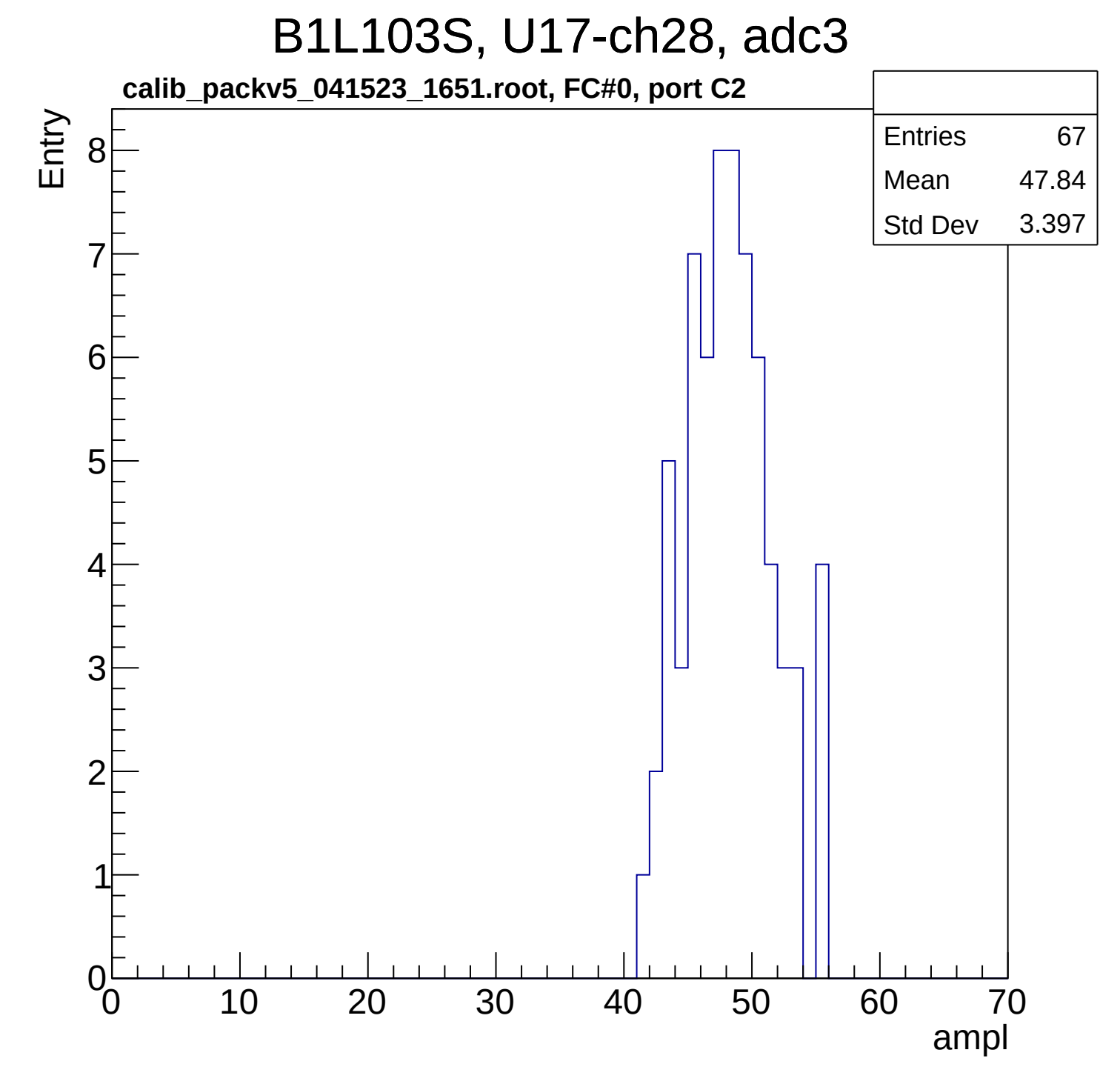

B1L103S, U17-ch27, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

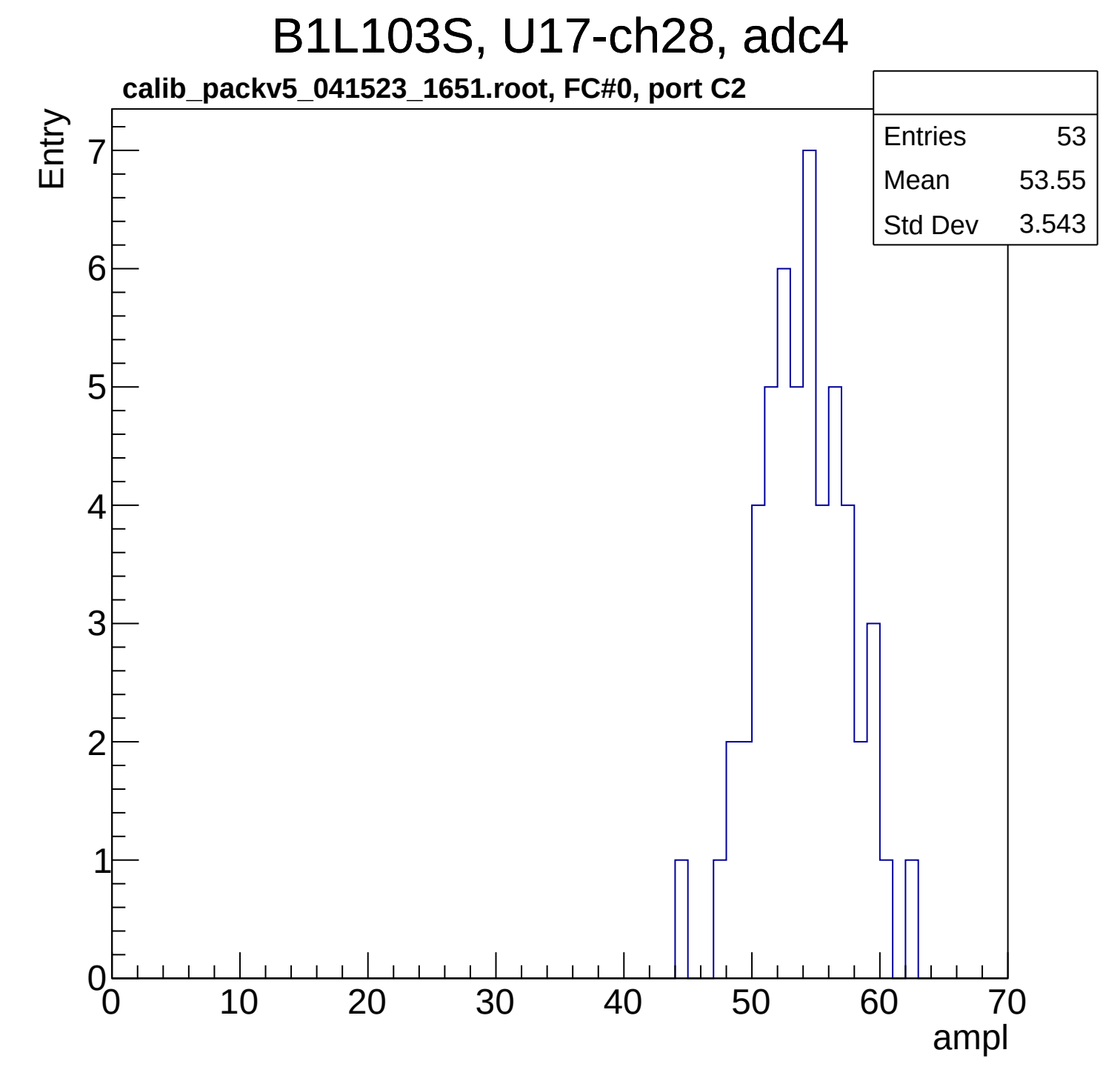

B1L103S, U17-ch27, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

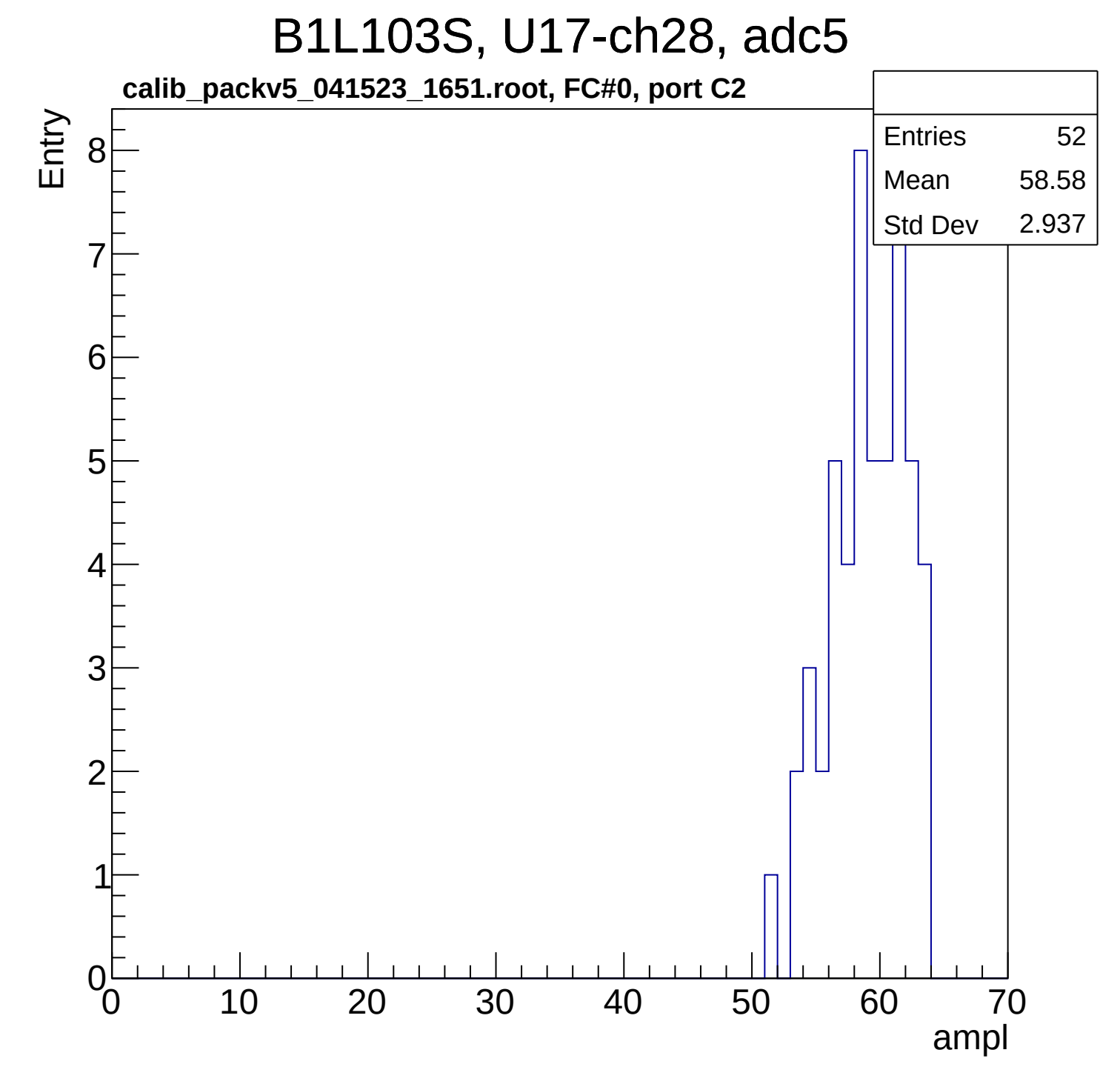

B1L103S, U17-ch28, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 24.35
Std Dev 10.01
Gaus mean : 27.7518
Gaus Width: 4.1234
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

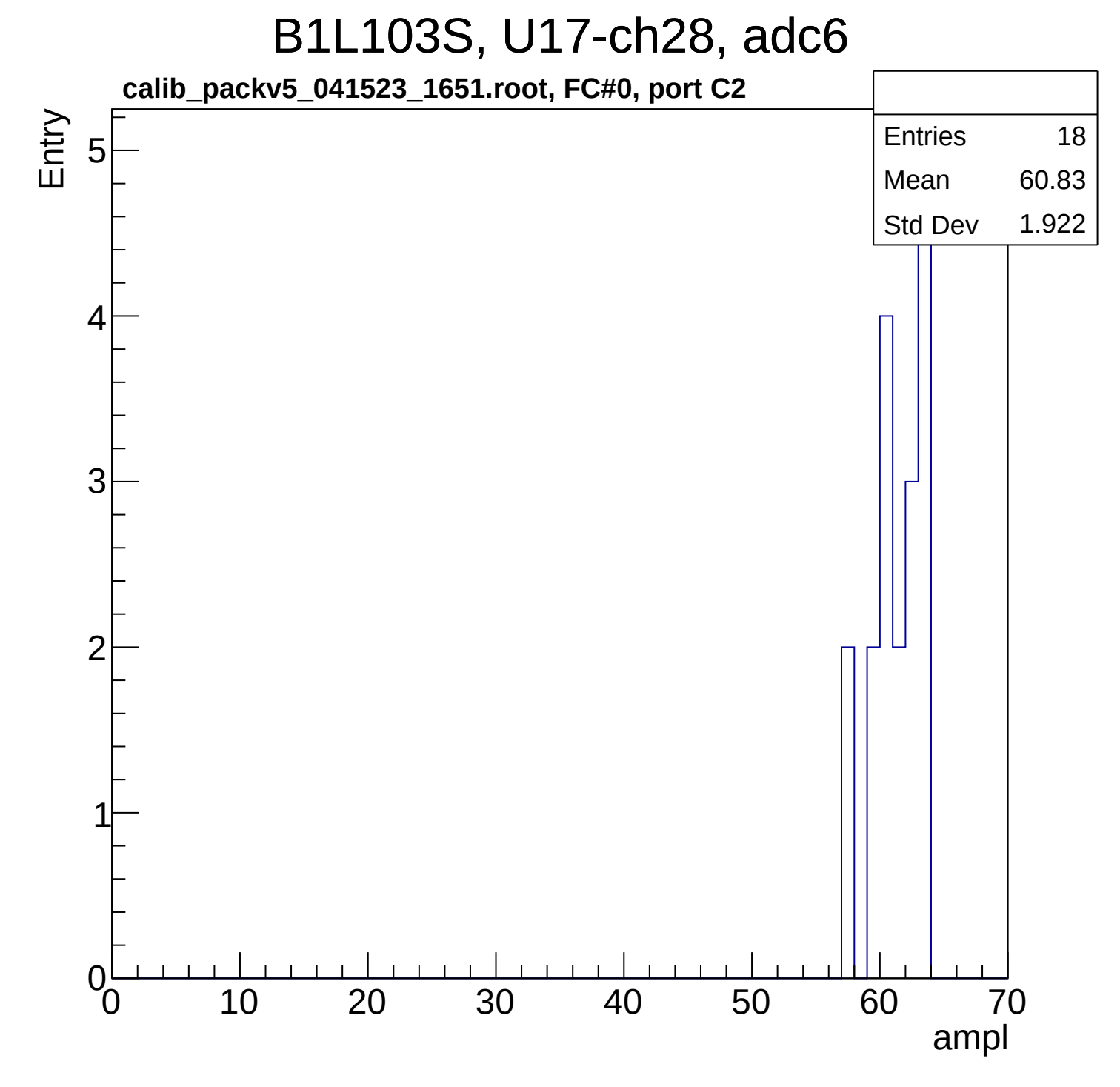

B1L103S, U17-ch28, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 33.18
Std Dev 6.74
Gaus mean : 34.8188
Gaus Width: 3.6914
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

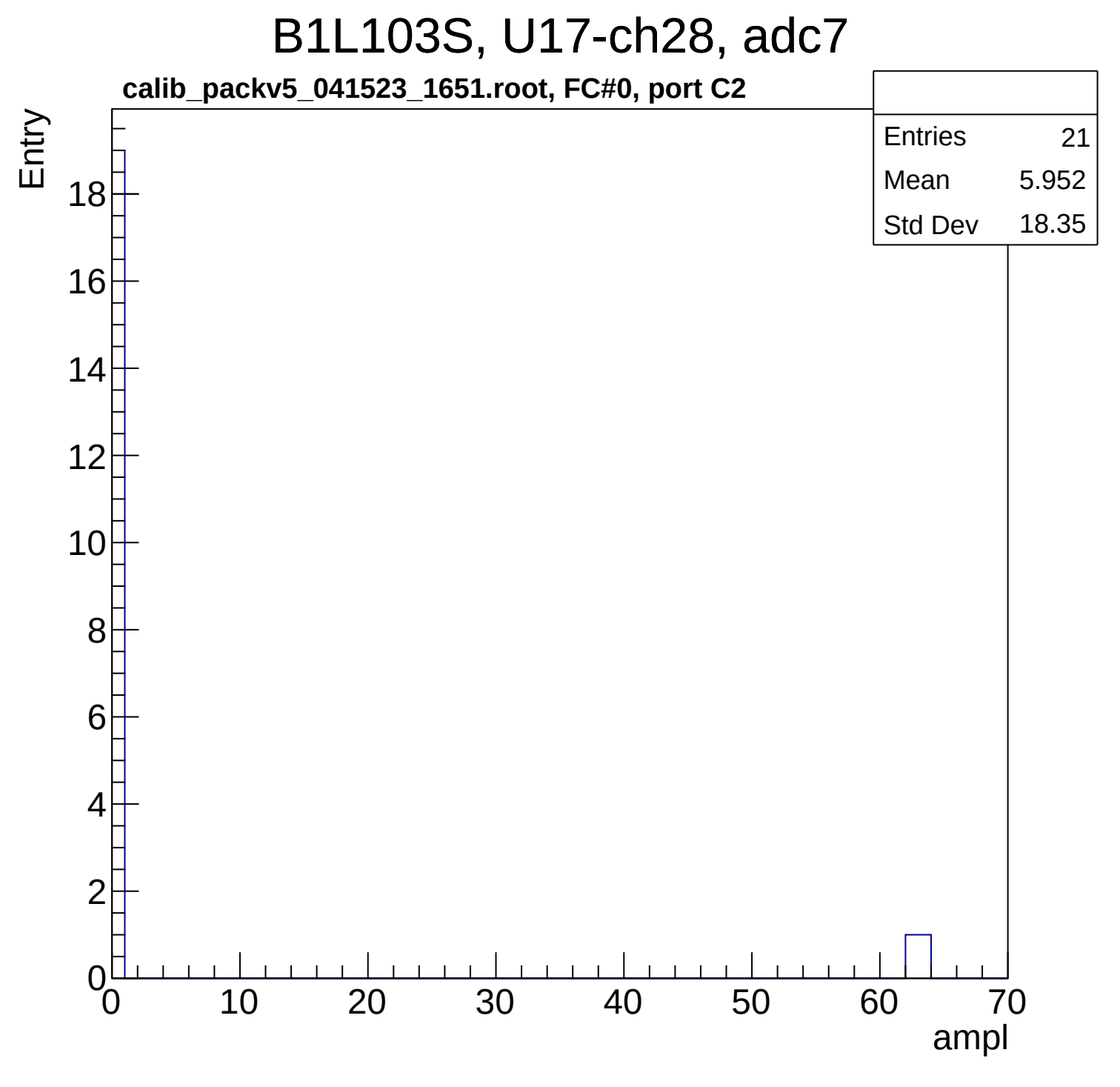

B1L103S, U17-ch28, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 33.39
Std Dev 16.48
Gaus mean : 41.7242
Gaus Width: 3.0950
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

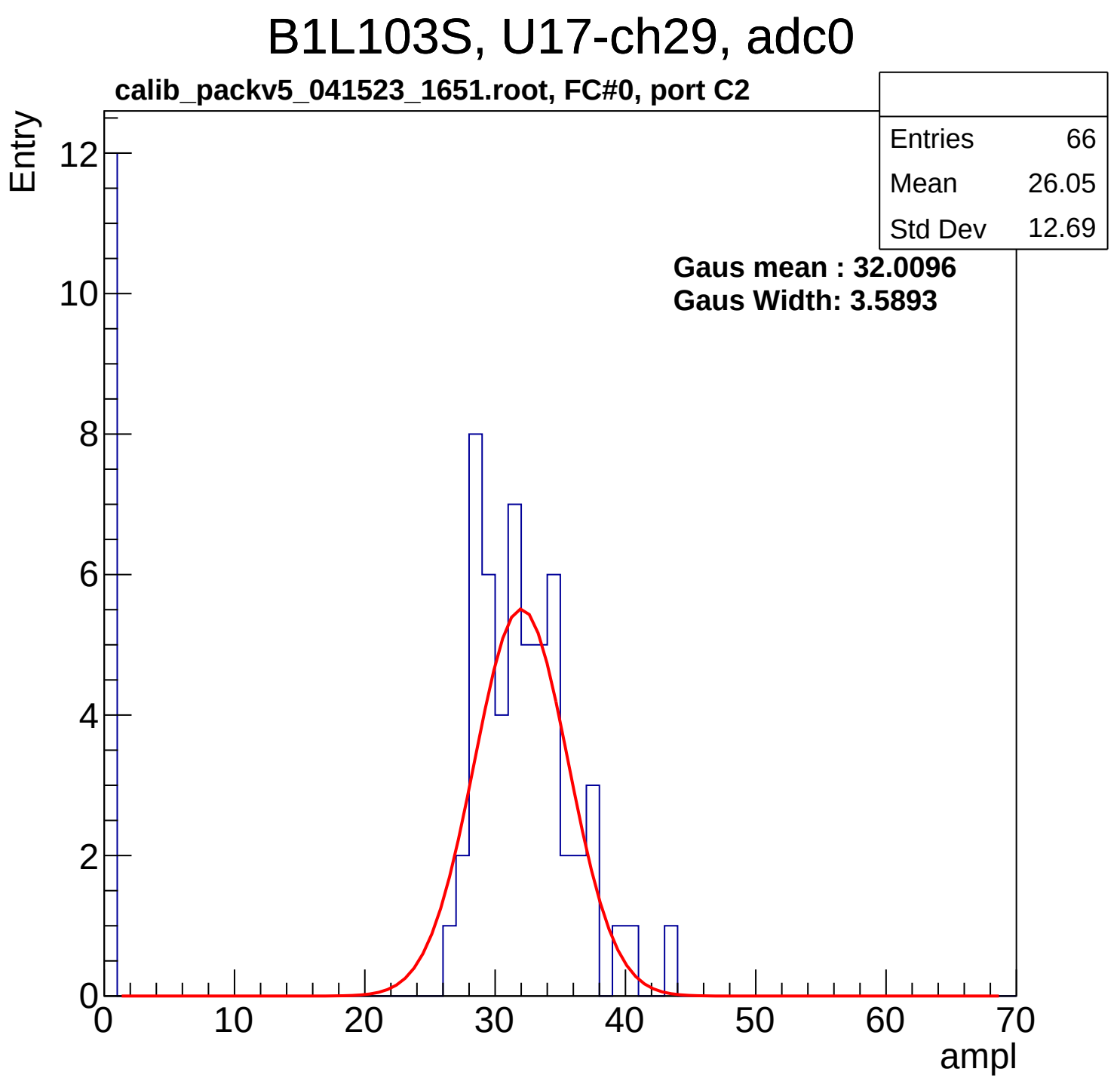

B1L103S, U17-ch28, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 47.84
Std Dev 3.397
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

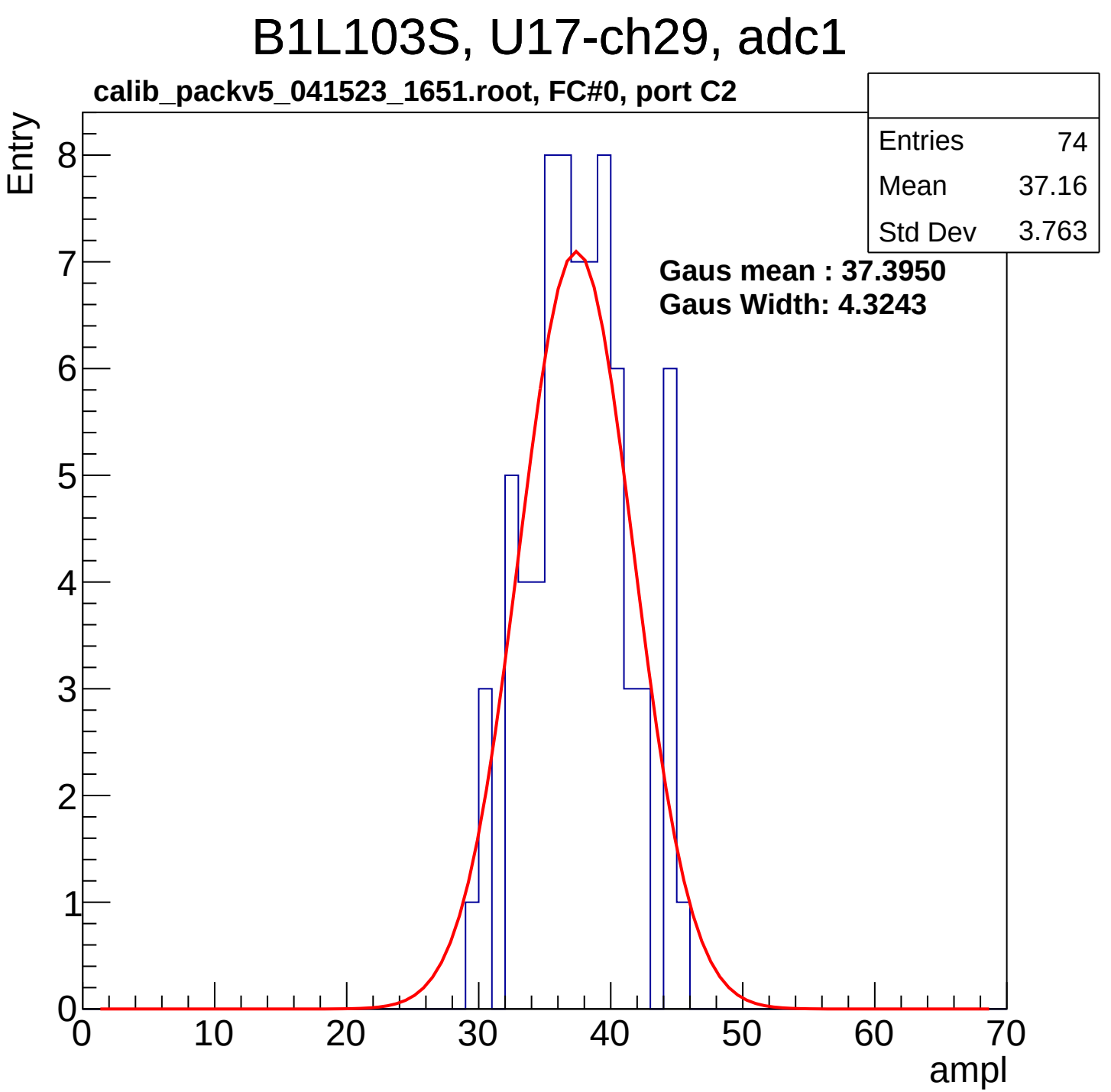

B1L103S, U17-ch28, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 53.55
Std Dev 3.543
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

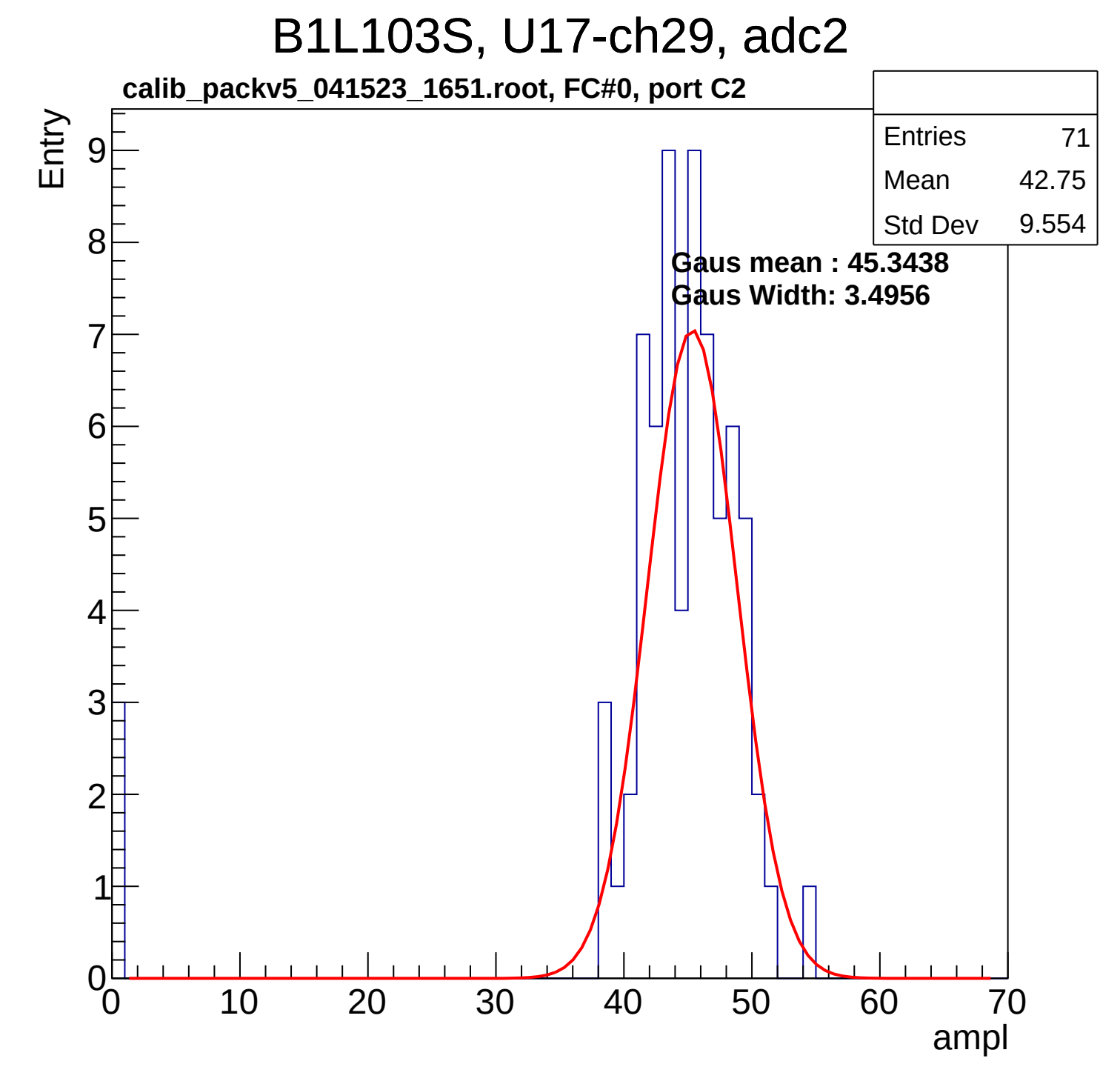

B1L103S, U17-ch28, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.58
Std Dev 2.937
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

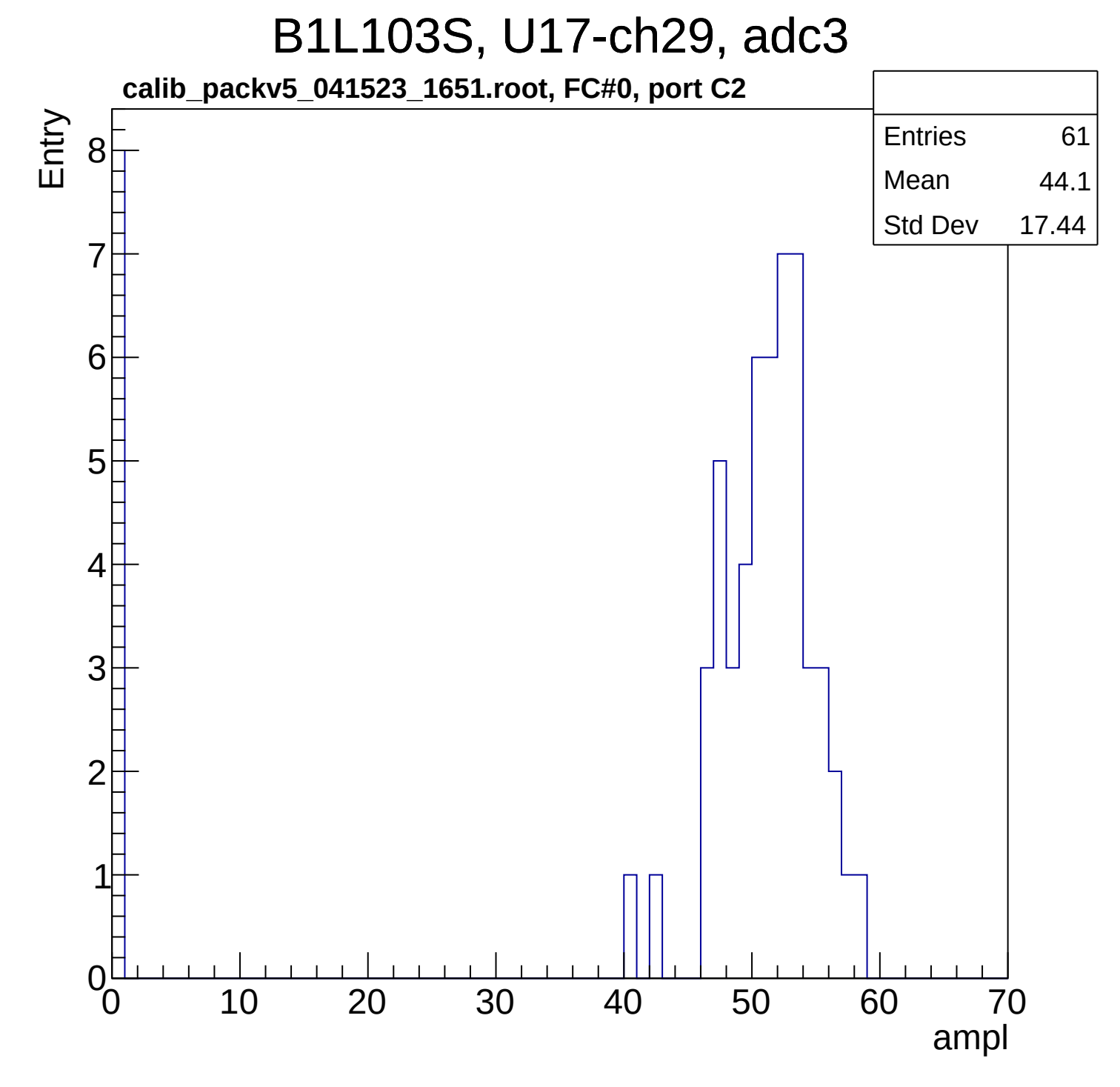

B1L103S, U17-ch28, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 60.83
Std Dev 1.922
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

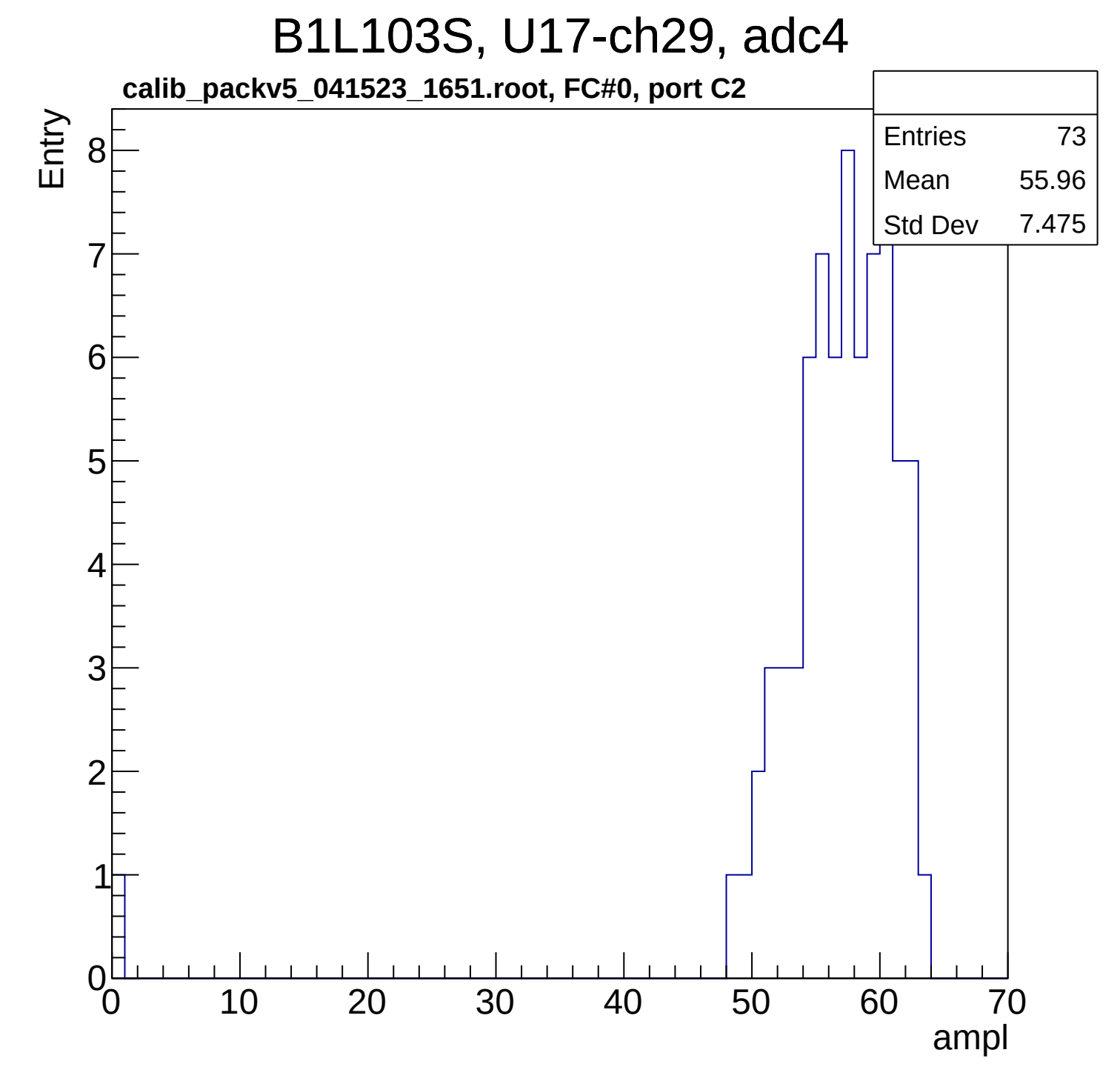

B1L103S, U17-ch28, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

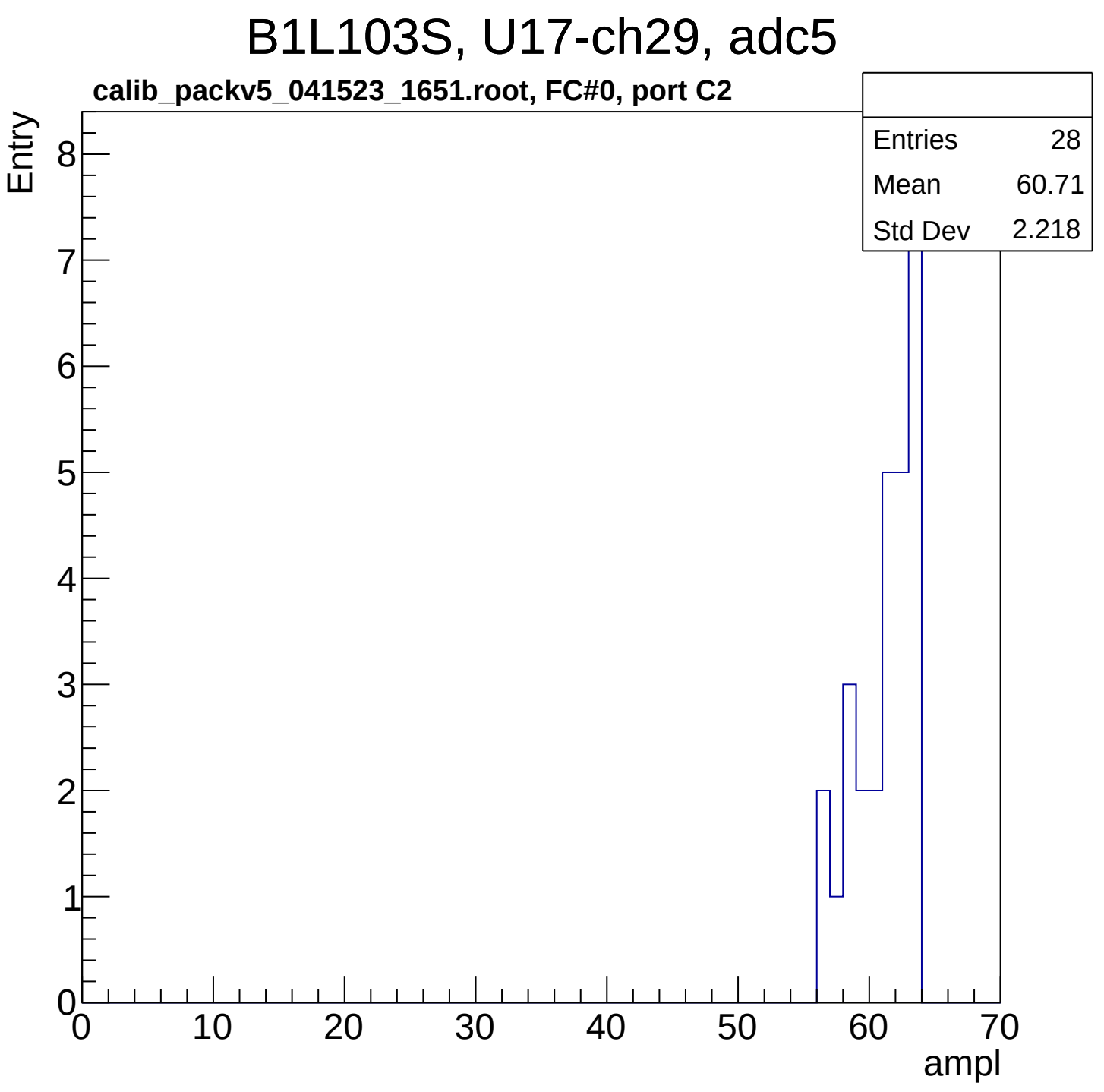

B1L103S, U17-ch29, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 26.05
Std Dev 12.69
Gaus mean : 32.0096
Gaus Width: 3.5893
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

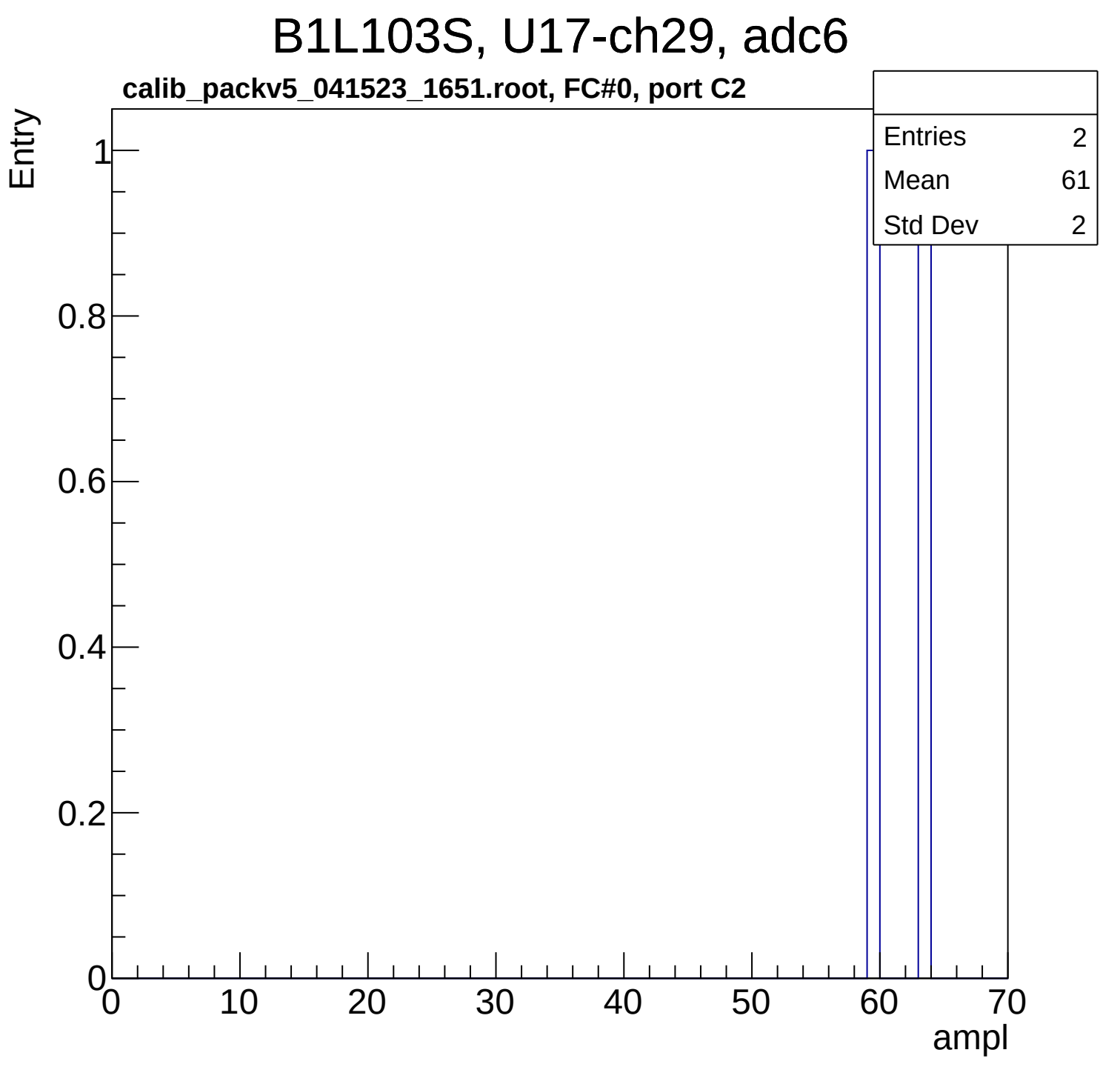

B1L103S, U17-ch29, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 37.16
Std Dev 3.763
Gaus mean : 37.3950
Gaus Width: 4.3243
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

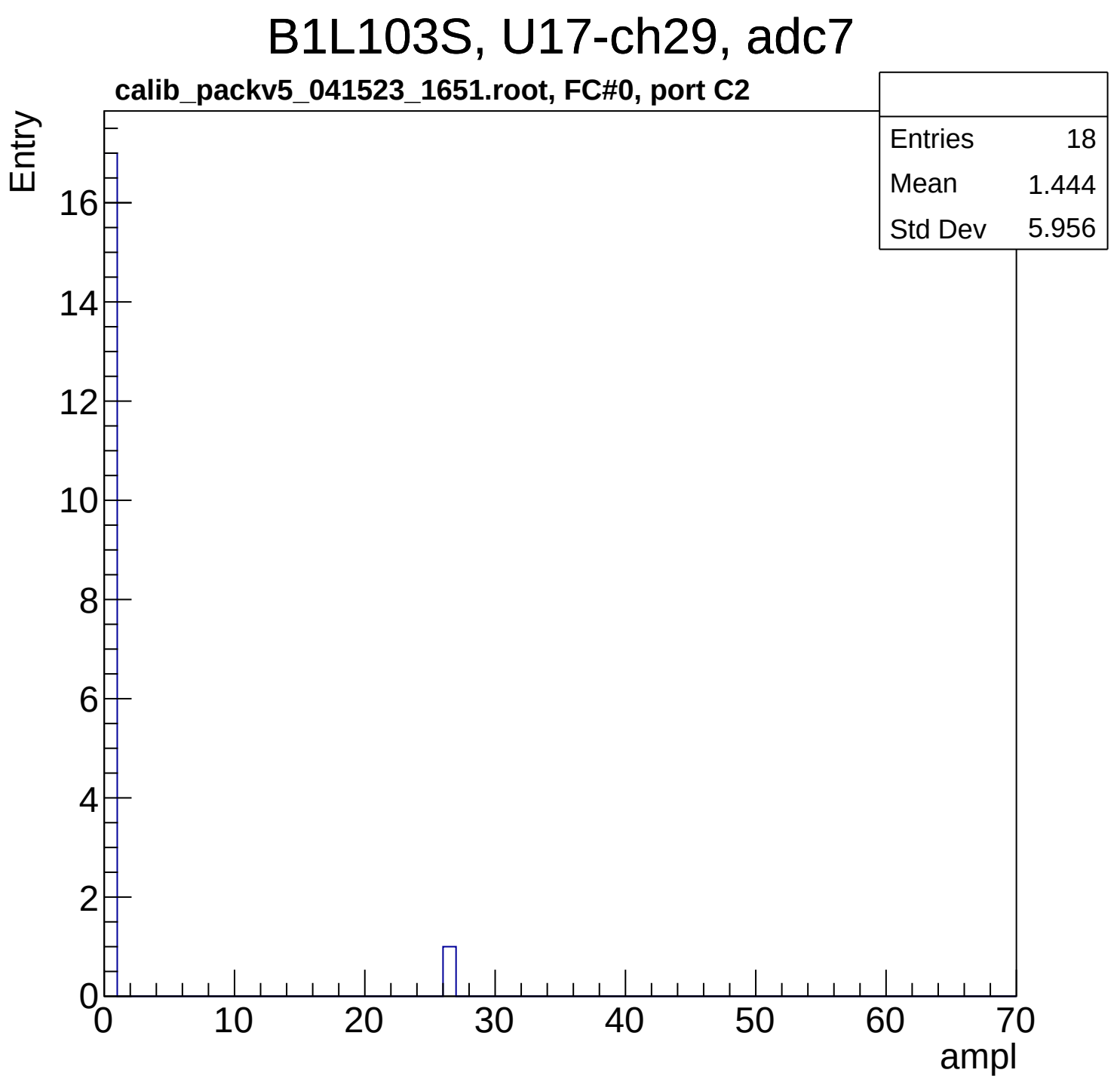

B1L103S, U17-ch29, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 42.75
Std Dev 9.554
Gaus mean : 45.3438
Gaus Width: 3.4956
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

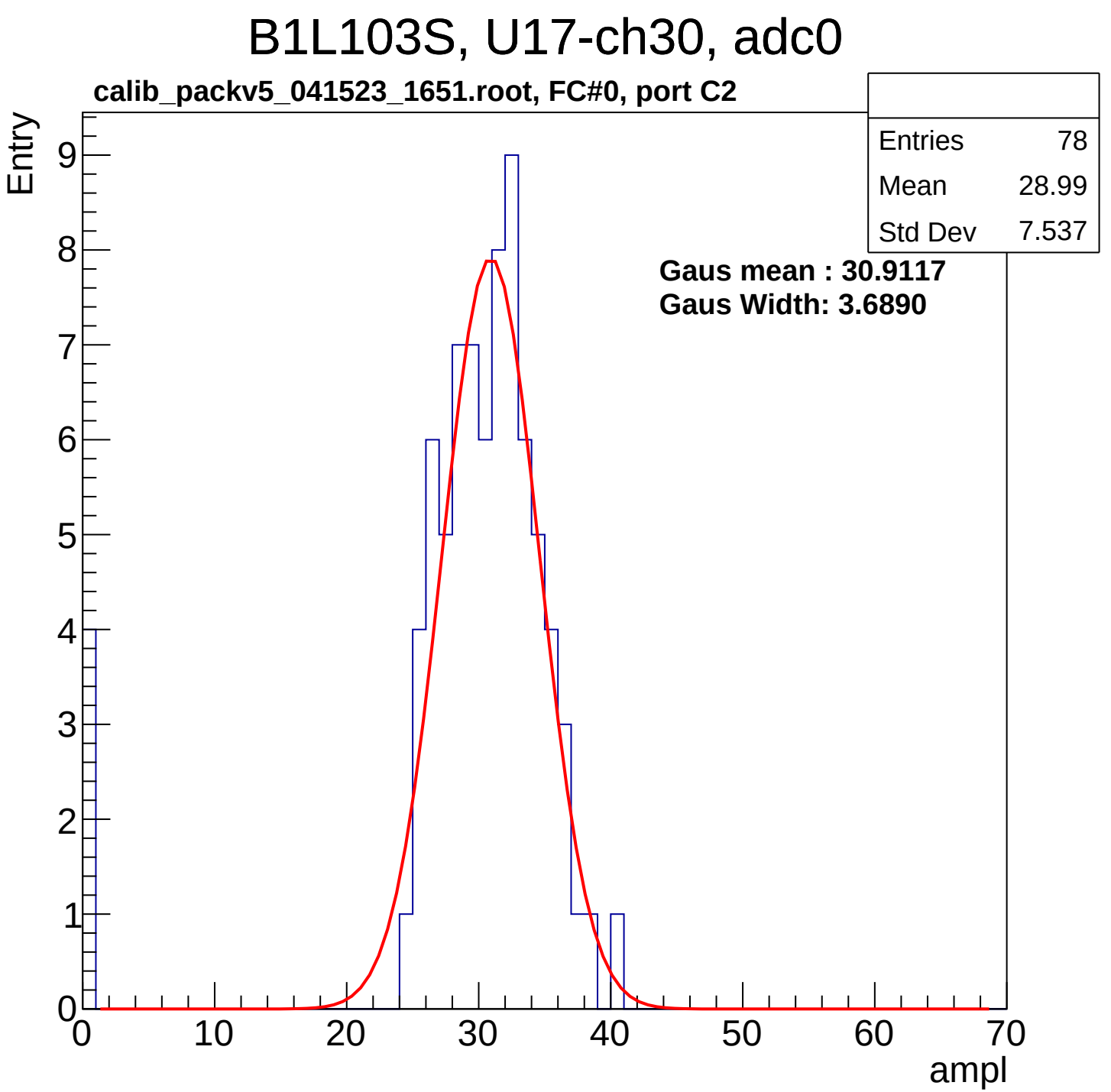

B1L103S, U17-ch29, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 44.1
Std Dev 17.44
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

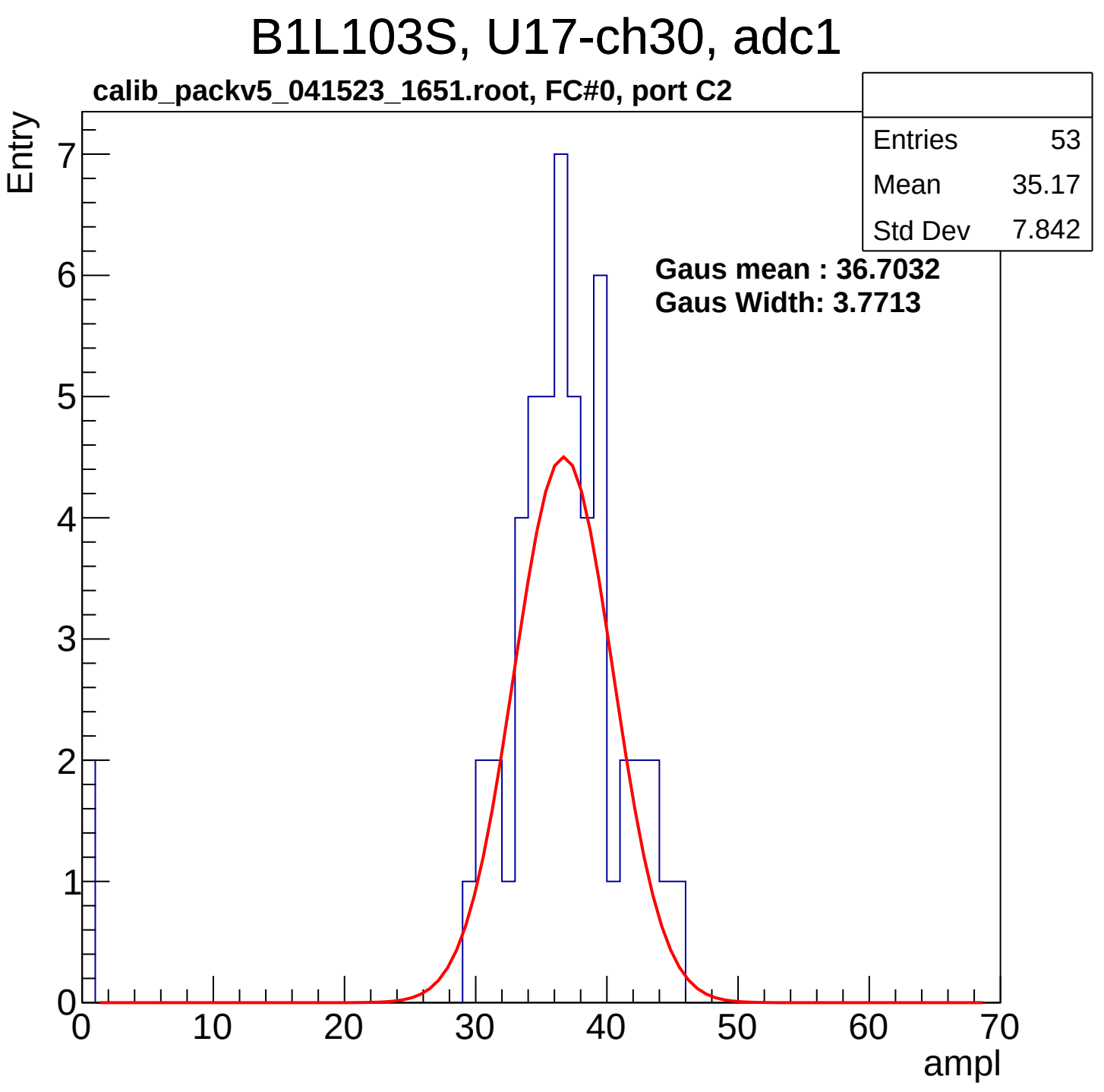

B1L103S, U17-ch29, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 55.96
Std Dev 7.475
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

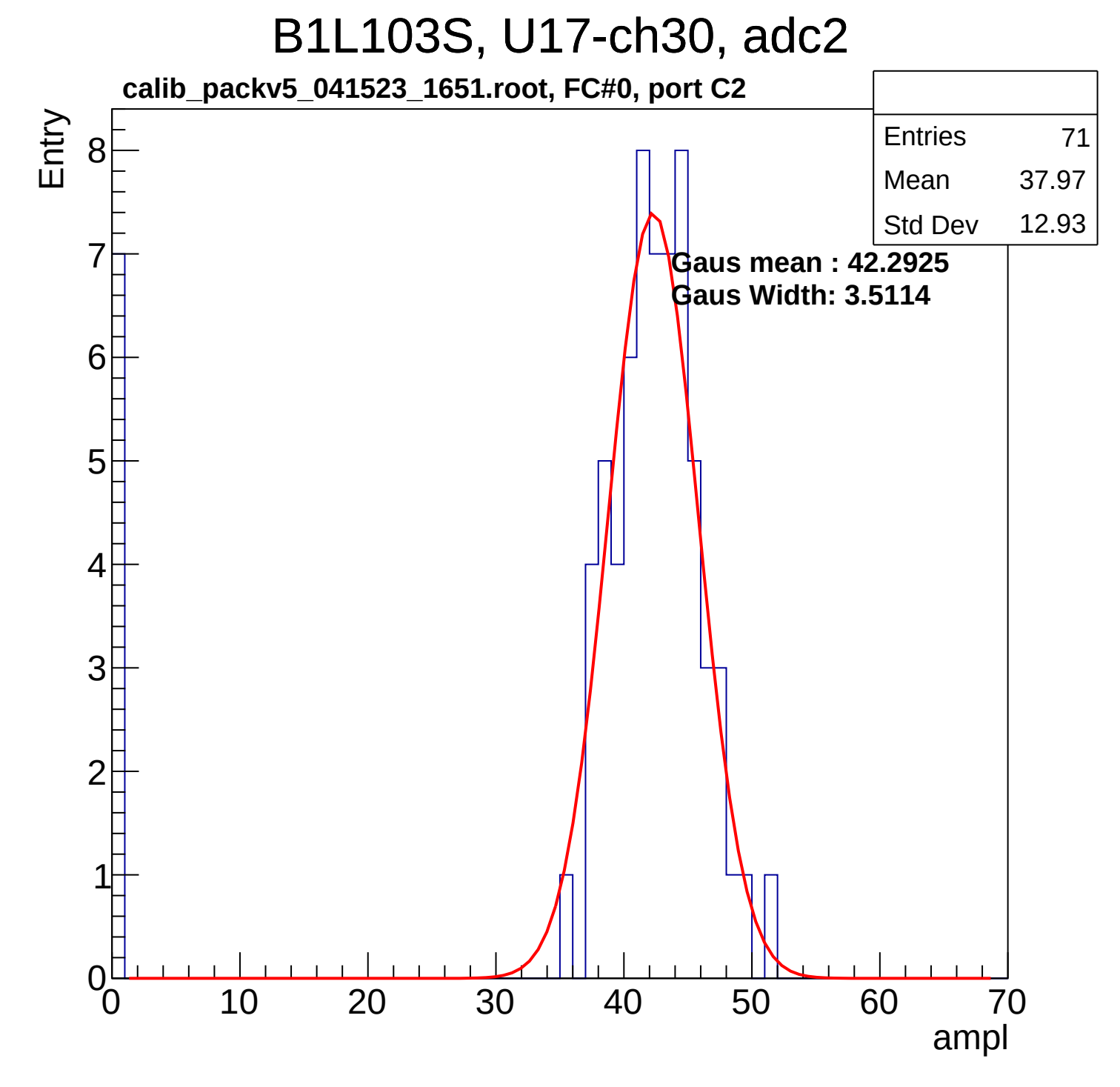

B1L103S, U17-ch29, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 60.71
Std Dev 2.218
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

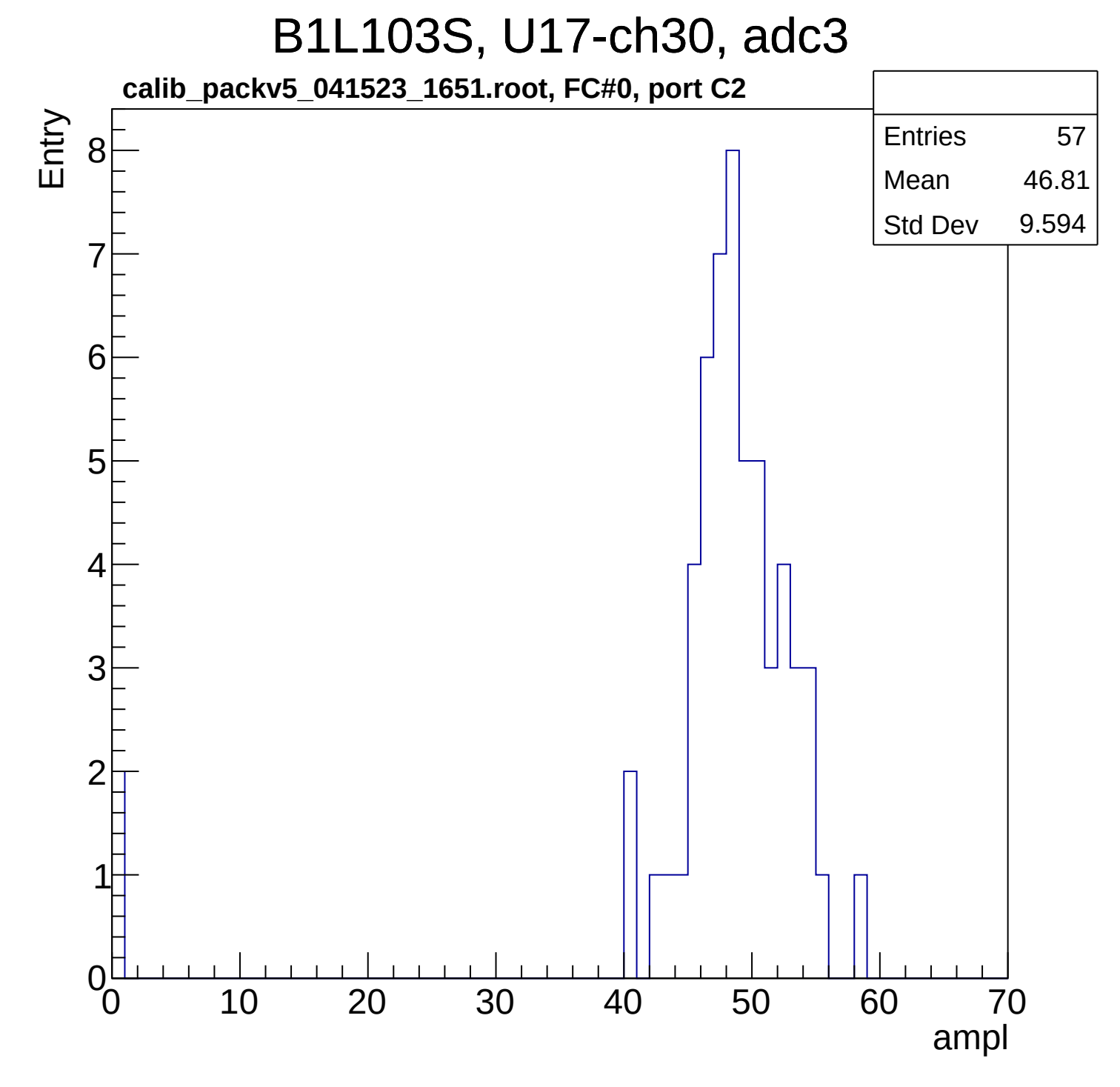

B1L103S, U17-ch29, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 61
Std Dev 2
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

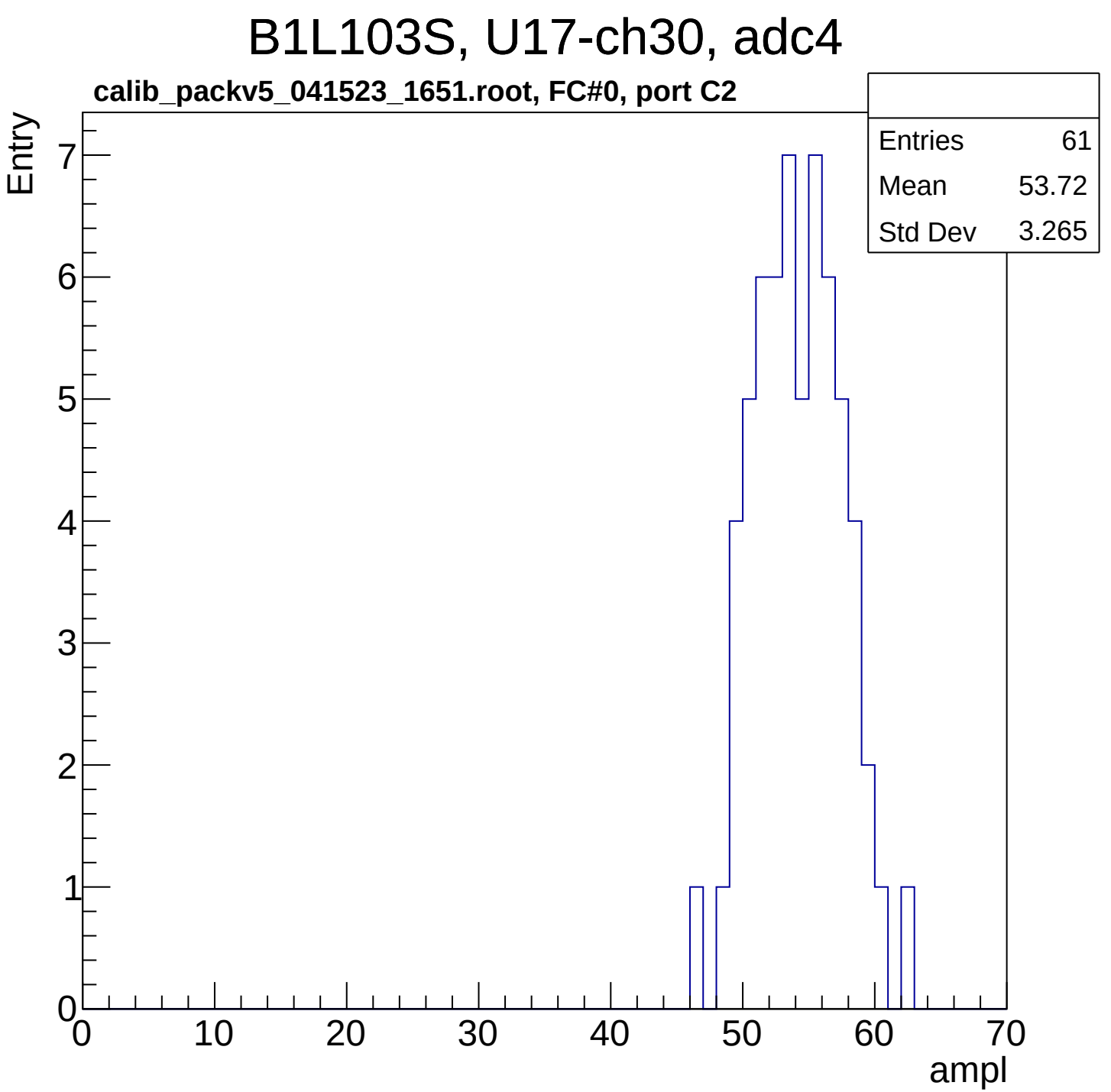

B1L103S, U17-ch29, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.444
Std Dev 5.956
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

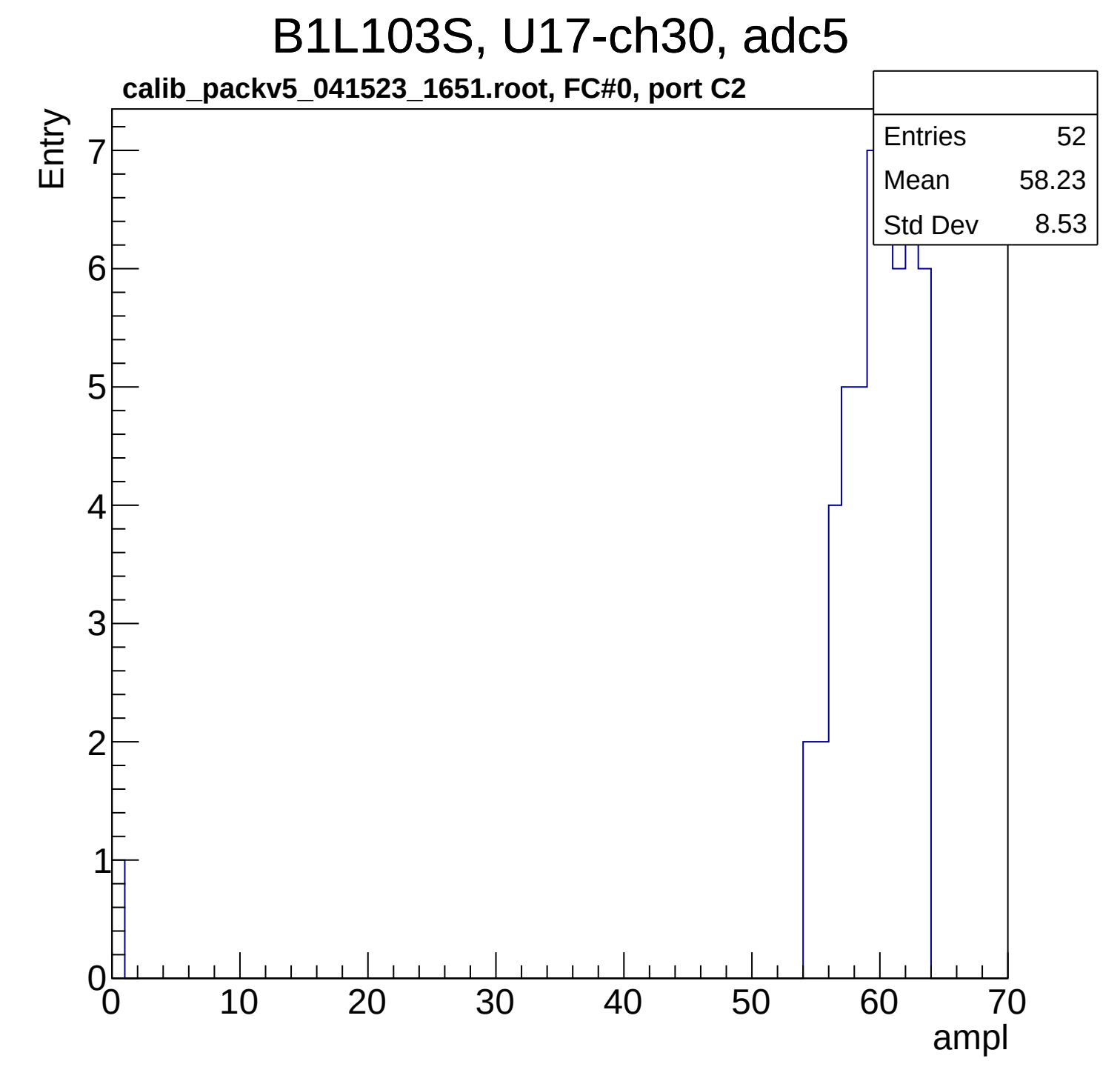

B1L103S, U17-ch30, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 28.99
Std Dev 7.537
Gaus mean : 30.9117
Gaus Width: 3.6890
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

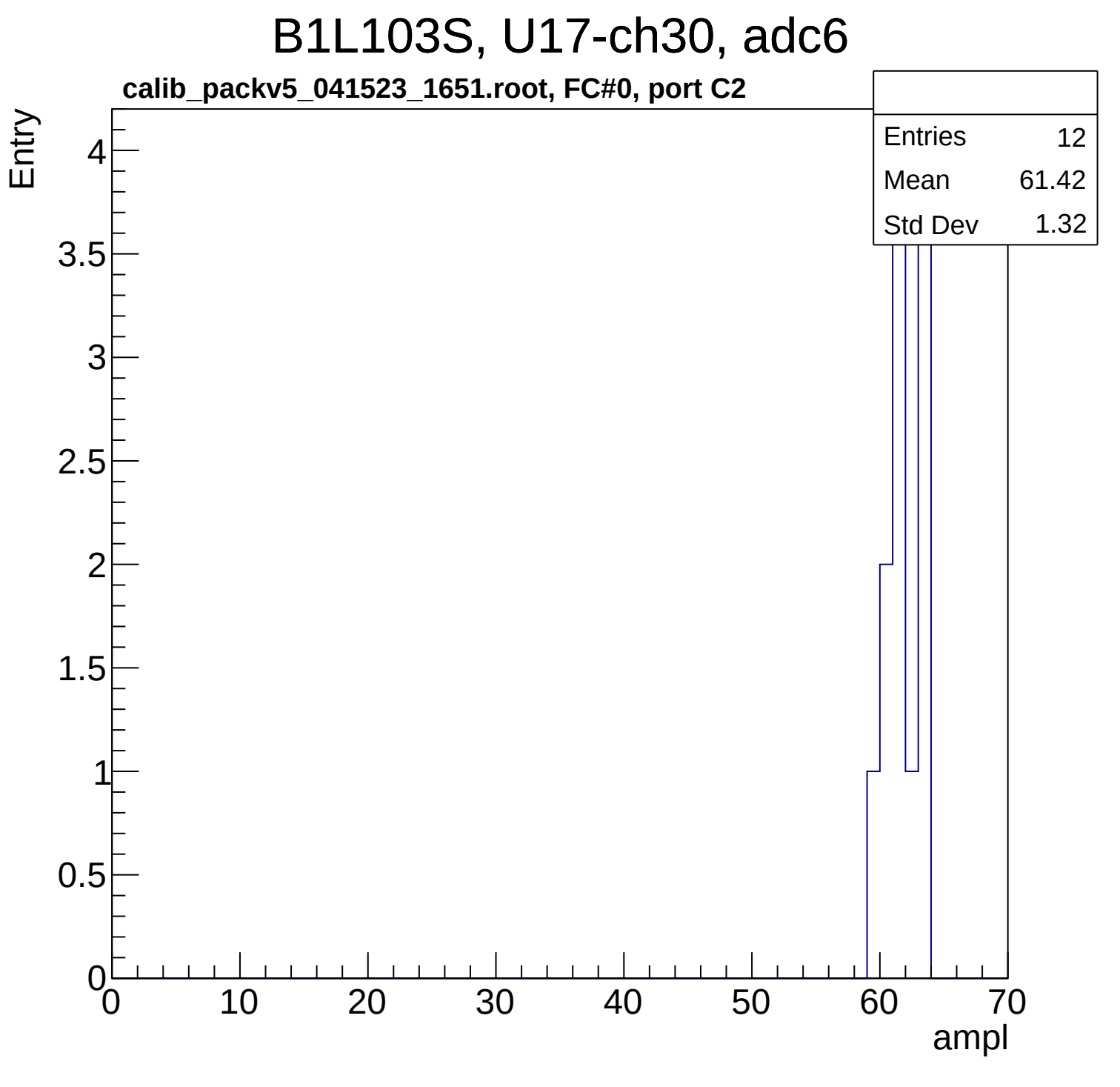

B1L103S, U17-ch30, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 35.17
Std Dev 7.842
Gaus mean : 36.7032
Gaus Width: 3.7713
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

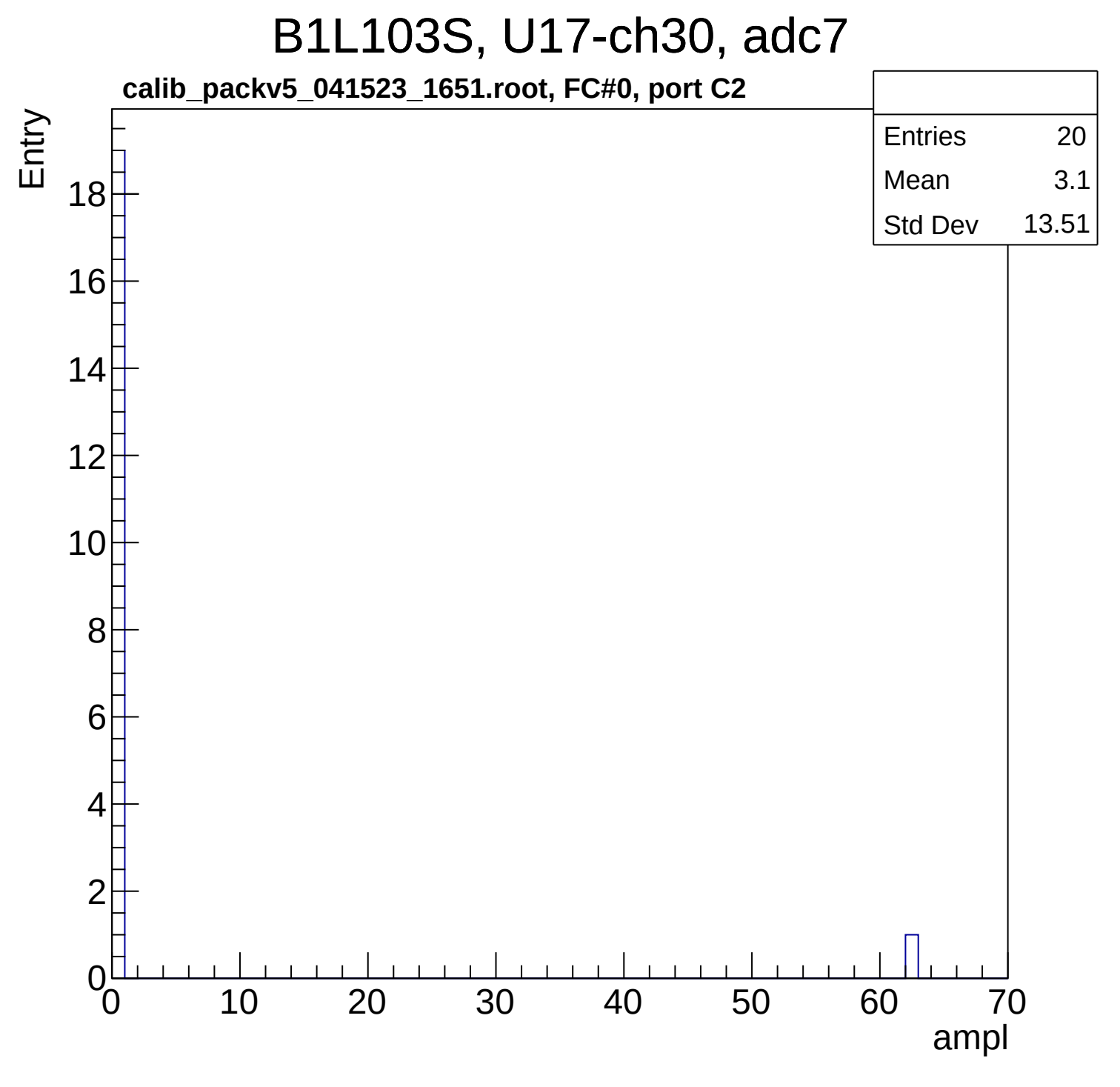

B1L103S, U17-ch30, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 37.97
Std Dev 12.93
Gaus mean : 42.2925
Gaus Width: 3.5114
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

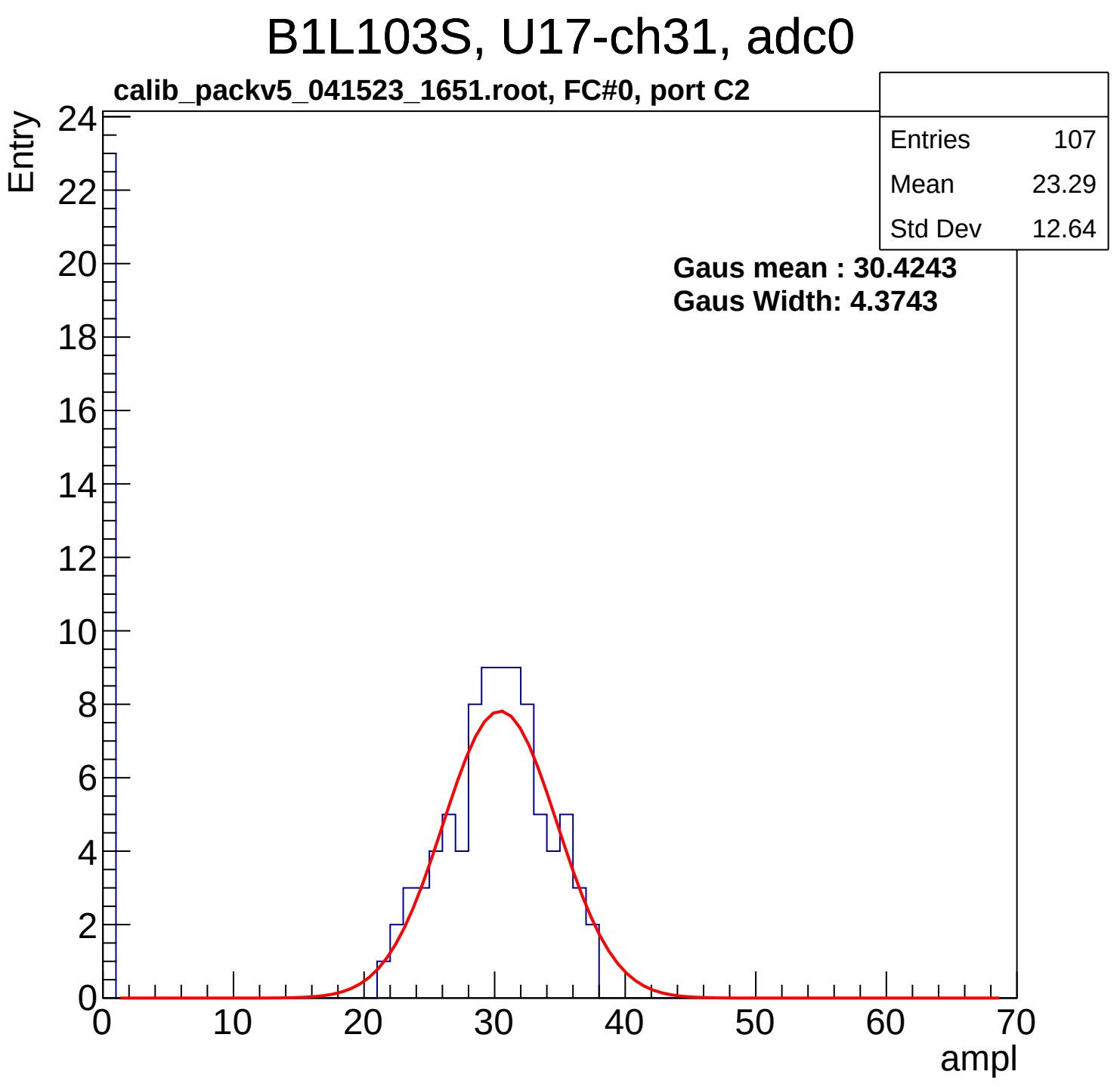

B1L103S, U17-ch30, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 46.81
Std Dev 9.594
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

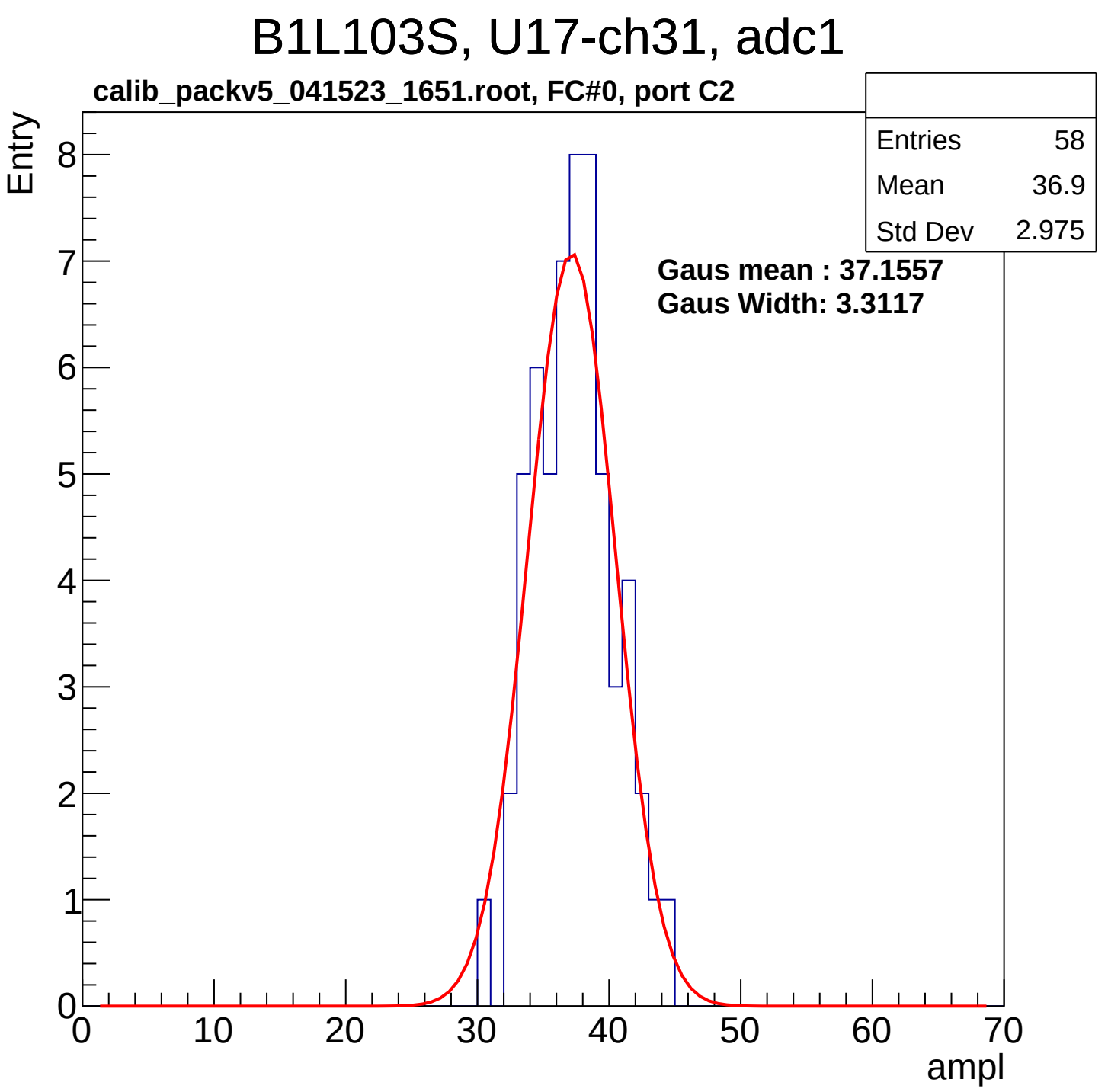

B1L103S, U17-ch30, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 53.72
Std Dev 3.265
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

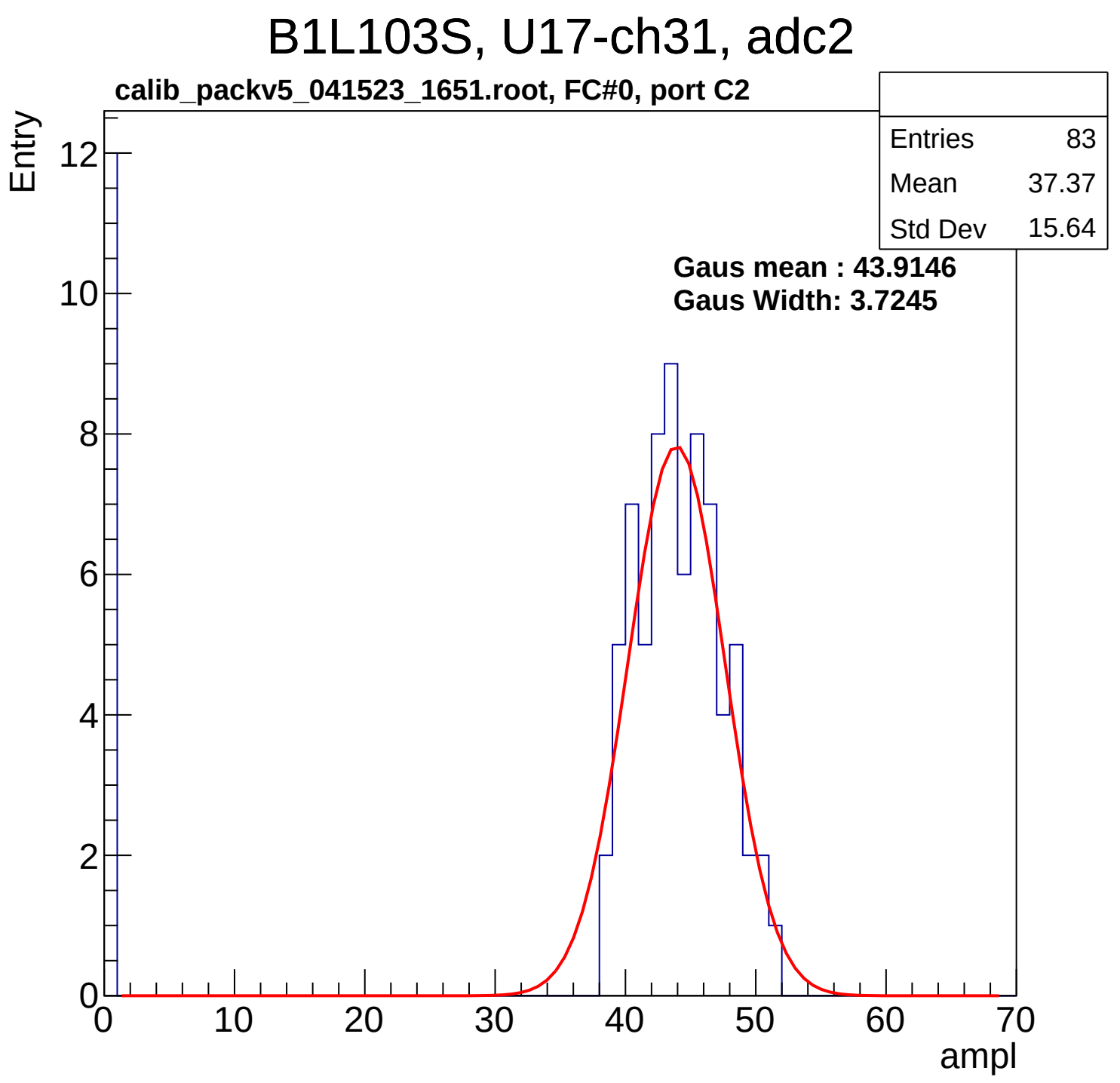

B1L103S, U17-ch30, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.23
Std Dev 8.53
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

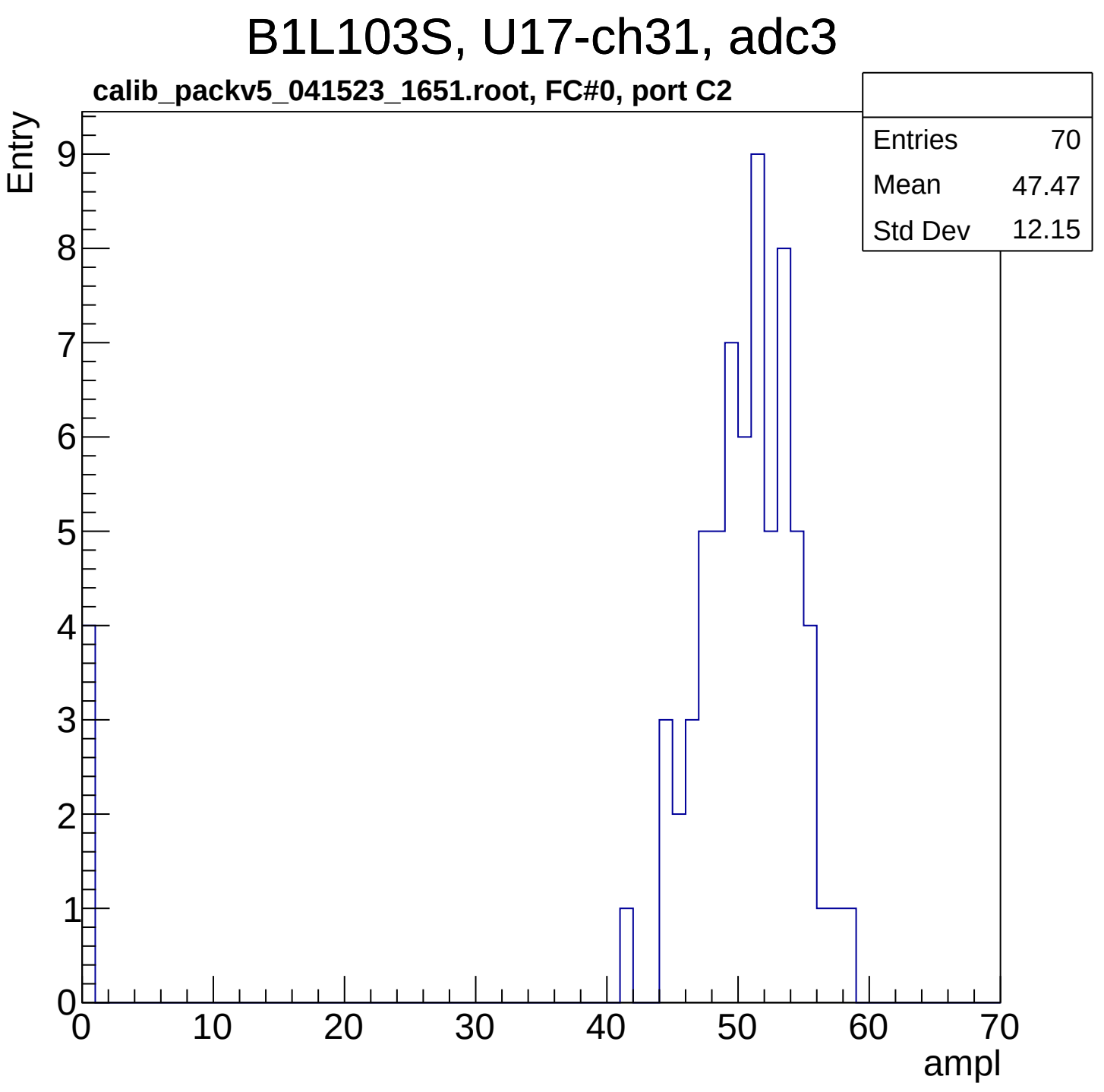

B1L103S, U17-ch30, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.42
Std Dev 1.32
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

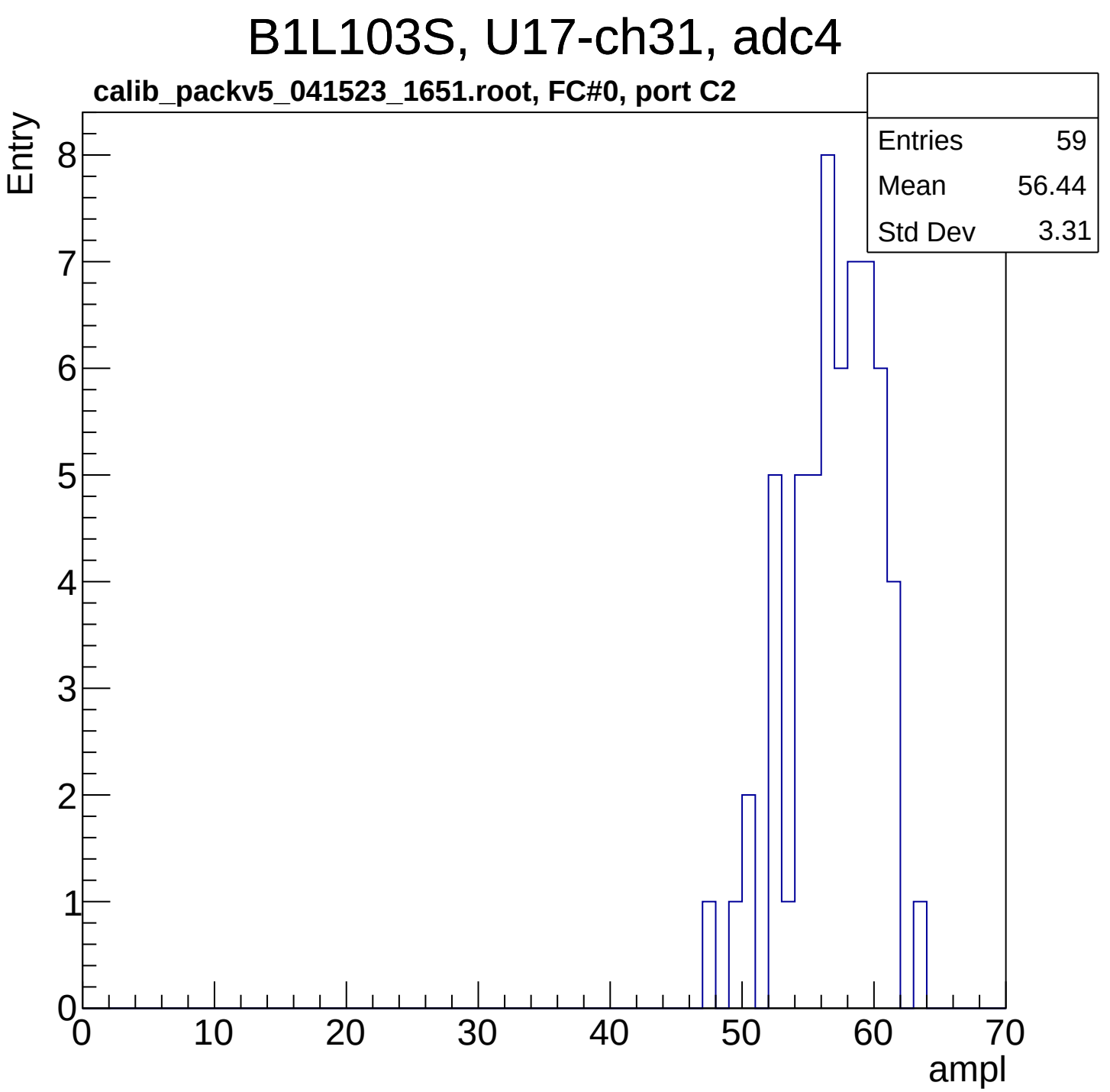

B1L103S, U17-ch30, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

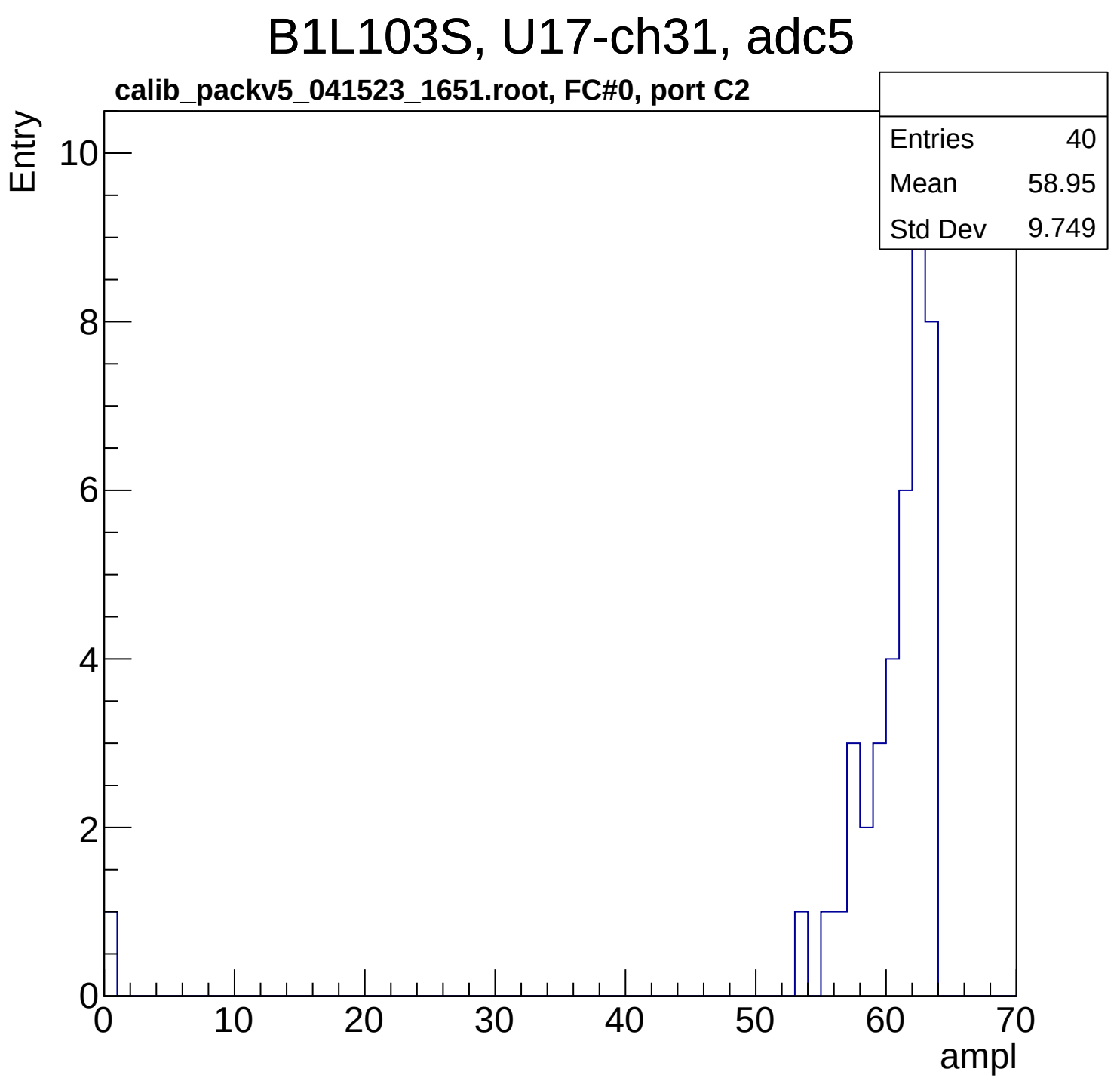

B1L103S, U17-ch31, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 107
Mean 23.29
Std Dev 12.64
Gaus mean : 30.4243
Gaus Width: 4.3743
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70

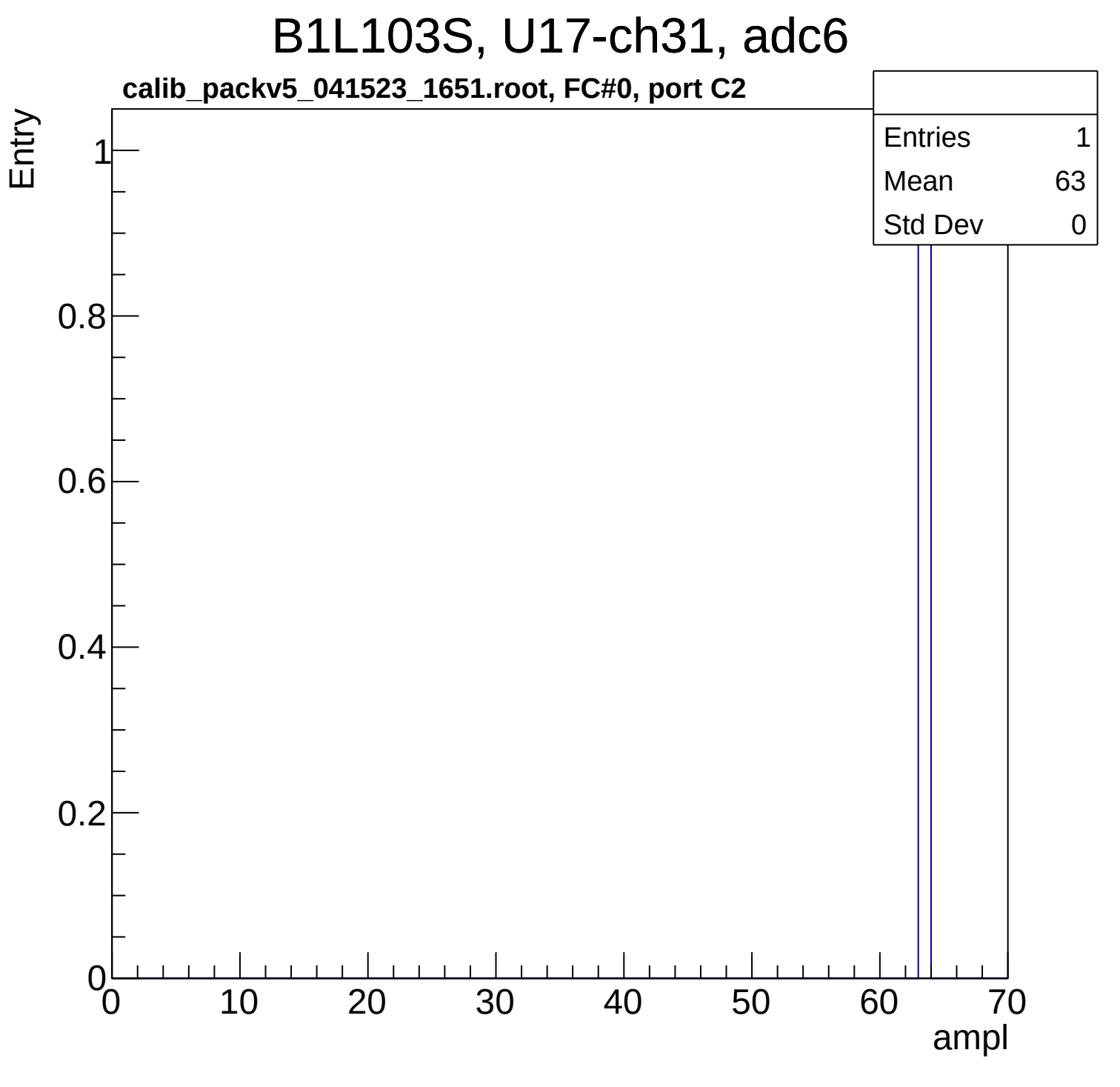

B1L103S, U17-ch31, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 36.9
Std Dev 2.975
Gaus mean : 37.1557
Gaus Width: 3.3117
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

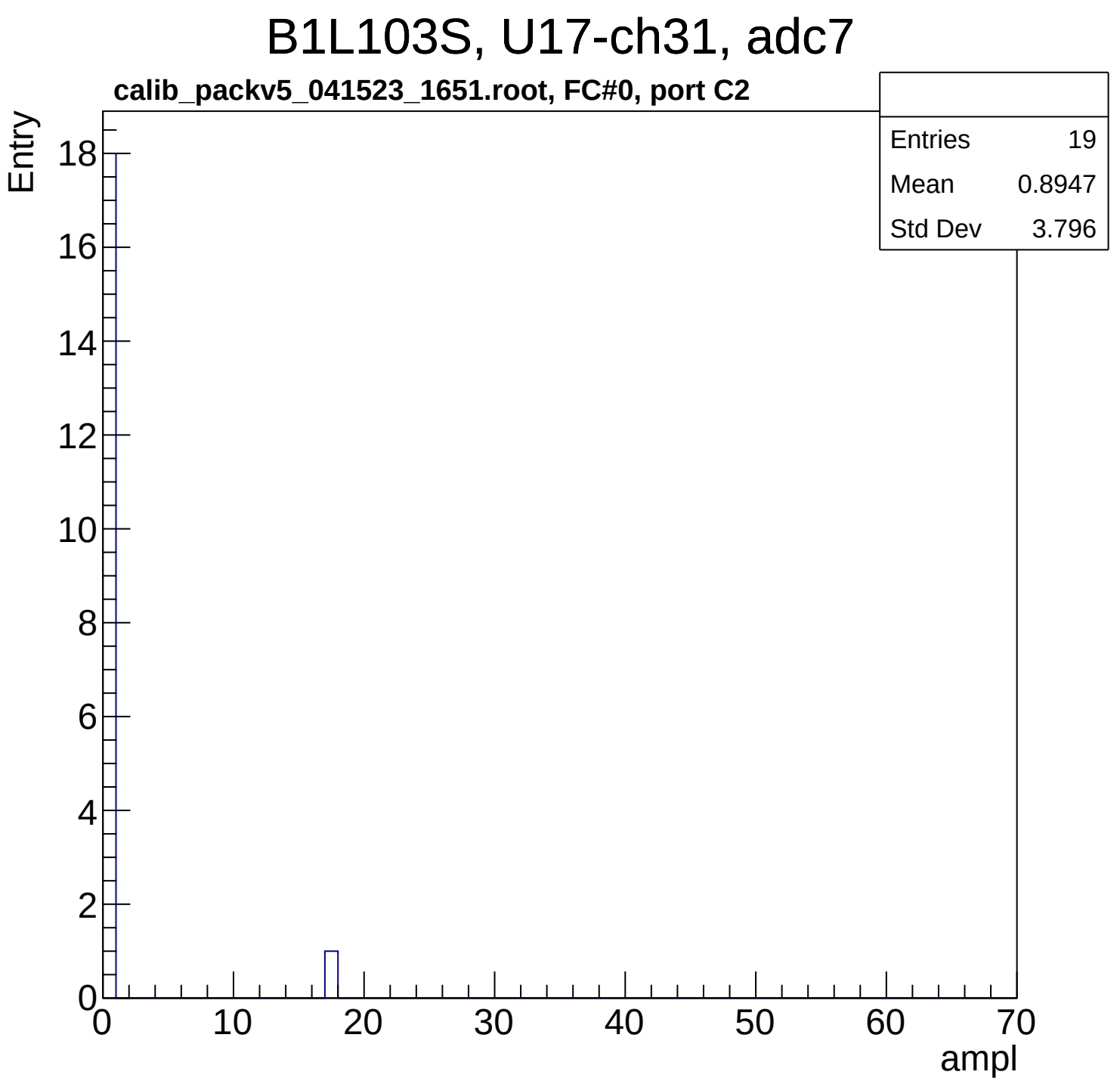

B1L103S, U17-ch31, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 37.37
Std Dev 15.64
Gaus mean : 43.9146
Gaus Width: 3.7245
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

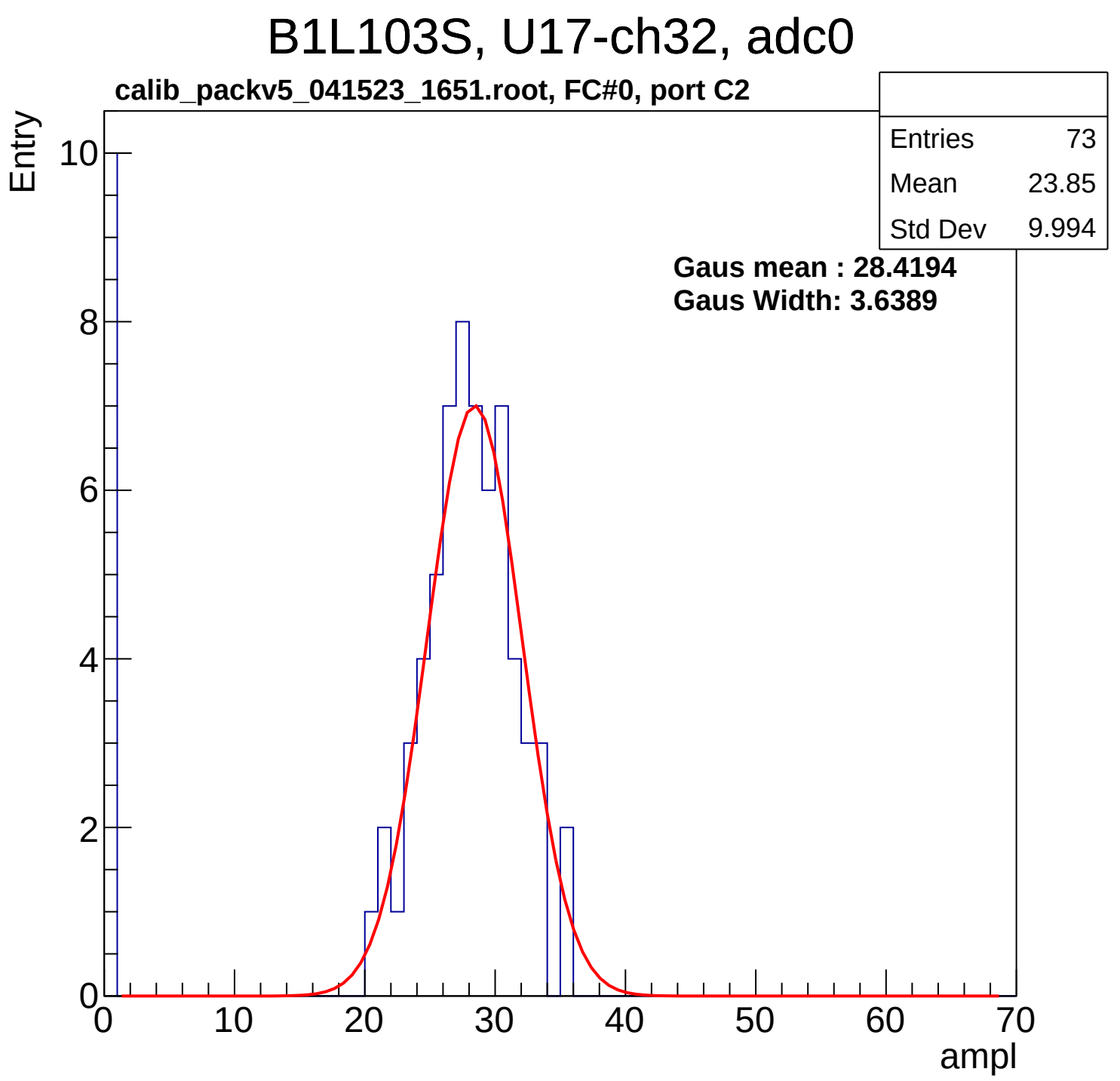

B1L103S, U17-ch31, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 47.47
Std Dev 12.15
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

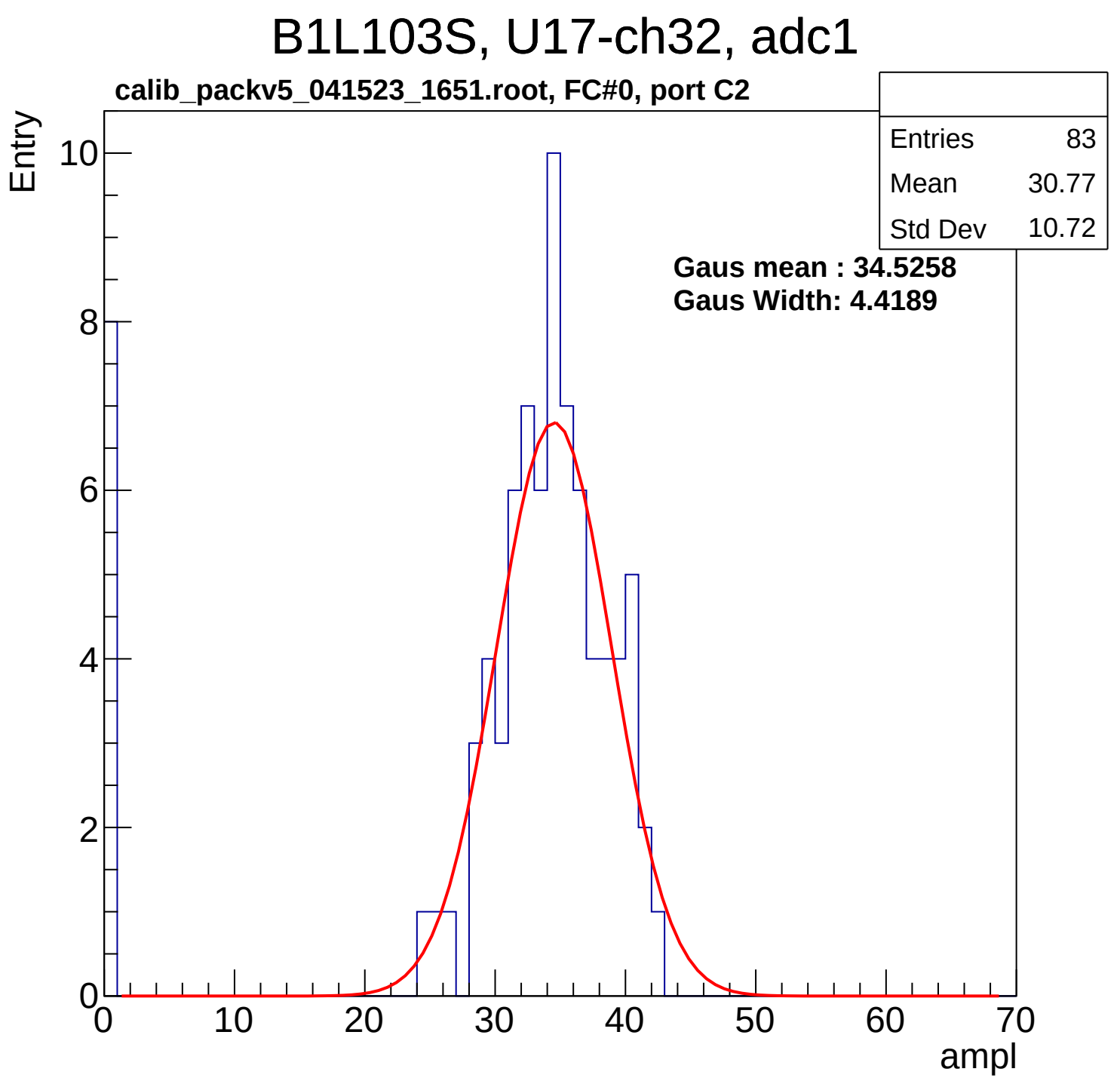

B1L103S, U17-ch31, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 56.44
Std Dev 3.31
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

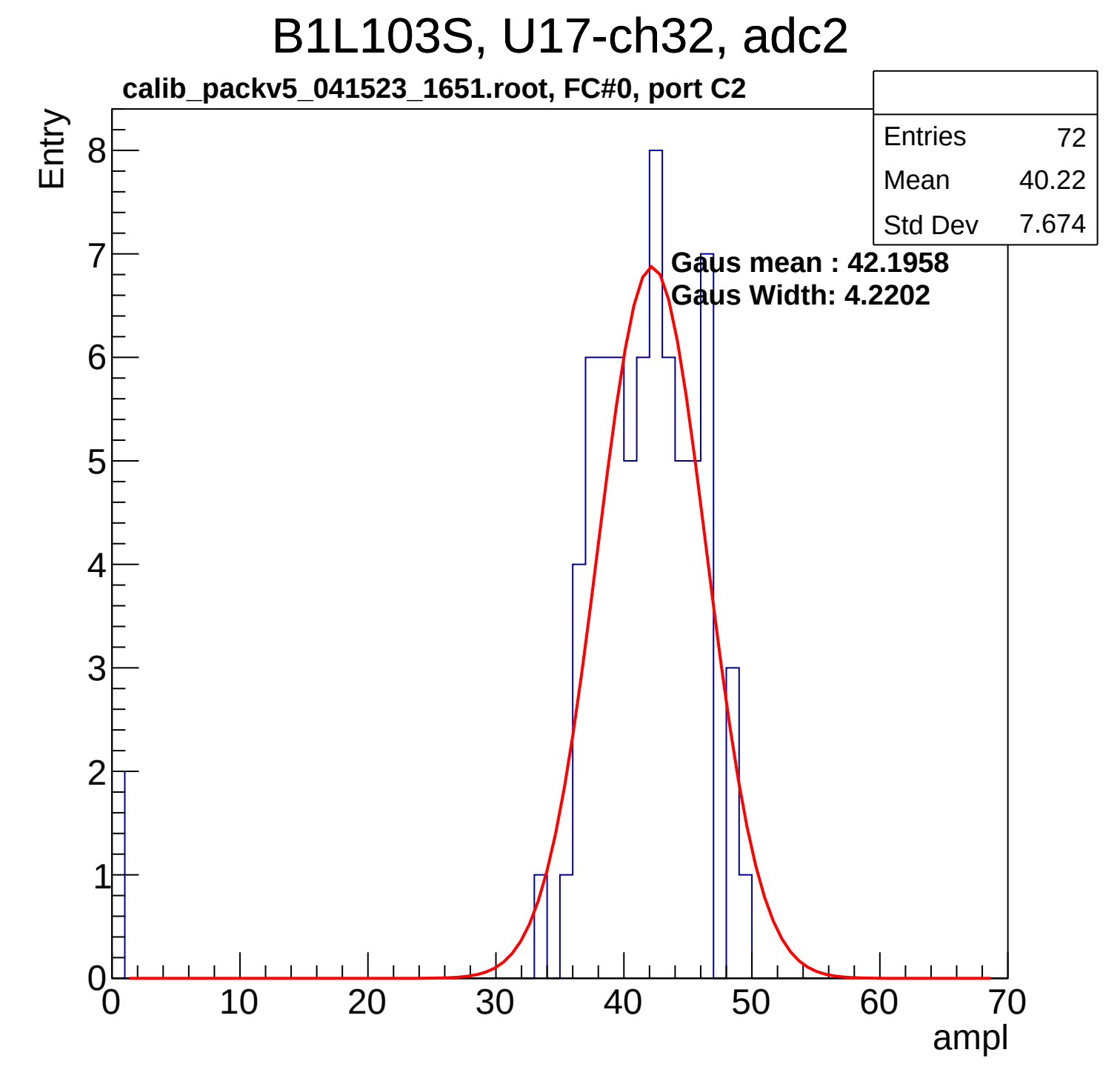

B1L103S, U17-ch31, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 58.95
Std Dev 9.749
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

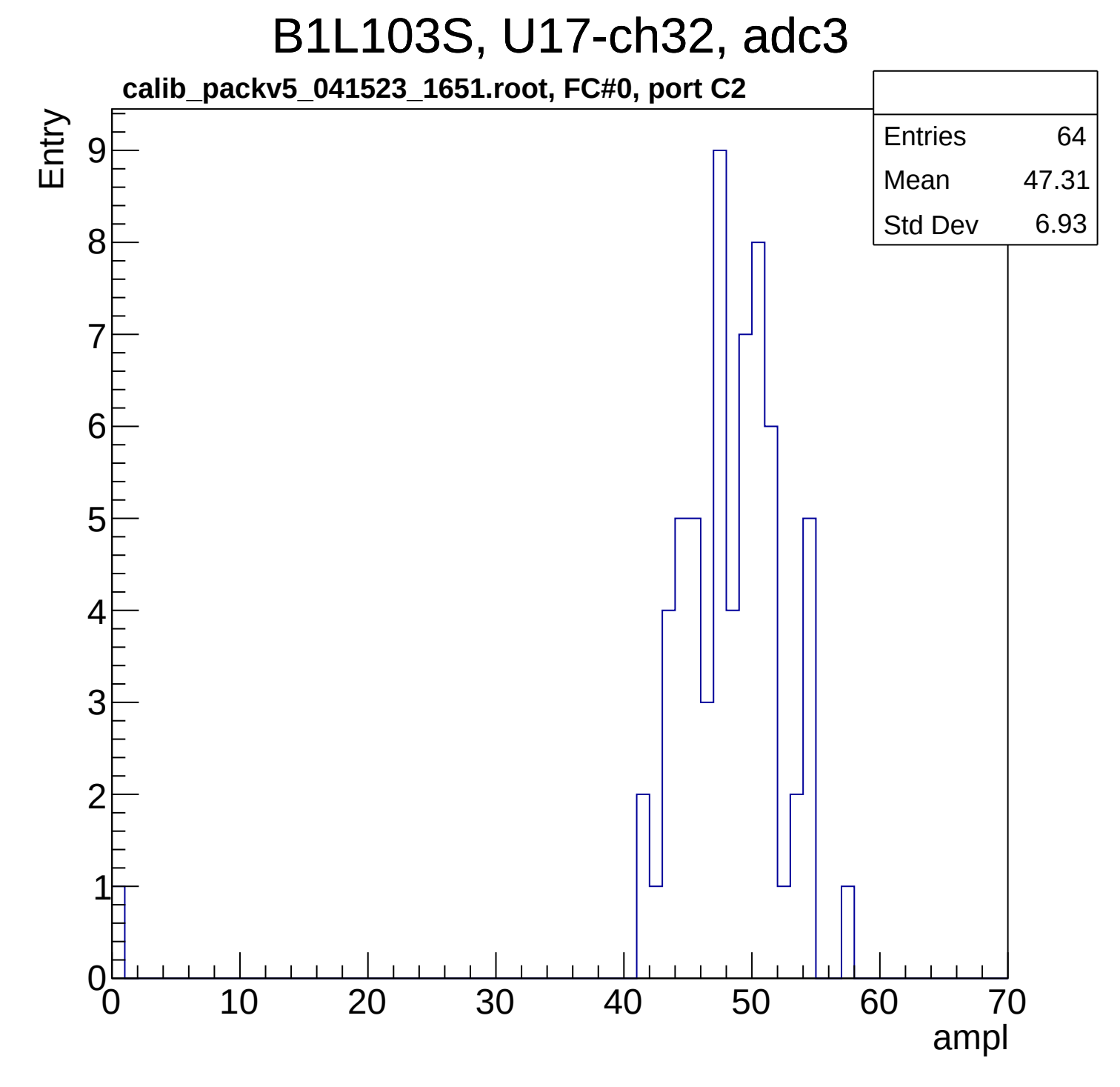

B1L103S, U17-ch31, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

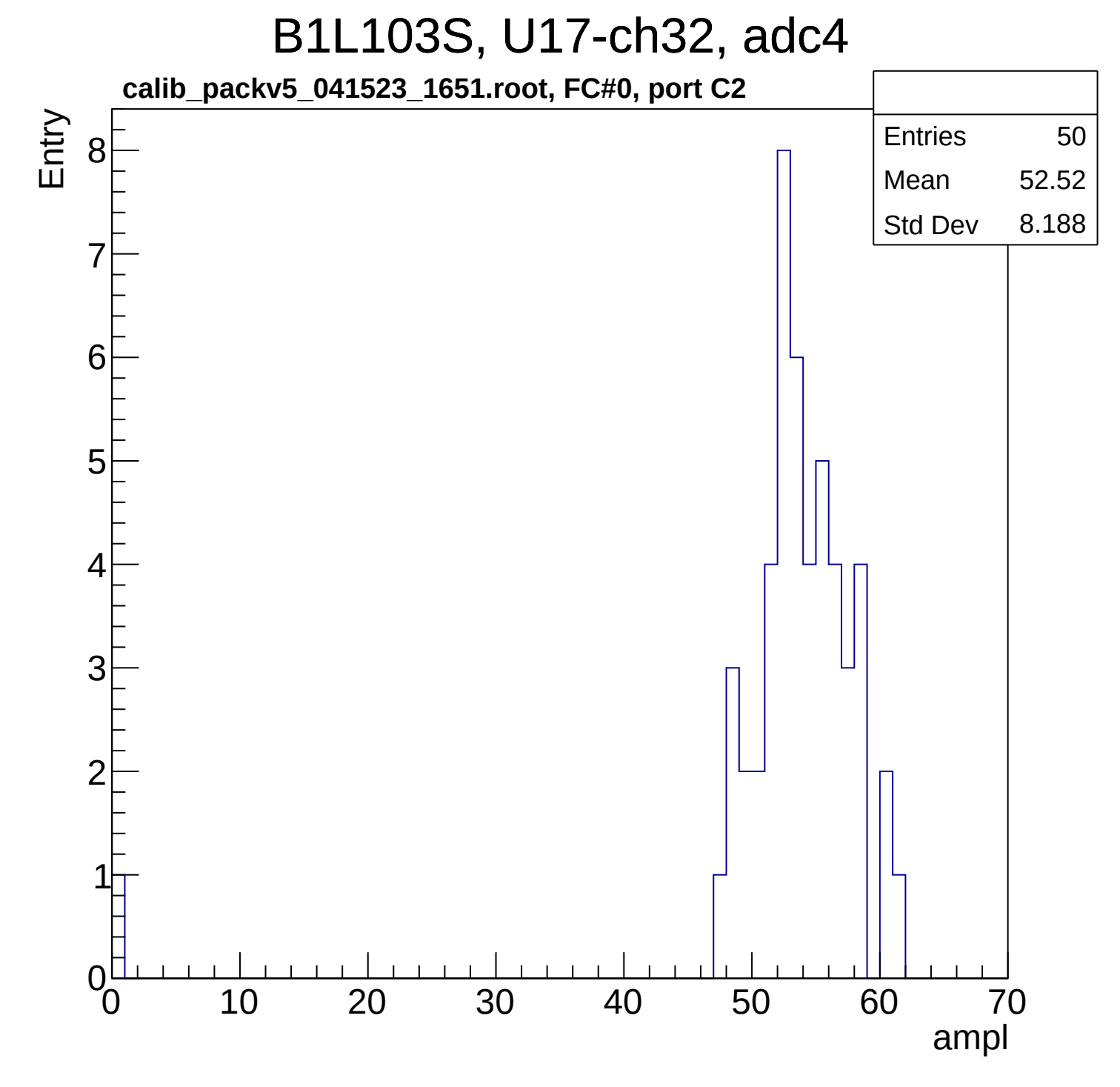

B1L103S, U17-ch31, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0.8947
Std Dev 3.796
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

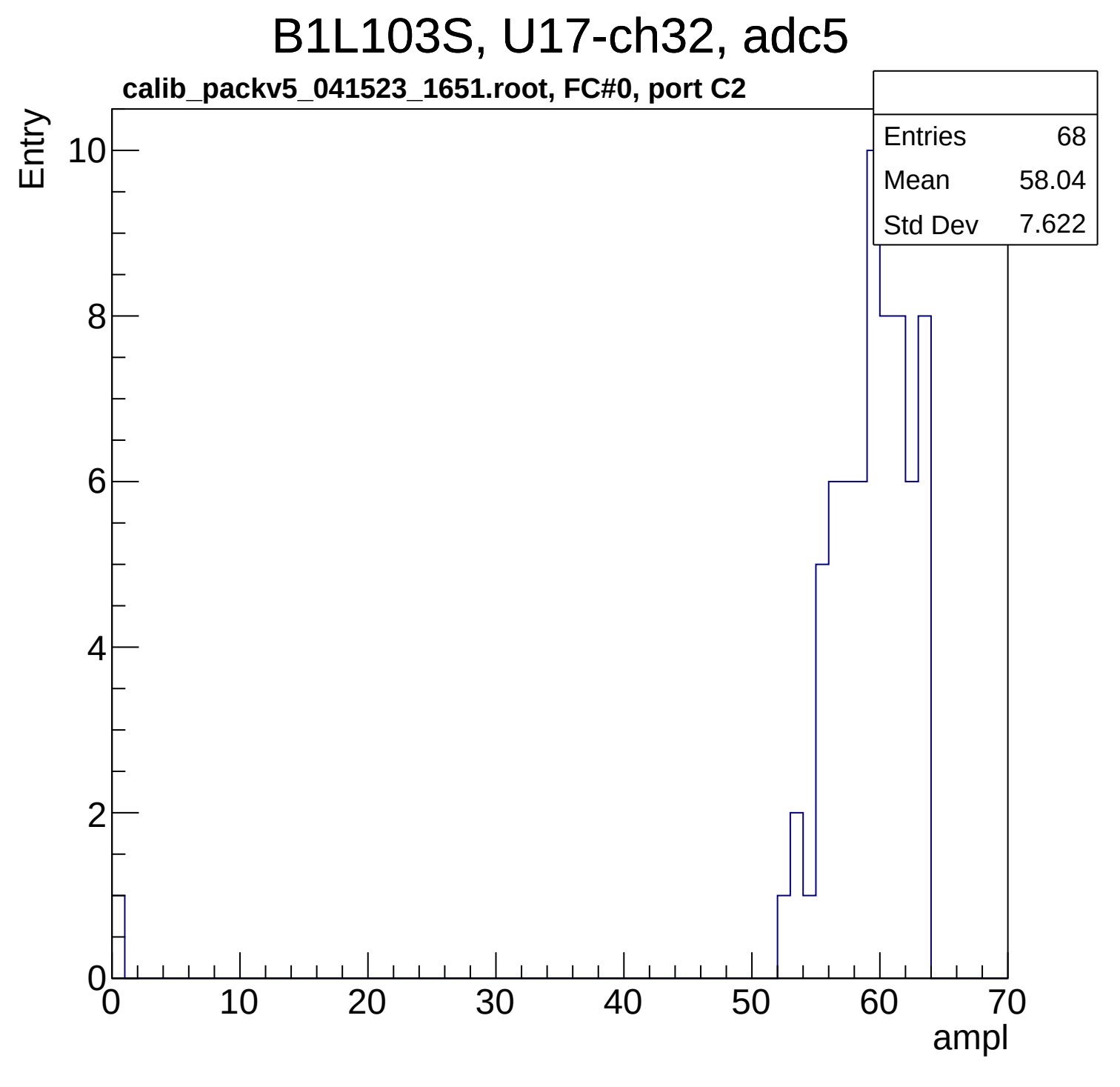

B1L103S, U17-ch32, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 23.85
Std Dev 9.994
Gaus mean : 28.4194
Gaus Width: 3.6389
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

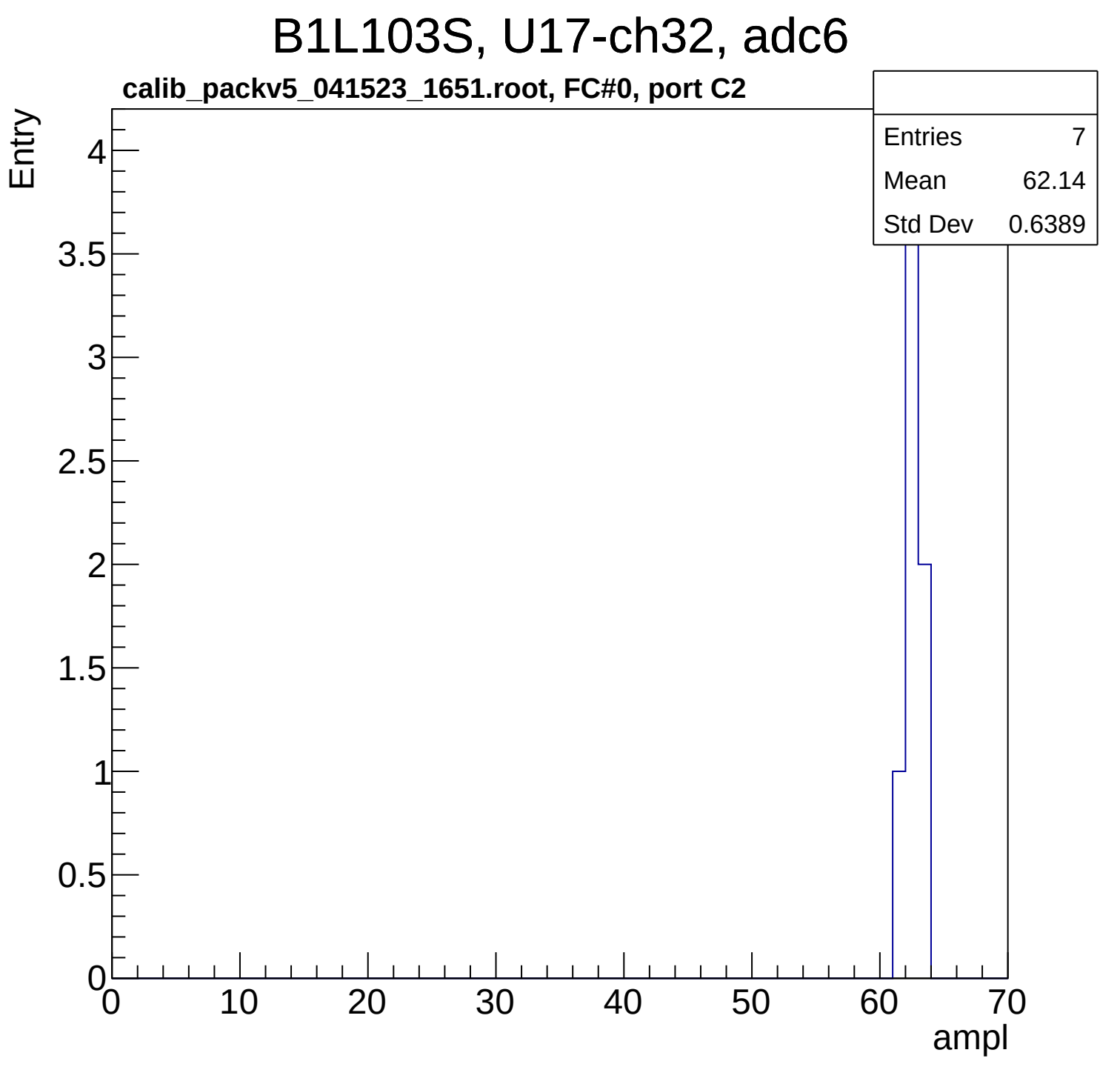

B1L103S, U17-ch32, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 30.77
Std Dev 10.72
Gaus mean : 34.5258
Gaus Width: 4.4189
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

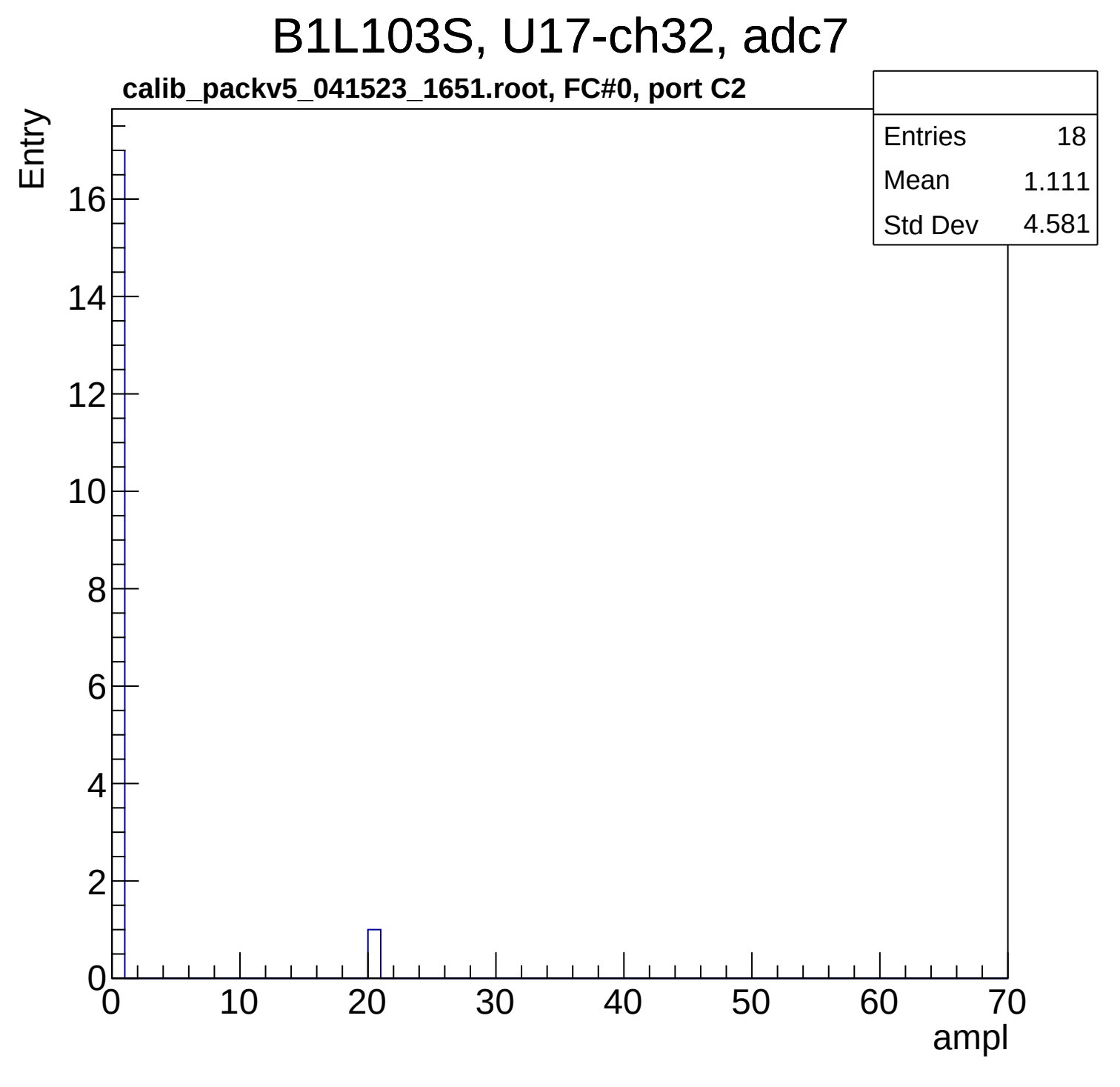

B1L103S, U17-ch32, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 40.22
Std Dev 7.674
Gaus mean : 42.1958
Gaus Width: 4.2202
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

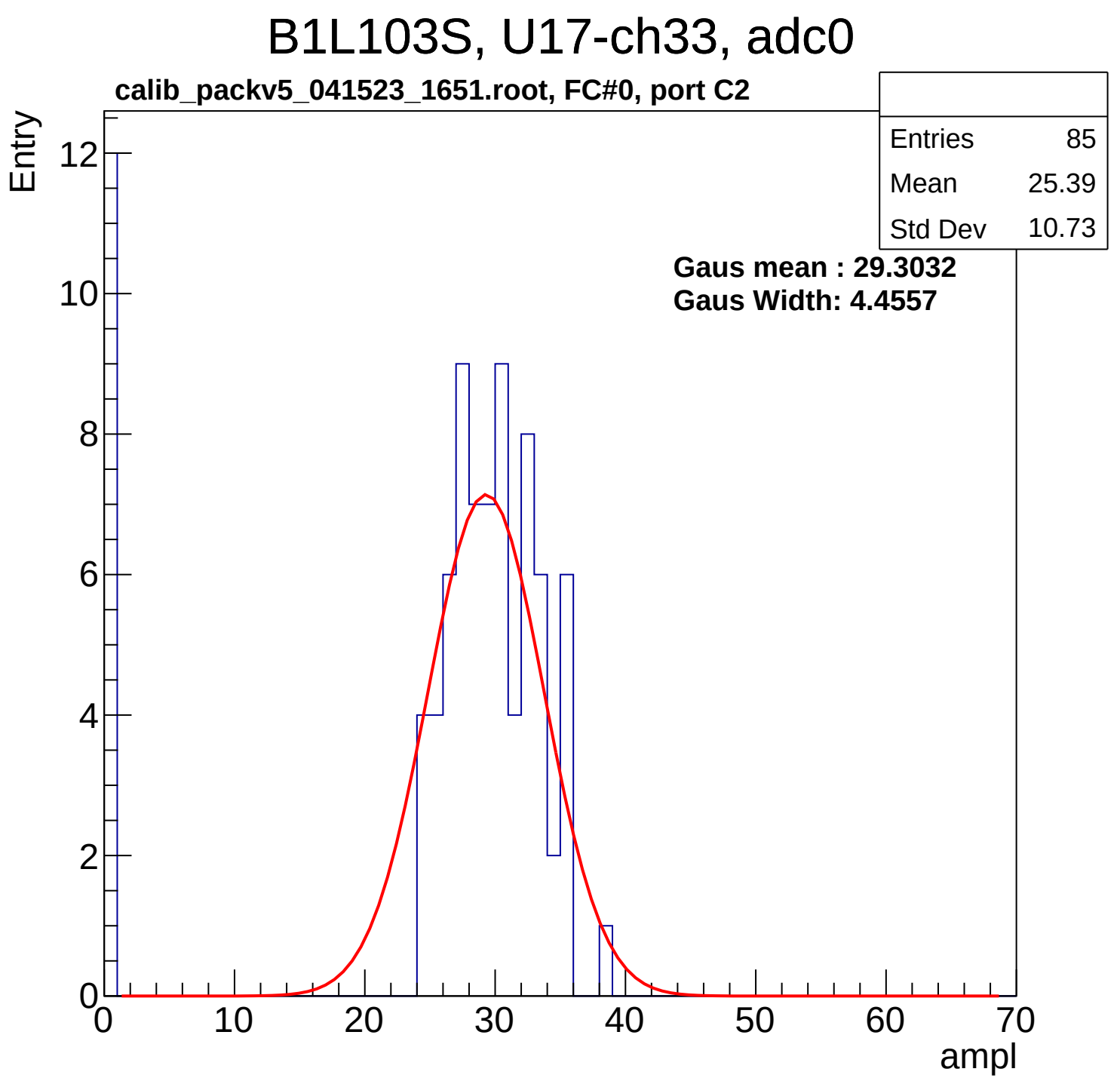

B1L103S, U17-ch32, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 47.31
Std Dev 6.93
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

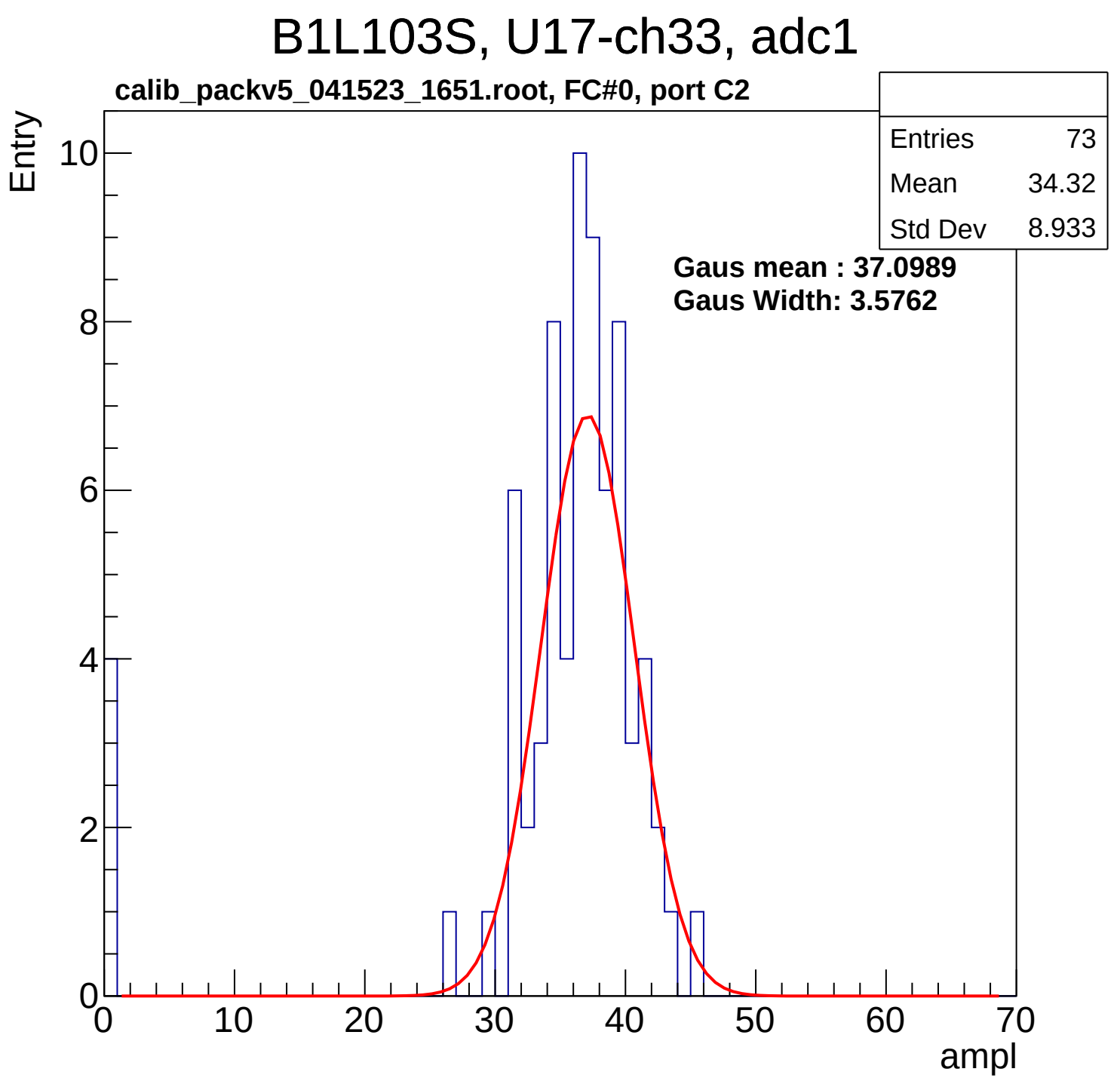

B1L103S, U17-ch32, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 52.52
Std Dev 8.188
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

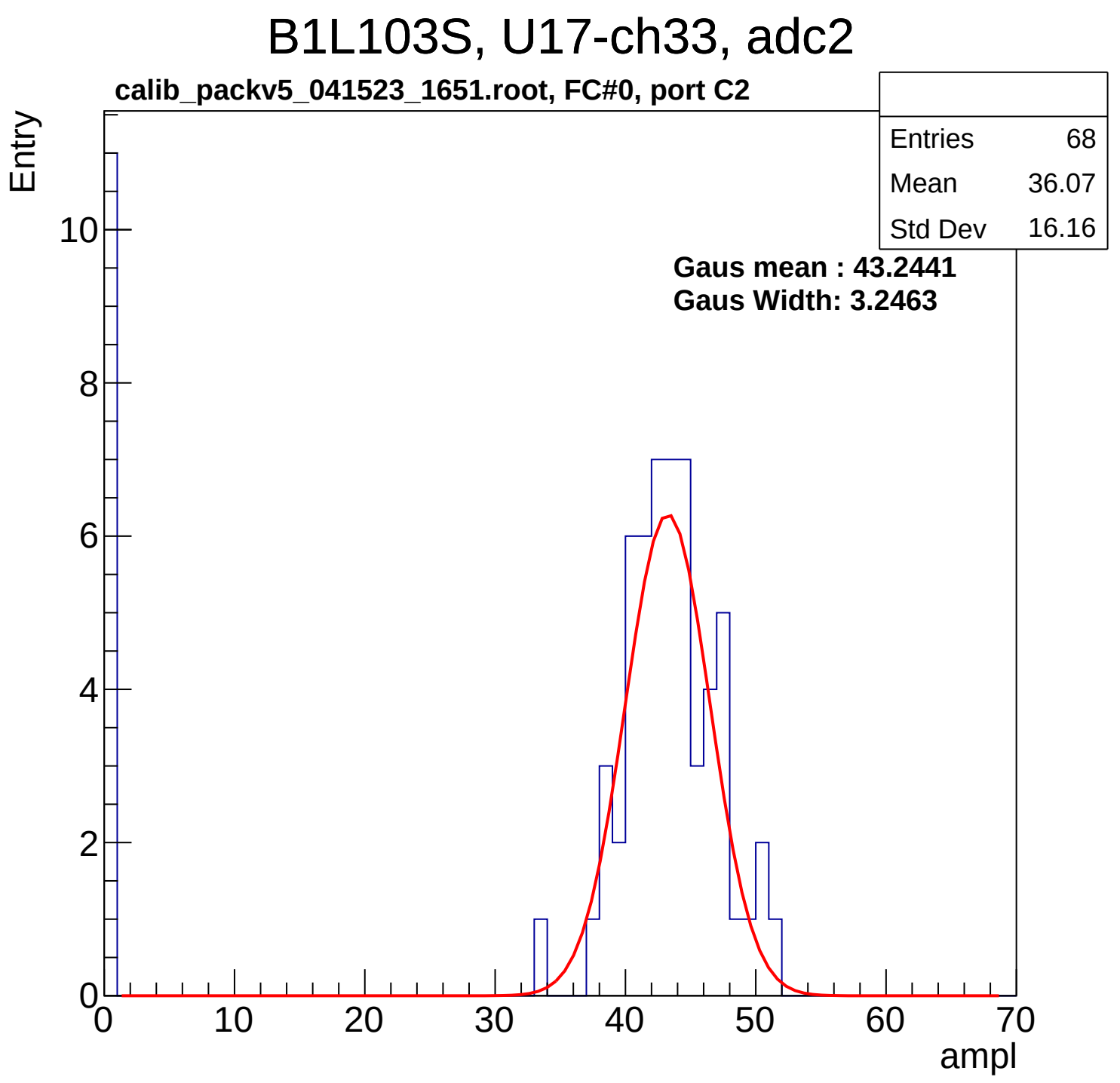

B1L103S, U17-ch32, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 58.04
Std Dev 7.622
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

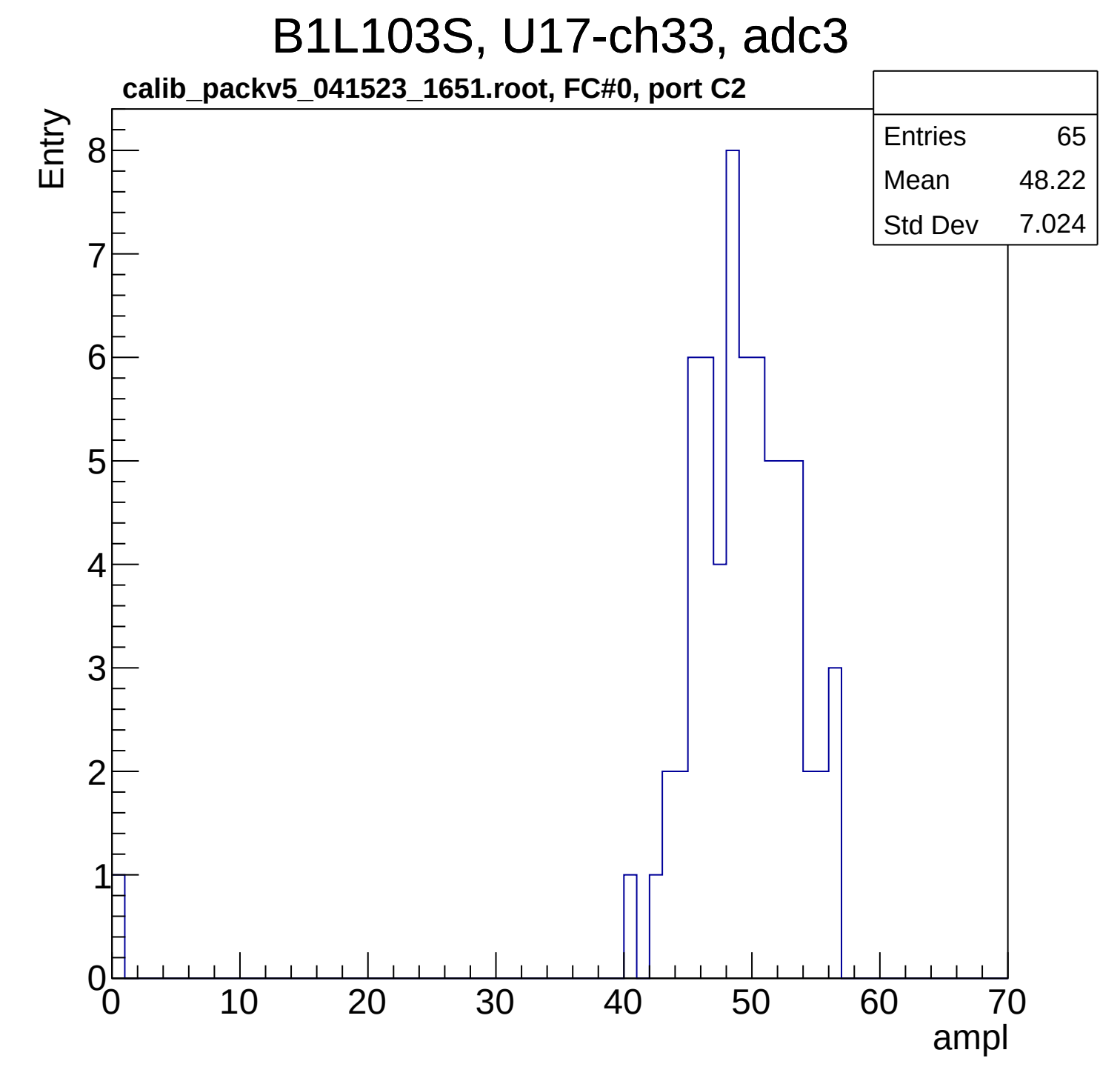

B1L103S, U17-ch32, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62.14
Std Dev 0.6389
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

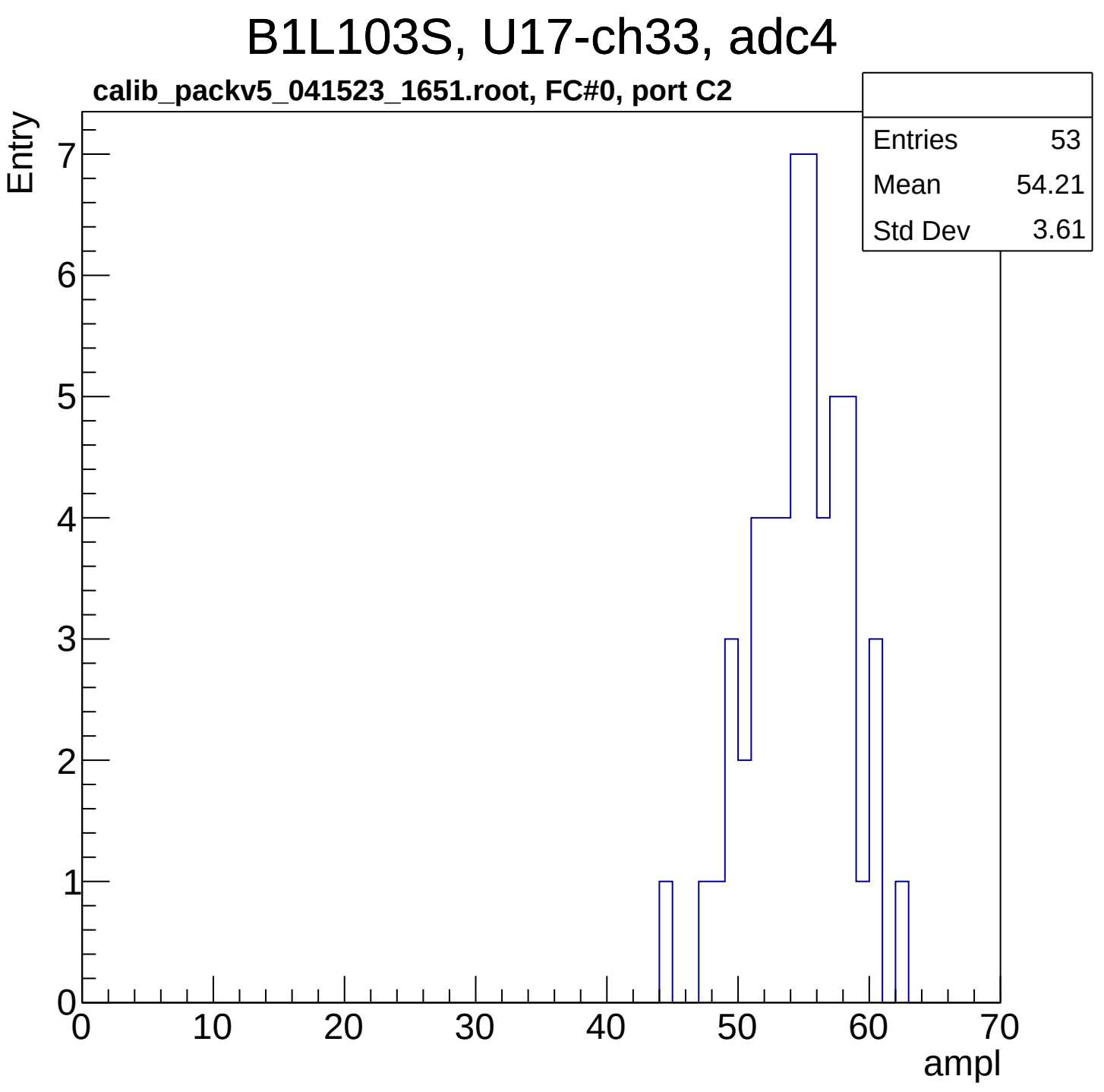

B1L103S, U17-ch32, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.111
Std Dev 4.581
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

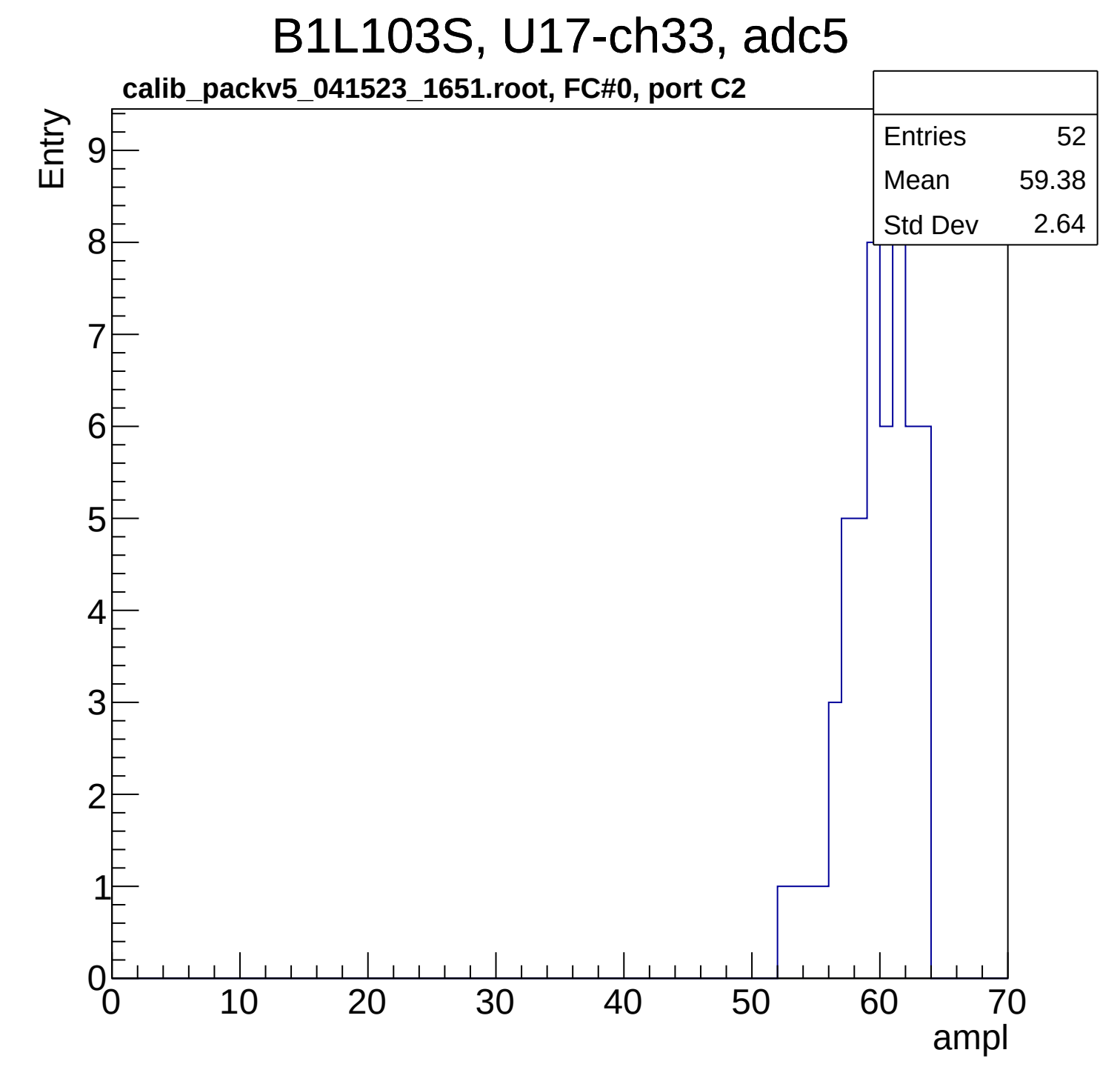

B1L103S, U17-ch33, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 25.39
Std Dev 10.73
Gaus mean : 29.3032
Gaus Width: 4.4557
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

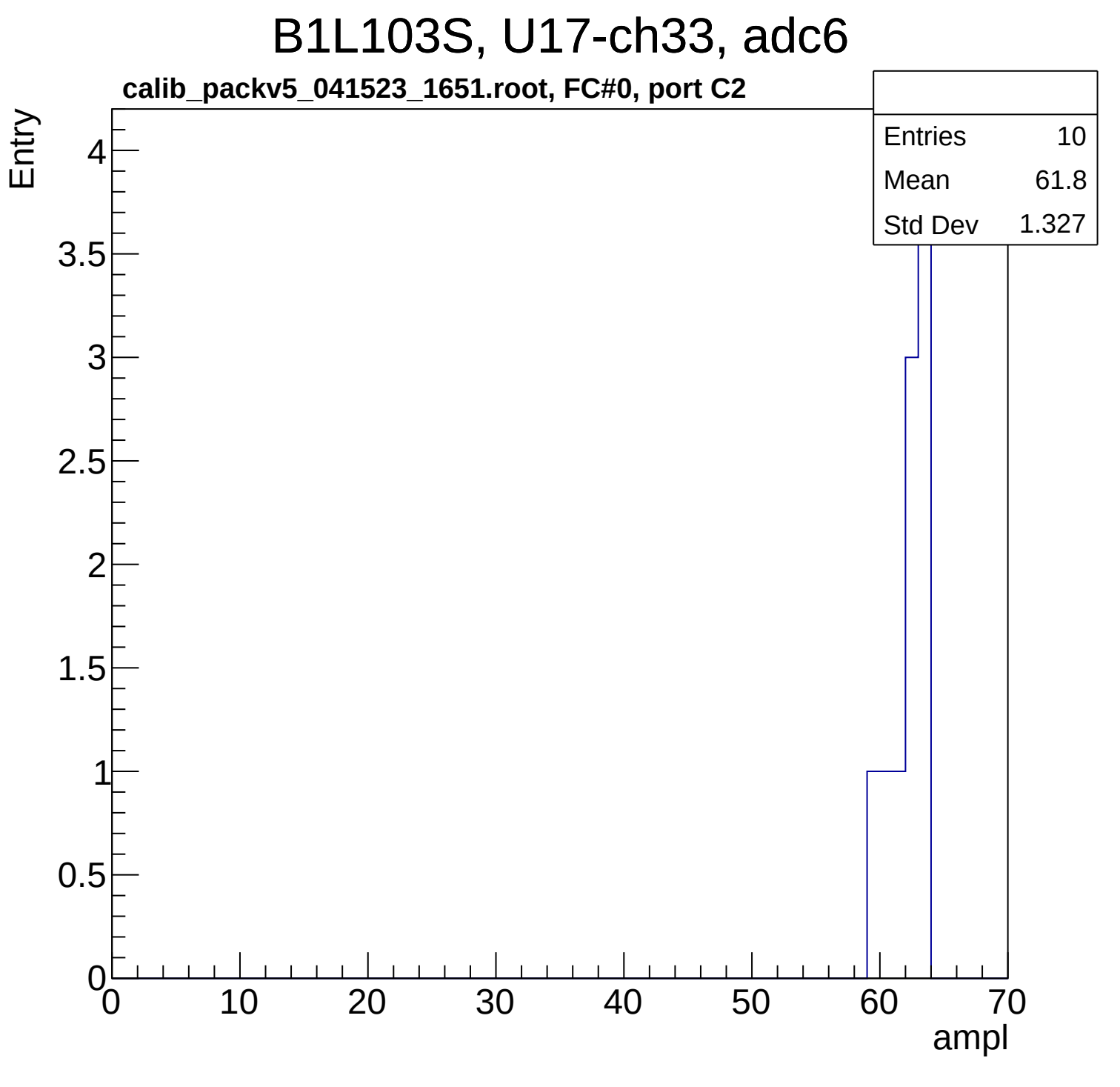

B1L103S, U17-ch33, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 34.32
Std Dev 8.933
Gaus mean : 37.0989
Gaus Width: 3.5762
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

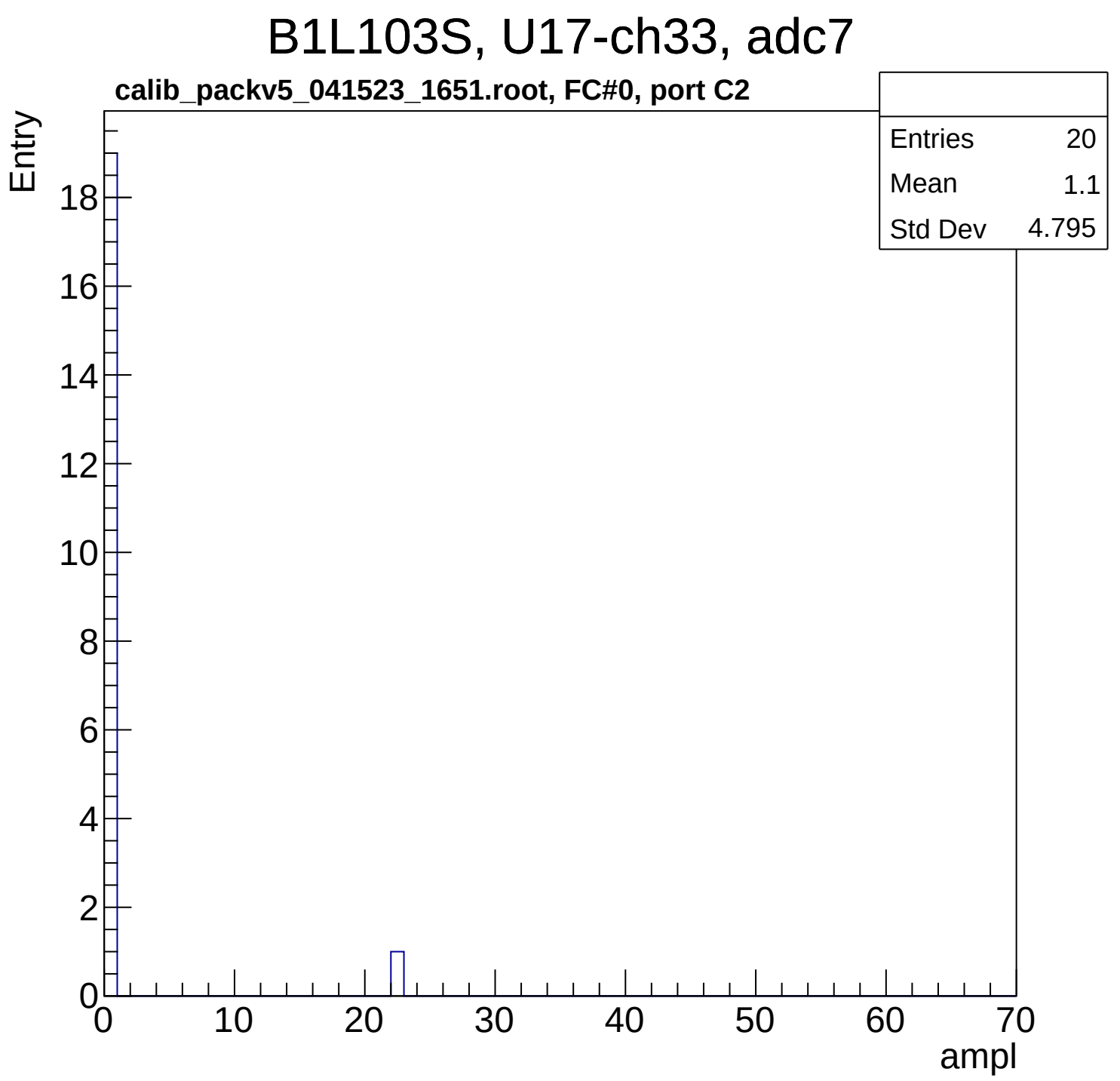

B1L103S, U17-ch33, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 36.07
Std Dev 16.16
Gaus mean : 43.2441
Gaus Width: 3.2463
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

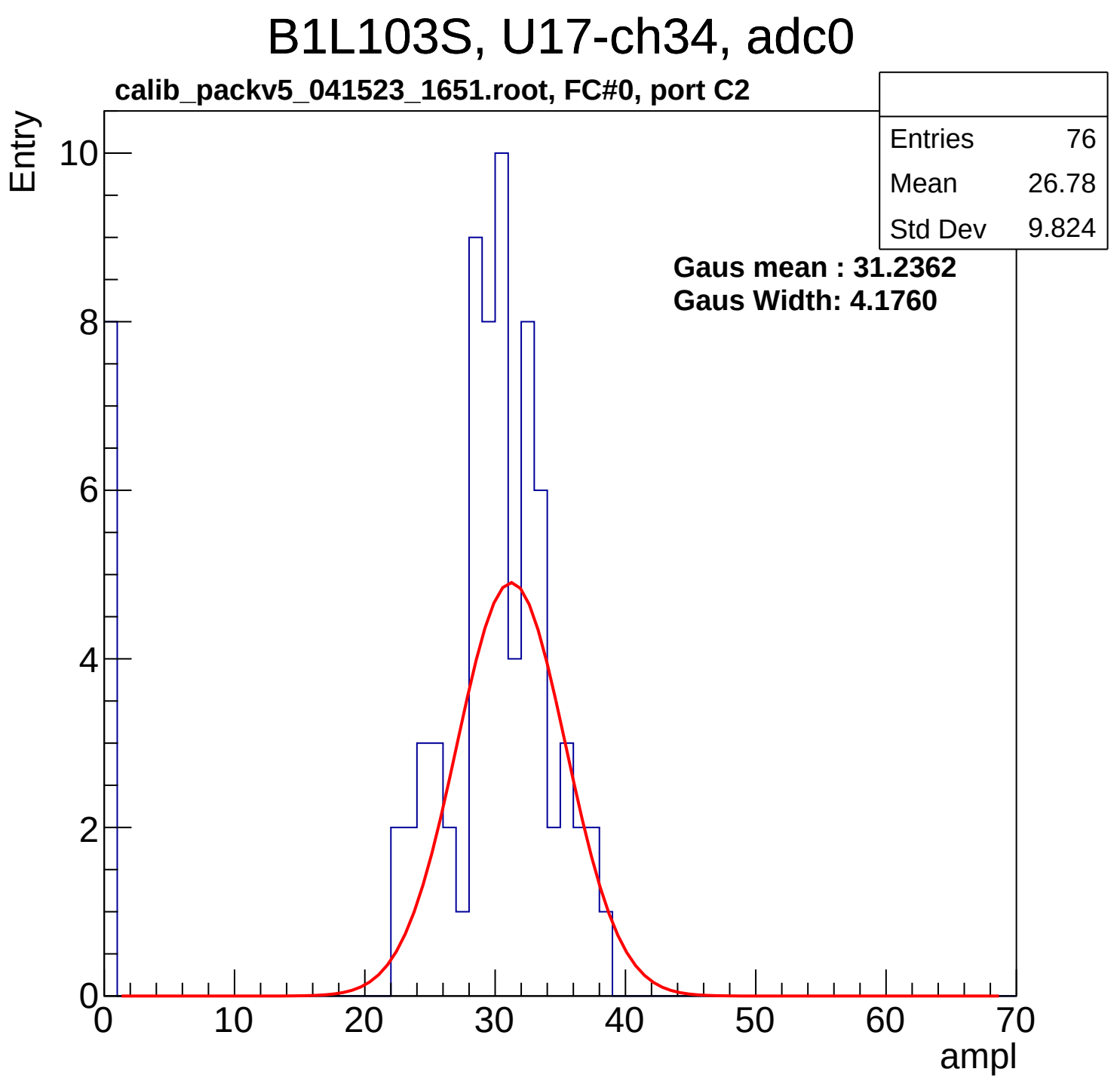

B1L103S, U17-ch33, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 48.22
Std Dev 7.024
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

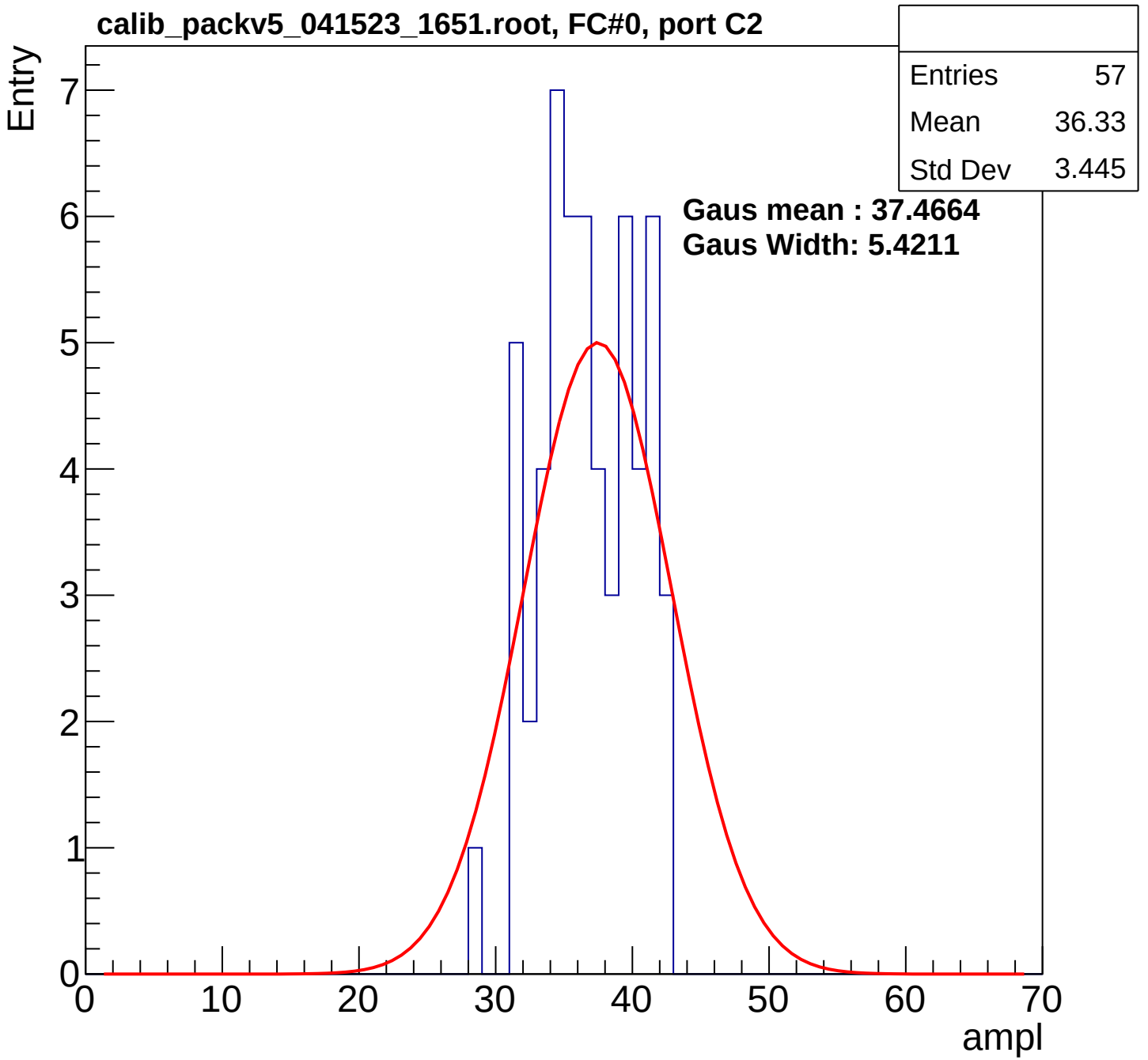

B1L103S, U17-ch33, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 54.21
Std Dev 3.61
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

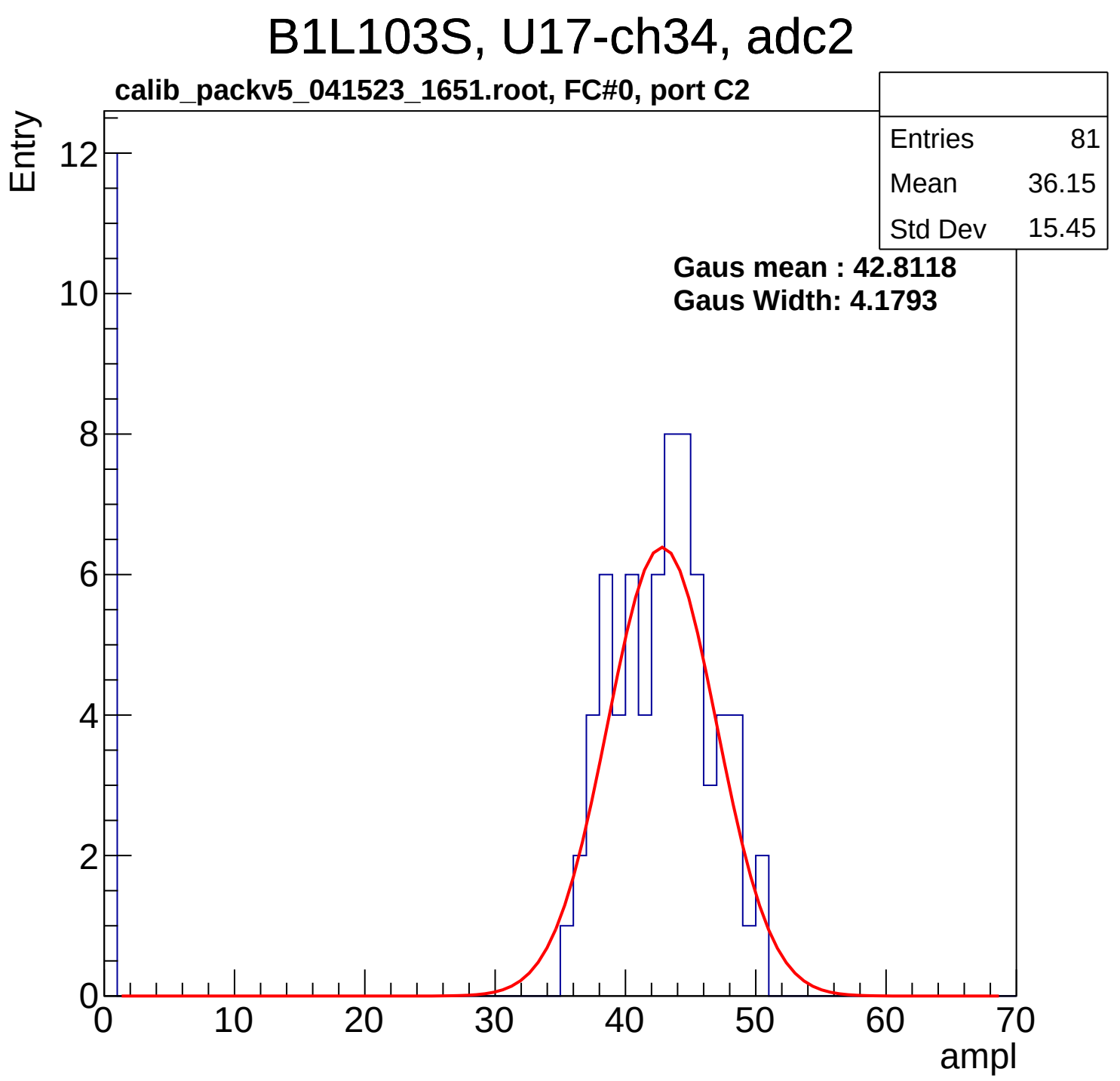

B1L103S, U17-ch33, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 59.38
Std Dev 2.64
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

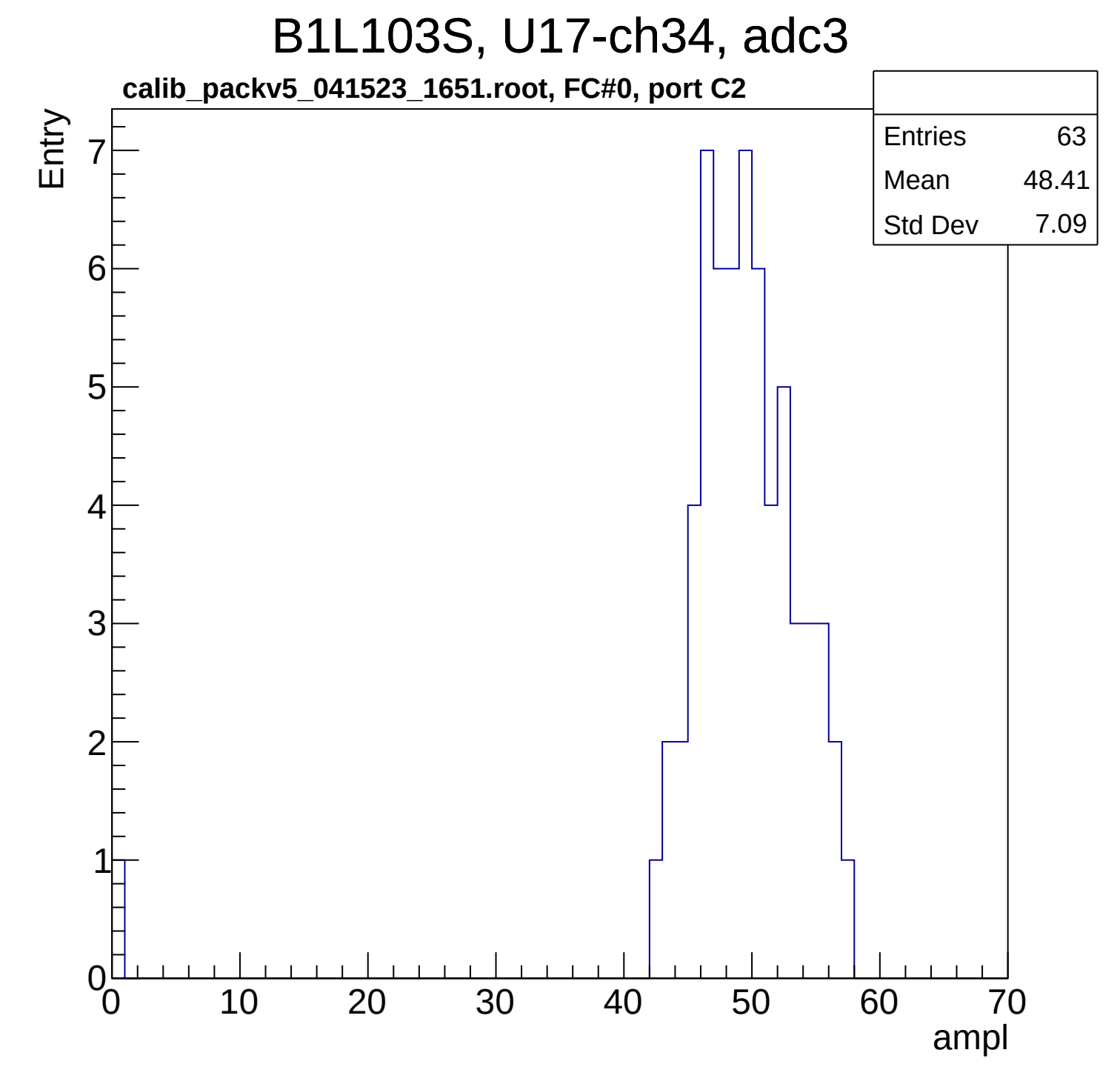

B1L103S, U17-ch33, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.8
Std Dev 1.327
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

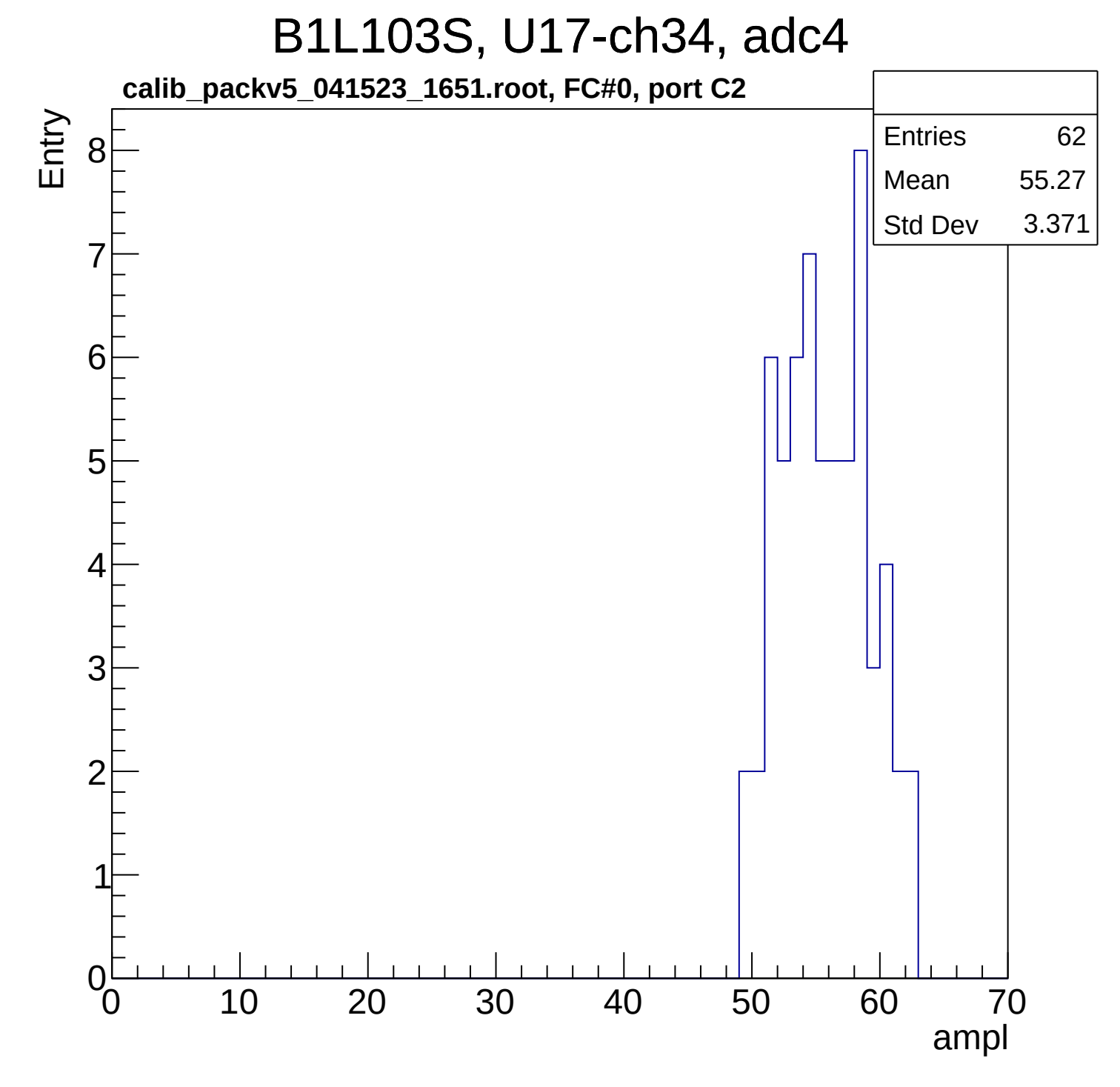

B1L103S, U17-ch33, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 1.1
Std Dev 4.795
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

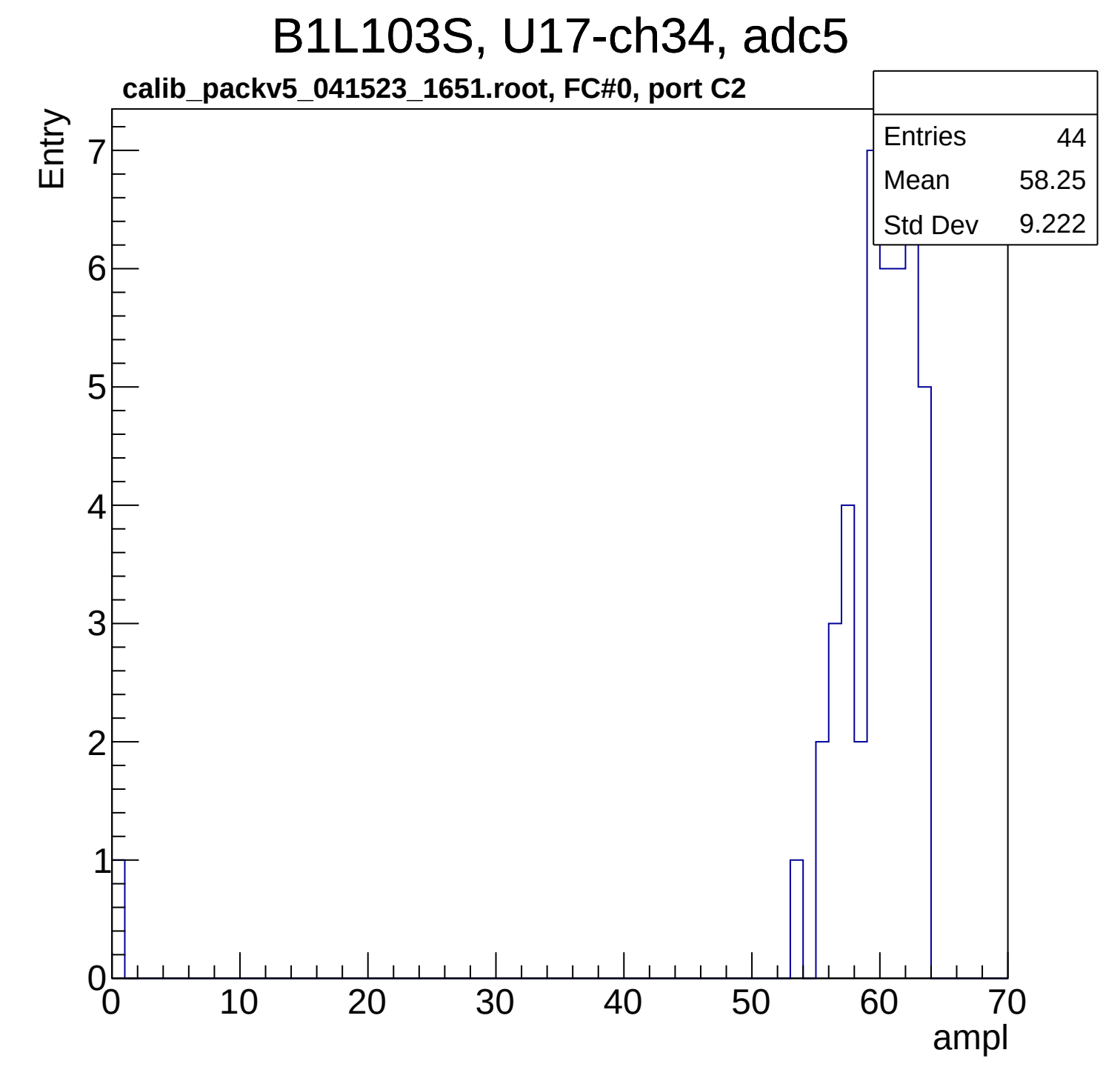

B1L103S, U17-ch34, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 26.78
Std Dev 9.824
Gaus mean : 31.2362
Gaus Width: 4.1760
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

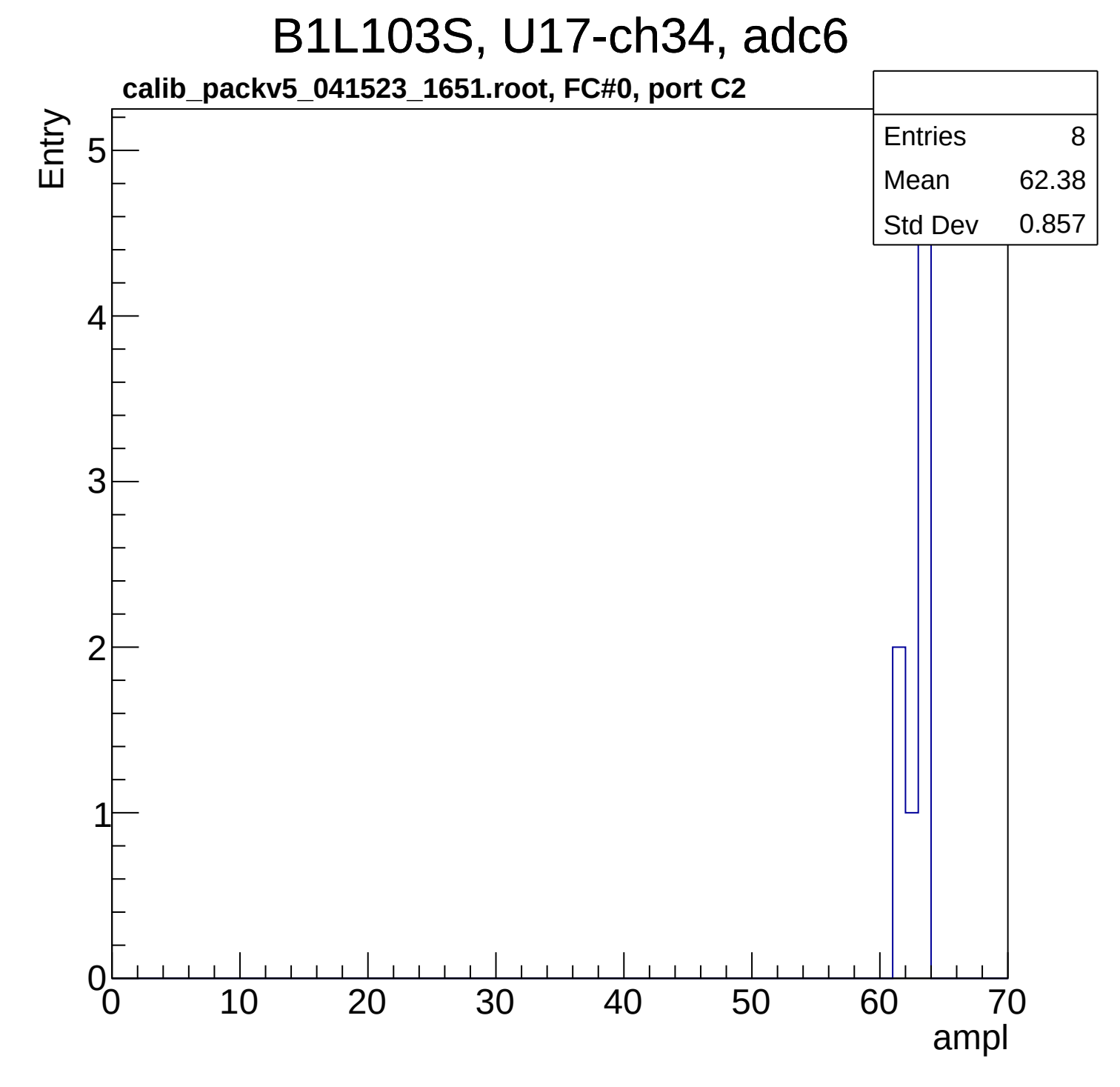

B1L103S, U17-ch34, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 36.33
Std Dev 3.445
Gaus mean : 37.4664
Gaus Width: 5.4211
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

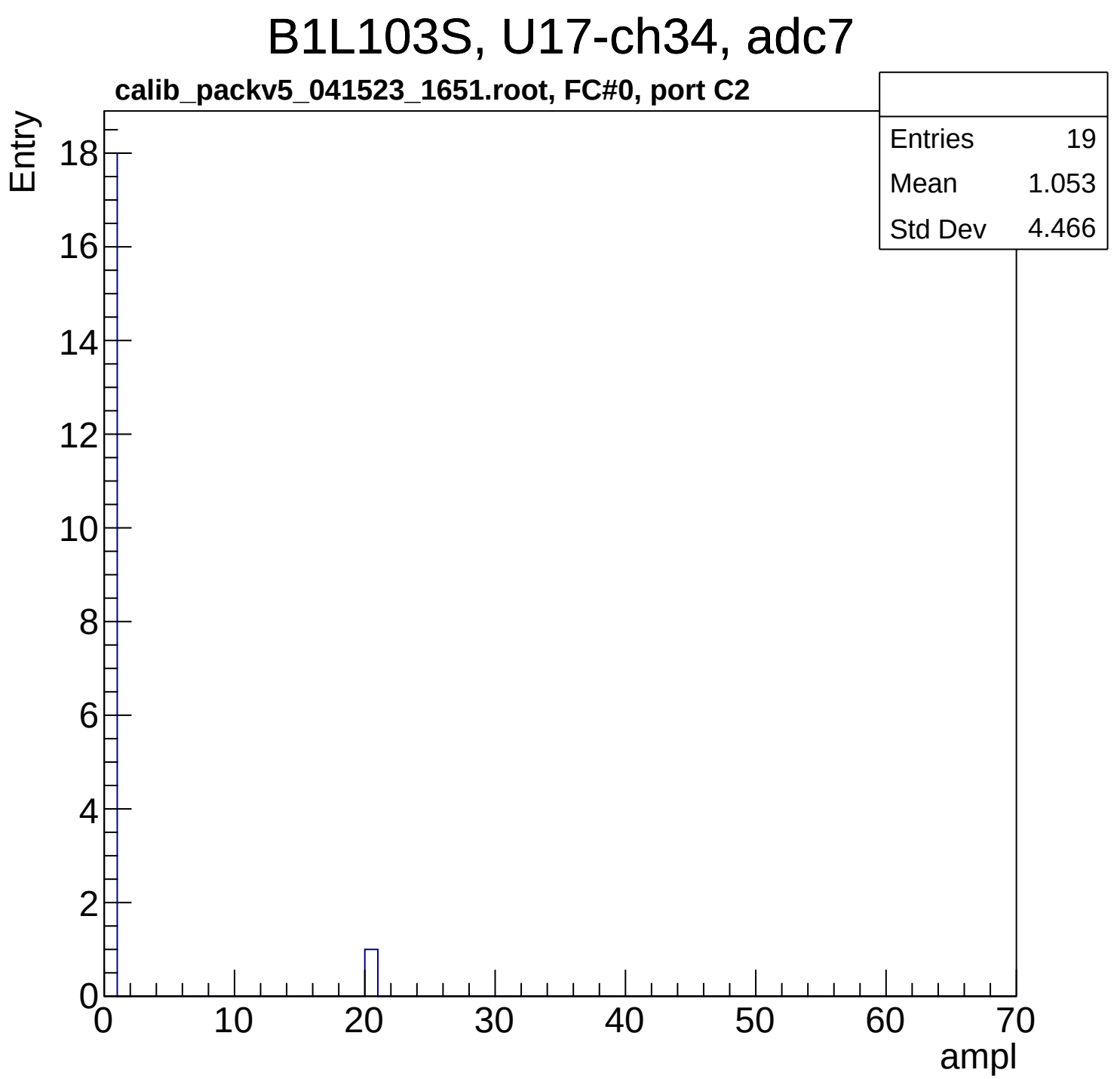

B1L103S, U17-ch34, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 36.15
Std Dev 15.45
Gaus mean : 42.8118
Gaus Width: 4.1793
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

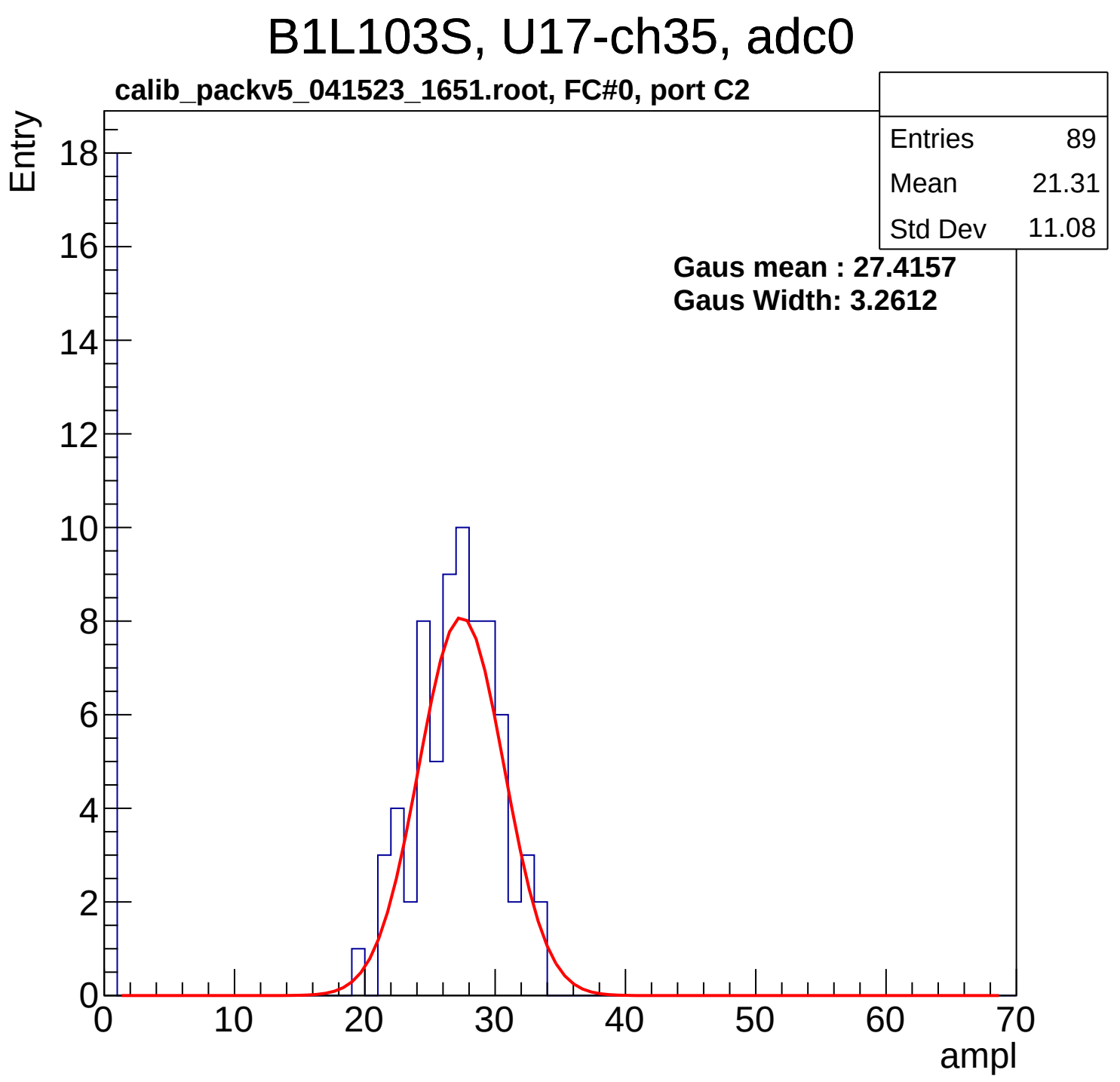

B1L103S, U17-ch34, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 48.41
Std Dev 7.09
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

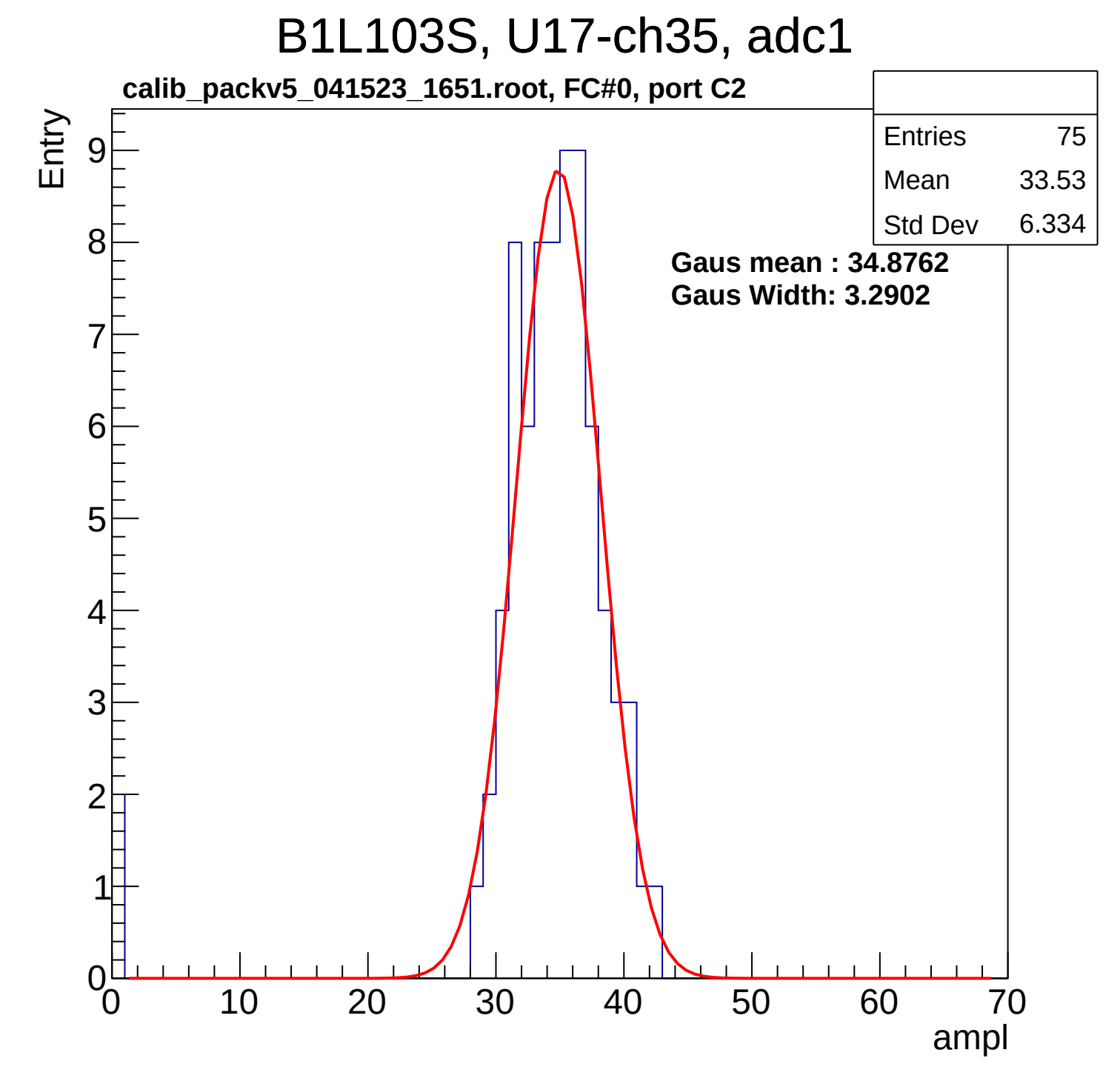

B1L103S, U17-ch34, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 55.27
Std Dev 3.371
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

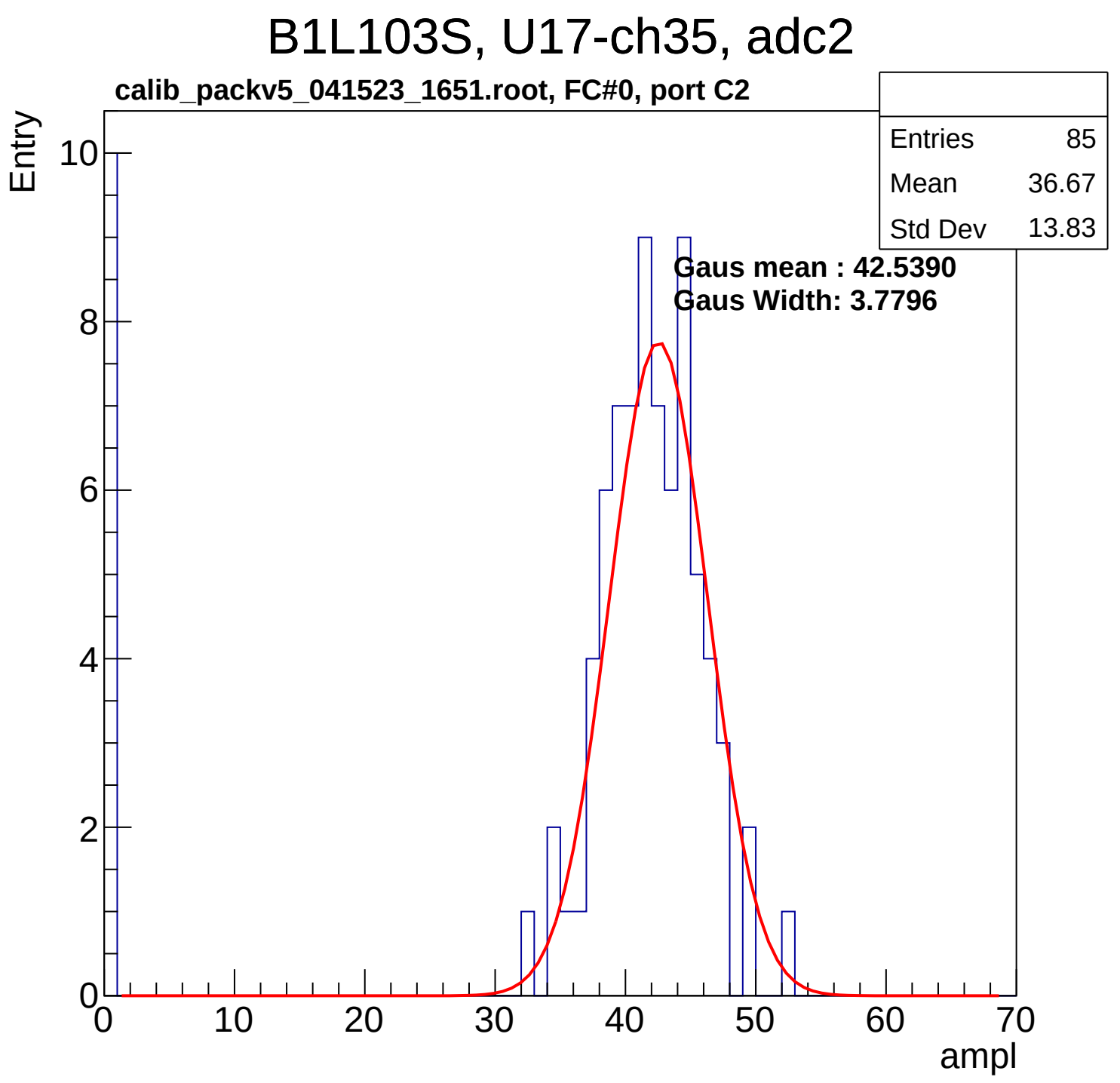

B1L103S, U17-ch34, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 58.25
Std Dev 9.222
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

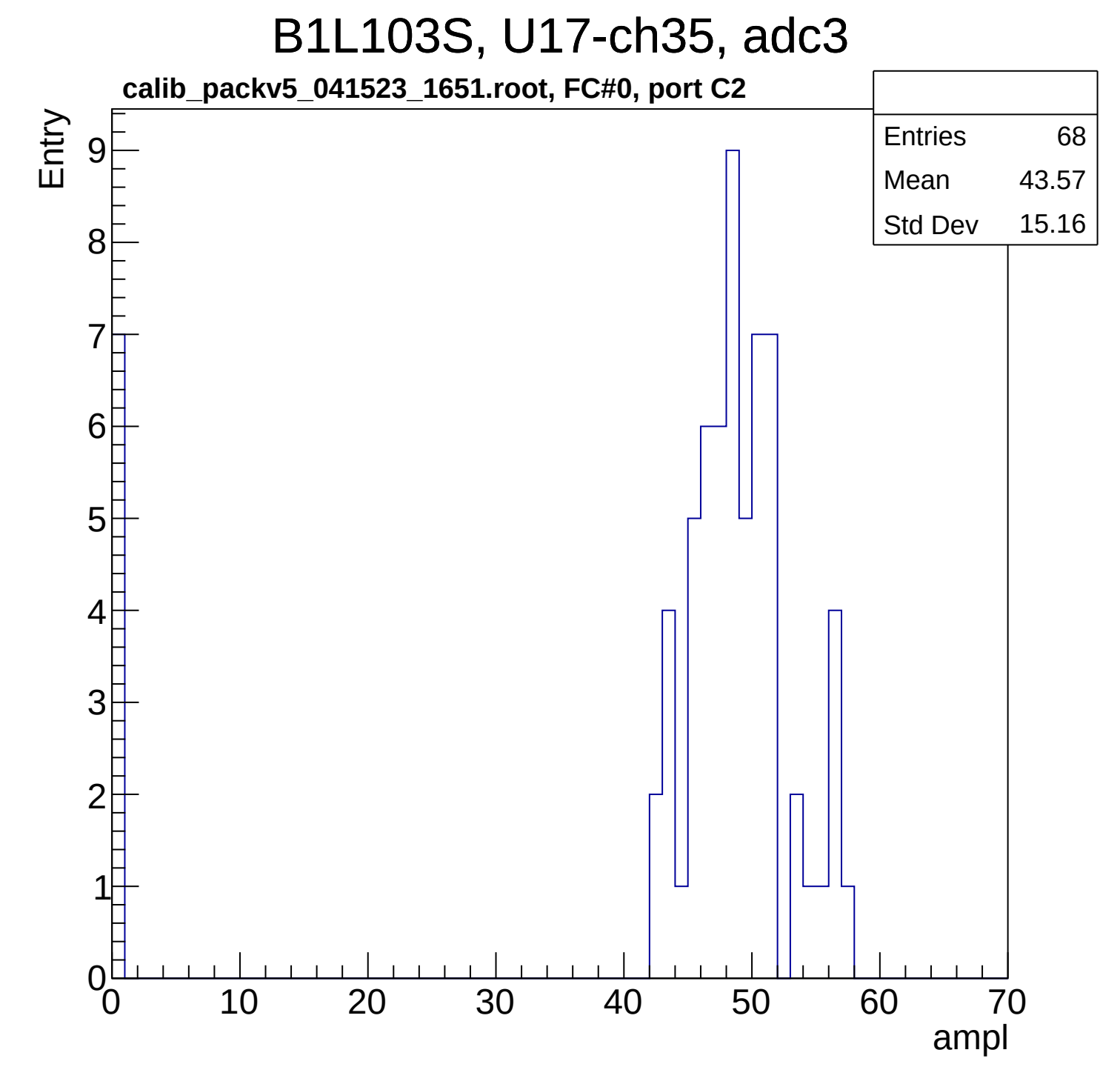

B1L103S, U17-ch34, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62.38
Std Dev 0.857
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

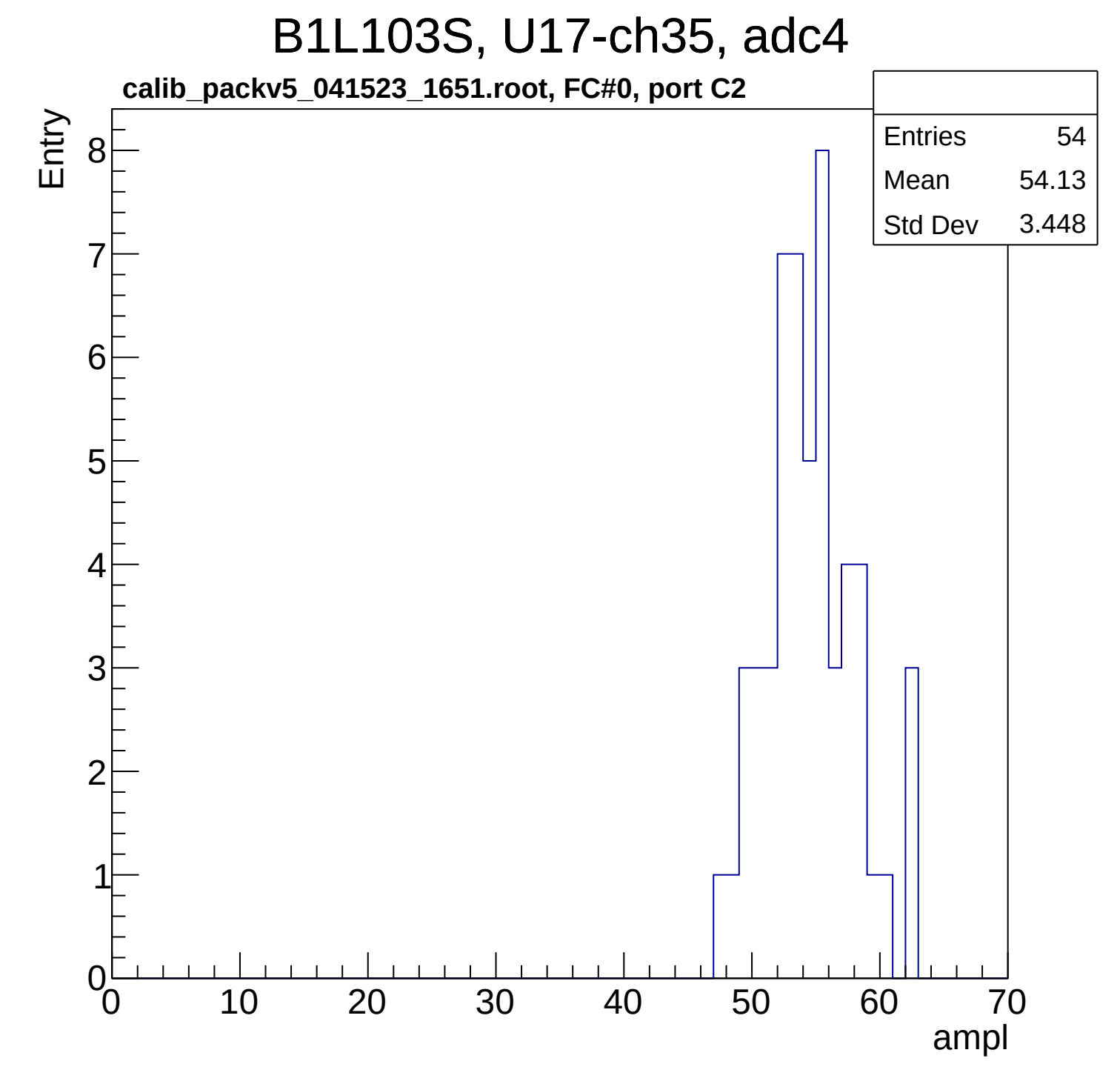

B1L103S, U17-ch34, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.053
Std Dev 4.466
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

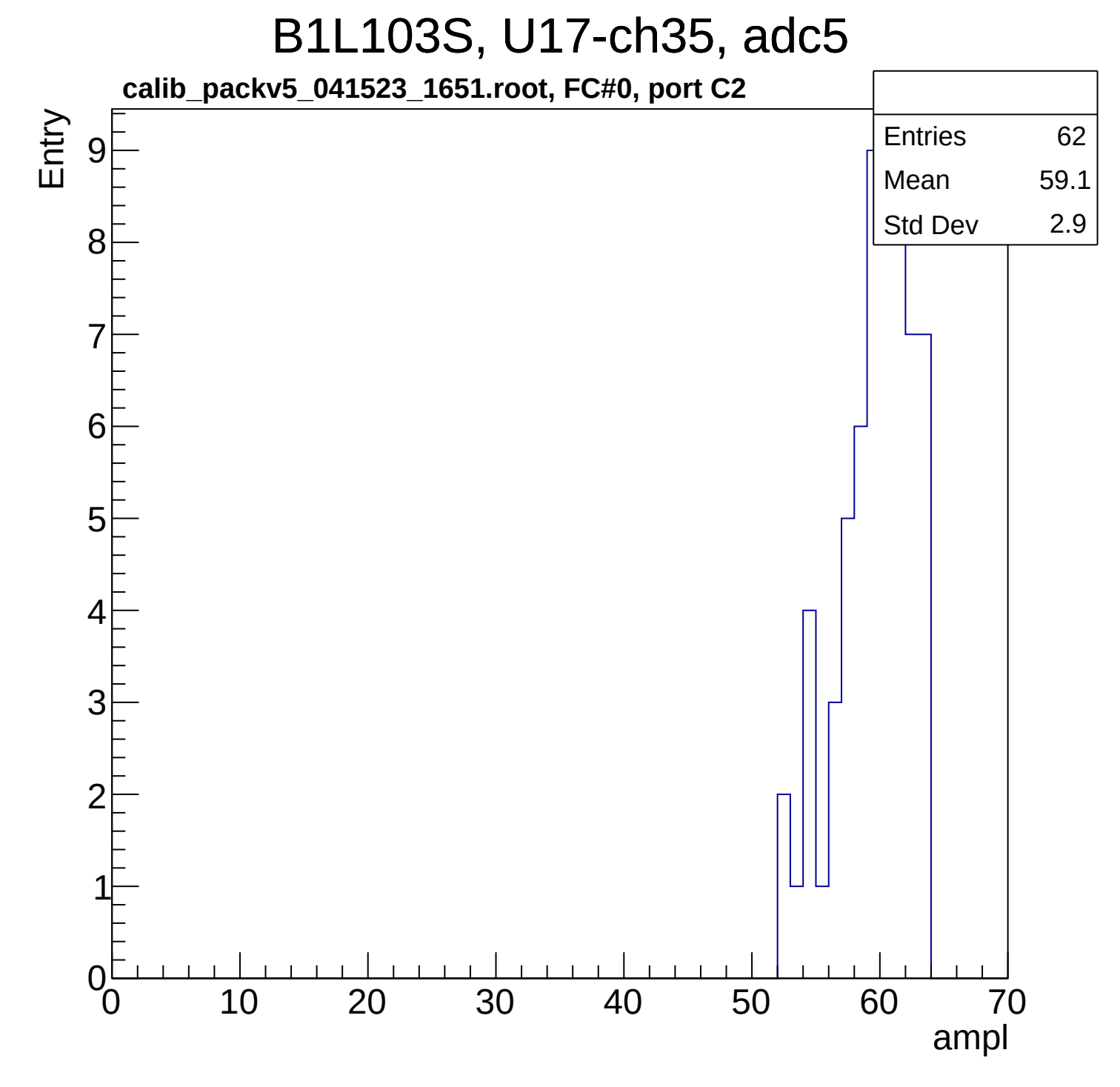

B1L103S, U17-ch35, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 21.31
Std Dev 11.08
Gaus mean : 27.4157
Gaus Width: 3.2612
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

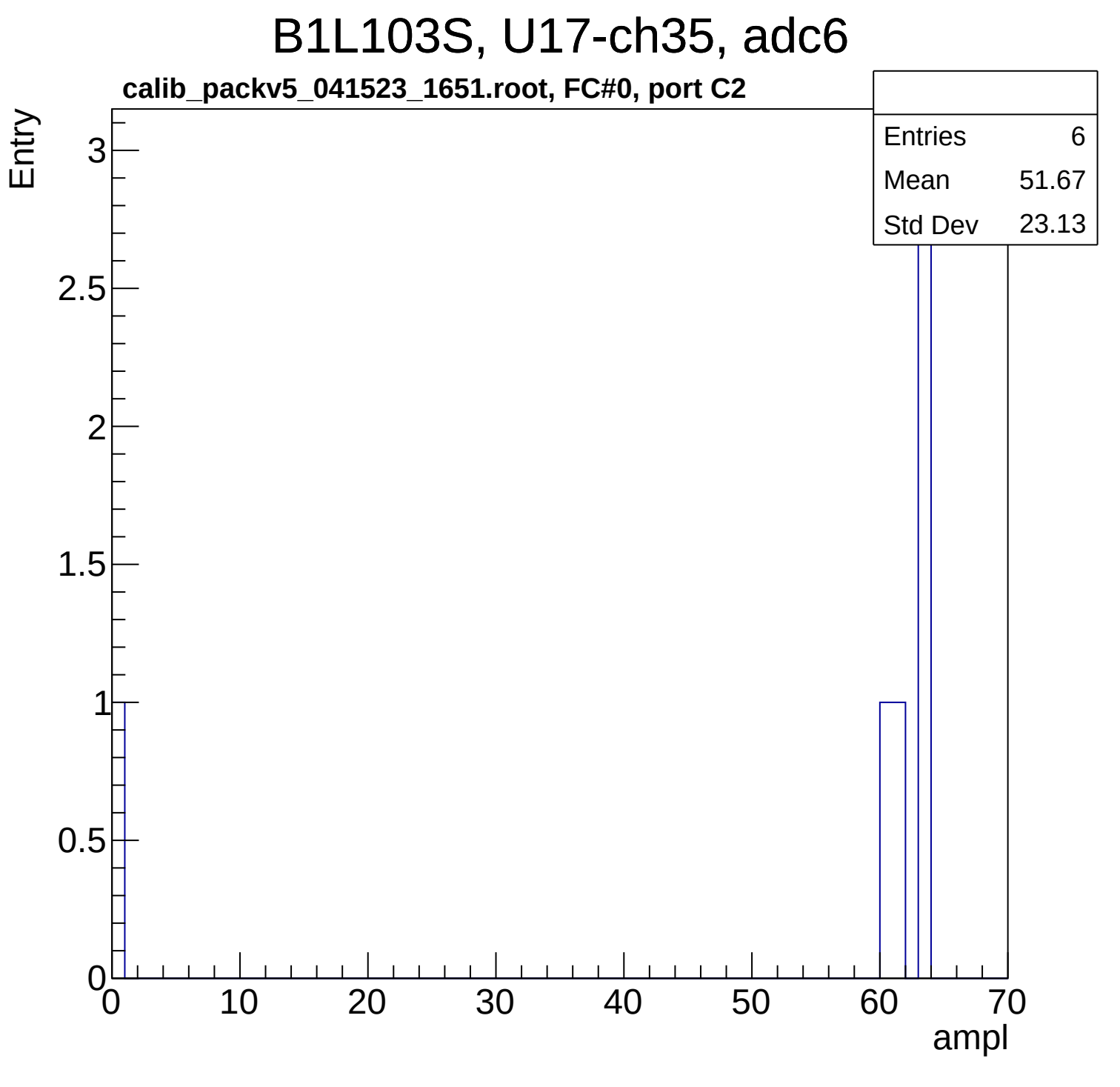

B1L103S, U17-ch35, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 33.53
Std Dev 6.334
Gaus mean : 34.8762
Gaus Width: 3.2902
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

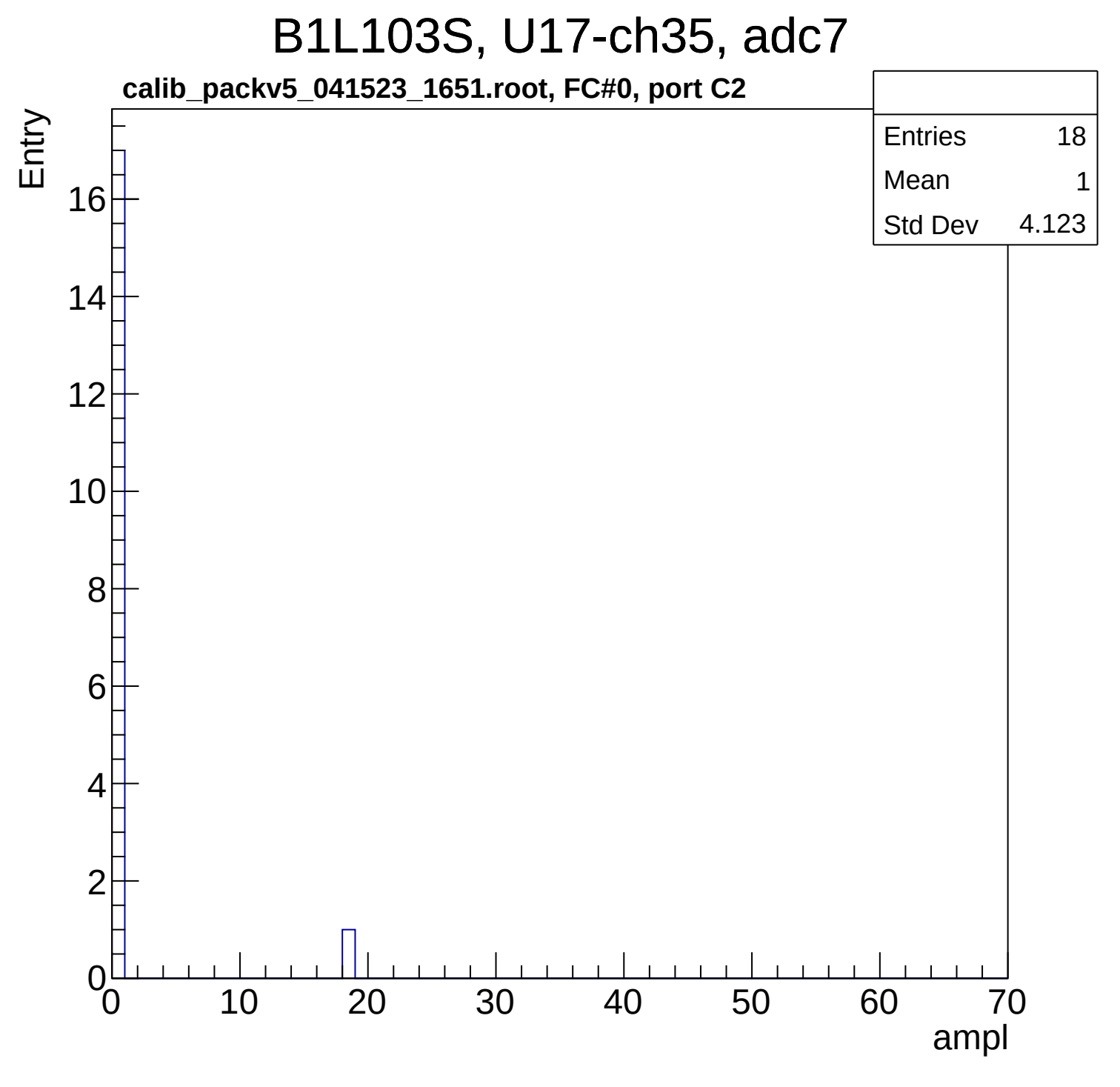

B1L103S, U17-ch35, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 36.67
Std Dev 13.83
Gaus mean : 42.5390
Gaus Width: 3.7796
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

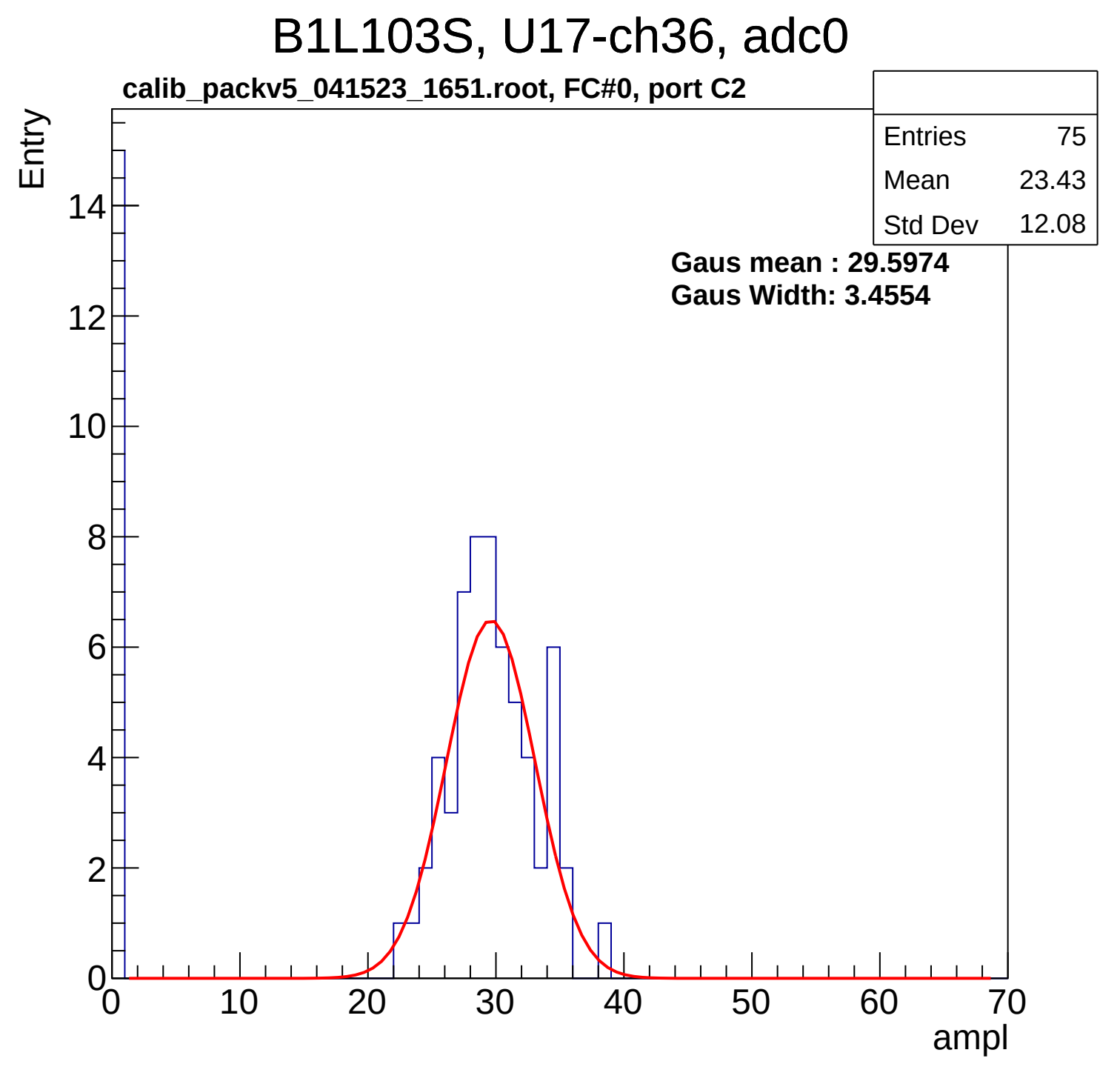

B1L103S, U17-ch35, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 43.57
Std Dev 15.16
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

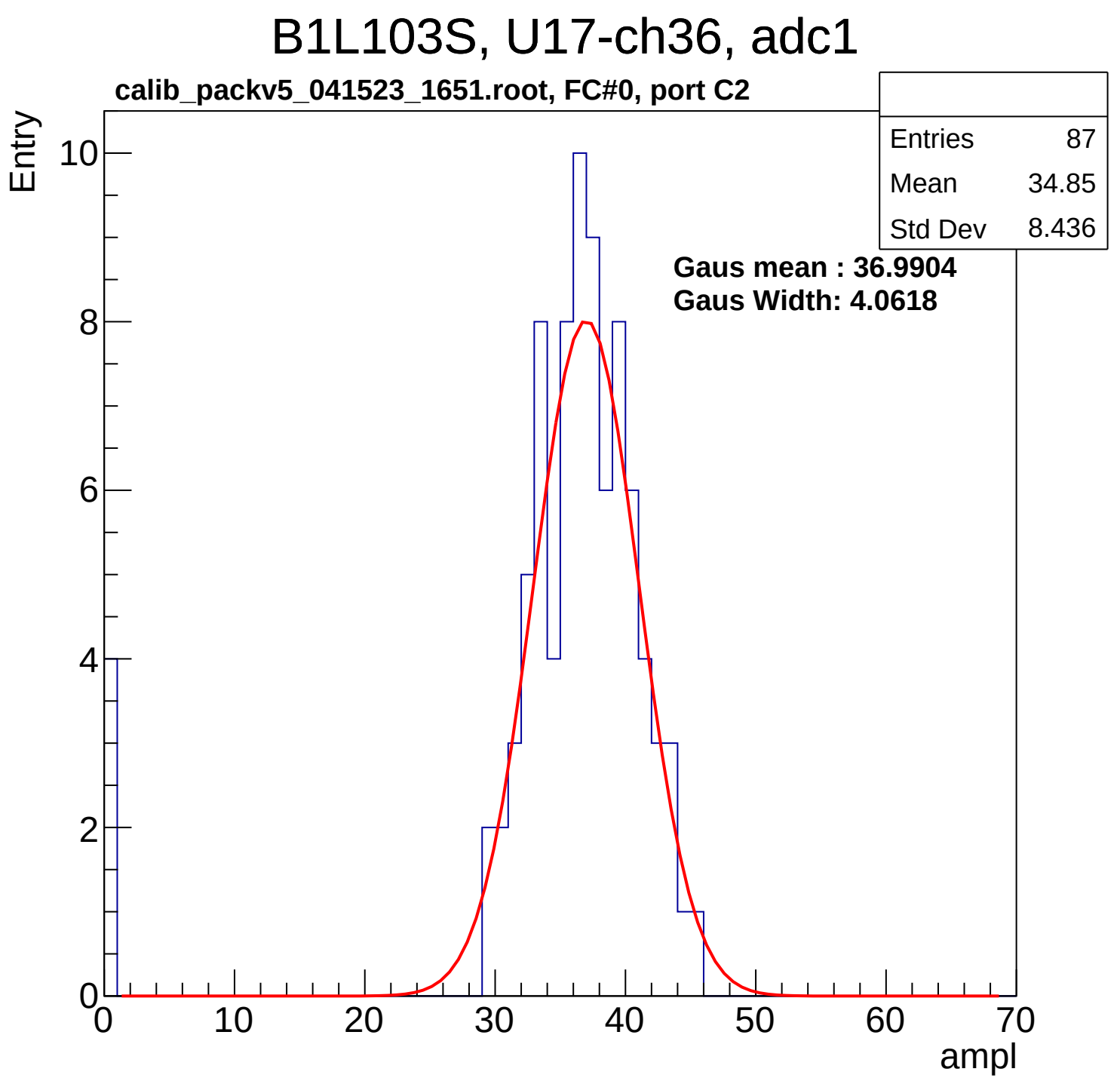

B1L103S, U17-ch35, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 54.13
Std Dev 3.448
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

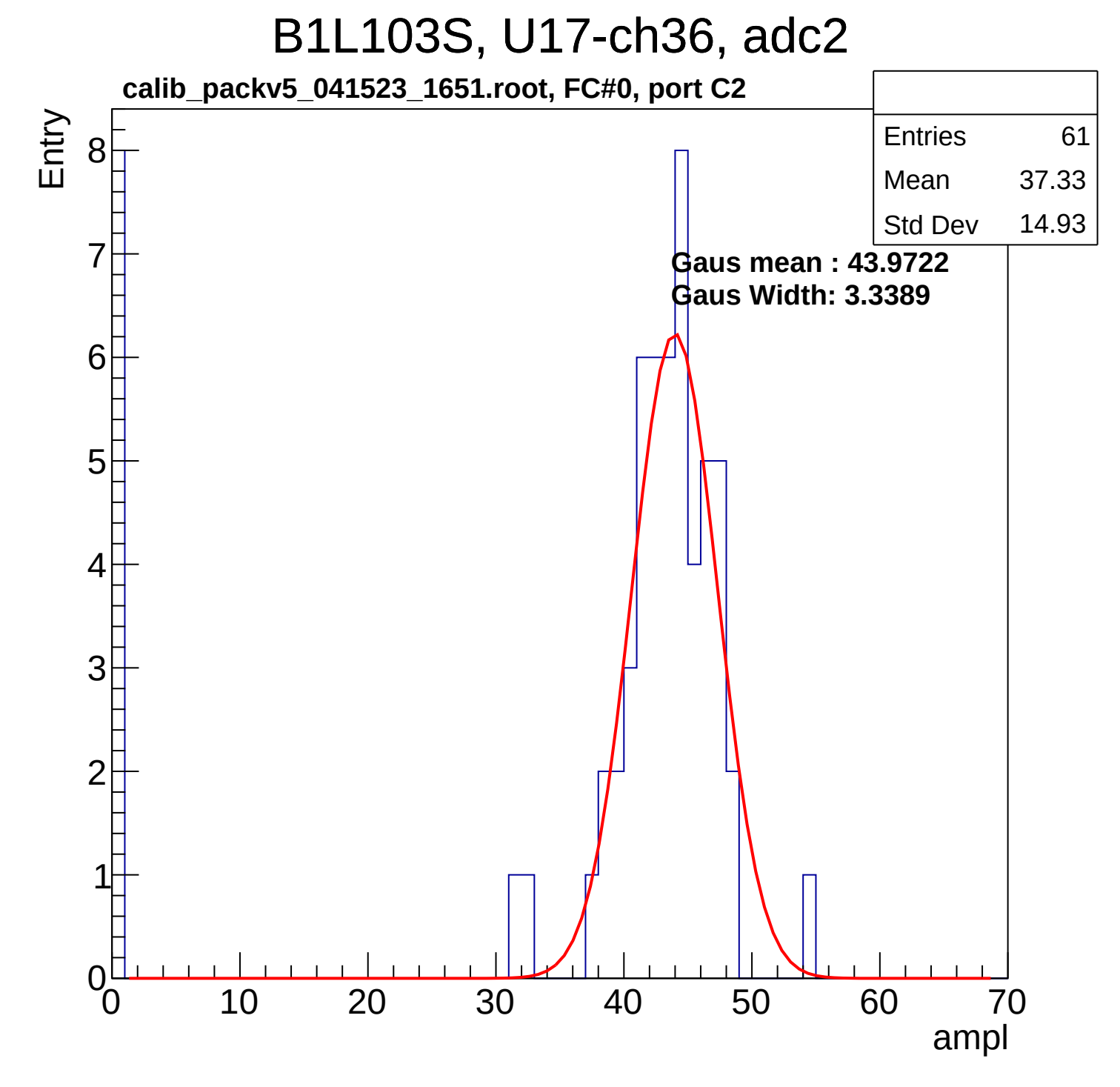

B1L103S, U17-ch35, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 59.1
Std Dev 2.9
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

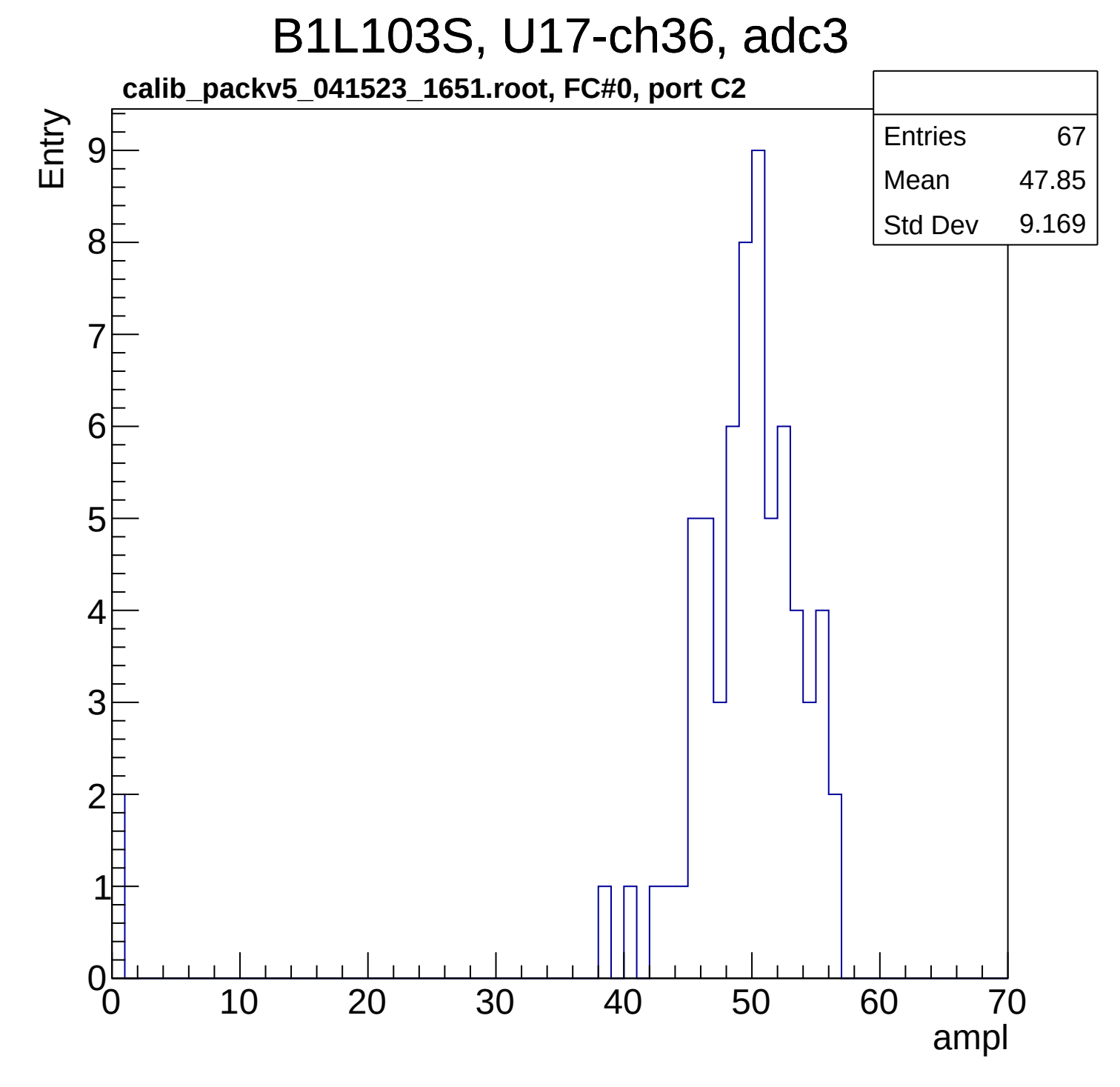

B1L103S, U17-ch35, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 51.67
Std Dev 23.13
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

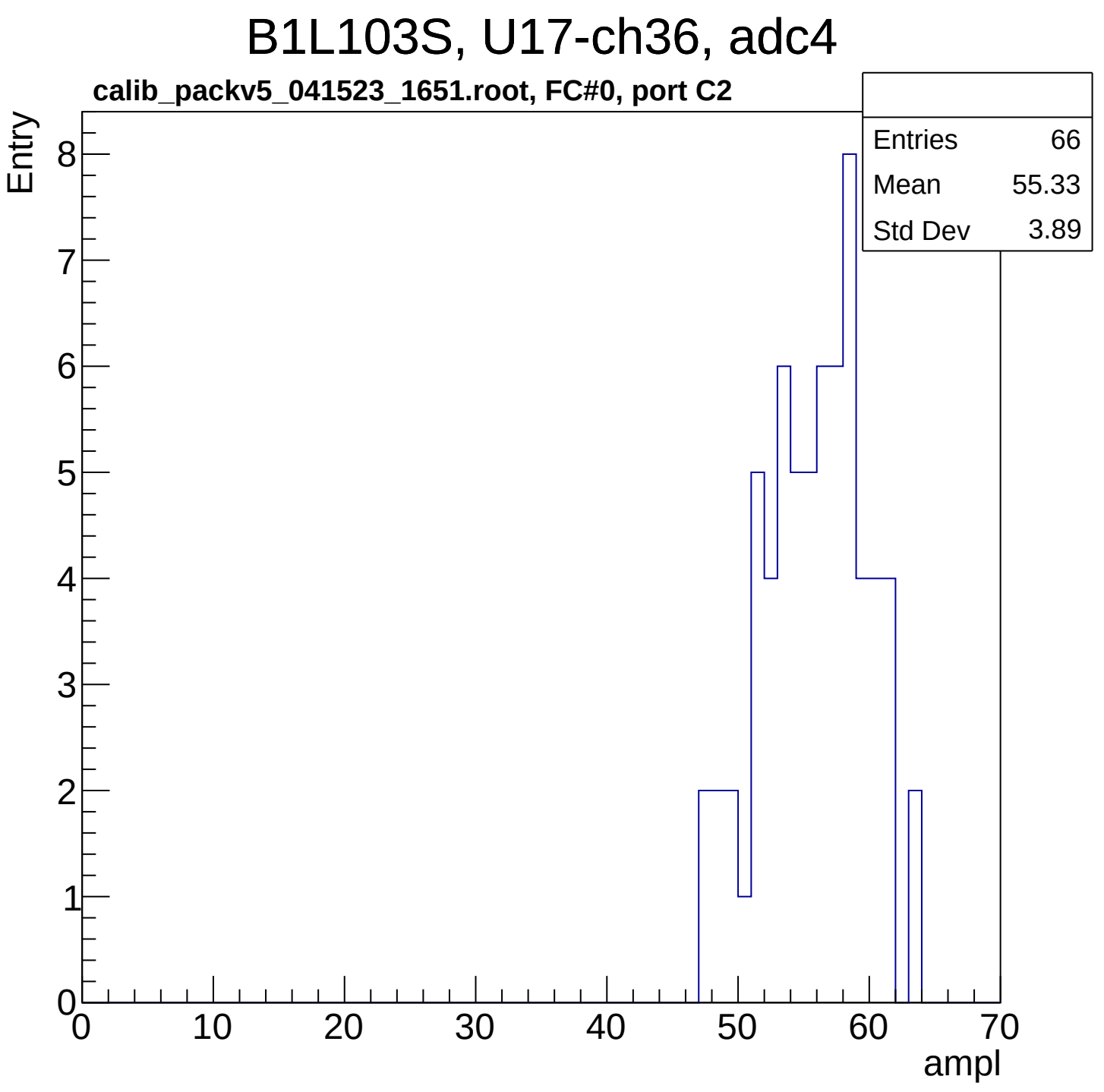

B1L103S, U17-ch35, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1
Std Dev 4.123
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

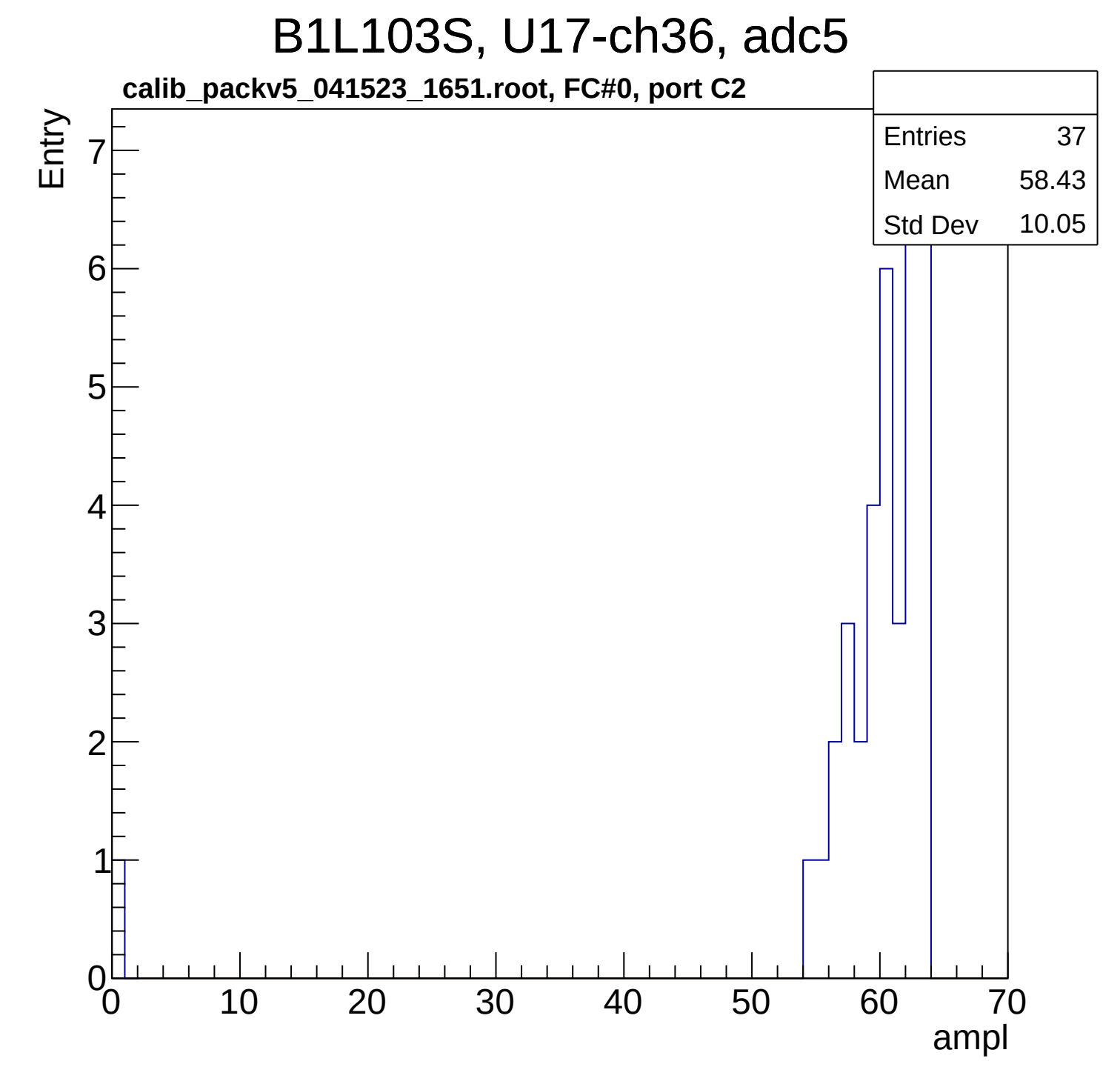

B1L103S, U17-ch36, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 23.43
Std Dev 12.08
Gaus mean : 29.5974
Gaus Width: 3.4554
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

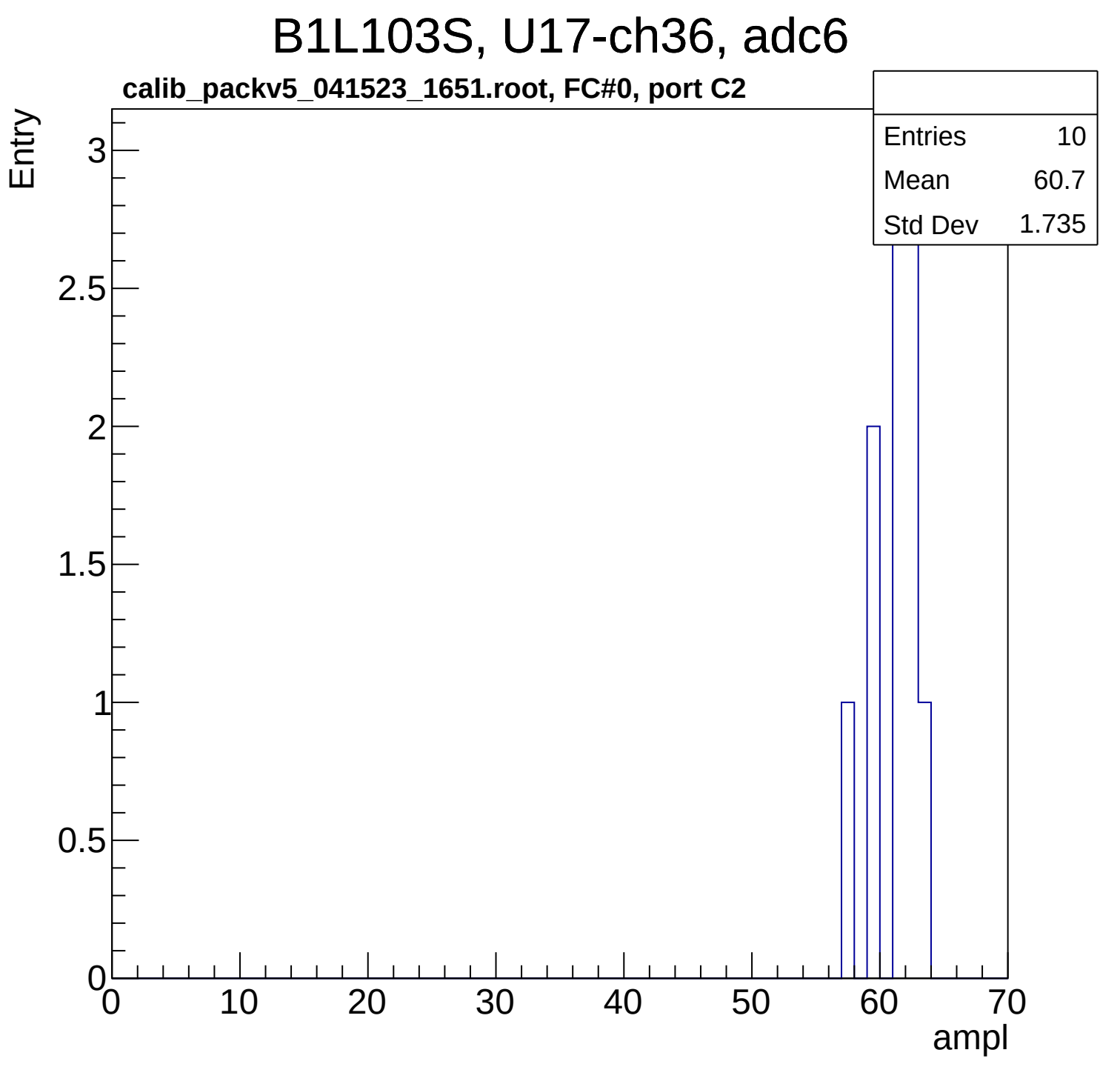

B1L103S, U17-ch36, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 34.85
Std Dev 8.436
Gaus mean : 36.9904
Gaus Width: 4.0618
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

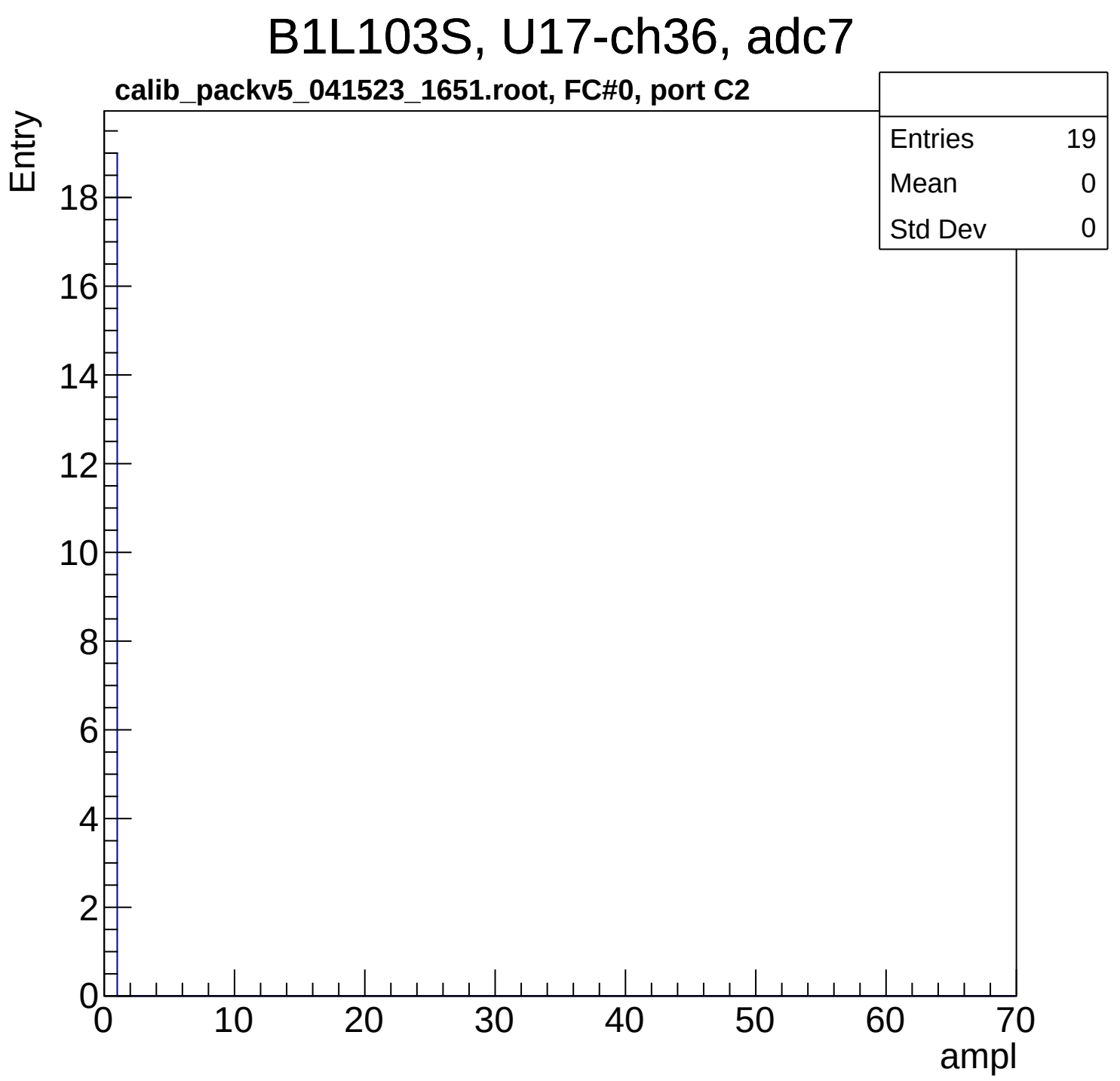

B1L103S, U17-ch36, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 37.33
Std Dev 14.93
Gaus mean : 43.9722
Gaus Width: 3.3389
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

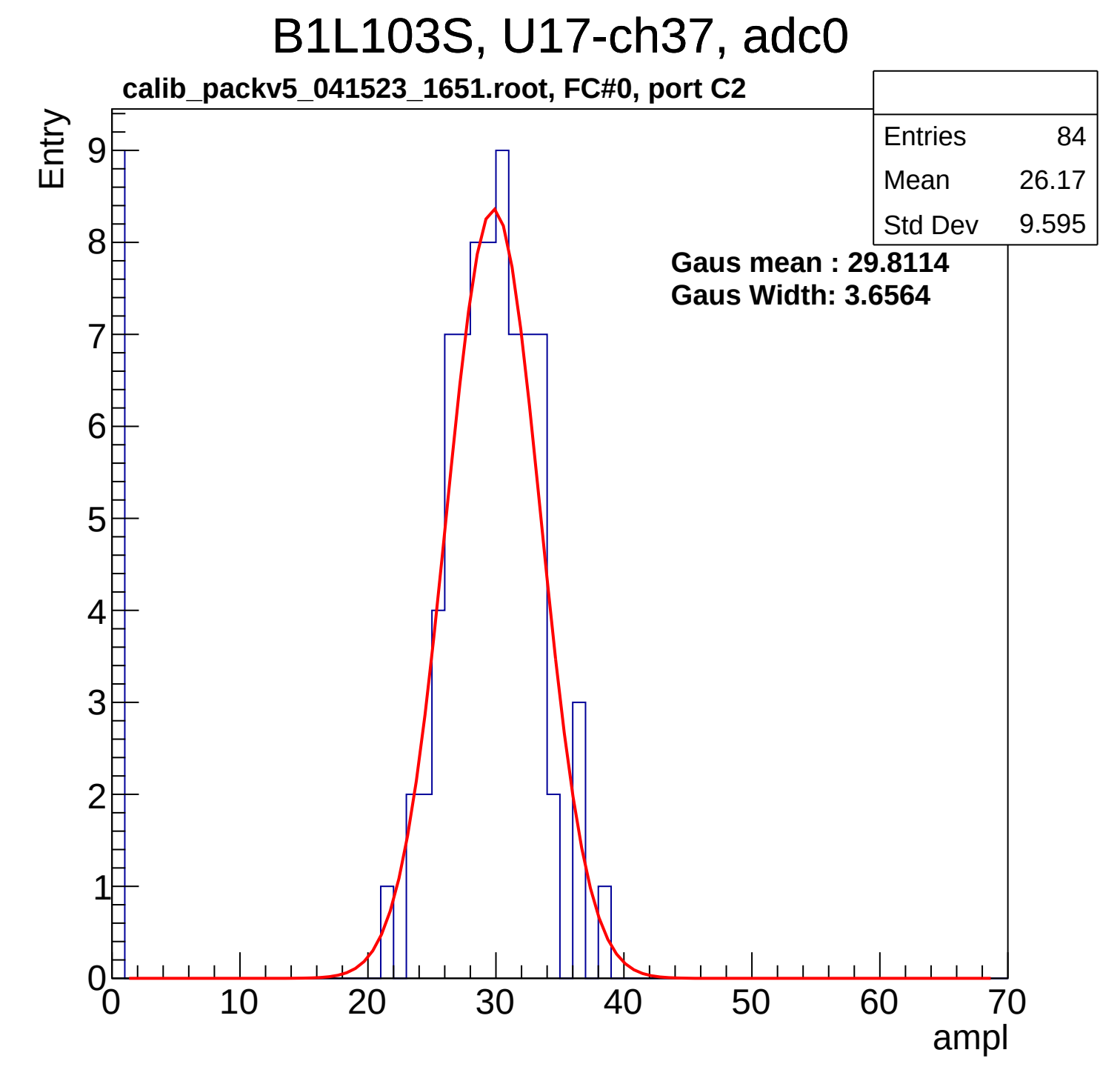

B1L103S, U17-ch36, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 47.85
Std Dev 9.169
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

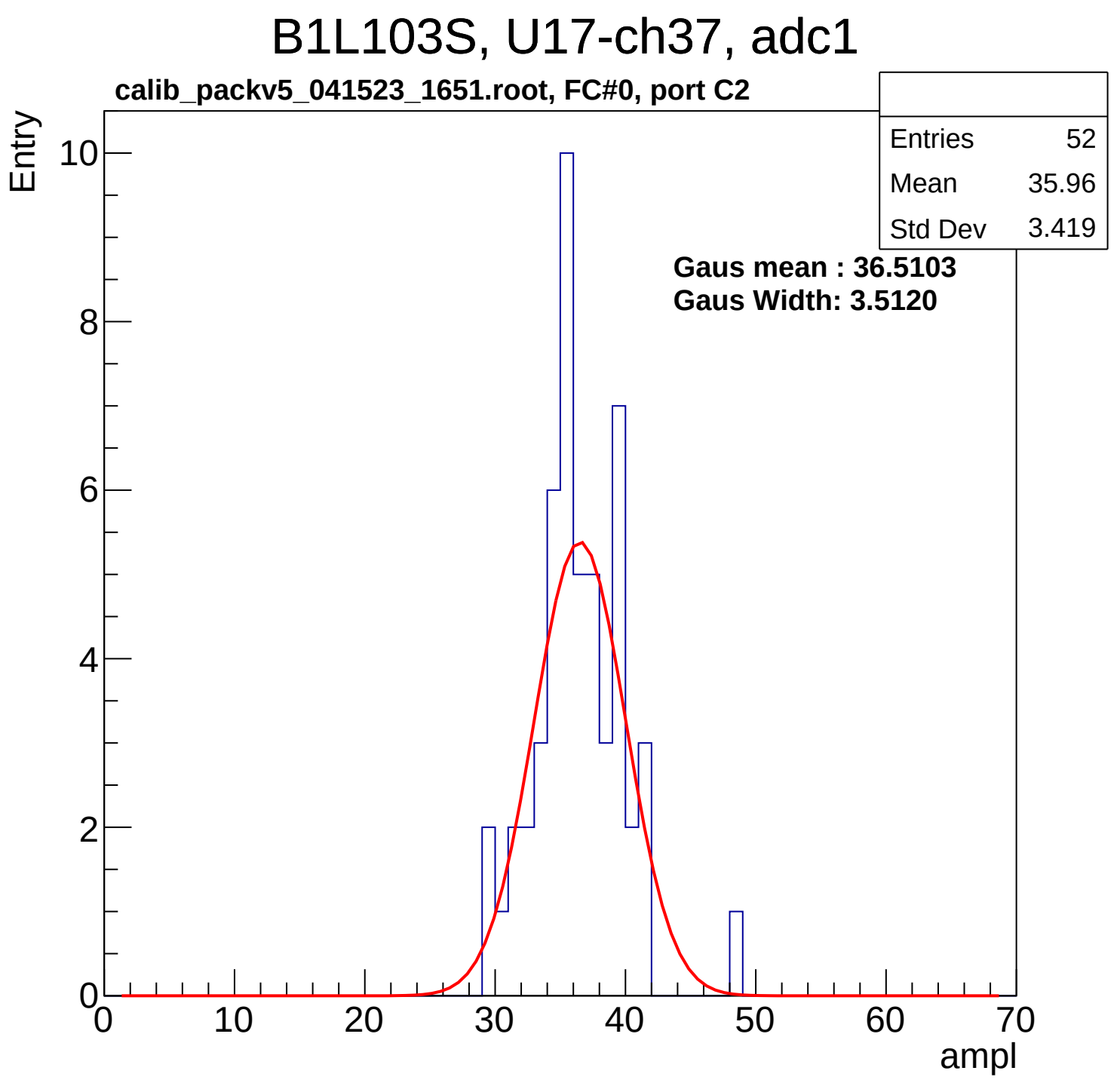

B1L103S, U17-ch36, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 55.33
Std Dev 3.89
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

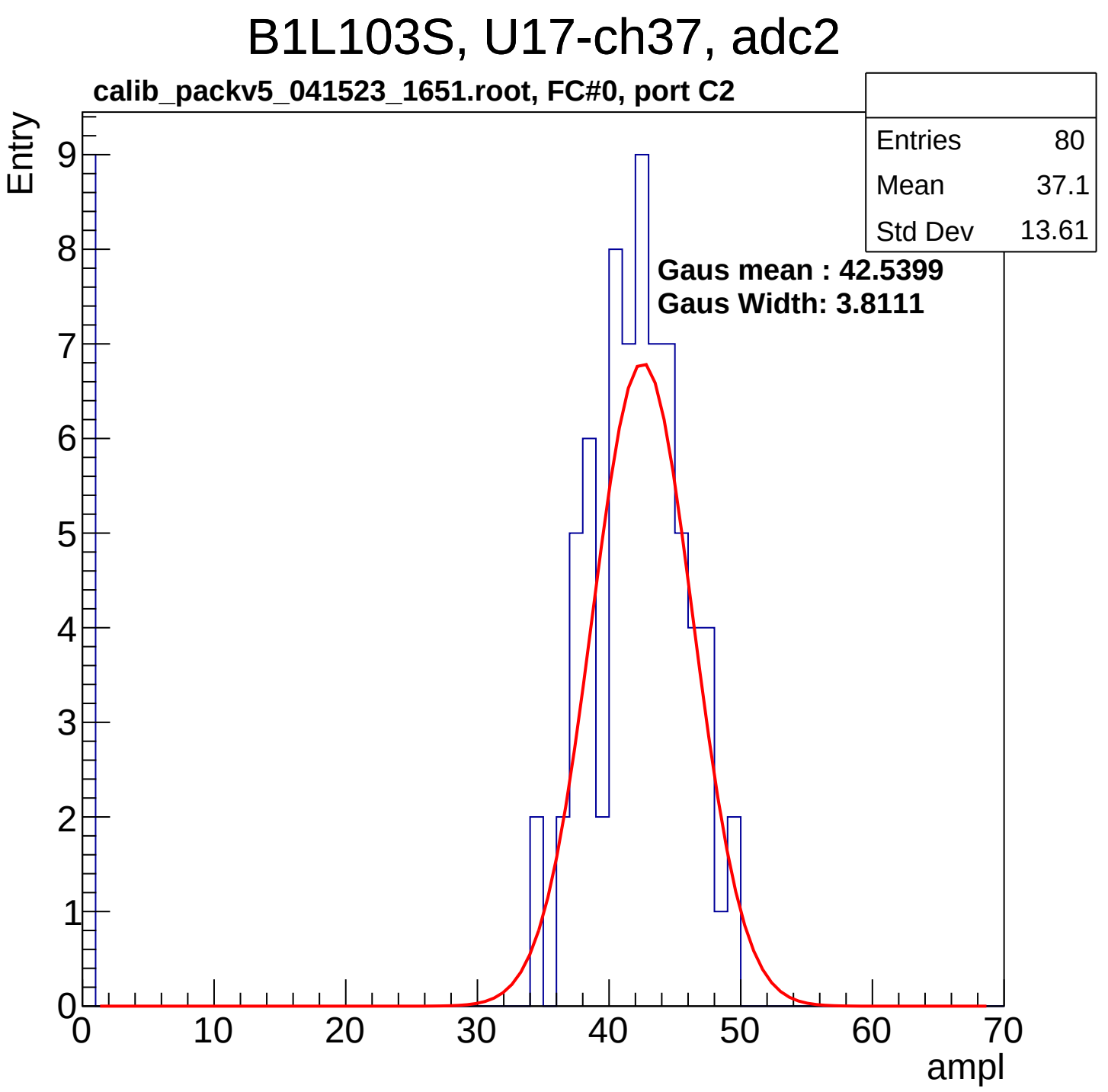

B1L103S, U17-ch36, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 58.43
Std Dev 10.05
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

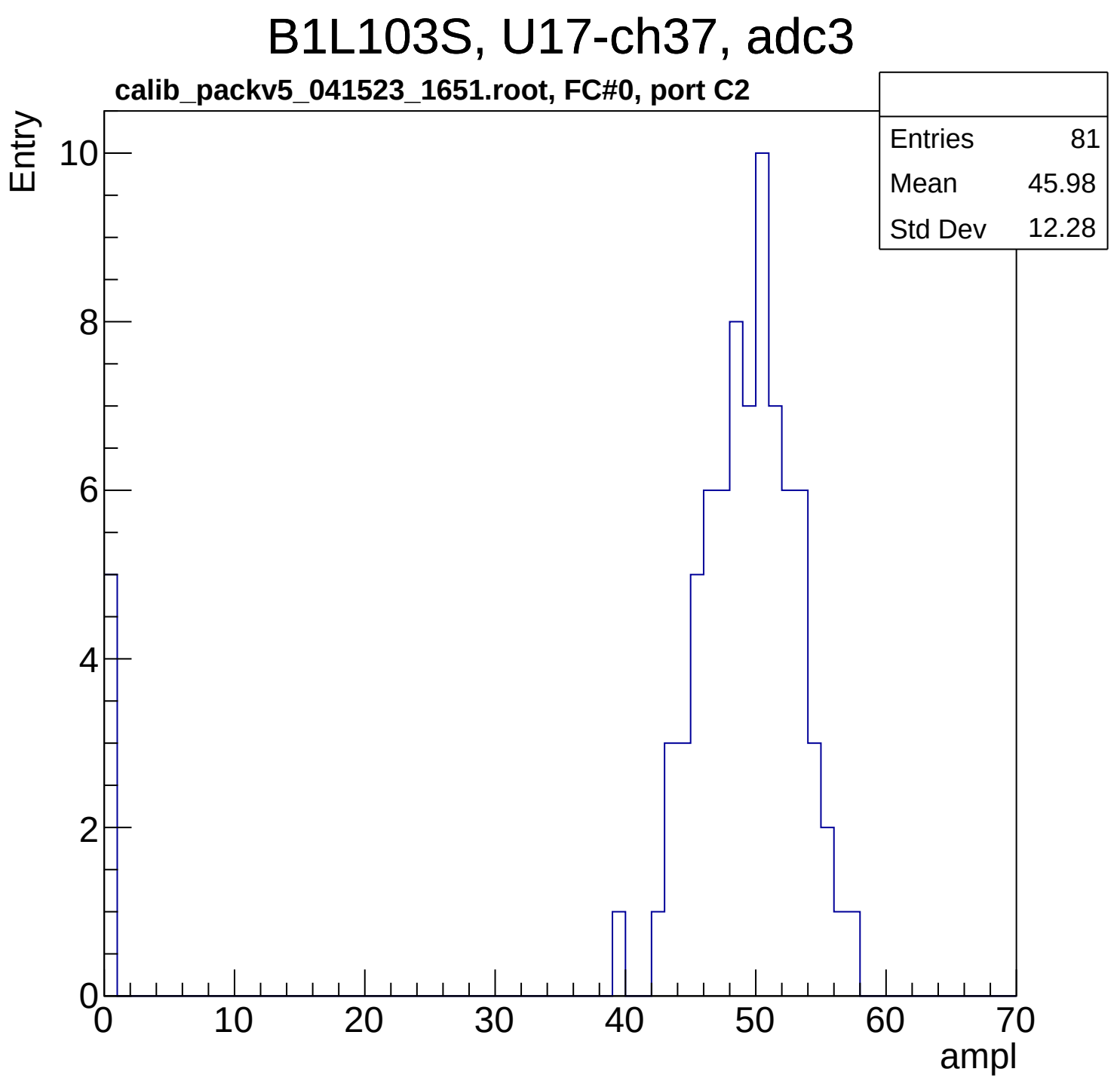

B1L103S, U17-ch36, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 60.7
Std Dev 1.735
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

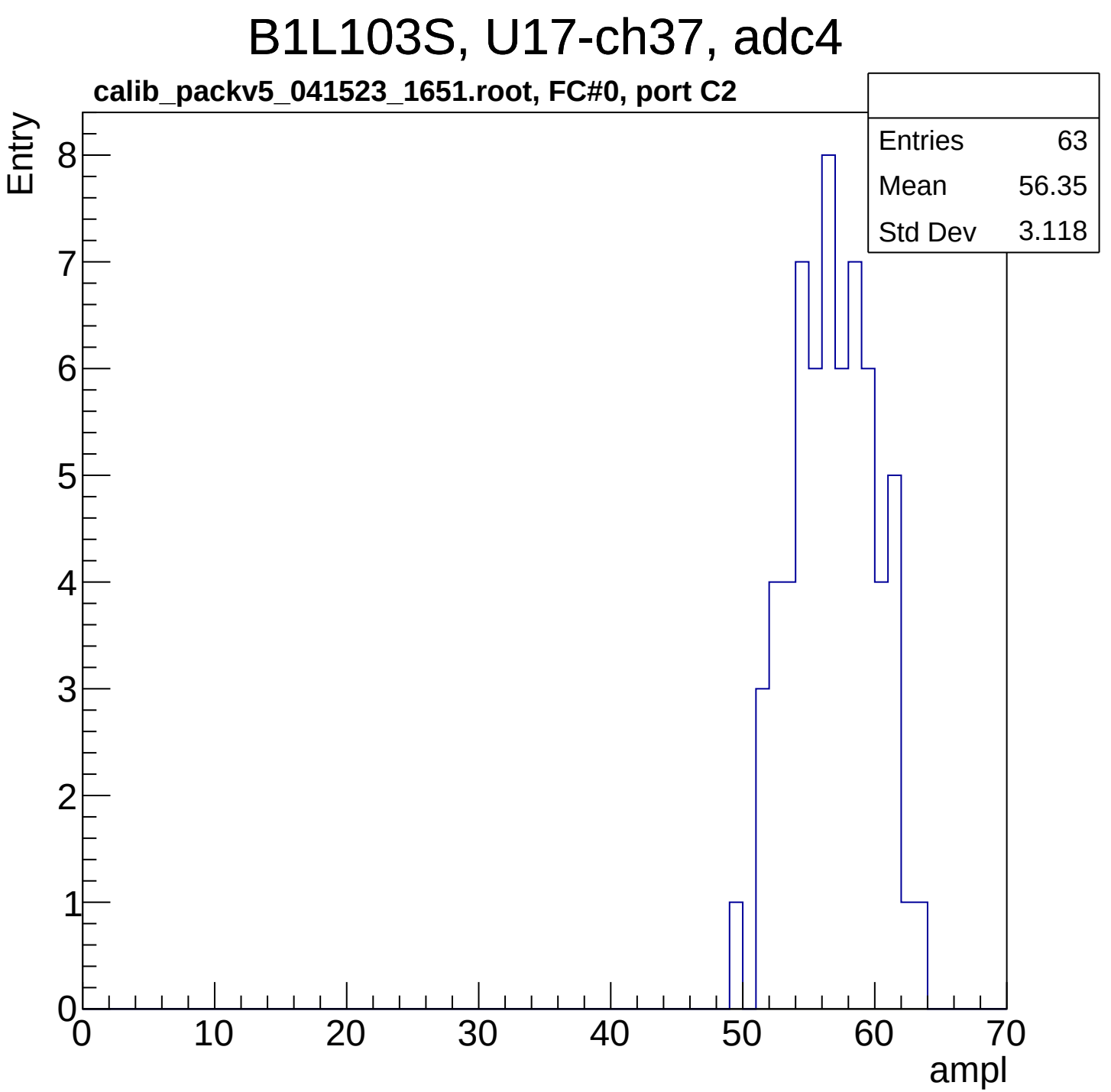

B1L103S, U17-ch36, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

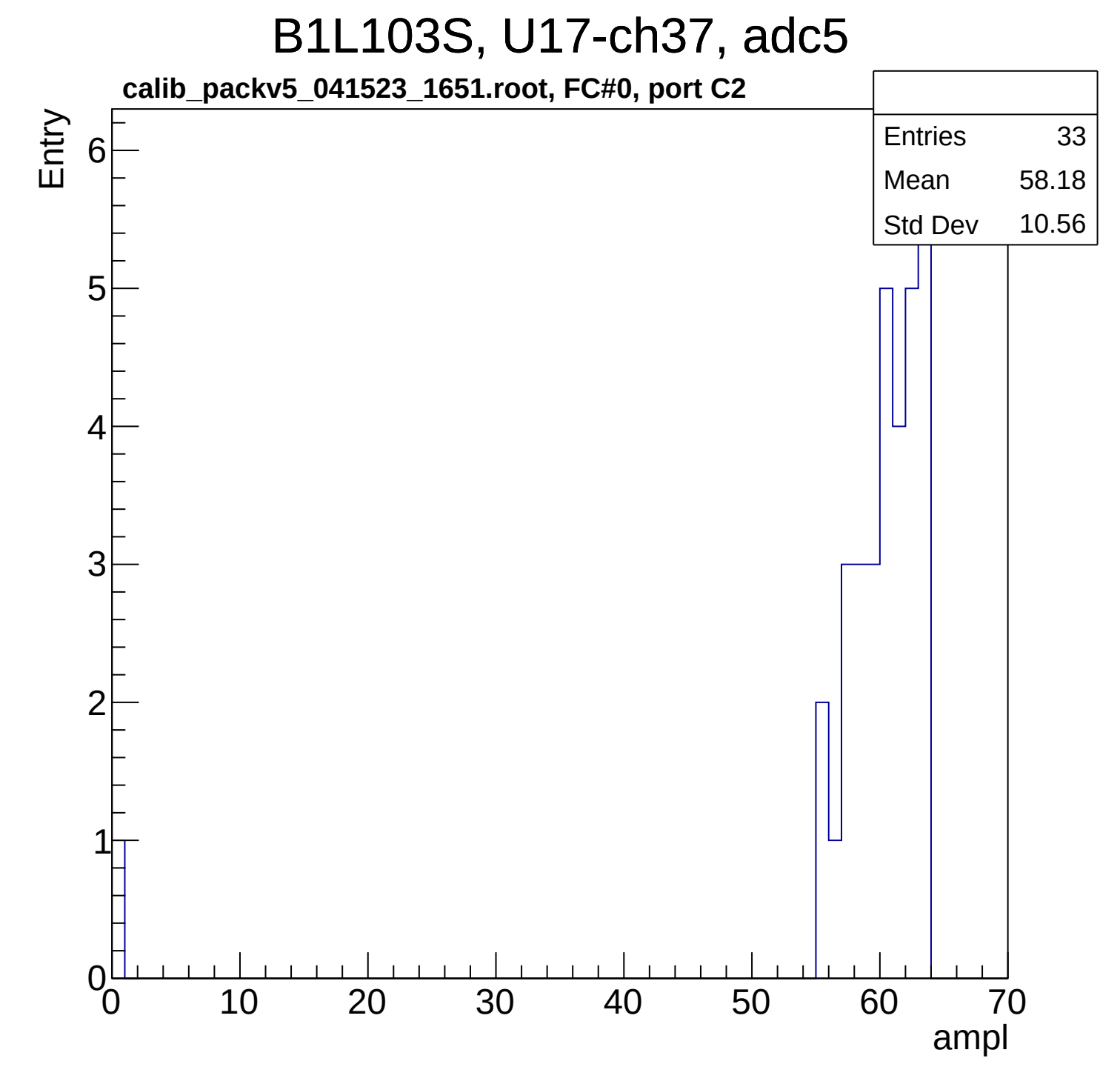

B1L103S, U17-ch37, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 26.17
Std Dev 9.595
Gaus mean : 29.8114
Gaus Width: 3.6564
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

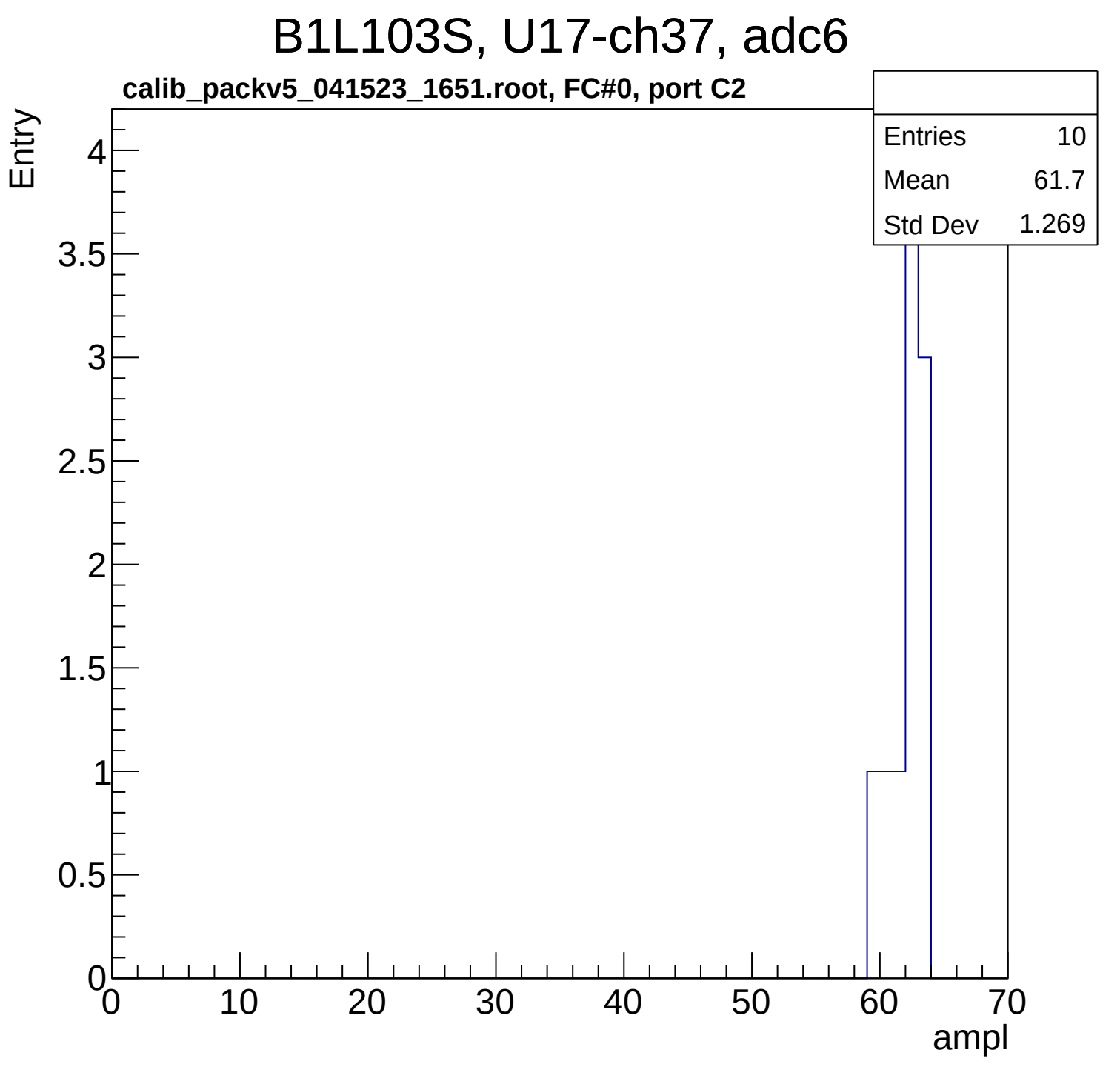

B1L103S, U17-ch37, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 35.96
Std Dev 3.419
Gaus mean : 36.5103
Gaus Width: 3.5120
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

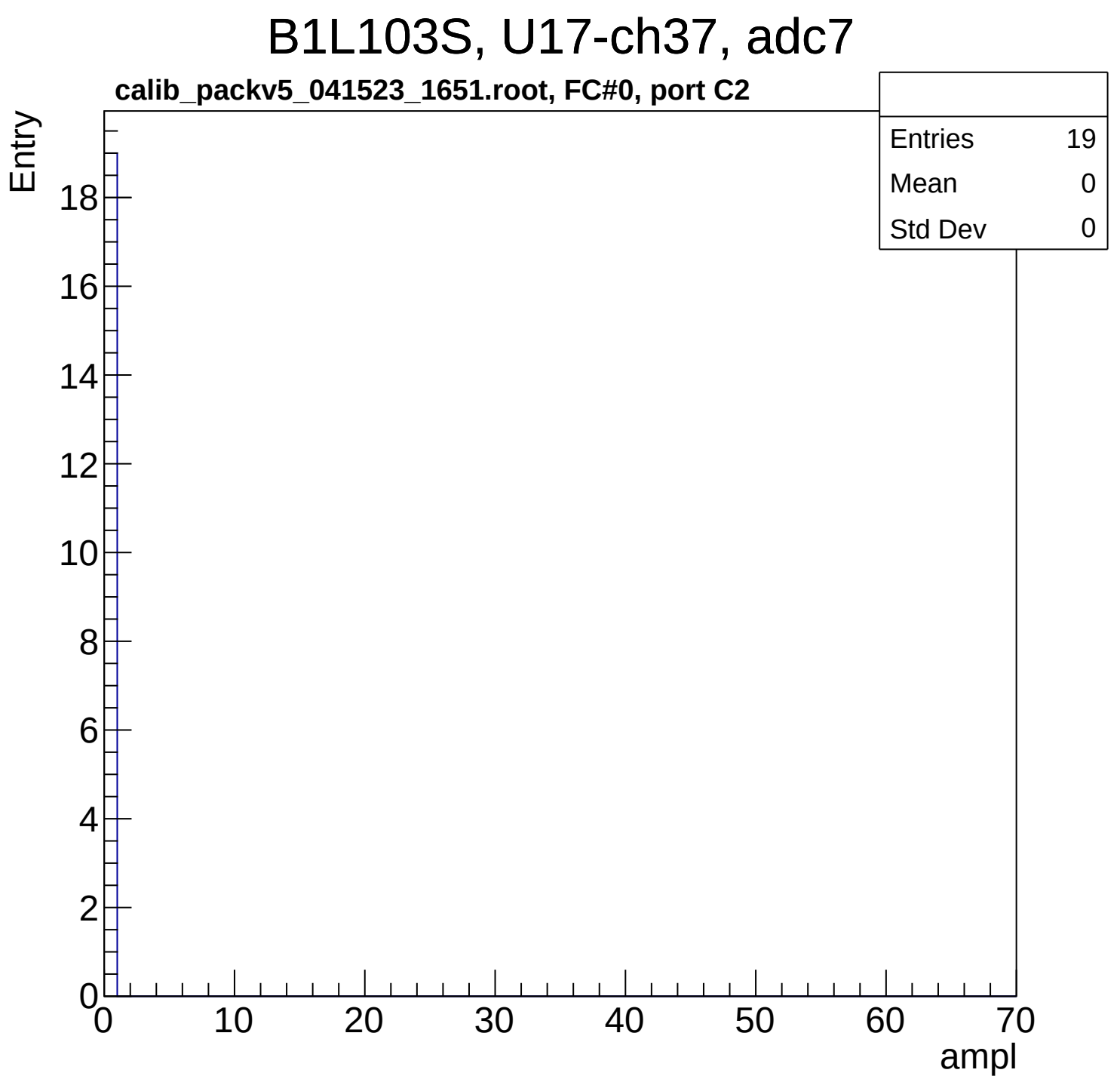

B1L103S, U17-ch37, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 37.1
Std Dev 13.61
Gaus mean : 42.5399
Gaus Width: 3.8111
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

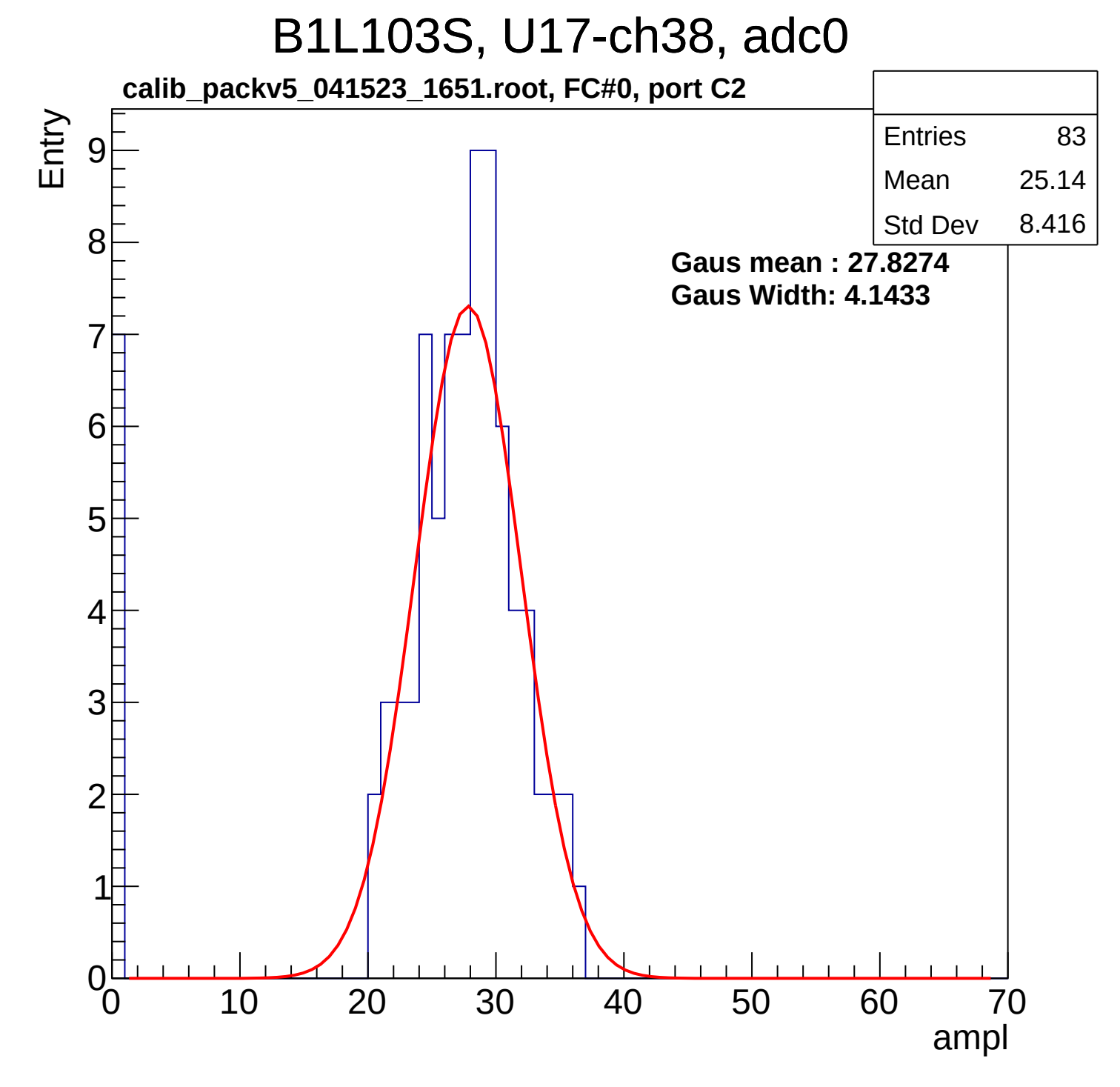

B1L103S, U17-ch37, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 45.98
Std Dev 12.28
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

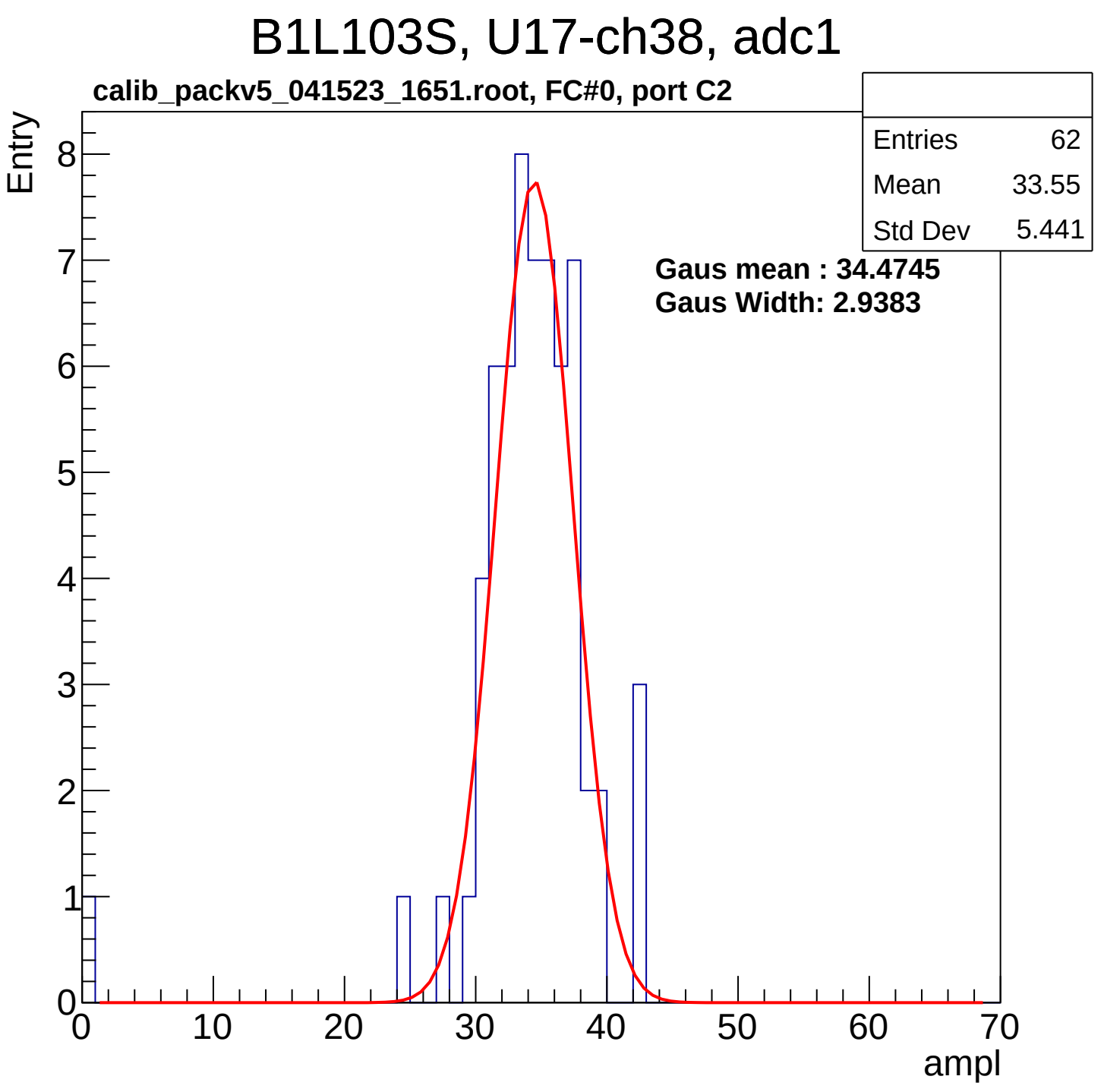

B1L103S, U17-ch37, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 56.35
Std Dev 3.118
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

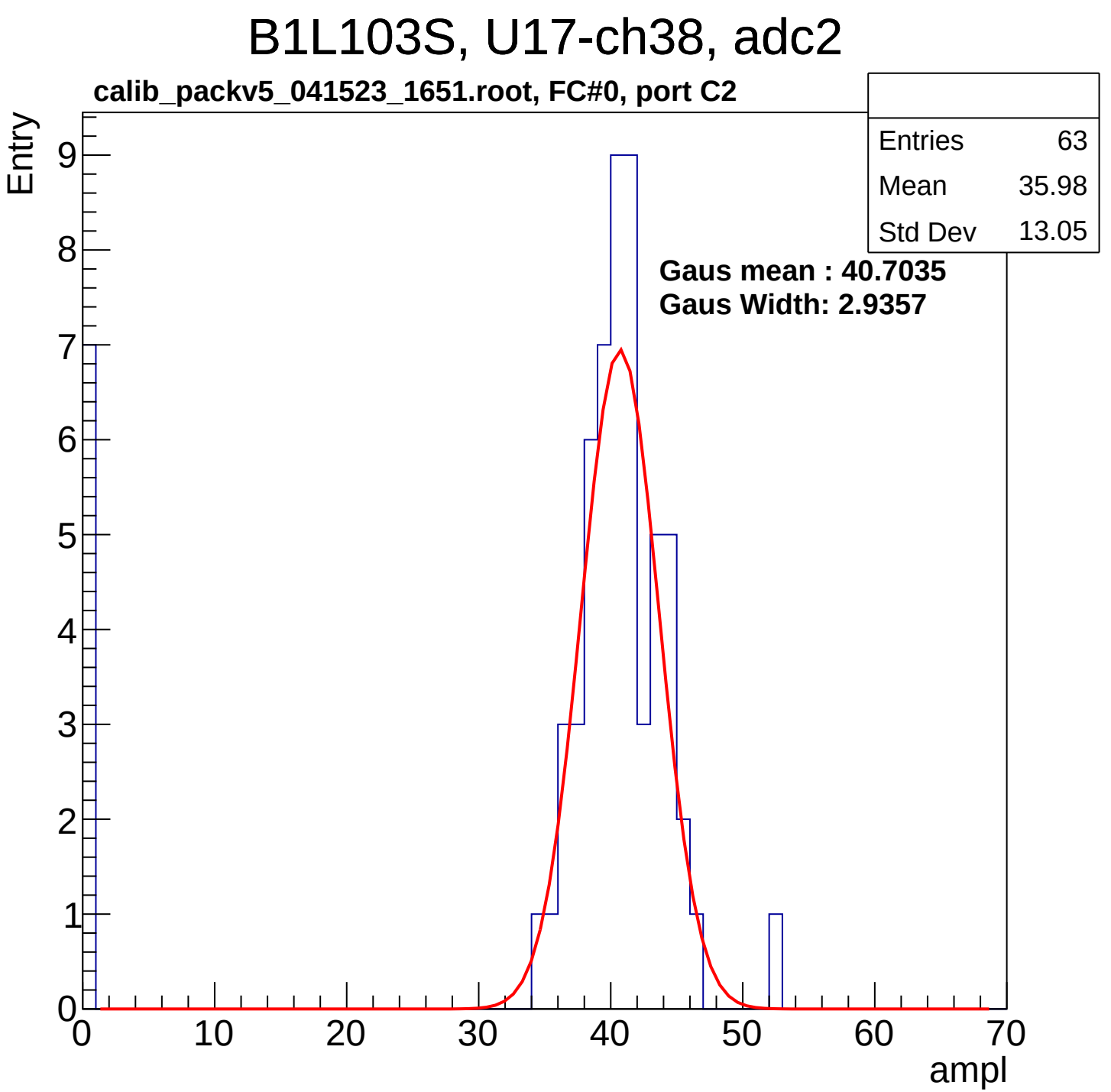

B1L103S, U17-ch37, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 58.18
Std Dev 10.56
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

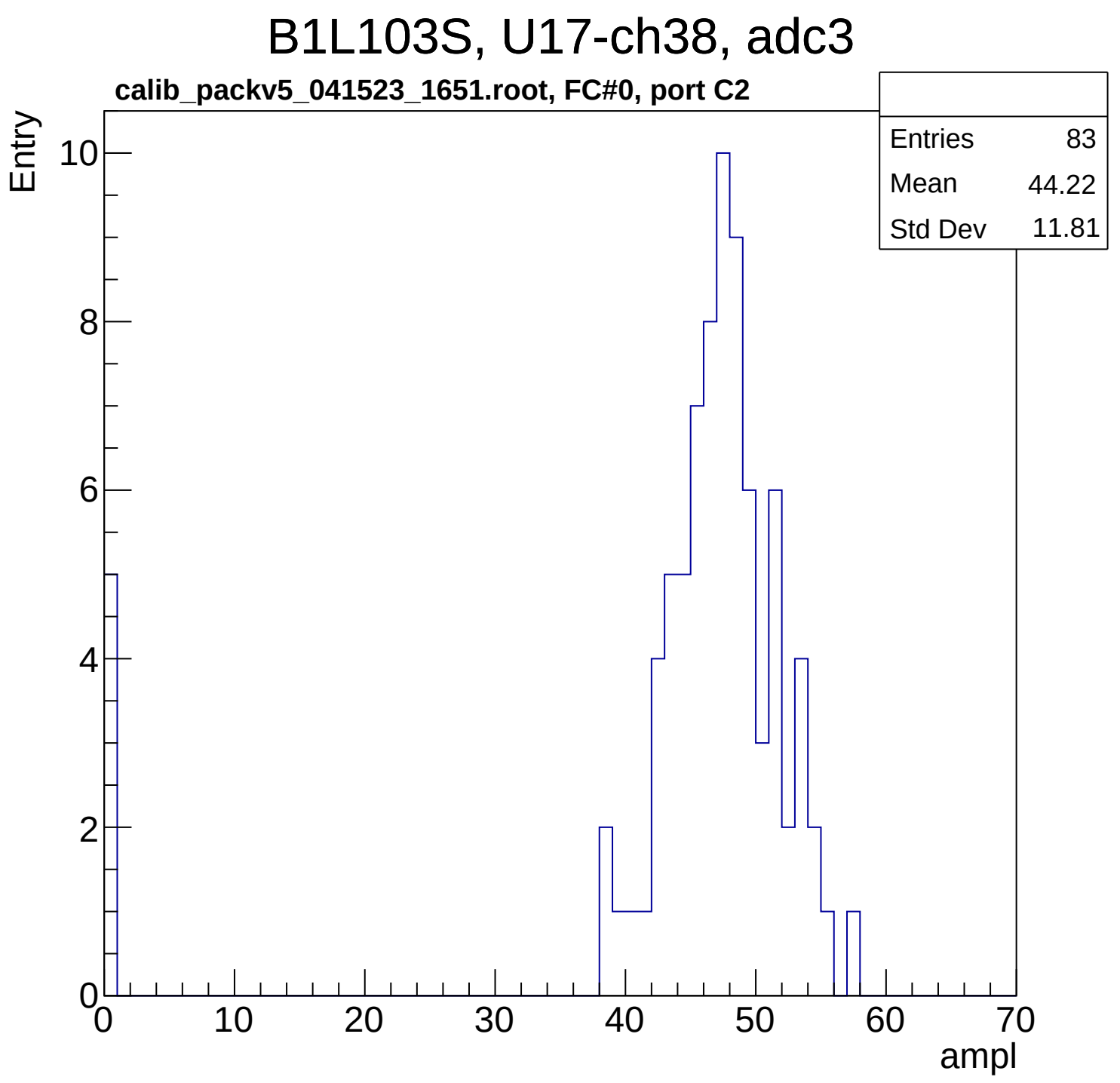

B1L103S, U17-ch37, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.7
Std Dev 1.269
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

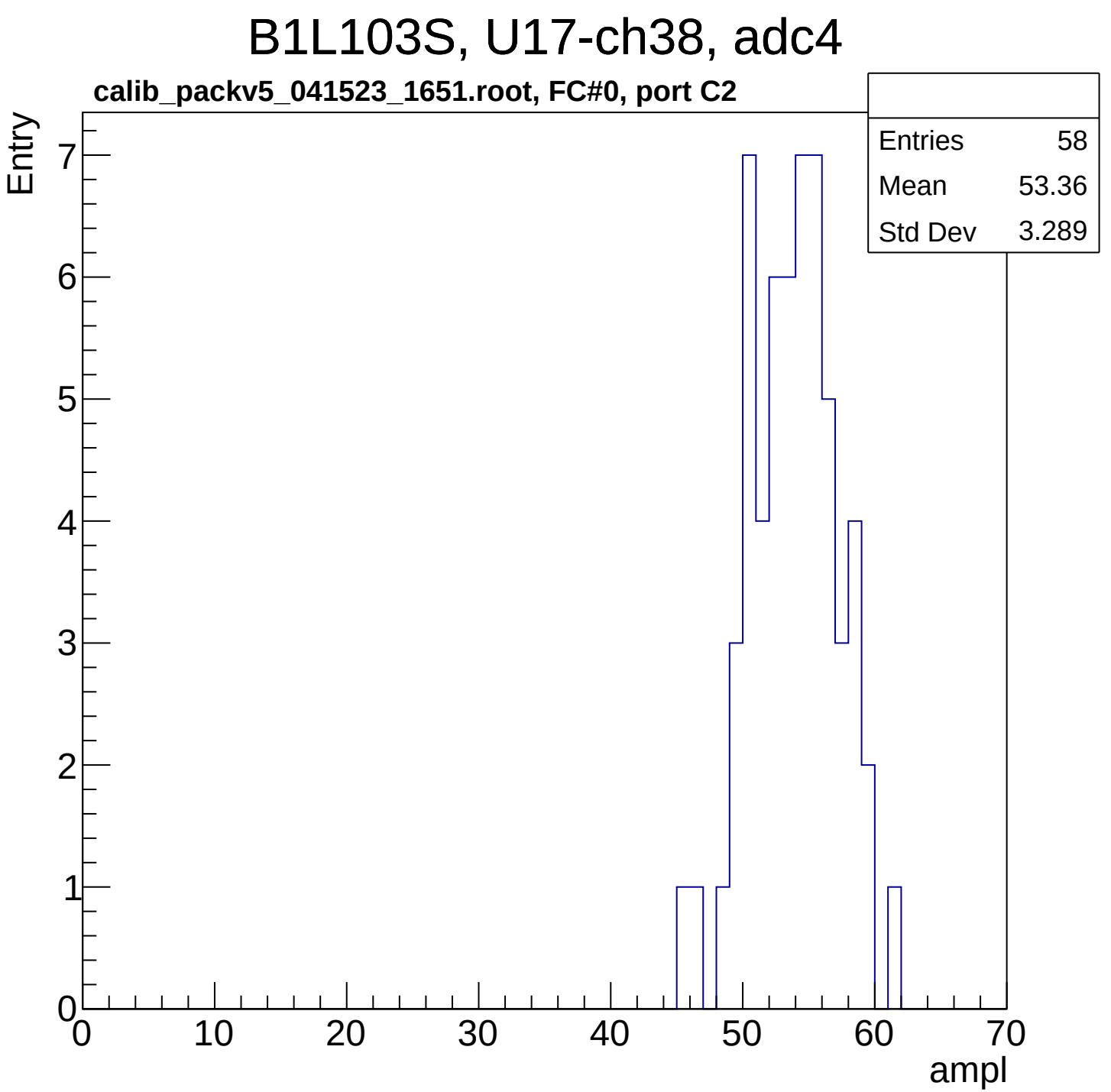

B1L103S, U17-ch37, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

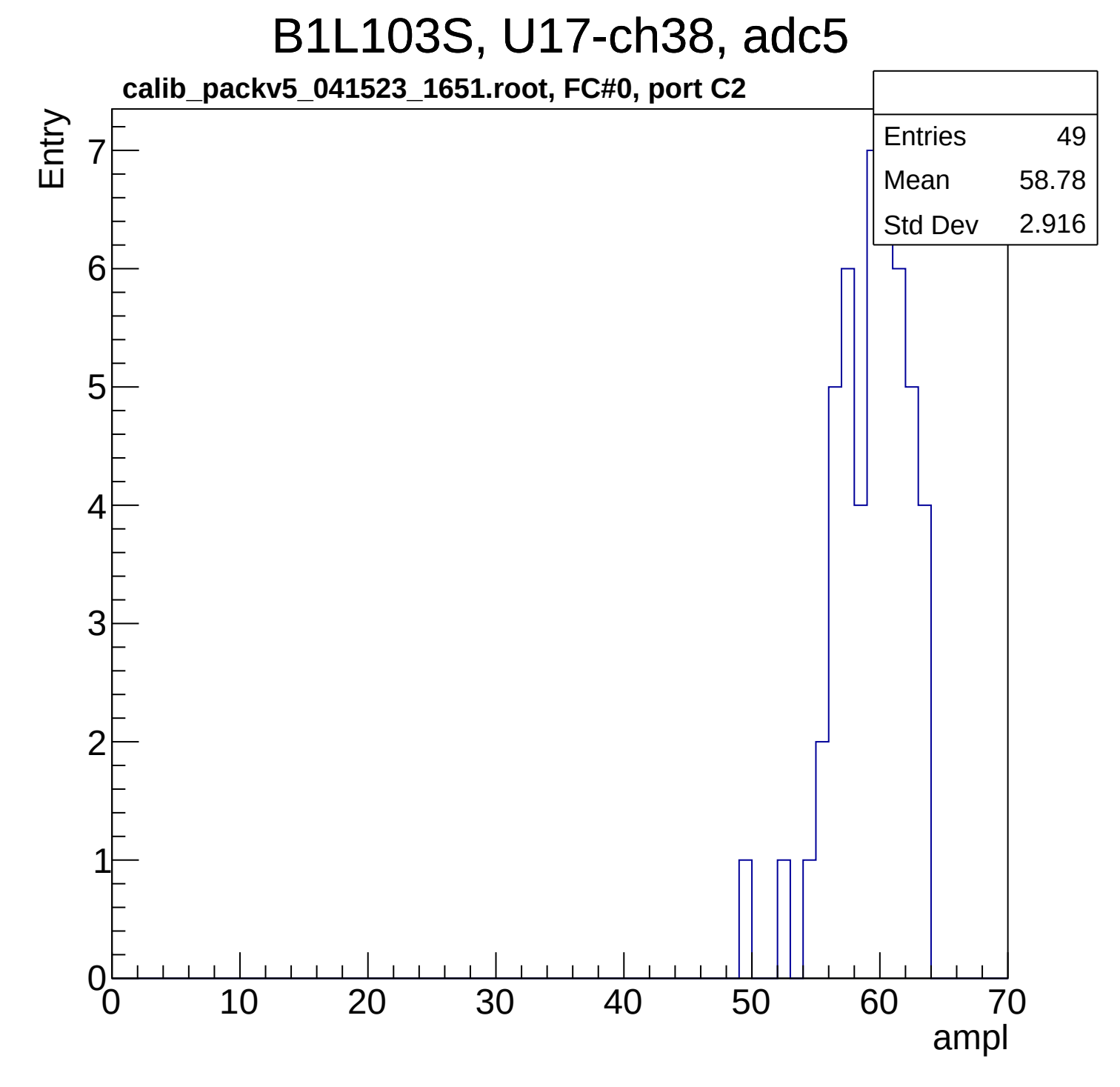

B1L103S, U17-ch38, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 25.14
Std Dev 8.416
Gaus mean : 27.8274
Gaus Width: 4.1433
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

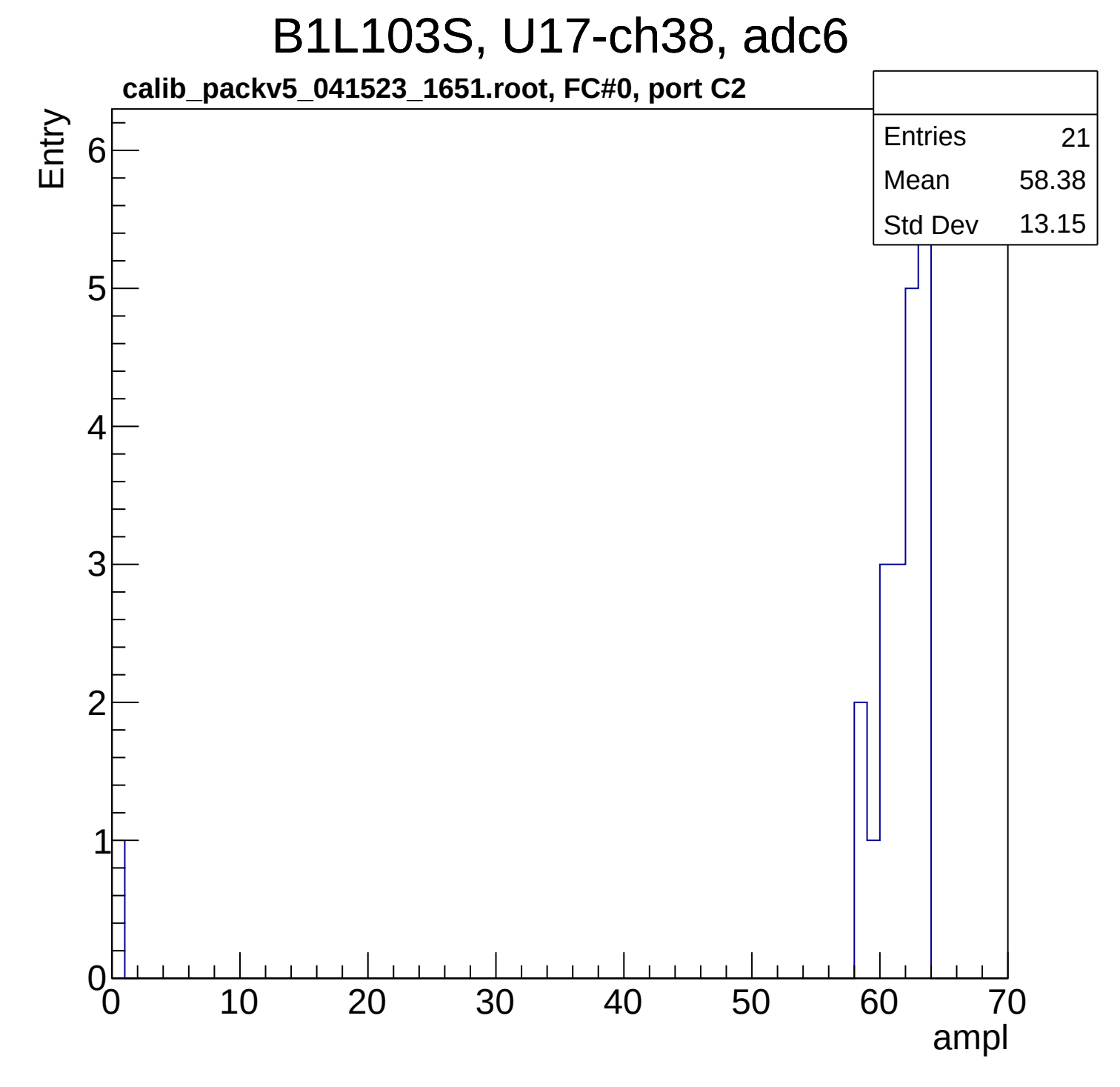

B1L103S, U17-ch38, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 33.55
Std Dev 5.441
Gaus mean : 34.4745
Gaus Width: 2.9383
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

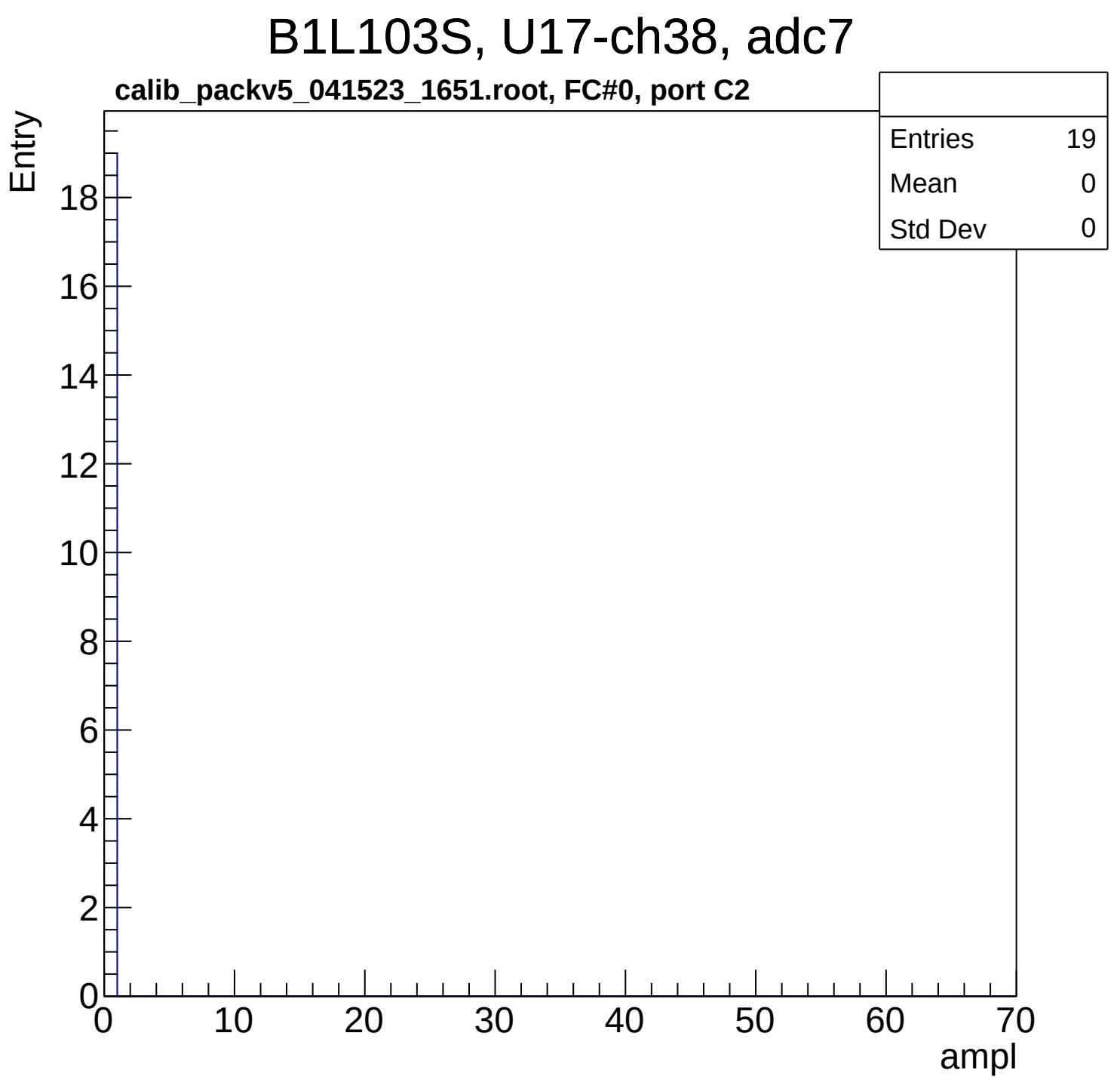

B1L103S, U17-ch38, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 35.98
Std Dev 13.05
Gaus mean : 40.7035
Gaus Width: 2.9357
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

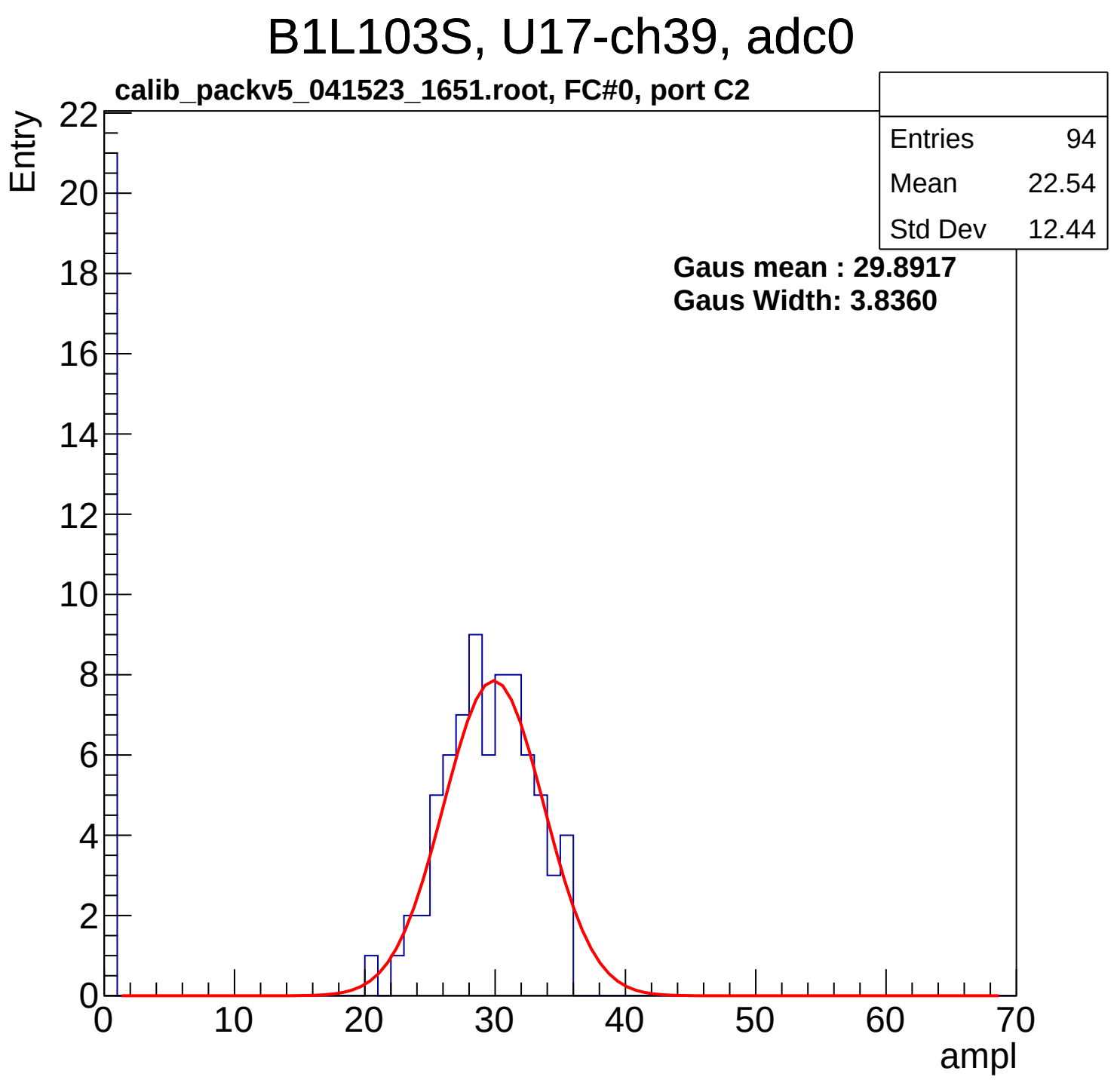

B1L103S, U17-ch38, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 44.22
Std Dev 11.81
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

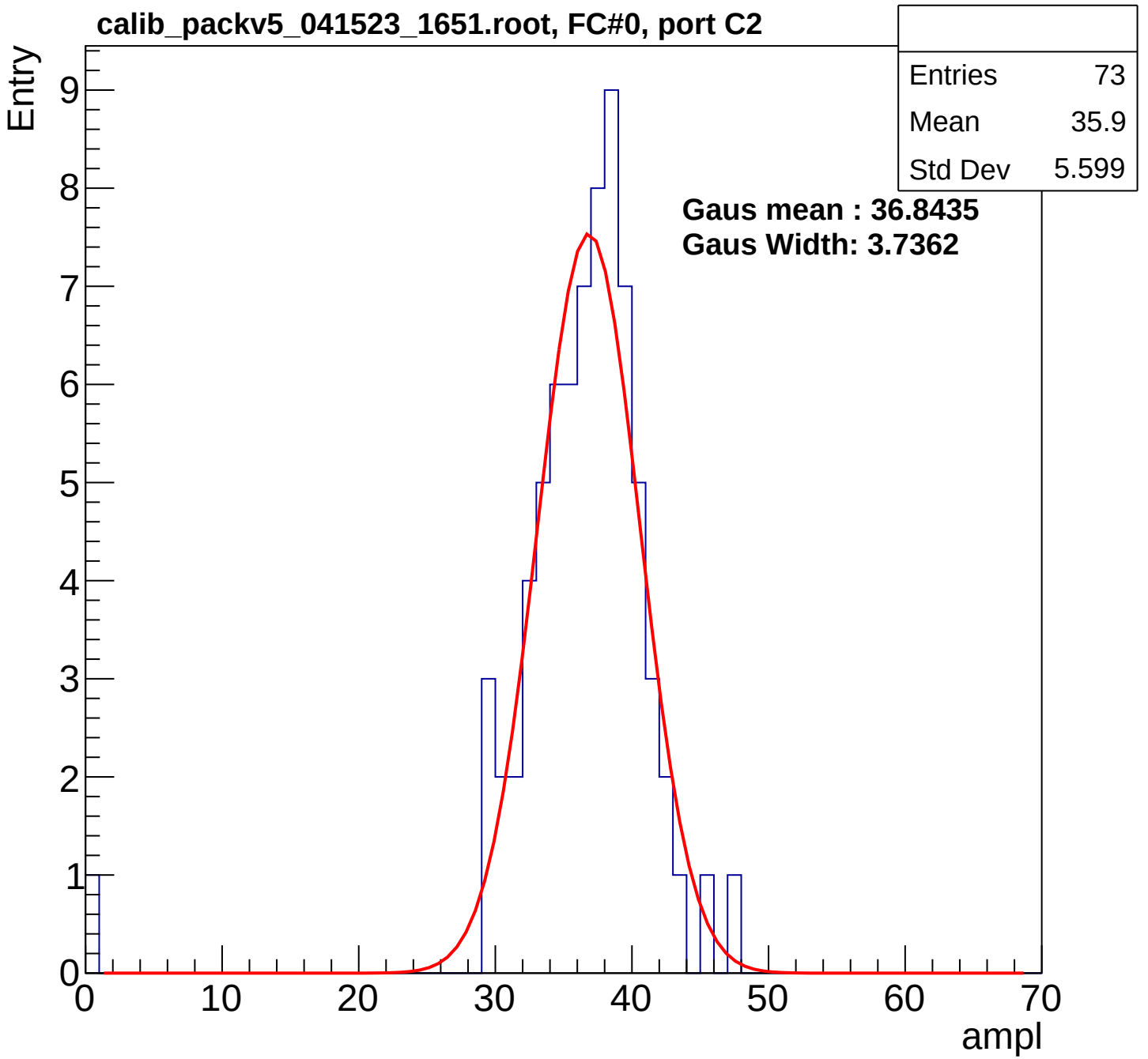

B1L103S, U17-ch38, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 53.36
Std Dev 3.289
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

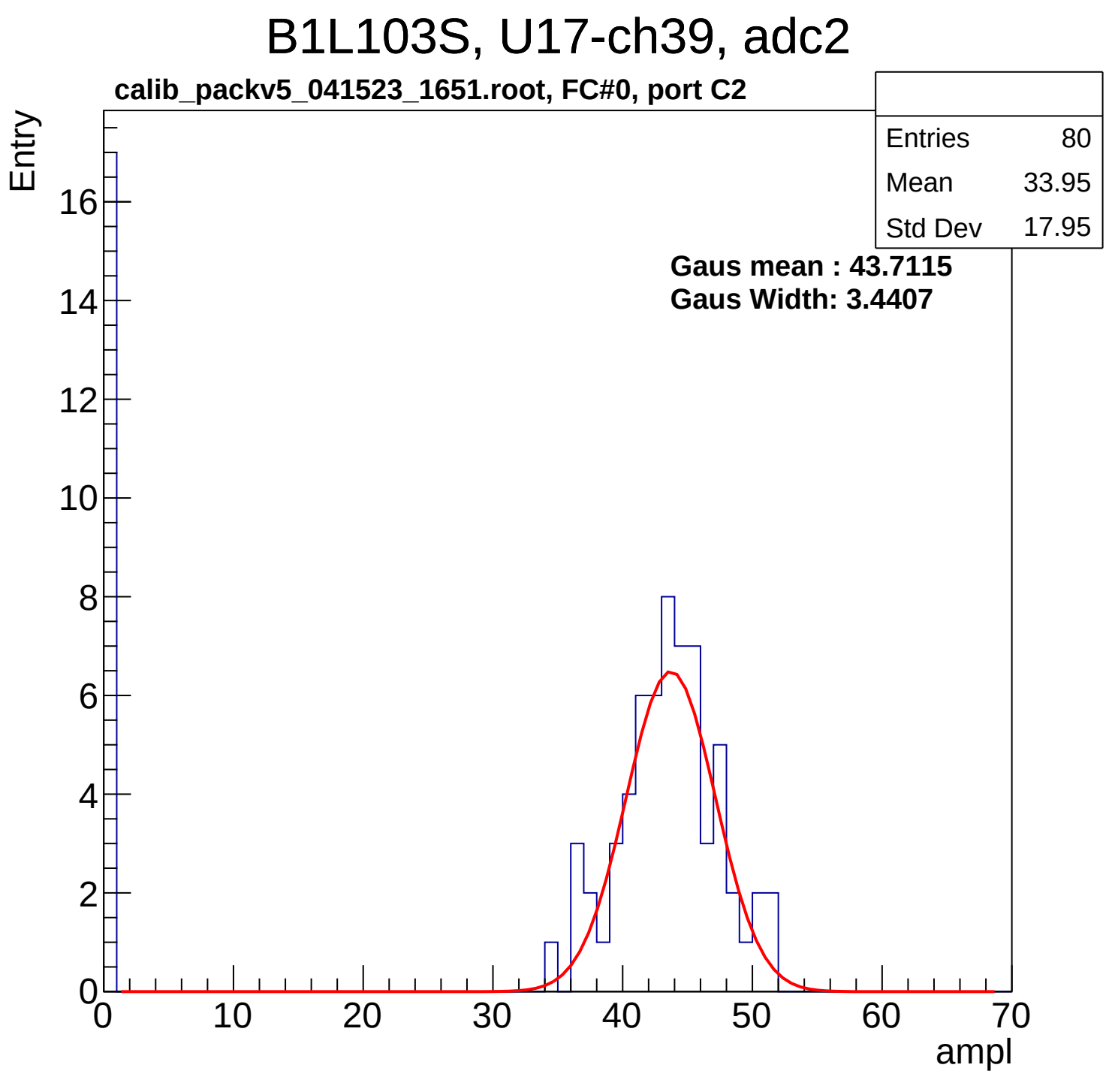

B1L103S, U17-ch38, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.78
Std Dev 2.916
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

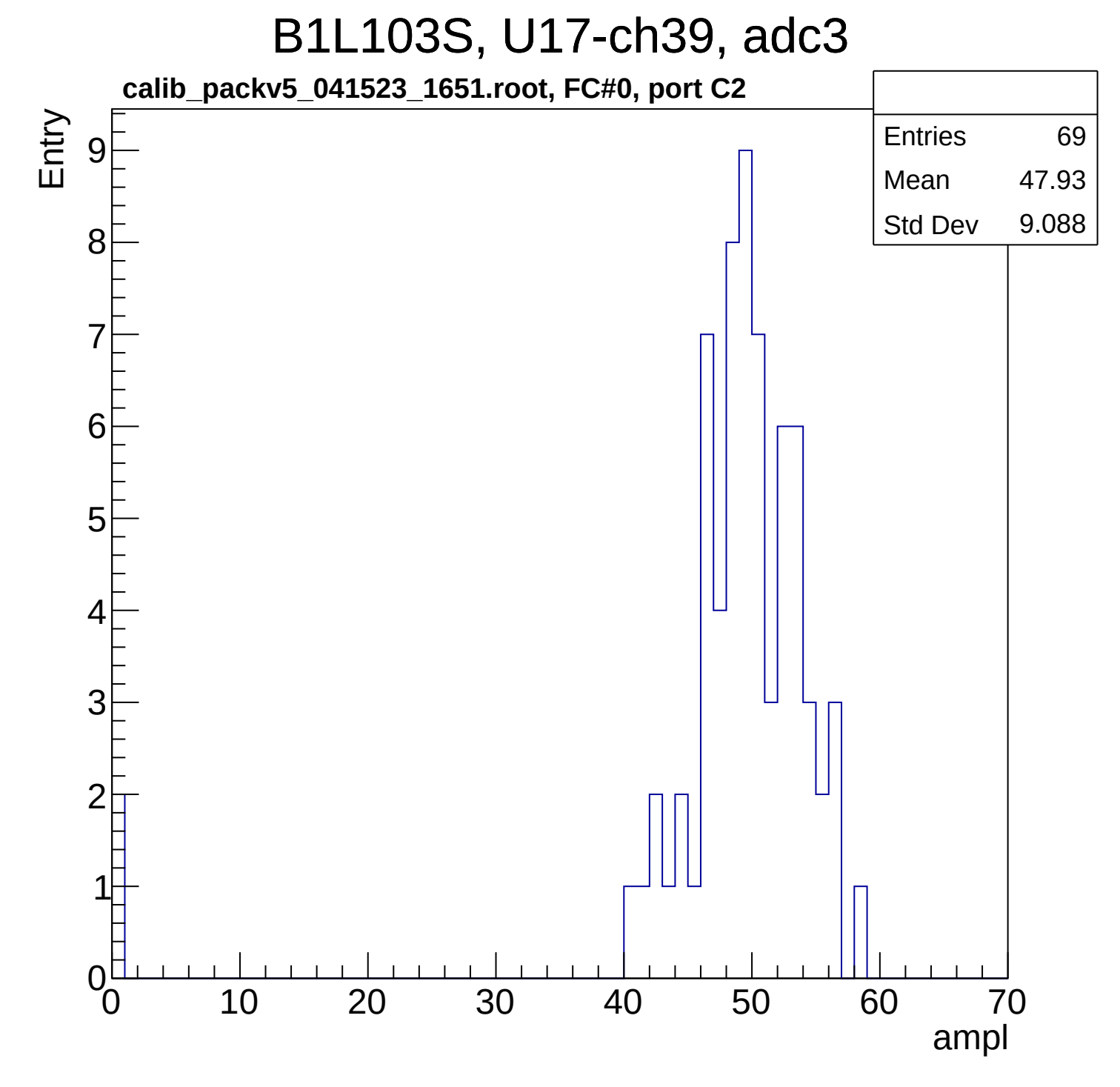

B1L103S, U17-ch38, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 58.38
Std Dev 13.15
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

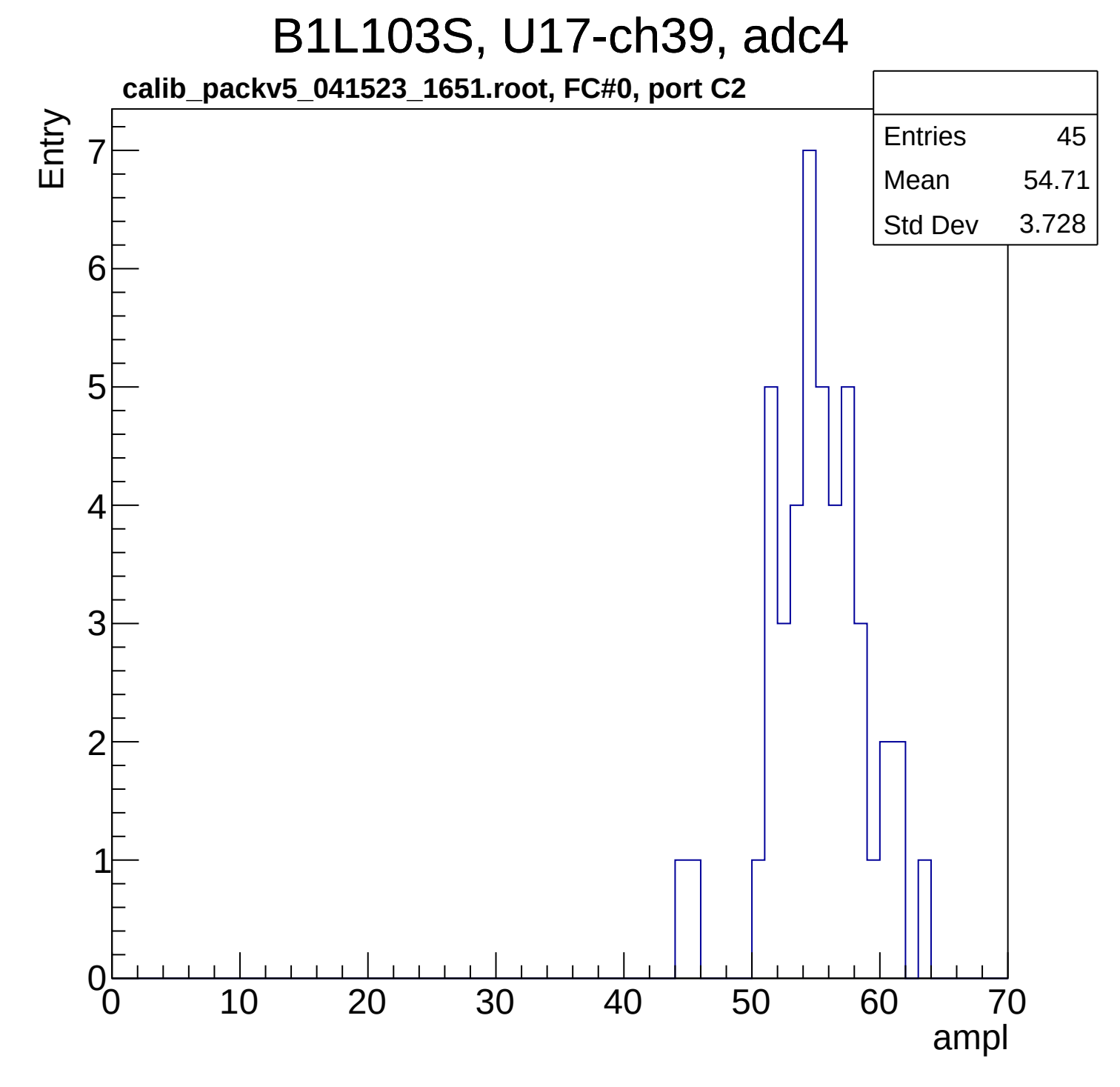

B1L103S, U17-ch38, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

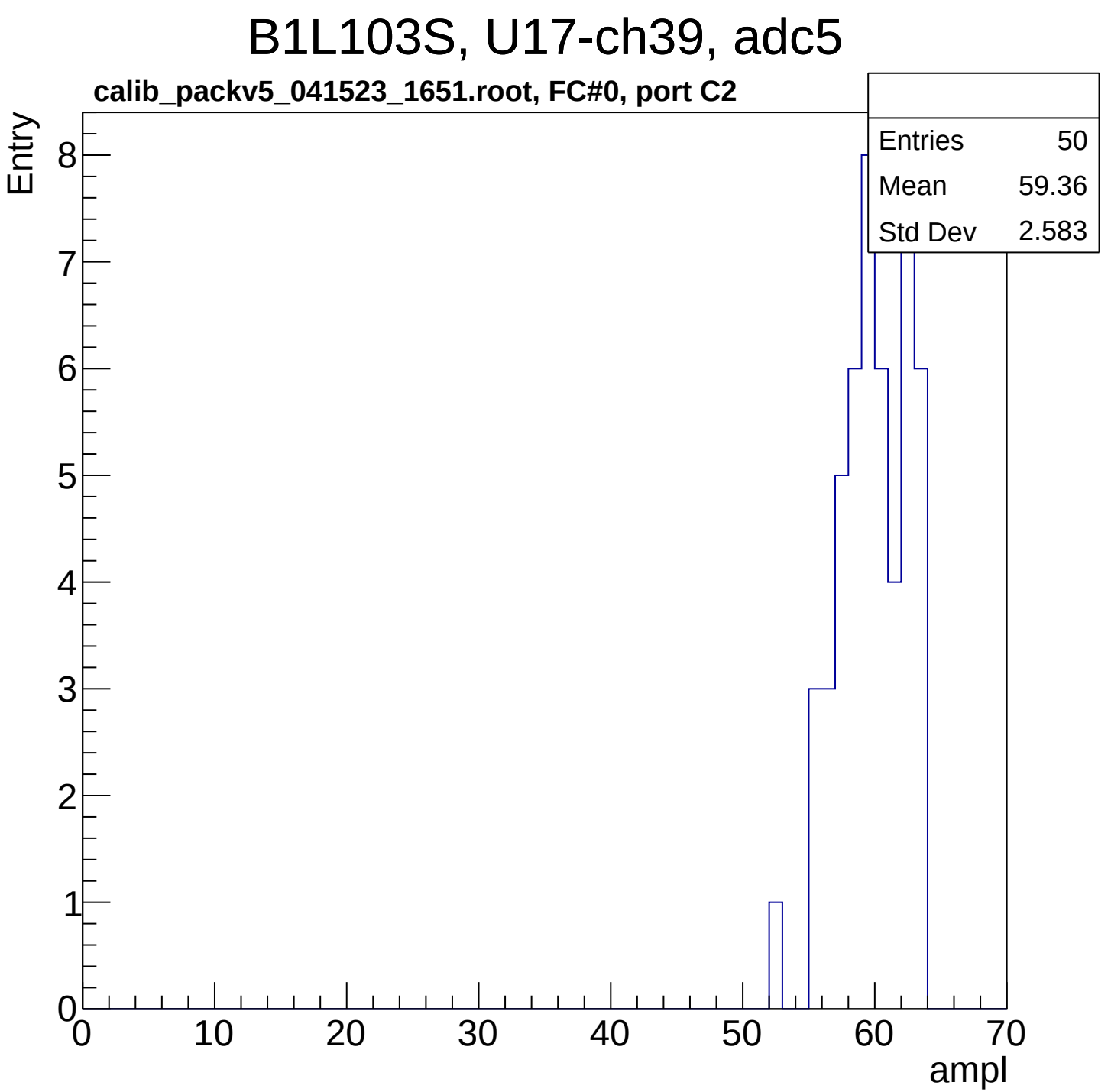

B1L103S, U17-ch39, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 22.54
Std Dev 12.44
Gaus mean : 29.8917
Gaus Width: 3.8360
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70

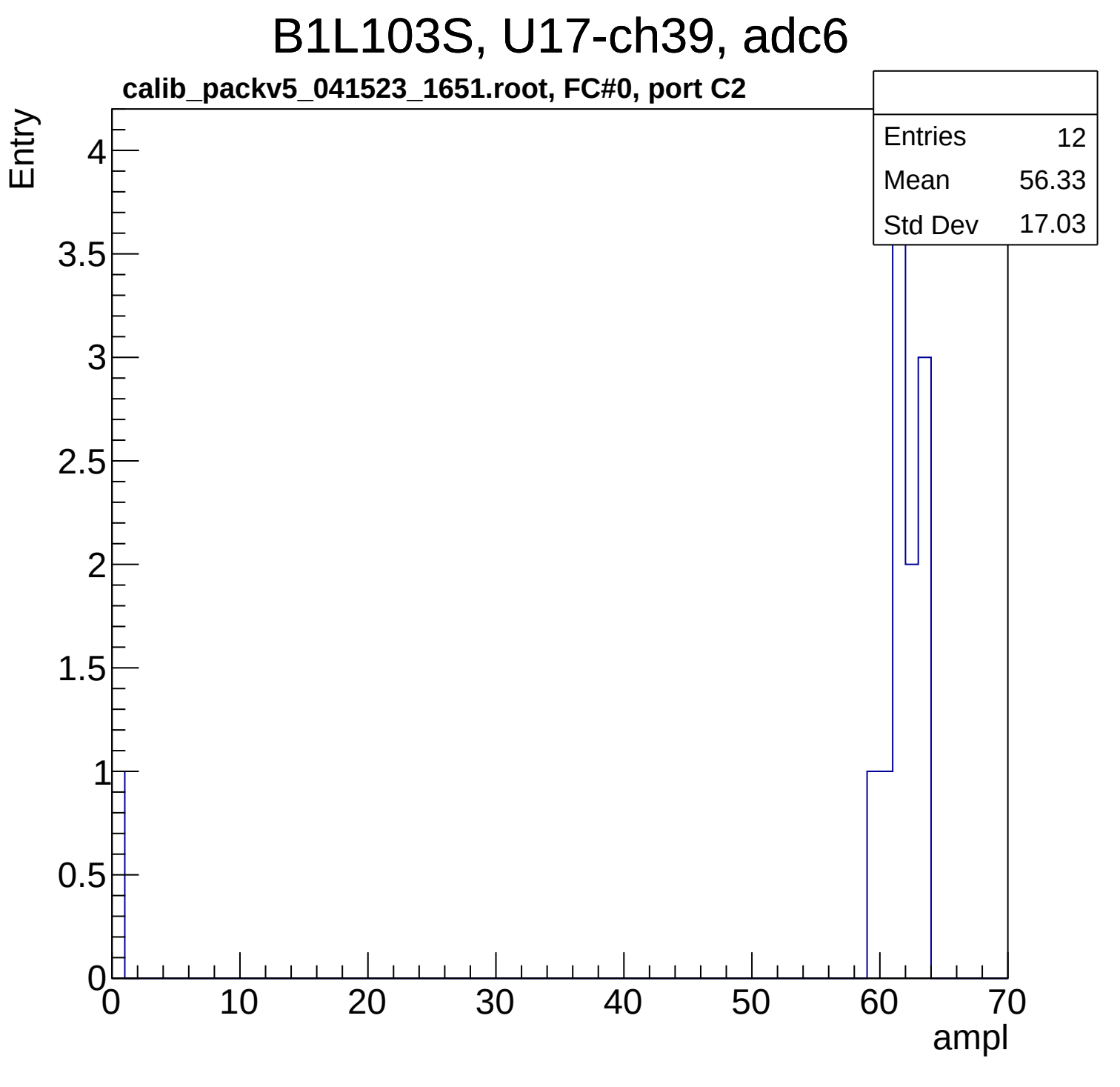

B1L103S, U17-ch39, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 35.9
Std Dev 5.599
Gaus mean : 36.8435
Gaus Width: 3.7362
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

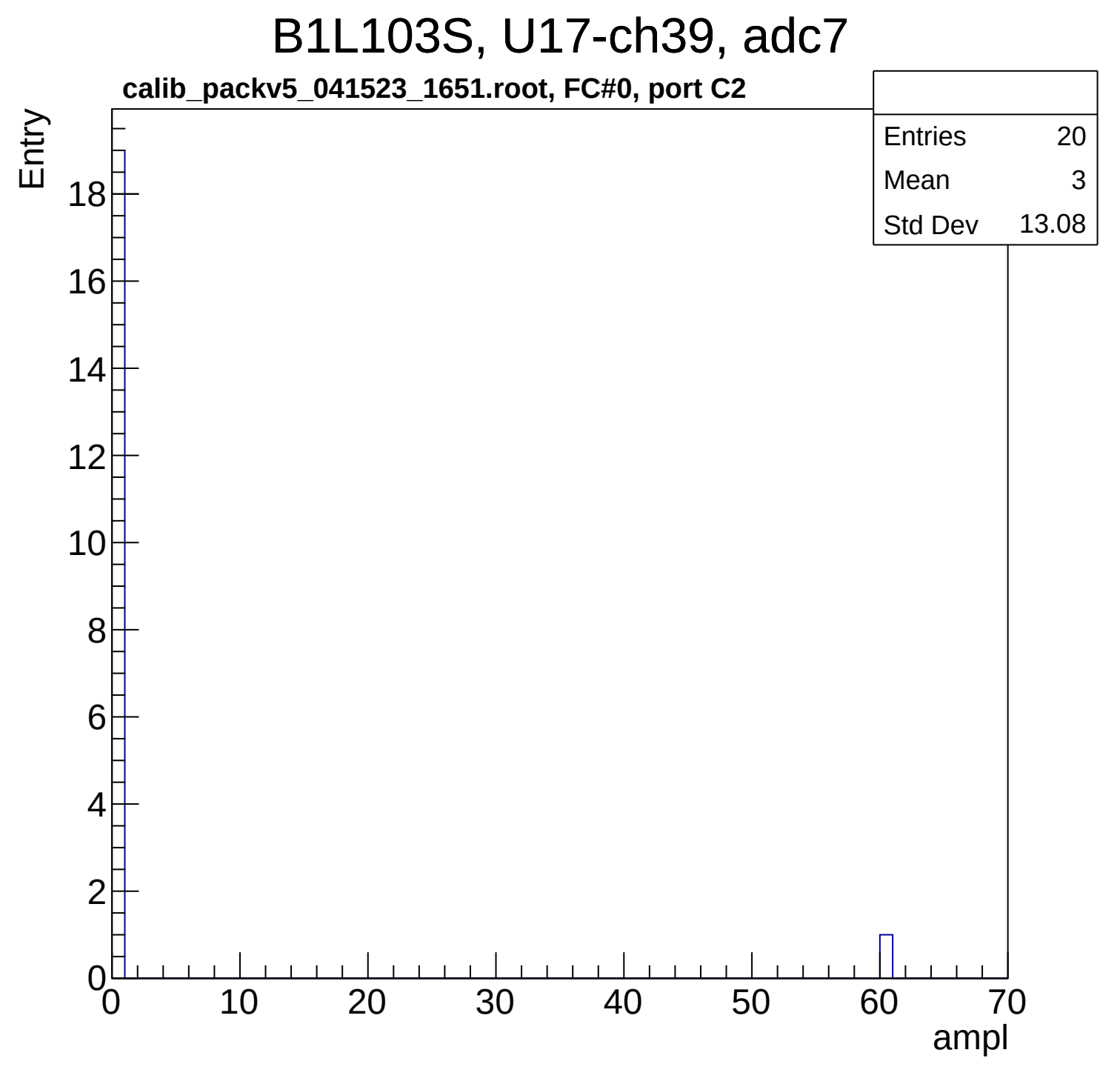

B1L103S, U17-ch39, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 33.95
Std Dev 17.95
Gaus mean : 43.7115
Gaus Width: 3.4407
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

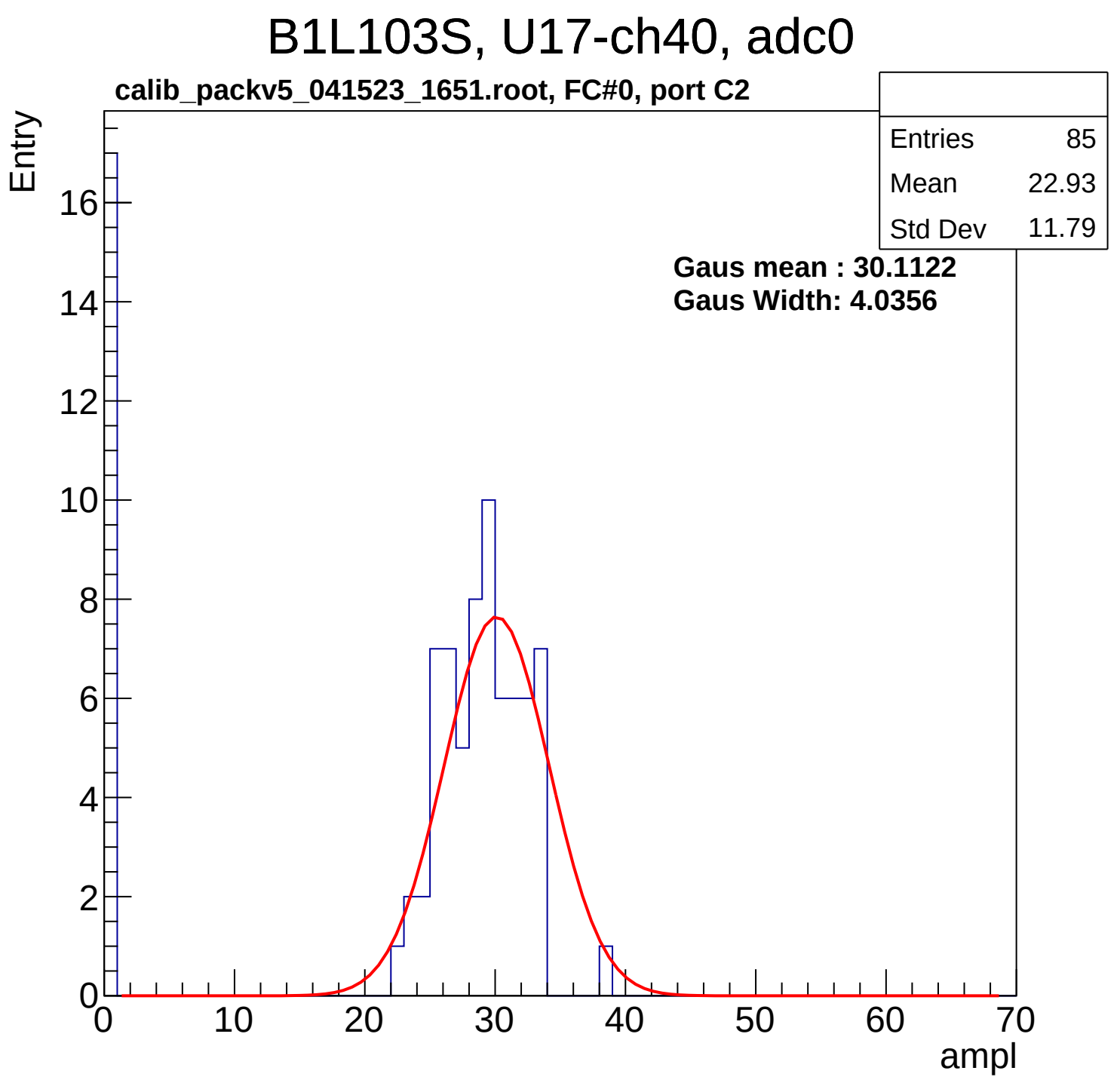

B1L103S, U17-ch39, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 47.93
Std Dev 9.088
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

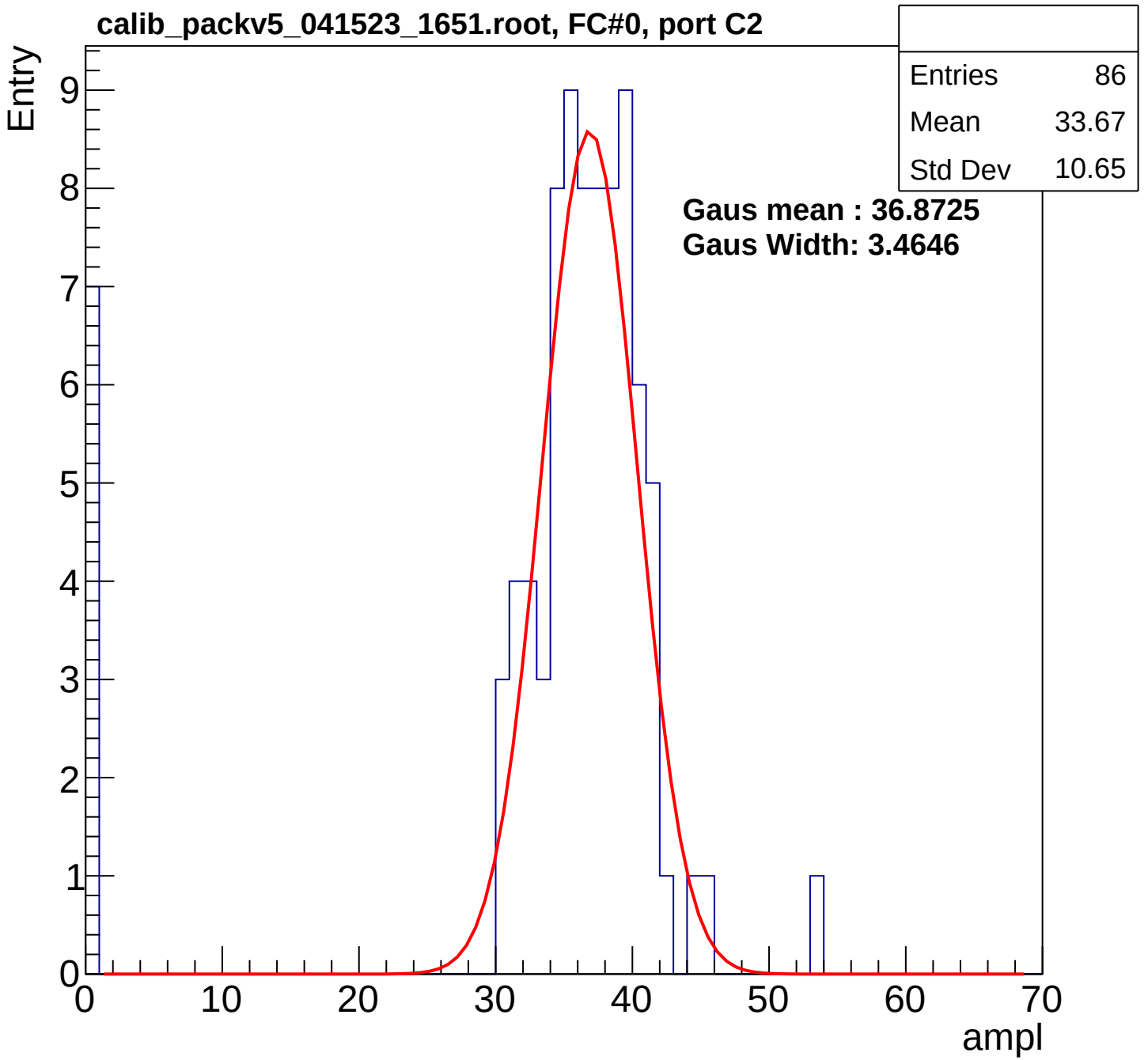

B1L103S, U17-ch39, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 54.71
Std Dev 3.728
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

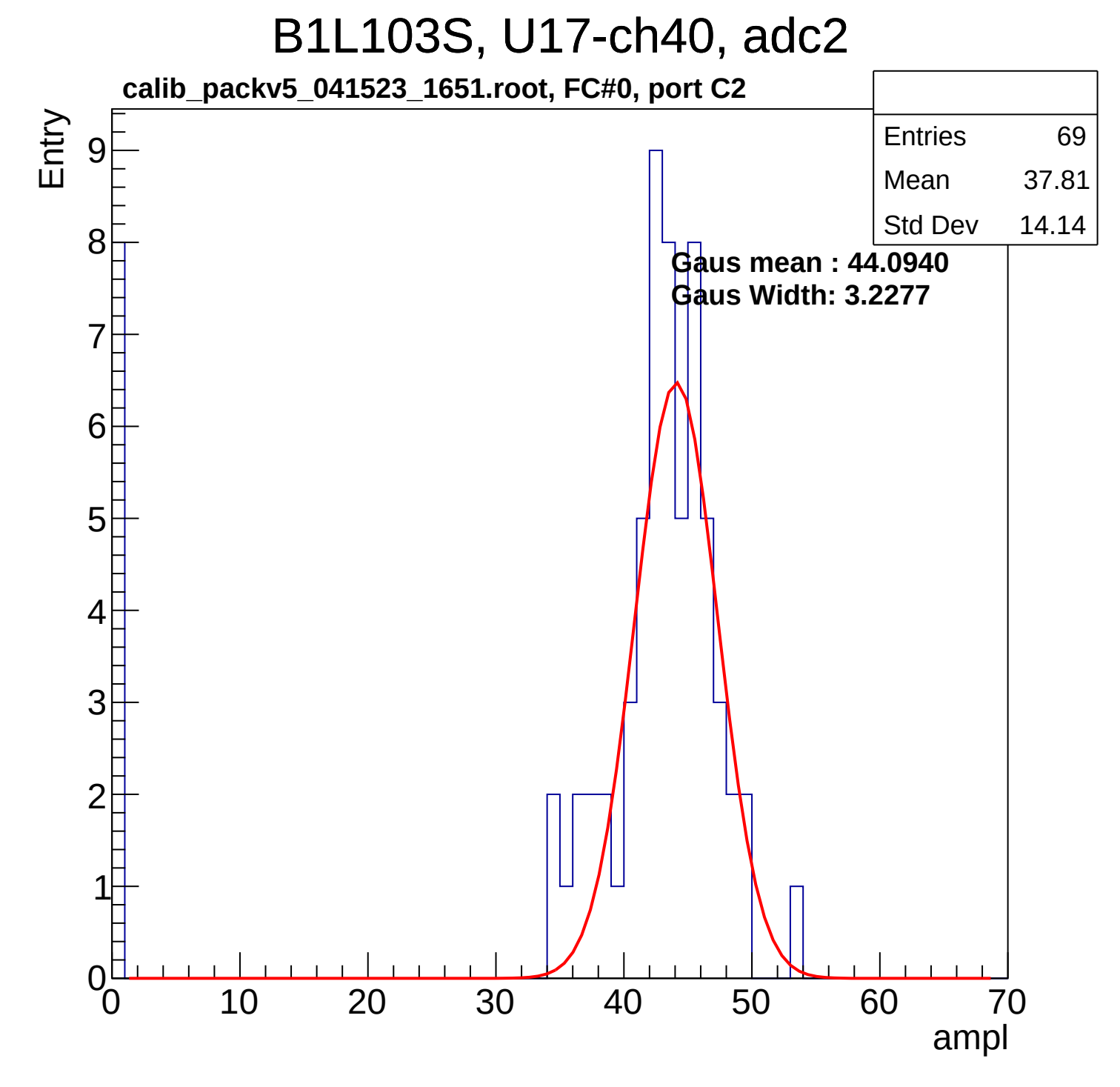

B1L103S, U17-ch39, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 59.36
Std Dev 2.583
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

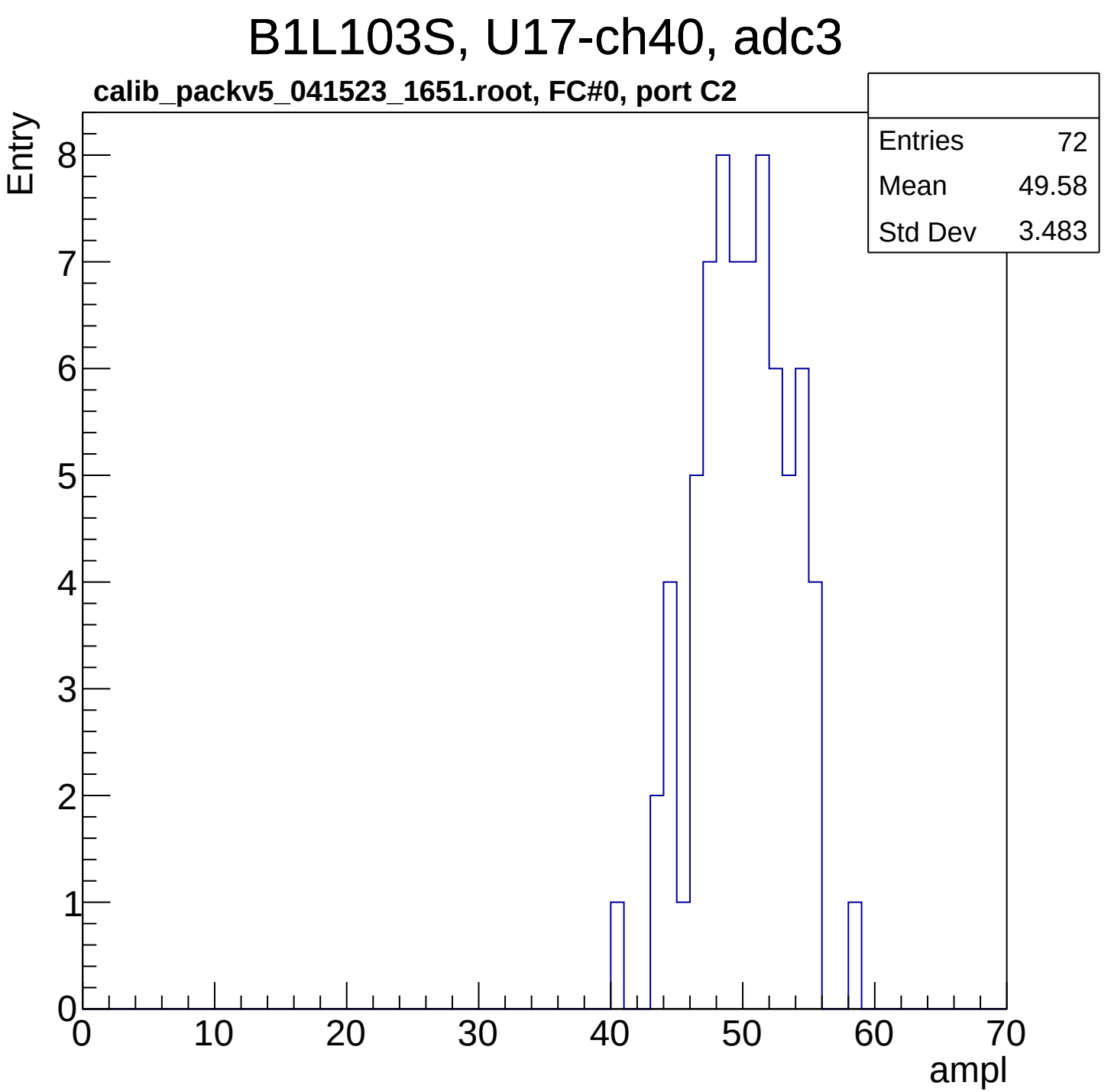

B1L103S, U17-ch39, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.33
Std Dev 17.03
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

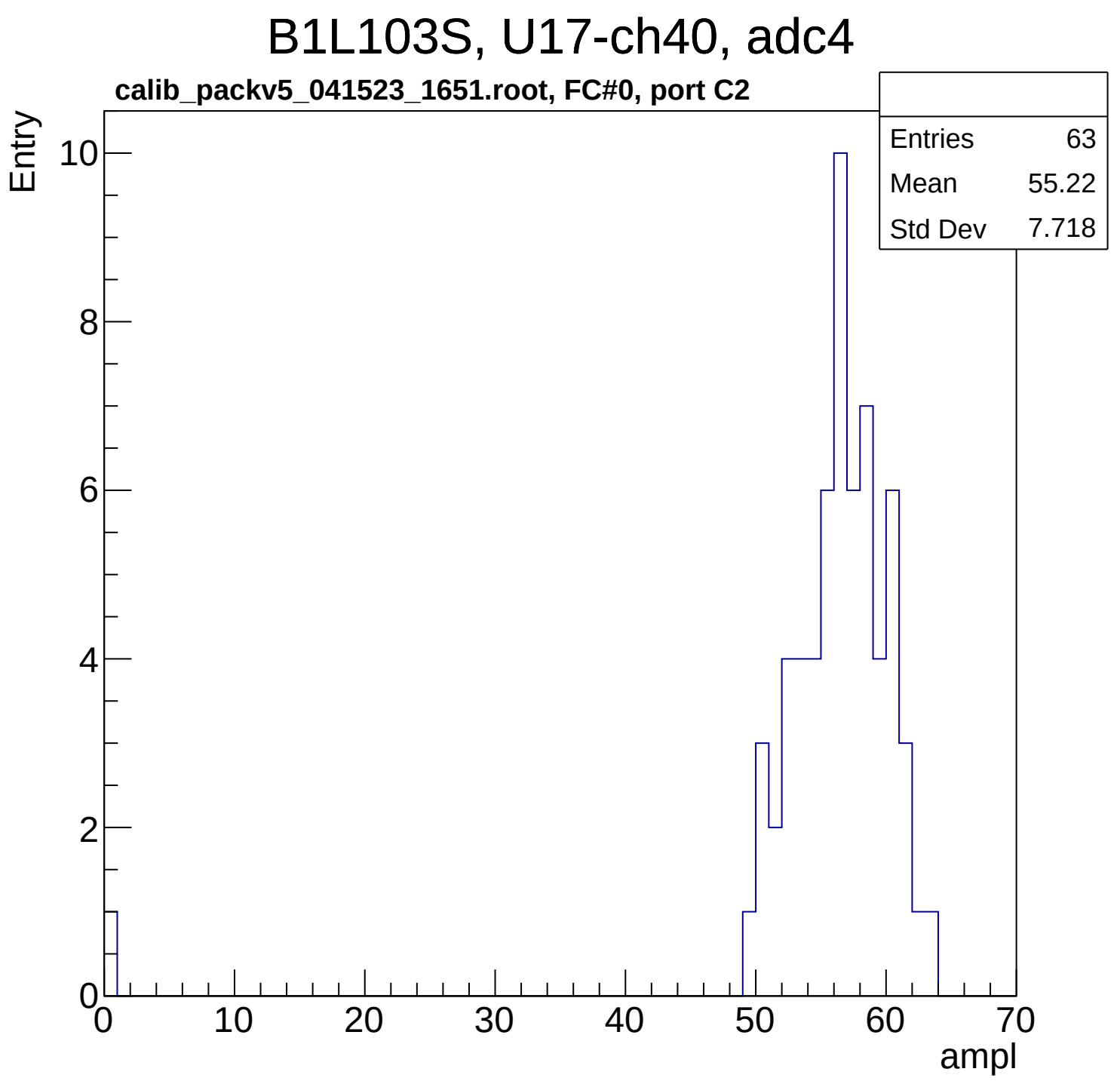

B1L103S, U17-ch39, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3
Std Dev 13.08
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

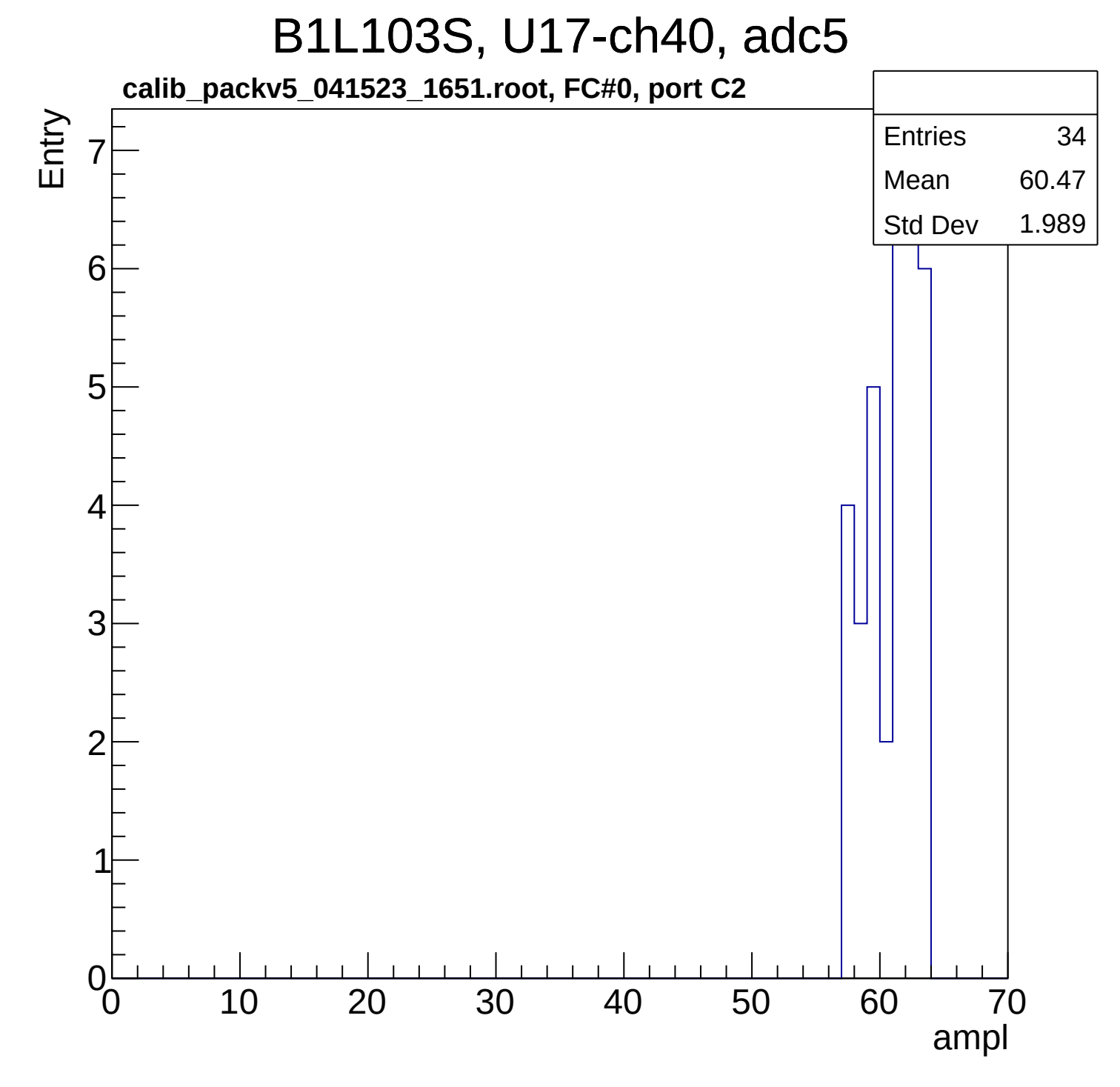

B1L103S, U17-ch40, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 22.93
Std Dev 11.79
Gaus mean : 30.1122
Gaus Width: 4.0356
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

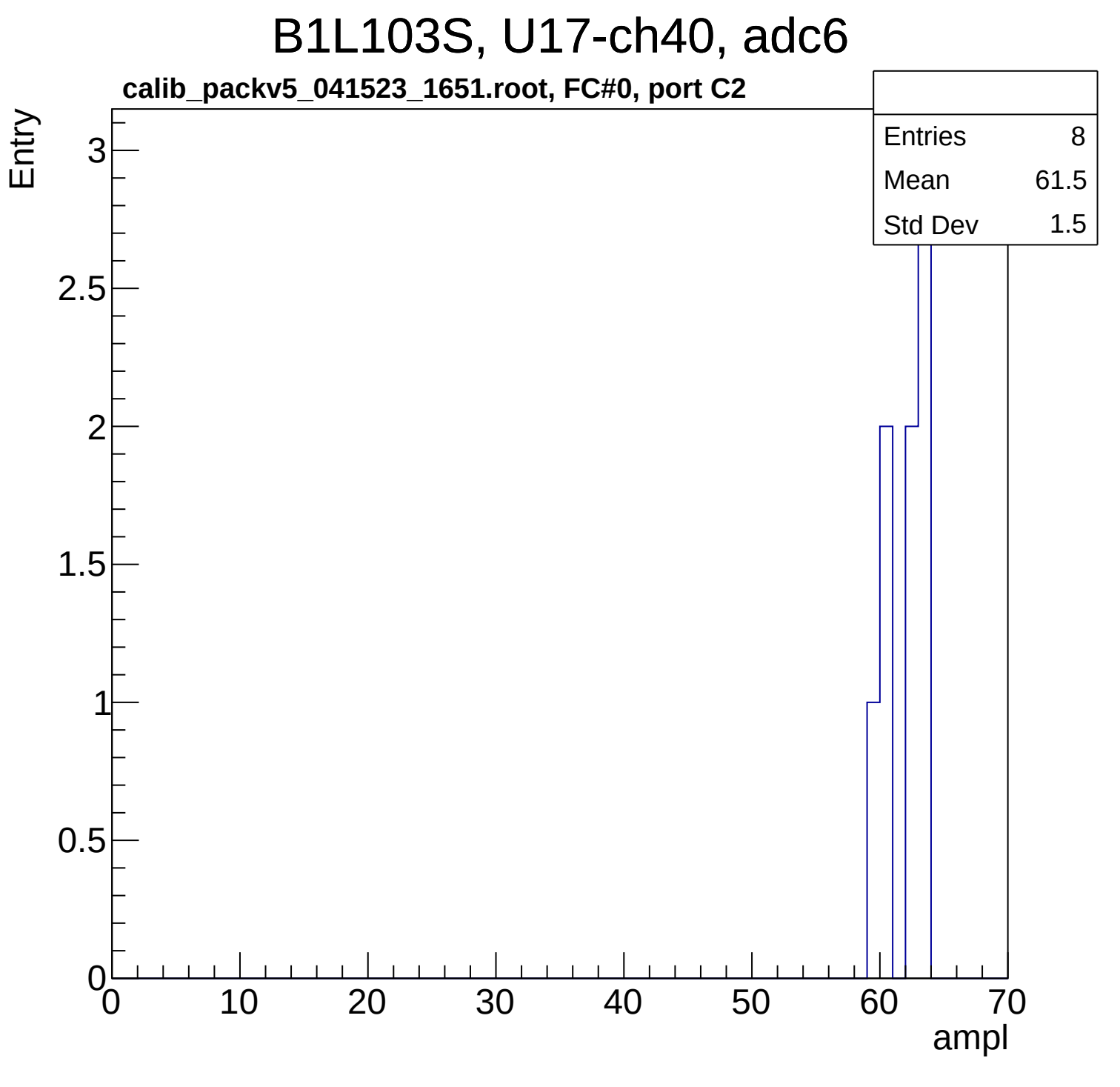

B1L103S, U17-ch40, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 33.67
Std Dev 10.65
Gaus mean : 36.8725
Gaus Width: 3.4646
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

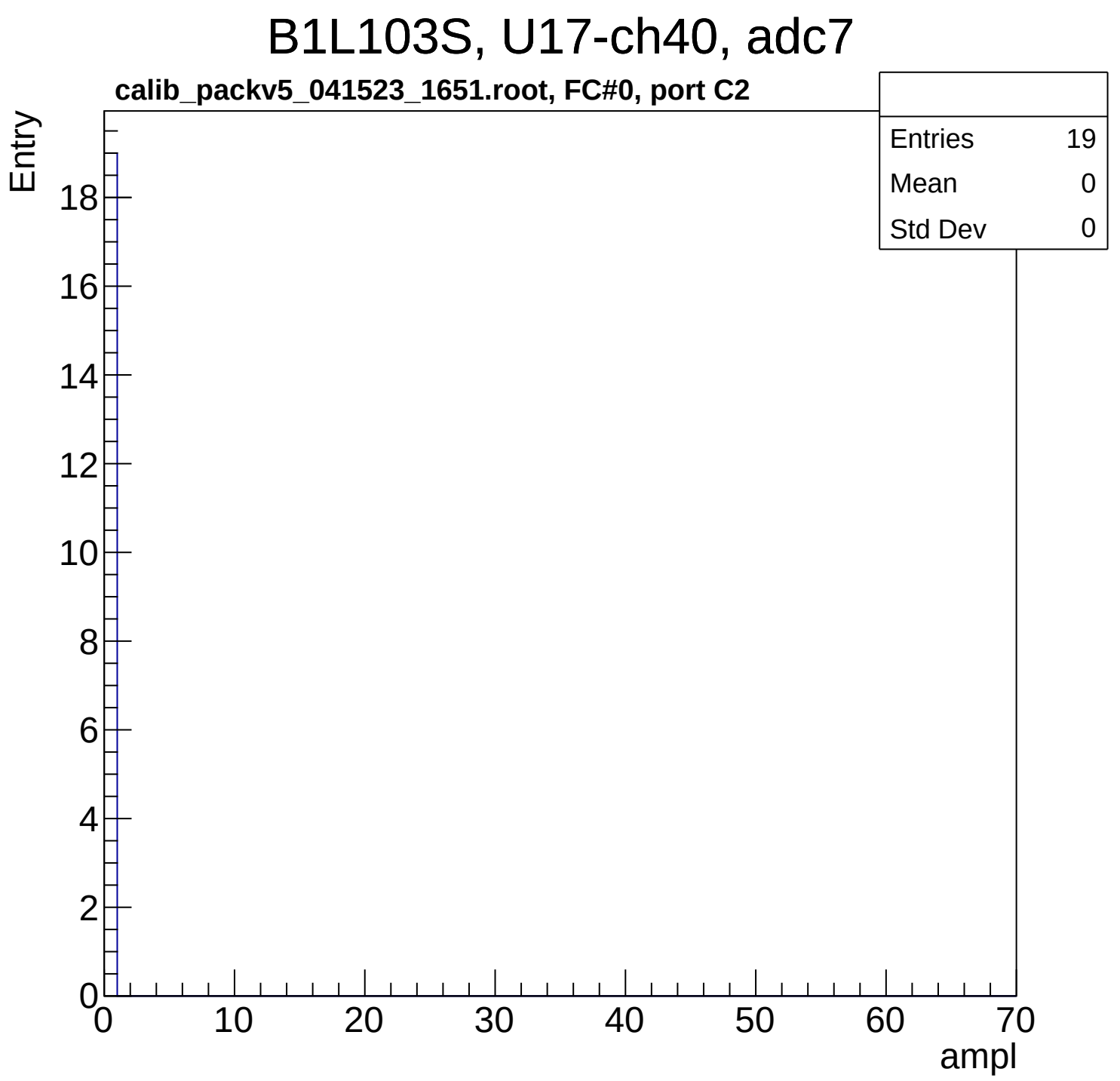

B1L103S, U17-ch40, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 37.81
Std Dev 14.14
Gaus mean : 44.0940
Gaus Width: 3.2277
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

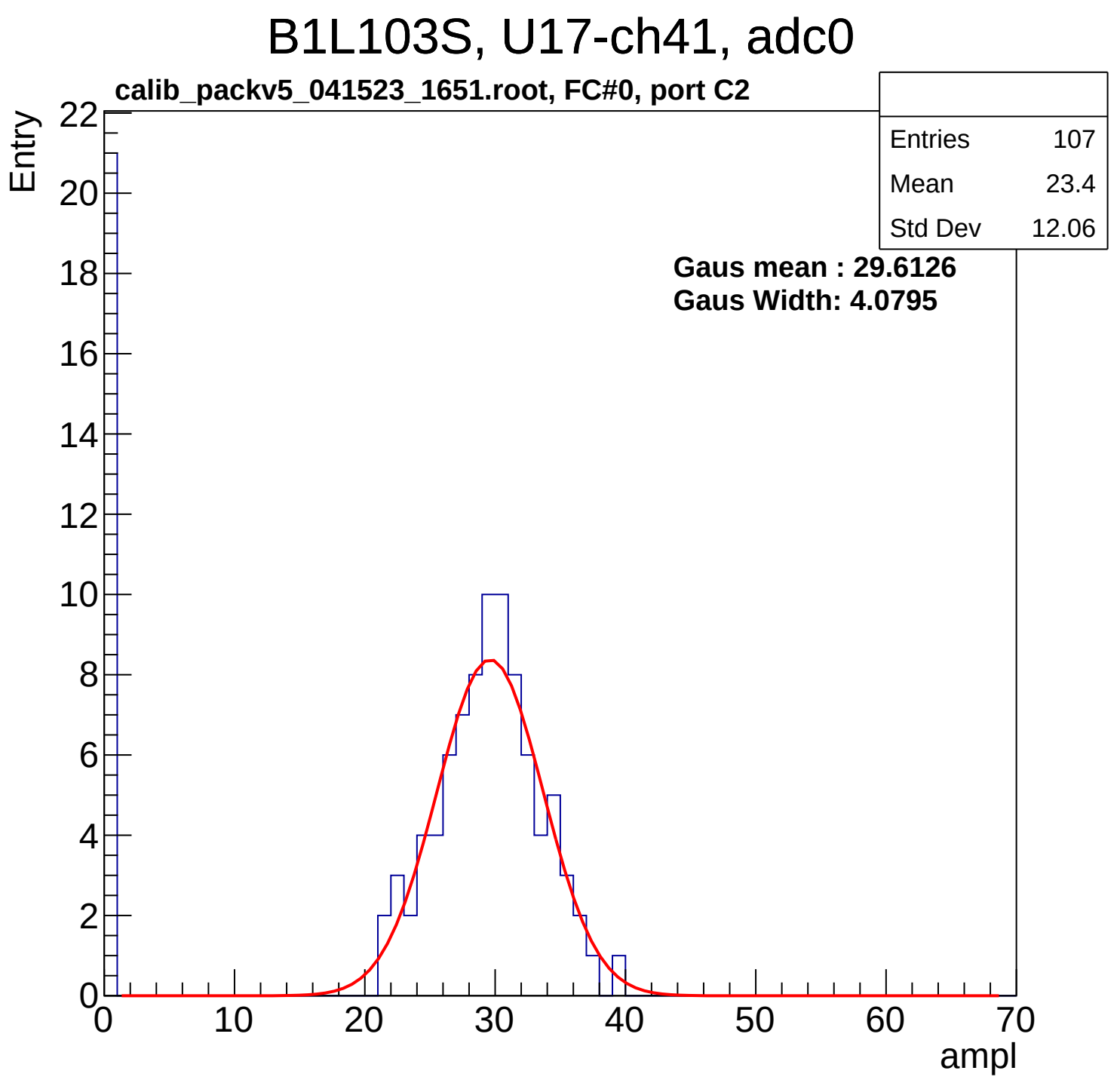

B1L103S, U17-ch40, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 49.58
Std Dev 3.483
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

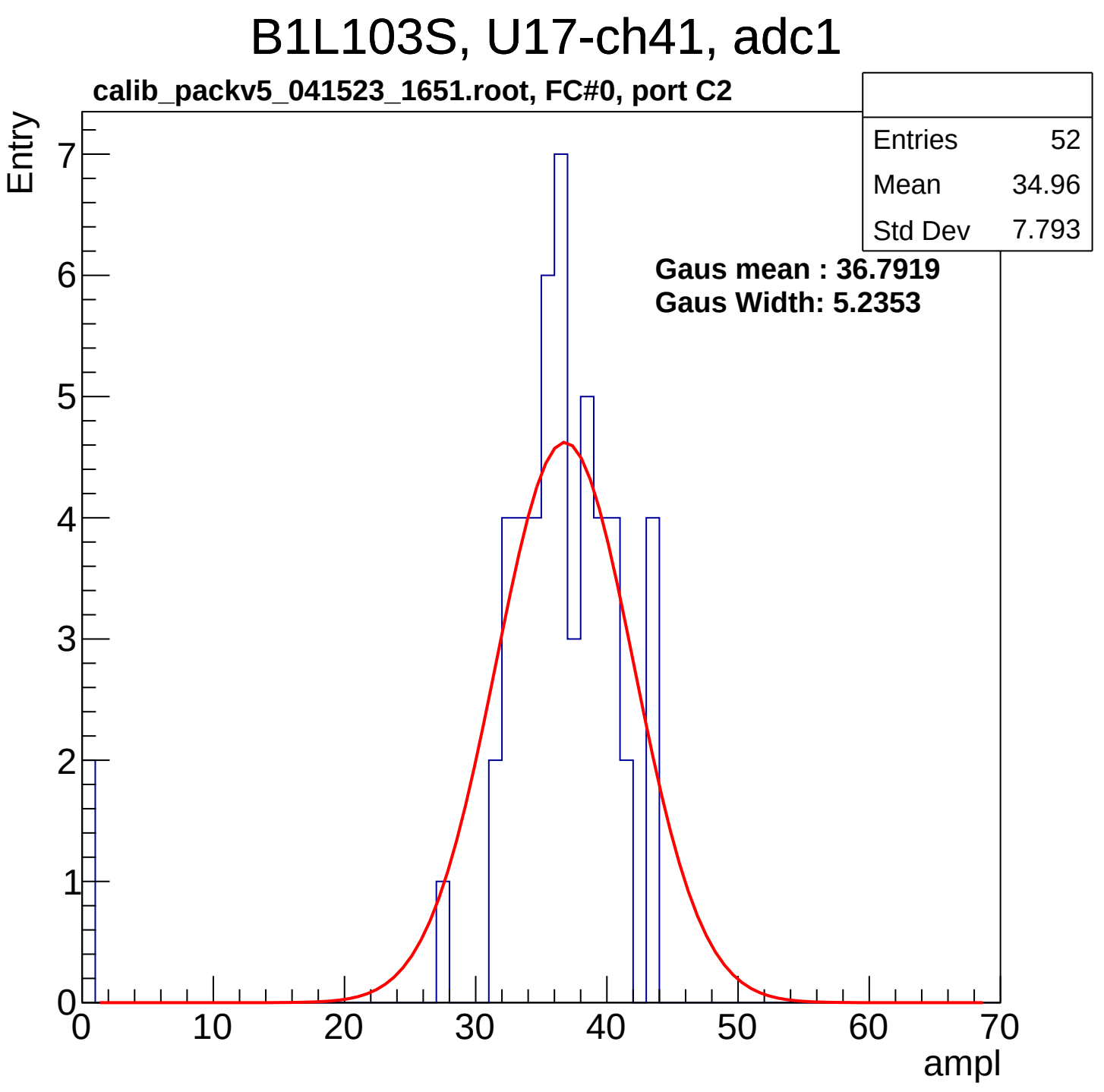

B1L103S, U17-ch40, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 55.22
Std Dev 7.718
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

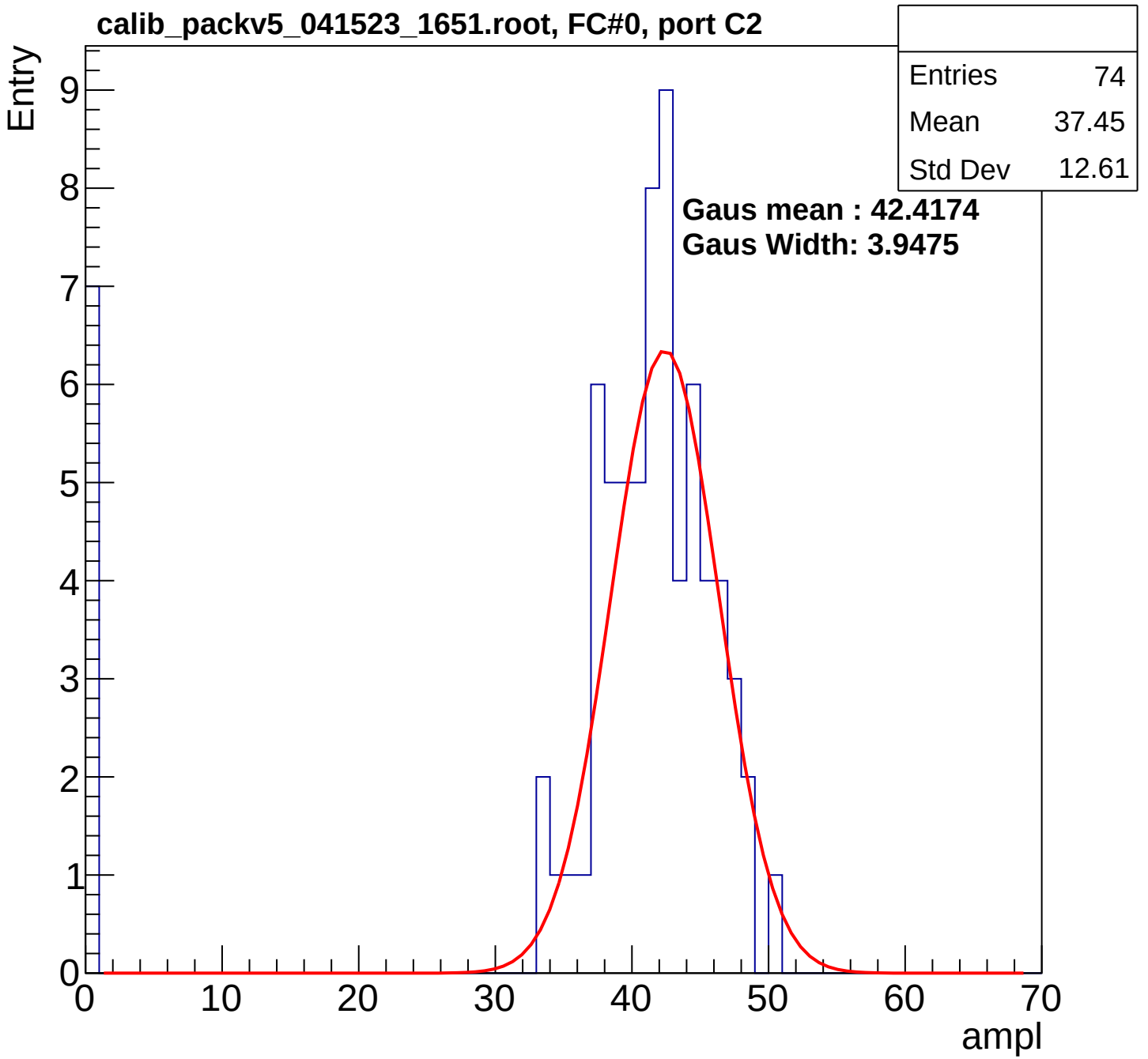

B1L103S, U17-ch40, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 60.47
Std Dev 1.989
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

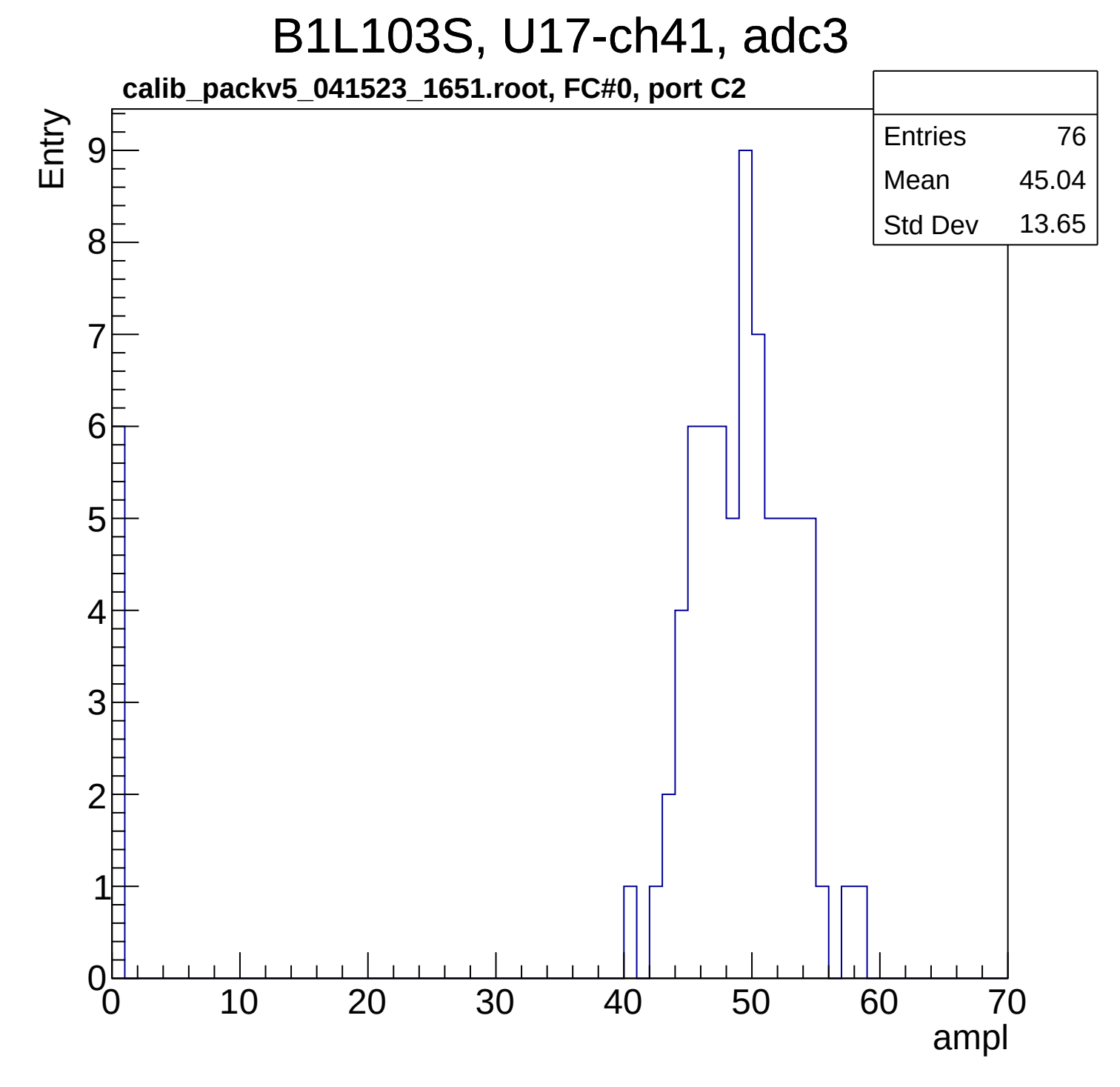

B1L103S, U17-ch40, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.5
Std Dev 1.5
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

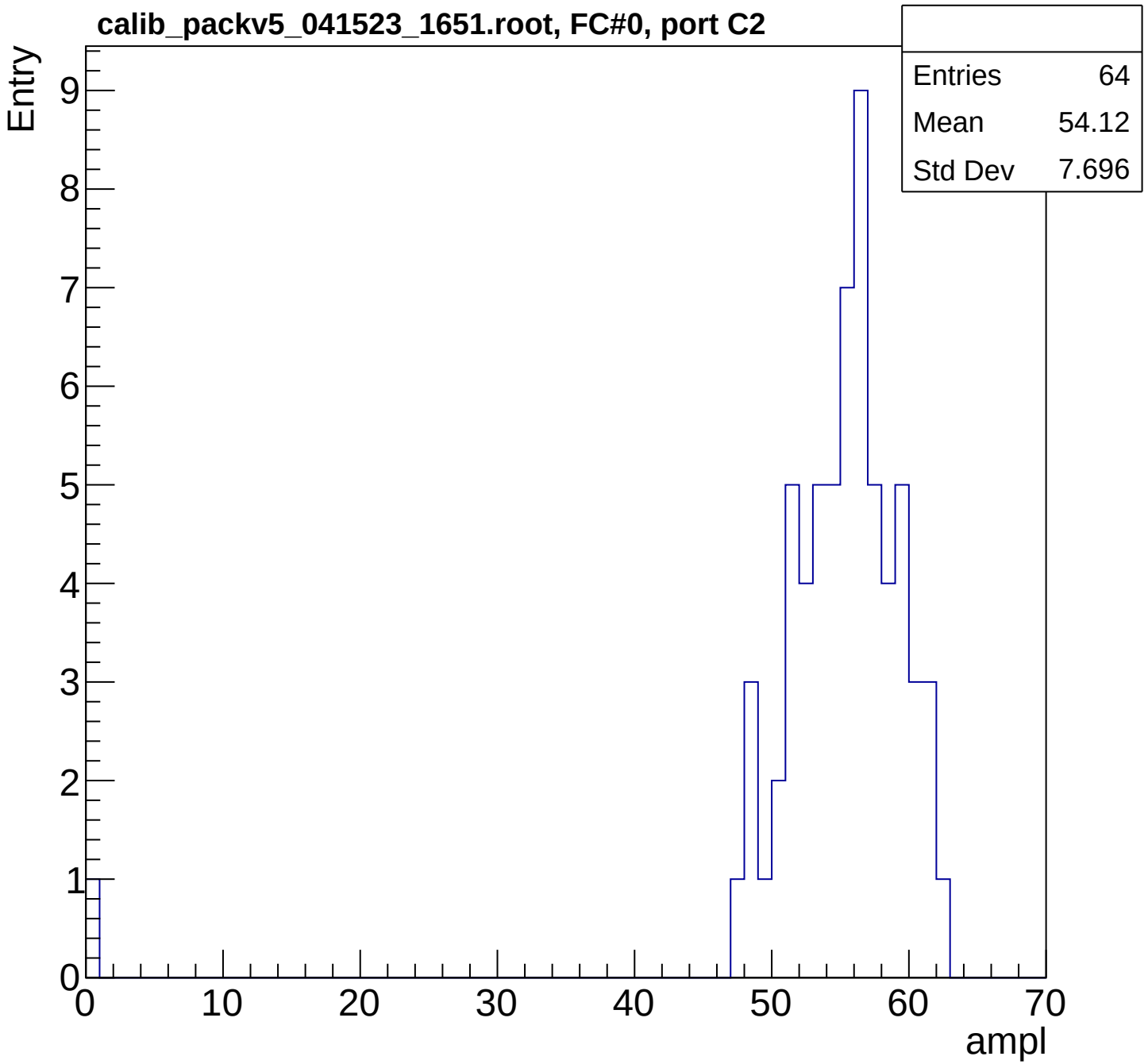

B1L103S, U17-ch40, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

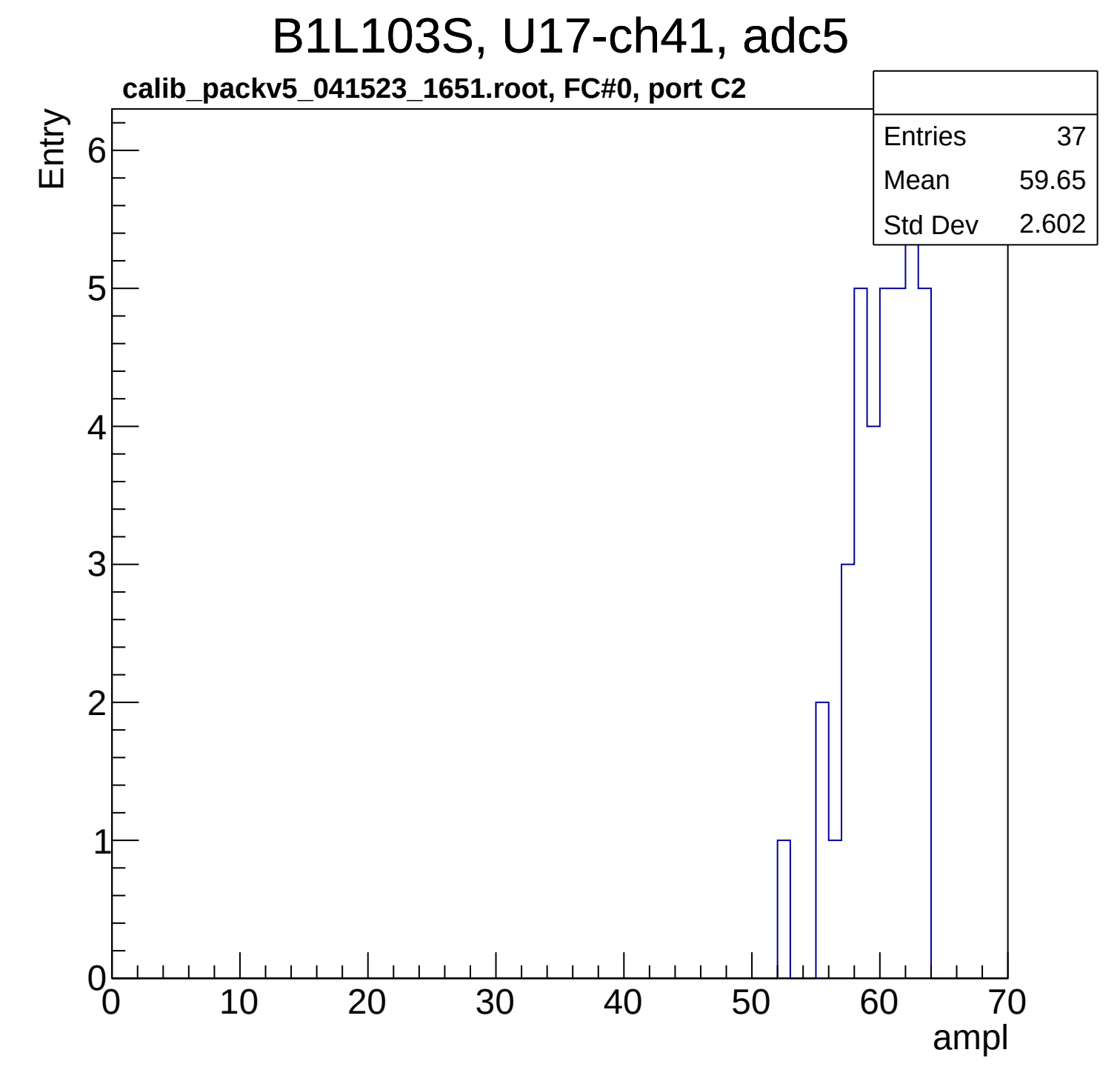

B1L103S, U17-ch41, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 107
Mean 23.4
Std Dev 12.06
Gaus mean : 29.6126
Gaus Width: 4.0795
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70

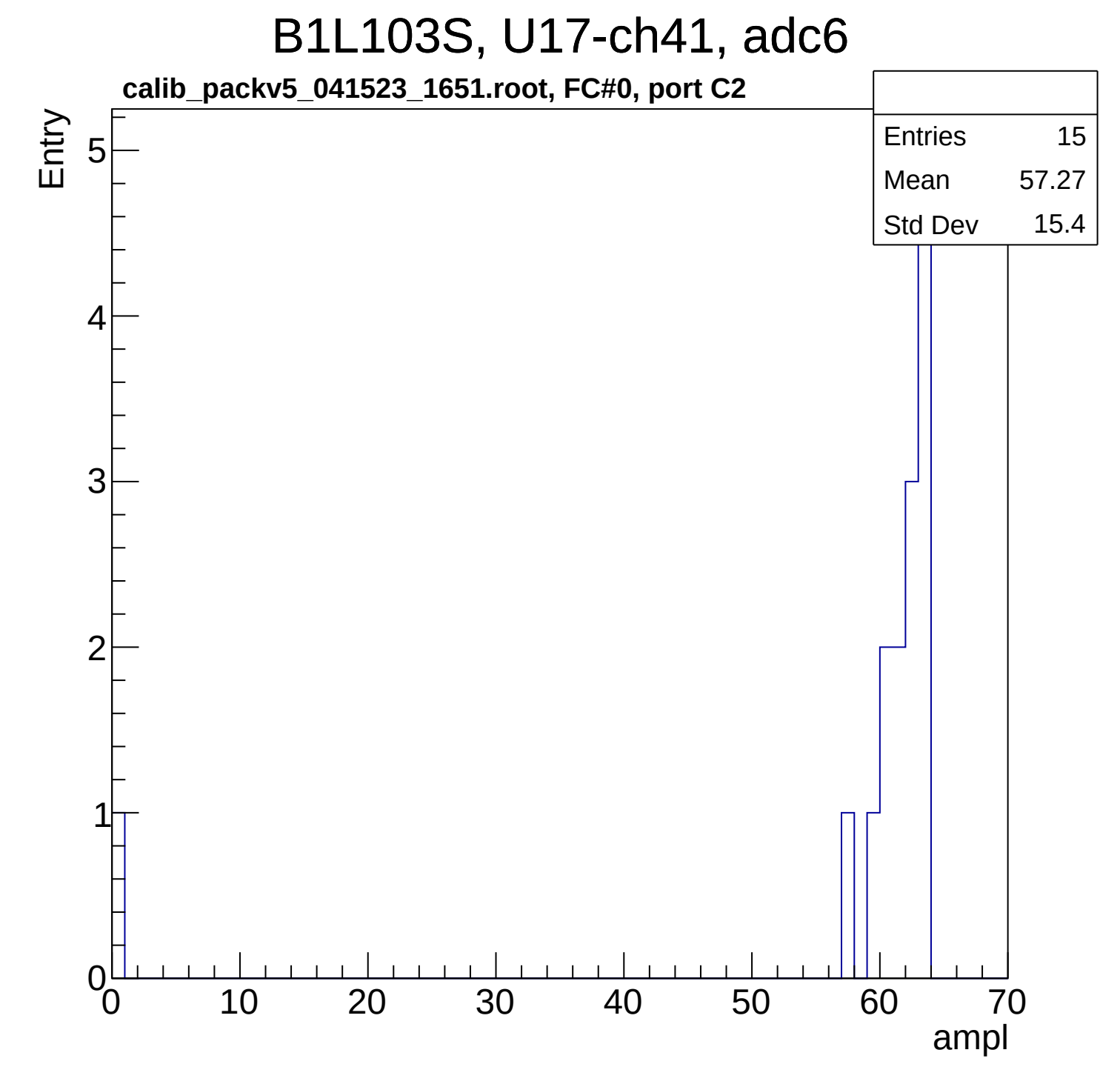

B1L103S, U17-ch41, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 34.96
Std Dev 7.793
Gaus mean : 36.7919
Gaus Width: 5.2353
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

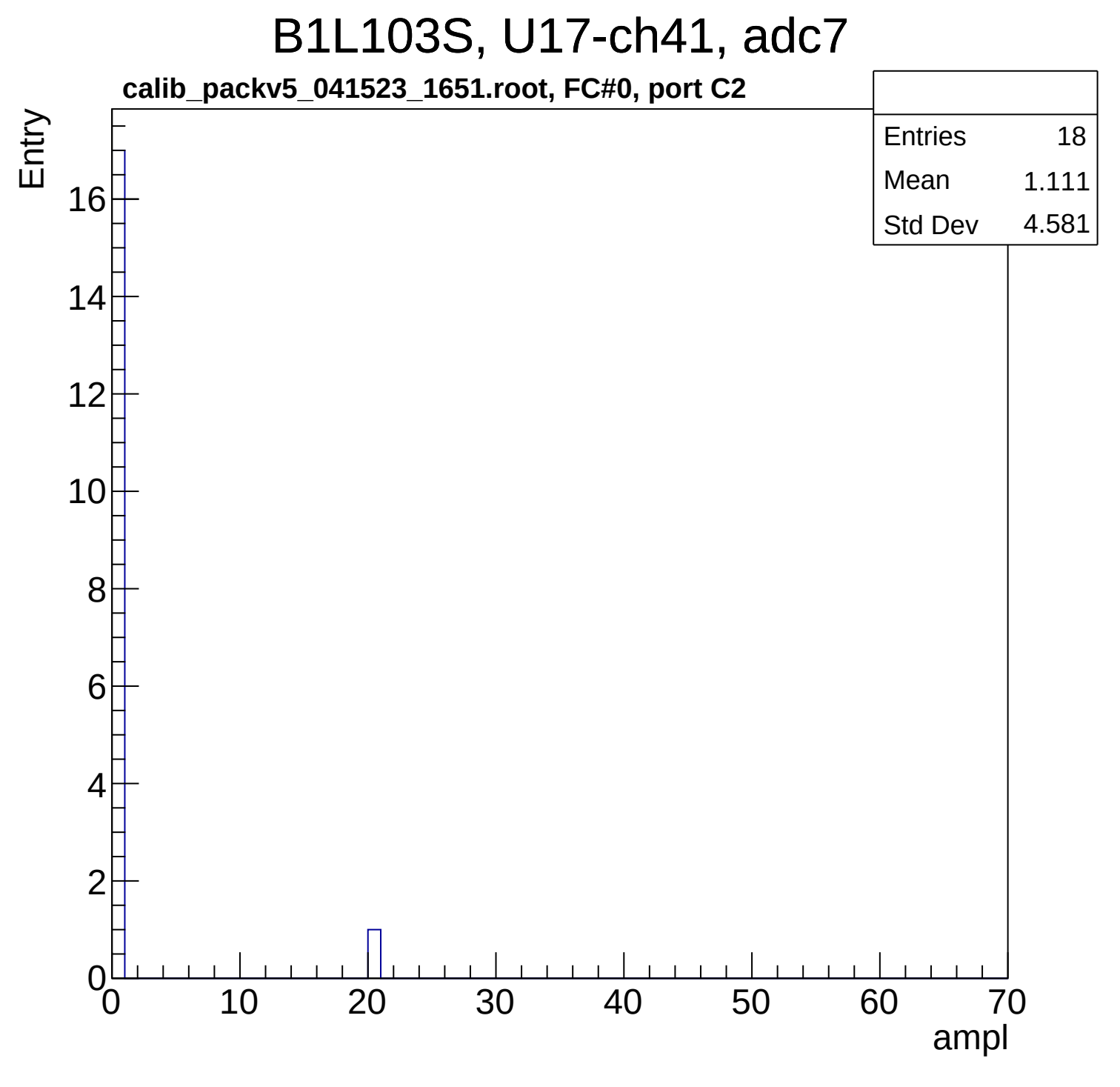

B1L103S, U17-ch41, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 37.45
Std Dev 12.61
Gaus mean : 42.4174
Gaus Width: 3.9475
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

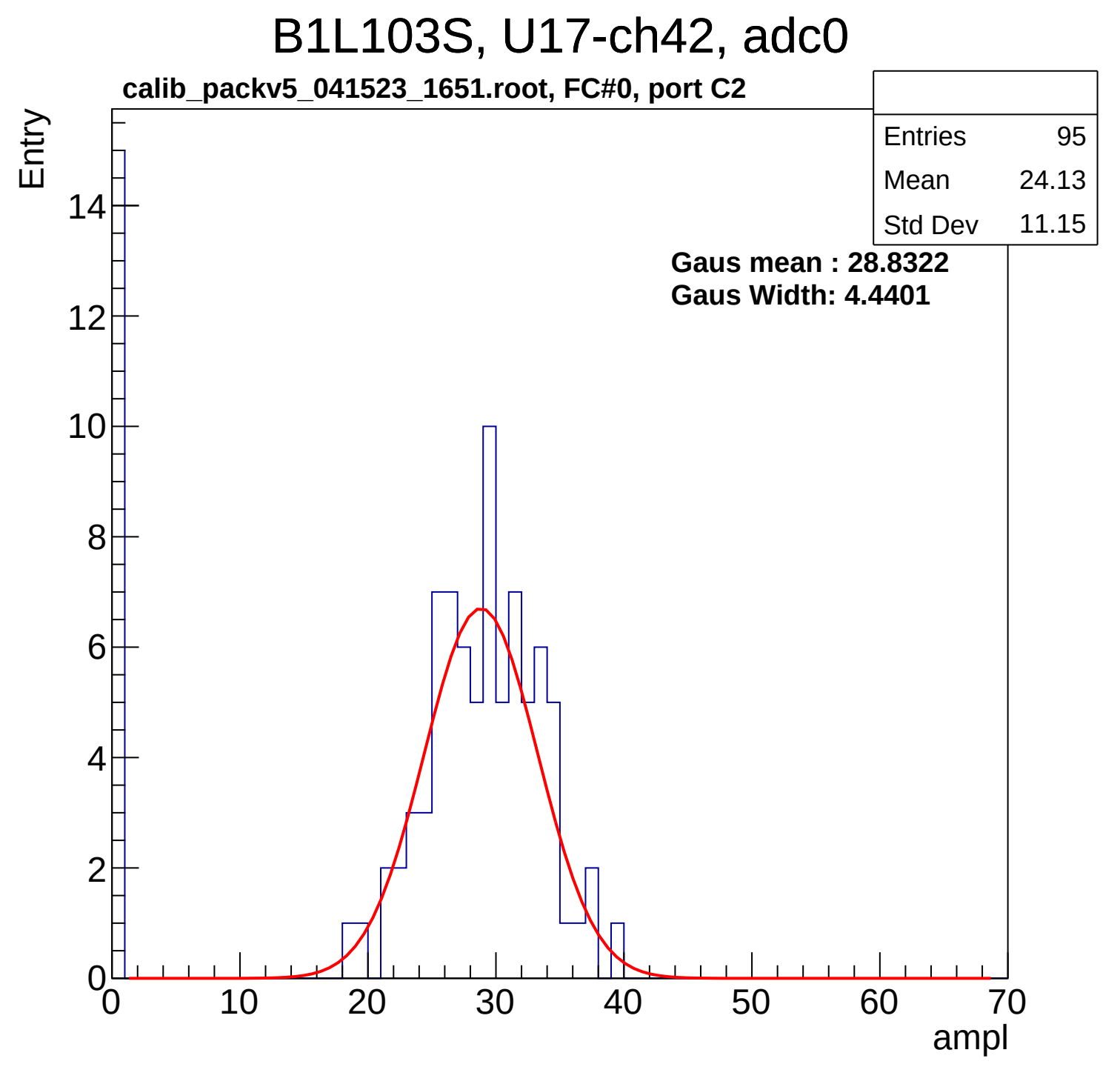

B1L103S, U17-ch41, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 45.04
Std Dev 13.65
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

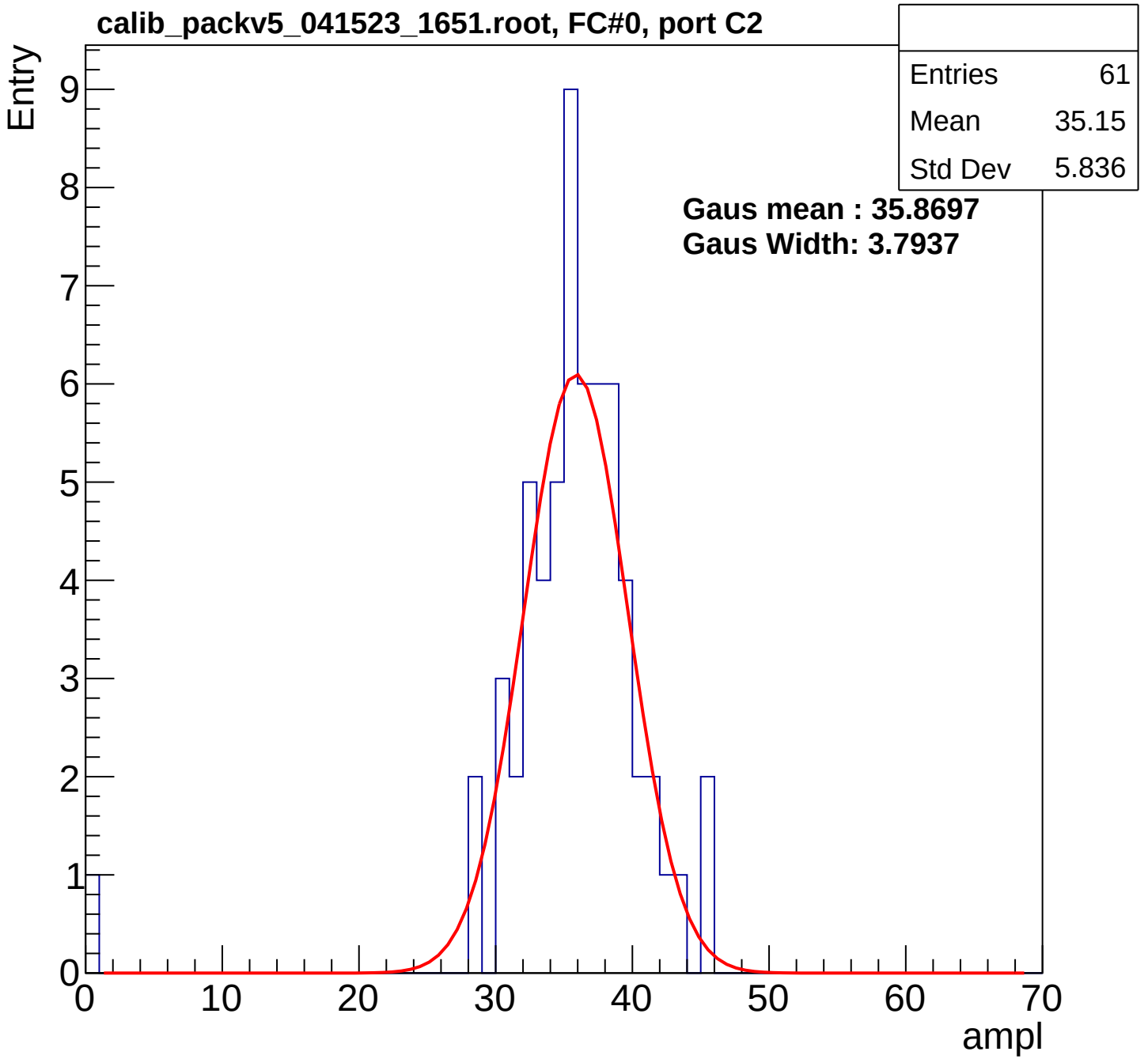

B1L103S, U17-ch41, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 54.12
Std Dev 7.696
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

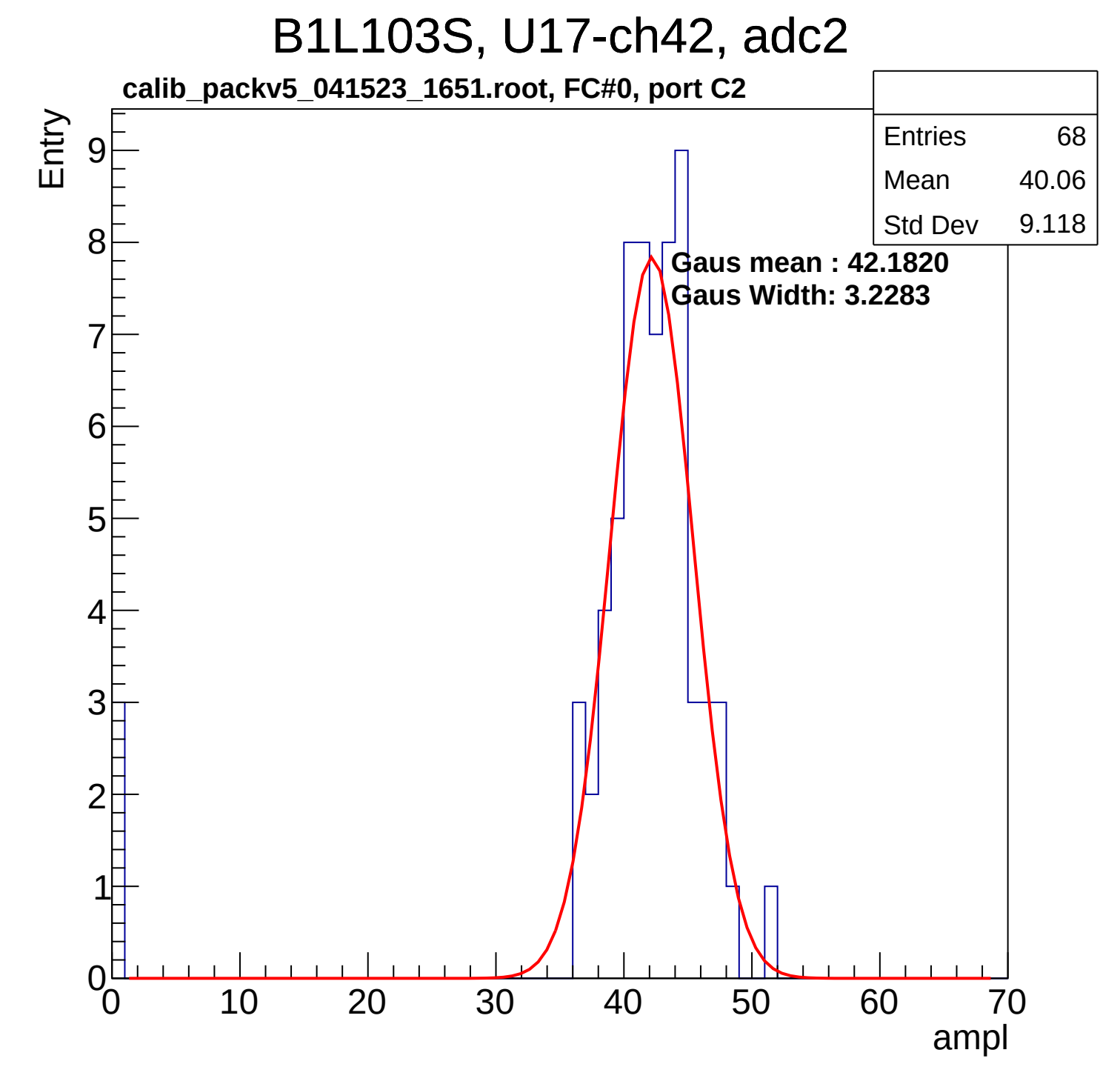

B1L103S, U17-ch41, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 59.65
Std Dev 2.602
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

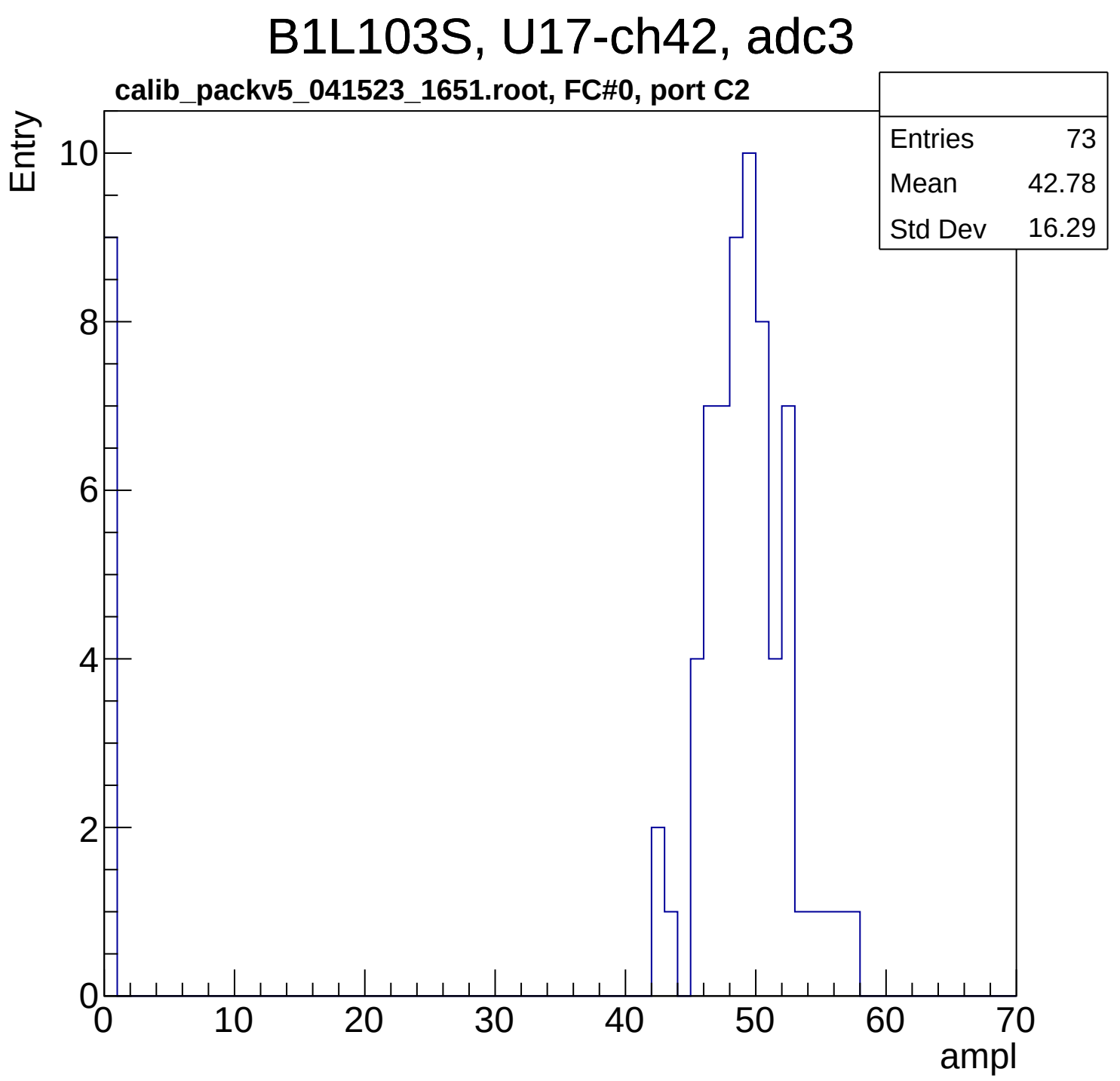

B1L103S, U17-ch41, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.27
Std Dev 15.4
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

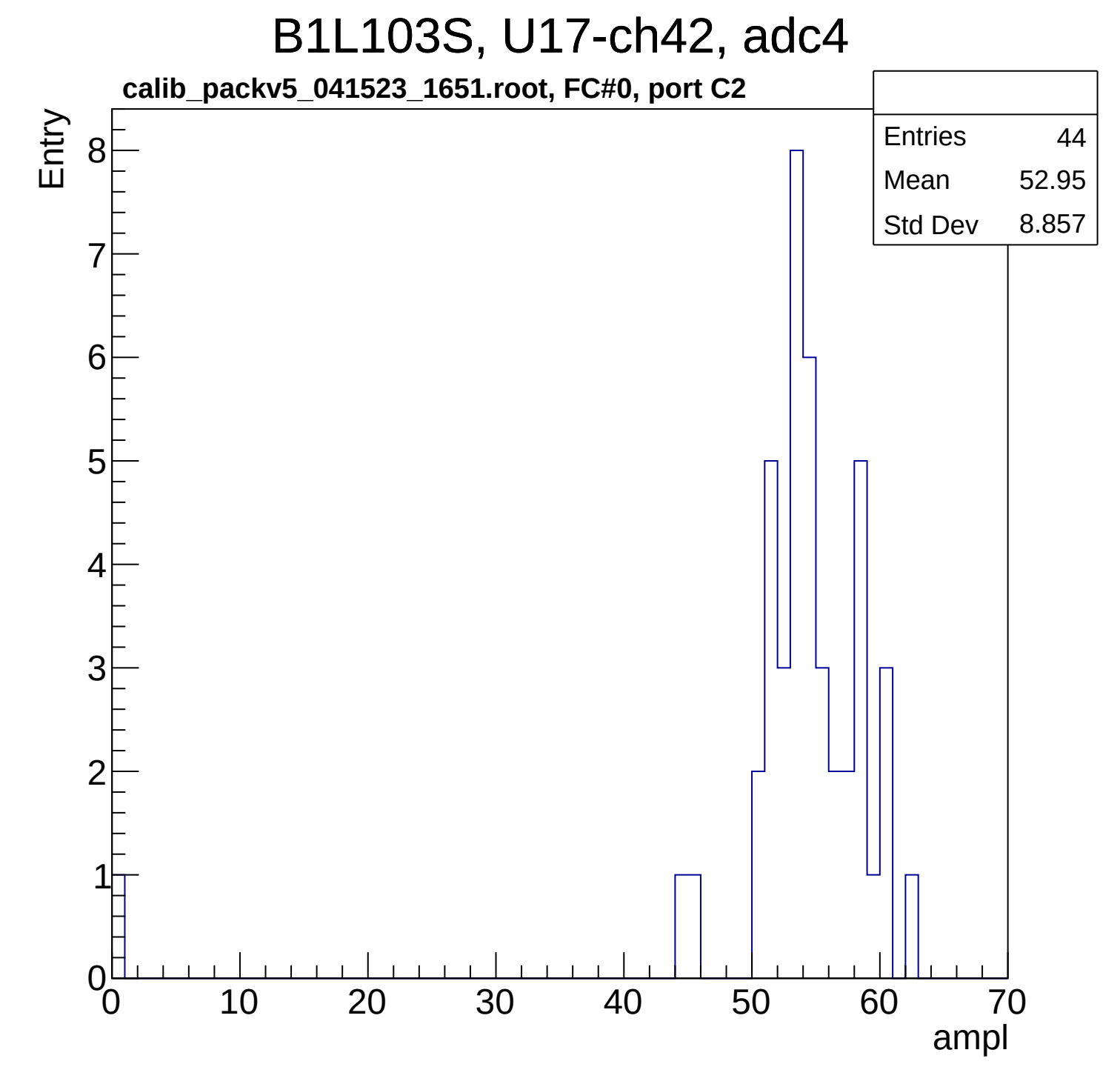

B1L103S, U17-ch41, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.111
Std Dev 4.581
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

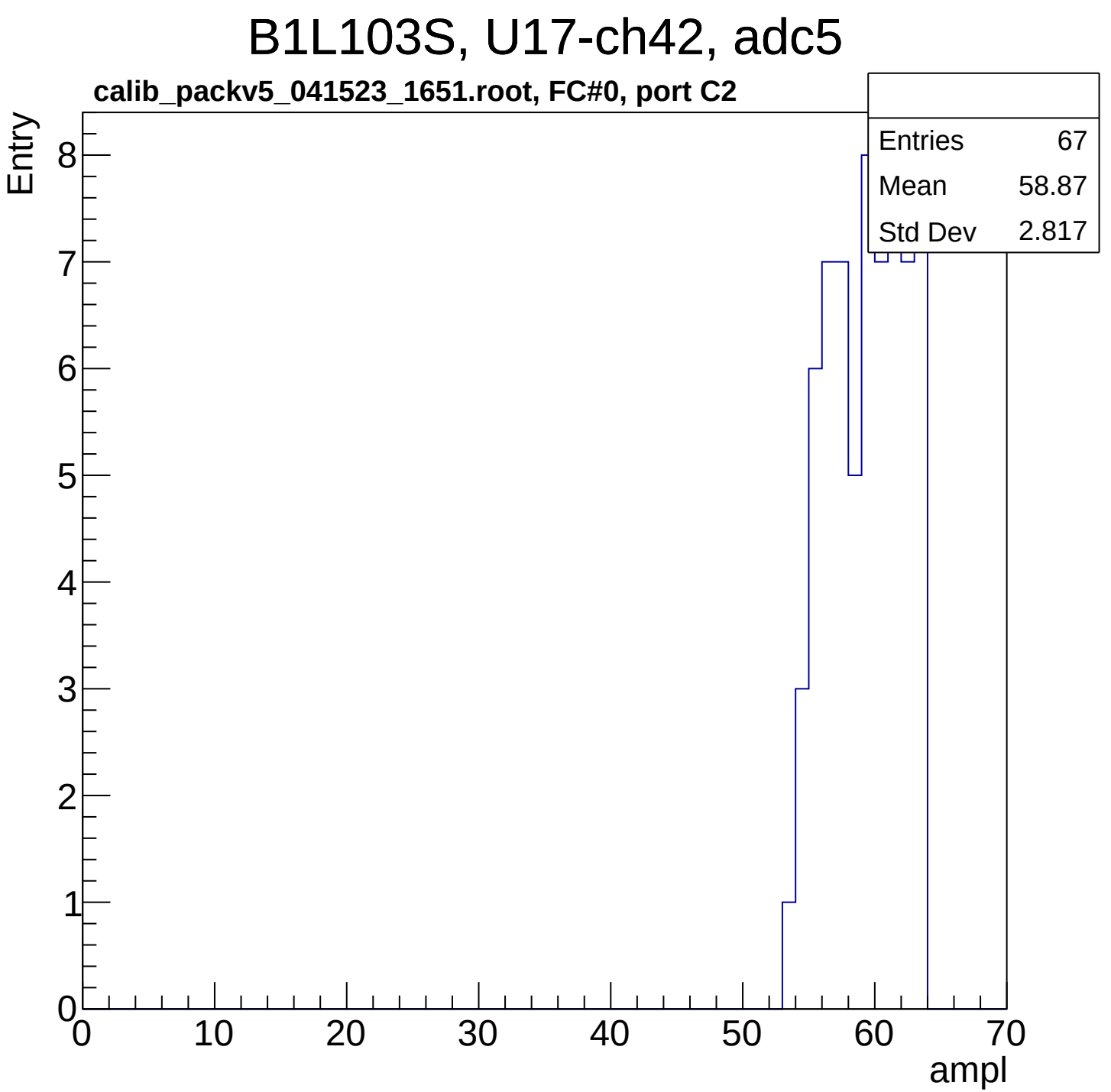

B1L103S, U17-ch42, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 24.13
Std Dev 11.15
Gaus mean : 28.8322
Gaus Width: 4.4401
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

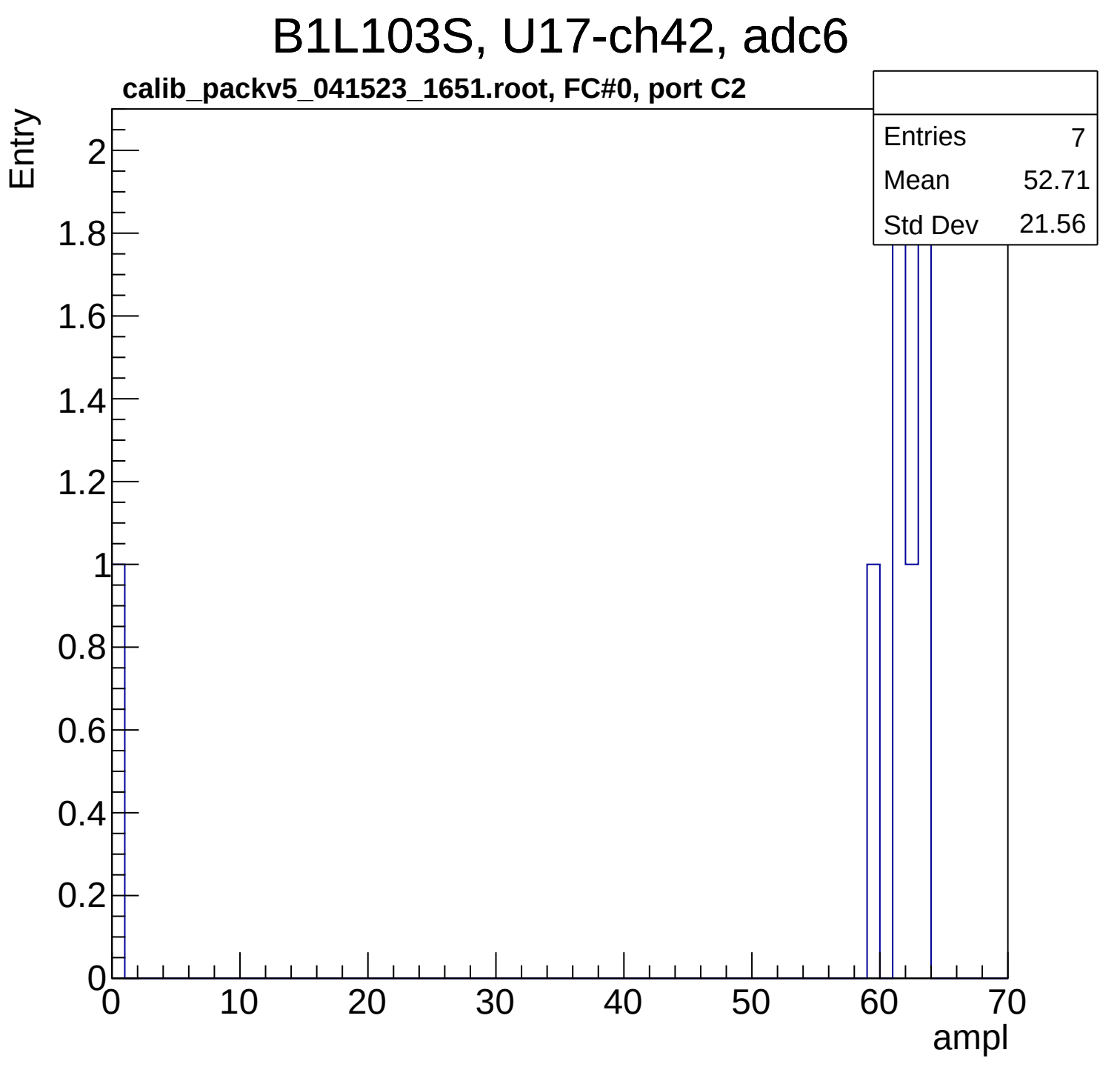

B1L103S, U17-ch42, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 35.15
Std Dev 5.836
Gaus mean : 35.8697
Gaus Width: 3.7937
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

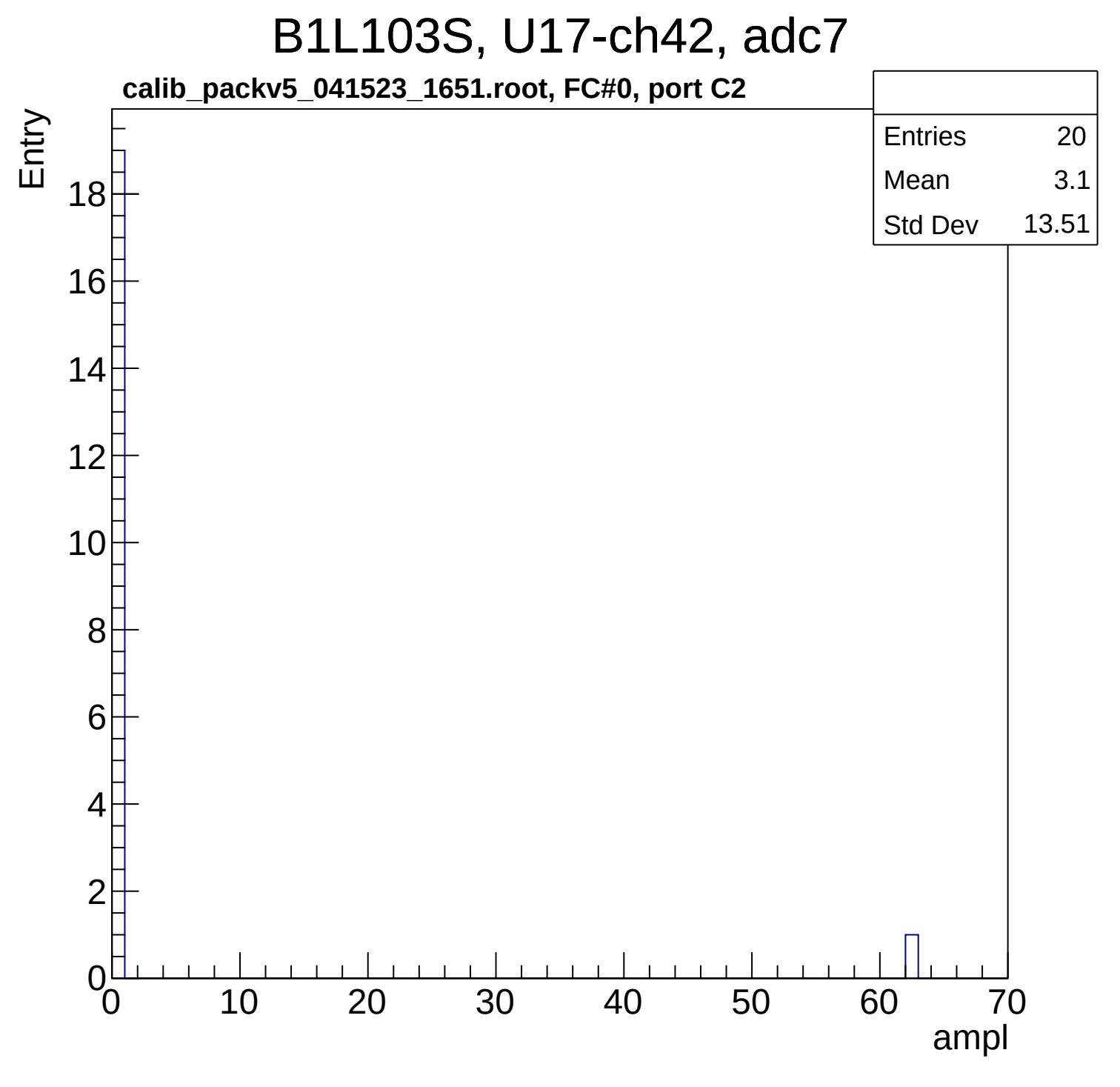

B1L103S, U17-ch42, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 40.06
Std Dev 9.118
Gaus mean : 42.1820
Gaus Width: 3.2283
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

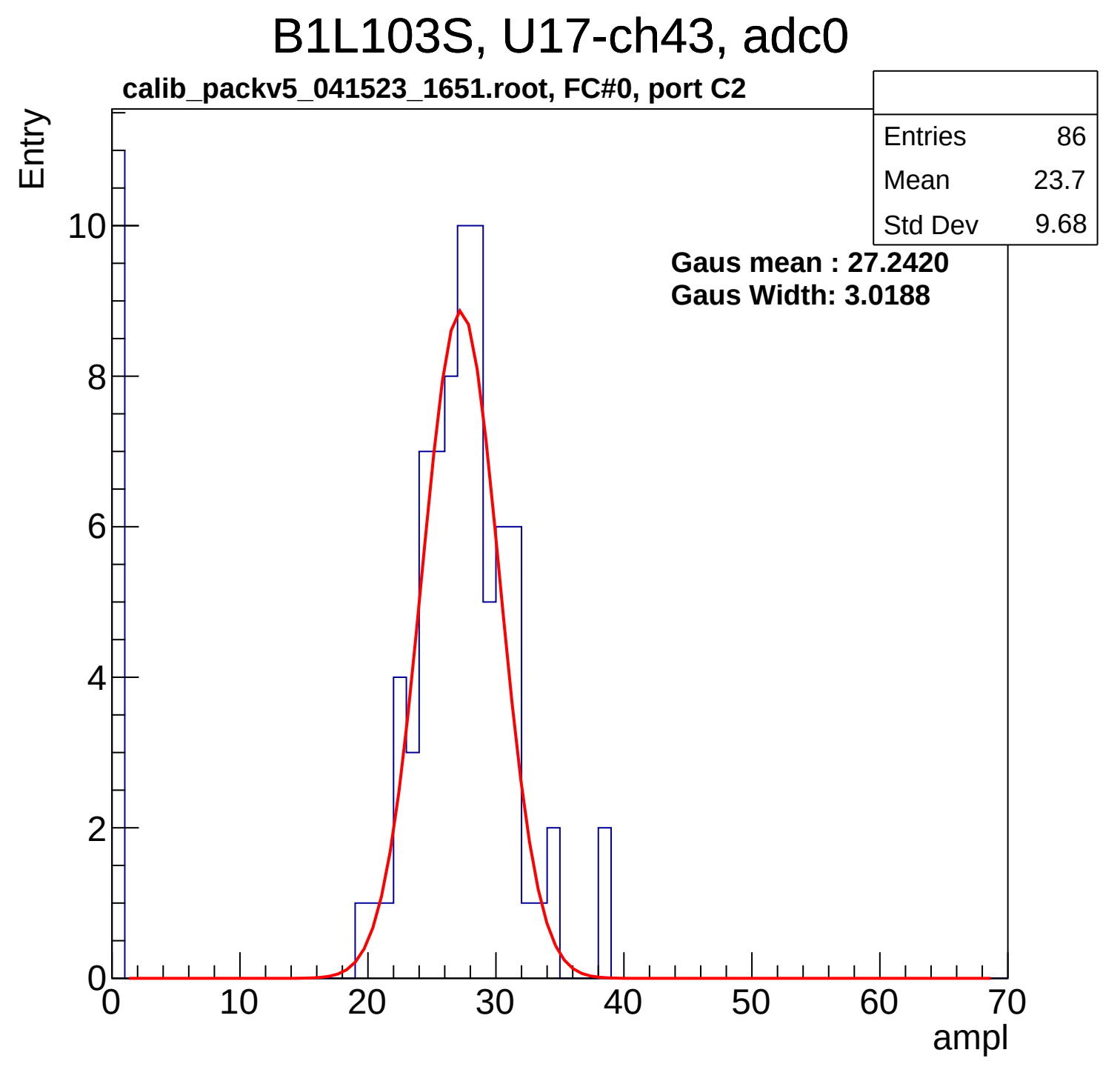

B1L103S, U17-ch42, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 42.78
Std Dev 16.29
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

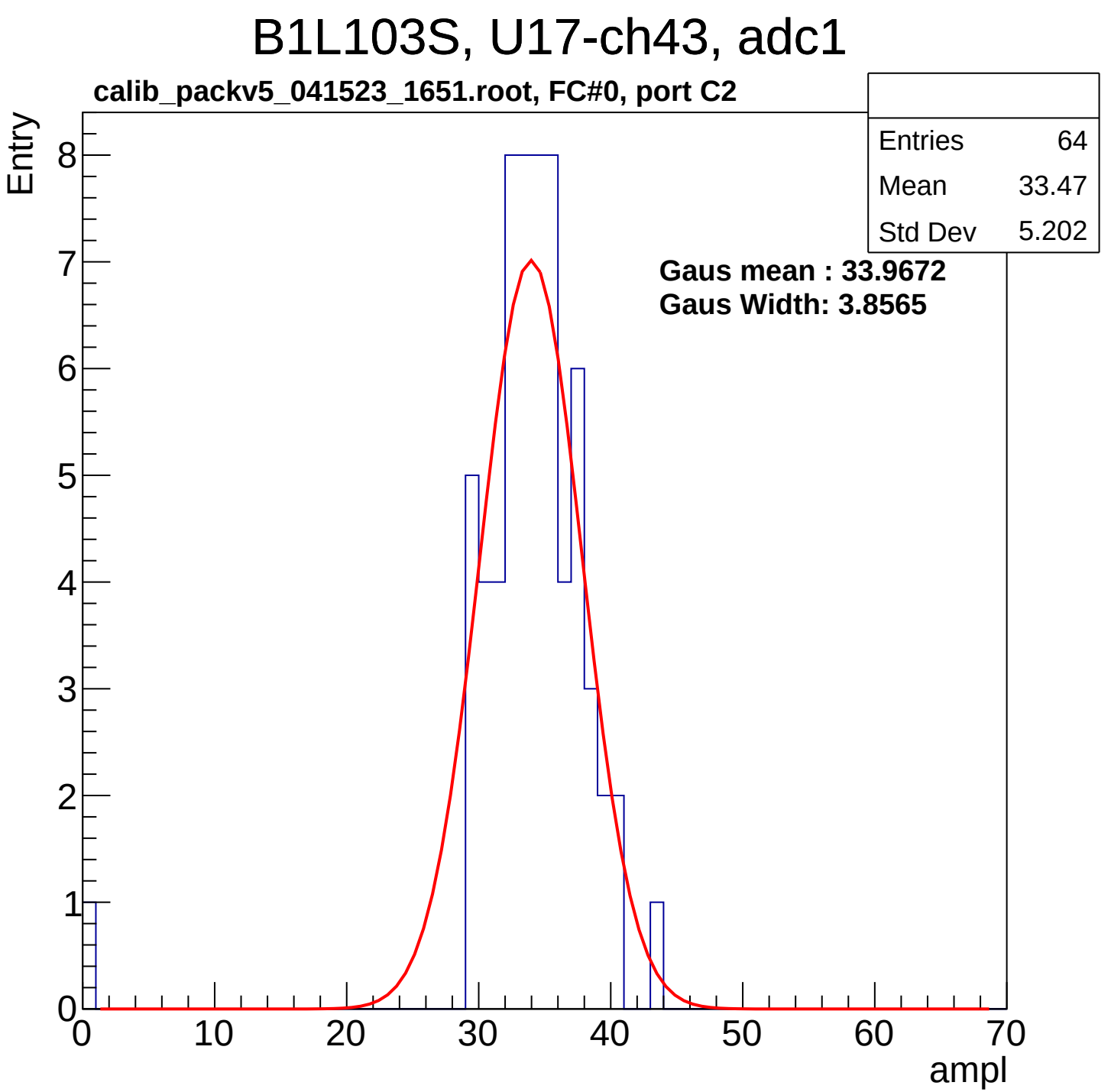

B1L103S, U17-ch42, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 52.95
Std Dev 8.857
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

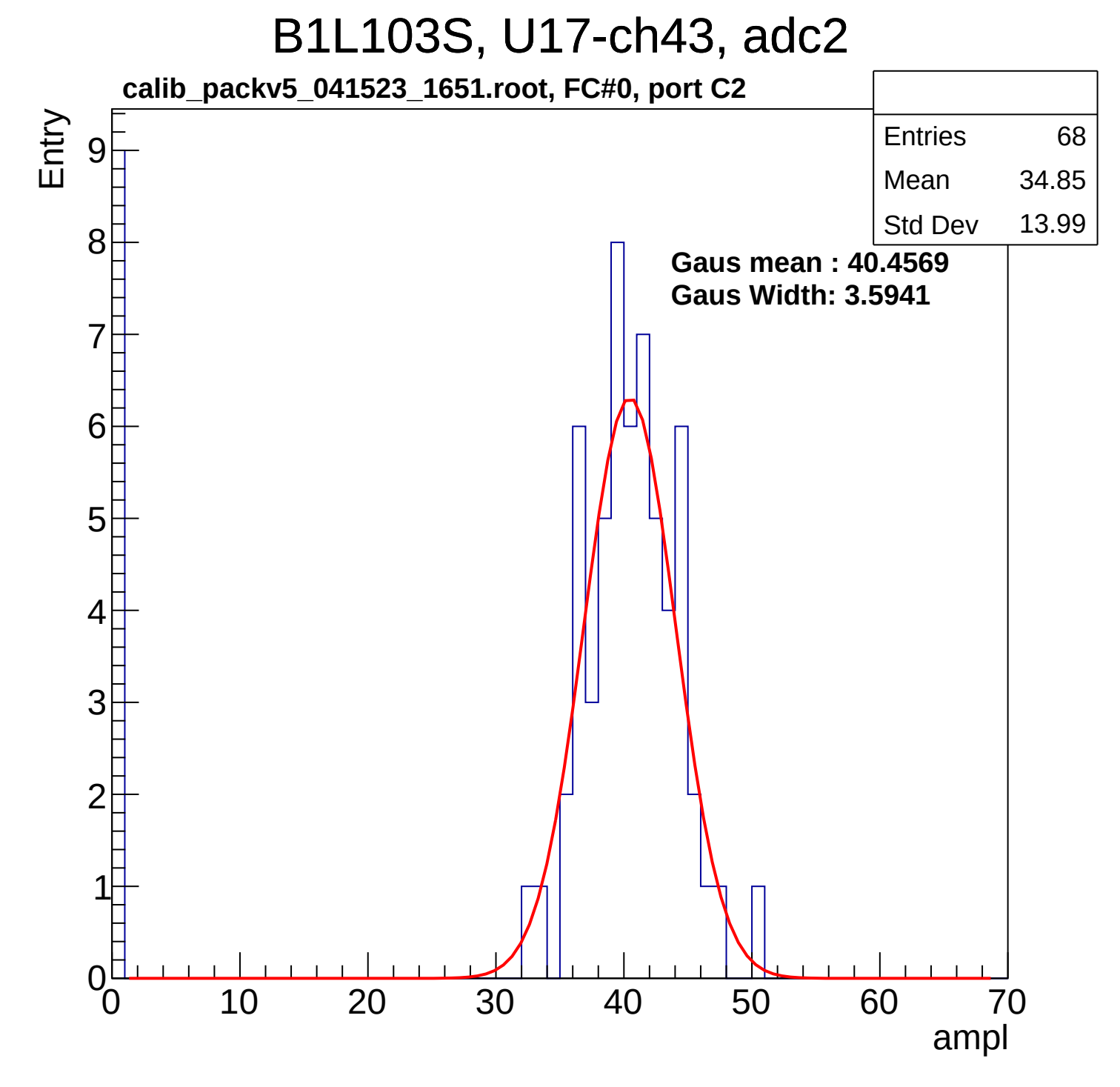

B1L103S, U17-ch42, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 58.87
Std Dev 2.817
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

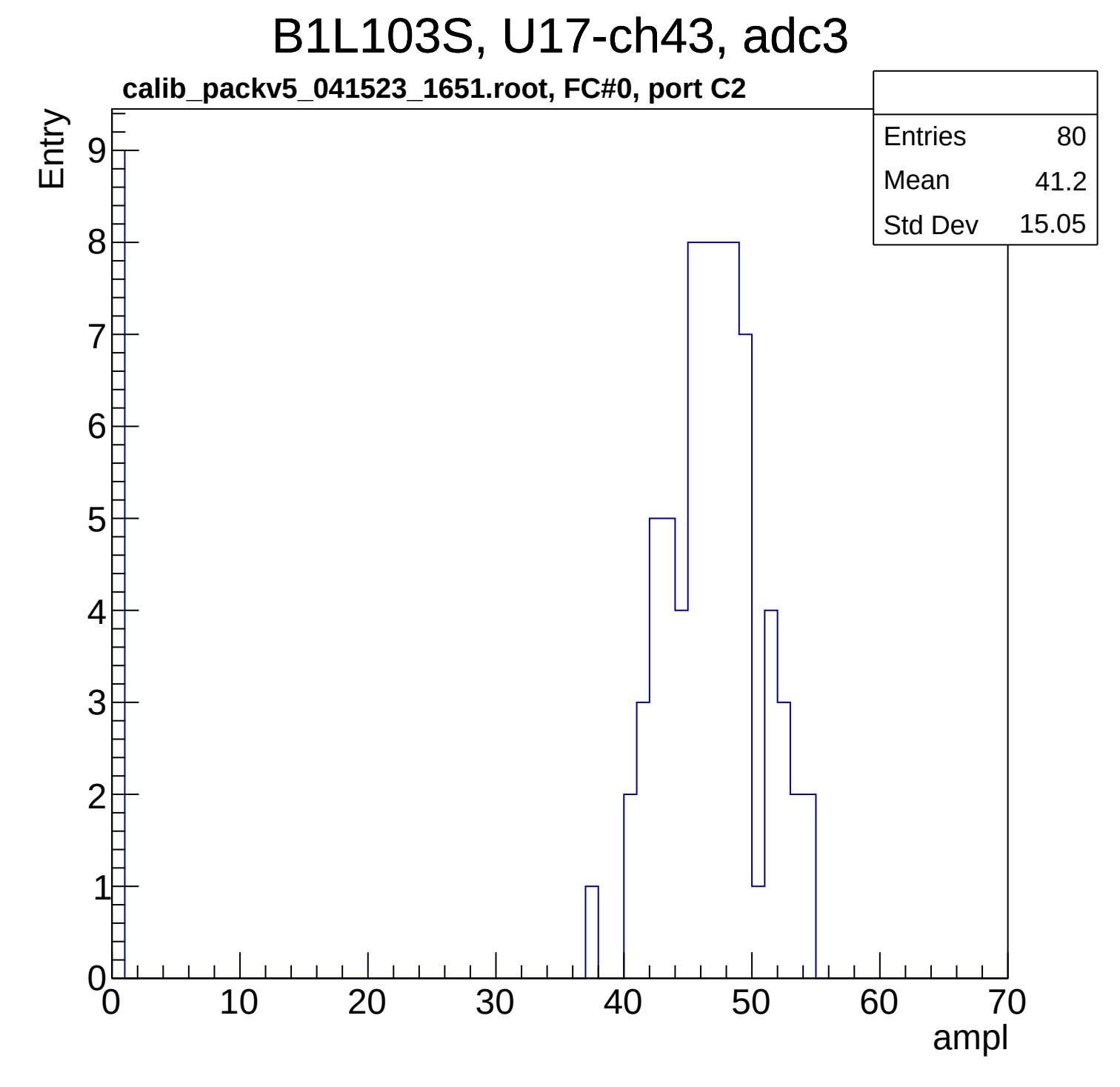

B1L103S, U17-ch42, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 52.71
Std Dev 21.56
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

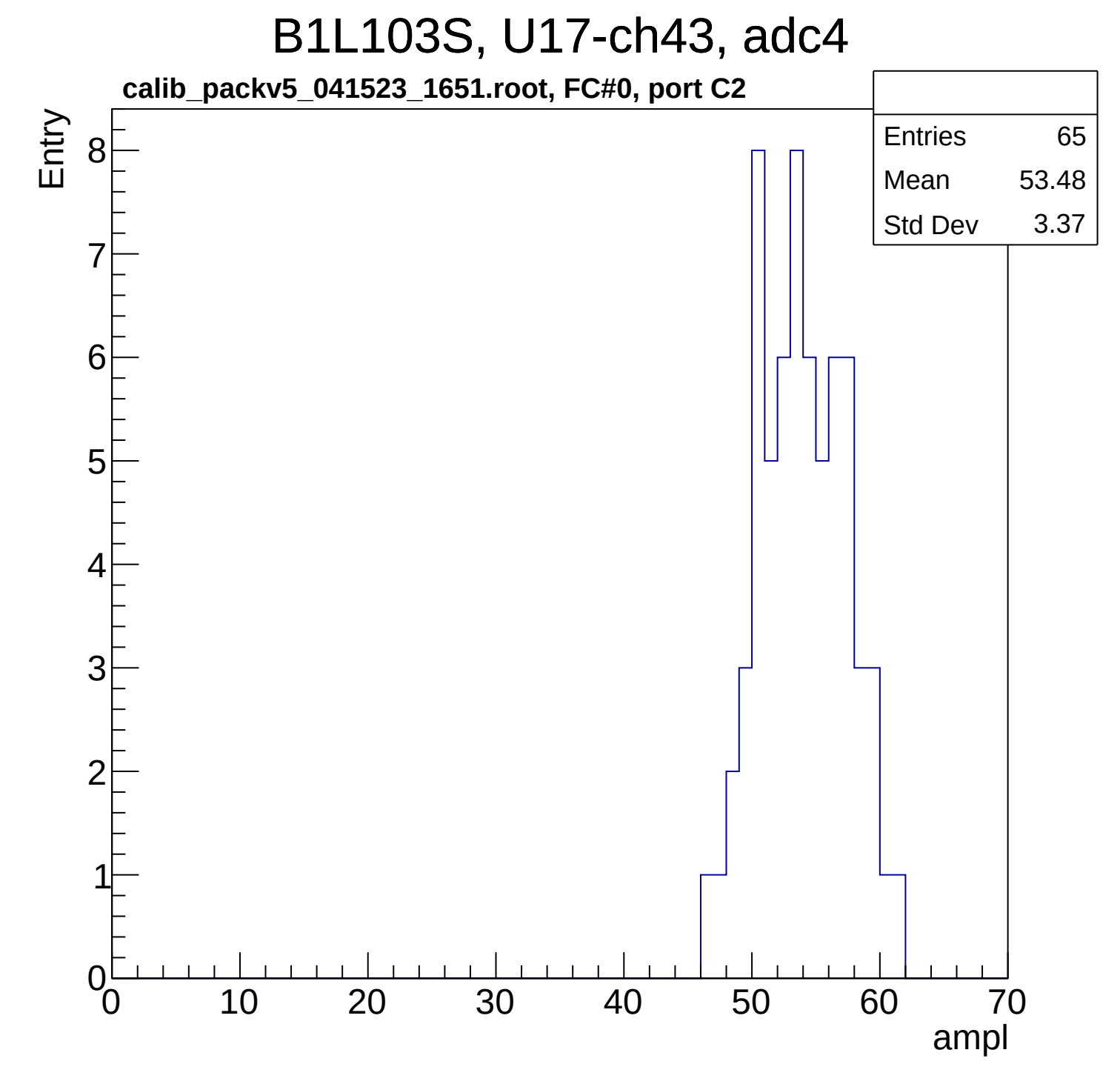

B1L103S, U17-ch42, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

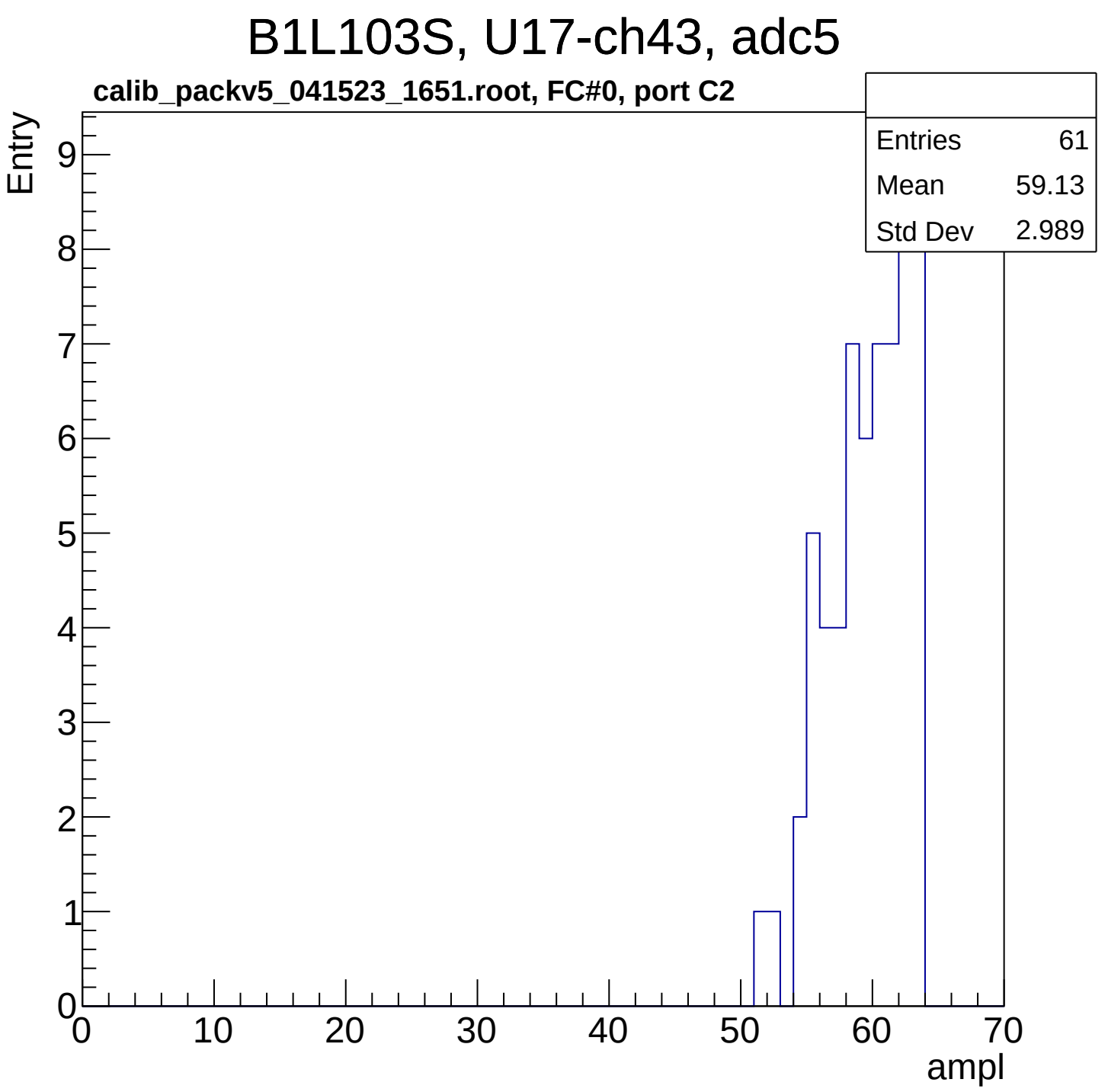

B1L103S, U17-ch43, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 23.7
Std Dev 9.68
Gaus mean : 27.2420
Gaus Width: 3.0188
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

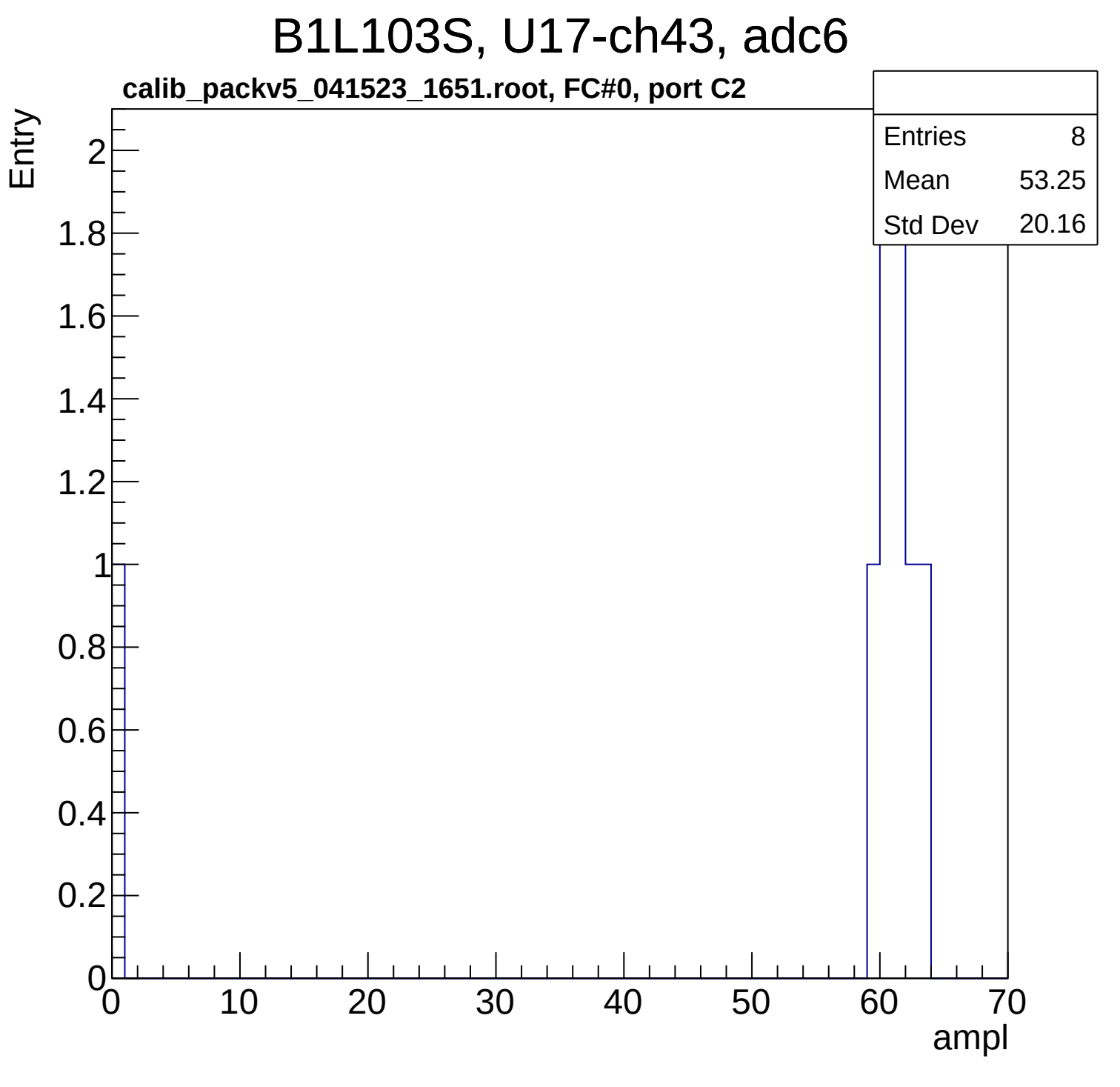

B1L103S, U17-ch43, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 33.47
Std Dev 5.202
Gaus mean : 33.9672
Gaus Width: 3.8565
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

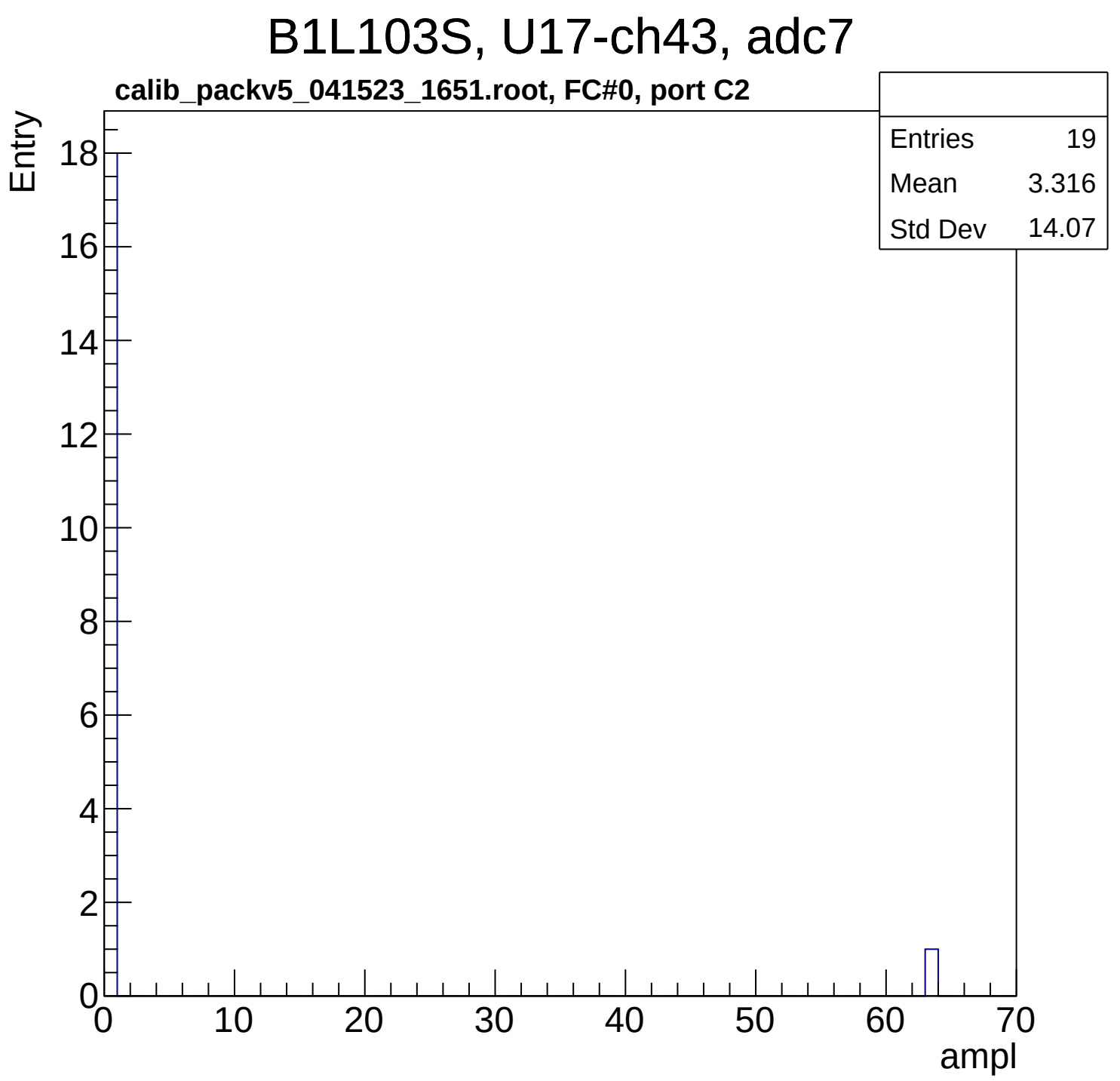

B1L103S, U17-ch43, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 34.85
Std Dev 13.99
Gaus mean : 40.4569
Gaus Width: 3.5941
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

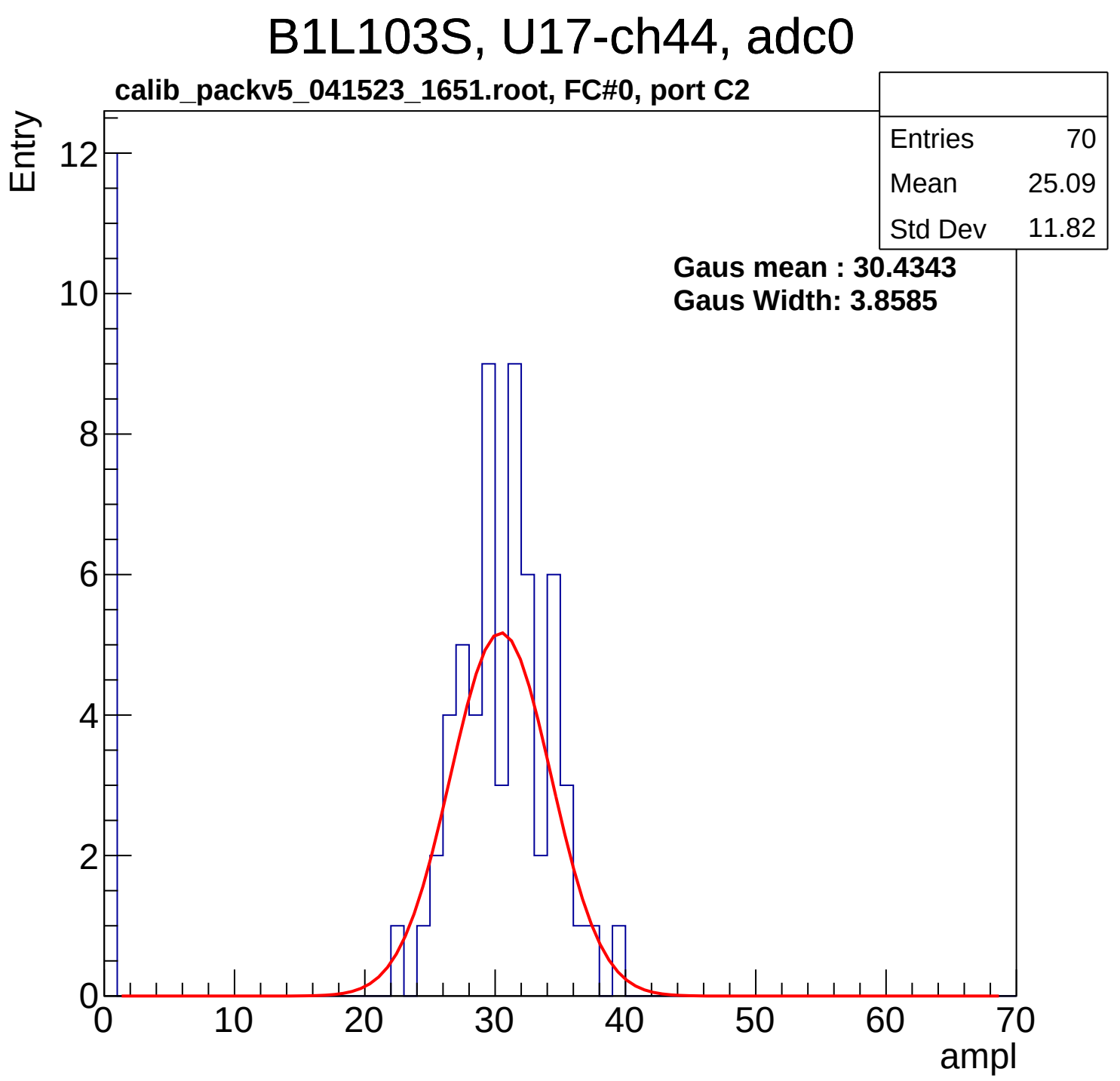

B1L103S, U17-ch43, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 41.2
Std Dev 15.05
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

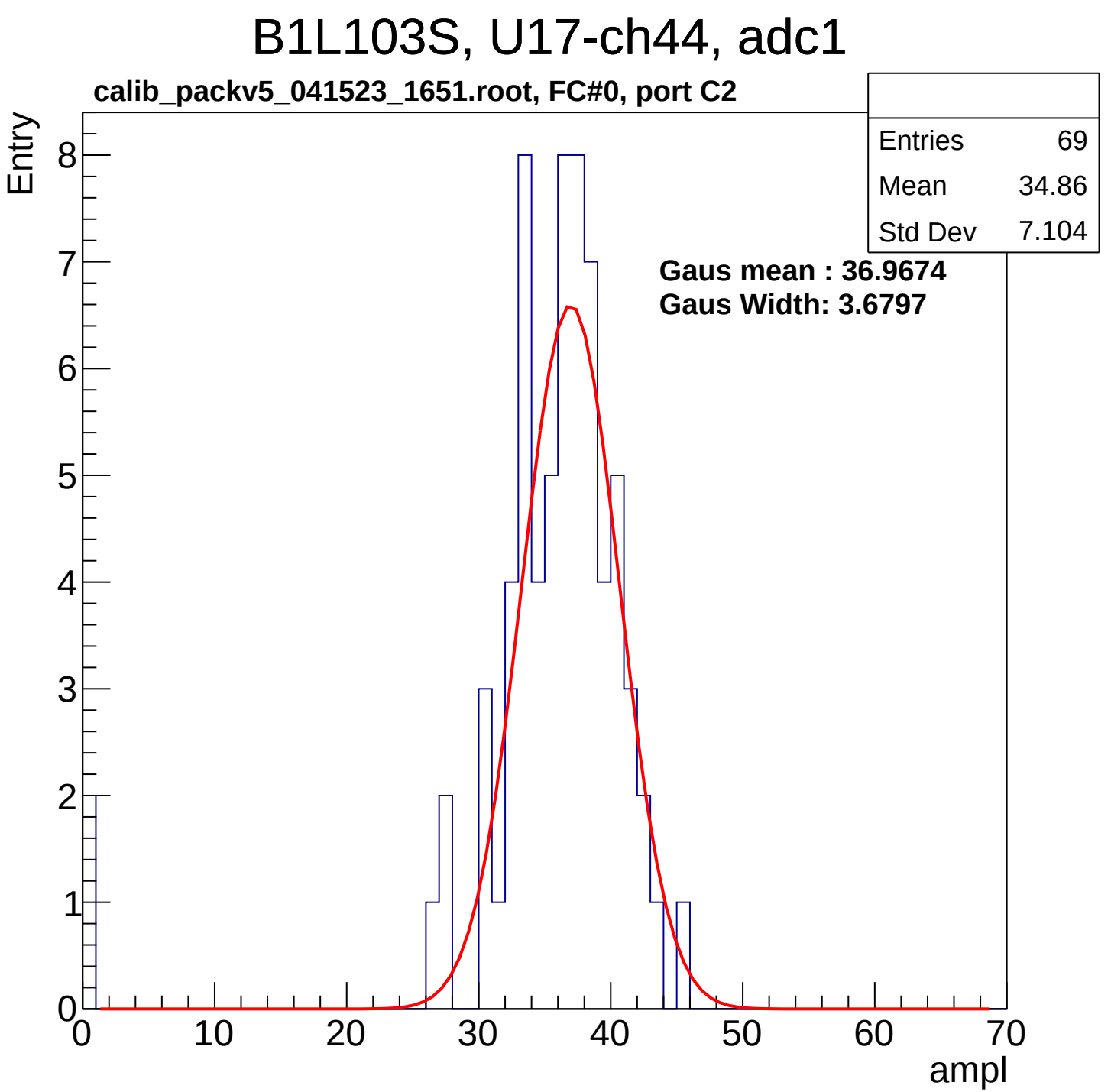

B1L103S, U17-ch43, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 53.48
Std Dev 3.37
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

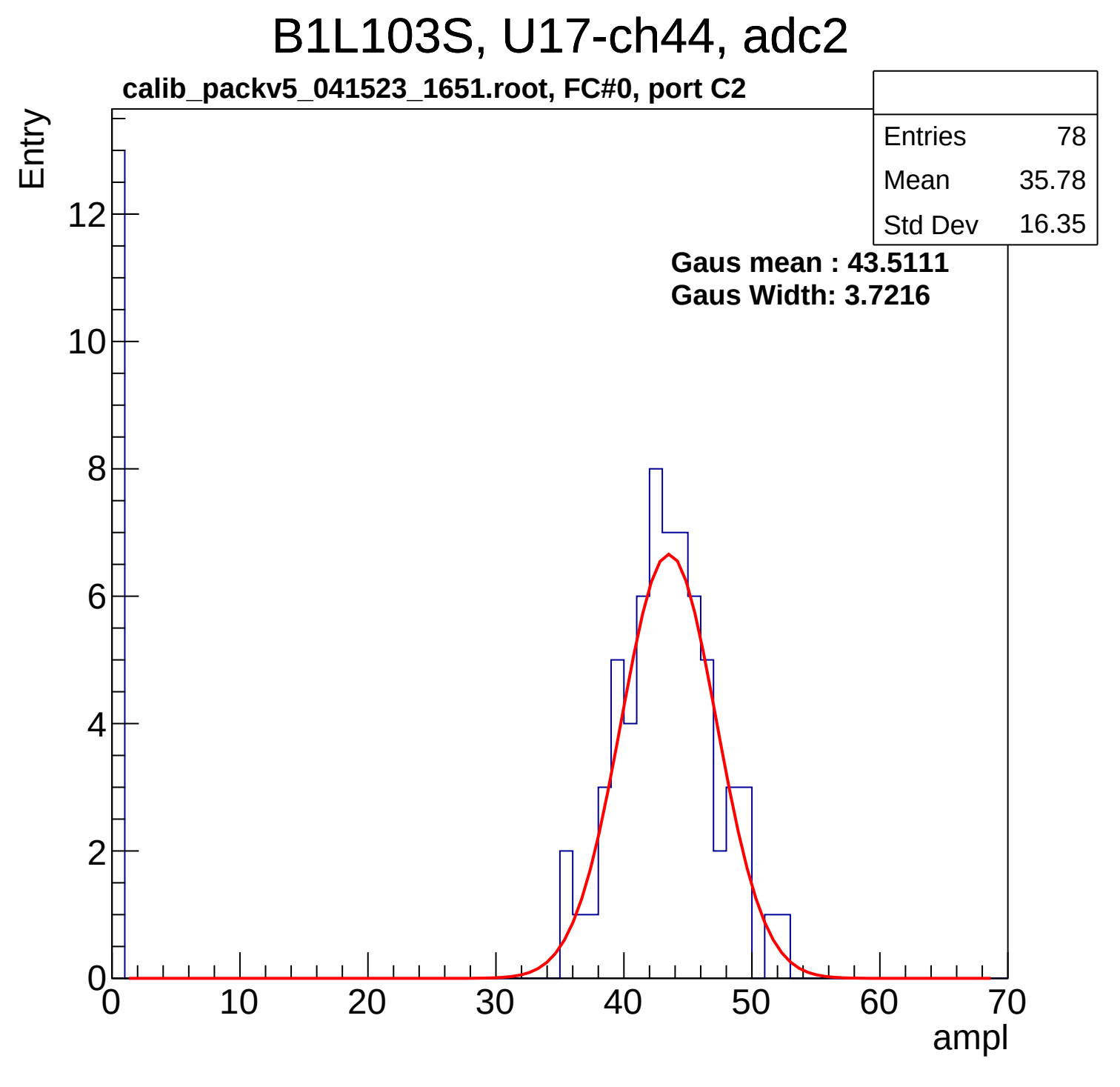

B1L103S, U17-ch43, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 59.13
Std Dev 2.989
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

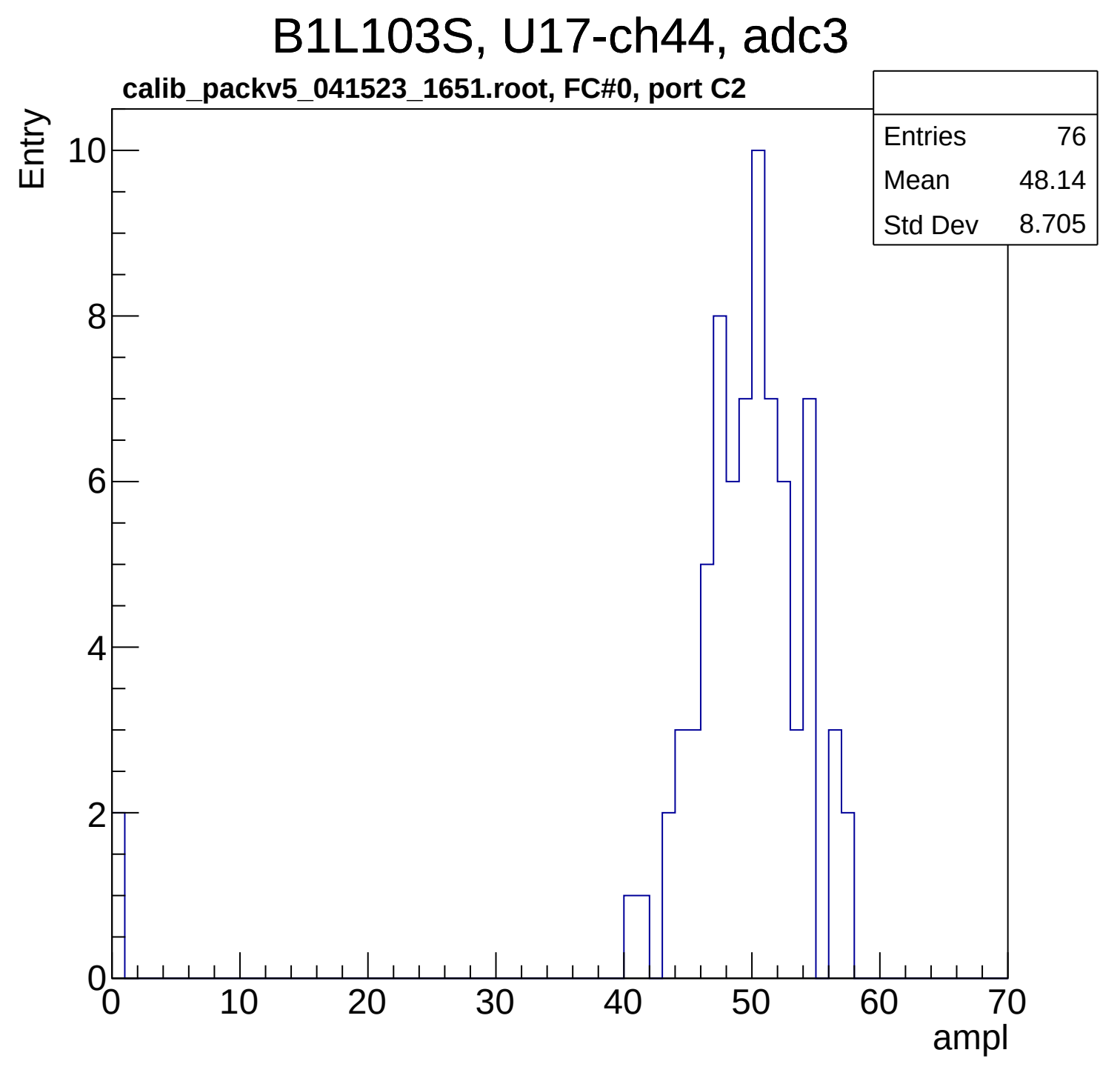

B1L103S, U17-ch43, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 53.25
Std Dev 20.16
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

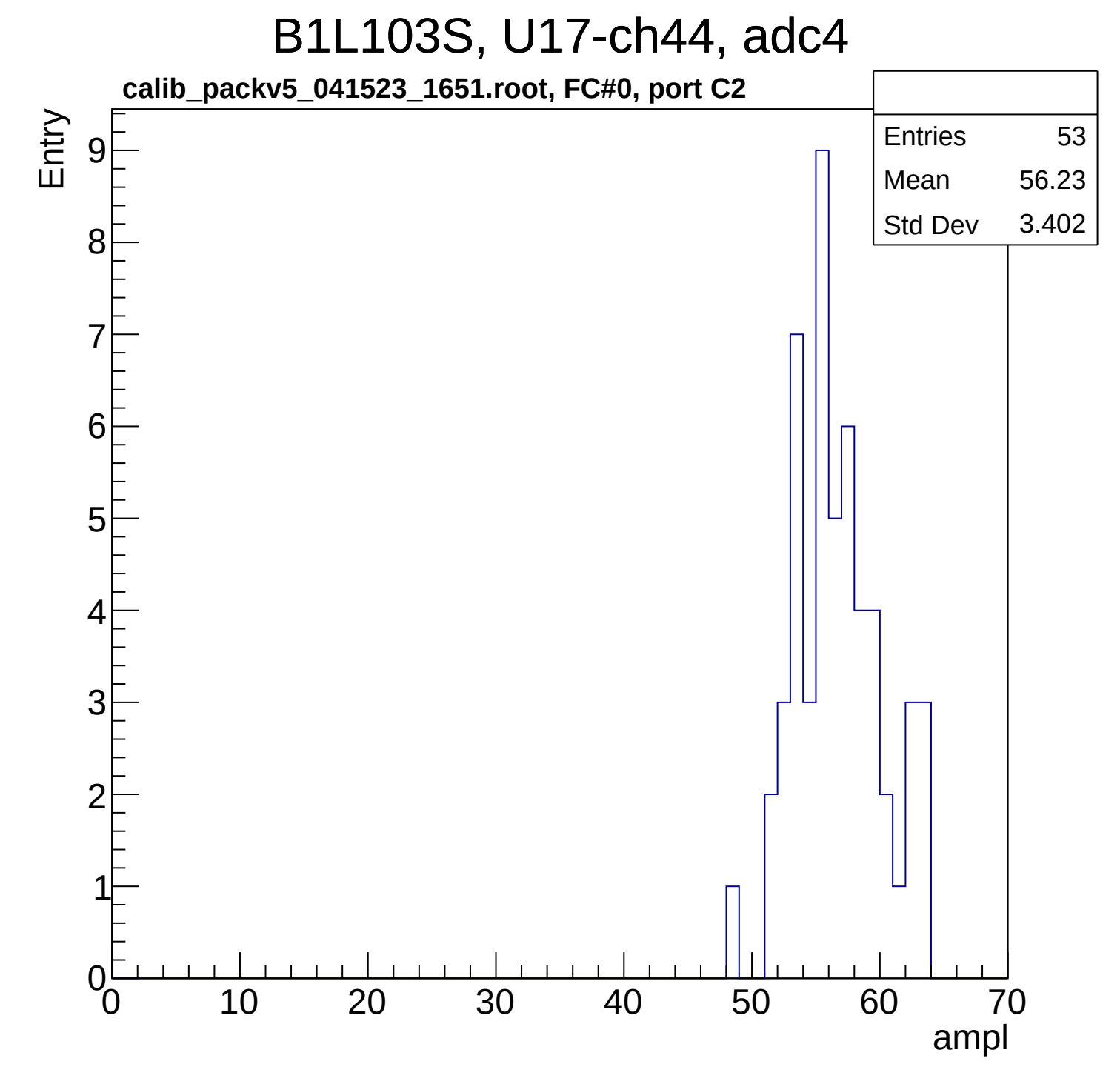

B1L103S, U17-ch43, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

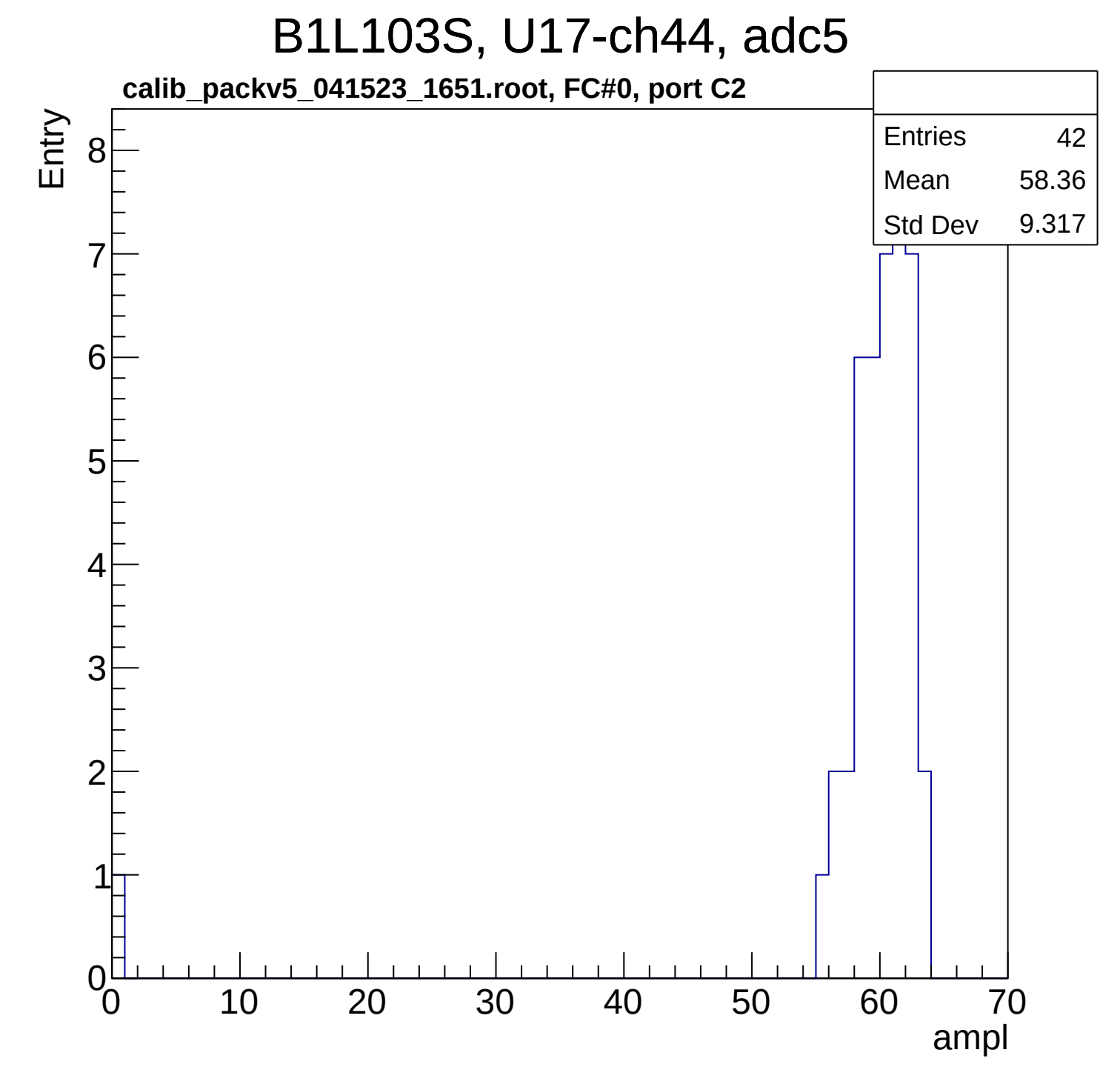

B1L103S, U17-ch44, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 25.09
Std Dev 11.82
Gaus mean : 30.4343
Gaus Width: 3.8585
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

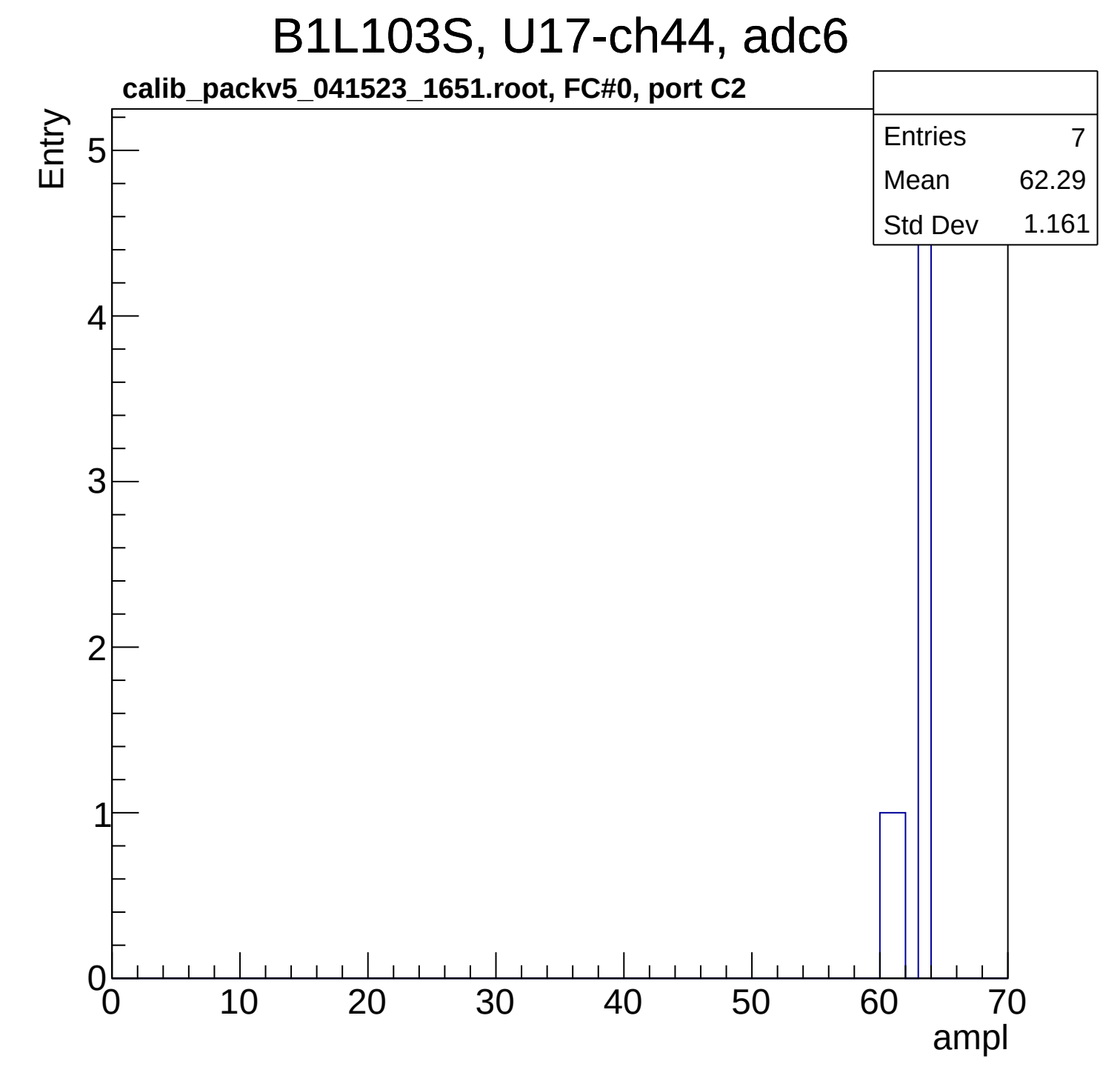

B1L103S, U17-ch44, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 34.86
Std Dev 7.104
Gaus mean : 36.9674
Gaus Width: 3.6797
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

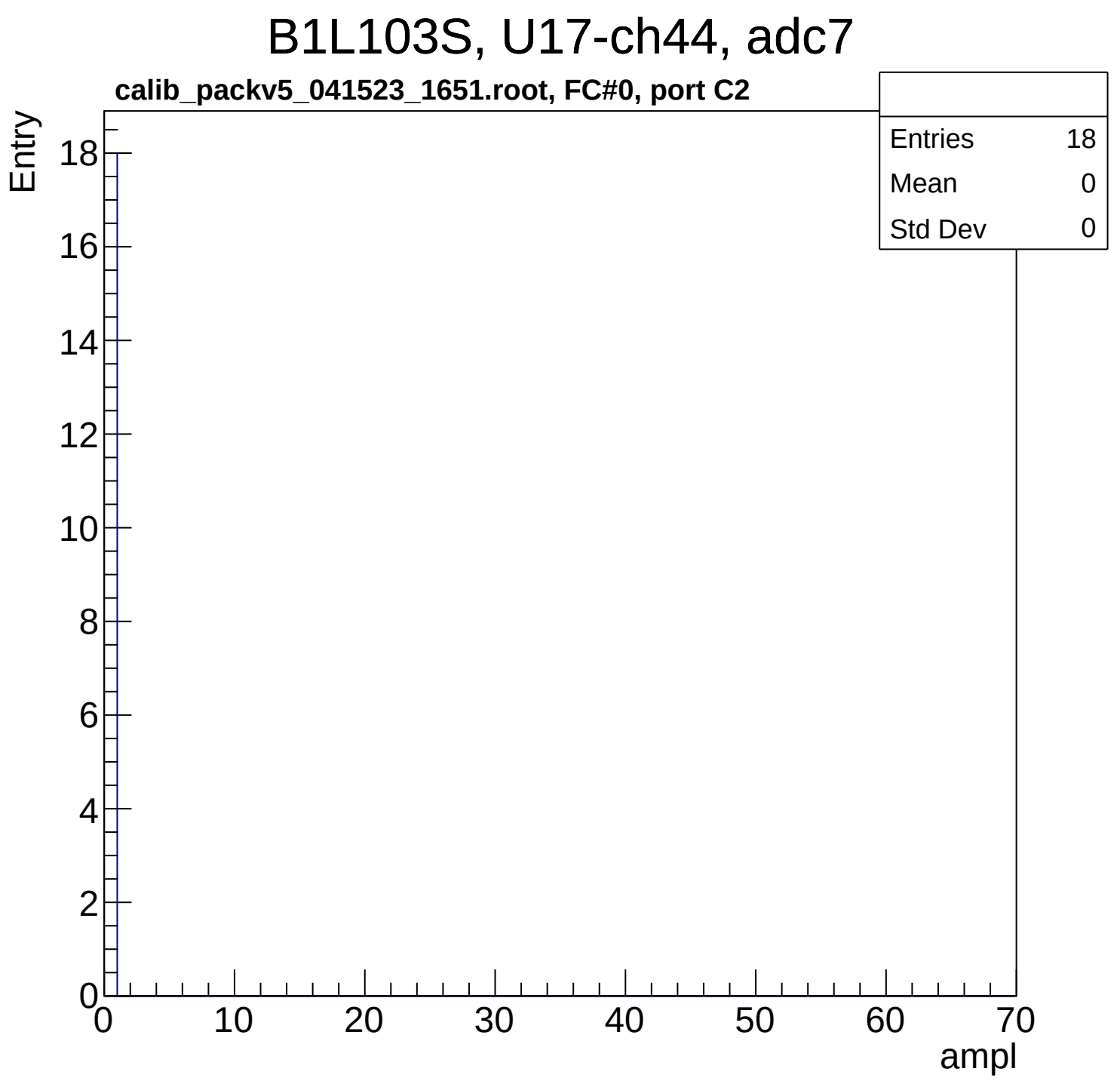

B1L103S, U17-ch44, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 35.78
Std Dev 16.35
Gaus mean : 43.5111
Gaus Width: 3.7216
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

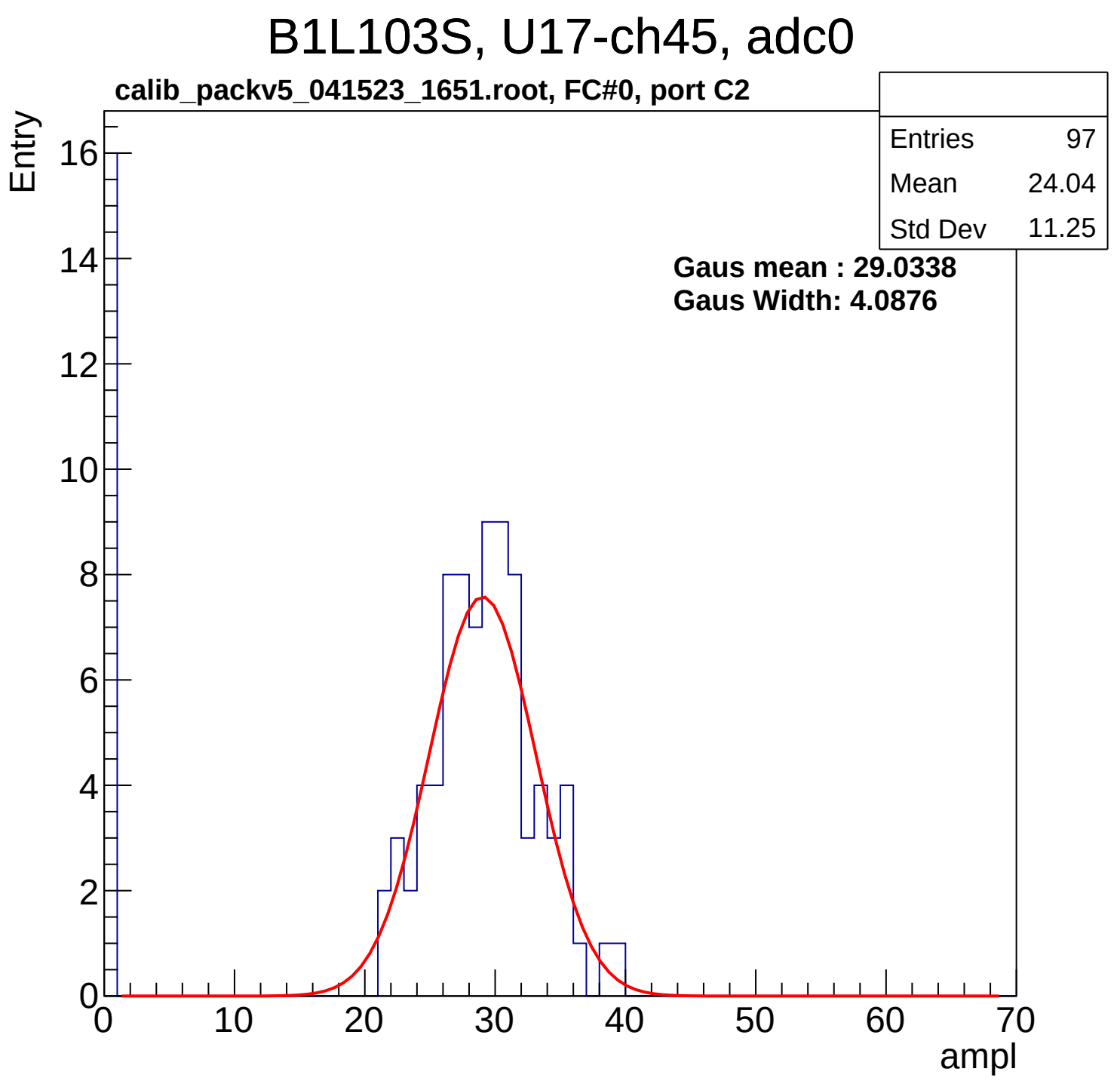

B1L103S, U17-ch44, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 48.14
Std Dev 8.705
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

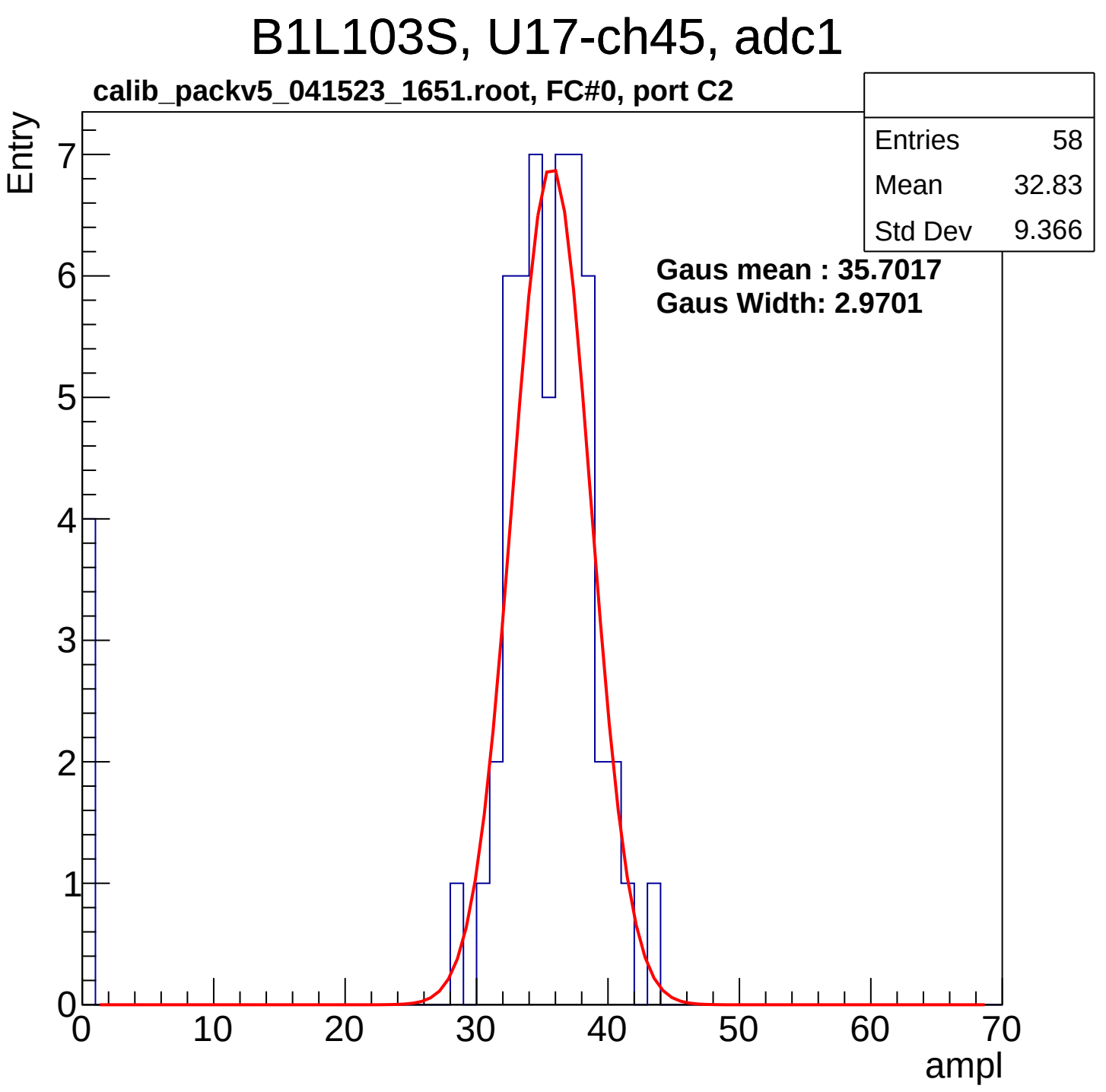

B1L103S, U17-ch44, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 56.23
Std Dev 3.402
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

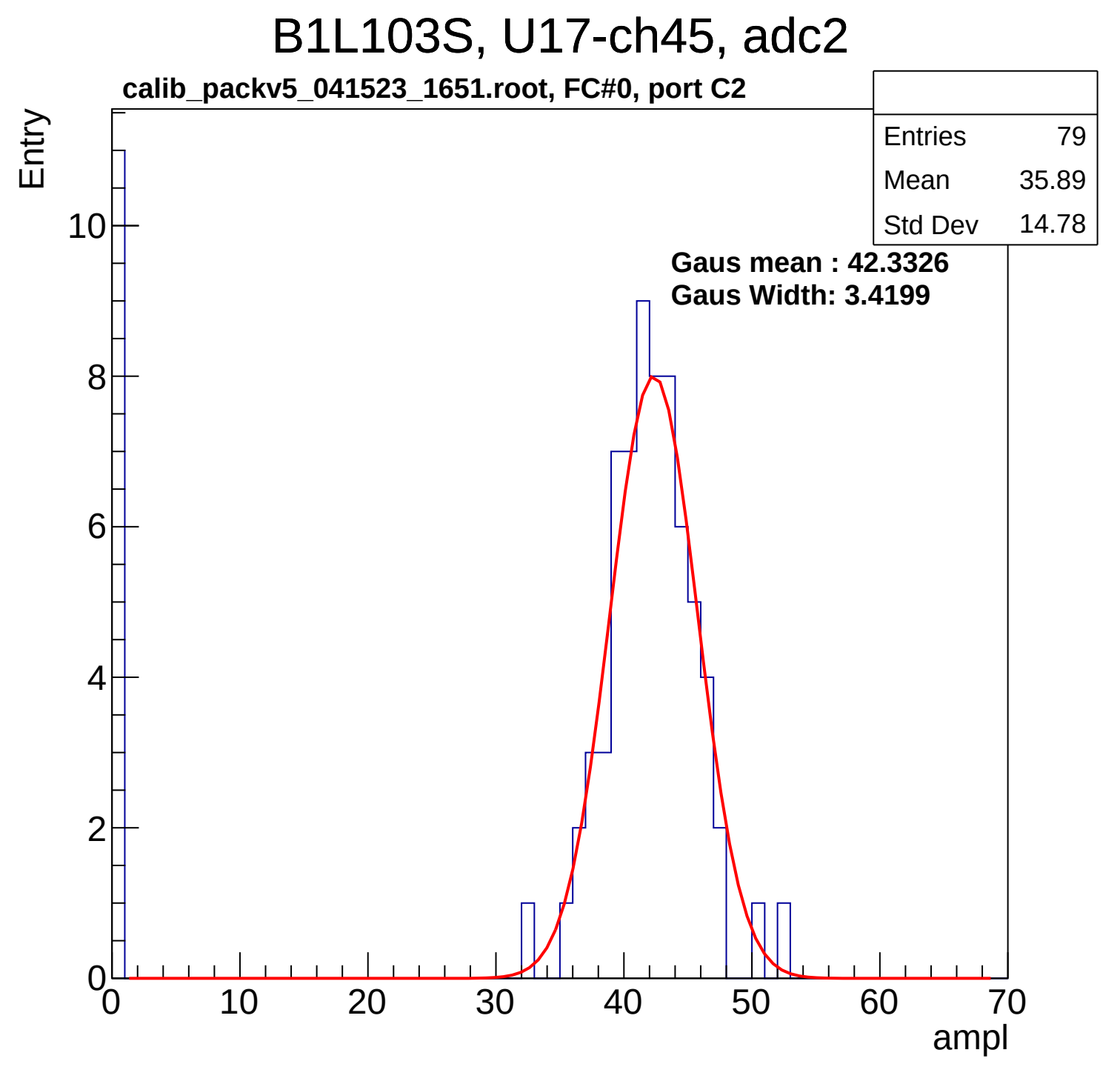

B1L103S, U17-ch44, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 58.36
Std Dev 9.317
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

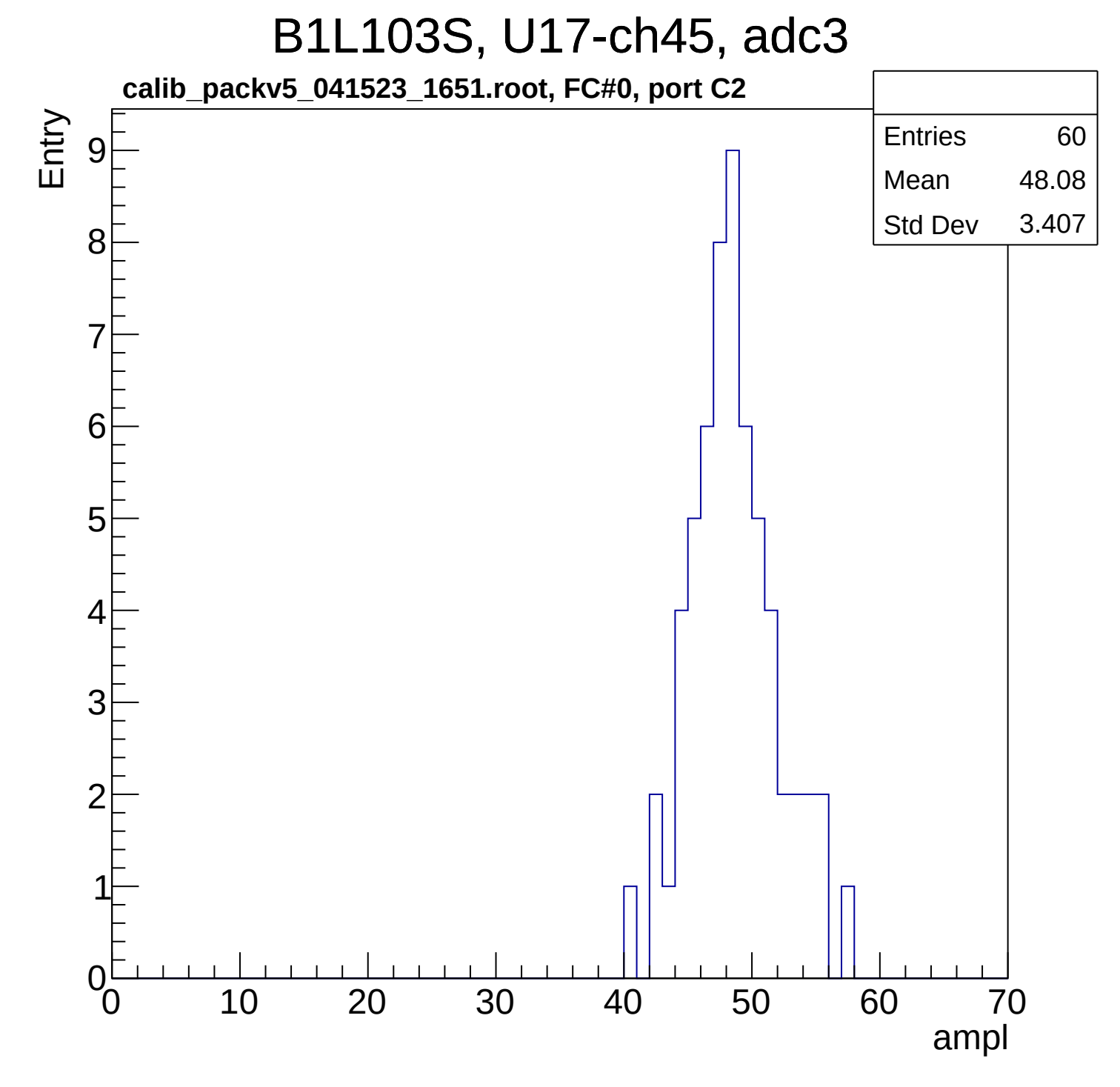

B1L103S, U17-ch44, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62.29
Std Dev 1.161
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

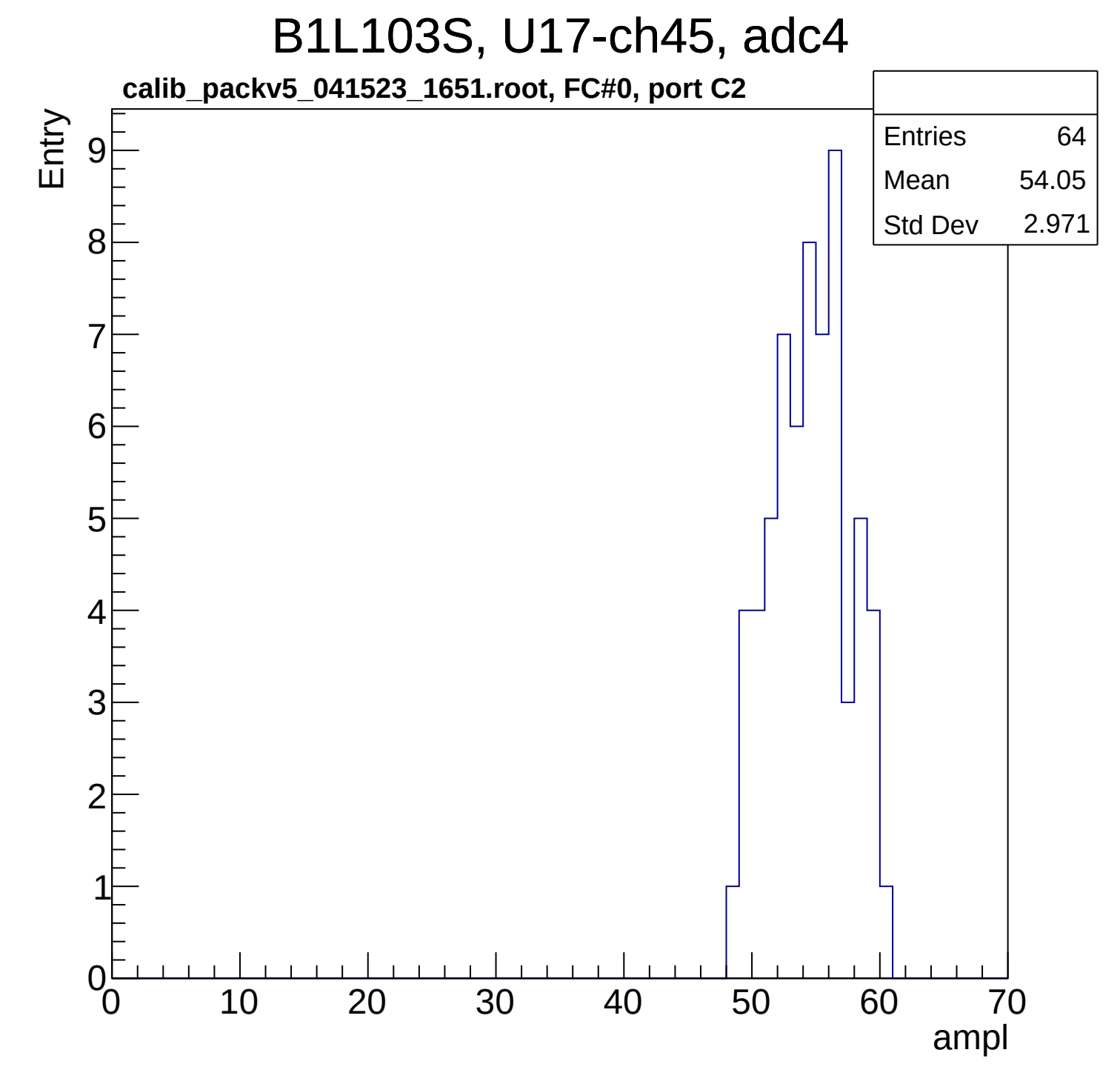

B1L103S, U17-ch44, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

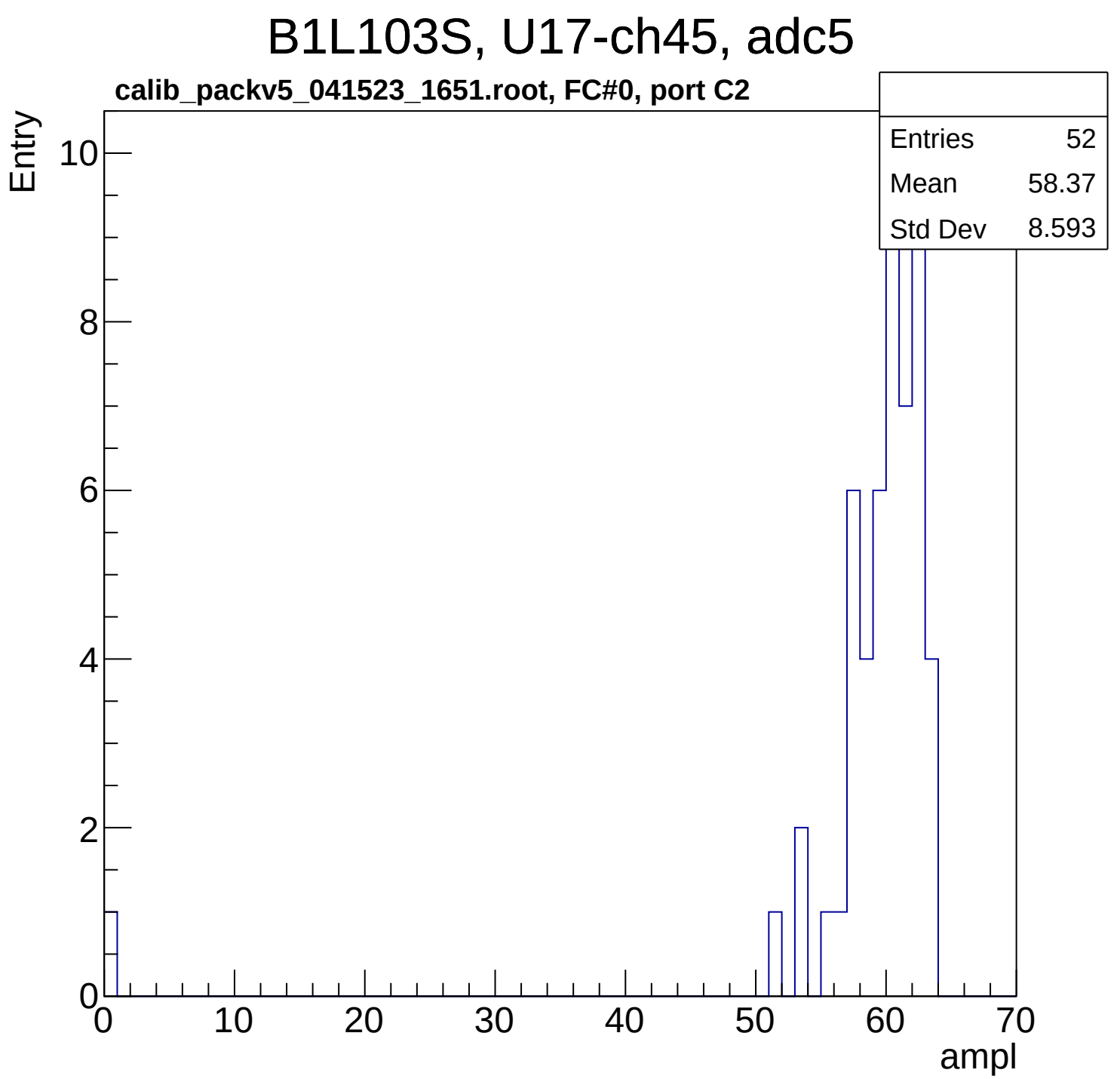

B1L103S, U17-ch45, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 24.04
Std Dev 11.25
Gaus mean : 29.0338
Gaus Width: 4.0876
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

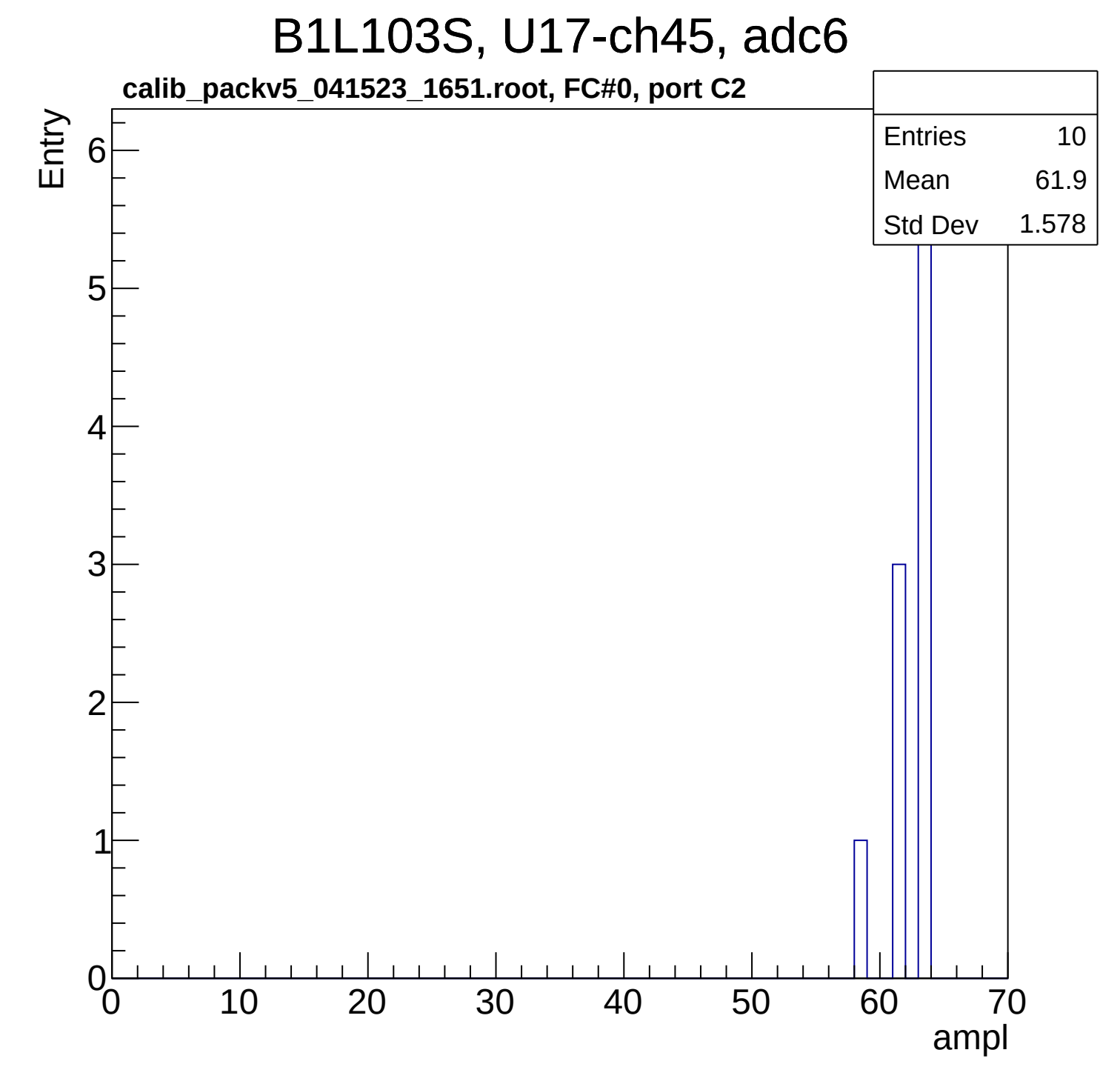

B1L103S, U17-ch45, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 32.83
Std Dev 9.366
Gaus mean : 35.7017
Gaus Width: 2.9701
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

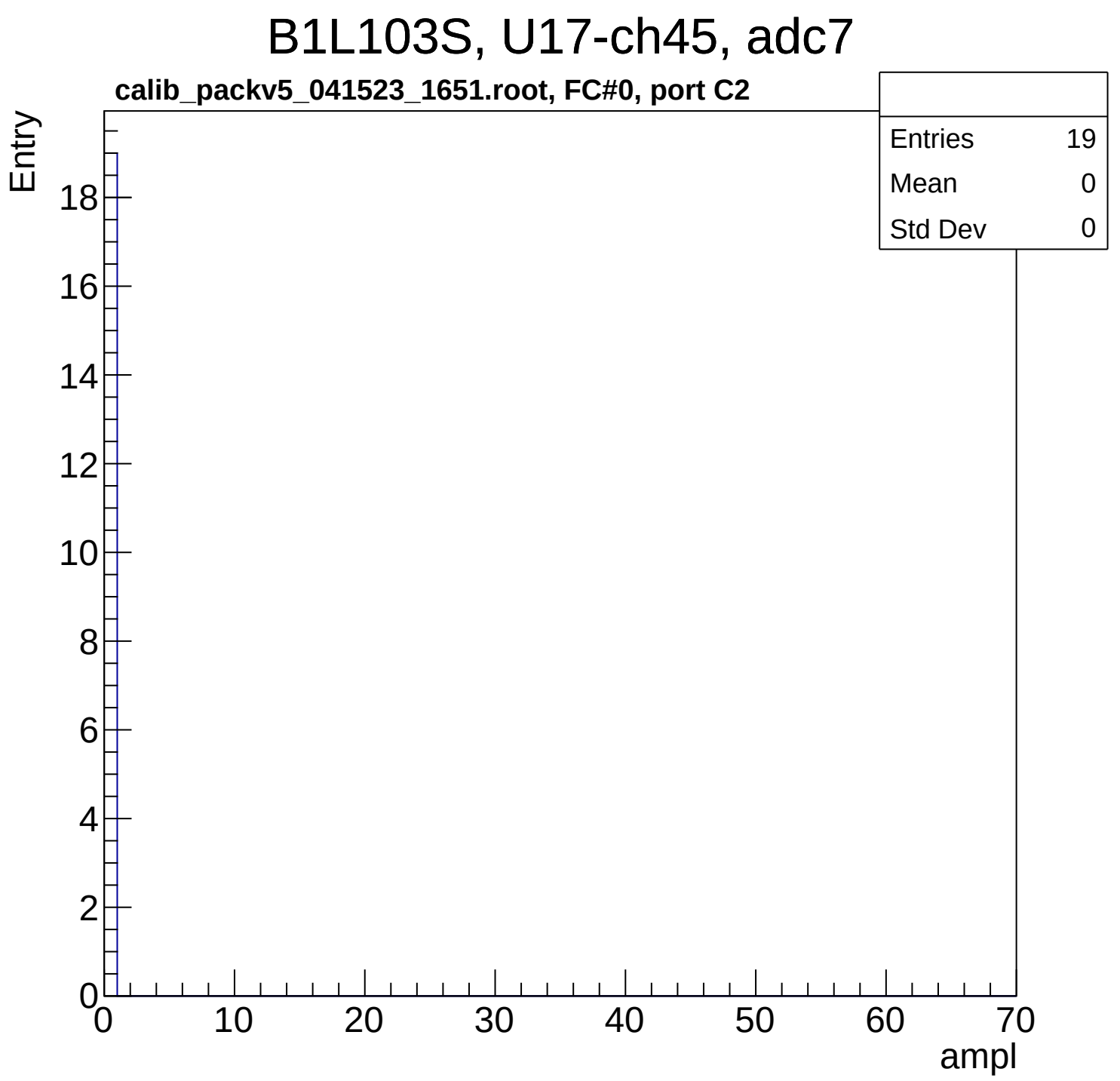

B1L103S, U17-ch45, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 35.89
Std Dev 14.78
Gaus mean : 42.3326
Gaus Width: 3.4199
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

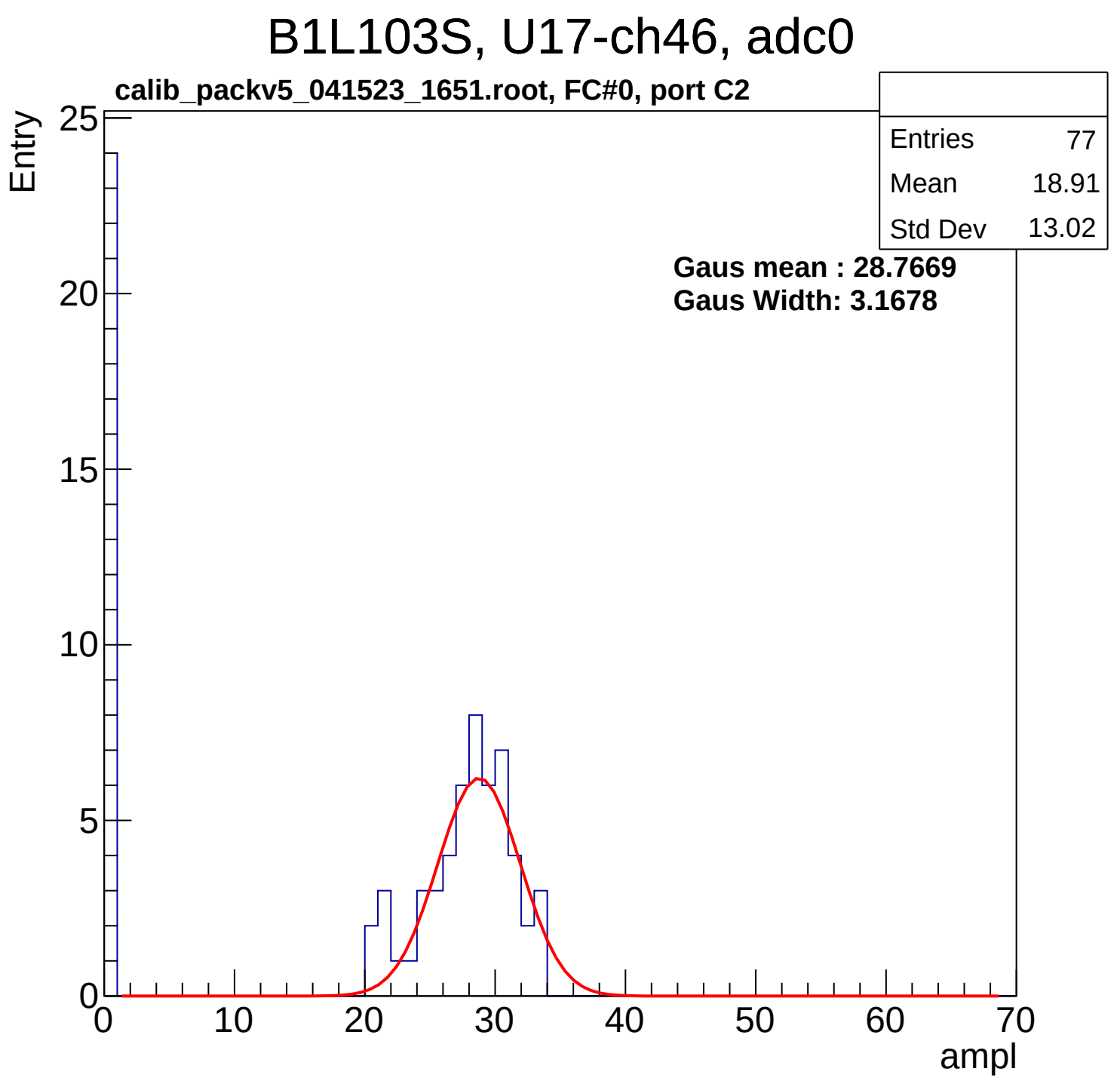

B1L103S, U17-ch45, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 48.08
Std Dev 3.407
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

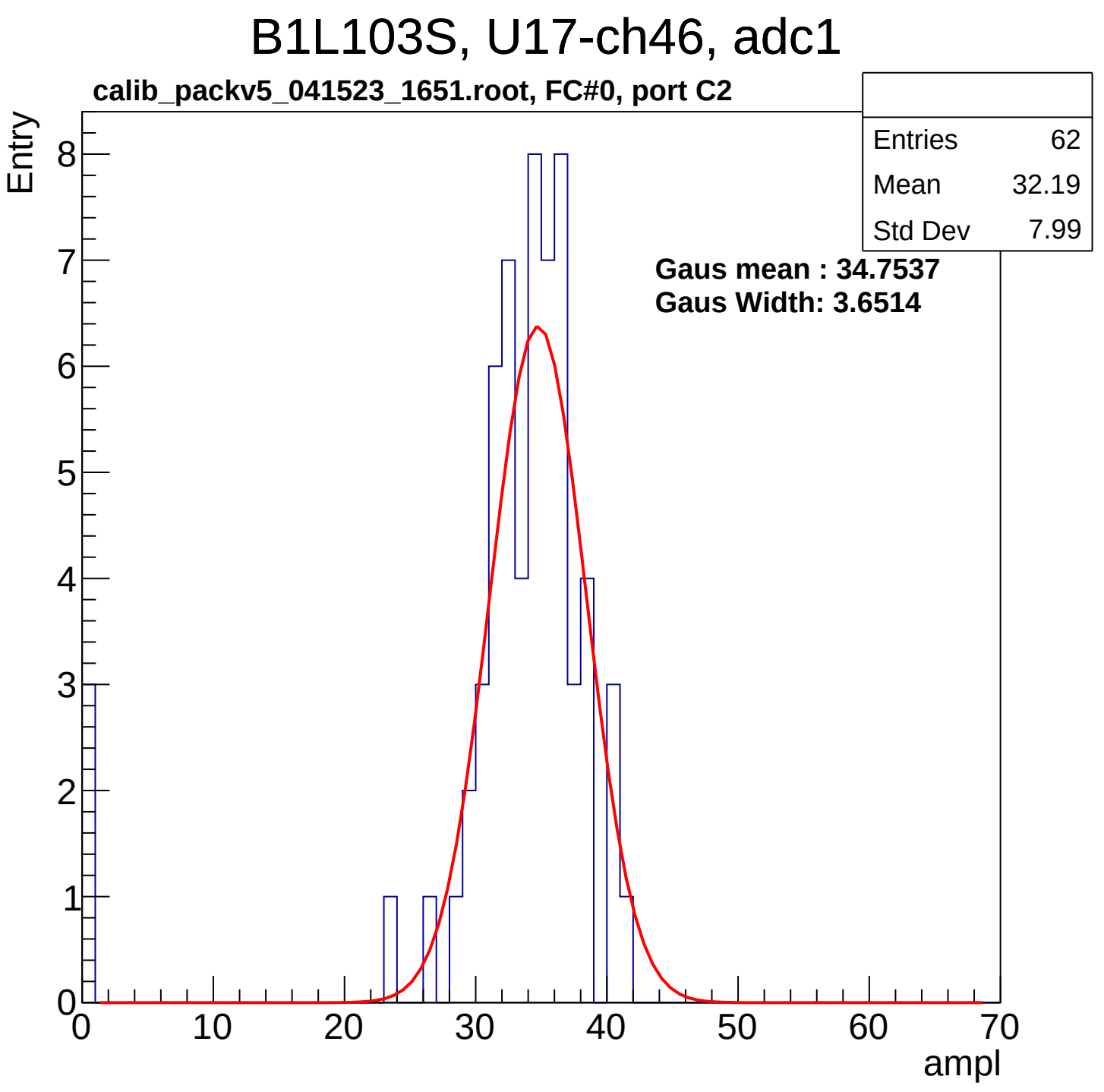

B1L103S, U17-ch45, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 54.05
Std Dev 2.971
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

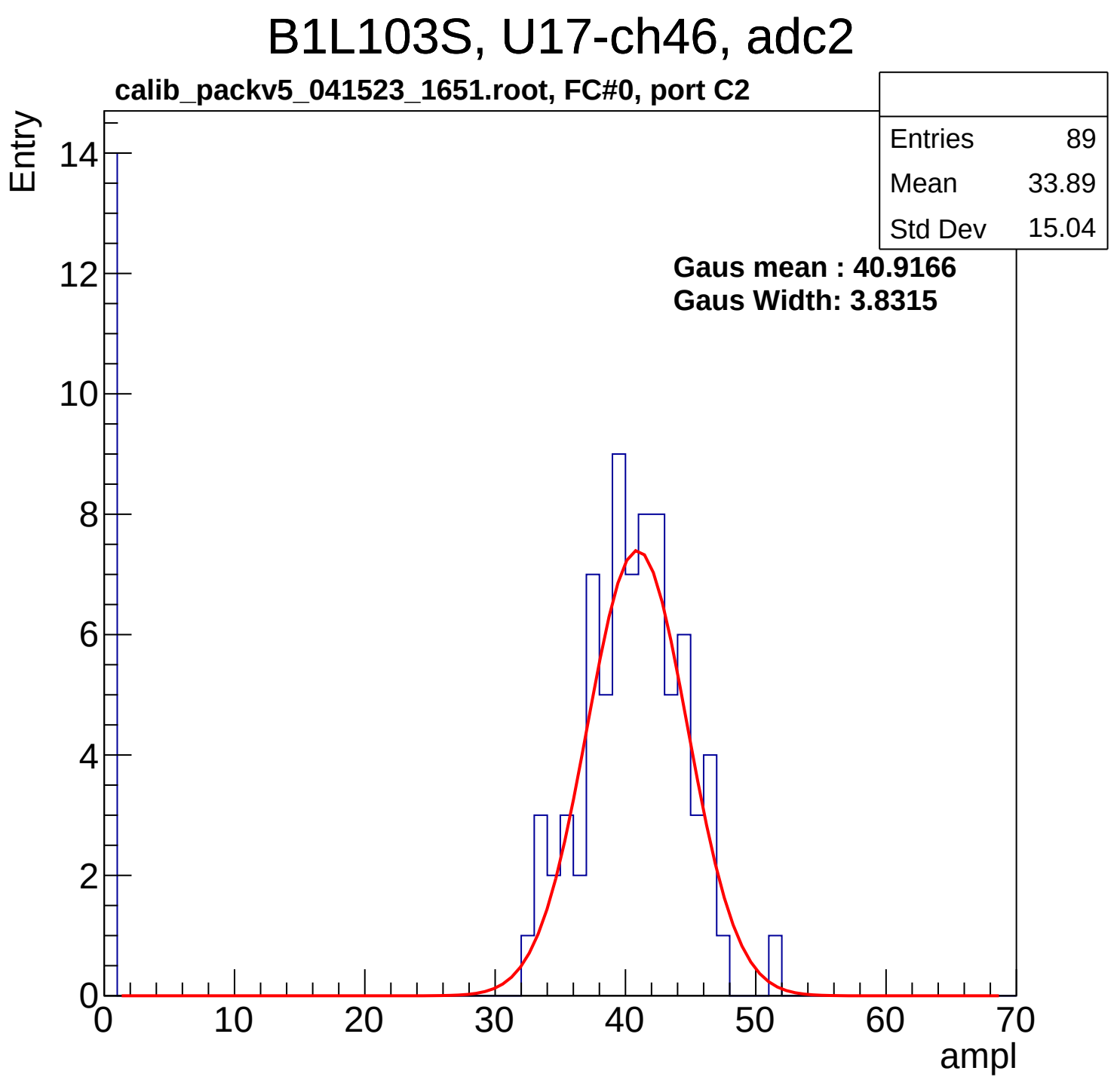

B1L103S, U17-ch45, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.37
Std Dev 8.593
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

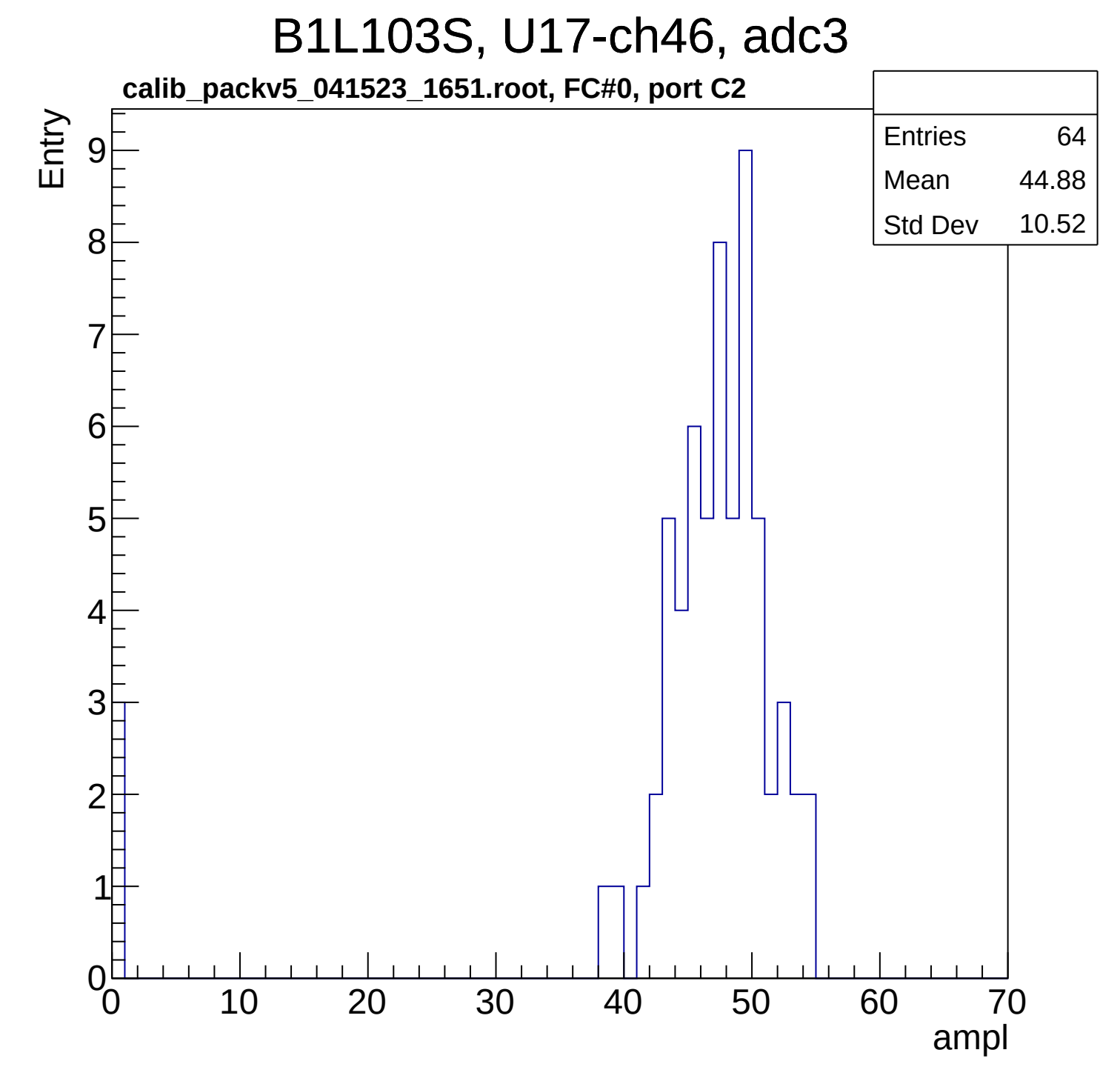

B1L103S, U17-ch45, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.9
Std Dev 1.578
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

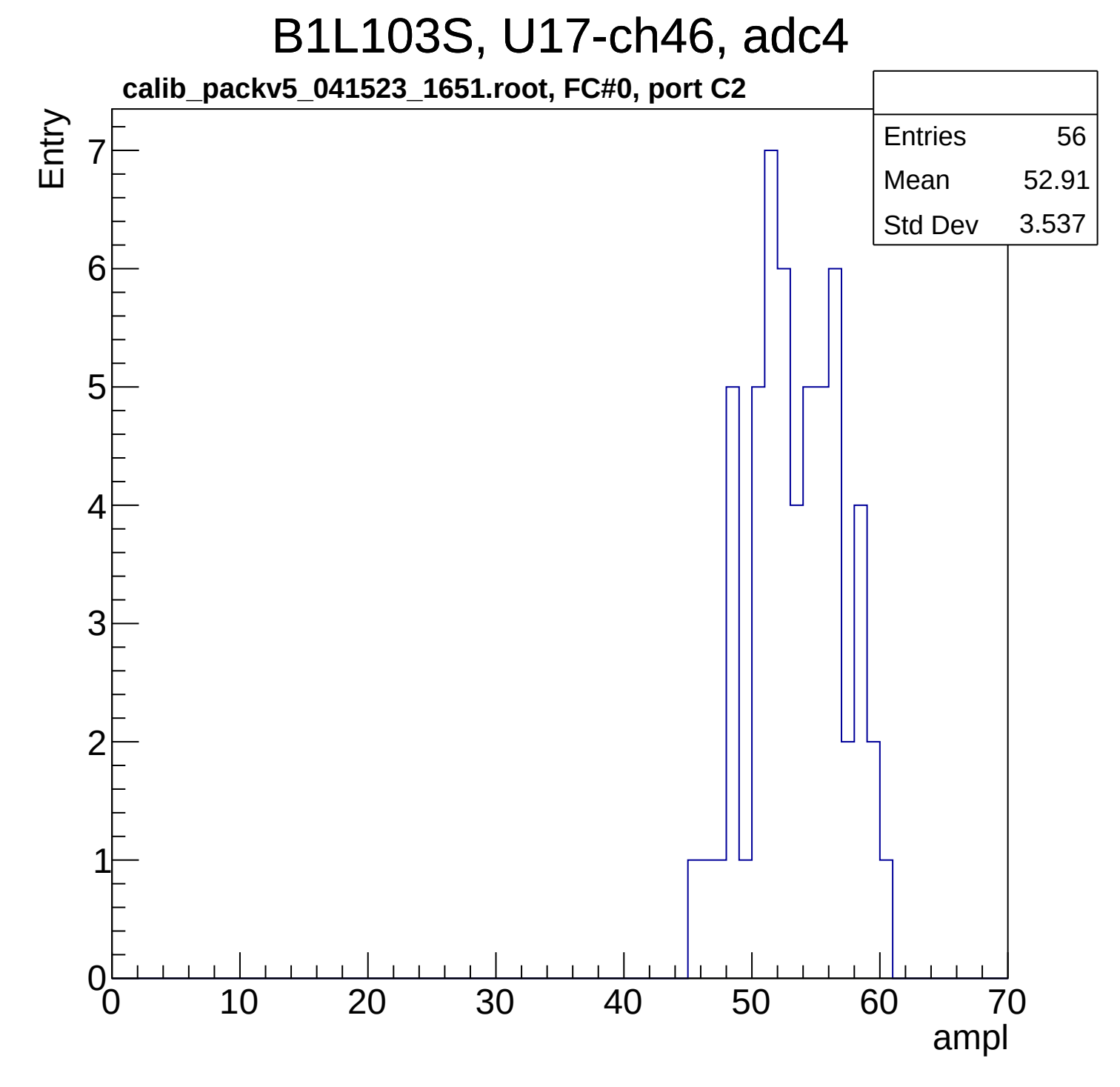

B1L103S, U17-ch45, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

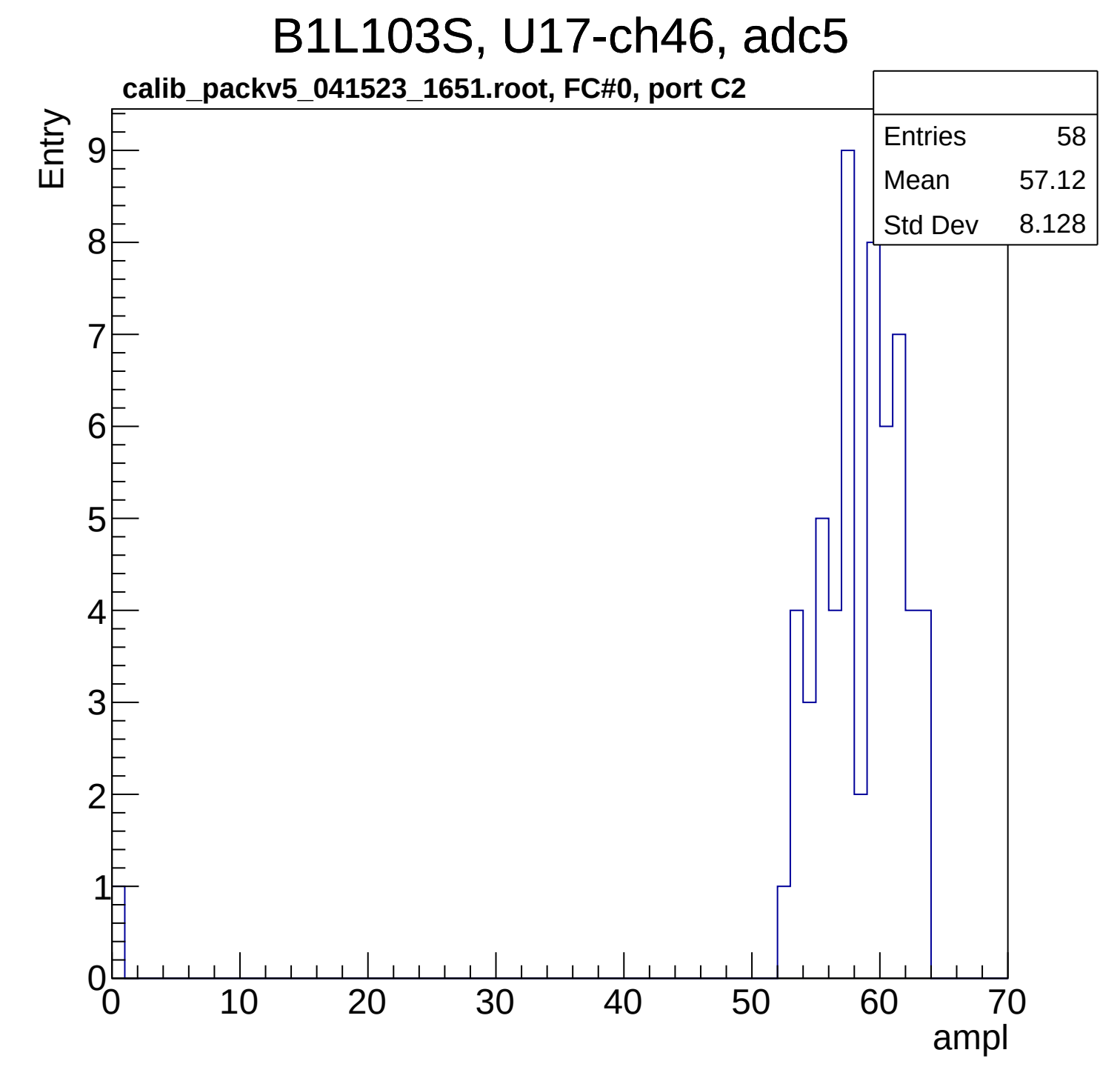

B1L103S, U17-ch46, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 18.91
Std Dev 13.02
Gaus mean : 28.7669
Gaus Width: 3.1678
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70

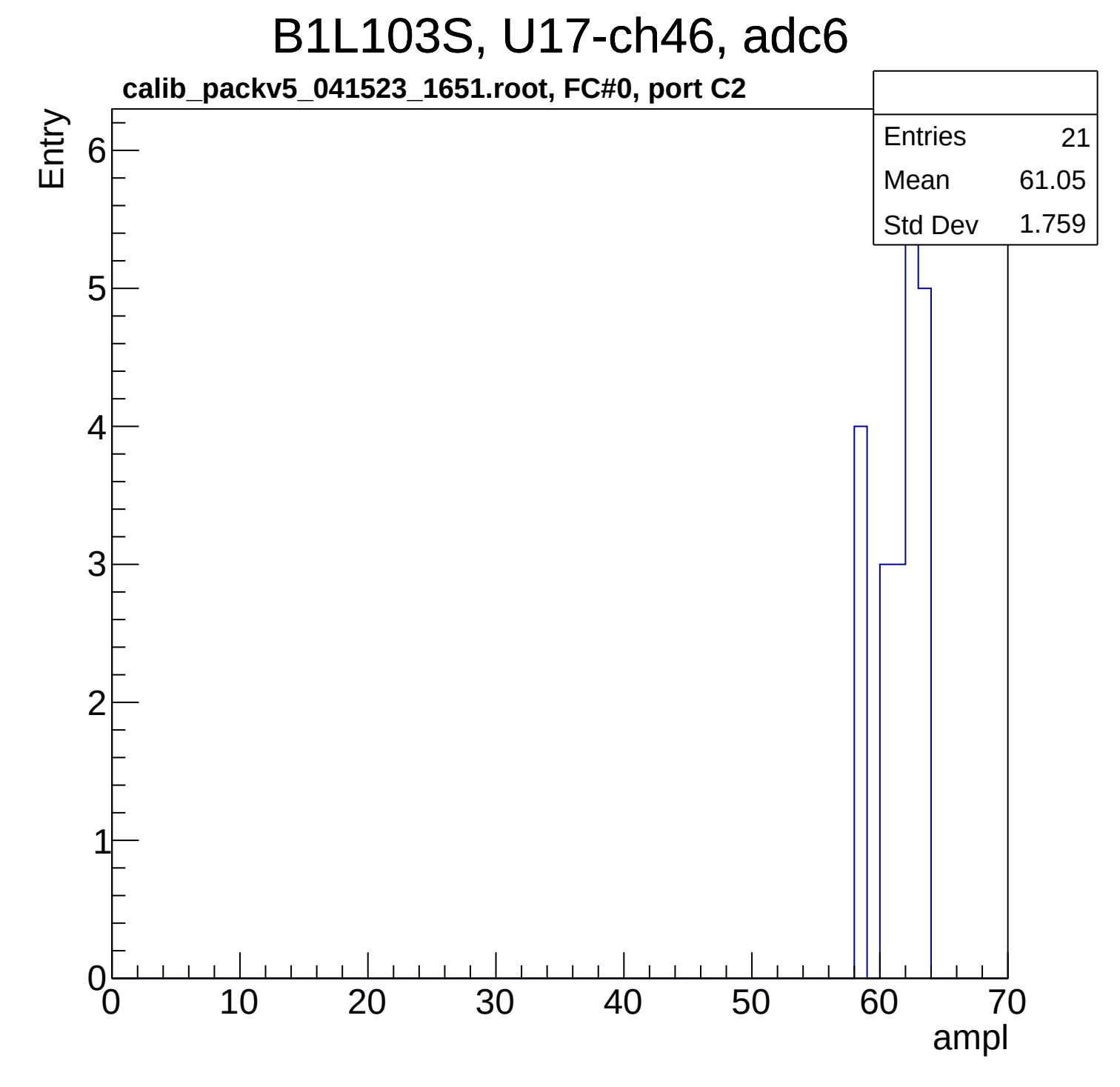

B1L103S, U17-ch46, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 32.19
Std Dev 7.99
Gaus mean : 34.7537
Gaus Width: 3.6514
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

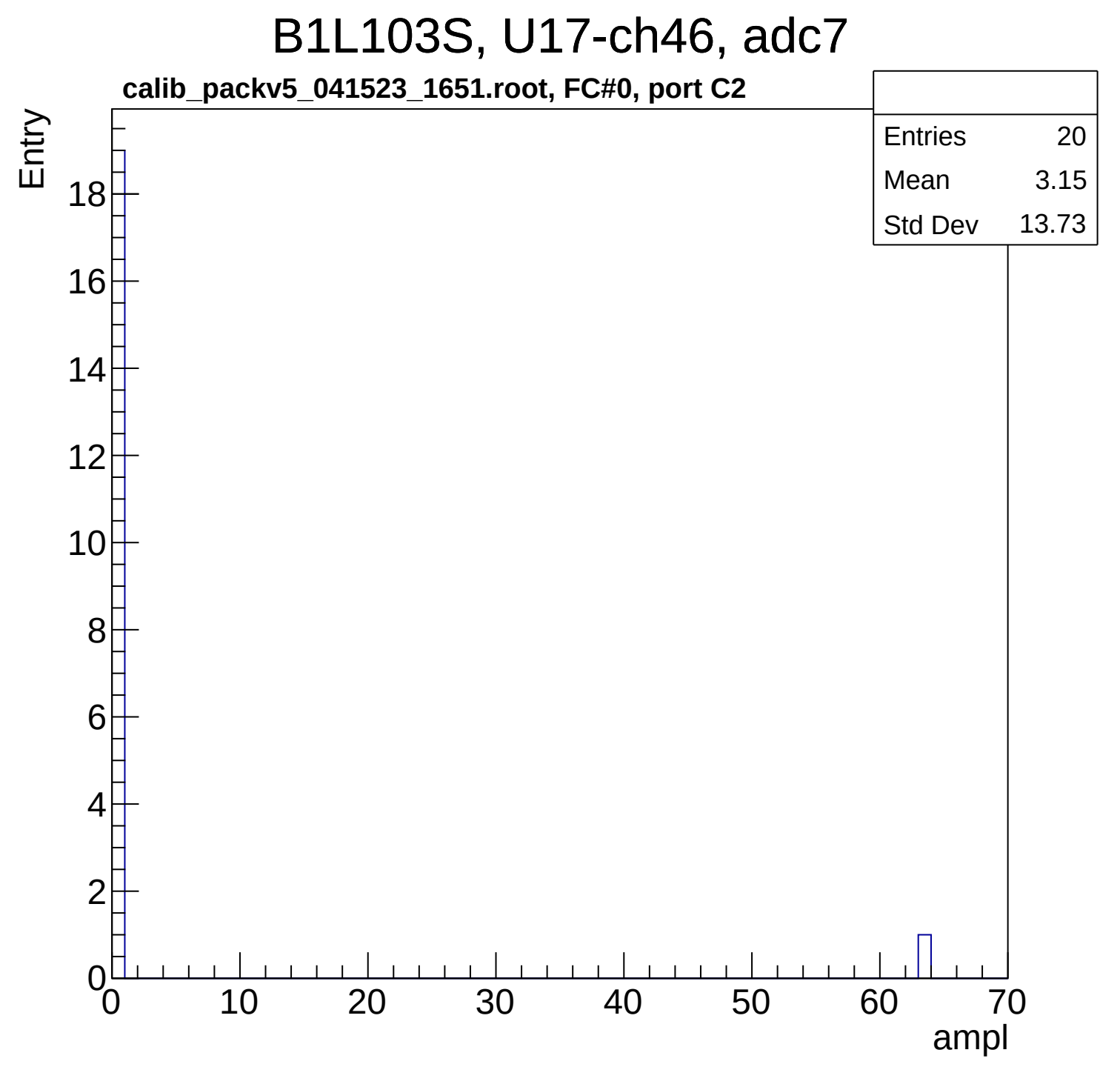

B1L103S, U17-ch46, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 33.89
Std Dev 15.04
Gaus mean : 40.9166
Gaus Width: 3.8315
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

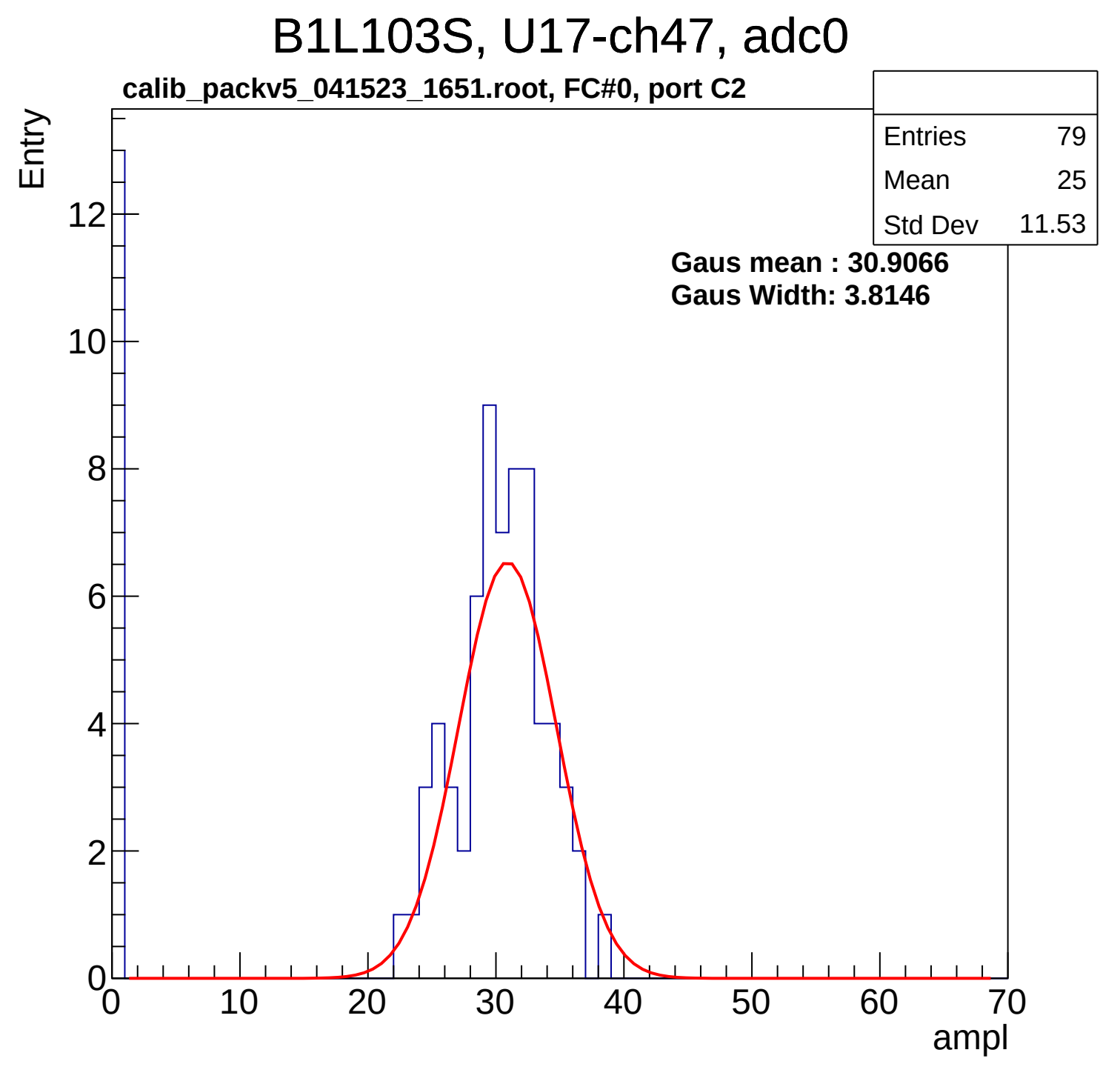

B1L103S, U17-ch46, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 44.88
Std Dev 10.52
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

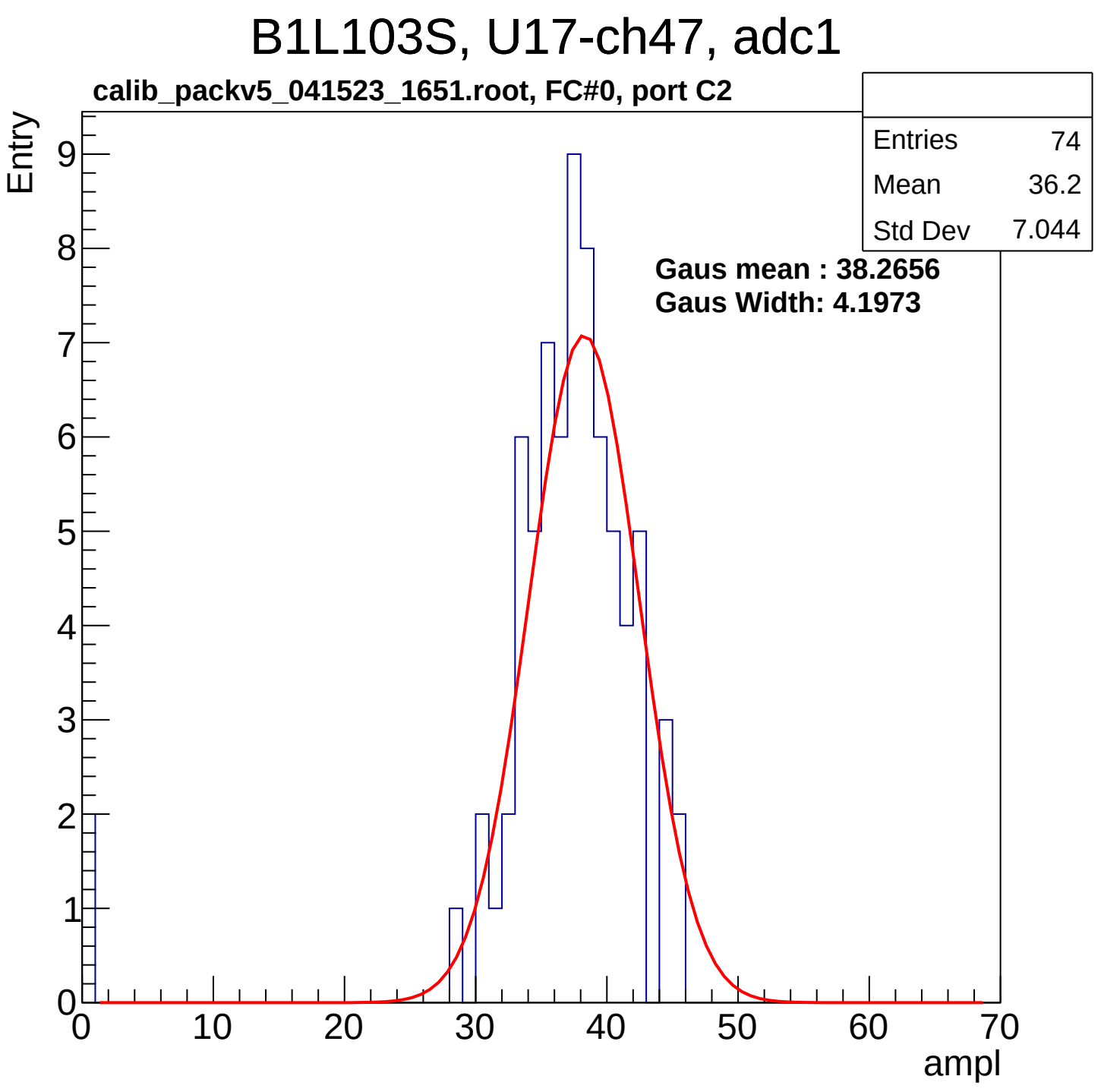

B1L103S, U17-ch46, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 52.91
Std Dev 3.537
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

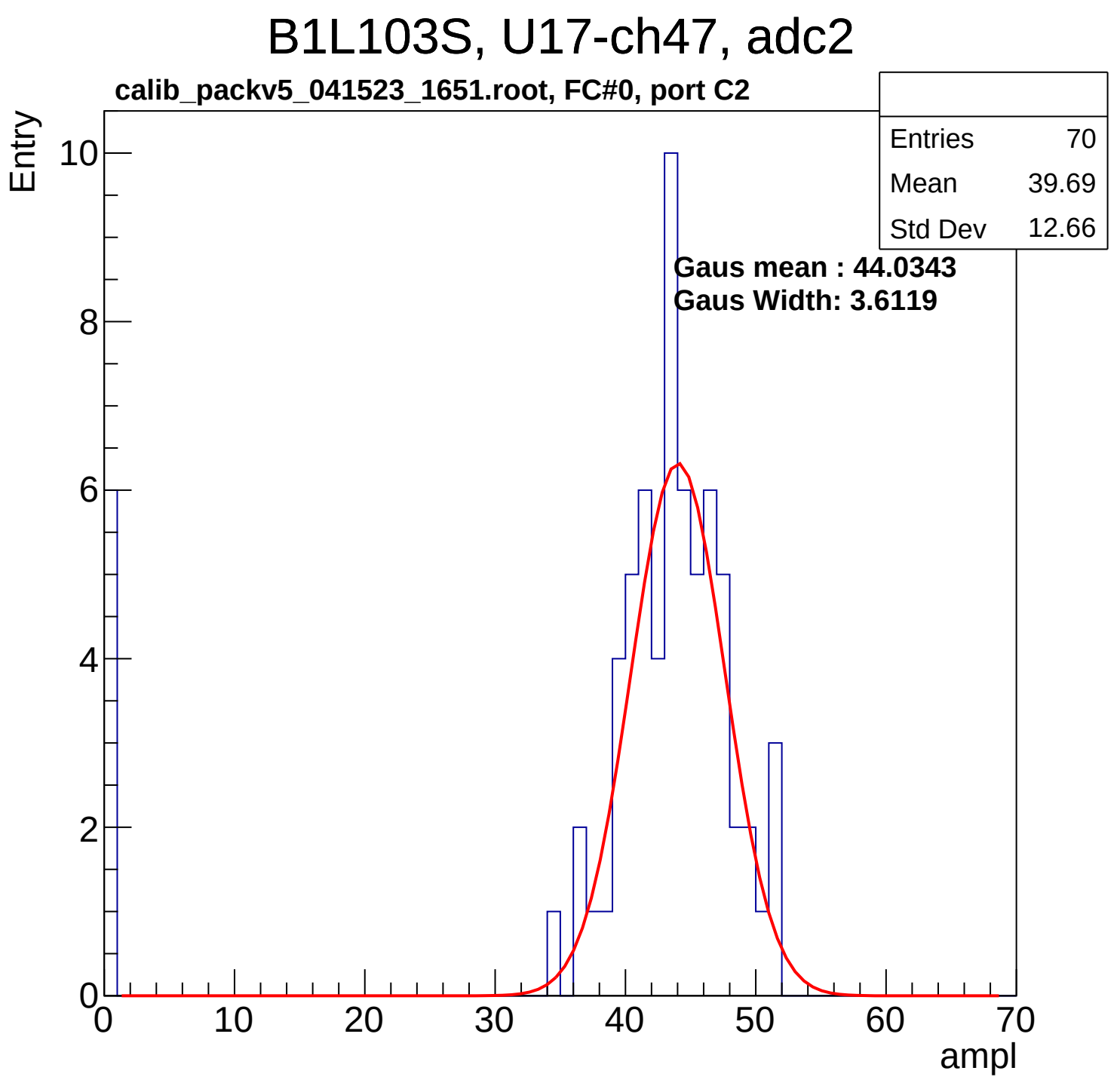

B1L103S, U17-ch46, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 57.12
Std Dev 8.128
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

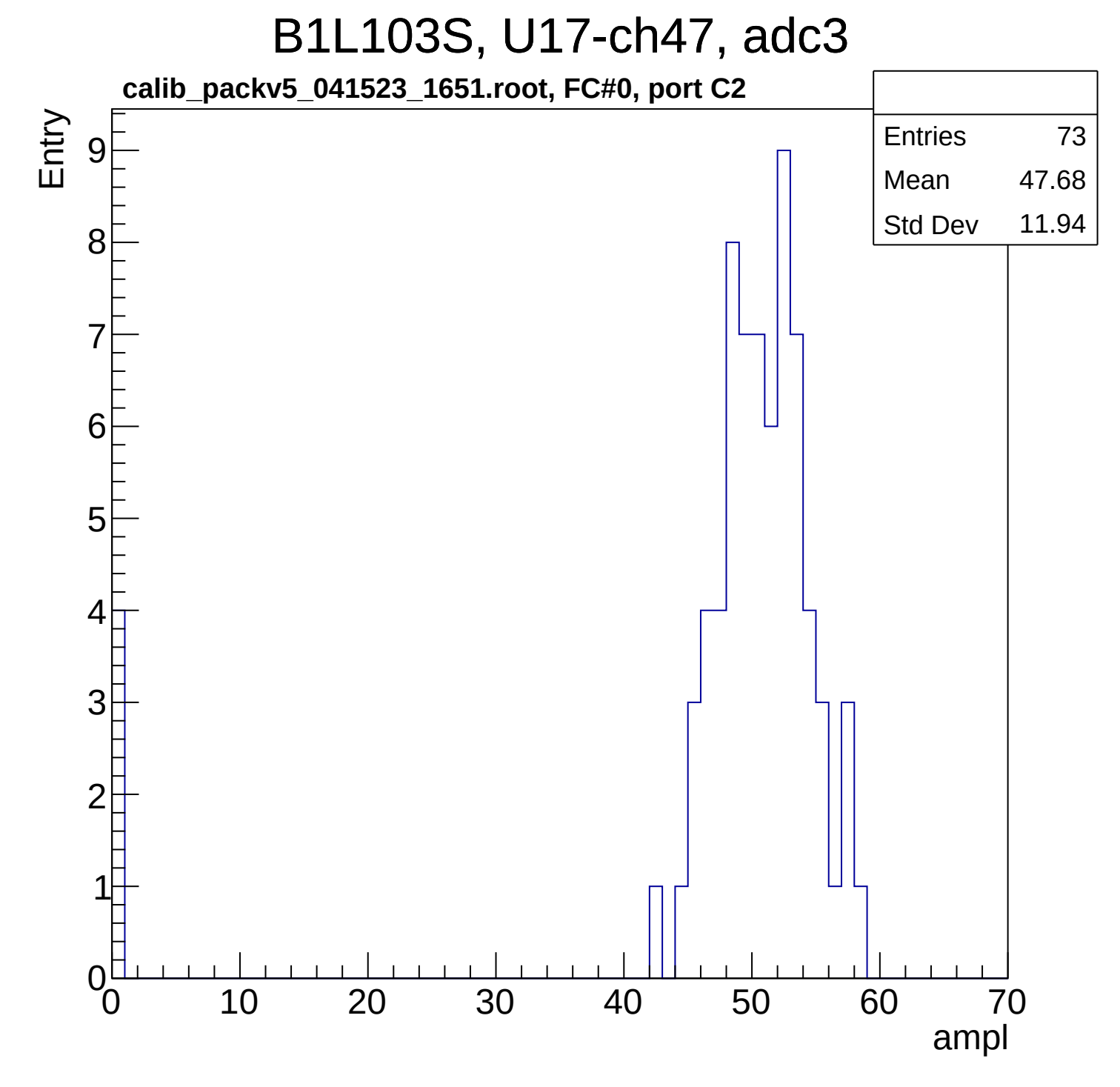

B1L103S, U17-ch46, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 61.05
Std Dev 1.759
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

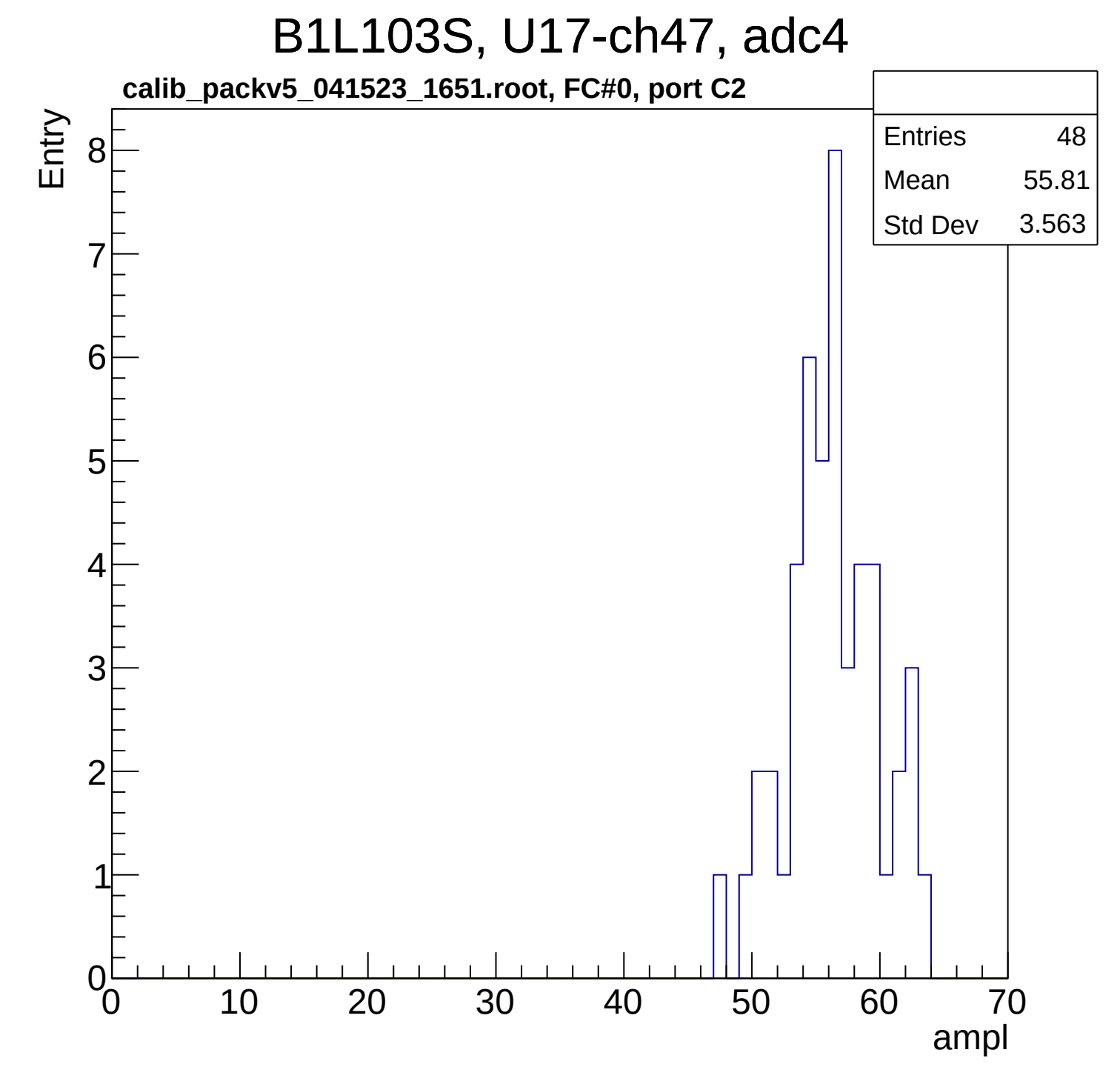

B1L103S, U17-ch46, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

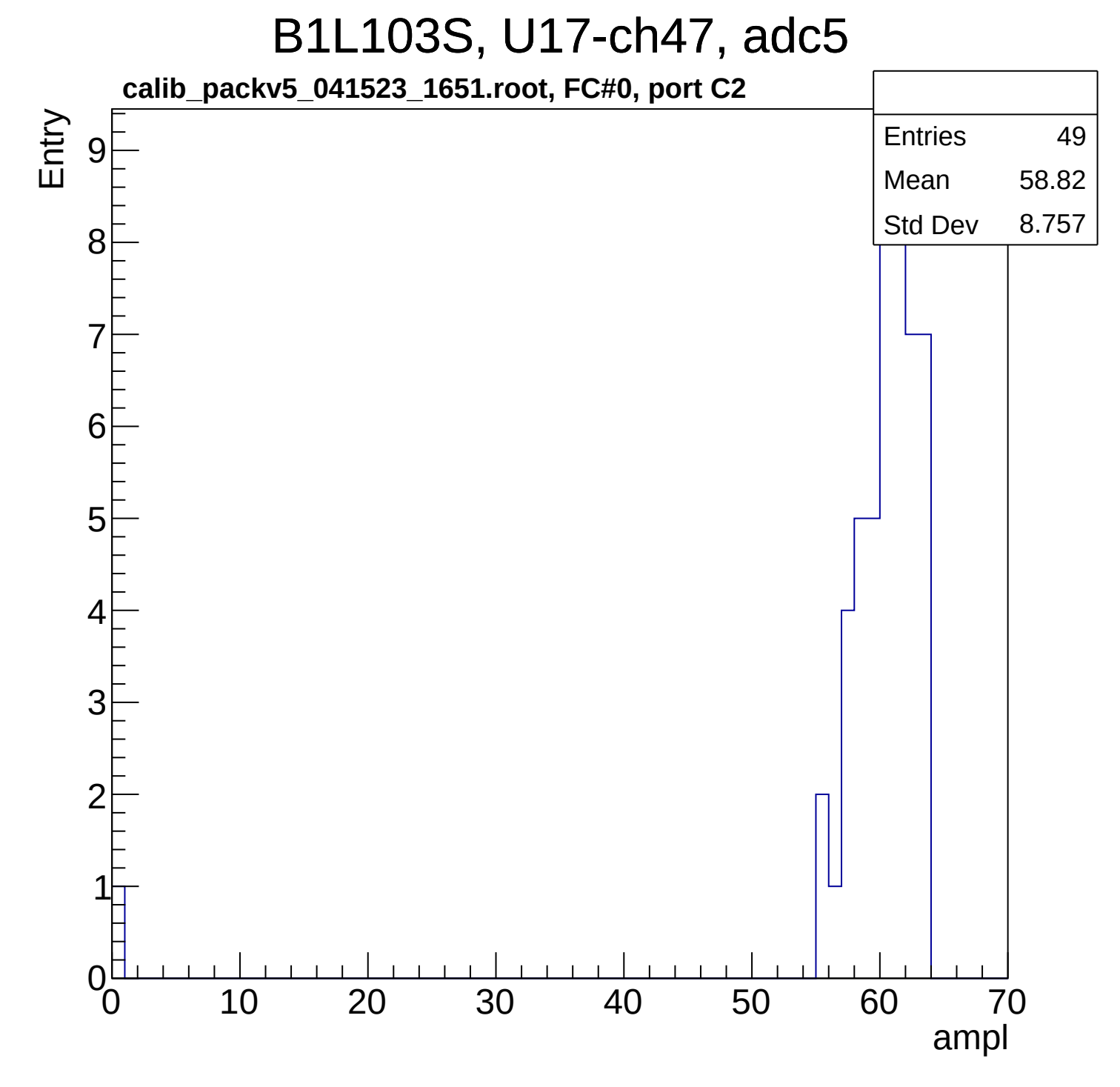

B1L103S, U17-ch47, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 25
Std Dev 11.53
Gaus mean : 30.9066
Gaus Width: 3.8146
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

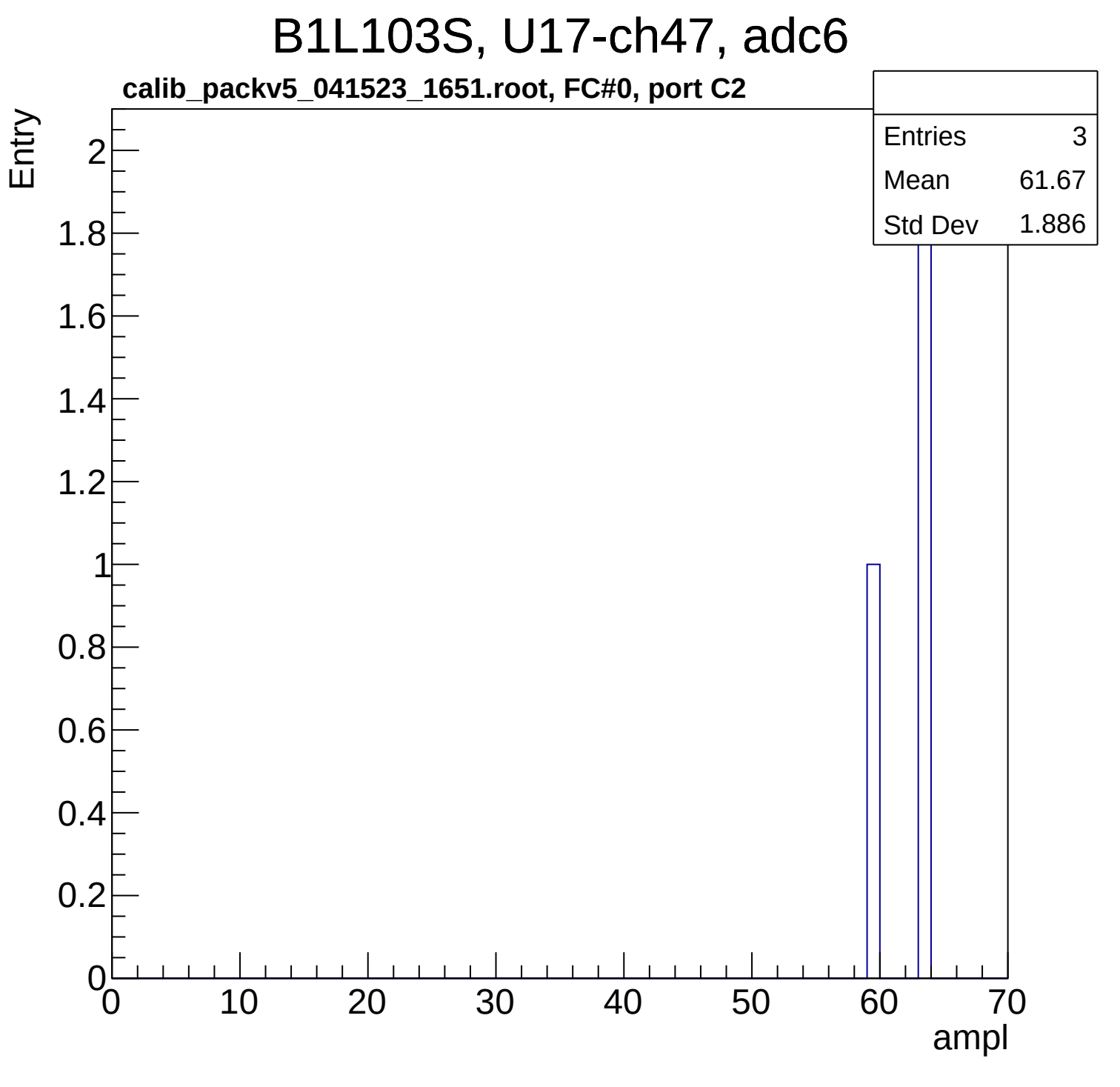

B1L103S, U17-ch47, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 36.2
Std Dev 7.044
Gaus mean : 38.2656
Gaus Width: 4.1973
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

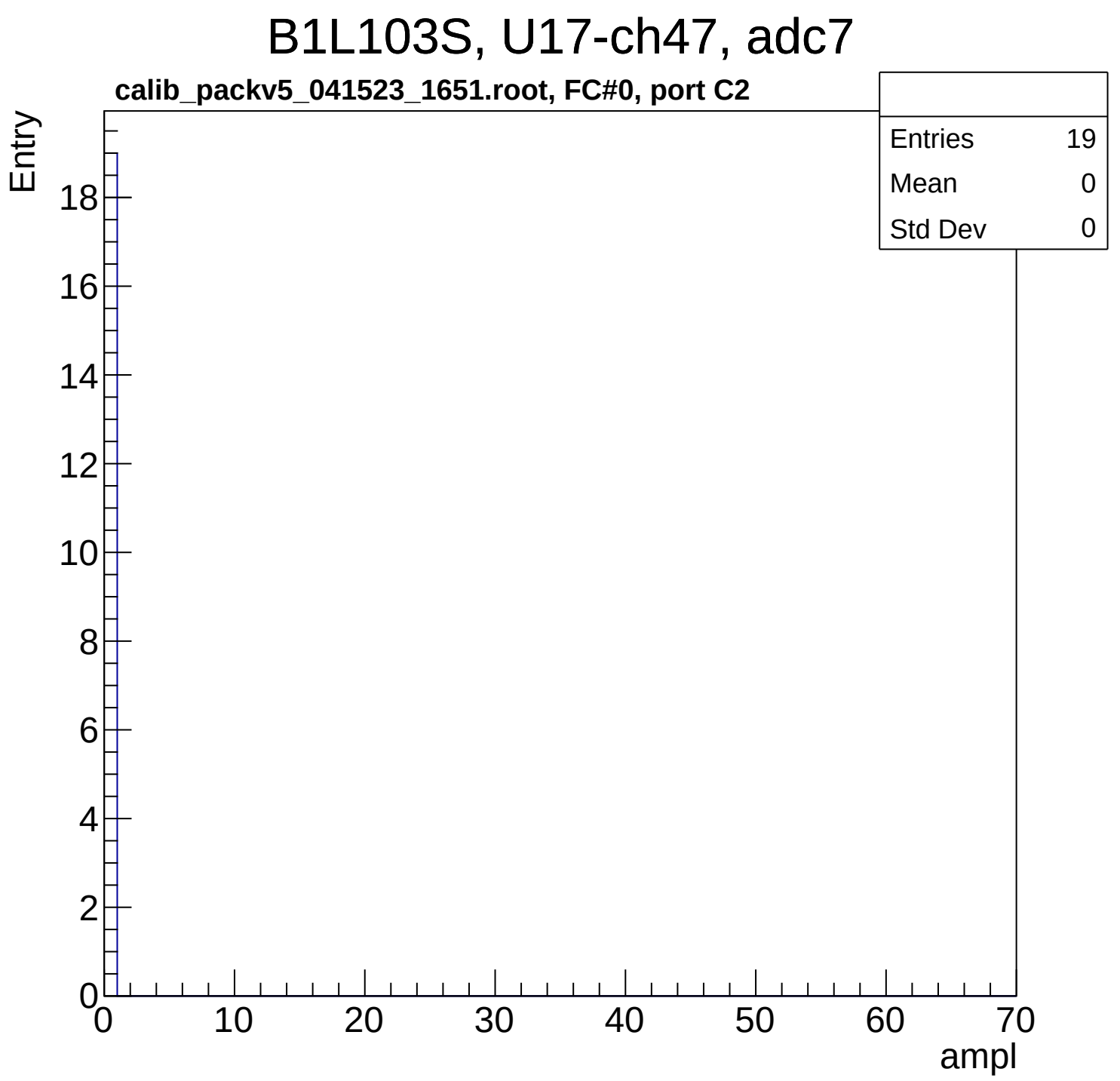

B1L103S, U17-ch47, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 39.69
Std Dev 12.66
Gaus mean : 44.0343
Gaus Width: 3.6119
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

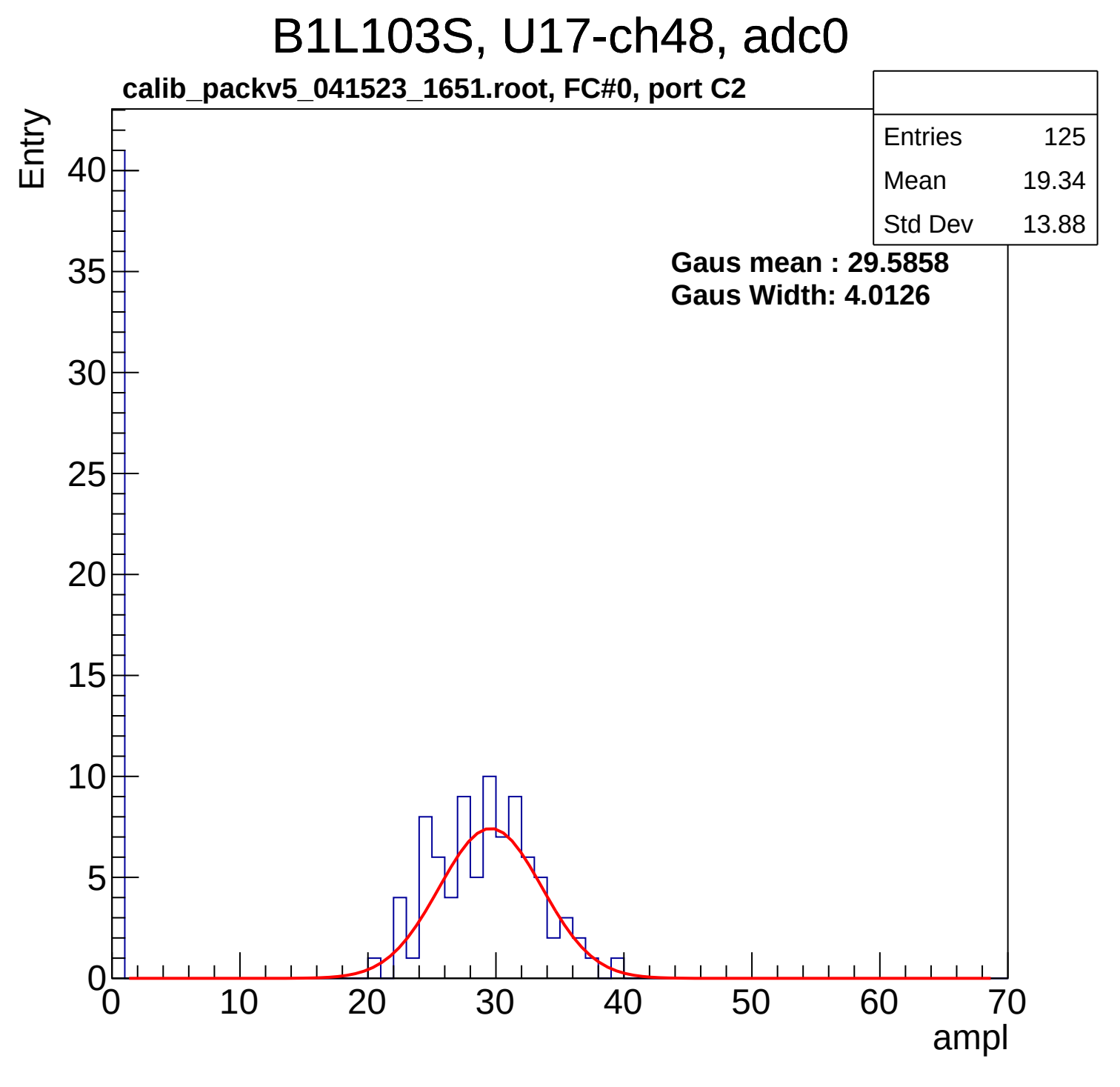

B1L103S, U17-ch47, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 47.68
Std Dev 11.94
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

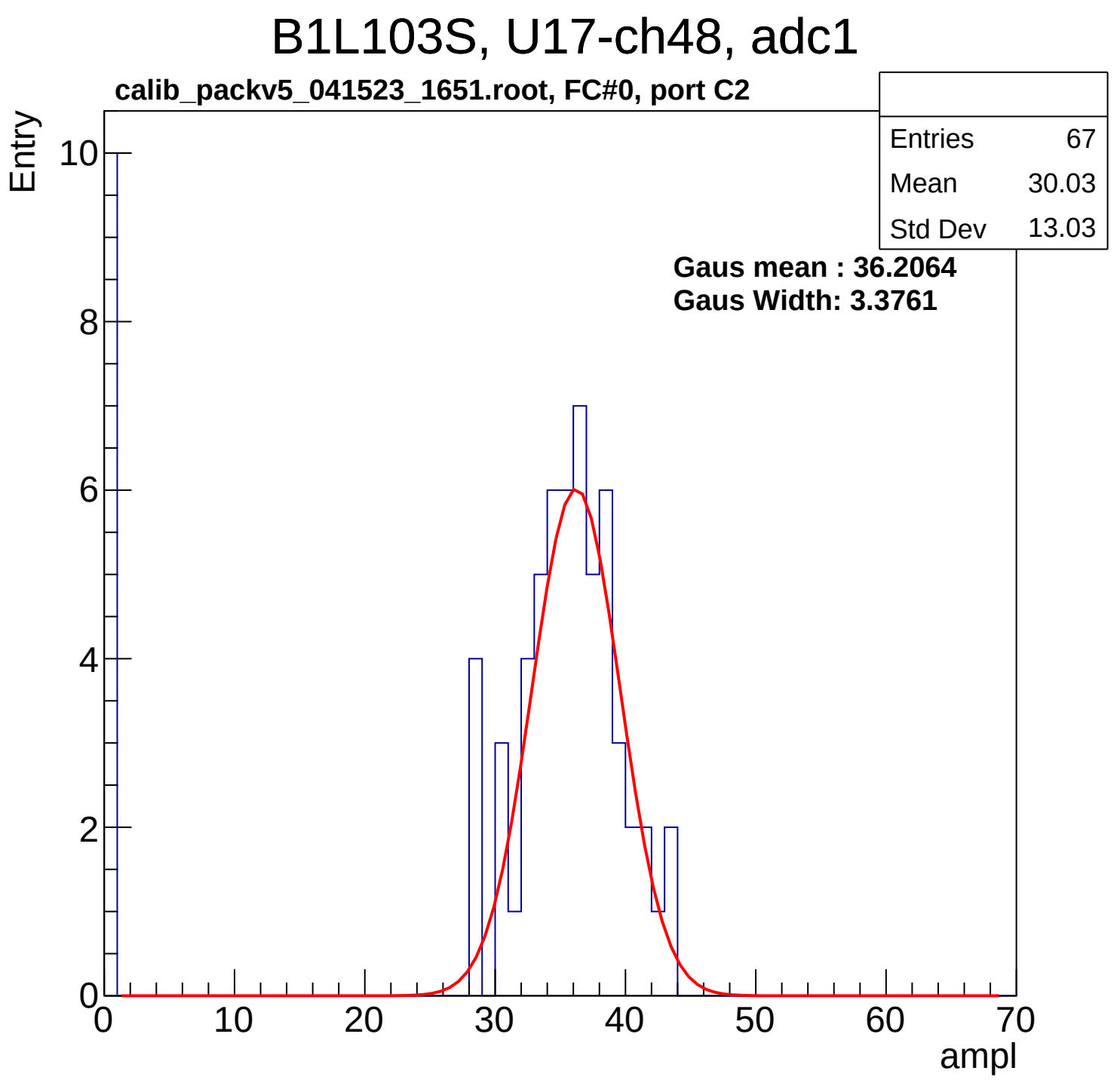

B1L103S, U17-ch47, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 55.81
Std Dev 3.563
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

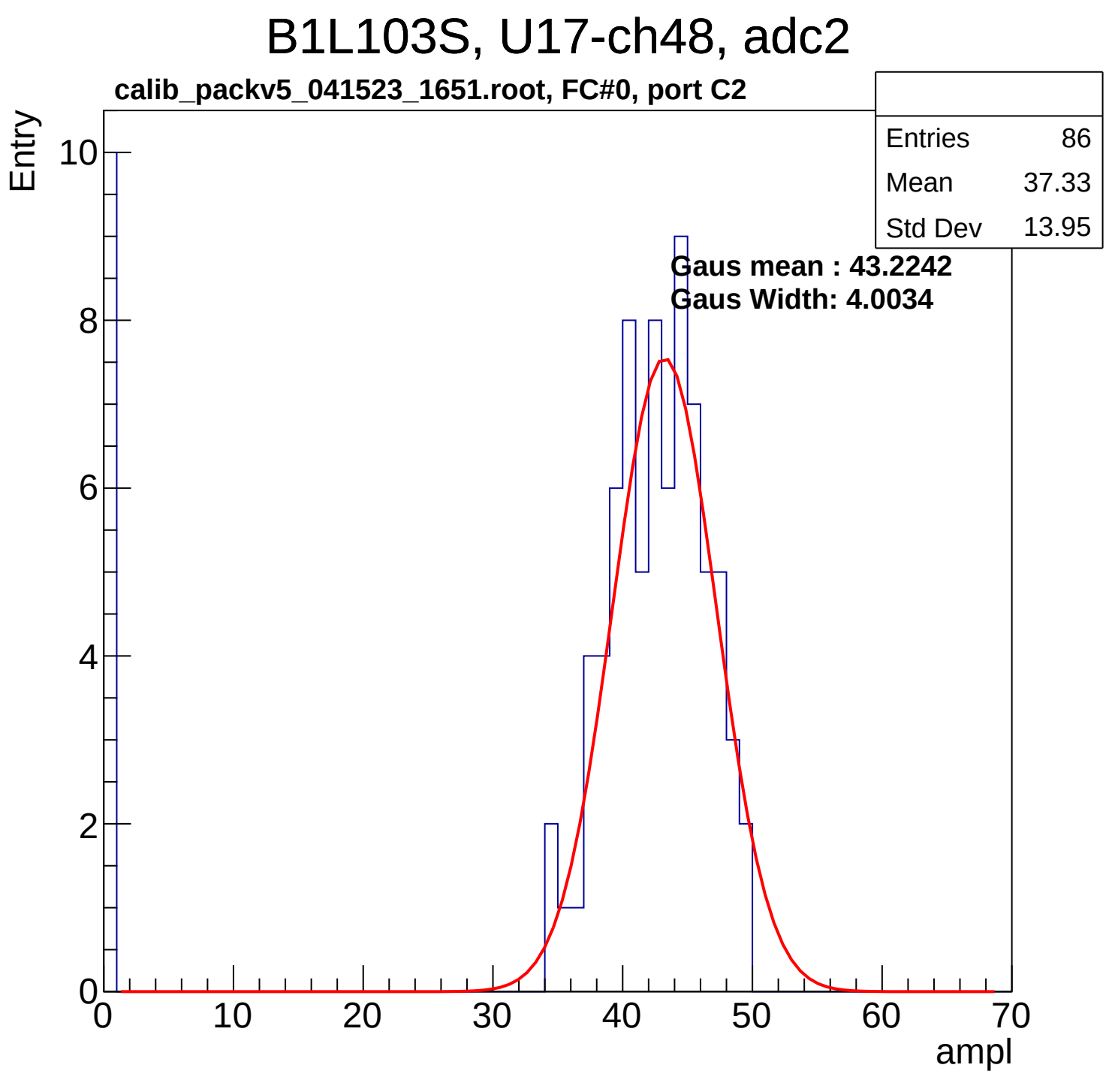

B1L103S, U17-ch47, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.82
Std Dev 8.757
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

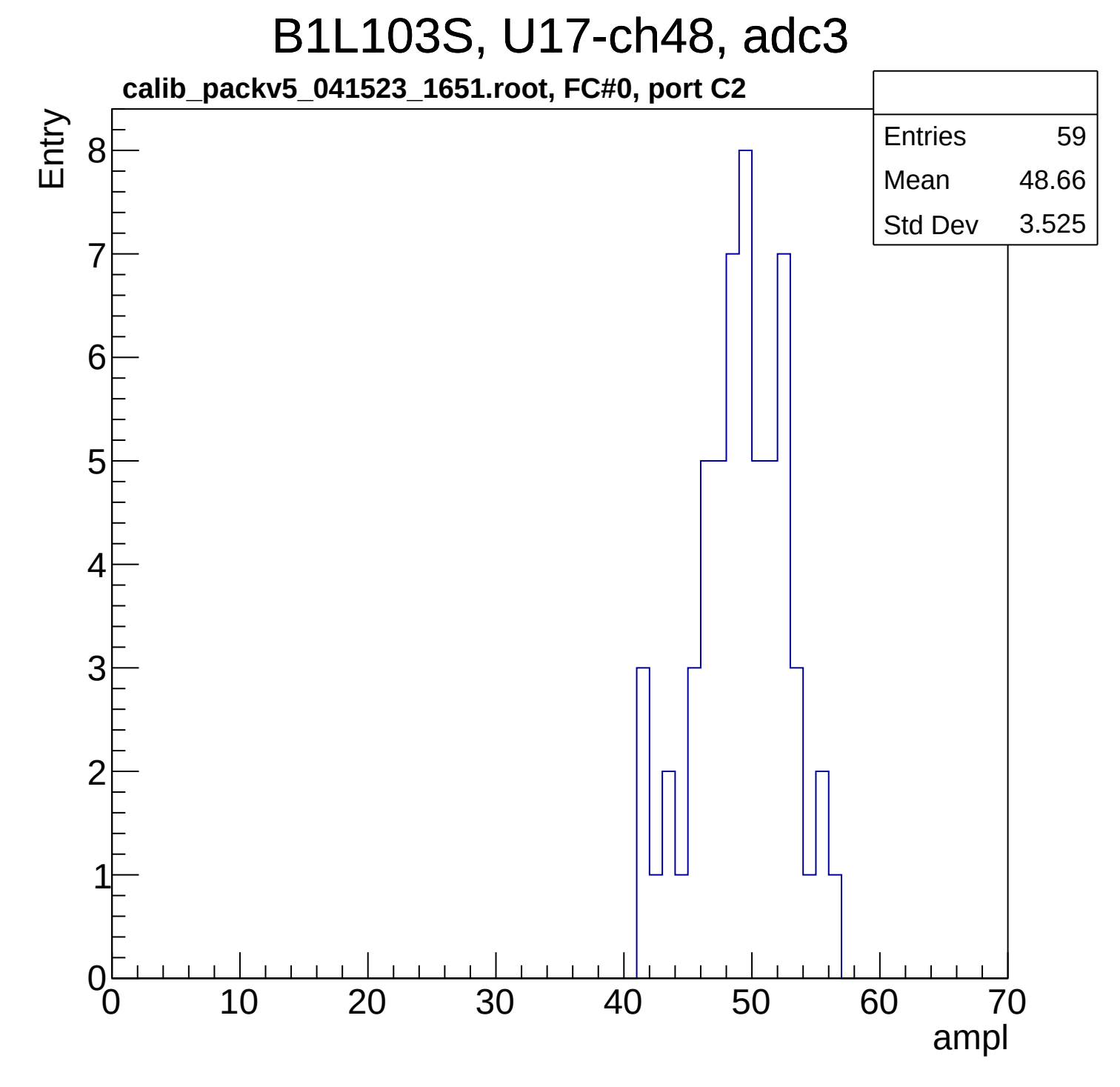

B1L103S, U17-ch47, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 61.67
Std Dev 1.886
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

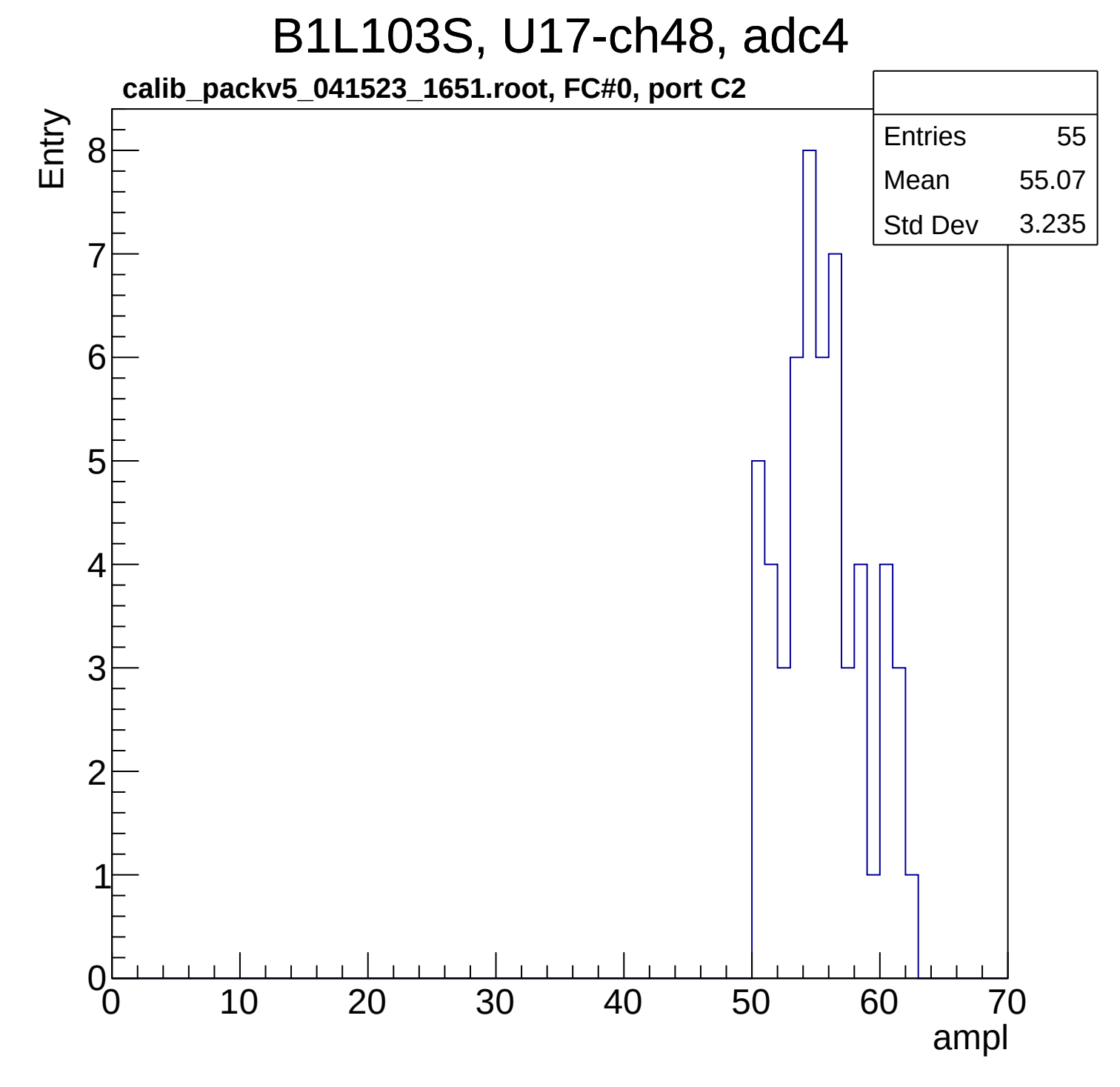

B1L103S, U17-ch47, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

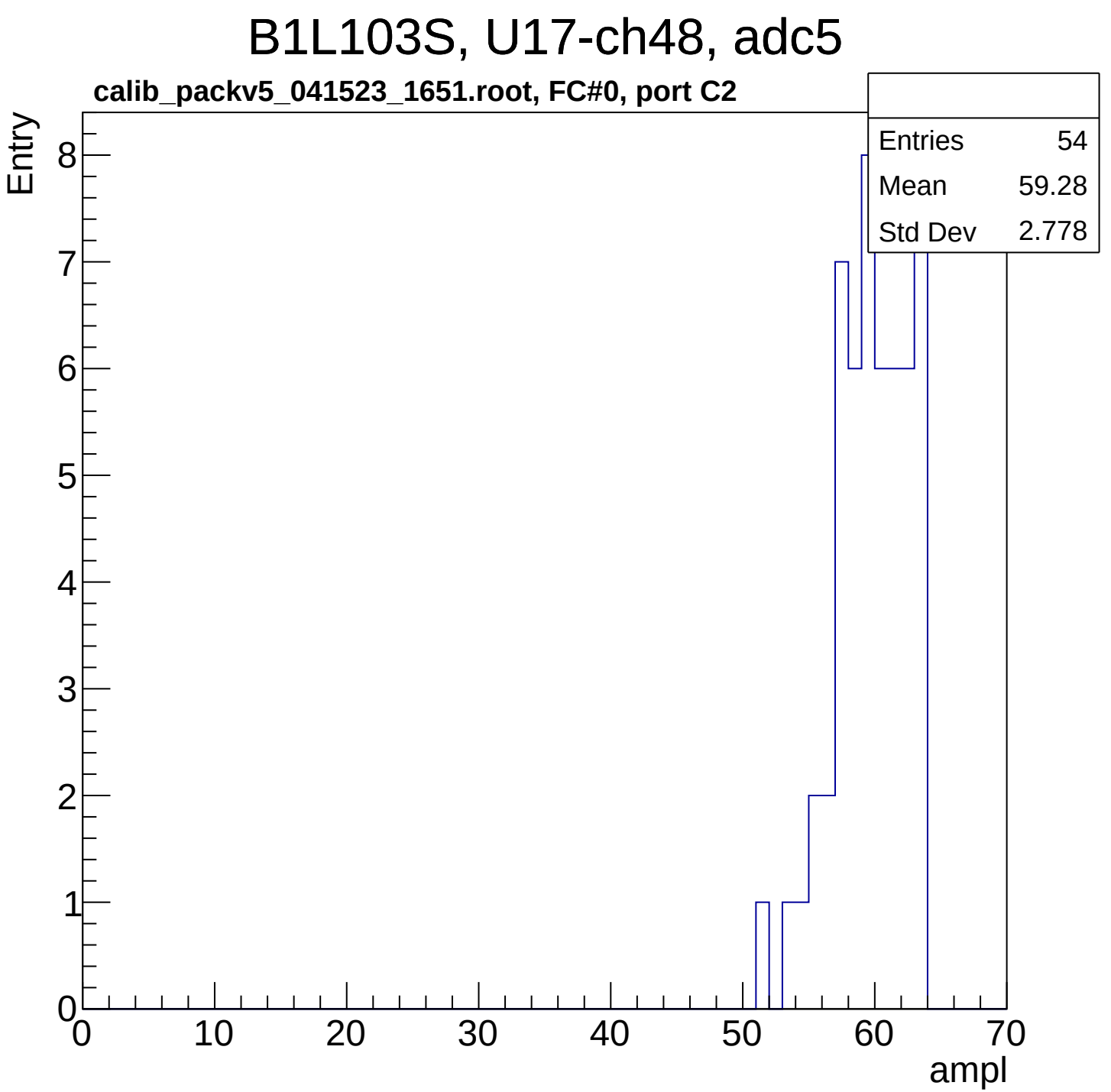

B1L103S, U17-ch48, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 125
Mean 19.34
Std Dev 13.88
Gaus mean : 29.5858
Gaus Width: 4.0126
Entry
ampl
0
5
10
15
20
25
30
35
40
0
10
20
30
40
50
60
70

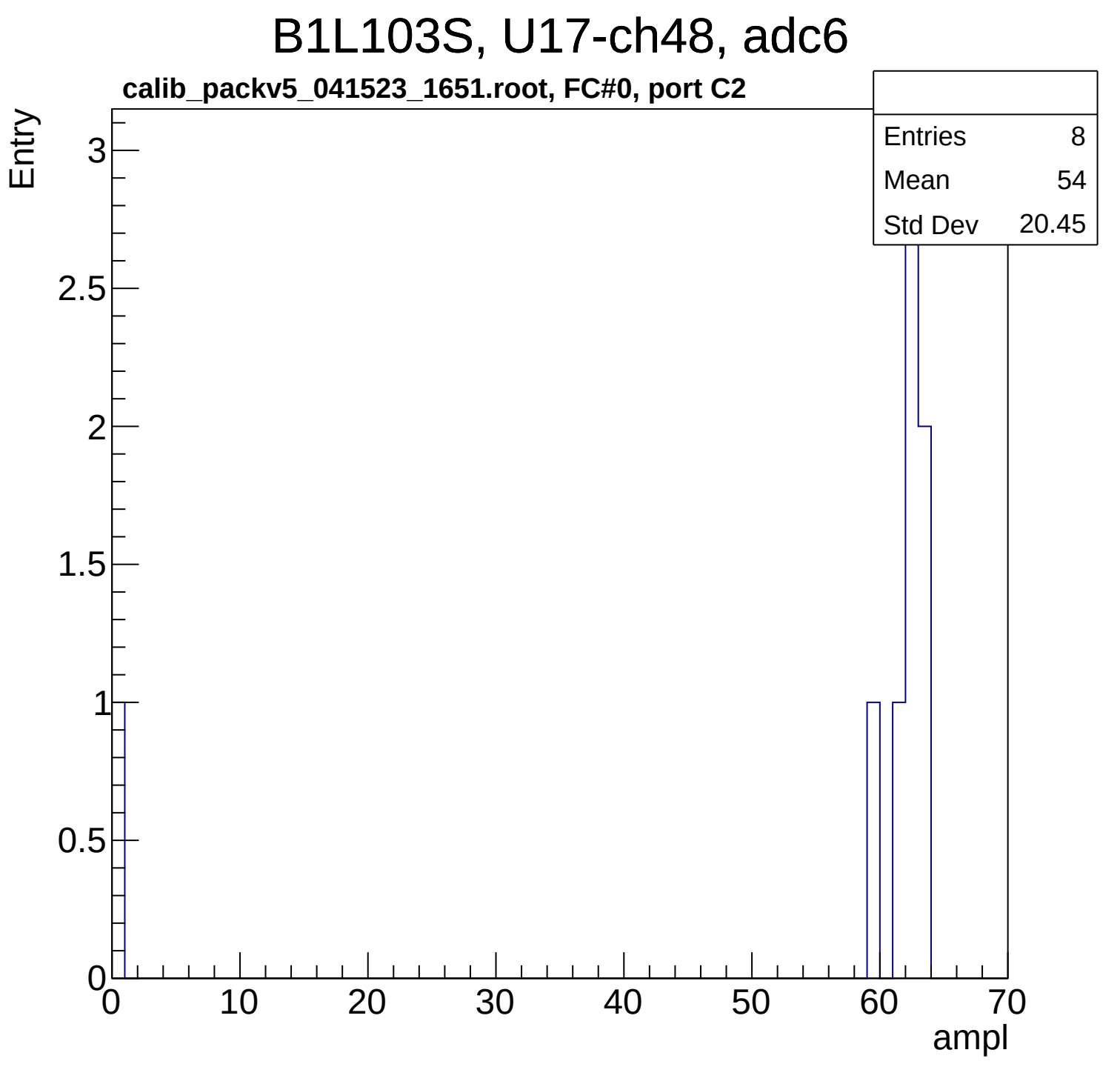

B1L103S, U17-ch48, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 30.03
Std Dev 13.03
Gaus mean : 36.2064
Gaus Width: 3.3761
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

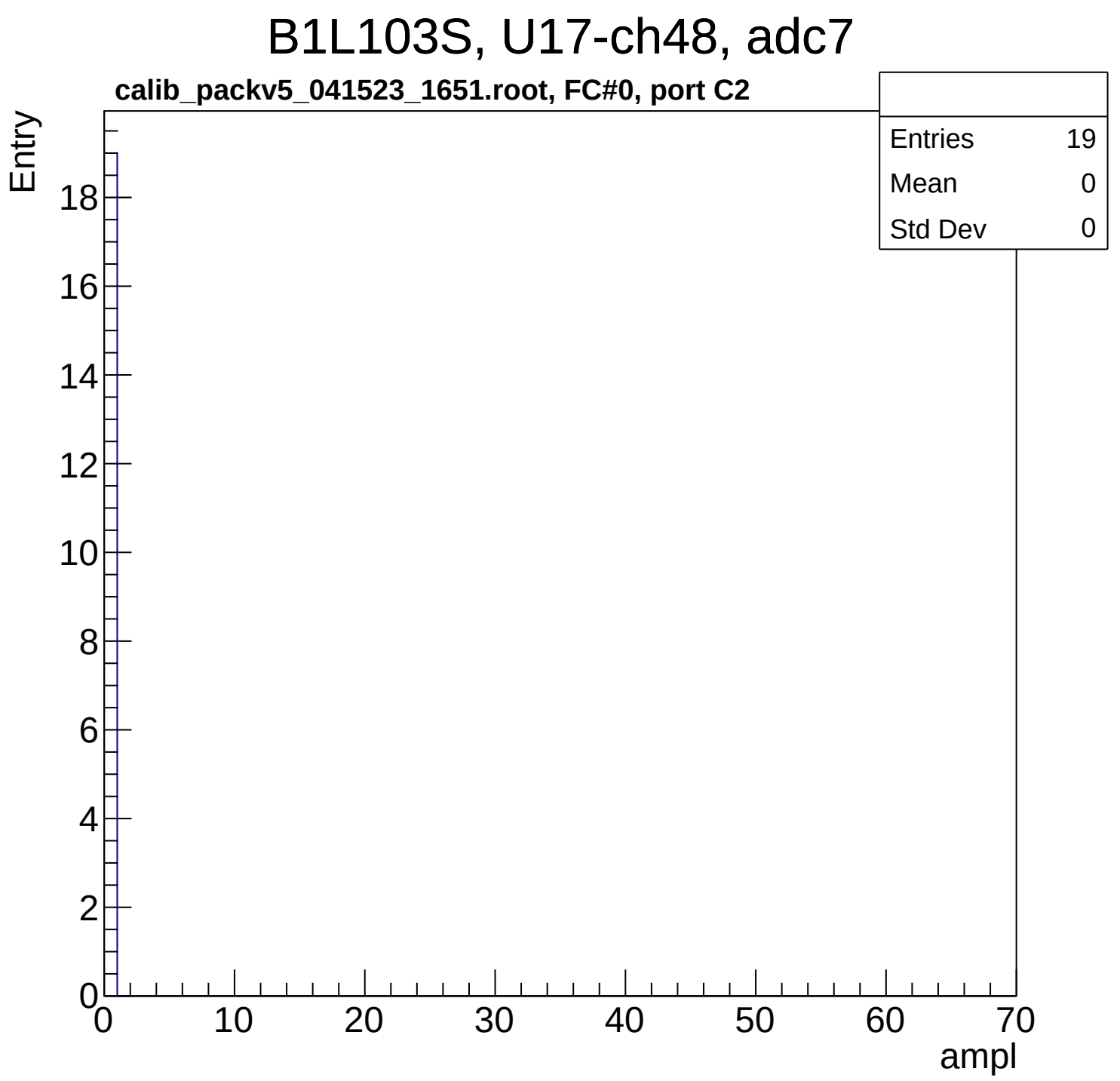

B1L103S, U17-ch48, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 37.33
Std Dev 13.95
Gaus mean : 43.2242
Gaus Width: 4.0034
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

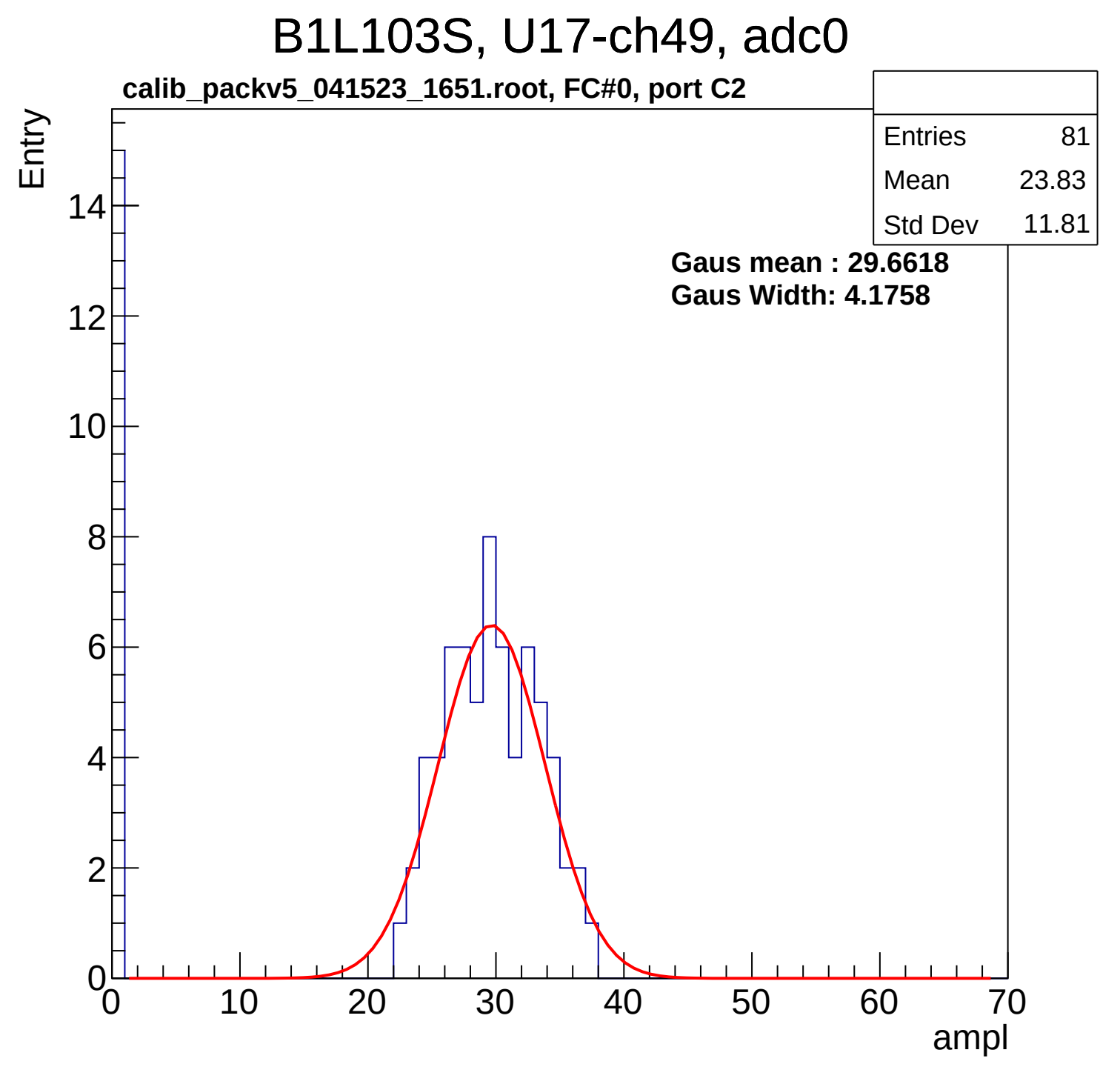

B1L103S, U17-ch48, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 48.66
Std Dev 3.525
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

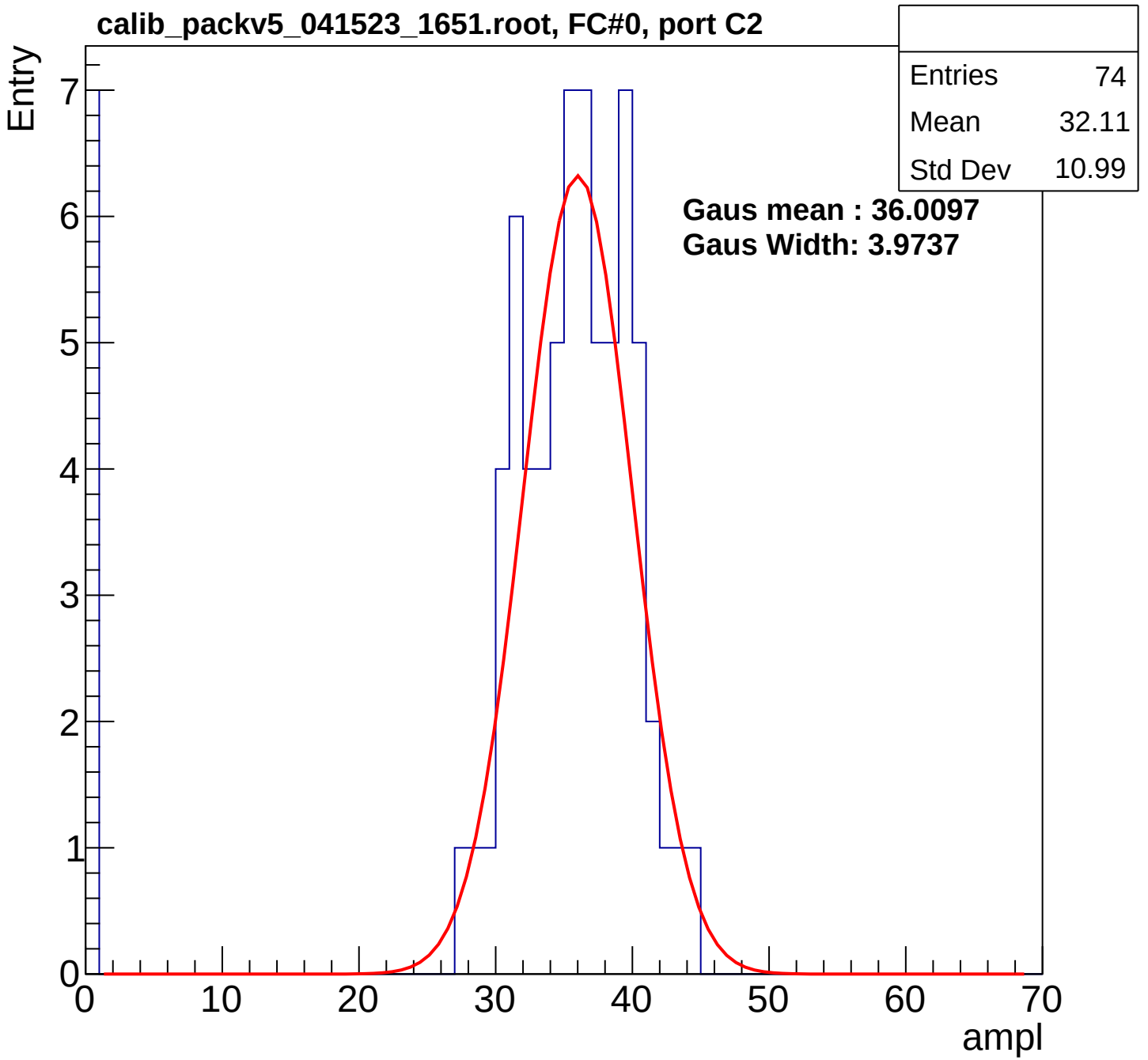

B1L103S, U17-ch48, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 55.07
Std Dev 3.235
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

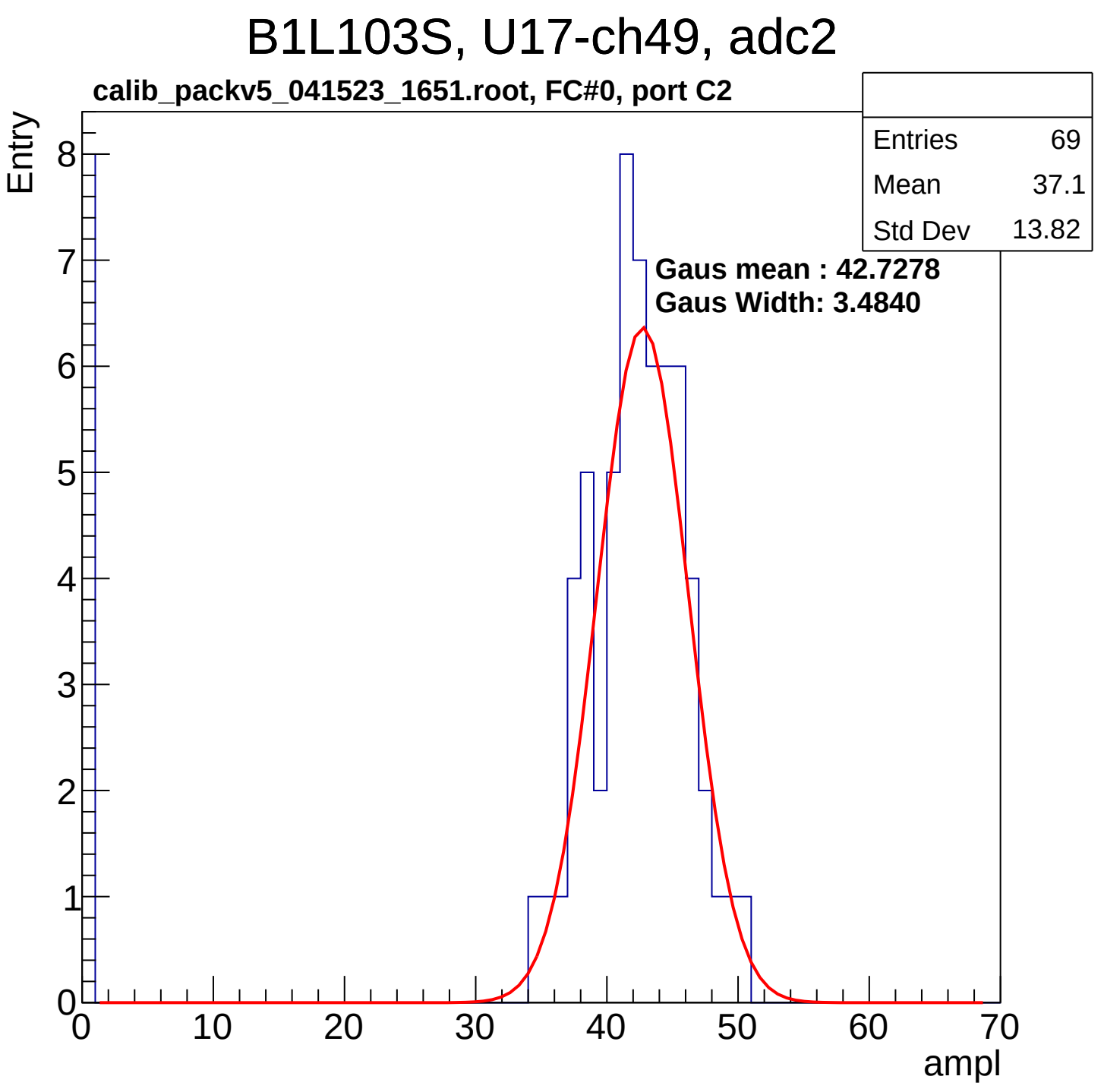

B1L103S, U17-ch48, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 59.28
Std Dev 2.778
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

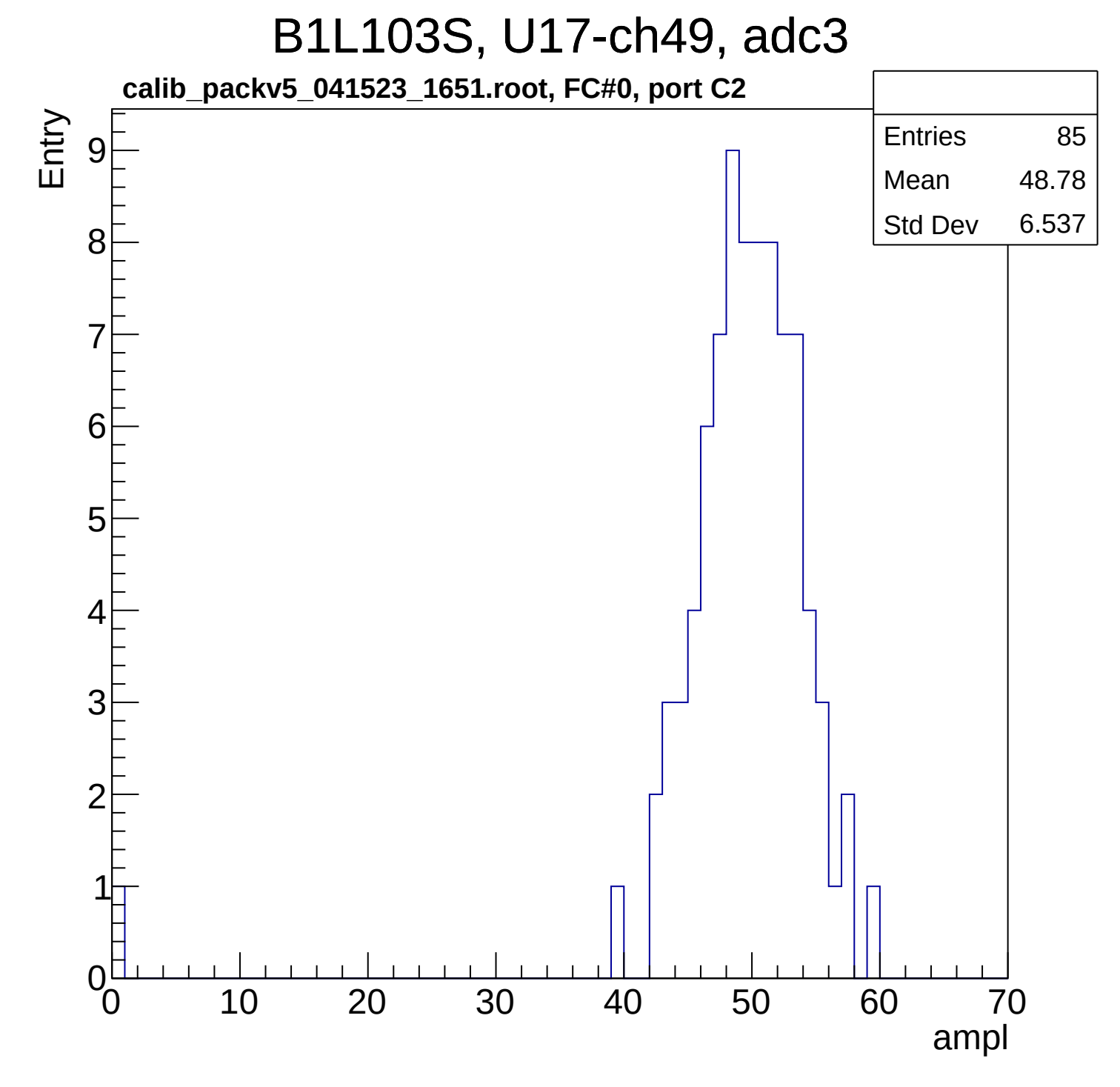

B1L103S, U17-ch48, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 54
Std Dev 20.45
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

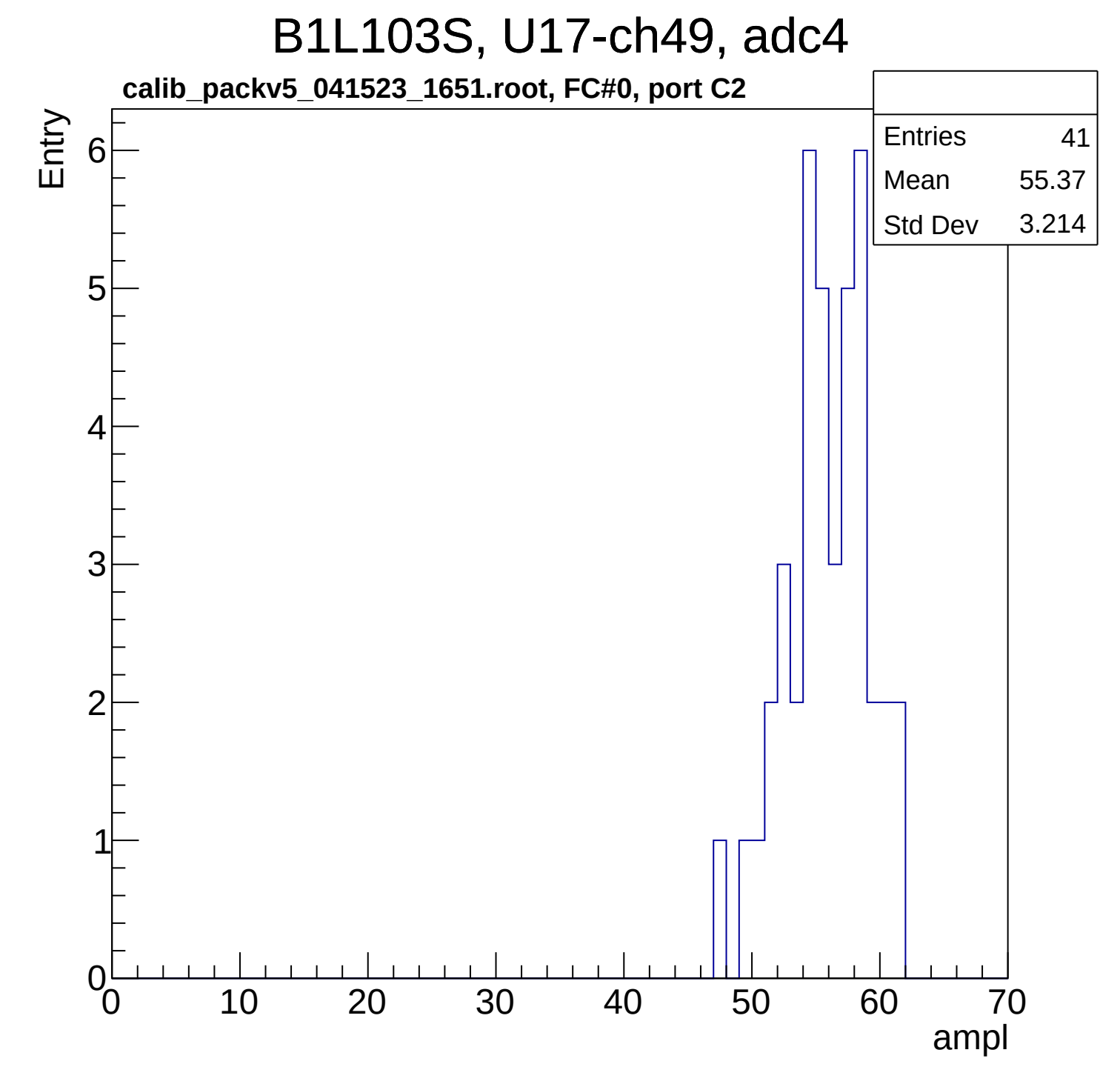

B1L103S, U17-ch48, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

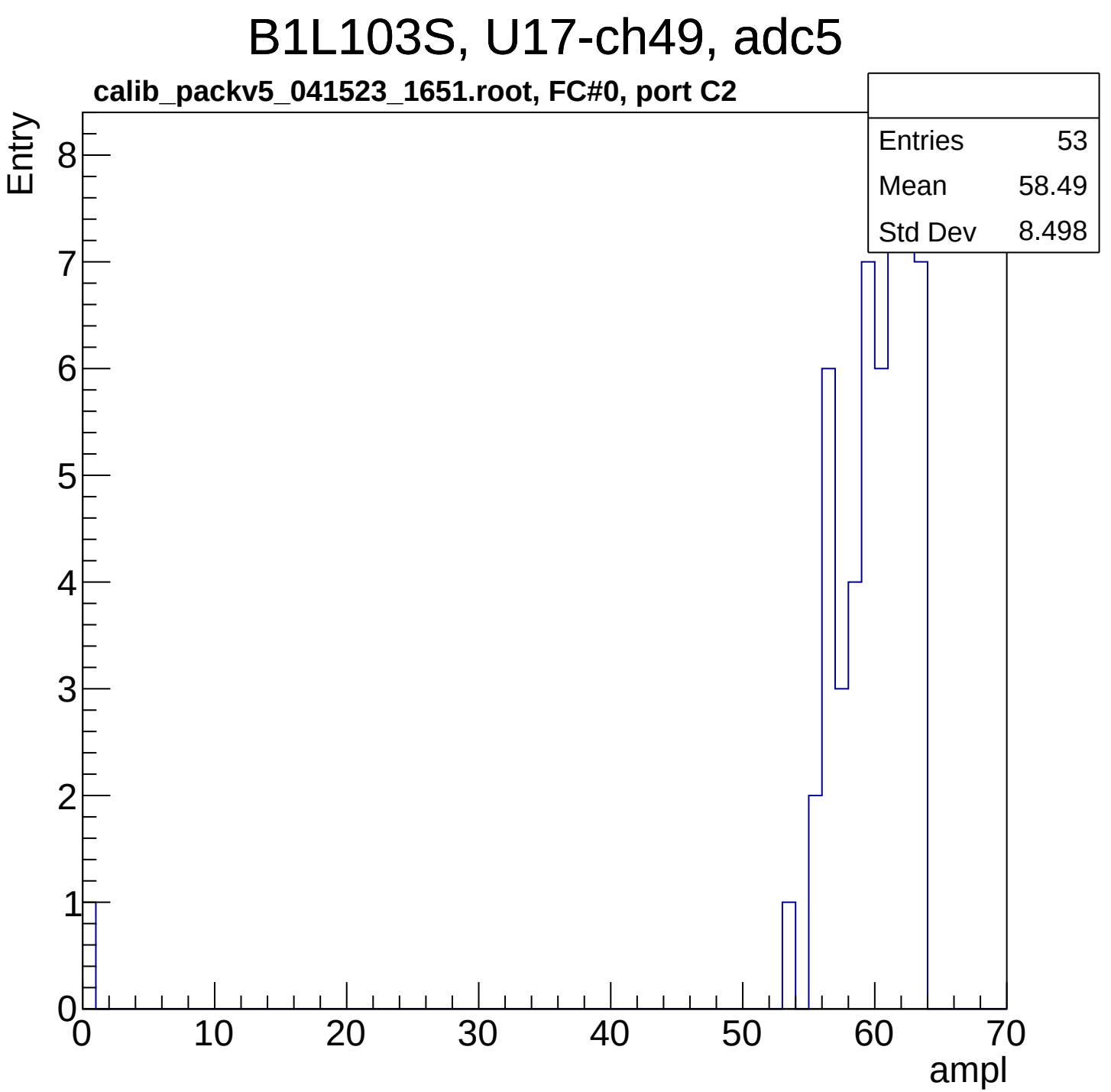

B1L103S, U17-ch49, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 23.83
Std Dev 11.81
Gaus mean : 29.6618
Gaus Width: 4.1758
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

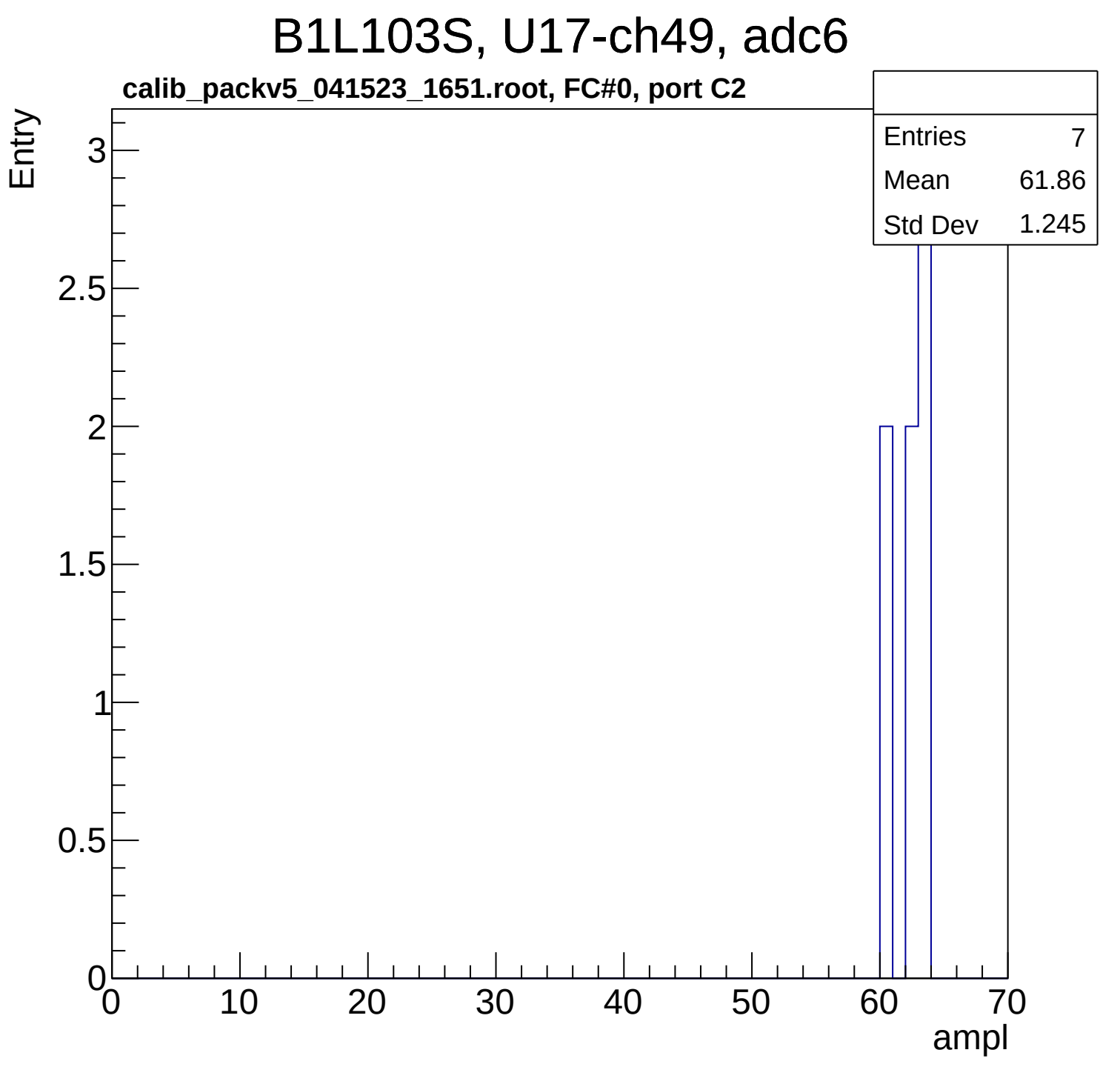

B1L103S, U17-ch49, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 32.11
Std Dev 10.99
Gaus mean : 36.0097
Gaus Width: 3.9737
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

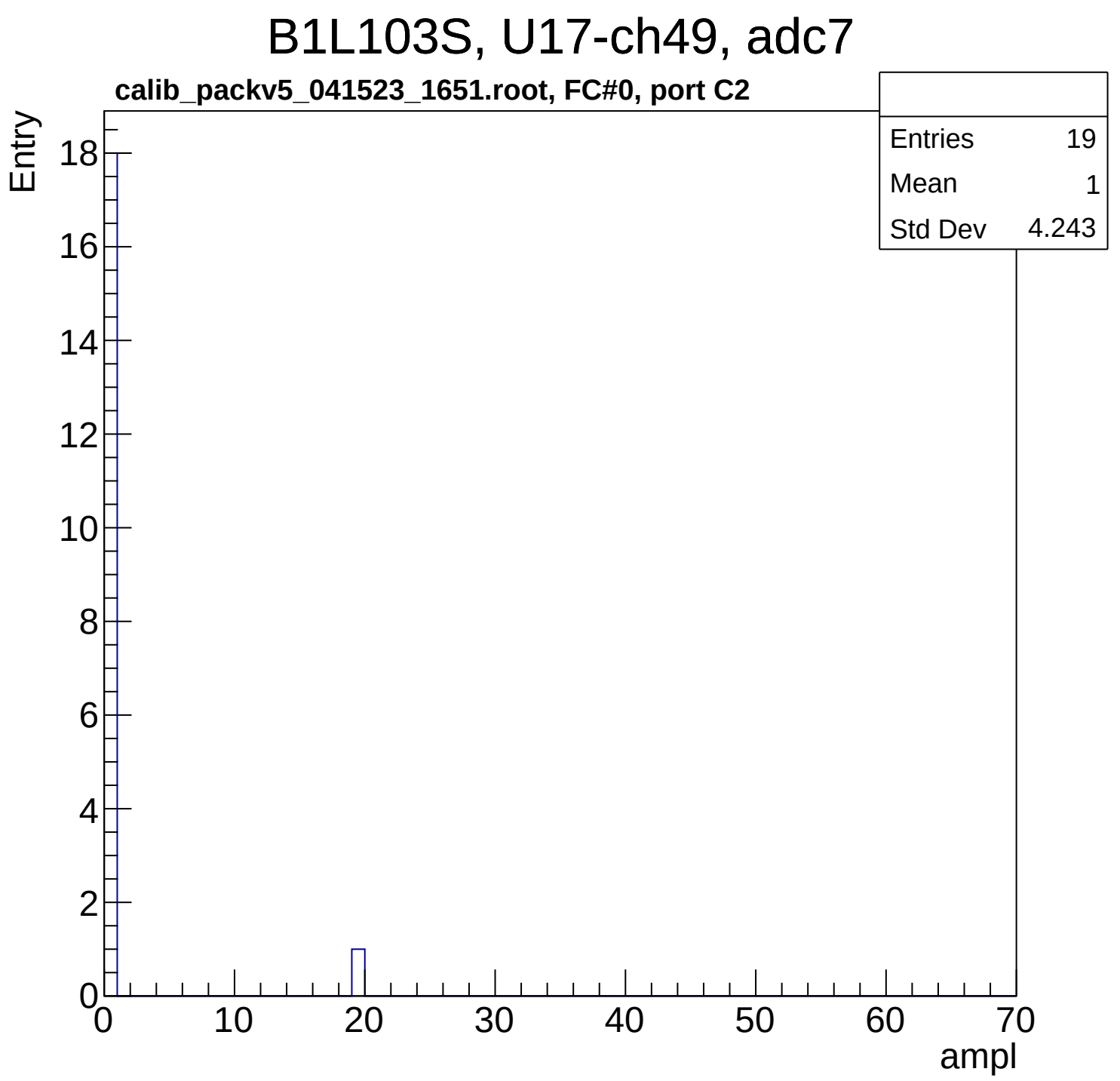

B1L103S, U17-ch49, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 37.1
Std Dev 13.82
Gaus mean : 42.7278
Gaus Width: 3.4840
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

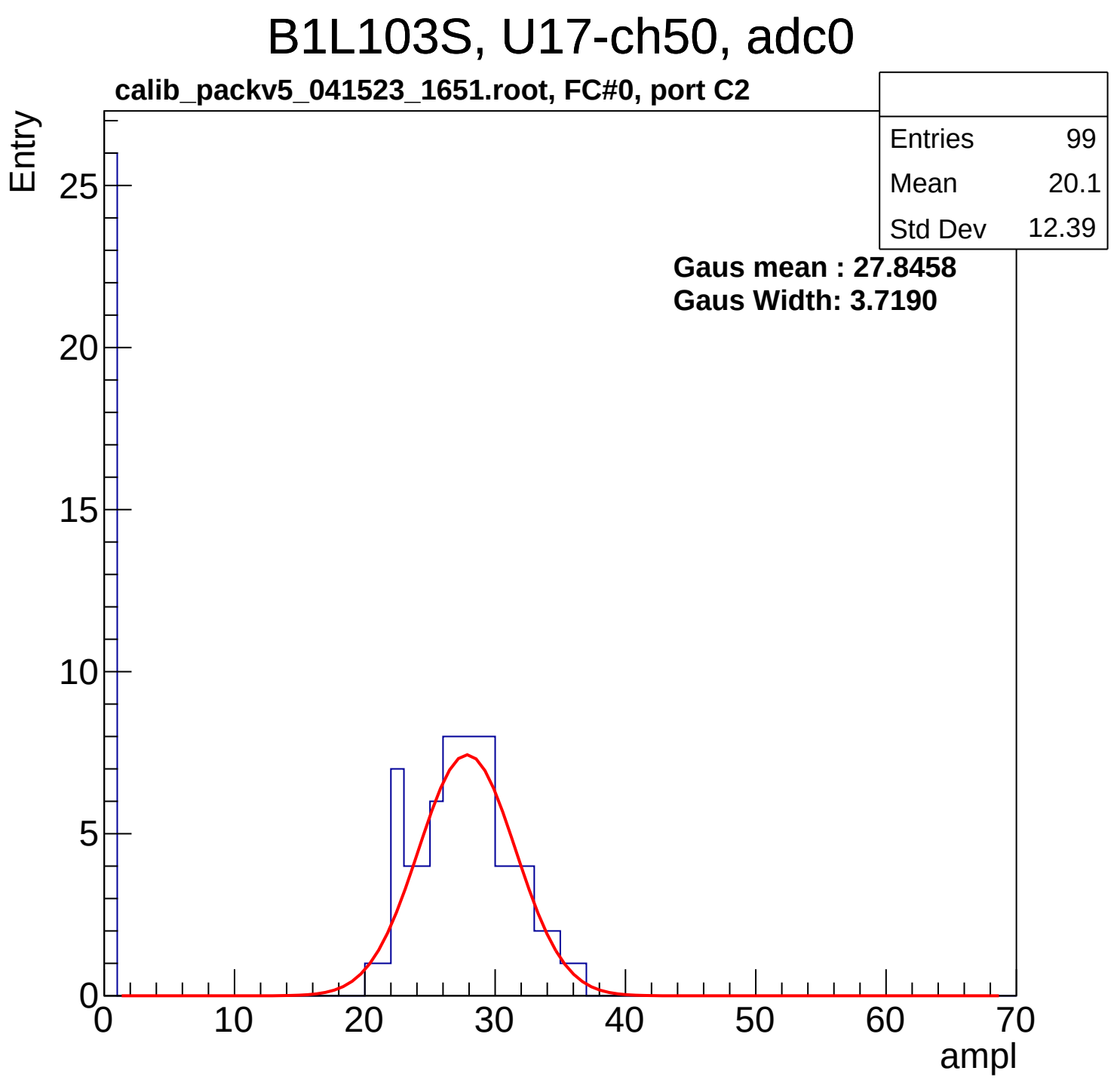

B1L103S, U17-ch49, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 48.78
Std Dev 6.537
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

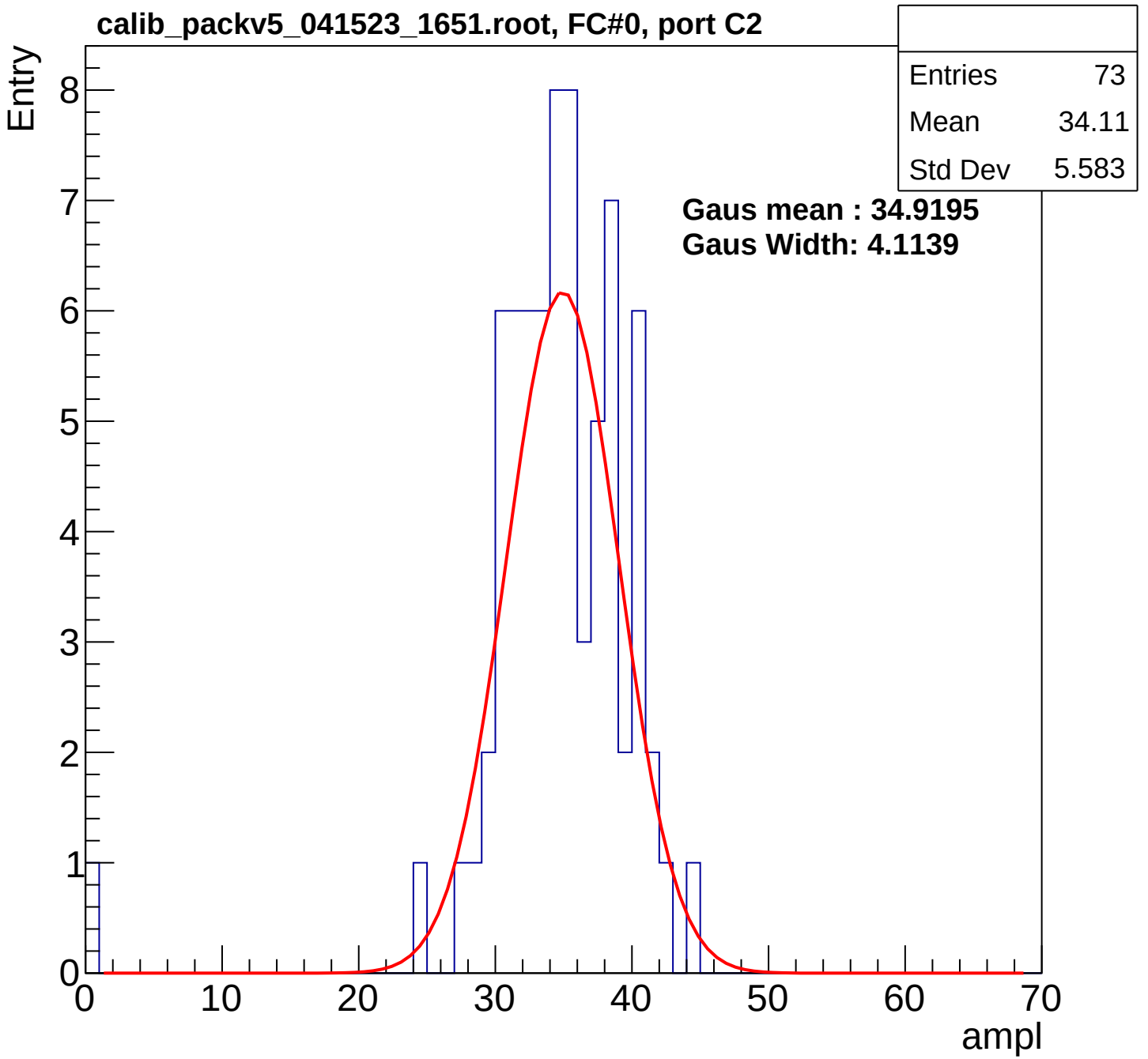

B1L103S, U17-ch49, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 55.37
Std Dev 3.214
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

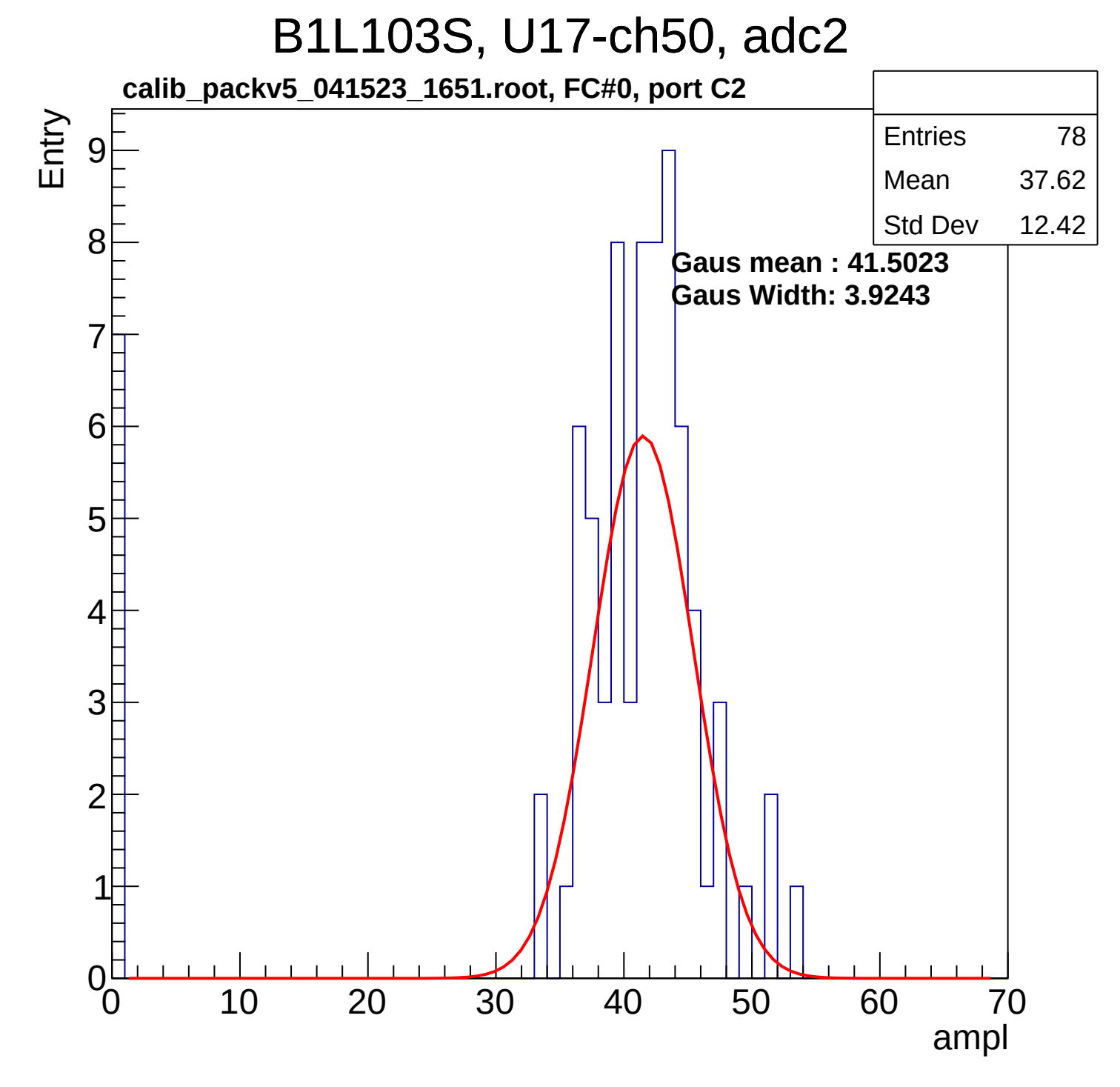

B1L103S, U17-ch49, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.49
Std Dev 8.498
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

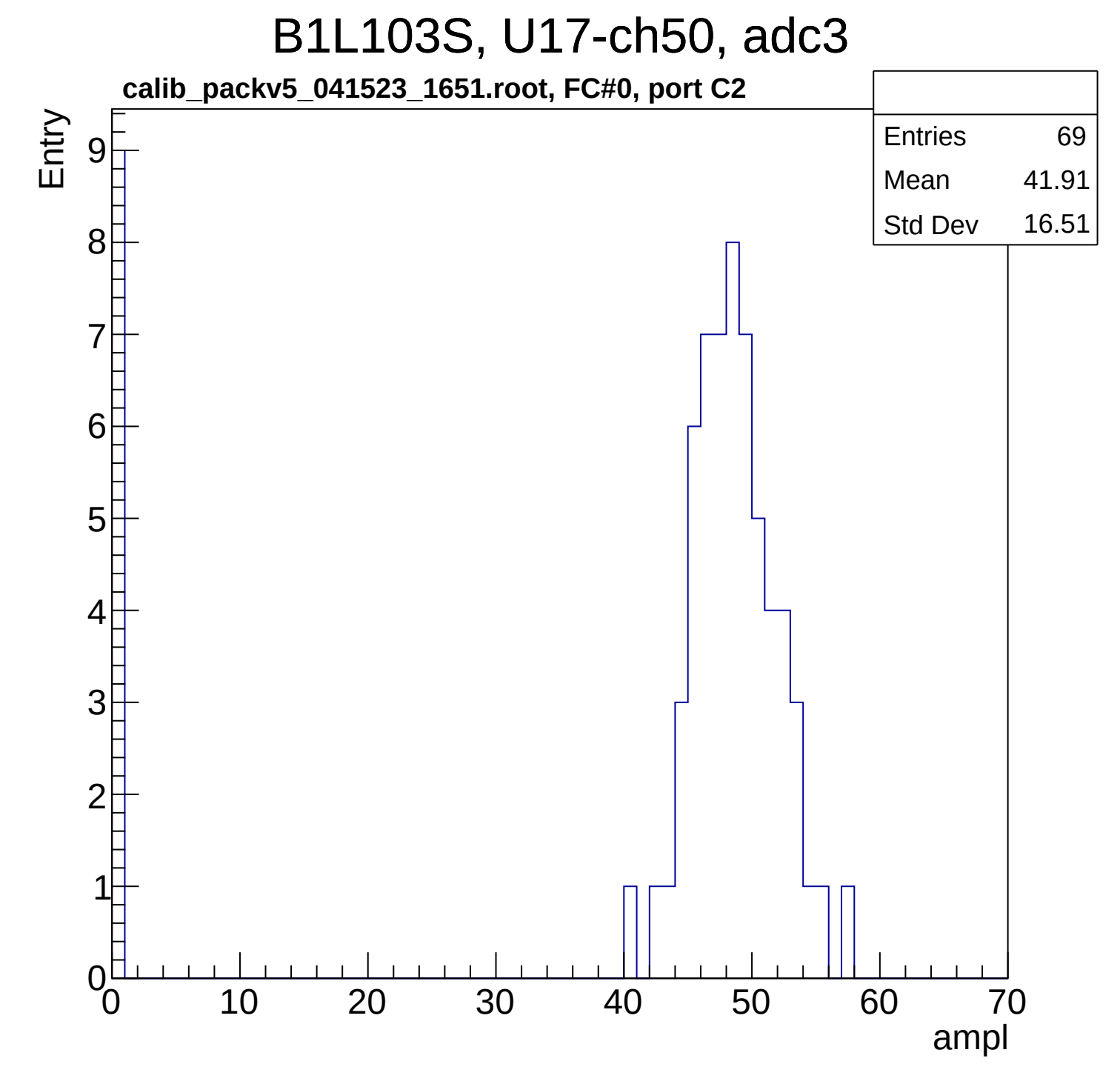

B1L103S, U17-ch49, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.86
Std Dev 1.245
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

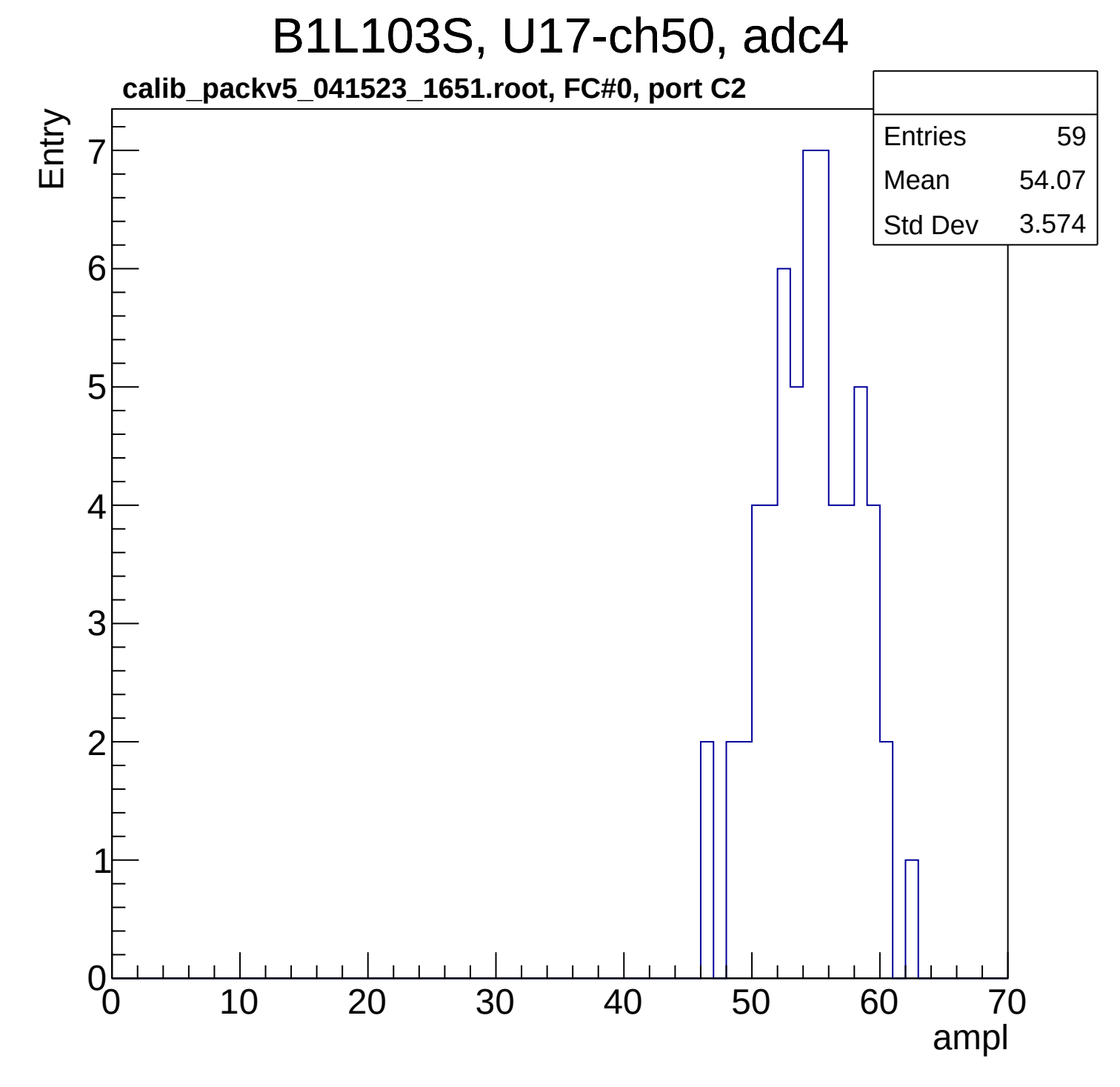

B1L103S, U17-ch49, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1
Std Dev 4.243
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

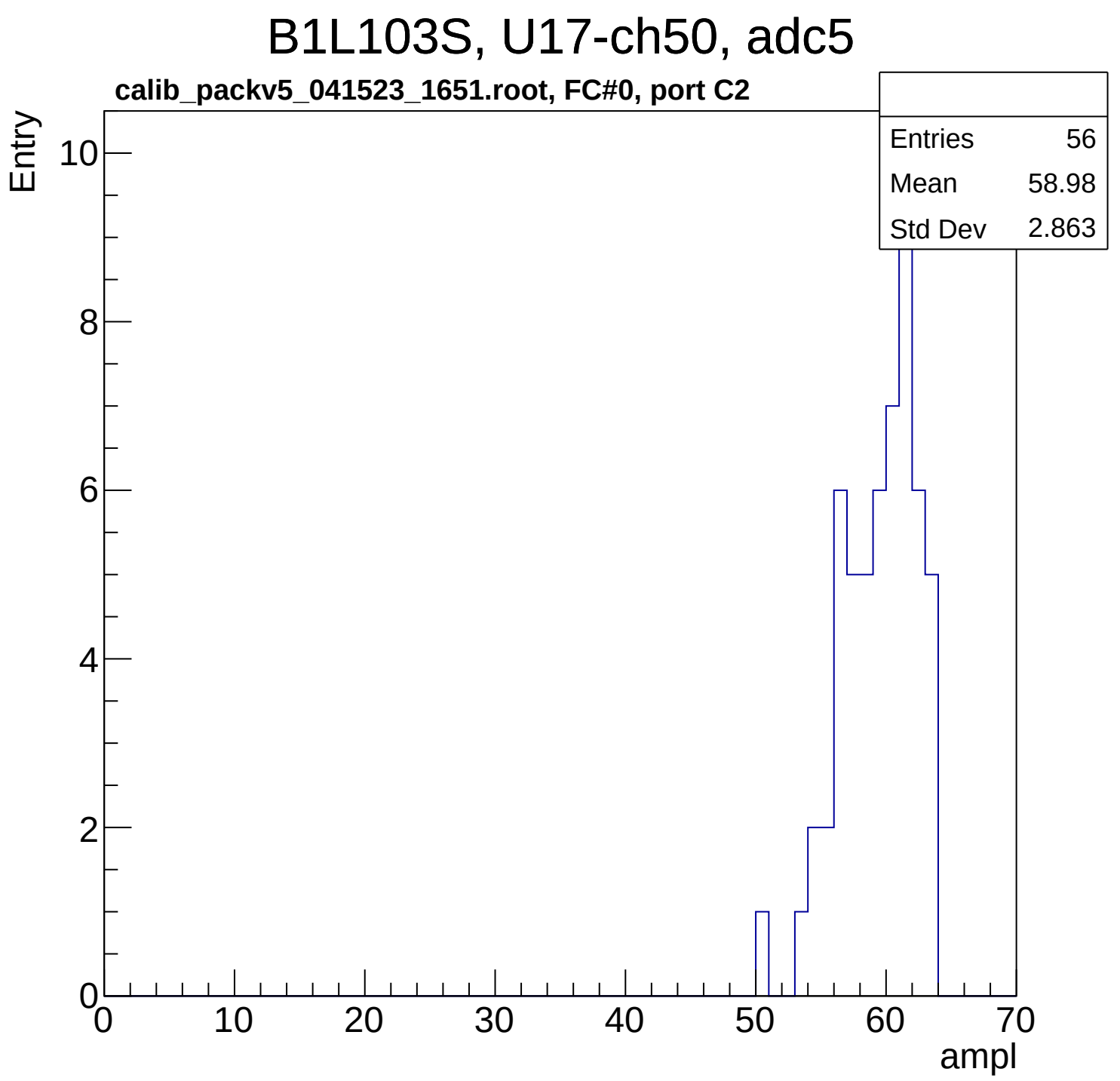

B1L103S, U17-ch50, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 20.1
Std Dev 12.39
Gaus mean : 27.8458
Gaus Width: 3.7190
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70

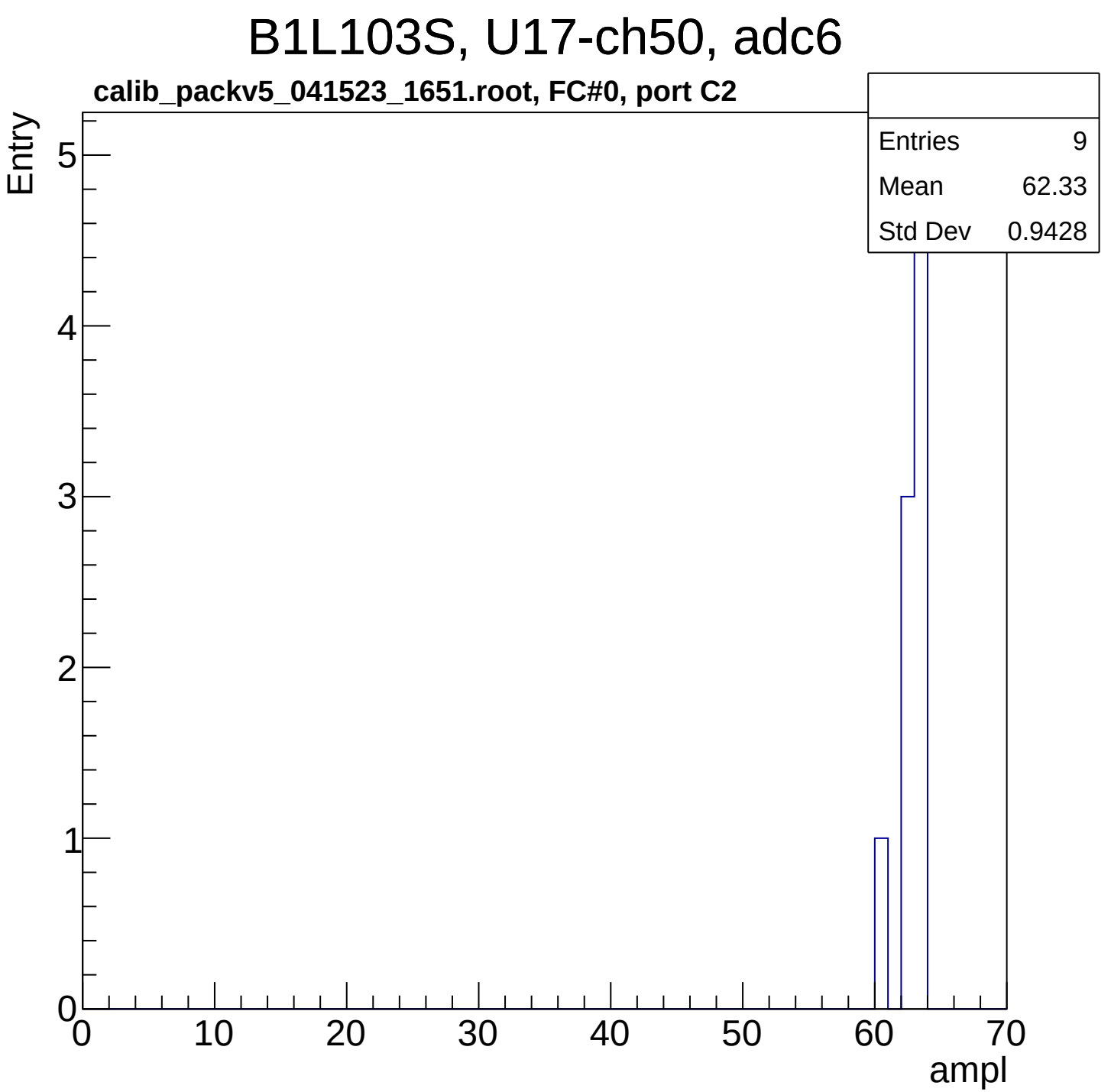

B1L103S, U17-ch50, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 34.11
Std Dev 5.583
Gaus mean : 34.9195
Gaus Width: 4.1139
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

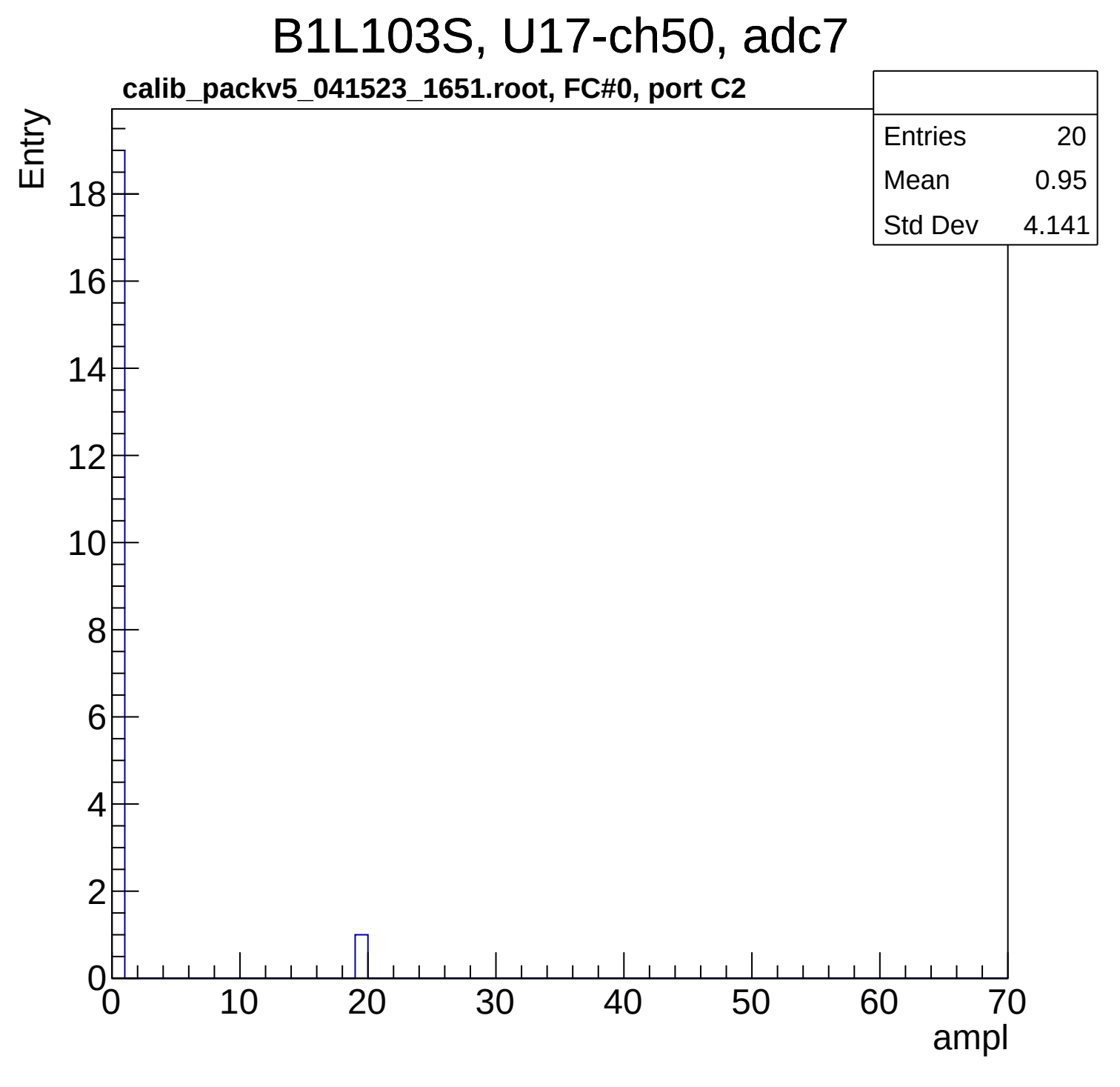

B1L103S, U17-ch50, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 37.62
Std Dev 12.42
Gaus mean : 41.5023
Gaus Width: 3.9243
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

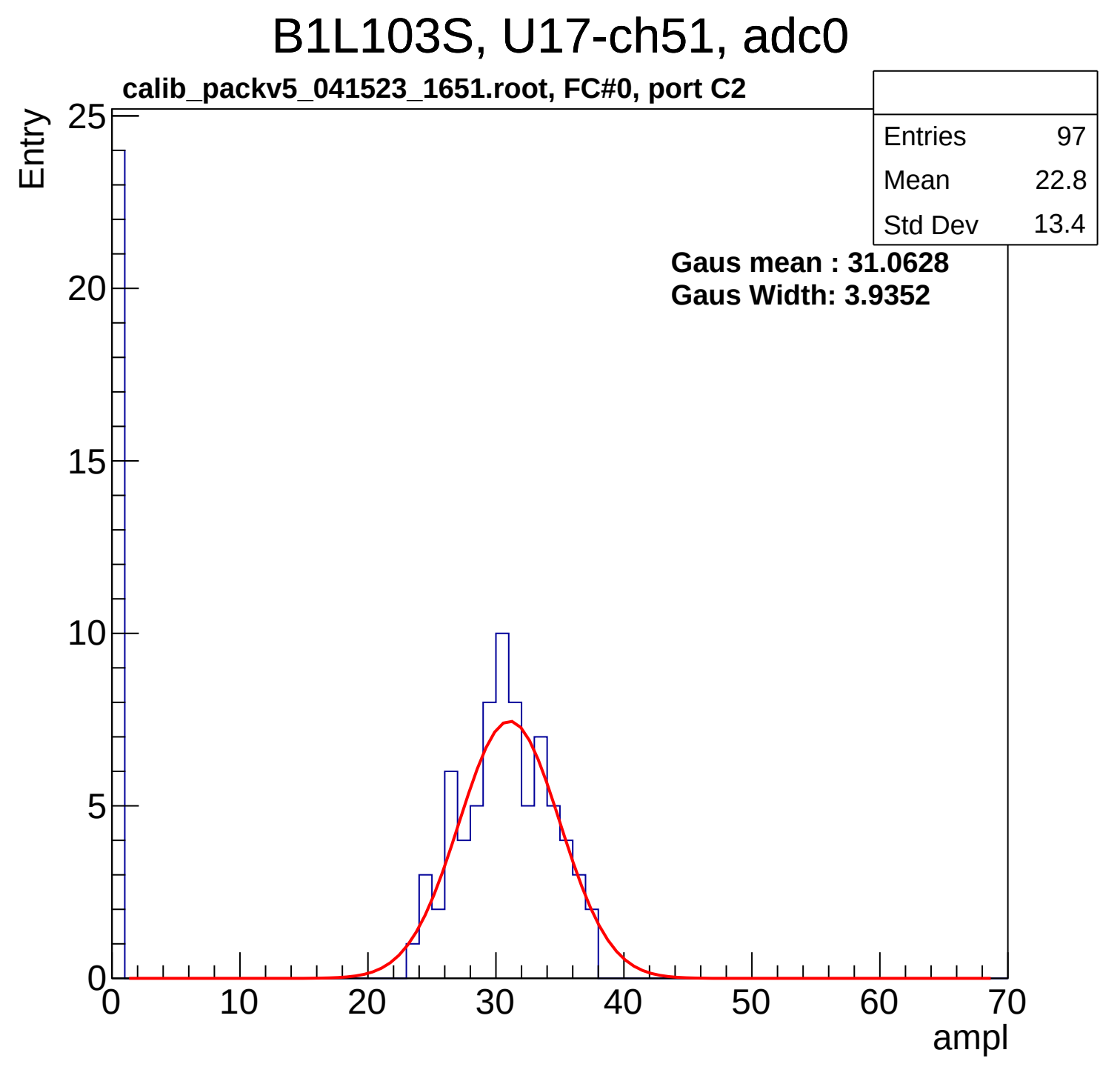

B1L103S, U17-ch50, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 41.91
Std Dev 16.51
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

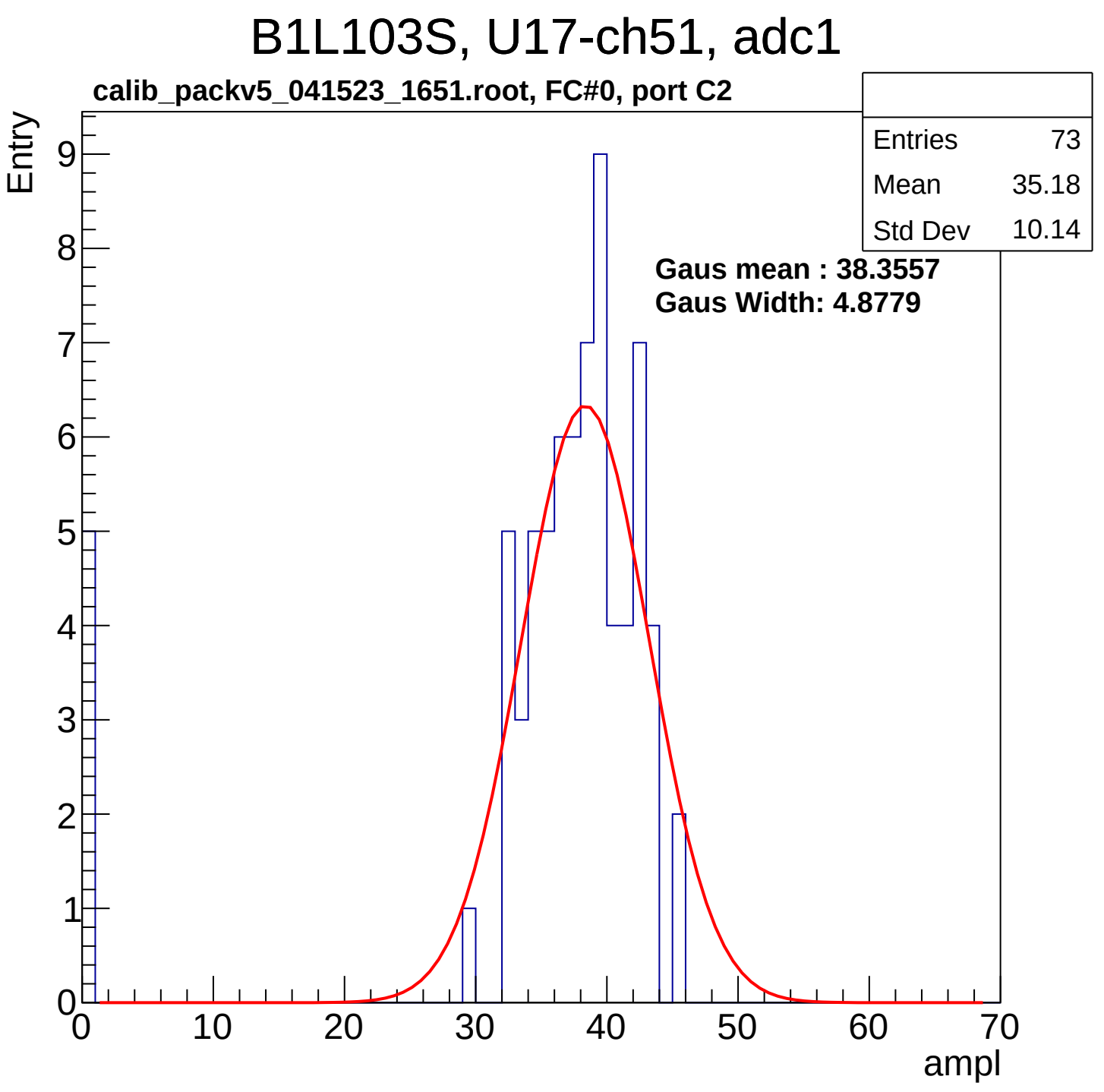

B1L103S, U17-ch50, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.07
Std Dev 3.574
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

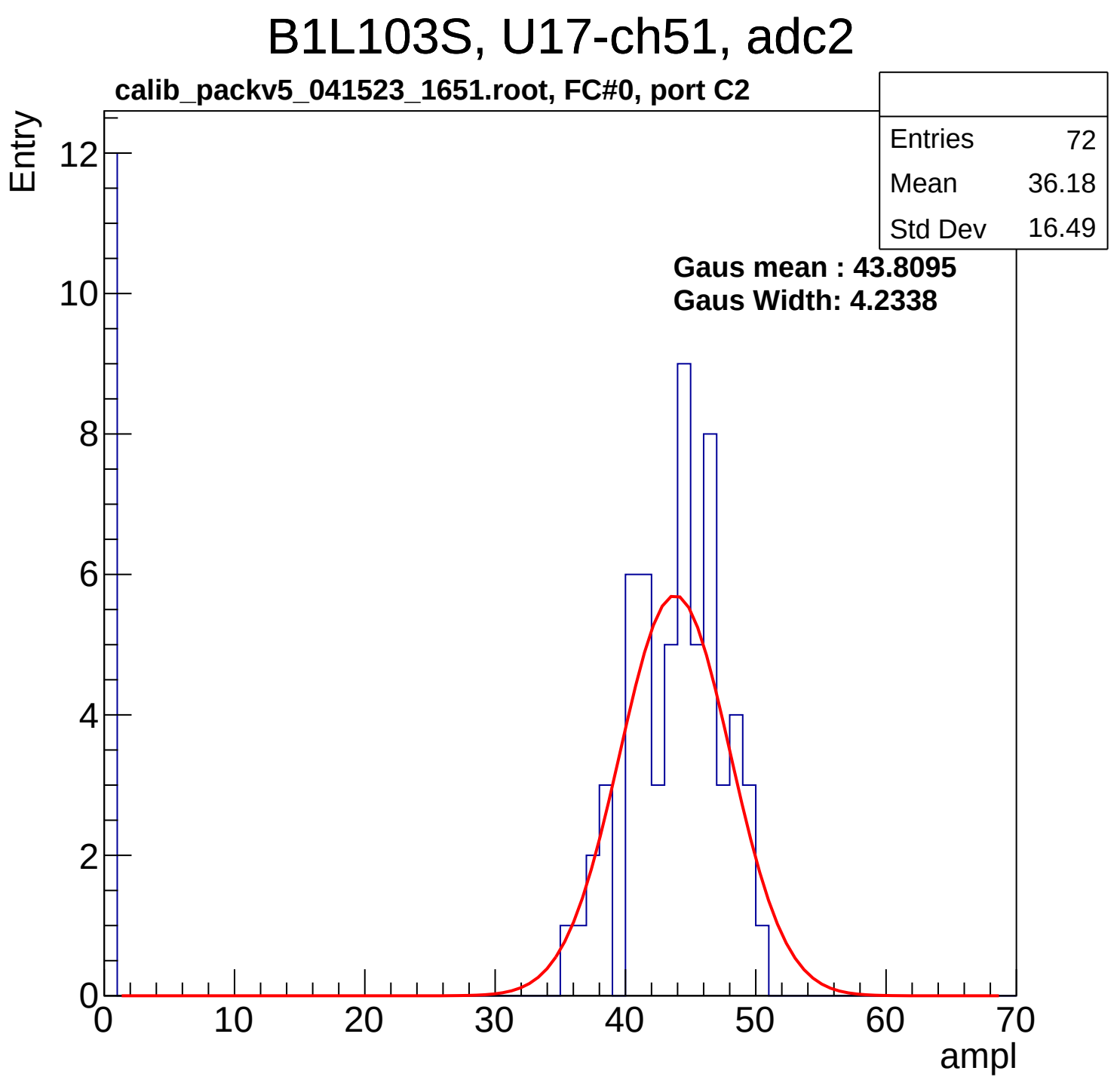

B1L103S, U17-ch50, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.98
Std Dev 2.863
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

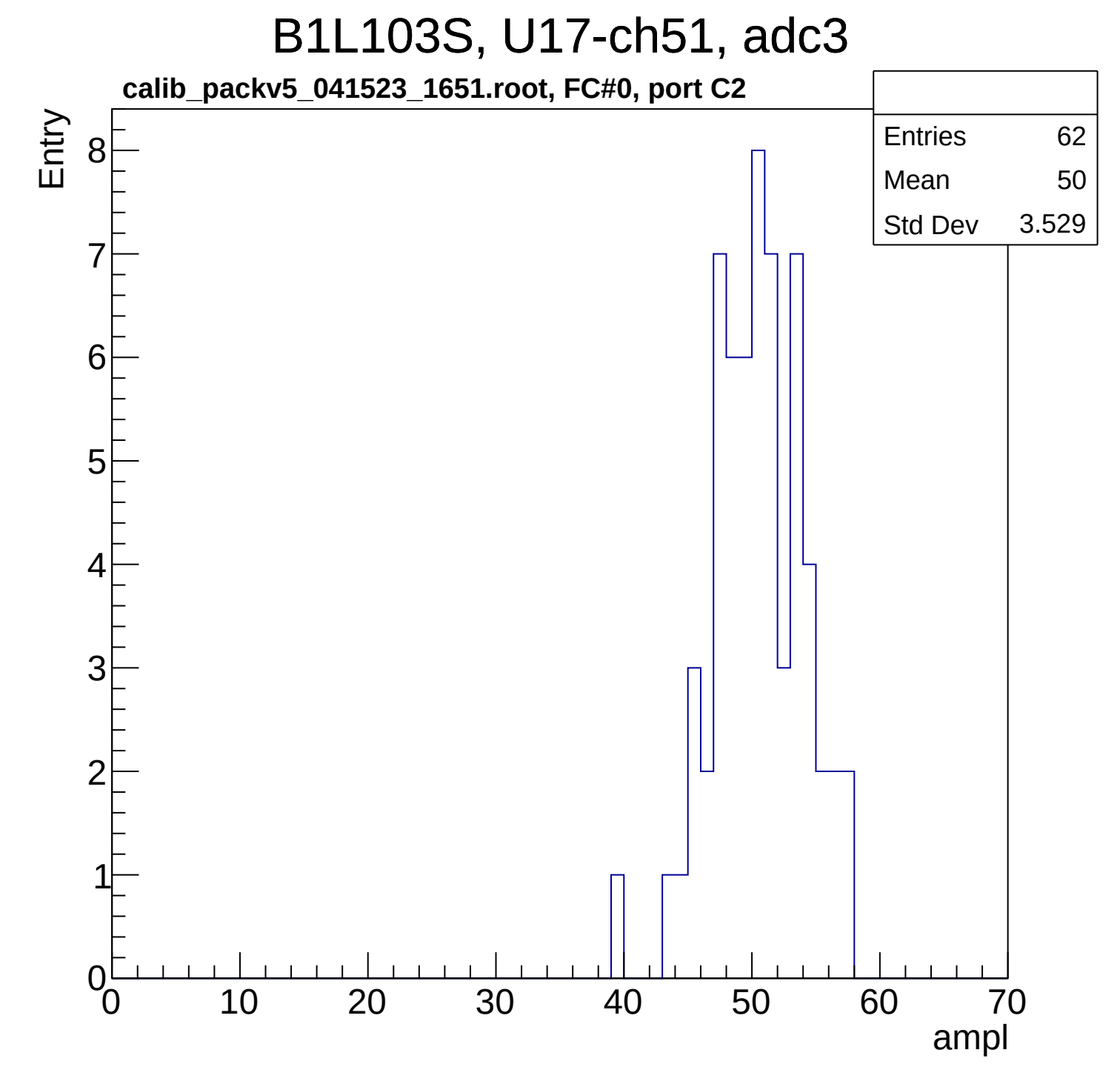

B1L103S, U17-ch50, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 62.33
Std Dev 0.9428
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

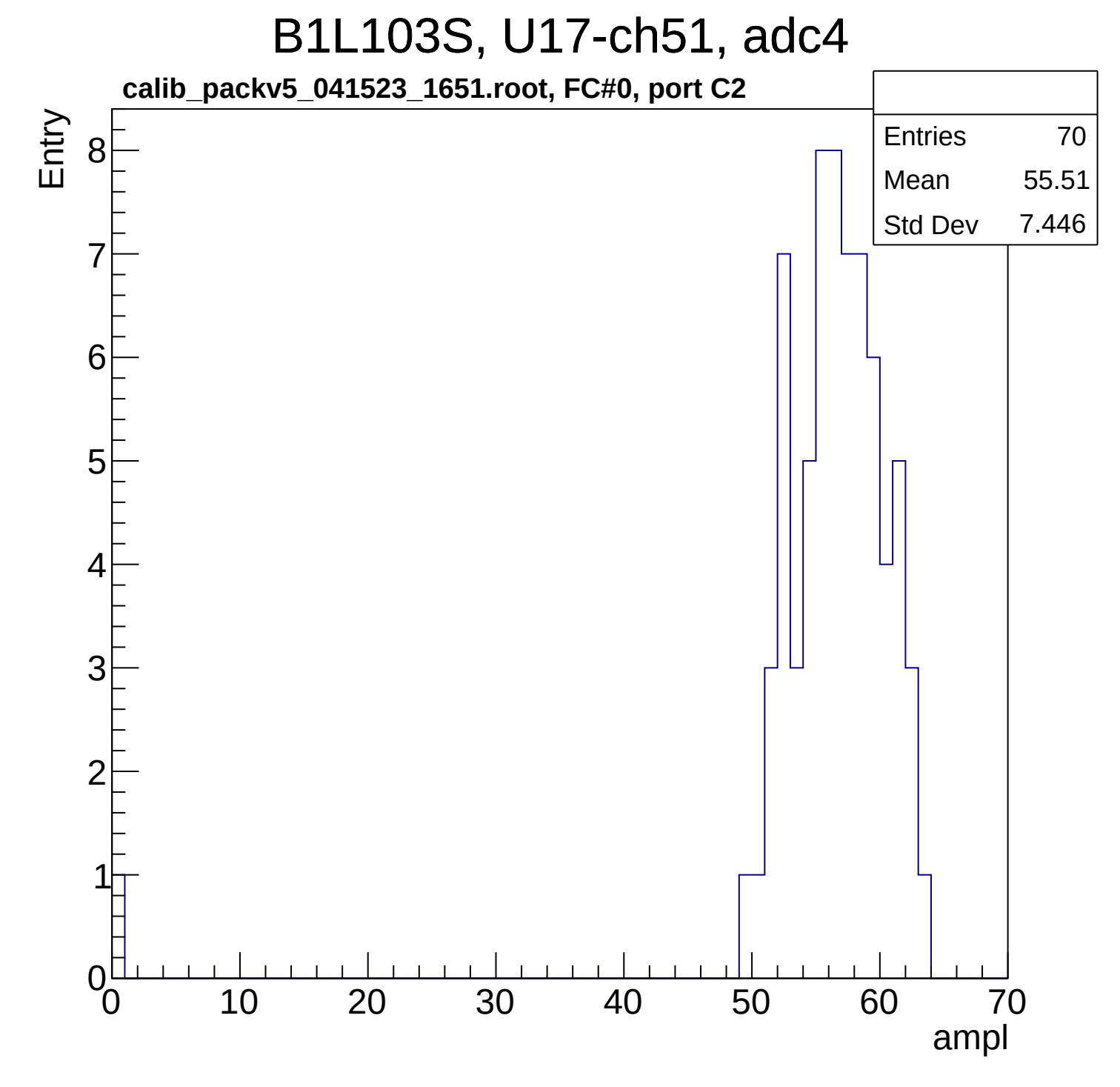

B1L103S, U17-ch50, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 0.95
Std Dev 4.141
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

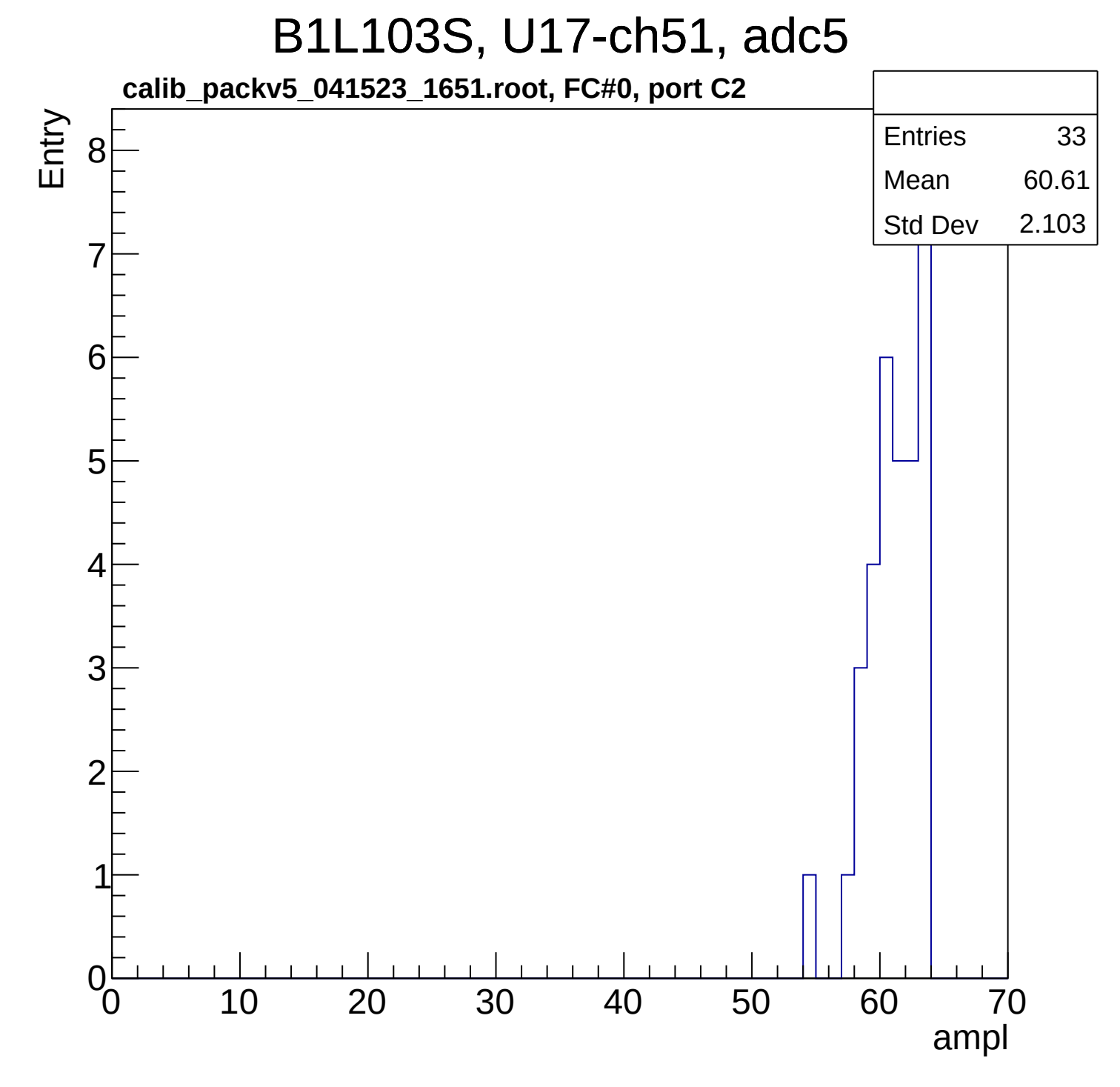

B1L103S, U17-ch51, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 22.8
Std Dev 13.4
Gaus mean : 31.0628
Gaus Width: 3.9352
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70

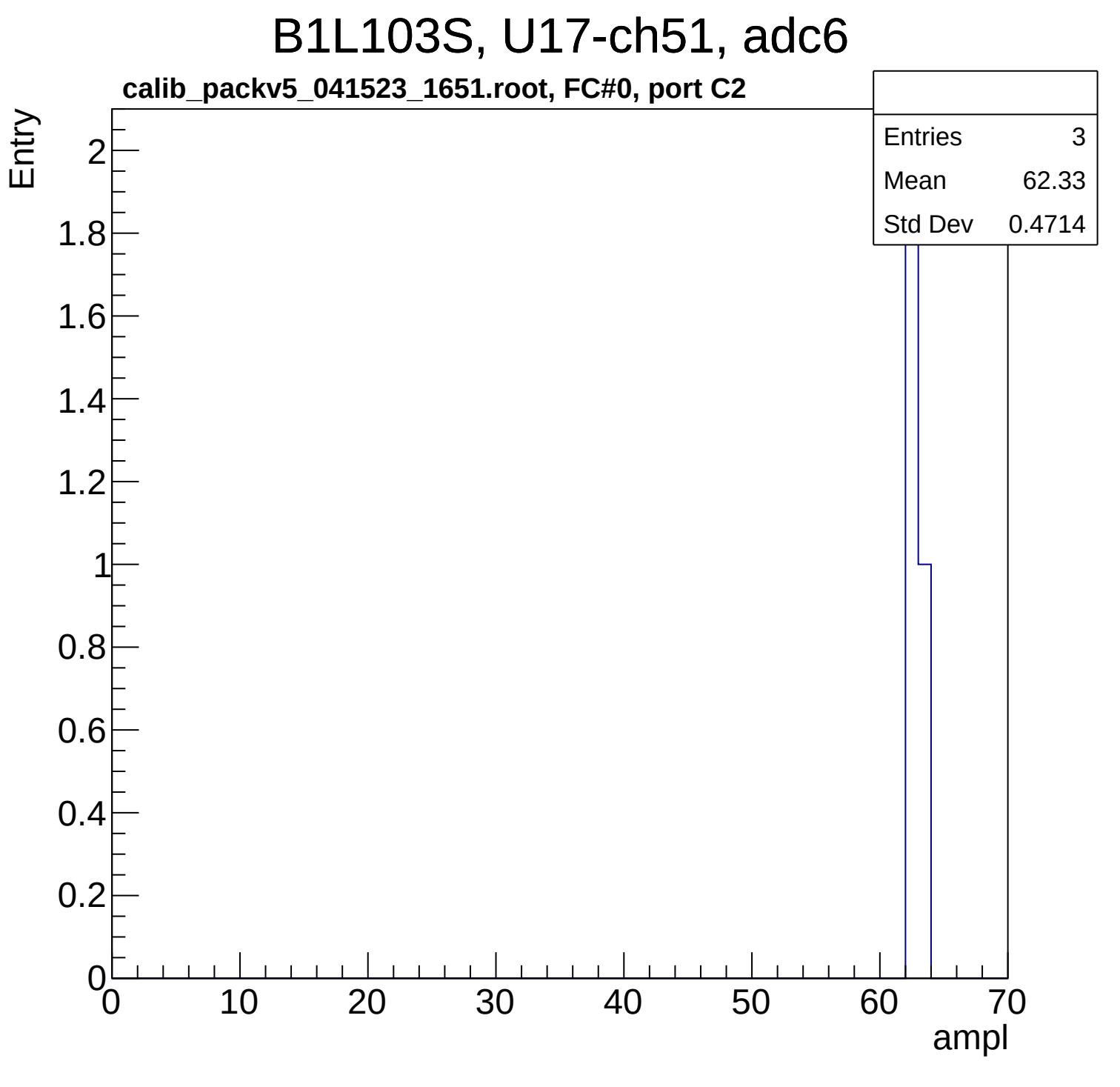

B1L103S, U17-ch51, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 35.18
Std Dev 10.14
Gaus mean : 38.3557
Gaus Width: 4.8779
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

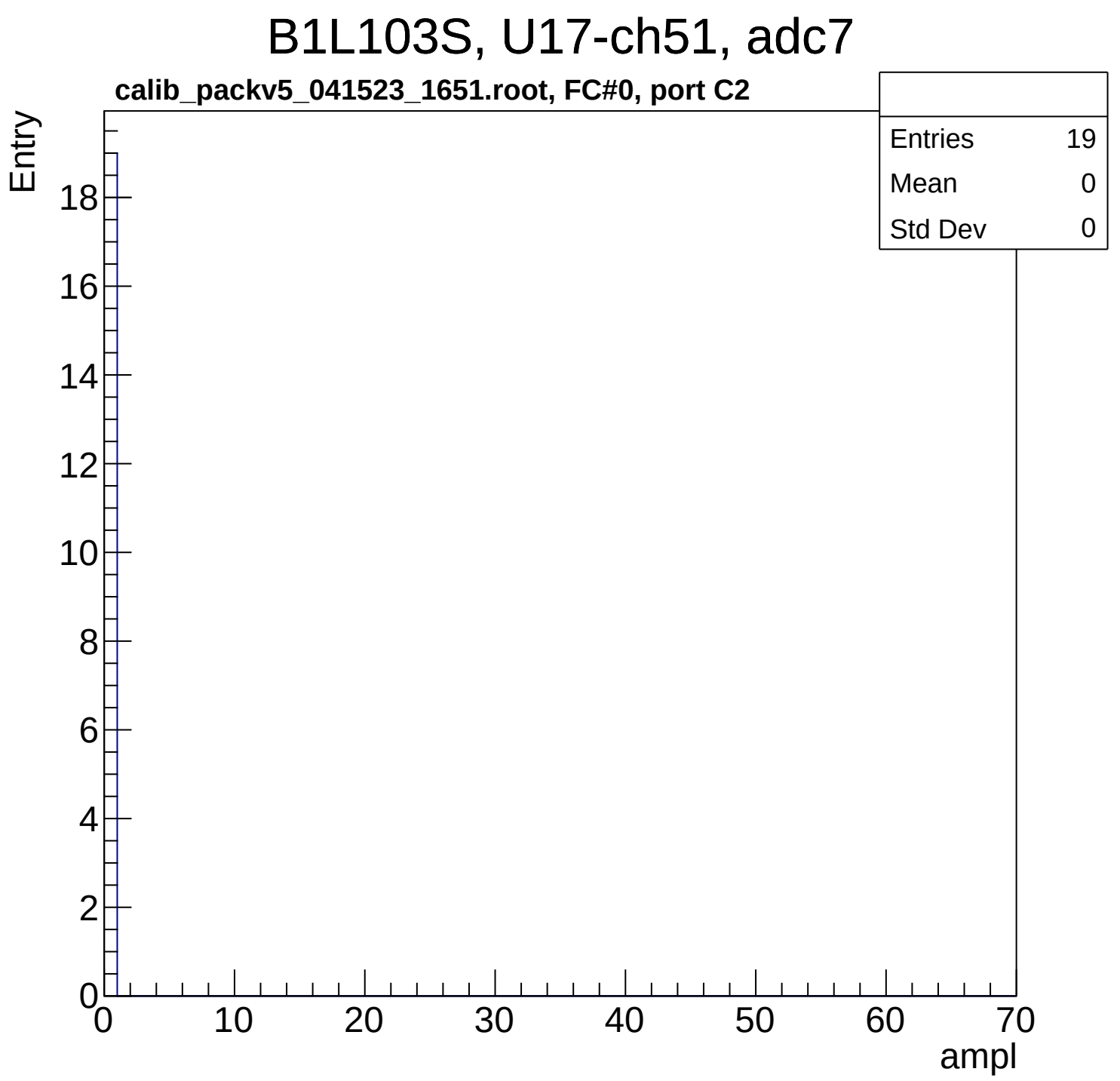

B1L103S, U17-ch51, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 36.18
Std Dev 16.49
Gaus mean : 43.8095
Gaus Width: 4.2338
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

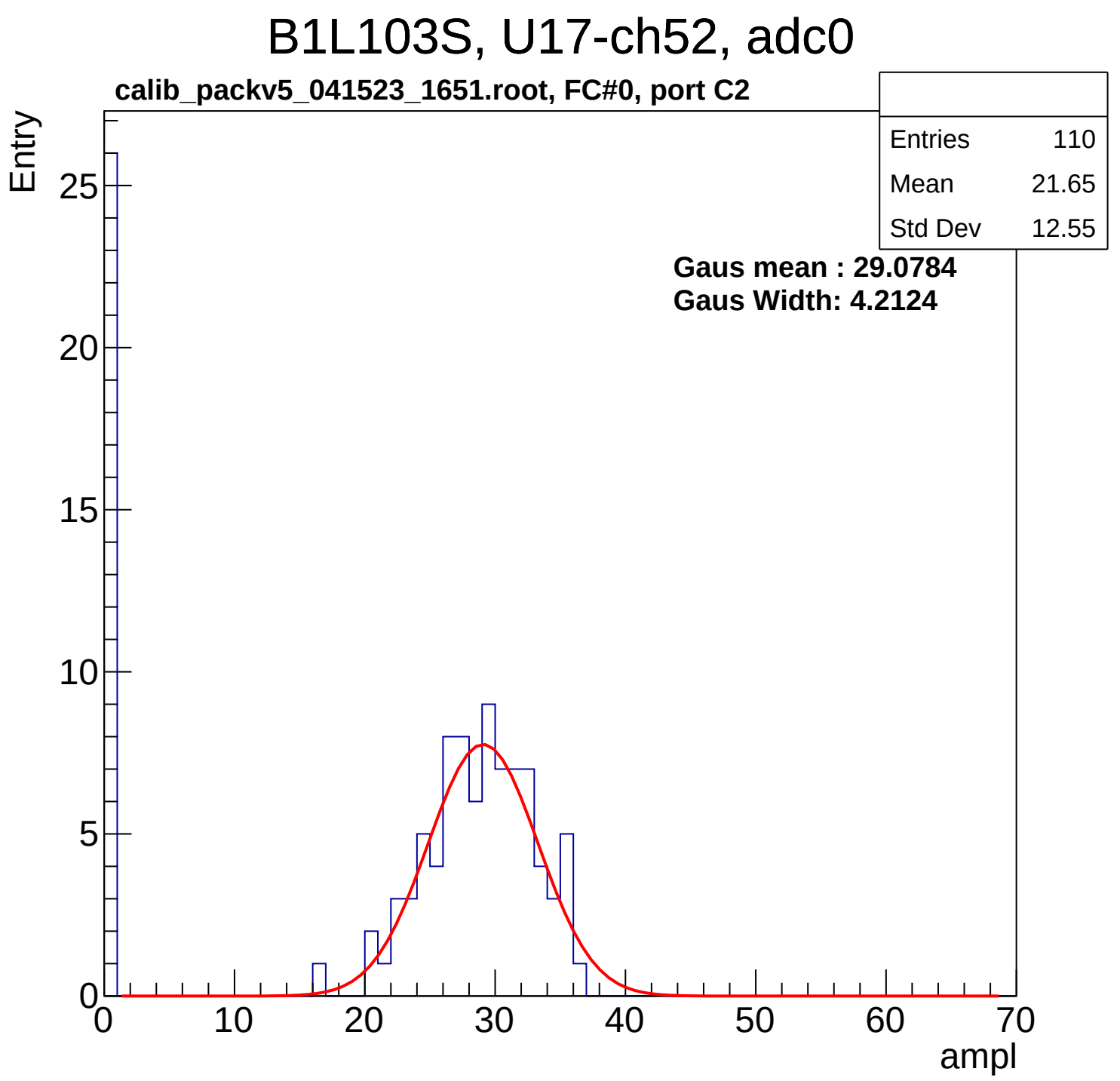

B1L103S, U17-ch51, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 50
Std Dev 3.529
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

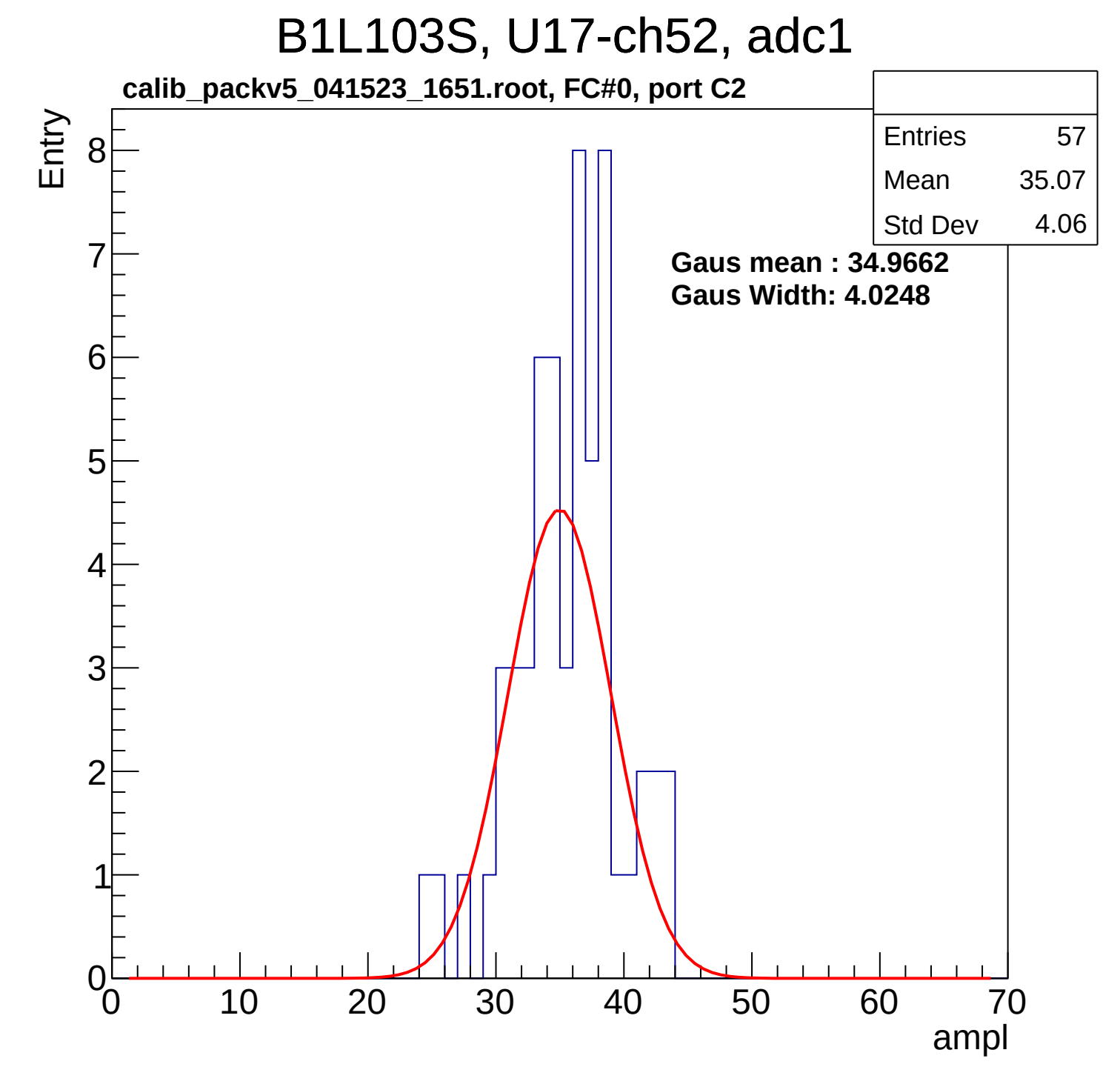

B1L103S, U17-ch51, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 55.51
Std Dev 7.446
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

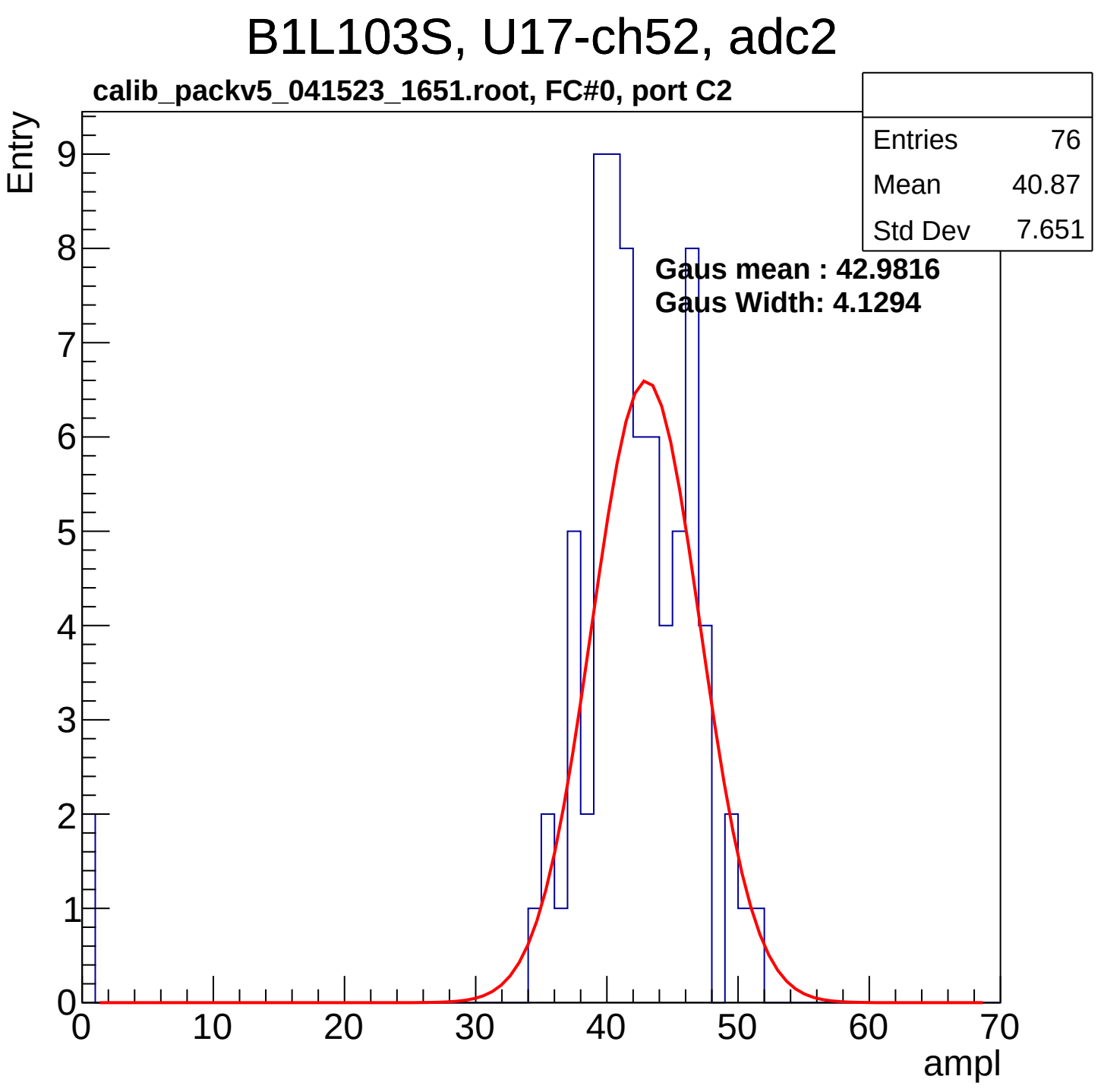

B1L103S, U17-ch51, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 60.61
Std Dev 2.103
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

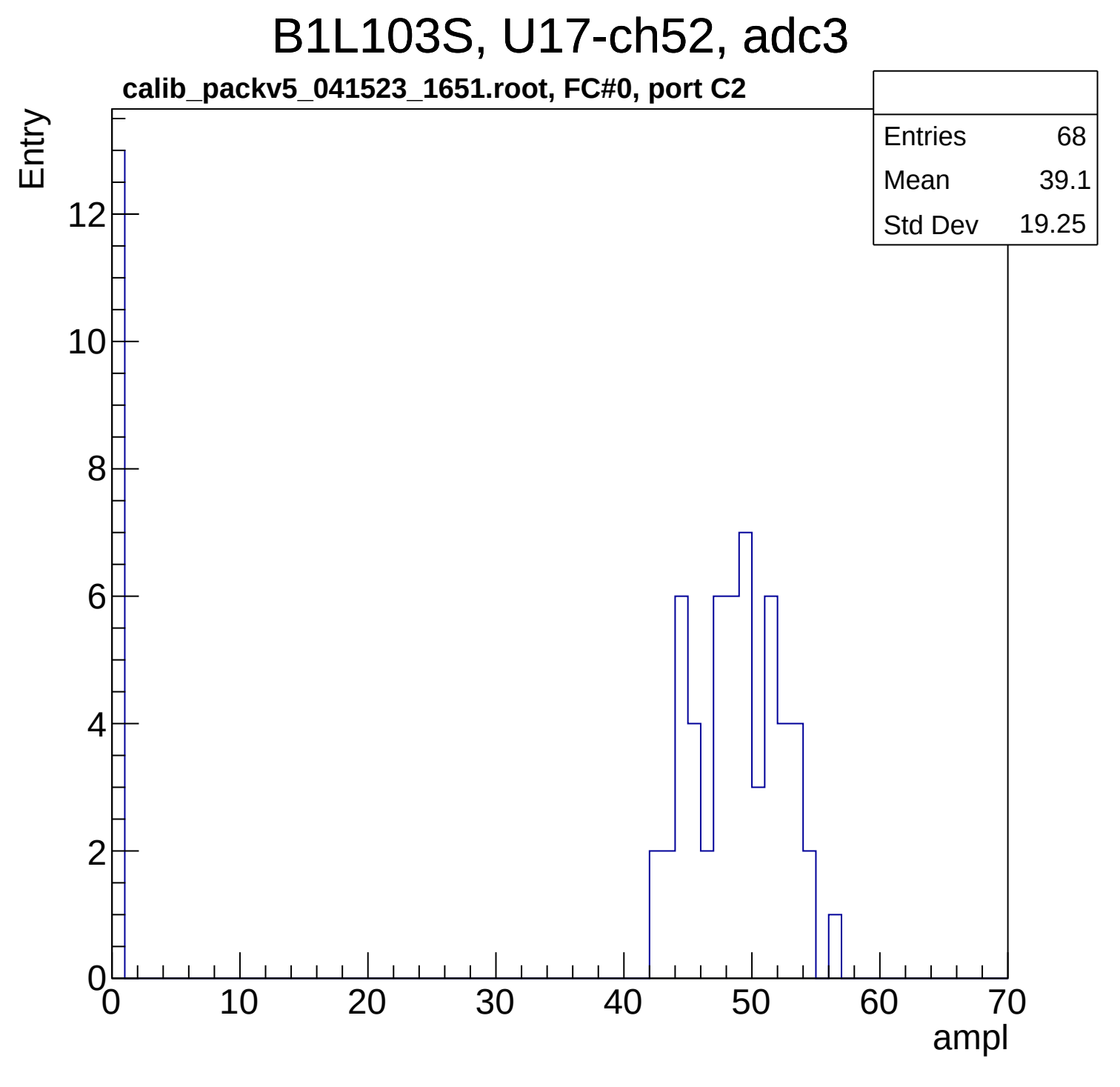

B1L103S, U17-ch51, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

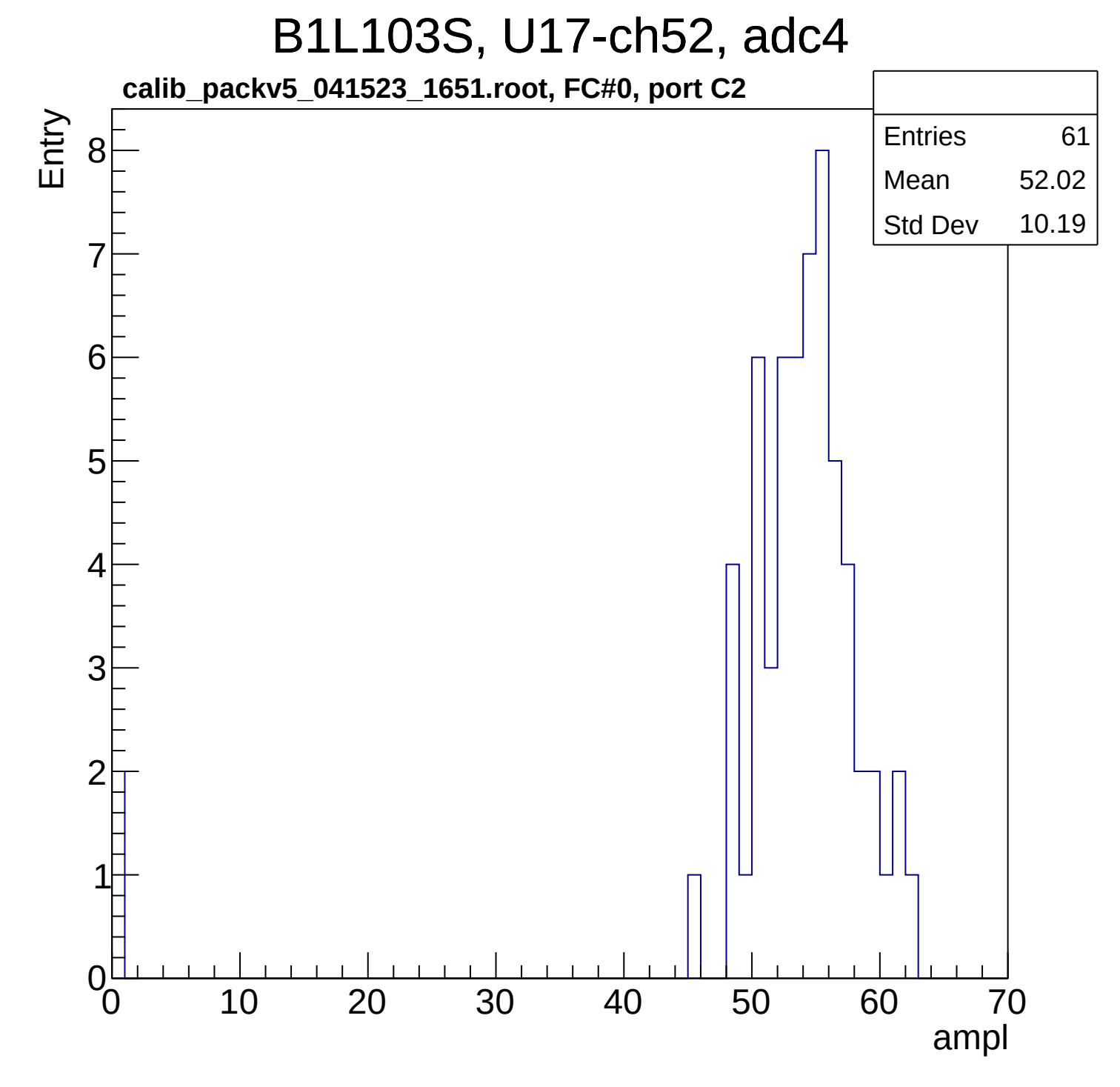

B1L103S, U17-ch51, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

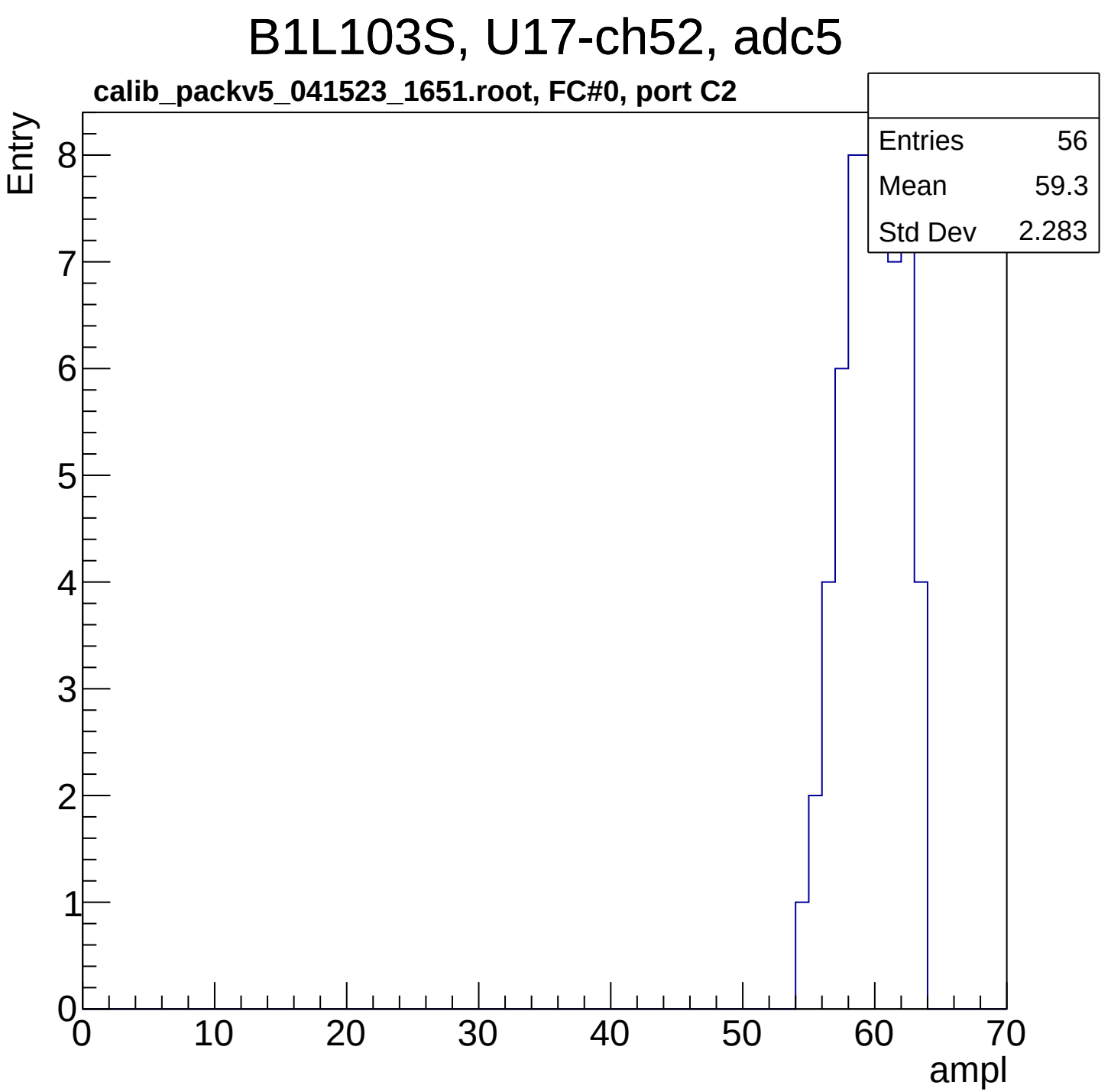

B1L103S, U17-ch52, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 110
Mean 21.65
Std Dev 12.55
Gaus mean : 29.0784
Gaus Width: 4.2124
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70

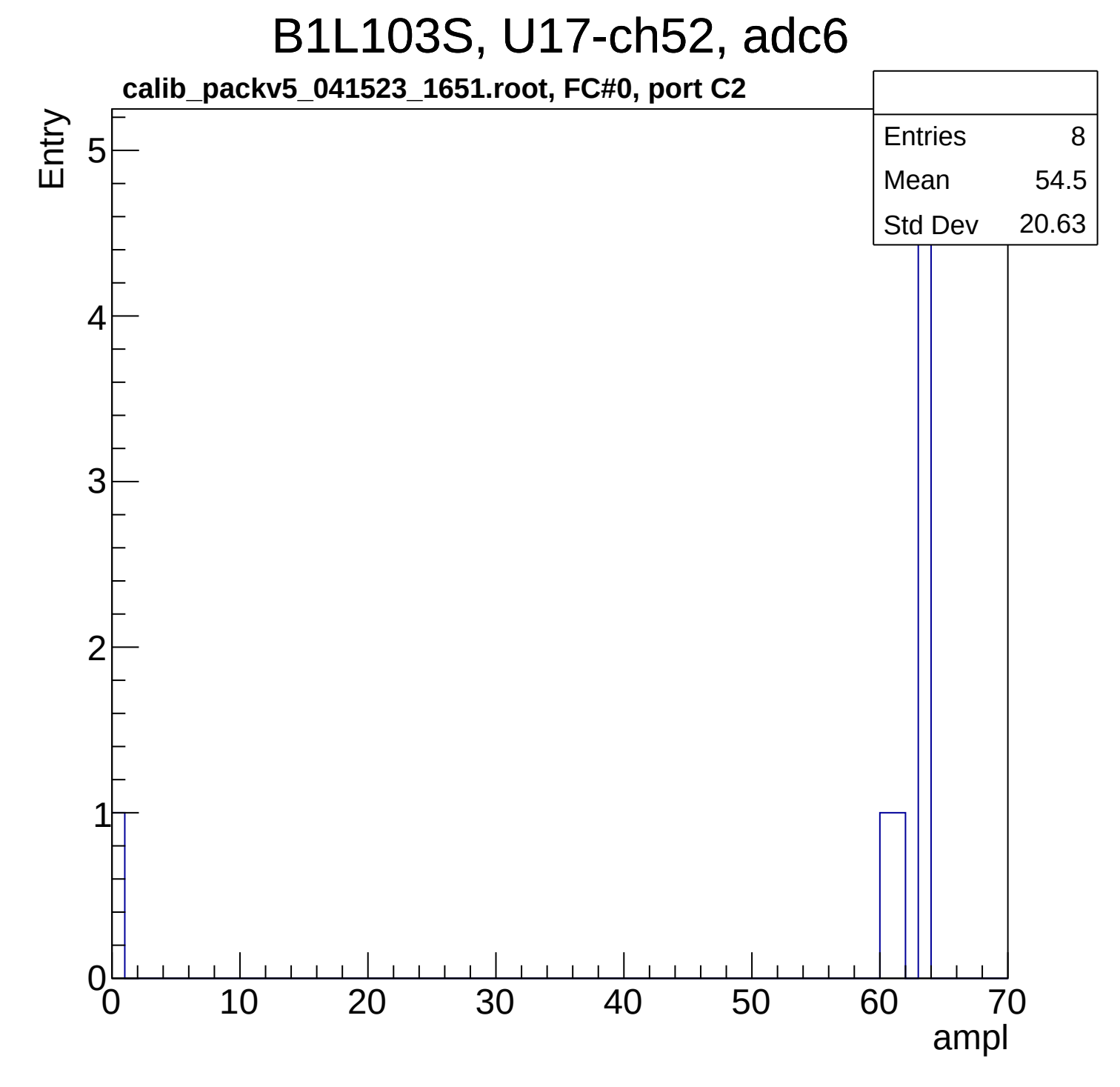

B1L103S, U17-ch52, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 35.07
Std Dev 4.06
Gaus mean : 34.9662
Gaus Width: 4.0248
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

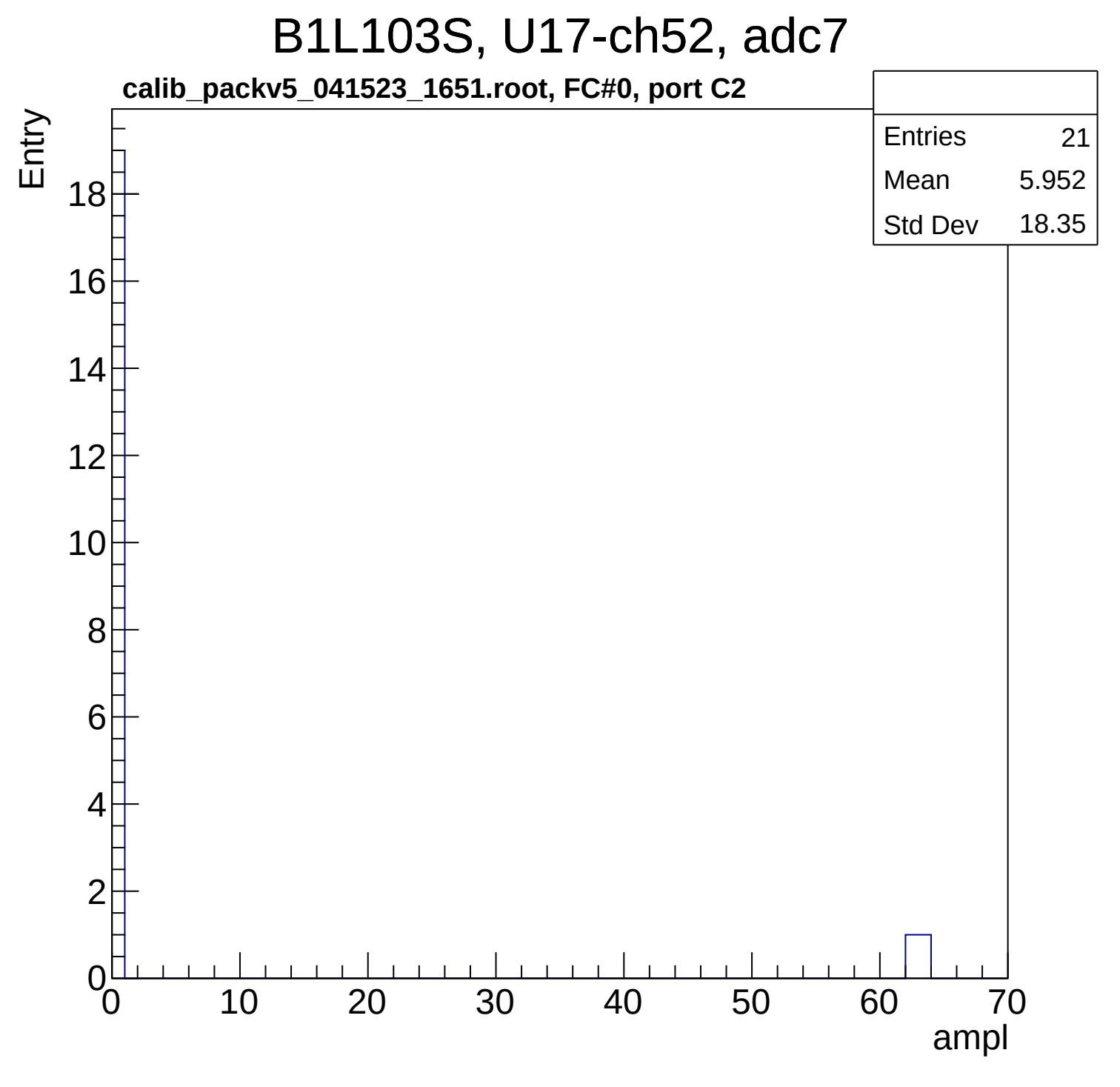

B1L103S, U17-ch52, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 40.87
Std Dev 7.651
Gaus mean : 42.9816
Gaus Width: 4.1294
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

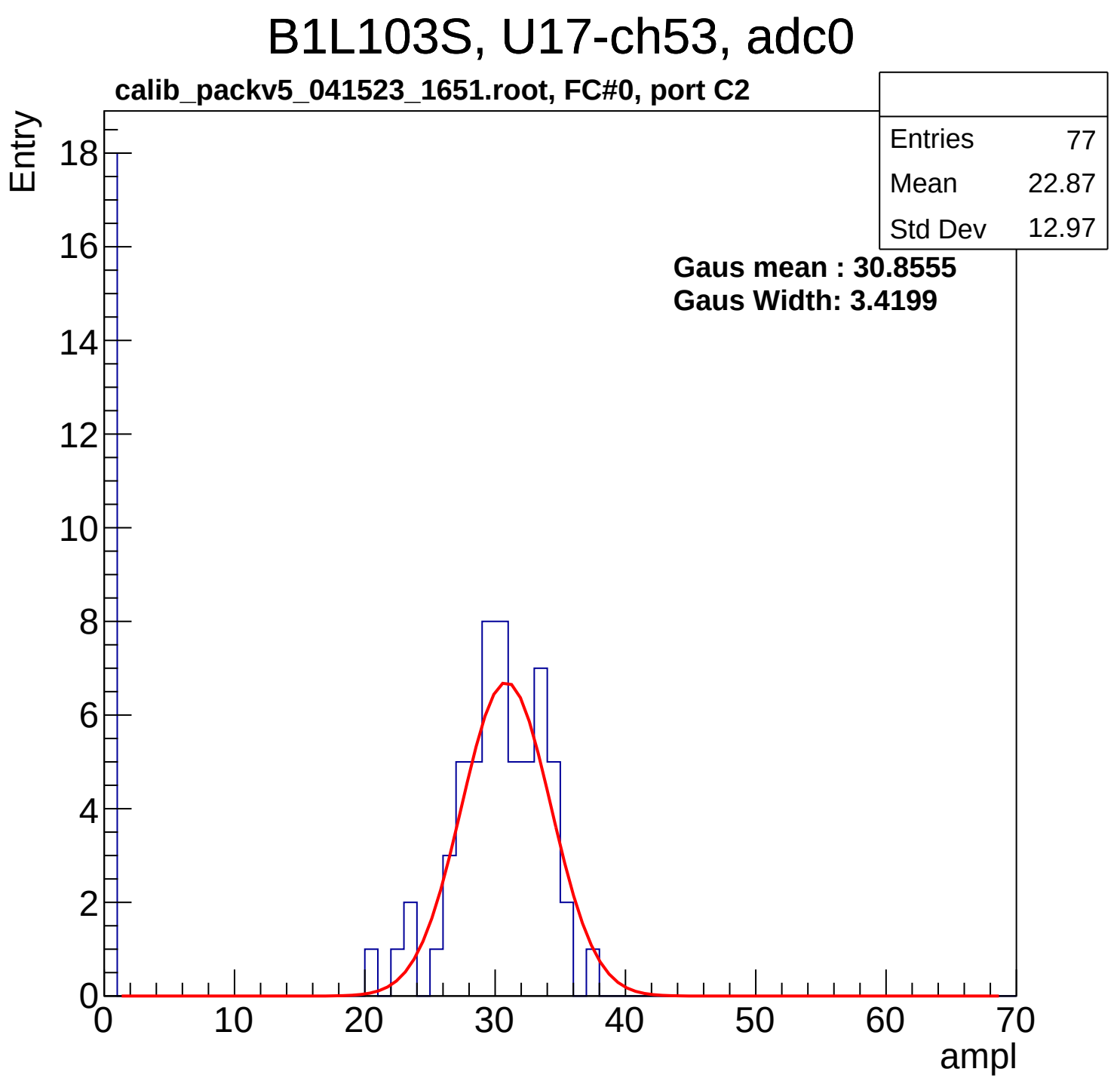

B1L103S, U17-ch52, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 39.1
Std Dev 19.25
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

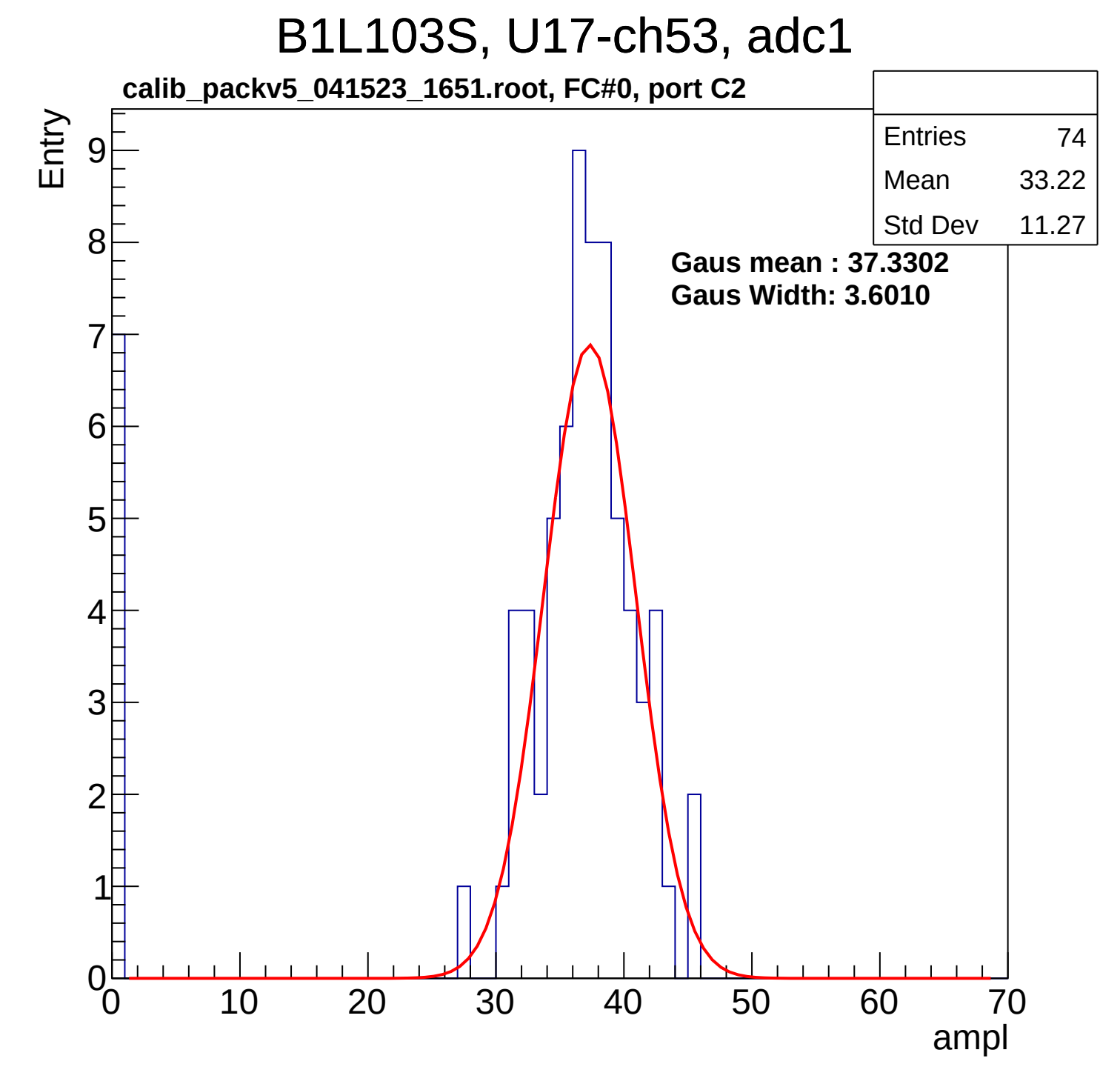

B1L103S, U17-ch52, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 52.02
Std Dev 10.19
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

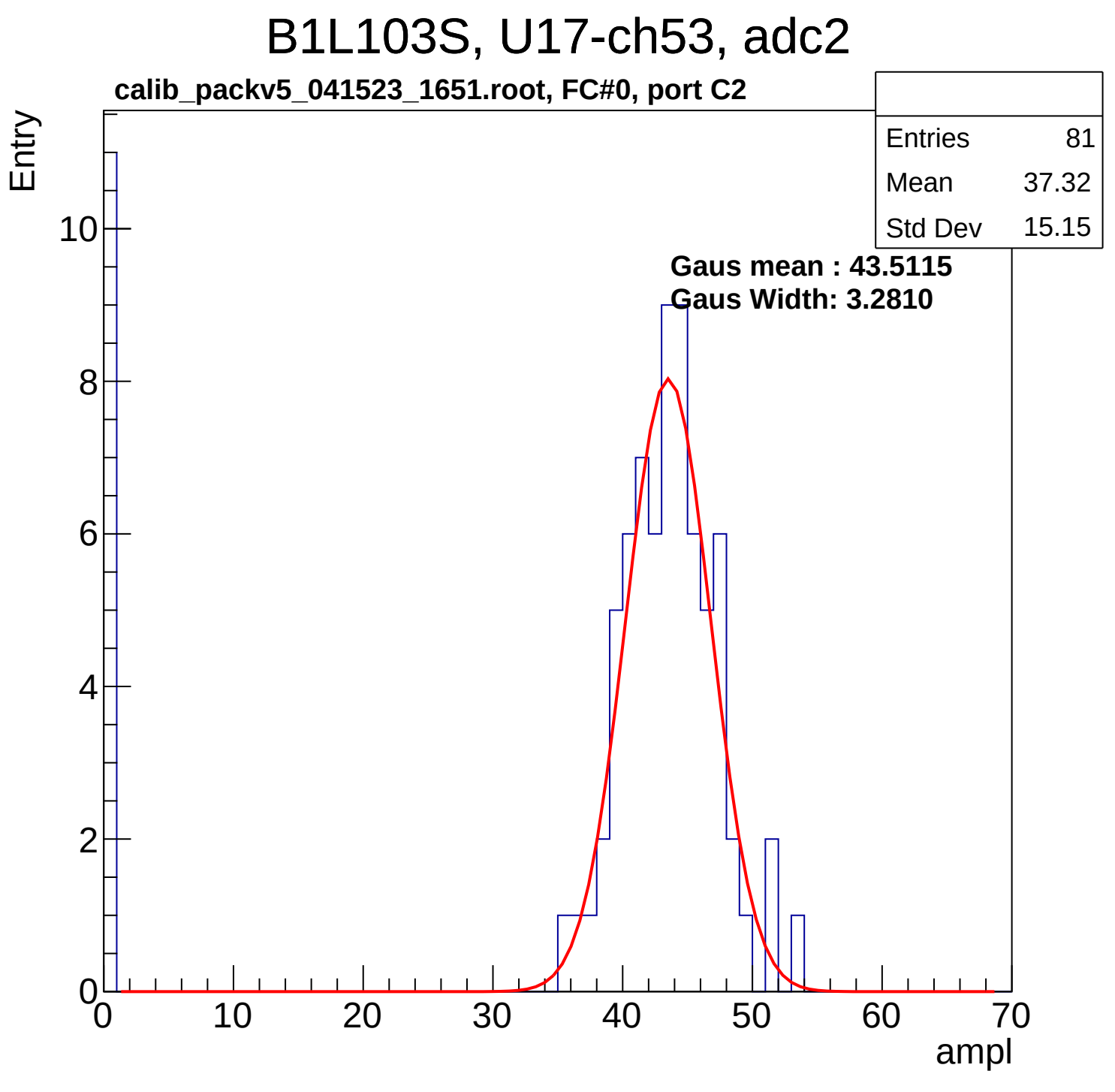

B1L103S, U17-ch52, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 59.3
Std Dev 2.283
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

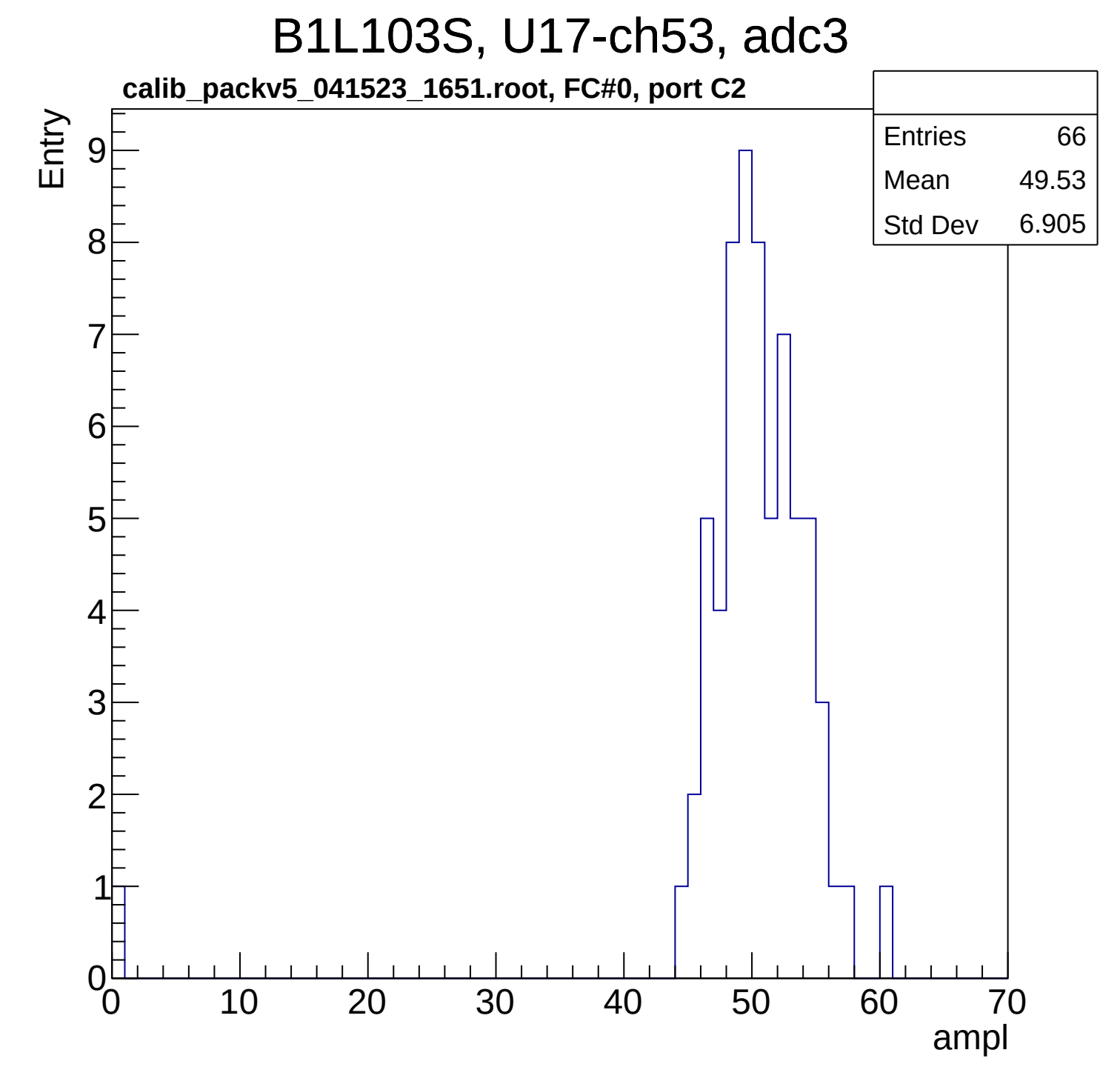

B1L103S, U17-ch52, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 54.5
Std Dev 20.63
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

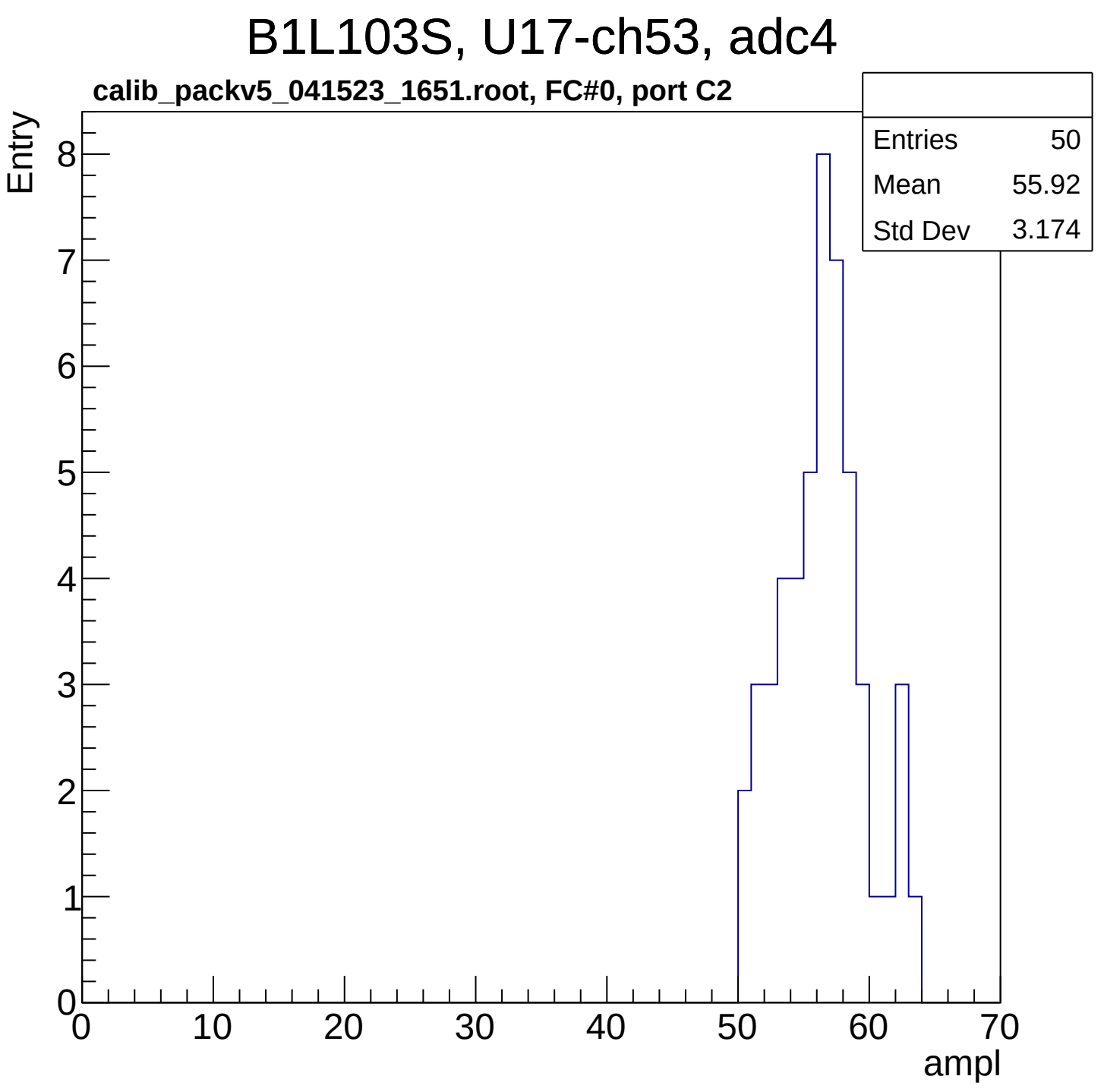

B1L103S, U17-ch52, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

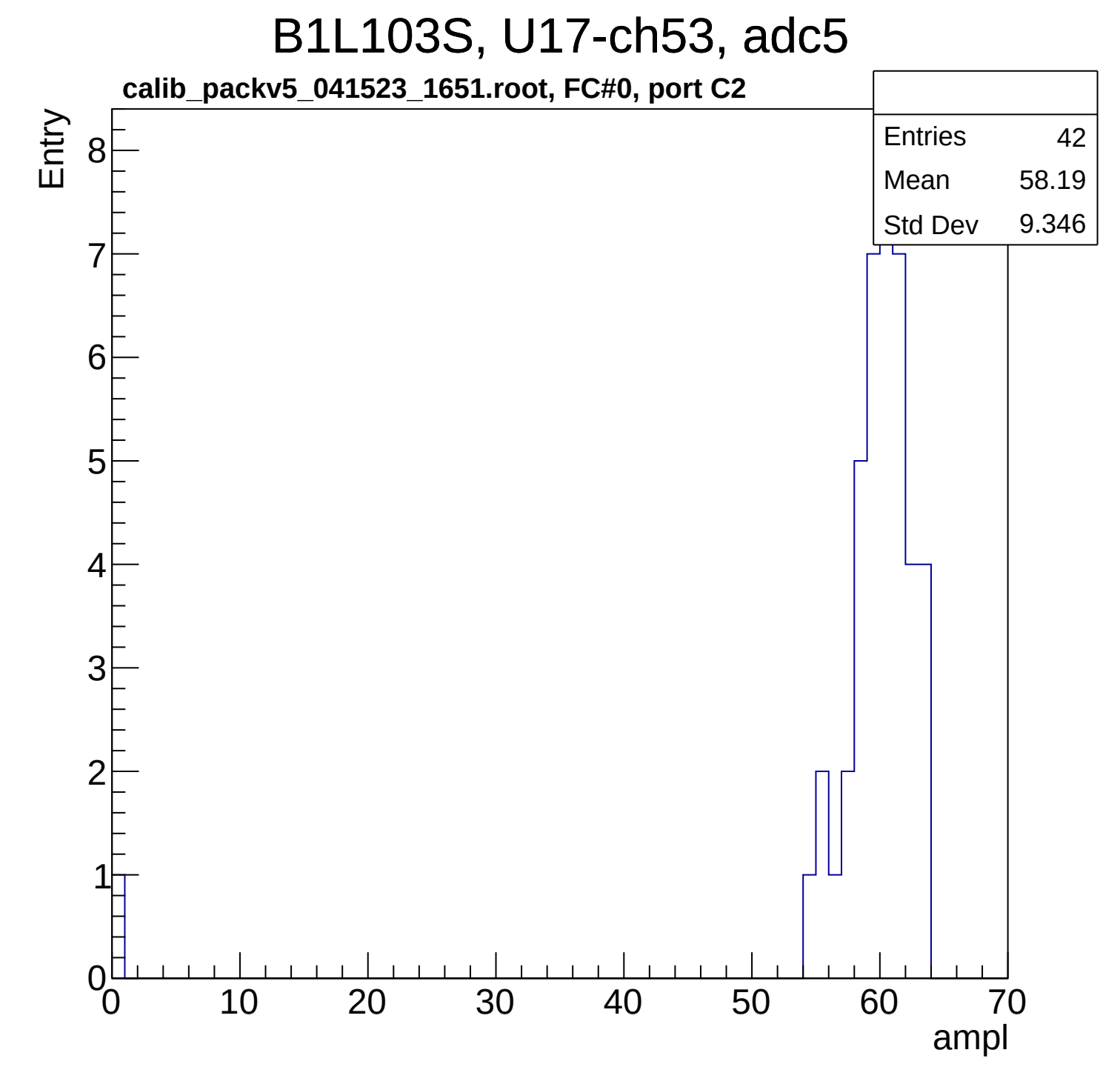

B1L103S, U17-ch53, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 22.87
Std Dev 12.97
Gaus mean : 30.8555
Gaus Width: 3.4199
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

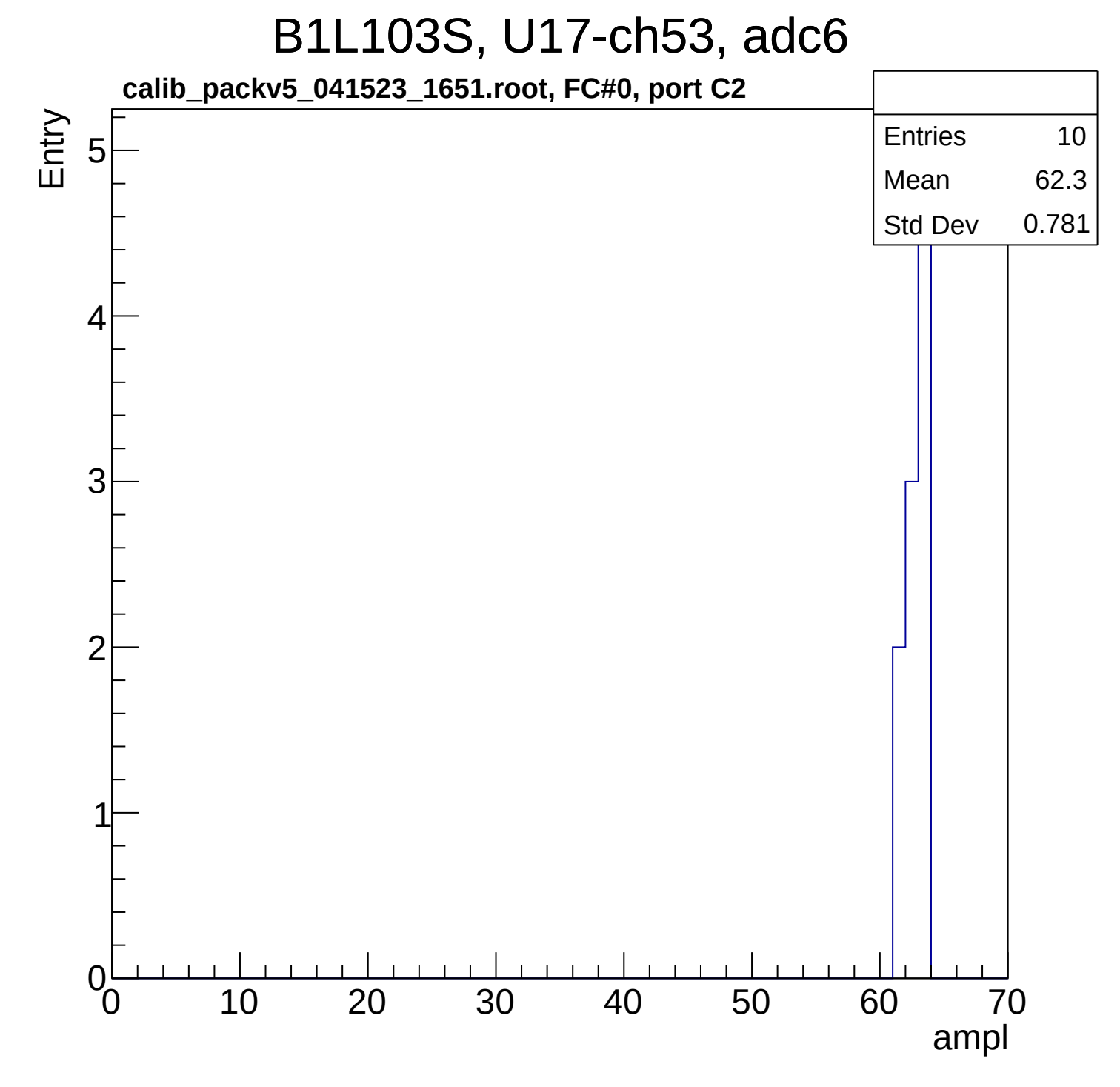

B1L103S, U17-ch53, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 33.22
Std Dev 11.27
Gaus mean : 37.3302
Gaus Width: 3.6010
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

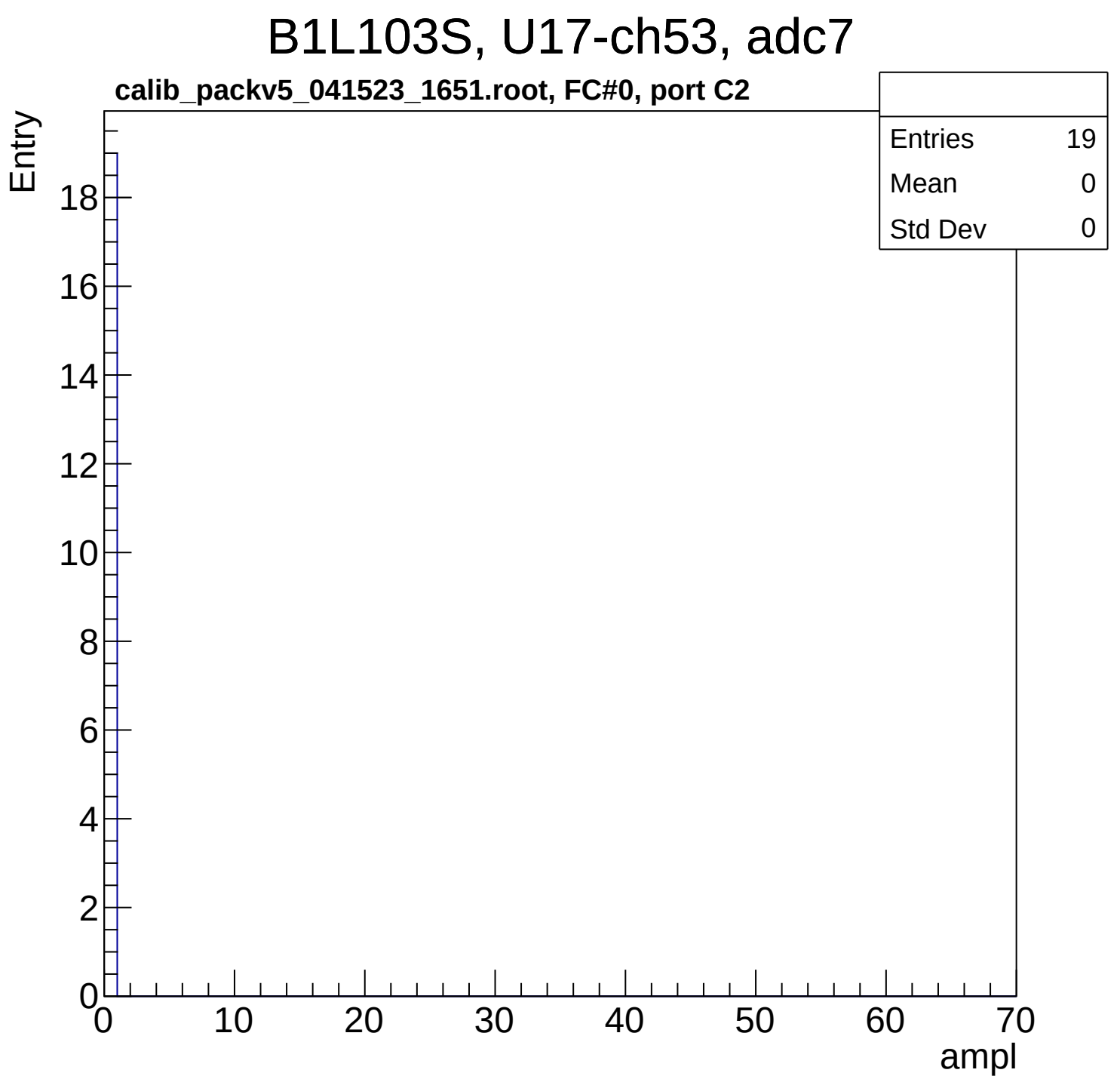

B1L103S, U17-ch53, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 37.32
Std Dev 15.15
Gaus mean : 43.5115
Gaus Width: 3.2810
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

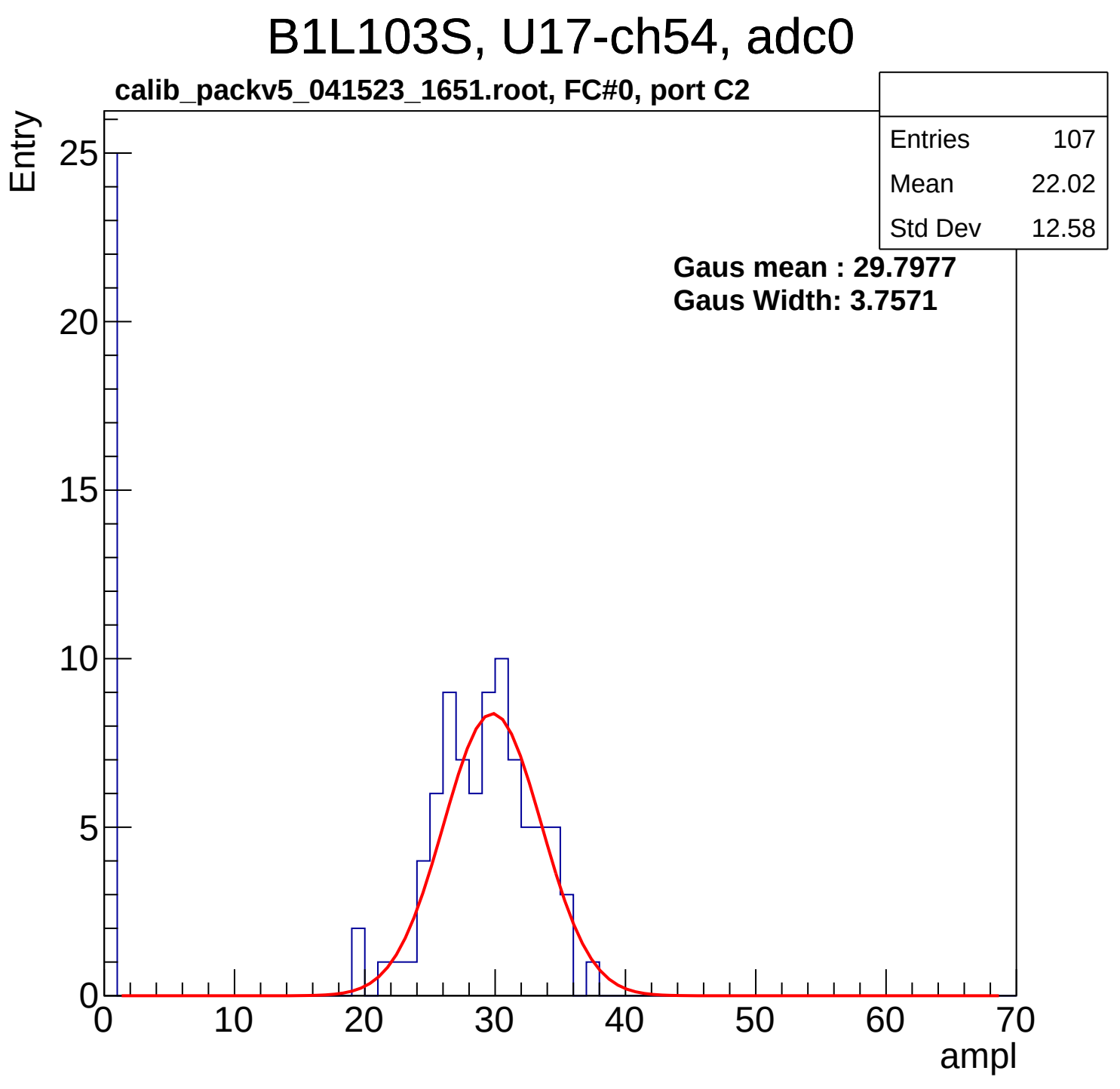

B1L103S, U17-ch53, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 49.53
Std Dev 6.905
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

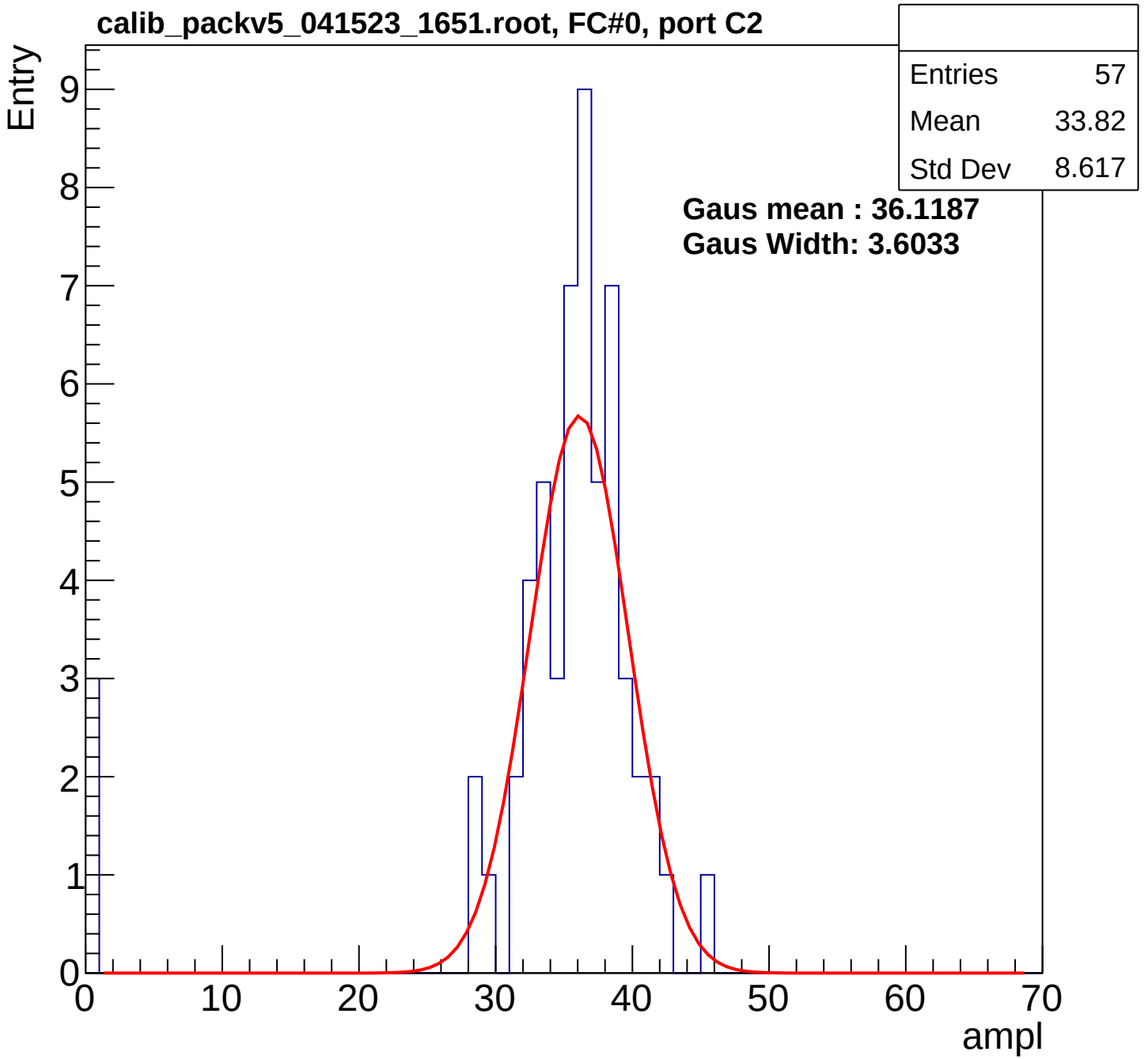

B1L103S, U17-ch53, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 55.92
Std Dev 3.174
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

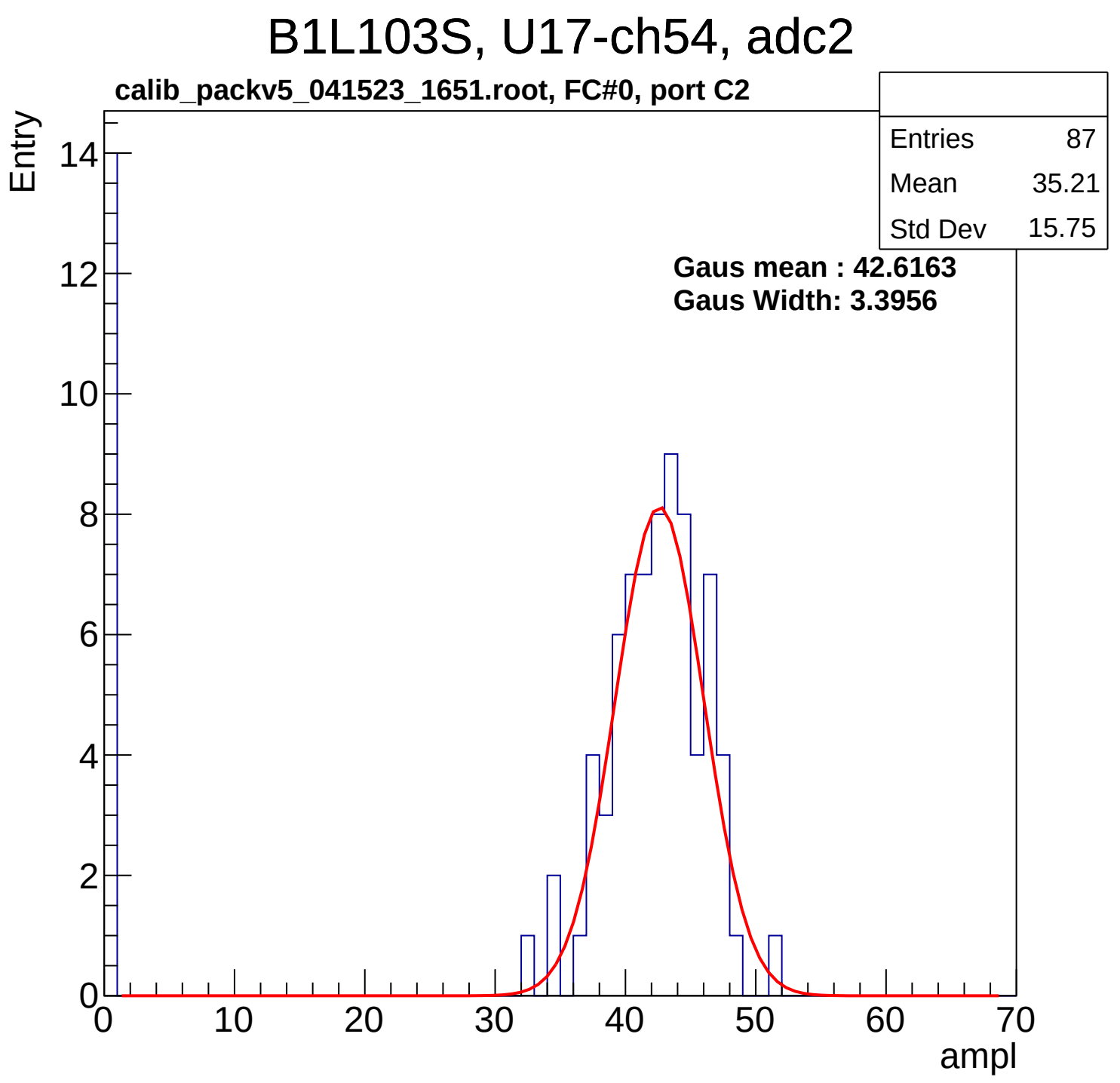

B1L103S, U17-ch53, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 58.19
Std Dev 9.346
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

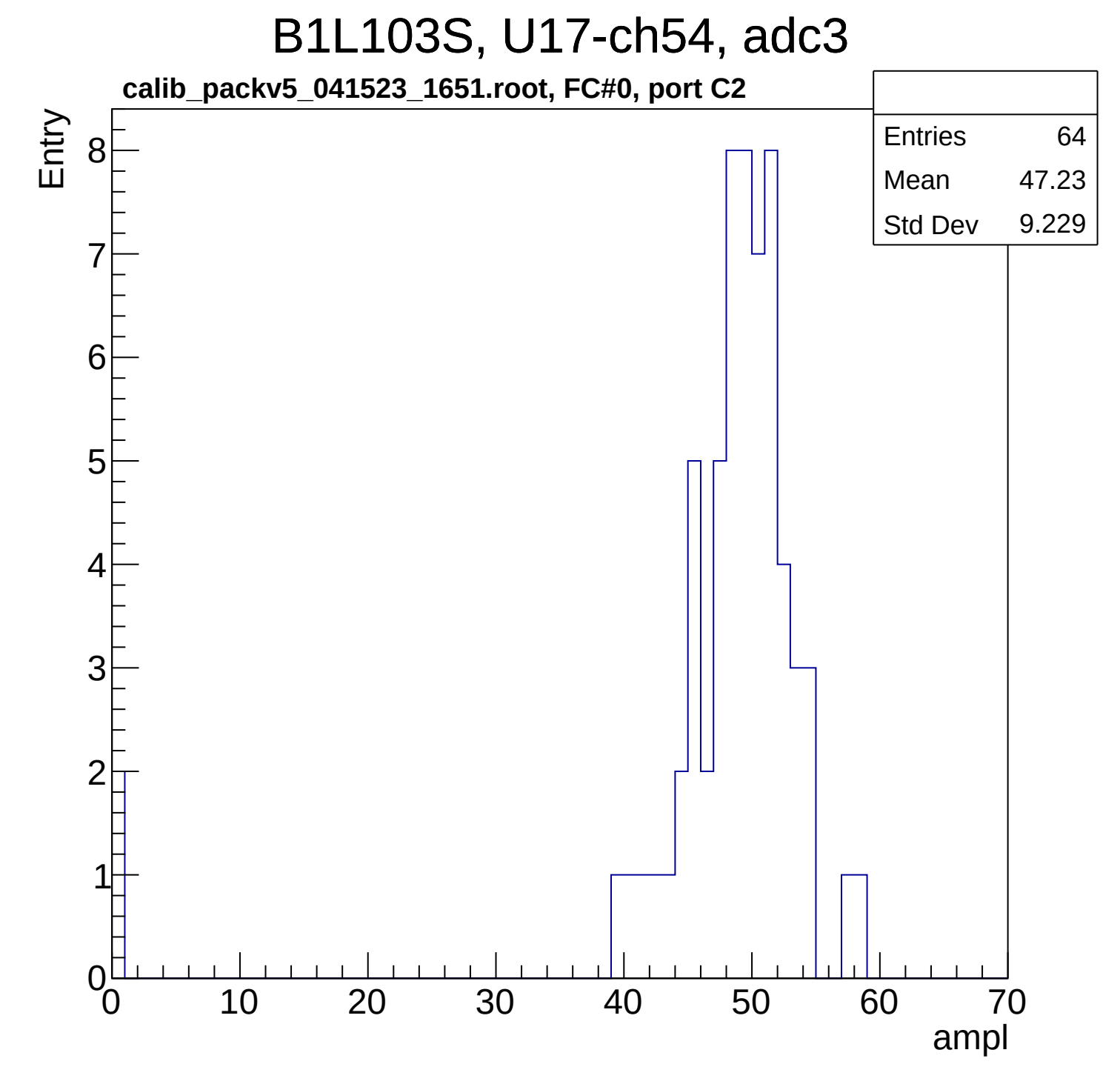

B1L103S, U17-ch53, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 62.3
Std Dev 0.781
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

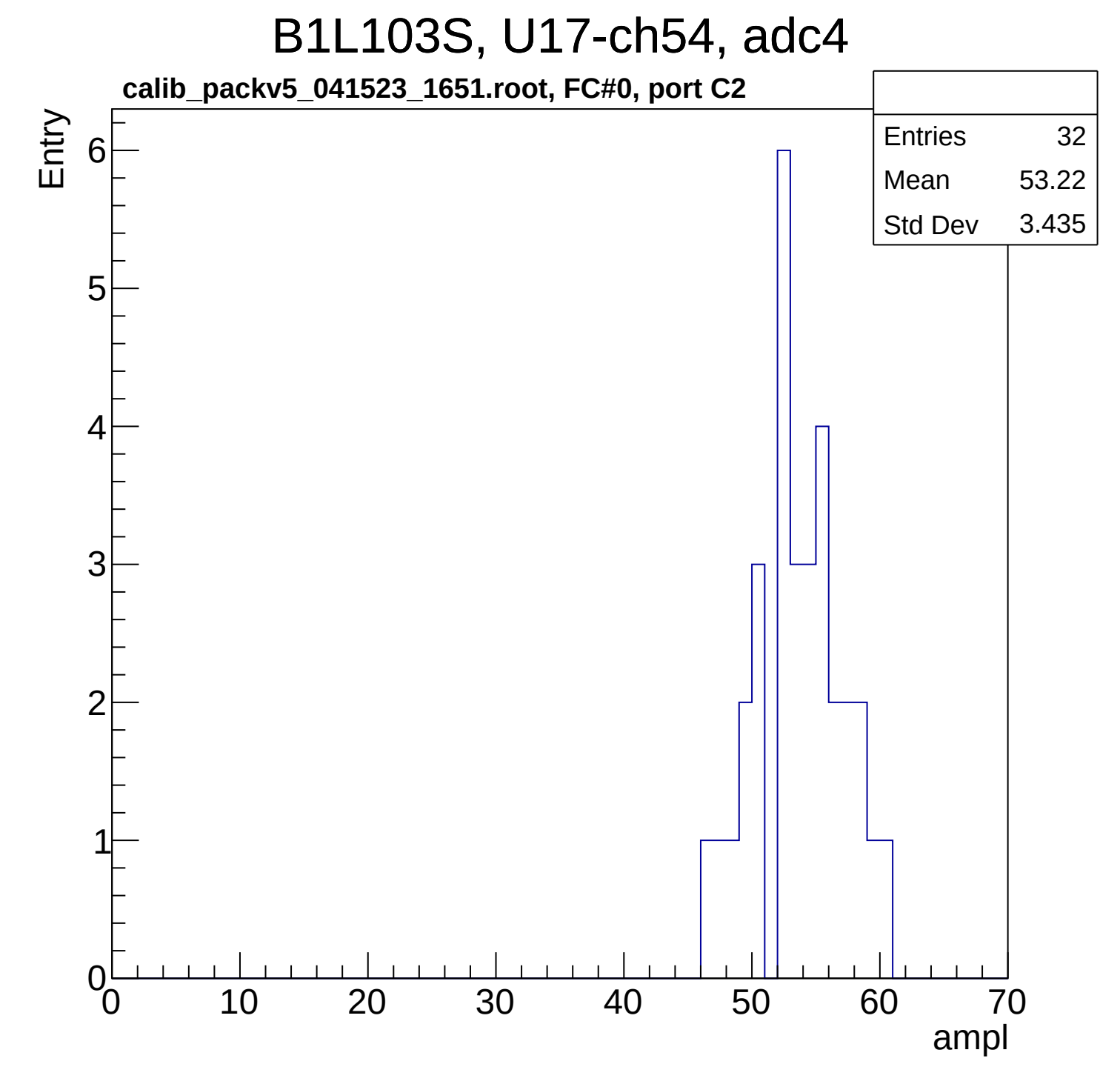

B1L103S, U17-ch53, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

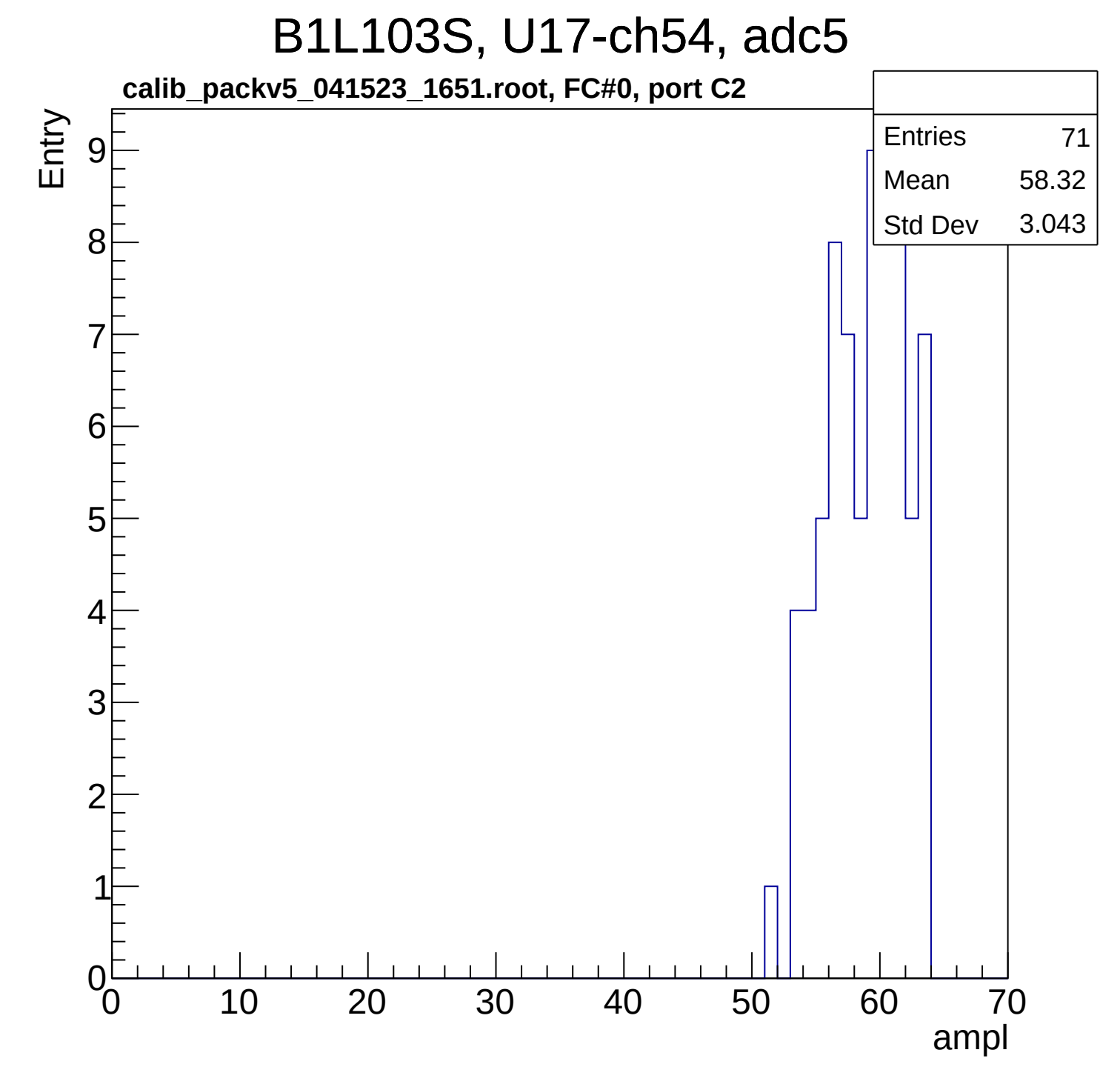

B1L103S, U17-ch54, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 107
Mean 22.02
Std Dev 12.58
Gaus mean : 29.7977
Gaus Width: 3.7571
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70

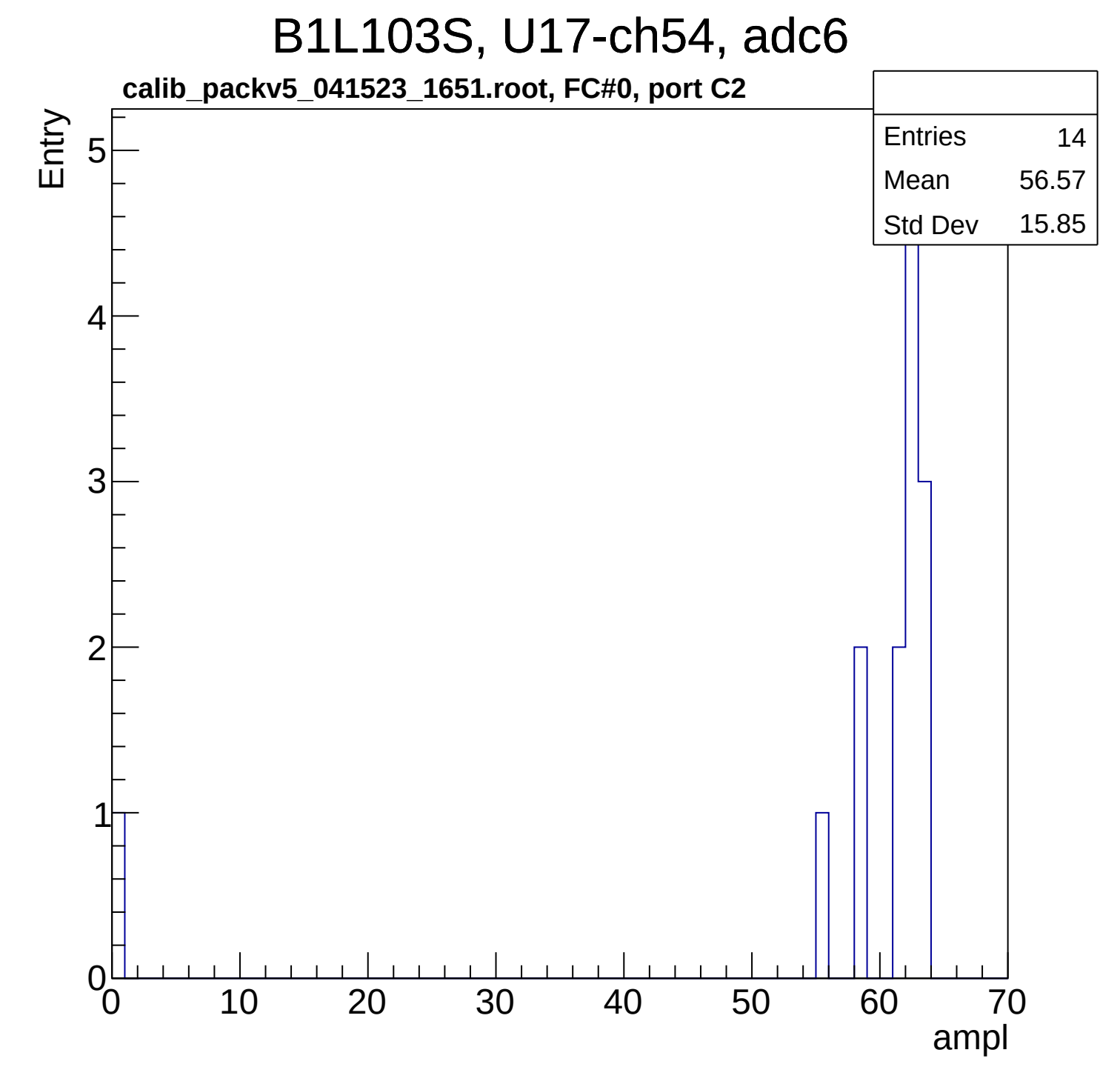

B1L103S, U17-ch54, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 33.82
Std Dev 8.617
Gaus mean : 36.1187
Gaus Width: 3.6033
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

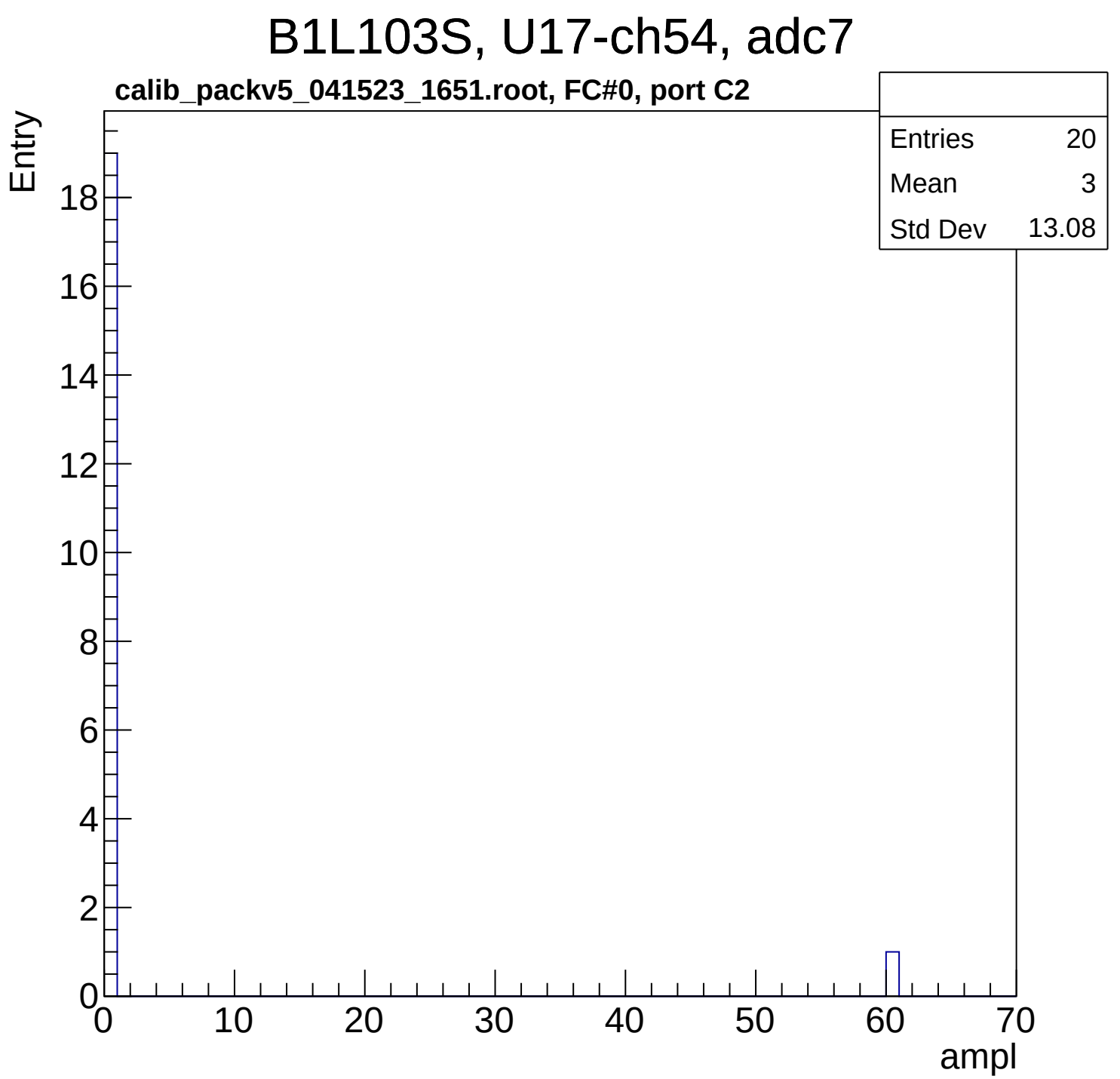

B1L103S, U17-ch54, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 35.21
Std Dev 15.75
Gaus mean : 42.6163
Gaus Width: 3.3956
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

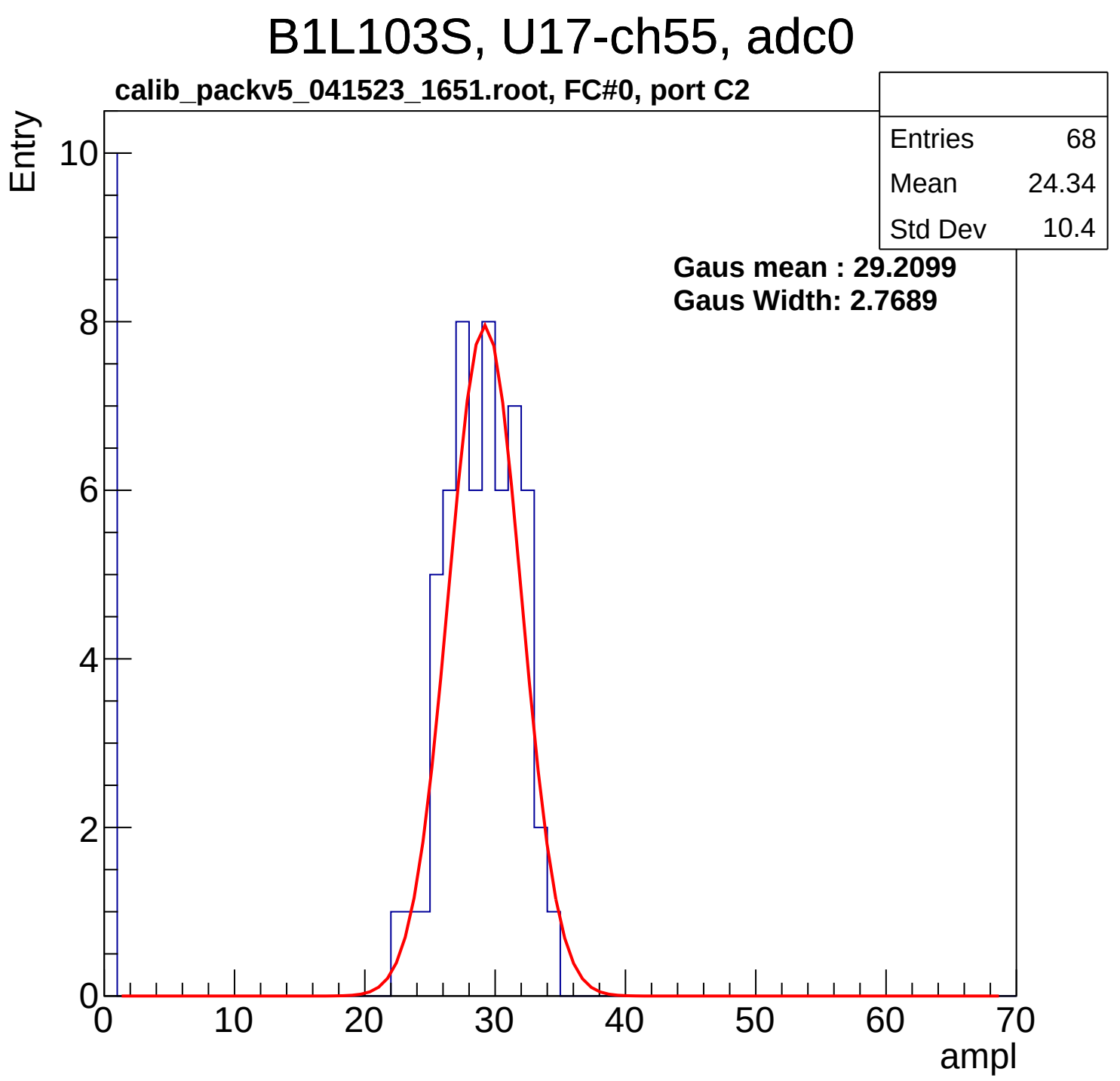

B1L103S, U17-ch54, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 47.23
Std Dev 9.229
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

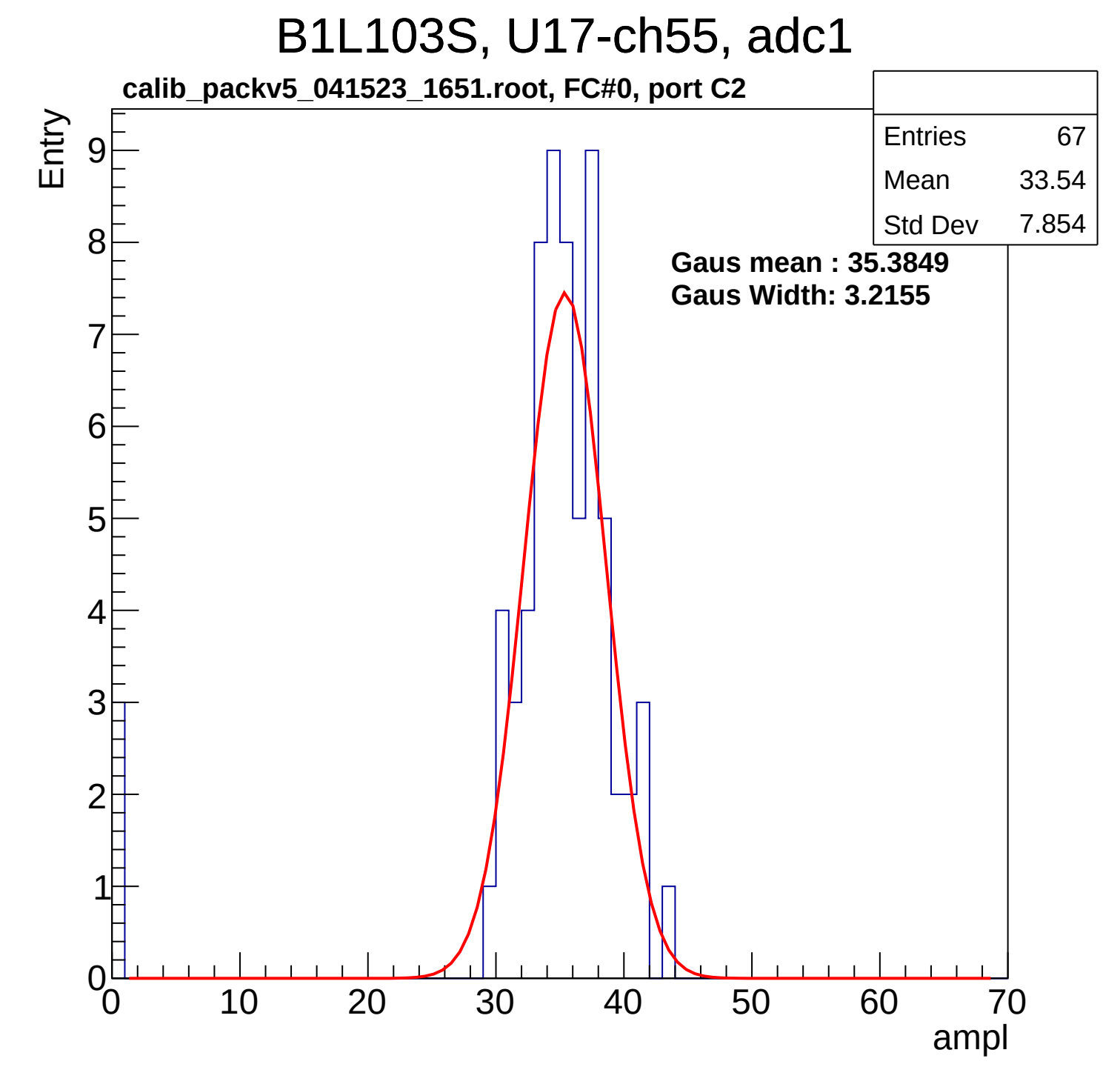

B1L103S, U17-ch54, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 53.22
Std Dev 3.435
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

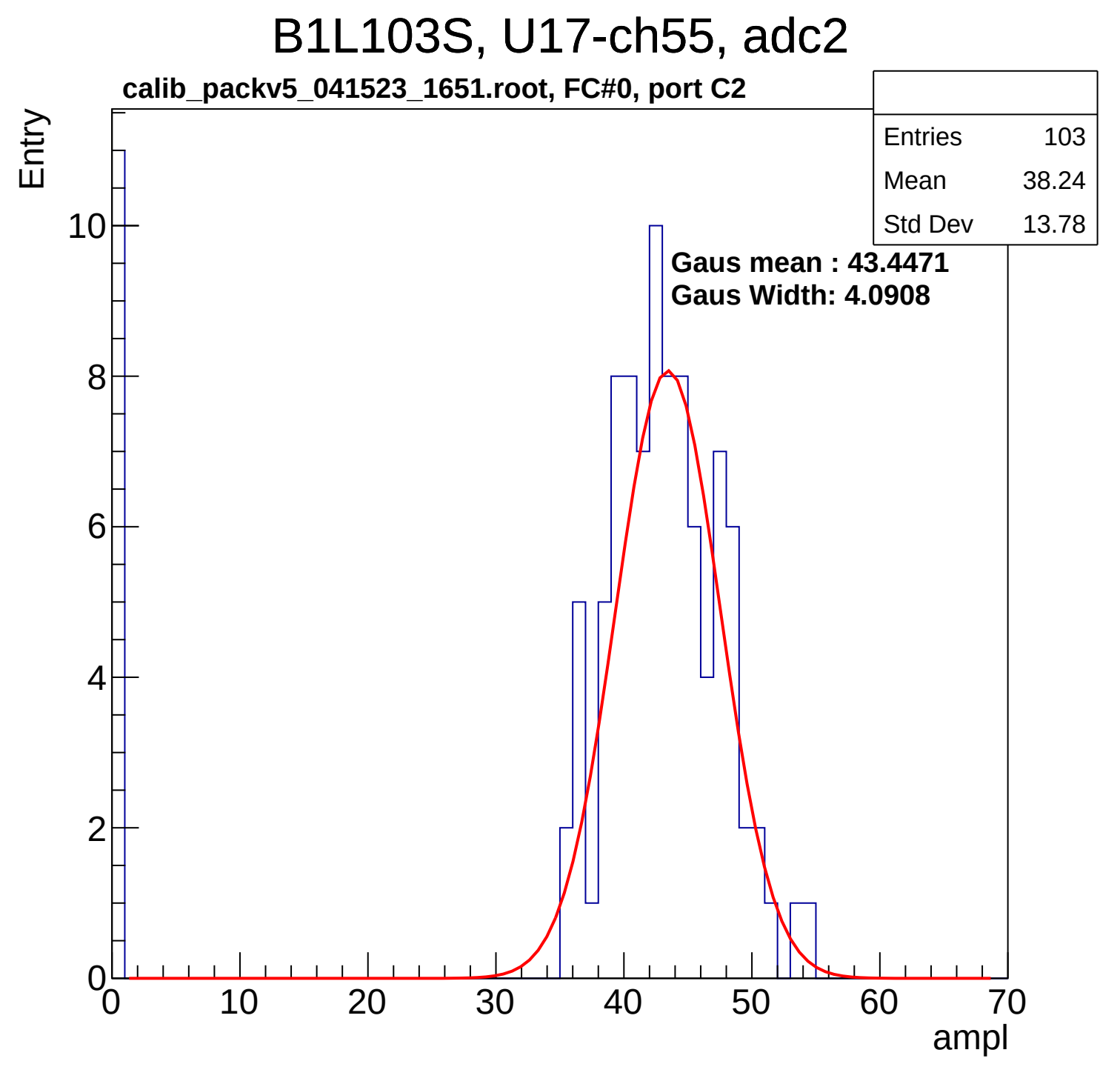

B1L103S, U17-ch54, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 58.32
Std Dev 3.043
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

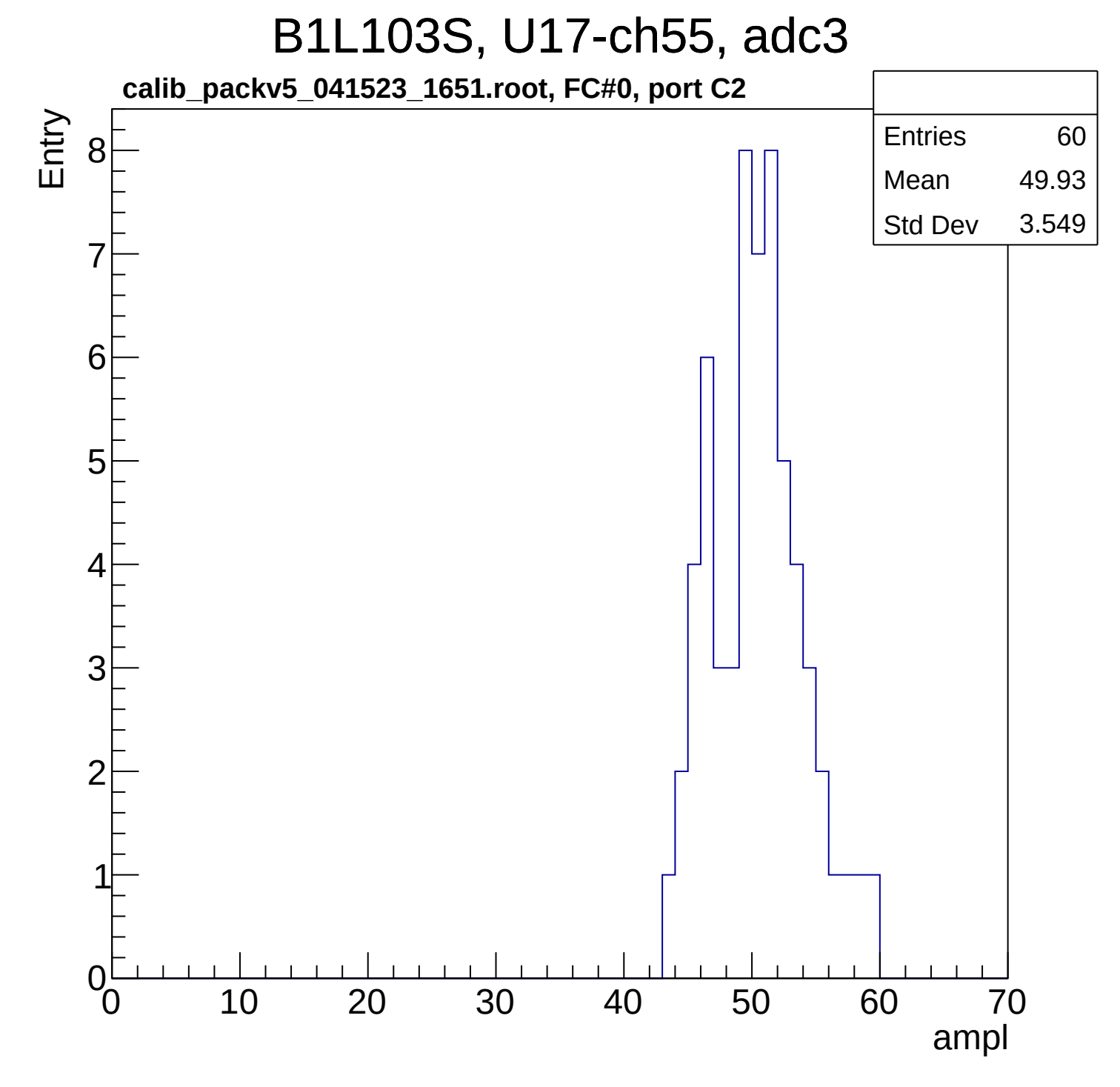

B1L103S, U17-ch54, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 56.57
Std Dev 15.85
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

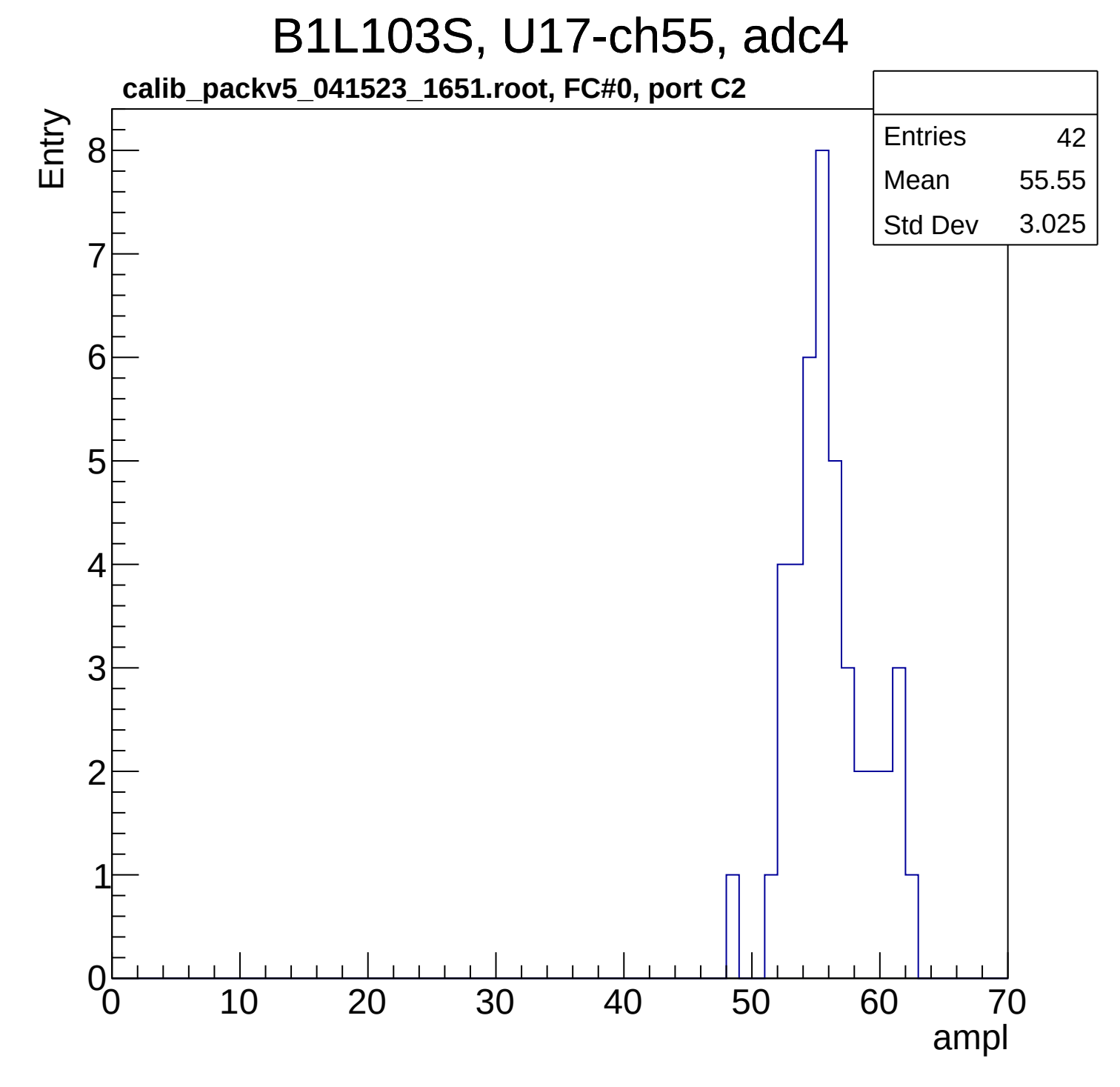

B1L103S, U17-ch54, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3
Std Dev 13.08
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

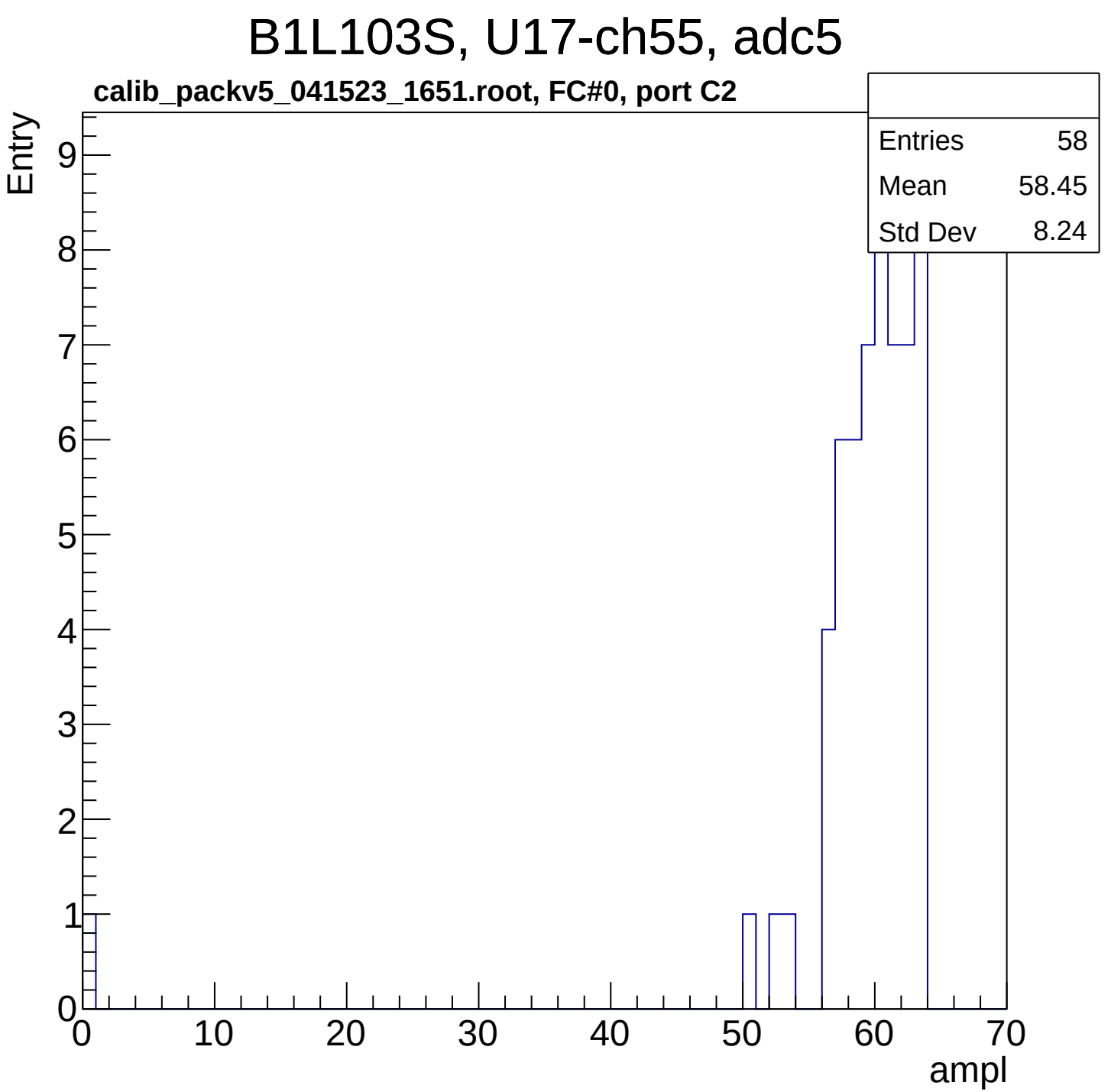

B1L103S, U17-ch55, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 24.34
Std Dev 10.4
Gaus mean : 29.2099
Gaus Width: 2.7689
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

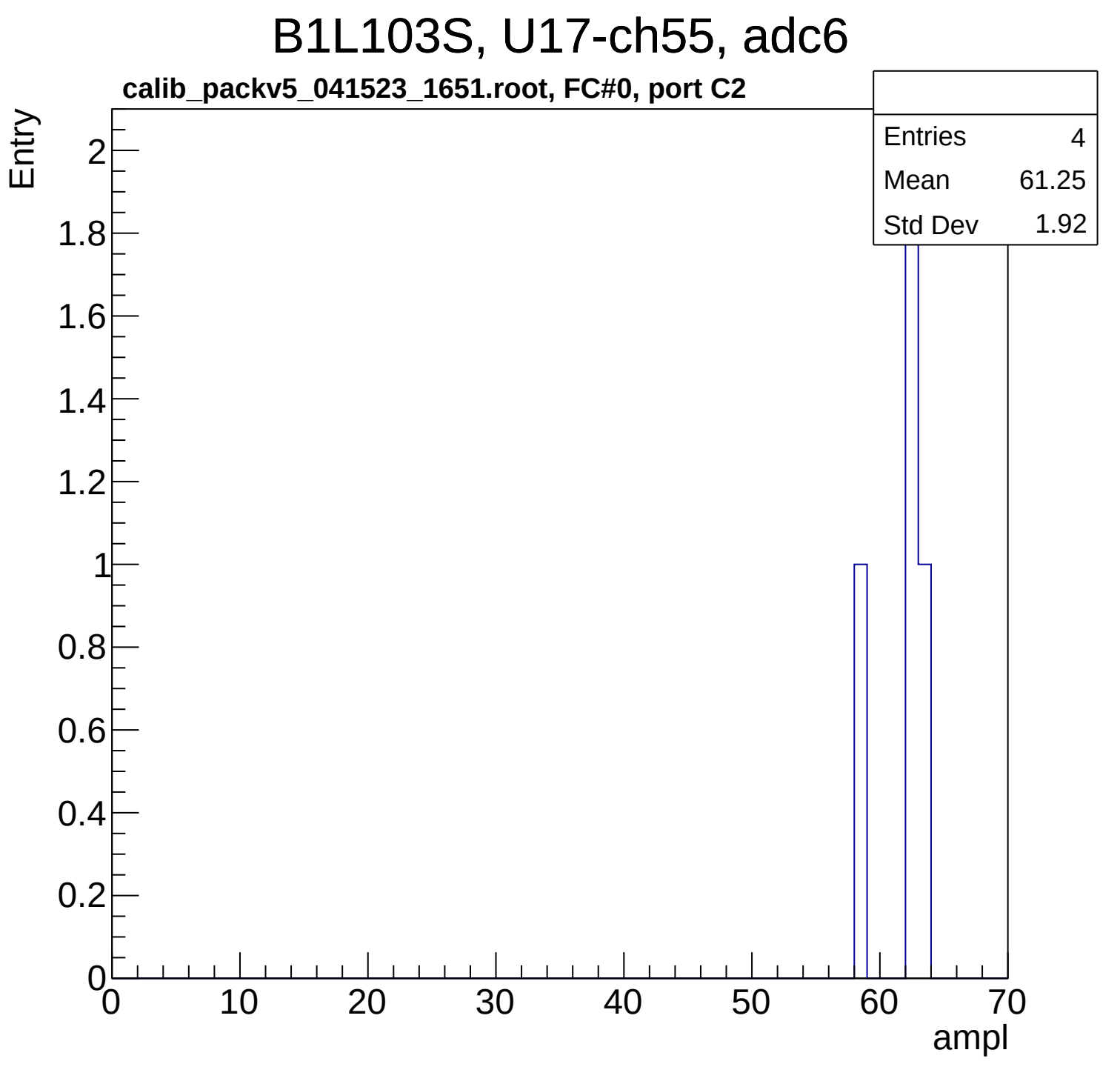

B1L103S, U17-ch55, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 33.54
Std Dev 7.854
Gaus mean : 35.3849
Gaus Width: 3.2155
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

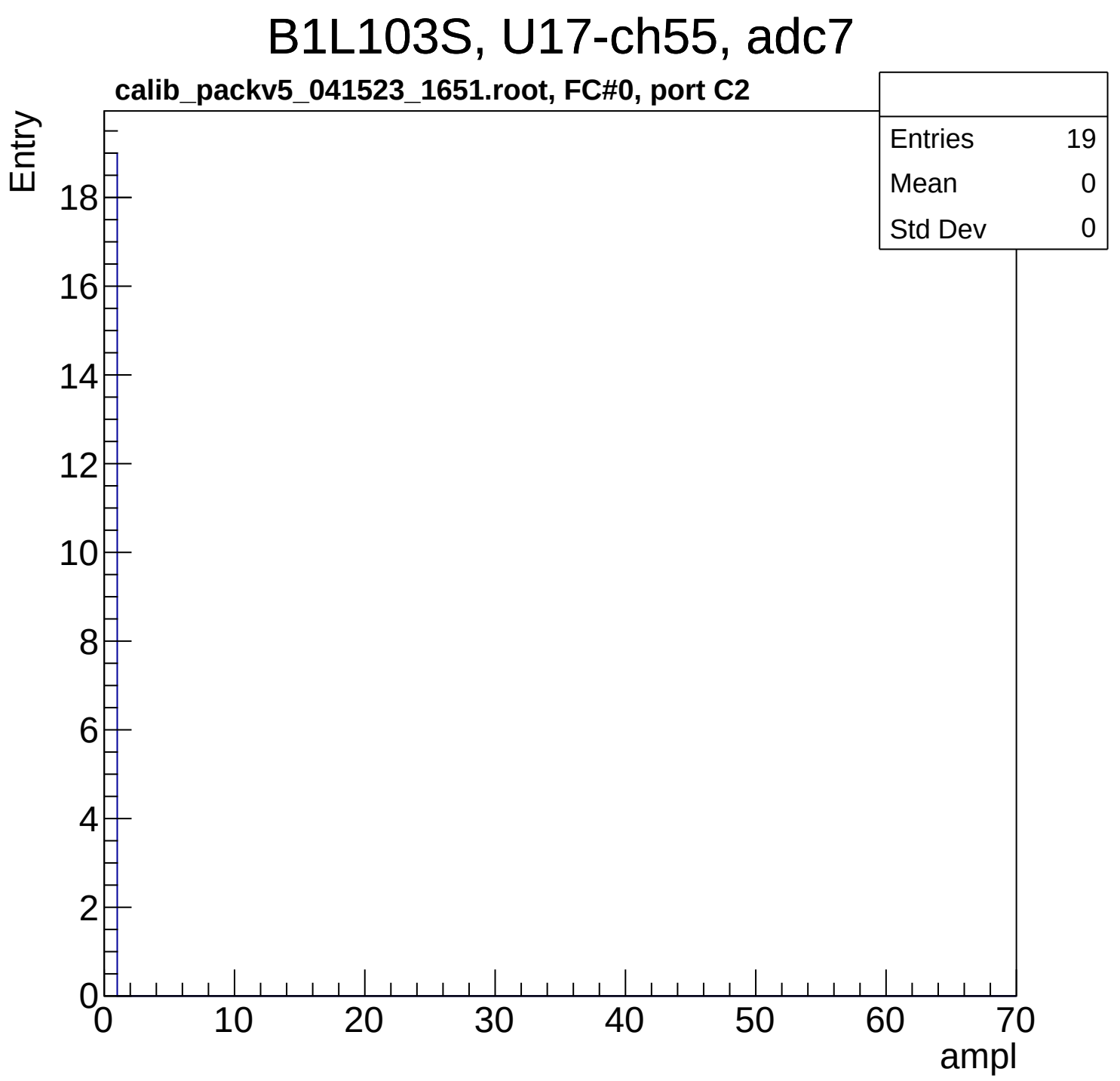

B1L103S, U17-ch55, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 38.24
Std Dev 13.78
Gaus mean : 43.4471
Gaus Width: 4.0908
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

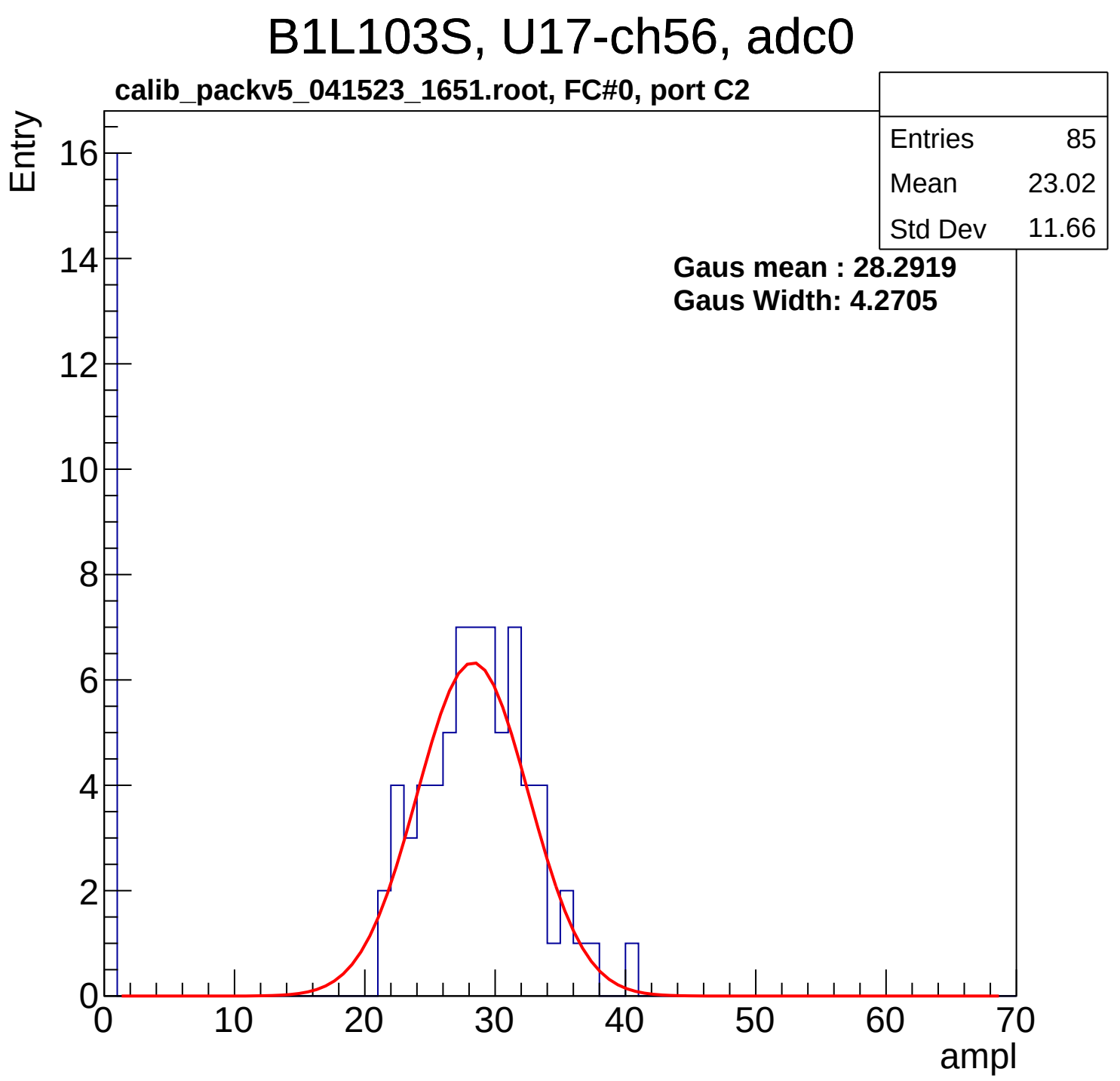

B1L103S, U17-ch55, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 49.93
Std Dev 3.549
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

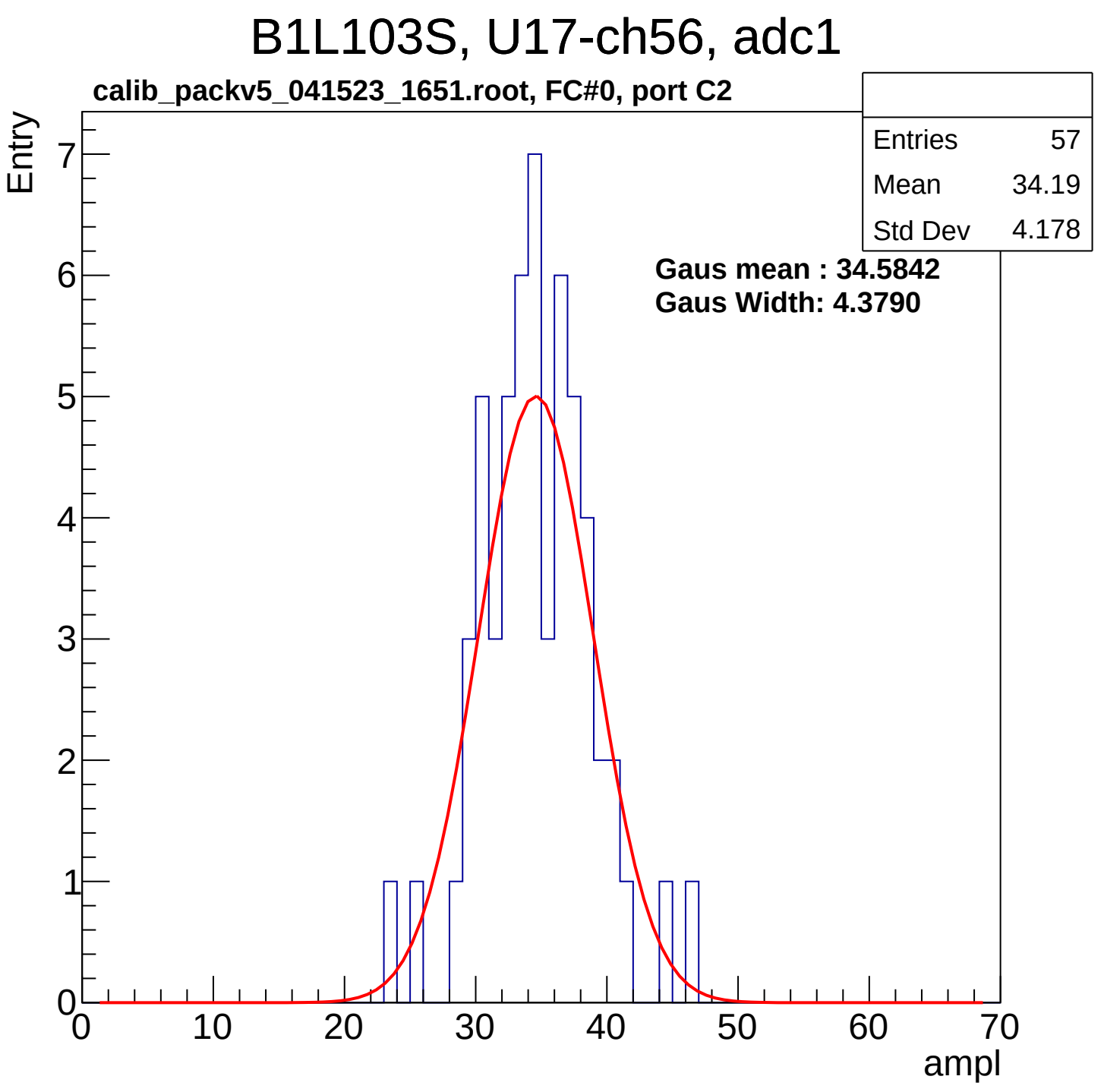

B1L103S, U17-ch55, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 55.55
Std Dev 3.025
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

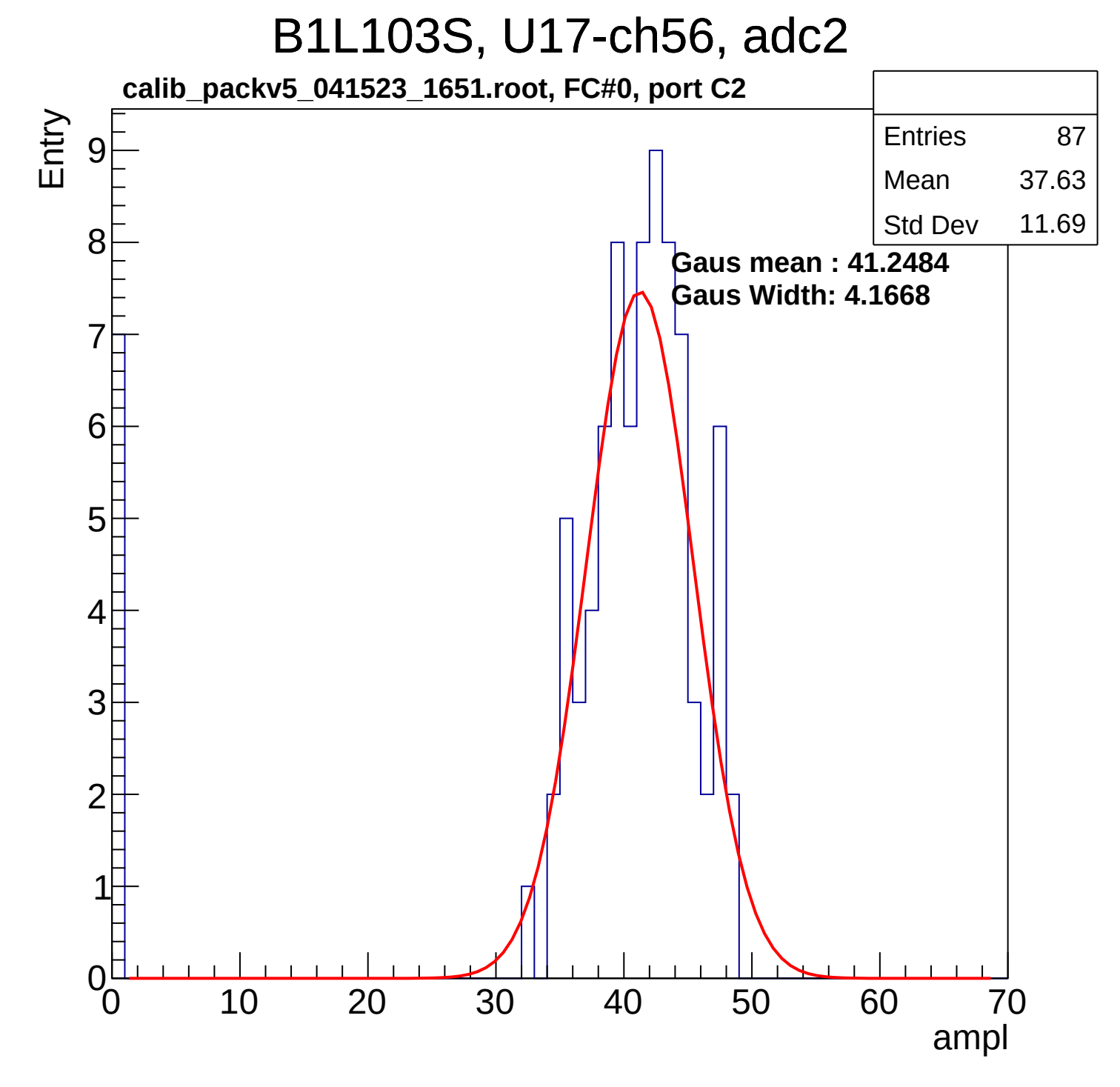

B1L103S, U17-ch55, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.45
Std Dev 8.24
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

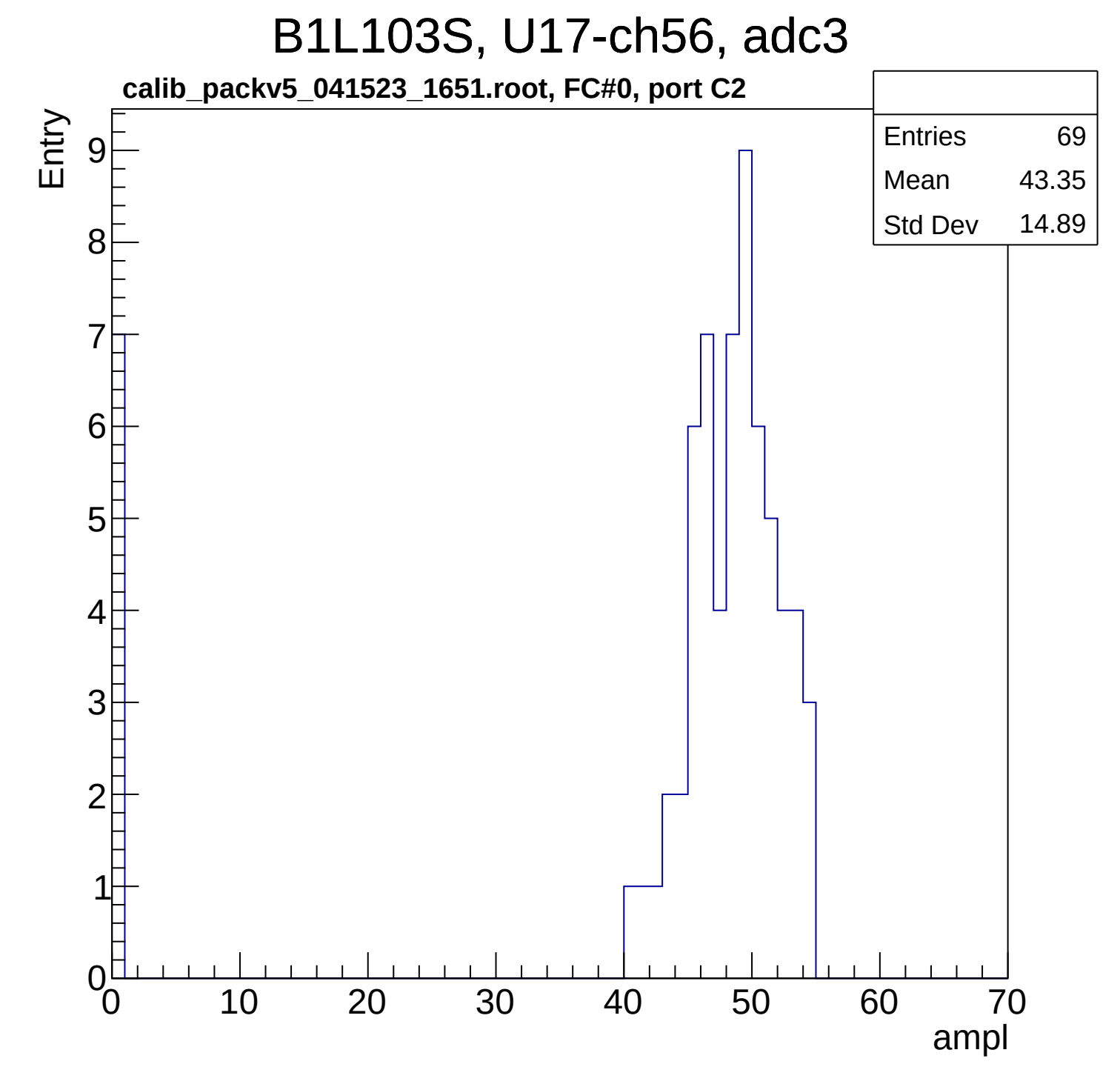

B1L103S, U17-ch55, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61.25
Std Dev 1.92
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

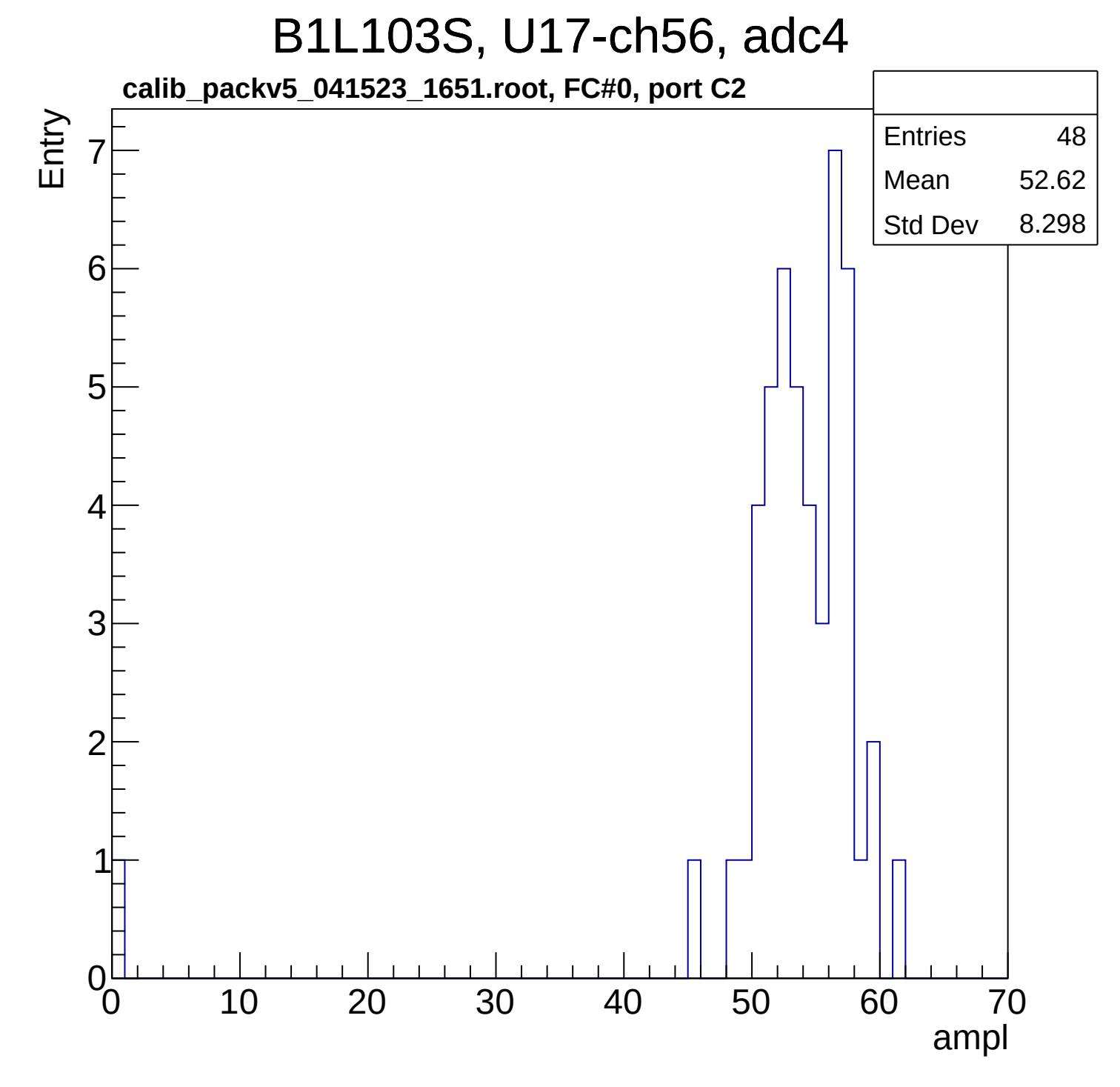

B1L103S, U17-ch55, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

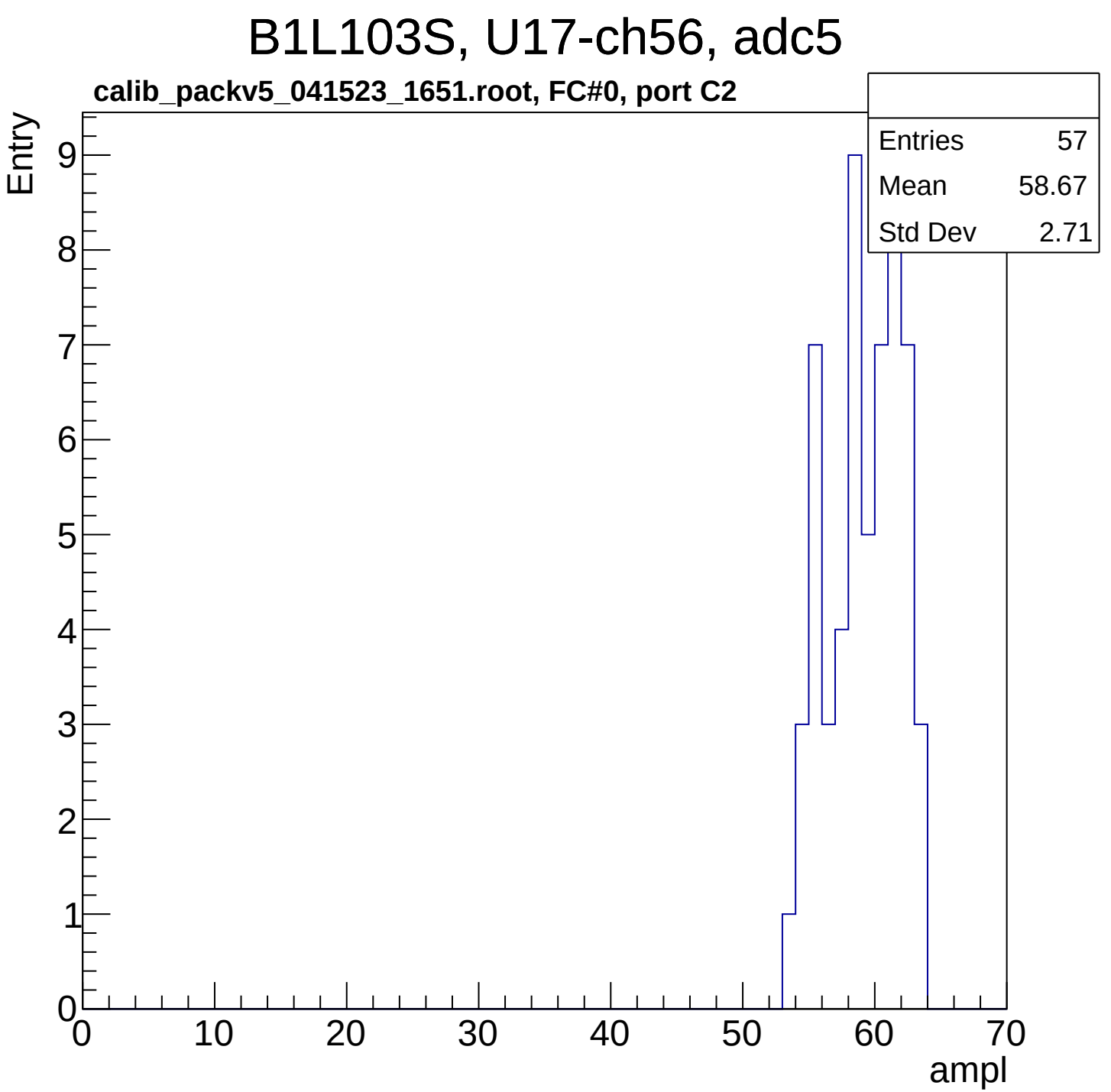

B1L103S, U17-ch56, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 23.02
Std Dev 11.66
Gaus mean : 28.2919
Gaus Width: 4.2705
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

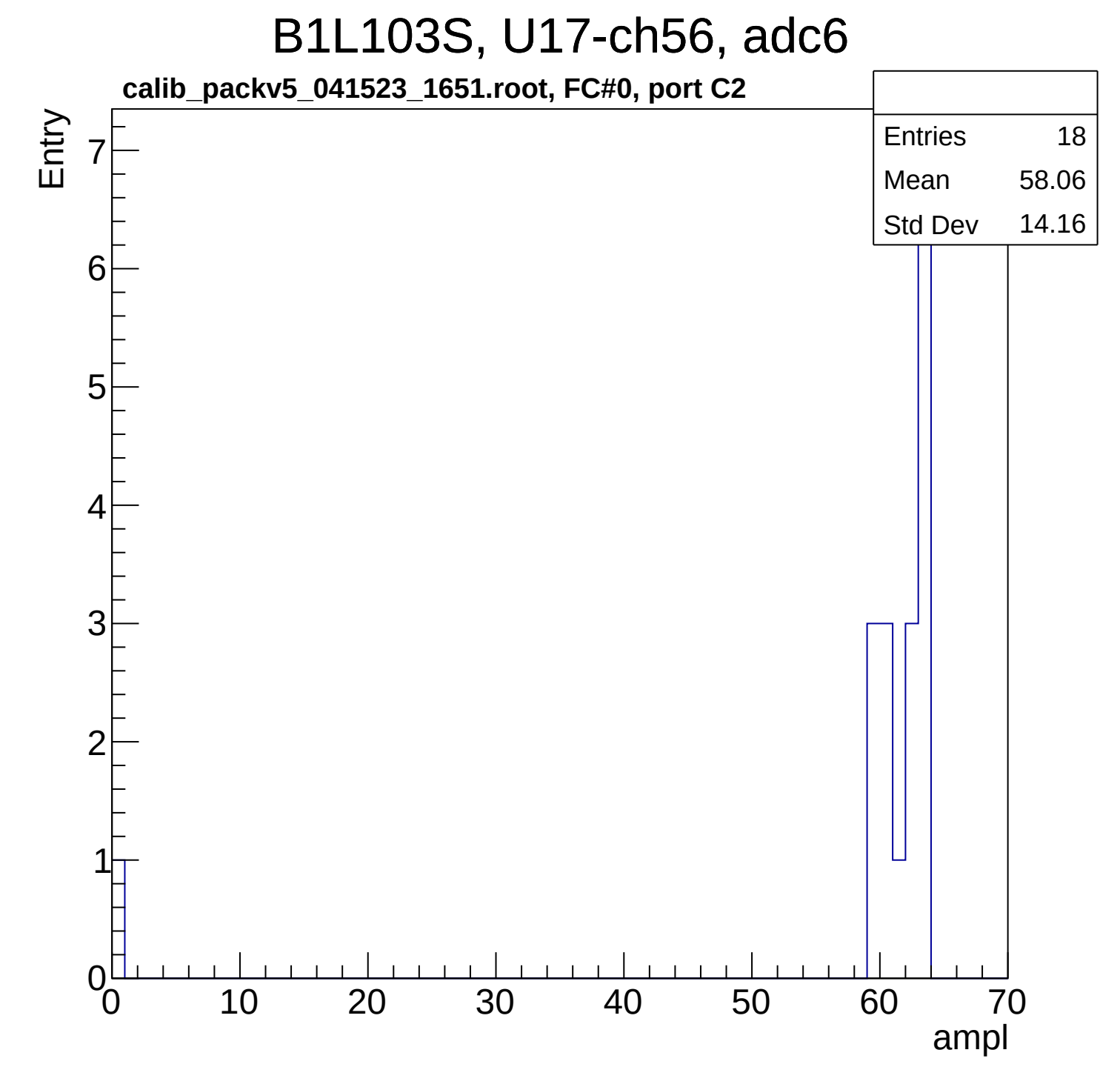

B1L103S, U17-ch56, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 34.19
Std Dev 4.178
Gaus mean : 34.5842
Gaus Width: 4.3790
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

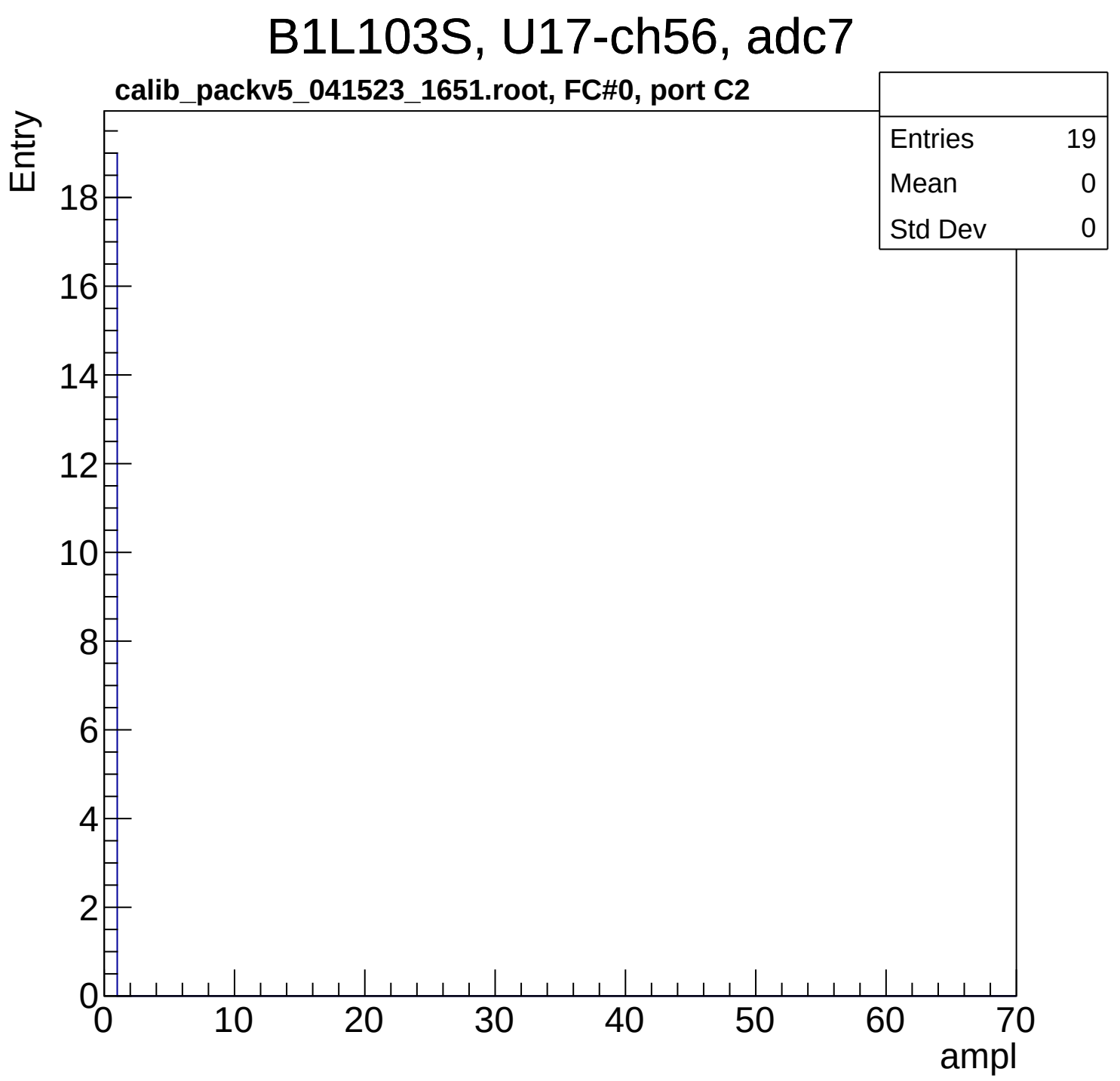

B1L103S, U17-ch56, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 37.63
Std Dev 11.69
Gaus mean : 41.2484
Gaus Width: 4.1668
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

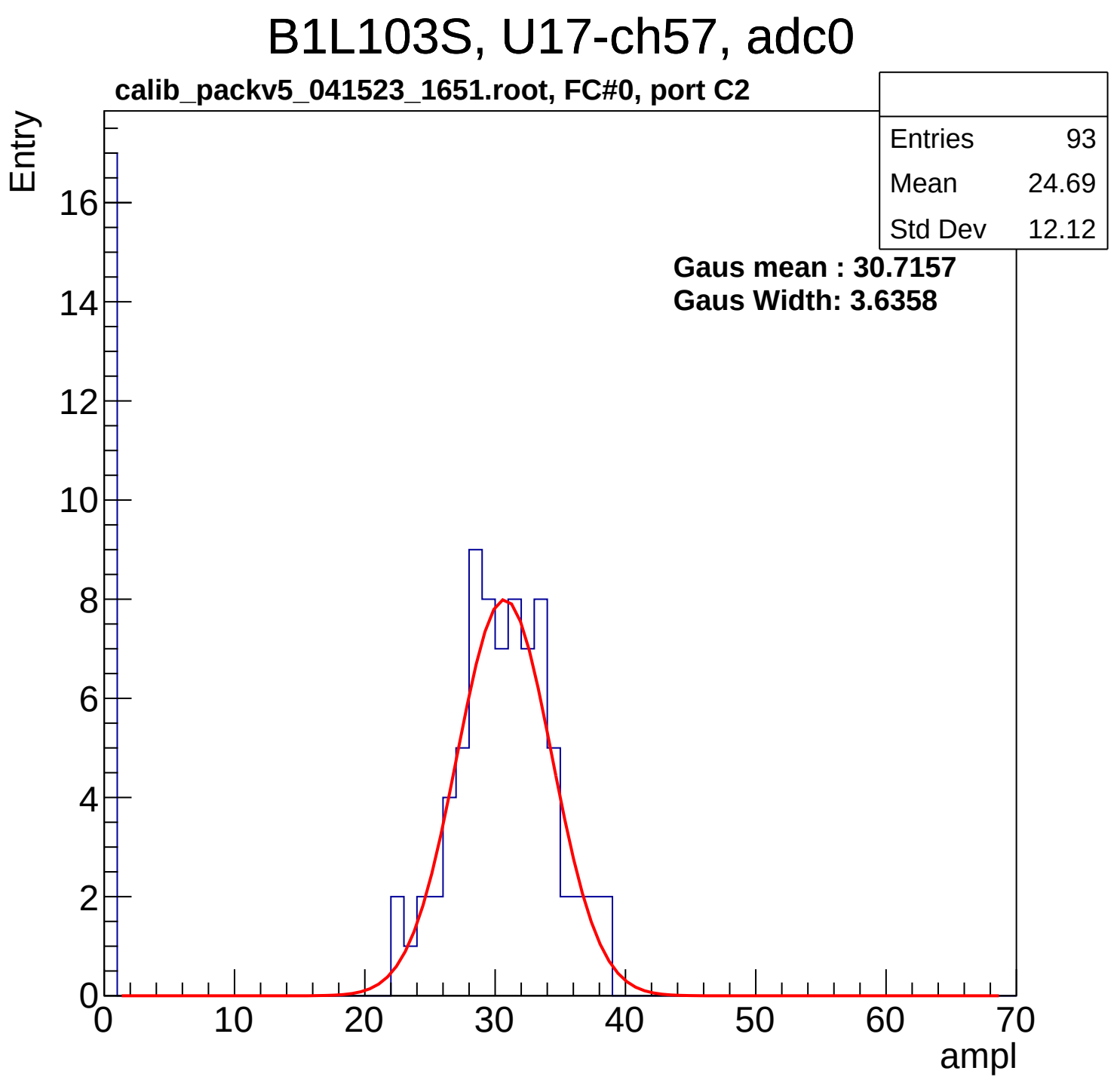

B1L103S, U17-ch56, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 43.35
Std Dev 14.89
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

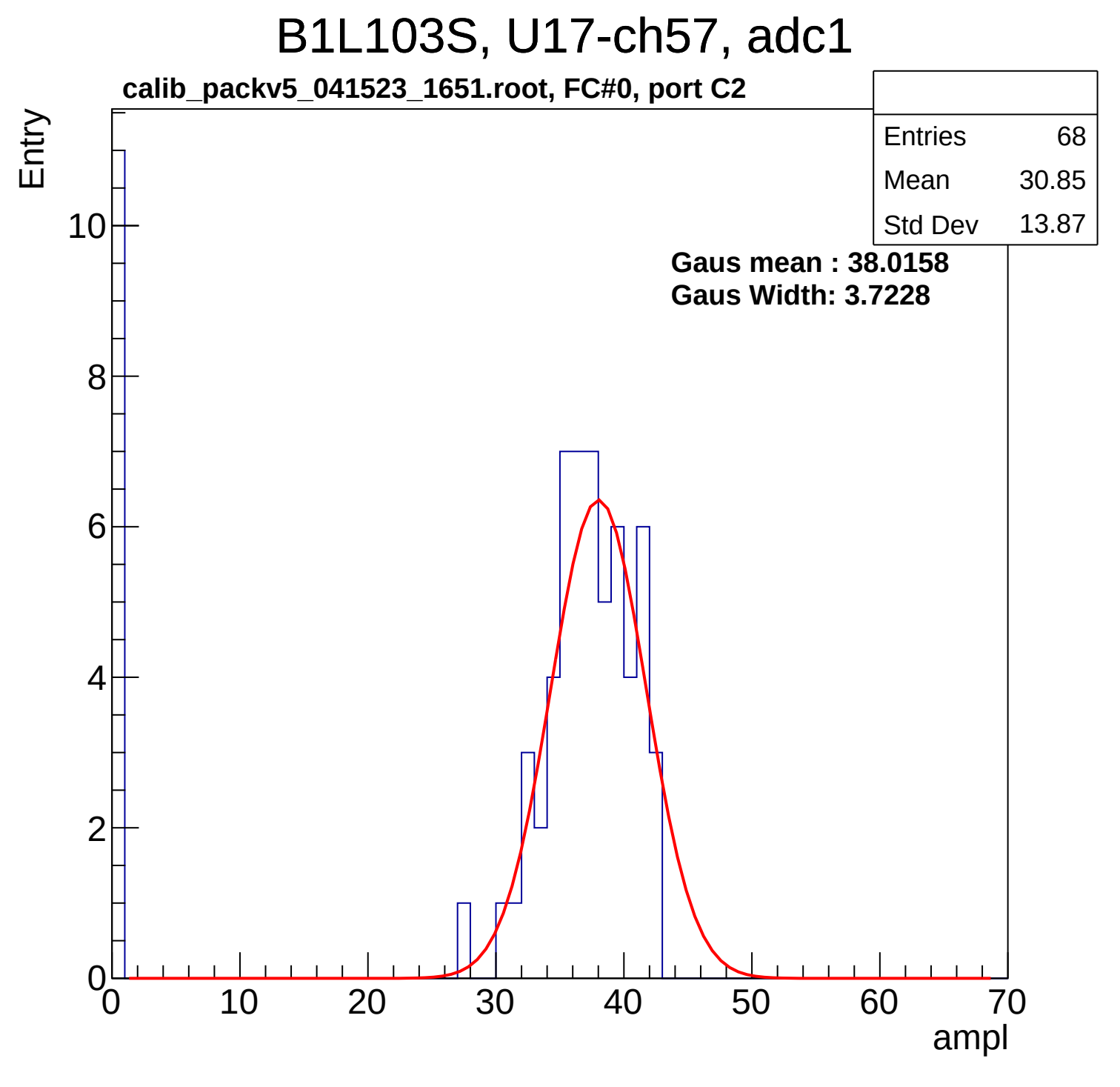

B1L103S, U17-ch56, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 52.62
Std Dev 8.298
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

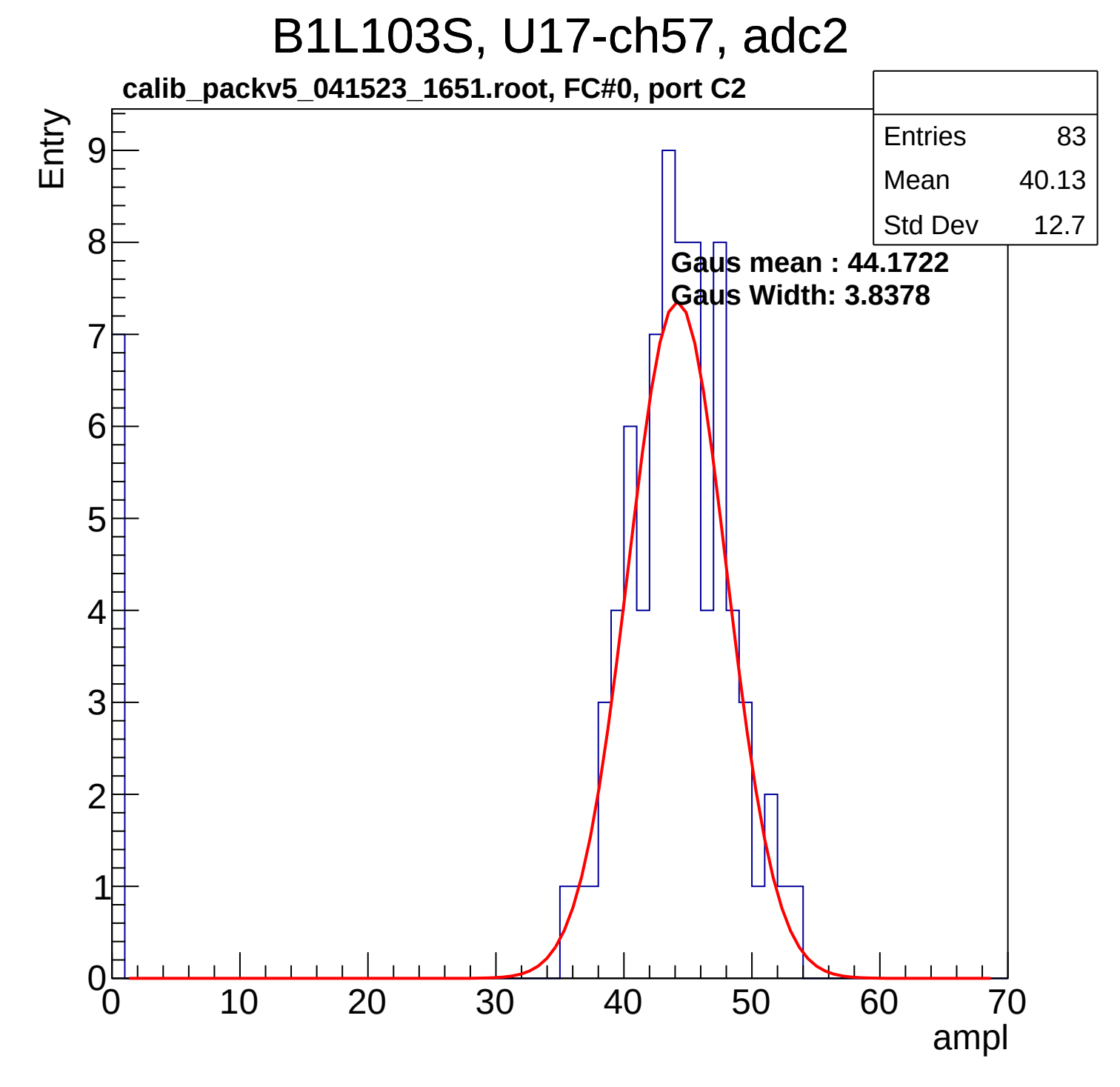

B1L103S, U17-ch56, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.67
Std Dev 2.71
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

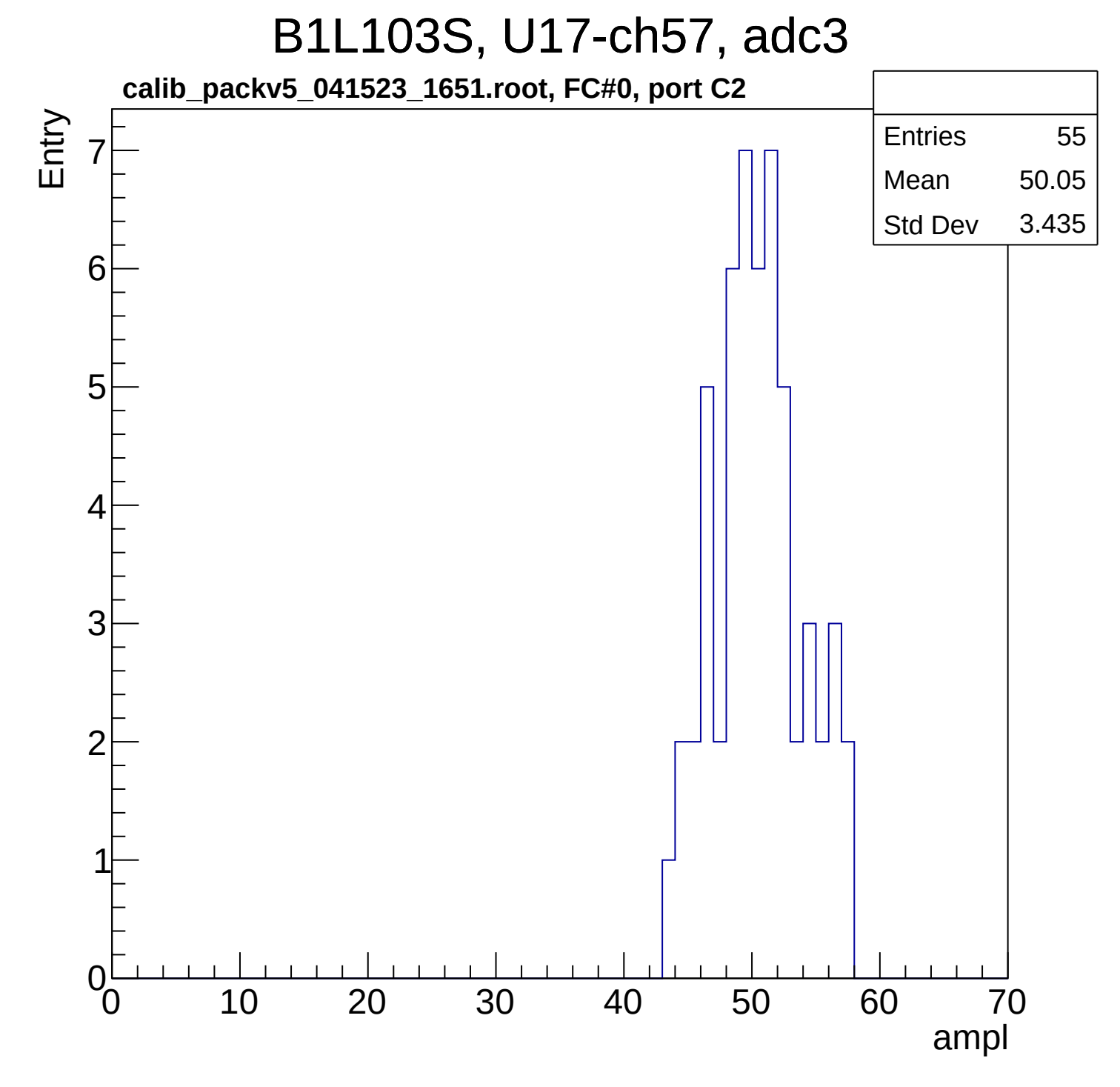

B1L103S, U17-ch56, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 58.06
Std Dev 14.16
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

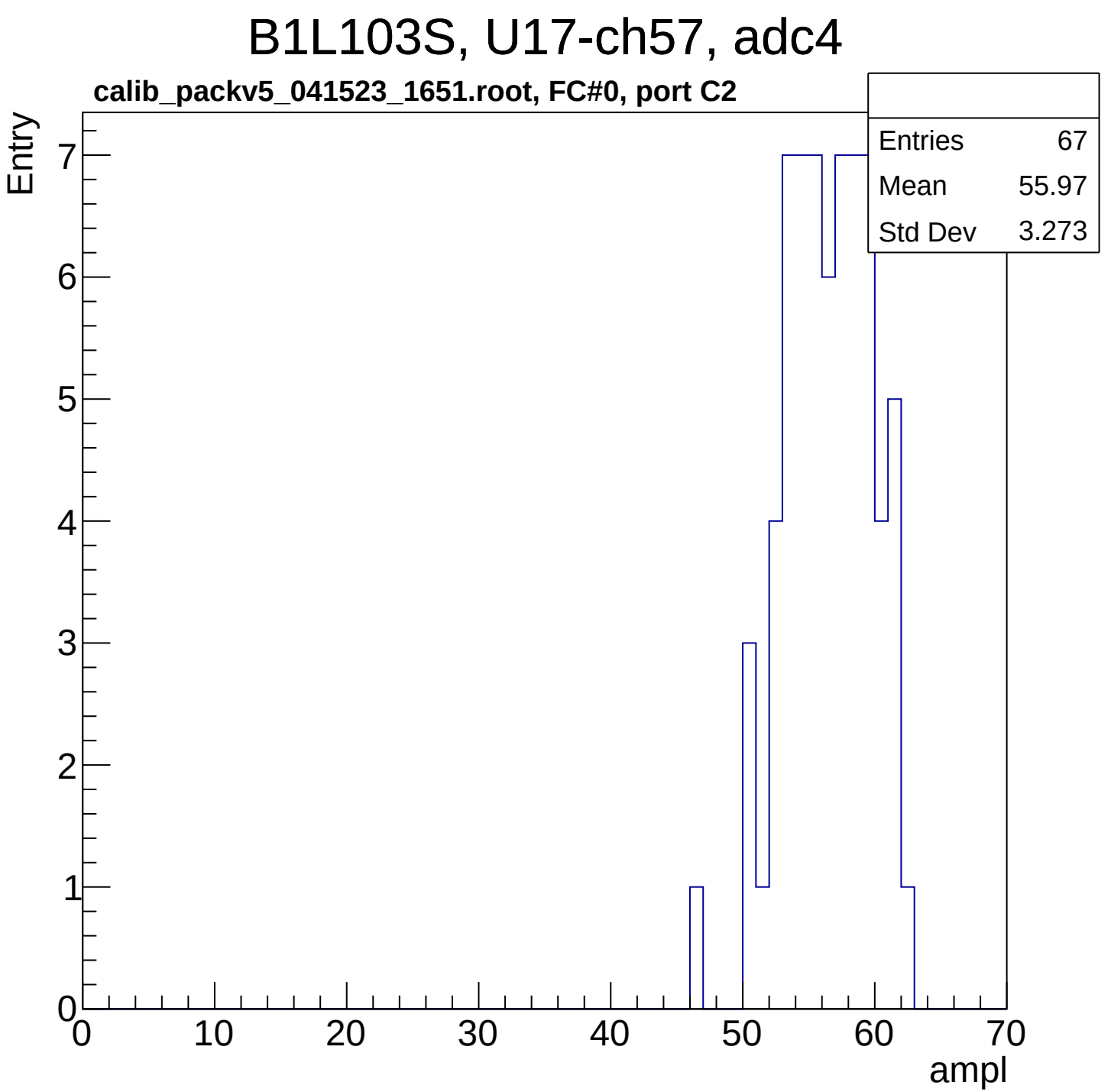

B1L103S, U17-ch56, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

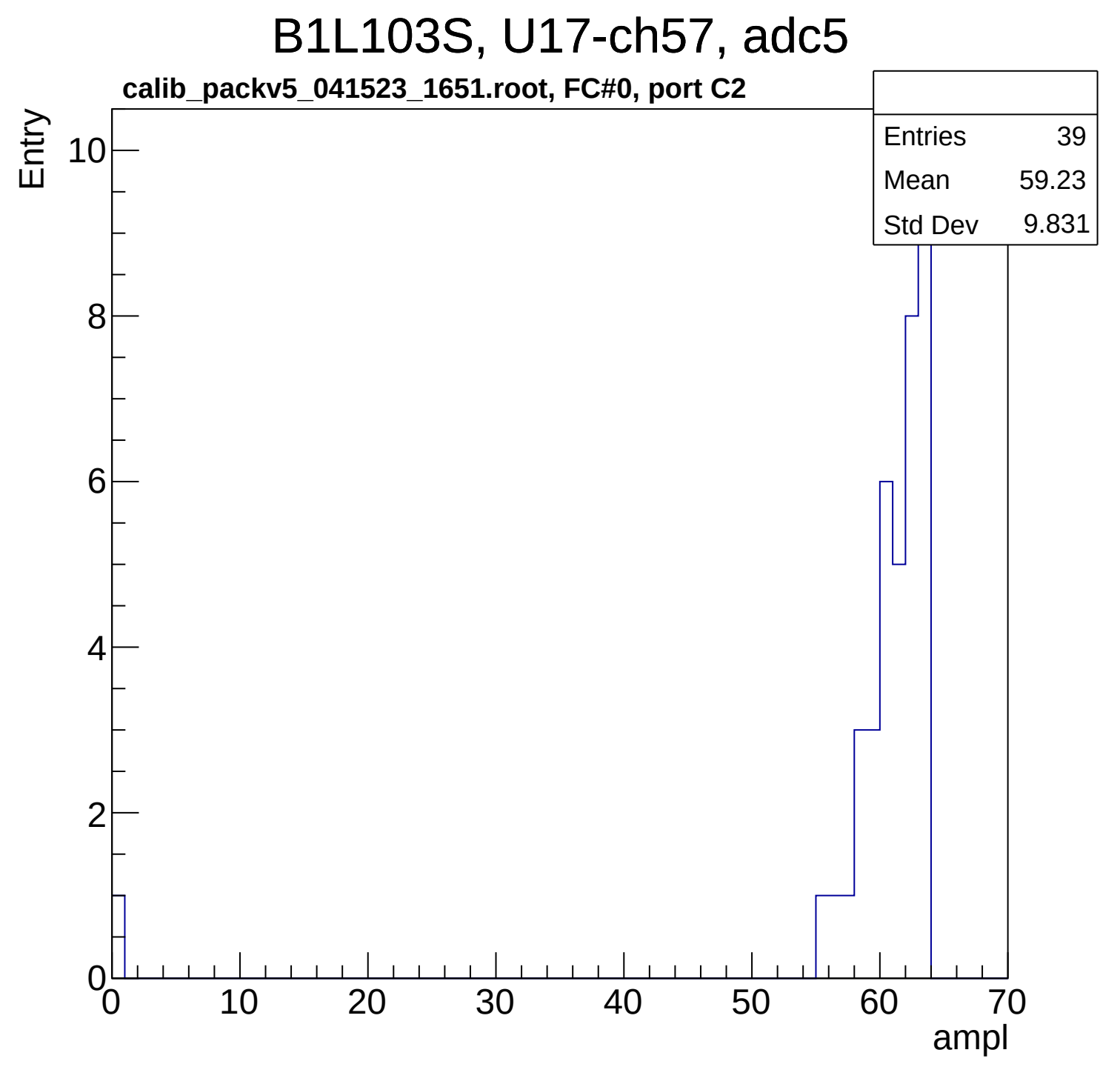

B1L103S, U17-ch57, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 24.69
Std Dev 12.12
Gaus mean : 30.7157
Gaus Width: 3.6358
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

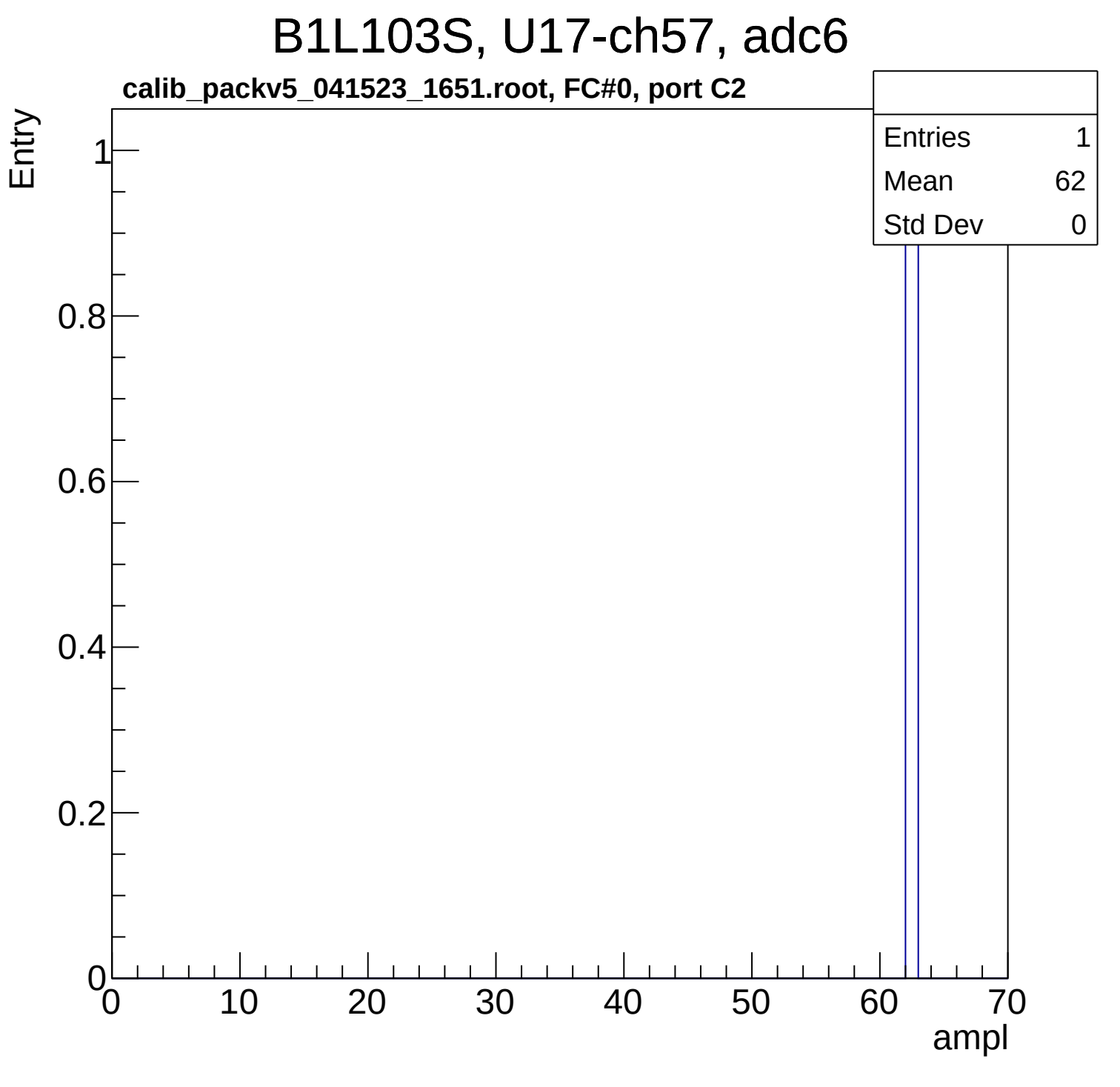

B1L103S, U17-ch57, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 30.85
Std Dev 13.87
Gaus mean : 38.0158
Gaus Width: 3.7228
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

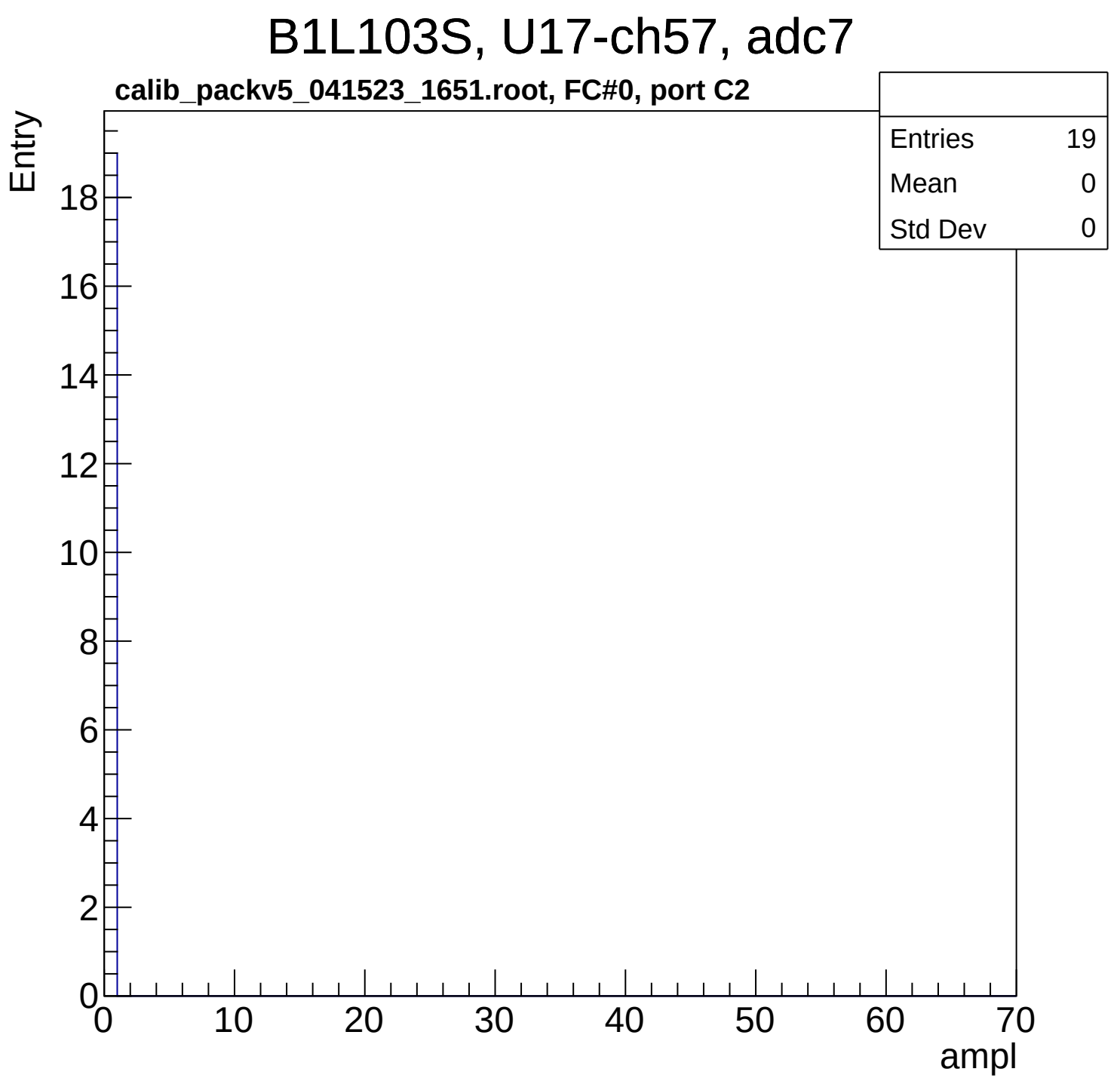

B1L103S, U17-ch57, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 40.13
Std Dev 12.7
Gaus mean : 44.1722
Gaus Width: 3.8378
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

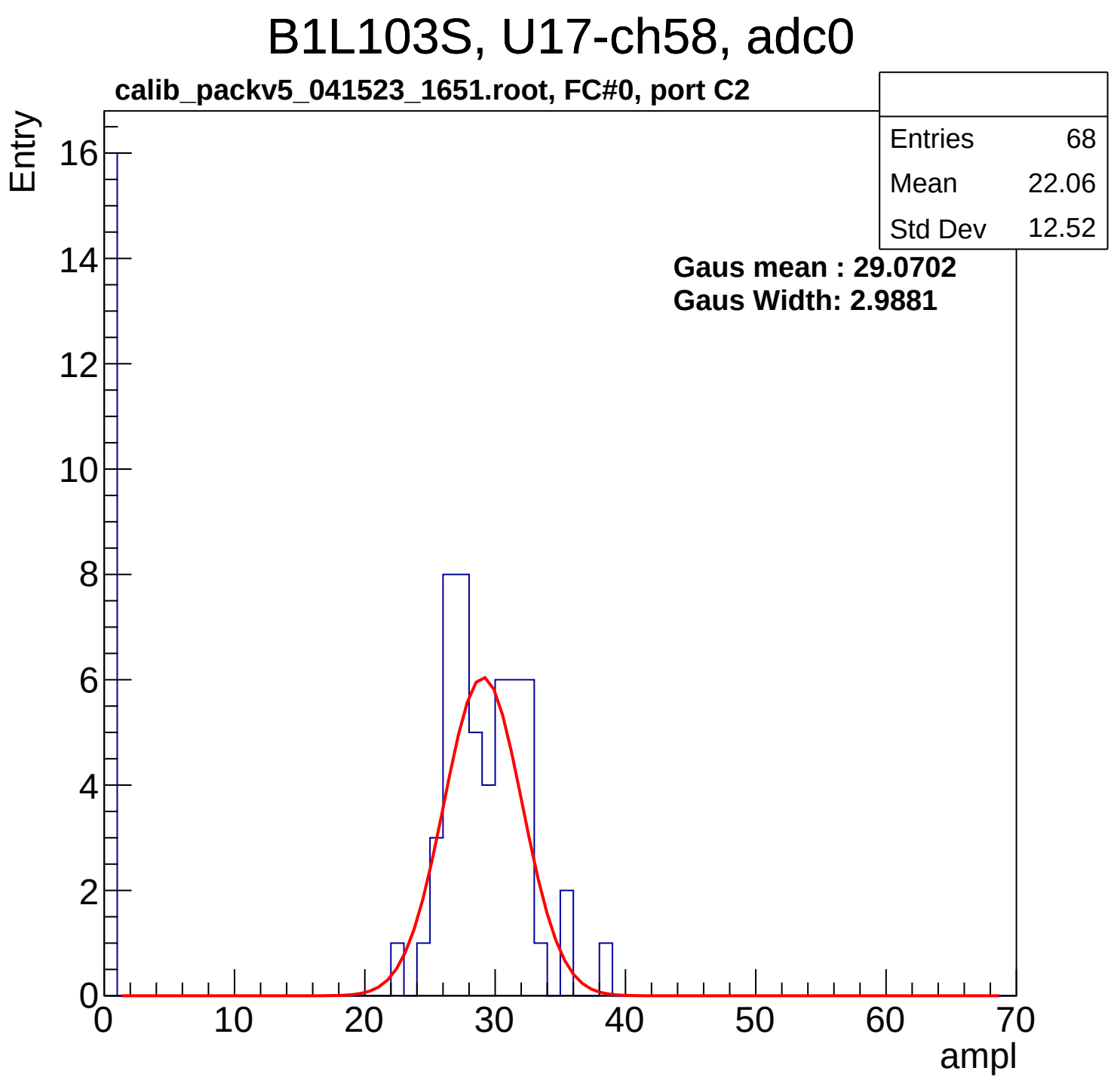

B1L103S, U17-ch57, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 50.05
Std Dev 3.435
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

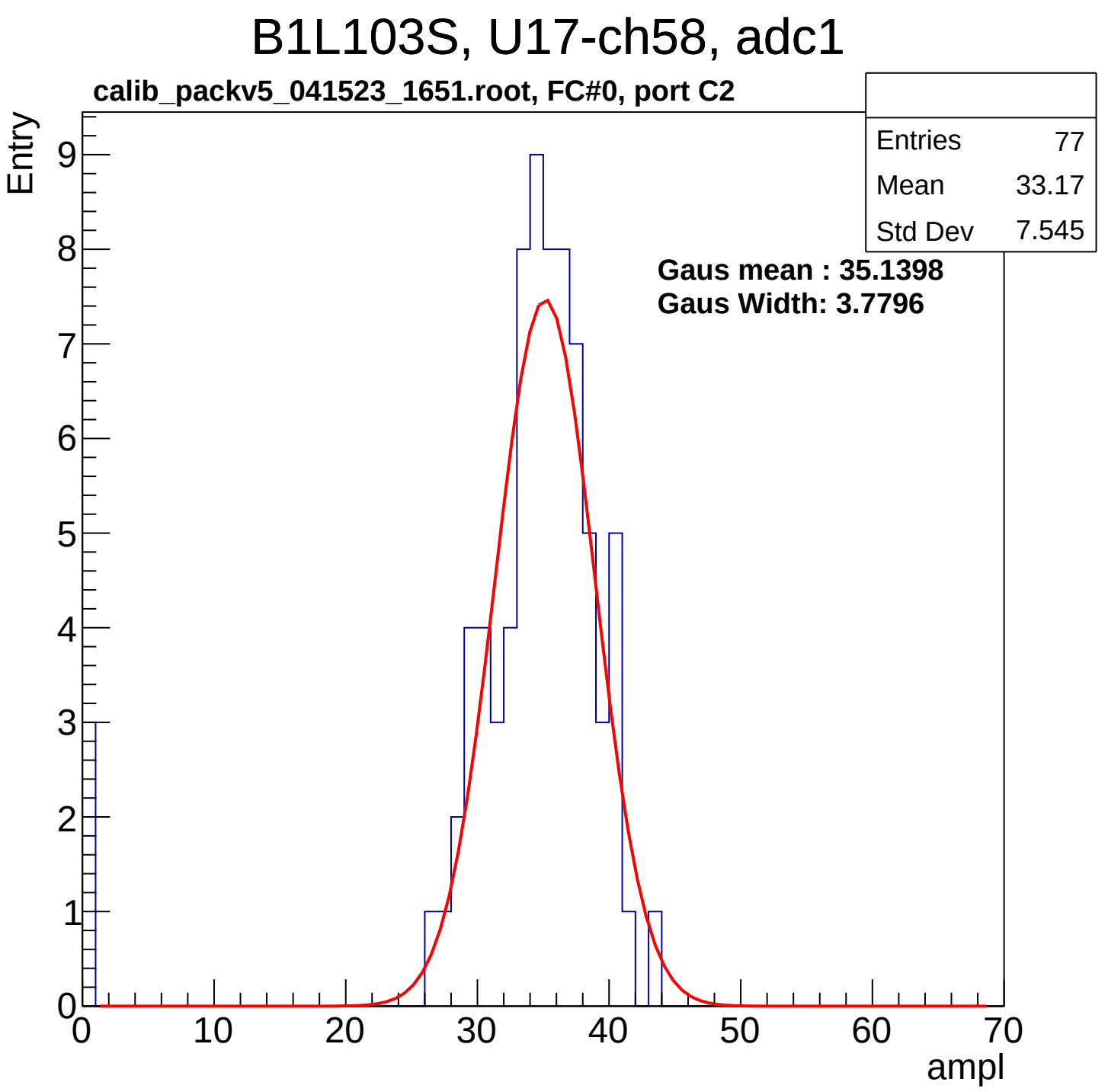

B1L103S, U17-ch57, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 55.97
Std Dev 3.273
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

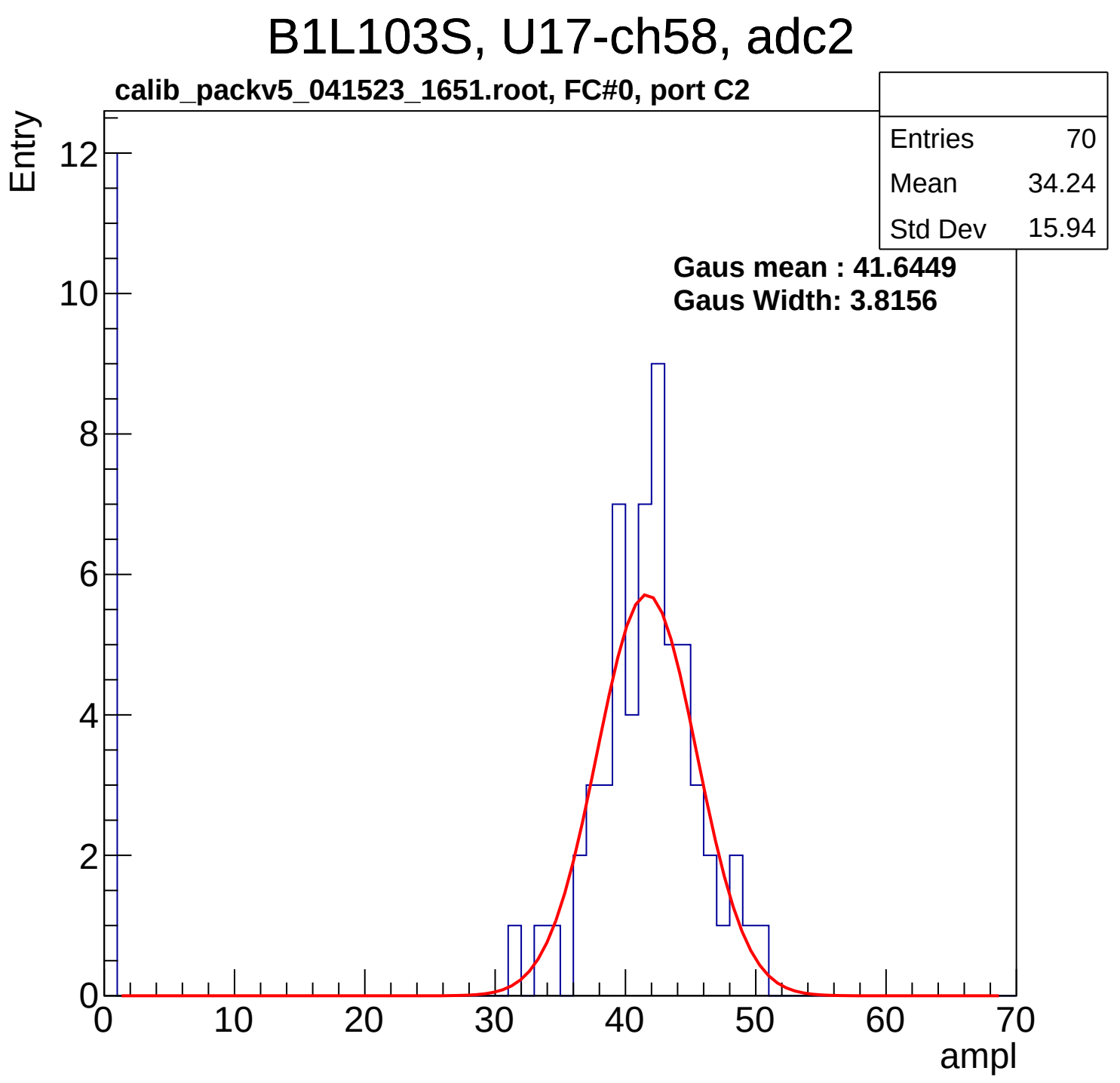

B1L103S, U17-ch57, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 59.23
Std Dev 9.831
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

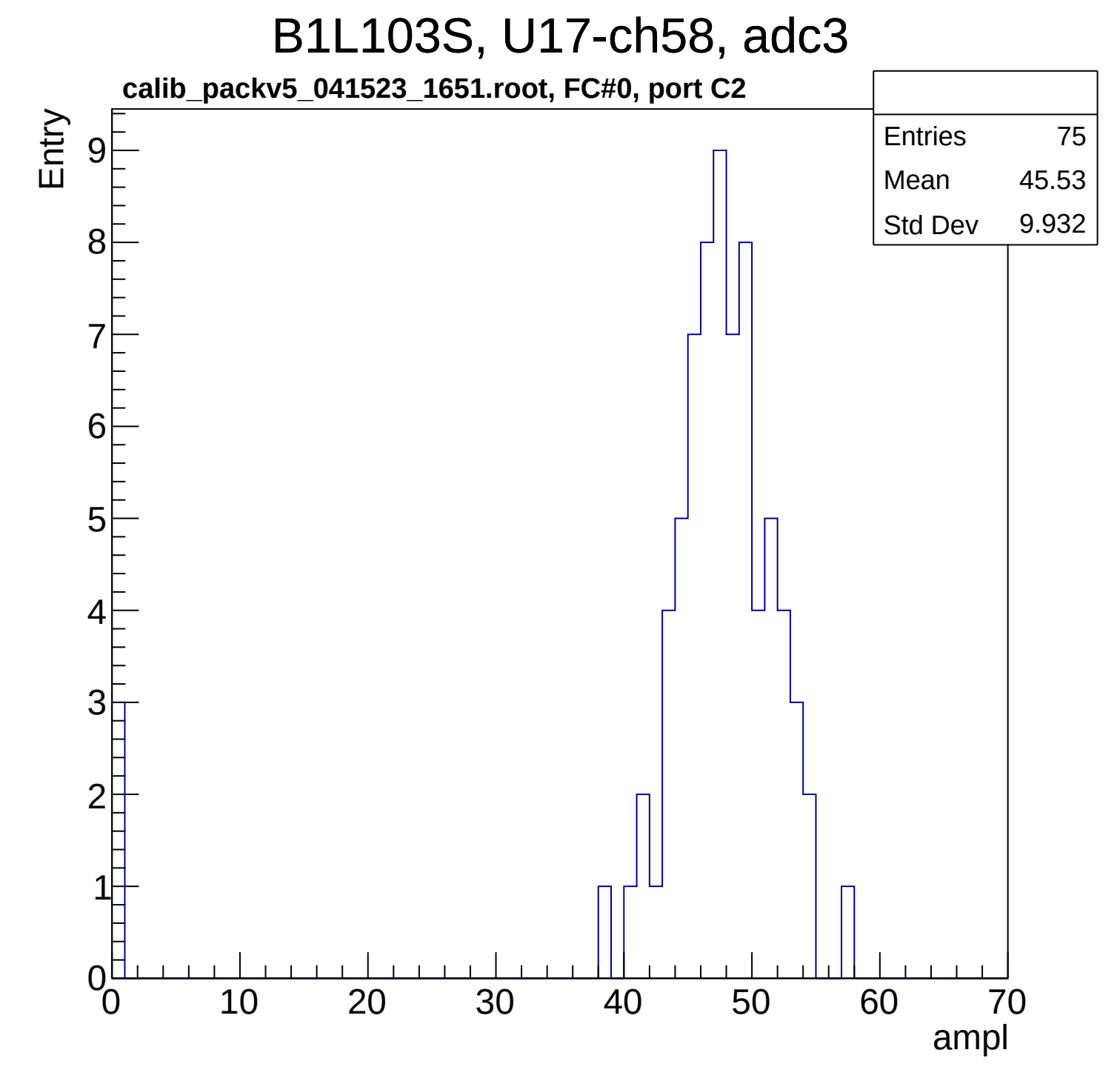

B1L103S, U17-ch57, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

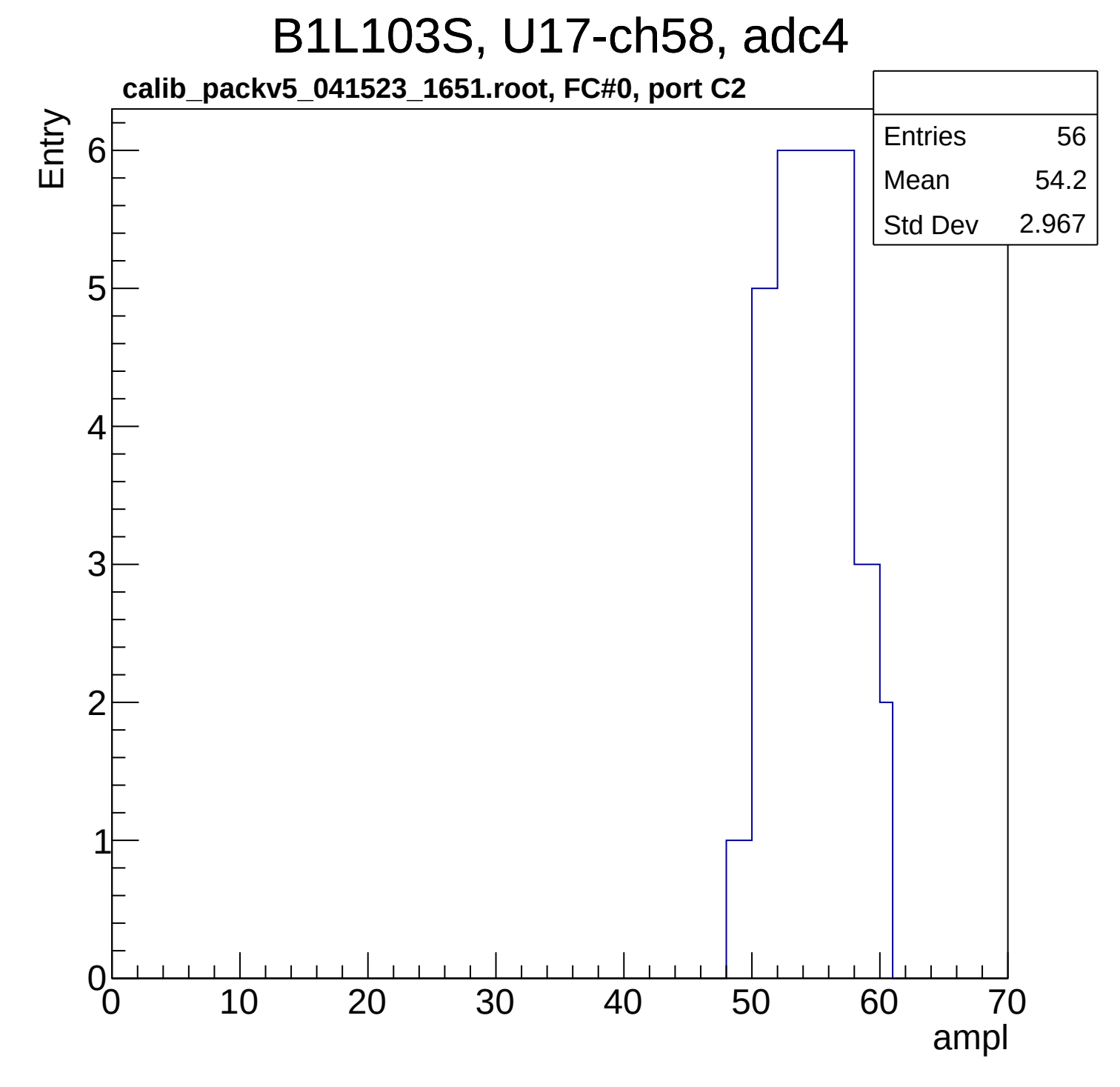

B1L103S, U17-ch57, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

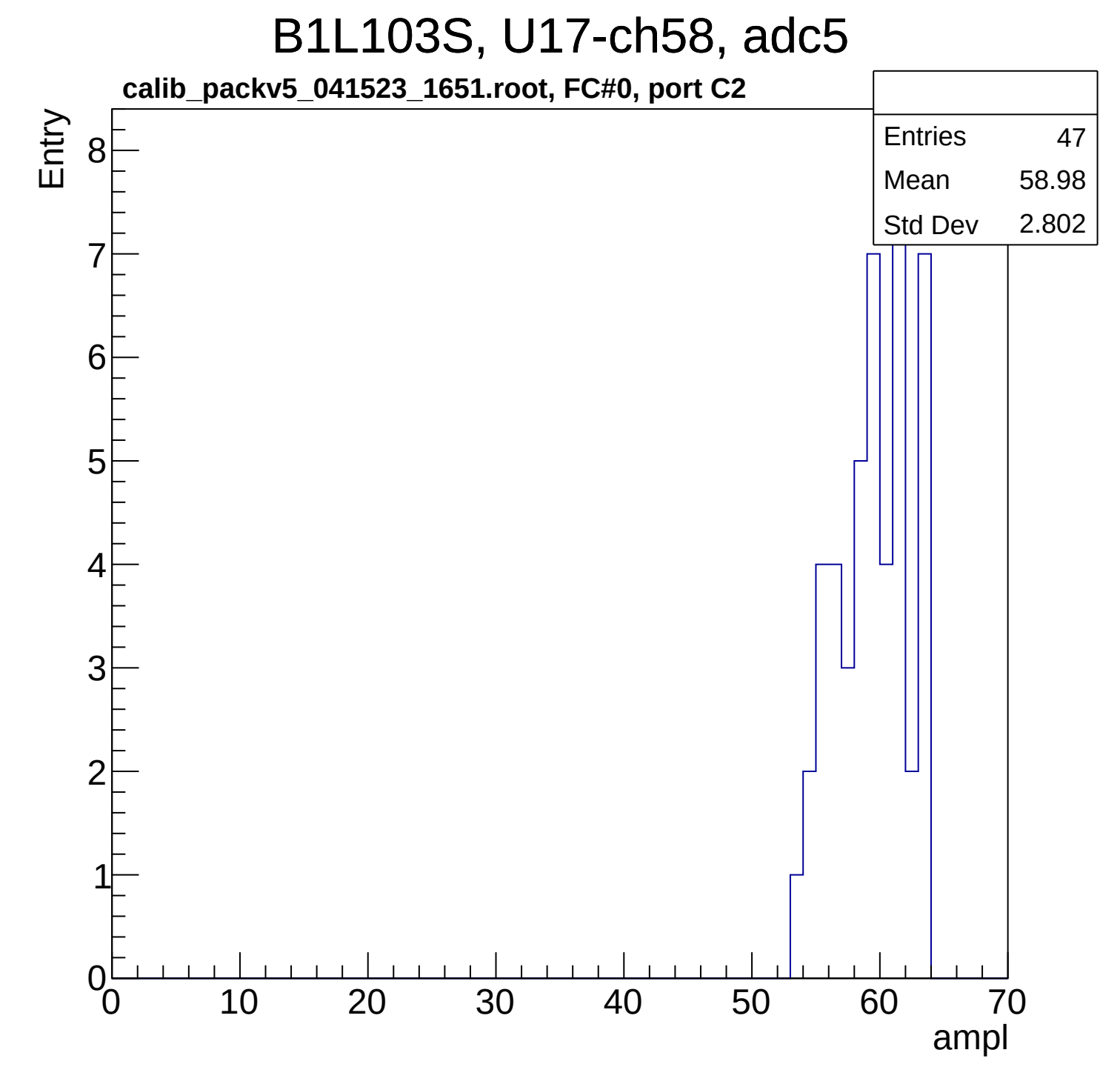

B1L103S, U17-ch58, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 22.06
Std Dev 12.52
Gaus mean : 29.0702
Gaus Width: 2.9881
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

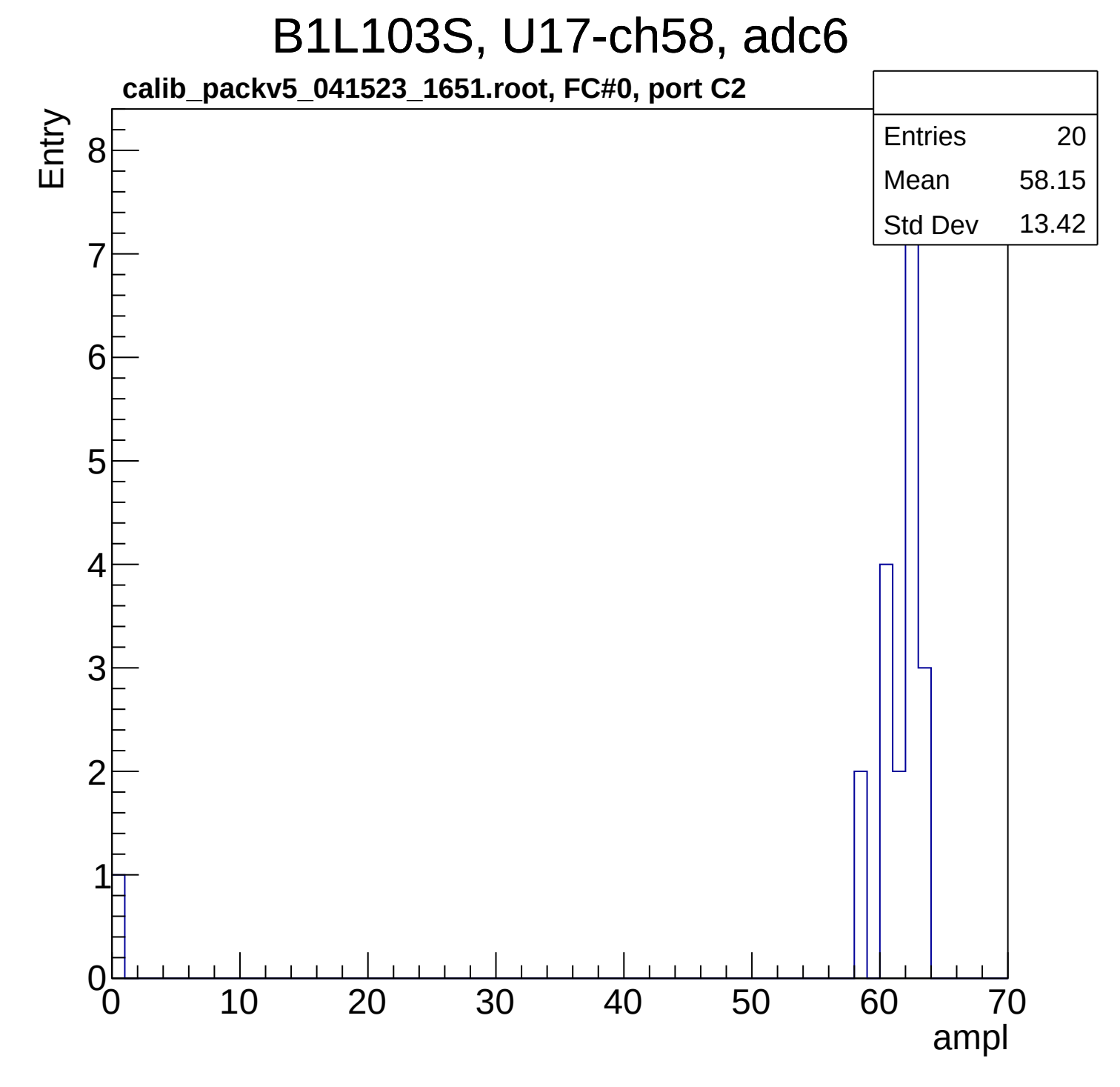

B1L103S, U17-ch58, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 33.17
Std Dev 7.545
Gaus mean : 35.1398
Gaus Width: 3.7796
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

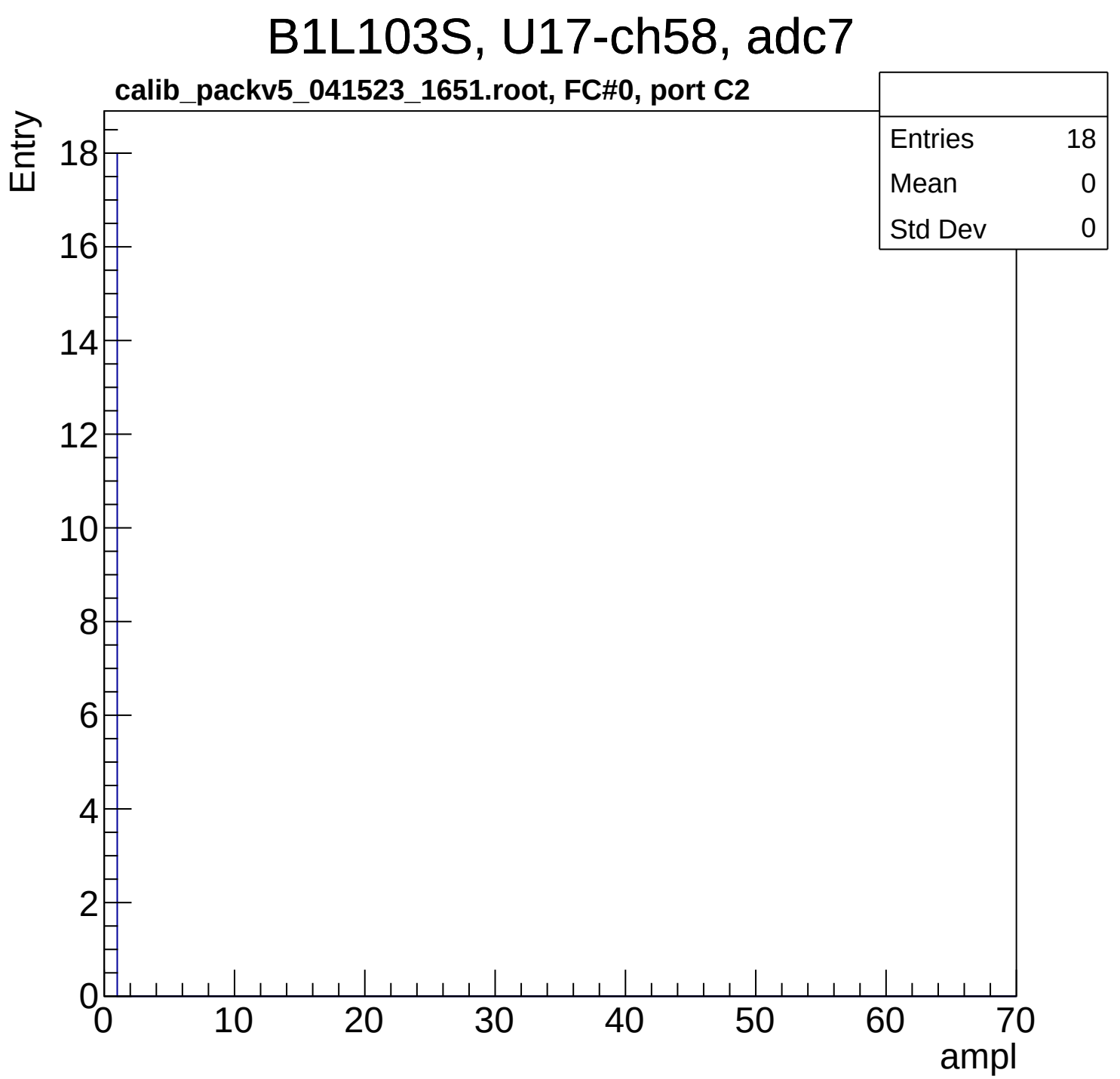

B1L103S, U17-ch58, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 34.24
Std Dev 15.94
Gaus mean : 41.6449
Gaus Width: 3.8156
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

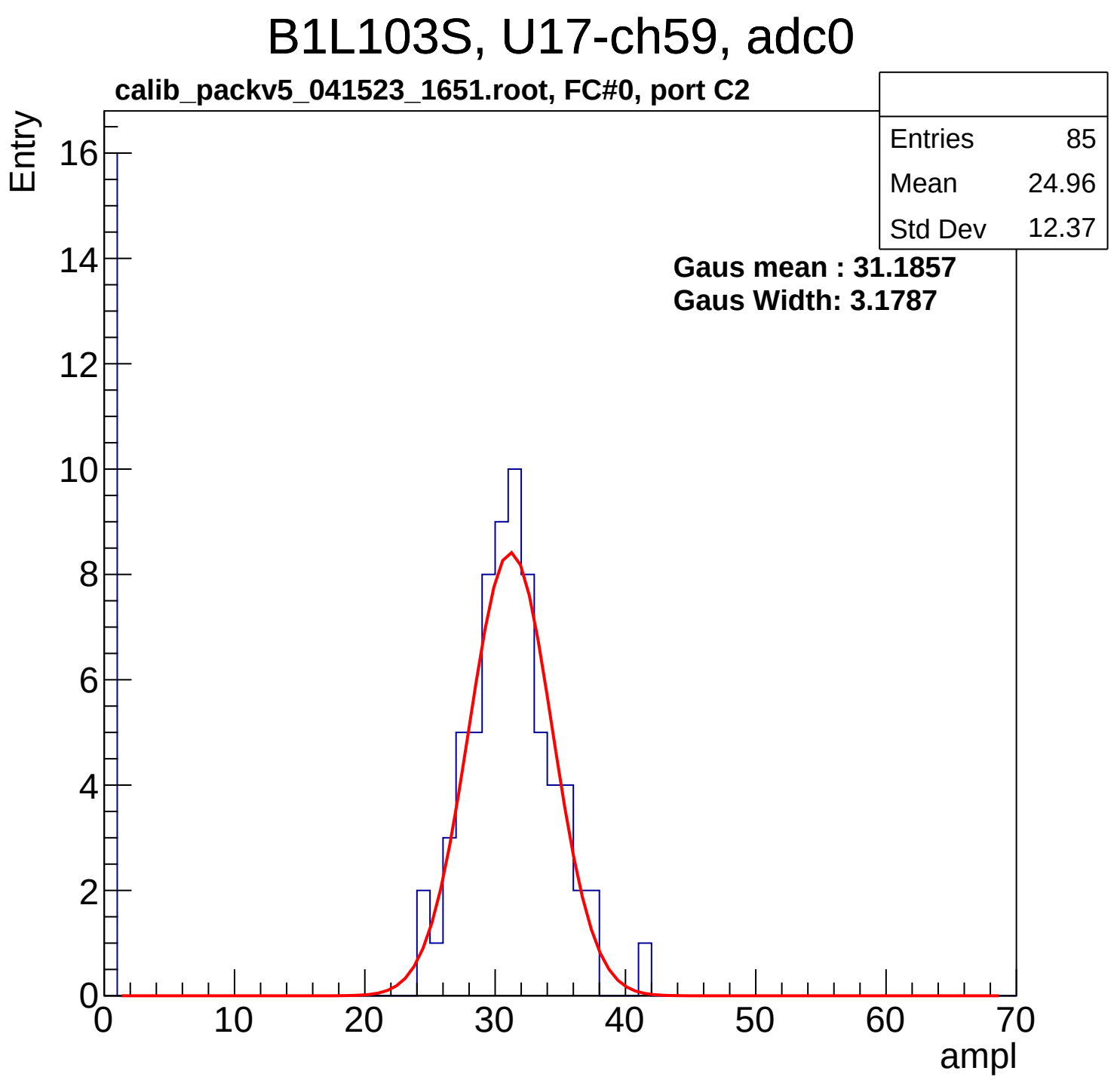

B1L103S, U17-ch58, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 45.53
Std Dev 9.932
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

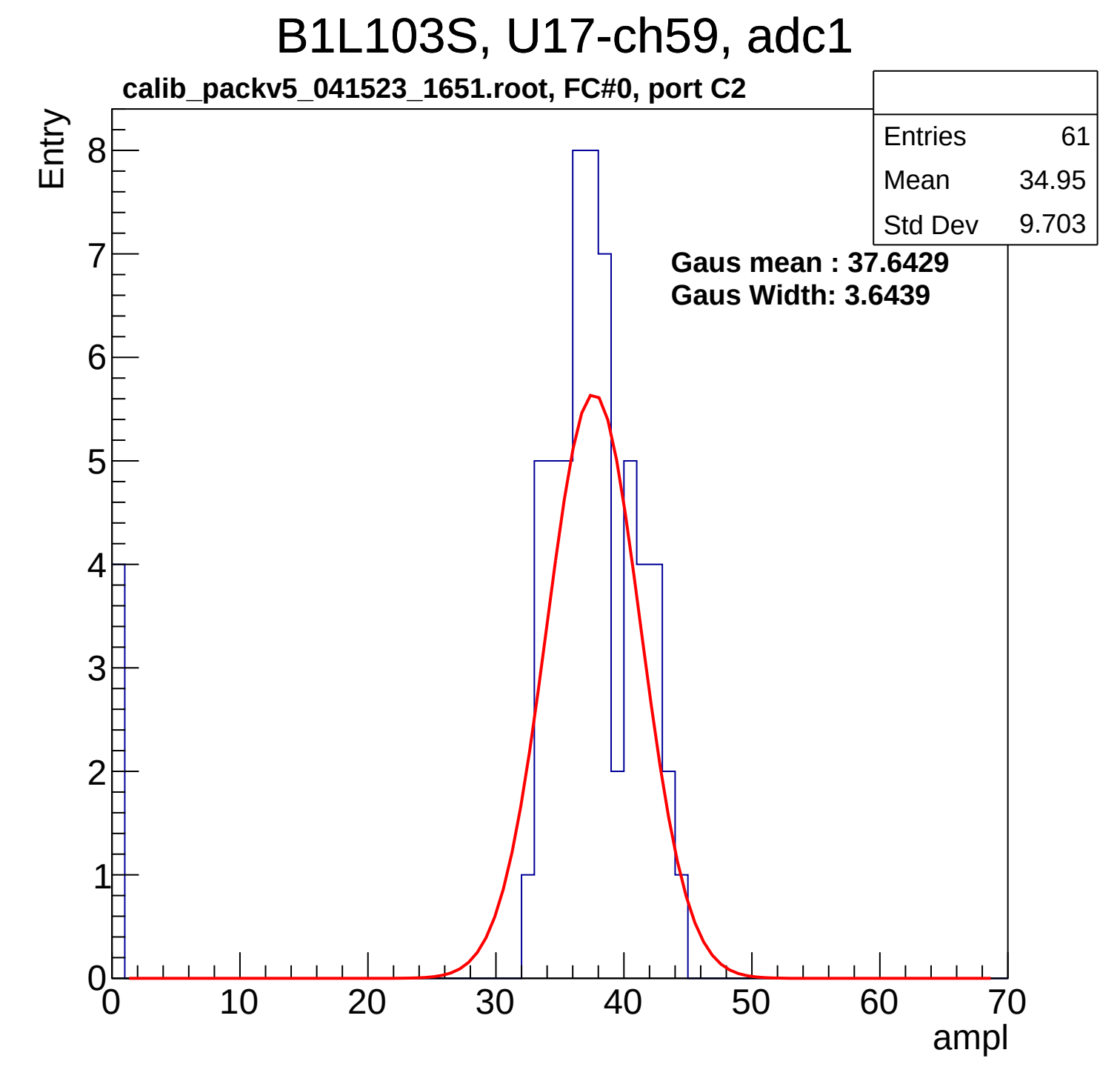

B1L103S, U17-ch58, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 54.2
Std Dev 2.967
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

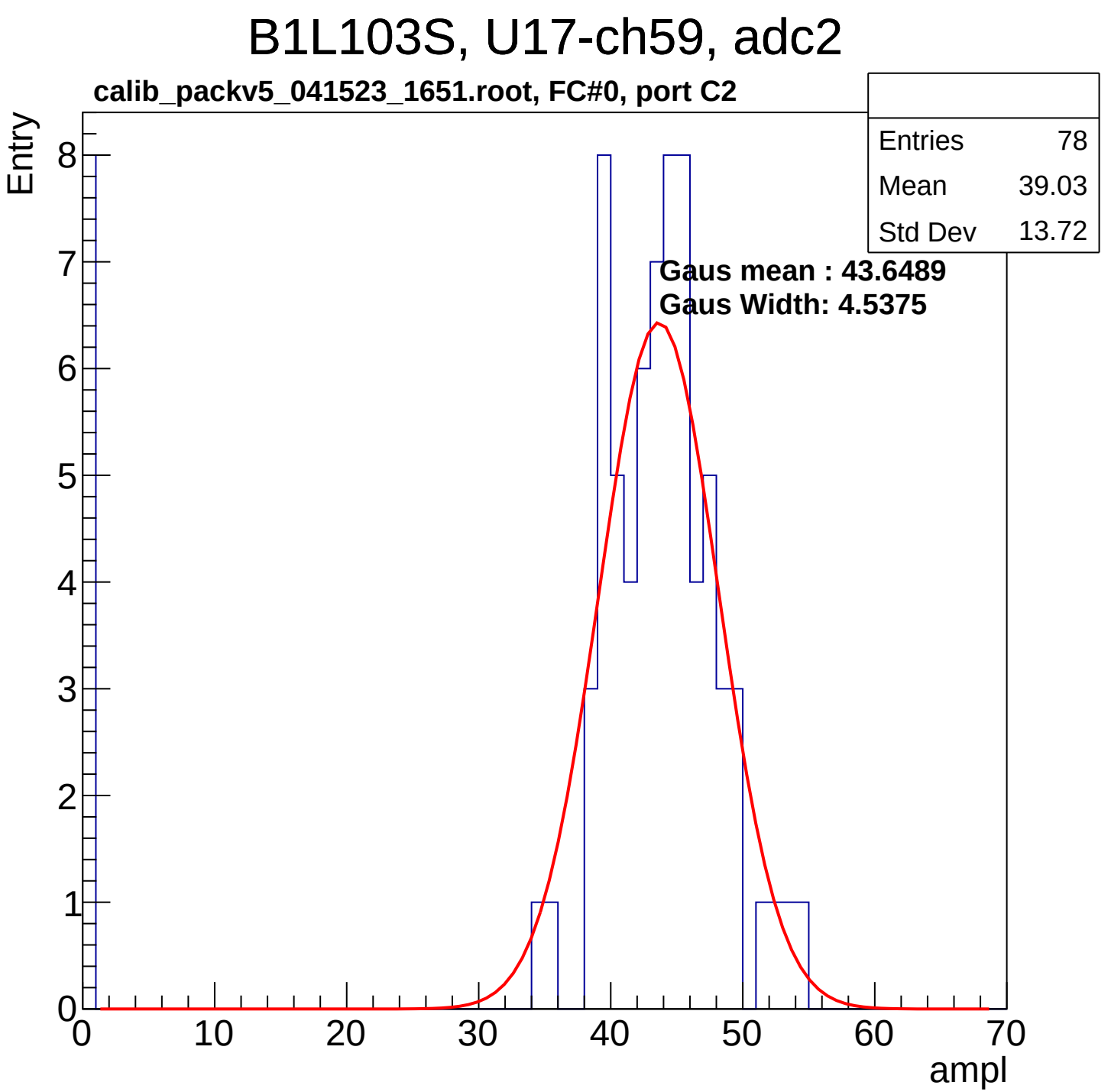

B1L103S, U17-ch58, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.98
Std Dev 2.802
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

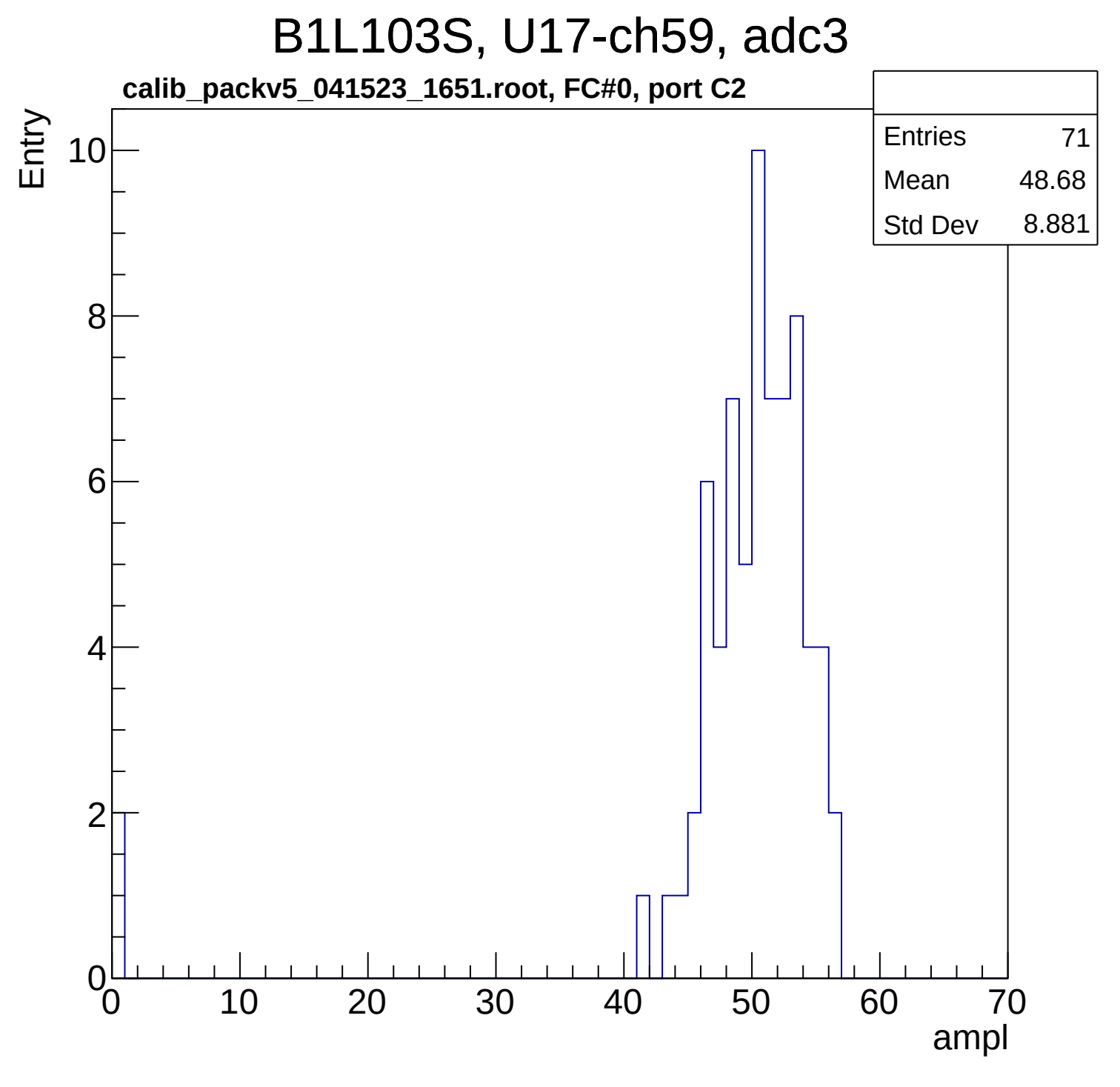

B1L103S, U17-ch58, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 58.15
Std Dev 13.42
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

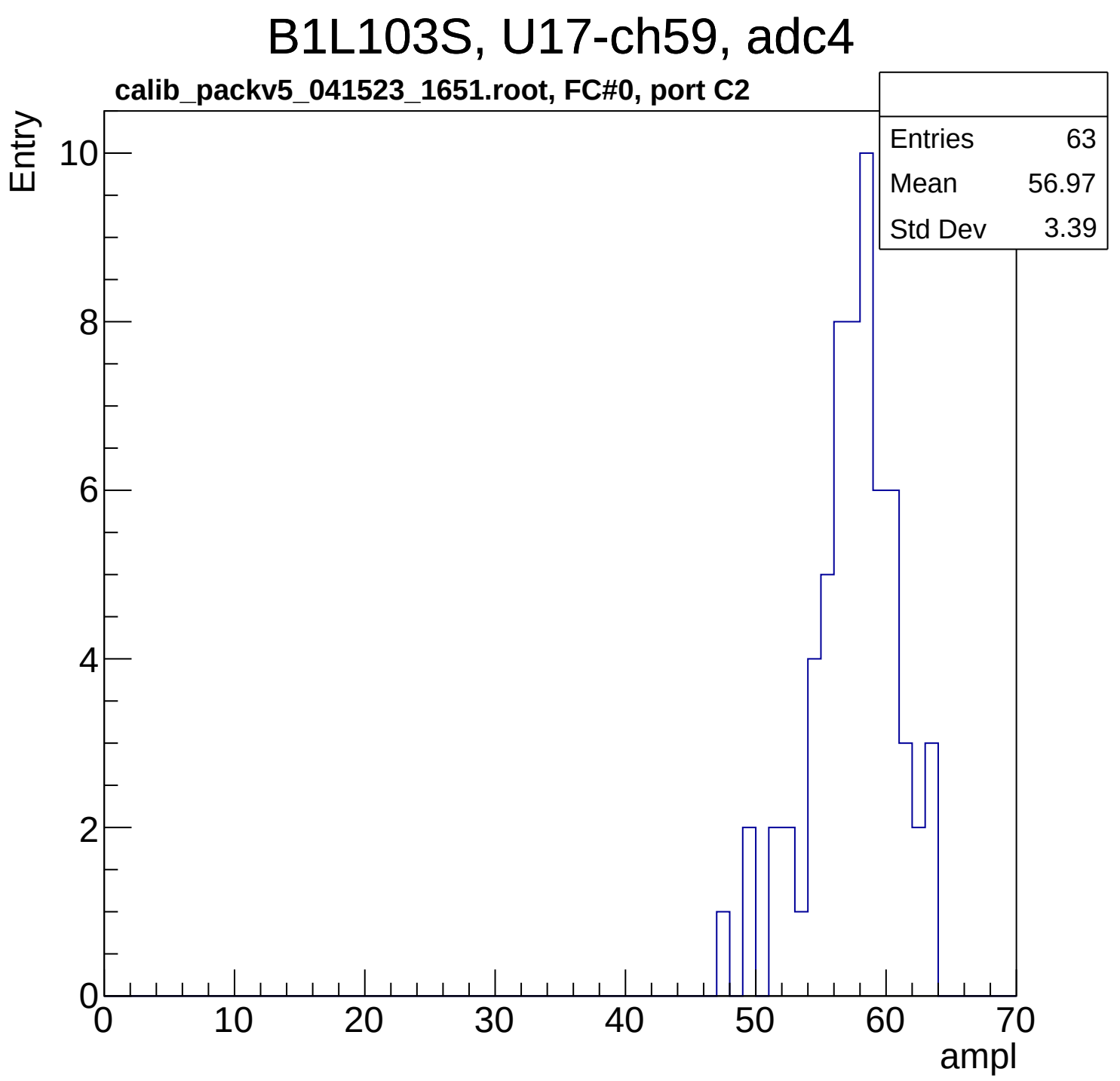

B1L103S, U17-ch58, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

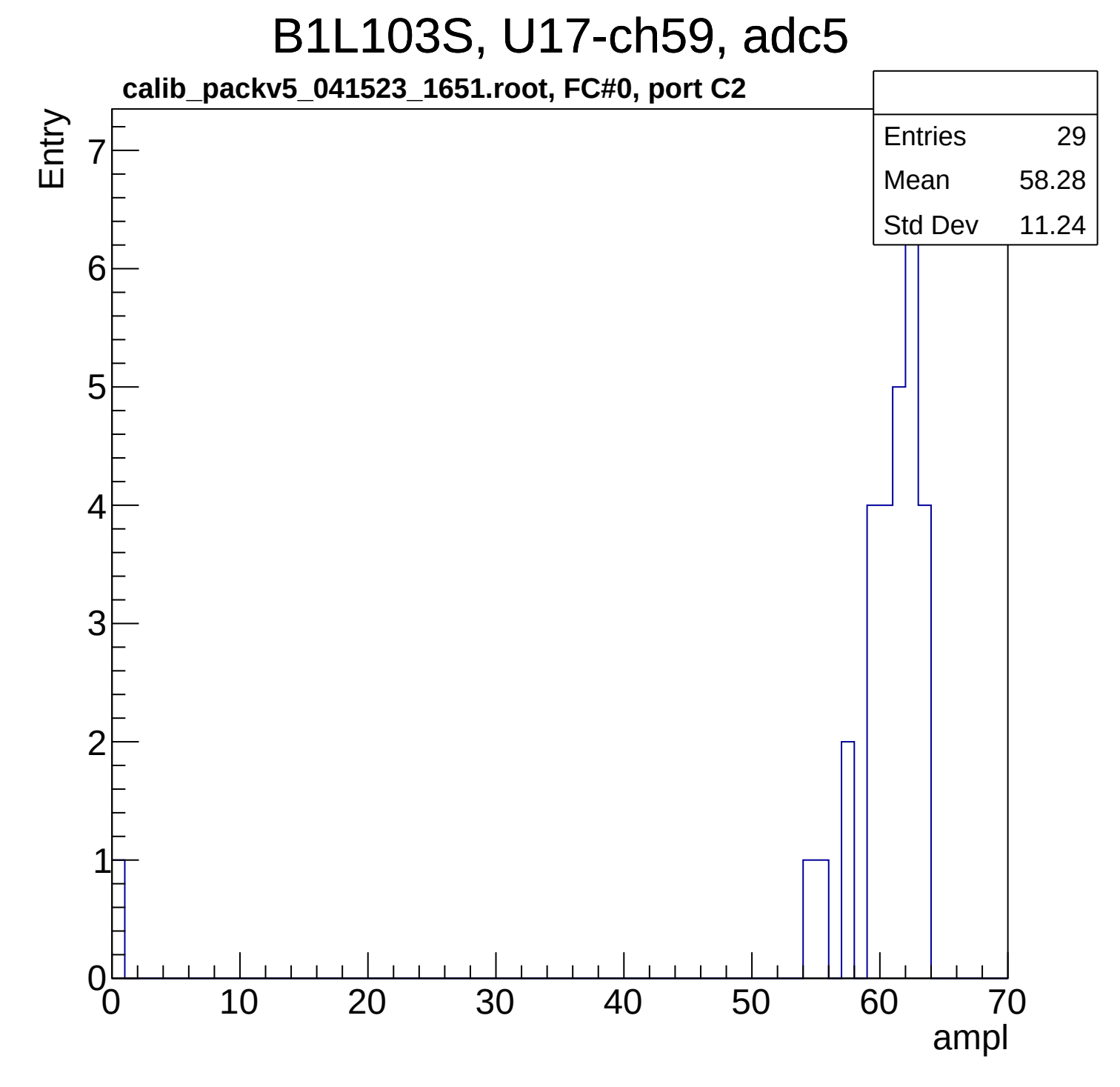

B1L103S, U17-ch59, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 24.96
Std Dev 12.37
Gaus mean : 31.1857
Gaus Width: 3.1787
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

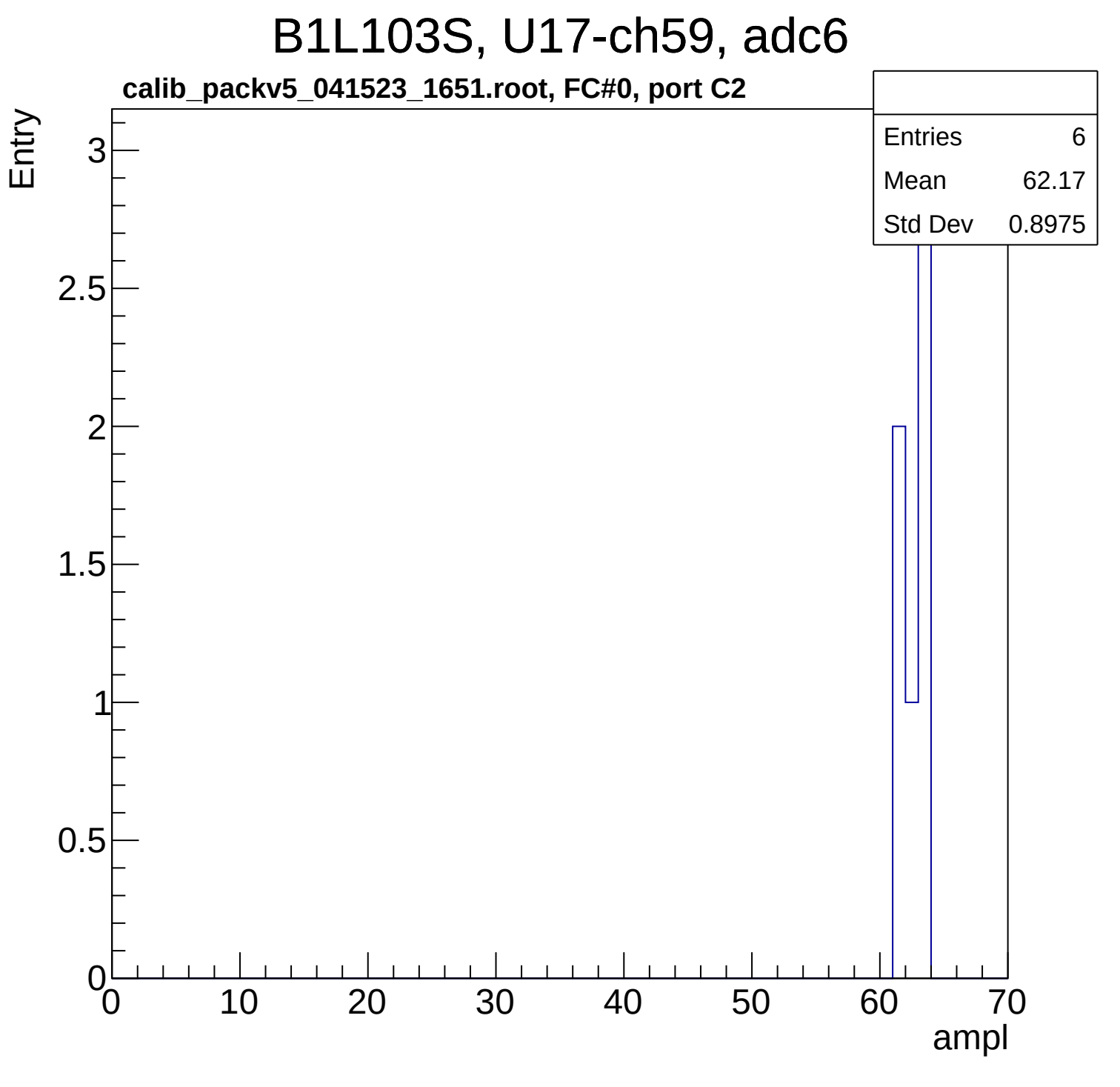

B1L103S, U17-ch59, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 34.95
Std Dev 9.703
Gaus mean : 37.6429
Gaus Width: 3.6439
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

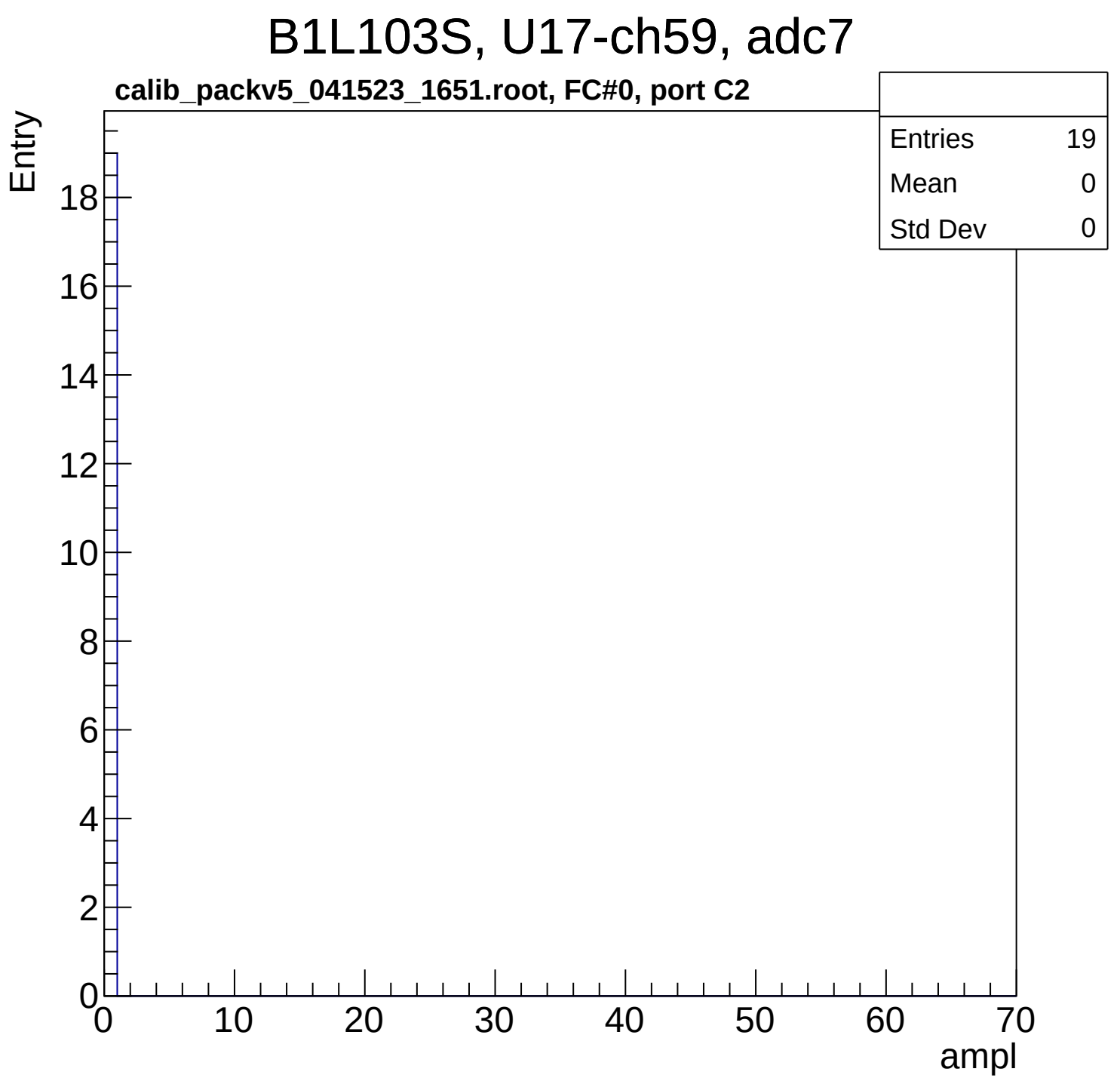

B1L103S, U17-ch59, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 39.03
Std Dev 13.72
Gaus mean : 43.6489
Gaus Width: 4.5375
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

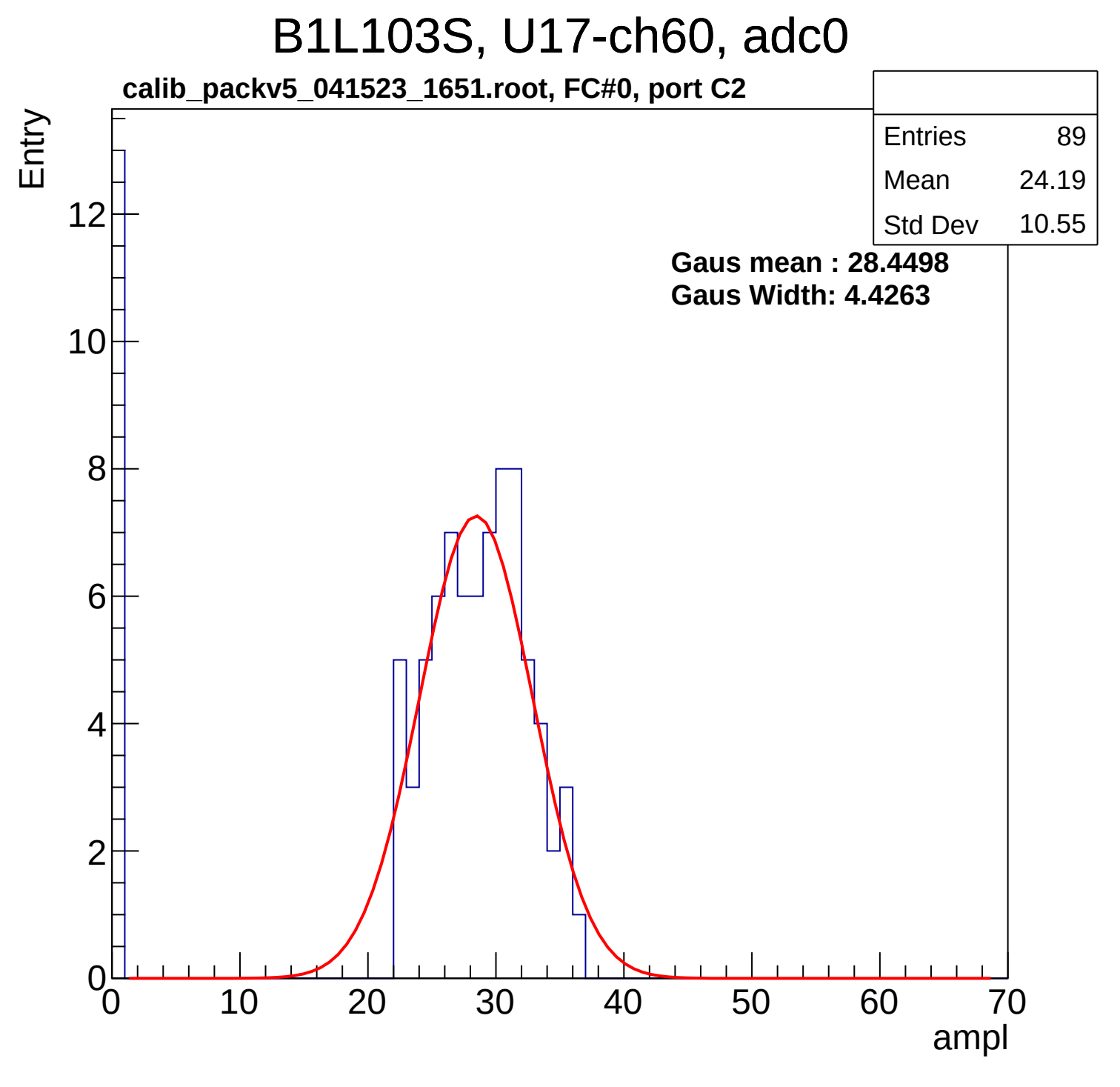

B1L103S, U17-ch59, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 48.68
Std Dev 8.881
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

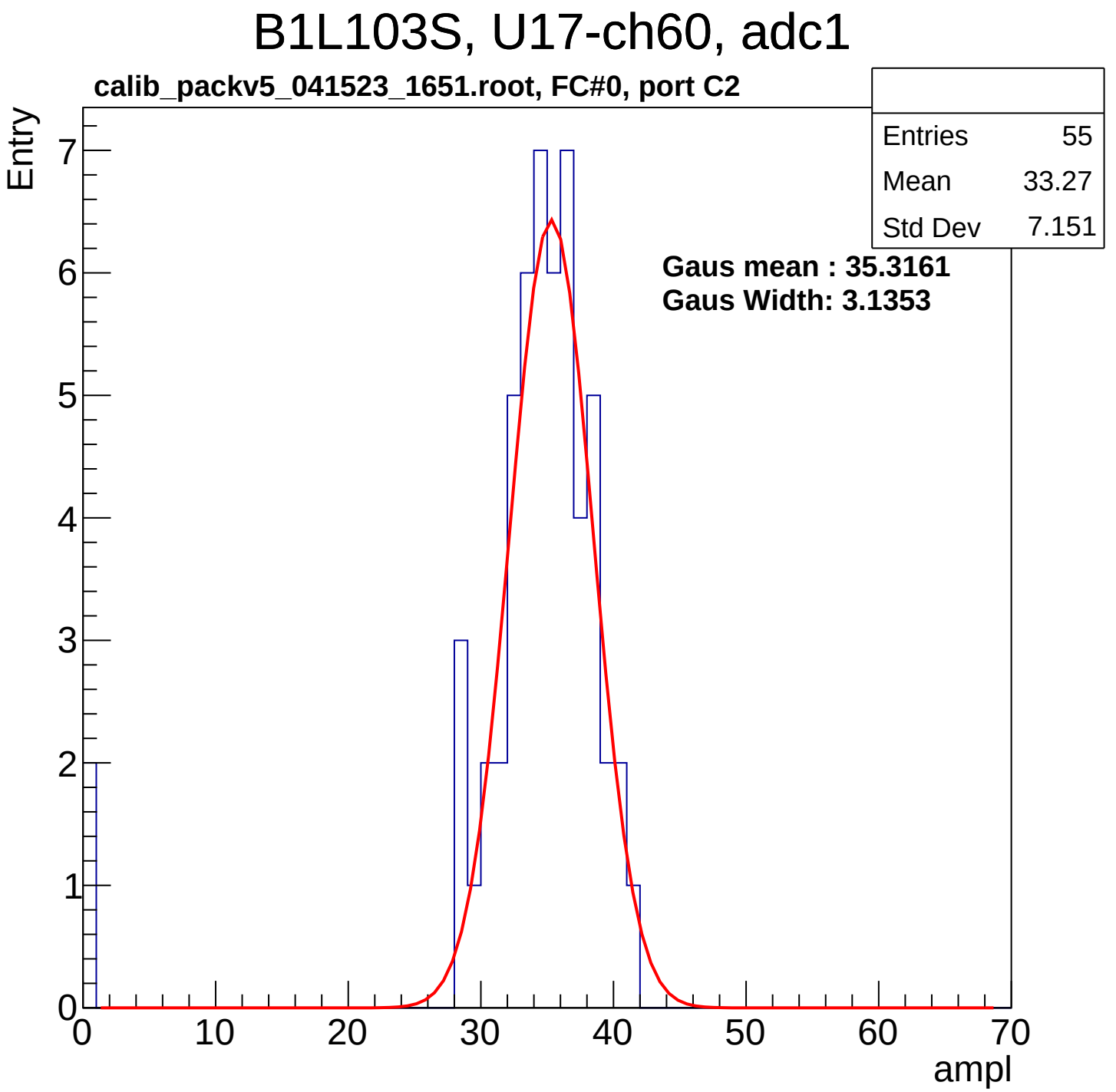

B1L103S, U17-ch59, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 56.97
Std Dev 3.39
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

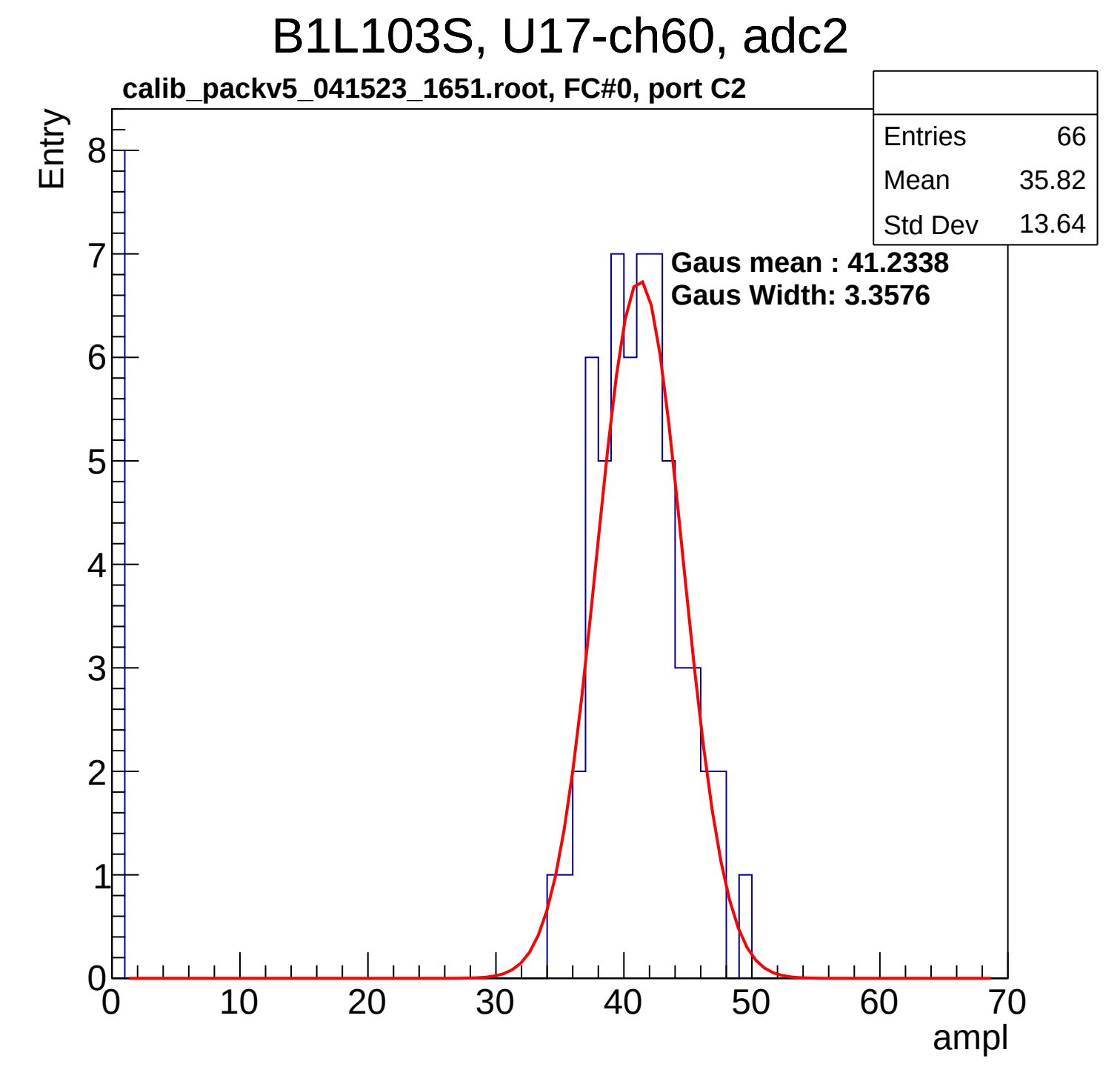

B1L103S, U17-ch59, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 58.28
Std Dev 11.24
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

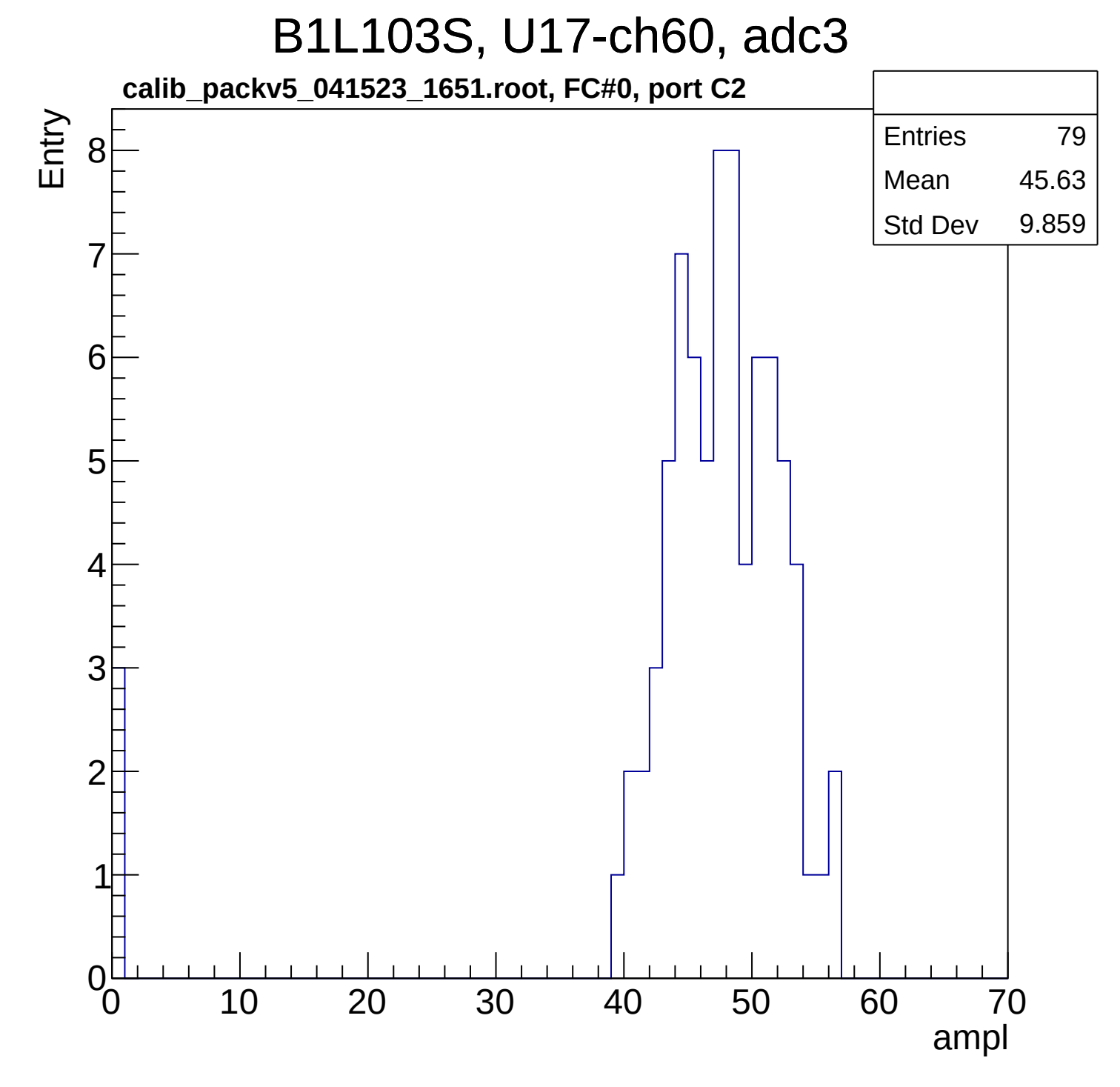

B1L103S, U17-ch59, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.17
Std Dev 0.8975
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

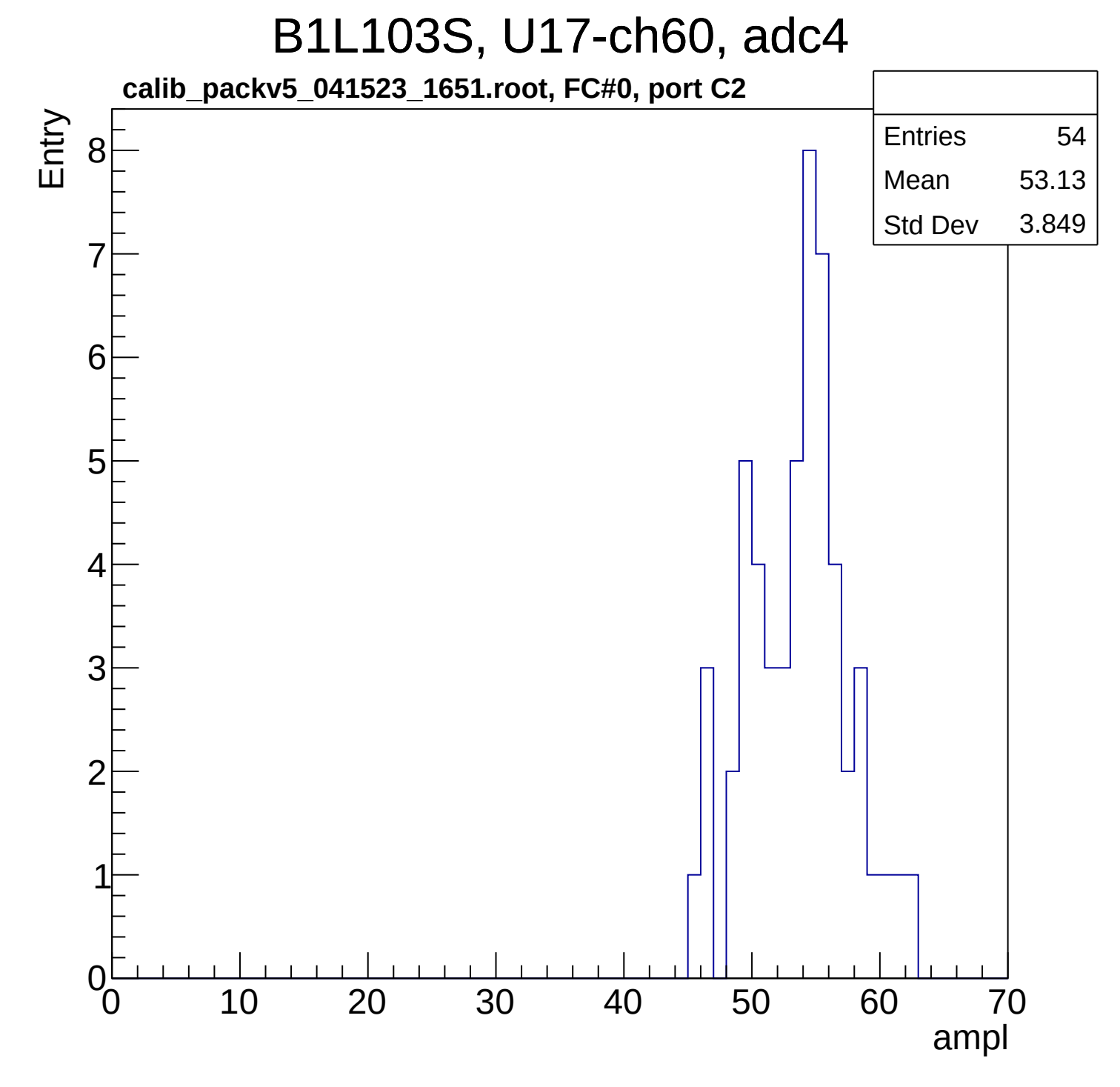

B1L103S, U17-ch59, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

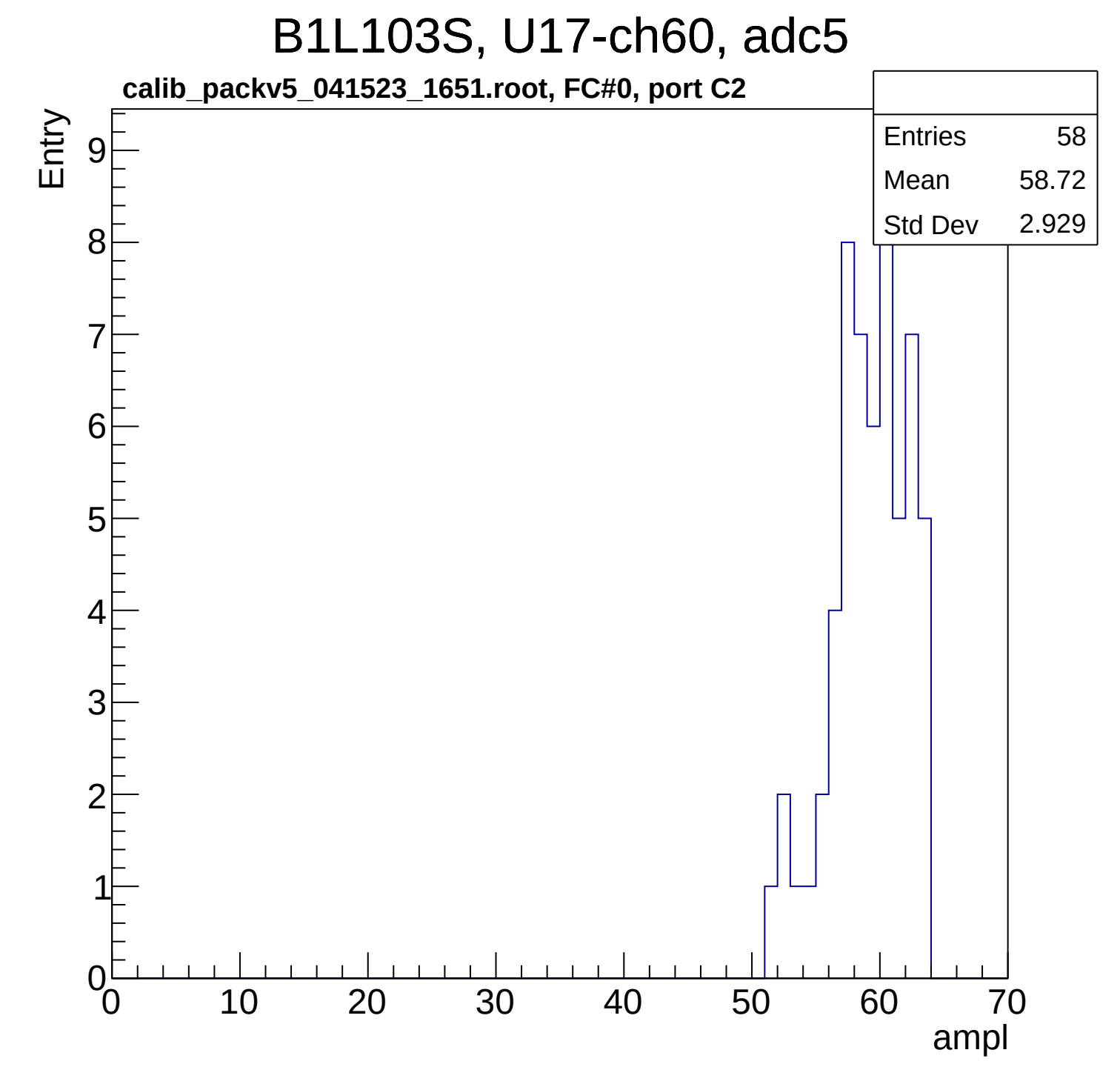

B1L103S, U17-ch60, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 24.19
Std Dev 10.55
Gaus mean : 28.4498
Gaus Width: 4.4263
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

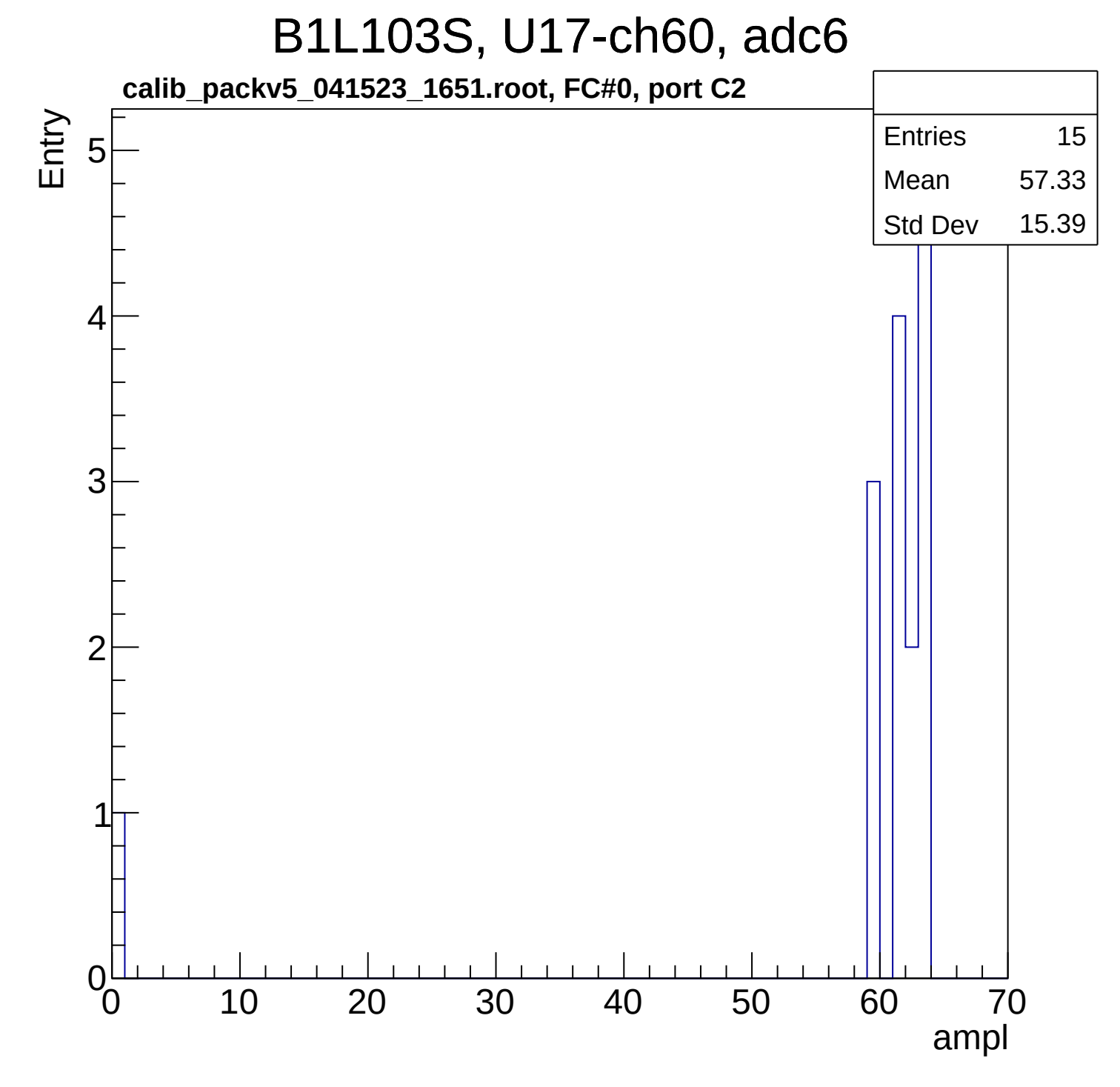

B1L103S, U17-ch60, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 33.27
Std Dev 7.151
Gaus mean : 35.3161
Gaus Width: 3.1353
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

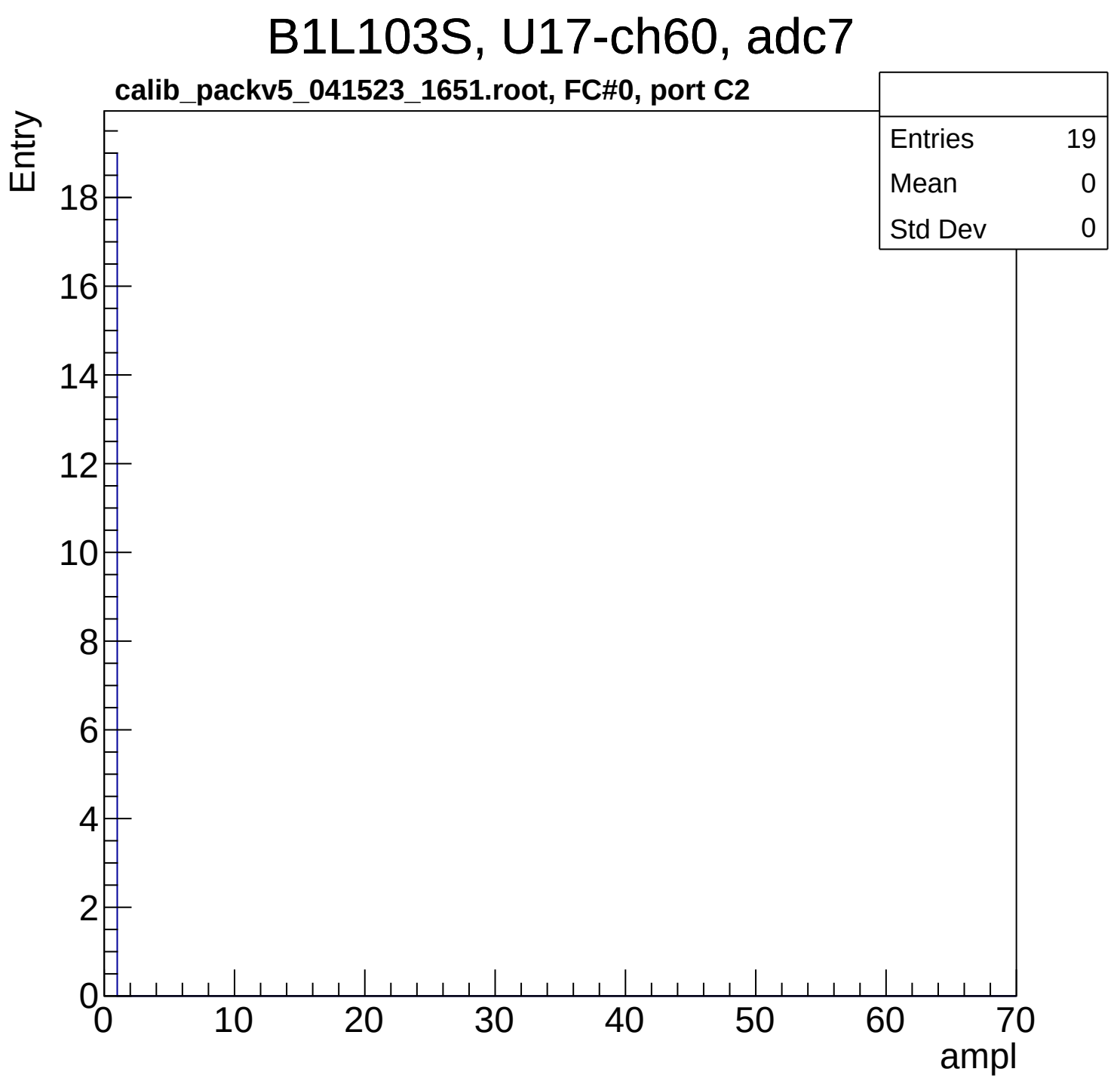

B1L103S, U17-ch60, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 35.82
Std Dev 13.64
Gaus mean : 41.2338
Gaus Width: 3.3576
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

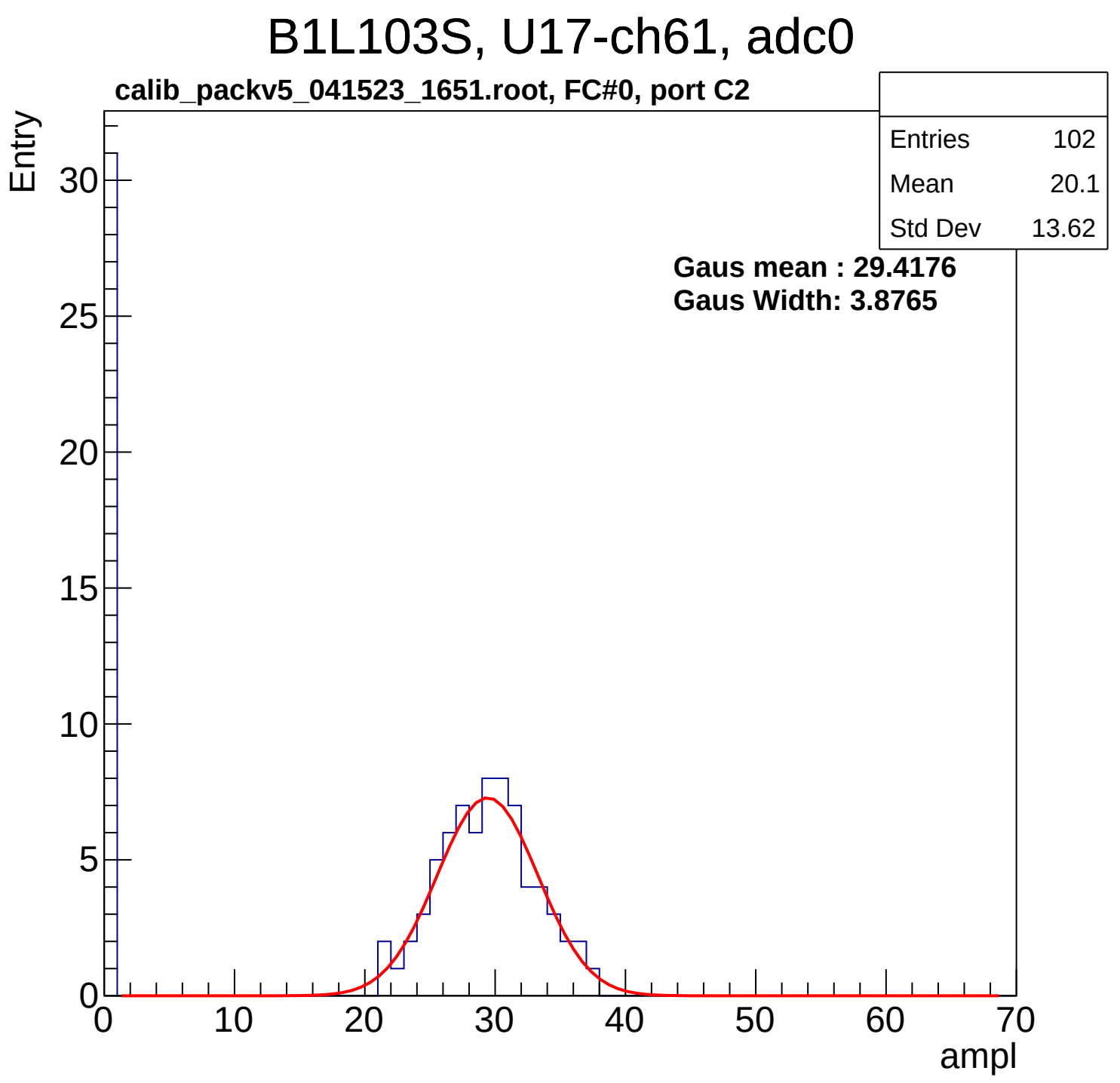

B1L103S, U17-ch60, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 45.63
Std Dev 9.859
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

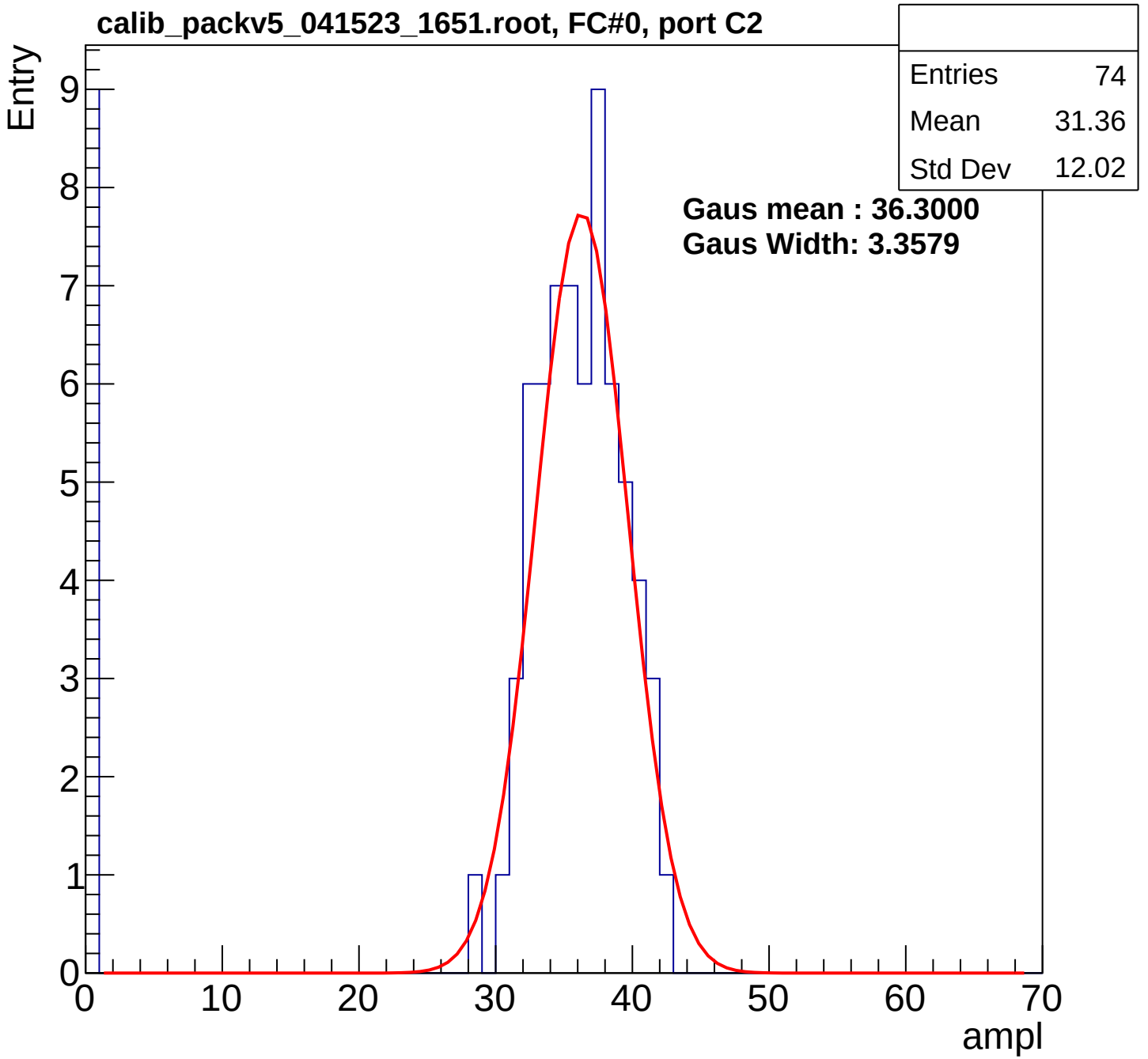

B1L103S, U17-ch60, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 53.13
Std Dev 3.849
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

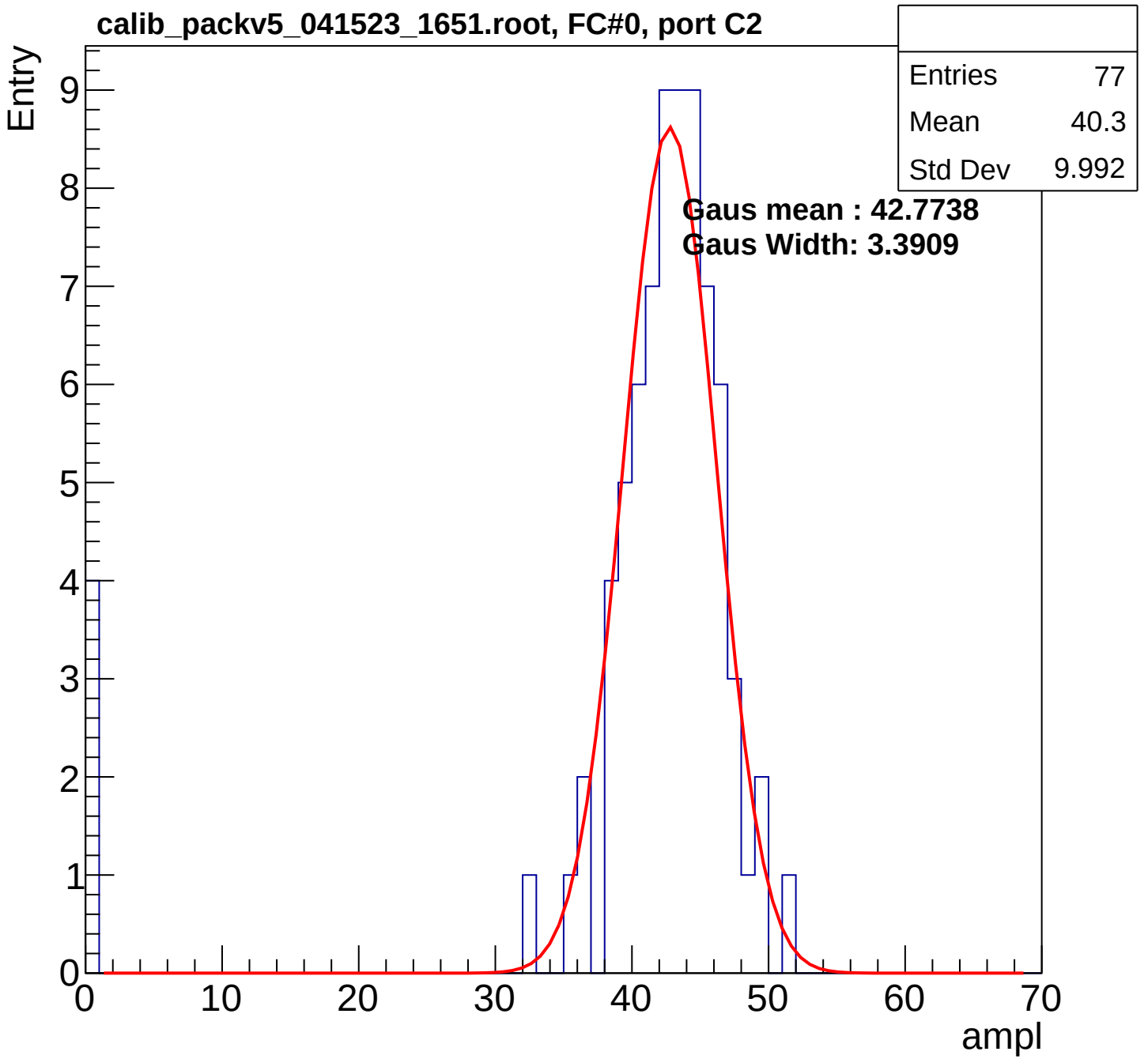

B1L103S, U17-ch60, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.72
Std Dev 2.929
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

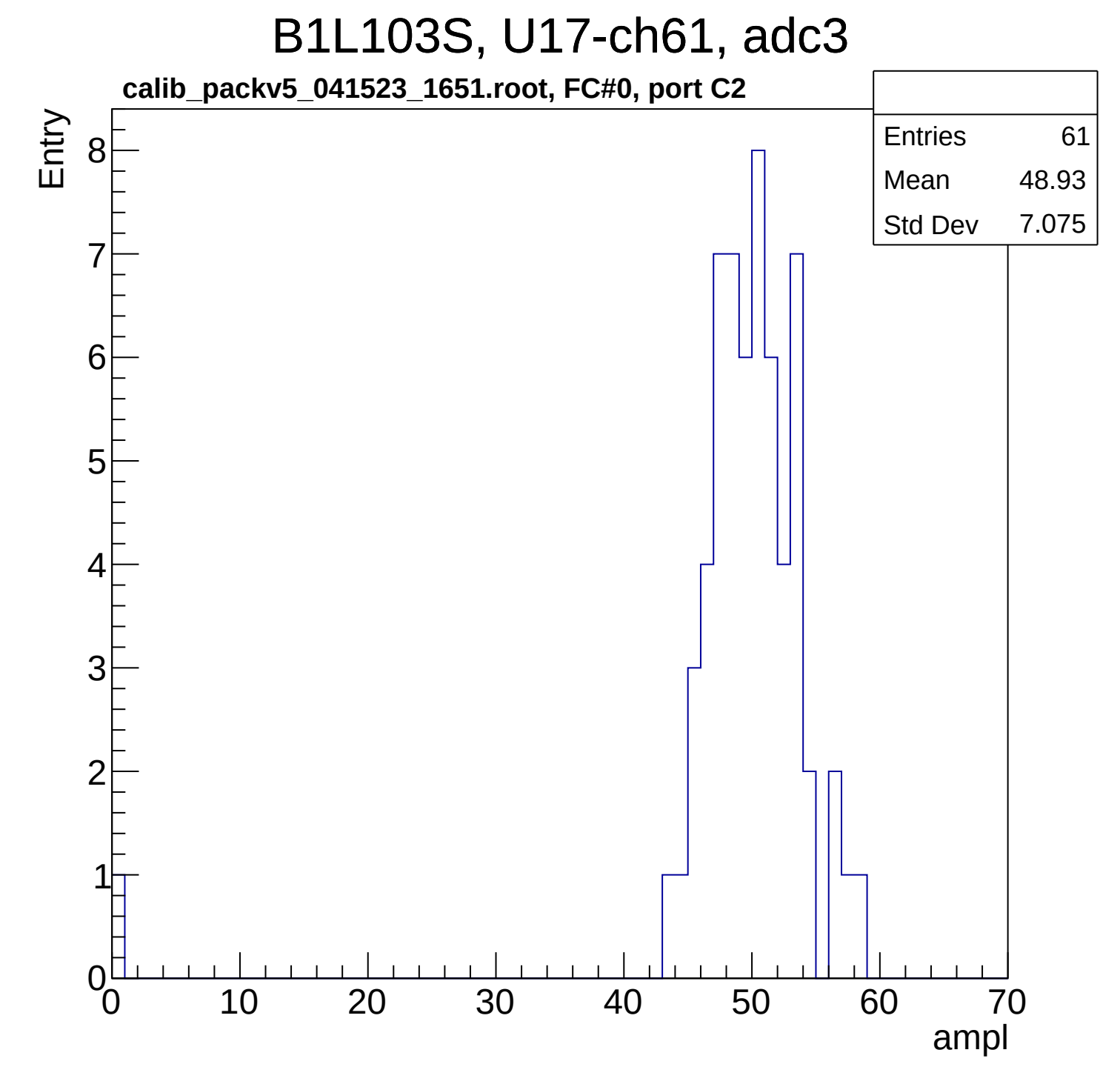

B1L103S, U17-ch60, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.33
Std Dev 15.39
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

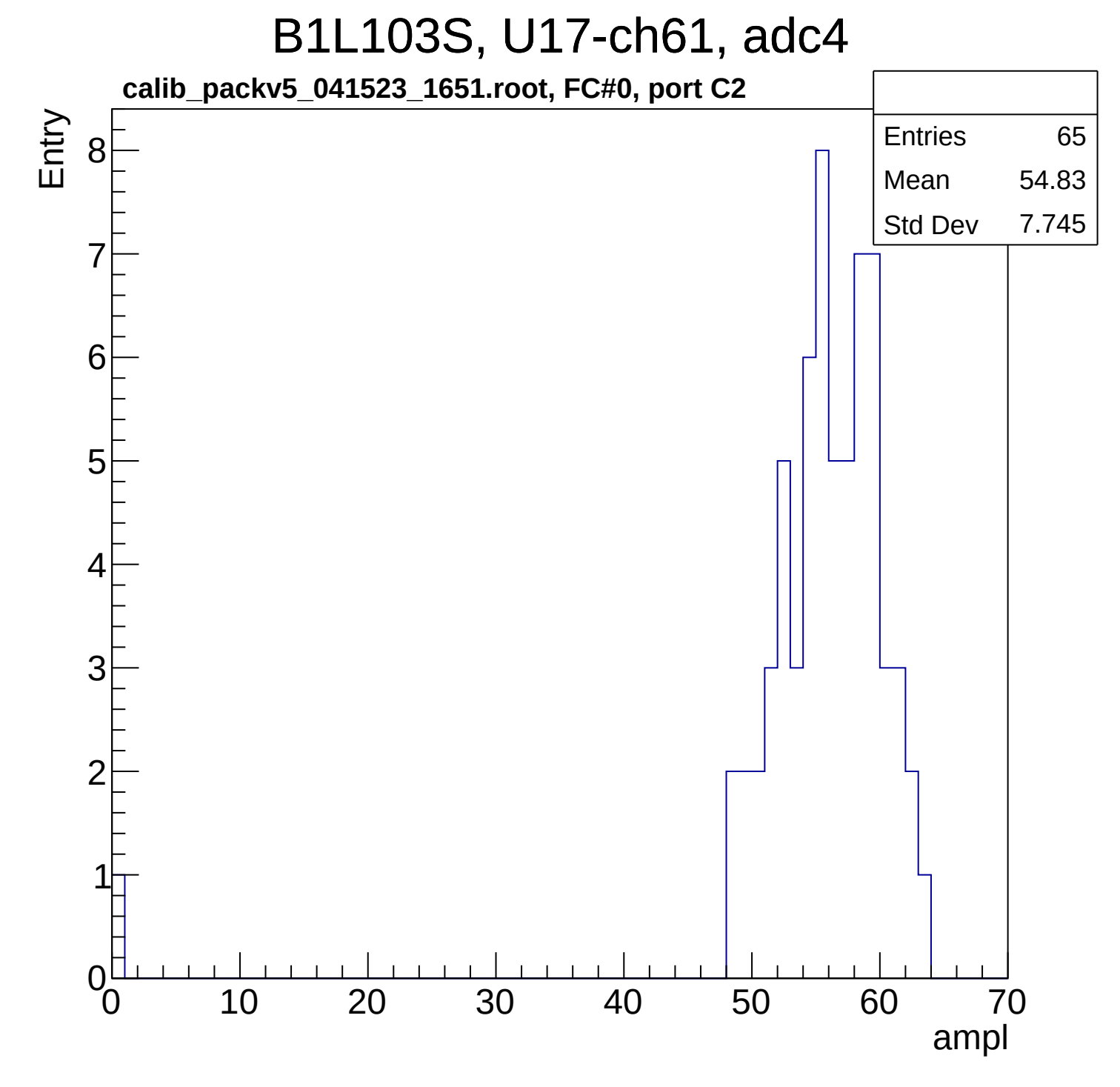

B1L103S, U17-ch60, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

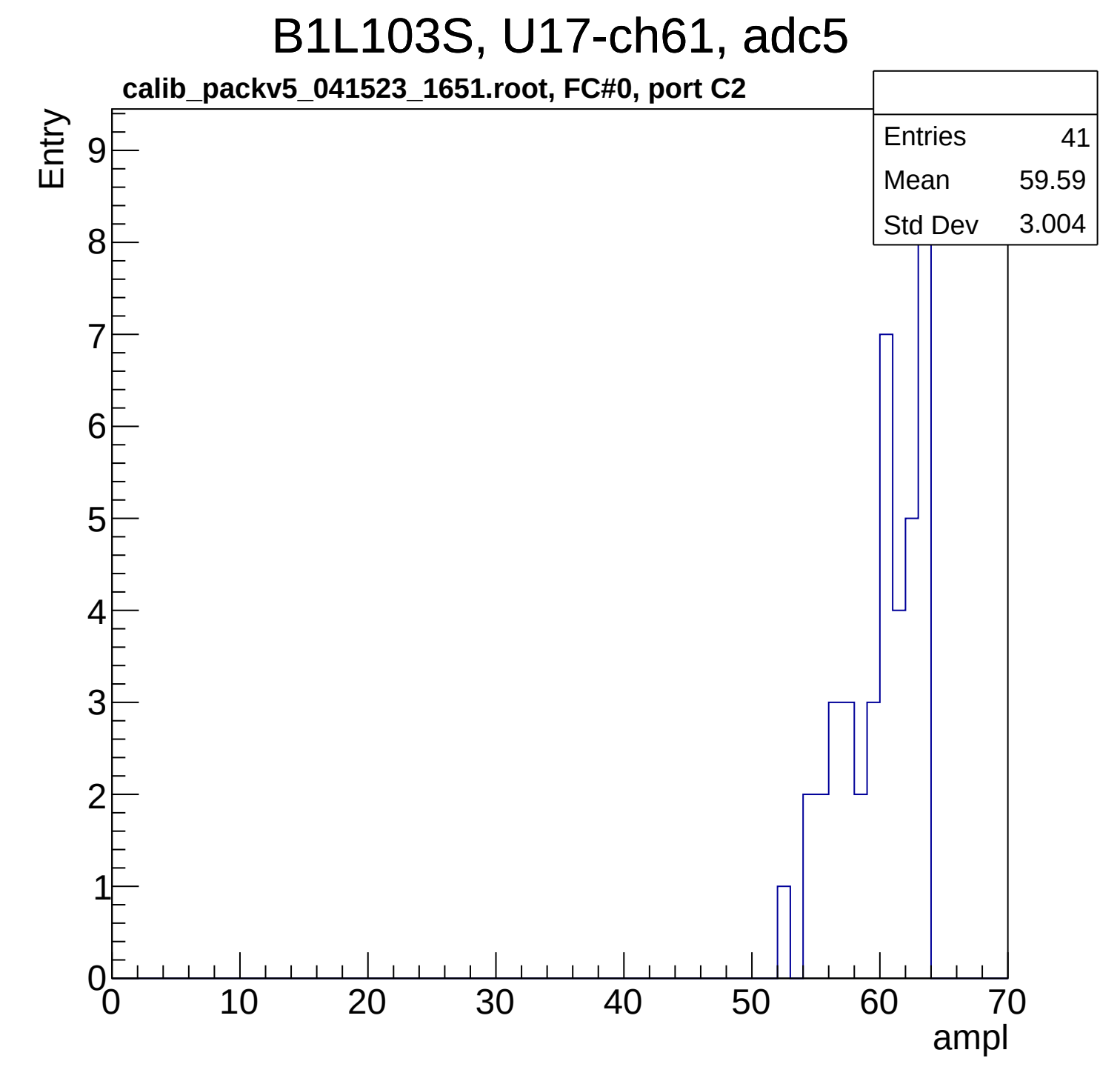

B1L103S, U17-ch61, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 20.1
Std Dev 13.62
Gaus mean : 29.4176
Gaus Width: 3.8765
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70

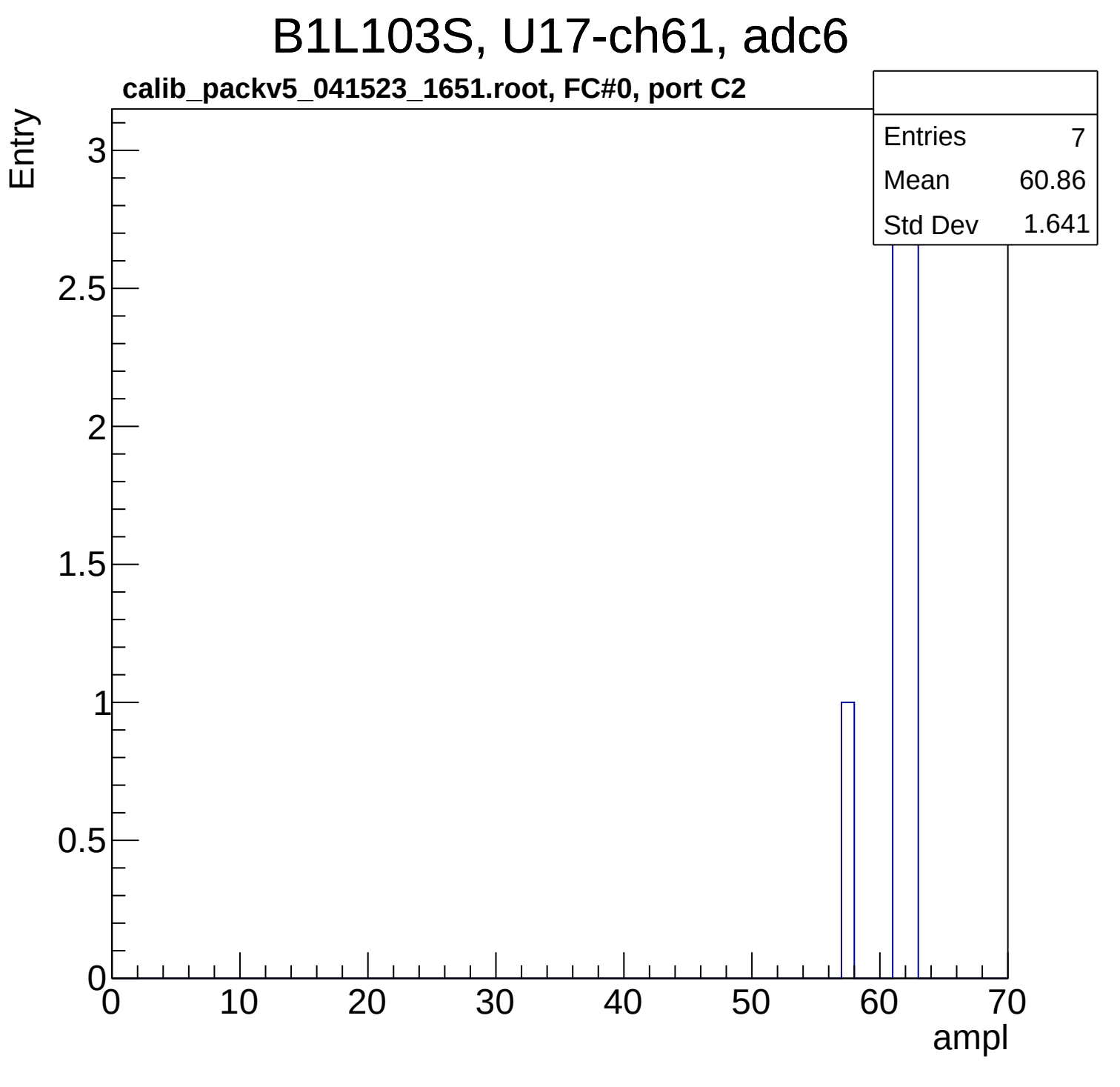

B1L103S, U17-ch61, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 31.36
Std Dev 12.02
Gaus mean : 36.3000
Gaus Width: 3.3579
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

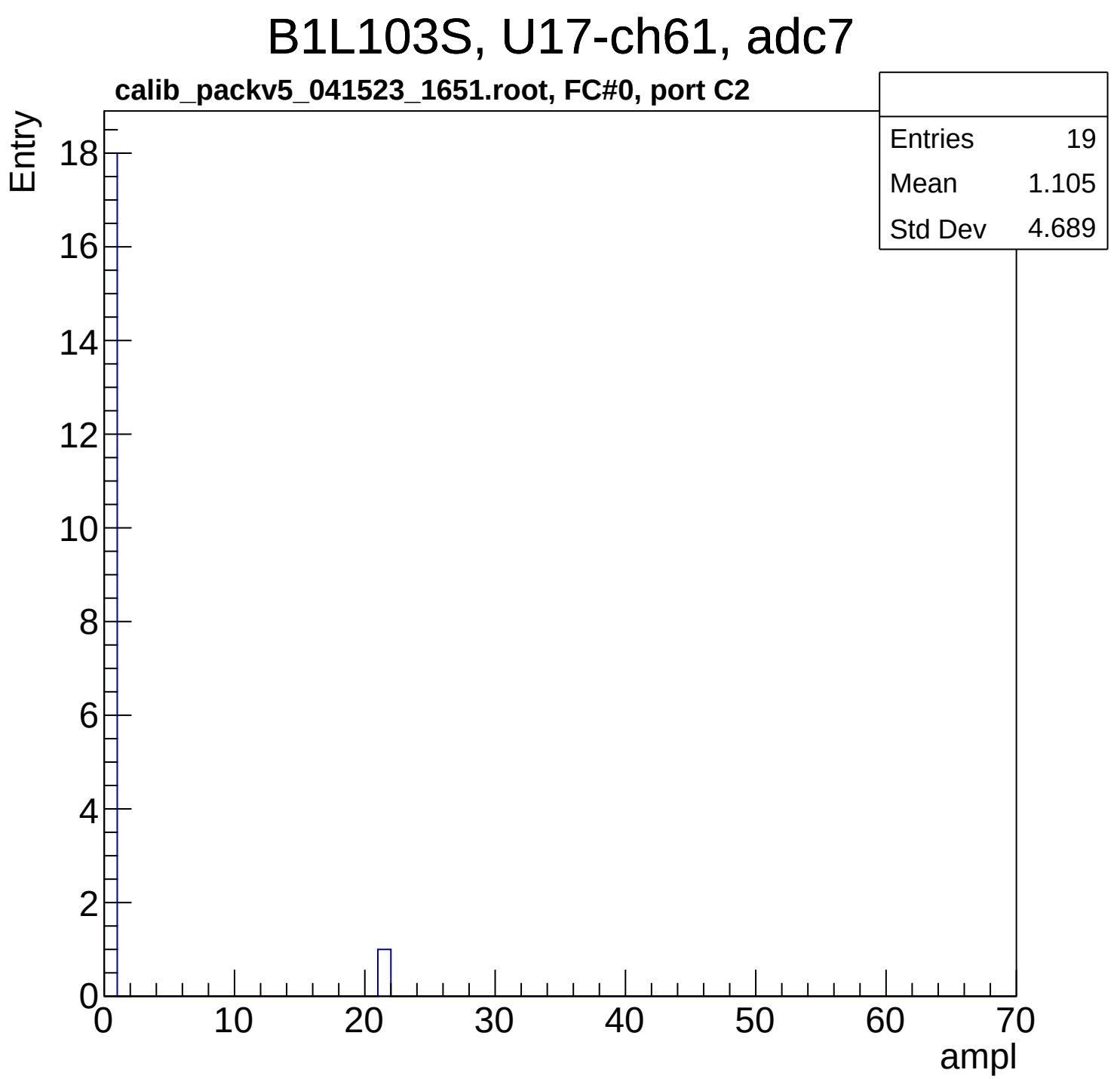

B1L103S, U17-ch61, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 40.3
Std Dev 9.992
Gaus mean : 42.7738
Gaus Width: 3.3909
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

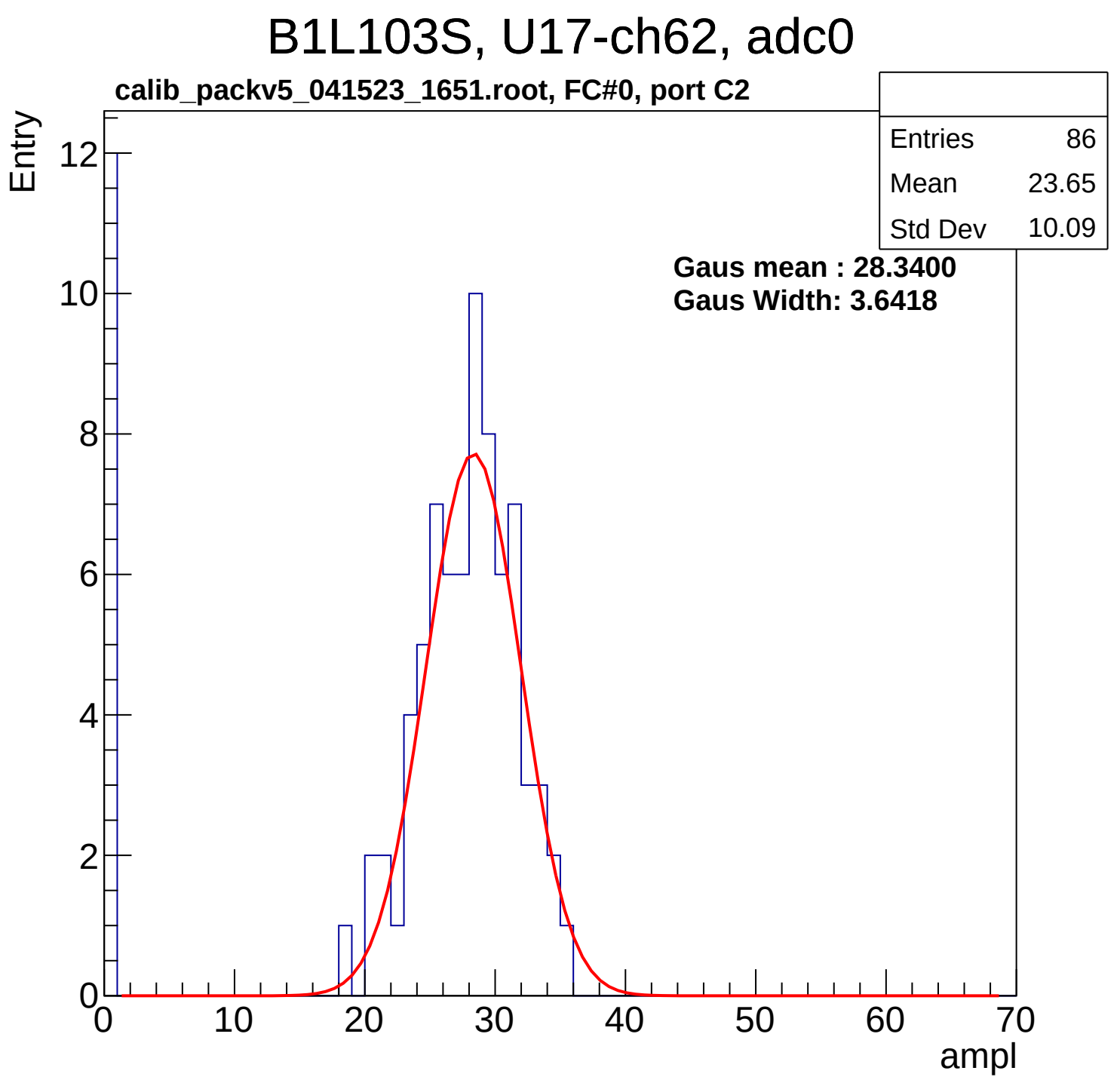

B1L103S, U17-ch61, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 48.93
Std Dev 7.075
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

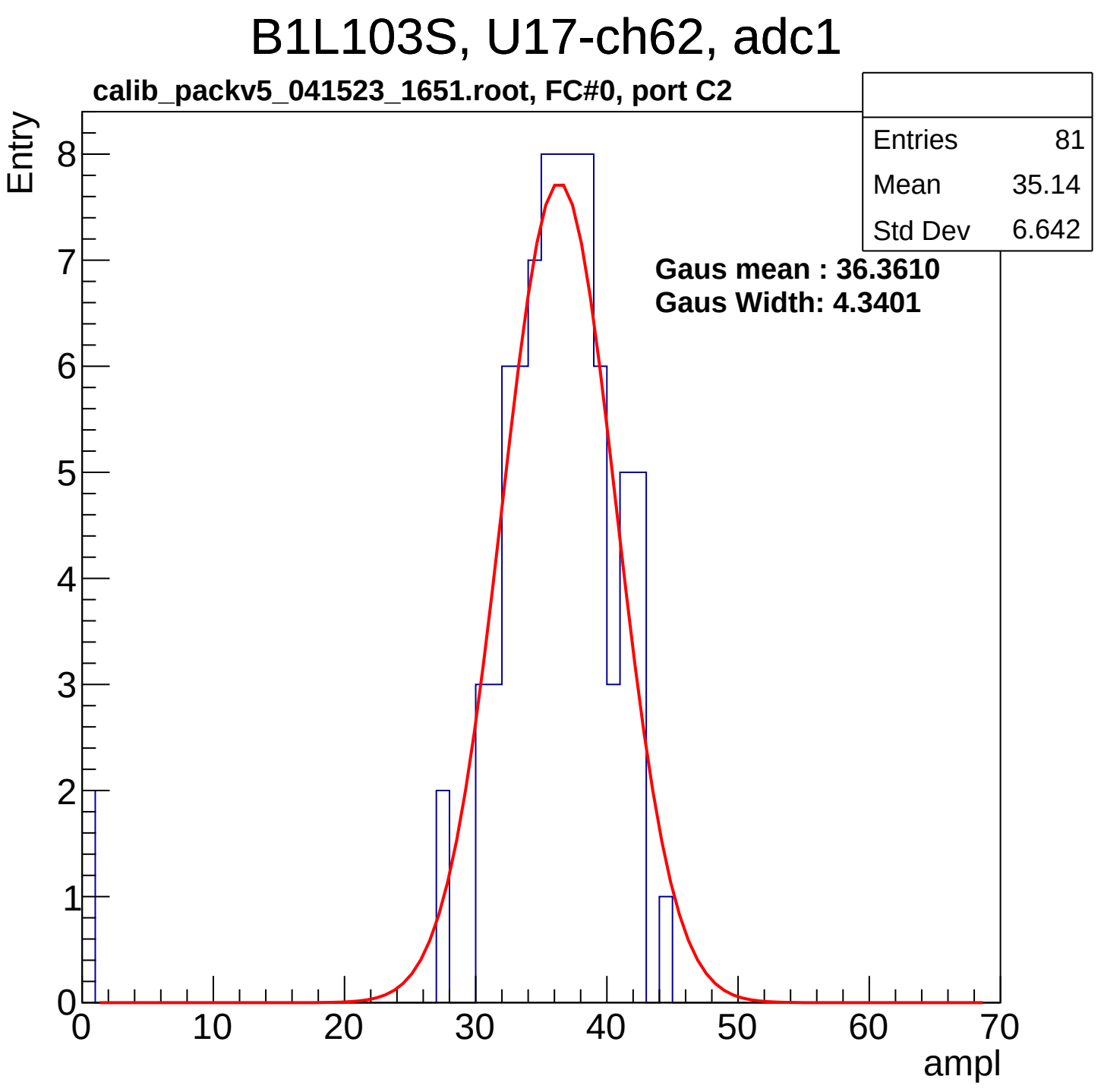

B1L103S, U17-ch61, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 54.83
Std Dev 7.745
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

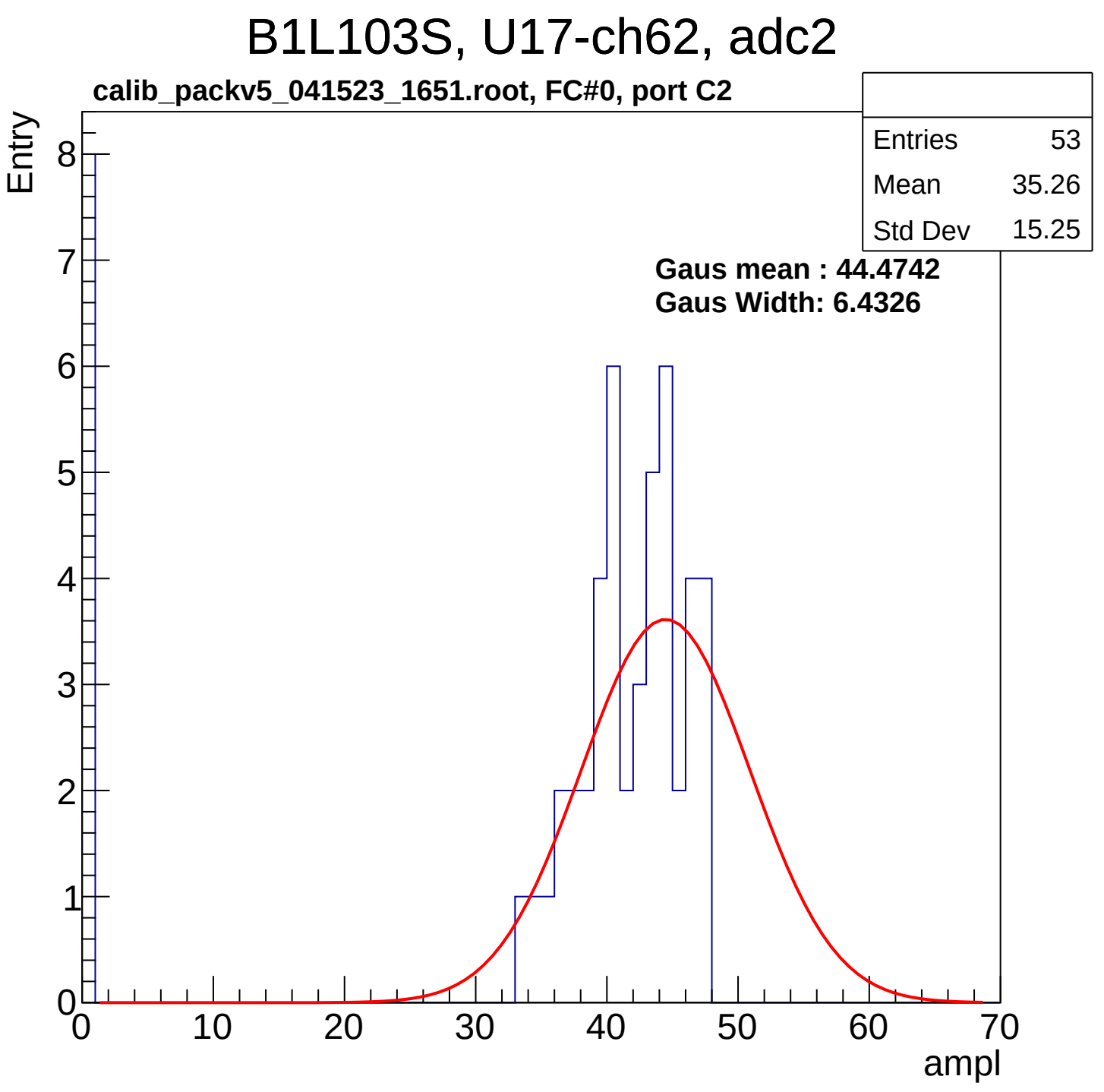

B1L103S, U17-ch61, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 59.59
Std Dev 3.004
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

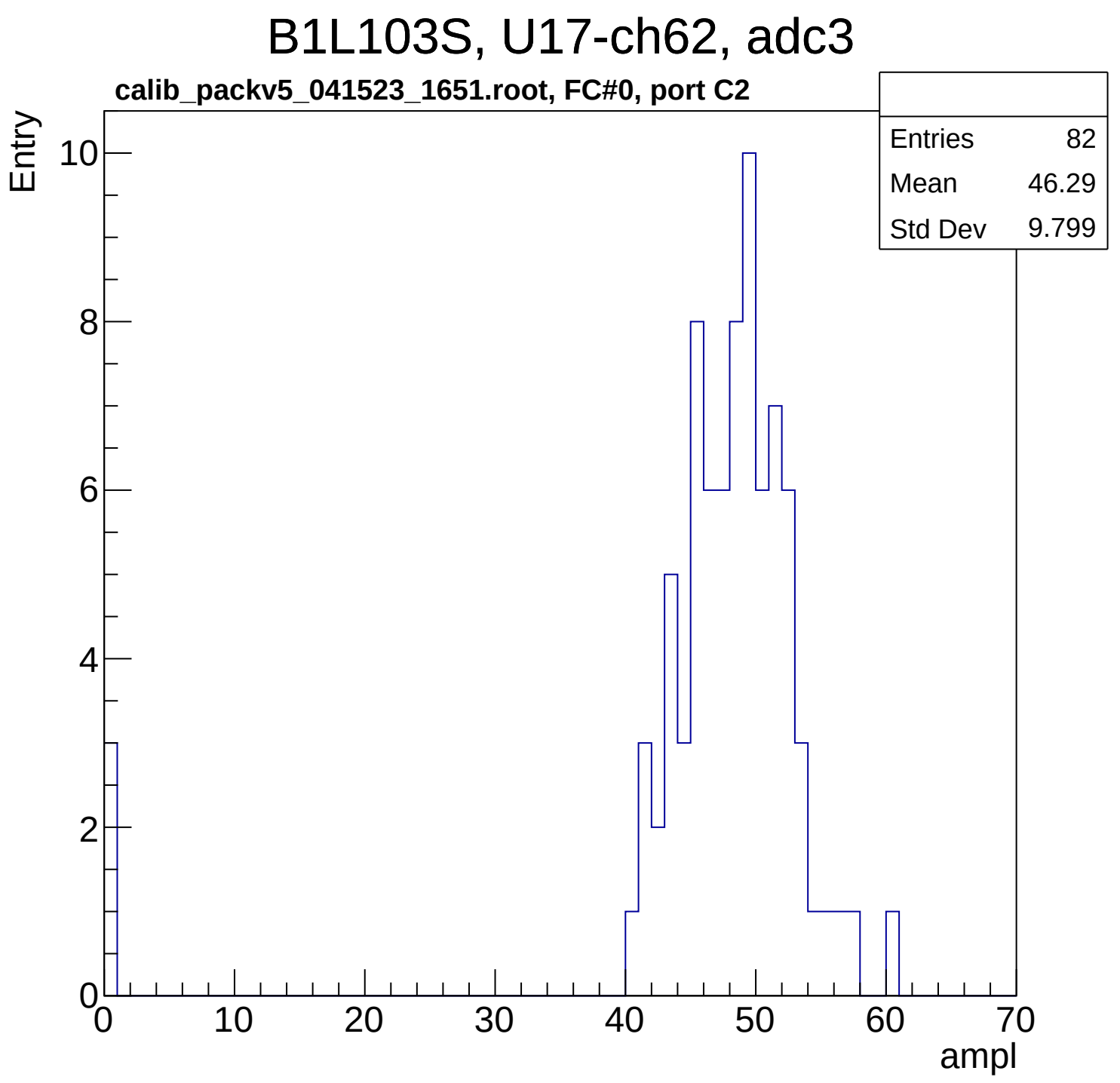

B1L103S, U17-ch61, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 60.86
Std Dev 1.641
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

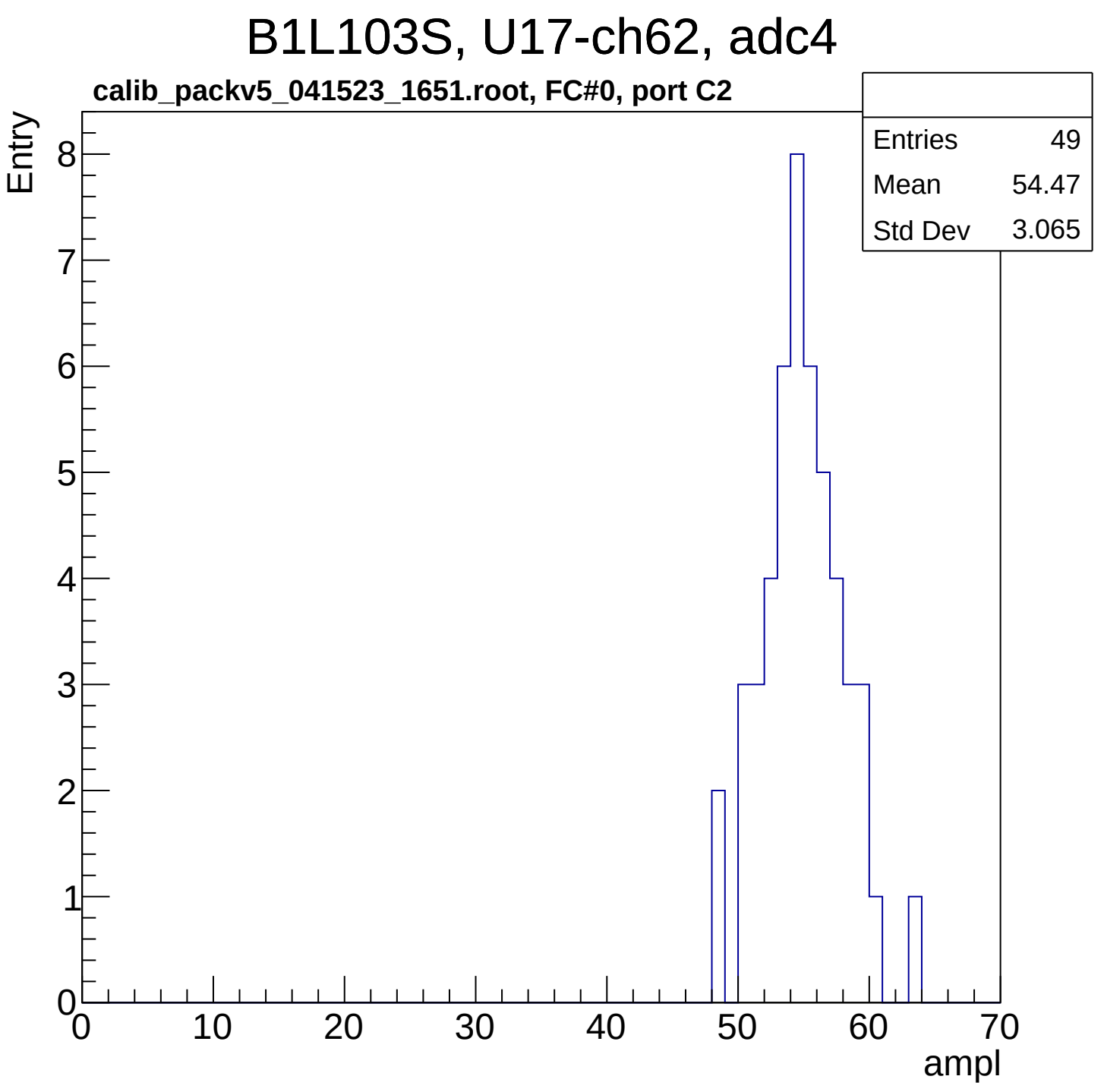

B1L103S, U17-ch61, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

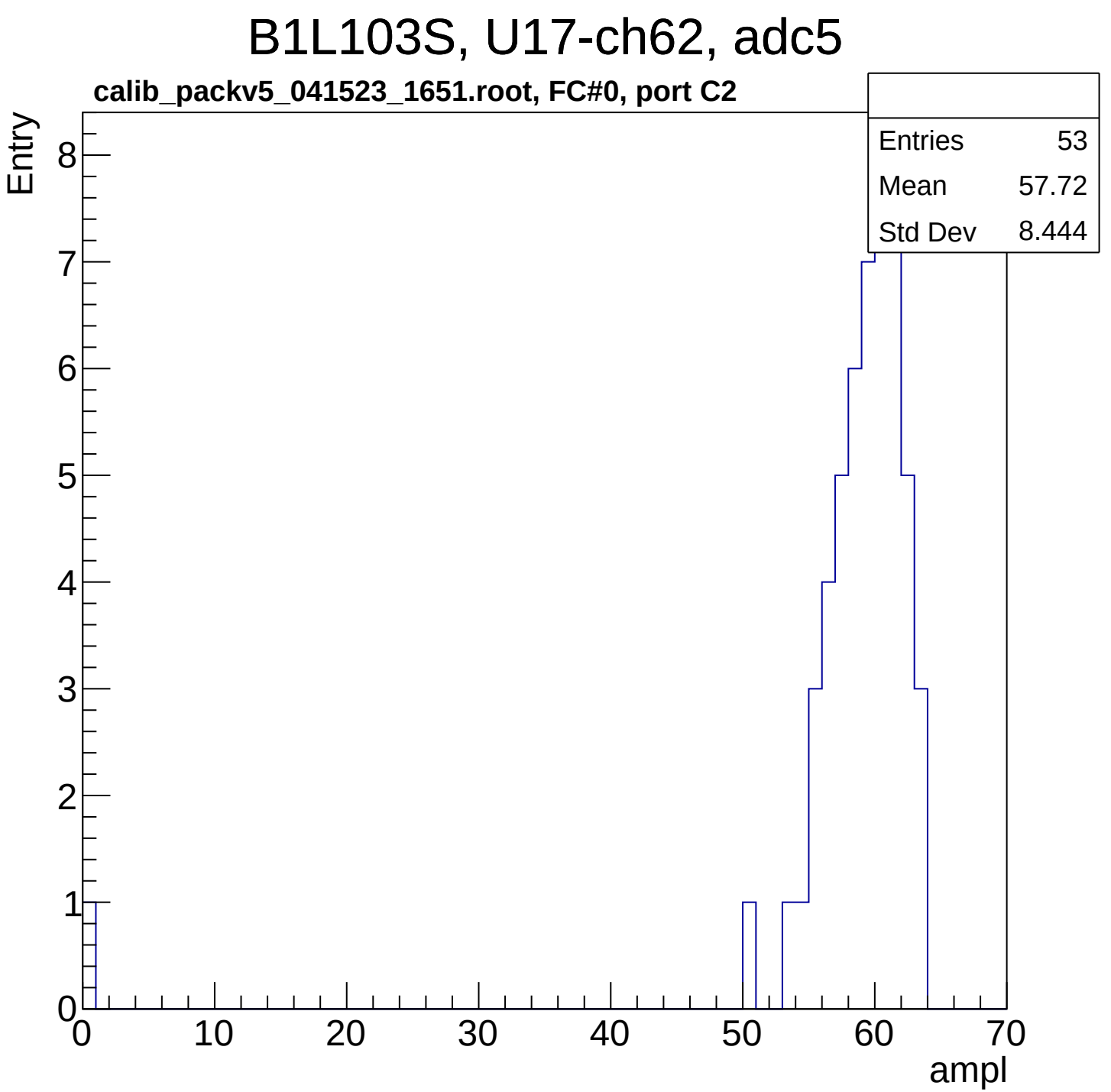

B1L103S, U17-ch62, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 23.65
Std Dev 10.09
Gaus mean : 28.3400
Gaus Width: 3.6418
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

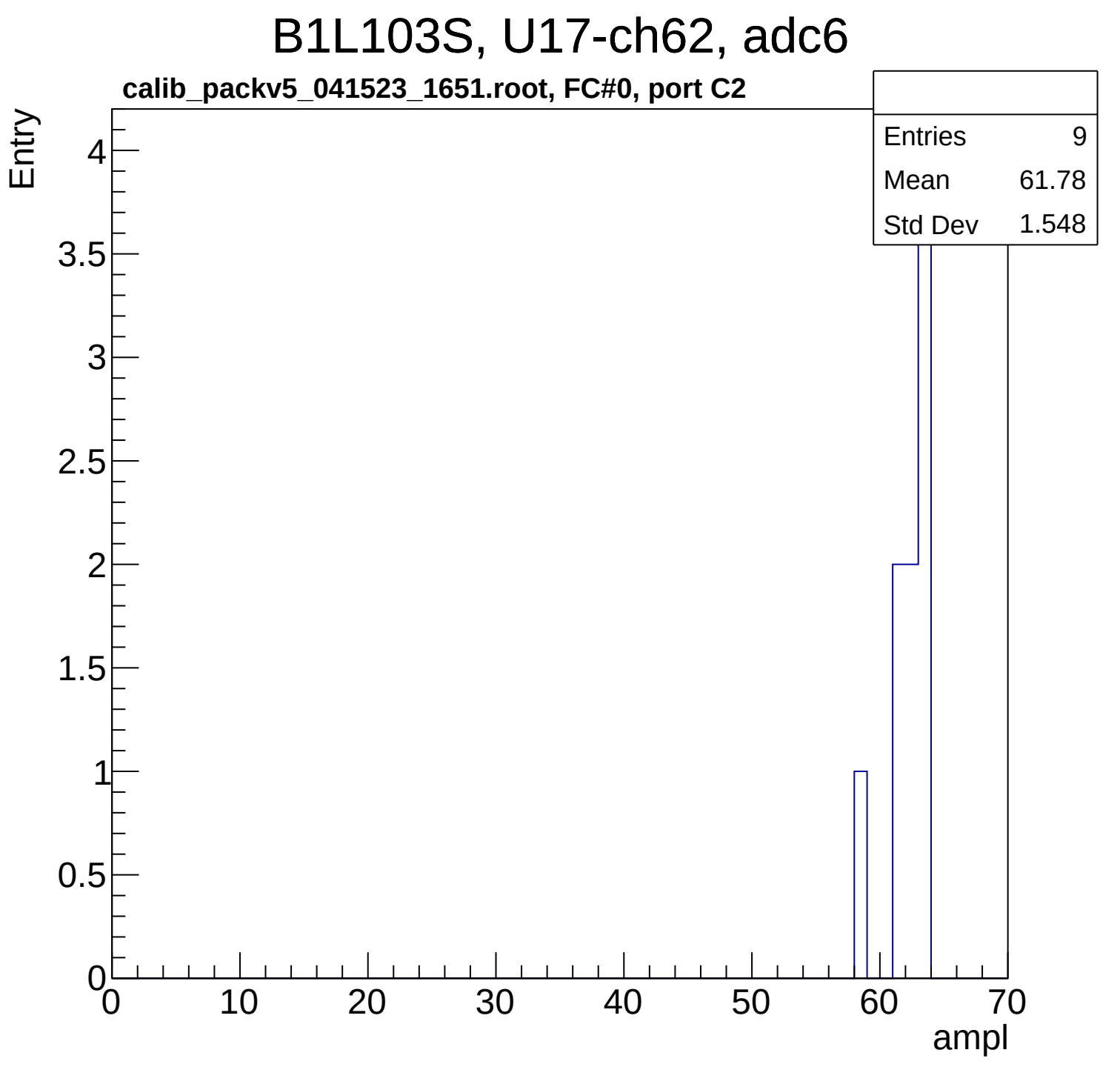

B1L103S, U17-ch62, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 35.14
Std Dev 6.642
Gaus mean : 36.3610
Gaus Width: 4.3401
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

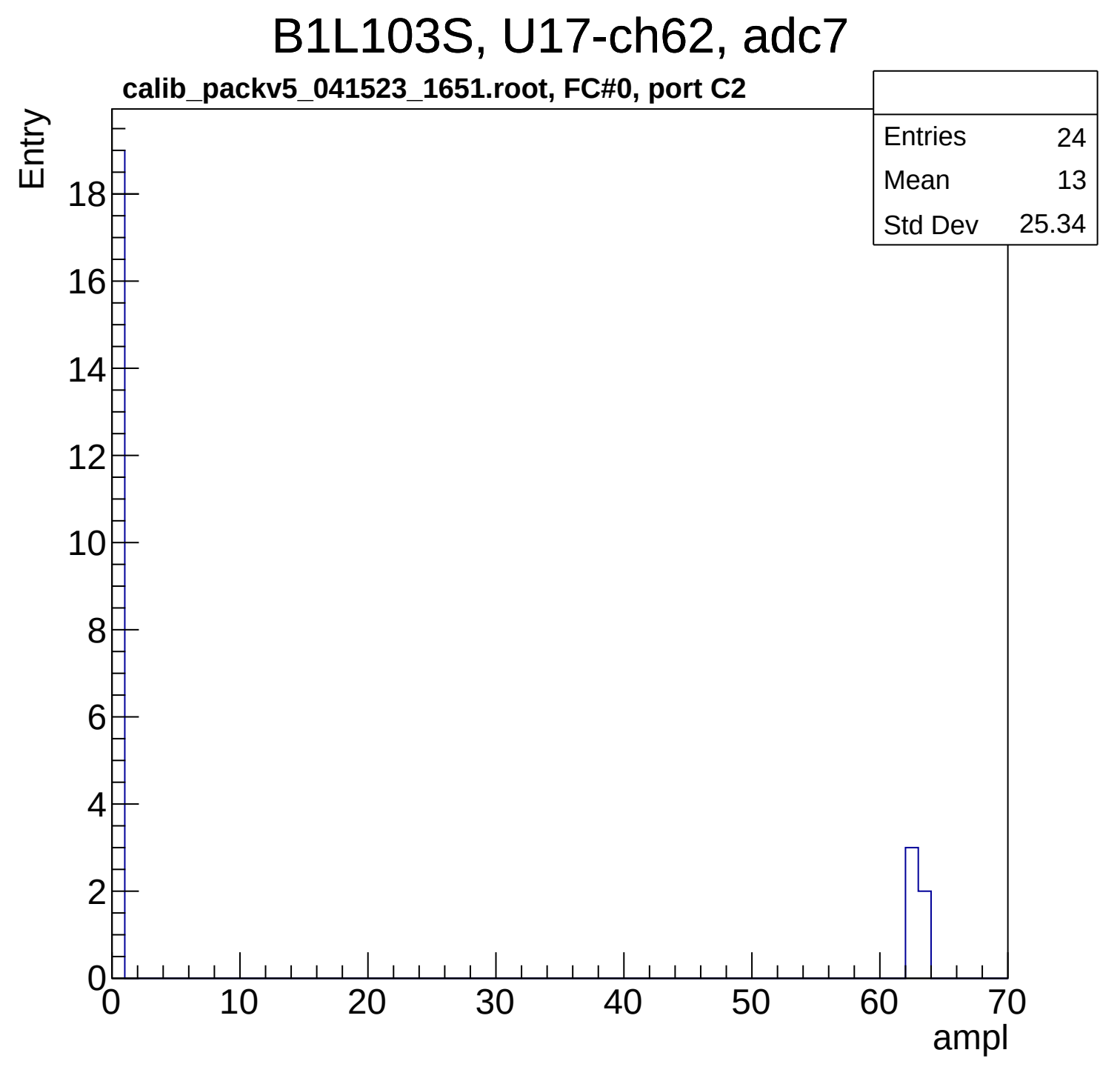

B1L103S, U17-ch62, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 35.26
Std Dev 15.25
Gaus mean : 44.4742
Gaus Width: 6.4326
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

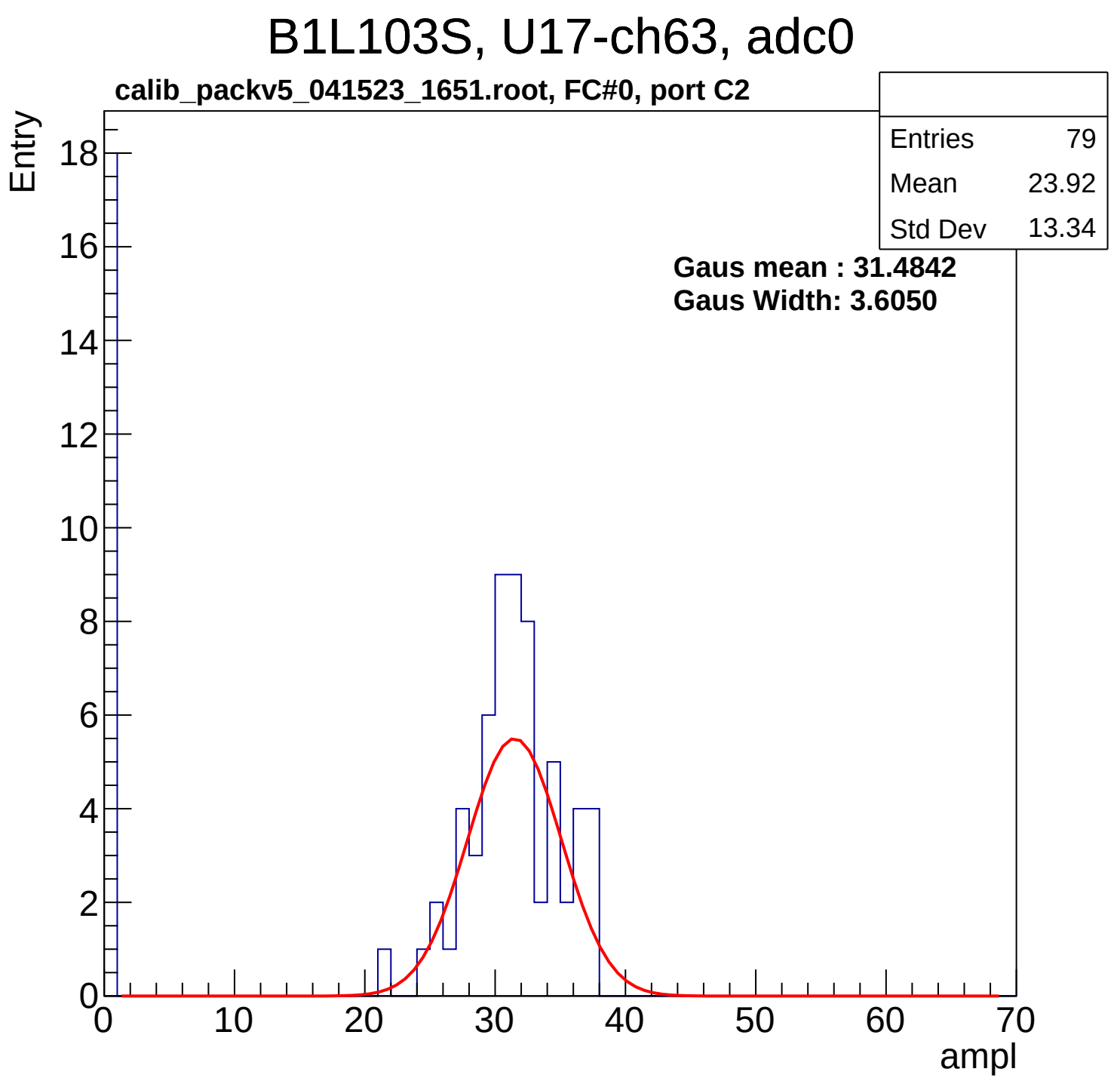

B1L103S, U17-ch62, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 46.29
Std Dev 9.799
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

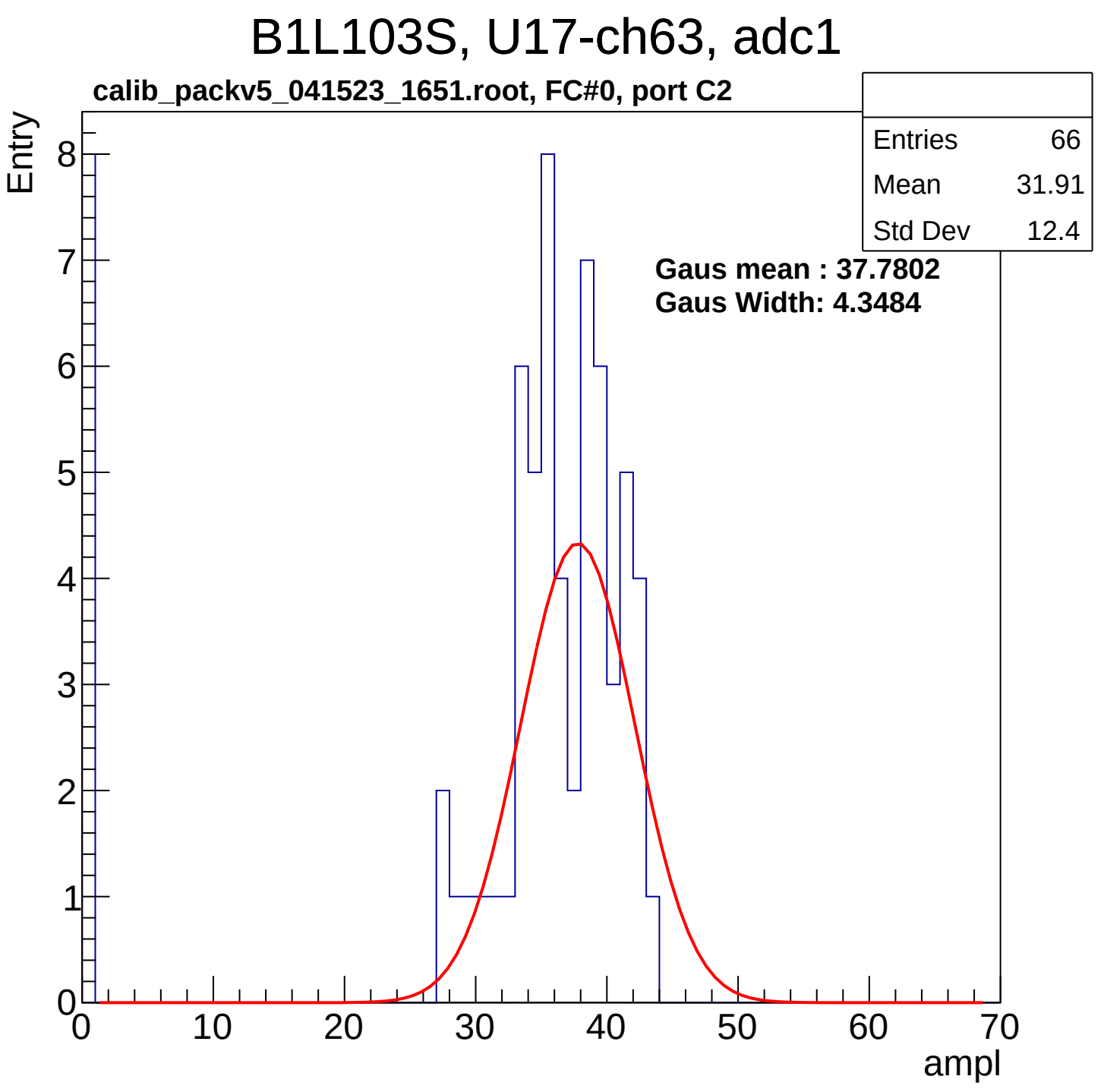

B1L103S, U17-ch62, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 54.47
Std Dev 3.065
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

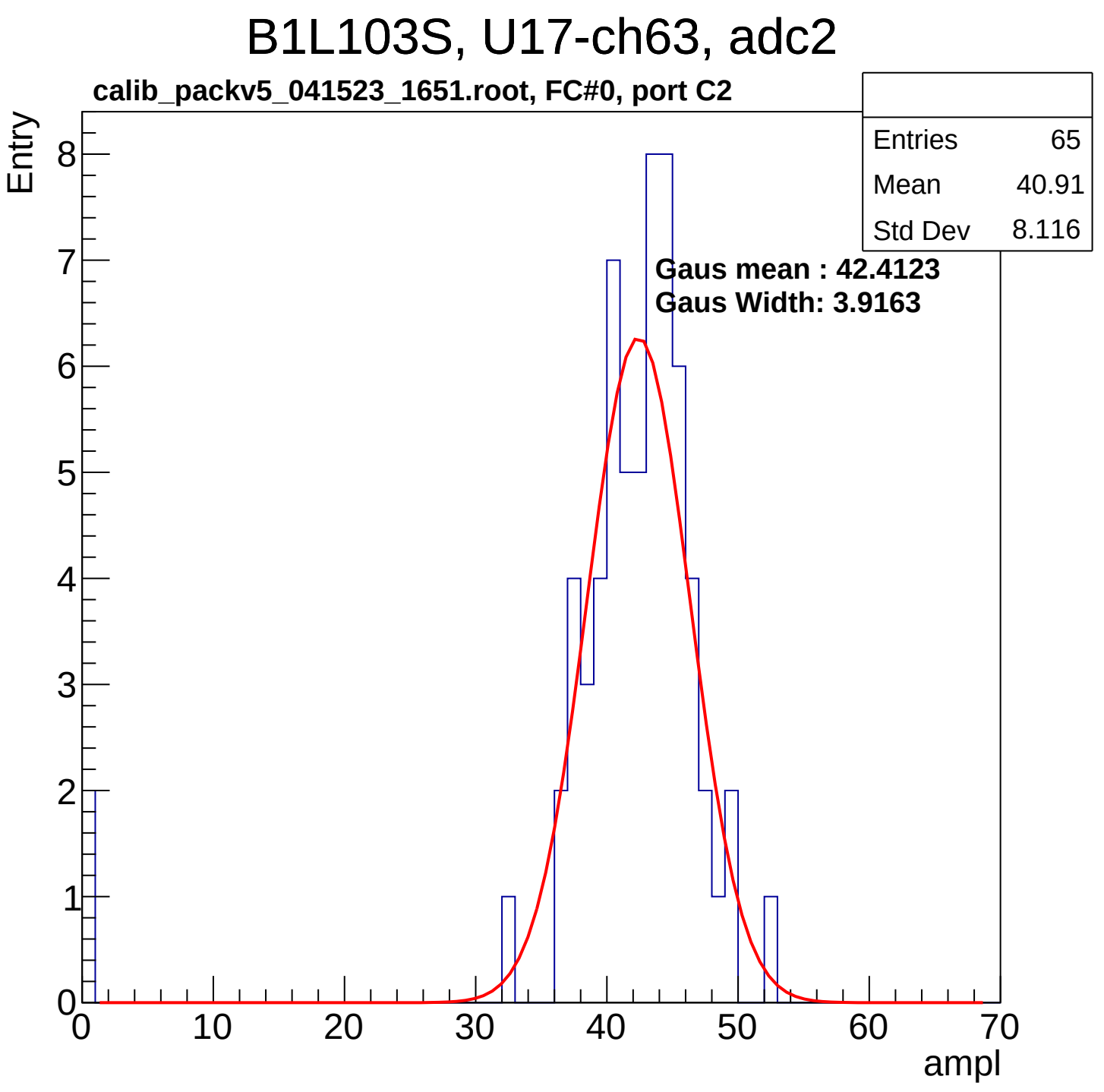

B1L103S, U17-ch62, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 57.72
Std Dev 8.444
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

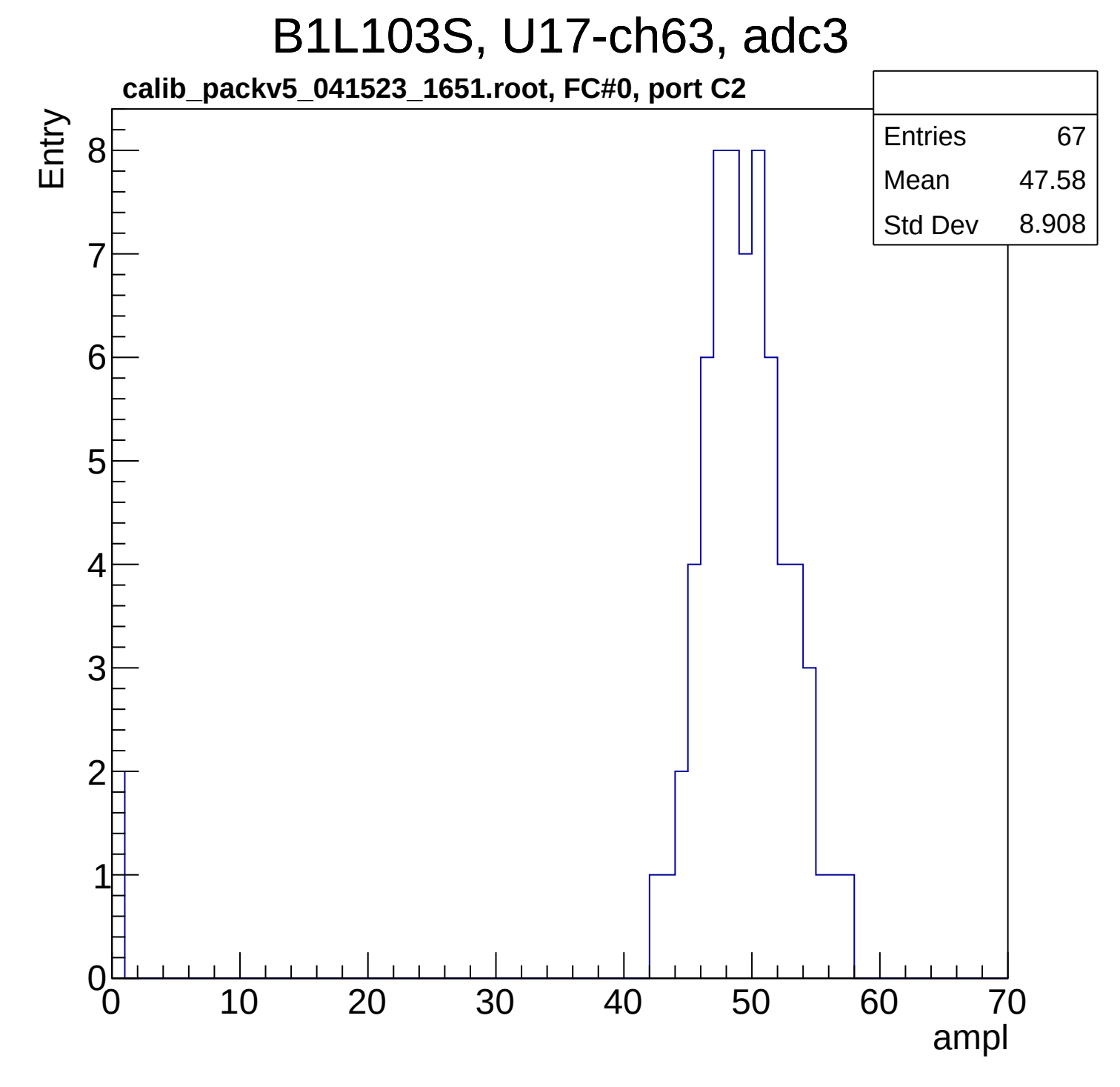

B1L103S, U17-ch62, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.78
Std Dev 1.548
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

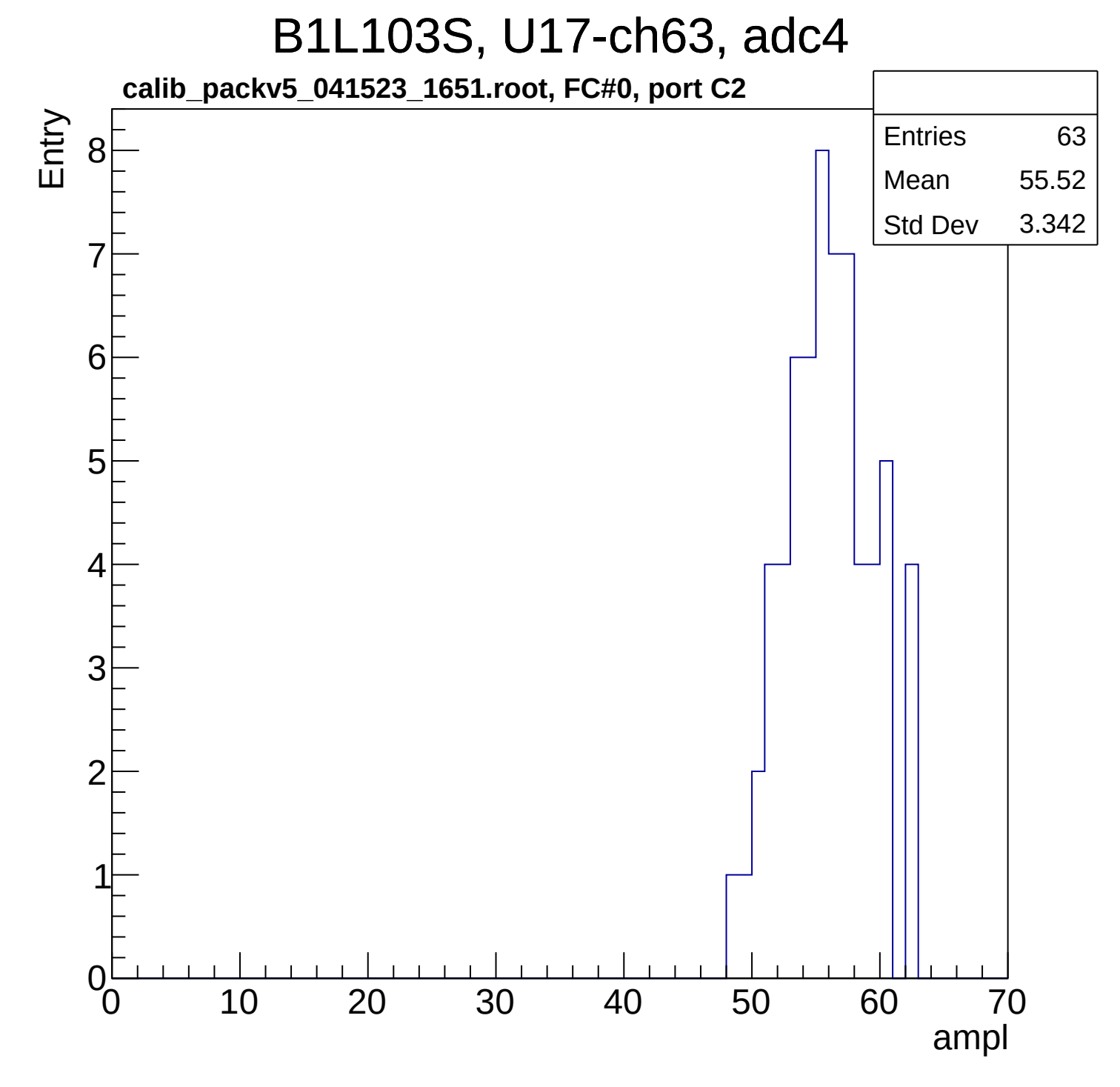

B1L103S, U17-ch62, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 13
Std Dev 25.34
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

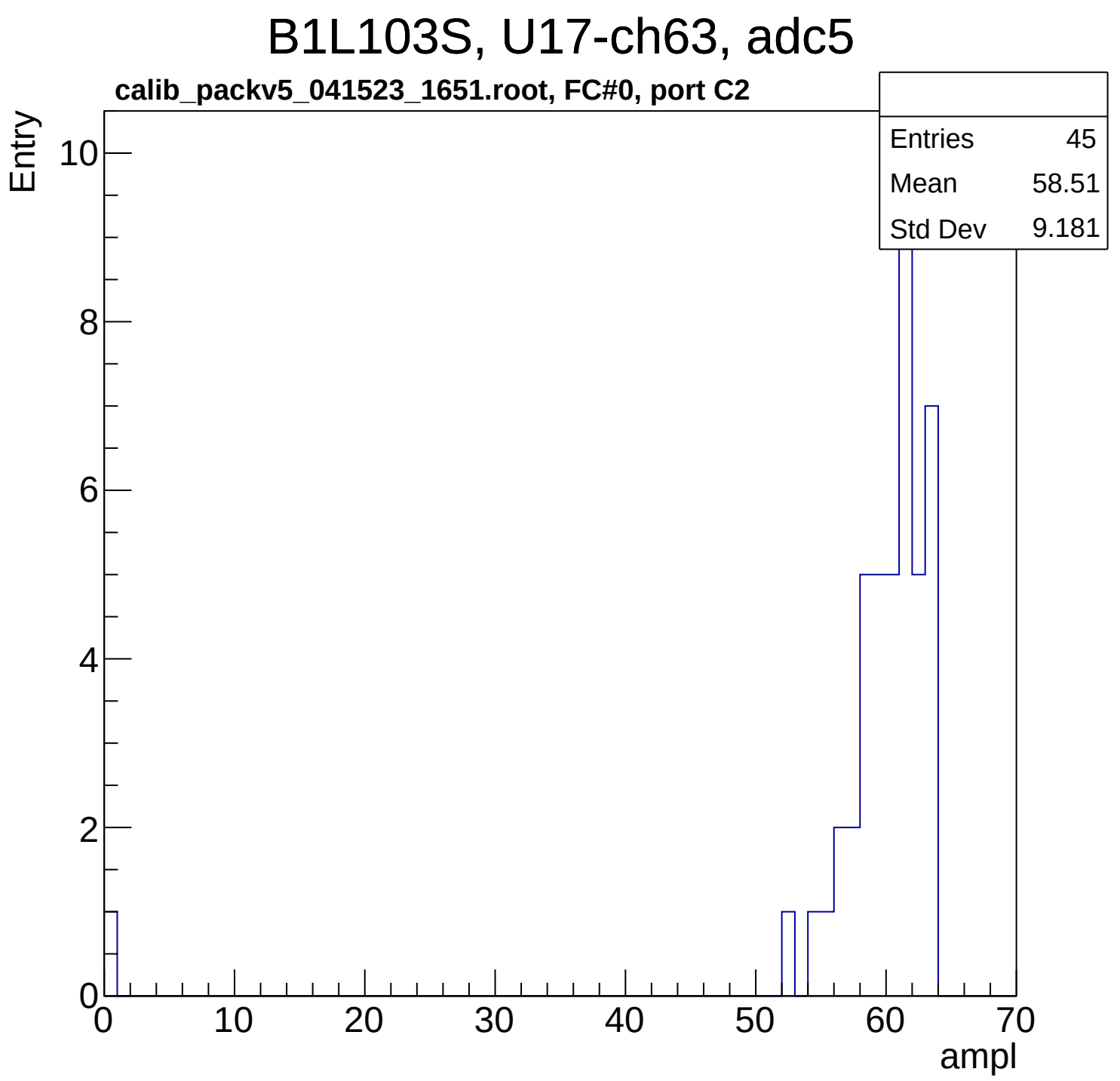

B1L103S, U17-ch63, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 23.92
Std Dev 13.34
Gaus mean : 31.4842
Gaus Width: 3.6050
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

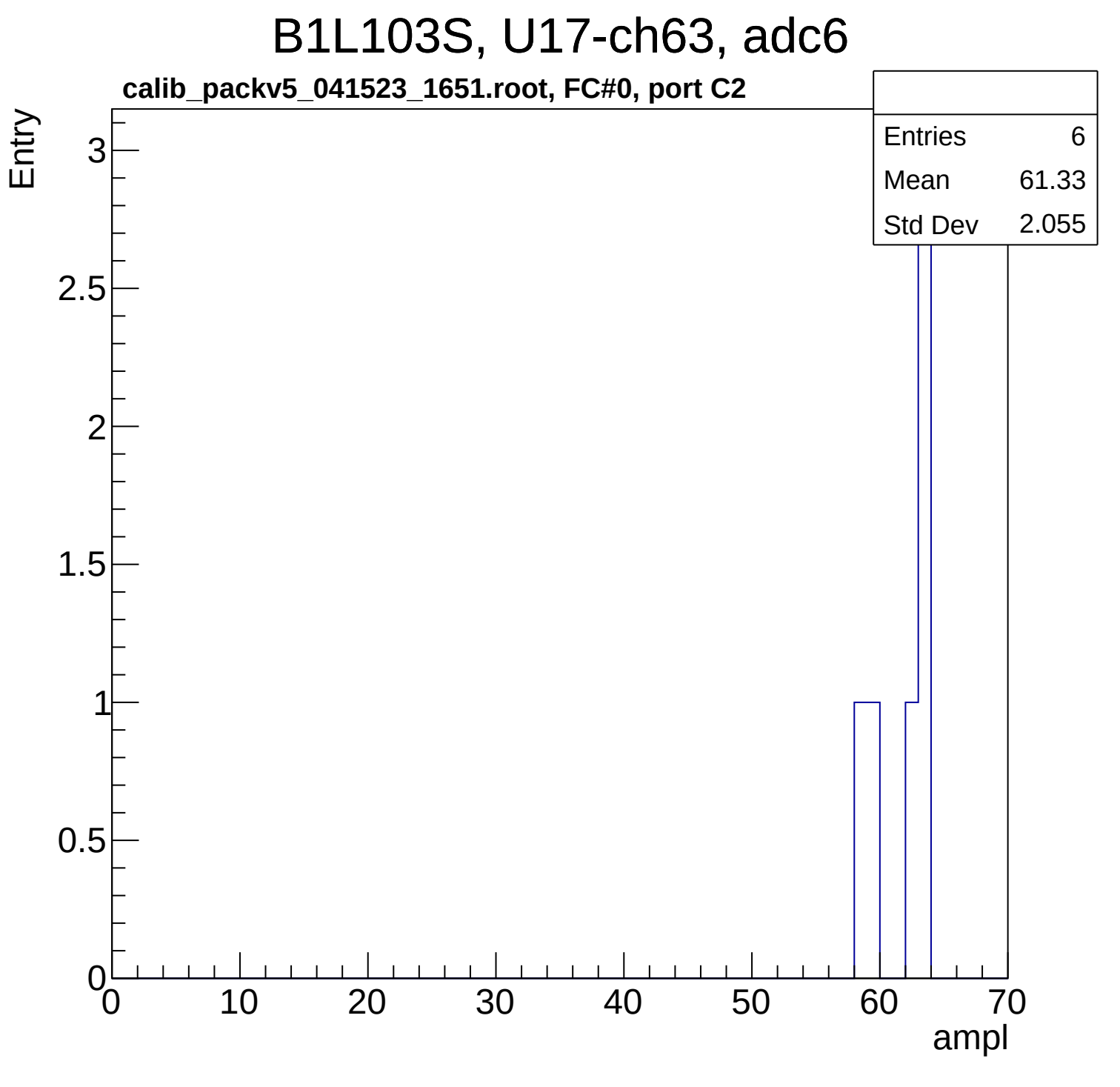

B1L103S, U17-ch63, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 31.91
Std Dev 12.4
Gaus mean : 37.7802
Gaus Width: 4.3484
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

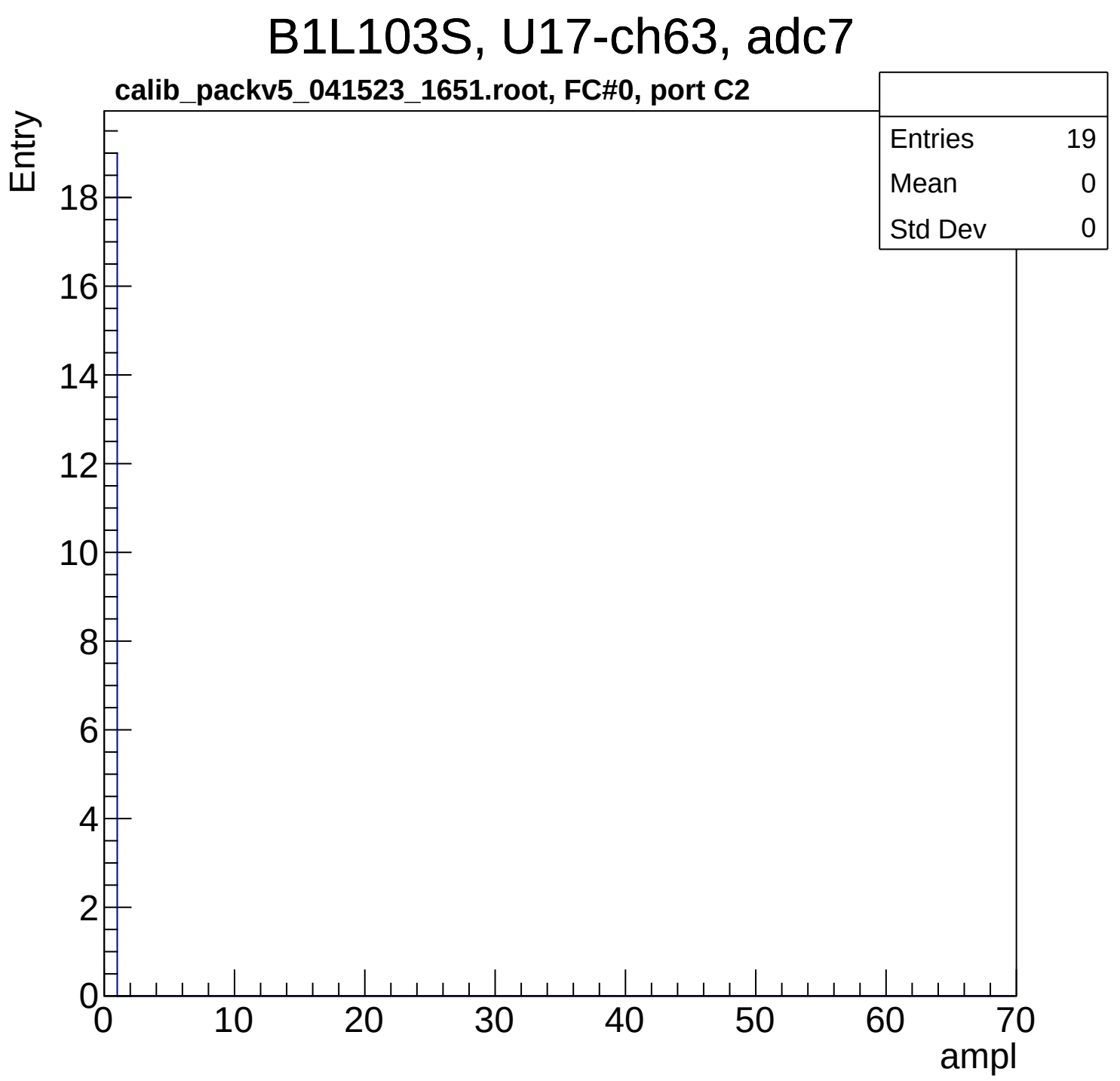

B1L103S, U17-ch63, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 40.91
Std Dev 8.116
Gaus mean : 42.4123
Gaus Width: 3.9163
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

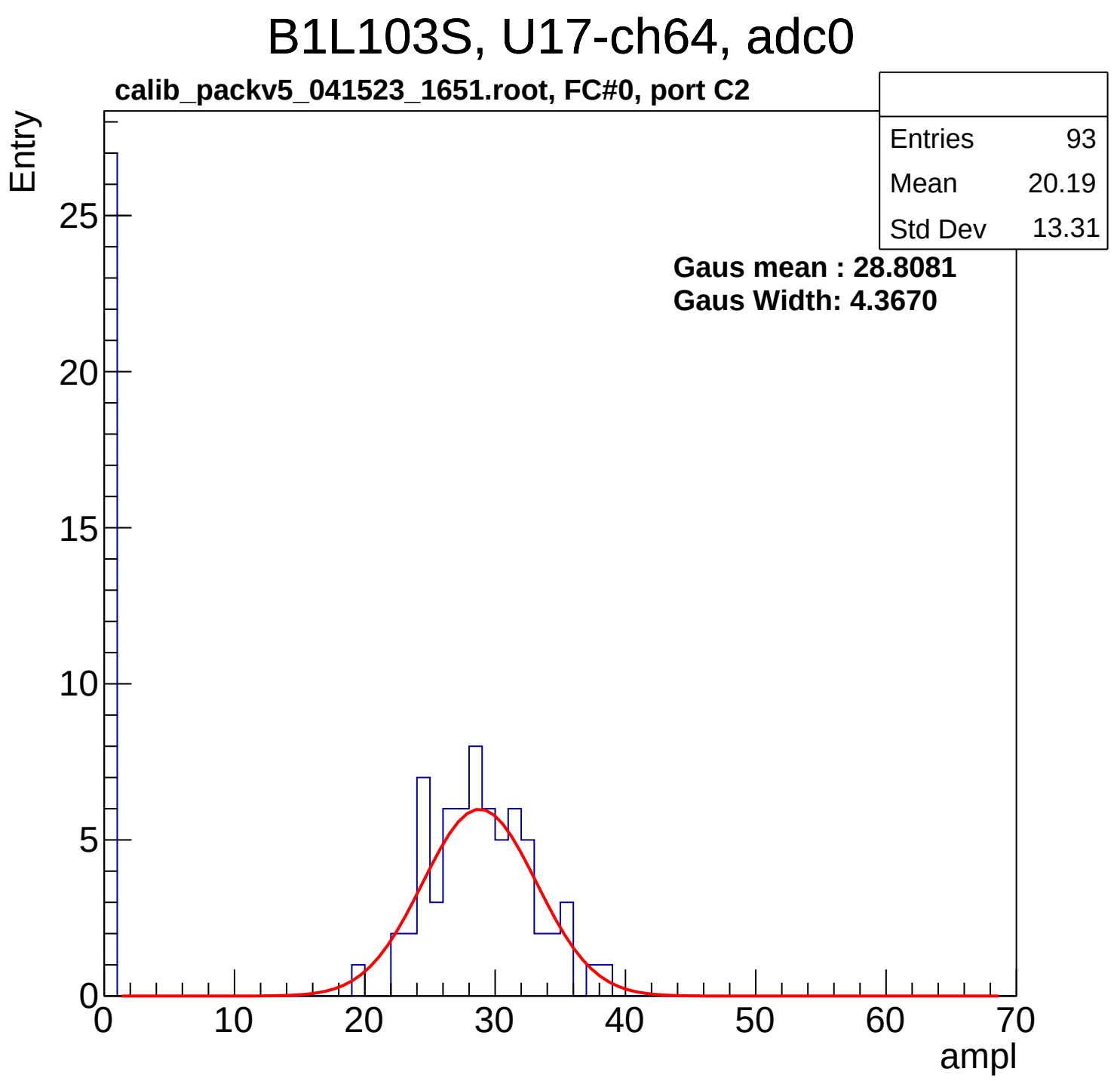

B1L103S, U17-ch63, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 47.58
Std Dev 8.908
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

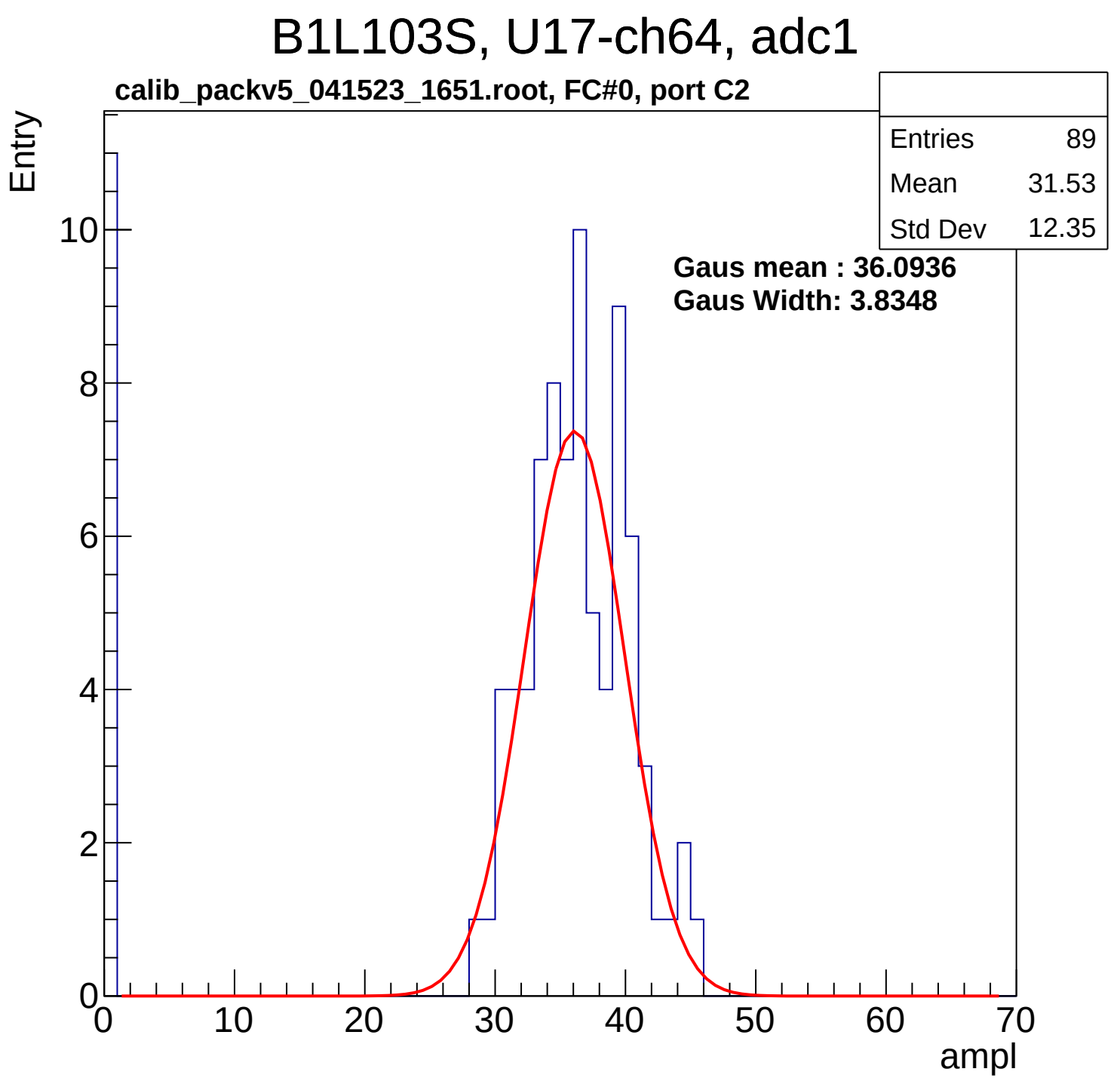

B1L103S, U17-ch63, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 55.52
Std Dev 3.342
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

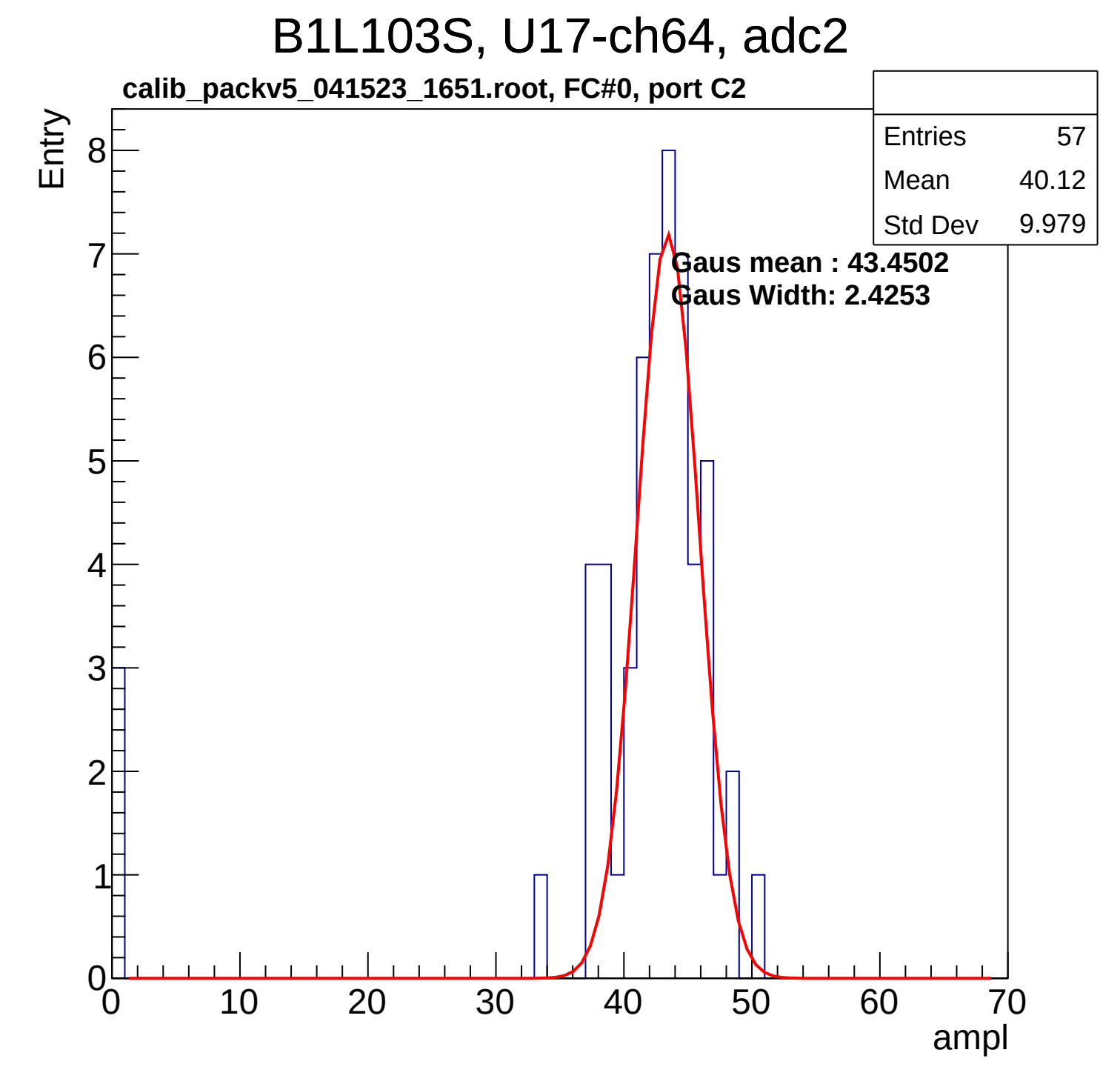

B1L103S, U17-ch63, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.51
Std Dev 9.181
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

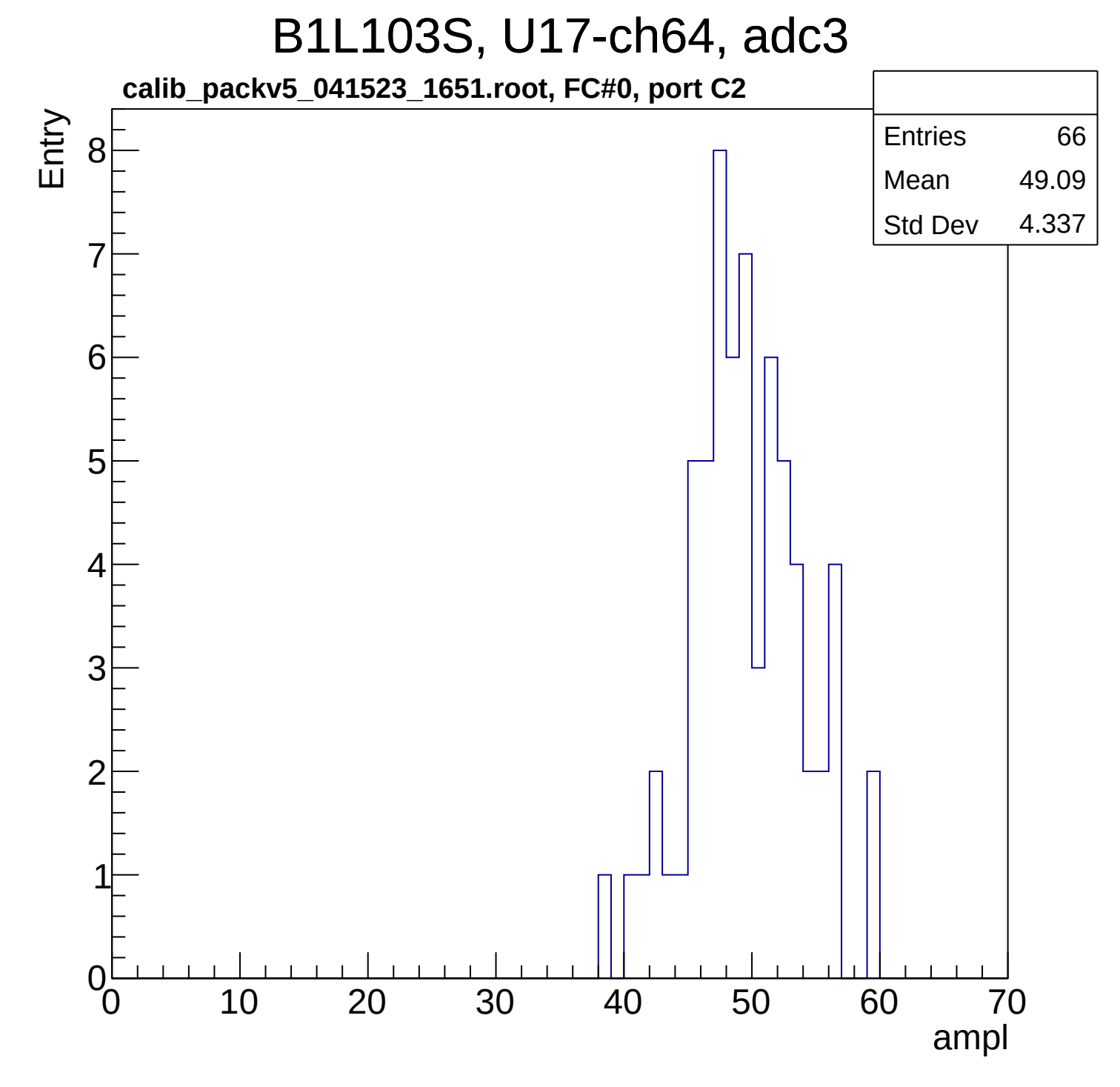

B1L103S, U17-ch63, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.33
Std Dev 2.055
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

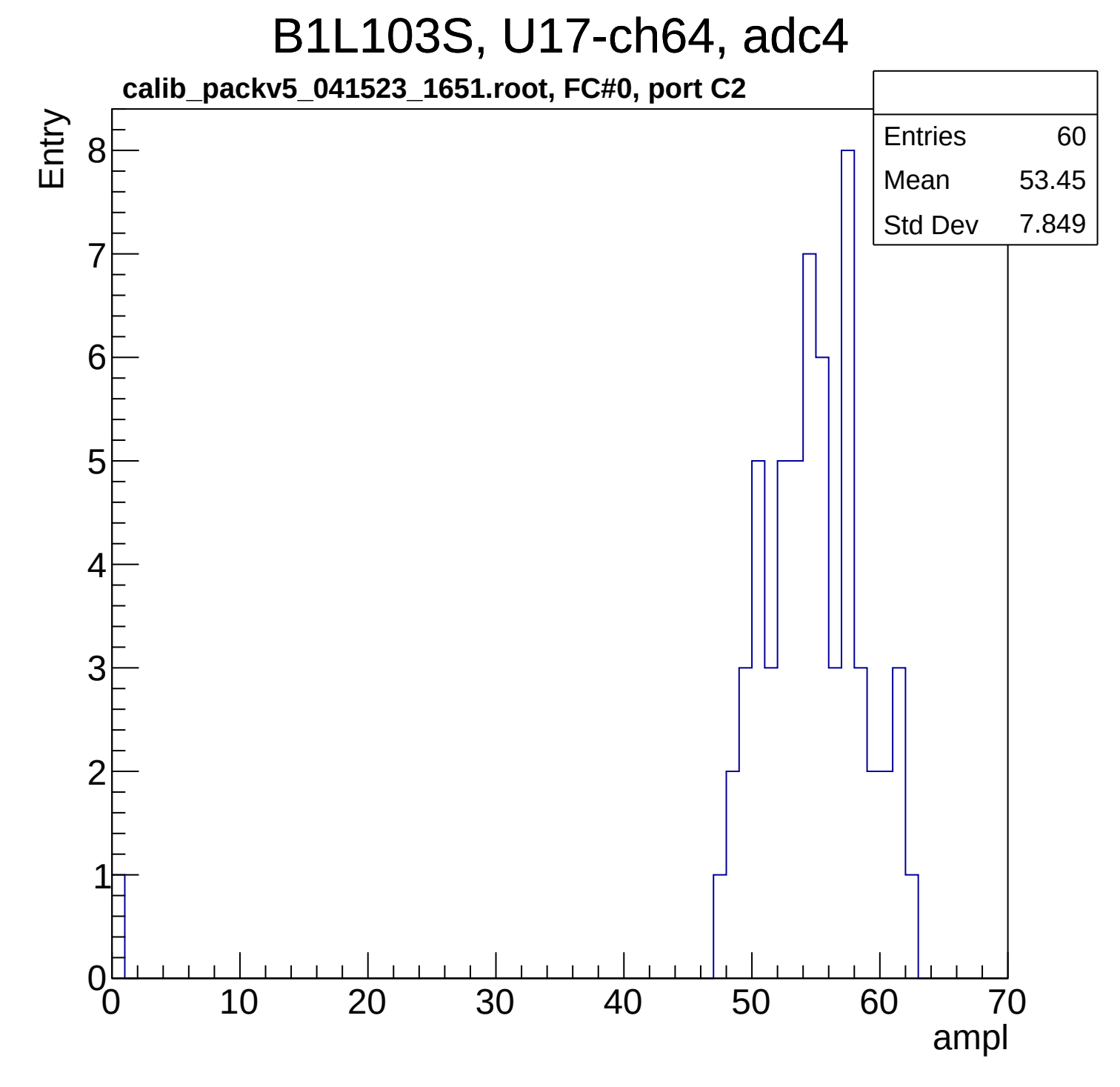

B1L103S, U17-ch63, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

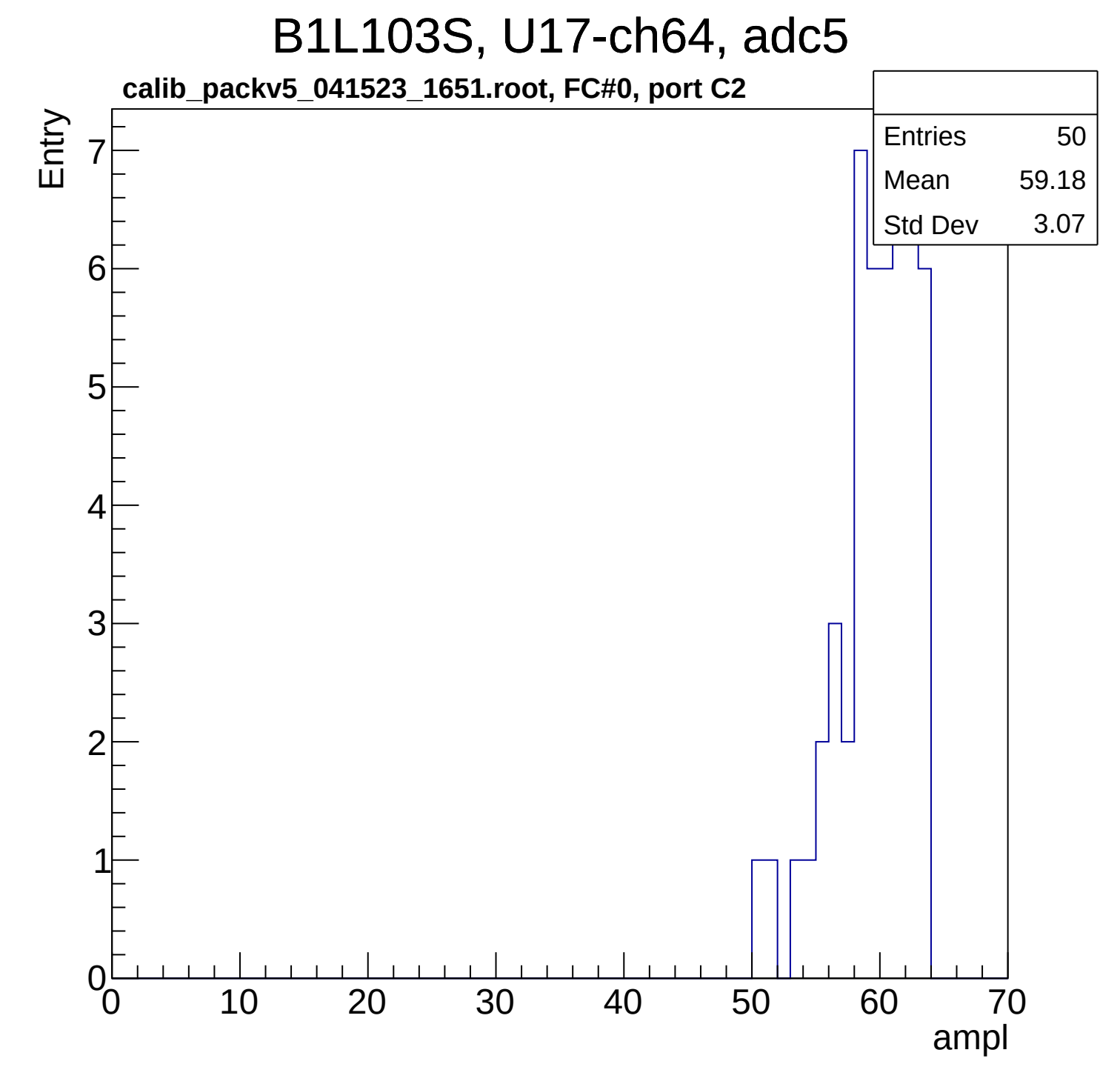

B1L103S, U17-ch64, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 20.19
Std Dev 13.31
Gaus mean : 28.8081
Gaus Width: 4.3670
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70

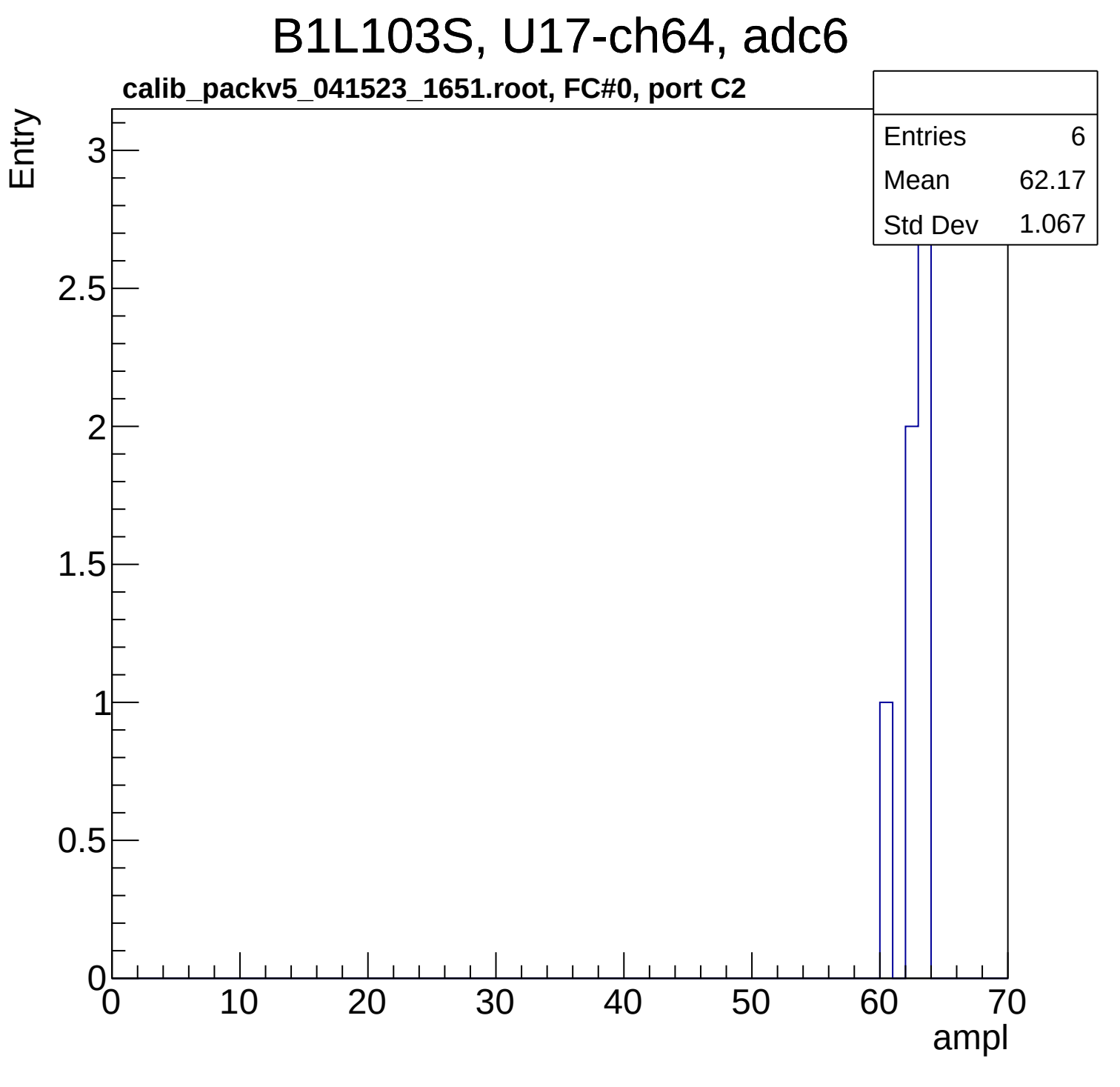

B1L103S, U17-ch64, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 31.53
Std Dev 12.35
Gaus mean : 36.0936
Gaus Width: 3.8348
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

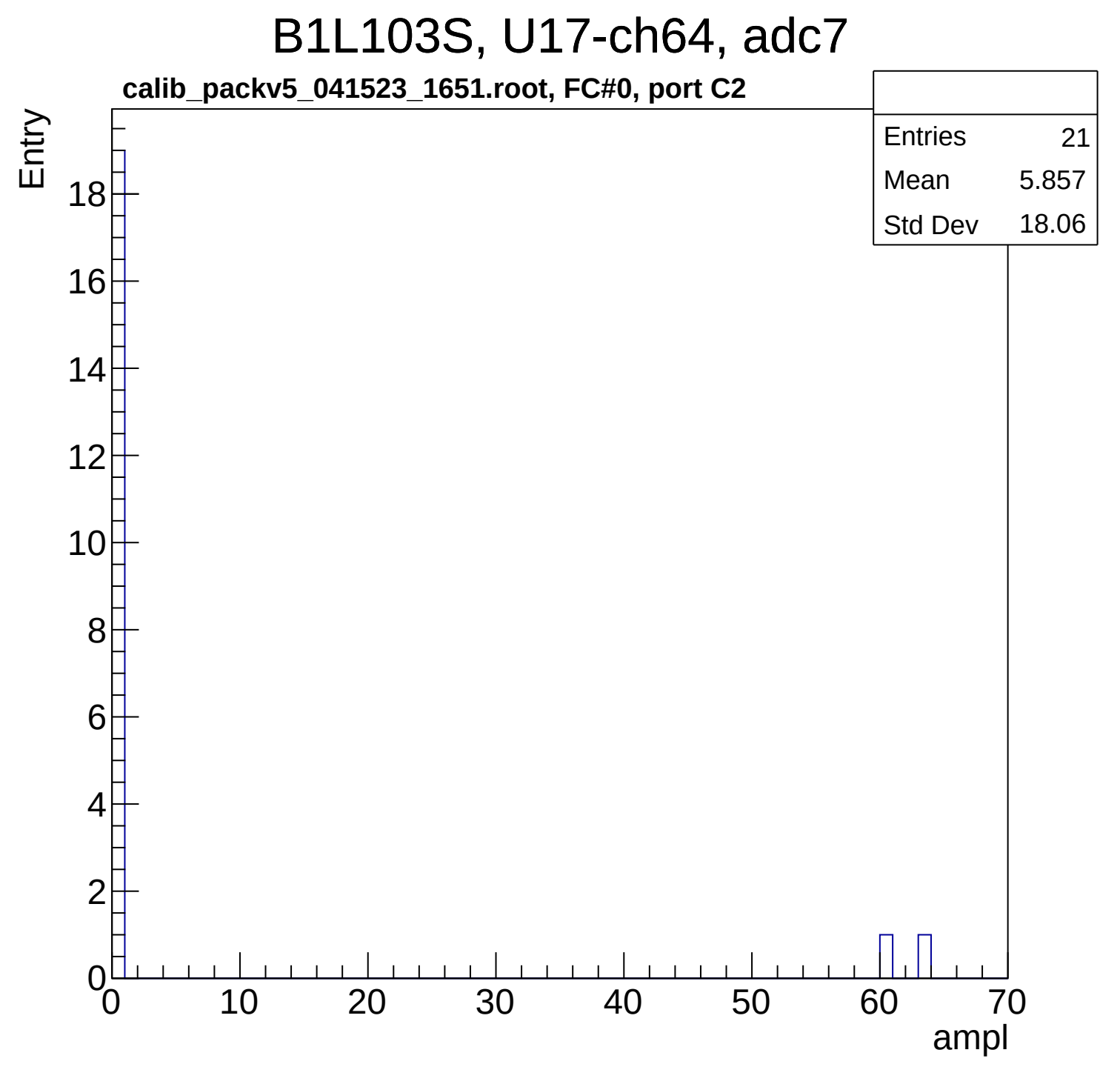

B1L103S, U17-ch64, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 40.12
Std Dev 9.979
Gaus mean : 43.4502
Gaus Width: 2.4253
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

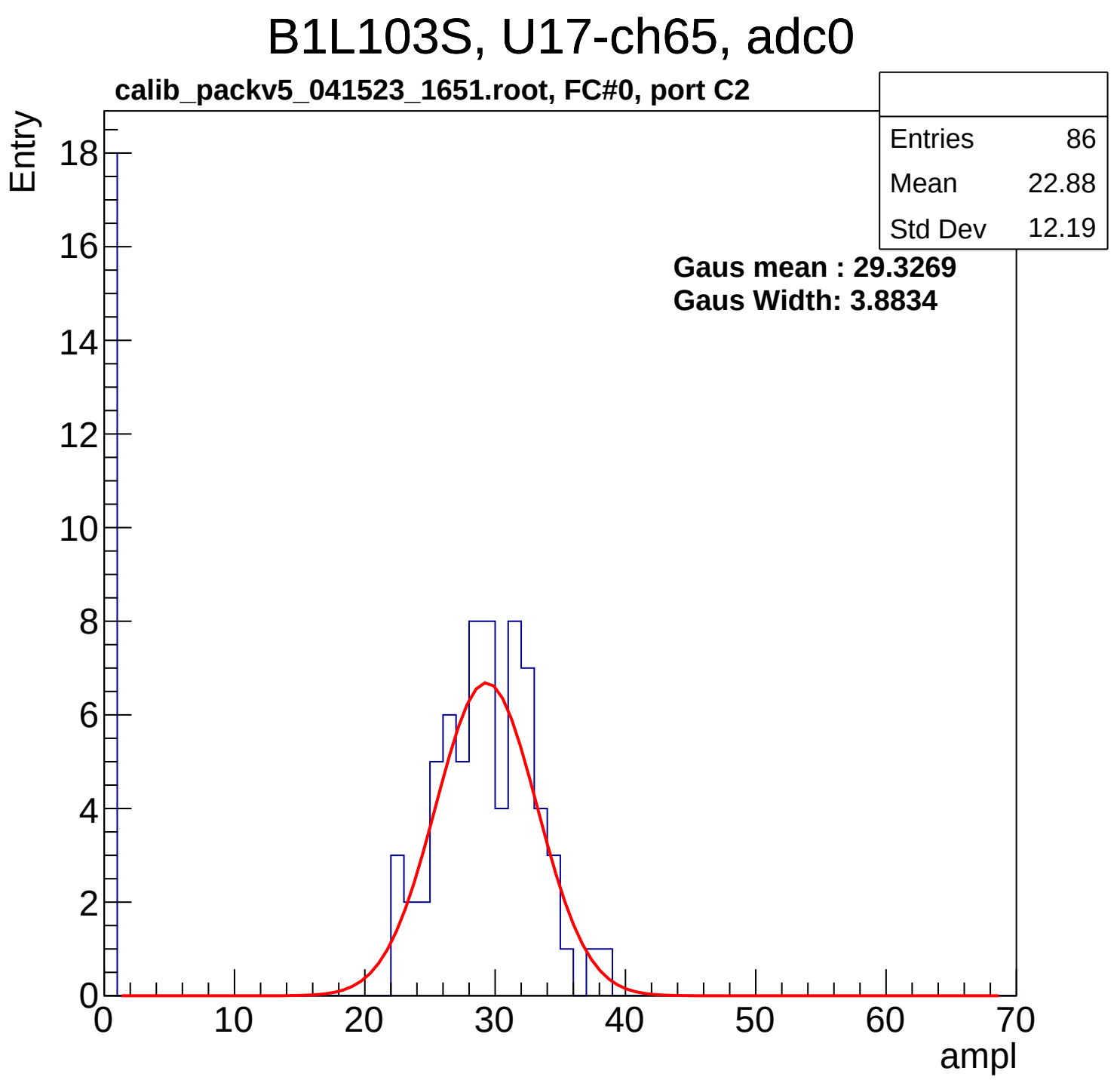

B1L103S, U17-ch64, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 49.09
Std Dev 4.337
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

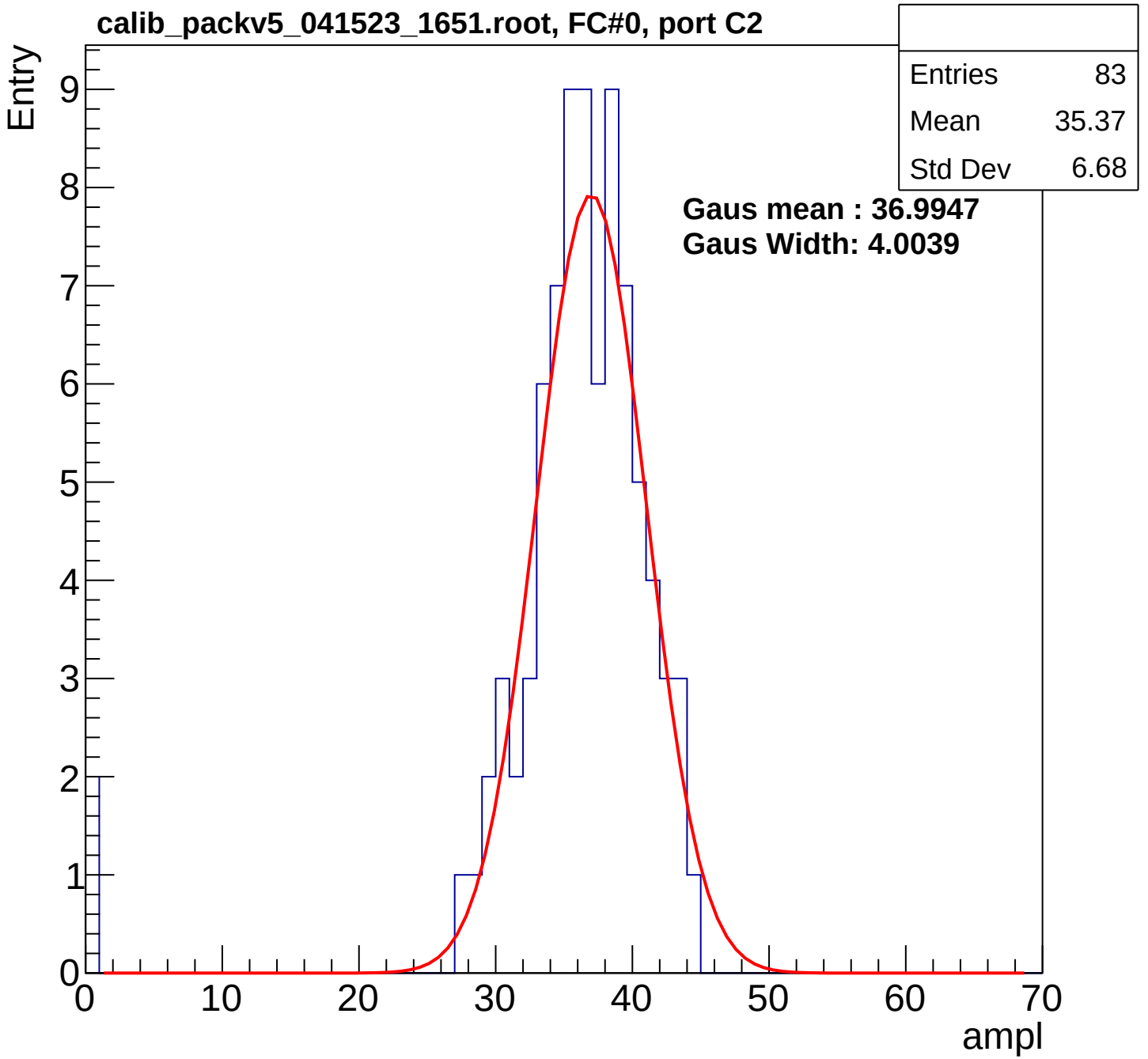

B1L103S, U17-ch64, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 53.45
Std Dev 7.849
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

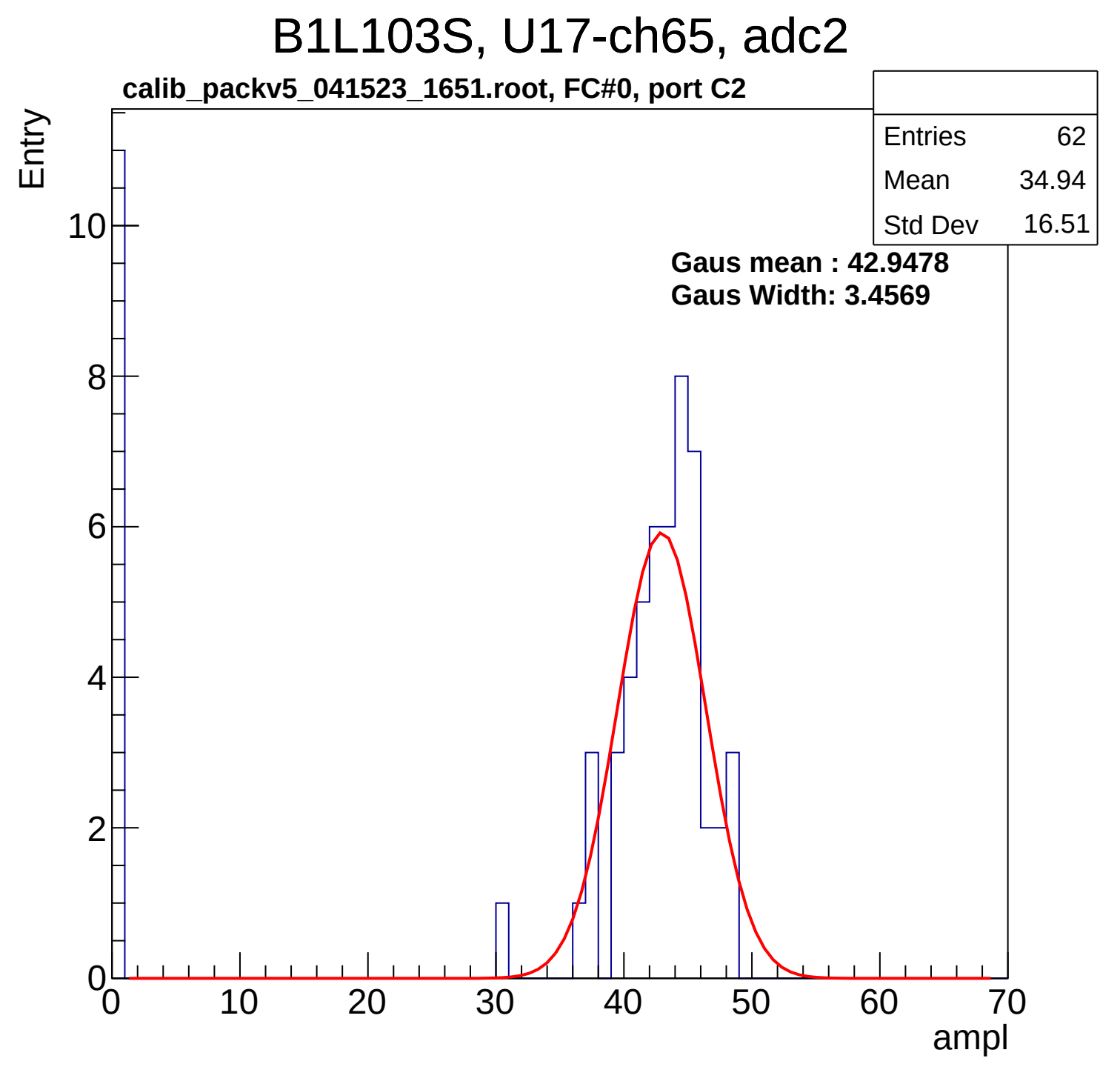

B1L103S, U17-ch64, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 59.18
Std Dev 3.07
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

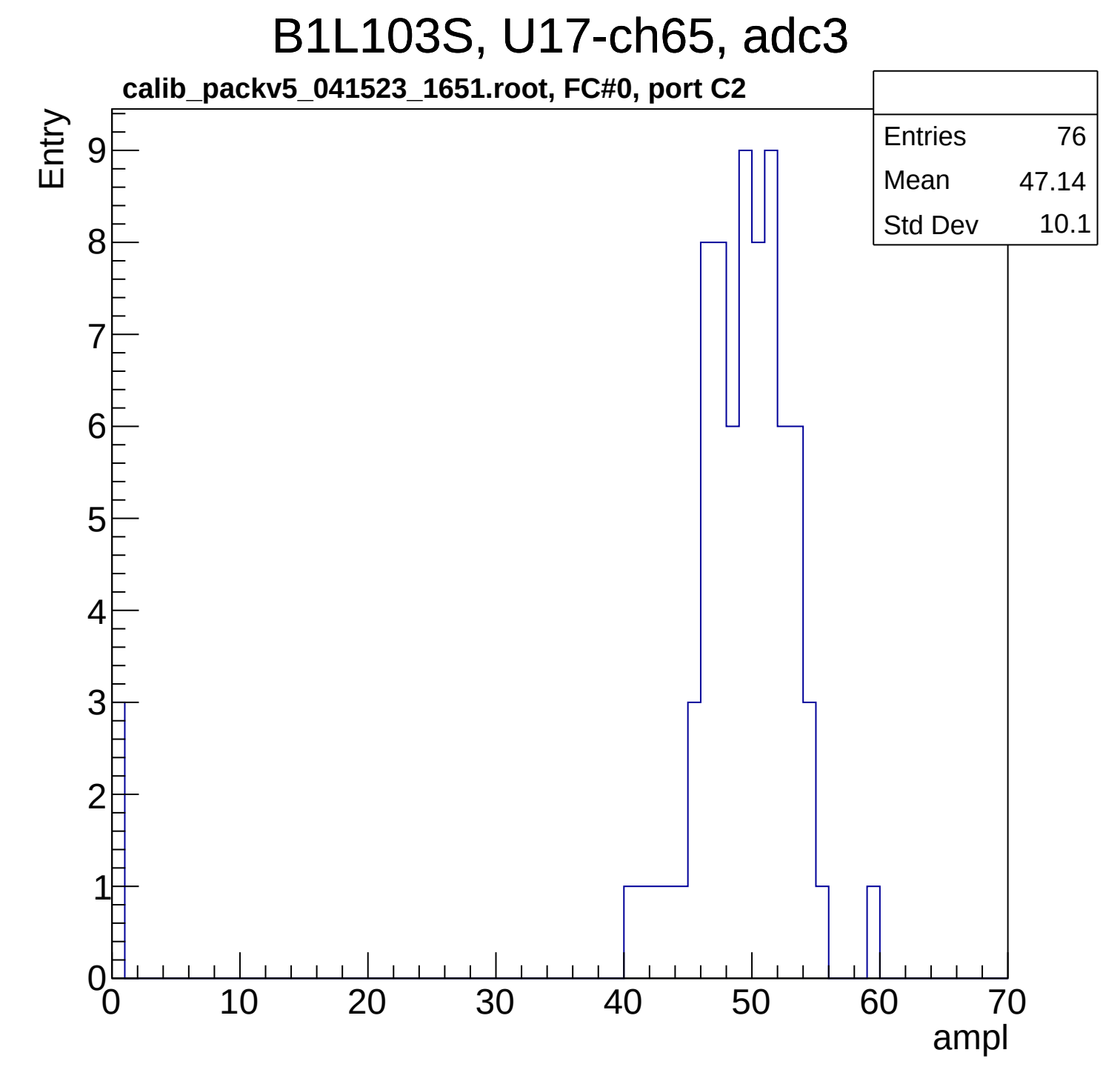

B1L103S, U17-ch64, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.17
Std Dev 1.067
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

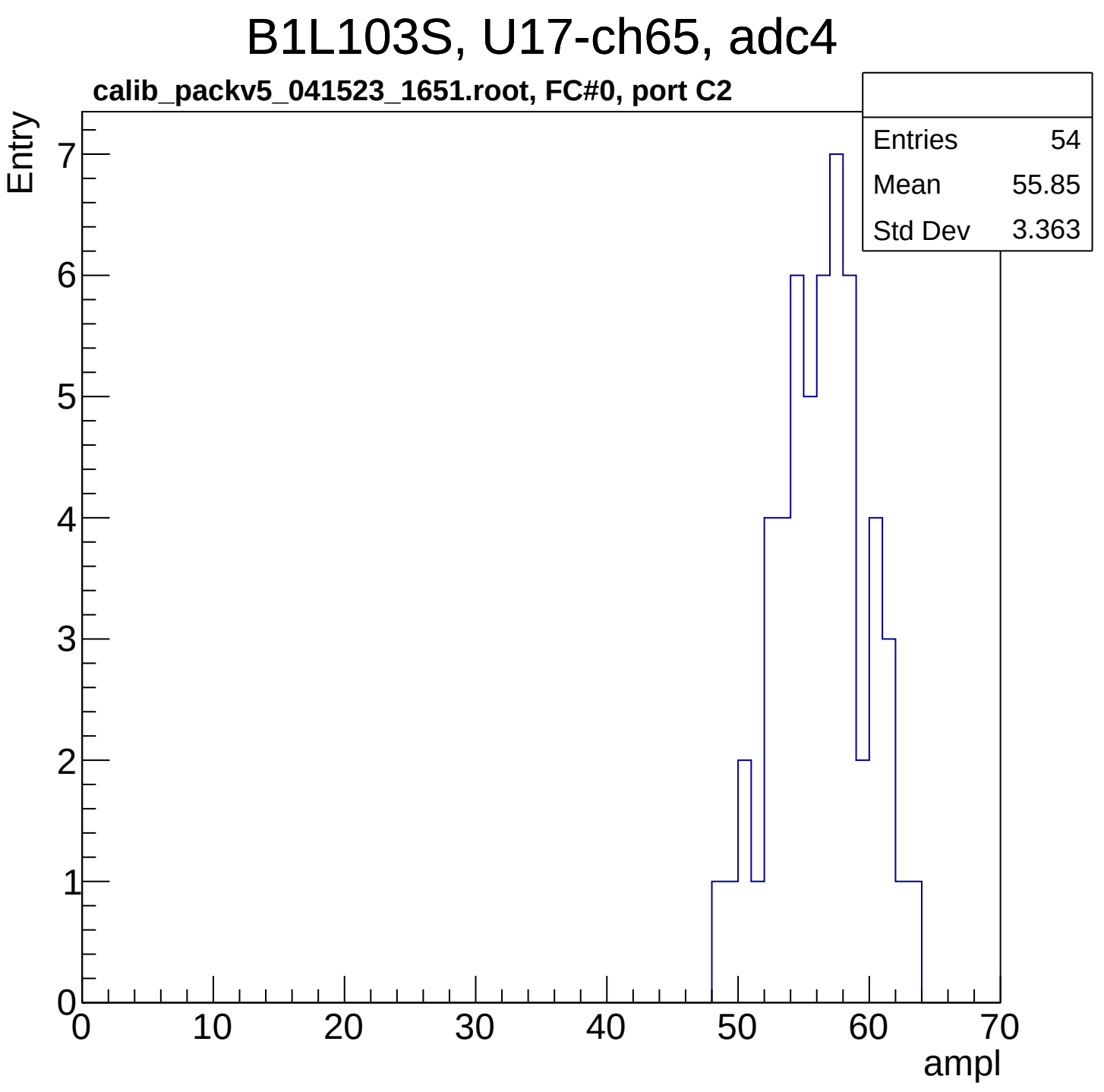

B1L103S, U17-ch64, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.857
Std Dev 18.06
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

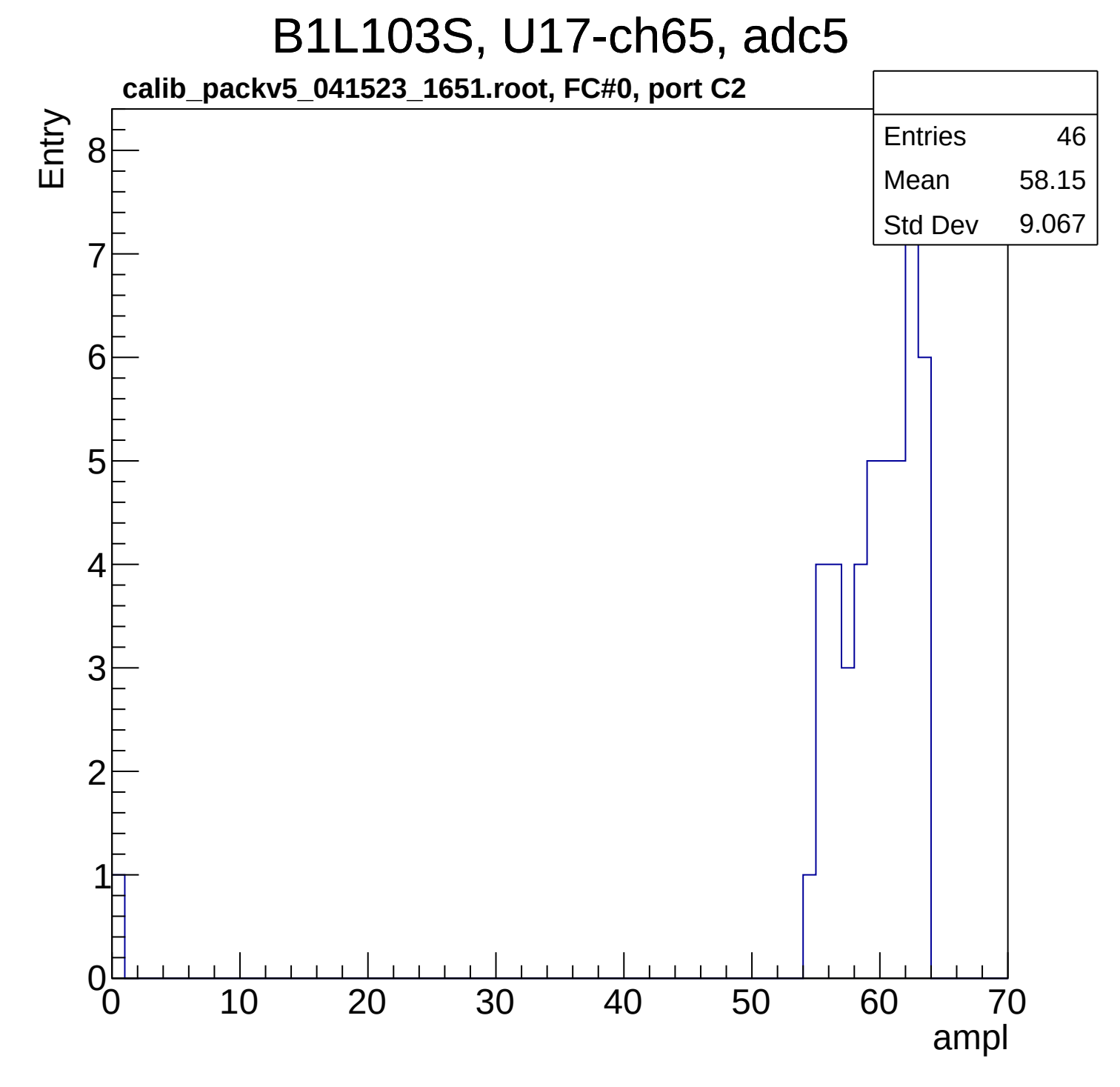

B1L103S, U17-ch65, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 22.88
Std Dev 12.19
Gaus mean : 29.3269
Gaus Width: 3.8834
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

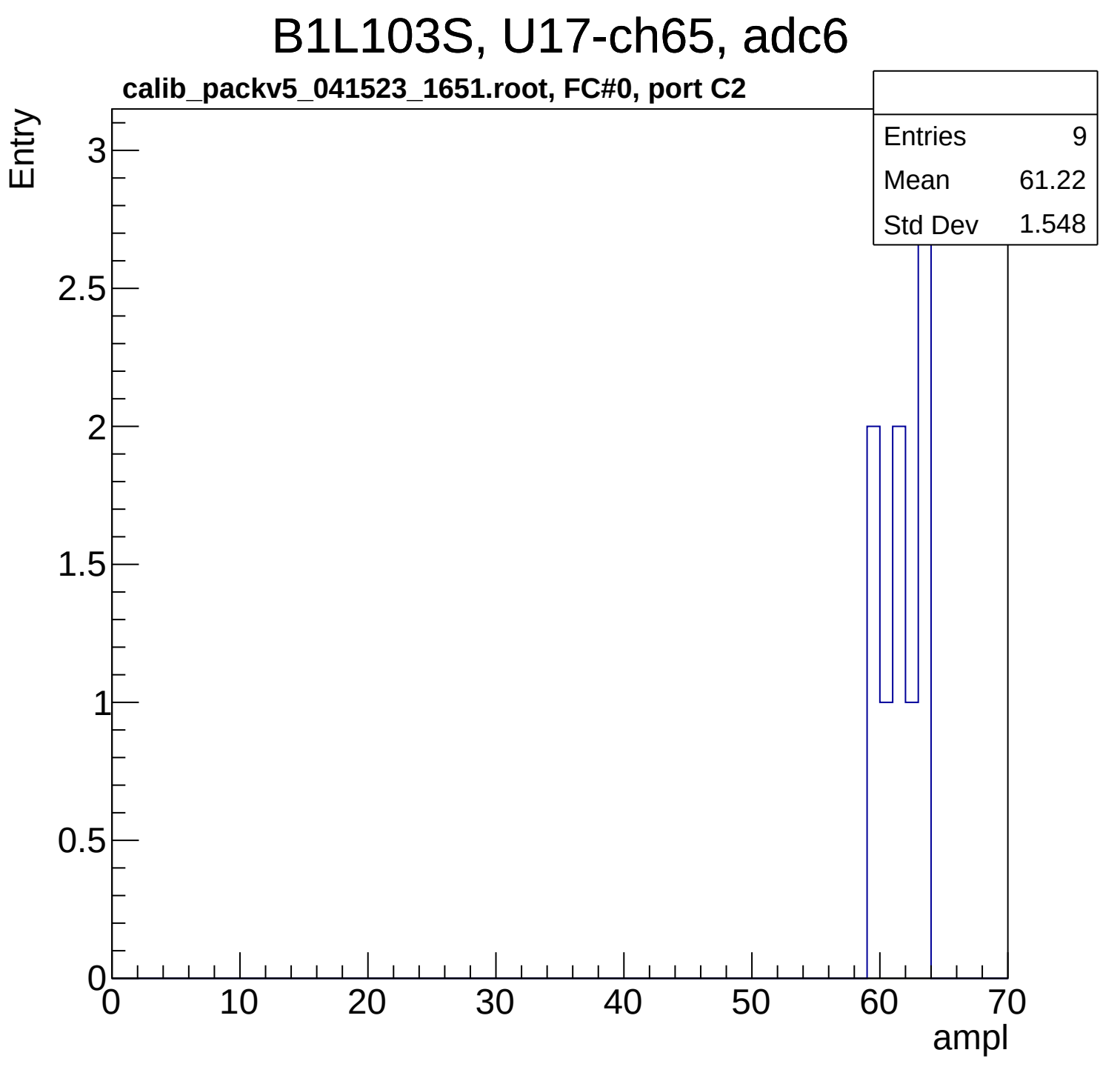

B1L103S, U17-ch65, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 35.37
Std Dev 6.68
Gaus mean : 36.9947
Gaus Width: 4.0039
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

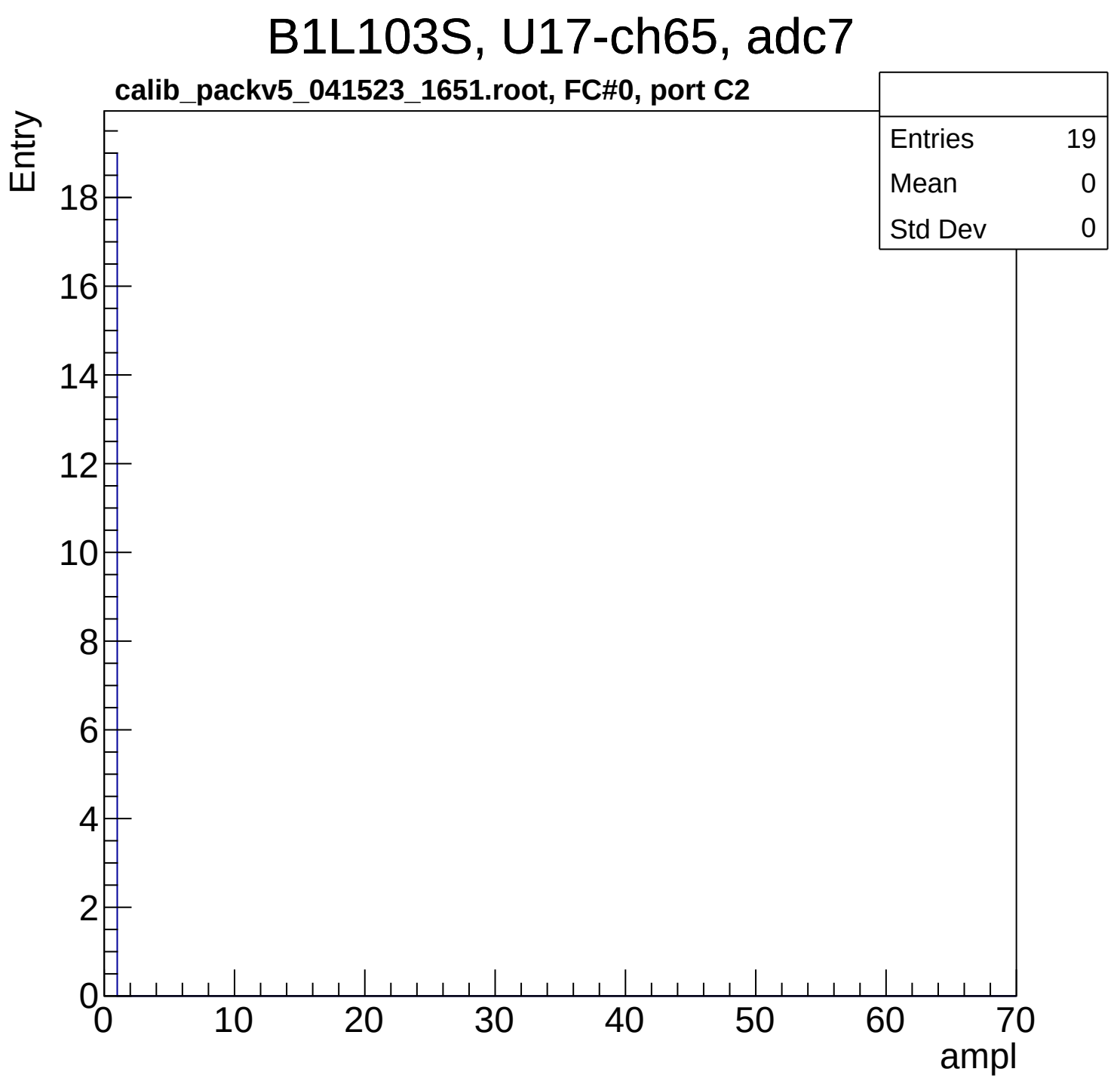

B1L103S, U17-ch65, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 34.94
Std Dev 16.51
Gaus mean : 42.9478
Gaus Width: 3.4569
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

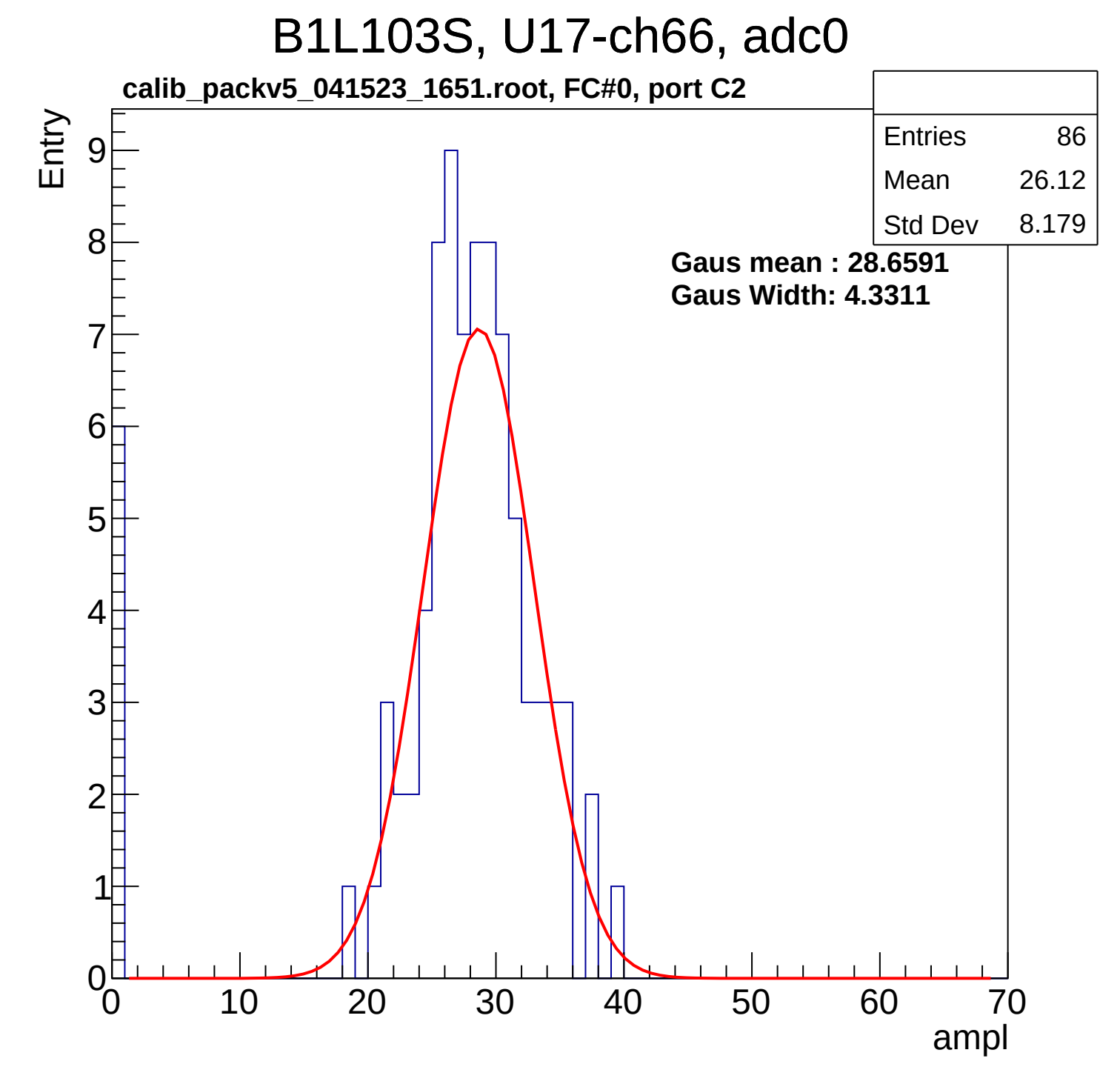

B1L103S, U17-ch65, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 47.14
Std Dev 10.1
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

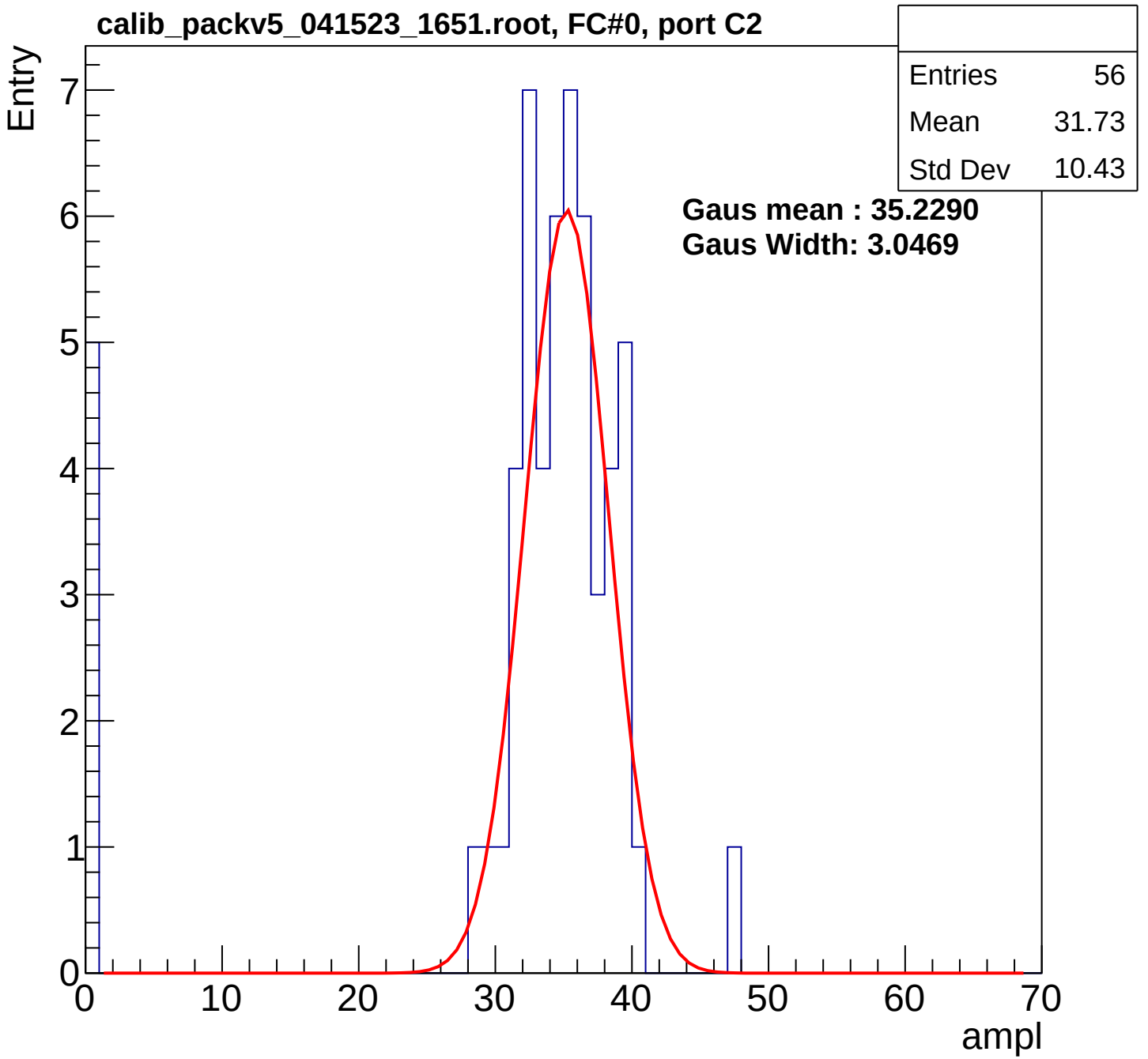

B1L103S, U17-ch65, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 55.85
Std Dev 3.363
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

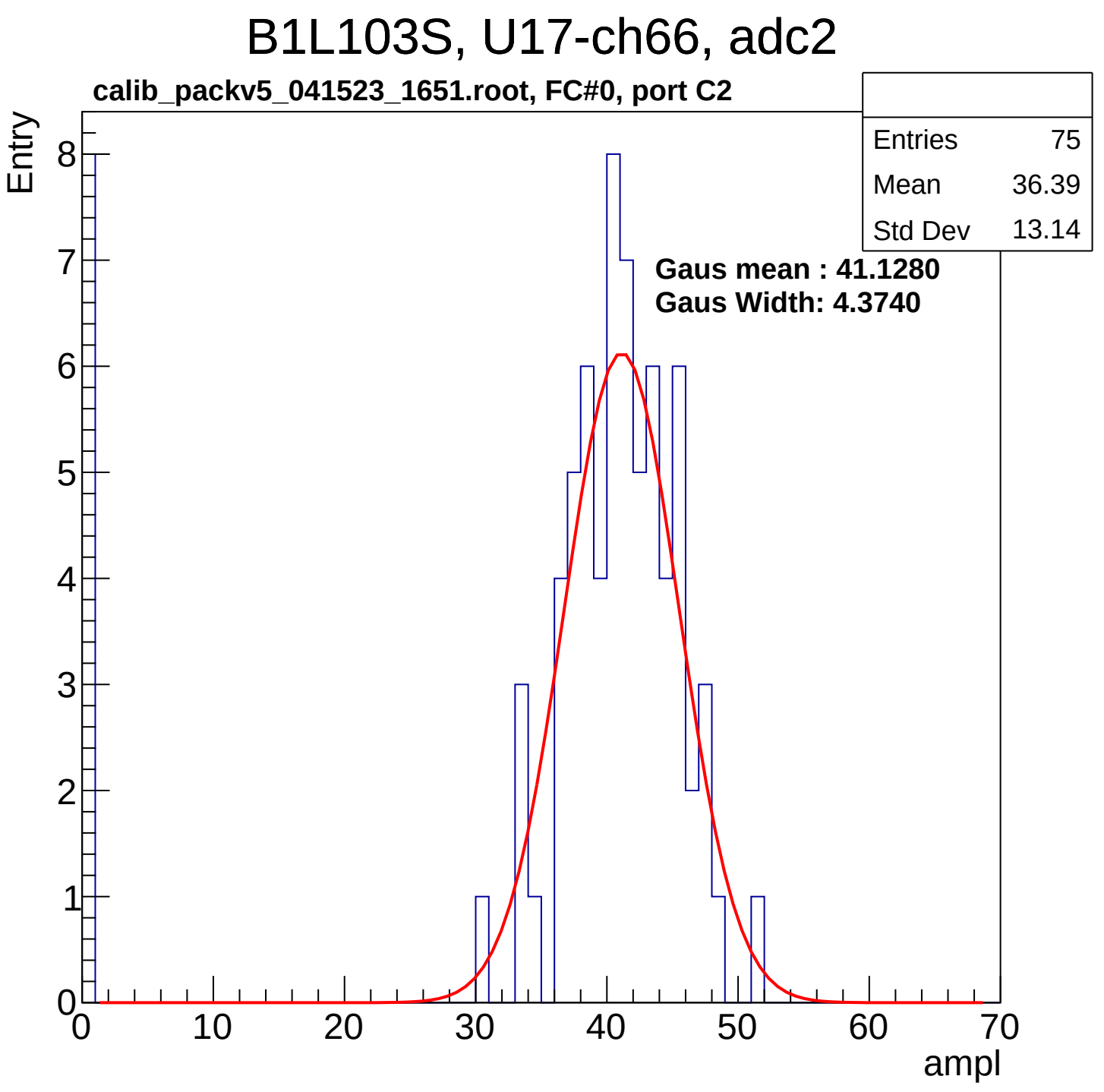

B1L103S, U17-ch65, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.15
Std Dev 9.067
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

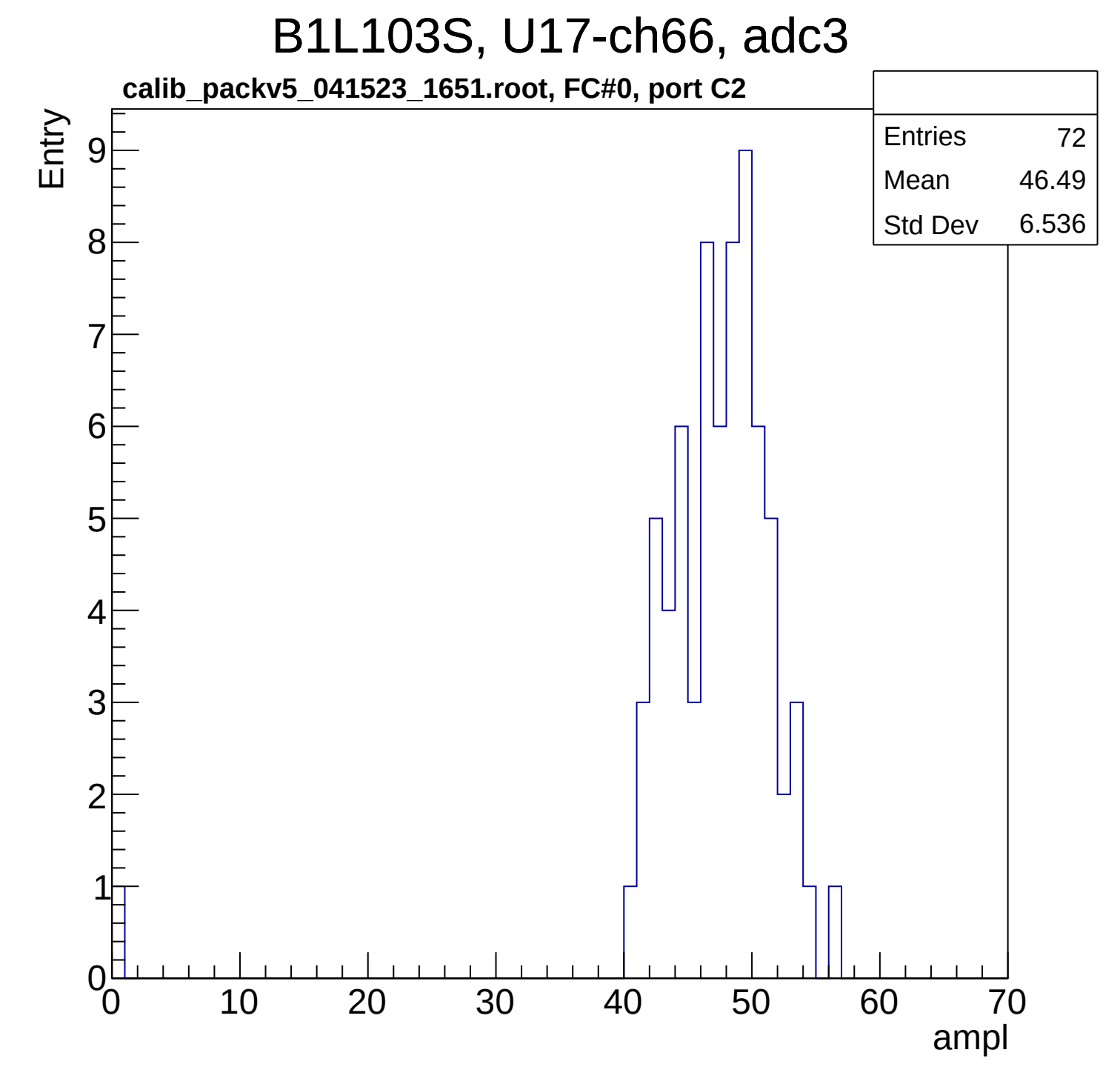

B1L103S, U17-ch65, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.22
Std Dev 1.548
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

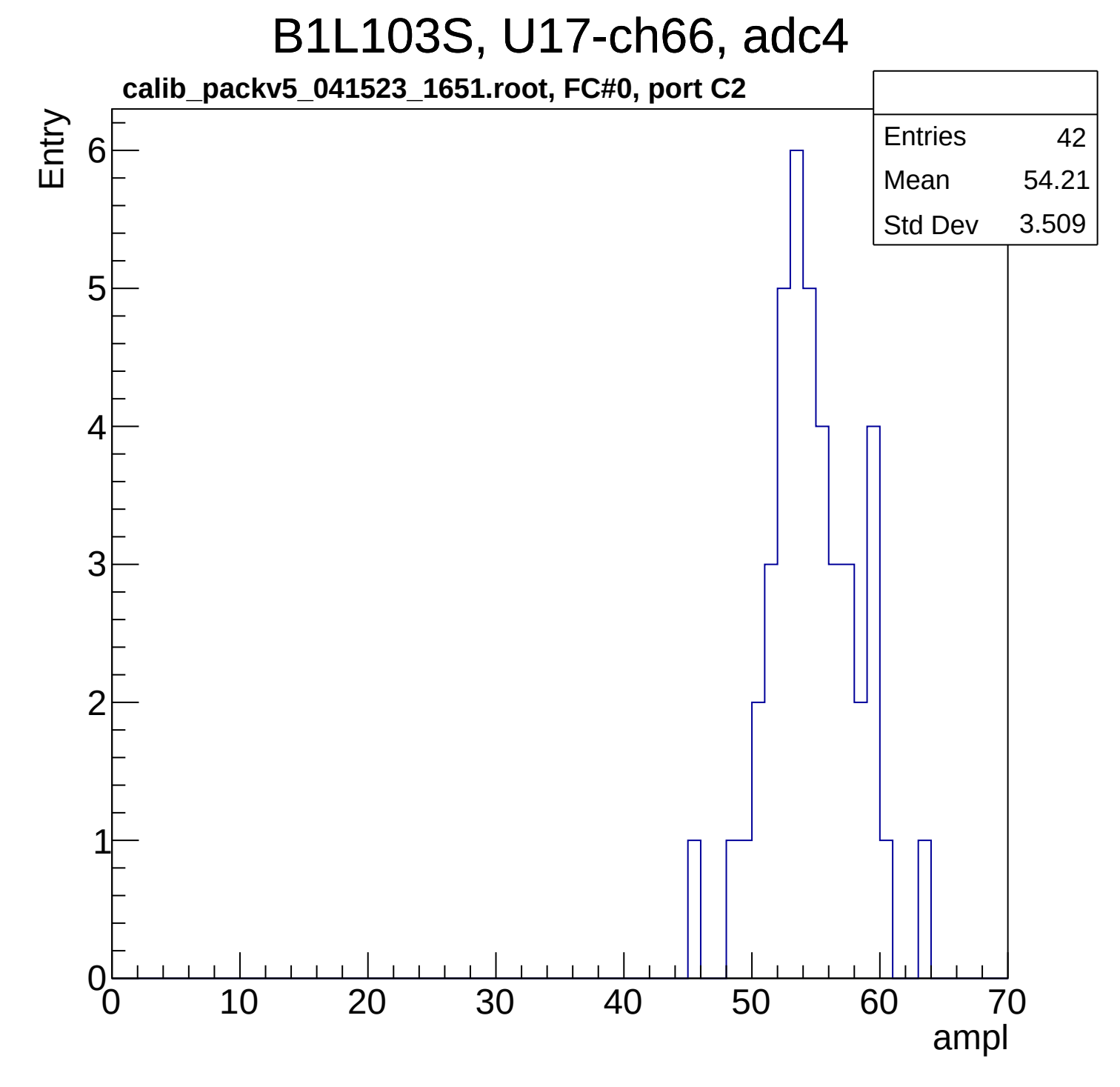

B1L103S, U17-ch65, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

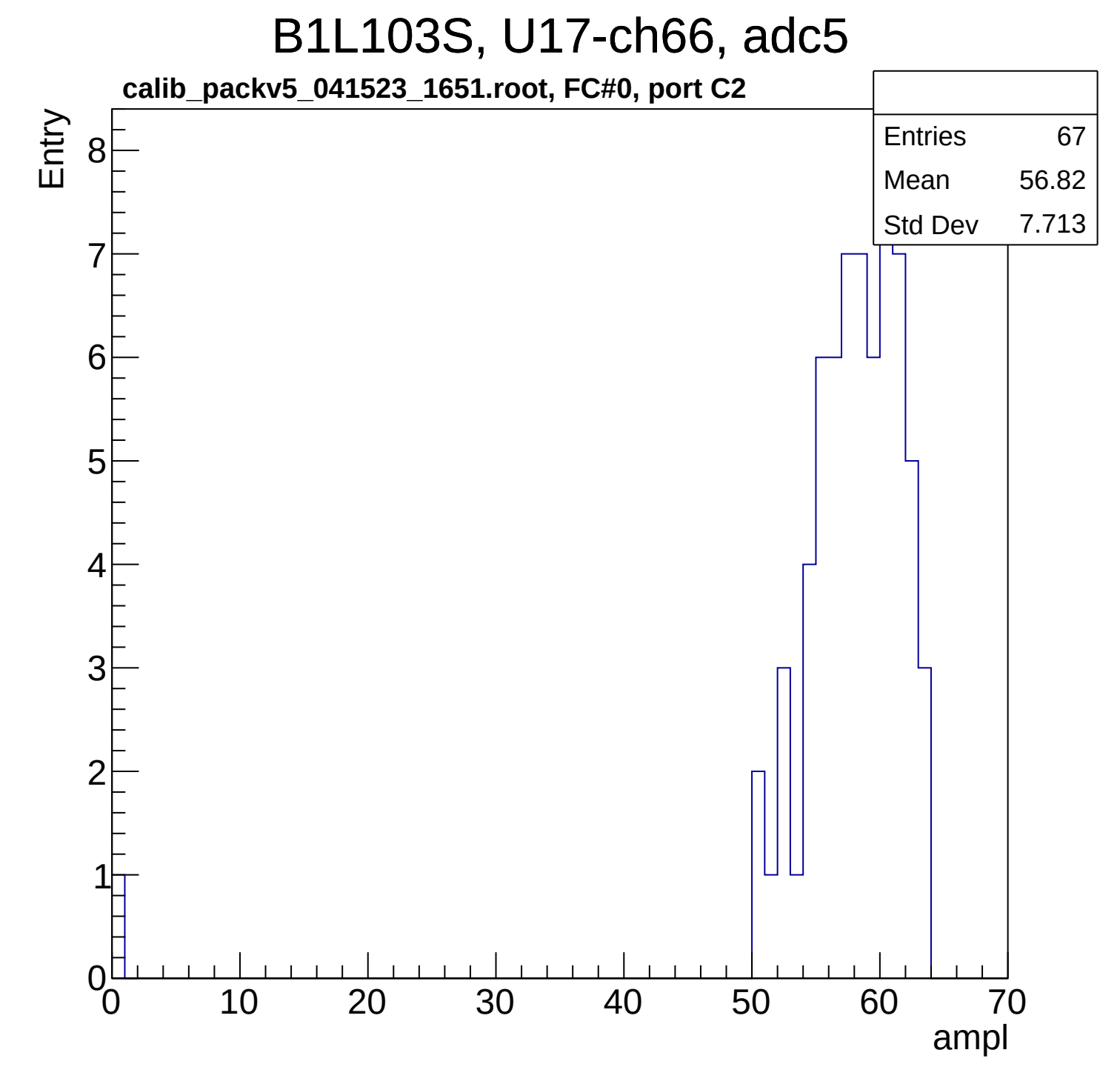

B1L103S, U17-ch66, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 26.12
Std Dev 8.179
Gaus mean : 28.6591
Gaus Width: 4.3311
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

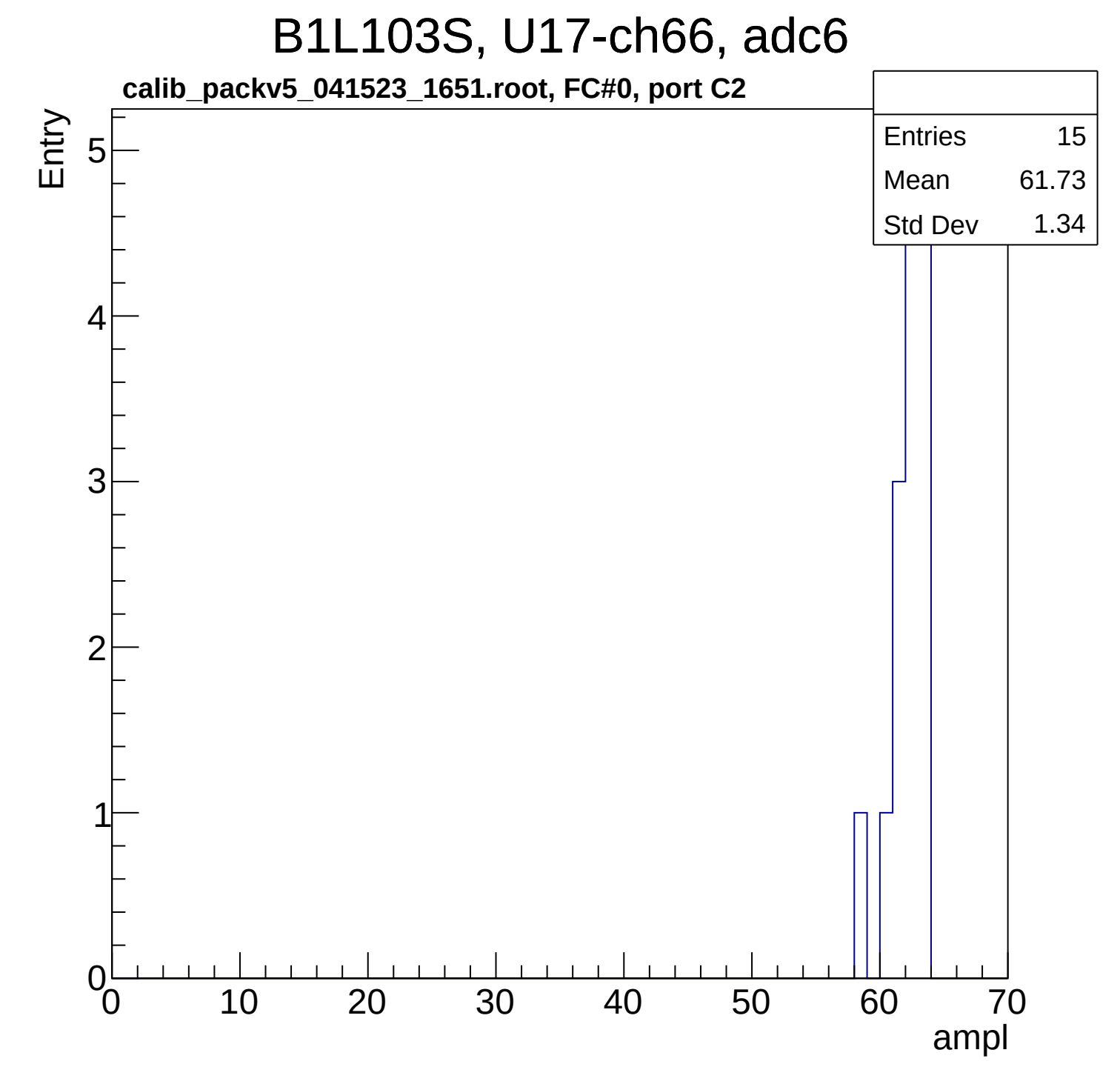

B1L103S, U17-ch66, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 31.73
Std Dev 10.43
Gaus mean : 35.2290
Gaus Width: 3.0469
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

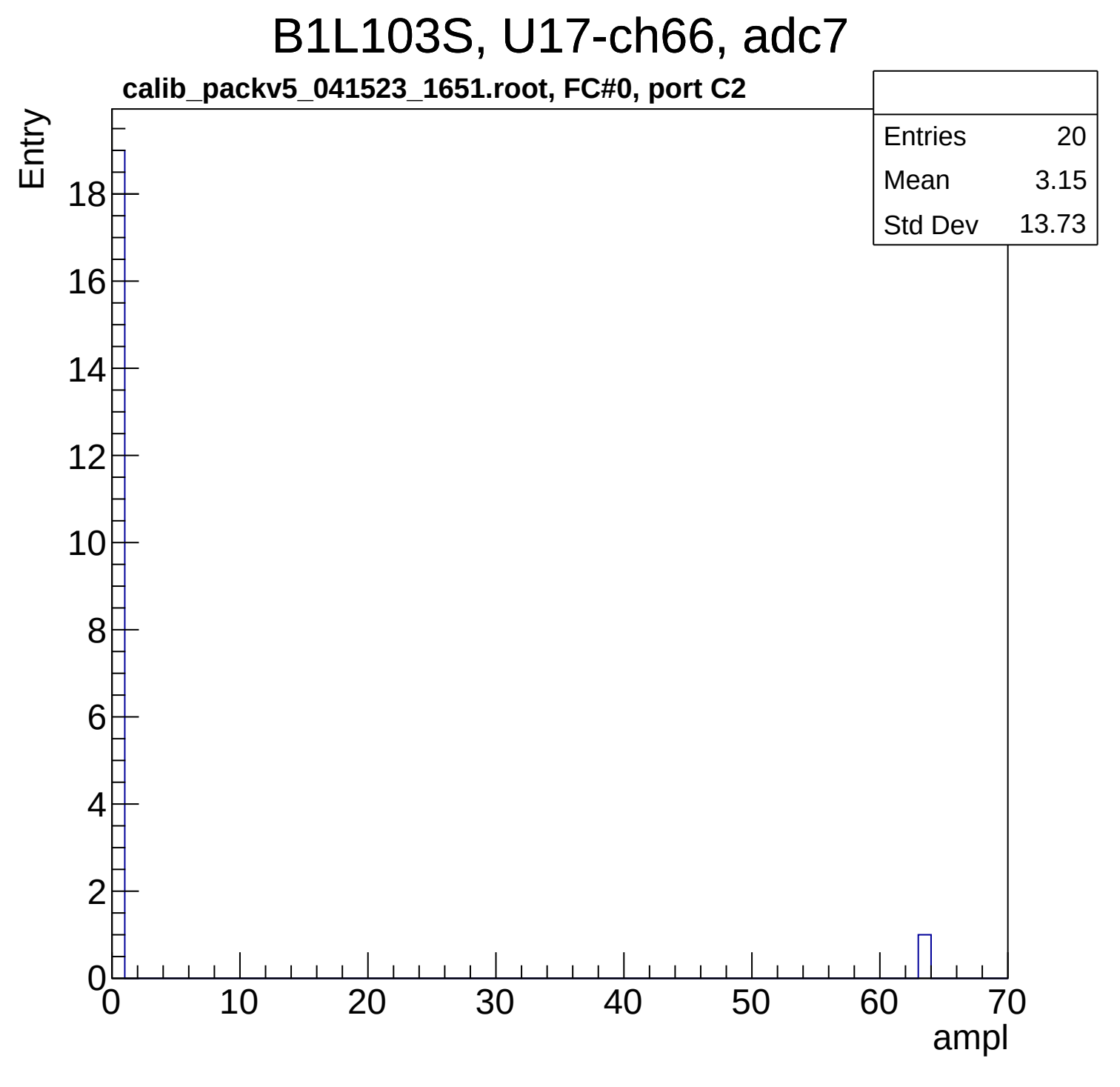

B1L103S, U17-ch66, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 36.39
Std Dev 13.14
Gaus mean : 41.1280
Gaus Width: 4.3740
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

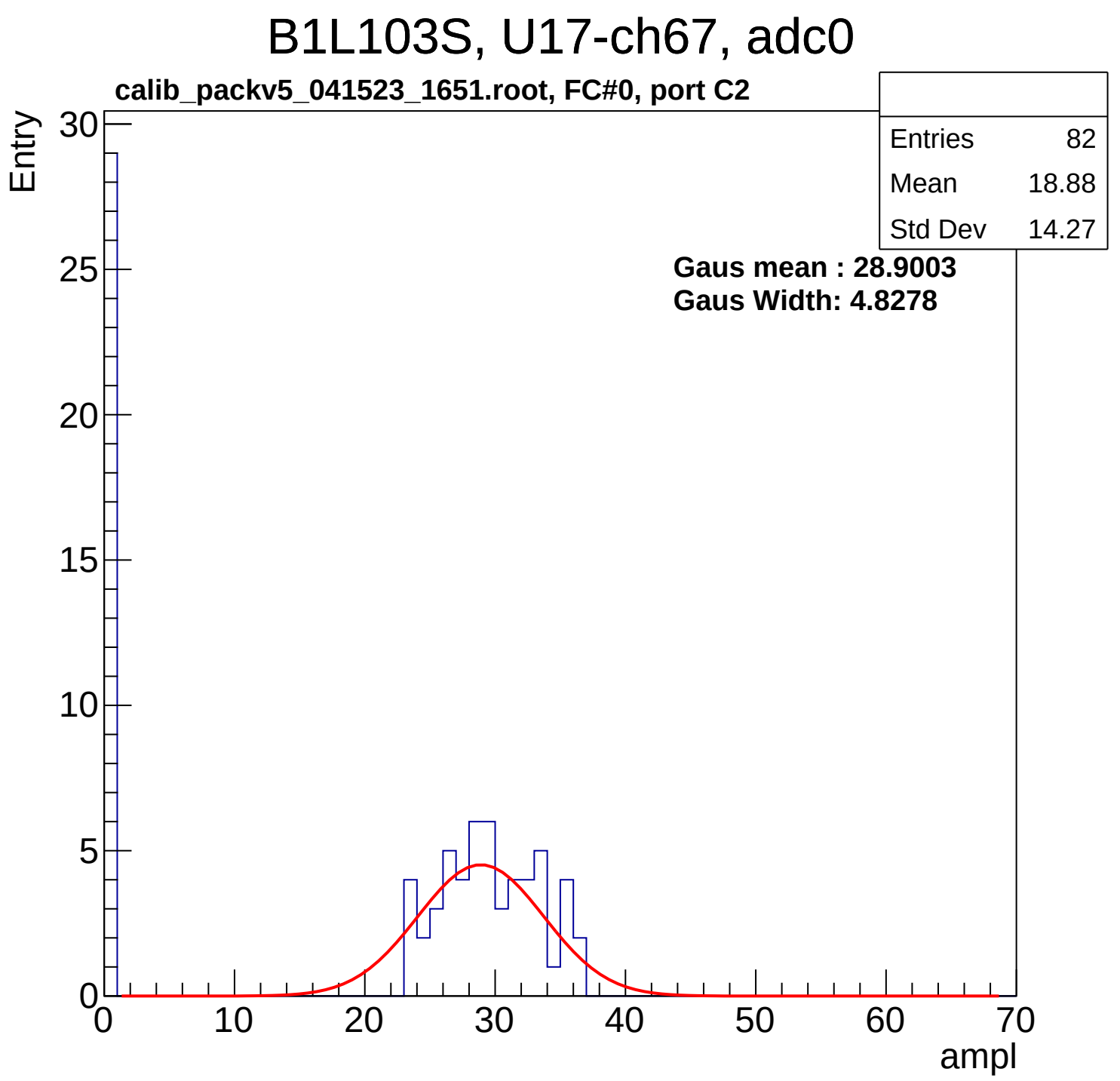

B1L103S, U17-ch66, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 46.49
Std Dev 6.536
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

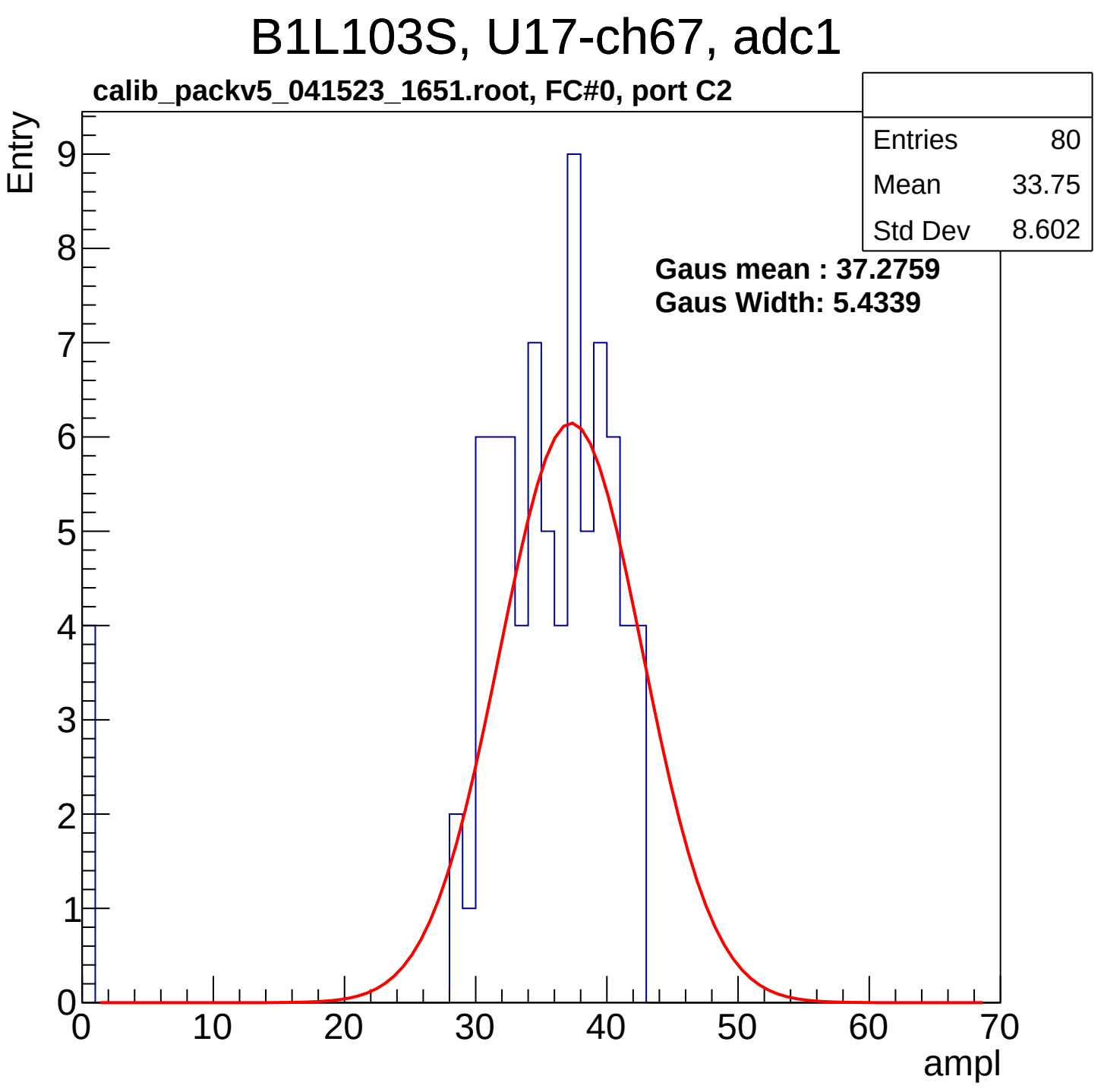

B1L103S, U17-ch66, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 54.21
Std Dev 3.509
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

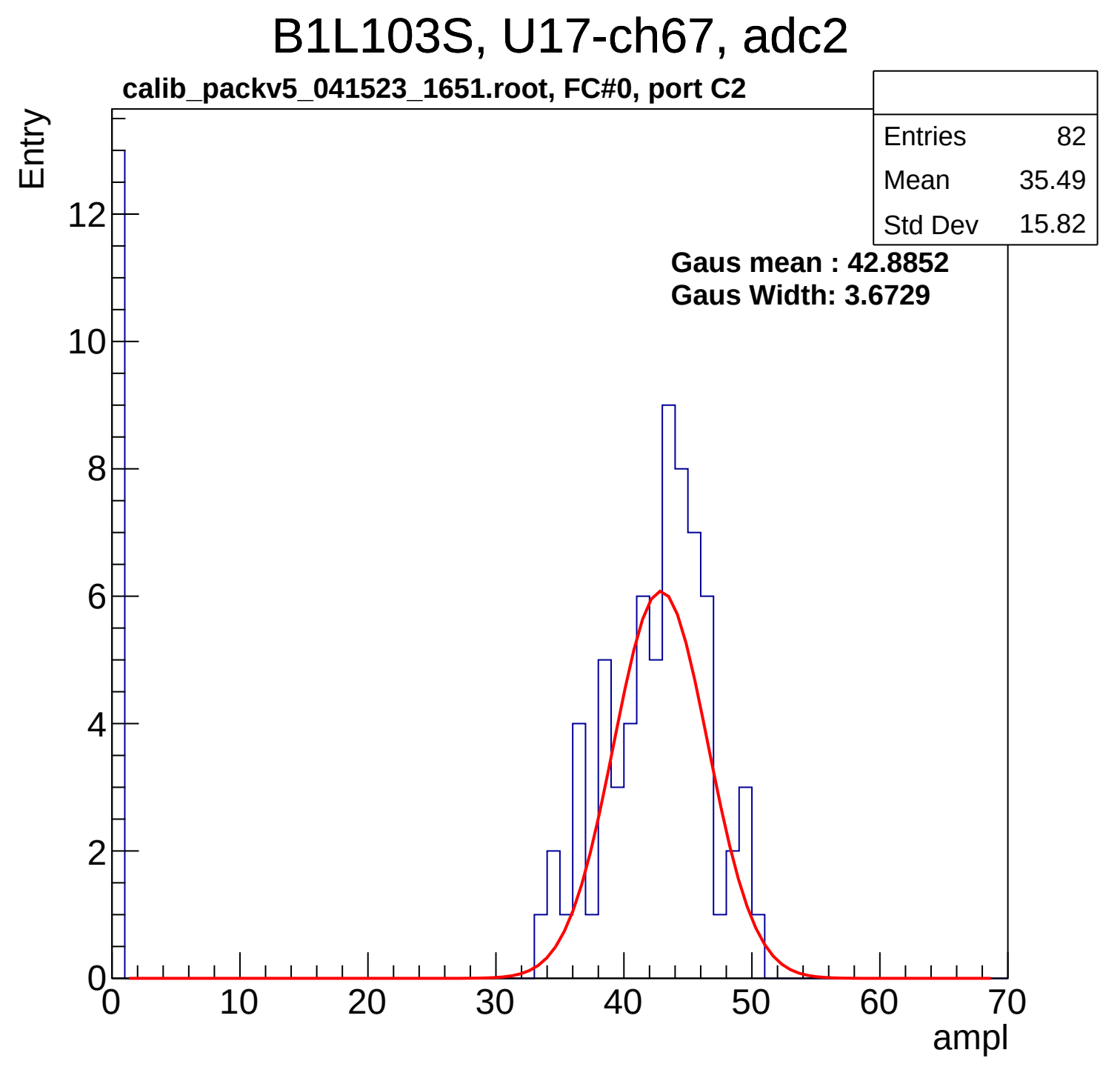

B1L103S, U17-ch66, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 56.82
Std Dev 7.713
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

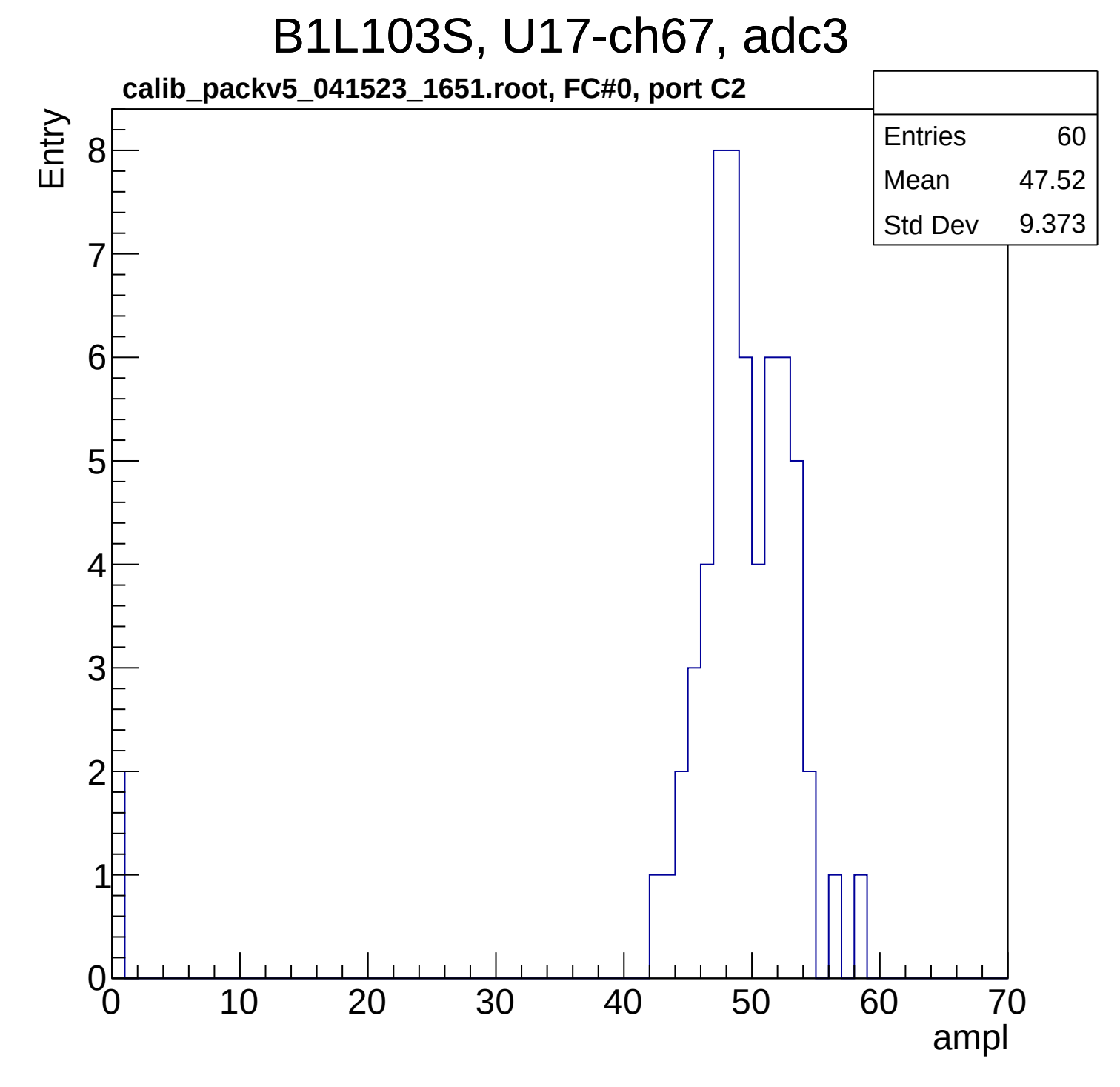

B1L103S, U17-ch66, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.73
Std Dev 1.34
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

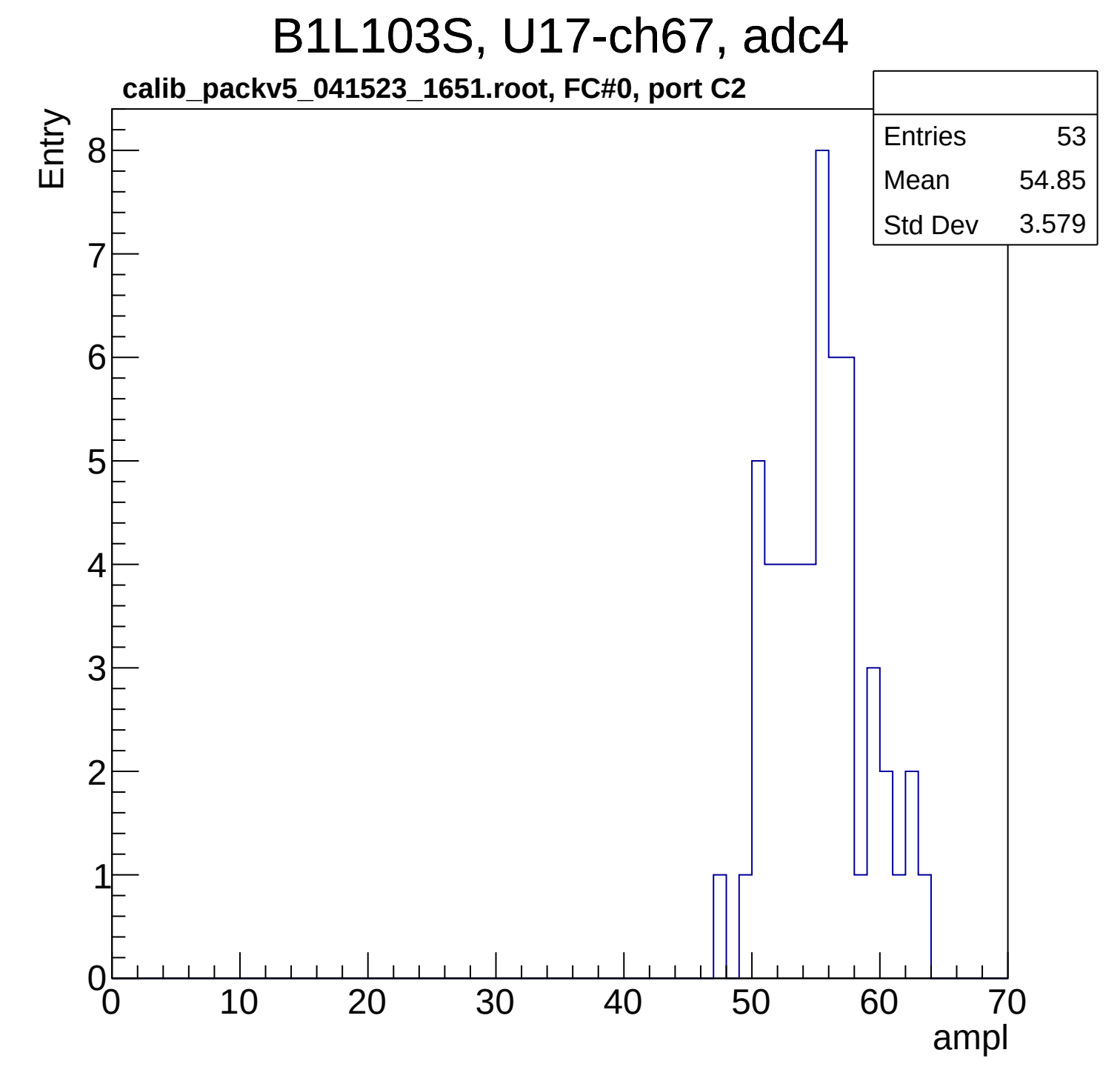

B1L103S, U17-ch66, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

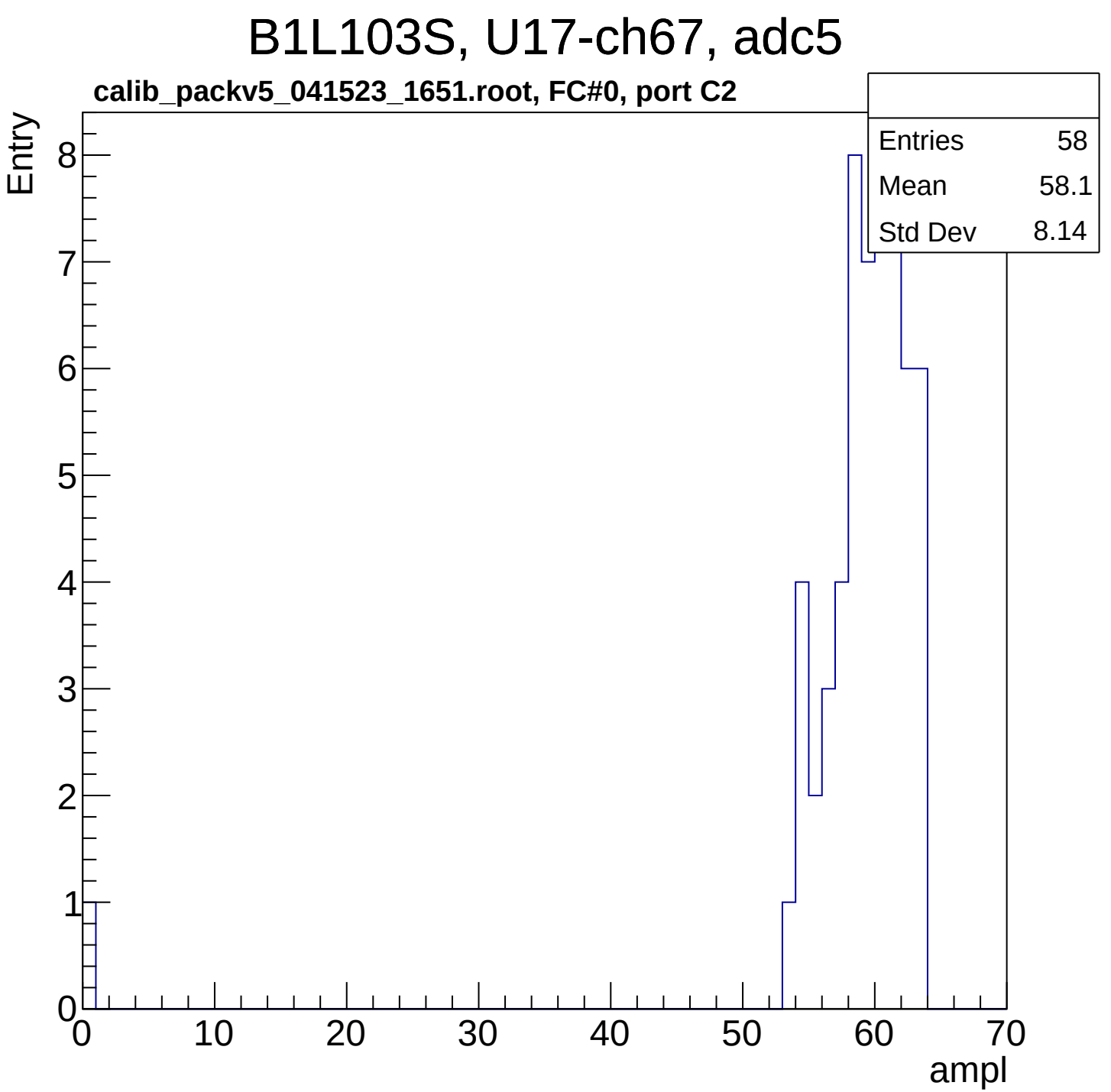

B1L103S, U17-ch67, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 18.88
Std Dev 14.27
Gaus mean : 28.9003
Gaus Width: 4.8278
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70

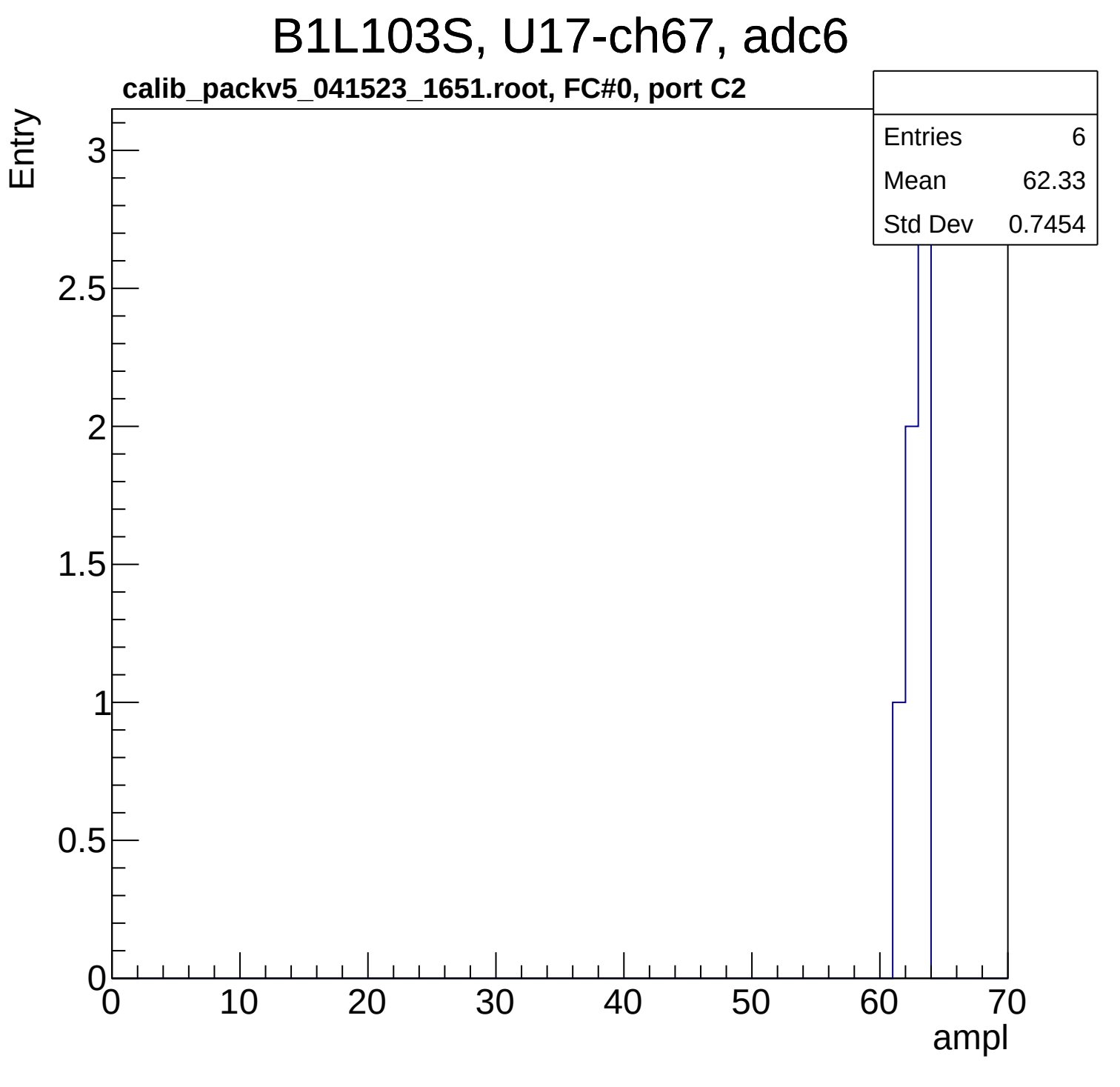

B1L103S, U17-ch67, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 33.75
Std Dev 8.602
Gaus mean : 37.2759
Gaus Width: 5.4339
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

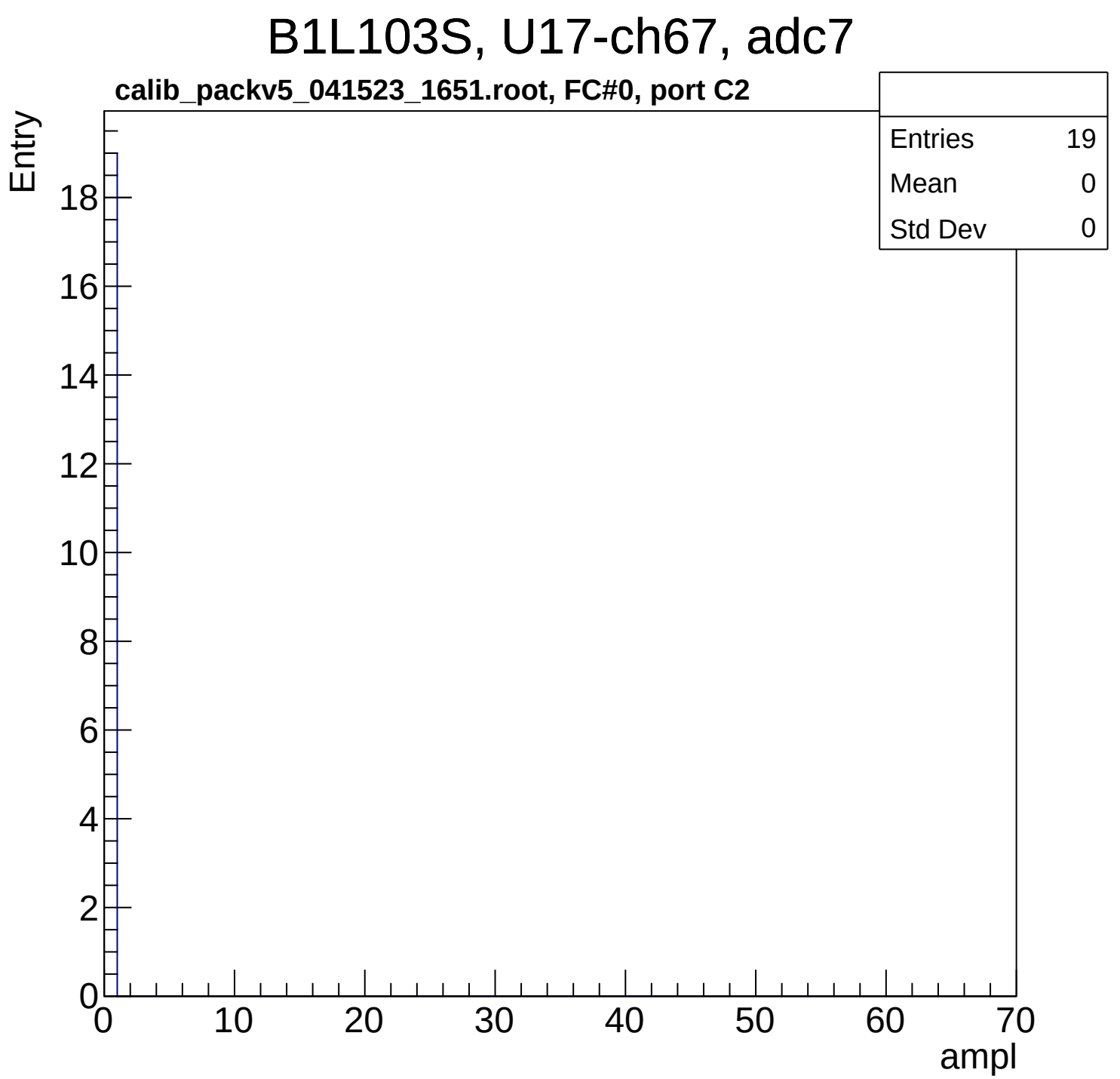

B1L103S, U17-ch67, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 35.49
Std Dev 15.82
Gaus mean : 42.8852
Gaus Width: 3.6729
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

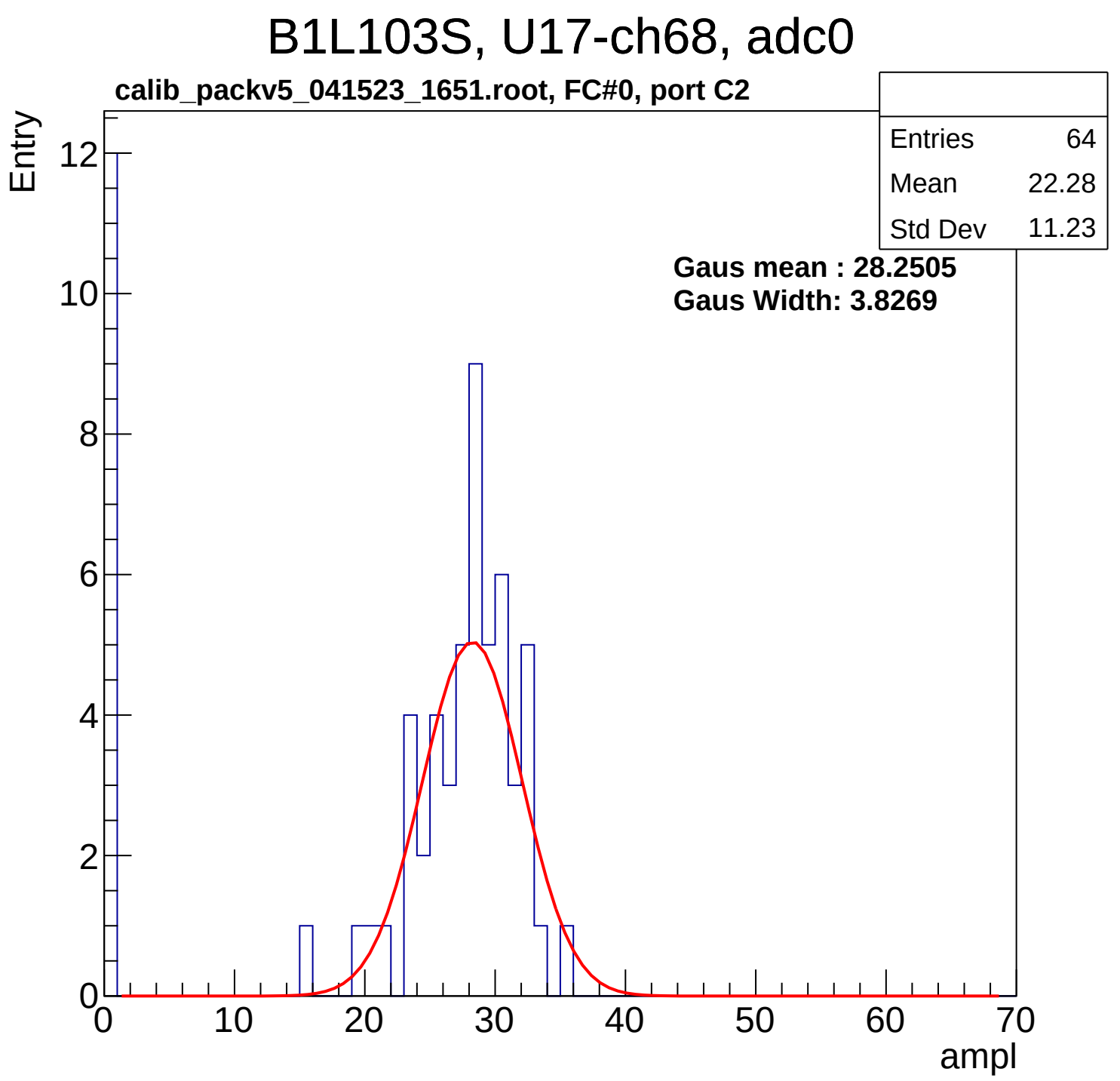

B1L103S, U17-ch67, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 47.52
Std Dev 9.373
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

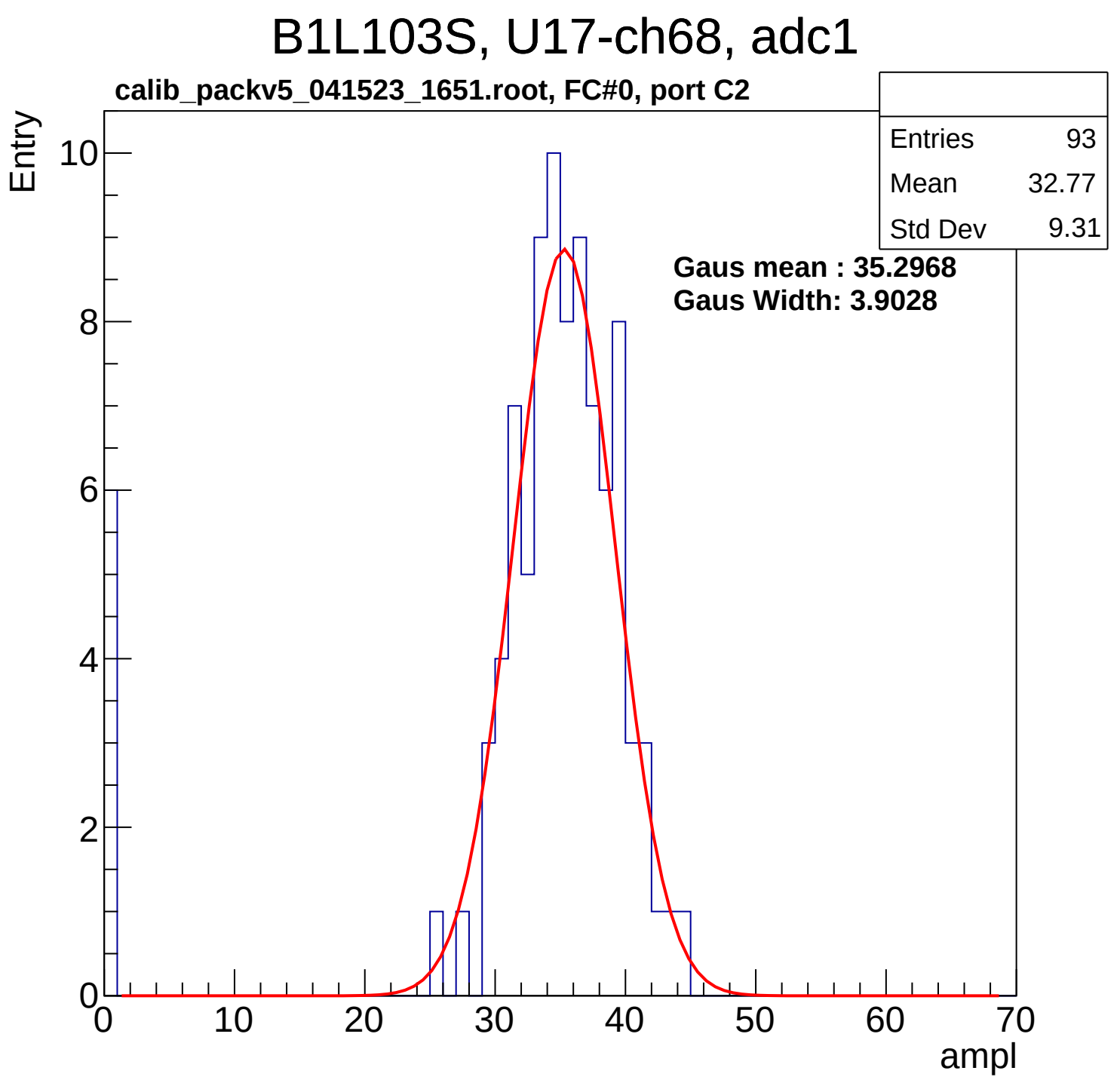

B1L103S, U17-ch67, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 54.85
Std Dev 3.579
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

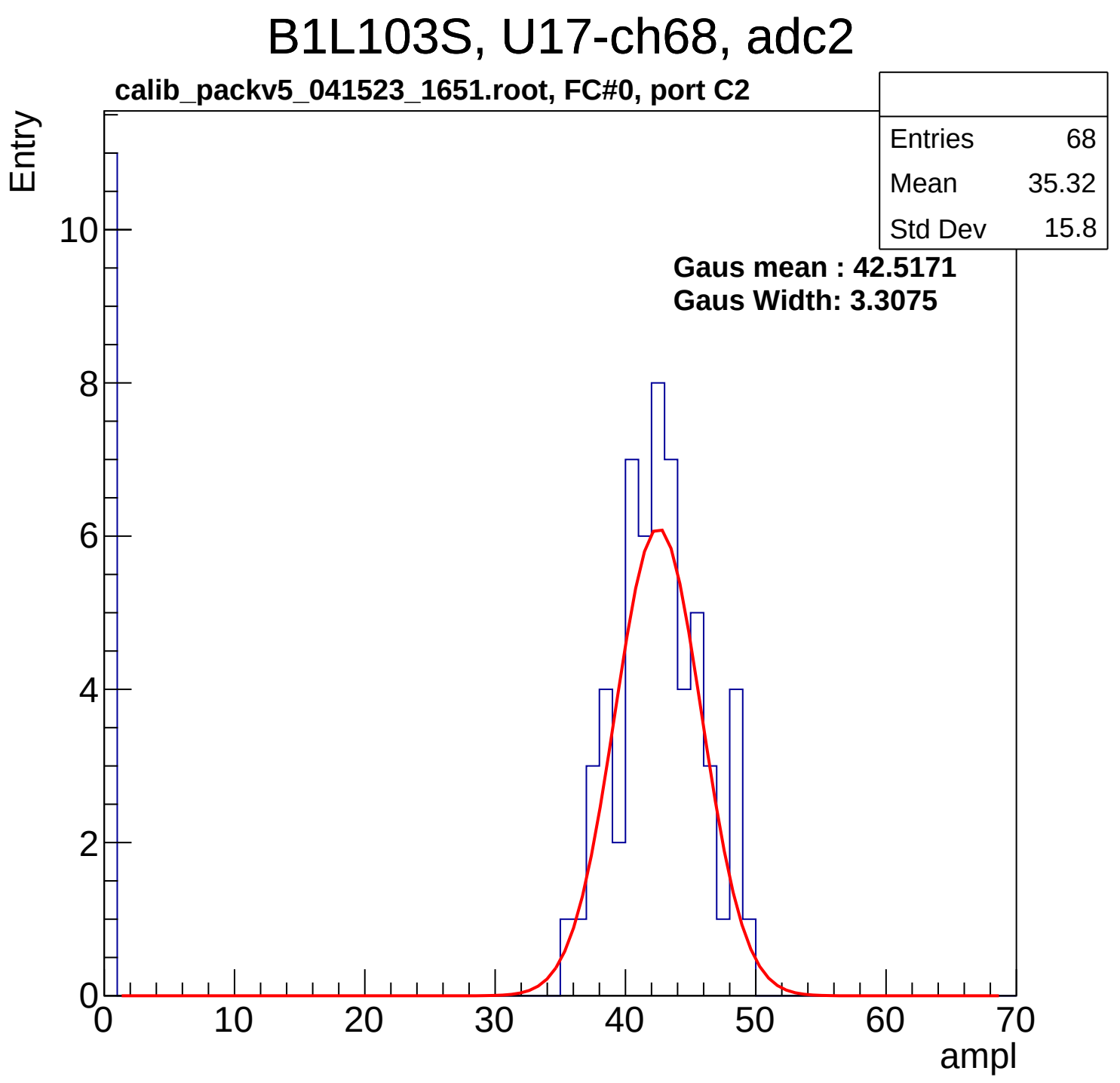

B1L103S, U17-ch67, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.1
Std Dev 8.14
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

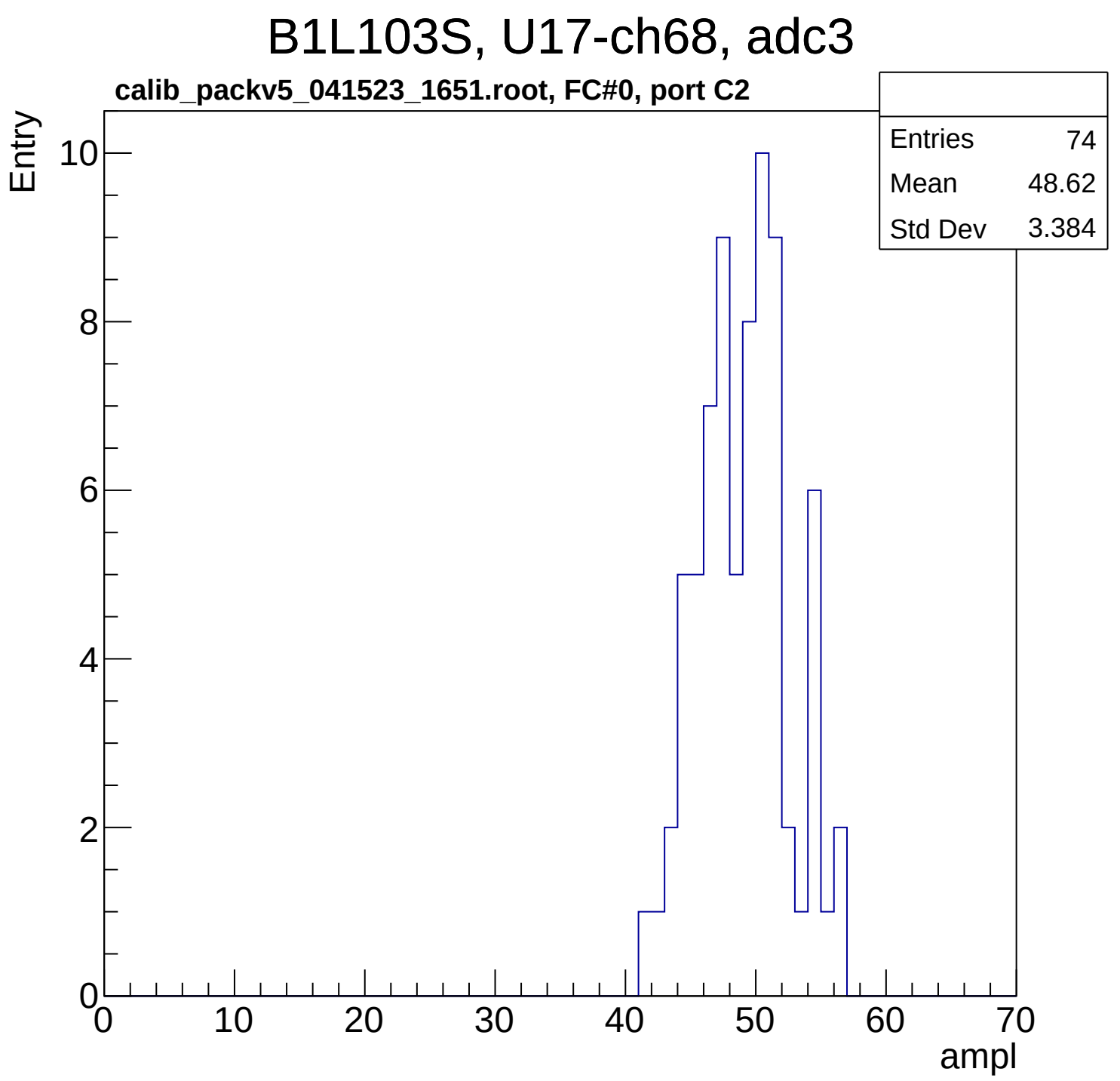

B1L103S, U17-ch67, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.33
Std Dev 0.7454
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

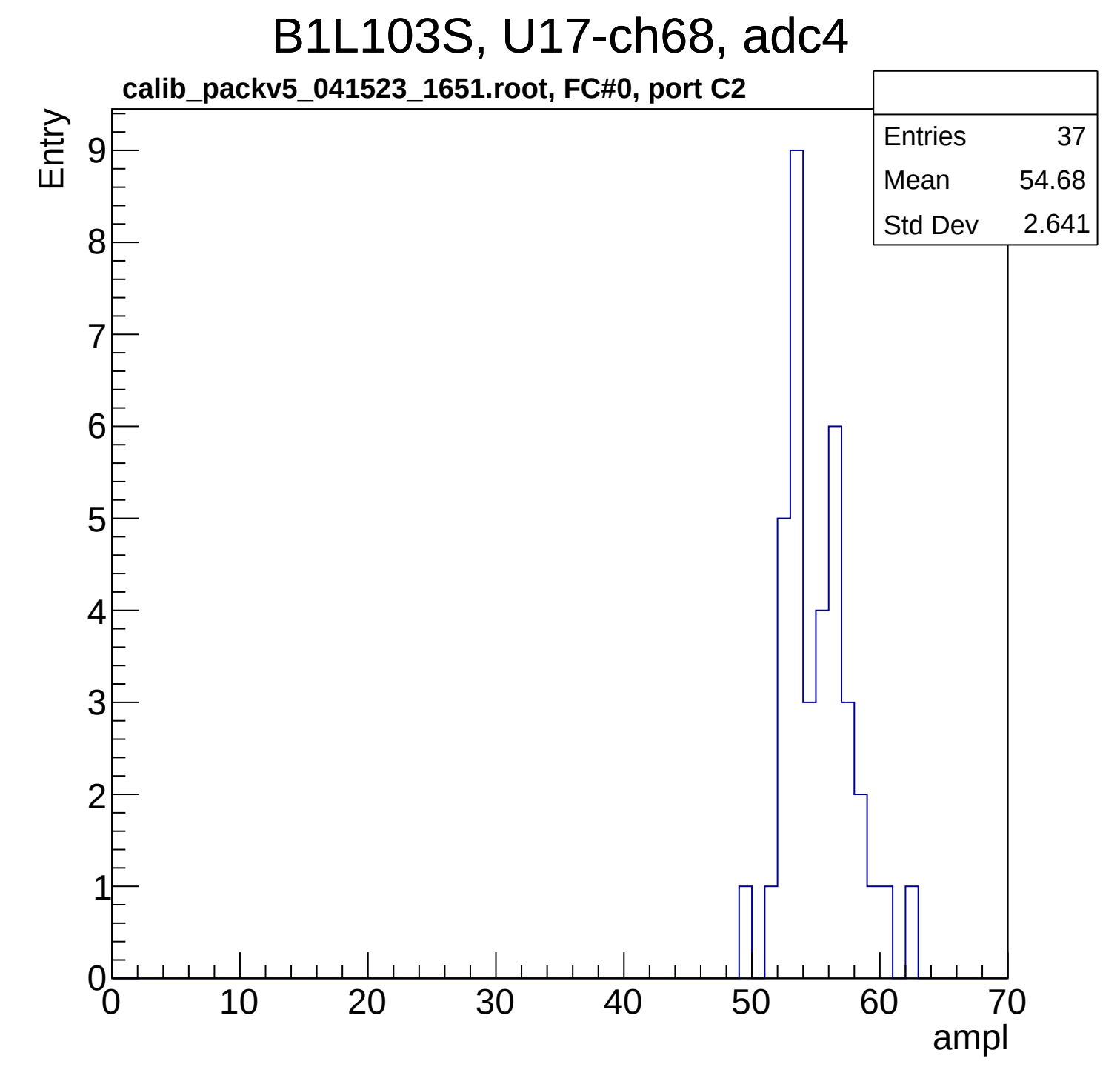

B1L103S, U17-ch67, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

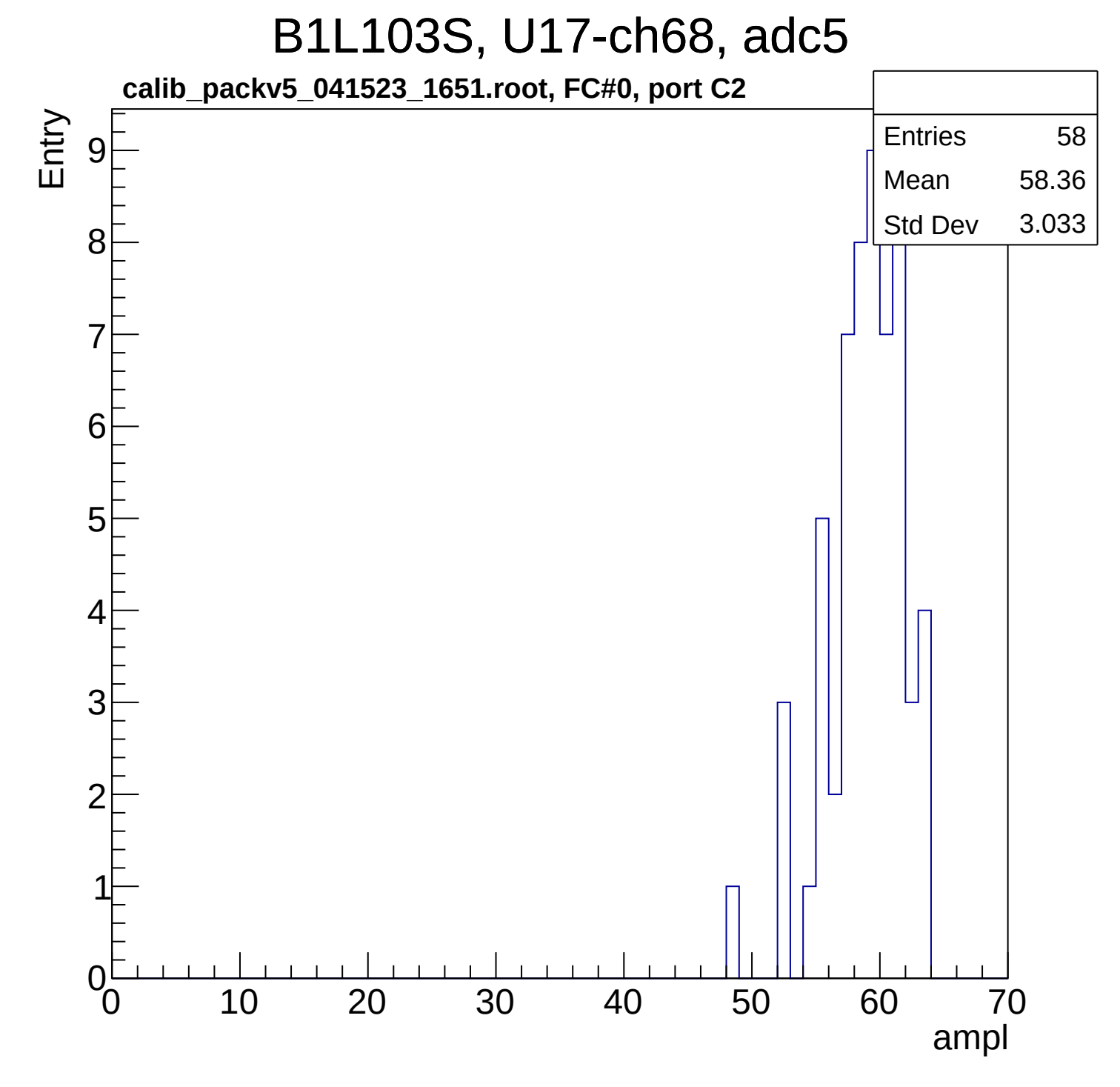

B1L103S, U17-ch68, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 22.28
Std Dev 11.23
Gaus mean : 28.2505
Gaus Width: 3.8269
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

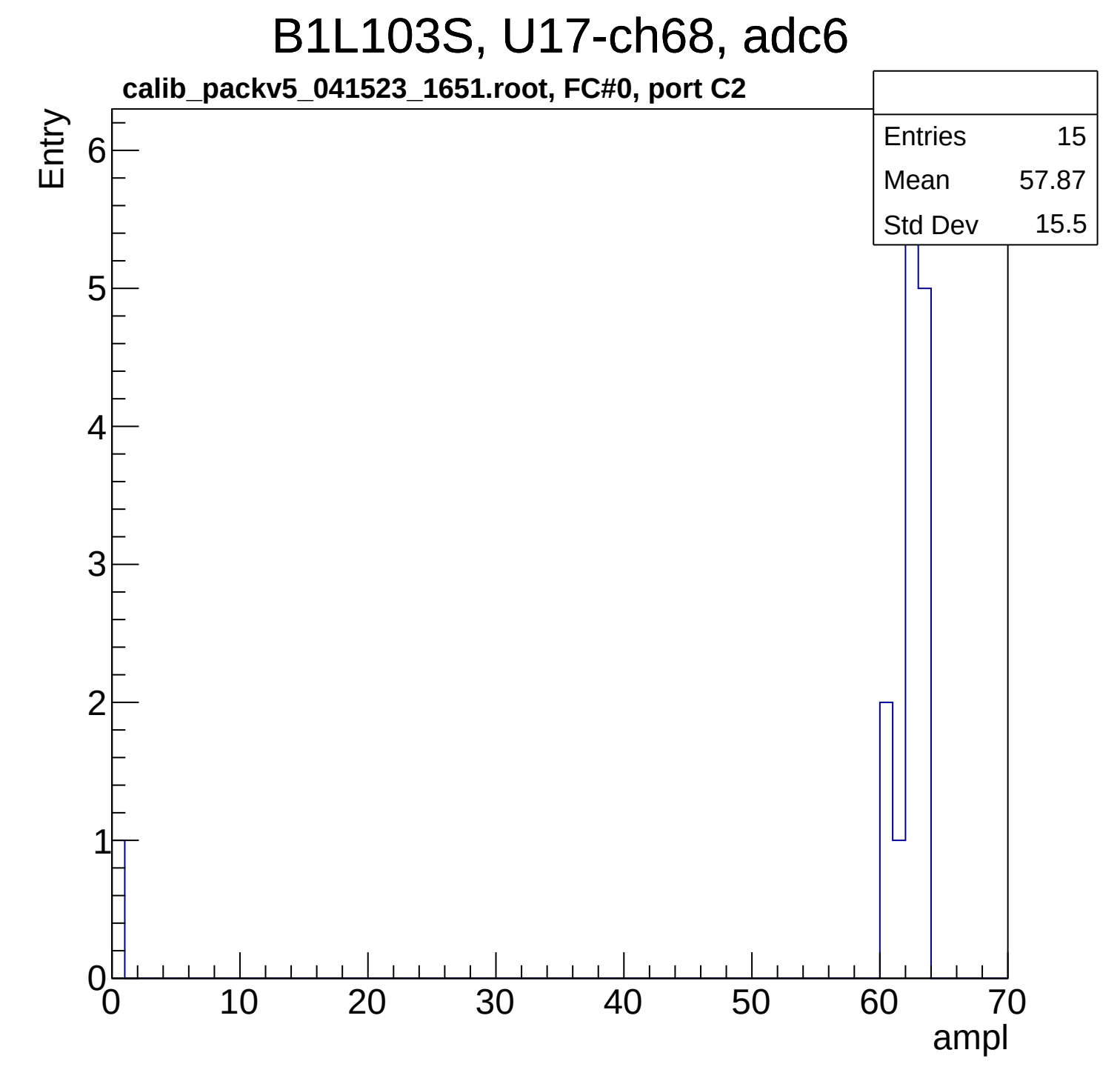

B1L103S, U17-ch68, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 32.77
Std Dev 9.31
Gaus mean : 35.2968
Gaus Width: 3.9028
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

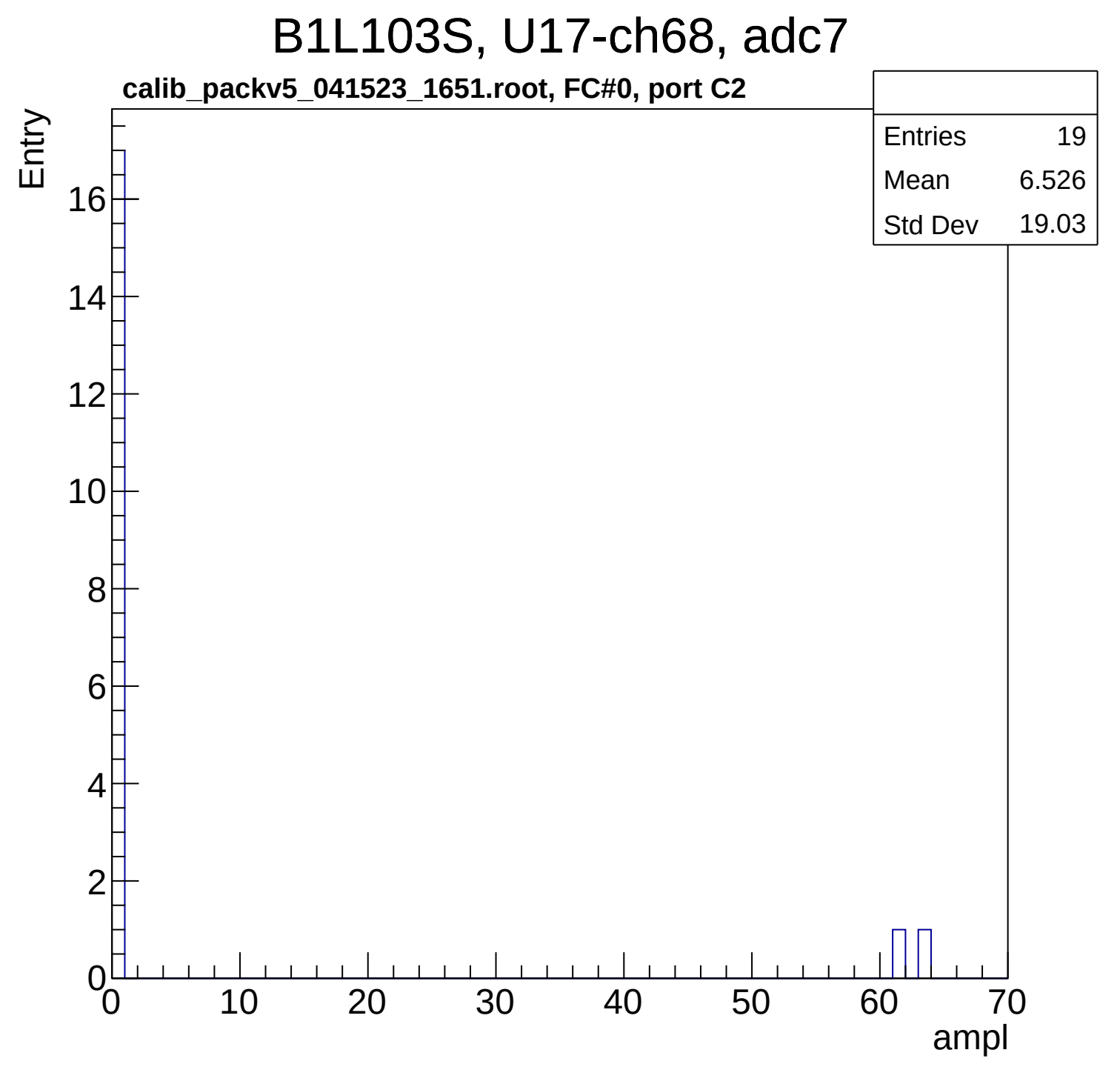

B1L103S, U17-ch68, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 35.32
Std Dev 15.8
Gaus mean : 42.5171
Gaus Width: 3.3075
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

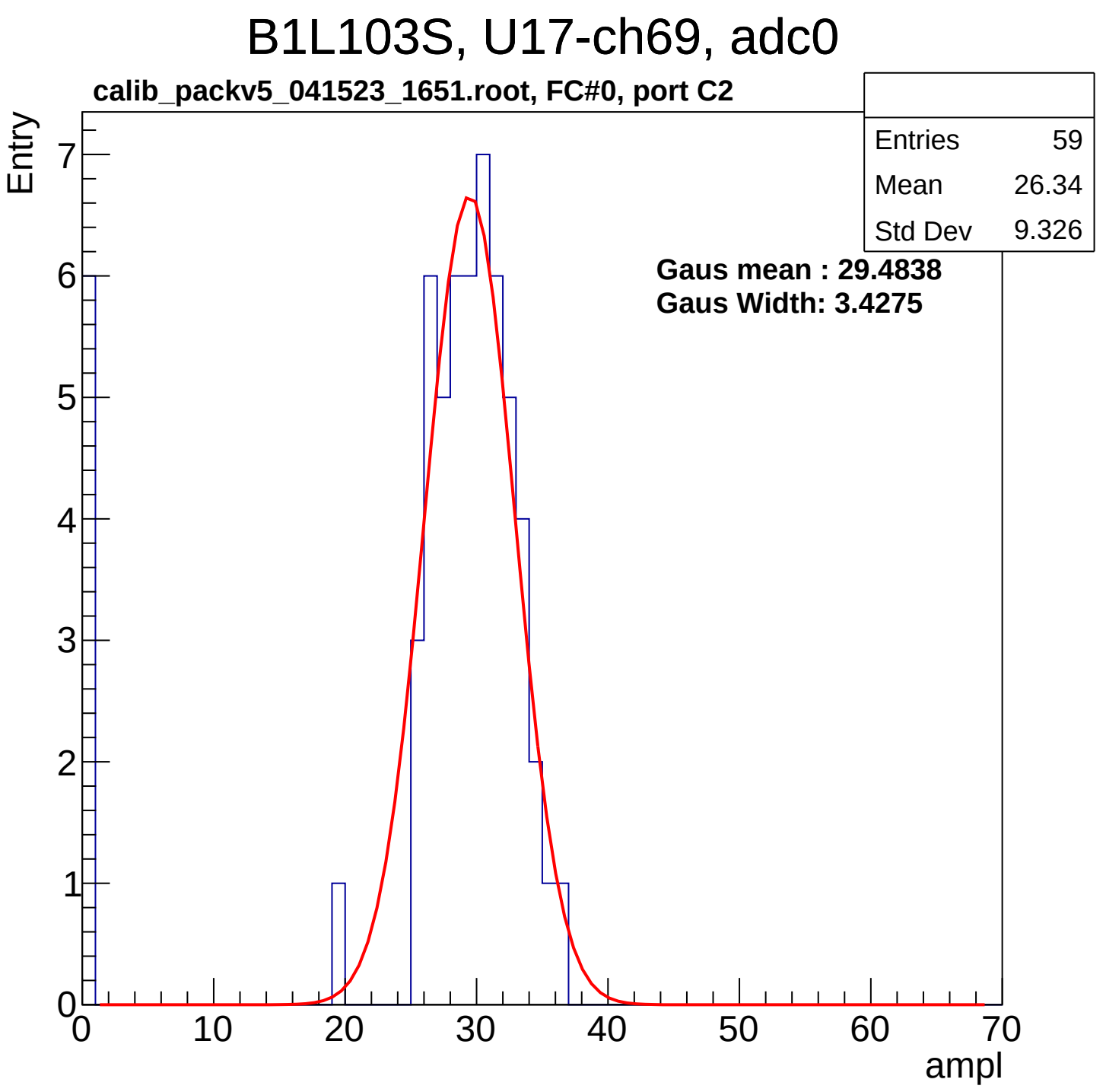

B1L103S, U17-ch68, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 48.62
Std Dev 3.384
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

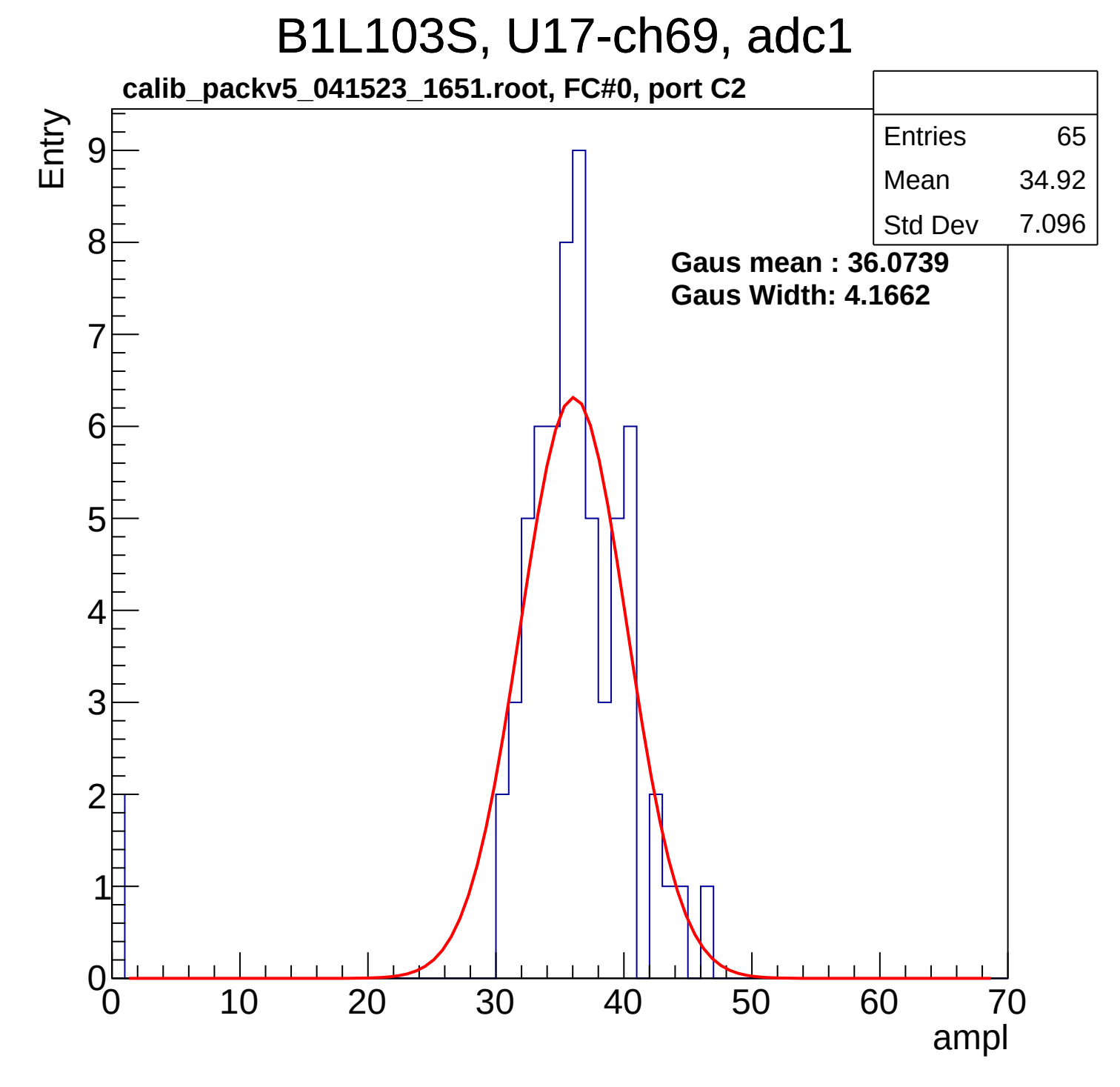

B1L103S, U17-ch68, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 54.68
Std Dev 2.641
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

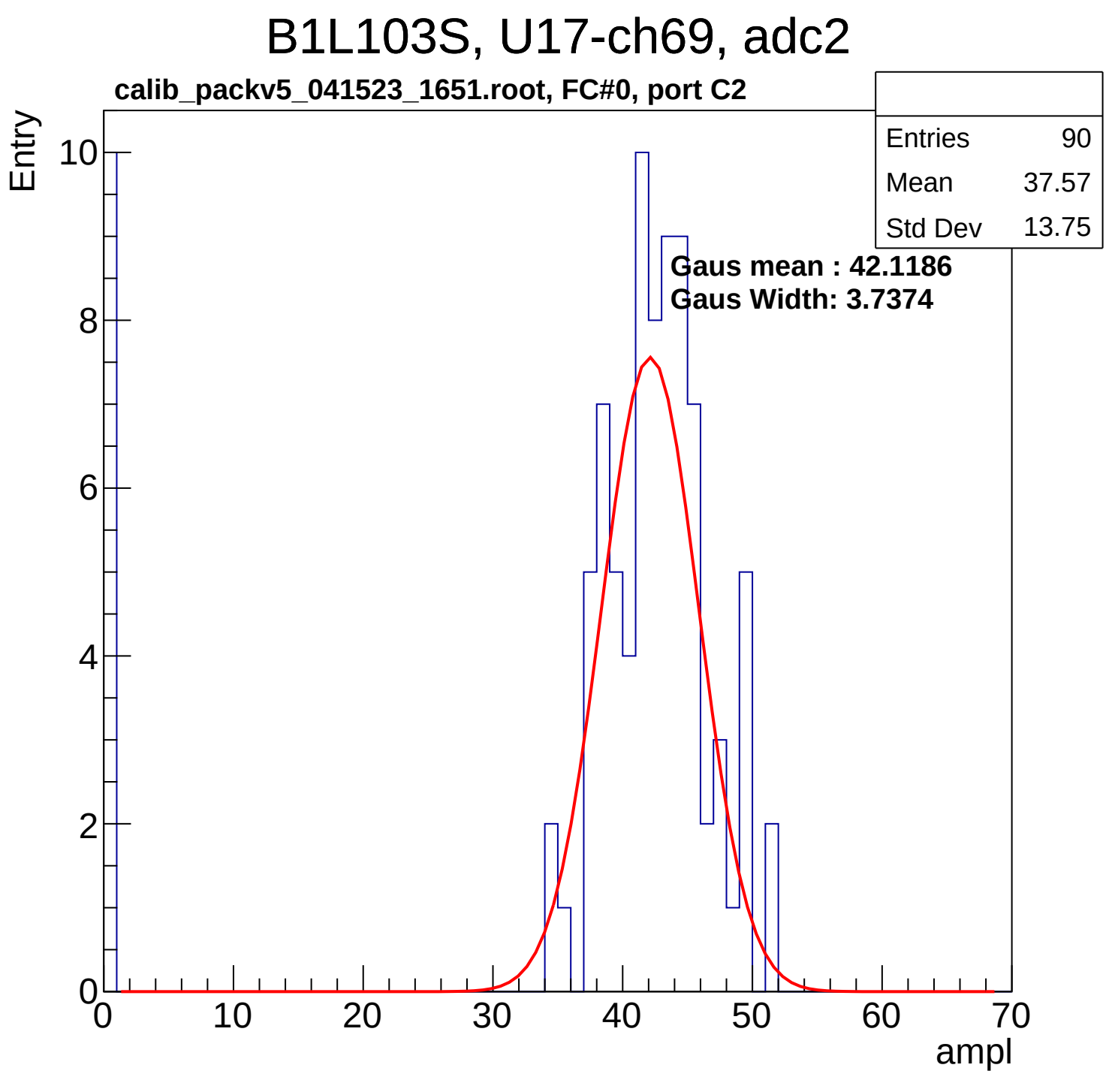

B1L103S, U17-ch68, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.36
Std Dev 3.033
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

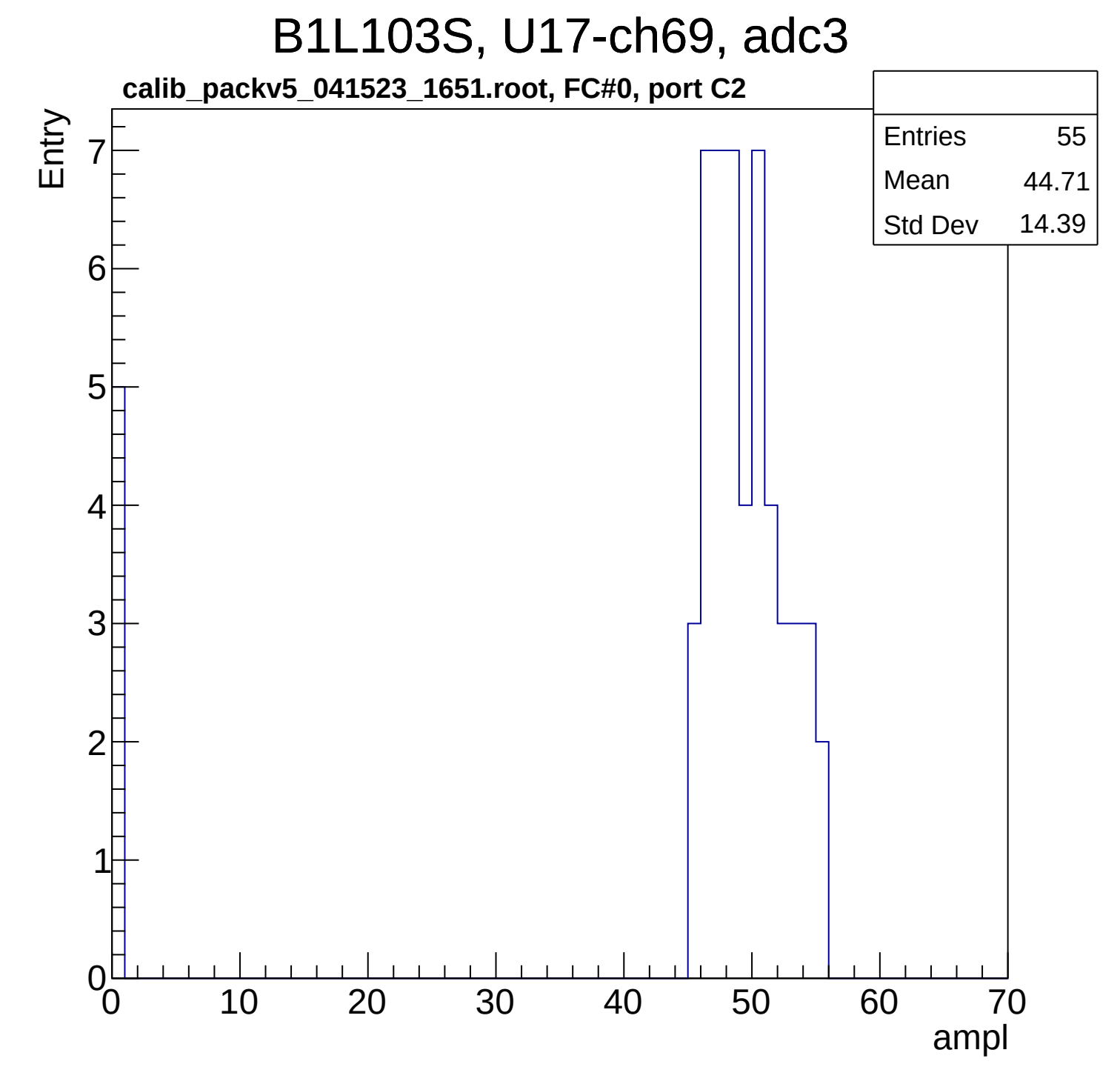

B1L103S, U17-ch68, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.87
Std Dev 15.5
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

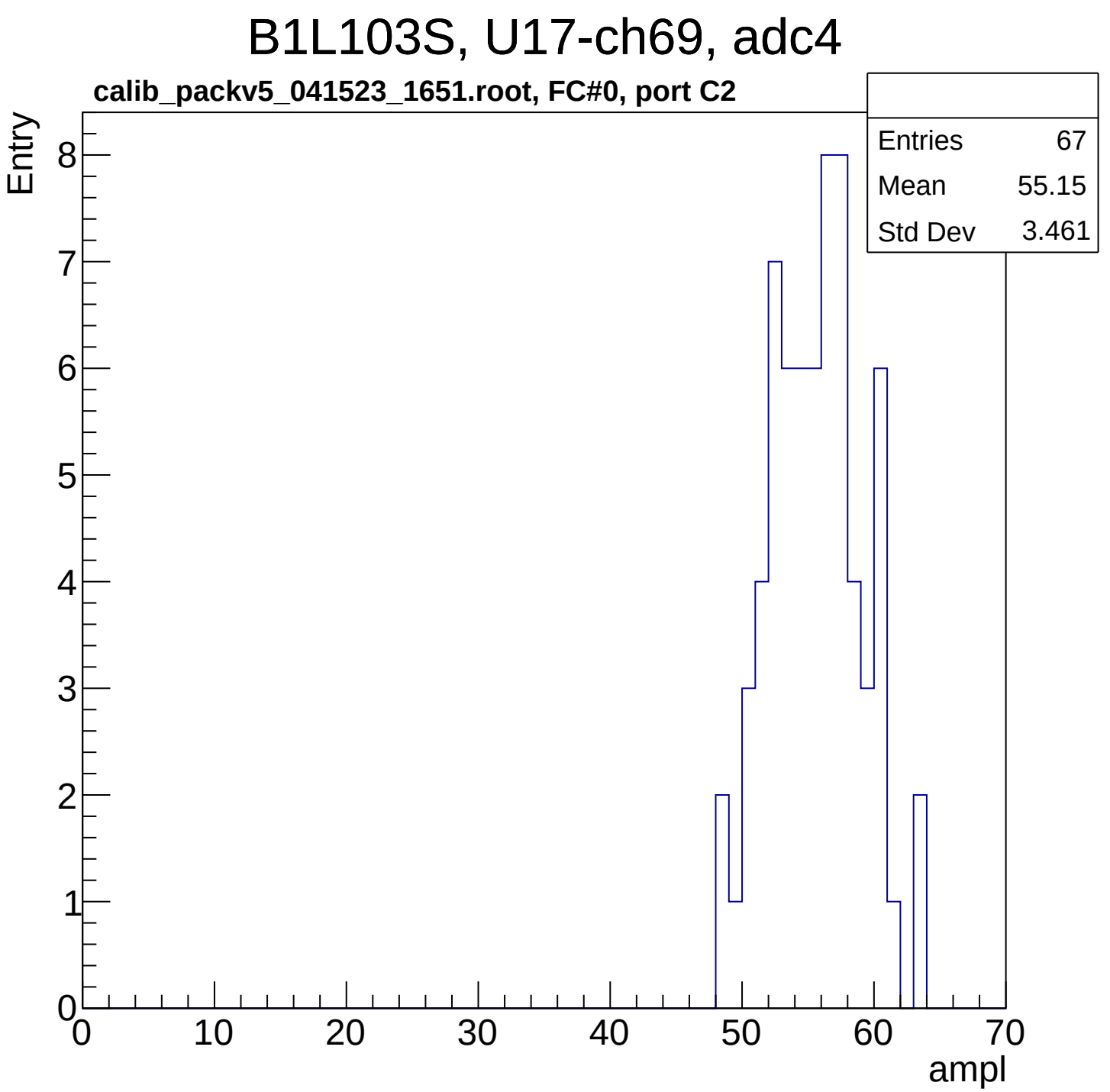

B1L103S, U17-ch68, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 6.526
Std Dev 19.03
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

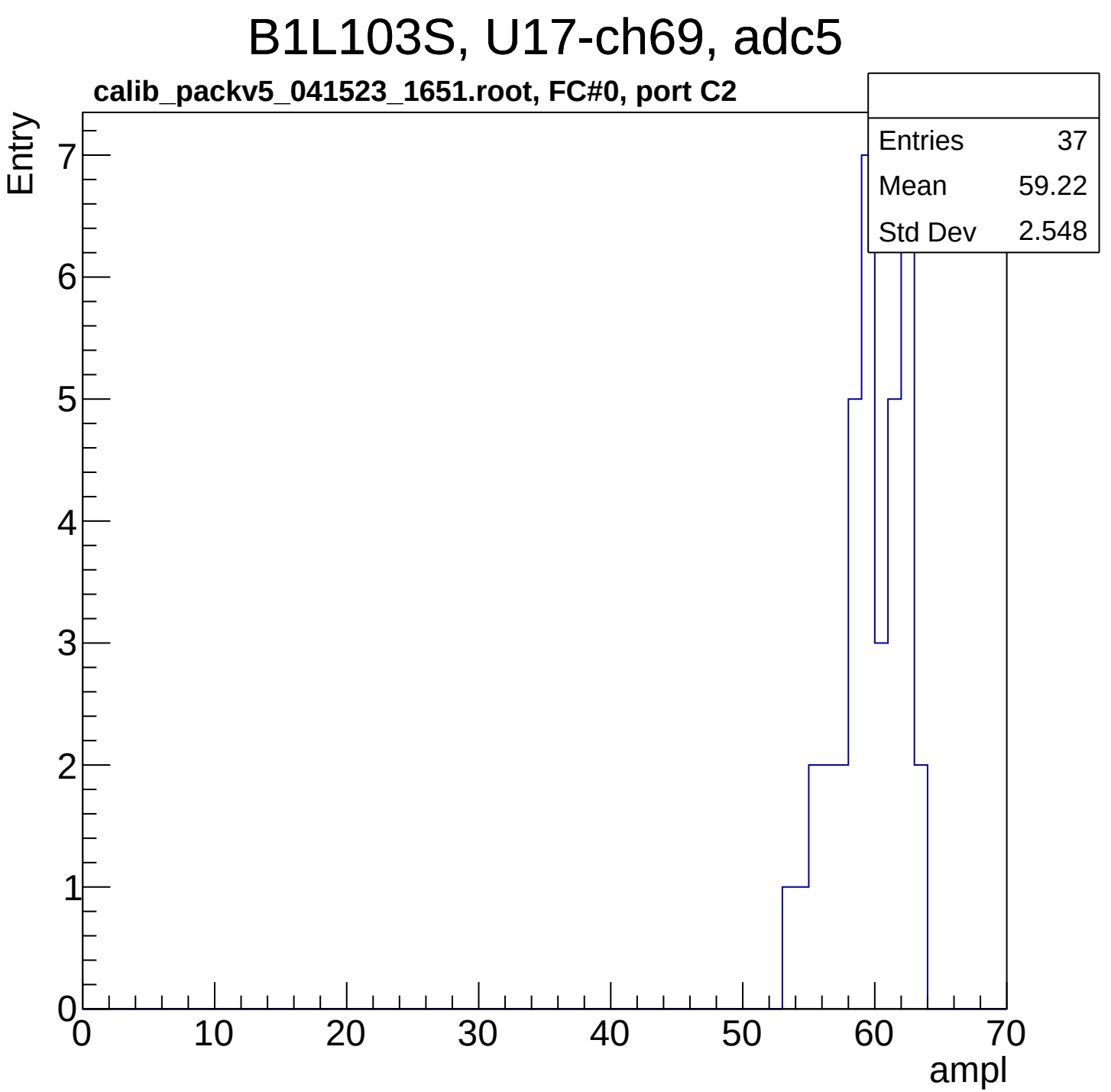

B1L103S, U17-ch69, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 26.34
Std Dev 9.326
Gaus mean : 29.4838
Gaus Width: 3.4275
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

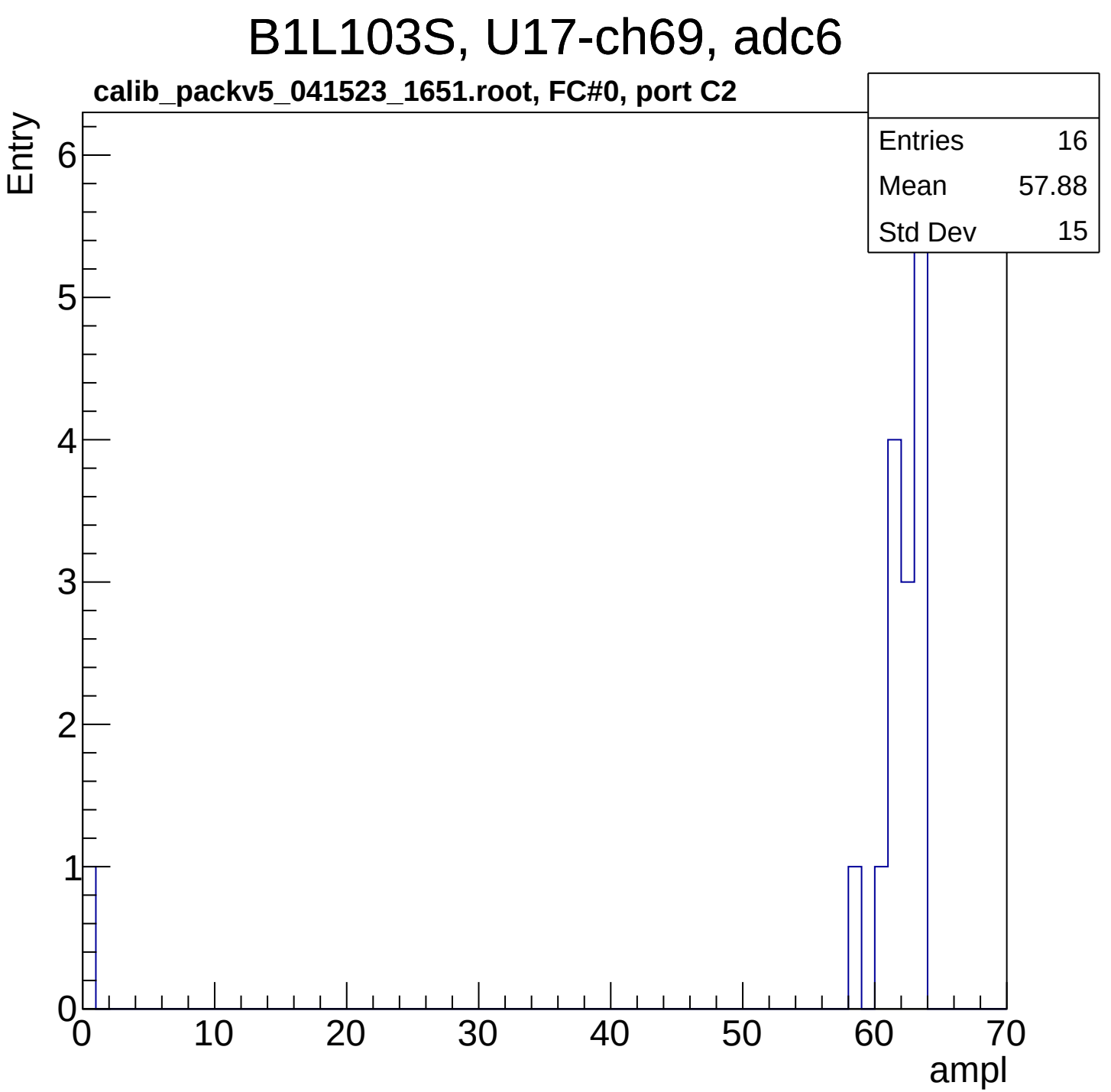

B1L103S, U17-ch69, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 34.92
Std Dev 7.096
Gaus mean : 36.0739
Gaus Width: 4.1662
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

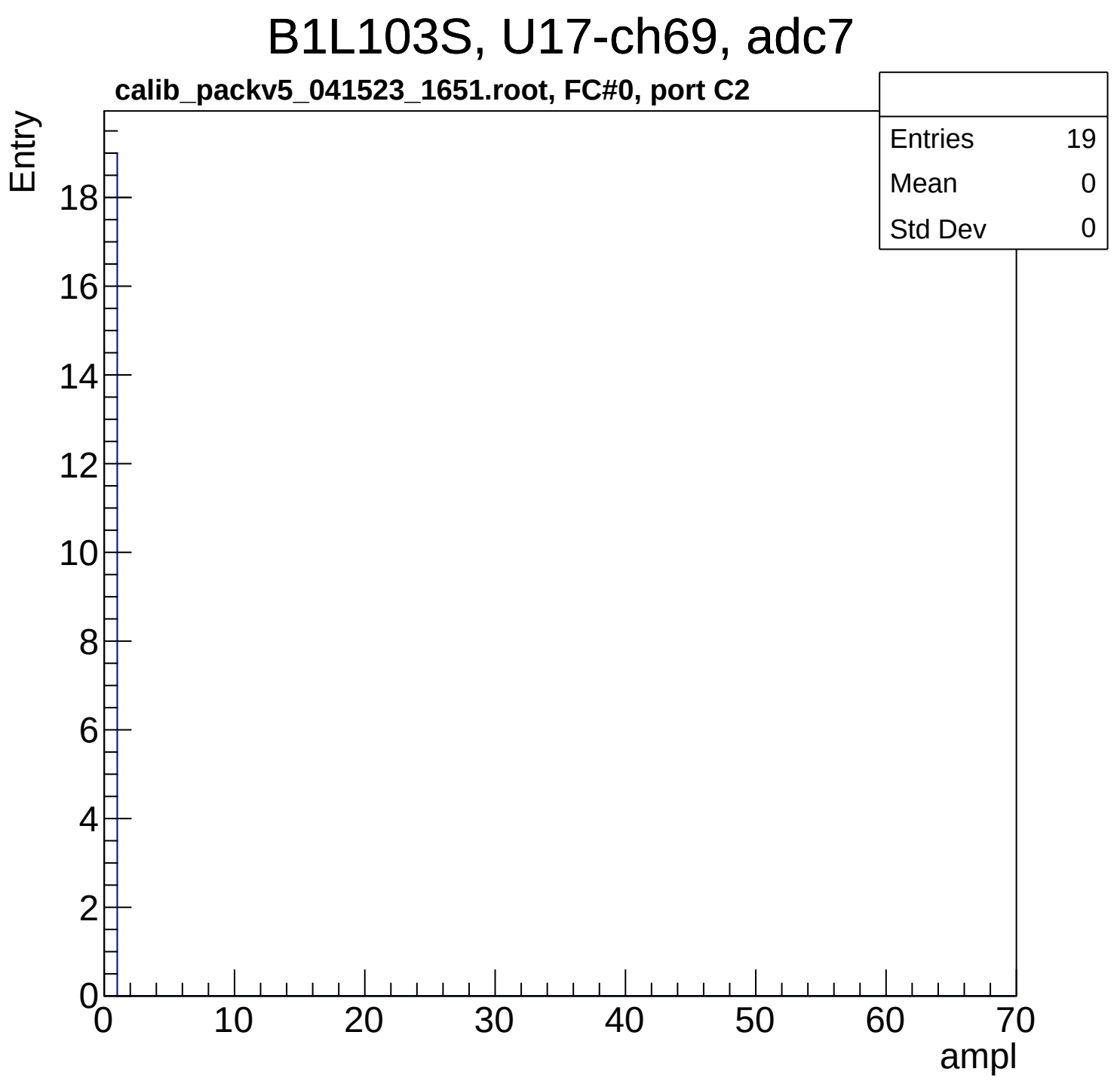

B1L103S, U17-ch69, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 37.57
Std Dev 13.75
Gaus mean : 42.1186
Gaus Width: 3.7374
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

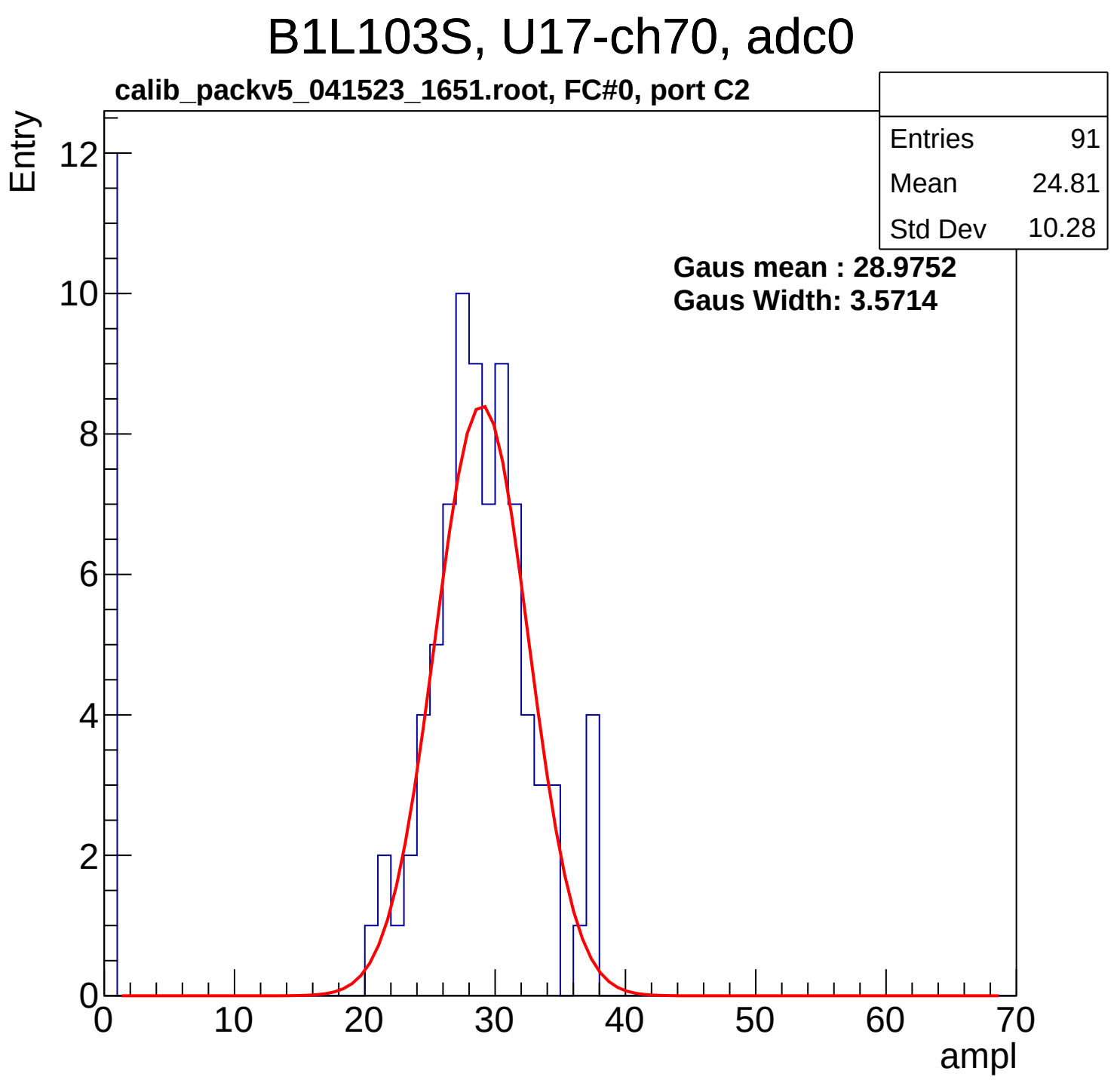

B1L103S, U17-ch69, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 44.71
Std Dev 14.39
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

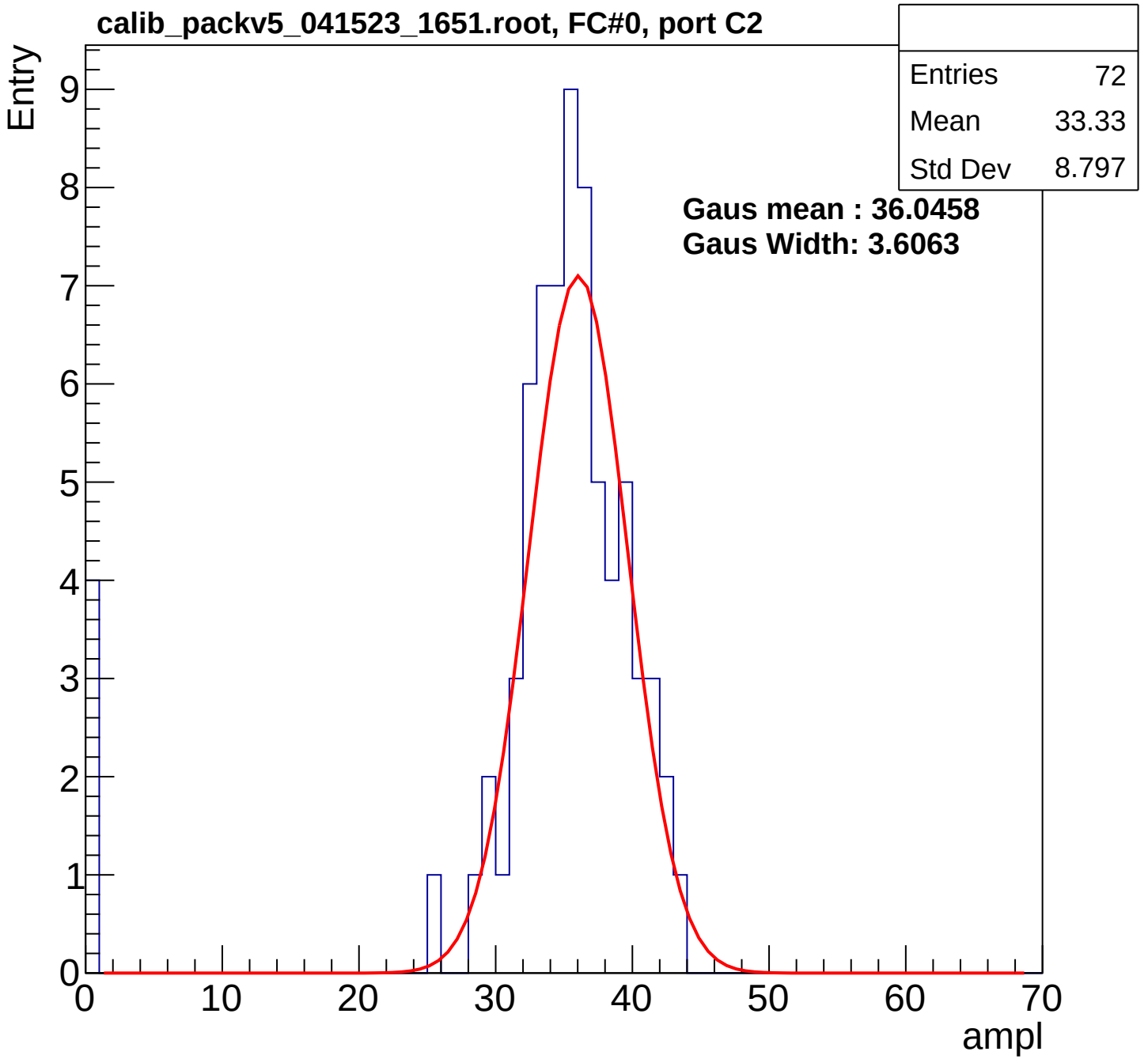

B1L103S, U17-ch69, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 55.15
Std Dev 3.461
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

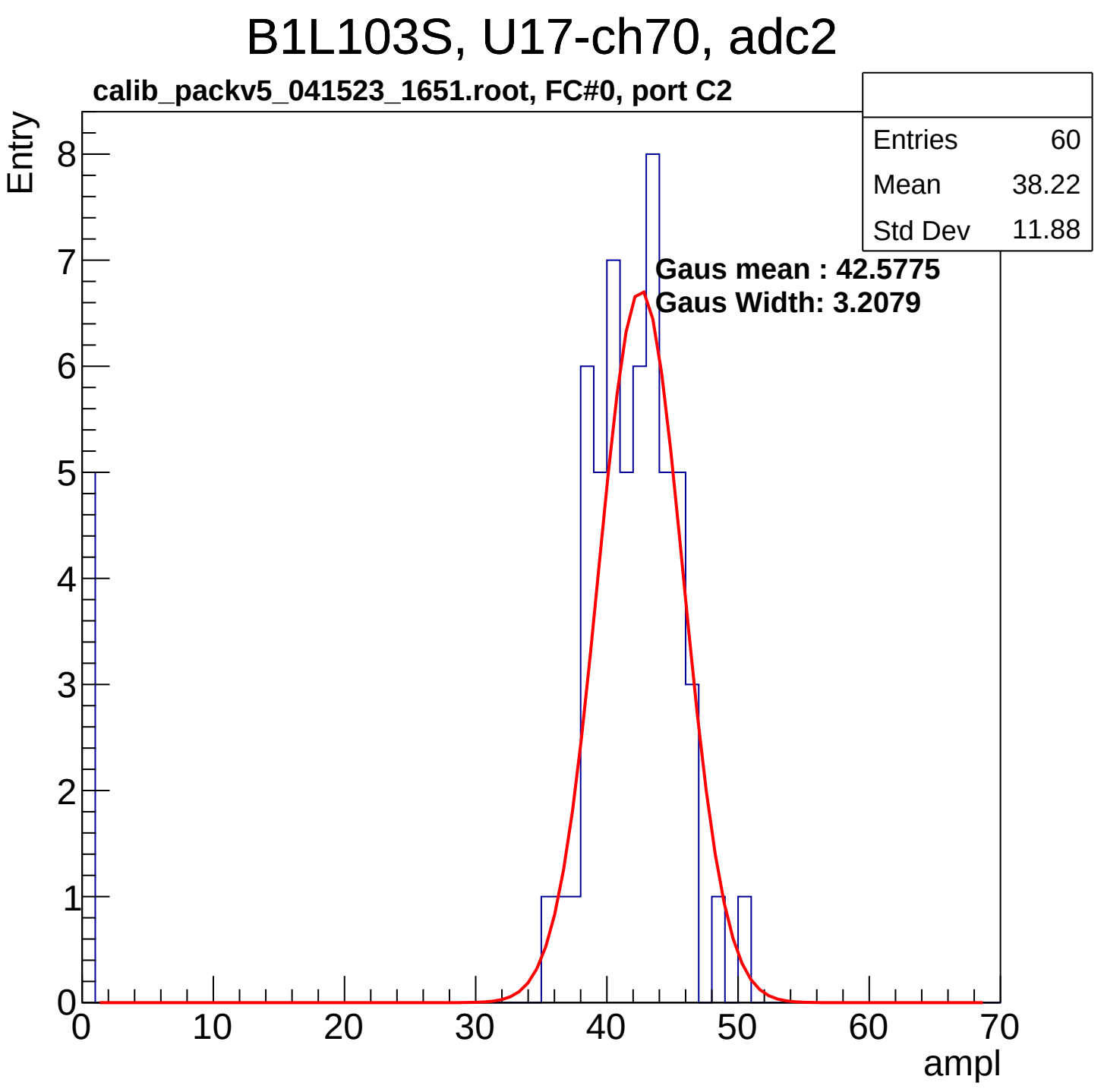

B1L103S, U17-ch69, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 59.22
Std Dev 2.548
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

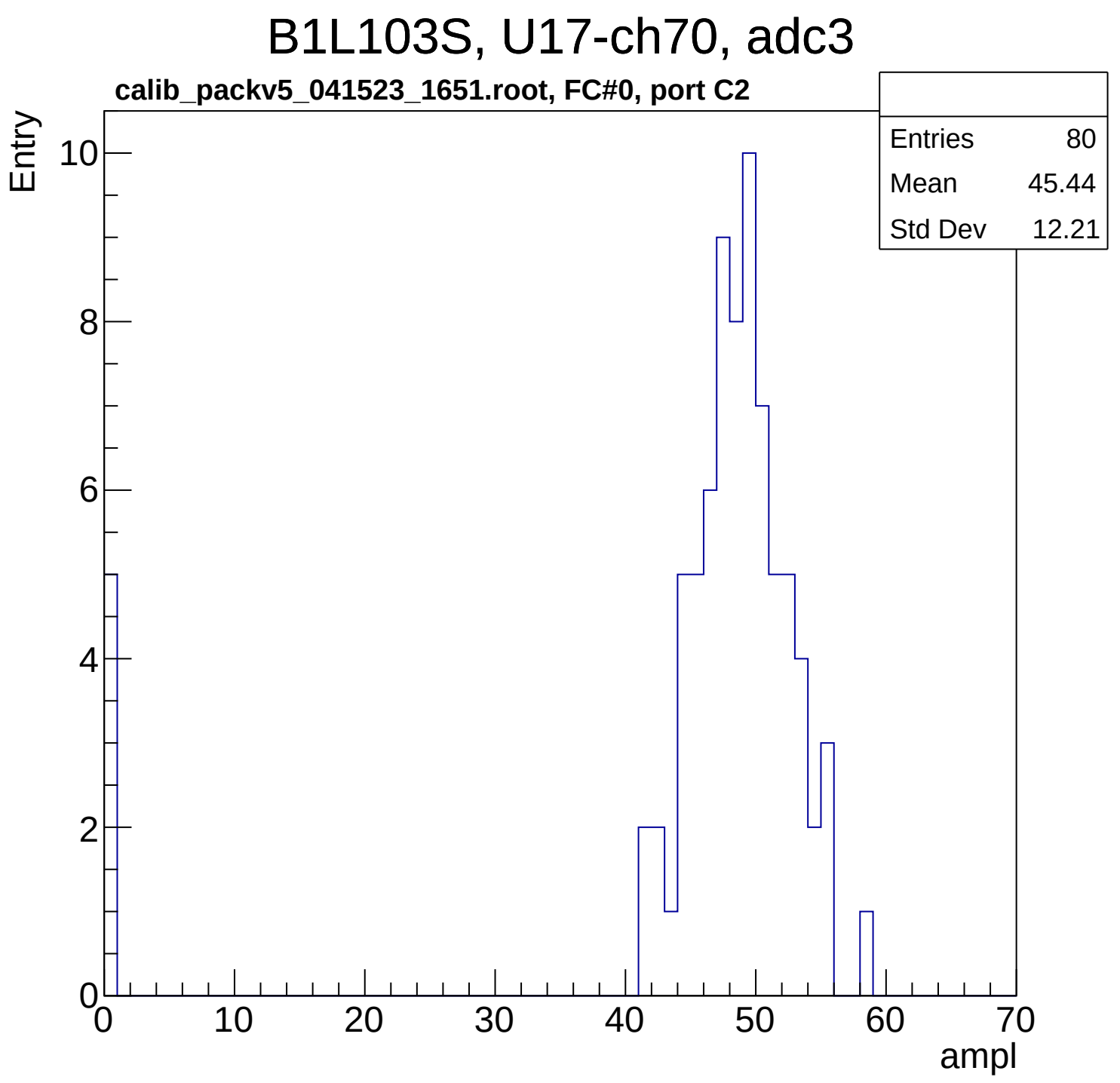

B1L103S, U17-ch69, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.88
Std Dev 15
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

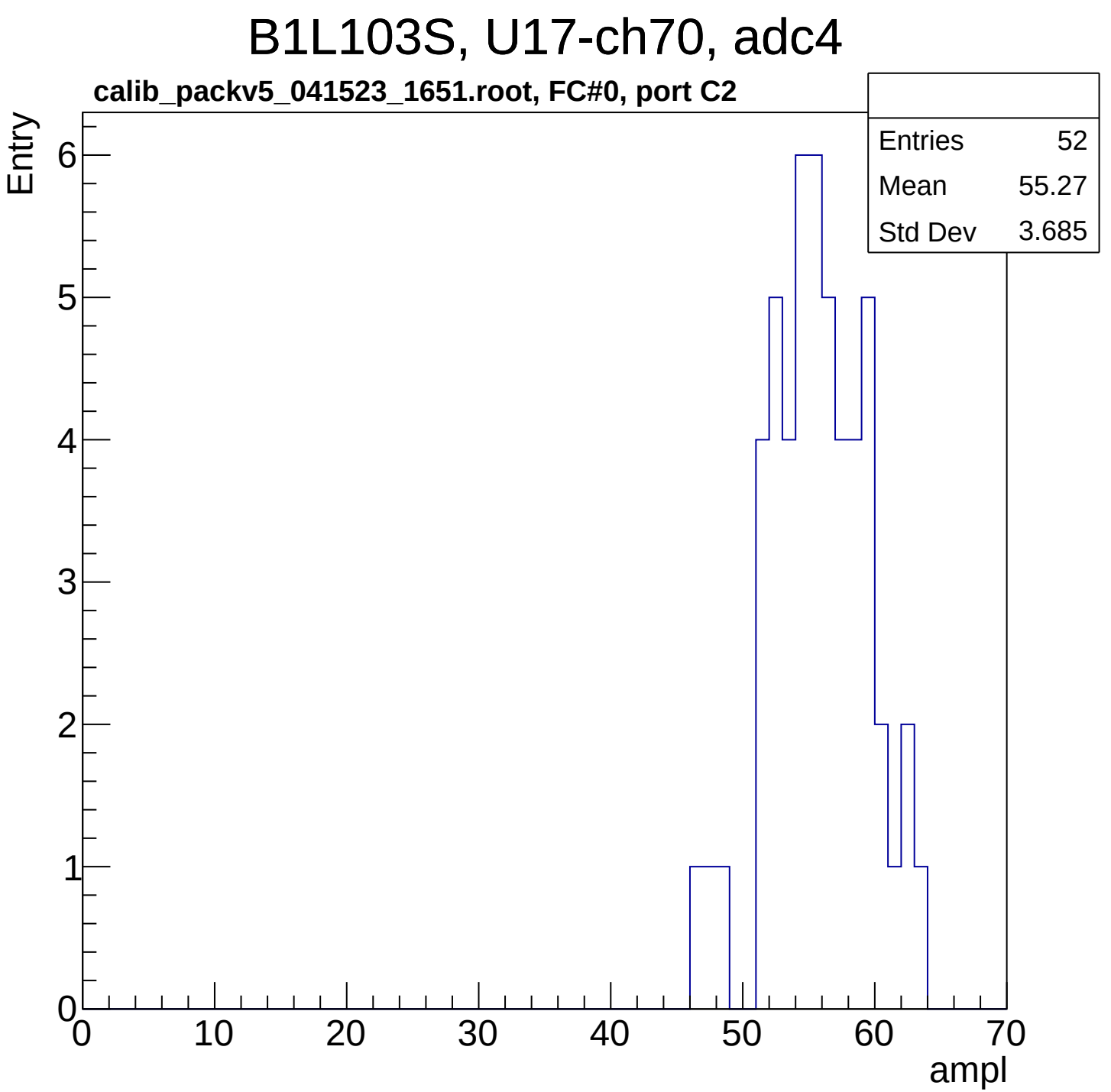

B1L103S, U17-ch69, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

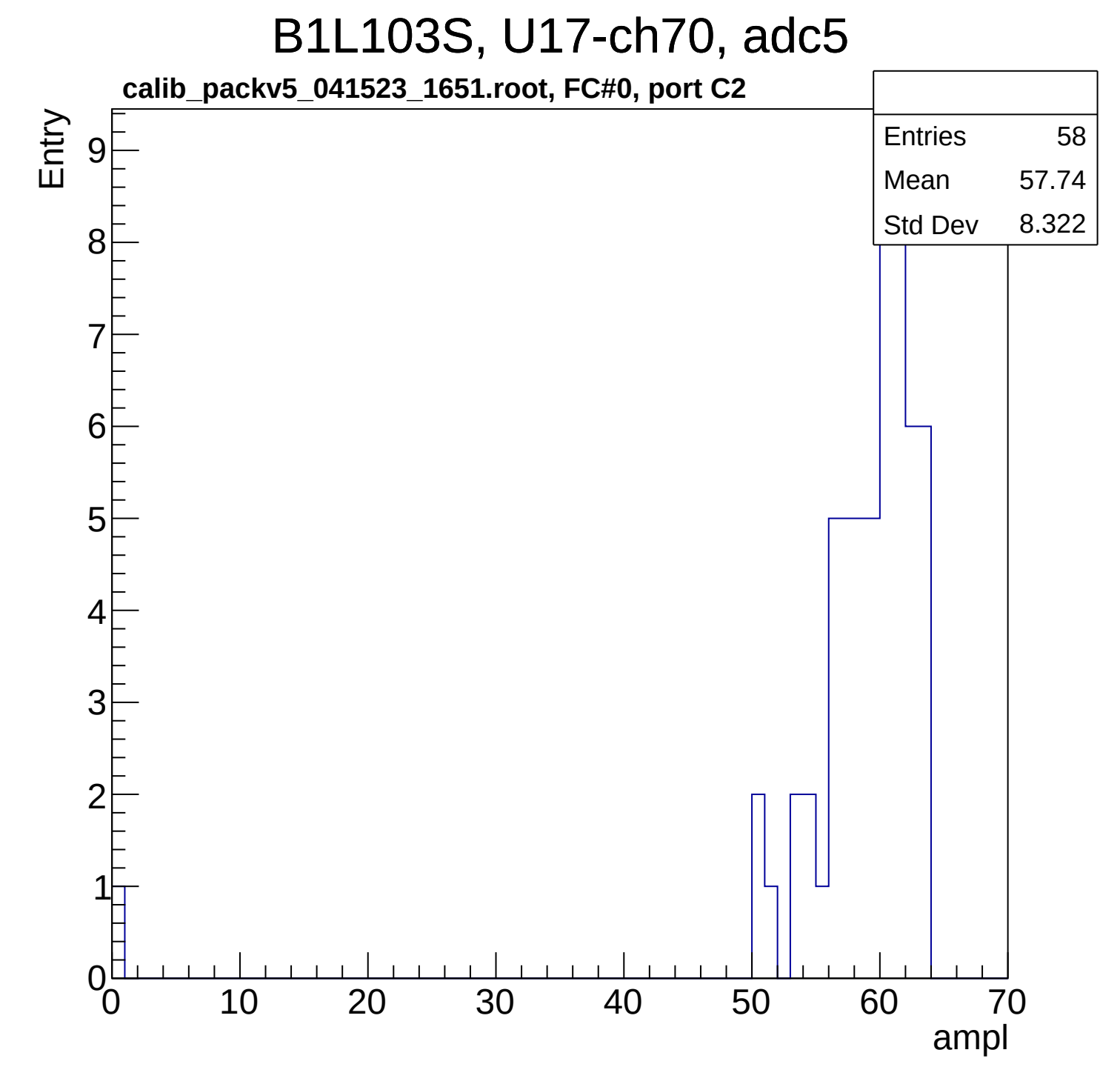

B1L103S, U17-ch70, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 24.81
Std Dev 10.28
Gaus mean : 28.9752
Gaus Width: 3.5714
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

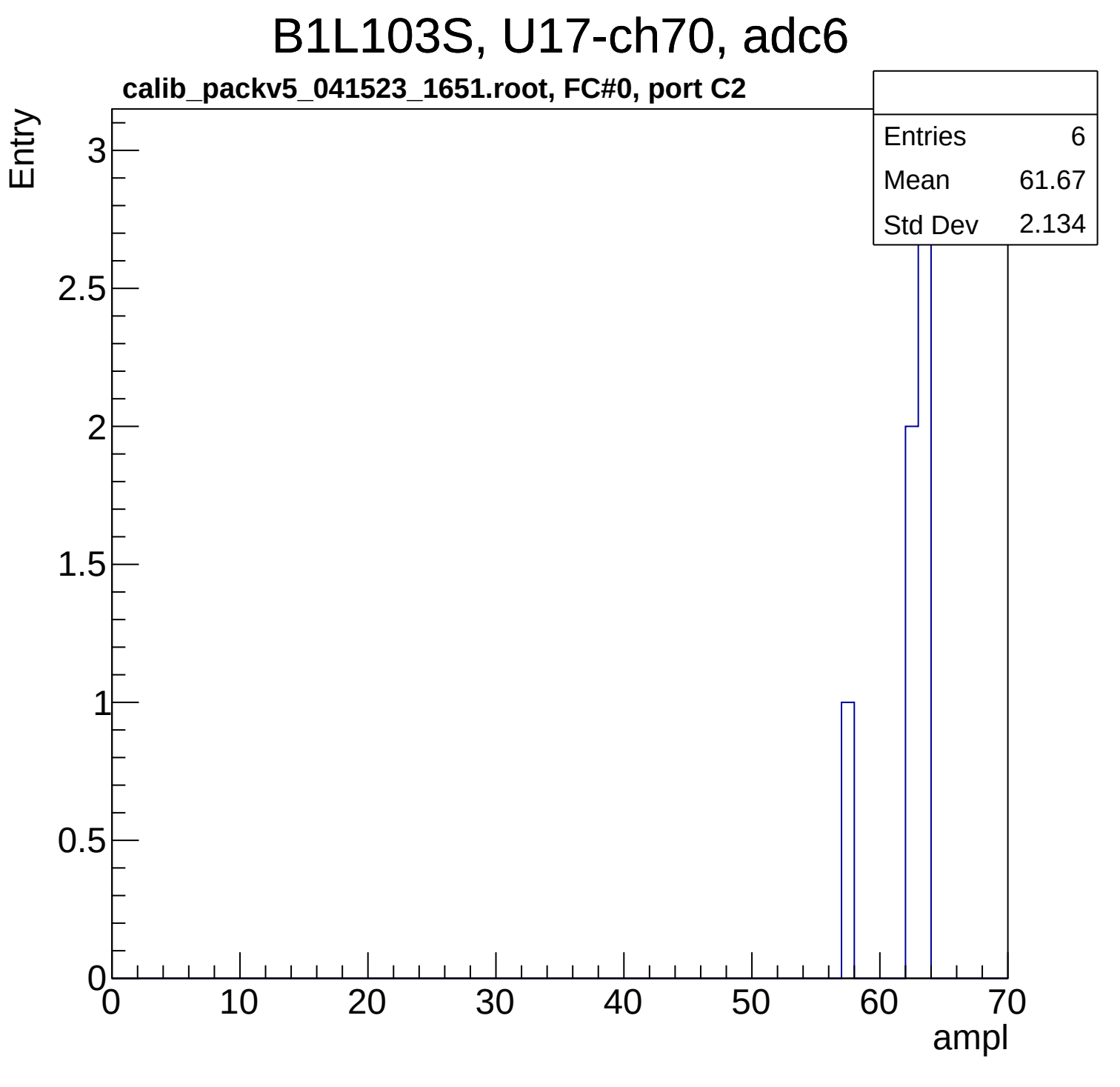

B1L103S, U17-ch70, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 33.33
Std Dev 8.797
Gaus mean : 36.0458
Gaus Width: 3.6063
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

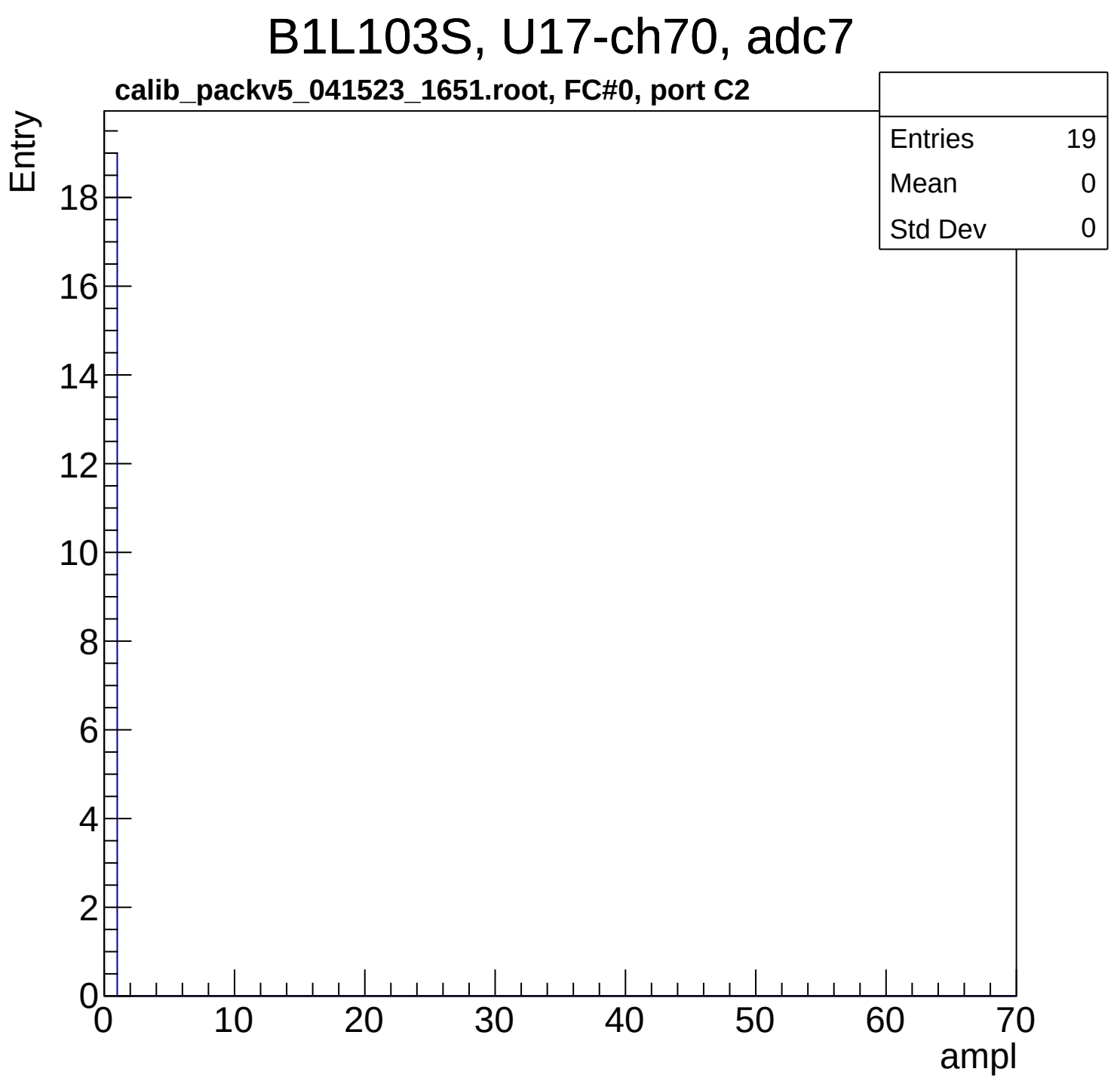

B1L103S, U17-ch70, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 38.22
Std Dev 11.88
Gaus mean : 42.5775
Gaus Width: 3.2079
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

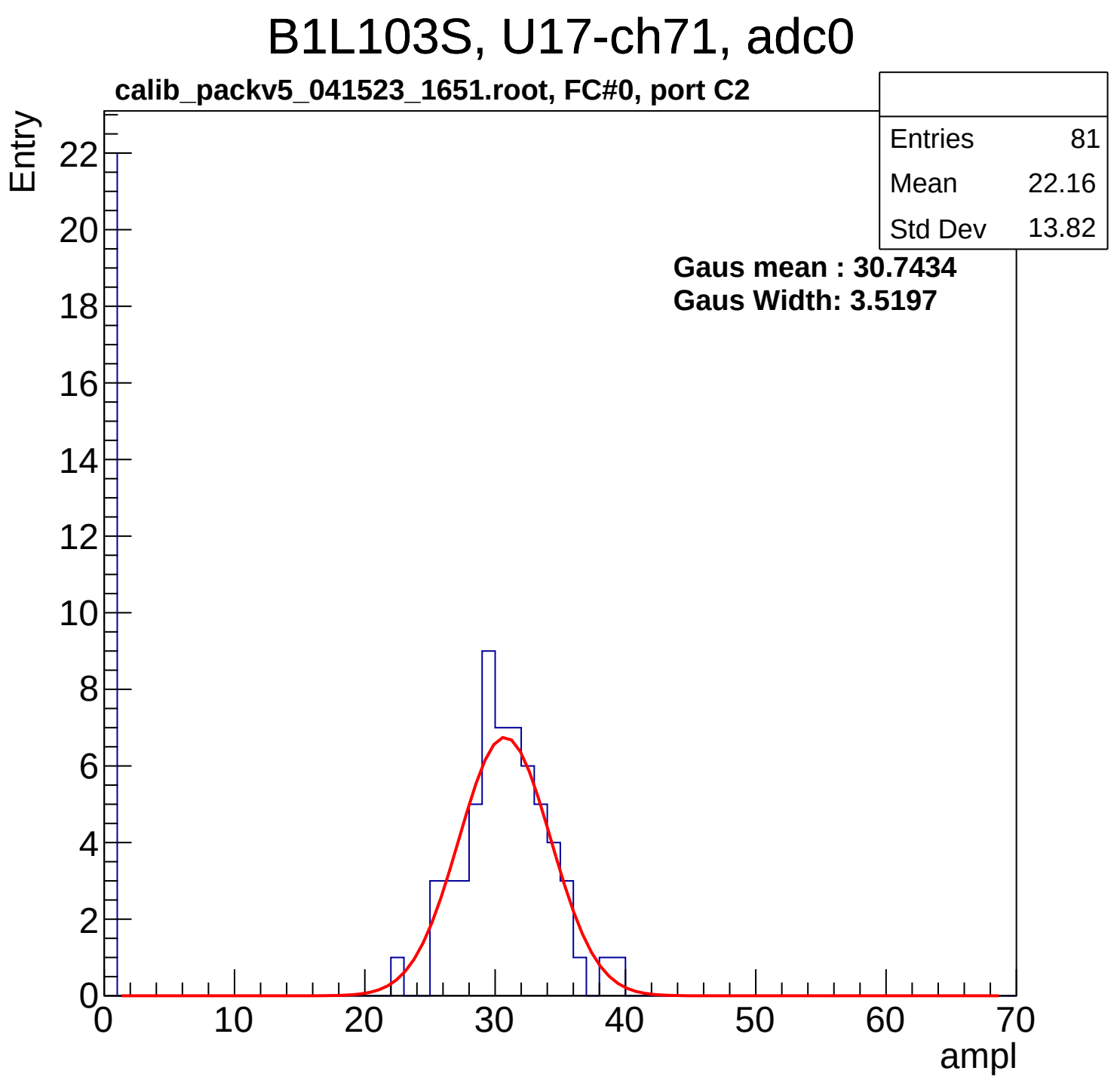

B1L103S, U17-ch70, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 45.44
Std Dev 12.21
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

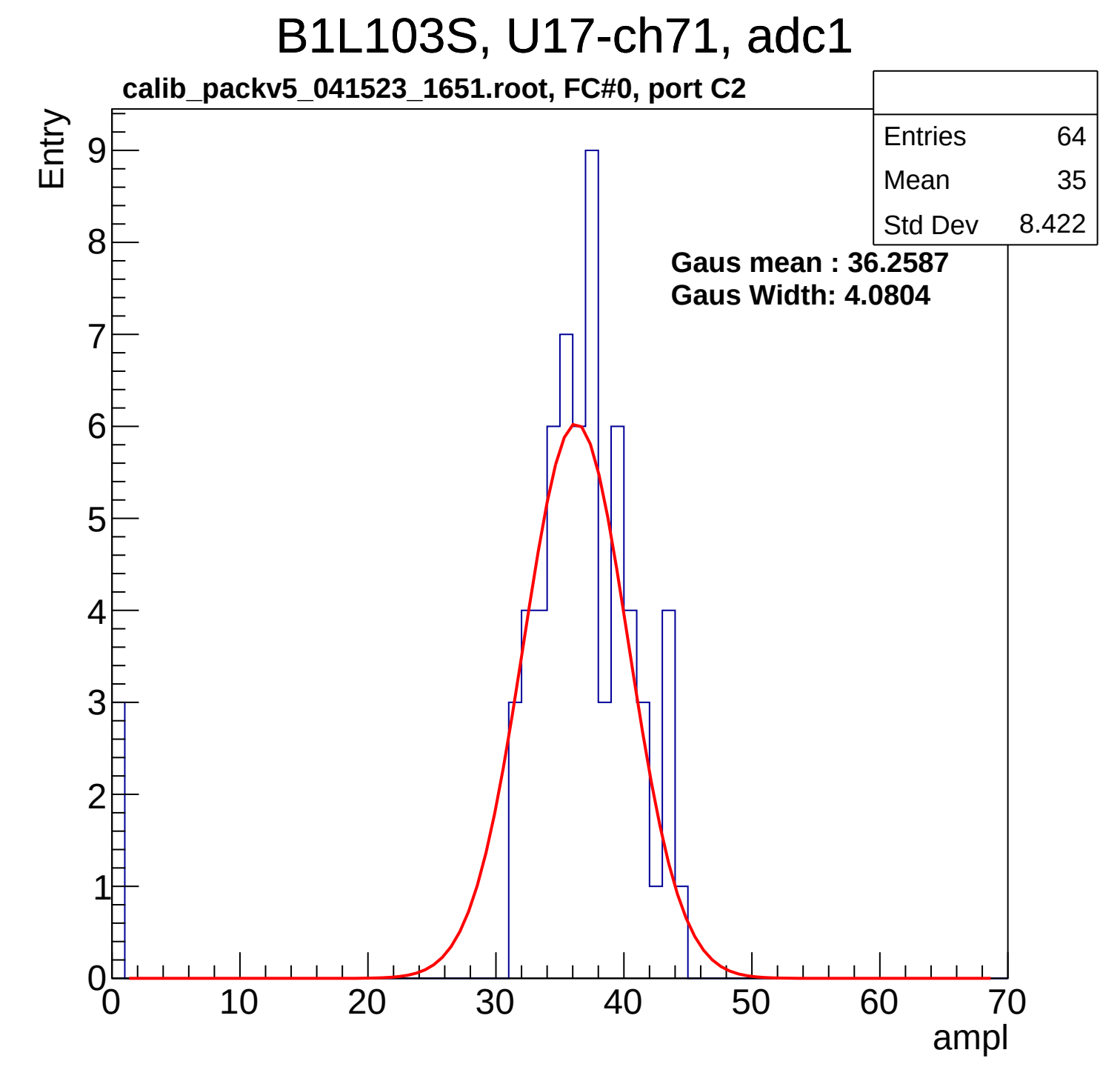

B1L103S, U17-ch70, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 55.27
Std Dev 3.685
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

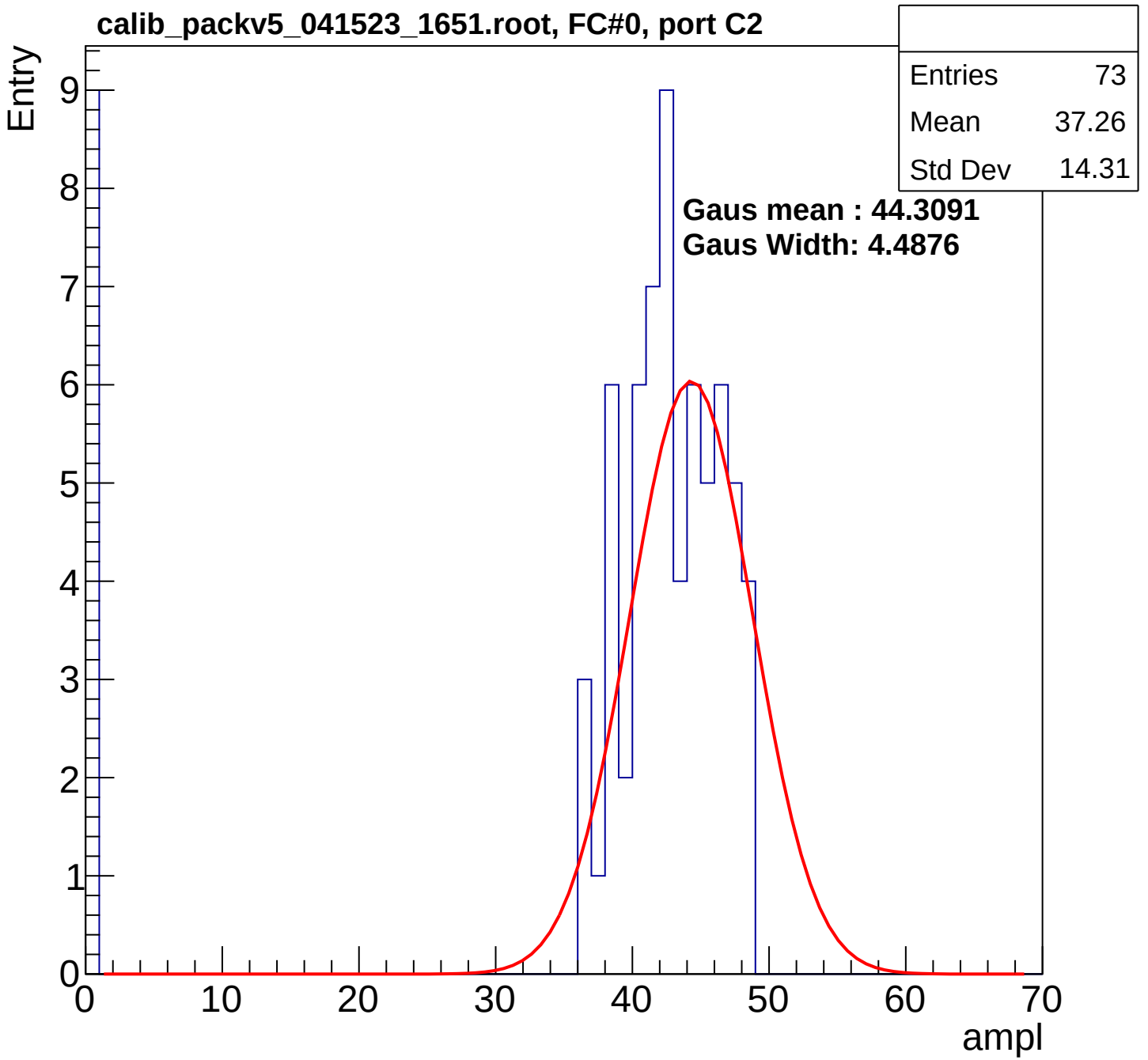

B1L103S, U17-ch70, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 57.74
Std Dev 8.322
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

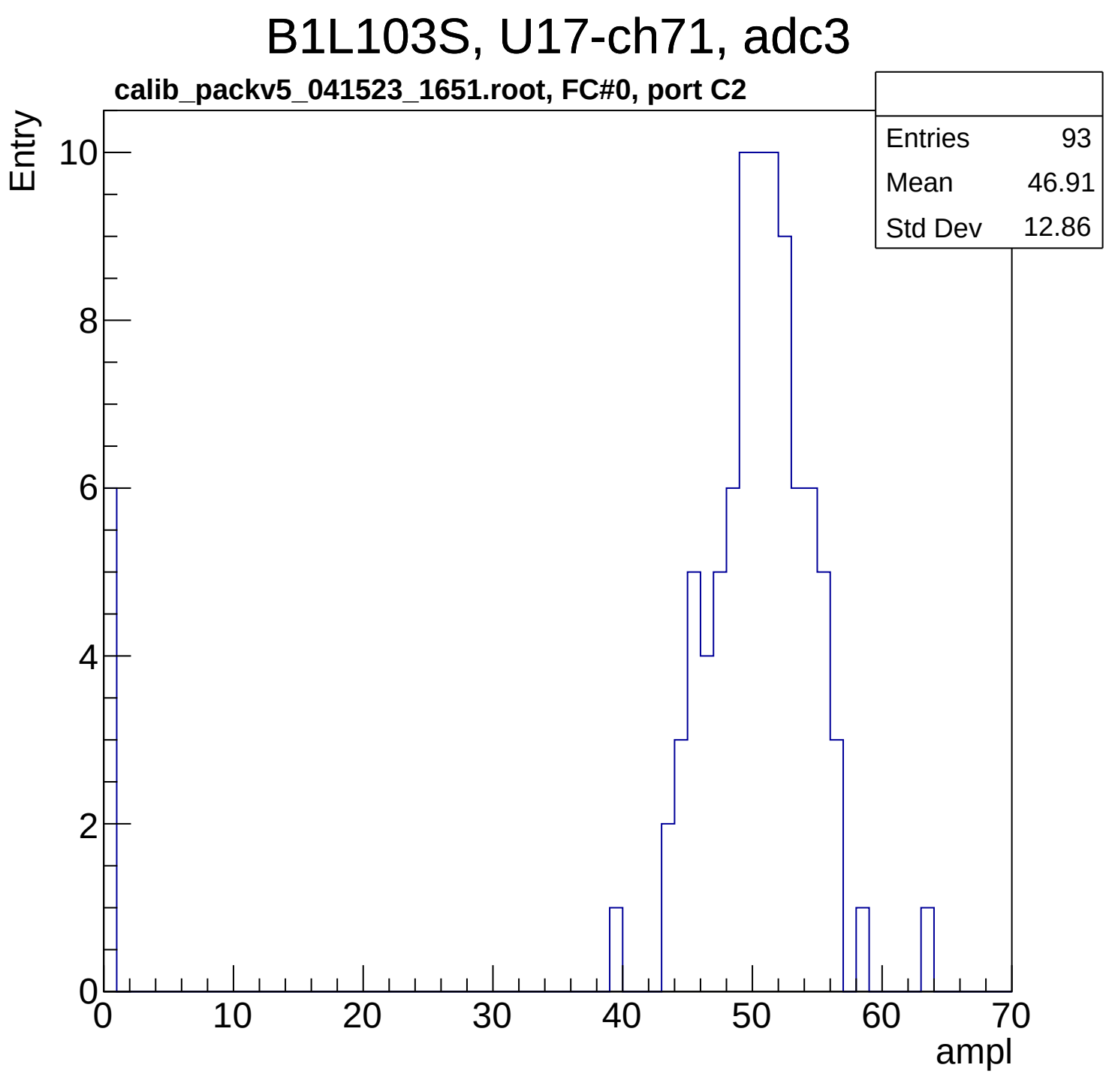

B1L103S, U17-ch70, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.67
Std Dev 2.134
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

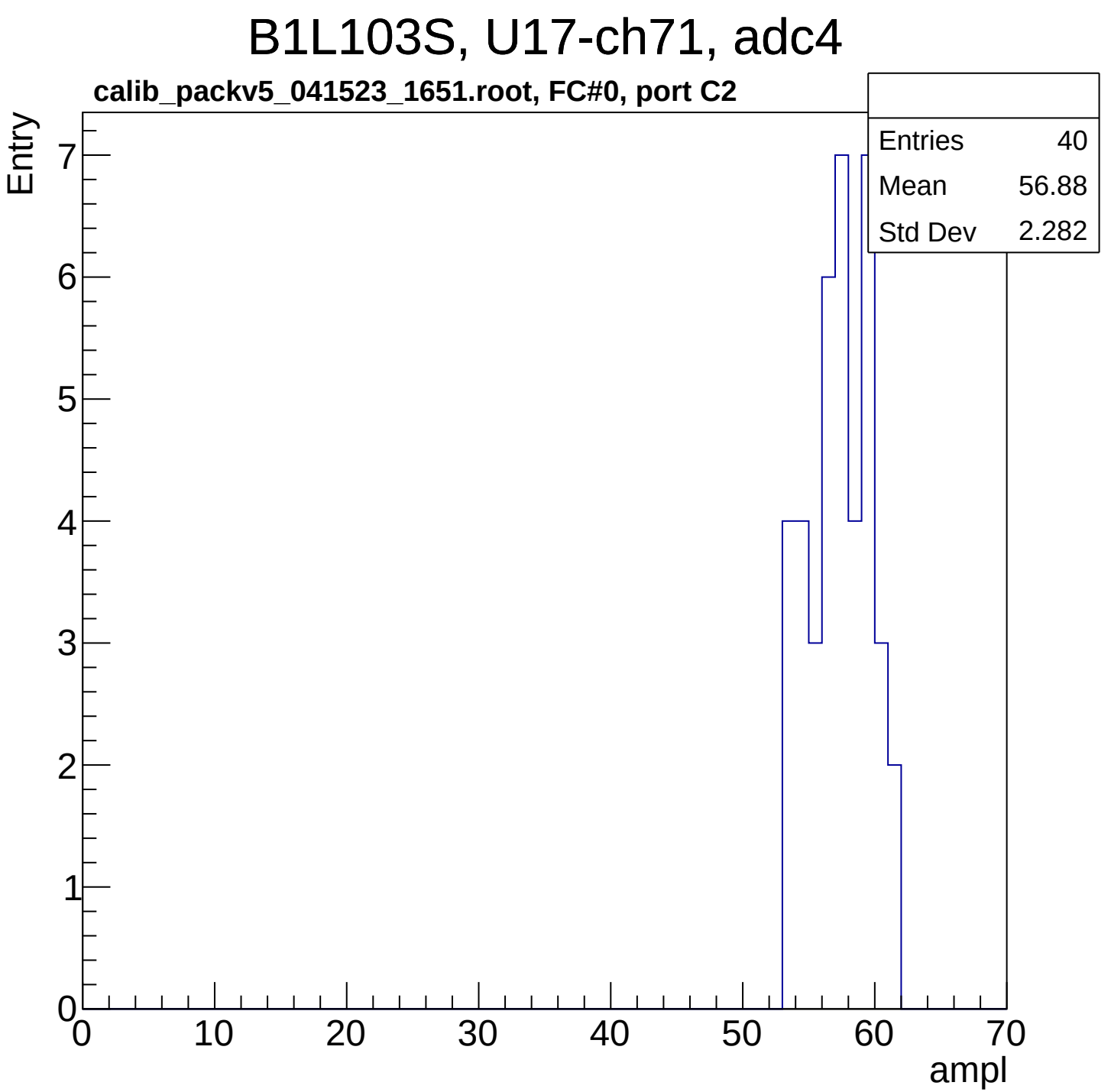

B1L103S, U17-ch70, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

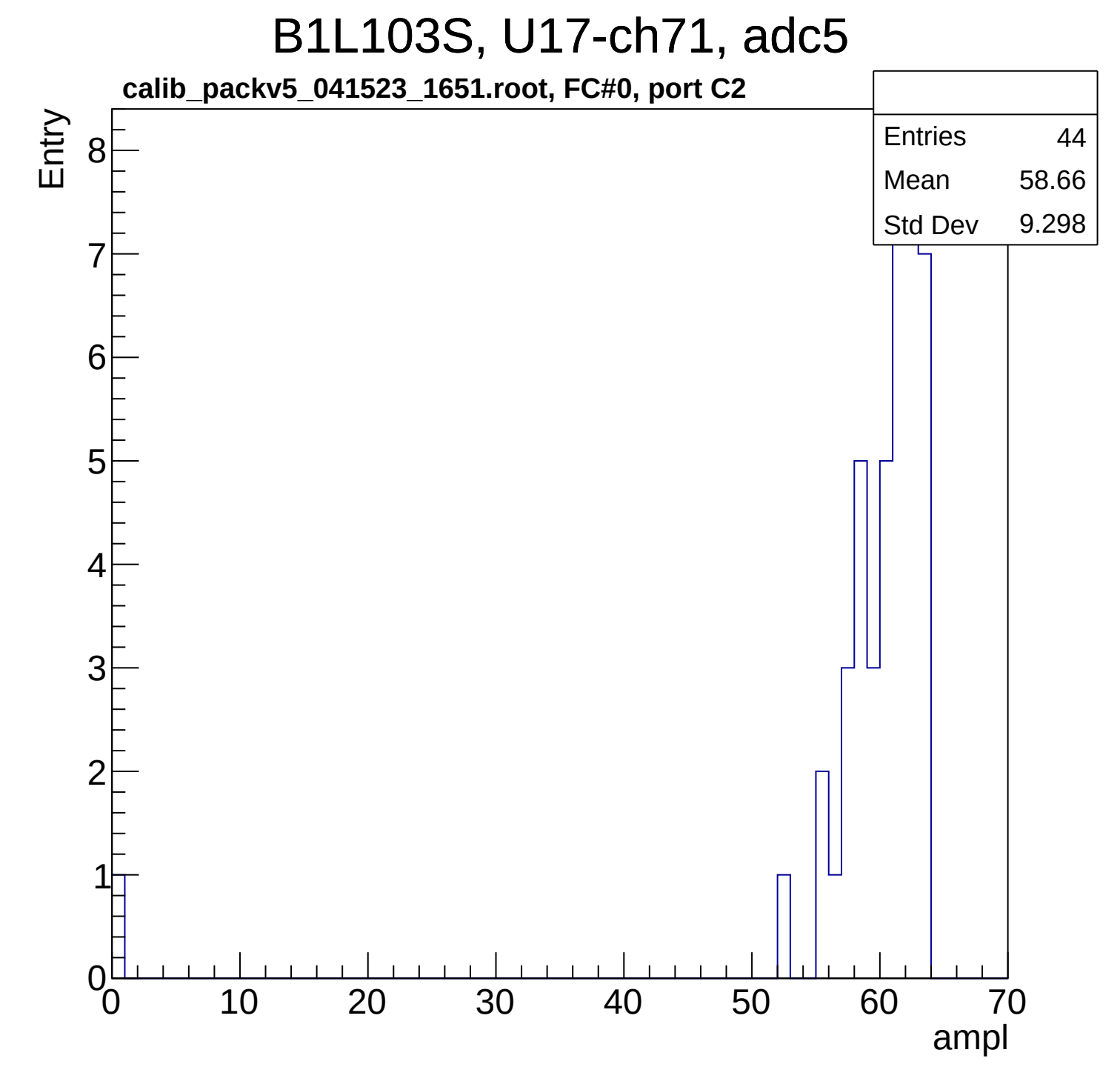

B1L103S, U17-ch71, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 22.16
Std Dev 13.82
Gaus mean : 30.7434
Gaus Width: 3.5197
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70

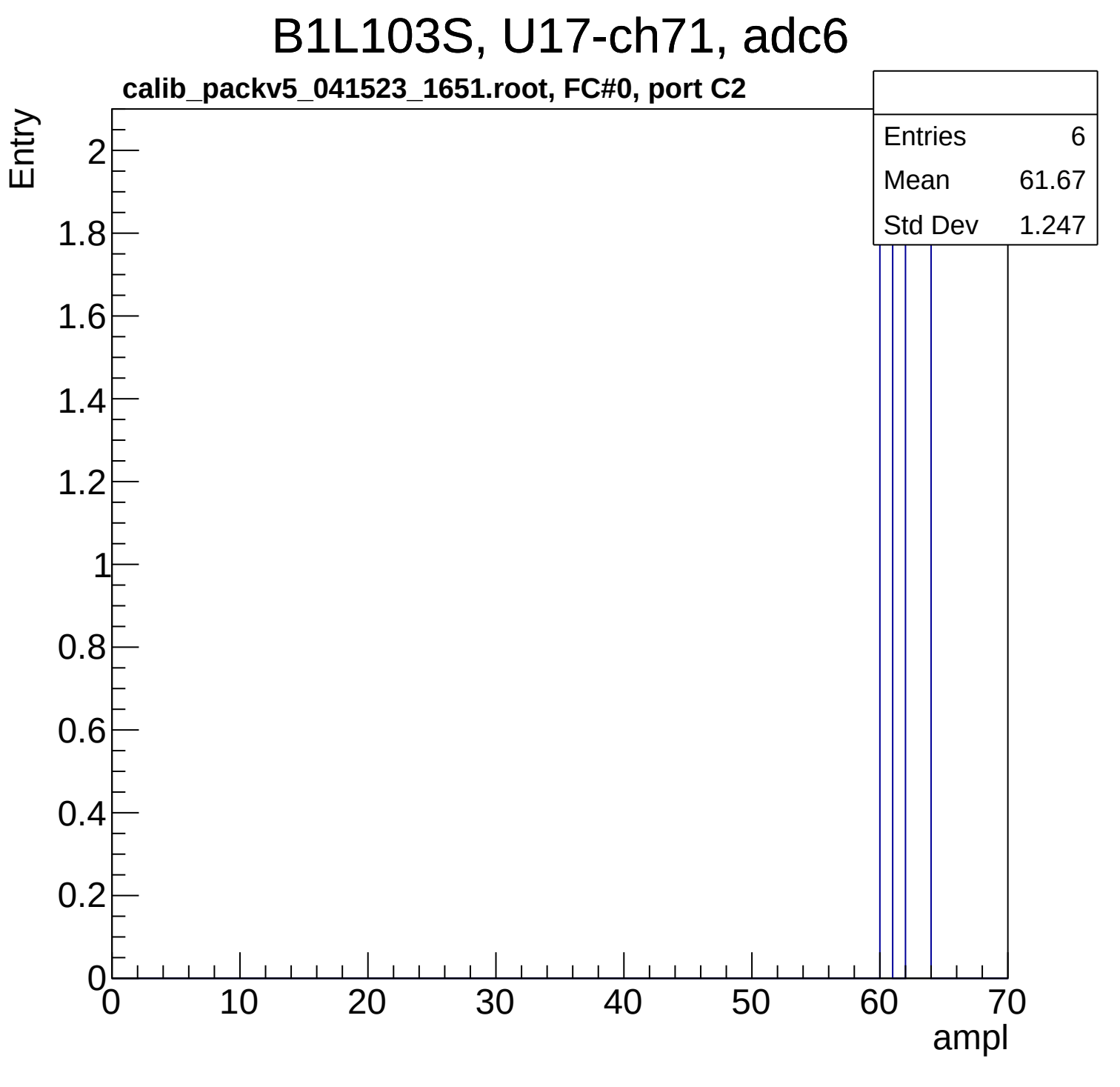

B1L103S, U17-ch71, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 35
Std Dev 8.422
Gaus mean : 36.2587
Gaus Width: 4.0804
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

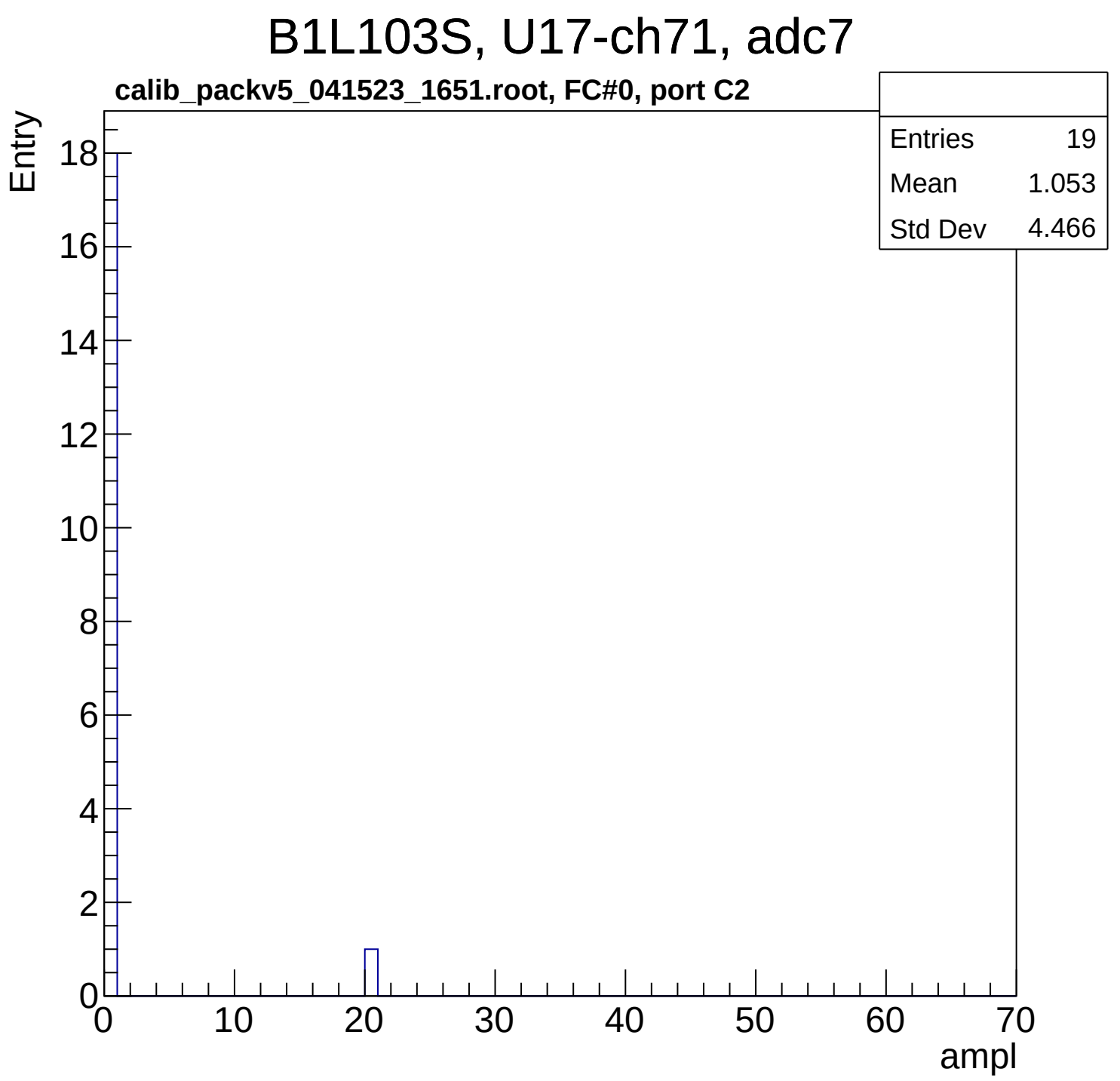

B1L103S, U17-ch71, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 37.26
Std Dev 14.31
Gaus mean : 44.3091
Gaus Width: 4.4876
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

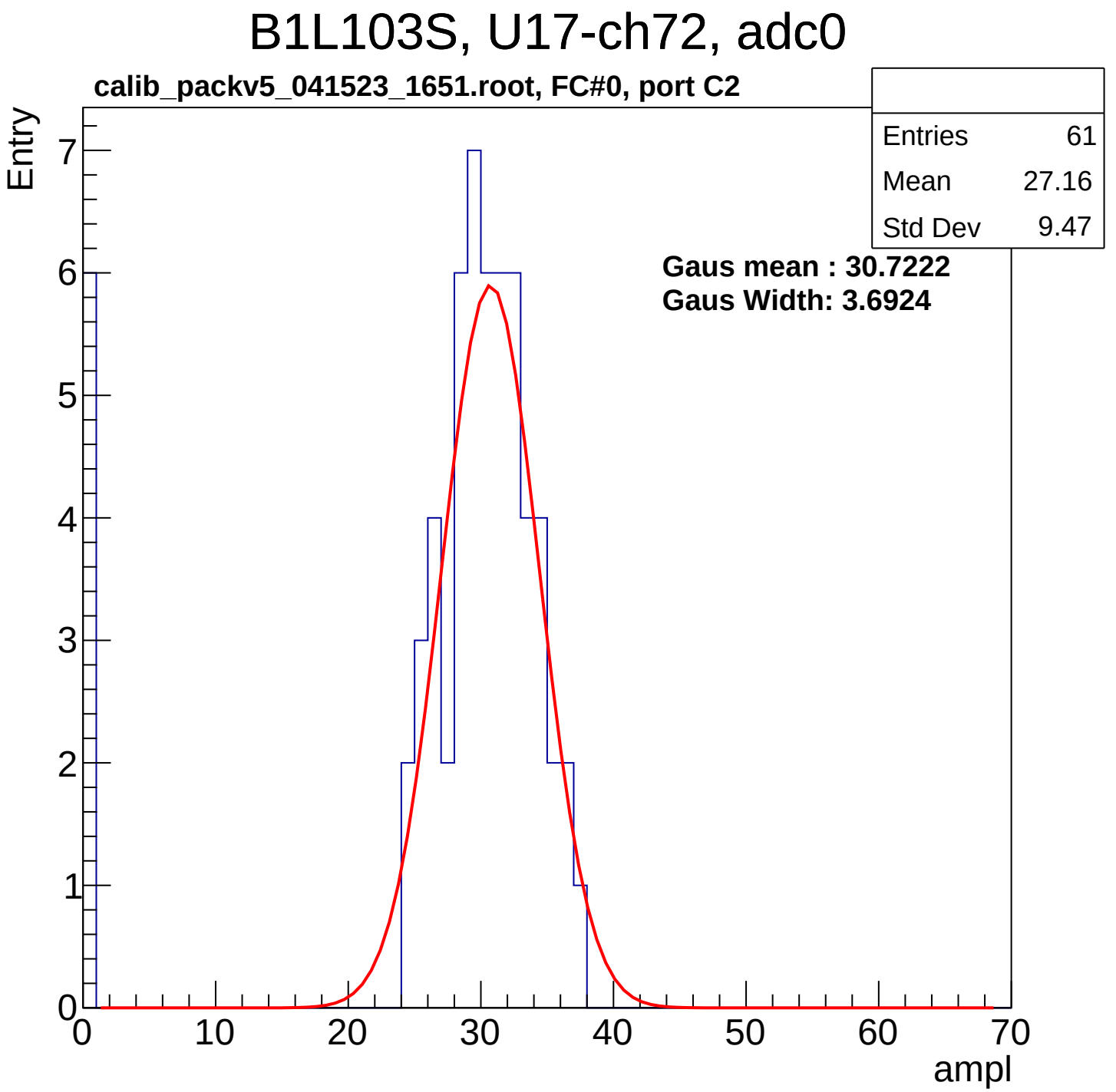

B1L103S, U17-ch71, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 46.91
Std Dev 12.86
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

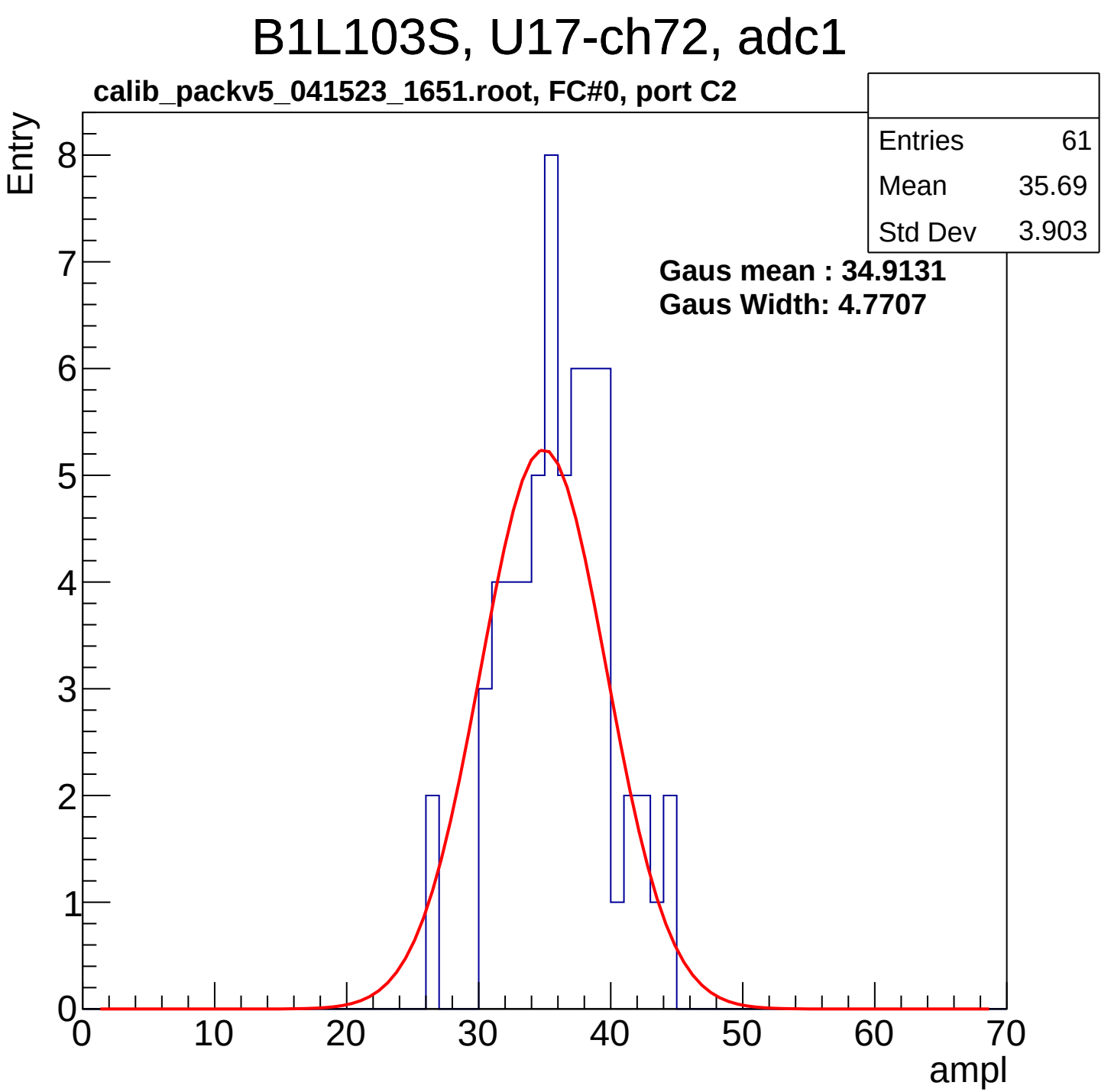

B1L103S, U17-ch71, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 56.88
Std Dev 2.282
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

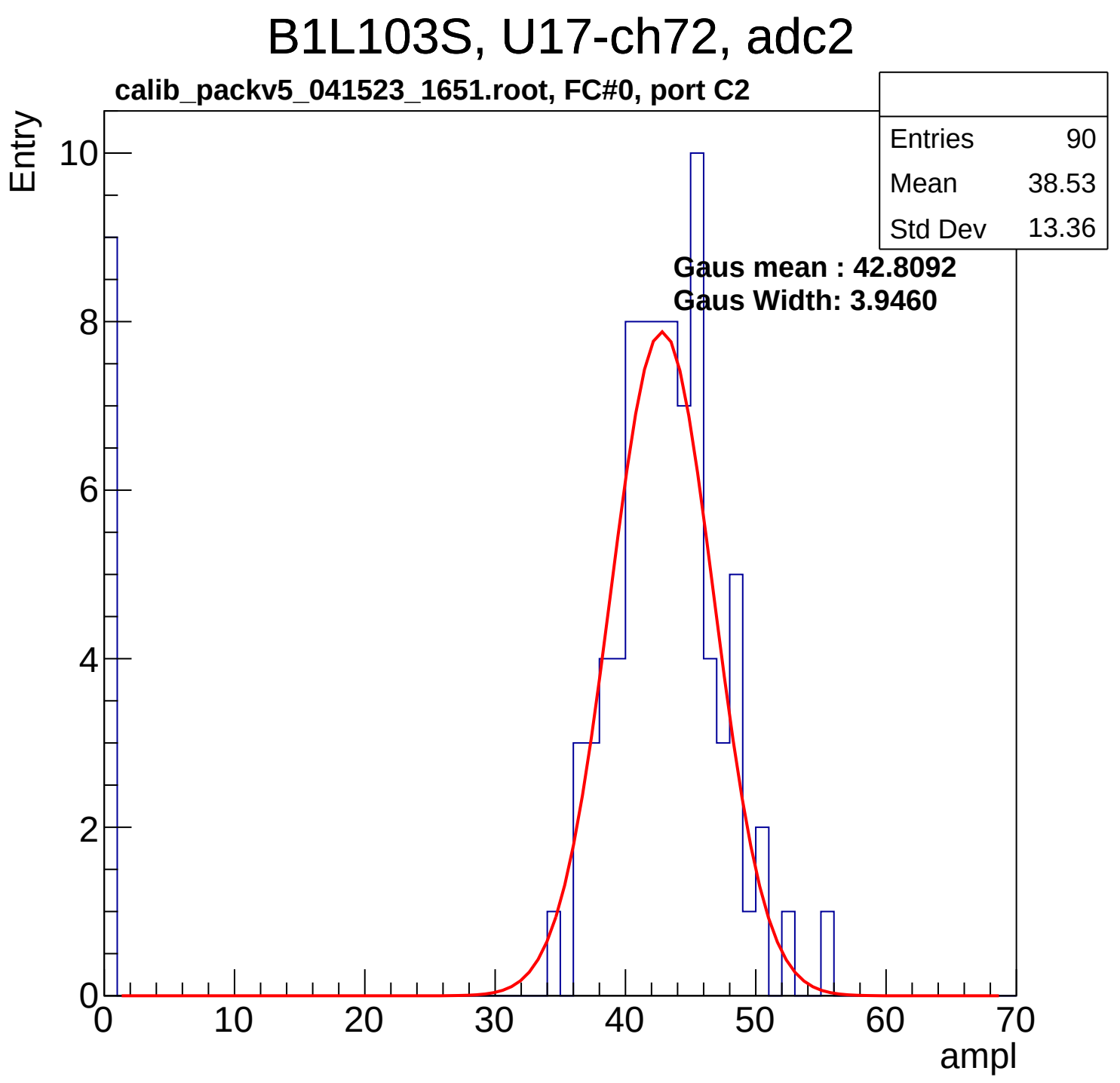

B1L103S, U17-ch71, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 58.66
Std Dev 9.298
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

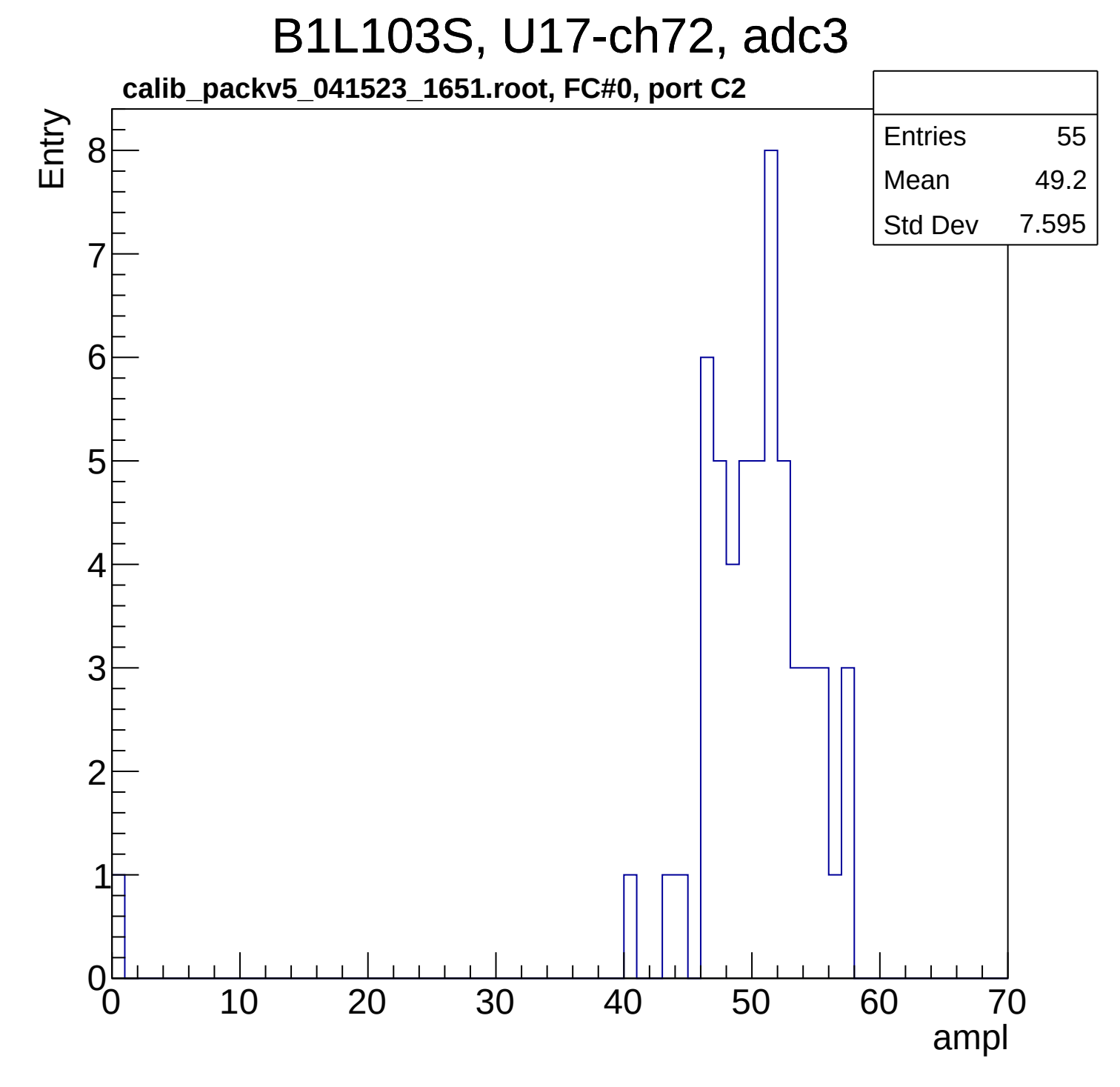

B1L103S, U17-ch71, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.67
Std Dev 1.247
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

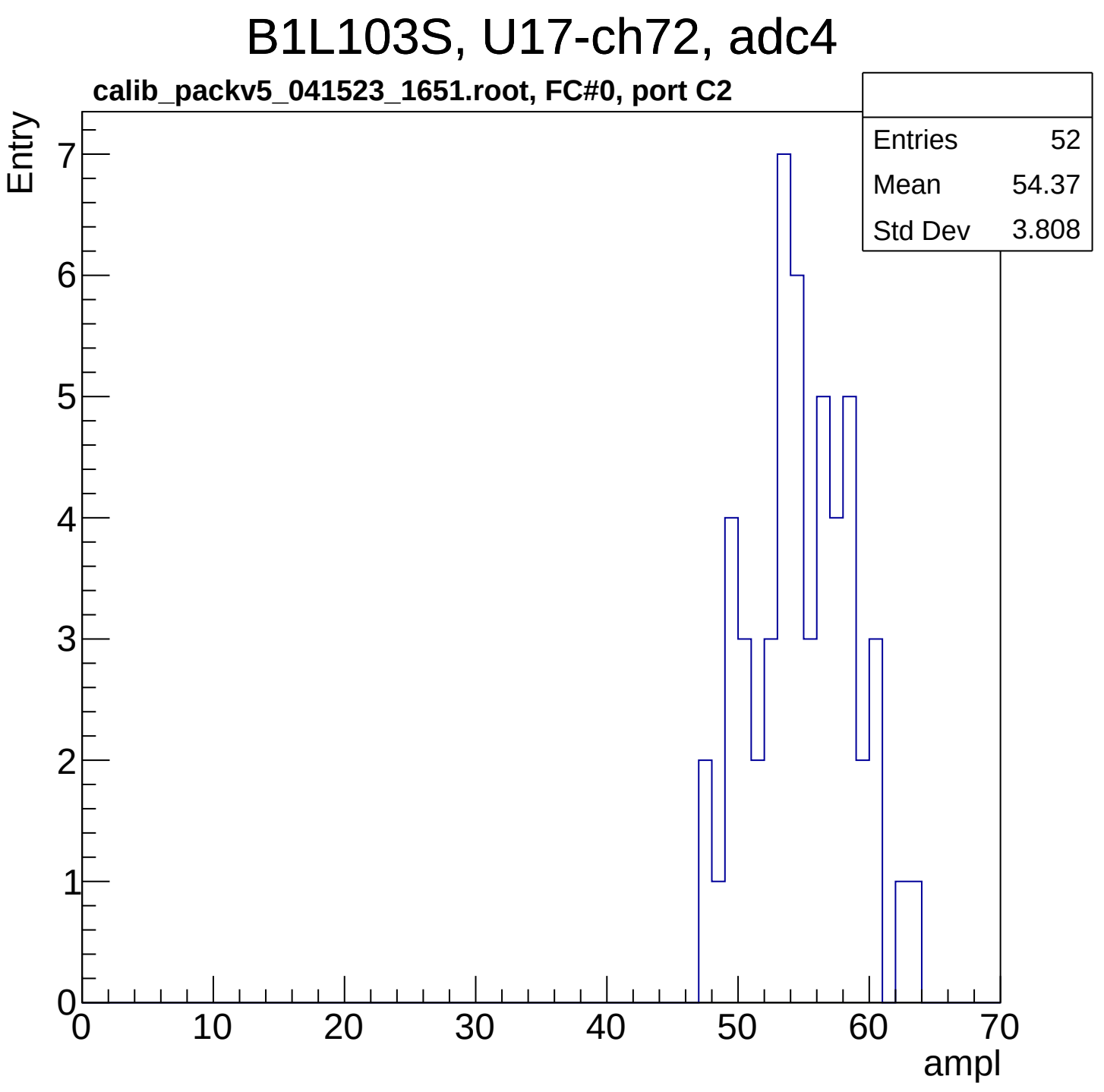

B1L103S, U17-ch71, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.053
Std Dev 4.466
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

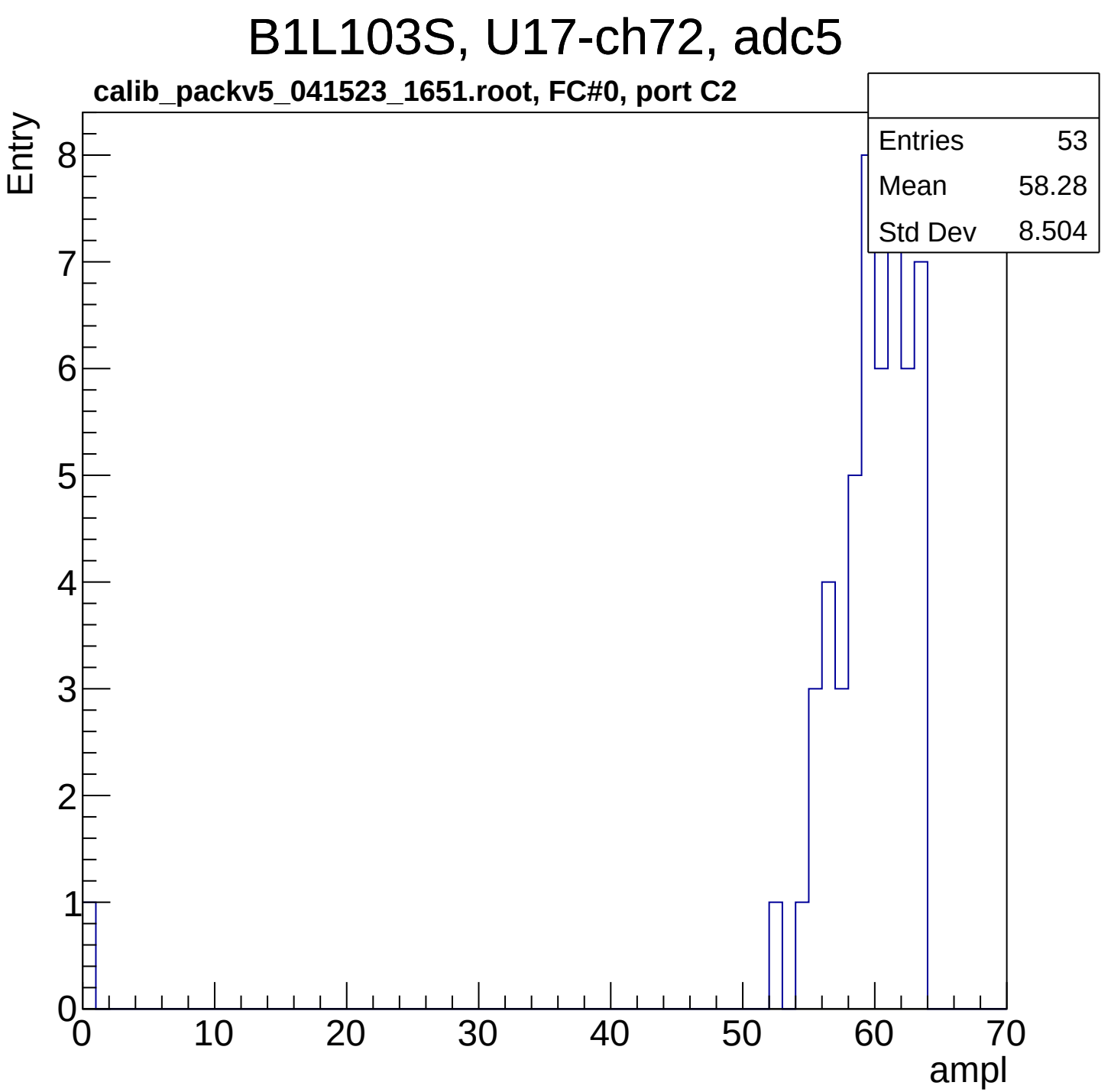

B1L103S, U17-ch72, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 27.16
Std Dev 9.47
Gaus mean : 30.7222
Gaus Width: 3.6924
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

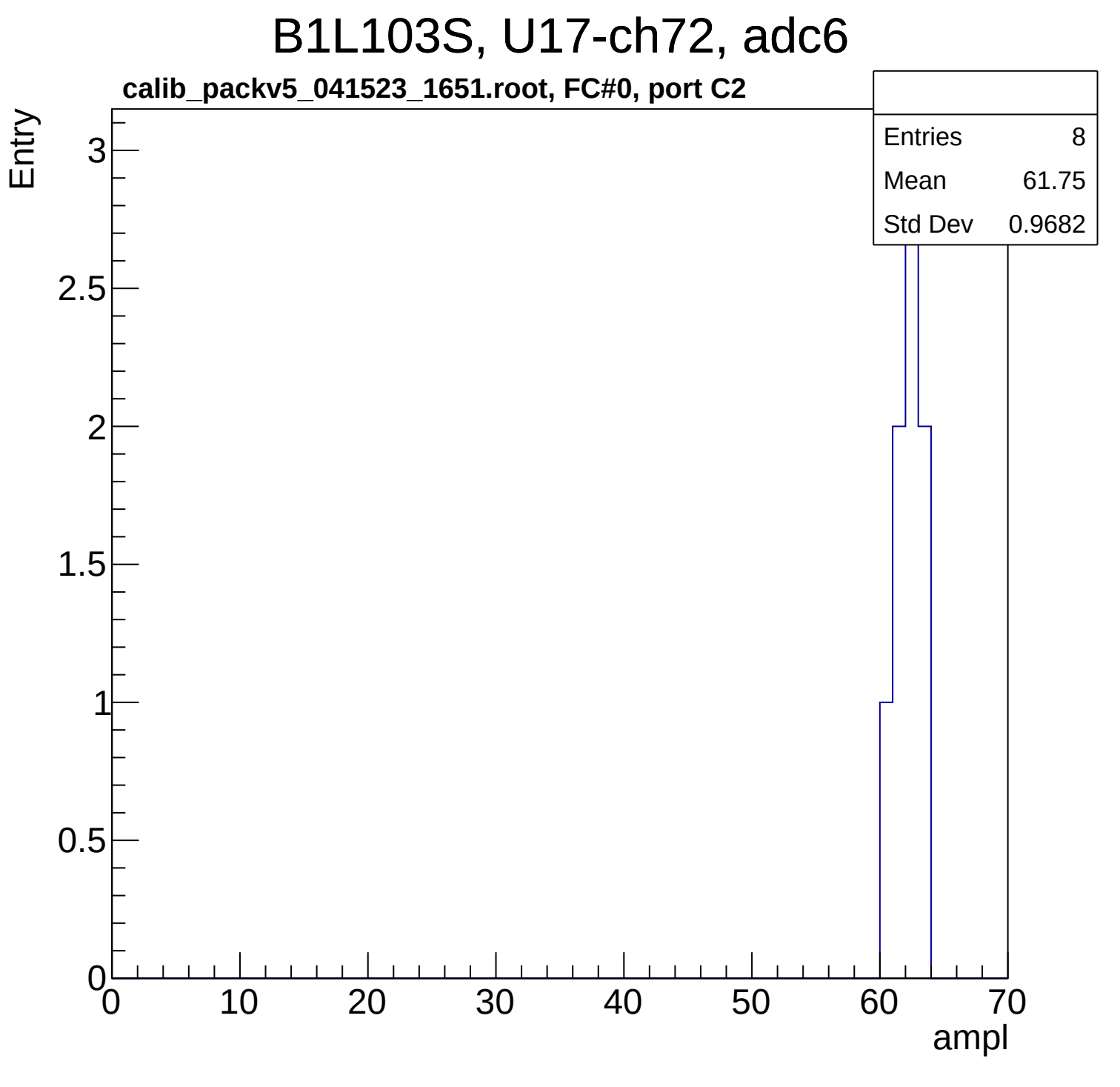

B1L103S, U17-ch72, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 35.69
Std Dev 3.903
Gaus mean : 34.9131
Gaus Width: 4.7707
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

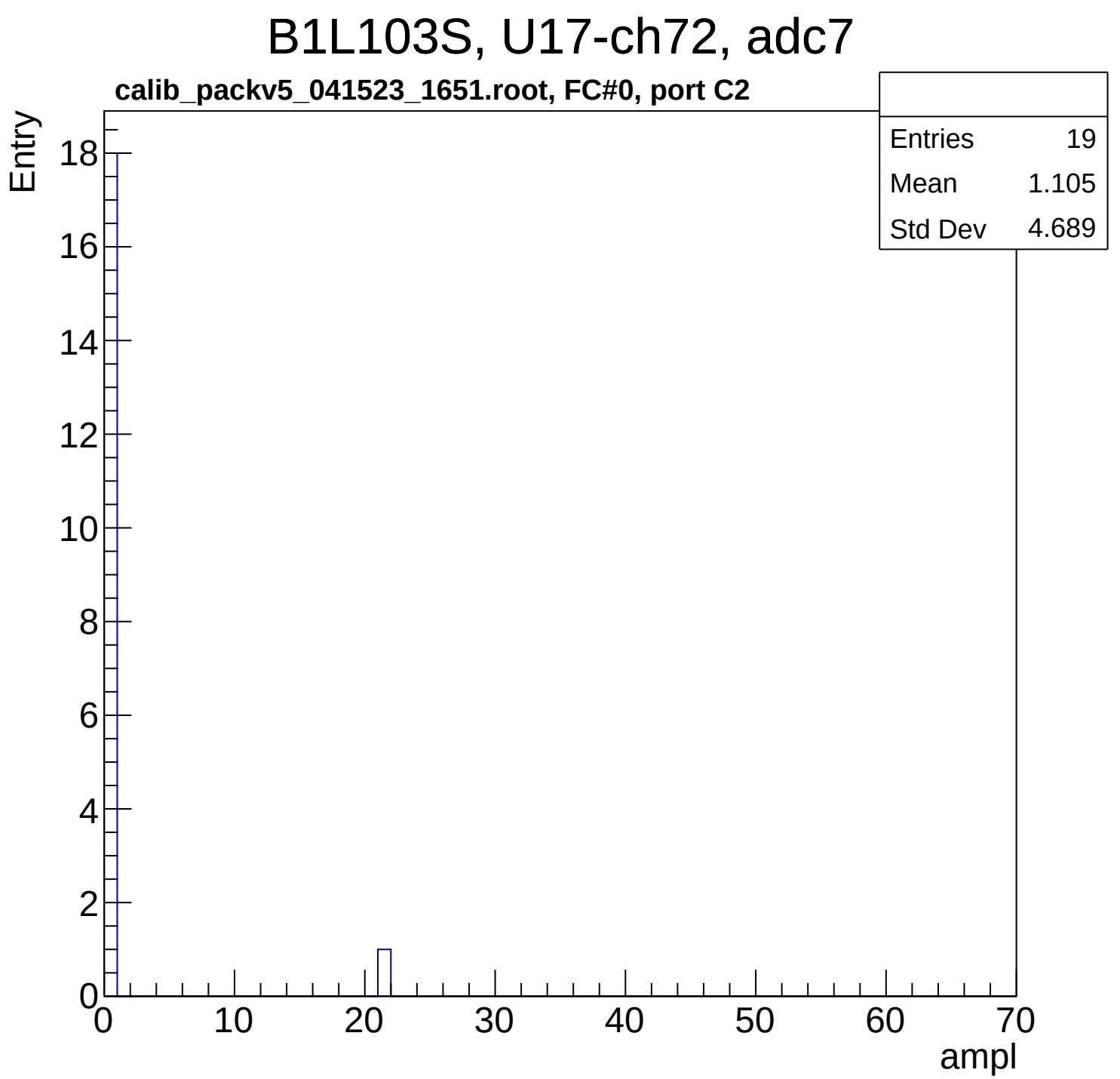

B1L103S, U17-ch72, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 38.53
Std Dev 13.36
Gaus mean : 42.8092
Gaus Width: 3.9460
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

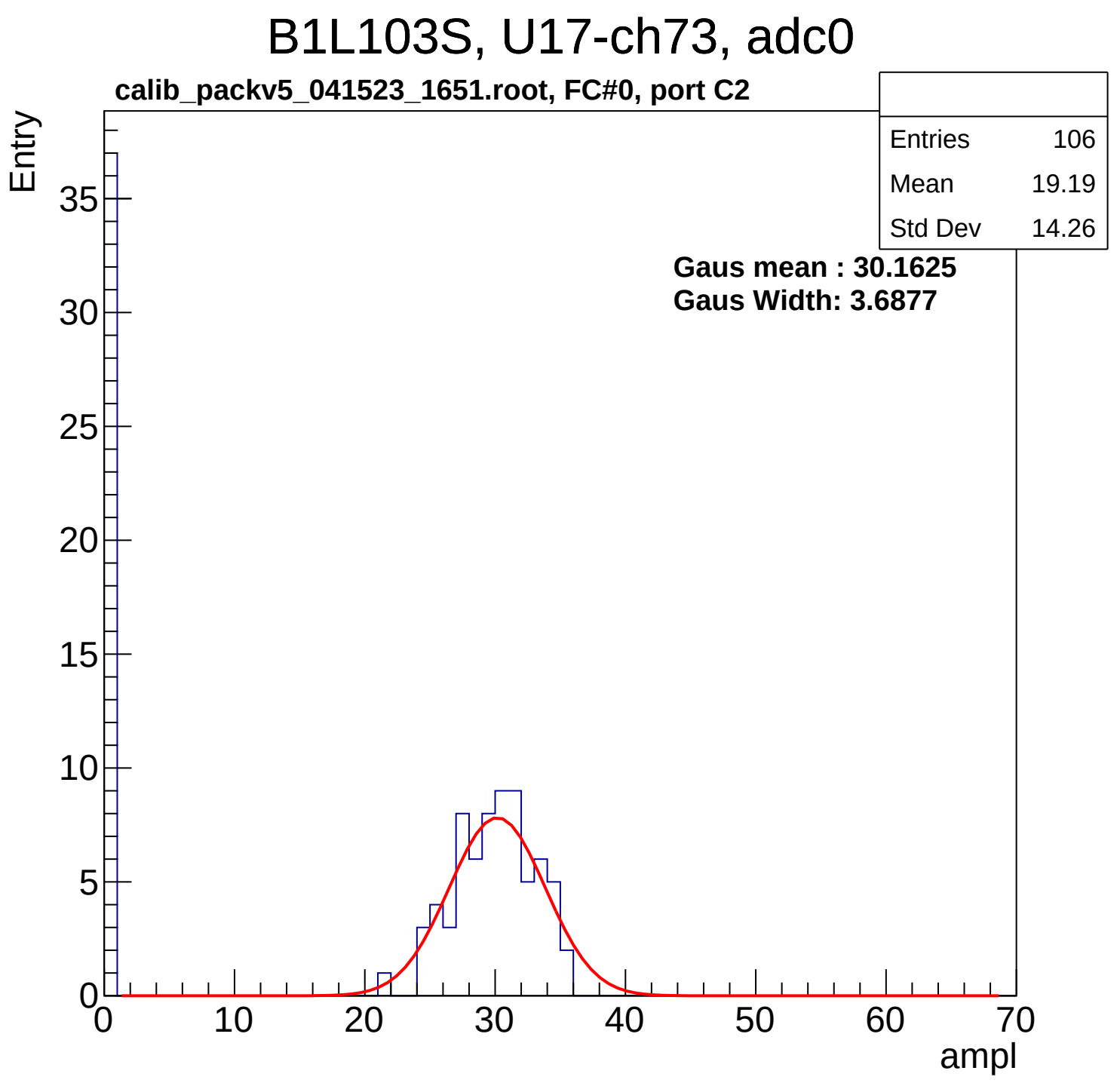

B1L103S, U17-ch72, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 49.2
Std Dev 7.595
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

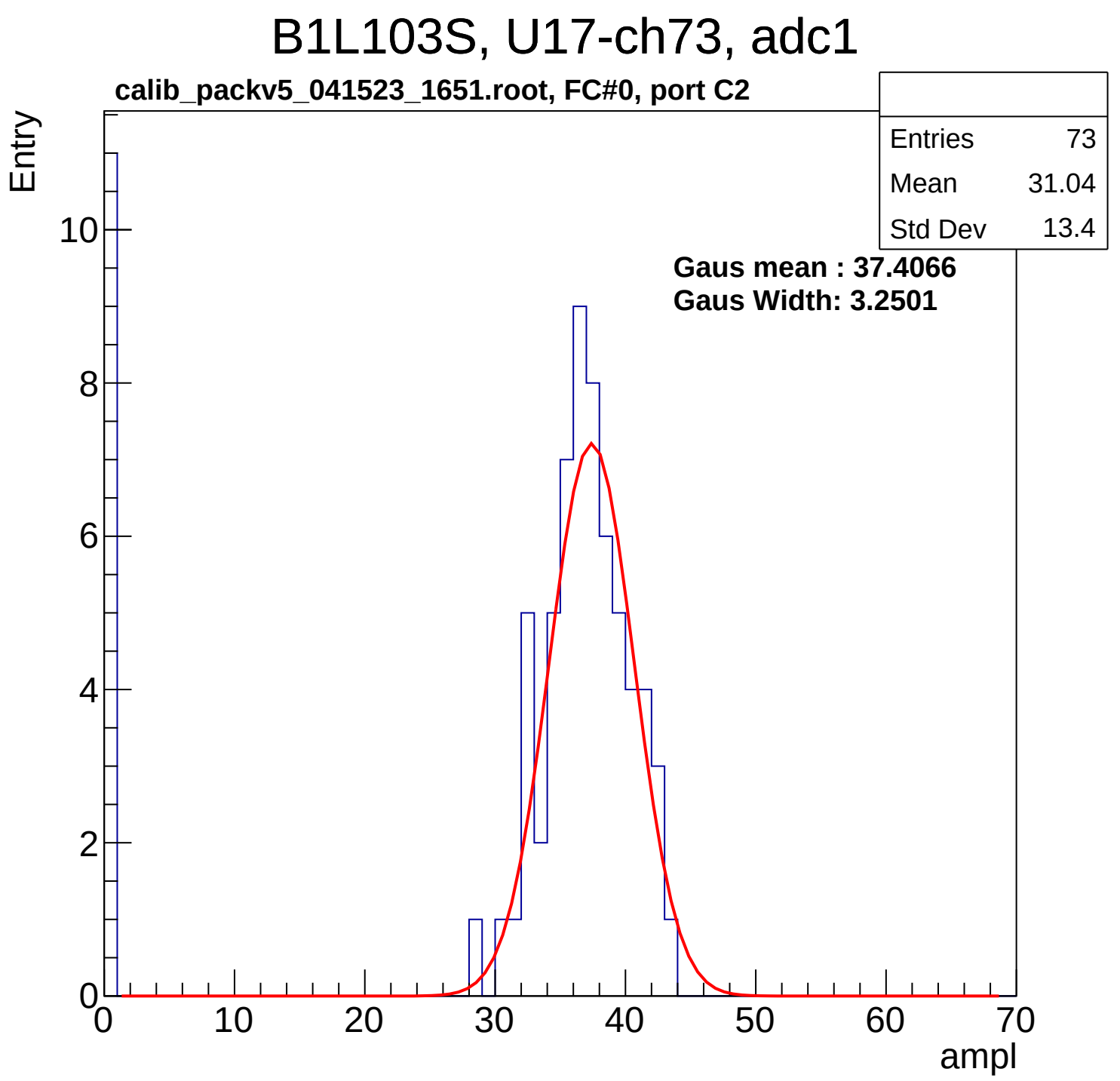

B1L103S, U17-ch72, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 54.37
Std Dev 3.808
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

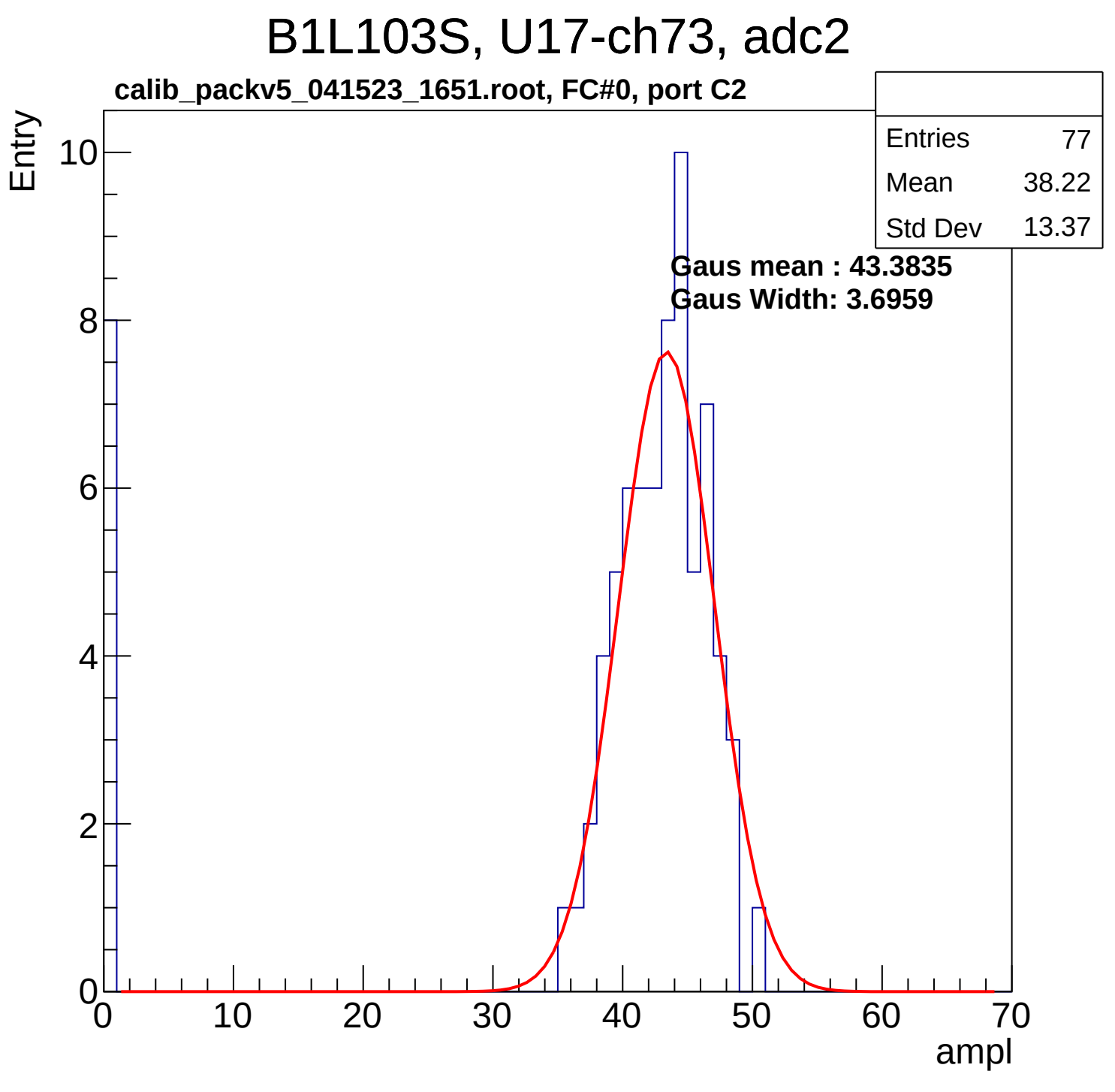

B1L103S, U17-ch72, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.28
Std Dev 8.504
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

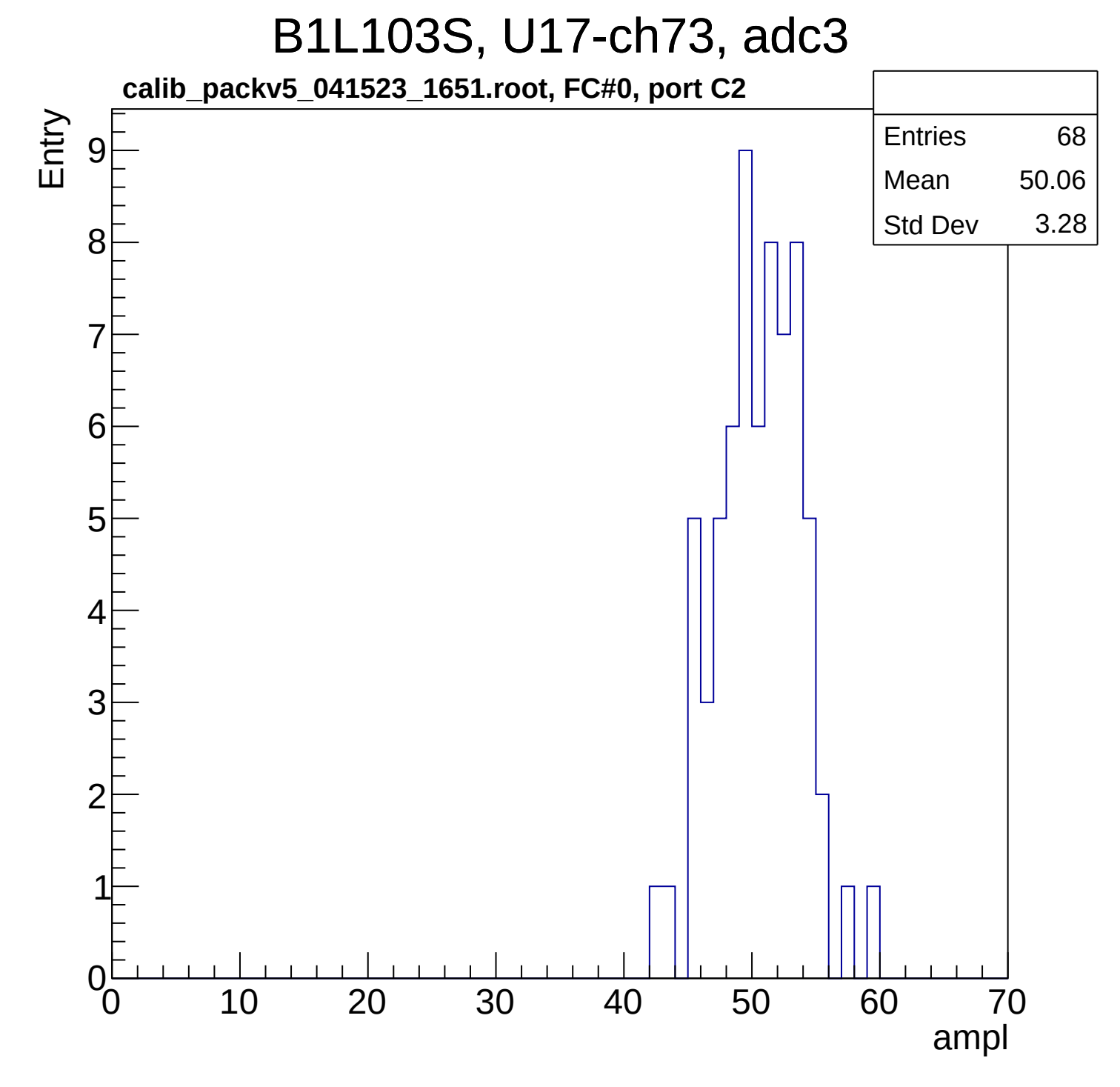

B1L103S, U17-ch72, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.75
Std Dev 0.9682
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

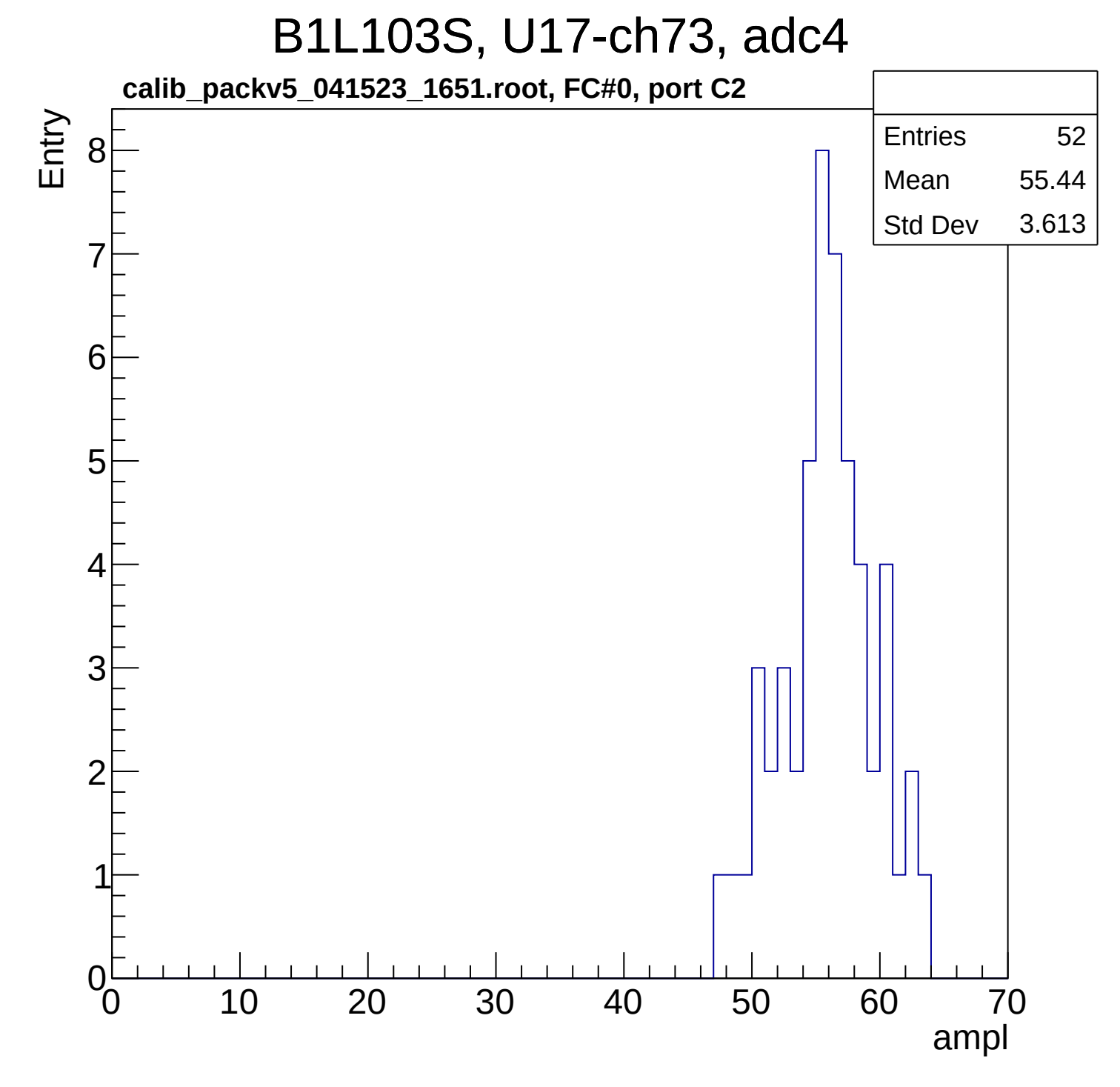

B1L103S, U17-ch72, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

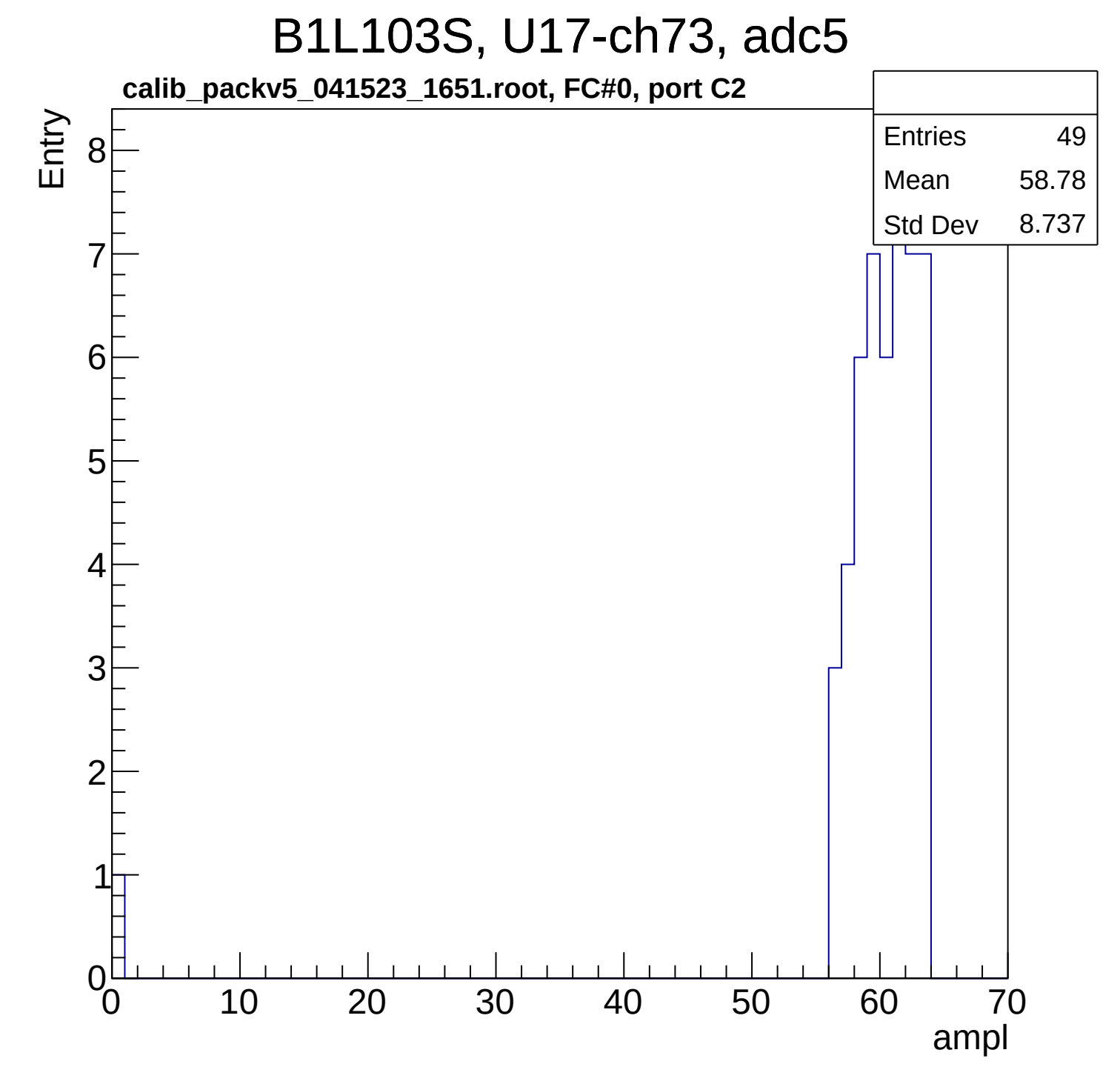

B1L103S, U17-ch73, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 106
Mean 19.19
Std Dev 14.26
Gaus mean : 30.1625
Gaus Width: 3.6877
Entry
ampl
0
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70

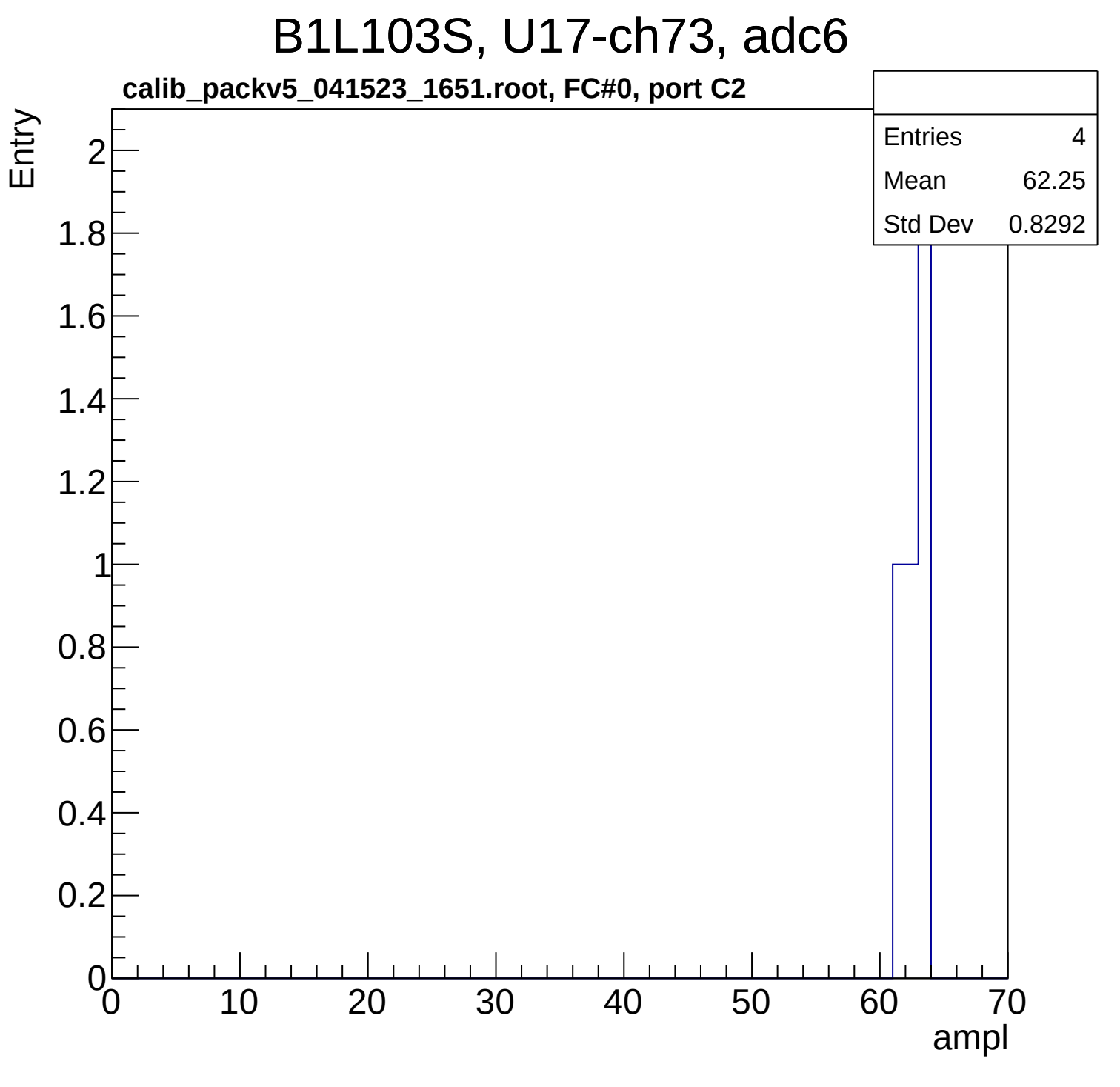

B1L103S, U17-ch73, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 31.04
Std Dev 13.4
Gaus mean : 37.4066
Gaus Width: 3.2501
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

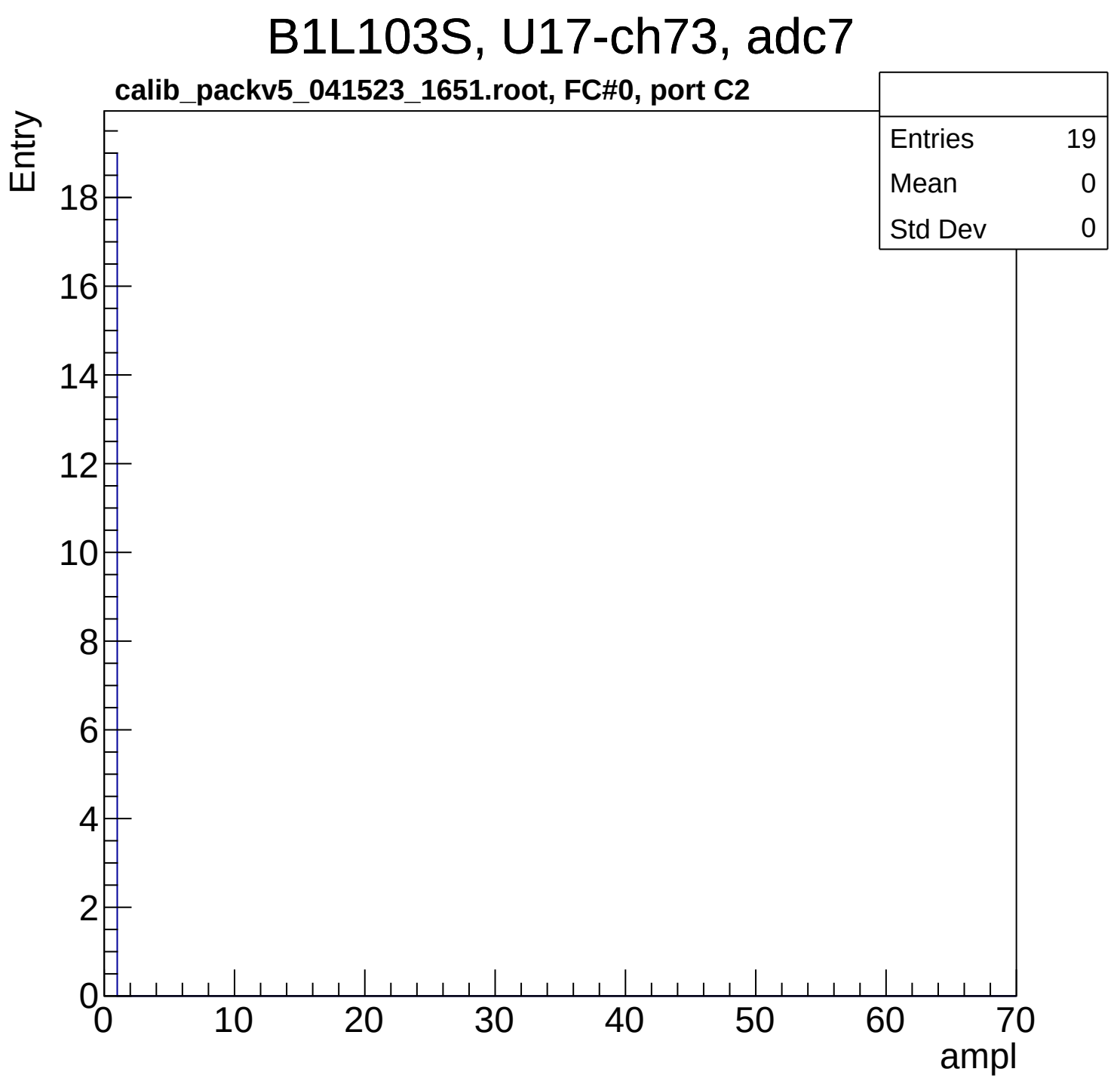

B1L103S, U17-ch73, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 38.22
Std Dev 13.37
Gaus mean : 43.3835
Gaus Width: 3.6959
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

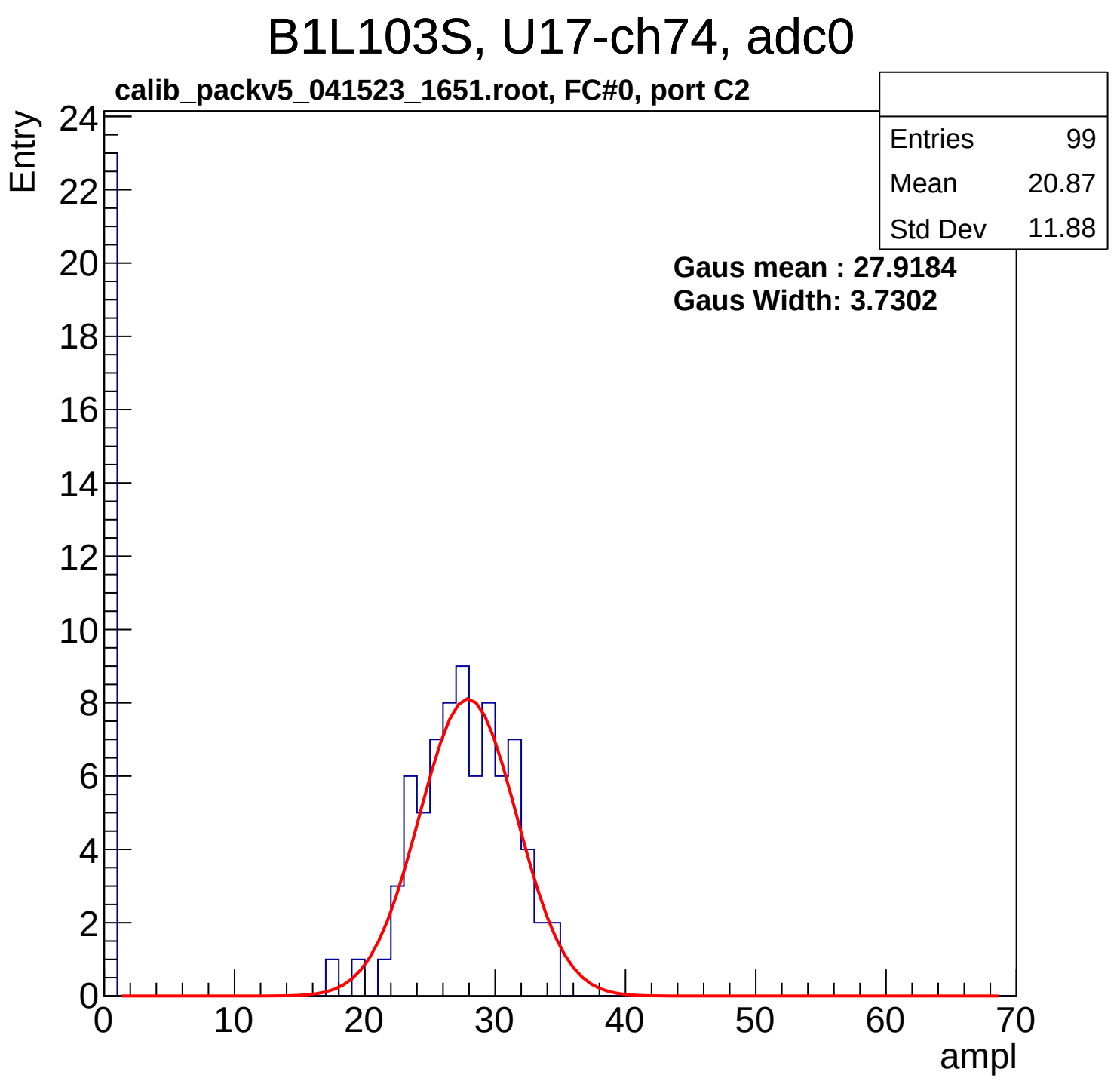

B1L103S, U17-ch73, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 50.06
Std Dev 3.28
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

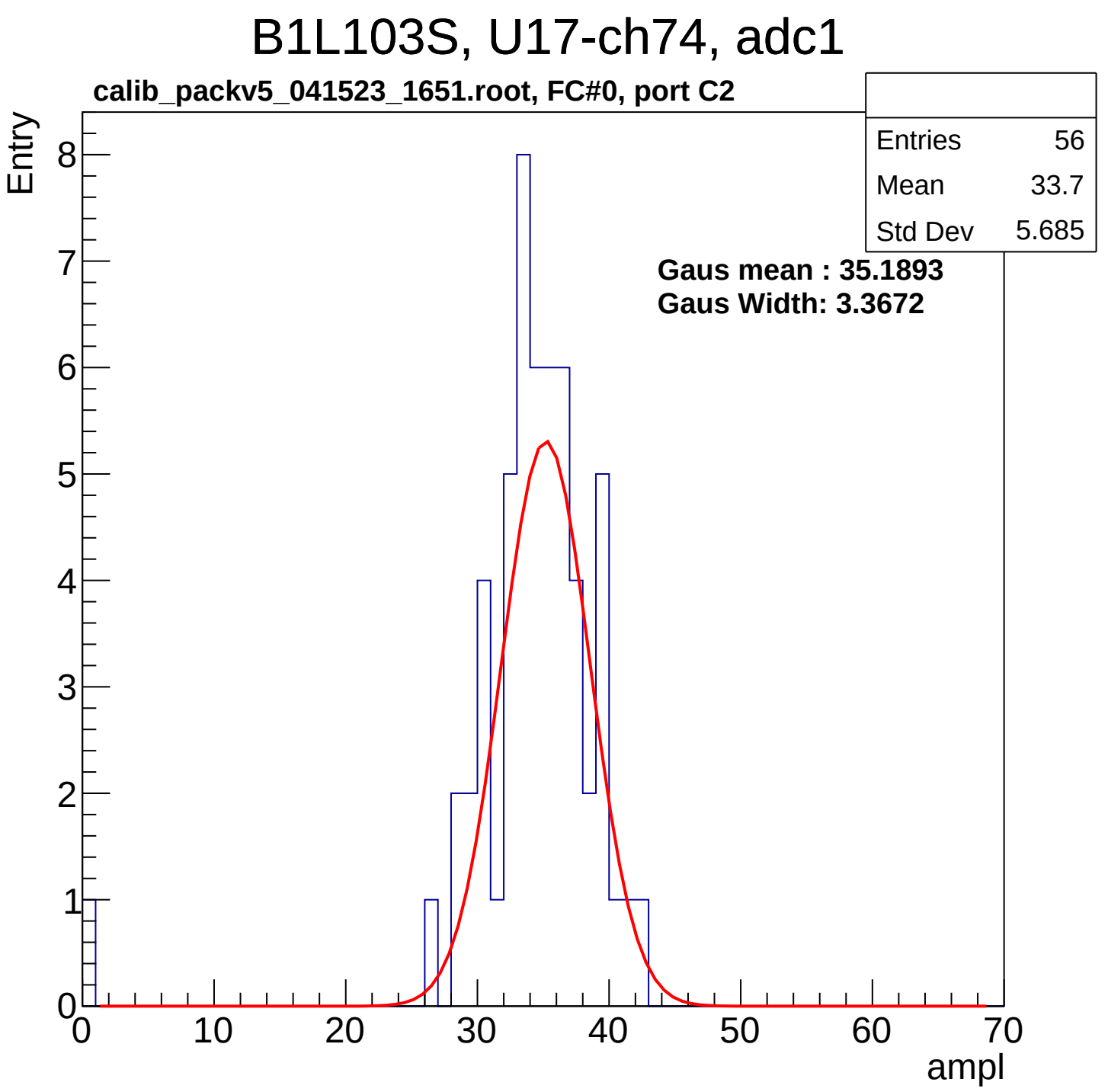

B1L103S, U17-ch73, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 55.44
Std Dev 3.613
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

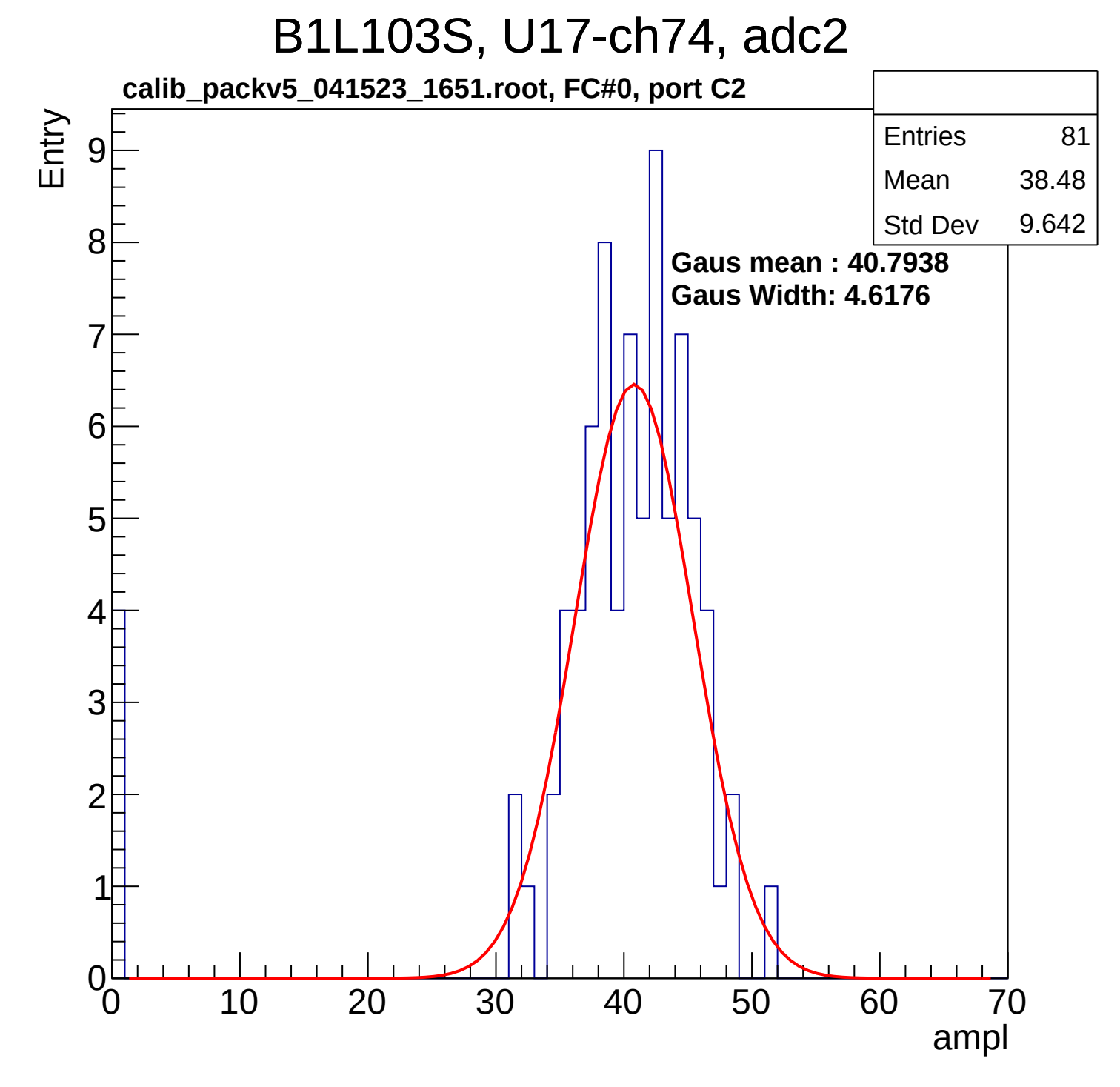

B1L103S, U17-ch73, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.78
Std Dev 8.737
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

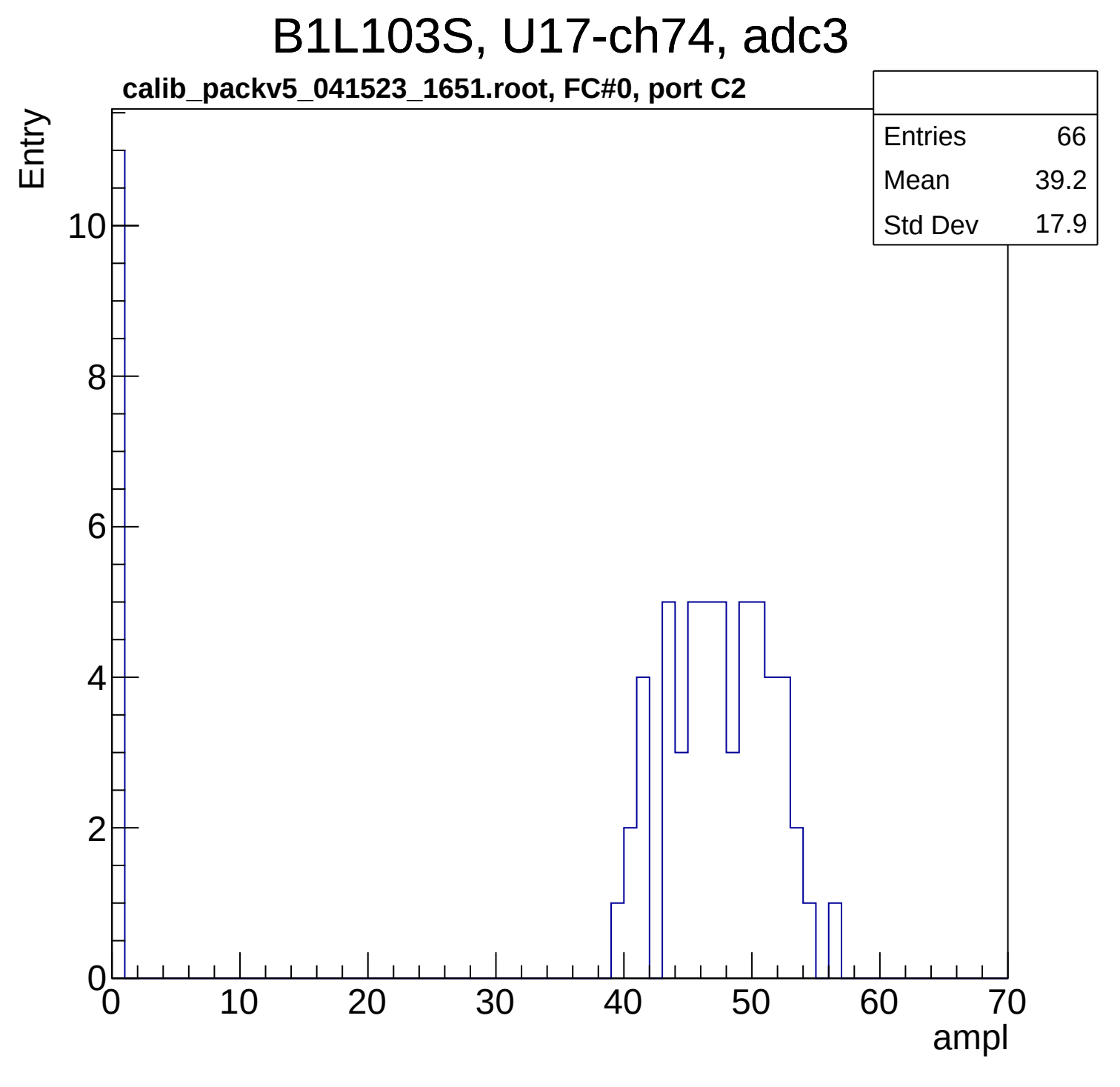

B1L103S, U17-ch73, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

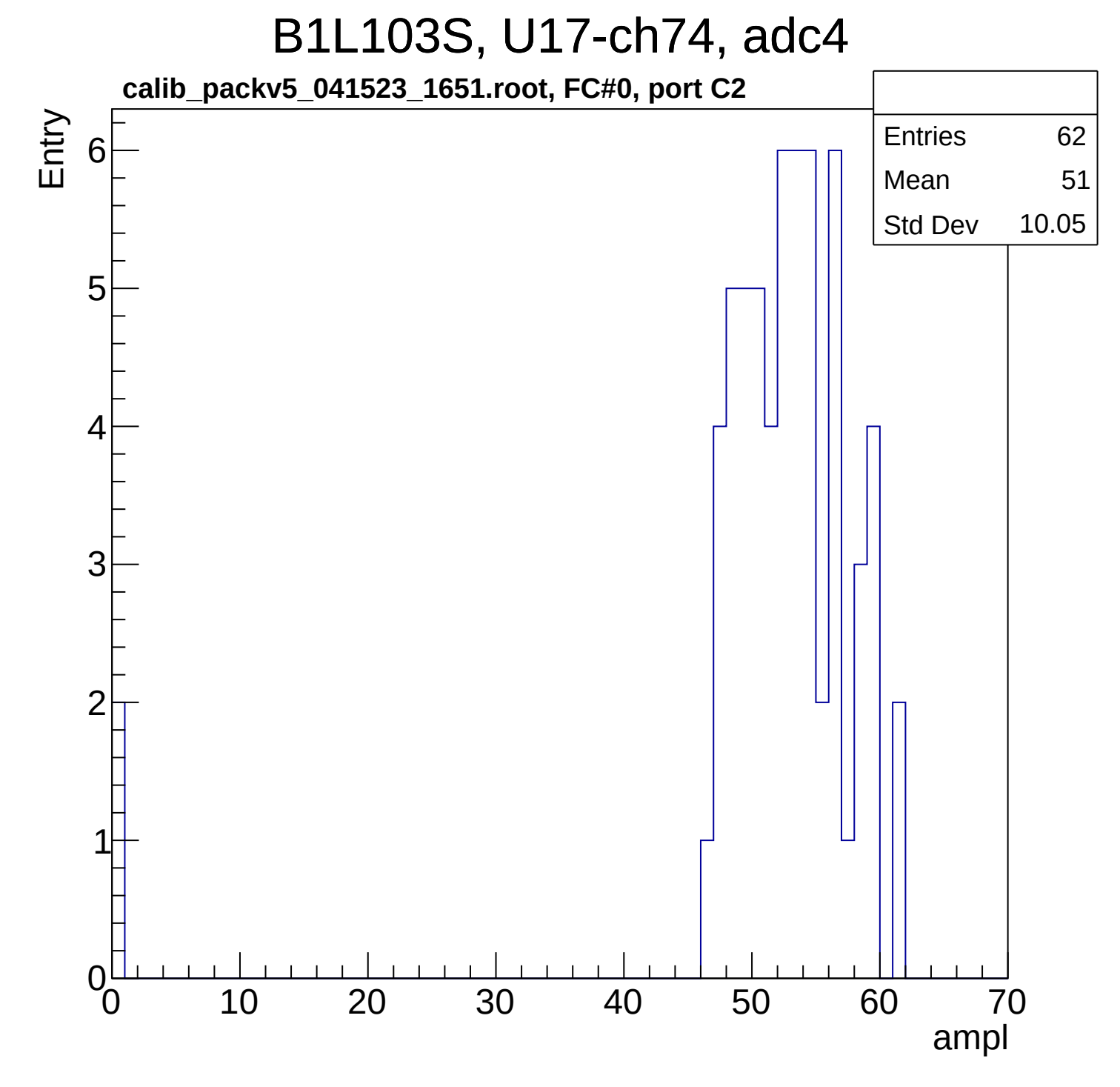

B1L103S, U17-ch73, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

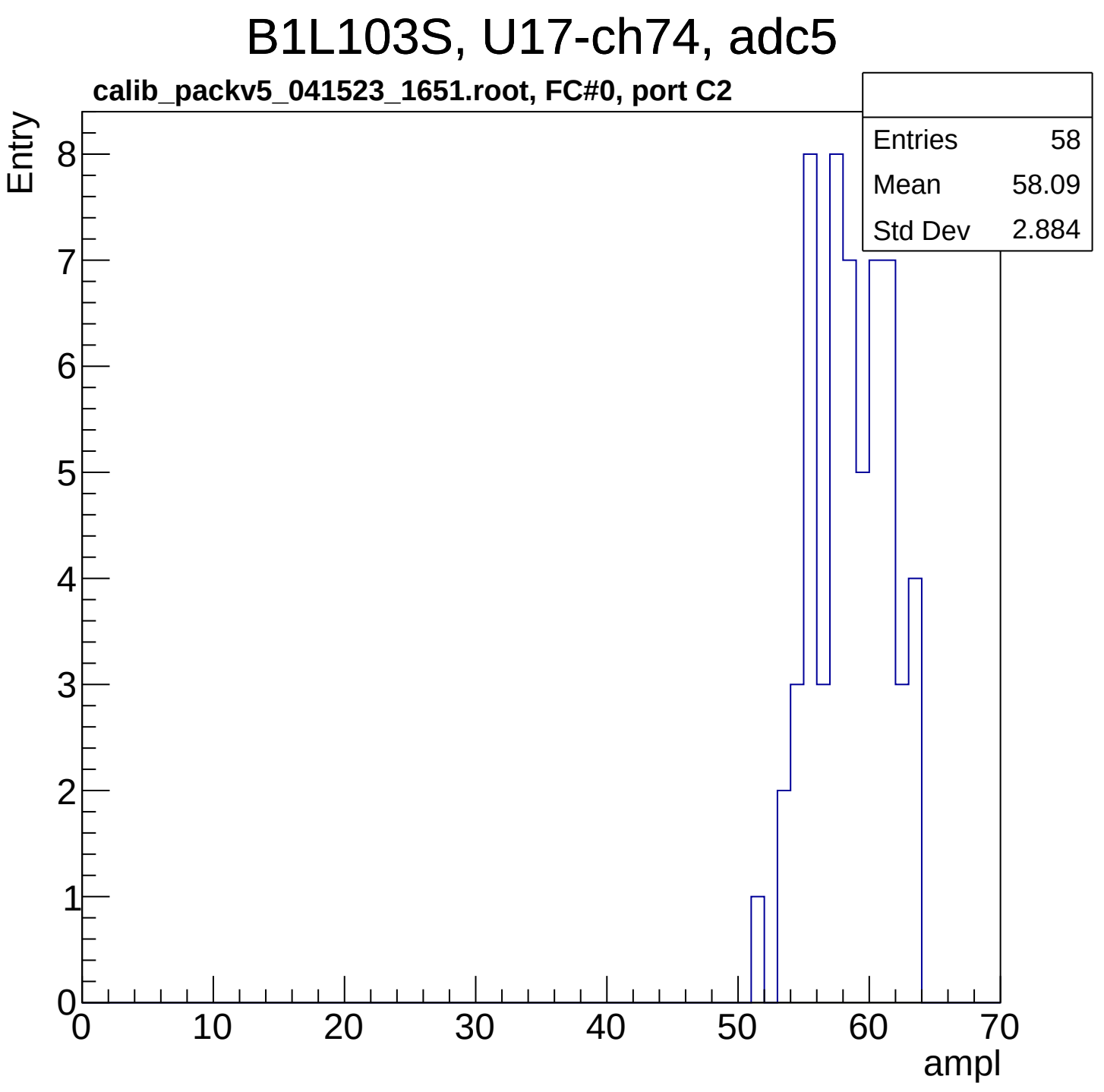

B1L103S, U17-ch74, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 20.87
Std Dev 11.88
Gaus mean : 27.9184
Gaus Width: 3.7302
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70

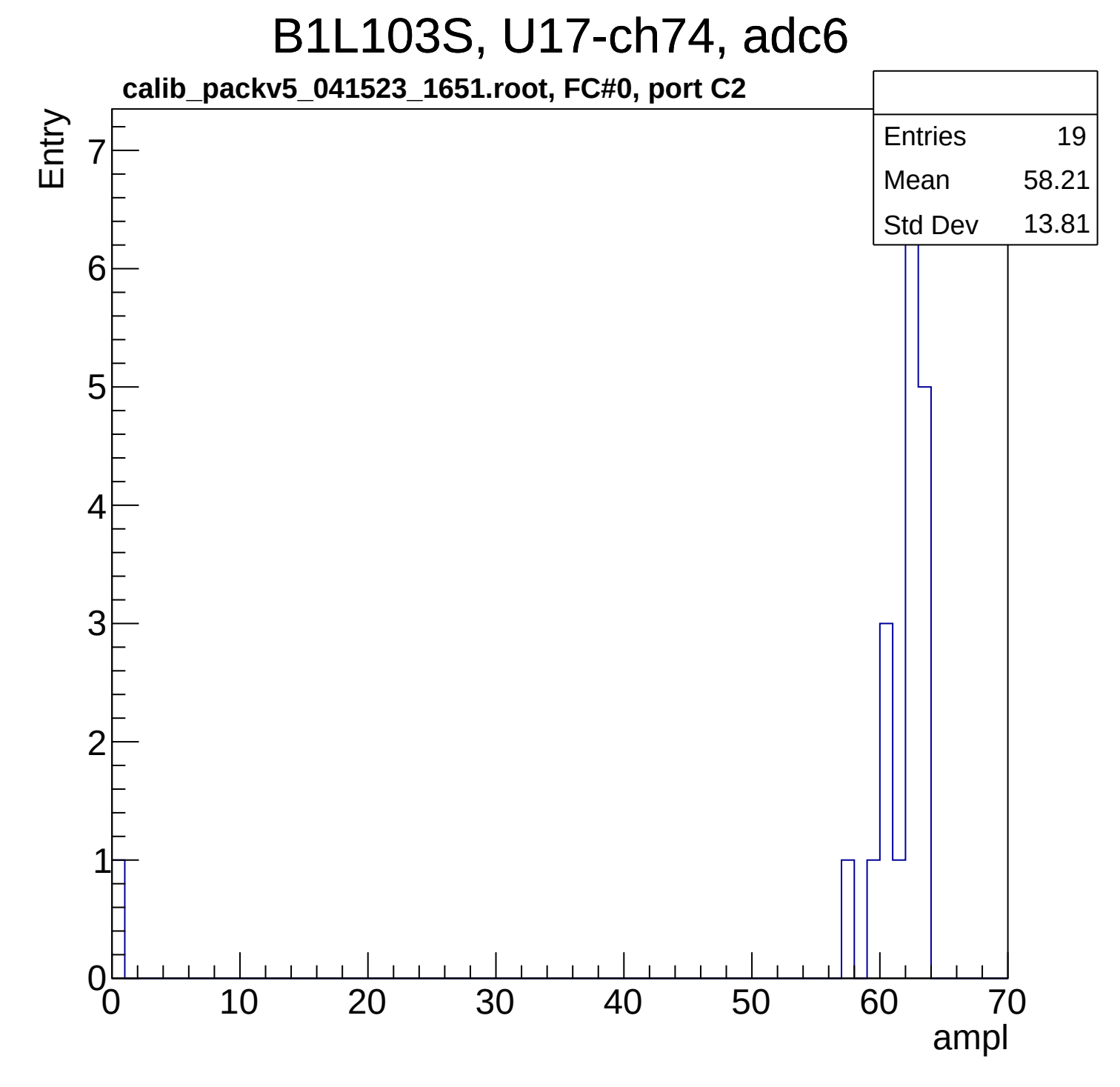

B1L103S, U17-ch74, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 33.7
Std Dev 5.685
Gaus mean : 35.1893
Gaus Width: 3.3672
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

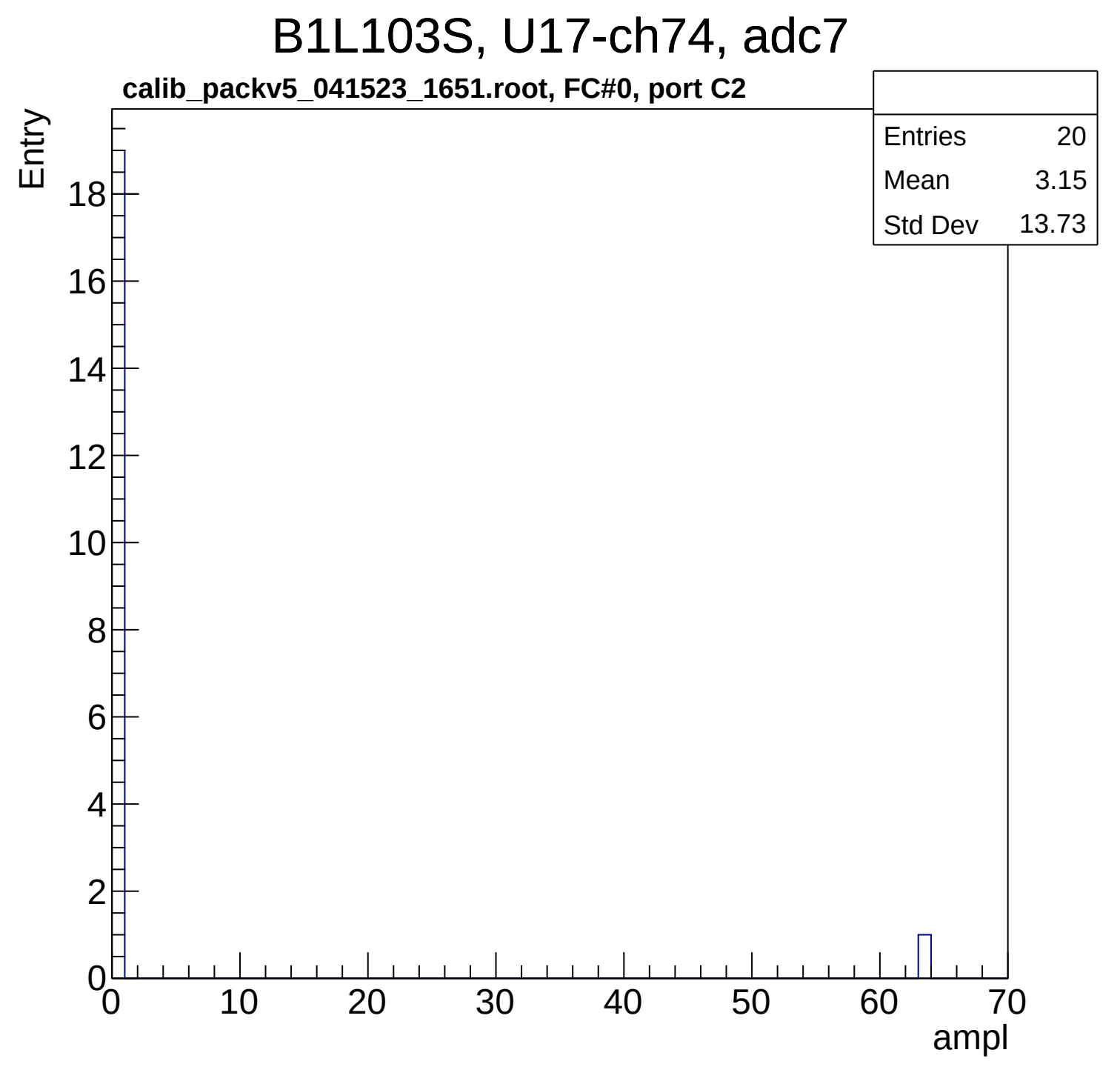

B1L103S, U17-ch74, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 38.48
Std Dev 9.642
Gaus mean : 40.7938
Gaus Width: 4.6176
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

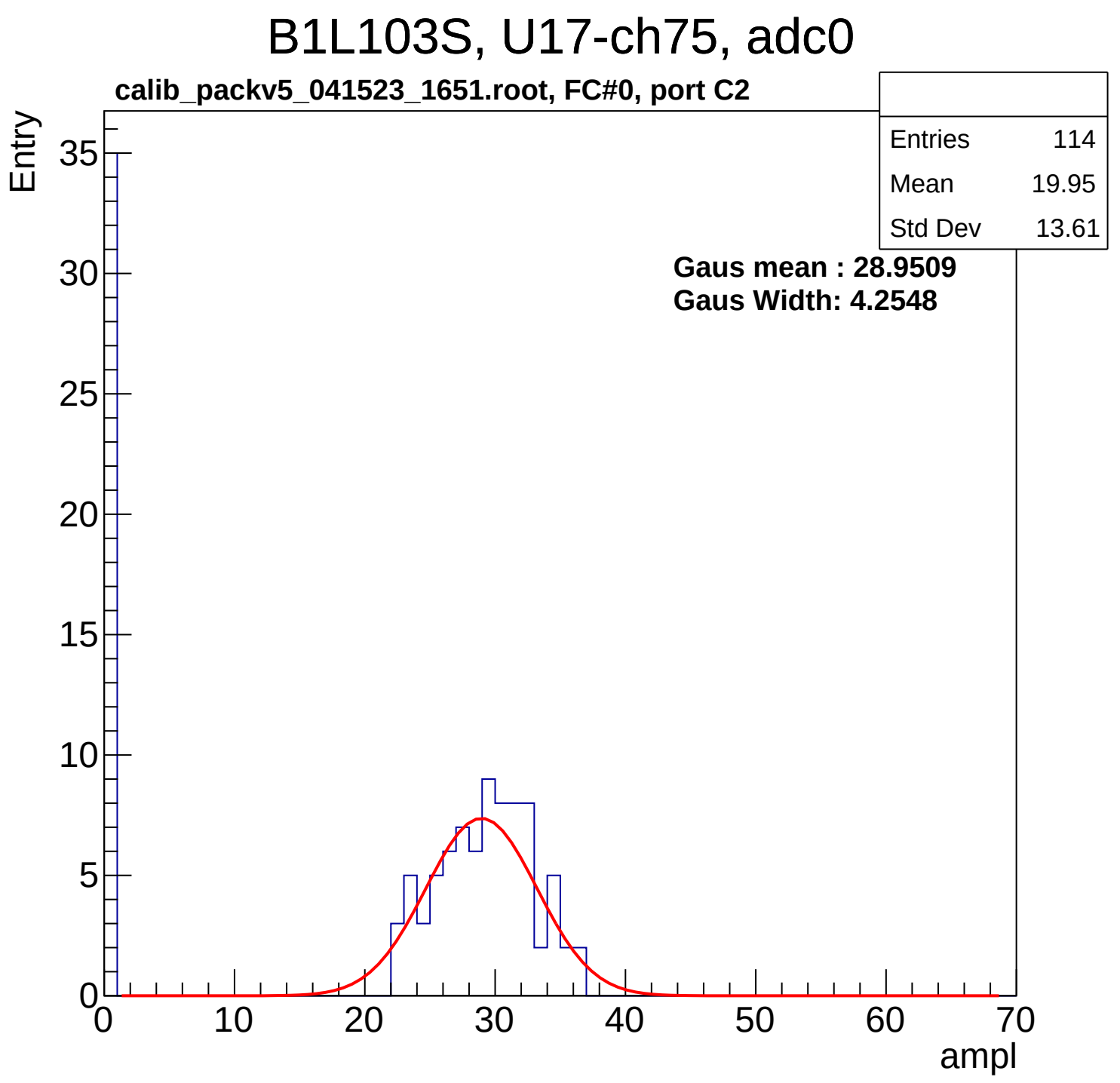

B1L103S, U17-ch74, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 39.2
Std Dev 17.9
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

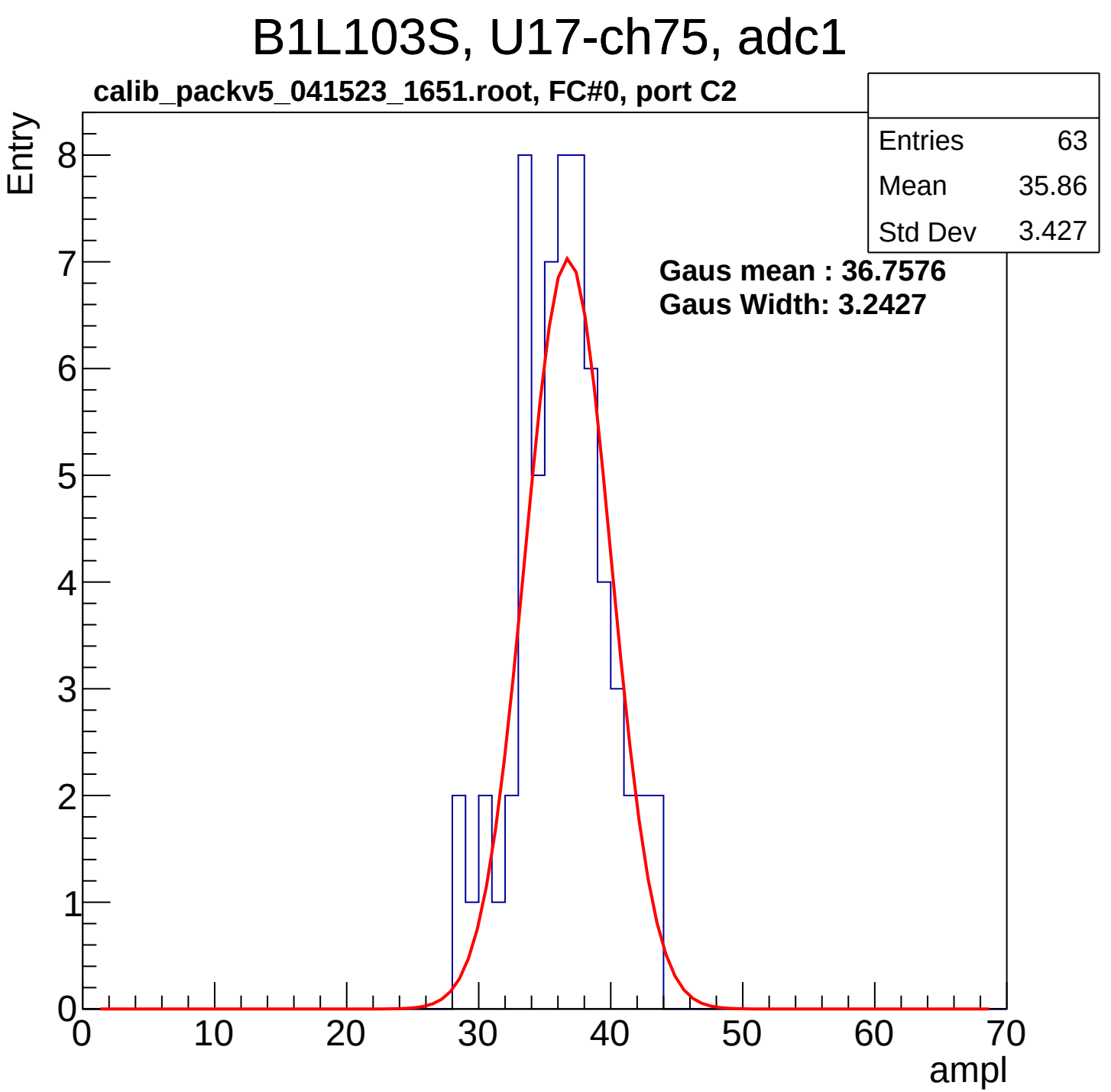

B1L103S, U17-ch74, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 51
Std Dev 10.05
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

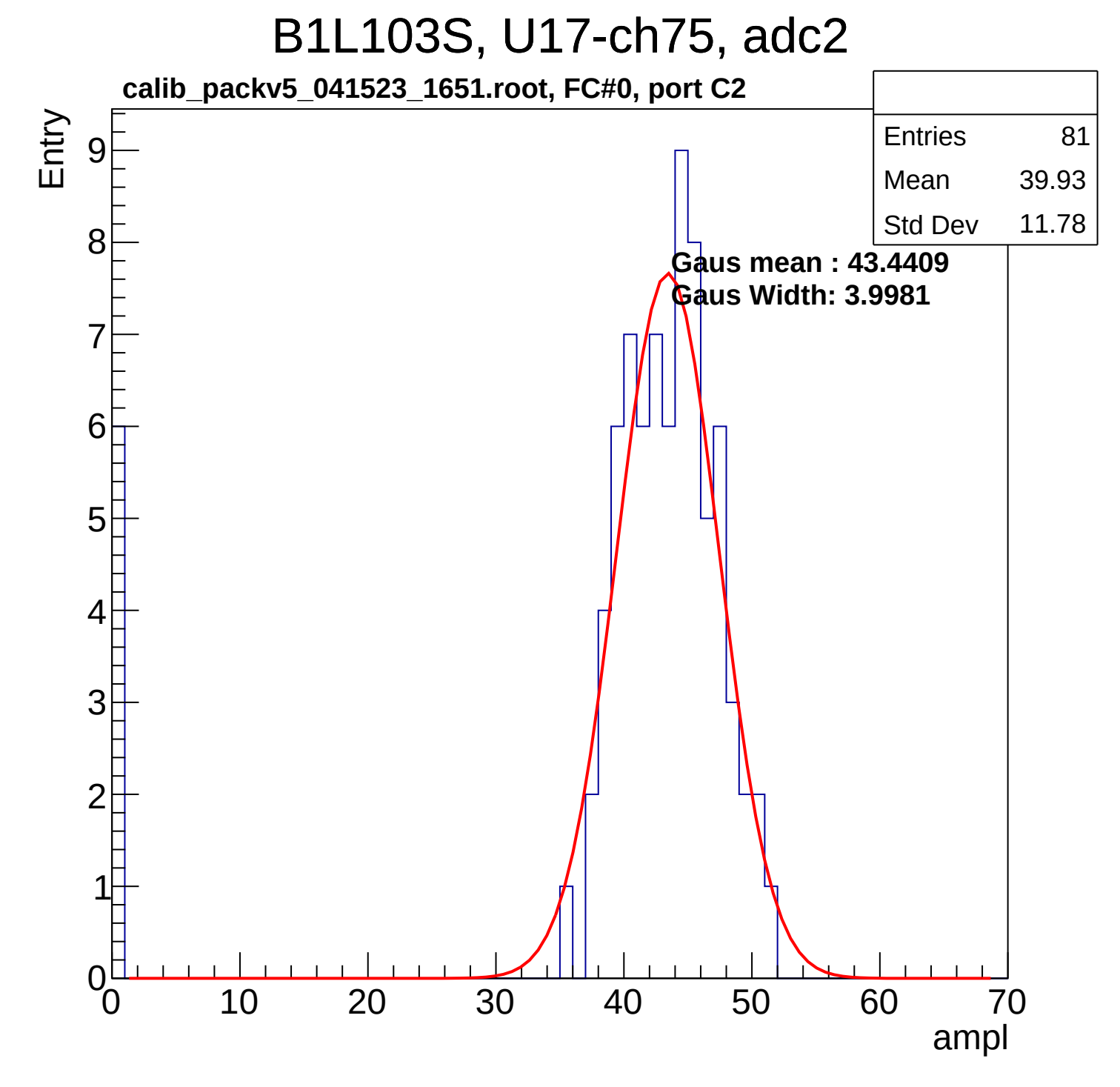

B1L103S, U17-ch74, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.09
Std Dev 2.884
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

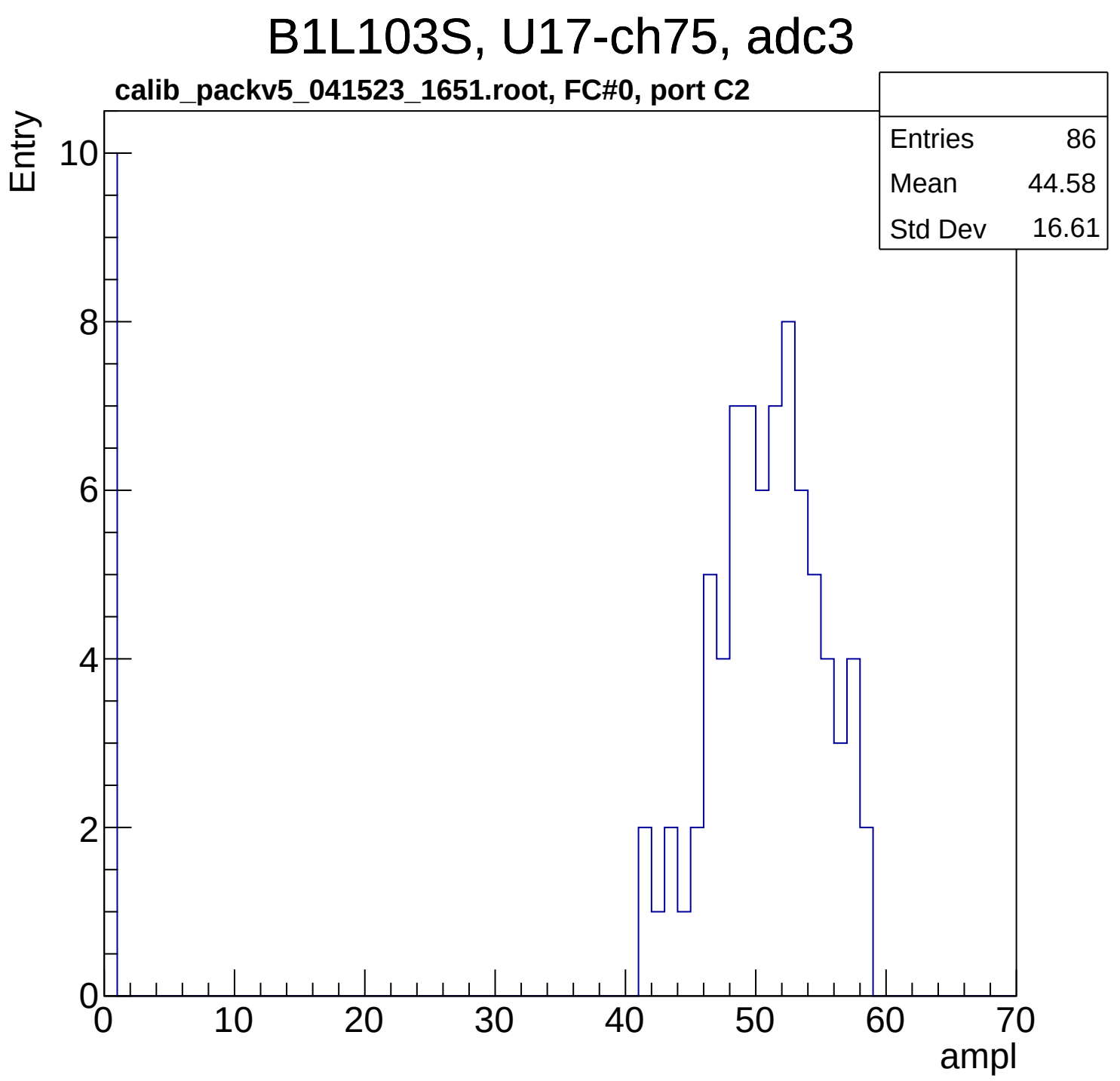

B1L103S, U17-ch74, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 58.21
Std Dev 13.81
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

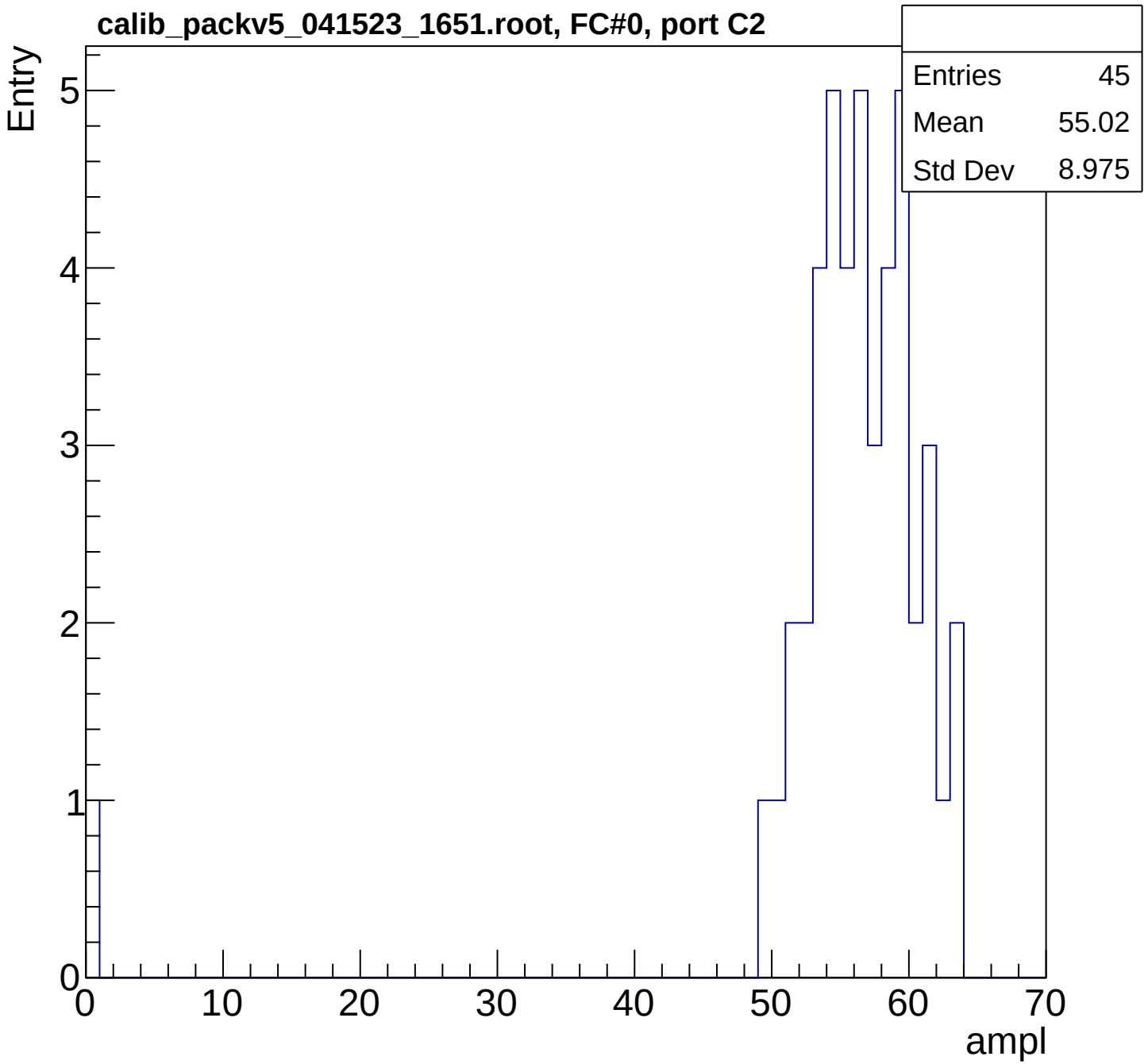

B1L103S, U17-ch74, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

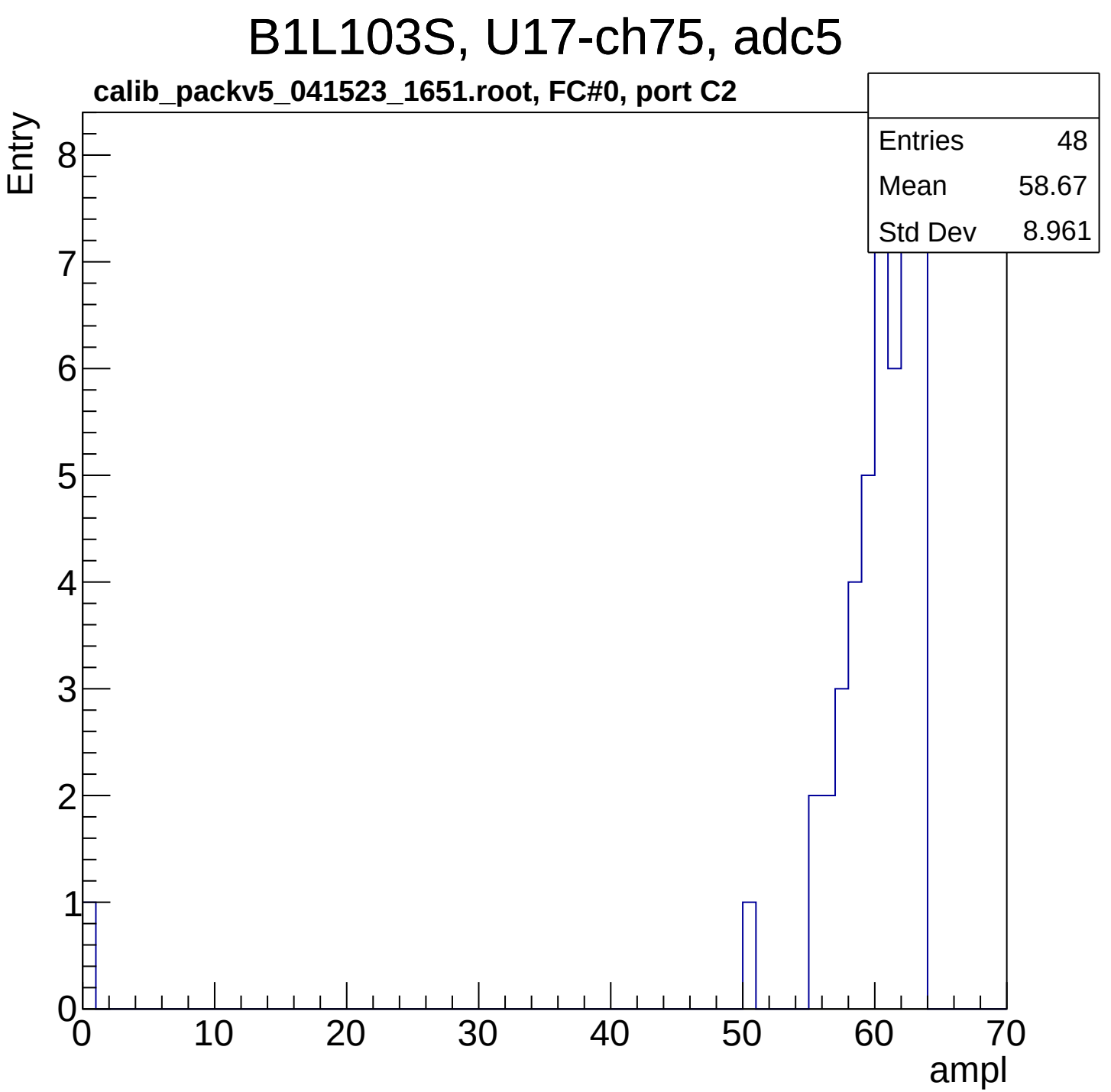

B1L103S, U17-ch75, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 114
Mean 19.95
Std Dev 13.61
Gaus mean : 28.9509
Gaus Width: 4.2548
Entry
ampl
0
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70

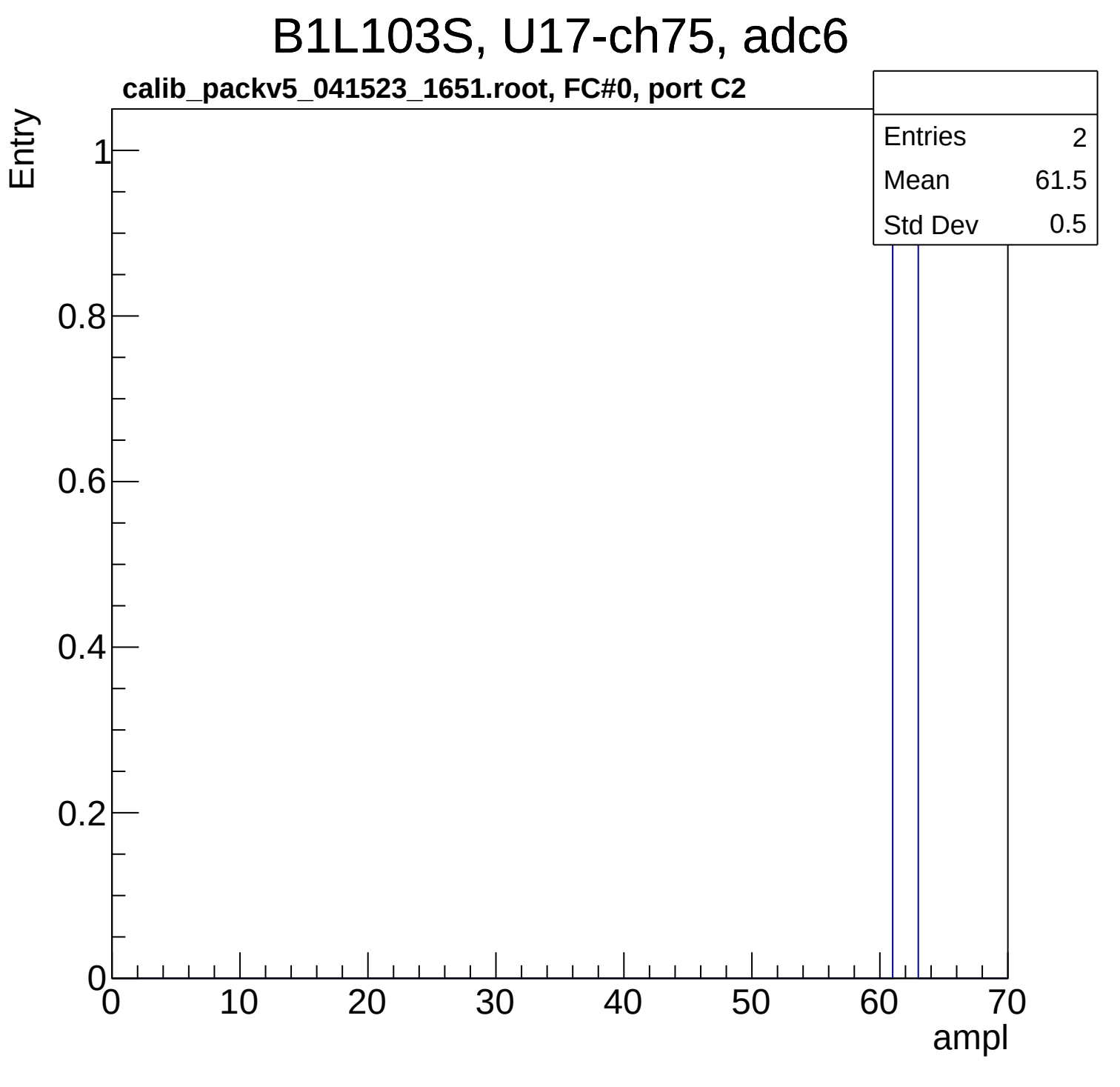

B1L103S, U17-ch75, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 35.86
Std Dev 3.427
Gaus mean : 36.7576
Gaus Width: 3.2427
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

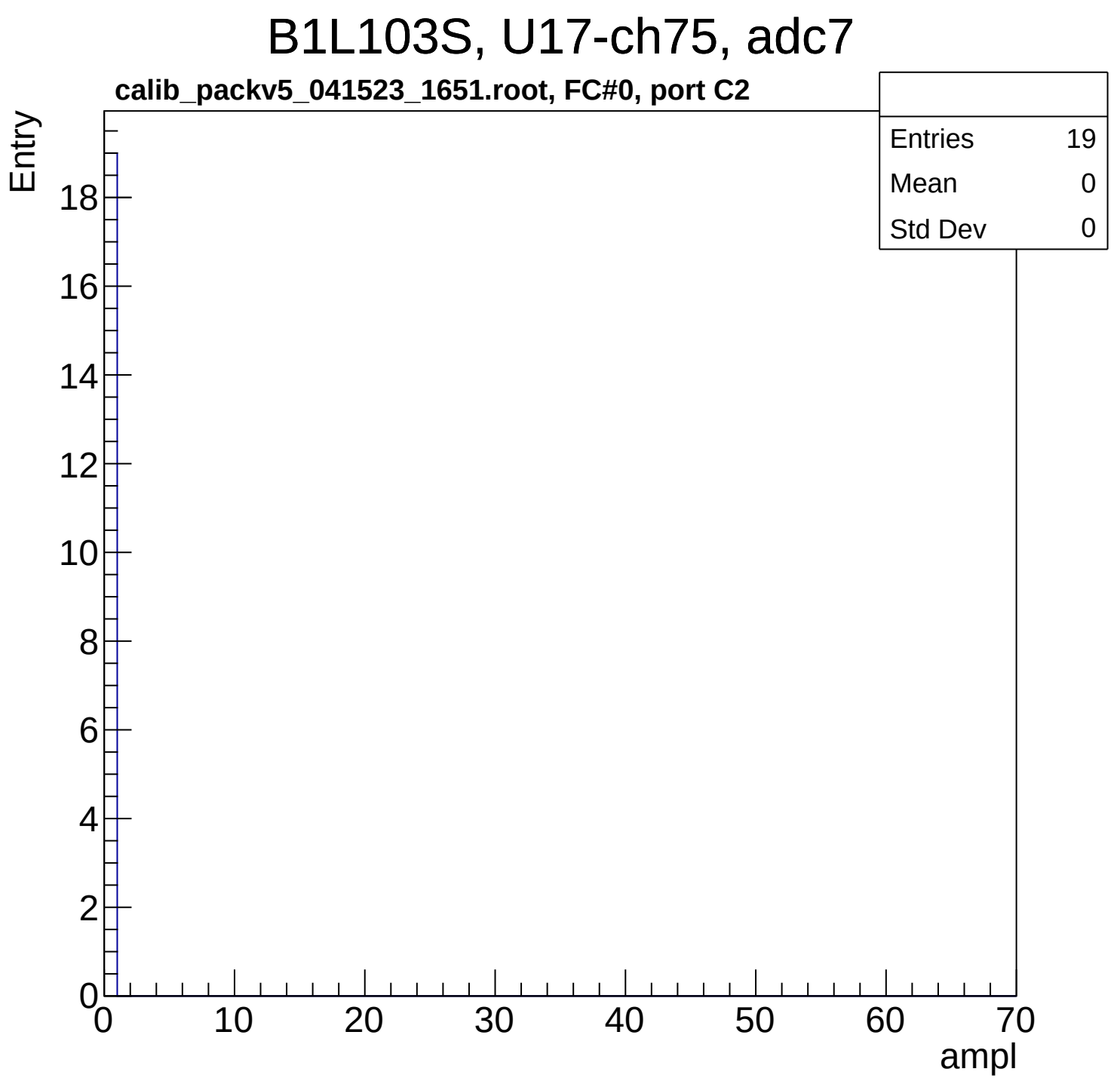

B1L103S, U17-ch75, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 39.93
Std Dev 11.78
Gaus mean : 43.4409
Gaus Width: 3.9981
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

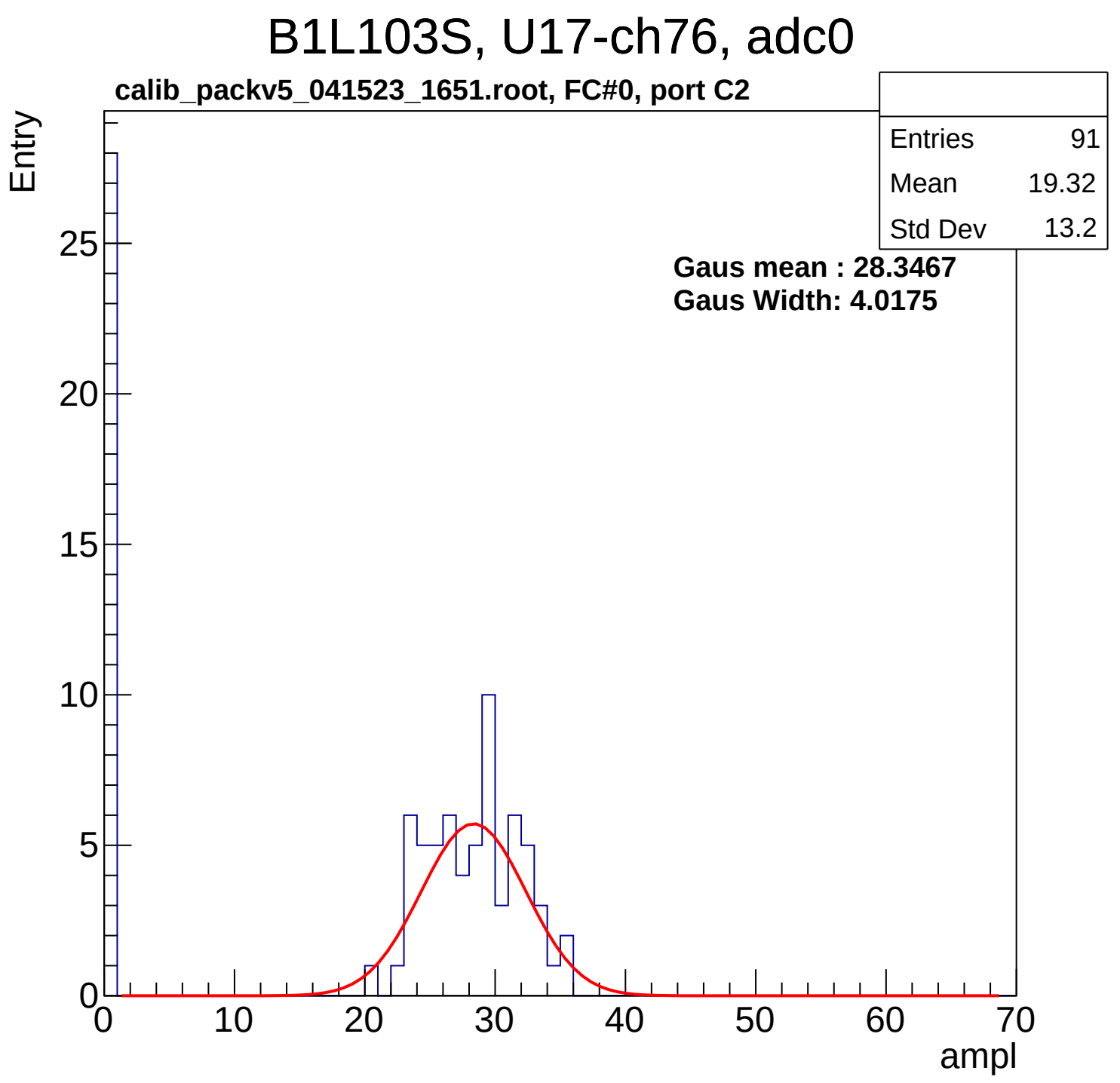

B1L103S, U17-ch75, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 44.58
Std Dev 16.61
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

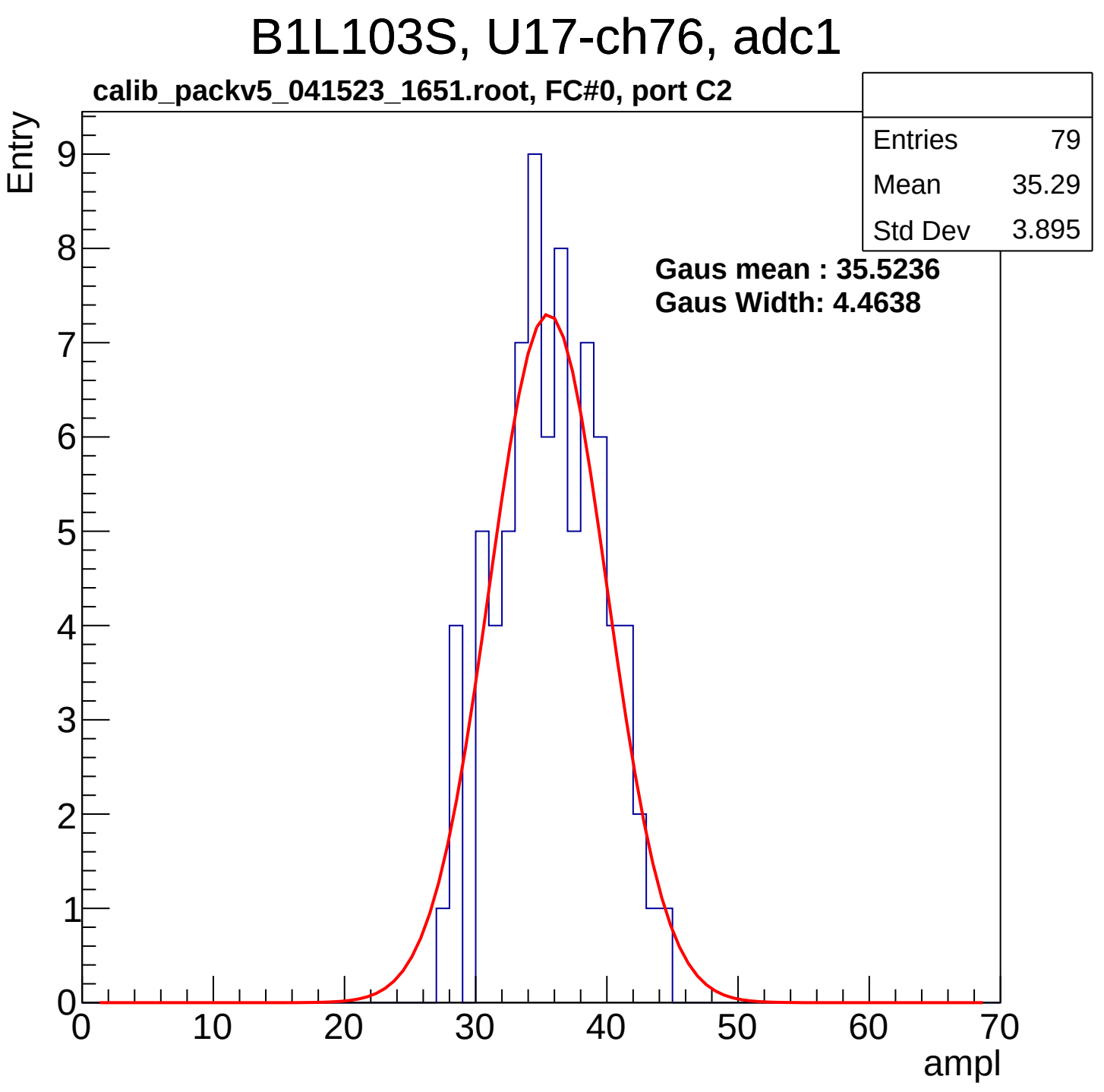

B1L103S, U17-ch75, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 55.02
Std Dev 8.975
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

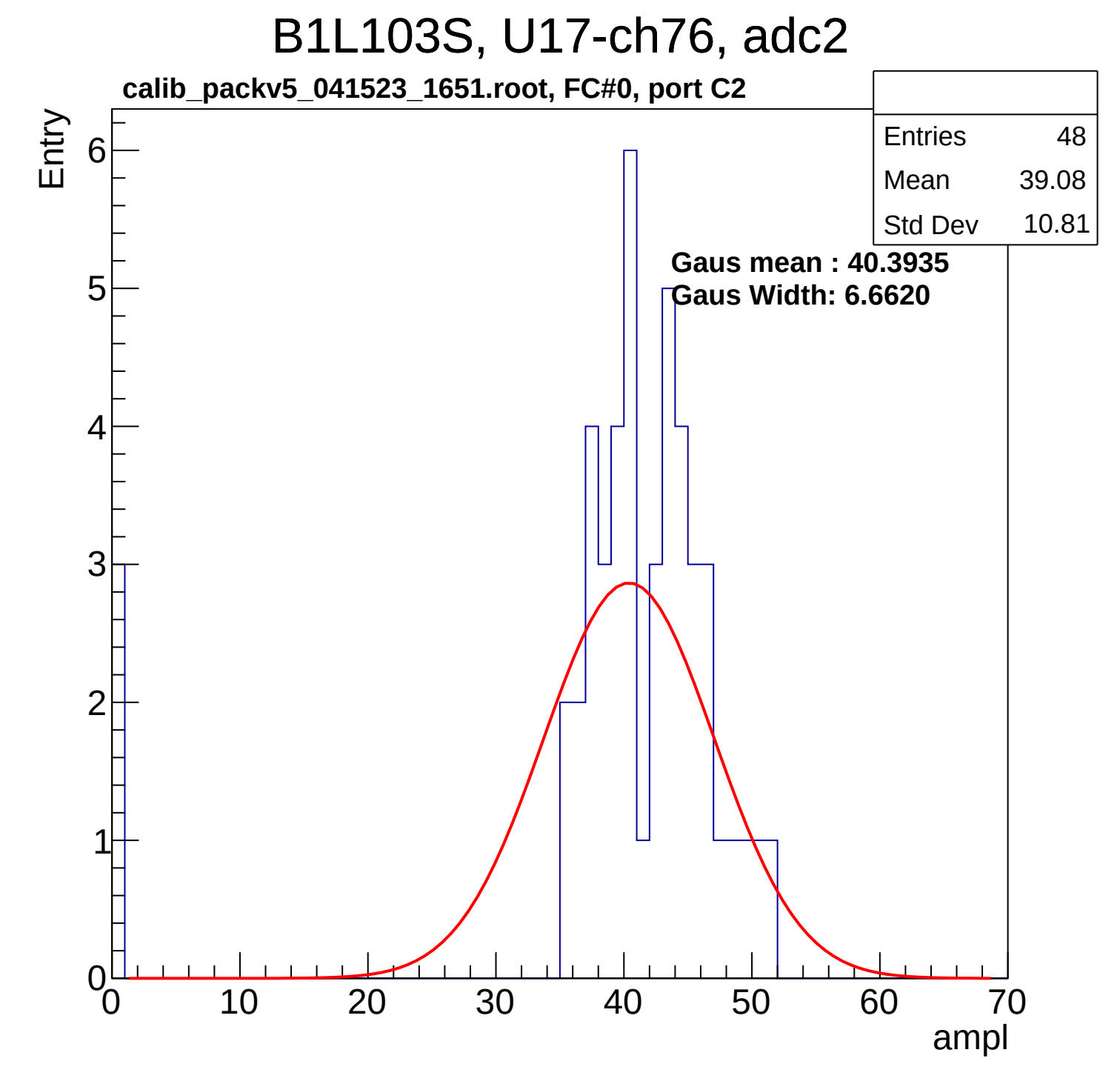

B1L103S, U17-ch75, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.67
Std Dev 8.961
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

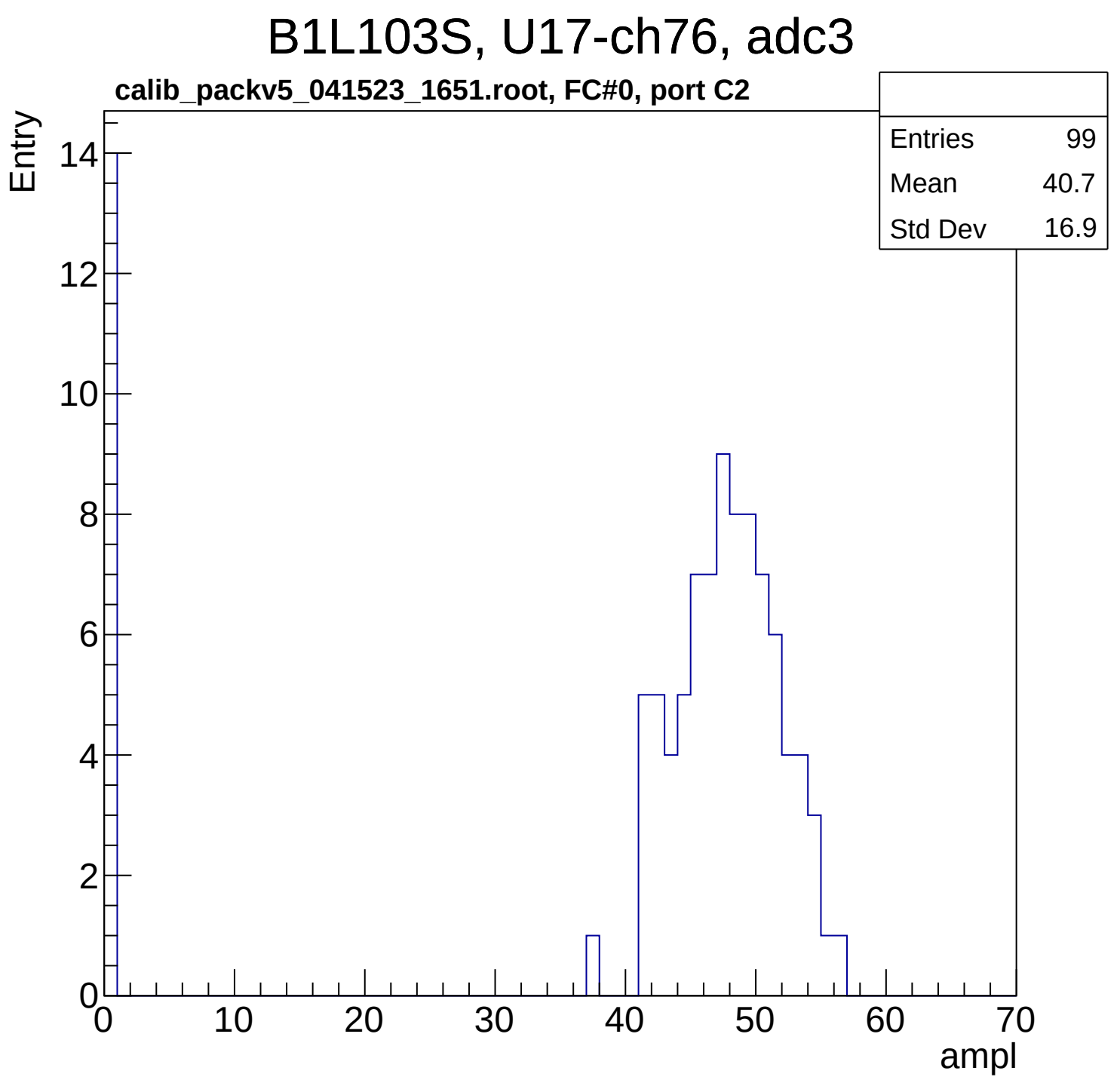

B1L103S, U17-ch75, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 61.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

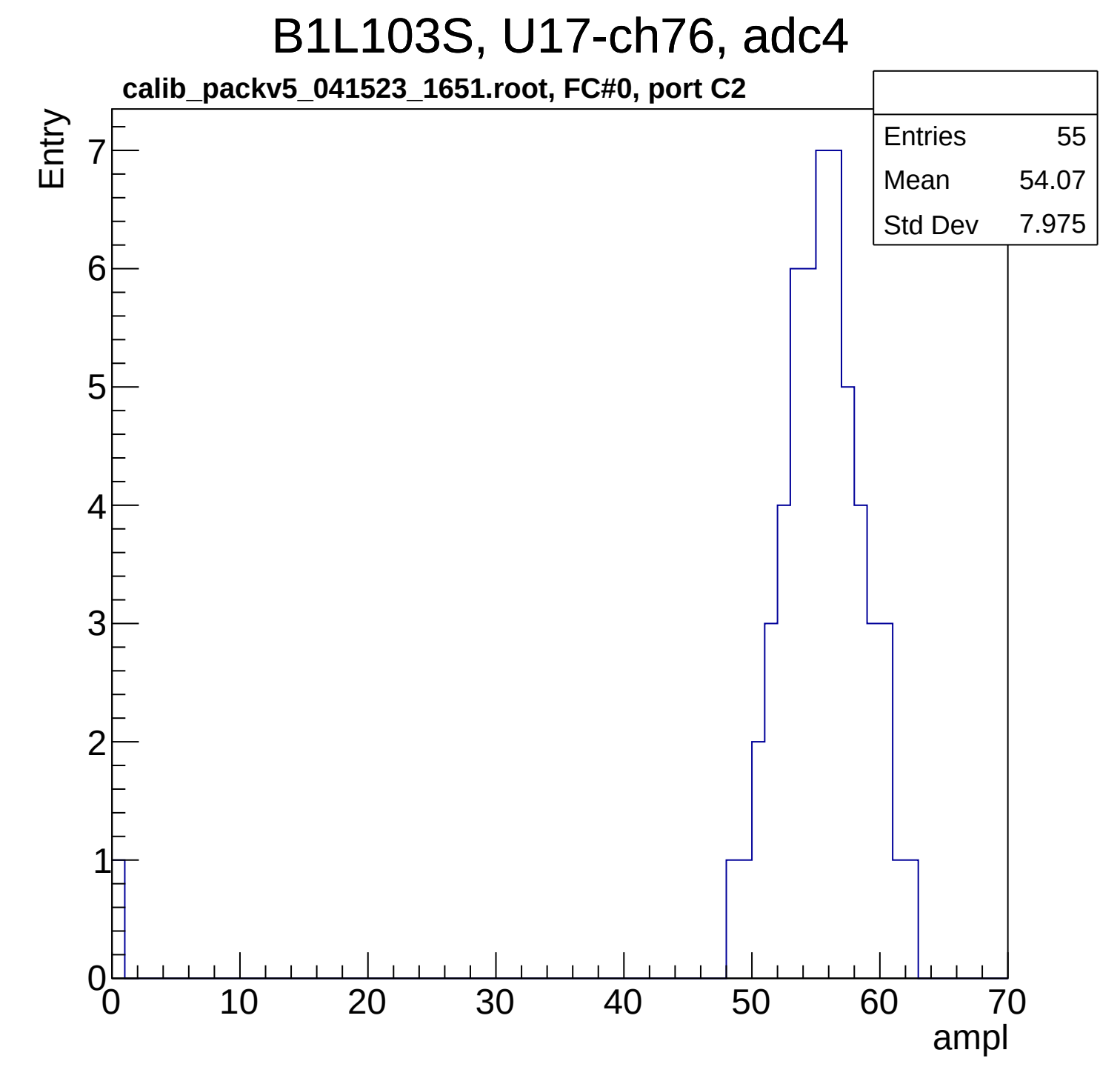

B1L103S, U17-ch75, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

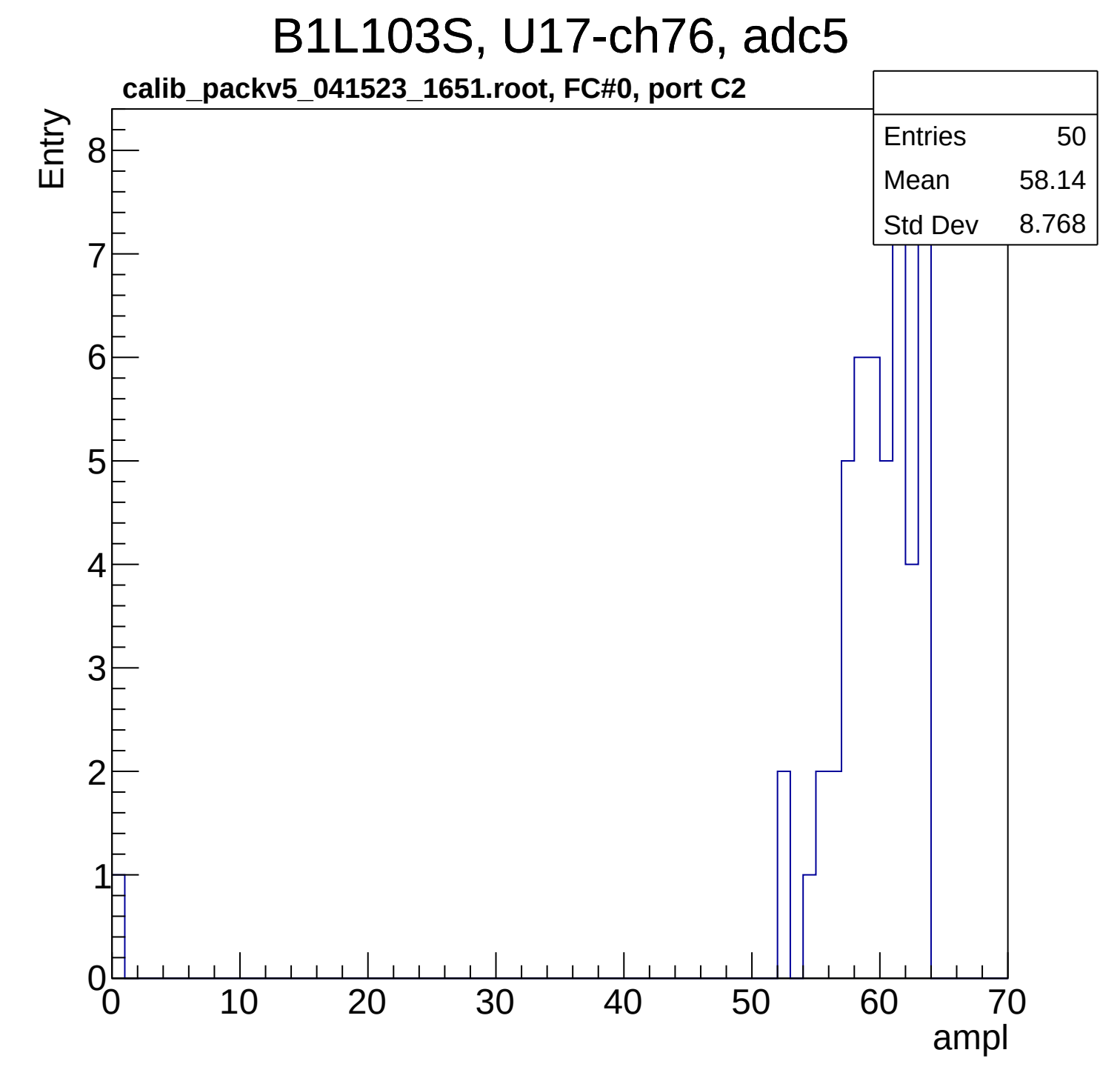

B1L103S, U17-ch76, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 19.32
Std Dev 13.2
Gaus mean : 28.3467
Gaus Width: 4.0175
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70

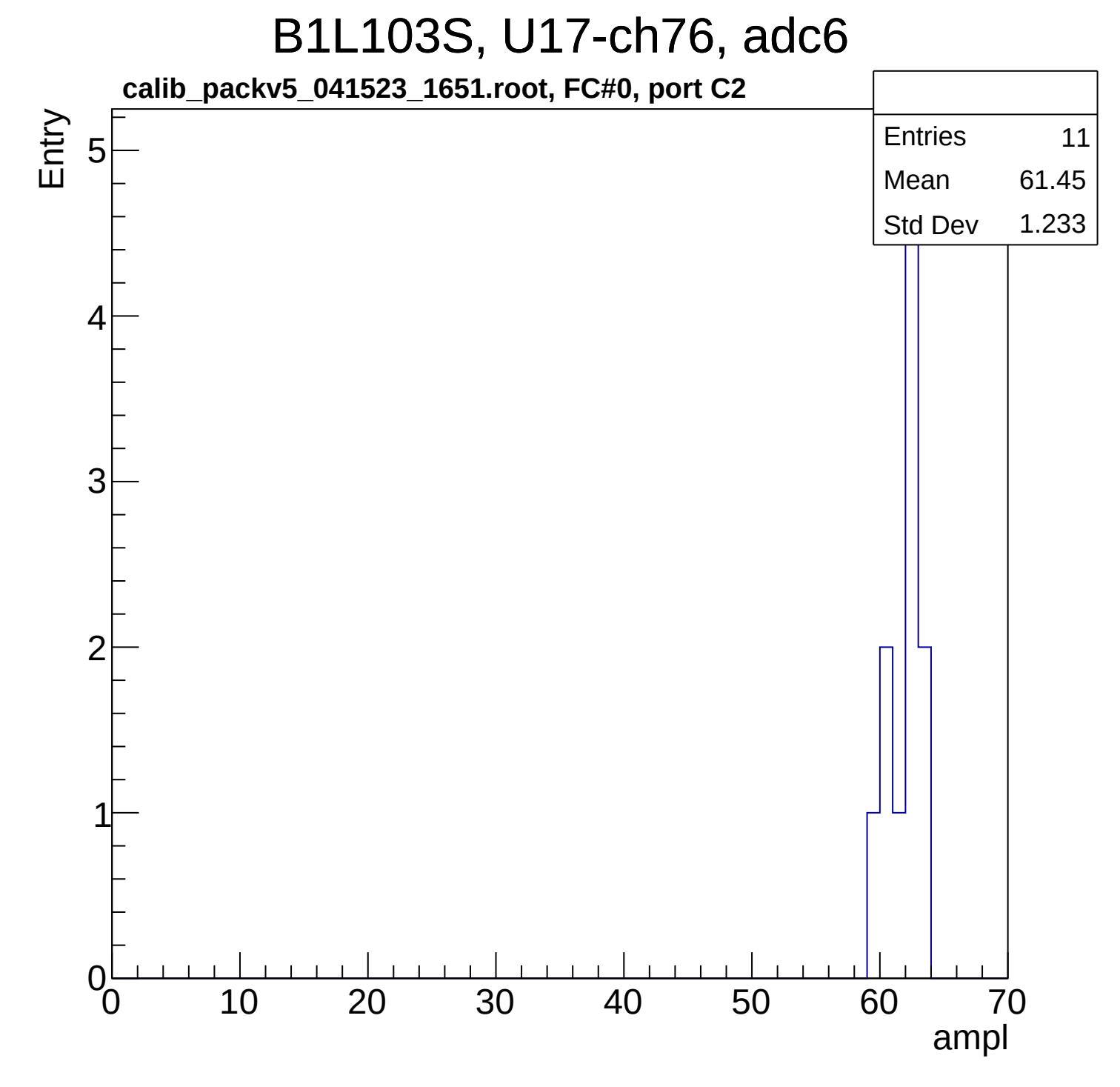

B1L103S, U17-ch76, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 35.29
Std Dev 3.895
Gaus mean : 35.5236
Gaus Width: 4.4638
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

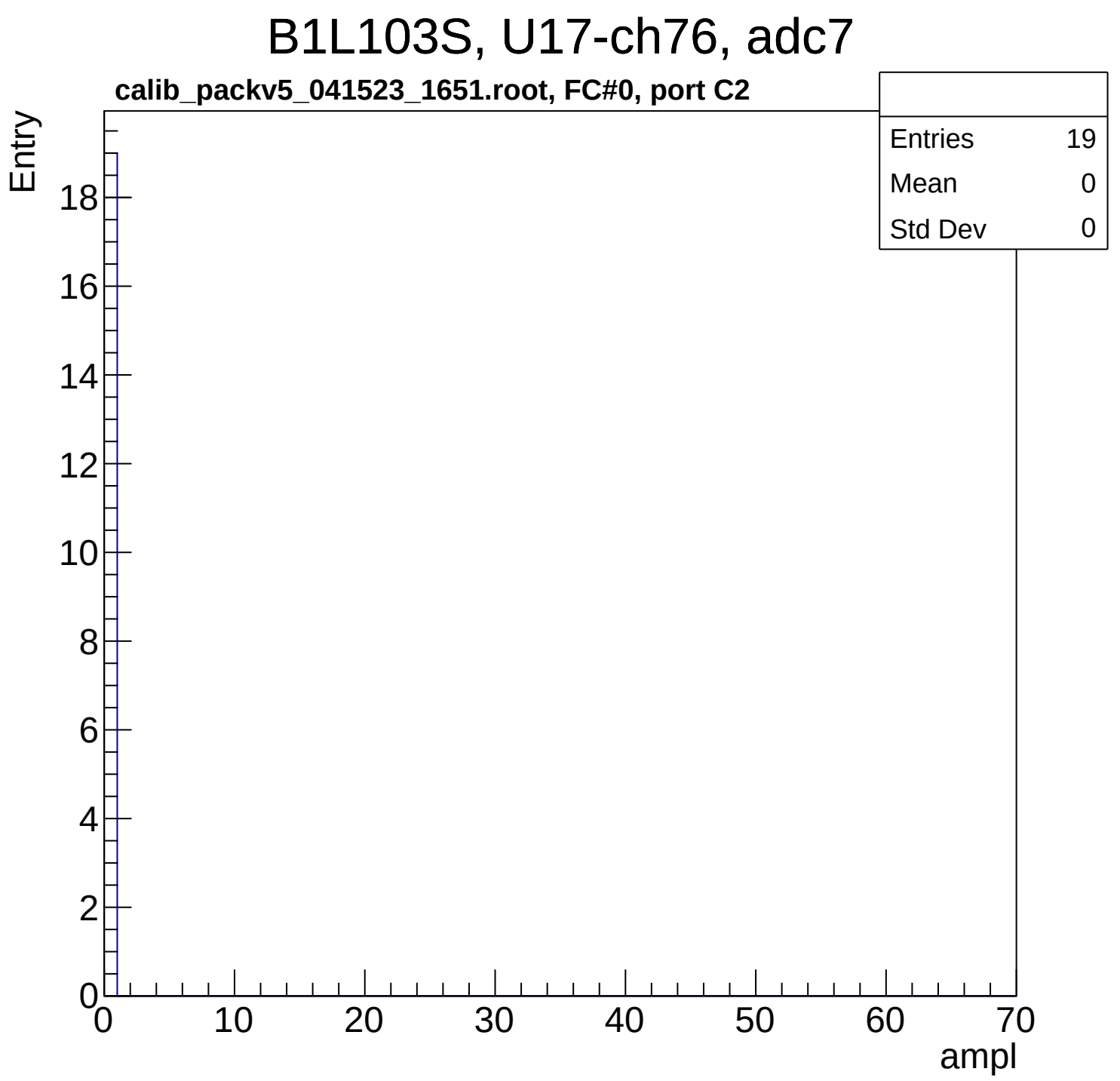

B1L103S, U17-ch76, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 39.08
Std Dev 10.81
Gaus mean : 40.3935
Gaus Width: 6.6620
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

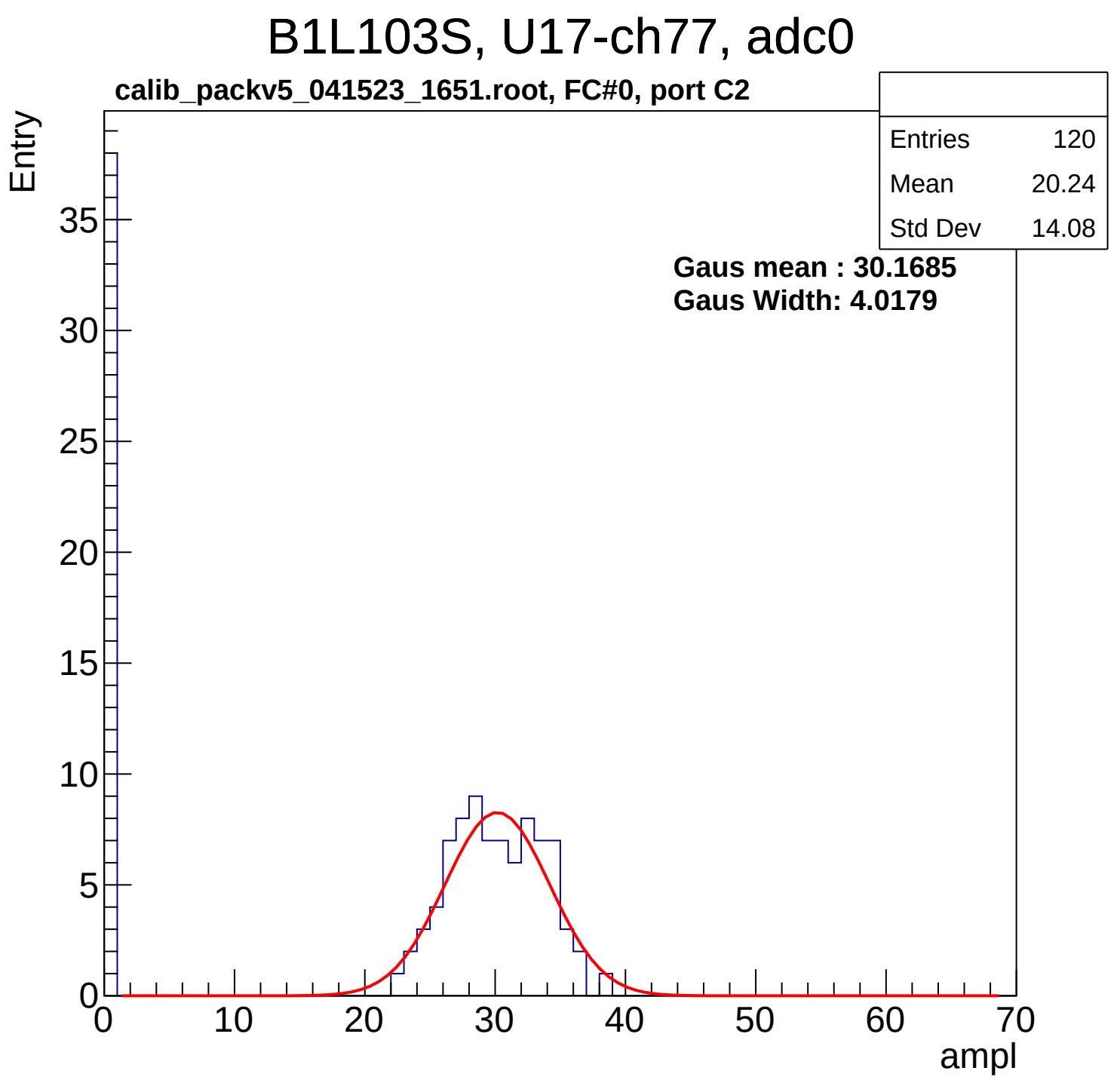

B1L103S, U17-ch76, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 40.7
Std Dev 16.9
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

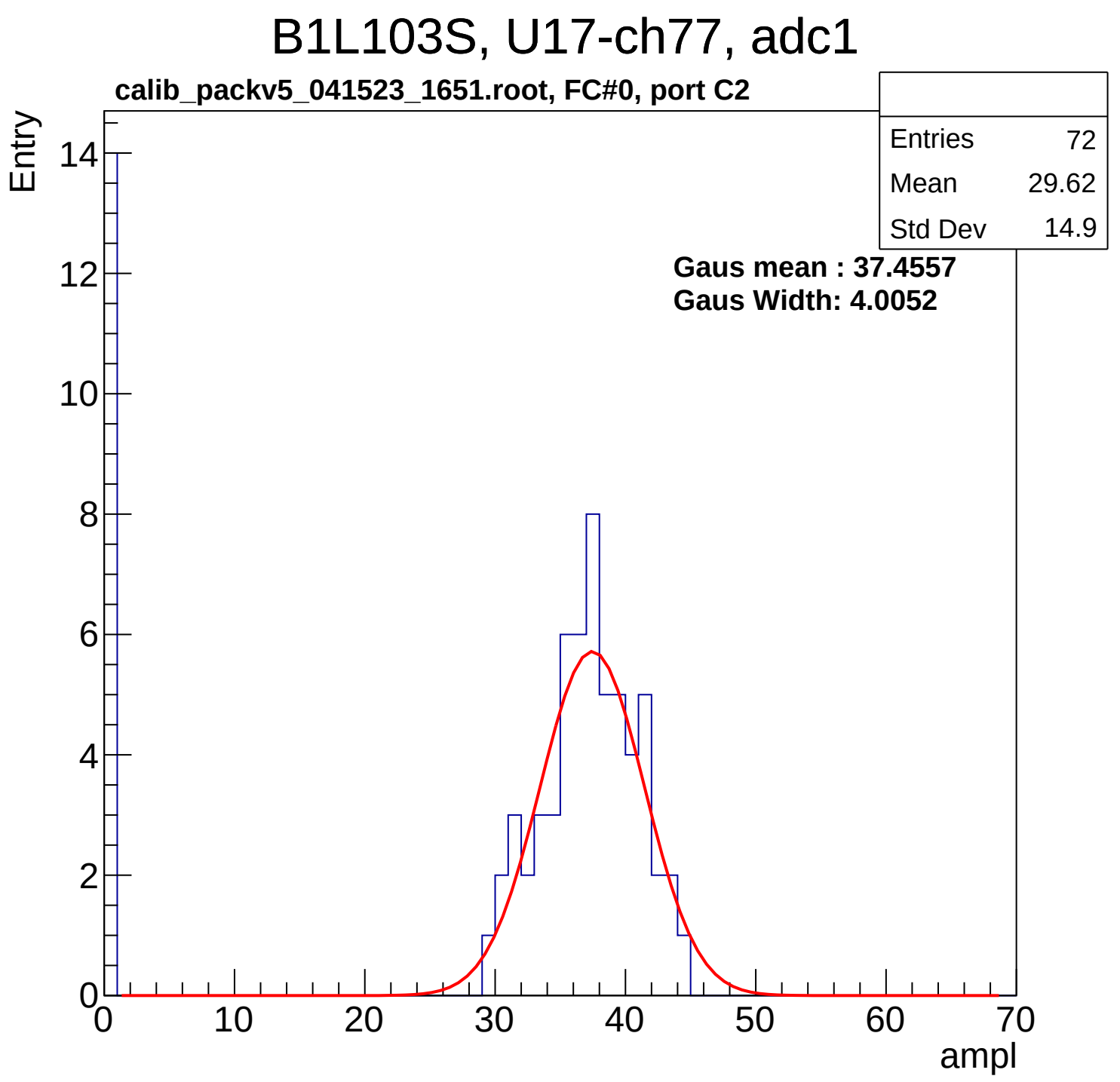

B1L103S, U17-ch76, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 54.07
Std Dev 7.975
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

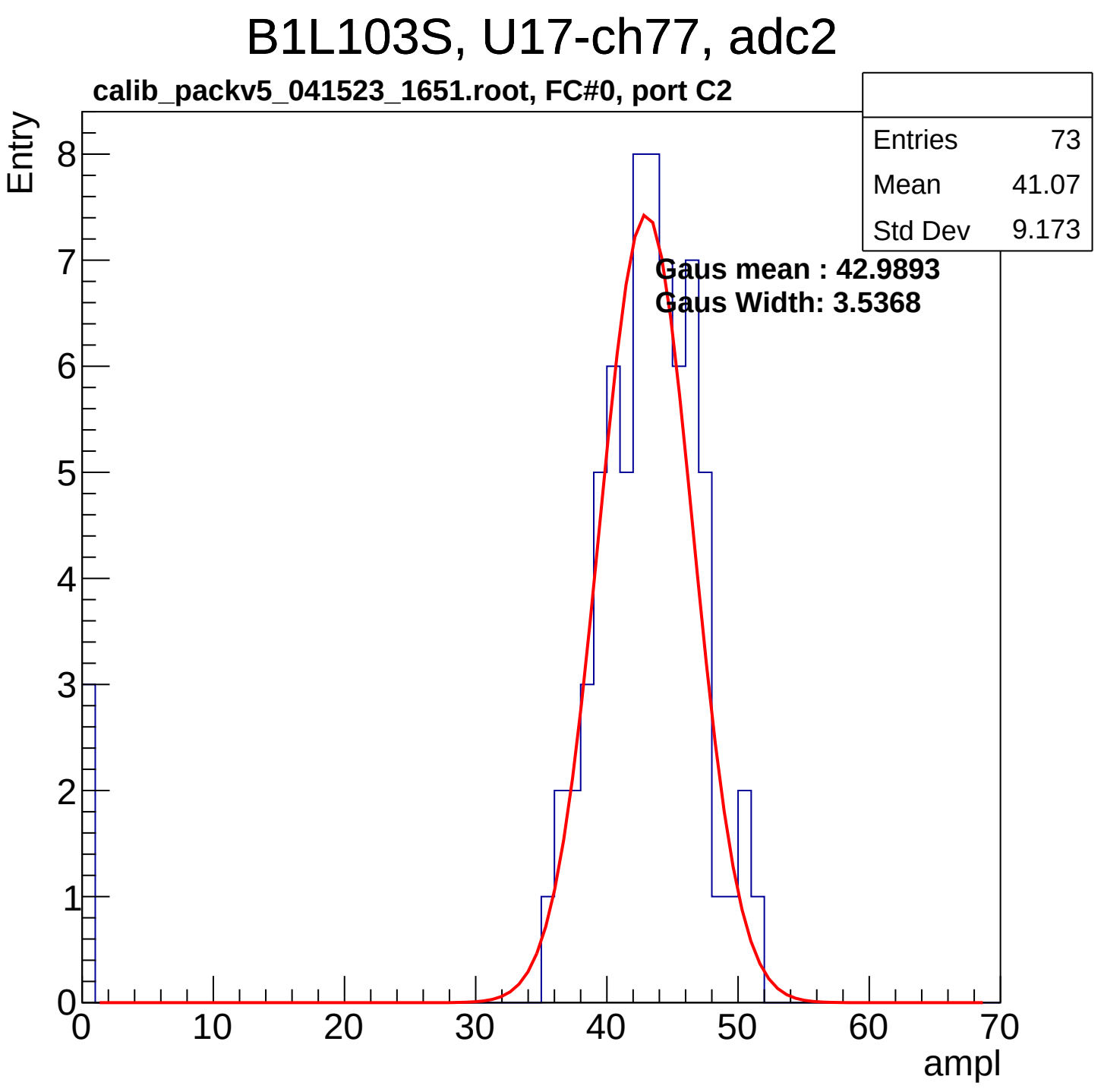

B1L103S, U17-ch76, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.14
Std Dev 8.768
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

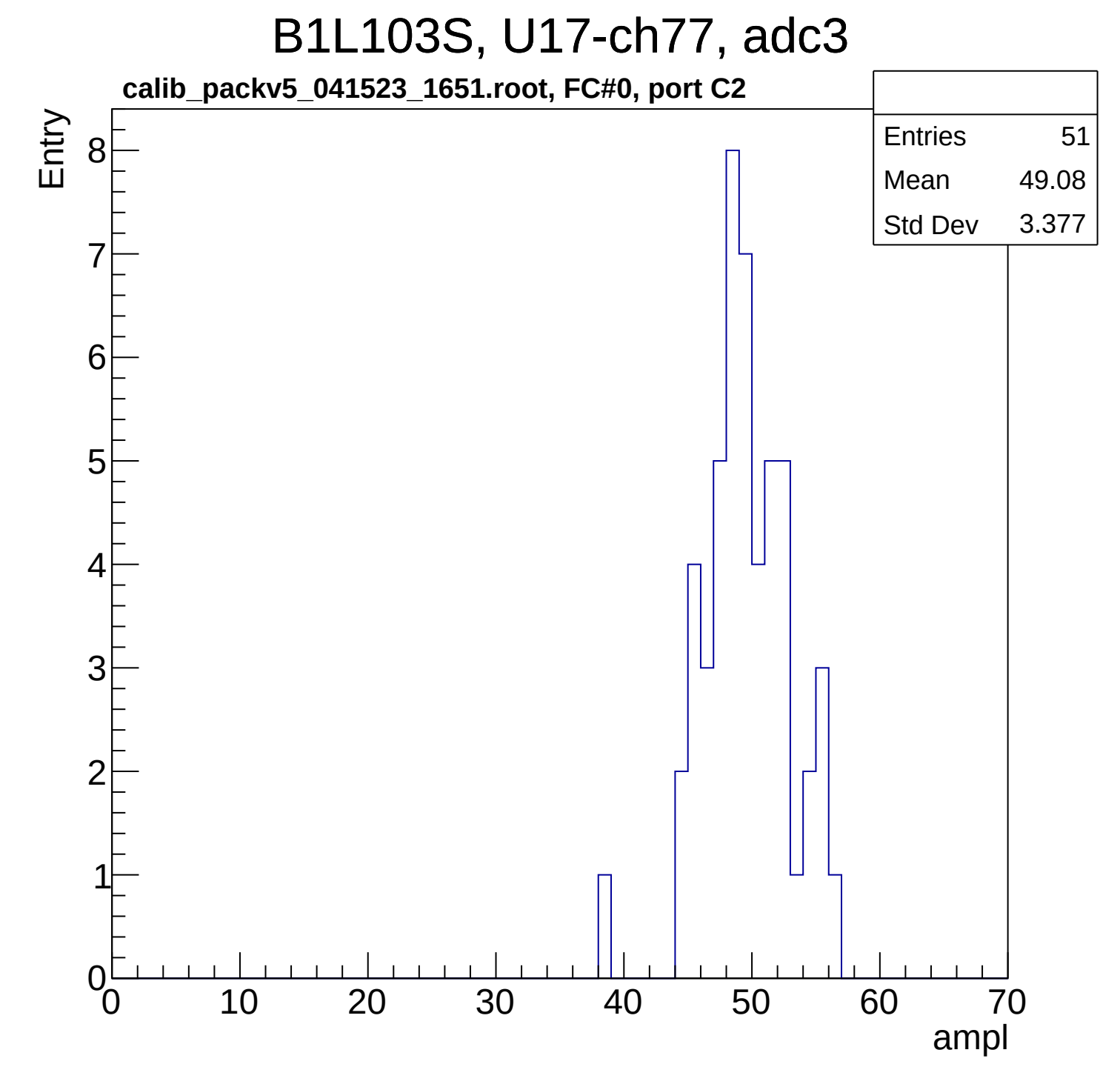

B1L103S, U17-ch76, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.45
Std Dev 1.233
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

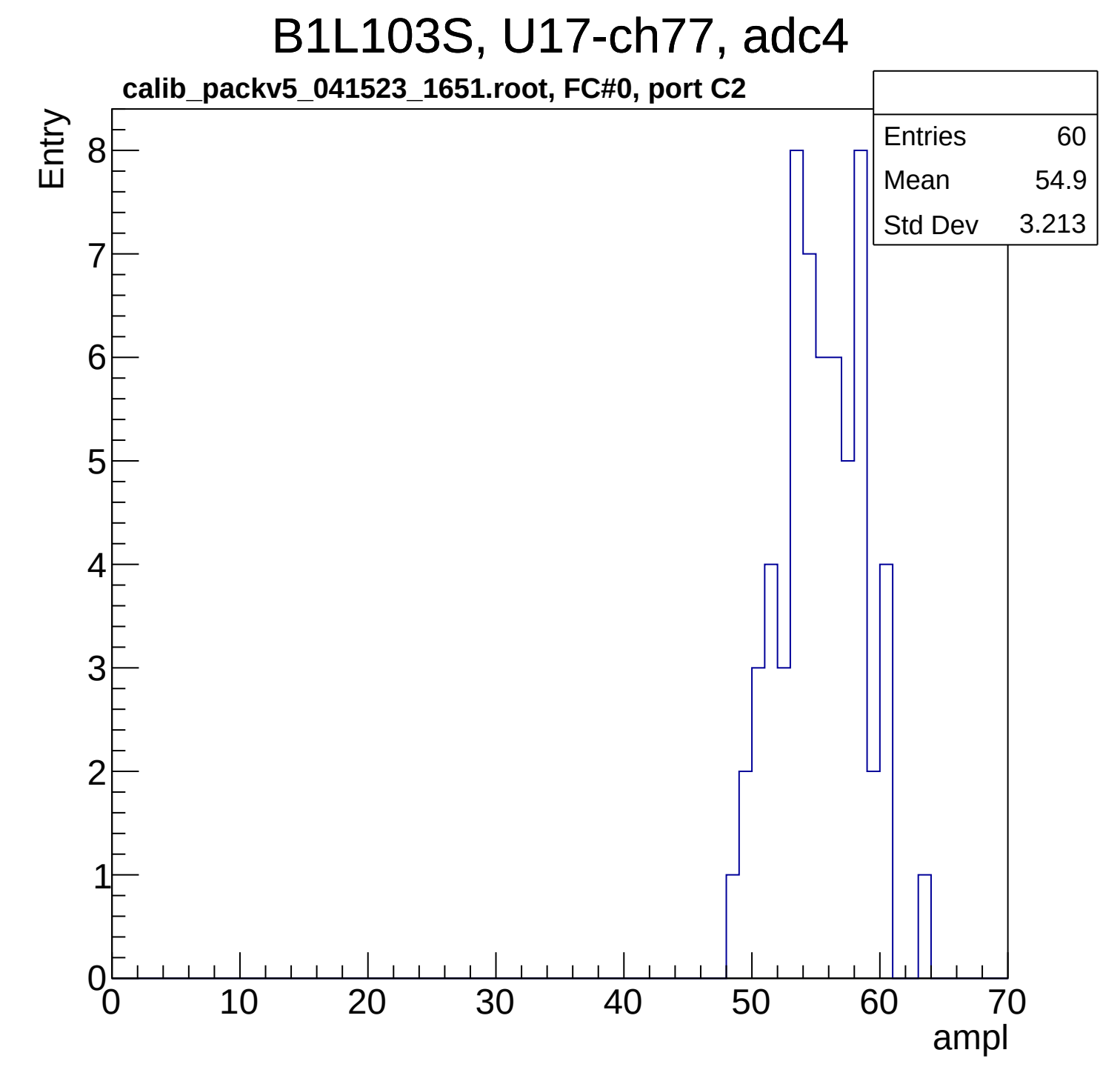

B1L103S, U17-ch76, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

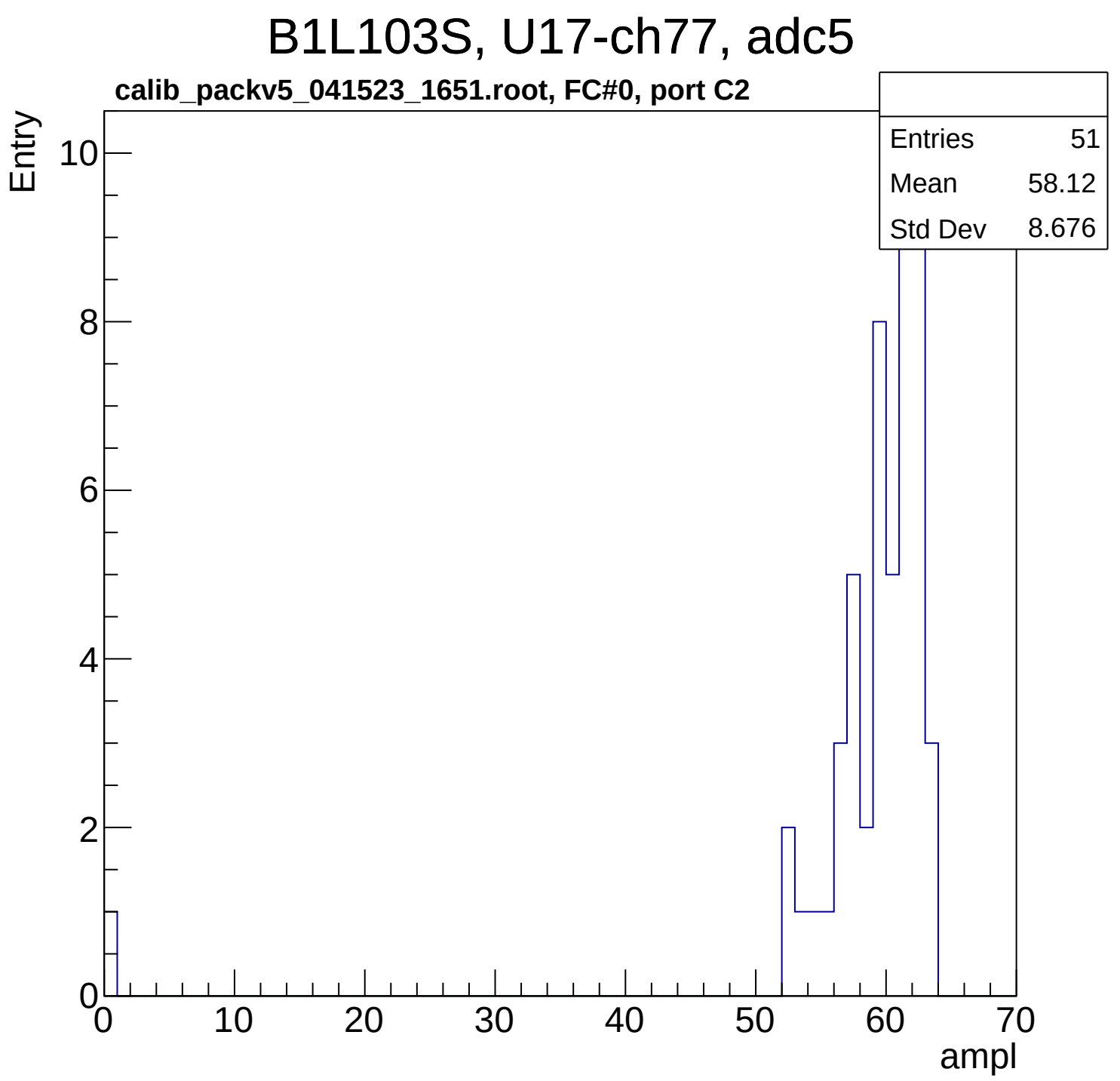

B1L103S, U17-ch77, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 120
Mean 20.24
Std Dev 14.08
Gaus mean : 30.1685
Gaus Width: 4.0179
Entry
ampl
0
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70

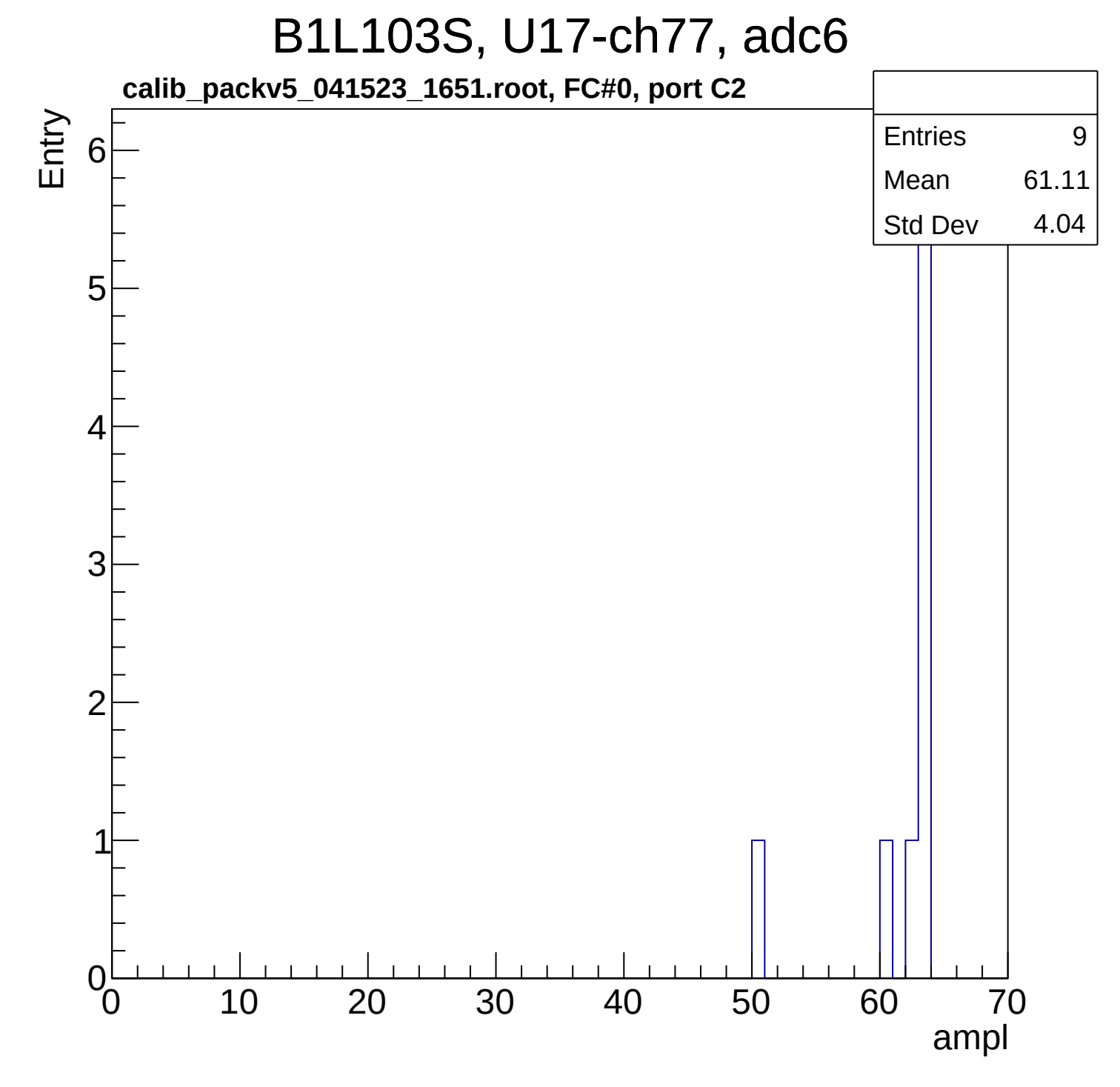

B1L103S, U17-ch77, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 29.62
Std Dev 14.9
Gaus mean : 37.4557
Gaus Width: 4.0052
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

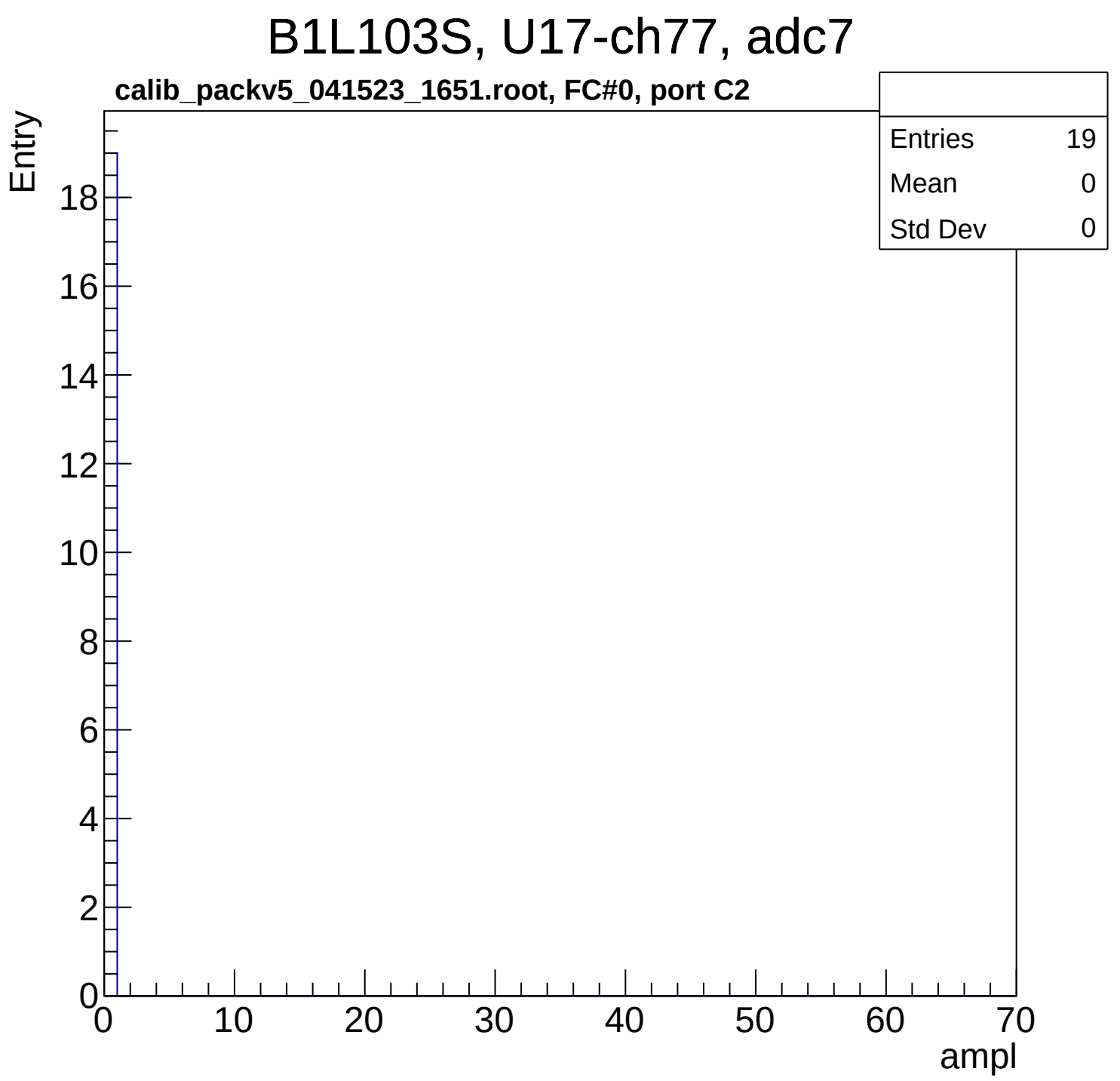

B1L103S, U17-ch77, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 41.07
Std Dev 9.173
Gaus mean : 42.9893
Gaus Width: 3.5368
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

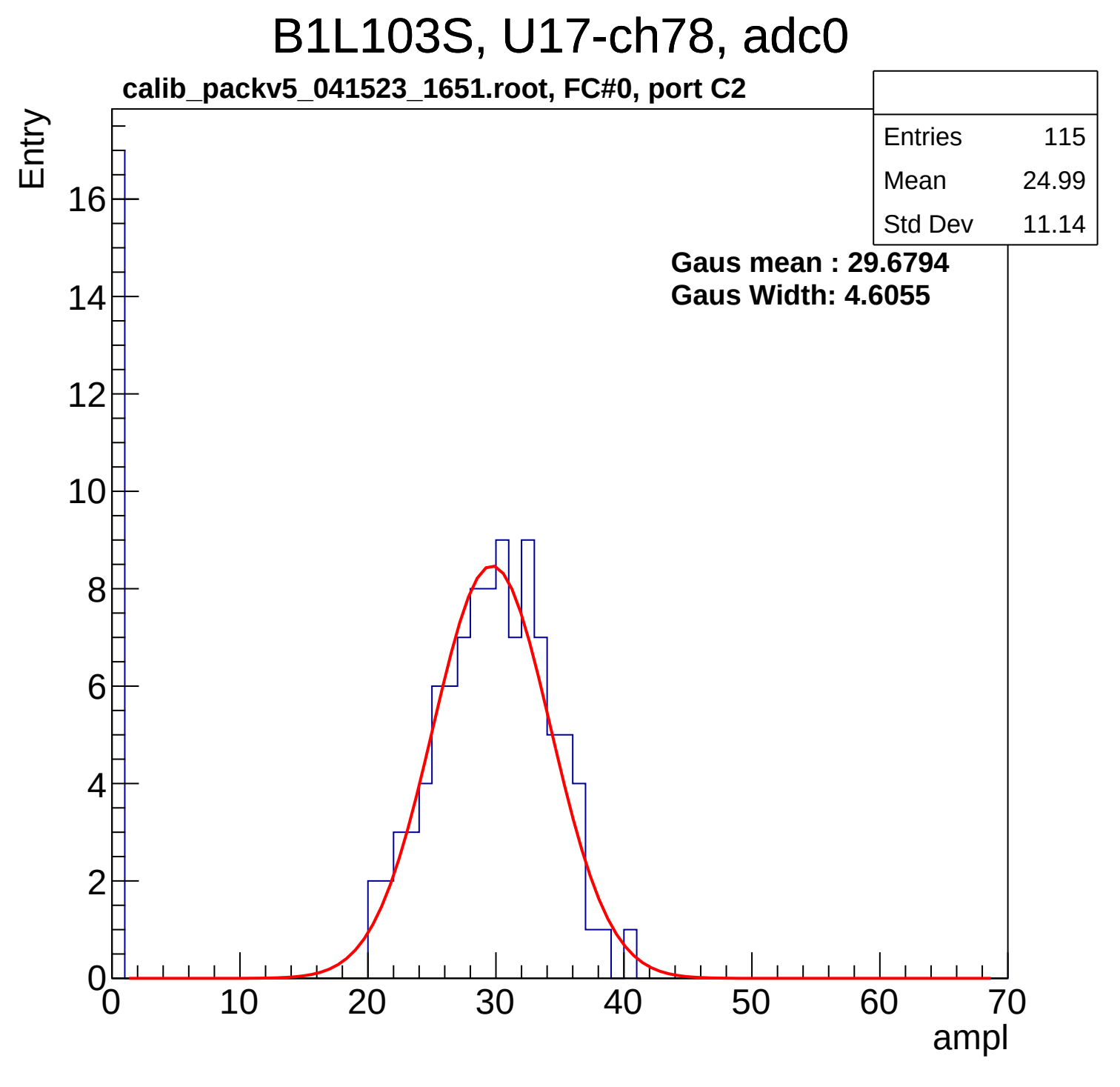

B1L103S, U17-ch77, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 49.08
Std Dev 3.377
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

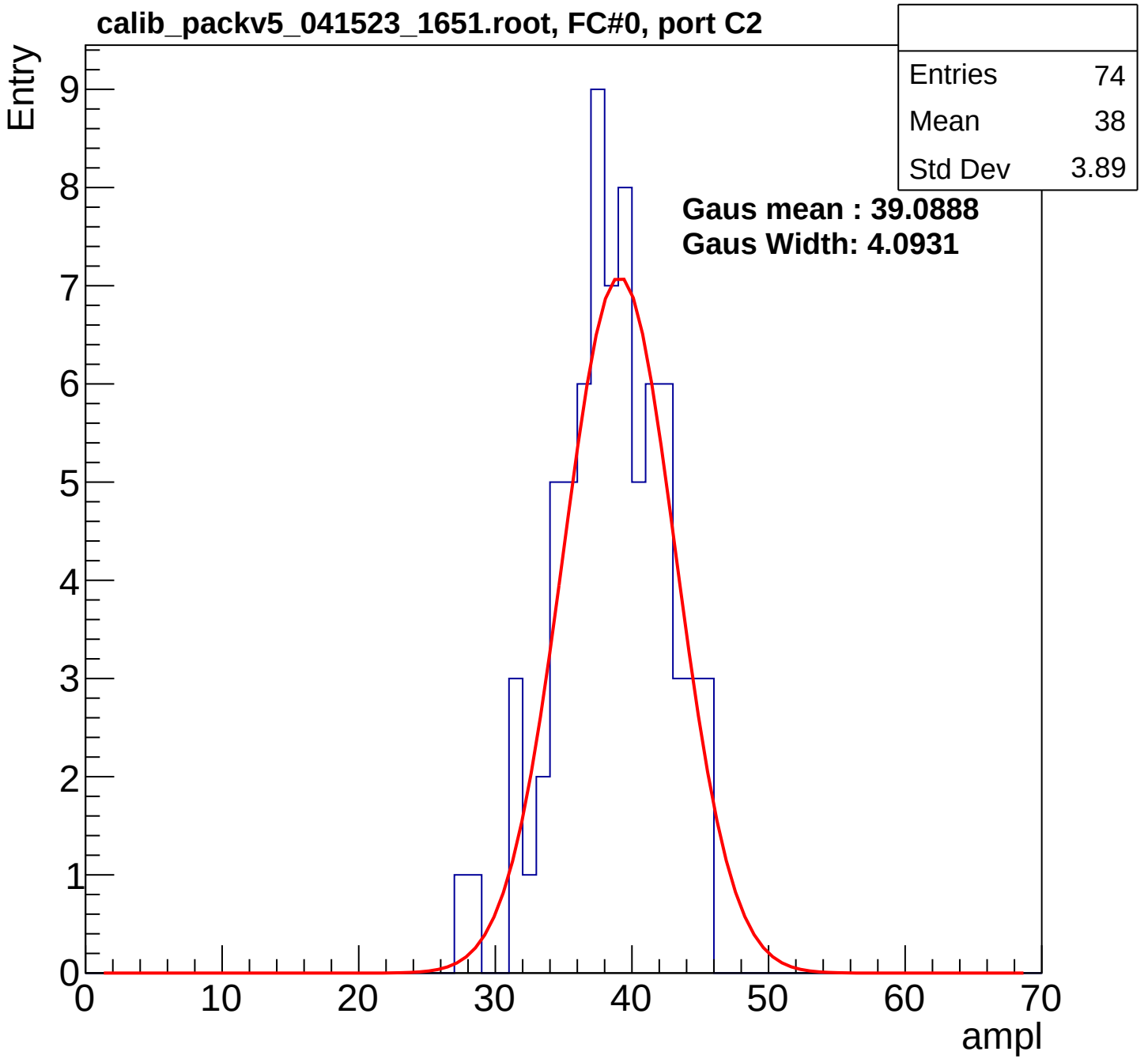

B1L103S, U17-ch77, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 54.9
Std Dev 3.213
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

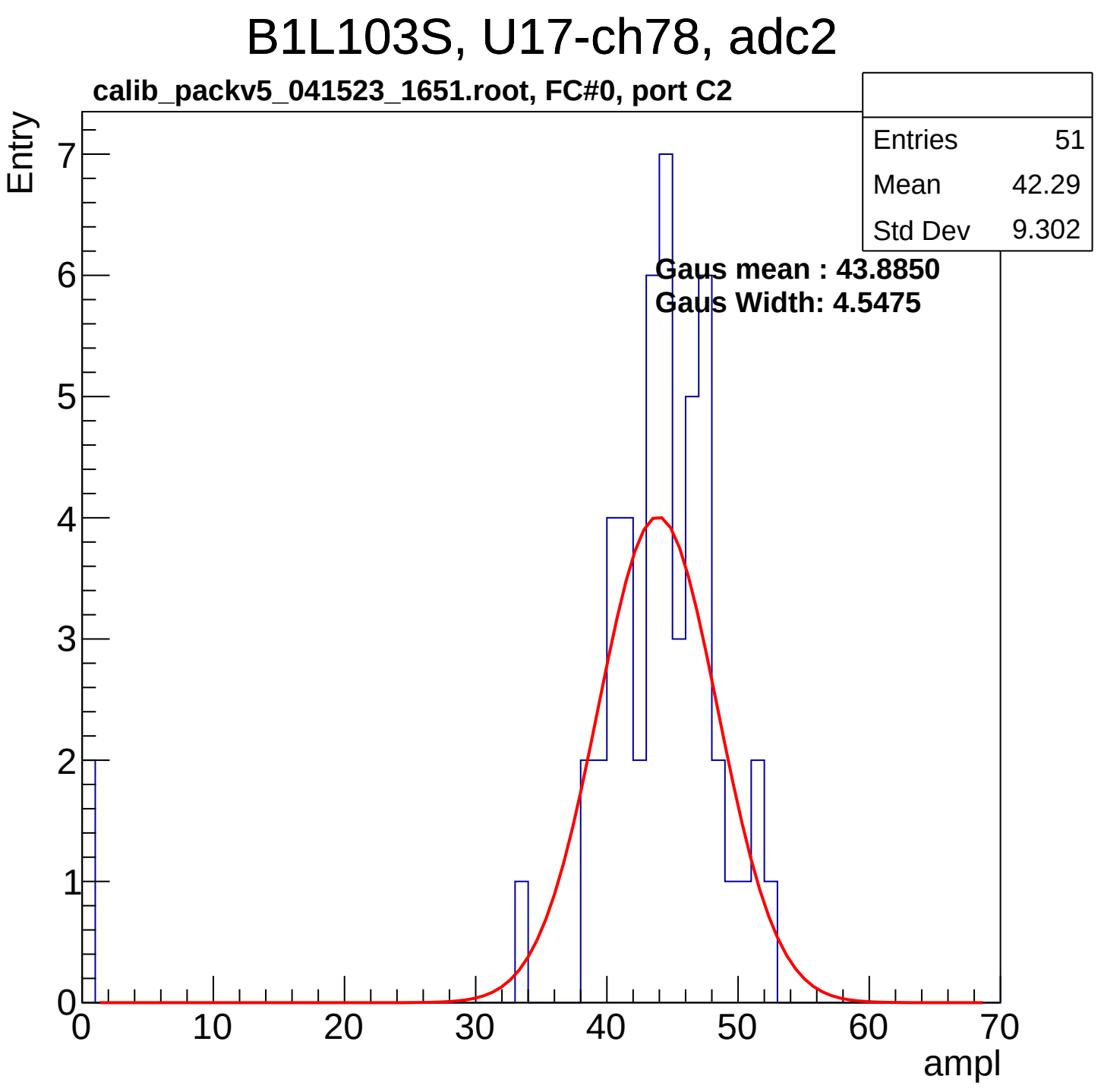

B1L103S, U17-ch77, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.12
Std Dev 8.676
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

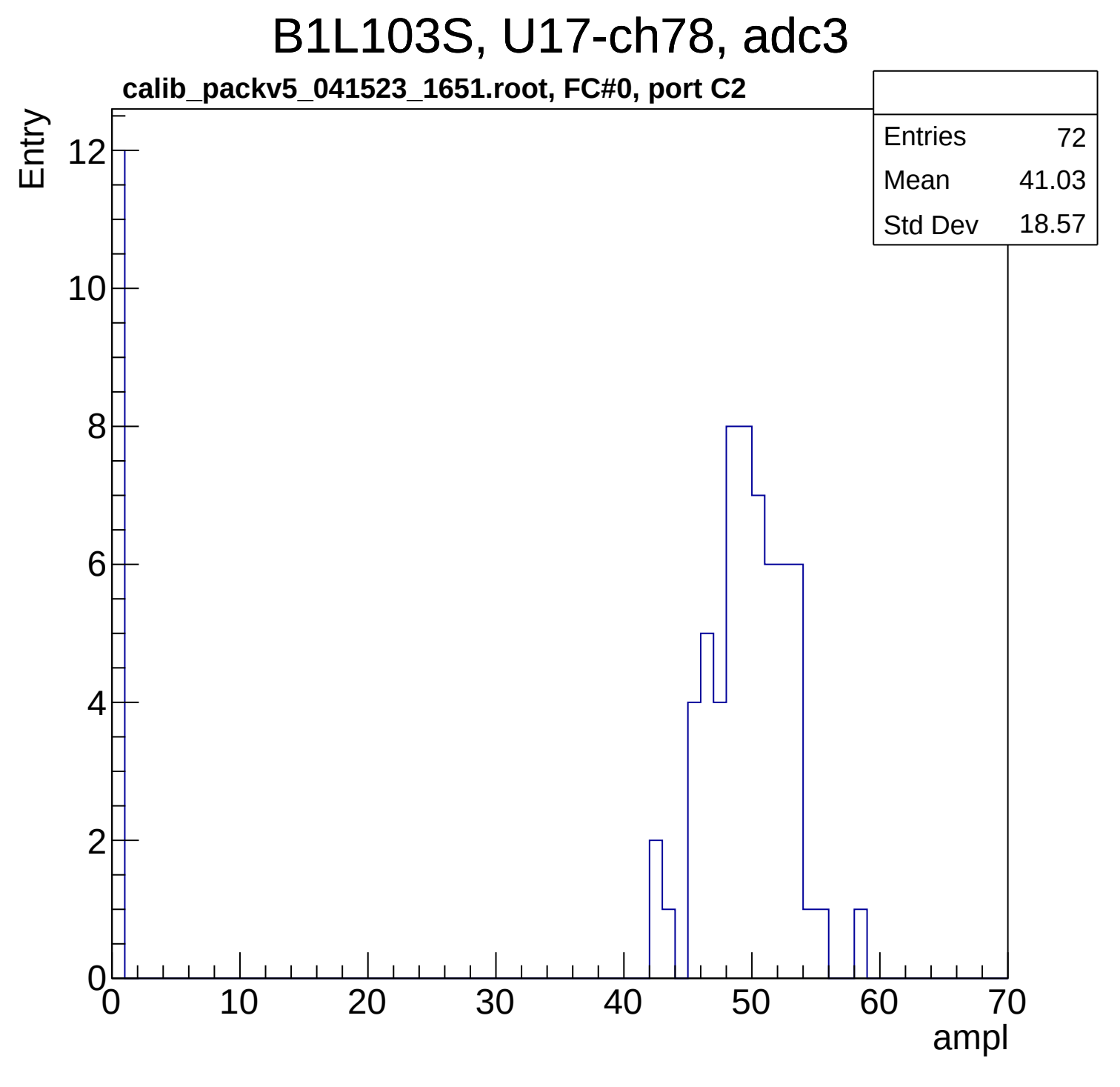

B1L103S, U17-ch77, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.11
Std Dev 4.04
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

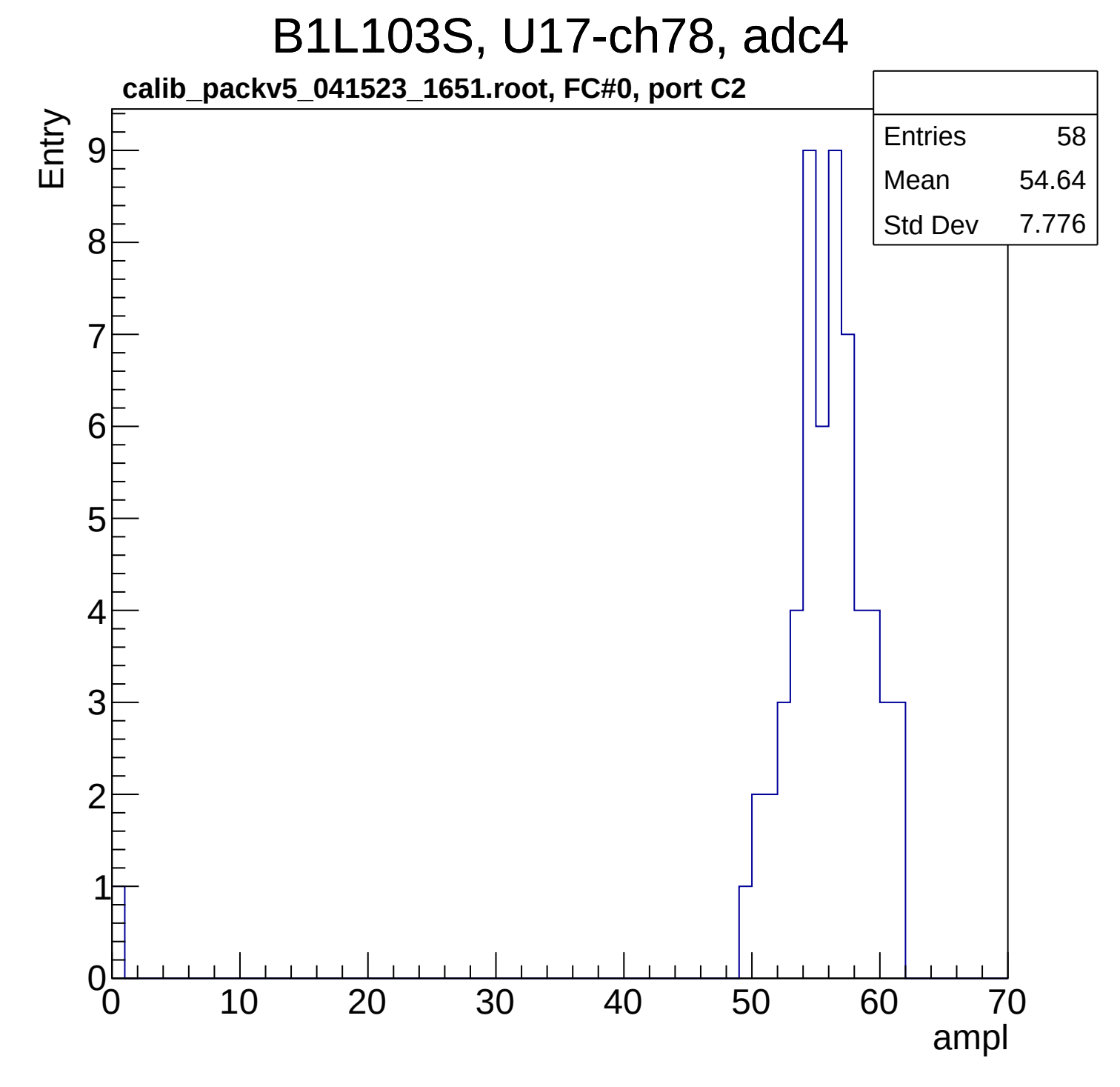

B1L103S, U17-ch77, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

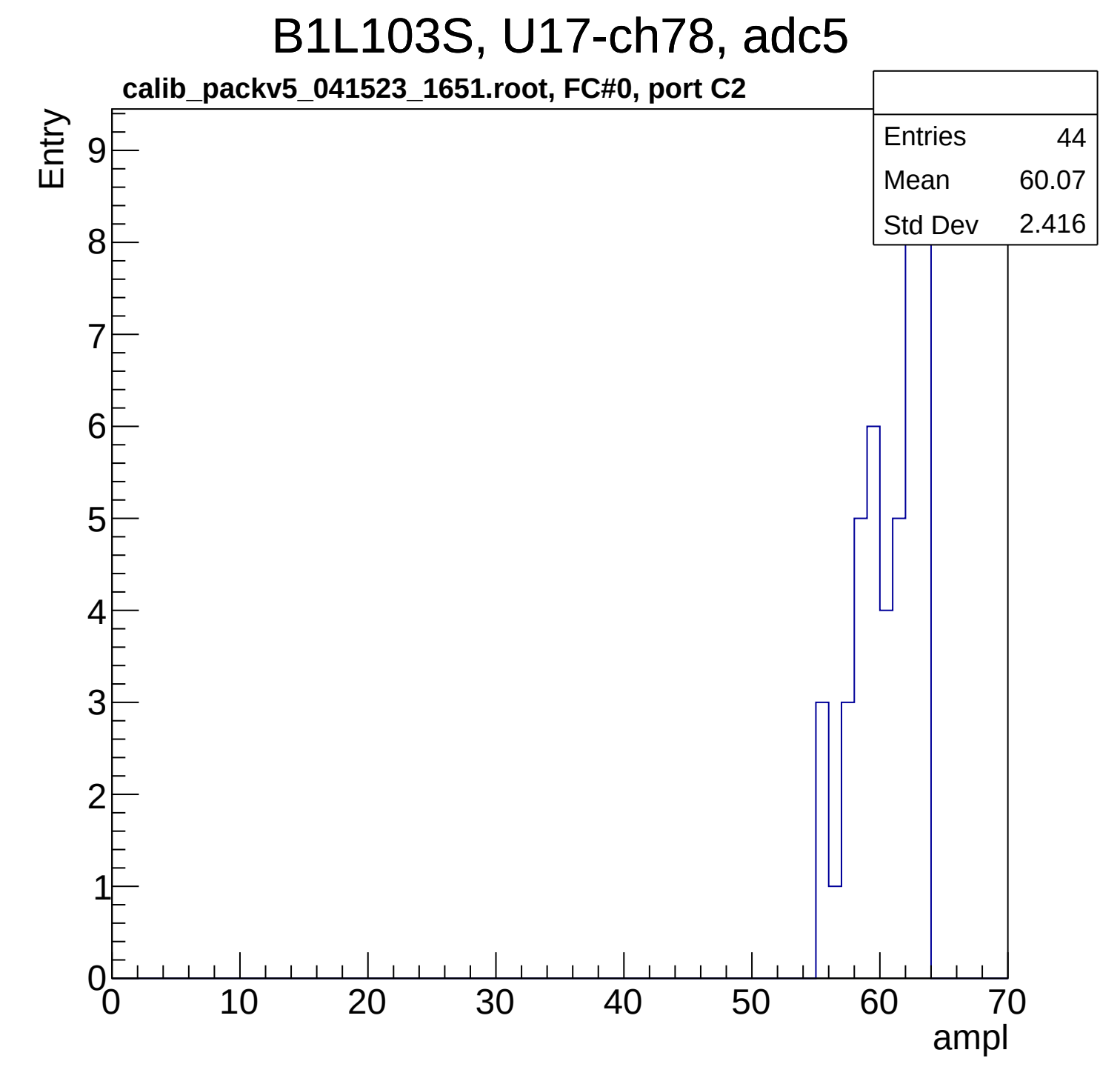

B1L103S, U17-ch78, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 115
Mean 24.99
Std Dev 11.14
Gaus mean : 29.6794
Gaus Width: 4.6055
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

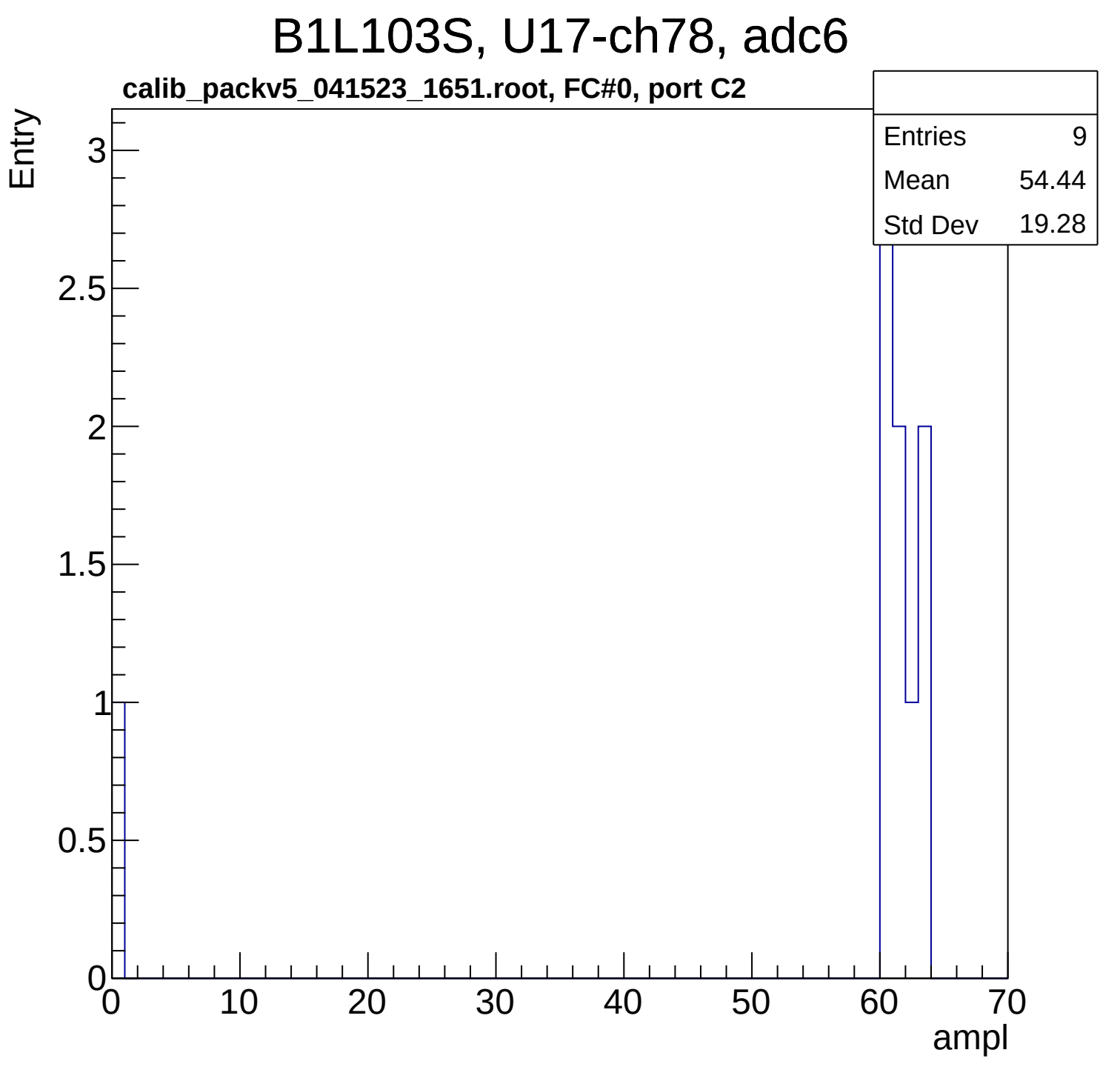

B1L103S, U17-ch78, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 38
Std Dev 3.89
Gaus mean : 39.0888
Gaus Width: 4.0931
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

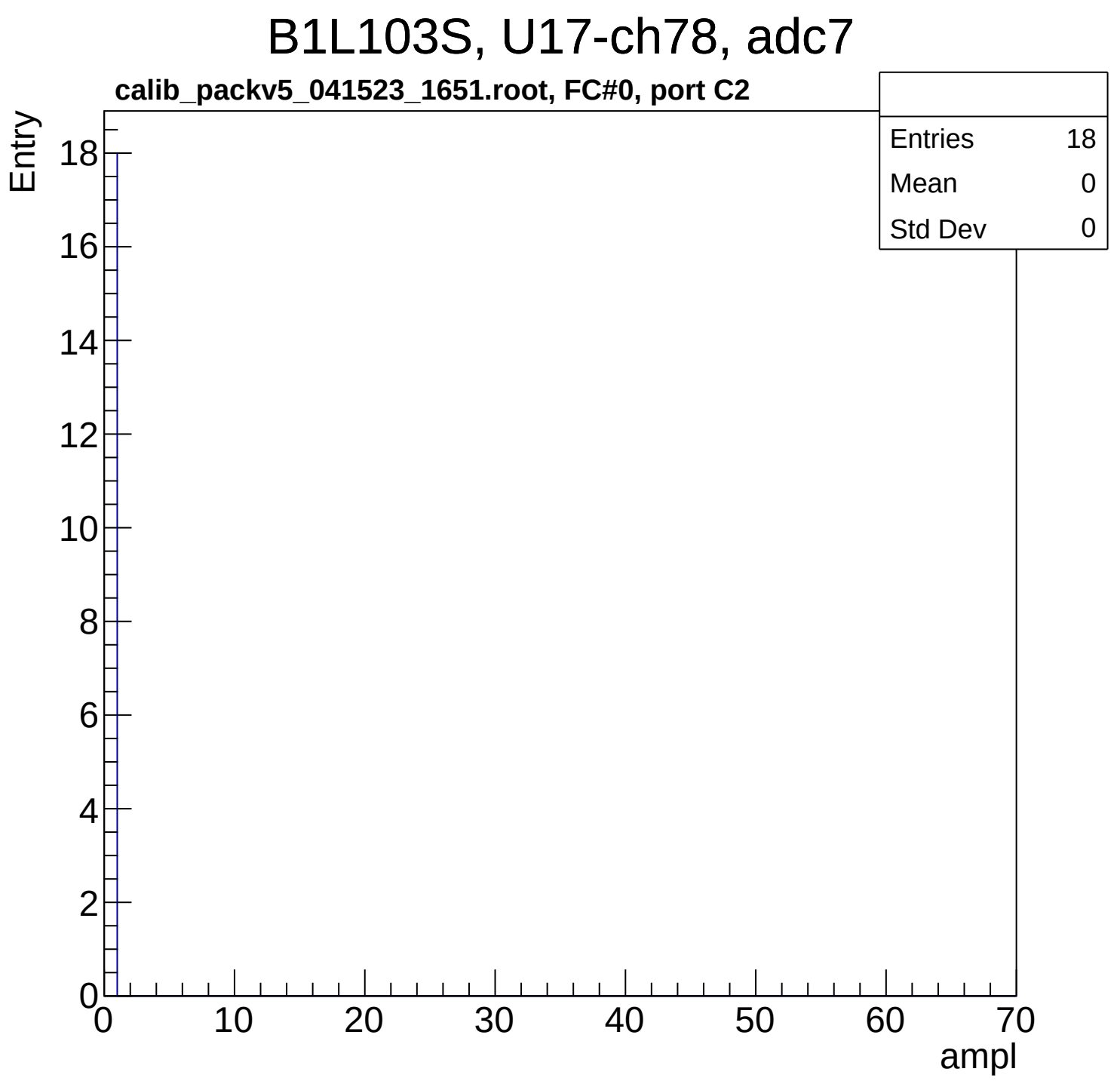

B1L103S, U17-ch78, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 42.29
Std Dev 9.302
Gaus mean : 43.8850
Gaus Width: 4.5475
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

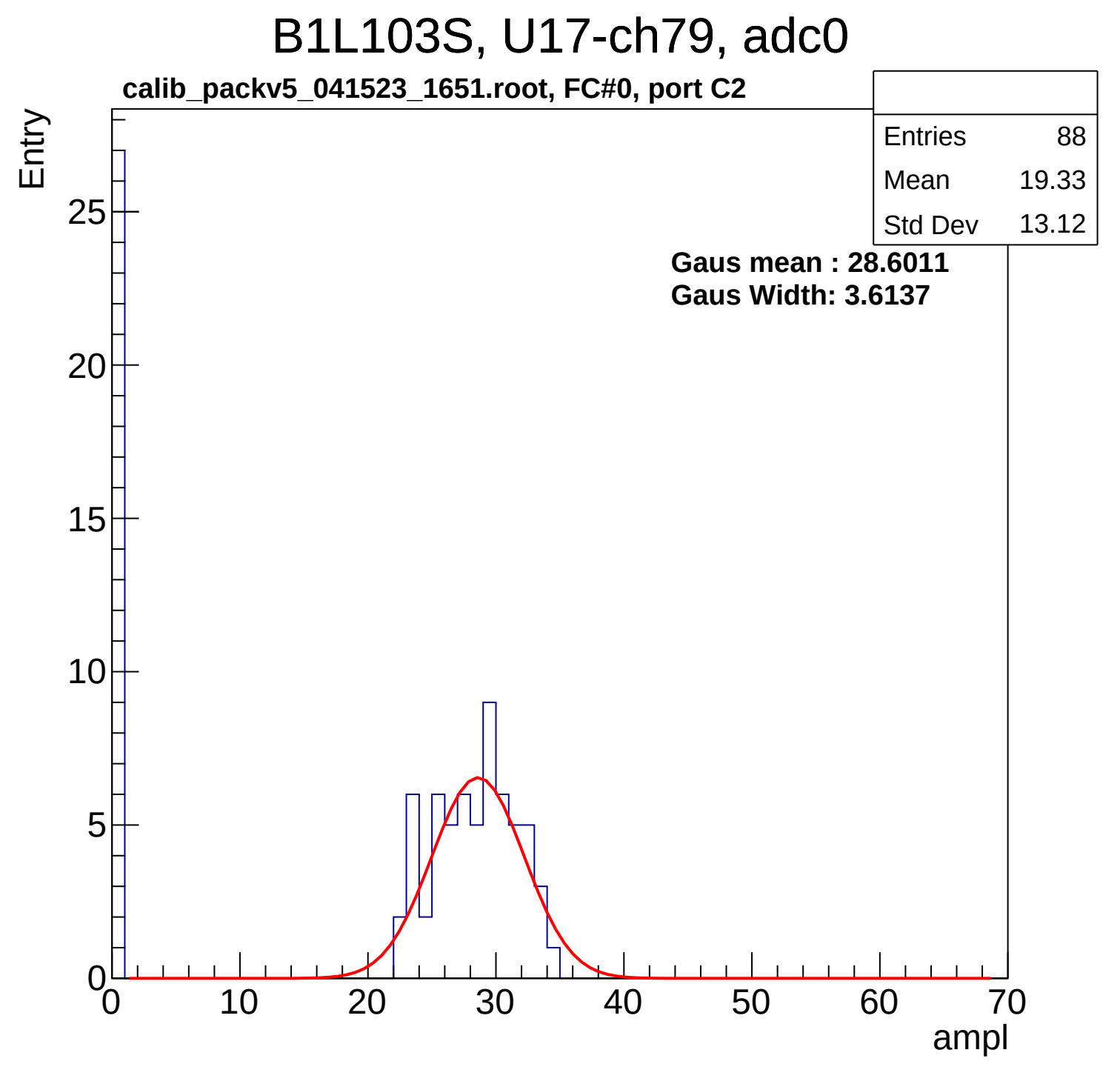

B1L103S, U17-ch78, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 41.03
Std Dev 18.57
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

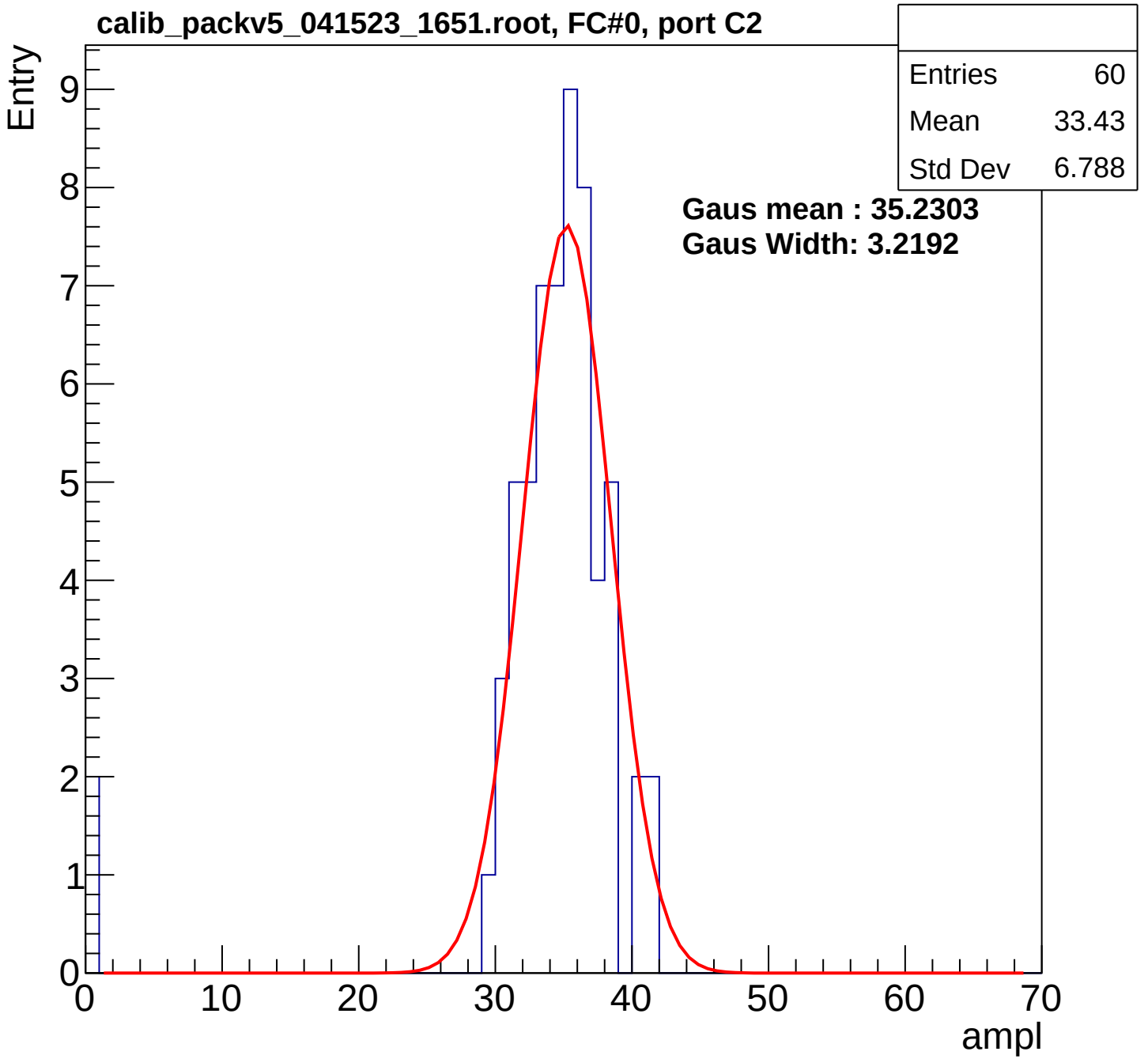

B1L103S, U17-ch78, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 54.64
Std Dev 7.776
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

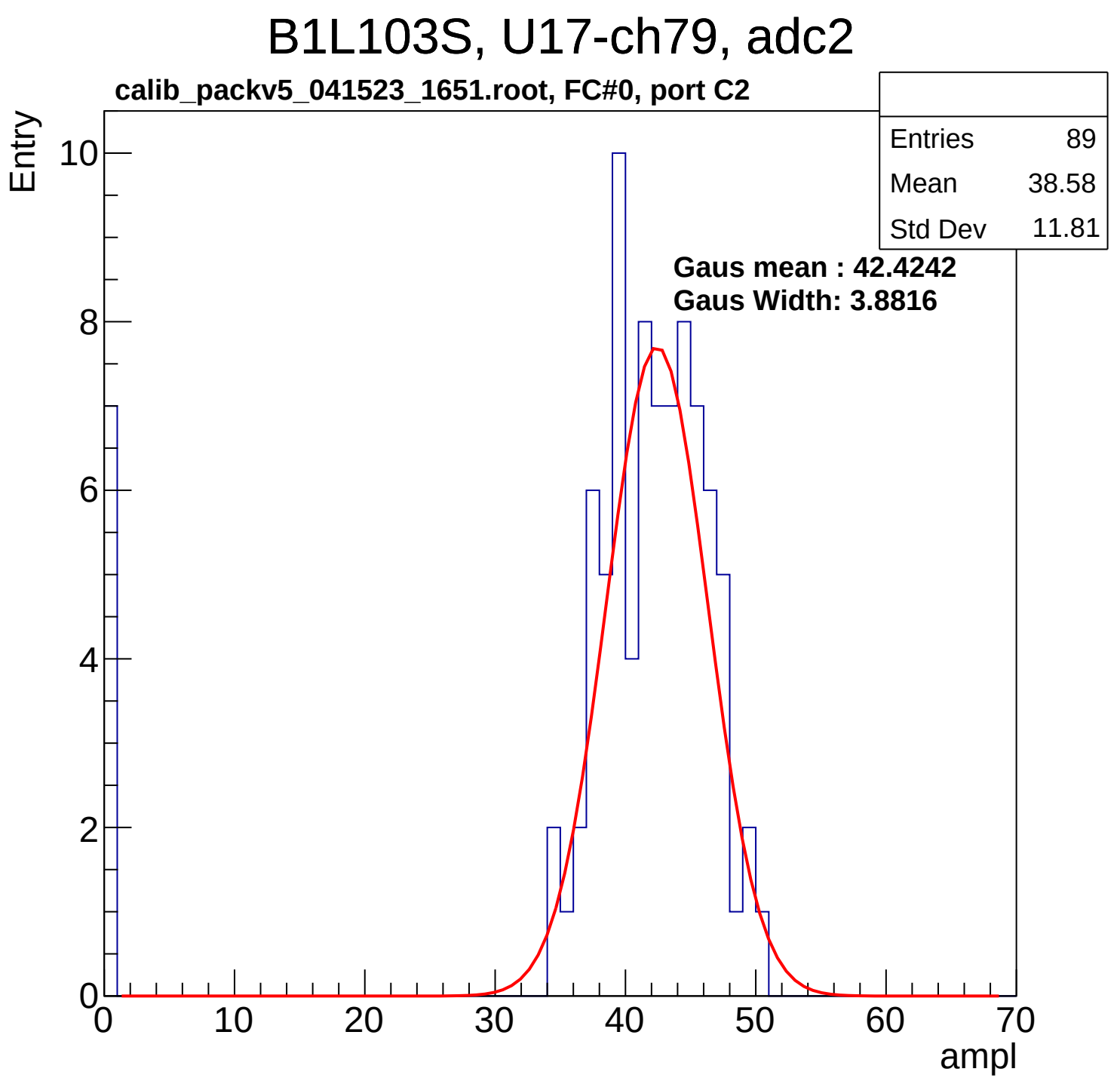

B1L103S, U17-ch78, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 60.07
Std Dev 2.416
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

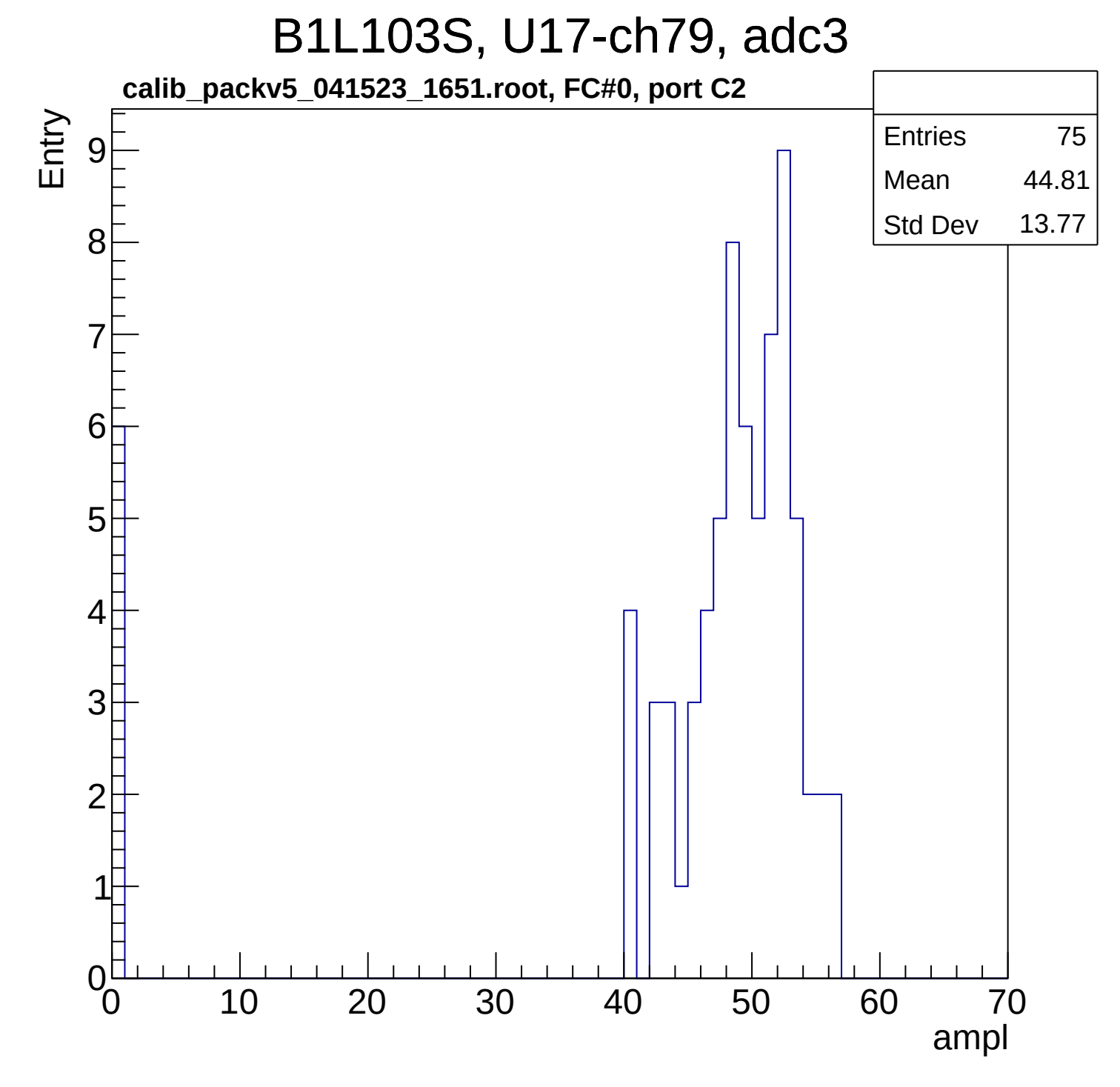

B1L103S, U17-ch78, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 54.44
Std Dev 19.28
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

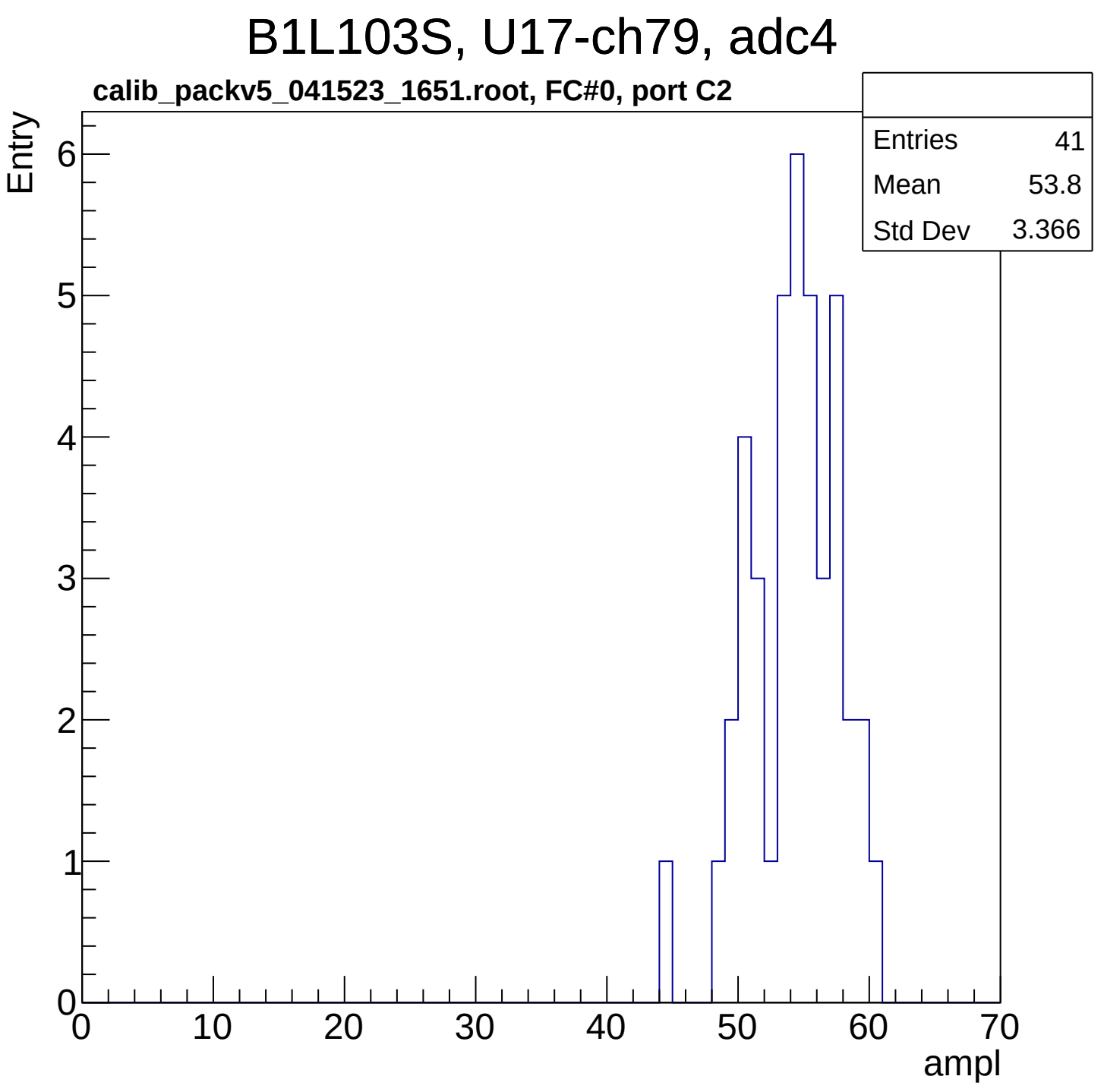

B1L103S, U17-ch78, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

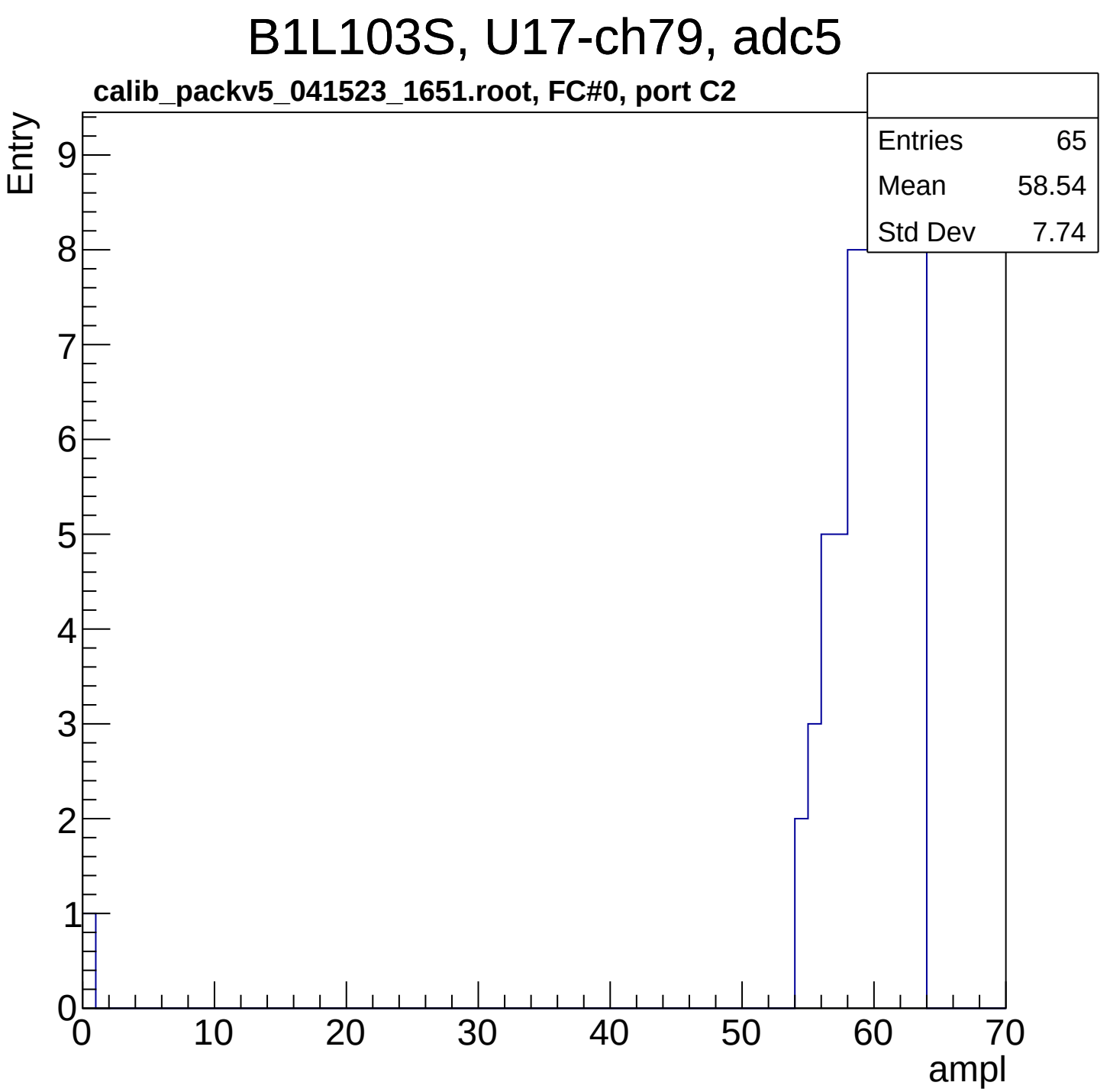

B1L103S, U17-ch79, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 19.33
Std Dev 13.12
Gaus mean : 28.6011
Gaus Width: 3.6137
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70

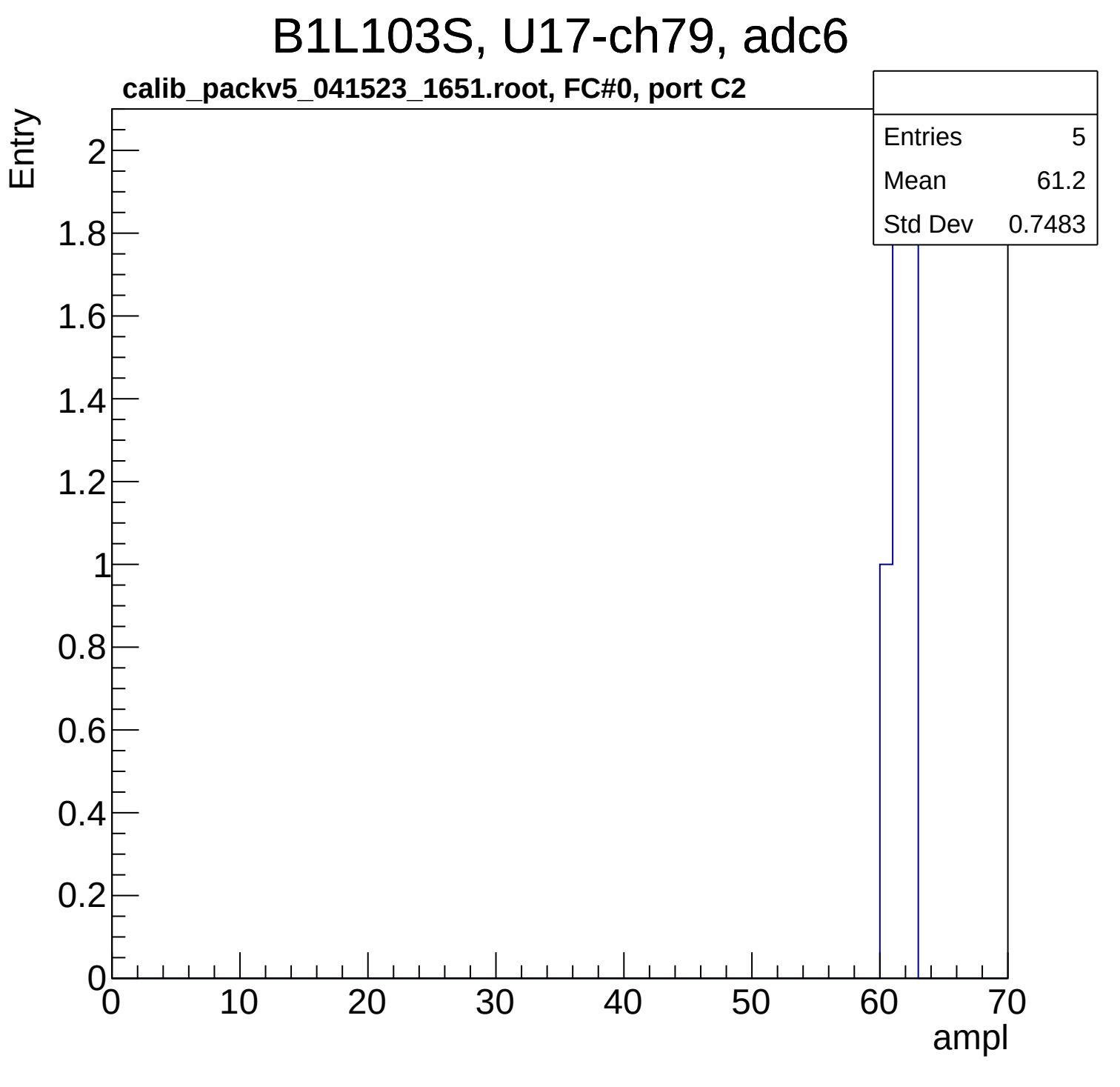

B1L103S, U17-ch79, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 33.43
Std Dev 6.788
Gaus mean : 35.2303
Gaus Width: 3.2192
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

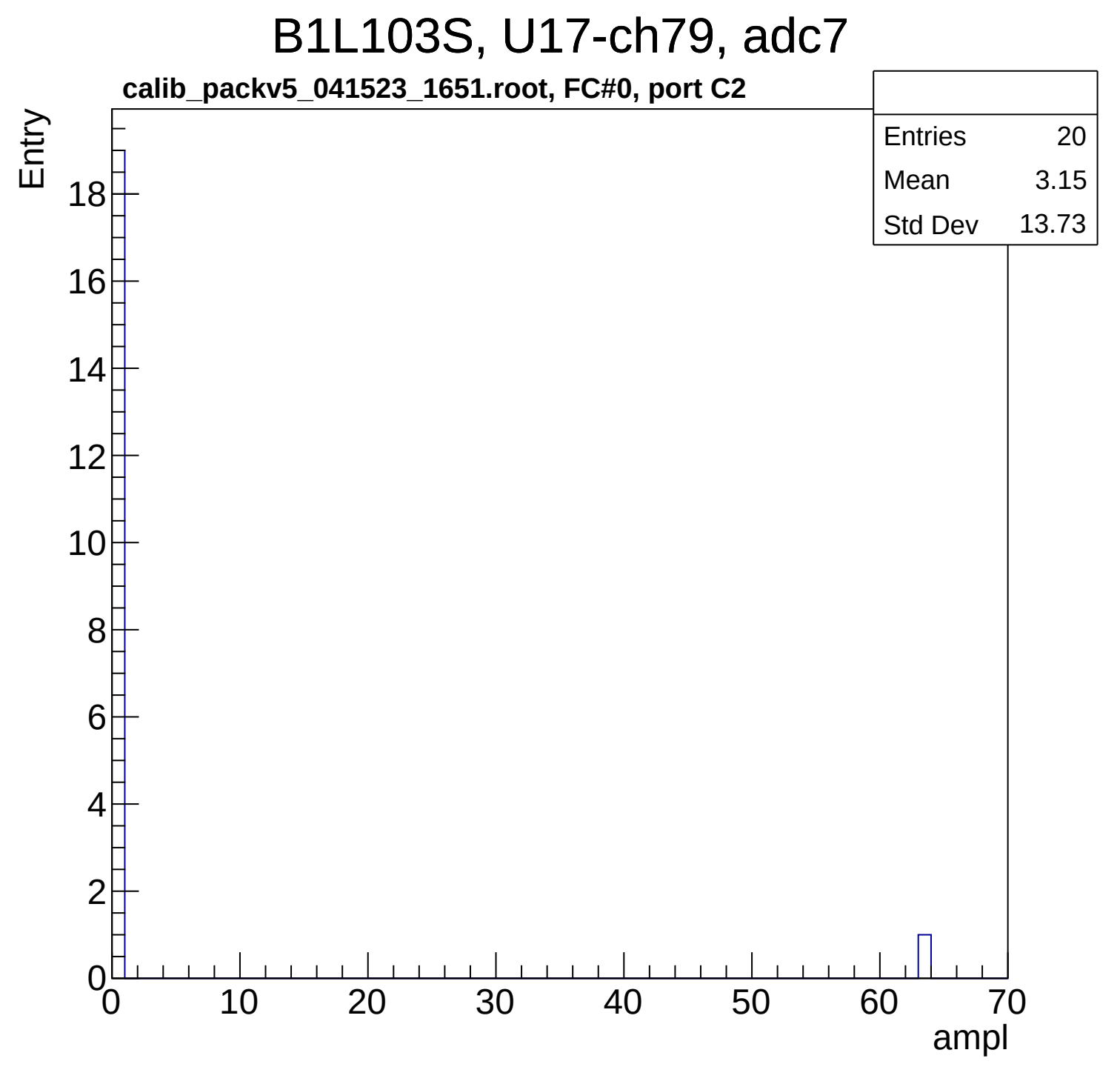

B1L103S, U17-ch79, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 38.58
Std Dev 11.81
Gaus mean : 42.4242
Gaus Width: 3.8816
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

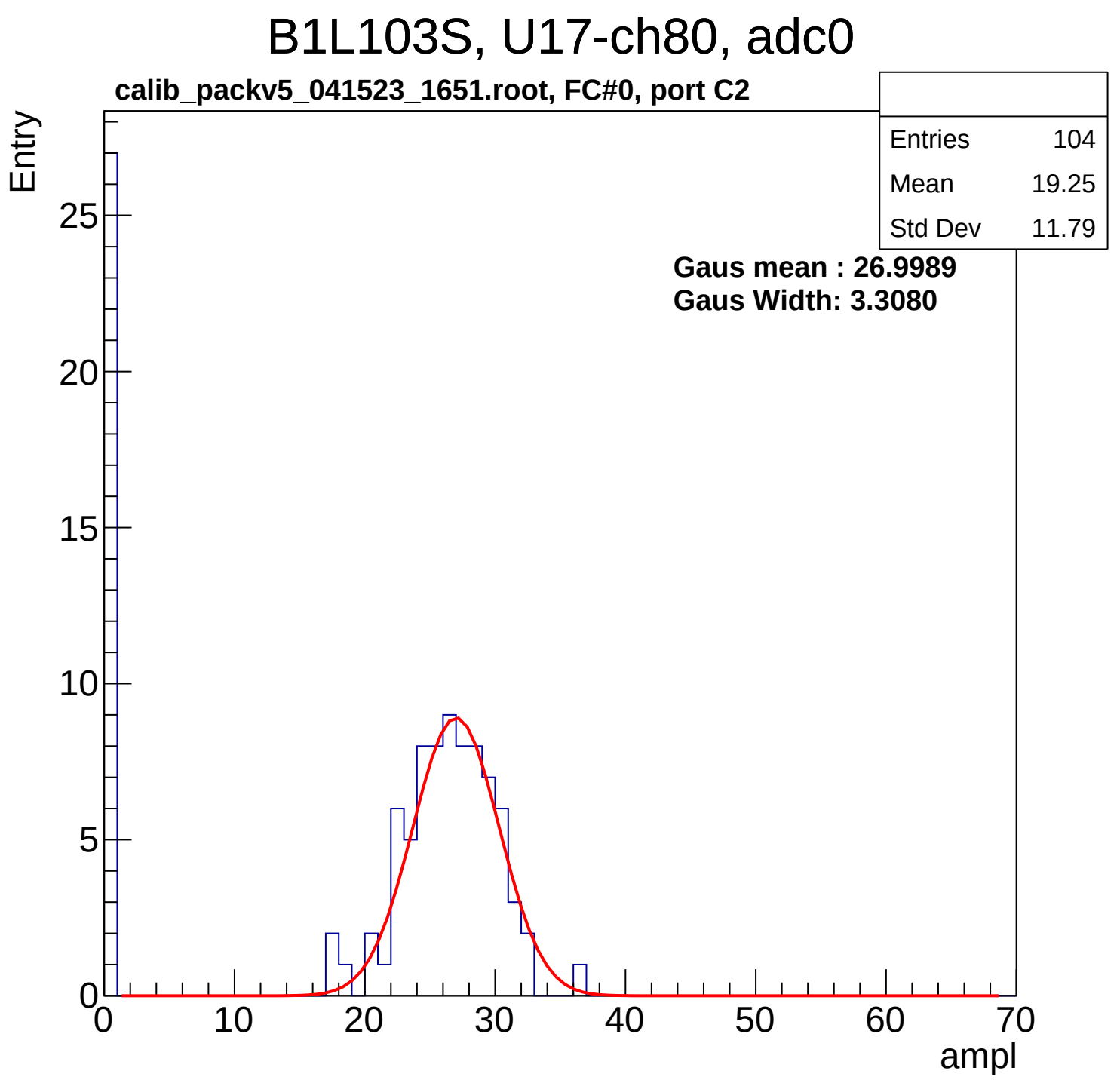

B1L103S, U17-ch79, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 44.81
Std Dev 13.77
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

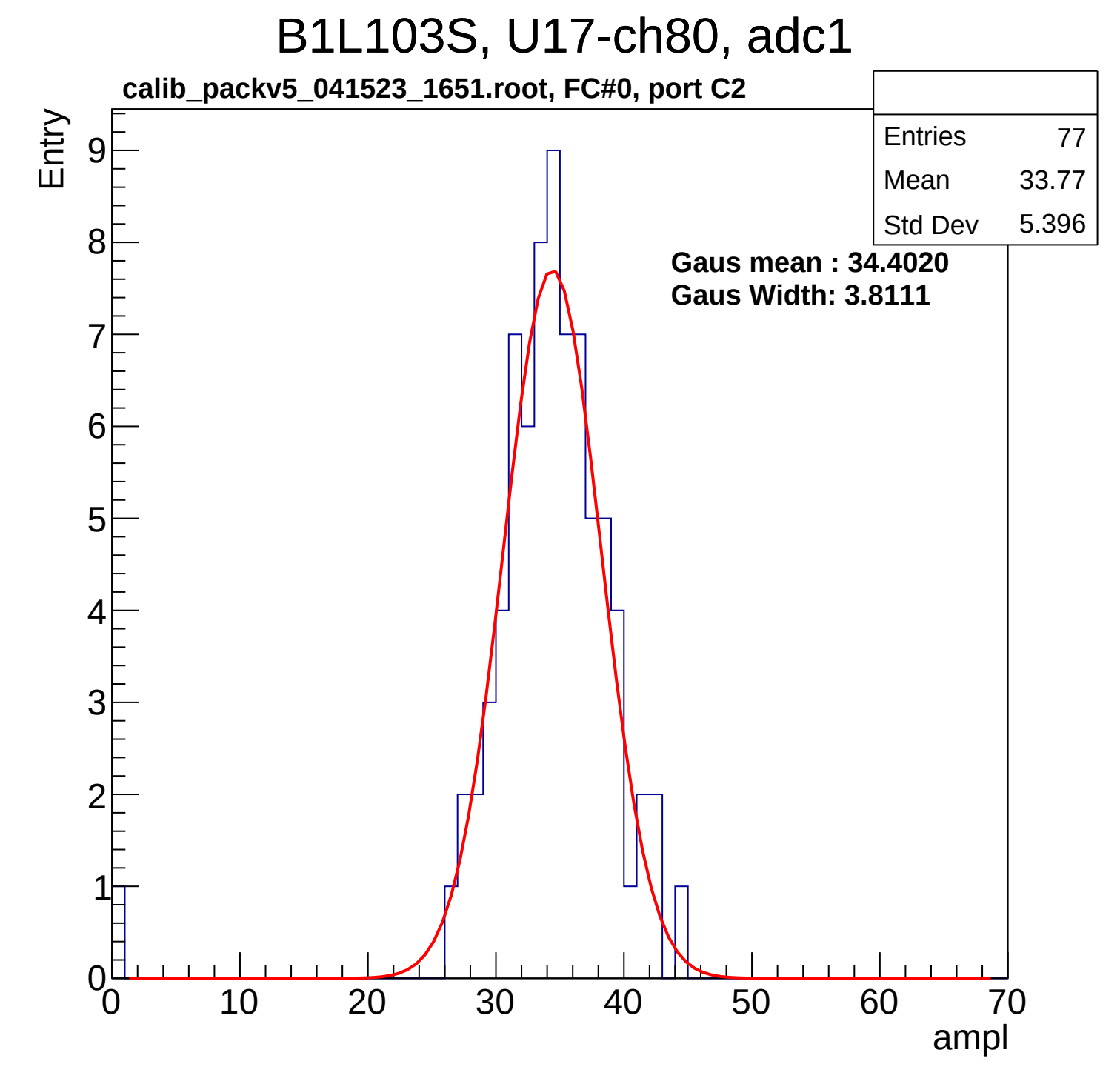

B1L103S, U17-ch79, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 53.8
Std Dev 3.366
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

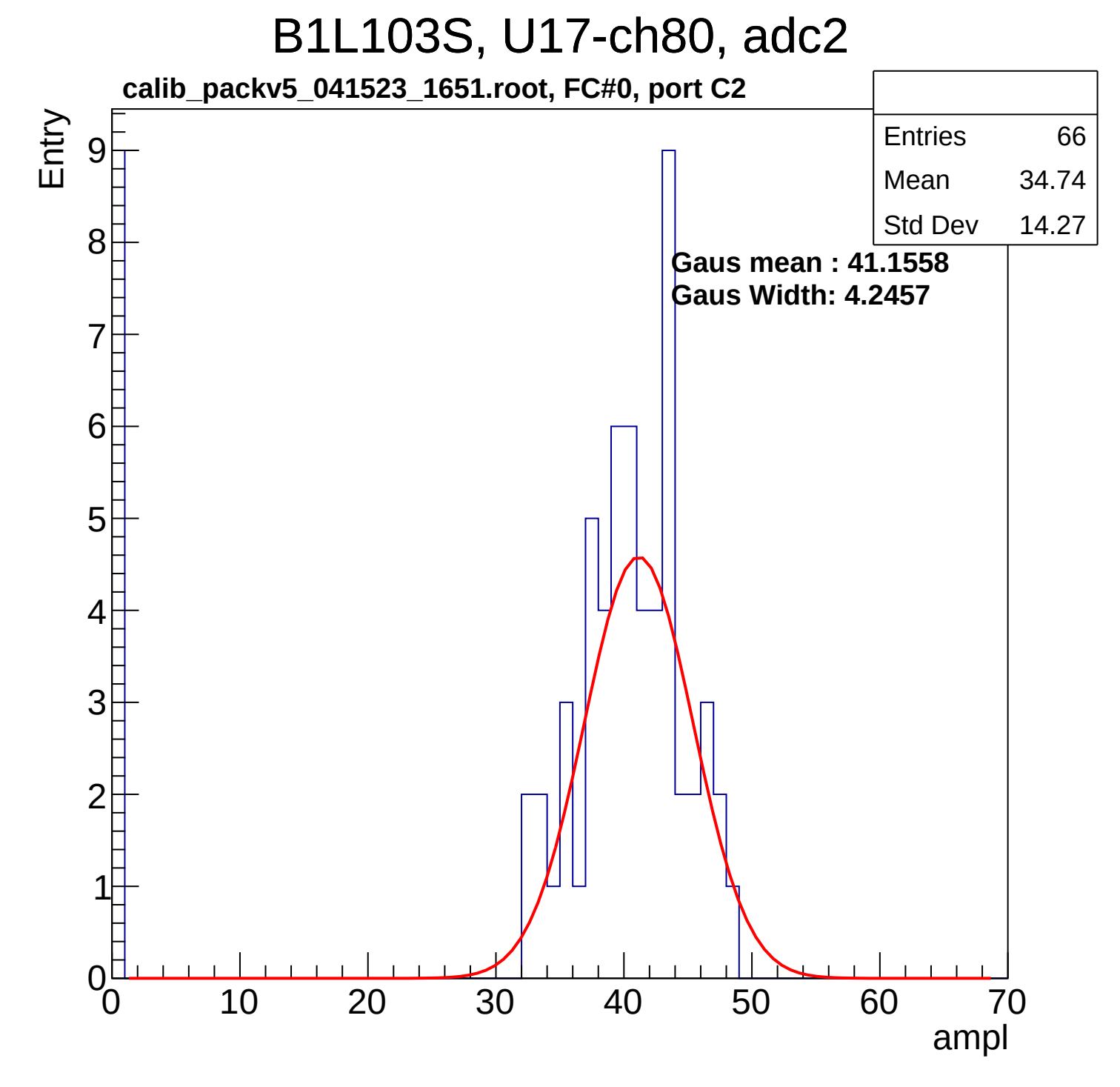

B1L103S, U17-ch79, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 58.54
Std Dev 7.74
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

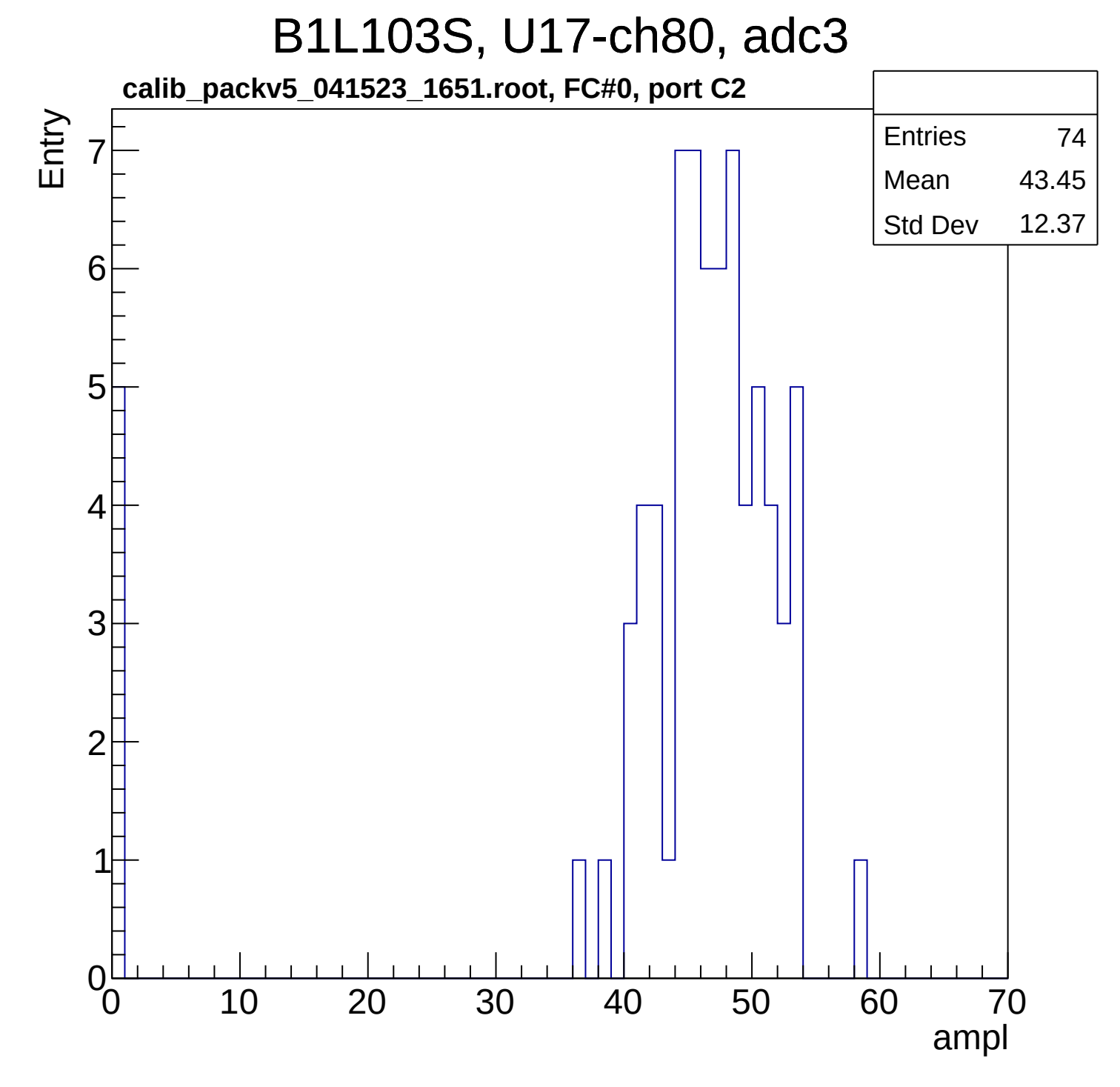

B1L103S, U17-ch79, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.2
Std Dev 0.7483
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

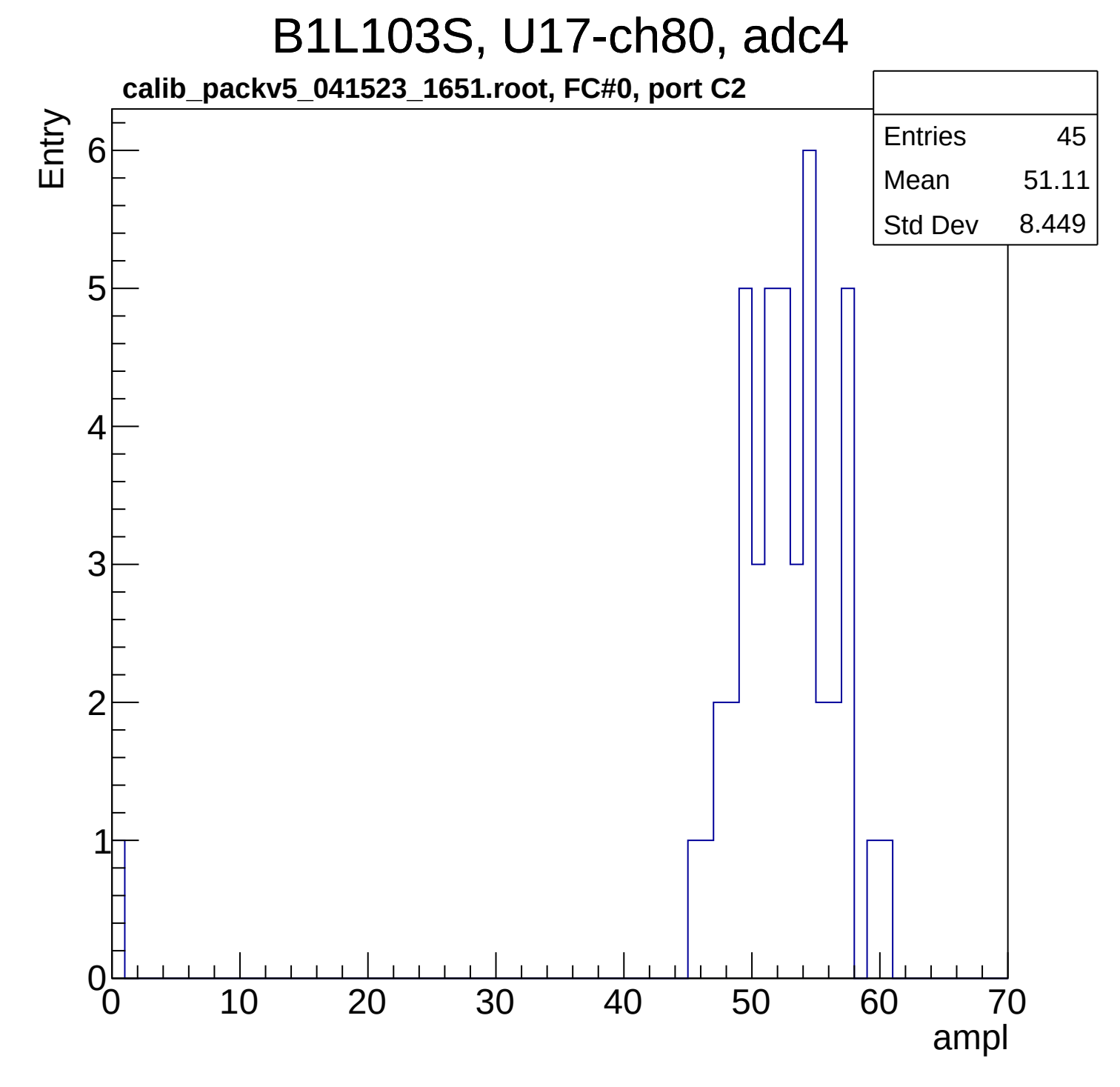

B1L103S, U17-ch79, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

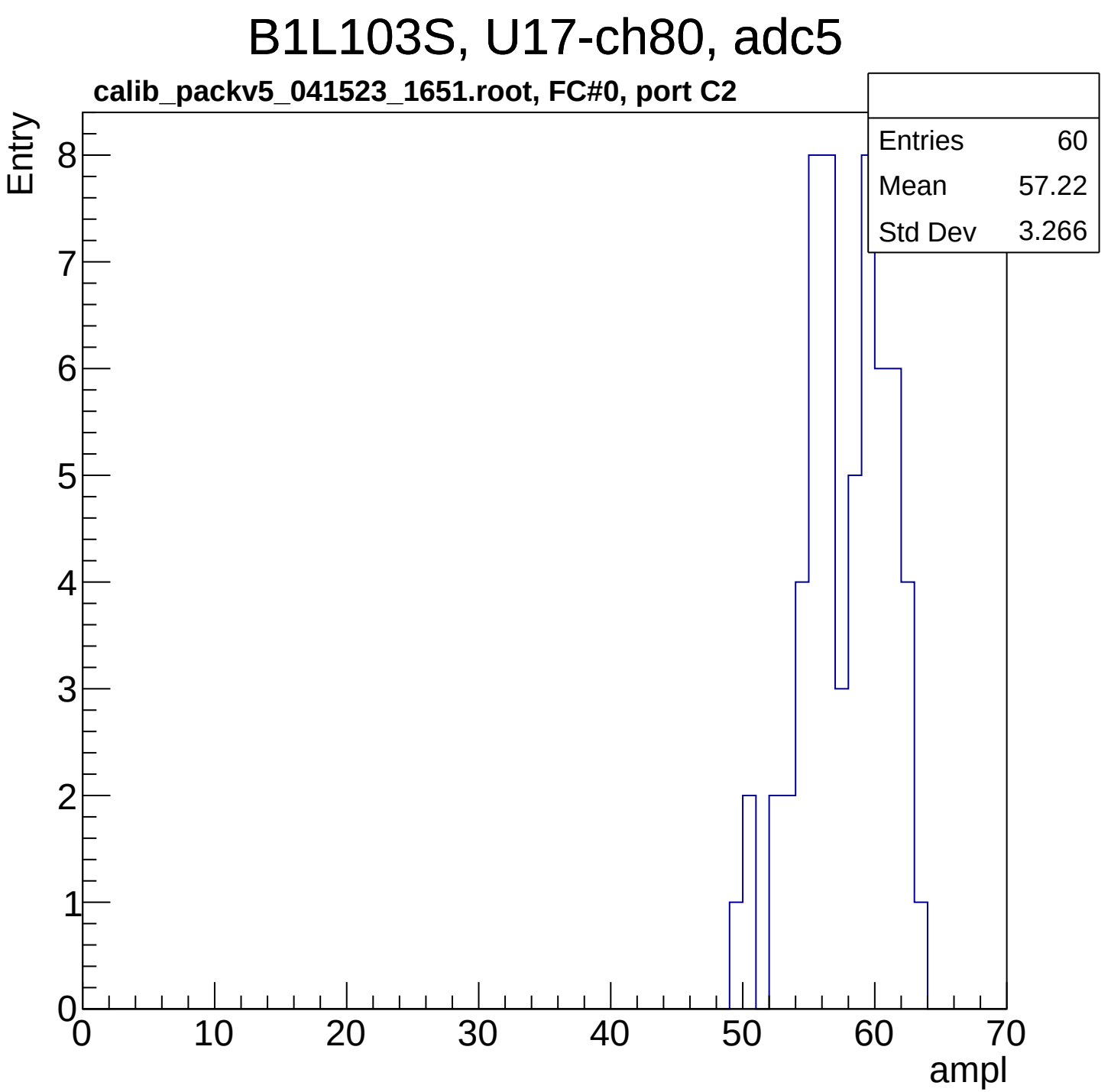

B1L103S, U17-ch80, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 19.25
Std Dev 11.79
Gaus mean : 26.9989
Gaus Width: 3.3080
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70

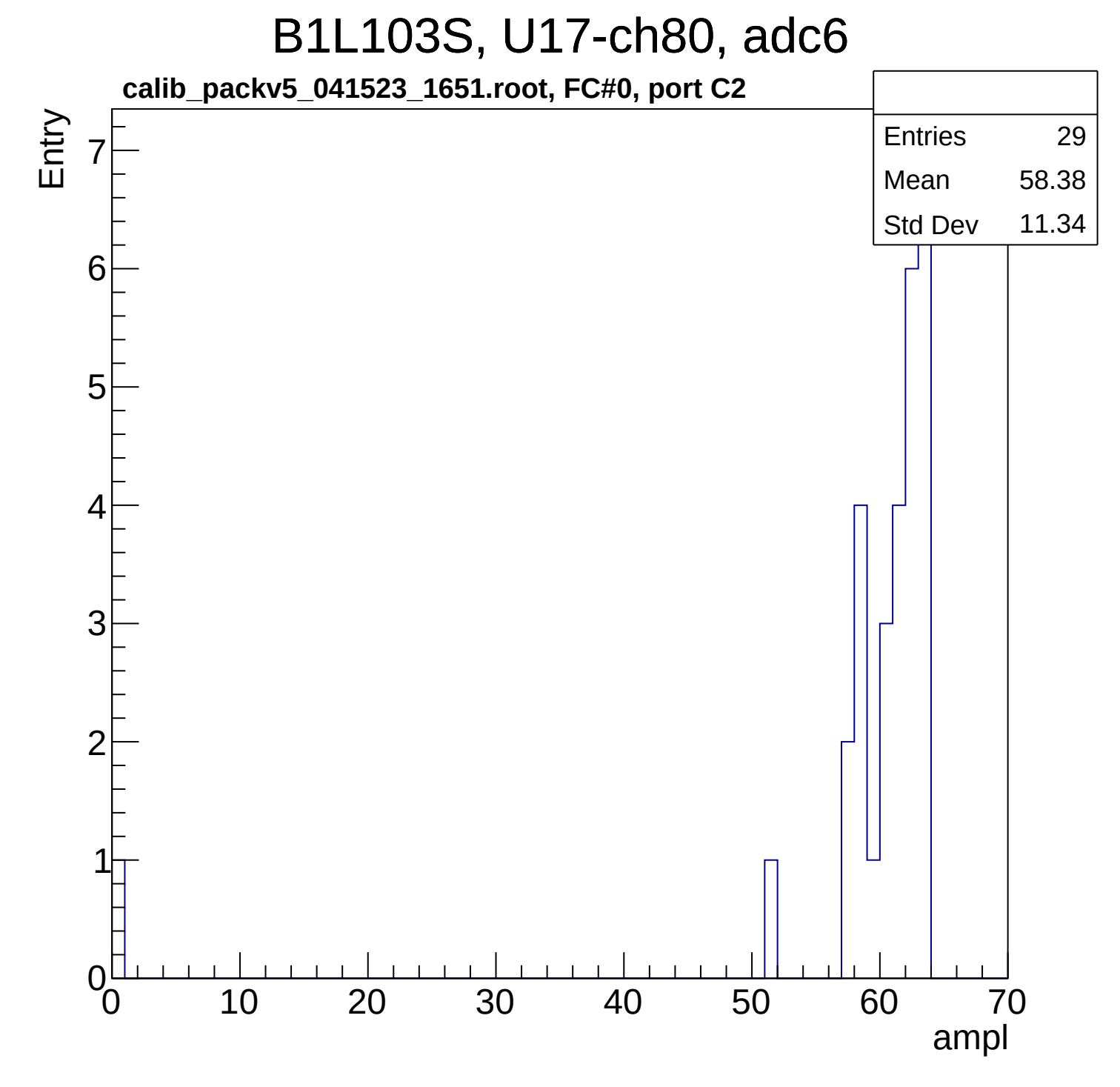

B1L103S, U17-ch80, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 33.77
Std Dev 5.396
Gaus mean : 34.4020
Gaus Width: 3.8111
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

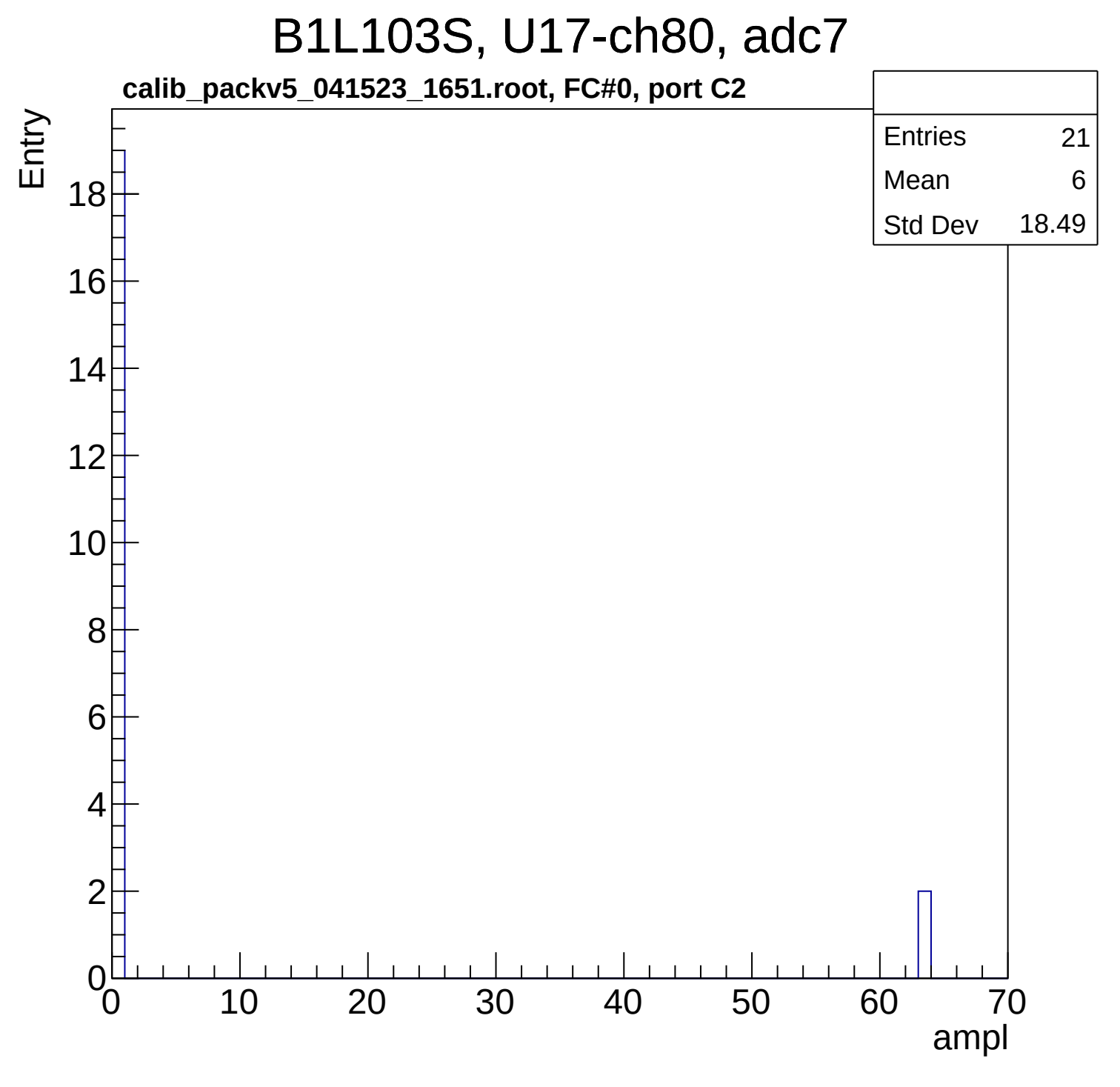

B1L103S, U17-ch80, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 34.74
Std Dev 14.27
Gaus mean : 41.1558
Gaus Width: 4.2457
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

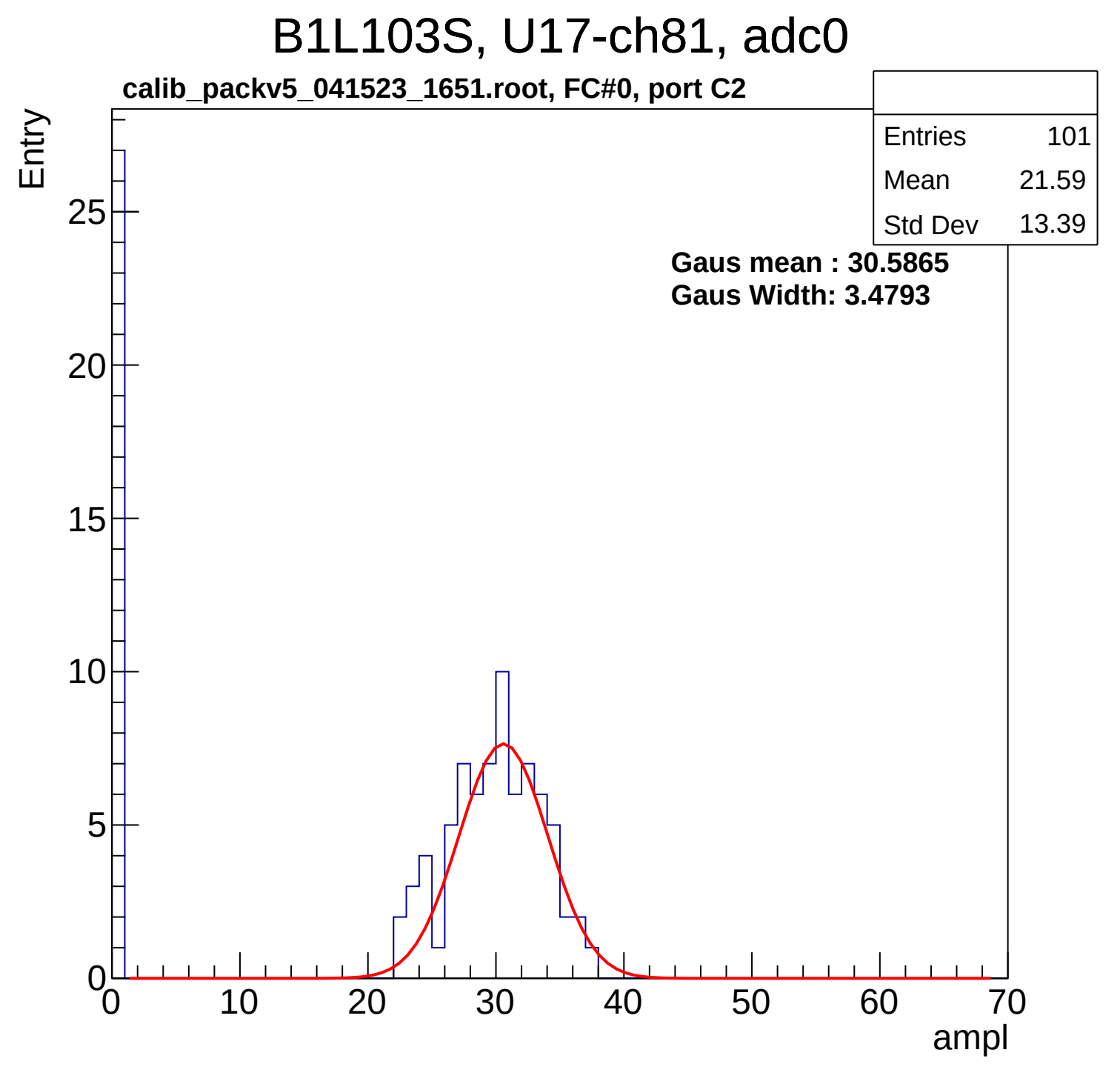

B1L103S, U17-ch80, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 43.45
Std Dev 12.37
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

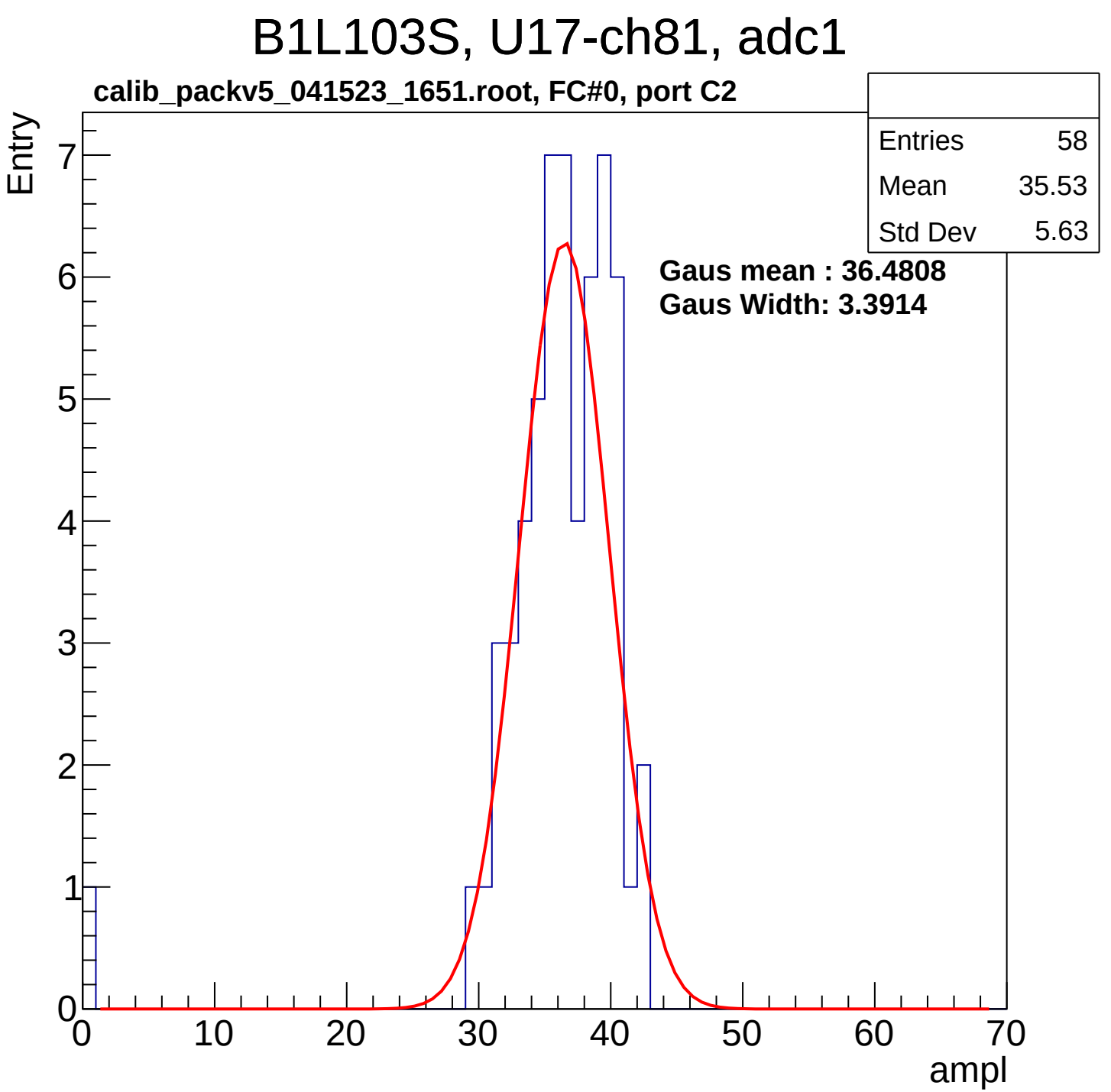

B1L103S, U17-ch80, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 51.11
Std Dev 8.449
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

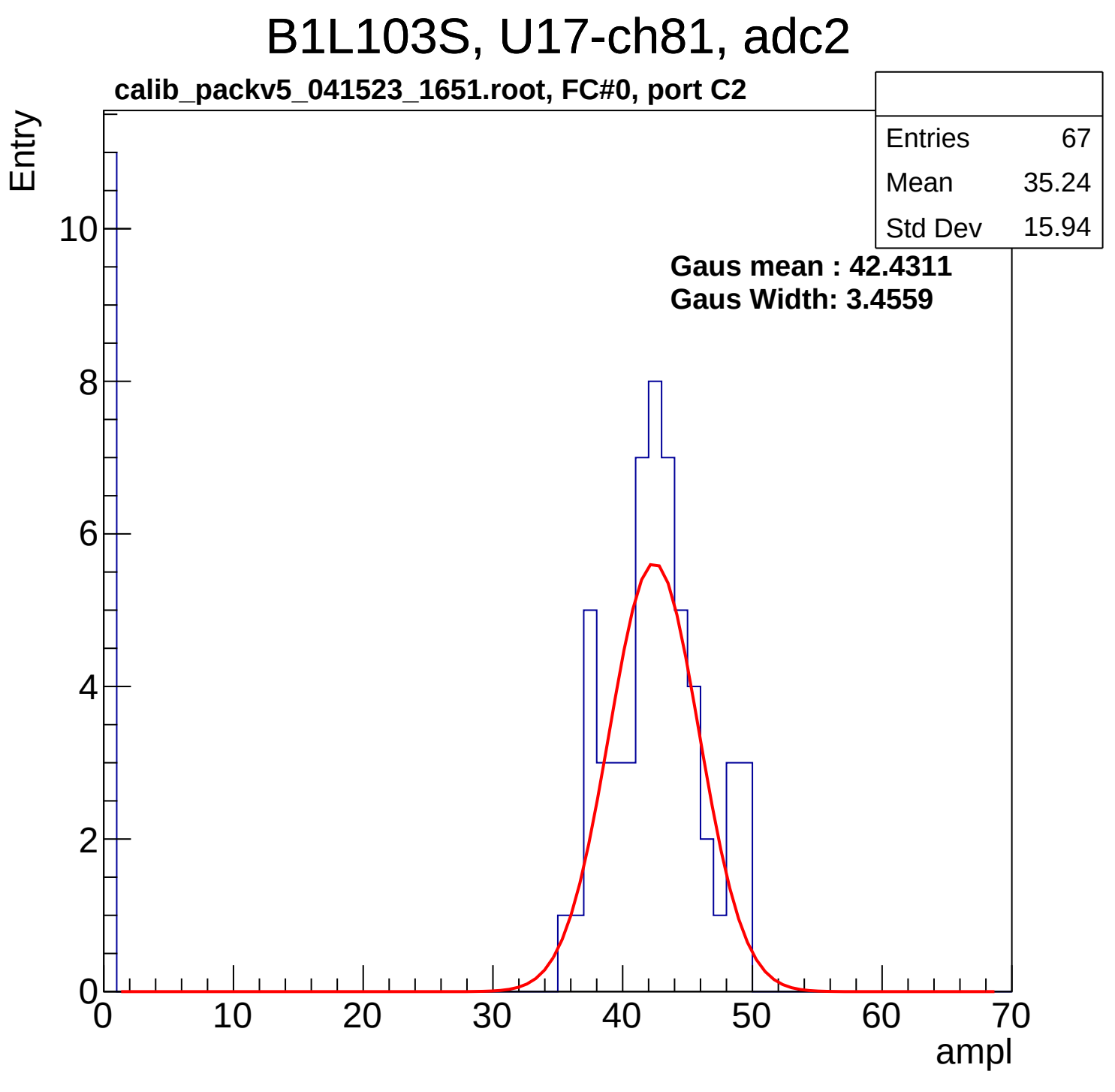

B1L103S, U17-ch80, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 57.22
Std Dev 3.266
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

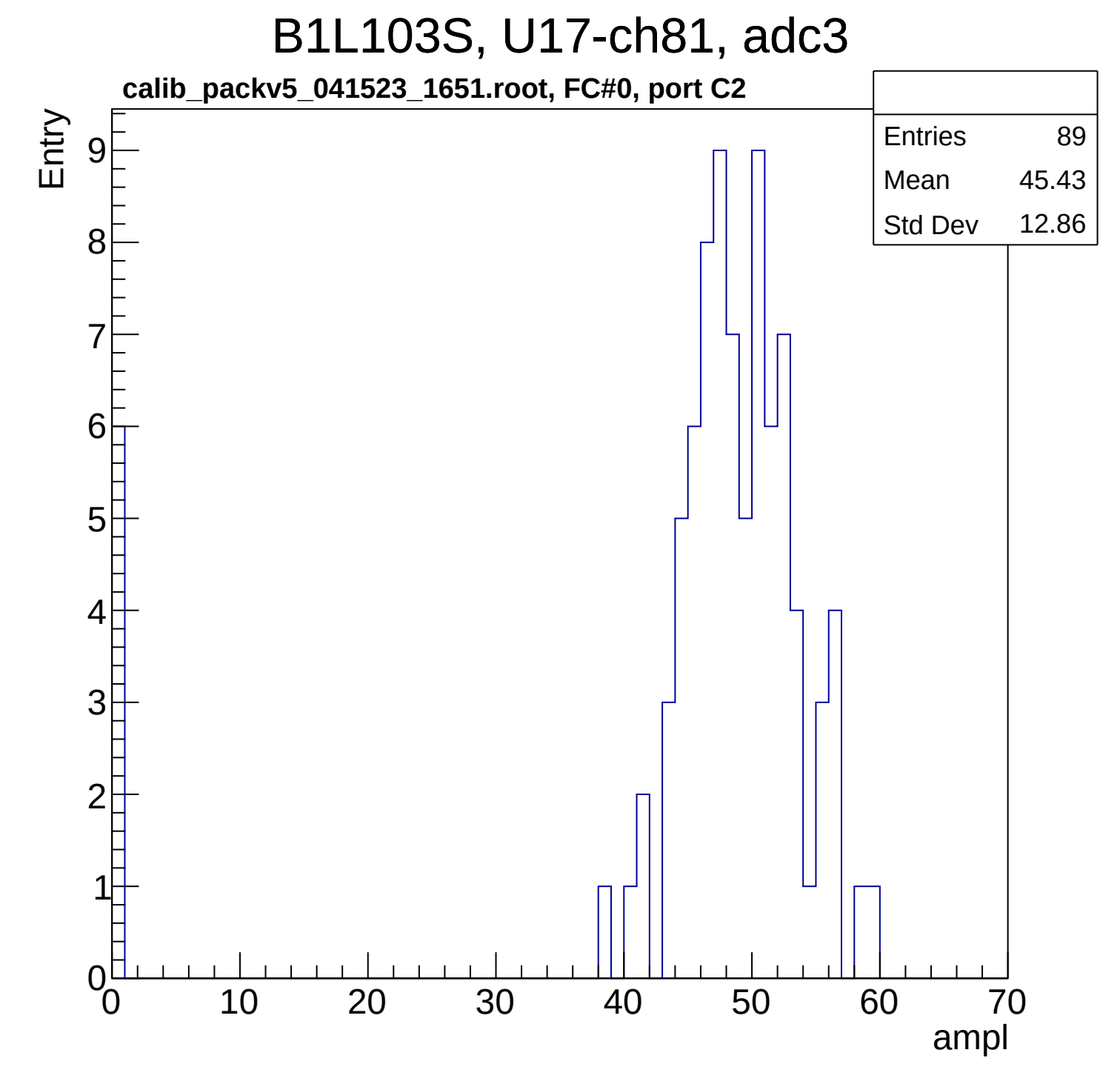

B1L103S, U17-ch80, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 58.38
Std Dev 11.34
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

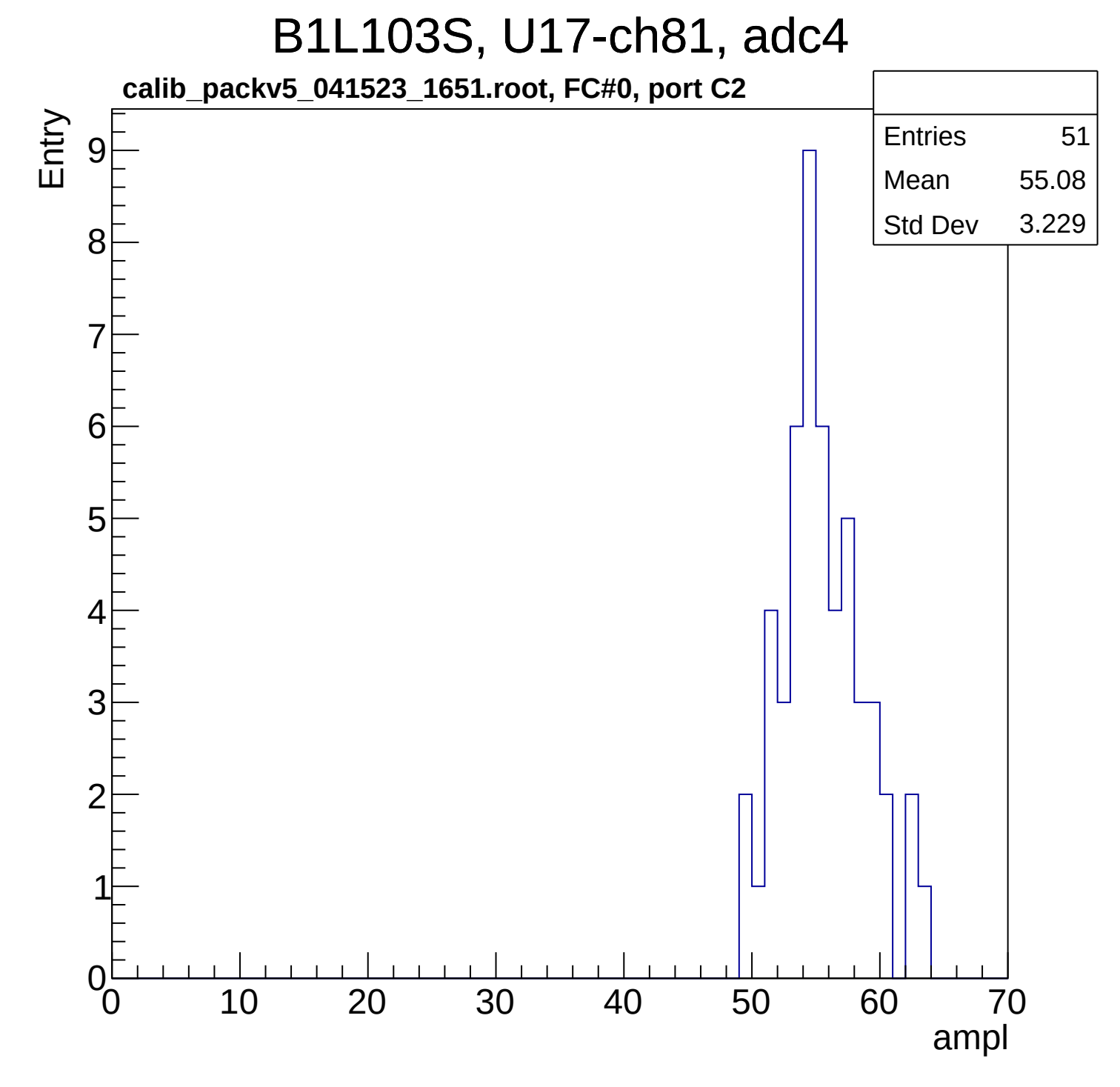

B1L103S, U17-ch80, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

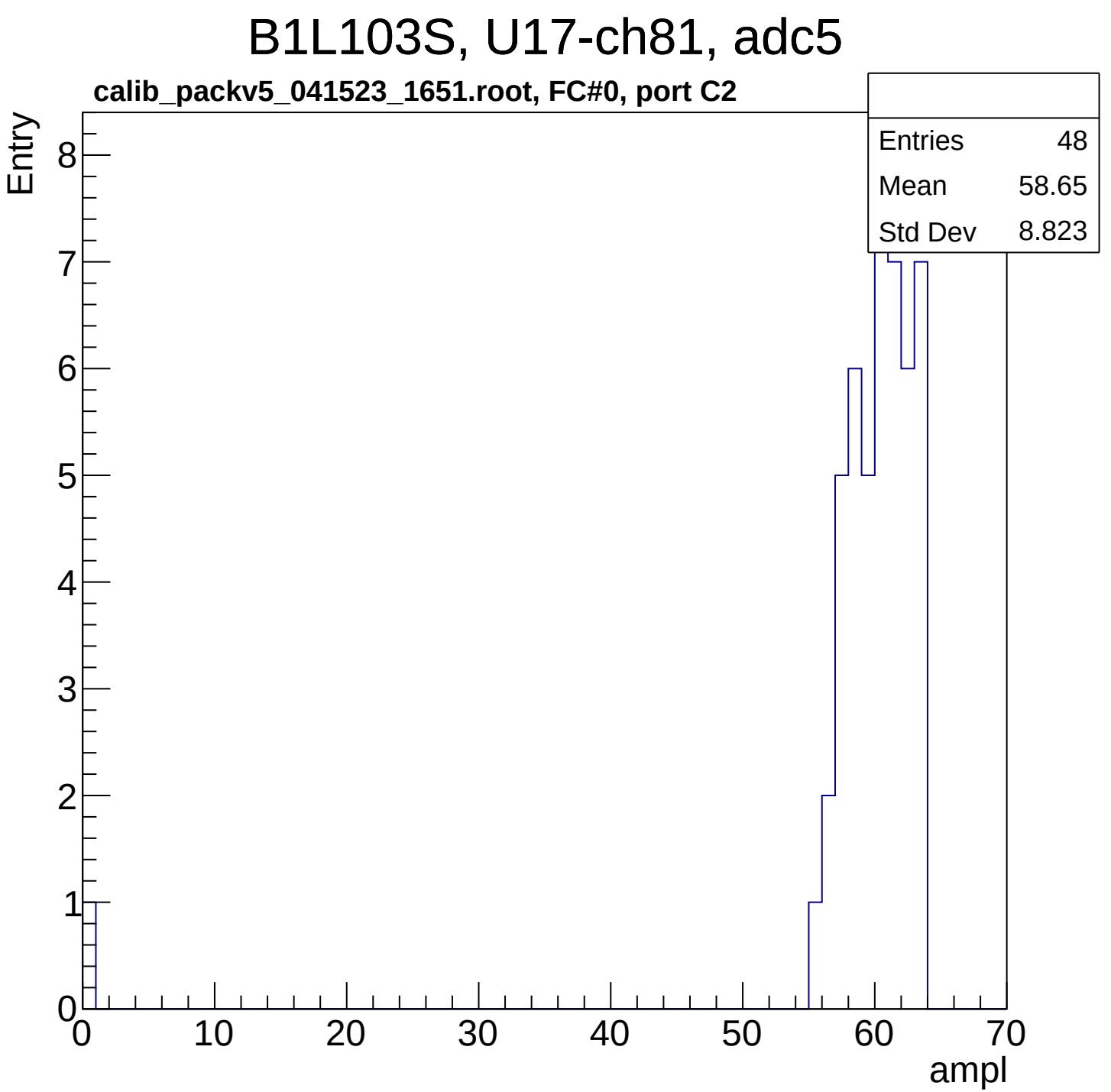

B1L103S, U17-ch81, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 21.59
Std Dev 13.39
Gaus mean : 30.5865
Gaus Width: 3.4793
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70

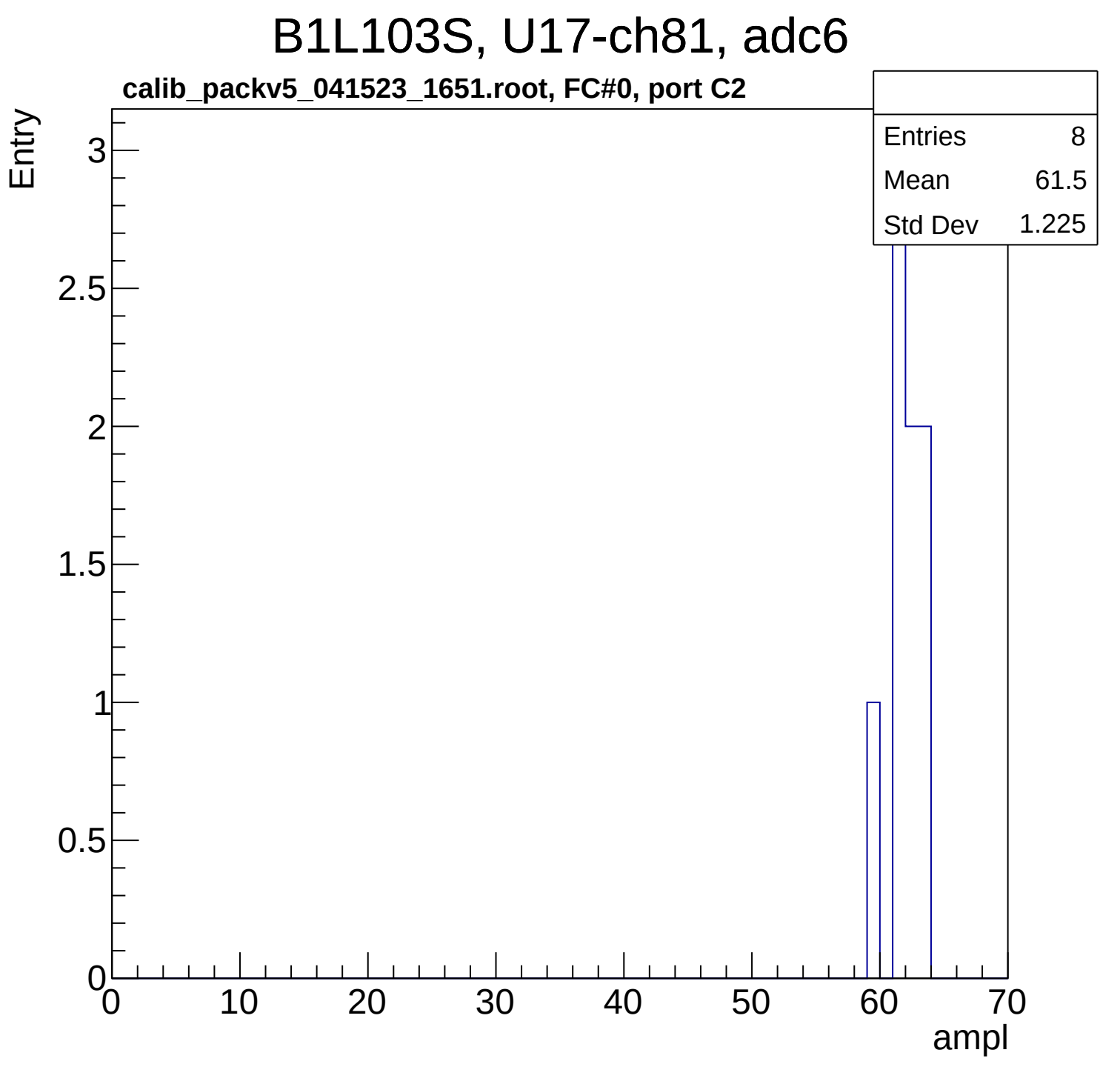

B1L103S, U17-ch81, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 35.53
Std Dev 5.63
Gaus mean : 36.4808
Gaus Width: 3.3914
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

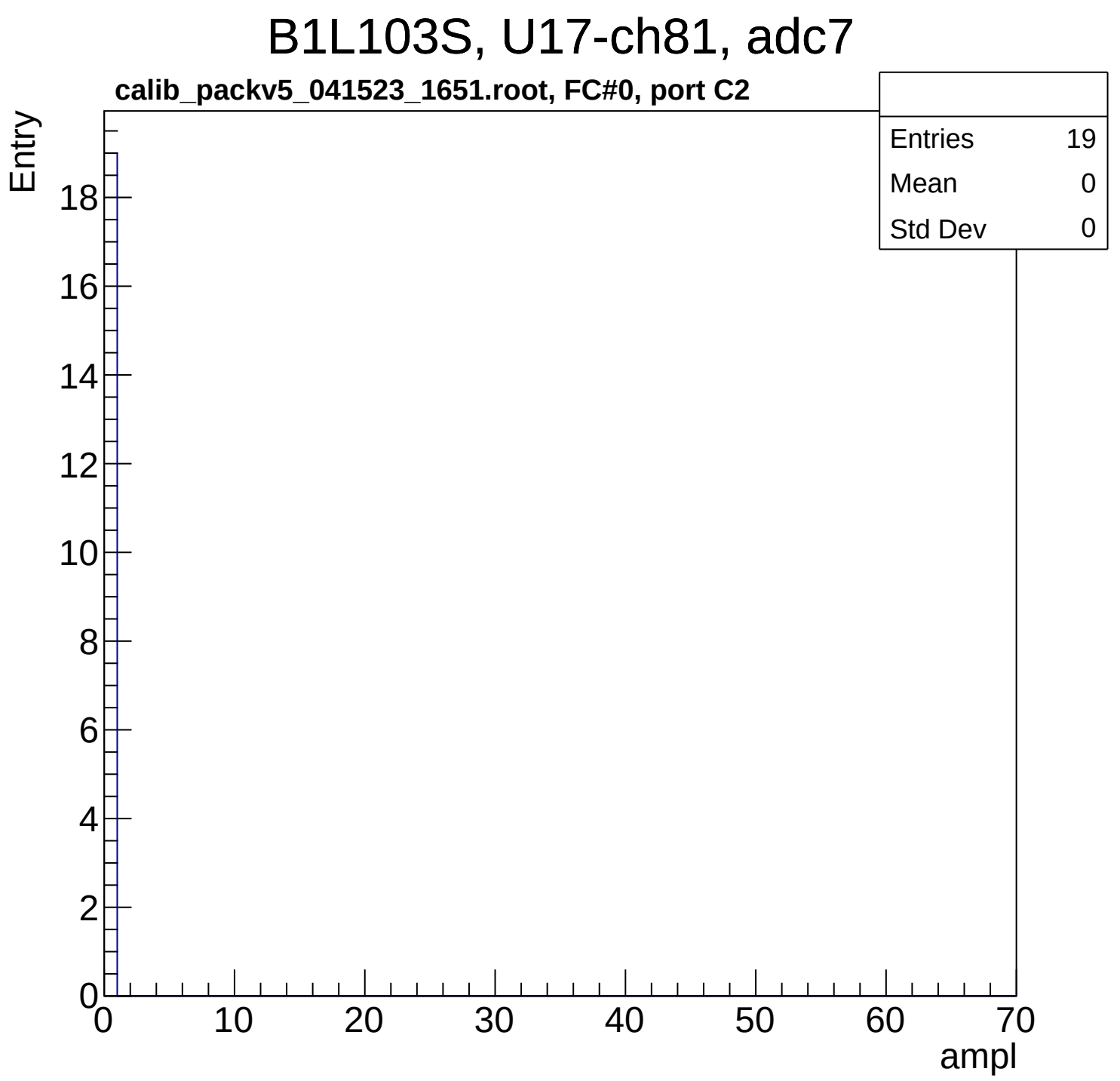

B1L103S, U17-ch81, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 35.24
Std Dev 15.94
Gaus mean : 42.4311
Gaus Width: 3.4559
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

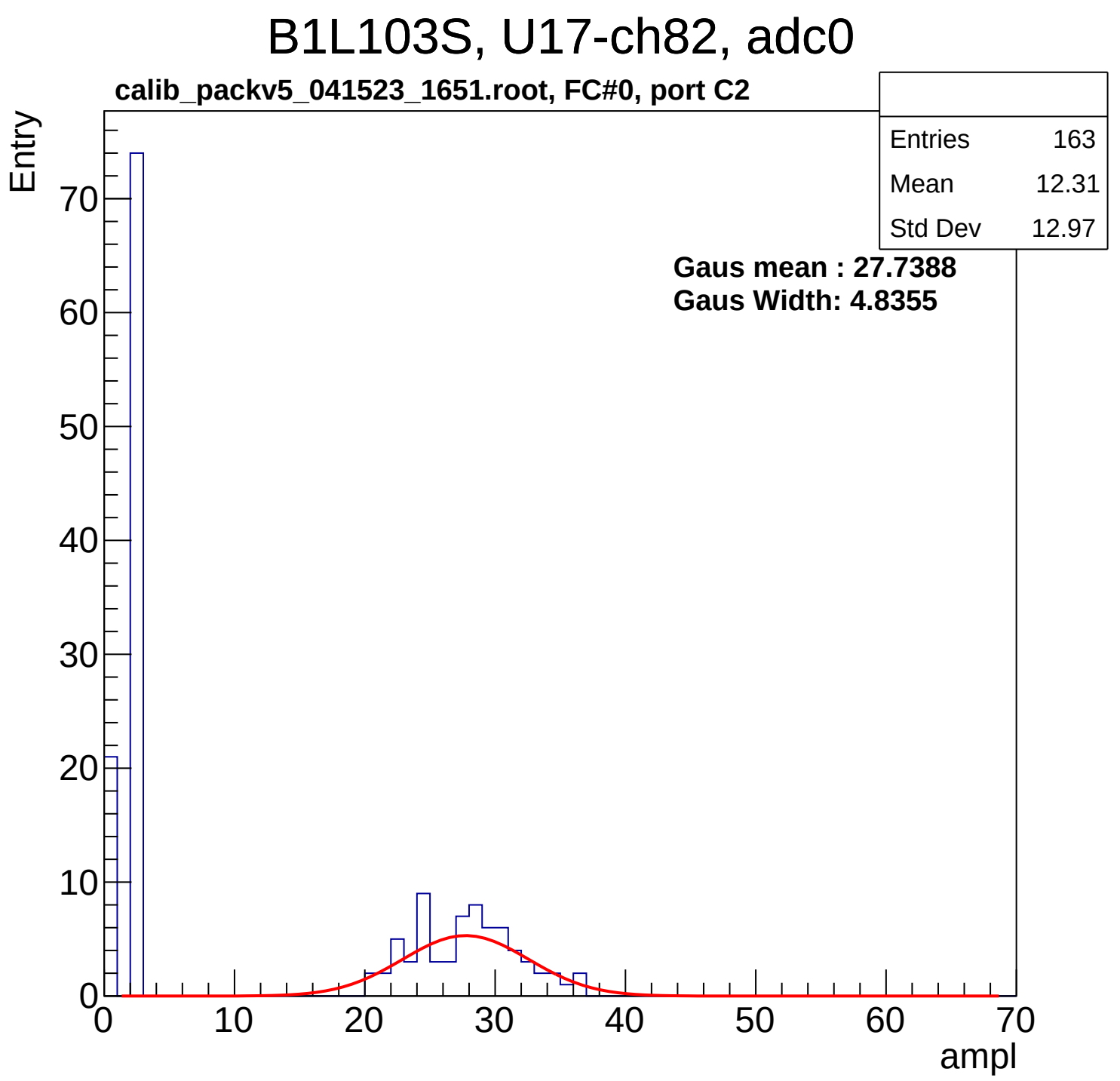

B1L103S, U17-ch81, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 45.43
Std Dev 12.86
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

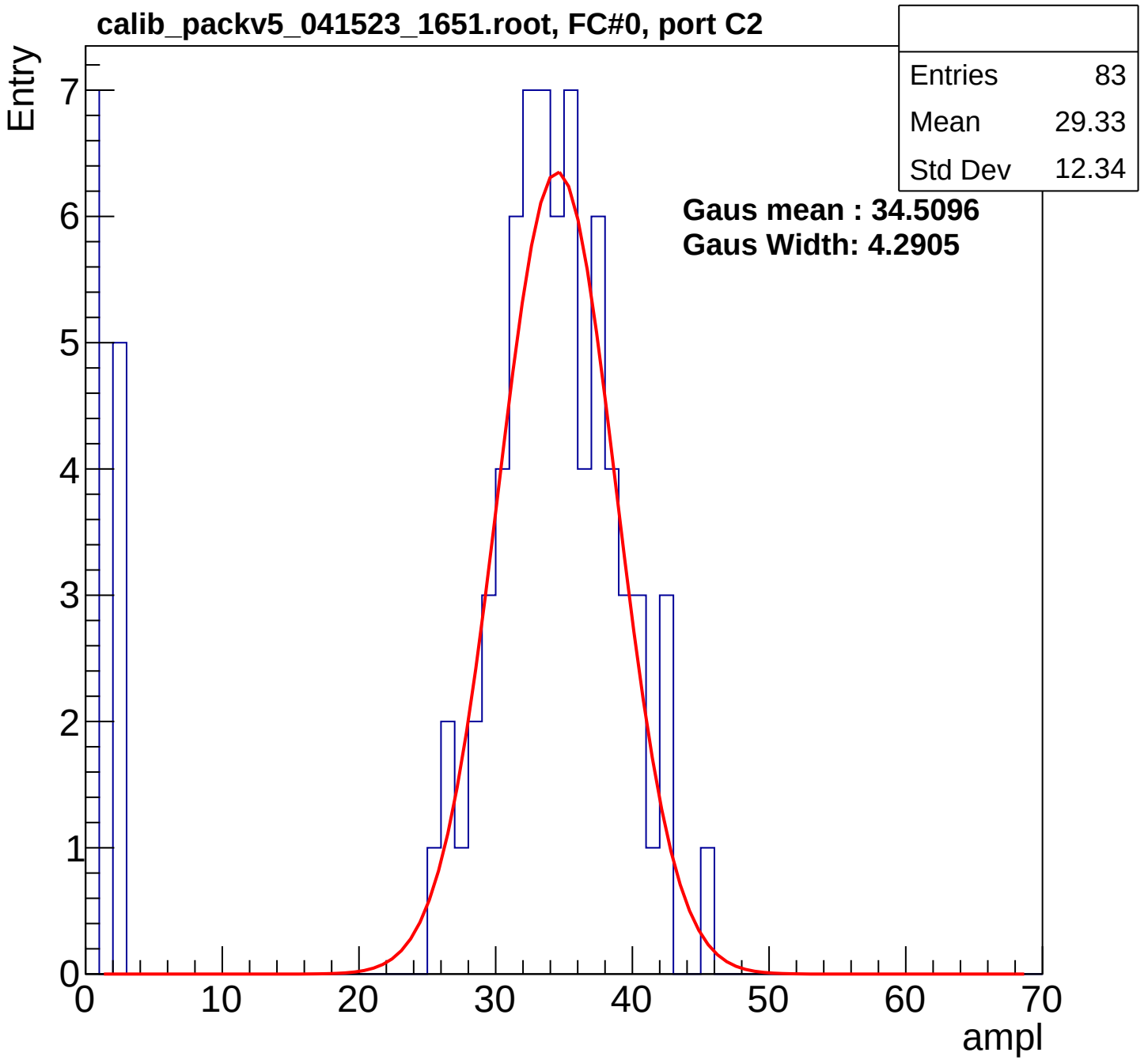

B1L103S, U17-ch81, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 55.08
Std Dev 3.229
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

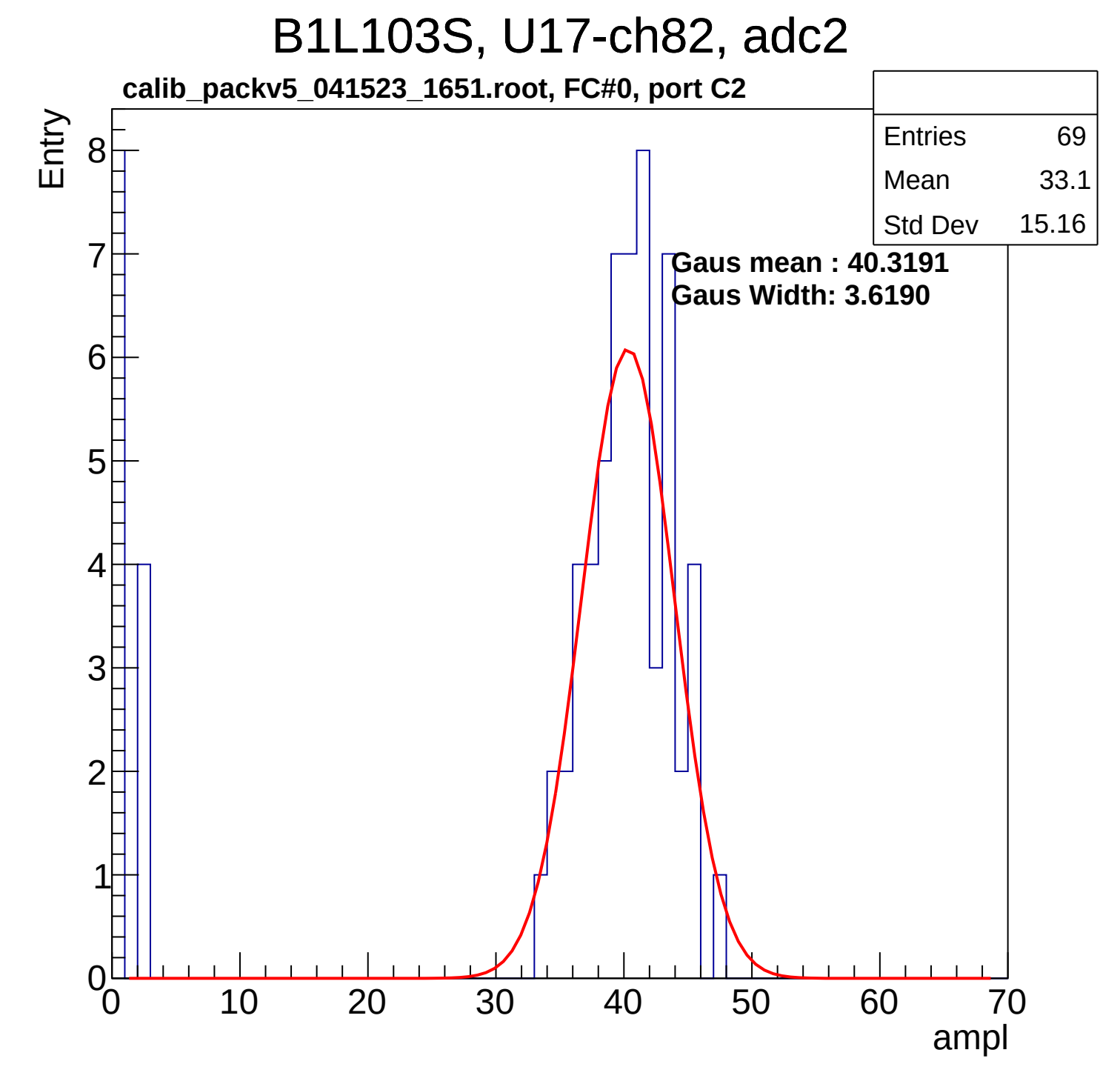

B1L103S, U17-ch81, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.65
Std Dev 8.823
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

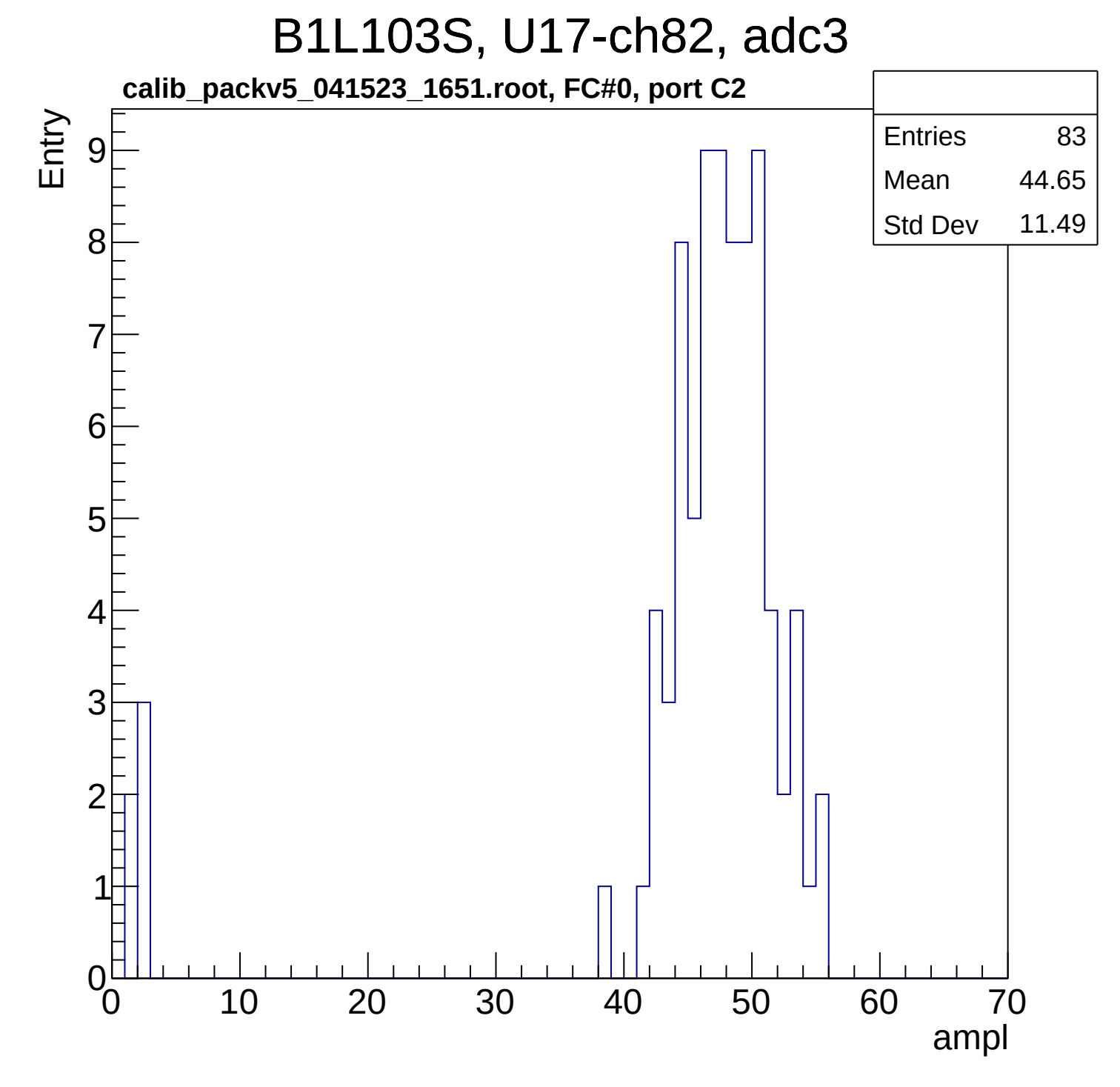

B1L103S, U17-ch81, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.5
Std Dev 1.225
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

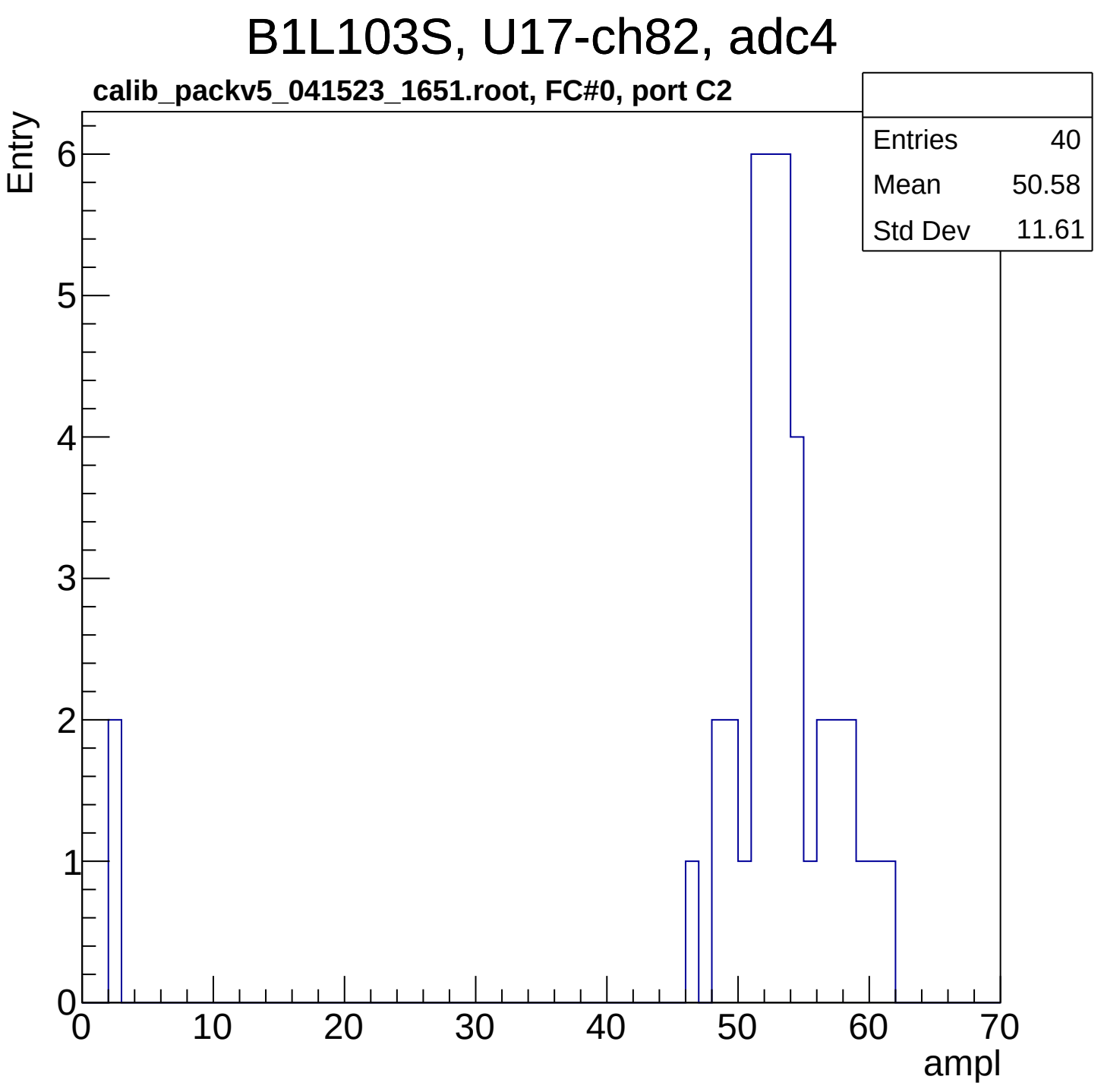

B1L103S, U17-ch81, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

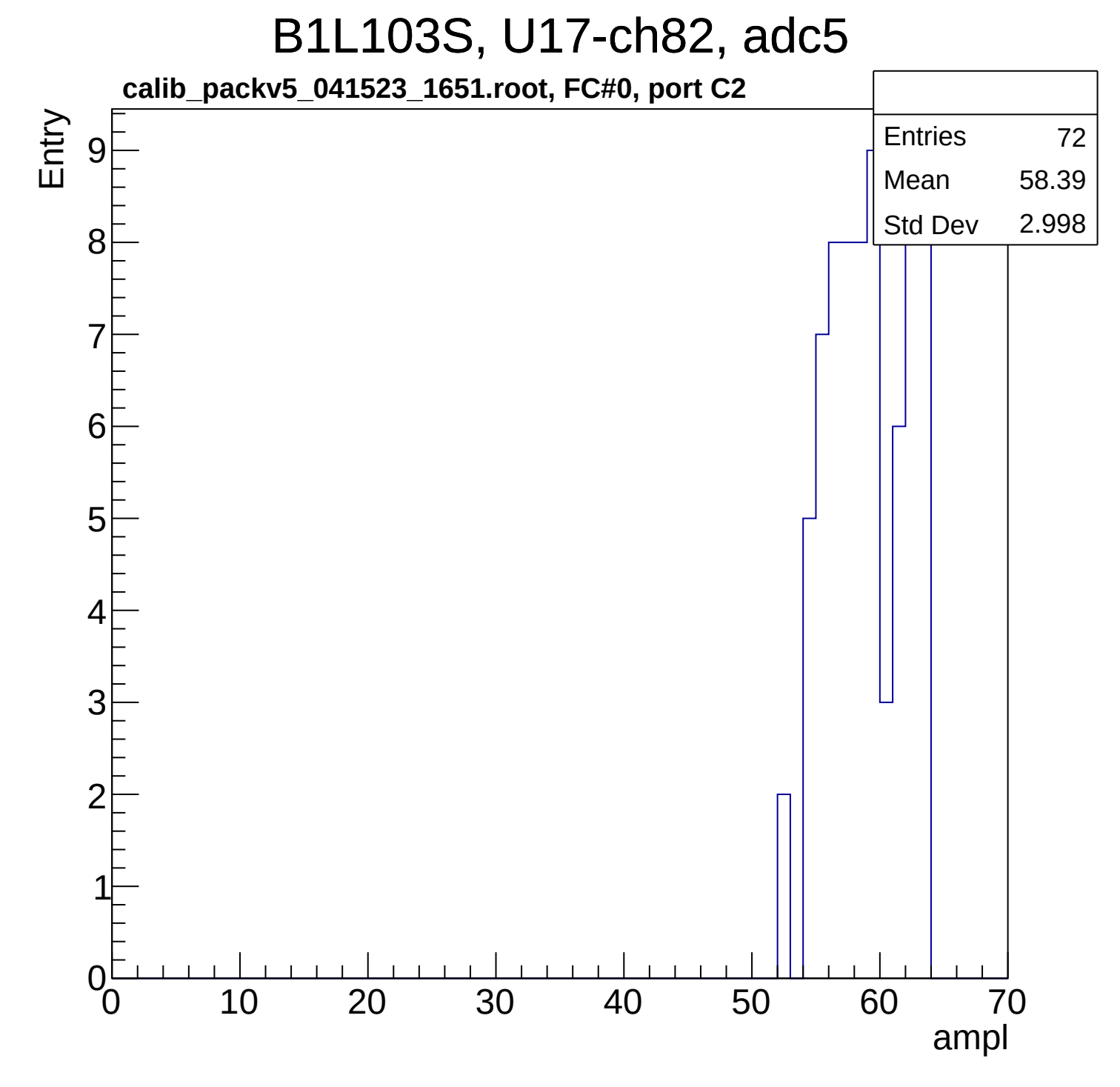

B1L103S, U17-ch82, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 163
Mean 12.31
Std Dev 12.97
Gaus mean : 27.7388
Gaus Width: 4.8355
Entry
ampl
0
10
20
30
40
50
60
70

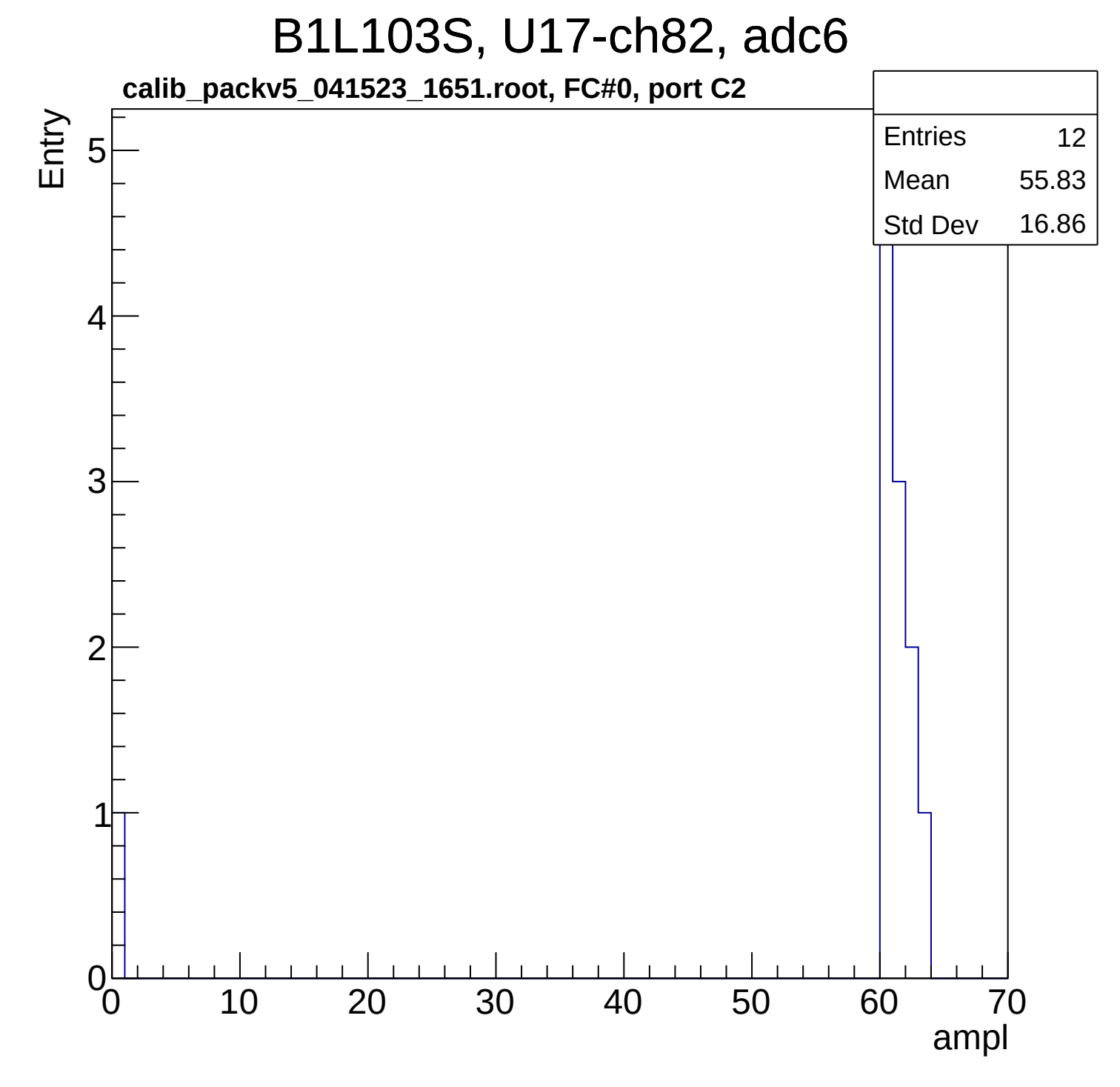

B1L103S, U17-ch82, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 29.33
Std Dev 12.34
Gaus mean : 34.5096
Gaus Width: 4.2905
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

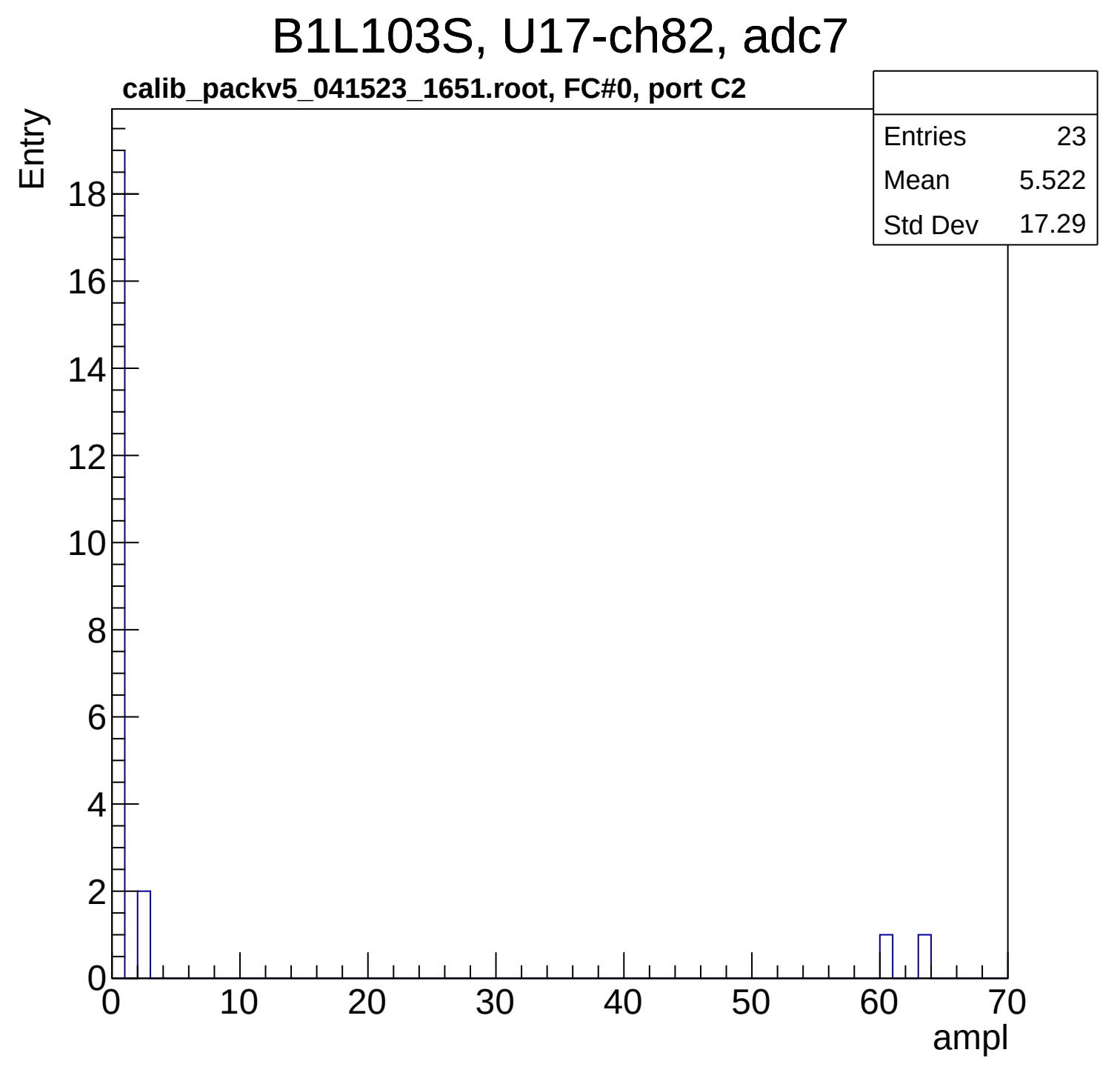

B1L103S, U17-ch82, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 33.1
Std Dev 15.16
Gaus mean : 40.3191
Gaus Width: 3.6190
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

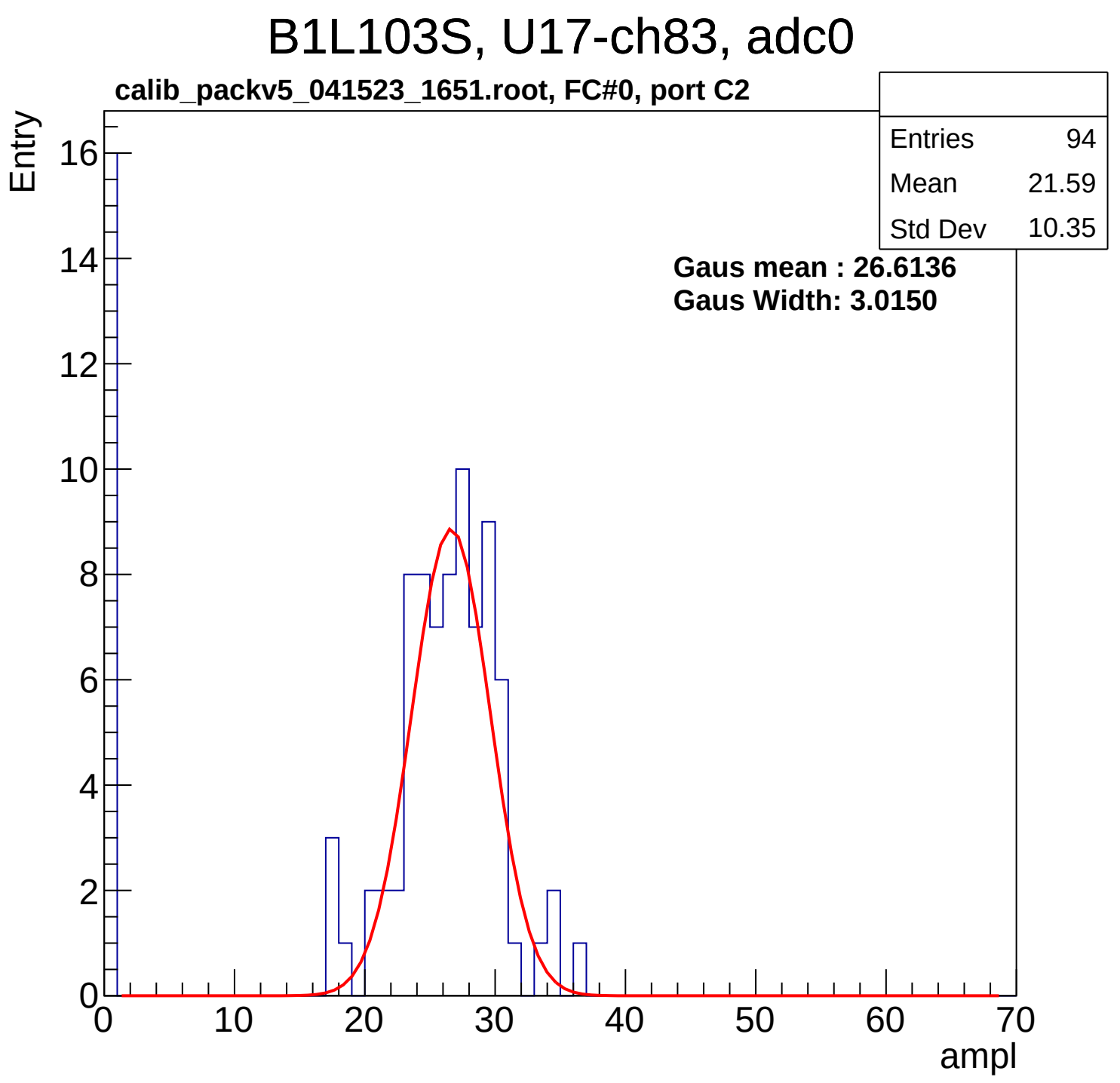

B1L103S, U17-ch82, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 44.65
Std Dev 11.49
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

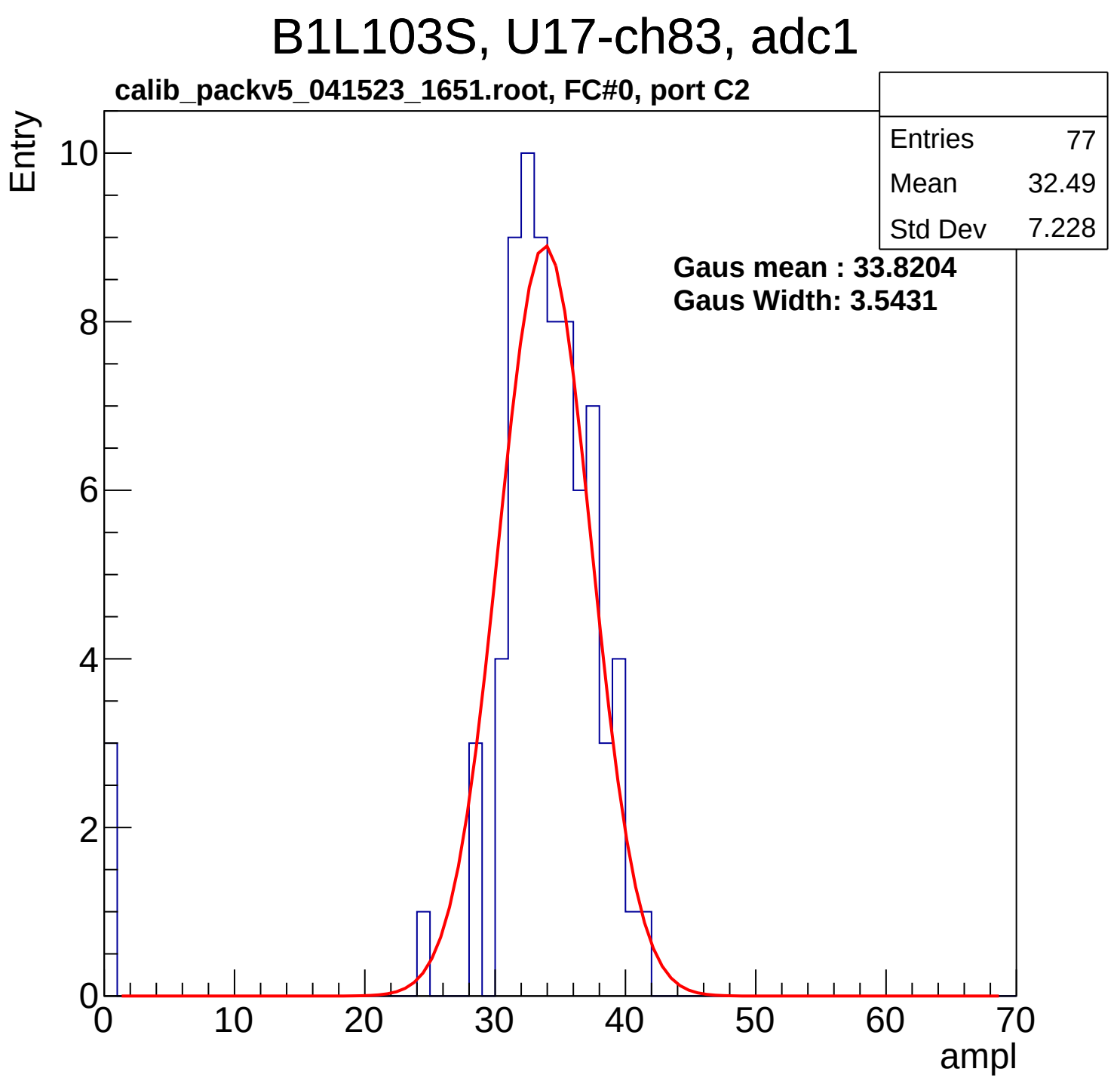

B1L103S, U17-ch82, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 50.58
Std Dev 11.61
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

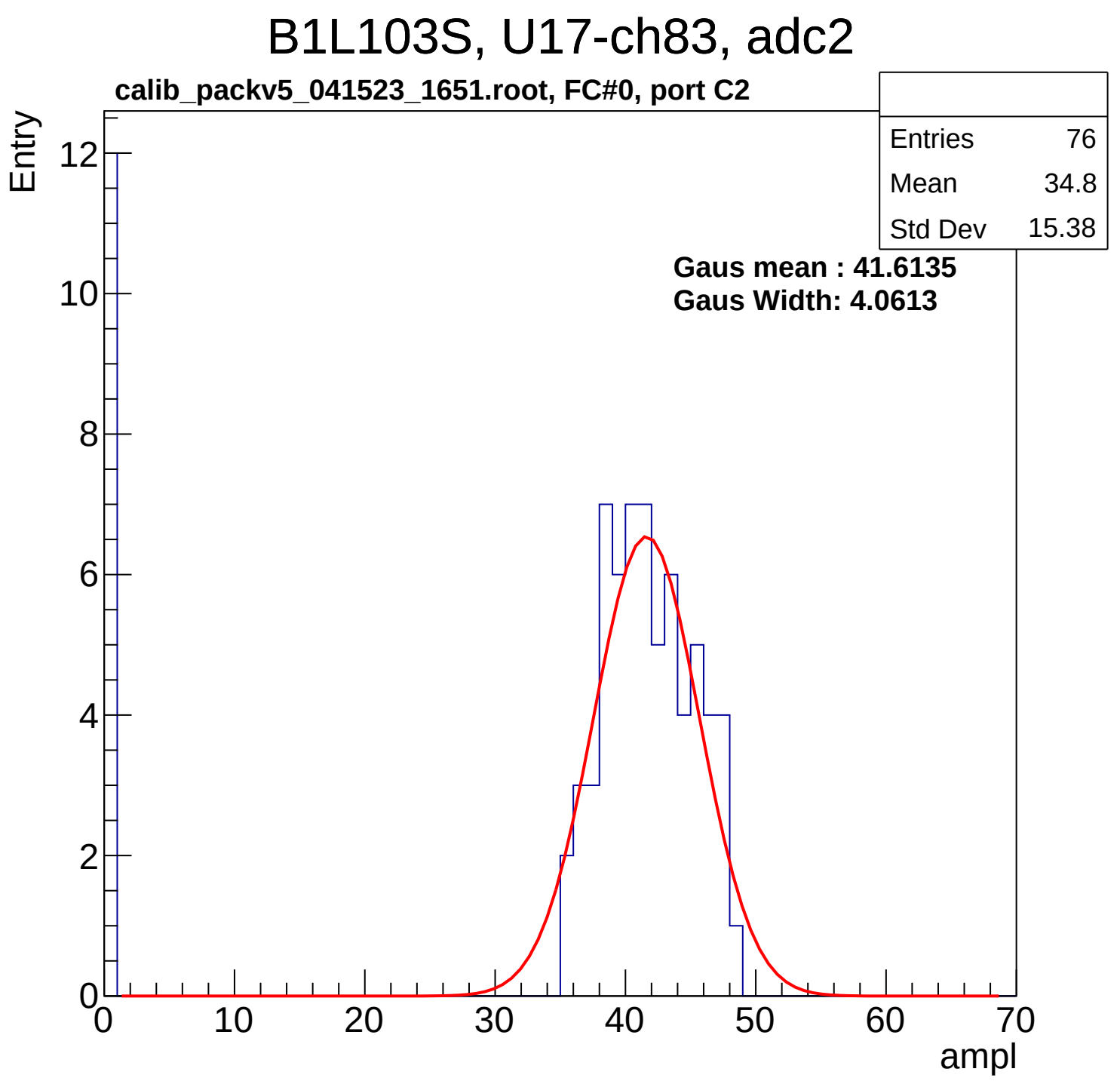

B1L103S, U17-ch82, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 58.39
Std Dev 2.998
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

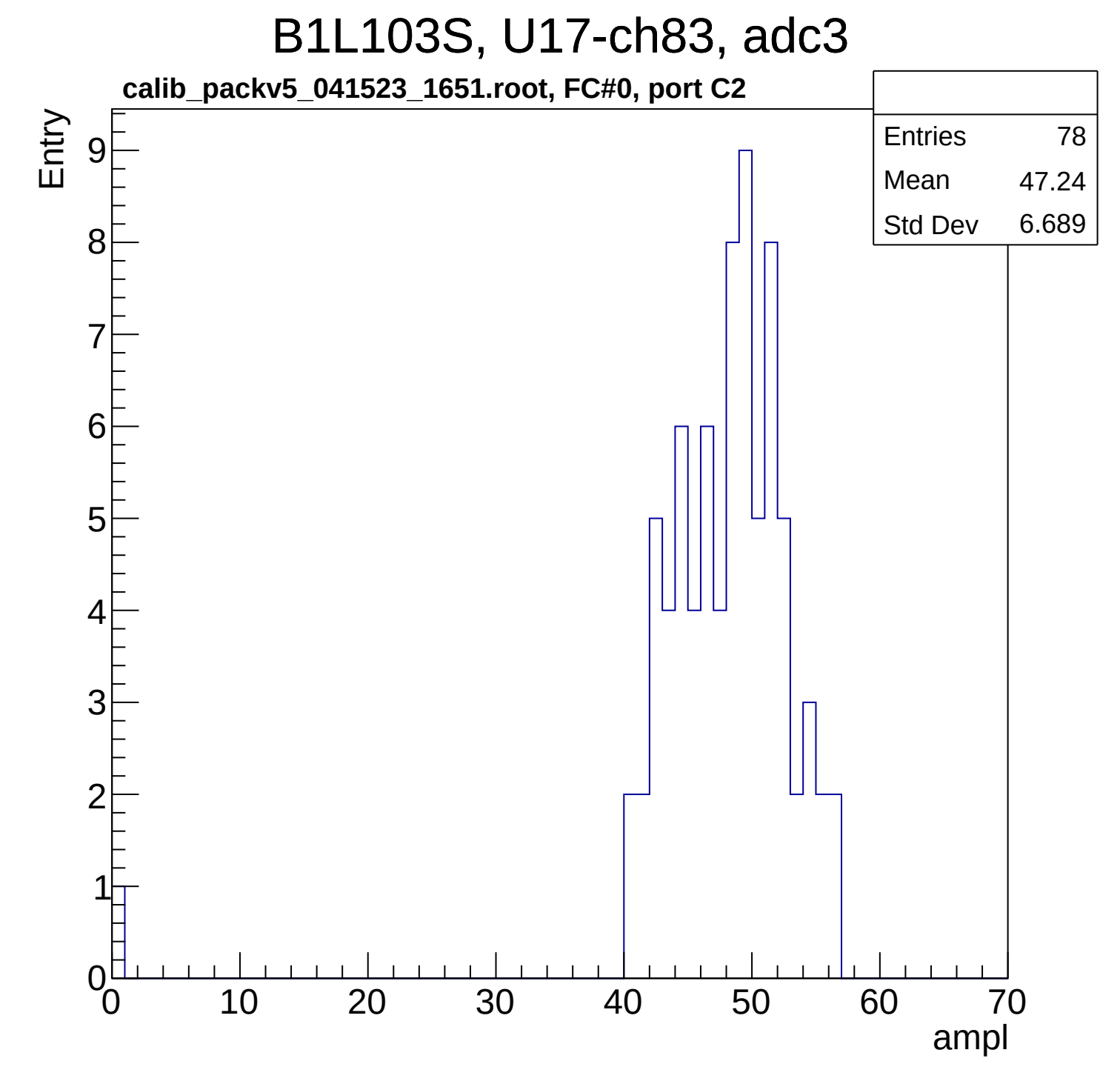

B1L103S, U17-ch82, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 55.83
Std Dev 16.86
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

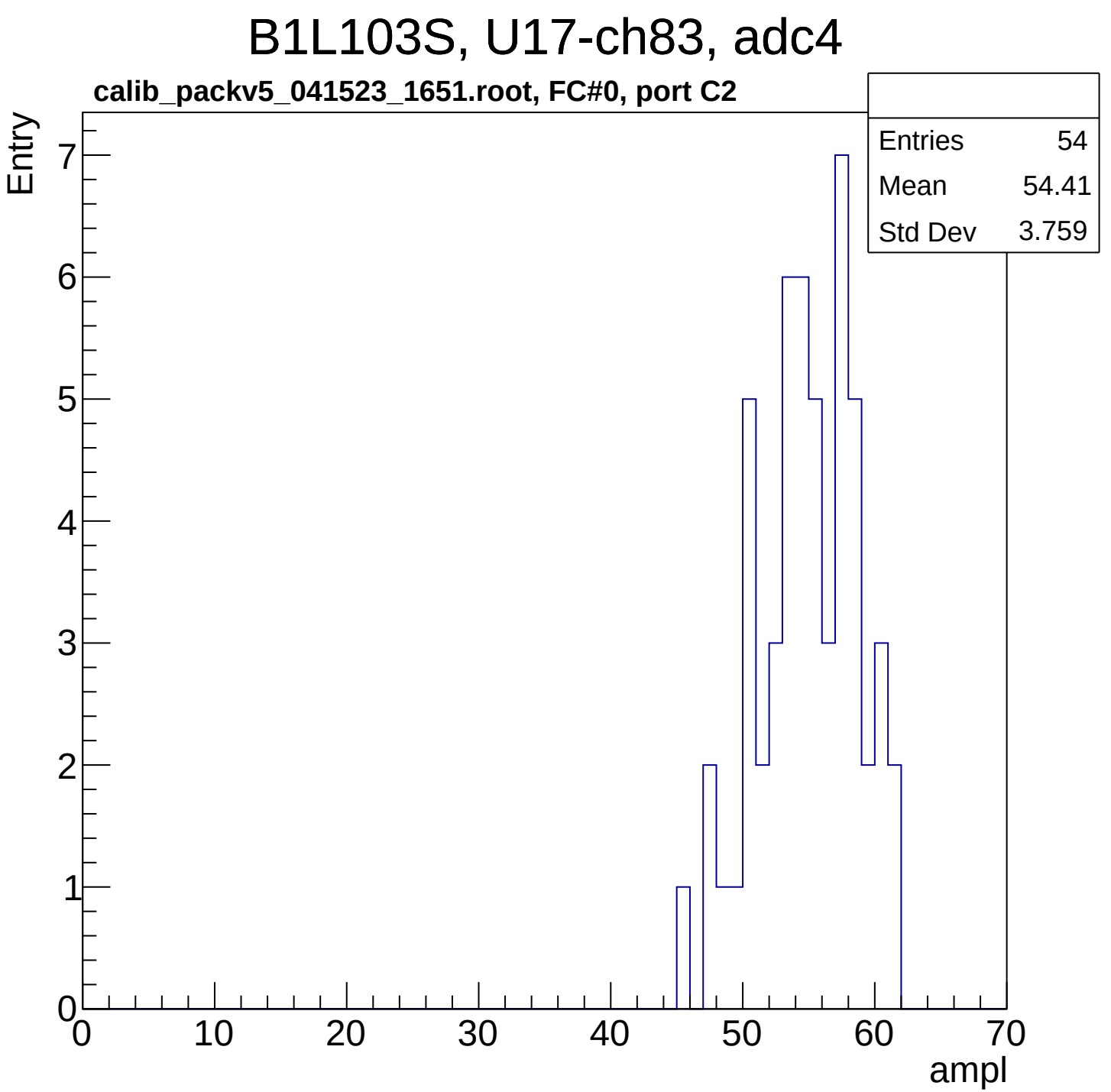

B1L103S, U17-ch82, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 5.522
Std Dev 17.29
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

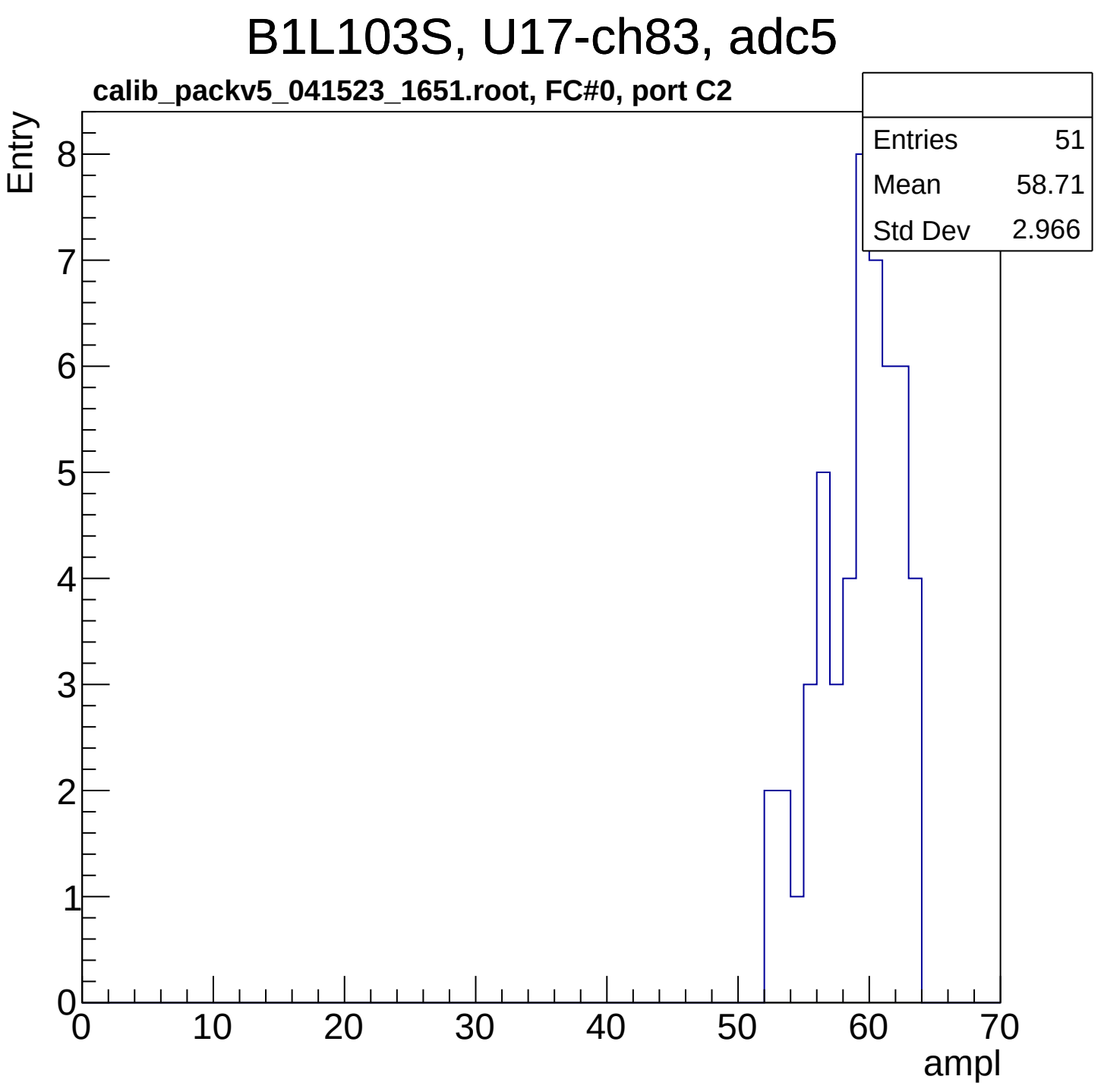

B1L103S, U17-ch83, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 21.59
Std Dev 10.35
Gaus mean : 26.6136
Gaus Width: 3.0150
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

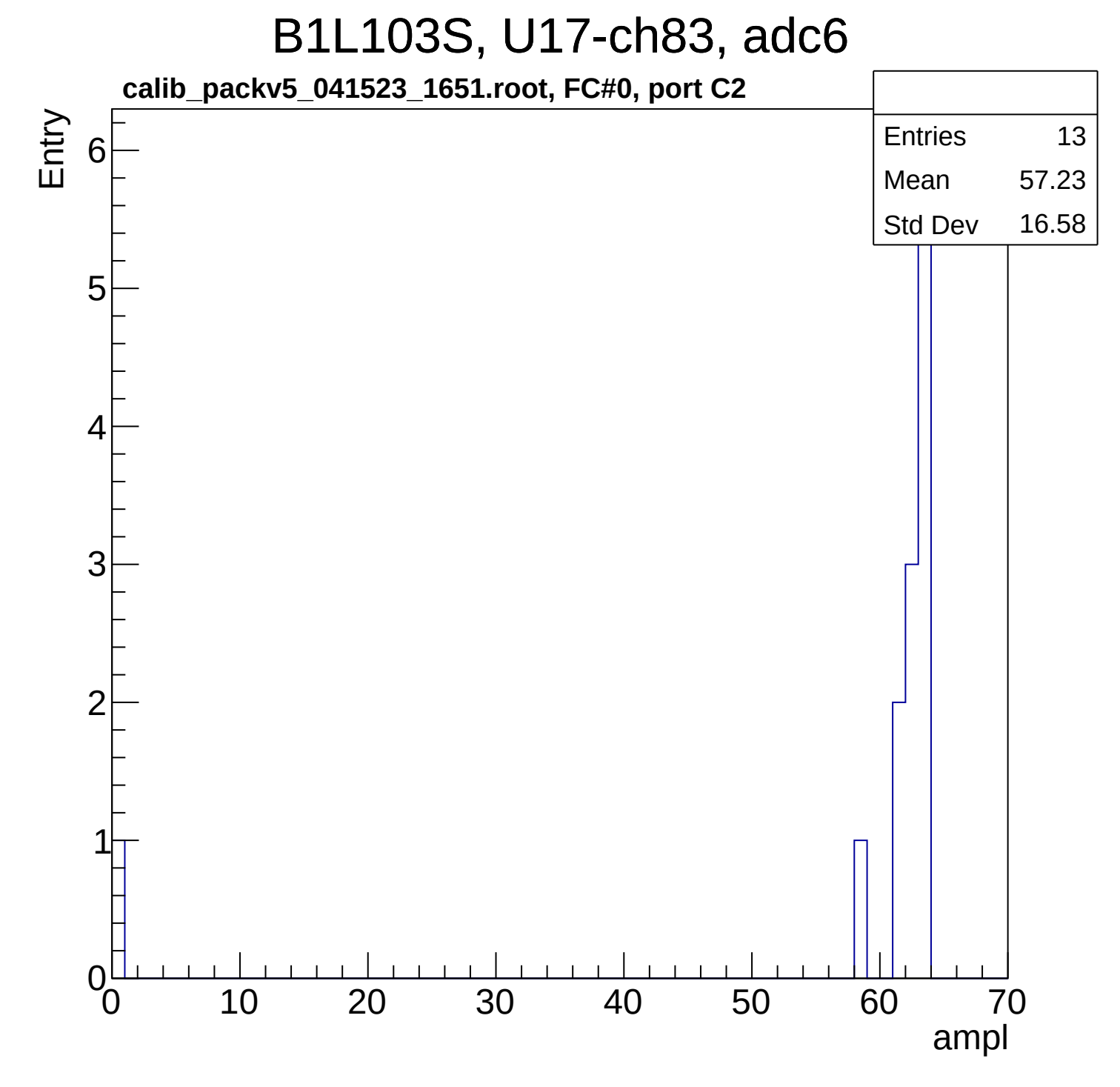

B1L103S, U17-ch83, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 32.49
Std Dev 7.228
Gaus mean : 33.8204
Gaus Width: 3.5431
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

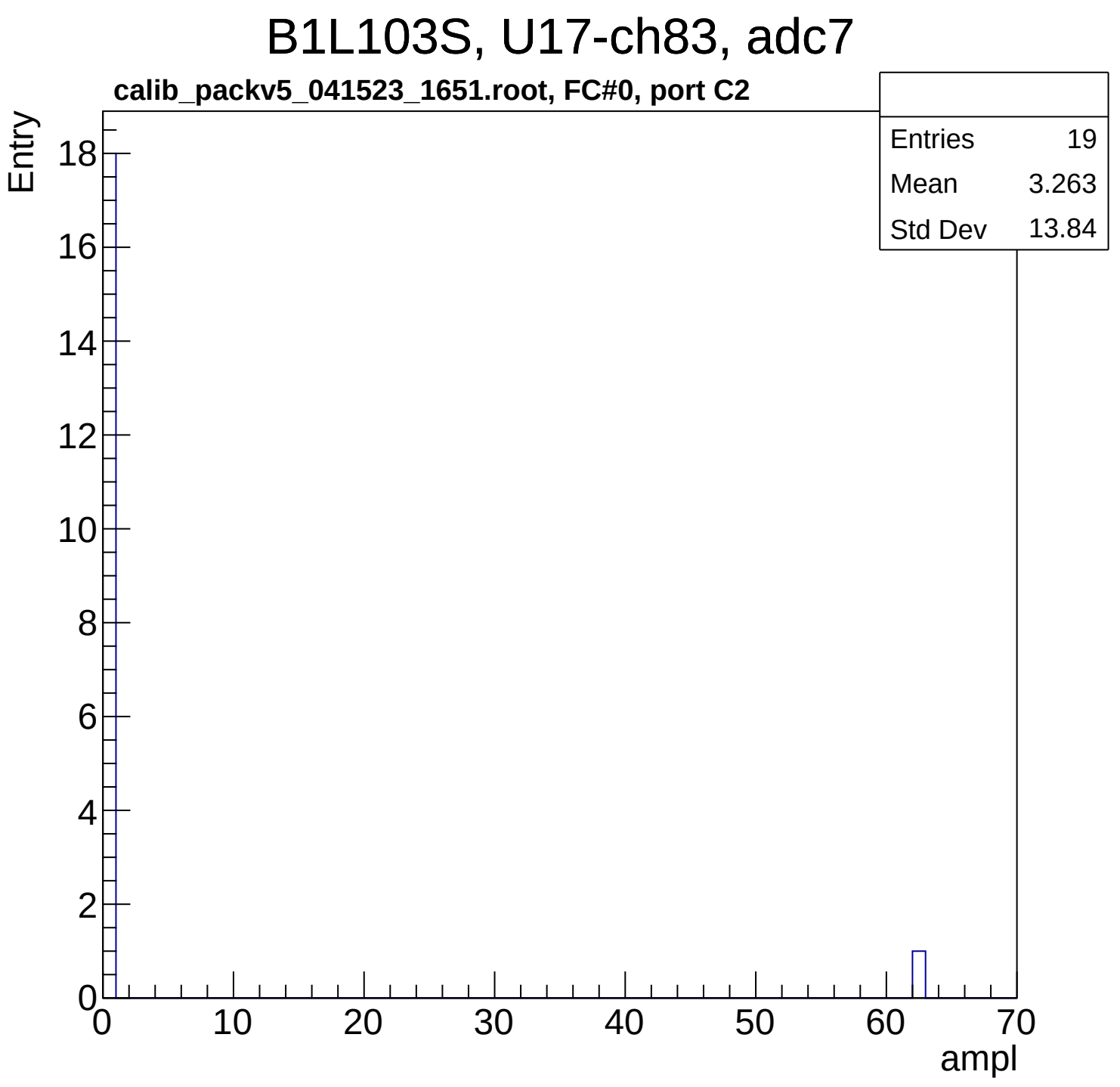

B1L103S, U17-ch83, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 34.8
Std Dev 15.38
Gaus mean : 41.6135
Gaus Width: 4.0613
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

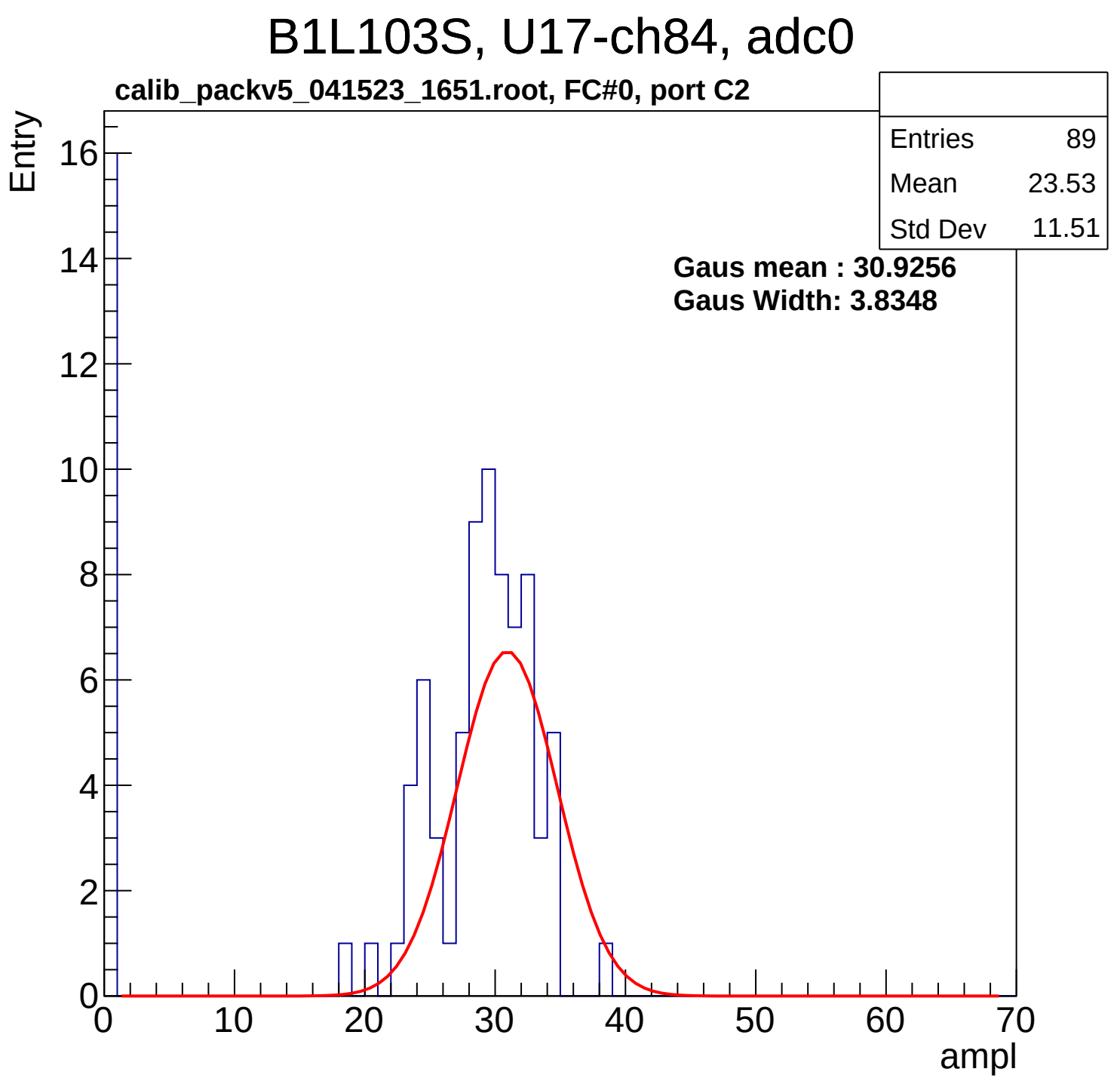

B1L103S, U17-ch83, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 47.24
Std Dev 6.689
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

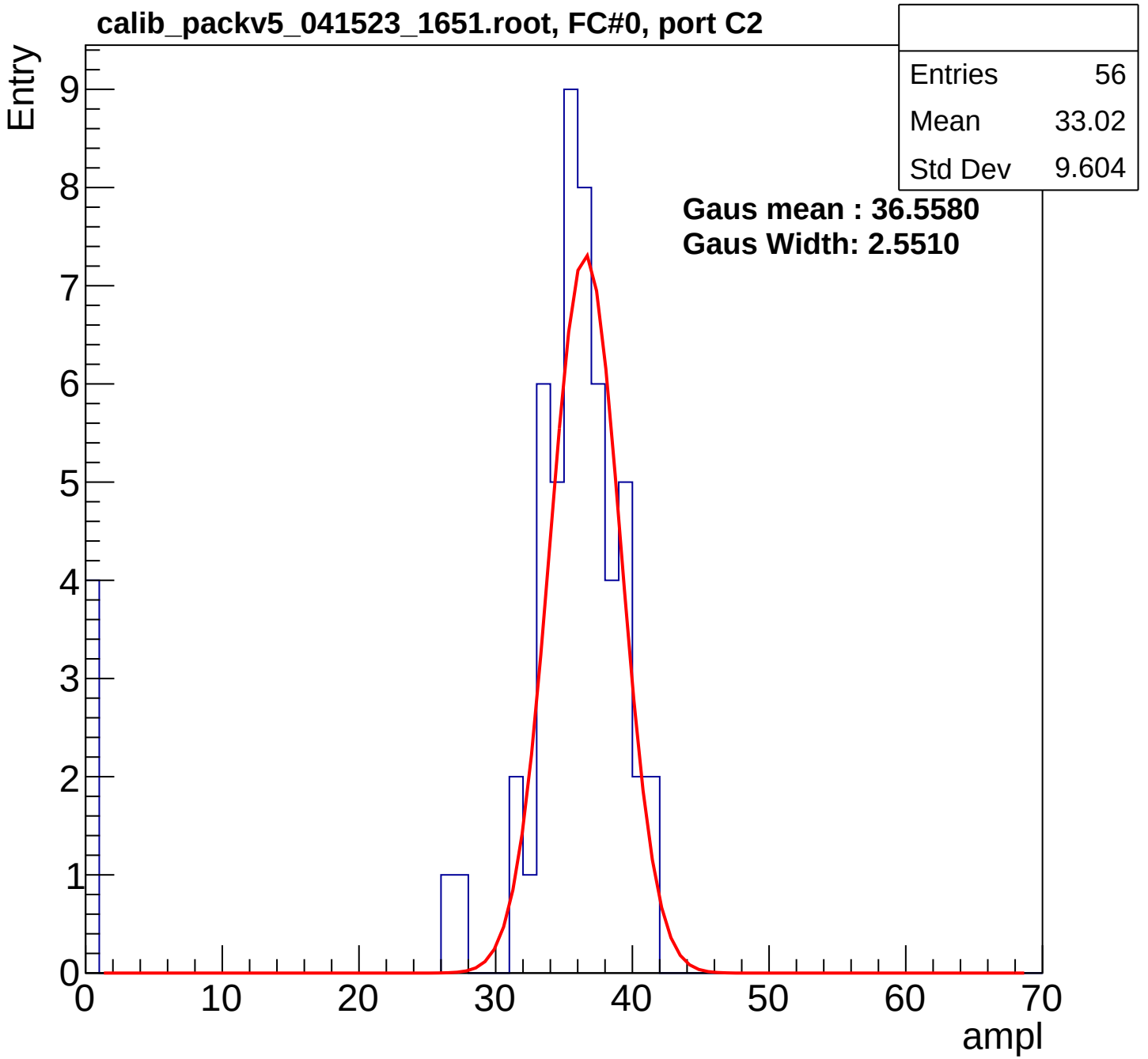

B1L103S, U17-ch83, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 54.41
Std Dev 3.759
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

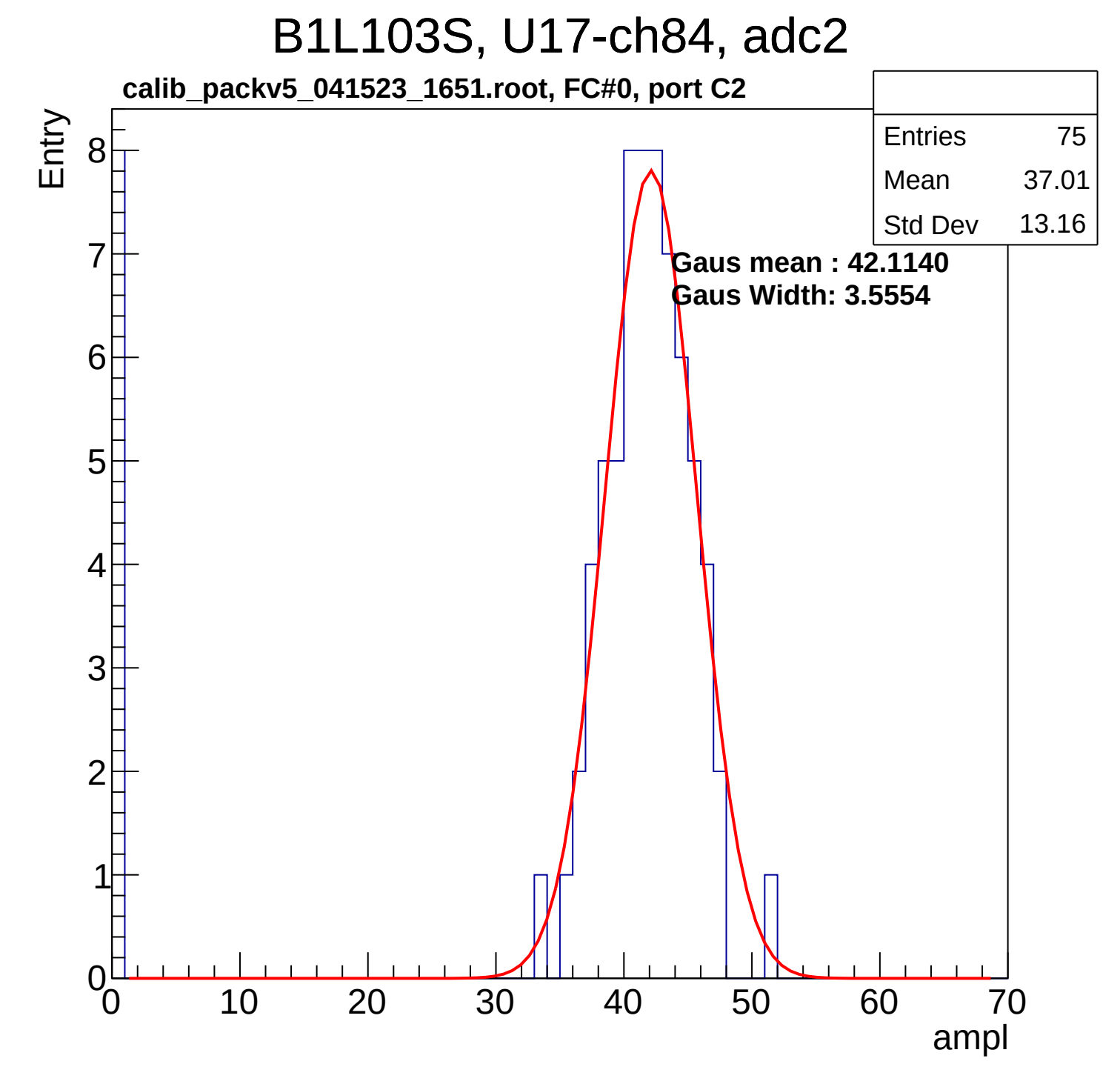

B1L103S, U17-ch83, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.71
Std Dev 2.966
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

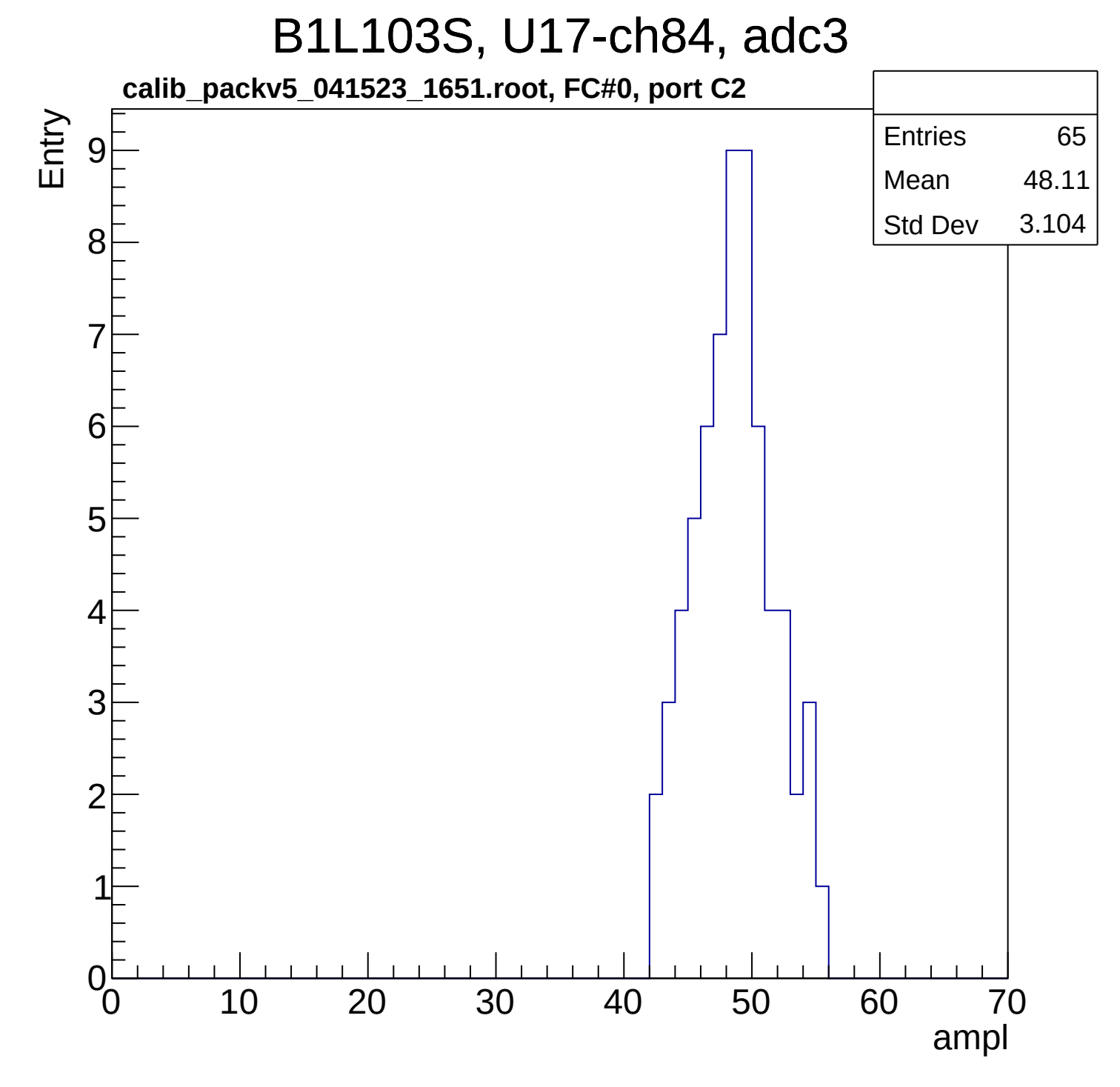

B1L103S, U17-ch83, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 57.23
Std Dev 16.58
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

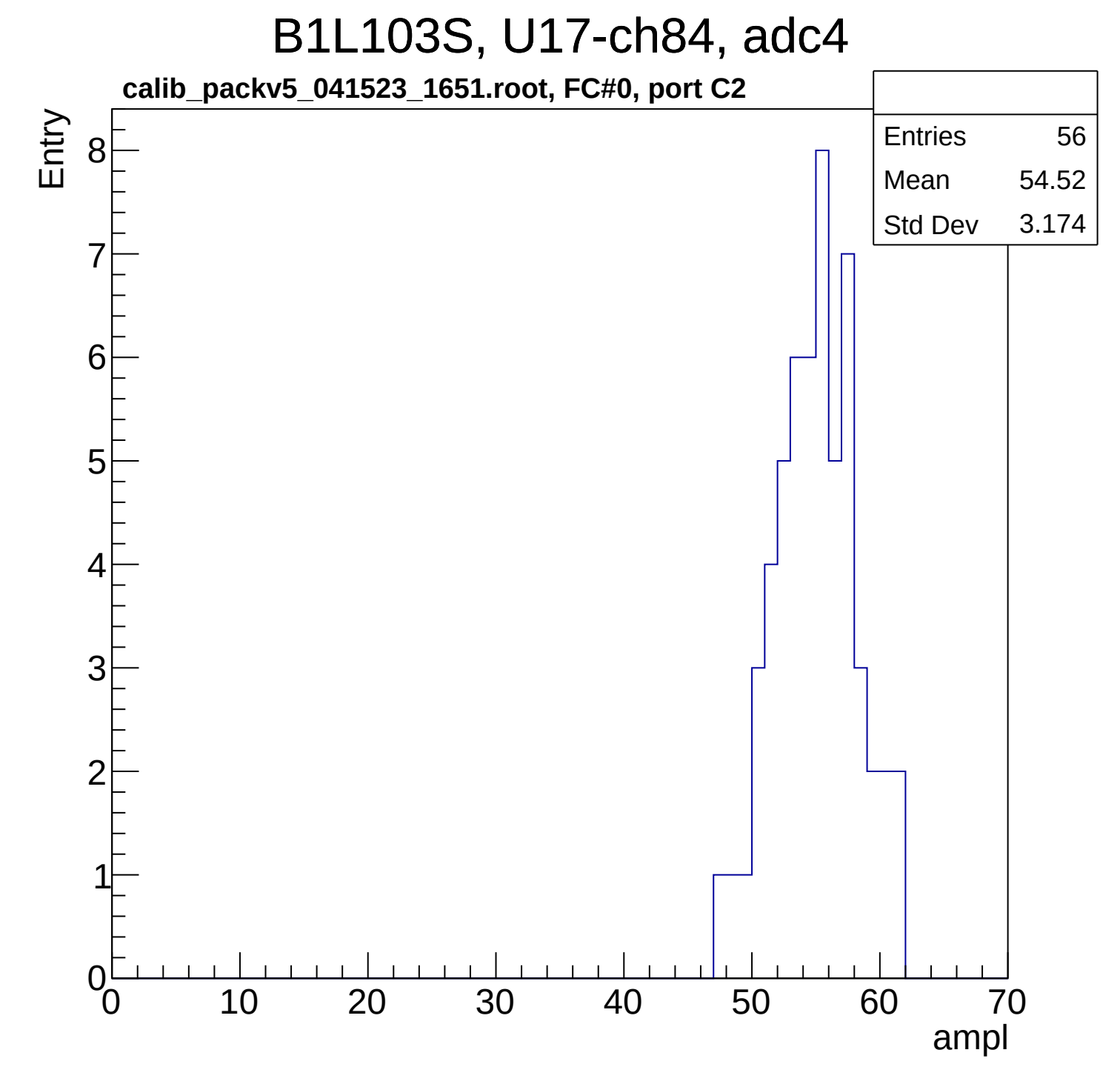

B1L103S, U17-ch83, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.263
Std Dev 13.84
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

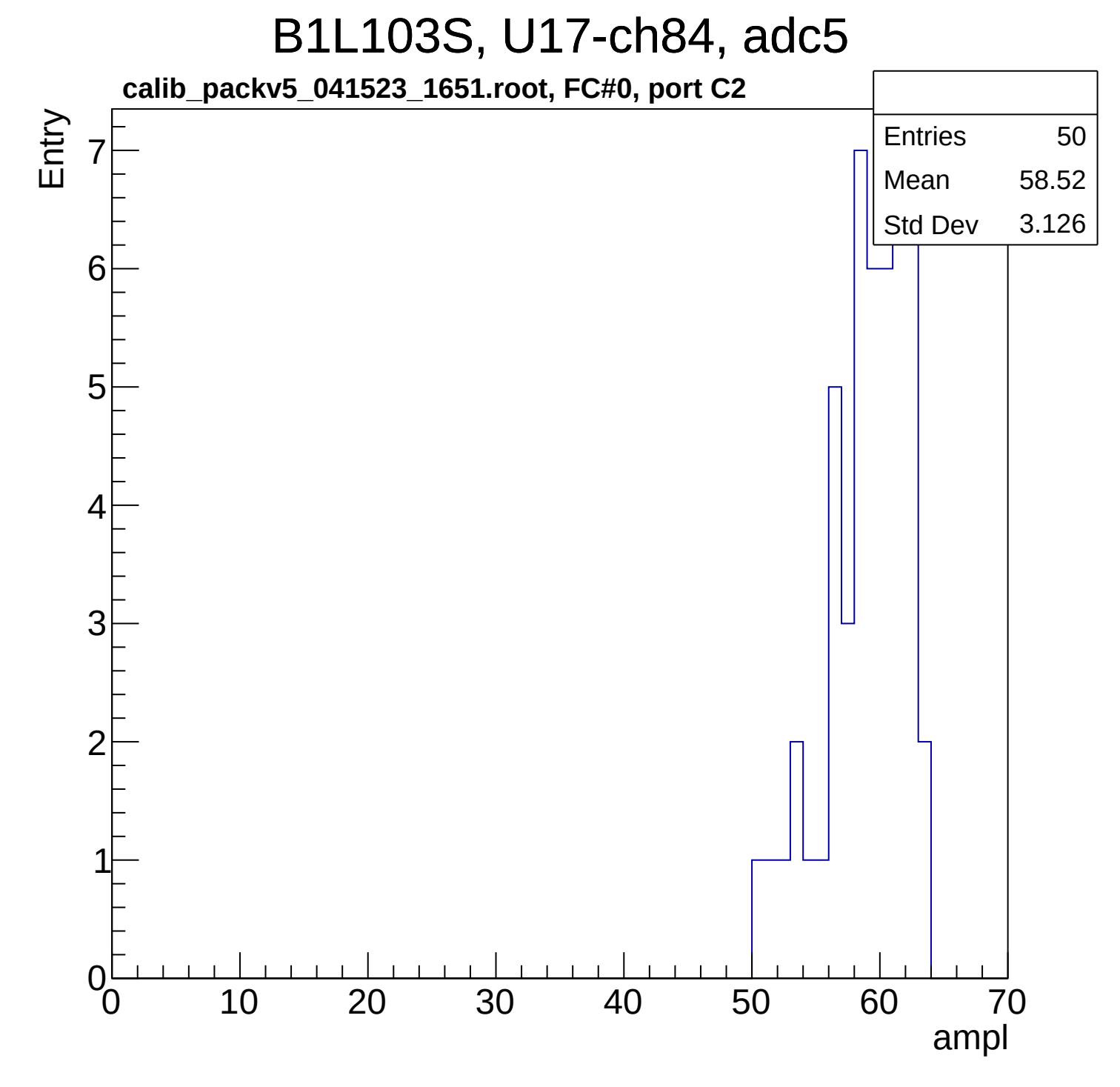

B1L103S, U17-ch84, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 23.53
Std Dev 11.51
Gaus mean : 30.9256
Gaus Width: 3.8348
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

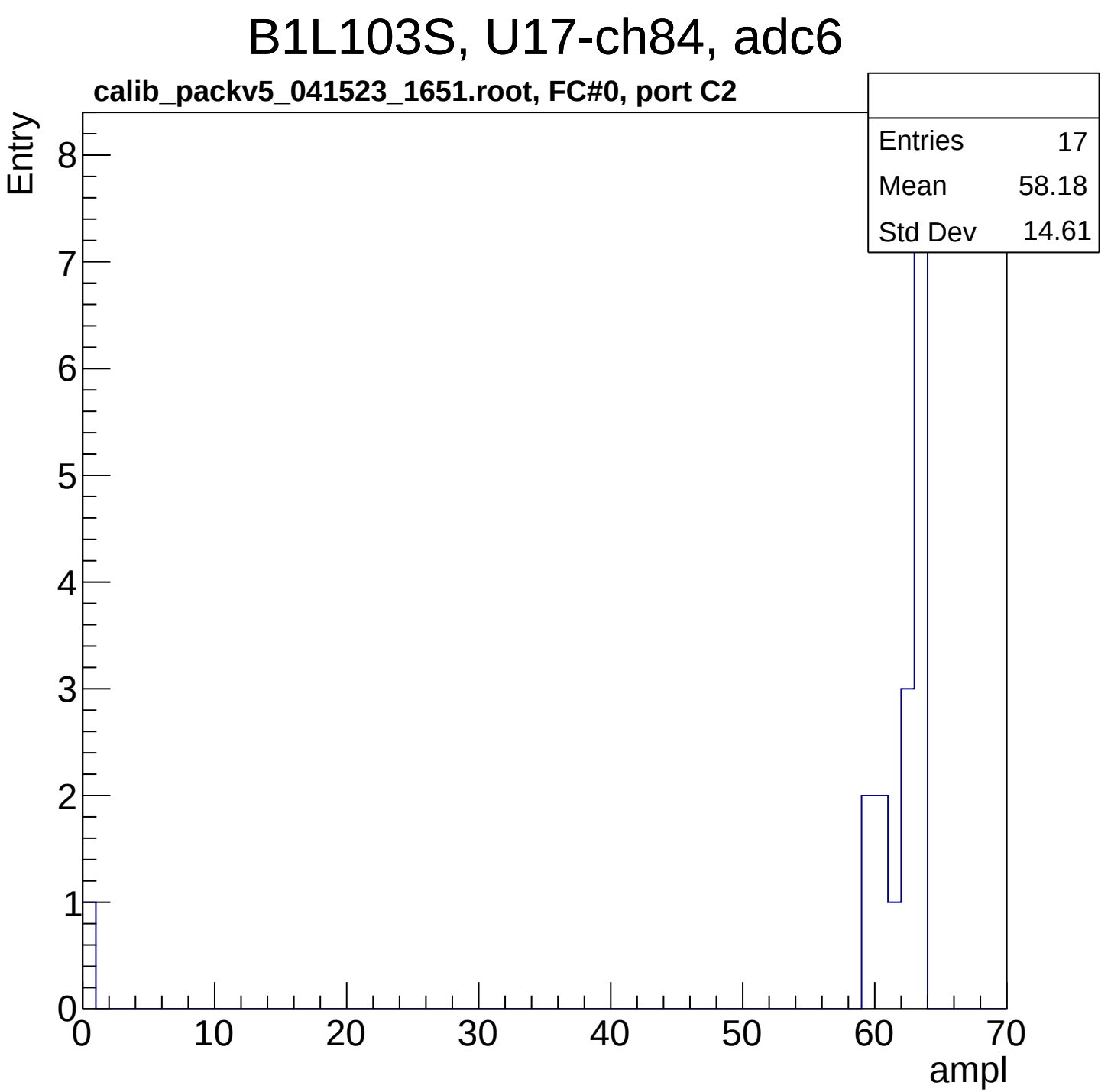

B1L103S, U17-ch84, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 33.02
Std Dev 9.604
Gaus mean : 36.5580
Gaus Width: 2.5510
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

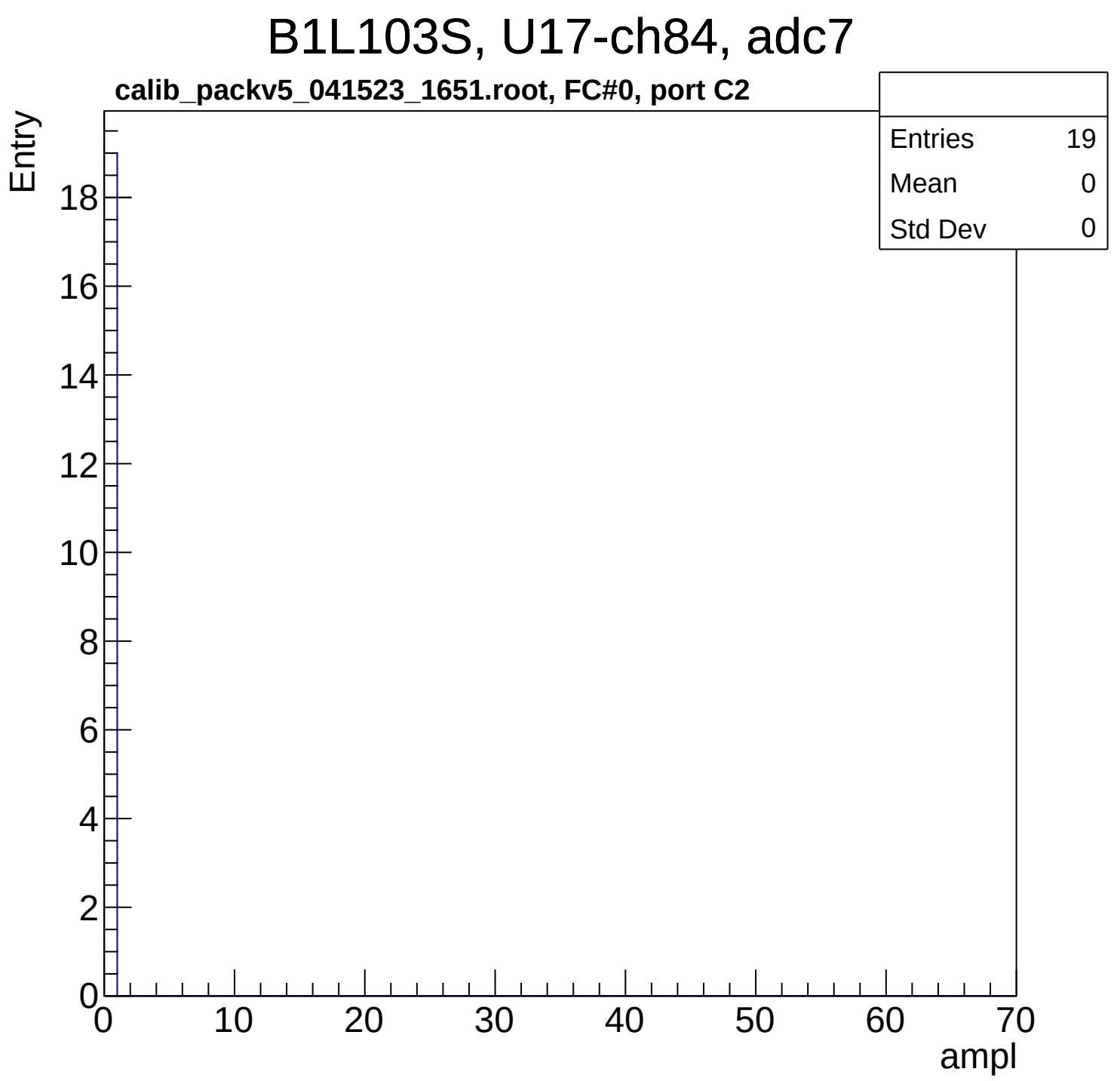

B1L103S, U17-ch84, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 37.01
Std Dev 13.16
Gaus mean : 42.1140
Gaus Width: 3.5554
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

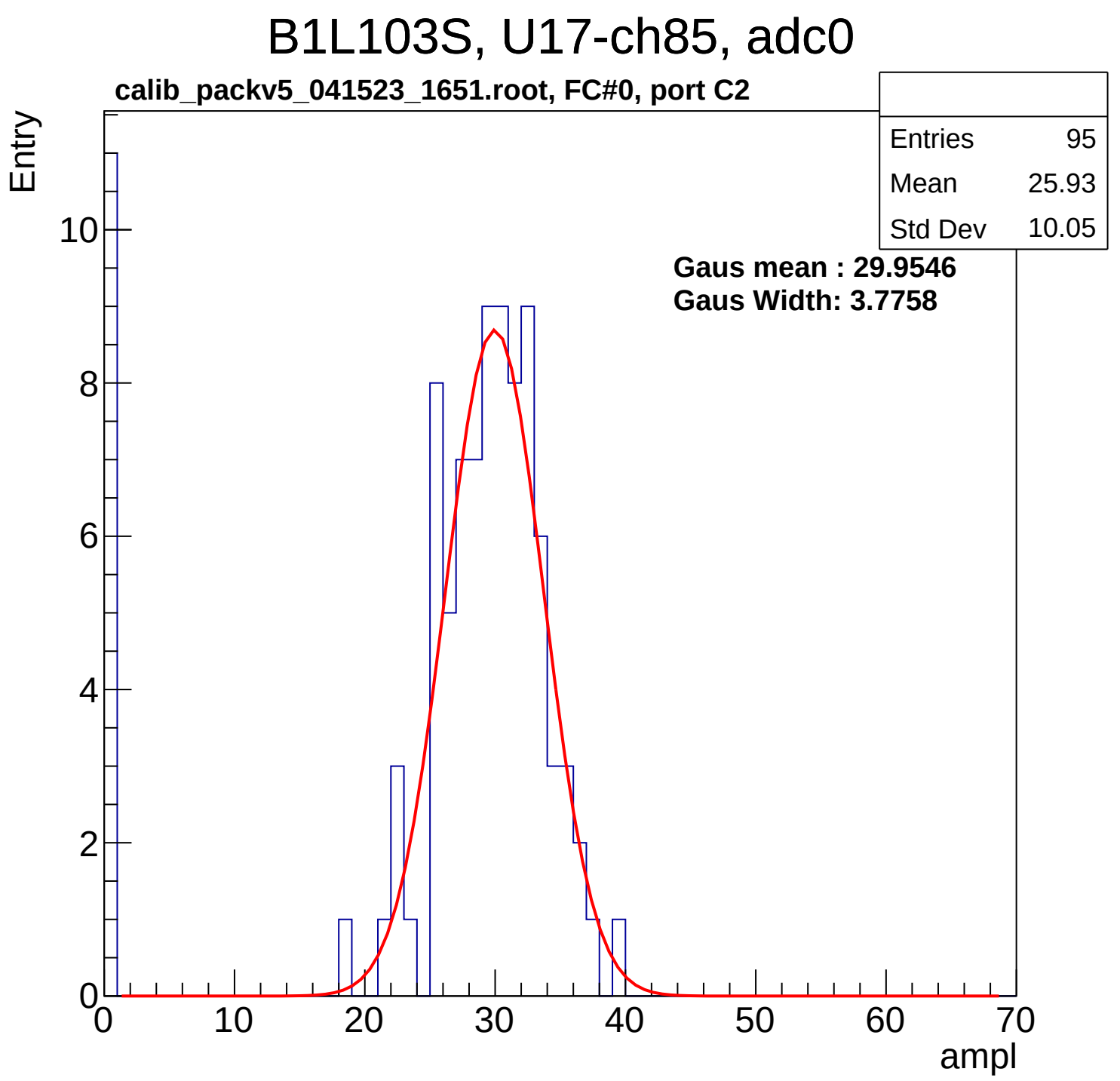

B1L103S, U17-ch84, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 48.11
Std Dev 3.104
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

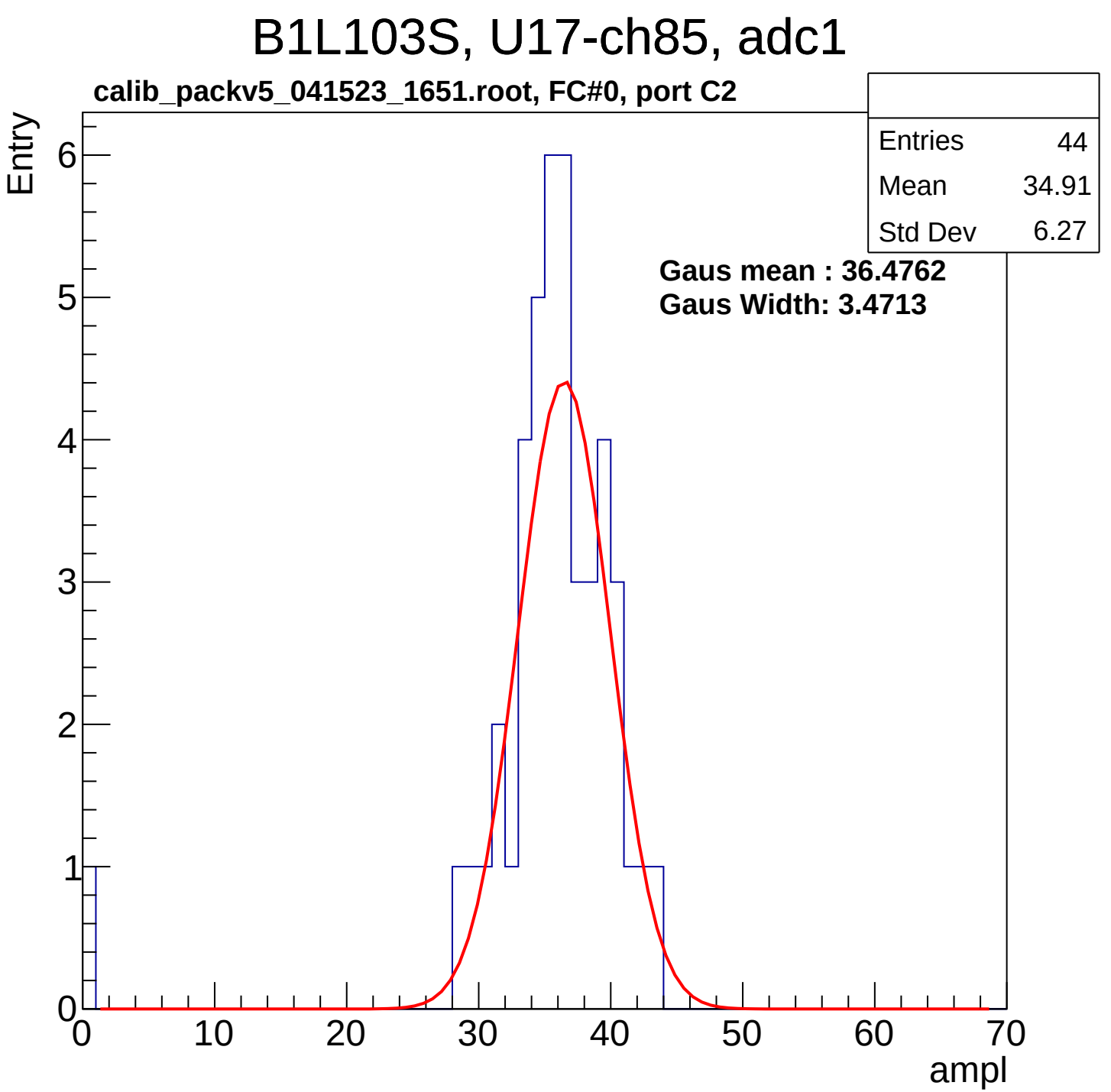

B1L103S, U17-ch84, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 54.52
Std Dev 3.174
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

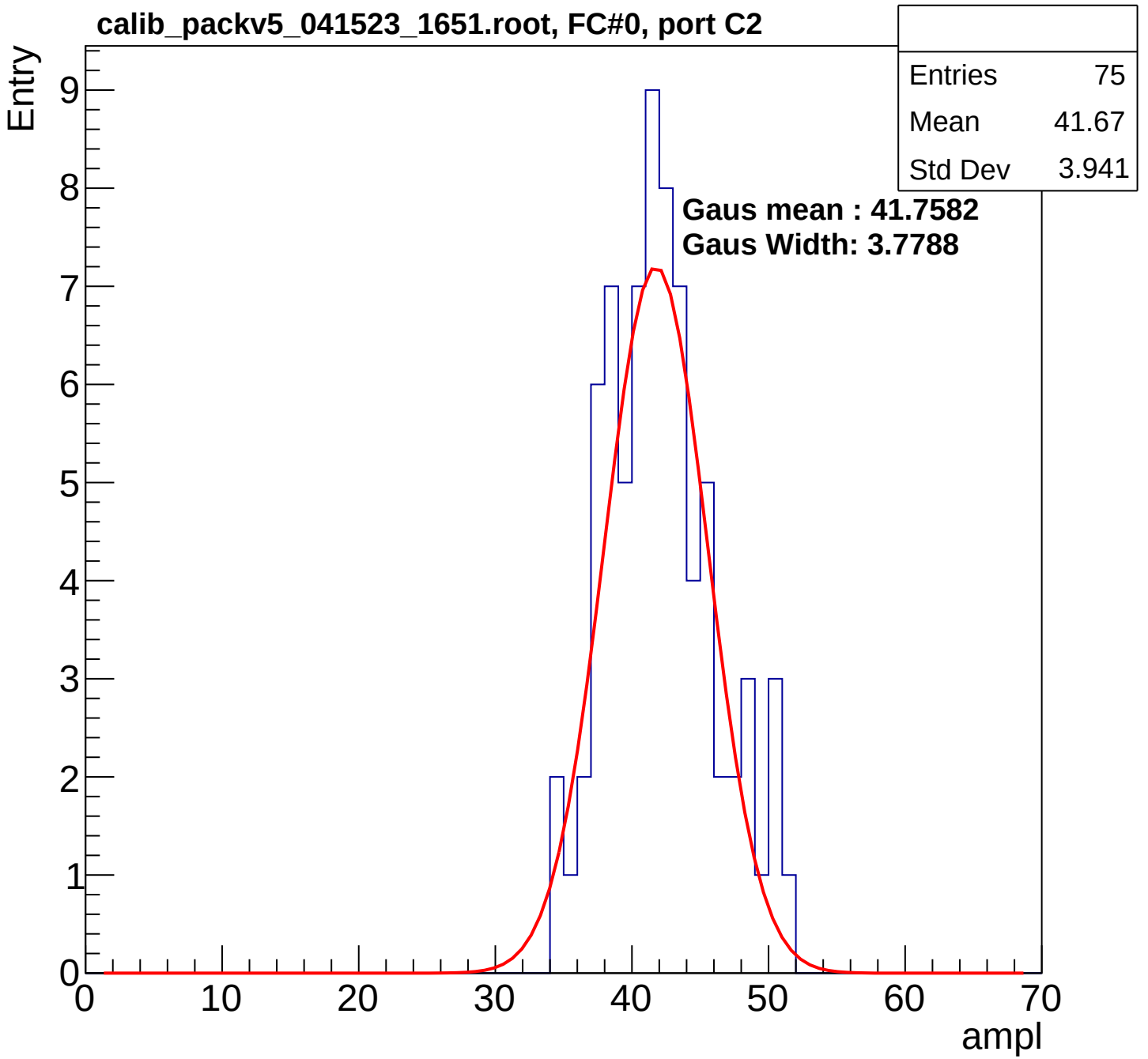

B1L103S, U17-ch84, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.52
Std Dev 3.126
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

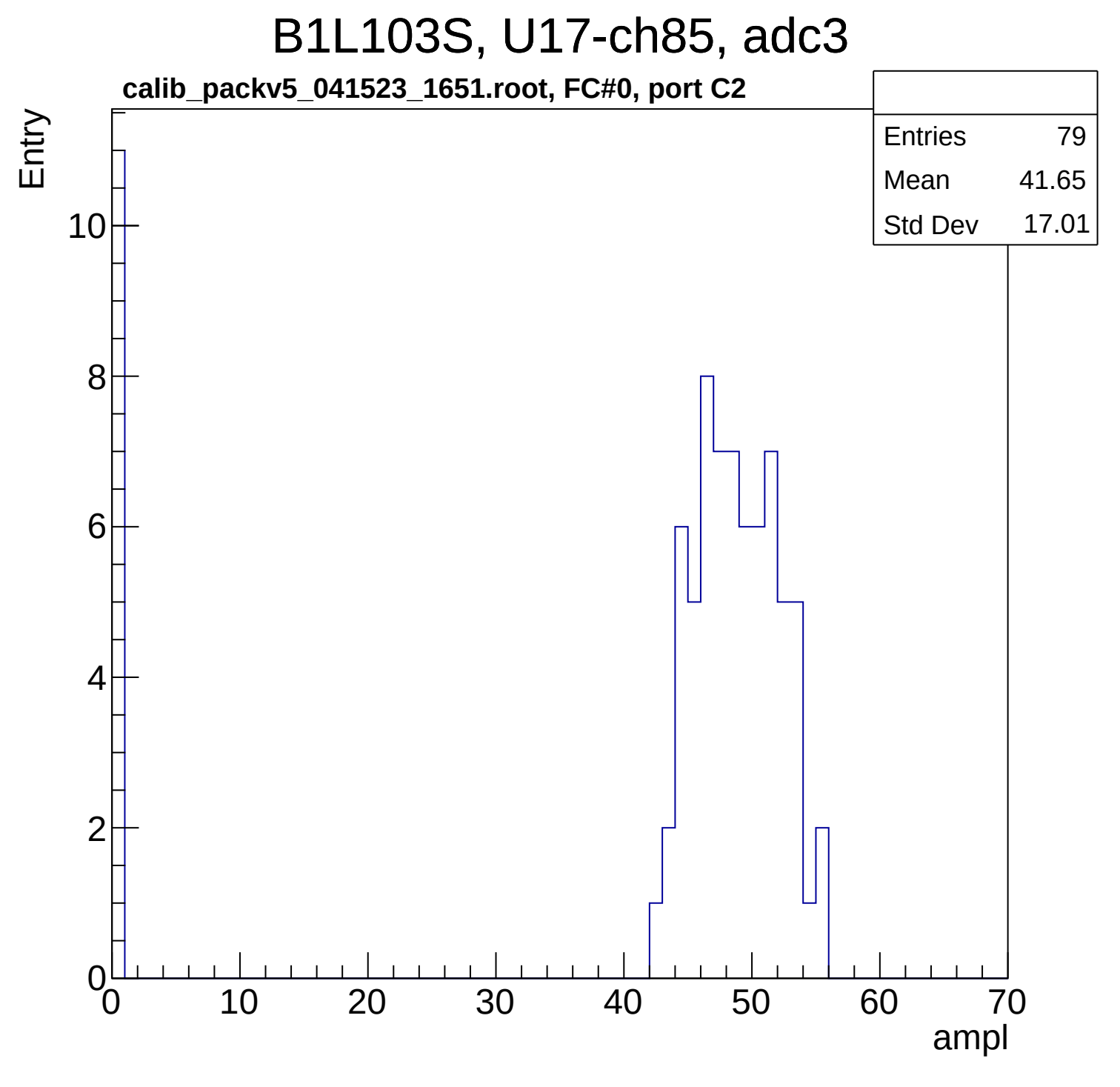

B1L103S, U17-ch84, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 58.18
Std Dev 14.61
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

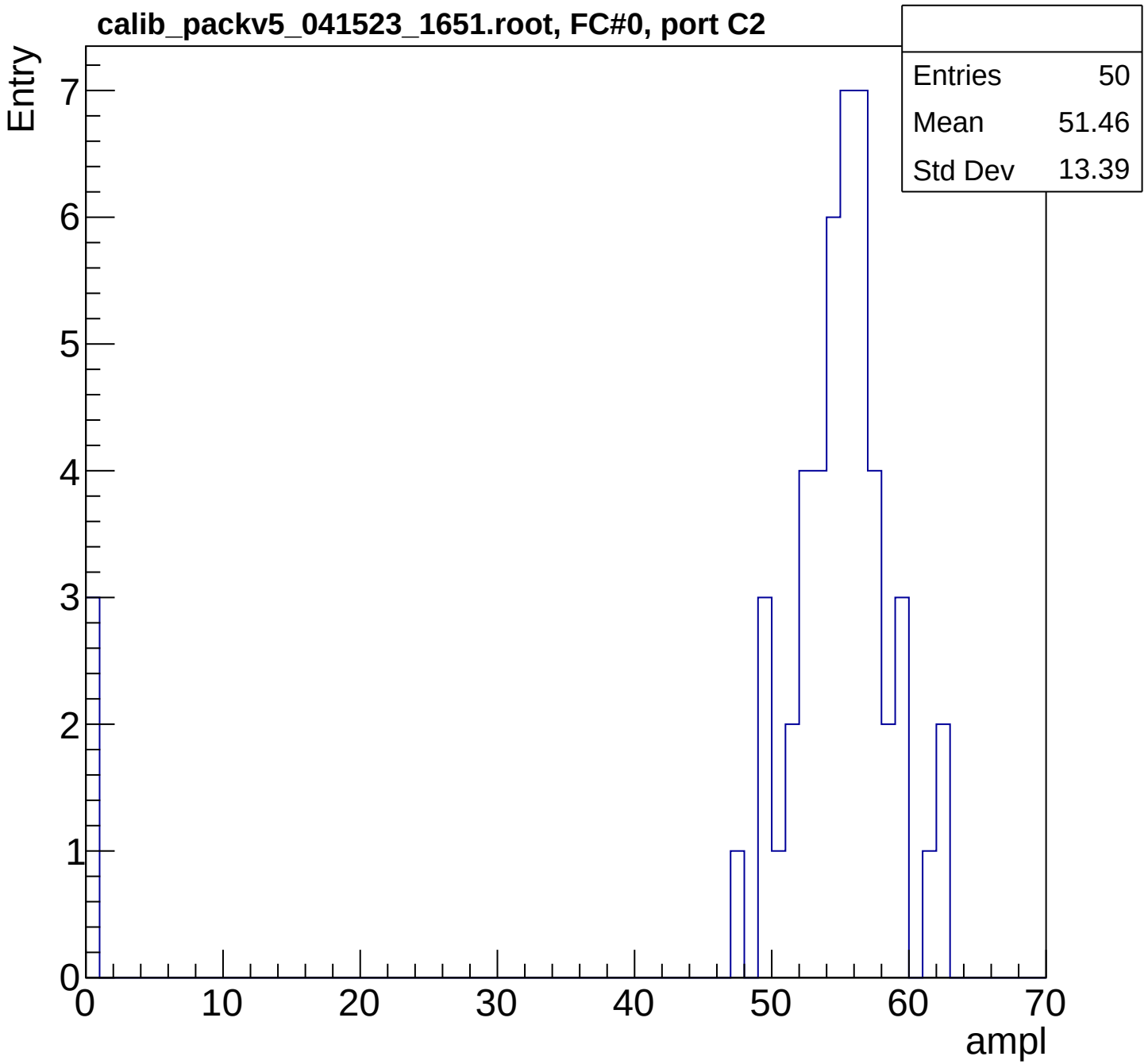

B1L103S, U17-ch84, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

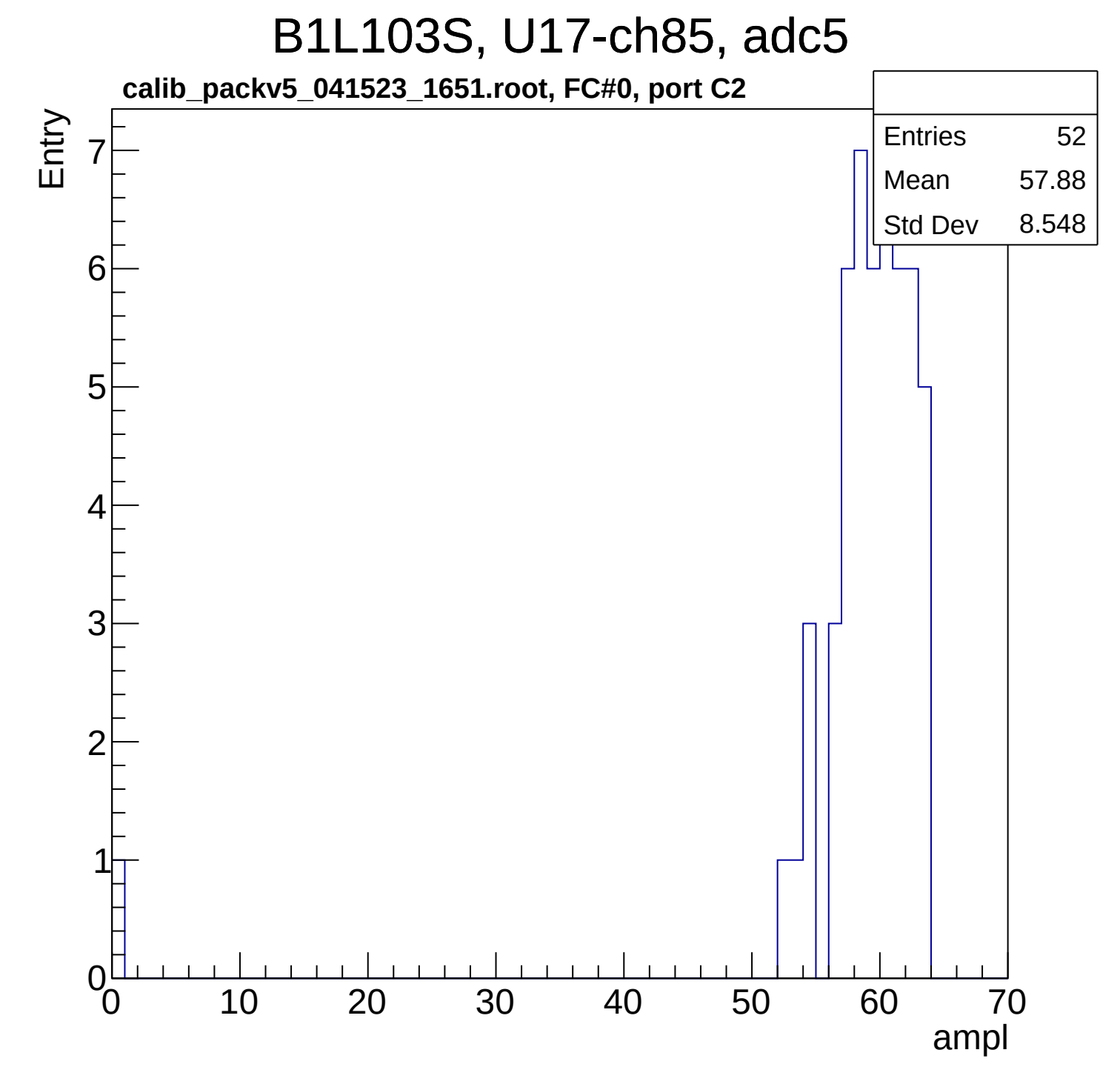

B1L103S, U17-ch85, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 25.93
Std Dev 10.05
Gaus mean : 29.9546
Gaus Width: 3.7758
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

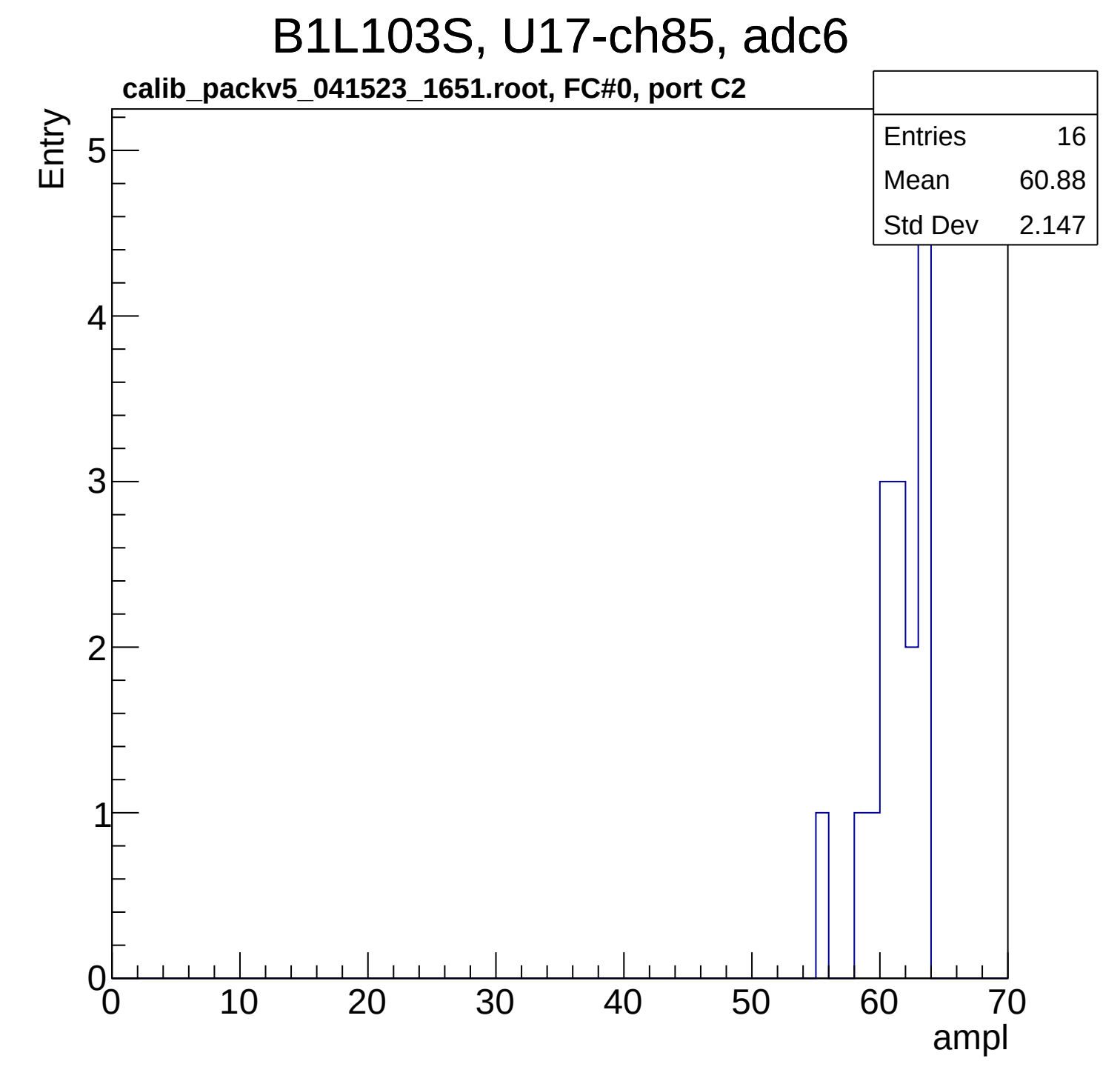

B1L103S, U17-ch85, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 34.91
Std Dev 6.27
Gaus mean : 36.4762
Gaus Width: 3.4713
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

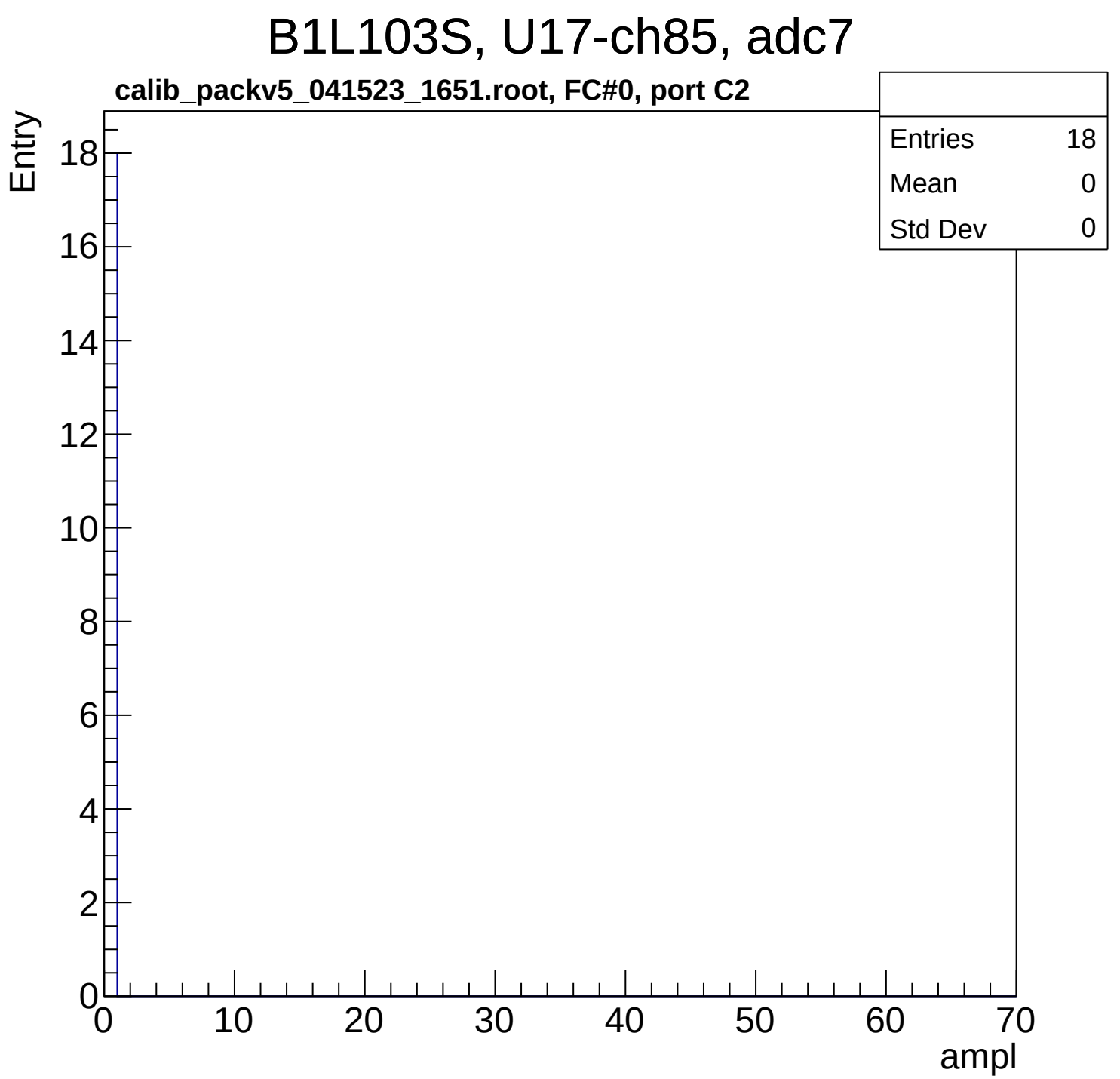

B1L103S, U17-ch85, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 41.67
Std Dev 3.941
Gaus mean : 41.7582
Gaus Width: 3.7788
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

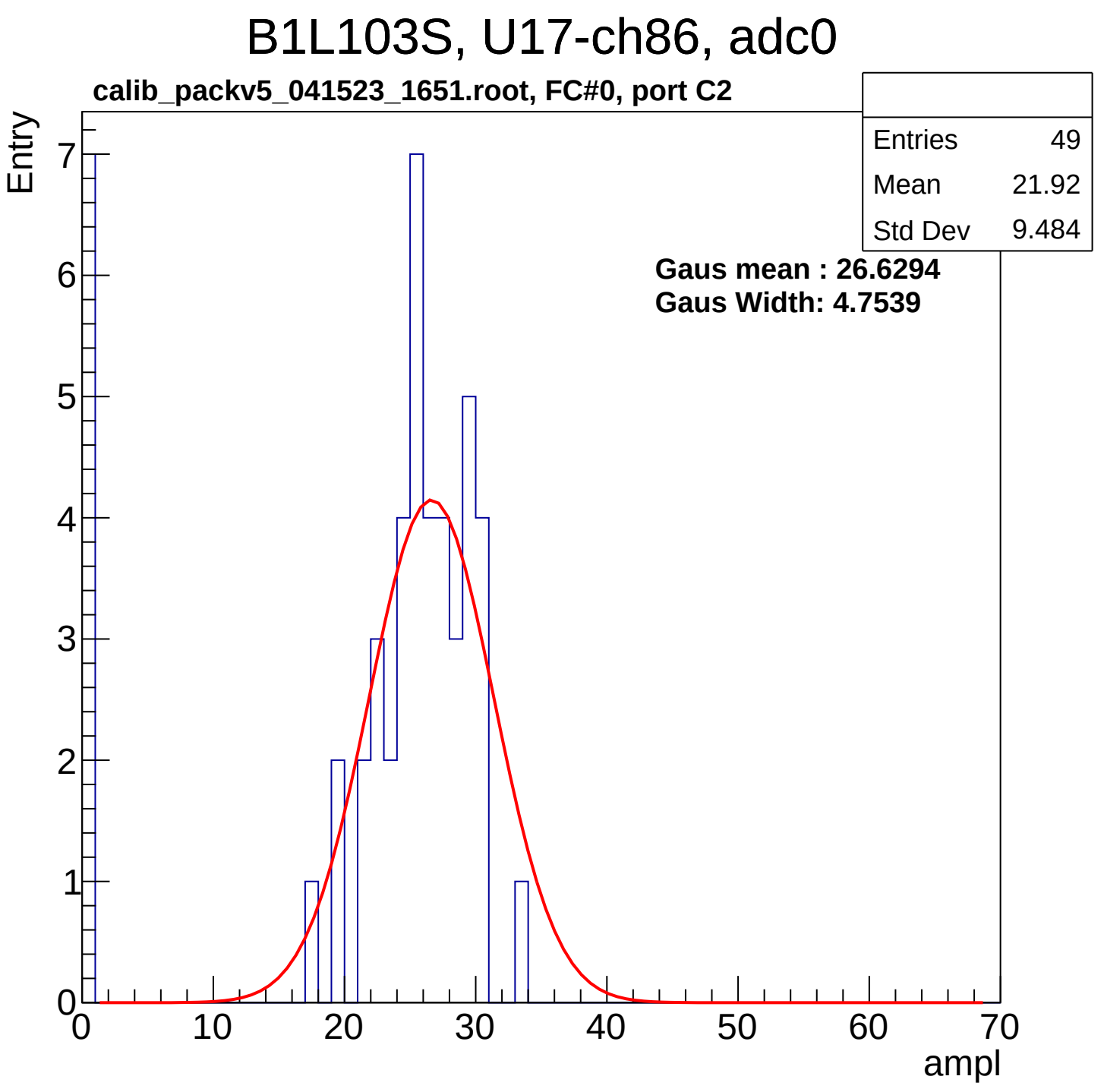

B1L103S, U17-ch85, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 41.65
Std Dev 17.01
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

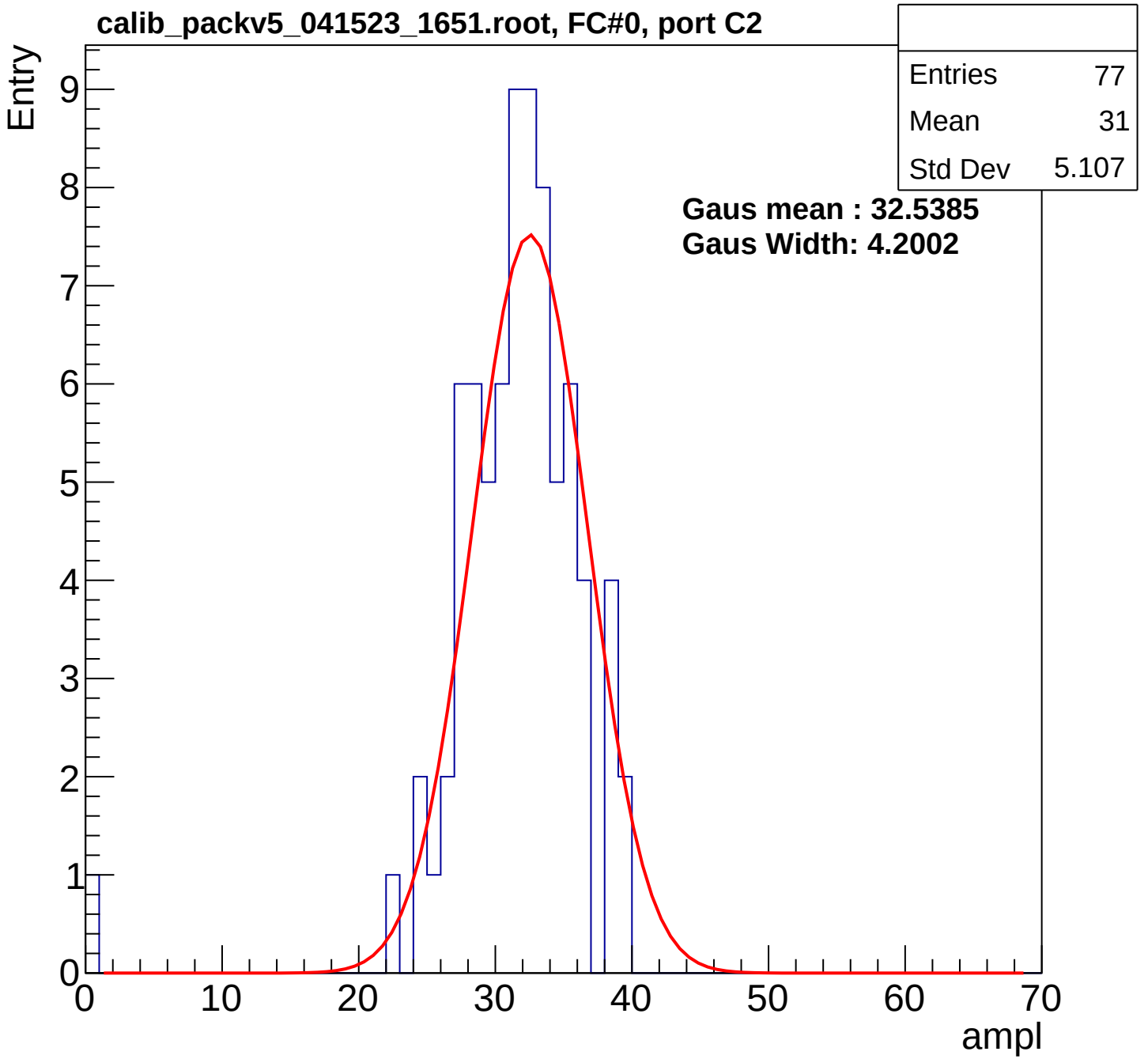

B1L103S, U17-ch85, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 51.46
Std Dev 13.39
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

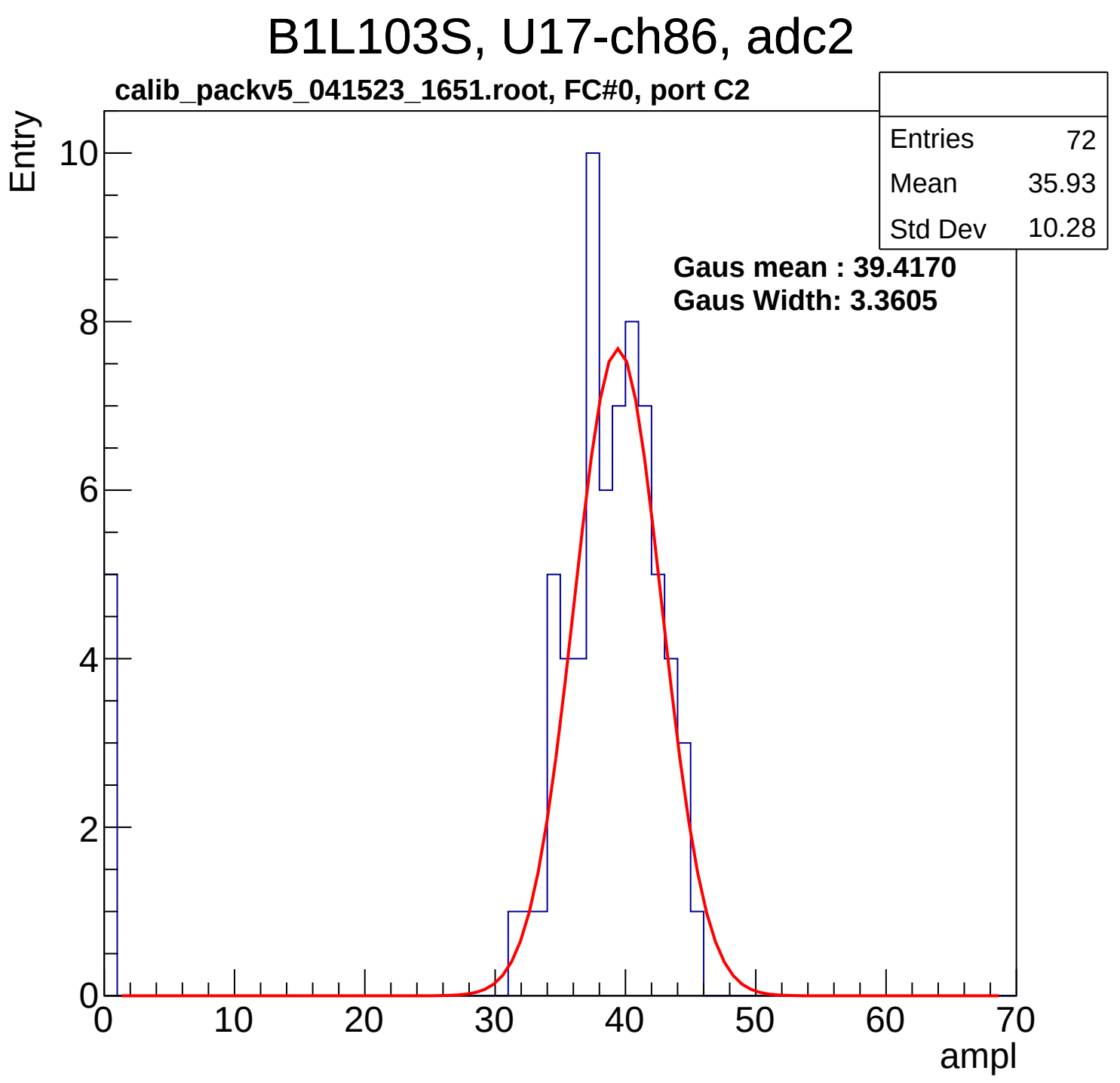

B1L103S, U17-ch85, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 57.88
Std Dev 8.548
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

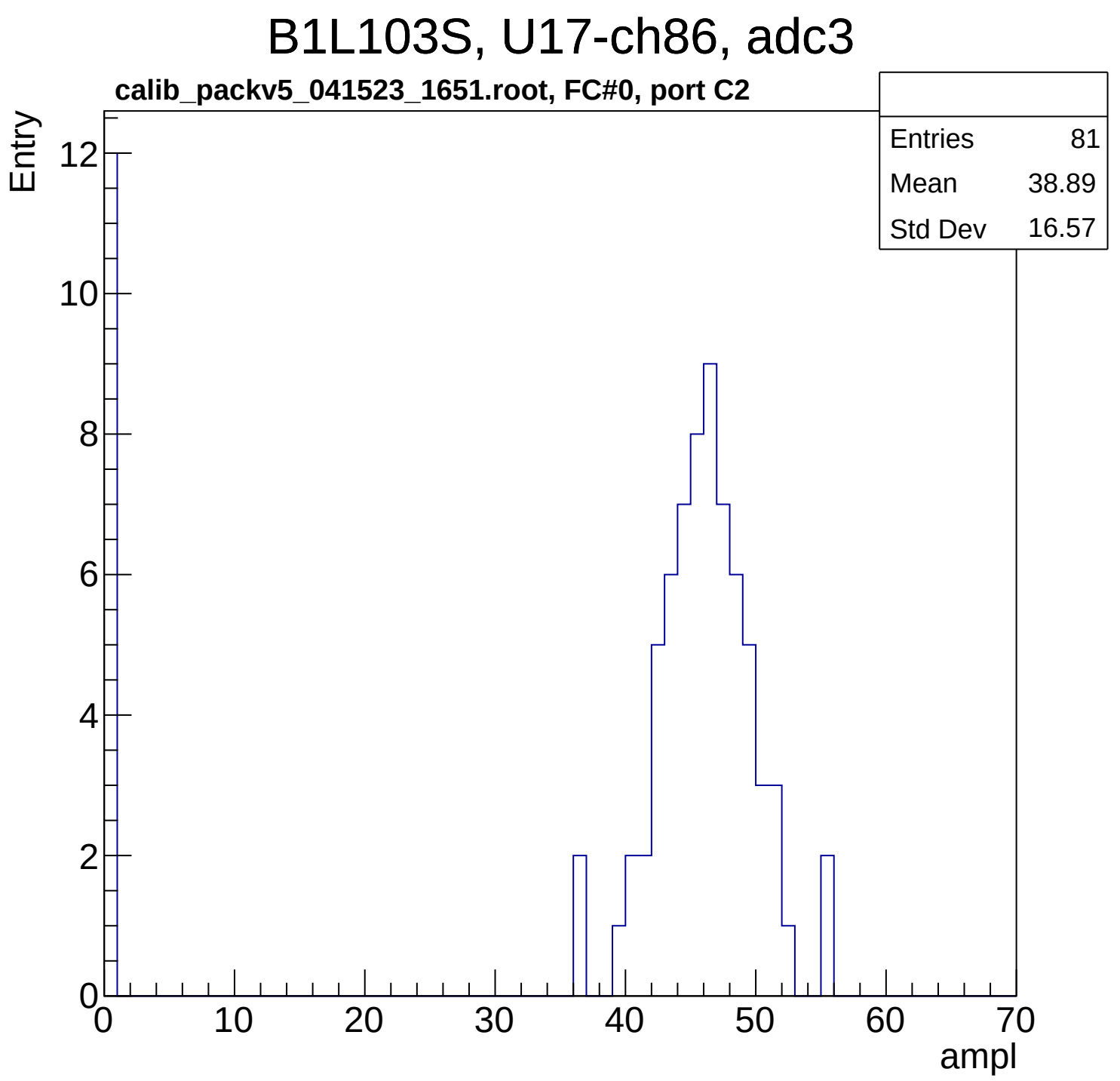

B1L103S, U17-ch85, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 60.88
Std Dev 2.147
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

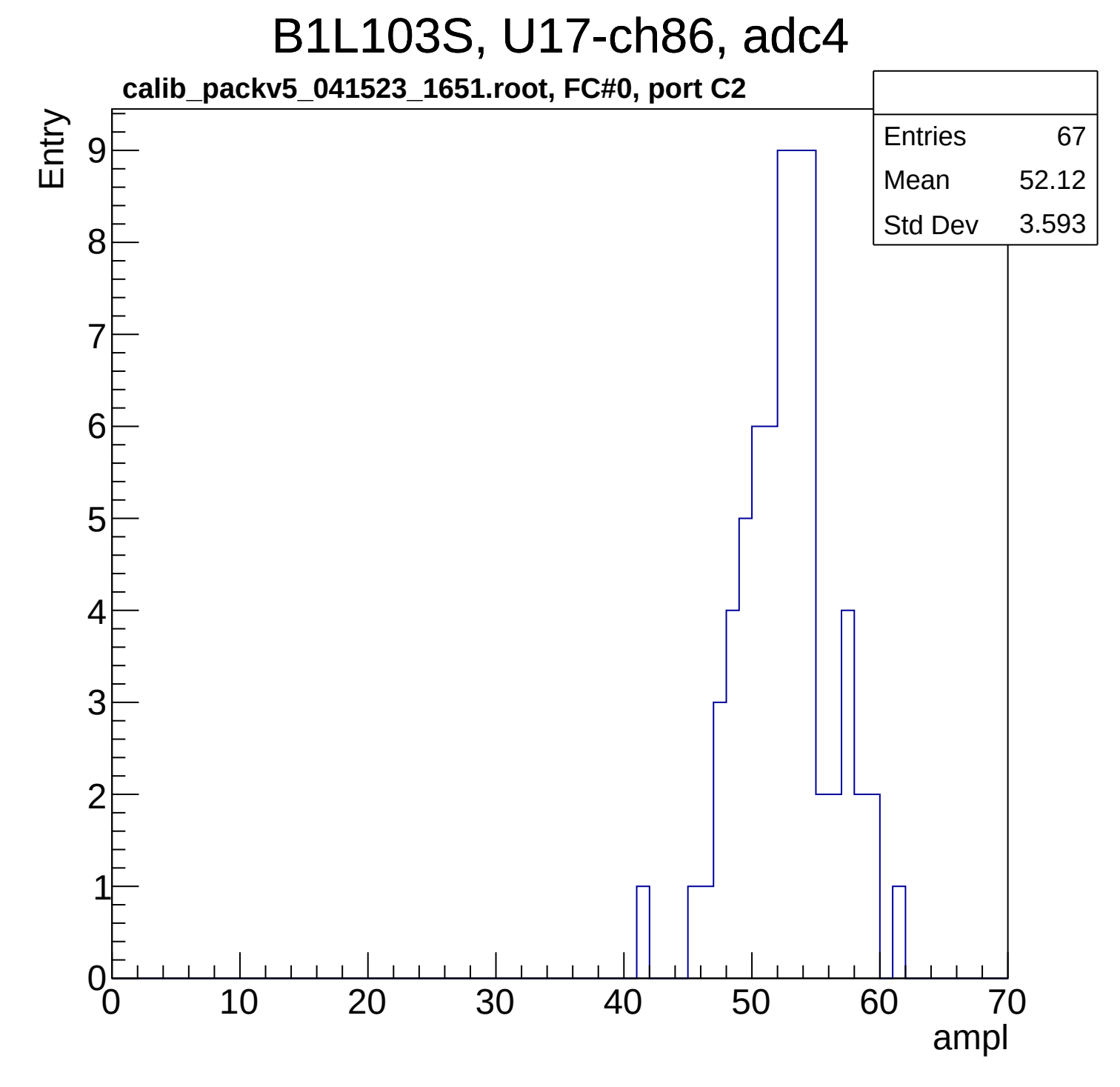

B1L103S, U17-ch85, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

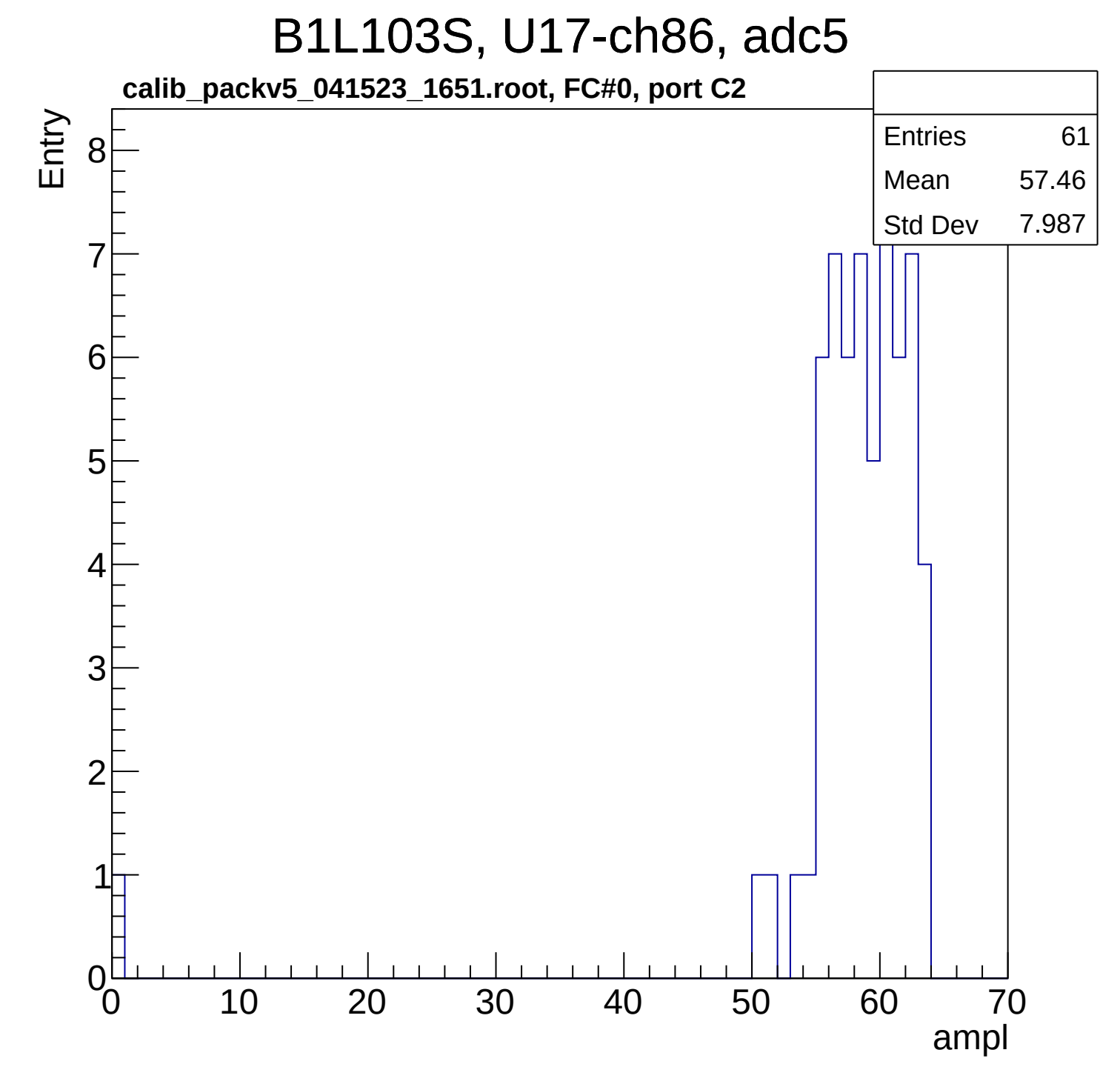

B1L103S, U17-ch86, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 21.92
Std Dev 9.484
Gaus mean : 26.6294
Gaus Width: 4.7539
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

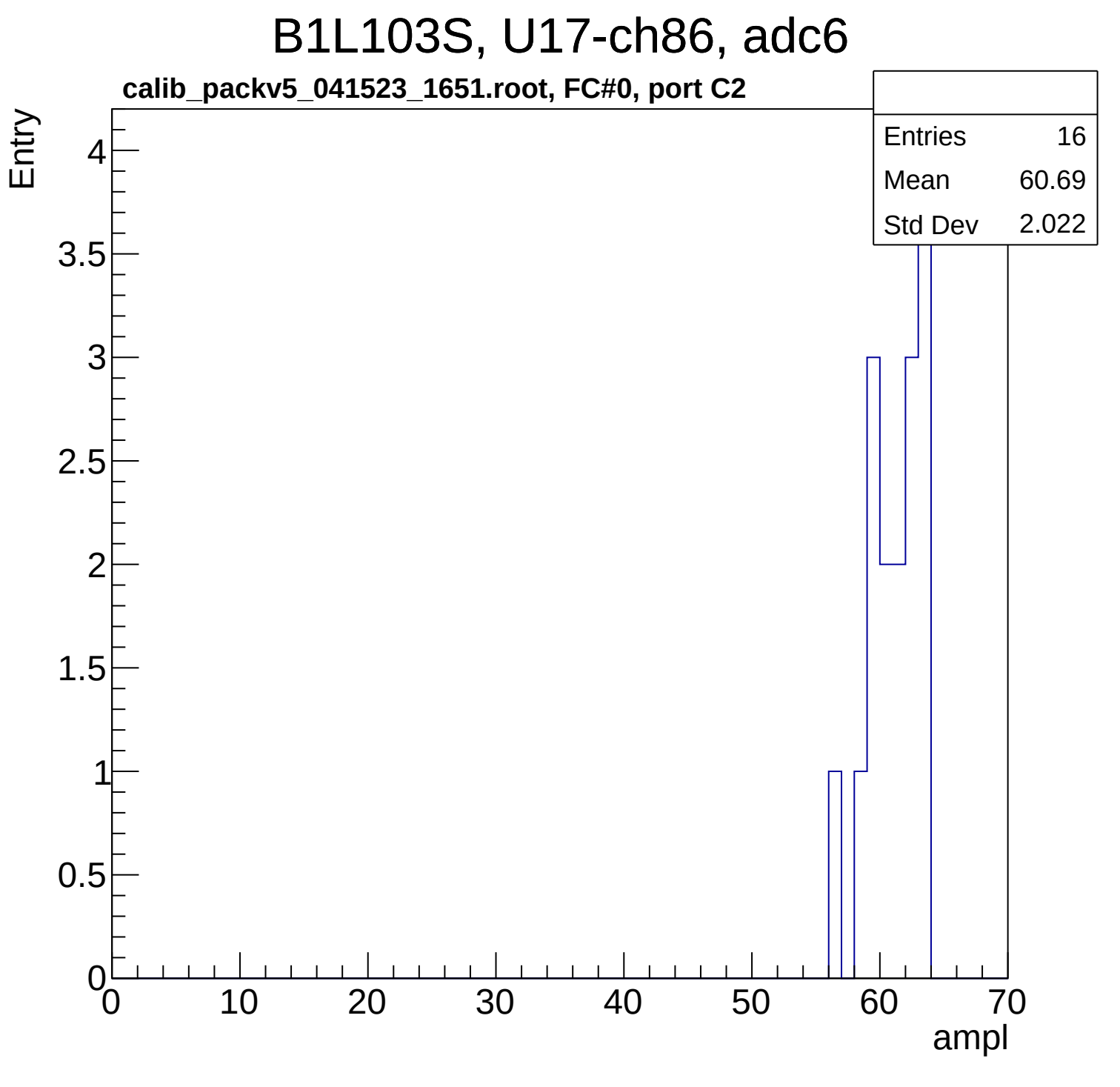

B1L103S, U17-ch86, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 31
Std Dev 5.107
Gaus mean : 32.5385
Gaus Width: 4.2002
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

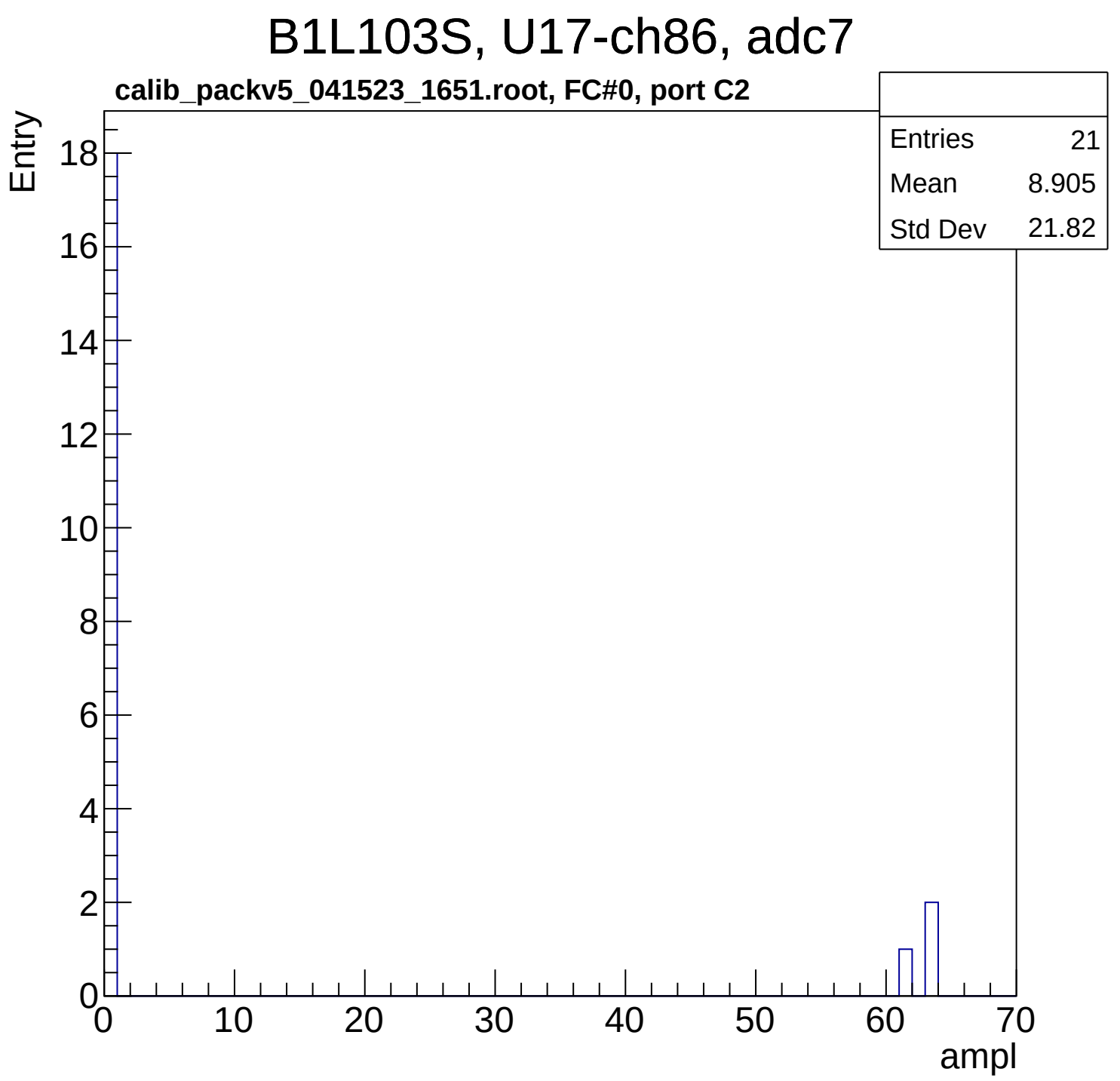

B1L103S, U17-ch86, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 35.93
Std Dev 10.28
Gaus mean : 39.4170
Gaus Width: 3.3605
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

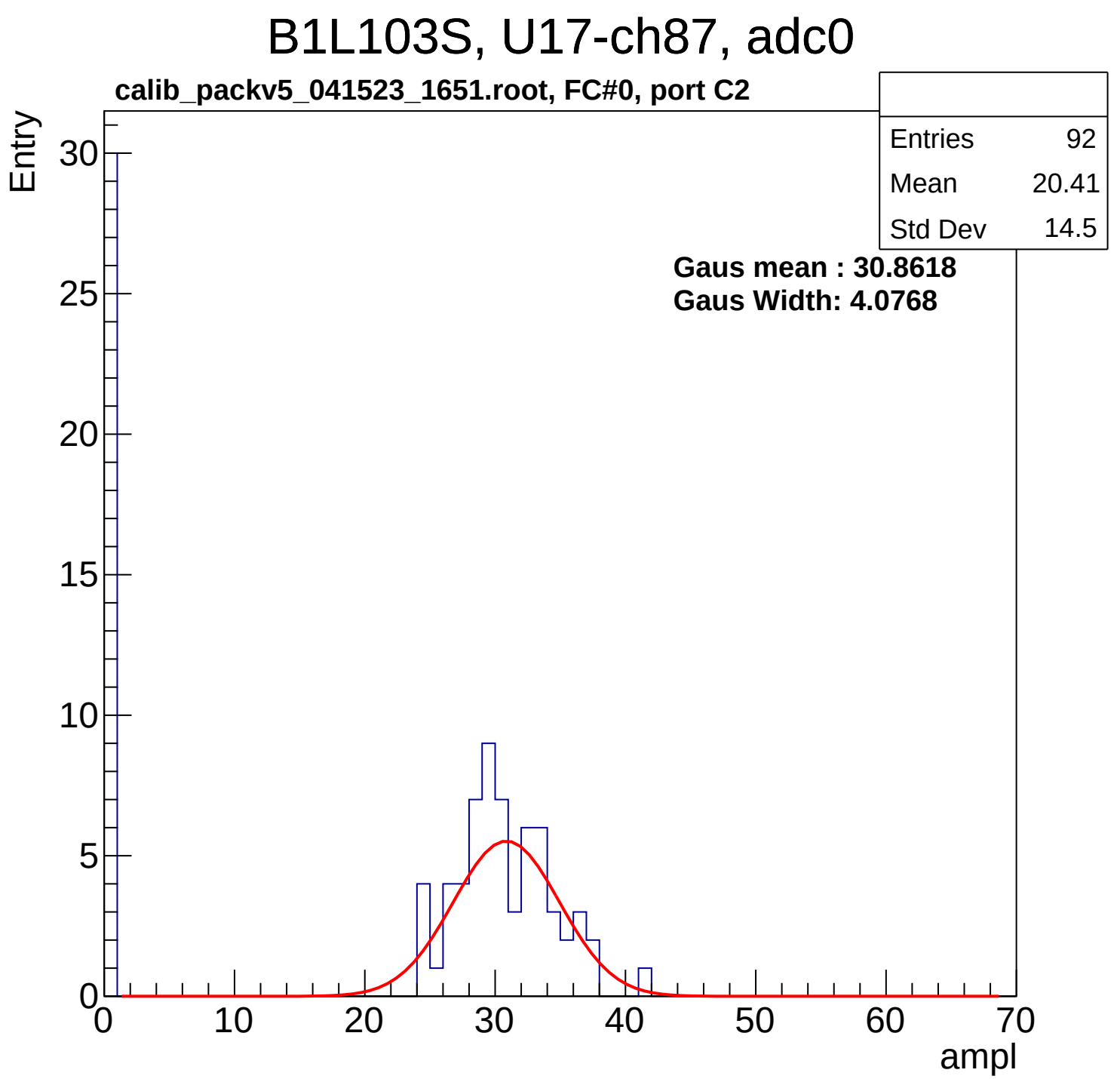

B1L103S, U17-ch86, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 38.89
Std Dev 16.57
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

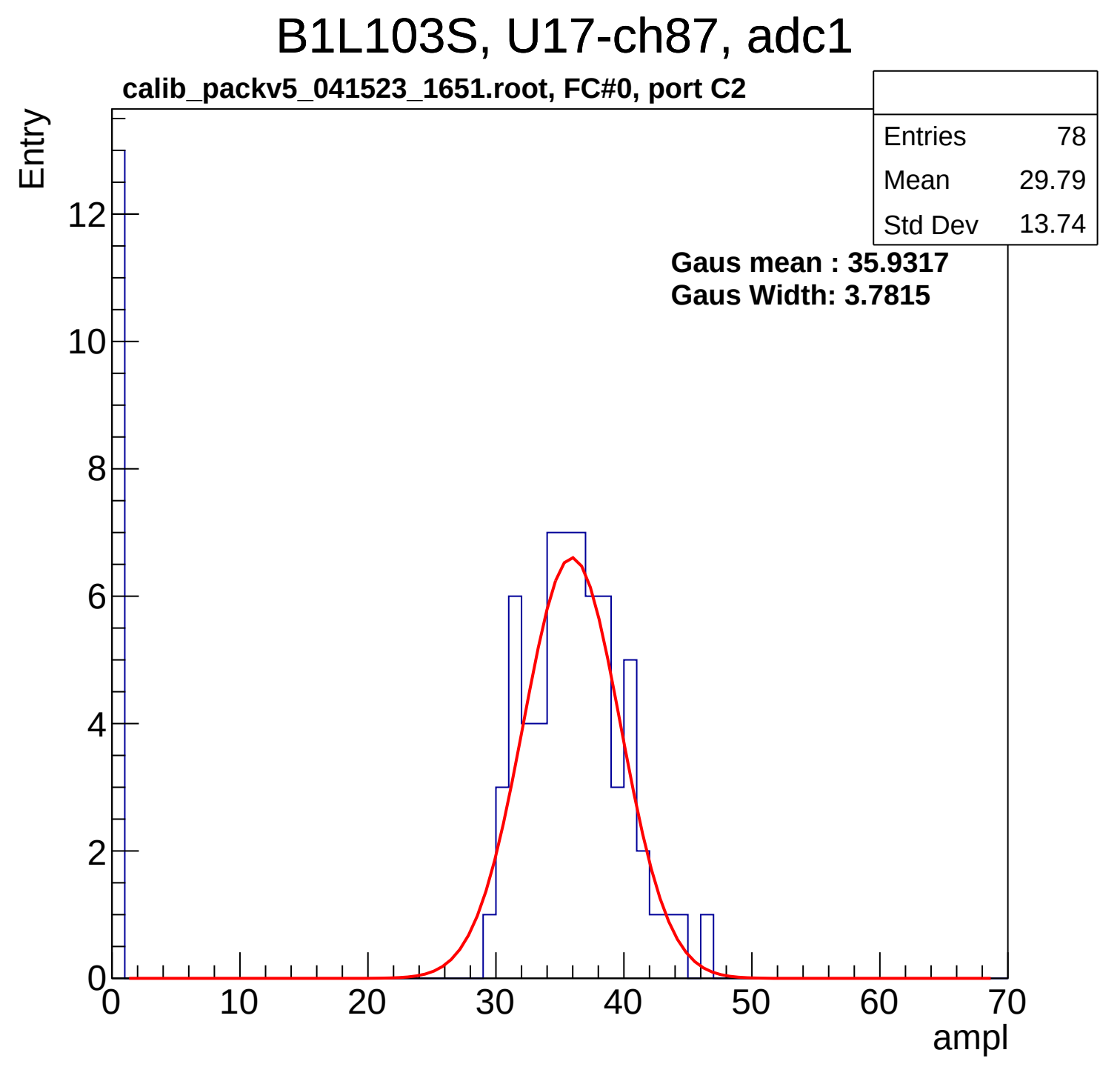

B1L103S, U17-ch86, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 52.12
Std Dev 3.593
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

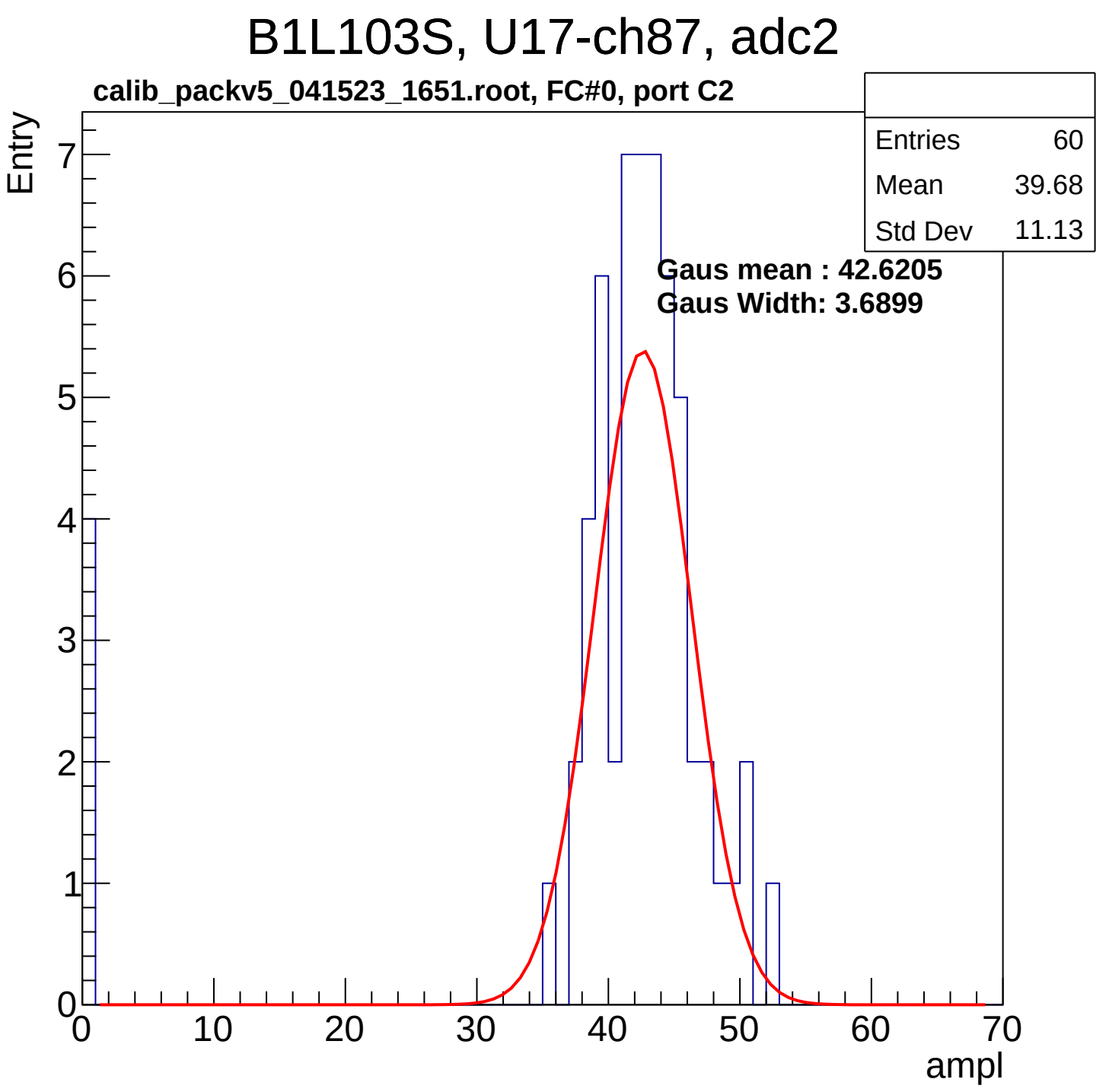

B1L103S, U17-ch86, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 57.46
Std Dev 7.987
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

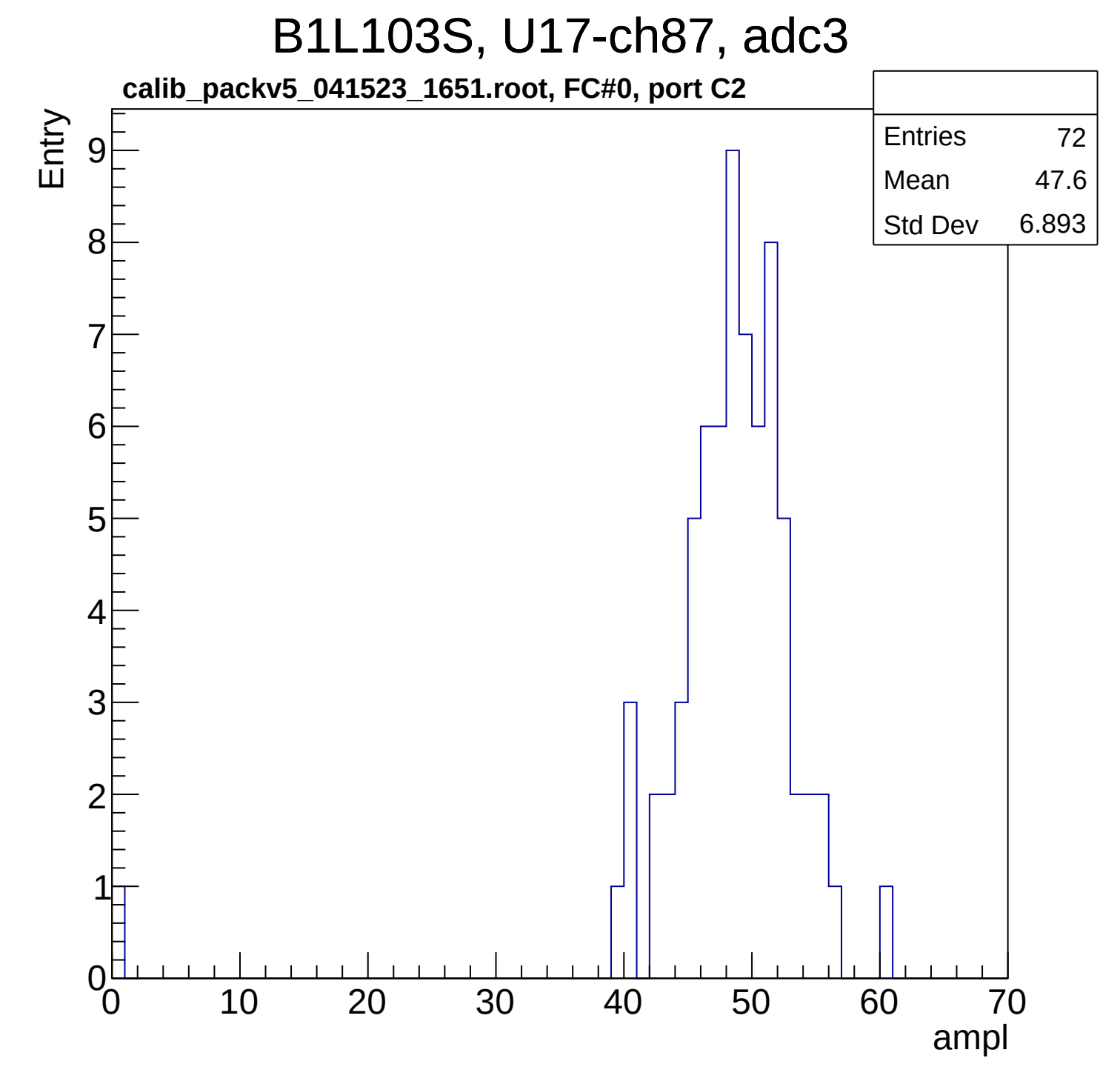

B1L103S, U17-ch86, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 60.69
Std Dev 2.022
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

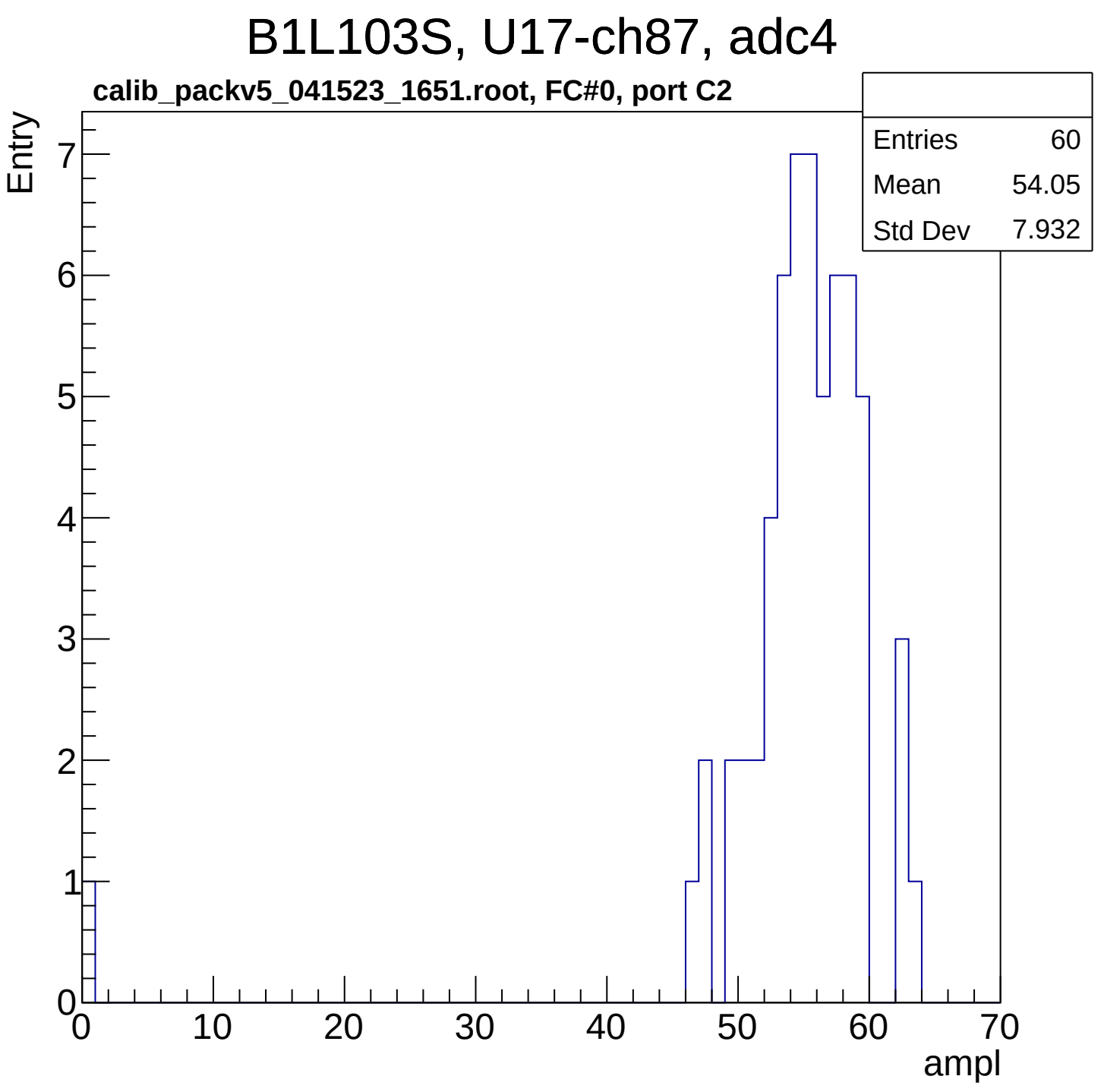

B1L103S, U17-ch86, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 8.905
Std Dev 21.82
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

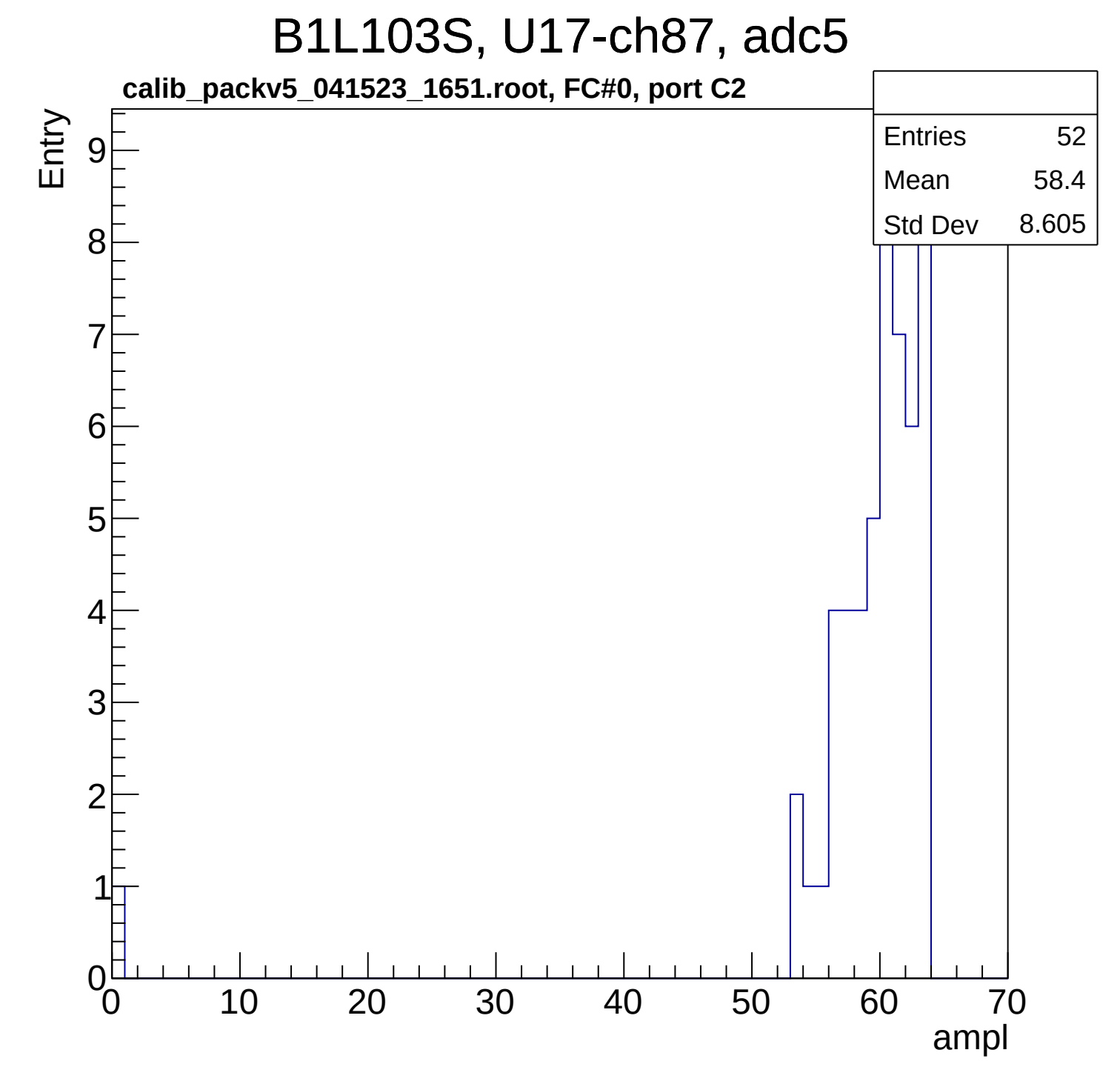

B1L103S, U17-ch87, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 20.41
Std Dev 14.5
Gaus mean : 30.8618
Gaus Width: 4.0768
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70

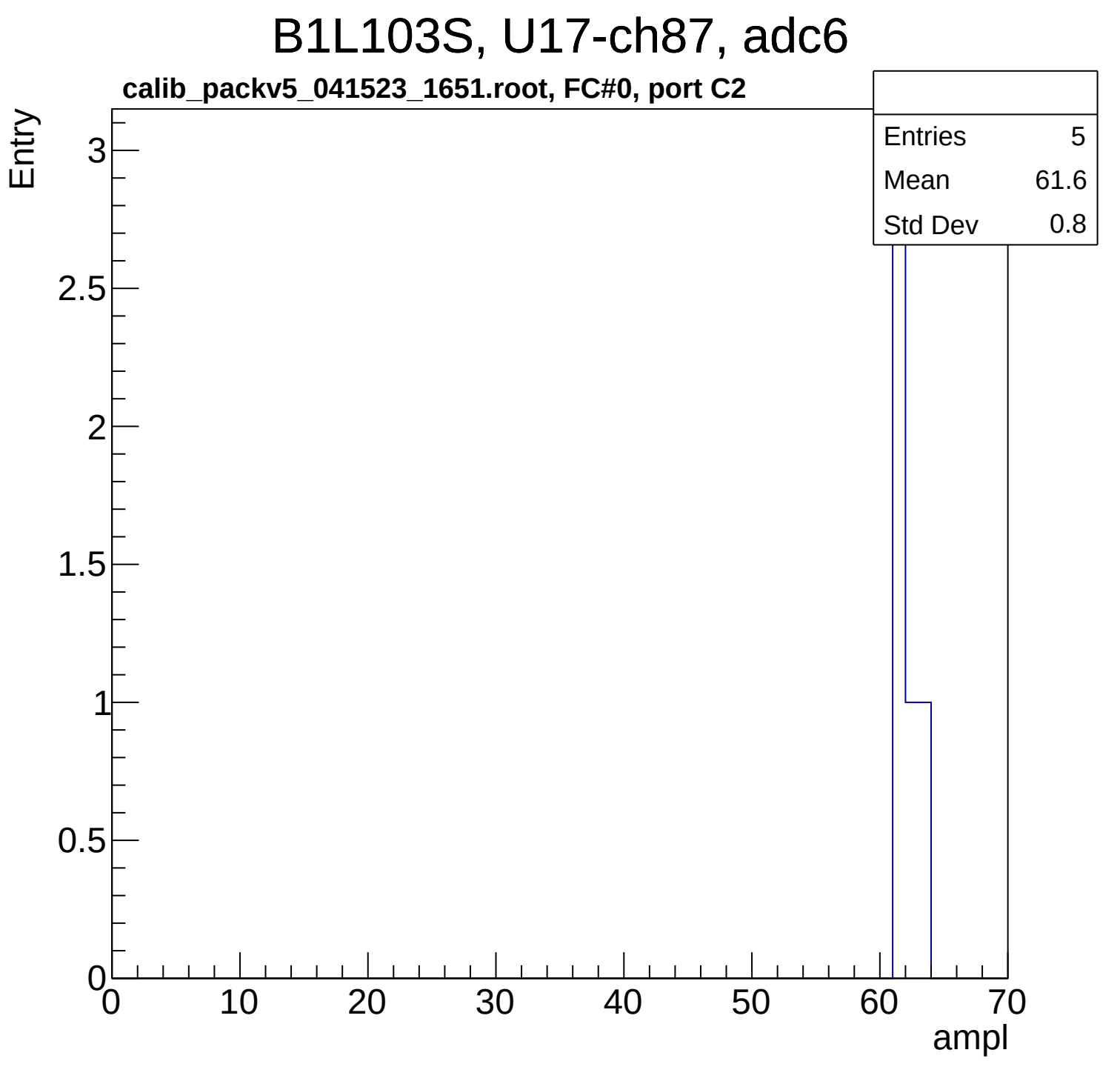

B1L103S, U17-ch87, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 29.79
Std Dev 13.74
Gaus mean : 35.9317
Gaus Width: 3.7815
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

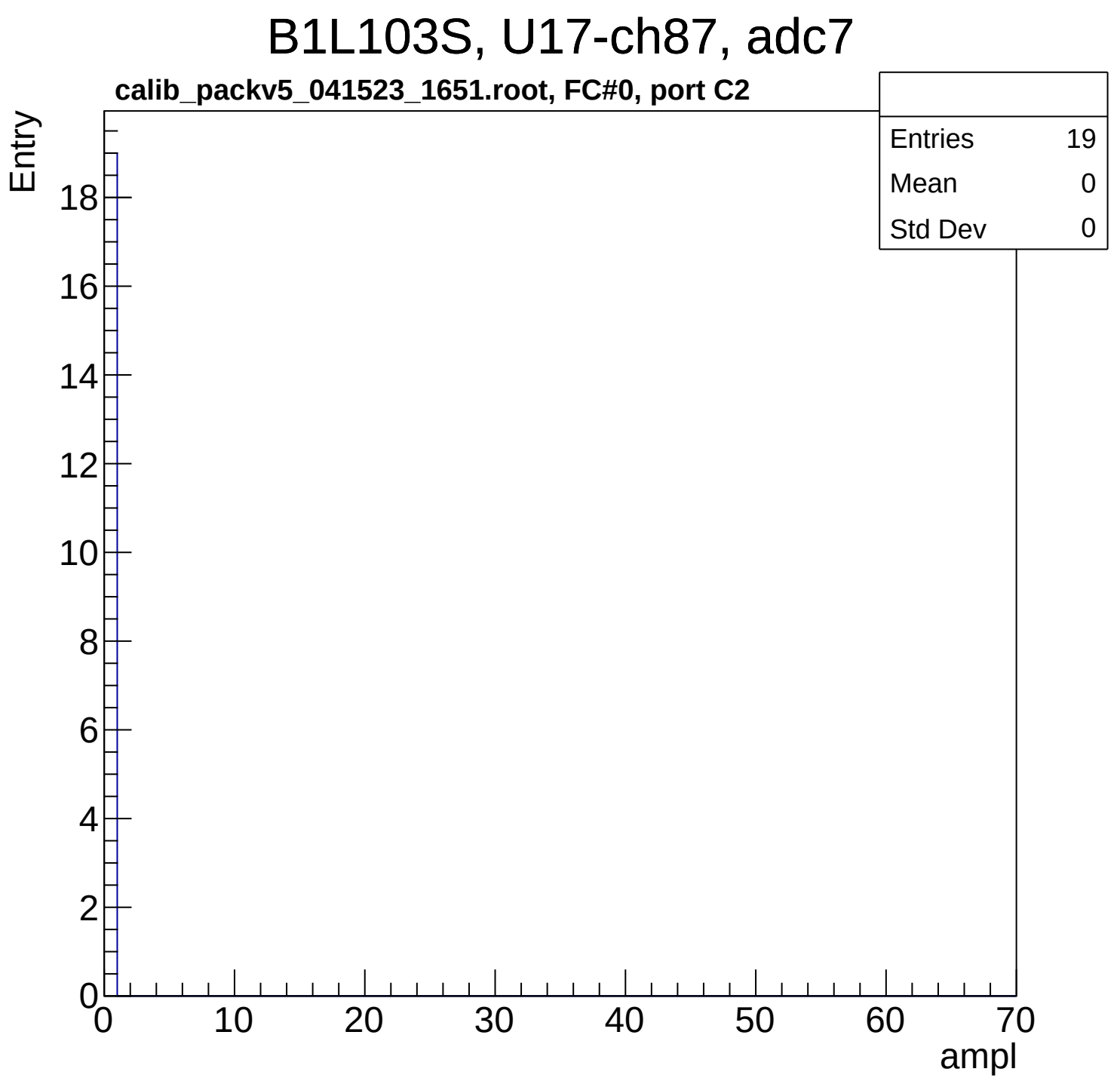

B1L103S, U17-ch87, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 39.68
Std Dev 11.13
Gaus mean : 42.6205
Gaus Width: 3.6899
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

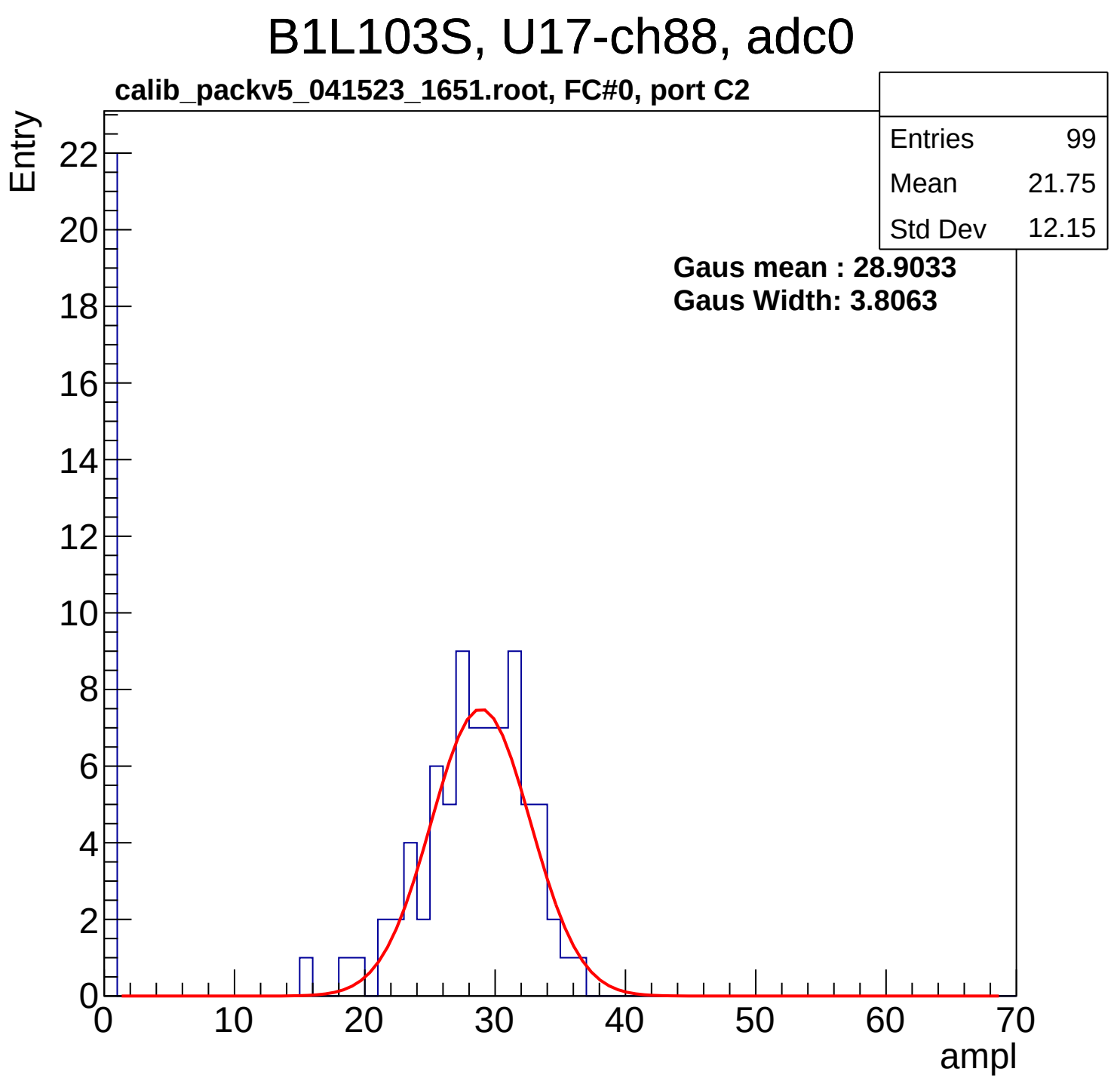

B1L103S, U17-ch87, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 47.6
Std Dev 6.893
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

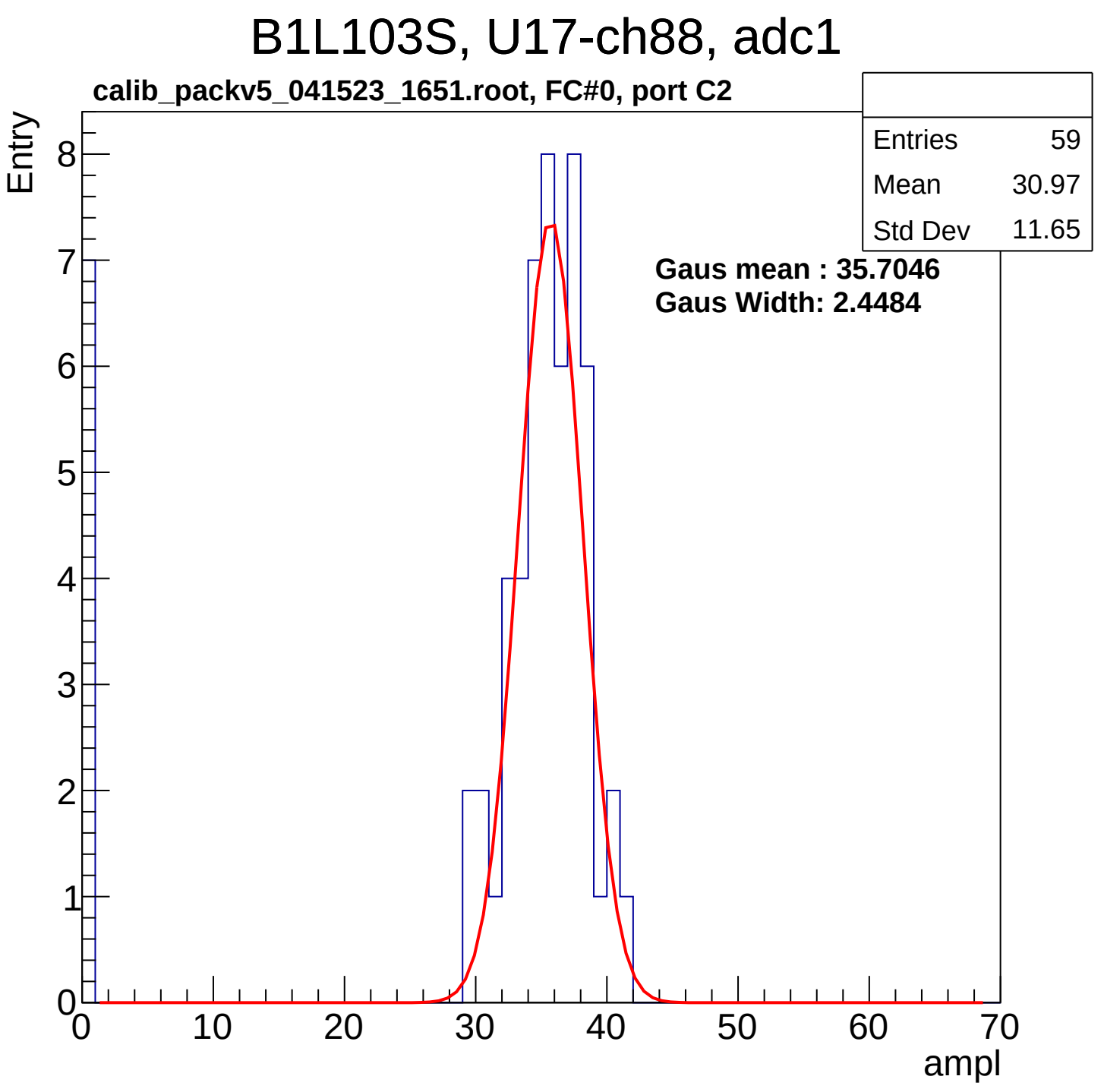

B1L103S, U17-ch87, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 54.05
Std Dev 7.932
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

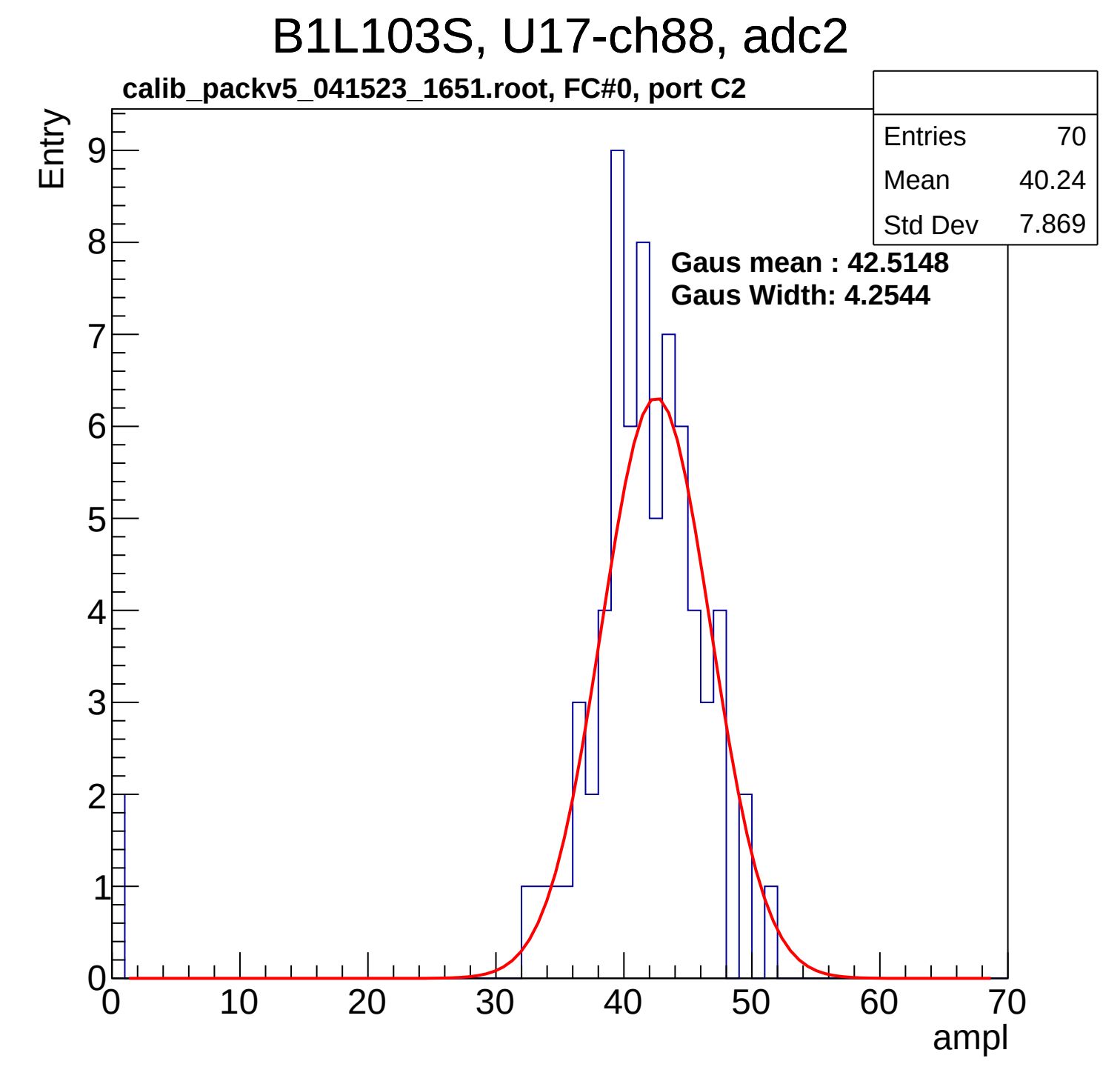

B1L103S, U17-ch87, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.4
Std Dev 8.605
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

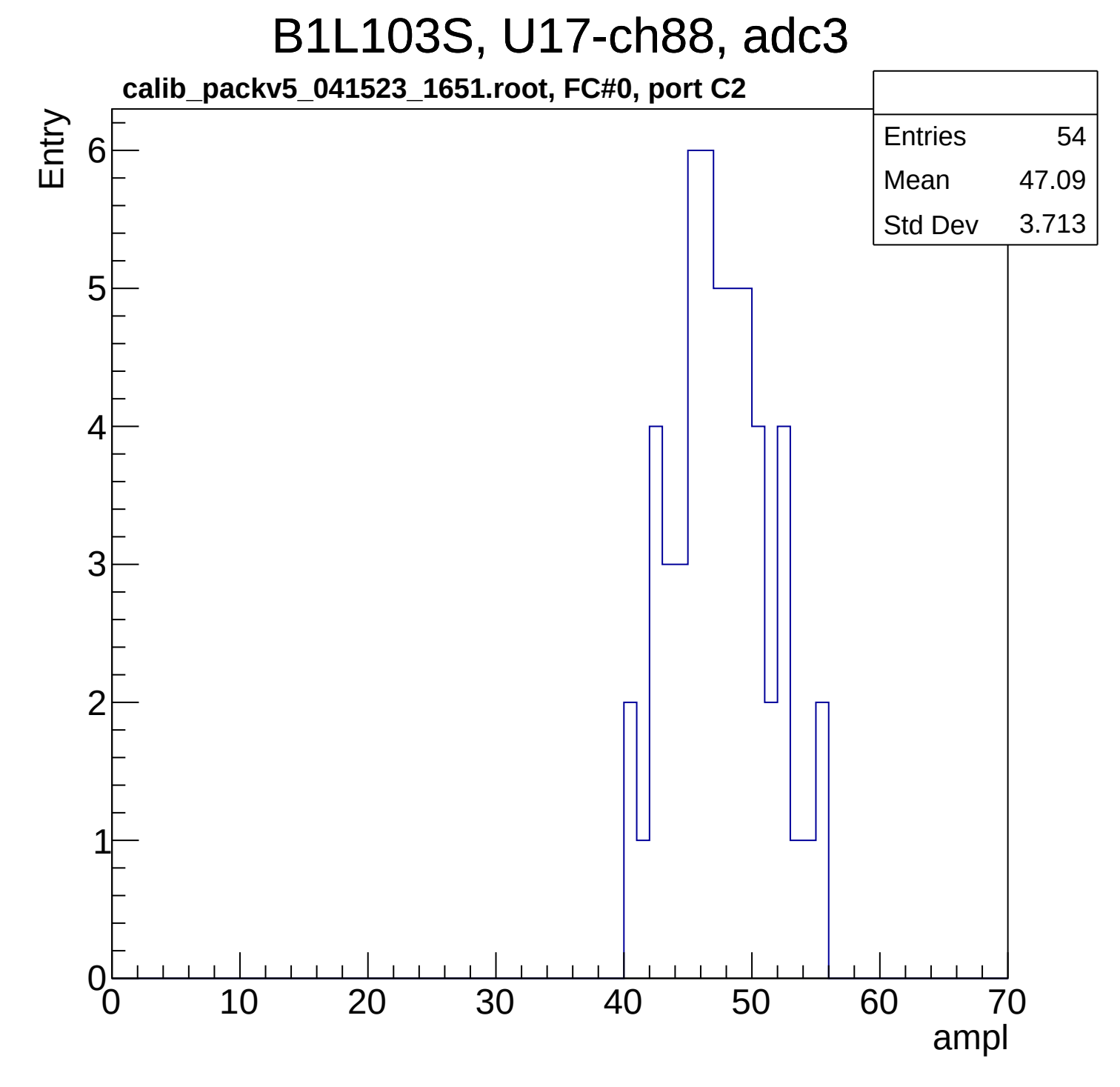

B1L103S, U17-ch87, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.6
Std Dev 0.8
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

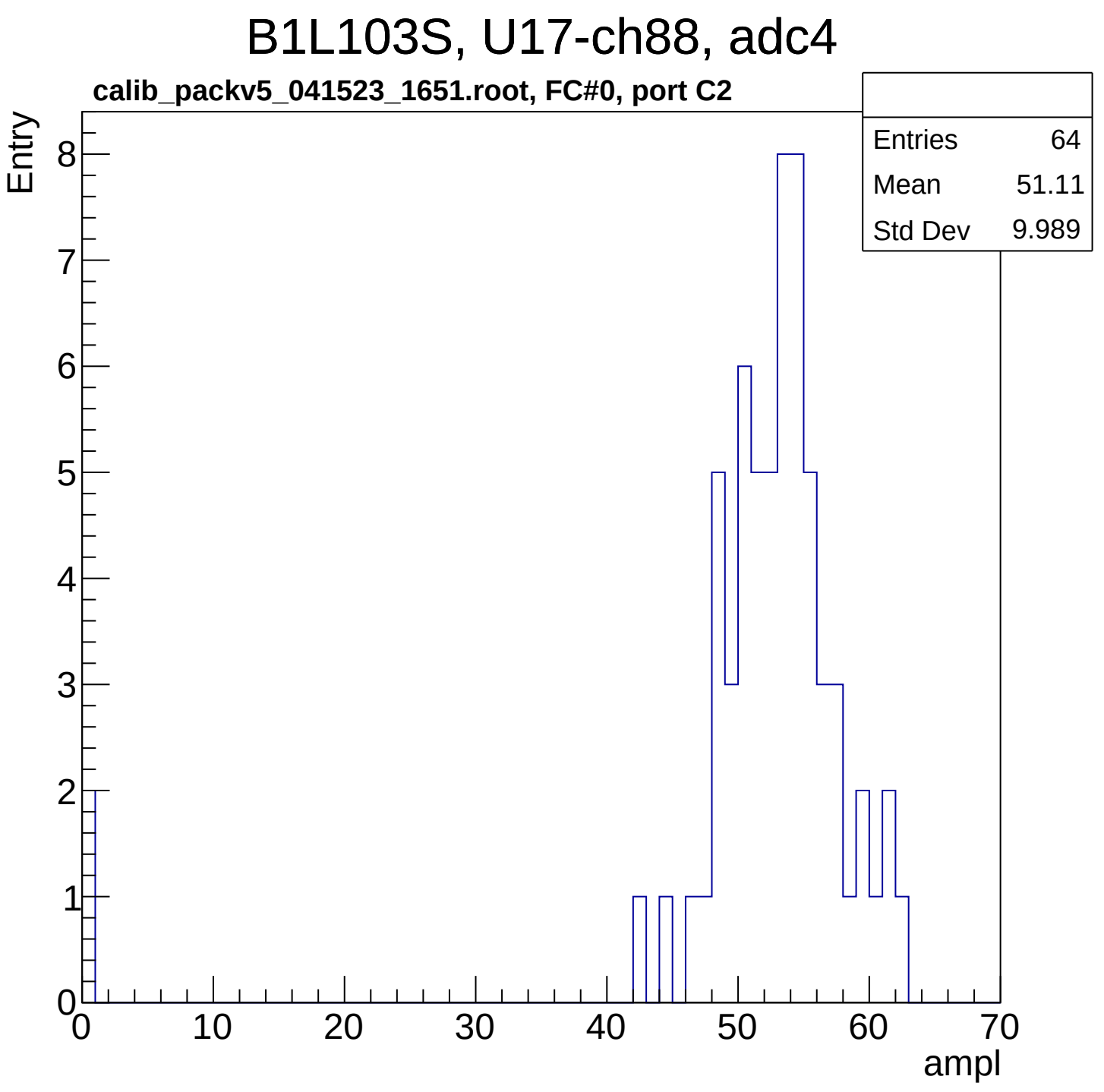

B1L103S, U17-ch87, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

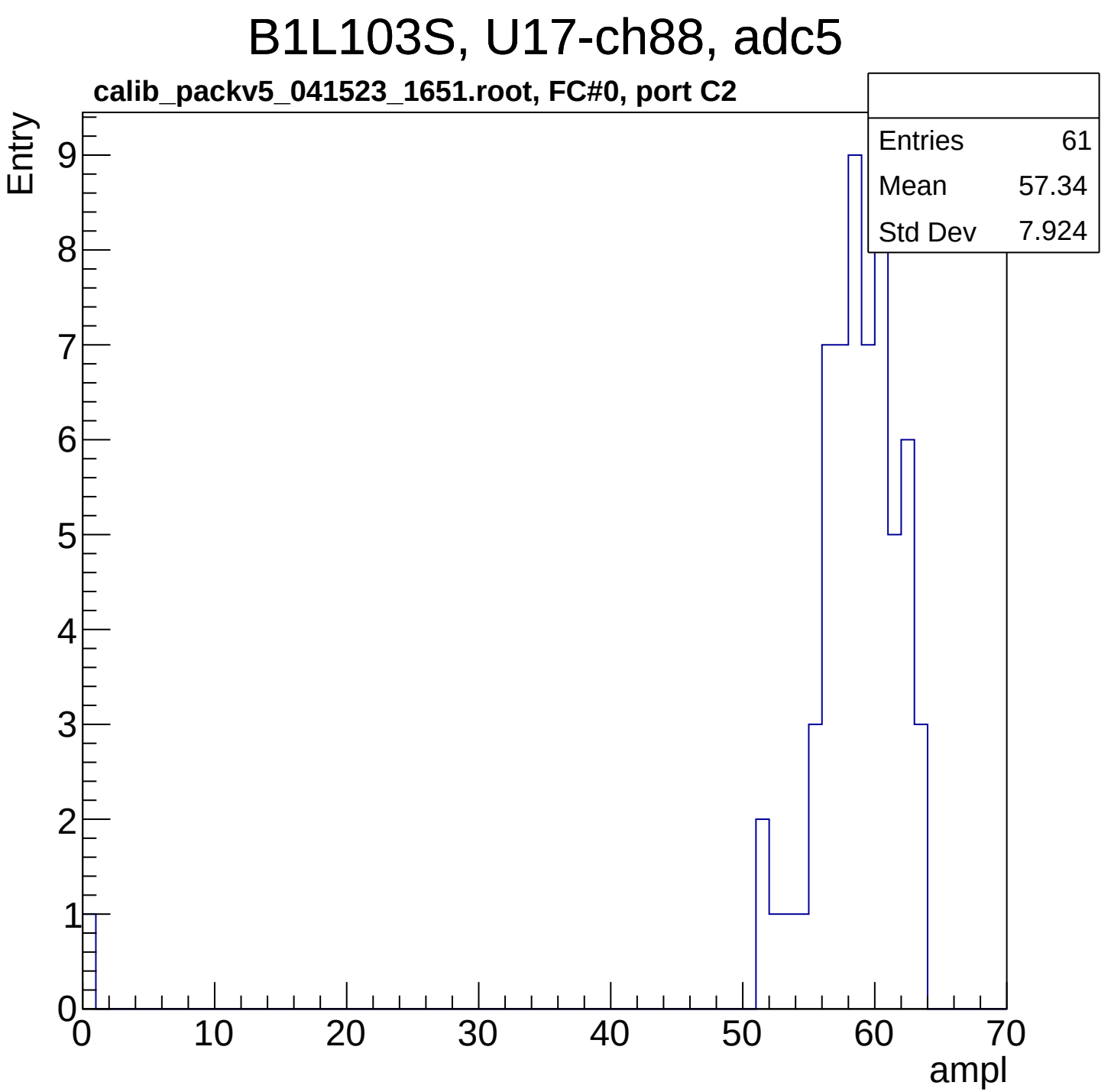

B1L103S, U17-ch88, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 21.75
Std Dev 12.15
Gaus mean : 28.9033
Gaus Width: 3.8063
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70

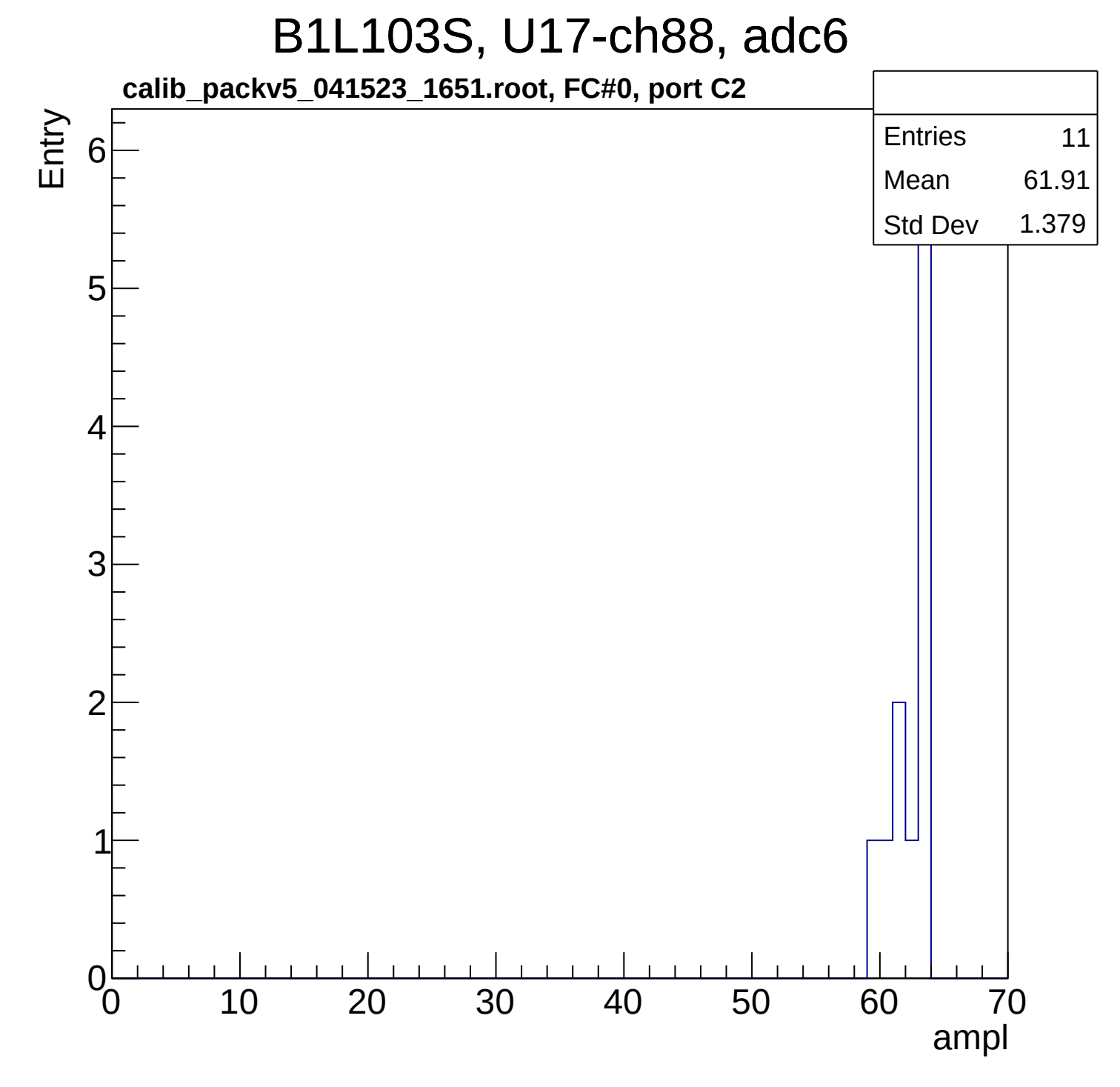

B1L103S, U17-ch88, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 30.97
Std Dev 11.65
Gaus mean : 35.7046
Gaus Width: 2.4484
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

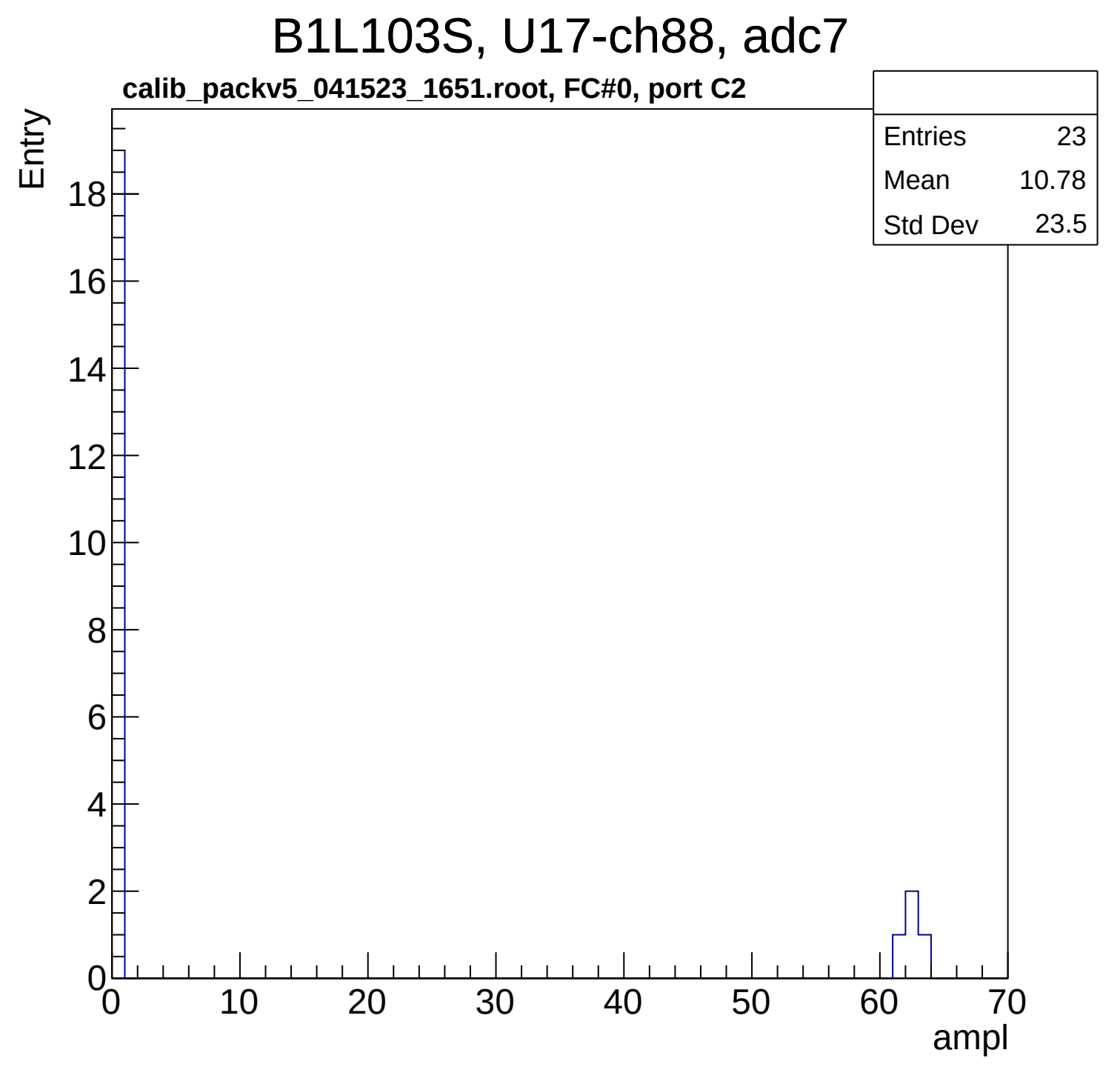

B1L103S, U17-ch88, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 40.24
Std Dev 7.869
Gaus mean : 42.5148
Gaus Width: 4.2544
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

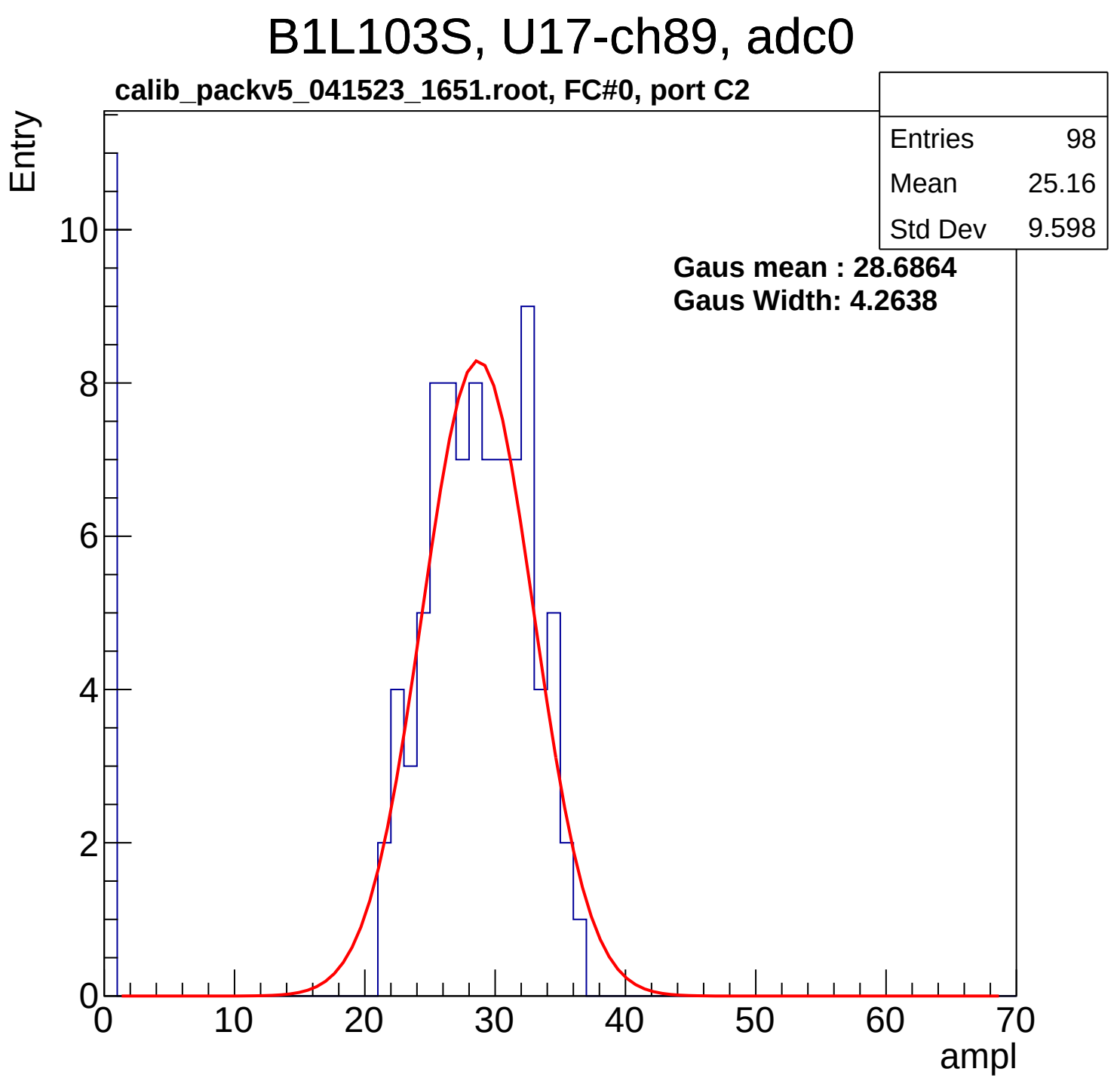

B1L103S, U17-ch88, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 47.09
Std Dev 3.713
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

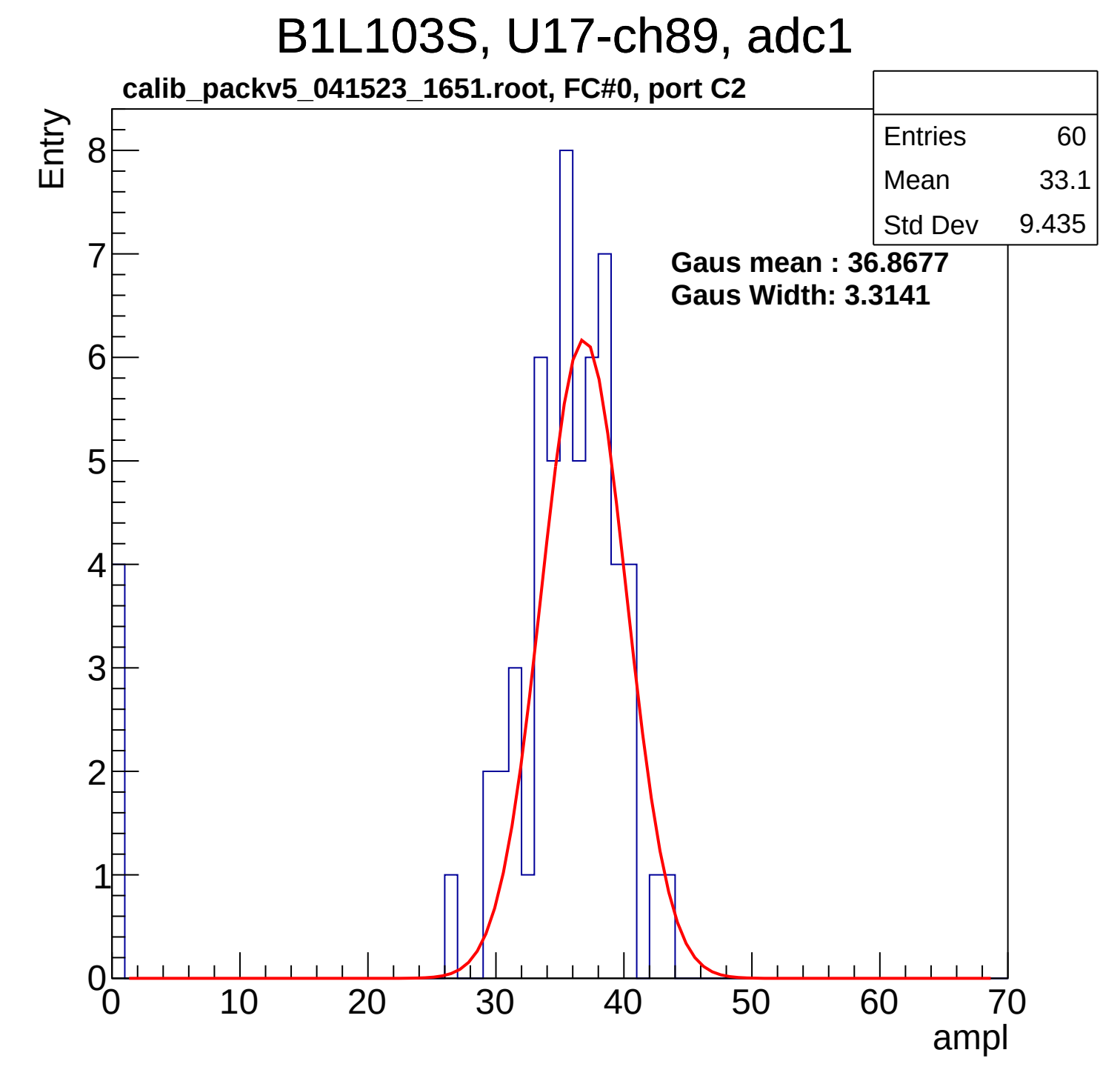

B1L103S, U17-ch88, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 51.11
Std Dev 9.989
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

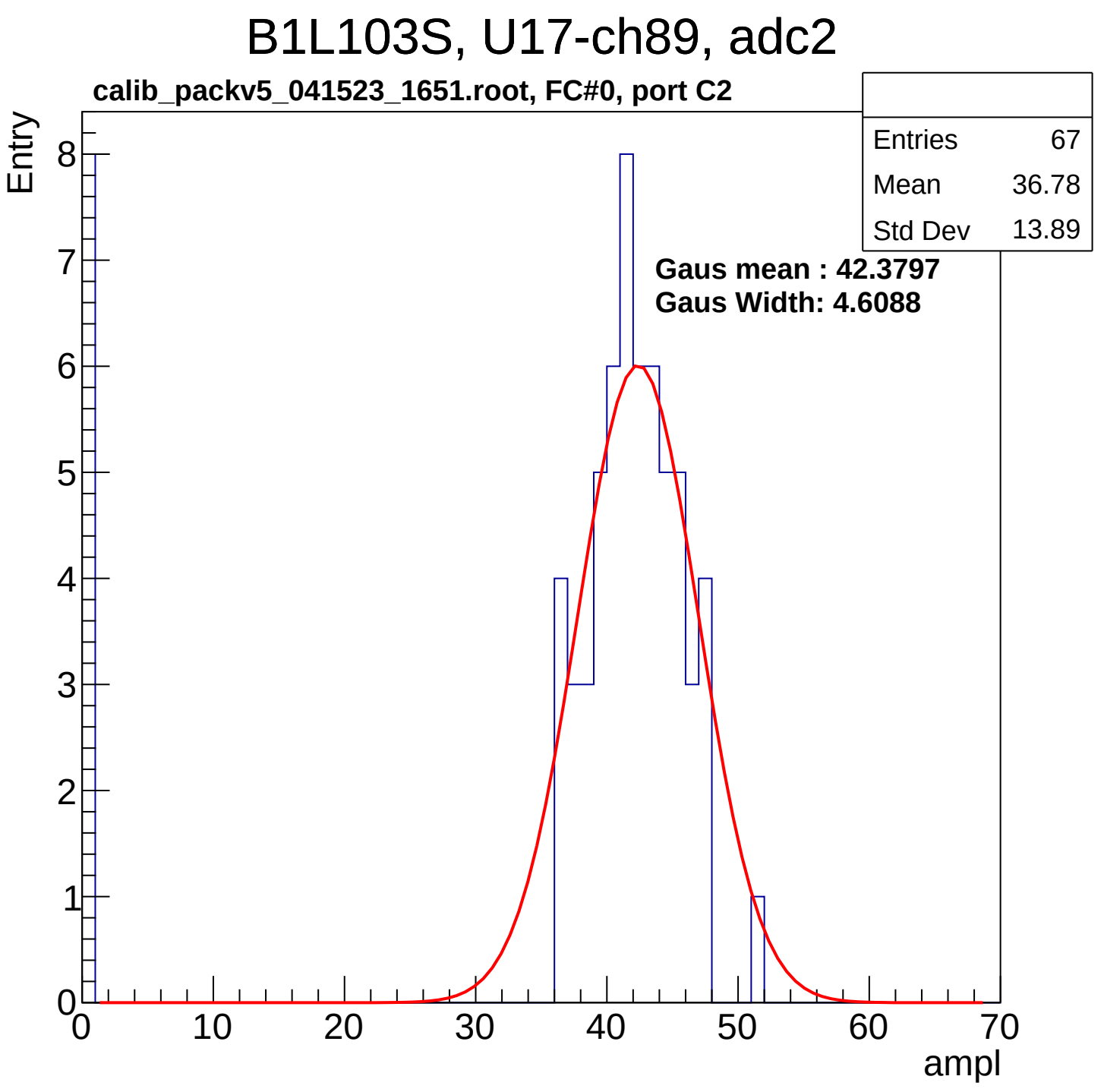

B1L103S, U17-ch88, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 57.34
Std Dev 7.924
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

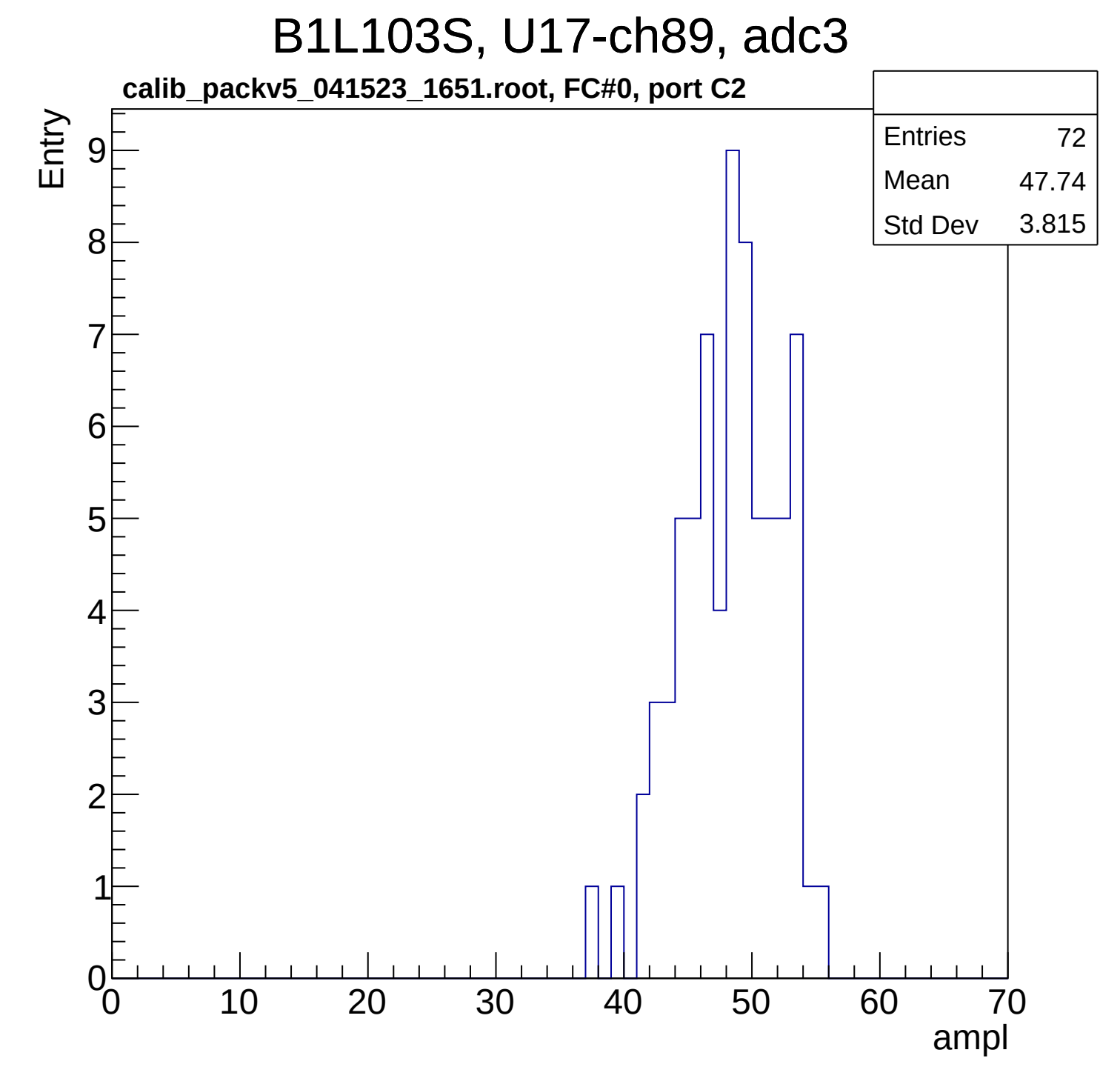

B1L103S, U17-ch88, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.91
Std Dev 1.379
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

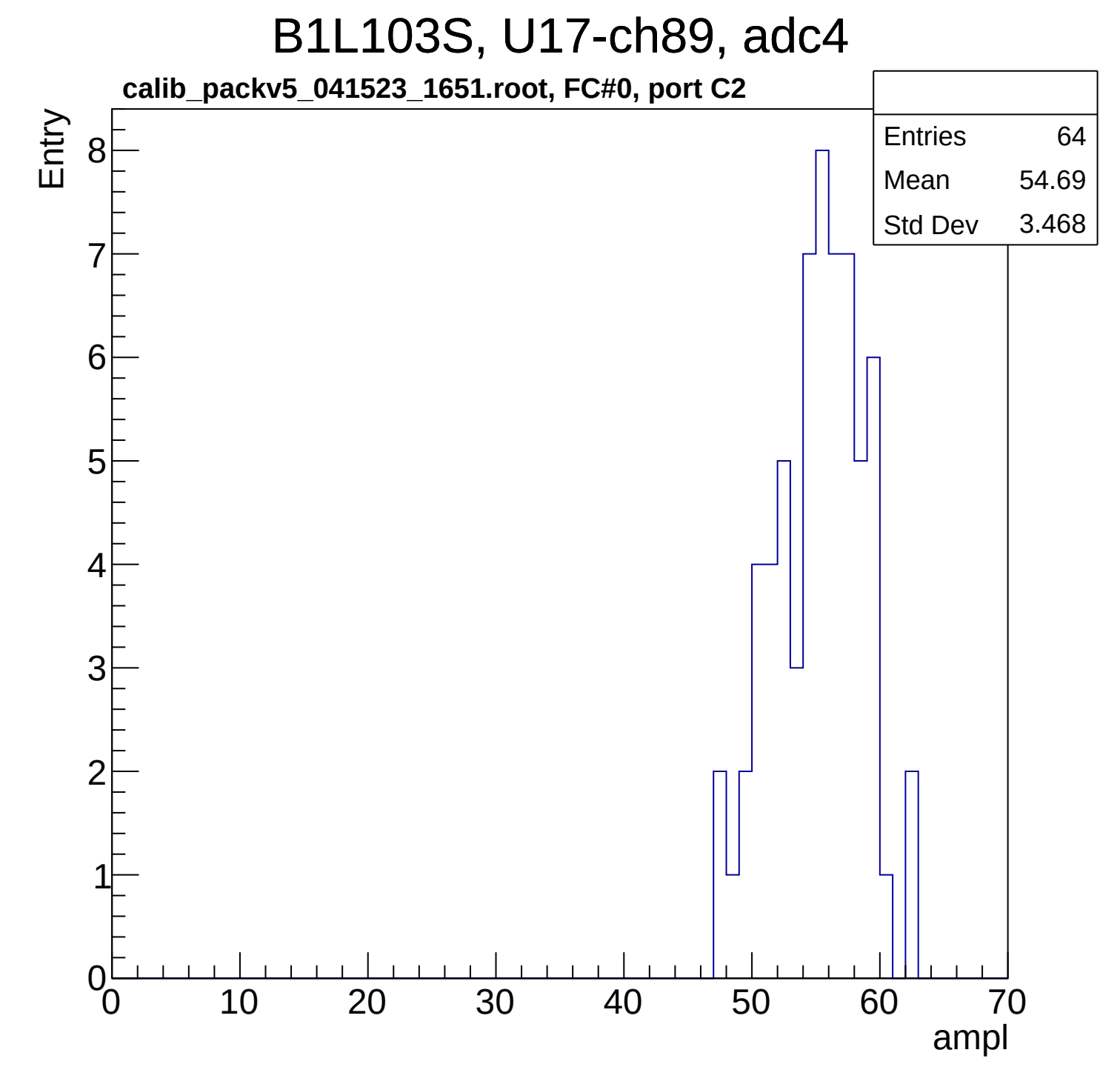

B1L103S, U17-ch88, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.78
Std Dev 23.5
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

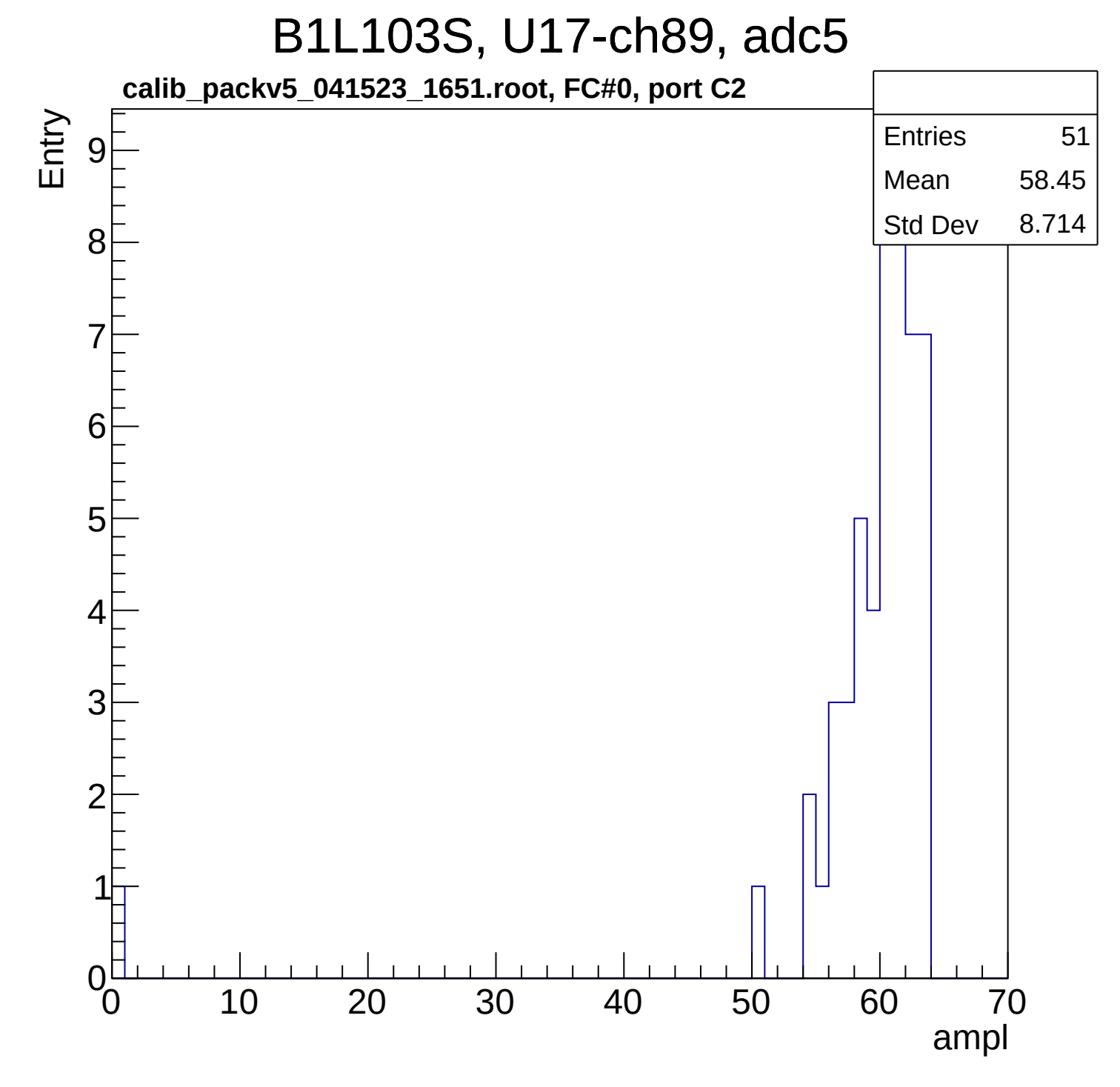

B1L103S, U17-ch89, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 25.16
Std Dev 9.598
Gaus mean : 28.6864
Gaus Width: 4.2638
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

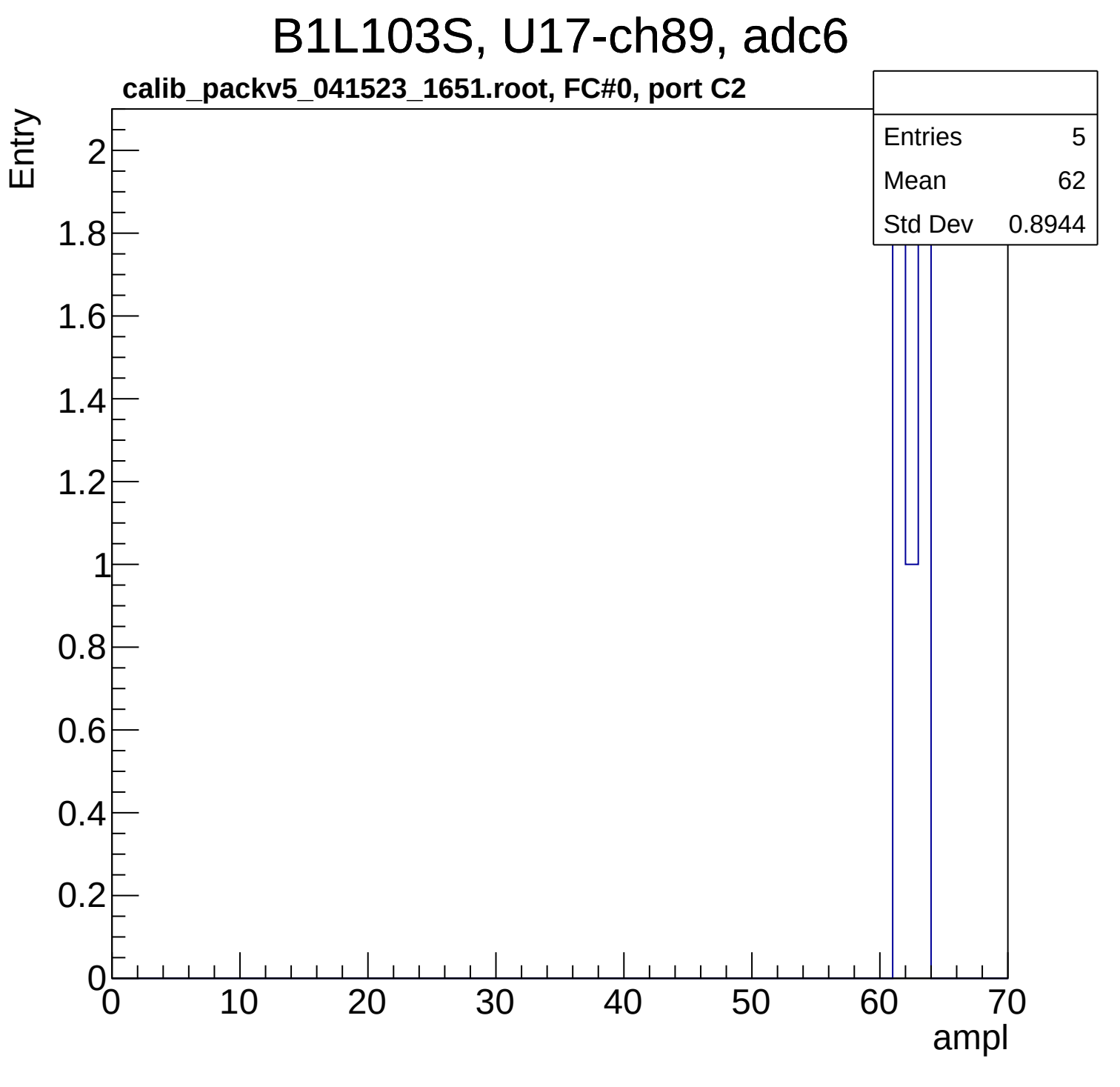

B1L103S, U17-ch89, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 33.1
Std Dev 9.435
Gaus mean : 36.8677
Gaus Width: 3.3141
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

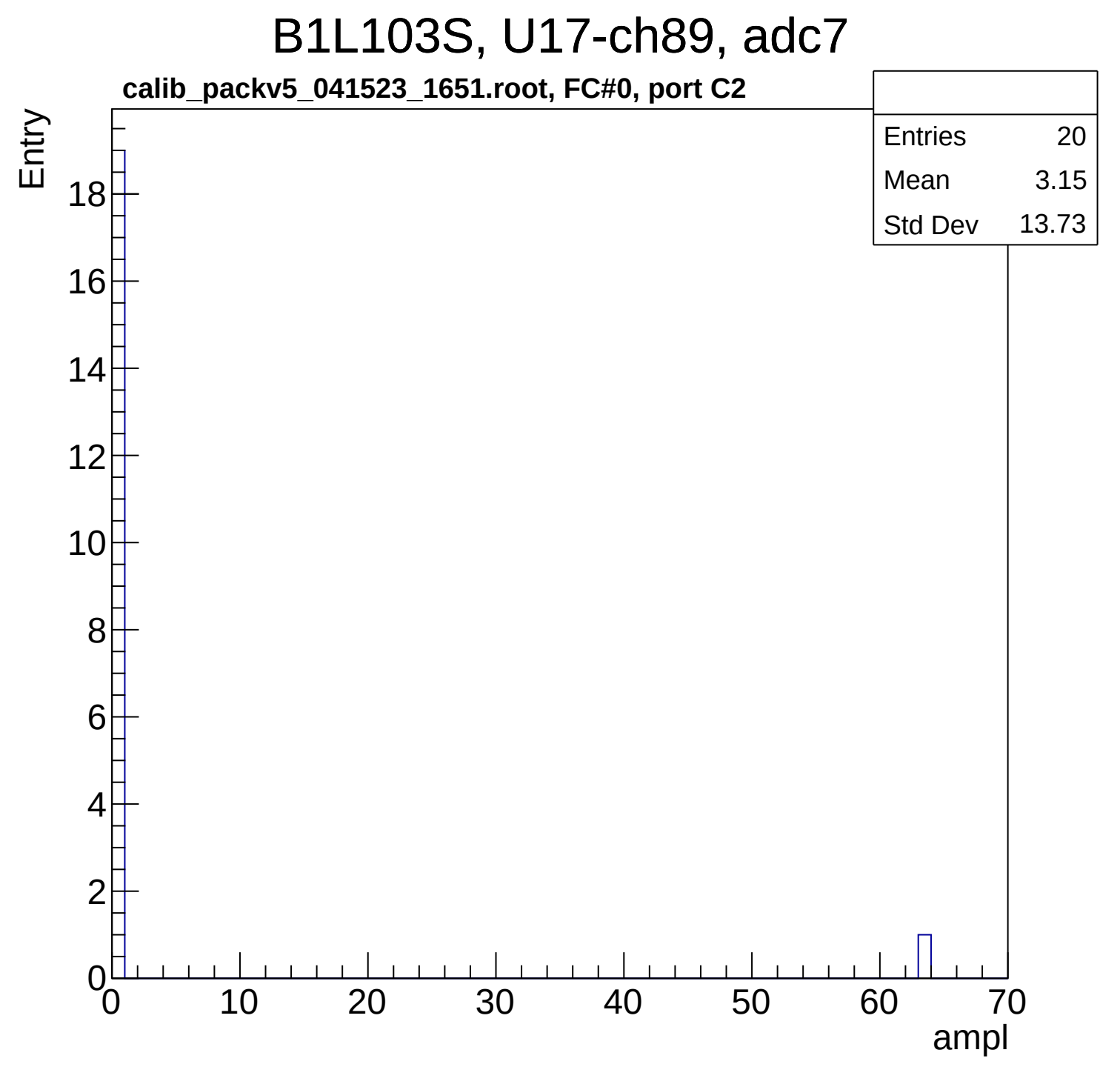

B1L103S, U17-ch89, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 36.78
Std Dev 13.89
Gaus mean : 42.3797
Gaus Width: 4.6088
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

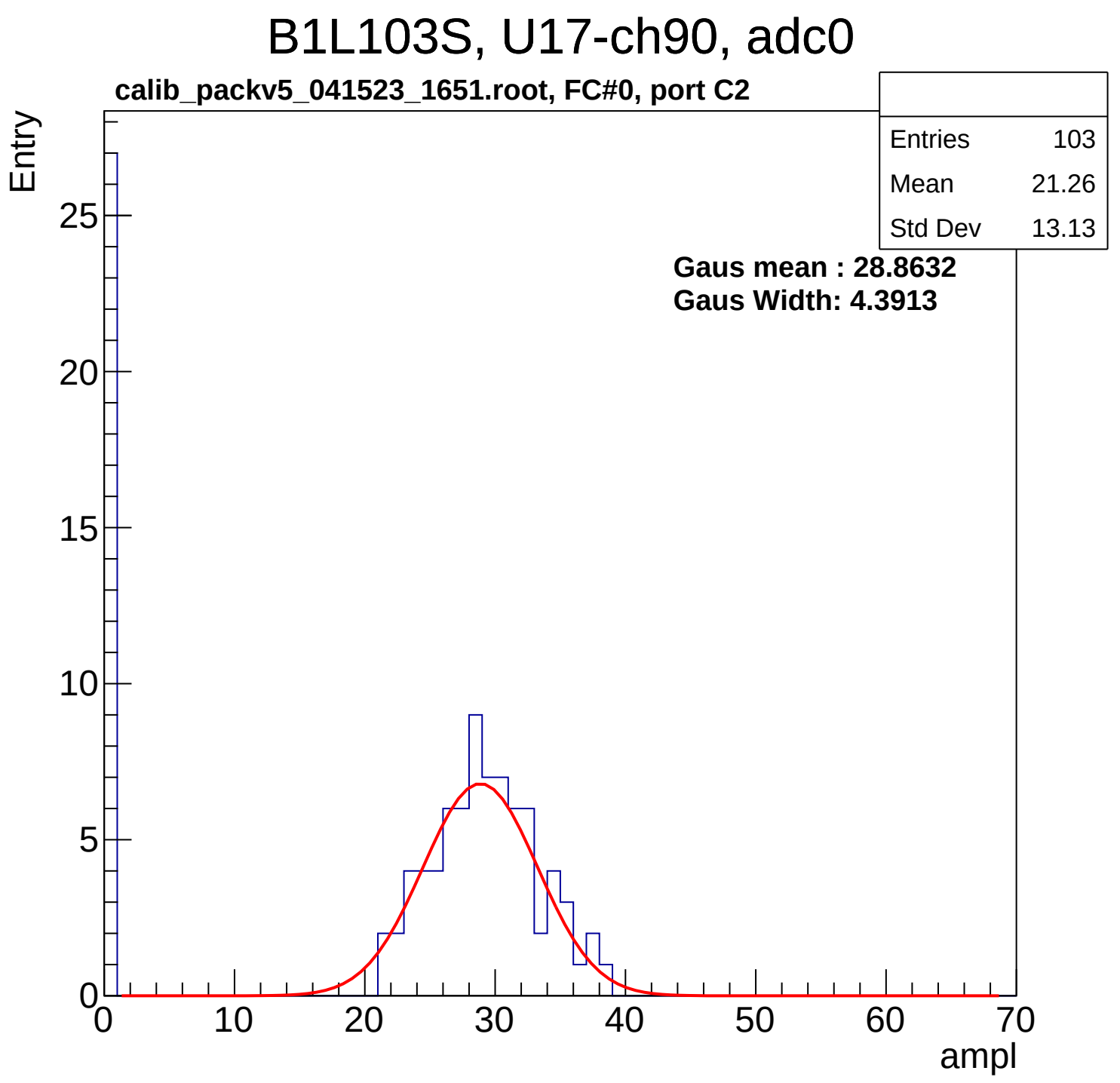

B1L103S, U17-ch89, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 47.74
Std Dev 3.815
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

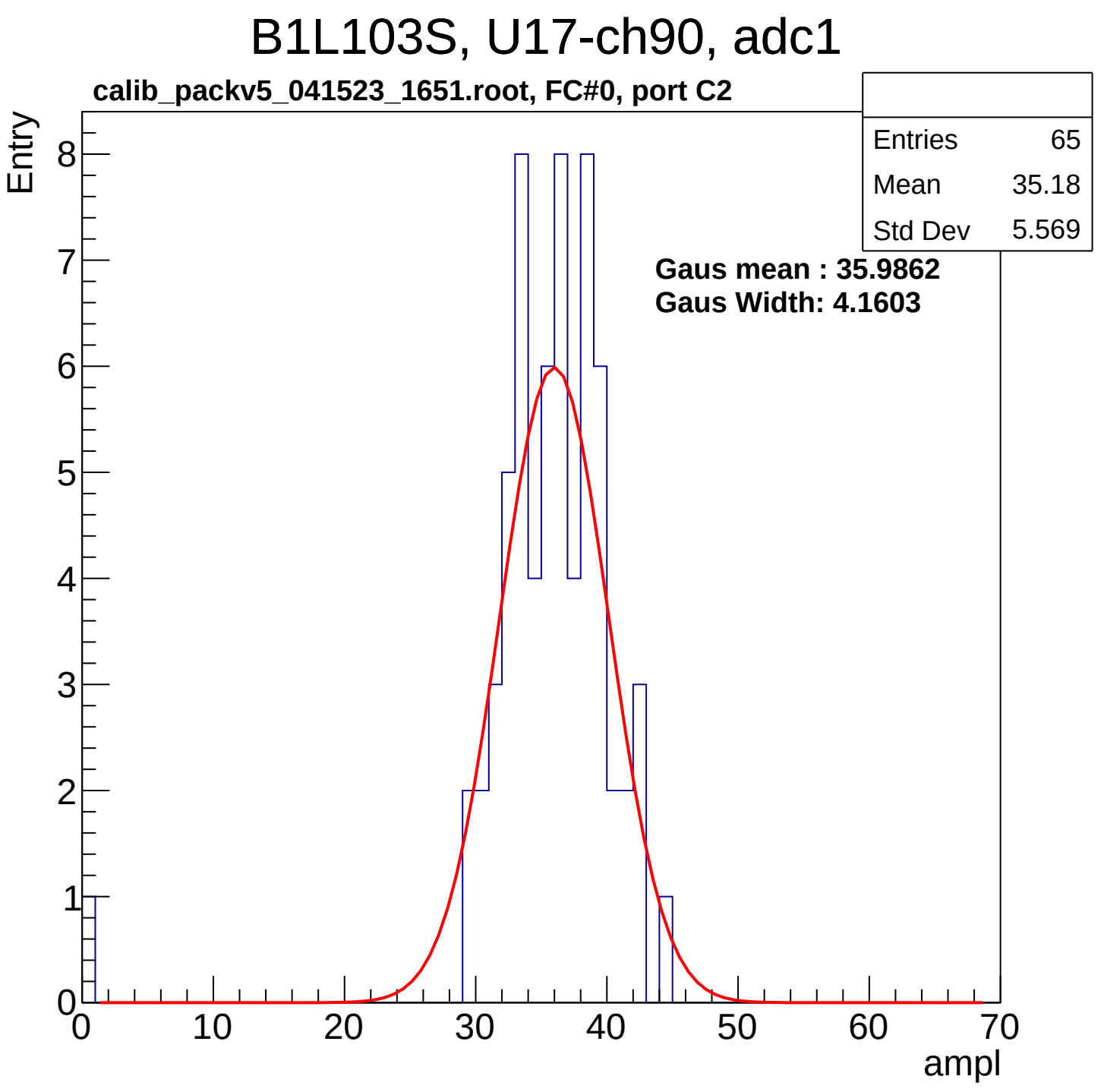

B1L103S, U17-ch89, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 54.69
Std Dev 3.468
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

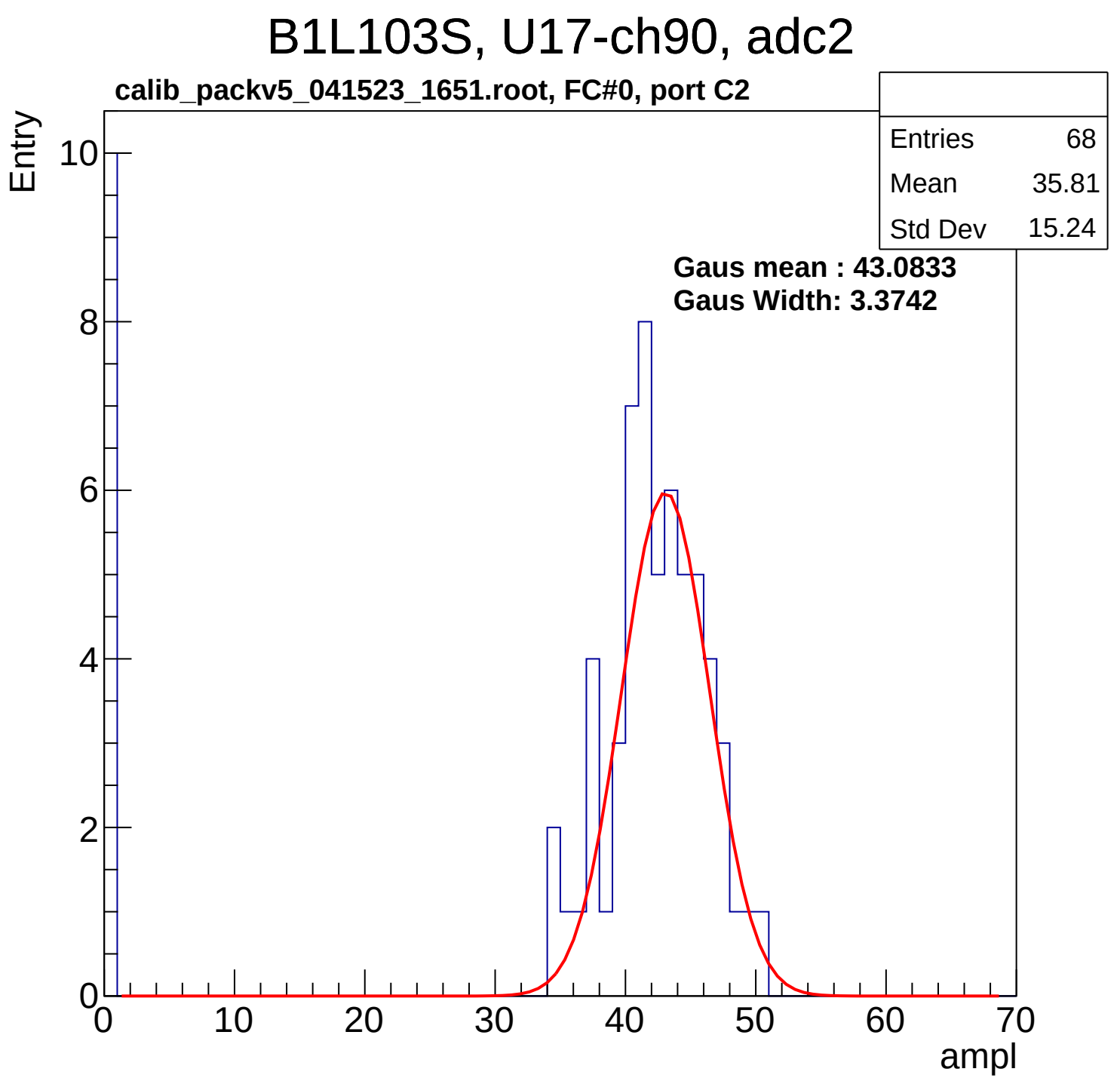

B1L103S, U17-ch89, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.45
Std Dev 8.714
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

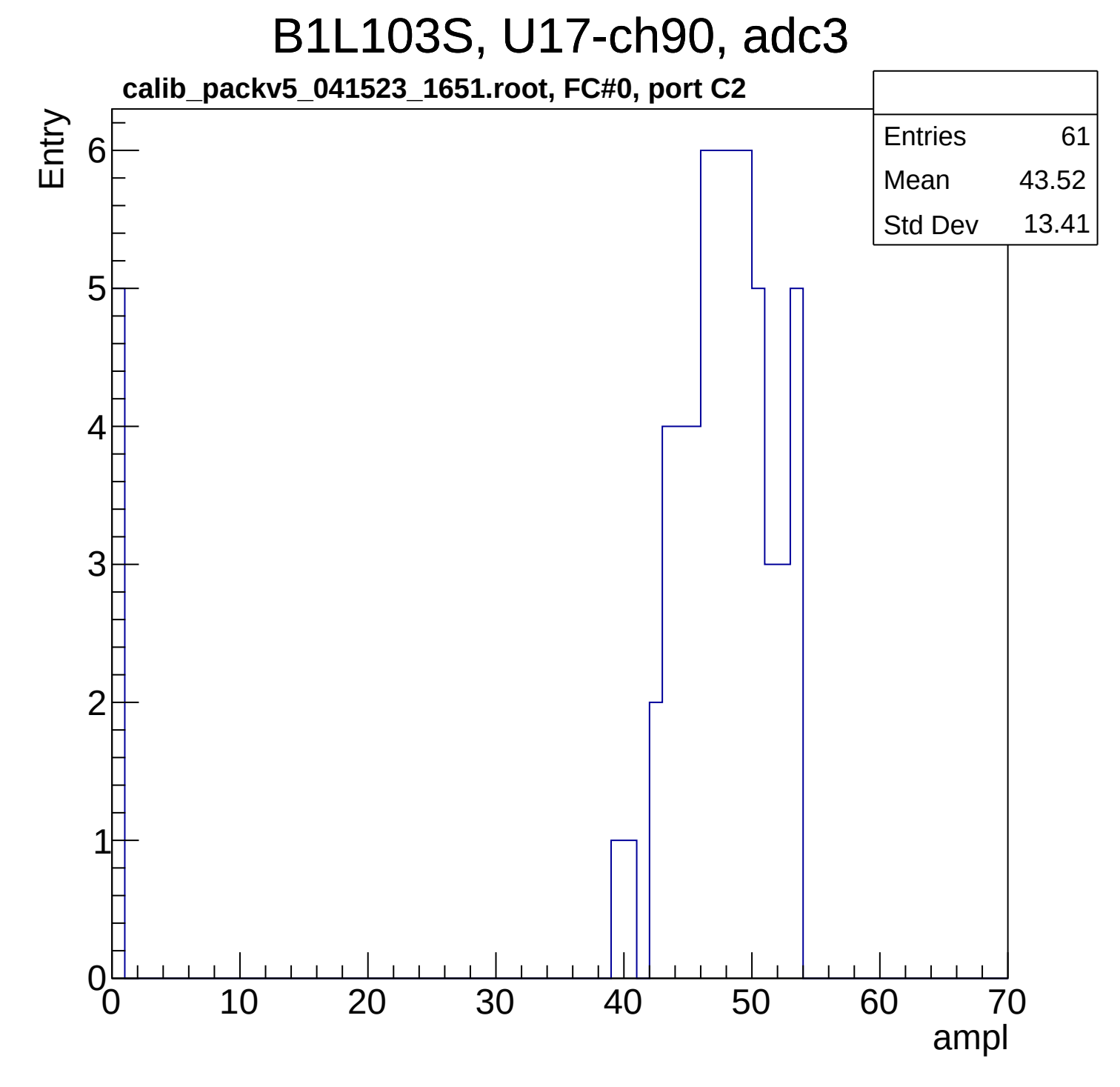

B1L103S, U17-ch89, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62
Std Dev 0.8944
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

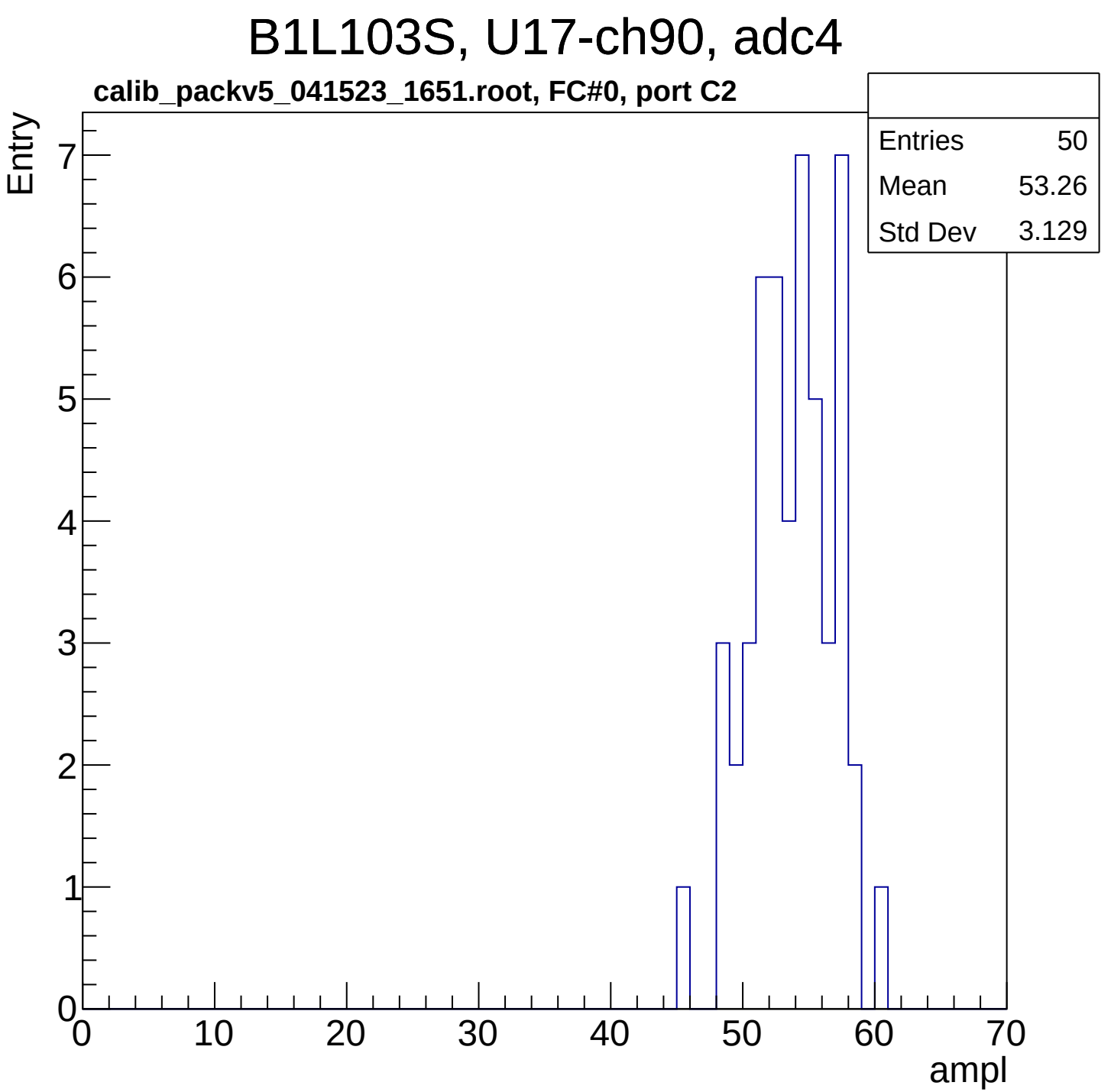

B1L103S, U17-ch89, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

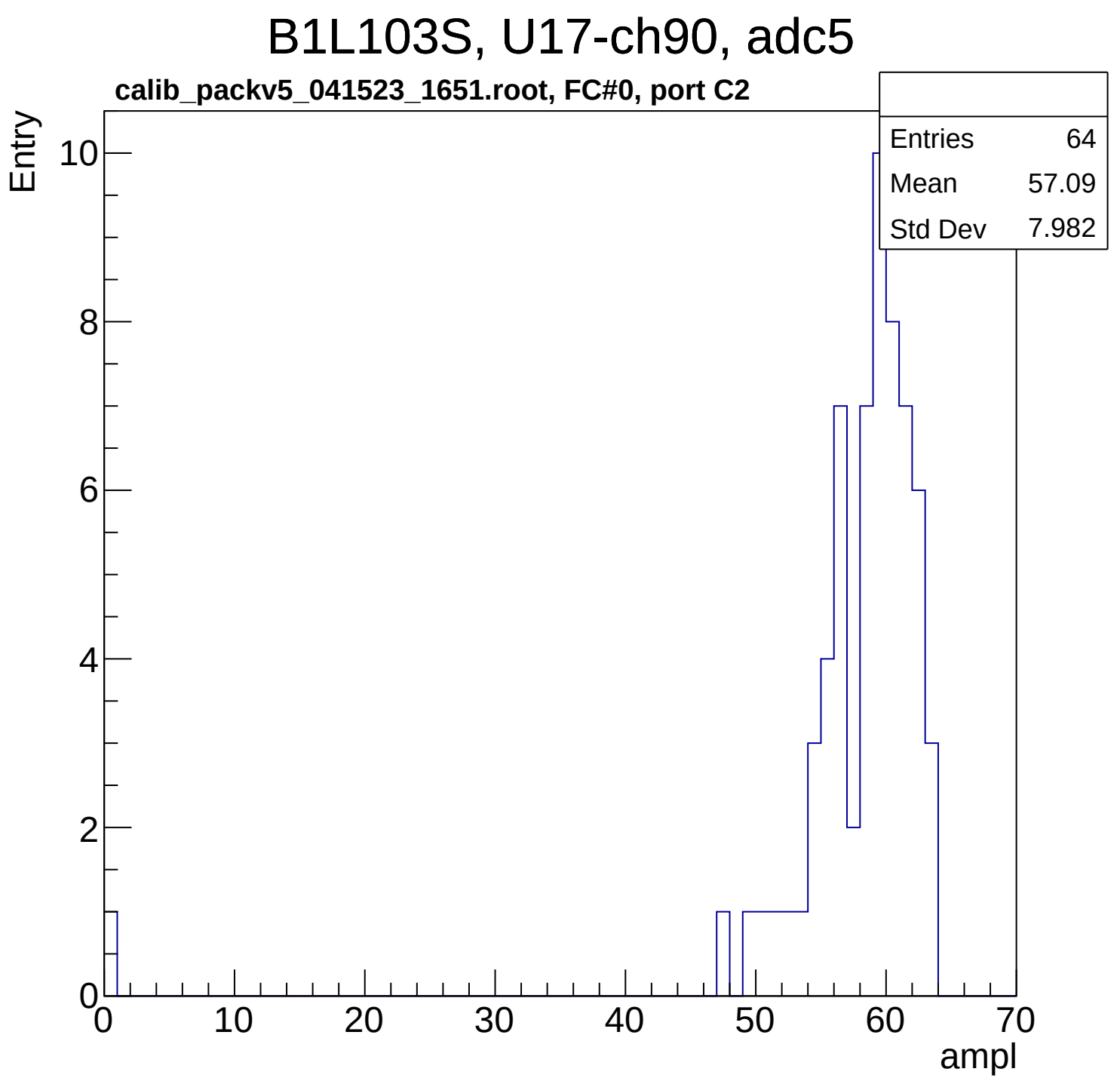

B1L103S, U17-ch90, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 21.26
Std Dev 13.13
Gaus mean : 28.8632
Gaus Width: 4.3913
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70

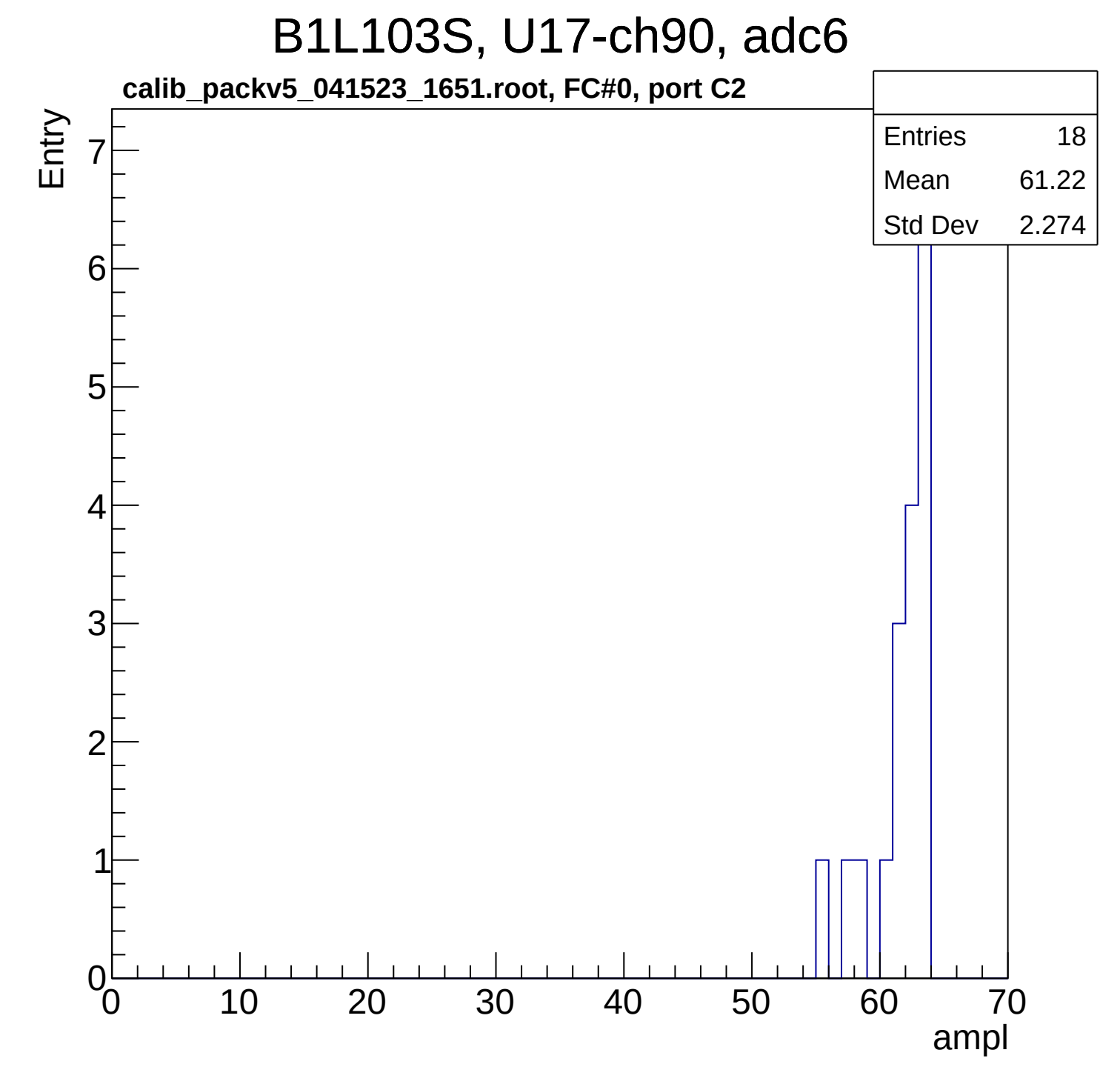

B1L103S, U17-ch90, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 35.18
Std Dev 5.569
Gaus mean : 35.9862
Gaus Width: 4.1603
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

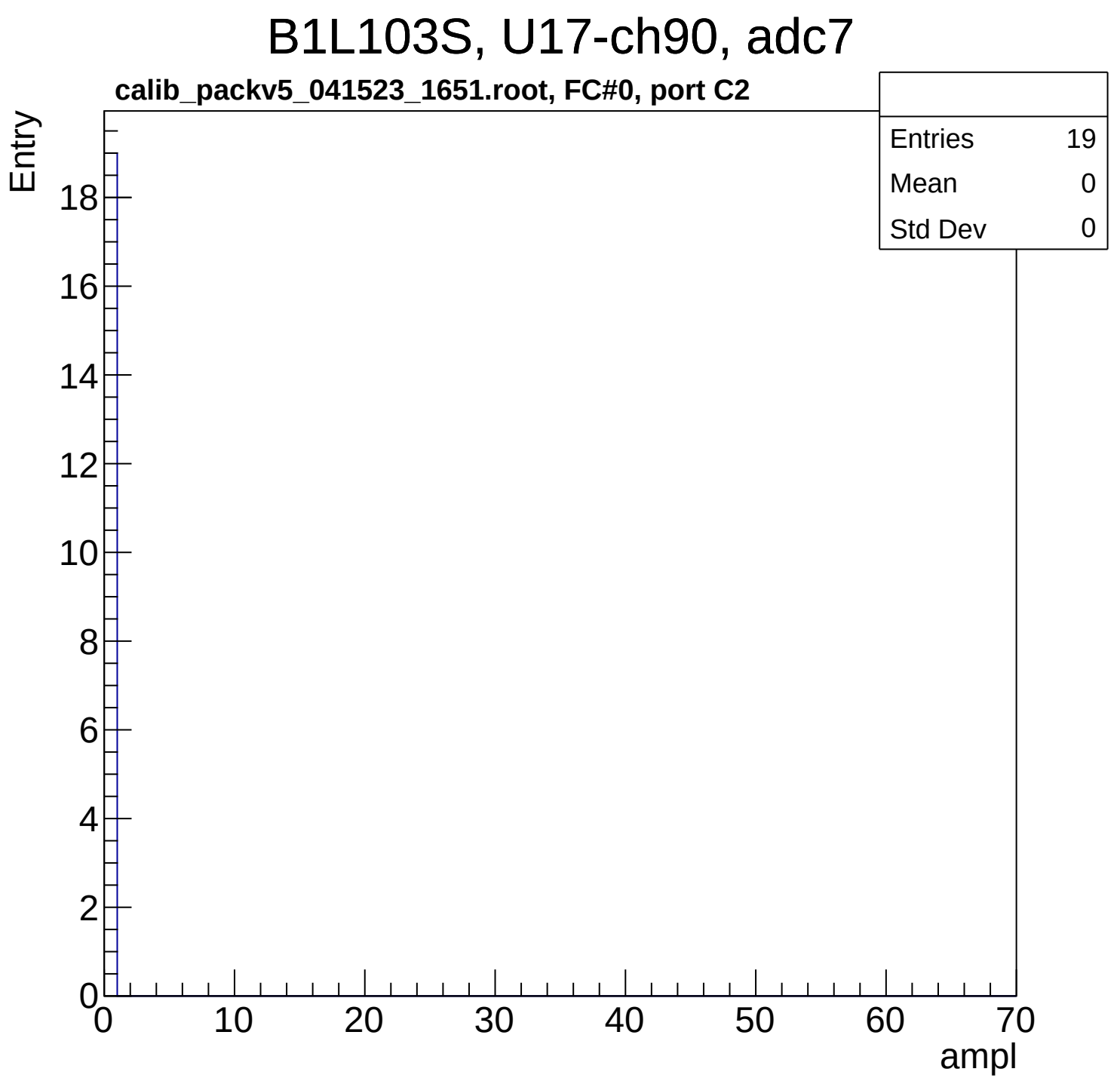

B1L103S, U17-ch90, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 35.81
Std Dev 15.24
Gaus mean : 43.0833
Gaus Width: 3.3742
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

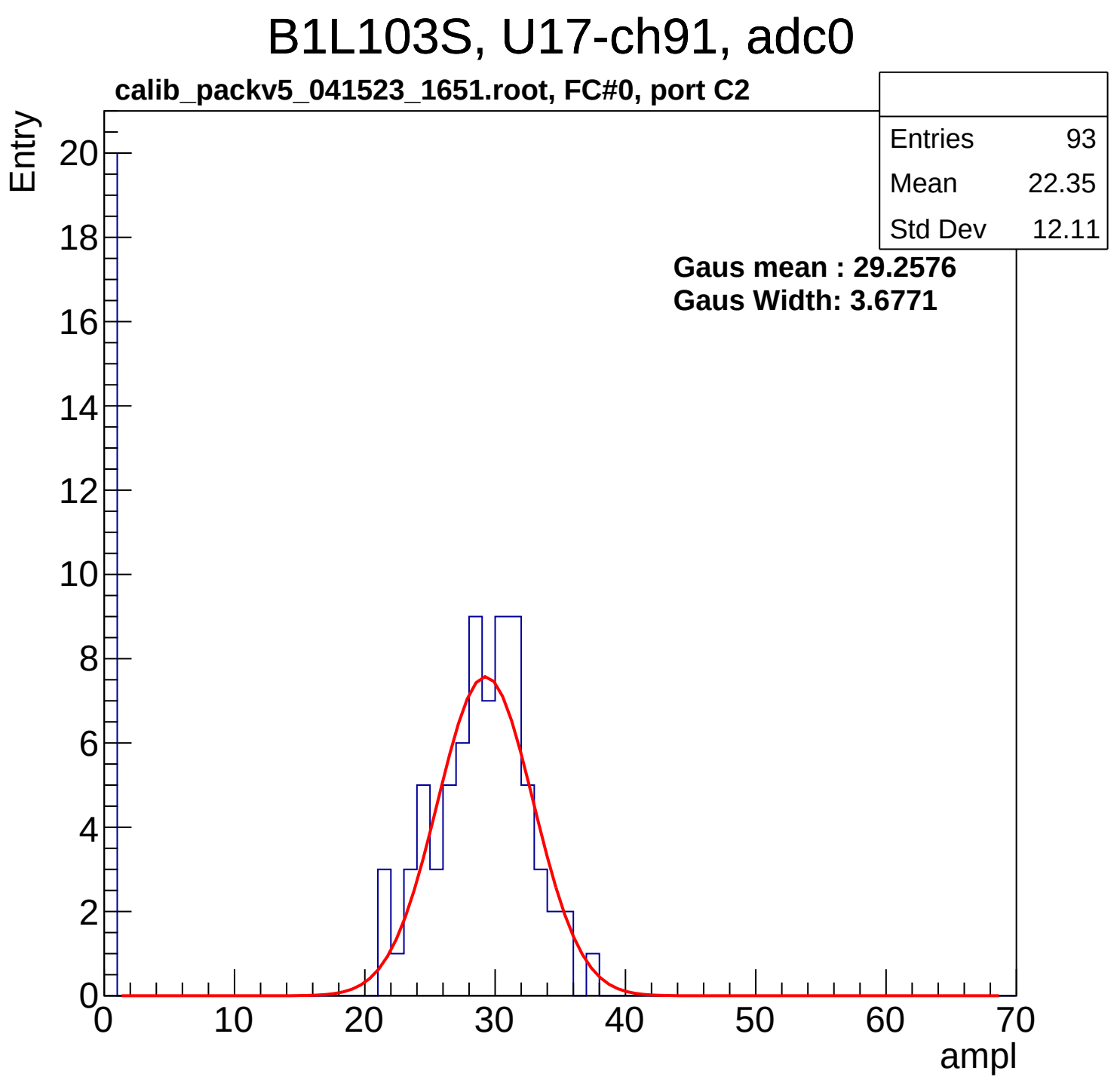

B1L103S, U17-ch90, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 43.52
Std Dev 13.41
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

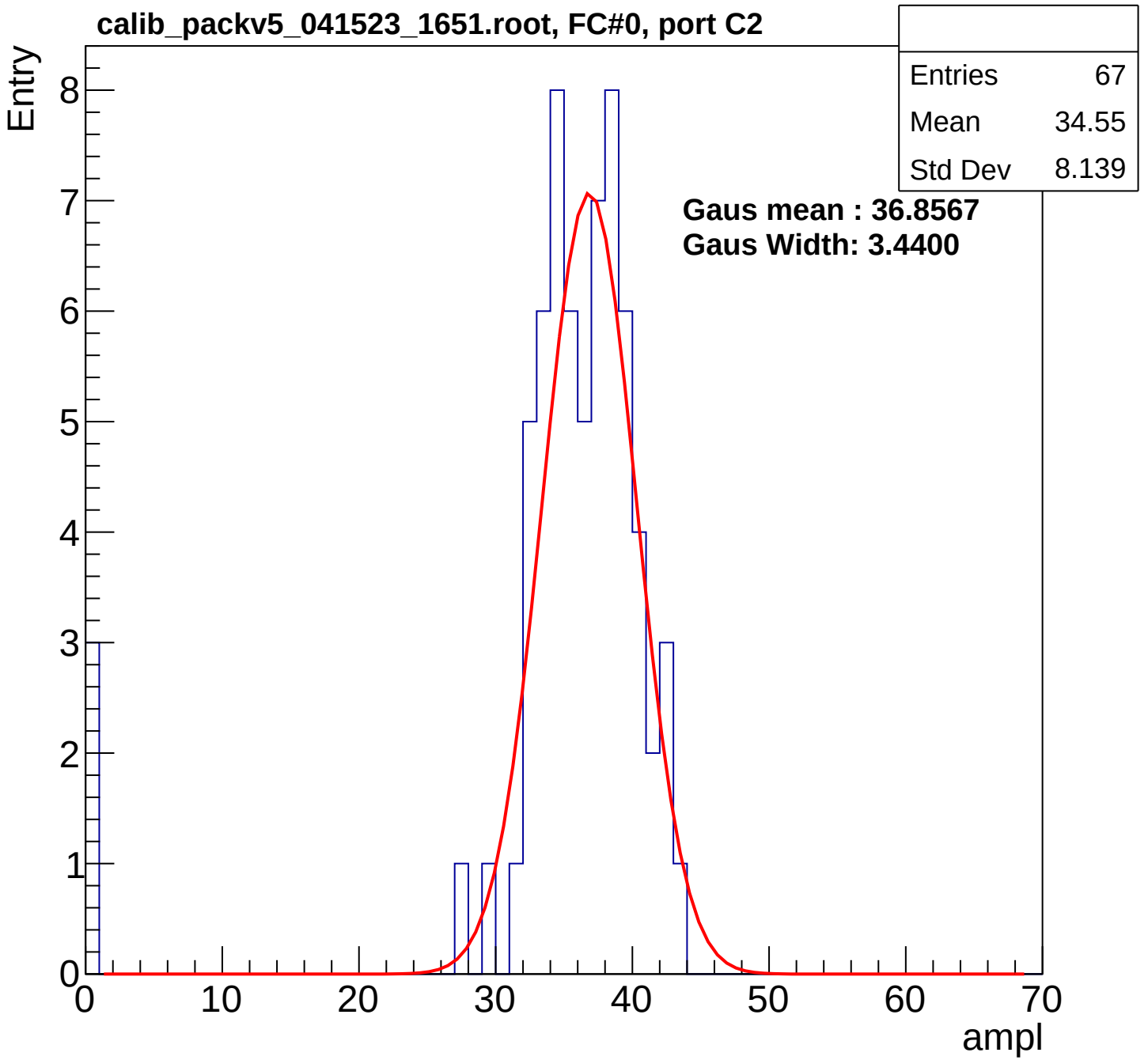

B1L103S, U17-ch90, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 53.26
Std Dev 3.129
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

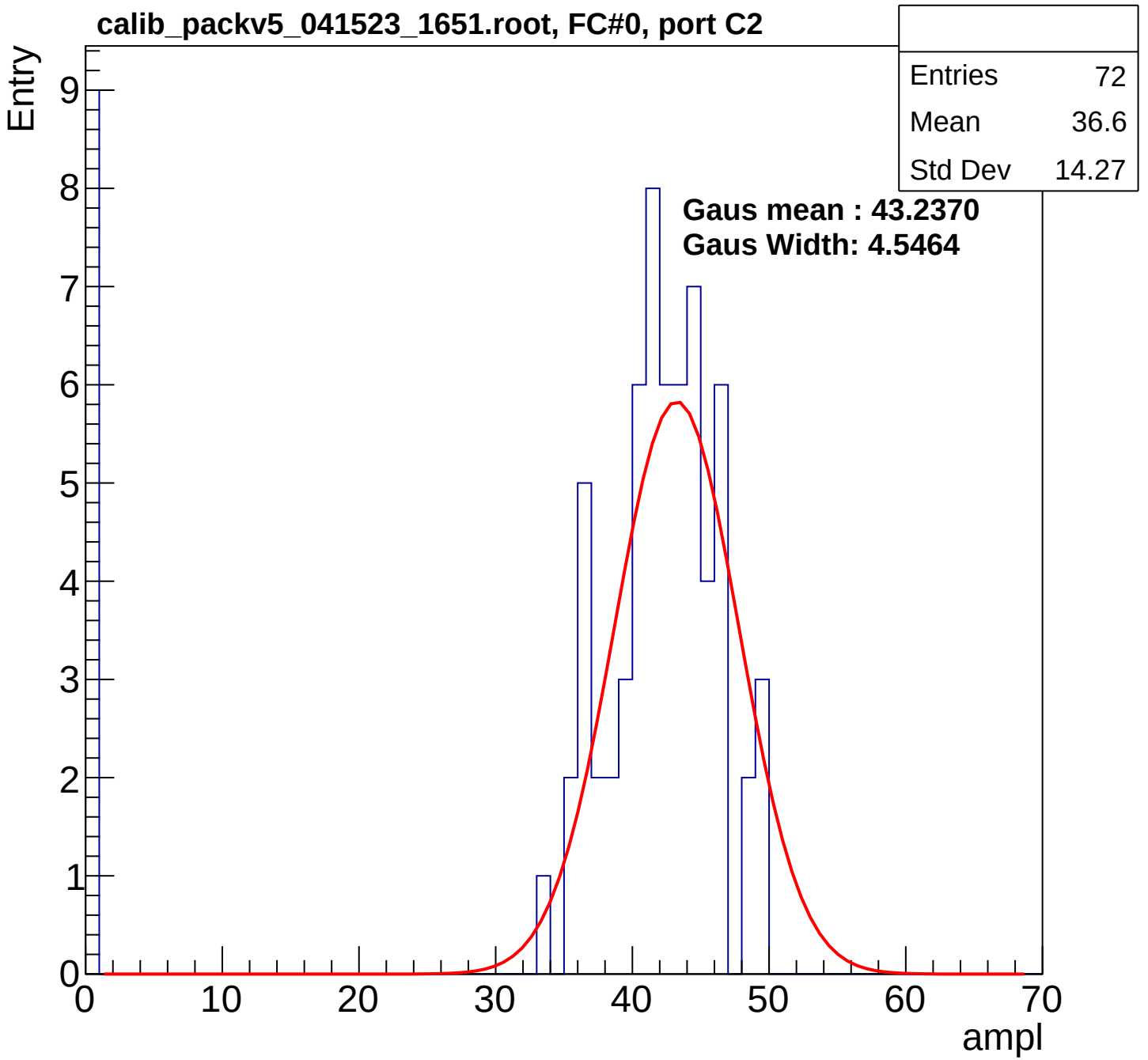

B1L103S, U17-ch90, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 57.09
Std Dev 7.982
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

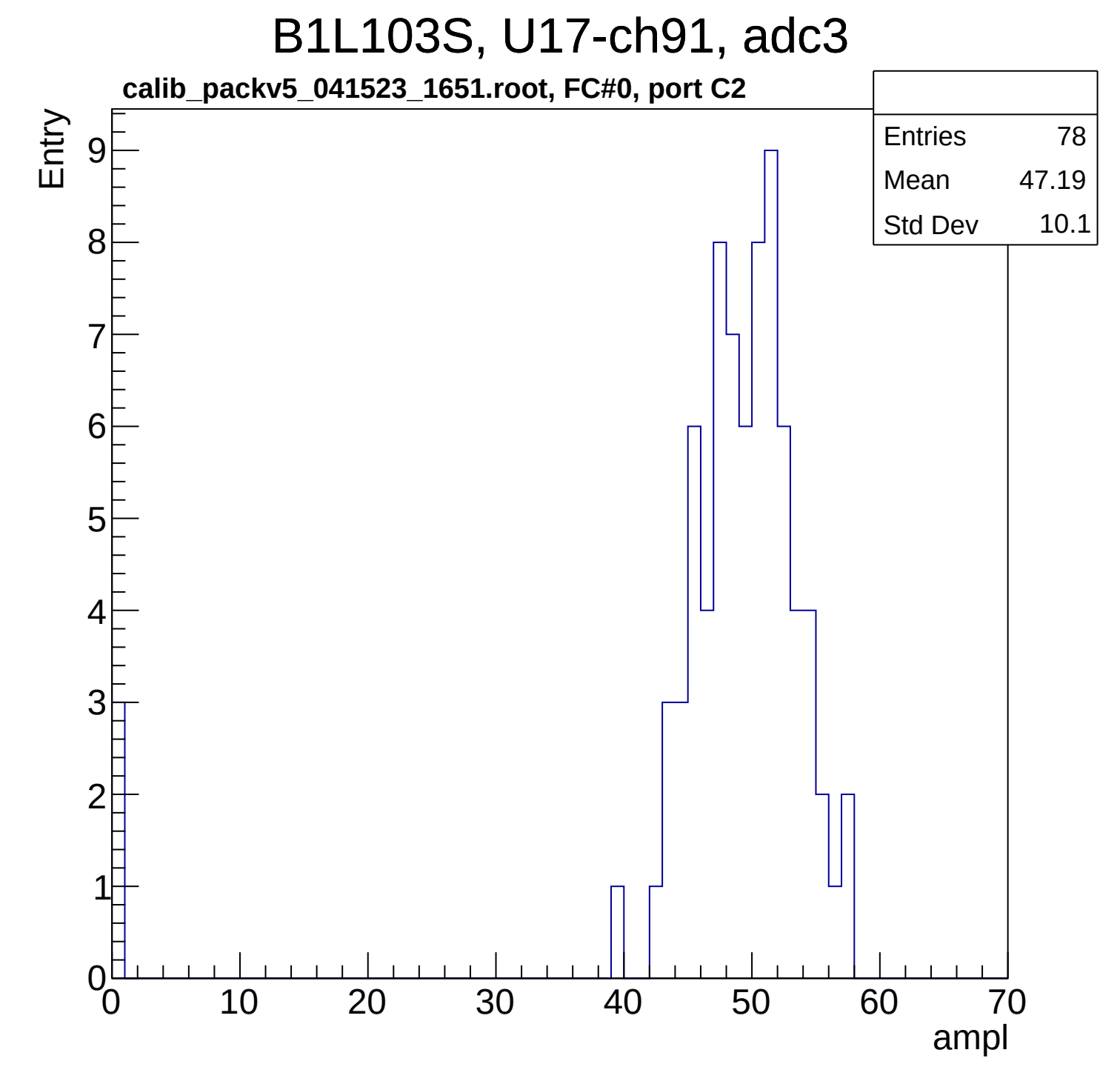

B1L103S, U17-ch90, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 61.22
Std Dev 2.274
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

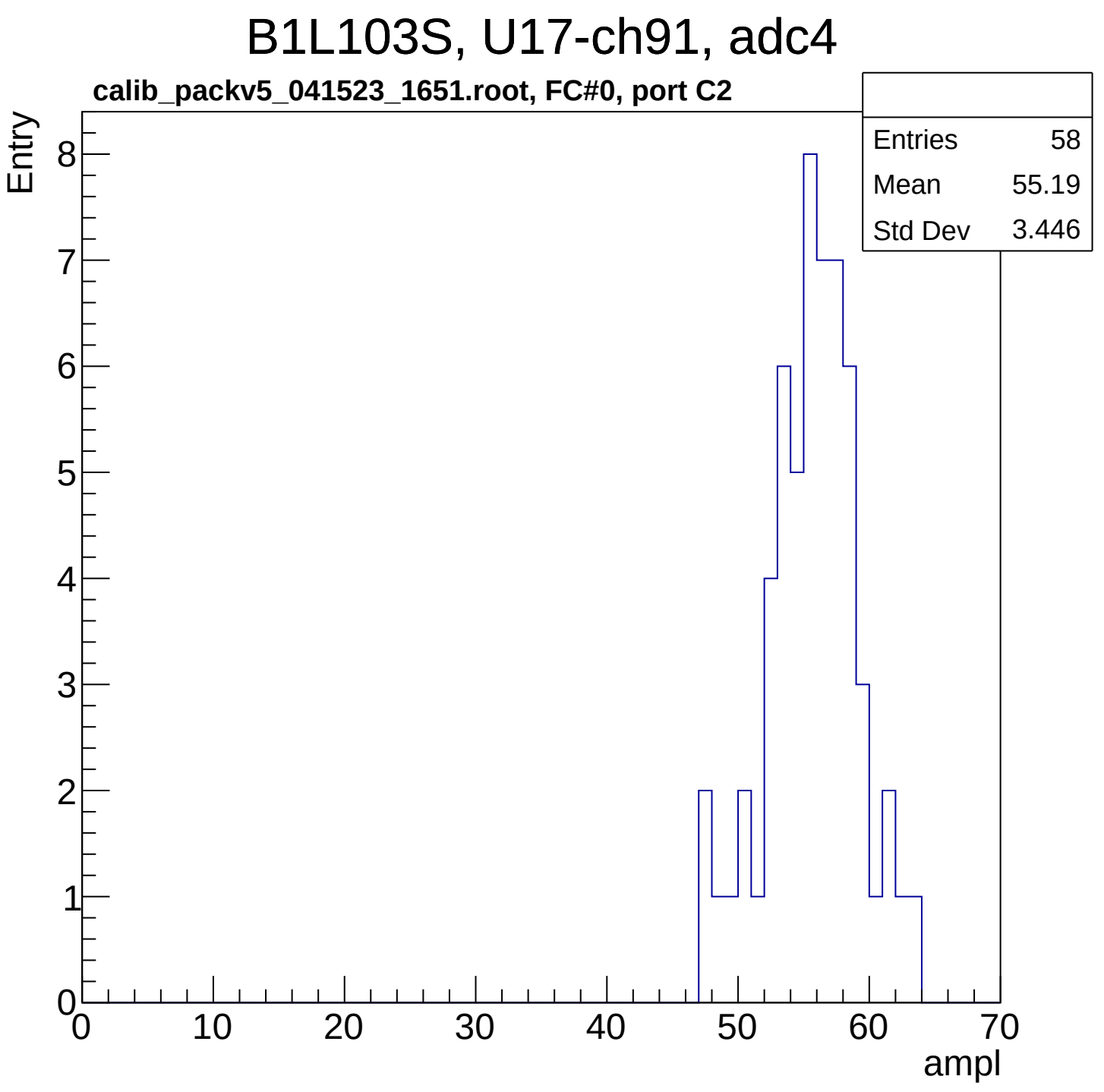

B1L103S, U17-ch90, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

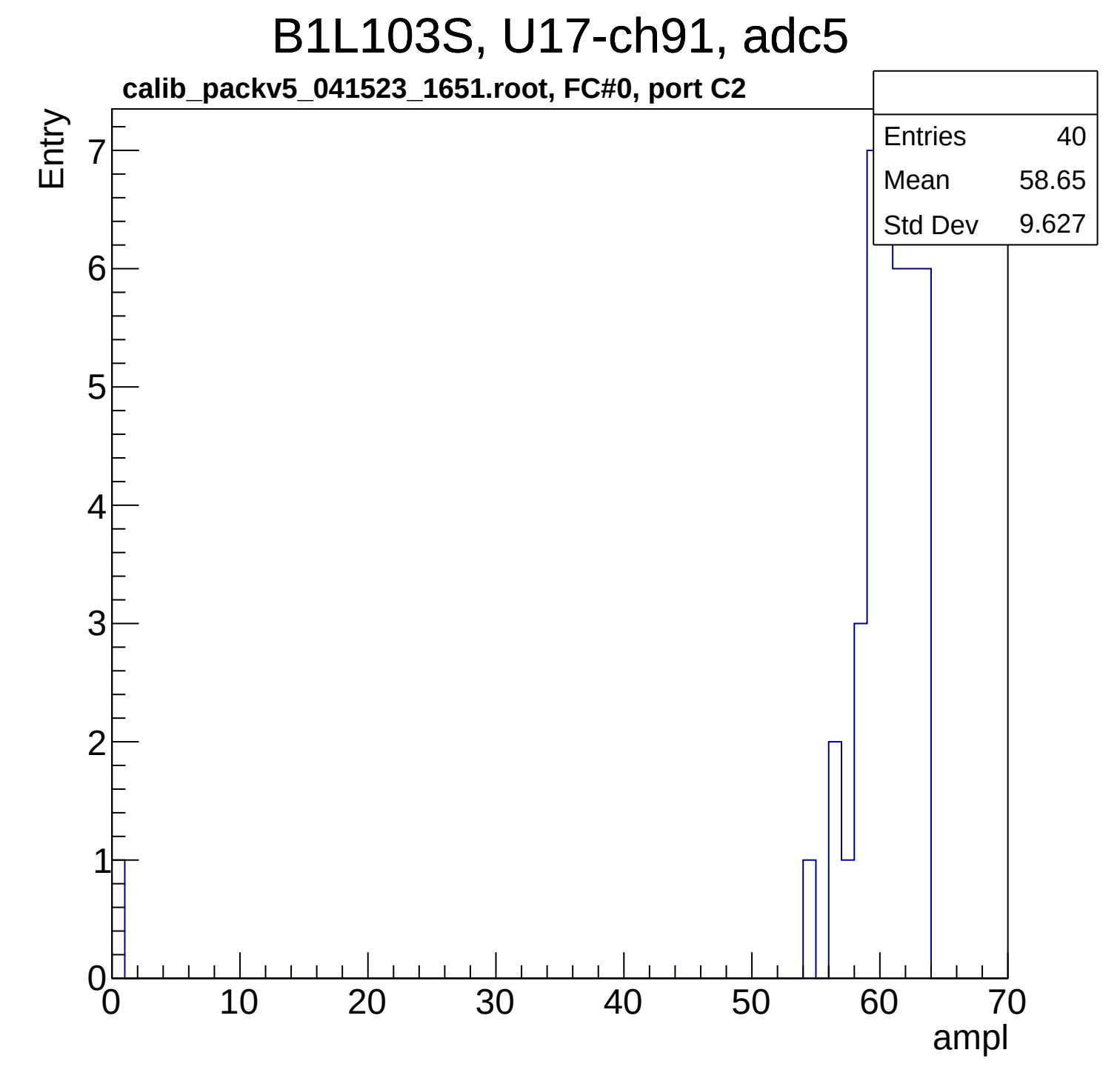

B1L103S, U17-ch91, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 22.35
Std Dev 12.11
Gaus mean : 29.2576
Gaus Width: 3.6771
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

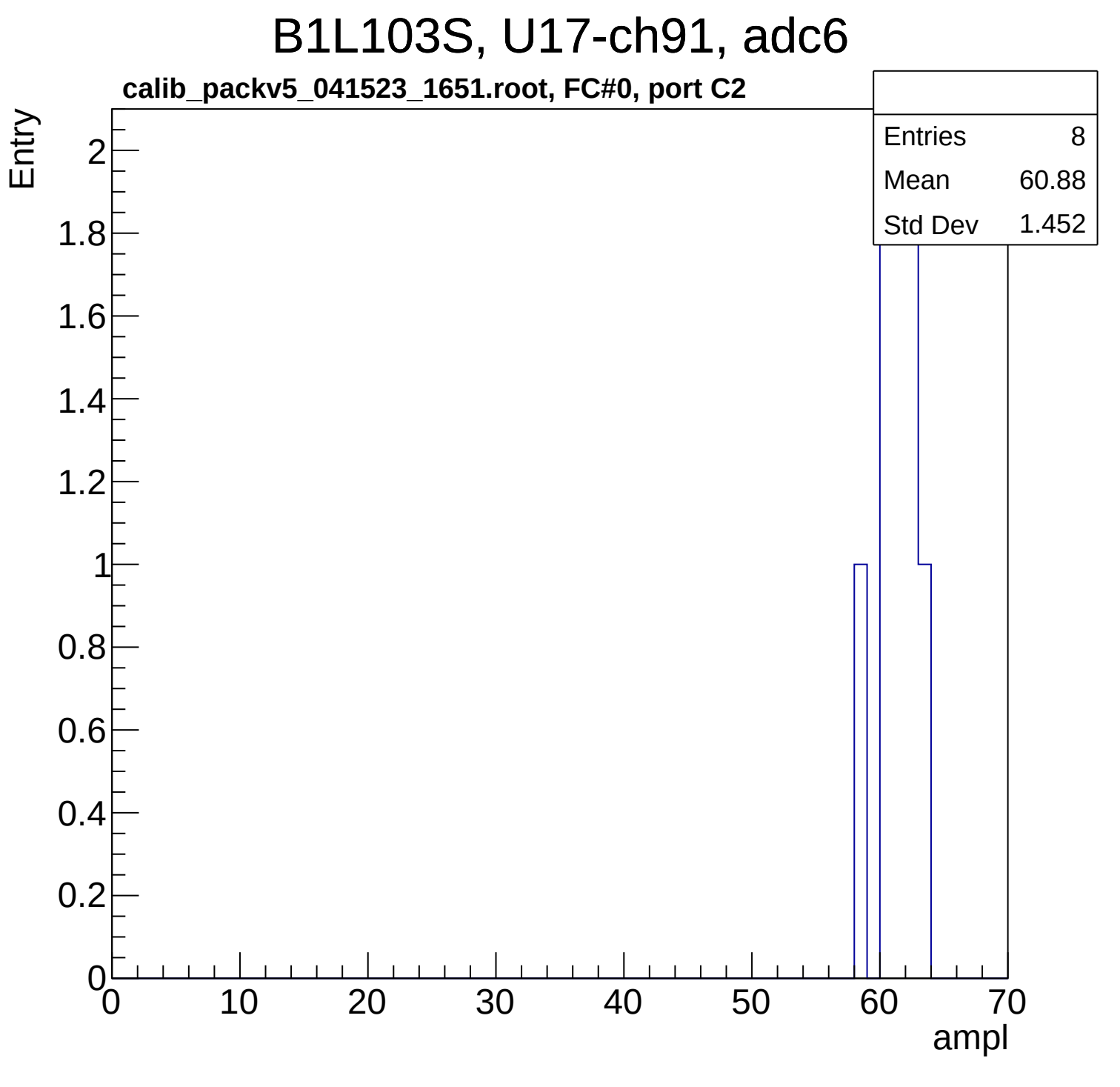

B1L103S, U17-ch91, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 34.55
Std Dev 8.139
Gaus mean : 36.8567
Gaus Width: 3.4400
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

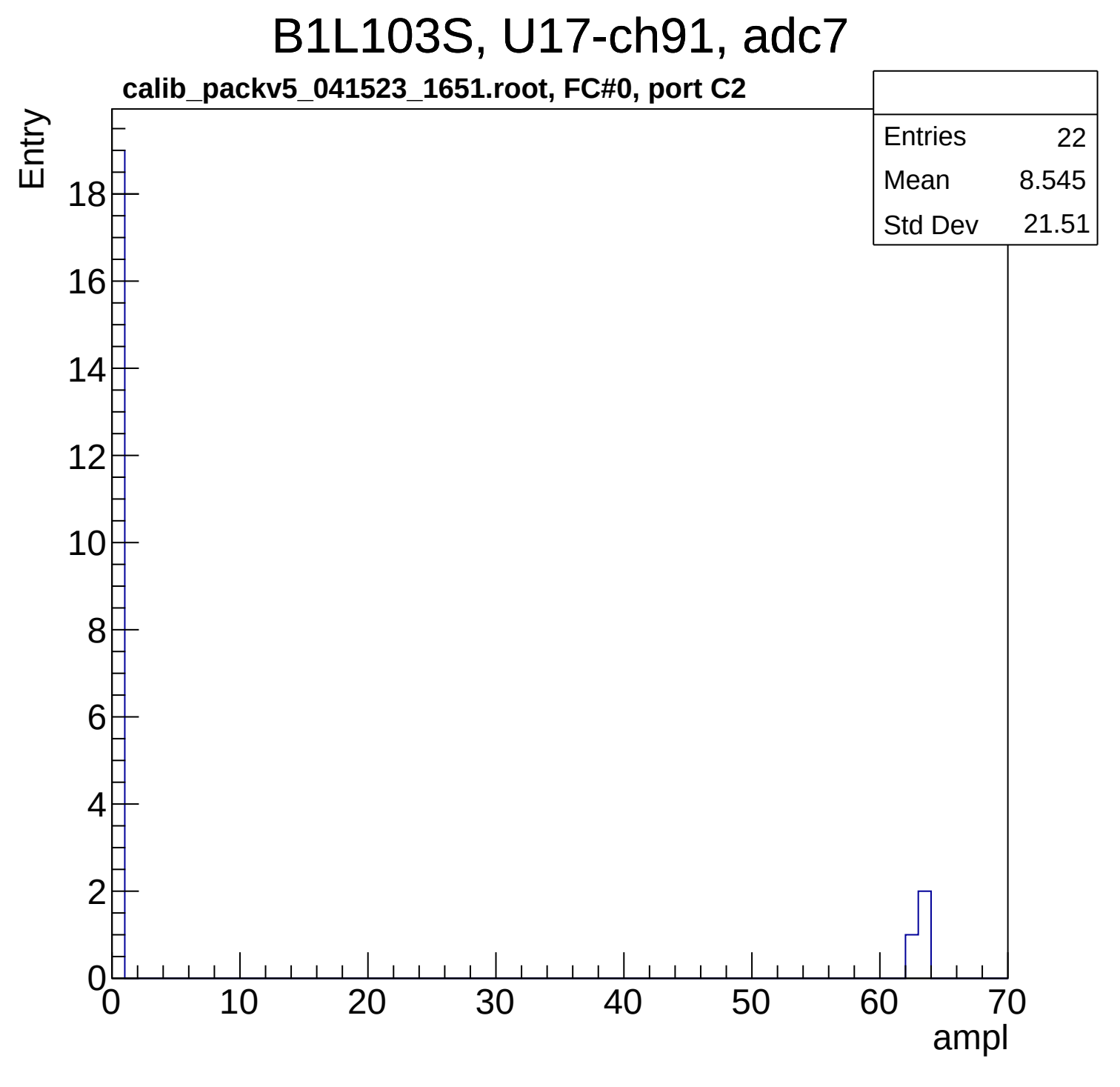

B1L103S, U17-ch91, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 36.6
Std Dev 14.27
Gaus mean : 43.2370
Gaus Width: 4.5464
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

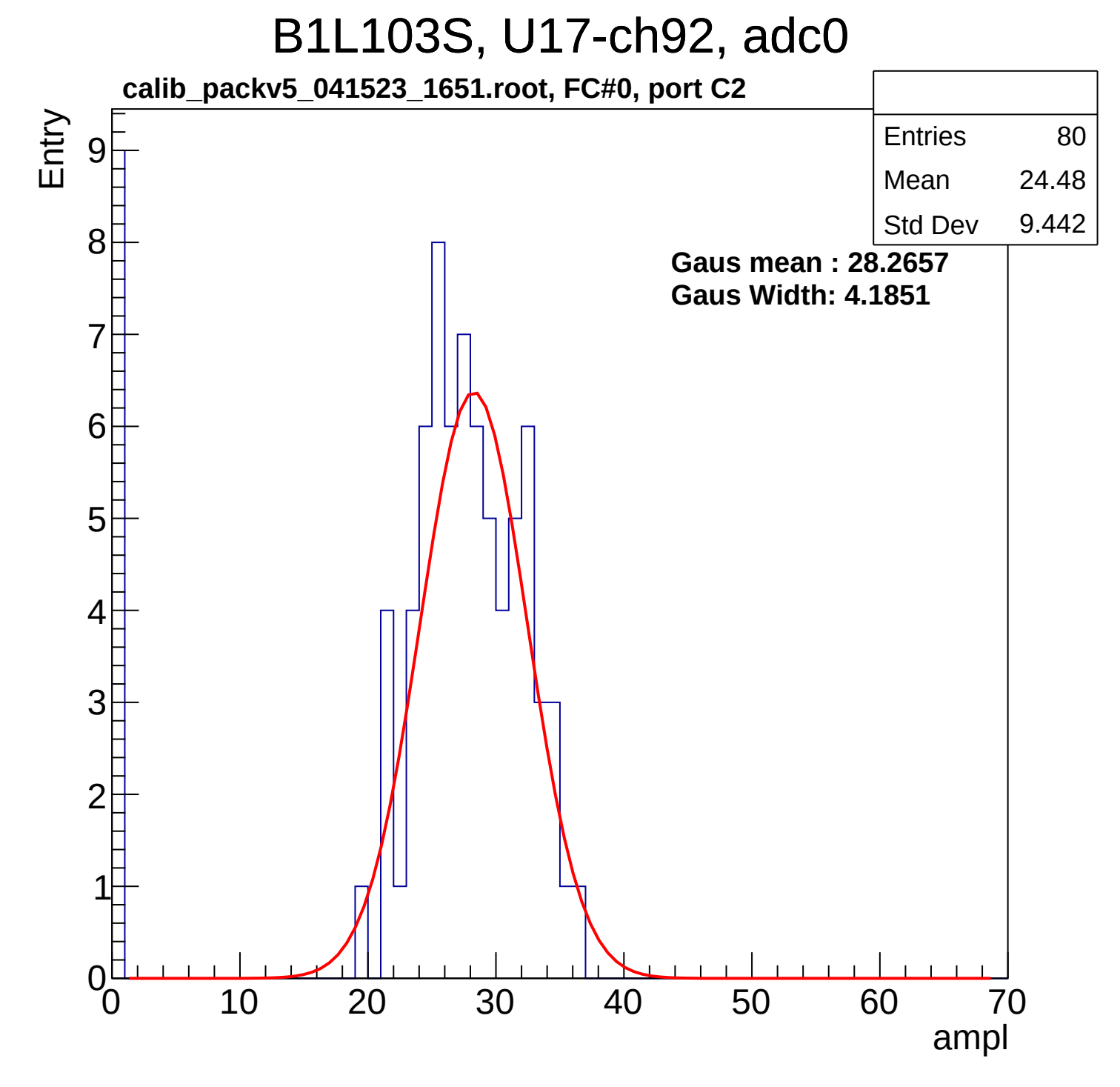

B1L103S, U17-ch91, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 47.19
Std Dev 10.1
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

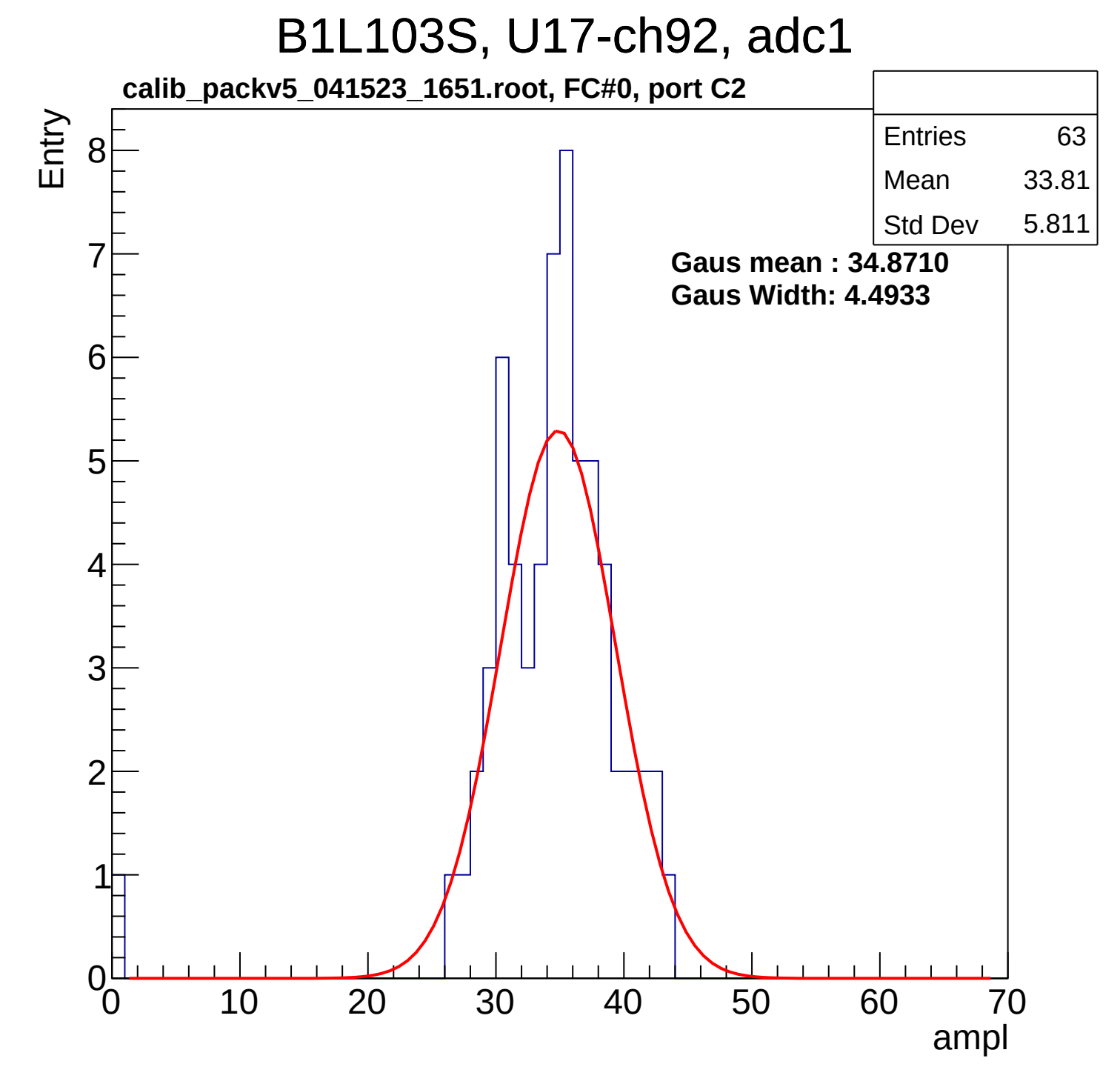

B1L103S, U17-ch91, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 55.19
Std Dev 3.446
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

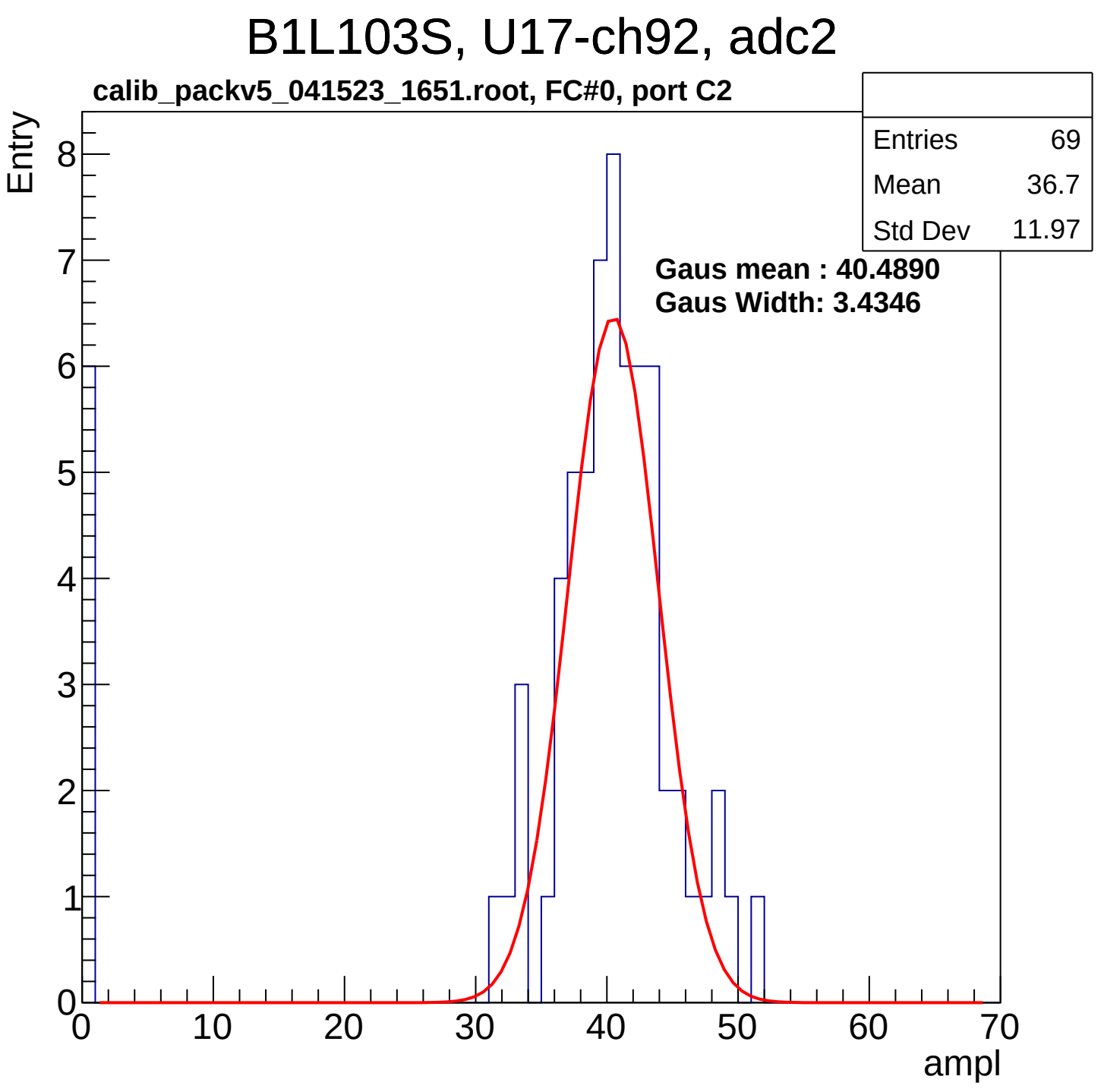

B1L103S, U17-ch91, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 58.65
Std Dev 9.627
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

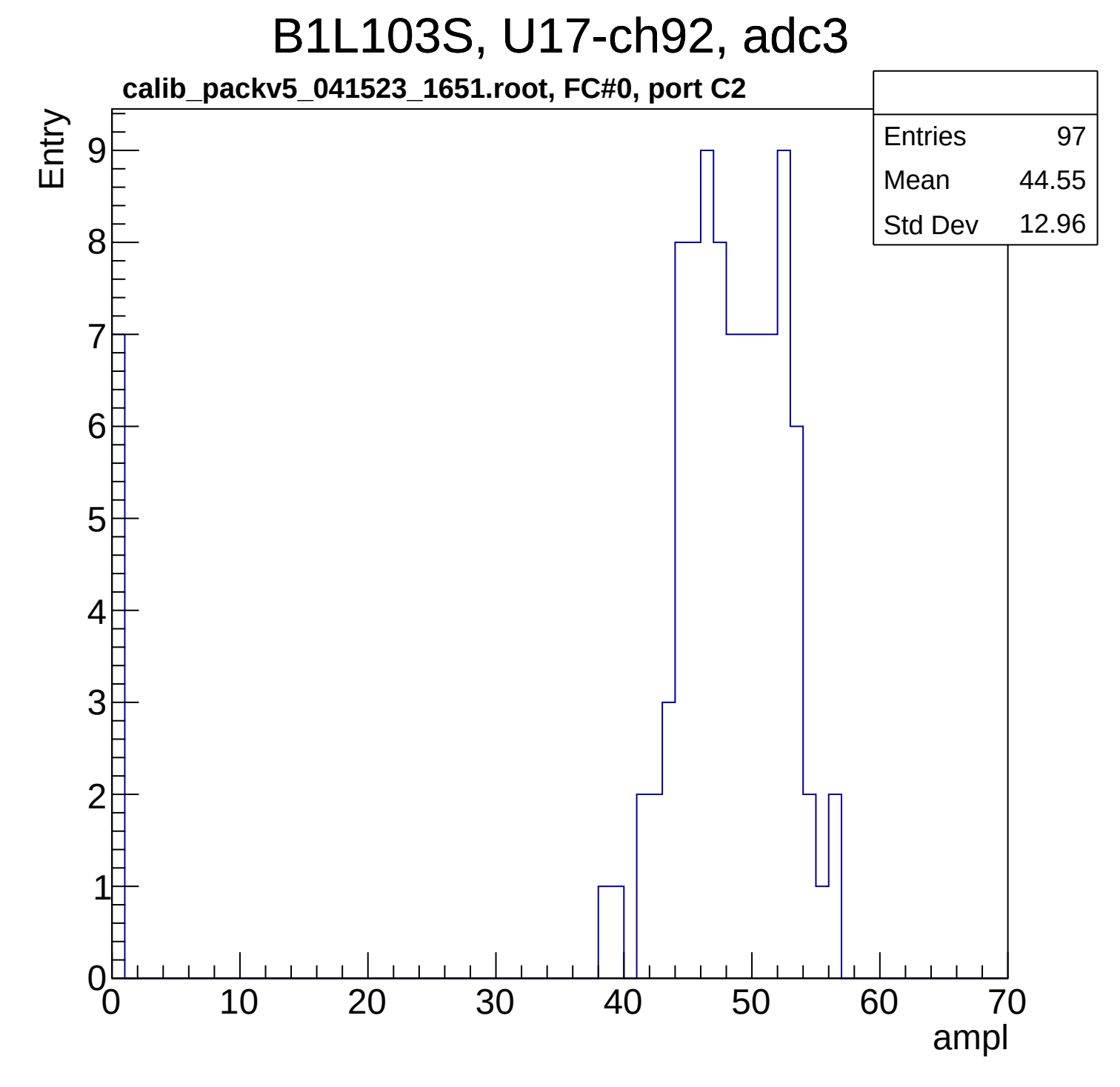

B1L103S, U17-ch91, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 60.88
Std Dev 1.452
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

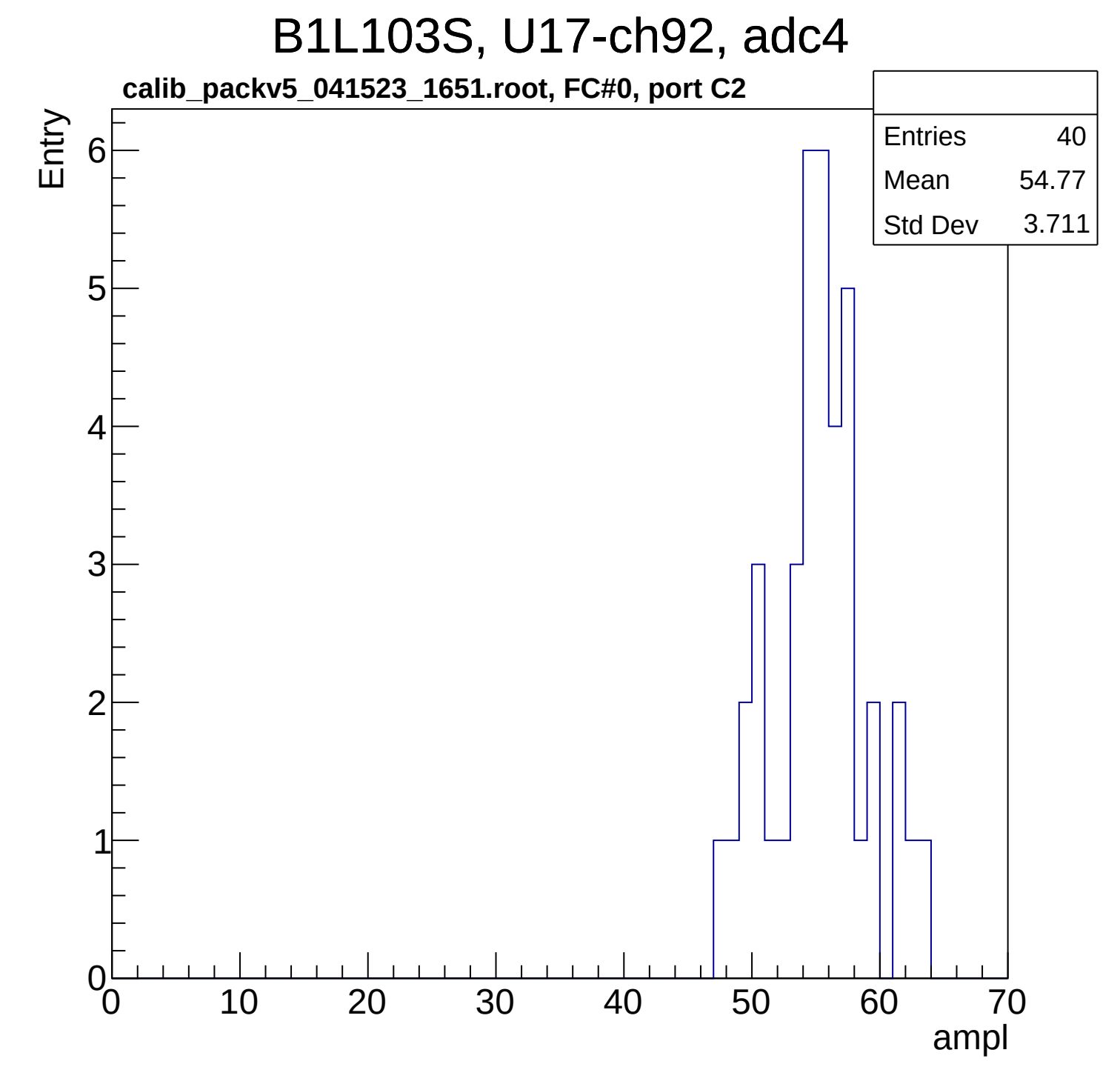

B1L103S, U17-ch91, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.545
Std Dev 21.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

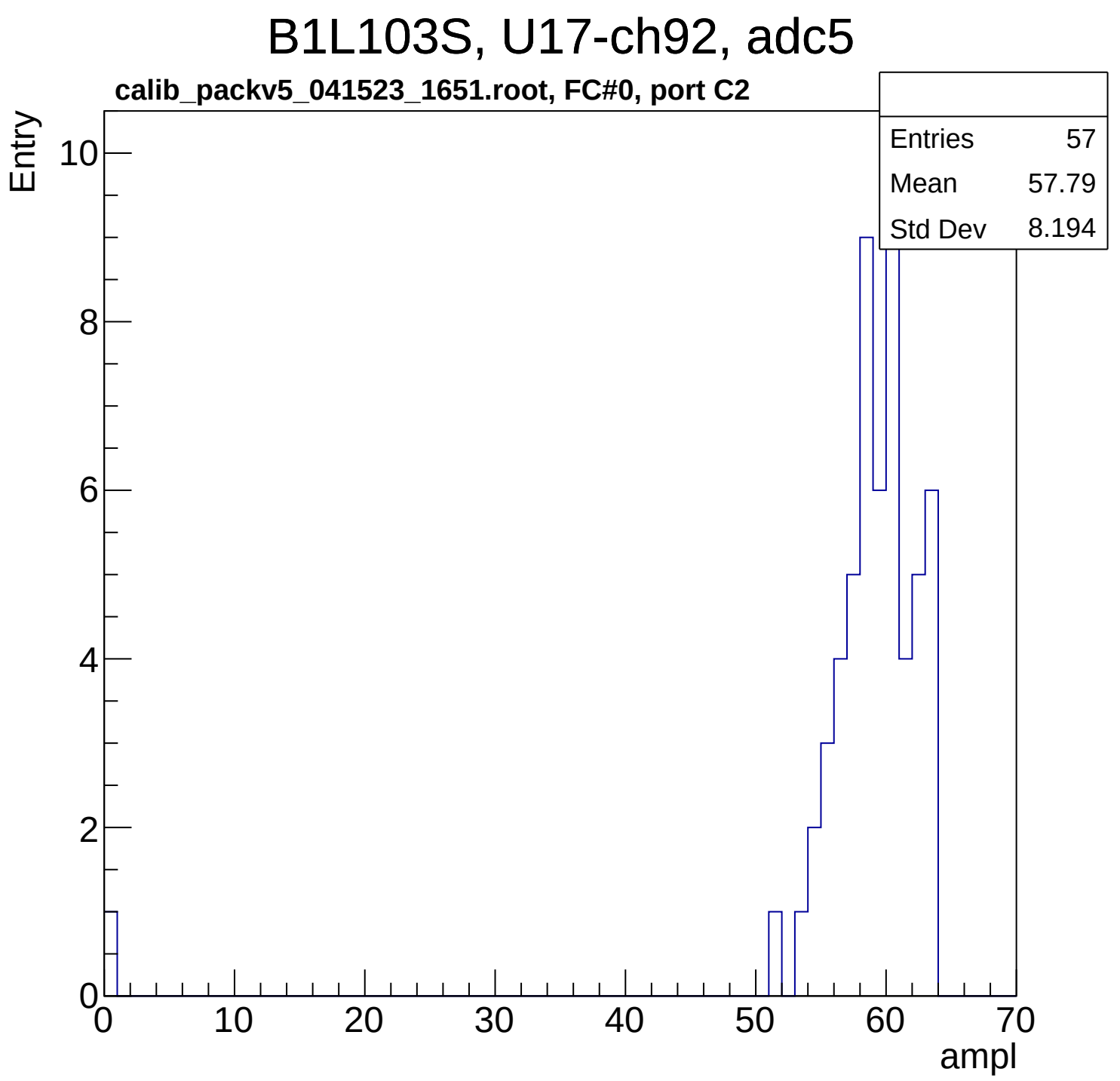

B1L103S, U17-ch92, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 24.48
Std Dev 9.442
Gaus mean : 28.2657
Gaus Width: 4.1851
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

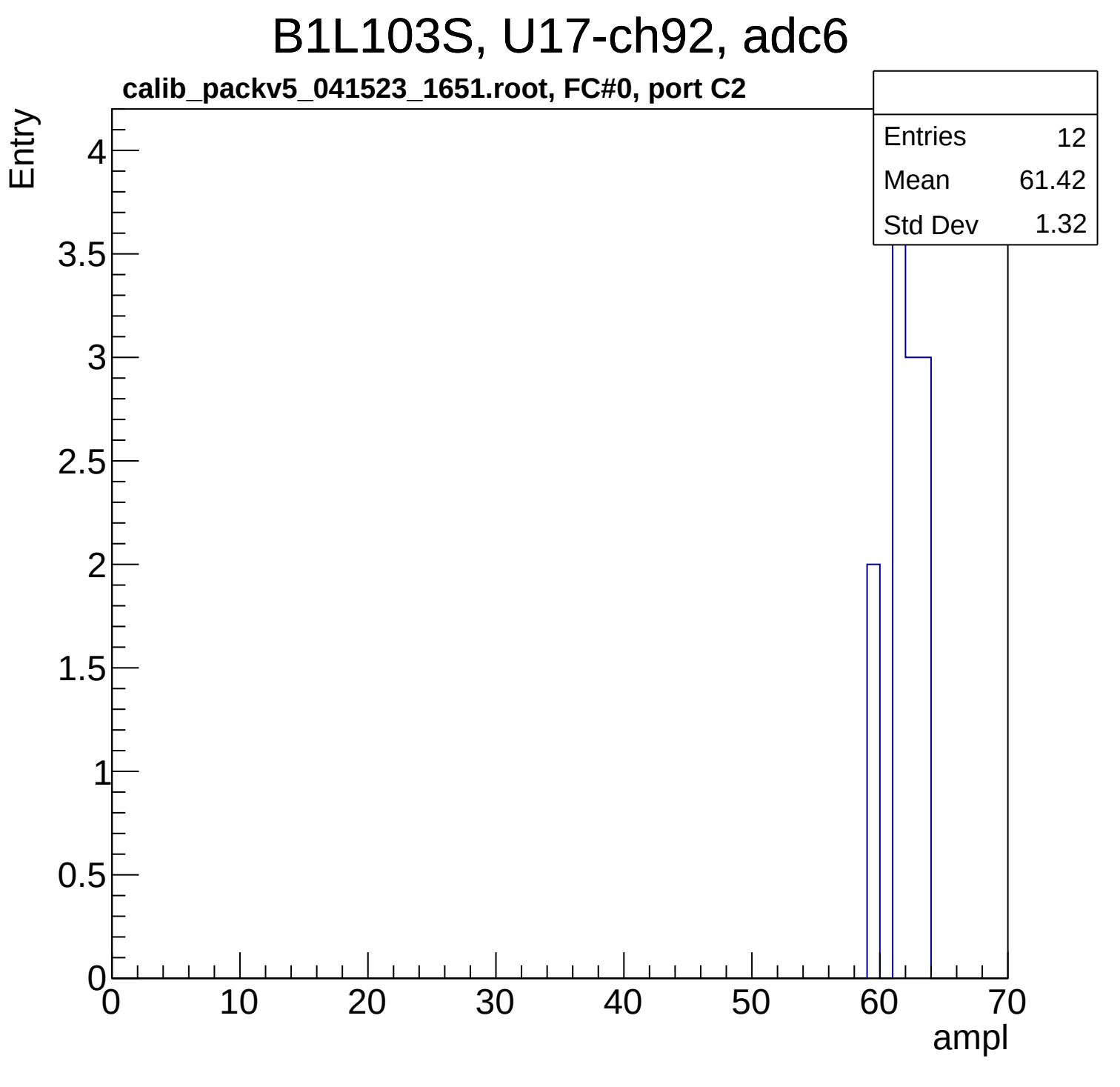

B1L103S, U17-ch92, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 33.81
Std Dev 5.811
Gaus mean : 34.8710
Gaus Width: 4.4933
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

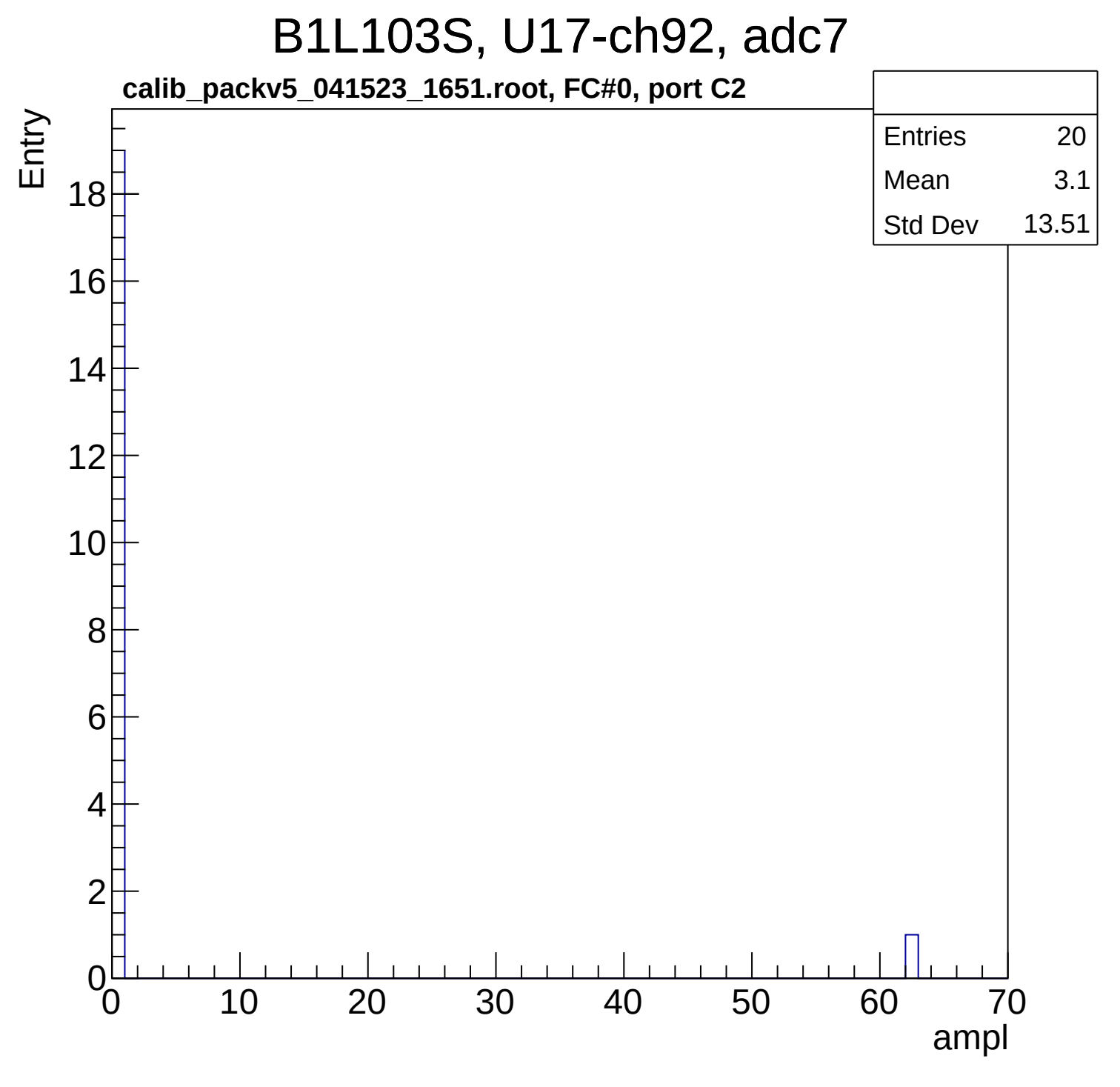

B1L103S, U17-ch92, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 36.7
Std Dev 11.97
Gaus mean : 40.4890
Gaus Width: 3.4346
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

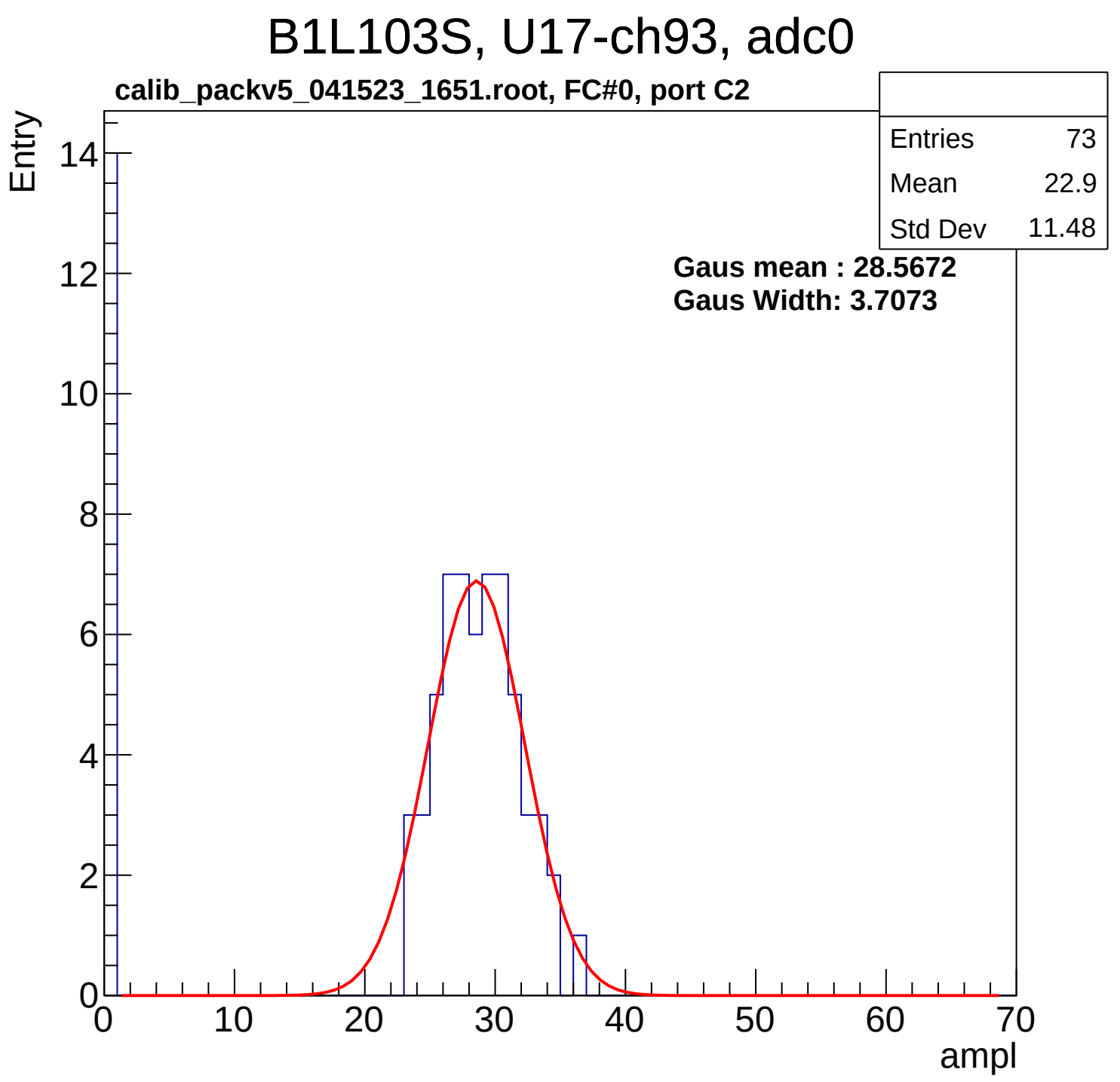

B1L103S, U17-ch92, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 44.55
Std Dev 12.96
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

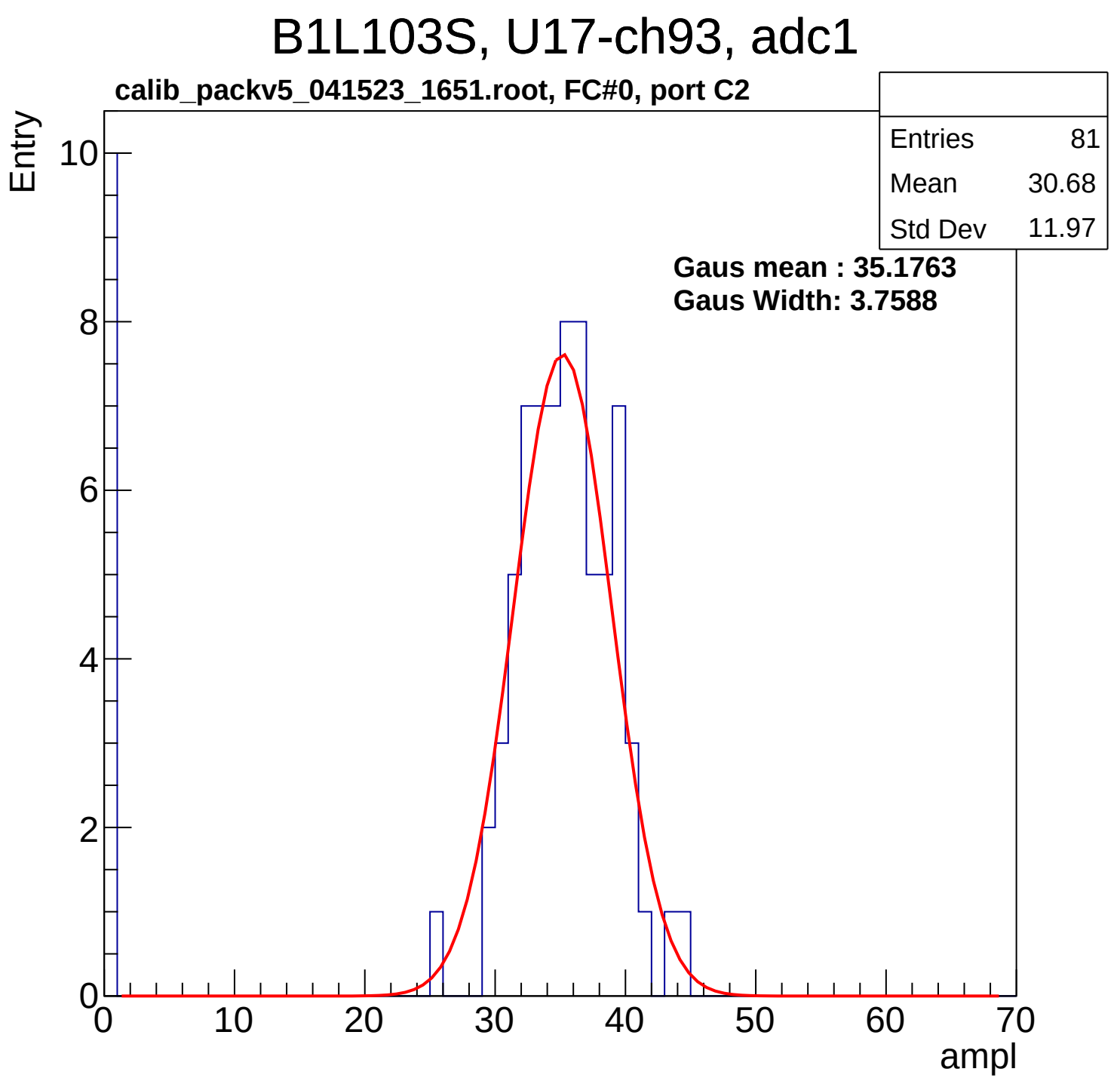

B1L103S, U17-ch92, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 54.77
Std Dev 3.711
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

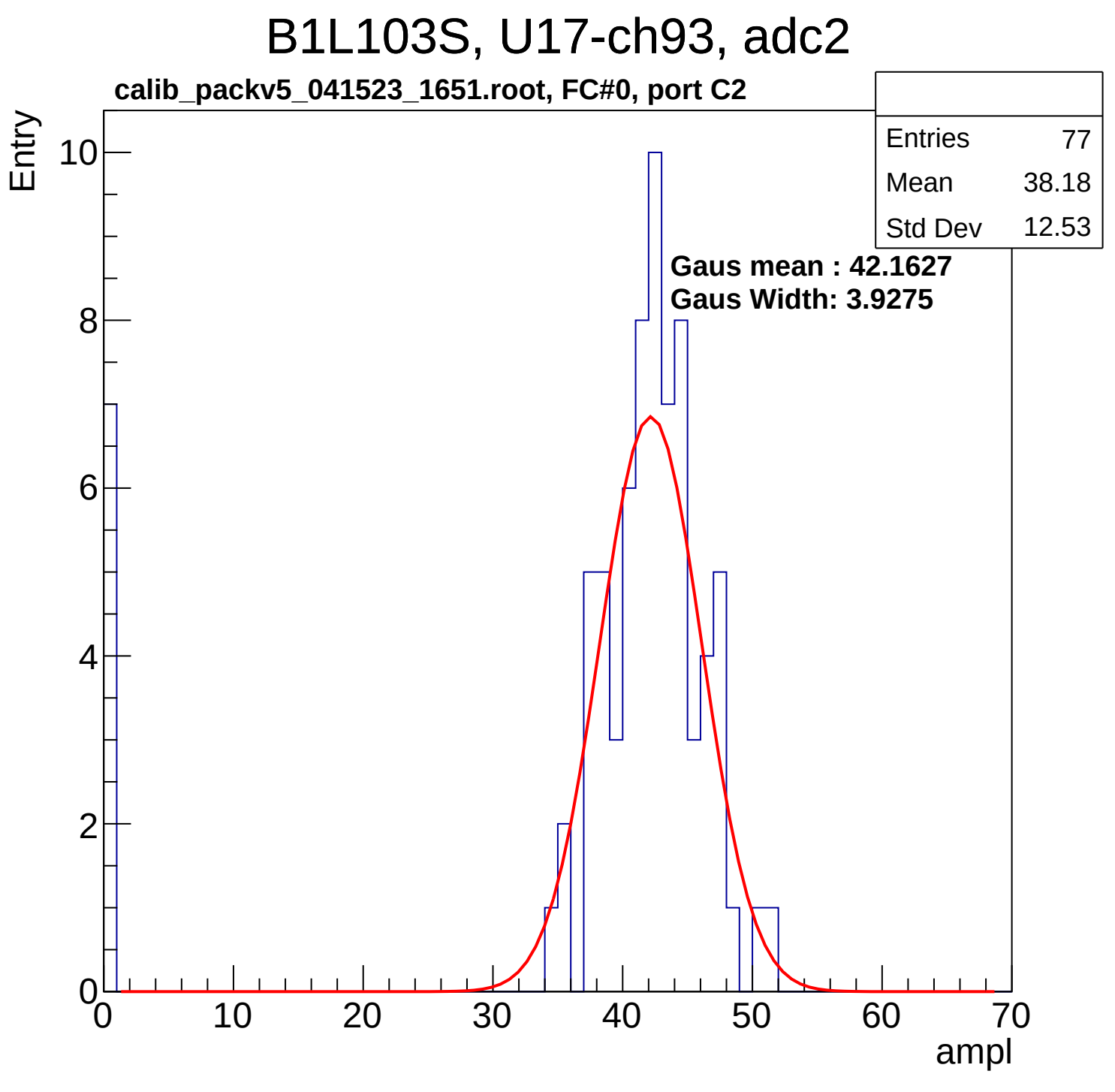

B1L103S, U17-ch92, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 57.79
Std Dev 8.194
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

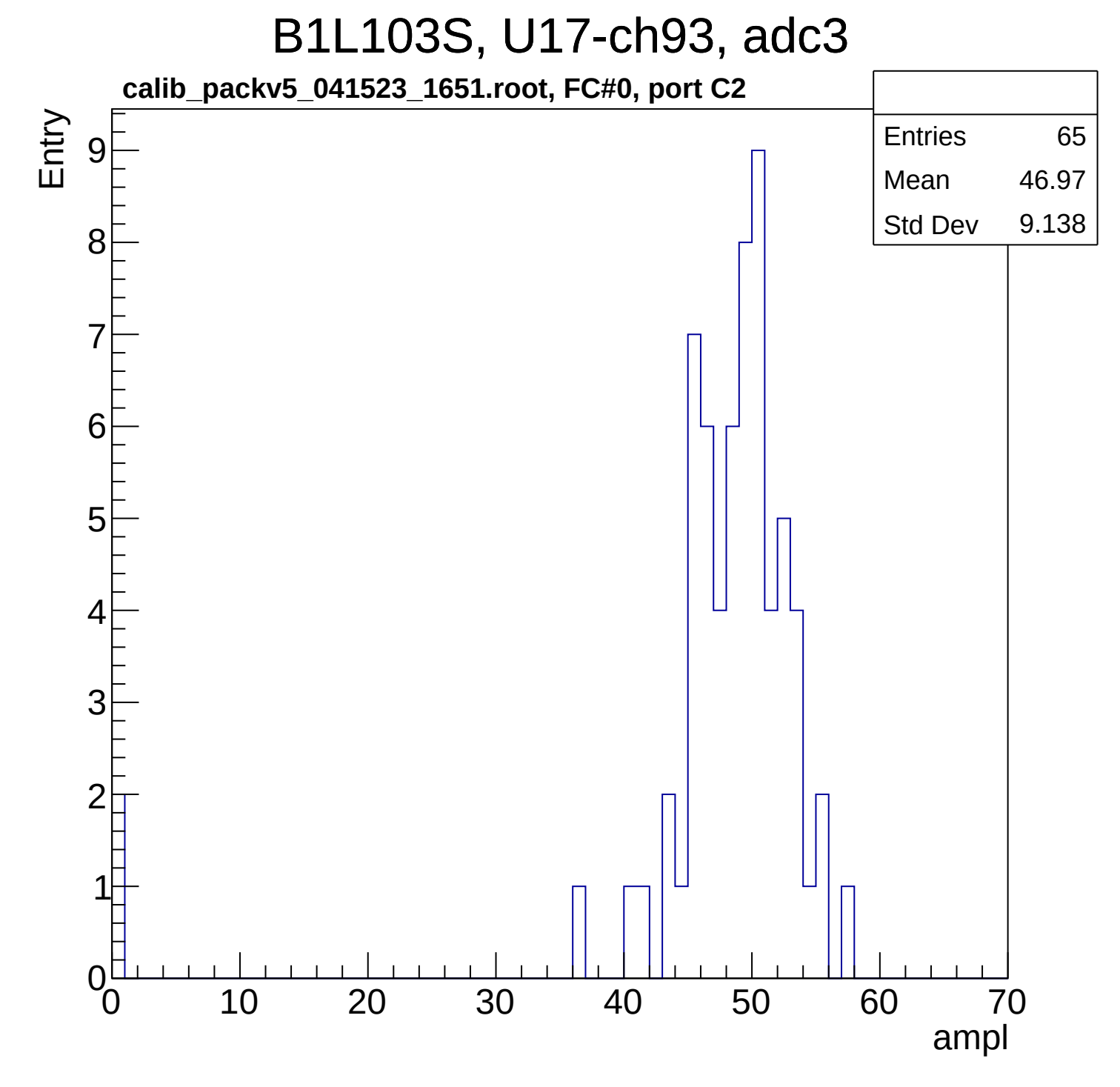

B1L103S, U17-ch92, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.42
Std Dev 1.32
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

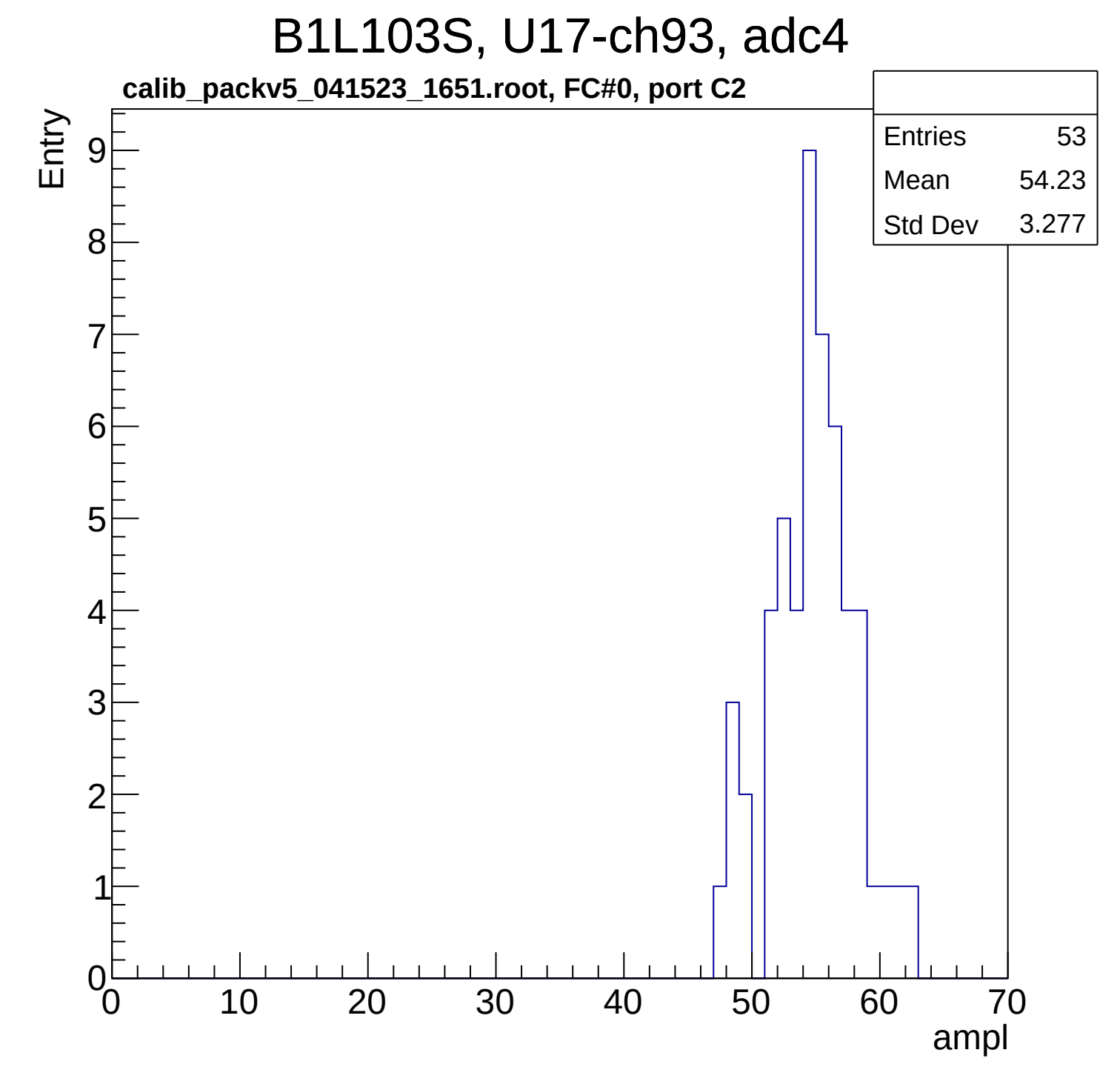

B1L103S, U17-ch92, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

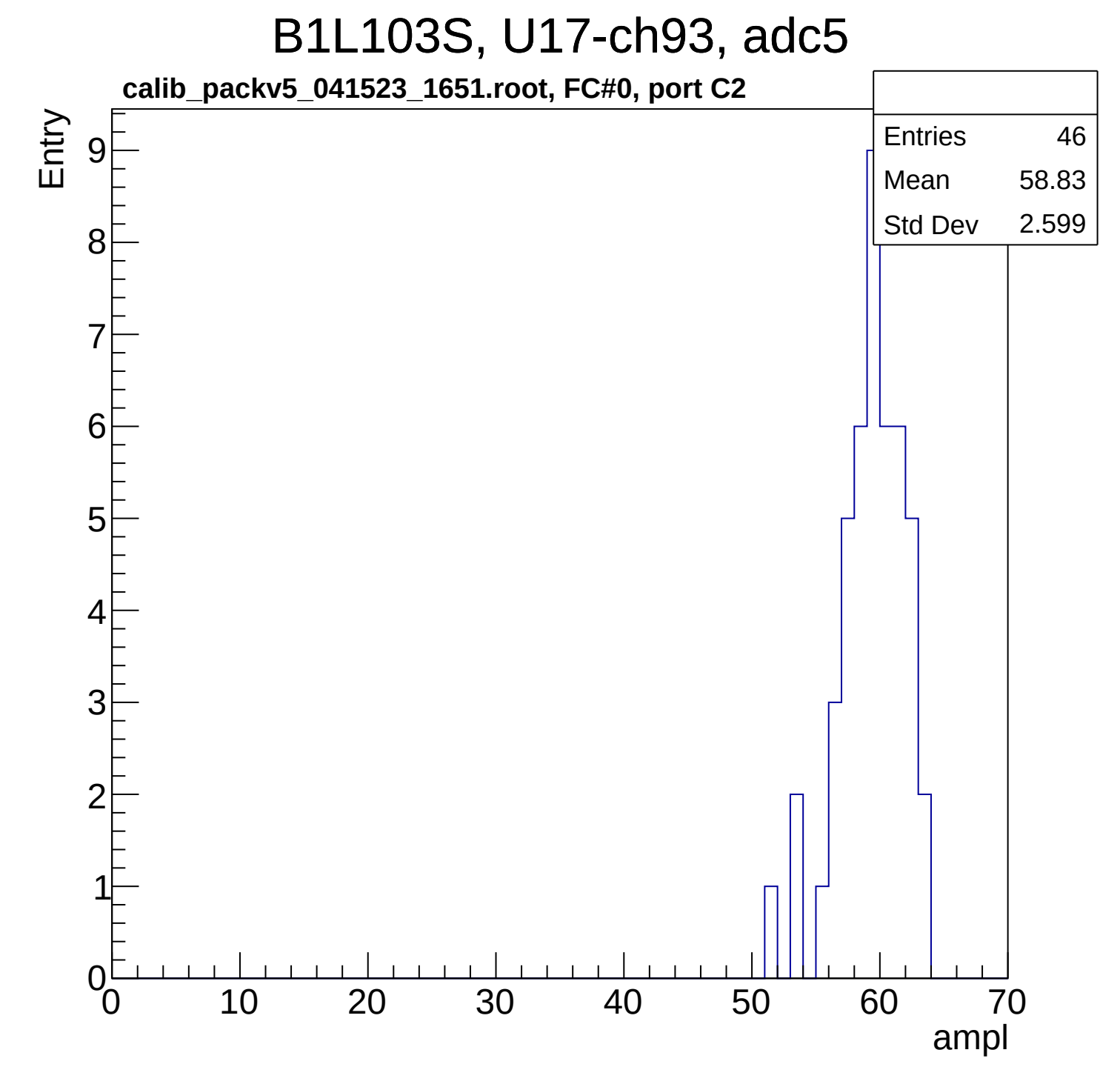

B1L103S, U17-ch93, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 22.9
Std Dev 11.48
Gaus mean : 28.5672
Gaus Width: 3.7073
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

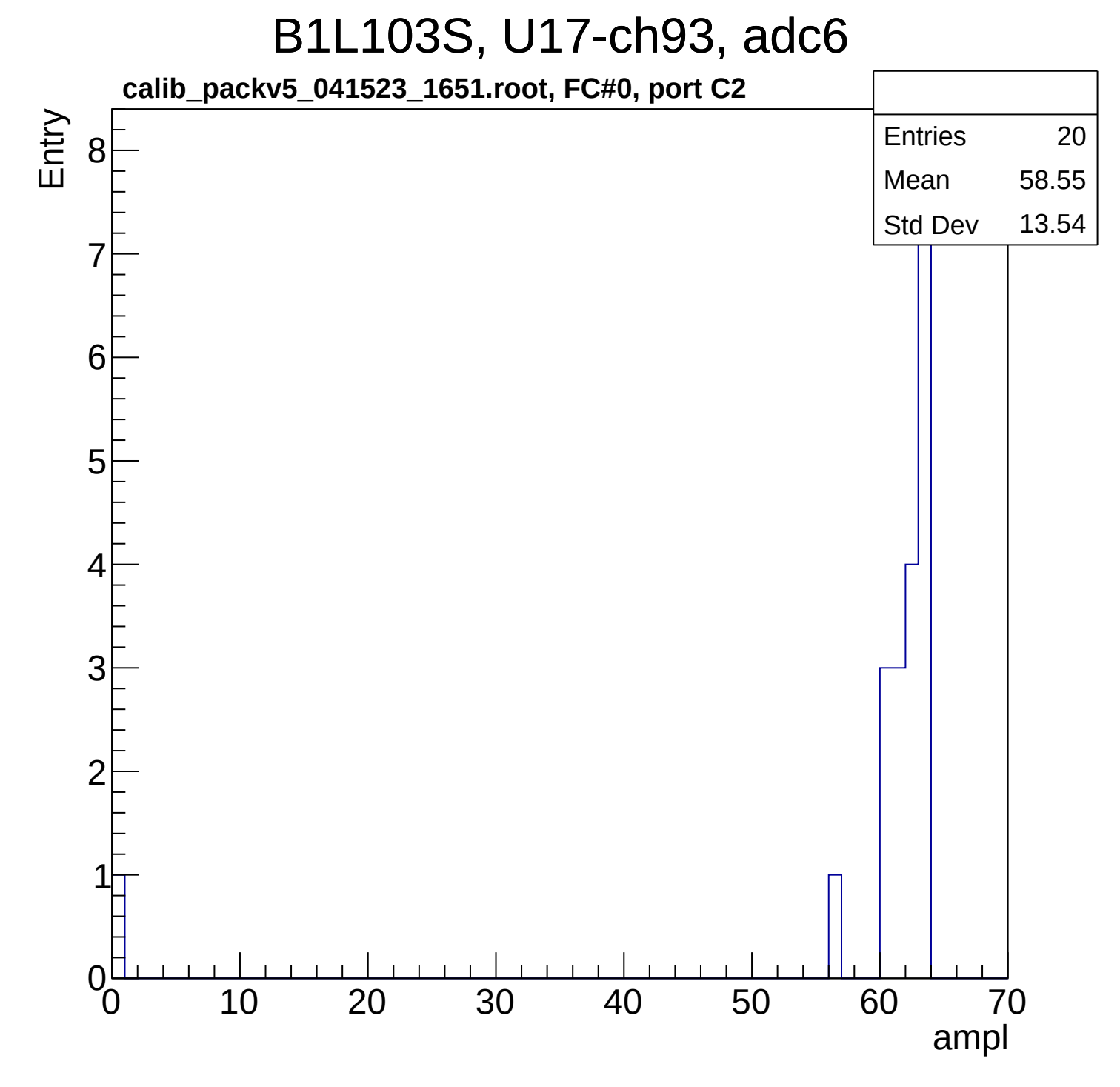

B1L103S, U17-ch93, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 30.68
Std Dev 11.97
Gaus mean : 35.1763
Gaus Width: 3.7588
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

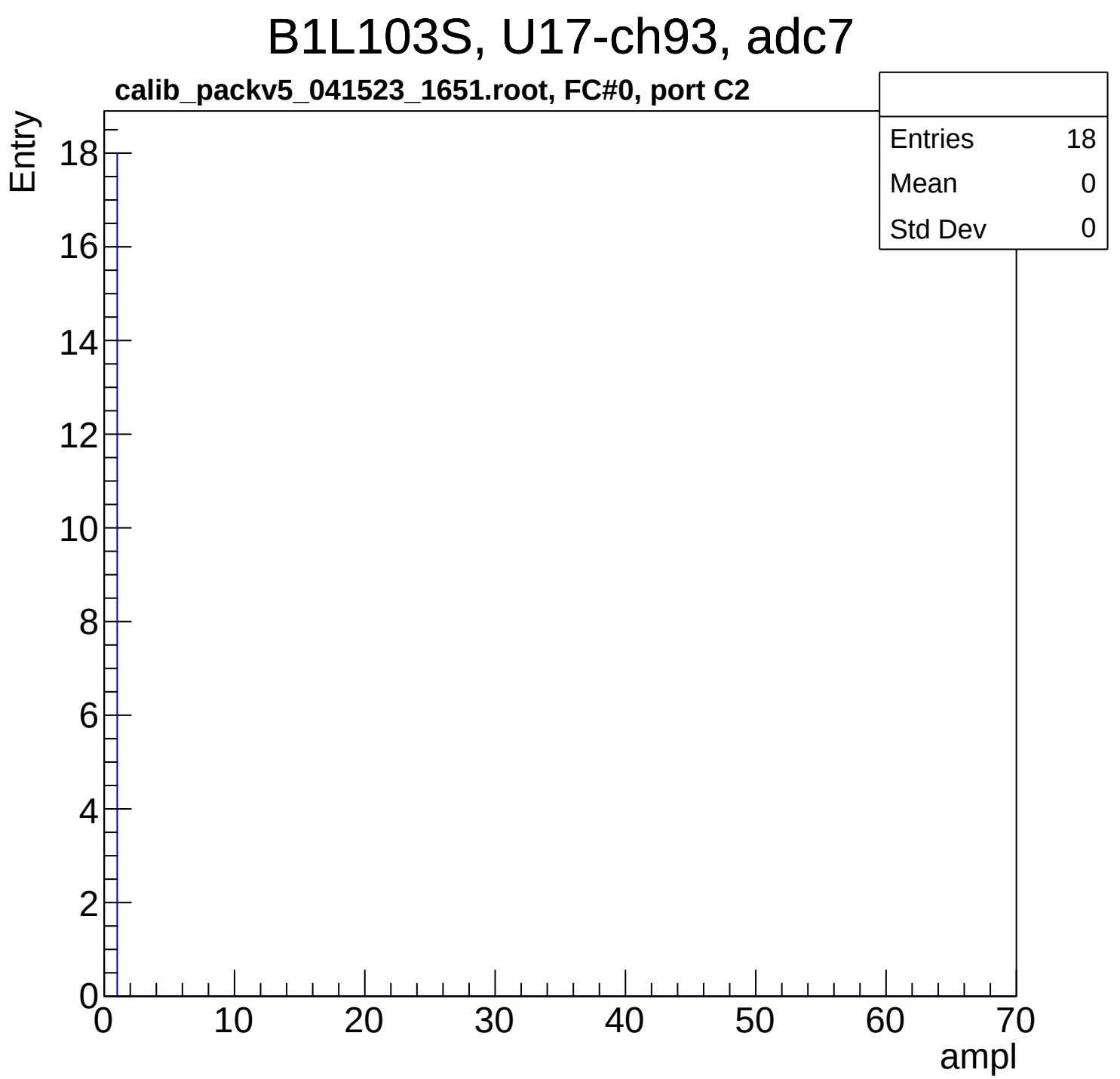

B1L103S, U17-ch93, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 38.18
Std Dev 12.53
Gaus mean : 42.1627
Gaus Width: 3.9275
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

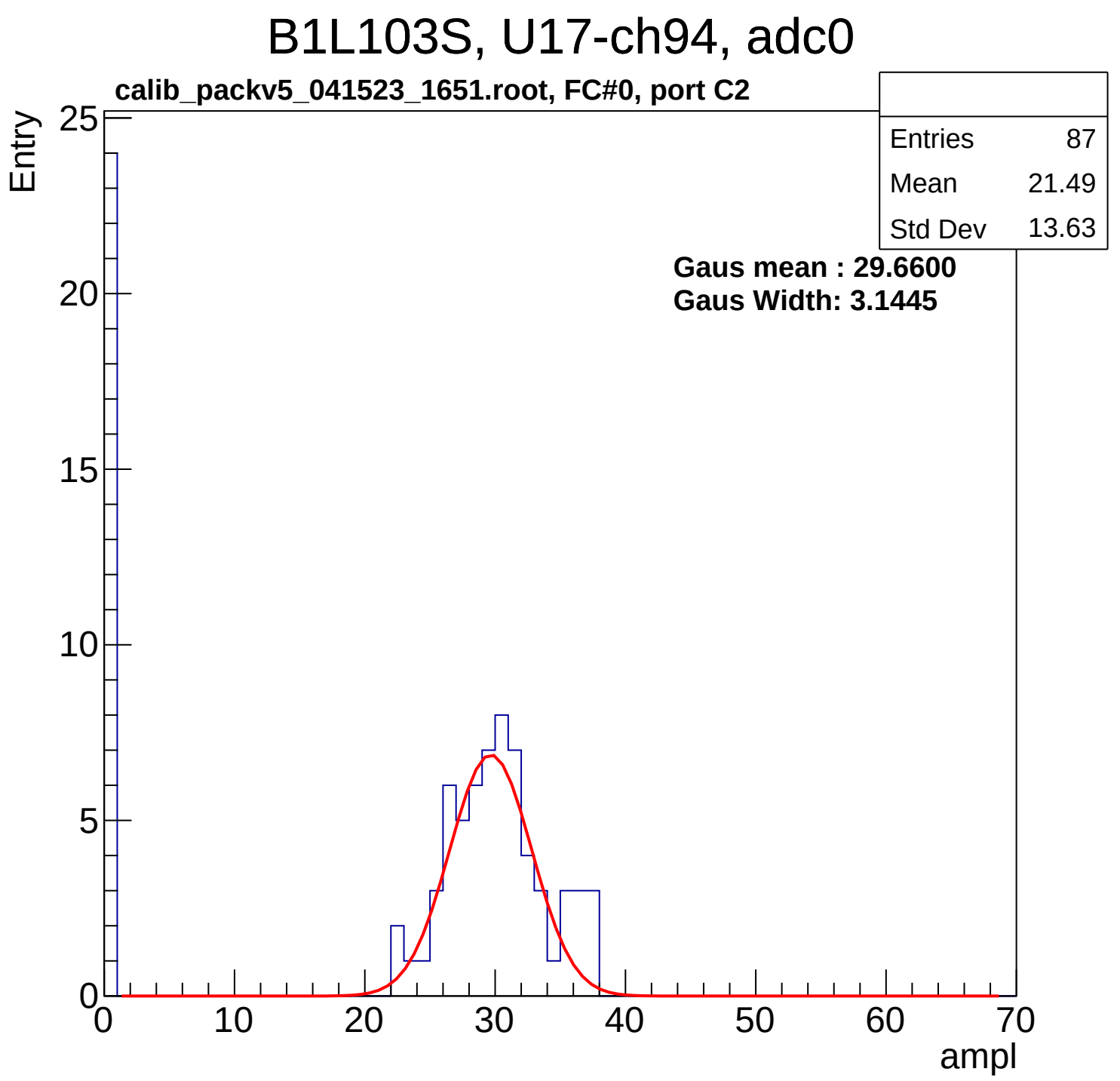

B1L103S, U17-ch93, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 46.97
Std Dev 9.138
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

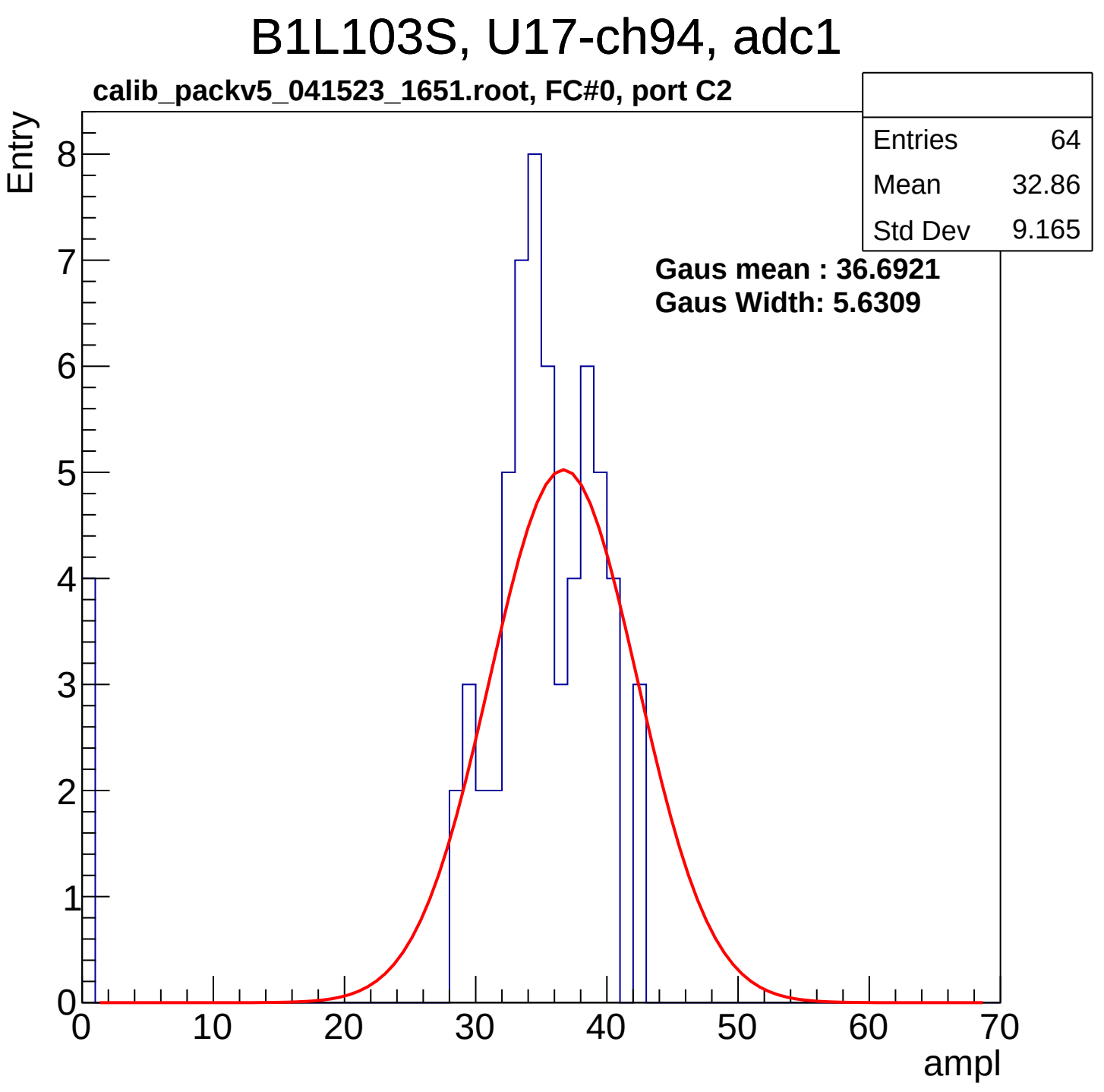

B1L103S, U17-ch93, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 54.23
Std Dev 3.277
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

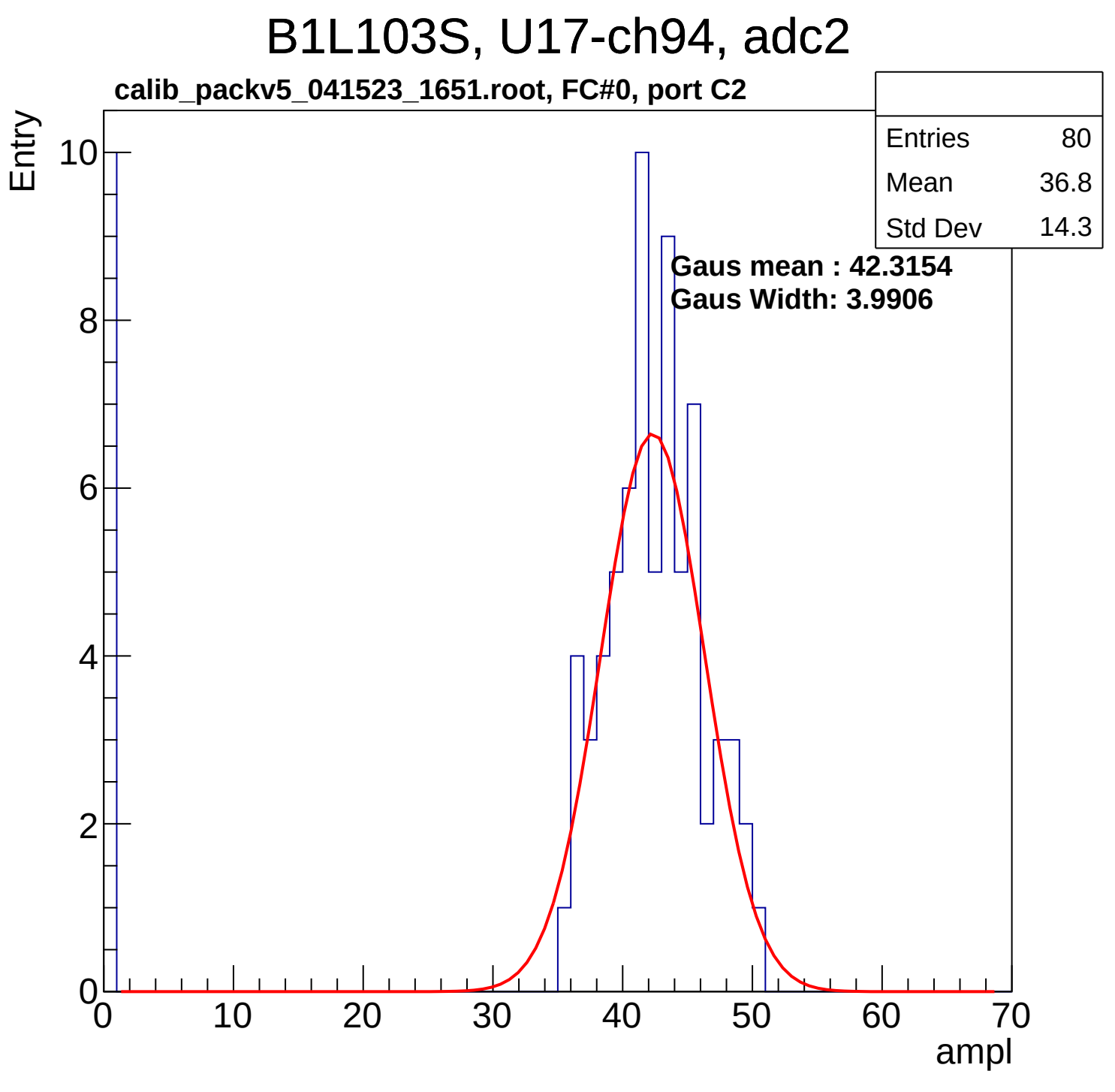

B1L103S, U17-ch93, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.83
Std Dev 2.599
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

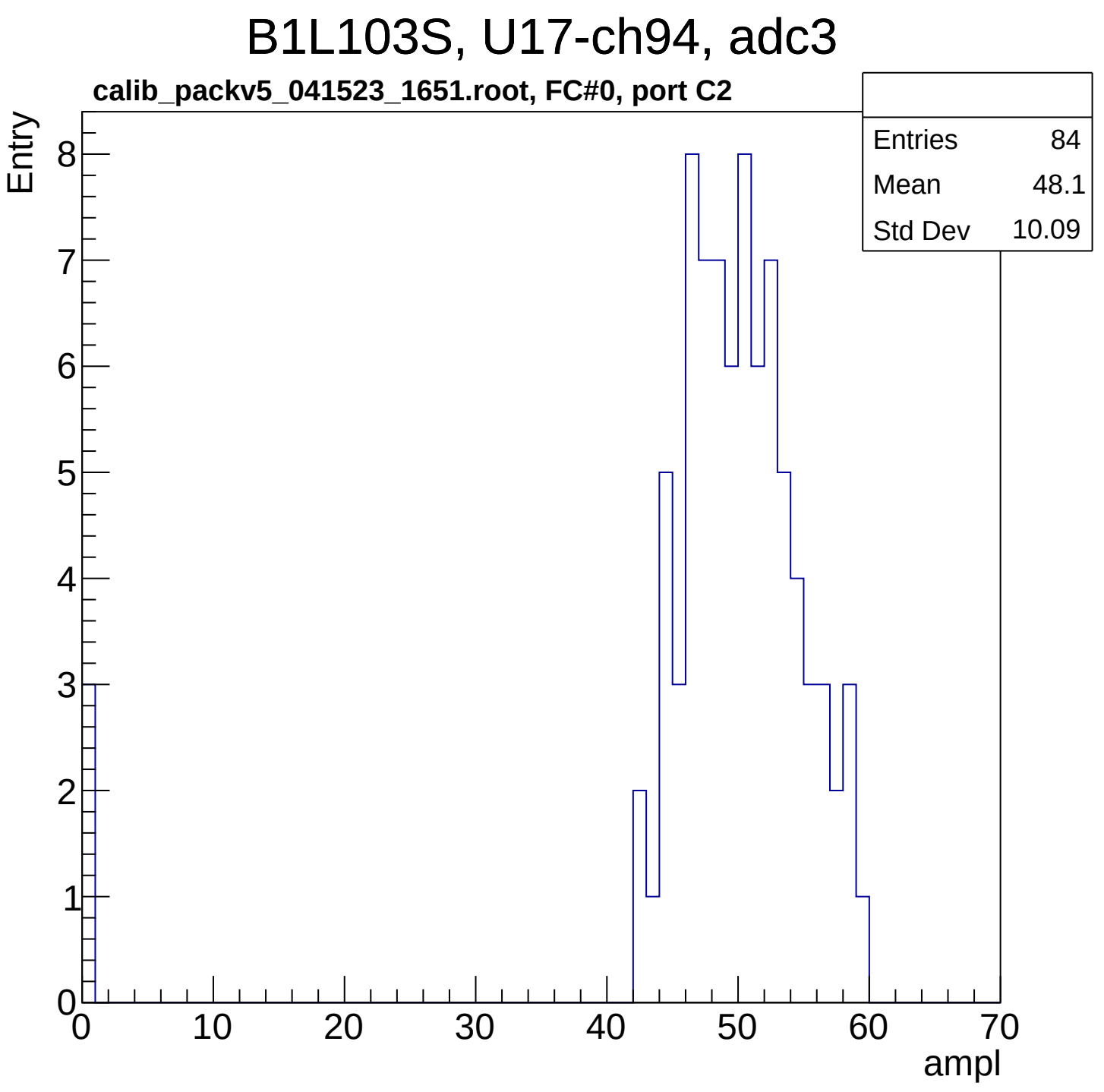

B1L103S, U17-ch93, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 58.55
Std Dev 13.54
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

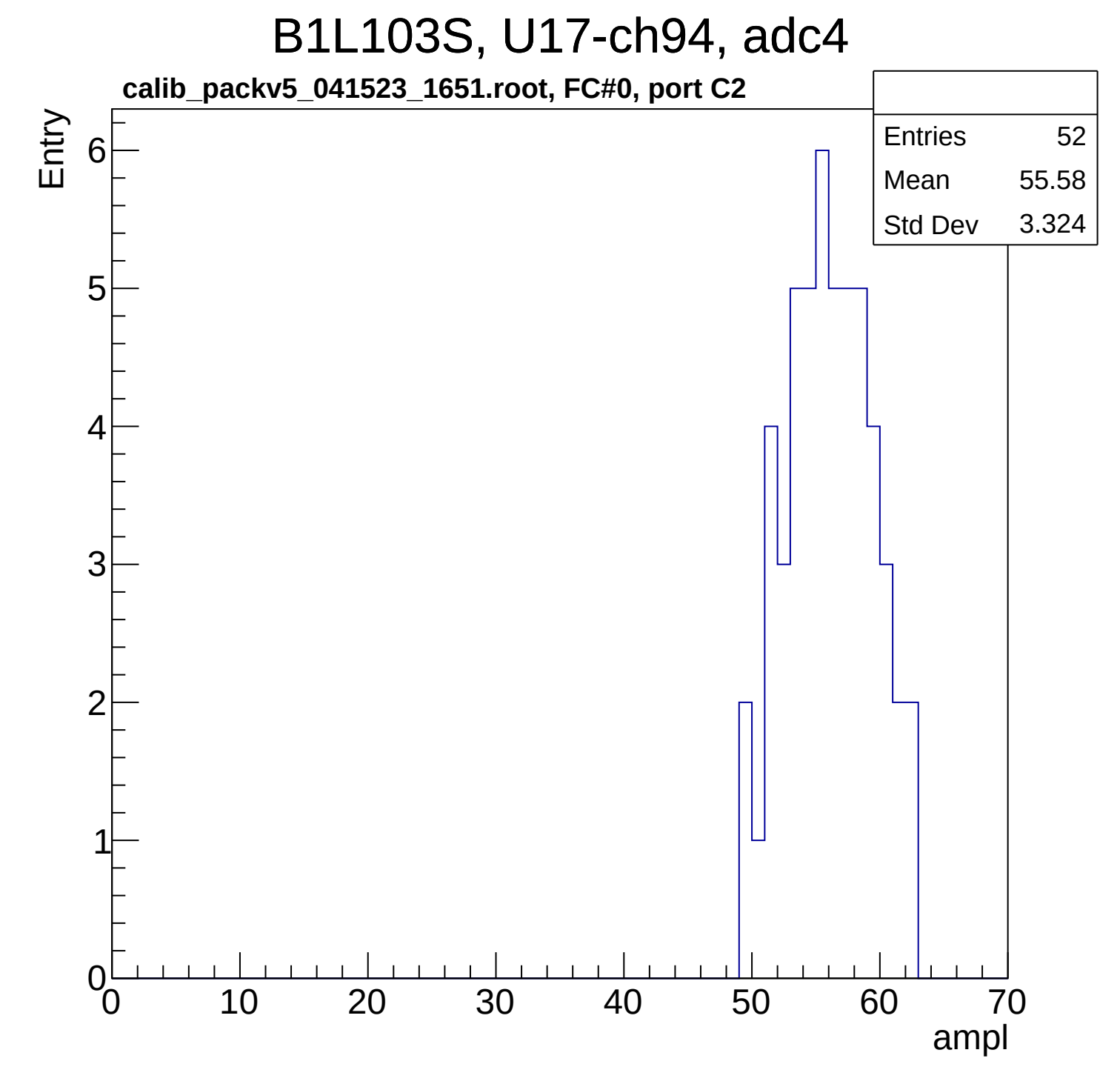

B1L103S, U17-ch93, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

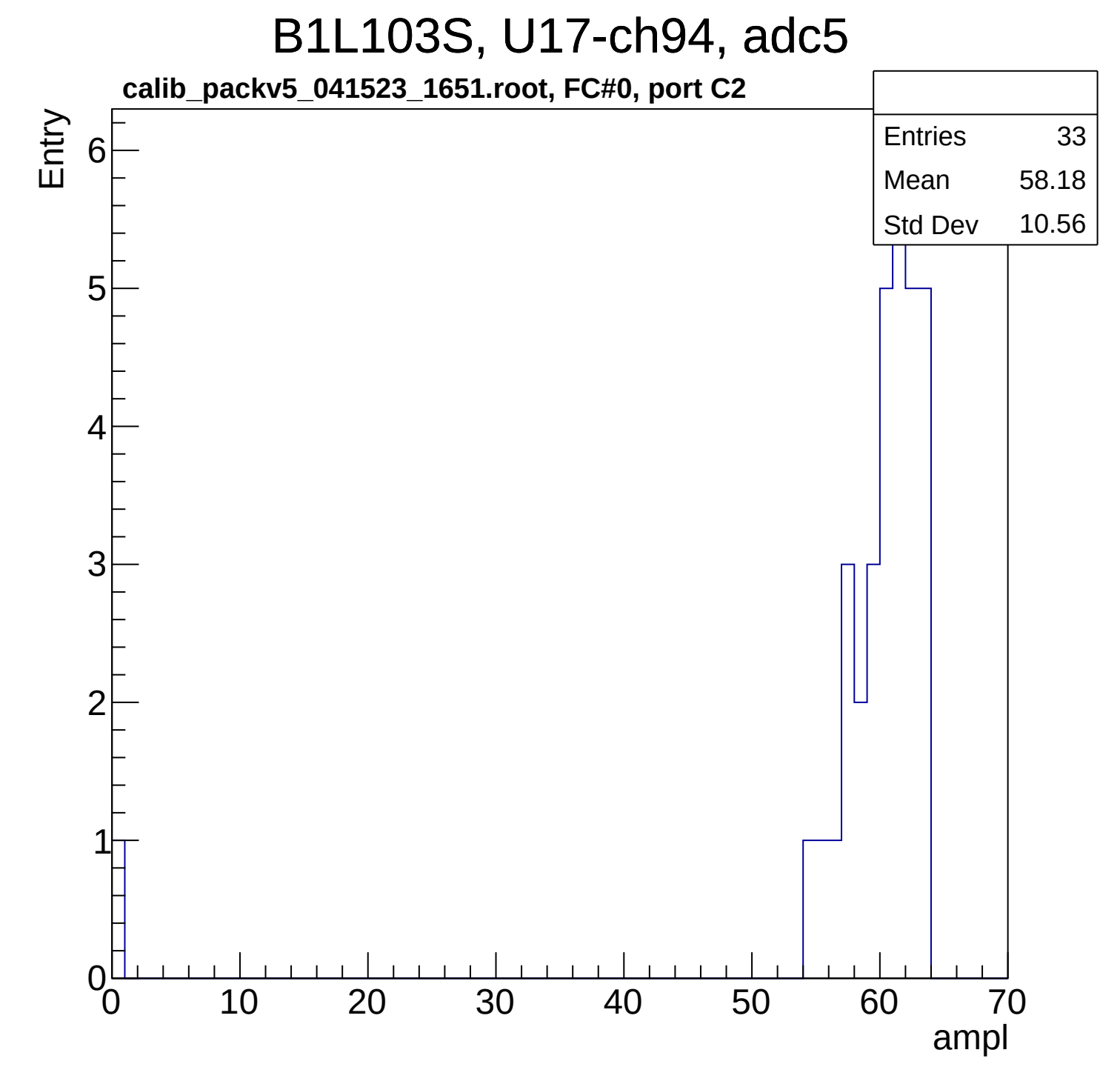

B1L103S, U17-ch94, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 21.49
Std Dev 13.63
Gaus mean : 29.6600
Gaus Width: 3.1445
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70

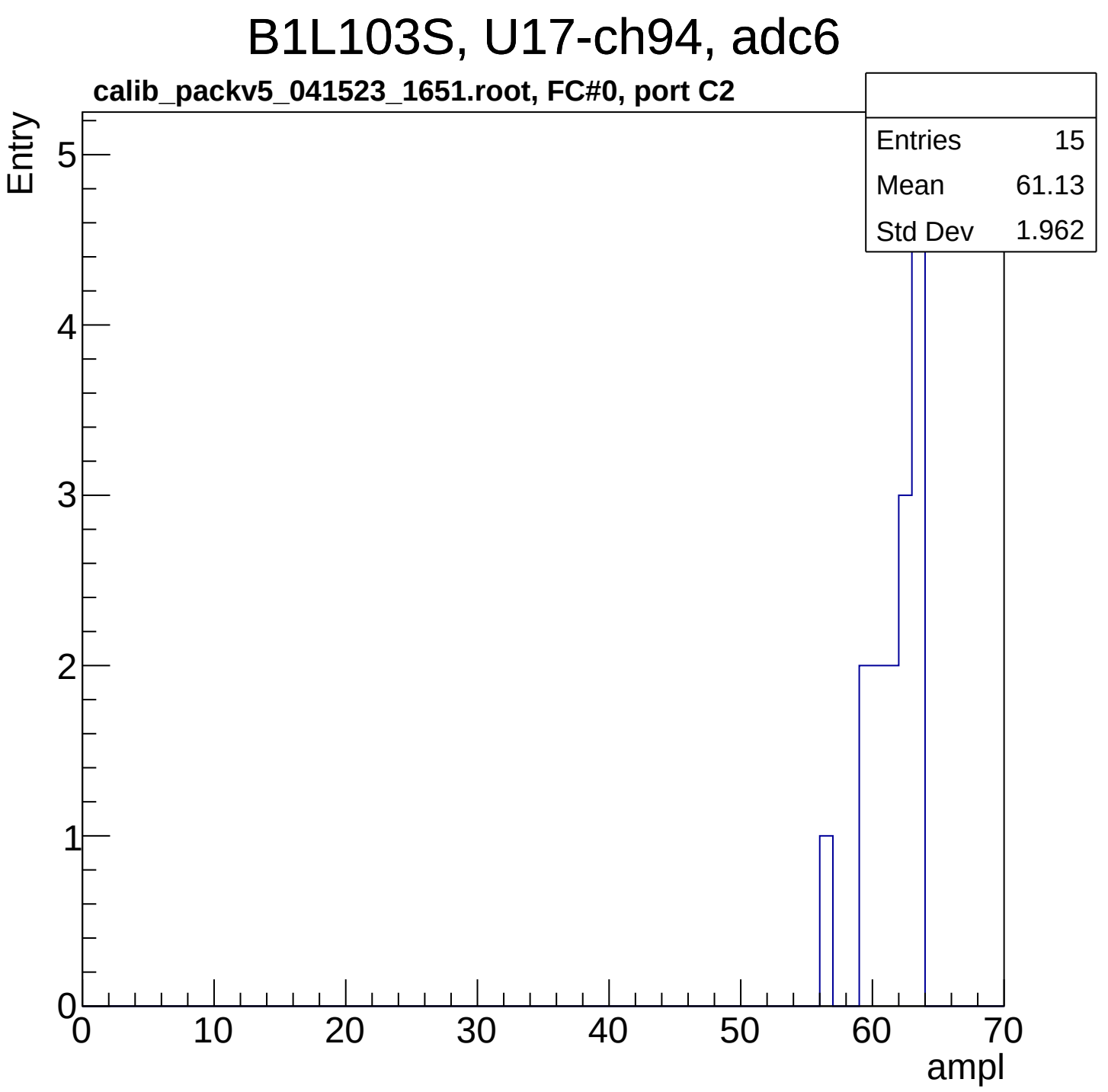

B1L103S, U17-ch94, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 32.86
Std Dev 9.165
Gaus mean : 36.6921
Gaus Width: 5.6309
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

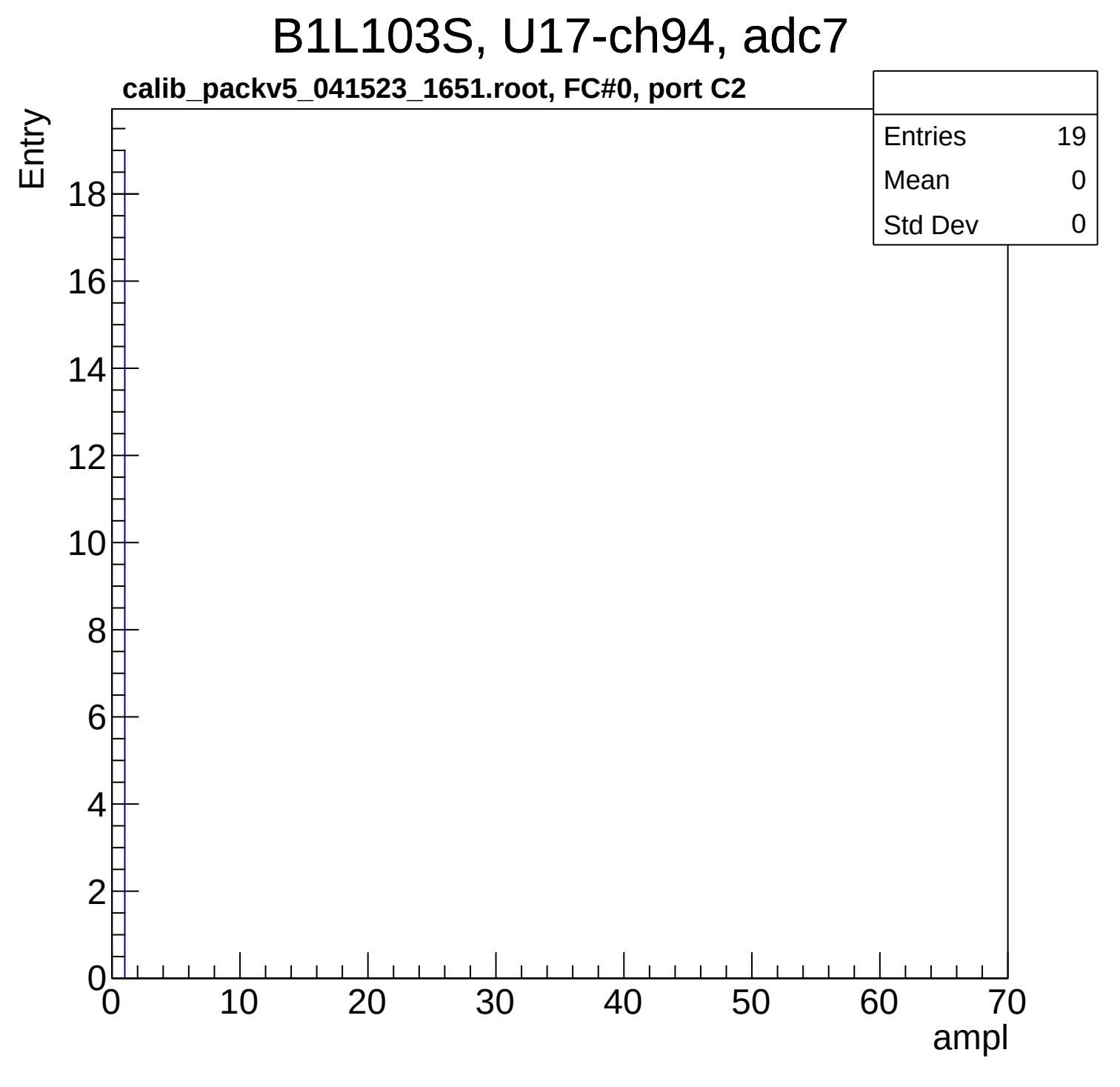

B1L103S, U17-ch94, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 36.8
Std Dev 14.3
Gaus mean : 42.3154
Gaus Width: 3.9906
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

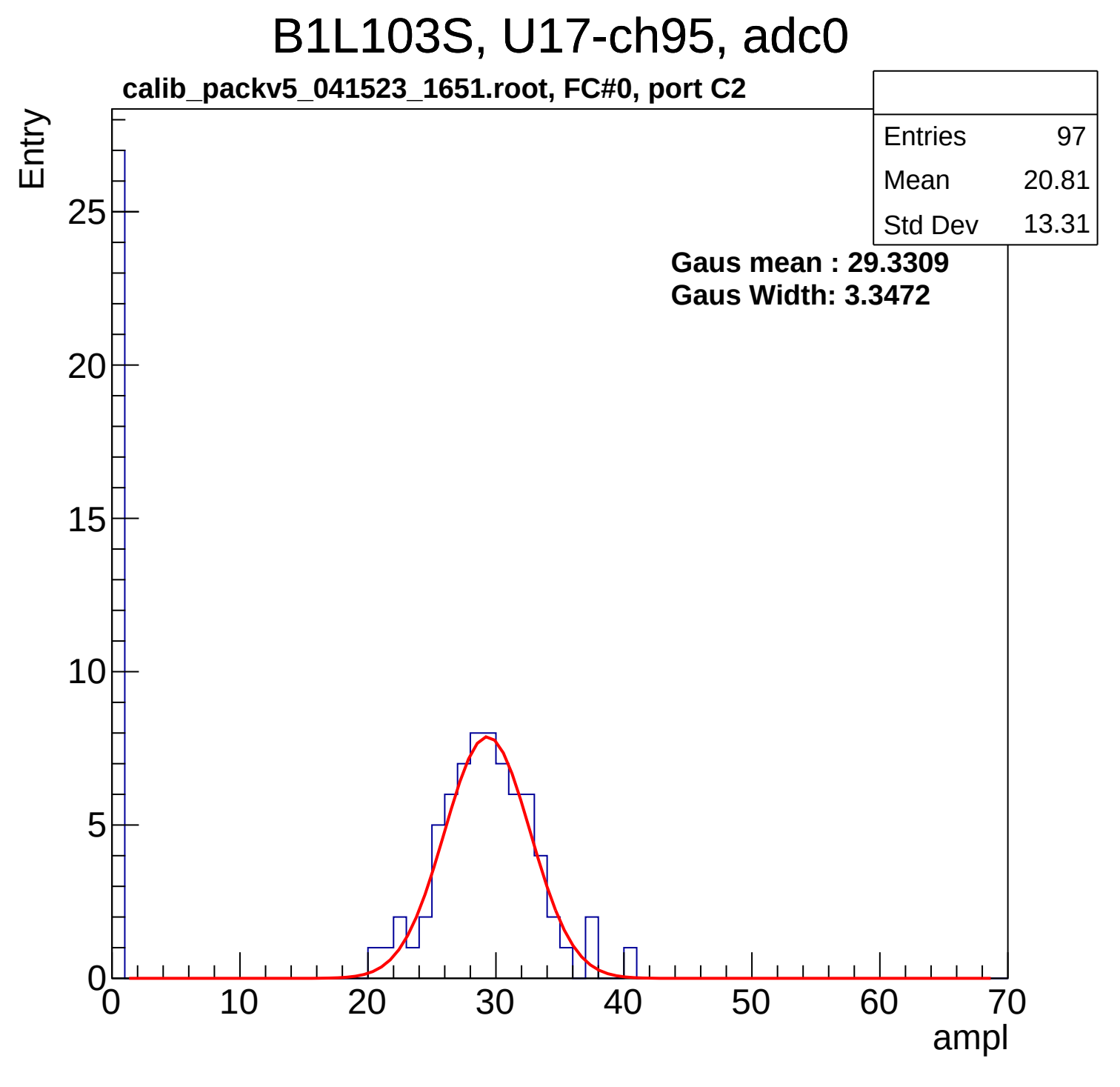

B1L103S, U17-ch94, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 48.1
Std Dev 10.09
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

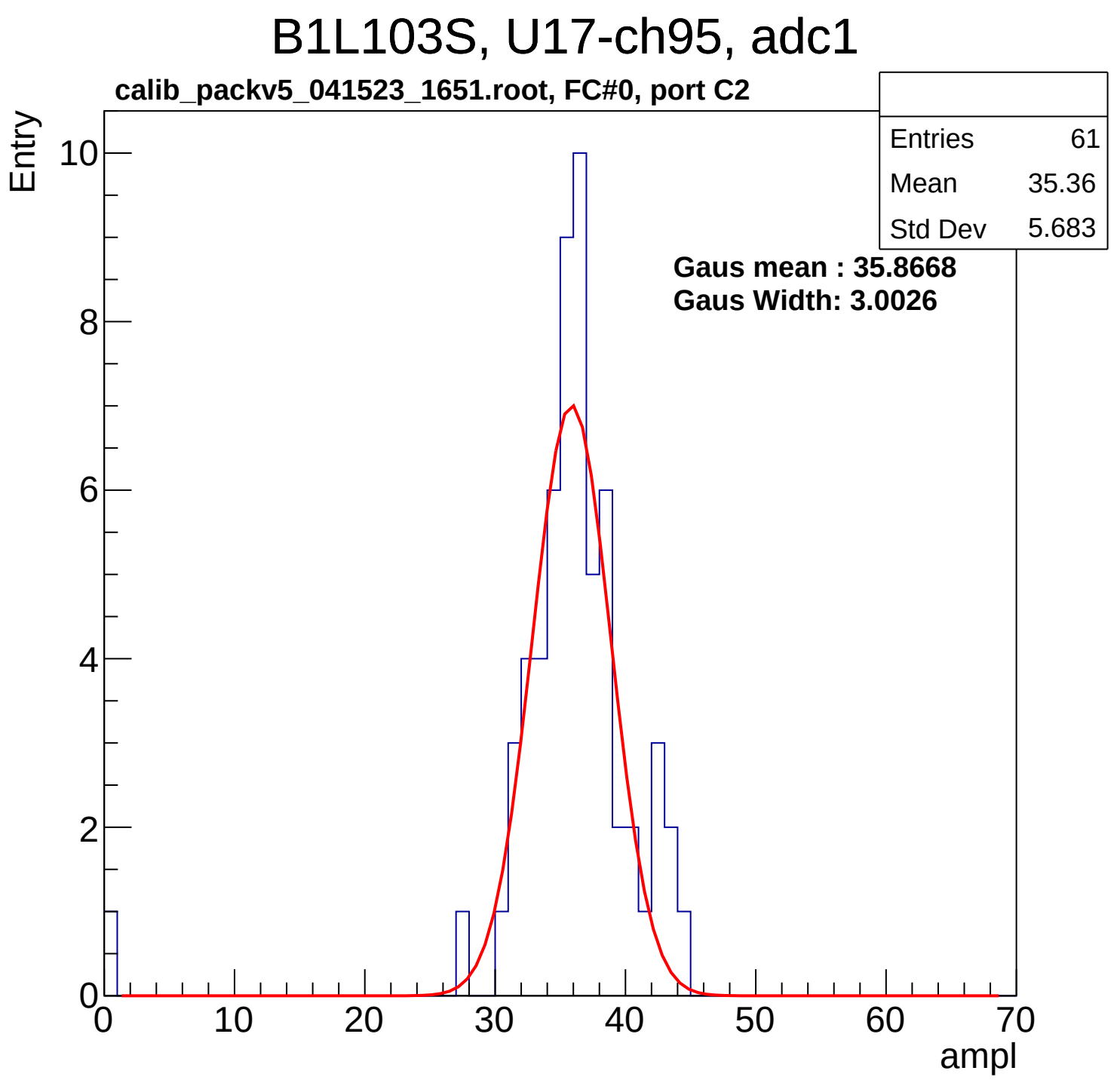

B1L103S, U17-ch94, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 55.58
Std Dev 3.324
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

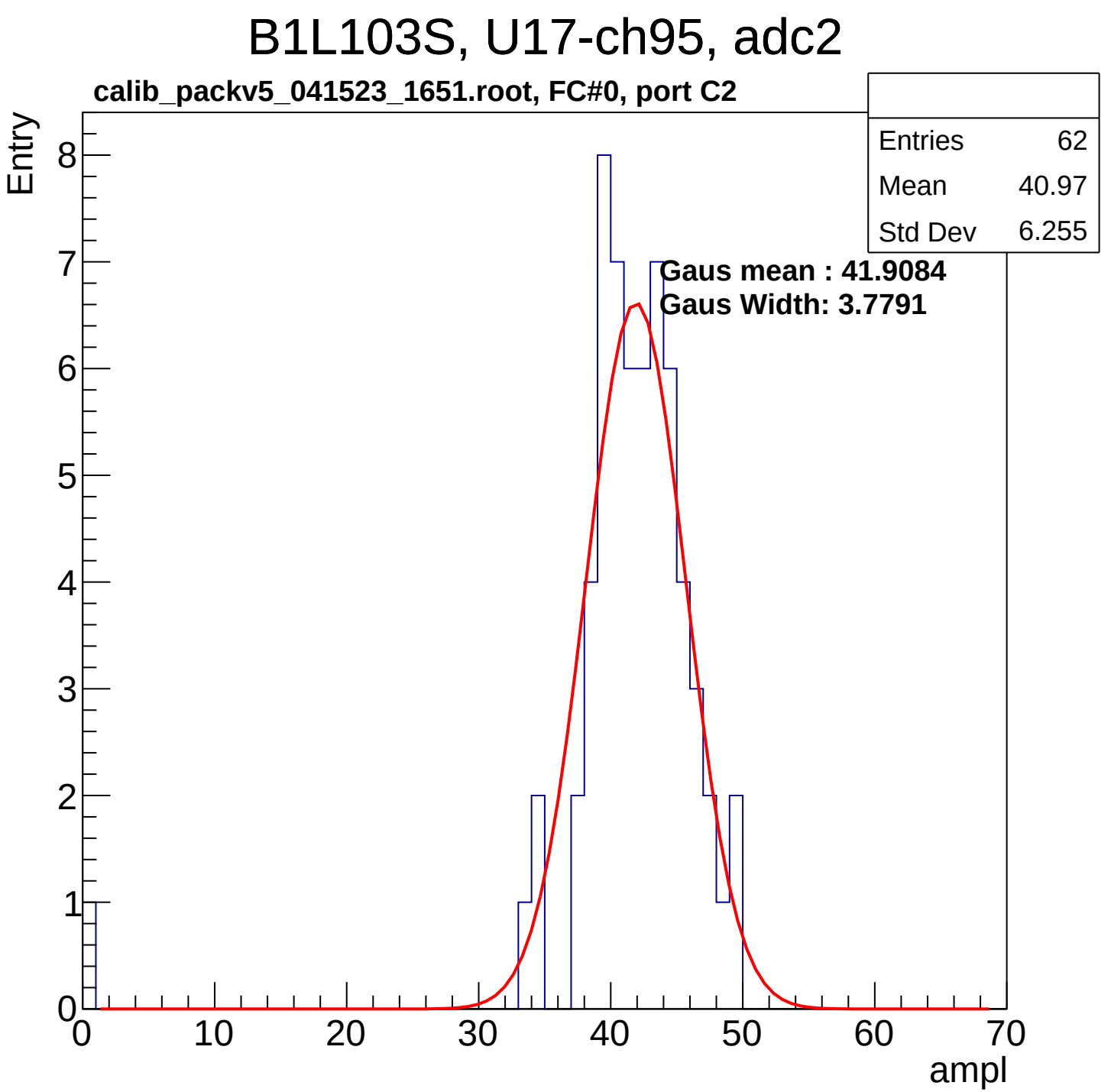

B1L103S, U17-ch94, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 58.18
Std Dev 10.56
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

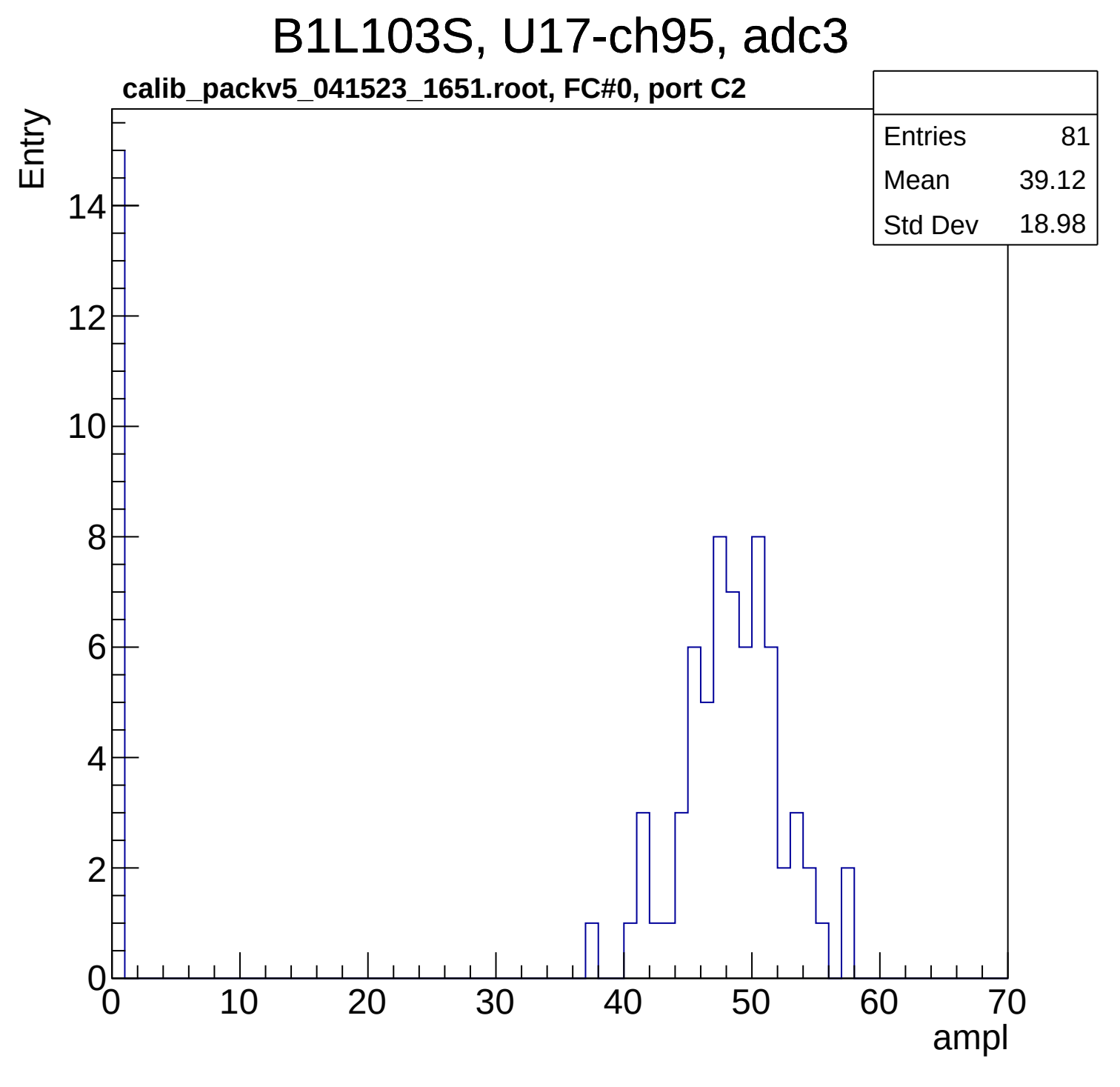

B1L103S, U17-ch94, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.13
Std Dev 1.962
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

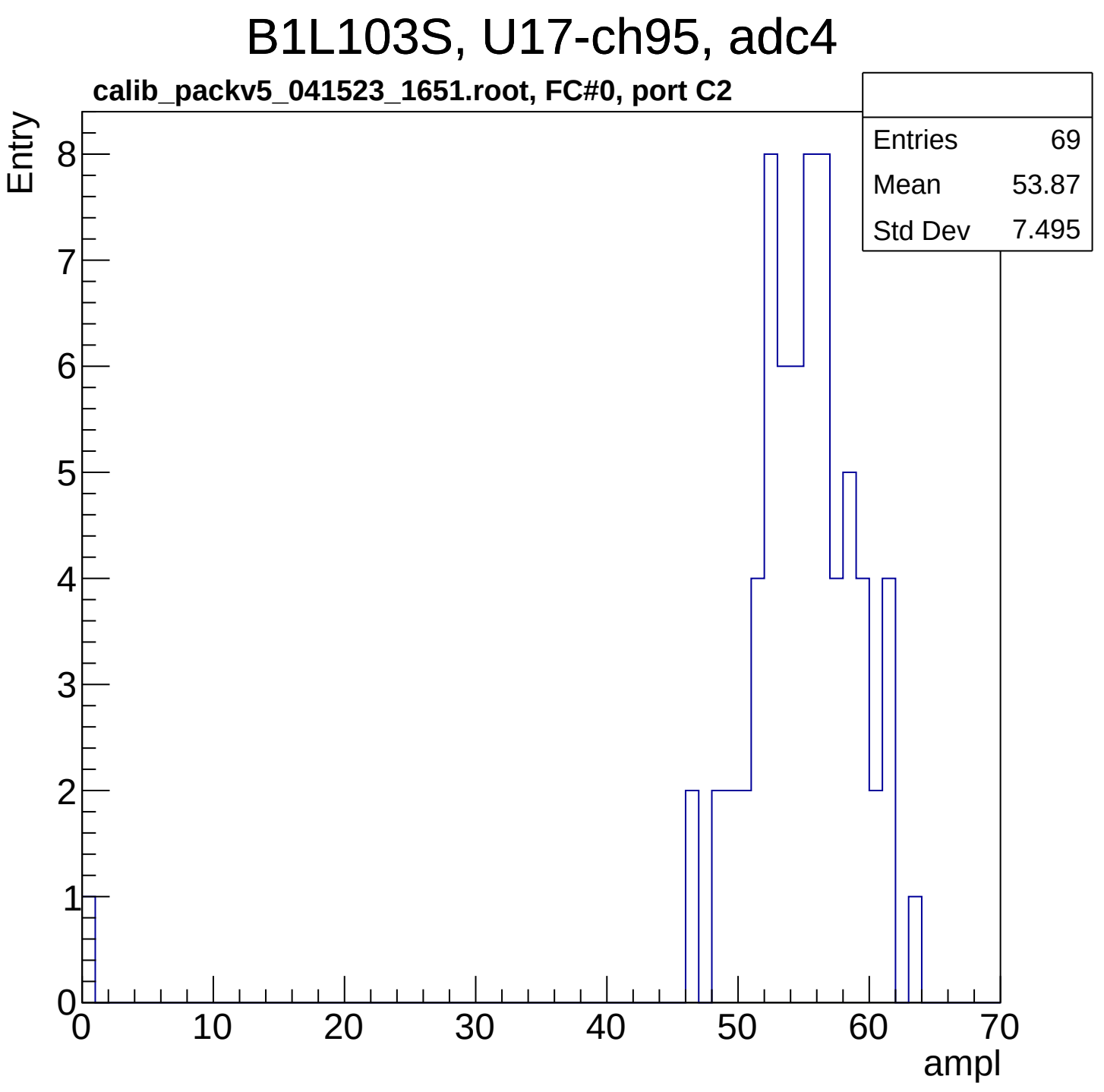

B1L103S, U17-ch94, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

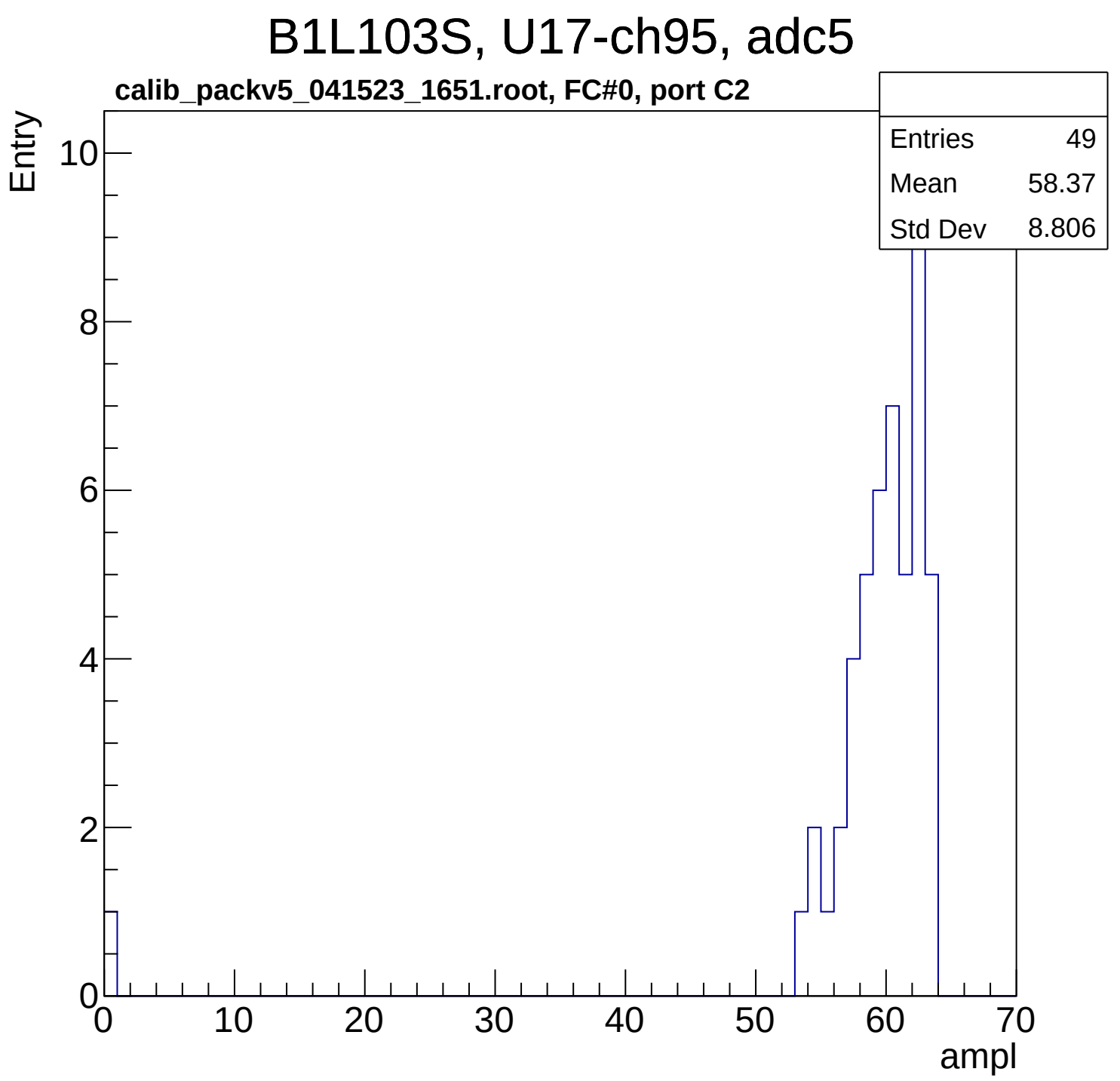

B1L103S, U17-ch95, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 20.81
Std Dev 13.31
Gaus mean : 29.3309
Gaus Width: 3.3472
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70

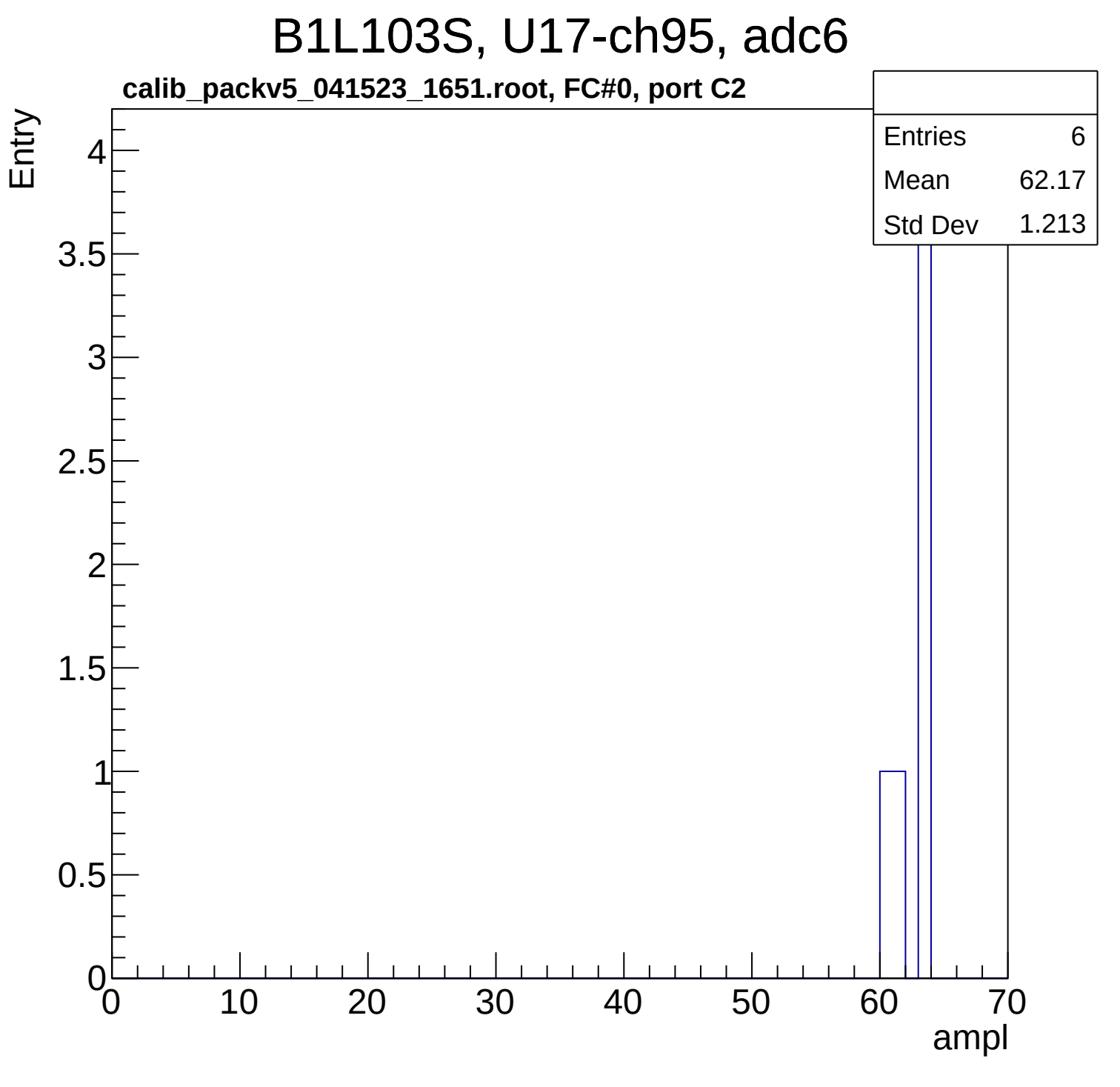

B1L103S, U17-ch95, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 35.36
Std Dev 5.683
Gaus mean : 35.8668
Gaus Width: 3.0026
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

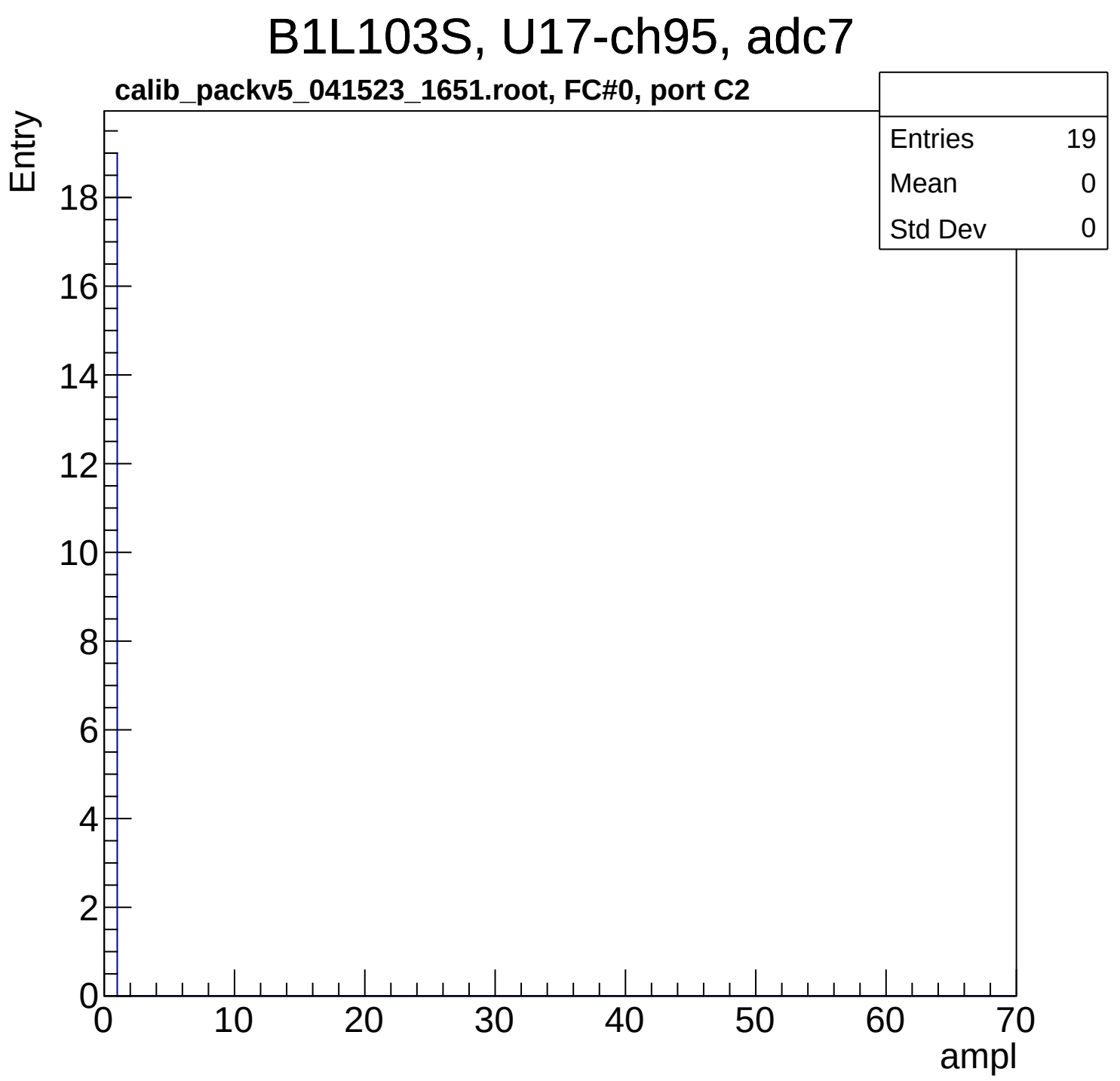

B1L103S, U17-ch95, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 40.97
Std Dev 6.255
Gaus mean : 41.9084
Gaus Width: 3.7791
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

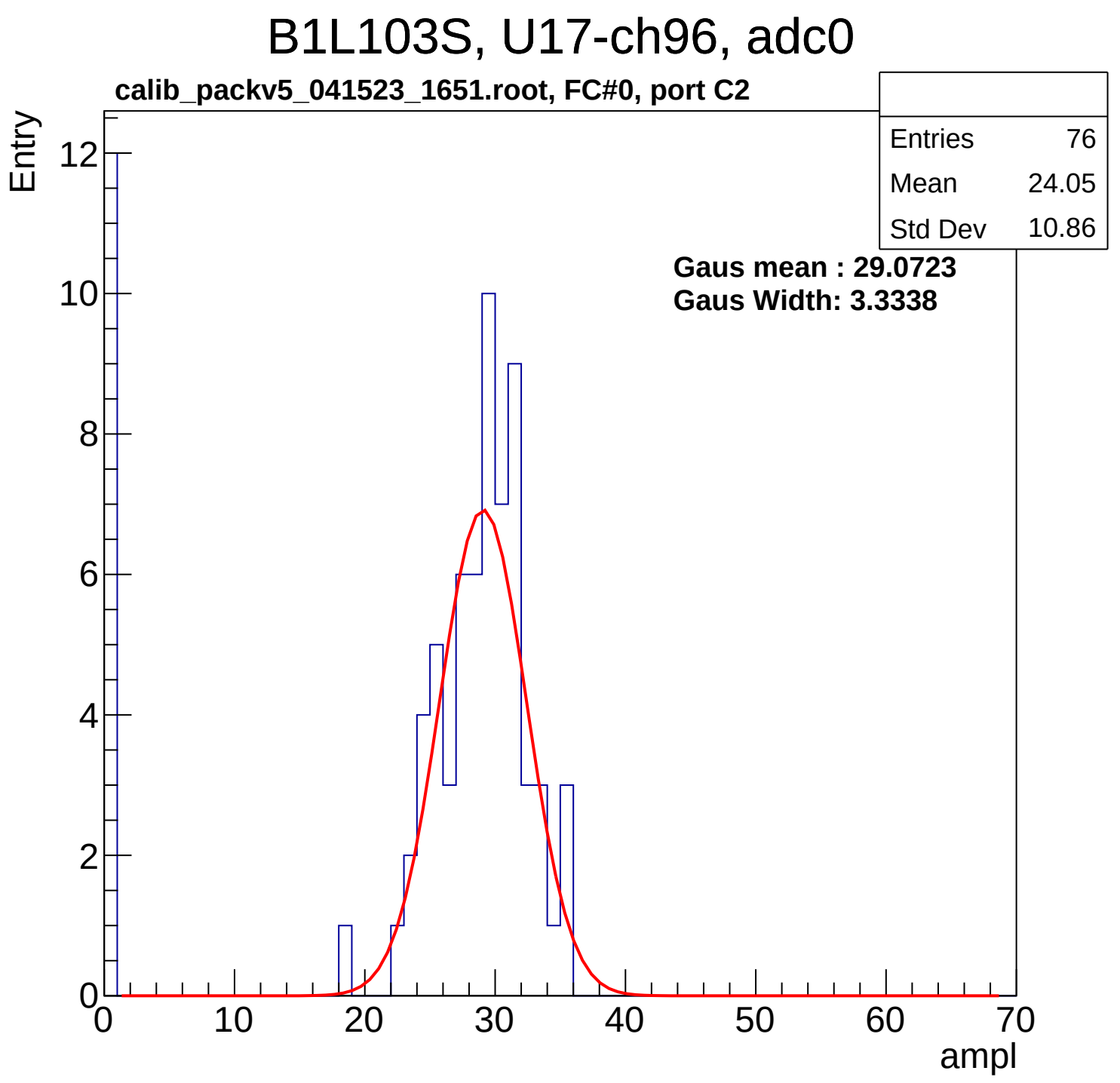

B1L103S, U17-ch95, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 39.12
Std Dev 18.98
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

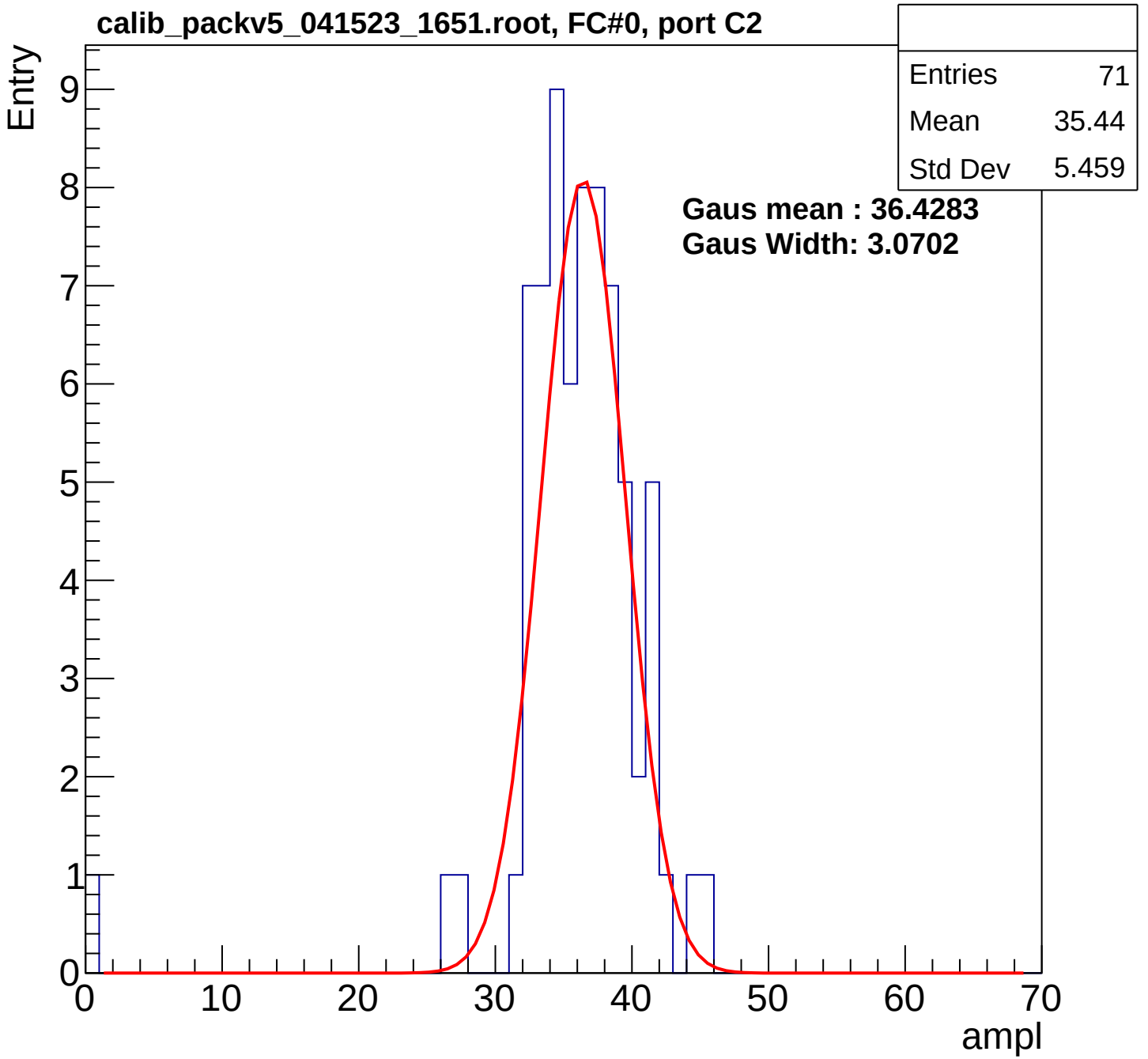

B1L103S, U17-ch95, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 53.87
Std Dev 7.495
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

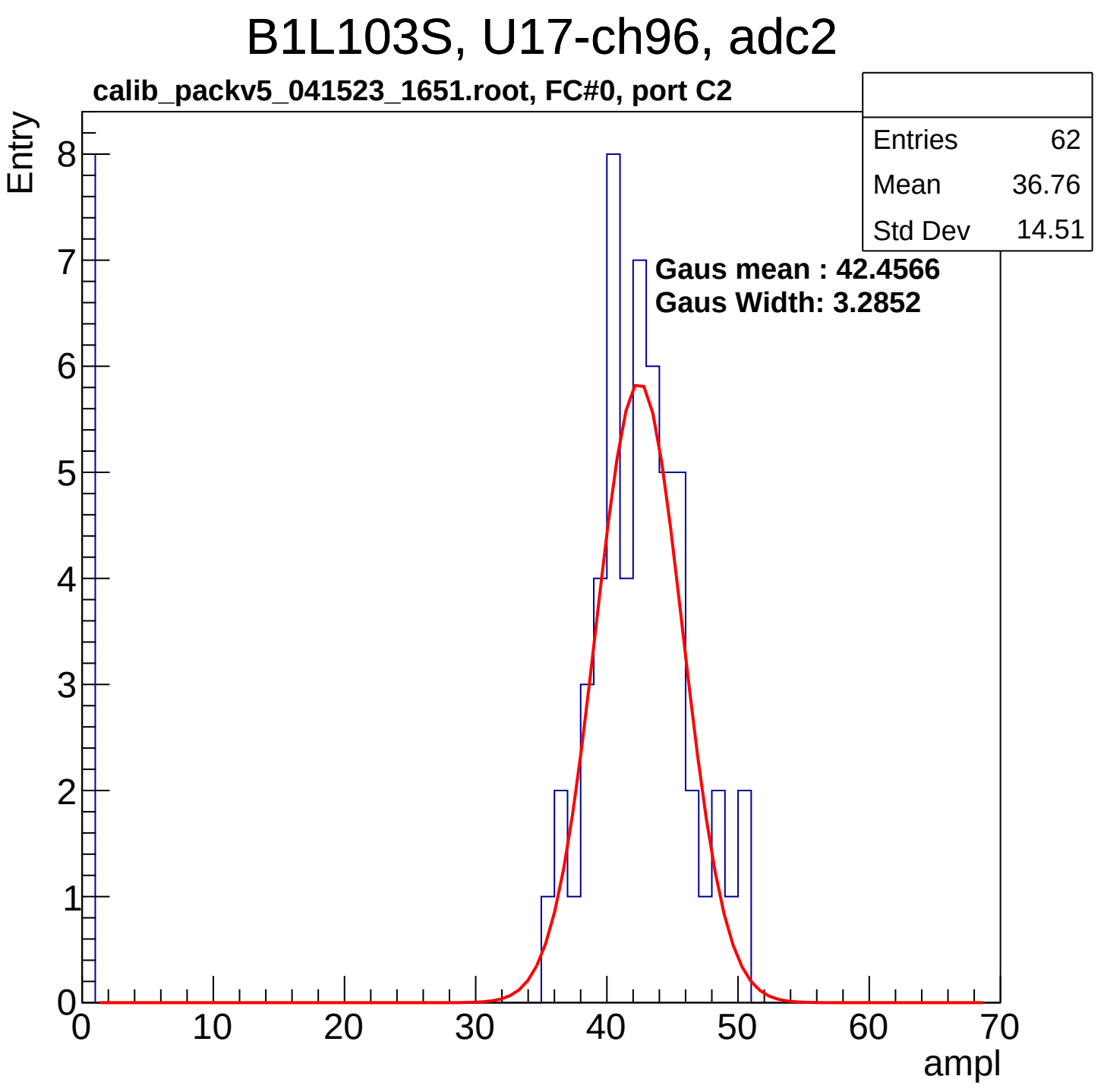

B1L103S, U17-ch95, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.37
Std Dev 8.806
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

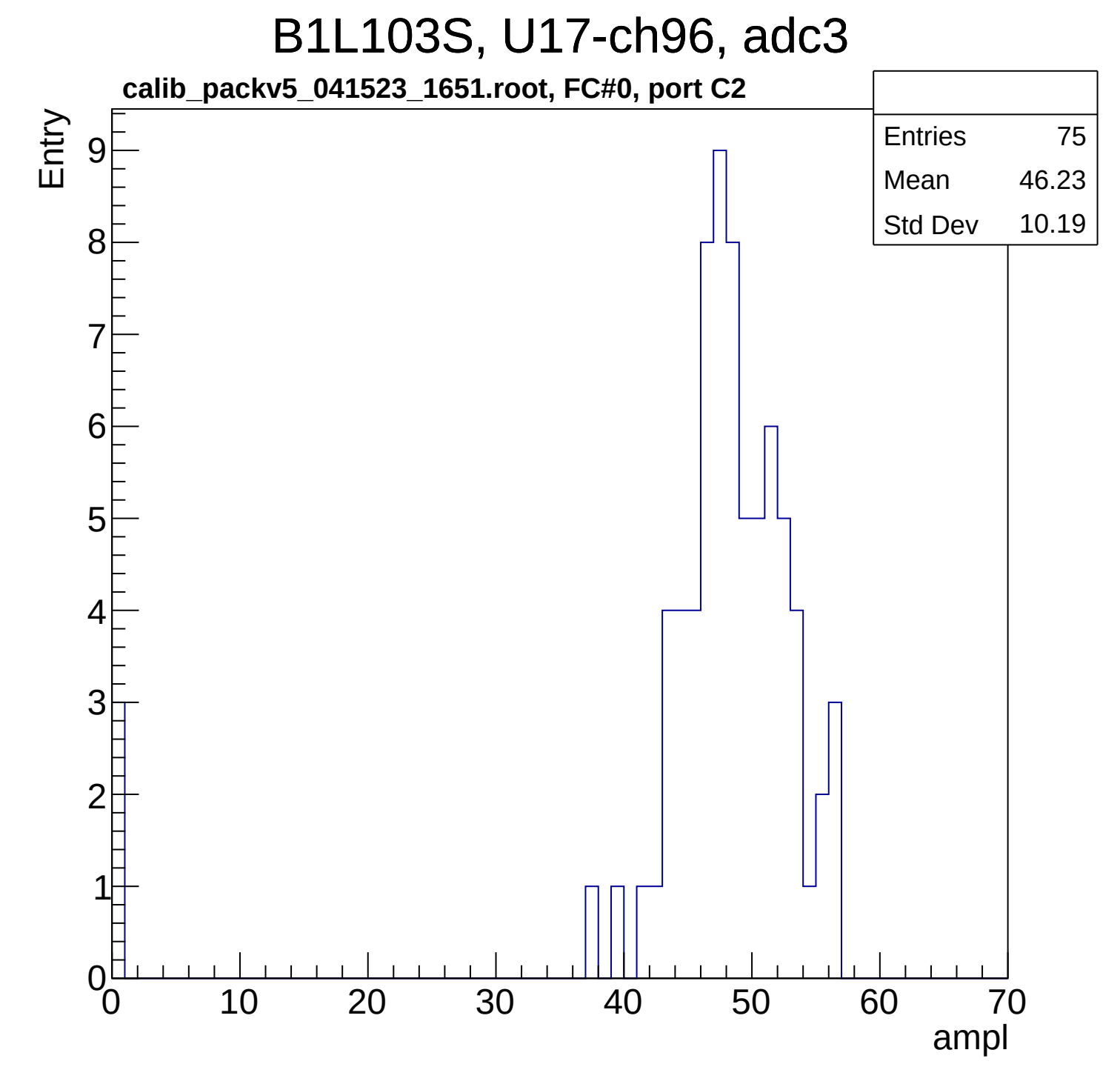

B1L103S, U17-ch95, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.17
Std Dev 1.213
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

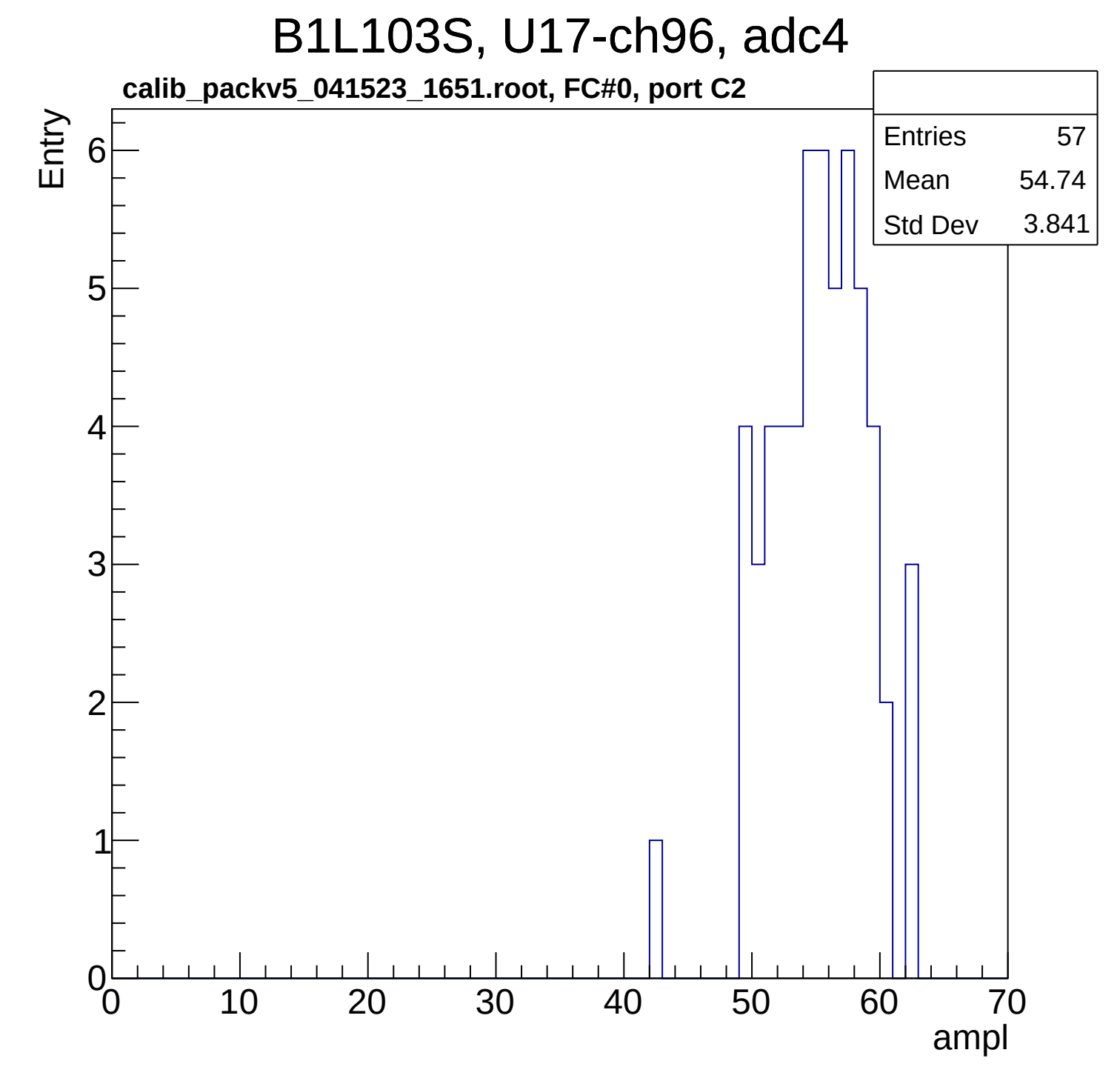

B1L103S, U17-ch95, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

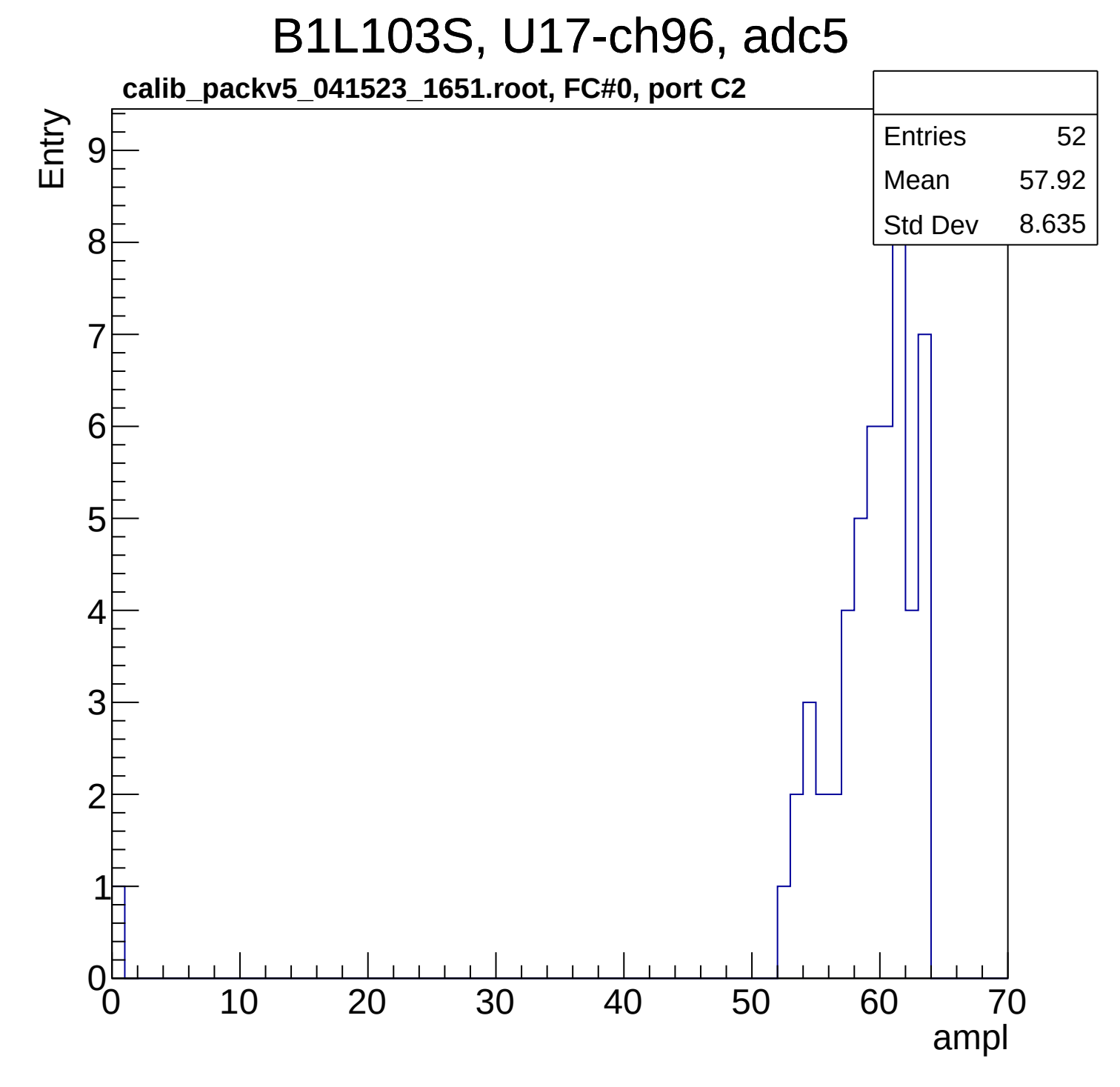

B1L103S, U17-ch96, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 24.05
Std Dev 10.86
Gaus mean : 29.0723
Gaus Width: 3.3338
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

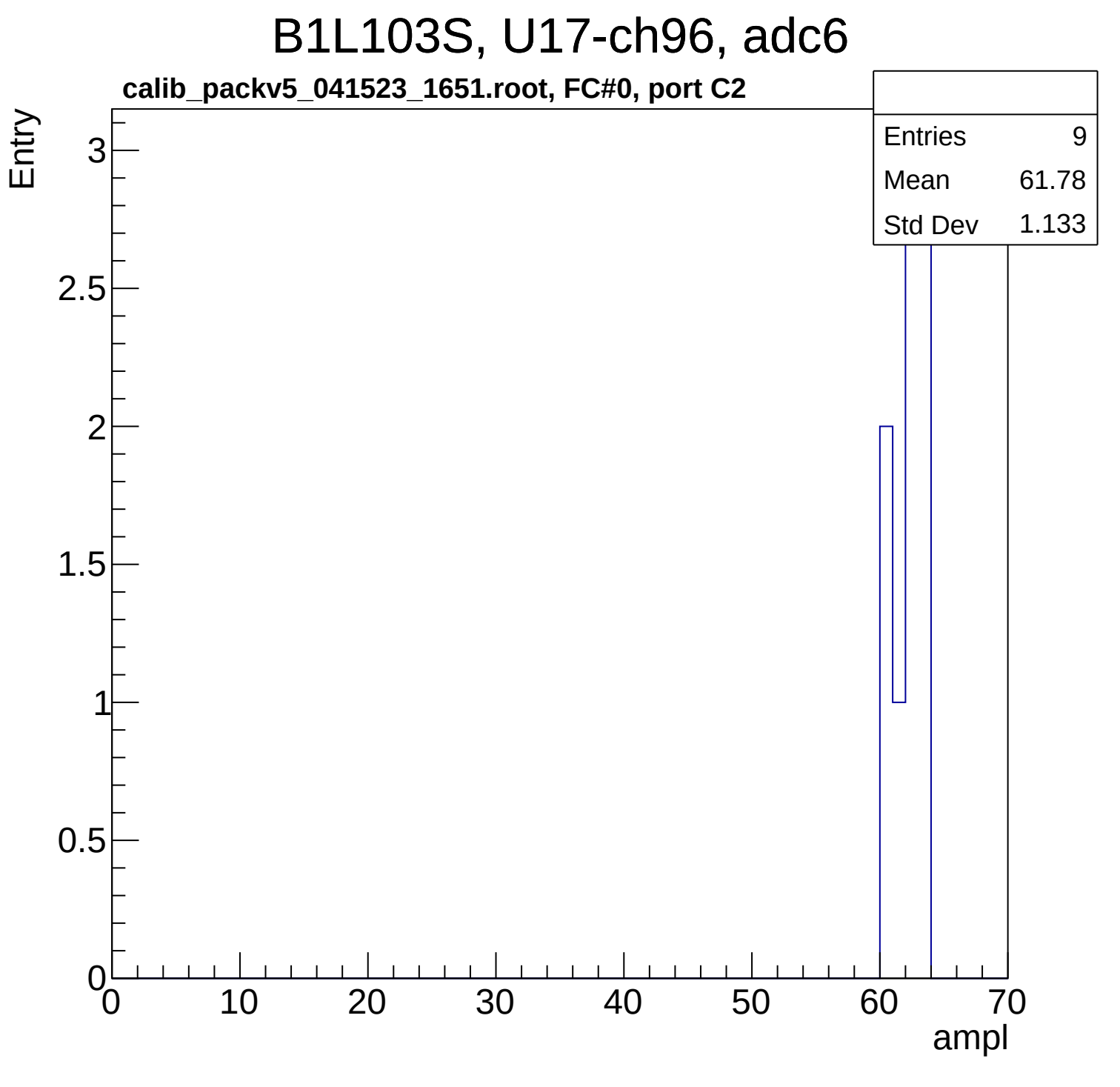

B1L103S, U17-ch96, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 35.44
Std Dev 5.459
Gaus mean : 36.4283
Gaus Width: 3.0702
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

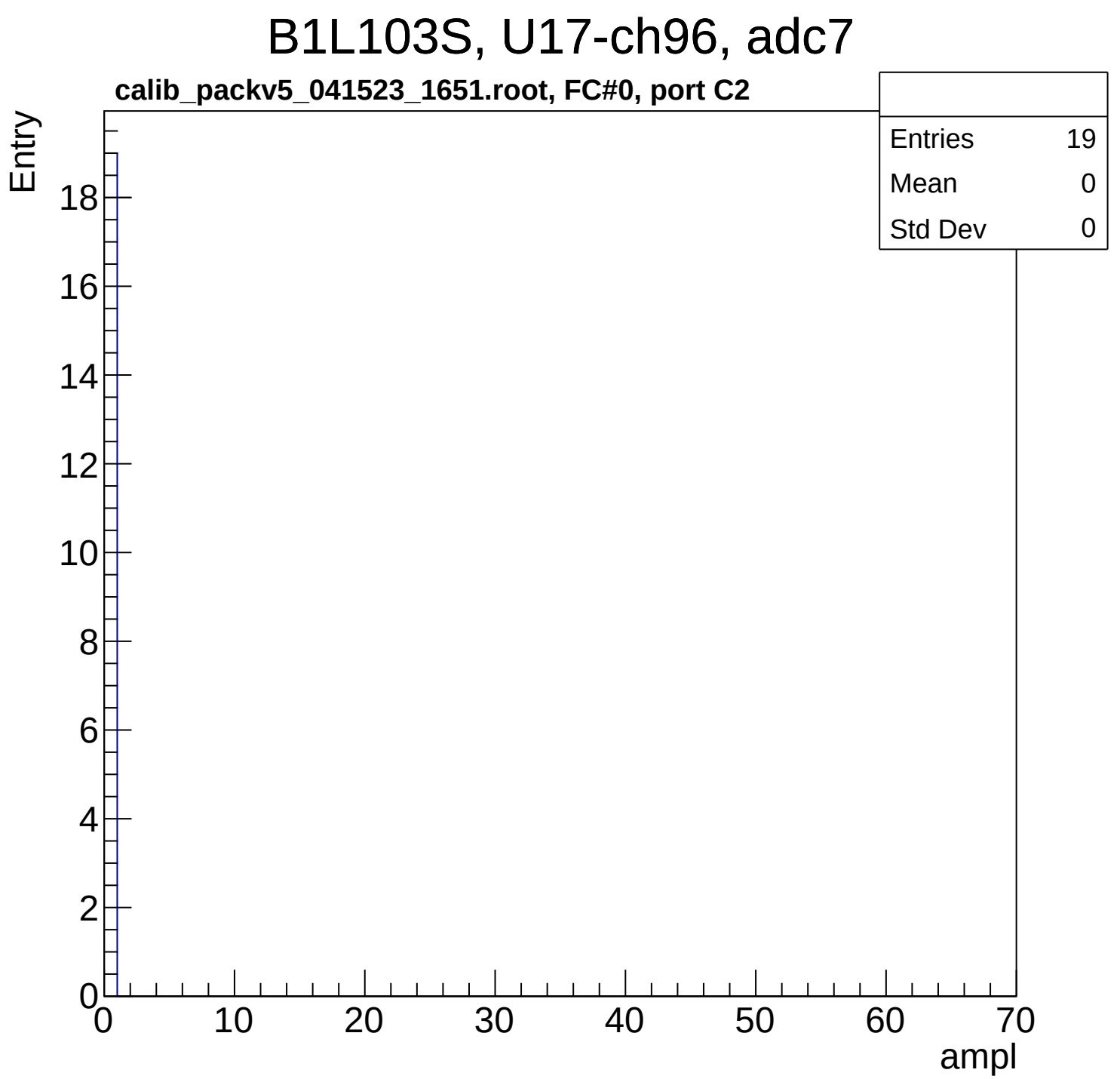

B1L103S, U17-ch96, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 36.76
Std Dev 14.51
Gaus mean : 42.4566
Gaus Width: 3.2852
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

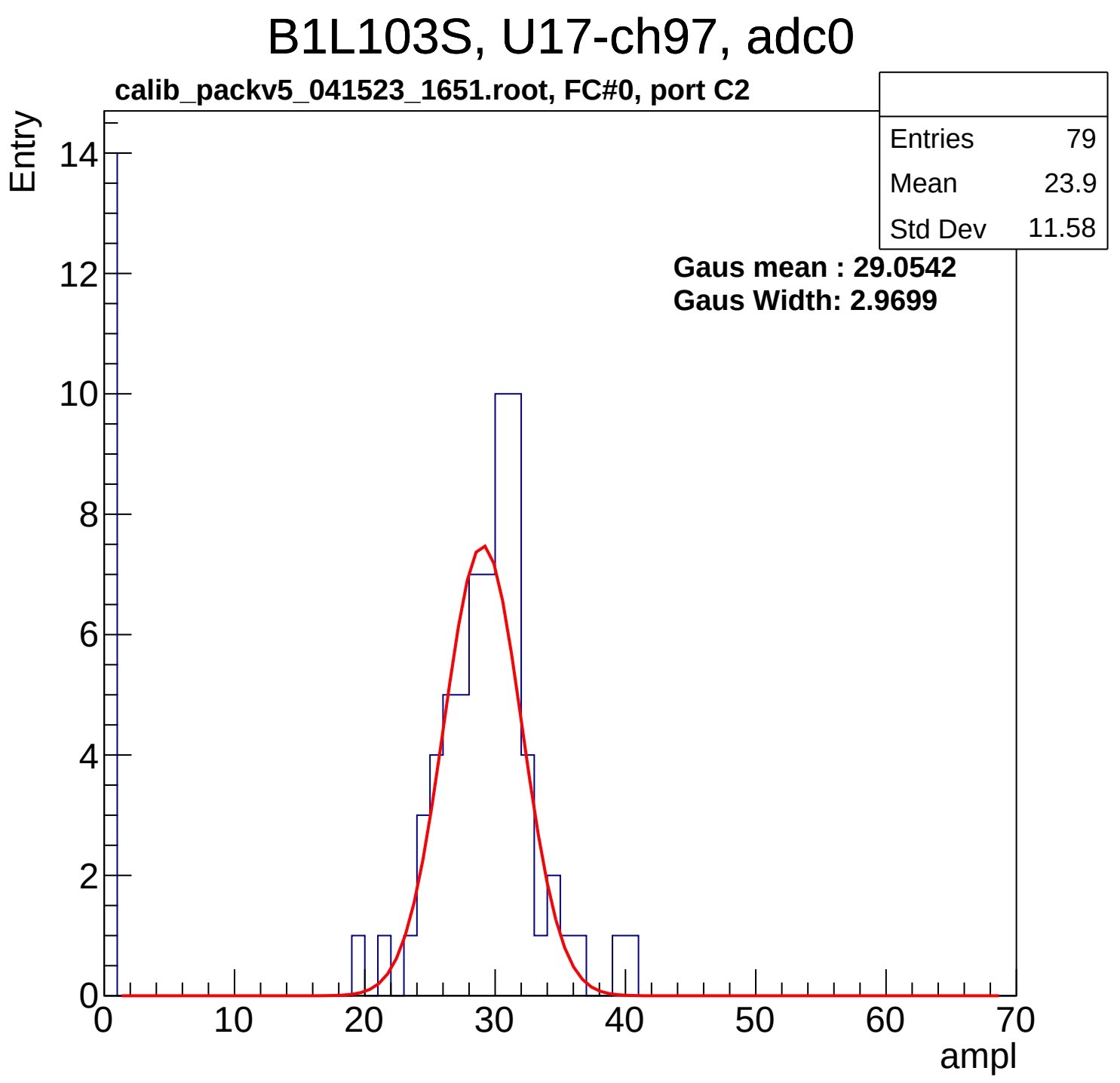

B1L103S, U17-ch96, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 46.23
Std Dev 10.19
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

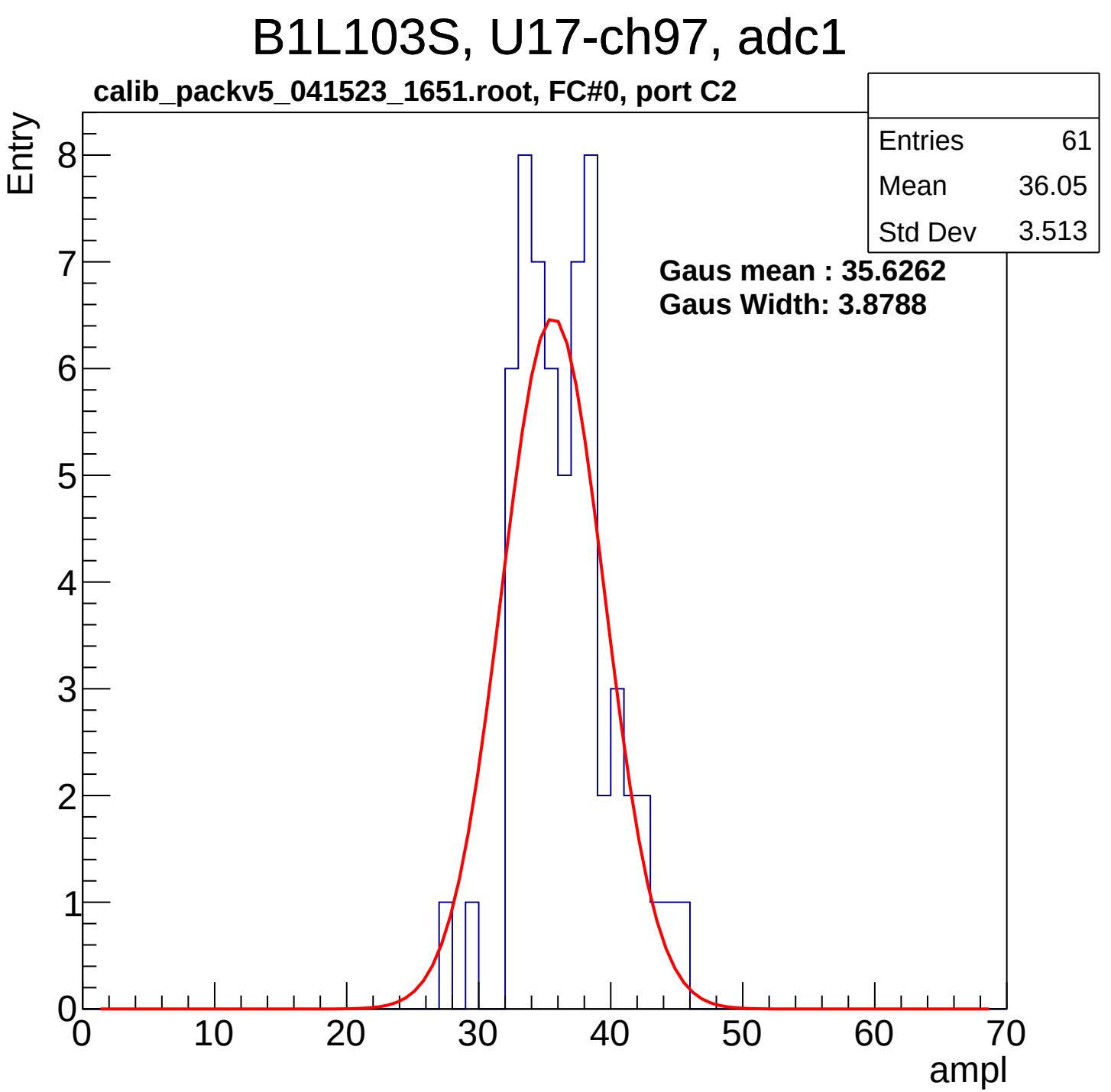

B1L103S, U17-ch96, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 54.74
Std Dev 3.841
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

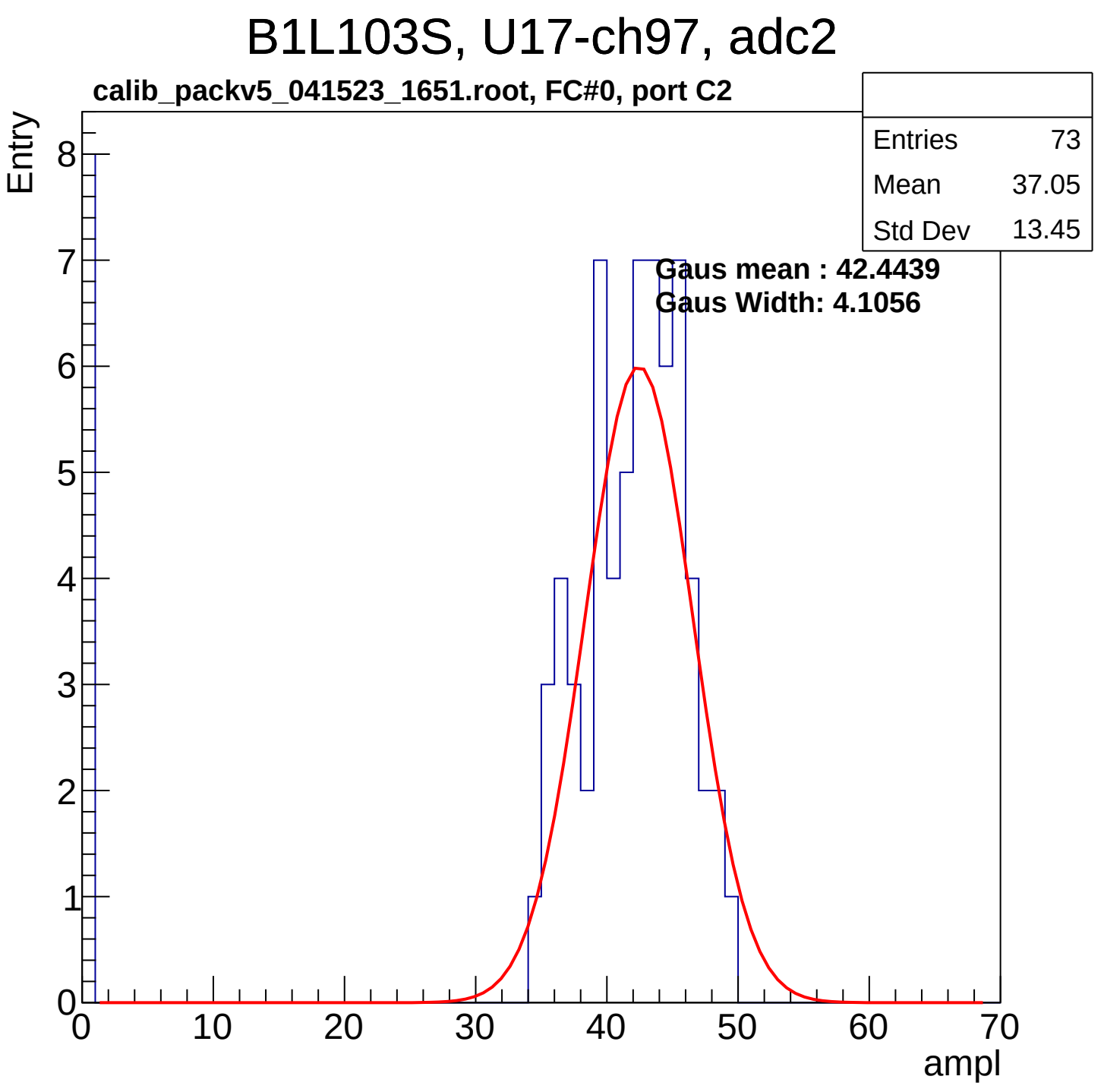

B1L103S, U17-ch96, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 57.92
Std Dev 8.635
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

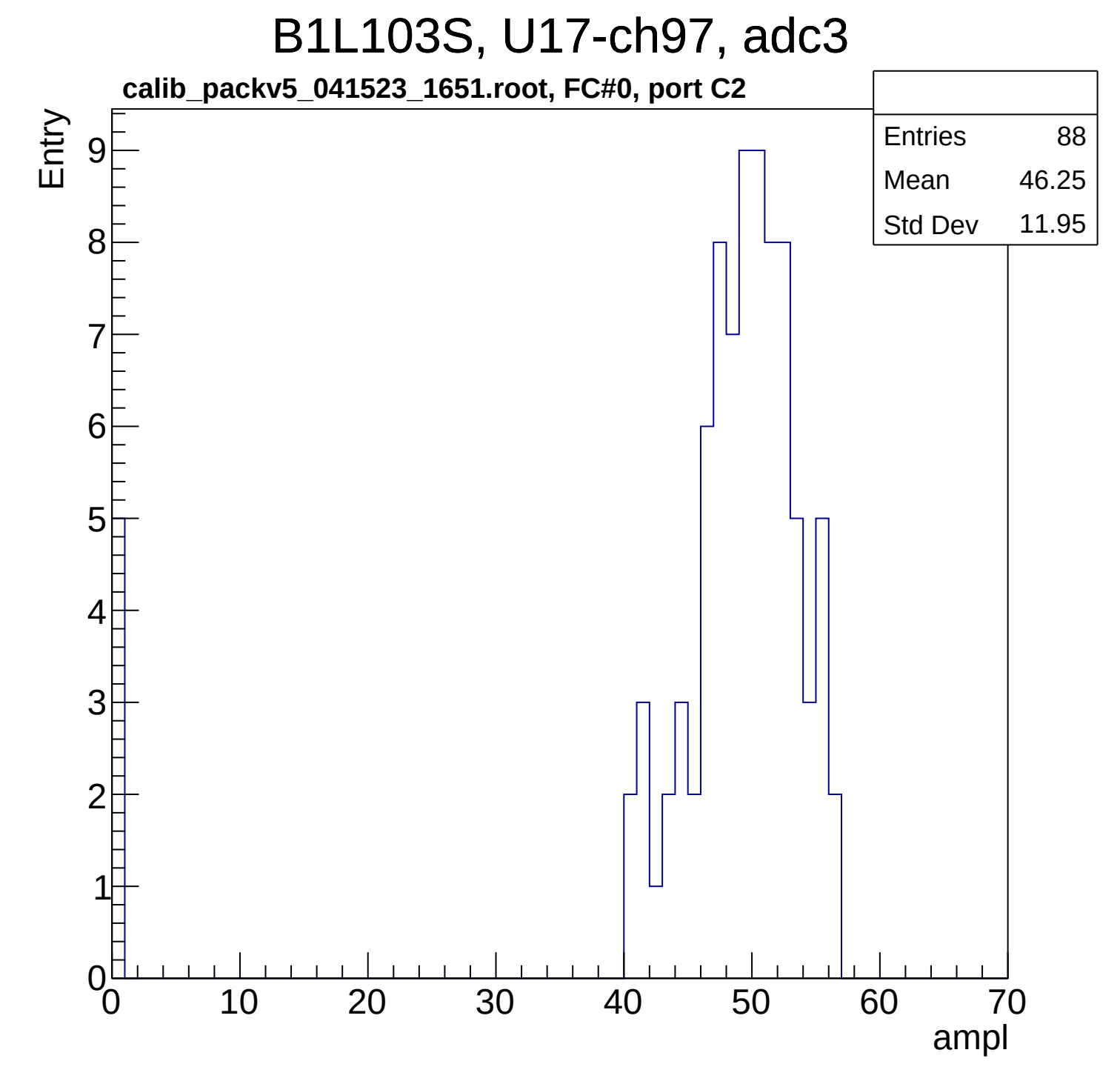

B1L103S, U17-ch96, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.78
Std Dev 1.133
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

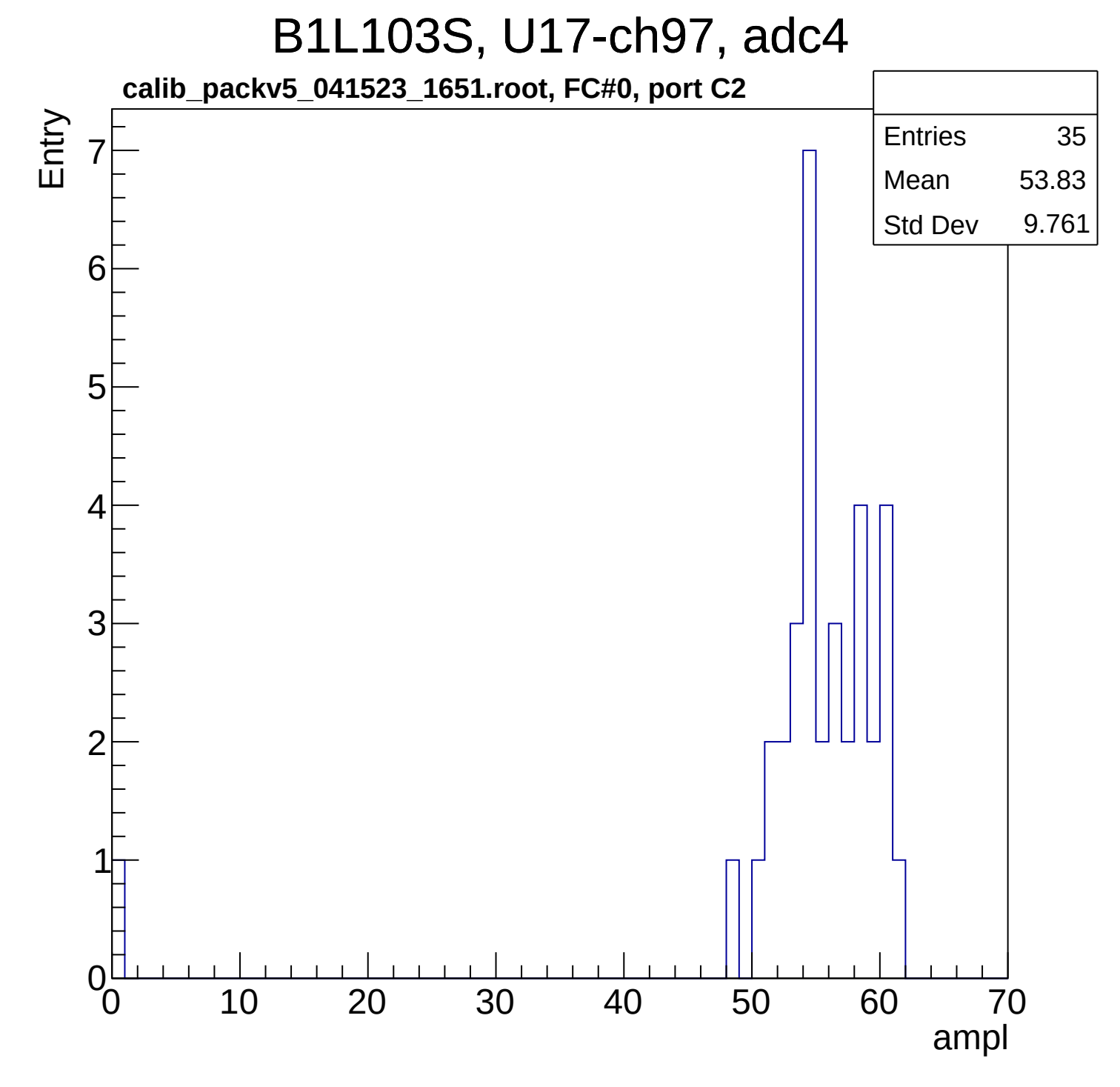

B1L103S, U17-ch96, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

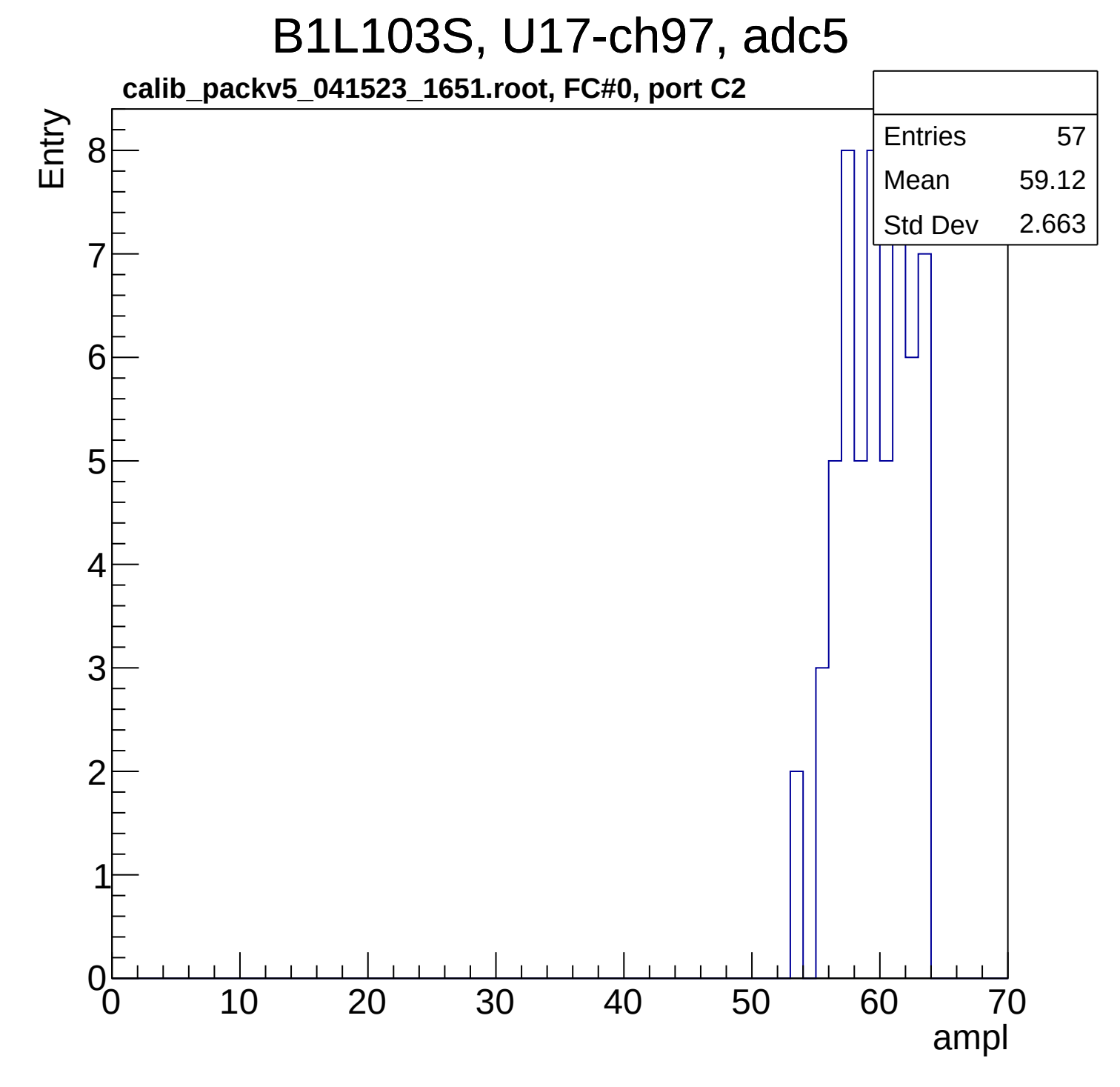

B1L103S, U17-ch97, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 23.9
Std Dev 11.58
Gaus mean : 29.0542
Gaus Width: 2.9699
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

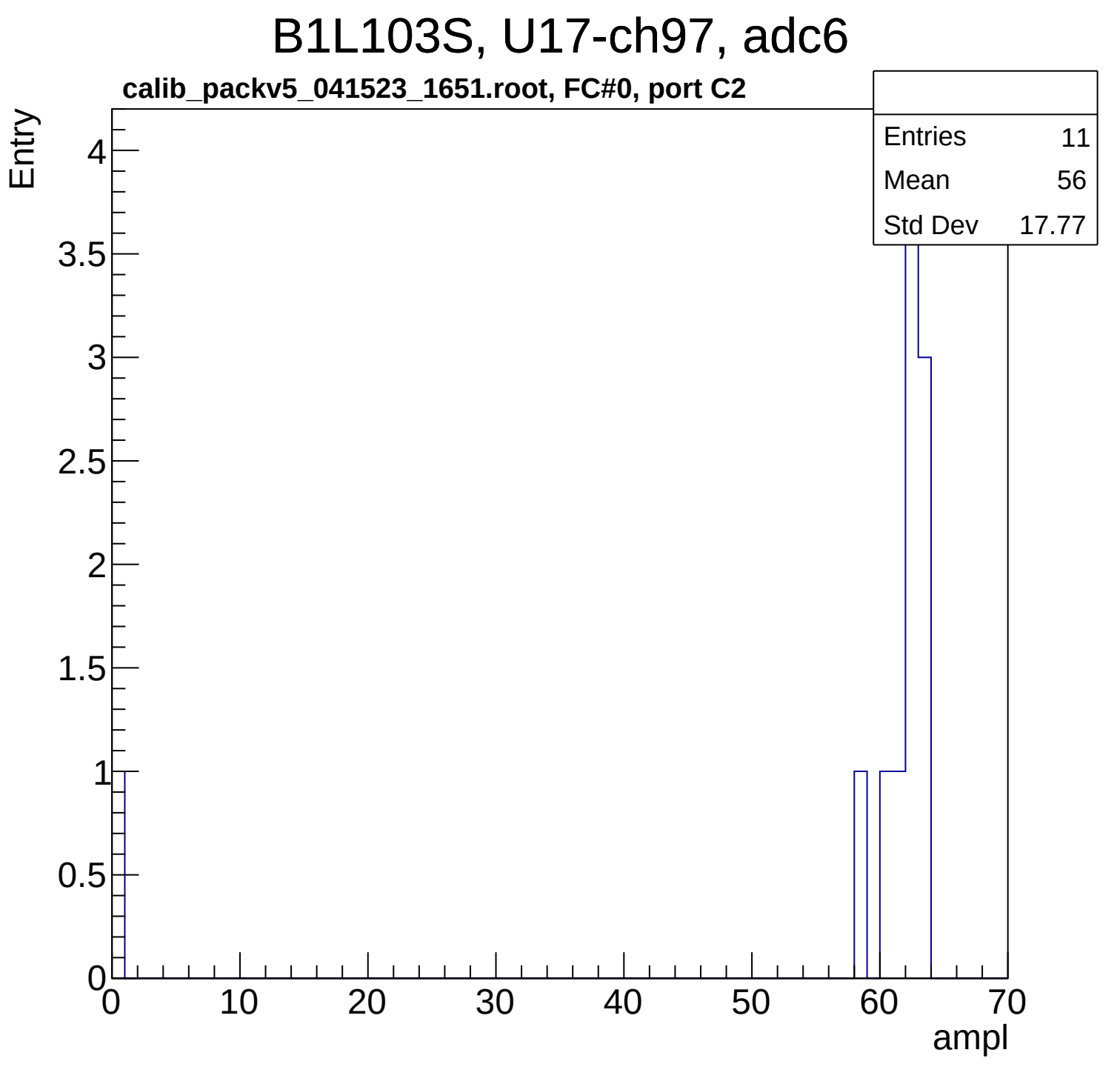

B1L103S, U17-ch97, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 36.05
Std Dev 3.513
Gaus mean : 35.6262
Gaus Width: 3.8788
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

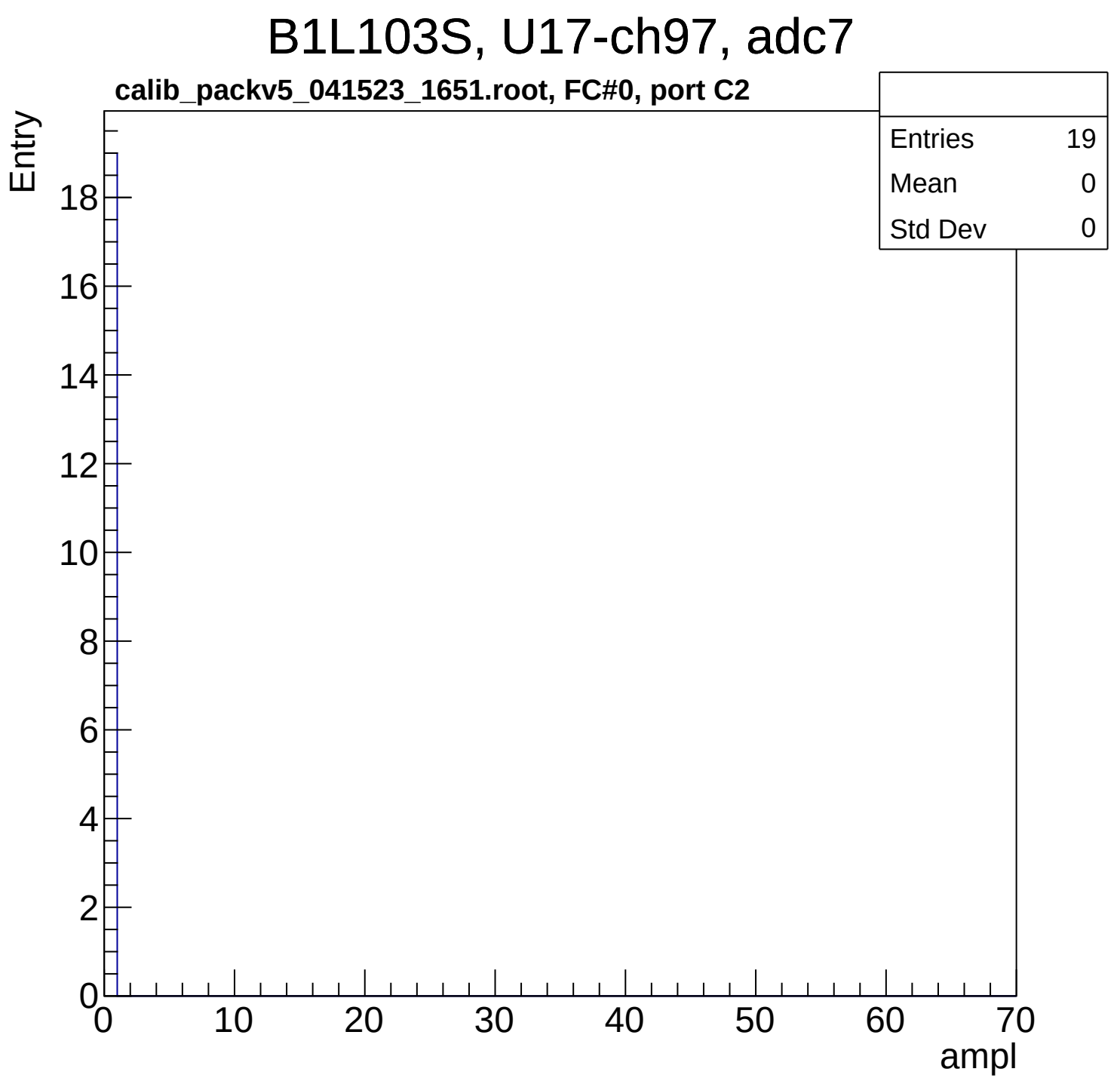

B1L103S, U17-ch97, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 37.05
Std Dev 13.45
Gaus mean : 42.4439
Gaus Width: 4.1056
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

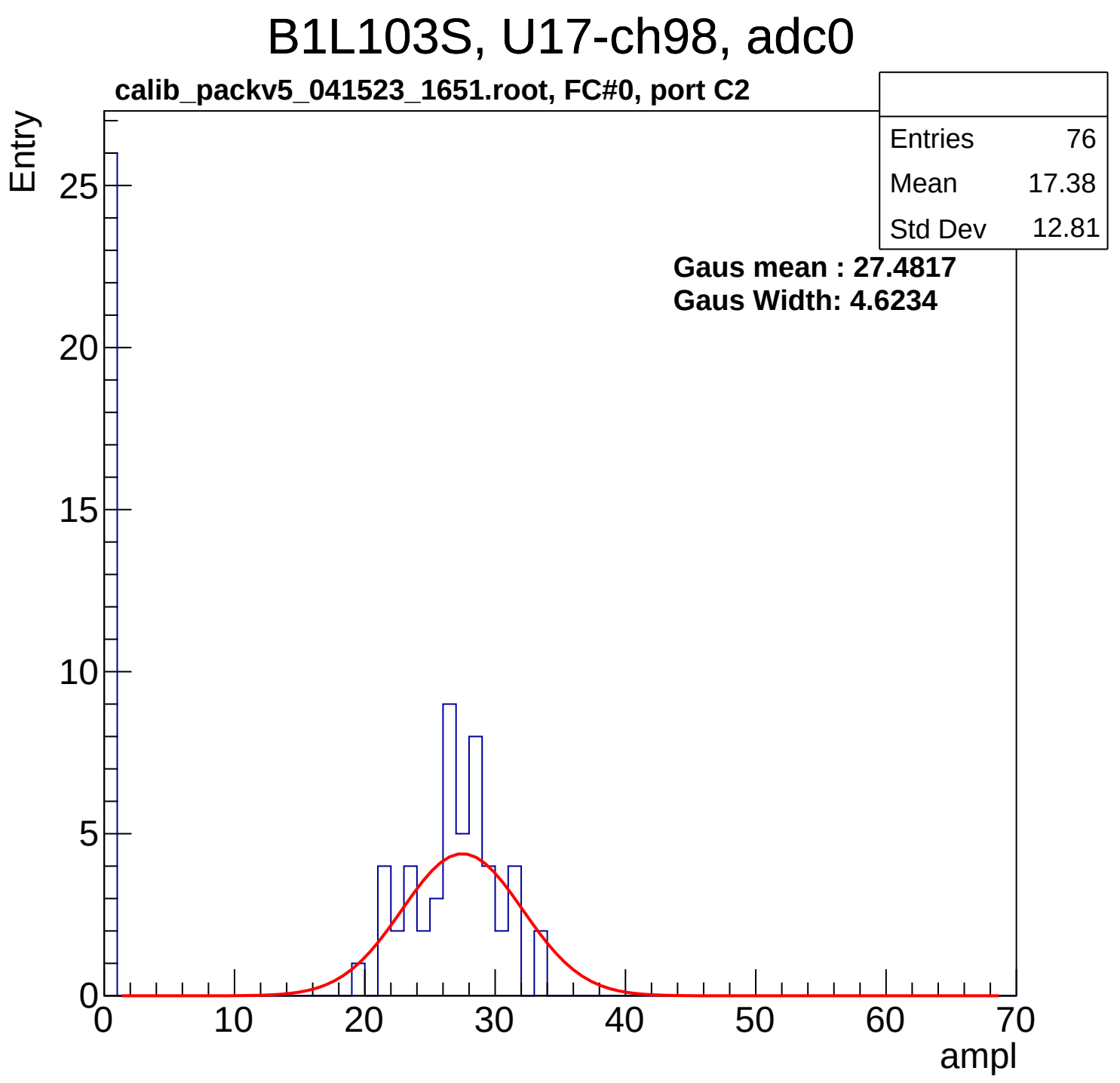

B1L103S, U17-ch97, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 46.25
Std Dev 11.95
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

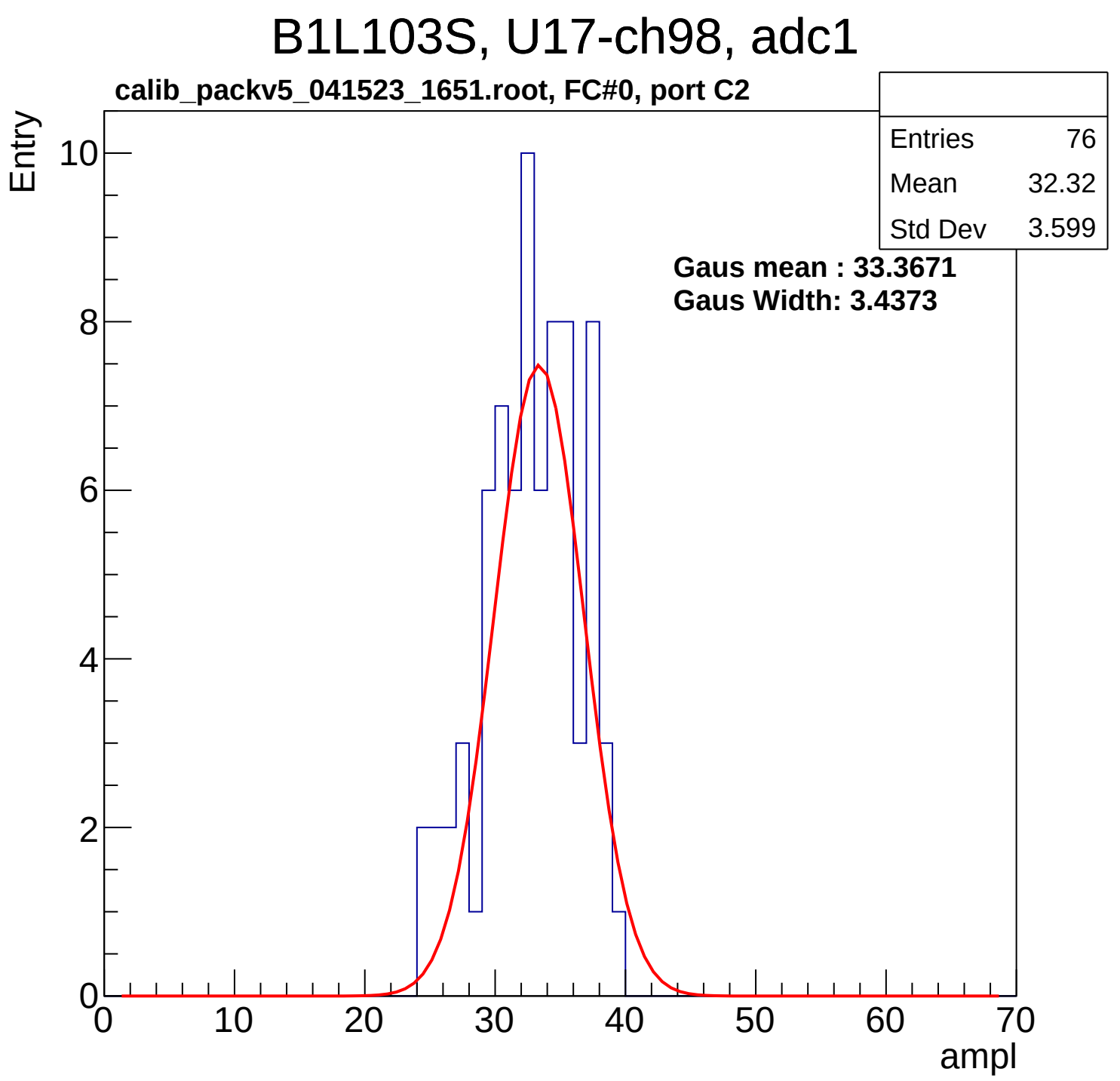

B1L103S, U17-ch97, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 53.83
Std Dev 9.761
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

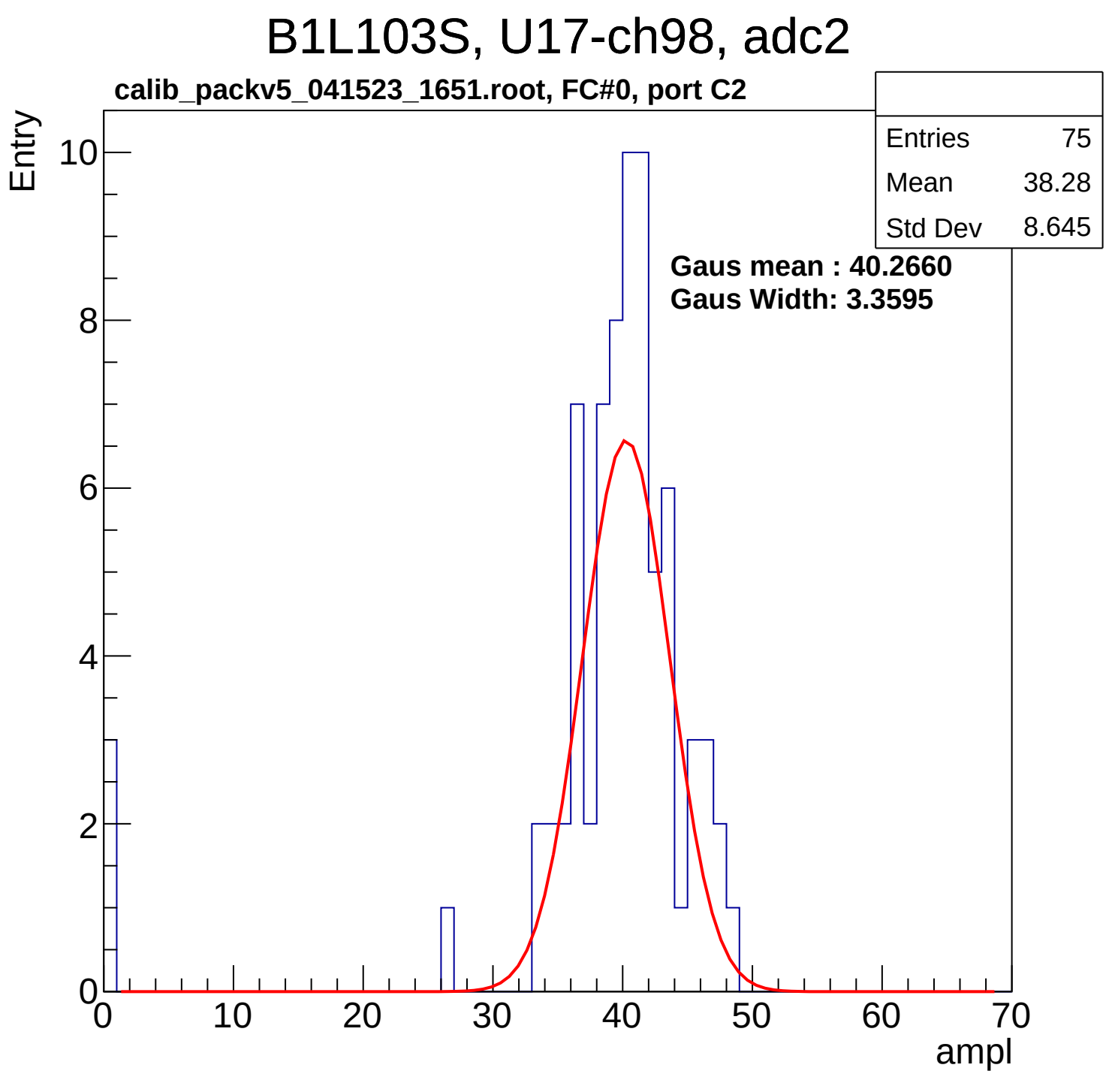

B1L103S, U17-ch97, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 59.12
Std Dev 2.663
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

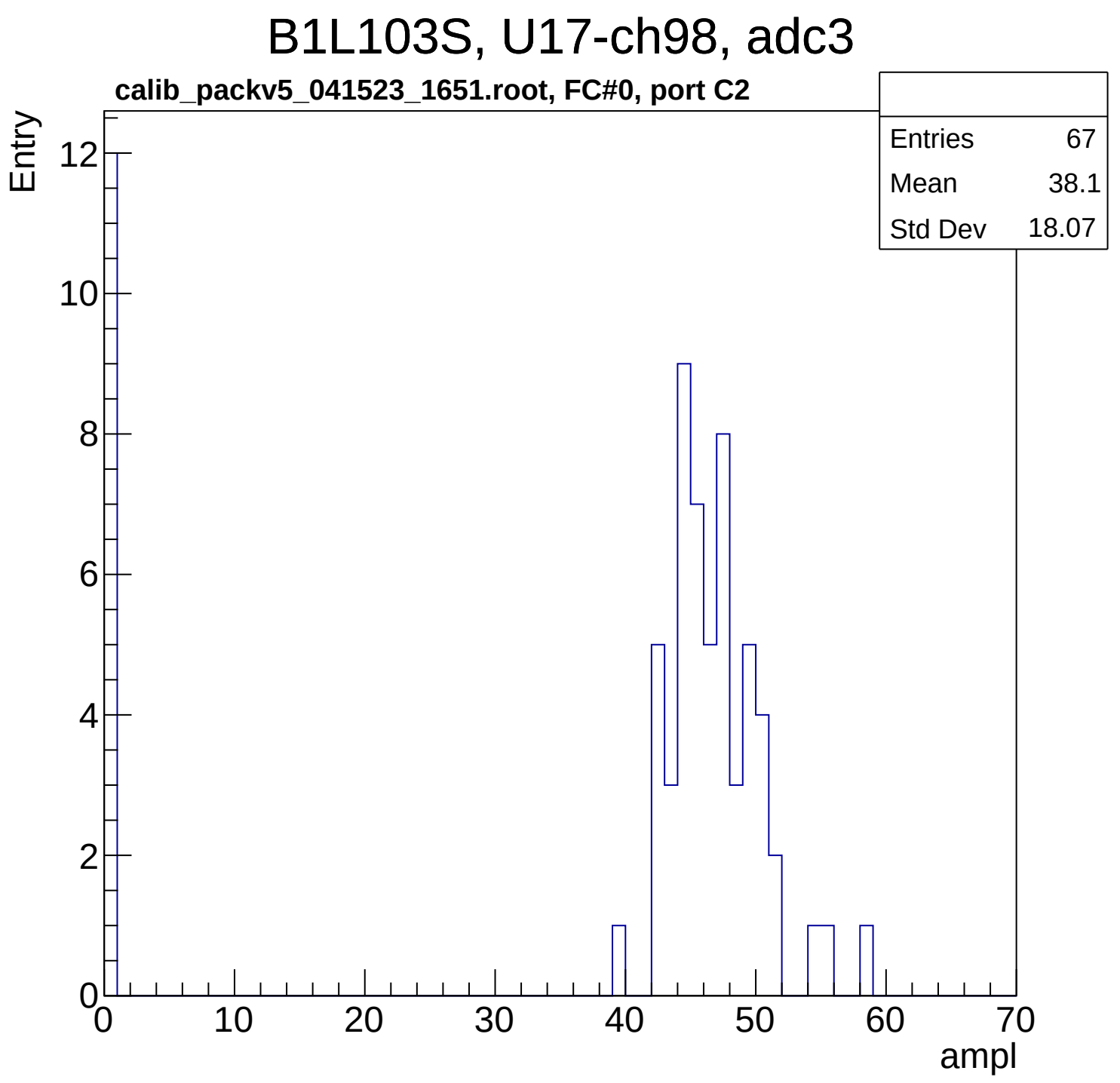

B1L103S, U17-ch97, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 56
Std Dev 17.77
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

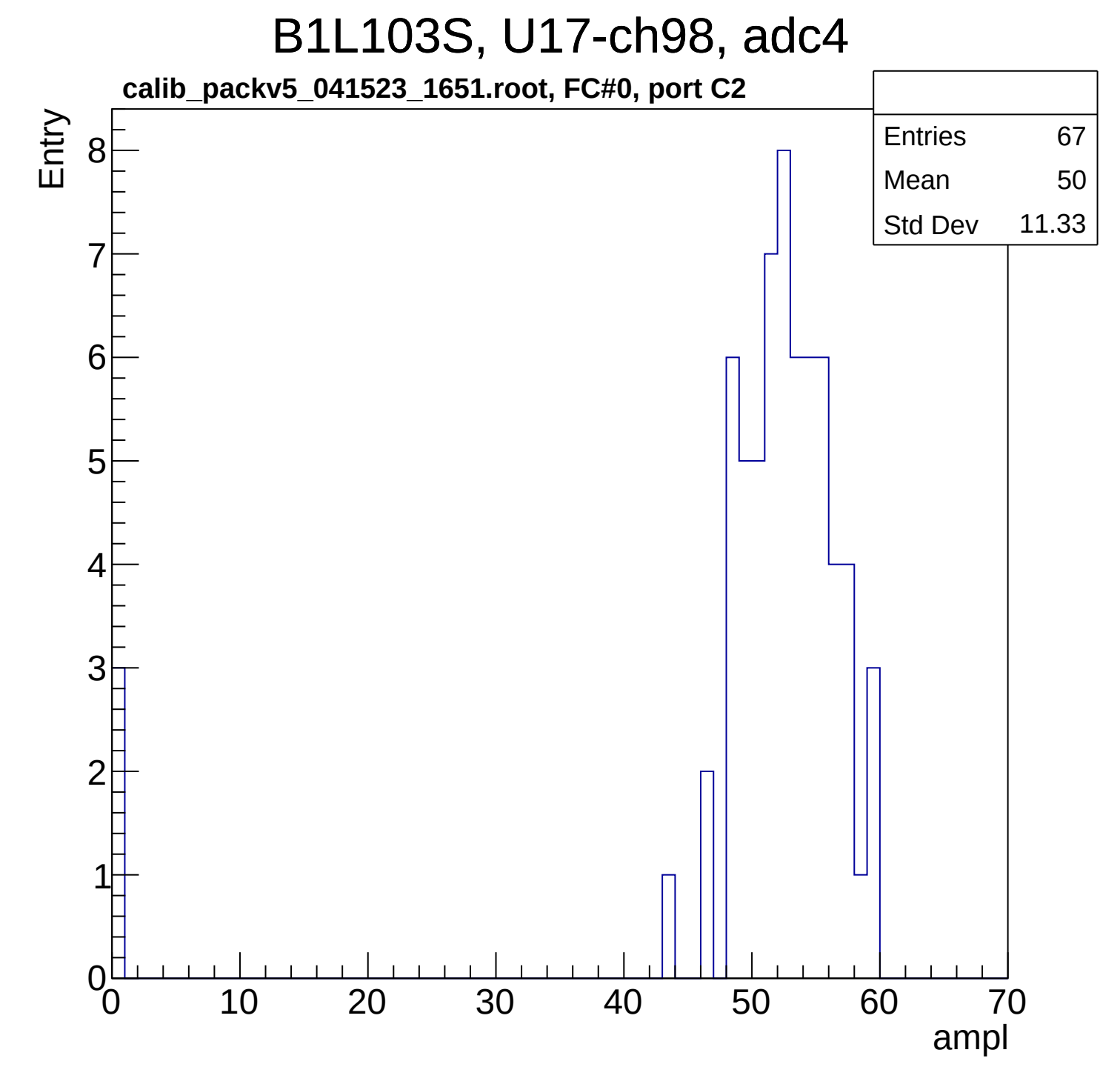

B1L103S, U17-ch97, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

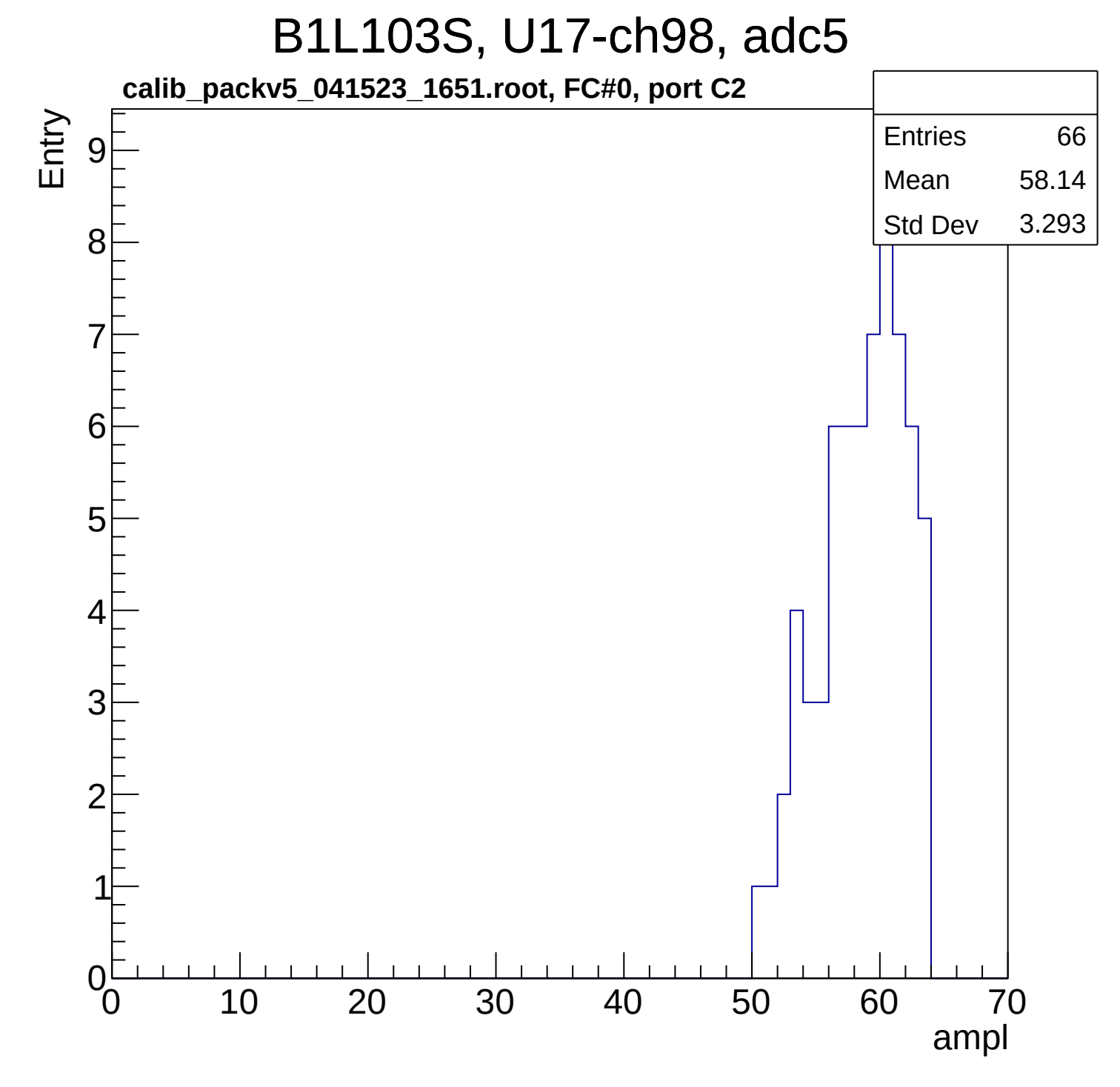

B1L103S, U17-ch98, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 17.38
Std Dev 12.81
Gaus mean : 27.4817
Gaus Width: 4.6234
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70

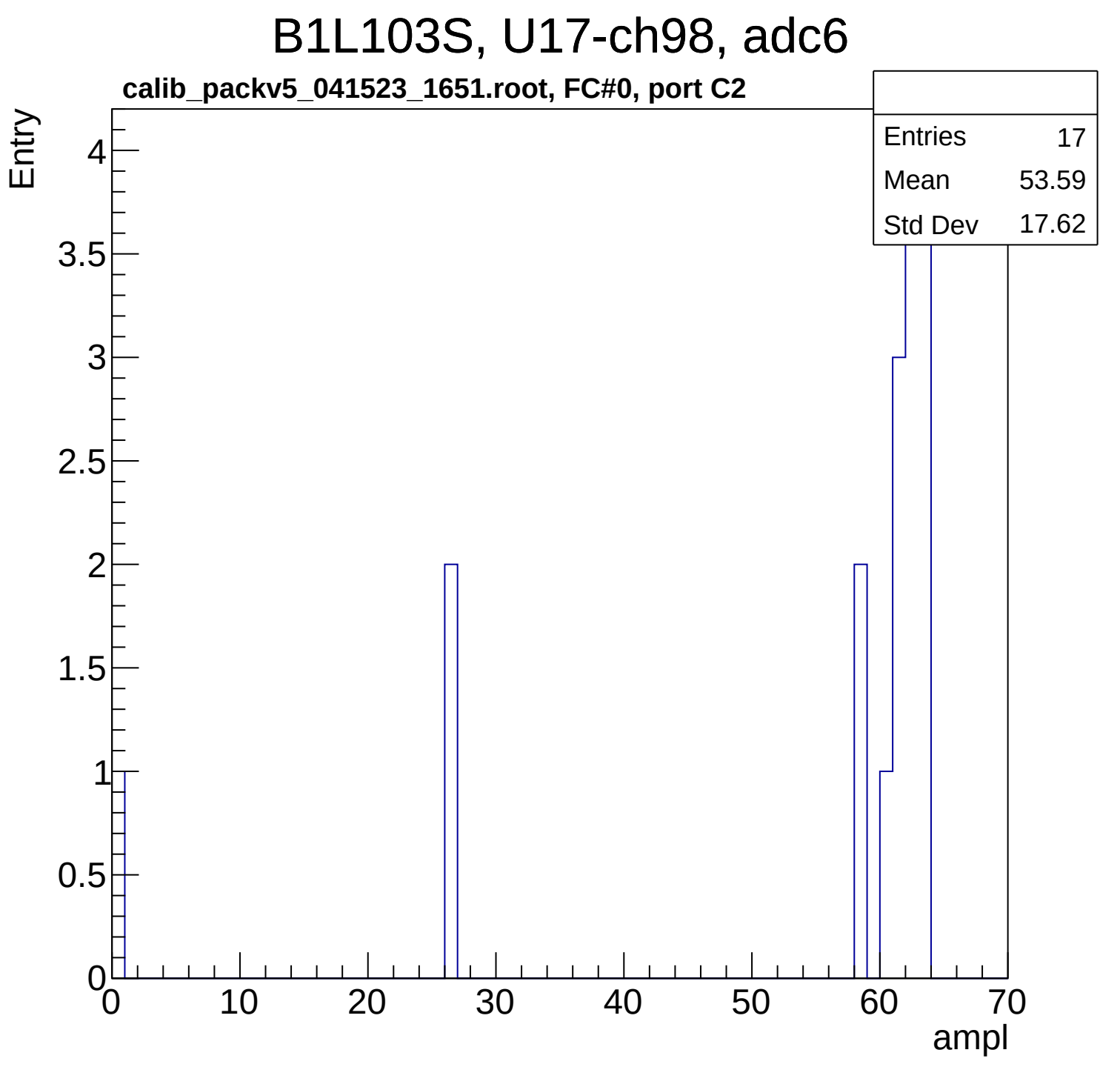

B1L103S, U17-ch98, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 32.32
Std Dev 3.599
Gaus mean : 33.3671
Gaus Width: 3.4373
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

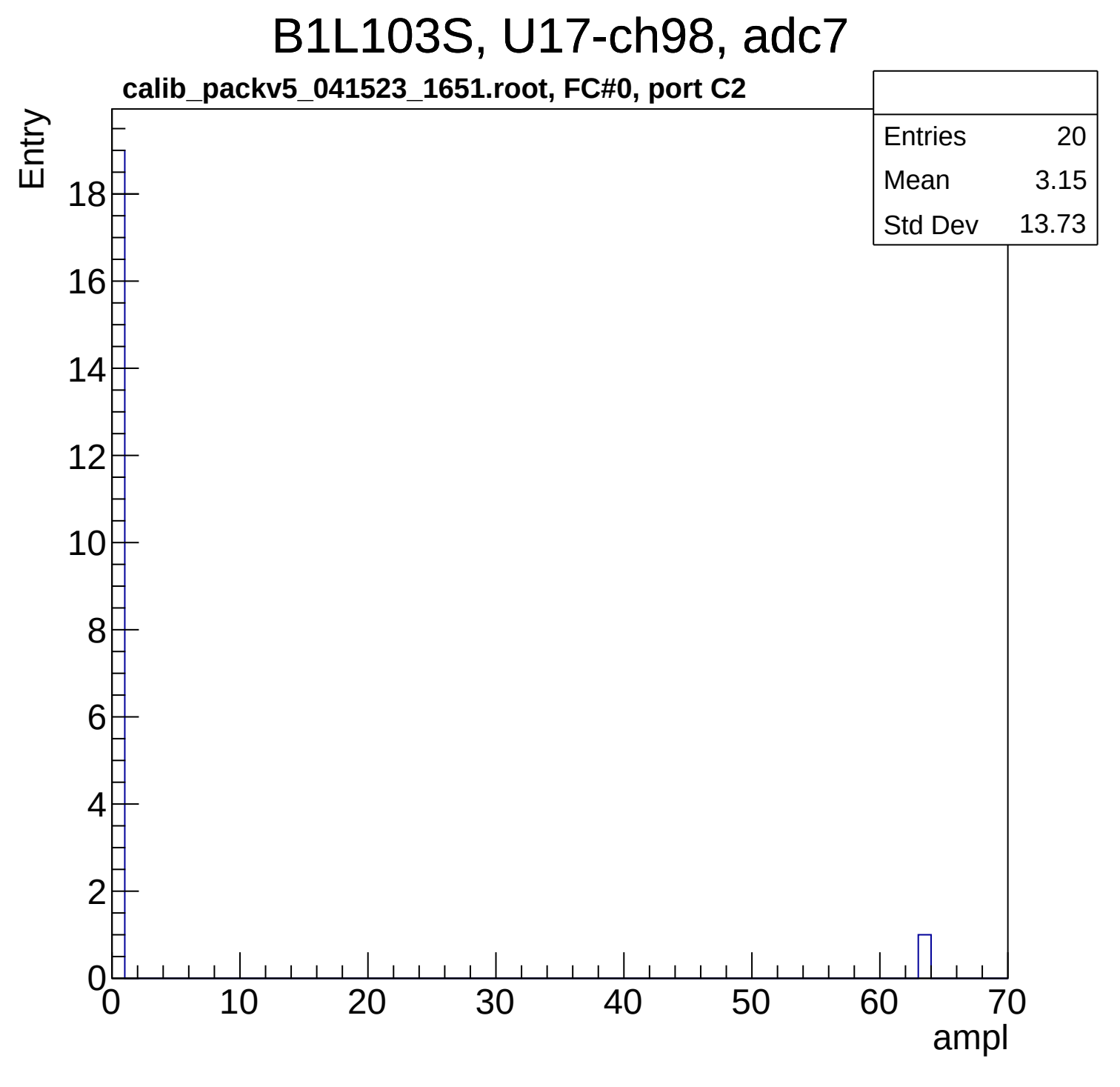

B1L103S, U17-ch98, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 38.28
Std Dev 8.645
Gaus mean : 40.2660
Gaus Width: 3.3595
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

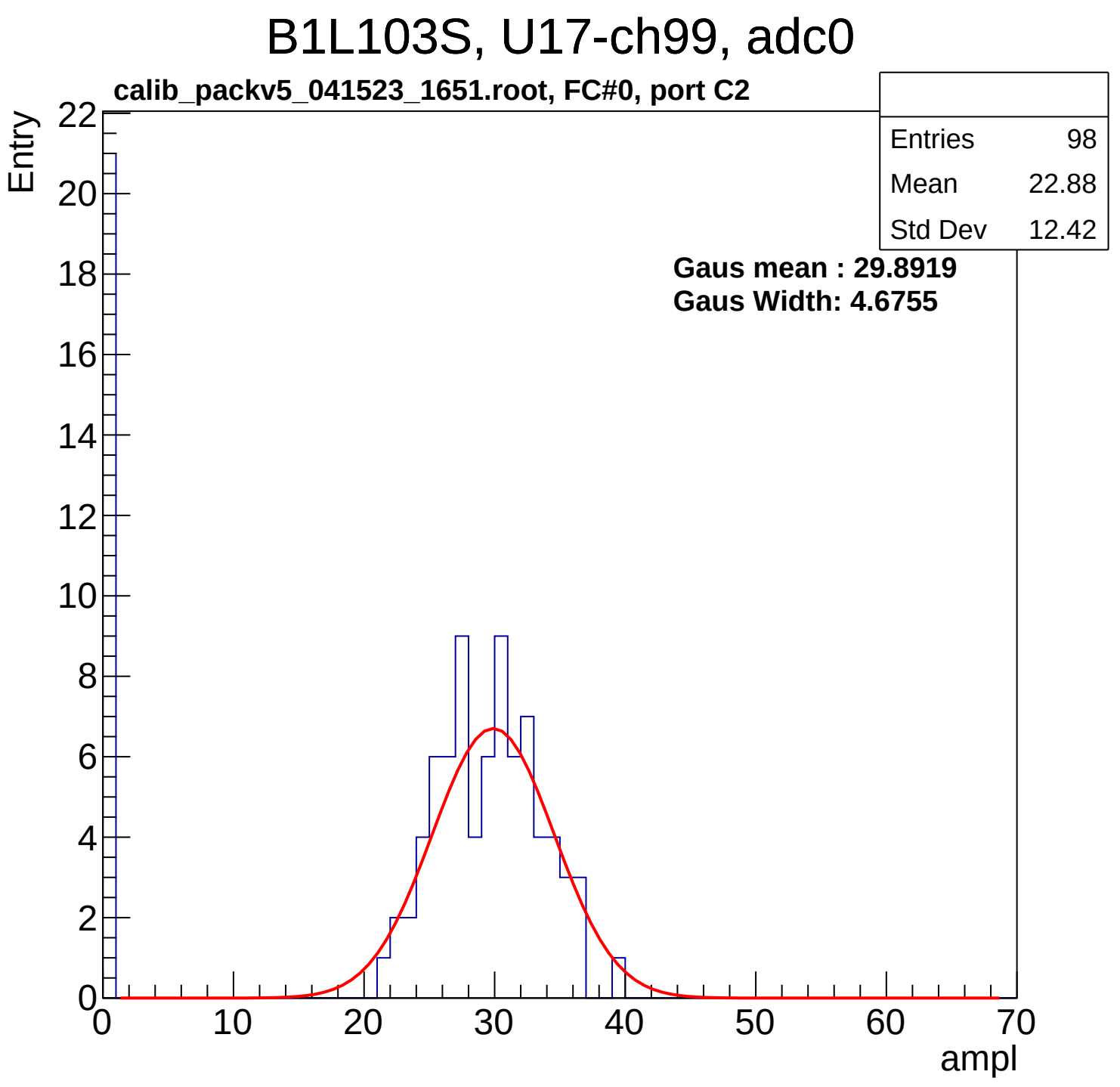

B1L103S, U17-ch98, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 38.1
Std Dev 18.07
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

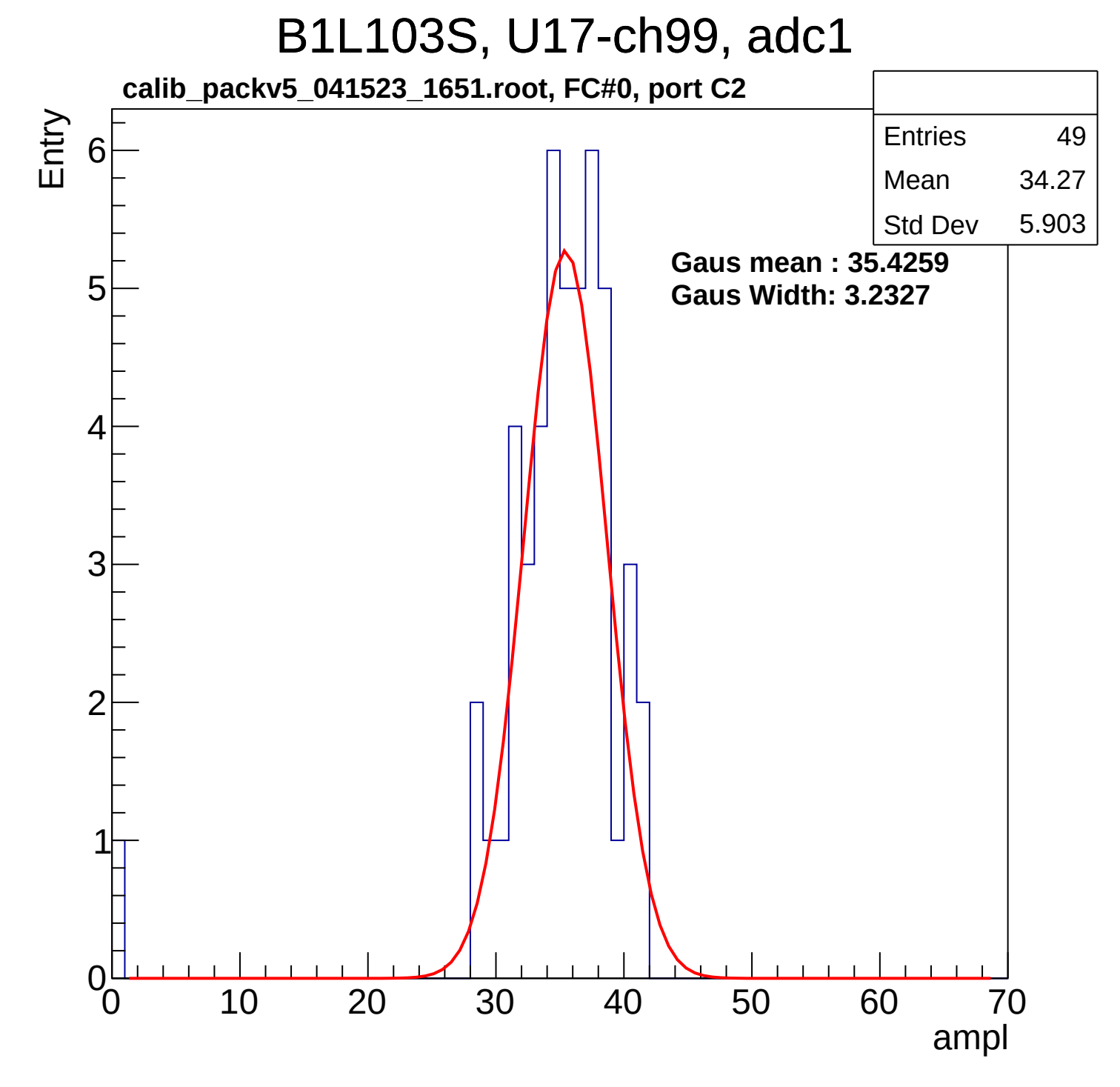

B1L103S, U17-ch98, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 50
Std Dev 11.33
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

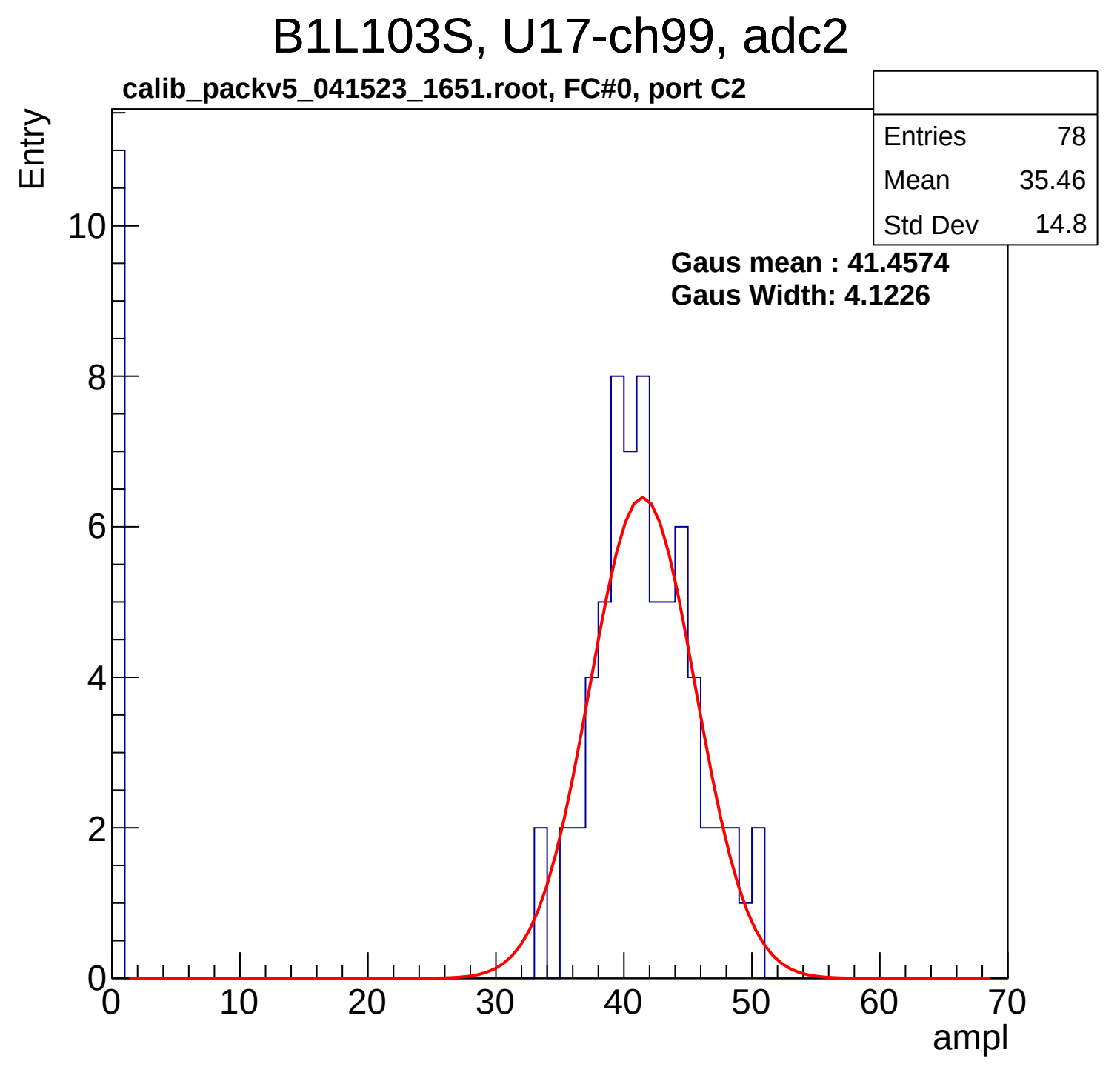

B1L103S, U17-ch98, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 58.14
Std Dev 3.293
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

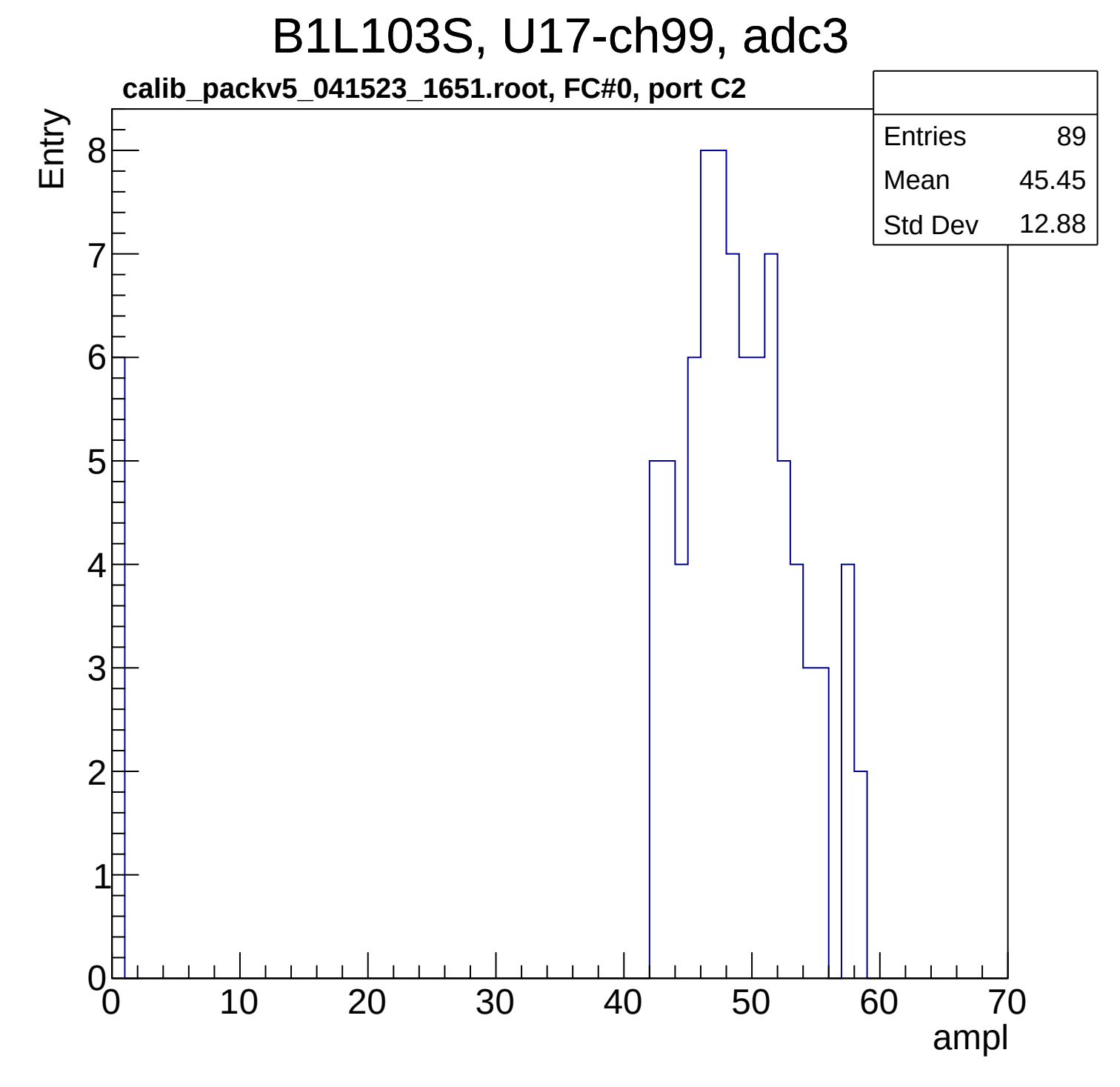

B1L103S, U17-ch98, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 53.59
Std Dev 17.62
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

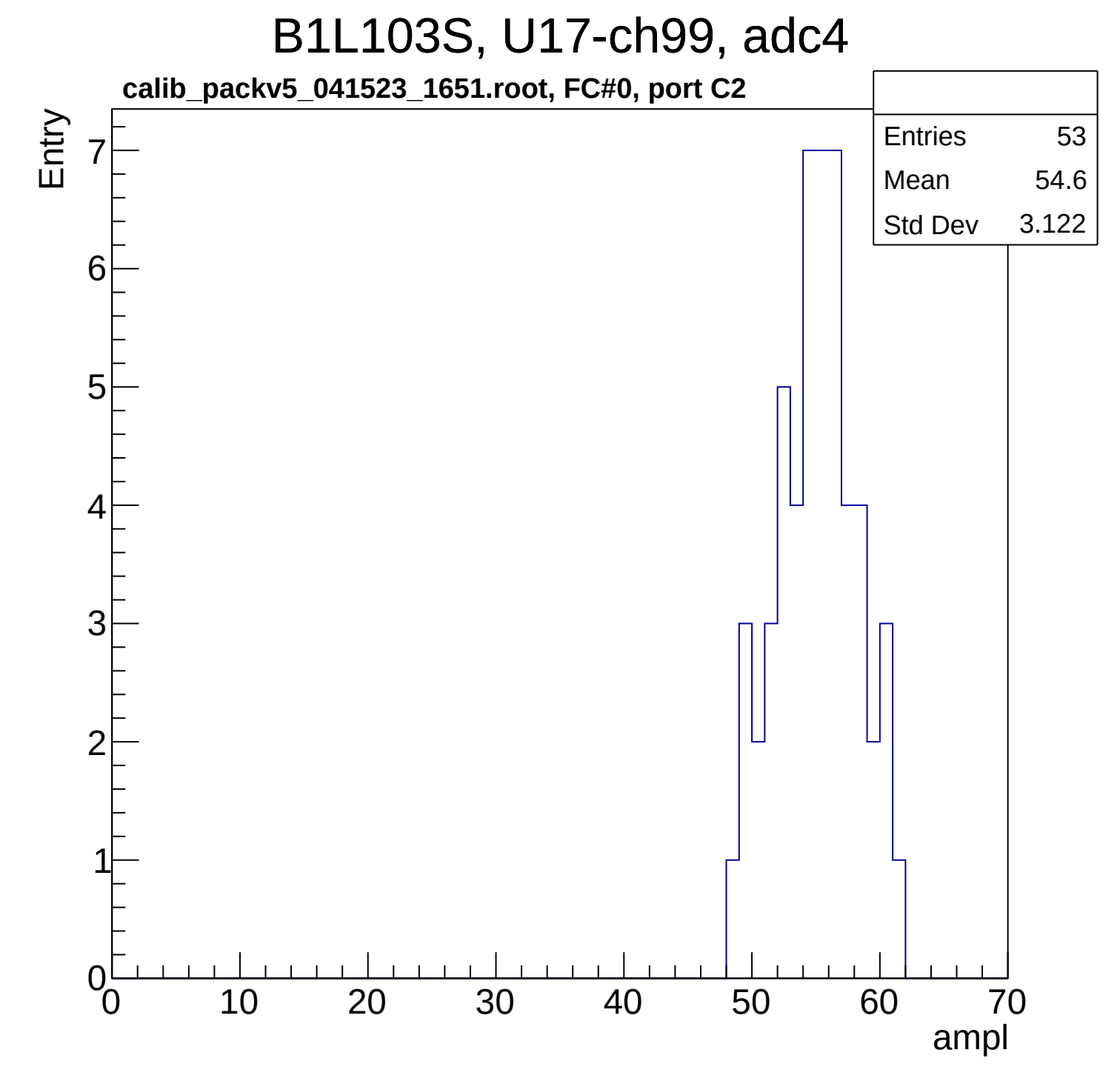

B1L103S, U17-ch98, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

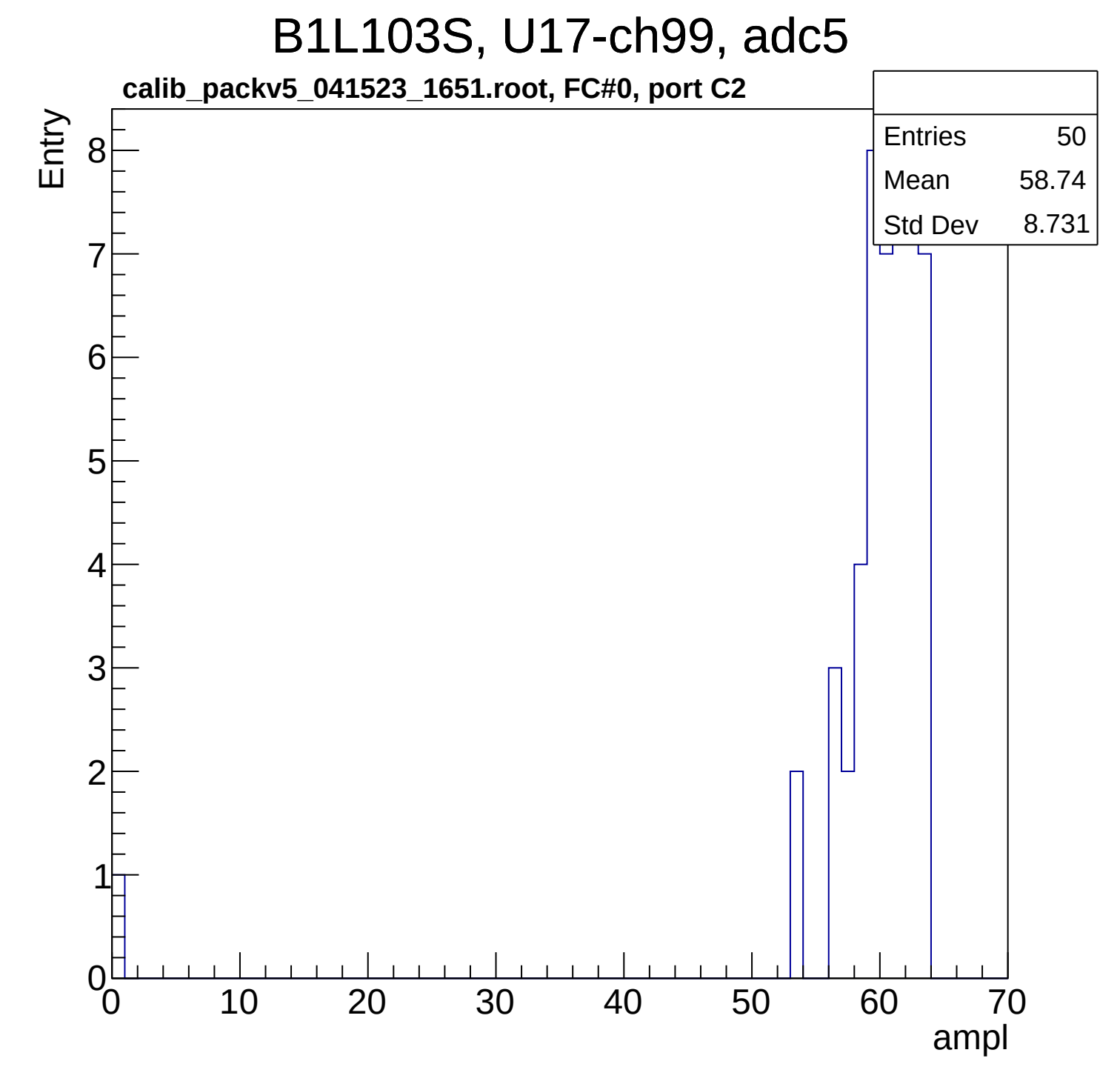

B1L103S, U17-ch99, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 22.88
Std Dev 12.42
Gaus mean : 29.8919
Gaus Width: 4.6755
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70

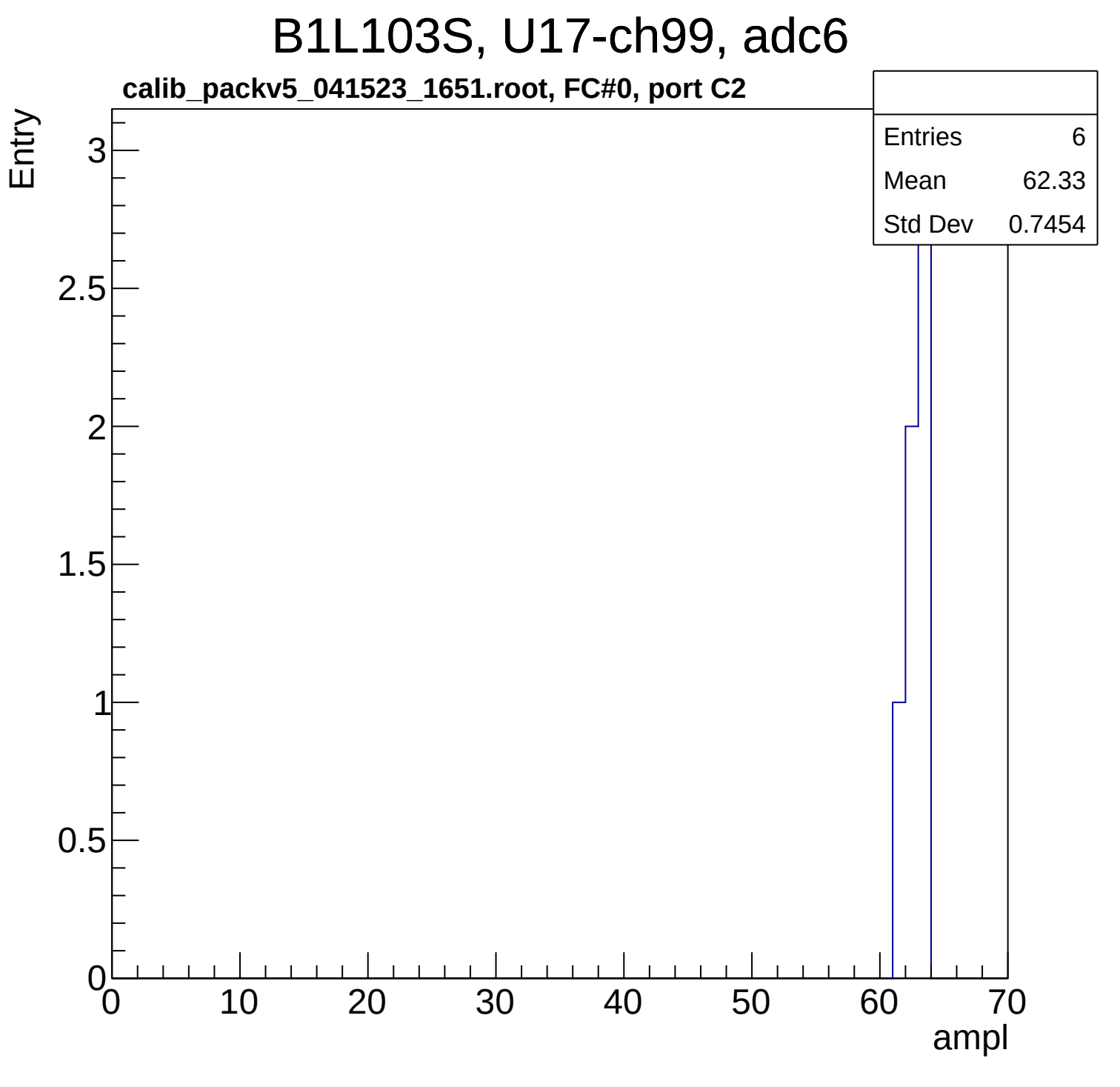

B1L103S, U17-ch99, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 34.27
Std Dev 5.903
Gaus mean : 35.4259
Gaus Width: 3.2327
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

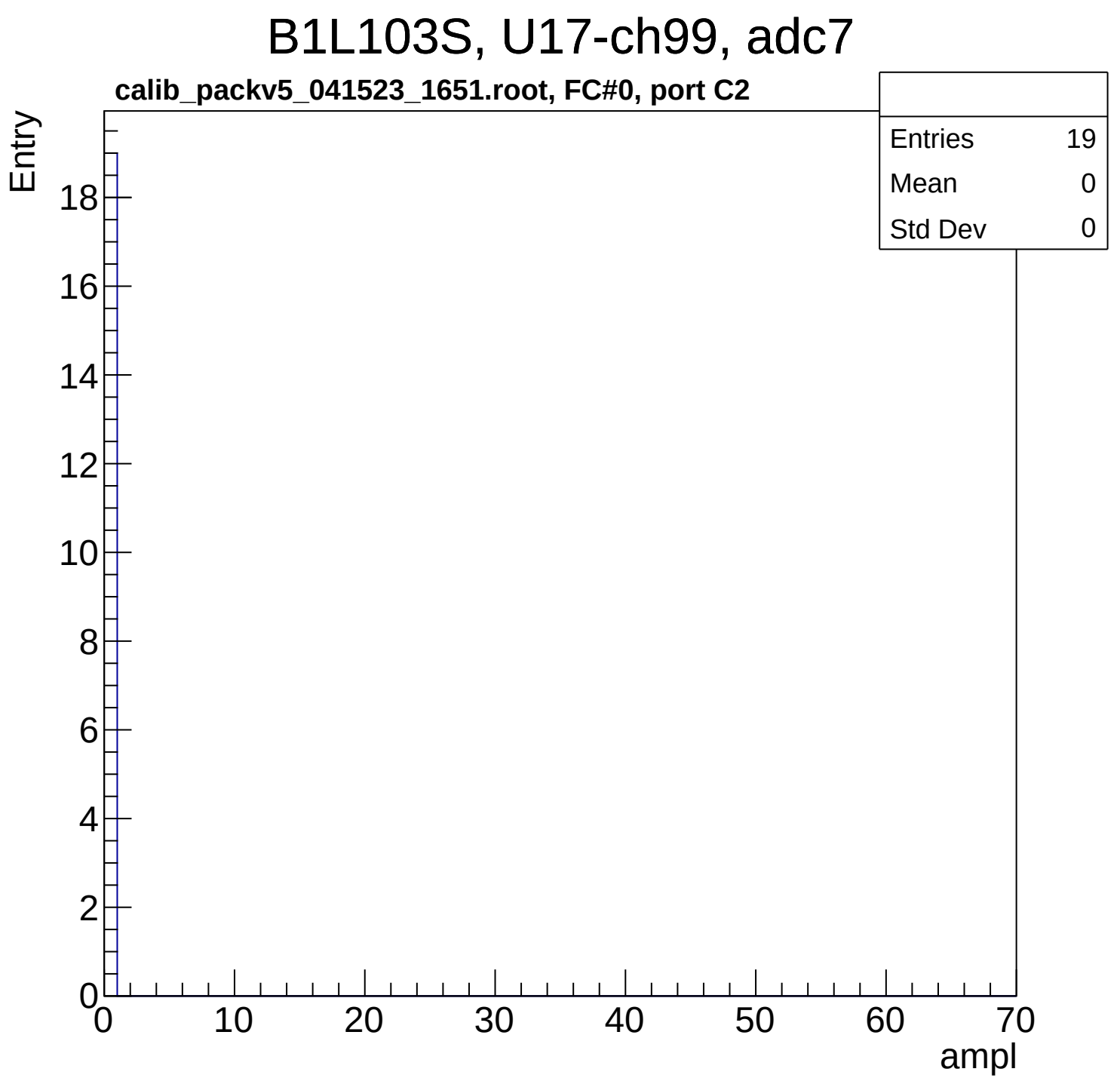

B1L103S, U17-ch99, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 35.46
Std Dev 14.8
Gaus mean : 41.4574
Gaus Width: 4.1226
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

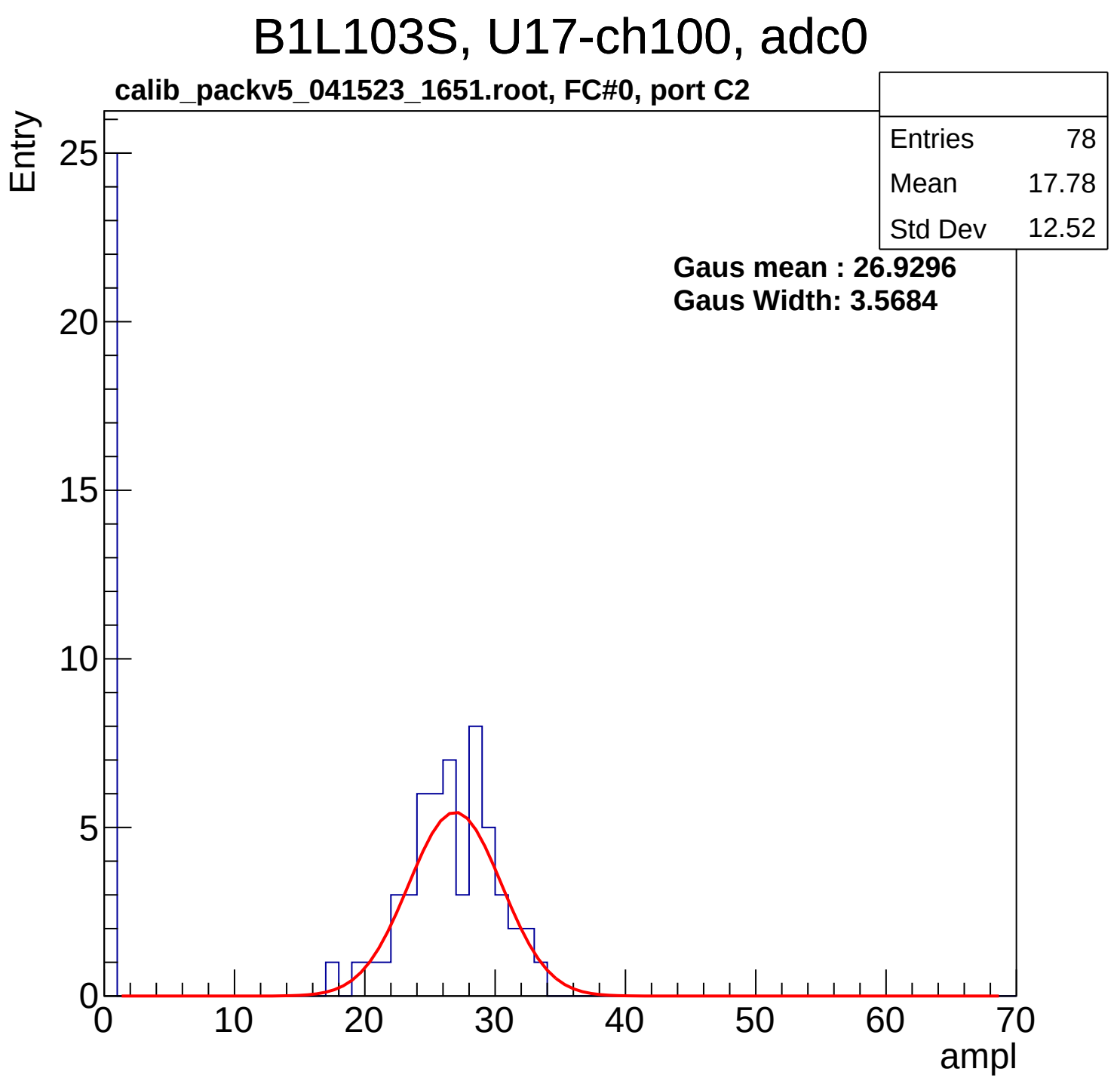

B1L103S, U17-ch99, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 45.45
Std Dev 12.88
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

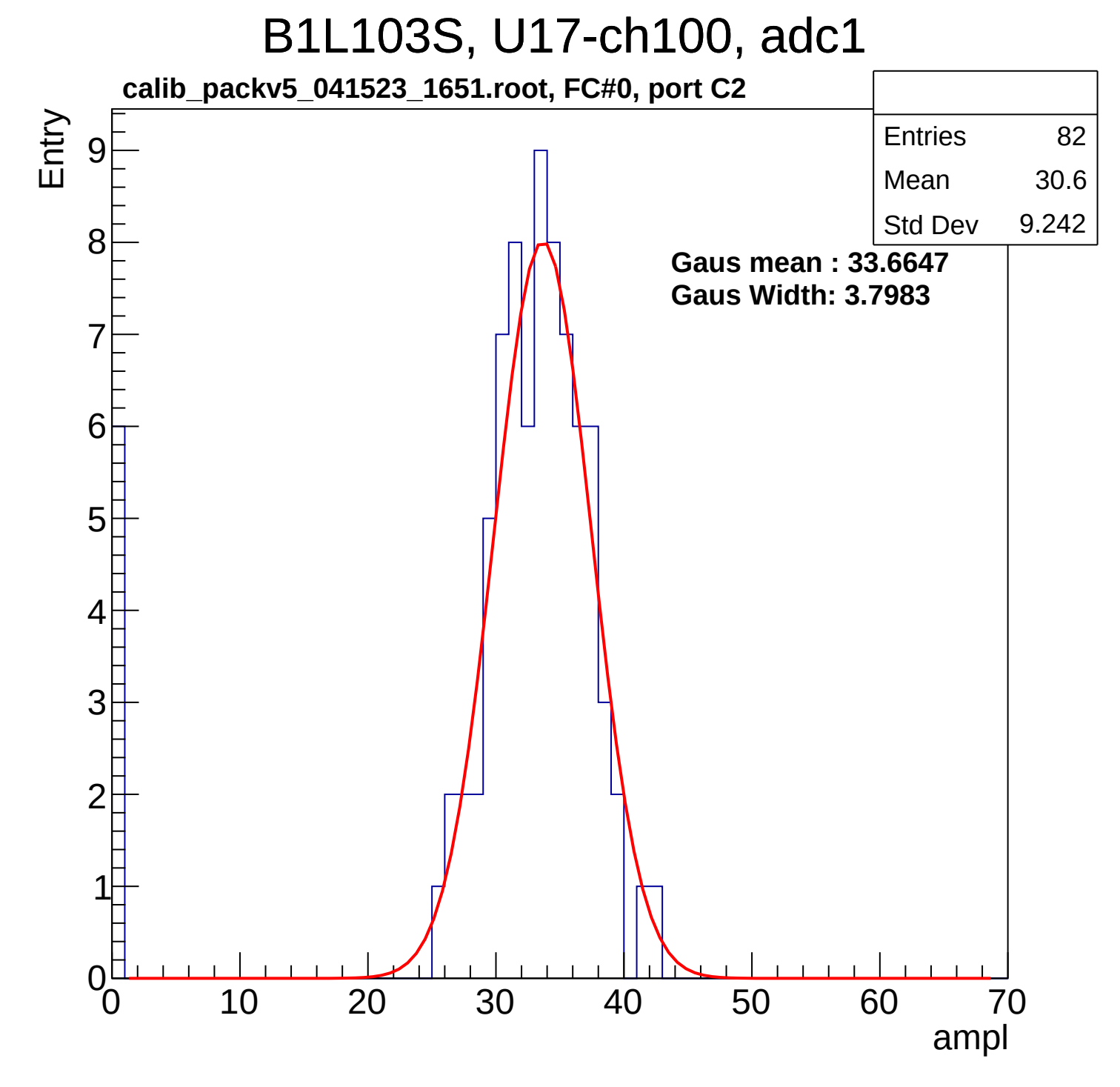

B1L103S, U17-ch99, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 54.6
Std Dev 3.122
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

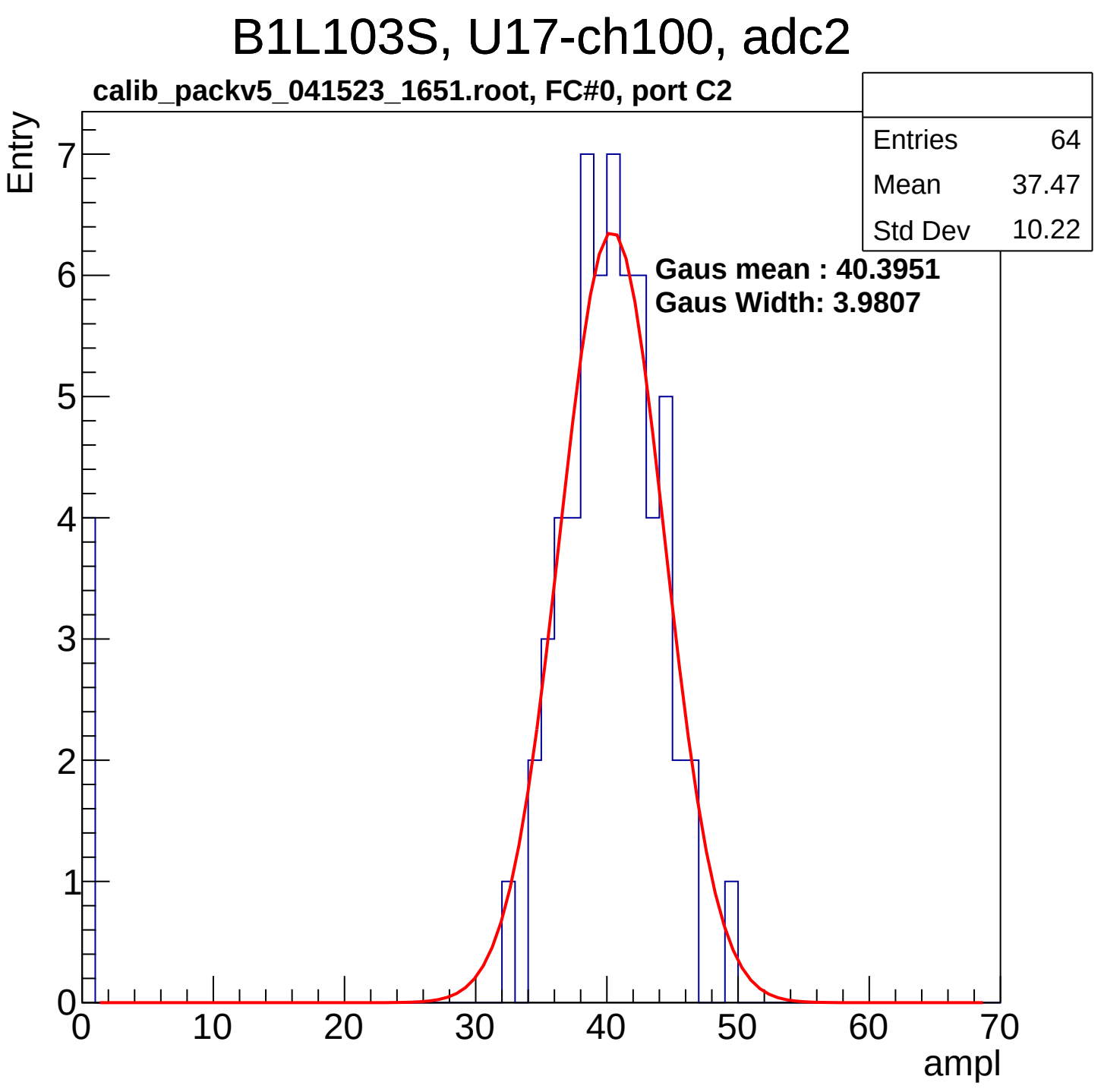

B1L103S, U17-ch99, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.74
Std Dev 8.731
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

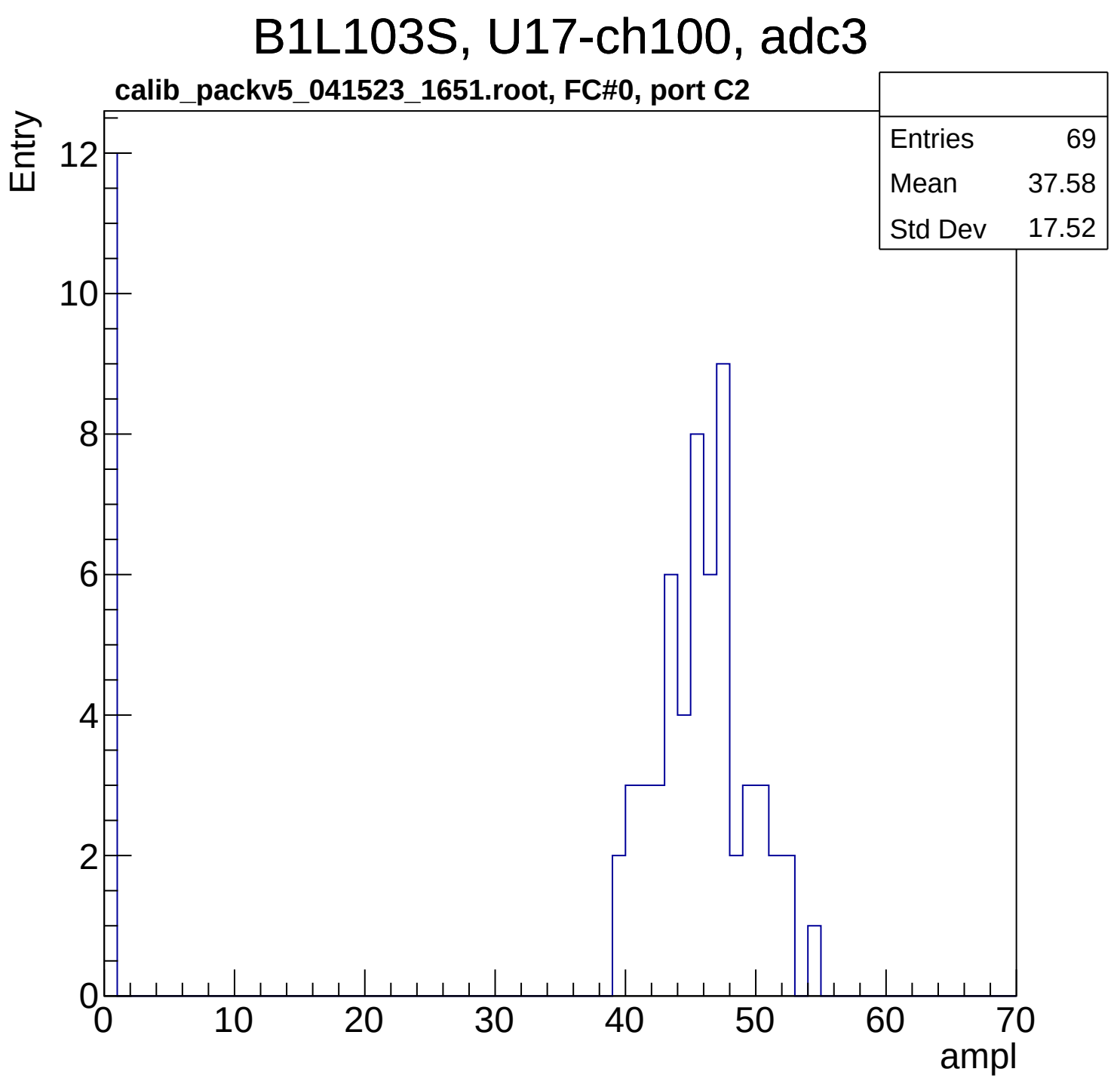

B1L103S, U17-ch99, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.33
Std Dev 0.7454
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

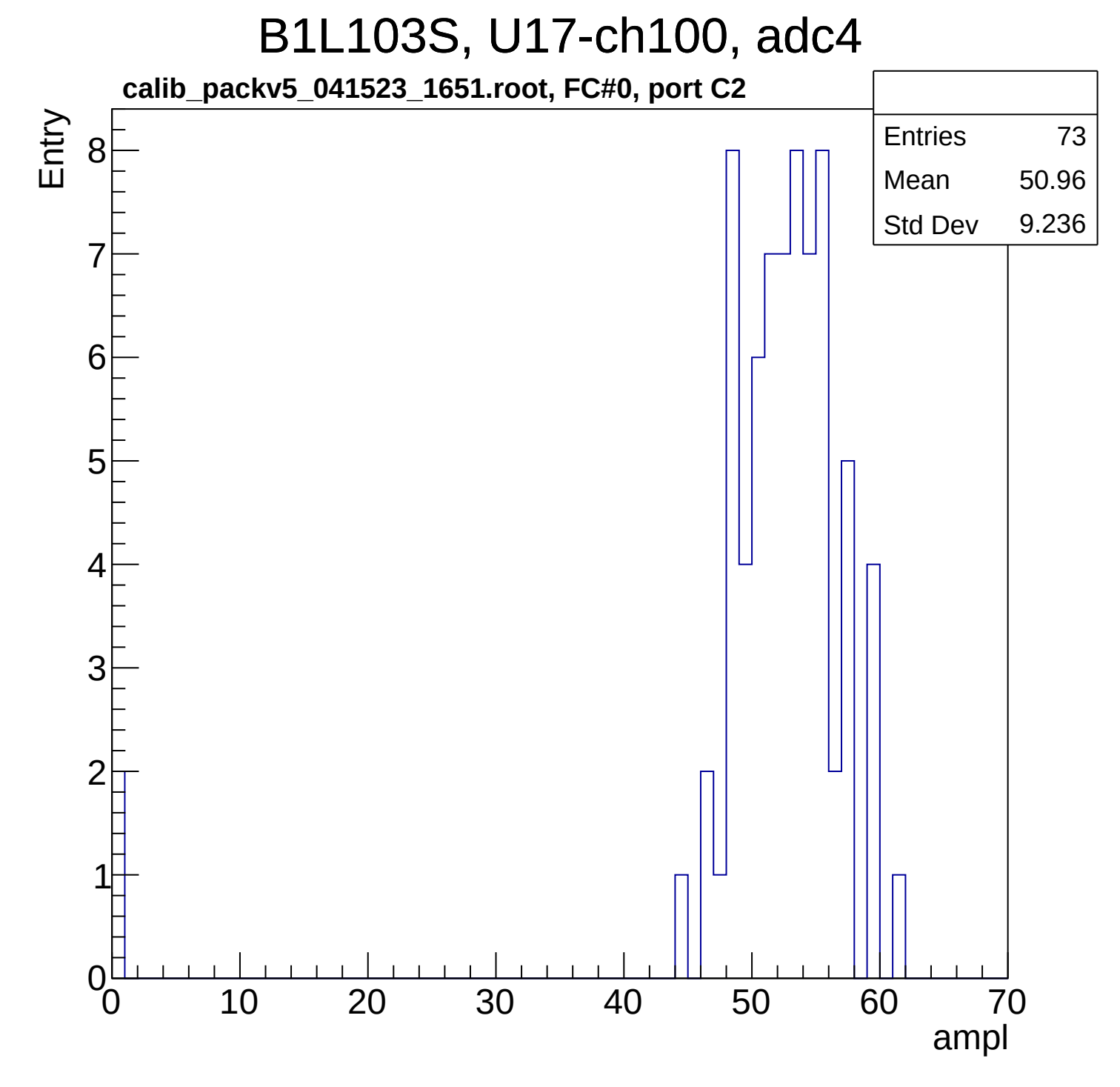

B1L103S, U17-ch99, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

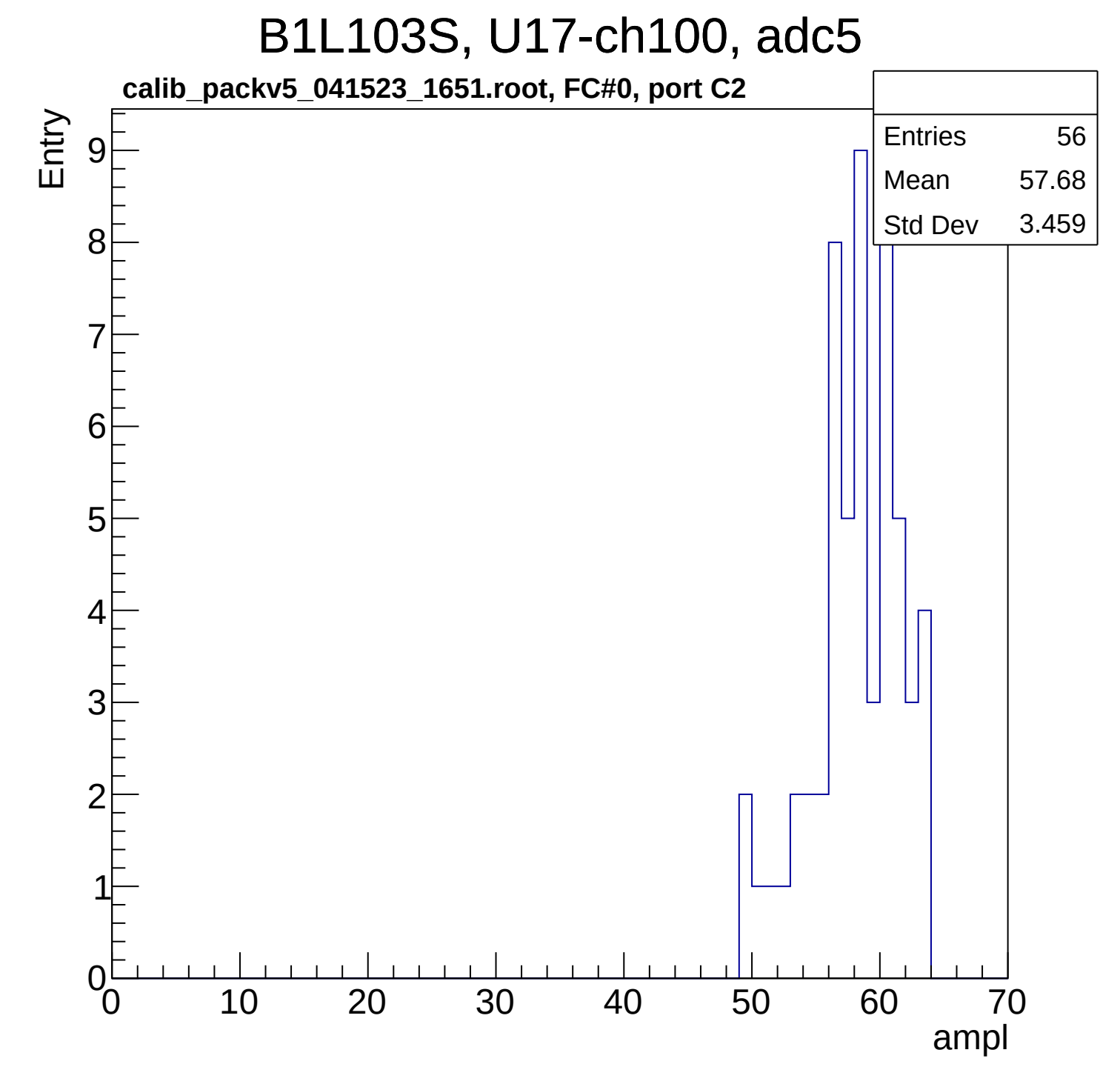

B1L103S, U17-ch100, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 17.78
Std Dev 12.52
Gaus mean : 26.9296
Gaus Width: 3.5684
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70

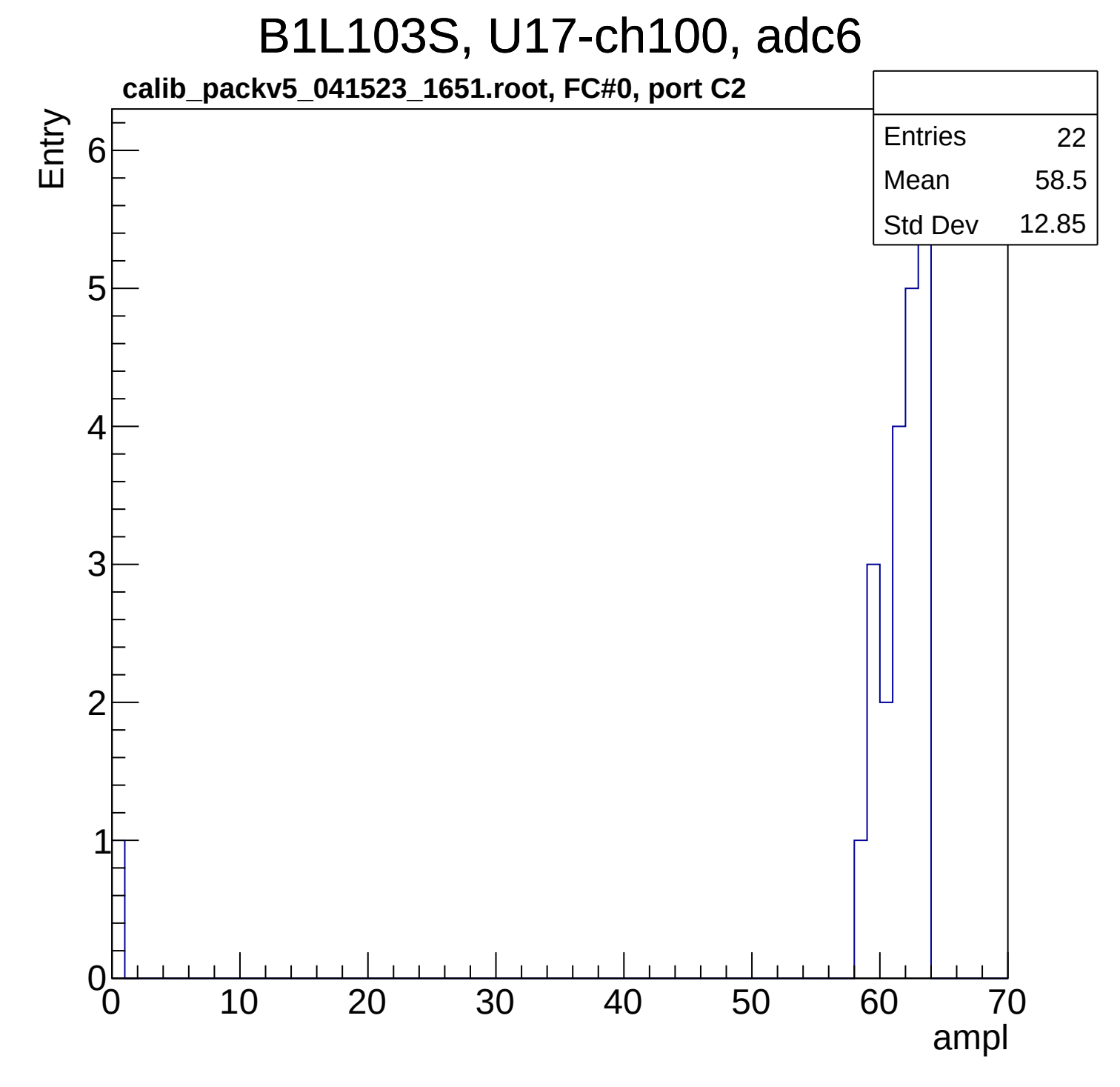

B1L103S, U17-ch100, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 30.6
Std Dev 9.242
Gaus mean : 33.6647
Gaus Width: 3.7983
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

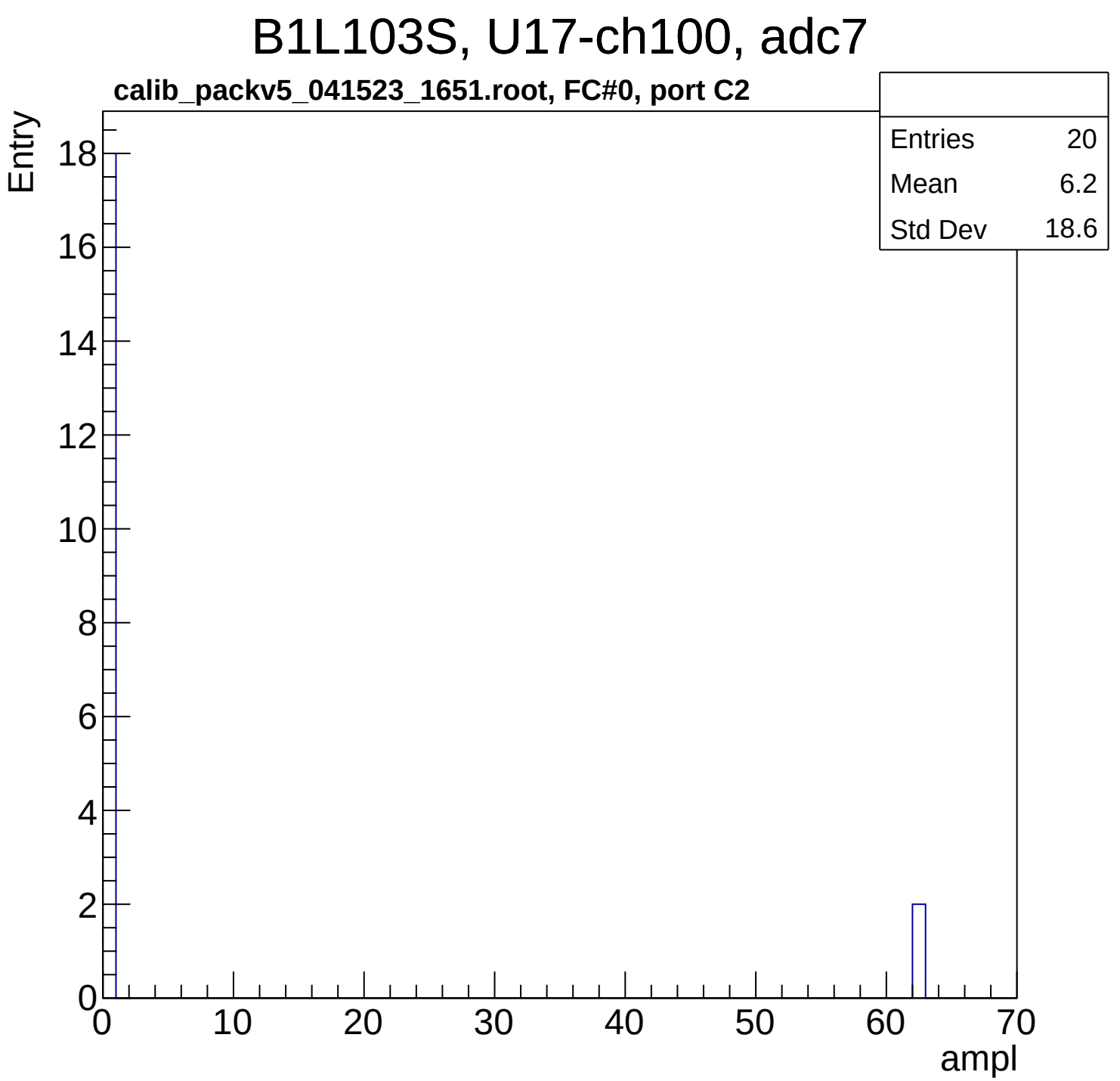

B1L103S, U17-ch100, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 37.47
Std Dev 10.22
Gaus mean : 40.3951
Gaus Width: 3.9807
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

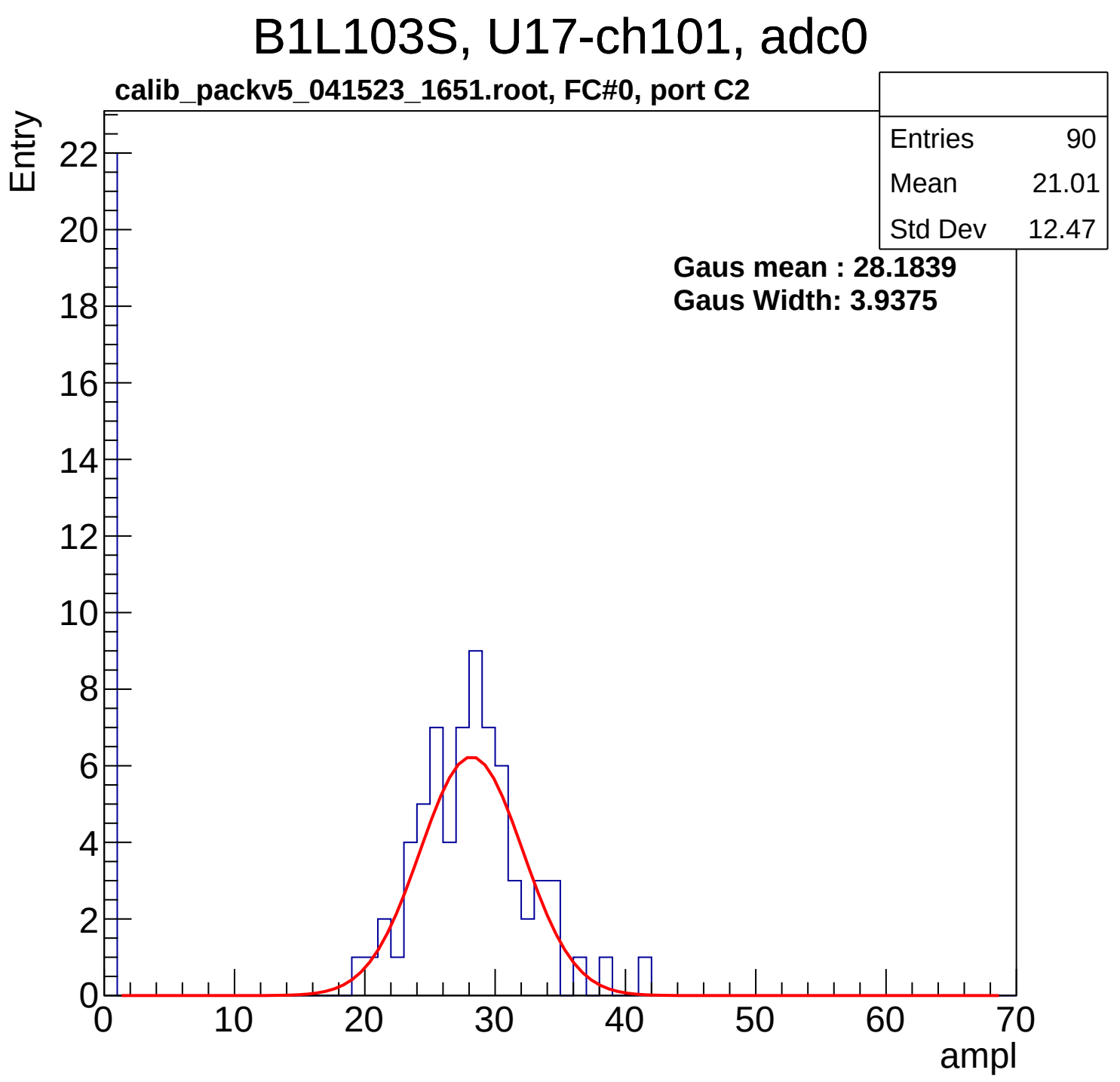

B1L103S, U17-ch100, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 37.58
Std Dev 17.52
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

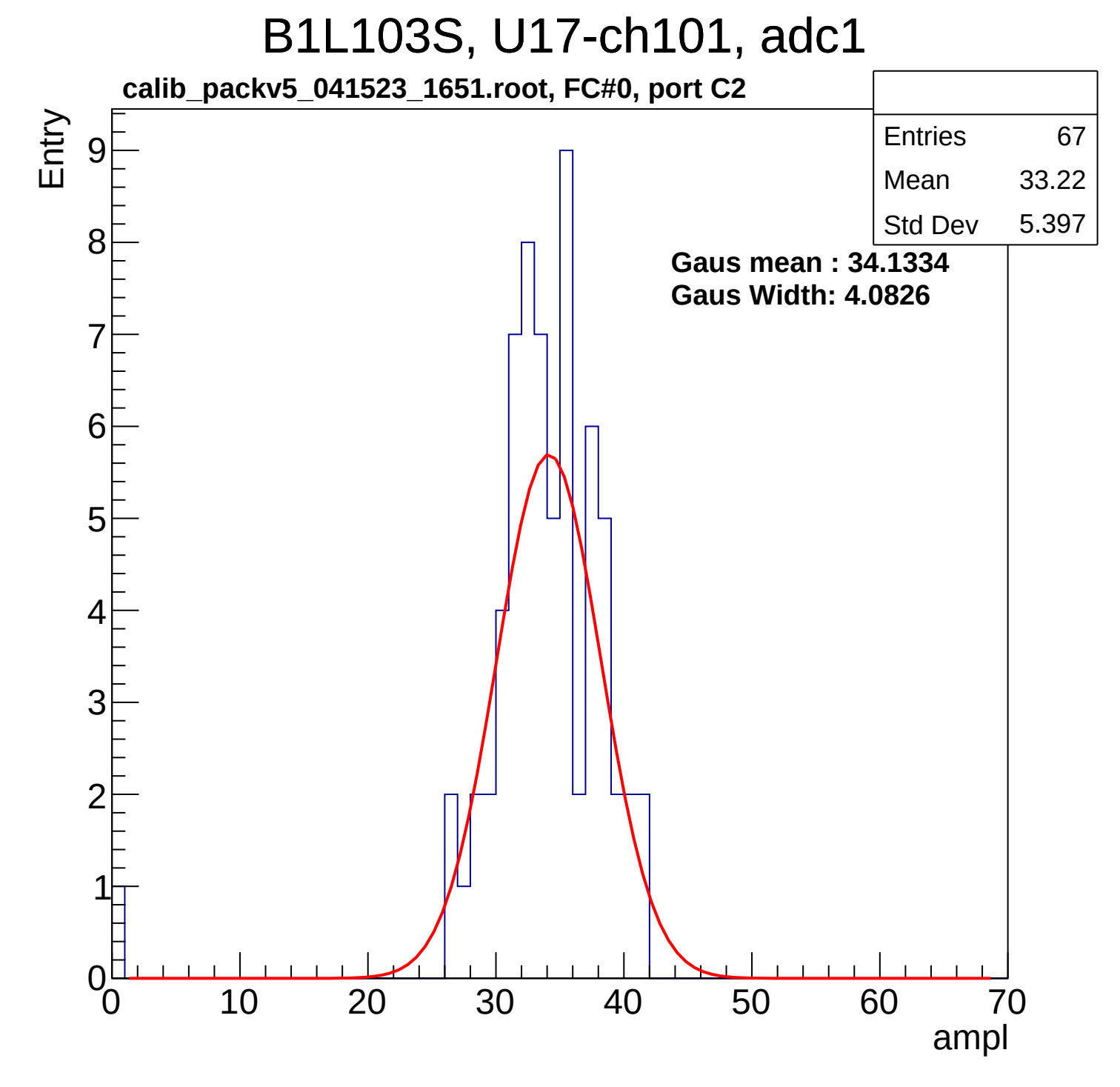

B1L103S, U17-ch100, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 50.96
Std Dev 9.236
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

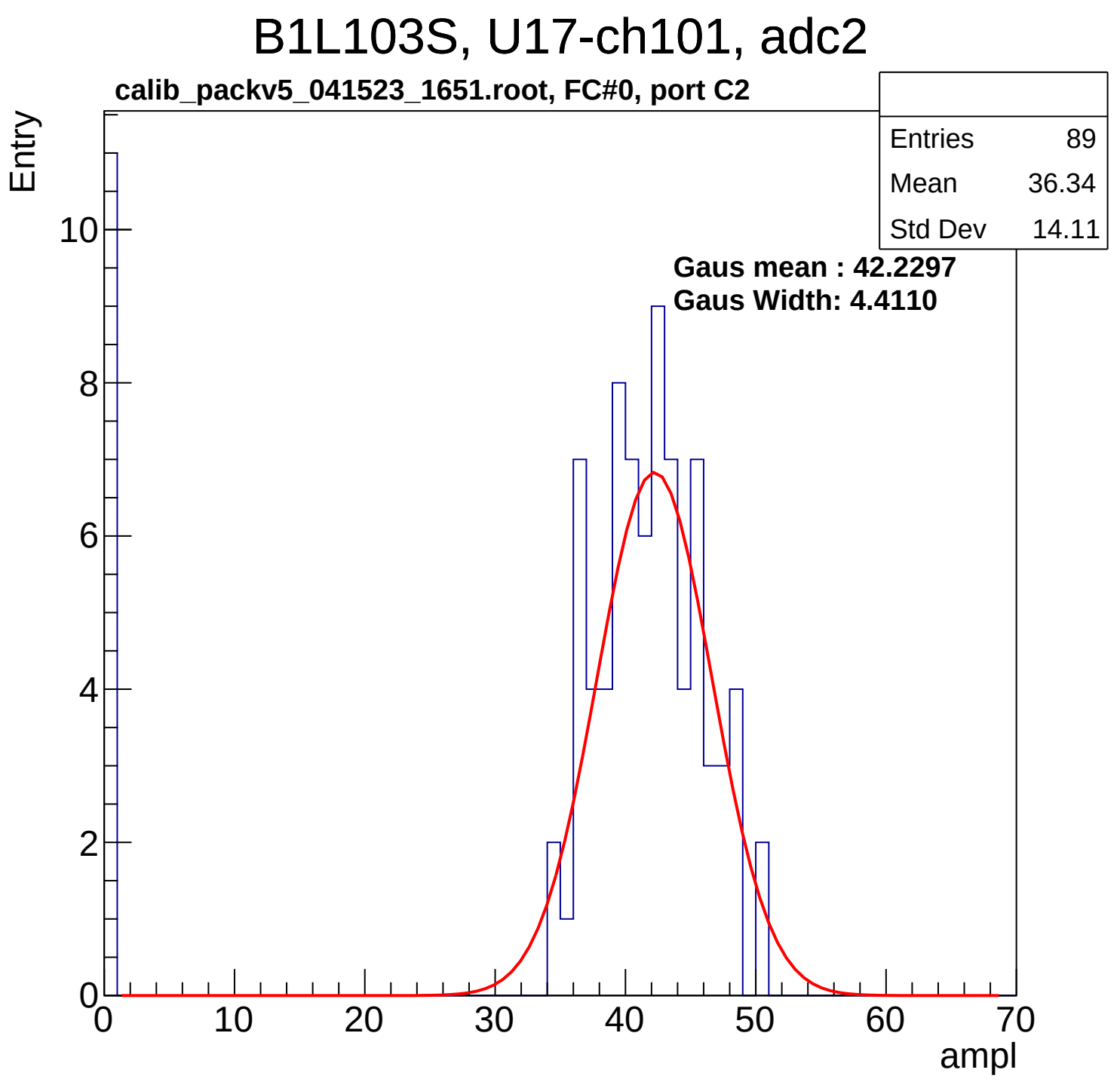

B1L103S, U17-ch100, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 57.68
Std Dev 3.459
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

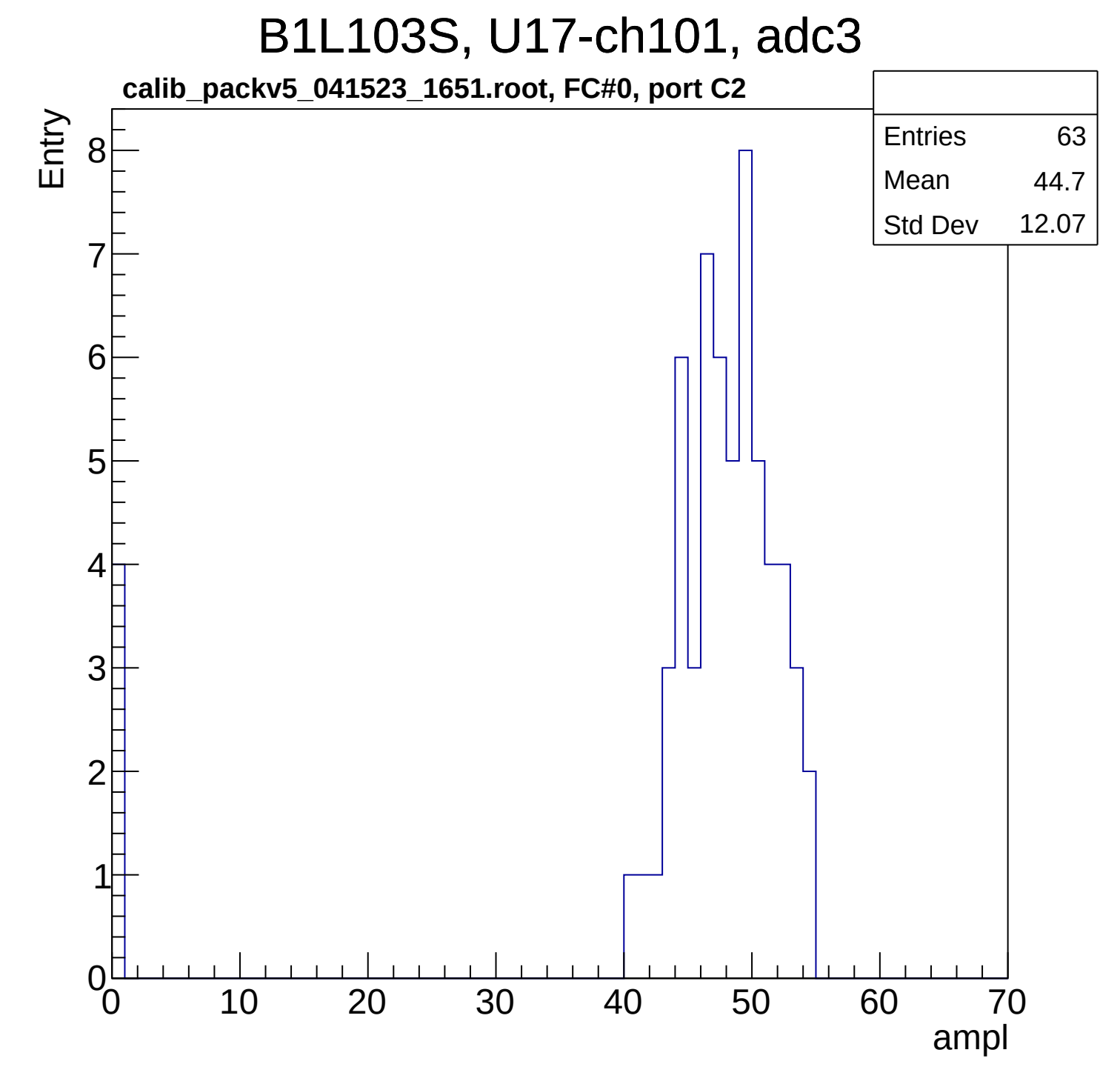

B1L103S, U17-ch100, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.5
Std Dev 12.85
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

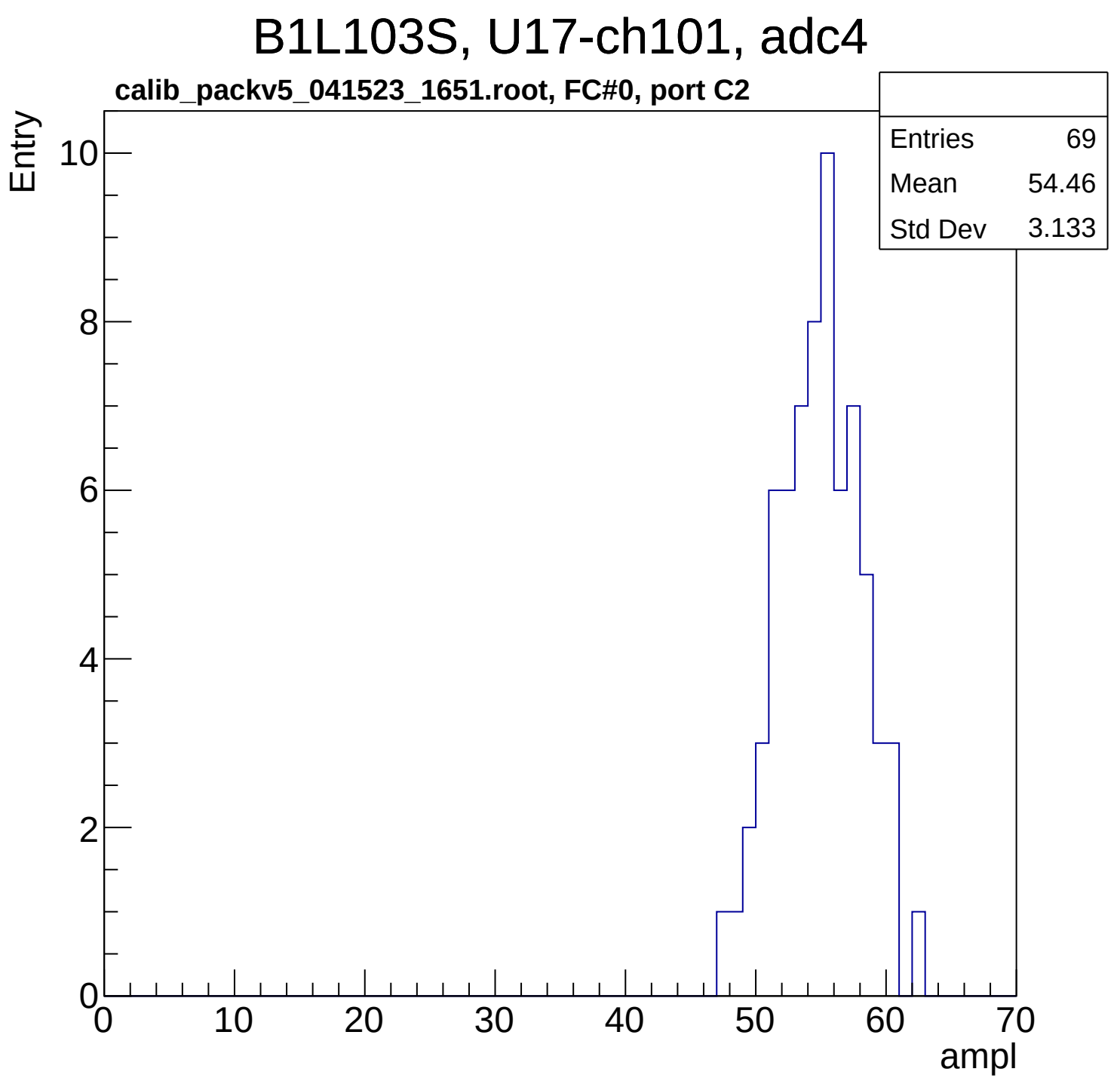

B1L103S, U17-ch100, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.2
Std Dev 18.6
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

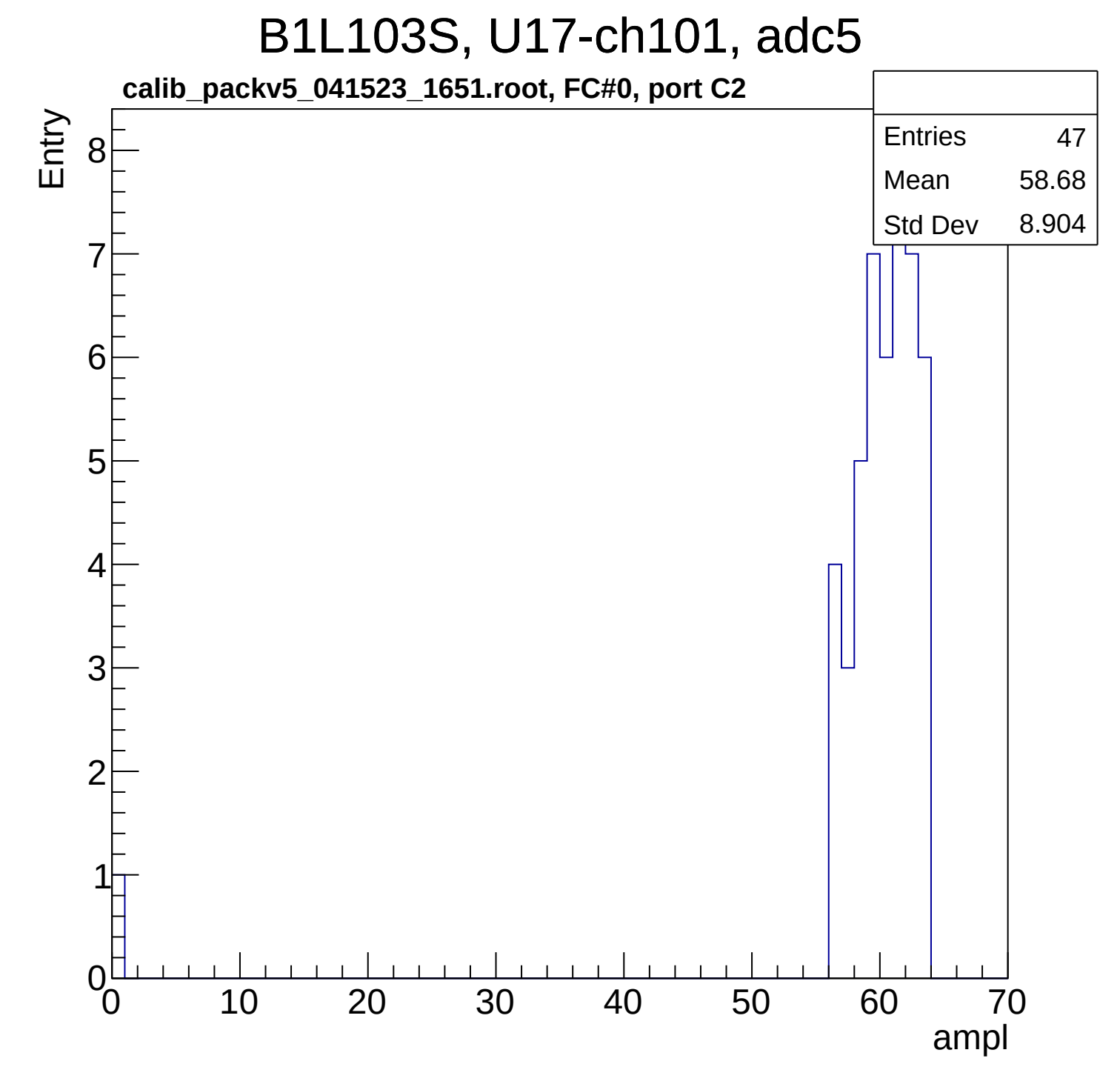

B1L103S, U17-ch101, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 21.01
Std Dev 12.47
Gaus mean : 28.1839
Gaus Width: 3.9375
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70

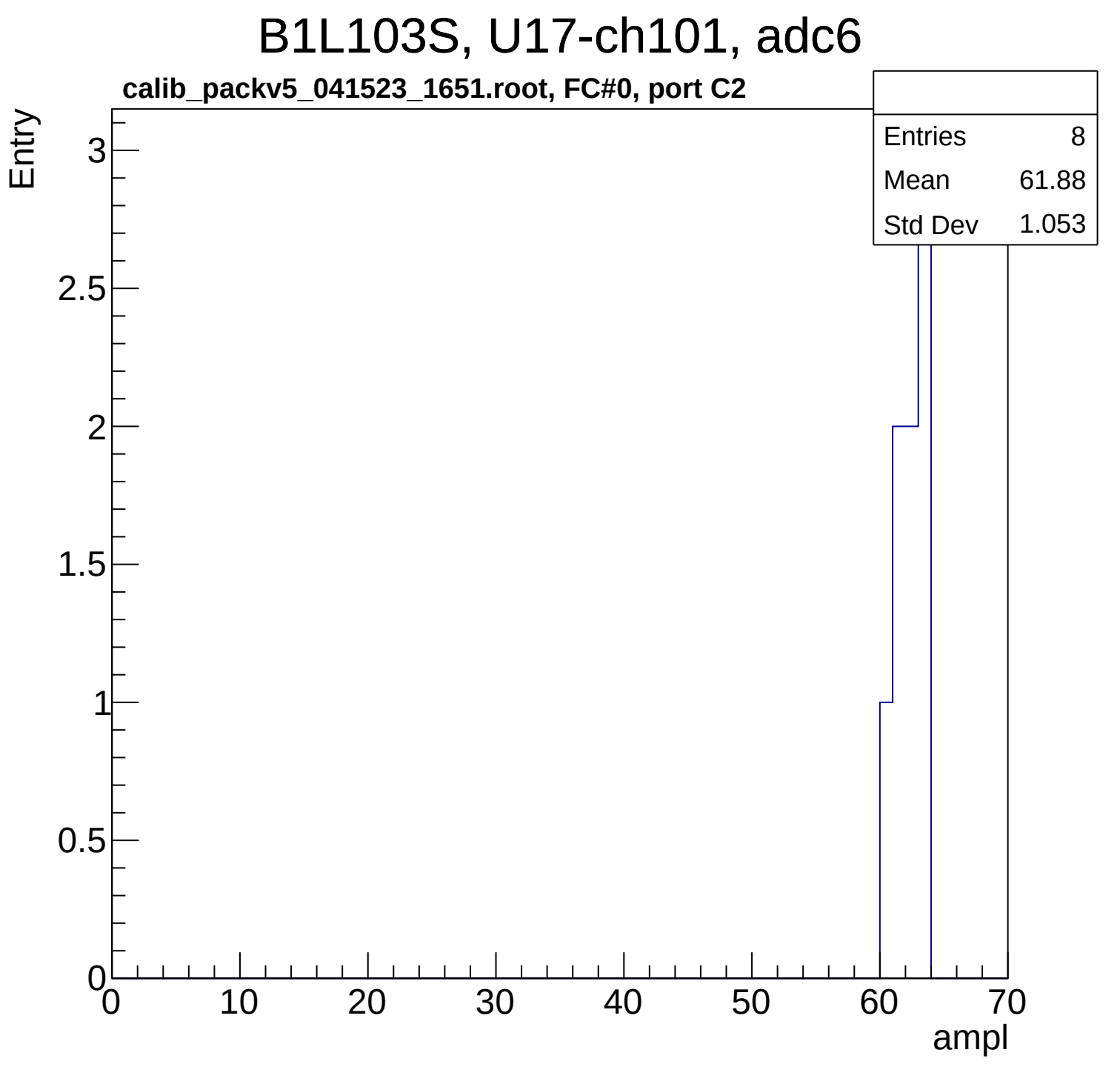

B1L103S, U17-ch101, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 33.22
Std Dev 5.397
Gaus mean : 34.1334
Gaus Width: 4.0826
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

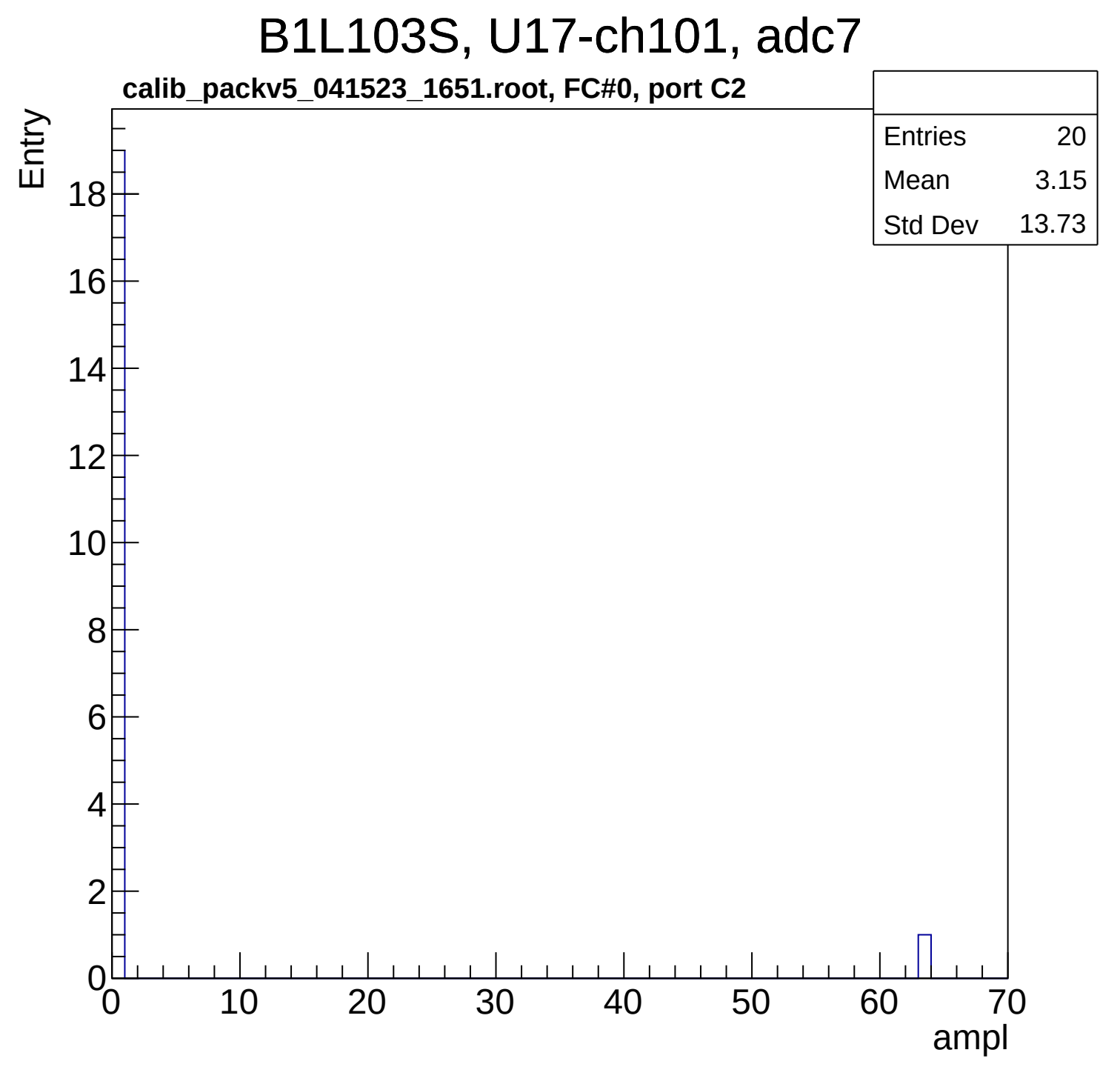

B1L103S, U17-ch101, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 36.34
Std Dev 14.11
Gaus mean : 42.2297
Gaus Width: 4.4110
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

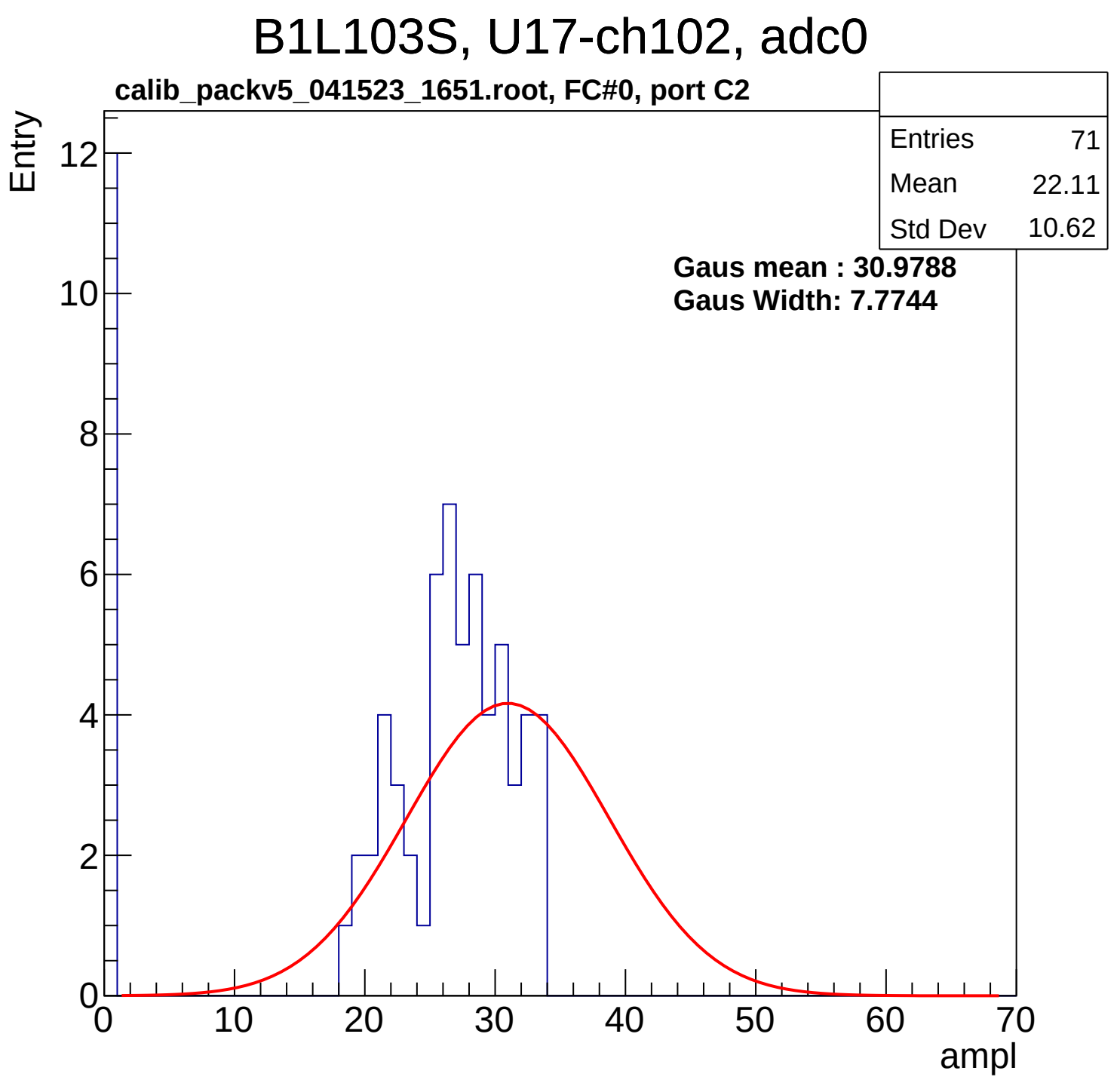

B1L103S, U17-ch101, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 44.7
Std Dev 12.07
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

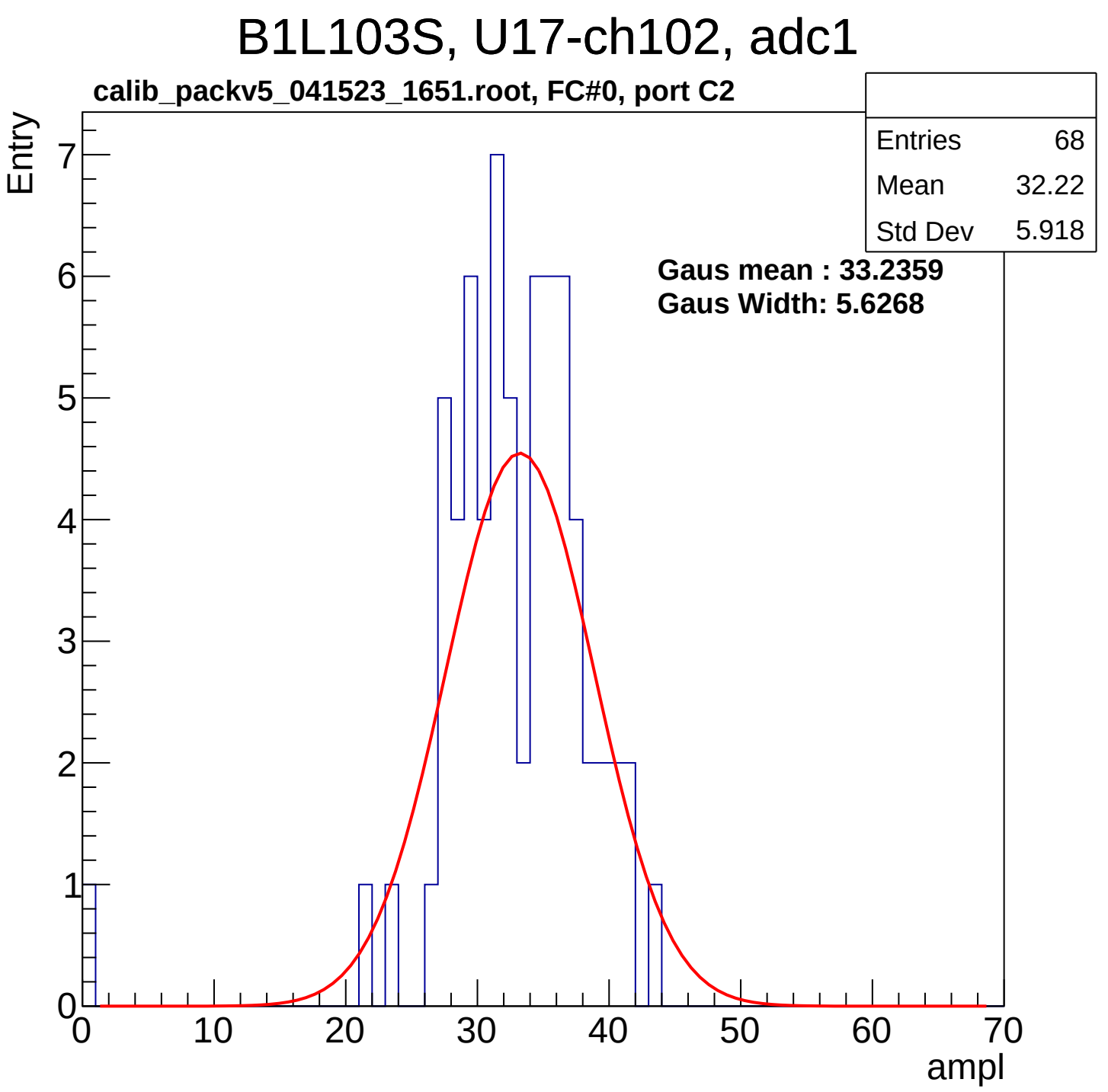

B1L103S, U17-ch101, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 54.46
Std Dev 3.133
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

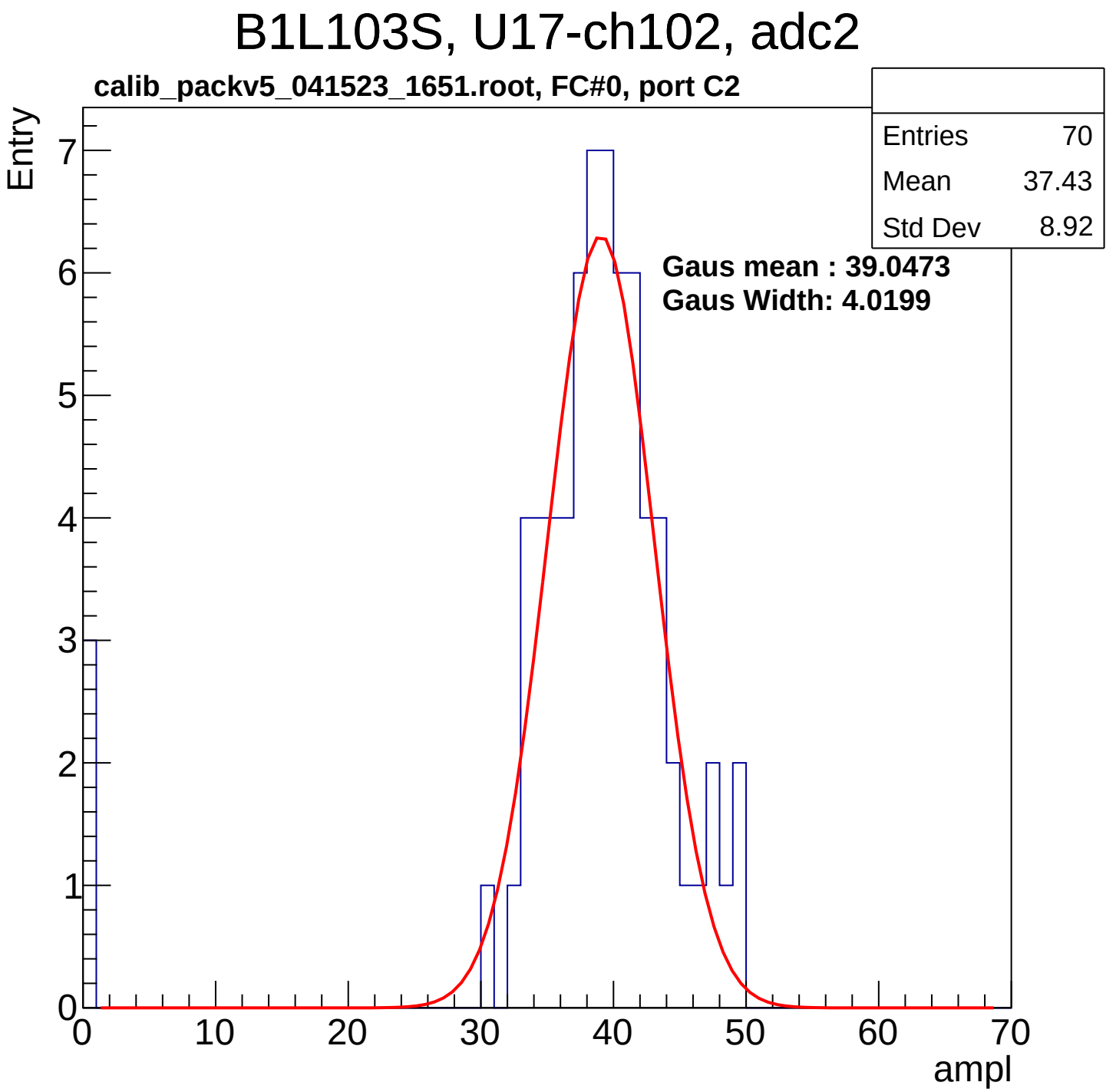

B1L103S, U17-ch101, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.68
Std Dev 8.904
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

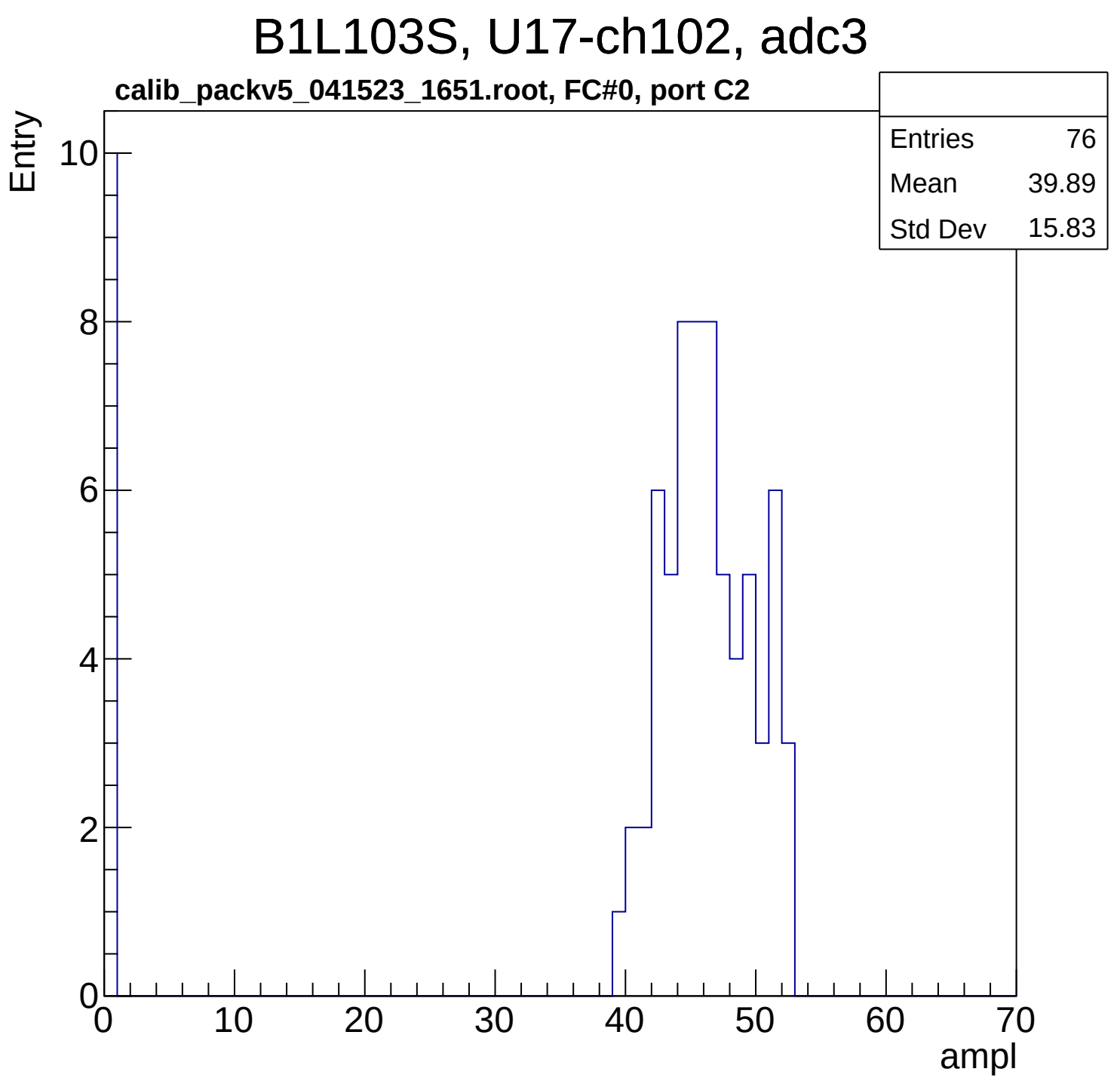

B1L103S, U17-ch101, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.88
Std Dev 1.053
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

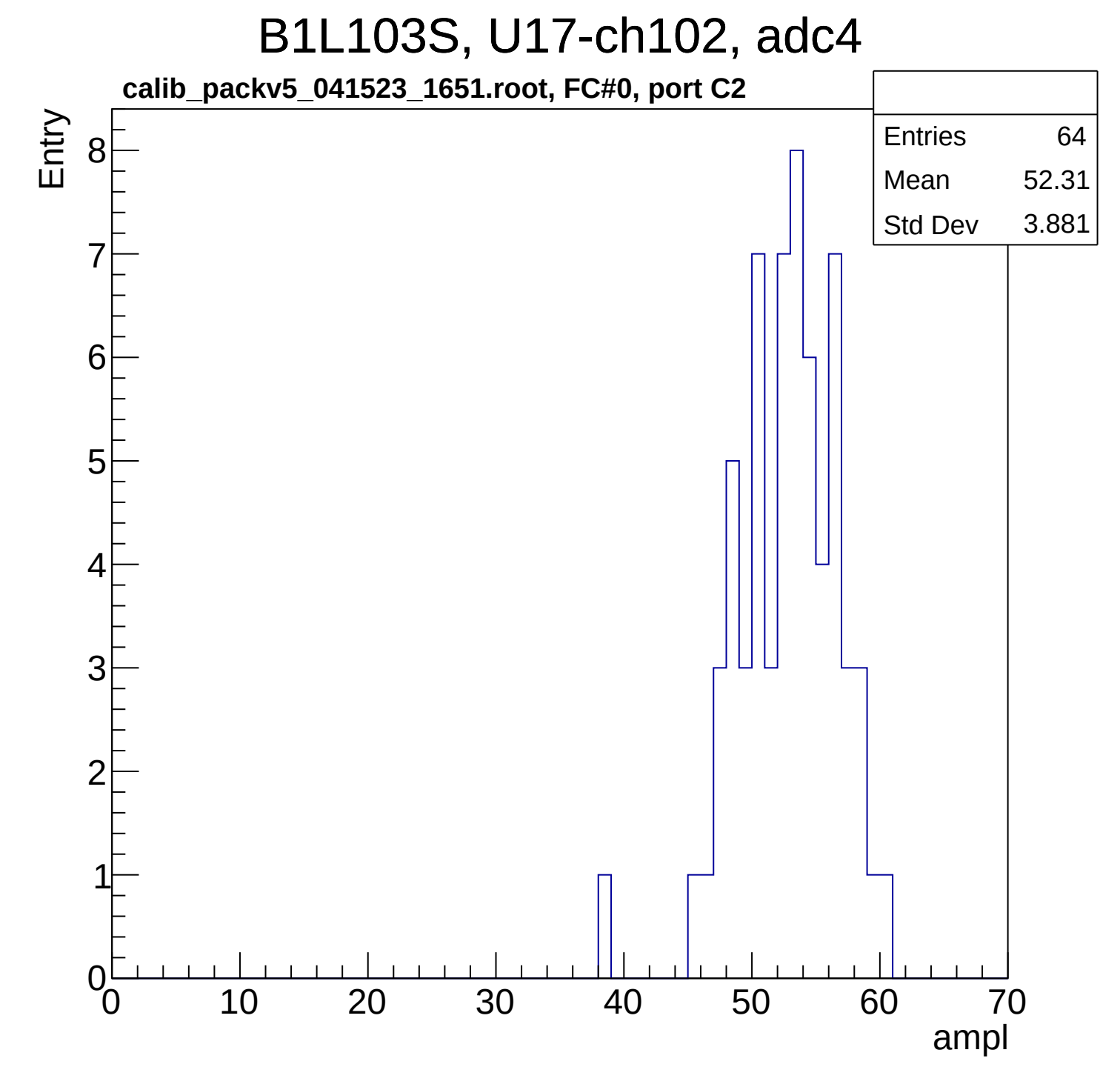

B1L103S, U17-ch101, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

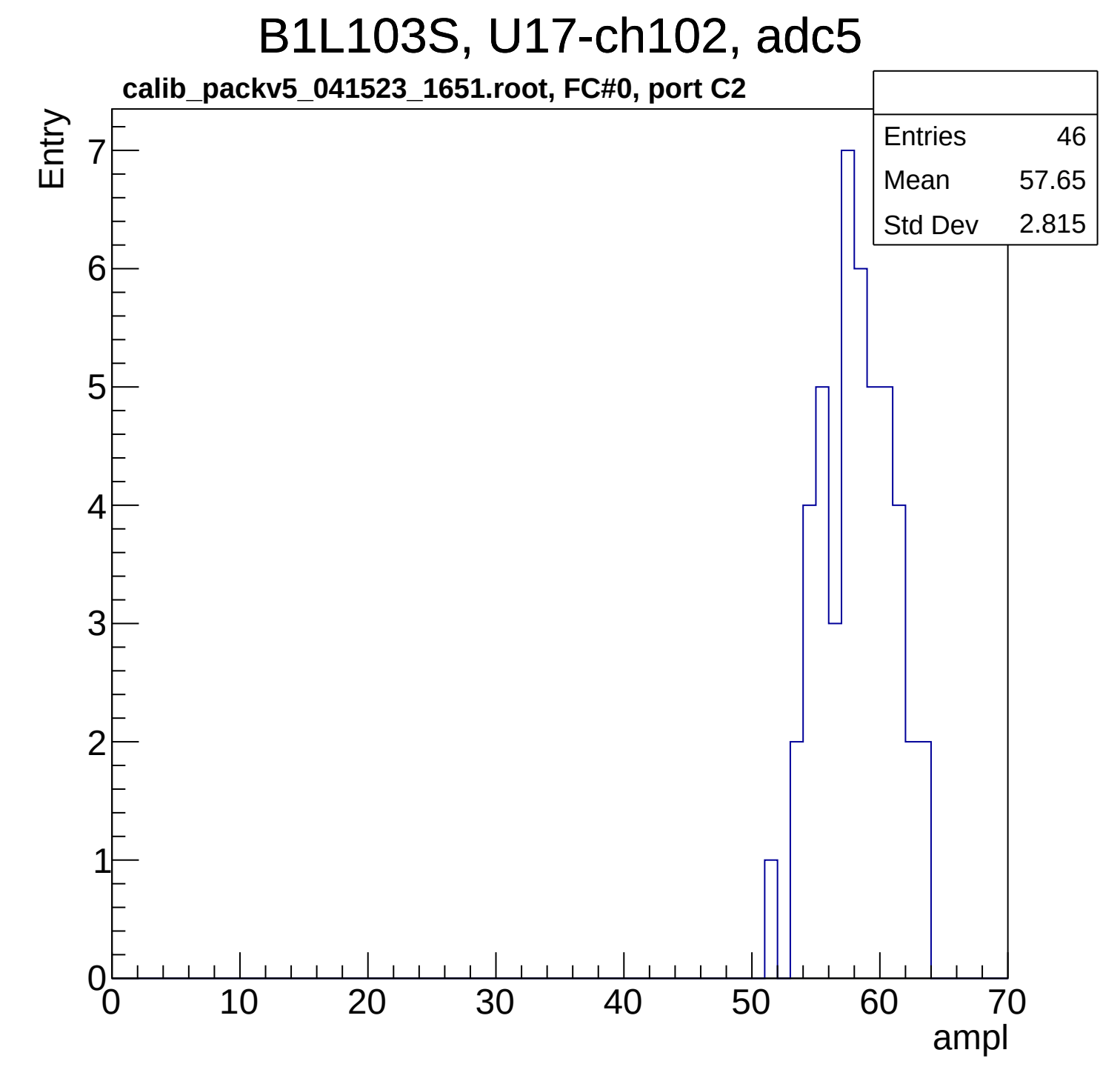

B1L103S, U17-ch102, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 22.11
Std Dev 10.62
Gaus mean : 30.9788
Gaus Width: 7.7744
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

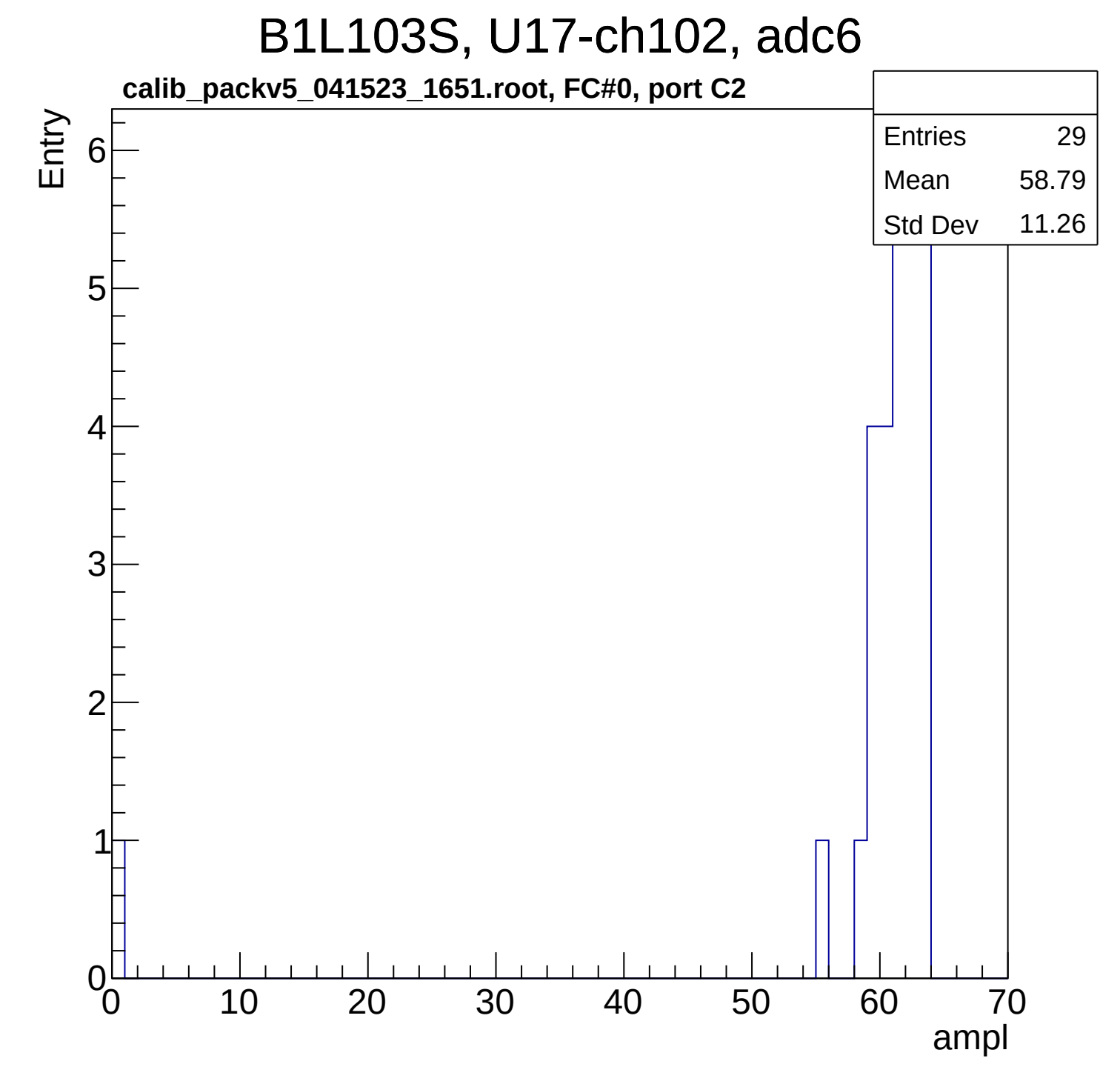

B1L103S, U17-ch102, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 32.22
Std Dev 5.918
Gaus mean : 33.2359
Gaus Width: 5.6268
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

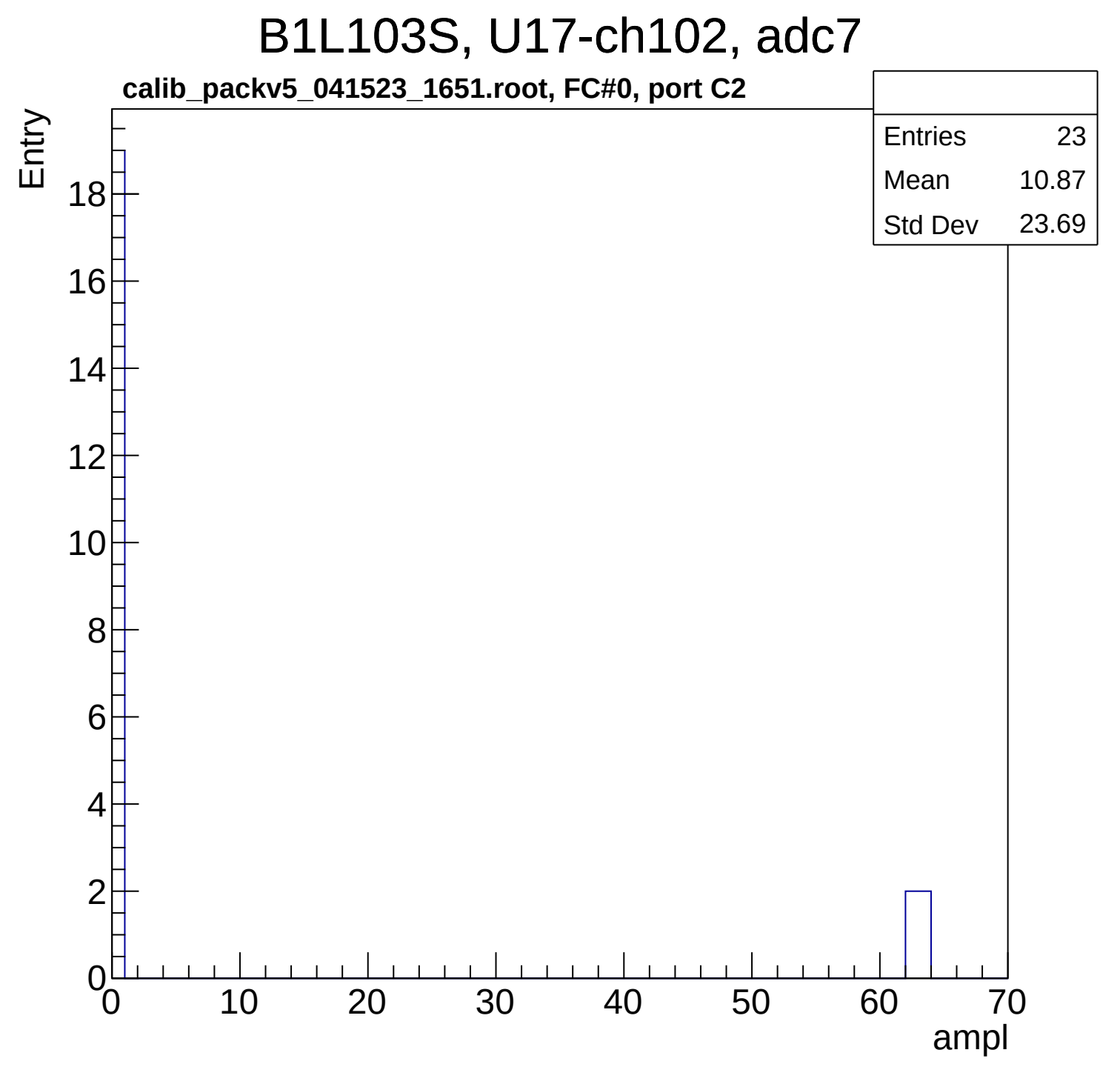

B1L103S, U17-ch102, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 37.43
Std Dev 8.92
Gaus mean : 39.0473
Gaus Width: 4.0199
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

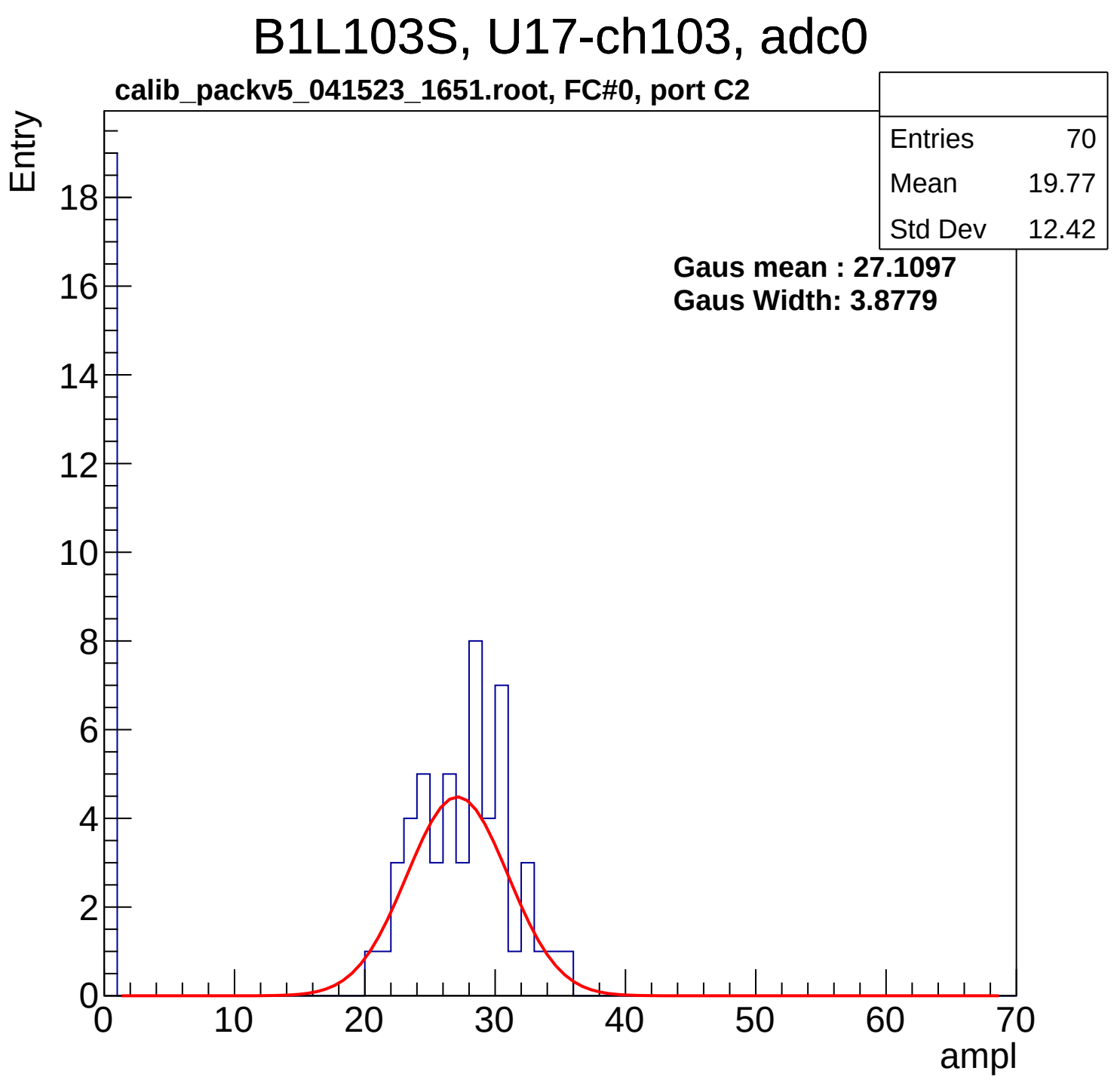

B1L103S, U17-ch102, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 39.89
Std Dev 15.83
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

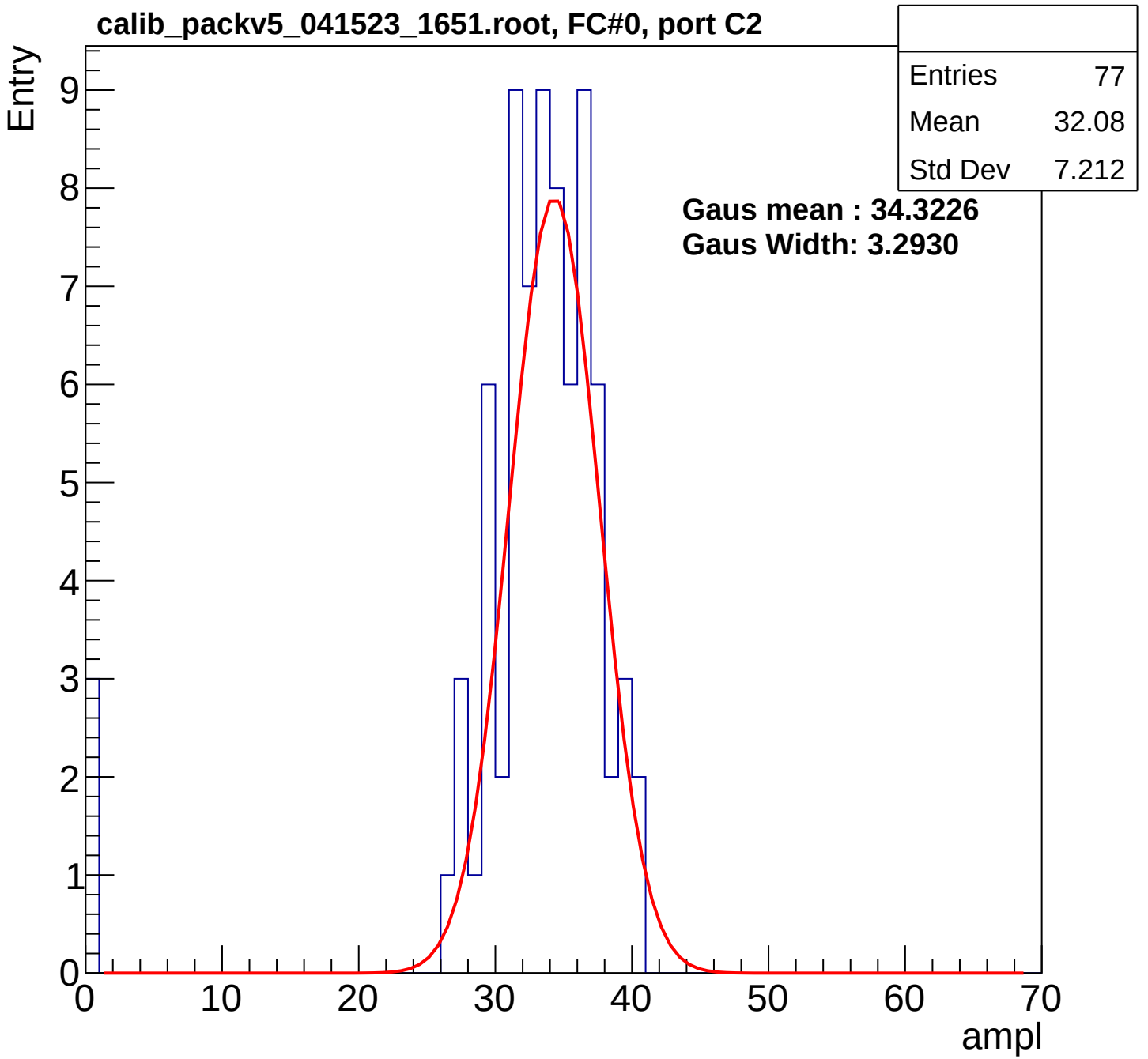

B1L103S, U17-ch102, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 52.31
Std Dev 3.881
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

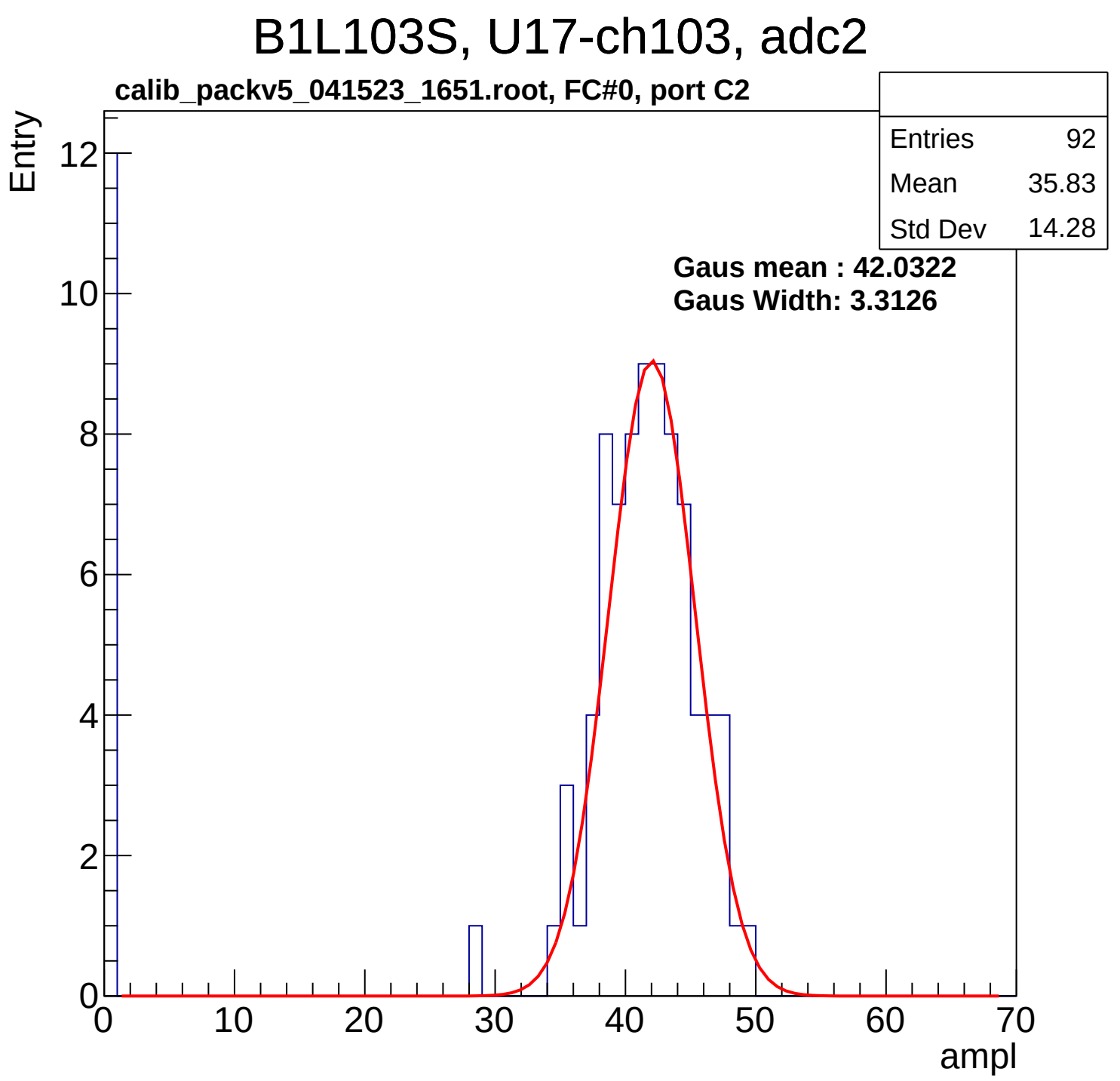

B1L103S, U17-ch102, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 57.65
Std Dev 2.815
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

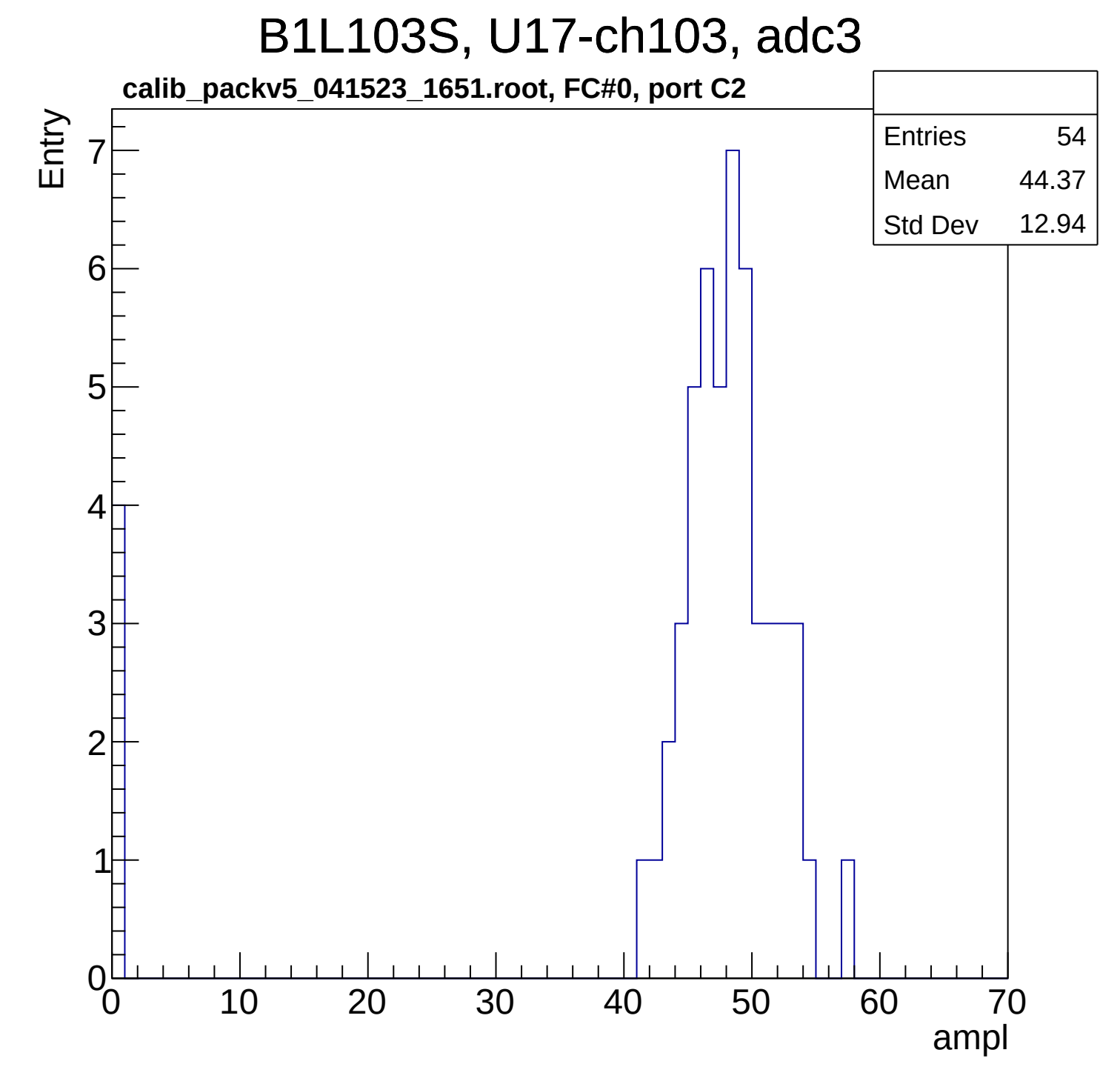

B1L103S, U17-ch102, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 58.79
Std Dev 11.26
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

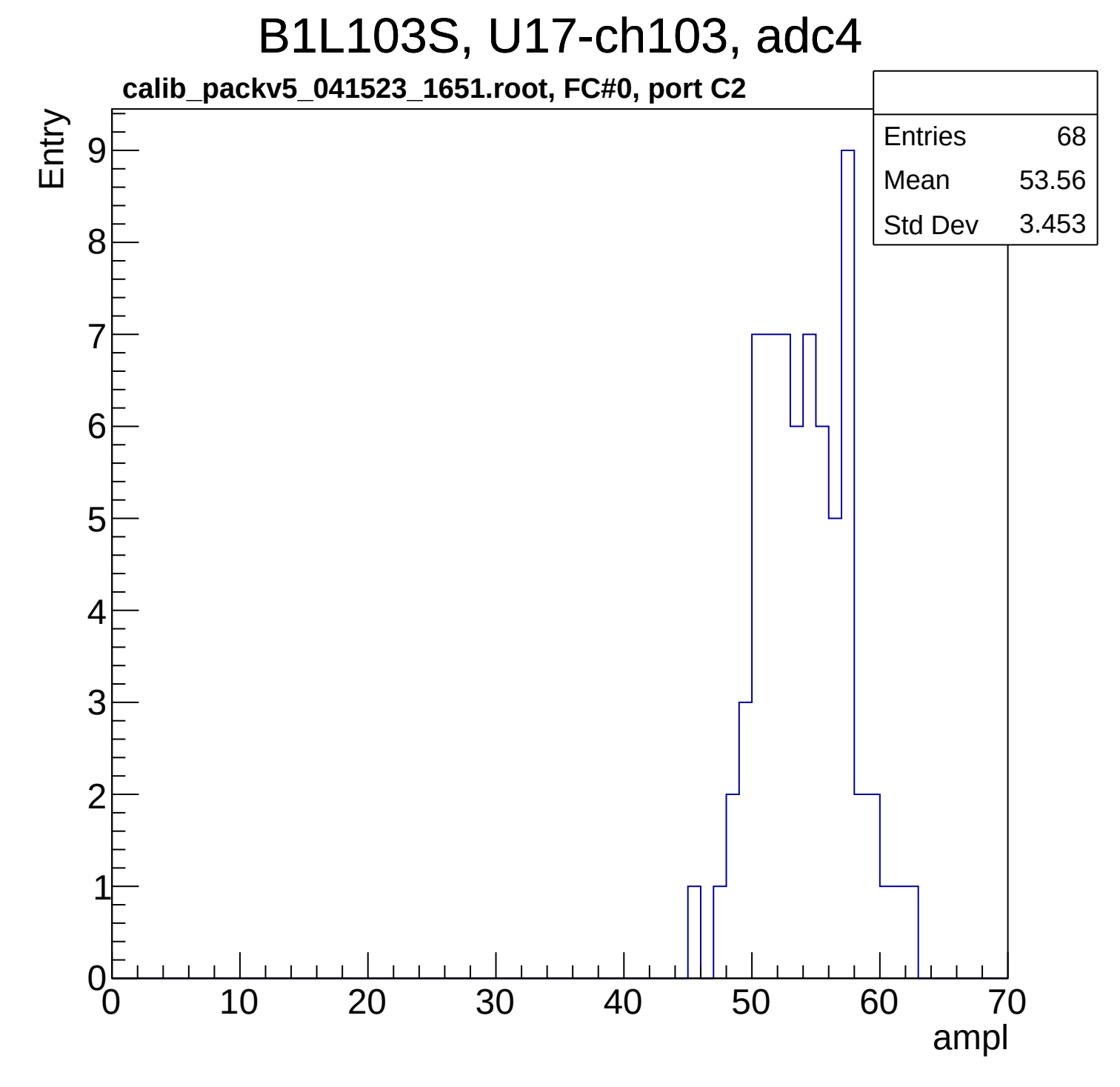

B1L103S, U17-ch102, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.87
Std Dev 23.69
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

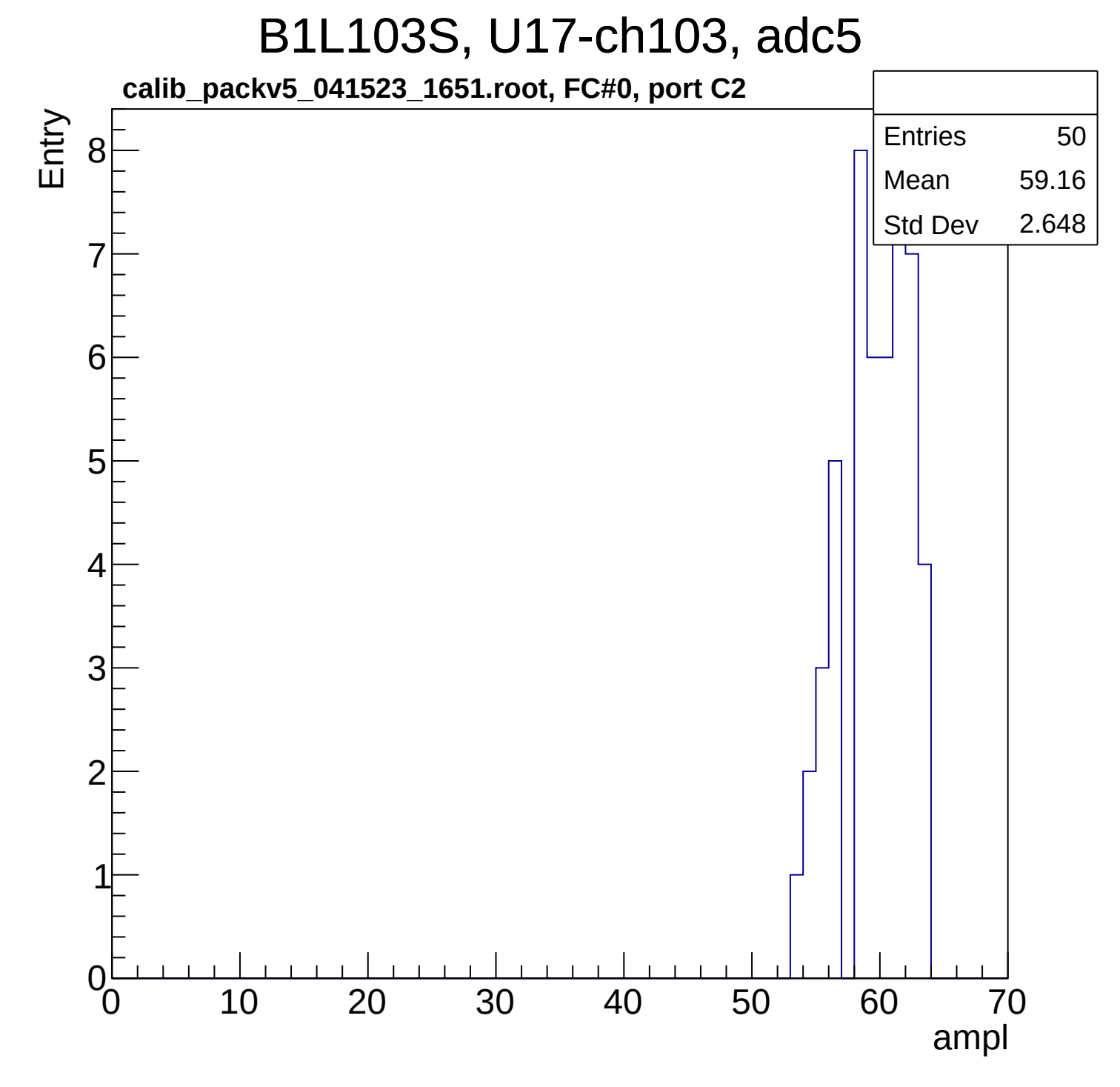

B1L103S, U17-ch103, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 19.77
Std Dev 12.42
Gaus mean : 27.1097
Gaus Width: 3.8779
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

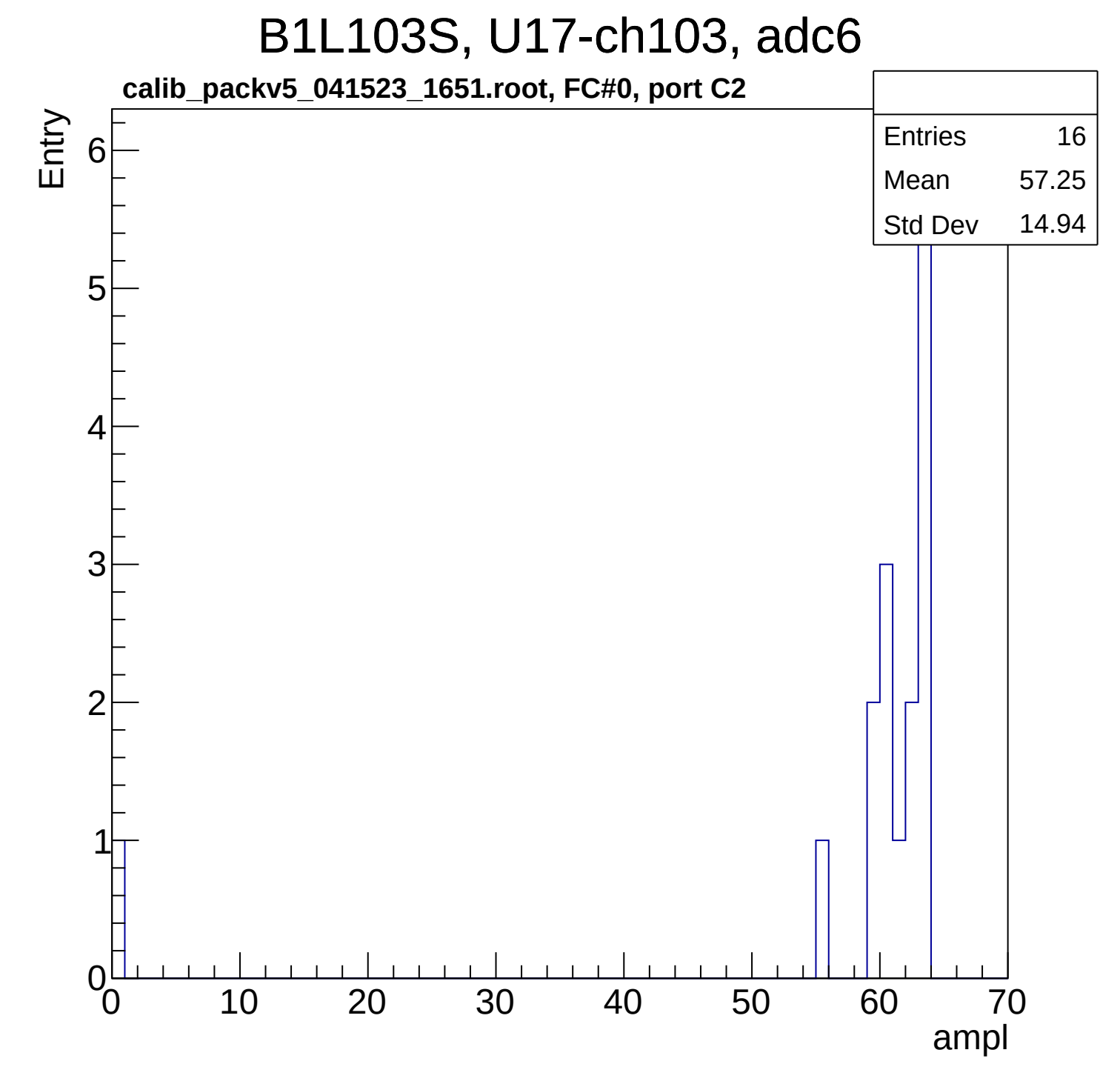

B1L103S, U17-ch103, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 32.08
Std Dev 7.212
Gaus mean : 34.3226
Gaus Width: 3.2930
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

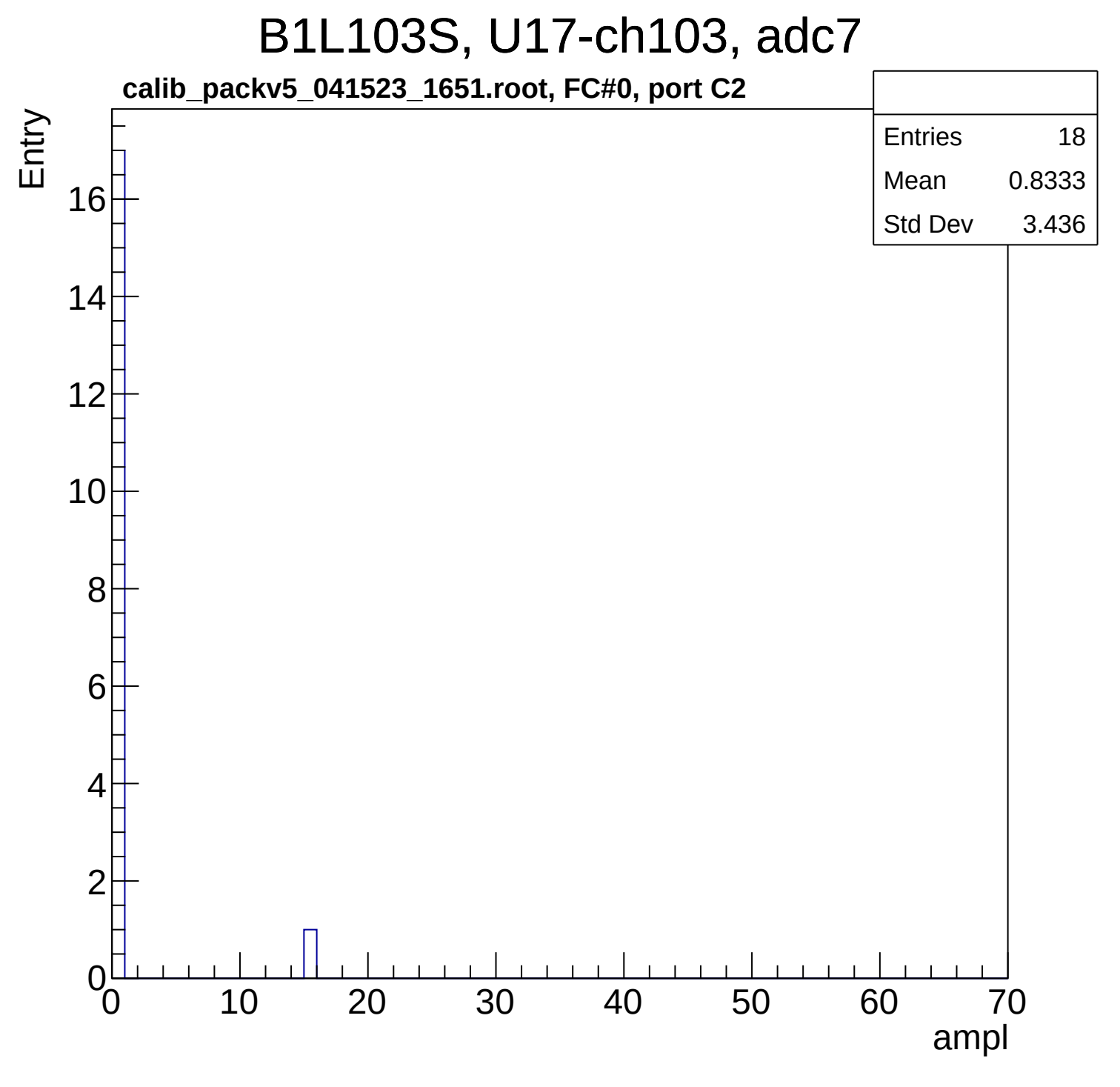

B1L103S, U17-ch103, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 35.83
Std Dev 14.28
Gaus mean : 42.0322
Gaus Width: 3.3126
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

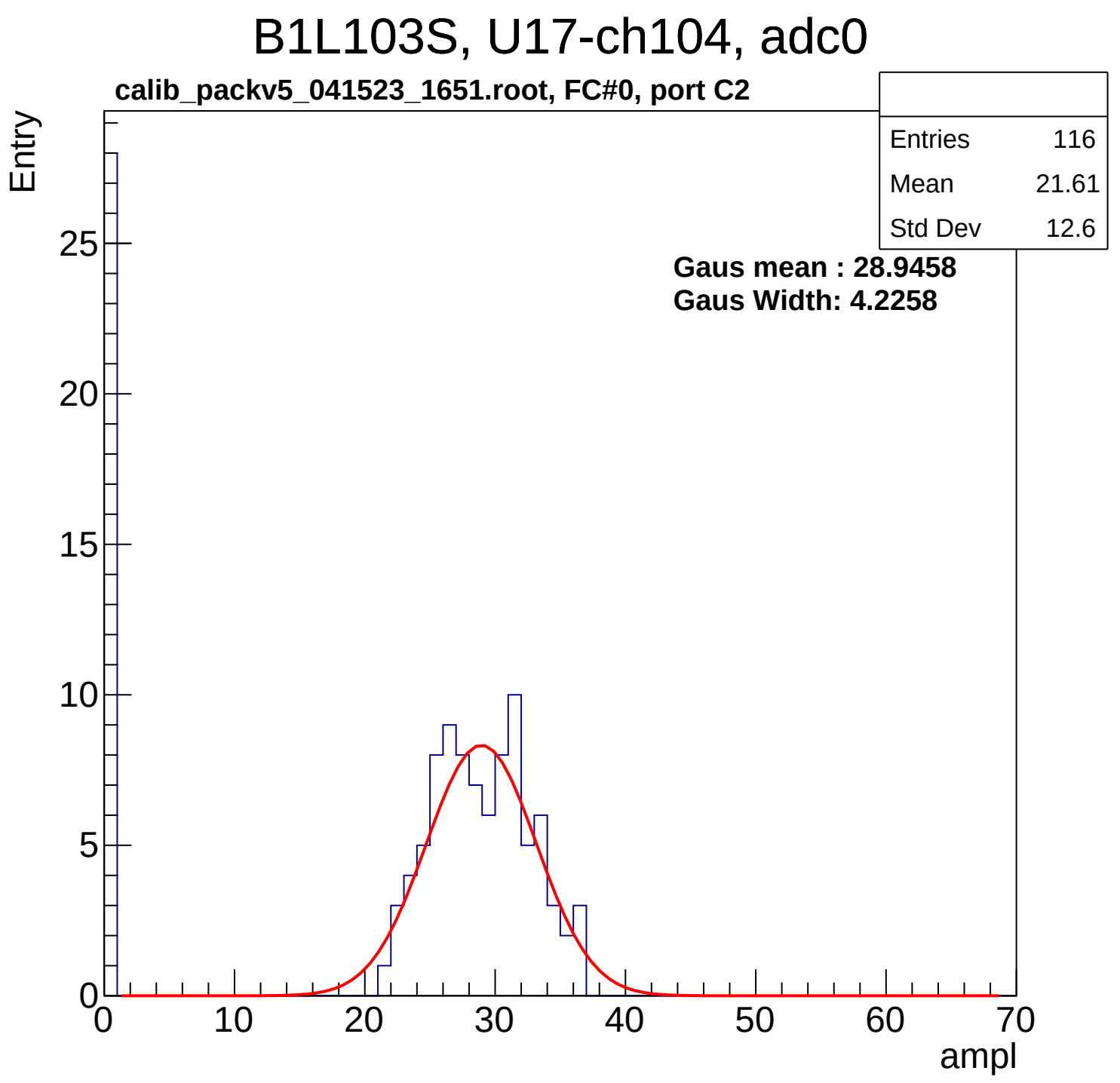

B1L103S, U17-ch103, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 44.37
Std Dev 12.94
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

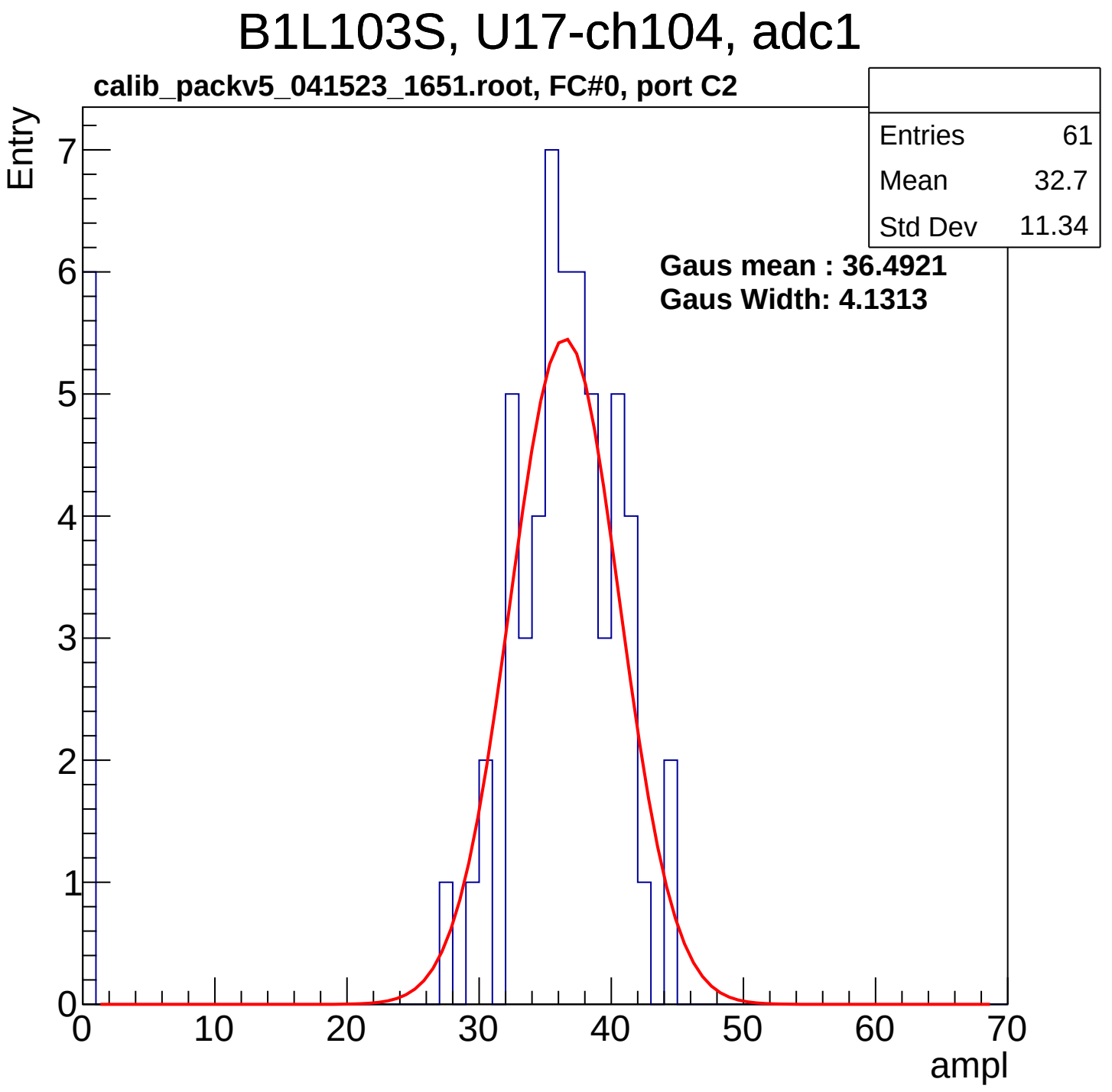

B1L103S, U17-ch103, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 53.56
Std Dev 3.453
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

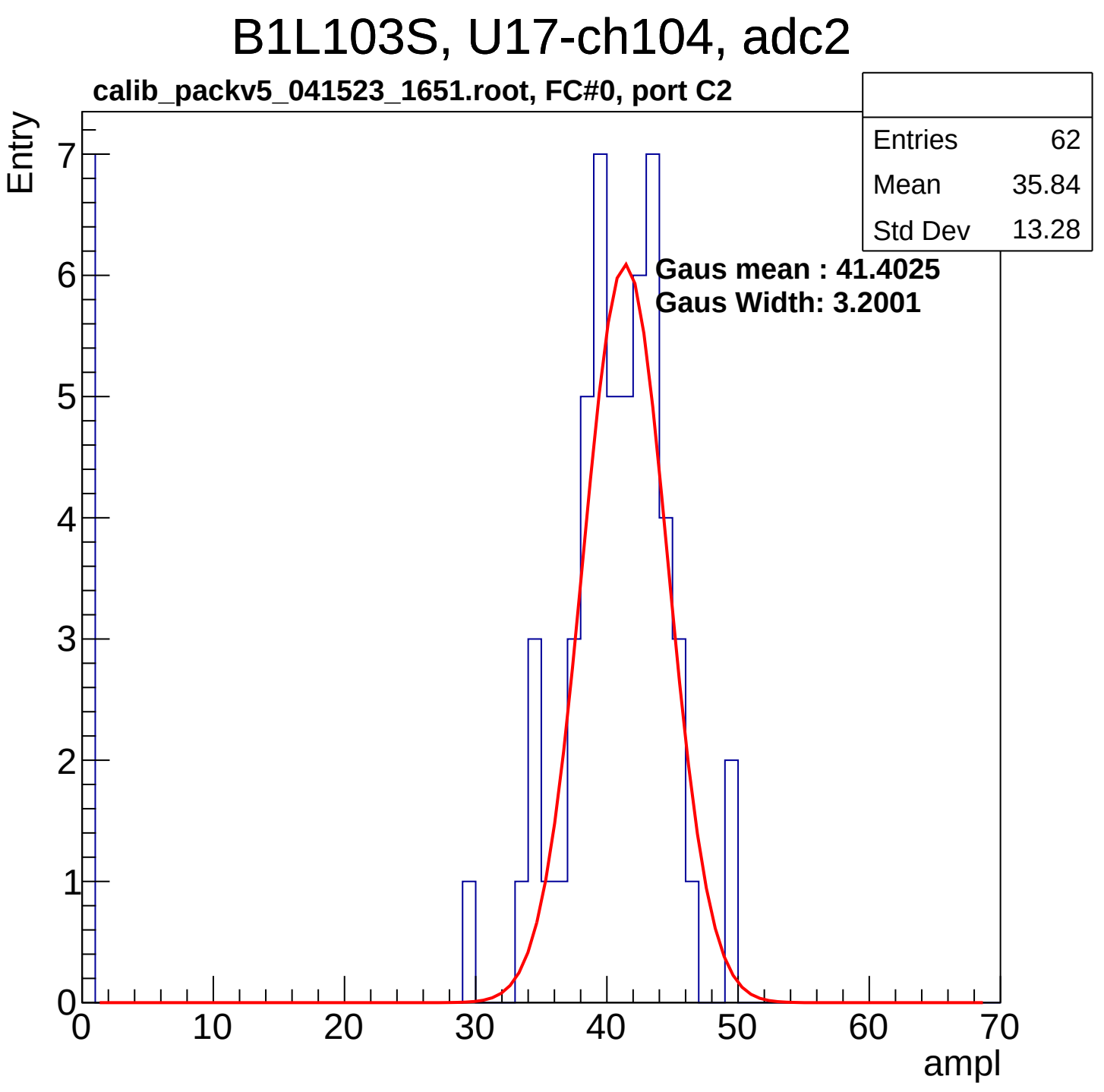

B1L103S, U17-ch103, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 59.16
Std Dev 2.648
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

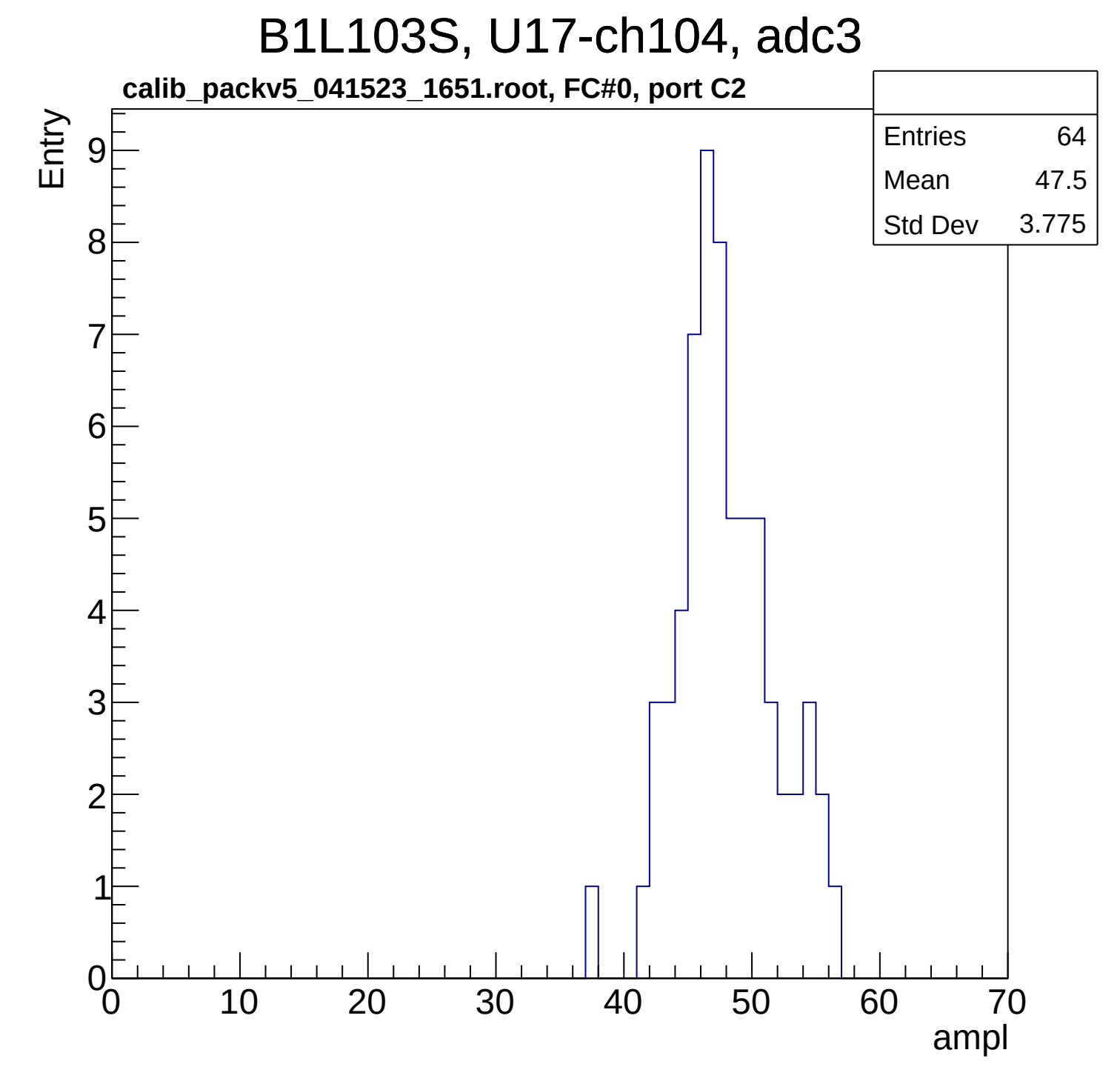

B1L103S, U17-ch103, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.25
Std Dev 14.94
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

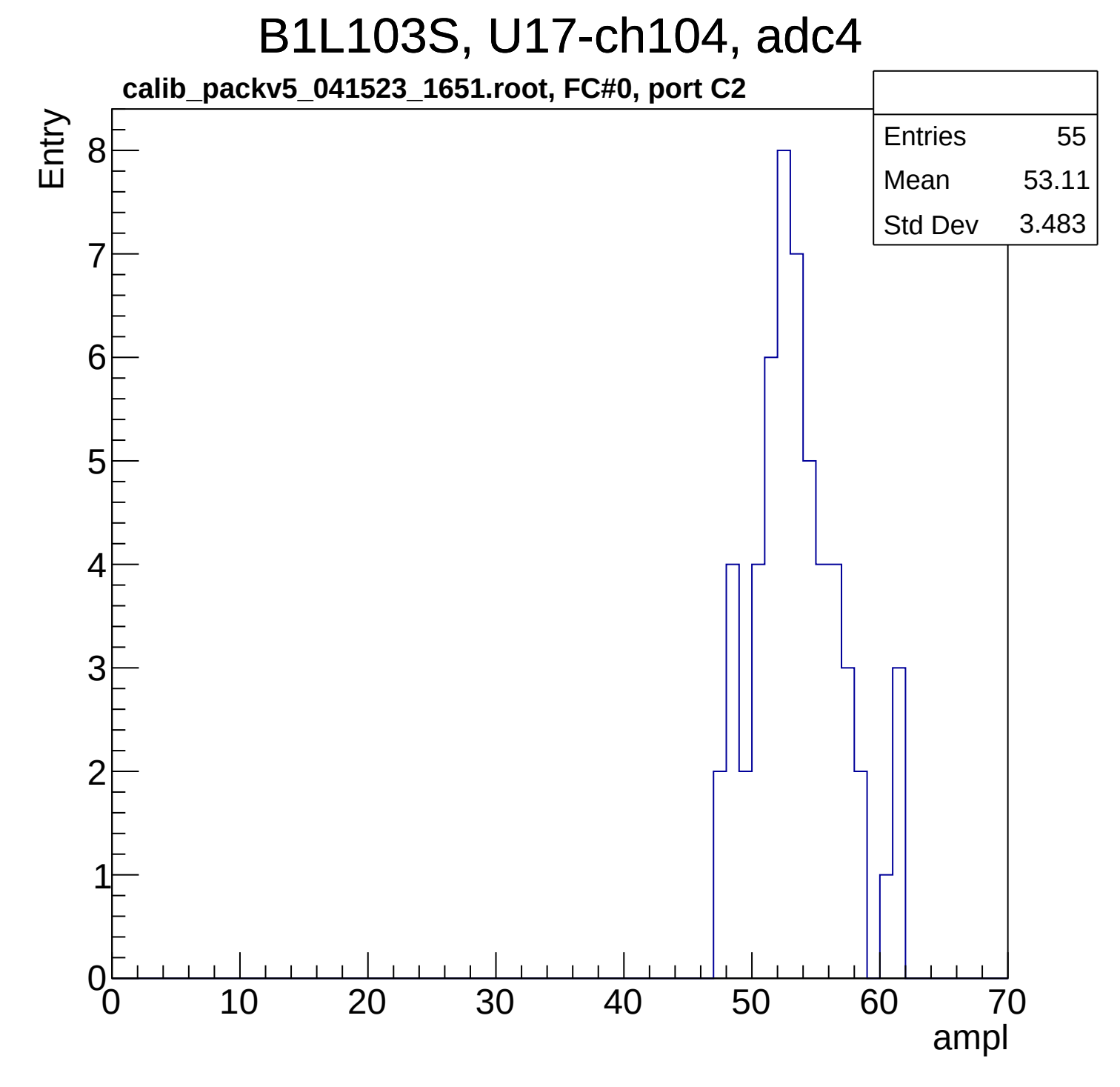

B1L103S, U17-ch103, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0.8333
Std Dev 3.436
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

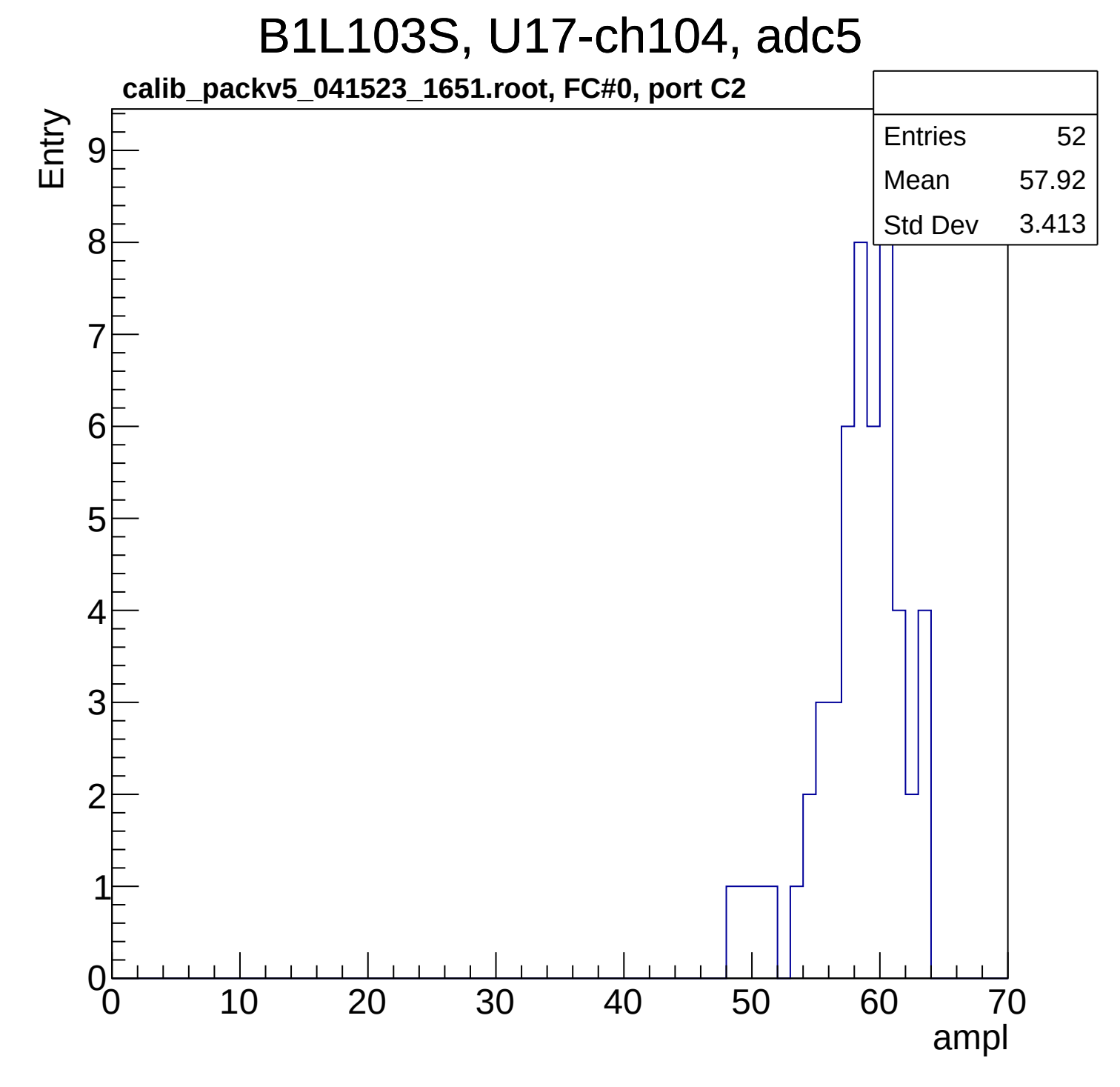

B1L103S, U17-ch104, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 116
Mean 21.61
Std Dev 12.6
Gaus mean : 28.9458
Gaus Width: 4.2258
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70

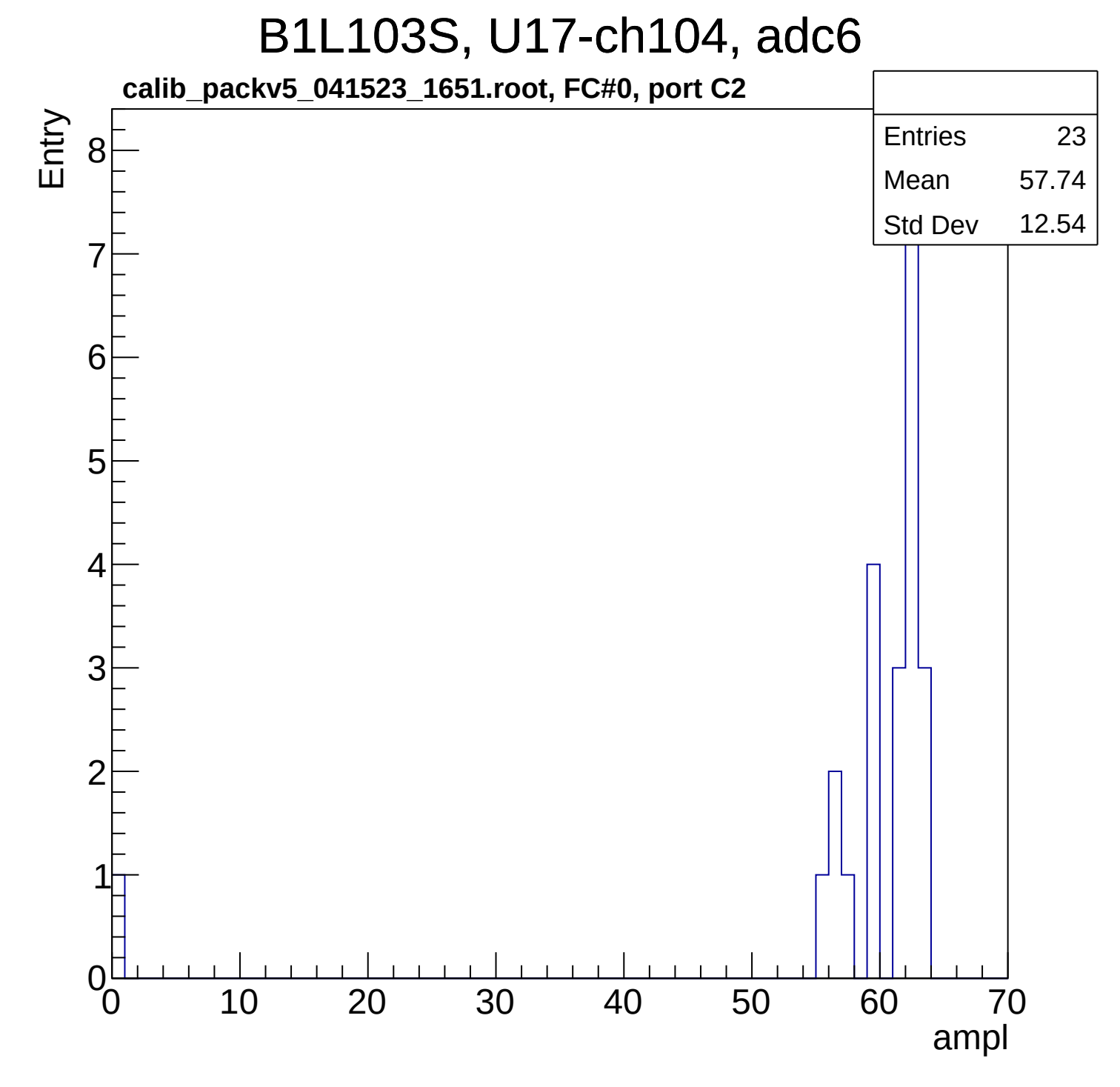

B1L103S, U17-ch104, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 32.7
Std Dev 11.34
Gaus mean : 36.4921
Gaus Width: 4.1313
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

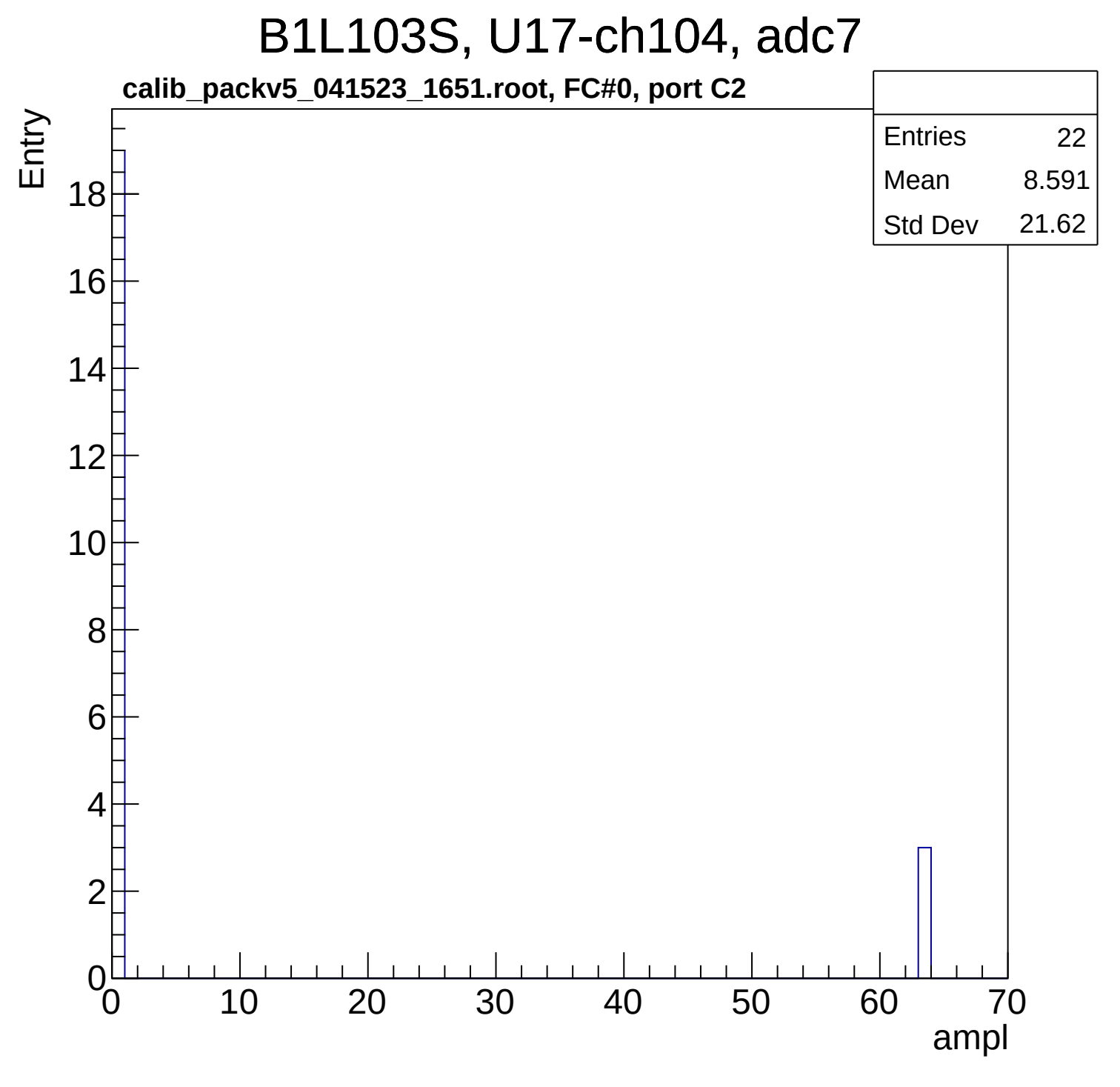

B1L103S, U17-ch104, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 35.84
Std Dev 13.28
Gaus mean : 41.4025
Gaus Width: 3.2001
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

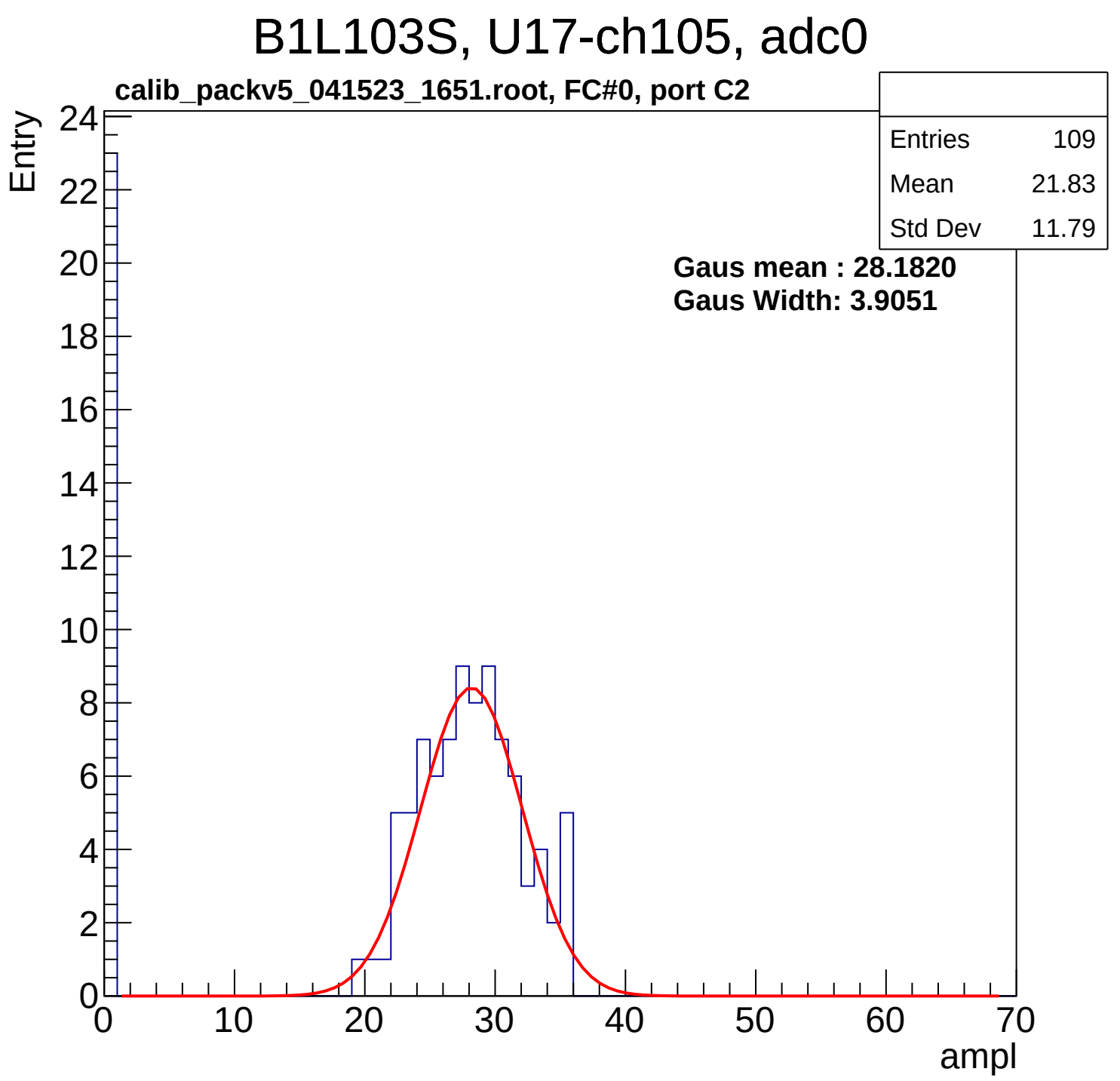

B1L103S, U17-ch104, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 47.5
Std Dev 3.775
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

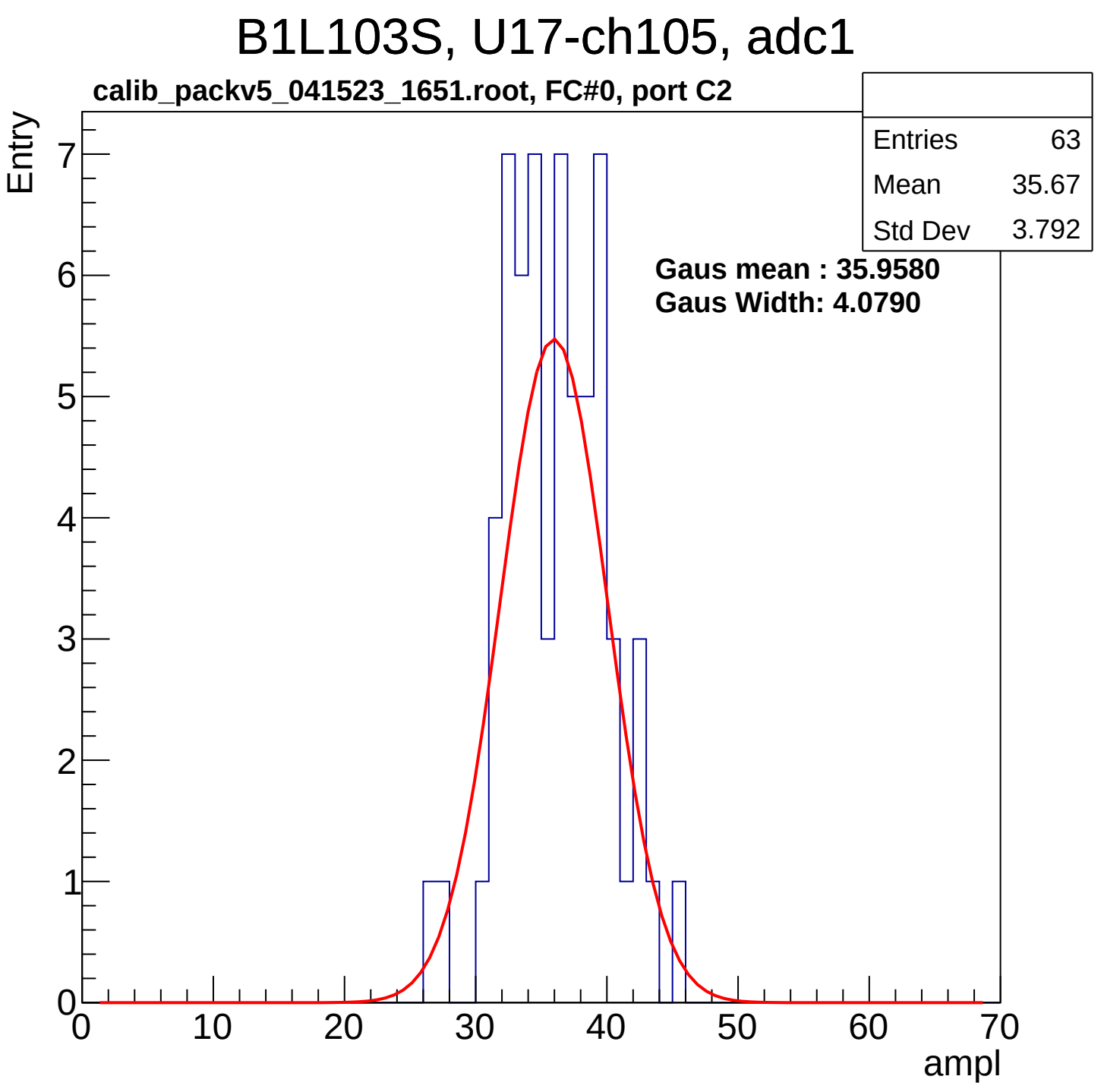

B1L103S, U17-ch104, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 53.11
Std Dev 3.483
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

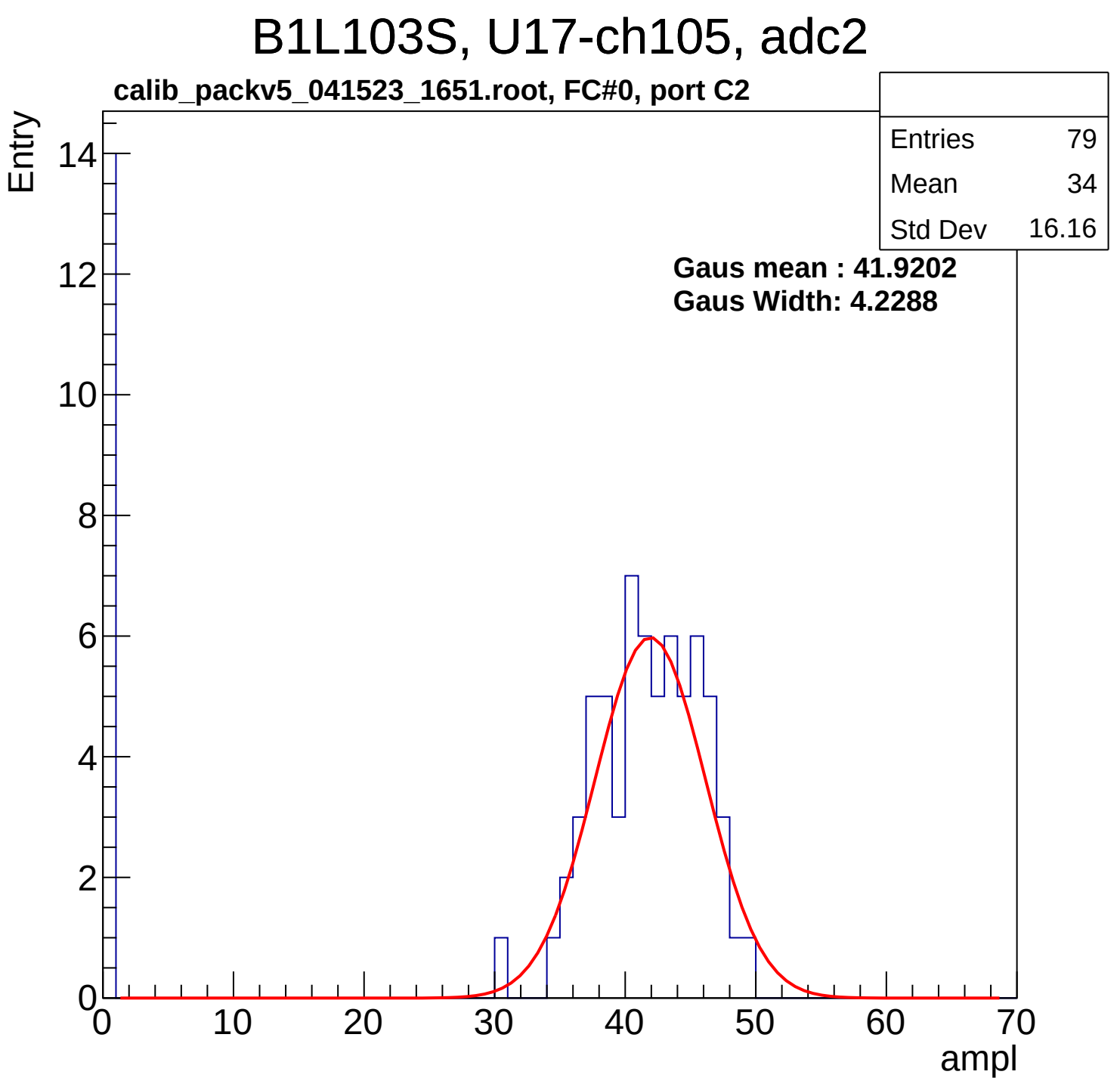

B1L103S, U17-ch104, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 57.92
Std Dev 3.413
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

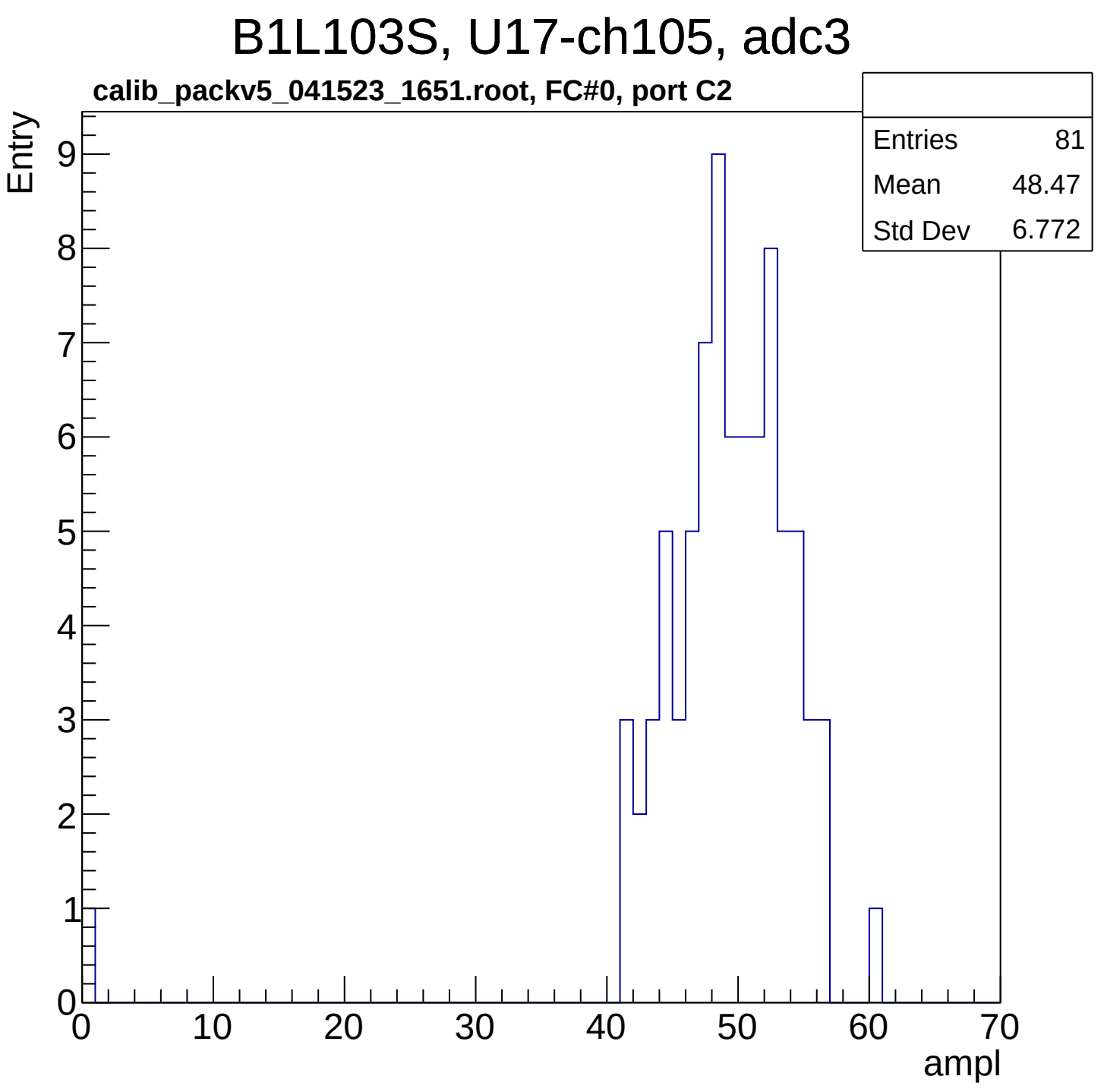

B1L103S, U17-ch104, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 57.74
Std Dev 12.54
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

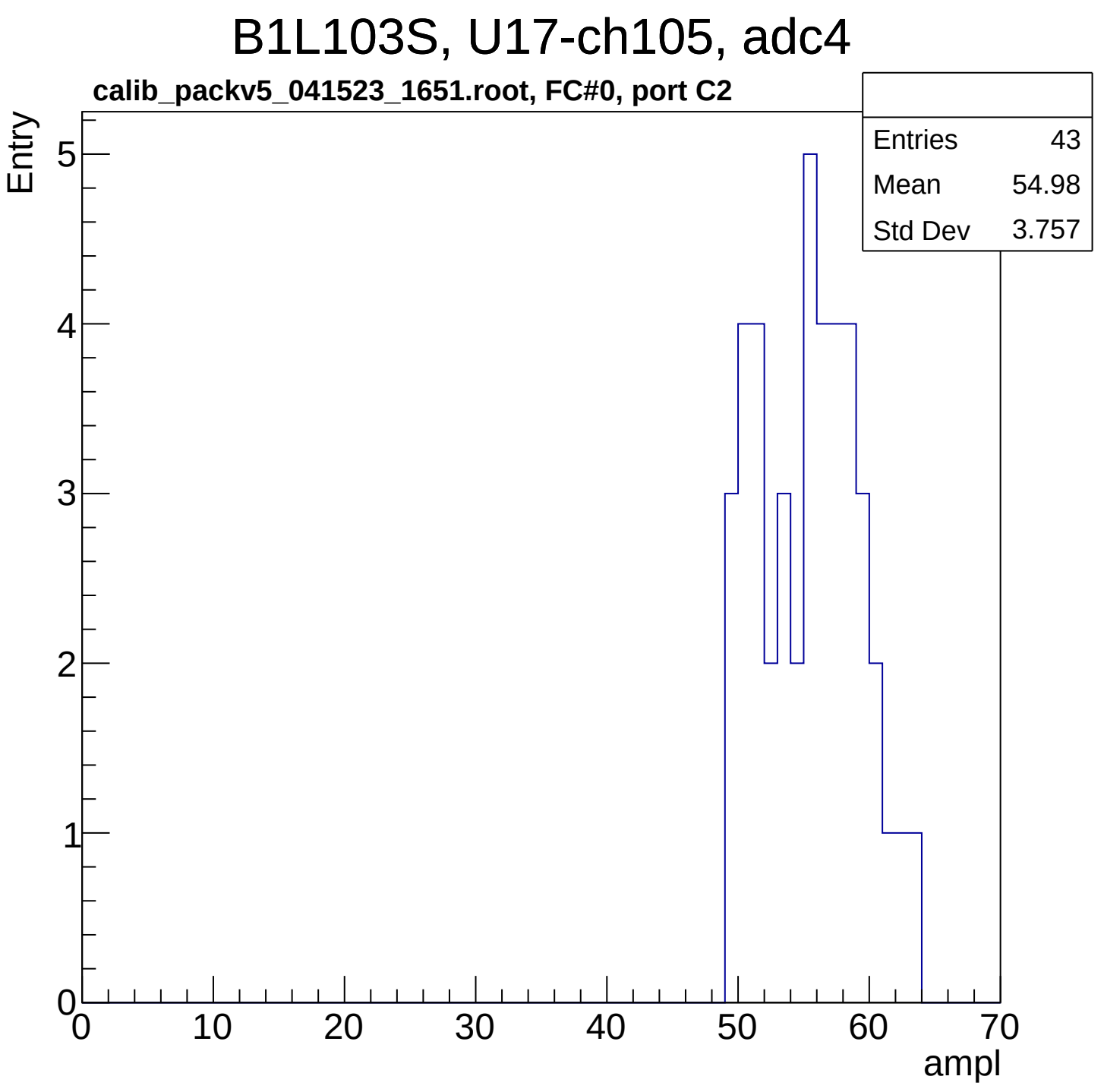

B1L103S, U17-ch104, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.591
Std Dev 21.62
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

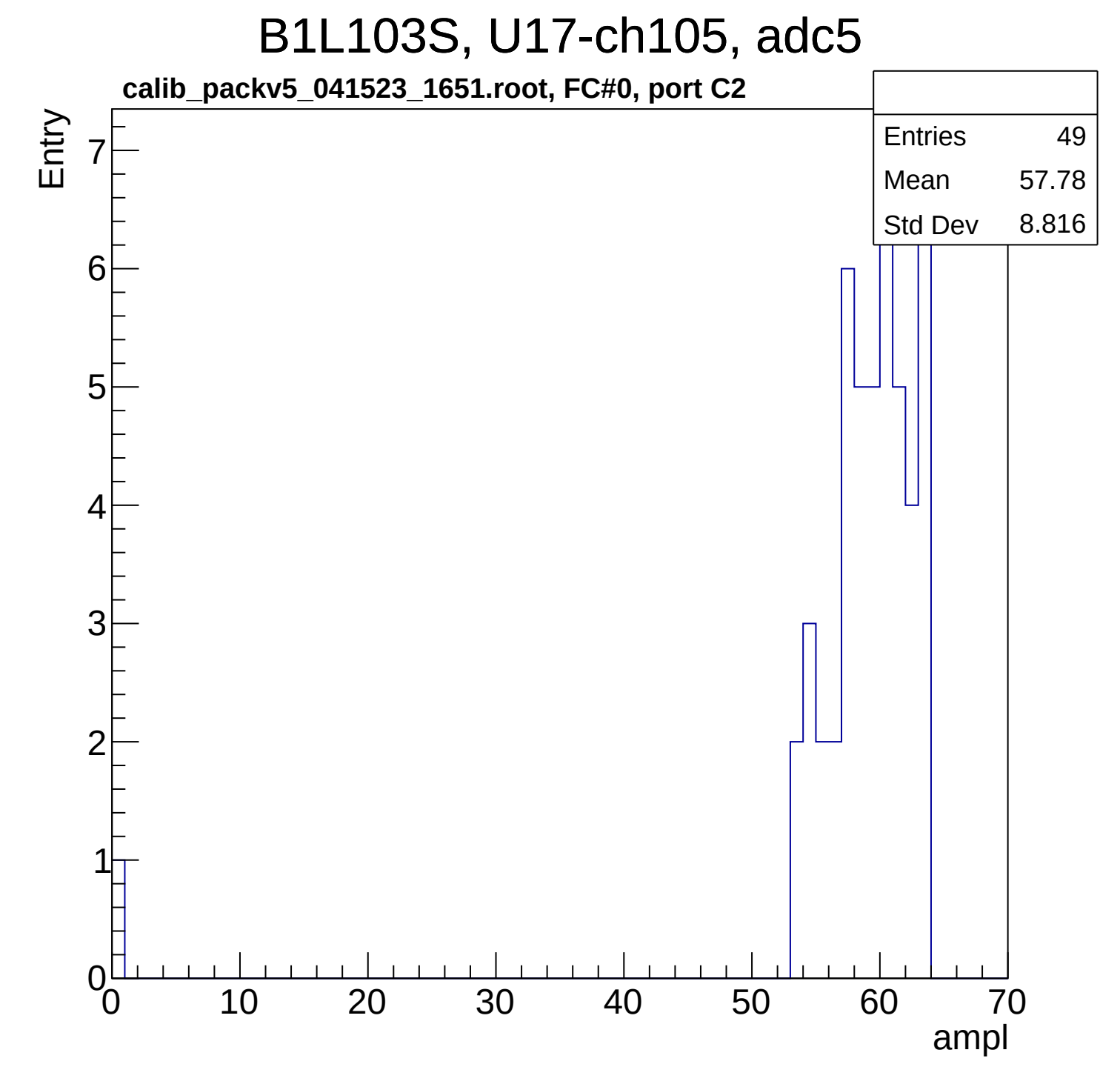

B1L103S, U17-ch105, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 109
Mean 21.83
Std Dev 11.79
Gaus mean : 28.1820
Gaus Width: 3.9051
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70

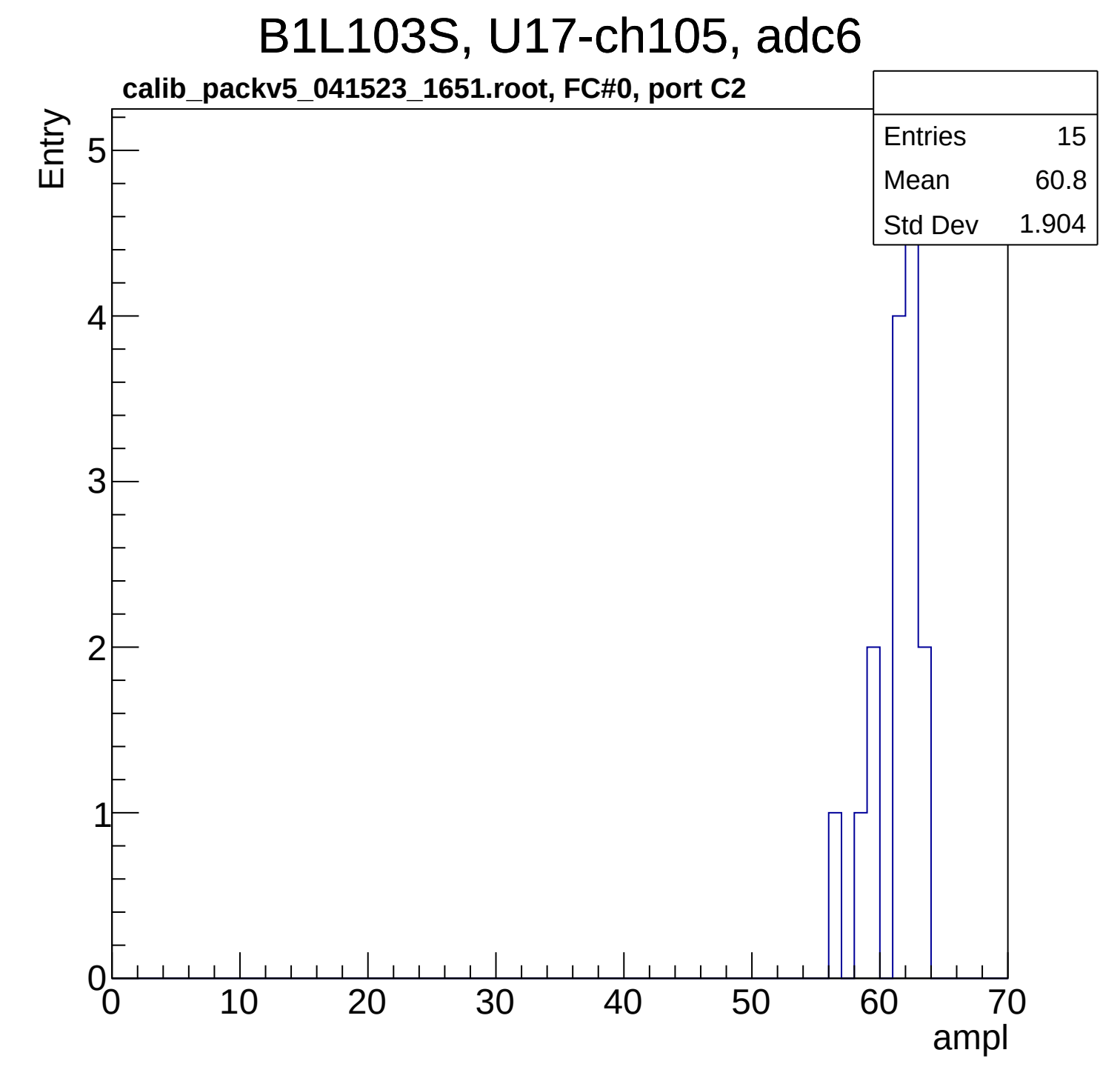

B1L103S, U17-ch105, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 35.67
Std Dev 3.792
Gaus mean : 35.9580
Gaus Width: 4.0790
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

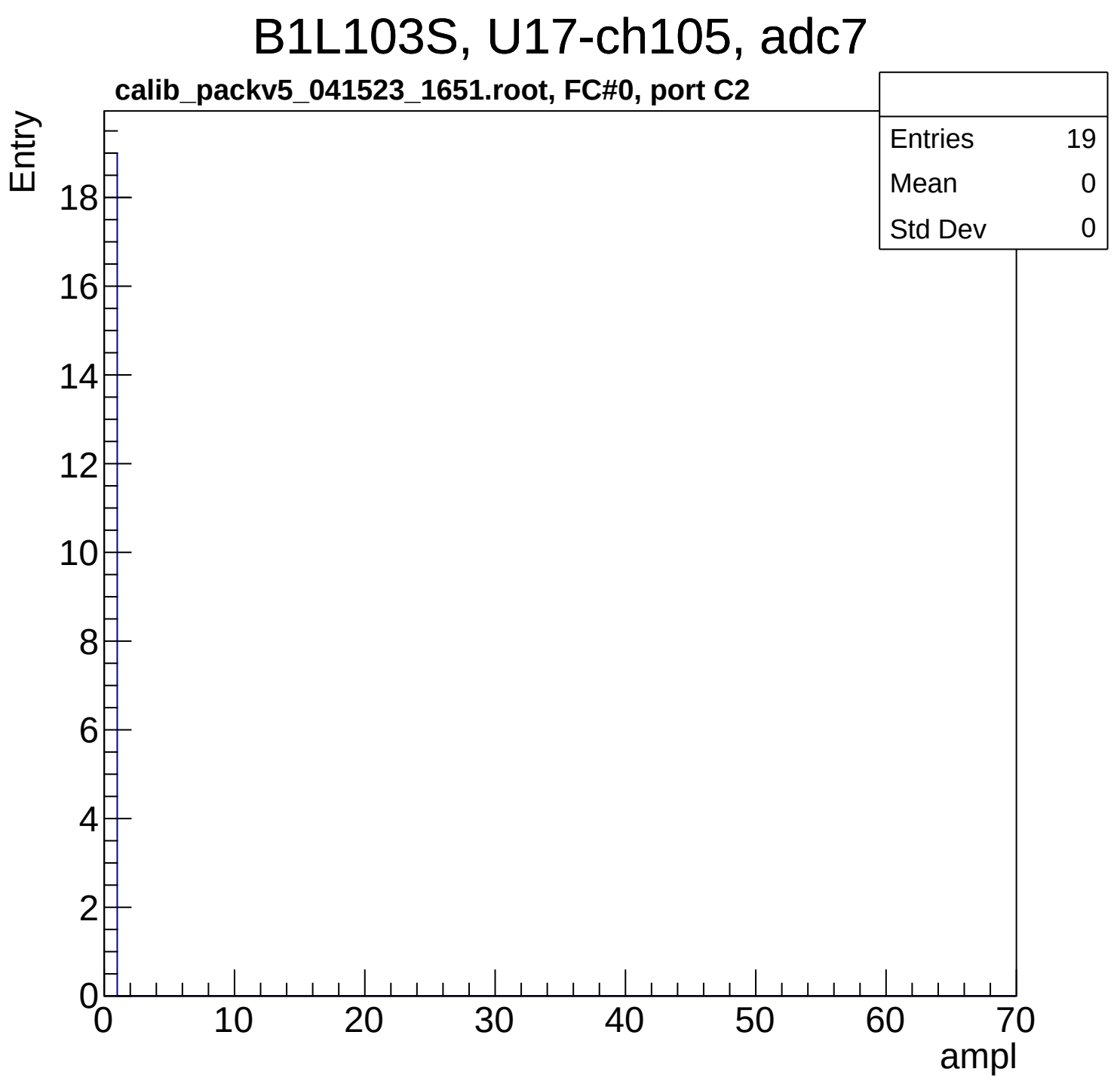

B1L103S, U17-ch105, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 34
Std Dev 16.16
Gaus mean : 41.9202
Gaus Width: 4.2288
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

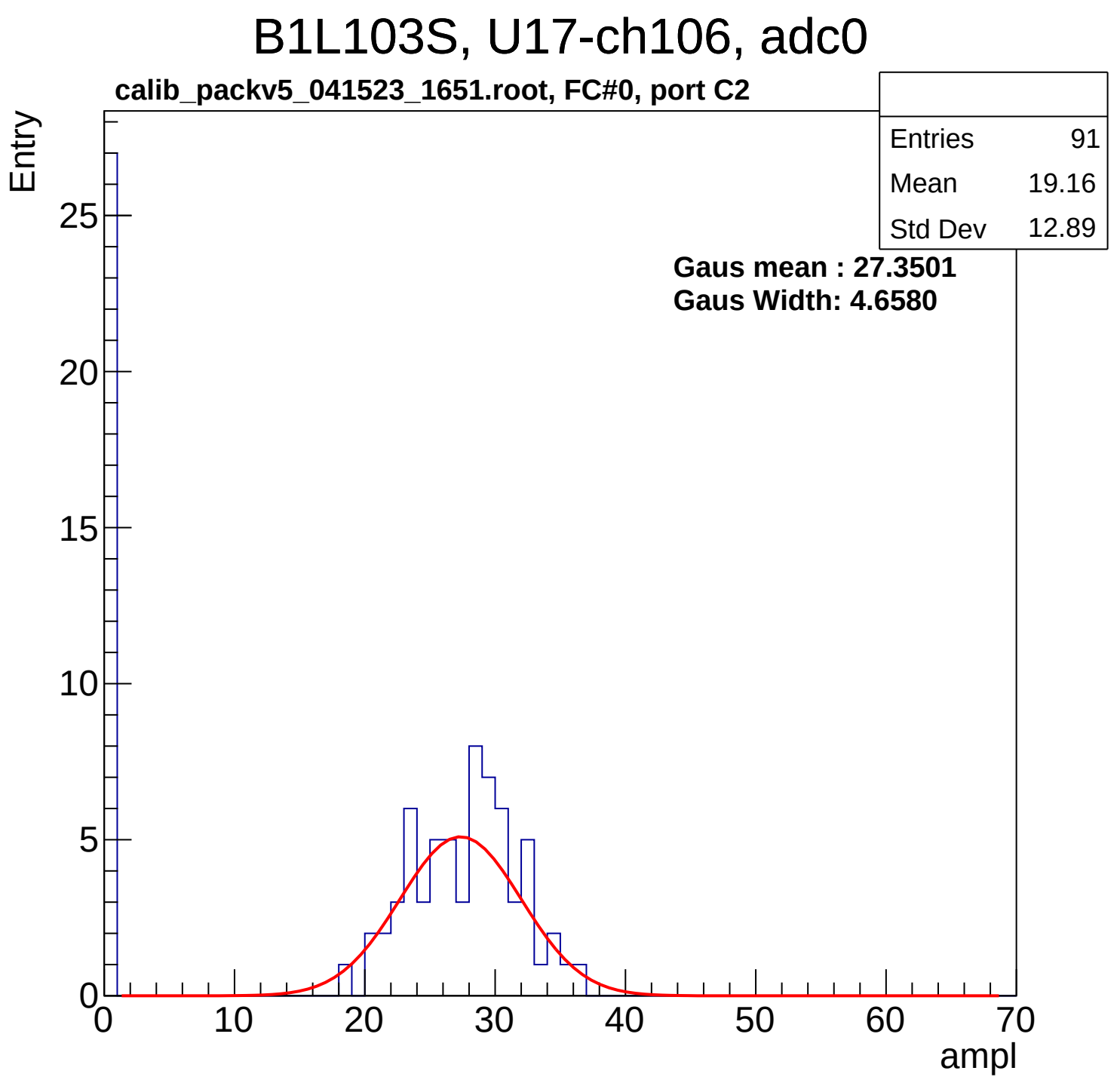

B1L103S, U17-ch105, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 48.47
Std Dev 6.772
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

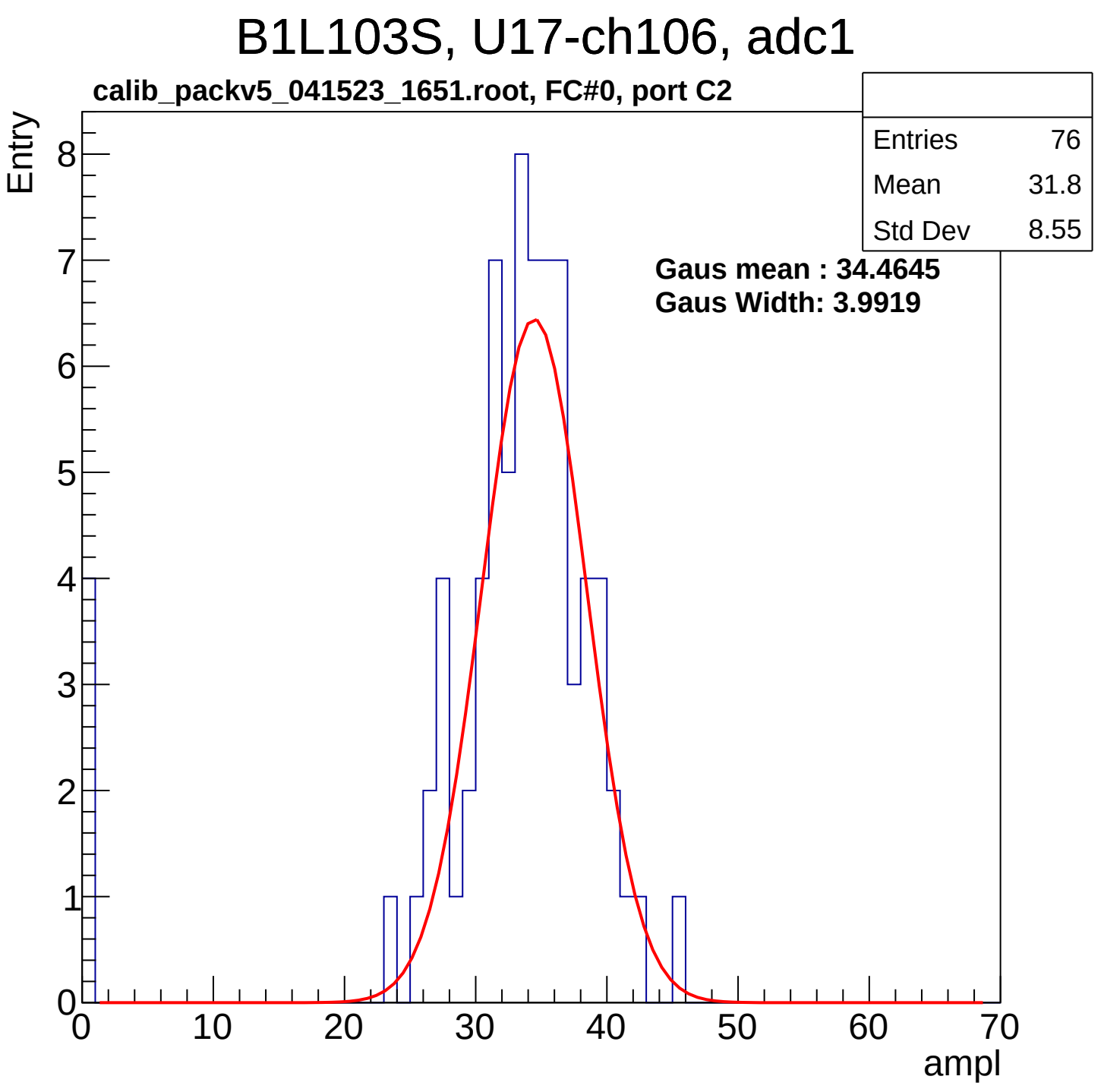

B1L103S, U17-ch105, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 54.98
Std Dev 3.757
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

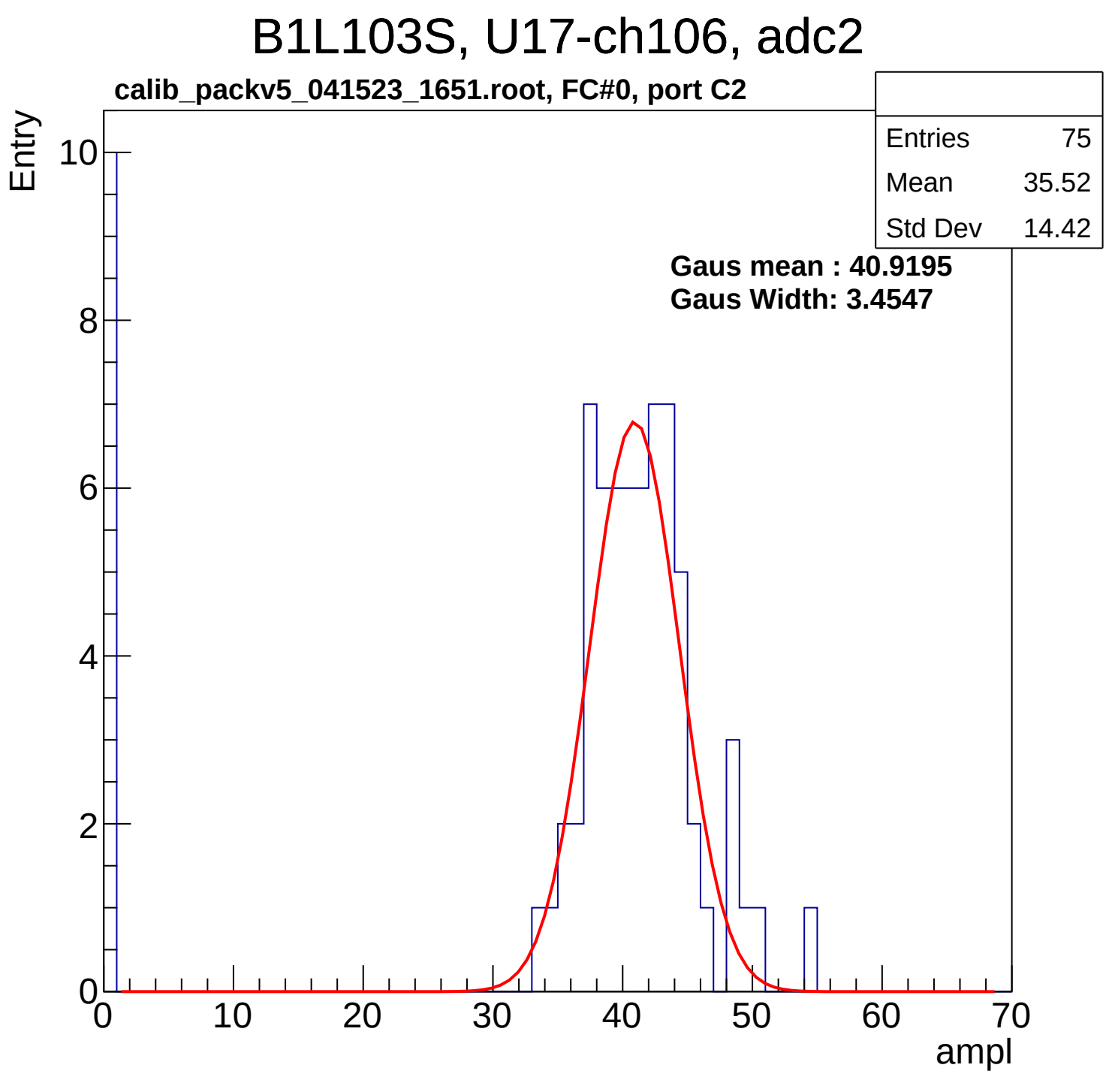

B1L103S, U17-ch105, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 57.78
Std Dev 8.816
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

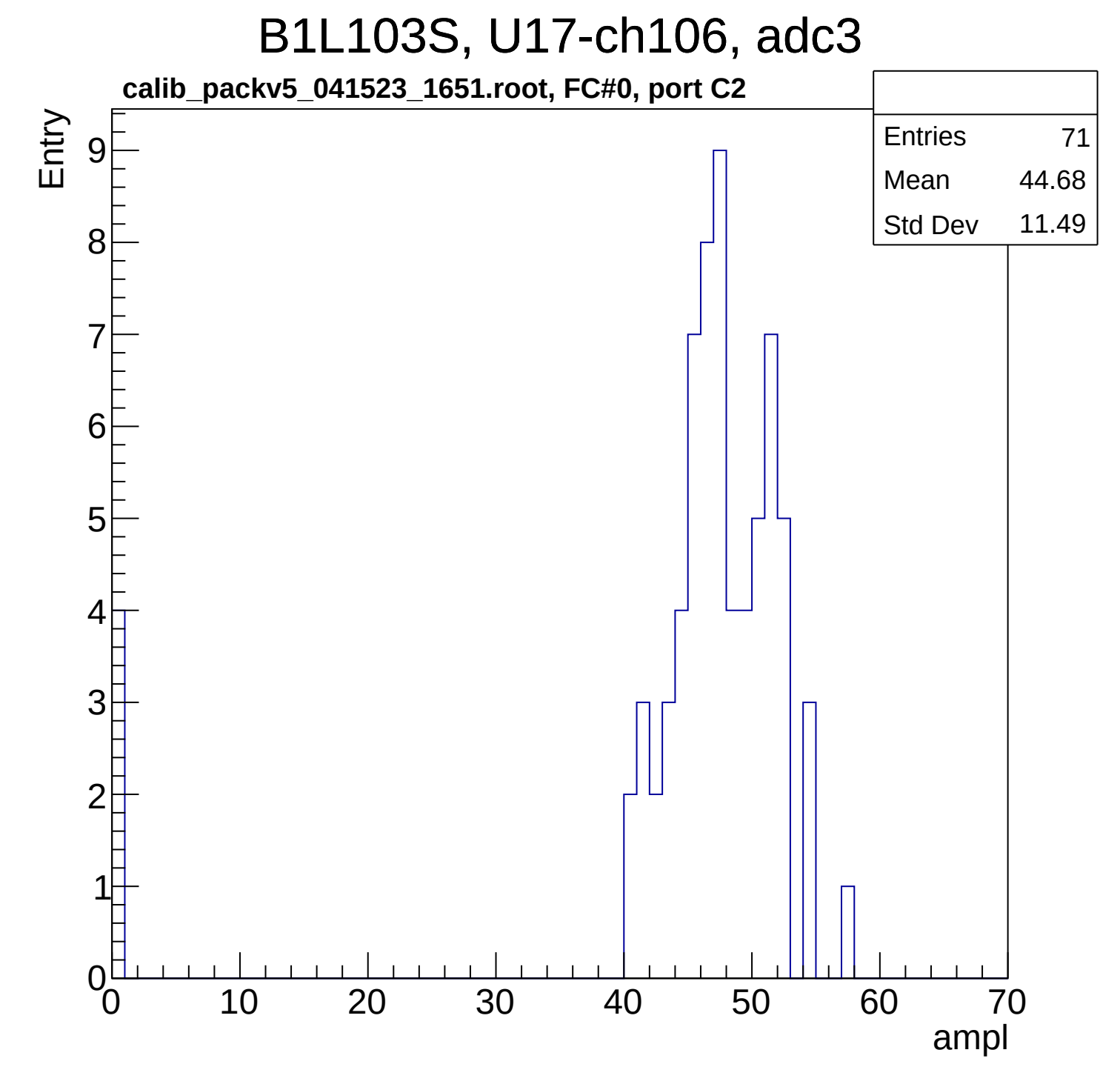

B1L103S, U17-ch105, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 60.8
Std Dev 1.904
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

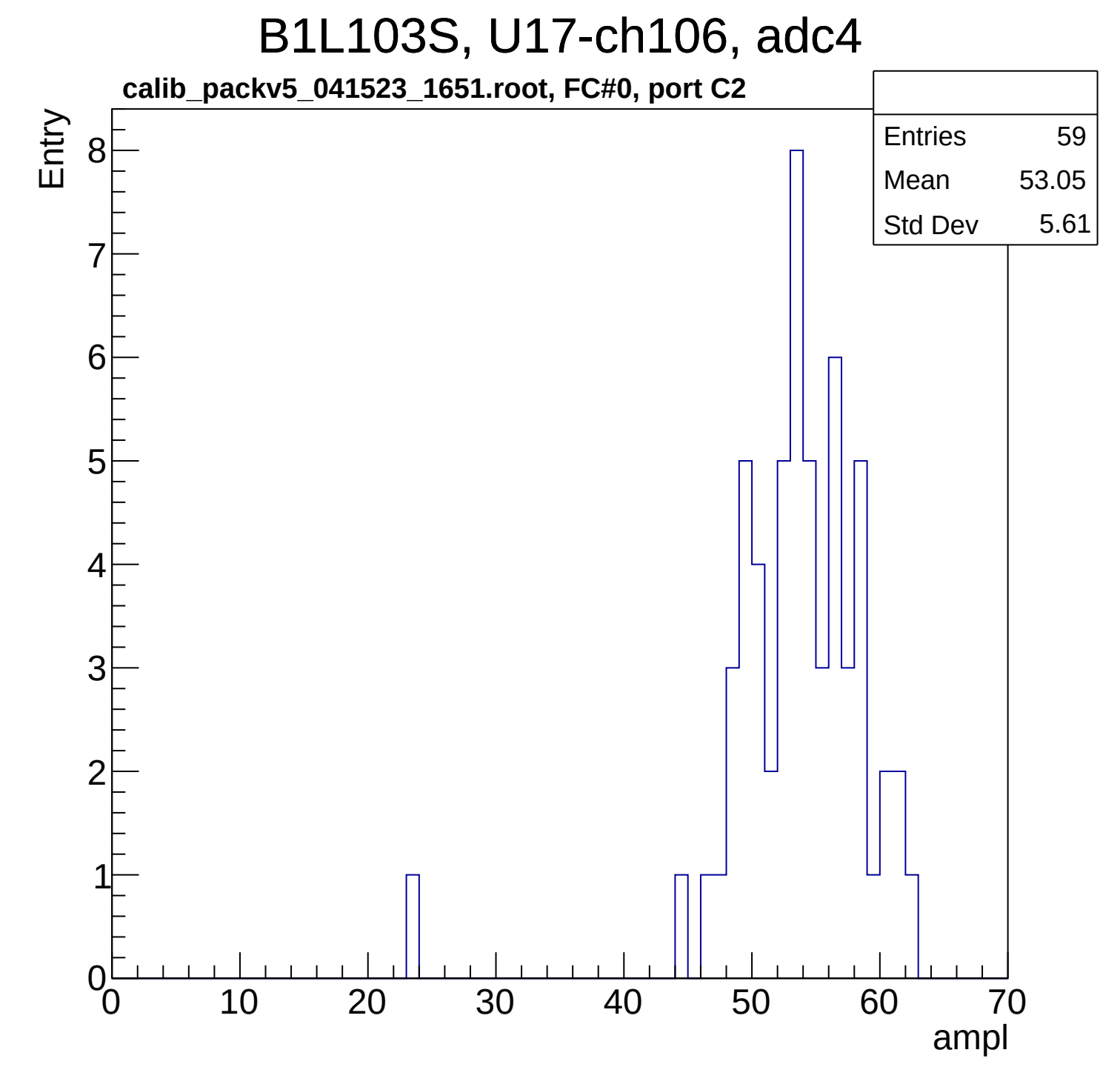

B1L103S, U17-ch105, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

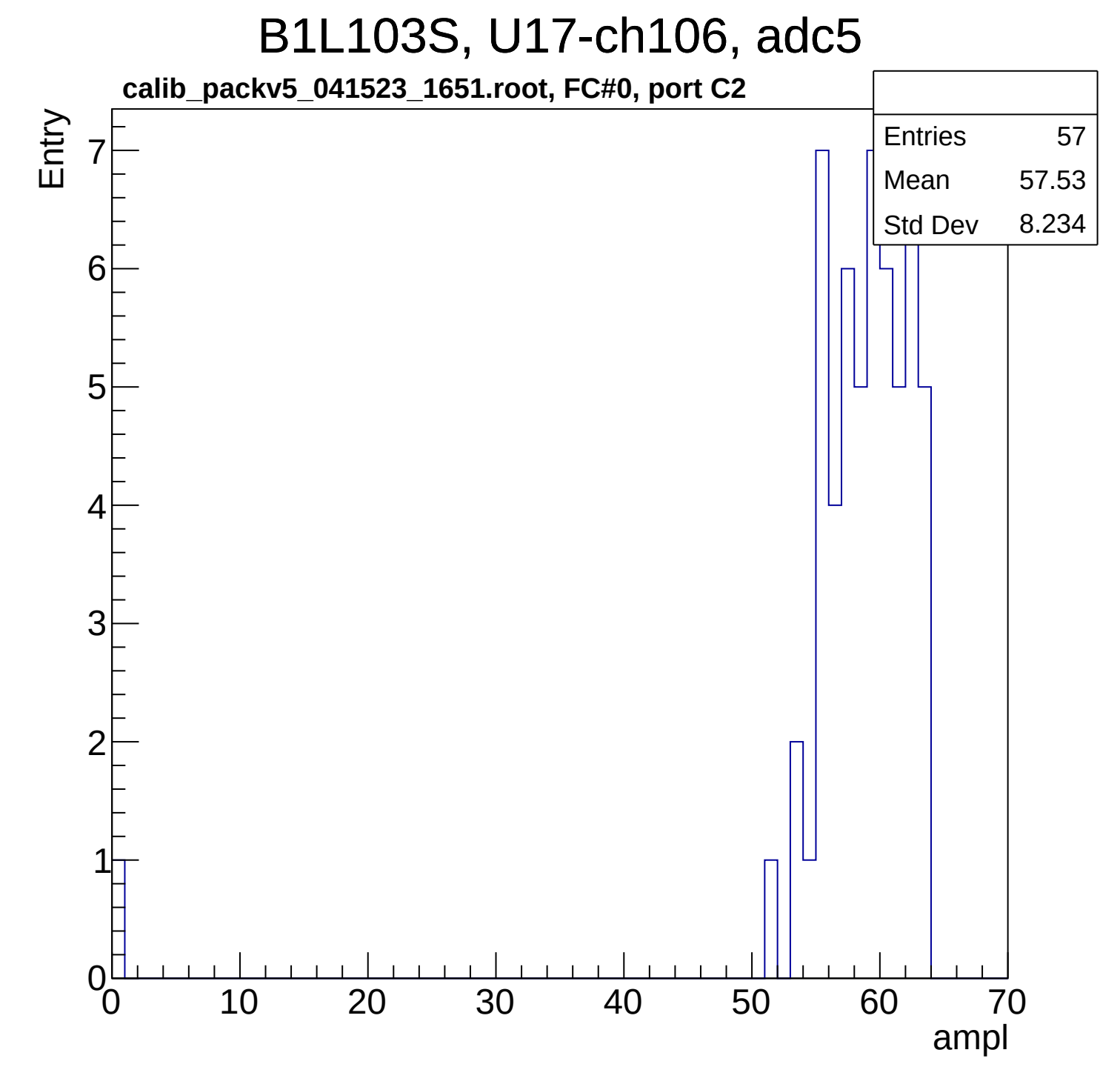

B1L103S, U17-ch106, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 19.16
Std Dev 12.89
Gaus mean : 27.3501
Gaus Width: 4.6580
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70

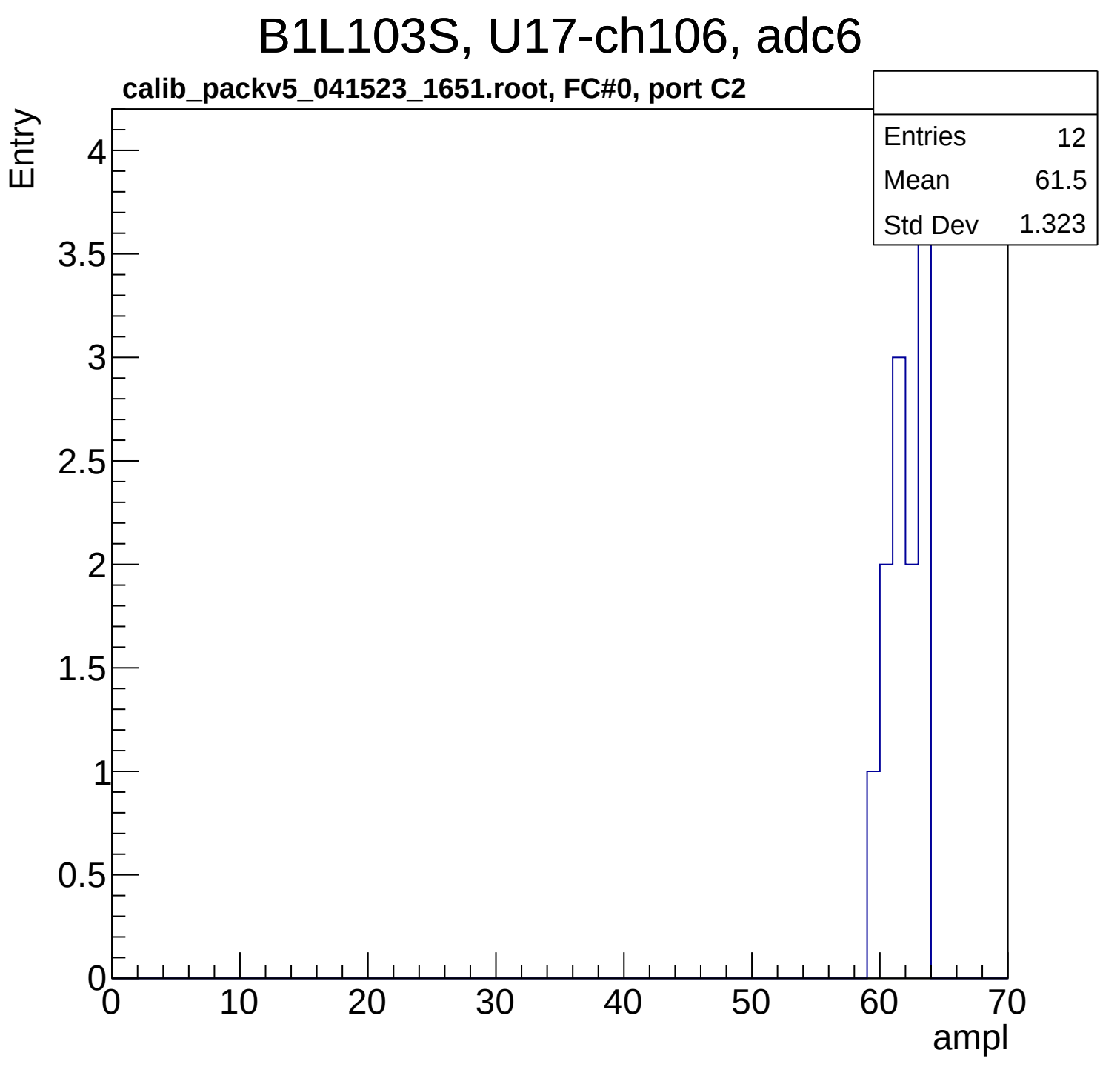

B1L103S, U17-ch106, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 31.8
Std Dev 8.55
Gaus mean : 34.4645
Gaus Width: 3.9919
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

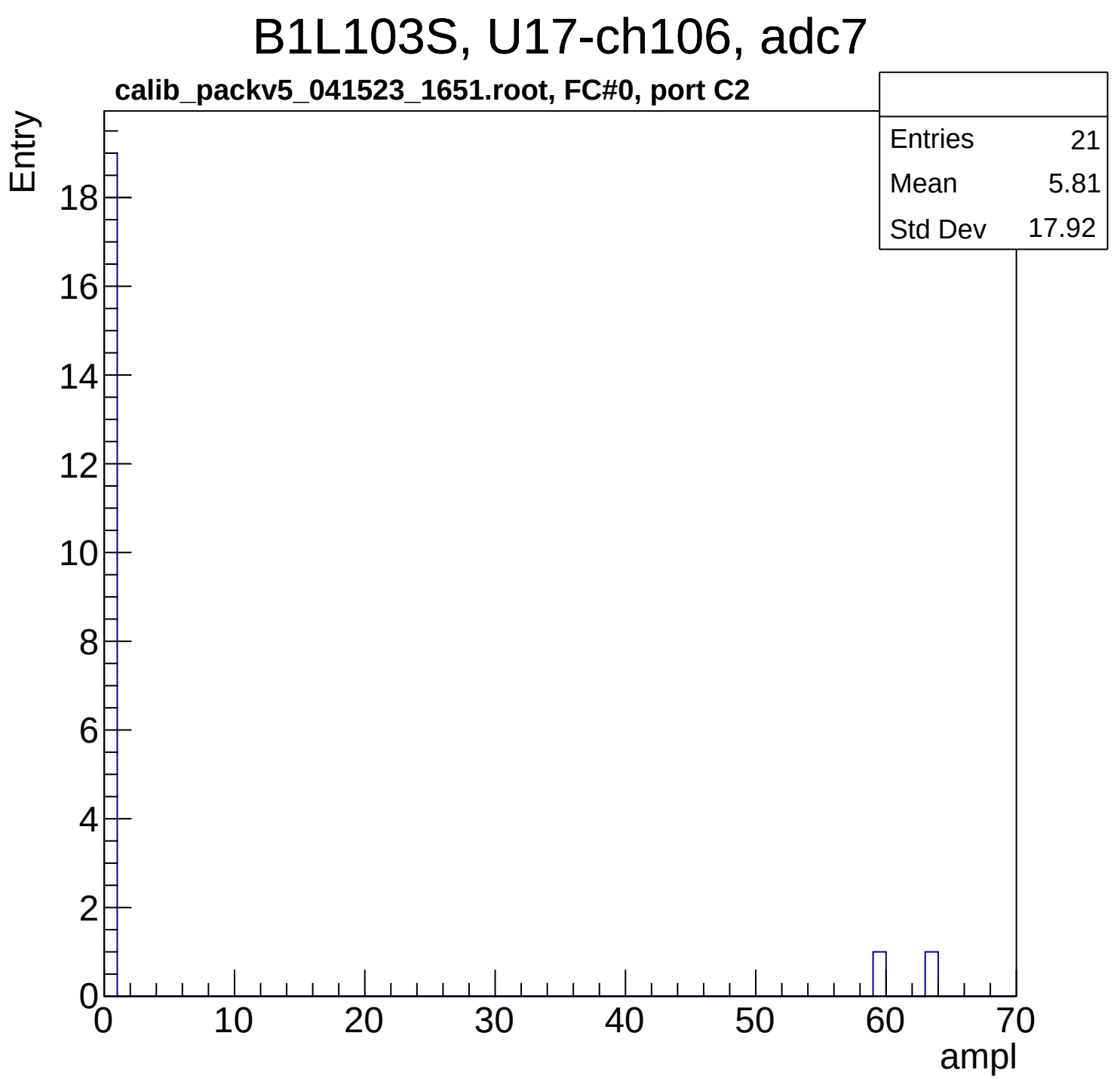

B1L103S, U17-ch106, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 35.52
Std Dev 14.42
Gaus mean : 40.9195
Gaus Width: 3.4547
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

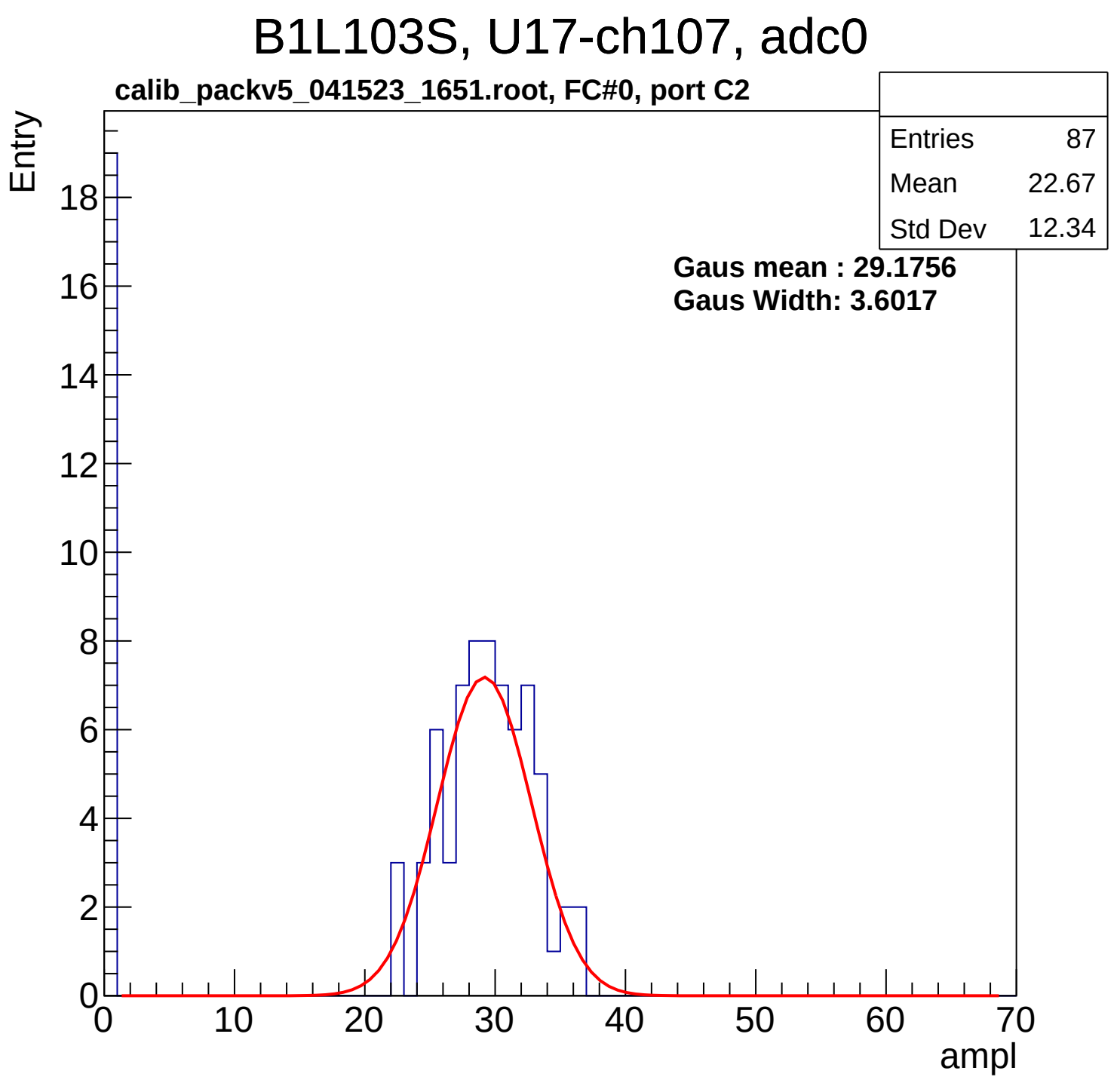

B1L103S, U17-ch106, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 44.68
Std Dev 11.49
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

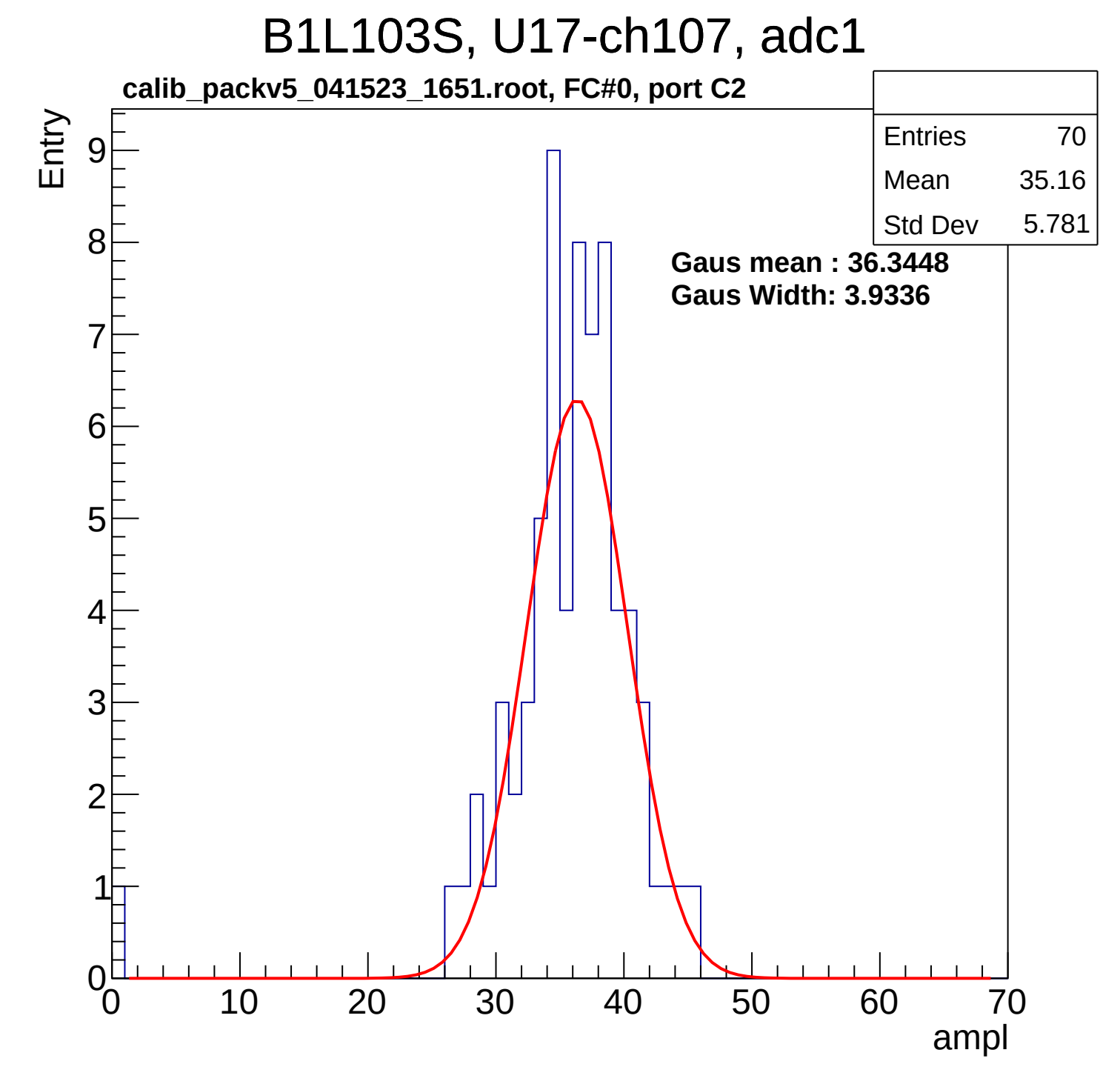

B1L103S, U17-ch106, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 53.05
Std Dev 5.61
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

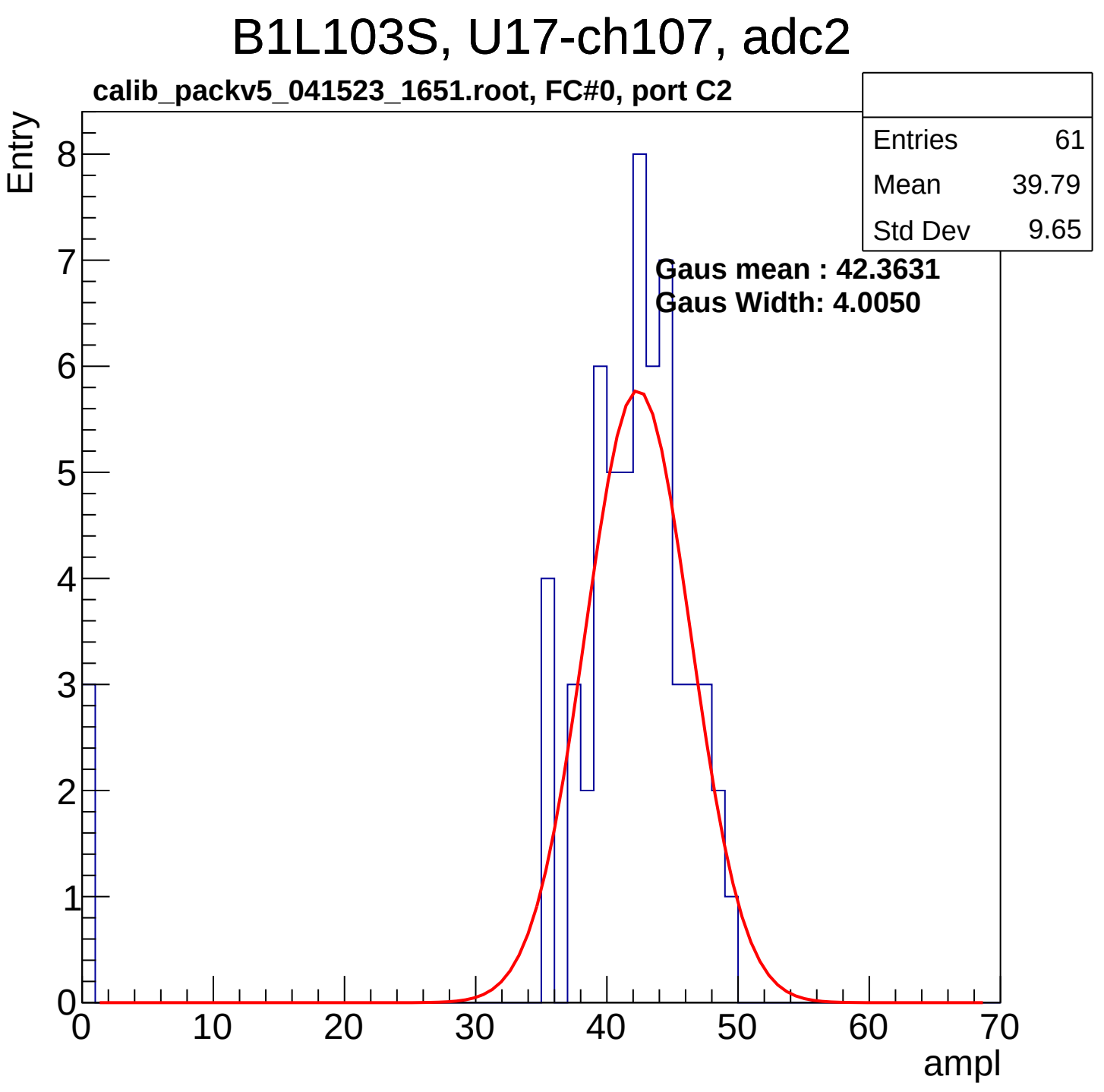

B1L103S, U17-ch106, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 57.53
Std Dev 8.234
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

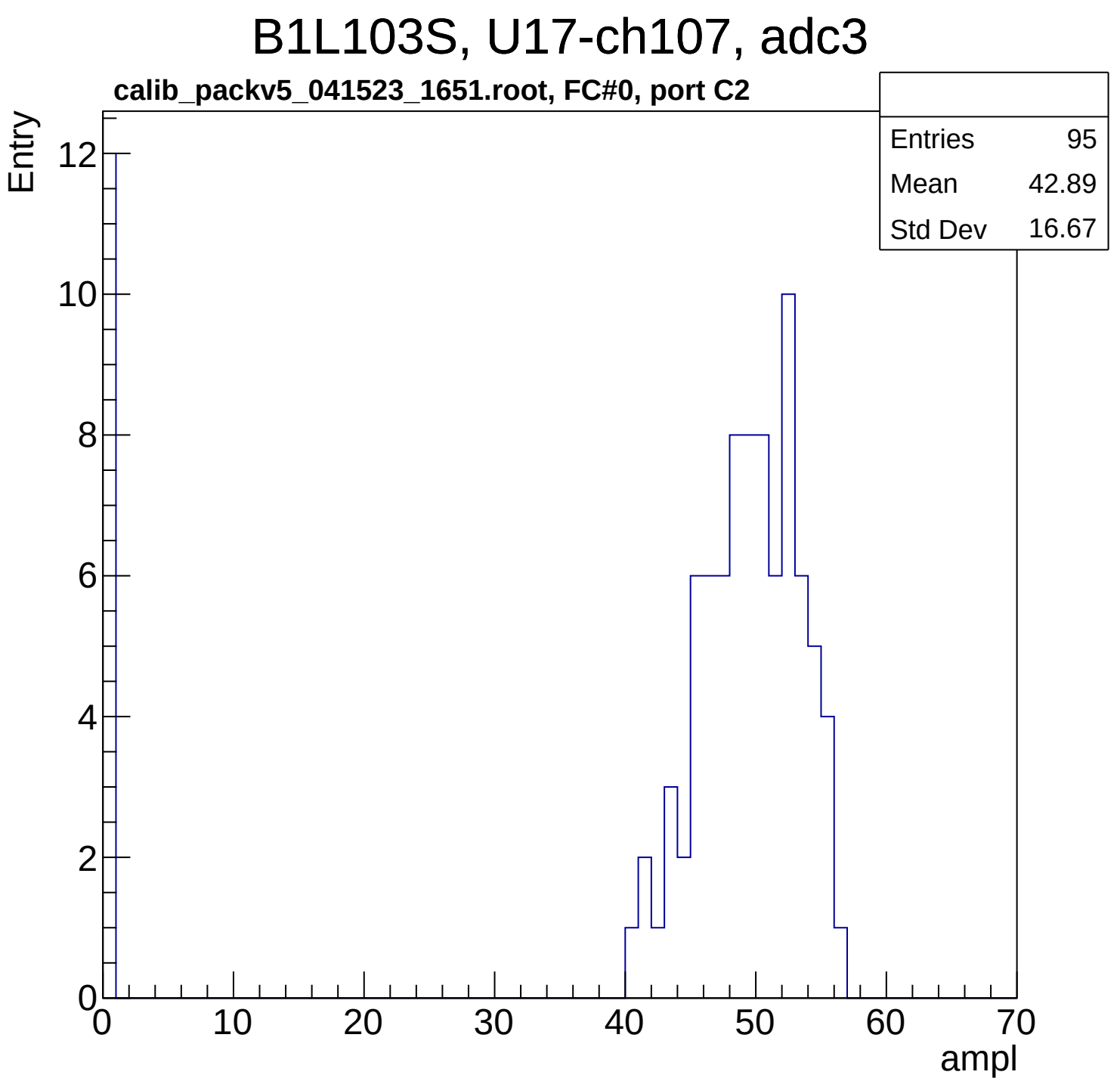

B1L103S, U17-ch106, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.5
Std Dev 1.323
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

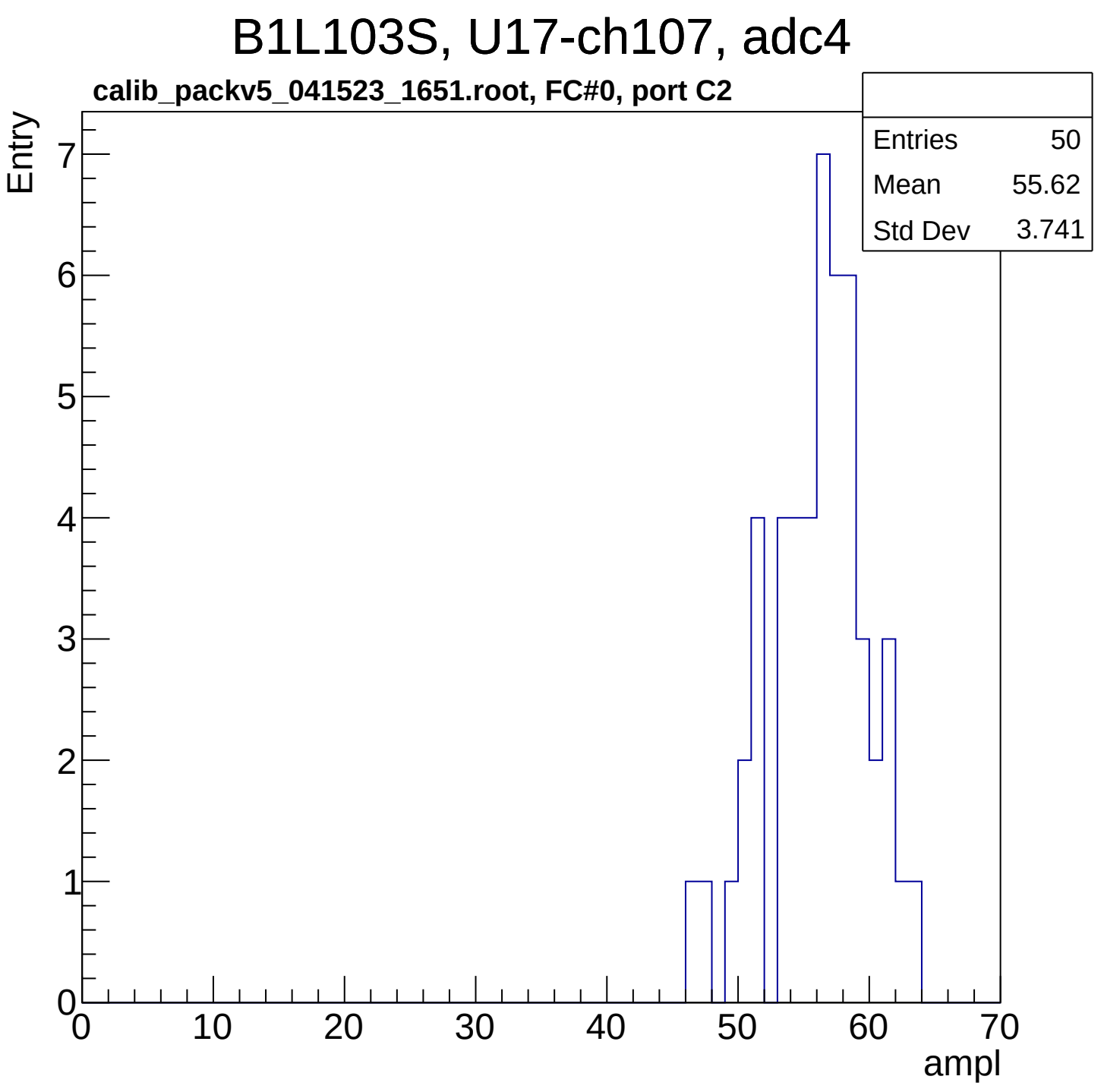

B1L103S, U17-ch106, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.81
Std Dev 17.92
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

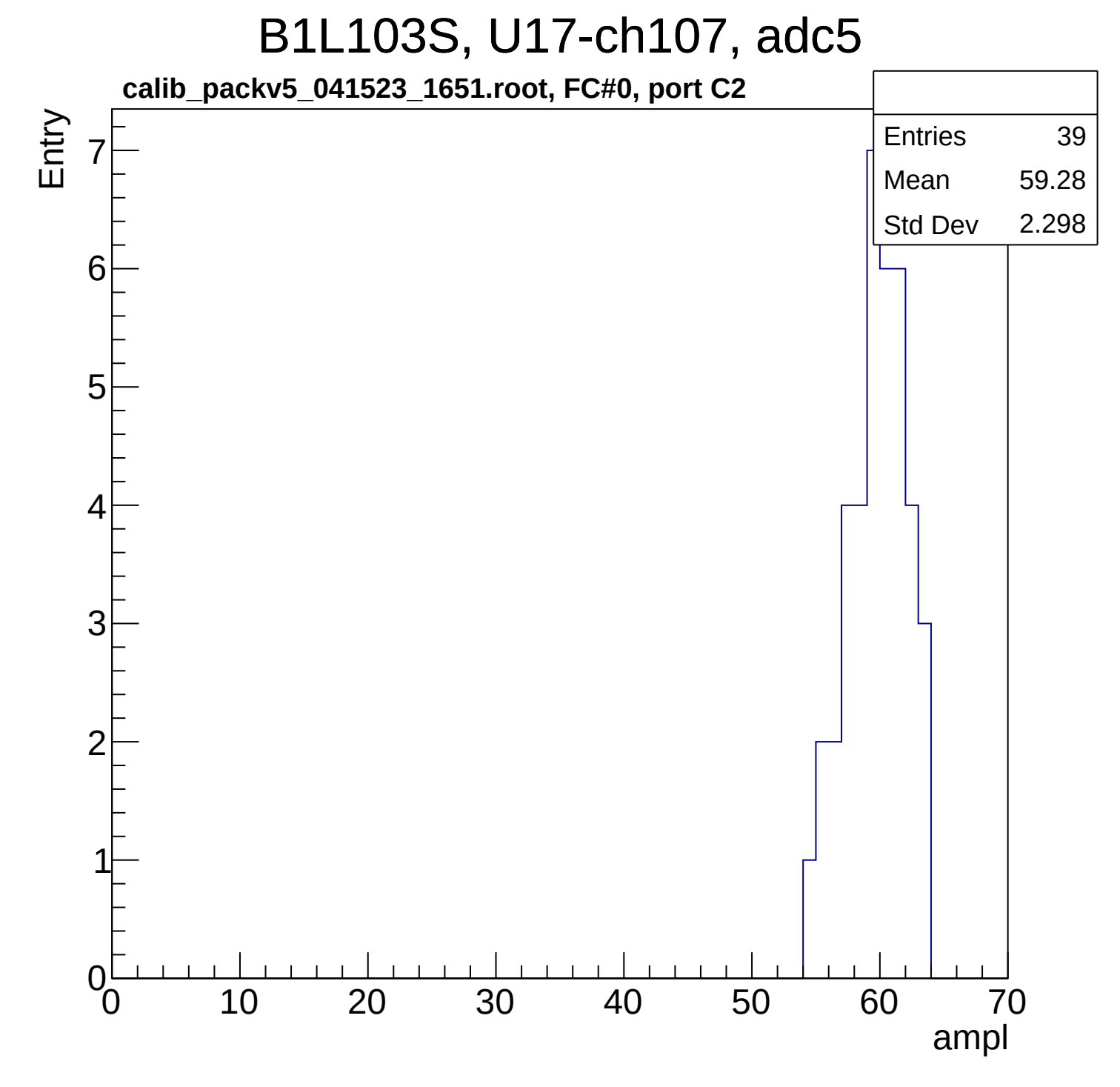

B1L103S, U17-ch107, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 22.67
Std Dev 12.34
Gaus mean : 29.1756
Gaus Width: 3.6017
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

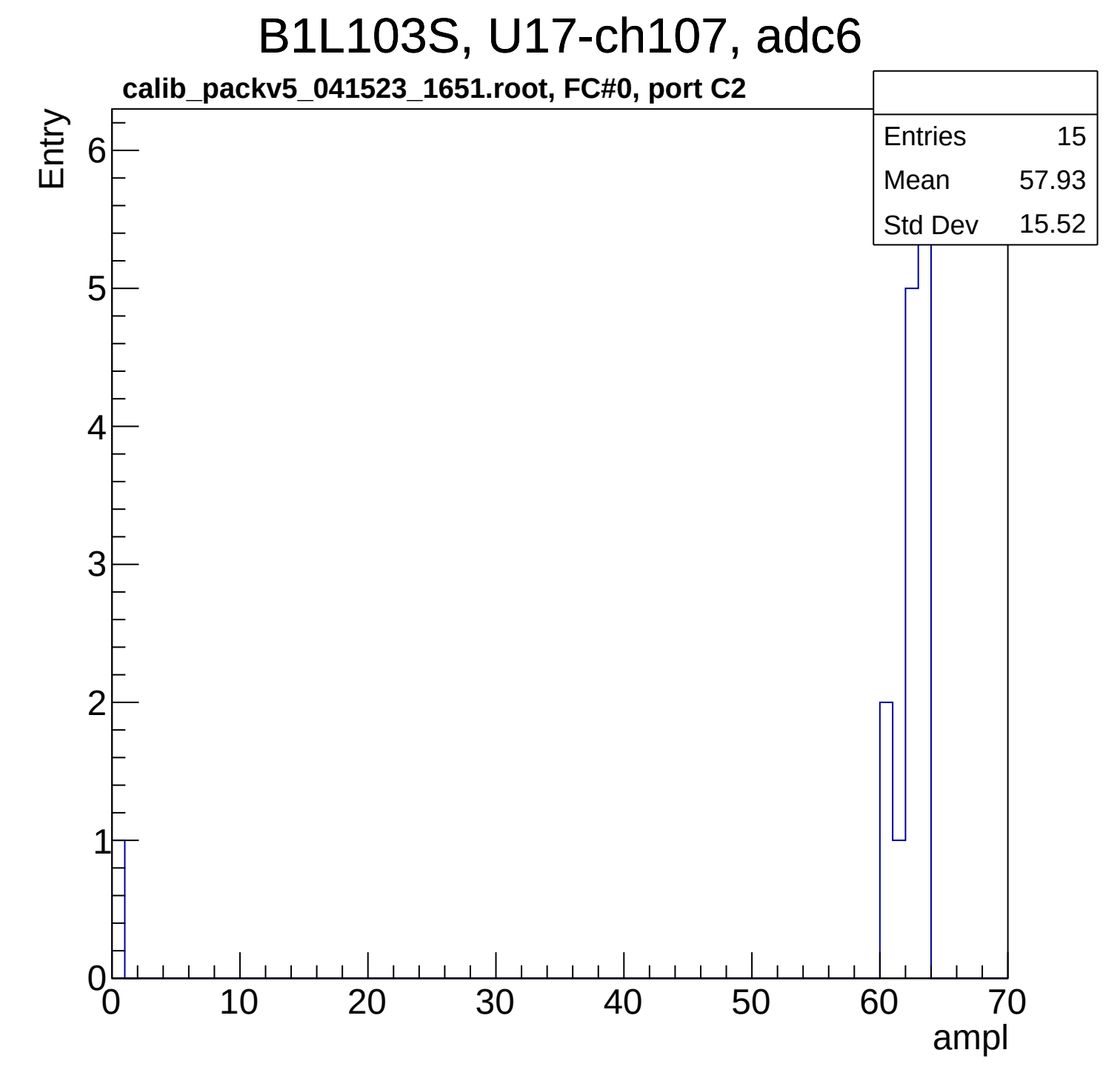

B1L103S, U17-ch107, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 35.16
Std Dev 5.781
Gaus mean : 36.3448
Gaus Width: 3.9336
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

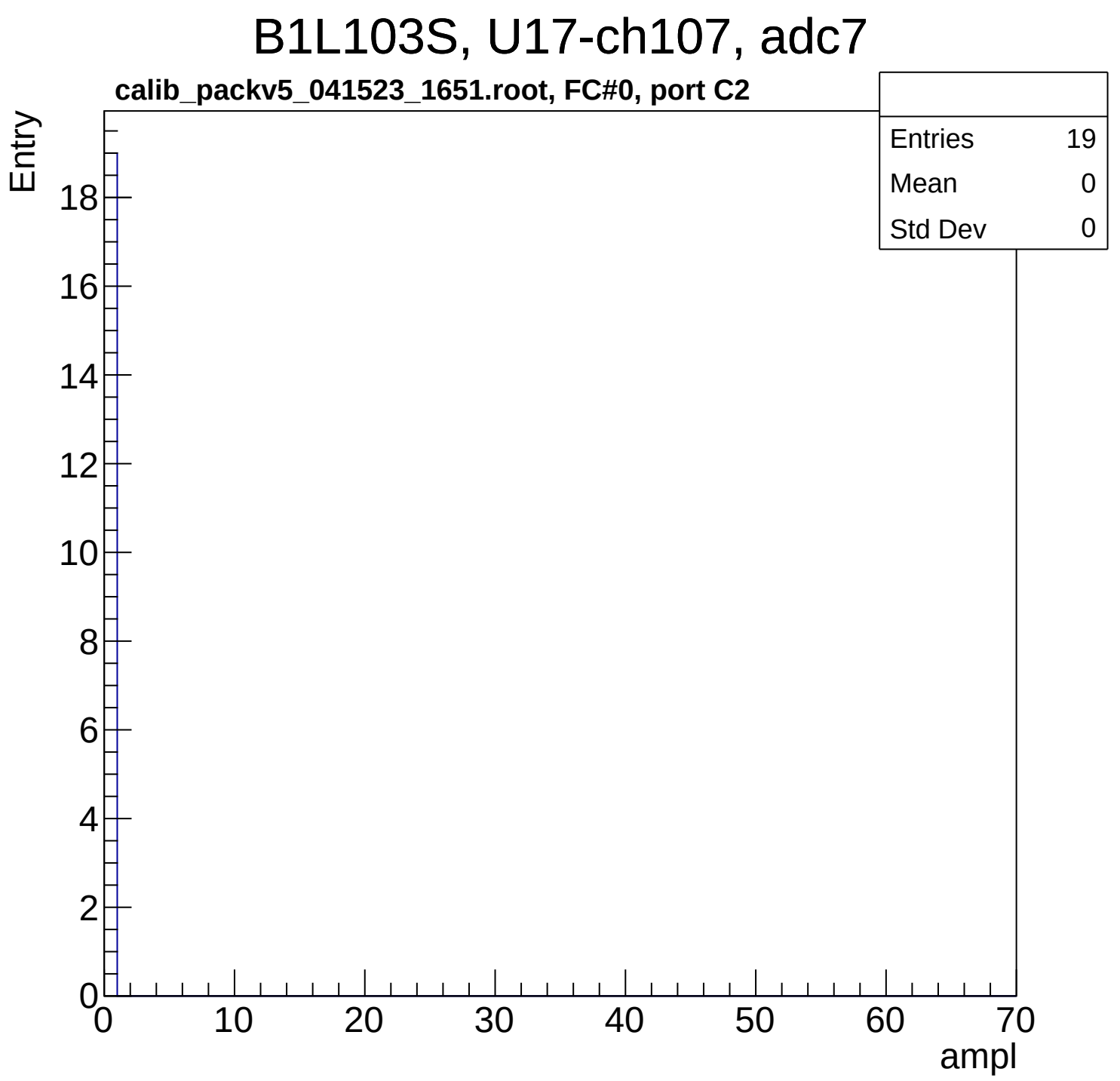

B1L103S, U17-ch107, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 39.79
Std Dev 9.65
Gaus mean : 42.3631
Gaus Width: 4.0050
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

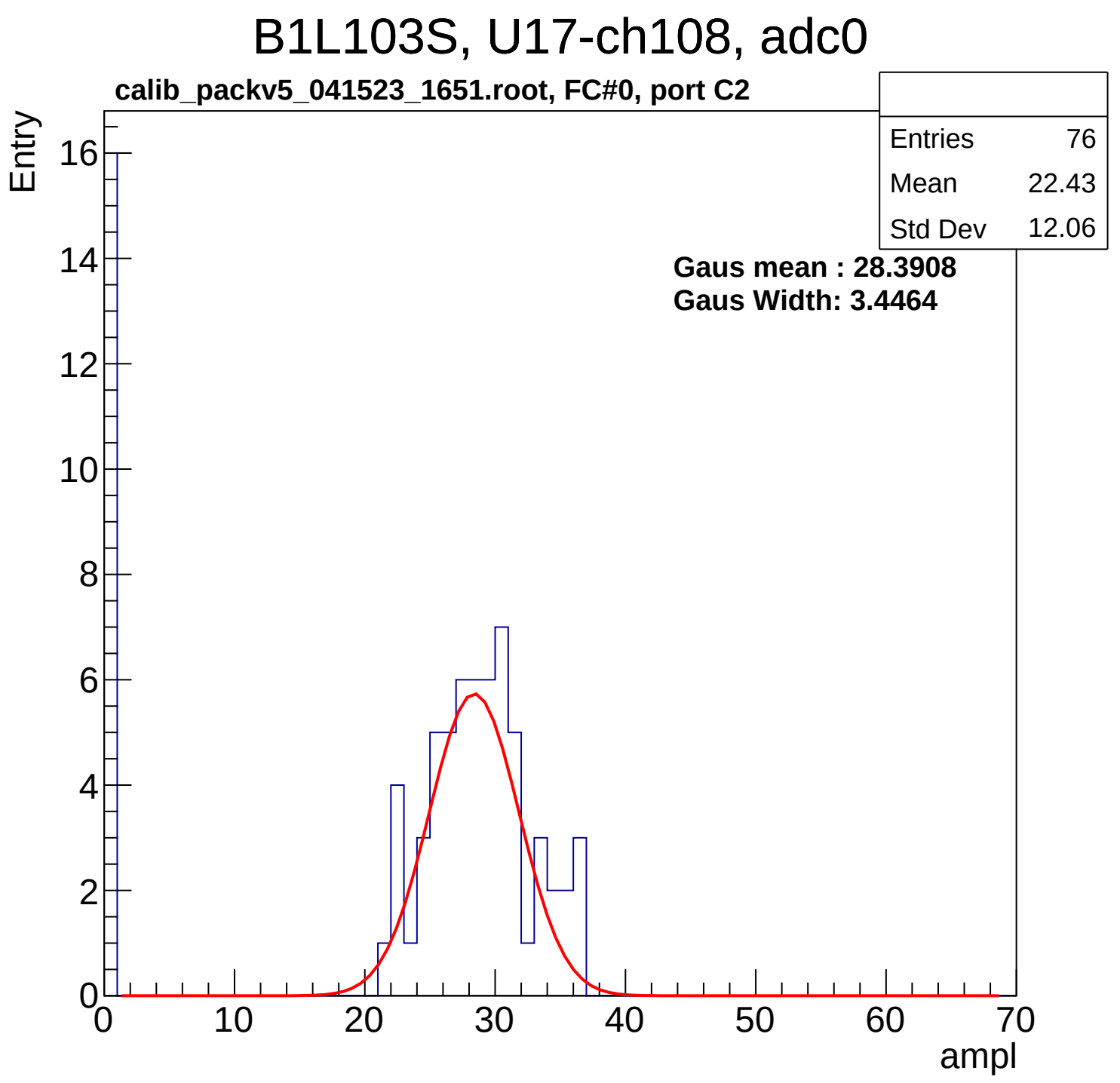

B1L103S, U17-ch107, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 42.89
Std Dev 16.67
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

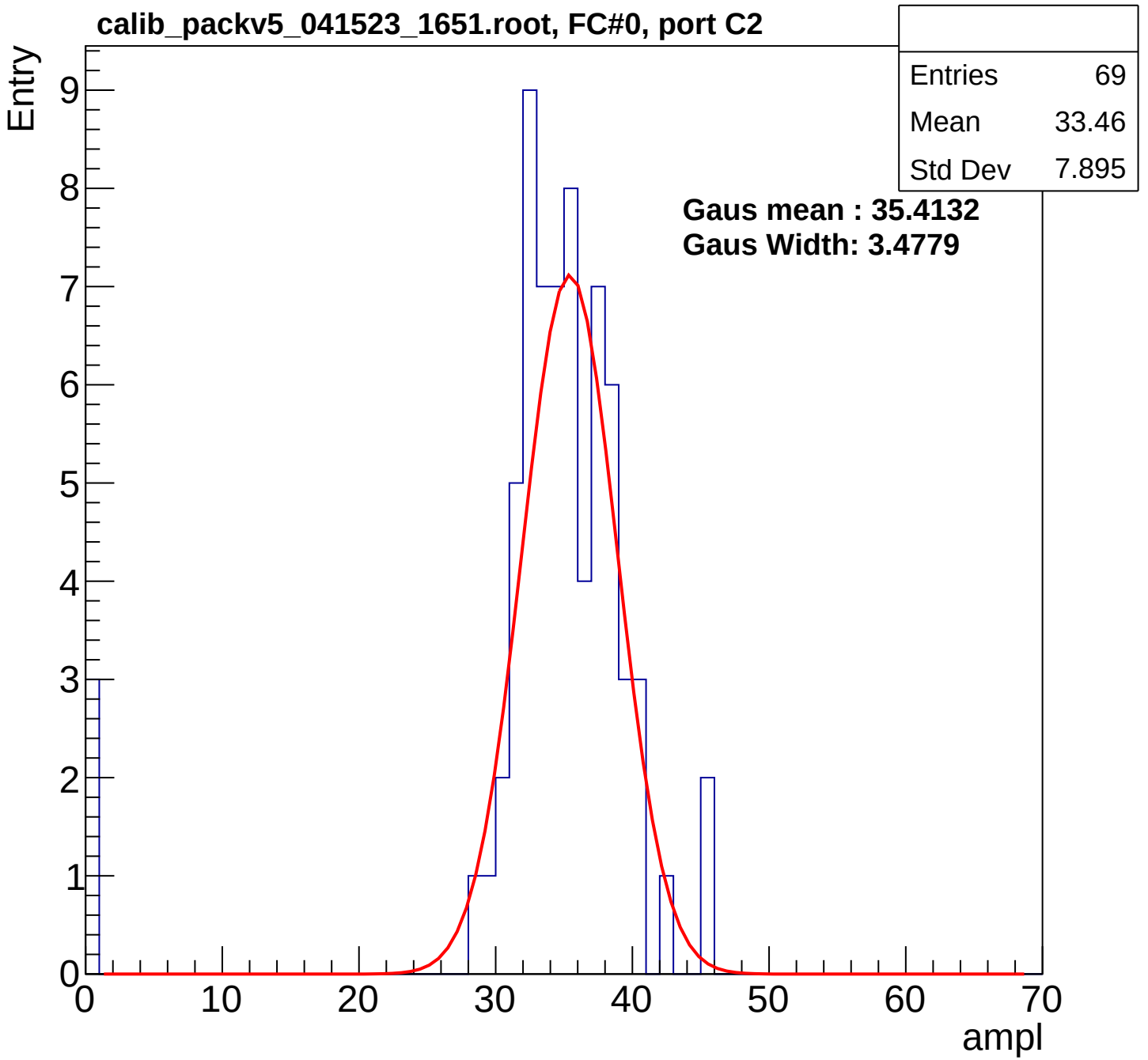

B1L103S, U17-ch107, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 55.62
Std Dev 3.741
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

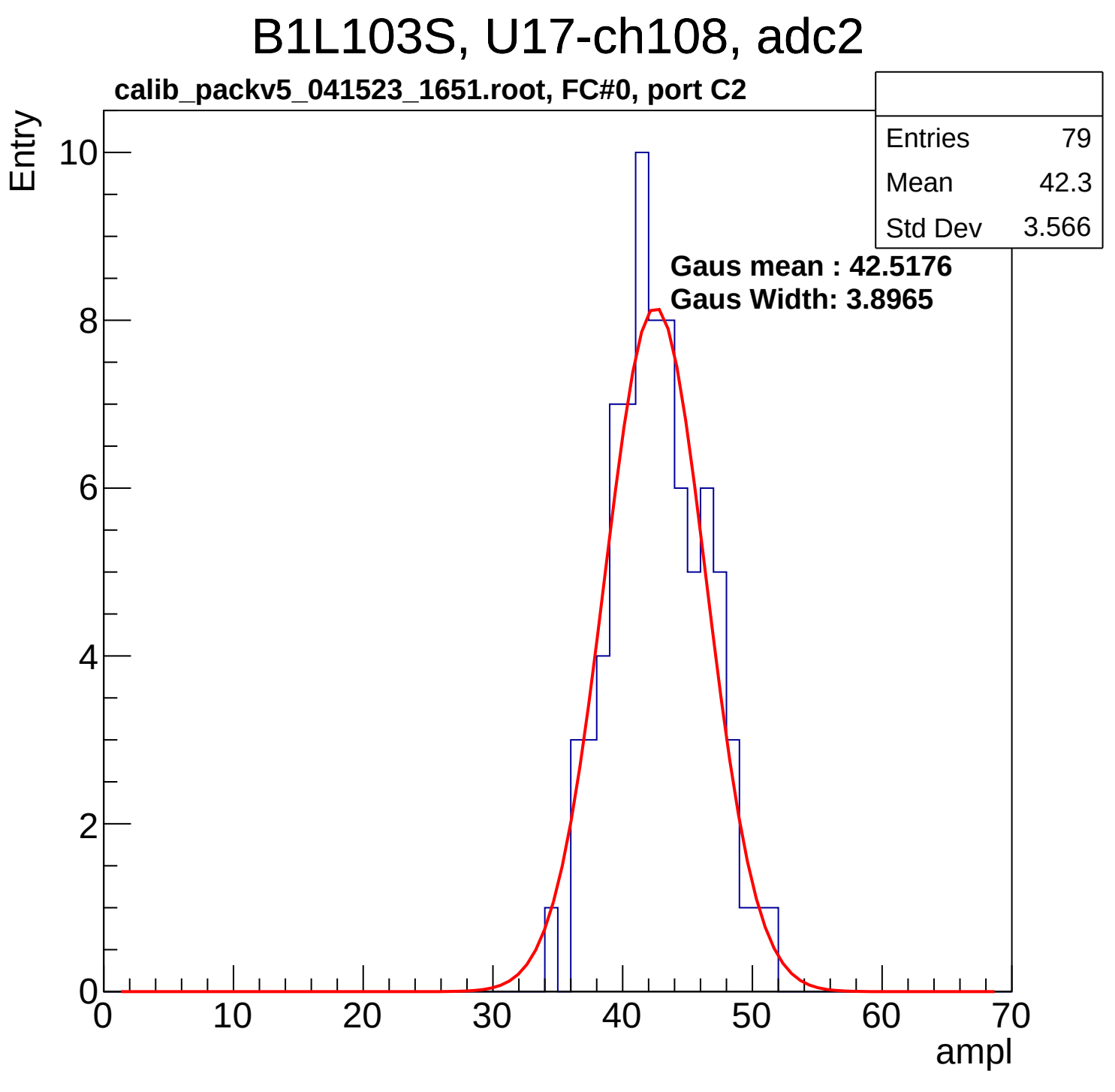

B1L103S, U17-ch107, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 59.28
Std Dev 2.298
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

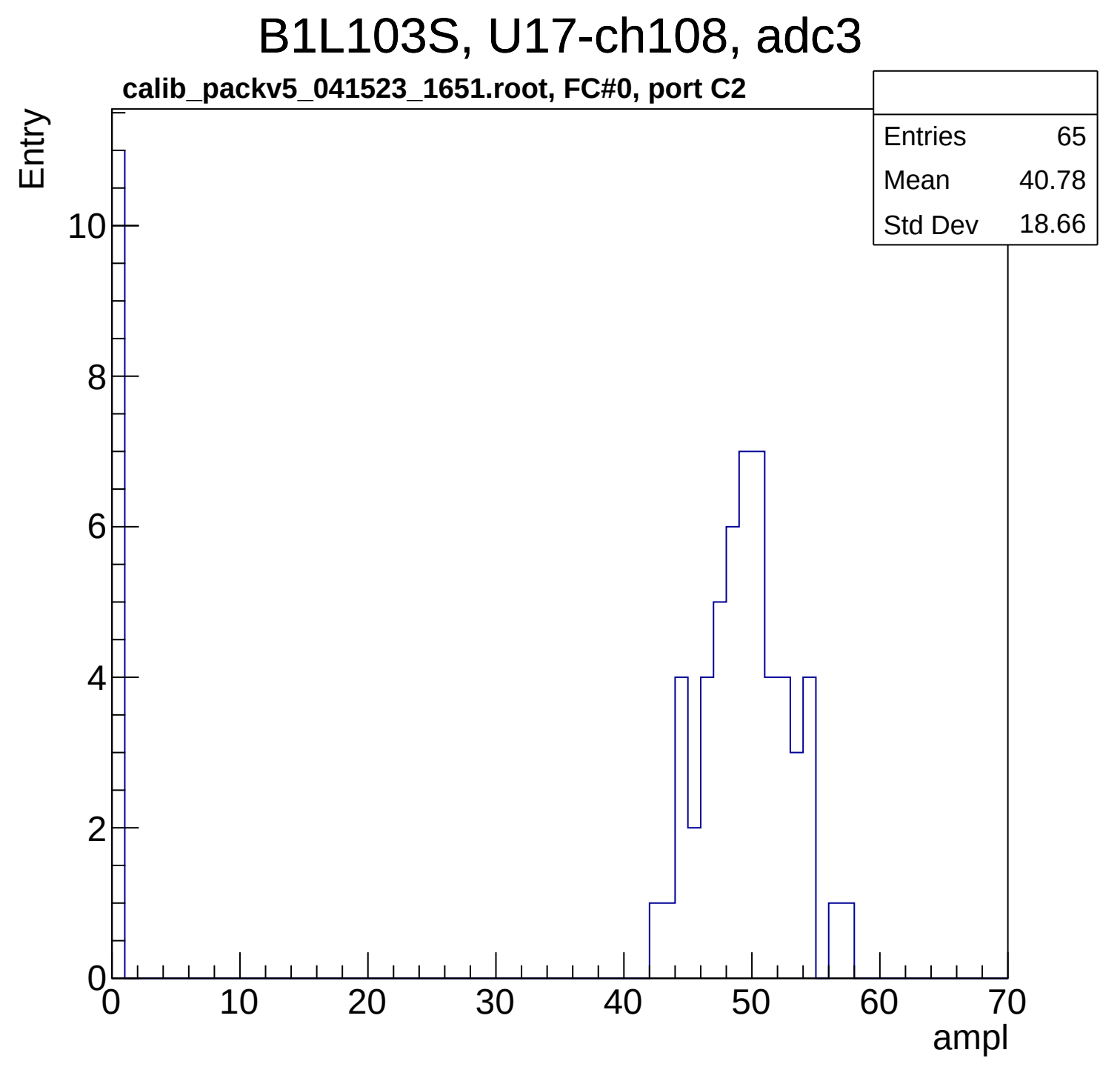

B1L103S, U17-ch107, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.93
Std Dev 15.52
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

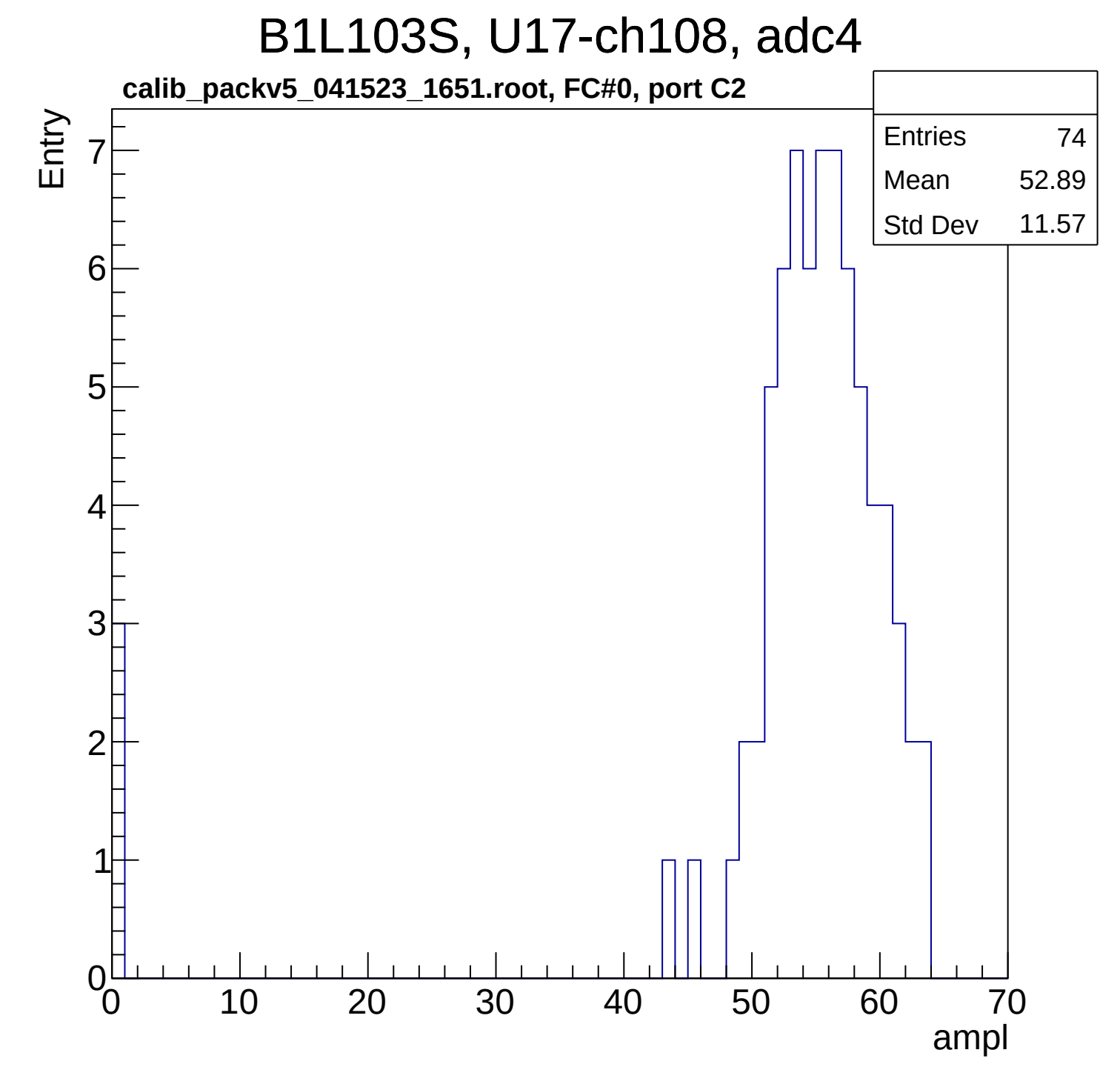

B1L103S, U17-ch107, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

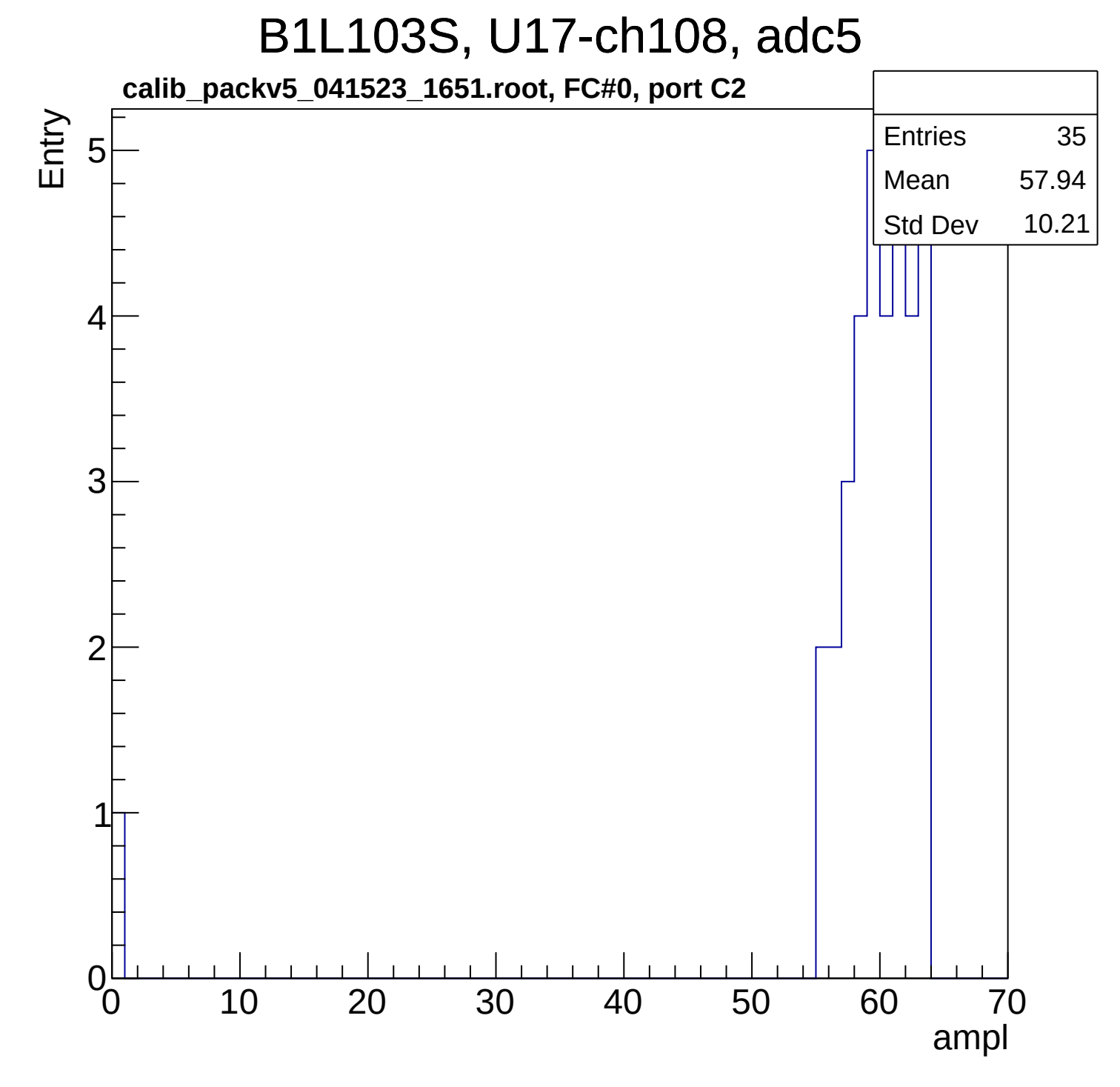

B1L103S, U17-ch108, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 22.43
Std Dev 12.06
Gaus mean : 28.3908
Gaus Width: 3.4464
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

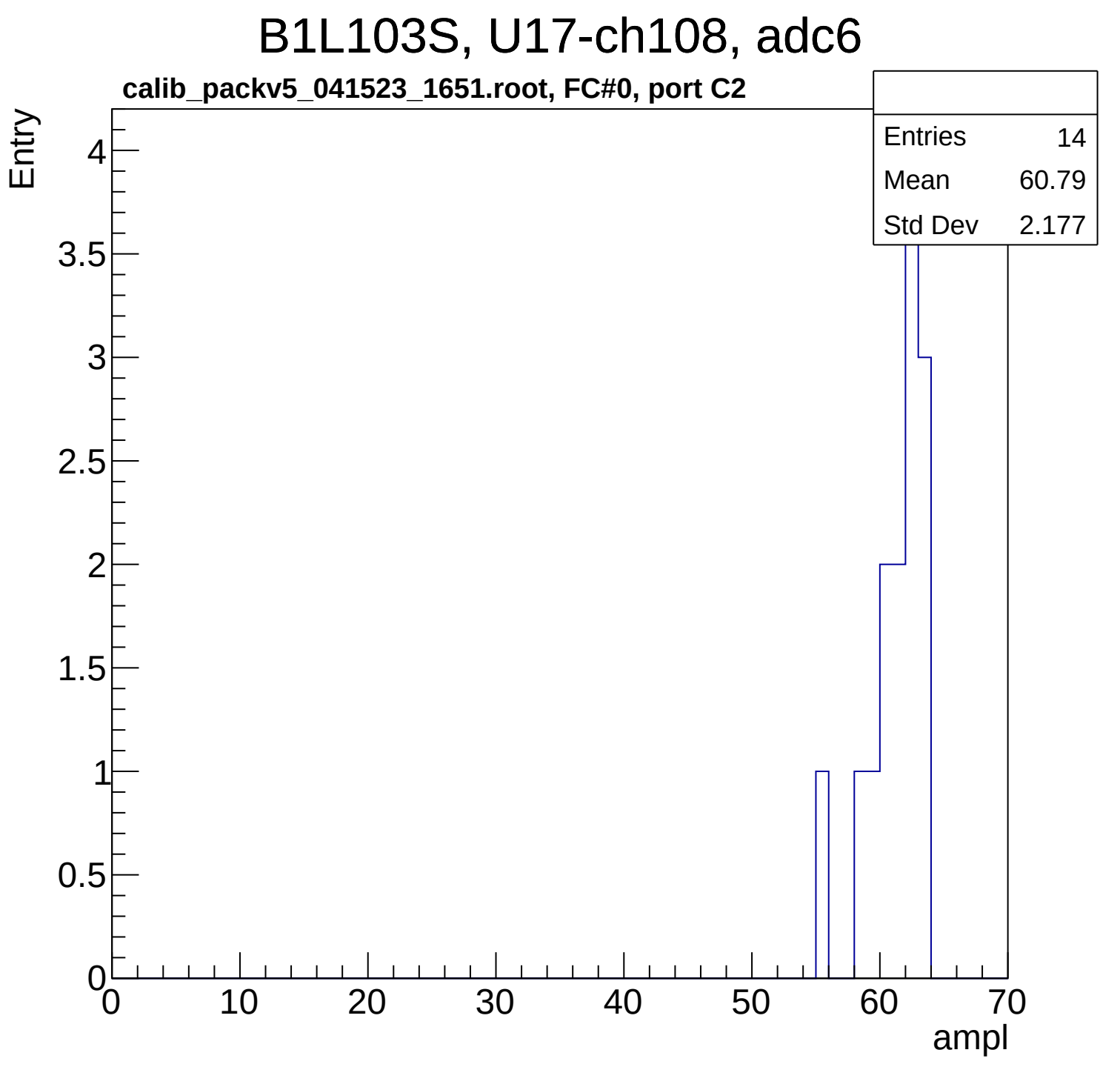

B1L103S, U17-ch108, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 33.46
Std Dev 7.895
Gaus mean : 35.4132
Gaus Width: 3.4779
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

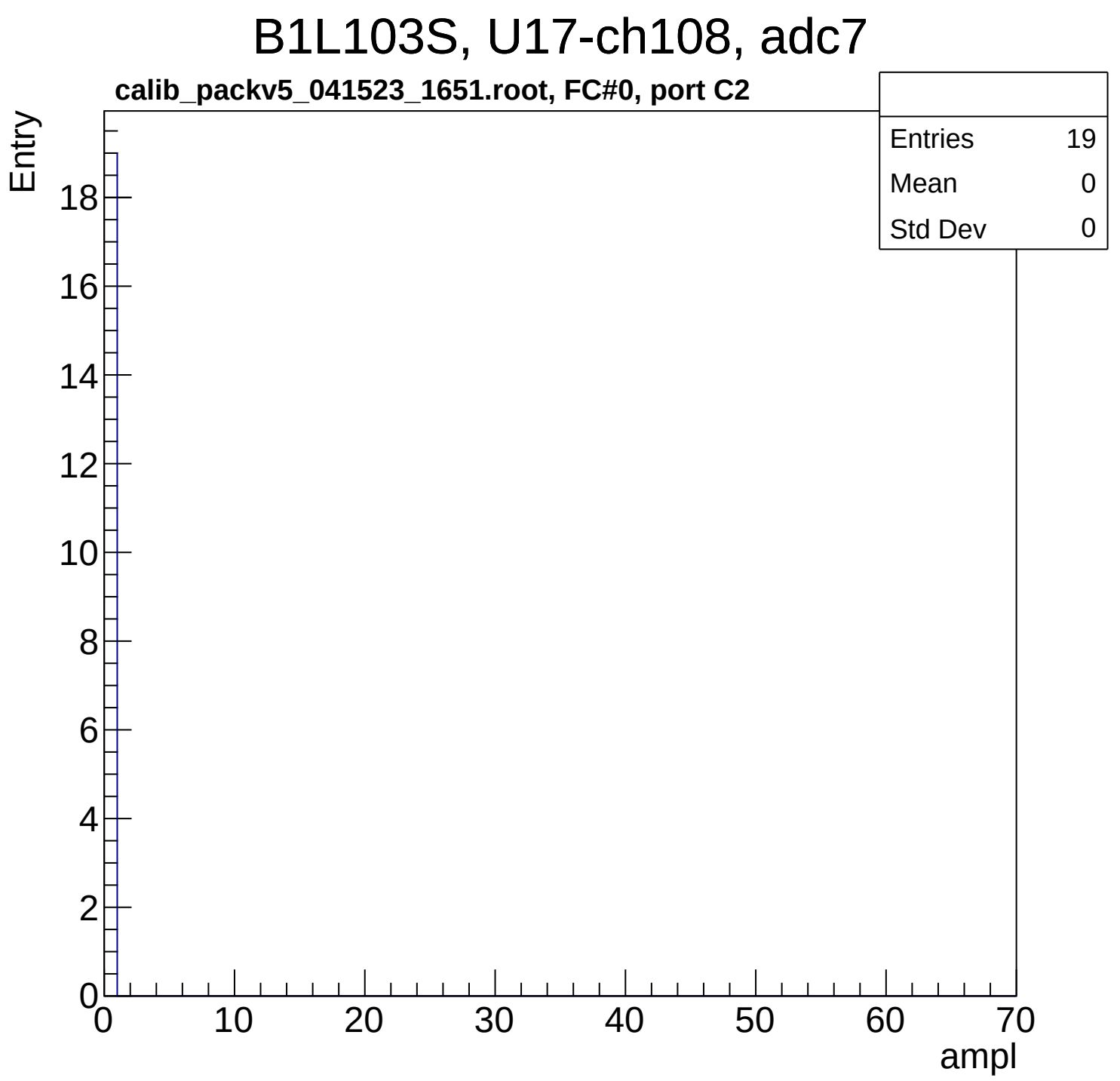

B1L103S, U17-ch108, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 42.3
Std Dev 3.566
Gaus mean : 42.5176
Gaus Width: 3.8965
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

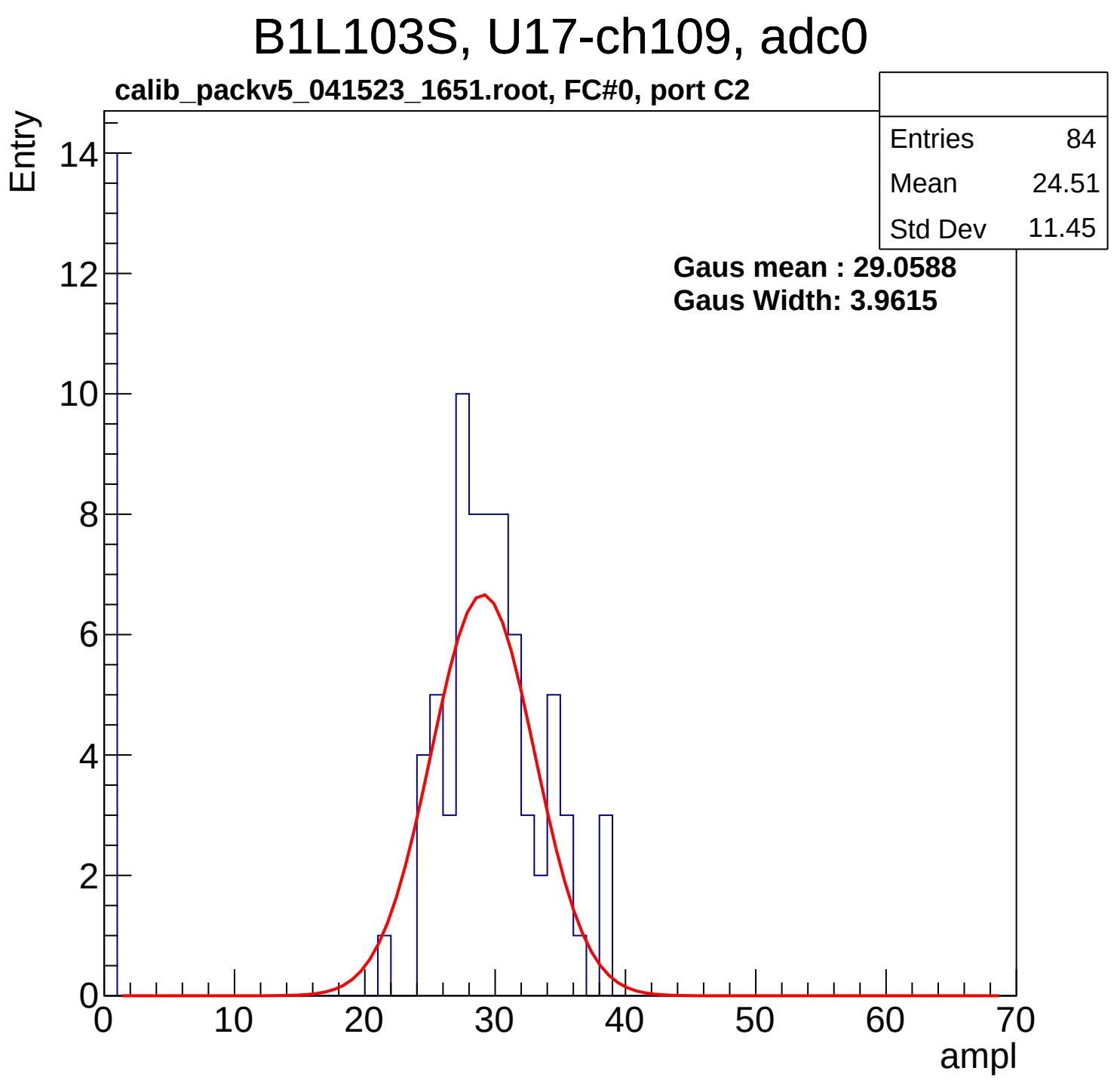

B1L103S, U17-ch108, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 40.78
Std Dev 18.66
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

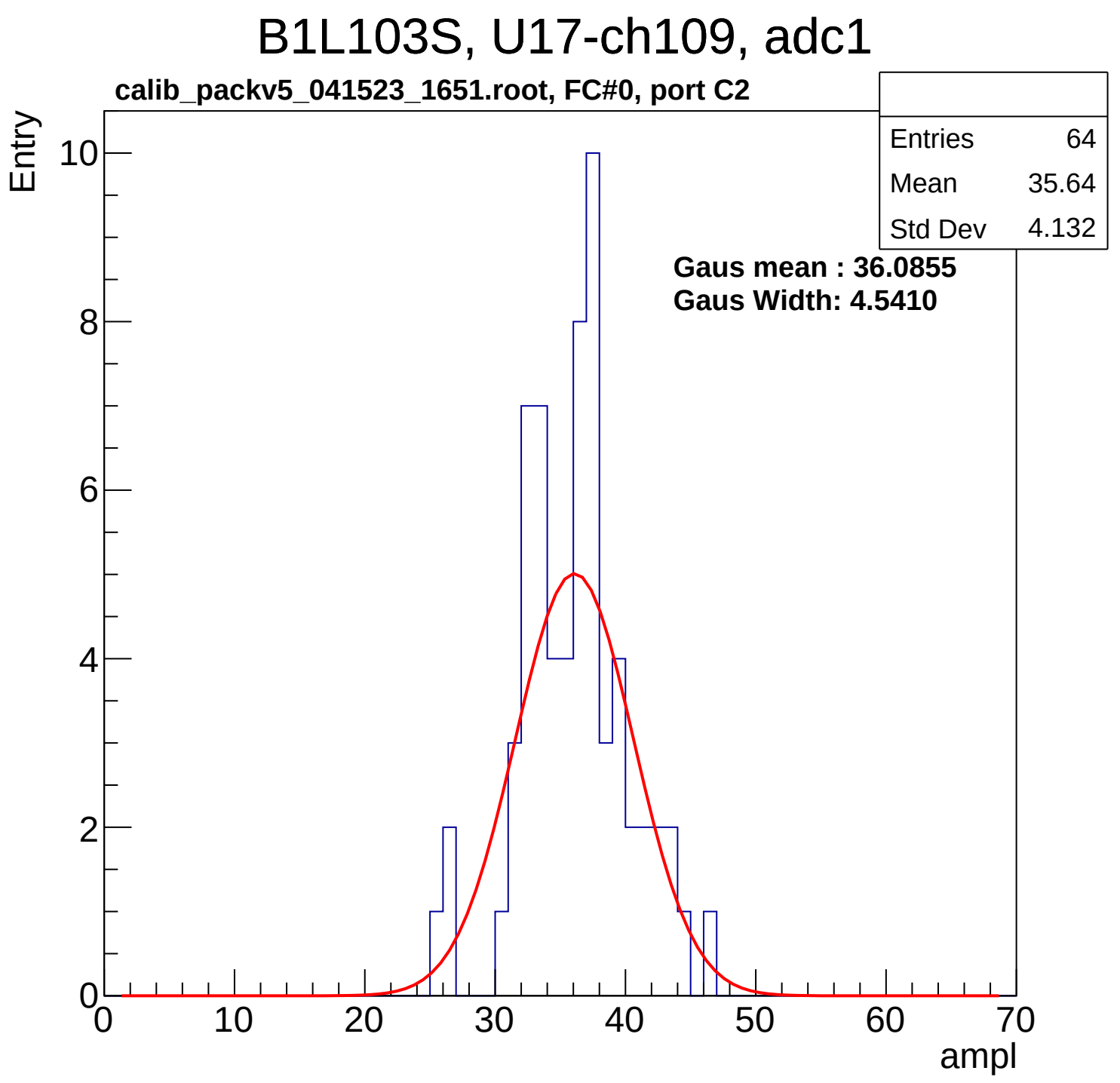

B1L103S, U17-ch108, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 52.89
Std Dev 11.57
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

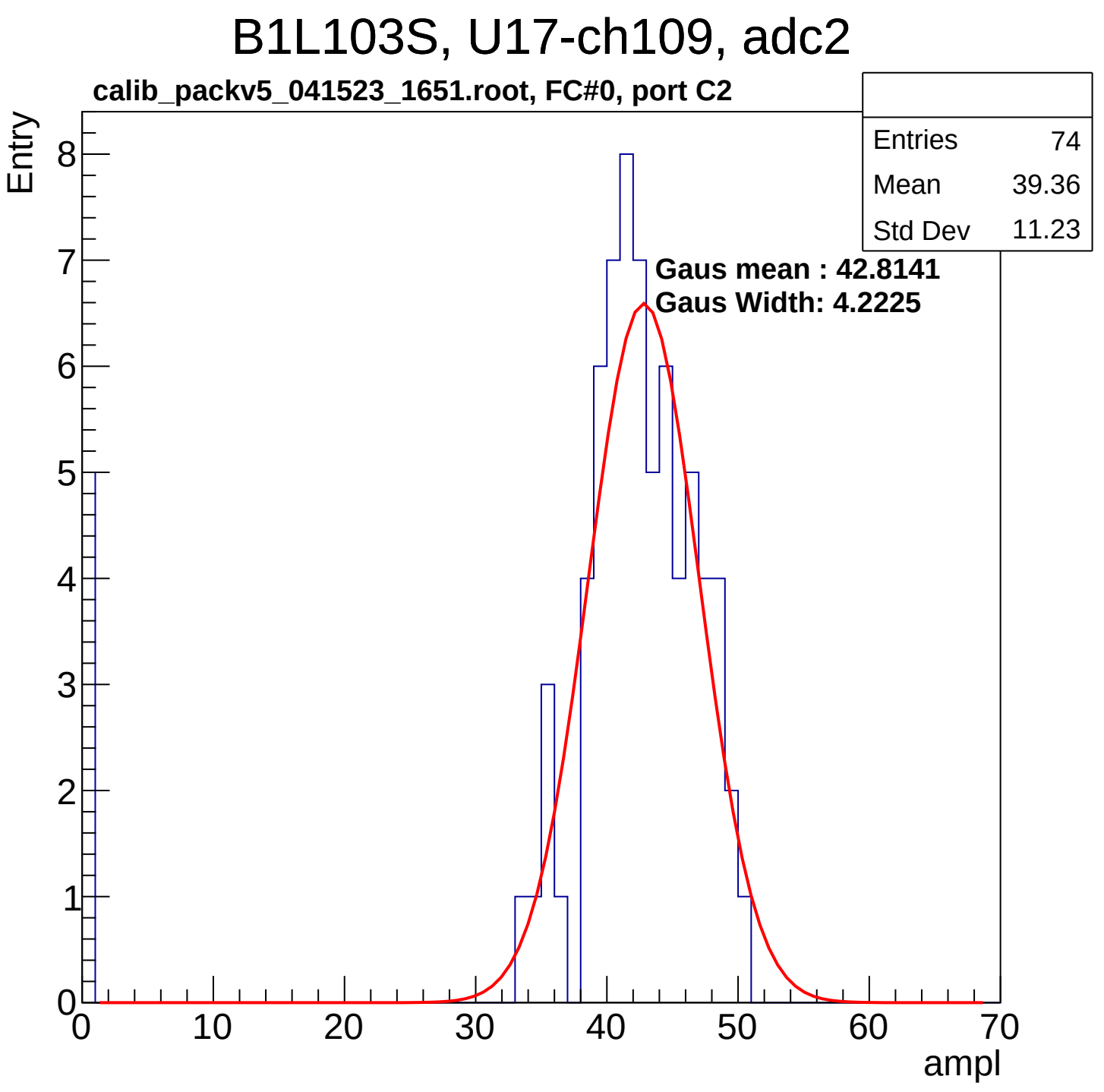

B1L103S, U17-ch108, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 57.94
Std Dev 10.21
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

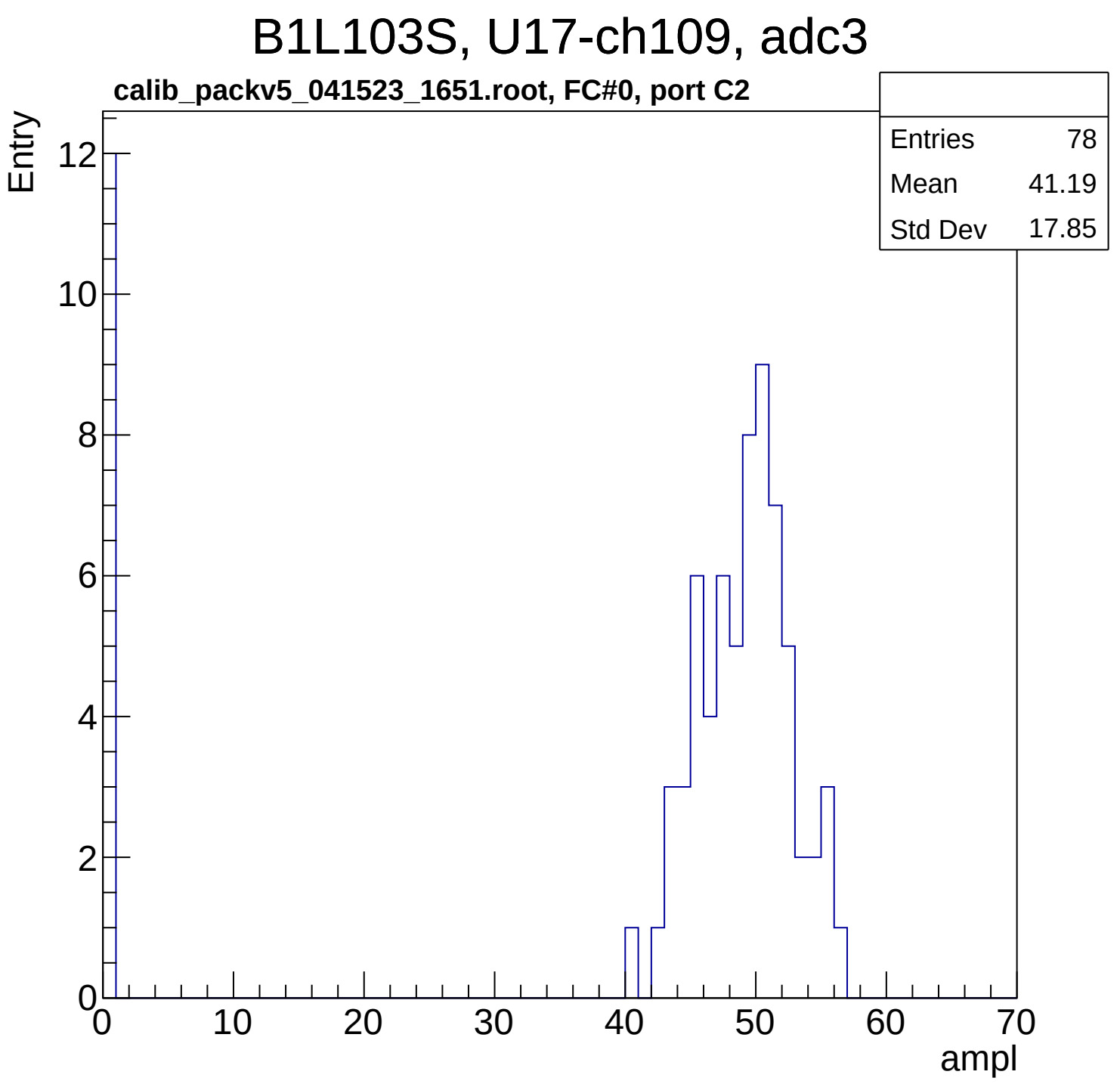

B1L103S, U17-ch108, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 60.79
Std Dev 2.177
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

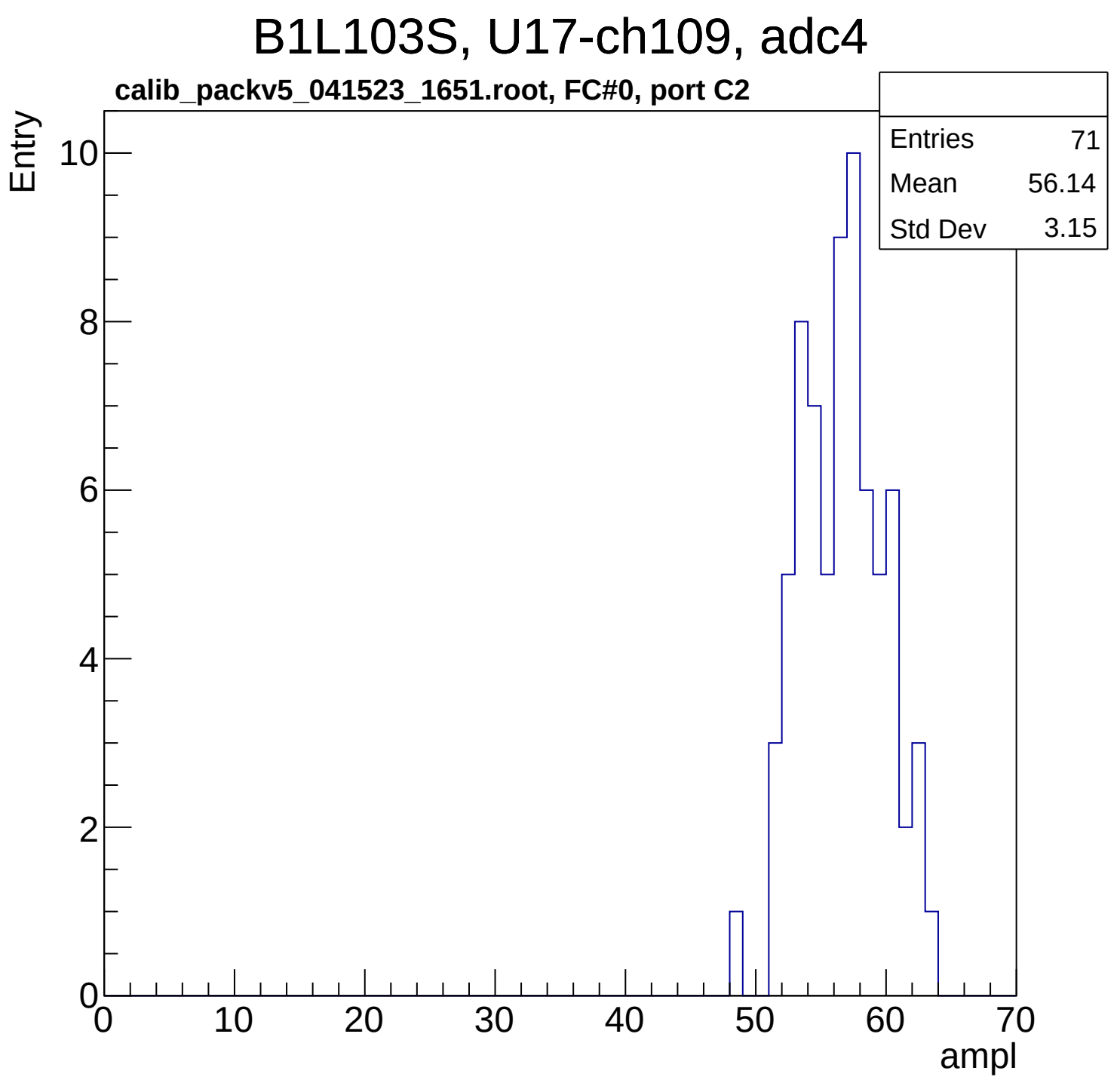

B1L103S, U17-ch108, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

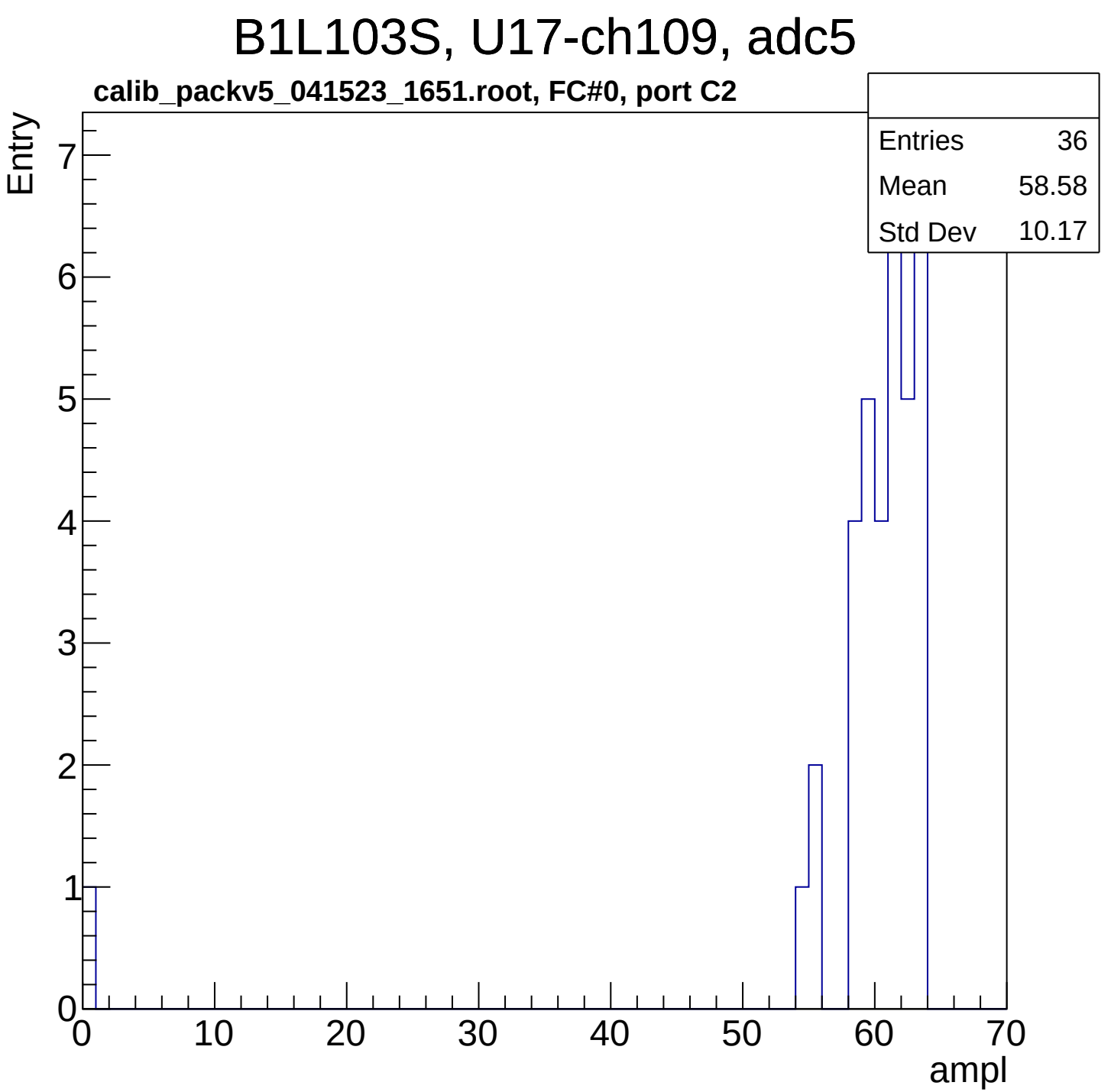

B1L103S, U17-ch109, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 24.51
Std Dev 11.45
Gaus mean : 29.0588
Gaus Width: 3.9615
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

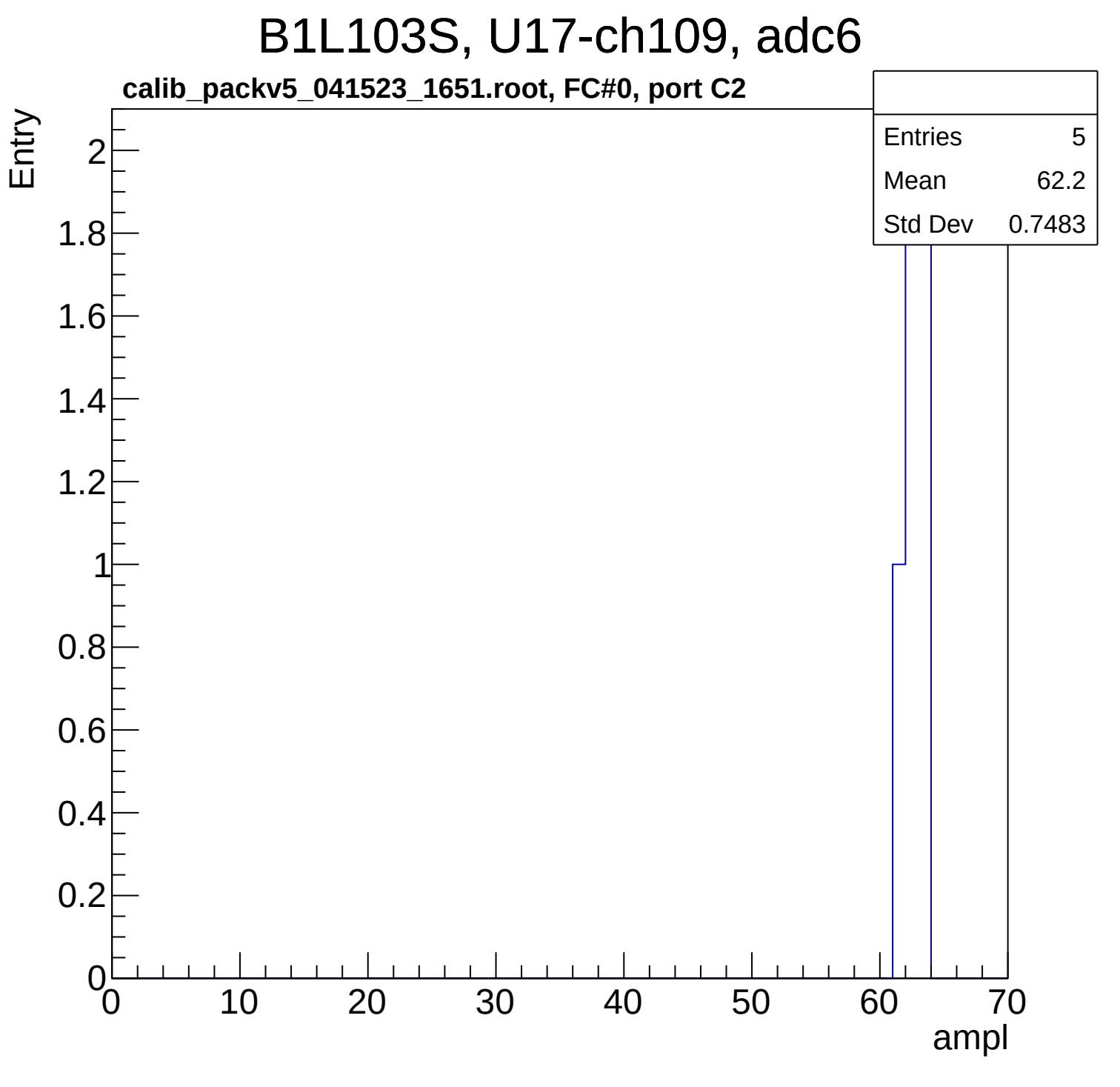

B1L103S, U17-ch109, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 35.64
Std Dev 4.132
Gaus mean : 36.0855
Gaus Width: 4.5410
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

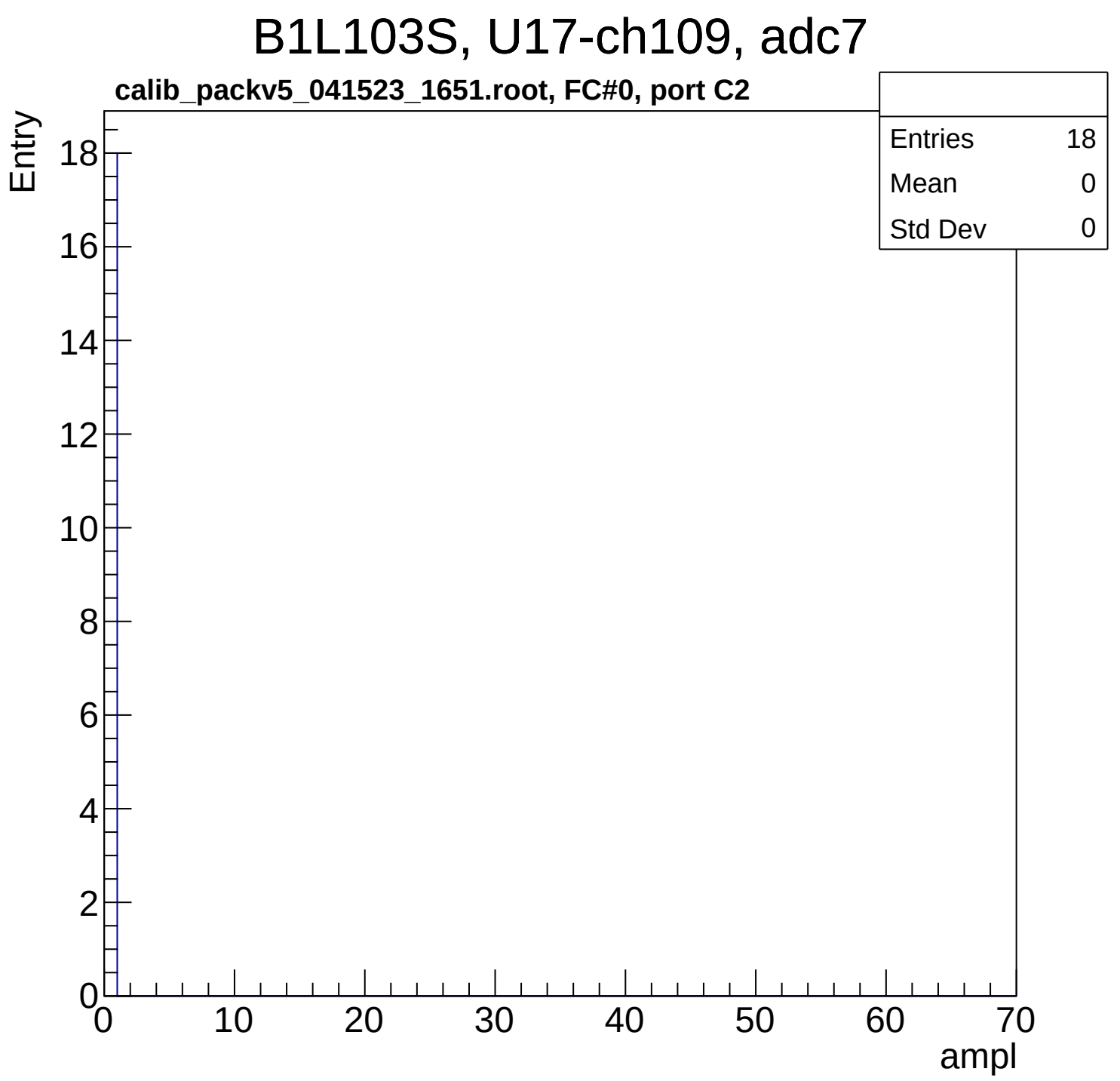

B1L103S, U17-ch109, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 39.36
Std Dev 11.23
Gaus mean : 42.8141
Gaus Width: 4.2225
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

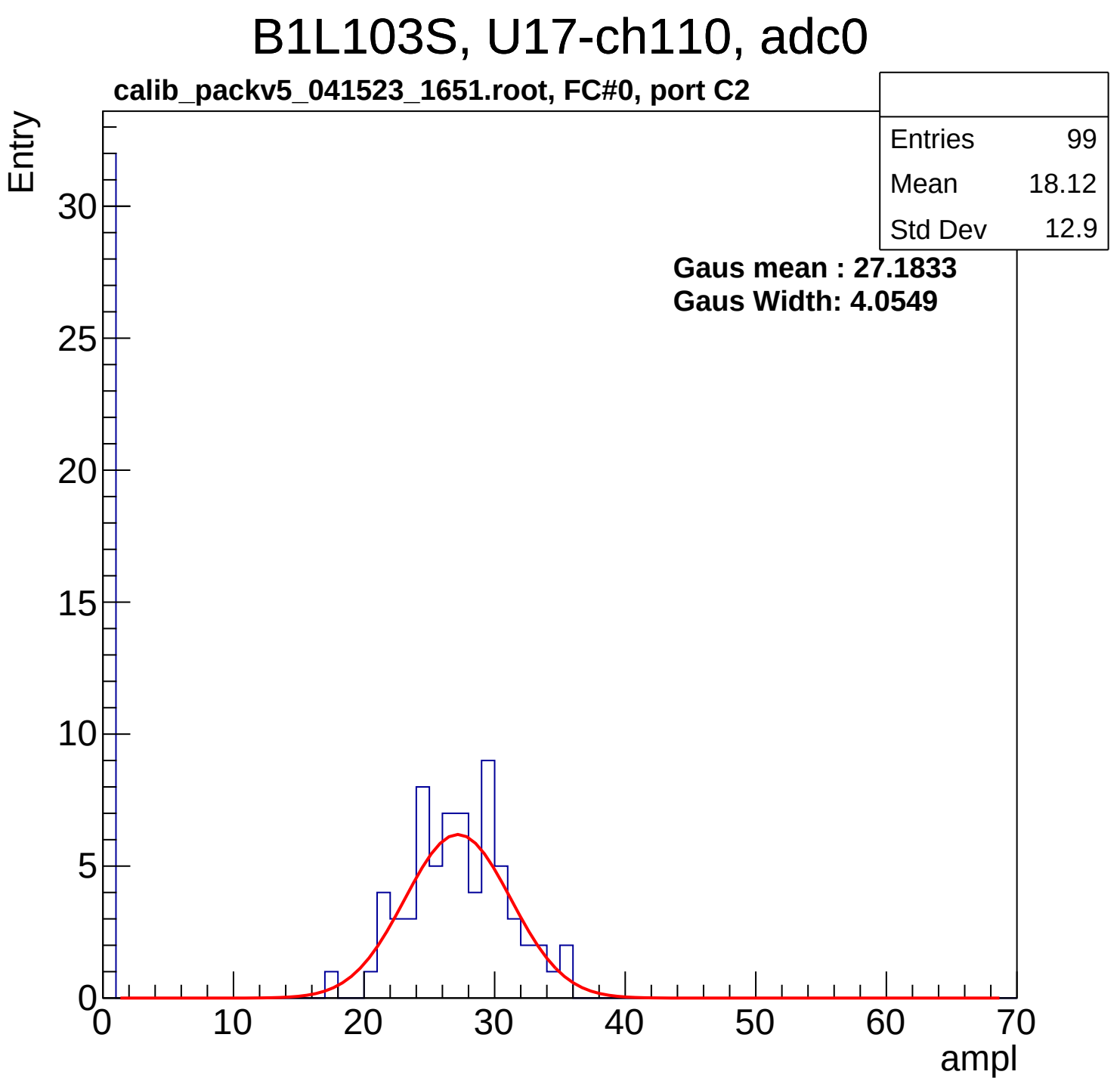

B1L103S, U17-ch109, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 41.19
Std Dev 17.85
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

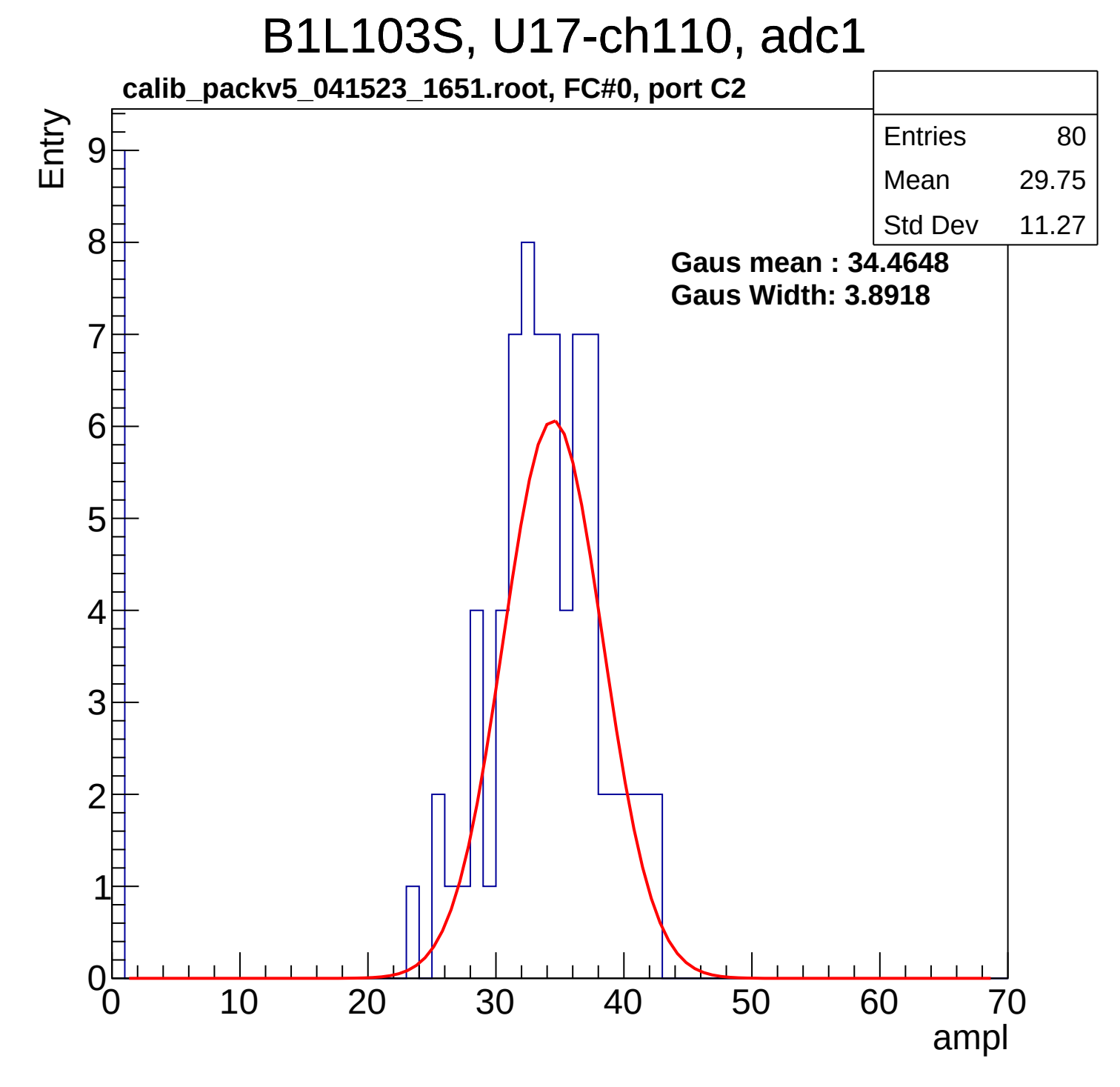

B1L103S, U17-ch109, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 56.14
Std Dev 3.15
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

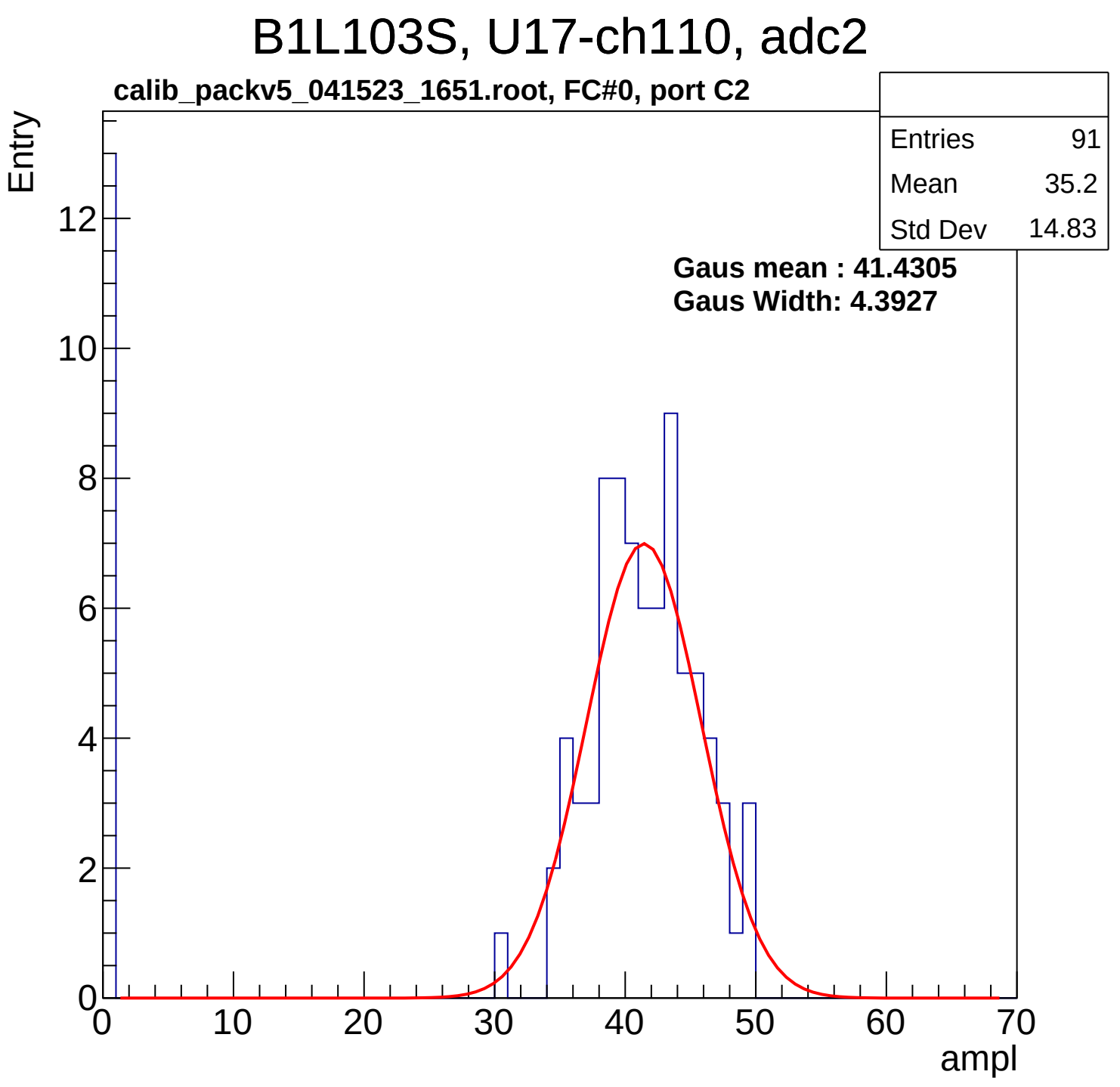

B1L103S, U17-ch109, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 58.58
Std Dev 10.17
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

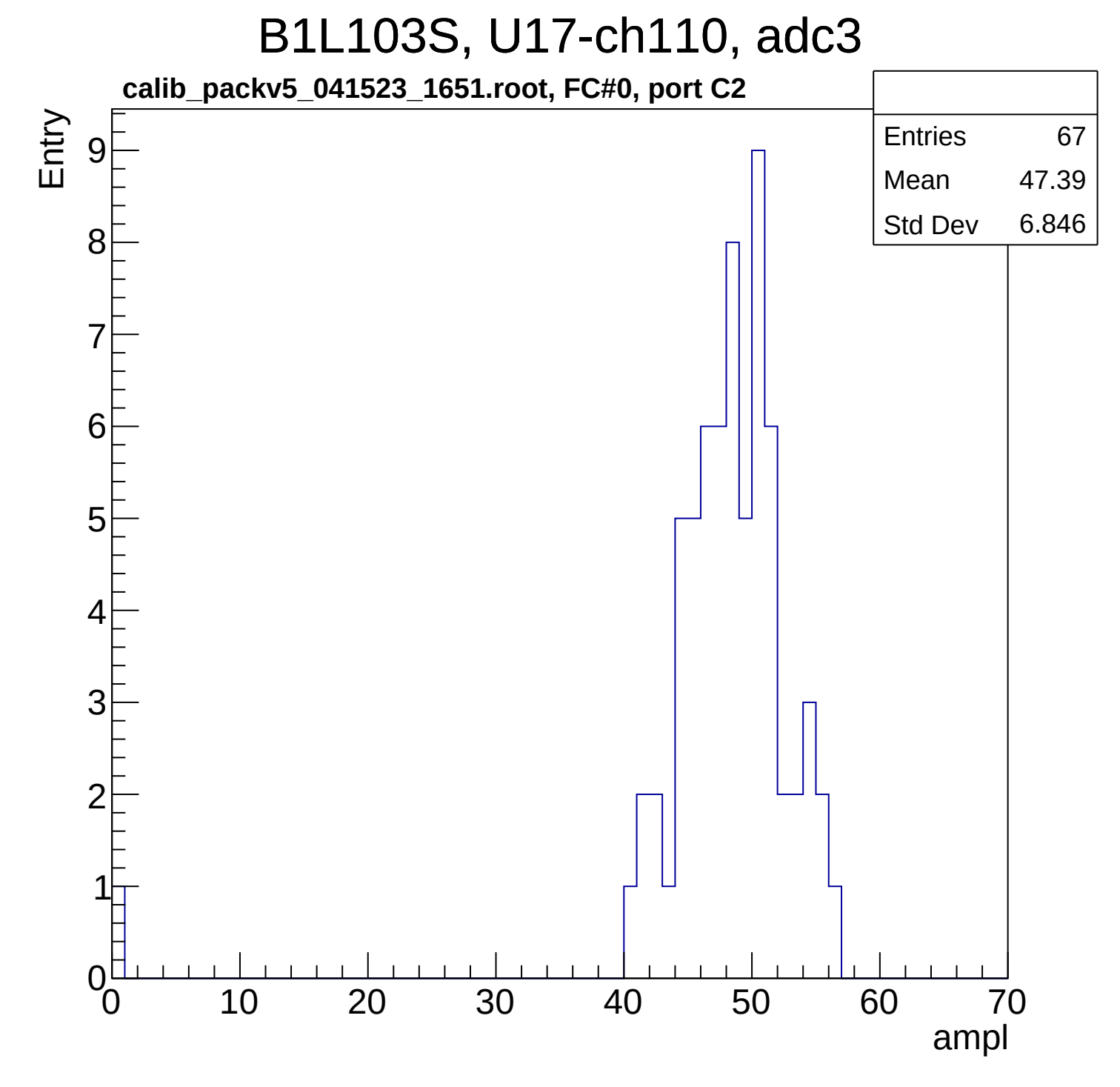

B1L103S, U17-ch109, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.2
Std Dev 0.7483
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

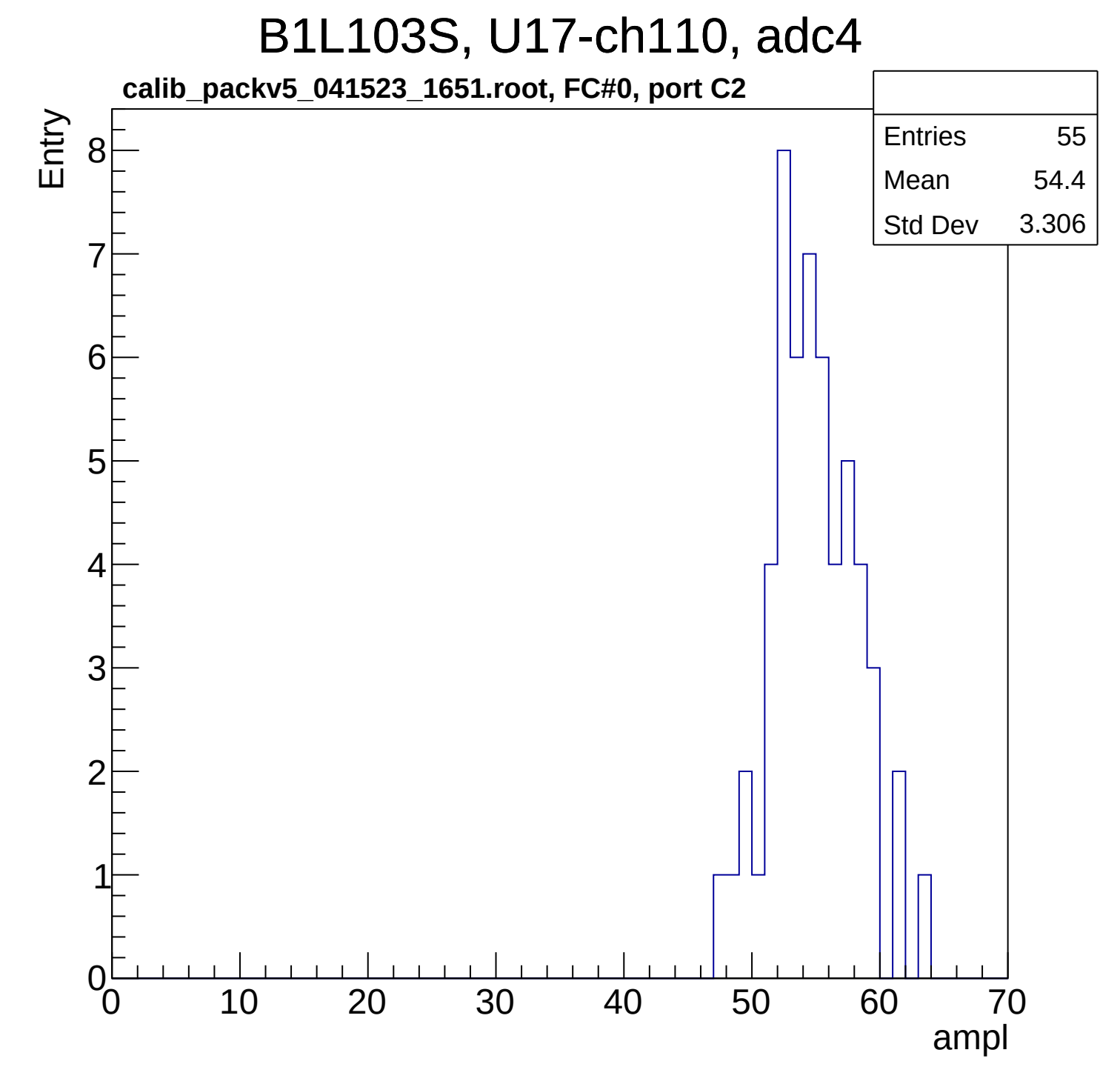

B1L103S, U17-ch109, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

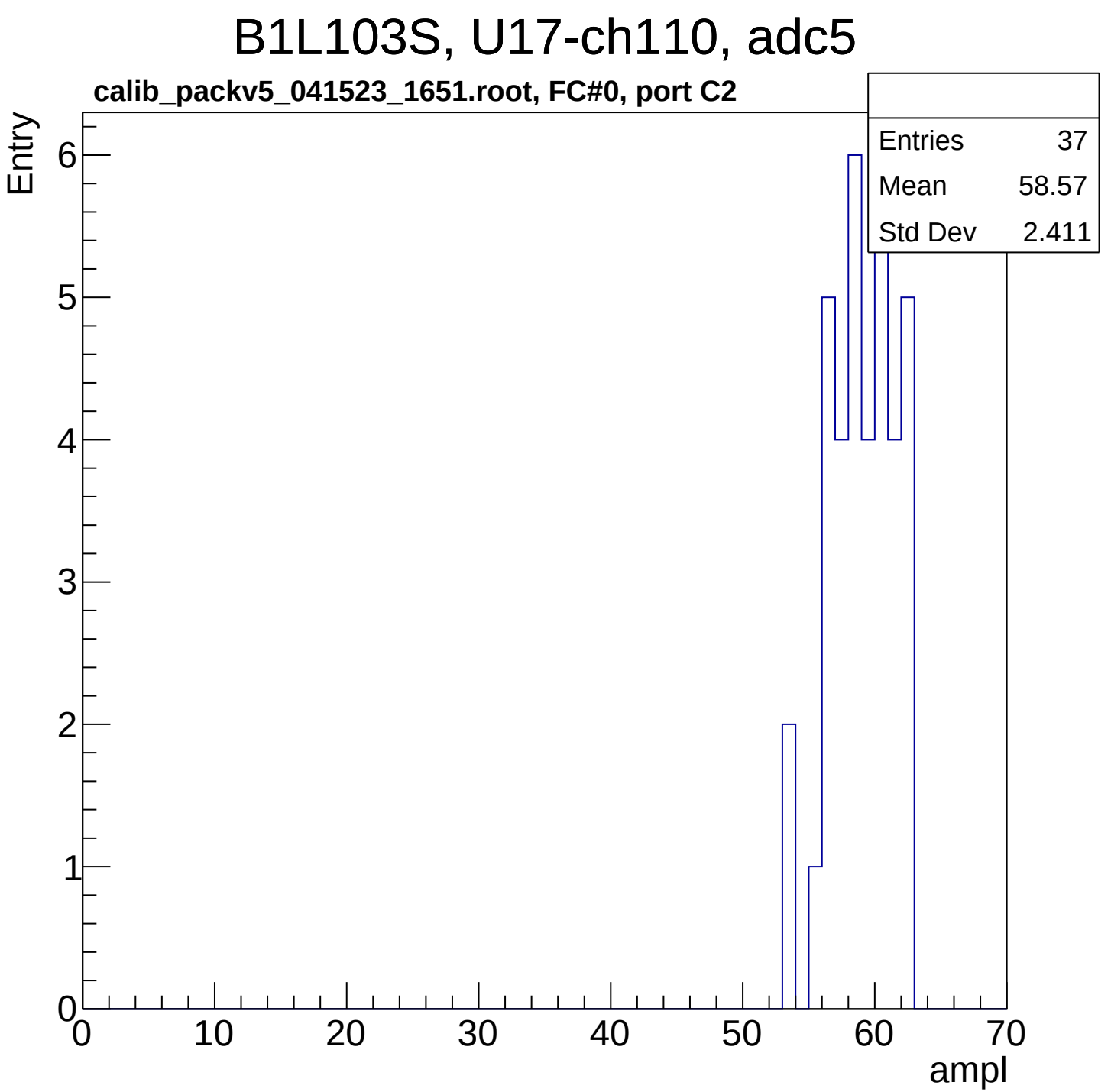

B1L103S, U17-ch110, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 18.12
Std Dev 12.9
Gaus mean : 27.1833
Gaus Width: 4.0549
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70

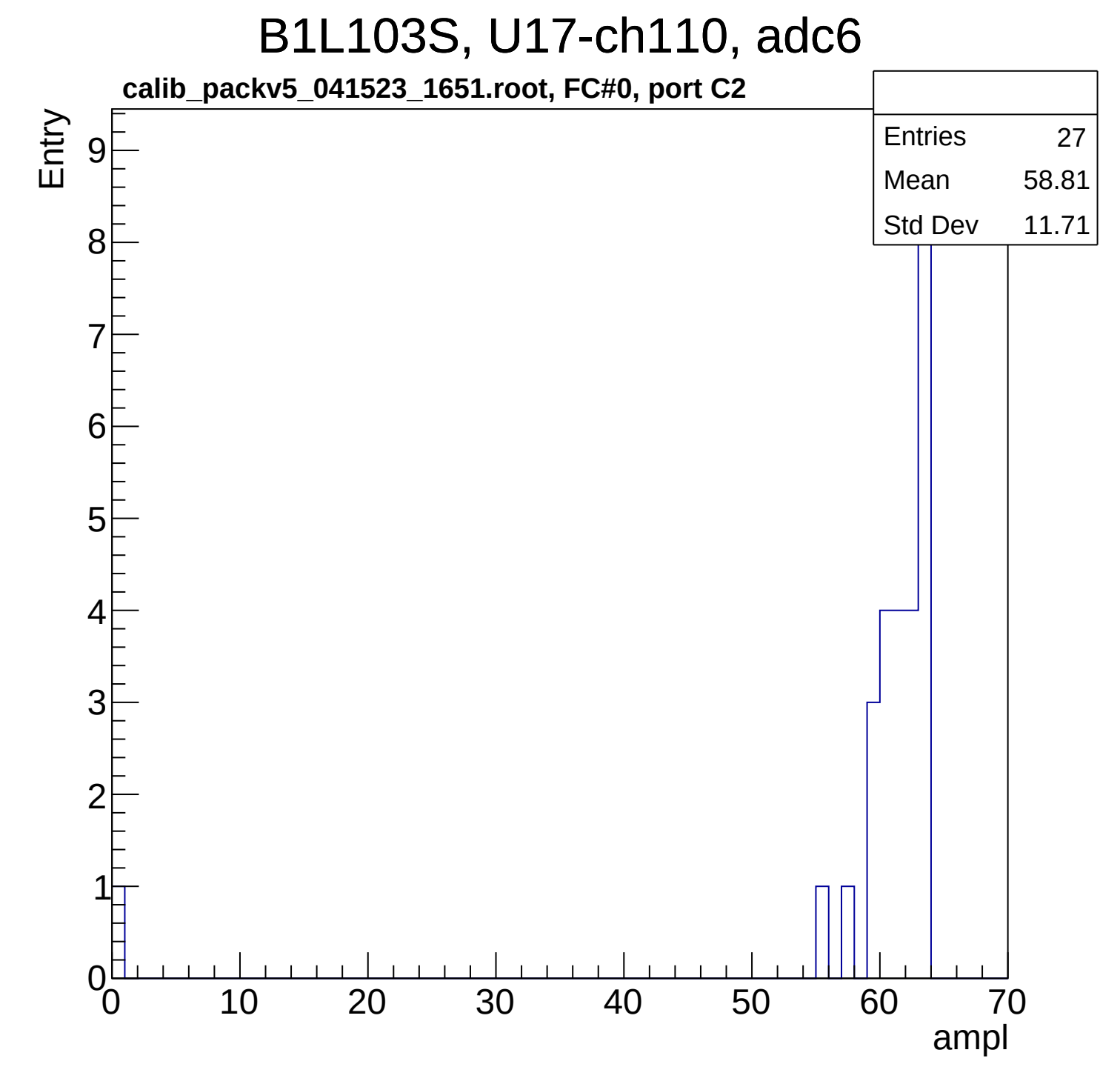

B1L103S, U17-ch110, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 29.75
Std Dev 11.27
Gaus mean : 34.4648
Gaus Width: 3.8918
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

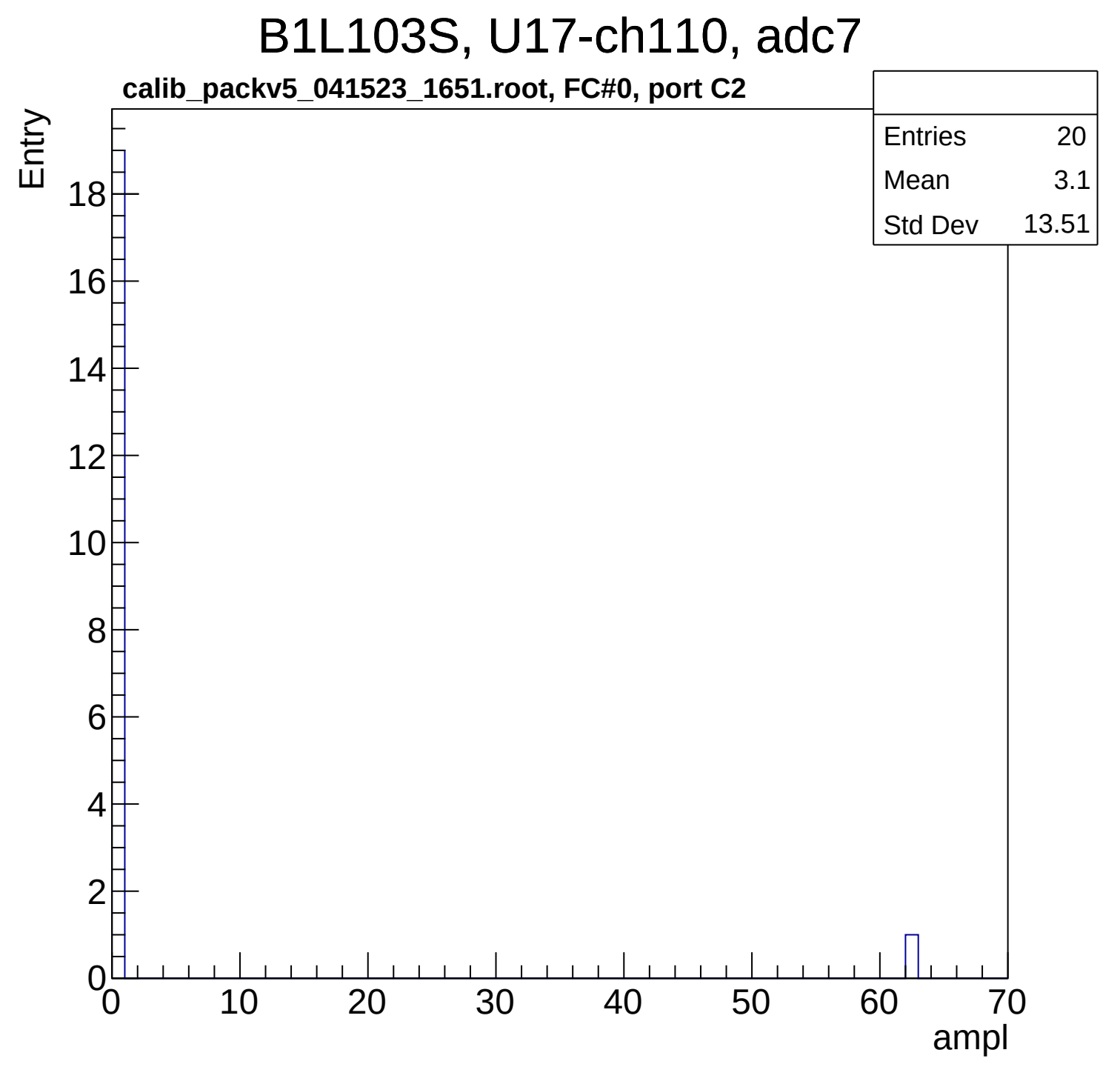

B1L103S, U17-ch110, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 35.2
Std Dev 14.83
Gaus mean : 41.4305
Gaus Width: 4.3927
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

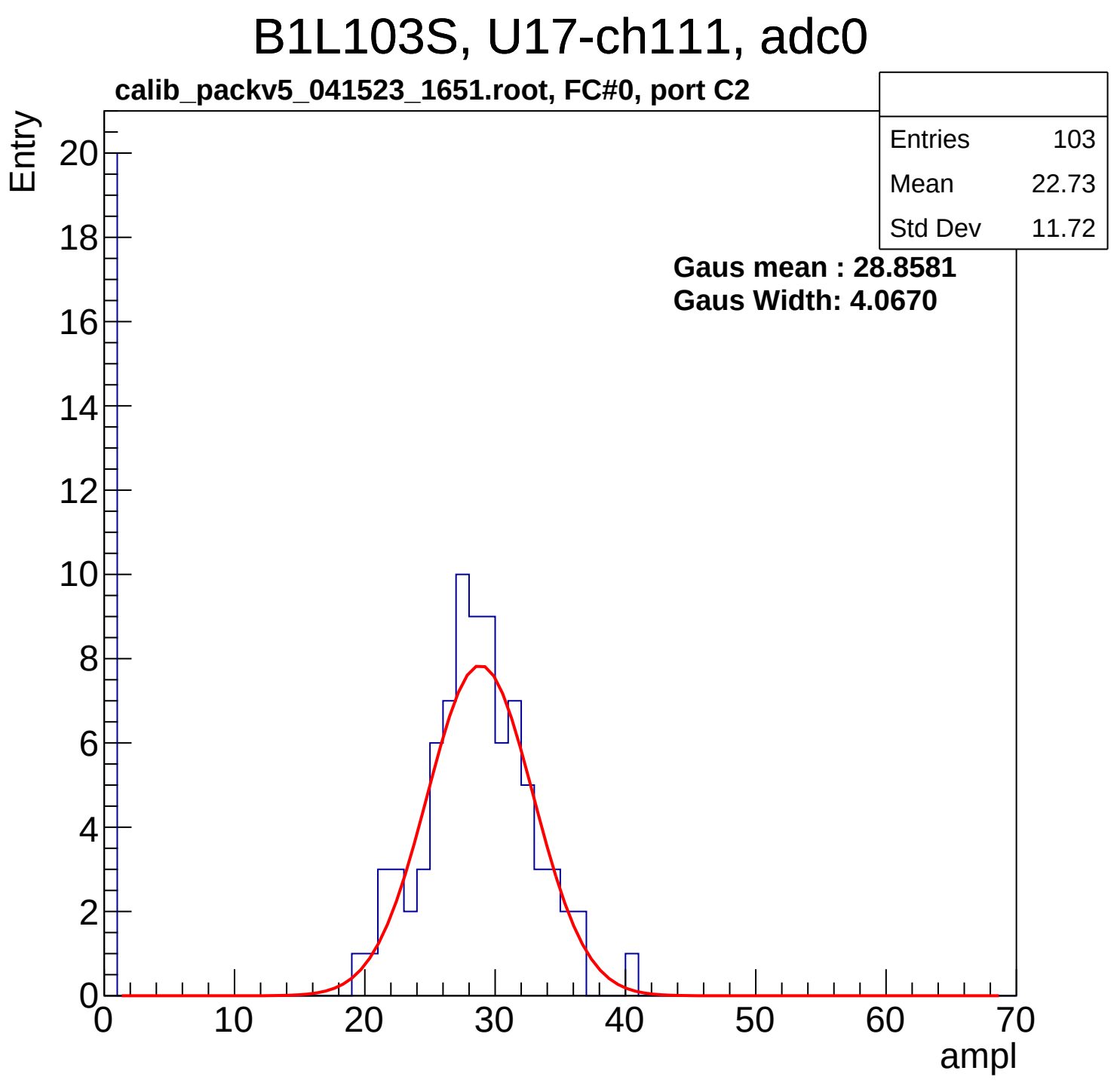

B1L103S, U17-ch110, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 47.39
Std Dev 6.846
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

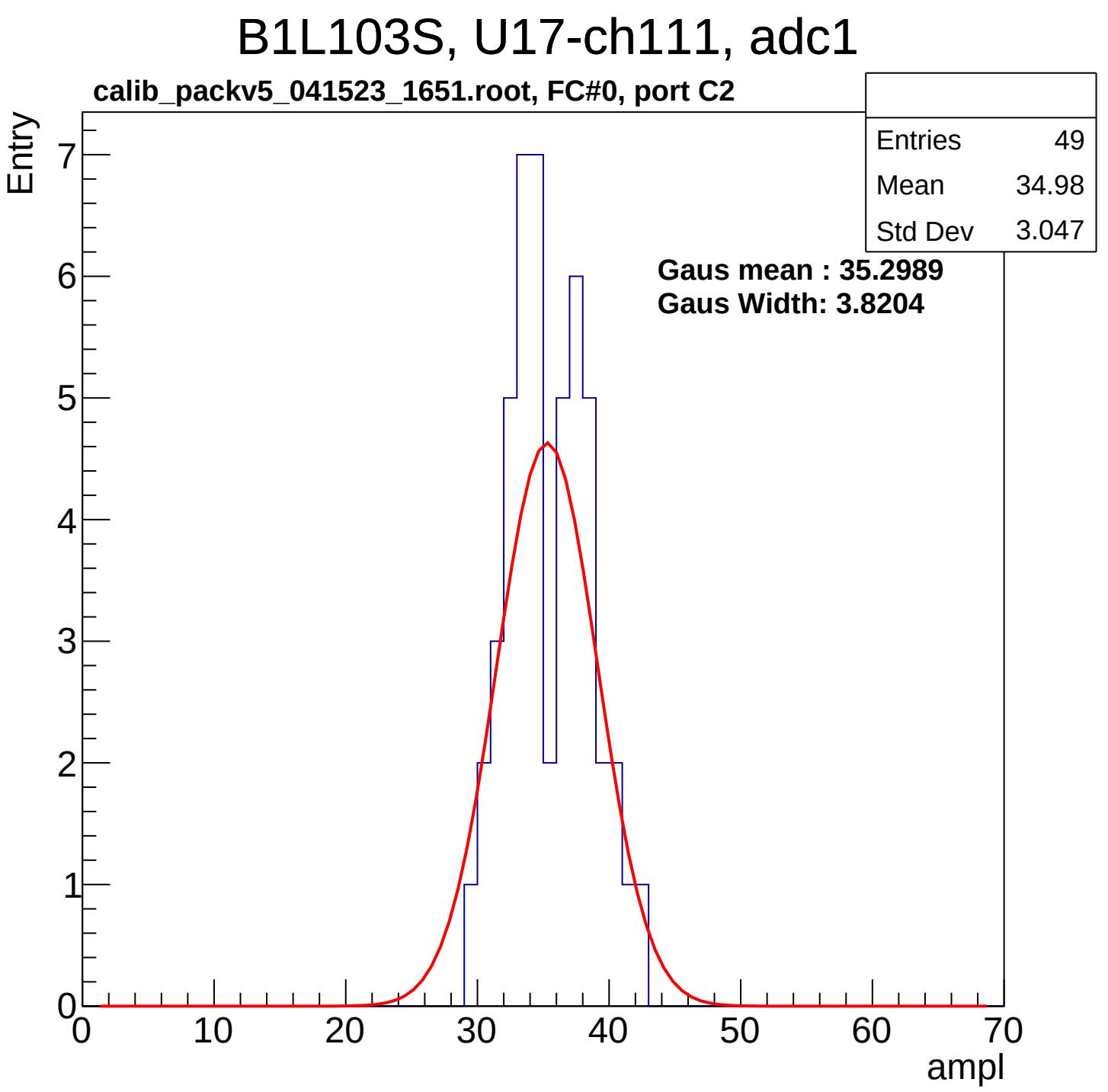

B1L103S, U17-ch110, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 54.4
Std Dev 3.306
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

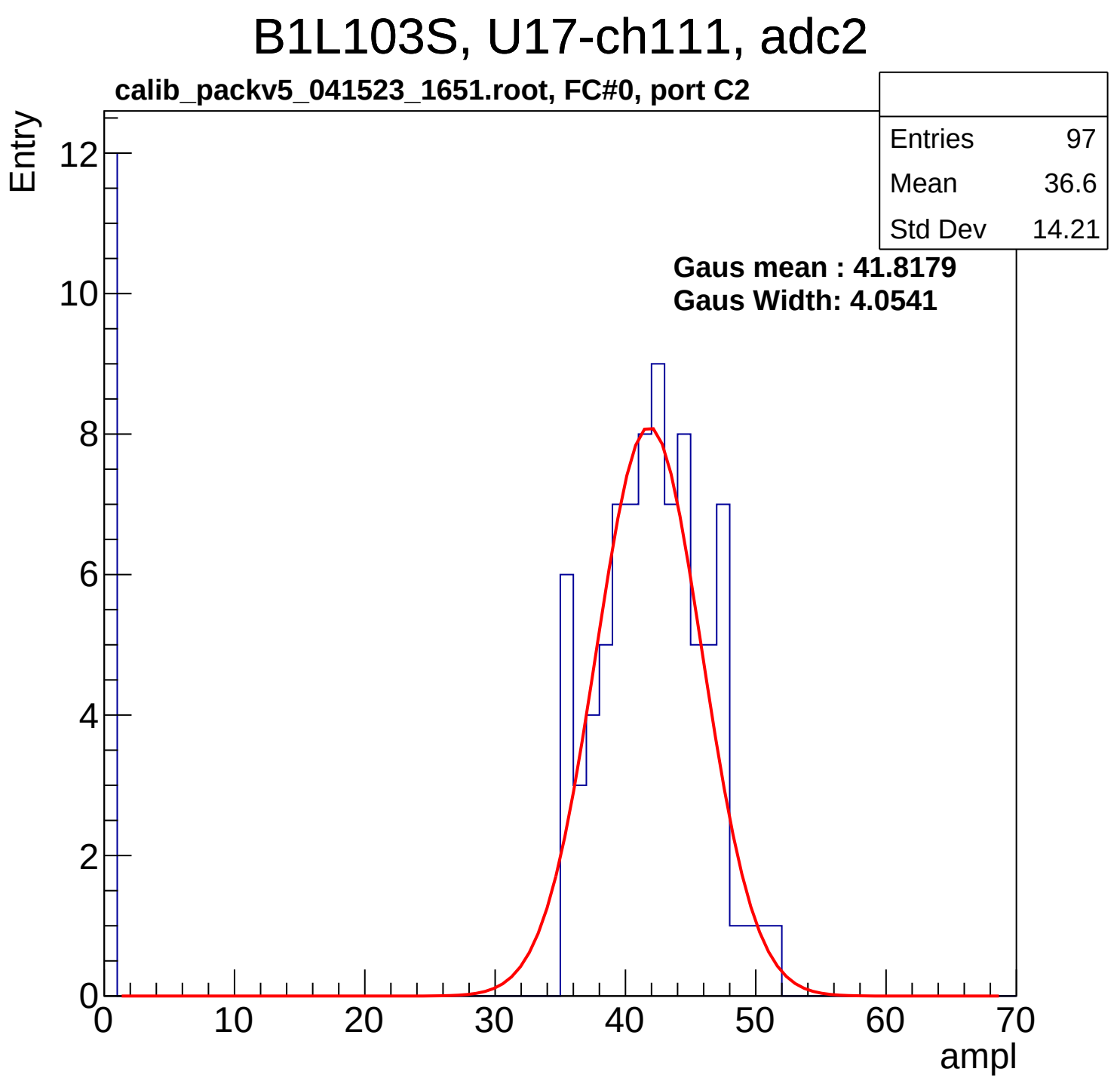

B1L103S, U17-ch110, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 58.57
Std Dev 2.411
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

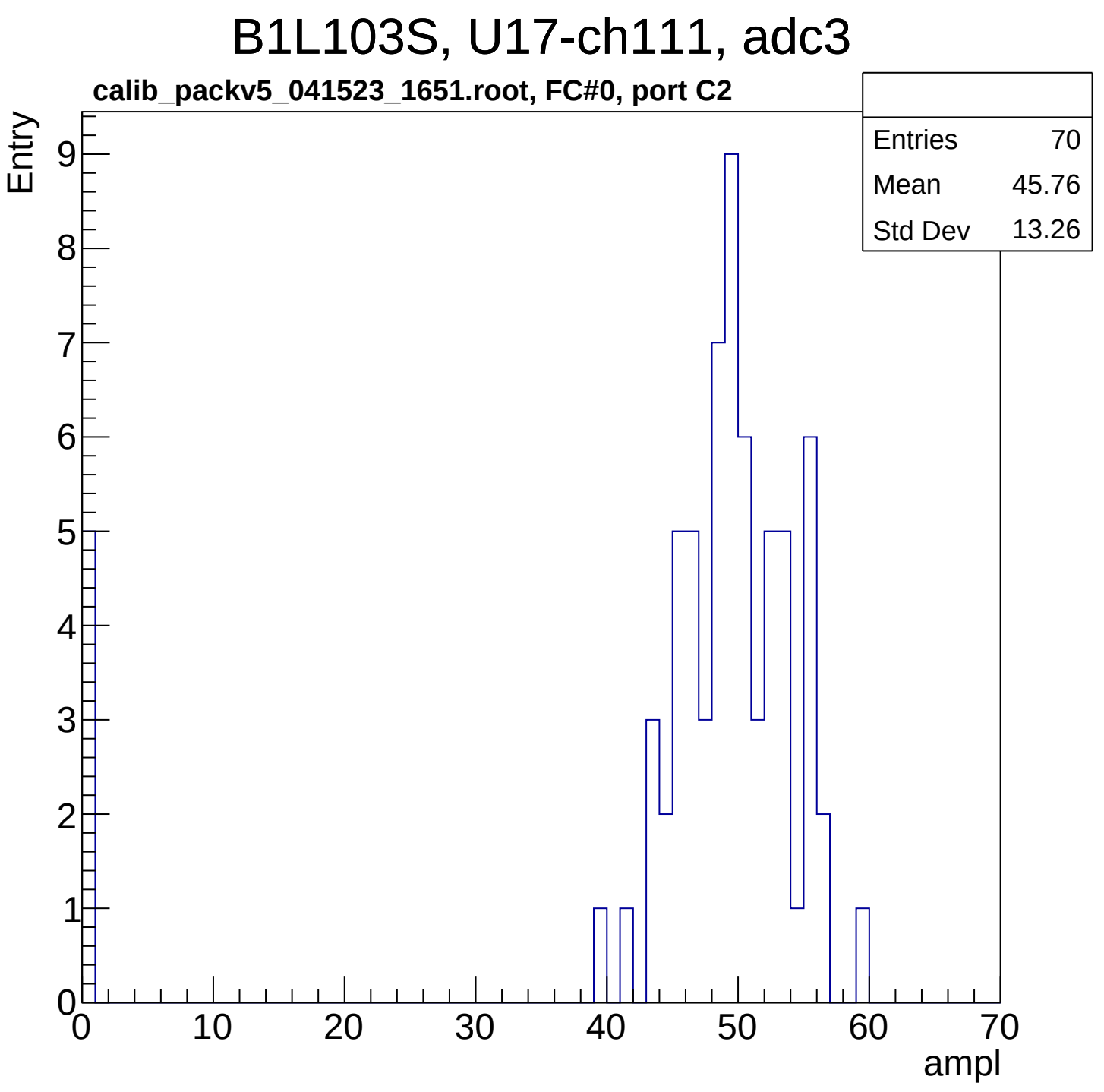

B1L103S, U17-ch110, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 58.81
Std Dev 11.71
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

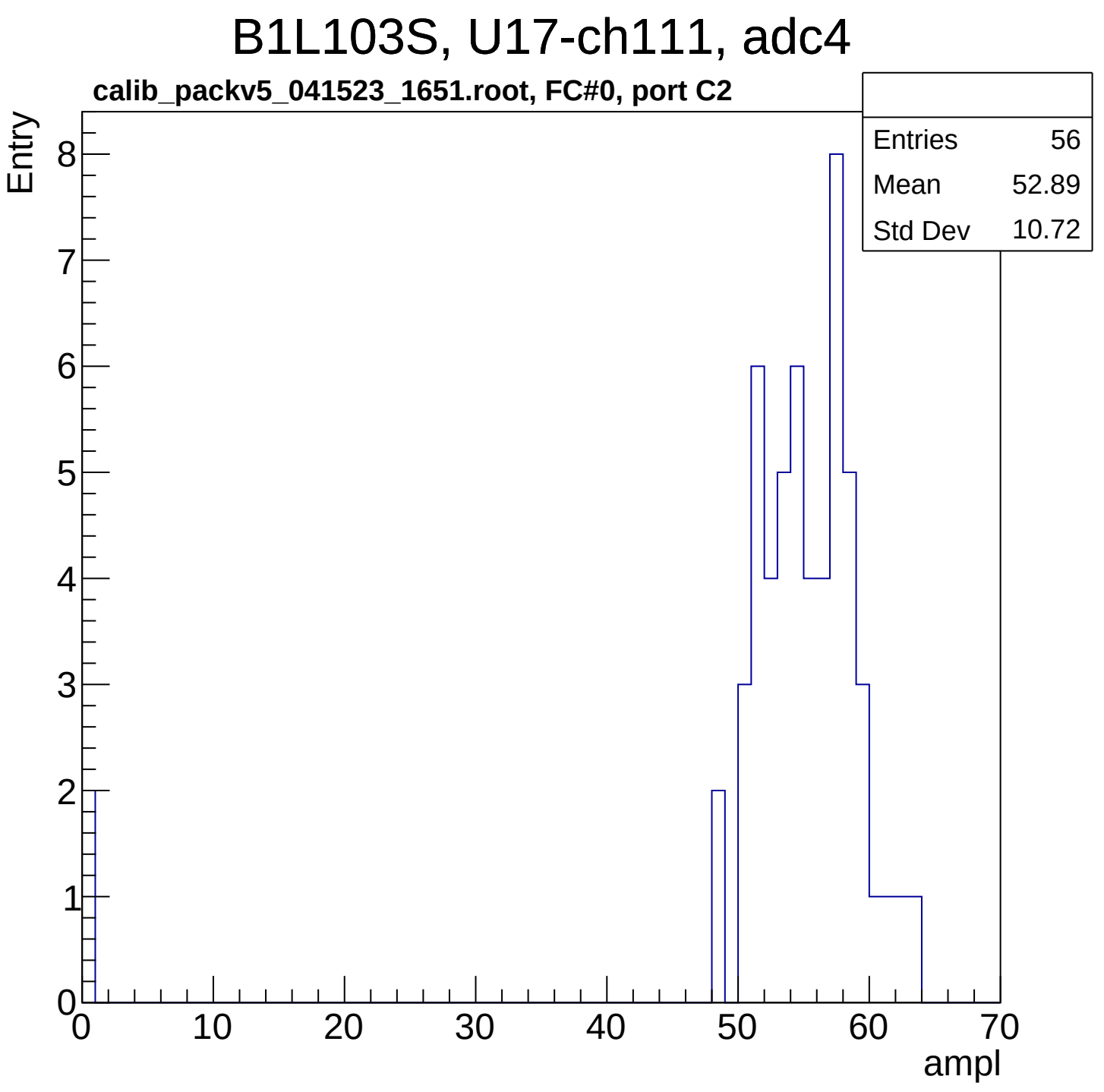

B1L103S, U17-ch110, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

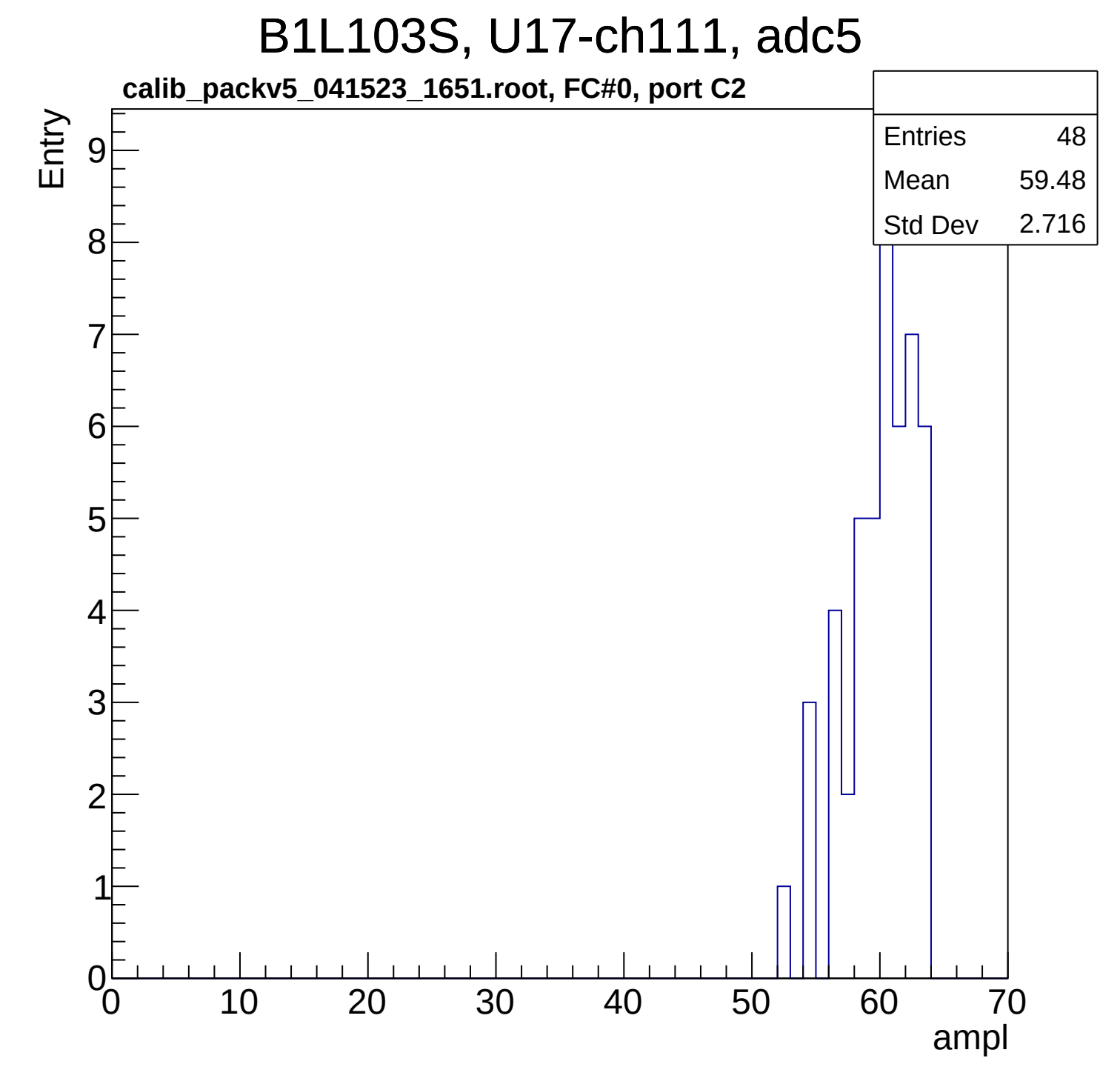

B1L103S, U17-ch111, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 22.73
Std Dev 11.72
Gaus mean : 28.8581
Gaus Width: 4.0670
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

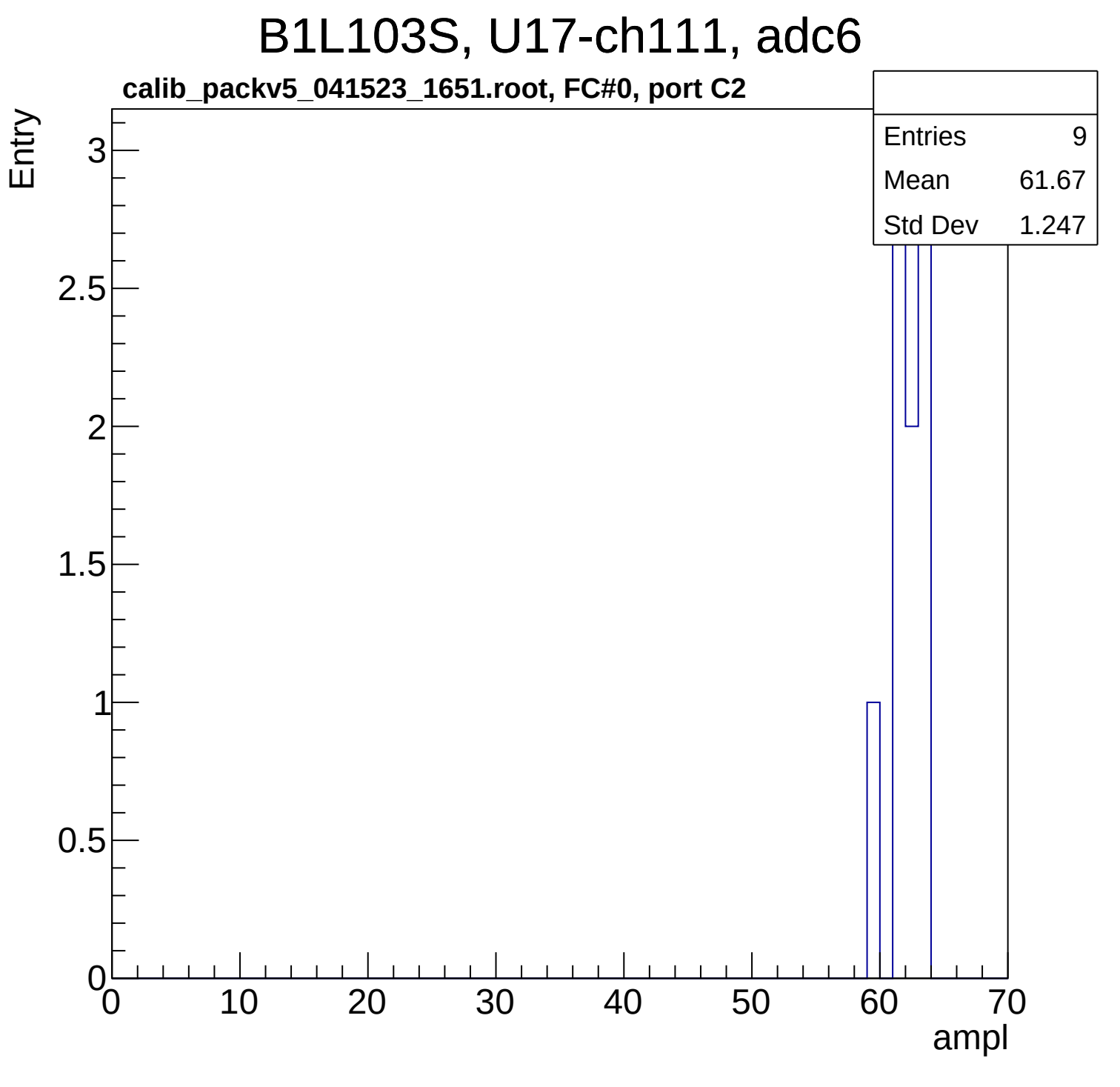

B1L103S, U17-ch111, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 34.98
Std Dev 3.047
Gaus mean : 35.2989
Gaus Width: 3.8204
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

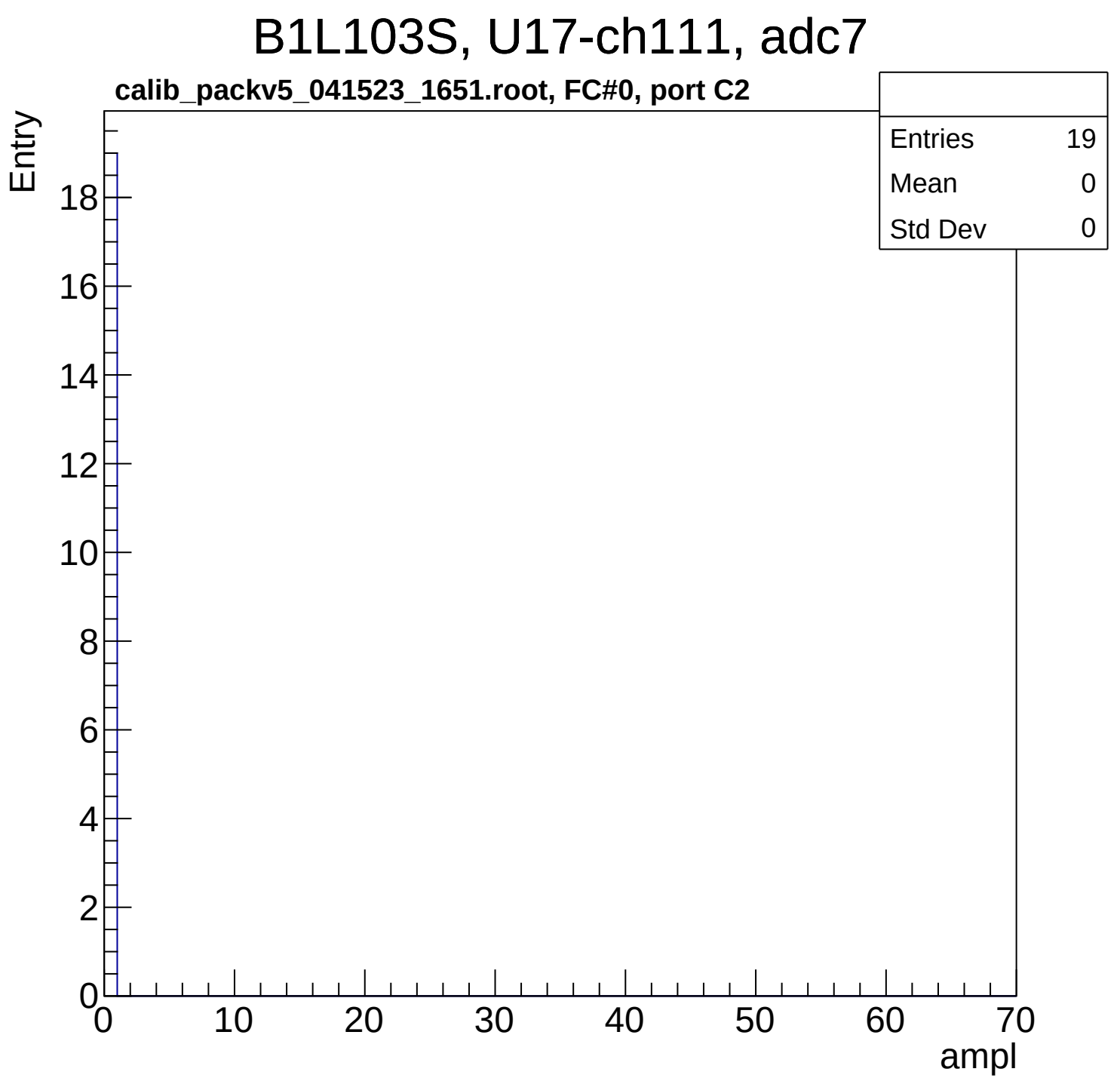

B1L103S, U17-ch111, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 36.6
Std Dev 14.21
Gaus mean : 41.8179
Gaus Width: 4.0541
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

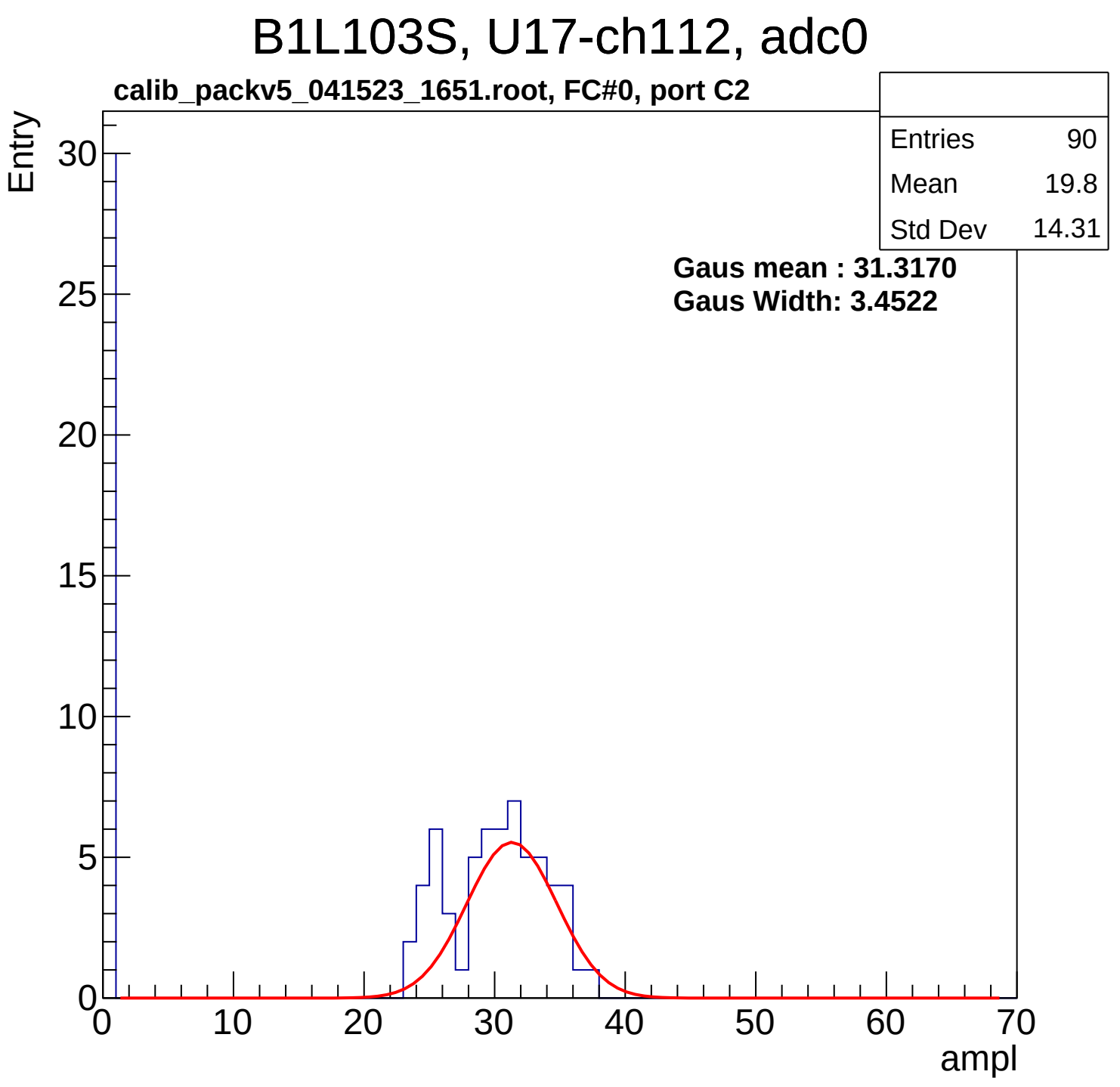

B1L103S, U17-ch111, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 45.76
Std Dev 13.26
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

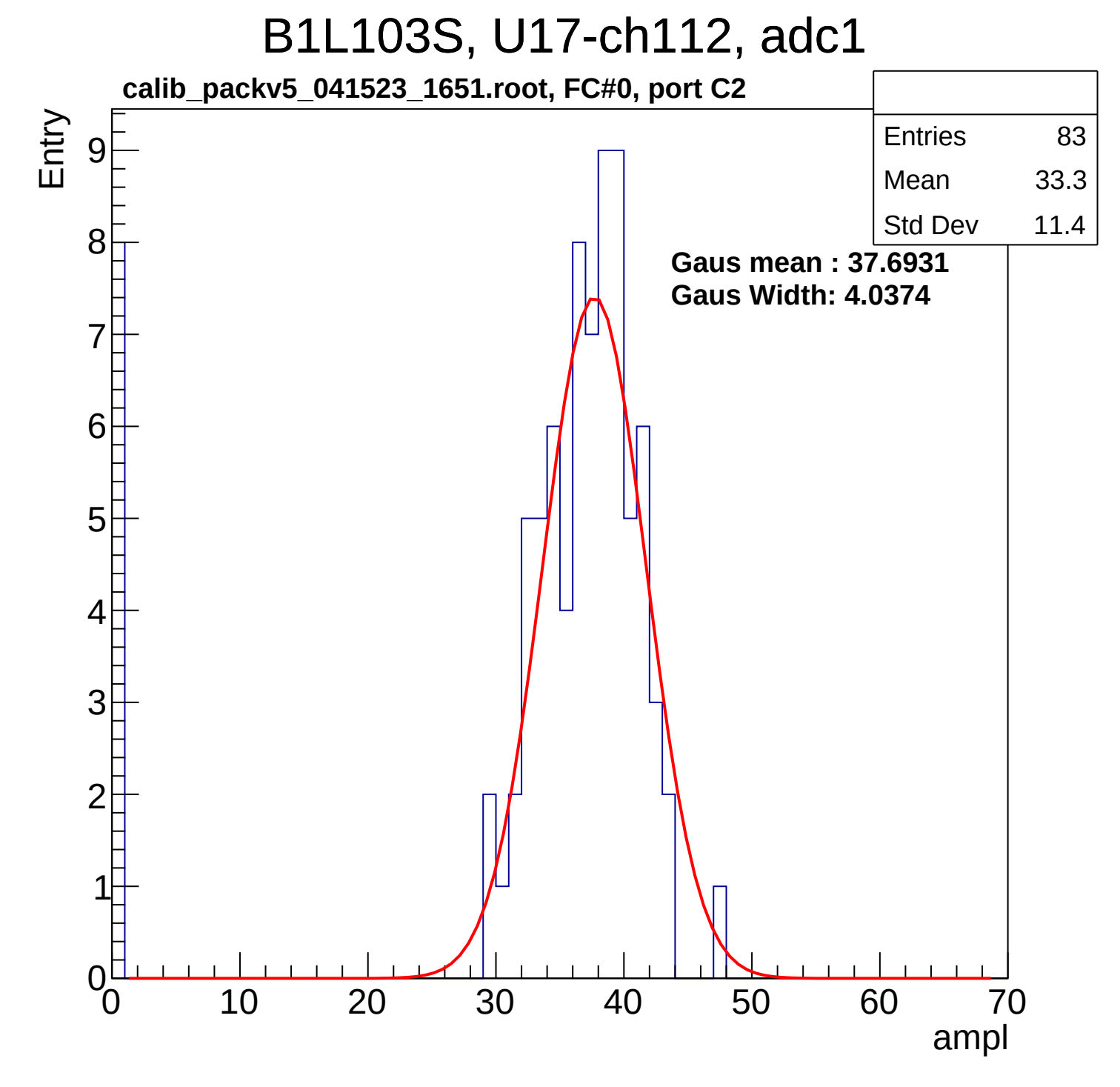

B1L103S, U17-ch111, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 52.89
Std Dev 10.72
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

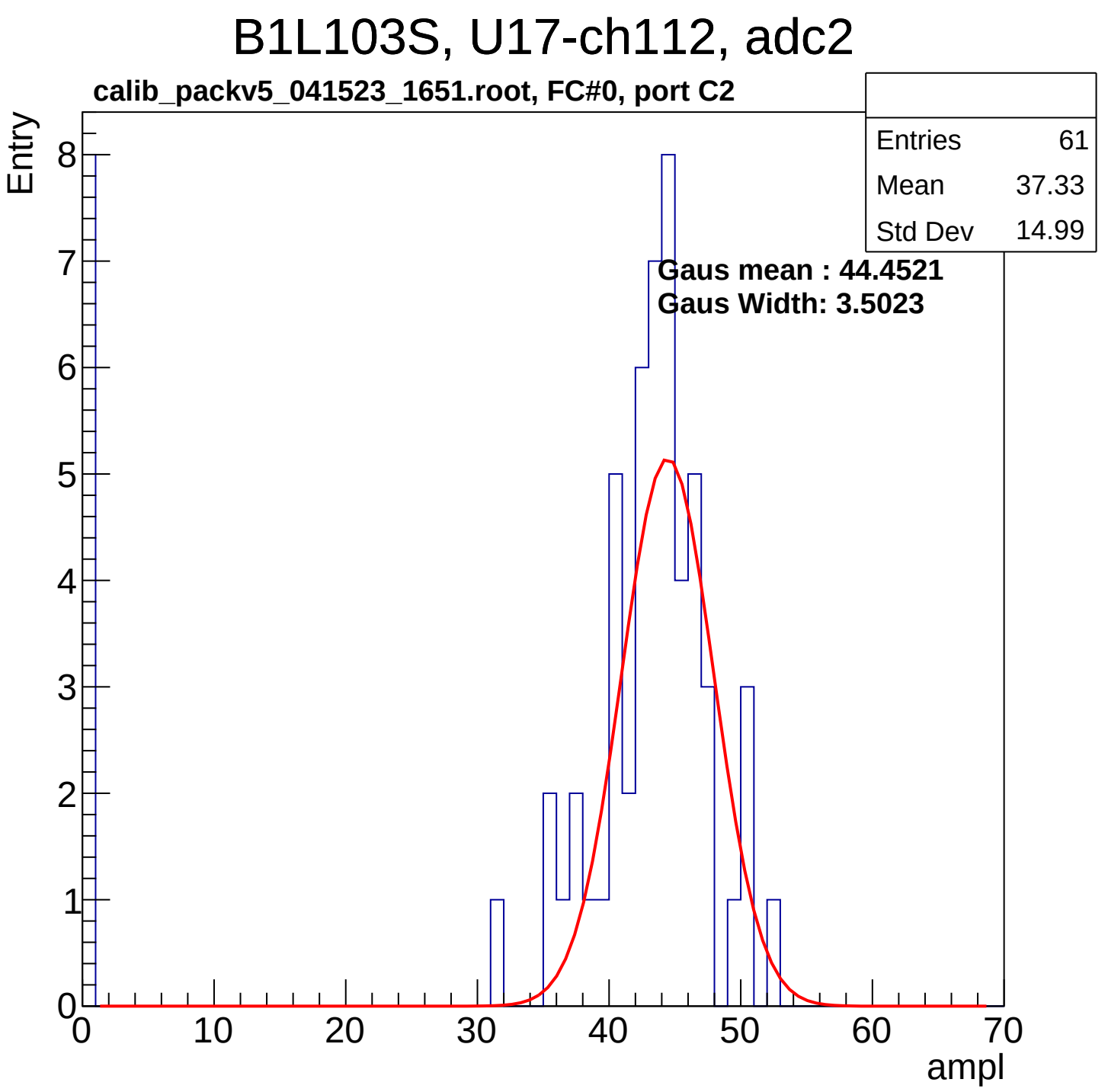

B1L103S, U17-ch111, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 59.48
Std Dev 2.716
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

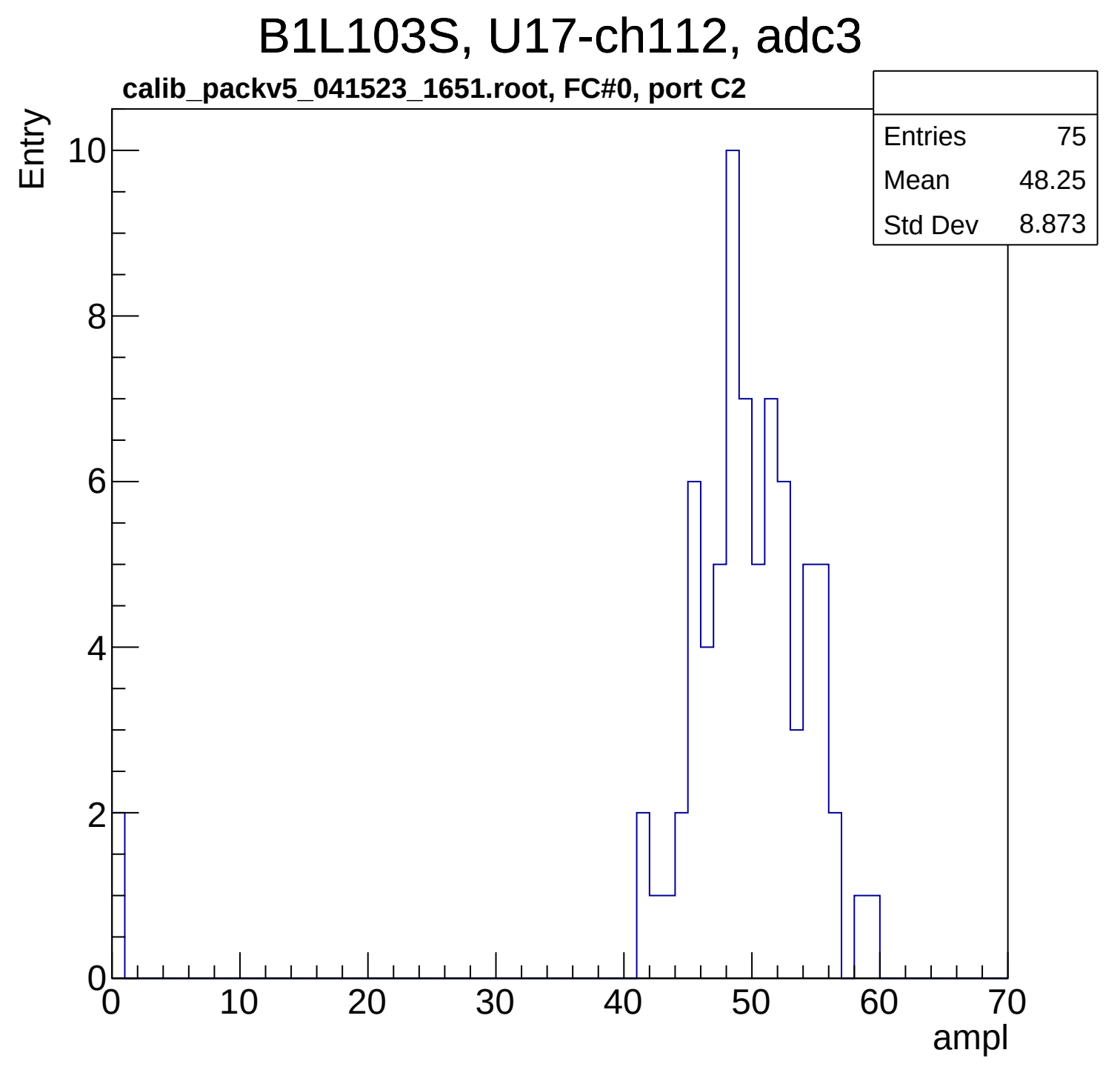

B1L103S, U17-ch111, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.67
Std Dev 1.247
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

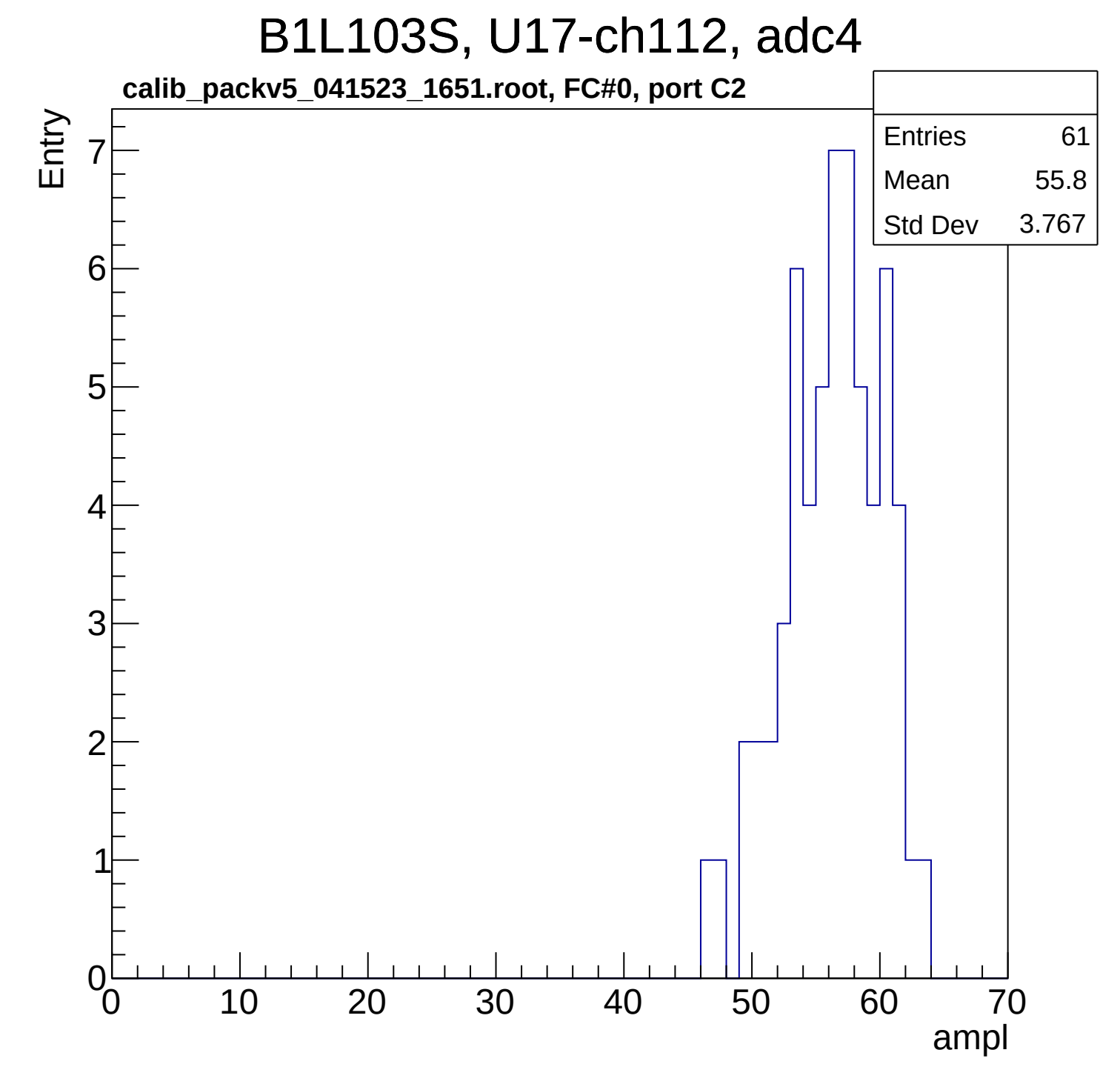

B1L103S, U17-ch111, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

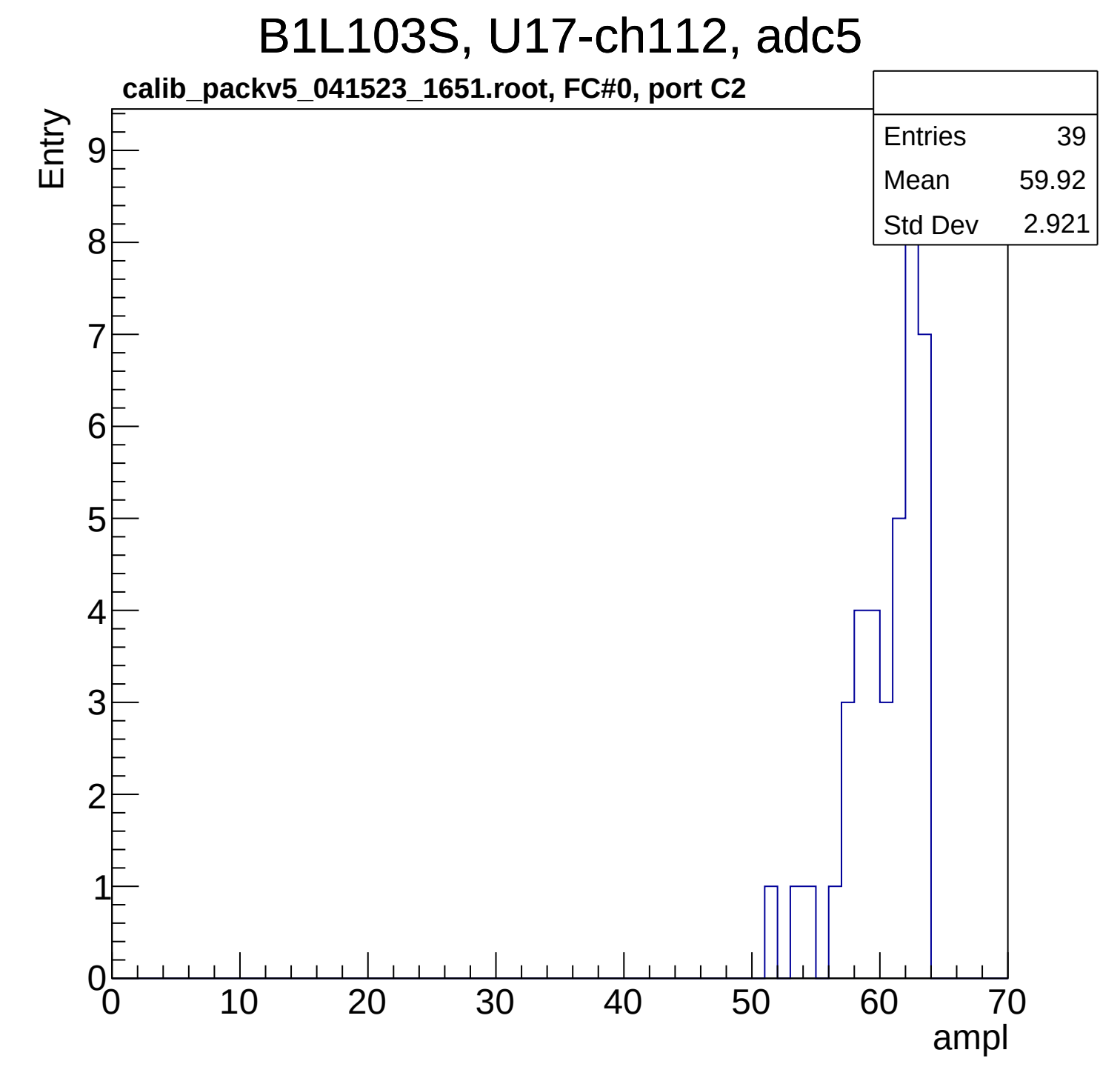

B1L103S, U17-ch112, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 19.8
Std Dev 14.31
Gaus mean : 31.3170
Gaus Width: 3.4522
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70

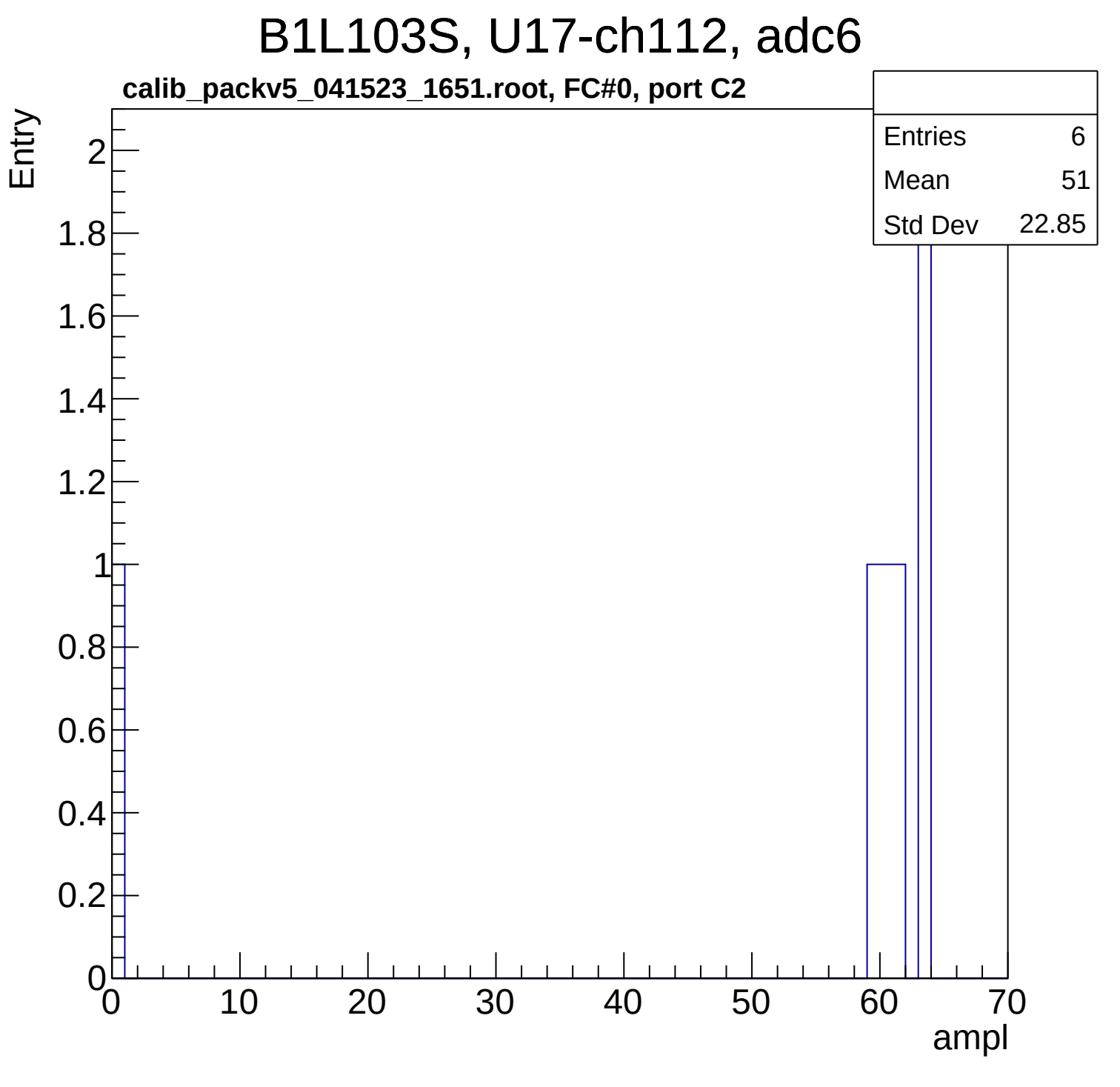

B1L103S, U17-ch112, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 33.3
Std Dev 11.4
Gaus mean : 37.6931
Gaus Width: 4.0374
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

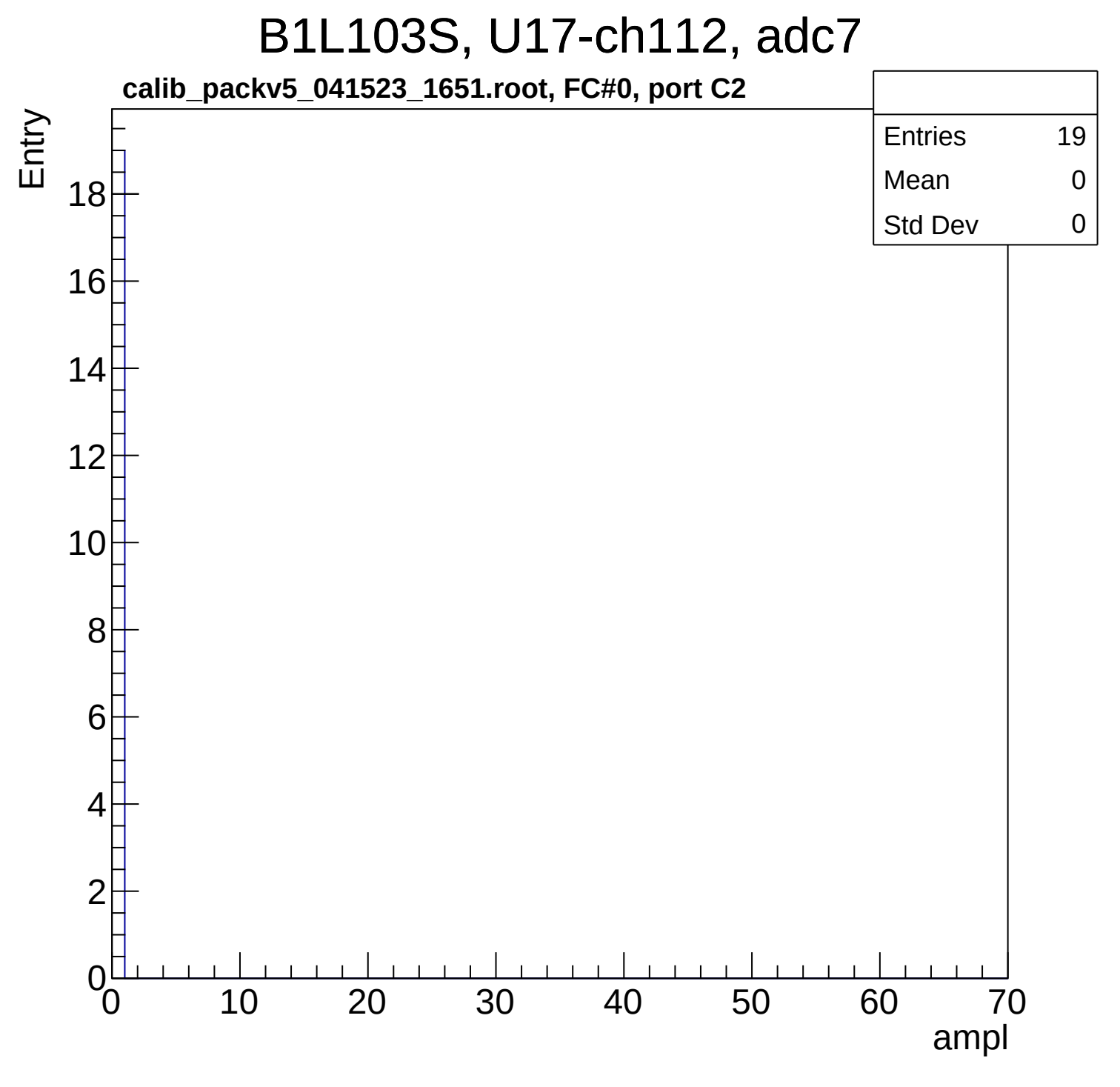

B1L103S, U17-ch112, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 37.33
Std Dev 14.99
Gaus mean : 44.4521
Gaus Width: 3.5023
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

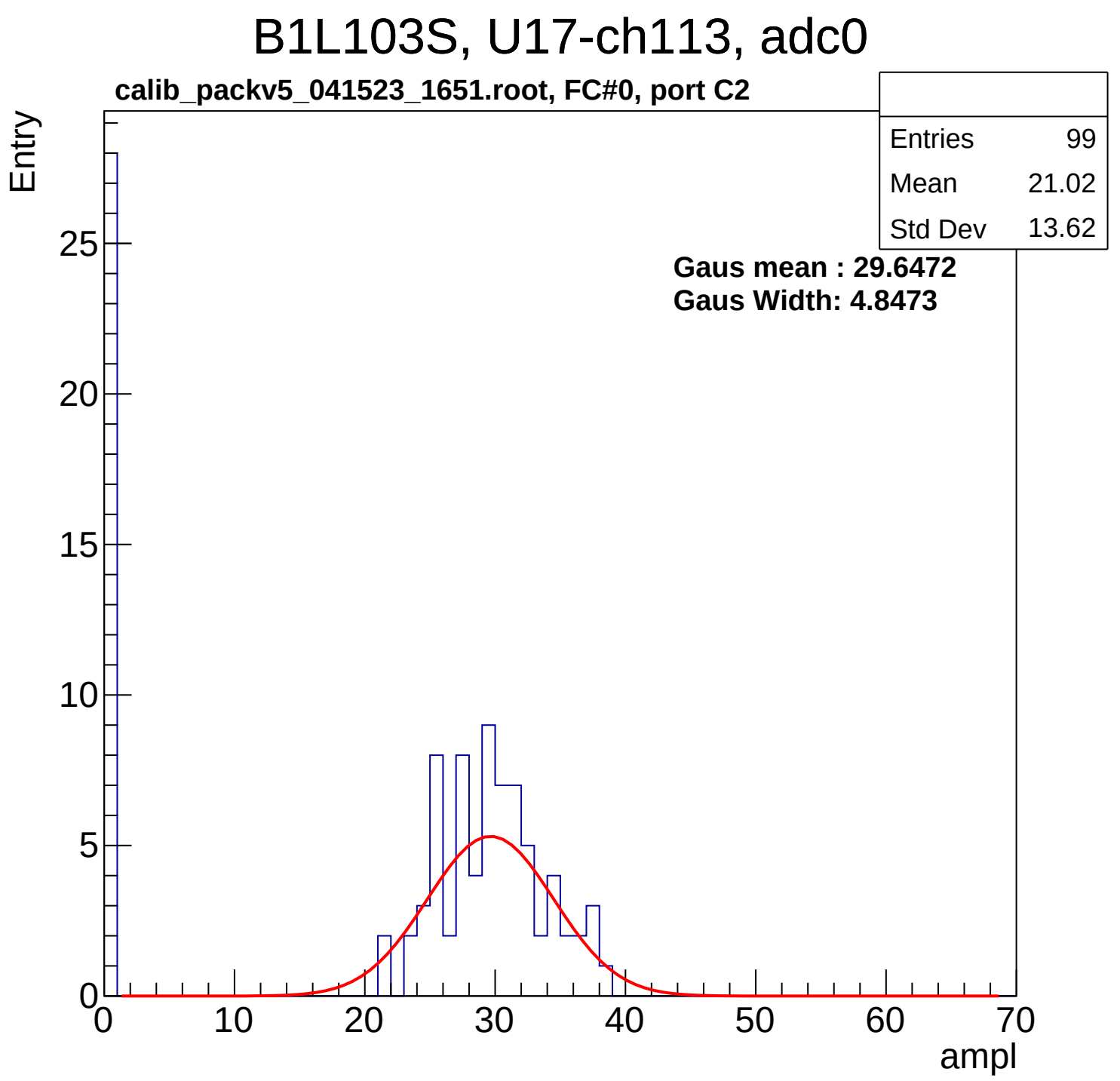

B1L103S, U17-ch112, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 48.25
Std Dev 8.873
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

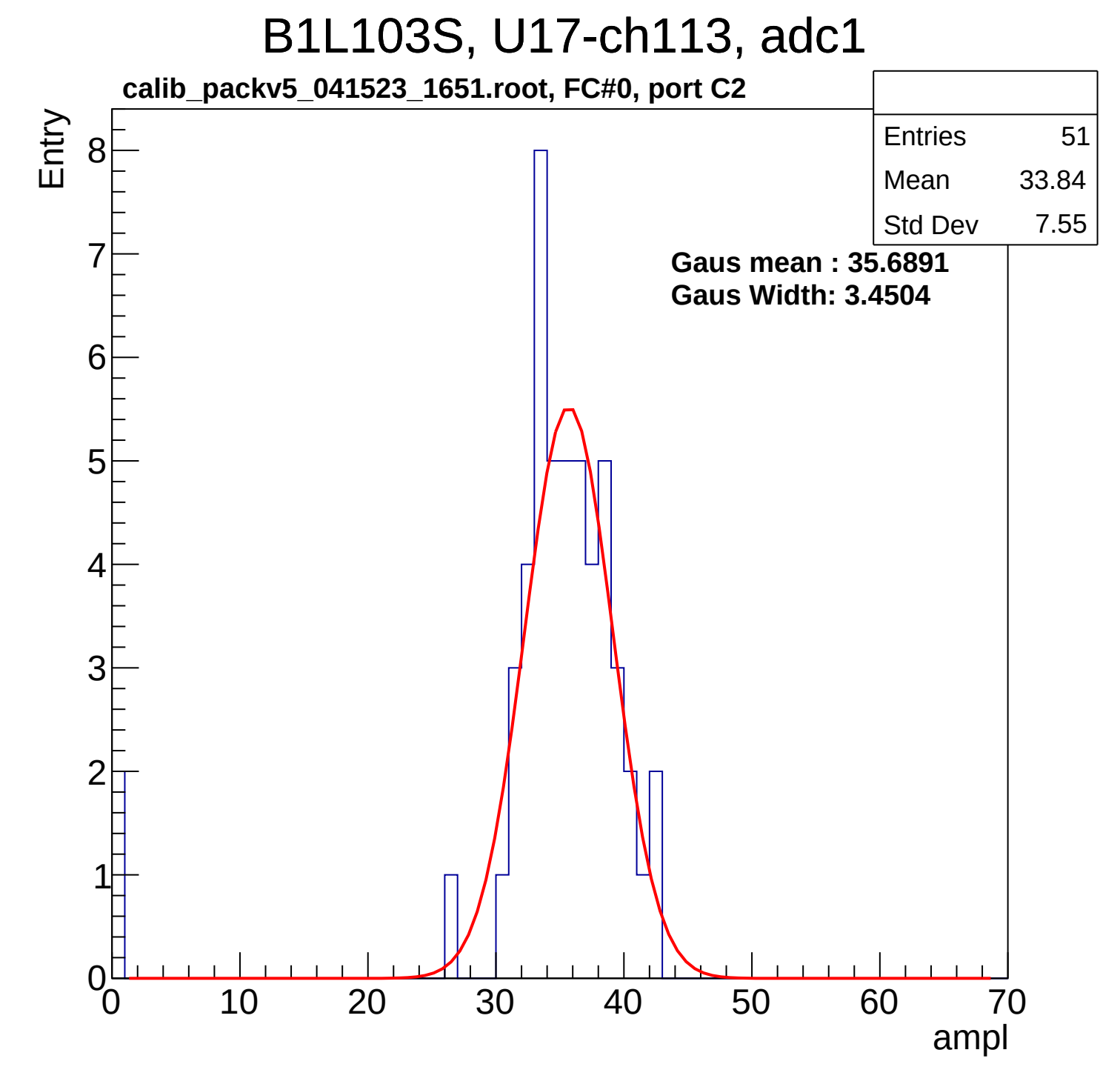

B1L103S, U17-ch112, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 55.8
Std Dev 3.767
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

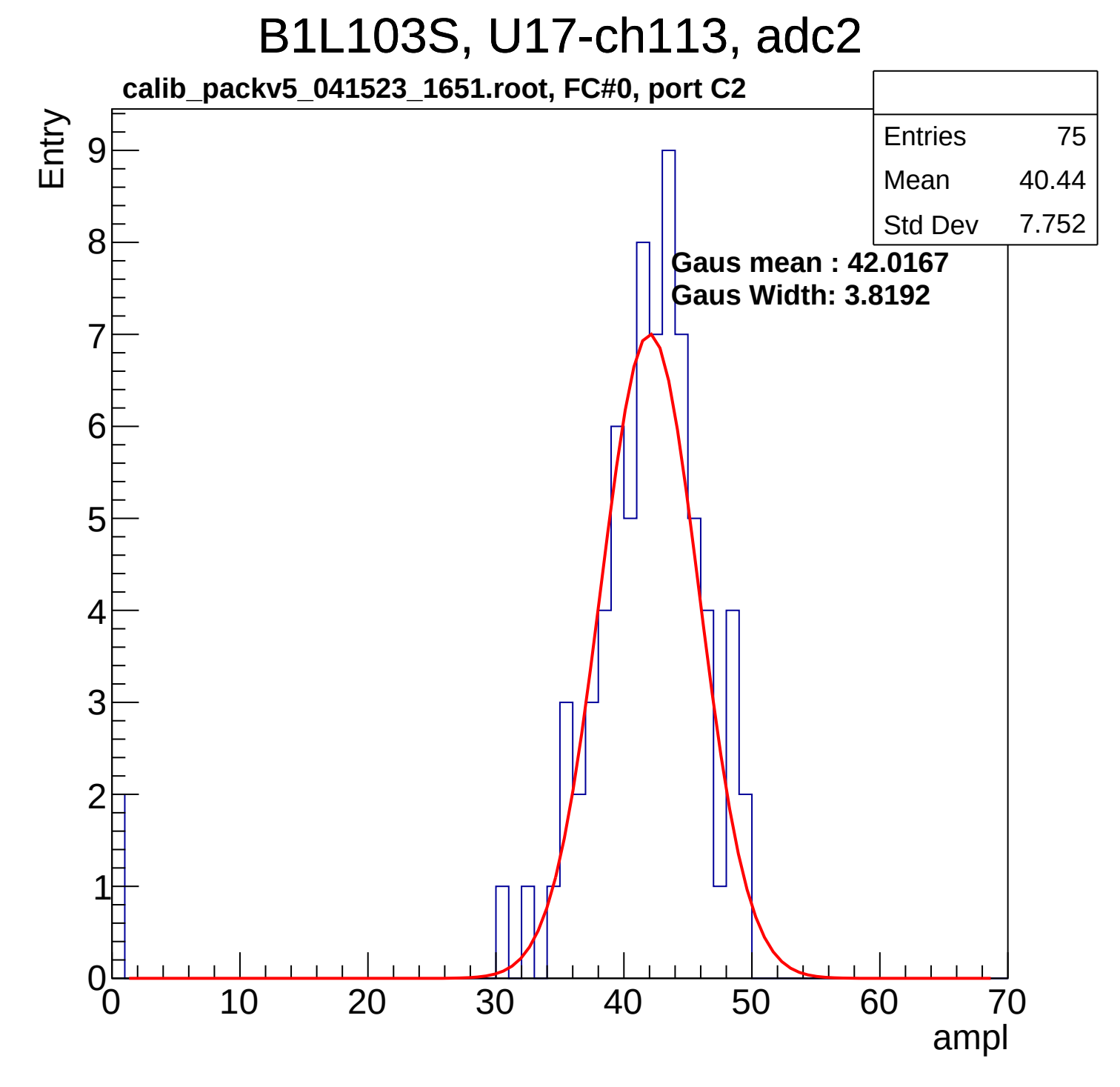

B1L103S, U17-ch112, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 59.92
Std Dev 2.921
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

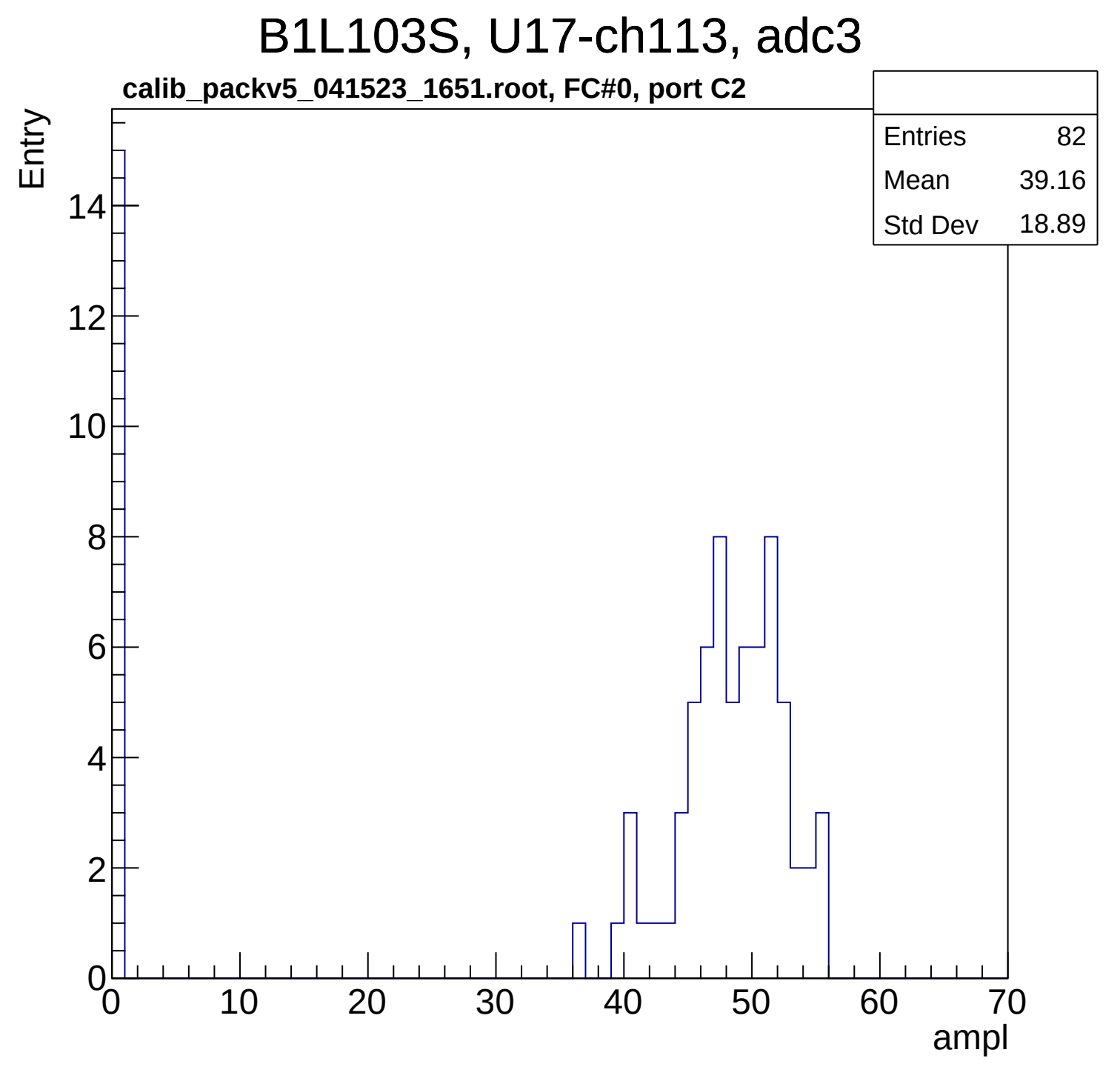

B1L103S, U17-ch112, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 51
Std Dev 22.85
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

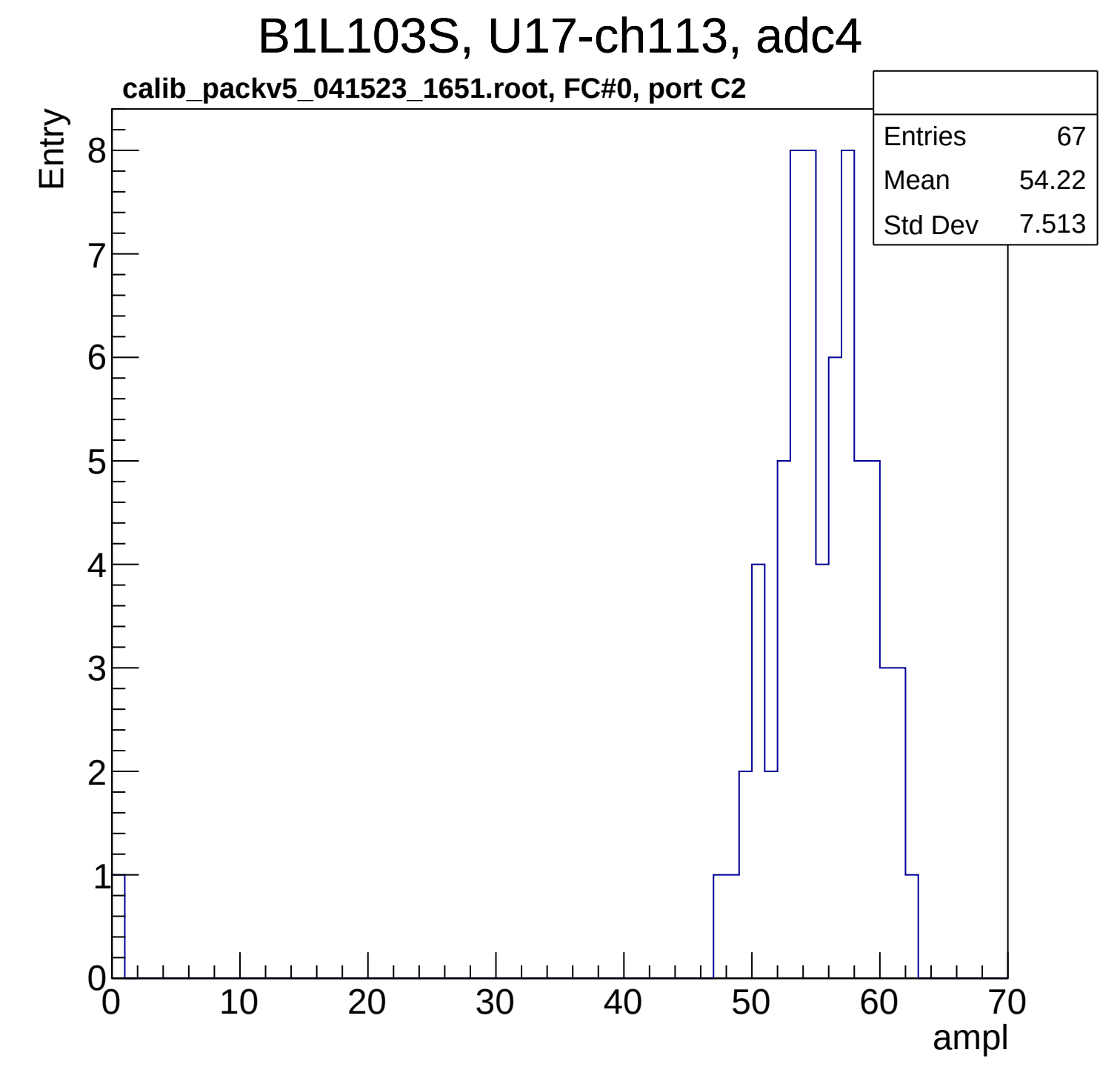

B1L103S, U17-ch112, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

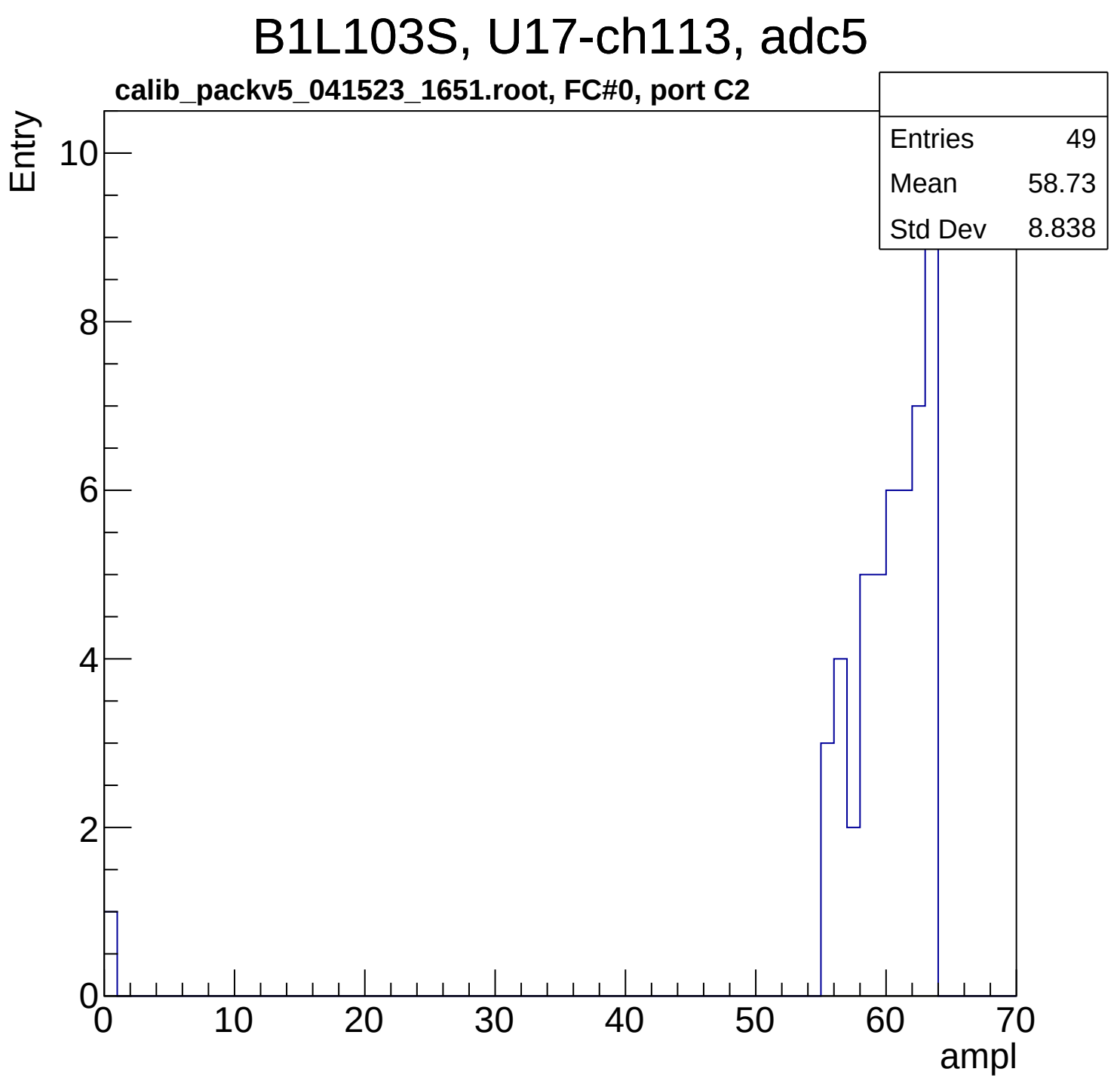

B1L103S, U17-ch113, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 21.02
Std Dev 13.62
Gaus mean : 29.6472
Gaus Width: 4.8473
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70

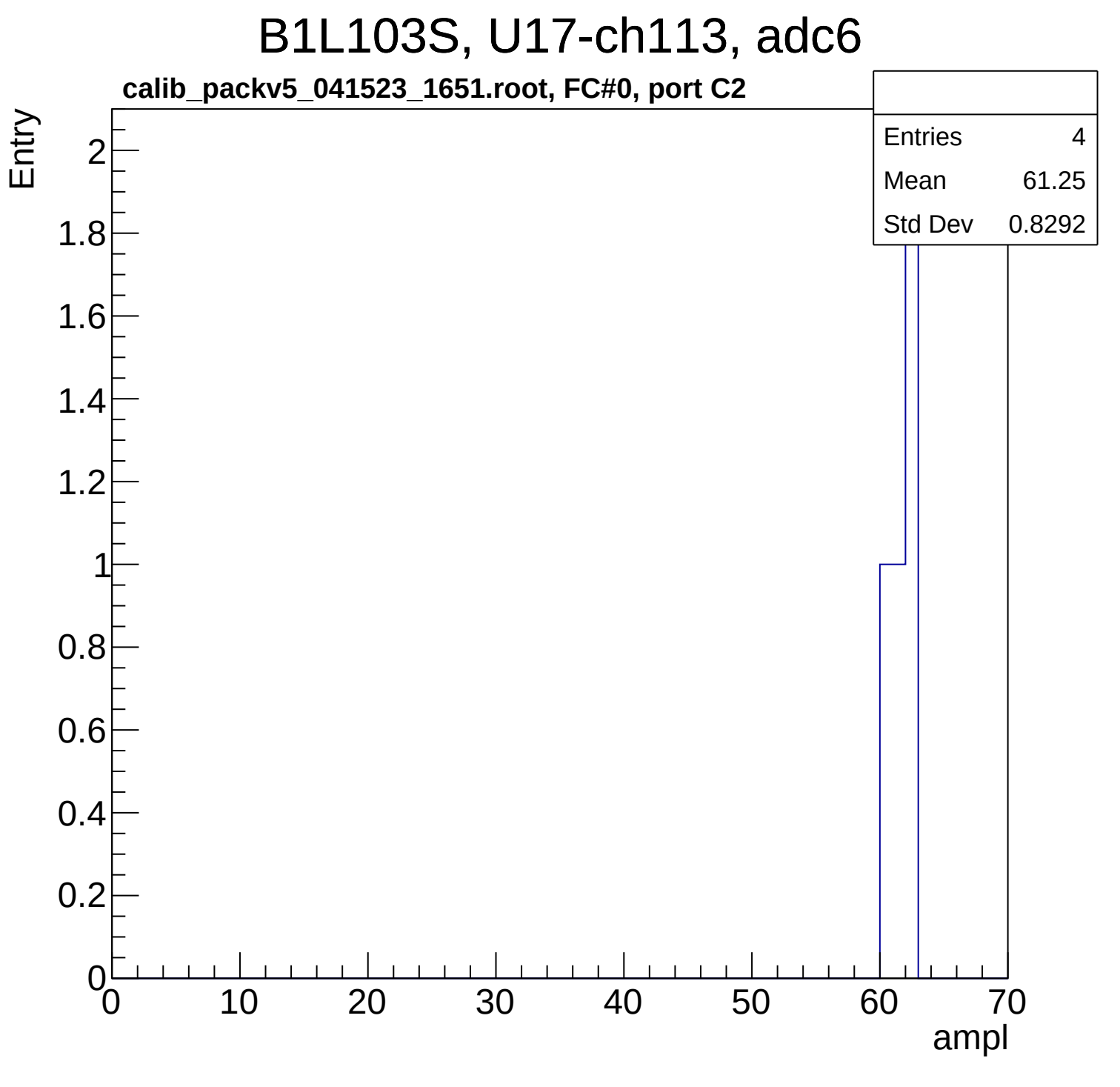

B1L103S, U17-ch113, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 33.84
Std Dev 7.55
Gaus mean : 35.6891
Gaus Width: 3.4504
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

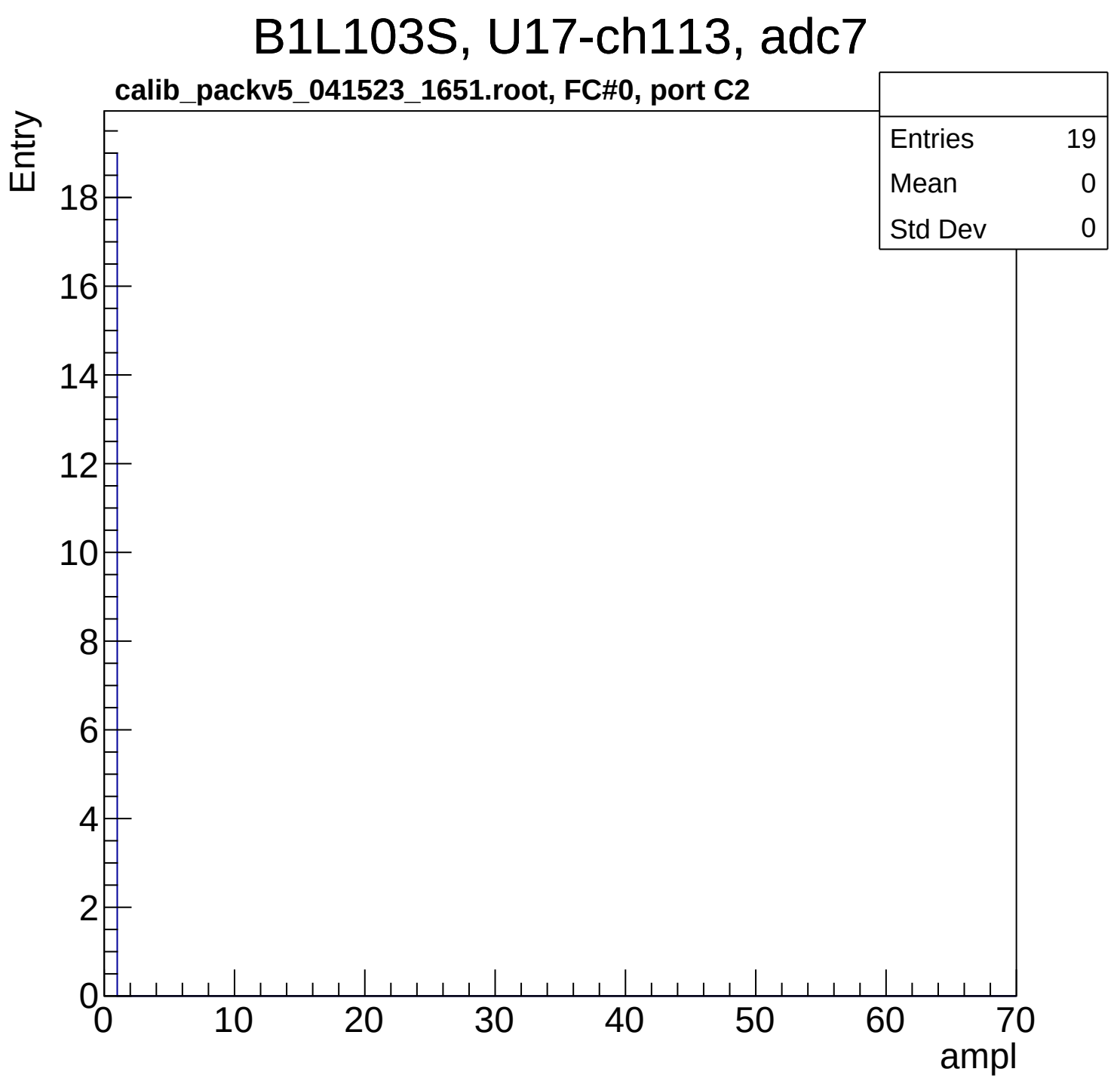

B1L103S, U17-ch113, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 40.44
Std Dev 7.752
Gaus mean : 42.0167
Gaus Width: 3.8192
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

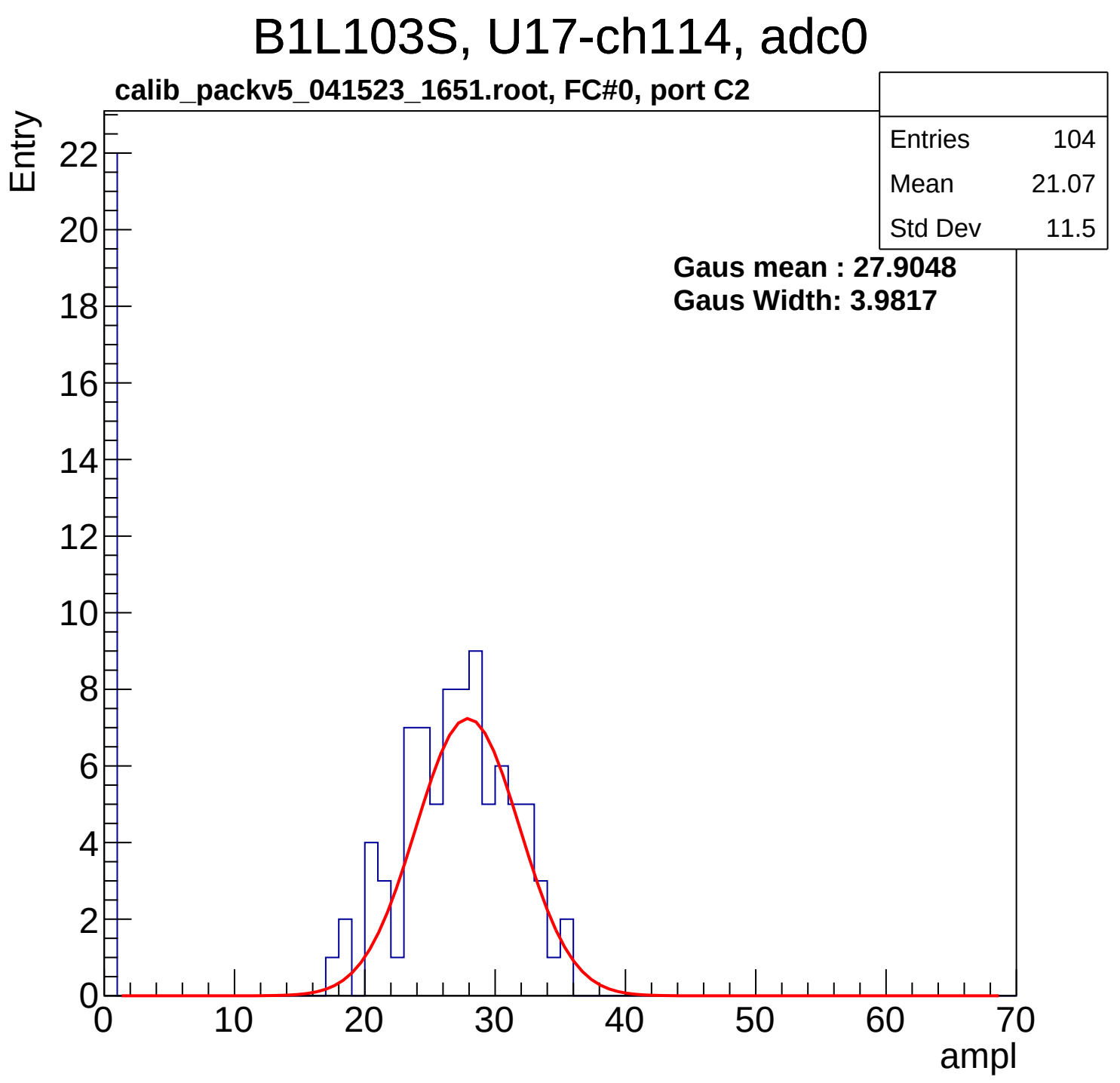

B1L103S, U17-ch113, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 39.16
Std Dev 18.89
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

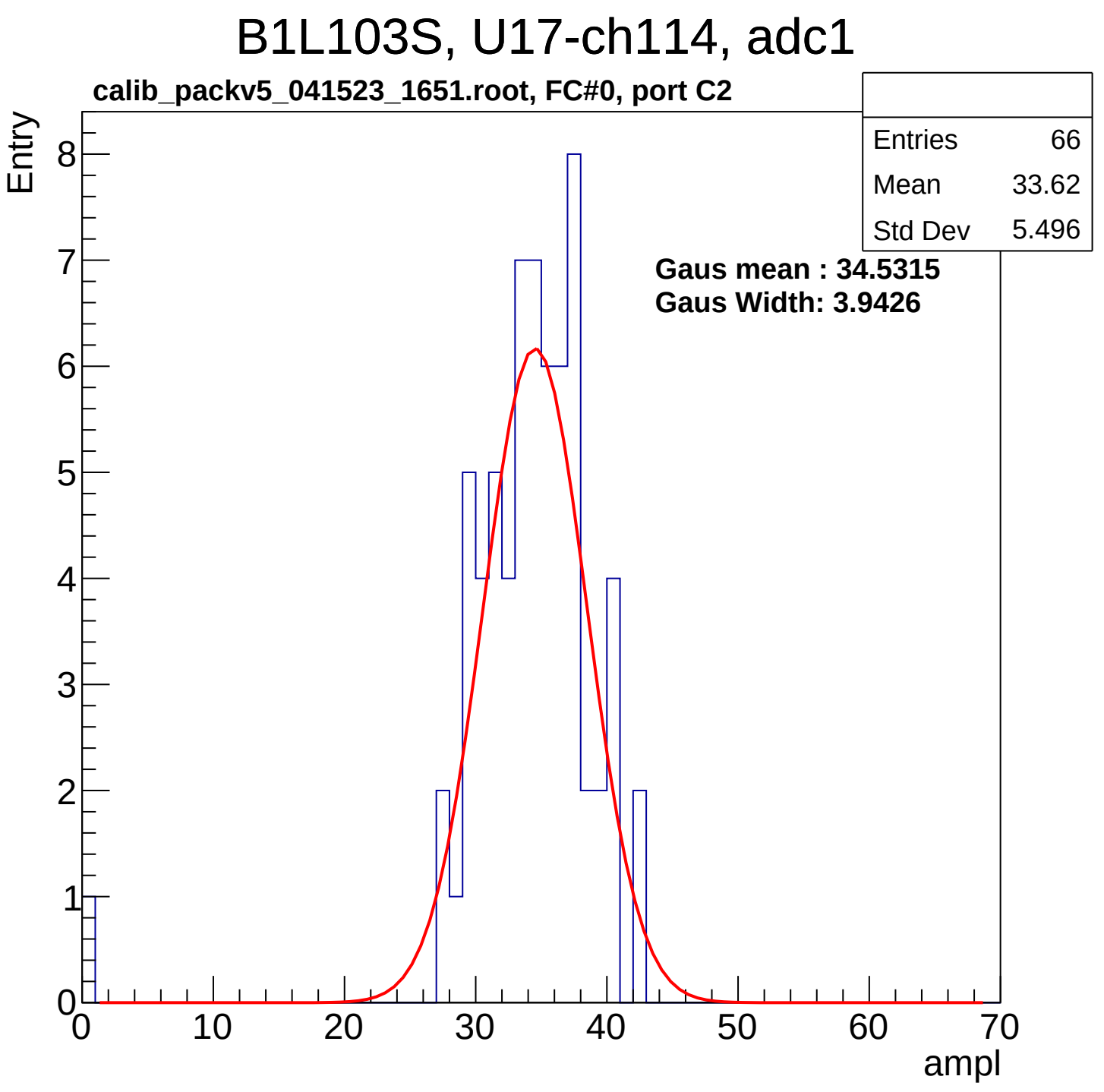

B1L103S, U17-ch113, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 54.22
Std Dev 7.513
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

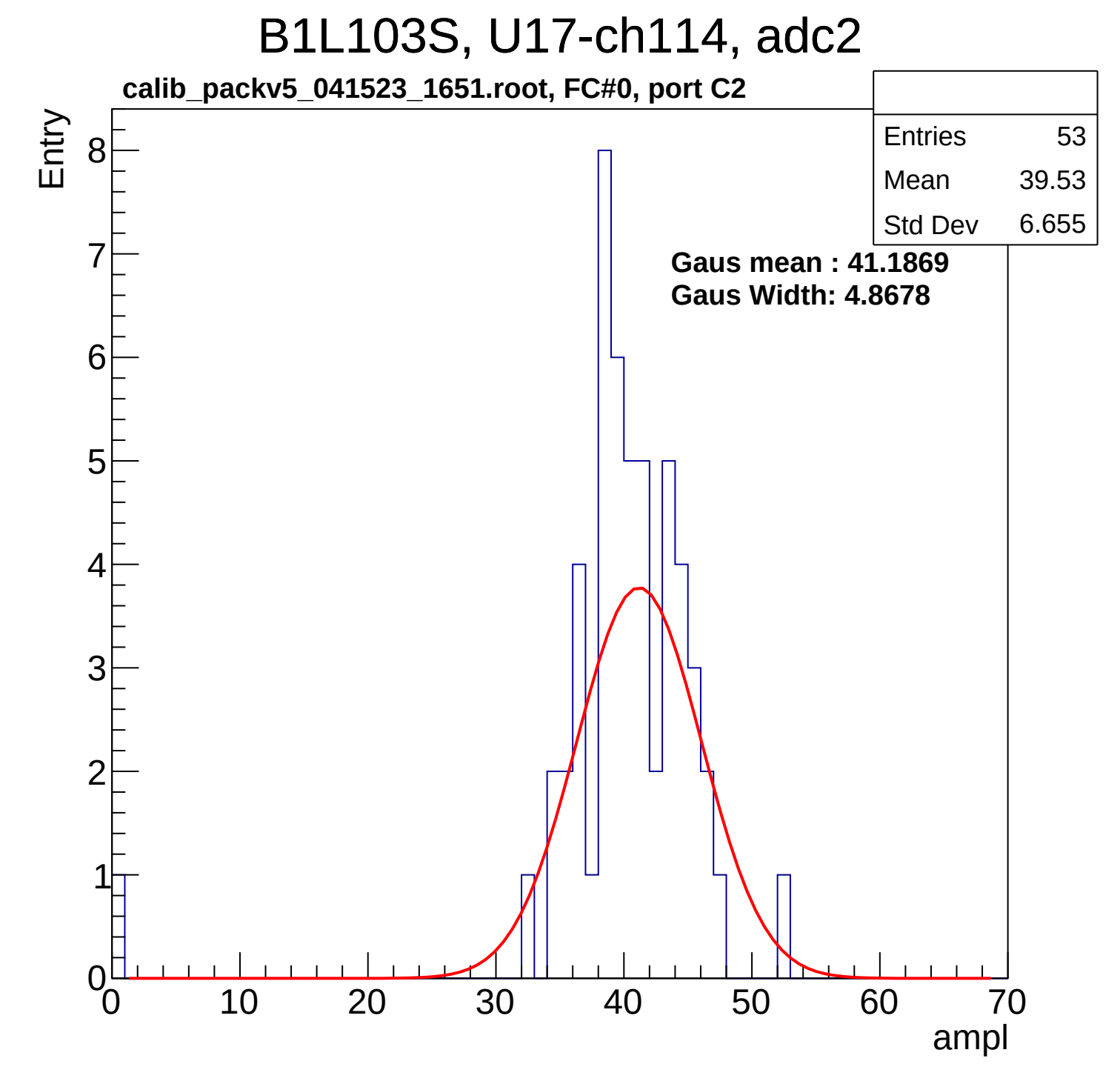

B1L103S, U17-ch113, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.73
Std Dev 8.838
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

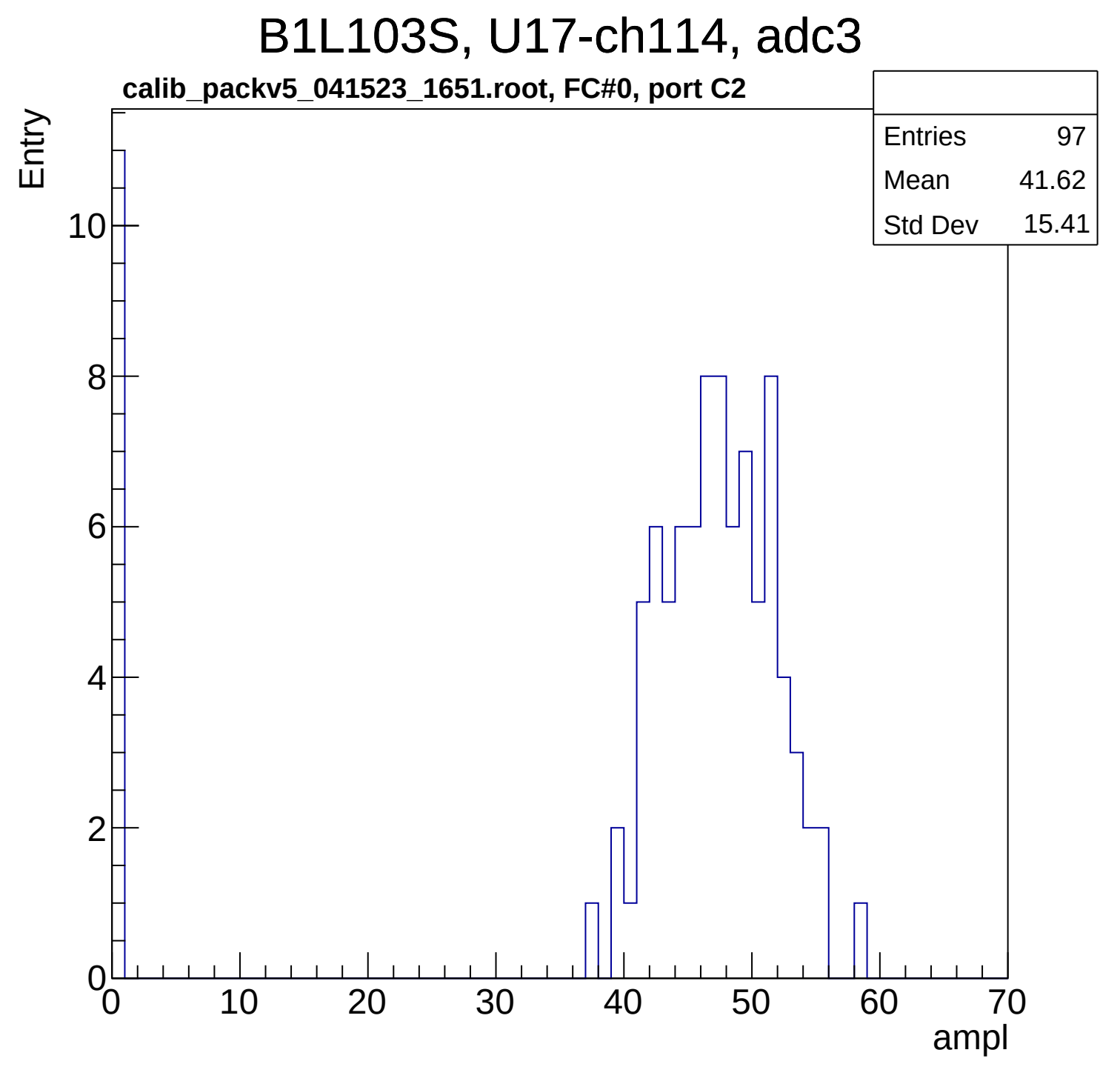

B1L103S, U17-ch113, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

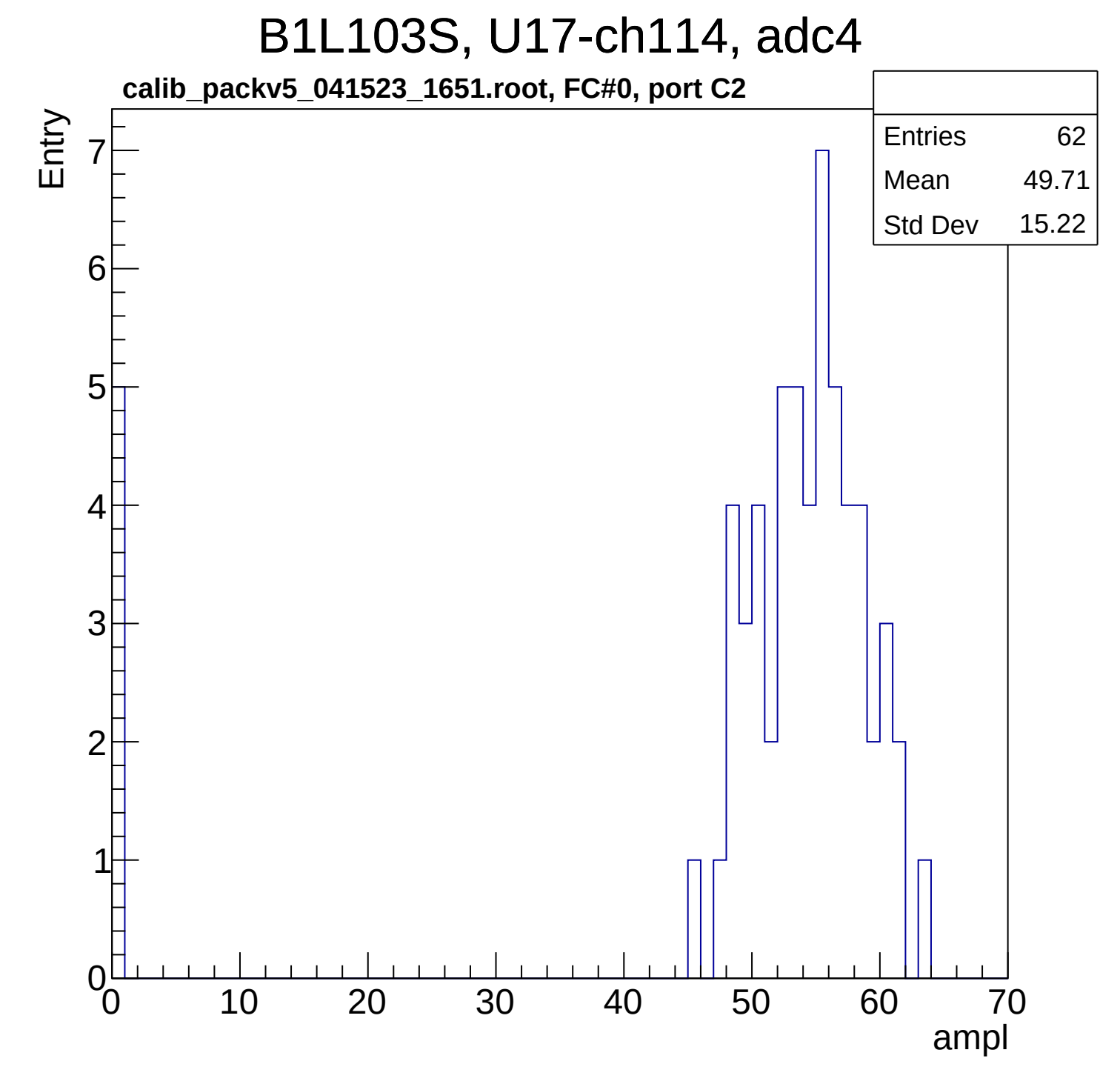

B1L103S, U17-ch113, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

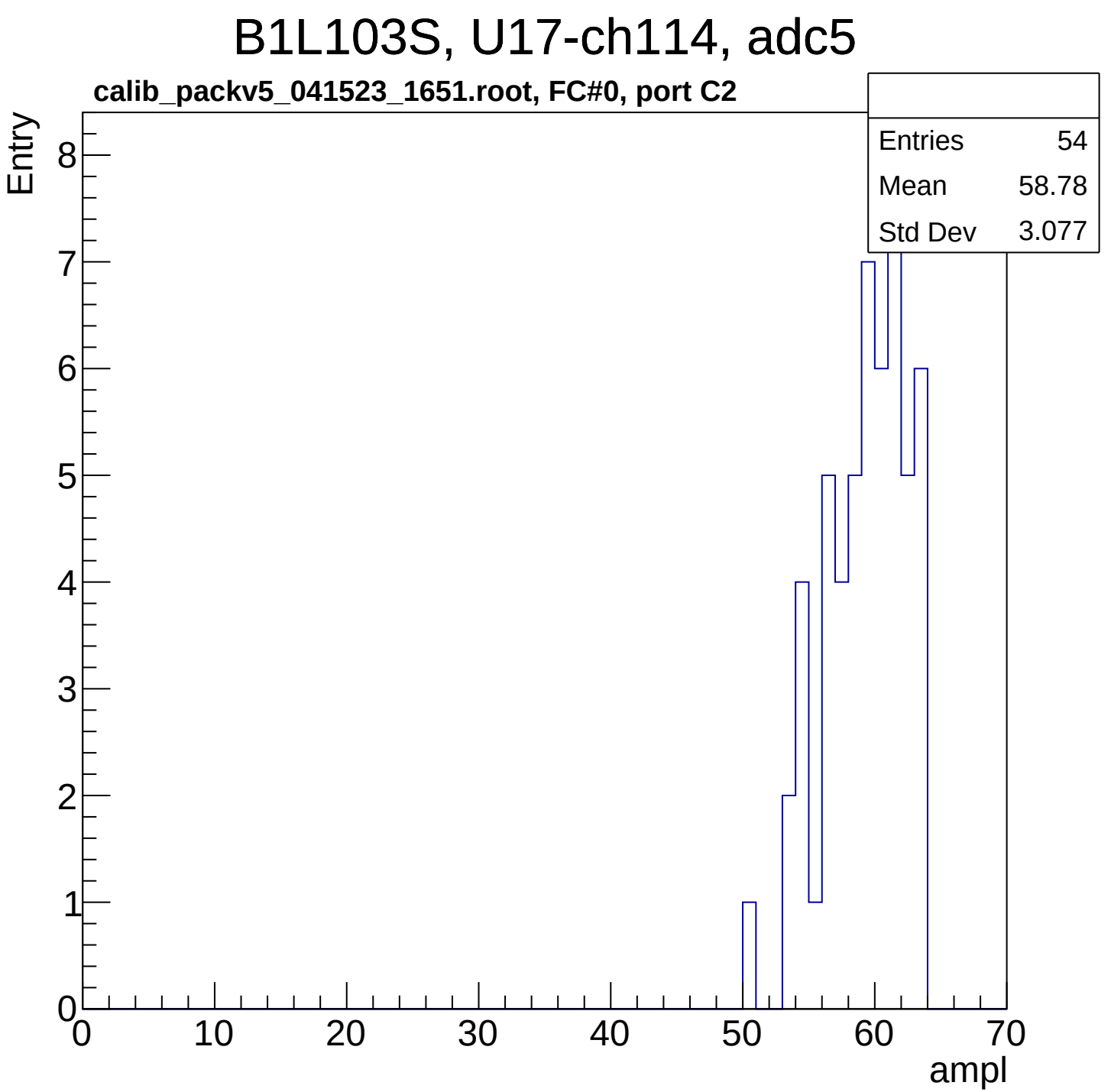

B1L103S, U17-ch114, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 21.07
Std Dev 11.5
Gaus mean : 27.9048
Gaus Width: 3.9817
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70

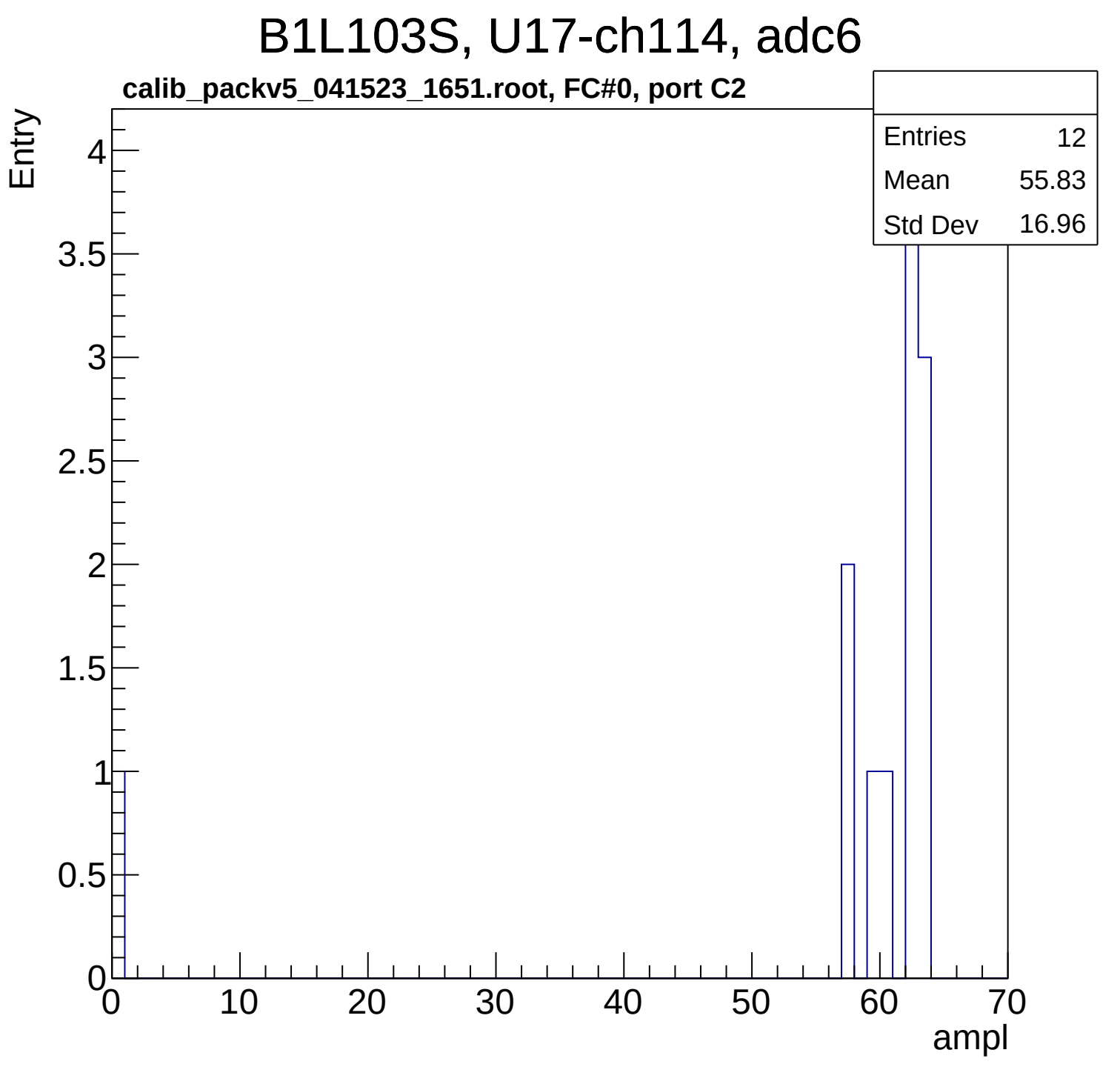

B1L103S, U17-ch114, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 33.62
Std Dev 5.496
Gaus mean : 34.5315
Gaus Width: 3.9426
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

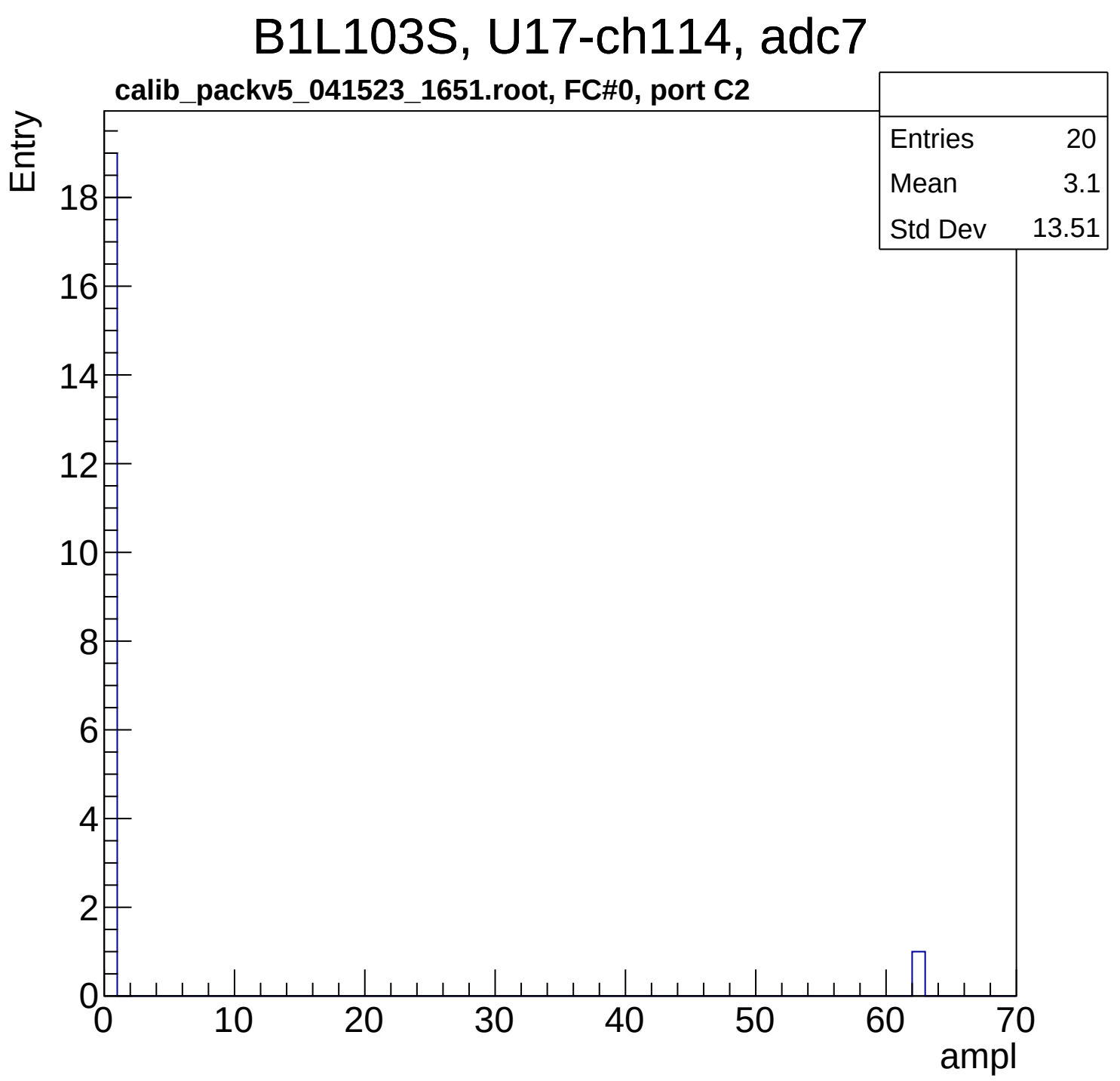

B1L103S, U17-ch114, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 39.53
Std Dev 6.655
Gaus mean : 41.1869
Gaus Width: 4.8678
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

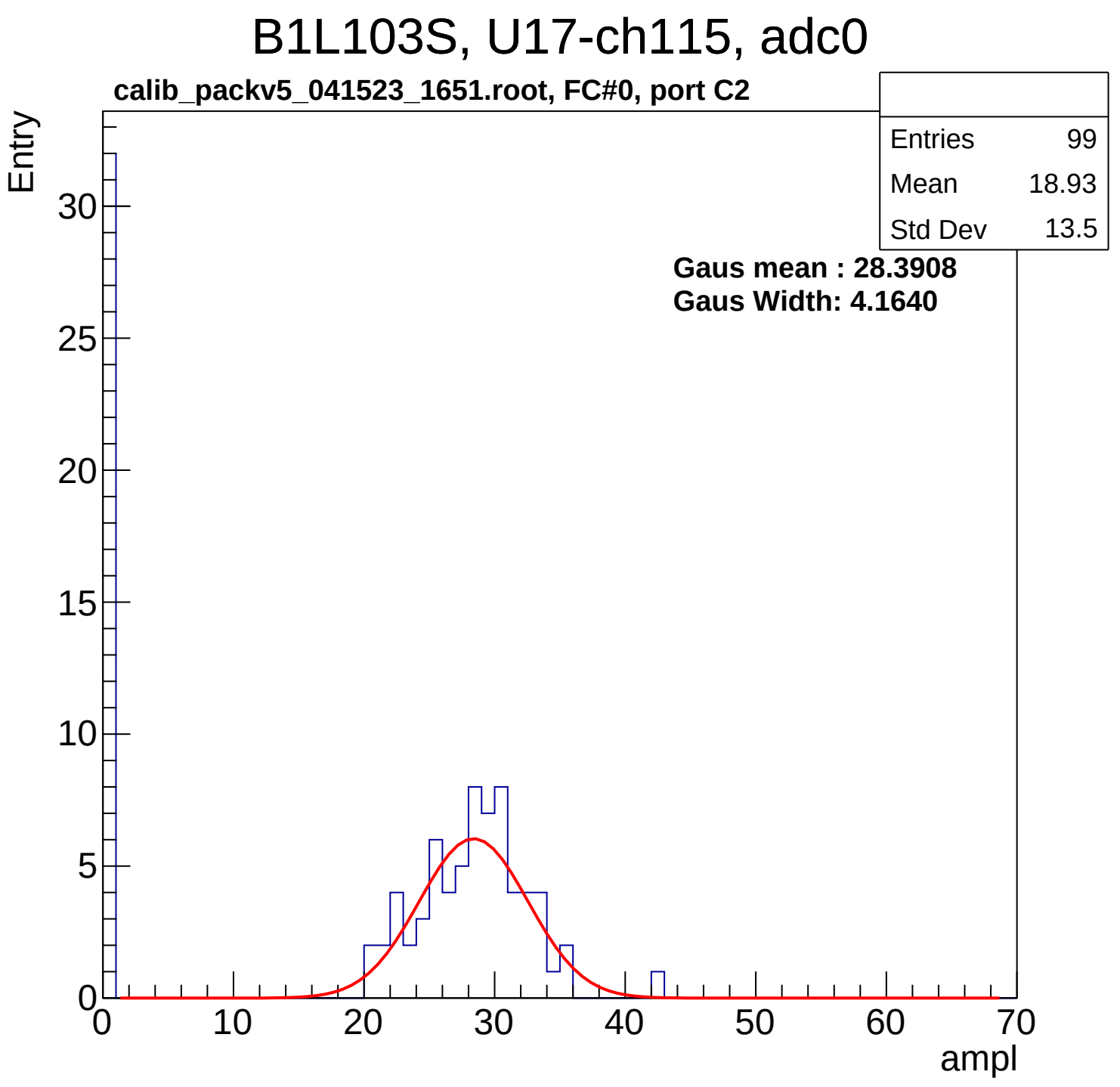

B1L103S, U17-ch114, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 41.62
Std Dev 15.41
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

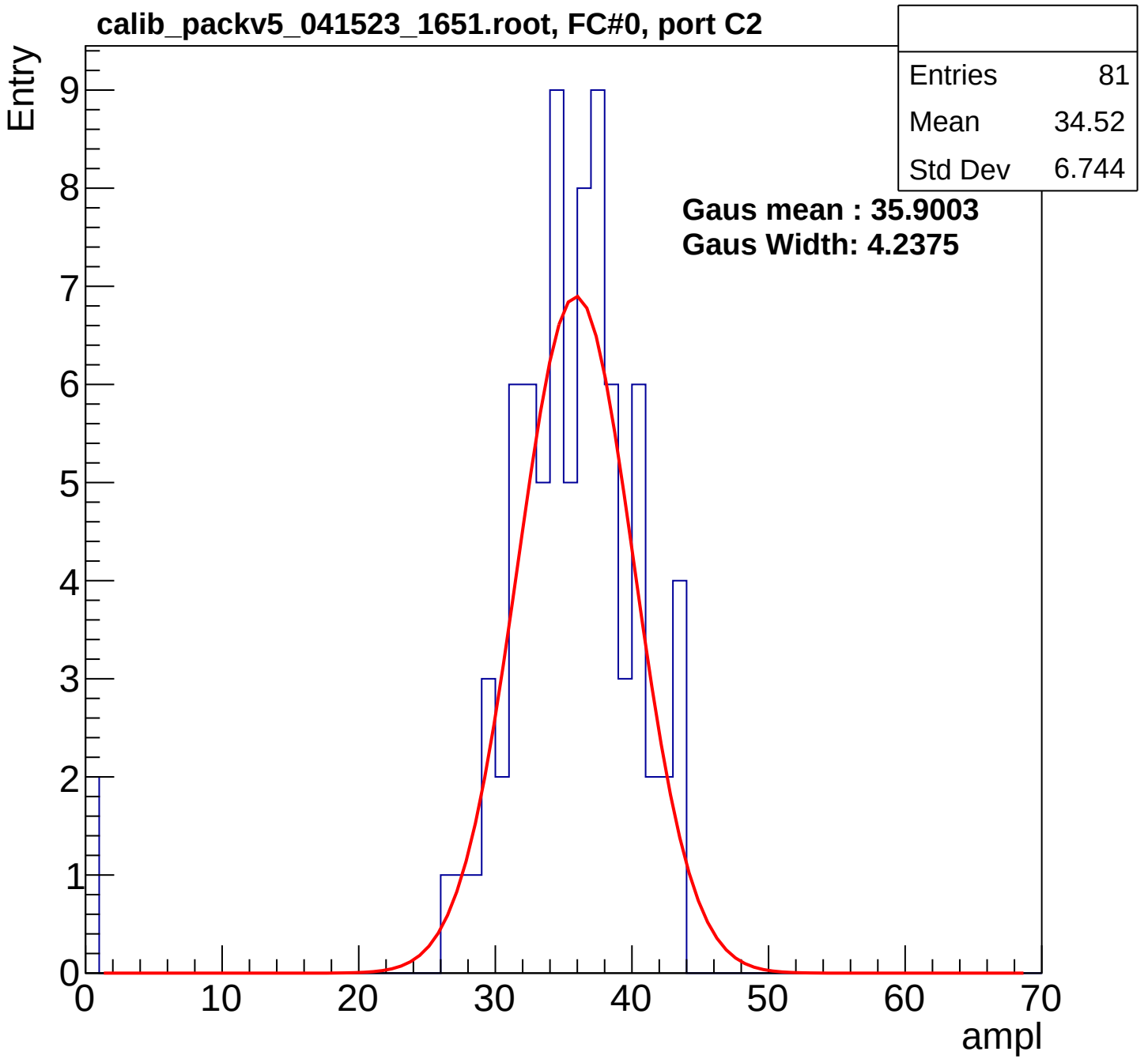

B1L103S, U17-ch114, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 49.71
Std Dev 15.22
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

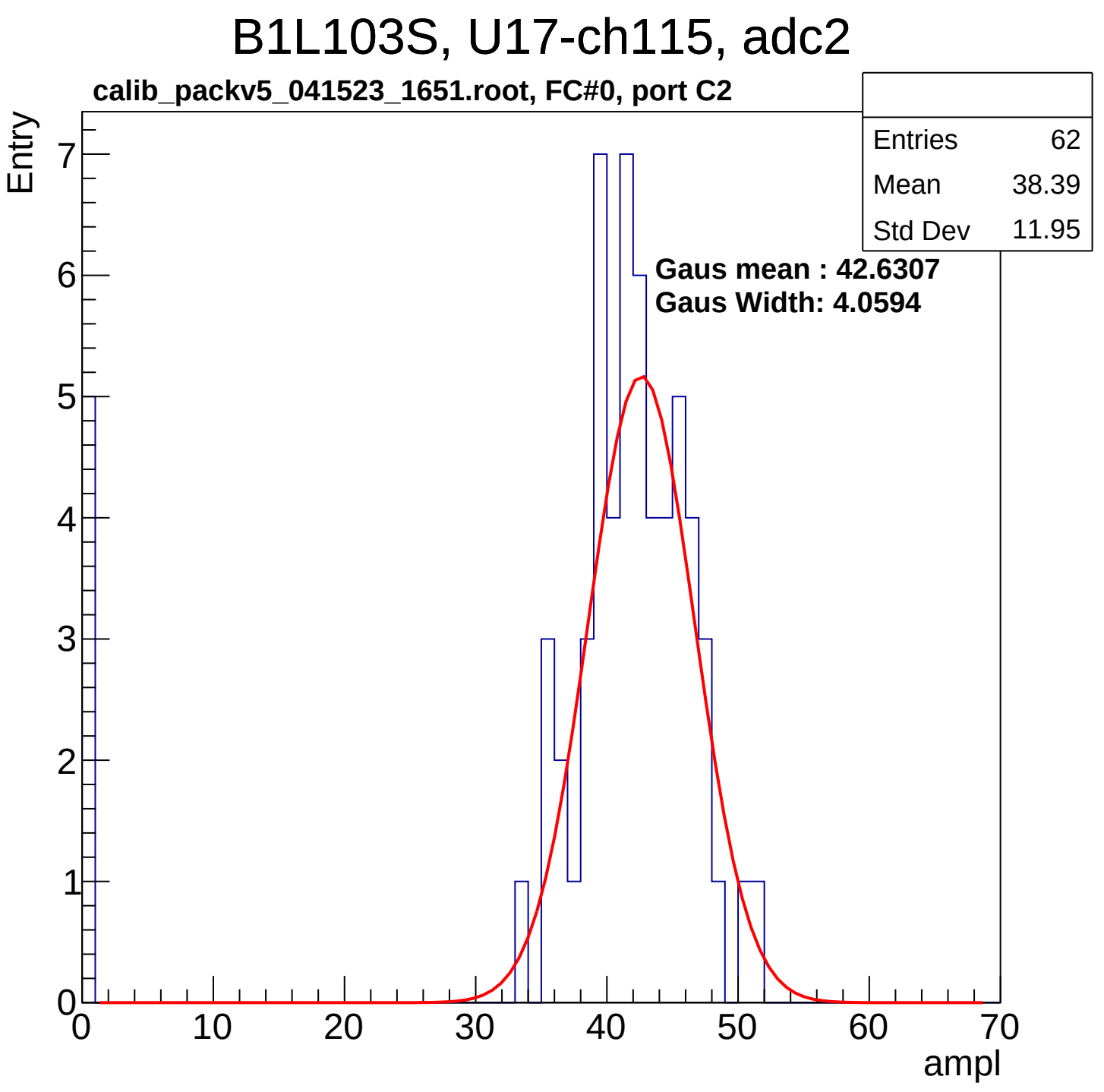

B1L103S, U17-ch114, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.78
Std Dev 3.077
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

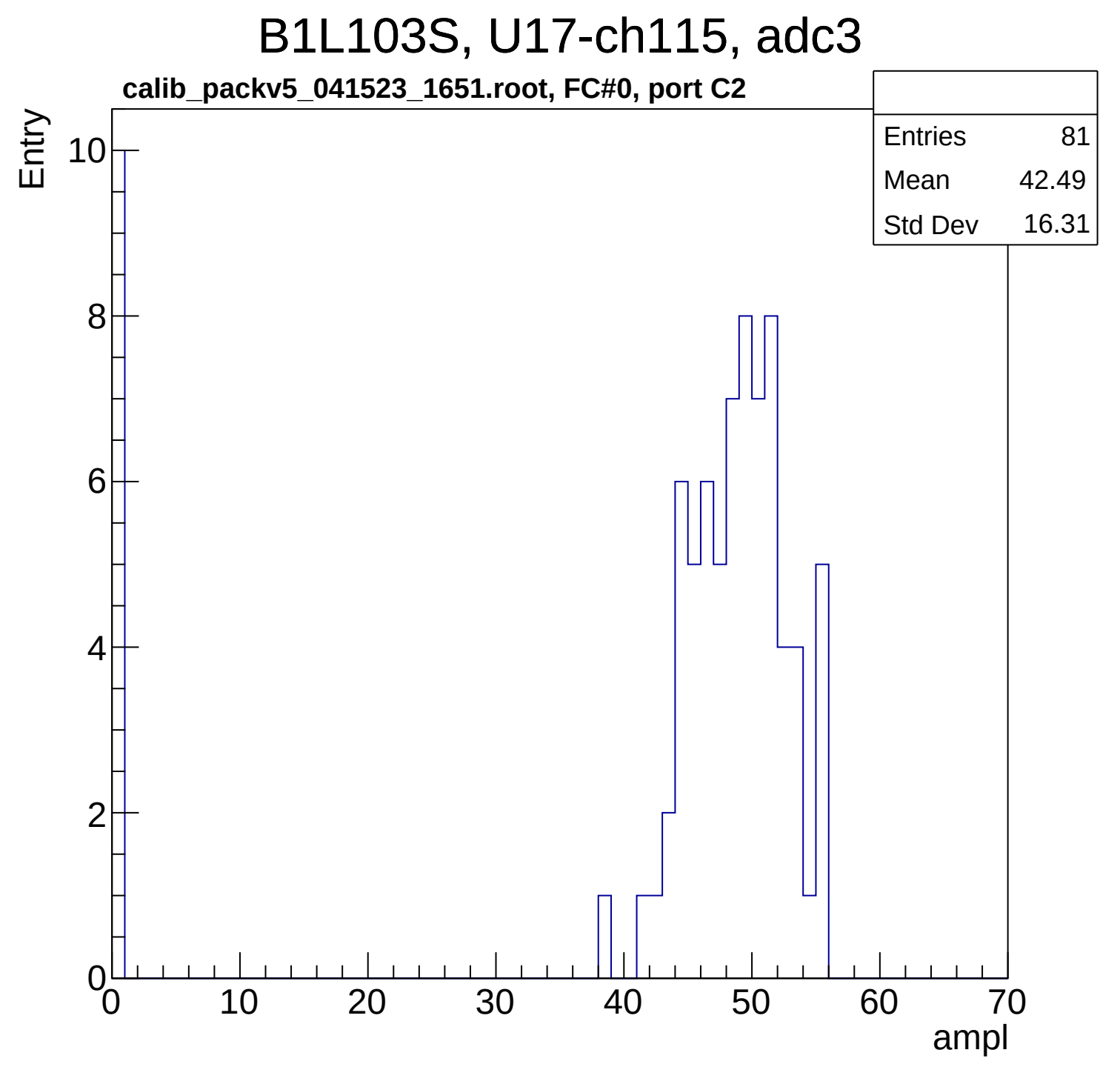

B1L103S, U17-ch114, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 55.83
Std Dev 16.96
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

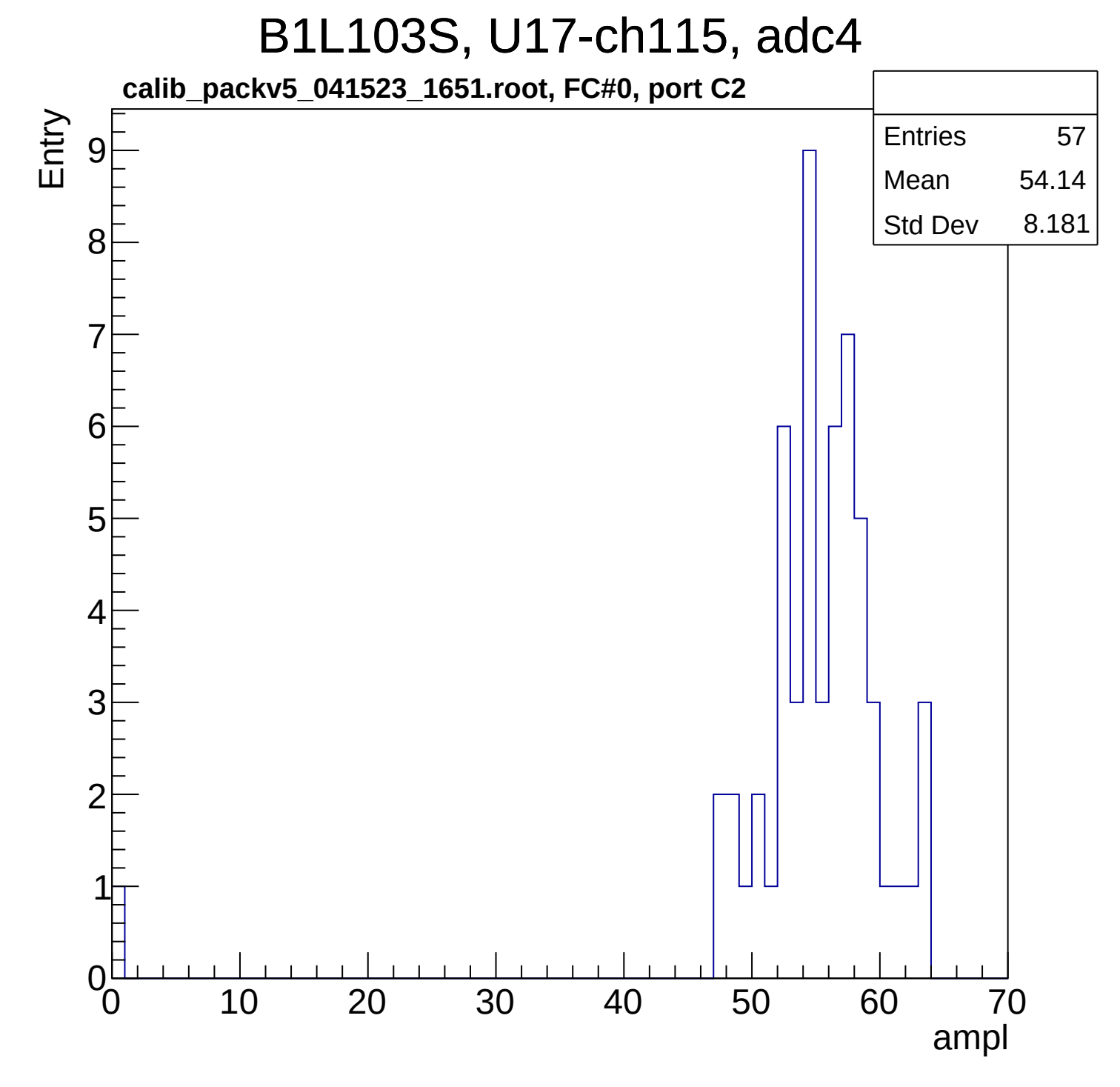

B1L103S, U17-ch114, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

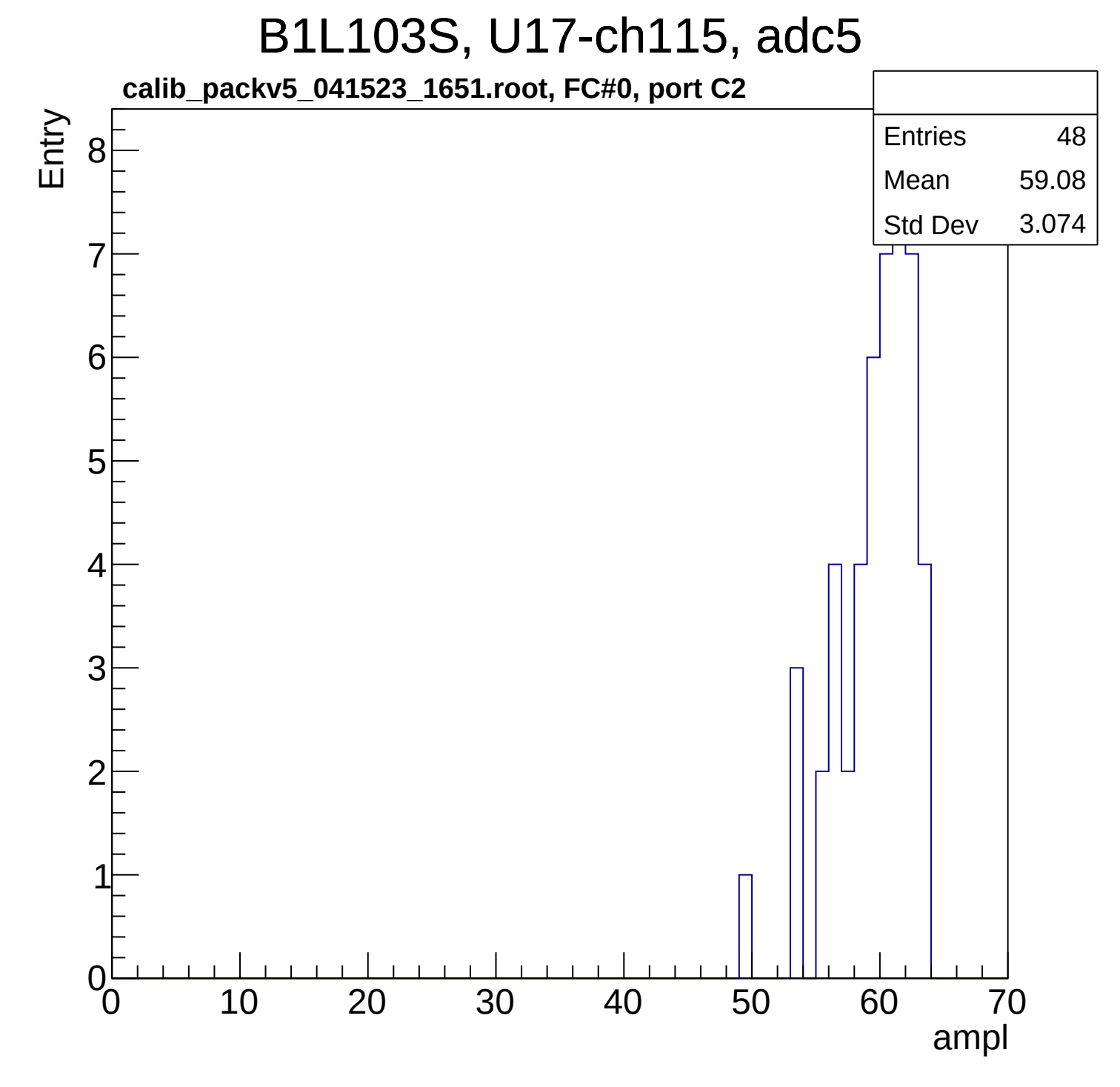

B1L103S, U17-ch115, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 18.93
Std Dev 13.5
Gaus mean : 28.3908
Gaus Width: 4.1640
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70

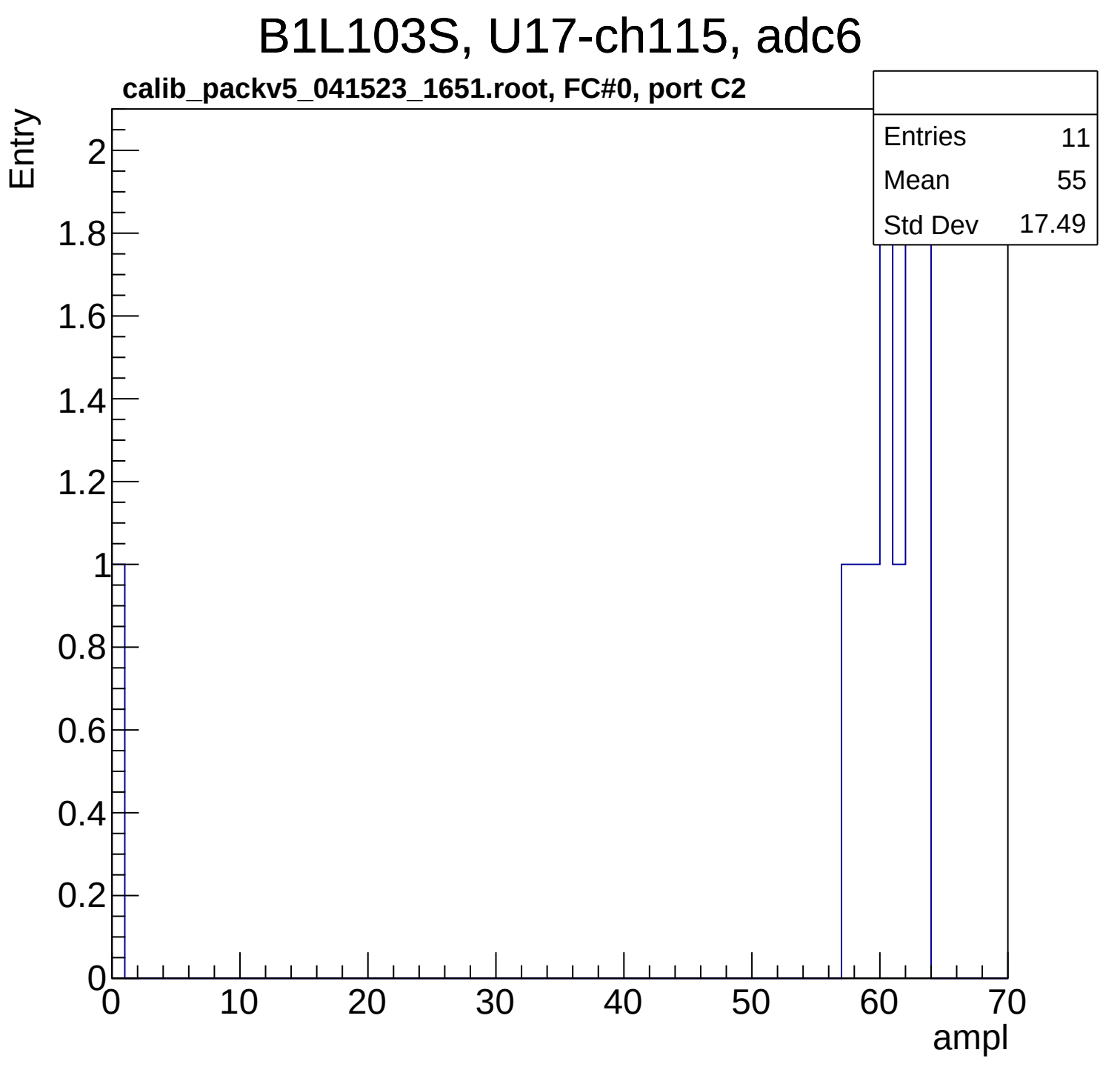

B1L103S, U17-ch115, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 34.52
Std Dev 6.744
Gaus mean : 35.9003
Gaus Width: 4.2375
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

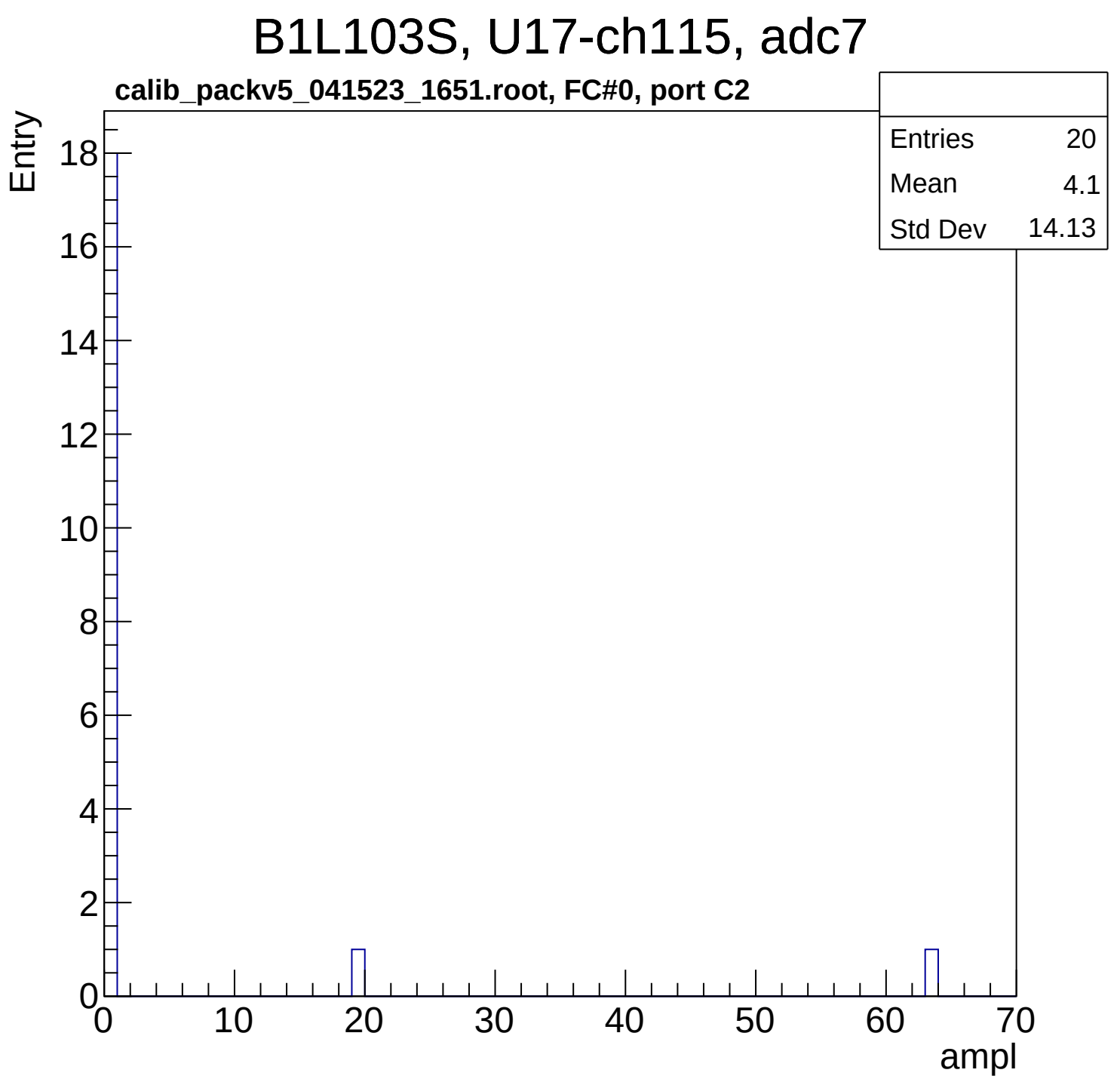

B1L103S, U17-ch115, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 38.39
Std Dev 11.95
Gaus mean : 42.6307
Gaus Width: 4.0594
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

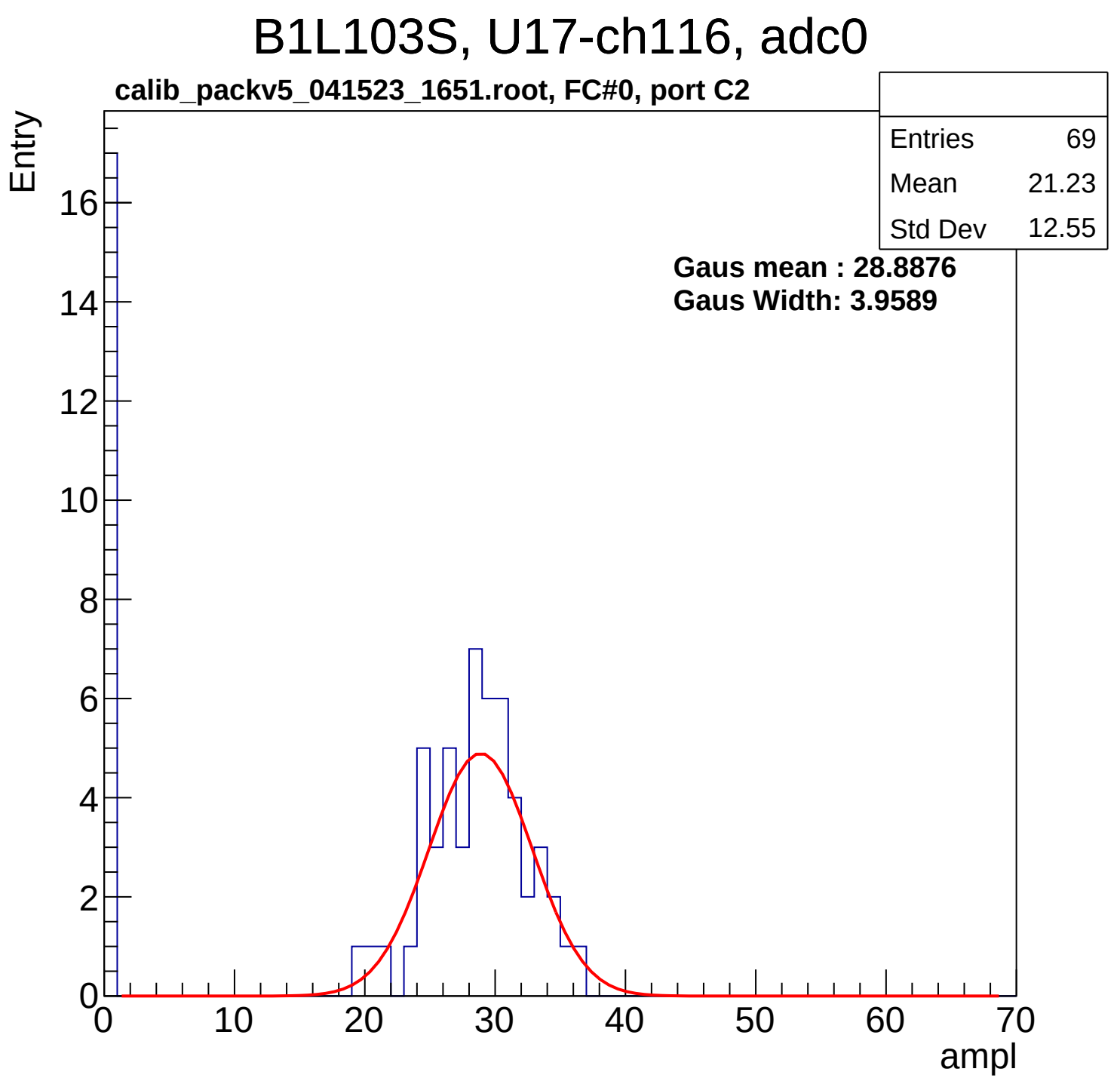

B1L103S, U17-ch115, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 42.49
Std Dev 16.31
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

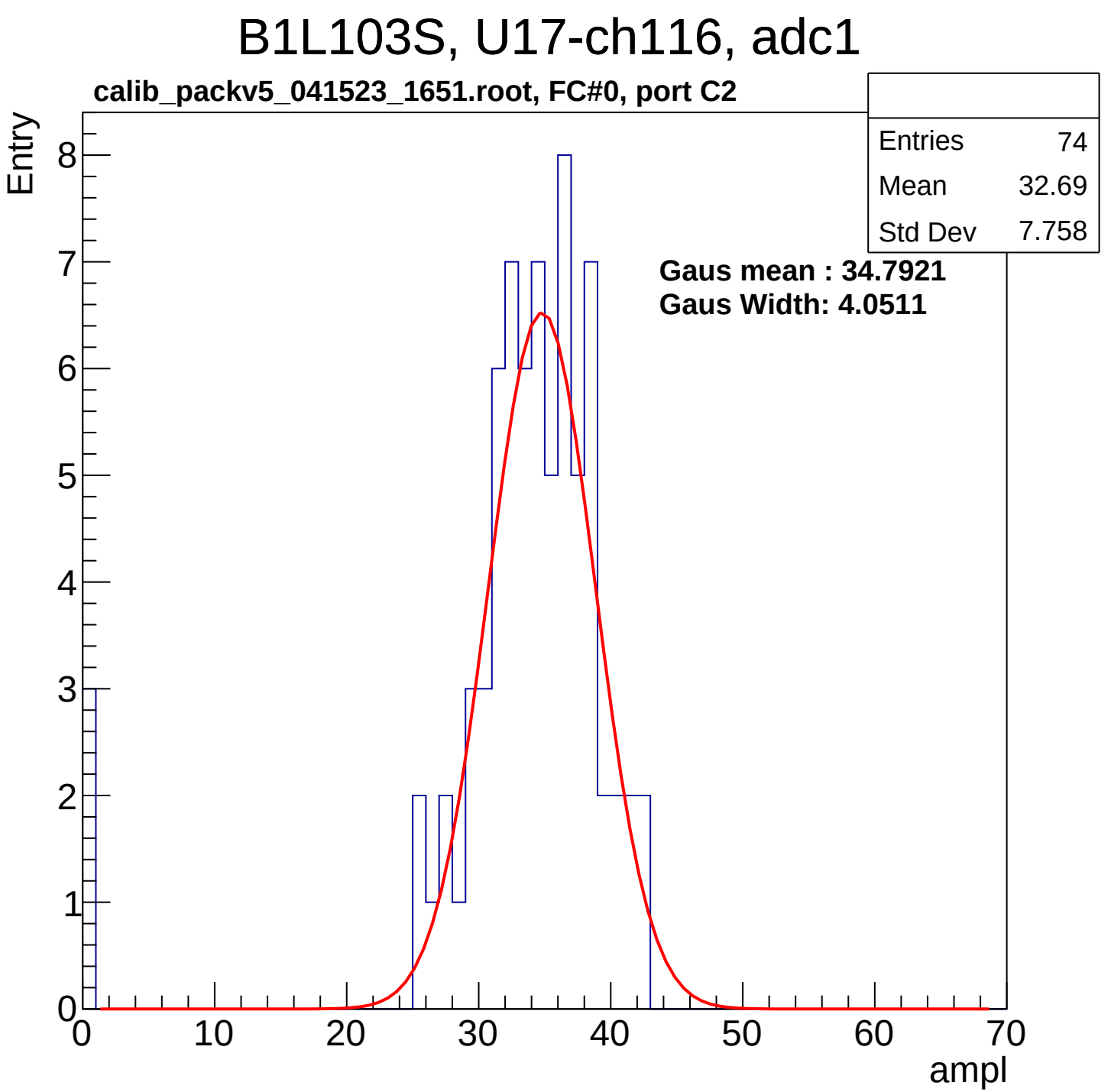

B1L103S, U17-ch115, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 54.14
Std Dev 8.181
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

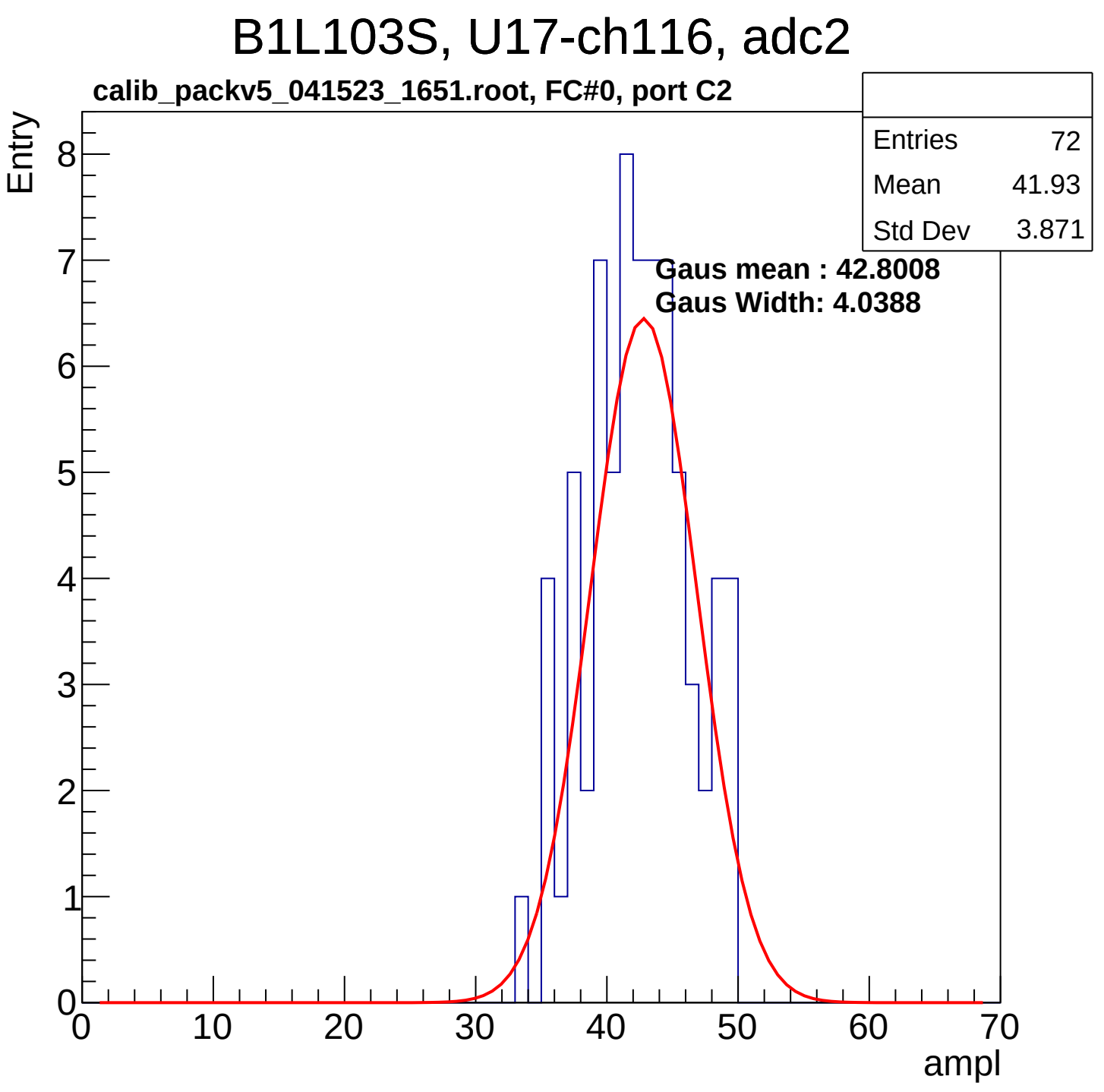

B1L103S, U17-ch115, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 59.08
Std Dev 3.074
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

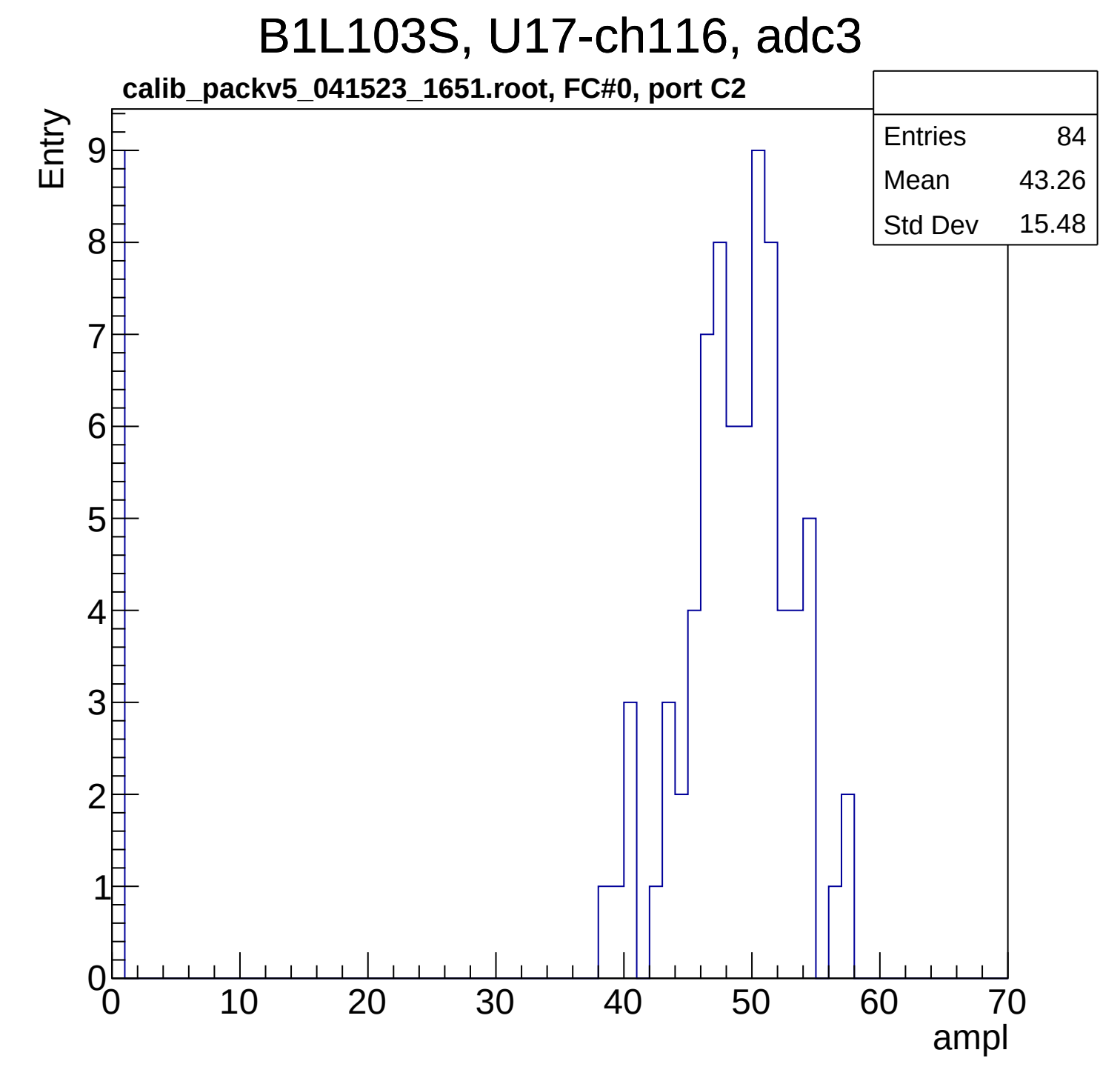

B1L103S, U17-ch115, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 55
Std Dev 17.49
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

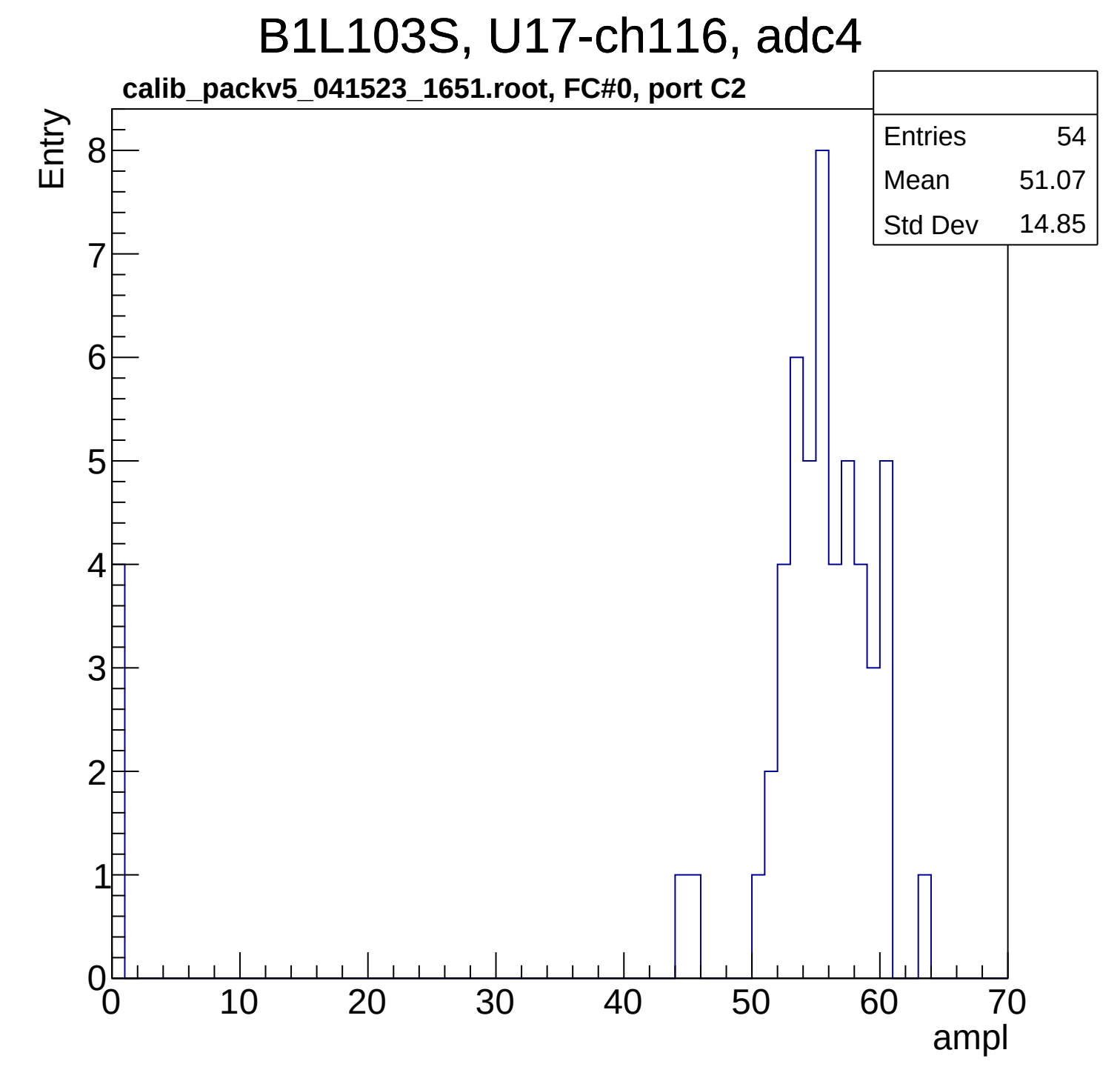

B1L103S, U17-ch115, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.1
Std Dev 14.13
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

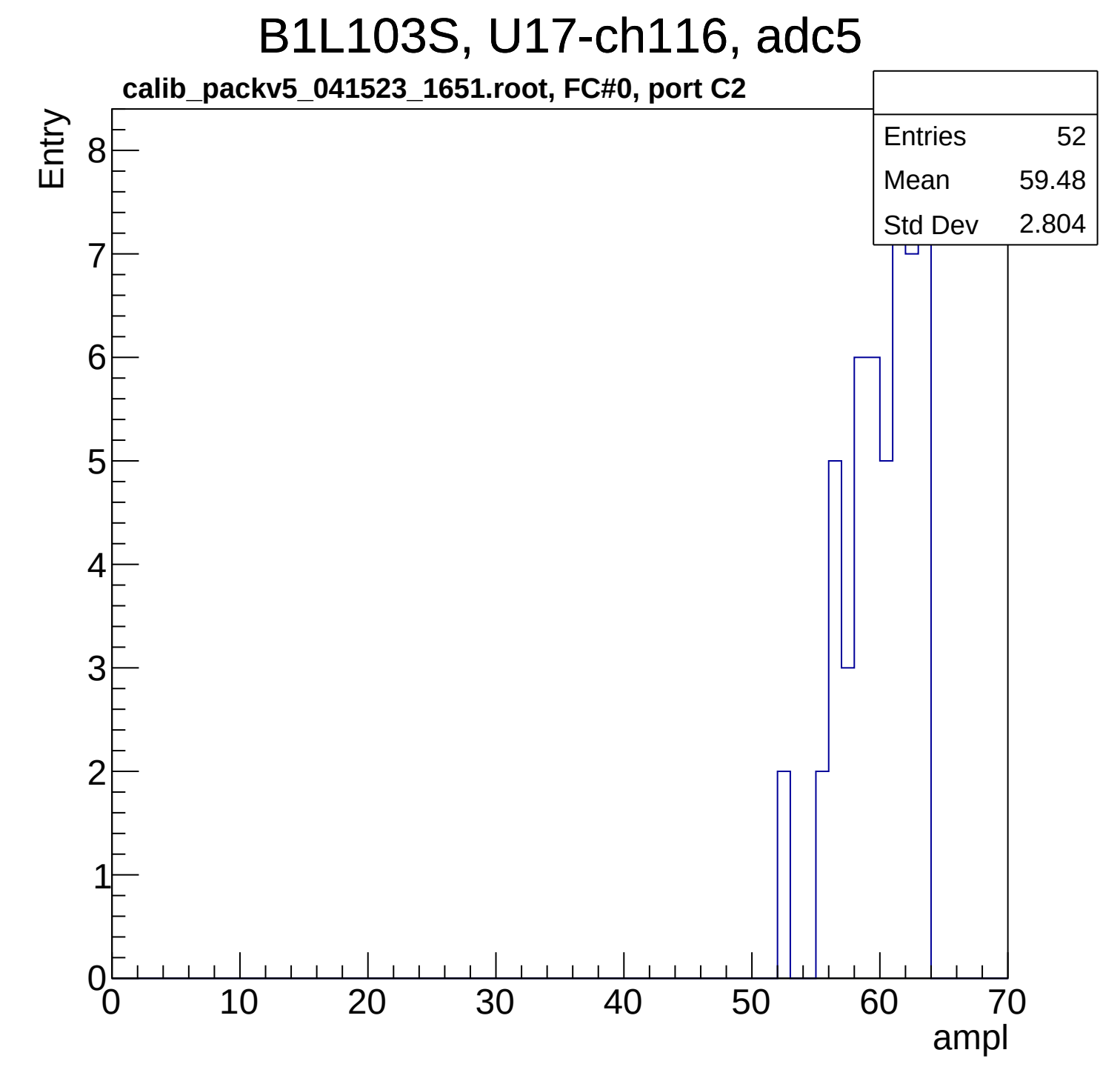

B1L103S, U17-ch116, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 21.23
Std Dev 12.55
Gaus mean : 28.8876
Gaus Width: 3.9589
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

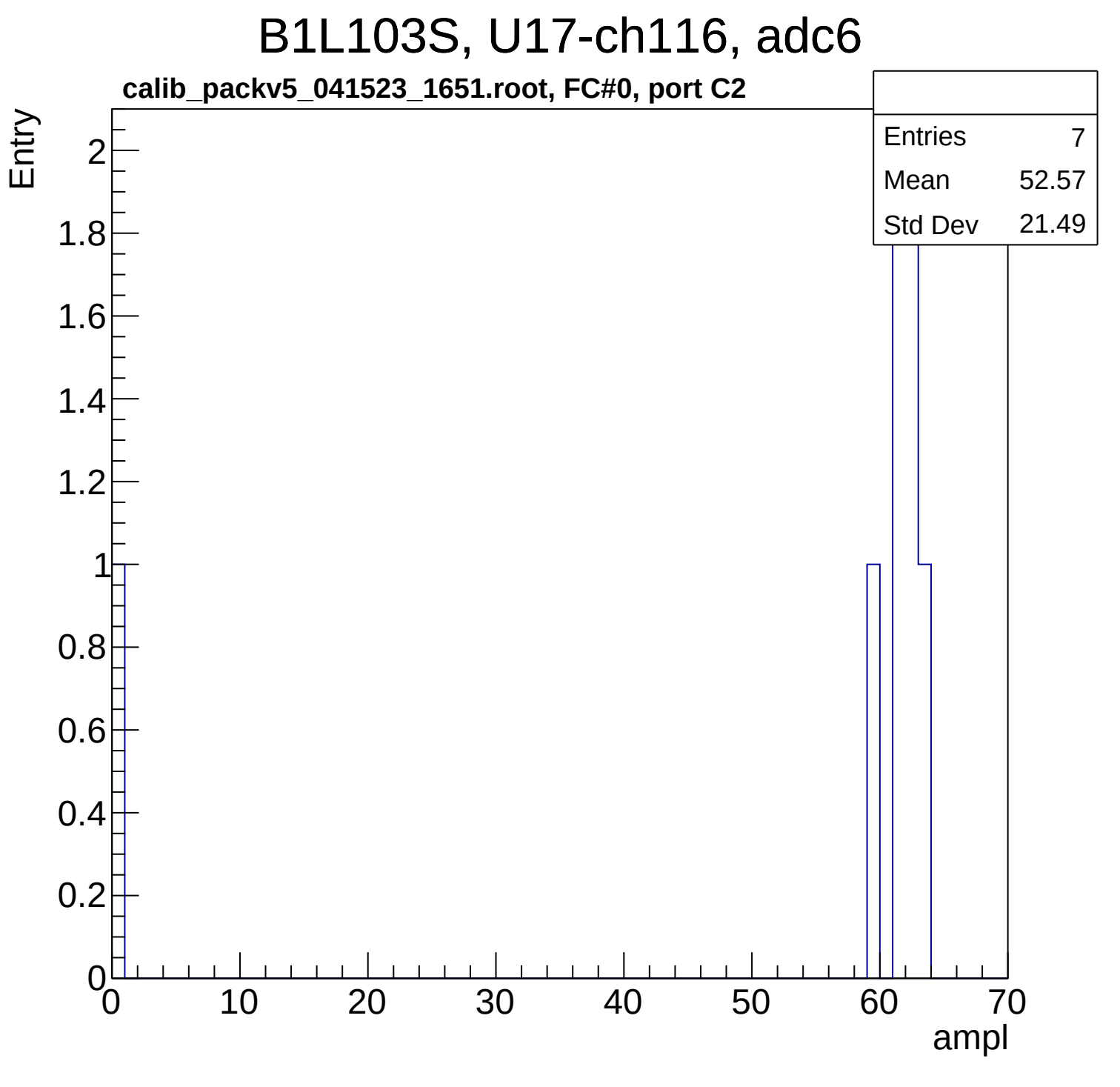

B1L103S, U17-ch116, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 32.69
Std Dev 7.758
Gaus mean : 34.7921
Gaus Width: 4.0511
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

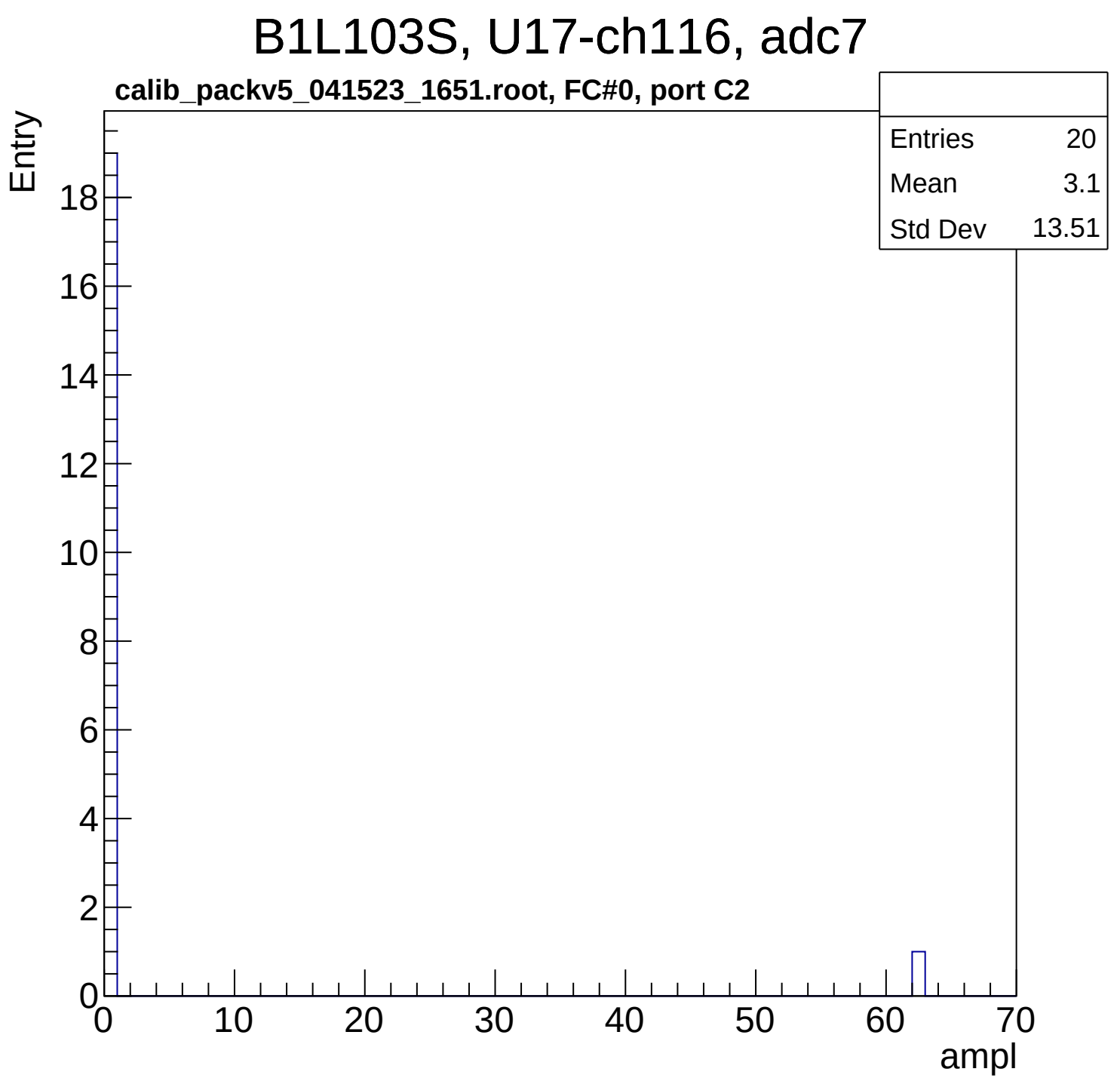

B1L103S, U17-ch116, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 41.93
Std Dev 3.871
Gaus mean : 42.8008
Gaus Width: 4.0388
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

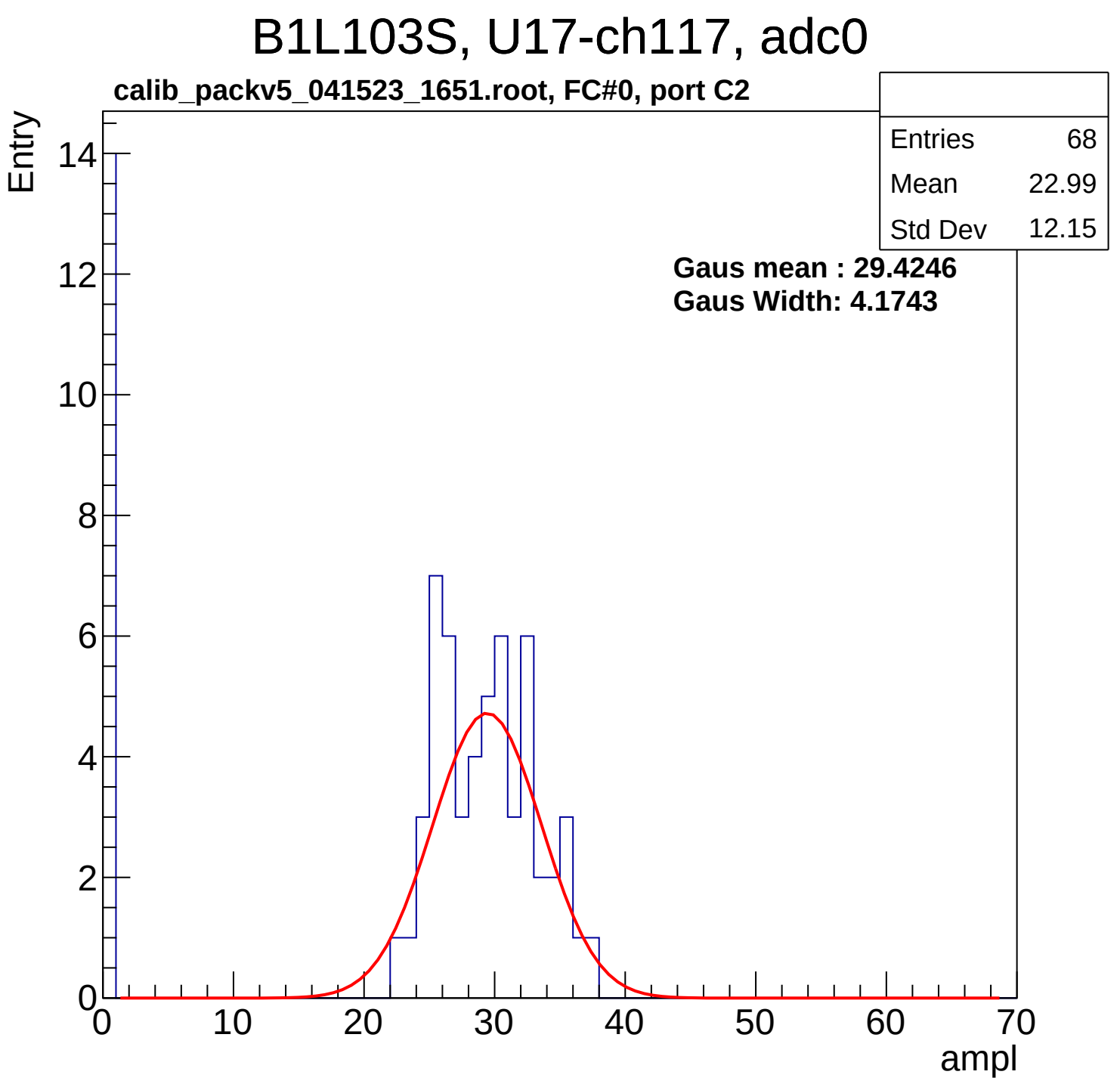

B1L103S, U17-ch116, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 43.26
Std Dev 15.48
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

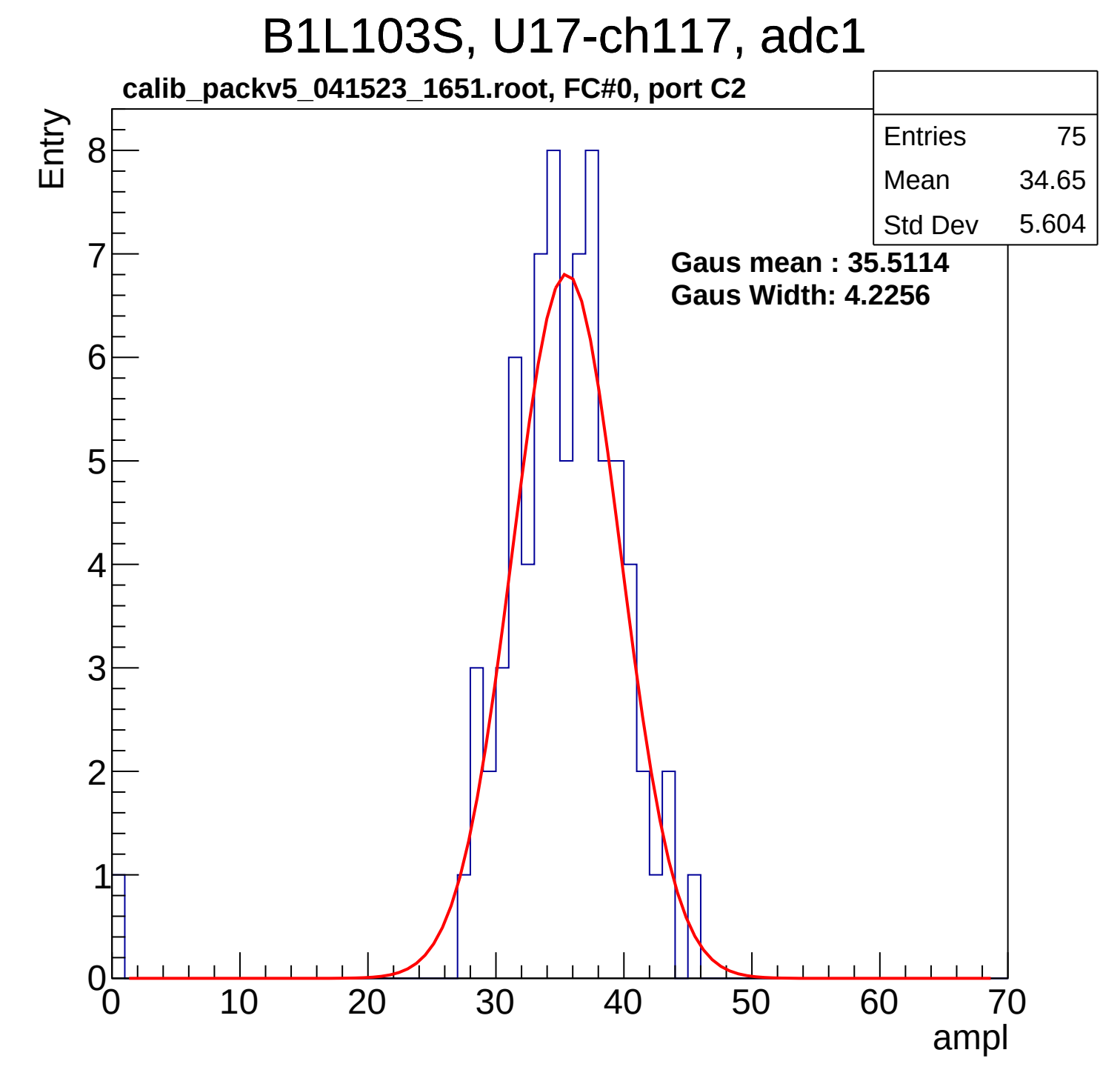

B1L103S, U17-ch116, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 51.07
Std Dev 14.85
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

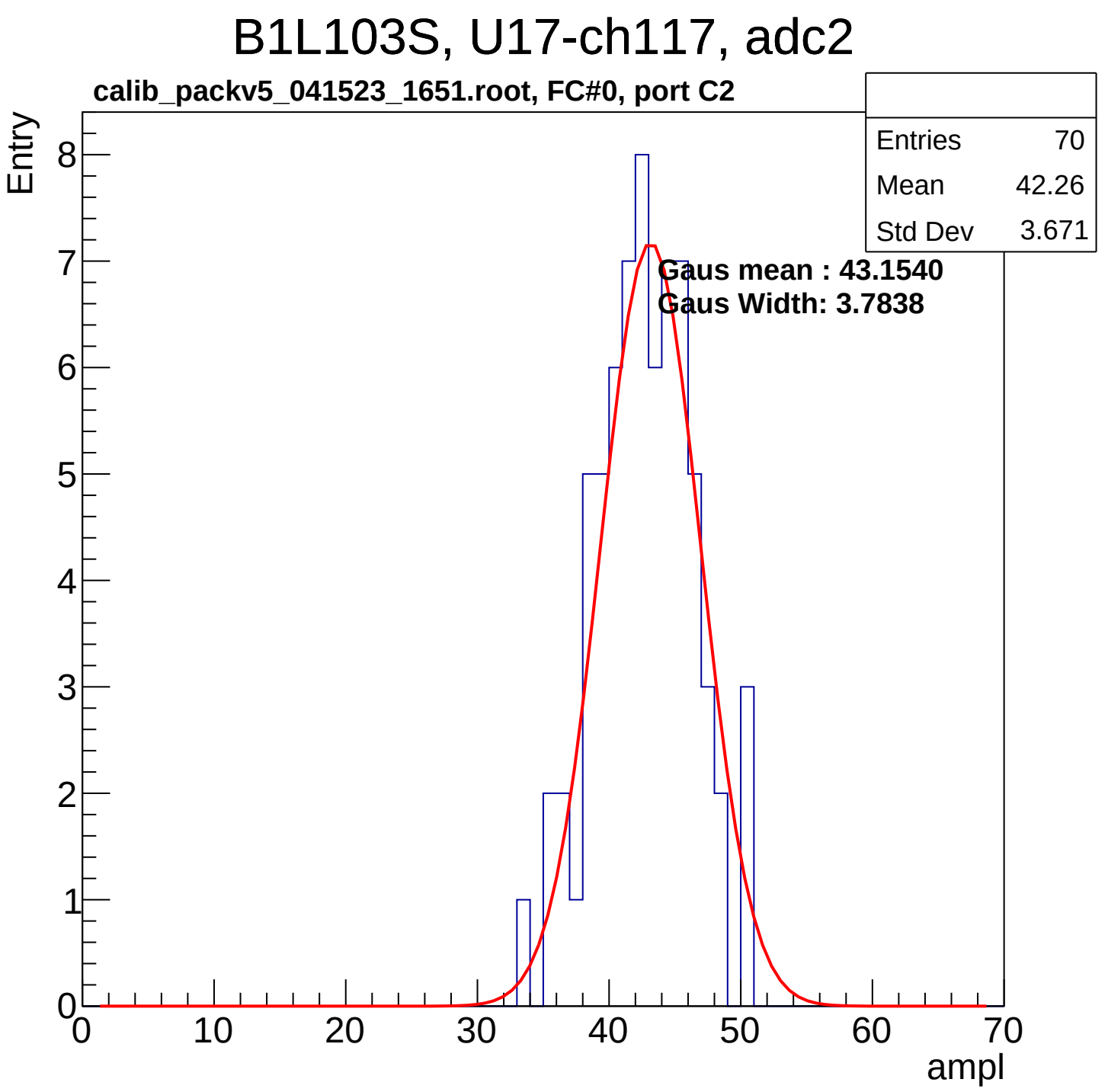

B1L103S, U17-ch116, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 59.48
Std Dev 2.804
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

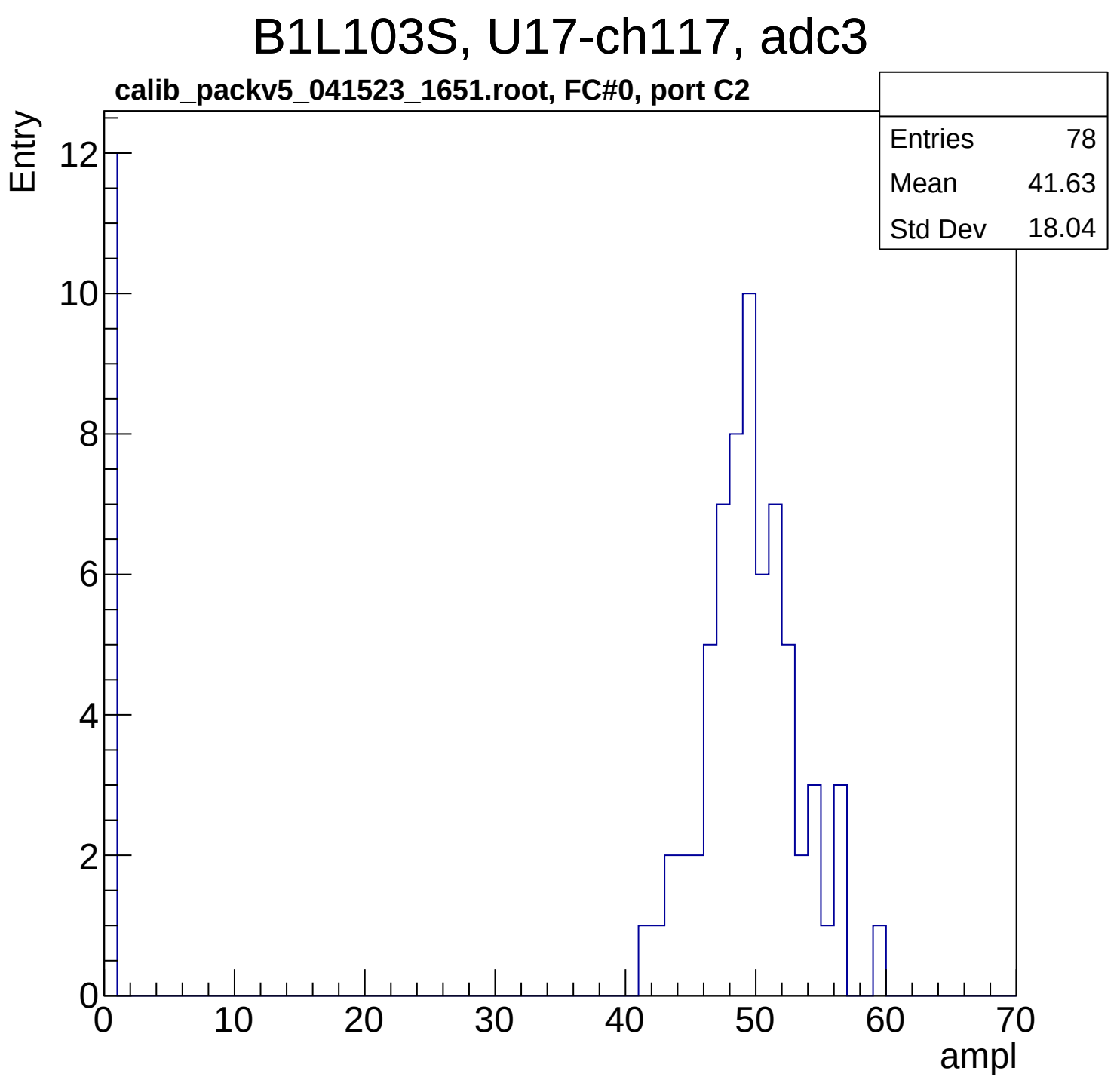

B1L103S, U17-ch116, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 52.57
Std Dev 21.49
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

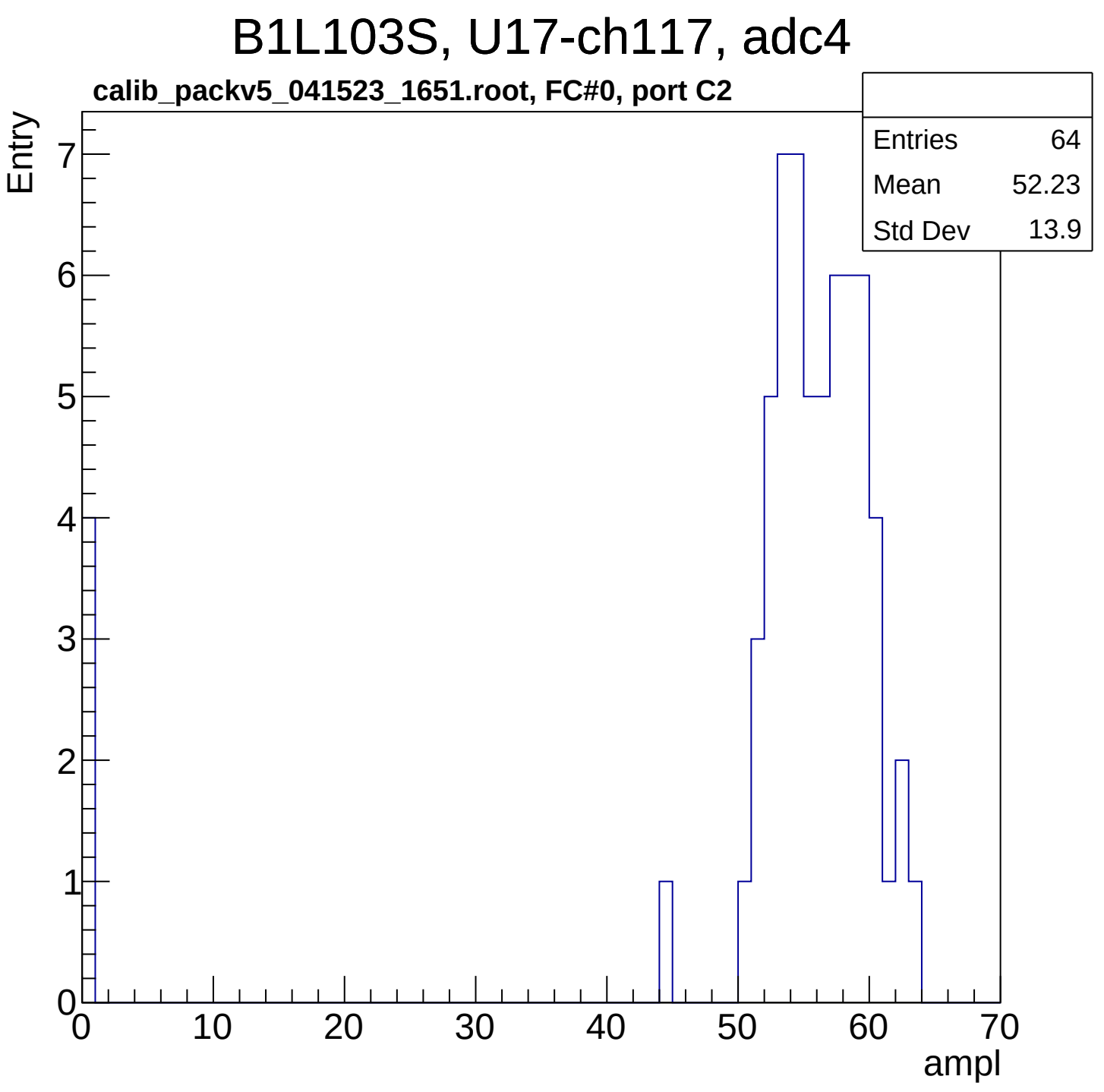

B1L103S, U17-ch116, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

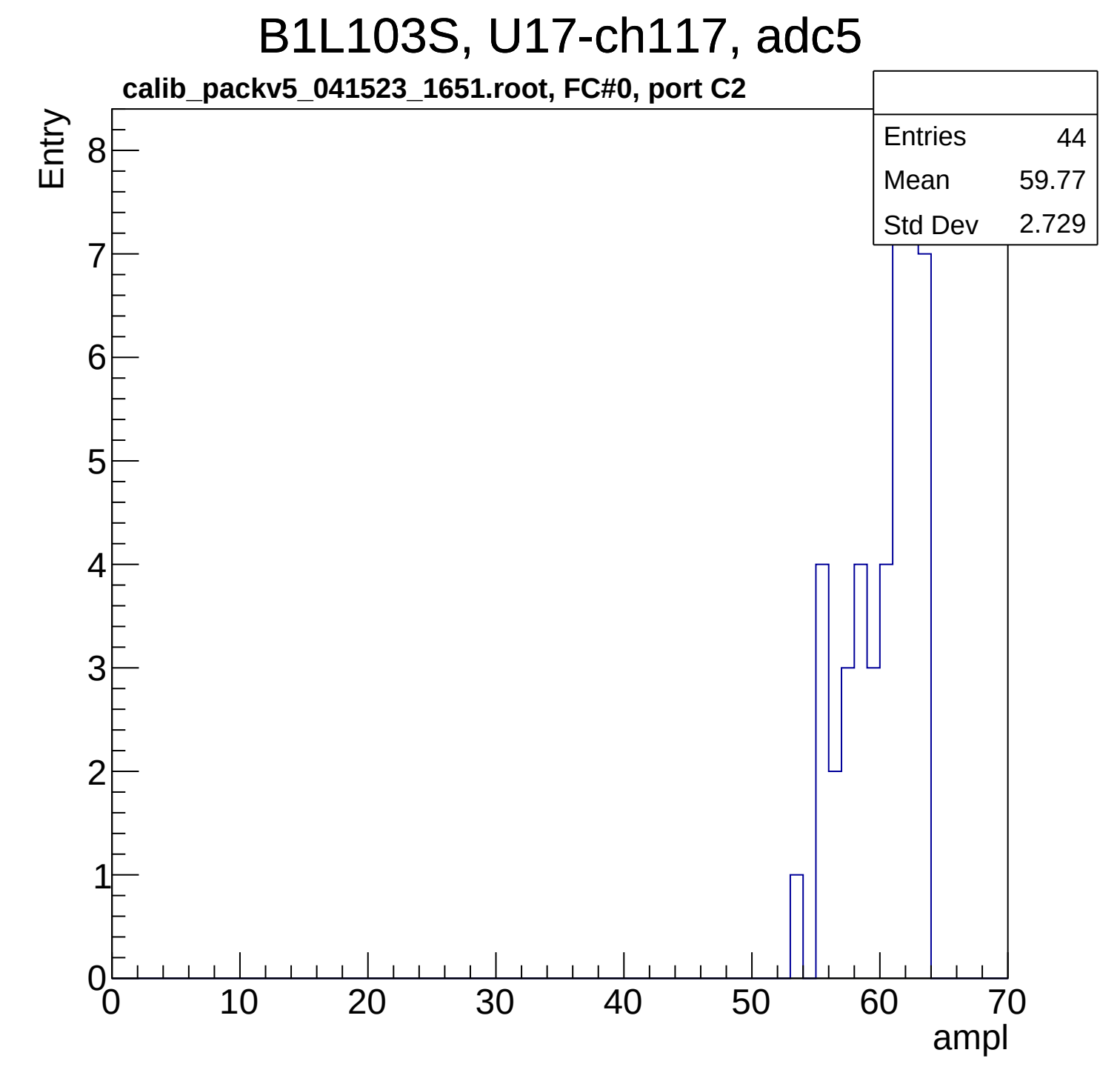

B1L103S, U17-ch117, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 22.99
Std Dev 12.15
Gaus mean : 29.4246
Gaus Width: 4.1743
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

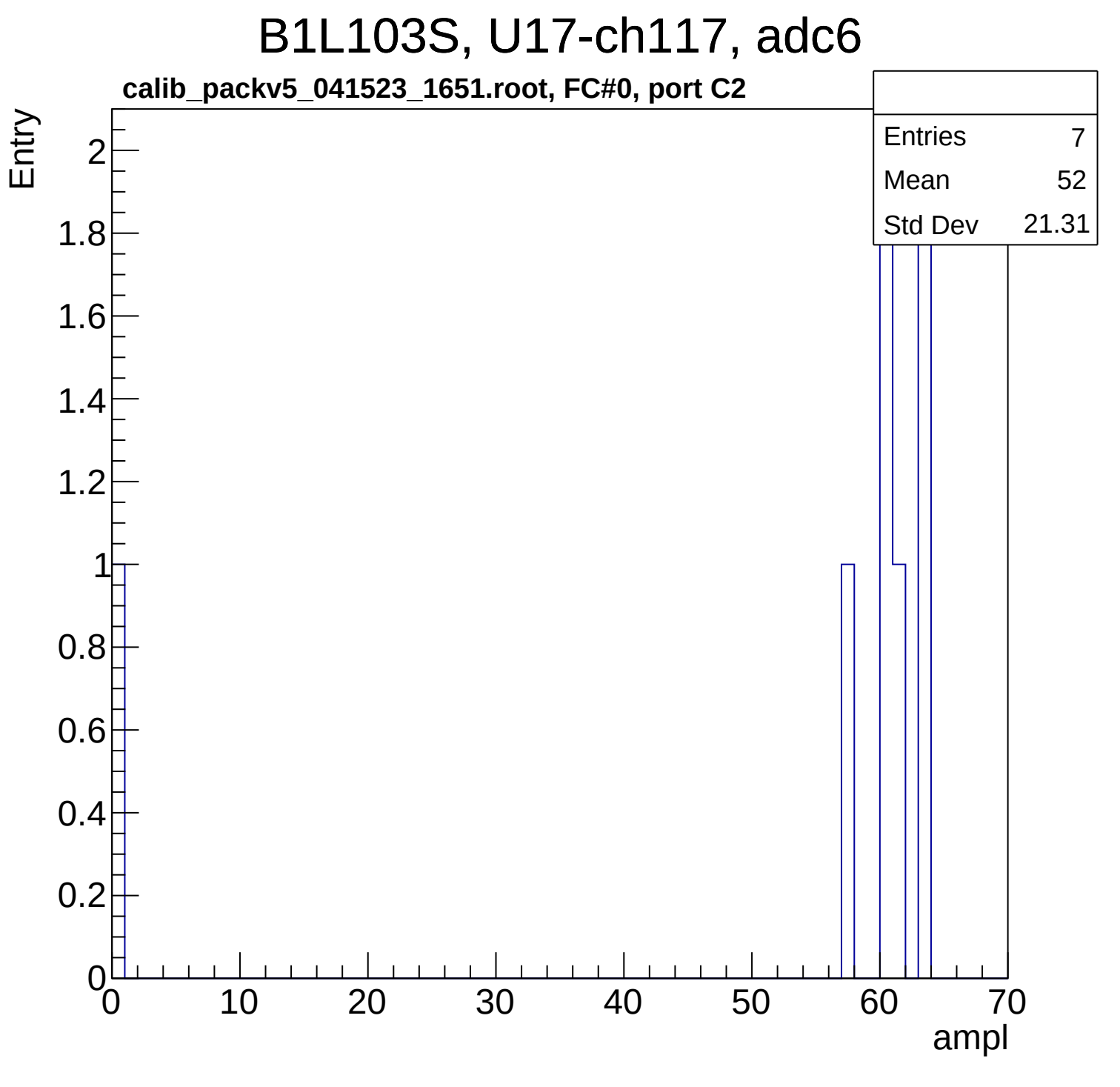

B1L103S, U17-ch117, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 34.65
Std Dev 5.604
Gaus mean : 35.5114
Gaus Width: 4.2256
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

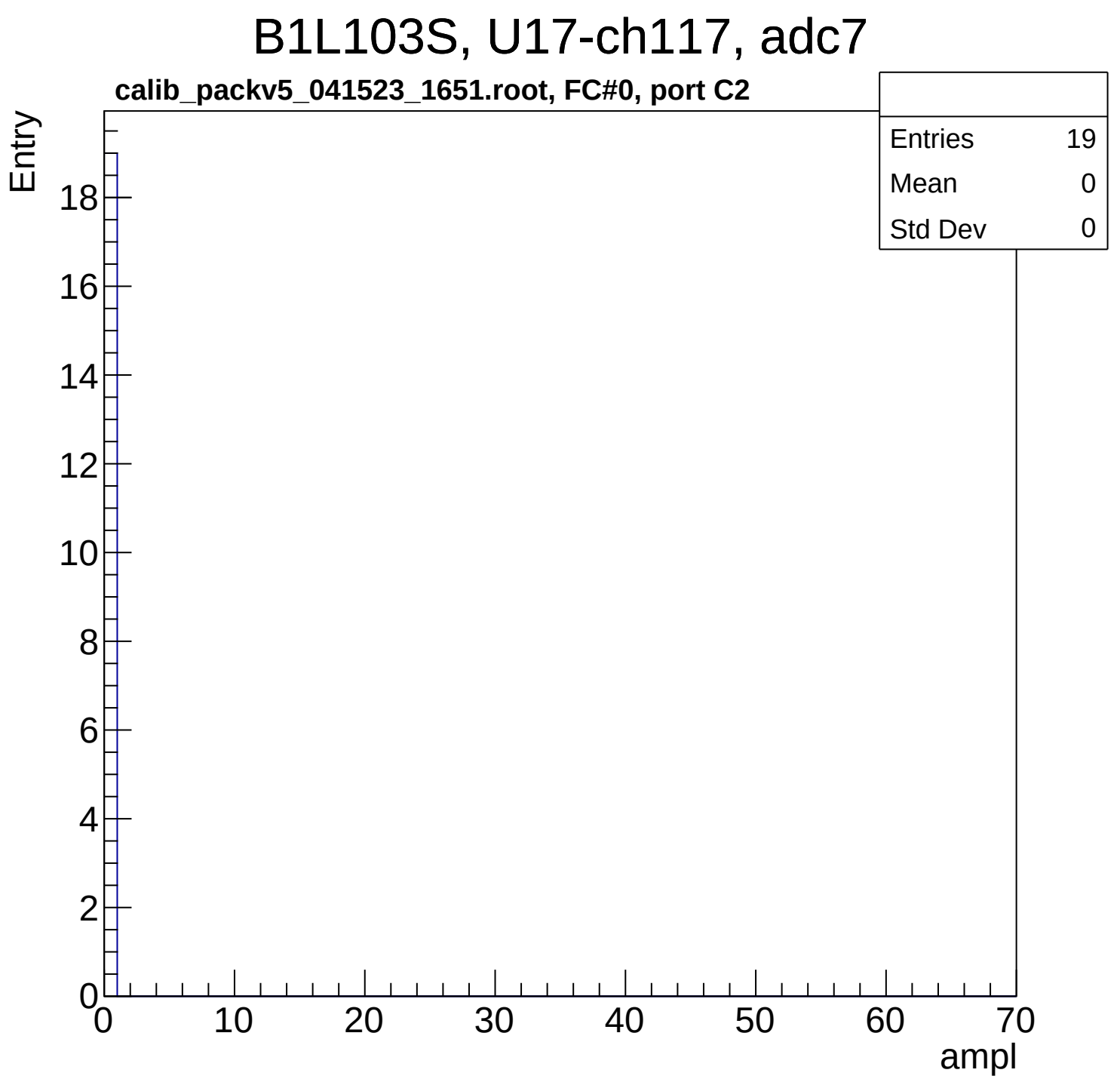

B1L103S, U17-ch117, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 42.26
Std Dev 3.671
Gaus mean : 43.1540
Gaus Width: 3.7838
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

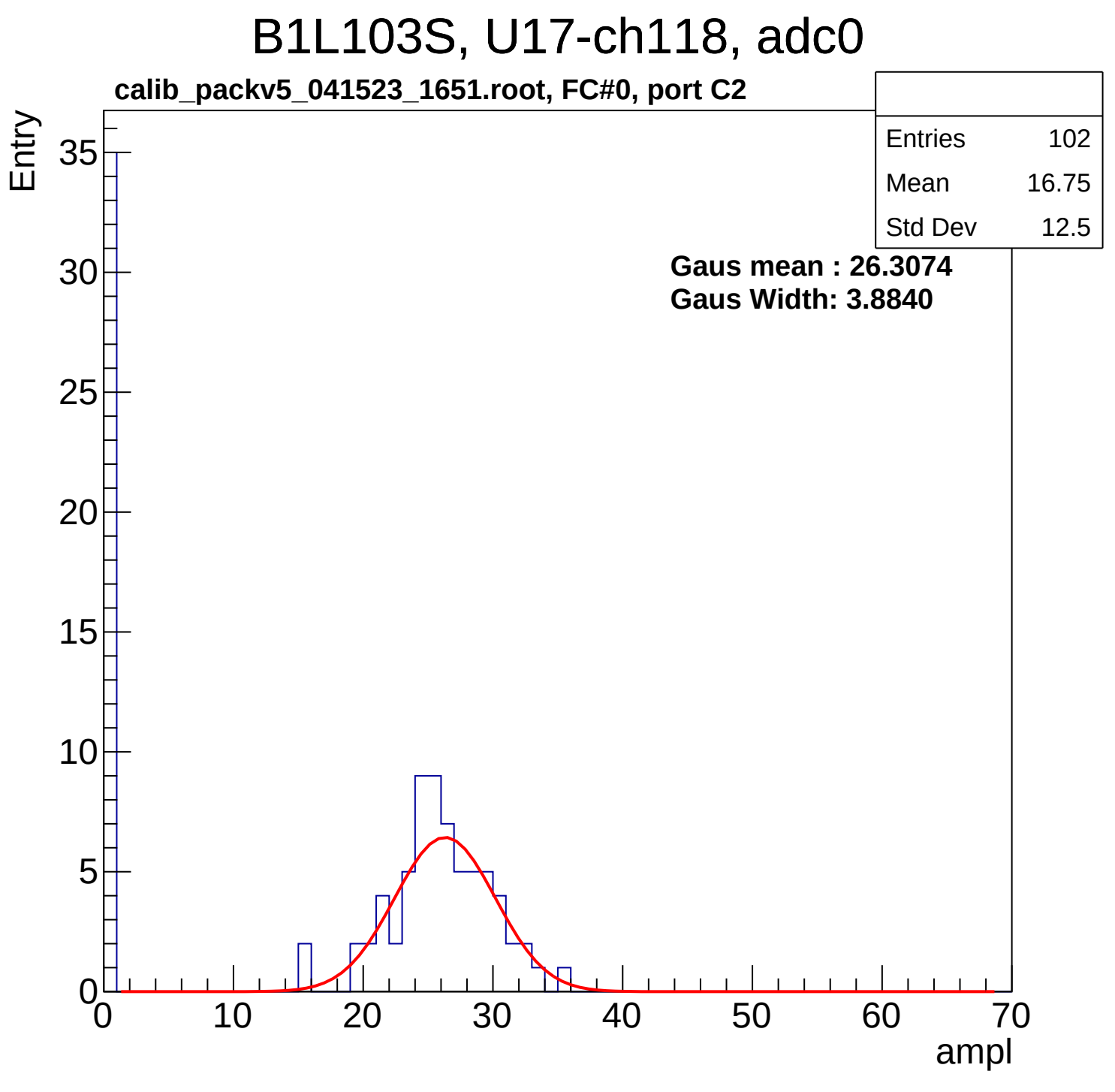

B1L103S, U17-ch117, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 41.63
Std Dev 18.04
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

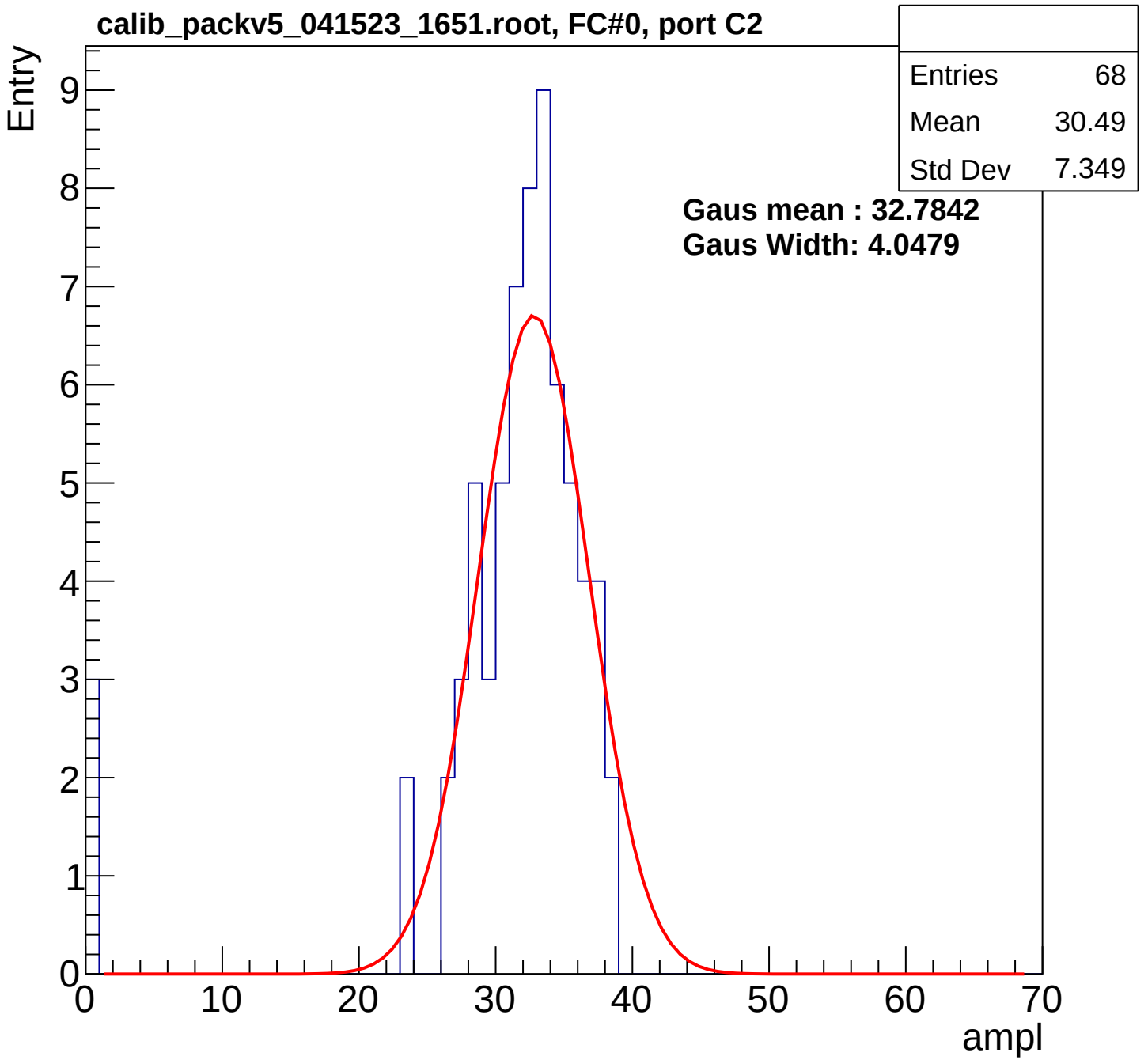

B1L103S, U17-ch117, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 52.23
Std Dev 13.9
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

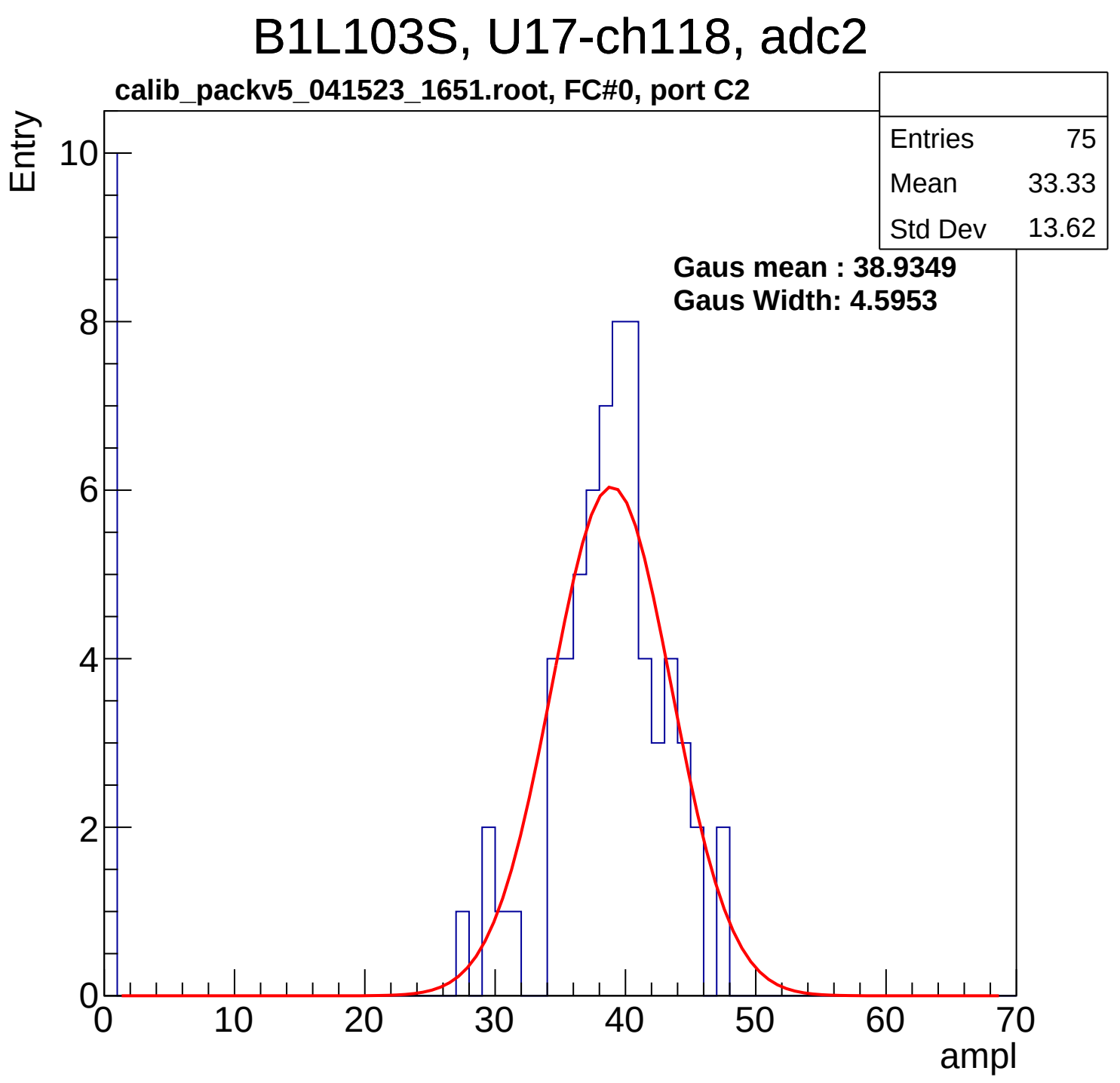

B1L103S, U17-ch117, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 59.77
Std Dev 2.729
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

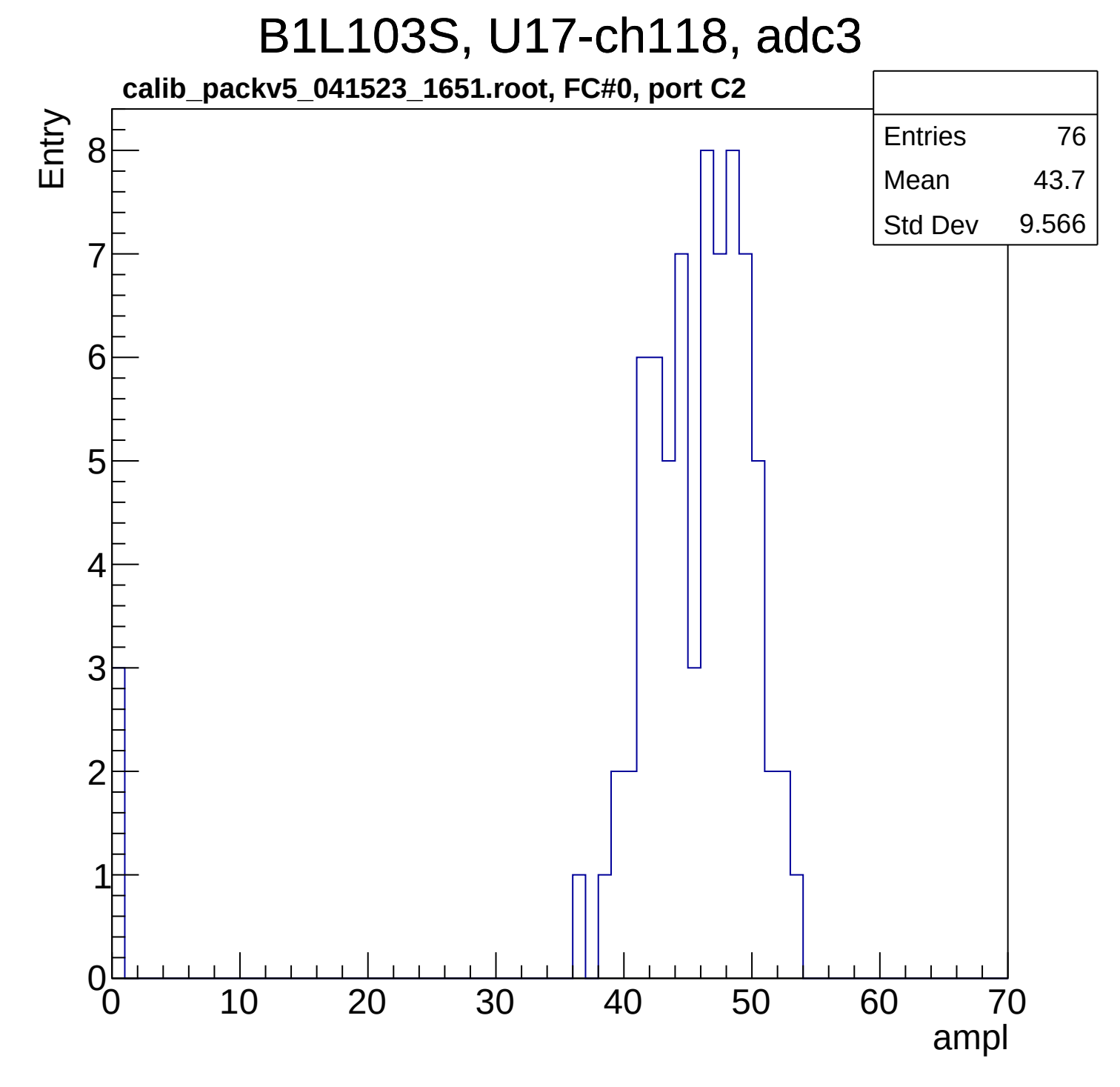

B1L103S, U17-ch117, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 52
Std Dev 21.31
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

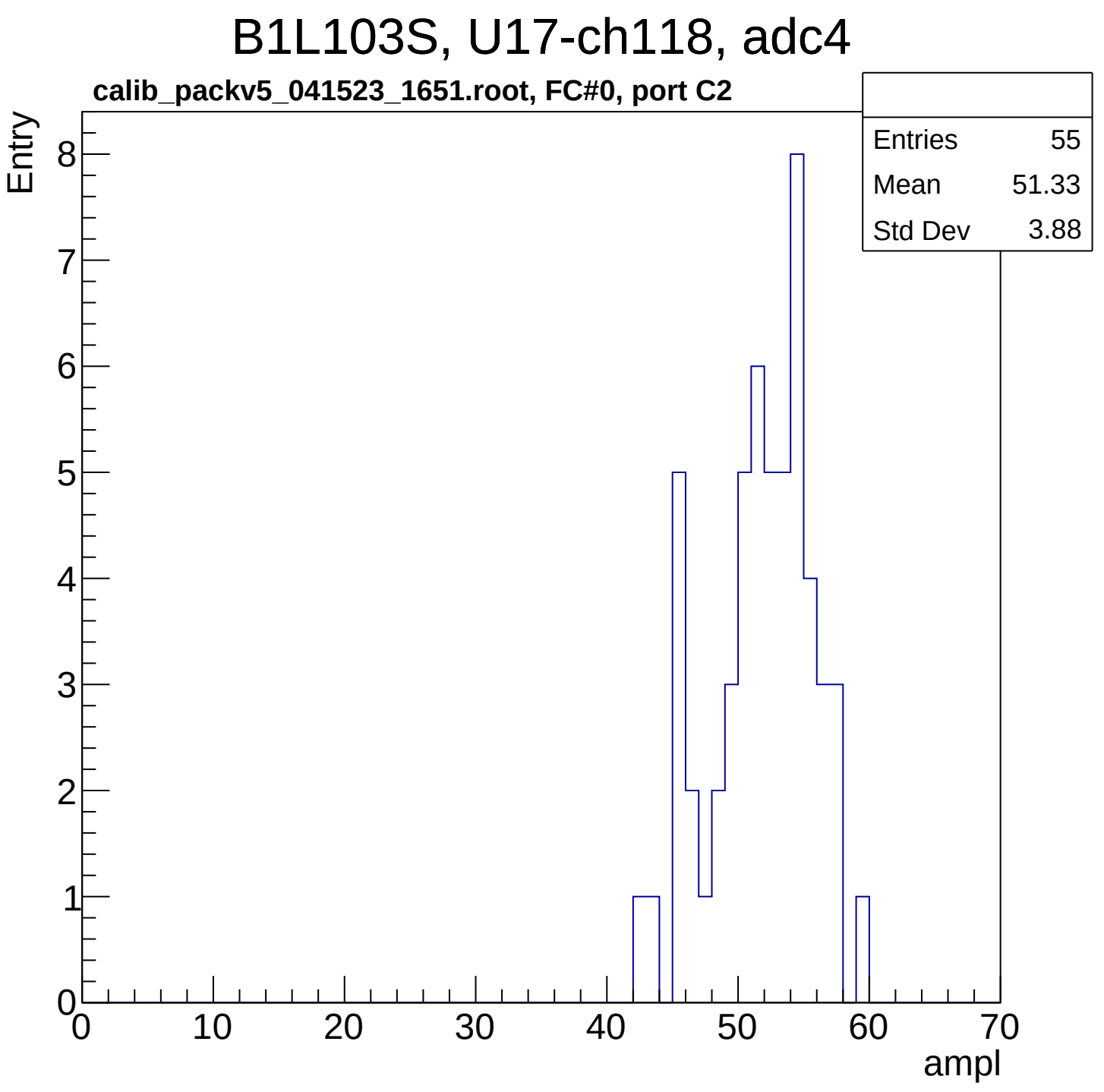

B1L103S, U17-ch117, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

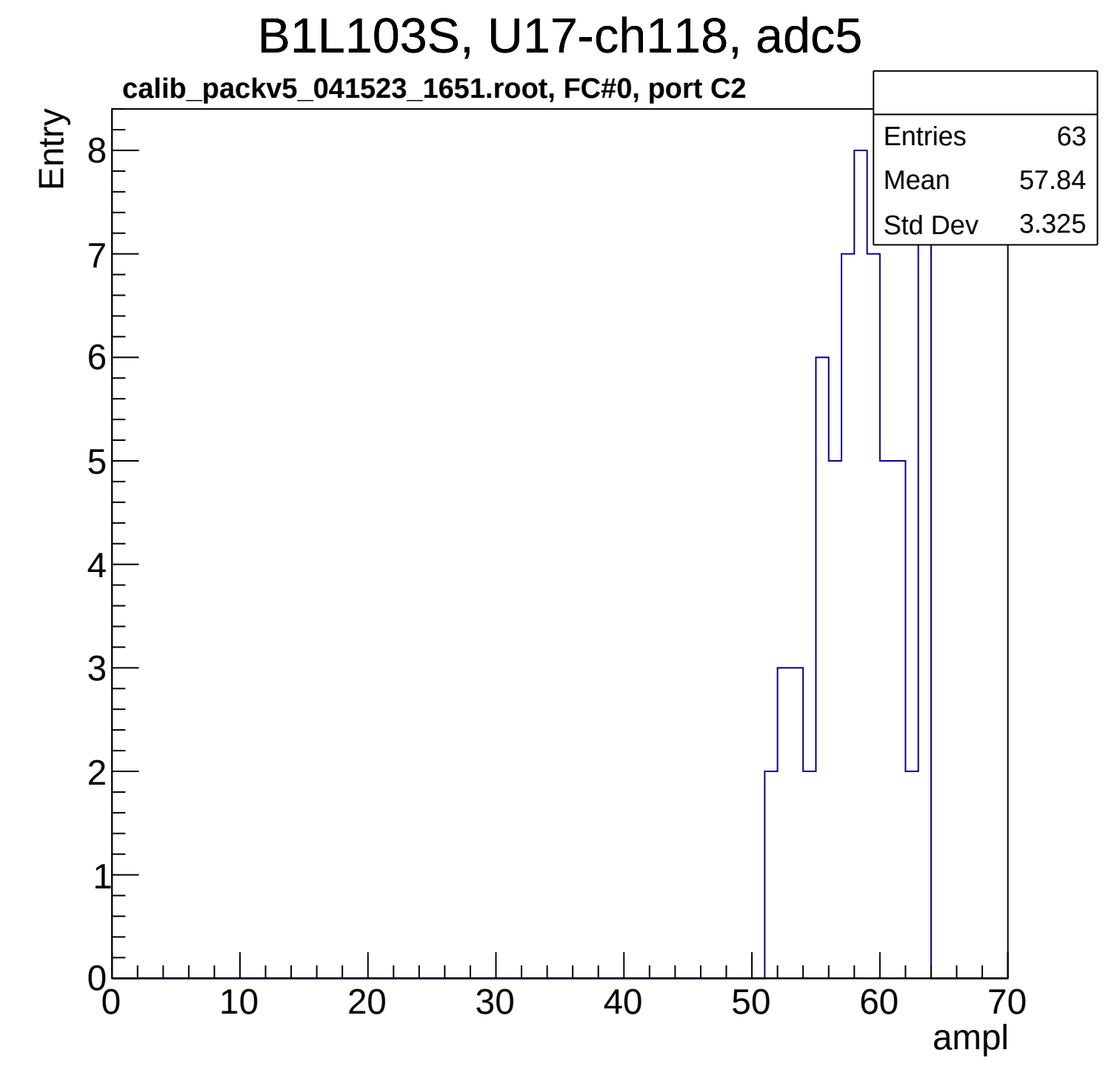

B1L103S, U17-ch118, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 16.75
Std Dev 12.5
Gaus mean : 26.3074
Gaus Width: 3.8840
Entry
ampl
0
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70

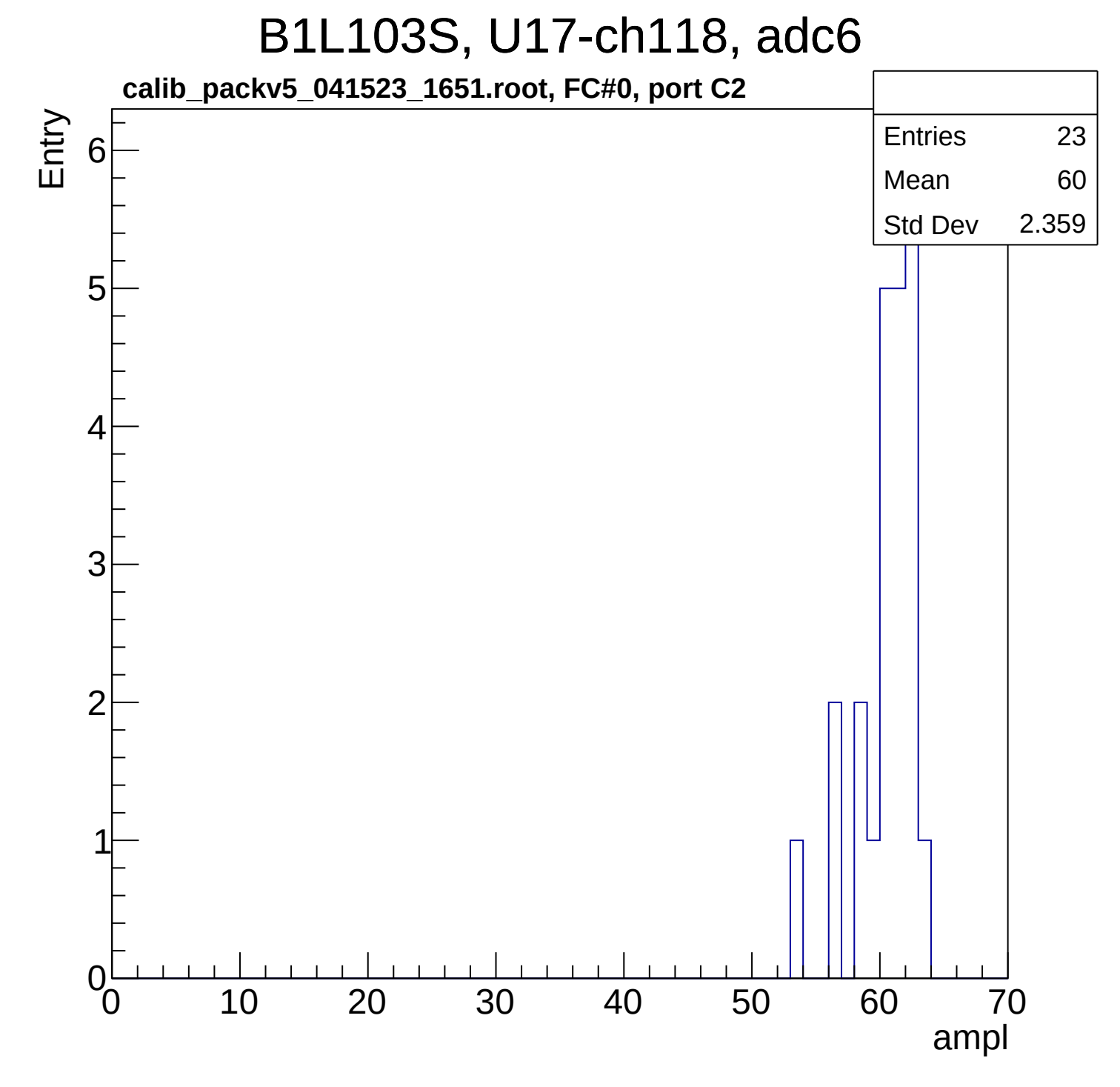

B1L103S, U17-ch118, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 30.49
Std Dev 7.349
Gaus mean : 32.7842
Gaus Width: 4.0479
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

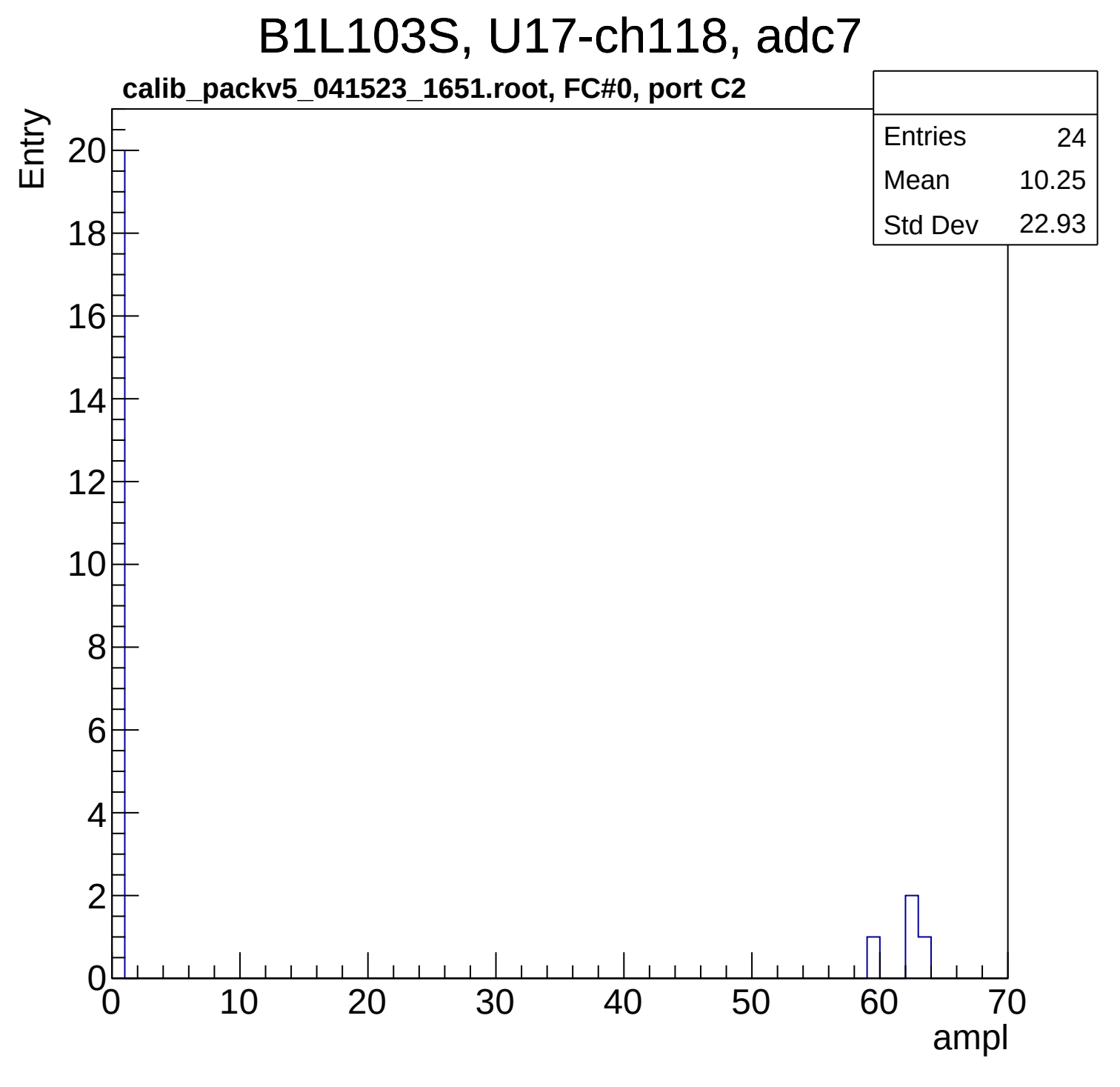

B1L103S, U17-ch118, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 33.33
Std Dev 13.62
Gaus mean : 38.9349
Gaus Width: 4.5953
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

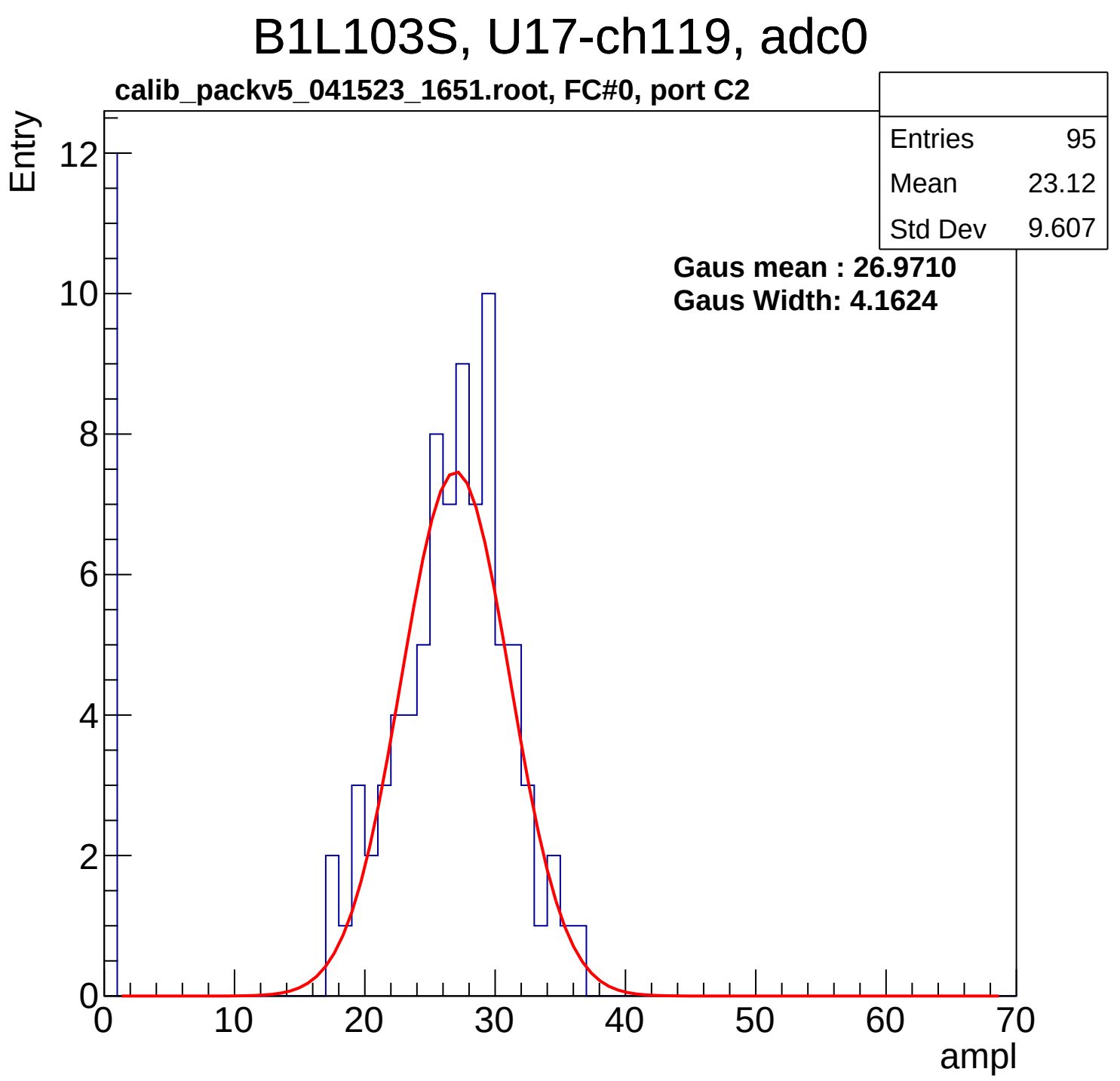

B1L103S, U17-ch118, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 43.7
Std Dev 9.566
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

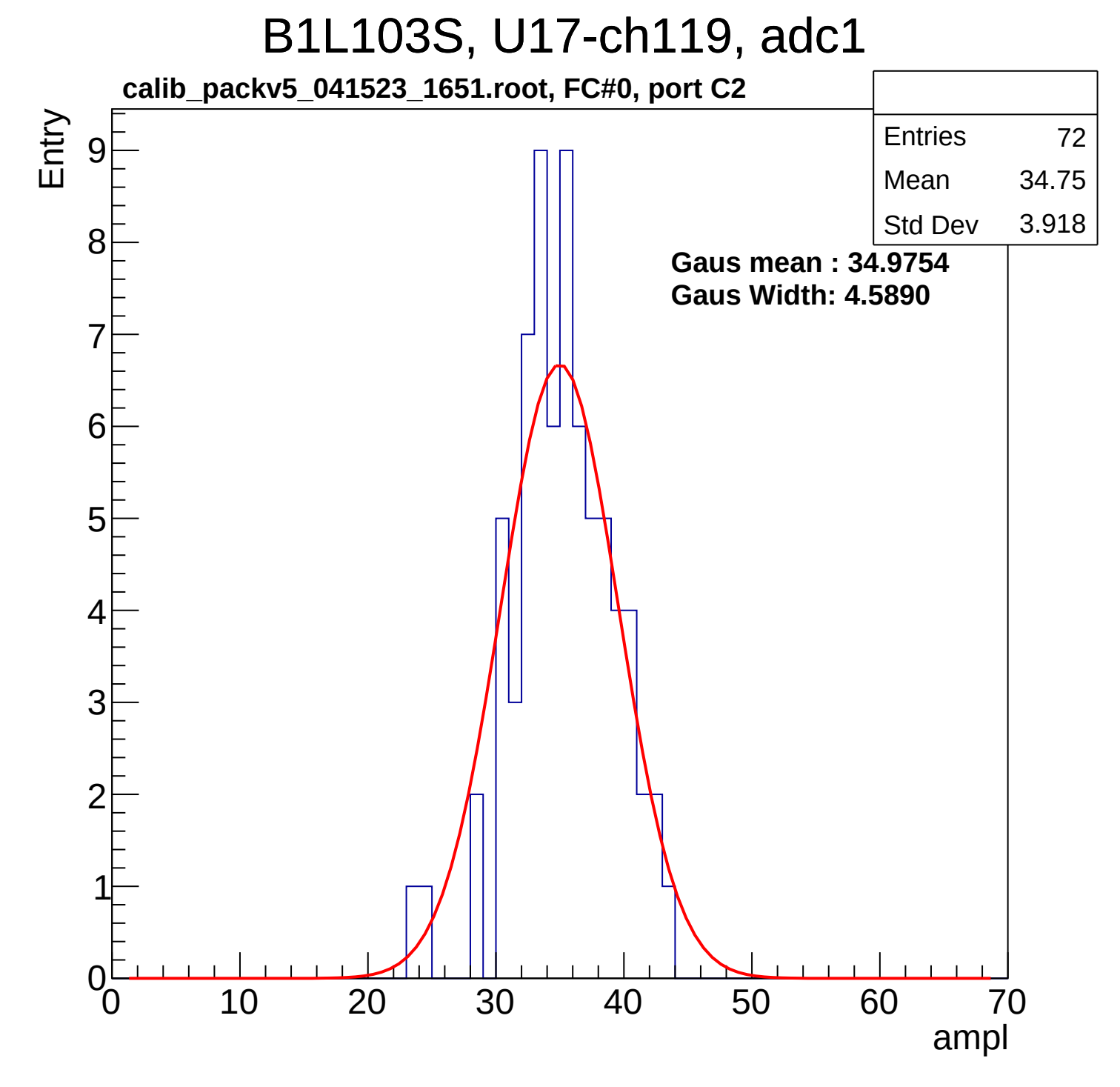

B1L103S, U17-ch118, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 51.33
Std Dev 3.88
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

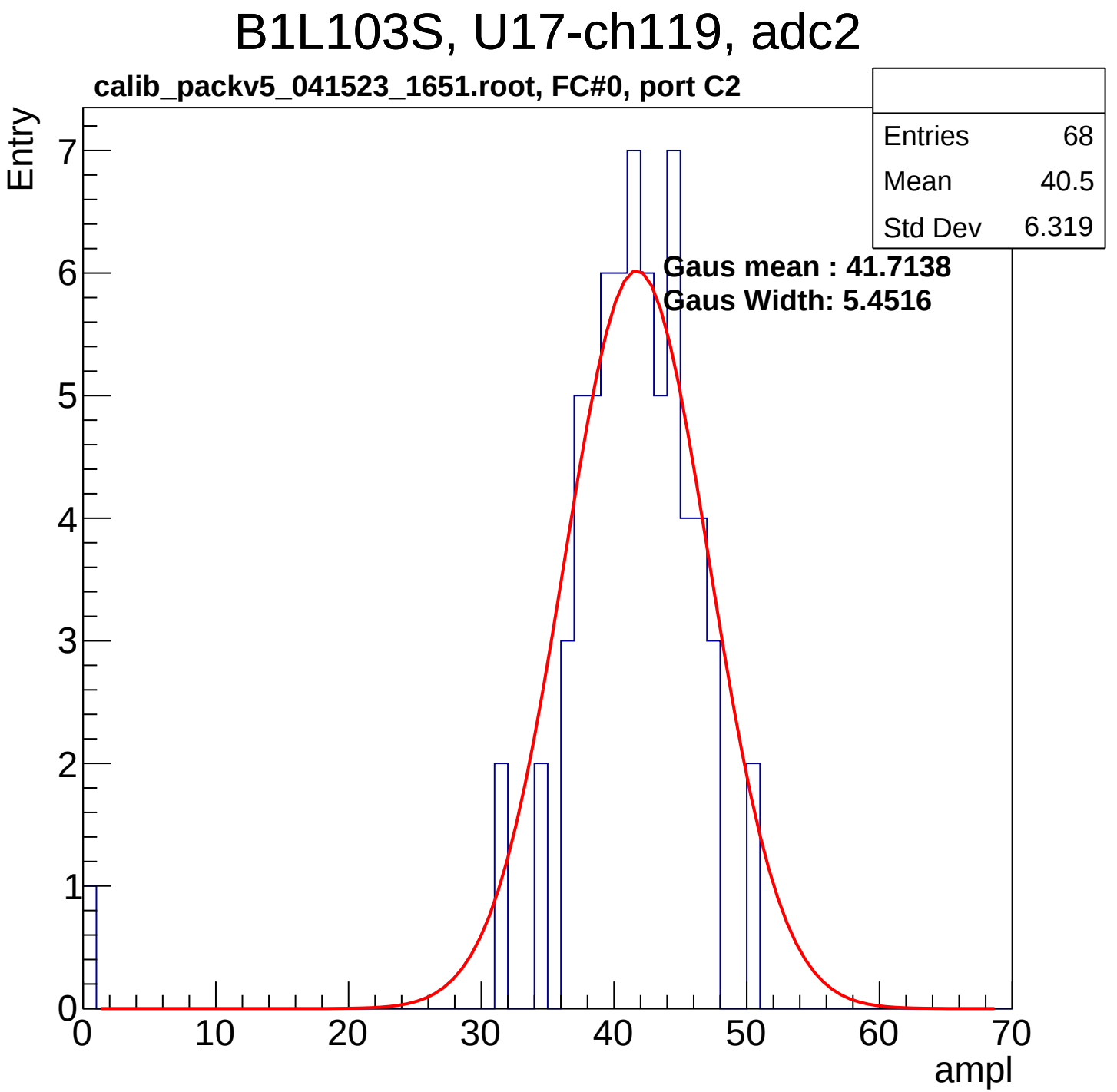

B1L103S, U17-ch118, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 57.84
Std Dev 3.325
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

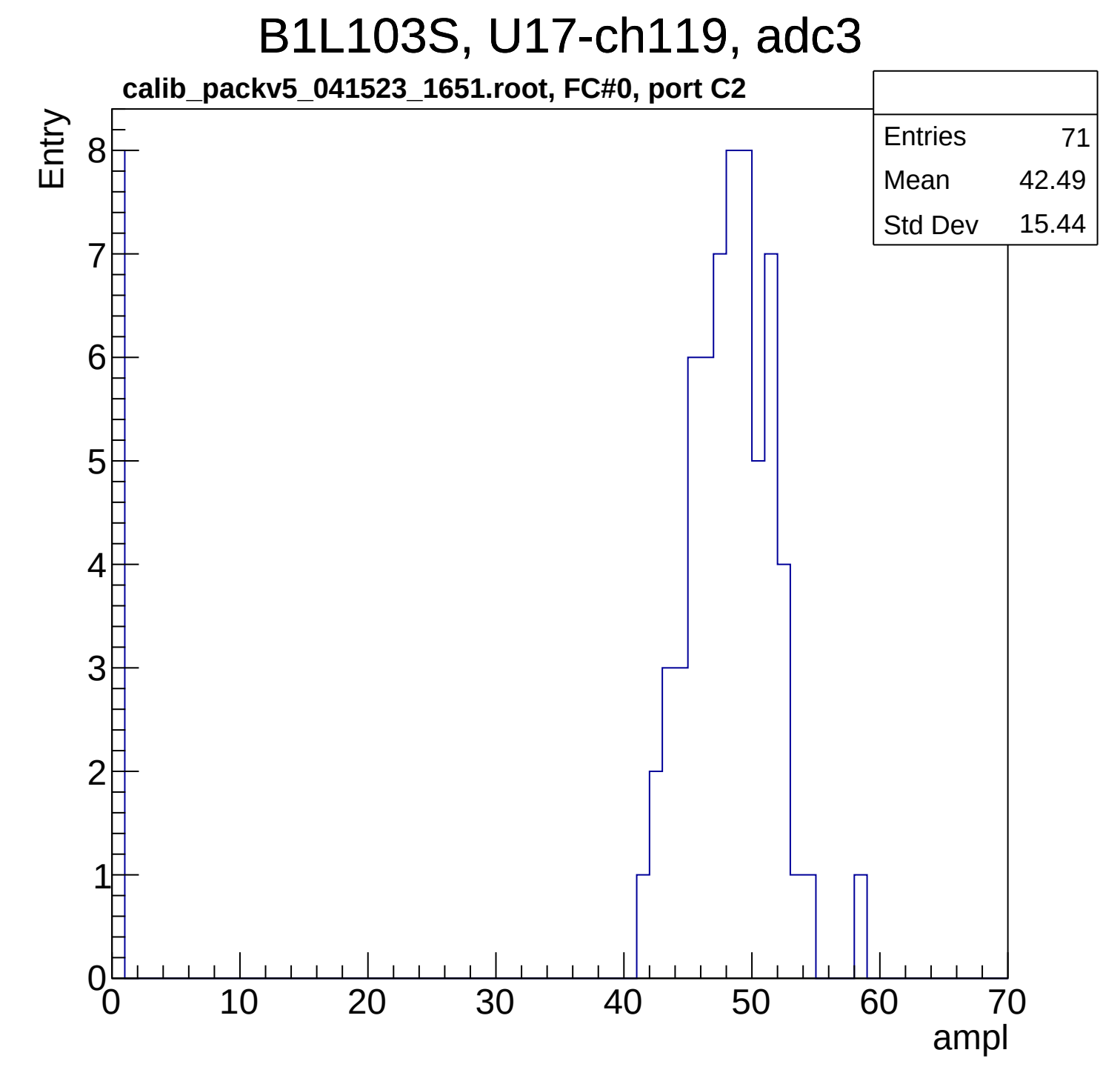

B1L103S, U17-ch118, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 60
Std Dev 2.359
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

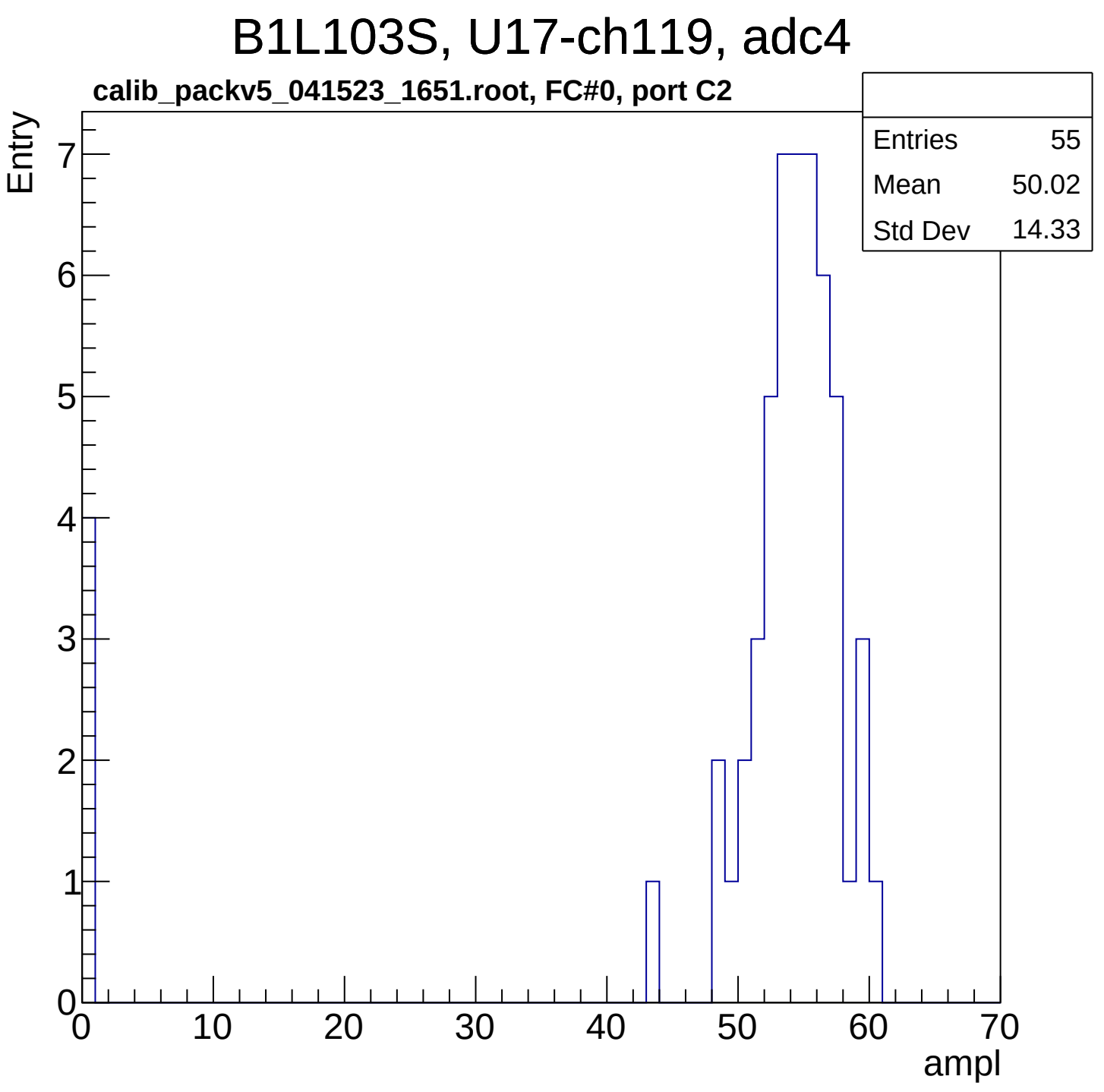

B1L103S, U17-ch118, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 10.25
Std Dev 22.93
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

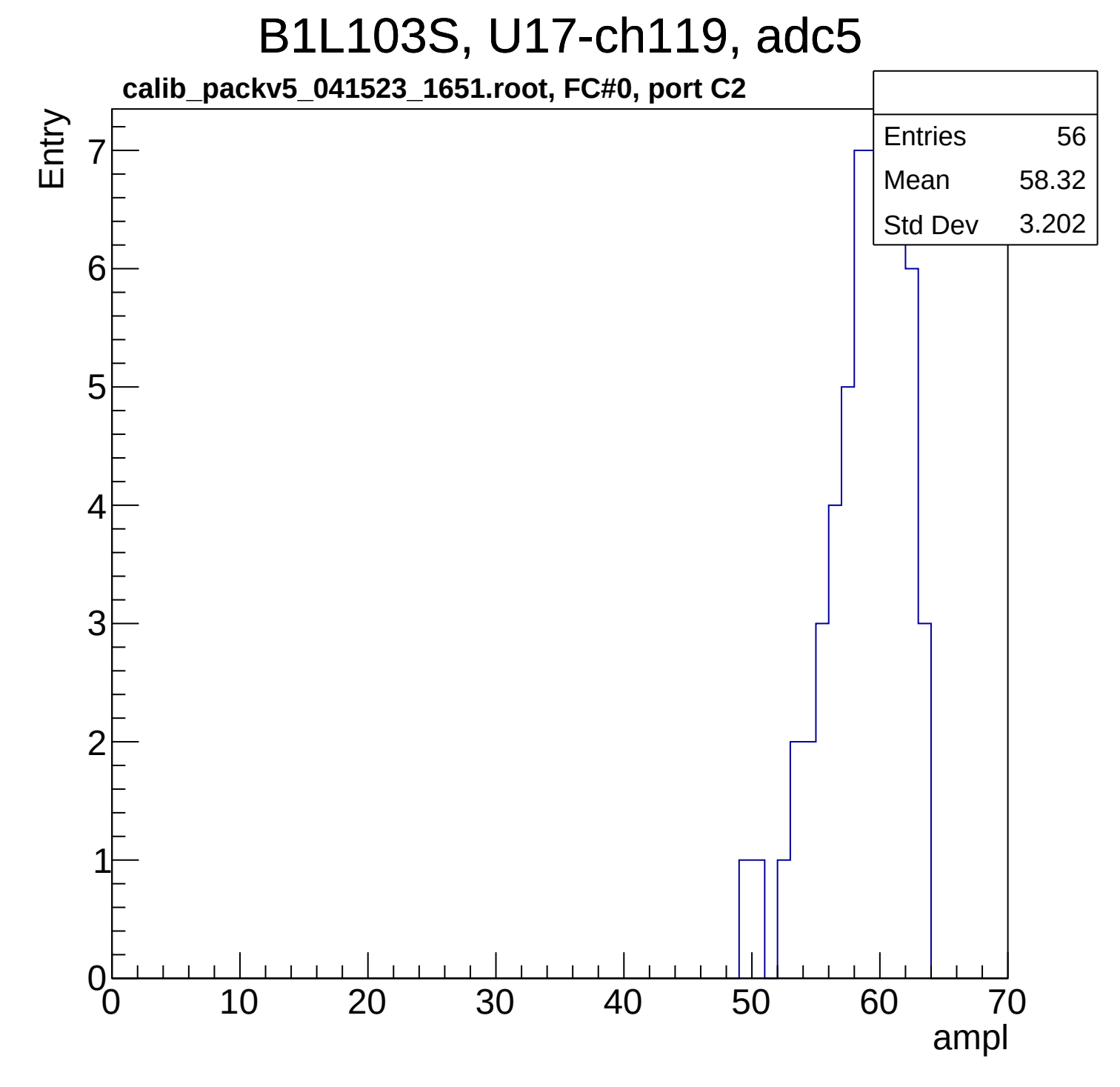

B1L103S, U17-ch119, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 23.12
Std Dev 9.607
Gaus mean : 26.9710
Gaus Width: 4.1624
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

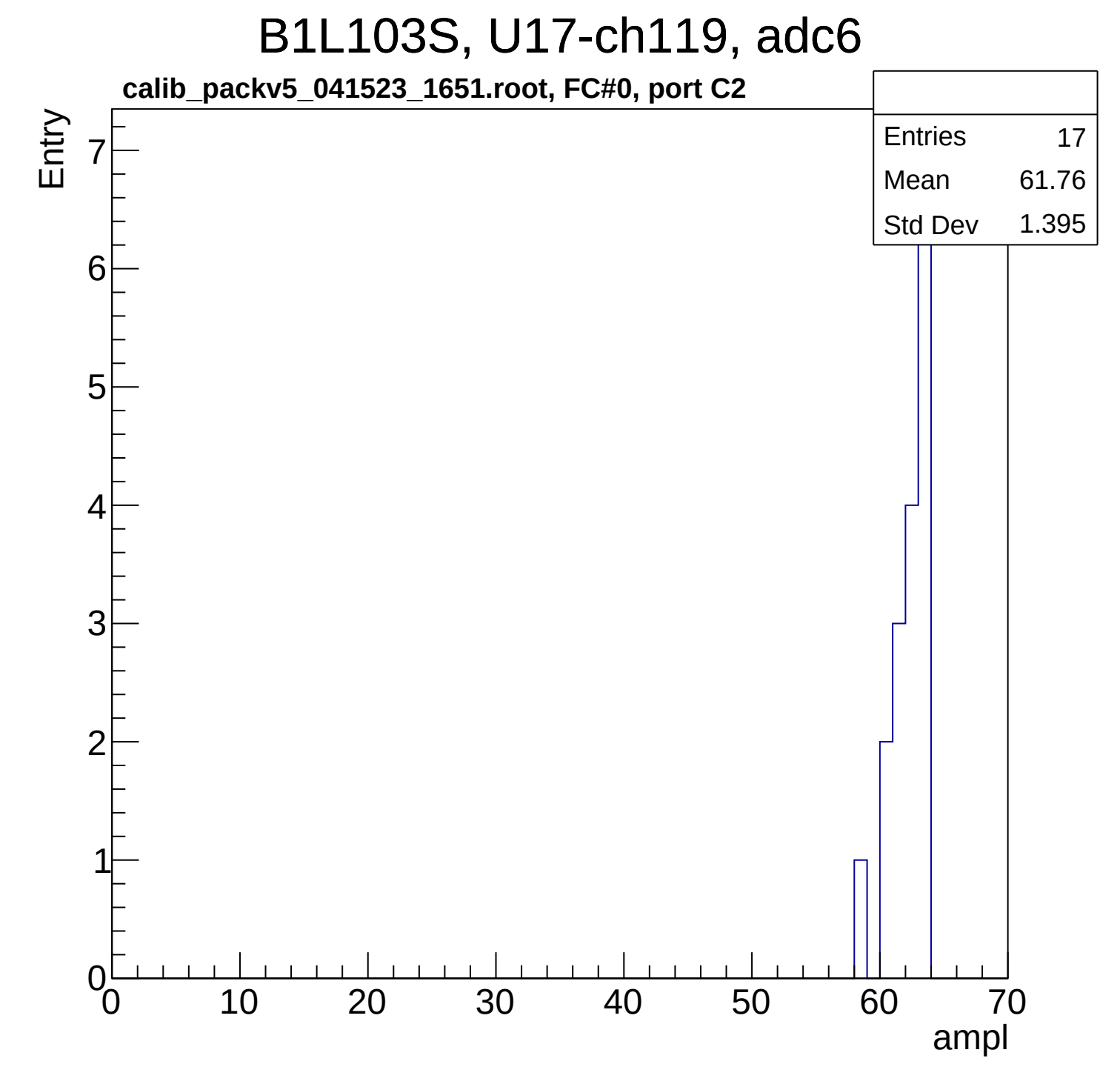

B1L103S, U17-ch119, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 34.75
Std Dev 3.918
Gaus mean : 34.9754
Gaus Width: 4.5890
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

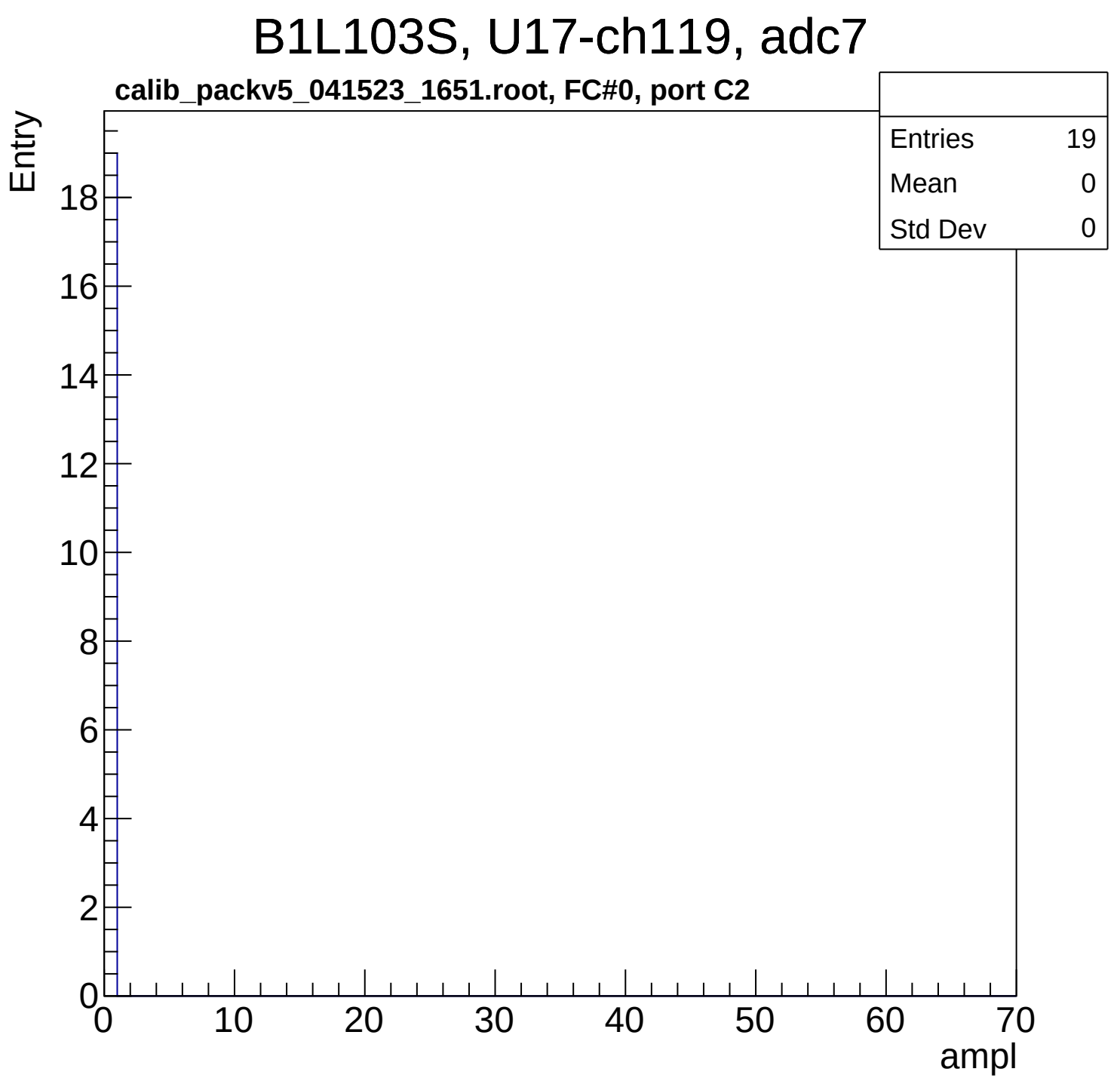

B1L103S, U17-ch119, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 40.5
Std Dev 6.319
Gaus mean : 41.7138
Gaus Width: 5.4516
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

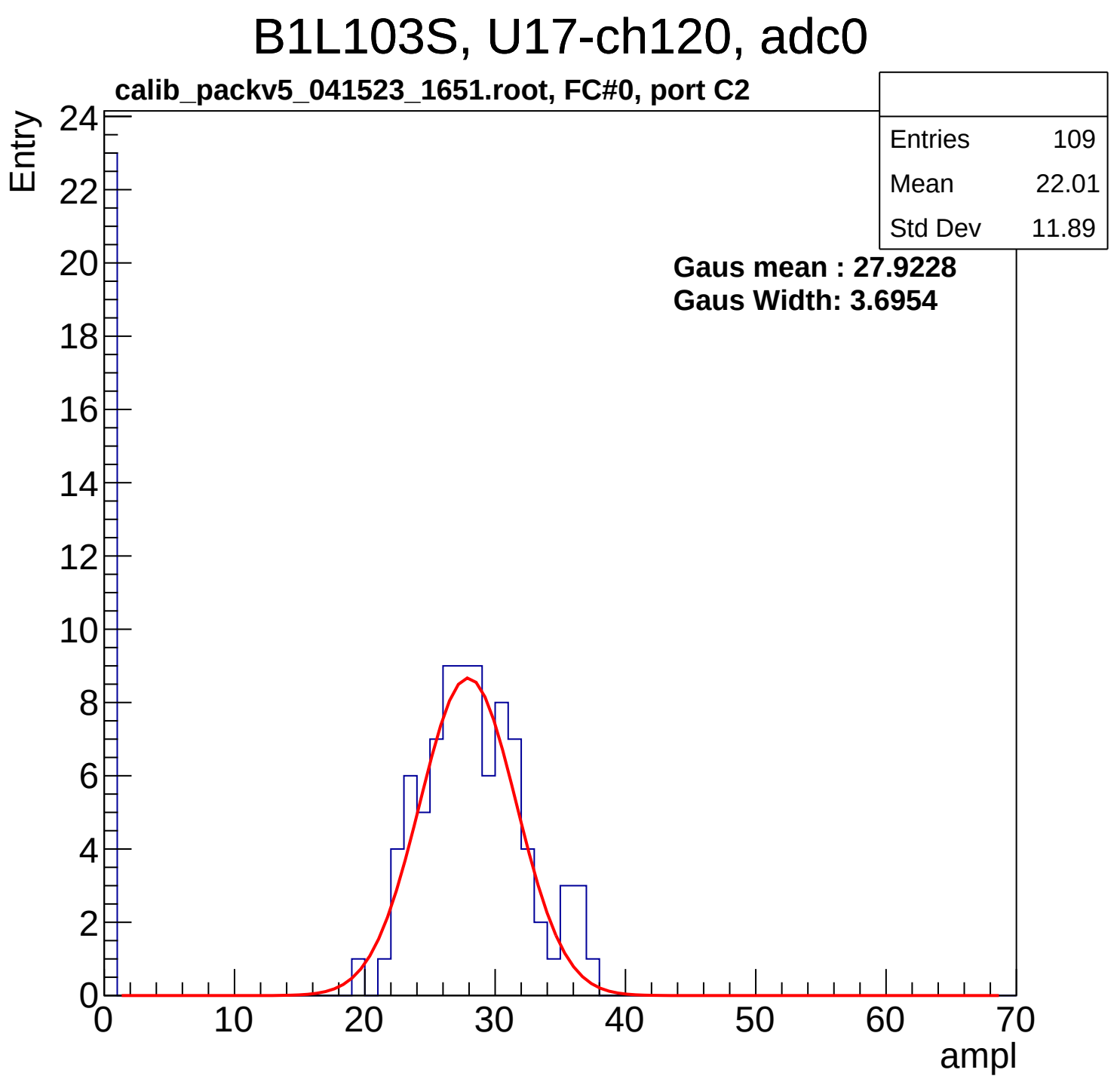

B1L103S, U17-ch119, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 42.49
Std Dev 15.44
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

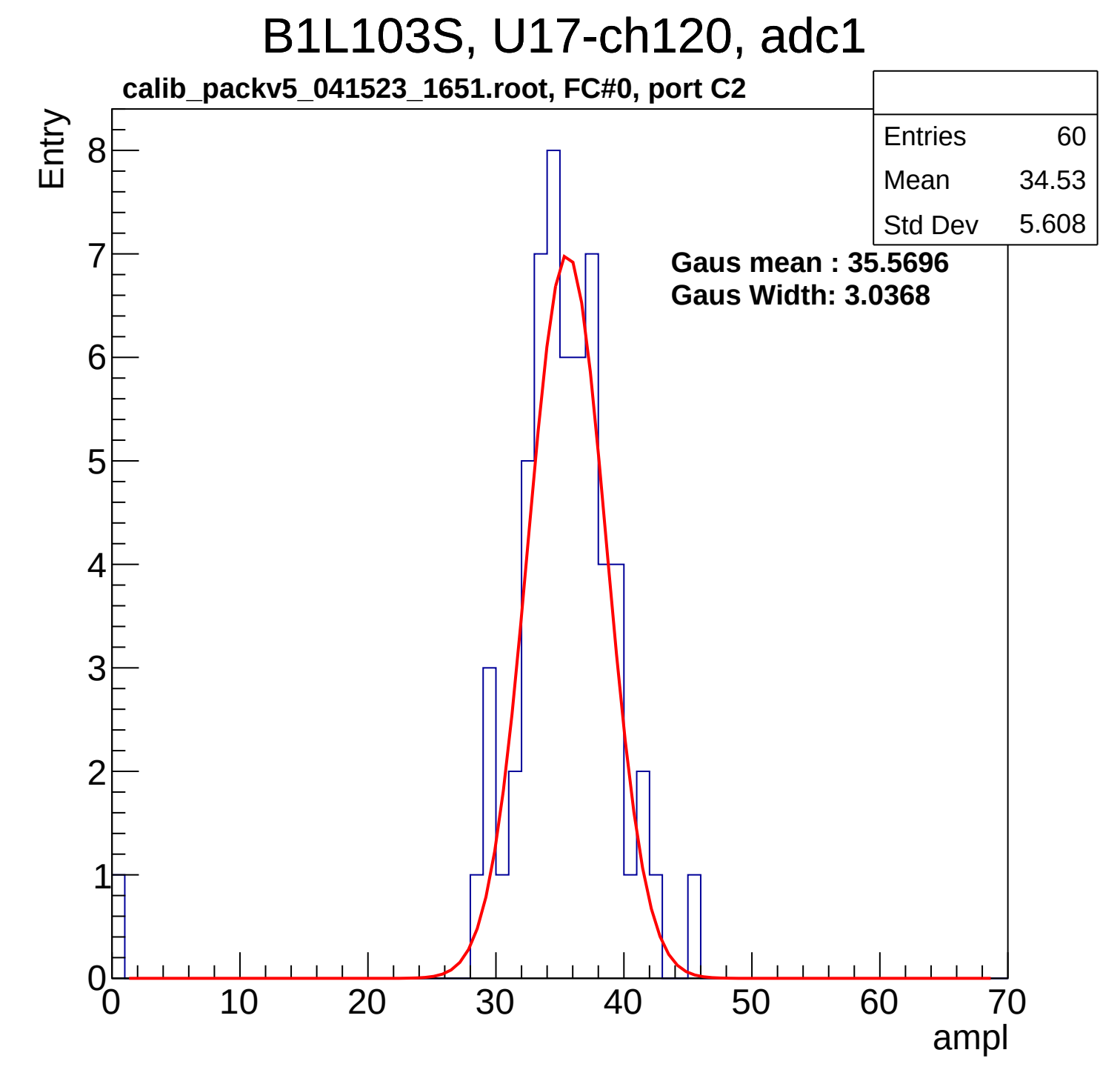

B1L103S, U17-ch119, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 50.02
Std Dev 14.33
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

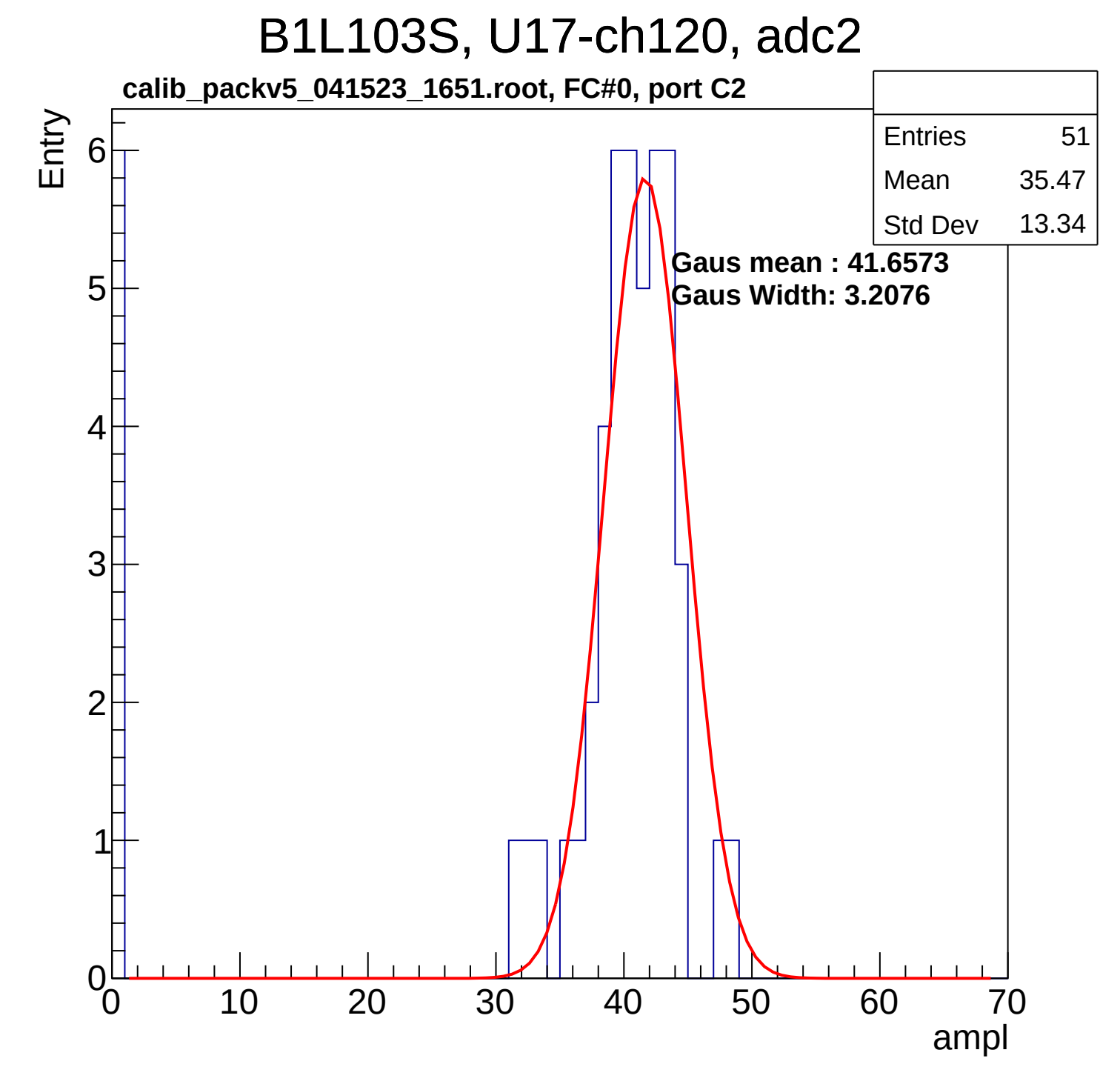

B1L103S, U17-ch119, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.32
Std Dev 3.202
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

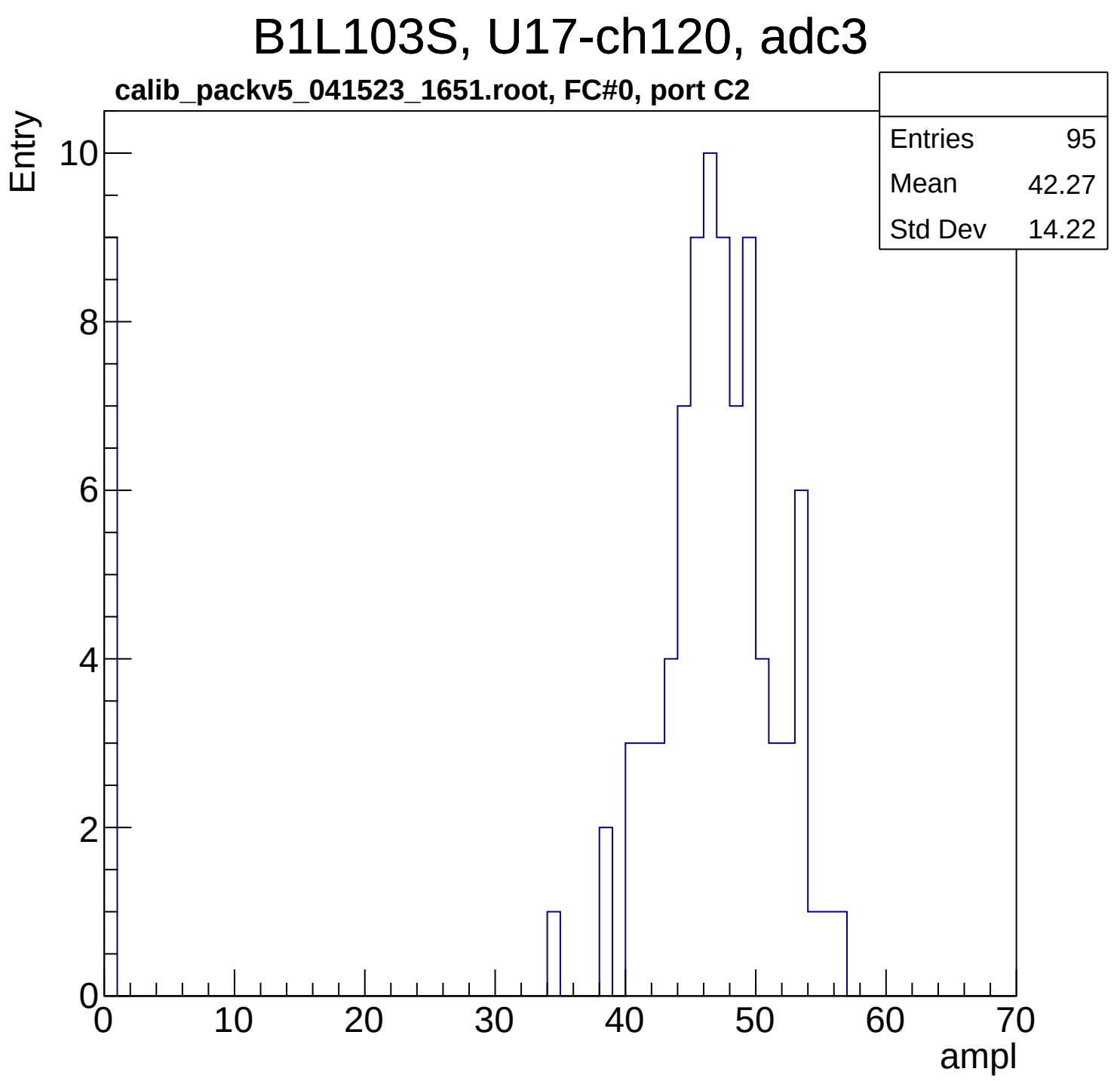

B1L103S, U17-ch119, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.76
Std Dev 1.395
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

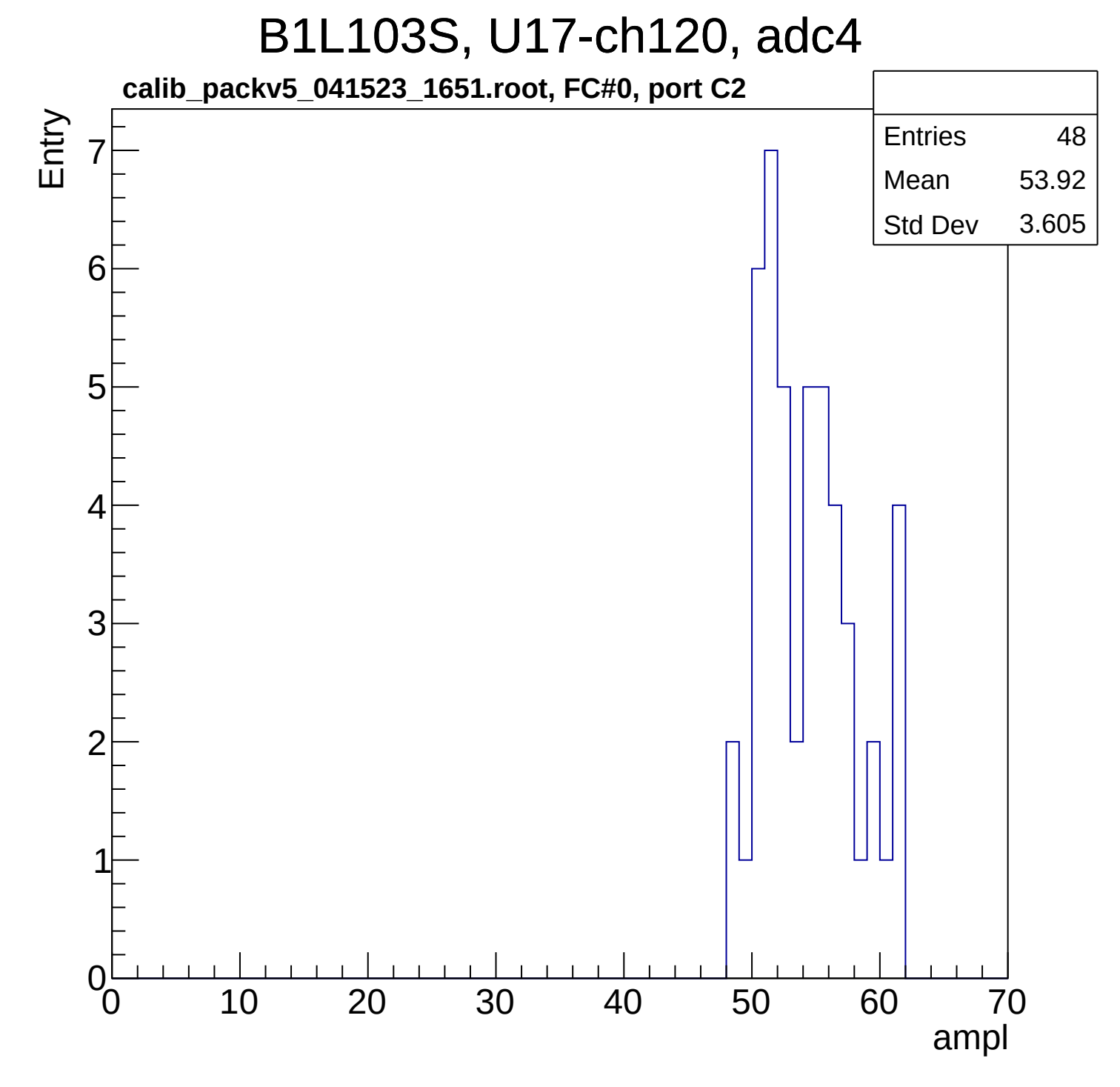

B1L103S, U17-ch119, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

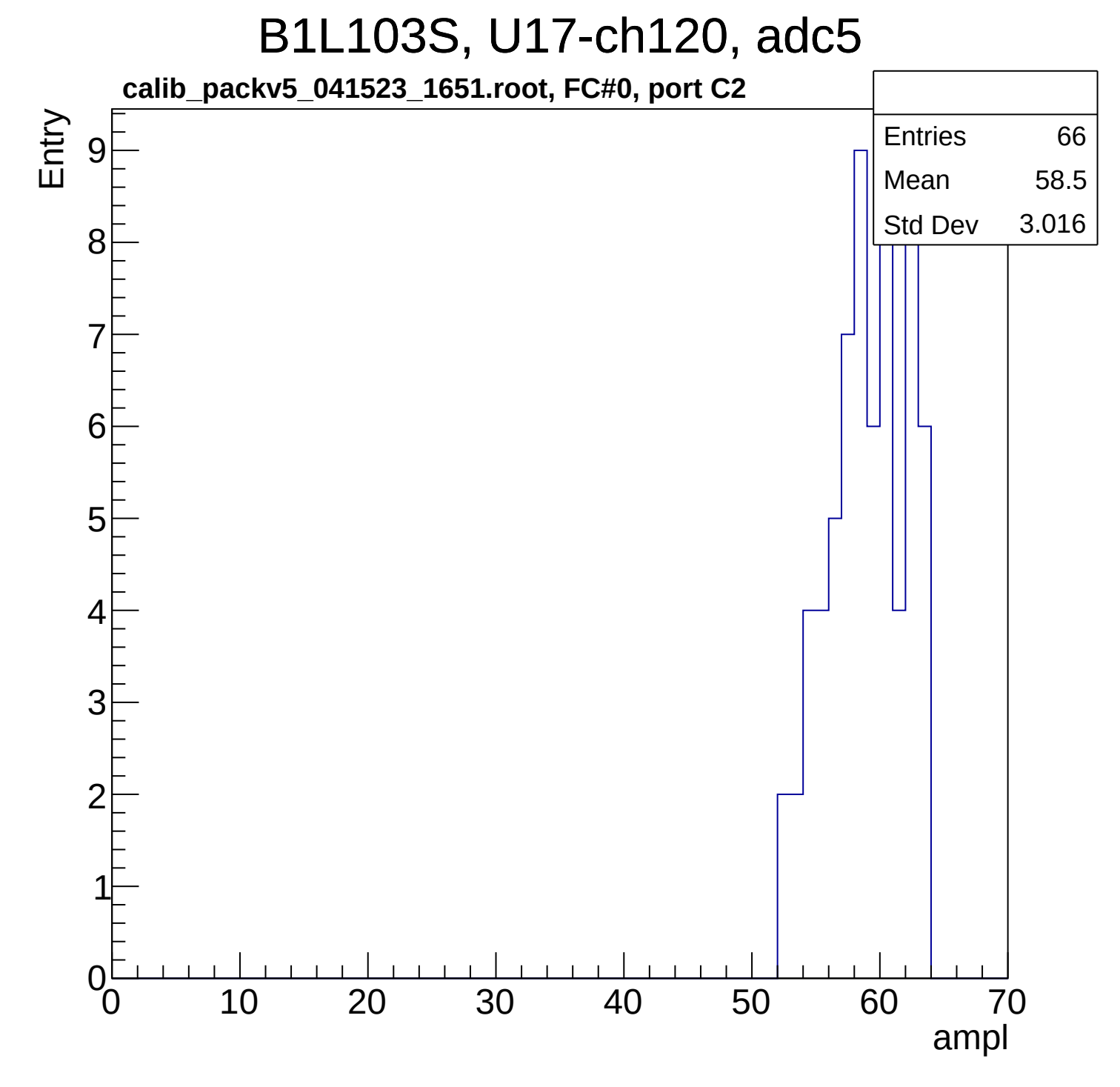

B1L103S, U17-ch120, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 109
Mean 22.01
Std Dev 11.89
Gaus mean : 27.9228
Gaus Width: 3.6954
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70

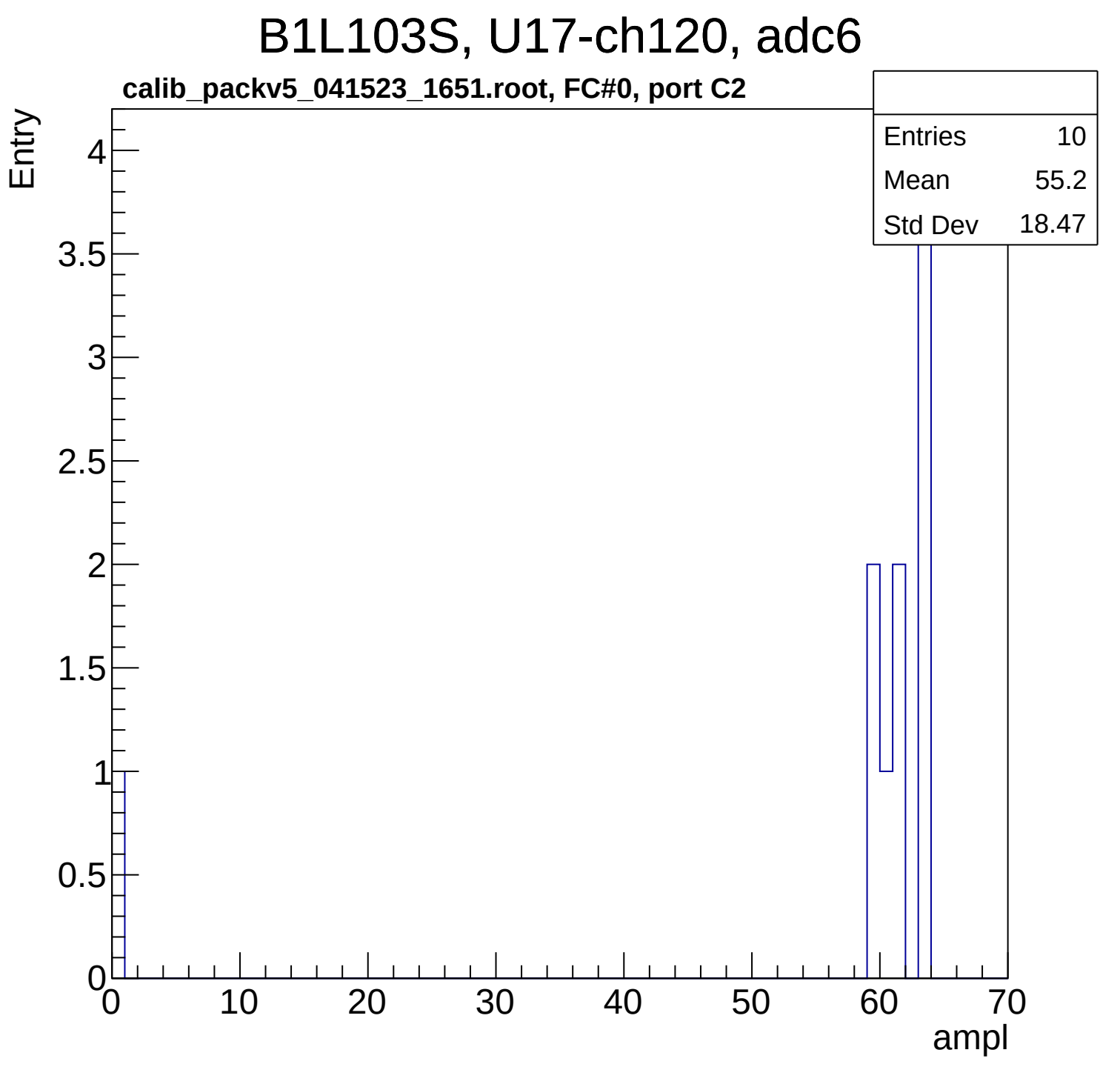

B1L103S, U17-ch120, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 34.53
Std Dev 5.608
Gaus mean : 35.5696
Gaus Width: 3.0368
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

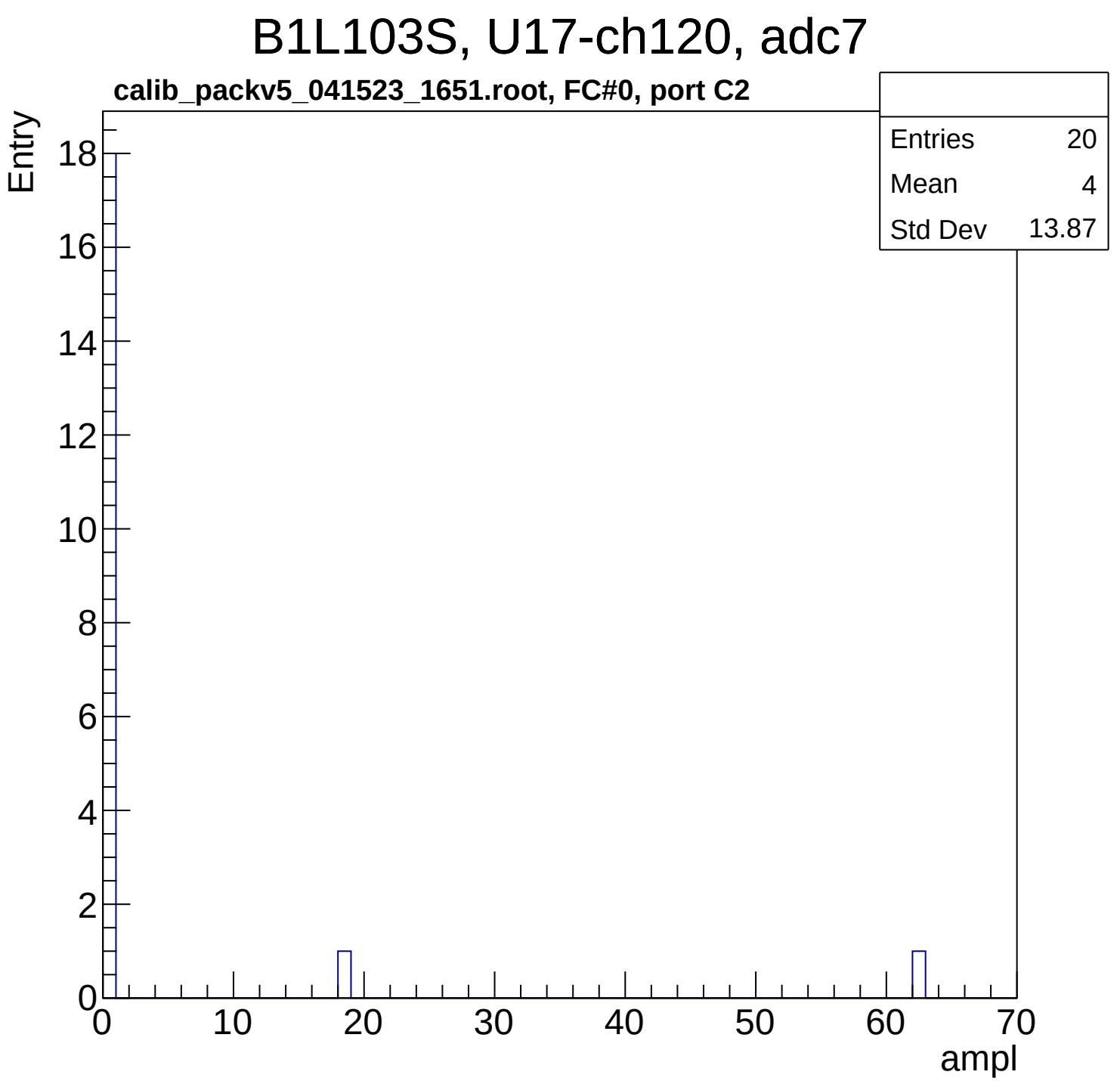

B1L103S, U17-ch120, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 35.47
Std Dev 13.34
Gaus mean : 41.6573
Gaus Width: 3.2076
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

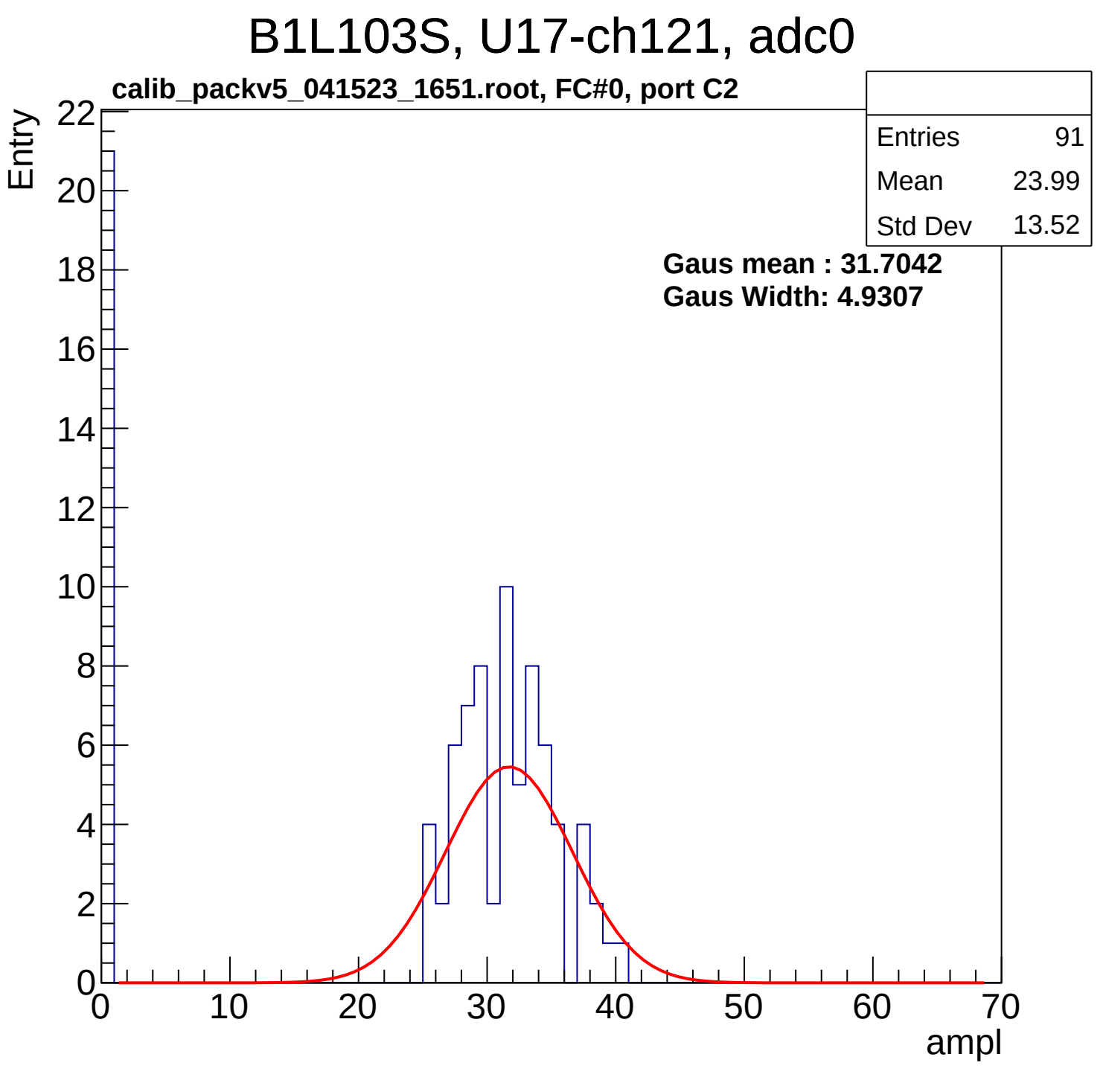

B1L103S, U17-ch120, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 42.27
Std Dev 14.22
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

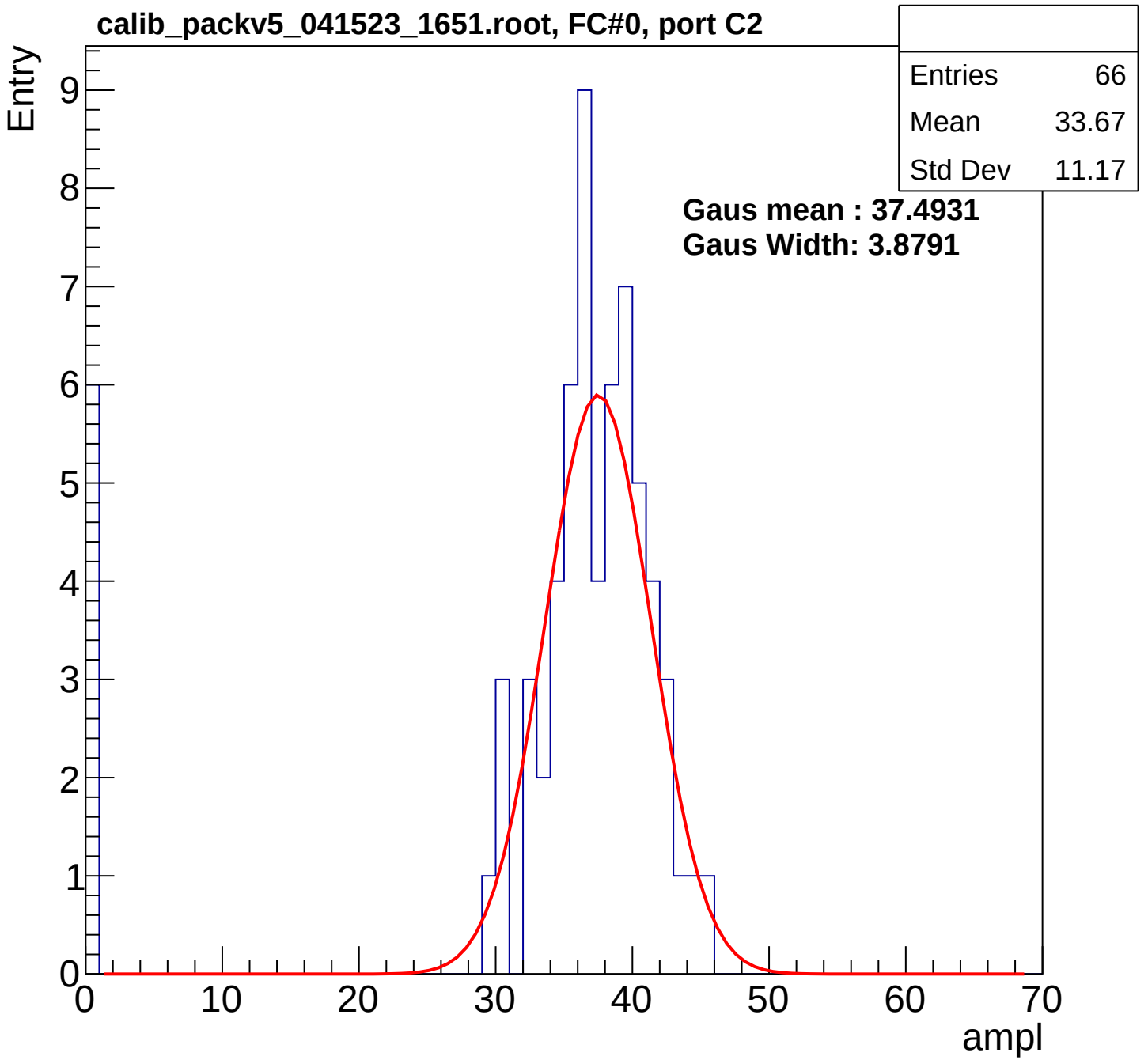

B1L103S, U17-ch120, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 53.92
Std Dev 3.605
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

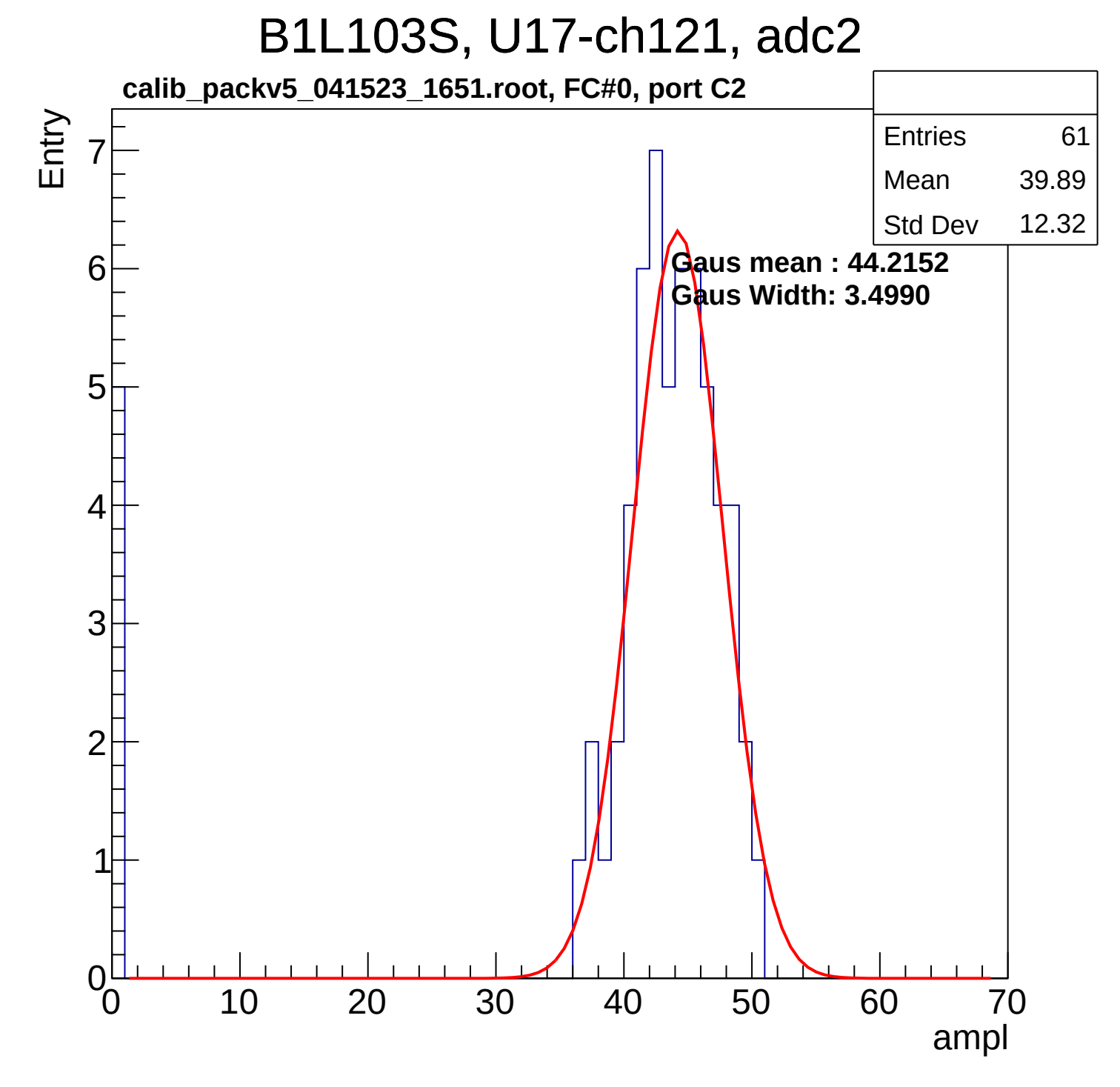

B1L103S, U17-ch120, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 58.5
Std Dev 3.016
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

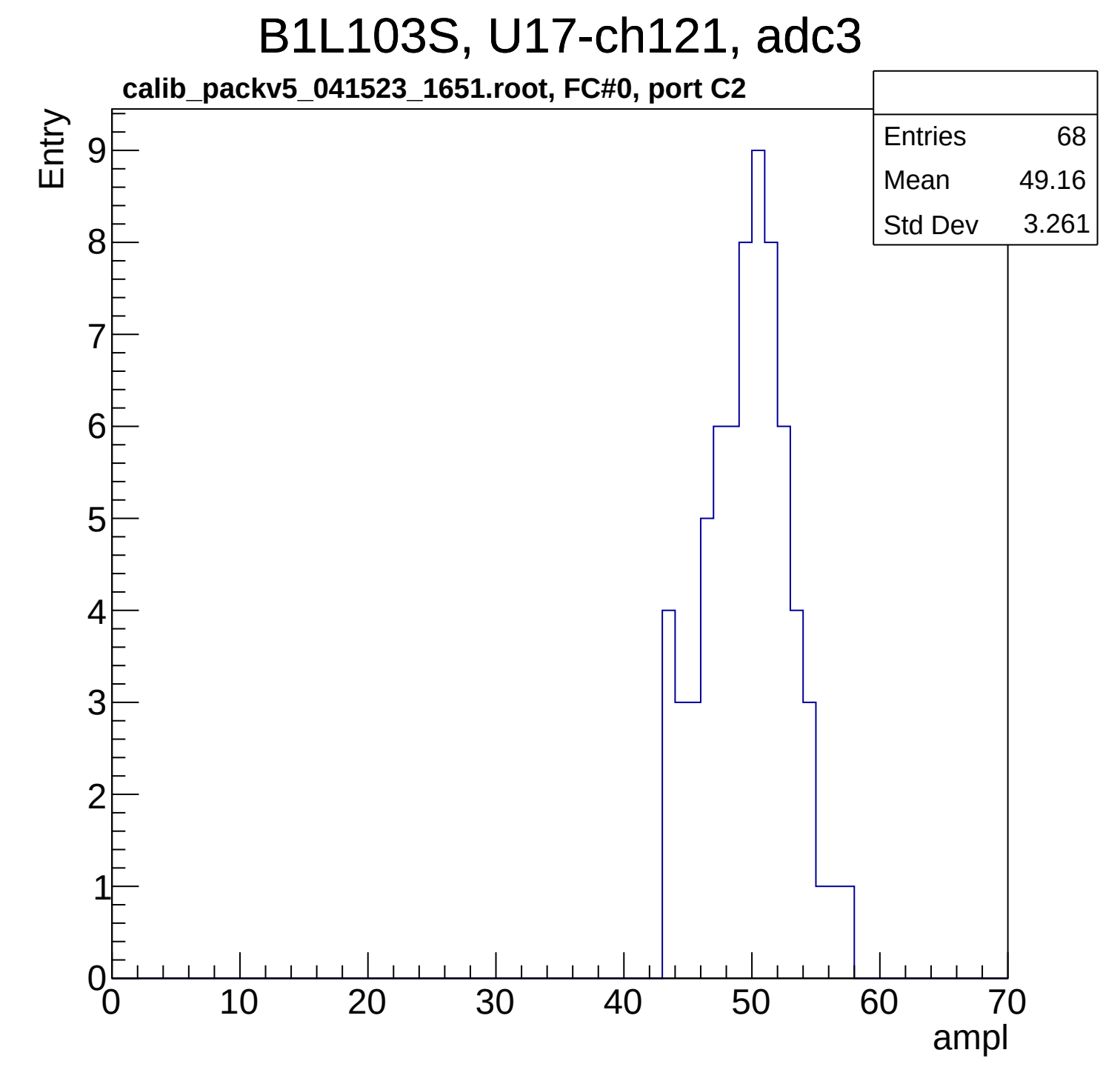

B1L103S, U17-ch120, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.2
Std Dev 18.47
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

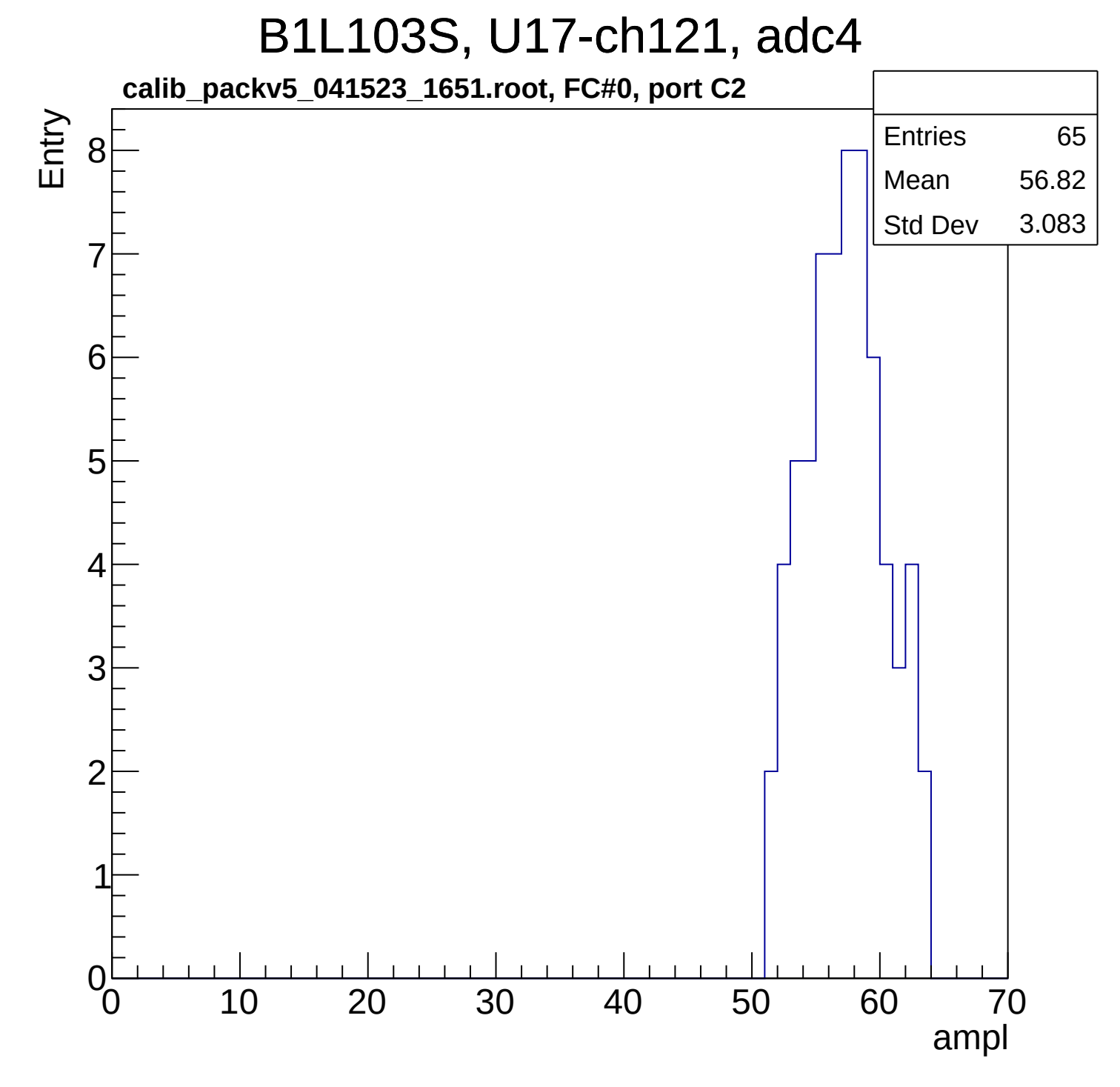

B1L103S, U17-ch120, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4
Std Dev 13.87
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

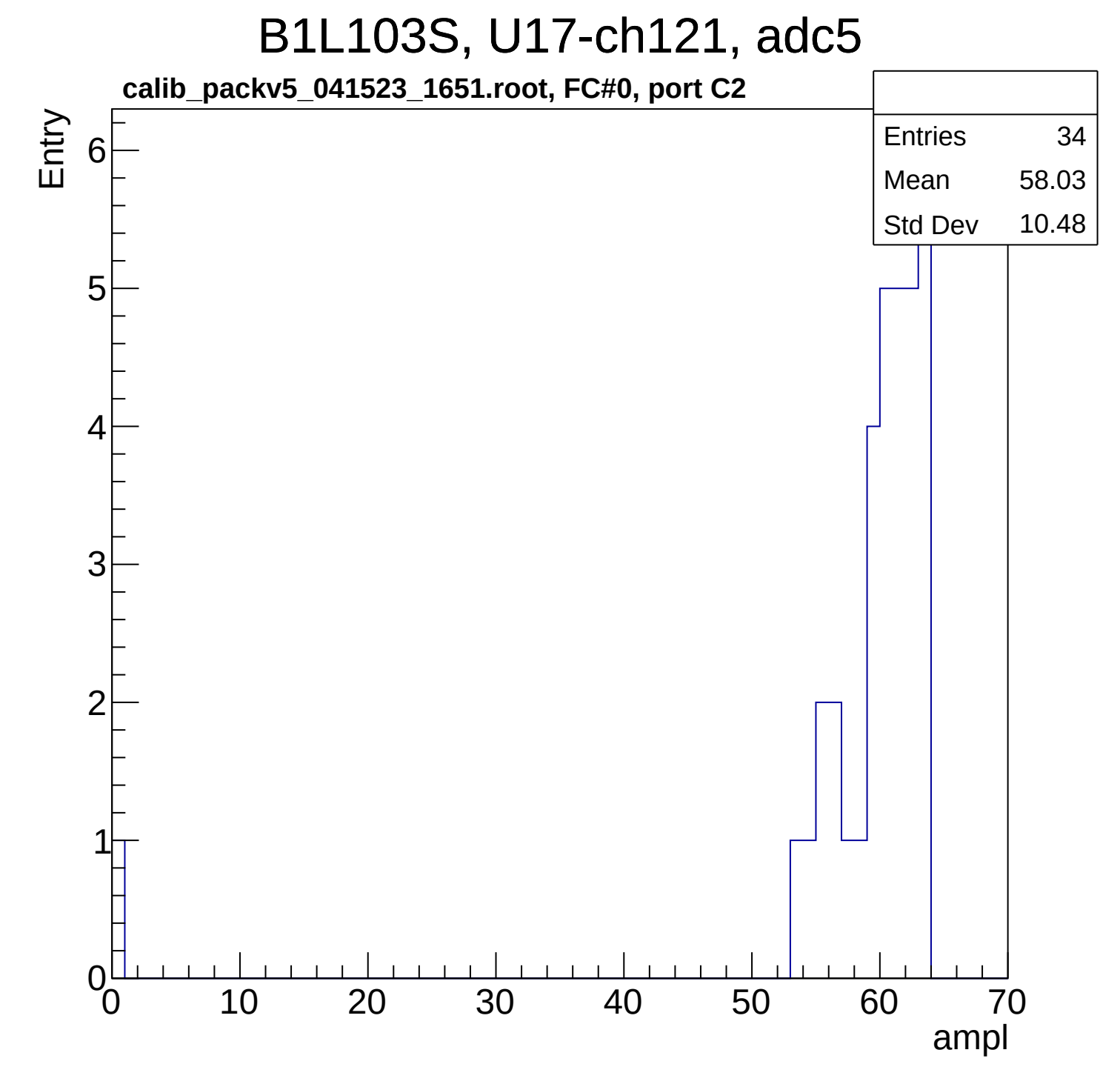

B1L103S, U17-ch121, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 23.99
Std Dev 13.52
Gaus mean : 31.7042
Gaus Width: 4.9307
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70

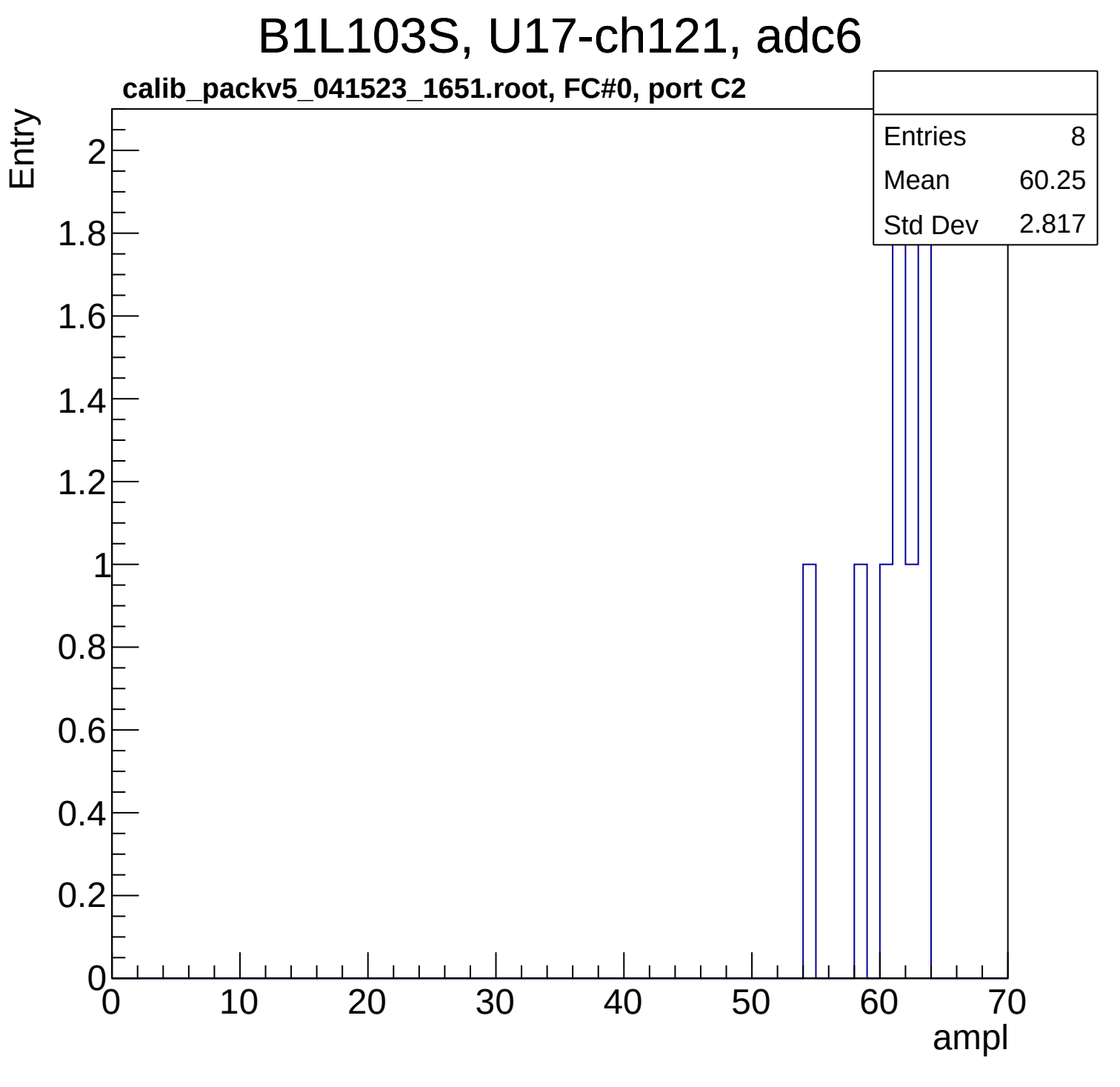

B1L103S, U17-ch121, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 33.67
Std Dev 11.17
Gaus mean : 37.4931
Gaus Width: 3.8791
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

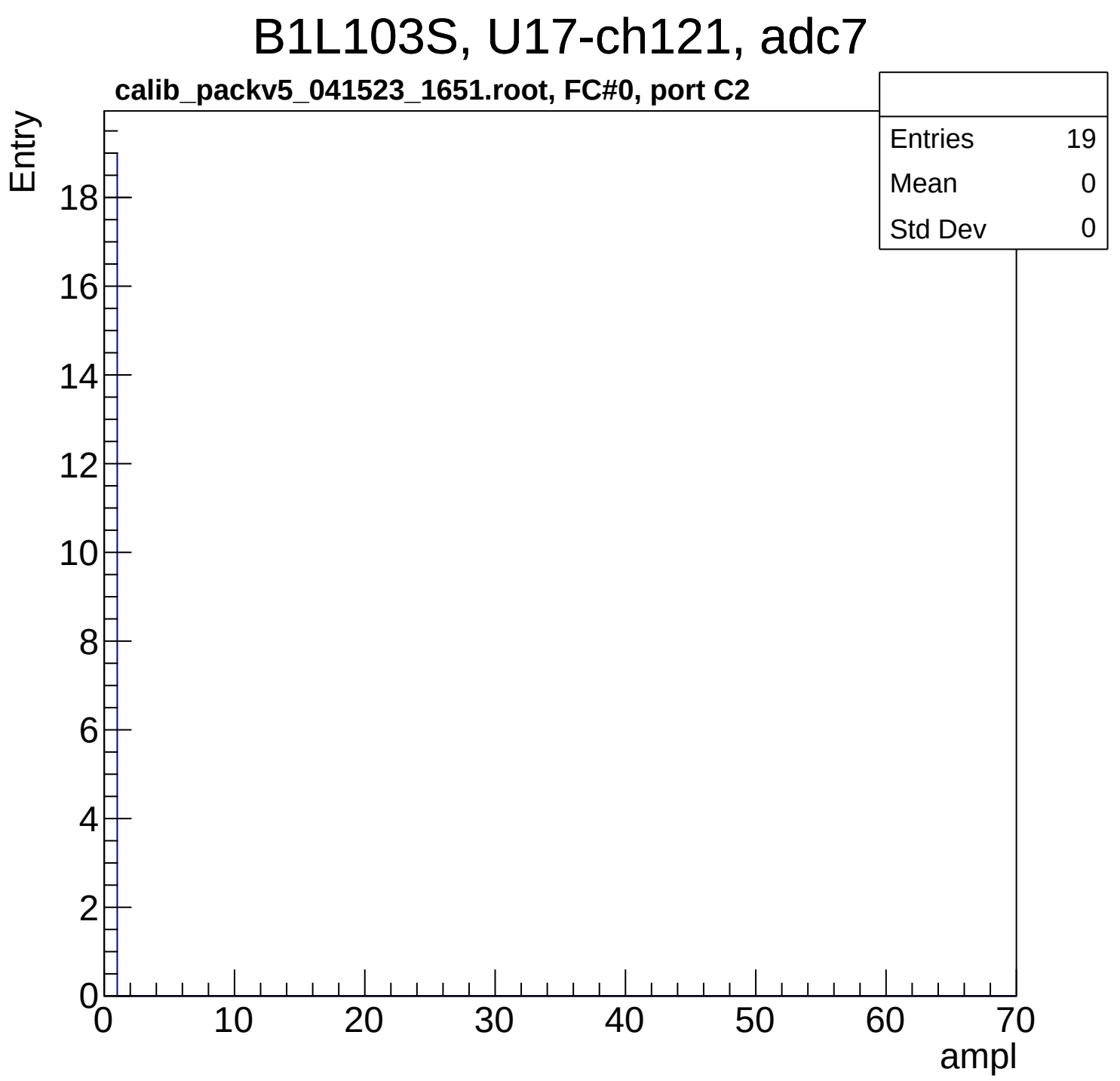

B1L103S, U17-ch121, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 39.89
Std Dev 12.32
Gaus mean : 44.2152
Gaus Width: 3.4990
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

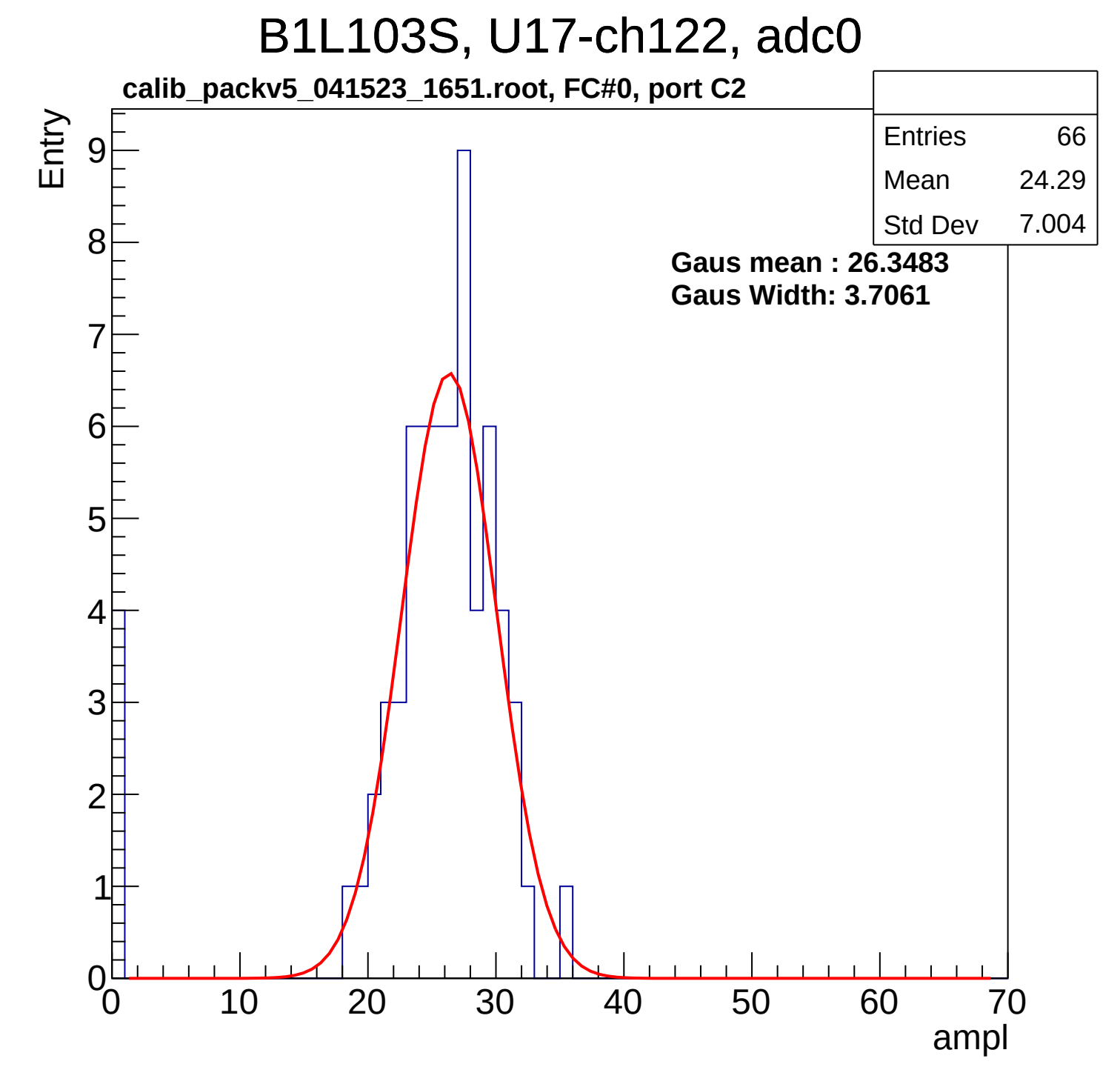

B1L103S, U17-ch121, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 49.16
Std Dev 3.261
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

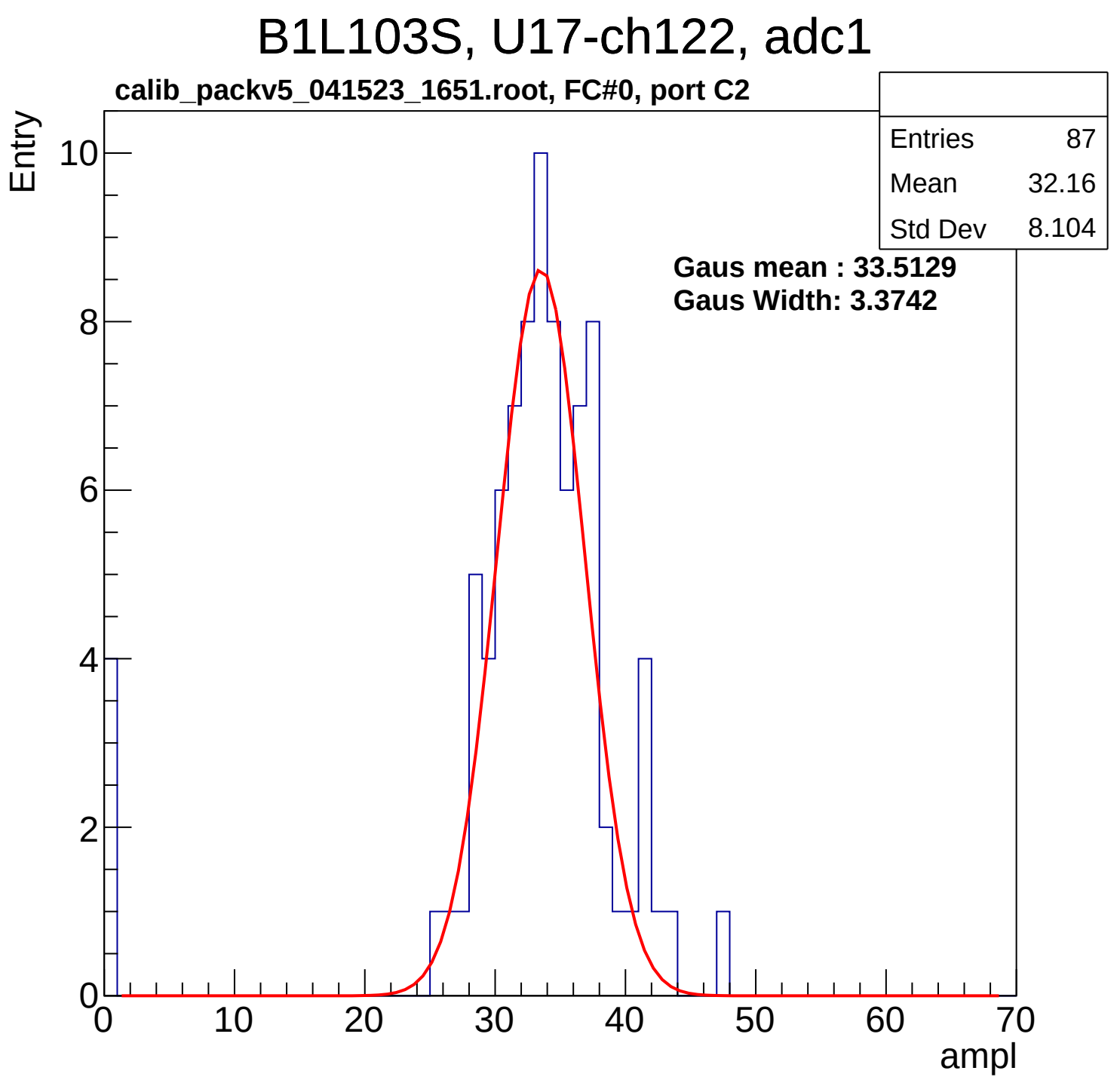

B1L103S, U17-ch121, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 56.82
Std Dev 3.083
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

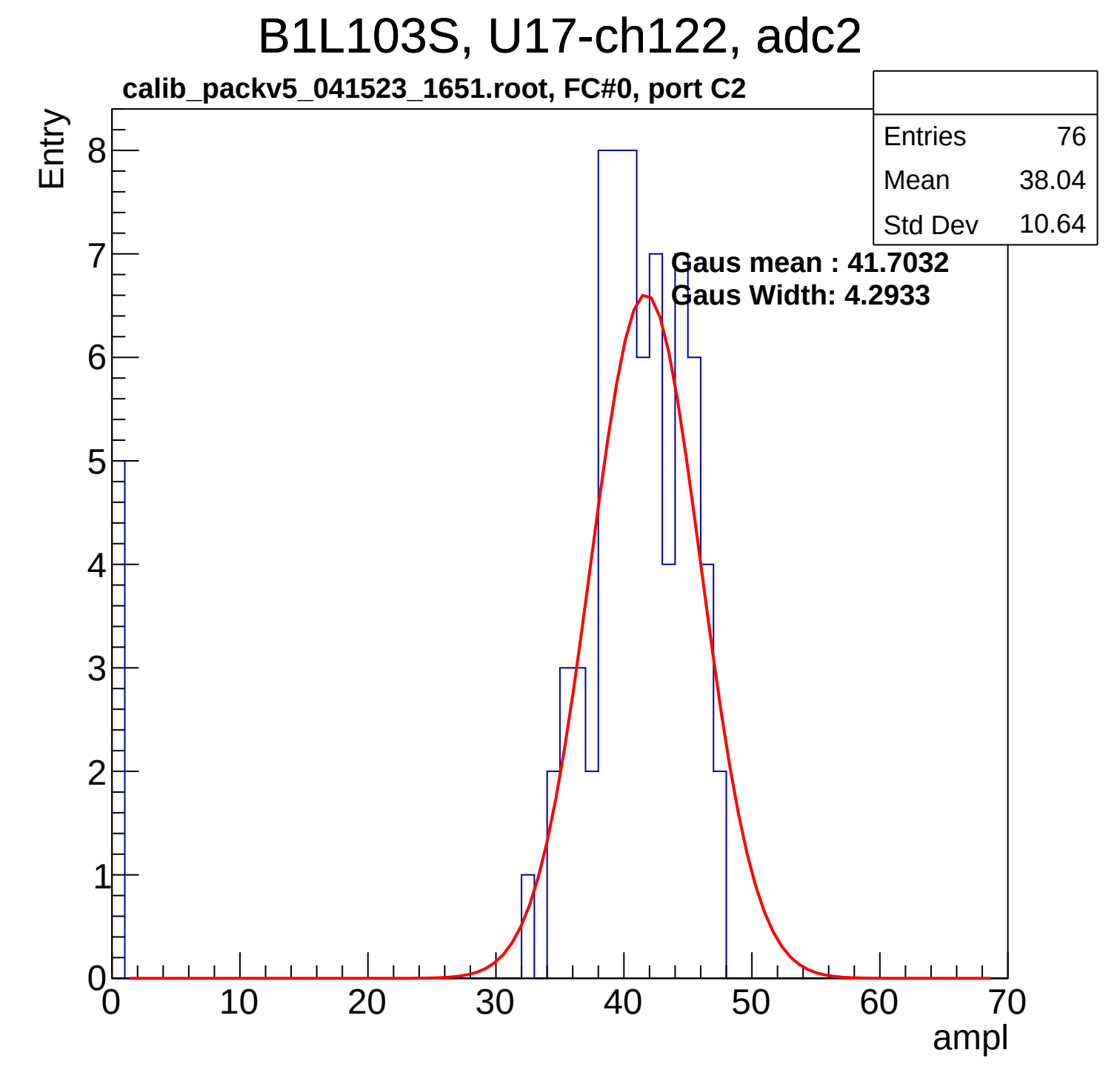

B1L103S, U17-ch121, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 58.03
Std Dev 10.48
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

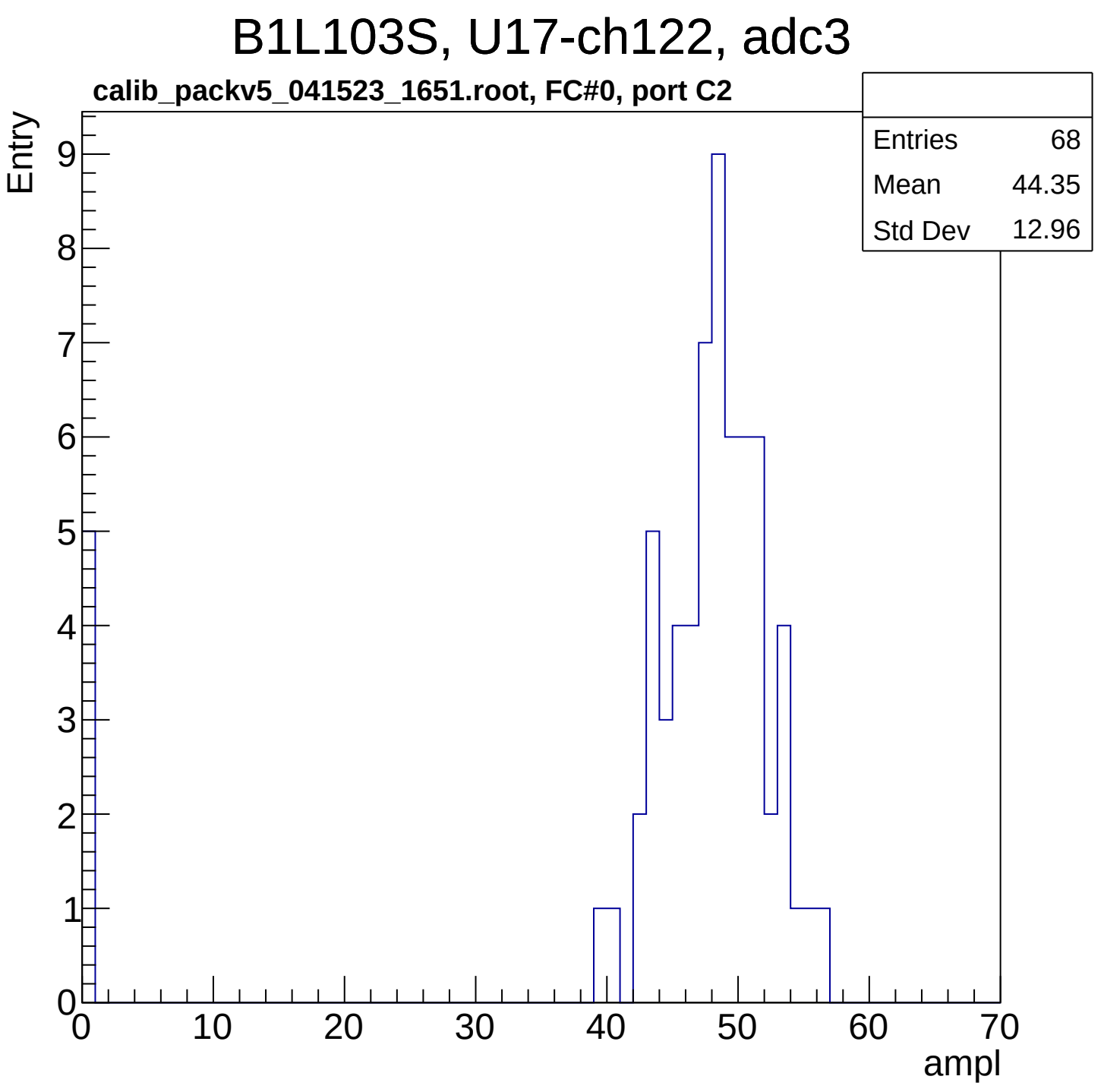

B1L103S, U17-ch121, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 60.25
Std Dev 2.817
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

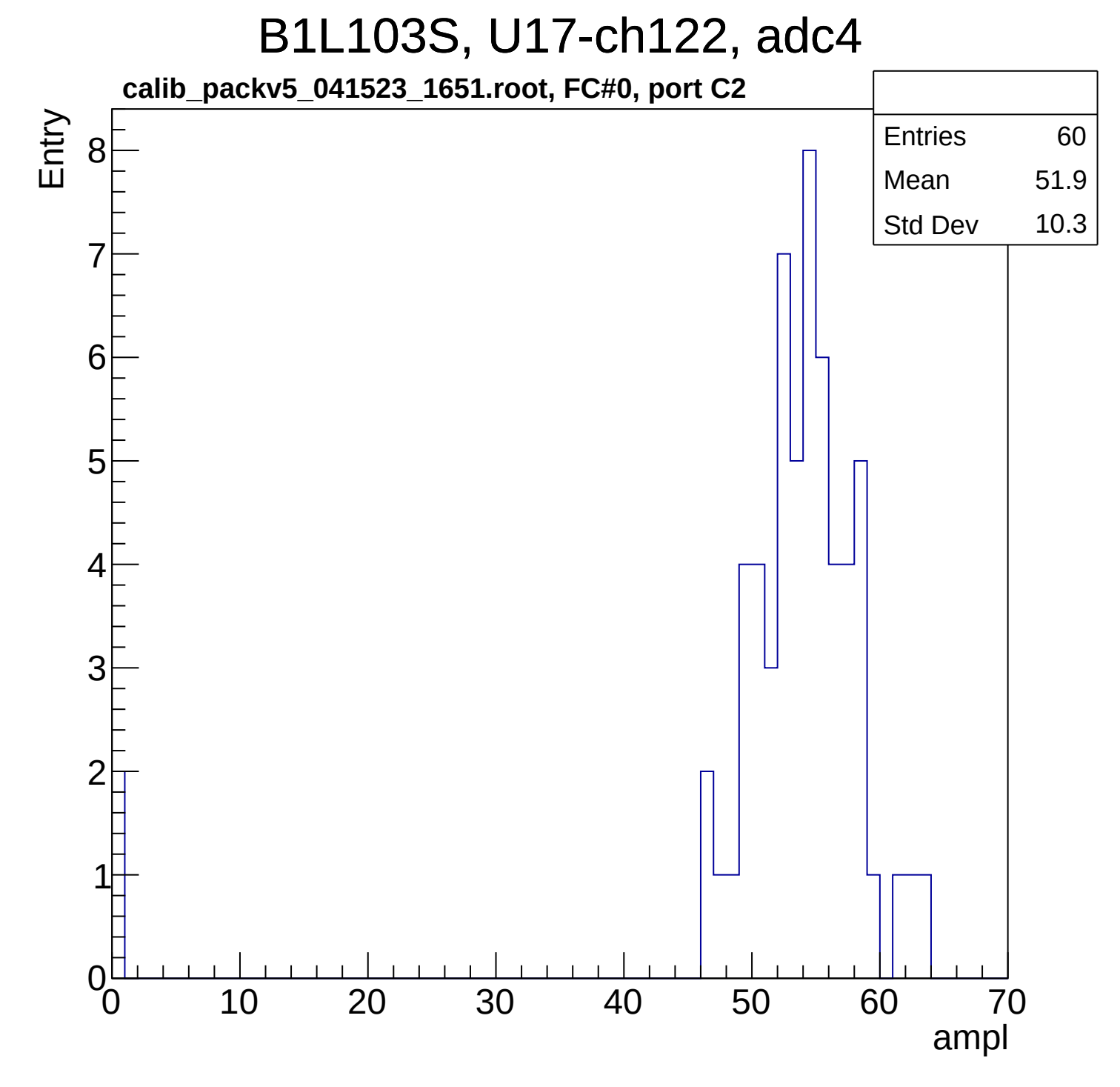

B1L103S, U17-ch121, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

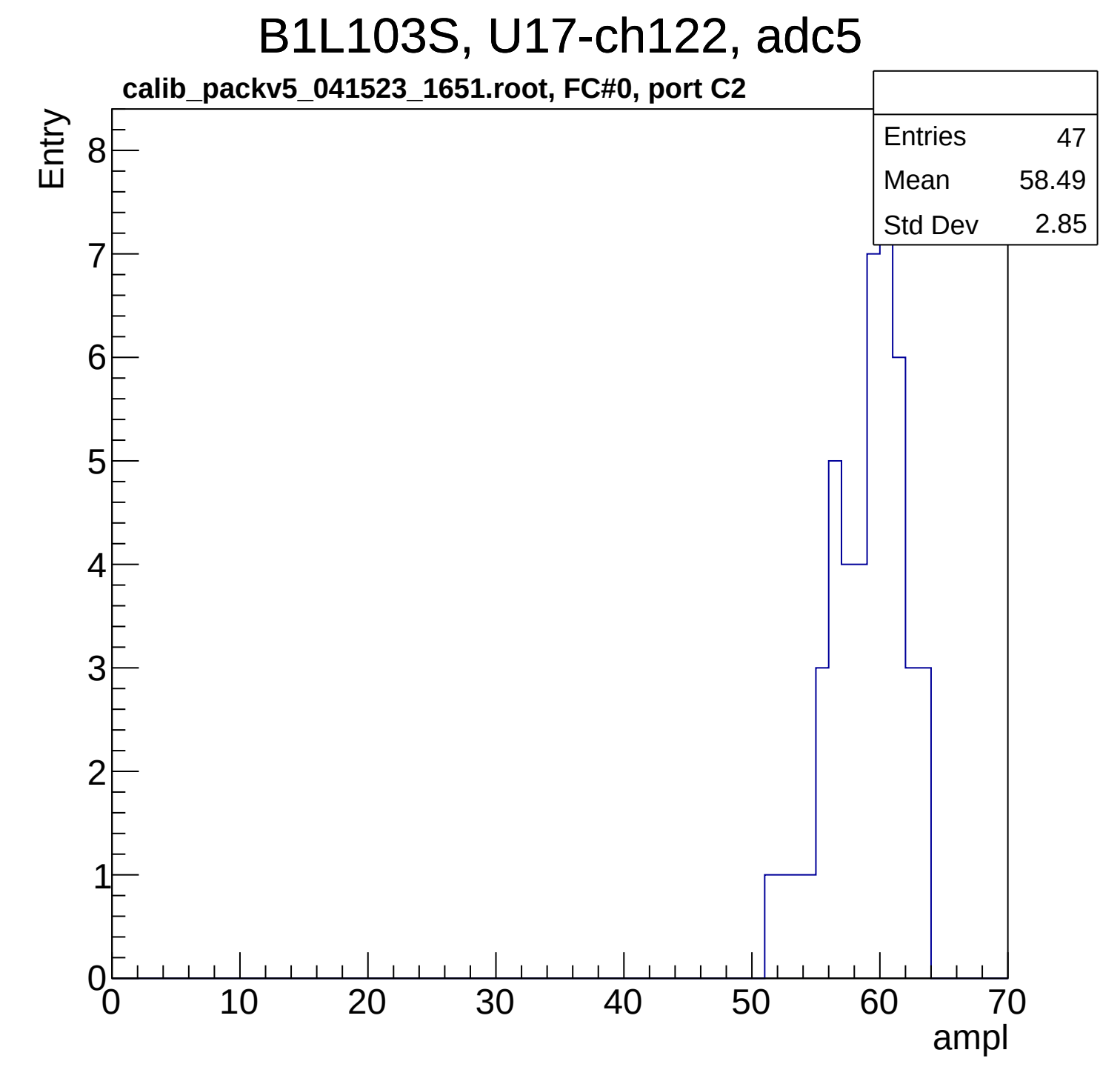

B1L103S, U17-ch122, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 24.29
Std Dev 7.004
Gaus mean : 26.3483
Gaus Width: 3.7061
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

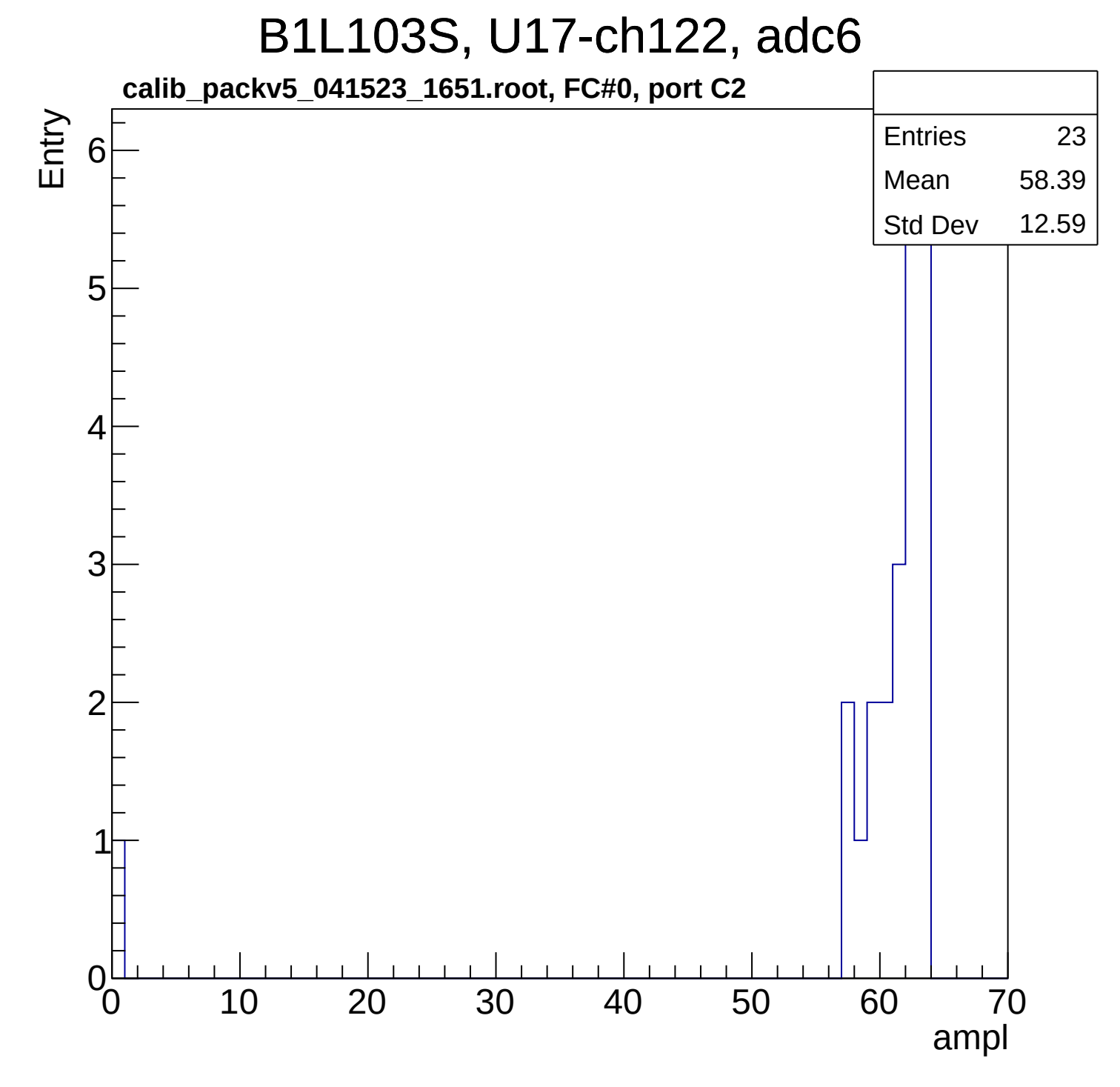

B1L103S, U17-ch122, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 32.16
Std Dev 8.104
Gaus mean : 33.5129
Gaus Width: 3.3742
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

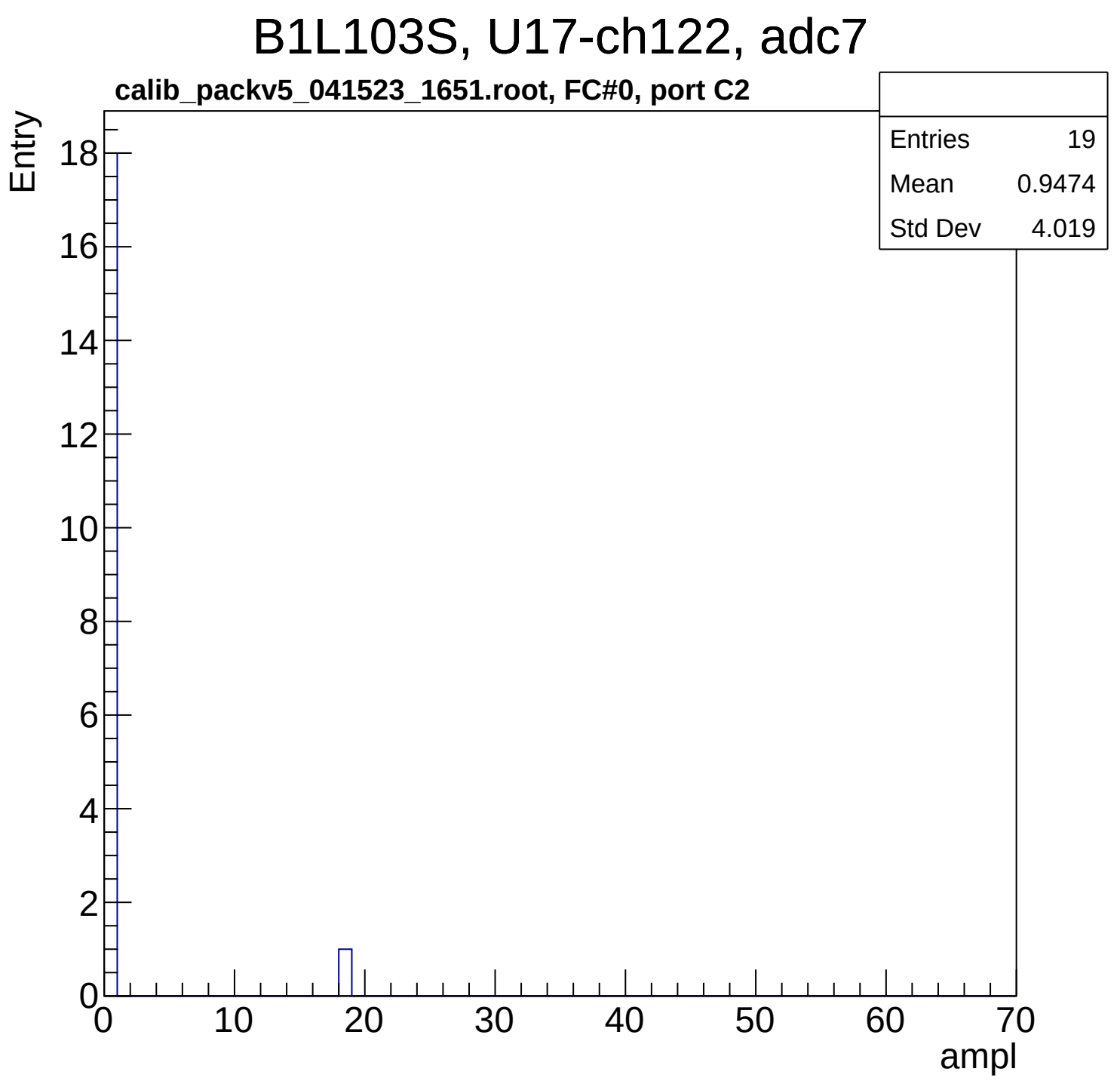

B1L103S, U17-ch122, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 38.04
Std Dev 10.64
Gaus mean : 41.7032
Gaus Width: 4.2933
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

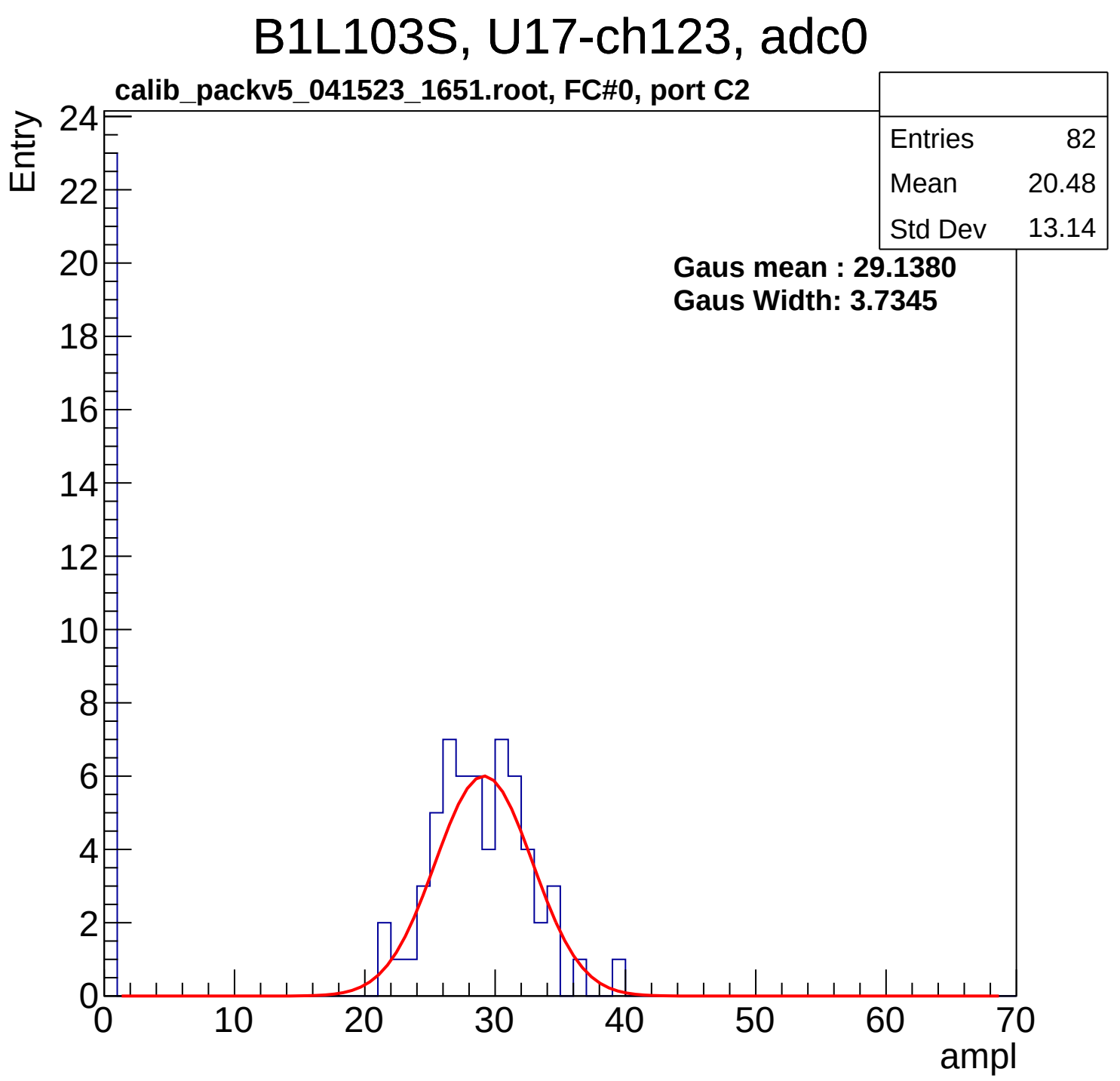

B1L103S, U17-ch122, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 44.35
Std Dev 12.96
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

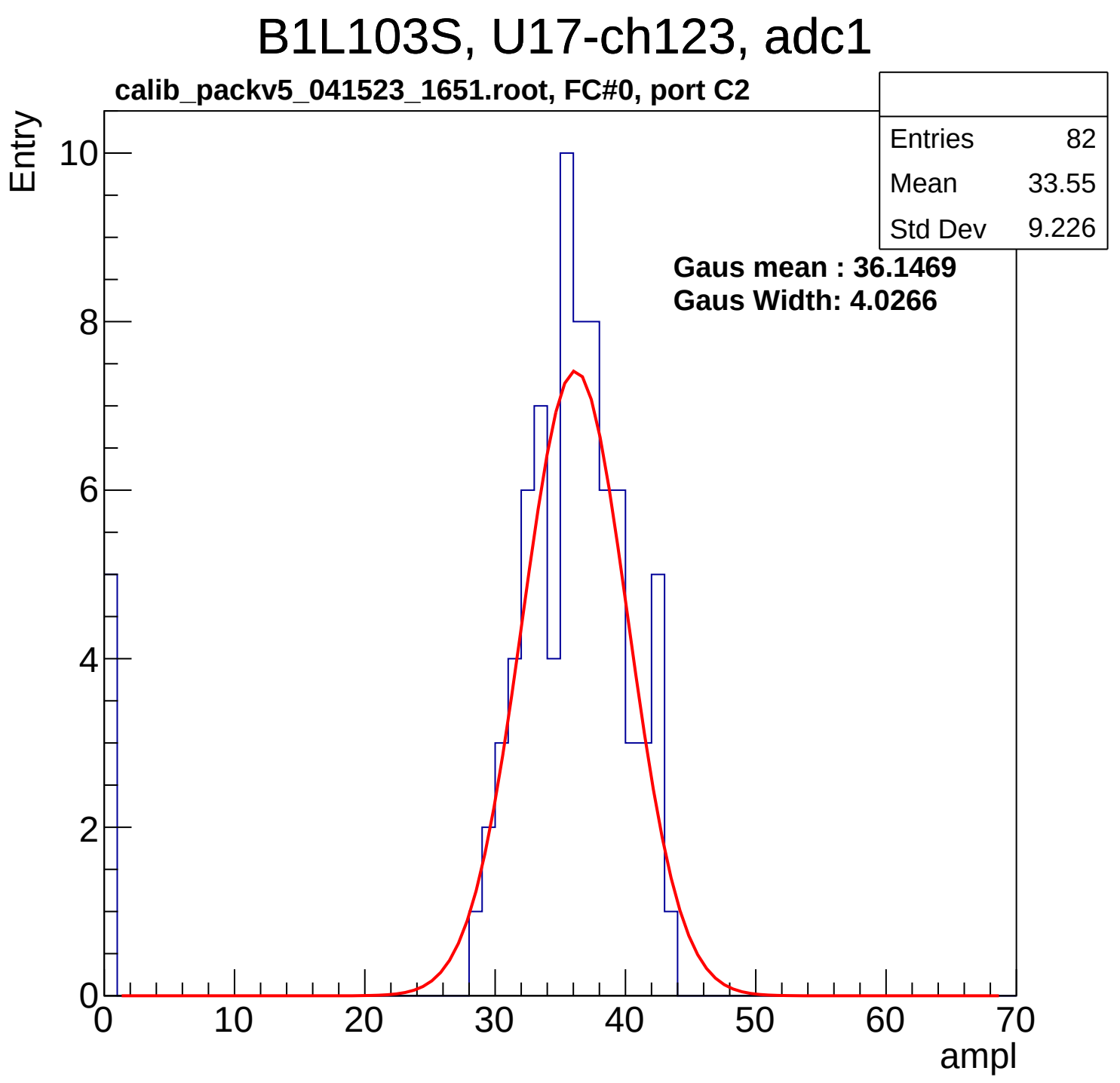

B1L103S, U17-ch122, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 51.9
Std Dev 10.3
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

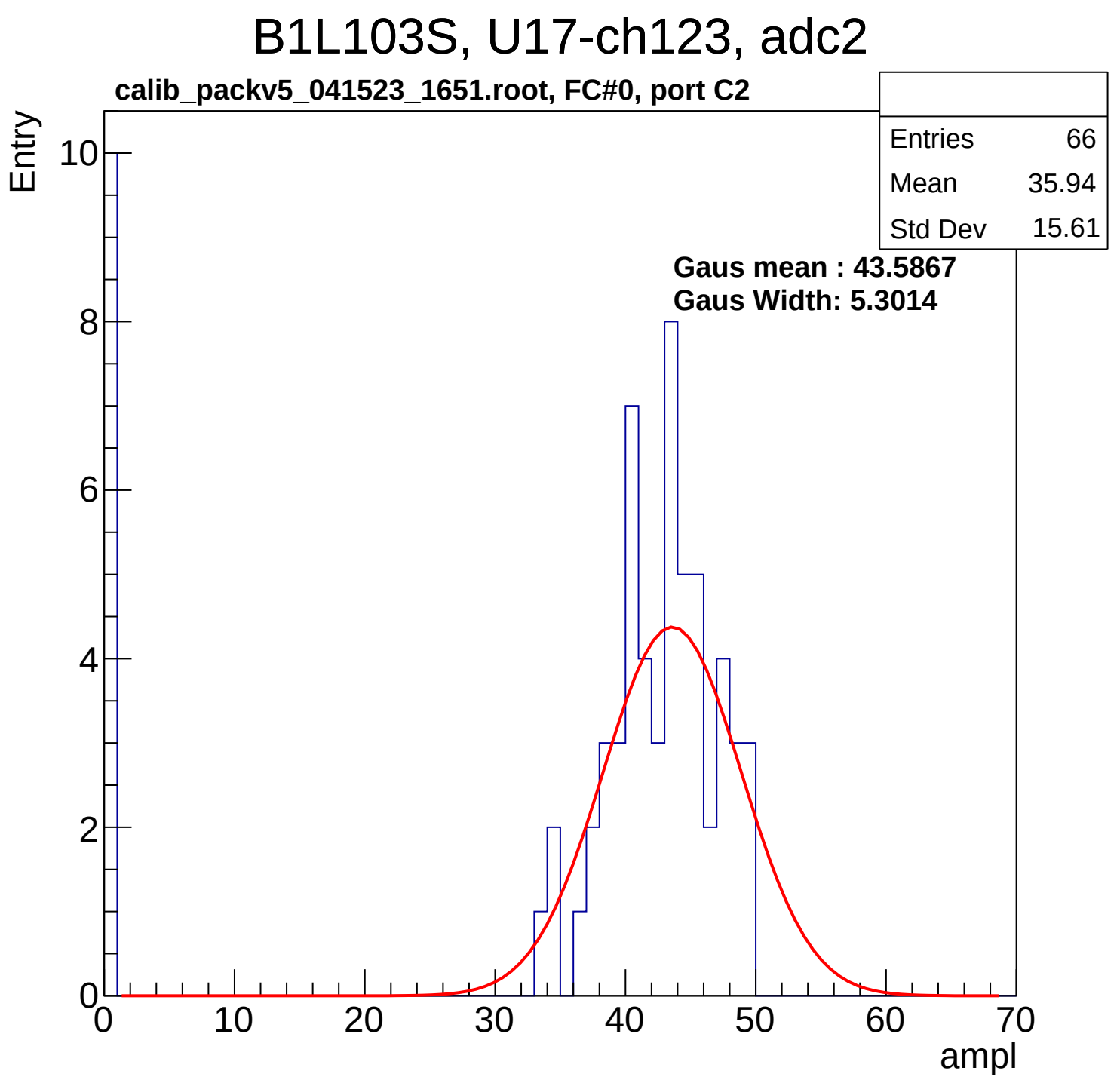

B1L103S, U17-ch122, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.49
Std Dev 2.85
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

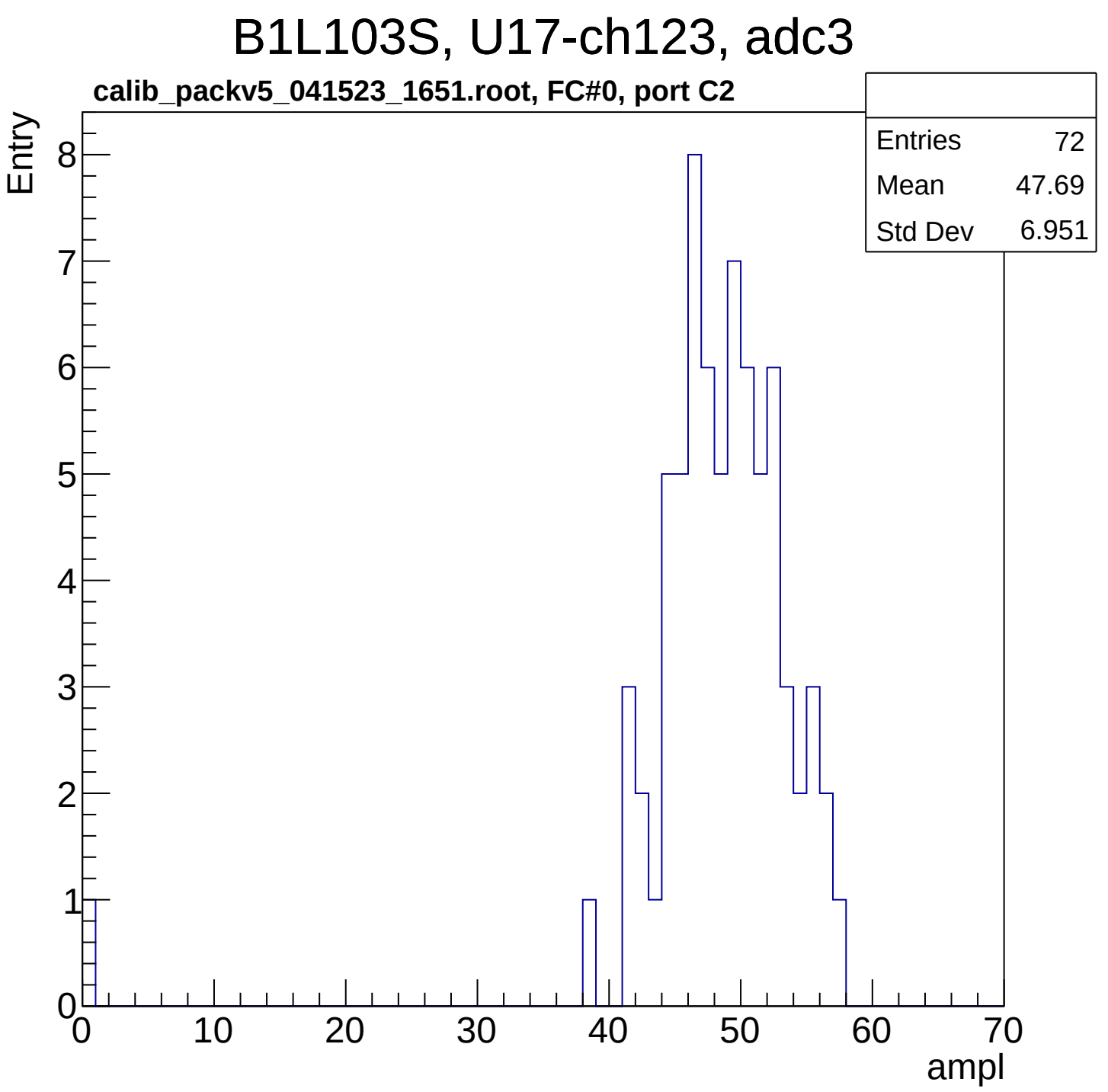

B1L103S, U17-ch122, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 58.39
Std Dev 12.59
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

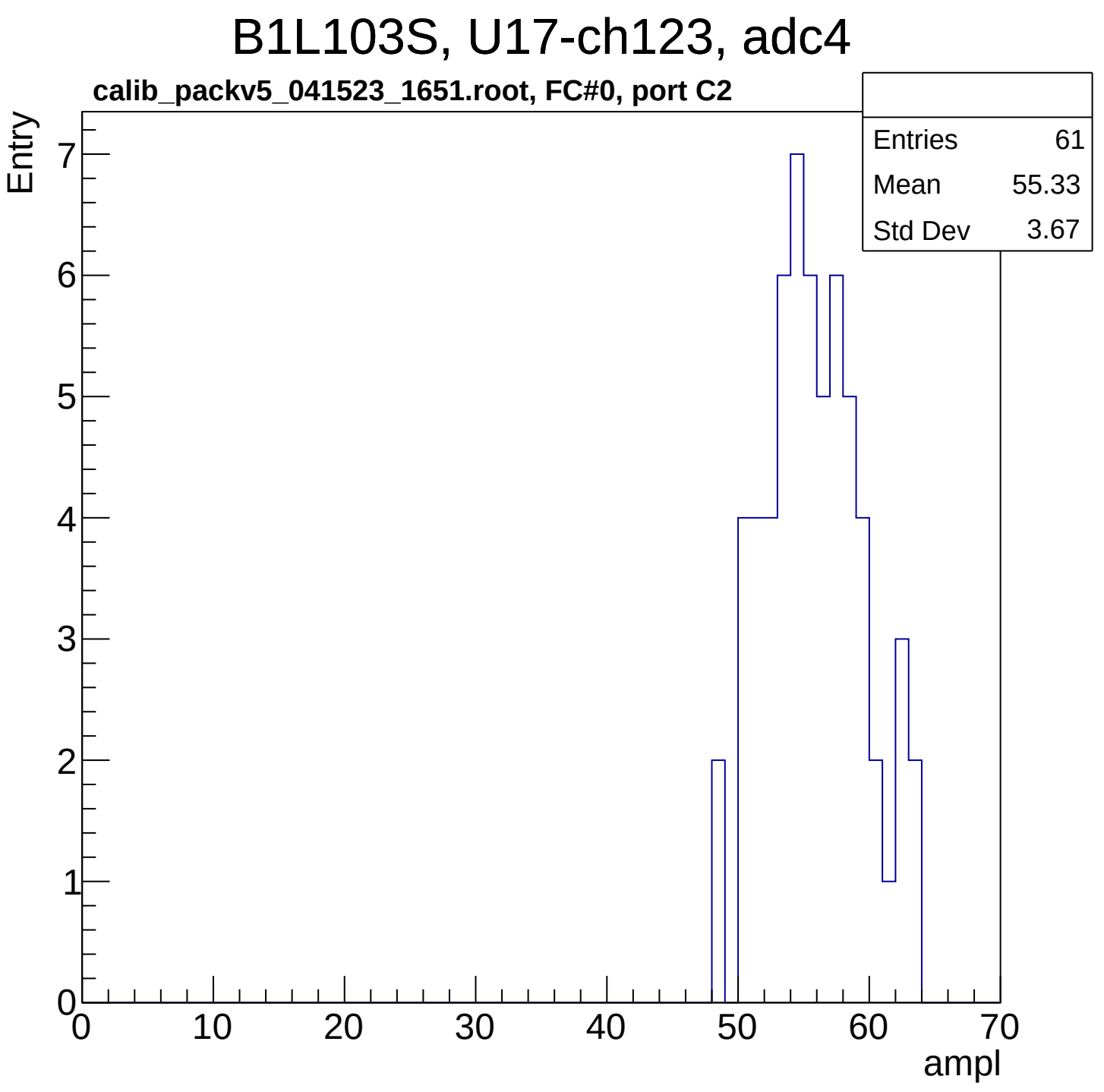

B1L103S, U17-ch122, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0.9474
Std Dev 4.019
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

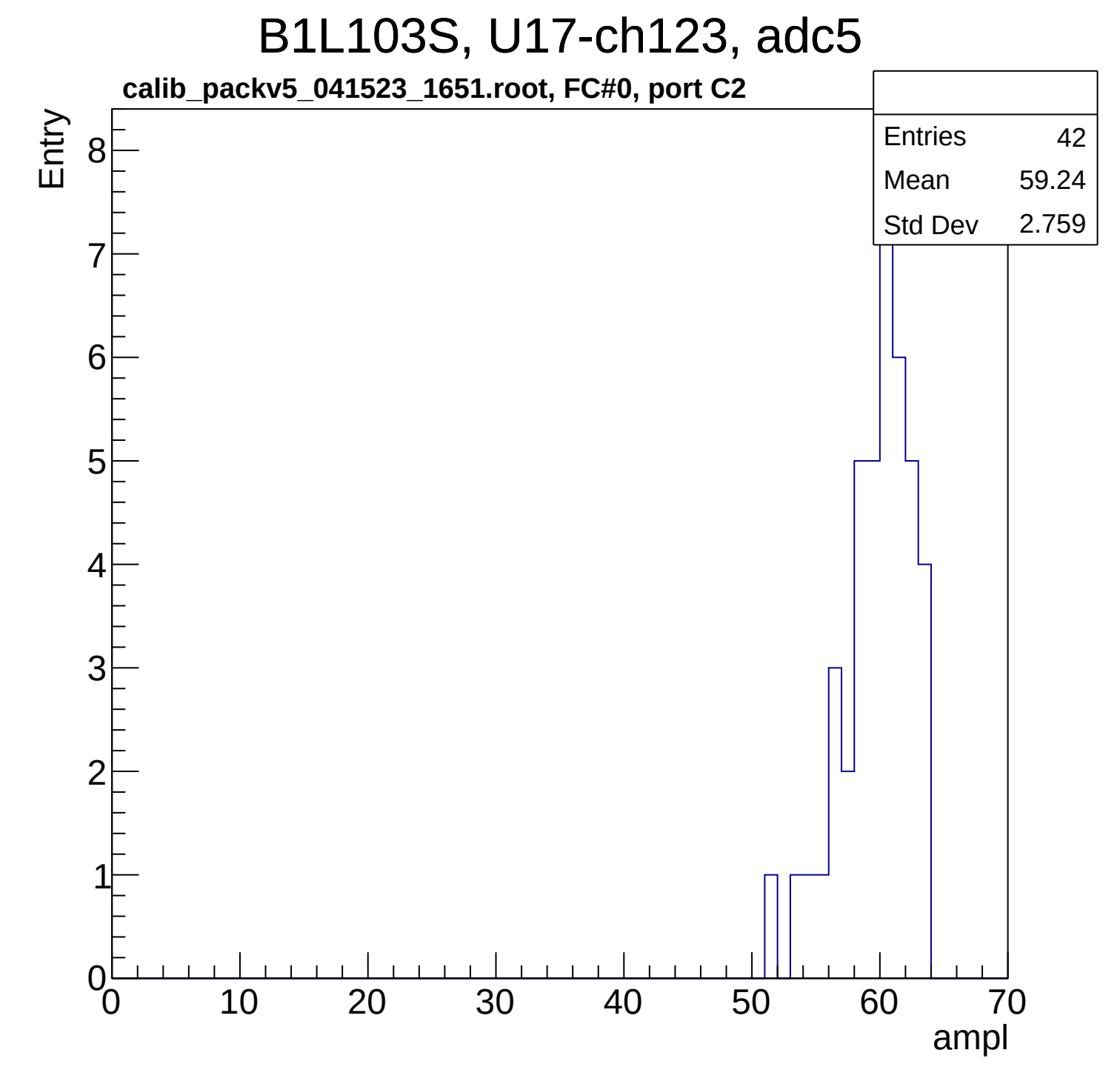

B1L103S, U17-ch123, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 20.48
Std Dev 13.14
Gaus mean : 29.1380
Gaus Width: 3.7345
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70

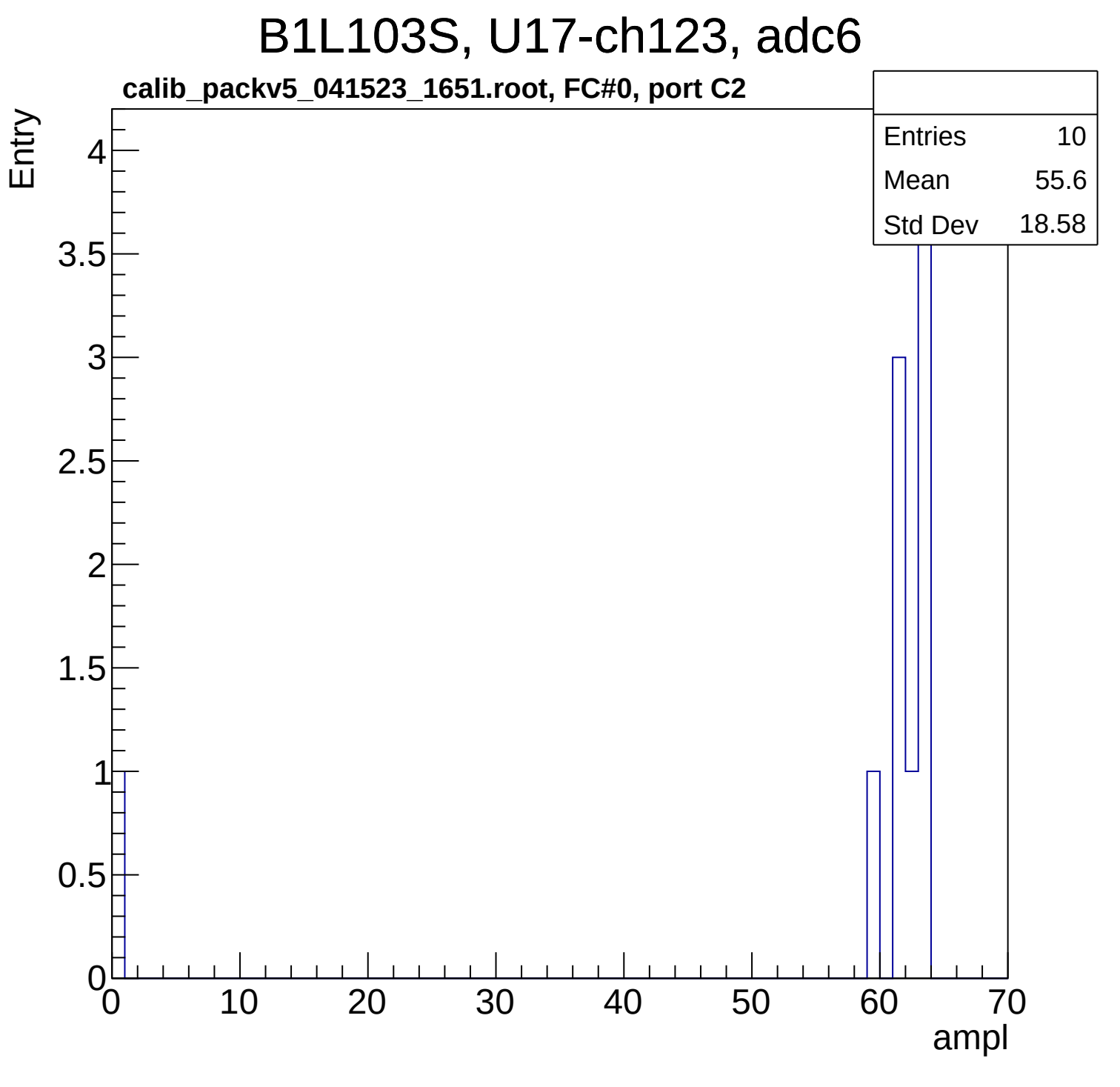

B1L103S, U17-ch123, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 33.55
Std Dev 9.226
Gaus mean : 36.1469
Gaus Width: 4.0266
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

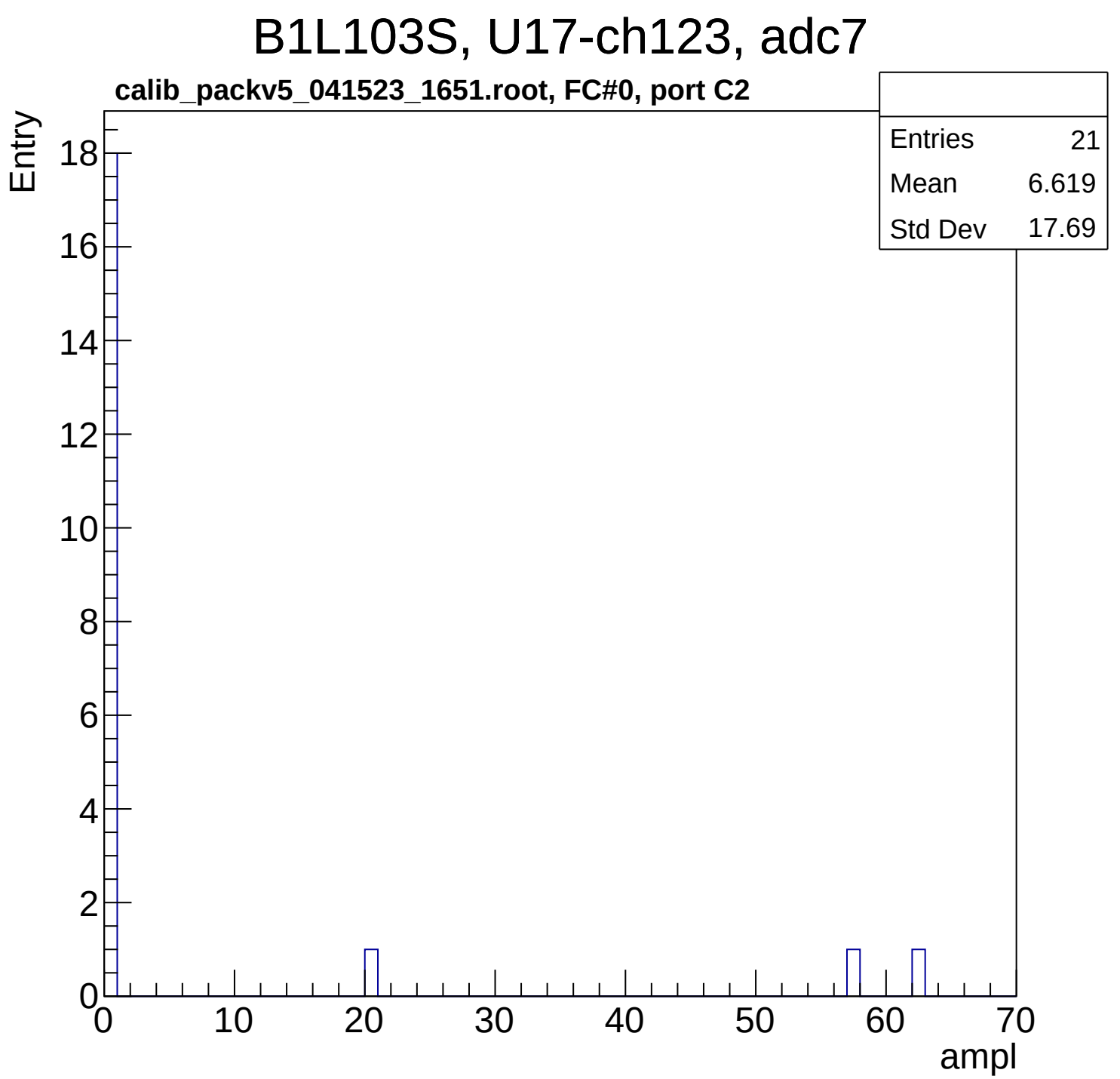

B1L103S, U17-ch123, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 35.94
Std Dev 15.61
Gaus mean : 43.5867
Gaus Width: 5.3014
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

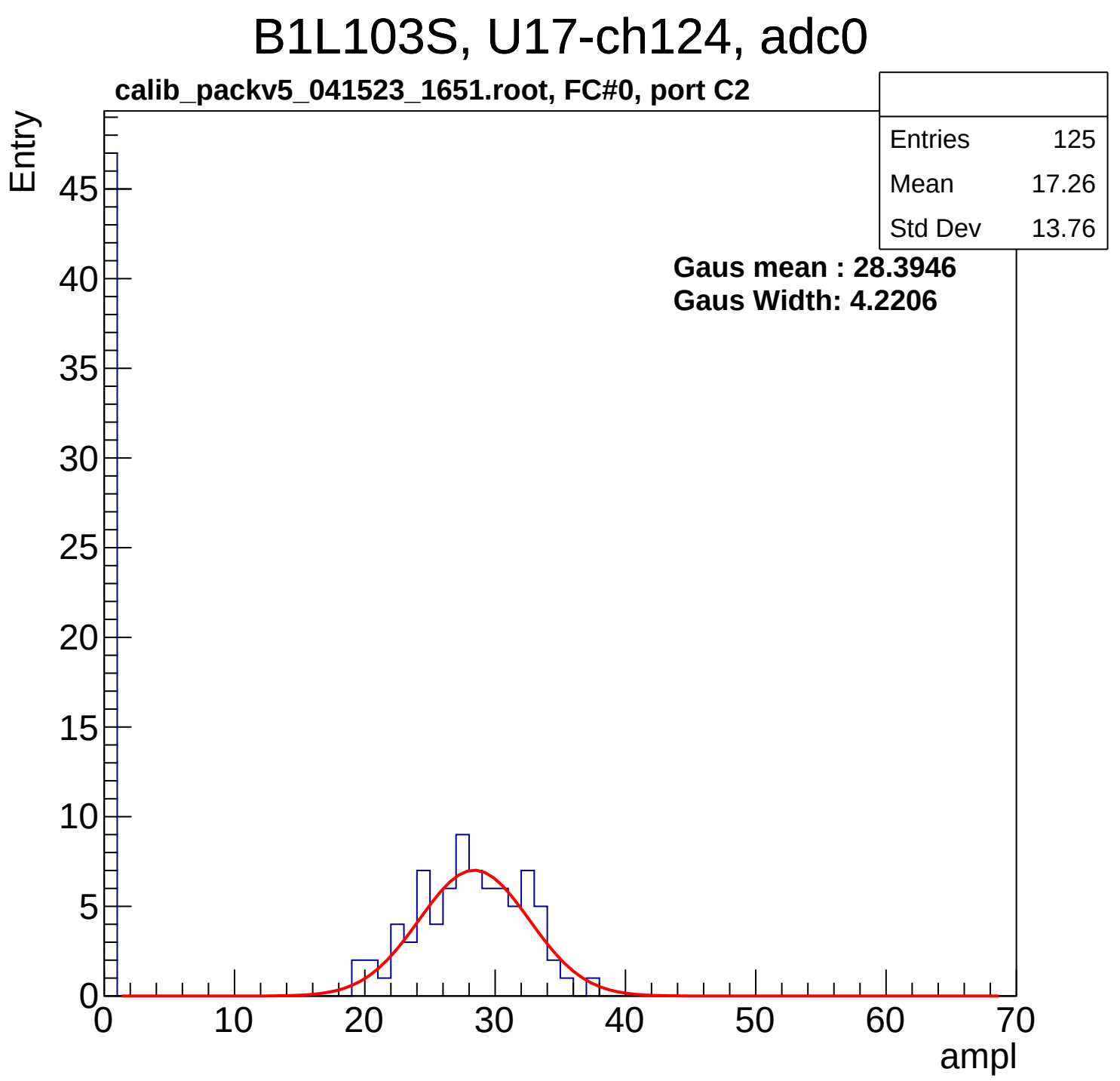

B1L103S, U17-ch123, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 47.69
Std Dev 6.951
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

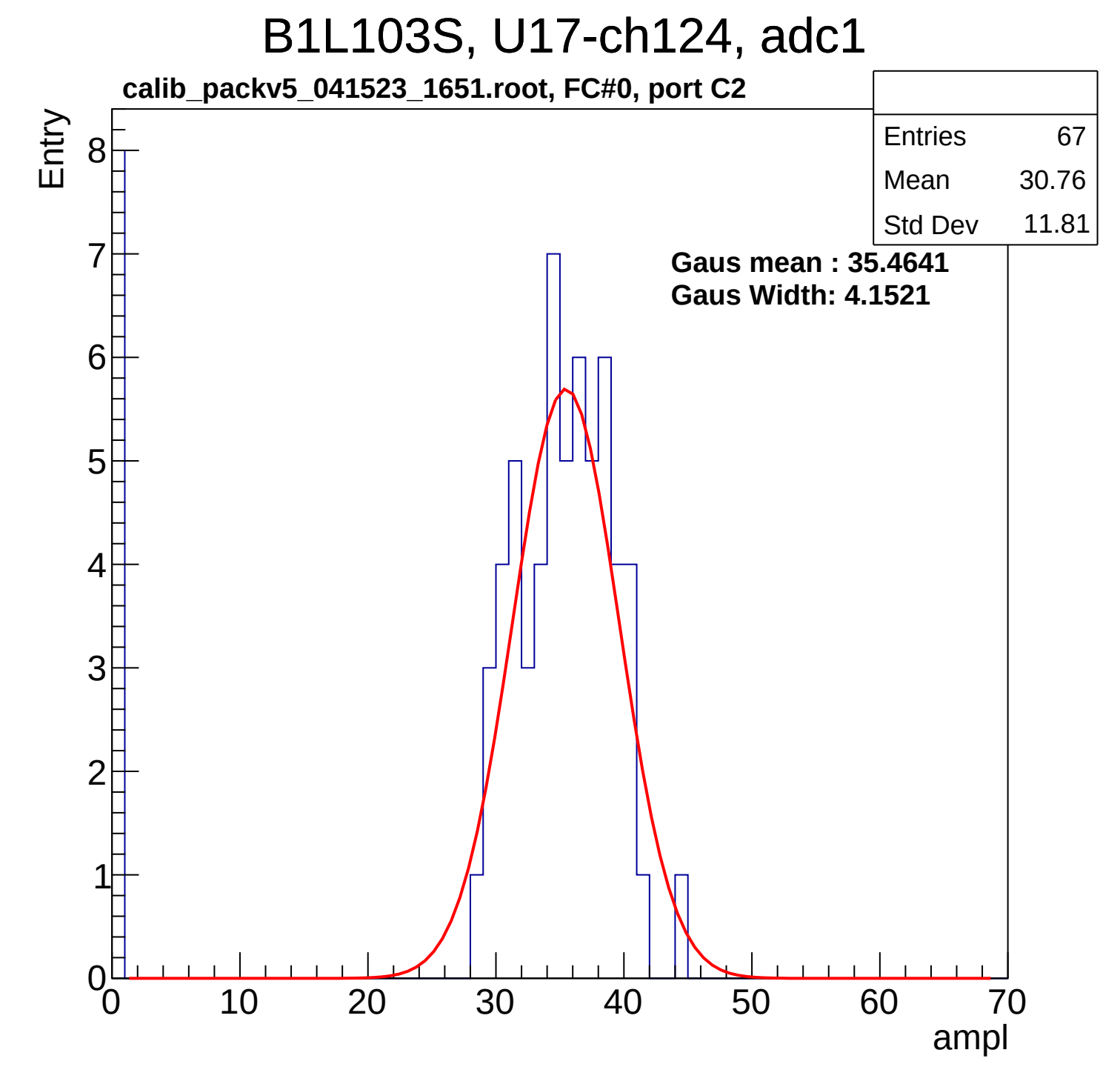

B1L103S, U17-ch123, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 55.33
Std Dev 3.67
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

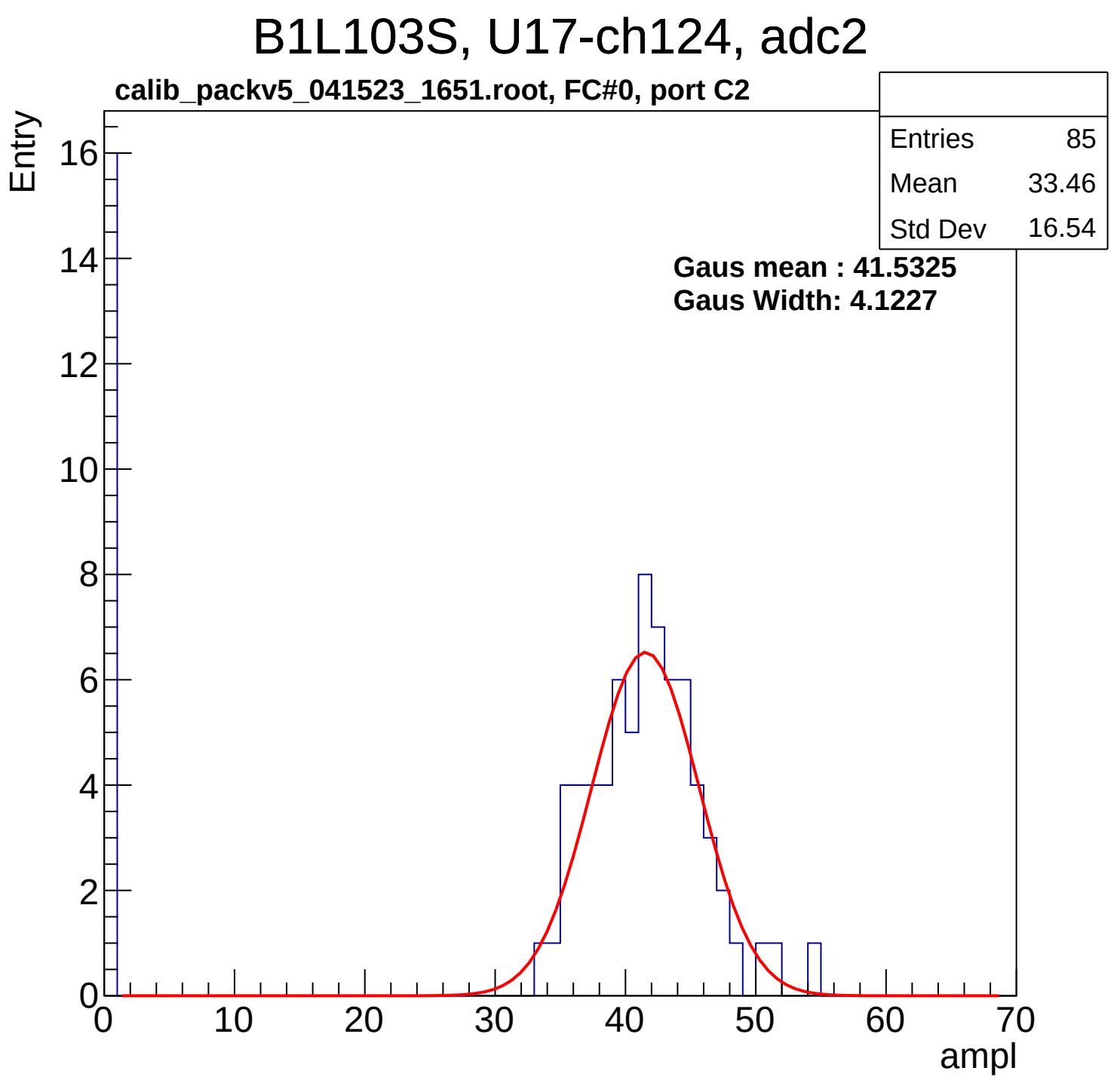

B1L103S, U17-ch123, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 59.24
Std Dev 2.759
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

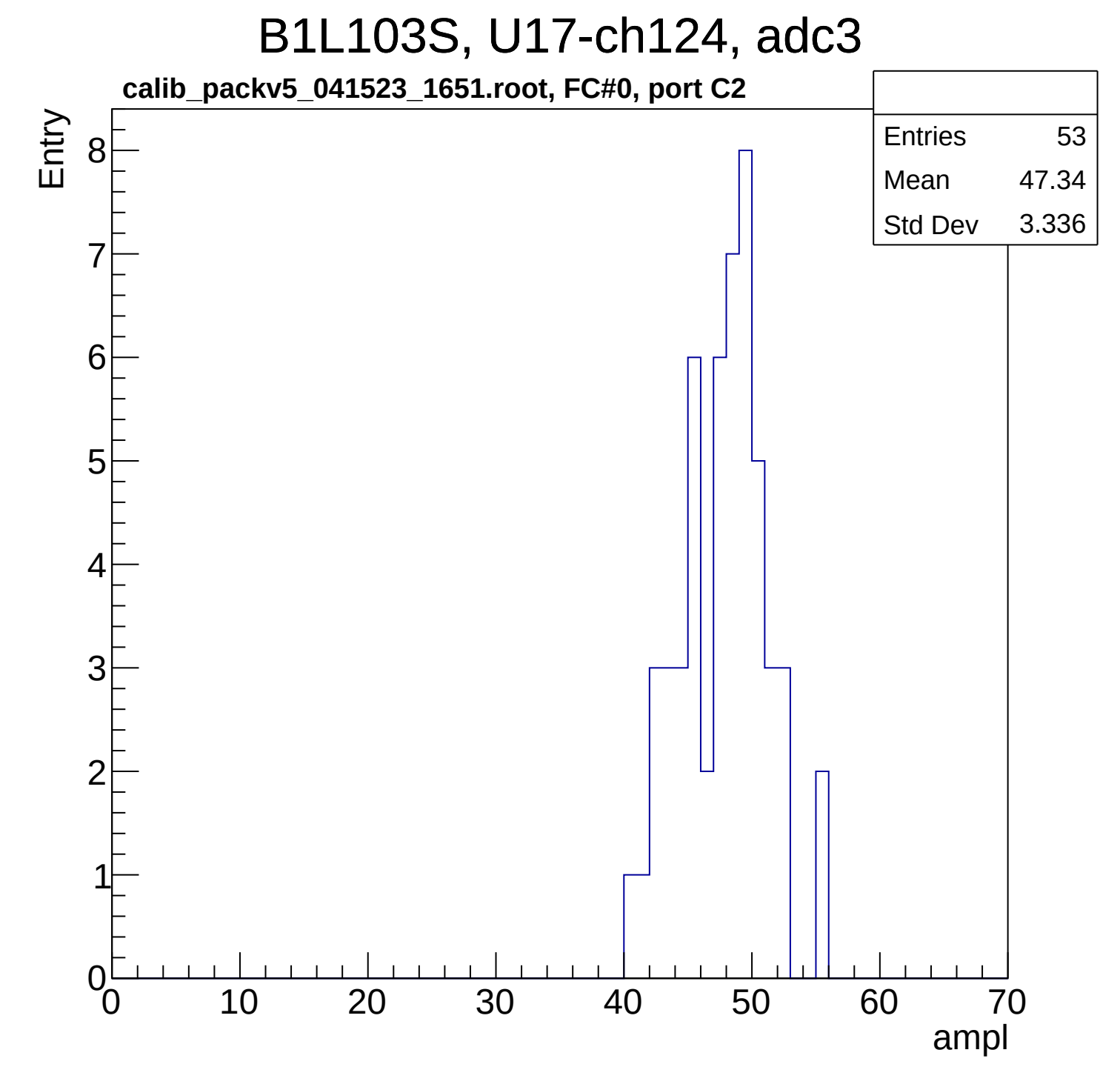

B1L103S, U17-ch123, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.6
Std Dev 18.58
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

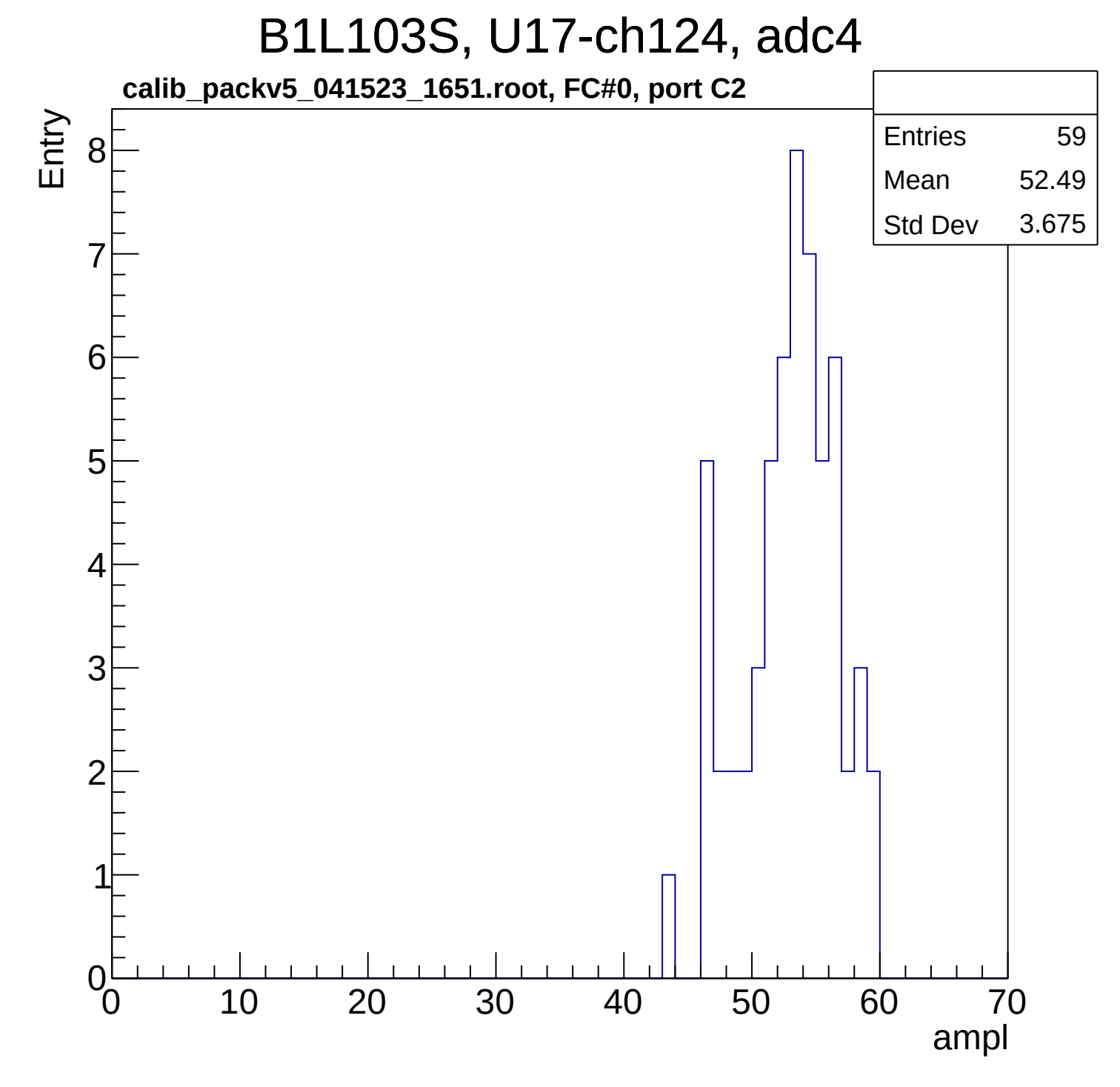

B1L103S, U17-ch123, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6.619
Std Dev 17.69
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

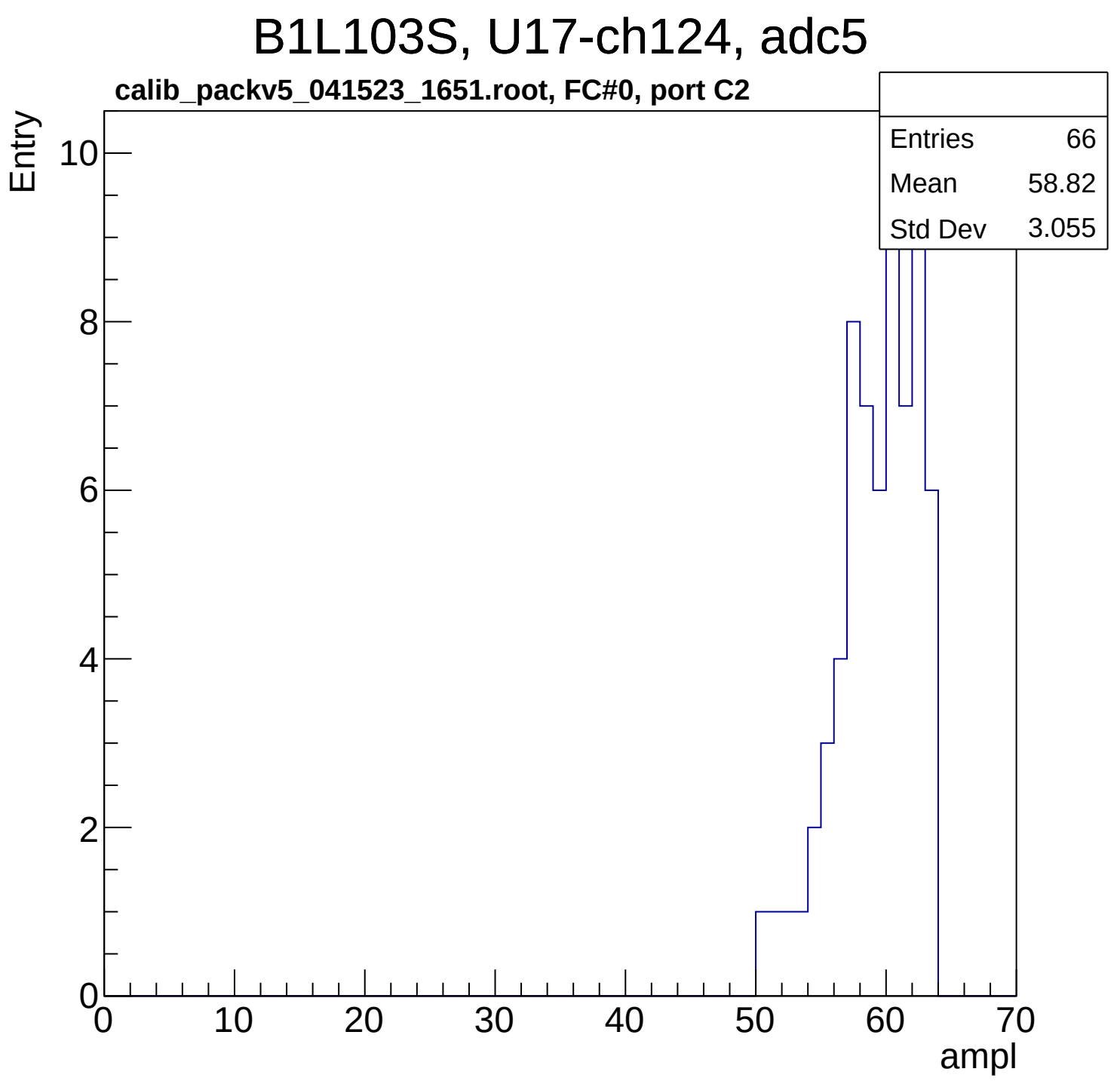

B1L103S, U17-ch124, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 125
Mean 17.26
Std Dev 13.76
Gaus mean : 28.3946
Gaus Width: 4.2206
Entry
ampl
0
5
10
15
20
25
30
35
40
45
0
10
20
30
40
50
60
70

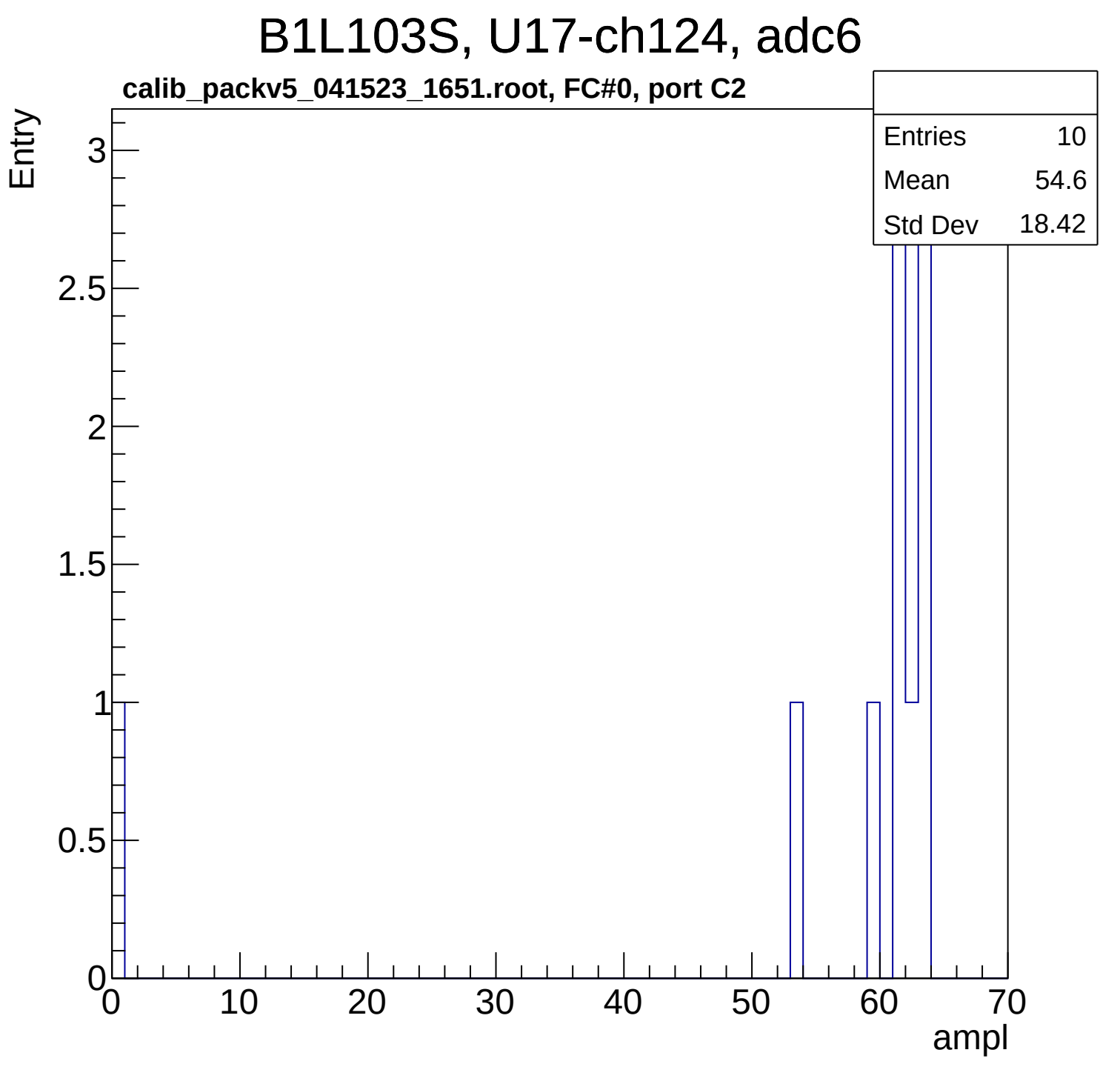

B1L103S, U17-ch124, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 30.76
Std Dev 11.81
Gaus mean : 35.4641
Gaus Width: 4.1521
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

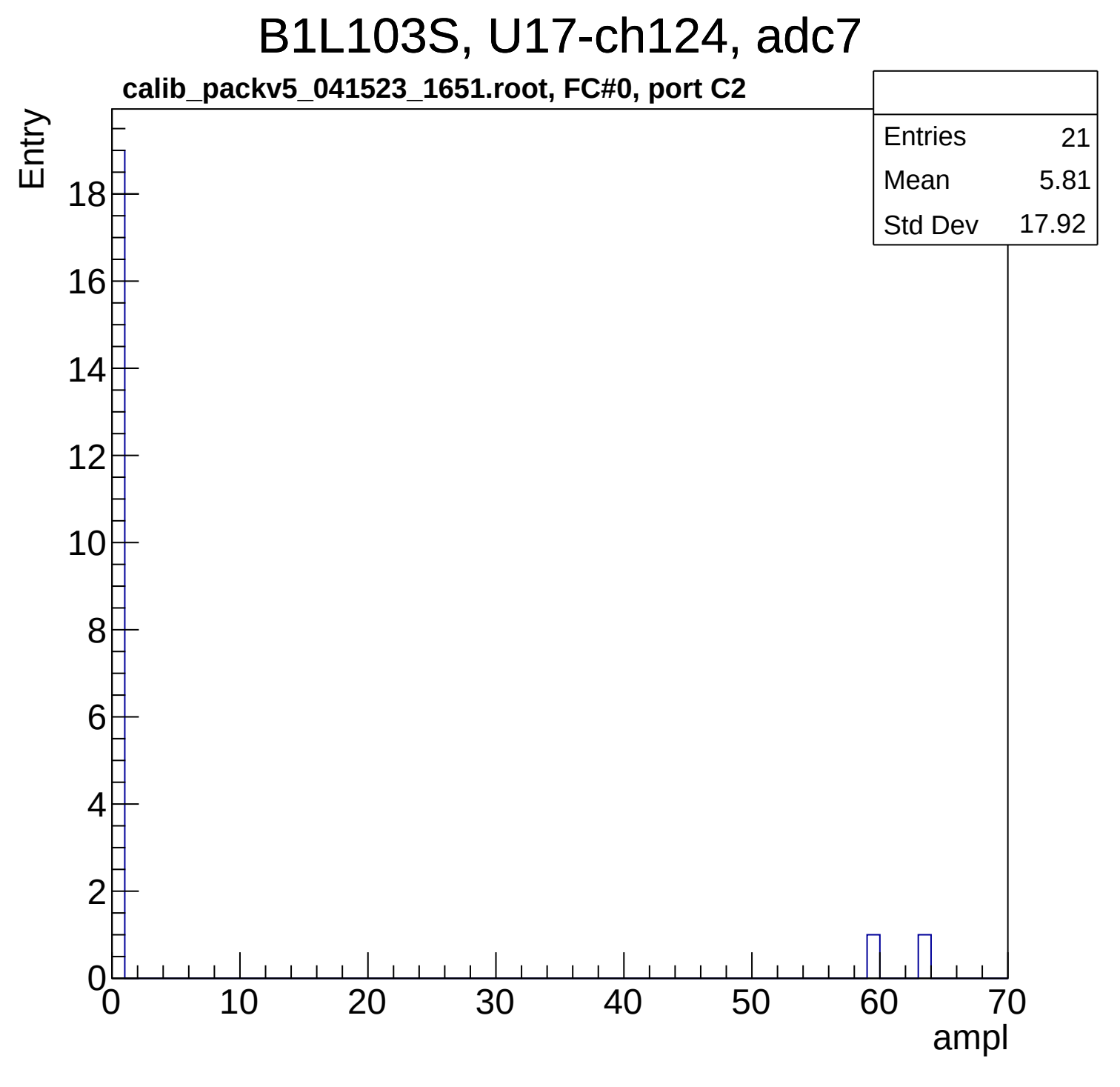

B1L103S, U17-ch124, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 33.46
Std Dev 16.54
Gaus mean : 41.5325
Gaus Width: 4.1227
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

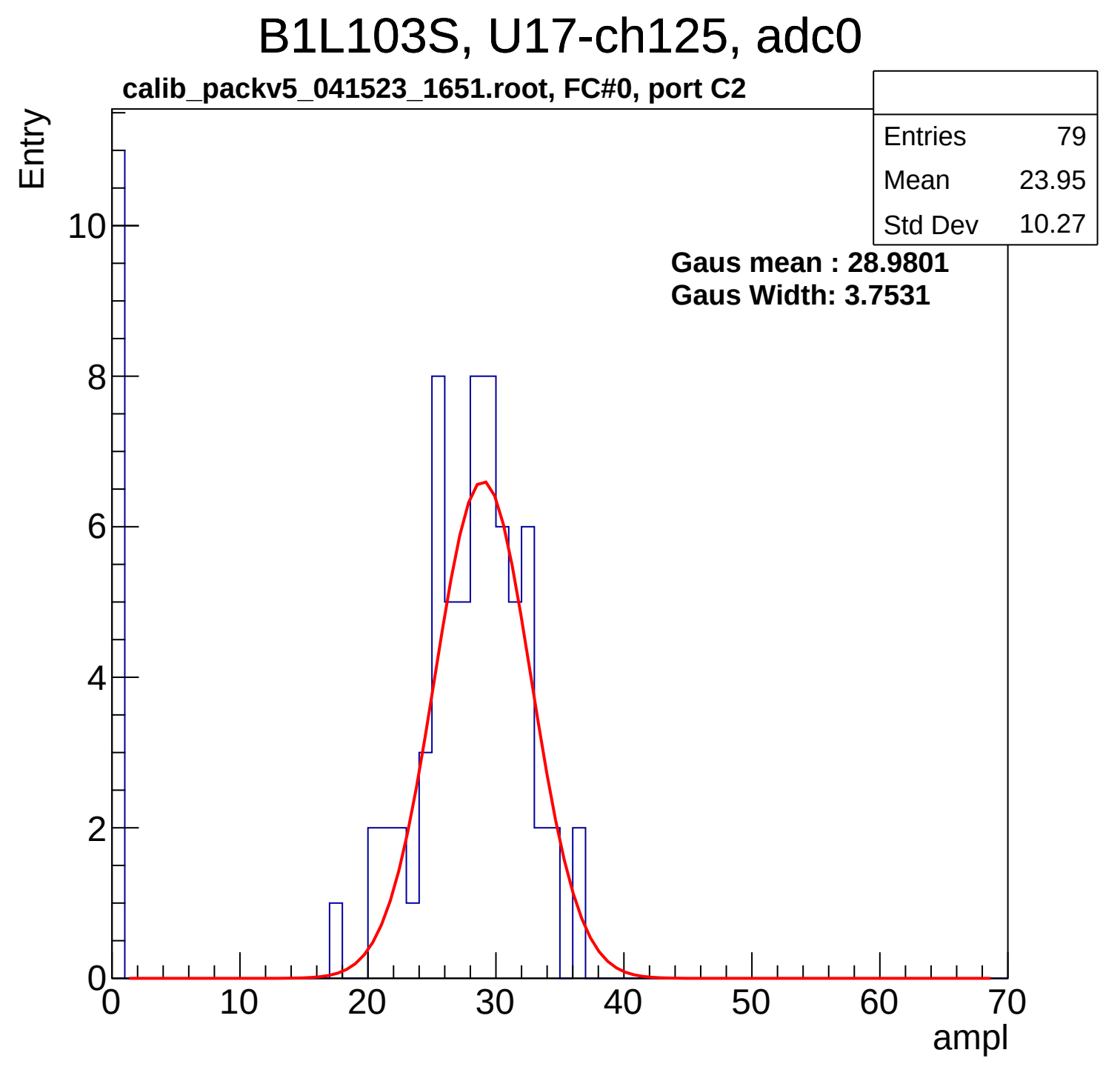

B1L103S, U17-ch124, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 47.34
Std Dev 3.336
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

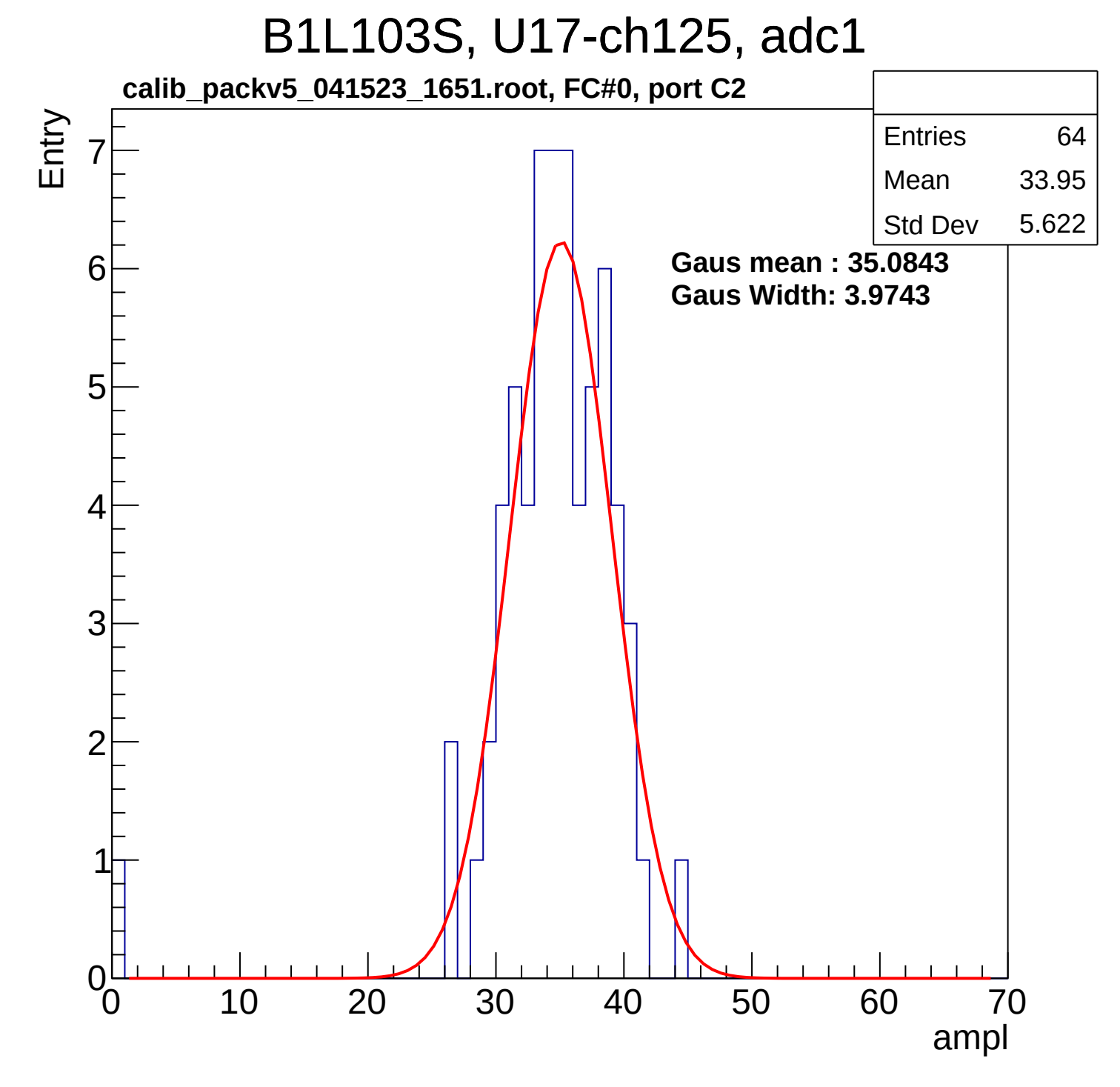

B1L103S, U17-ch124, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 52.49
Std Dev 3.675
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

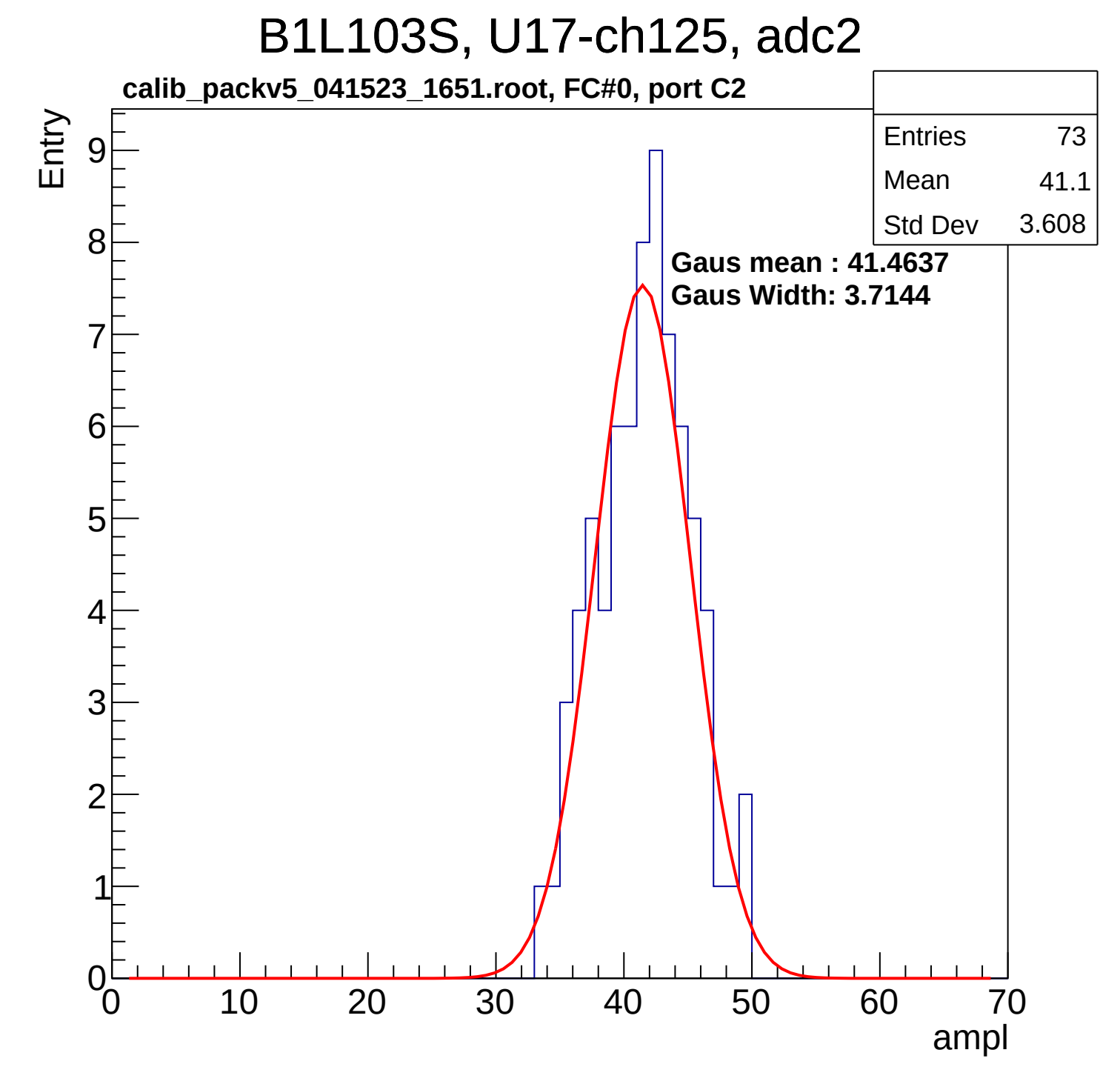

B1L103S, U17-ch124, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 58.82
Std Dev 3.055
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

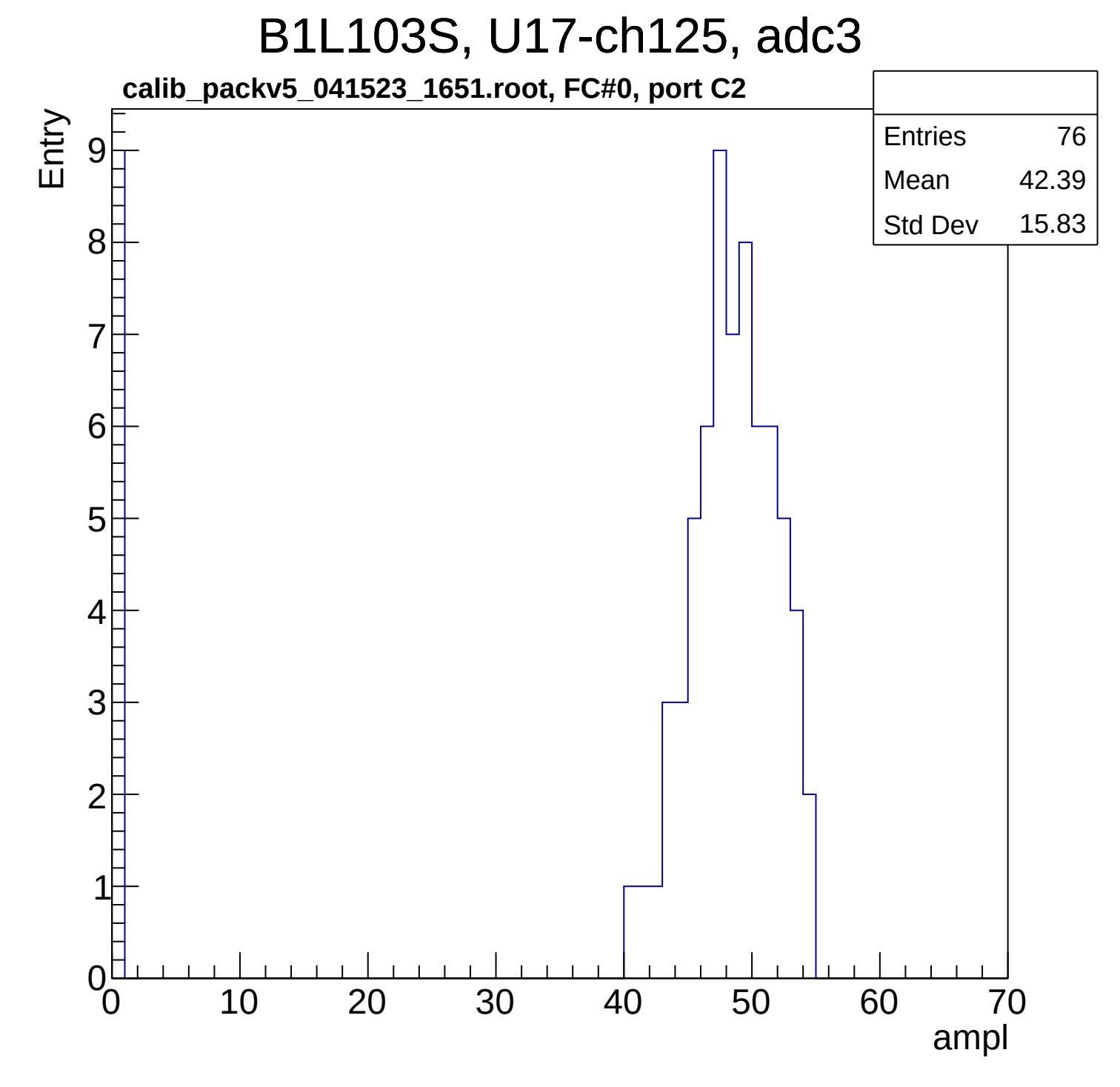

B1L103S, U17-ch124, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 54.6
Std Dev 18.42
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

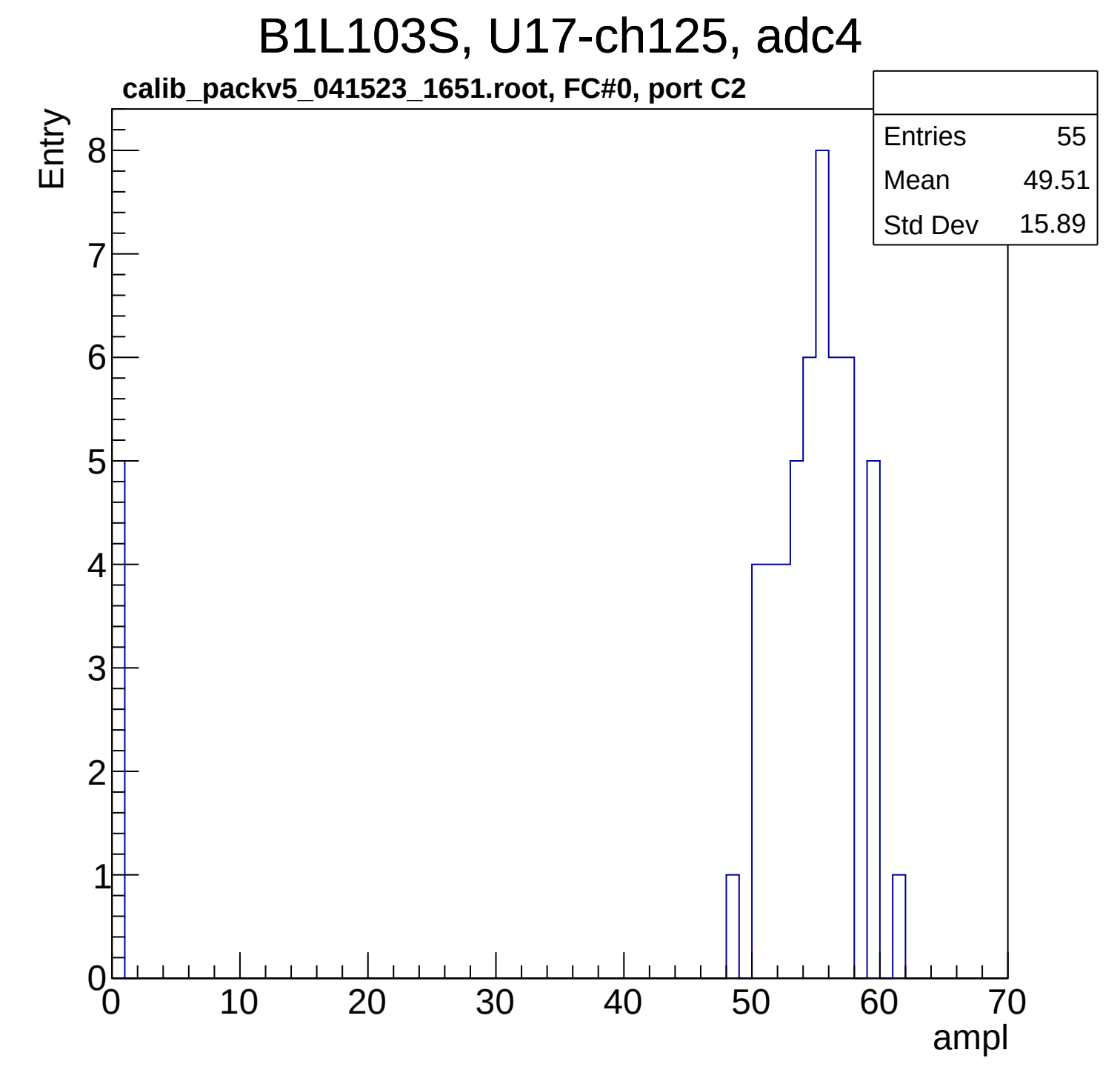

B1L103S, U17-ch124, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.81
Std Dev 17.92
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

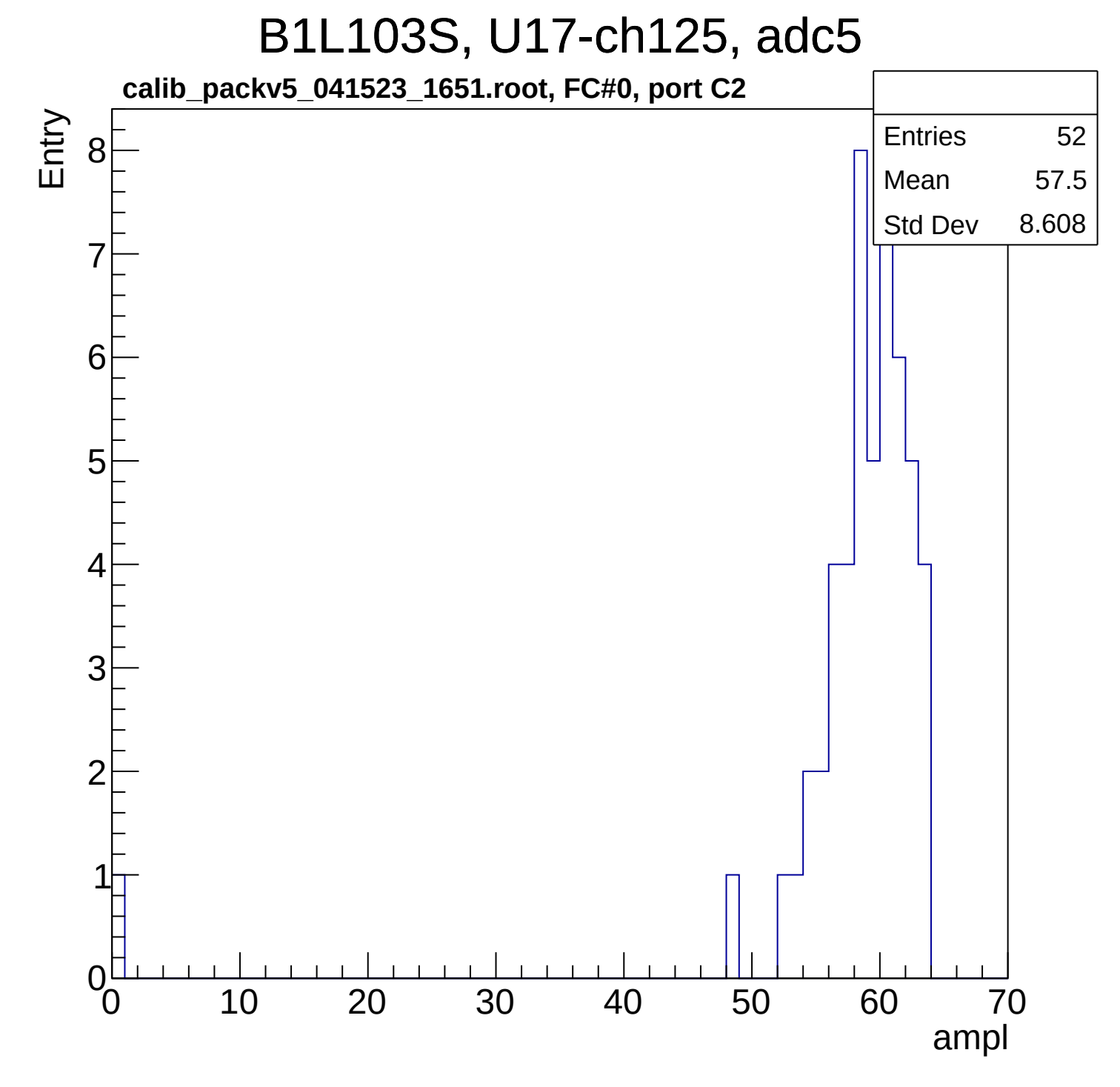

B1L103S, U17-ch125, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 23.95
Std Dev 10.27
Gaus mean : 28.9801
Gaus Width: 3.7531
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

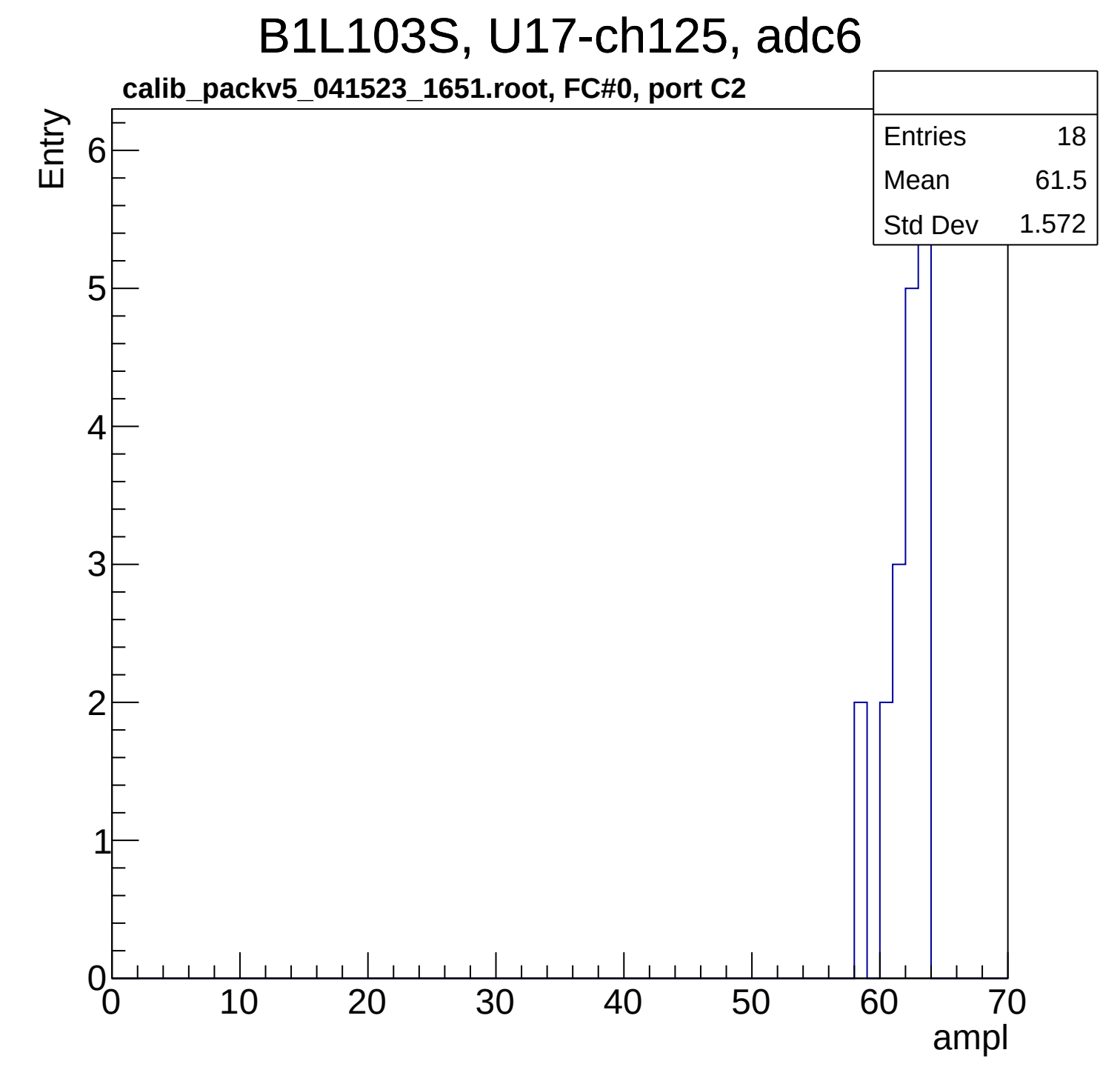

B1L103S, U17-ch125, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 33.95
Std Dev 5.622
Gaus mean : 35.0843
Gaus Width: 3.9743
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

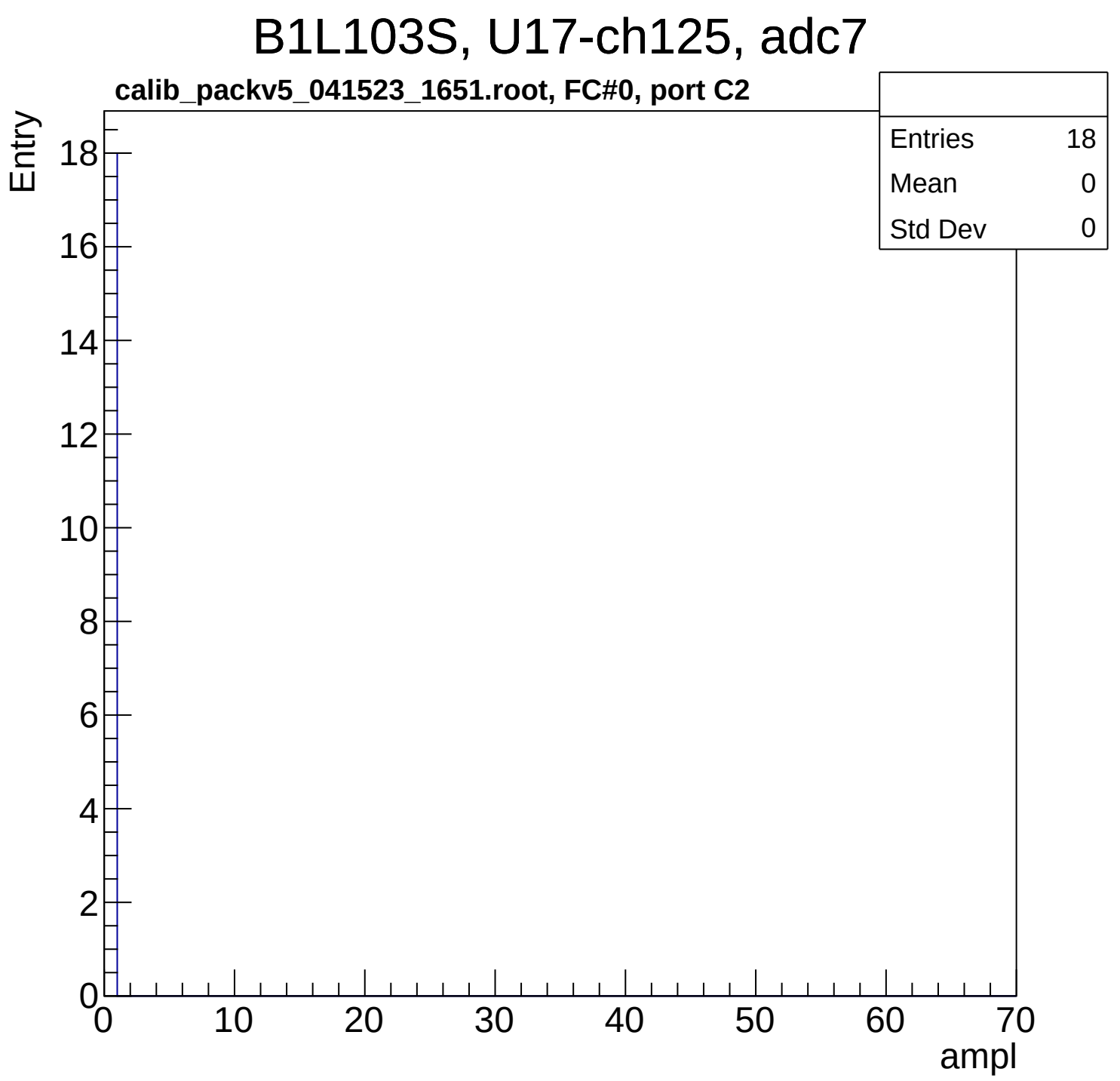

B1L103S, U17-ch125, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 41.1
Std Dev 3.608
Gaus mean : 41.4637
Gaus Width: 3.7144
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

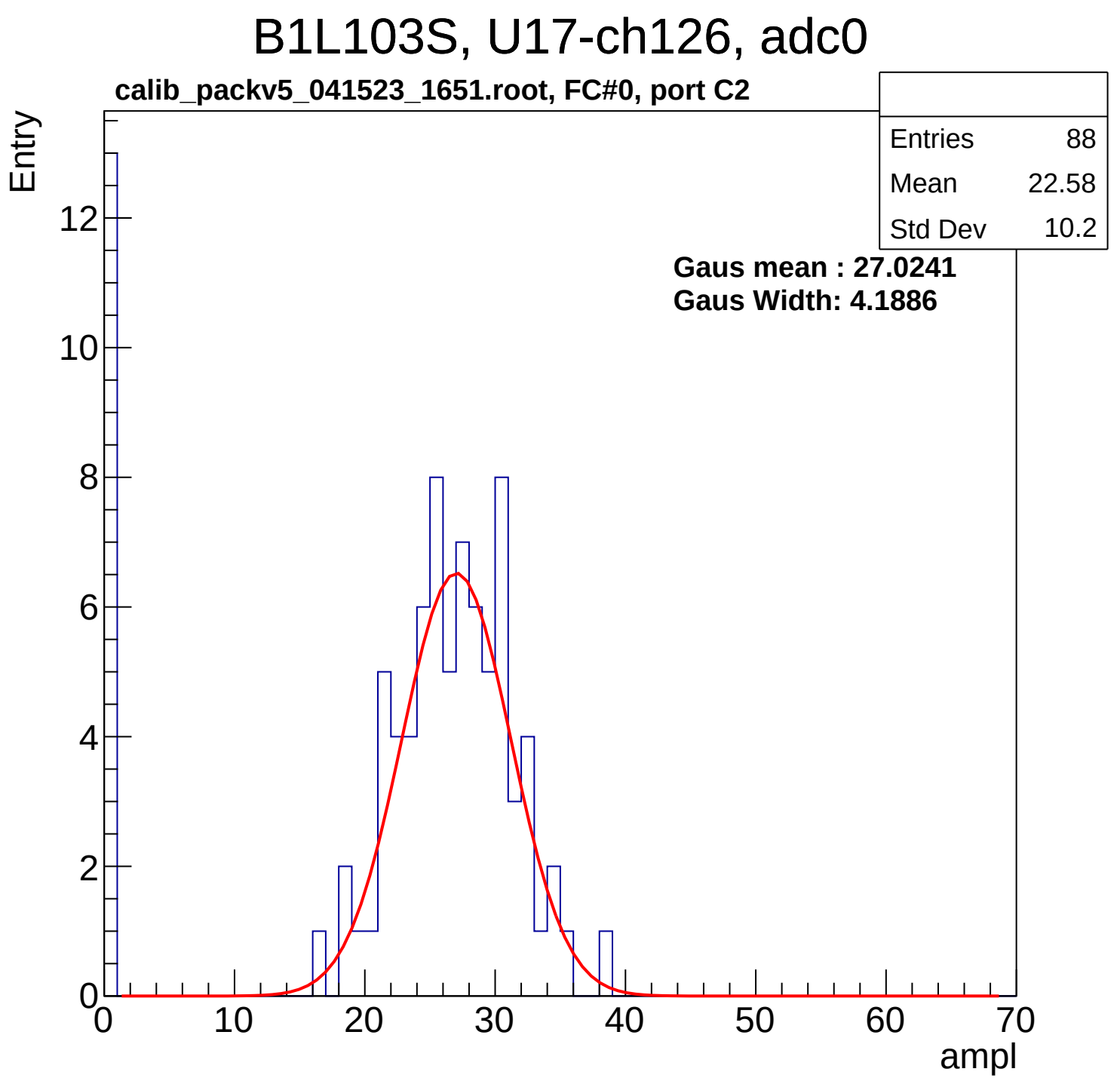

B1L103S, U17-ch125, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 42.39
Std Dev 15.83
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

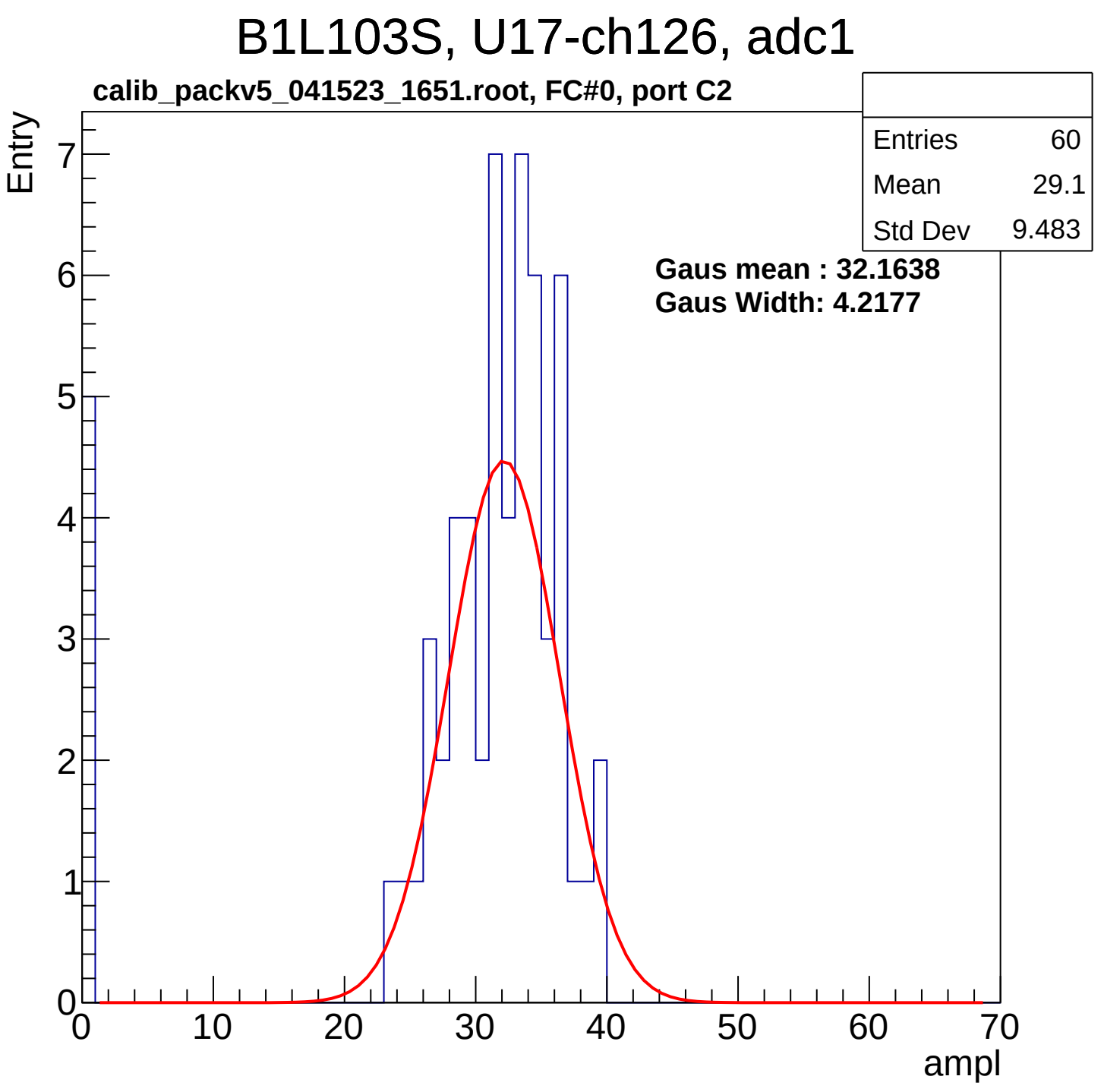

B1L103S, U17-ch125, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 49.51
Std Dev 15.89
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

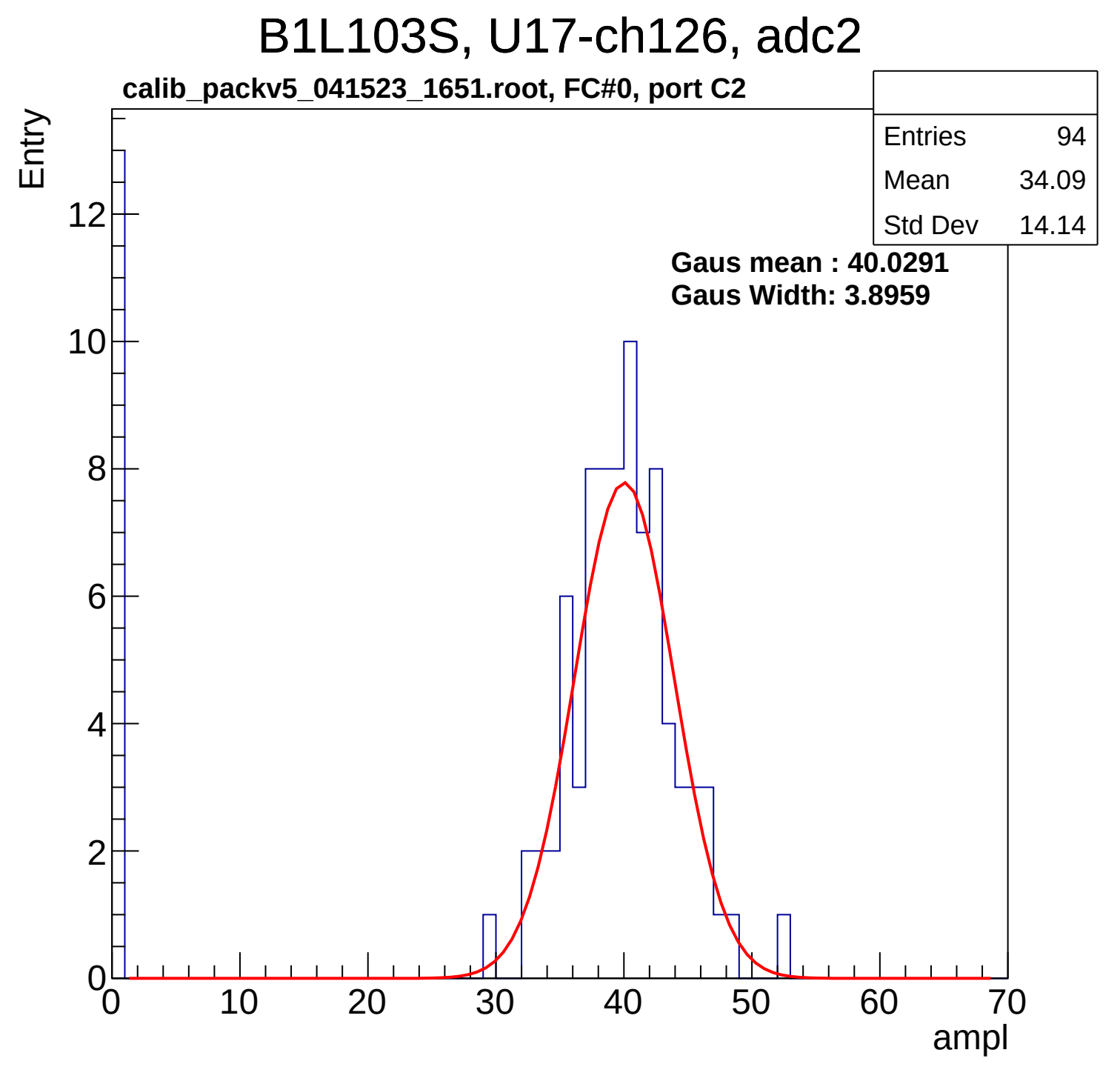

B1L103S, U17-ch125, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 57.5
Std Dev 8.608
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

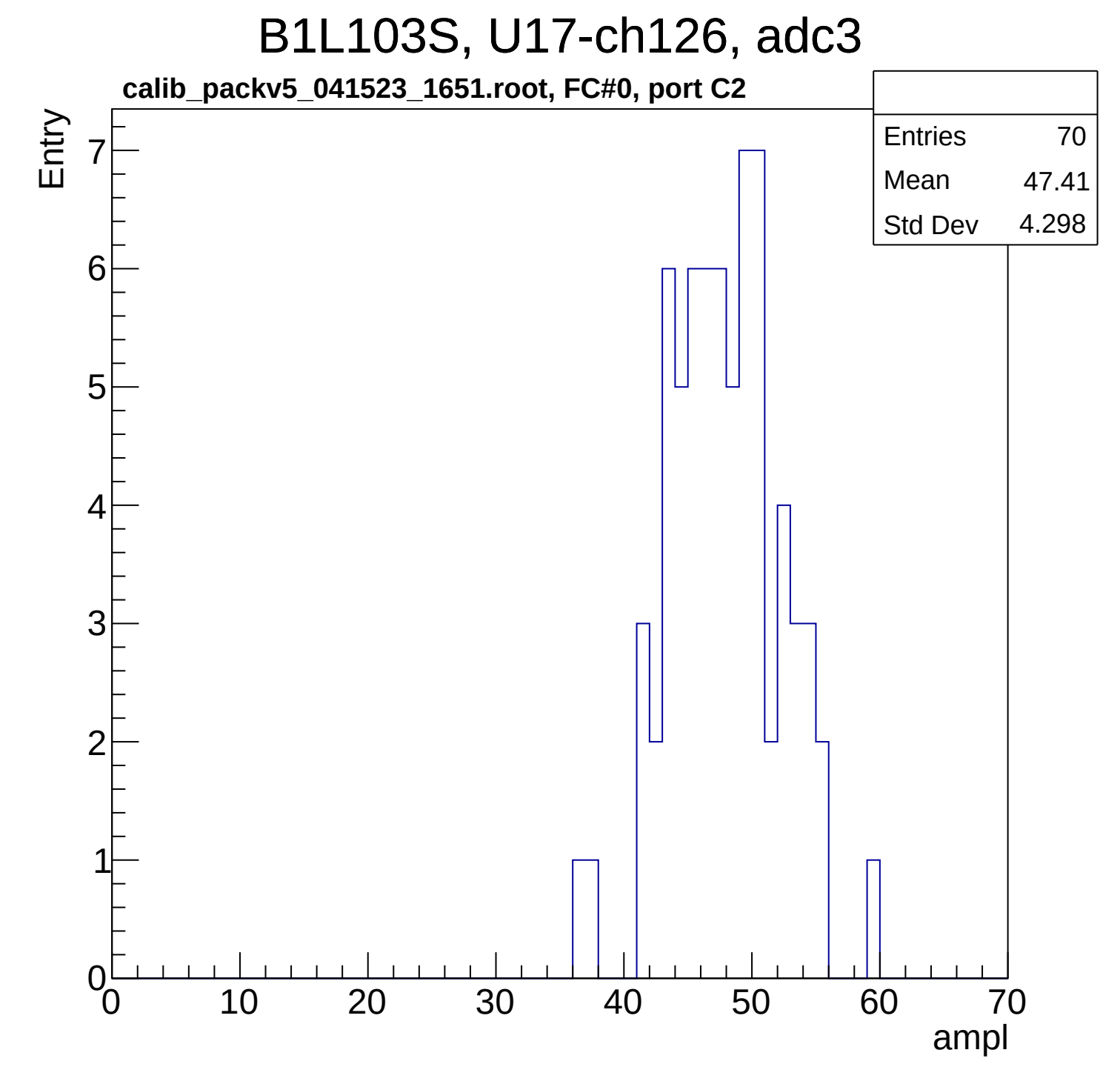

B1L103S, U17-ch125, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 61.5
Std Dev 1.572
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

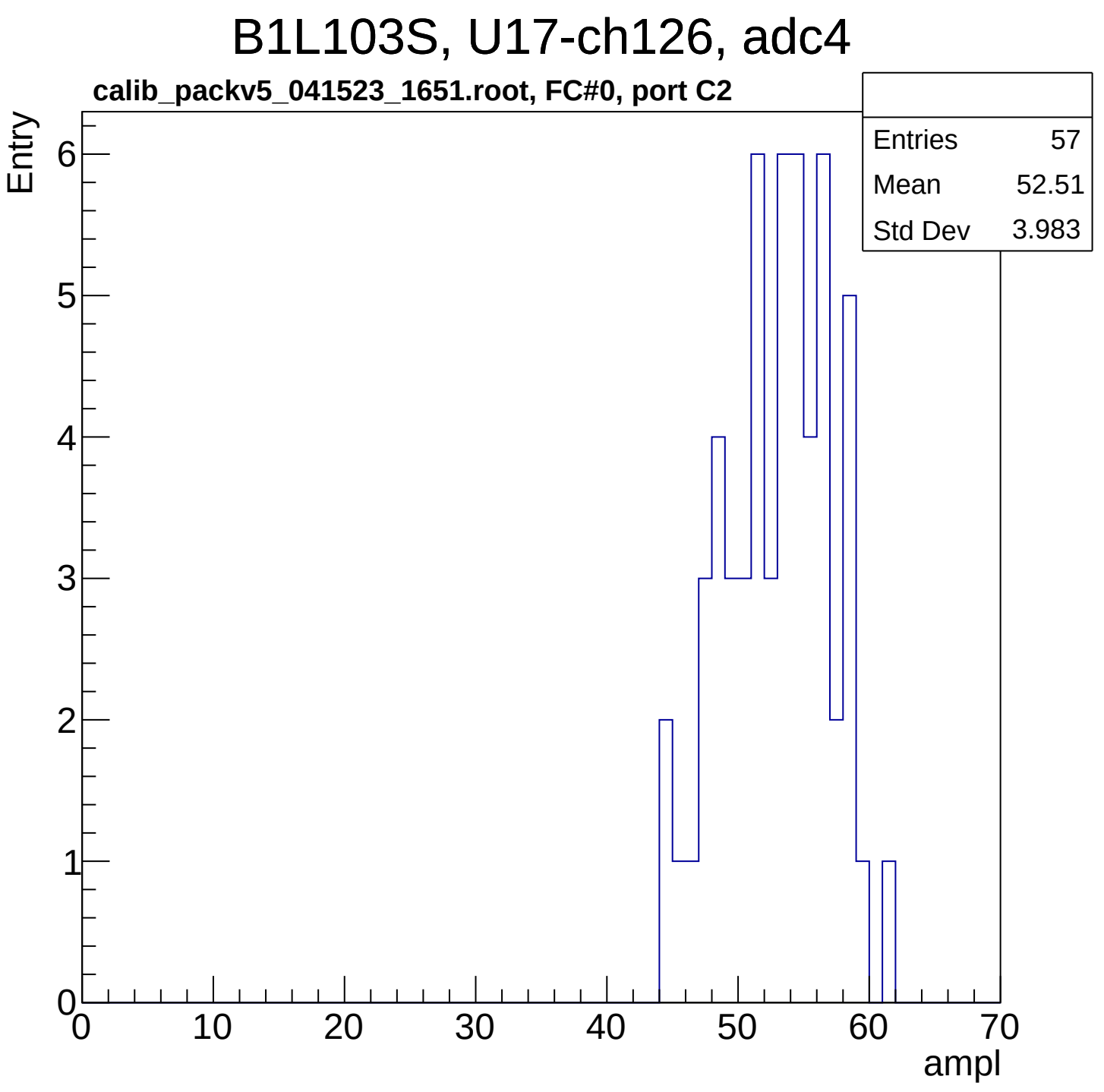

B1L103S, U17-ch125, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

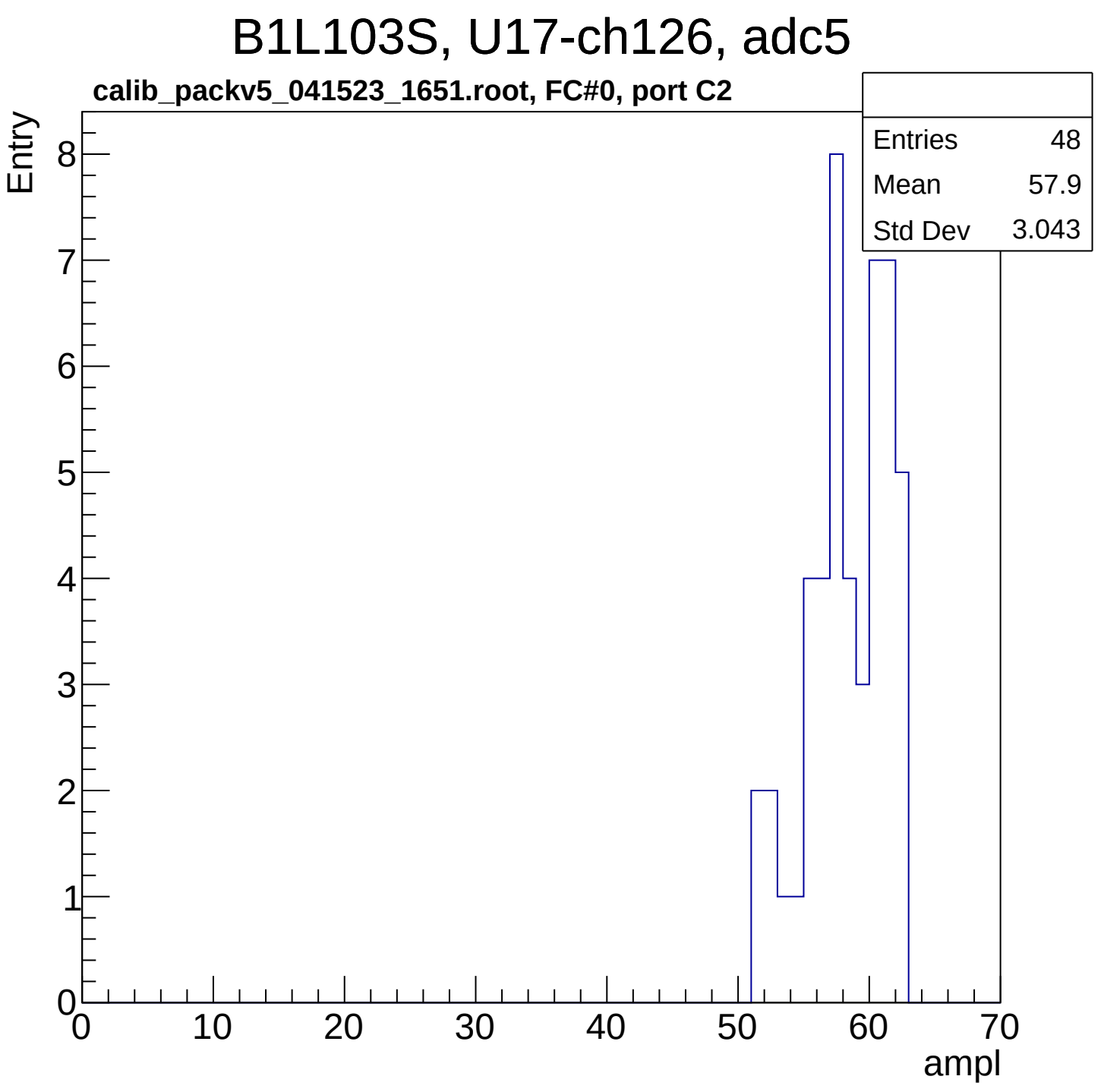

B1L103S, U17-ch126, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 22.58
Std Dev 10.2
Gaus mean : 27.0241
Gaus Width: 4.1886
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

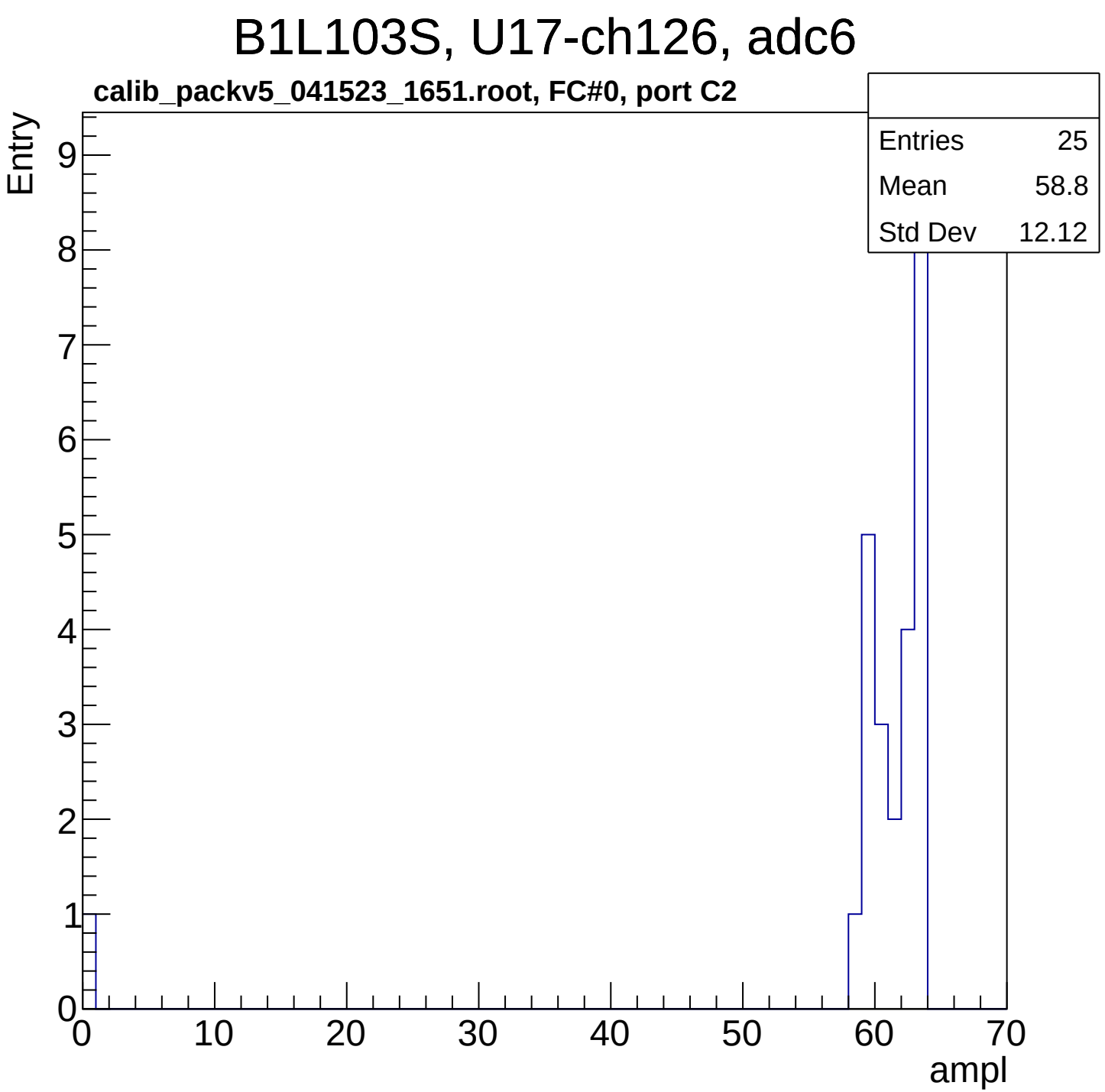

B1L103S, U17-ch126, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 29.1
Std Dev 9.483
Gaus mean : 32.1638
Gaus Width: 4.2177
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

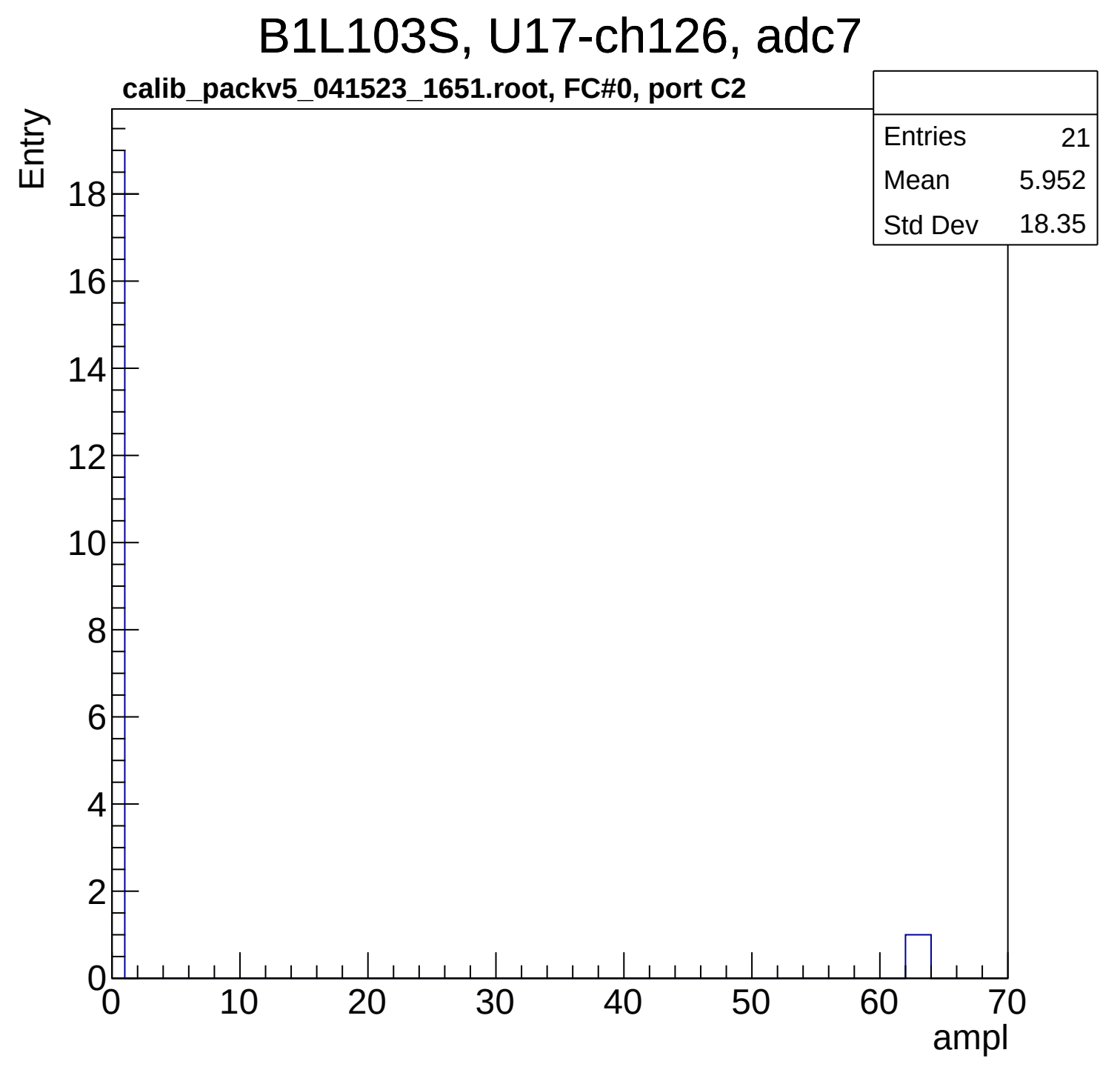

B1L103S, U17-ch126, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 34.09
Std Dev 14.14
Gaus mean : 40.0291
Gaus Width: 3.8959
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

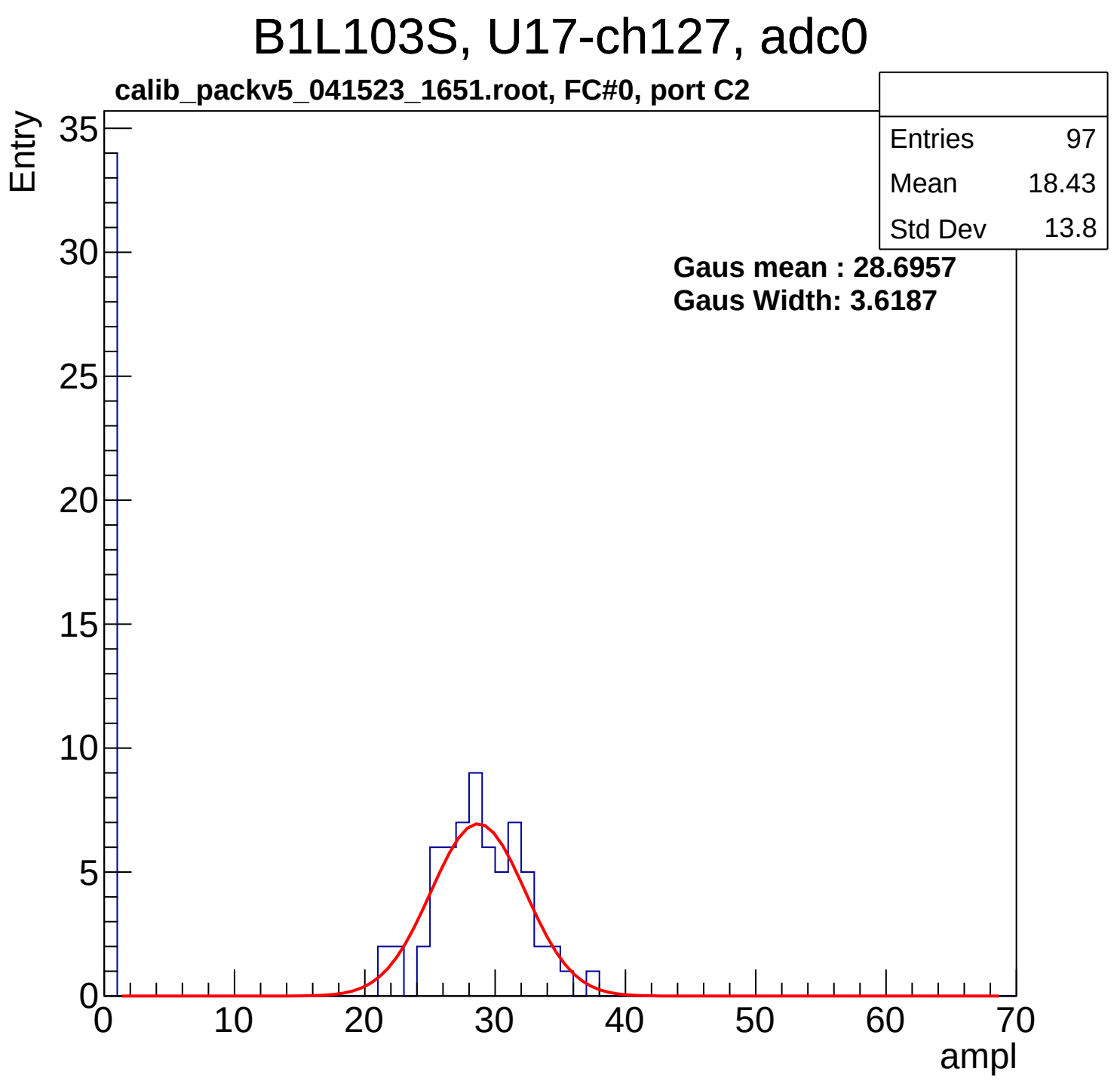

B1L103S, U17-ch126, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 47.41
Std Dev 4.298
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

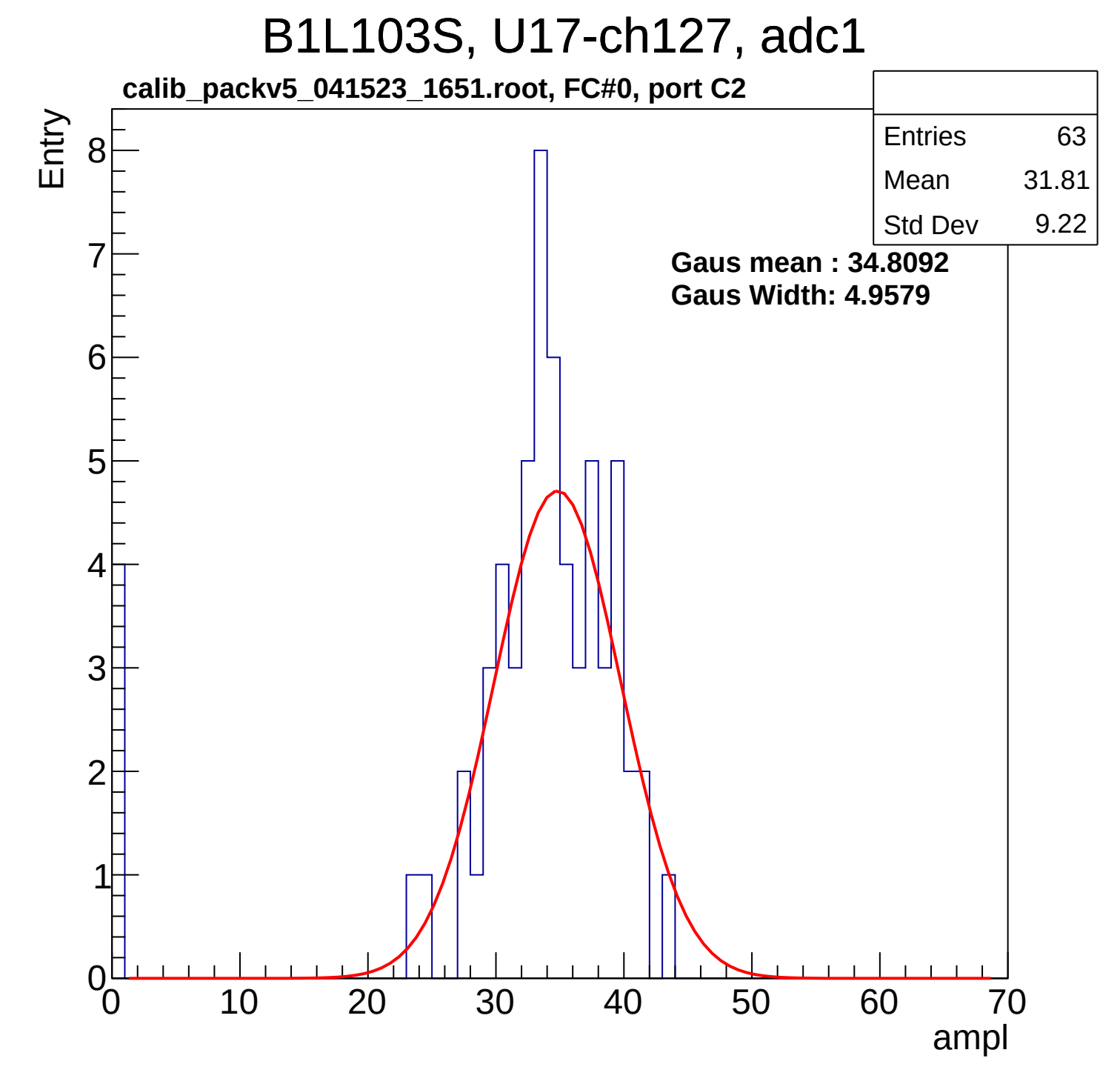

B1L103S, U17-ch126, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 52.51
Std Dev 3.983
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

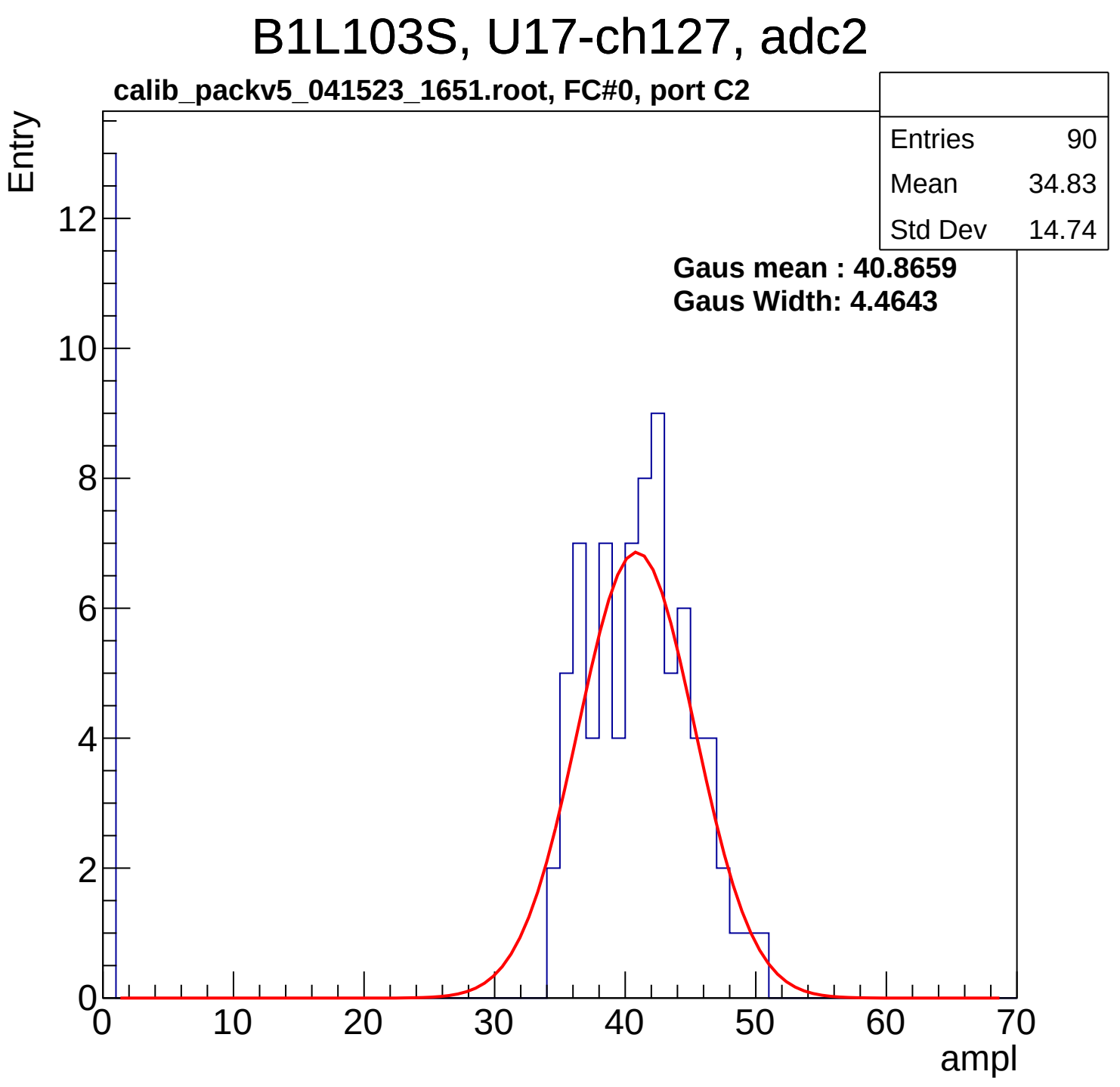

B1L103S, U17-ch126, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 57.9
Std Dev 3.043
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

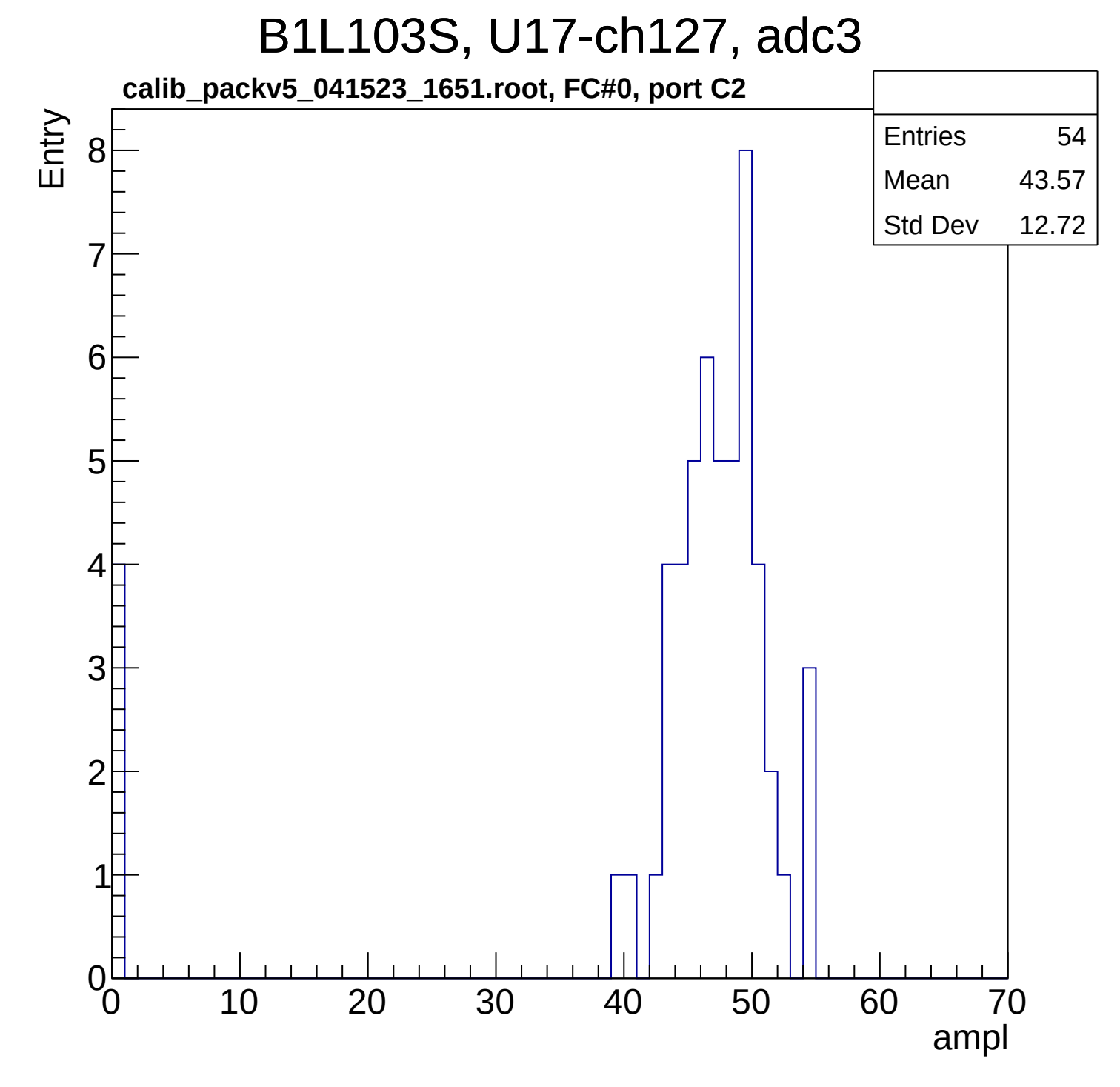

B1L103S, U17-ch126, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 58.8
Std Dev 12.12
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

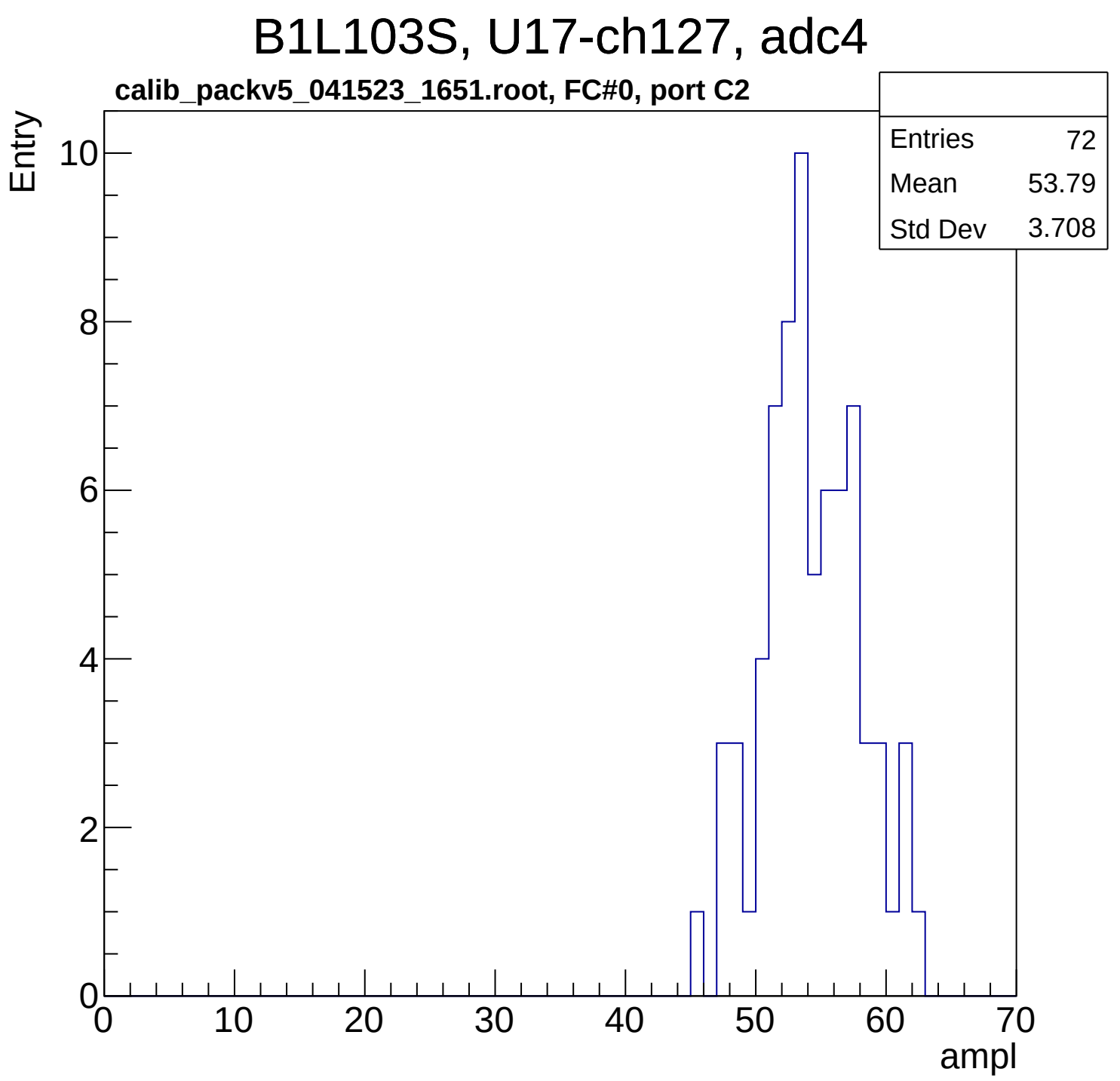

B1L103S, U17-ch126, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

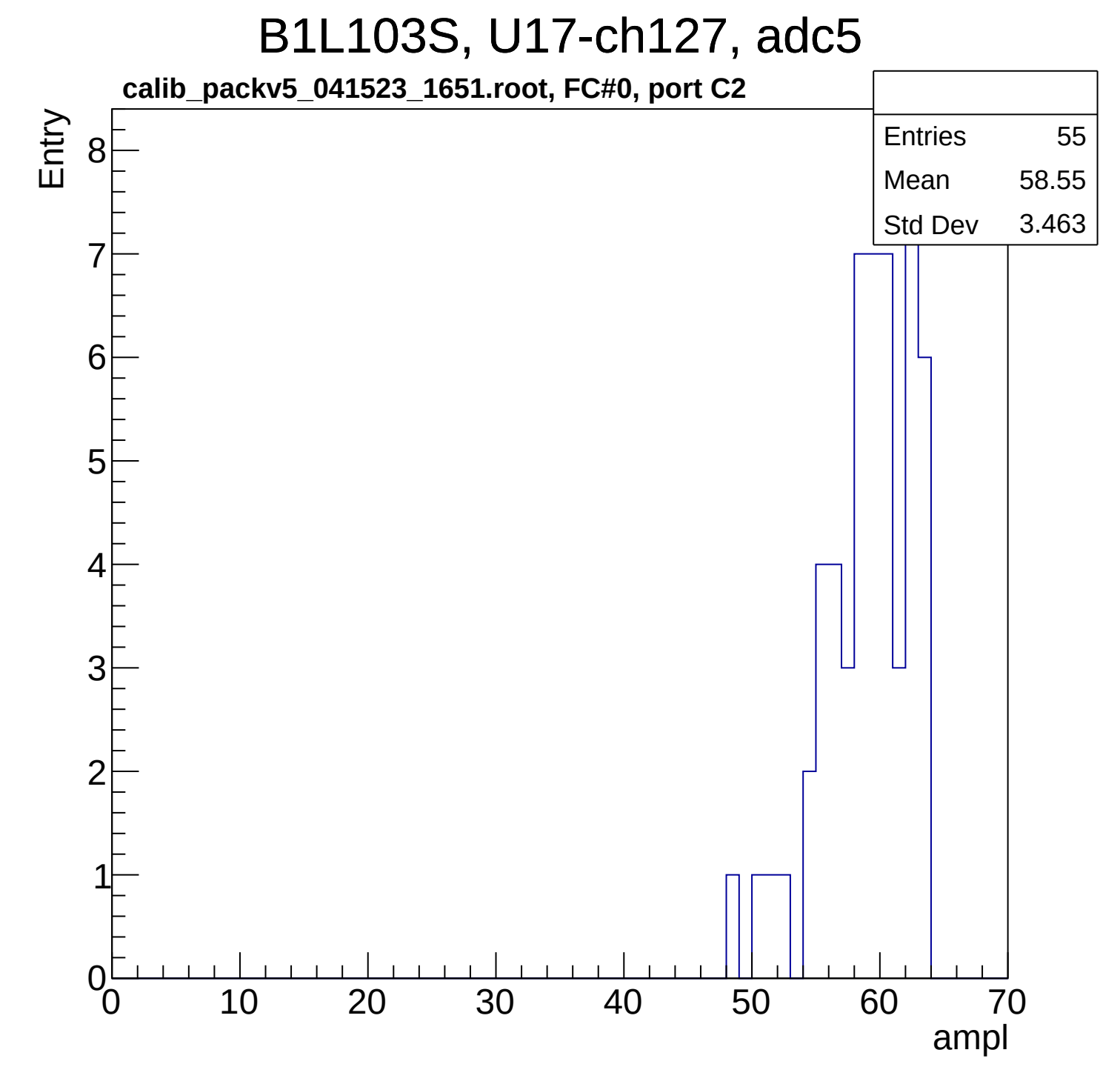

B1L103S, U17-ch127, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 18.43
Std Dev 13.8
Gaus mean : 28.6957
Gaus Width: 3.6187
Entry
ampl
0
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70

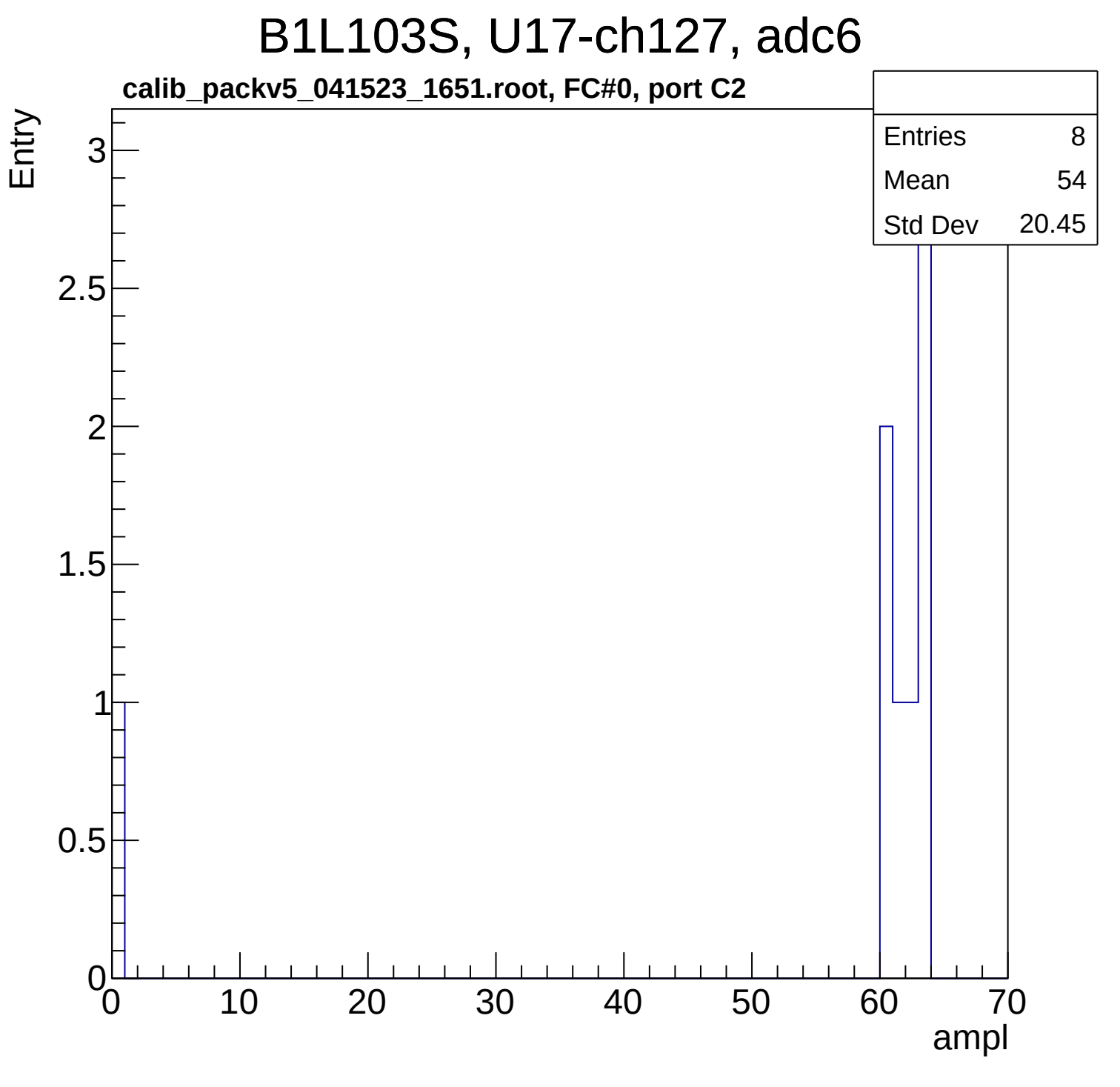

B1L103S, U17-ch127, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 31.81
Std Dev 9.22
Gaus mean : 34.8092
Gaus Width: 4.9579
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

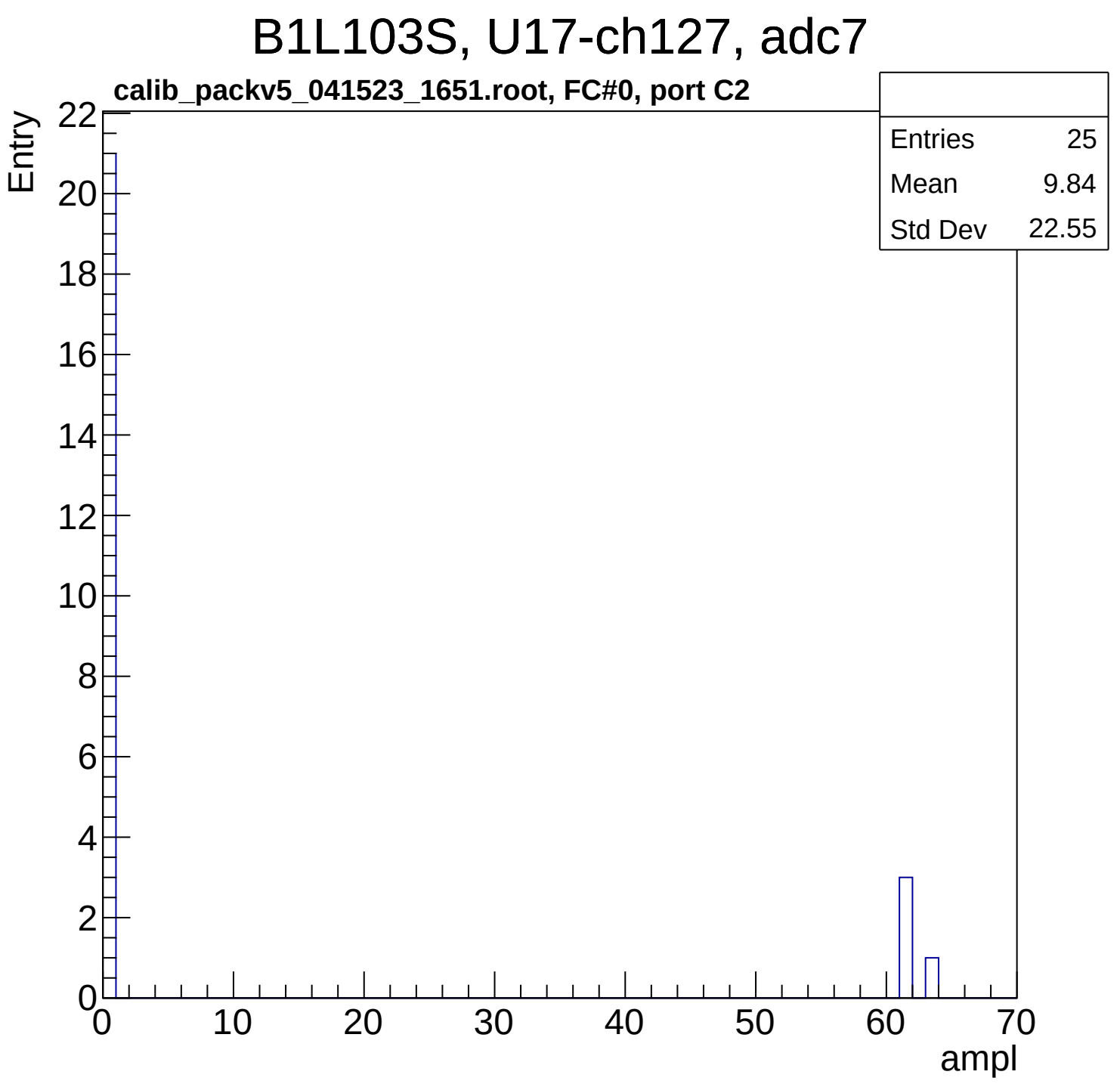

B1L103S, U17-ch127, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 34.83
Std Dev 14.74
Gaus mean : 40.8659
Gaus Width: 4.4643
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

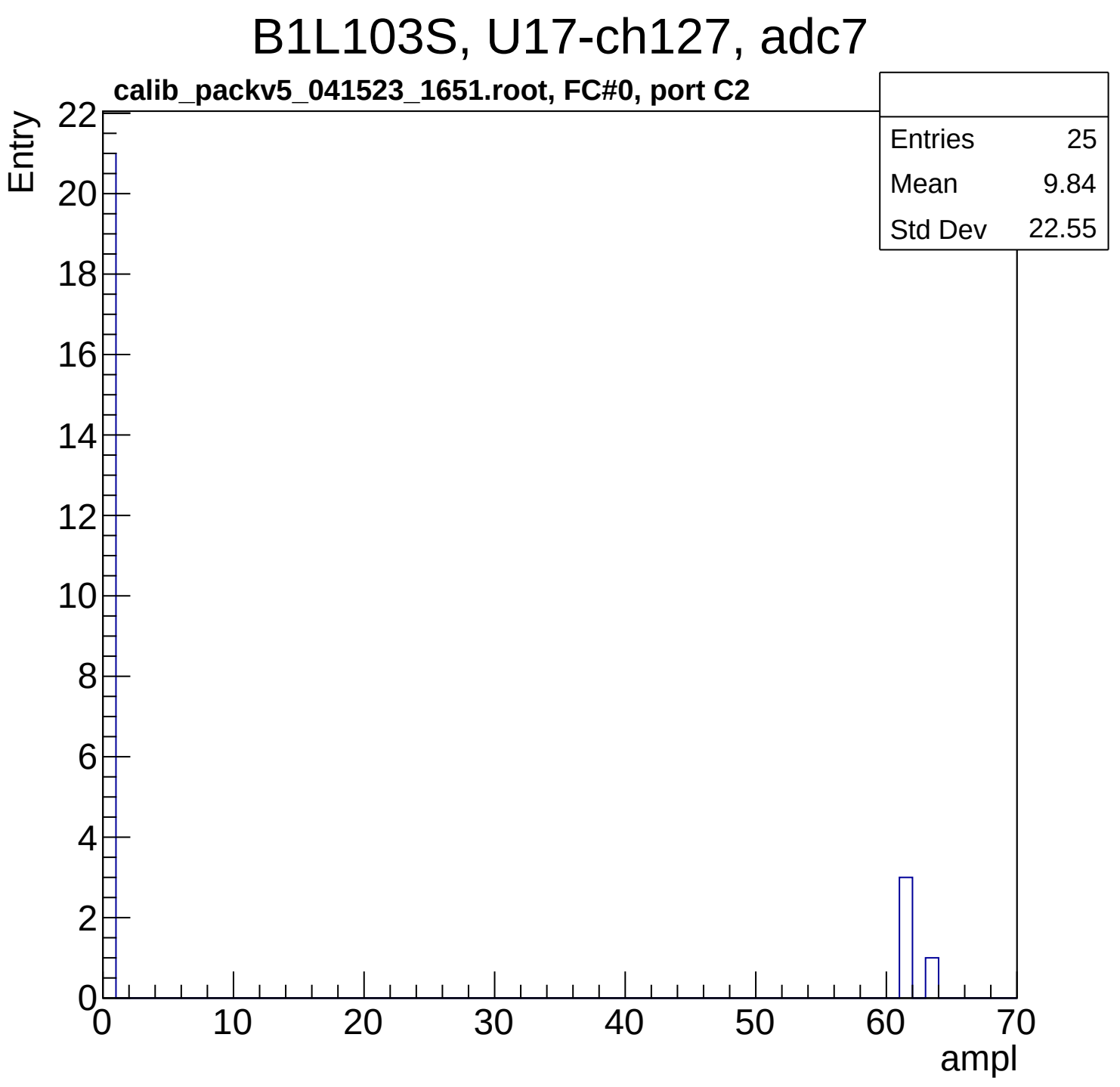

B1L103S, U17-ch127, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 43.57
Std Dev 12.72
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch127, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 53.79
Std Dev 3.708
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U17-ch127, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.55
Std Dev 3.463
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U17-ch127, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 54
Std Dev 20.45
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U17-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 9.84
Std Dev 22.55
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U17-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 9.84
Std Dev 22.55
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70