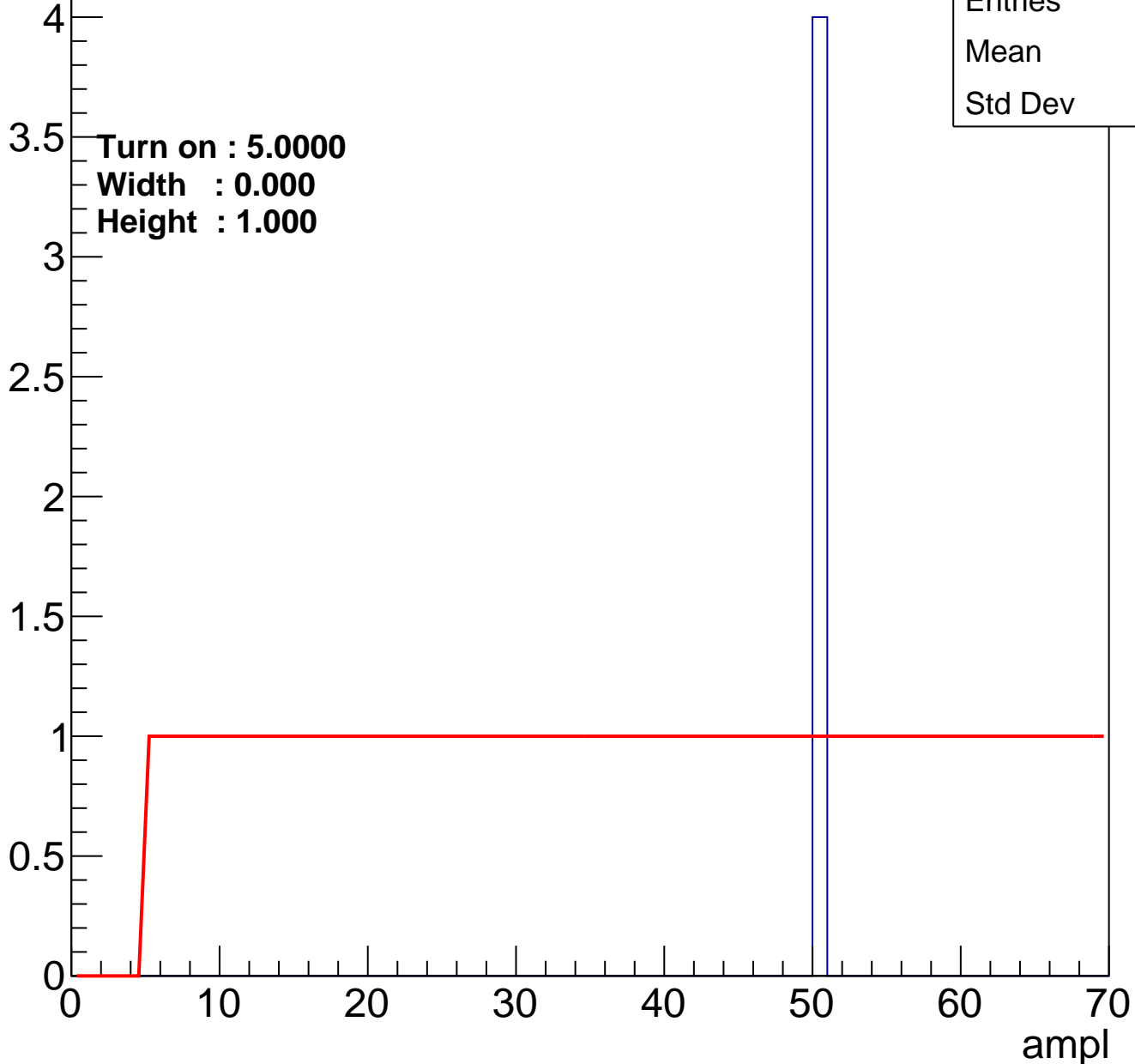




# B0L100S, U12-ch0

calib\_packv5\_042523\_0143.root, FC#6, port A1

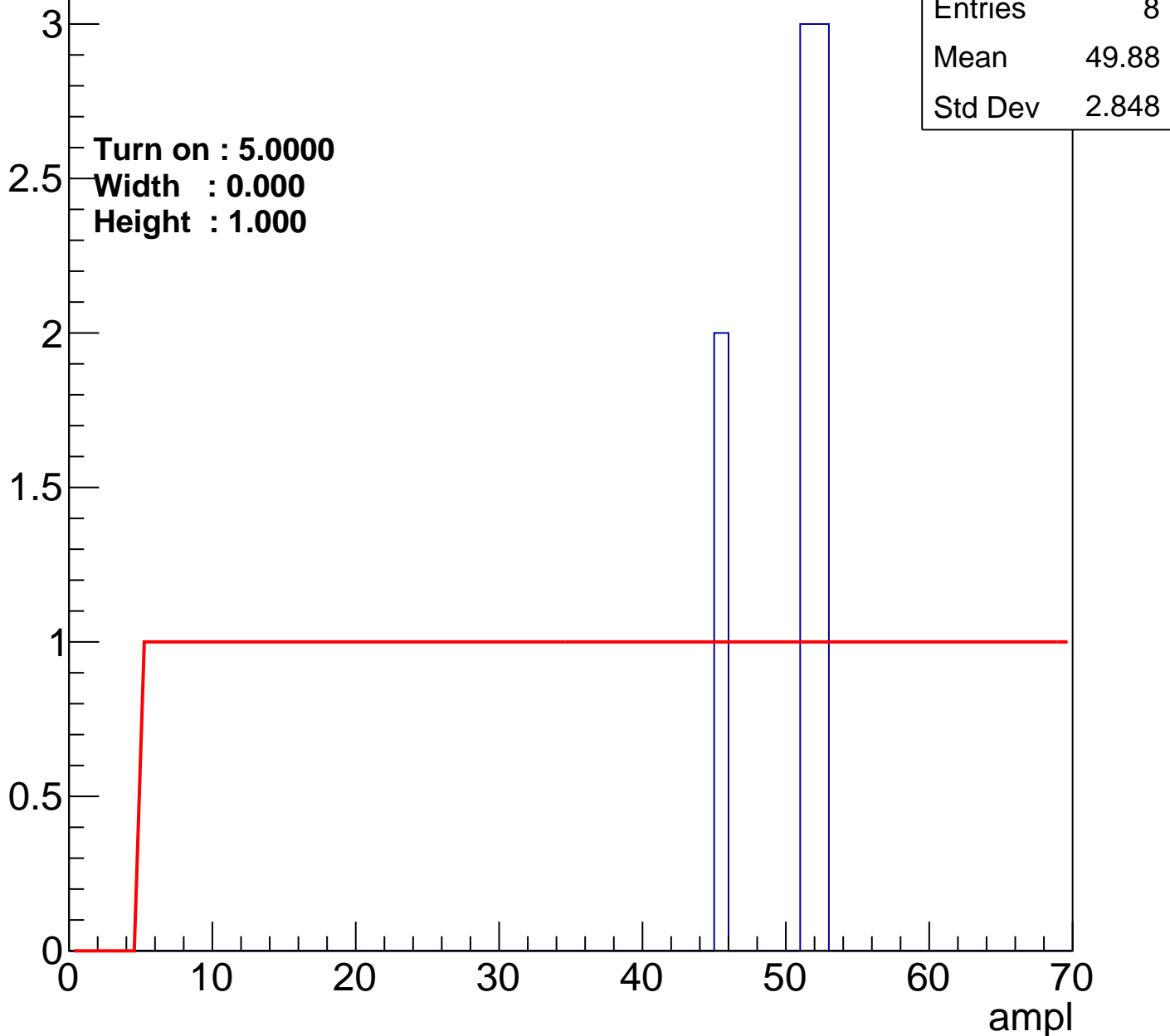
Entry



# B0L100S, U12-ch1

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U12-ch2

calib\_packv5\_042523\_0143.root, FC#6, port A1

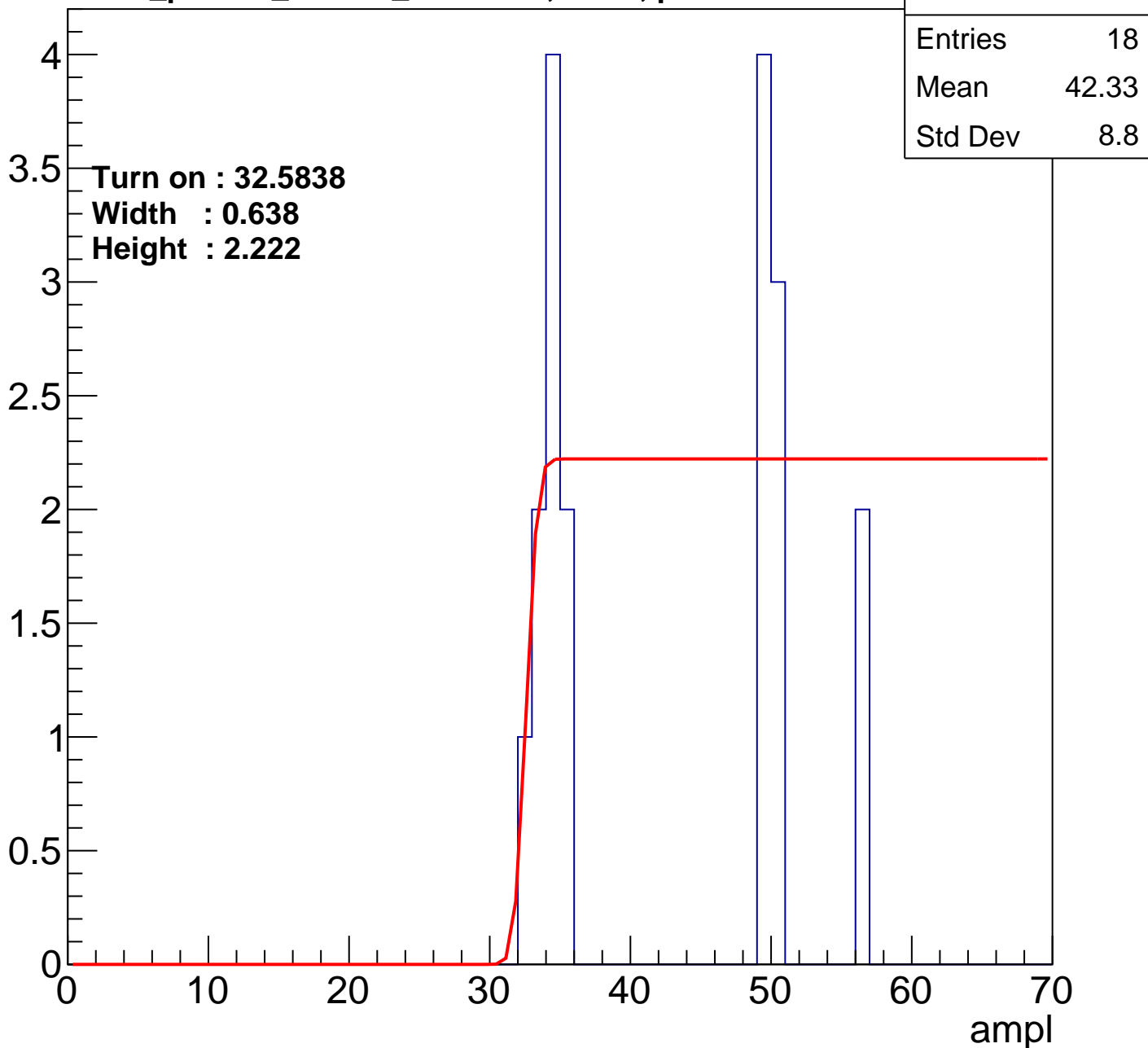
Entry

4  
3.5  
3  
2.5  
2  
1.5  
1  
0.5  
0

Turn on : 32.5838  
Width : 0.638  
Height : 2.222

Entries	18
Mean	42.33
Std Dev	8.8

ampl



# B0L100S, U12-ch3

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U12-ch4

calib\_packv5\_042523\_0143.root, FC#6, port A1

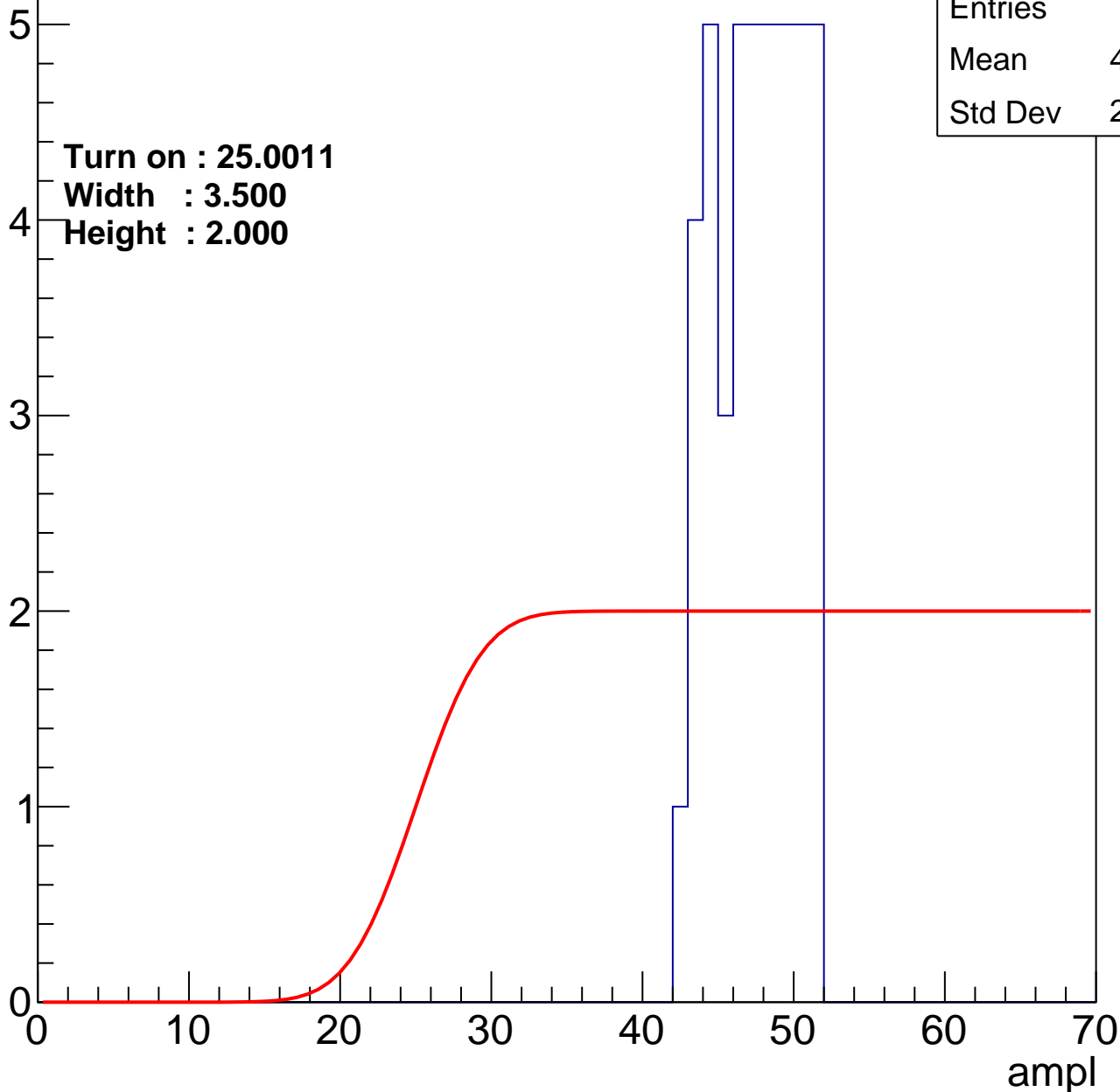
Entry

Entries	43
Mean	47.07
Std Dev	2.645

Turn on : 25.0011

Width : 3.500

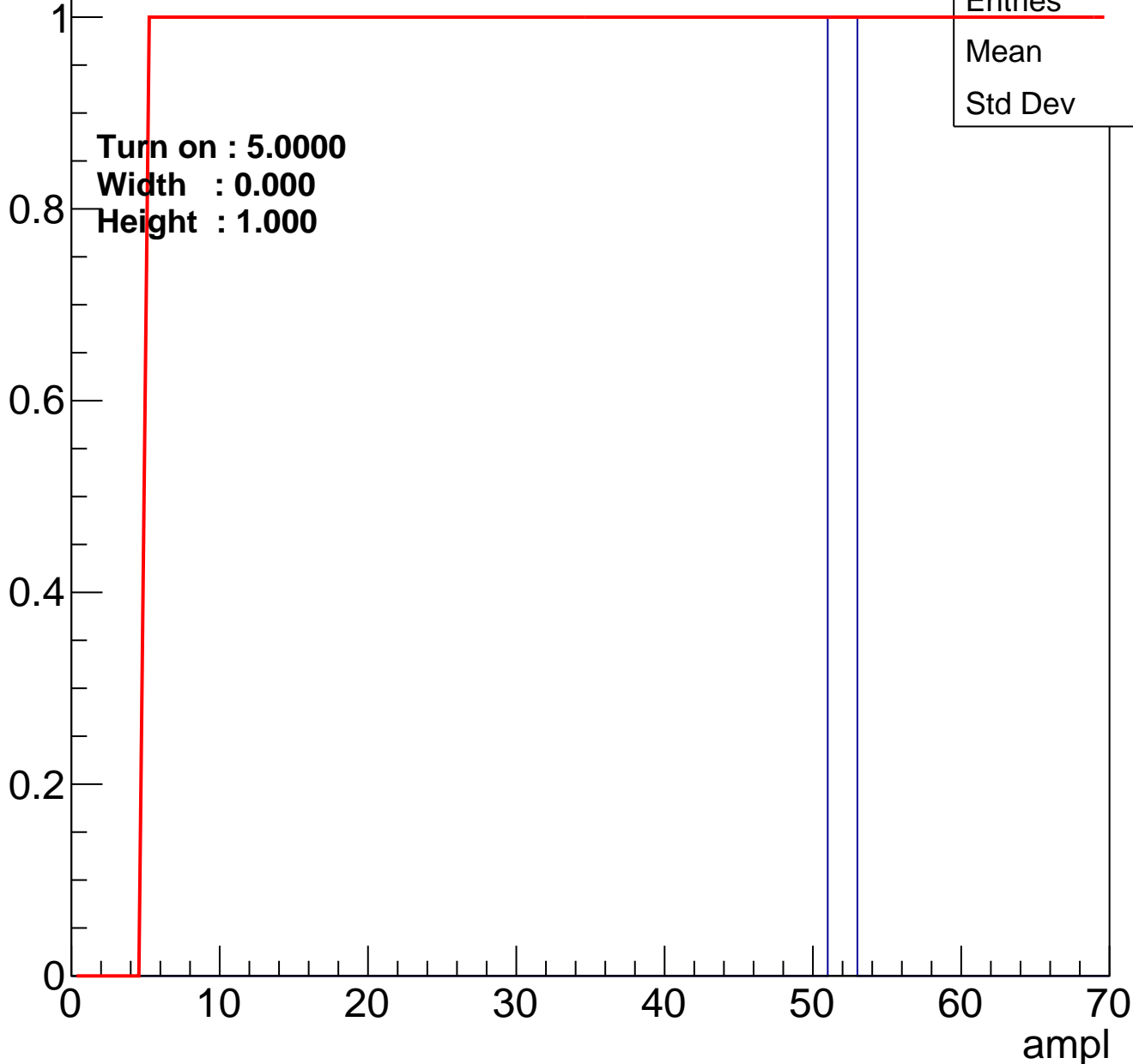
Height : 2.000



# B0L100S, U12-ch5

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	2
Mean	51.5
Std Dev	0.5

# B0L100S, U12-ch6

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L100S, U12-ch7

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U12-ch8

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U12-ch9

calib\_packv5\_042523\_0143.root, FC#6, port A1

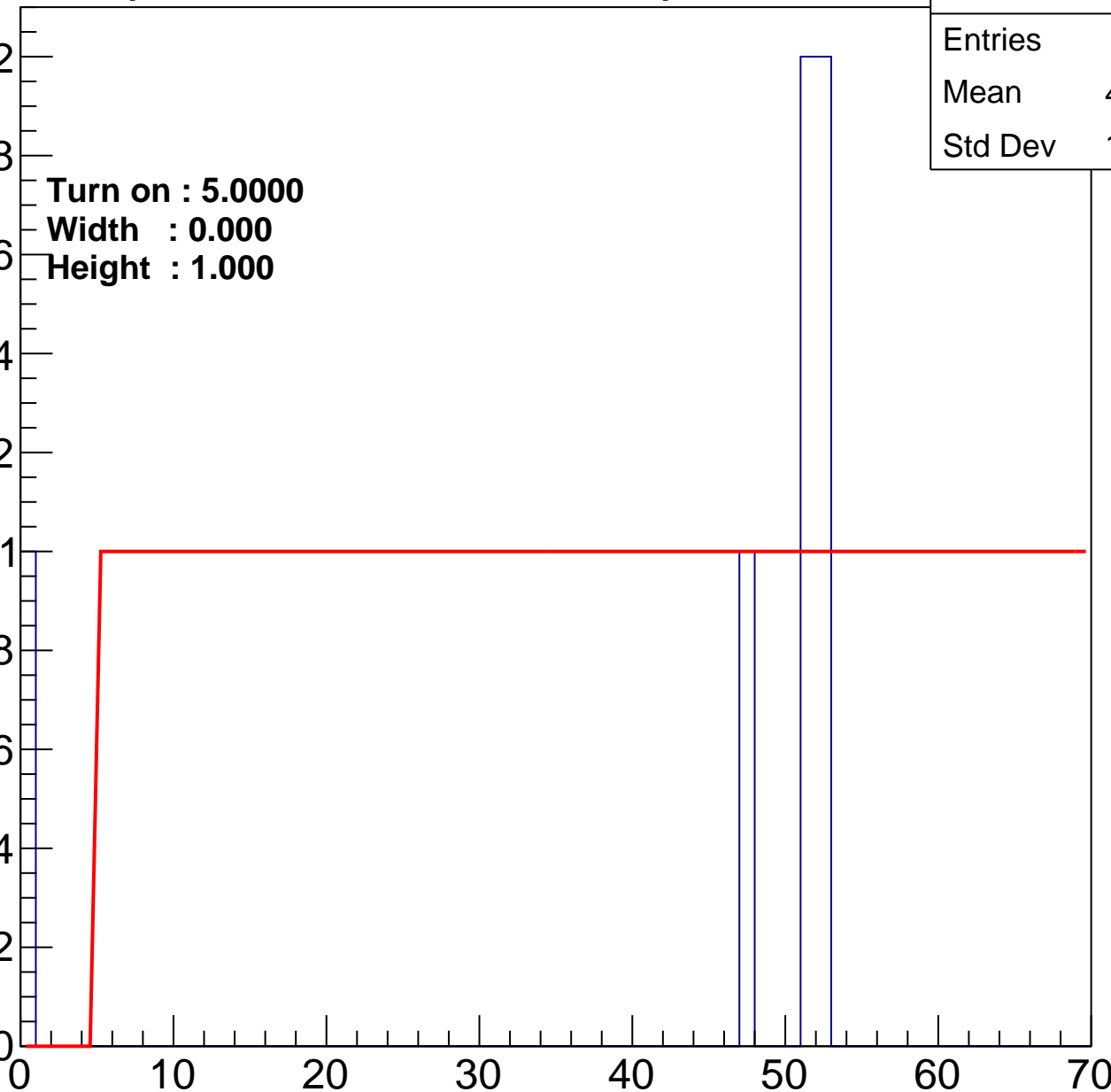
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Turn on : 5.0000  
Width : 0.000  
Height : 1.000

Entries	6
Mean	42.17
Std Dev	18.93

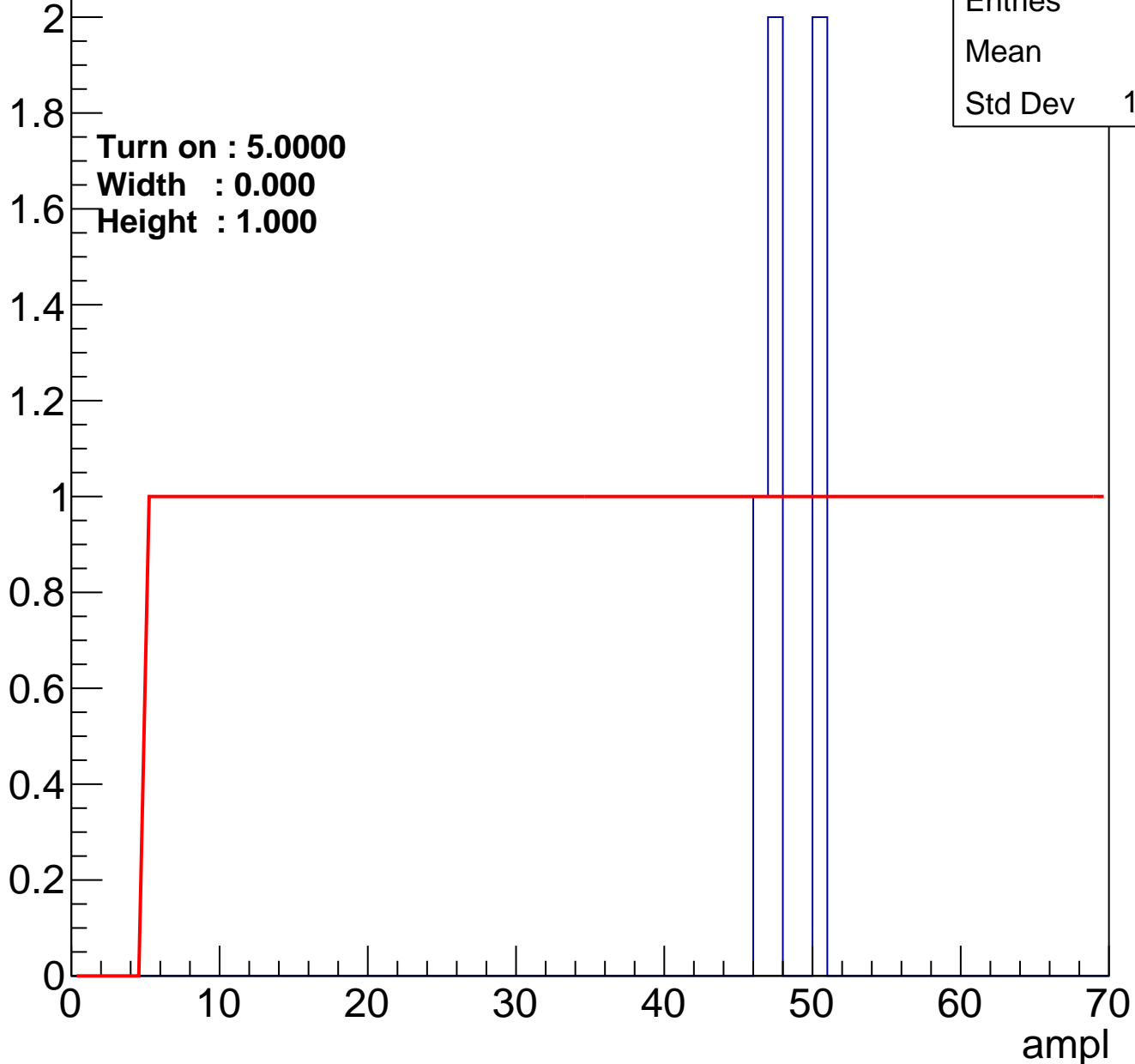
ampl



# B0L100S, U12-ch10

calib\_packv5\_042523\_0143.root, FC#6, port A1

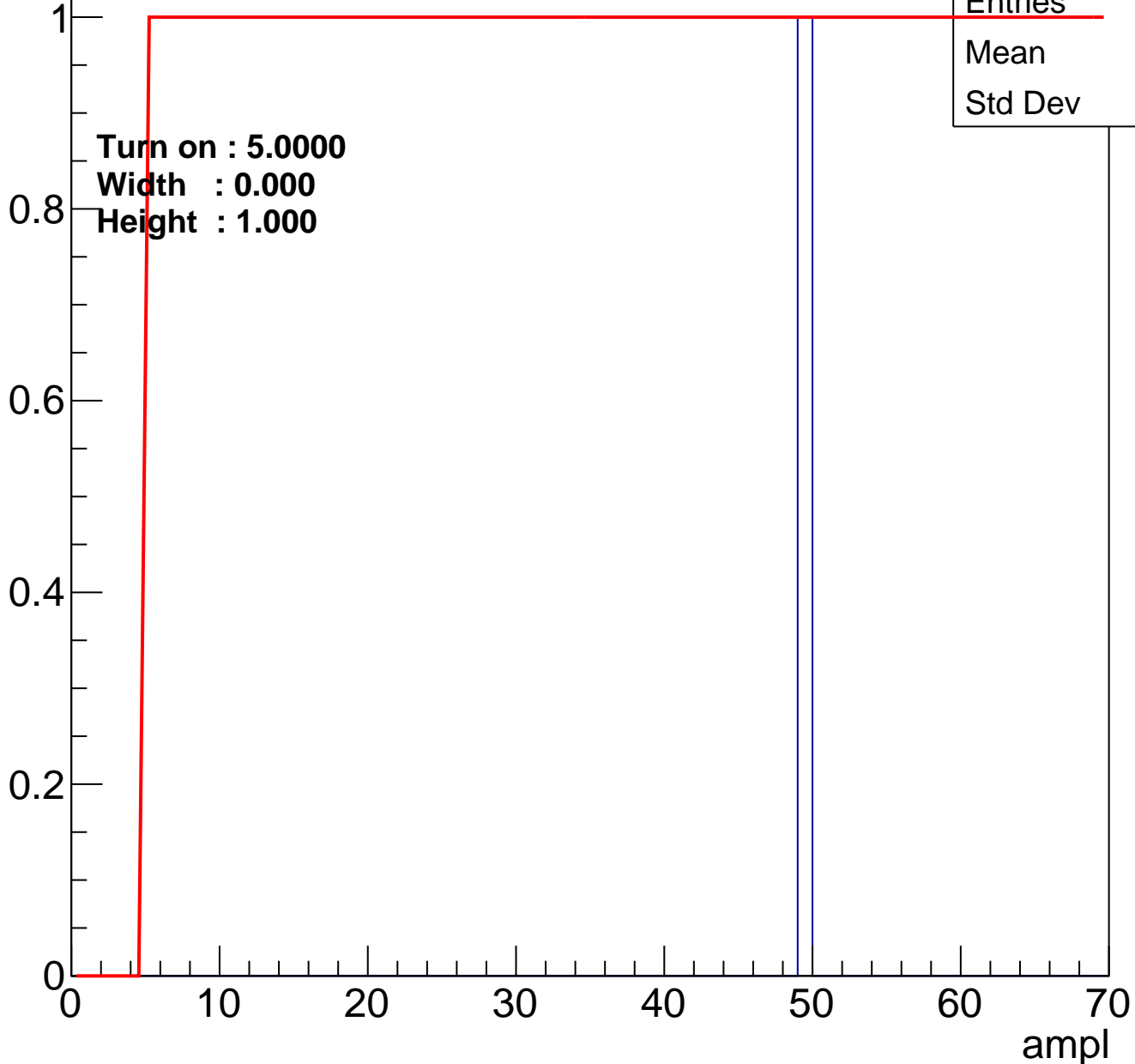
Entry



# B0L100S, U12-ch11

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	1
Mean	49
Std Dev	0

# B0L100S, U12-ch12

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

5

4

3

2

1

0

Turn on : 5.0000

Width : 0.000

Height : 1.000

Entries	8
Mean	51.62
Std Dev	0.4841

ampl

0

10

20

30

40

50

60

70

# B0L100S, U12-ch13

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U12-ch14

calib\_packv5\_042523\_0143.root, FC#6, port A1

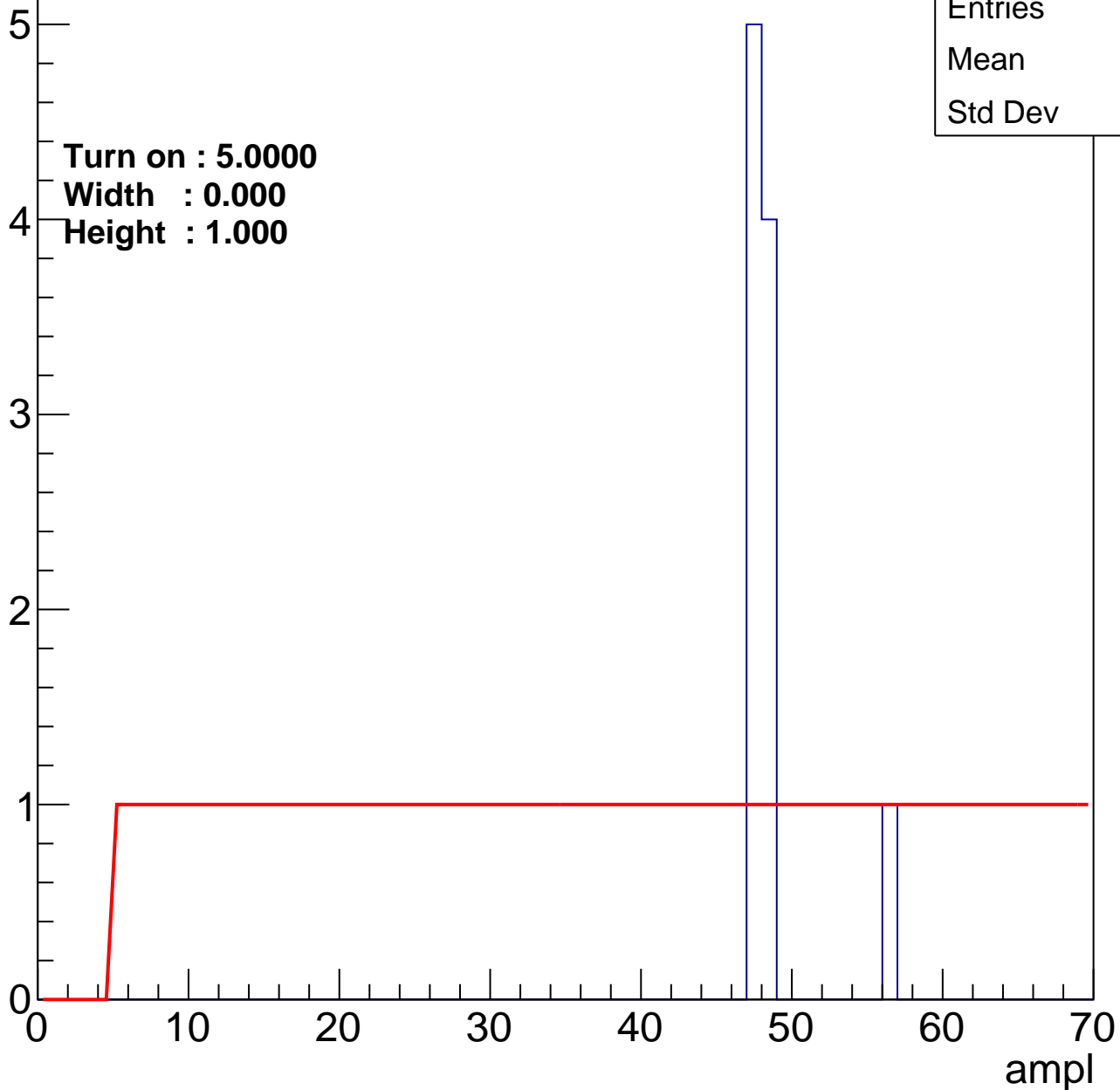
Entry

Entries	10
Mean	48.3
Std Dev	2.61

Turn on : 5.0000

Width : 0.000

Height : 1.000





# B0L100S, U12-ch15

calib\_packv5\_042523\_0143.root, FC#6, port A1

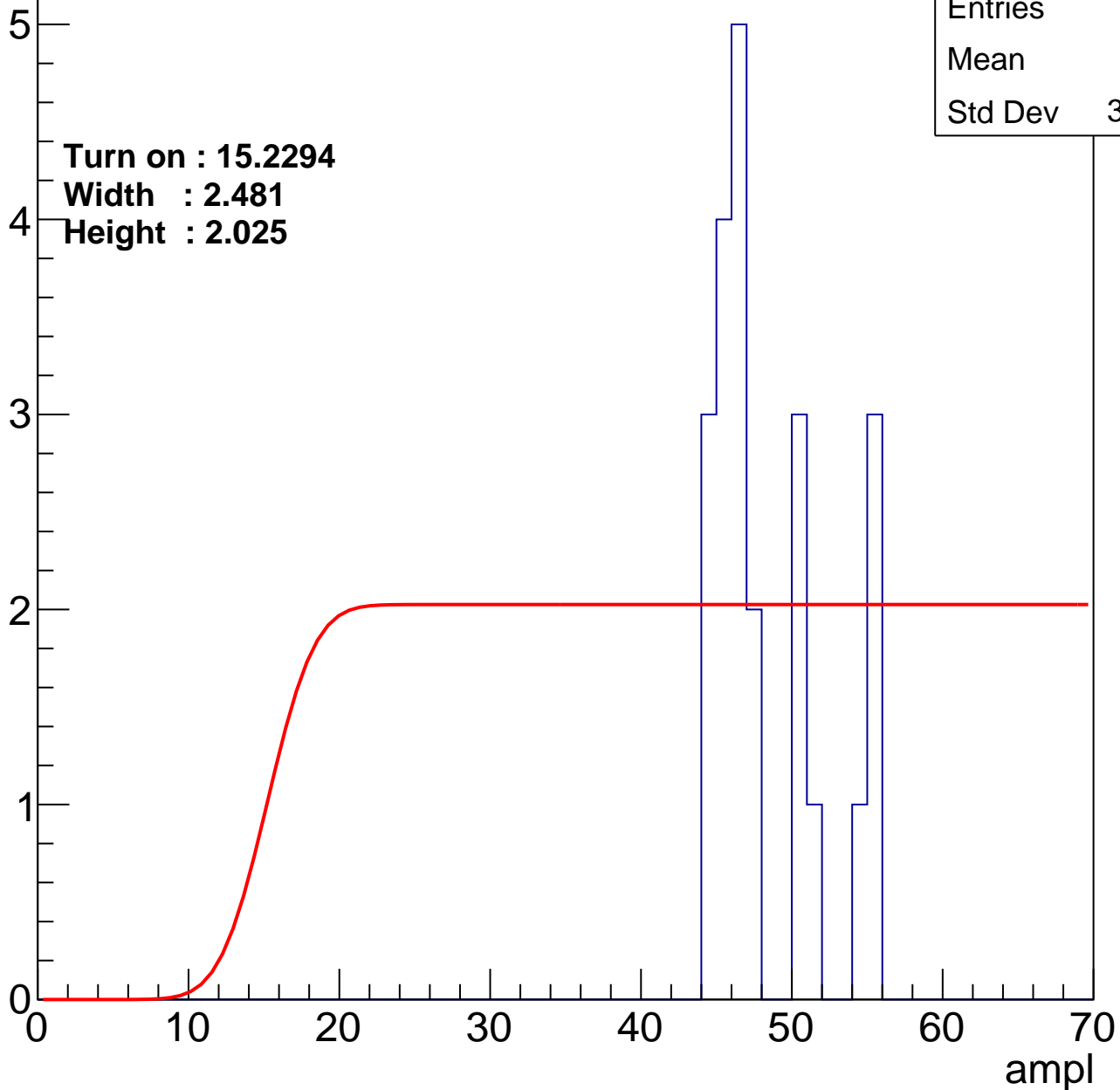
Entry

Entries	22
Mean	48
Std Dev	3.754

Turn on : 15.2294

Width : 2.481

Height : 2.025



# B0L100S, U12-ch16

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U12-ch17

calib\_packv5\_042523\_0143.root, FC#6, port A1

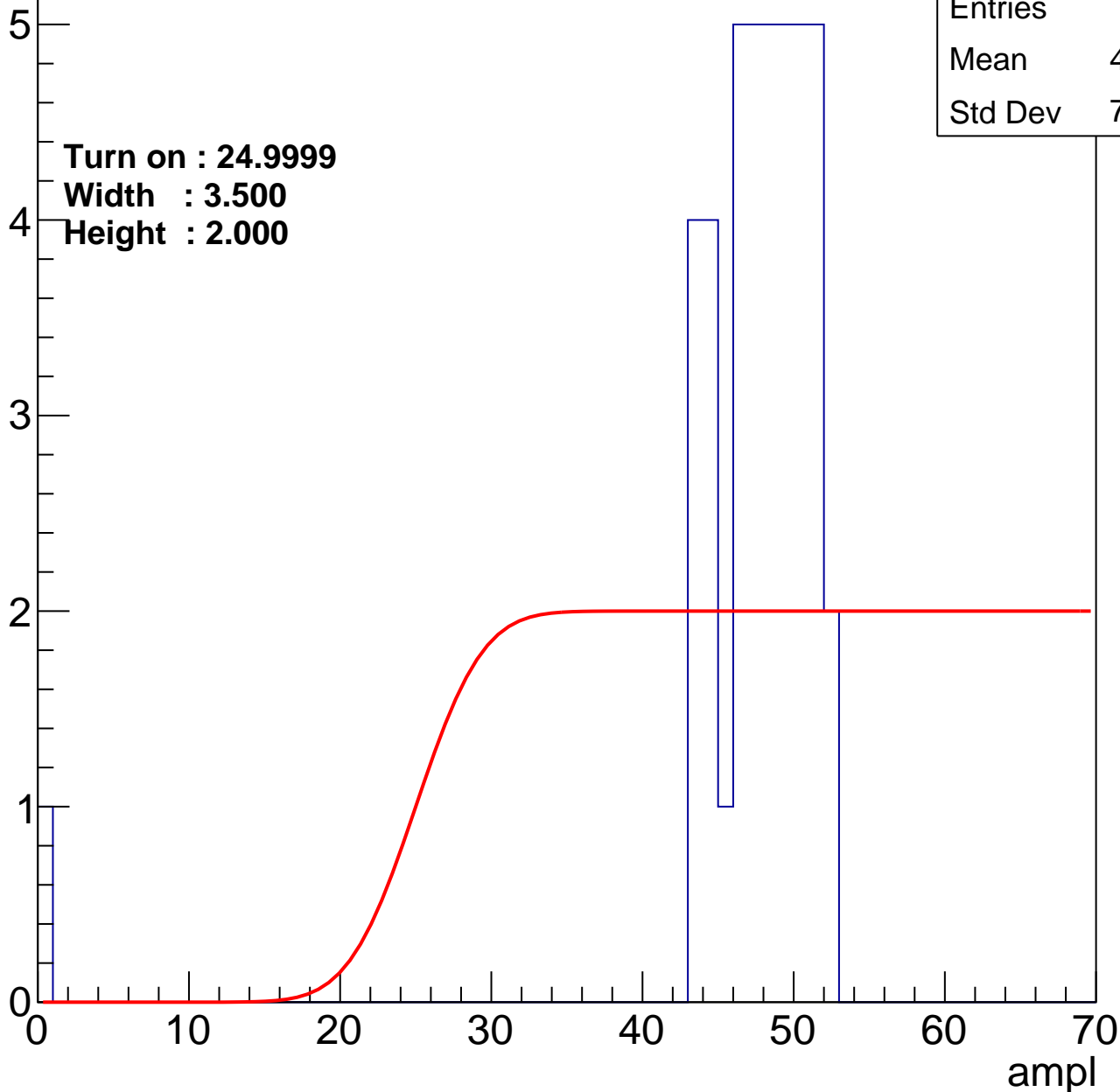
Entry

Entries	42
Mean	46.48
Std Dev	7.725

Turn on : 24.9999

Width : 3.500

Height : 2.000



# B0L100S, U12-ch18

calib\_packv5\_042523\_0143.root, FC#6, port A1

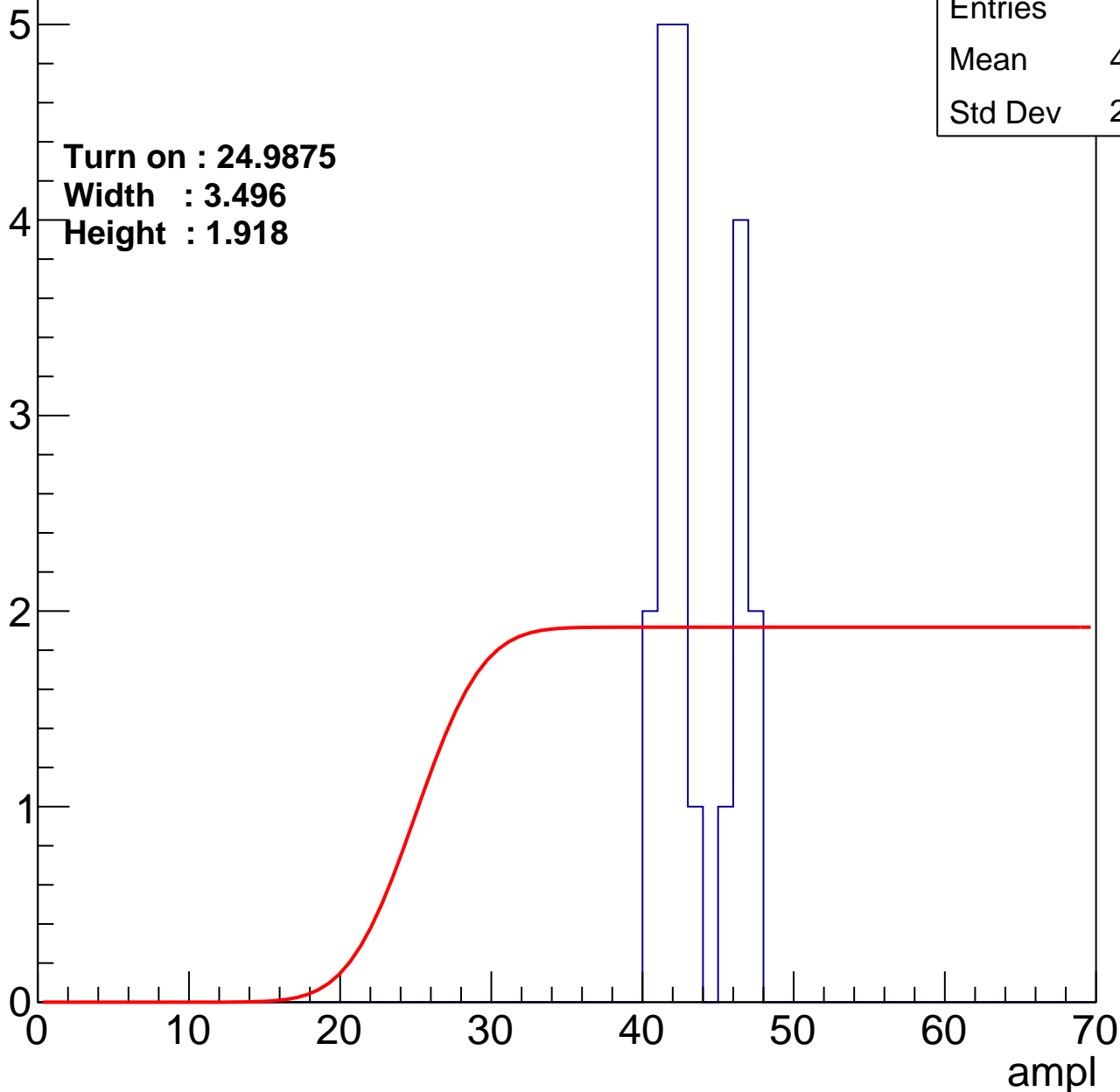
Entry

Entries	20
Mean	43.05
Std Dev	2.397

Turn on : 24.9875

Width : 3.496

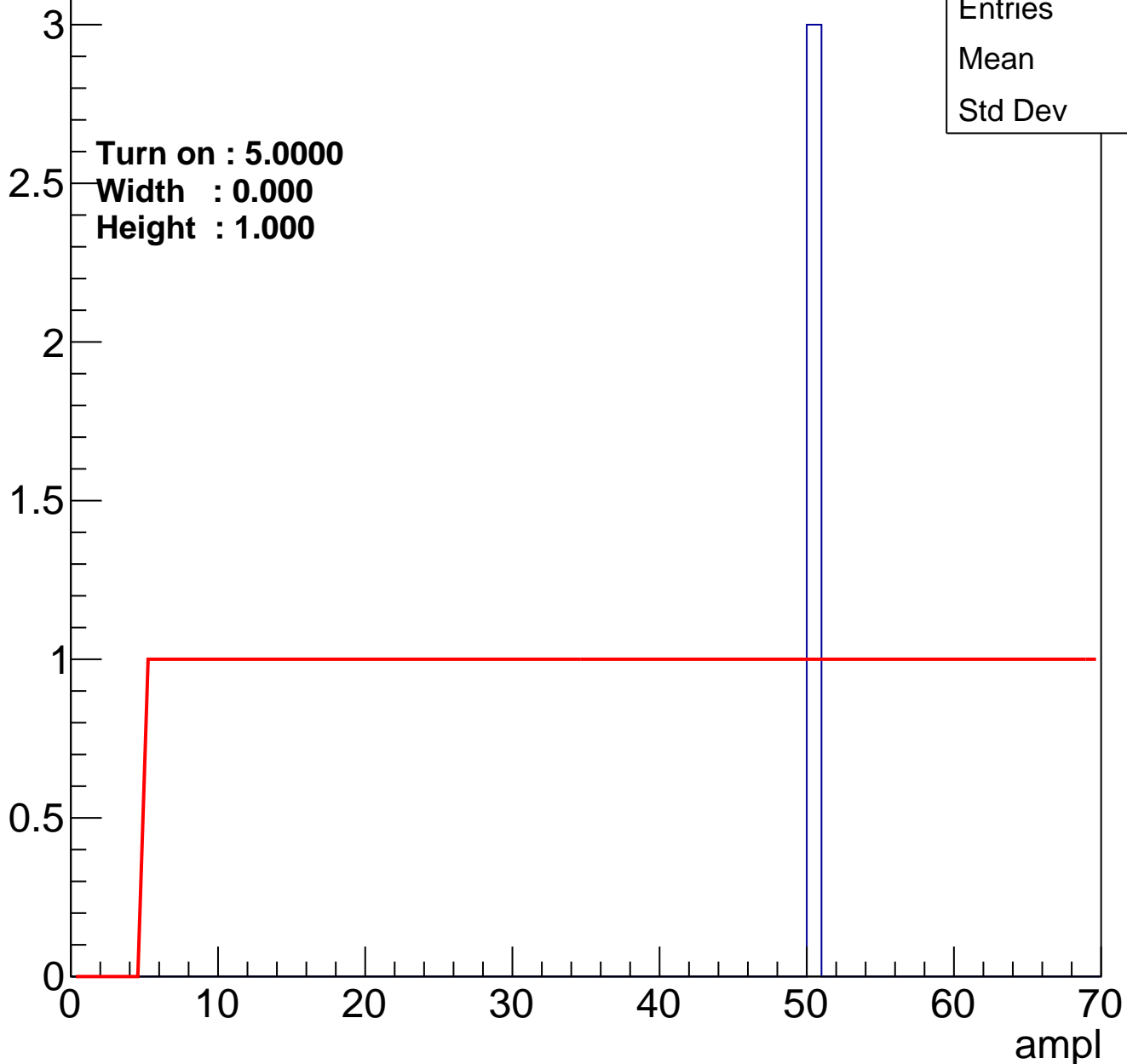
Height : 1.918



# B0L100S, U12-ch19

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U12-ch20

calib\_packv5\_042523\_0143.root, FC#6, port A1

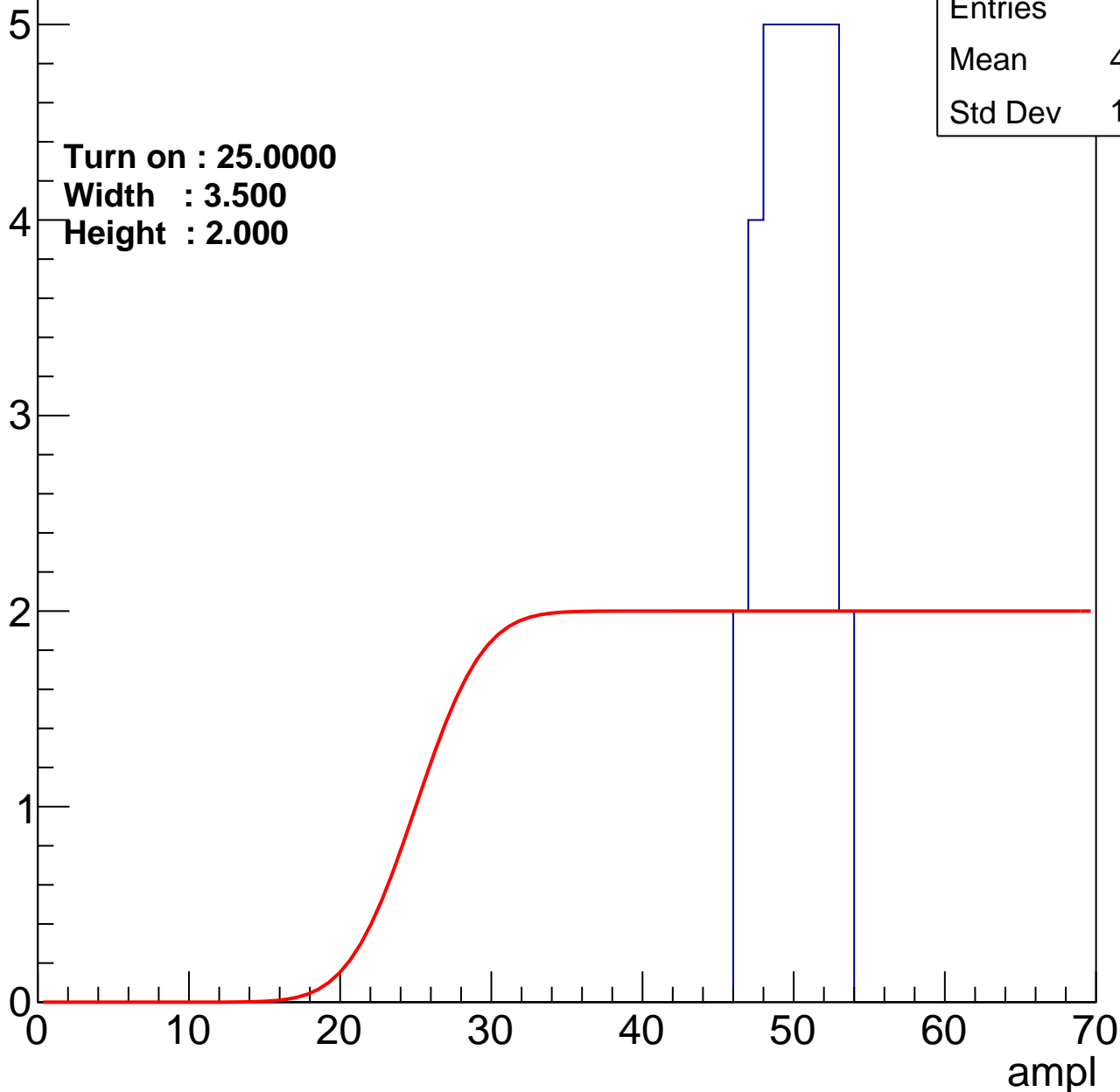
Entry

Entries	33
Mean	49.58
Std Dev	1.985

Turn on : 25.0000

Width : 3.500

Height : 2.000



# B0L100S, U12-ch21

calib\_packv5\_042523\_0143.root, FC#6, port A1

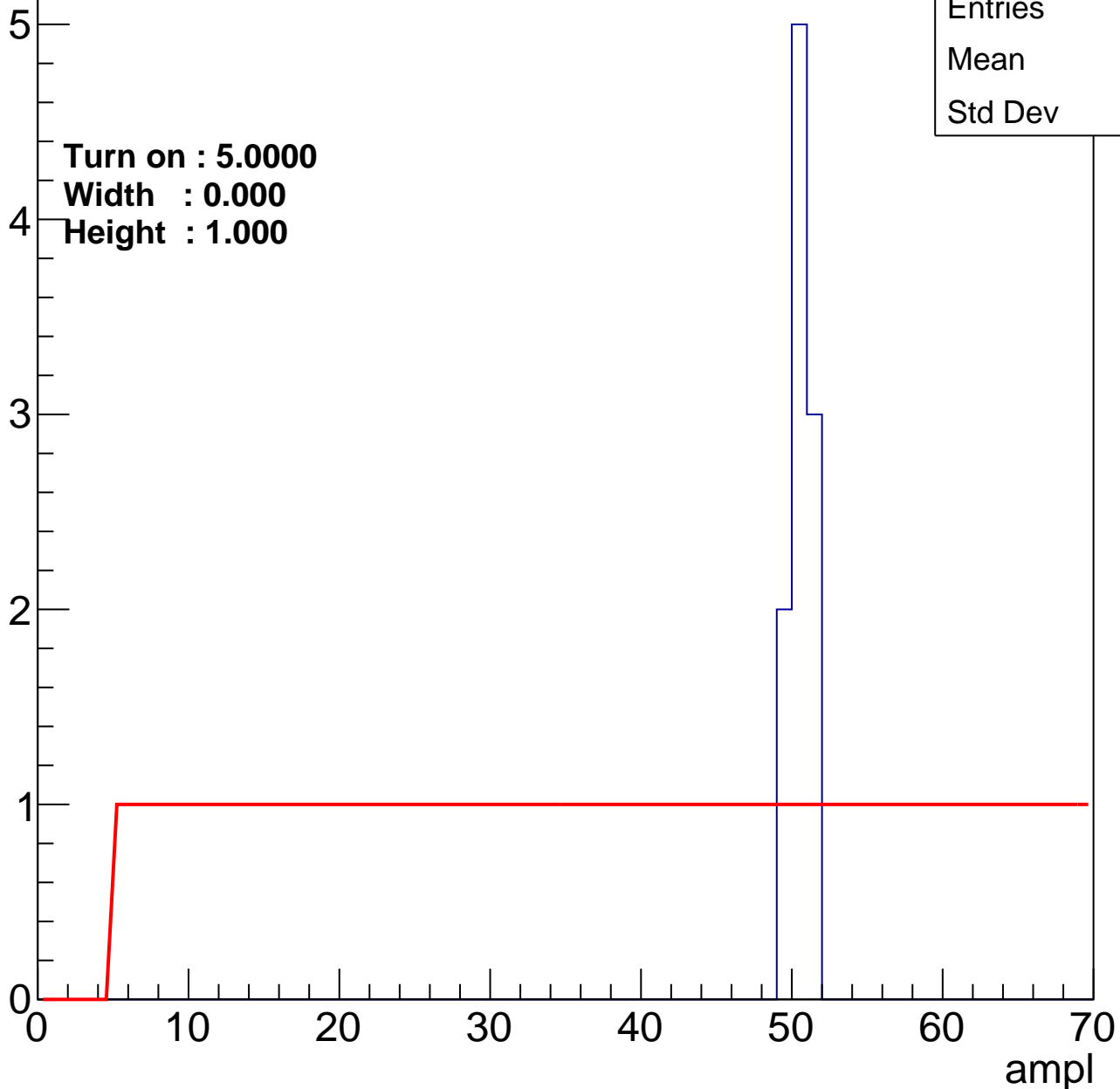
Entry

Entries	10
Mean	50.1
Std Dev	0.7

Turn on : 5.0000

Width : 0.000

Height : 1.000



# B0L100S, U12-ch22

calib\_packv5\_042523\_0143.root, FC#6, port A1

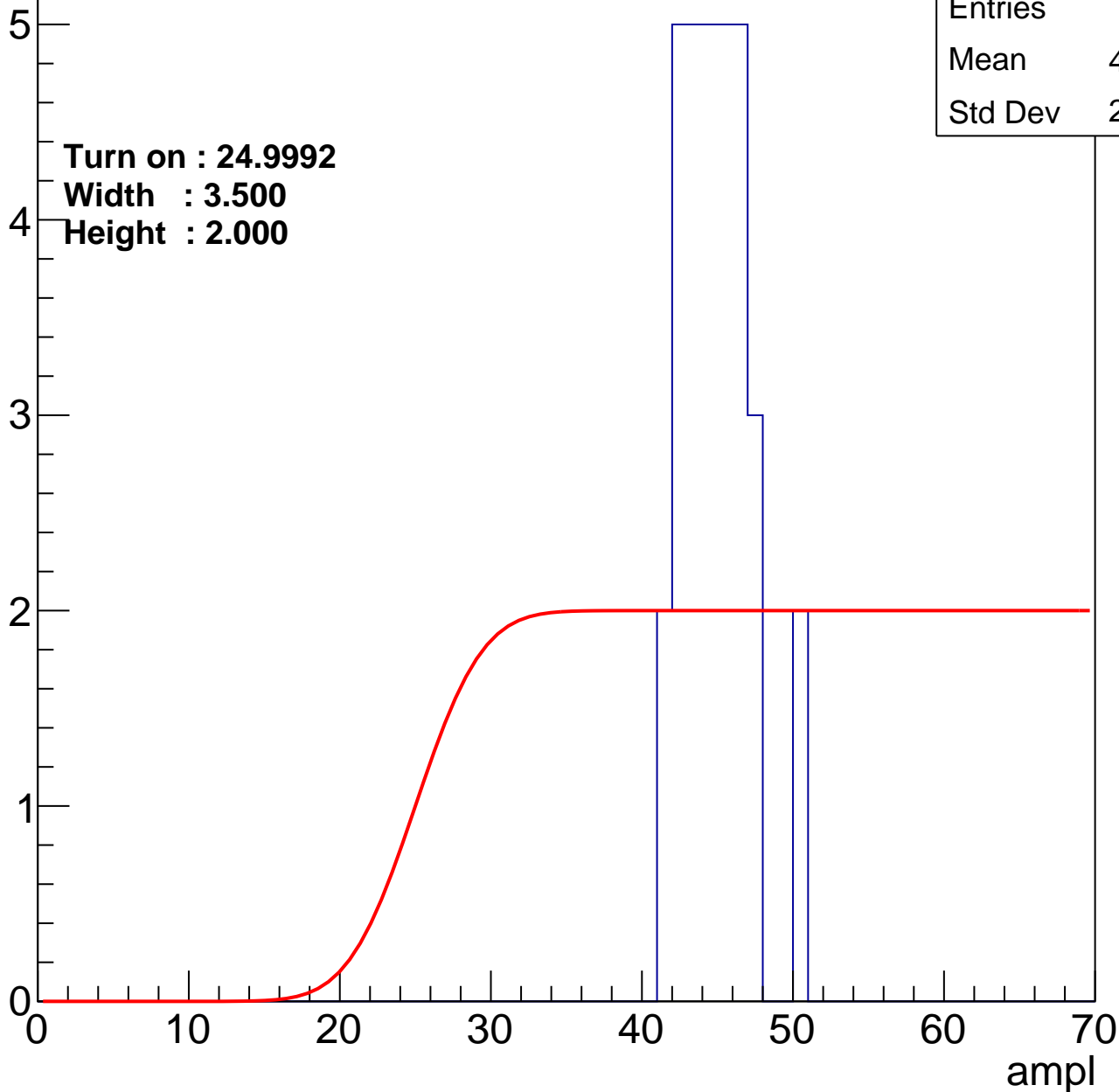
Entry

Entries	32
Mean	44.47
Std Dev	2.236

Turn on : 24.9992

Width : 3.500

Height : 2.000





# B0L100S, U12-ch23

calib\_packv5\_042523\_0143.root, FC#6, port A1

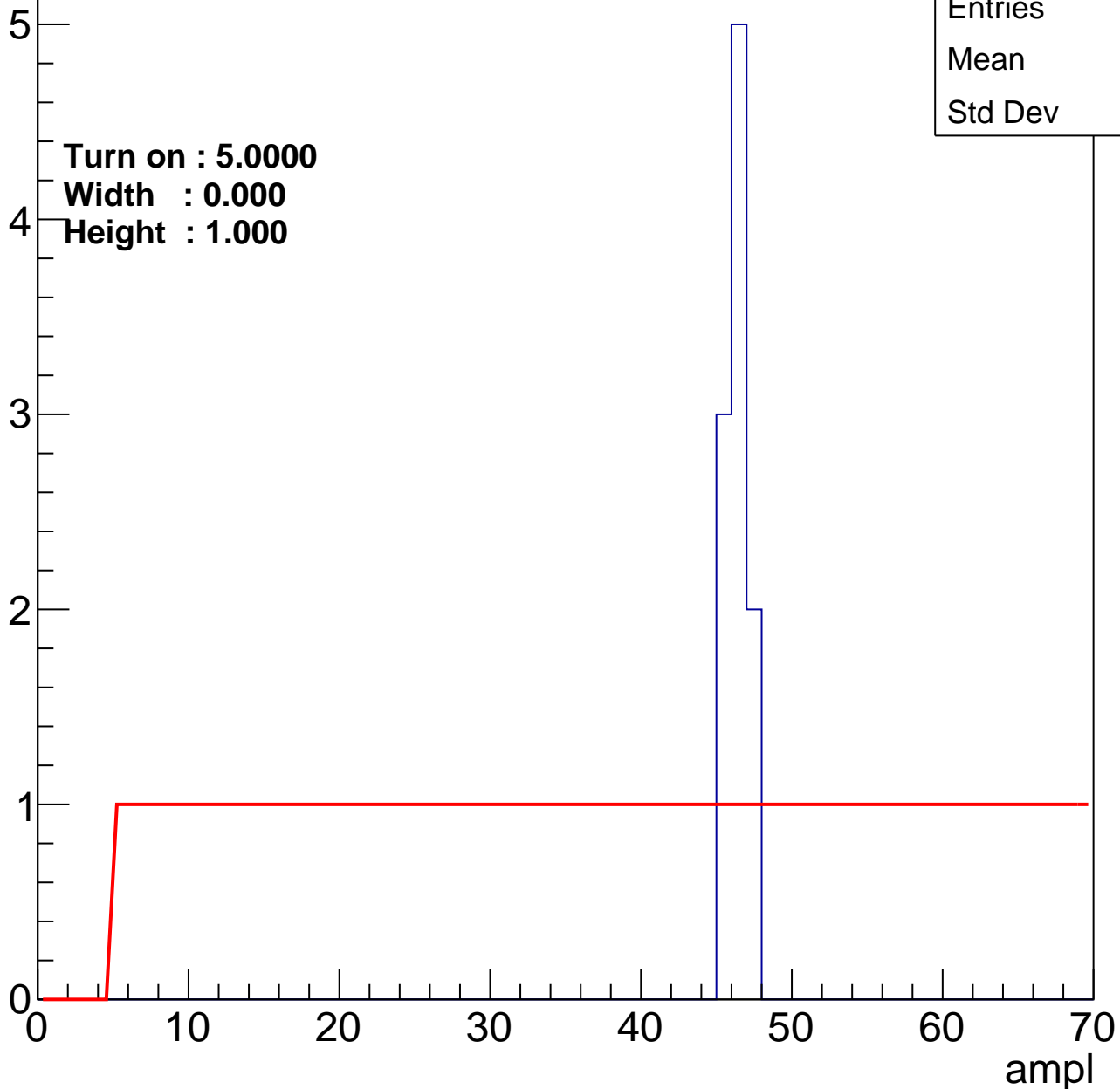
Entry

Entries	10
Mean	45.9
Std Dev	0.7

Turn on : 5.0000

Width : 0.000

Height : 1.000



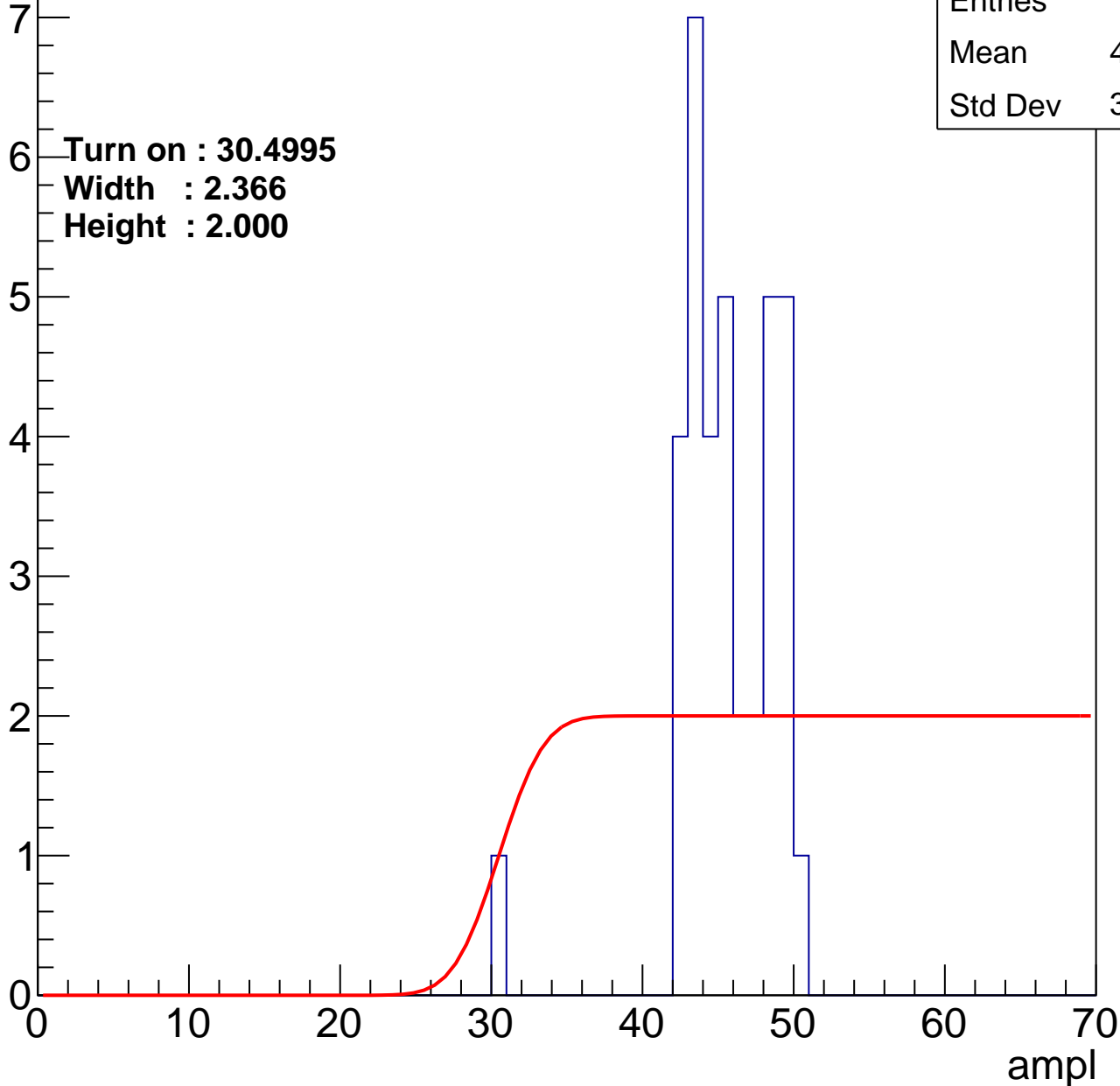
# B0L100S, U12-ch24

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

Entries	36
Mean	45.03
Std Dev	3.547

Turn on : 30.4995  
Width : 2.366  
Height : 2.000



# B0L100S, U12-ch25

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U12-ch26

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U12-ch27

calib\_packv5\_042523\_0143.root, FC#6, port A1

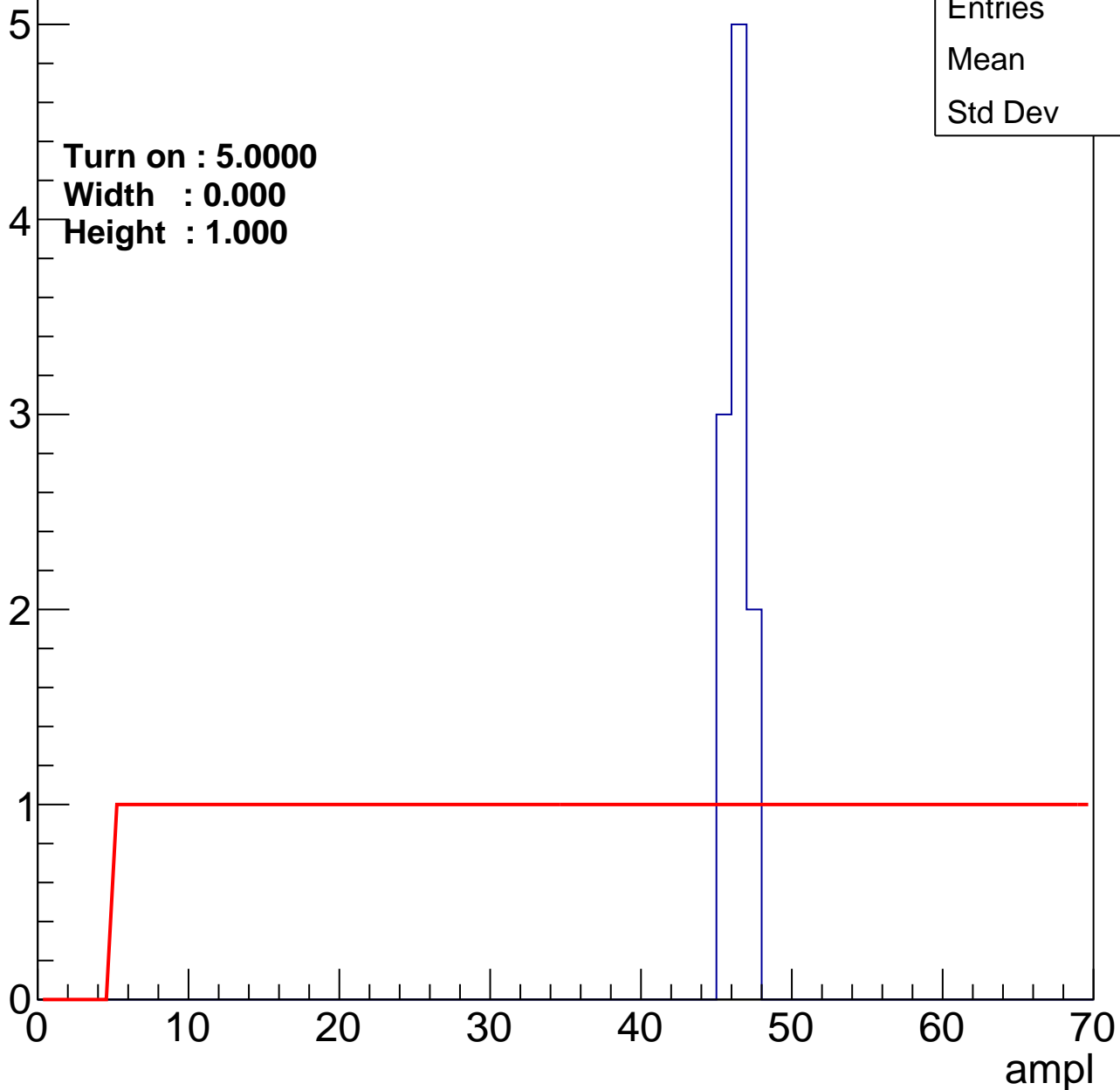
Entry

Entries	10
Mean	45.9
Std Dev	0.7

Turn on : 5.0000

Width : 0.000

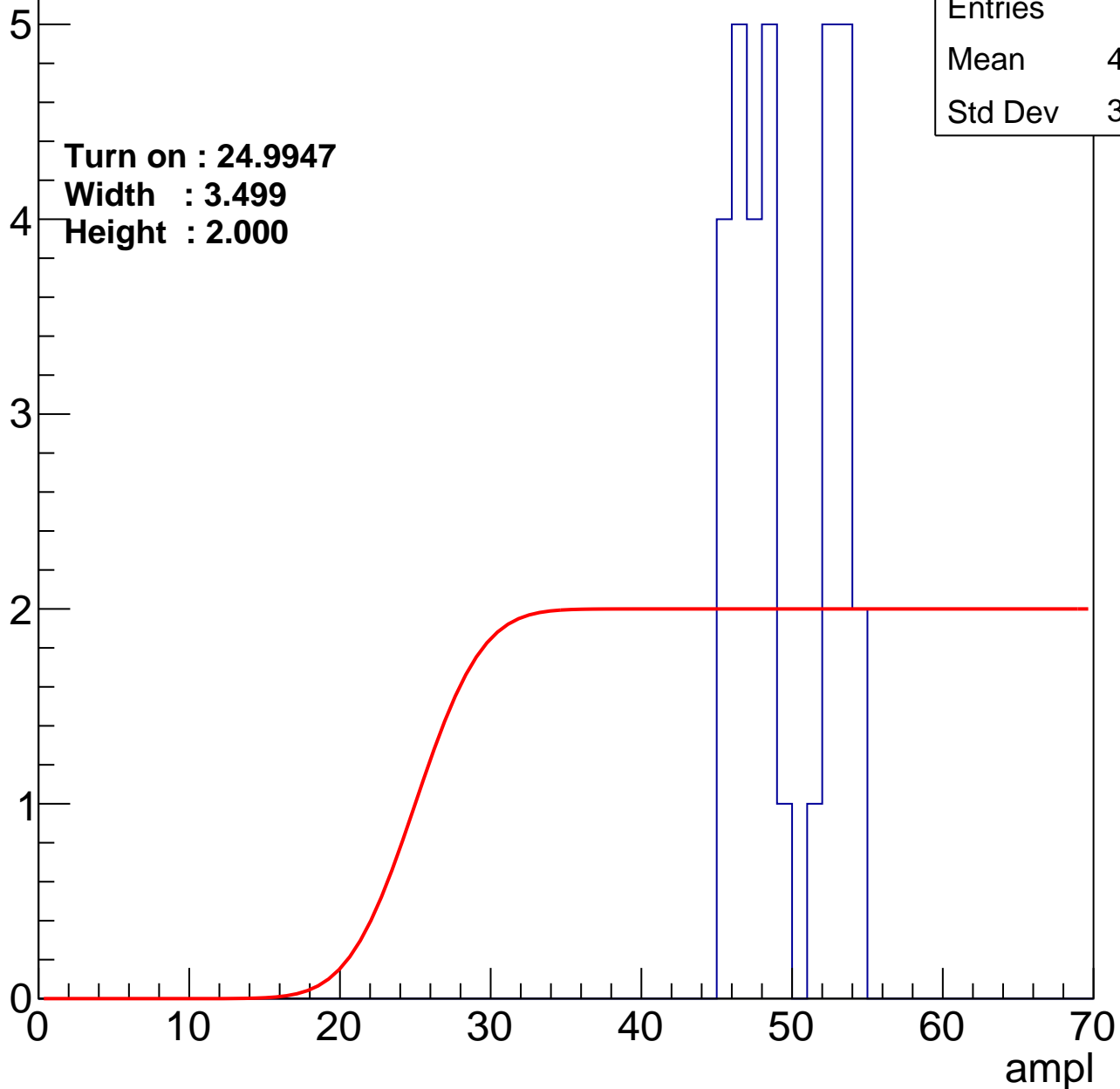
Height : 1.000



# B0L100S, U12-ch28

calib\_packv5\_042523\_0143.root, FC#6, port A1

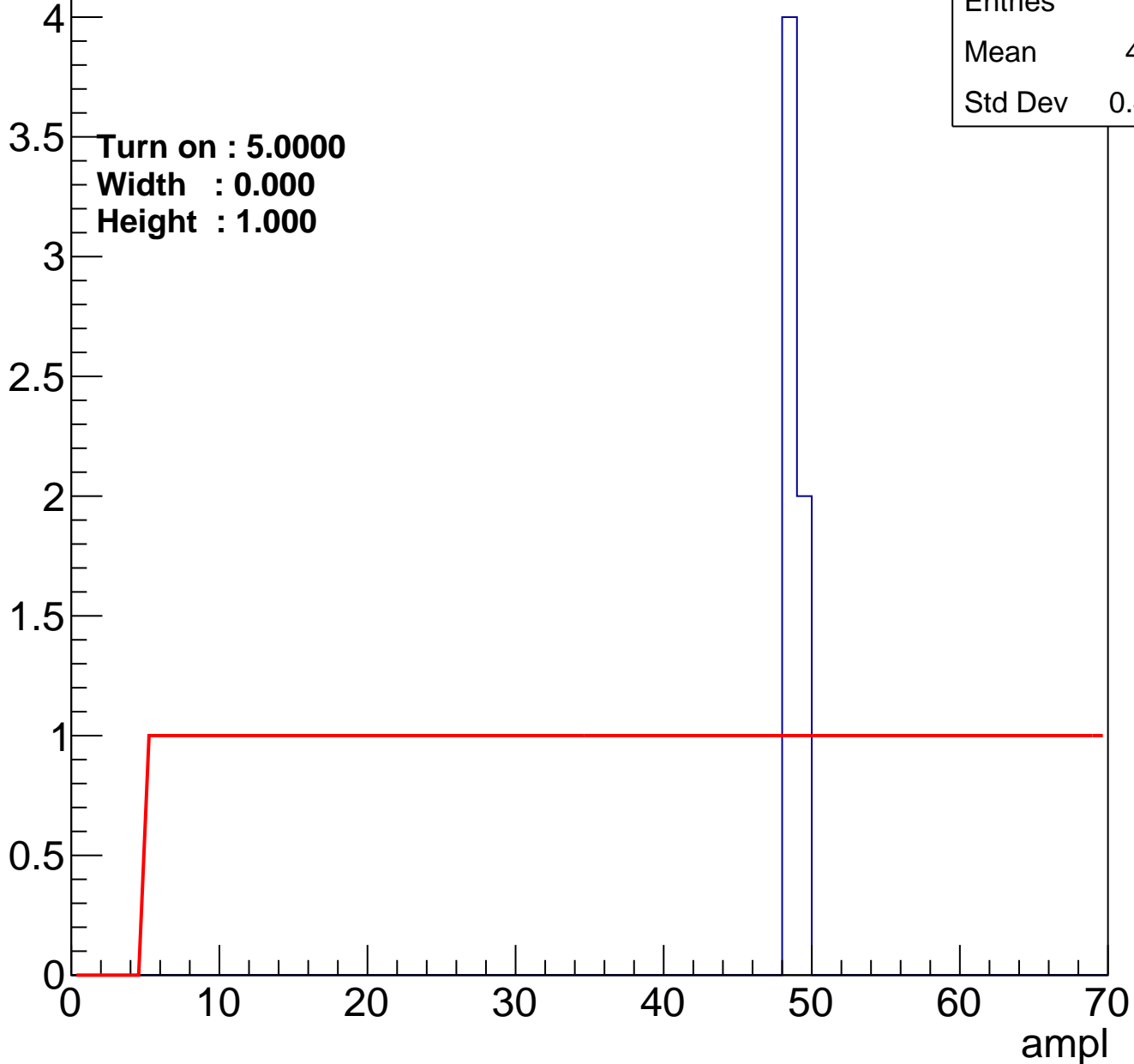
Entry



# B0L100S, U12-ch29

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	6
Mean	48.33
Std Dev	0.4714

# B0L100S, U12-ch30

calib\_packv5\_042523\_0143.root, FC#6, port A1

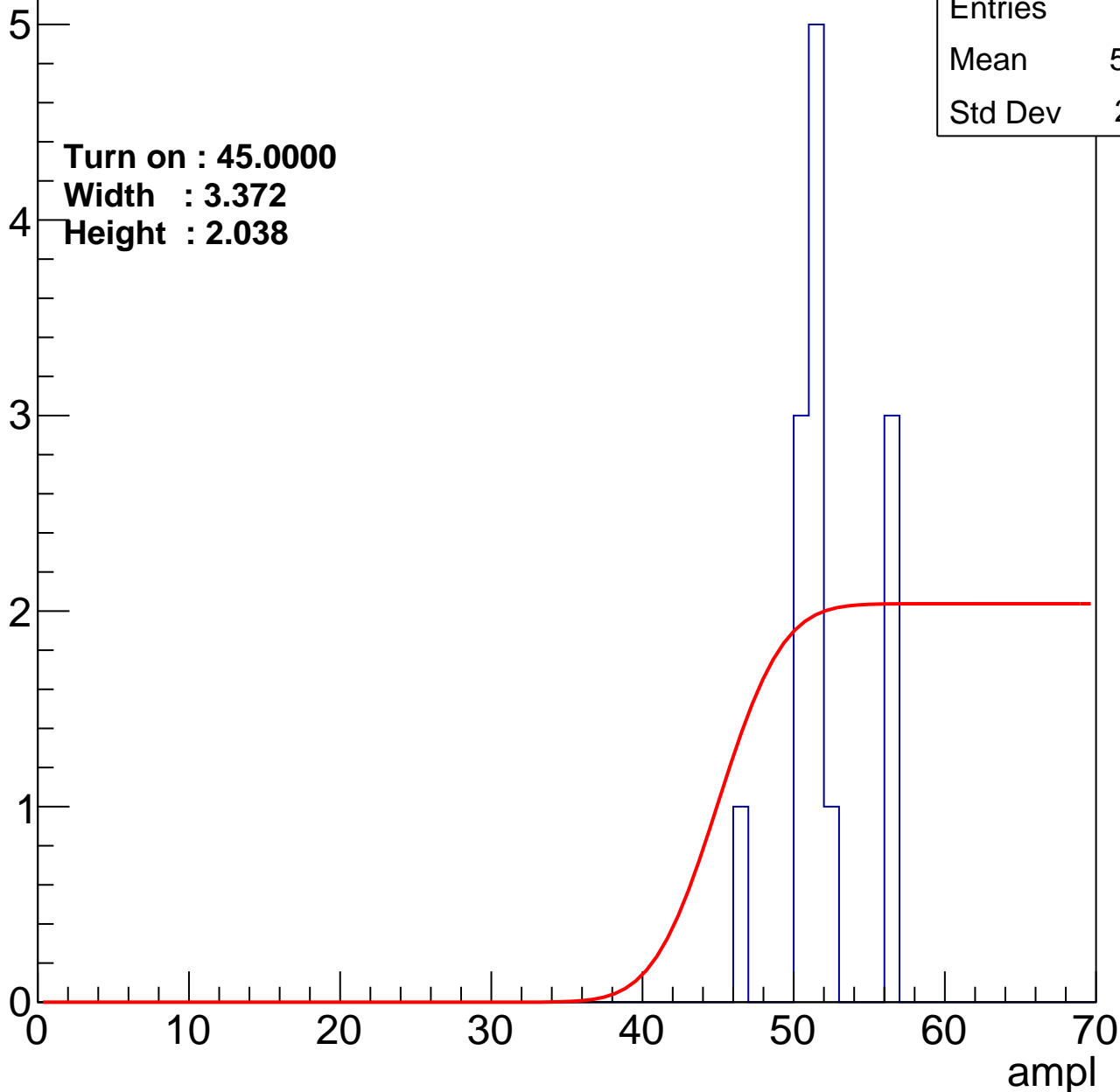
Entry

Entries	13
Mean	51.62
Std Dev	2.761

Turn on : 45.0000

Width : 3.372

Height : 2.038





# B0L100S, U12-ch31

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U12-ch32

calib\_packv5\_042523\_0143.root, FC#6, port A1

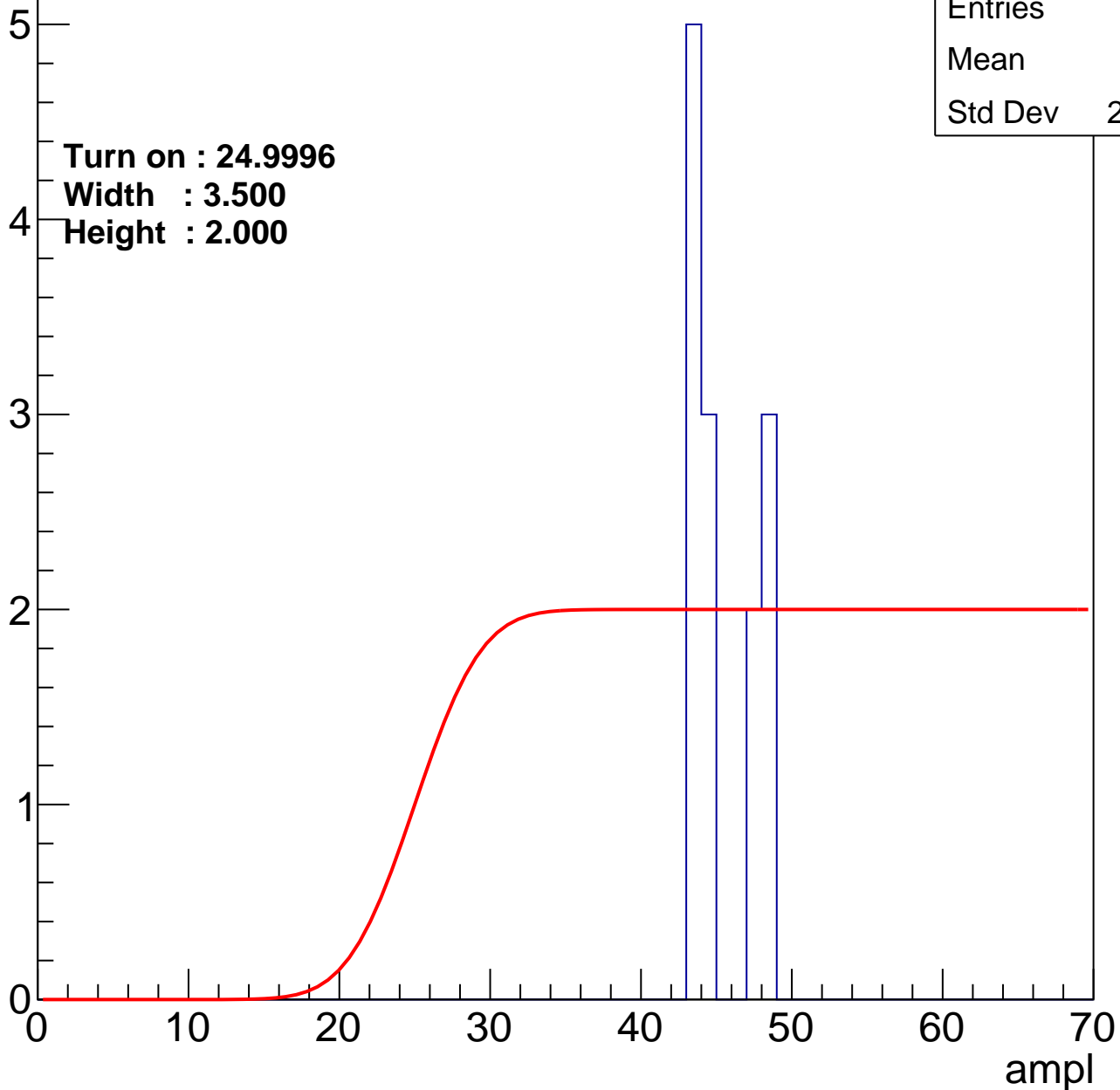
Entry

Entries	13
Mean	45
Std Dev	2.112

Turn on : 24.9996

Width : 3.500

Height : 2.000



# B0L100S, U12-ch33

calib\_packv5\_042523\_0143.root, FC#6, port A1

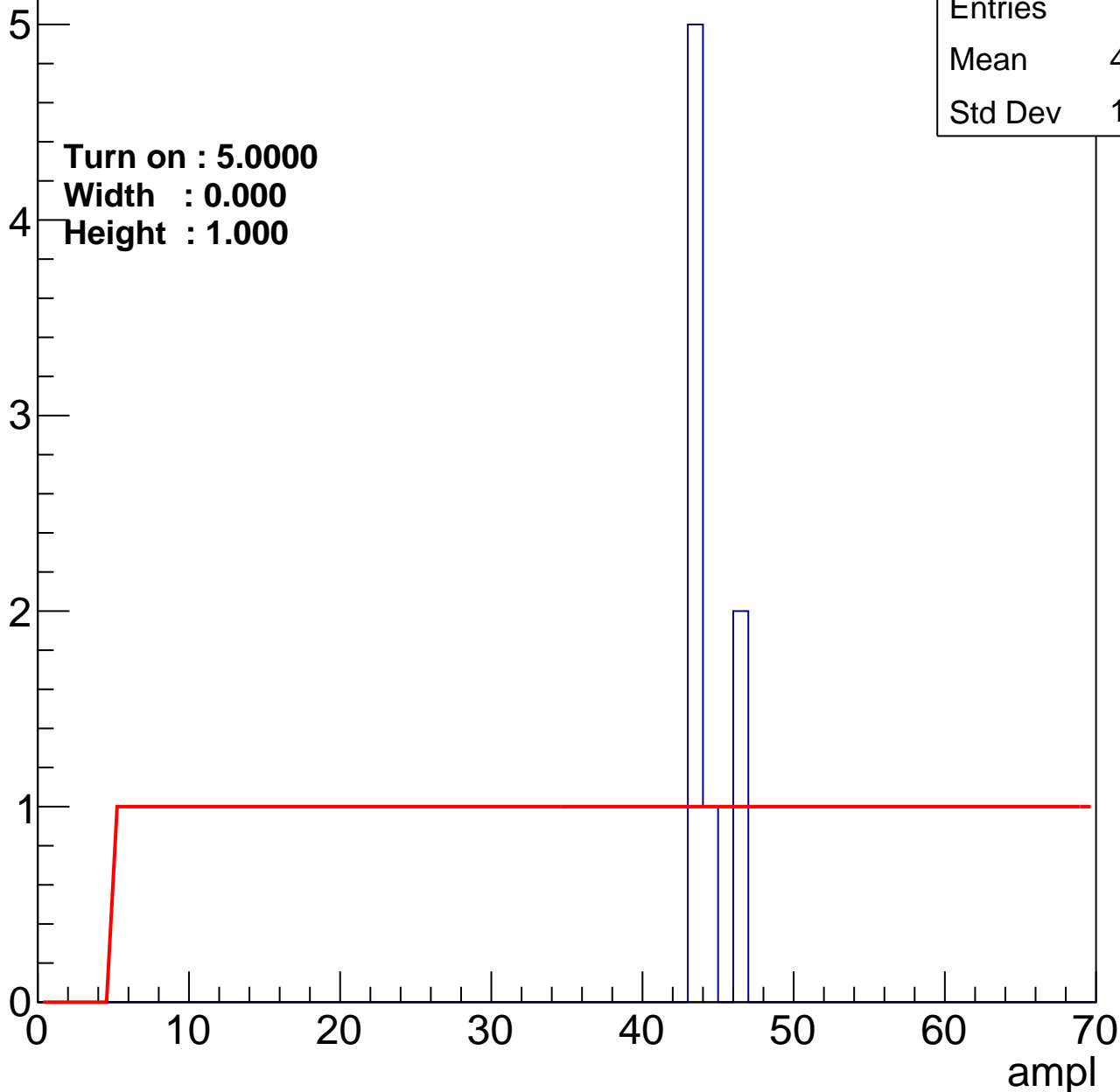
Entry

Entries	8
Mean	43.88
Std Dev	1.269

Turn on : 5.0000

Width : 0.000

Height : 1.000



# B0L100S, U12-ch34

calib\_packv5\_042523\_0143.root, FC#6, port A1

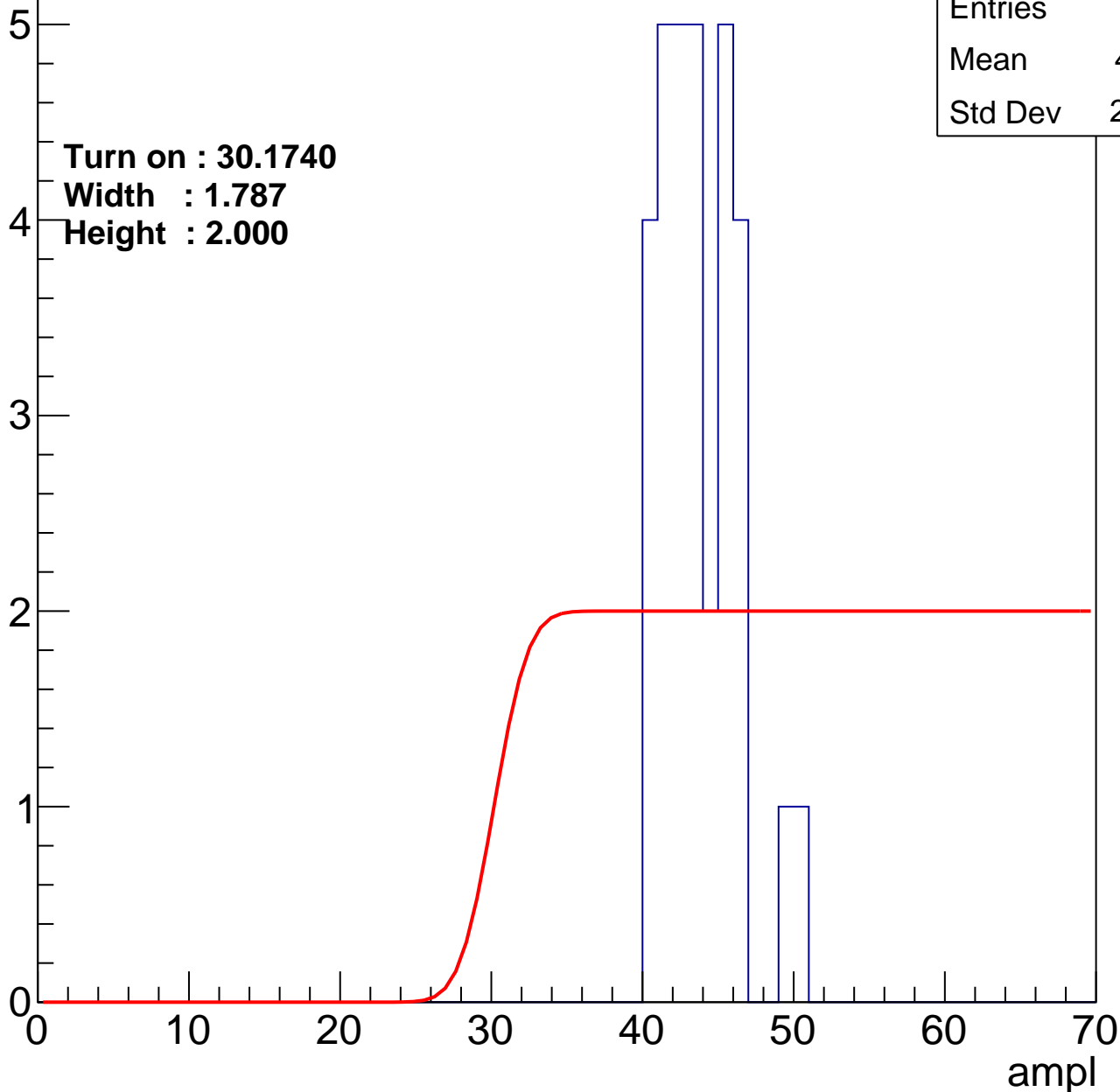
Entry

Entries	32
Mean	43.31
Std Dev	2.505

Turn on : 30.1740

Width : 1.787

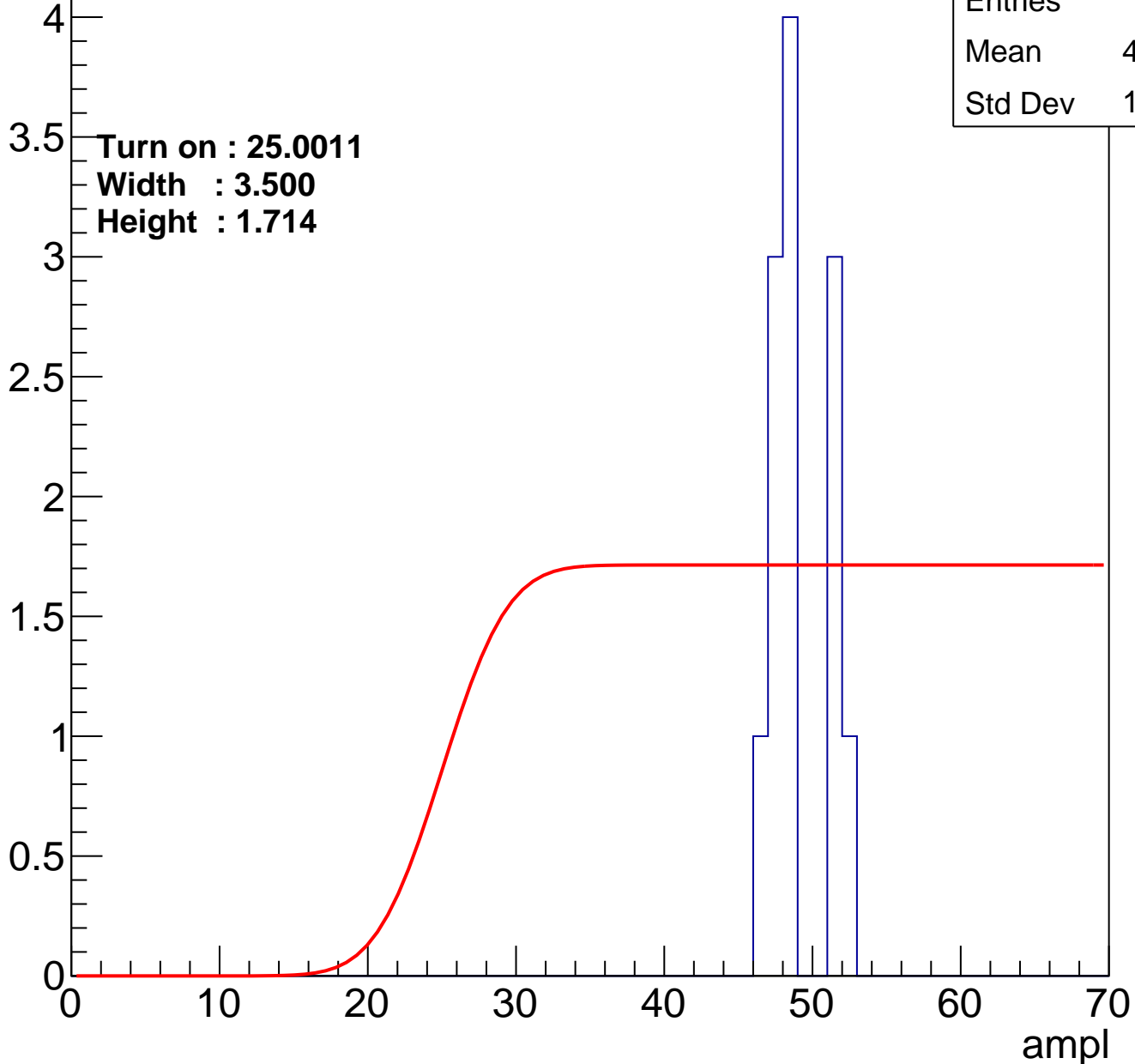
Height : 2.000



# B0L100S, U12-ch35

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	12
Mean	48.67
Std Dev	1.929

# B0L100S, U12-ch36

calib\_packv5\_042523\_0143.root, FC#6, port A1

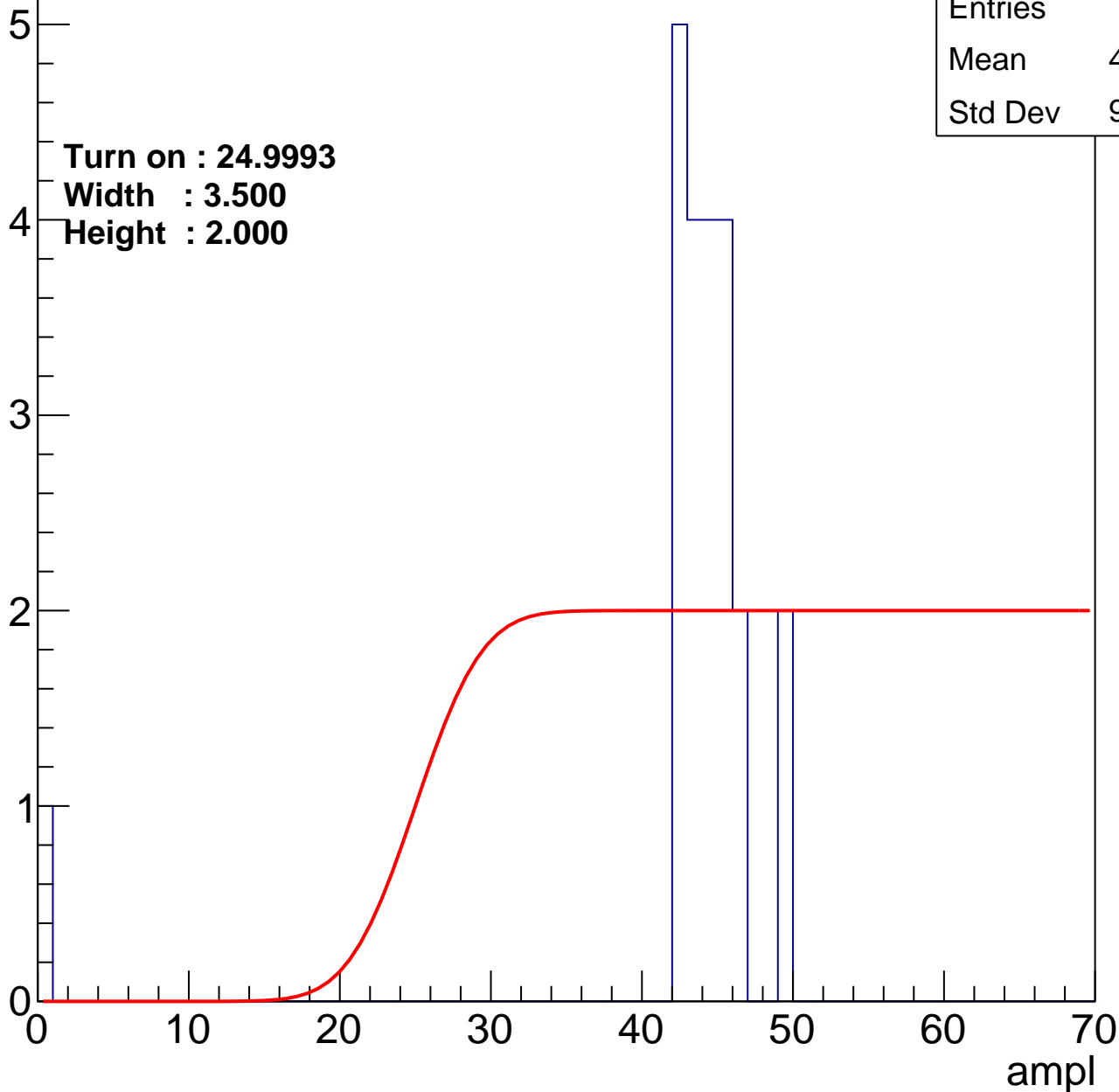
Entry

Entries	22
Mean	42.18
Std Dev	9.413

Turn on : 24.9993

Width : 3.500

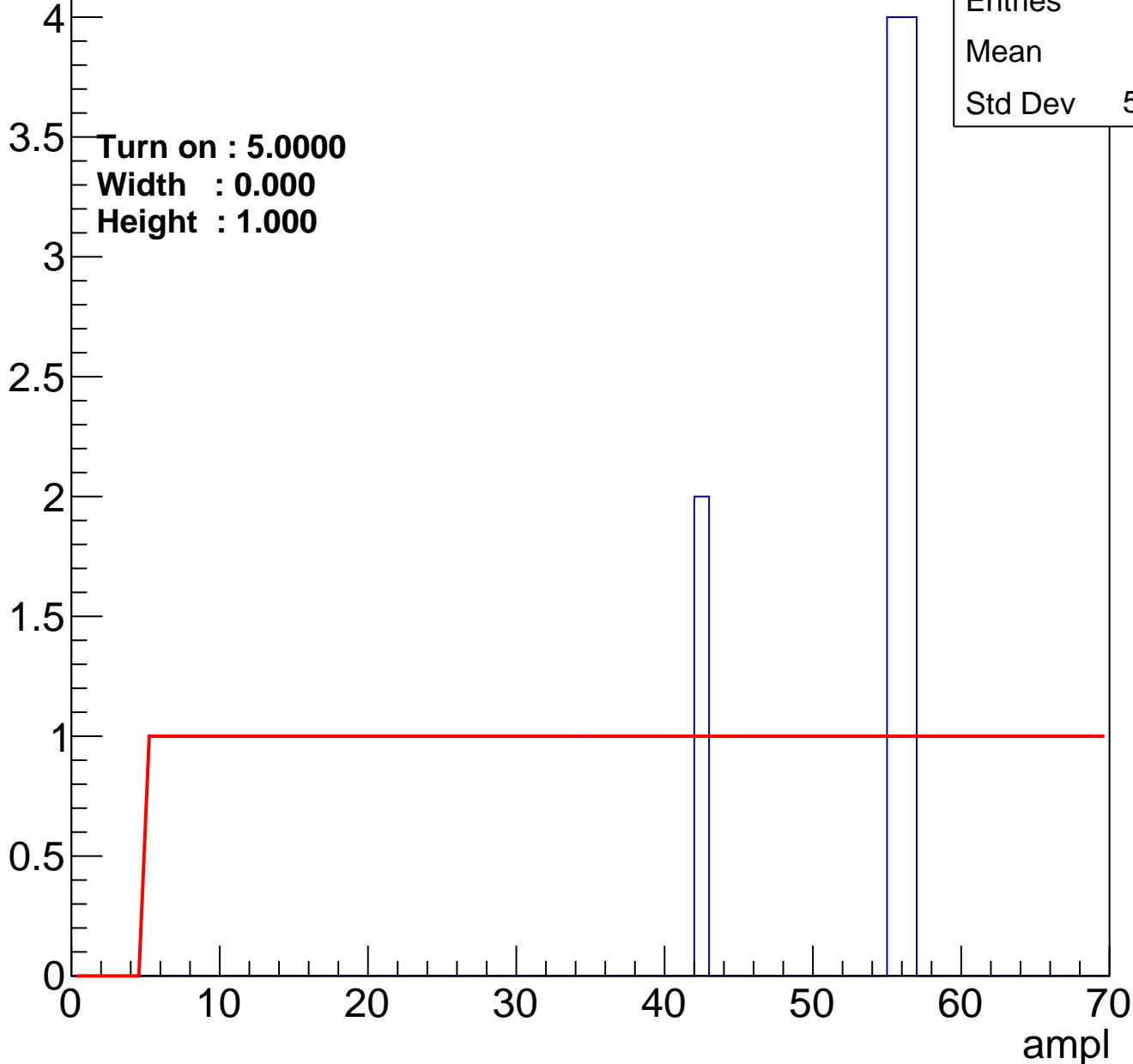
Height : 2.000



# B0L100S, U12-ch37

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U12-ch38

calib\_packv5\_042523\_0143.root, FC#6, port A1

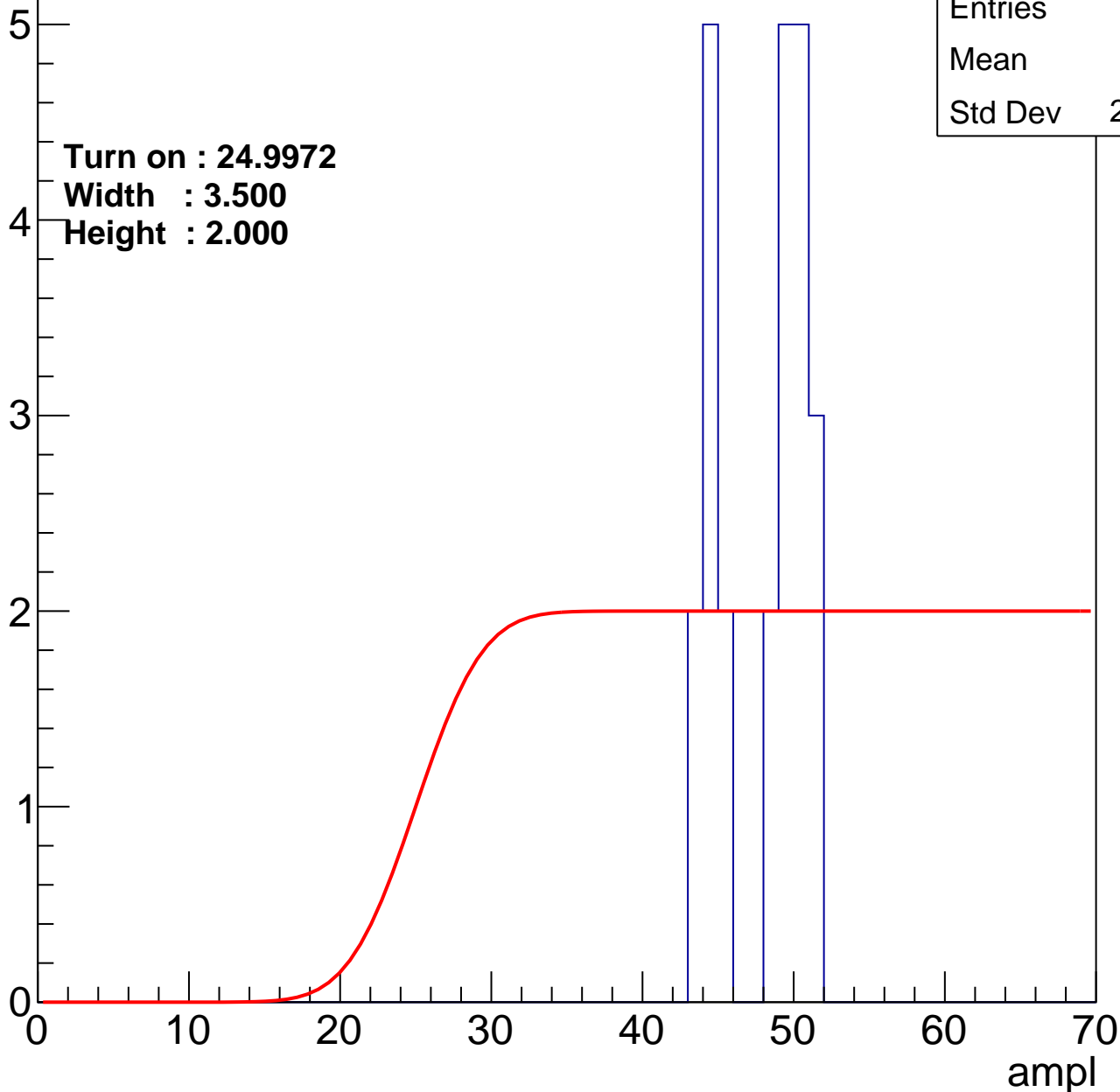
Entry

Entries	24
Mean	47.5
Std Dev	2.843

Turn on : 24.9972

Width : 3.500

Height : 2.000





# B0L100S, U12-ch39

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U12-ch40

calib\_packv5\_042523\_0143.root, FC#6, port A1

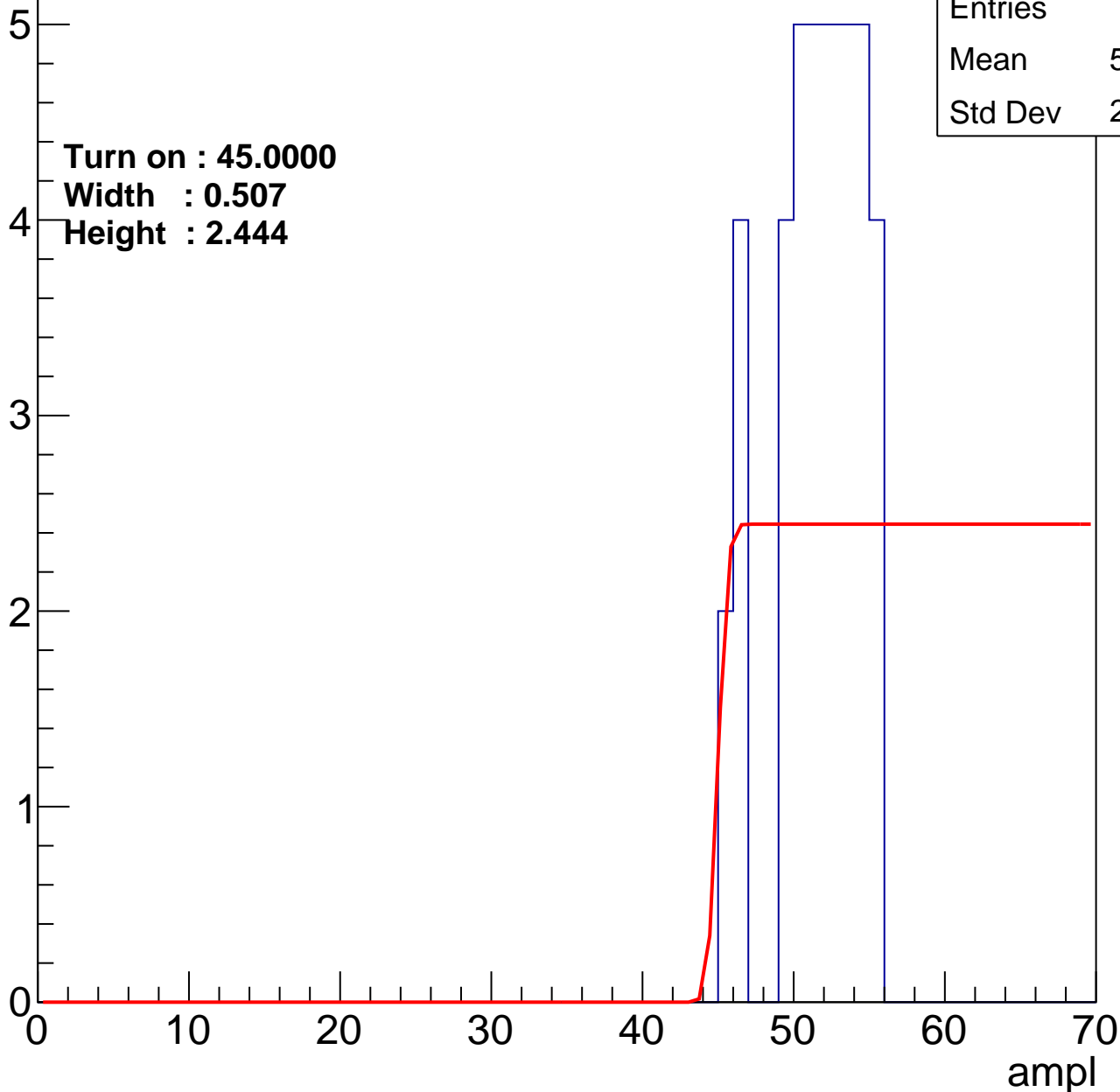
Entry

Entries	39
Mean	51.03
Std Dev	2.896

Turn on : 45.0000

Width : 0.507

Height : 2.444



# B0L100S, U12-ch41

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U12-ch42

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U12-ch43

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U12-ch44

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U12-ch45

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U12-ch46

calib\_packv5\_042523\_0143.root, FC#6, port A1

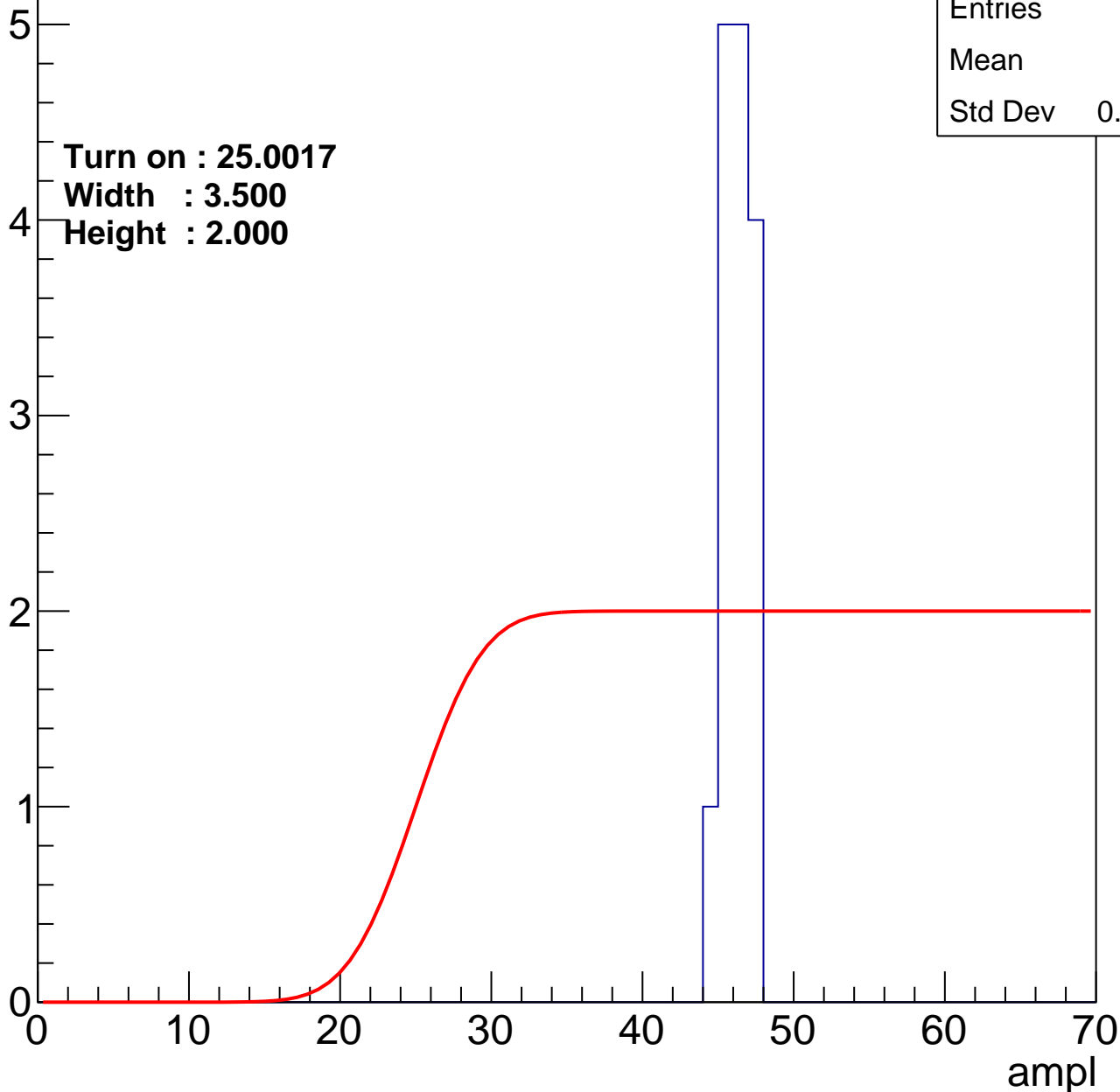
Entry

Entries	15
Mean	45.8
Std Dev	0.9092

Turn on : 25.0017

Width : 3.500

Height : 2.000





# B0L100S, U12-ch47

calib\_packv5\_042523\_0143.root, FC#6, port A1

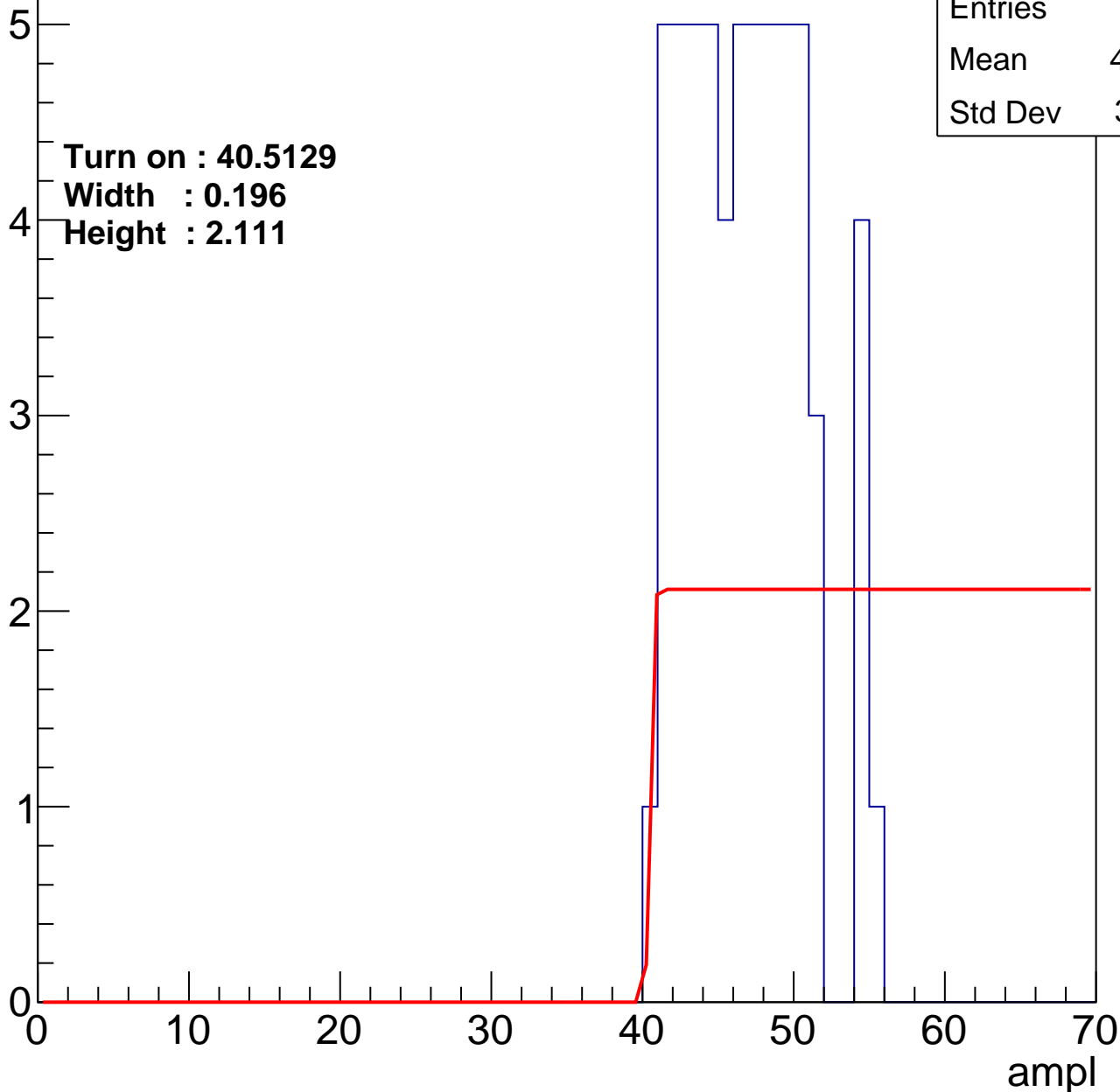
Entry

Entries	58
Mean	46.45
Std Dev	3.851

Turn on : 40.5129

Width : 0.196

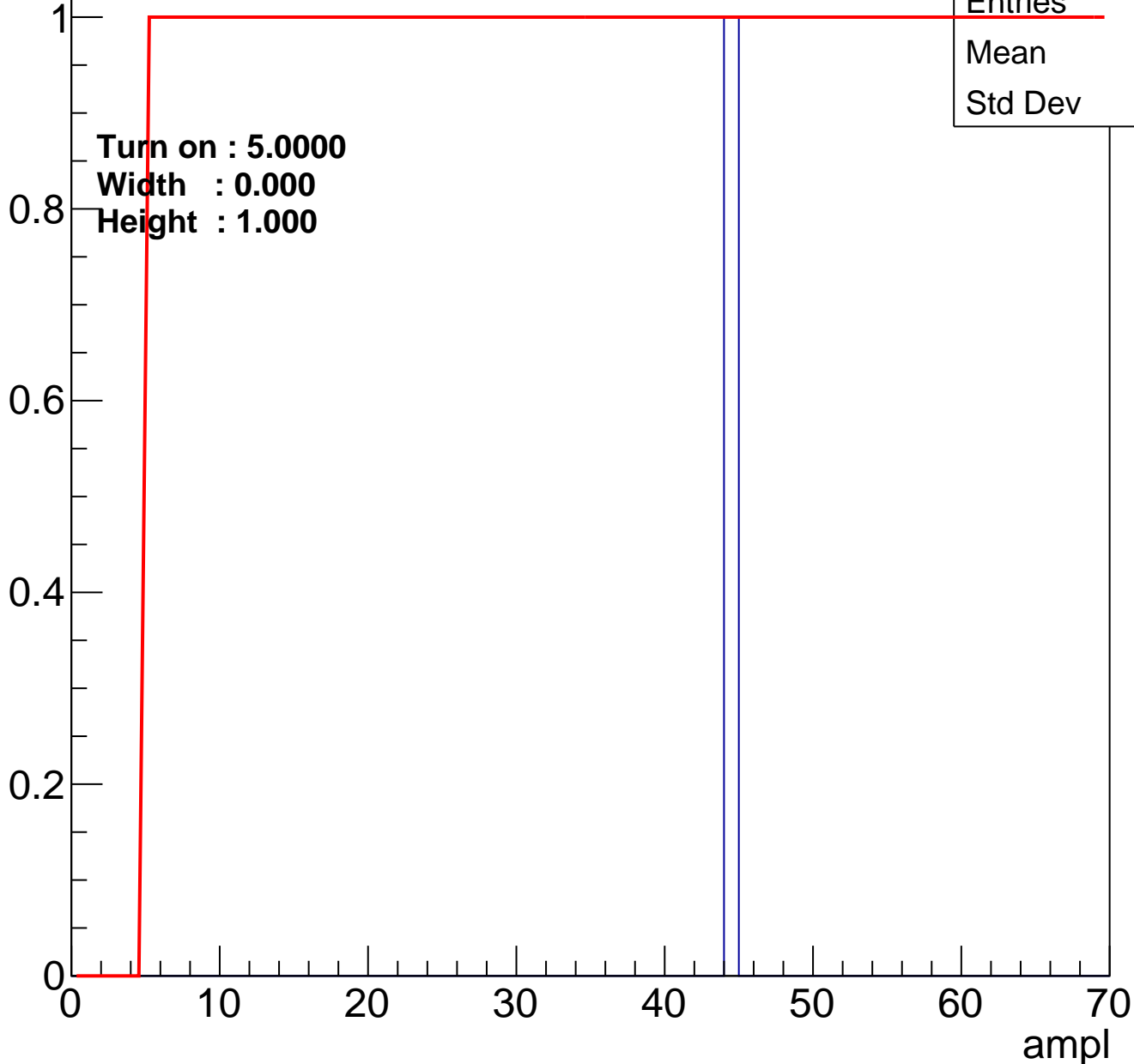
Height : 2.111



# B0L100S, U12-ch48

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U12-ch49

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

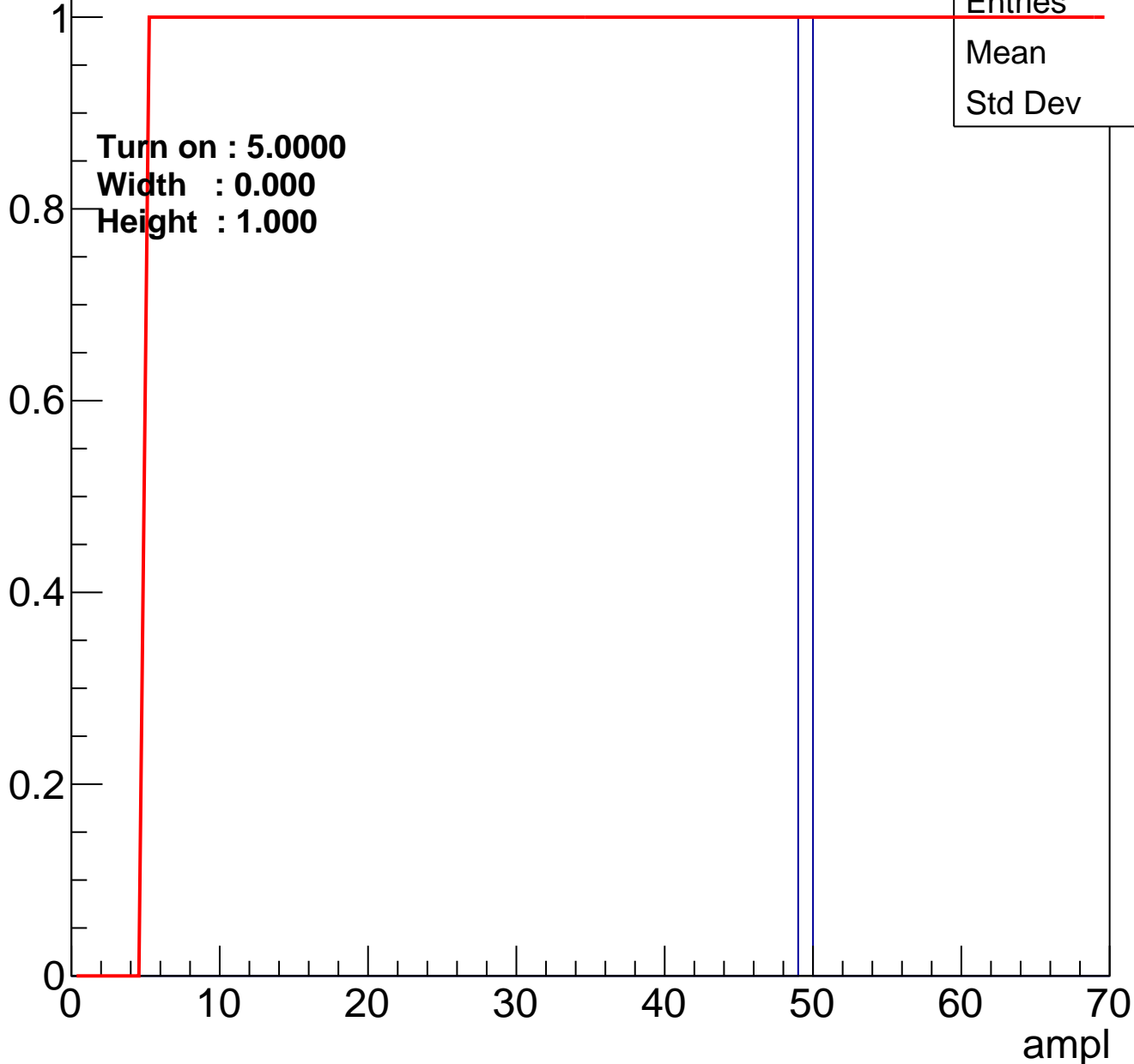


Entries	0
Mean	0
Std Dev	0

# B0L100S, U12-ch50

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U12-ch51

calib\_packv5\_042523\_0143.root, FC#6, port A1

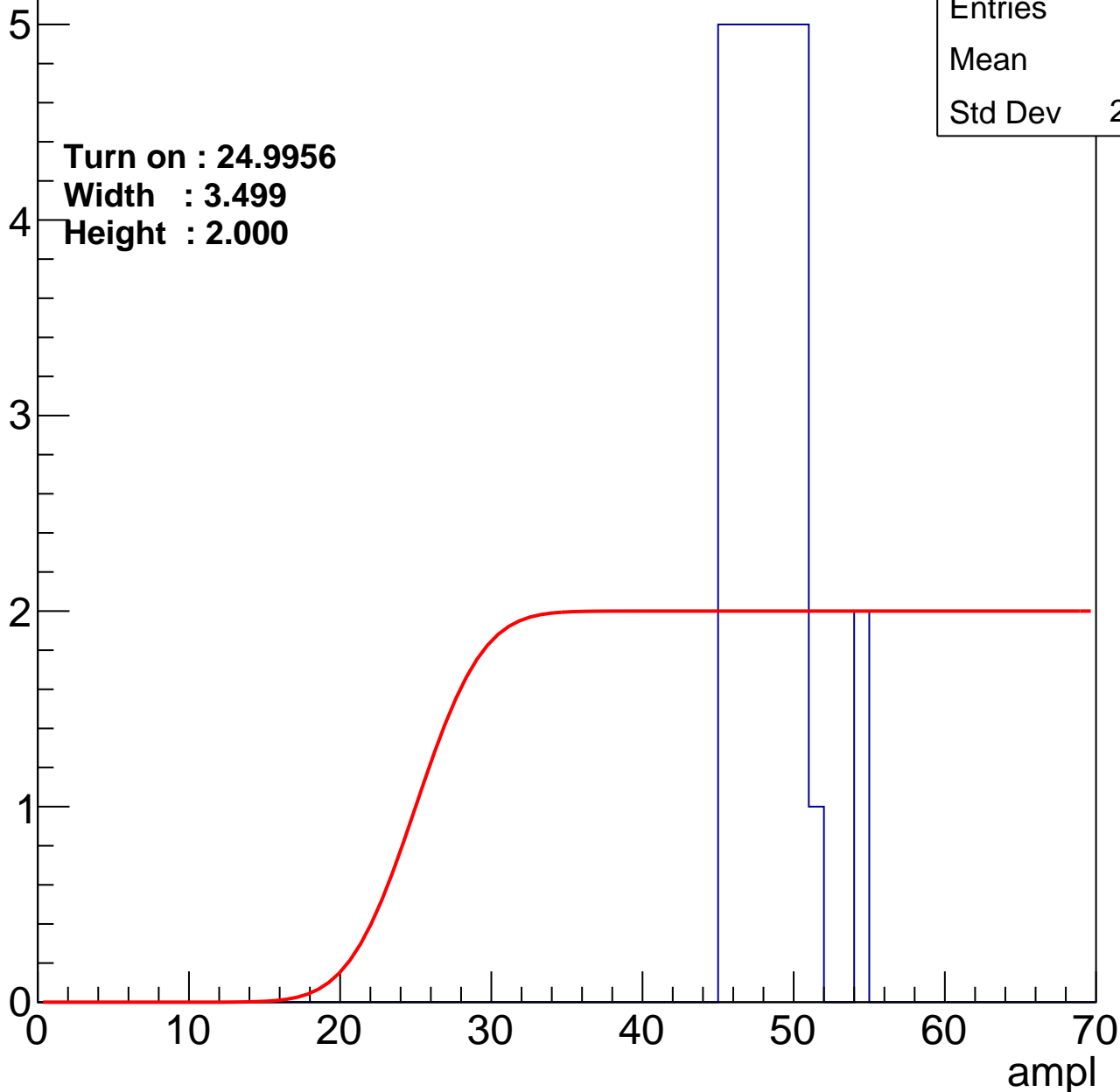
Entry

Entries	33
Mean	48
Std Dev	2.309

Turn on : 24.9956

Width : 3.499

Height : 2.000



# B0L100S, U12-ch52

calib\_packv5\_042523\_0143.root, FC#6, port A1

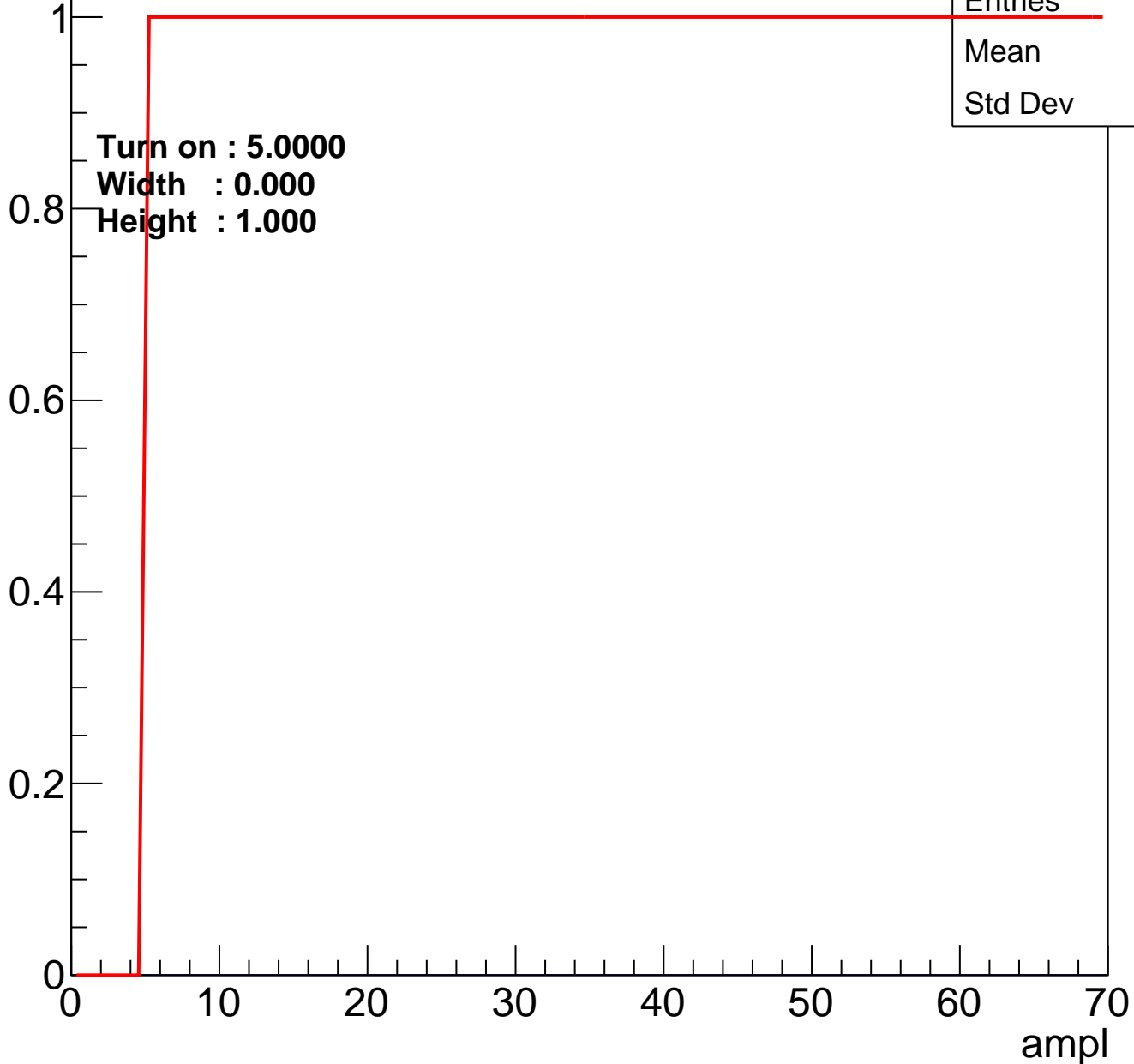
Entry



# B0L100S, U12-ch53

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U12-ch54

calib\_packv5\_042523\_0143.root, FC#6, port A1

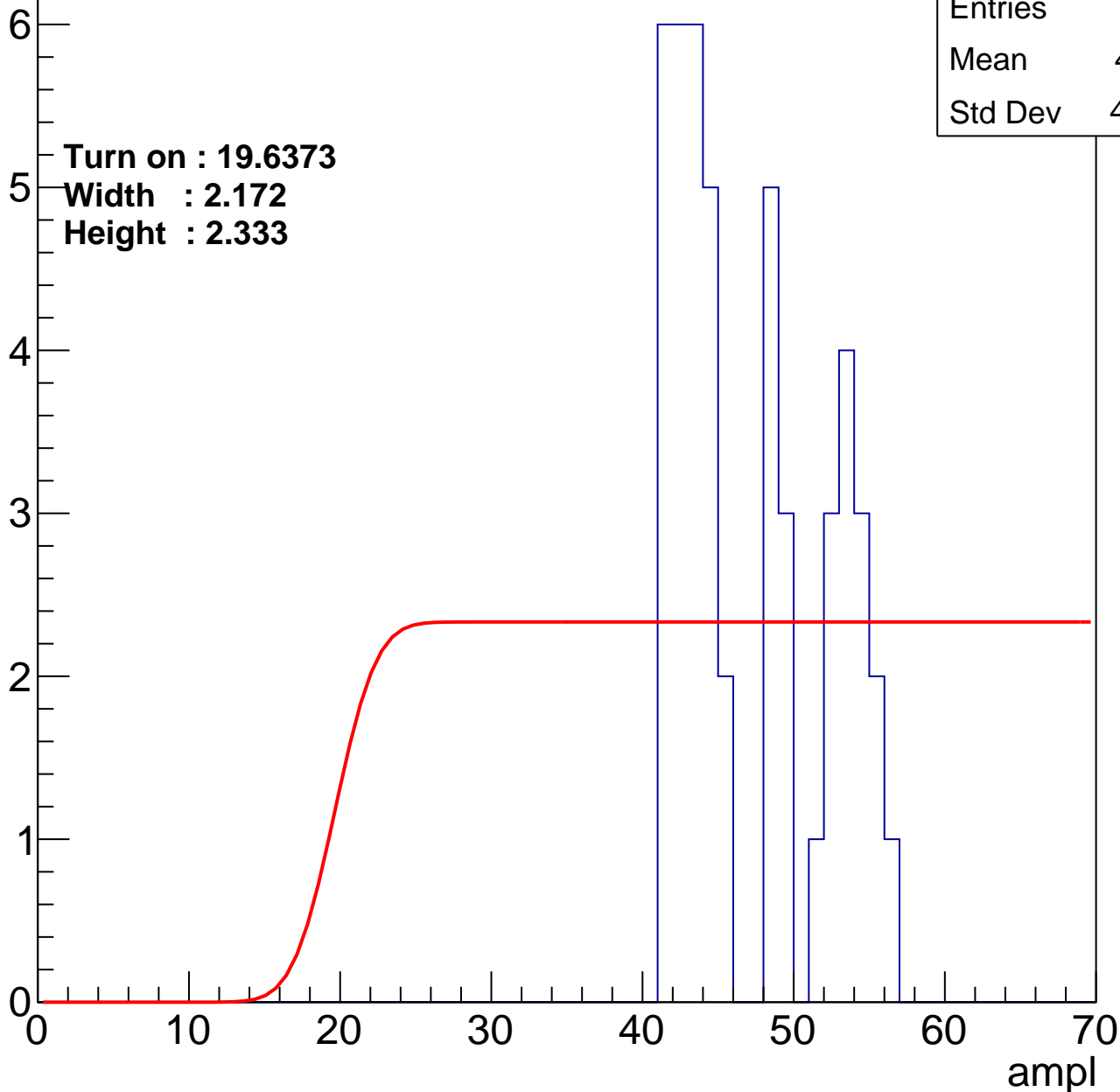
Entry

Entries	47
Mean	46.81
Std Dev	4.884

Turn on : 19.6373

Width : 2.172

Height : 2.333

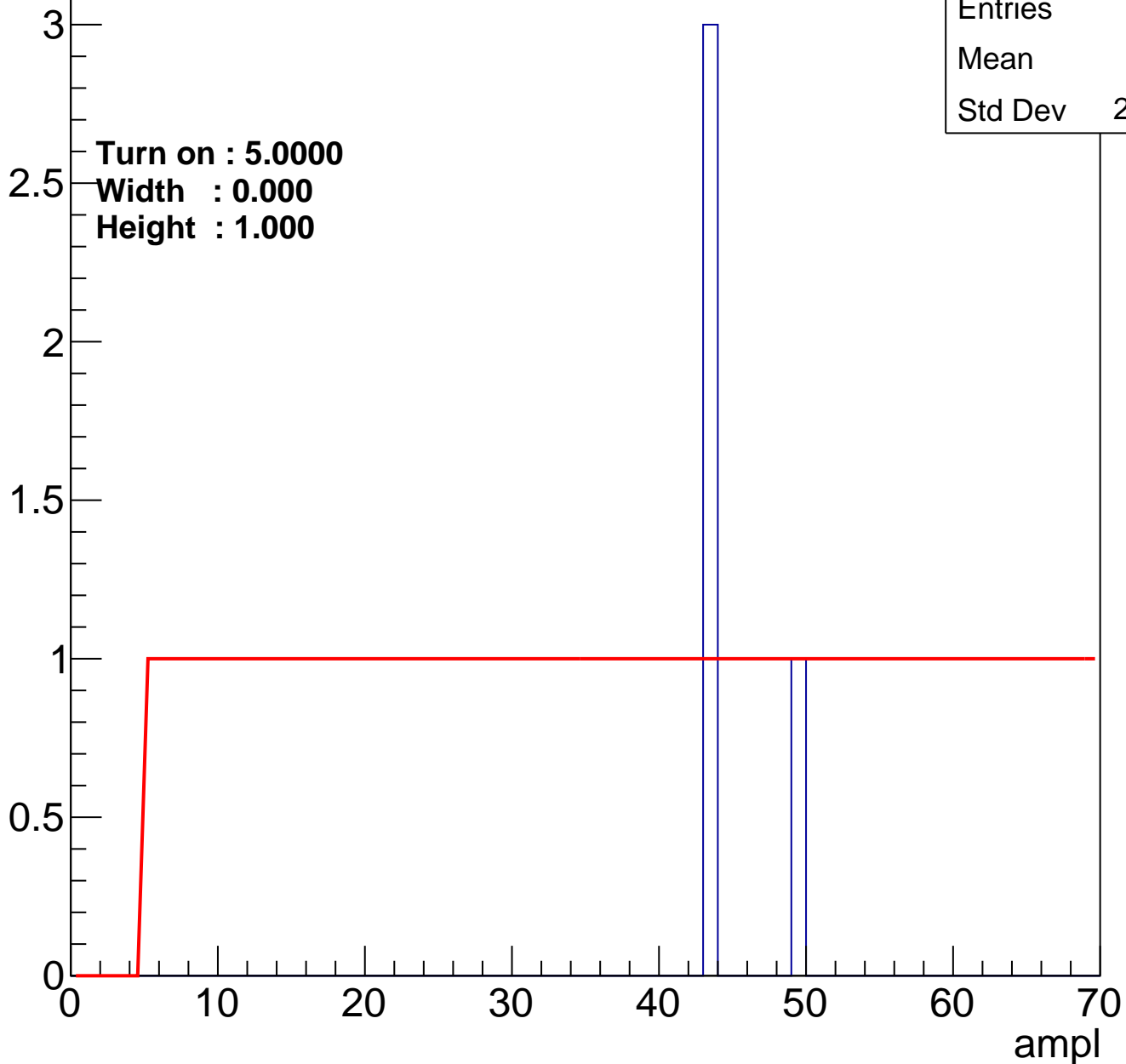




# B0L100S, U12-ch55

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U12-ch56

calib\_packv5\_042523\_0143.root, FC#6, port A1

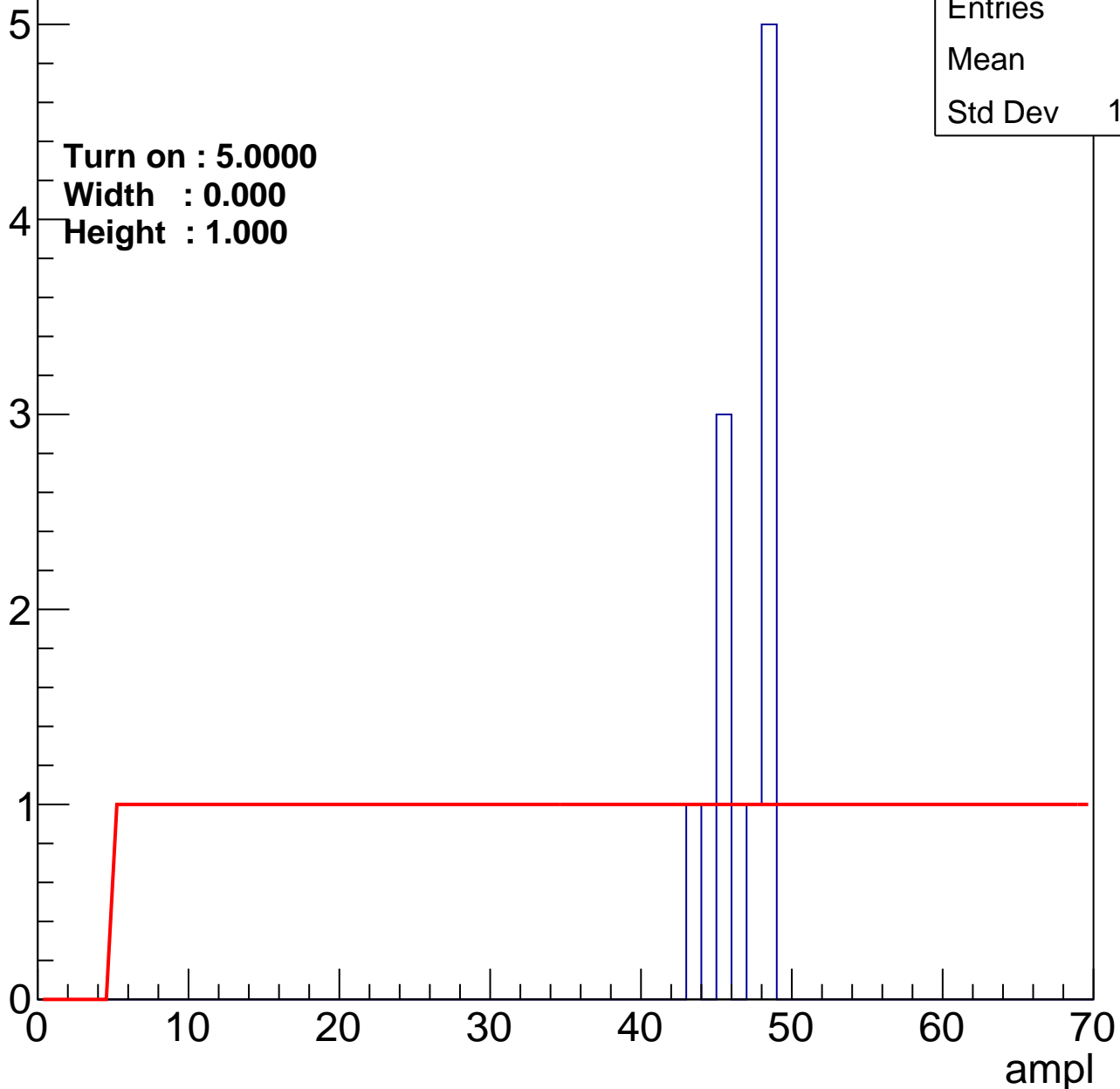
Entry

Entries	10
Mean	46.5
Std Dev	1.746

Turn on : 5.0000

Width : 0.000

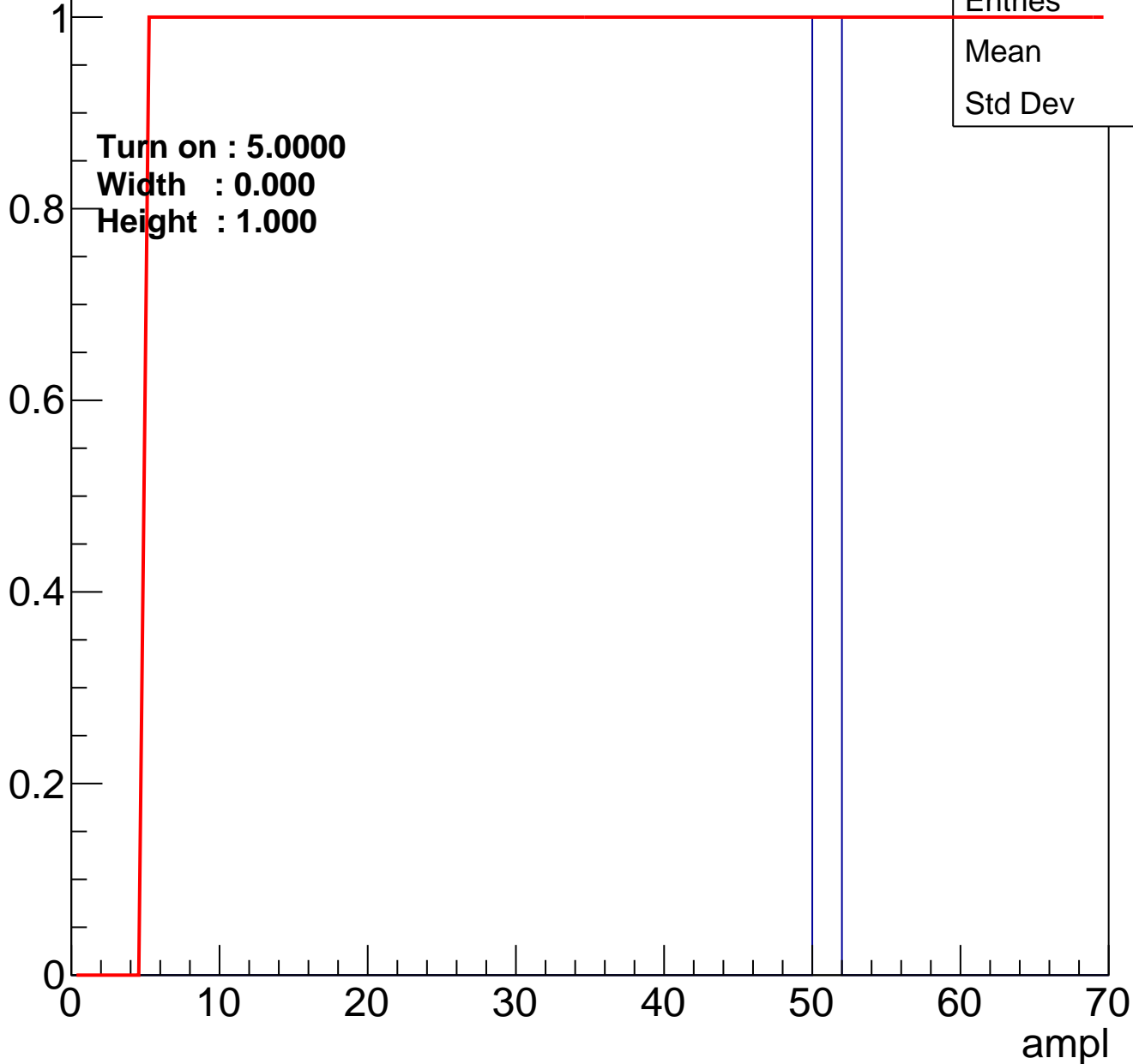
Height : 1.000



# B0L100S, U12-ch57

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U12-ch58

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

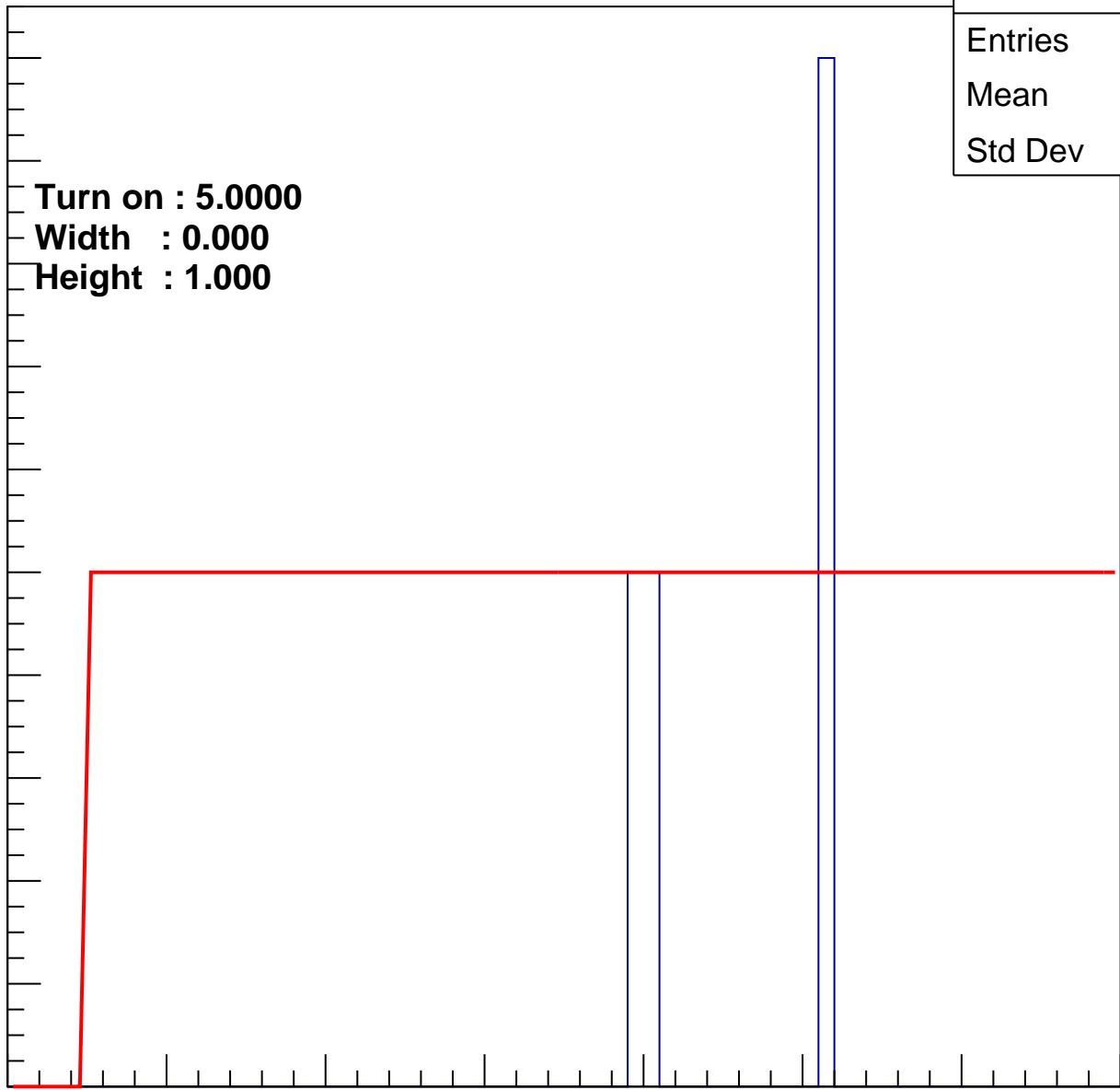
2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Turn on : 5.0000  
Width : 0.000  
Height : 1.000

Entries	4
Mean	45.25
Std Dev	5.761

0 10 20 30 40 50 60 70

ampl



# B0L100S, U12-ch59

calib\_packv5\_042523\_0143.root, FC#6, port A1

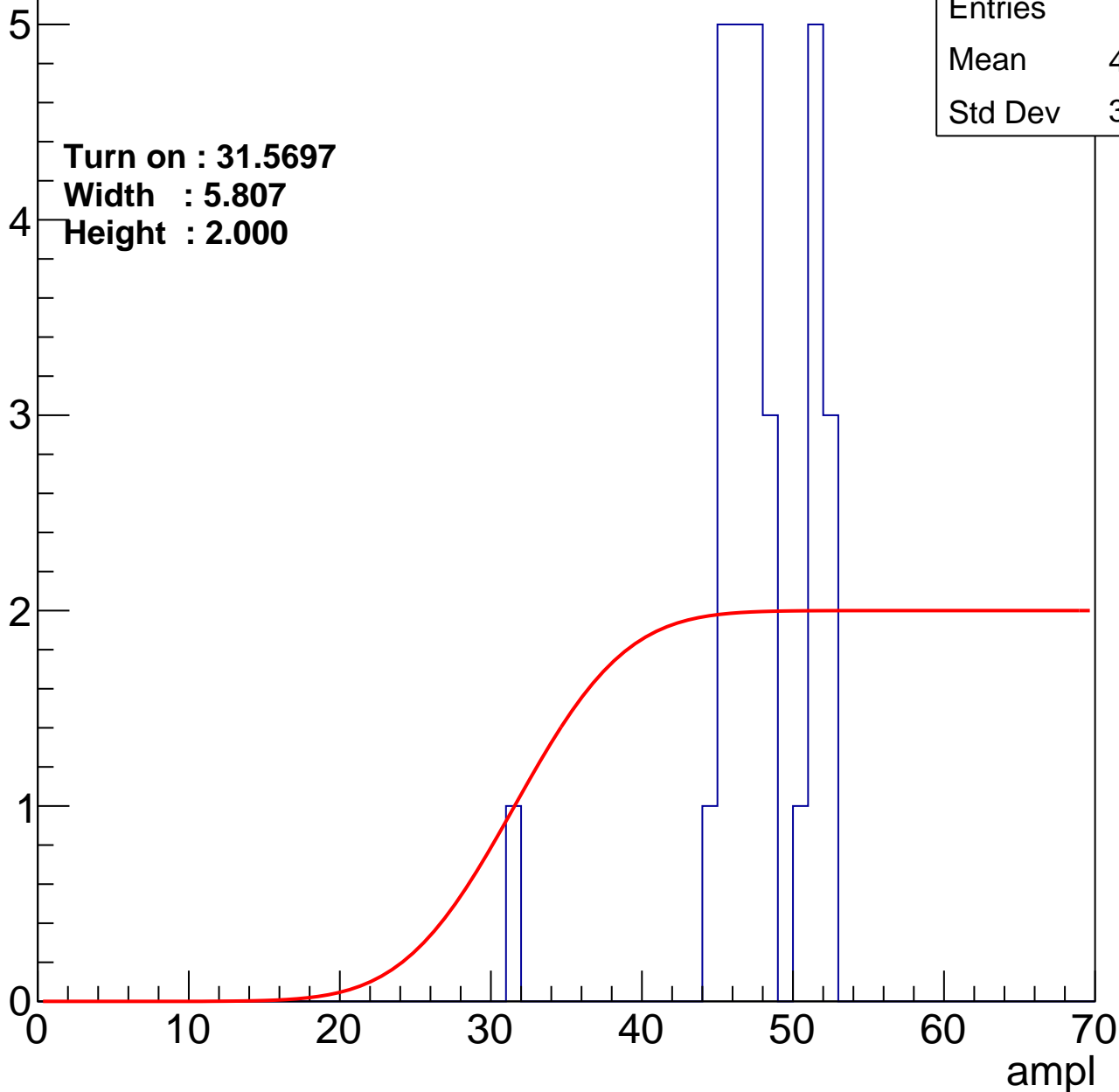
Entry

Entries	29
Mean	47.24
Std Dev	3.962

Turn on : 31.5697

Width : 5.807

Height : 2.000



# B0L100S, U12-ch60

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

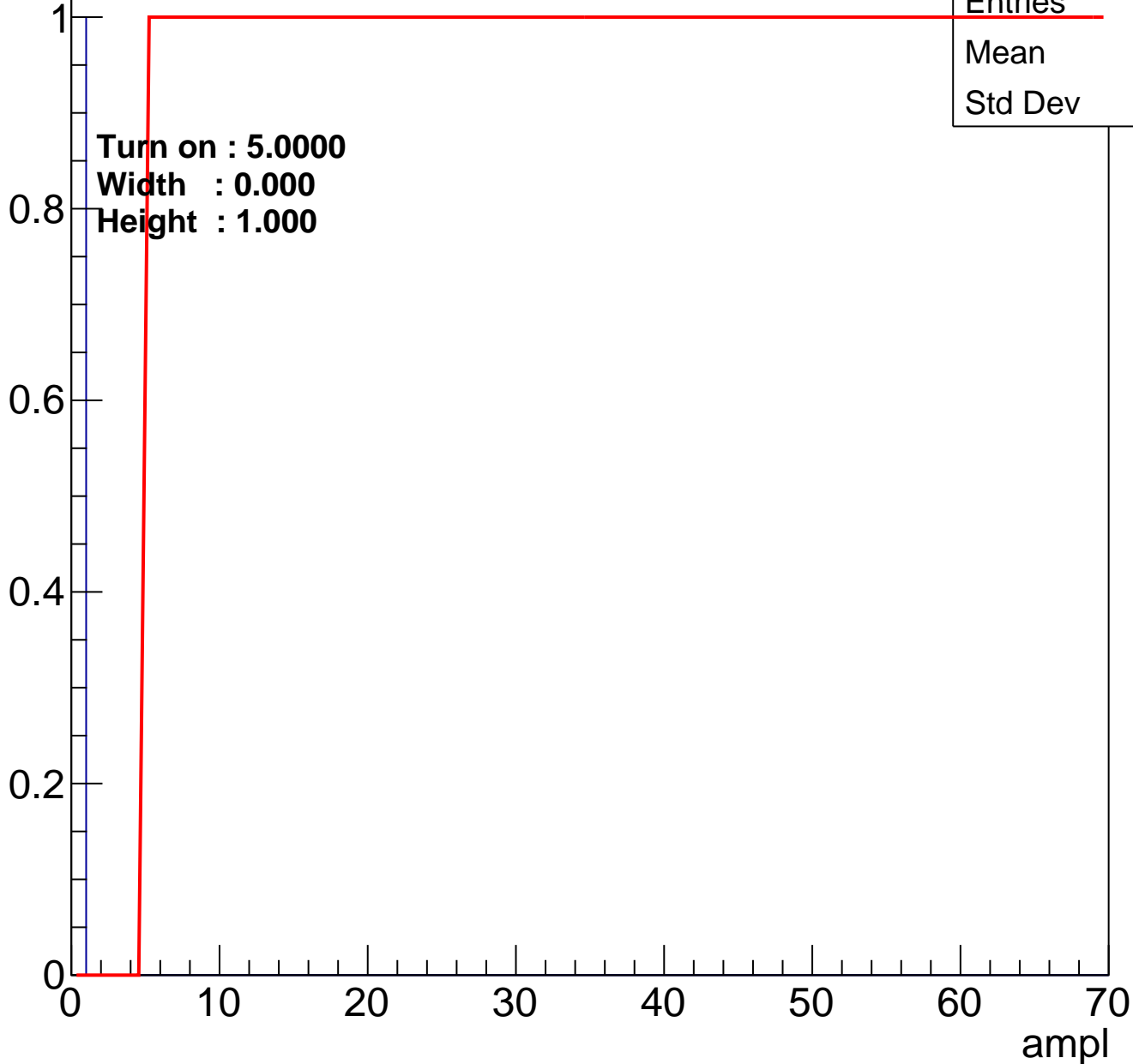


Entries	0
Mean	0
Std Dev	0

# B0L100S, U12-ch61

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L100S, U12-ch62

calib\_packv5\_042523\_0143.root, FC#6, port A1

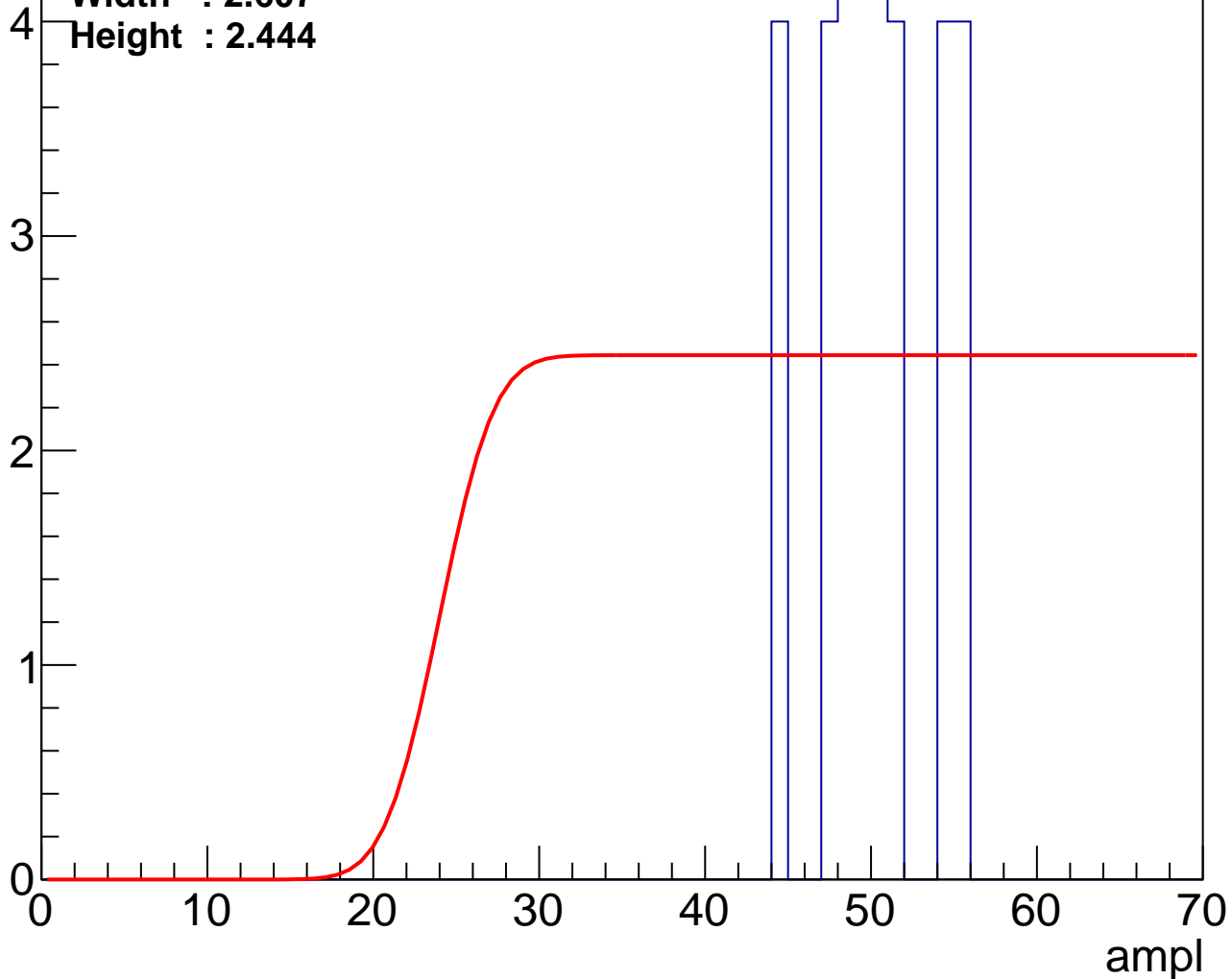
Entry

Entries	35
Mean	49.69
Std Dev	3.249

Turn on : 23.9882

Width : 2.607

Height : 2.444





# B0L100S, U12-ch63

calib\_packv5\_042523\_0143.root, FC#6, port A1

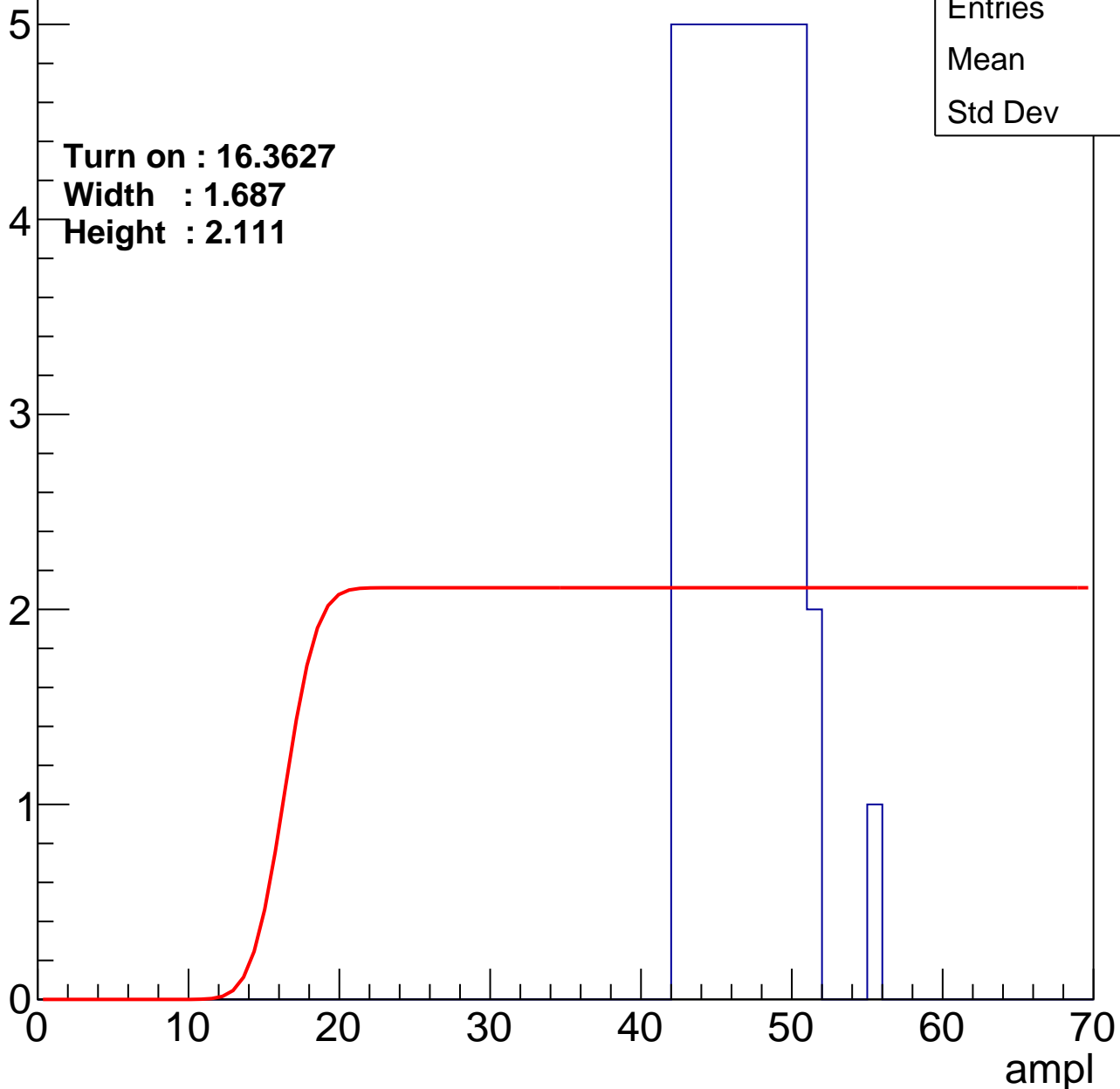
Entry

Entries	48
Mean	46.4
Std Dev	2.97

Turn on : 16.3627

Width : 1.687

Height : 2.111



# B0L100S, U12-ch64

calib\_packv5\_042523\_0143.root, FC#6, port A1

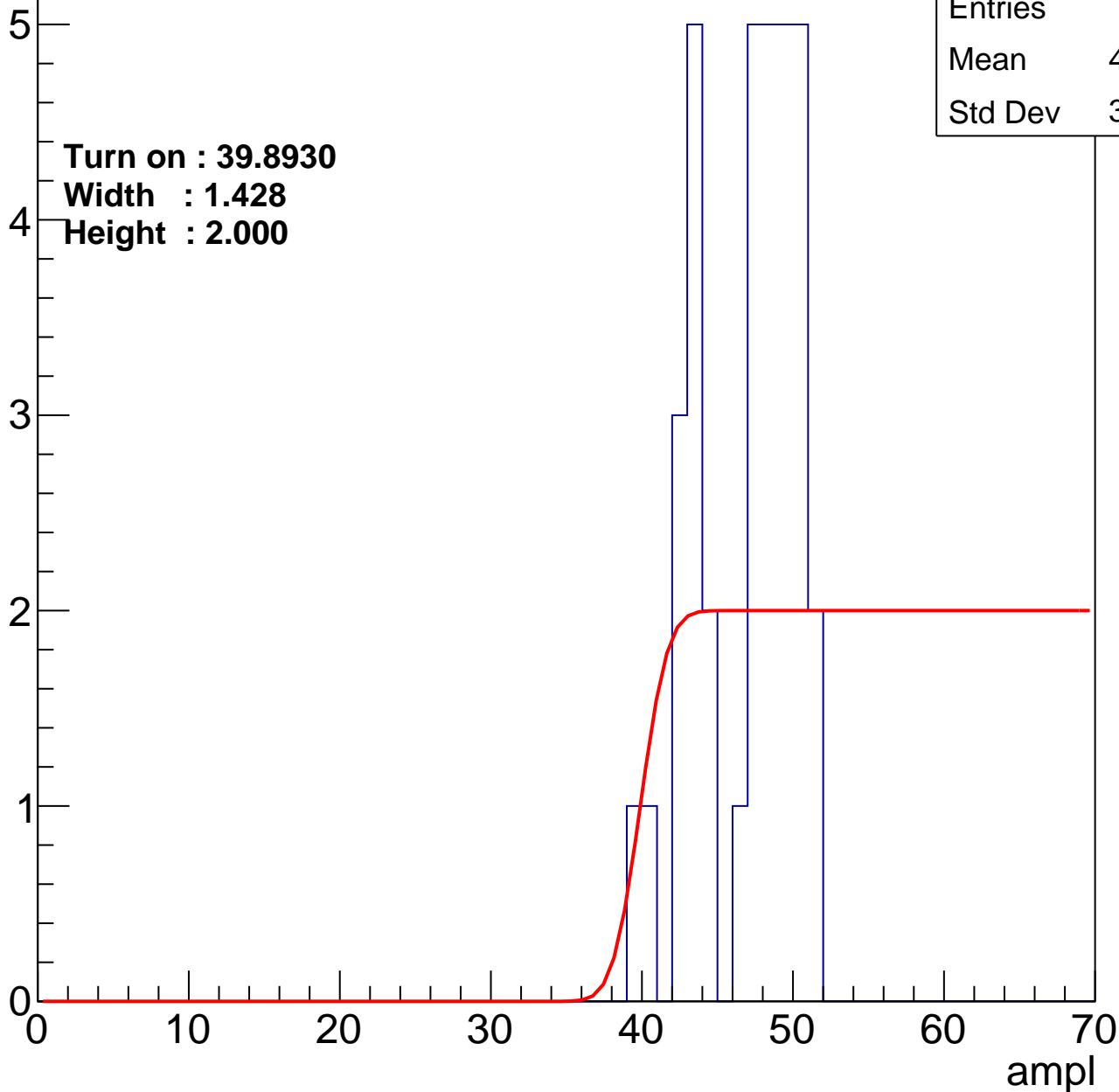
Entry

Entries	35
Mean	46.46
Std Dev	3.289

Turn on : 39.8930

Width : 1.428

Height : 2.000



# B0L100S, U12-ch65

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L100S, U12-ch66

calib\_packv5\_042523\_0143.root, FC#6, port A1

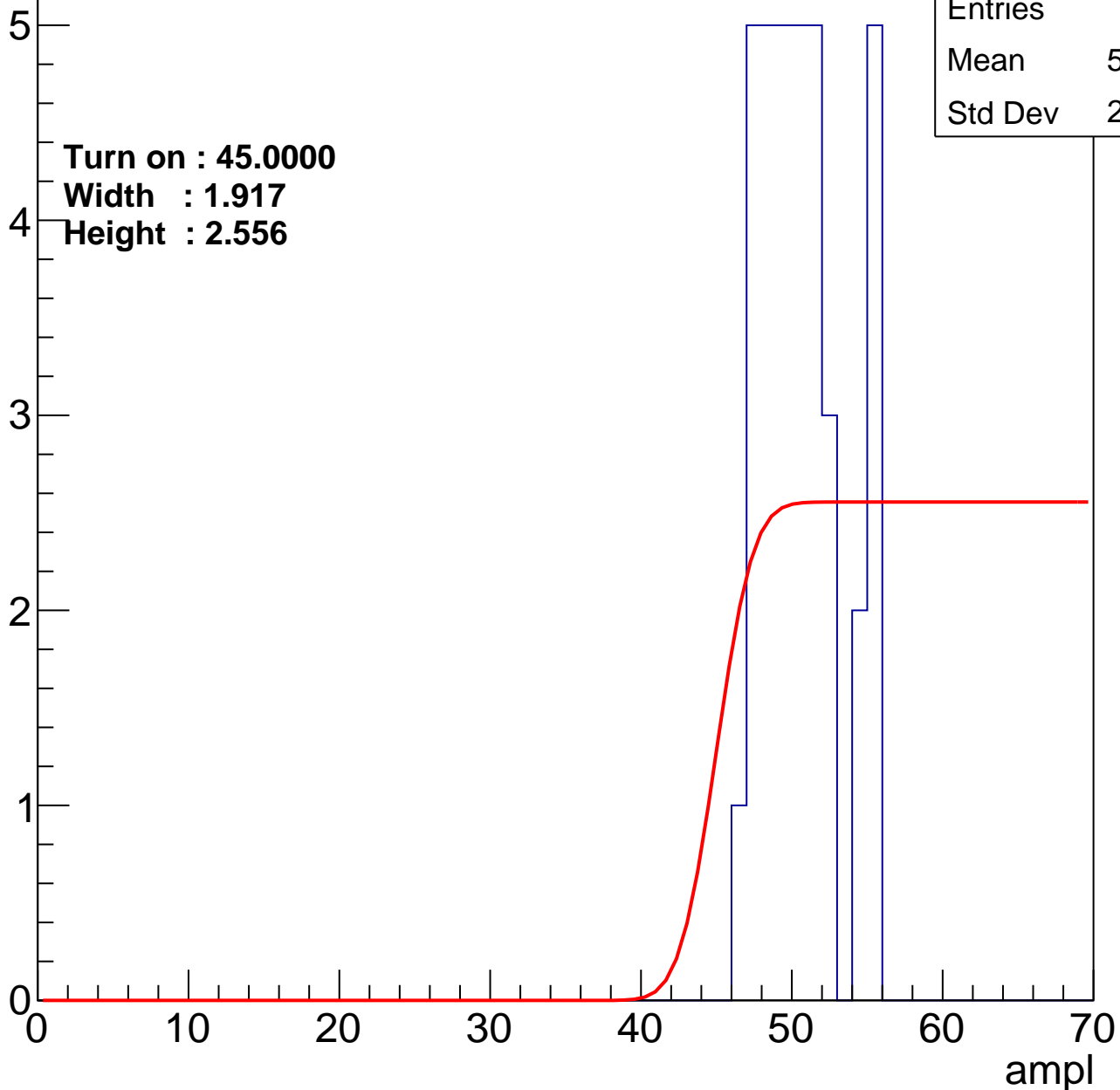
Entry

Entries	36
Mean	50.28
Std Dev	2.673

Turn on : 45.0000

Width : 1.917

Height : 2.556



# B0L100S, U12-ch67

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U12-ch68

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

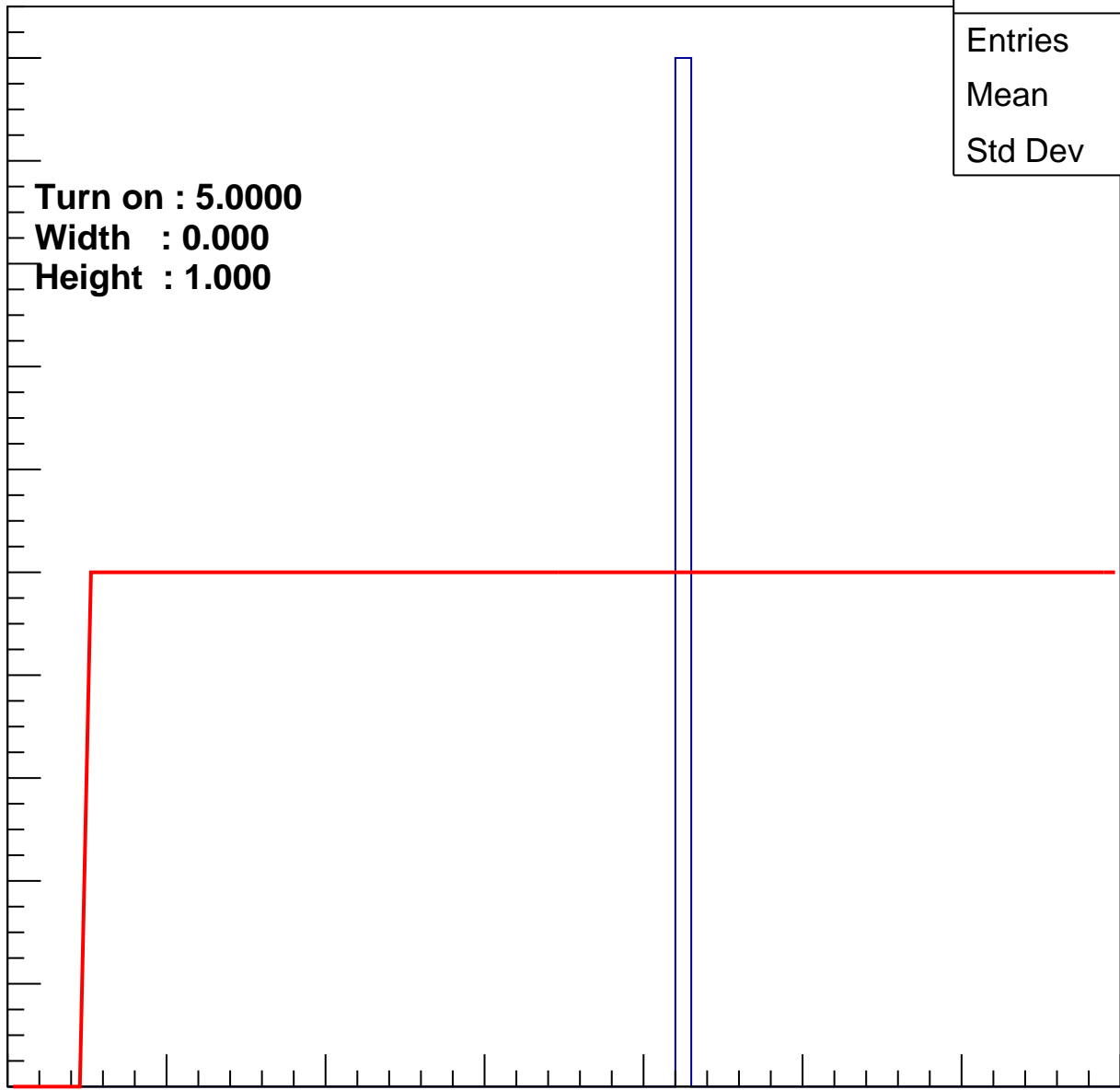
2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Turn on : 5.0000  
Width : 0.000  
Height : 1.000

Entries	2
Mean	42
Std Dev	0

0 10 20 30 40 50 60 70

ampl



# B0L100S, U12-ch69

calib\_packv5\_042523\_0143.root, FC#6, port A1

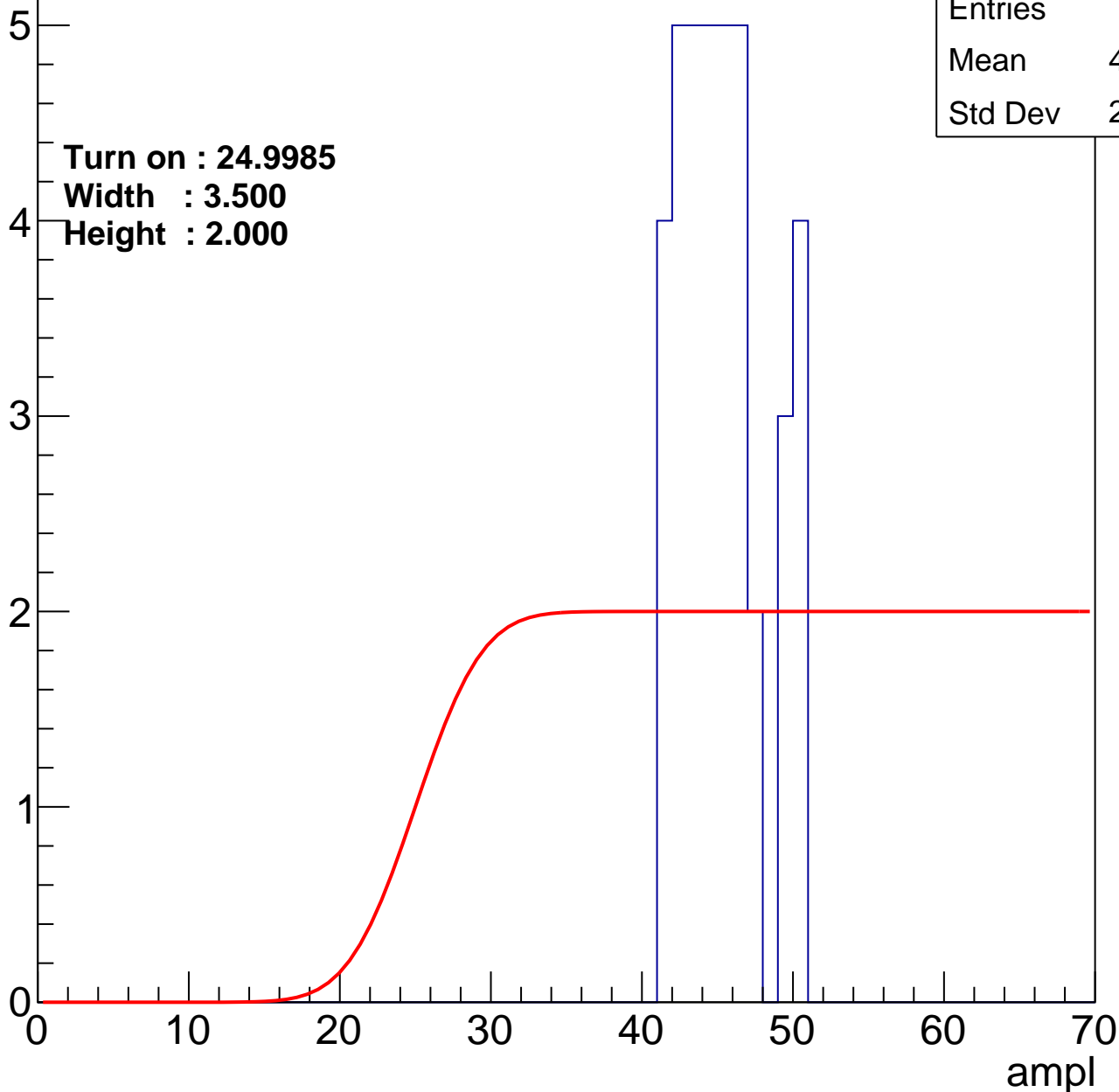
Entry

Entries	38
Mean	44.87
Std Dev	2.783

Turn on : 24.9985

Width : 3.500

Height : 2.000



# B0L100S, U12-ch70

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



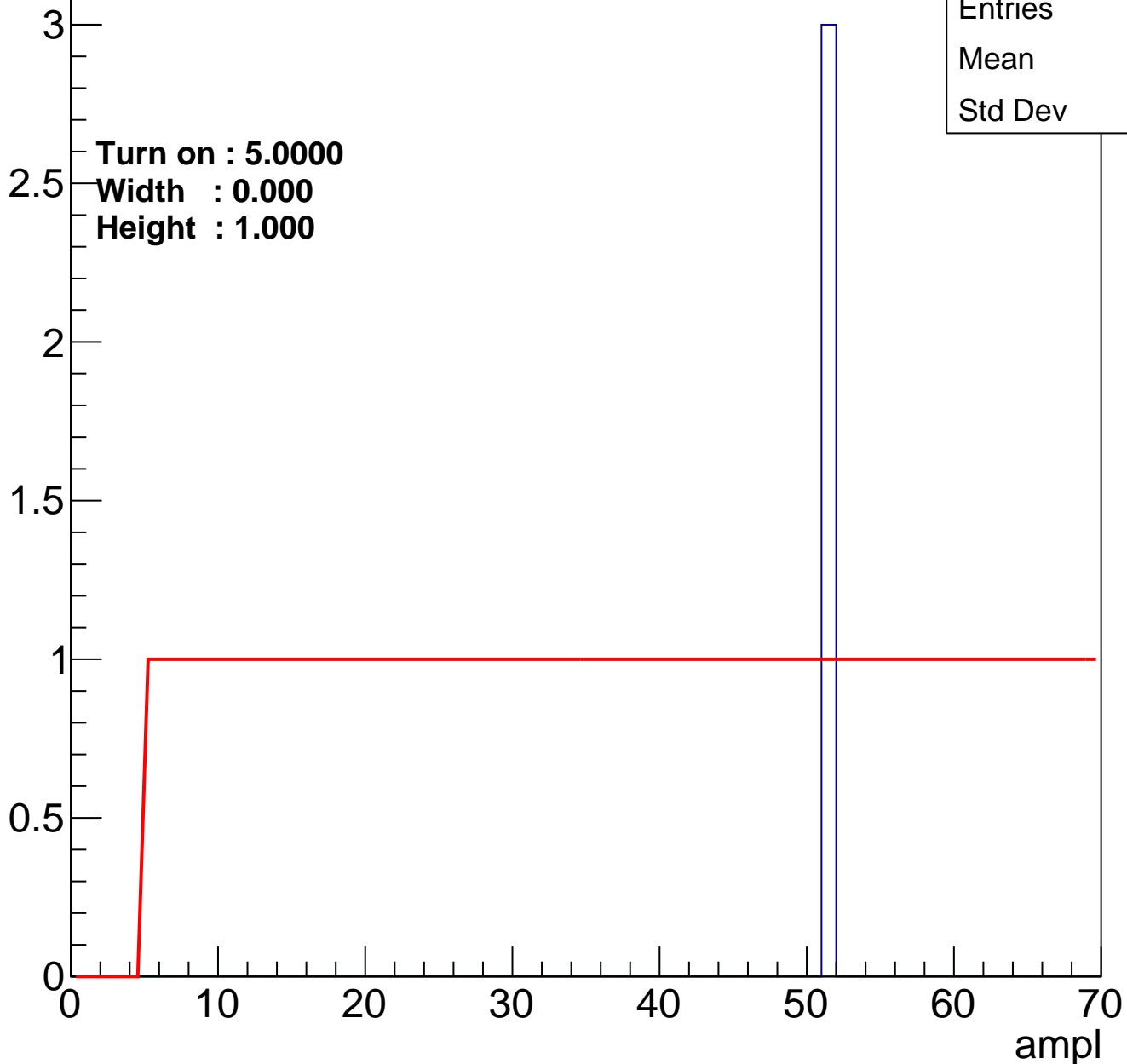
Entries	0
Mean	0
Std Dev	0



# B0L100S, U12-ch71

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U12-ch72

calib\_packv5\_042523\_0143.root, FC#6, port A1

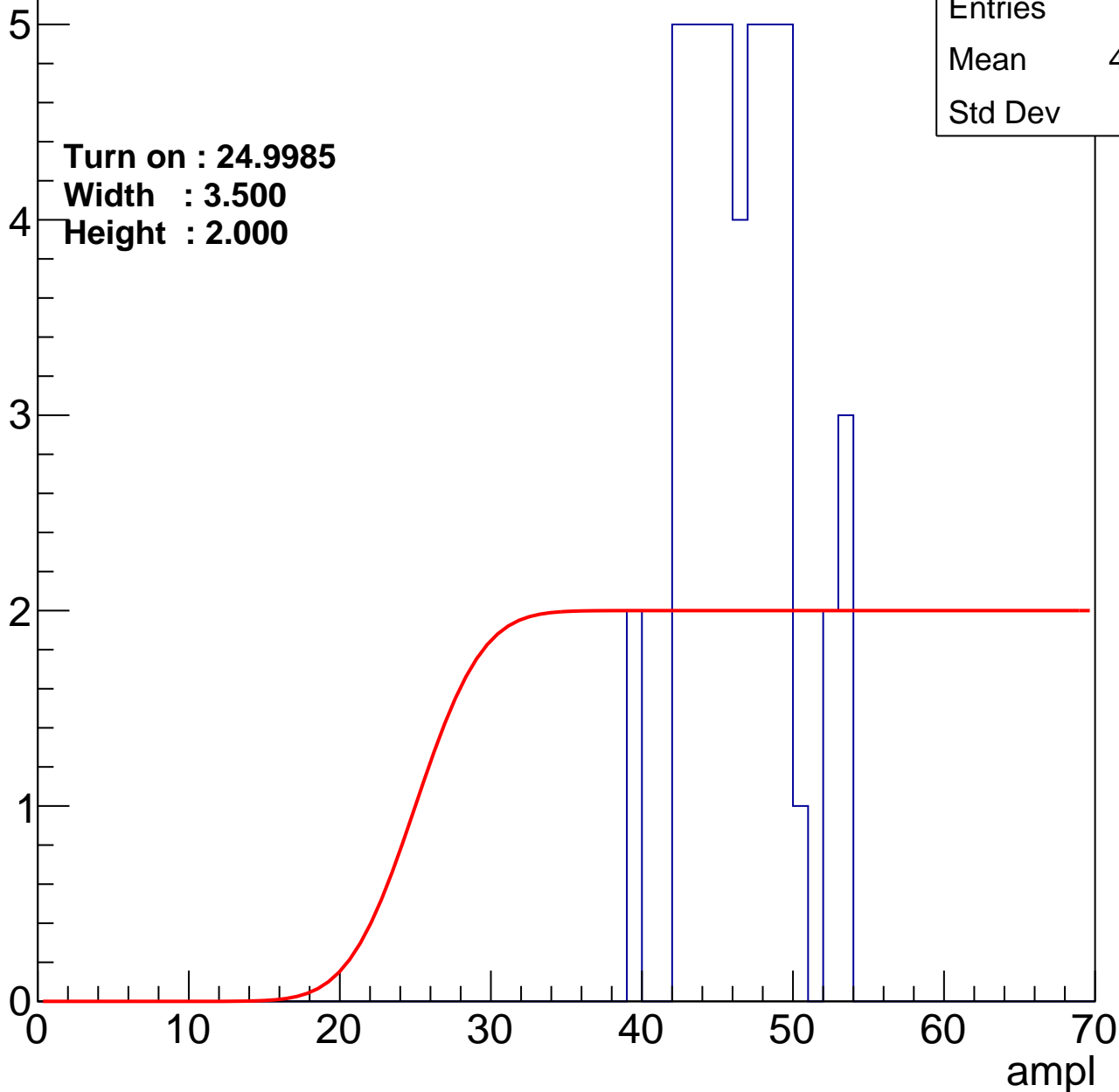
Entry

Entries	47
Mean	46.06
Std Dev	3.43

Turn on : 24.9985

Width : 3.500

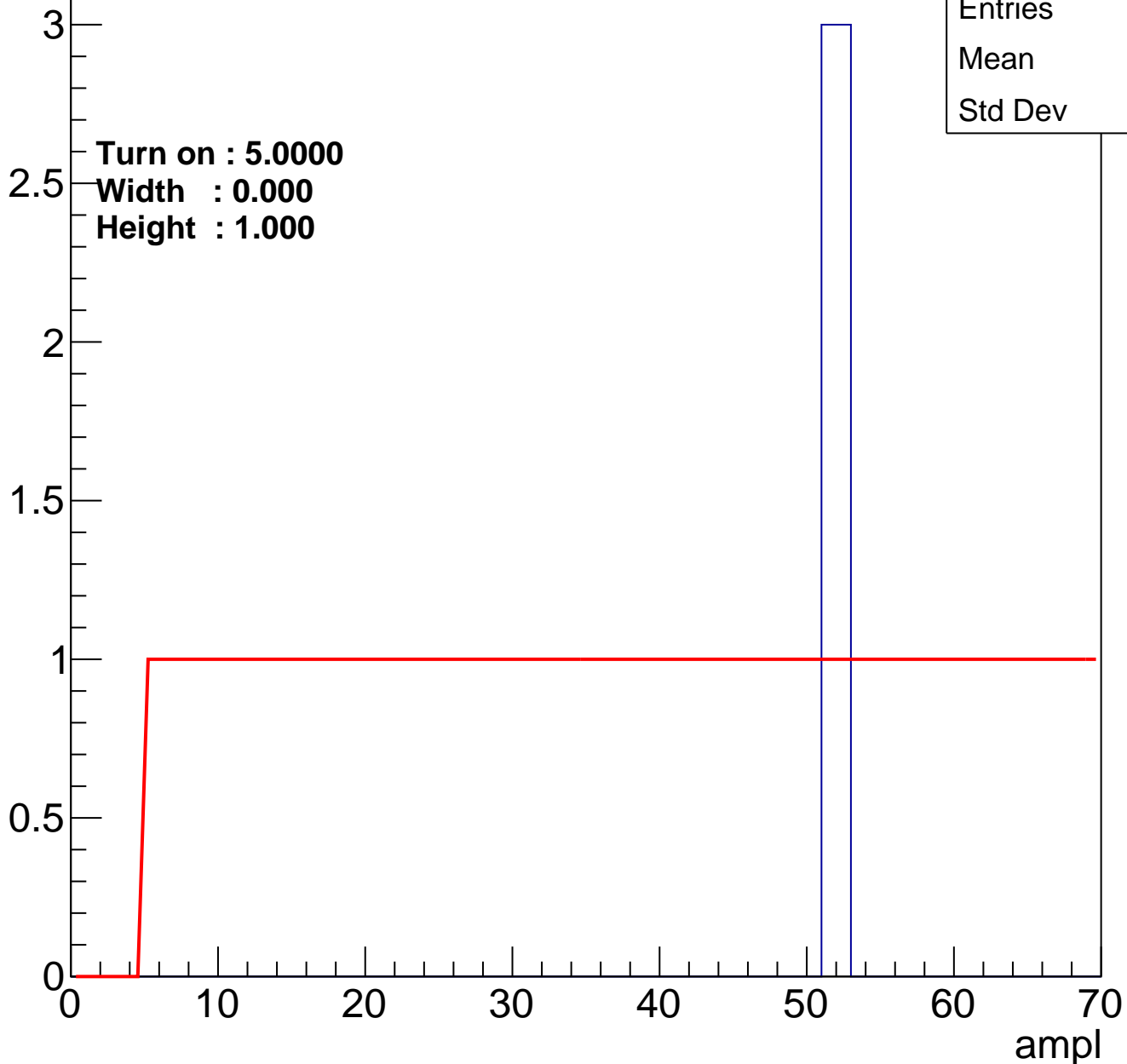
Height : 2.000



# B0L100S, U12-ch73

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U12-ch74

calib\_packv5\_042523\_0143.root, FC#6, port A1

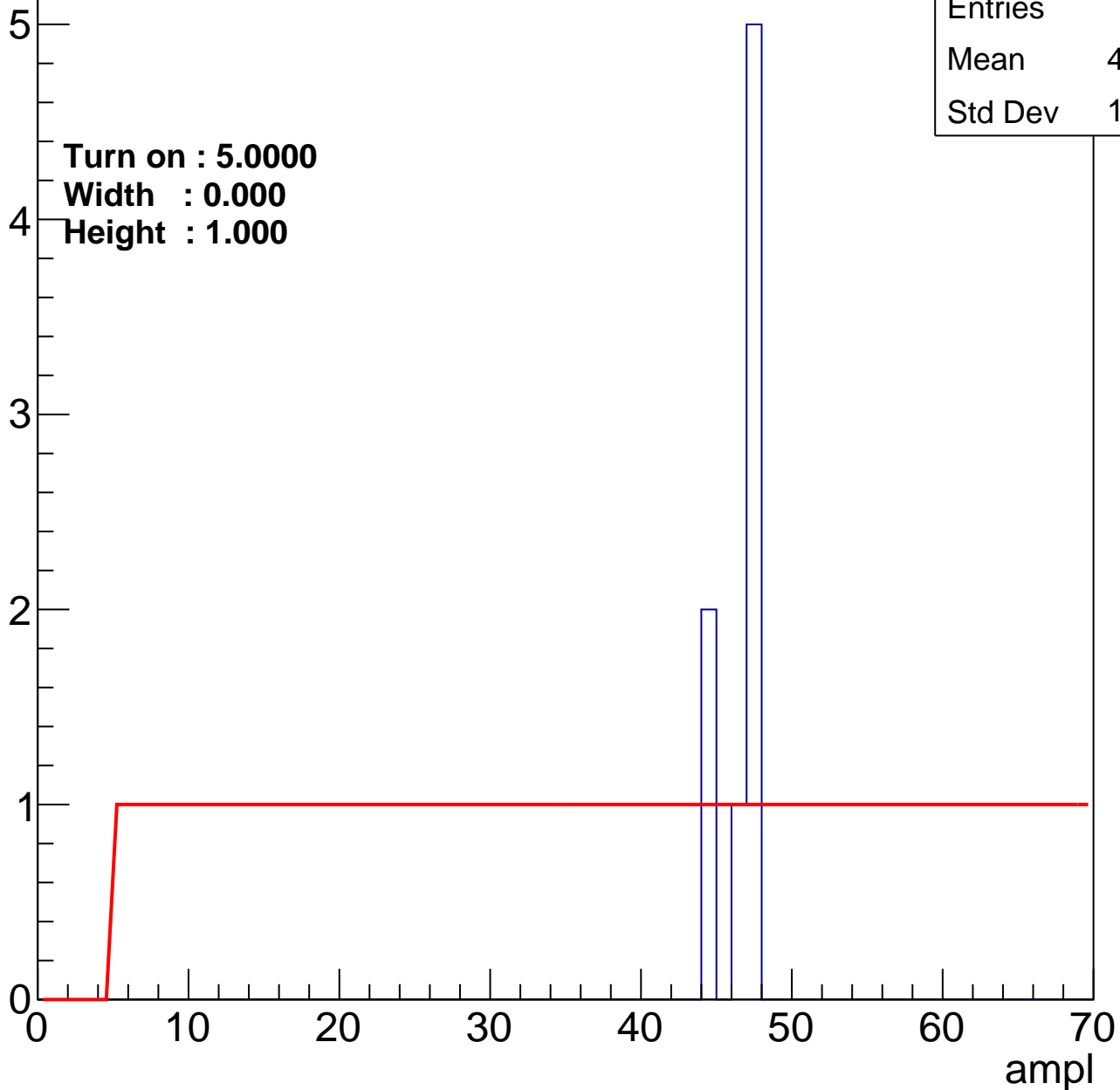
Entry

Entries	8
Mean	46.12
Std Dev	1.269

Turn on : 5.0000

Width : 0.000

Height : 1.000



# B0L100S, U12-ch75

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U12-ch76

calib\_packv5\_042523\_0143.root, FC#6, port A1

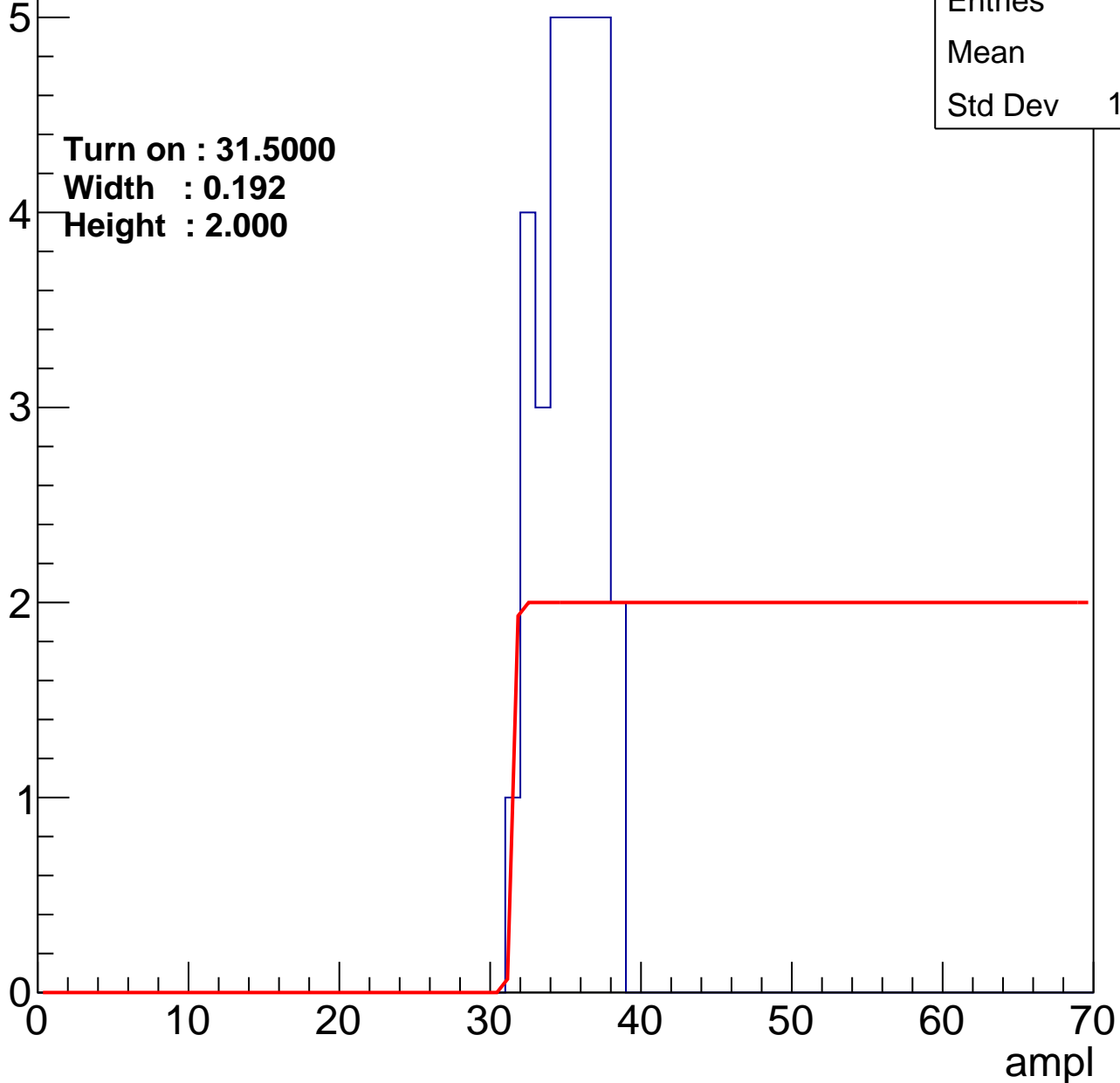
Entry

Entries	30
Mean	34.8
Std Dev	1.922

Turn on : 31.5000

Width : 0.192

Height : 2.000



# B0L100S, U12-ch77

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U12-ch78

calib\_packv5\_042523\_0143.root, FC#6, port A1

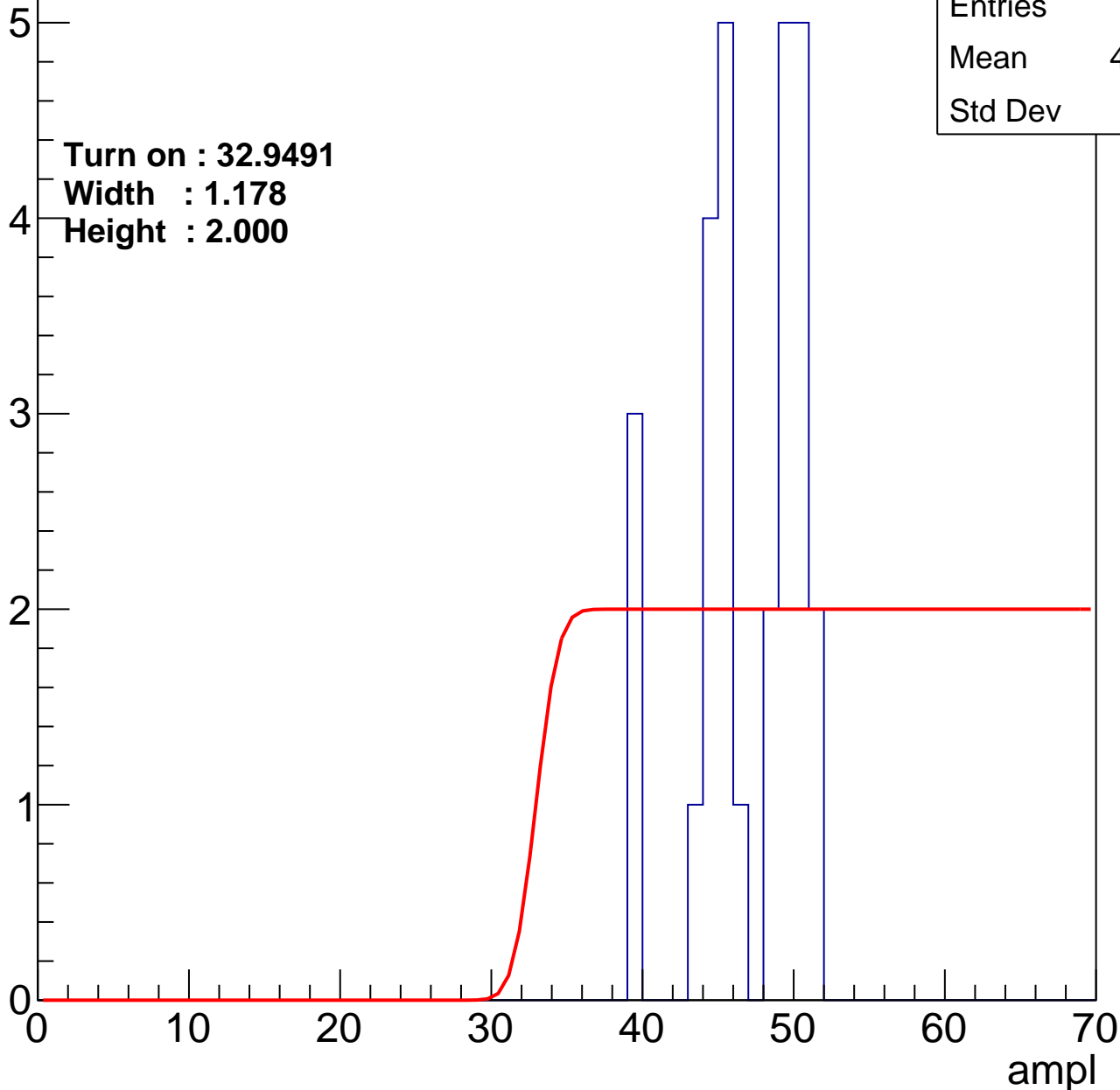
Entry

Entries	28
Mean	46.43
Std Dev	3.56

Turn on : 32.9491

Width : 1.178

Height : 2.000





# B0L100S, U12-ch79

calib\_packv5\_042523\_0143.root, FC#6, port A1

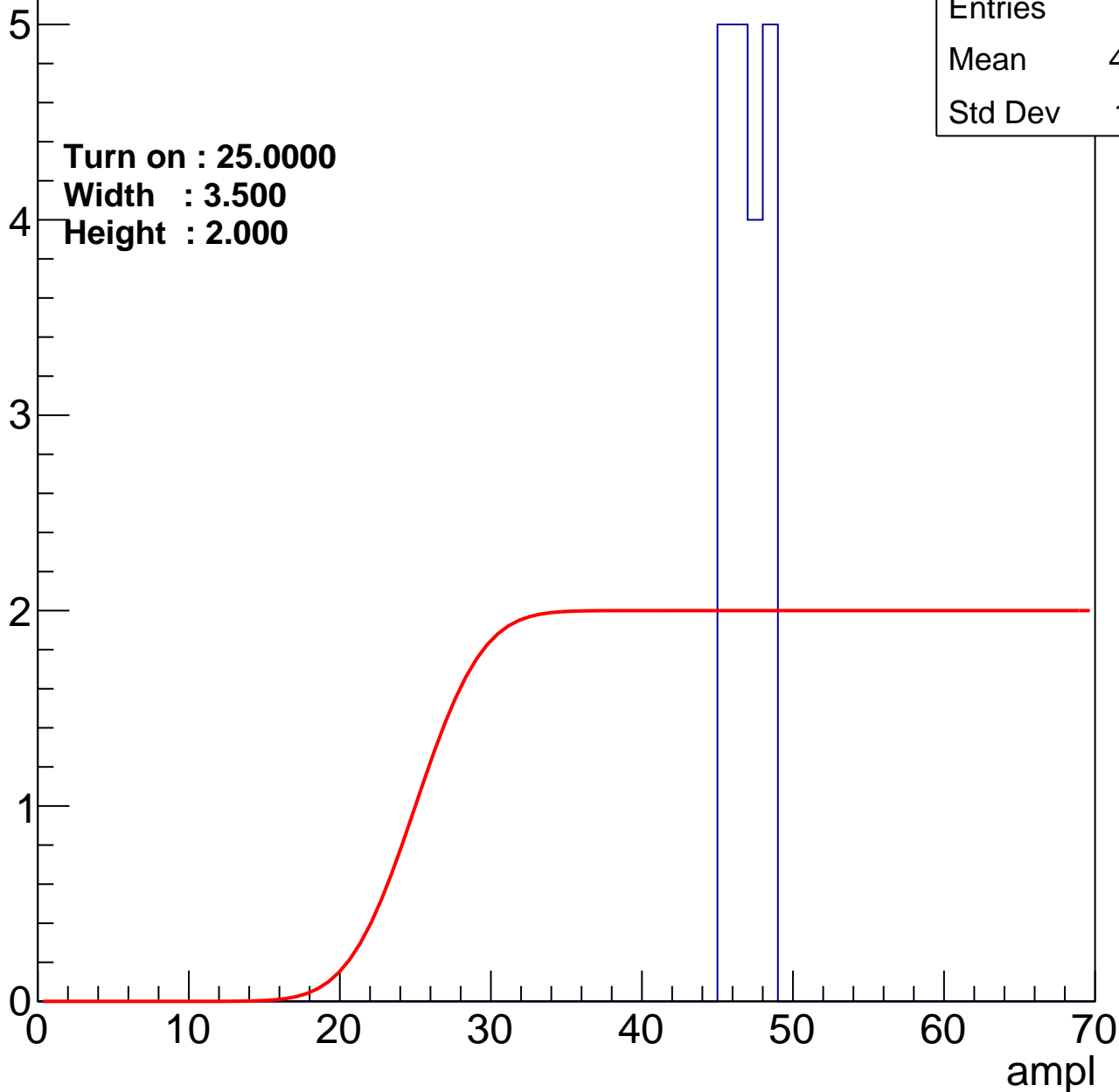
Entry

Entries	19
Mean	46.47
Std Dev	1.141

Turn on : 25.0000

Width : 3.500

Height : 2.000



# B0L100S, U12-ch80

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

5

4

3

2

1

0

Turn on : 5.0000

Width : 0.000

Height : 1.000

Entries	8
Mean	45.75
Std Dev	17.3

ampl

0

10

20

30

40

50

60

70

# B0L100S, U12-ch81

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

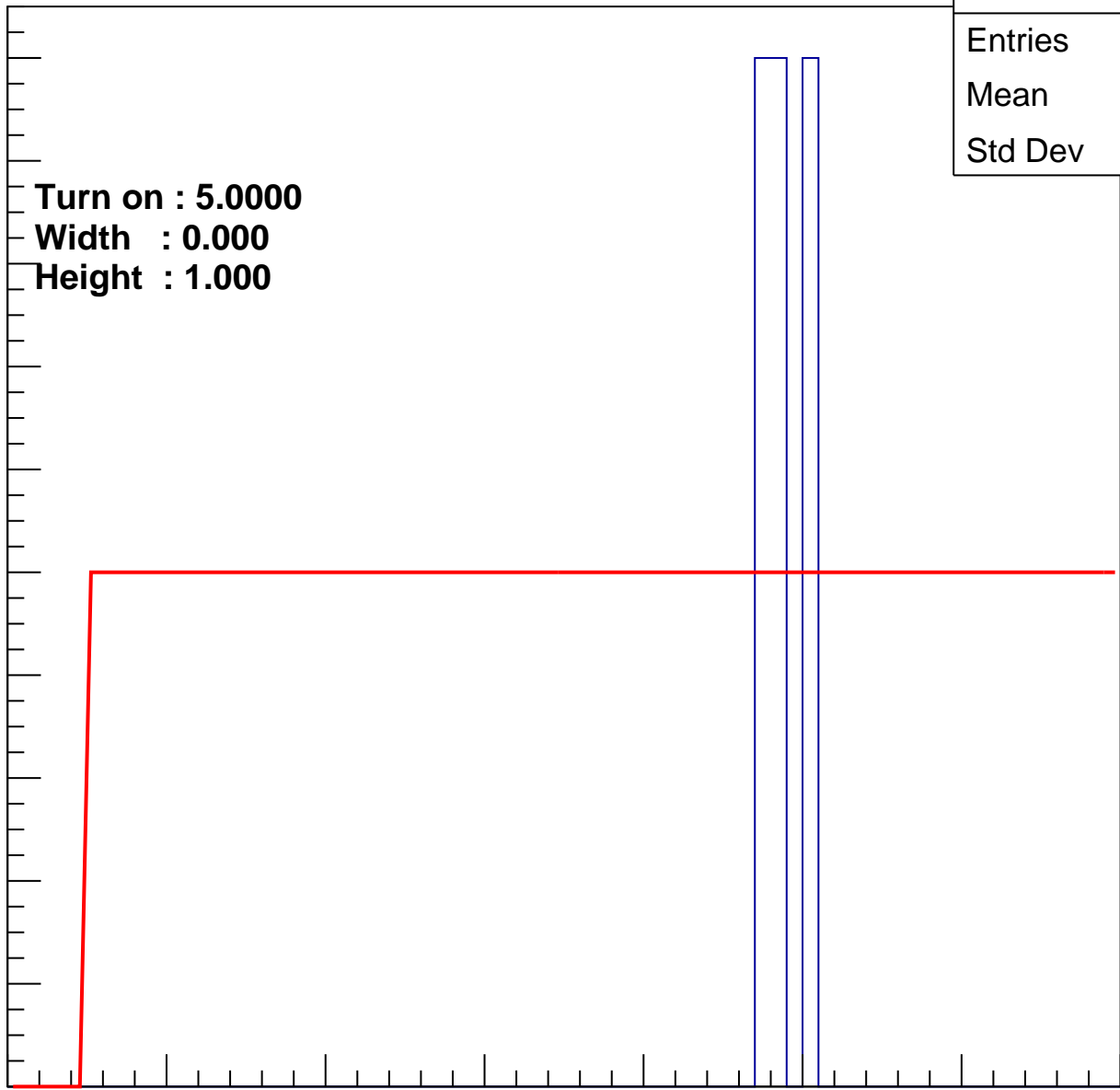
2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Turn on : 5.0000  
Width : 0.000  
Height : 1.000

Entries	6
Mean	48.33
Std Dev	1.247

0 10 20 30 40 50 60 70

ampl



# B0L100S, U12-ch82

calib\_packv5\_042523\_0143.root, FC#6, port A1

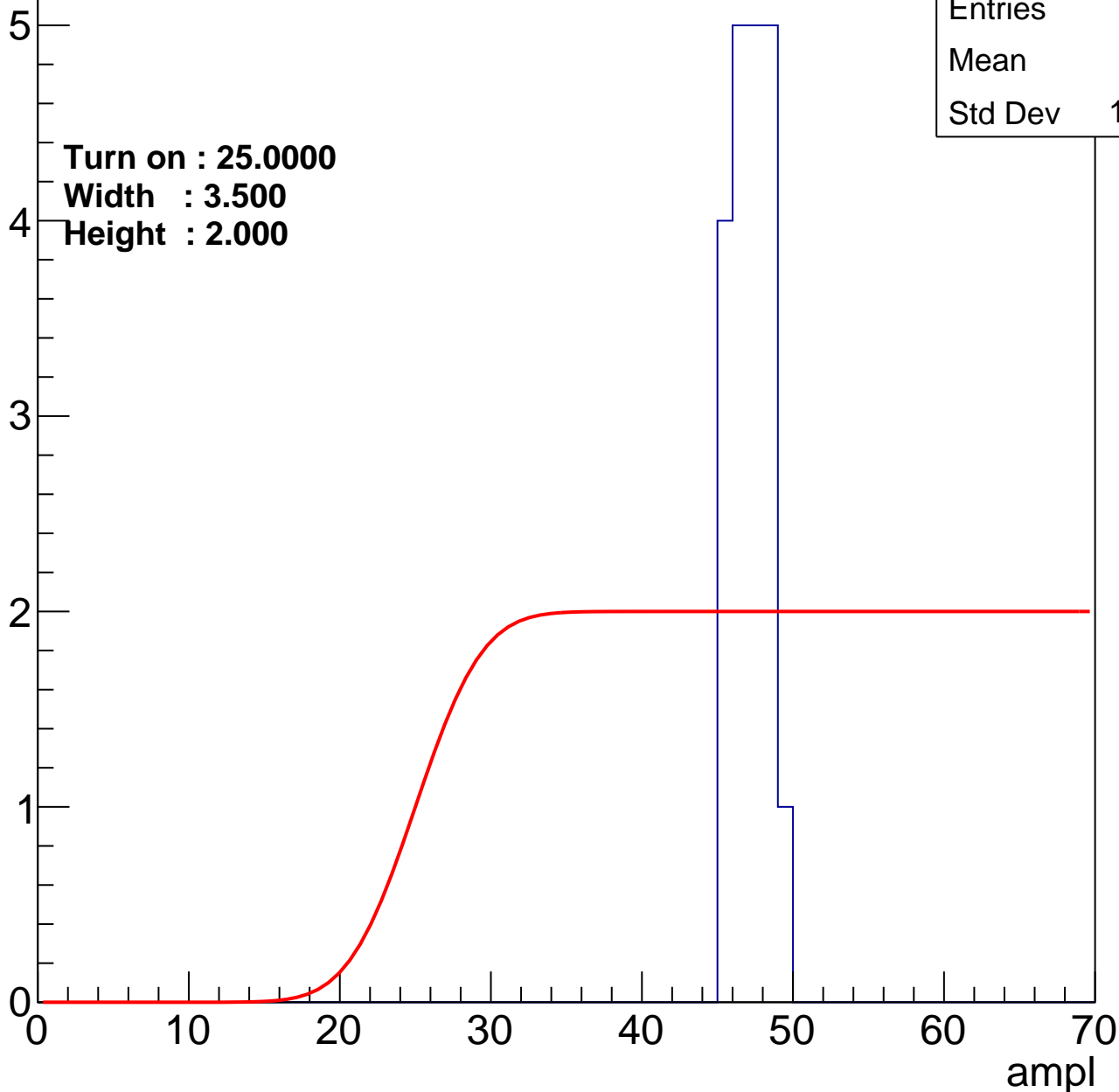
Entry

Entries	20
Mean	46.7
Std Dev	1.187

Turn on : 25.0000

Width : 3.500

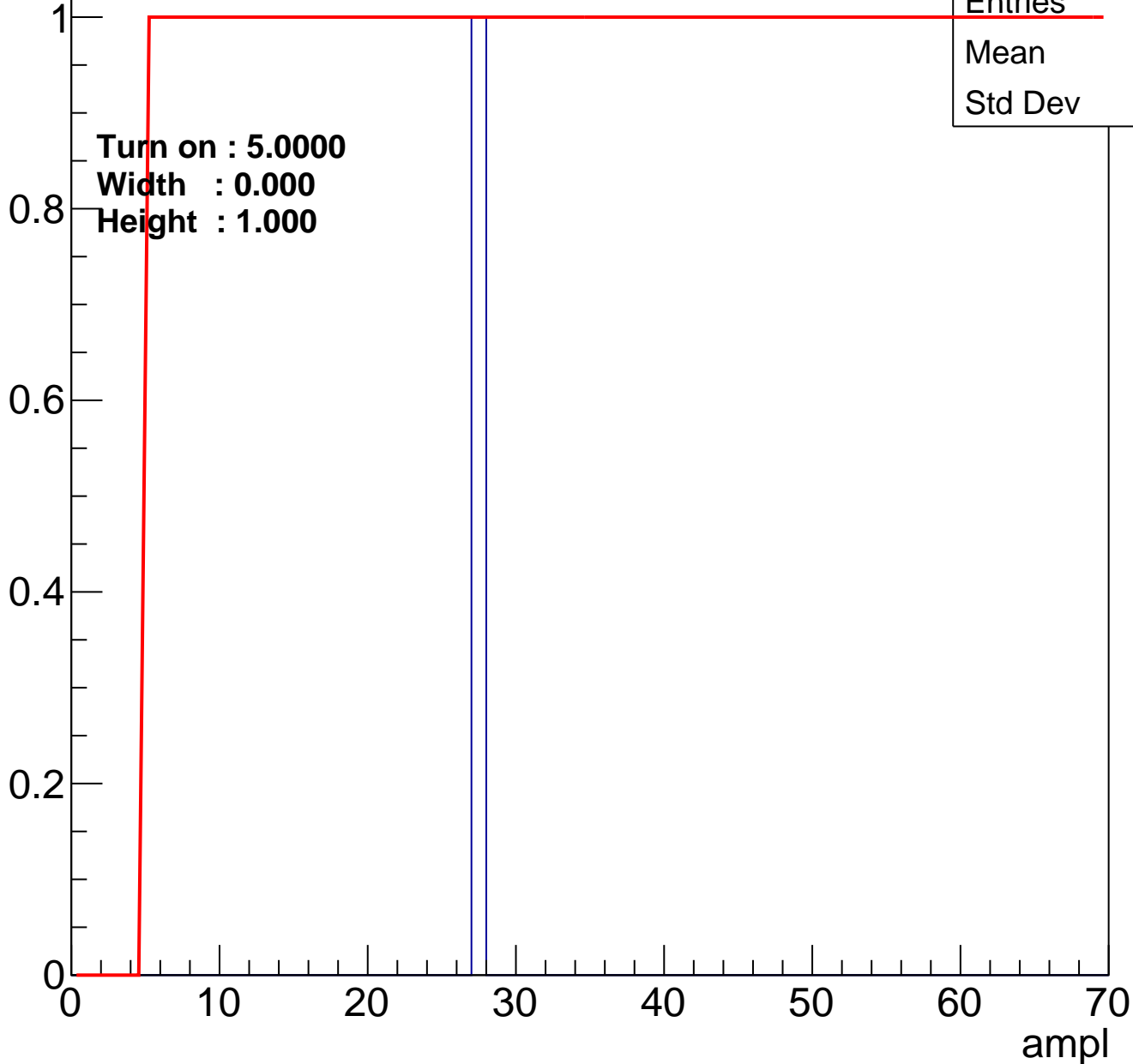
Height : 2.000



# B0L100S, U12-ch83

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U12-ch84

calib\_packv5\_042523\_0143.root, FC#6, port A1

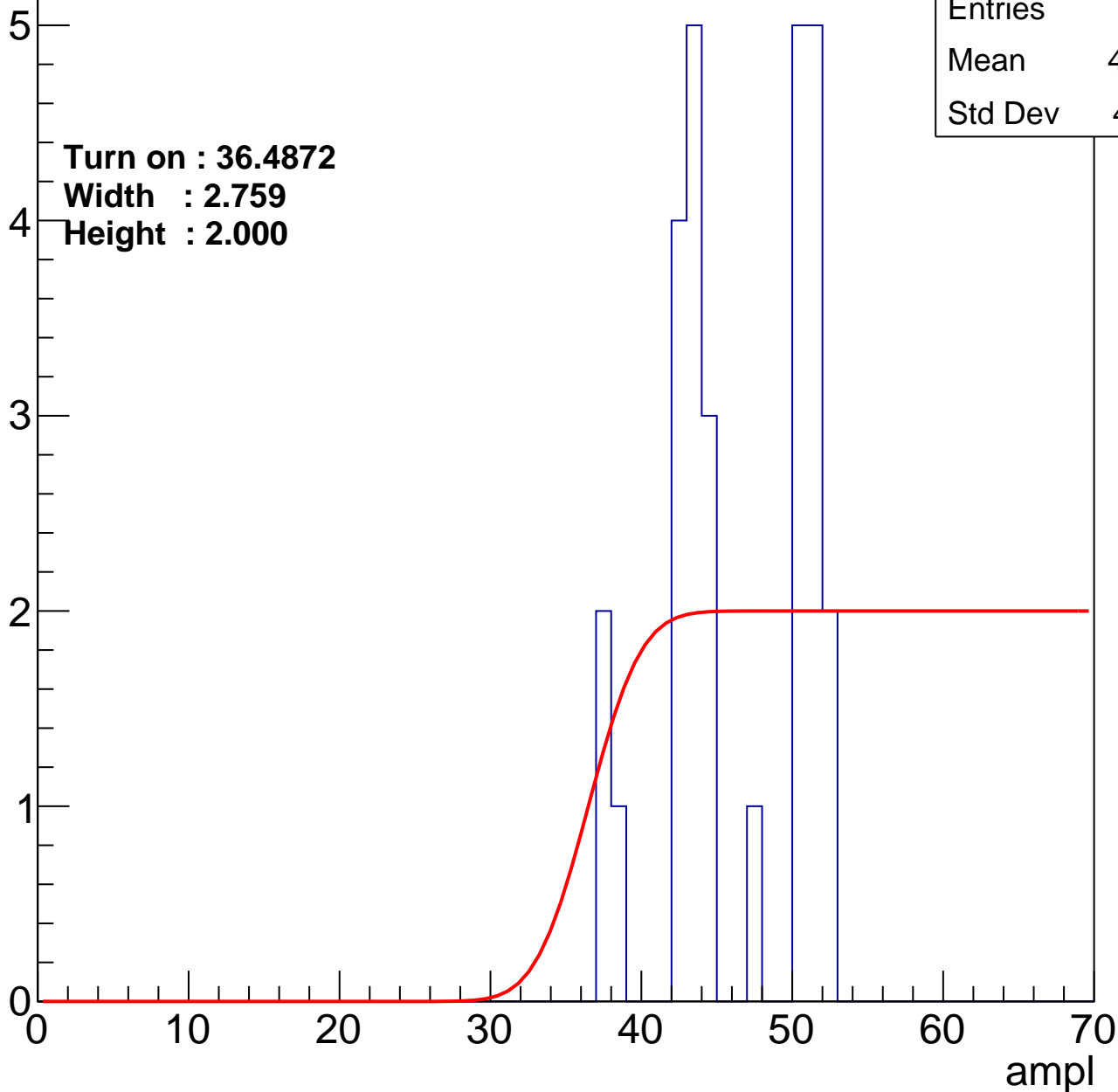
Entry

Entries	28
Mean	45.82
Std Dev	4.721

Turn on : 36.4872

Width : 2.759

Height : 2.000



# B0L100S, U12-ch85

calib\_packv5\_042523\_0143.root, FC#6, port A1

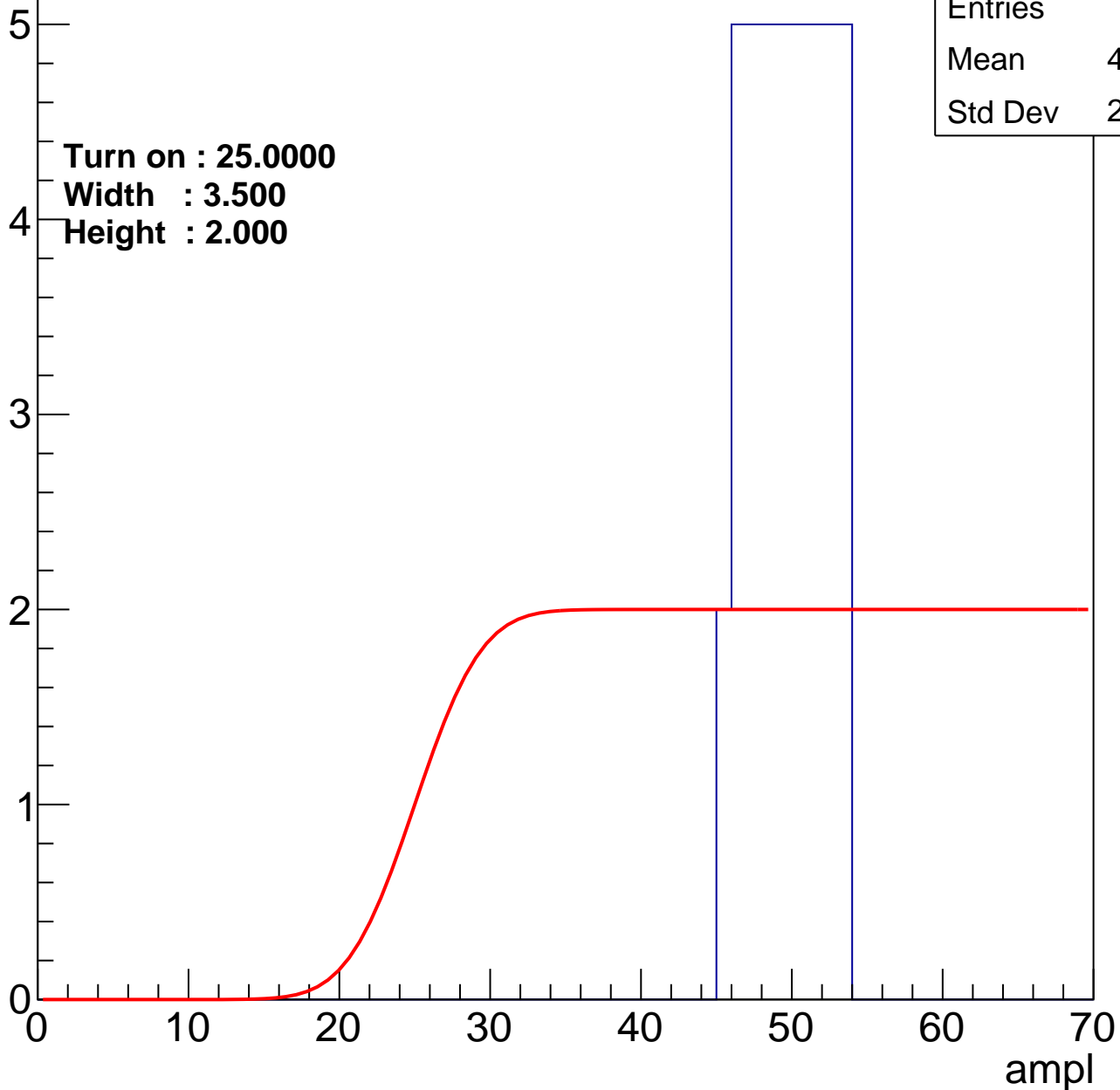
Entry

Entries	42
Mean	49.29
Std Dev	2.433

Turn on : 25.0000

Width : 3.500

Height : 2.000



# B0L100S, U12-ch86

calib\_packv5\_042523\_0143.root, FC#6, port A1

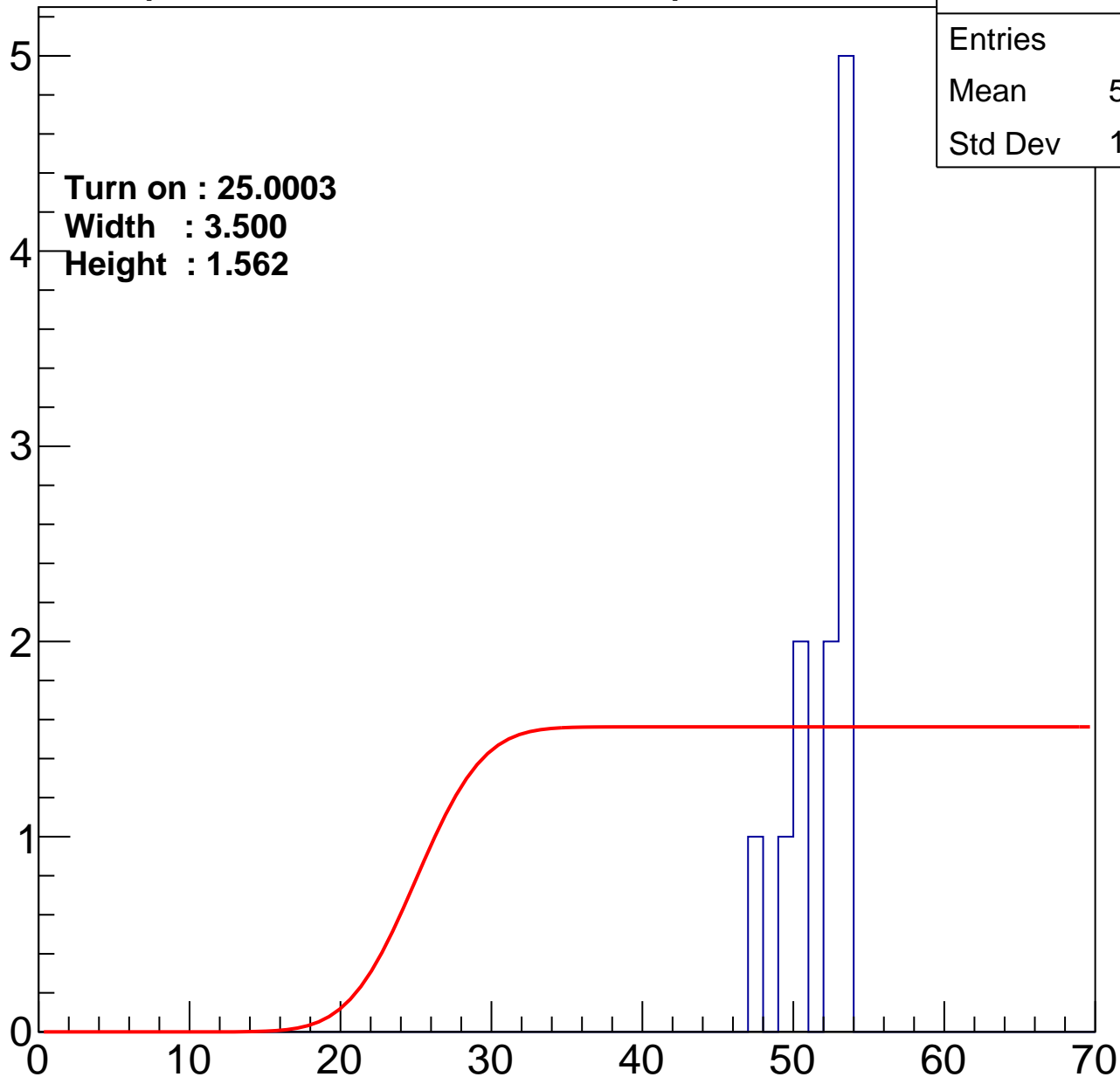
Entry

5  
4  
3  
2  
1  
0

Turn on : 25.0003  
Width : 3.500  
Height : 1.562

Entries	11
Mean	51.36
Std Dev	1.967

ampl

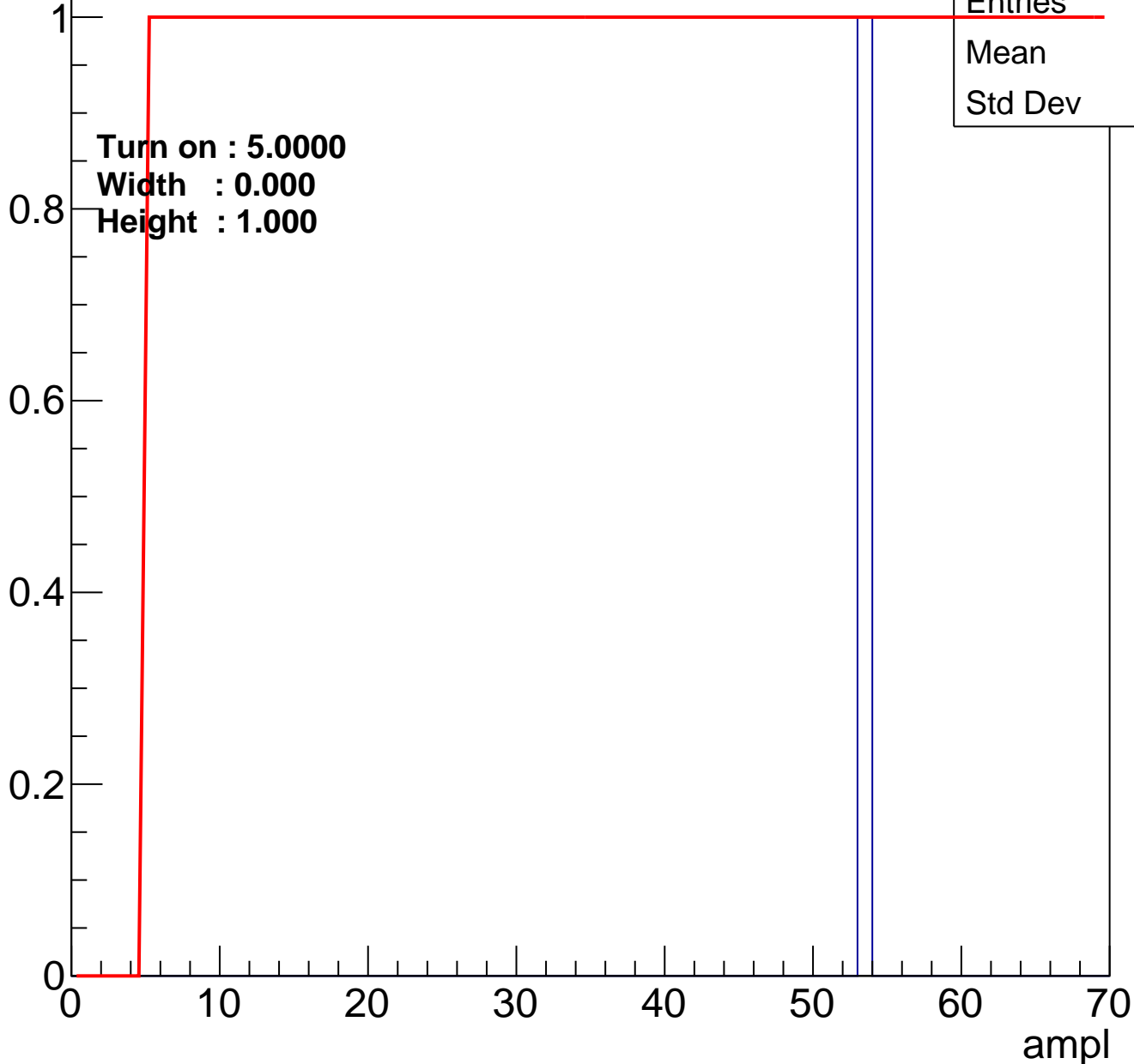




# B0L100S, U12-ch87

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U12-ch88

calib\_packv5\_042523\_0143.root, FC#6, port A1

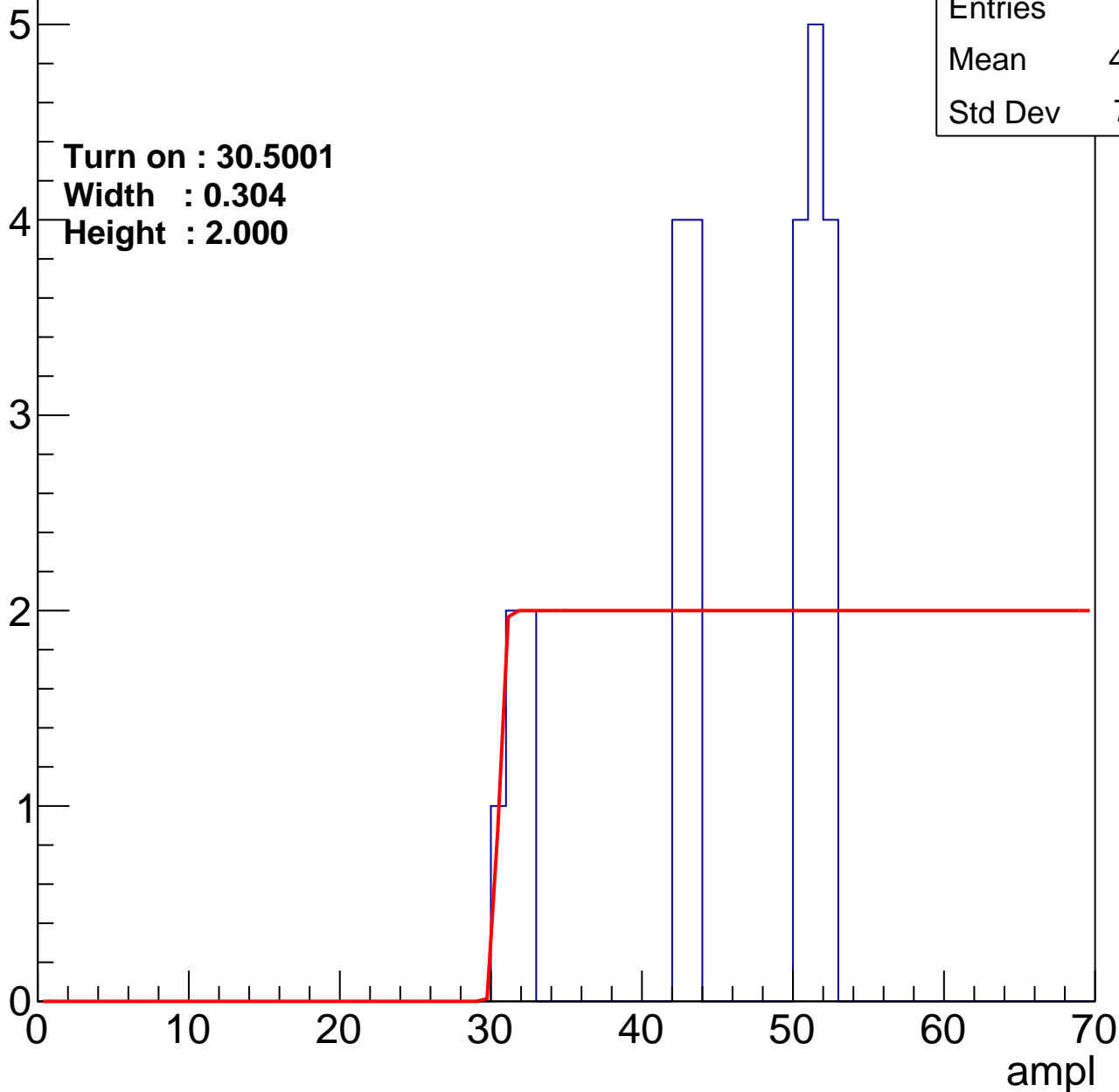
Entry

Entries	26
Mean	44.58
Std Dev	7.541

Turn on : 30.5001

Width : 0.304

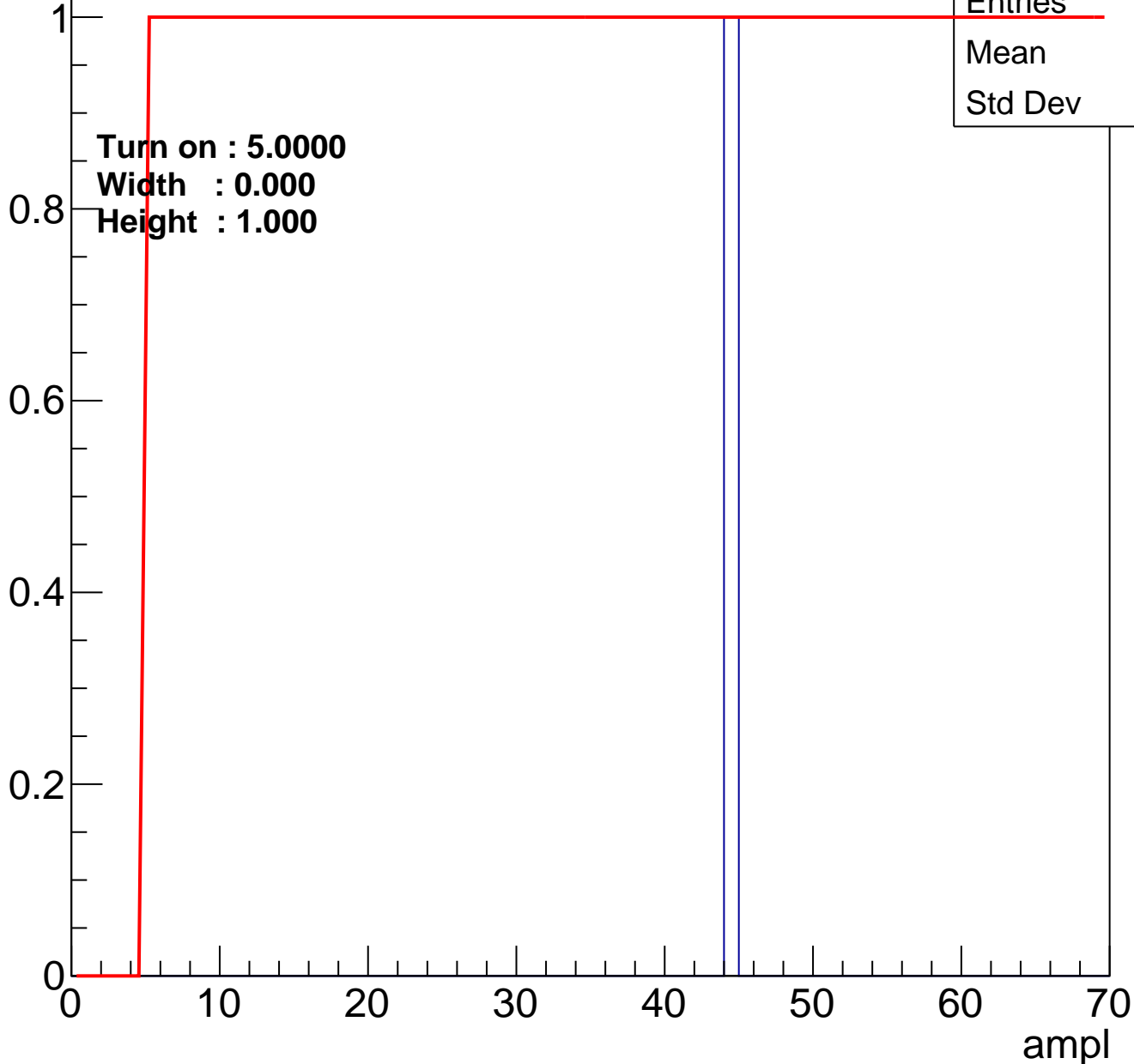
Height : 2.000



# B0L100S, U12-ch89

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U12-ch90

**calib\_packv5\_042523\_0143.root, FC#6, port A1**

# Entry

Entries	36
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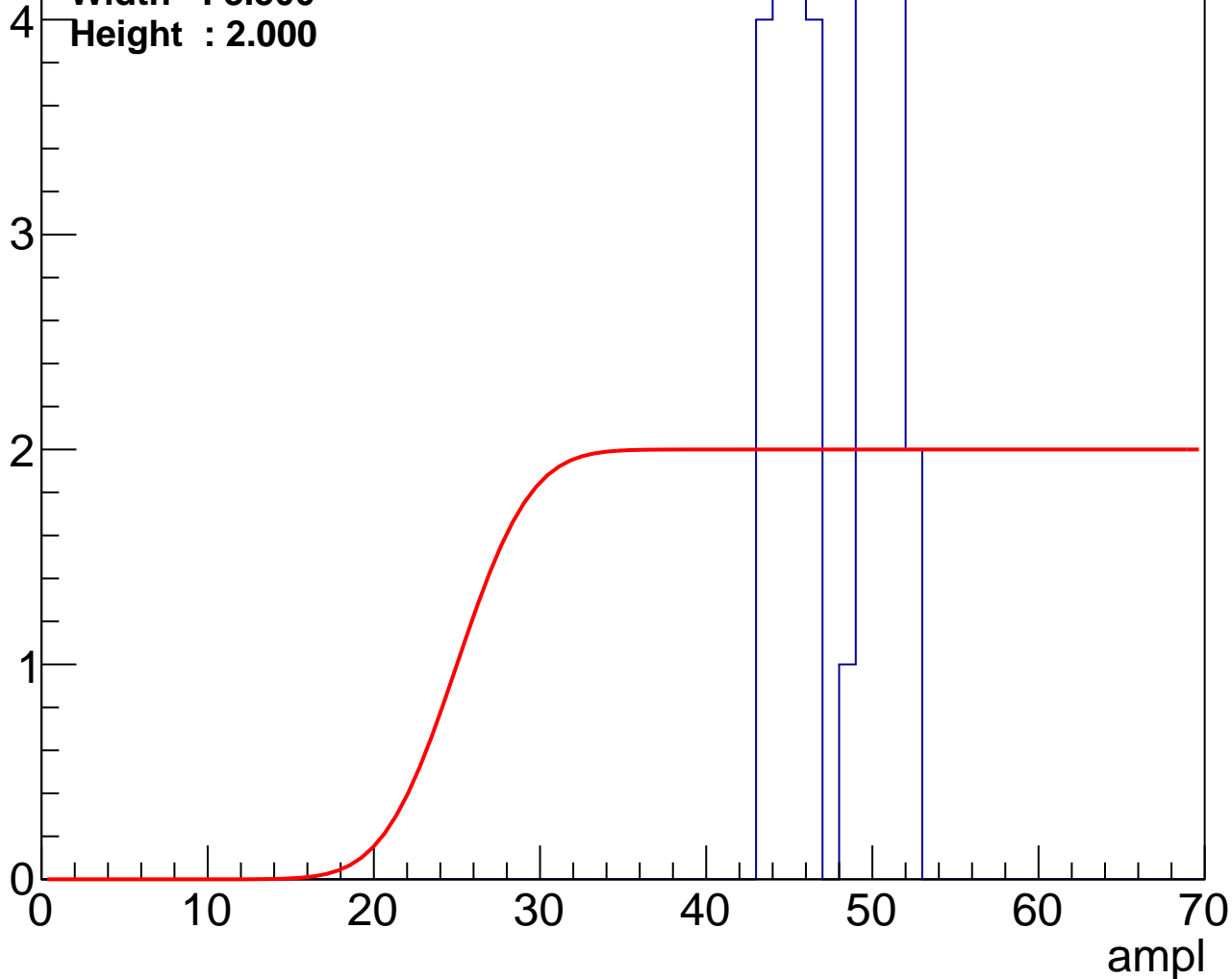
Mean	47.31
------	-------

Std Dev	3.008
---------	-------

**Turn on : 24.9999**

**Width : 3.500**

**Height : 2.000**



# B0L100S, U12-ch91

calib\_packv5\_042523\_0143.root, FC#6, port A1

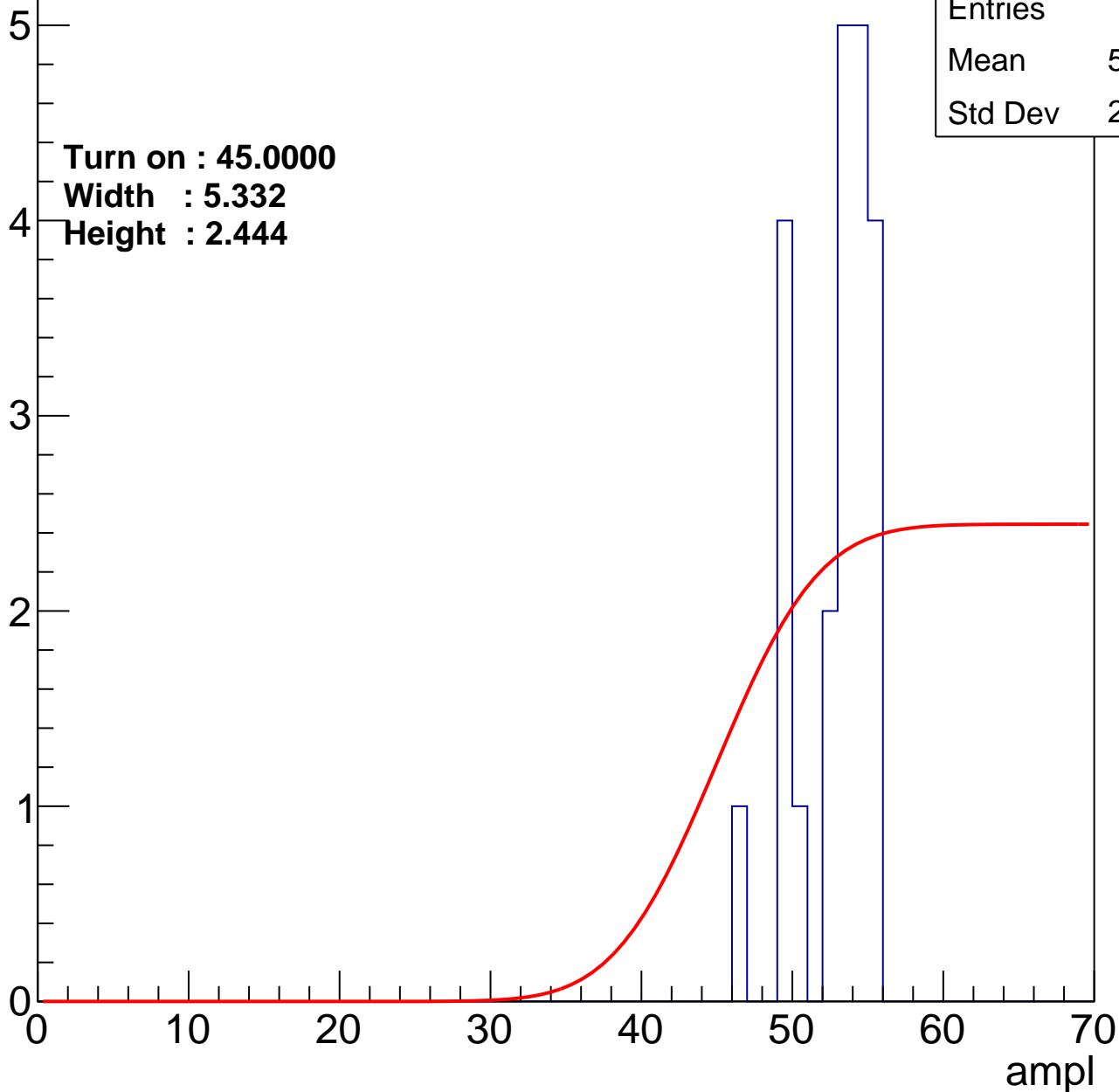
Entry

Entries	22
Mean	52.32
Std Dev	2.475

Turn on : 45.0000

Width : 5.332

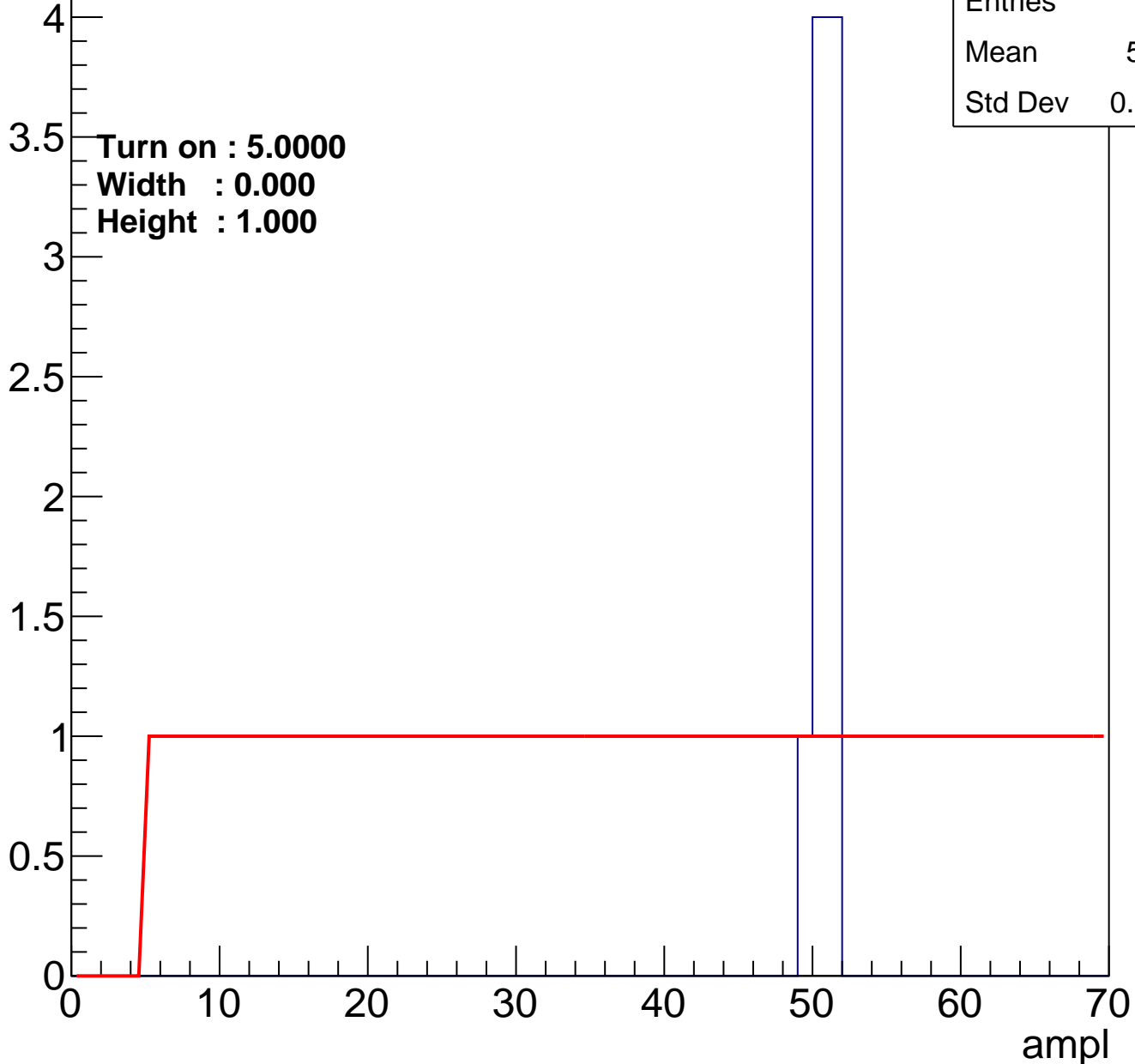
Height : 2.444



# B0L100S, U12-ch92

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U12-ch93

calib\_packv5\_042523\_0143.root, FC#6, port A1

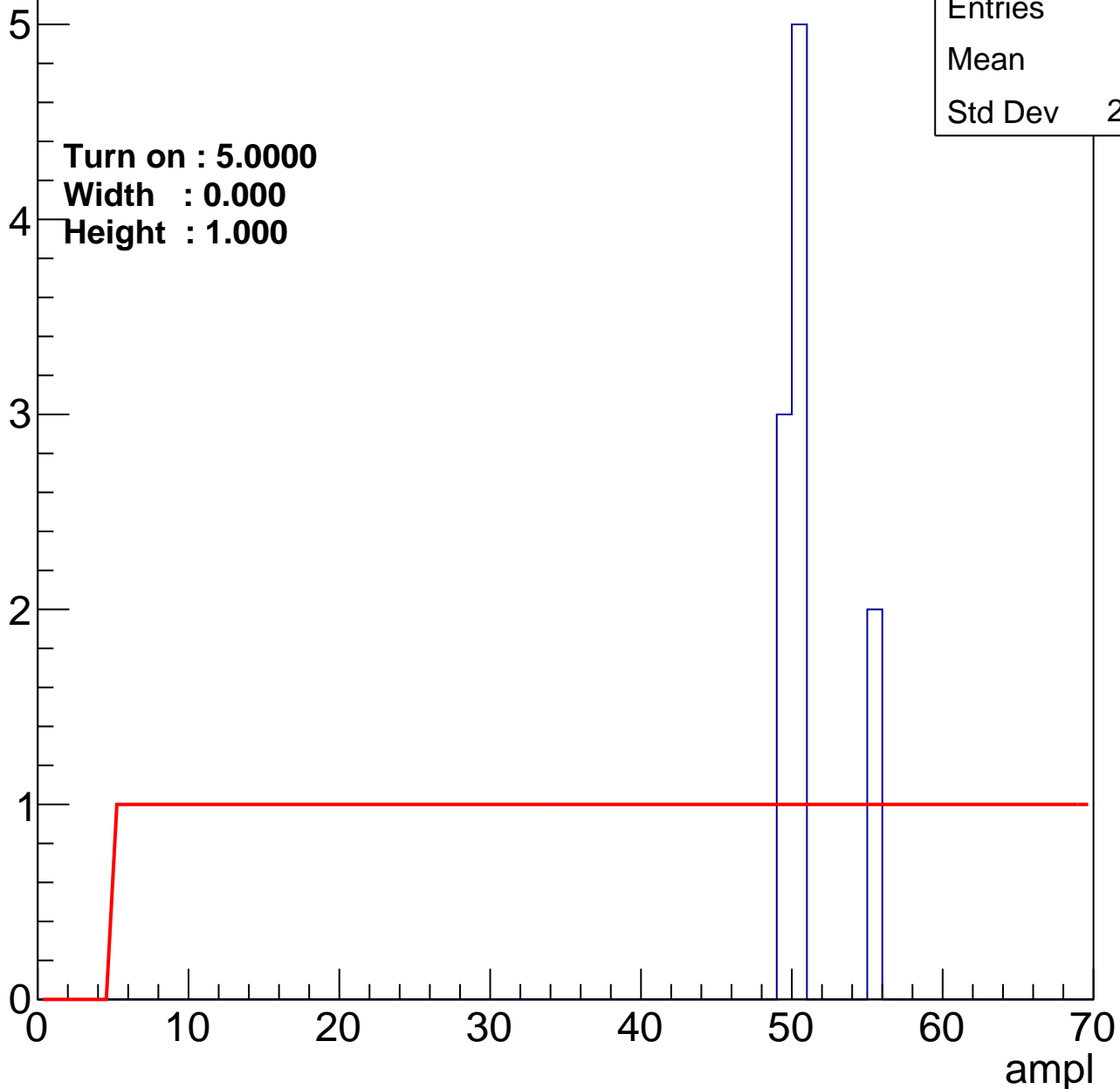
Entry

Entries	10
Mean	50.7
Std Dev	2.193

Turn on : 5.0000

Width : 0.000

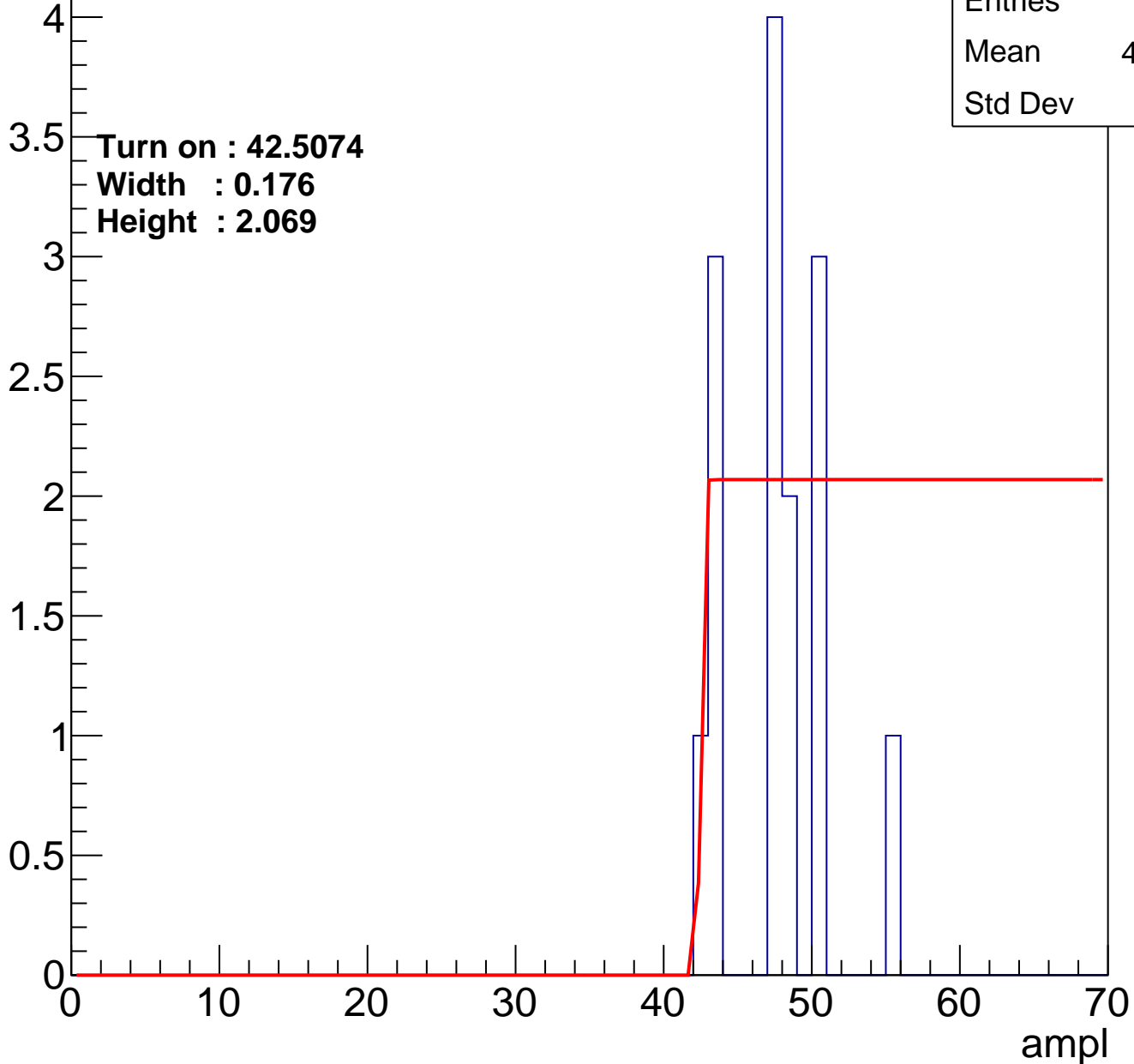
Height : 1.000



# B0L100S, U12-ch94

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry





# B0L100S, U12-ch95

calib\_packv5\_042523\_0143.root, FC#6, port A1

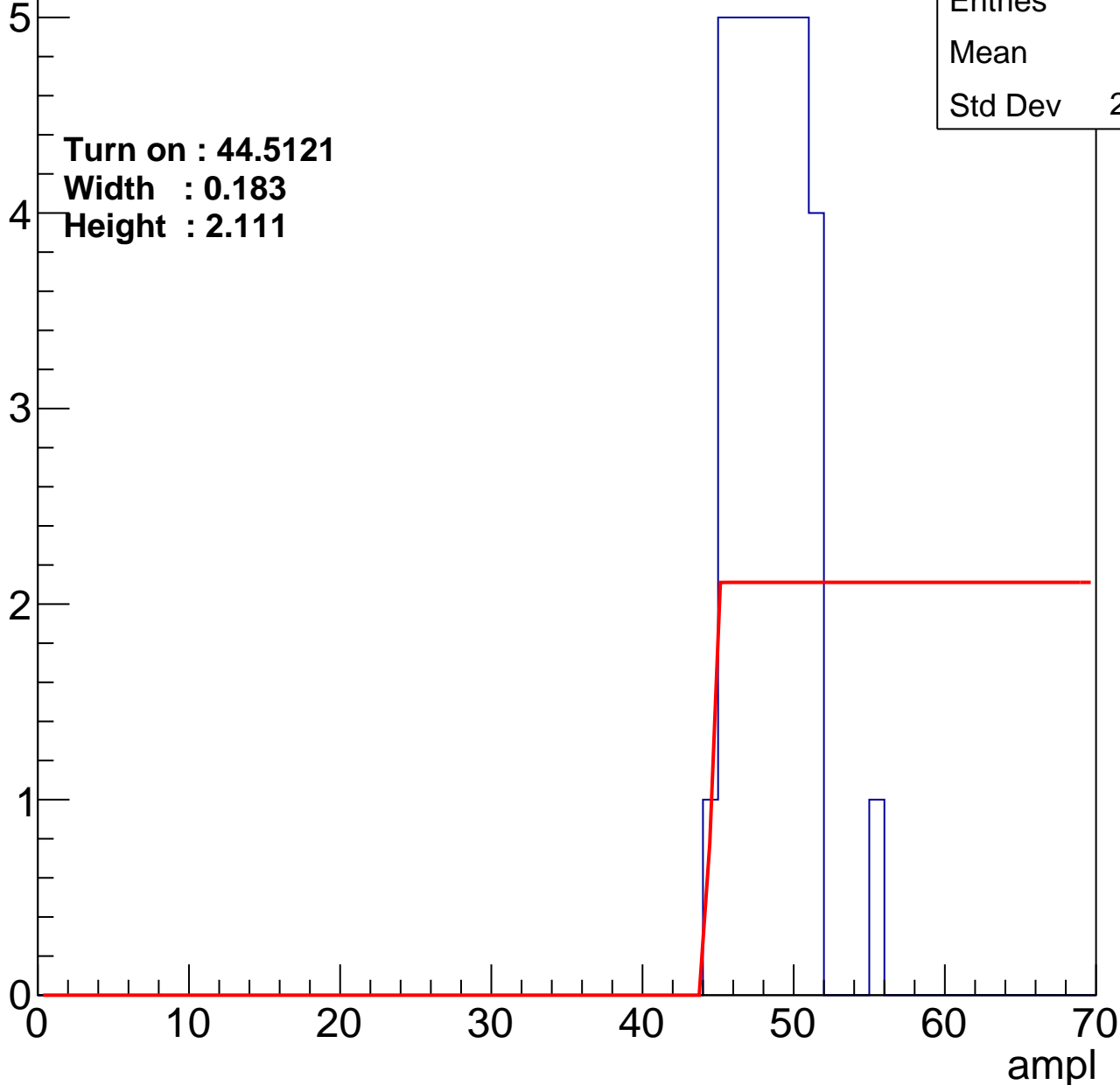
Entry

Entries	36
Mean	48
Std Dev	2.333

Turn on : 44.5121

Width : 0.183

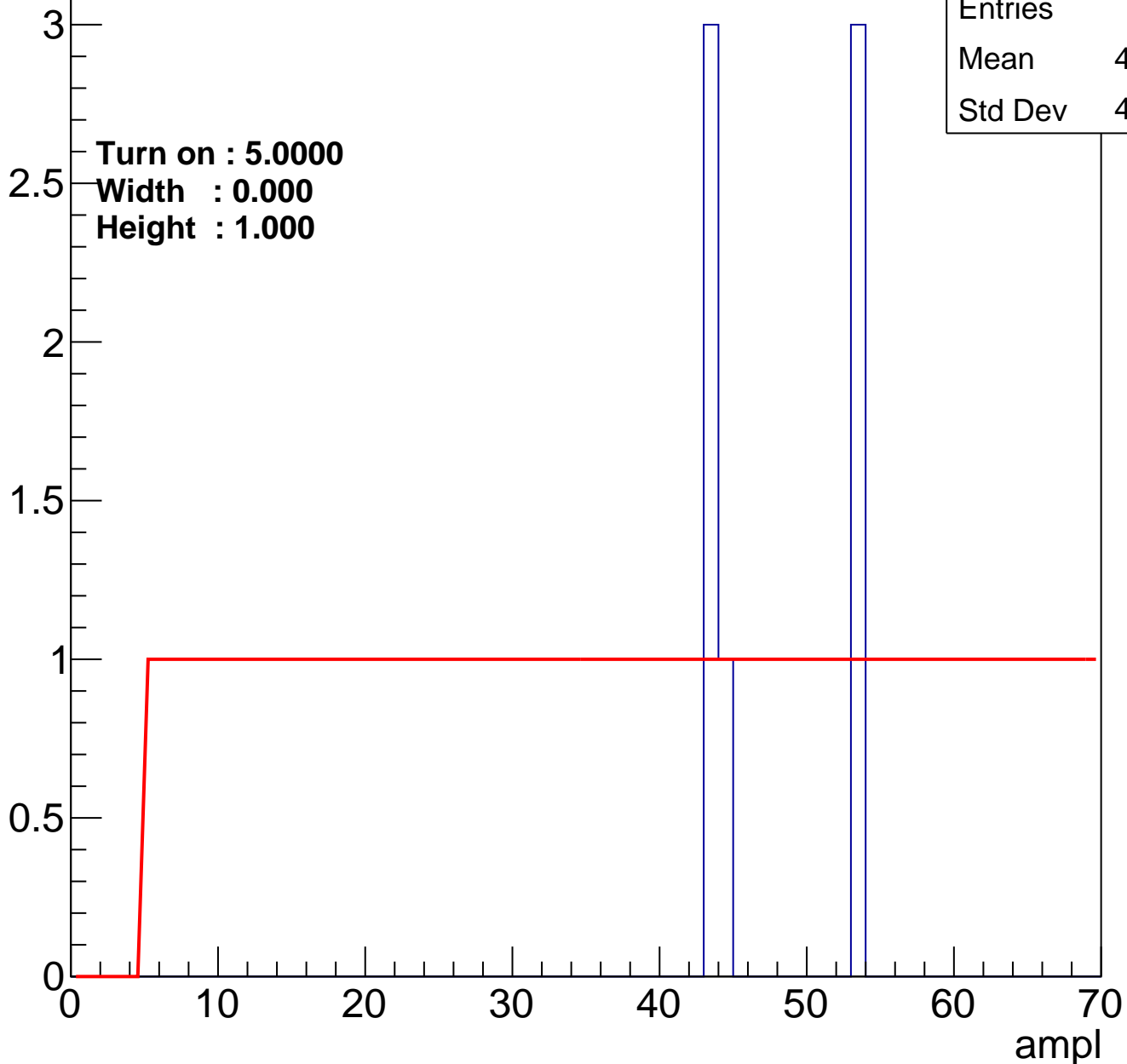
Height : 2.111



# B0L100S, U12-ch96

calib\_packv5\_042523\_0143.root, FC#6, port A1

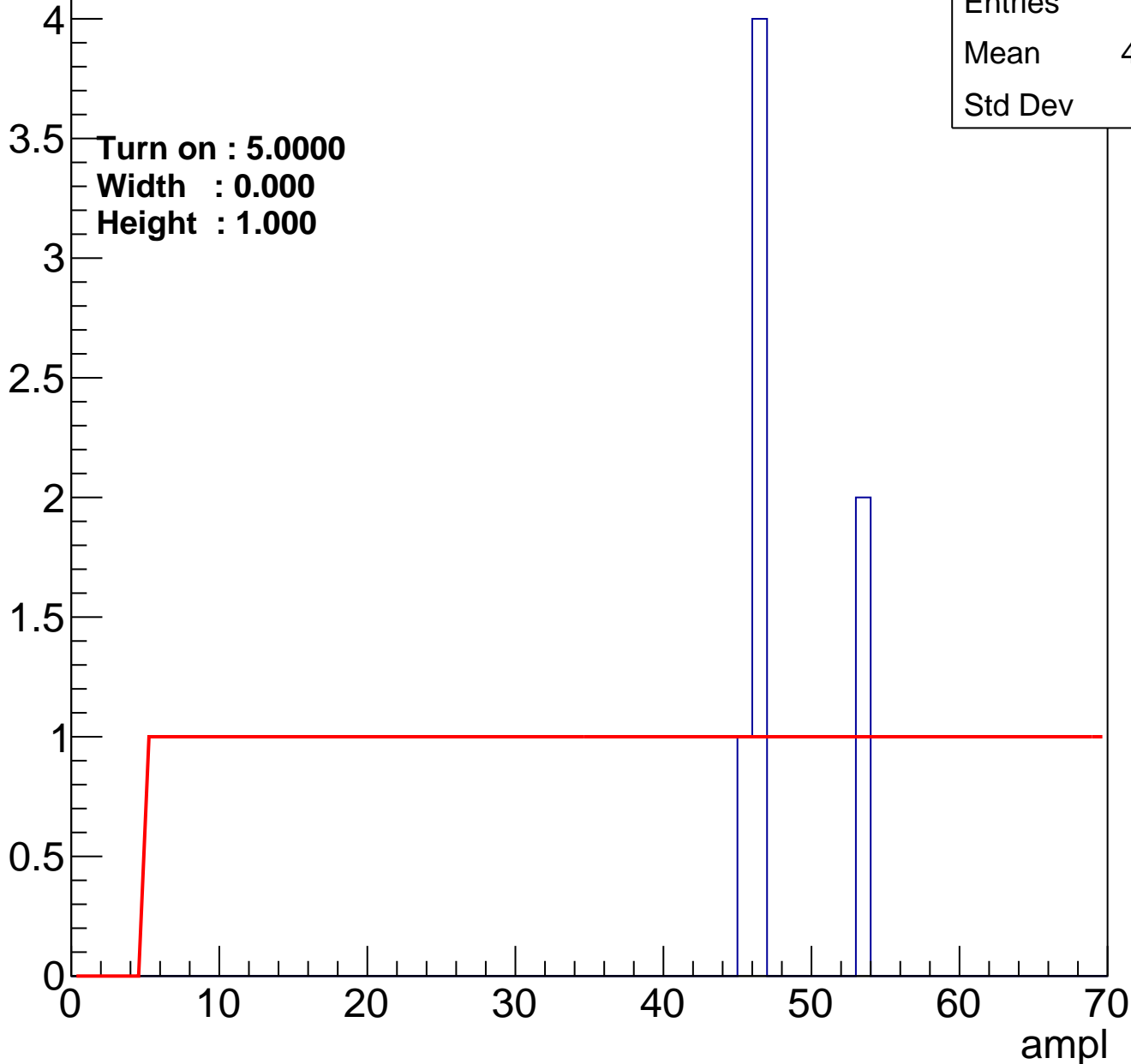
Entry



# B0L100S, U12-ch97

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U12-ch98

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

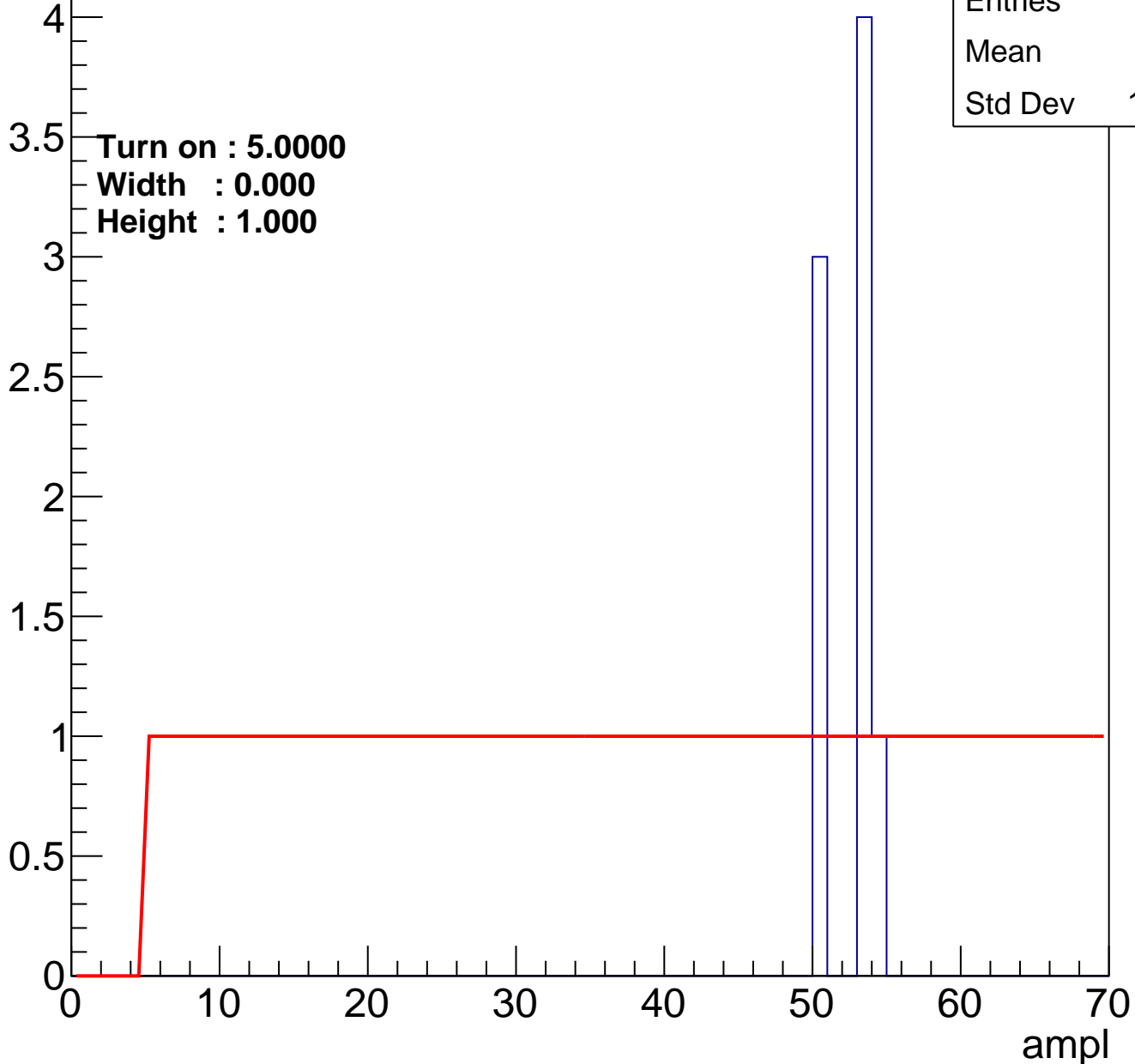


Entries	0
Mean	0
Std Dev	0

# B0L100S, U12-ch99

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Turn on : 5.0000

Width : 0.000

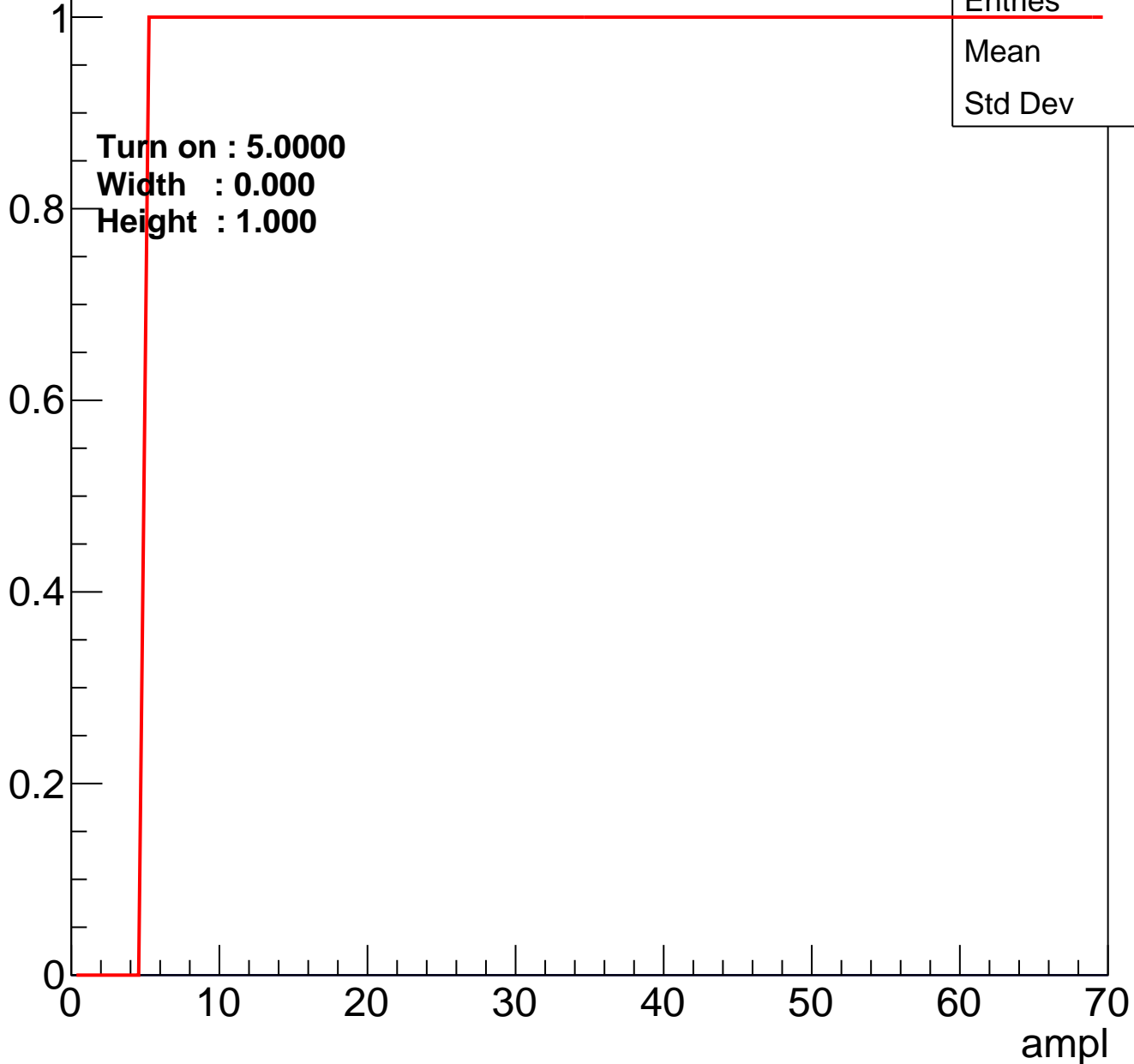
Height : 1.000

Entries	8
Mean	52
Std Dev	1.581

# B0L100S, U12-ch100

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

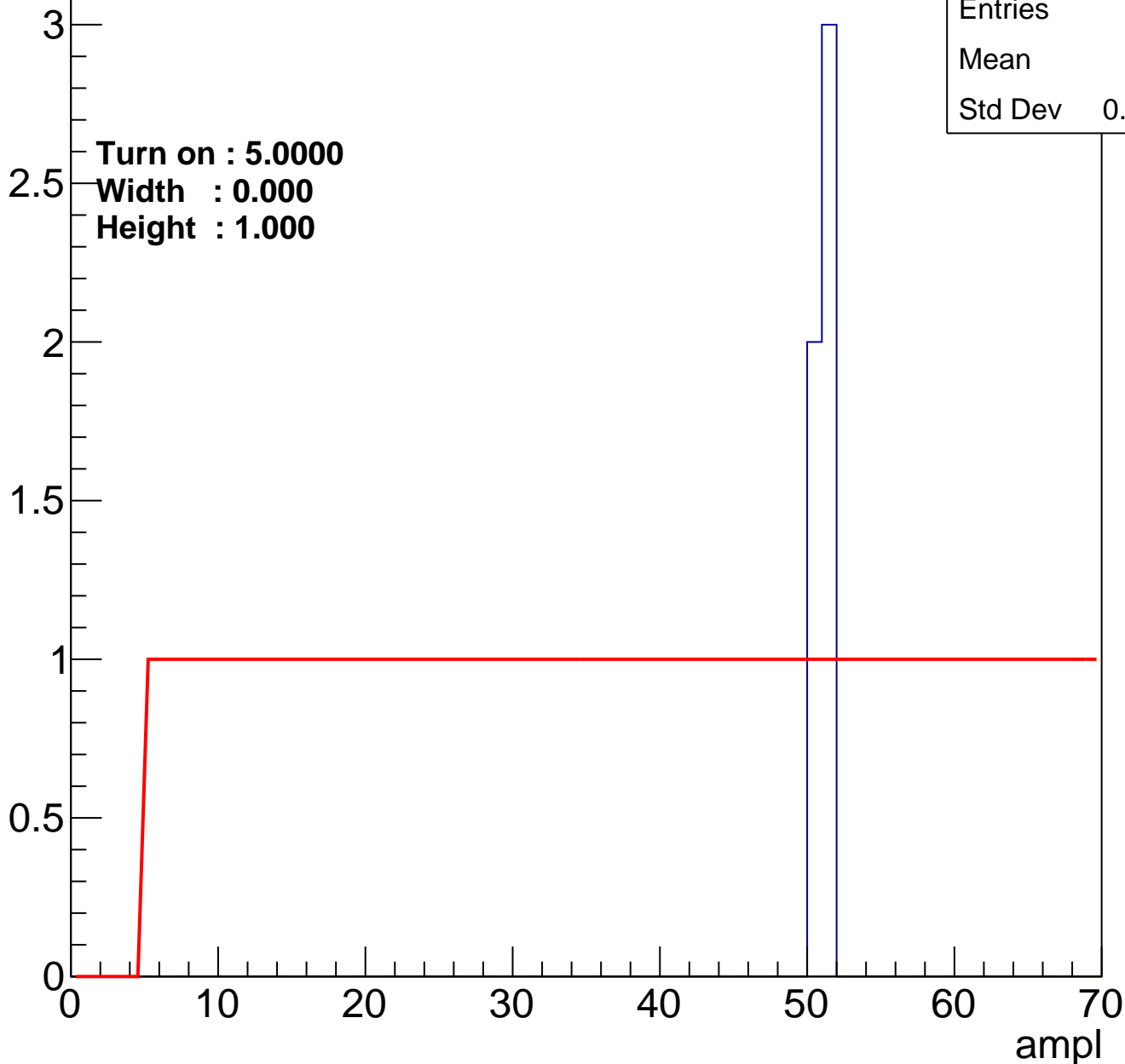


Entries	0
Mean	0
Std Dev	0

# B0L100S, U12-ch101

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U12-ch102

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry





# B0L100S, U12-ch103

calib\_packv5\_042523\_0143.root, FC#6, port A1

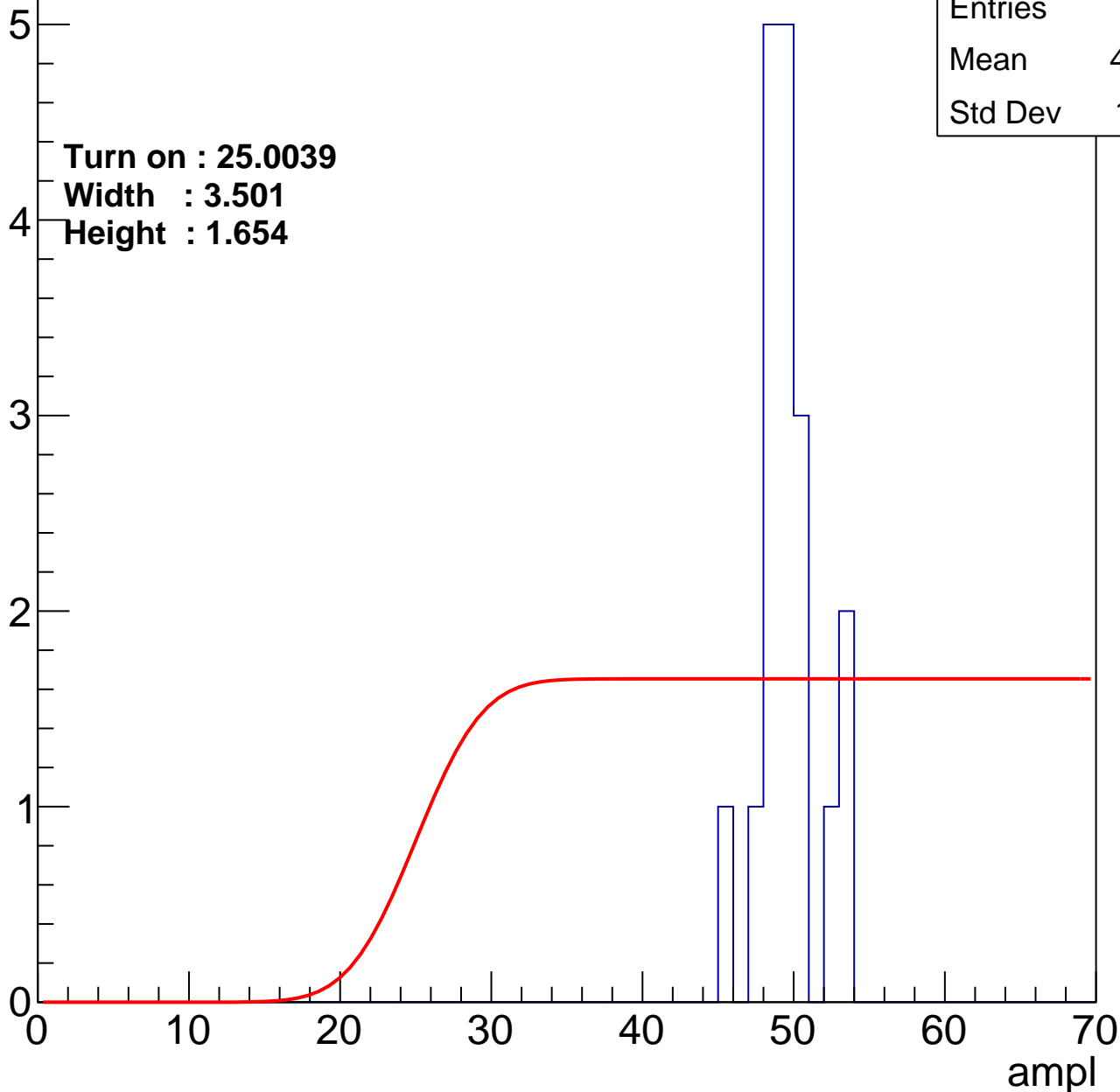
Entry

Entries	18
Mean	49.17
Std Dev	1.951

Turn on : 25.0039

Width : 3.501

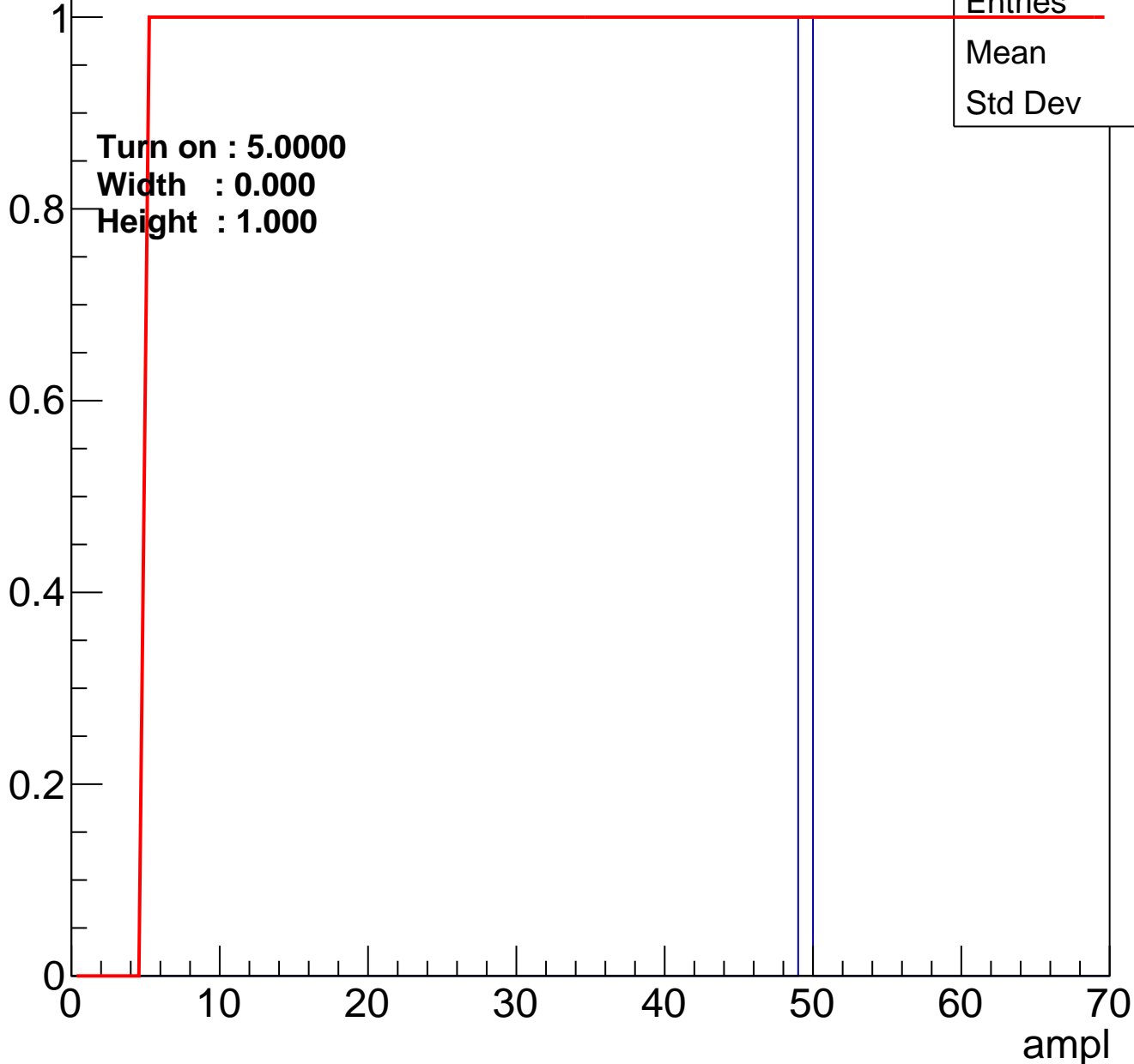
Height : 1.654



# B0L100S, U12-ch104

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U12-ch105

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U12-ch106

calib\_packv5\_042523\_0143.root, FC#6, port A1

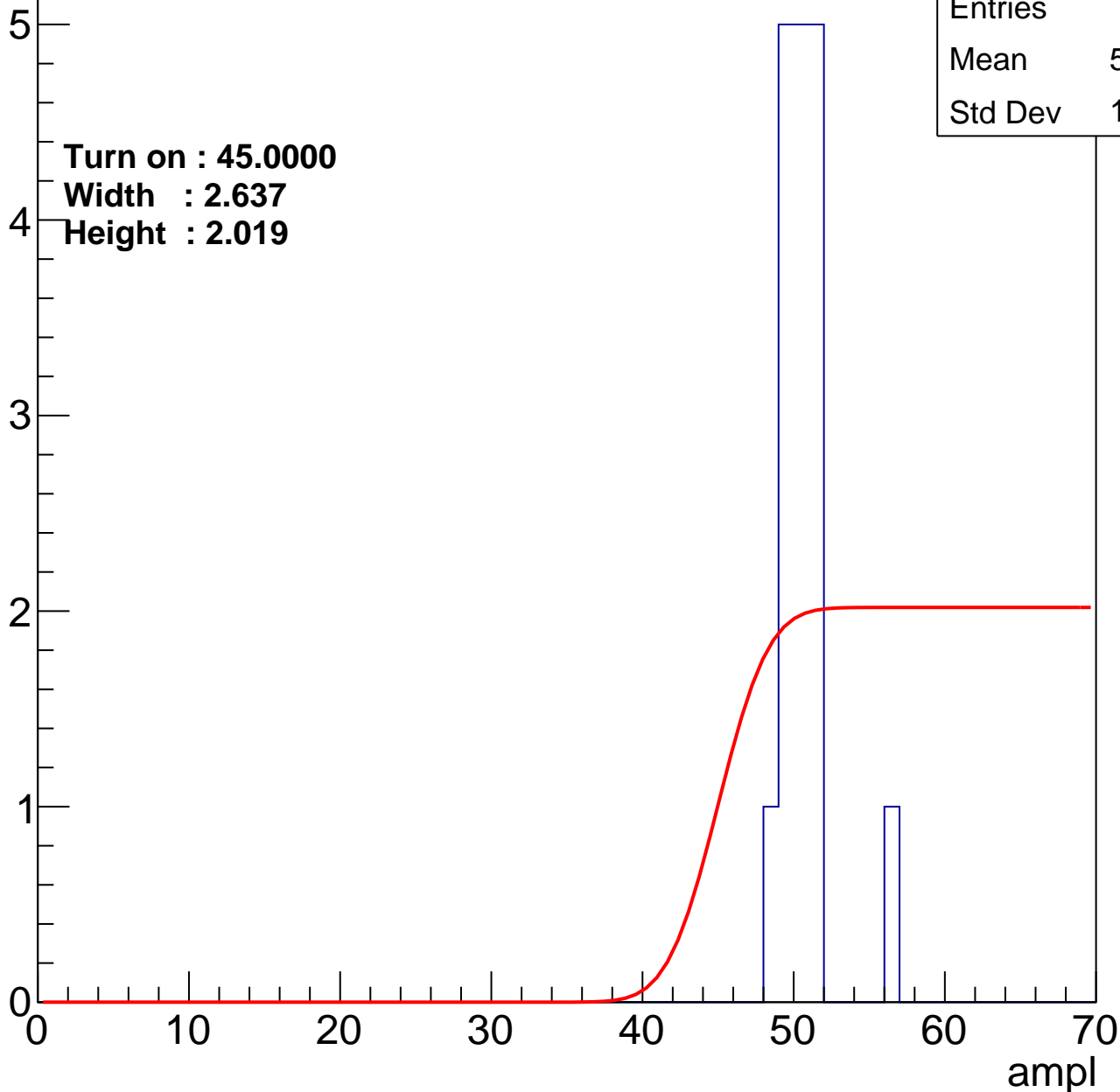
Entry

Entries	17
Mean	50.24
Std Dev	1.699

Turn on : 45.0000

Width : 2.637

Height : 2.019



# B0L100S, U12-ch107

calib\_packv5\_042523\_0143.root, FC#6, port A1

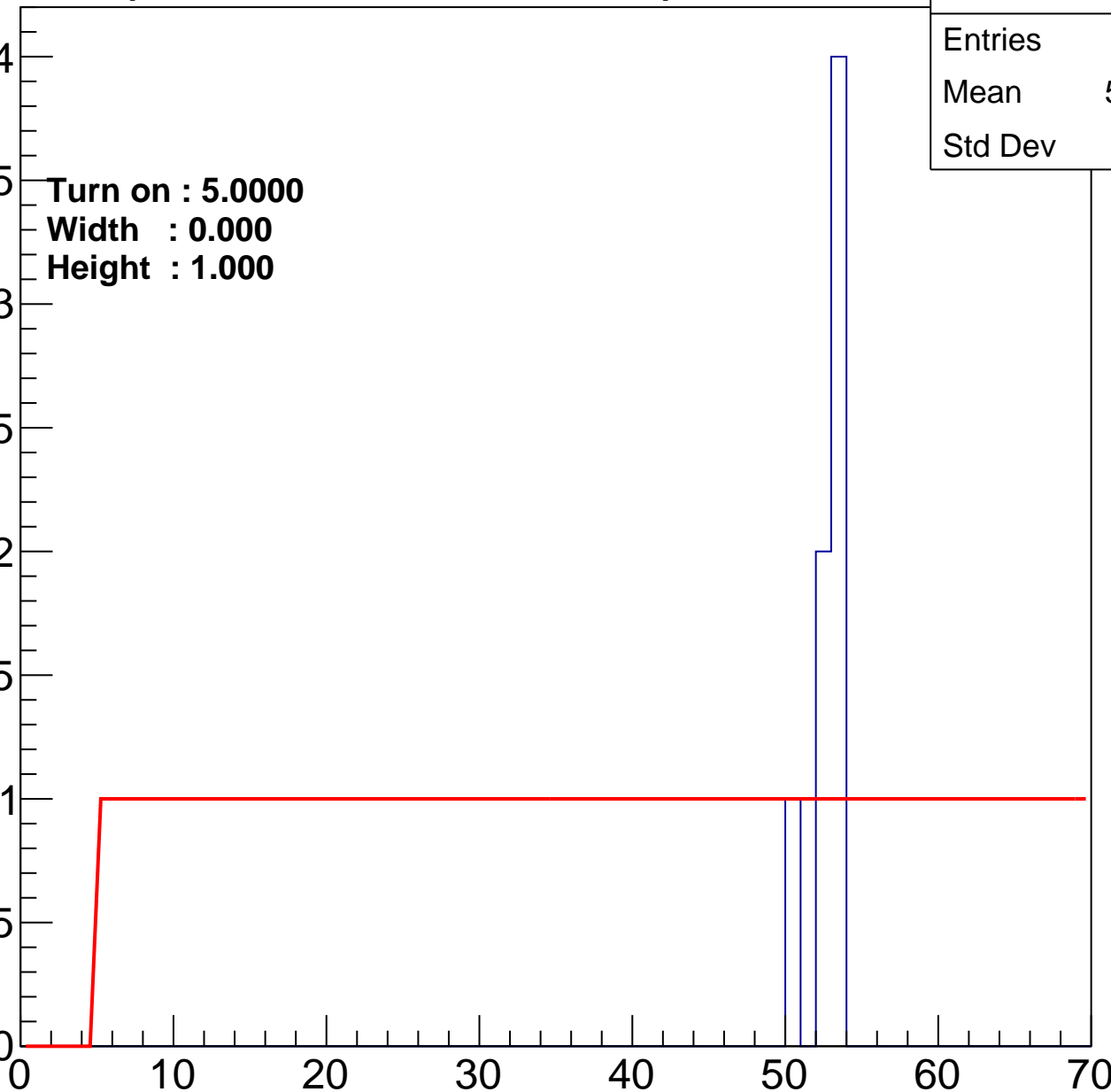
Entry

4  
3.5  
3  
2.5  
2  
1.5  
1  
0.5  
0

Turn on : 5.0000  
Width : 0.000  
Height : 1.000

Entries	7
Mean	52.29
Std Dev	1.03

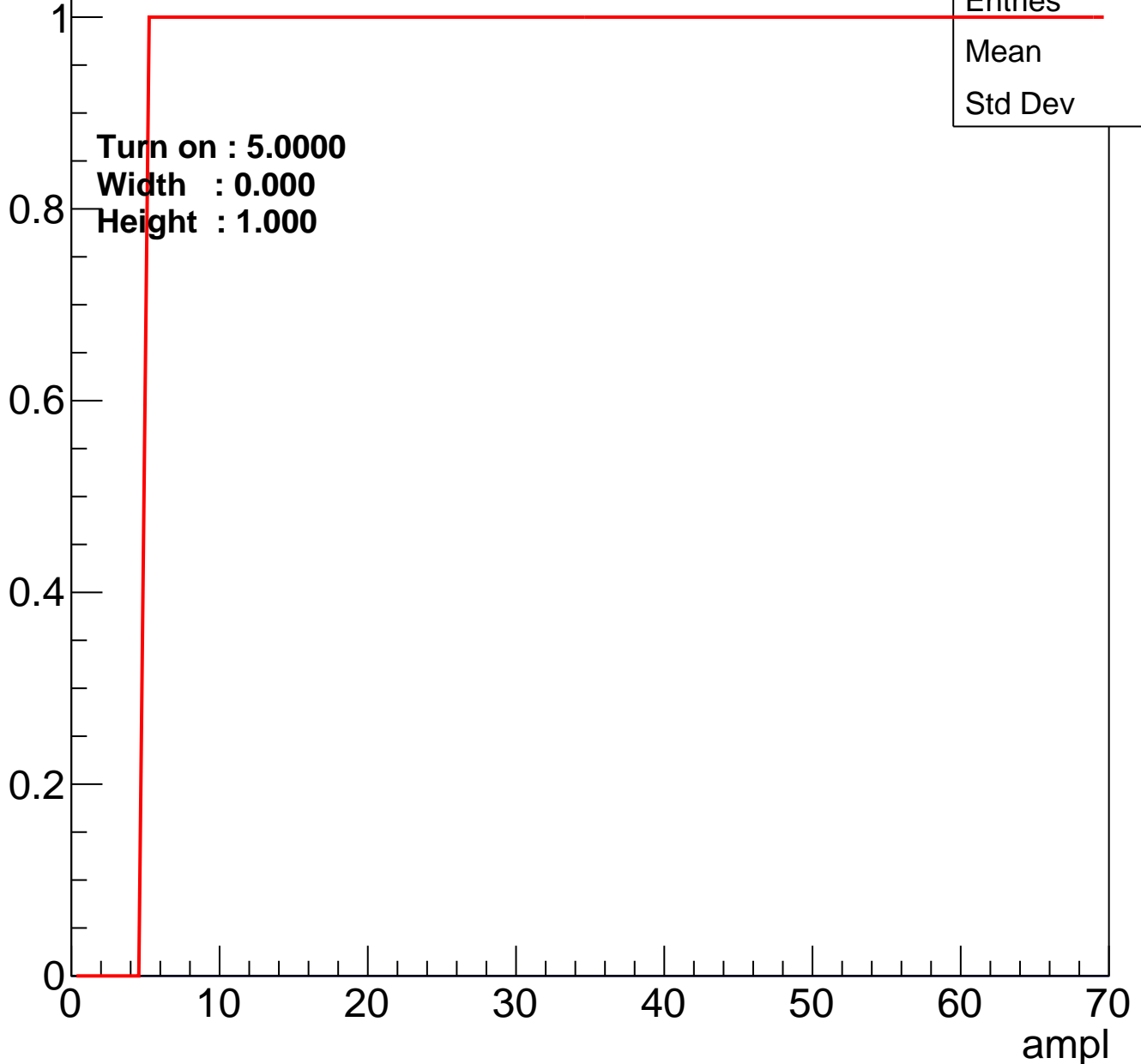
ampl



# B0L100S, U12-ch108

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U12-ch109

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U12-ch110

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L100S, U12-ch111

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U12-ch112

calib\_packv5\_042523\_0143.root, FC#6, port A1

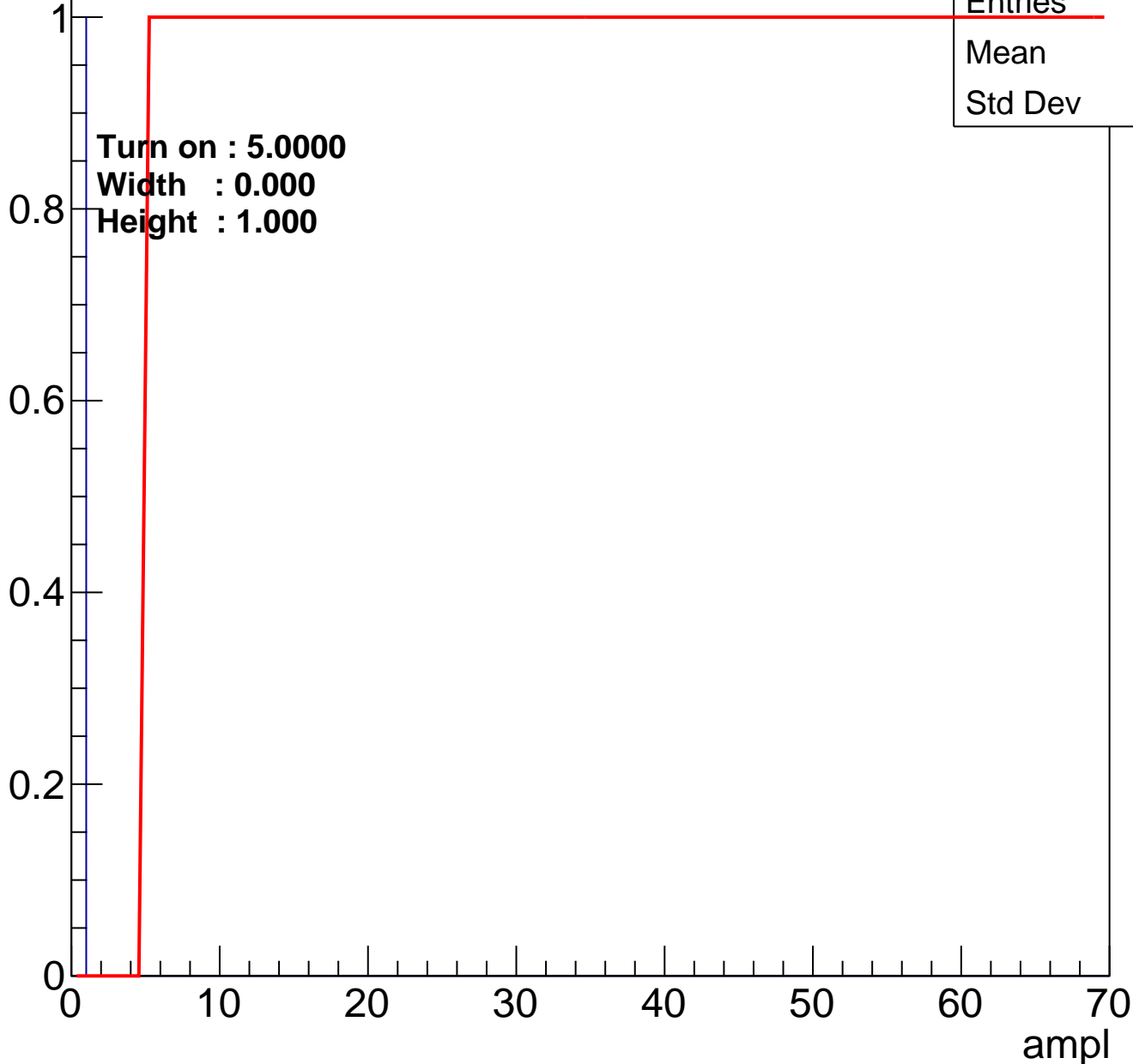
Entry



# B0L100S, U12-ch113

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L100S, U12-ch114

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

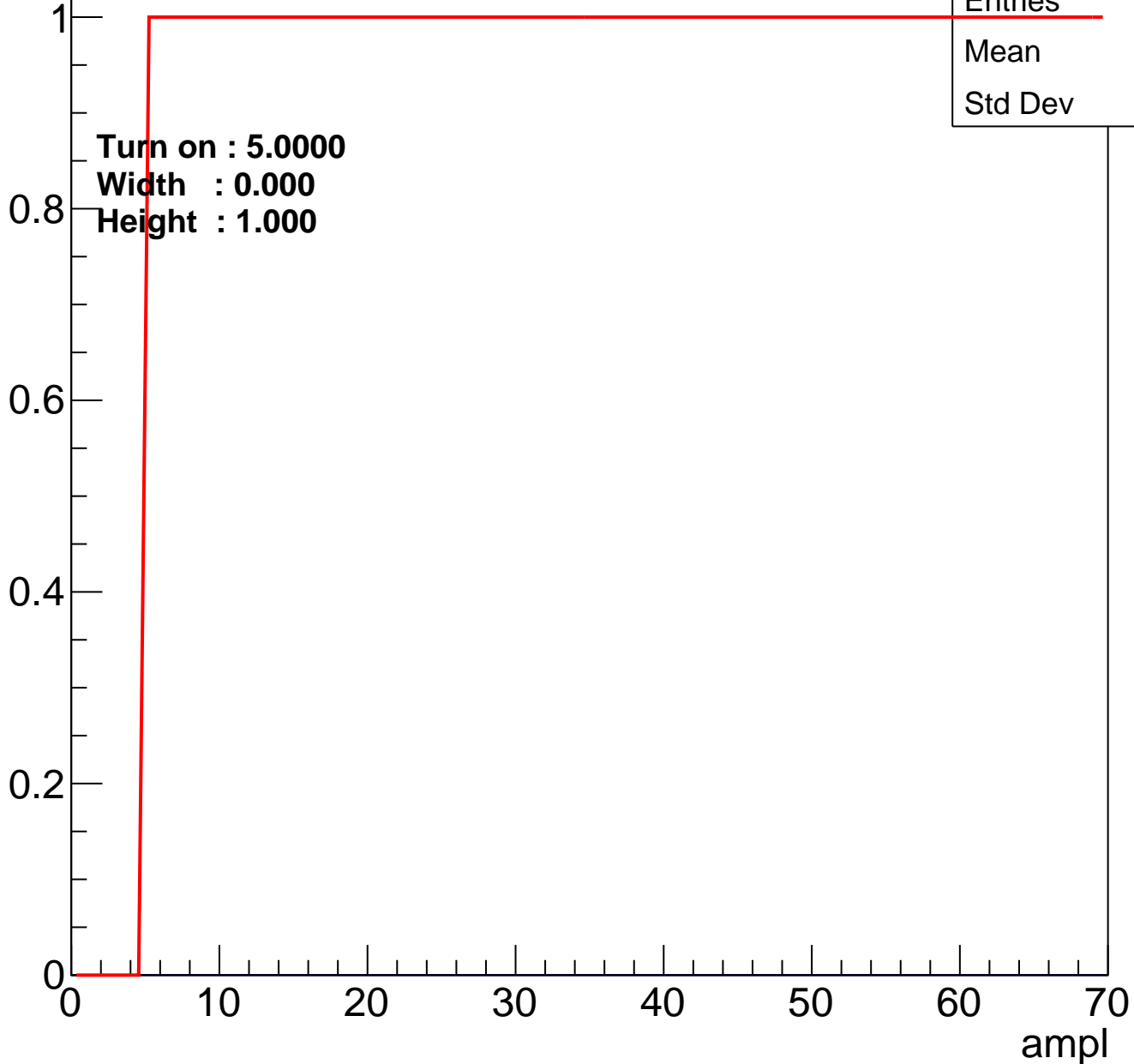


Entries	0
Mean	0
Std Dev	0

# B0L100S, U12-ch115

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U12-ch116

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U12-ch117

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L100S, U12-ch118

calib\_packv5\_042523\_0143.root, FC#6, port A1

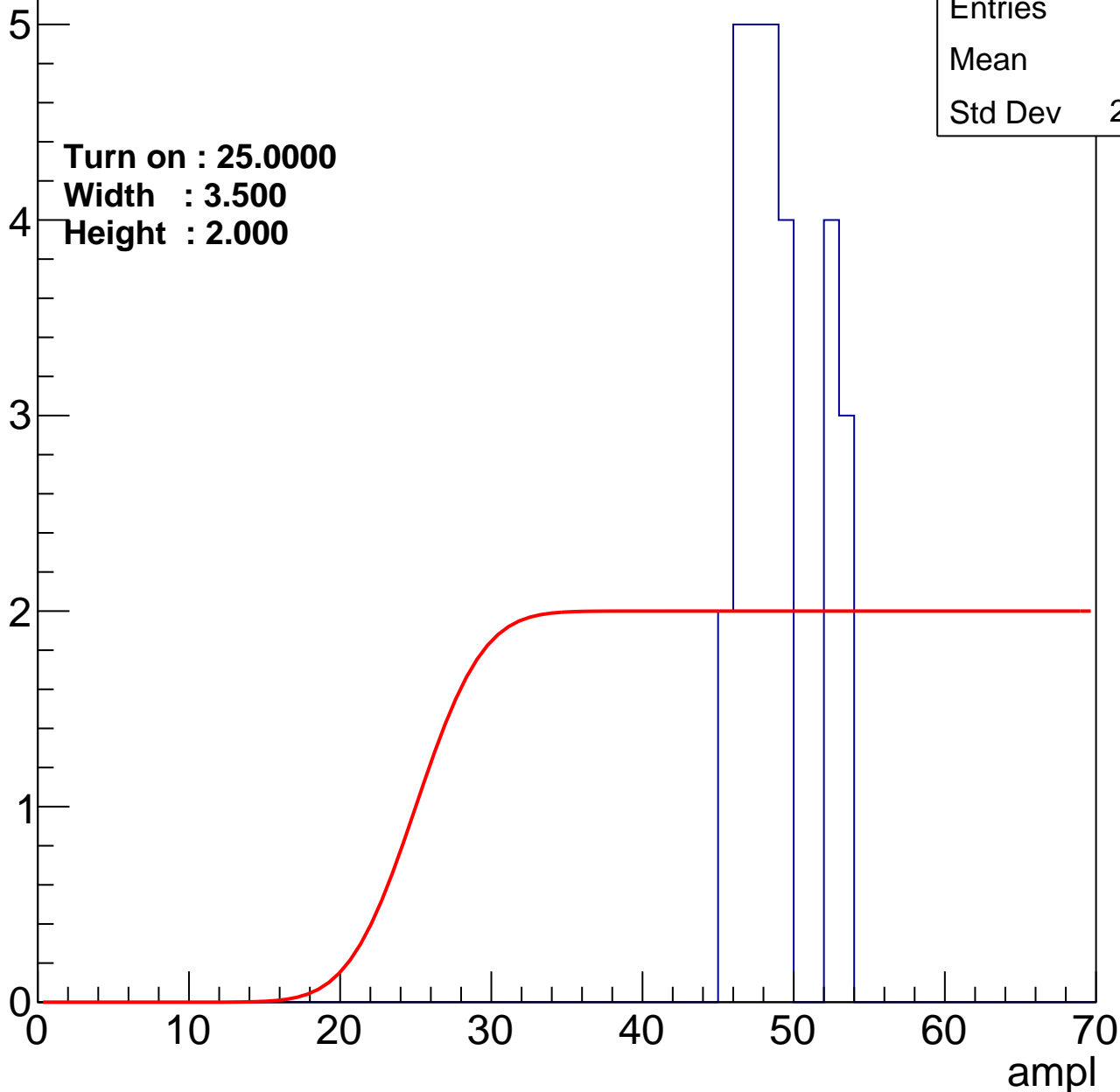
Entry

Entries	28
Mean	48.5
Std Dev	2.528

Turn on : 25.0000

Width : 3.500

Height : 2.000





# B0L100S, U12-ch119

calib\_packv5\_042523\_0143.root, FC#6, port A1

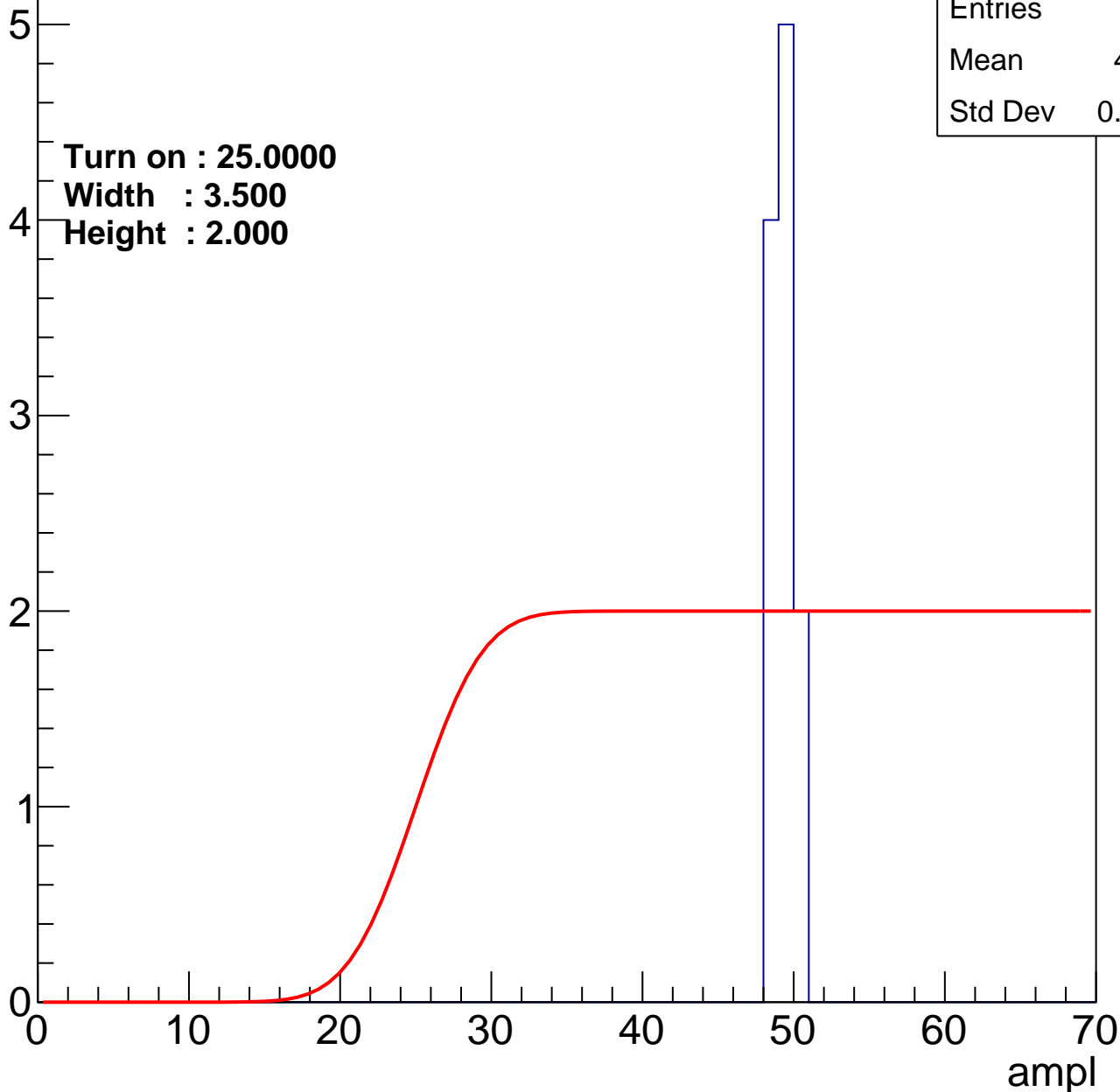
Entry

Entries	11
Mean	48.82
Std Dev	0.7158

Turn on : 25.0000

Width : 3.500

Height : 2.000



# B0L100S, U12-ch120

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

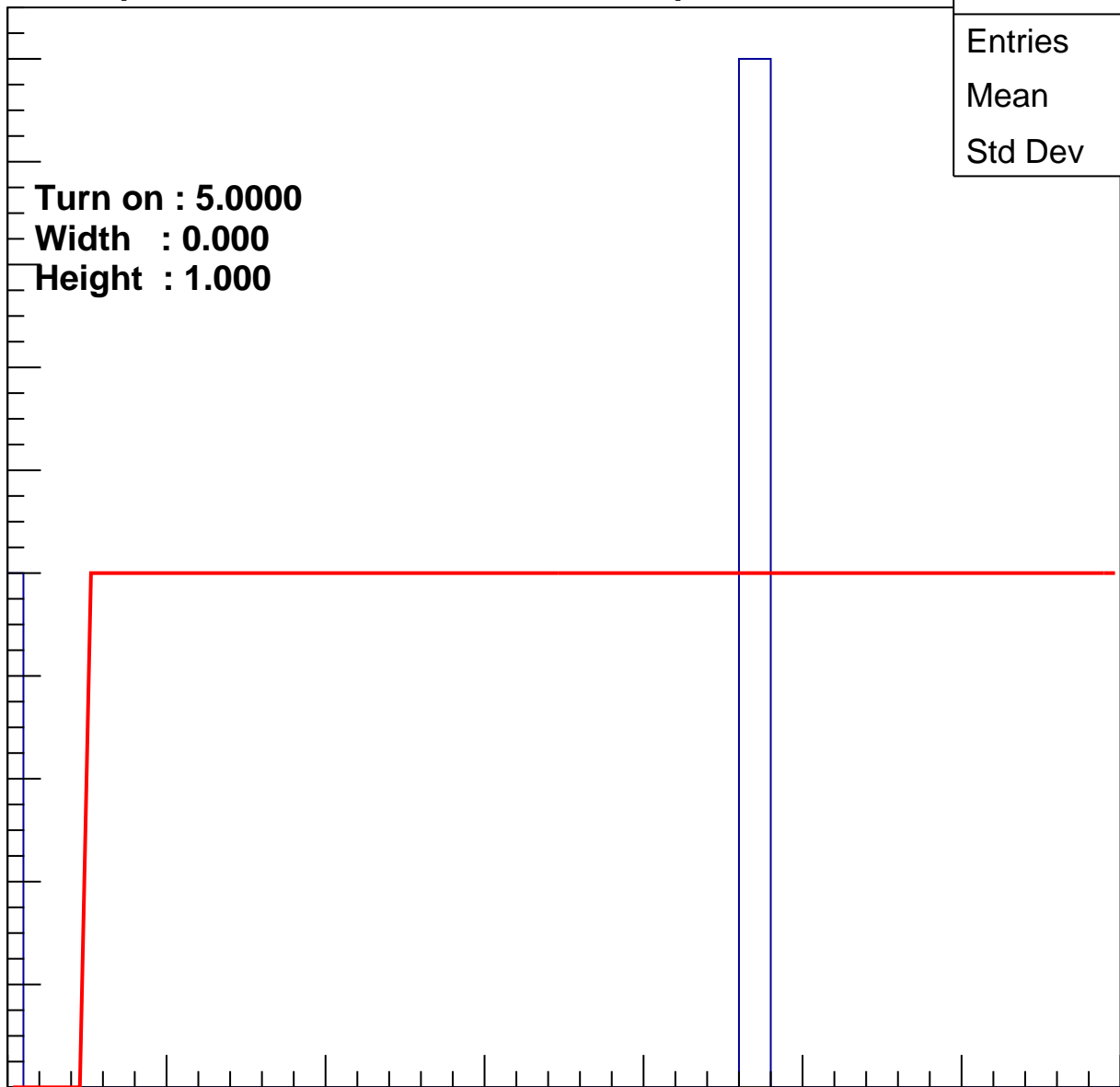
2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Turn on : 5.0000  
Width : 0.000  
Height : 1.000

Entries	5
Mean	37.2
Std Dev	18.61

0 10 20 30 40 50 60 70

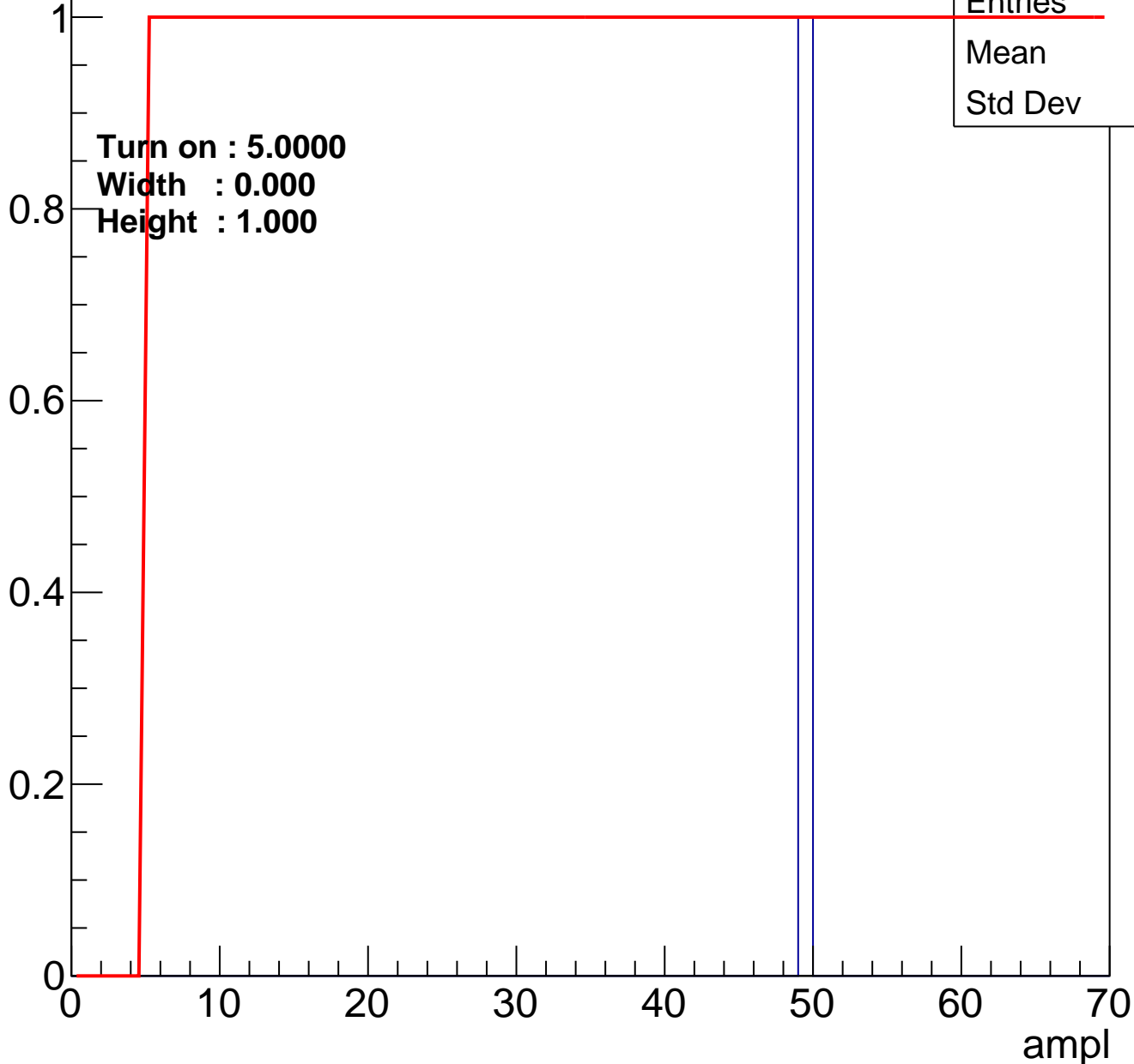
ampl



# B0L100S, U12-ch121

calib\_packv5\_042523\_0143.root, FC#6, port A1

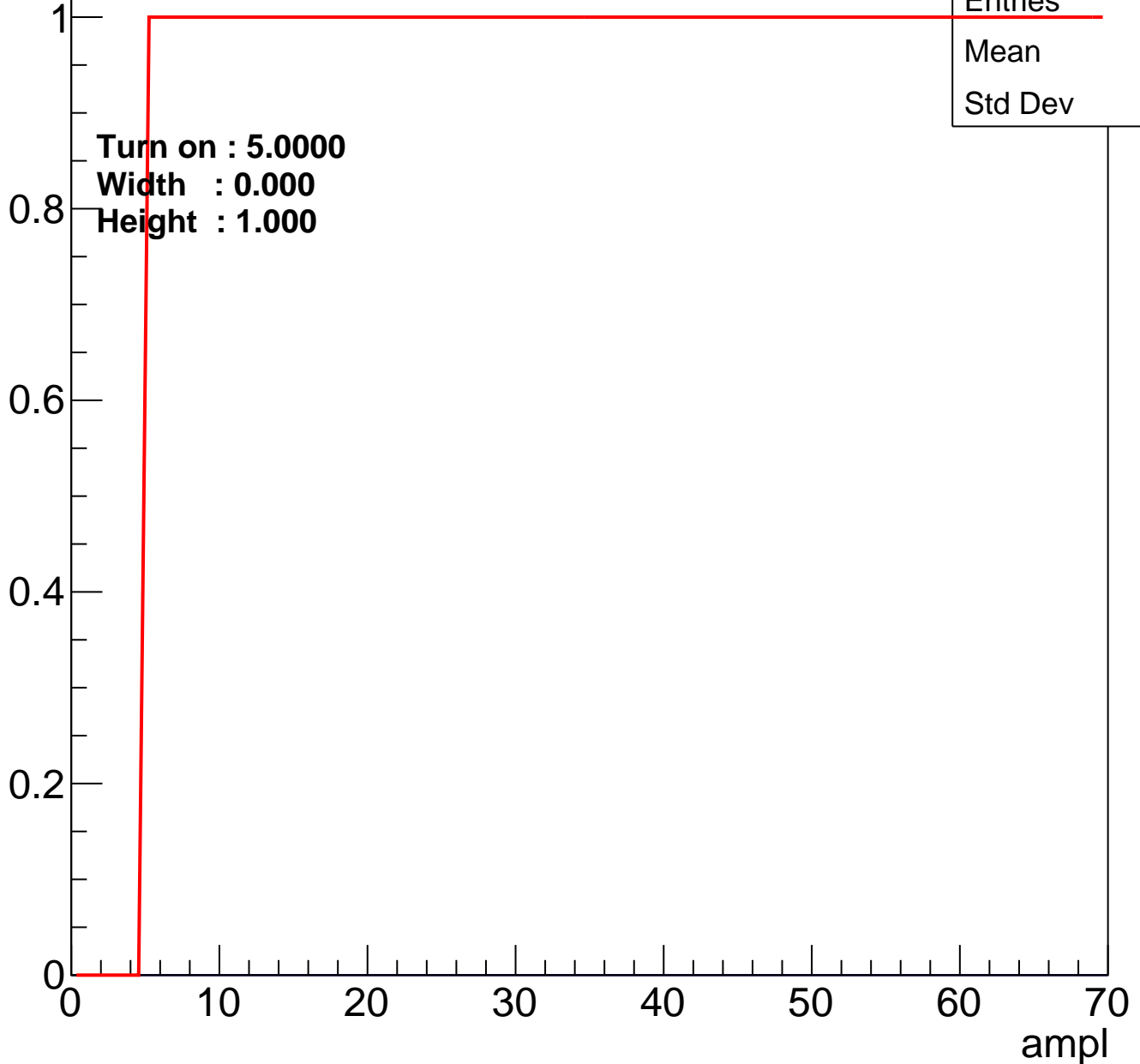
Entry



# B0L100S, U12-ch122

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U12-ch123

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

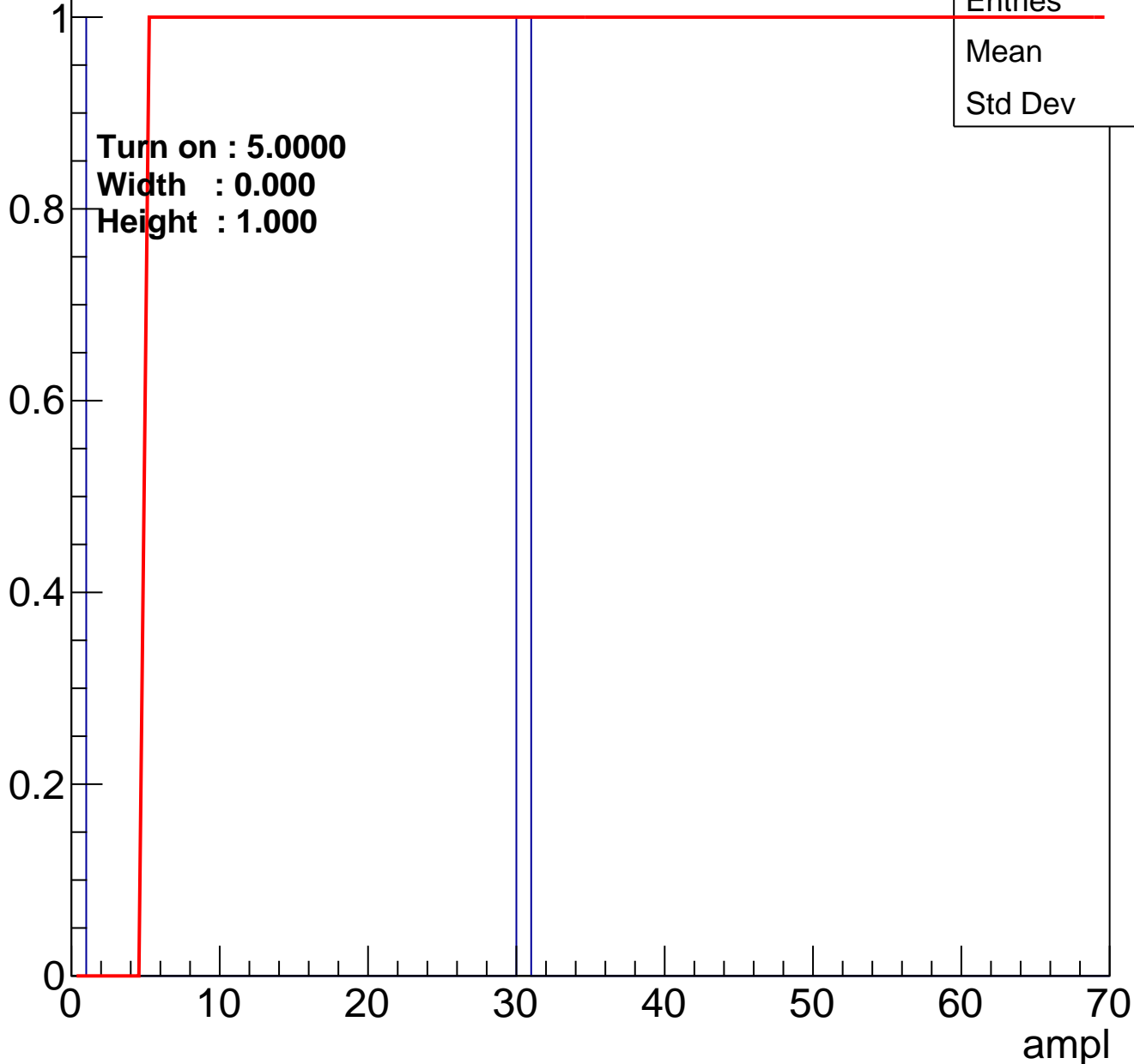


Entries	0
Mean	0
Std Dev	0

# B0L100S, U12-ch124

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



# B0L100S, U12-ch125

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

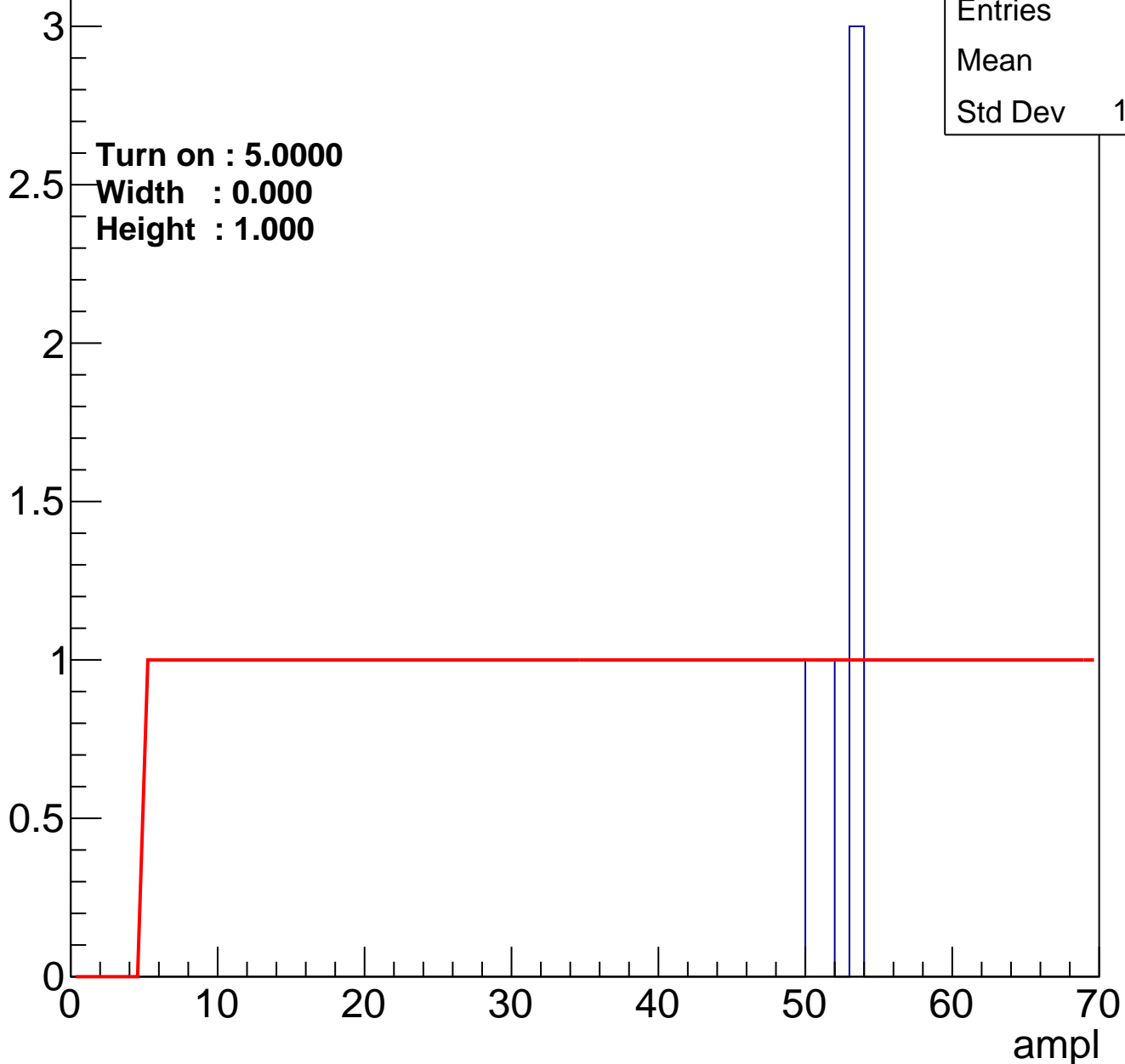


Entries	0
Mean	0
Std Dev	0

# B0L100S, U12-ch126

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



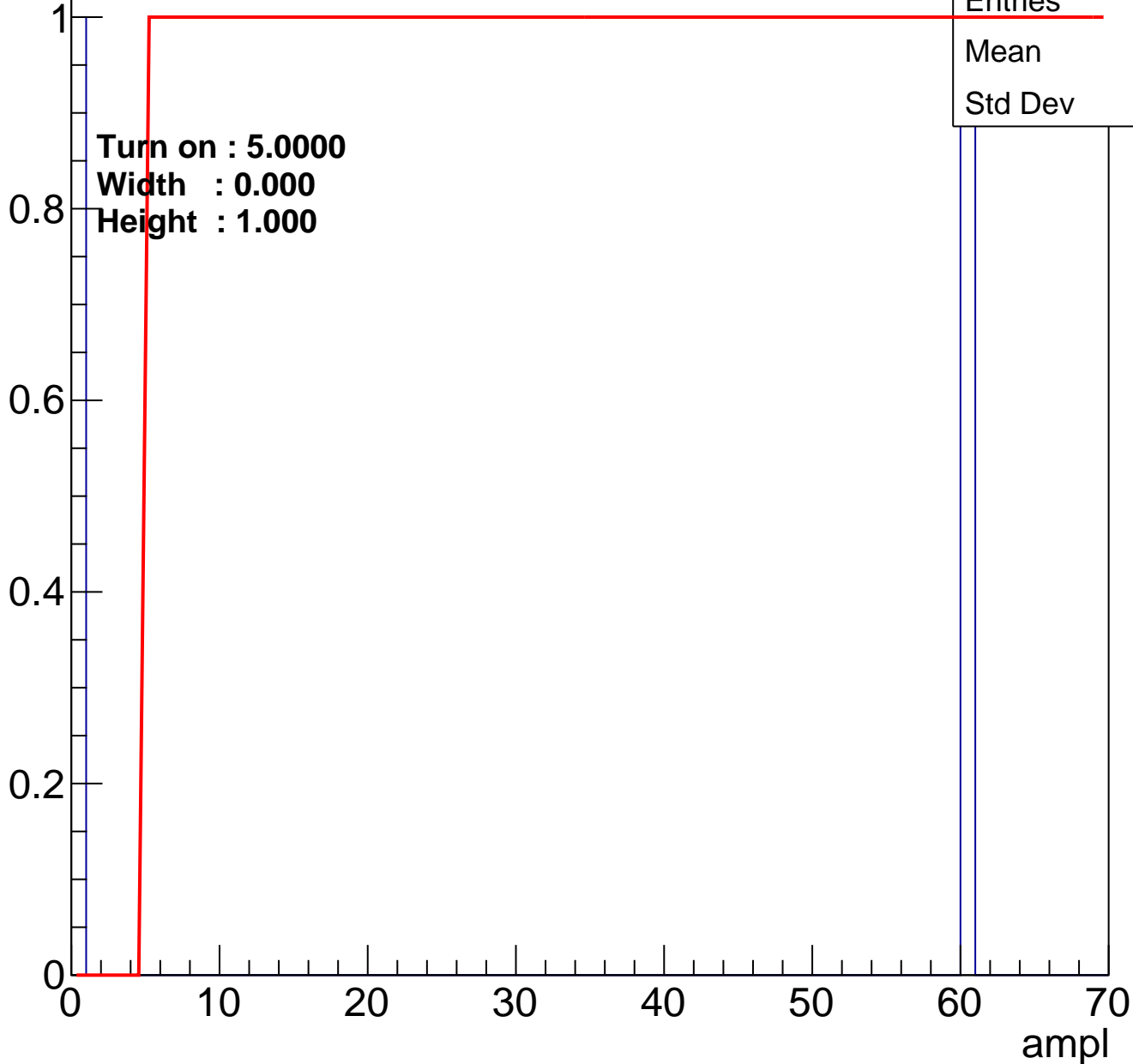
Entries	5
Mean	52
Std Dev	1.265



# B0L100S, U12-ch127

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry

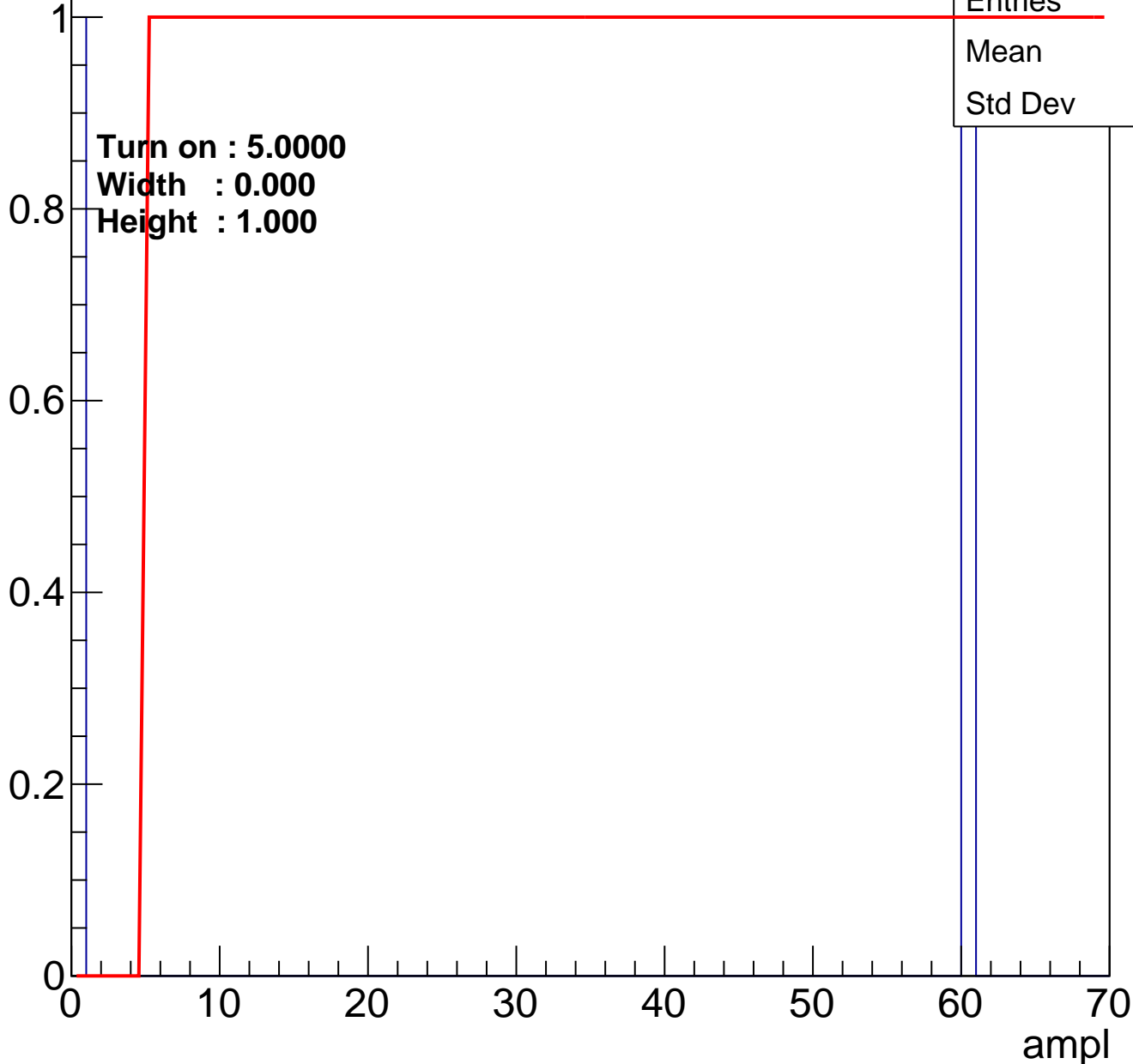


Entries	2
Mean	30
Std Dev	30

# B0L100S, U12-ch127

calib\_packv5\_042523\_0143.root, FC#6, port A1

Entry



Entries	2
Mean	30
Std Dev	30