

B1L103S, U8-ch0

calib_packv5_041523_1651.root, FC#0, port C2

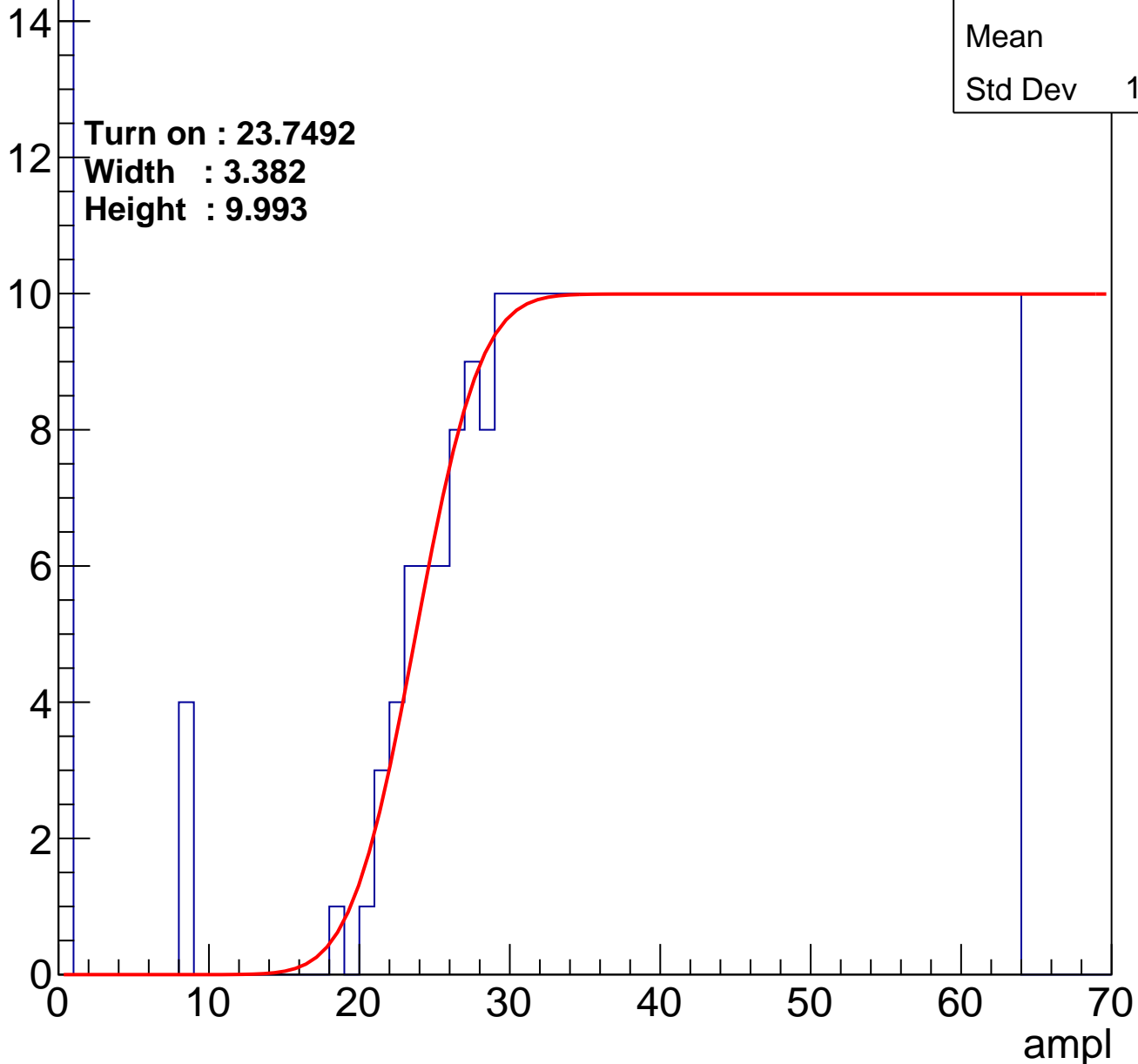
Entry

Entries	461
Mean	37.8
Std Dev	18.06

Turn on : 23.7492

Width : 3.382

Height : 9.993



B1L103S, U8-ch1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	410
Mean	40.56
Std Dev	16.76

Turn on : 27.1129

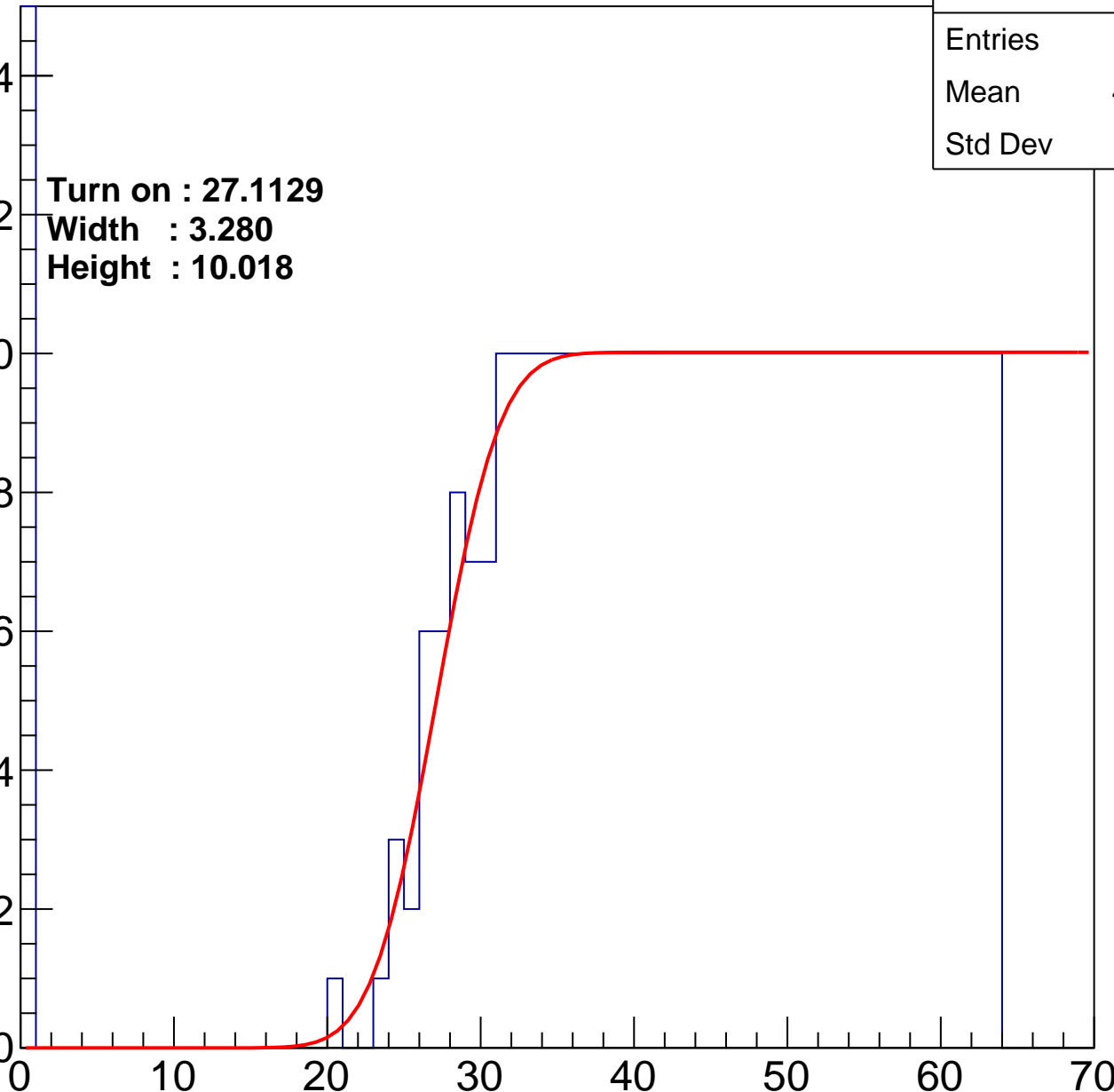
Width : 3.280

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	39.45
Std Dev	17.26

Turn on : 25.5464

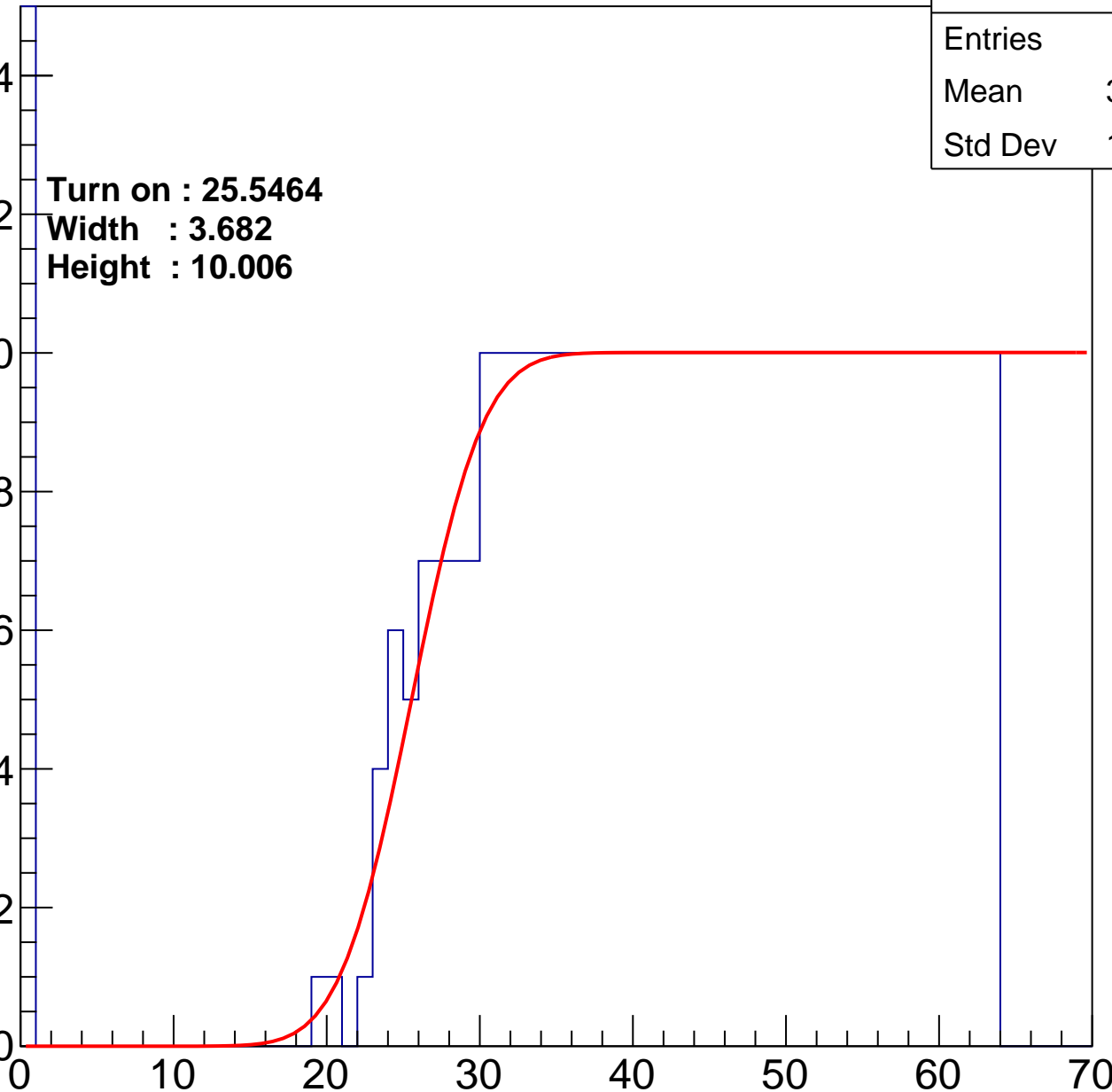
Width : 3.682

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	40.4
Std Dev	16.49

Turn on : 26.3835

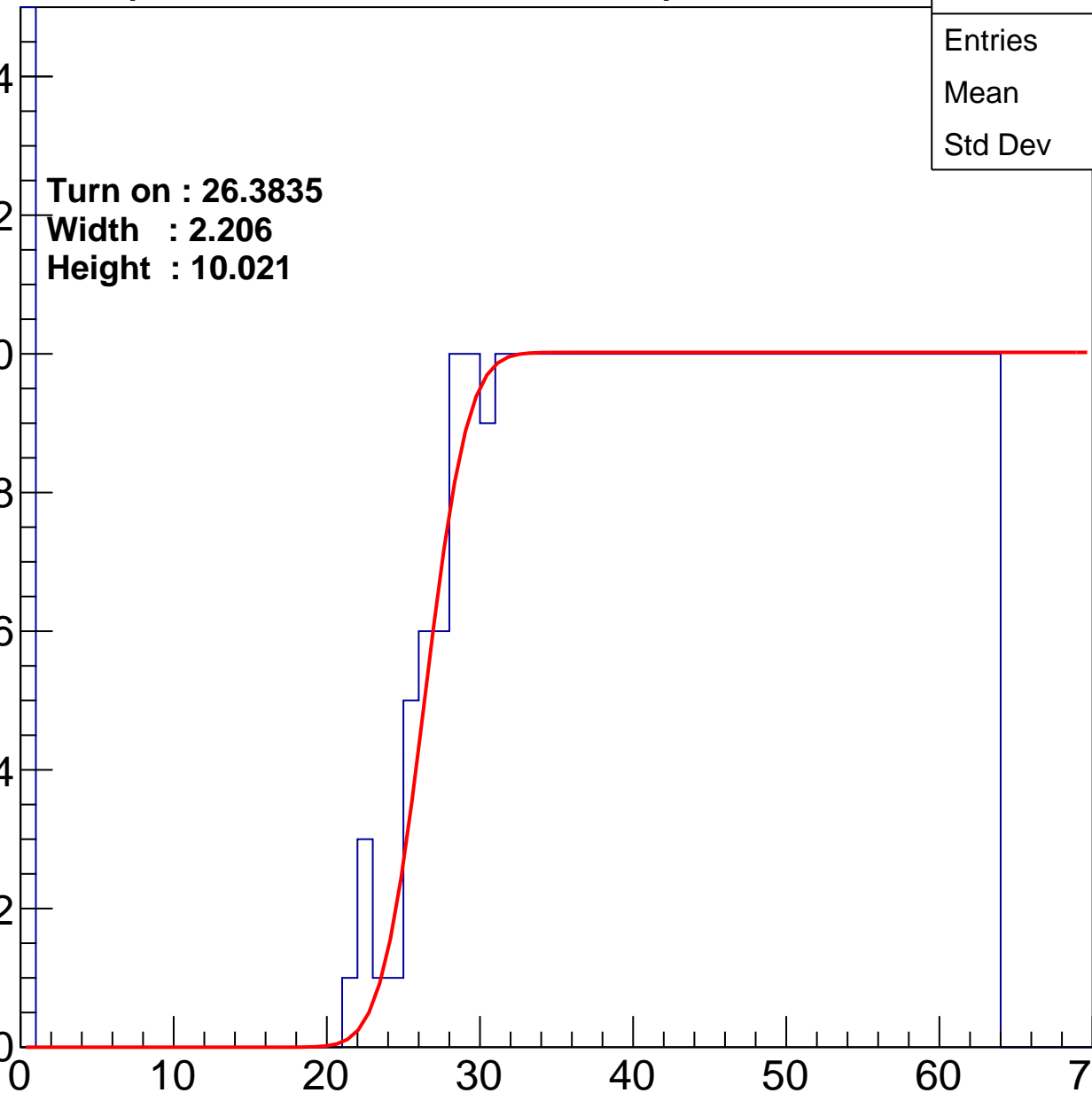
Width : 2.206

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch4

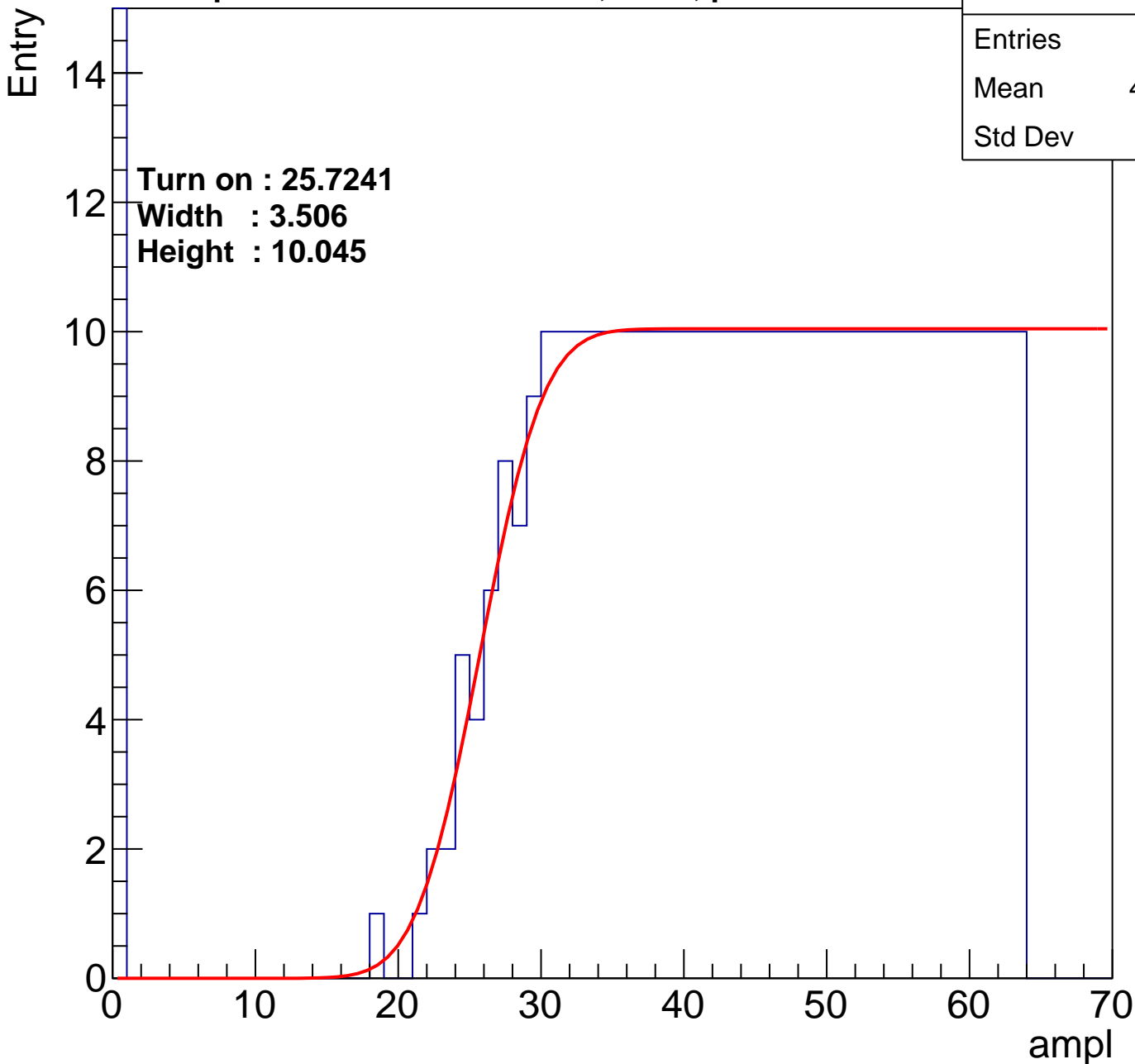
calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	40.16
Std Dev	16.61

Turn on : 25.7241

Width : 3.506

Height : 10.045



B1L103S, U8-ch5

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.21
Std Dev	17.84

Turn on : 26.4341

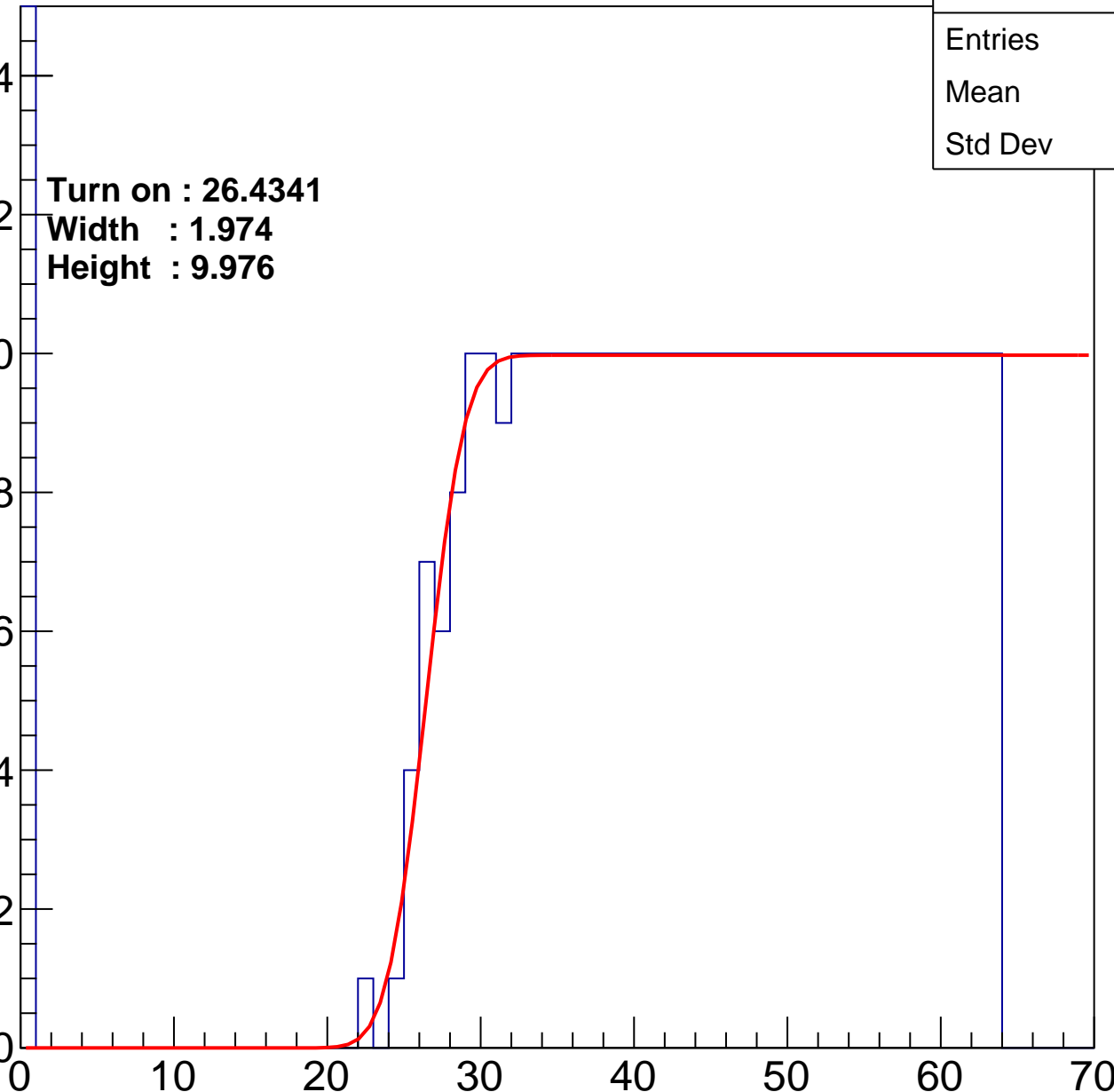
Width : 1.974

Height : 9.976

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch6

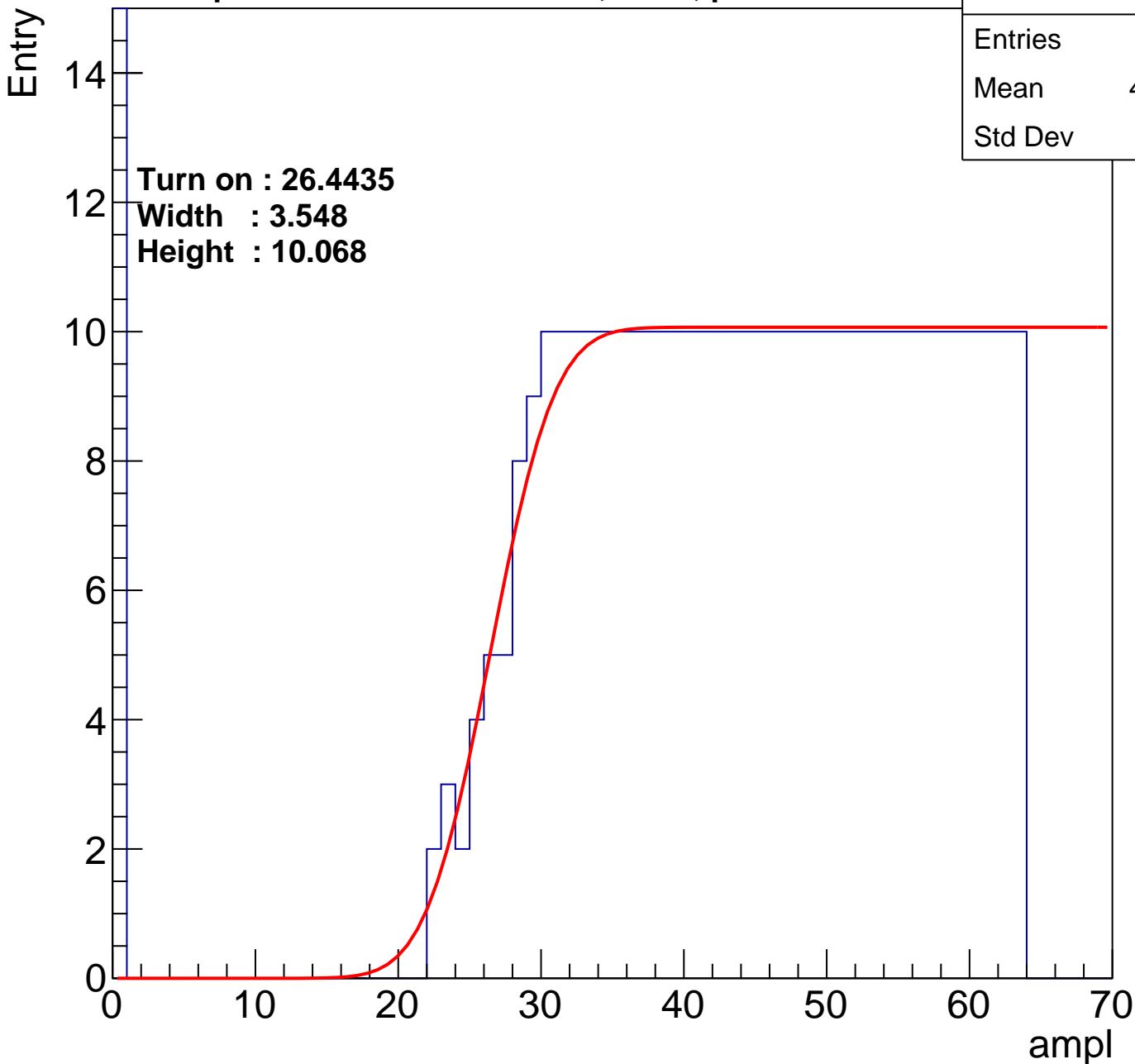
calib_packv5_041523_1651.root, FC#0, port C2

Entries	415
Mean	40.53
Std Dev	16.51

Turn on : 26.4435

Width : 3.548

Height : 10.068



B1L103S, U8-ch7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	40.46
Std Dev	16.42

Turn on : 25.6546

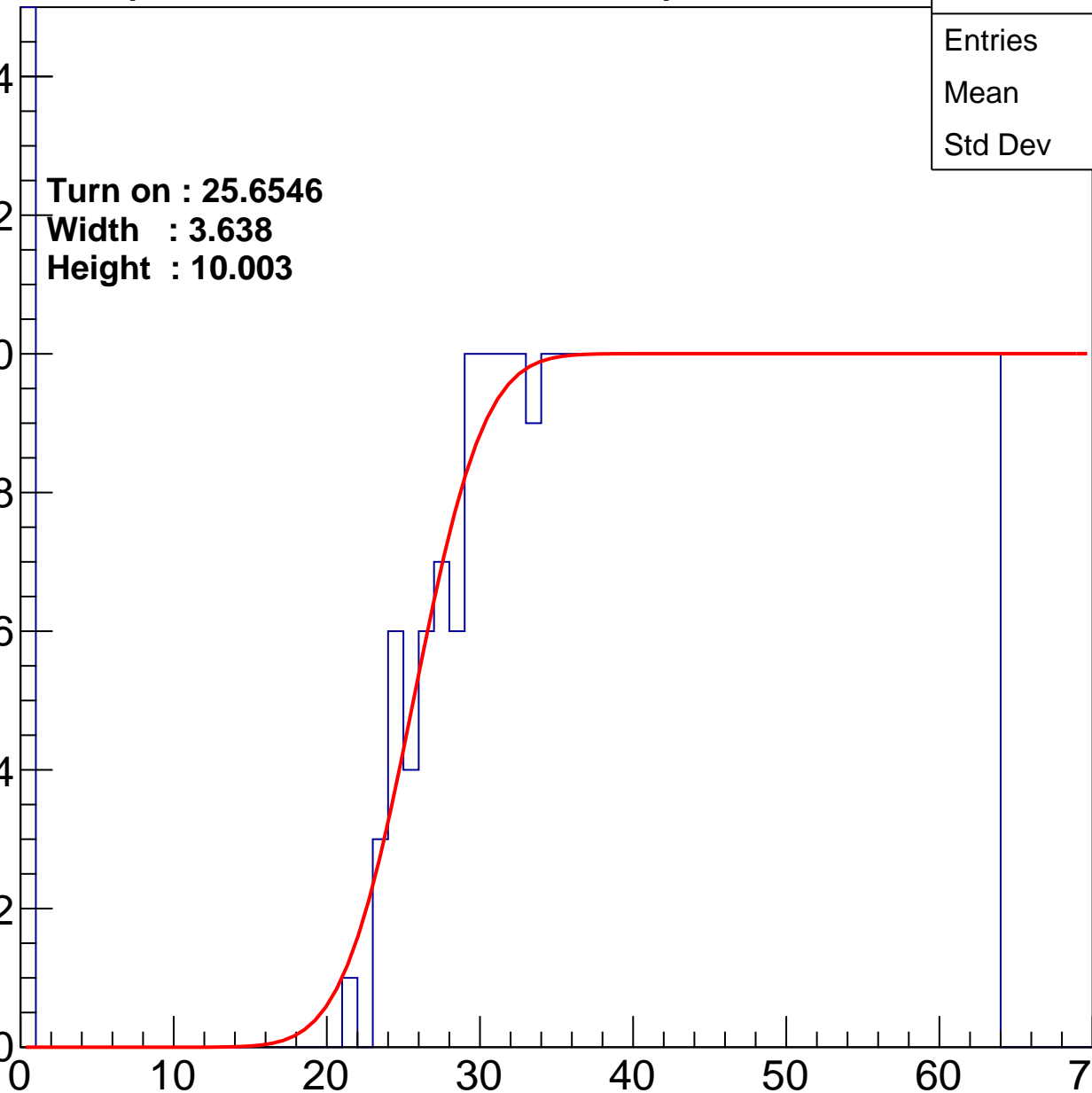
Width : 3.638

Height : 10.003

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch8

calib_packv5_041523_1651.root, FC#0, port C2

Entries	444
Mean	38.86
Std Dev	17.43

Turn on : 24.6369

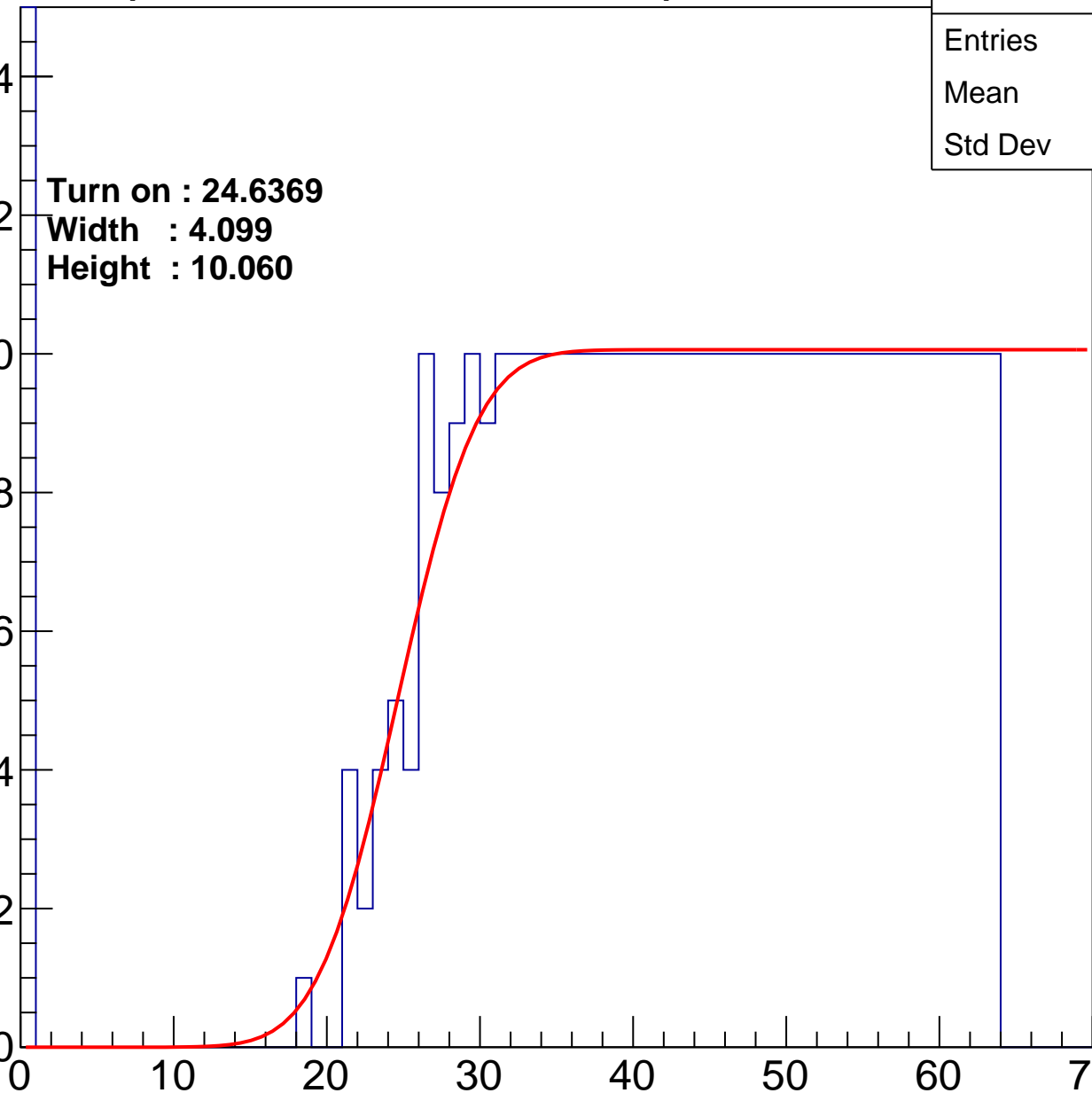
Width : 4.099

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch9

calib_packv5_041523_1651.root, FC#0, port C2

Entries	405
Mean	40.36
Std Dev	17.4

Turn on : 28.2014

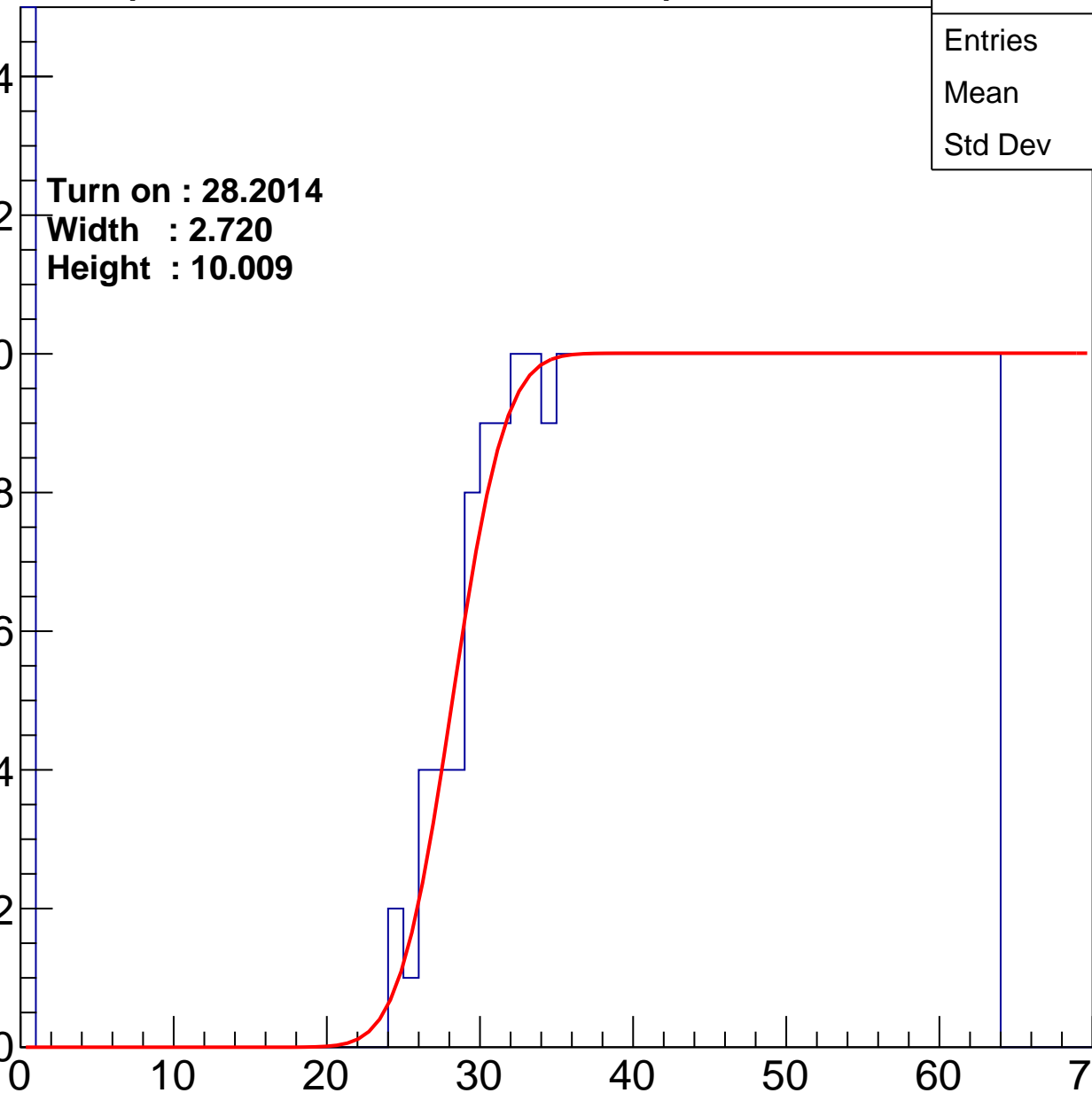
Width : 2.720

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch10

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	40.23
Std Dev	16.93

Turn on : 26.7328

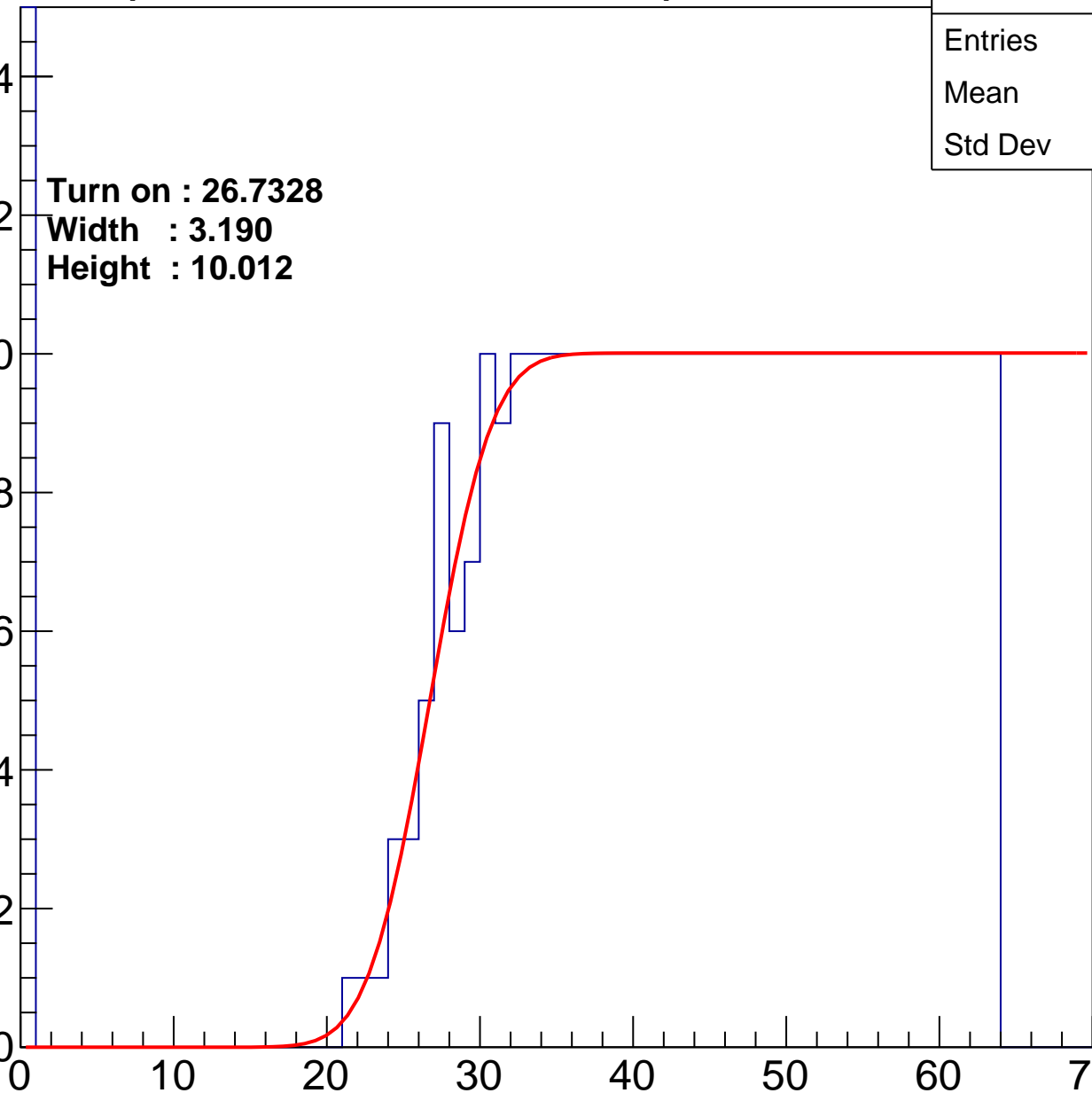
Width : 3.190

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch11

calib_packv5_041523_1651.root, FC#0, port C2

Entries	392
Mean	41.49
Std Dev	16.38

Turn on : 28.1549

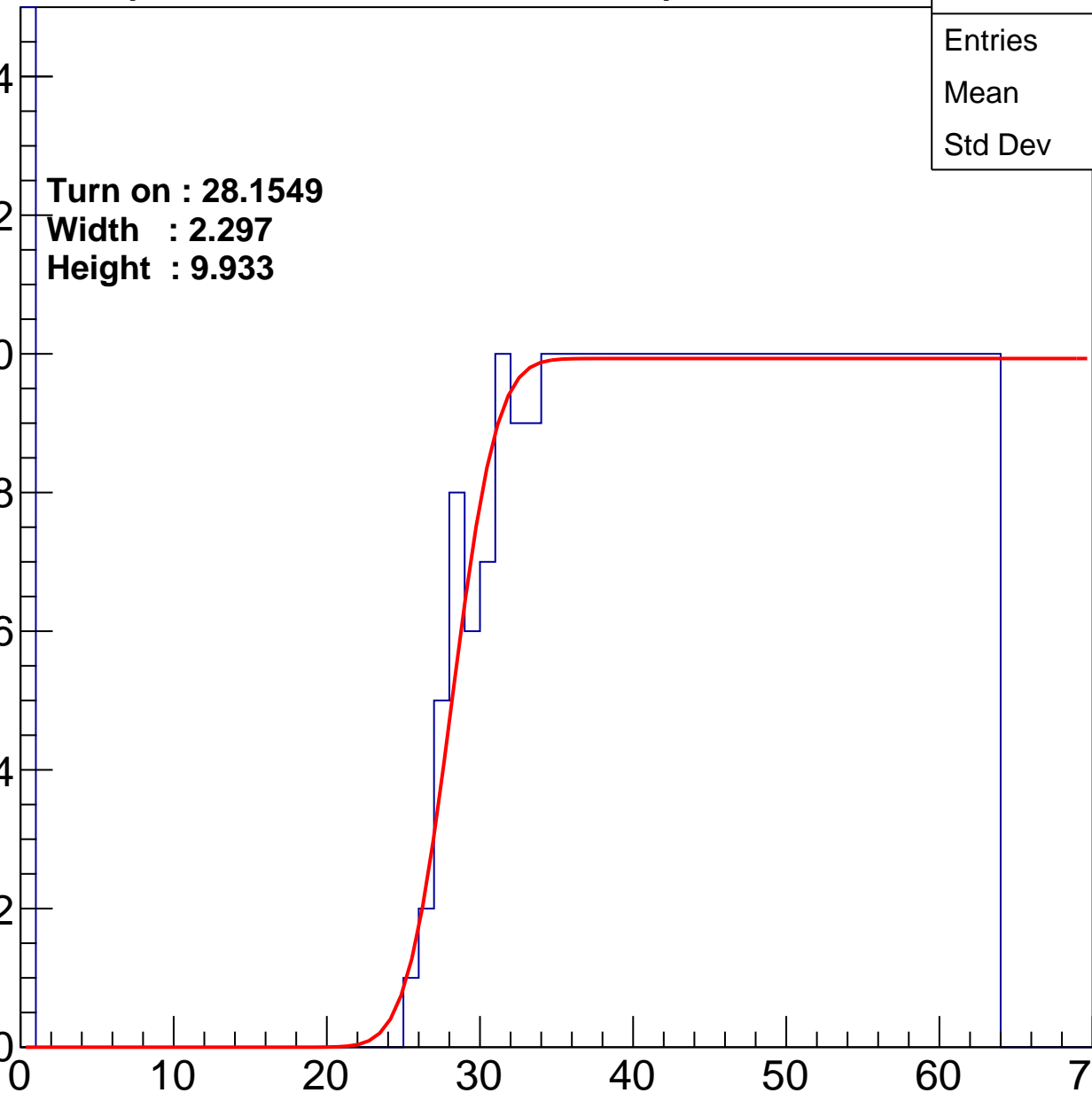
Width : 2.297

Height : 9.933

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch12

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	39.54
Std Dev	17.44

Turn on : 26.8700

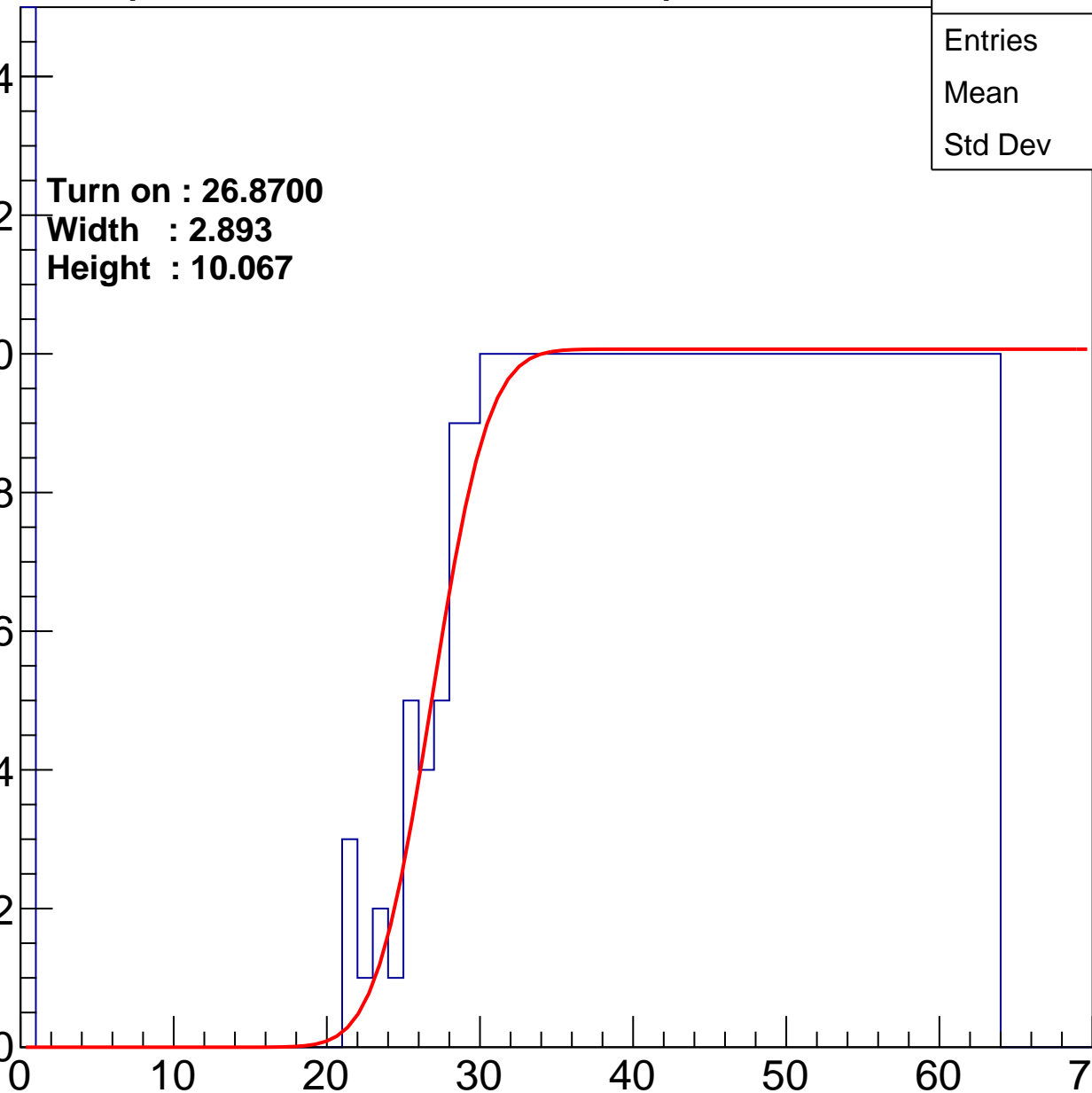
Width : 2.893

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch13

calib_packv5_041523_1651.root, FC#0, port C2

Entries	399
Mean	41.12
Std Dev	16.56

Turn on : 27.8180

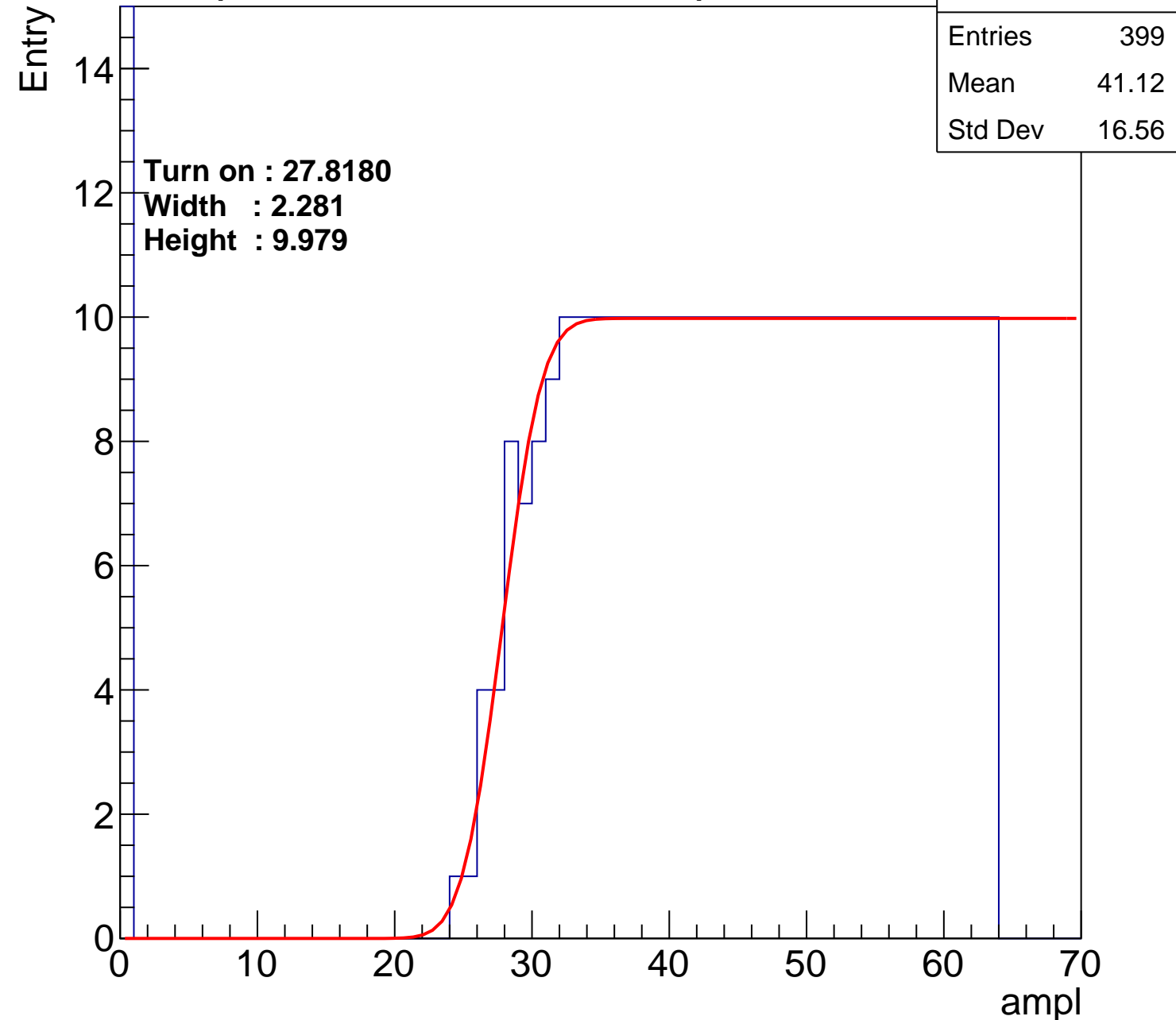
Width : 2.281

Height : 9.979

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch14

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	39.66
Std Dev	17.43

Turn on : 26.5620

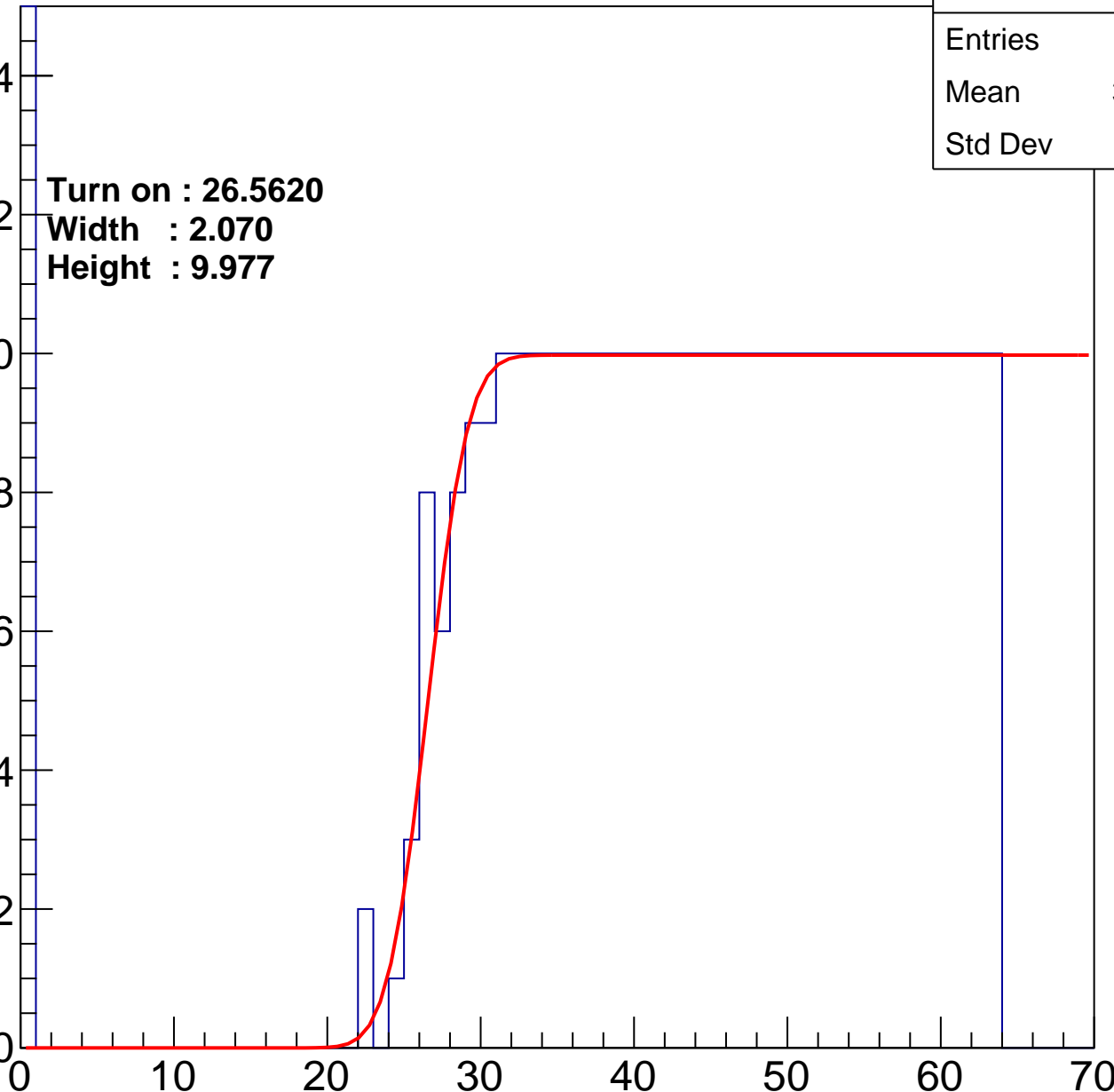
Width : 2.070

Height : 9.977

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch15

calib_packv5_041523_1651.root, FC#0, port C2

Entries	413
Mean	40.24
Std Dev	17.08

Turn on : 26.9518

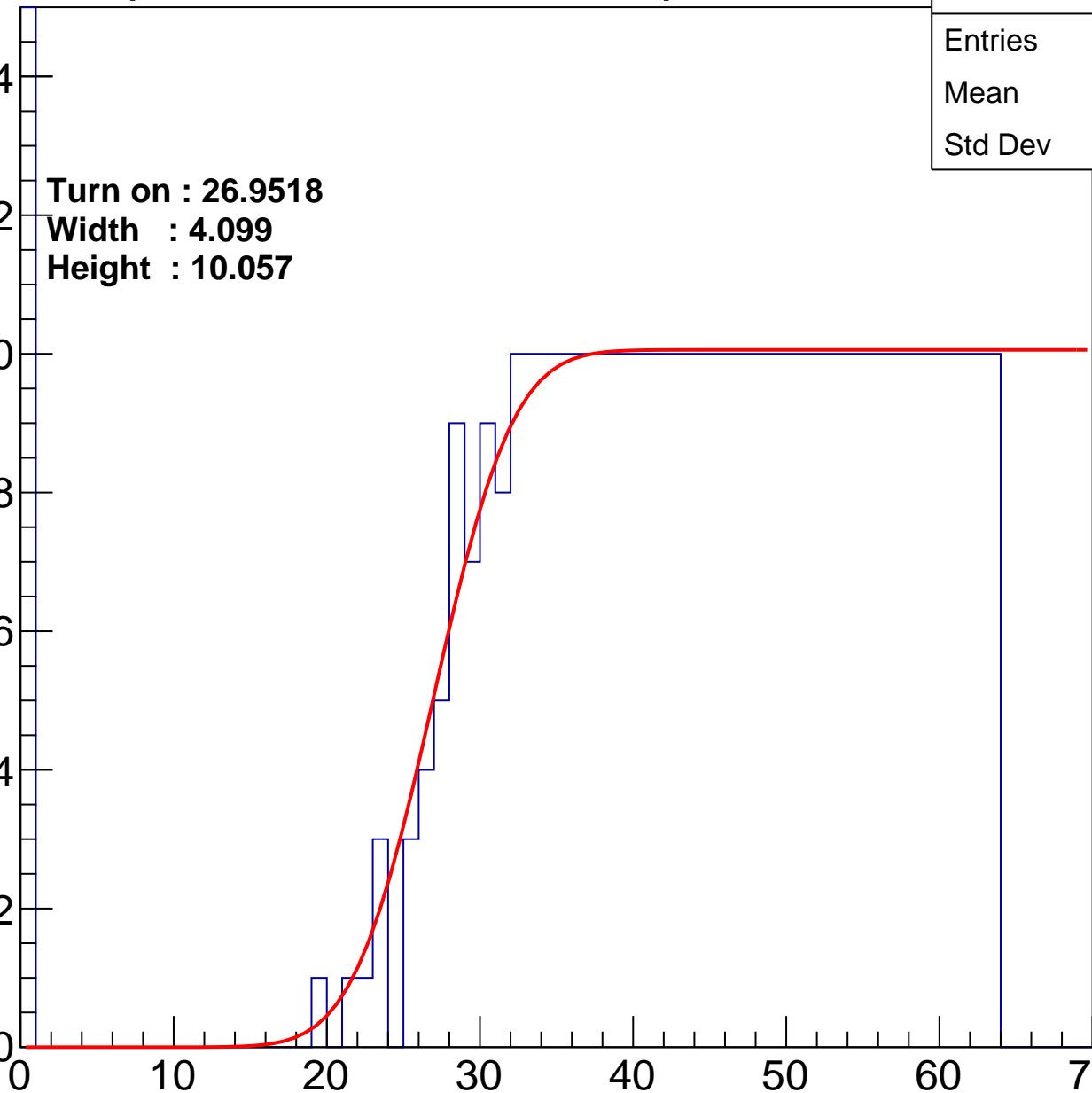
Width : 4.099

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch16

calib_packv5_041523_1651.root, FC#0, port C2

Entries	406
Mean	41.22
Std Dev	15.96

Turn on : 27.1271

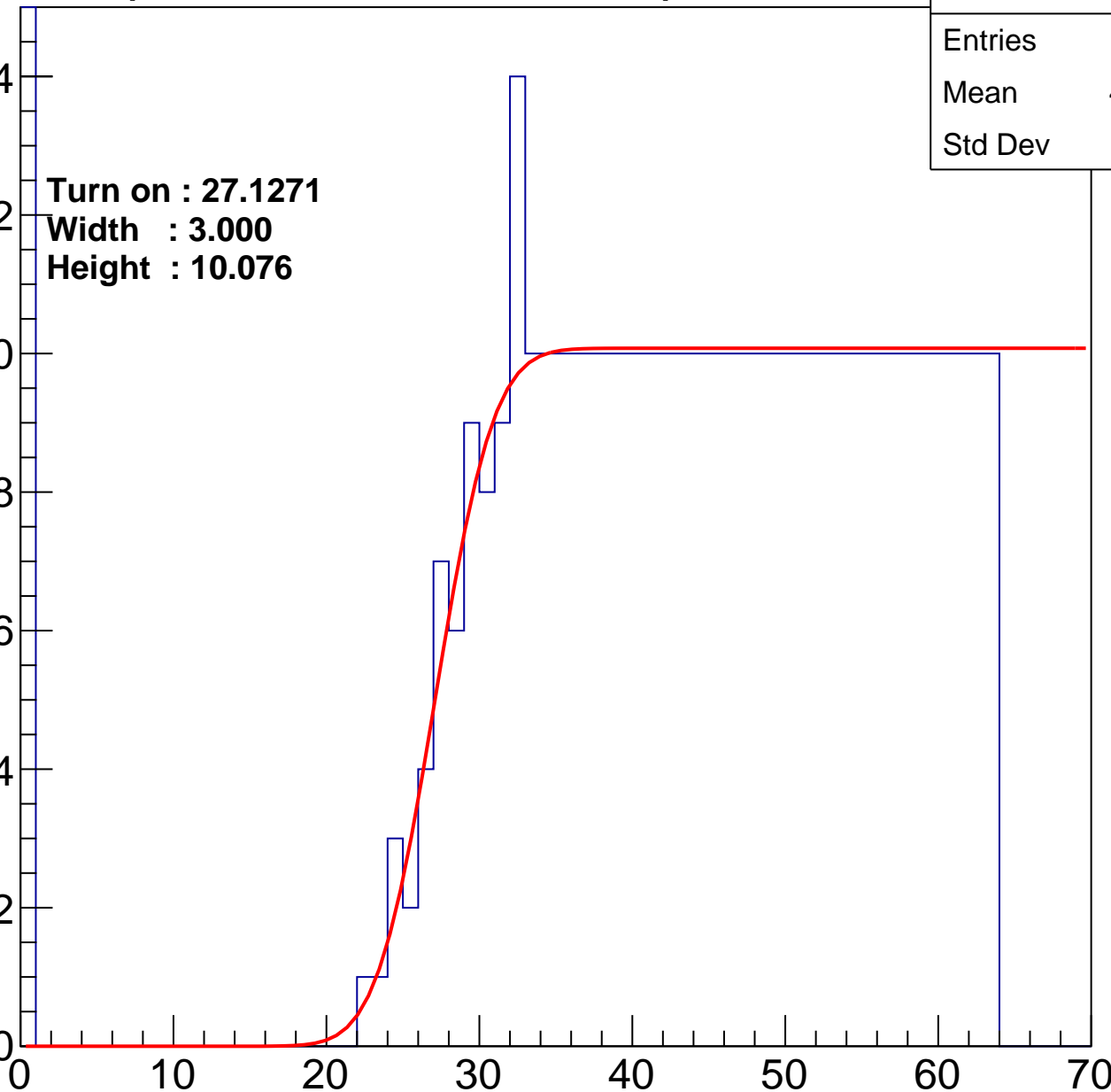
Width : 3.000

Height : 10.076

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch17

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	39.44
Std Dev	17.93

Turn on : 26.9639

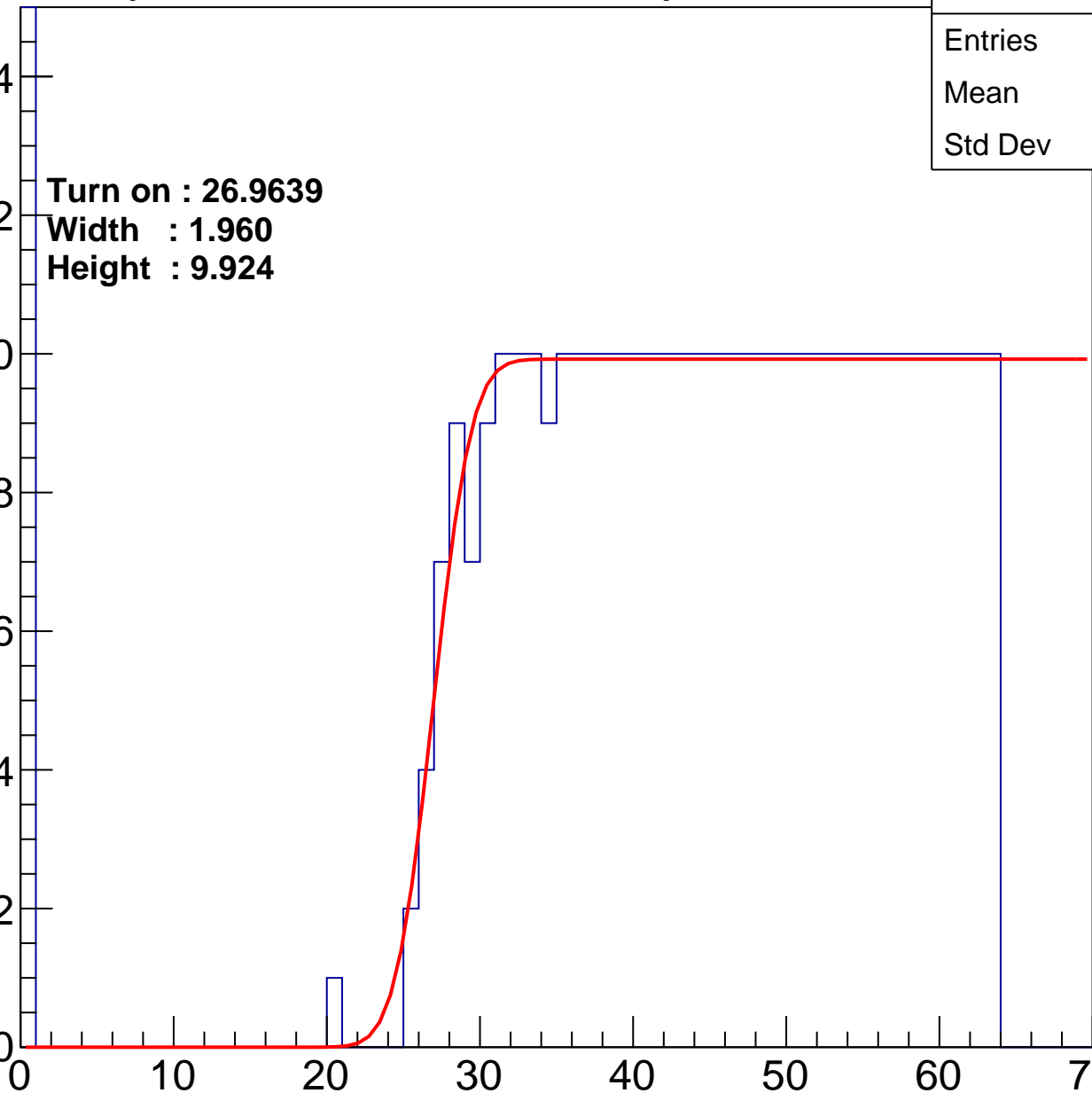
Width : 1.960

Height : 9.924

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch18

calib_packv5_041523_1651.root, FC#0, port C2

Entries	421
Mean	39.84
Std Dev	17.27

Turn on : 26.8275

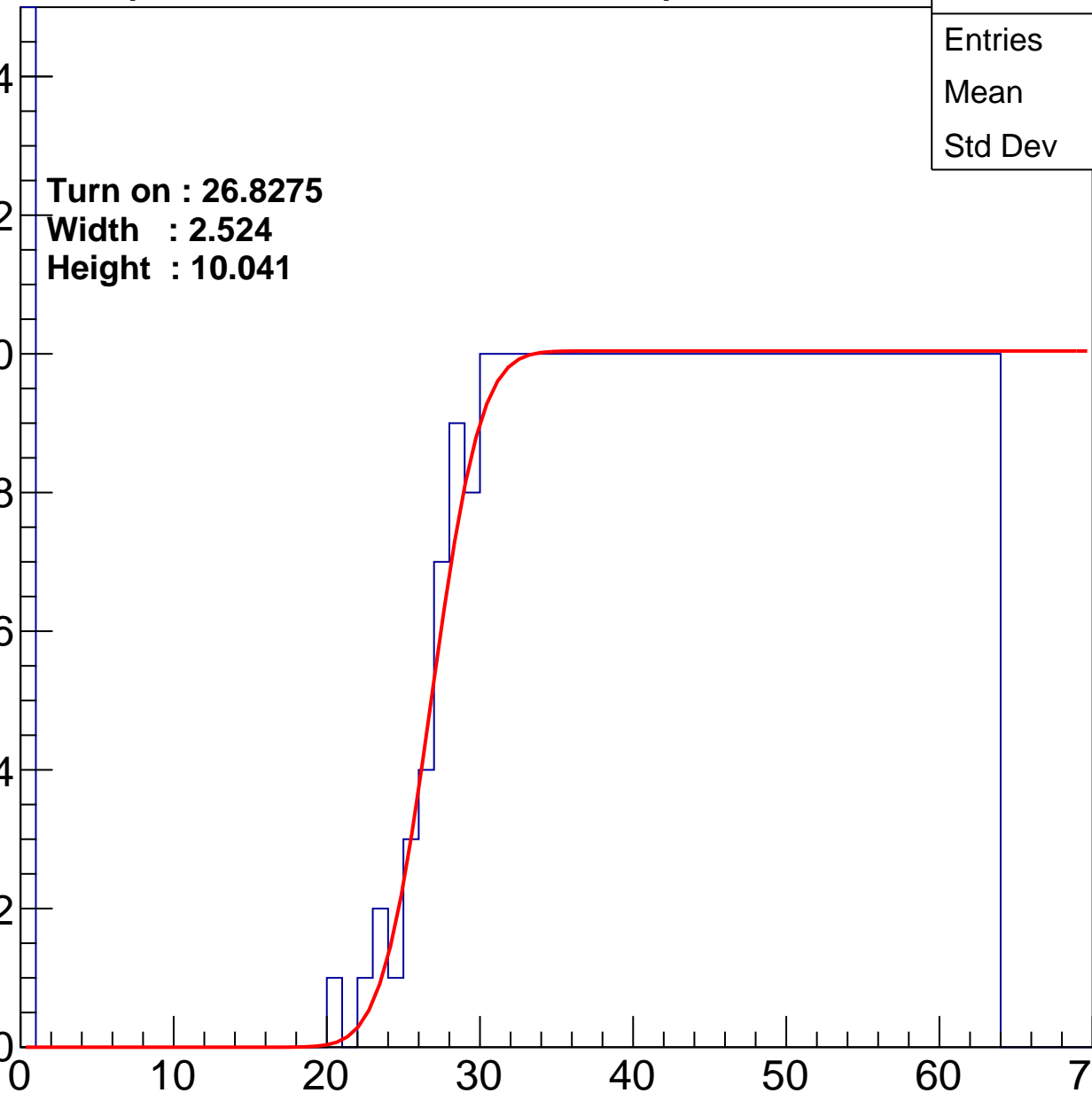
Width : 2.524

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch19

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	40.17
Std Dev	16.57

Turn on : 25.4493

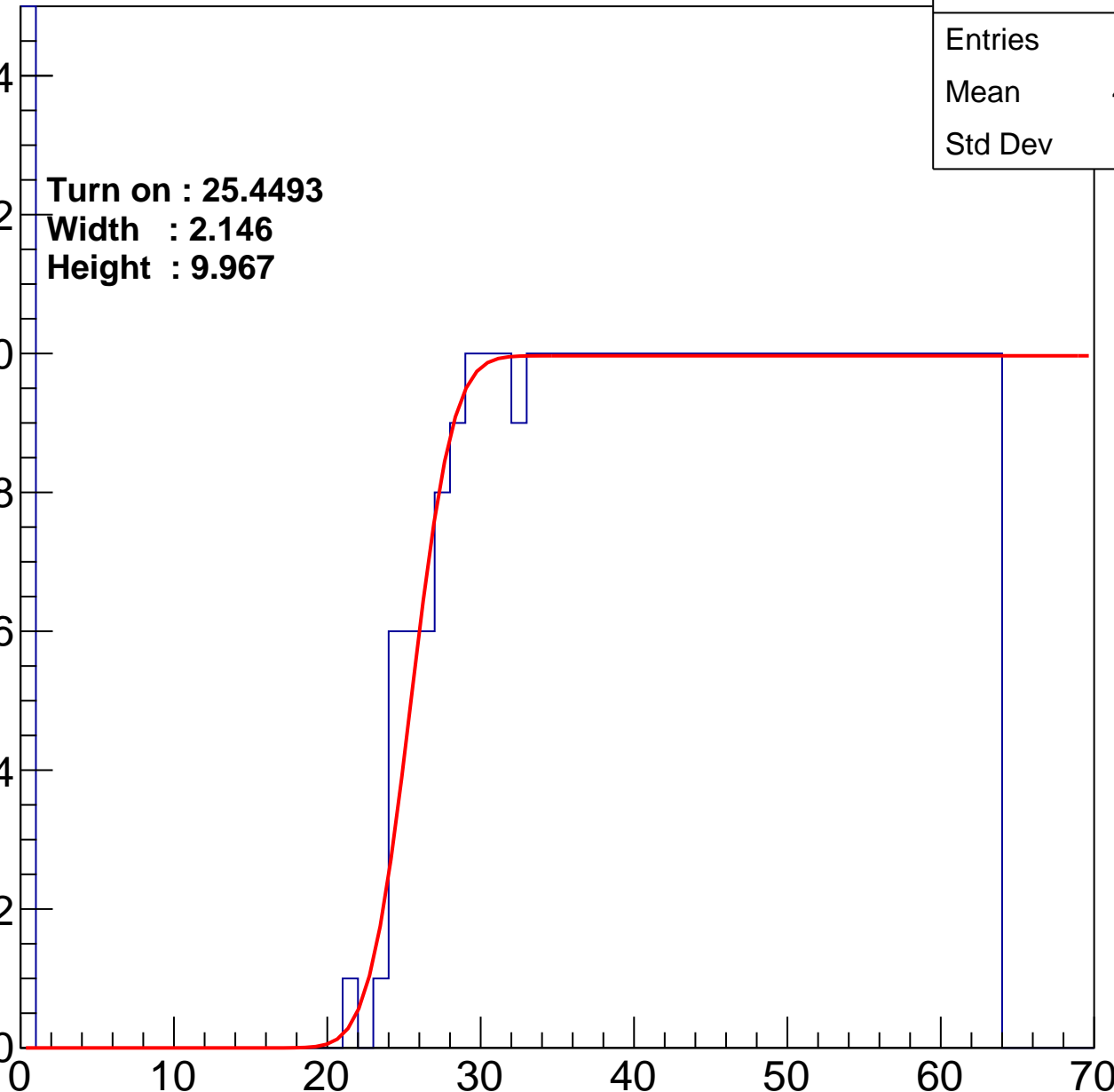
Width : 2.146

Height : 9.967

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch20

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	40.2
Std Dev	16.54

Turn on : 25.5923

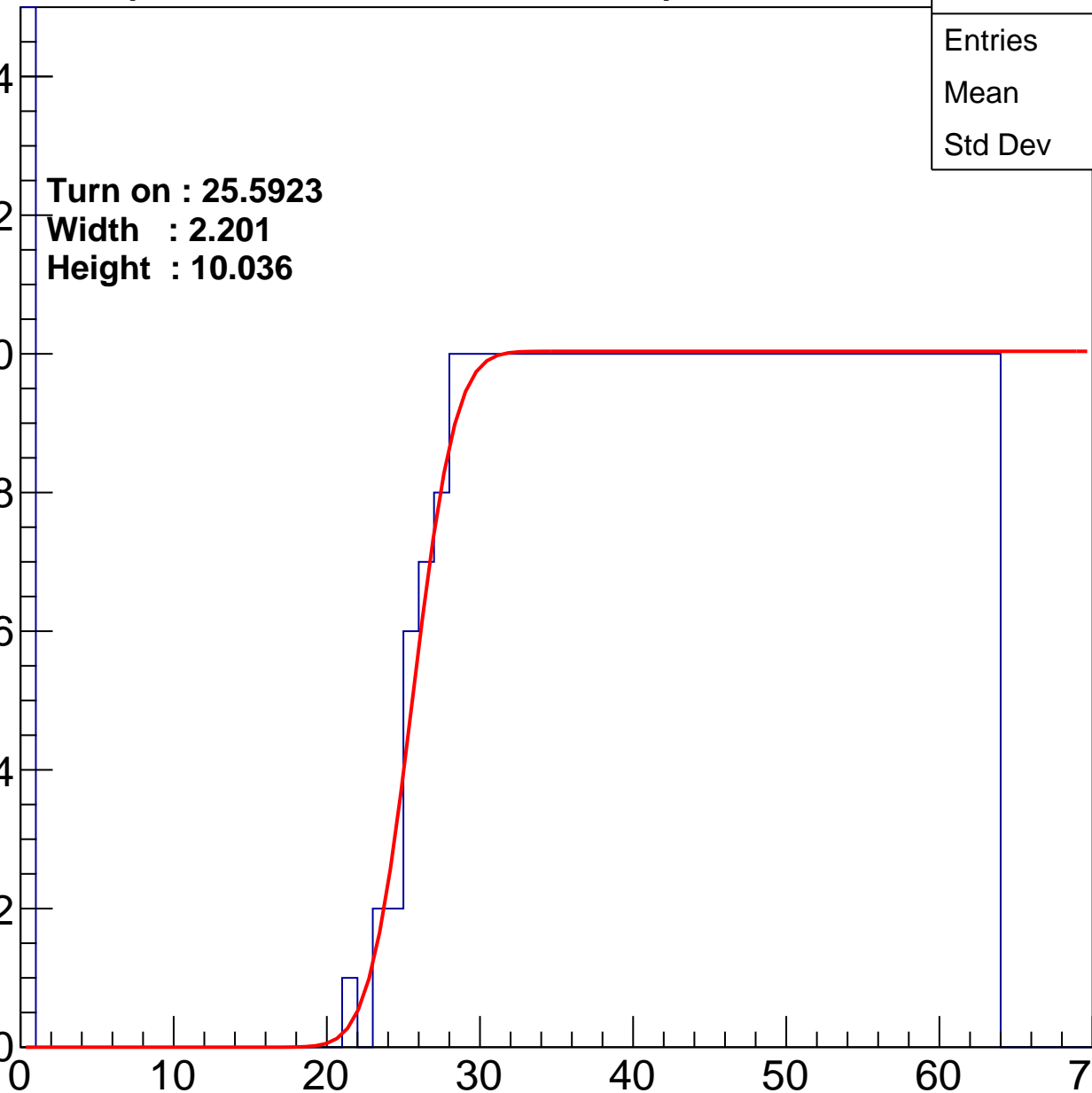
Width : 2.201

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch21

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	39.28
Std Dev	17.64

Turn on : 25.9205

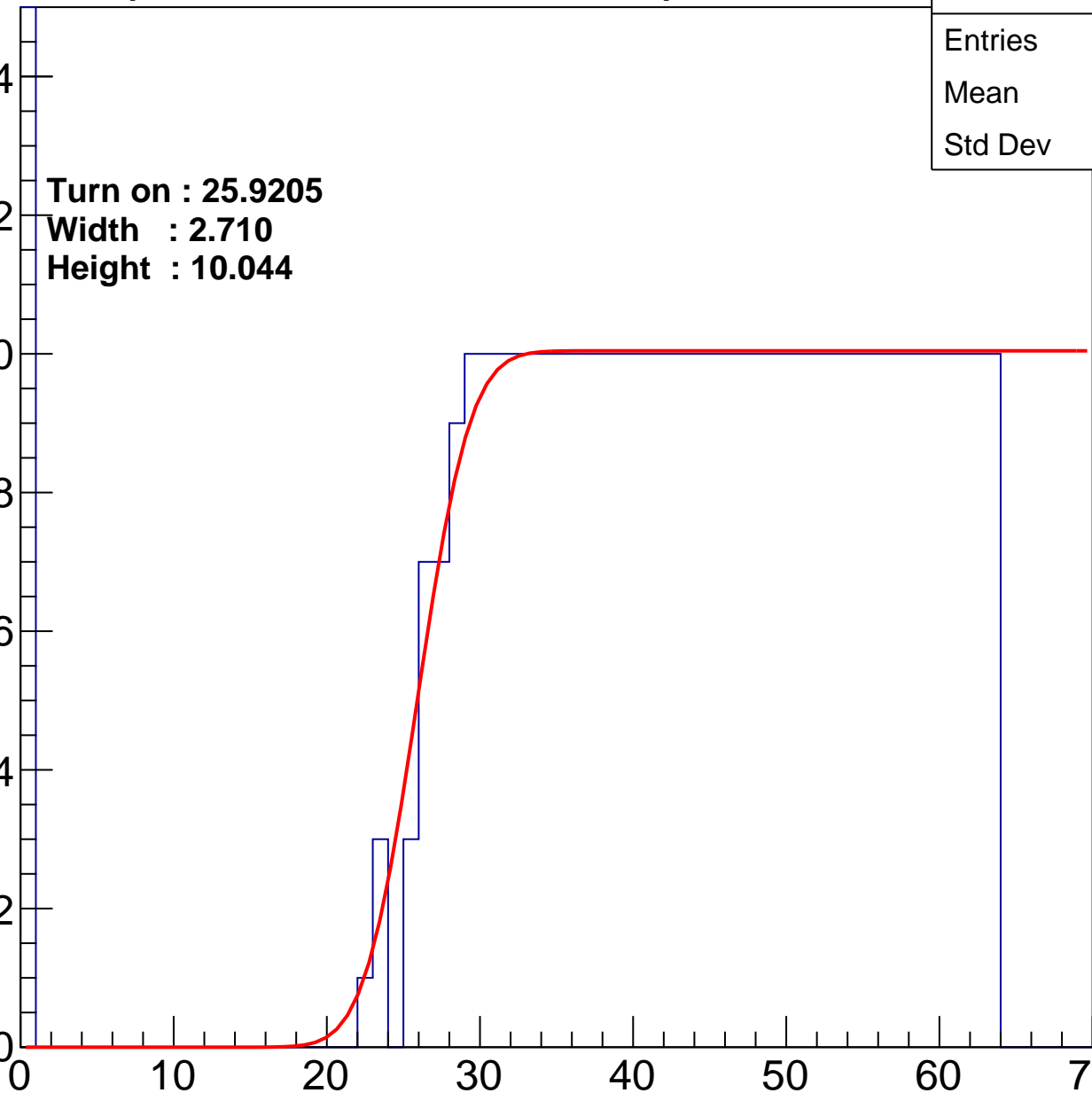
Width : 2.710

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch22

calib_packv5_041523_1651.root, FC#0, port C2

Entries	410
Mean	40.68
Std Dev	16.56

Turn on : 26.7735

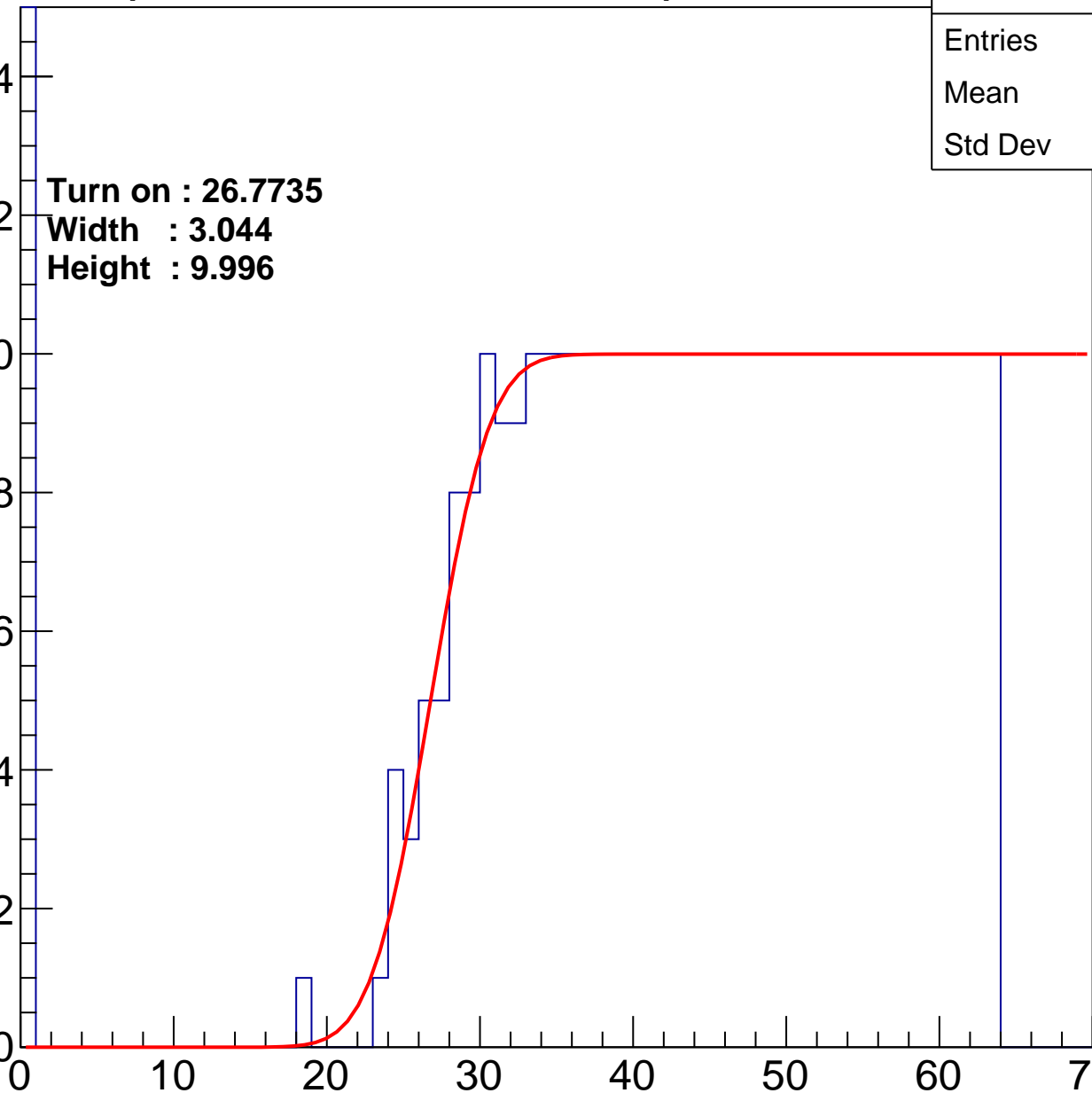
Width : 3.044

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch23

calib_packv5_041523_1651.root, FC#0, port C2

Entries	410
Mean	40.22
Std Dev	17.33

Turn on : 27.2168

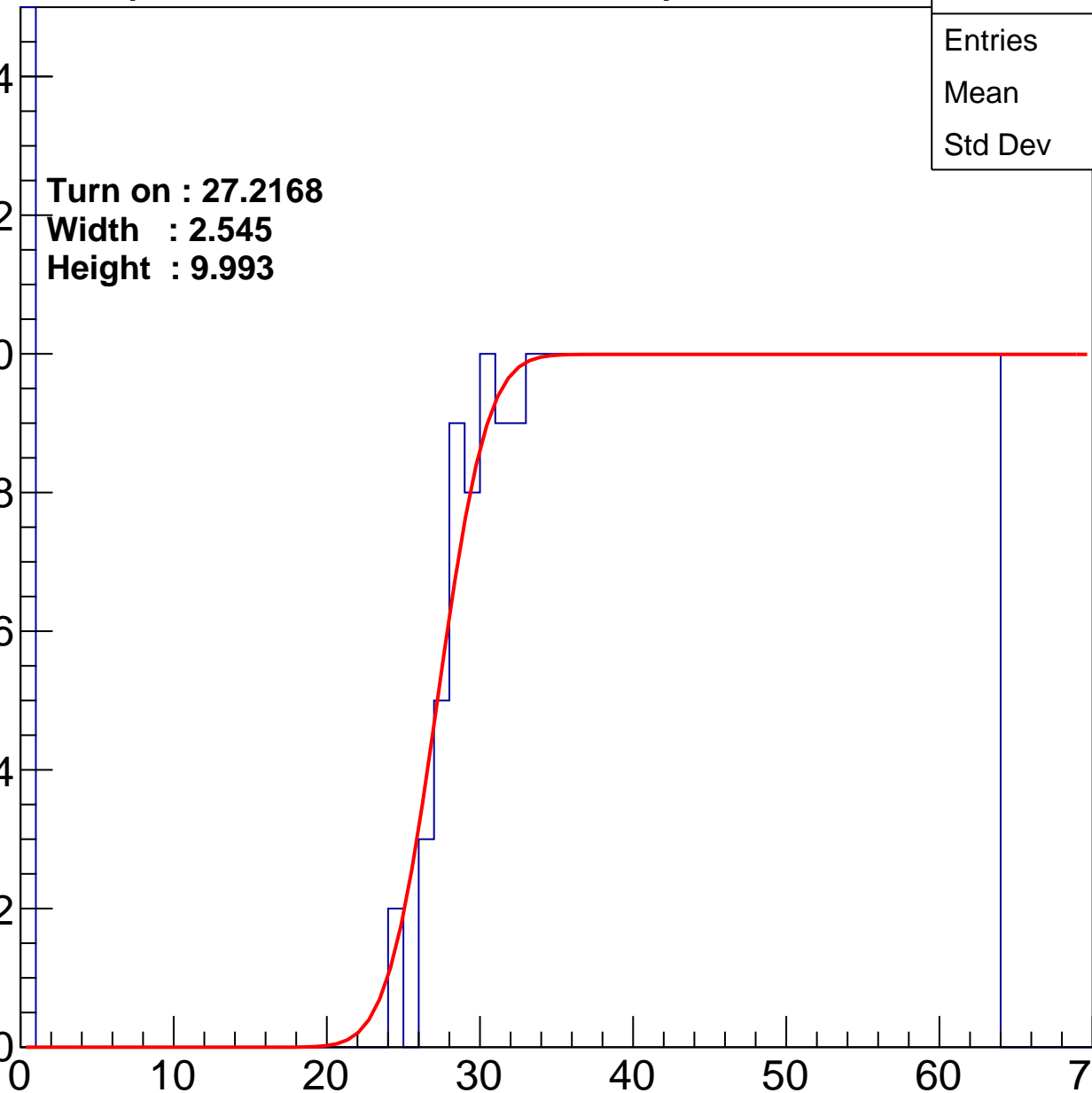
Width : 2.545

Height : 9.993

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch24

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	39.5
Std Dev	16.56

Turn on : 23.8572

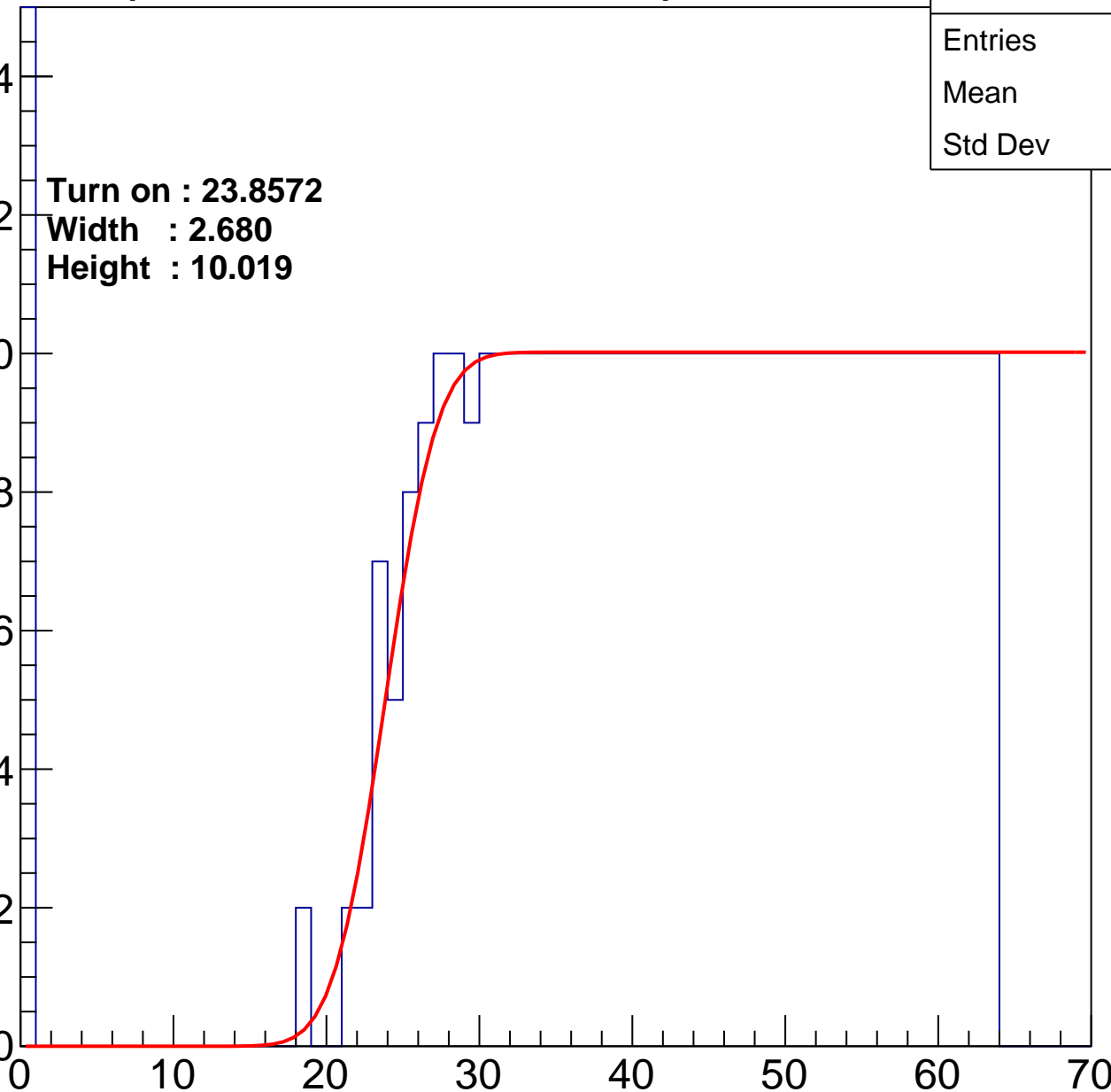
Width : 2.680

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch25

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	40.02
Std Dev	17.09

Turn on : 26.4882

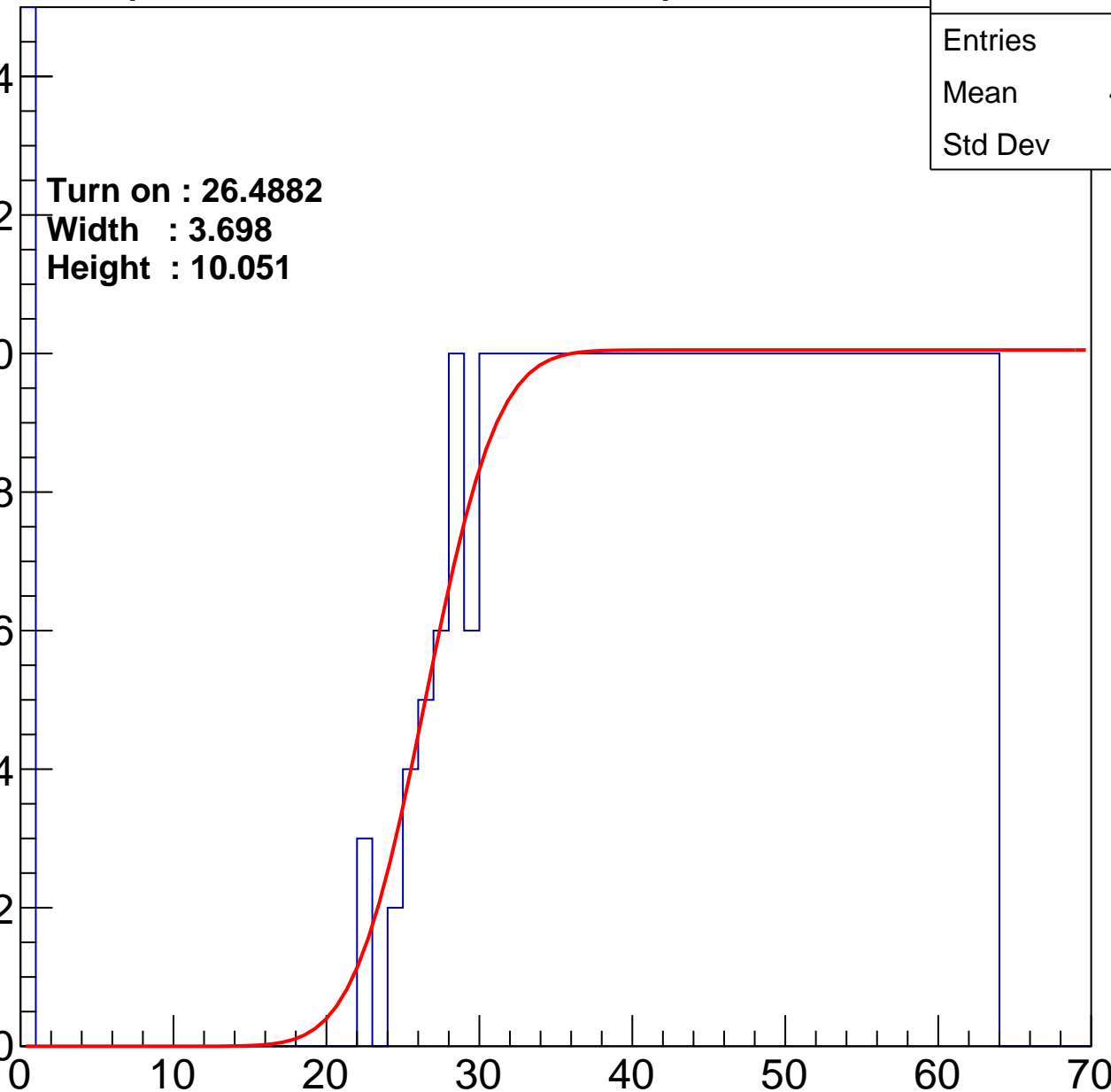
Width : 3.698

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch26

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	39.46
Std Dev	17.24

Turn on : 25.6249

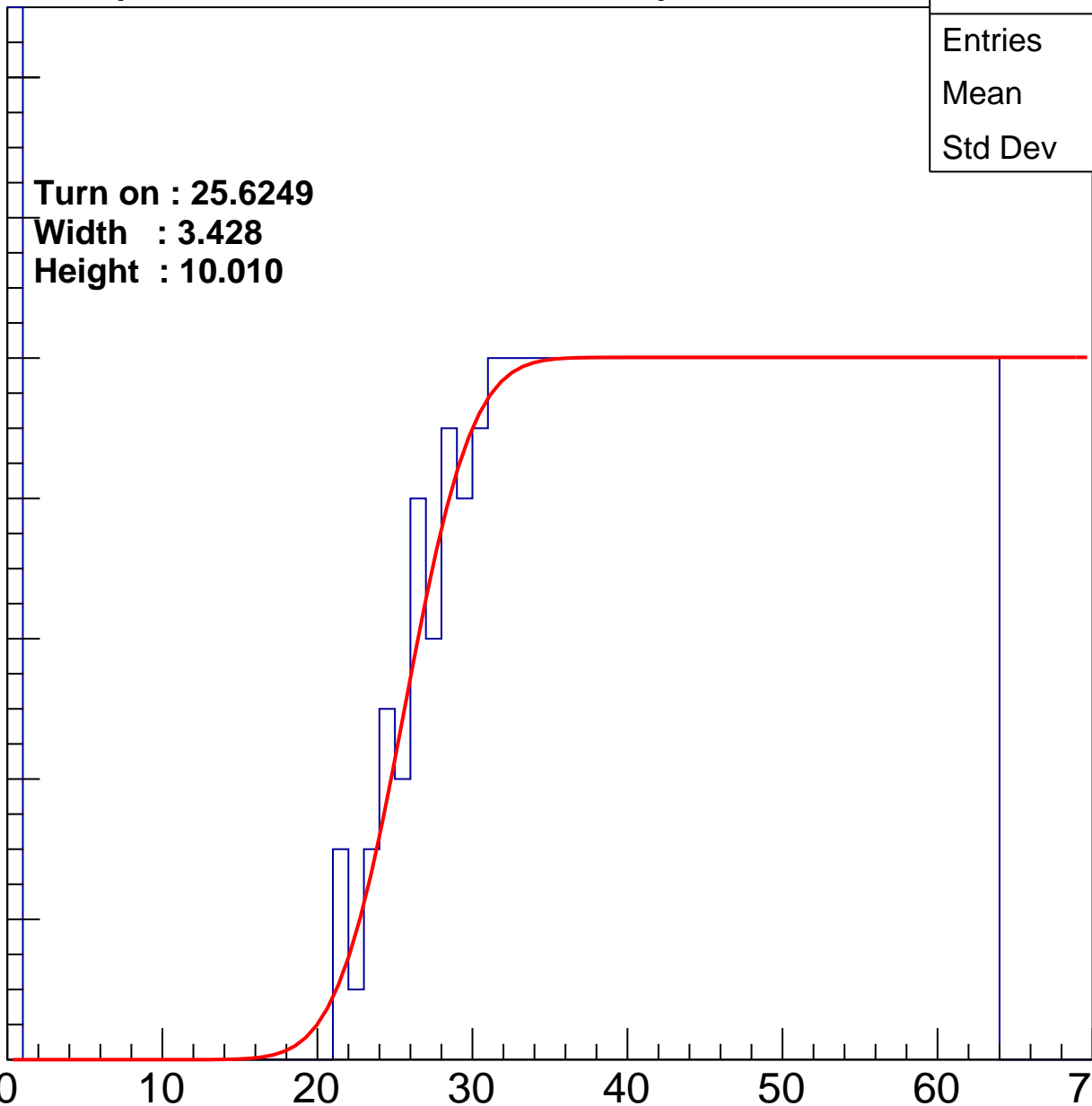
Width : 3.428

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch27

calib_packv5_041523_1651.root, FC#0, port C2

Entries	415
Mean	40.27
Std Dev	16.93

Turn on : 26.7789

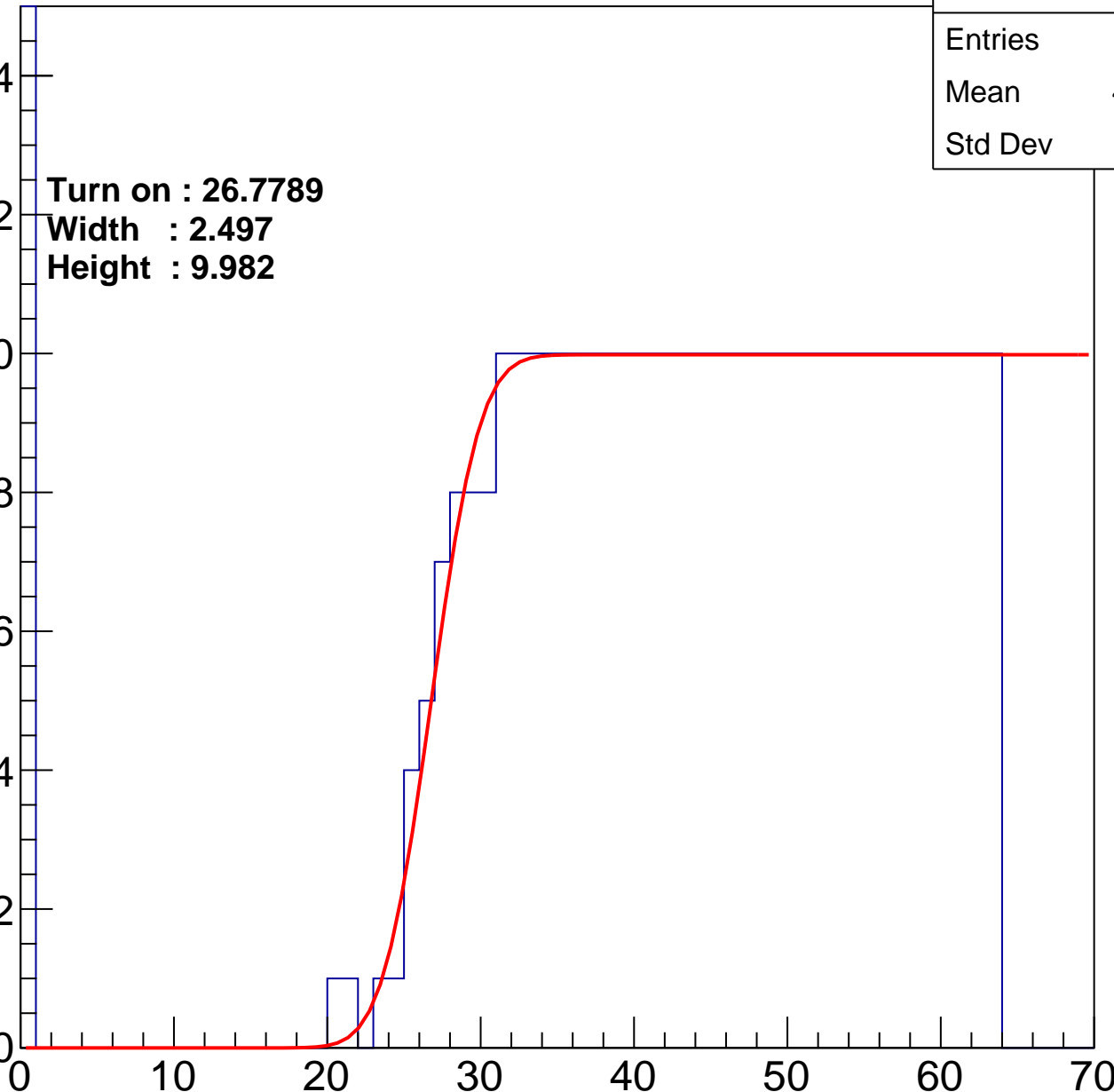
Width : 2.497

Height : 9.982

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch28

calib_packv5_041523_1651.root, FC#0, port C2

Entries	417
Mean	40.59
Std Dev	16.29

Turn on : 26.3648

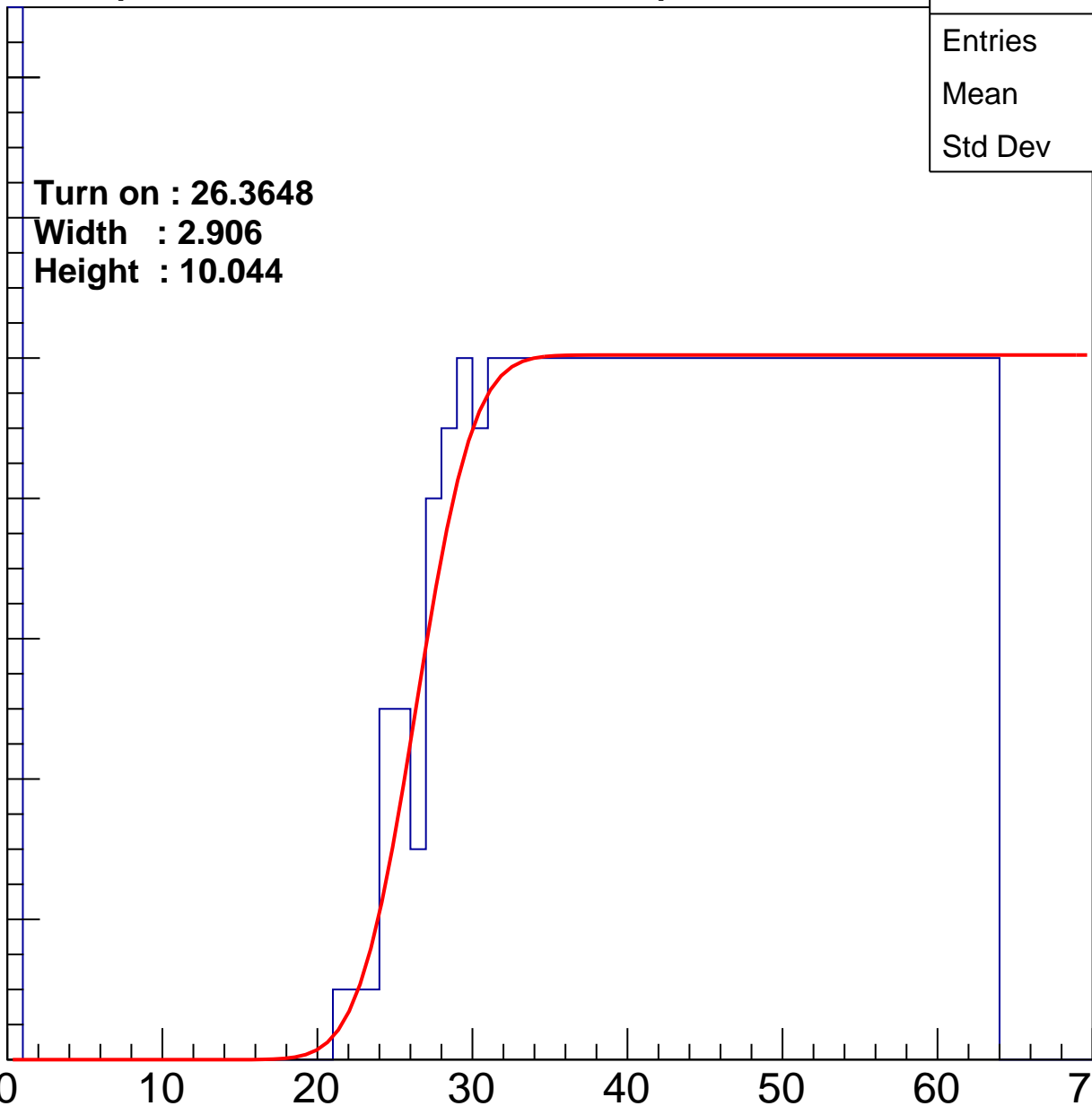
Width : 2.906

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch29

calib_packv5_041523_1651.root, FC#0, port C2

Entries	399
Mean	41.05
Std Dev	16.68

Turn on : 27.6677

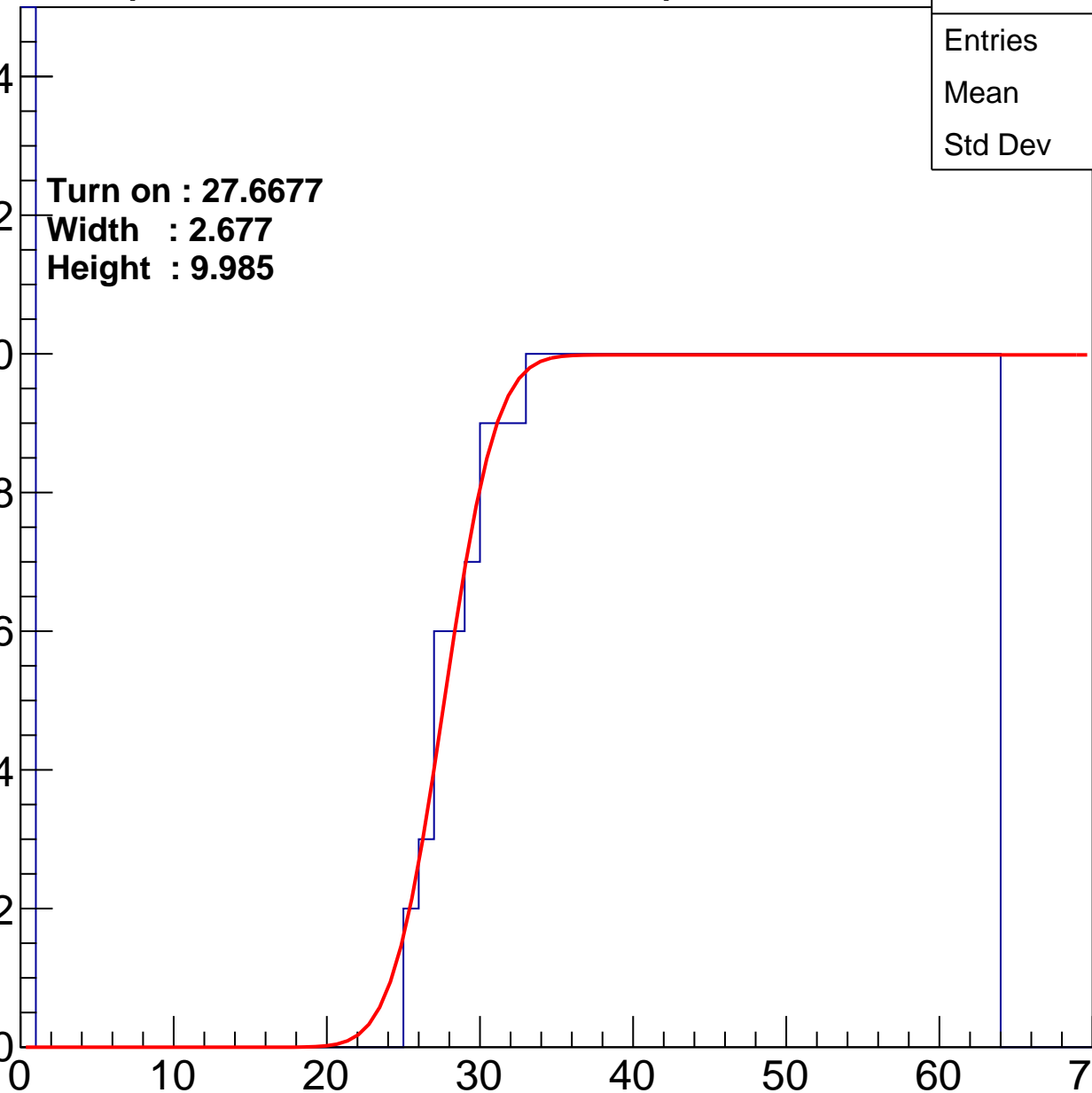
Width : 2.677

Height : 9.985

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch30

calib_packv5_041523_1651.root, FC#0, port C2

Entries	427
Mean	39.4
Std Dev	17.6

Turn on : 26.4013

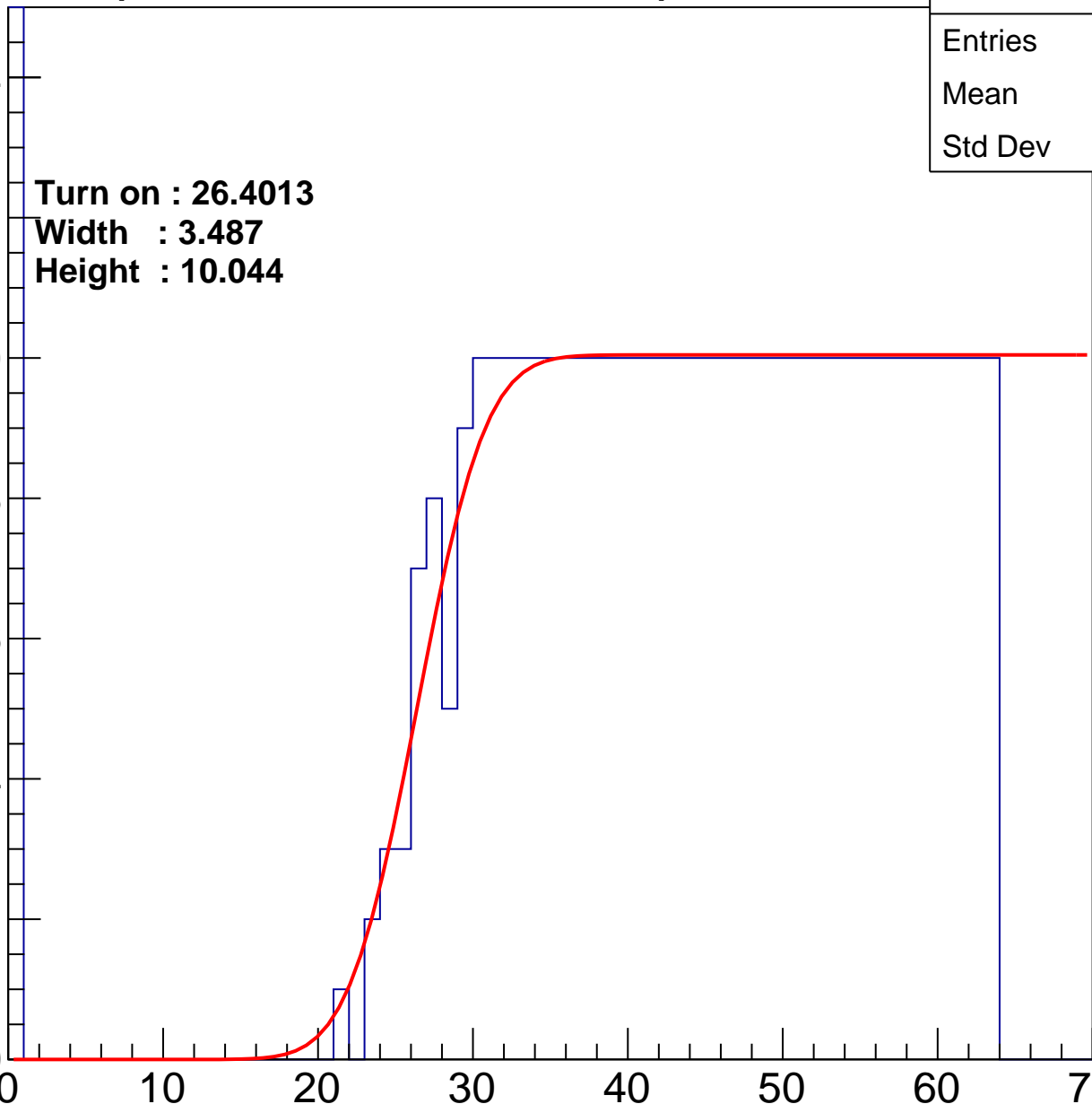
Width : 3.487

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch31

calib_packv5_041523_1651.root, FC#0, port C2

Entries	391
Mean	41.35
Std Dev	16.72

Turn on : 29.0525

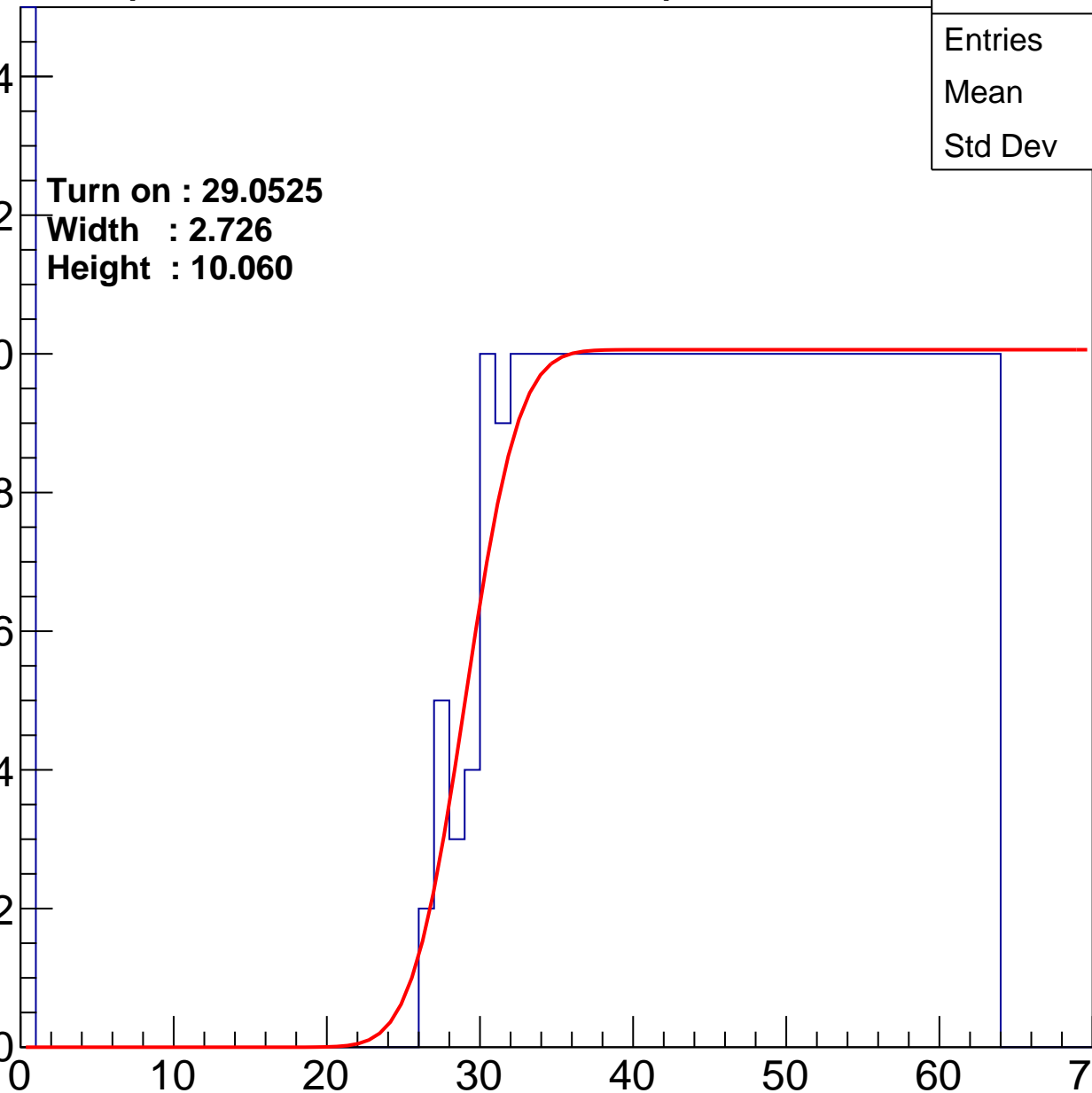
Width : 2.726

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch32

calib_packv5_041523_1651.root, FC#0, port C2

Entries	447
Mean	38.92
Std Dev	17.18

Turn on : 24.3980

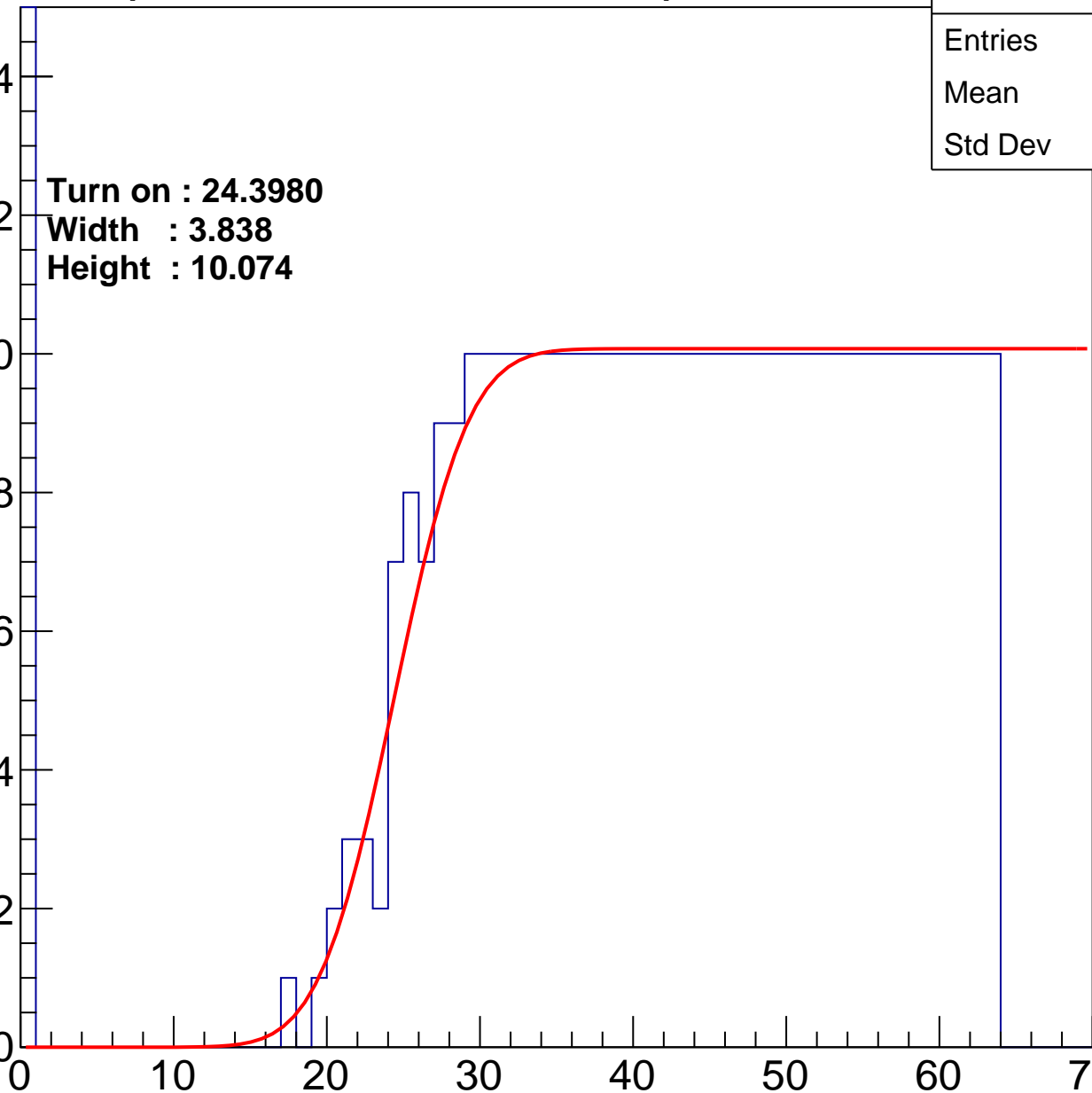
Width : 3.838

Height : 10.074

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch33

calib_packv5_041523_1651.root, FC#0, port C2

Entries	403
Mean	41.12
Std Dev	16.31

Turn on : 27.1480

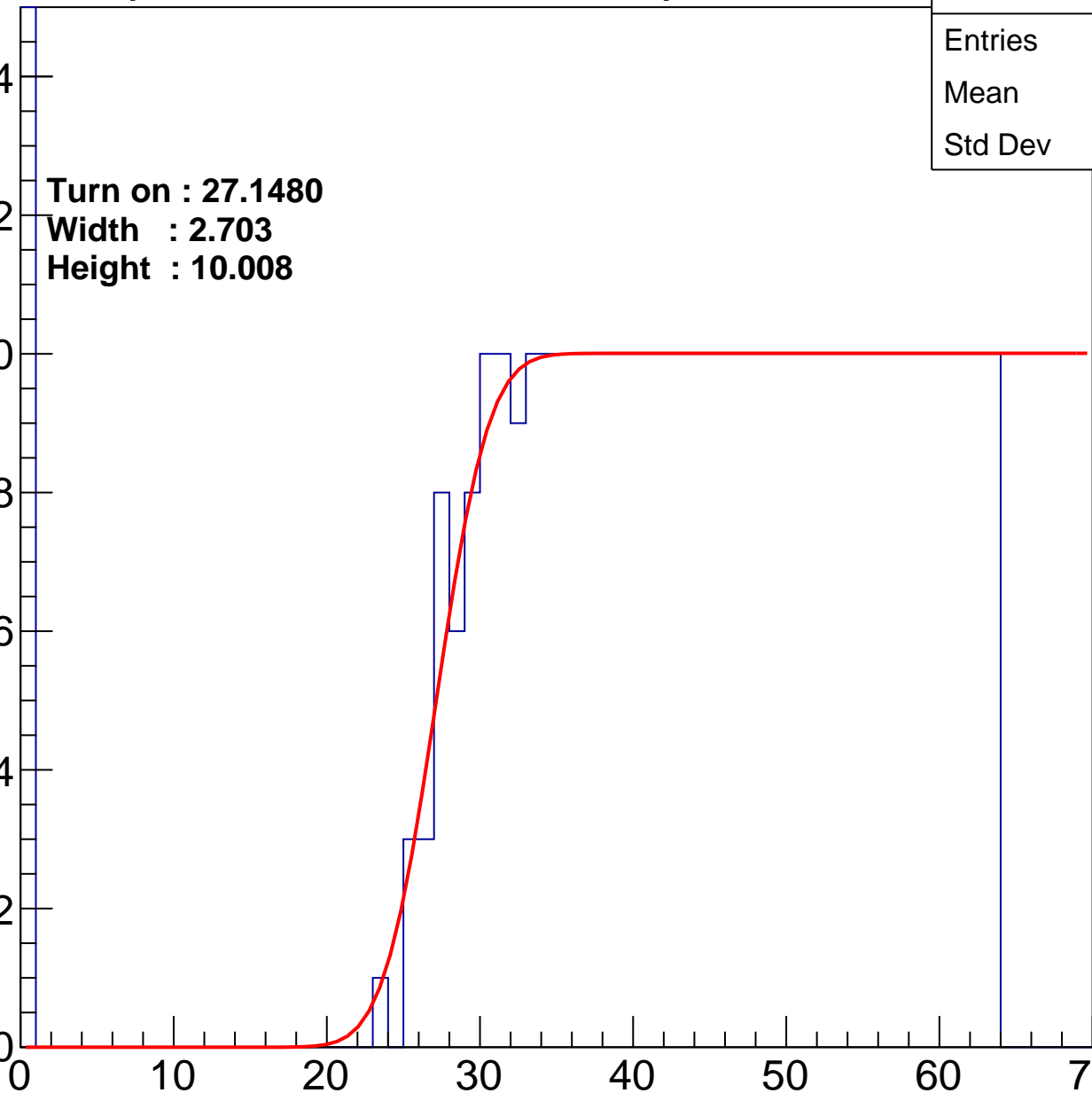
Width : 2.703

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch34

calib_packv5_041523_1651.root, FC#0, port C2

Entries	414
Mean	40.34
Std Dev	16.91

Turn on : 26.6131

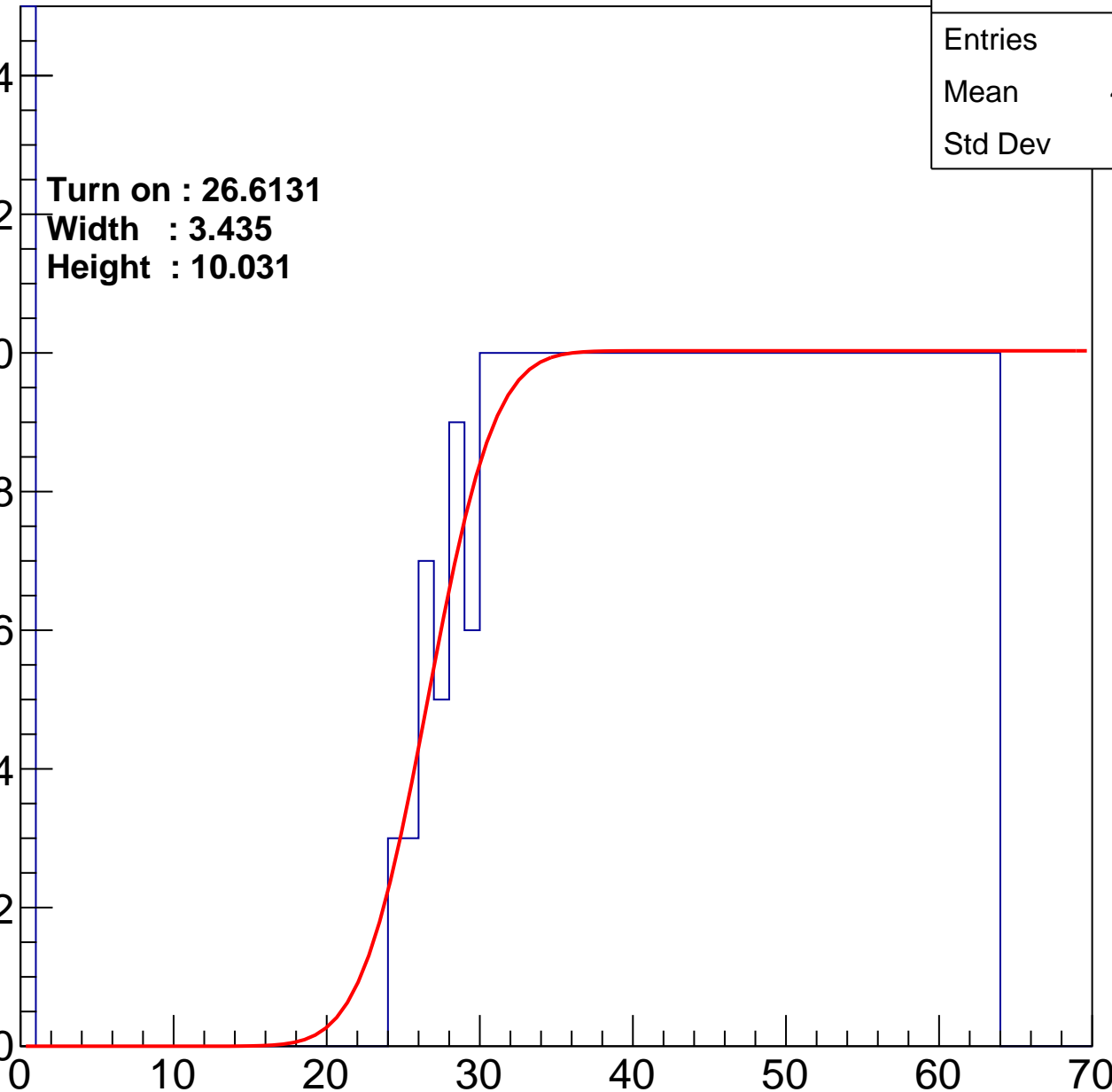
Width : 3.435

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch35

calib_packv5_041523_1651.root, FC#0, port C2

Entries	399
Mean	41.09
Std Dev	16.59

Turn on : 28.1668

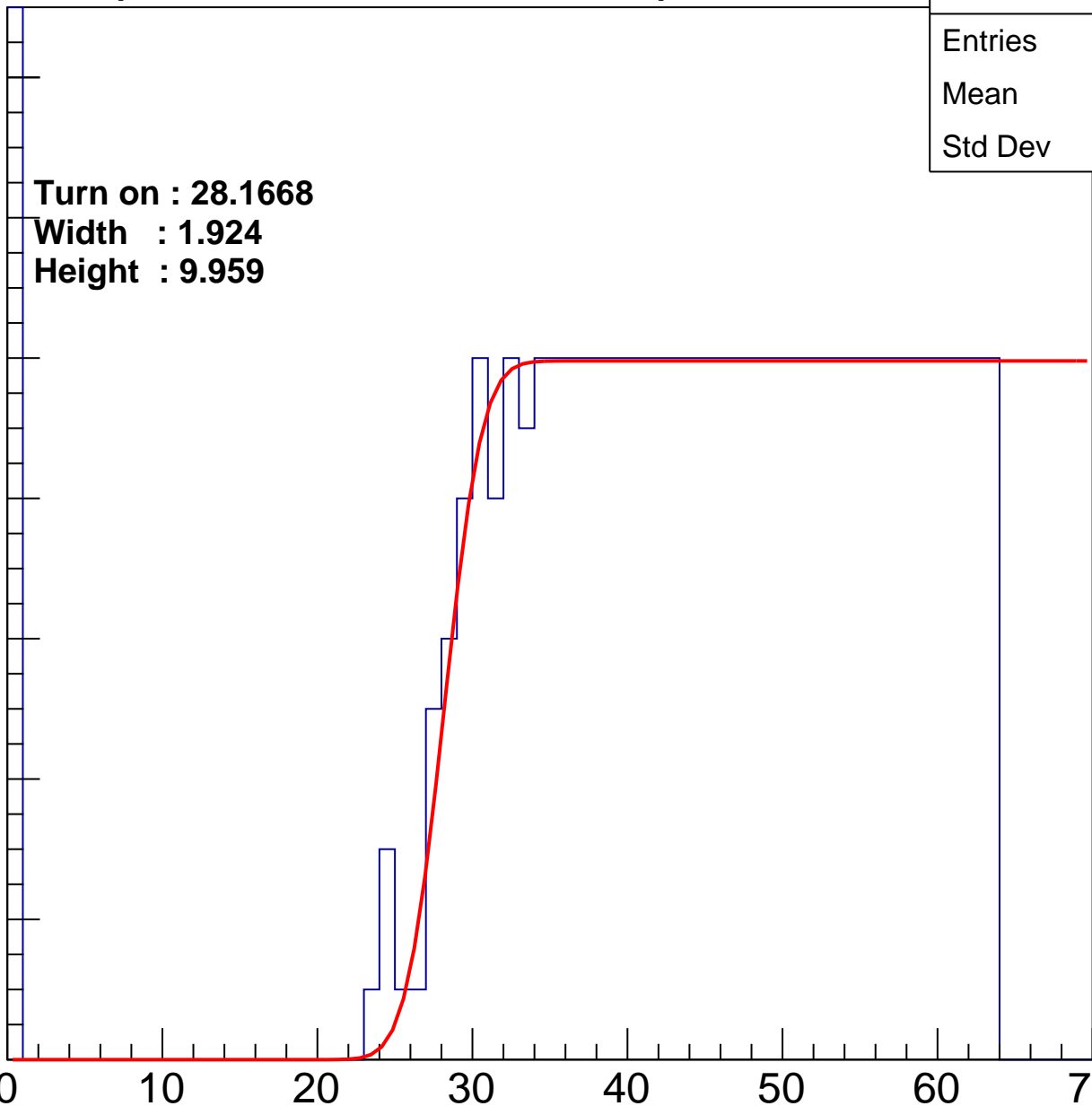
Width : 1.924

Height : 9.959

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch36

calib_packv5_041523_1651.root, FC#0, port C2

Entries	417
Mean	40.64
Std Dev	16.19

Turn on : 25.5103

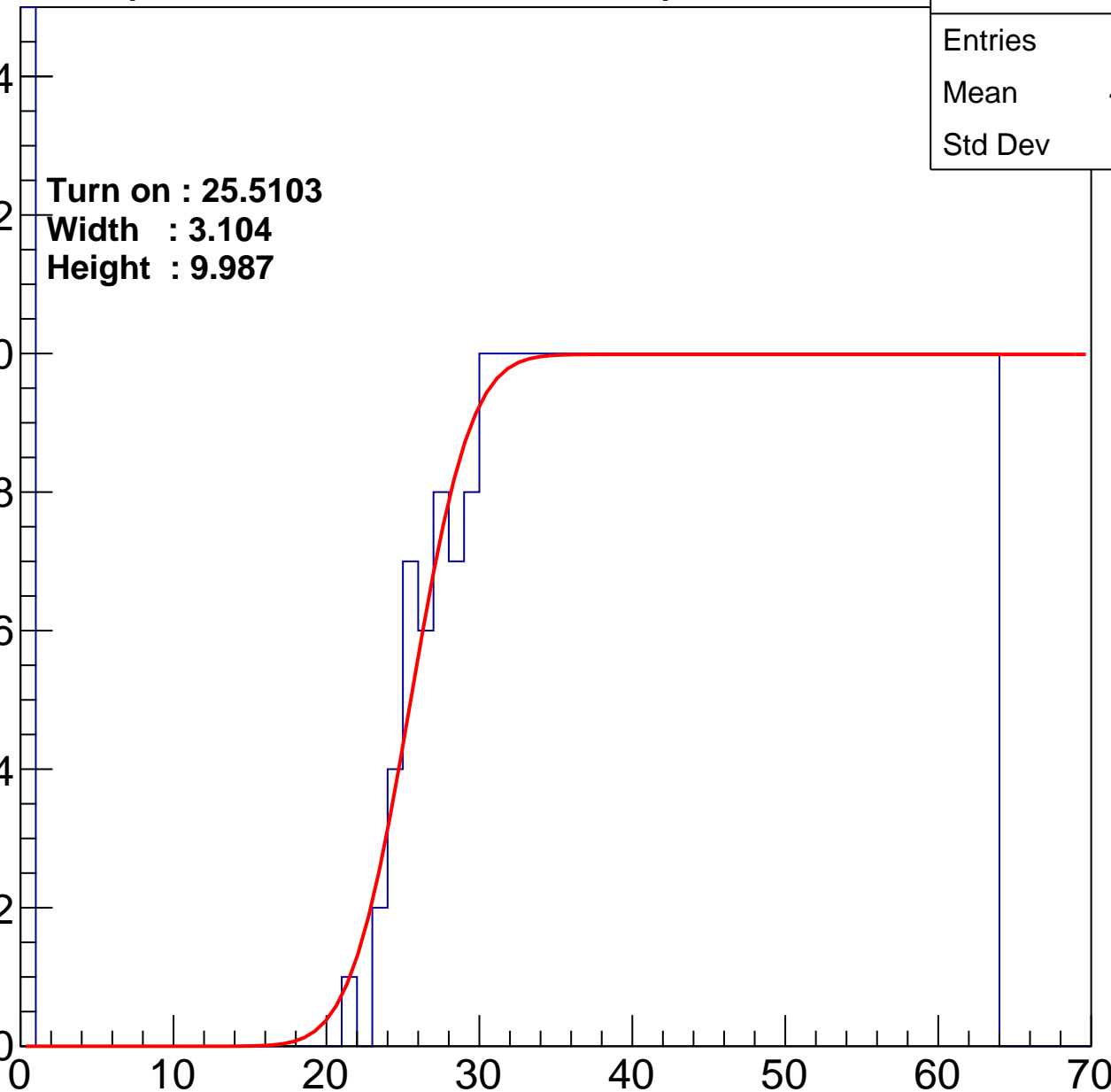
Width : 3.104

Height : 9.987

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch37

calib_packv5_041523_1651.root, FC#0, port C2

Entries	407
Mean	40.3
Std Dev	17.37

Turn on : 27.8289

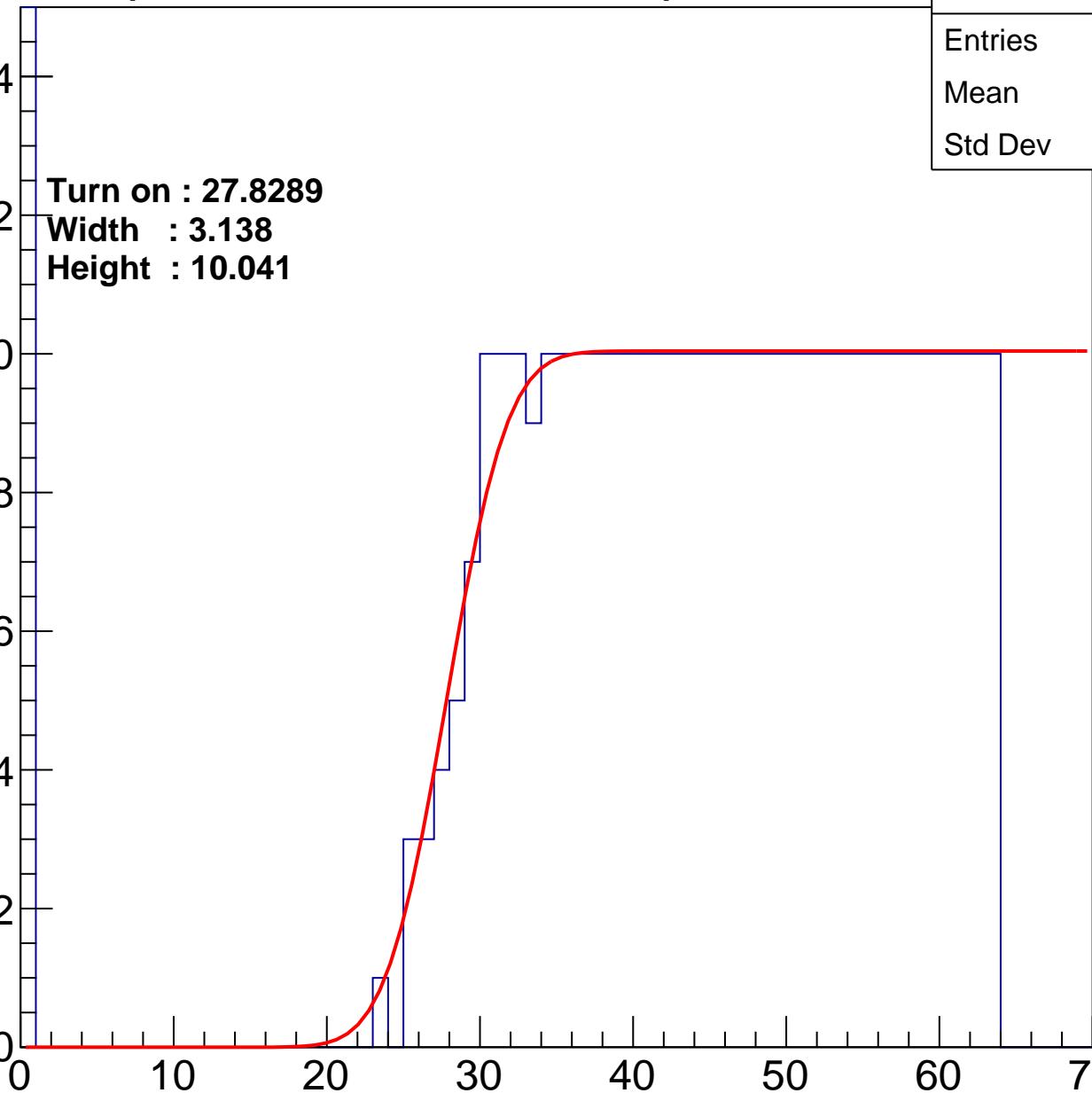
Width : 3.138

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch38

calib_packv5_041523_1651.root, FC#0, port C2

Entries	446
Mean	39.19
Std Dev	16.82

Turn on : 23.3815

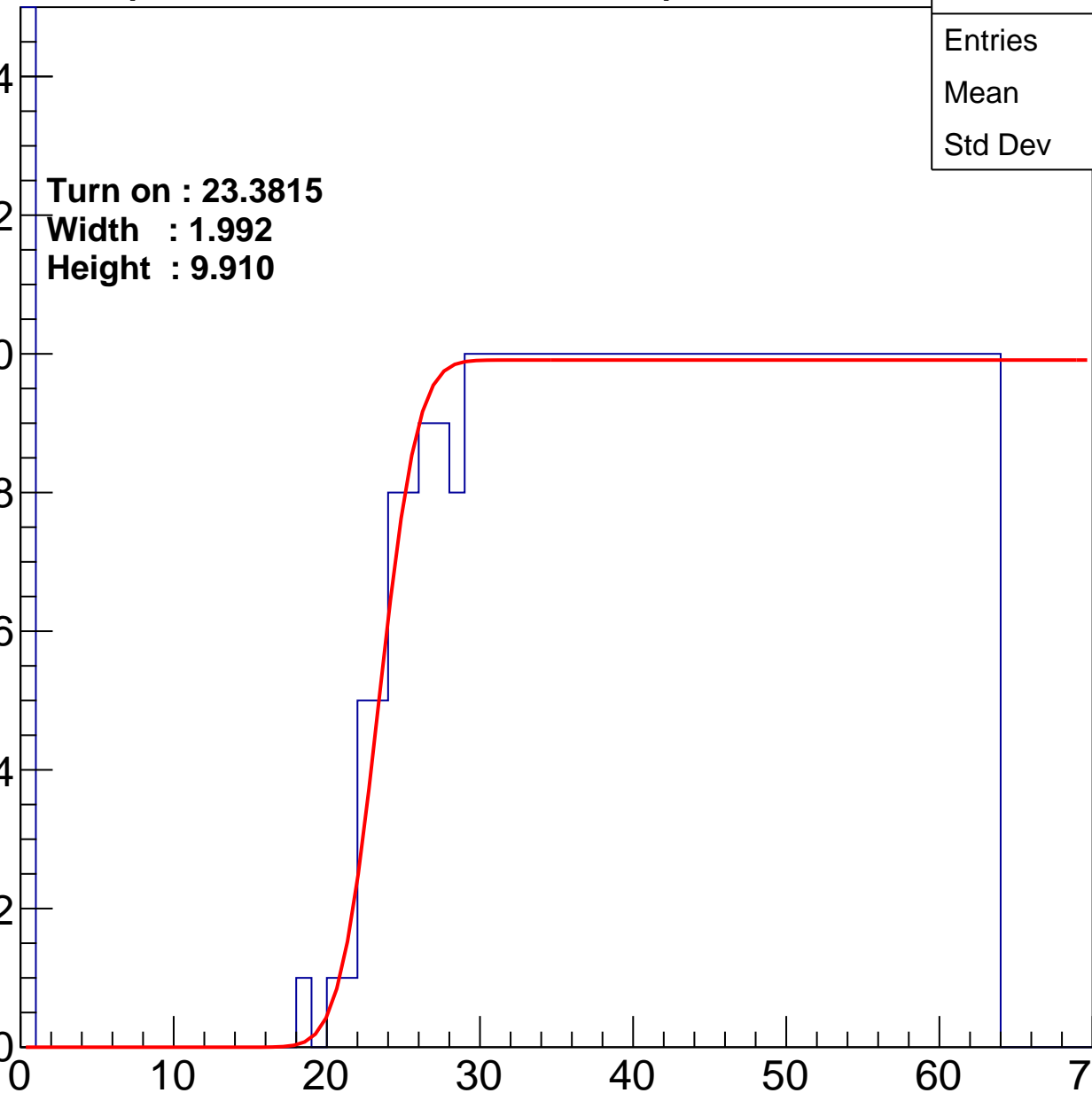
Width : 1.992

Height : 9.910

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch39

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	39.12
Std Dev	17.56

Turn on : 25.3513

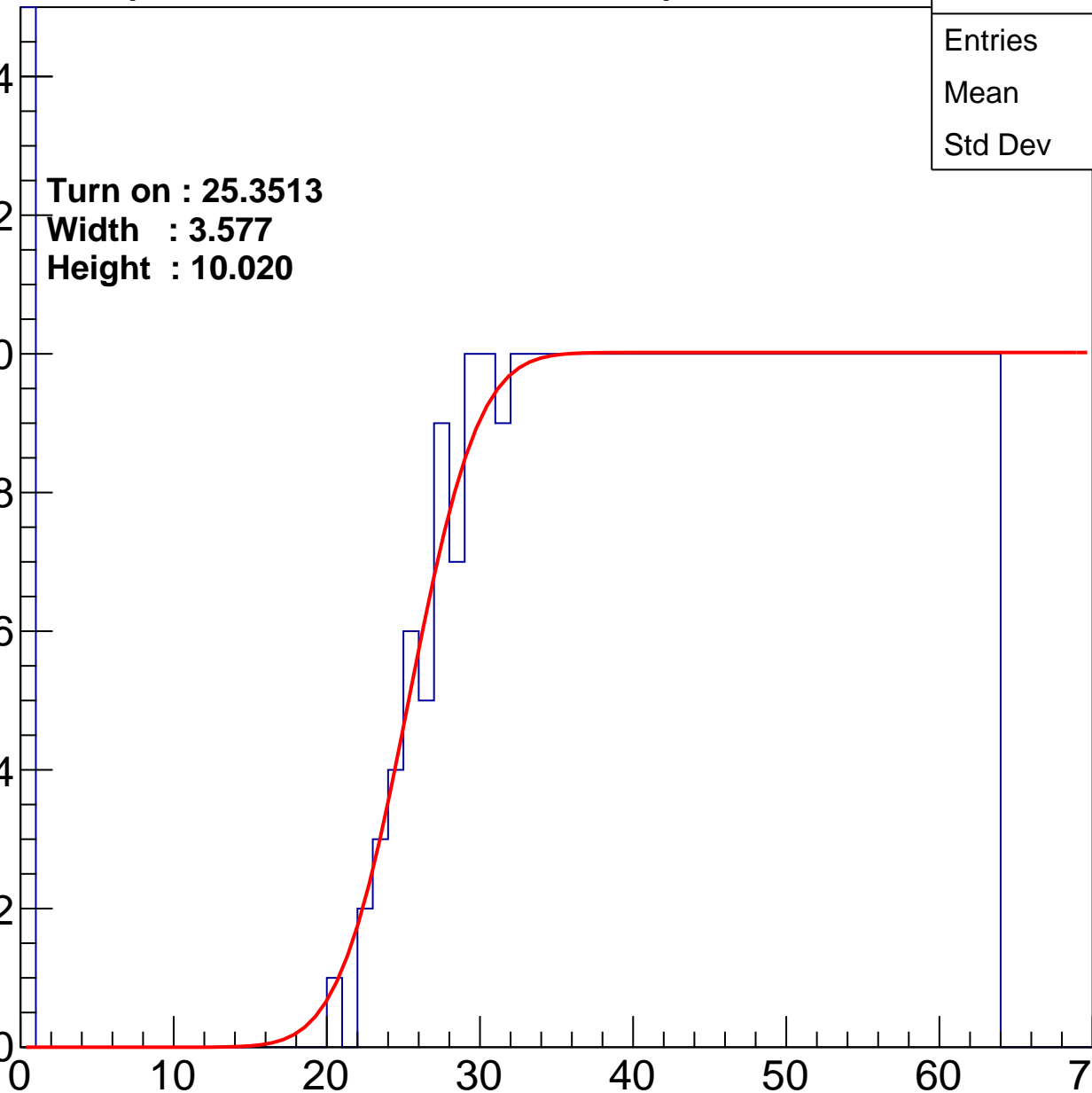
Width : 3.577

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch40

calib_packv5_041523_1651.root, FC#0, port C2

Entries	421
Mean	39.78
Std Dev	17.56

Turn on : 27.2644

Width : 2.674

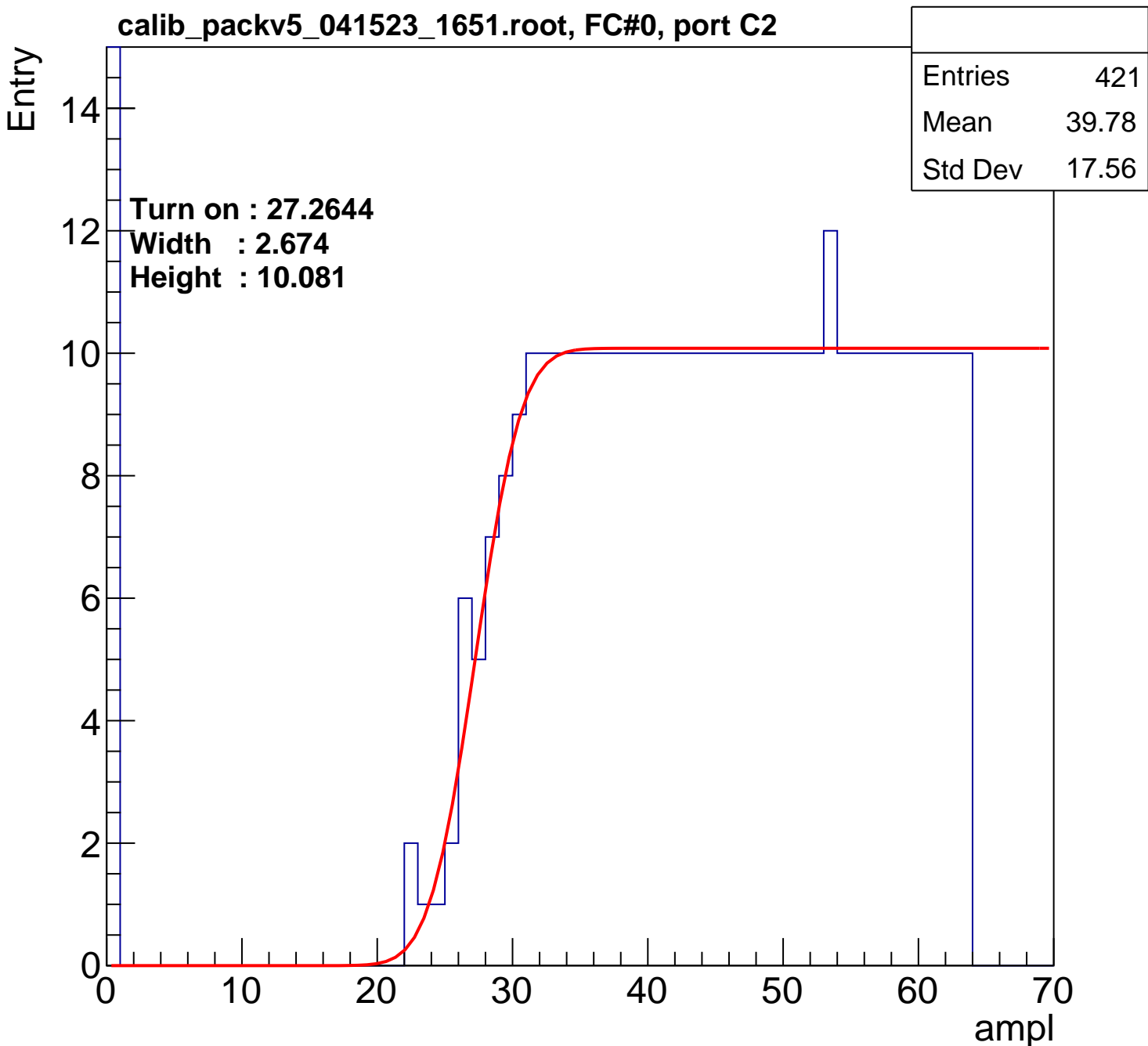
Height : 10.081

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U8-ch41

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	40.02
Std Dev	16.87

Turn on : 26.2727

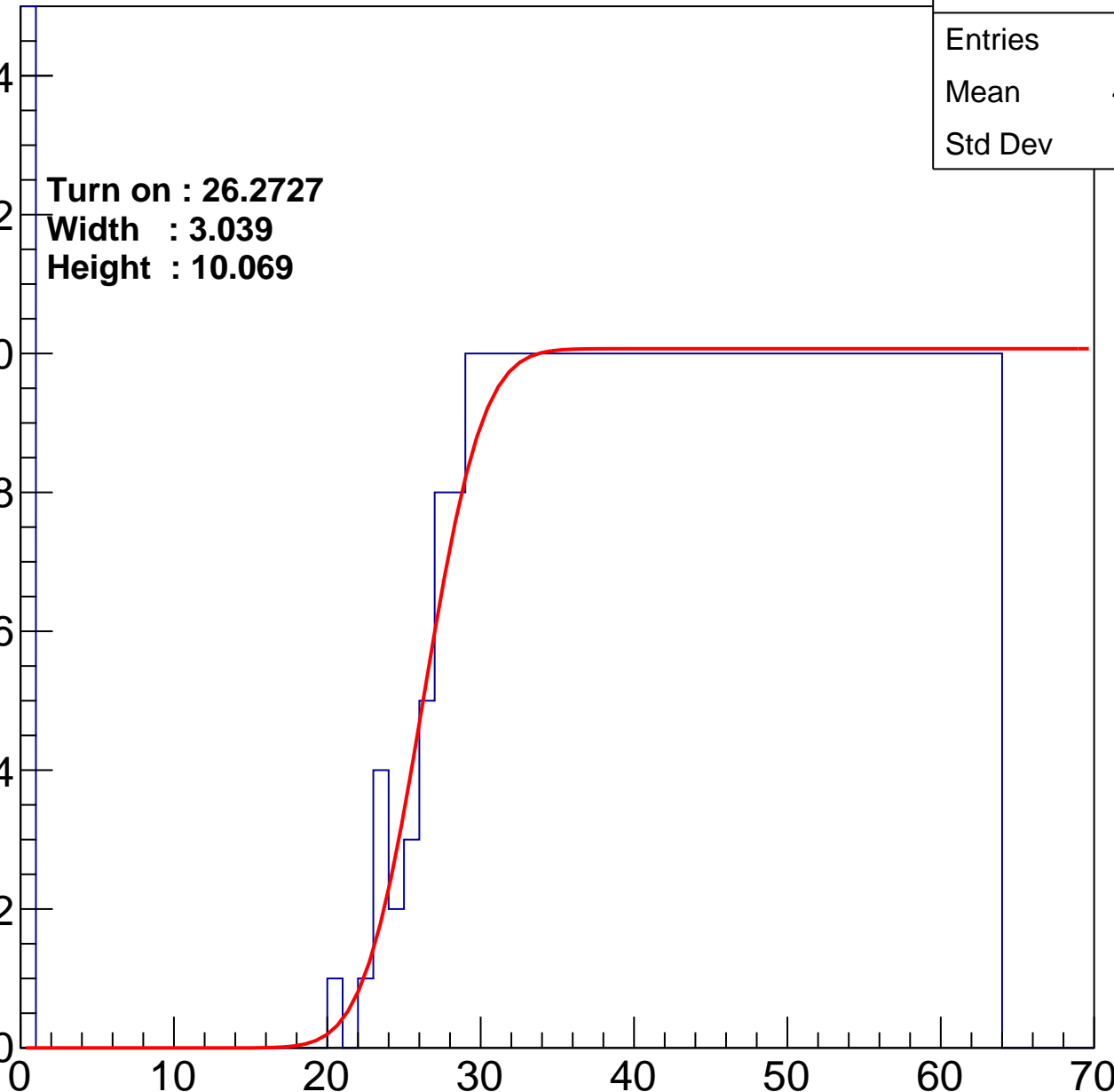
Width : 3.039

Height : 10.069

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch42

calib_packv5_041523_1651.root, FC#0, port C2

Entries	410
Mean	40.86
Std Dev	16.25

Turn on : 27.4704

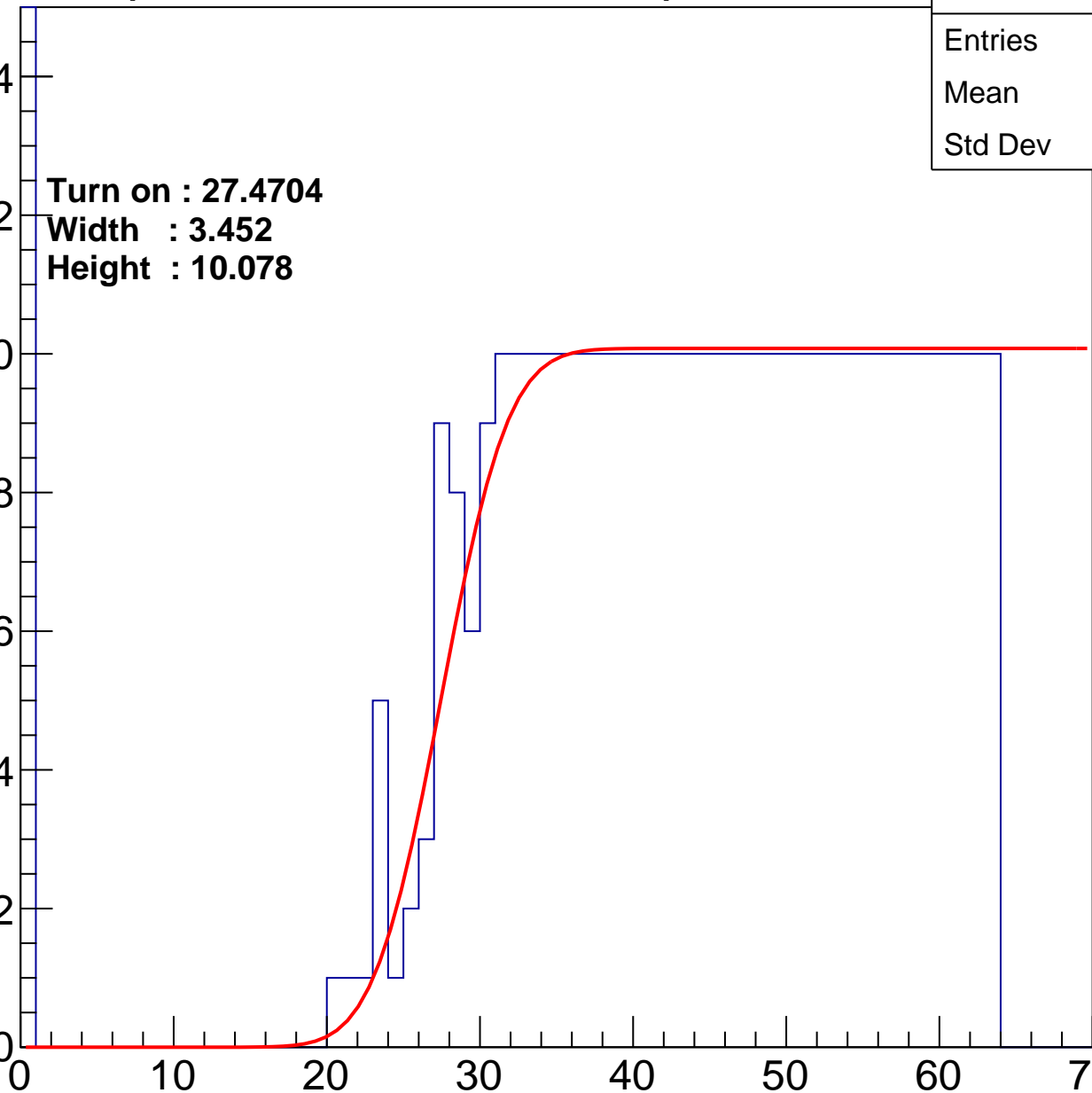
Width : 3.452

Height : 10.078

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch43

calib_packv5_041523_1651.root, FC#0, port C2

Entries	412
Mean	40.95
Std Dev	15.98

Turn on : 26.2029

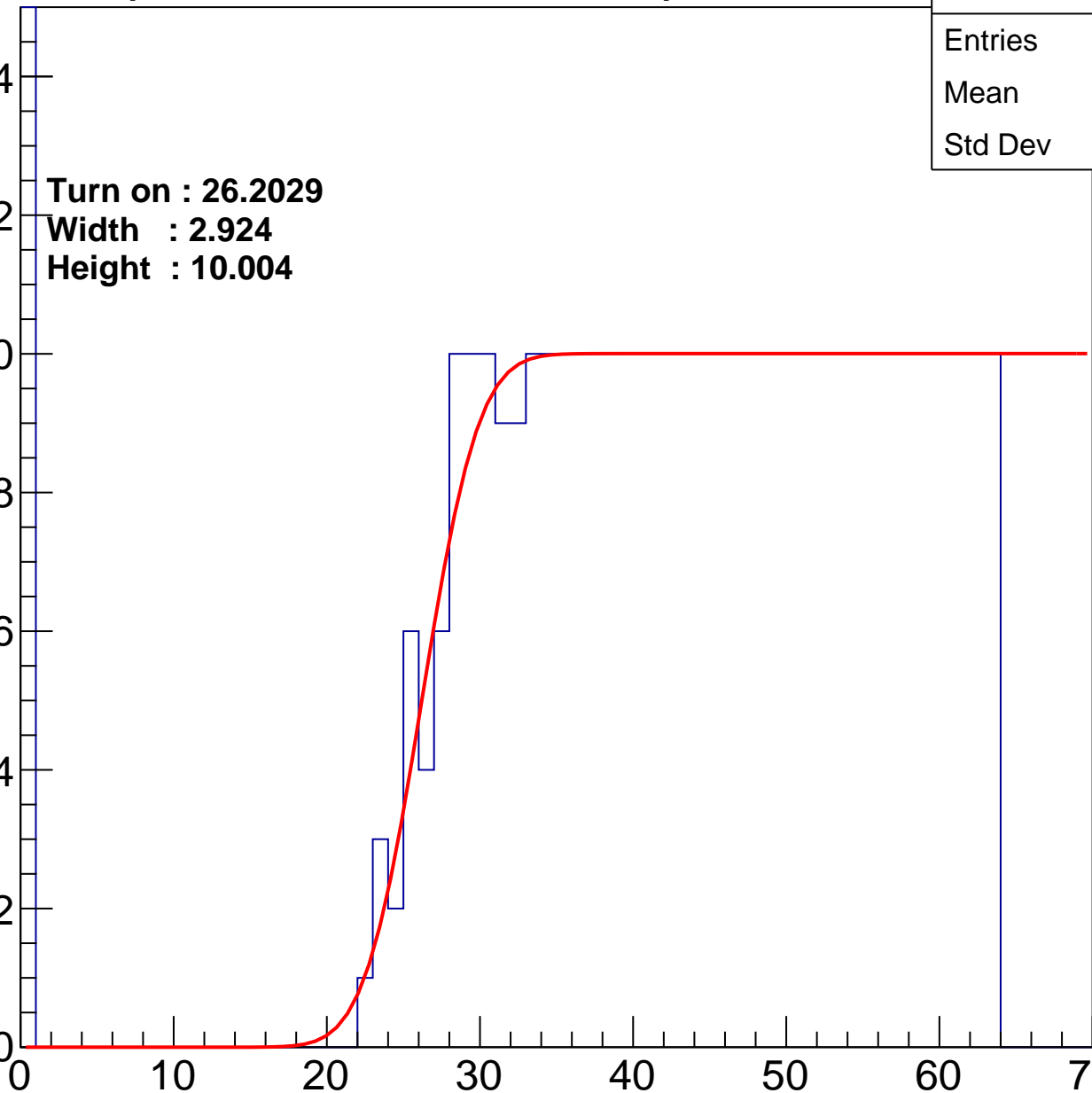
Width : 2.924

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch44

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	39.73
Std Dev	16.93

Turn on : 25.2295

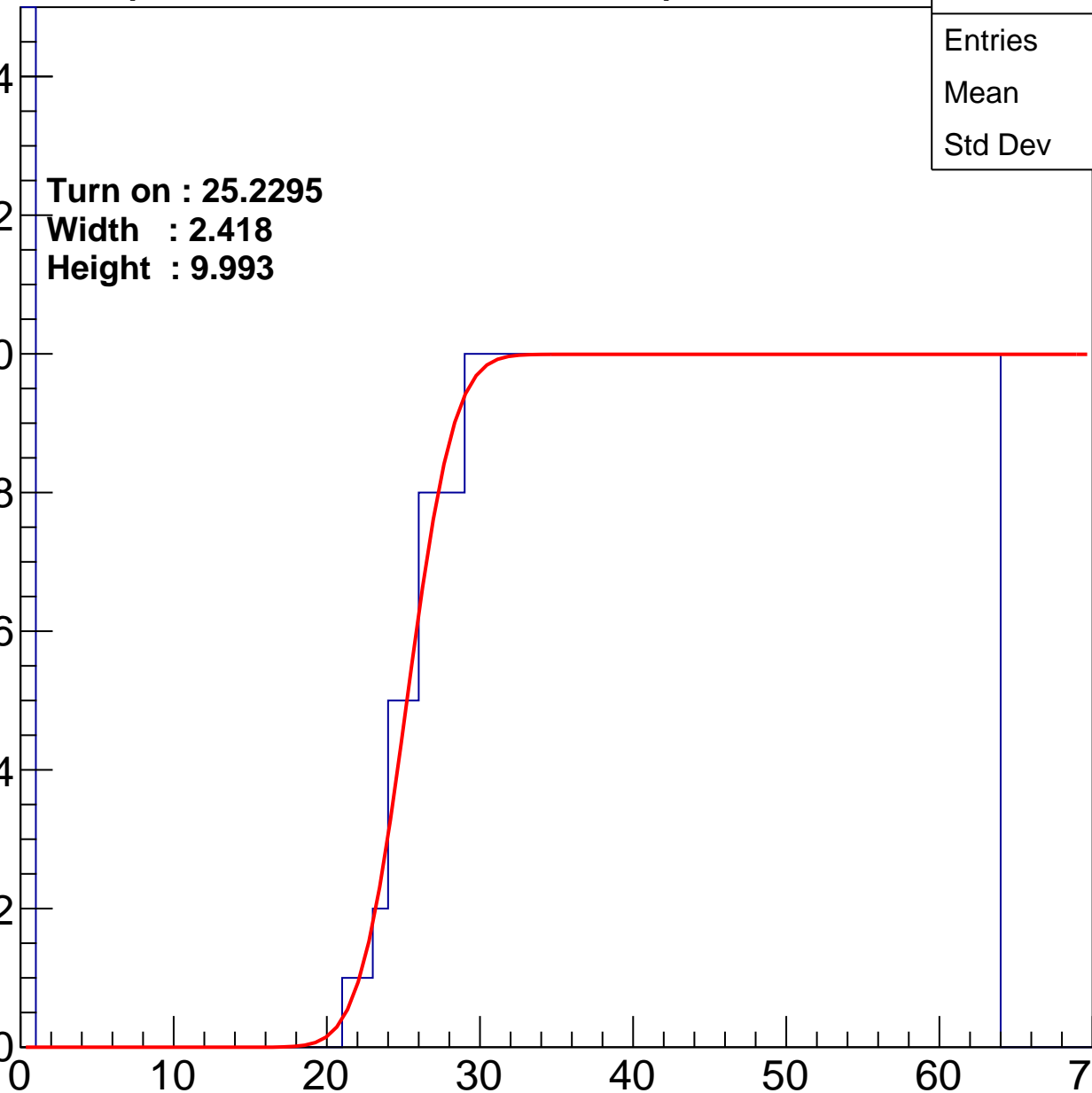
Width : 2.418

Height : 9.993

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch45

calib_packv5_041523_1651.root, FC#0, port C2

Entries	412
Mean	40.58
Std Dev	16.63

Turn on : 27.0115

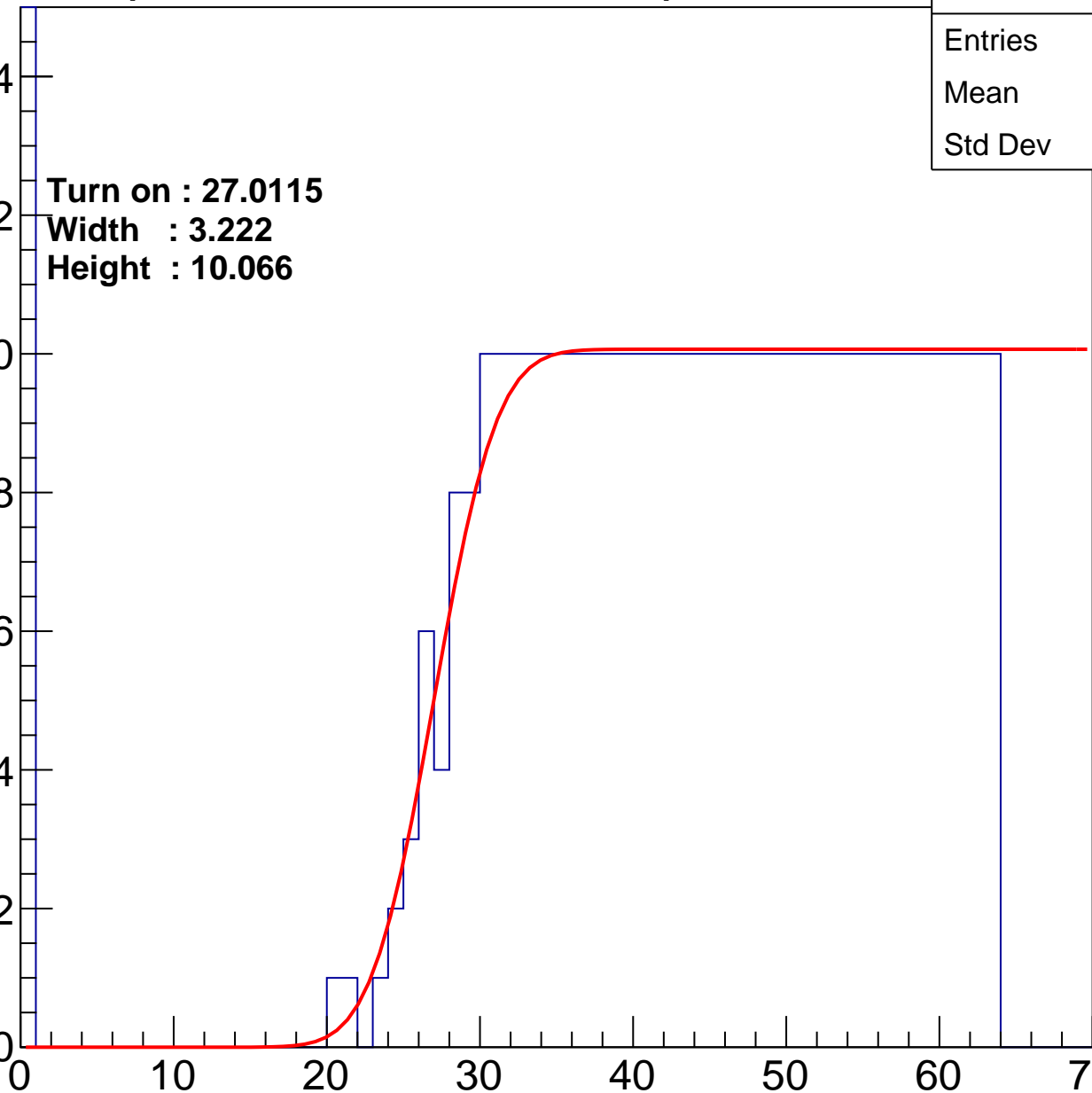
Width : 3.222

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch46

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	39.57
Std Dev	17.15

Turn on : 25.4636

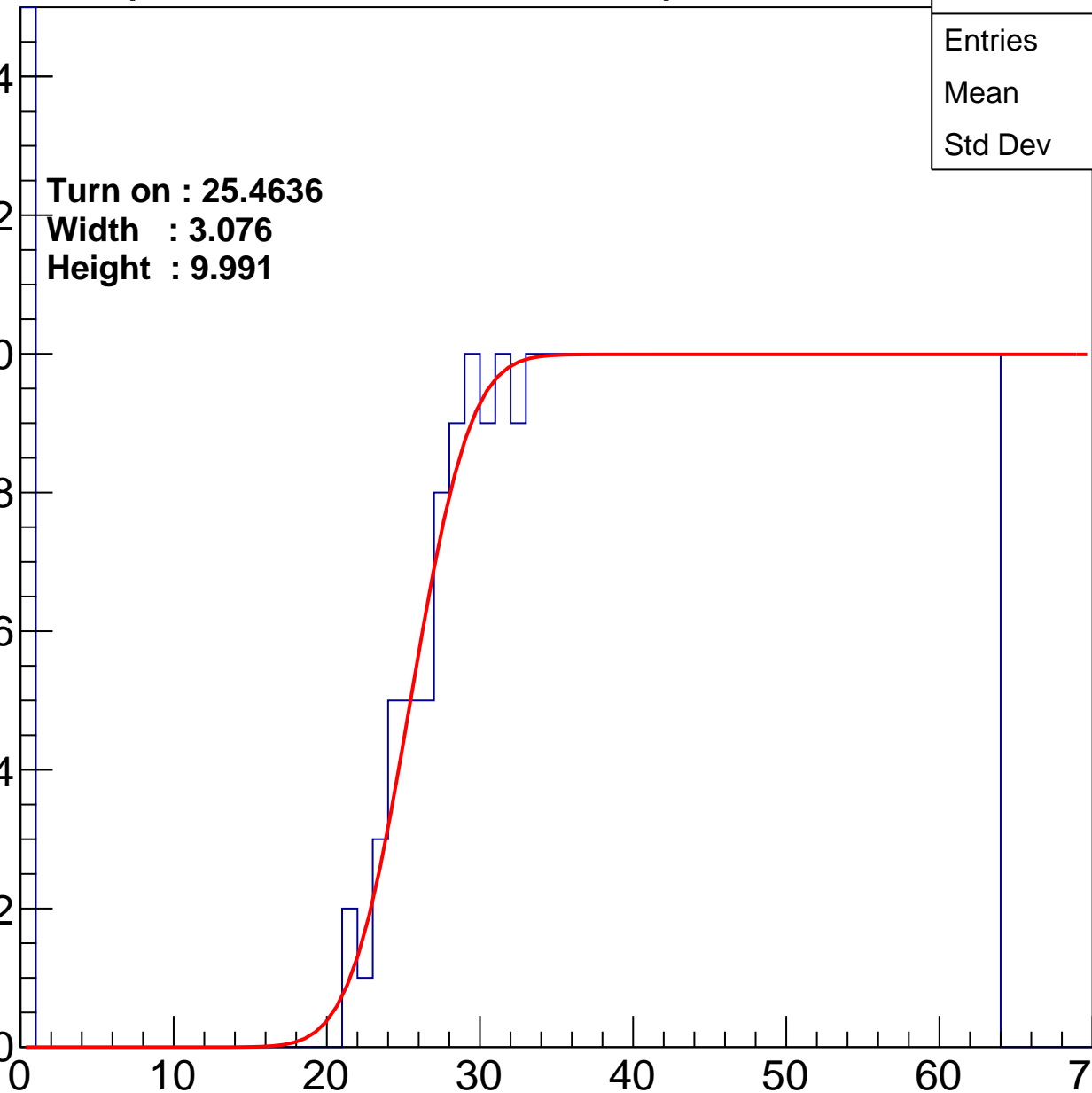
Width : 3.076

Height : 9.991

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch47

calib_packv5_041523_1651.root, FC#0, port C2

Entries	408
Mean	40.8
Std Dev	16.52

Turn on : 27.2017

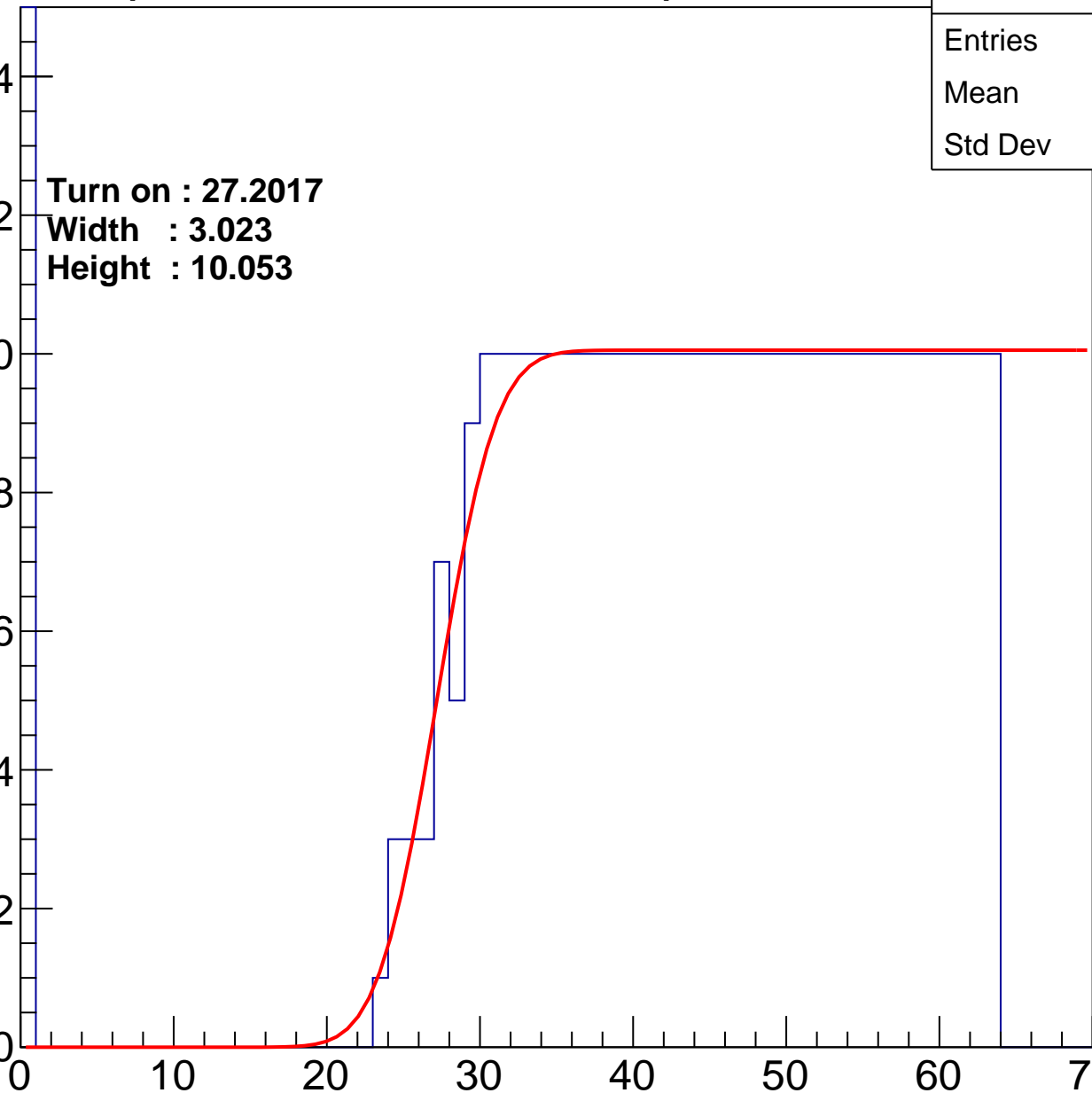
Width : 3.023

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch48

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	38.88
Std Dev	17.81

Turn on : 25.3705

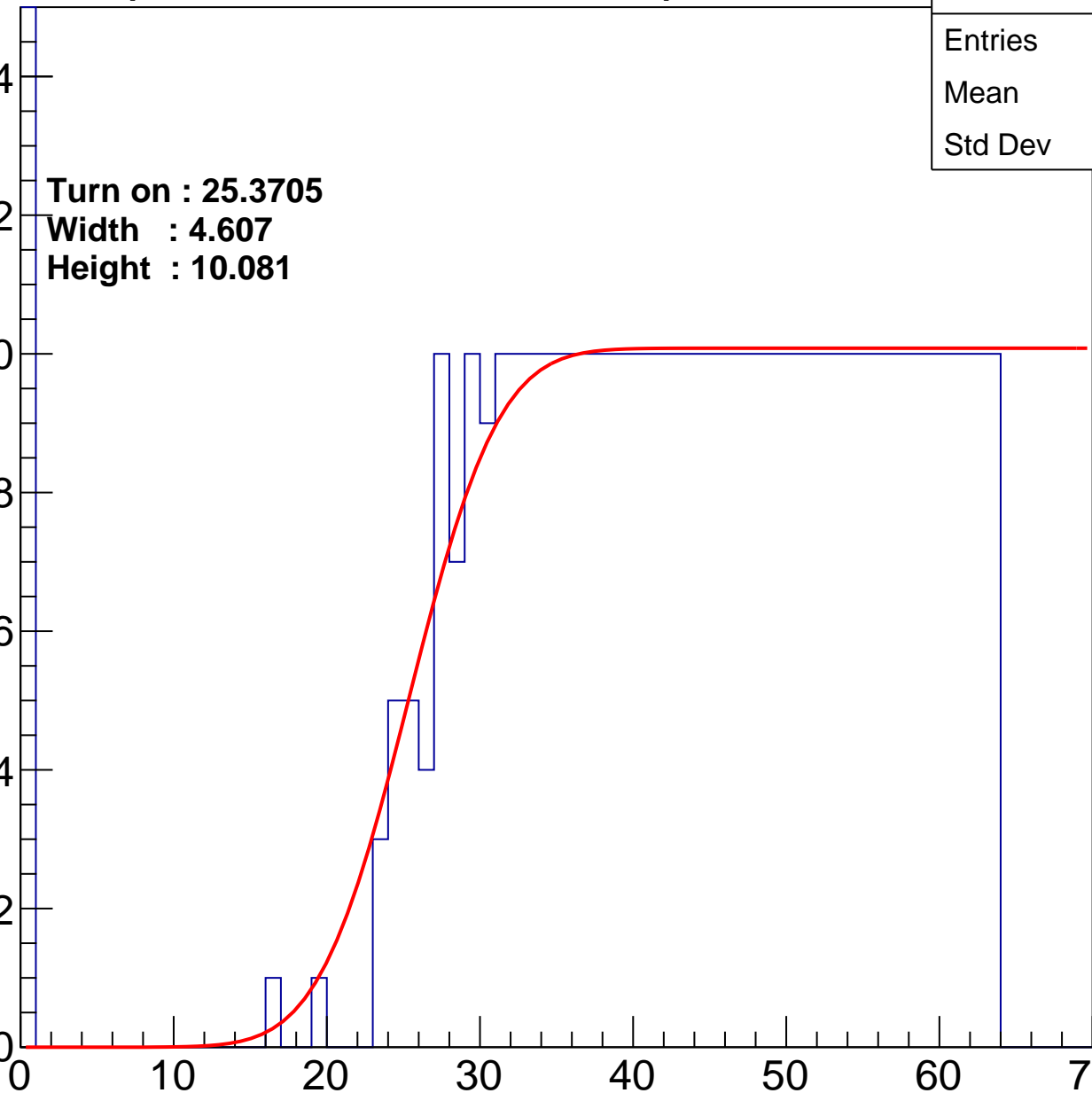
Width : 4.607

Height : 10.081

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch49

calib_packv5_041523_1651.root, FC#0, port C2

Entries	414
Mean	40.64
Std Dev	16.41

Turn on : 26.7895

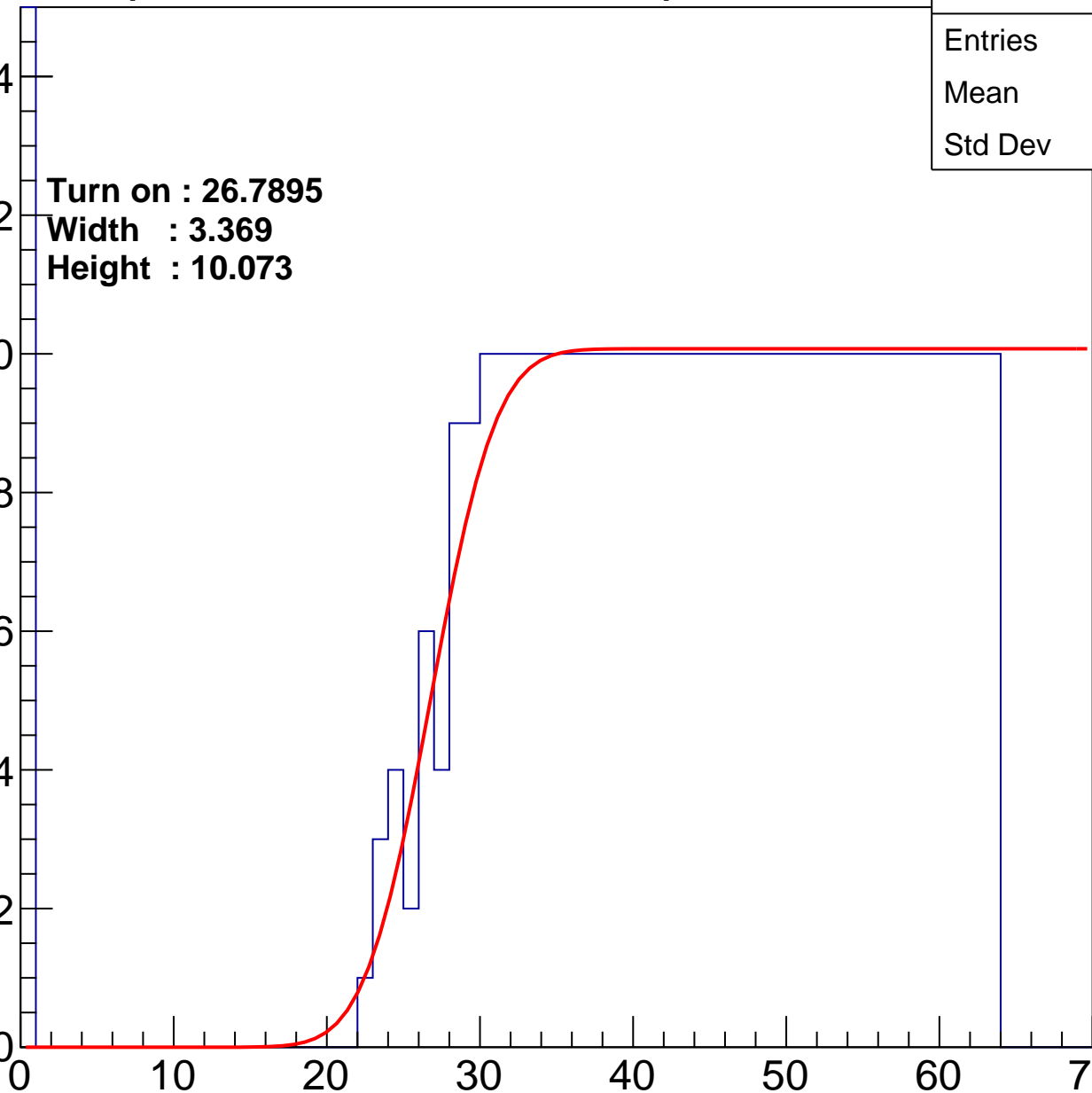
Width : 3.369

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch50

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	39.58
Std Dev	17.03

Turn on : 25.4644

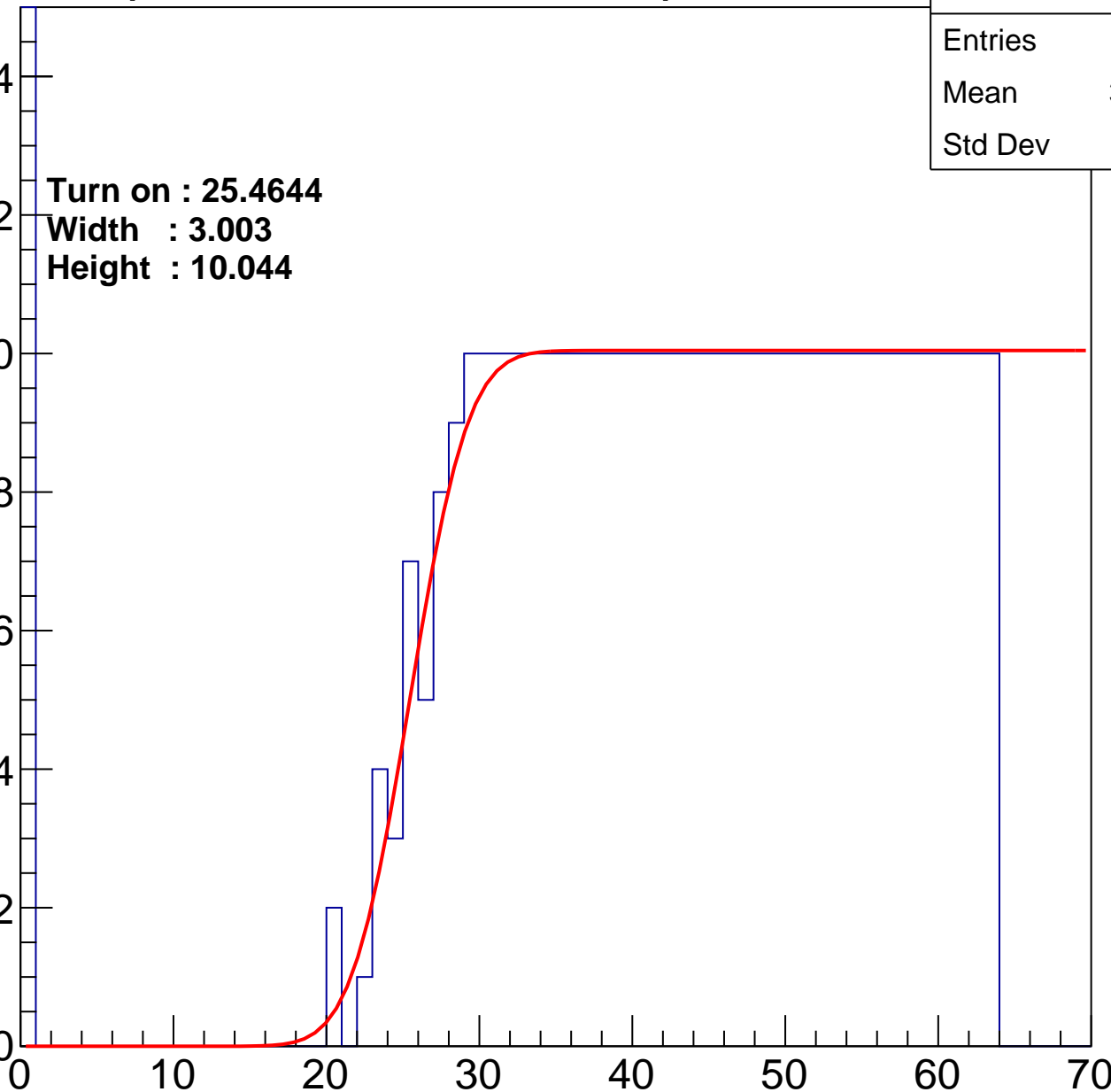
Width : 3.003

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch51

calib_packv5_041523_1651.root, FC#0, port C2

Entries	402
Mean	40.68
Std Dev	17.09

Turn on : 27.9207

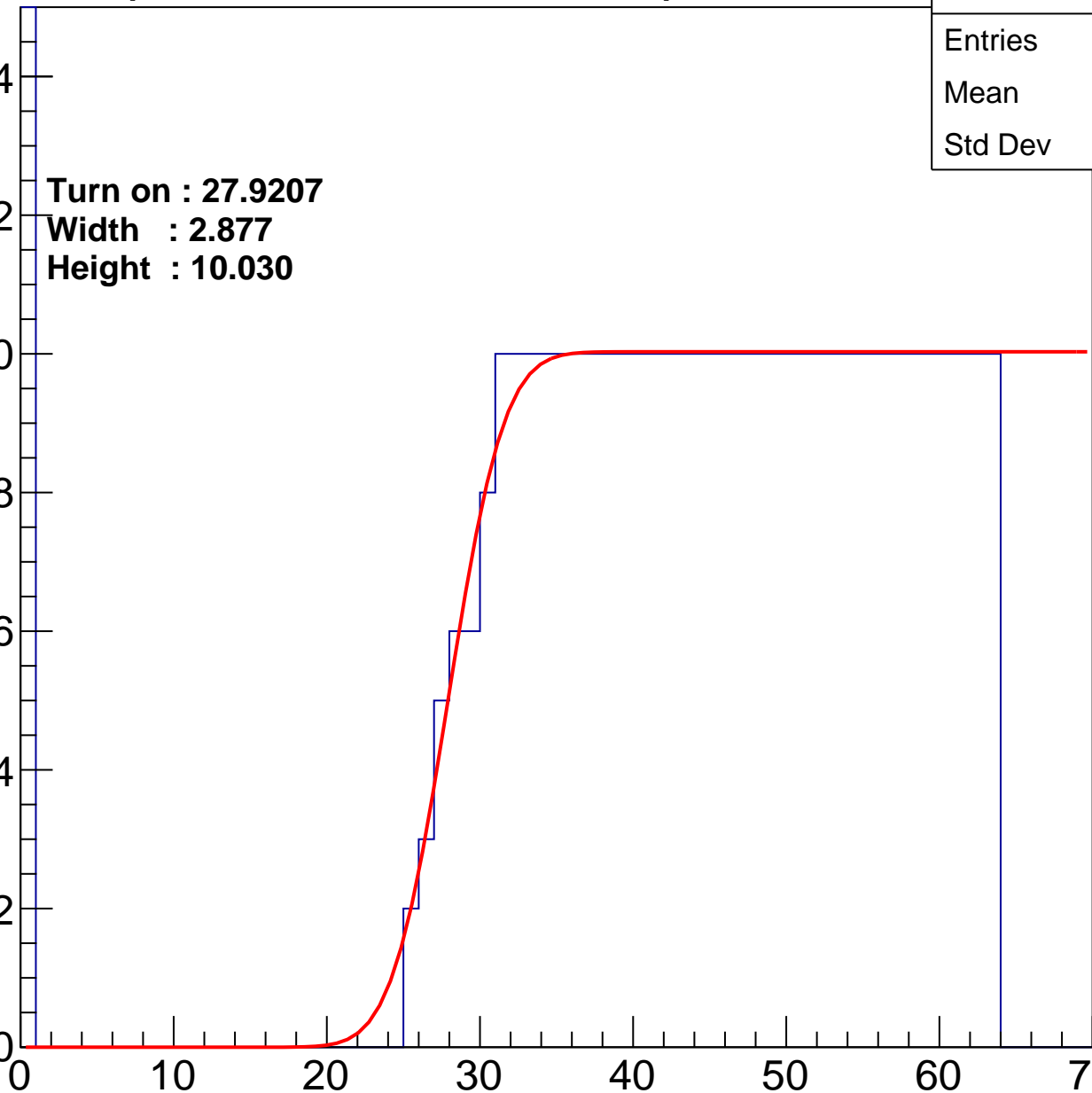
Width : 2.877

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch52

calib_packv5_041523_1651.root, FC#0, port C2

Entries	446
Mean	38.67
Std Dev	17.64

Turn on : 24.5967

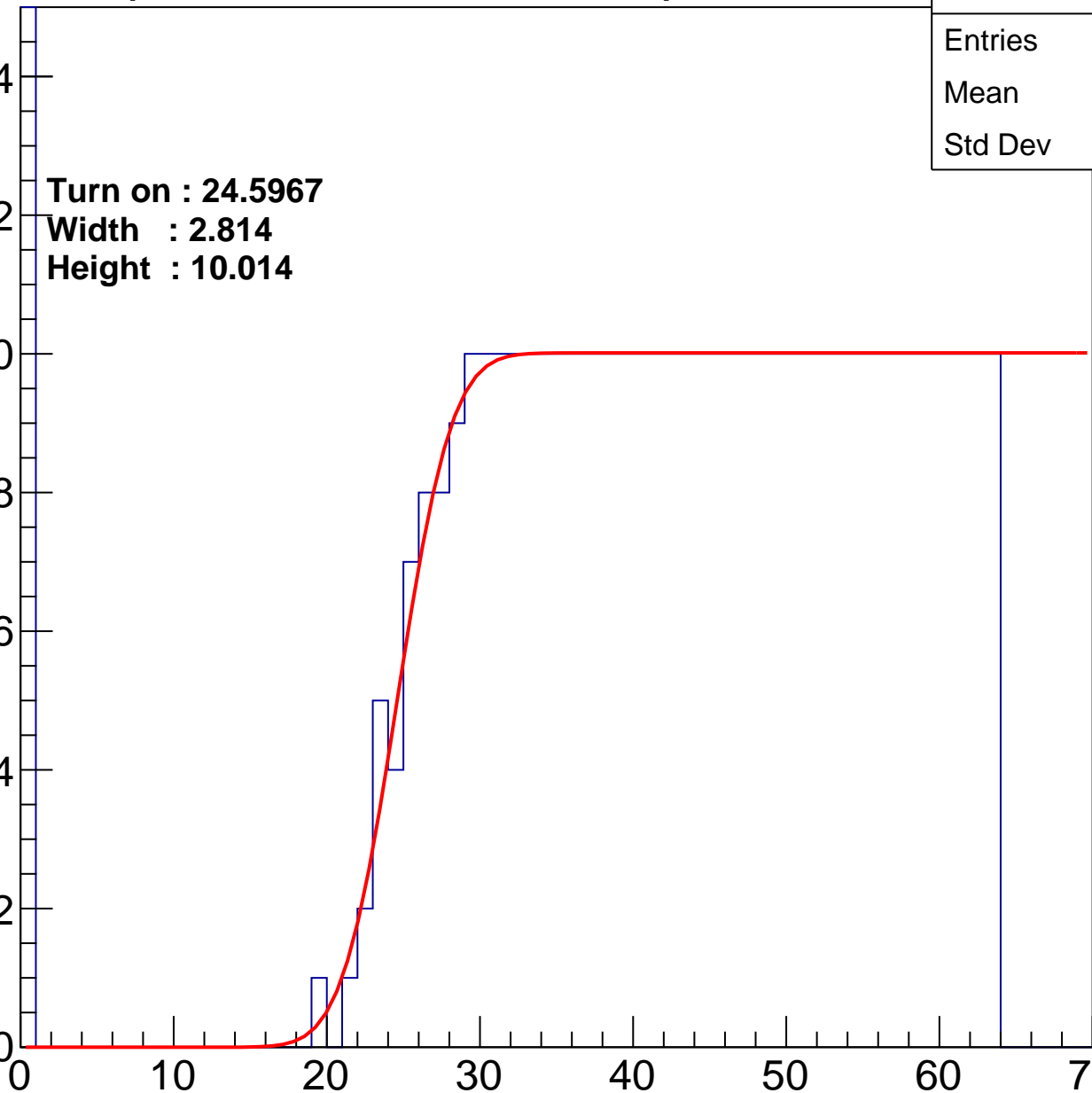
Width : 2.814

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch53

calib_packv5_041523_1651.root, FC#0, port C2

Entries	393
Mean	41.96
Std Dev	15.45

Turn on : 27.3700

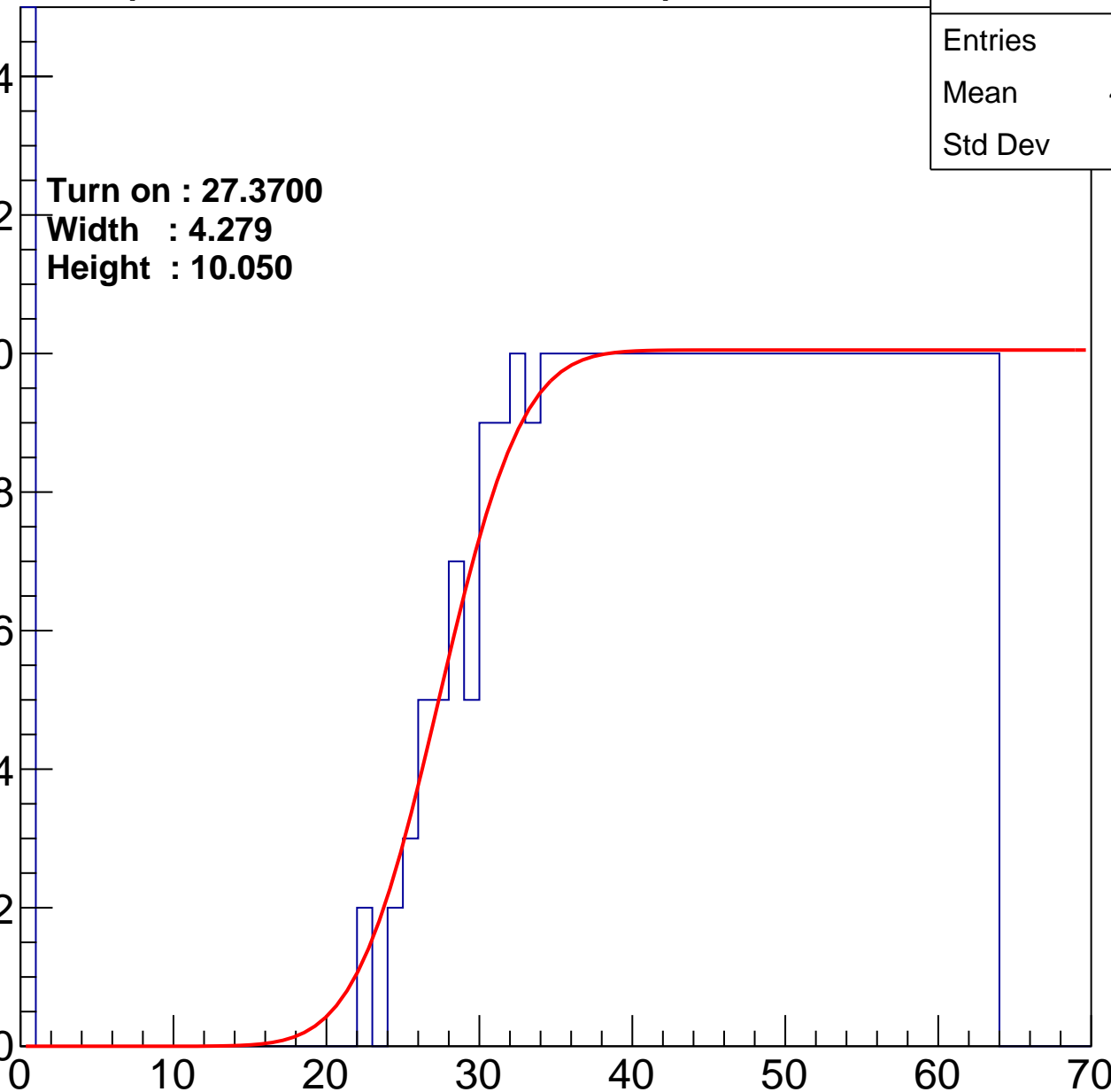
Width : 4.279

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch54

calib_packv5_041523_1651.root, FC#0, port C2

Entries	414
Mean	41.06
Std Dev	15.66

Turn on : 25.7555

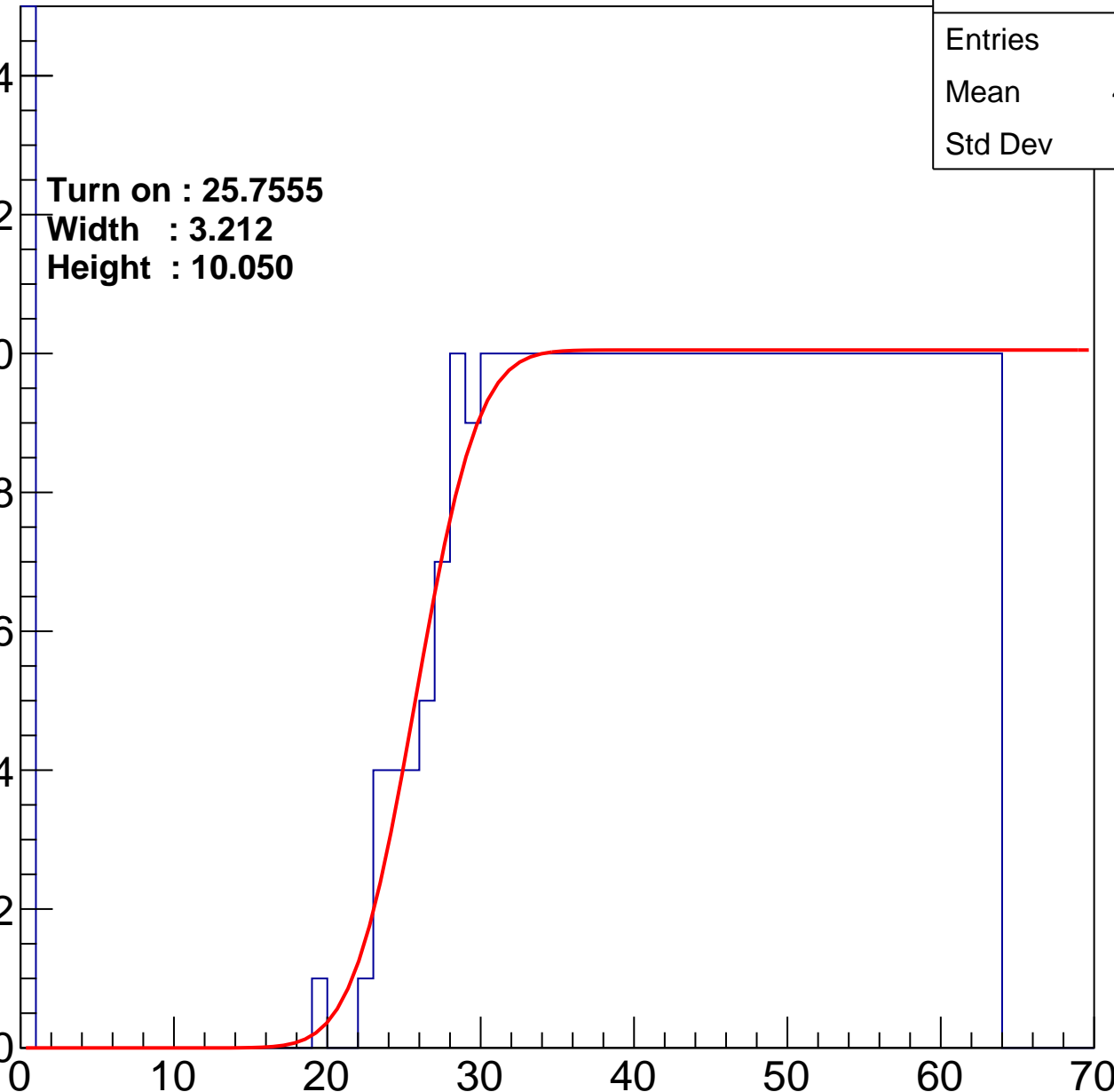
Width : 3.212

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch55

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	39.36
Std Dev	17.89

Turn on : 26.5529

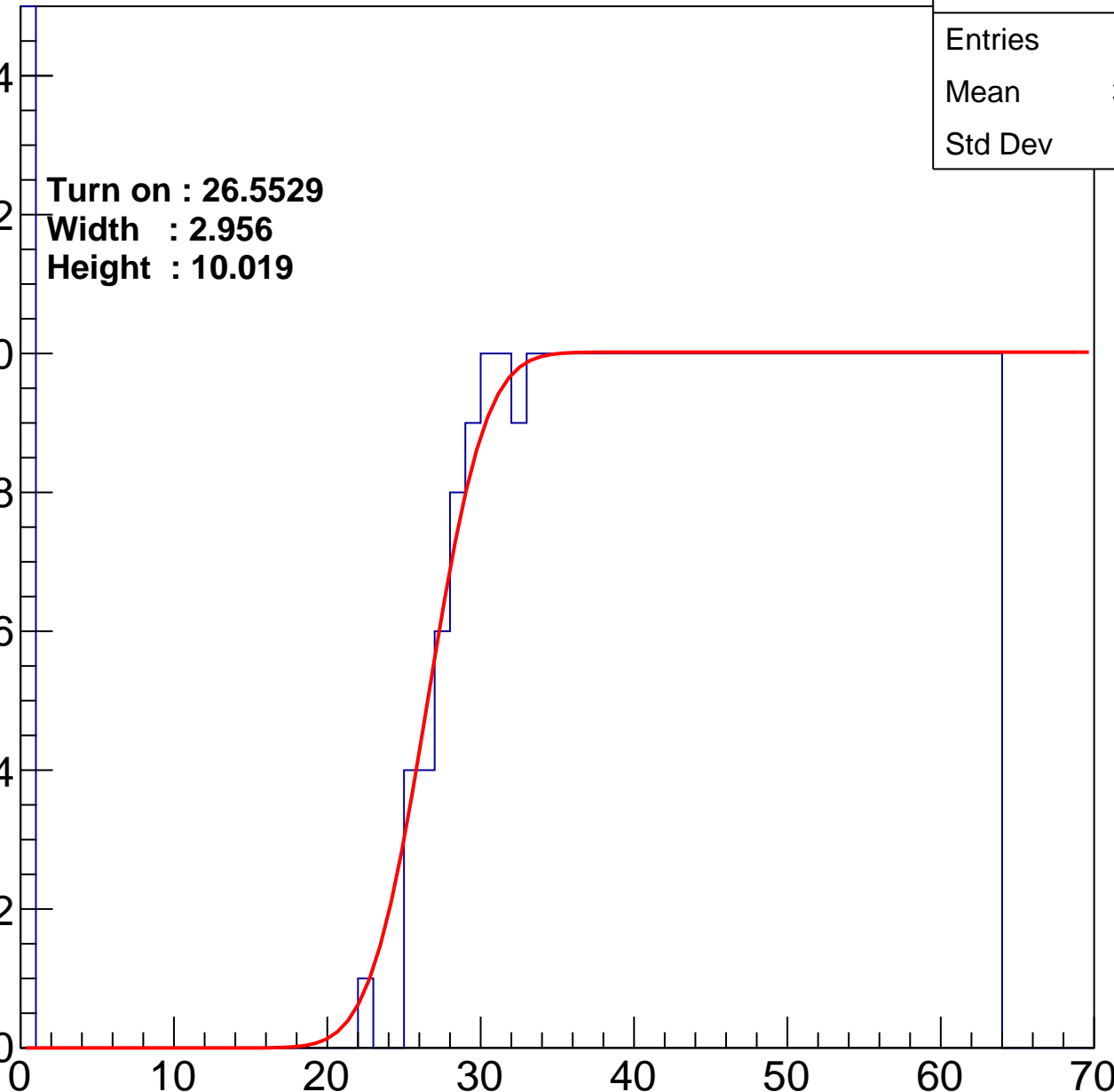
Width : 2.956

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch56

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	38.45
Std Dev	18.57

Turn on : 26.7292

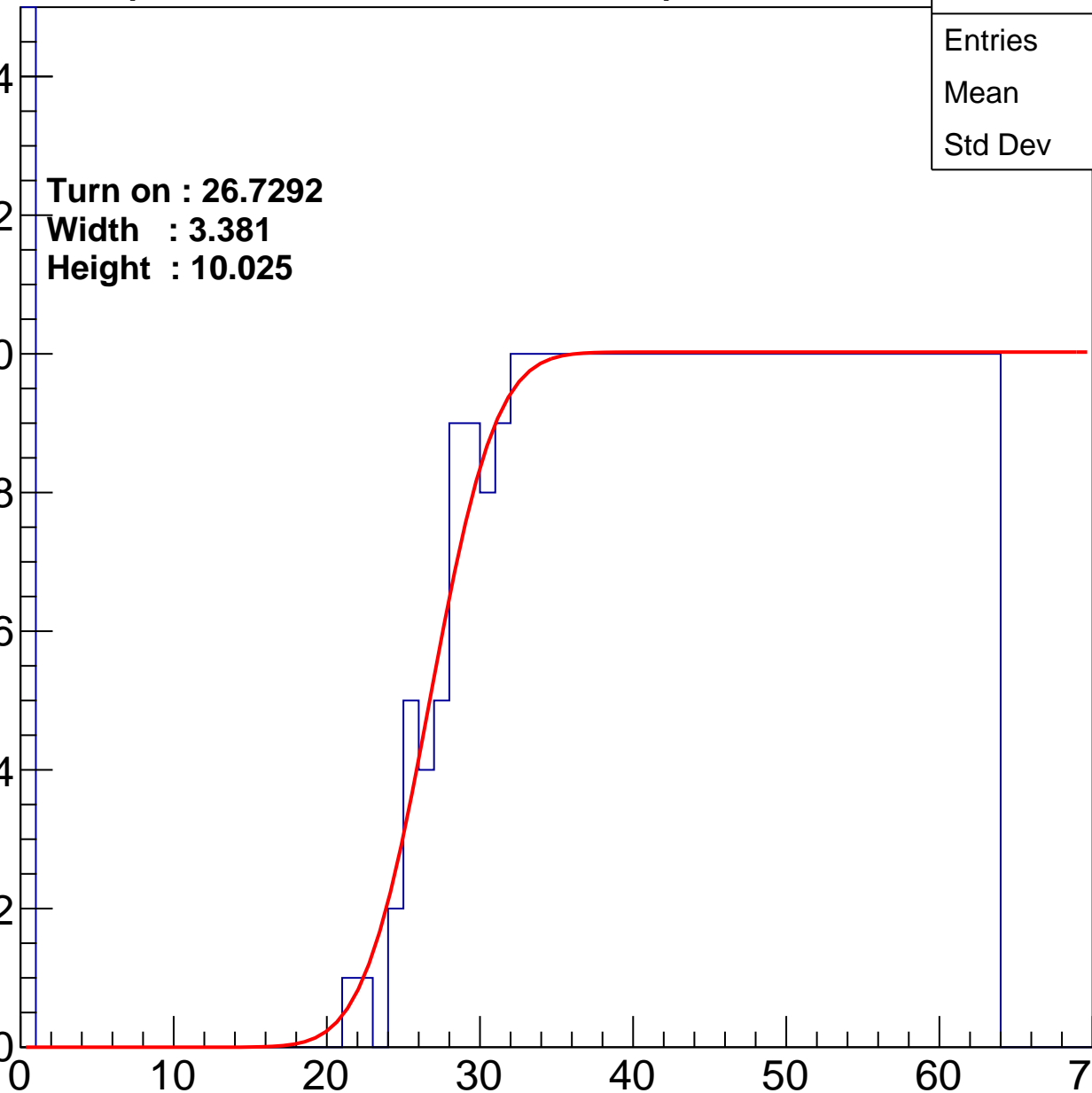
Width : 3.381

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch57

calib_packv5_041523_1651.root, FC#0, port C2

Entries	427
Mean	39.71
Std Dev	17.08

Turn on : 25.5659

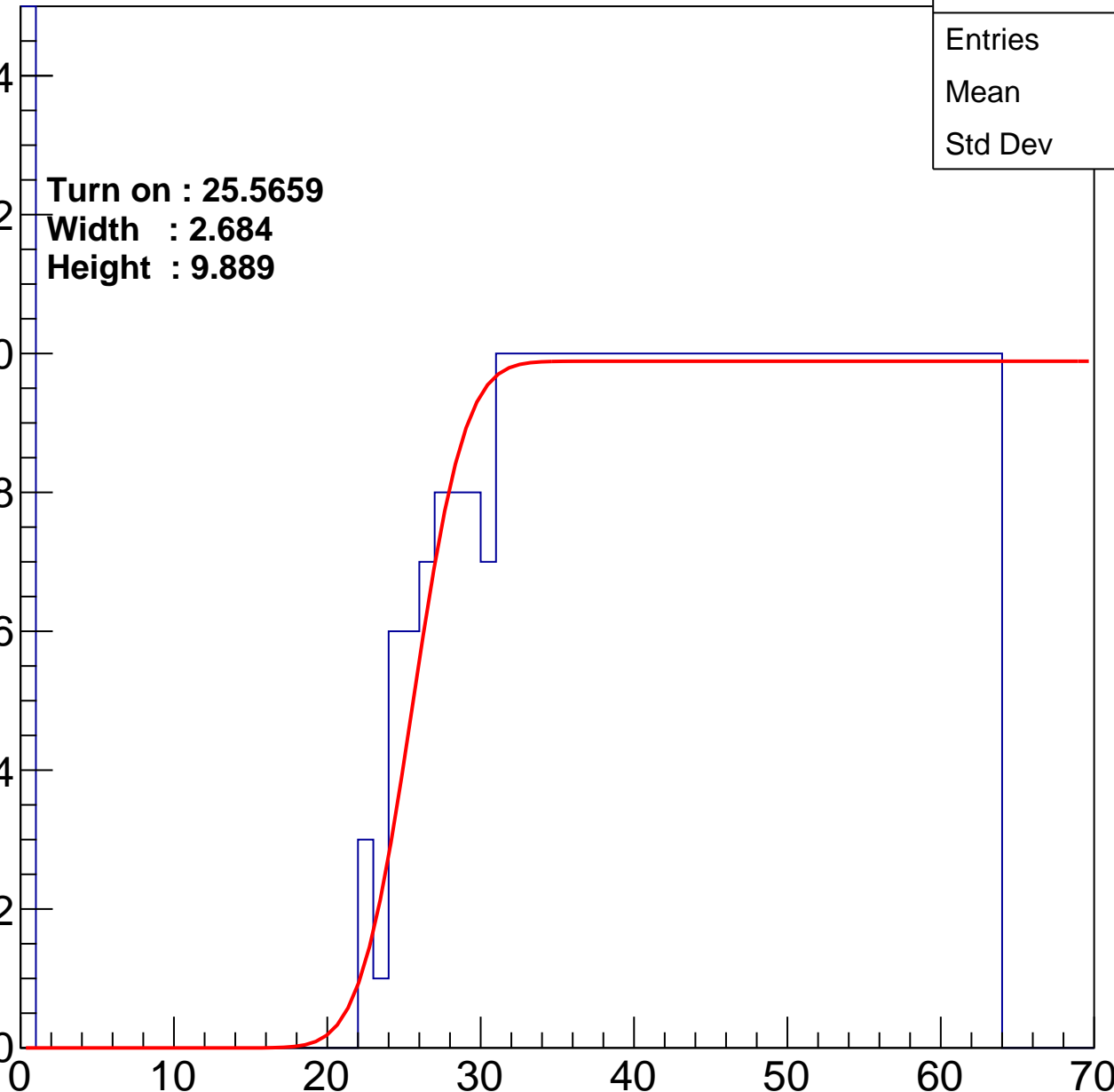
Width : 2.684

Height : 9.889

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch58

calib_packv5_041523_1651.root, FC#0, port C2

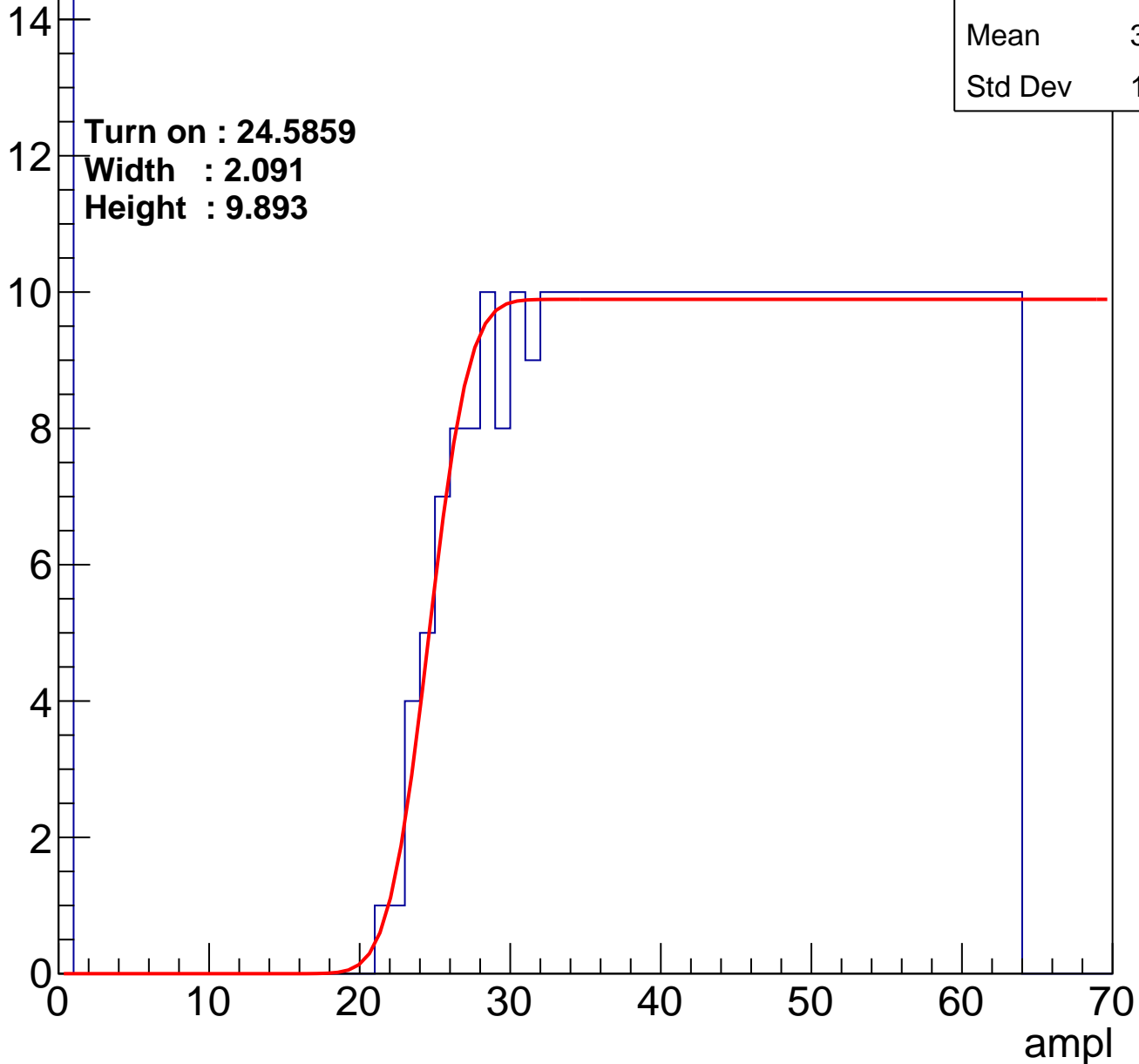
Entry

Entries	430
Mean	39.87
Std Dev	16.67

Turn on : 24.5859

Width : 2.091

Height : 9.893



B1L103S, U8-ch59

calib_packv5_041523_1651.root, FC#0, port C2

Entries	427
Mean	39.52
Std Dev	17.42

Turn on : 26.3604

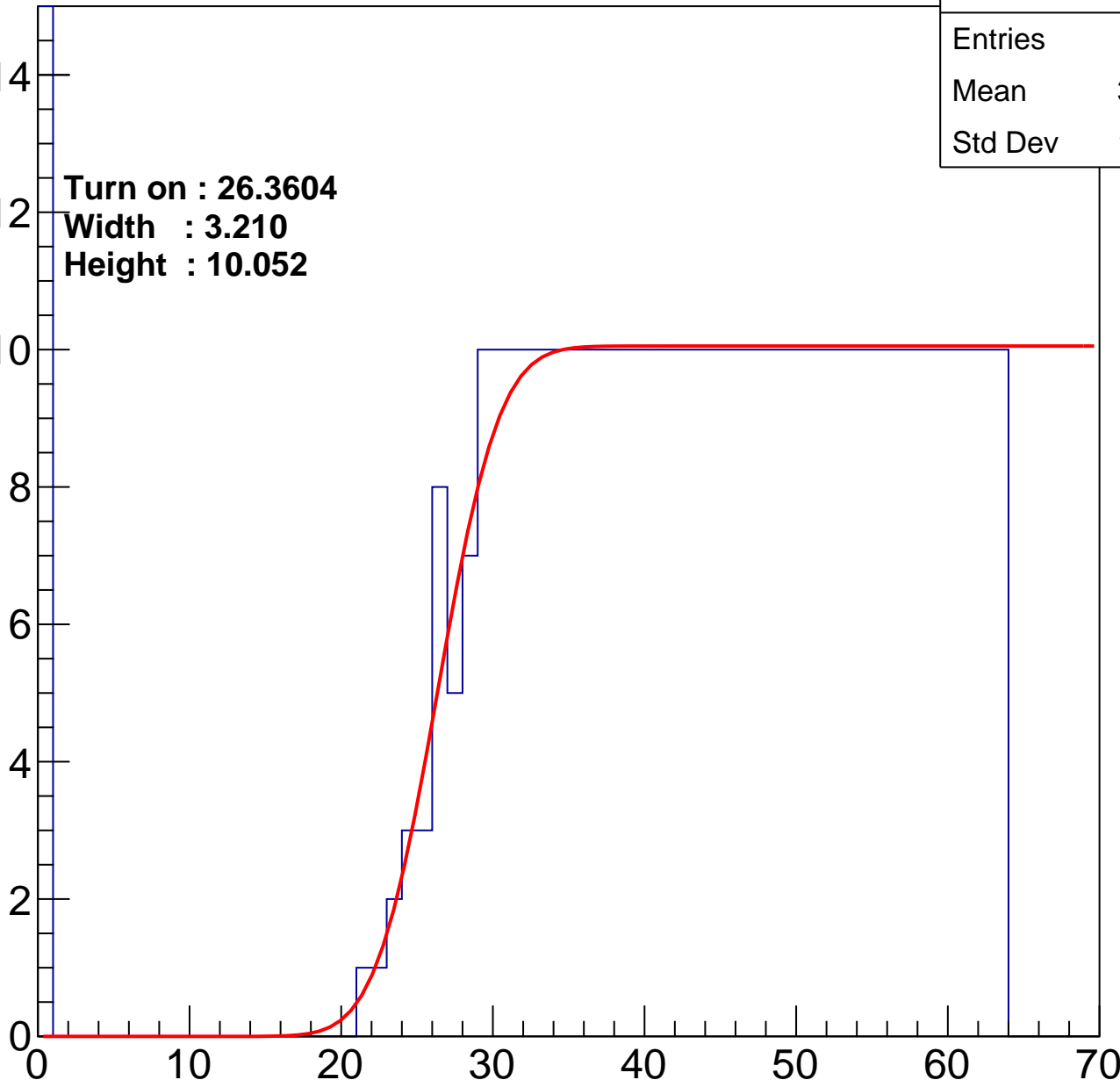
Width : 3.210

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch60

calib_packv5_041523_1651.root, FC#0, port C2

Entries	461
Mean	38.06
Std Dev	17.73

Turn on : 23.3123

Width : 3.187

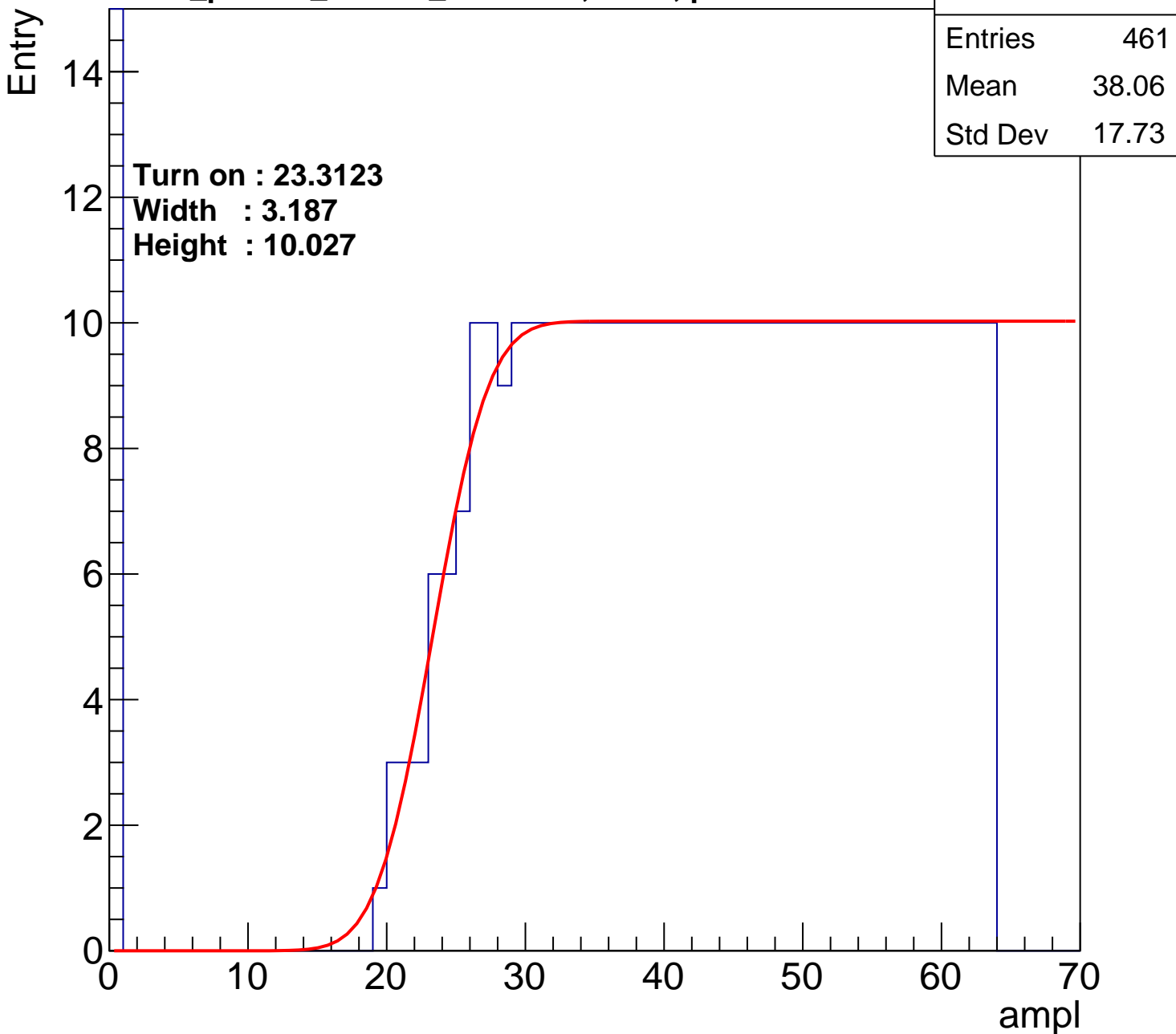
Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U8-ch61

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.41
Std Dev	17.48

Turn on : 25.3873

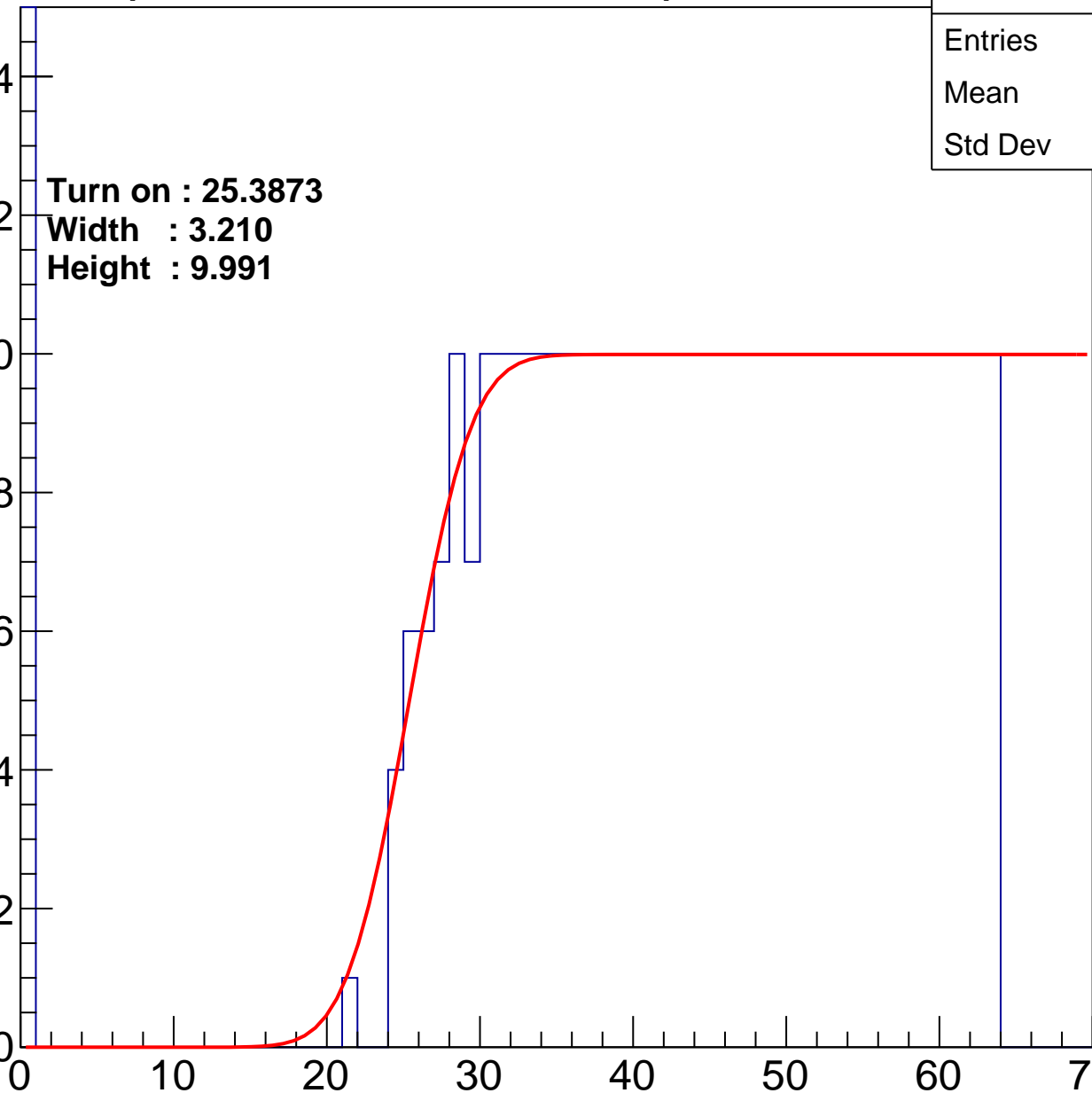
Width : 3.210

Height : 9.991

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch62

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	40.35
Std Dev	16.3

Turn on : 25.1180

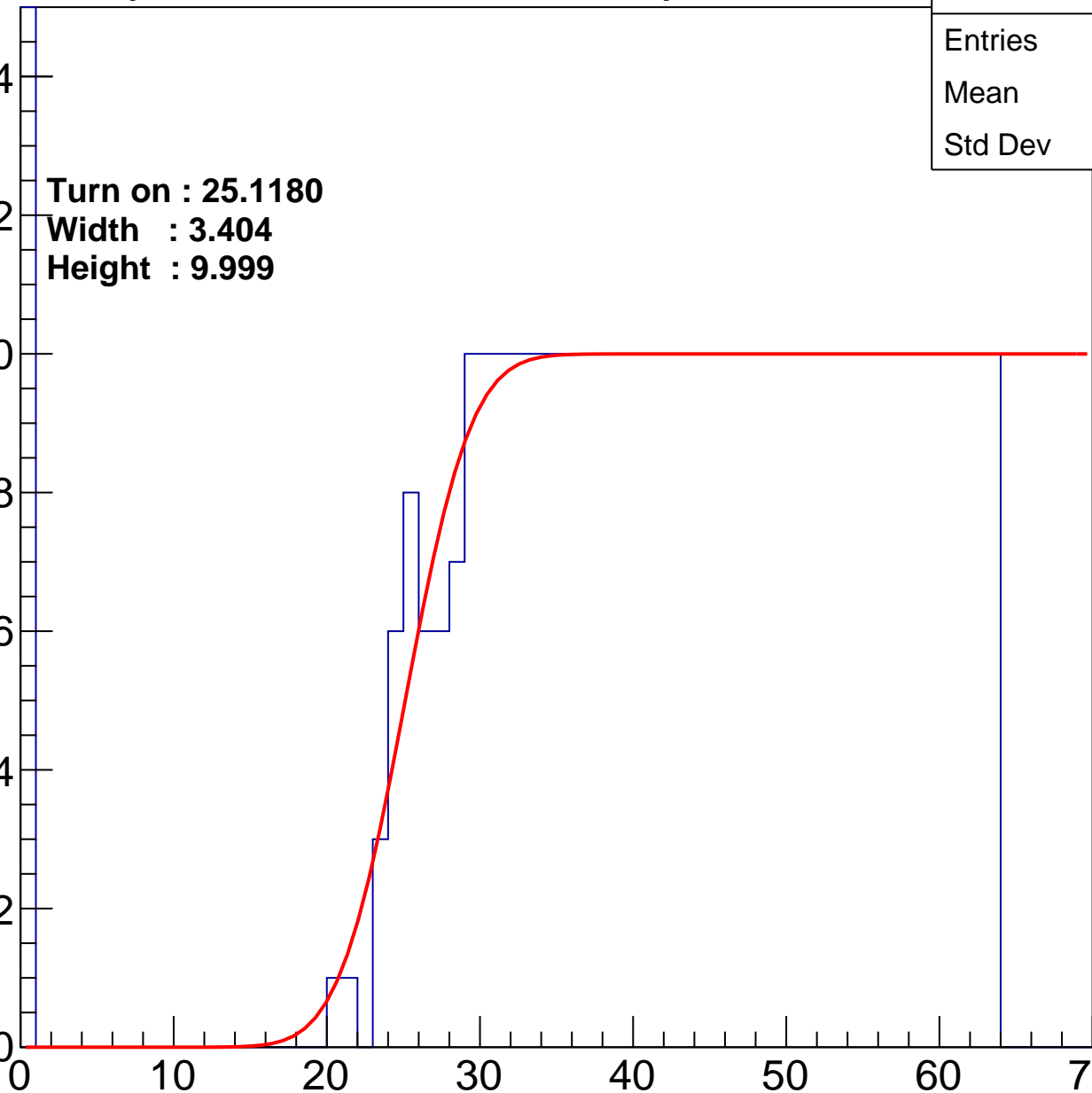
Width : 3.404

Height : 9.999

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch63

calib_packv5_041523_1651.root, FC#0, port C2

Entries	408
Mean	40.9
Std Dev	16.33

Turn on : 26.3360

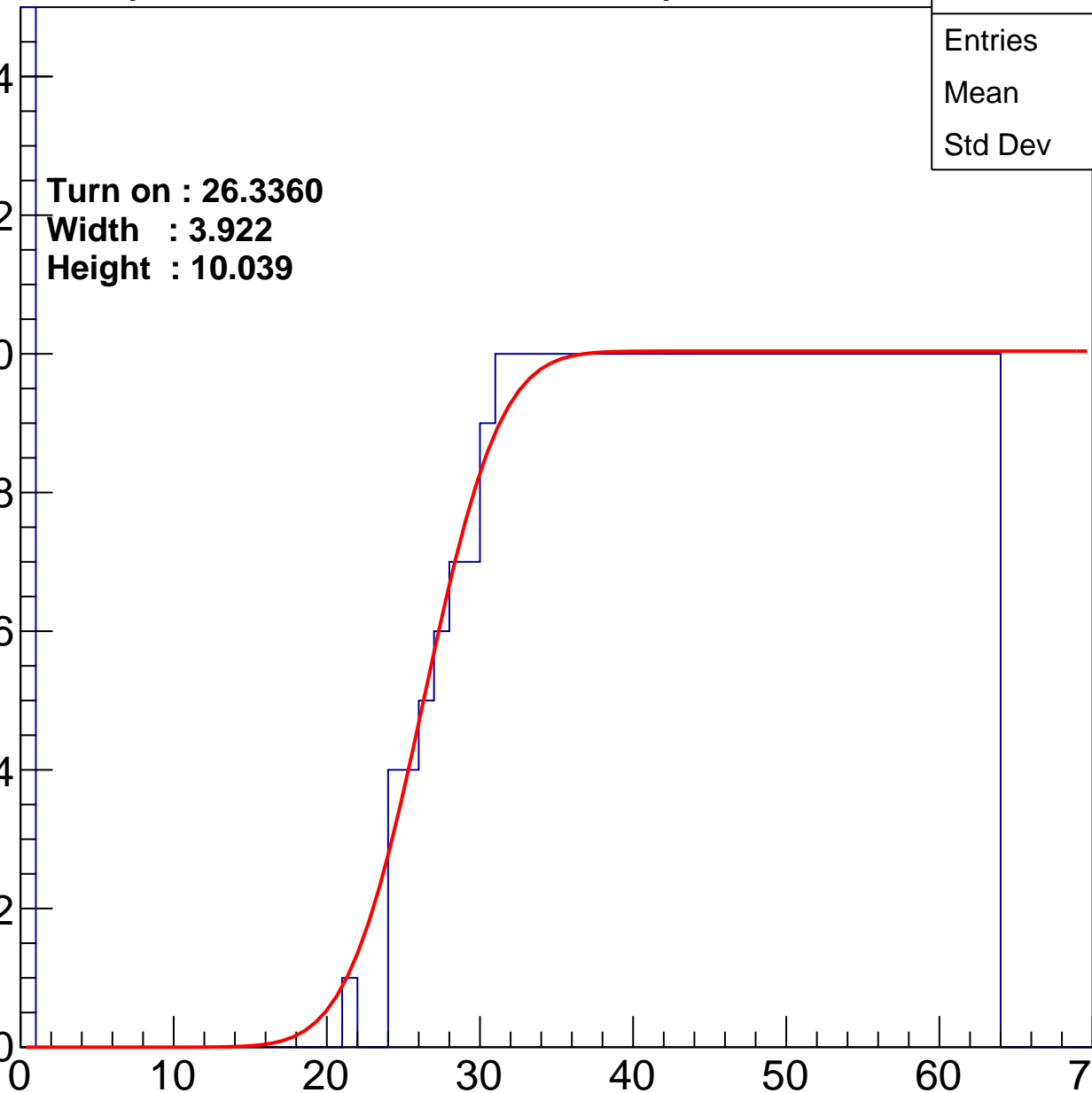
Width : 3.922

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch64

calib_packv5_041523_1651.root, FC#0, port C2

Entries	450
Mean	38.08
Std Dev	18.27

Turn on : 25.9125

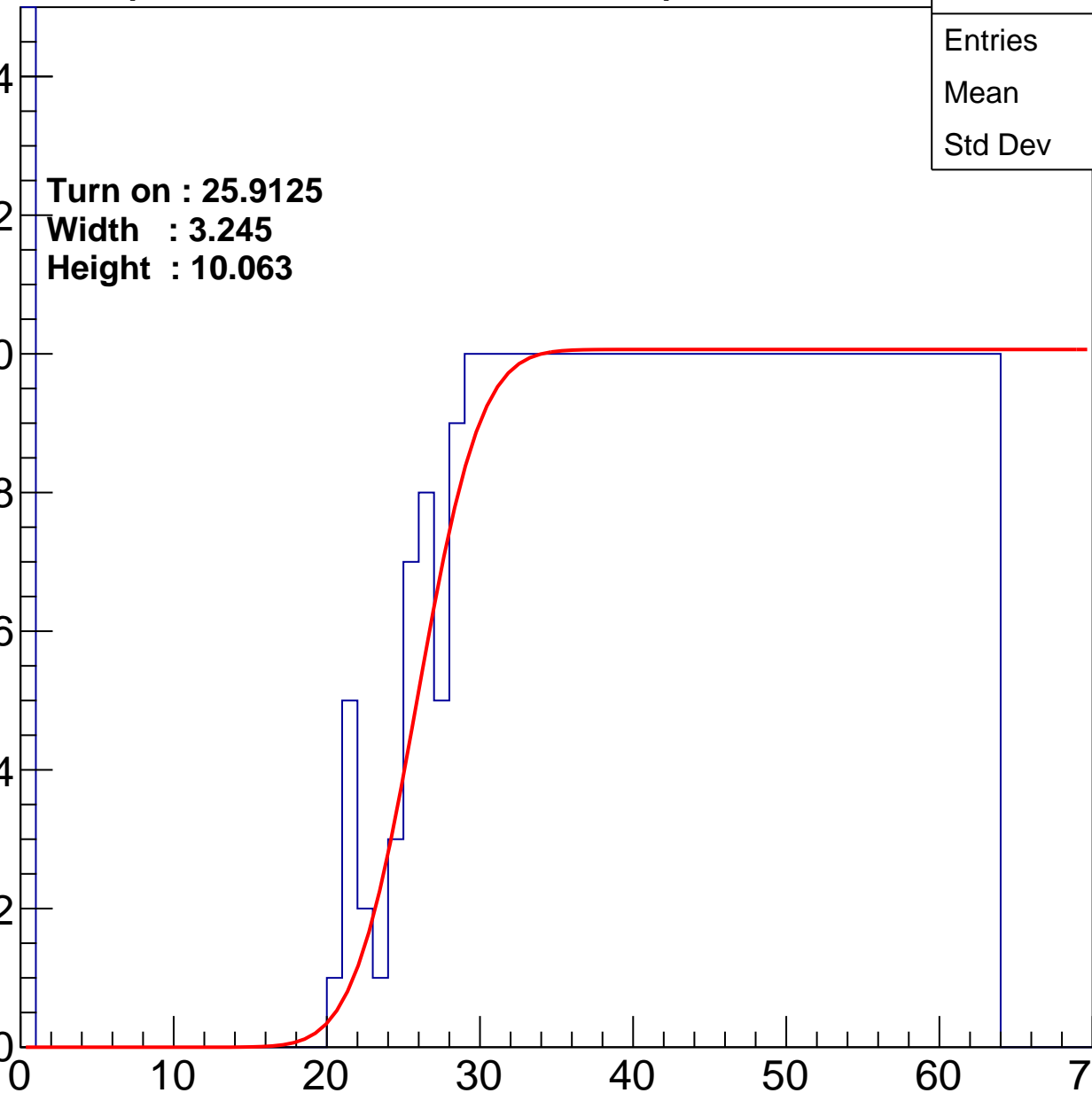
Width : 3.245

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch65

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	39.66
Std Dev	17.25

Turn on : 25.6076

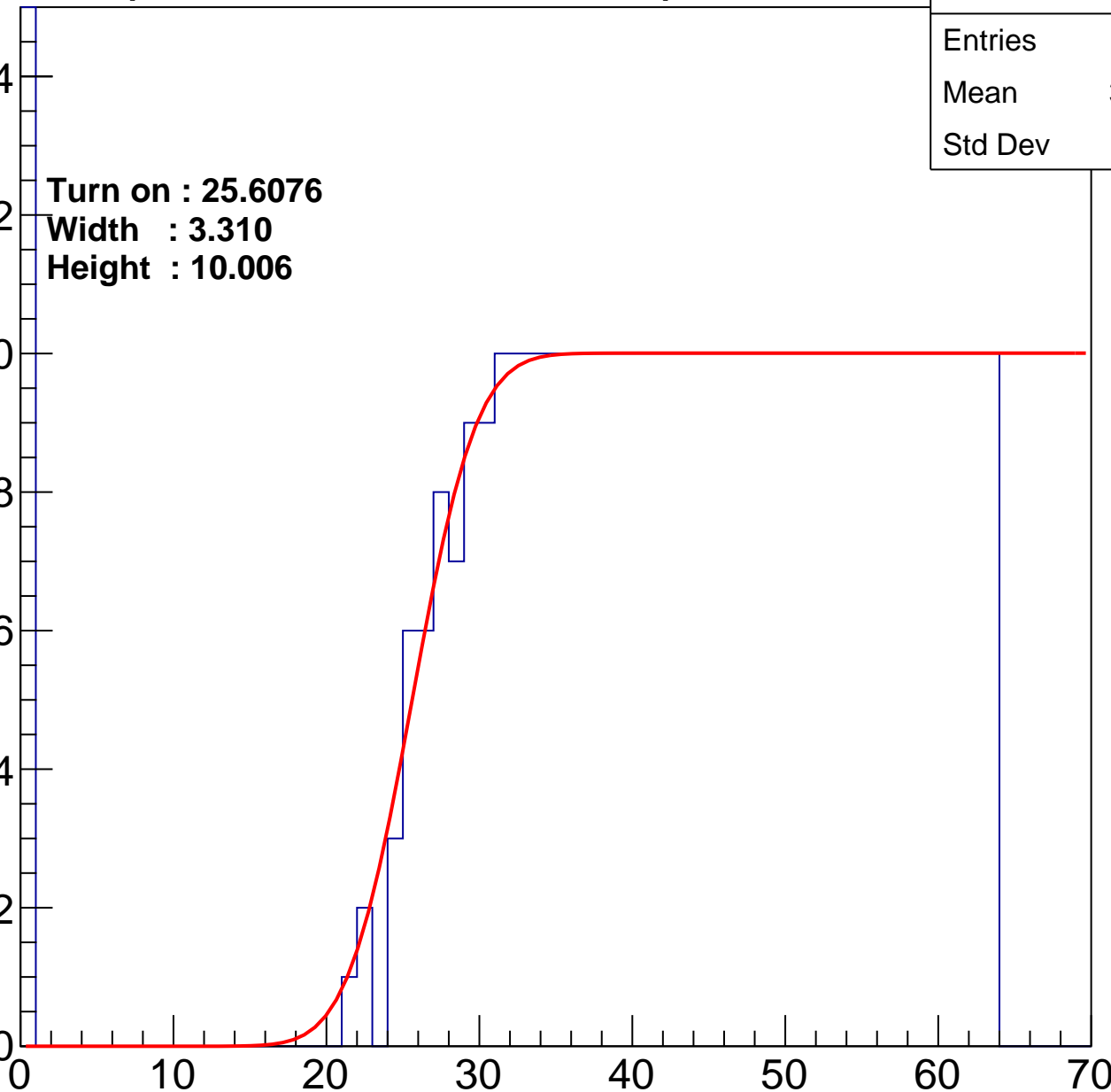
Width : 3.310

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch66

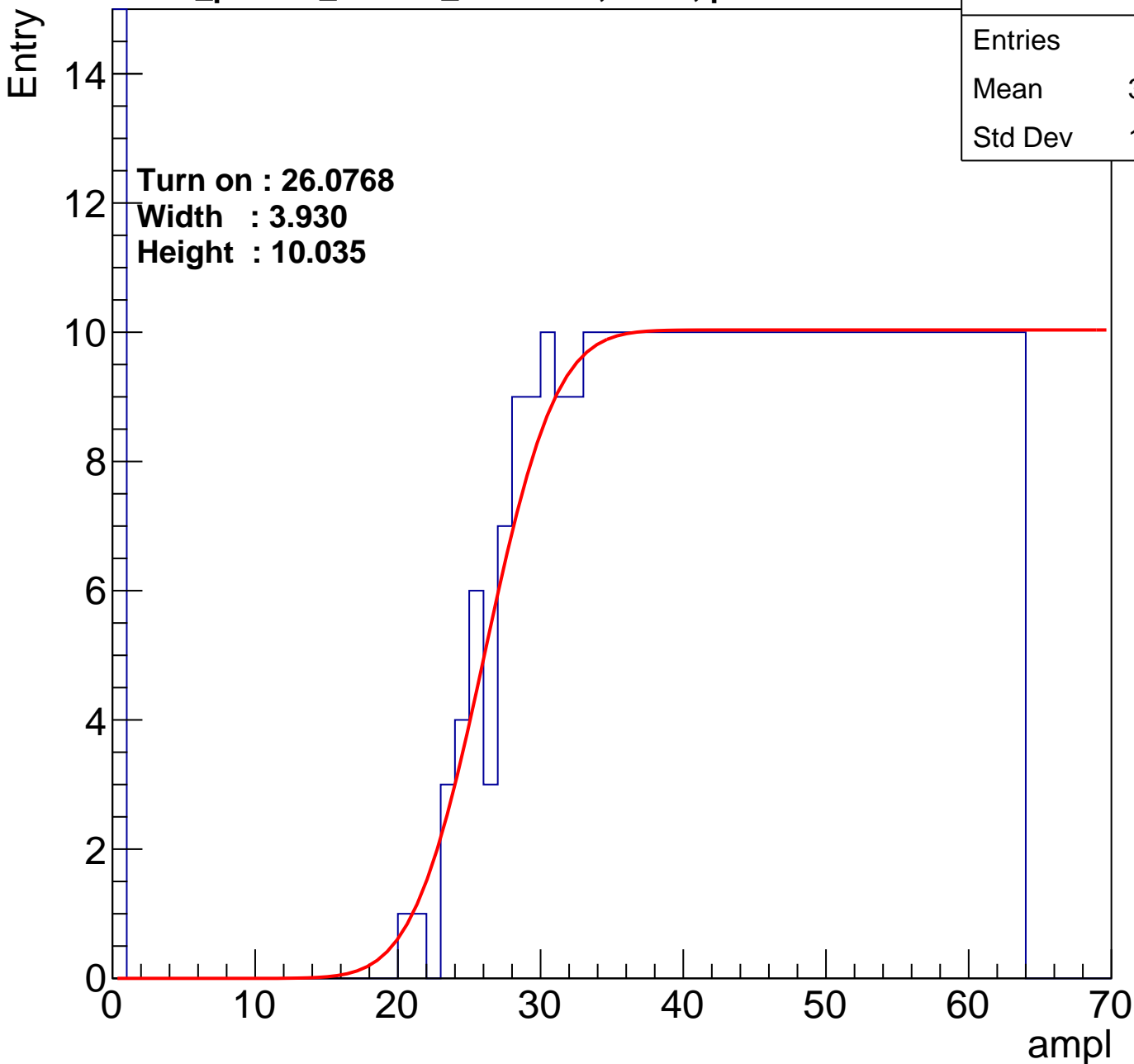
calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.45
Std Dev	17.44

Turn on : 26.0768

Width : 3.930

Height : 10.035



B1L103S, U8-ch67

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	39.08
Std Dev	17.63

Turn on : 25.9128

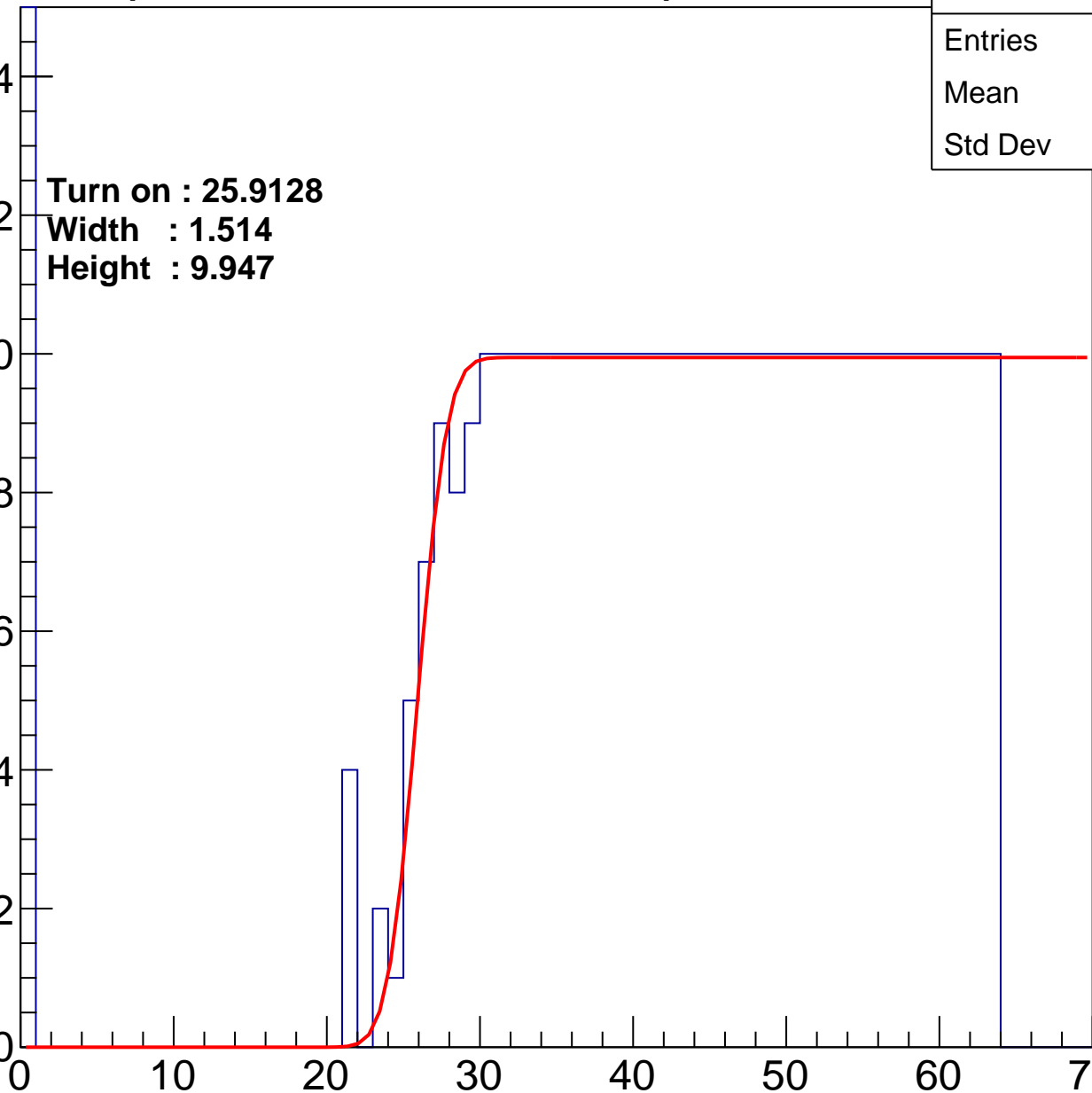
Width : 1.514

Height : 9.947

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch68

calib_packv5_041523_1651.root, FC#0, port C2

Entries	413
Mean	40.53
Std Dev	16.64

Turn on : 26.7487

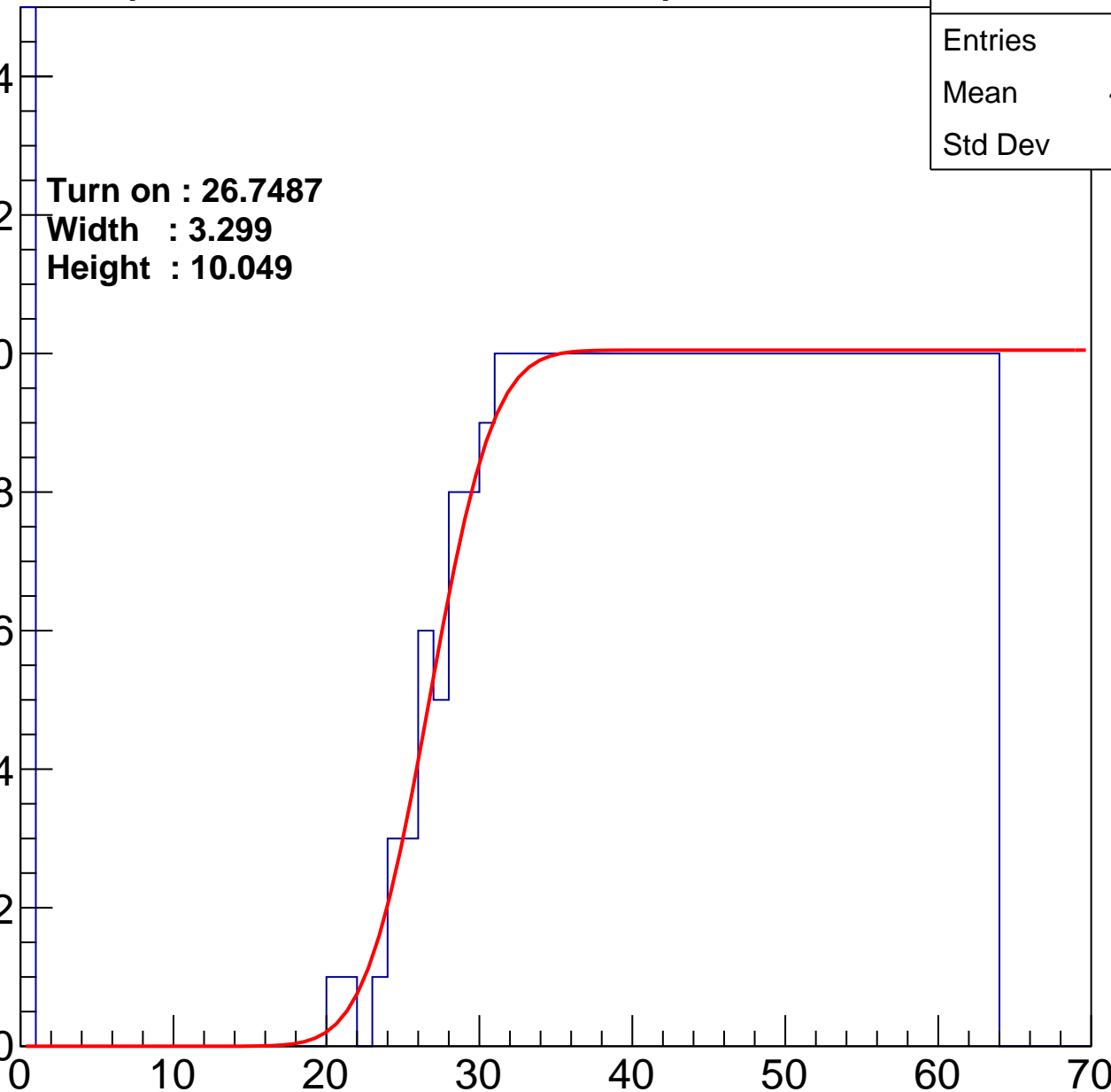
Width : 3.299

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch69

calib_packv5_041523_1651.root, FC#0, port C2

Entries	425
Mean	39.51
Std Dev	17.54

Turn on : 26.8126

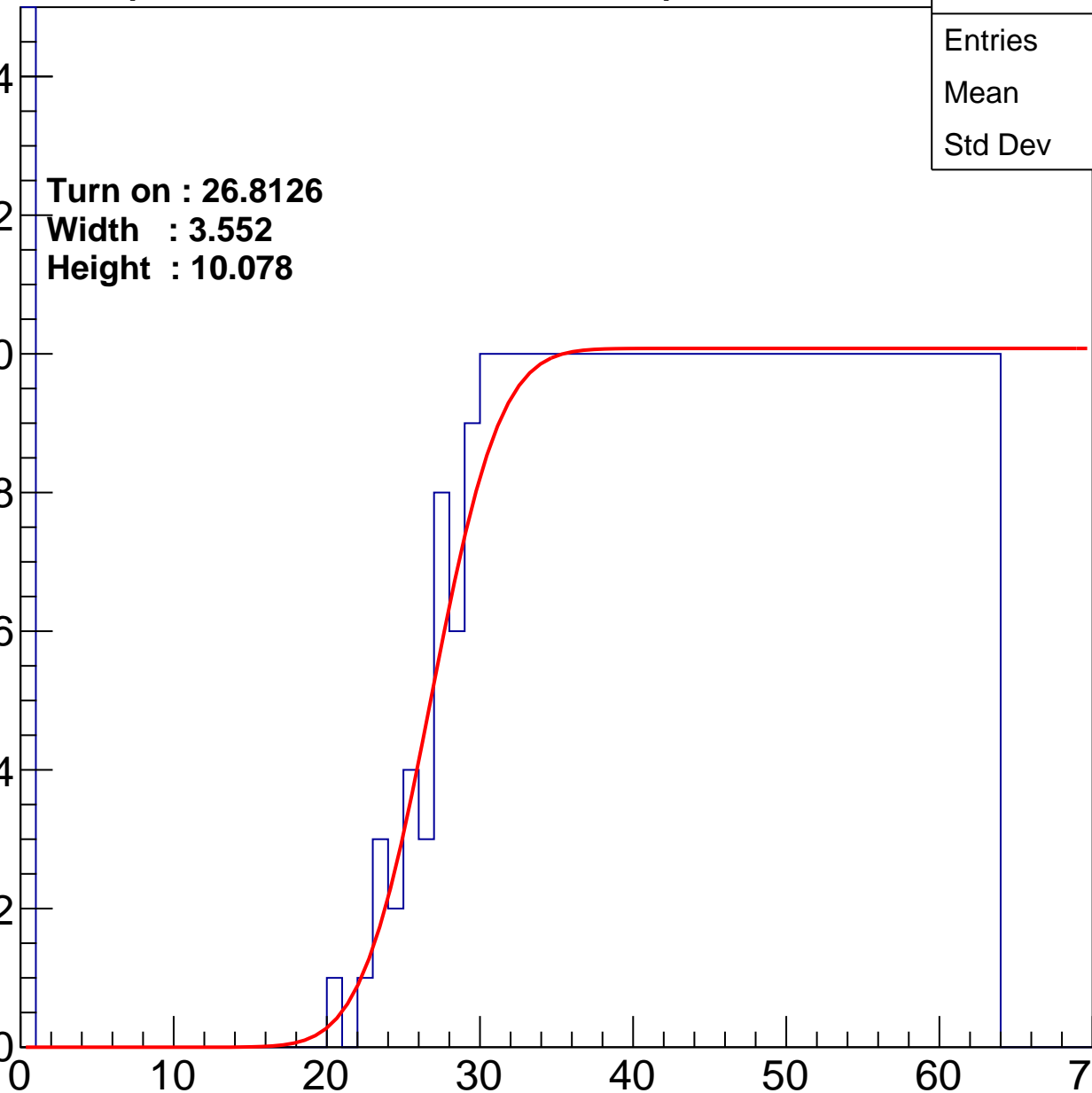
Width : 3.552

Height : 10.078

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch70

calib_packv5_041523_1651.root, FC#0, port C2

Entries	425
Mean	40.29
Std Dev	16.29

Turn on : 25.1251

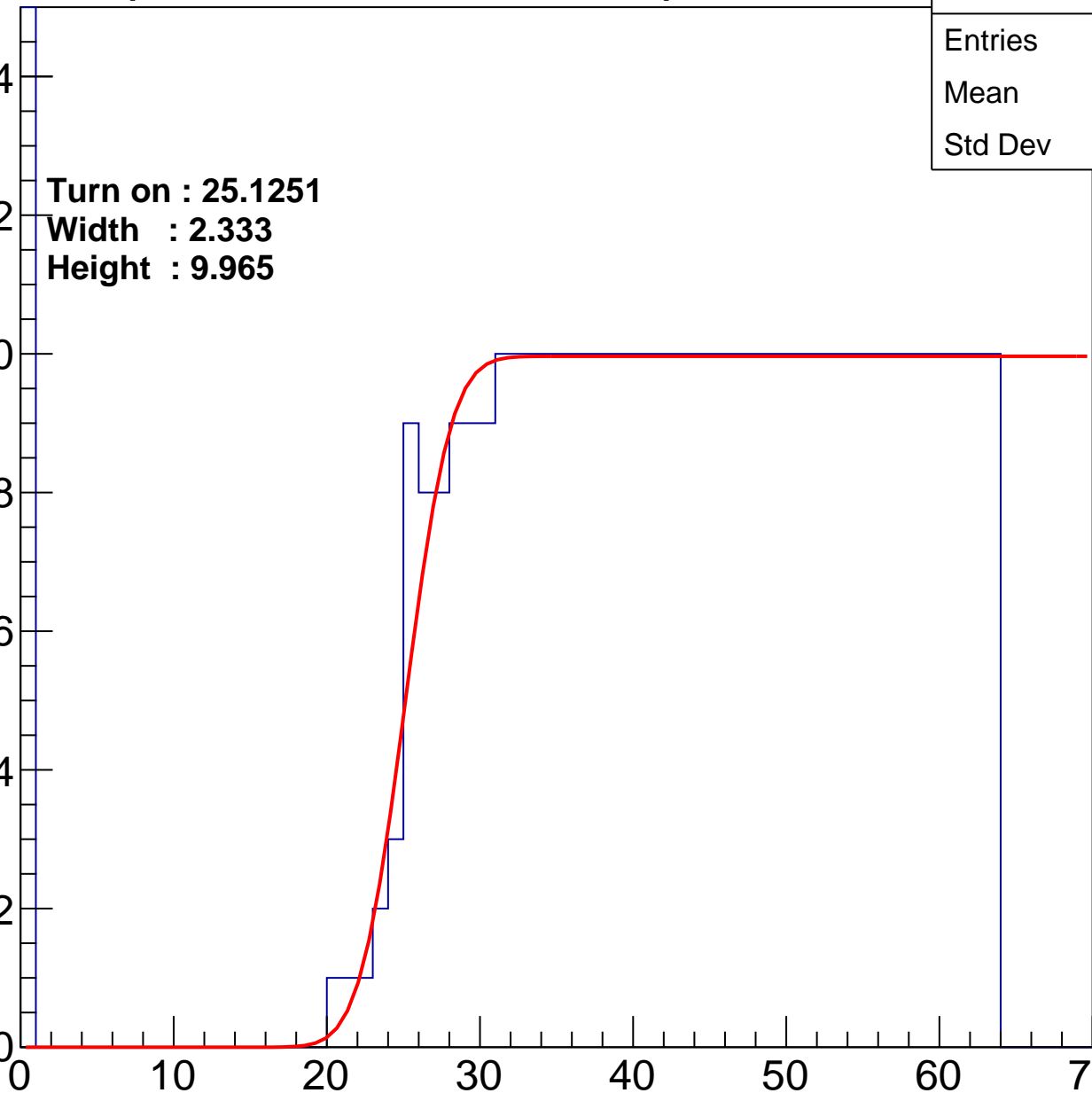
Width : 2.333

Height : 9.965

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch71

calib_packv5_041523_1651.root, FC#0, port C2

Entries	422
Mean	39.66
Std Dev	17.52

Turn on : 26.7261

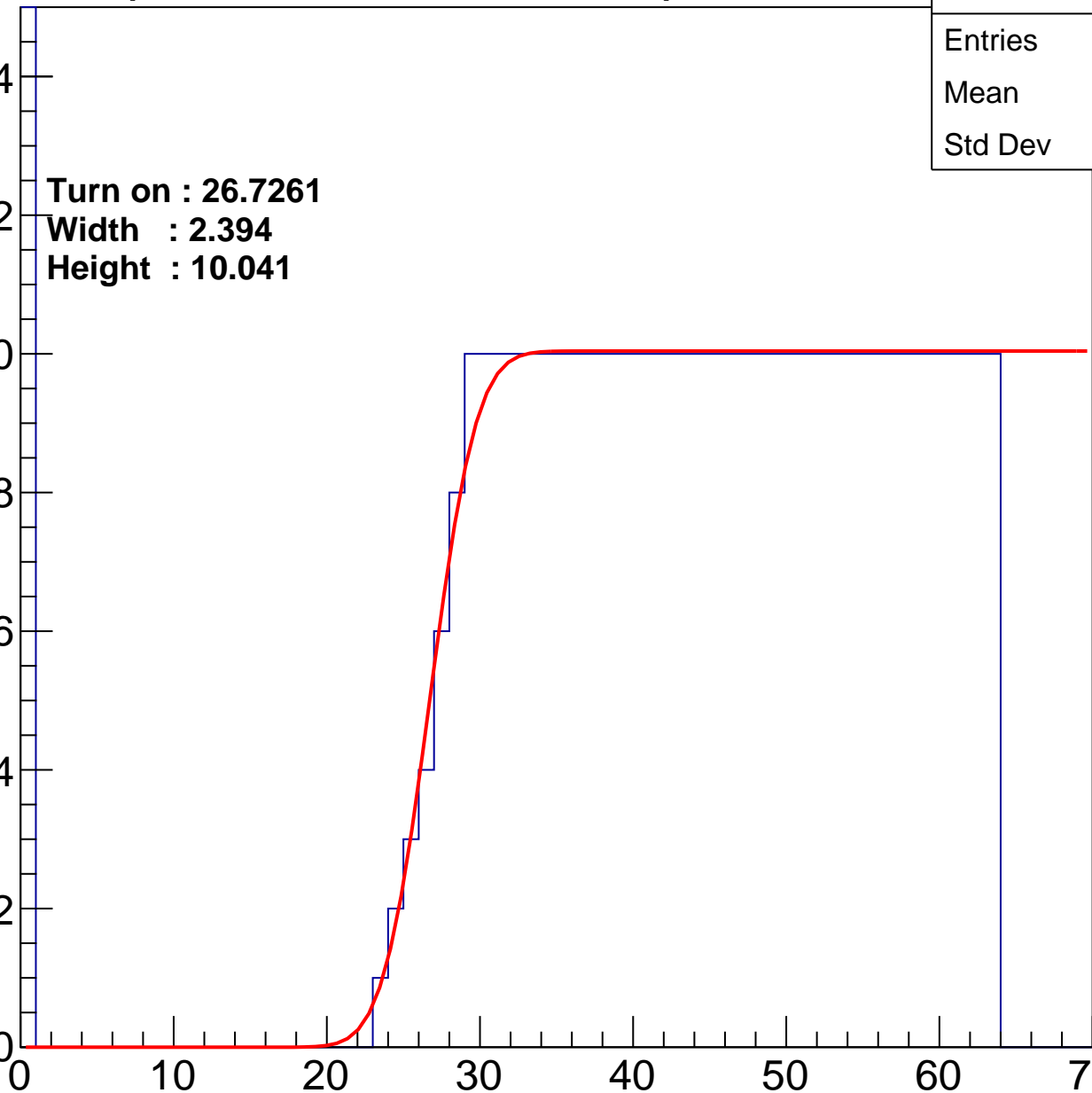
Width : 2.394

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch72

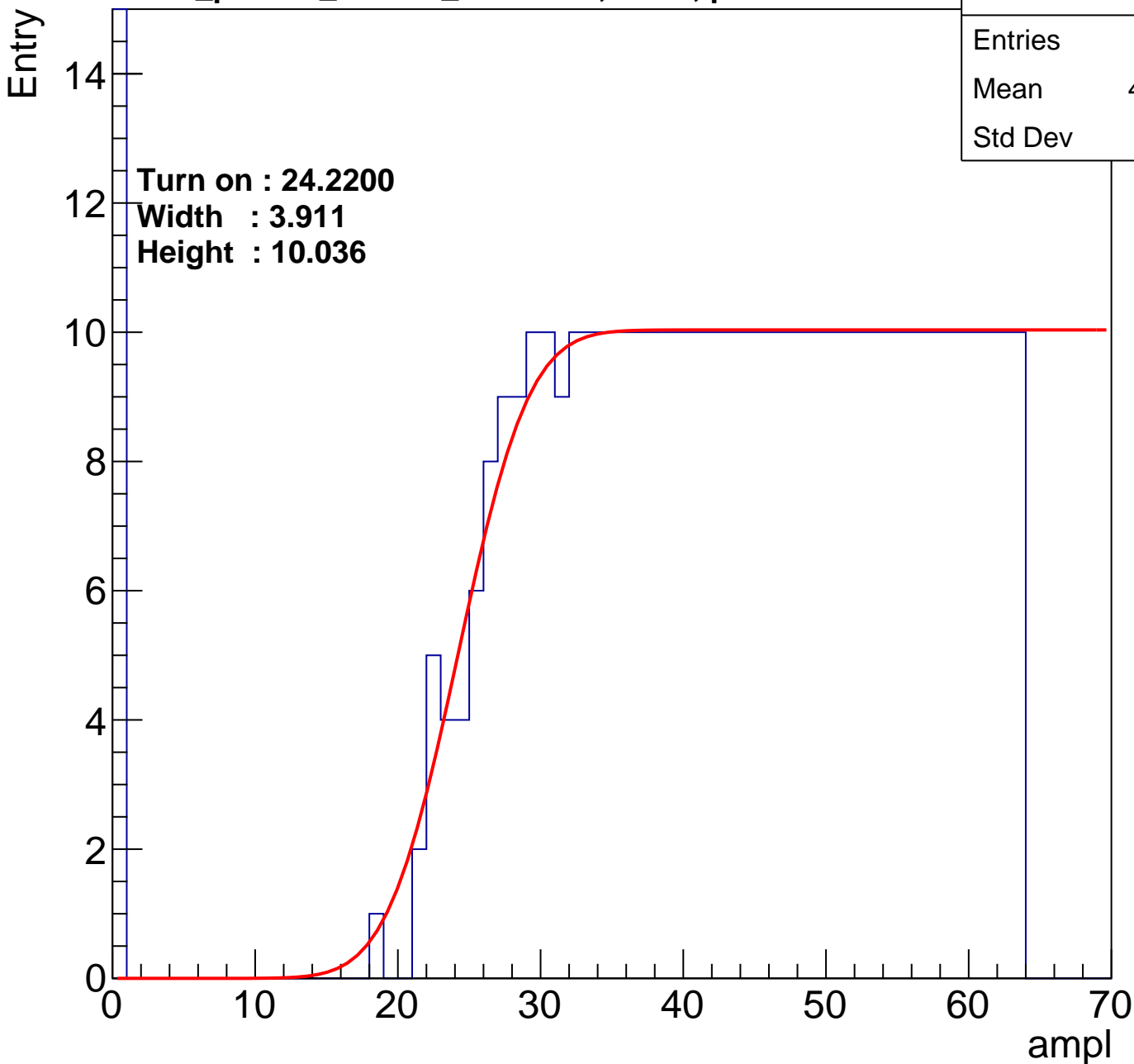
calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	40.85
Std Dev	15.4

Turn on : 24.2200

Width : 3.911

Height : 10.036



B1L103S, U8-ch73

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	39.99
Std Dev	17.31

Turn on : 27.1024

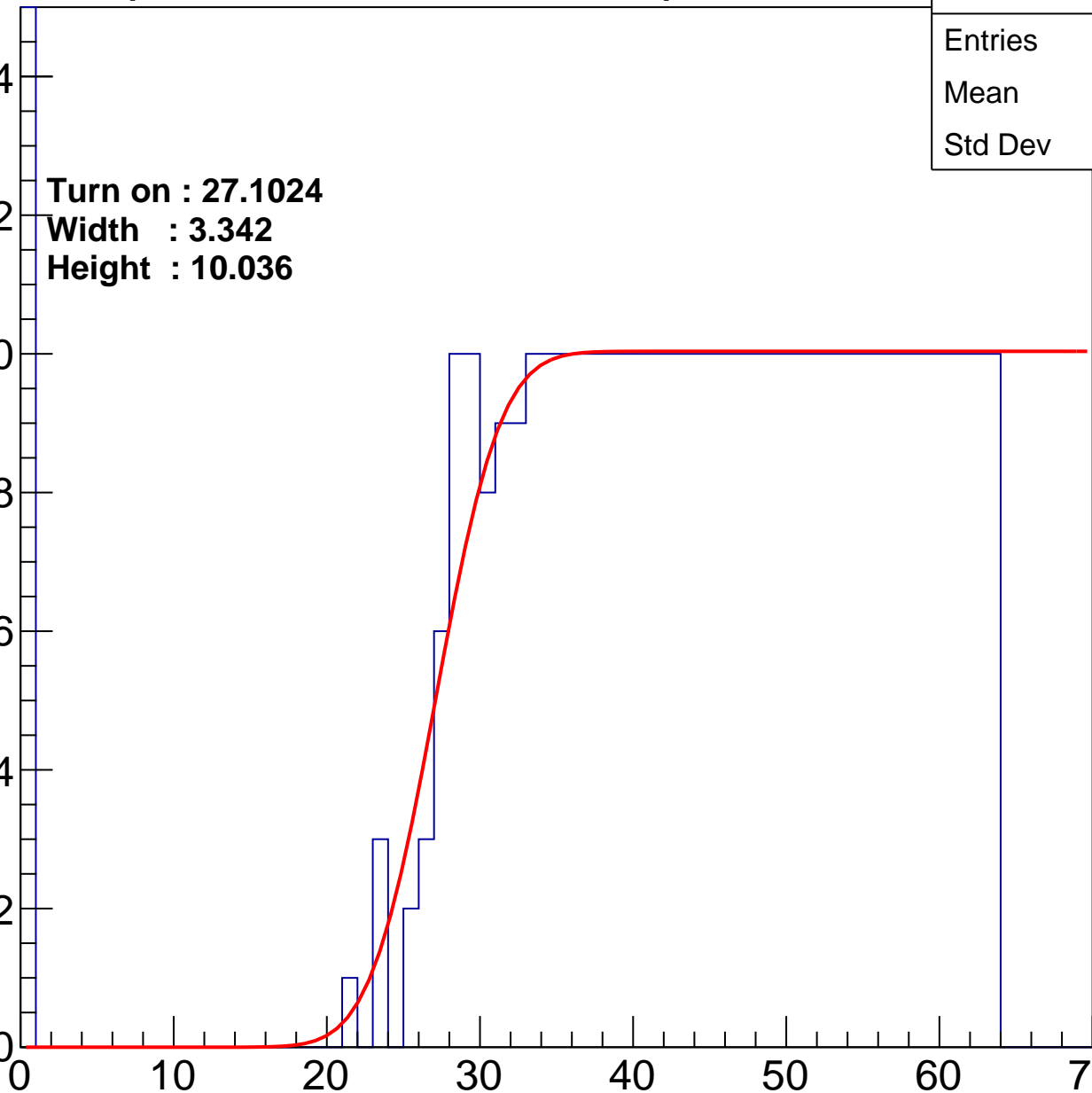
Width : 3.342

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch74

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	40.53
Std Dev	16.2

Turn on : 25.4508

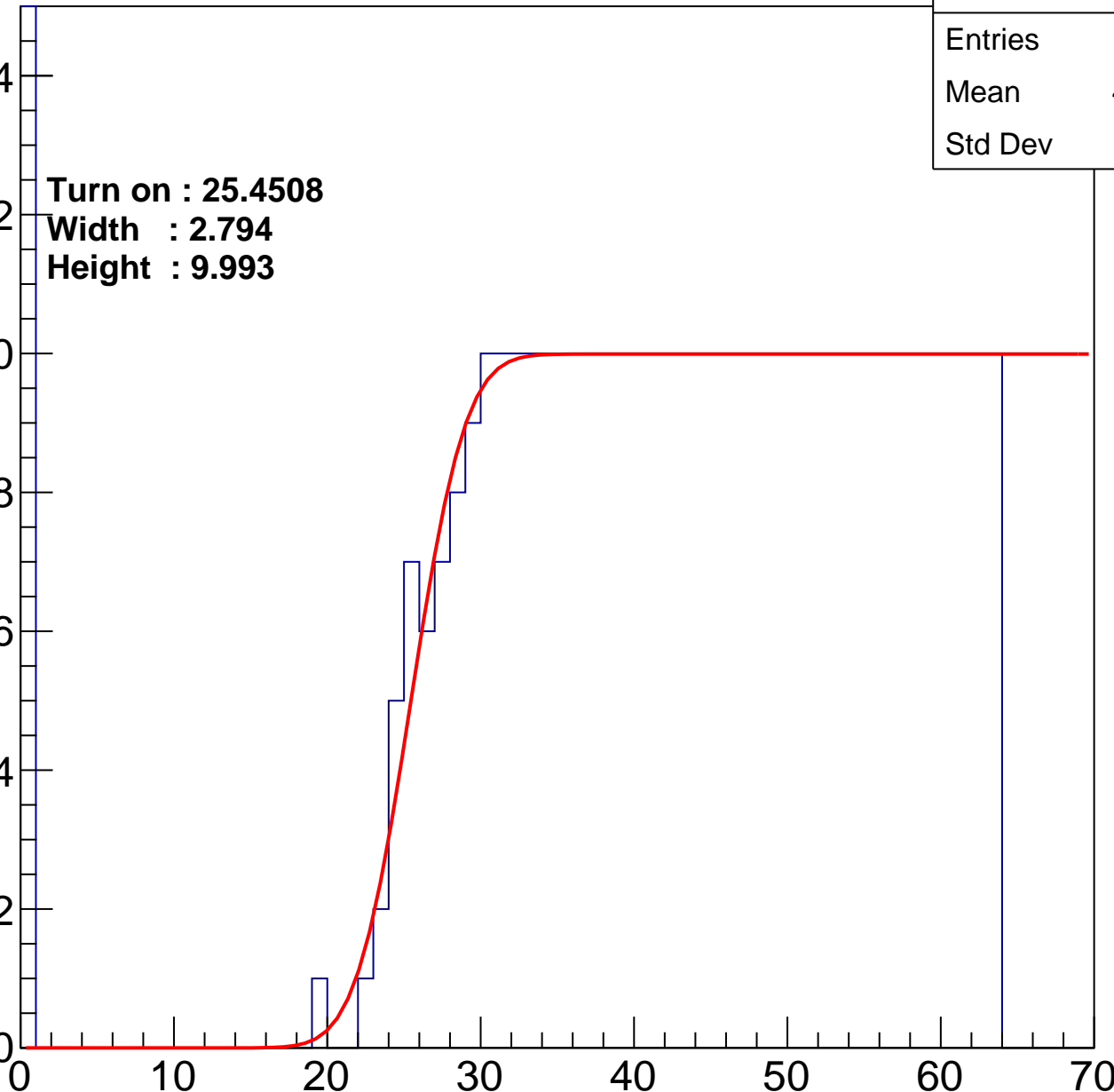
Width : 2.794

Height : 9.993

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch75

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	38.94
Std Dev	18

Turn on : 26.2373

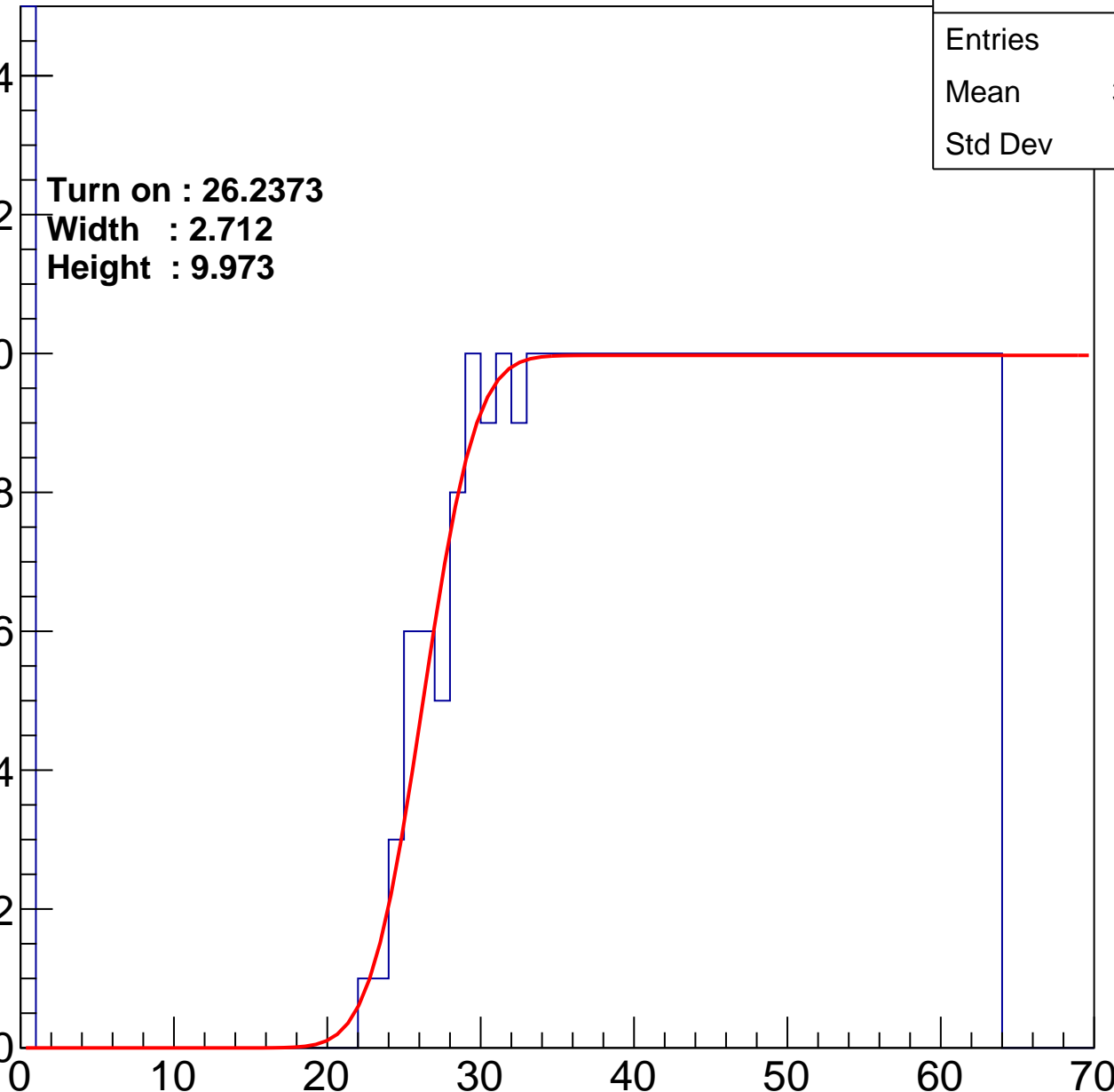
Width : 2.712

Height : 9.973

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch76

calib_packv5_041523_1651.root, FC#0, port C2

Entries	452
Mean	38.33
Std Dev	17.83

Turn on : 24.5035

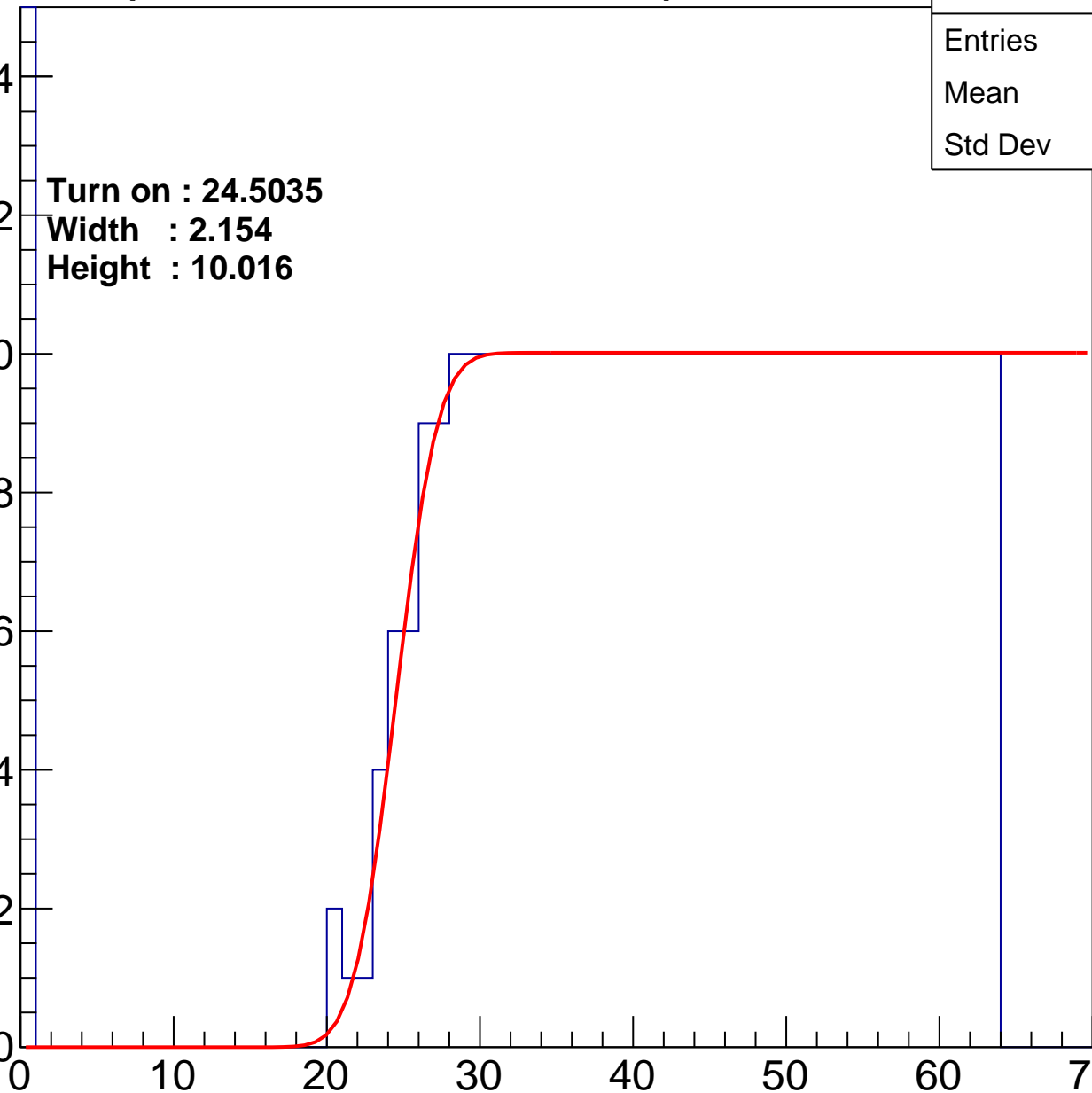
Width : 2.154

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch77

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	40.43
Std Dev	16.5

Turn on : 26.1213

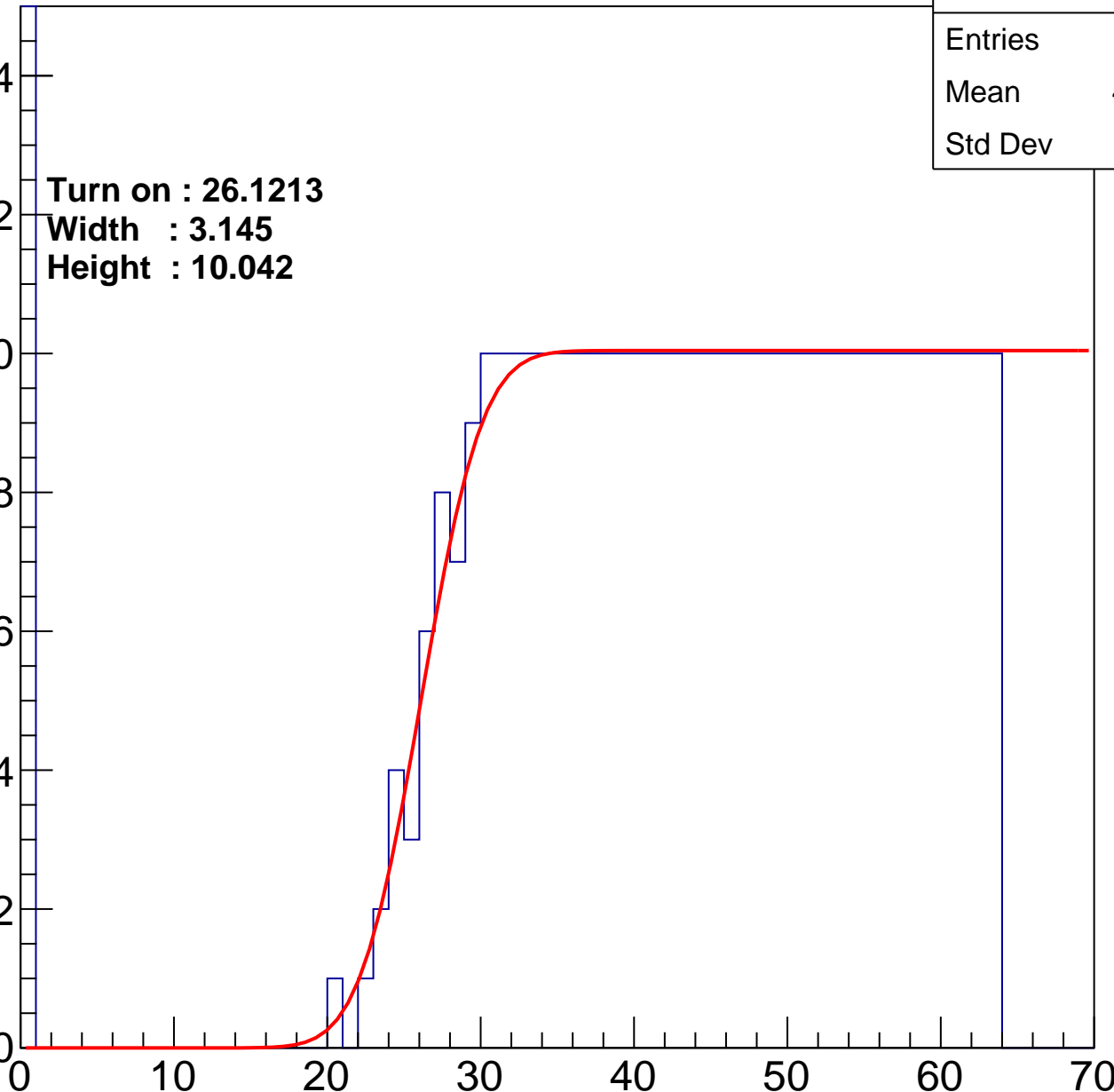
Width : 3.145

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch78

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	38.62
Std Dev	18.1

Turn on : 25.7488

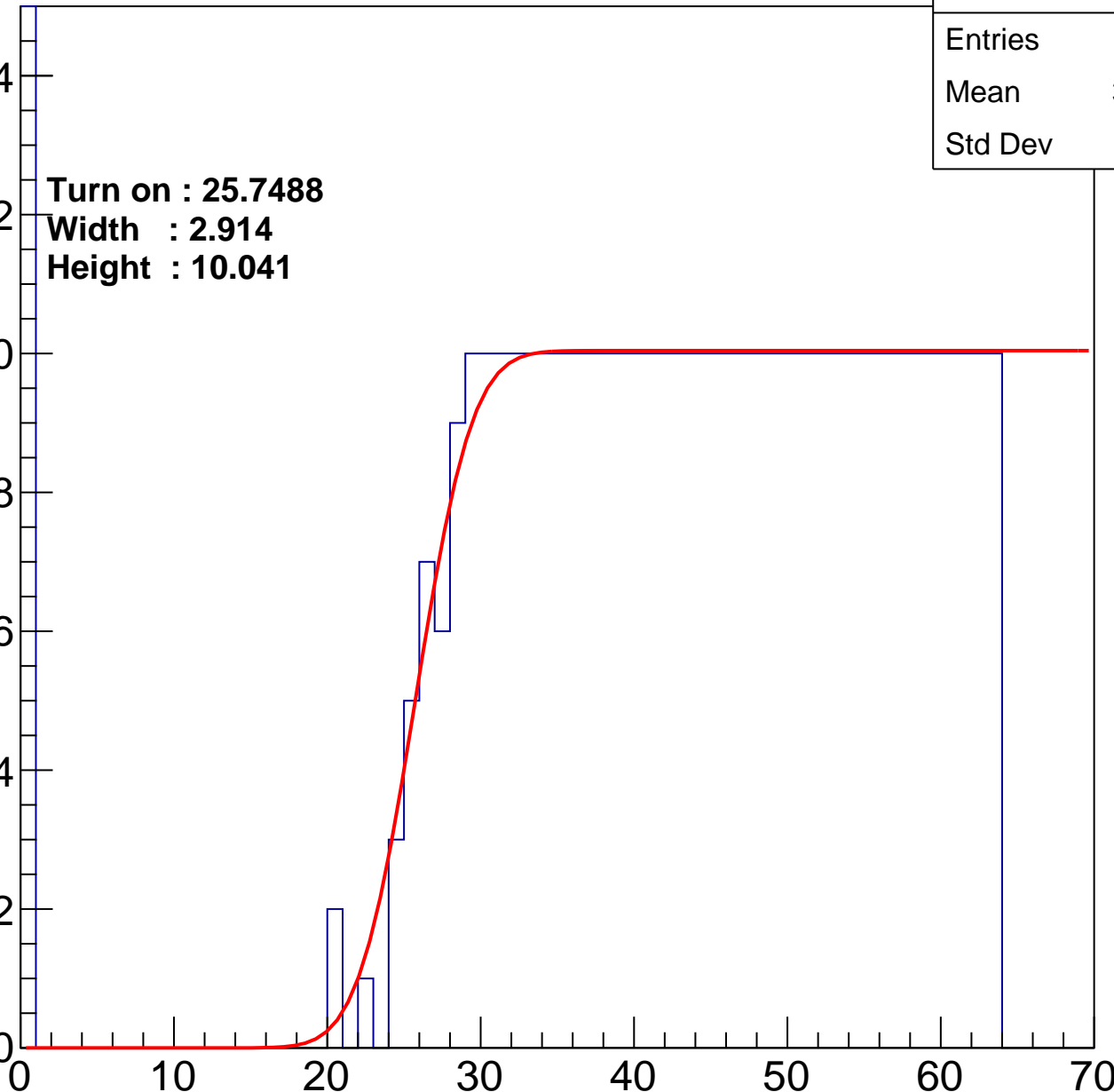
Width : 2.914

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch79

calib_packv5_041523_1651.root, FC#0, port C2

Entries	411
Mean	40.67
Std Dev	16.53

Turn on : 26.7172

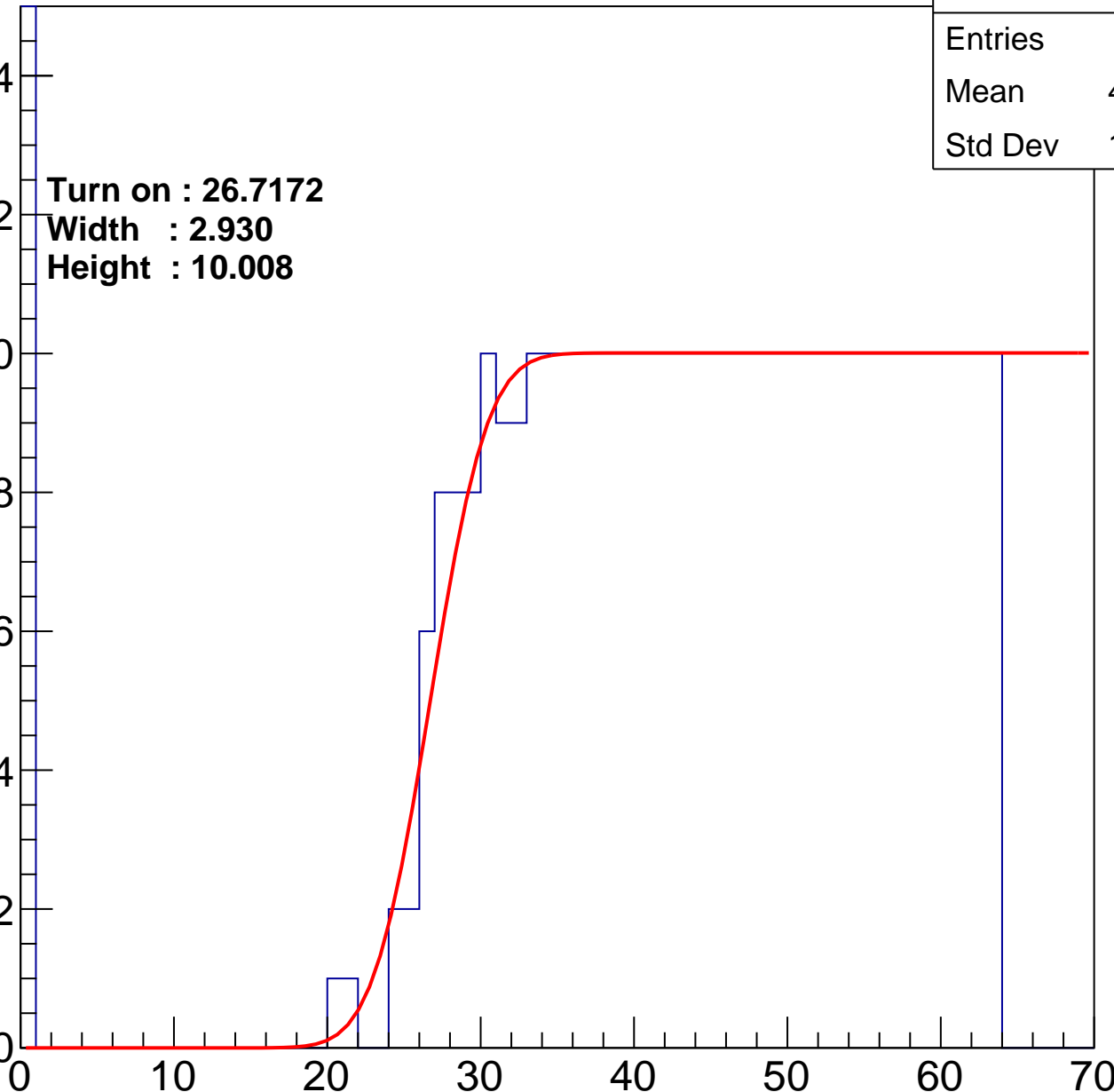
Width : 2.930

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch80

calib_packv5_041523_1651.root, FC#0, port C2

Entries	415
Mean	40.09
Std Dev	17.22

Turn on : 26.8250

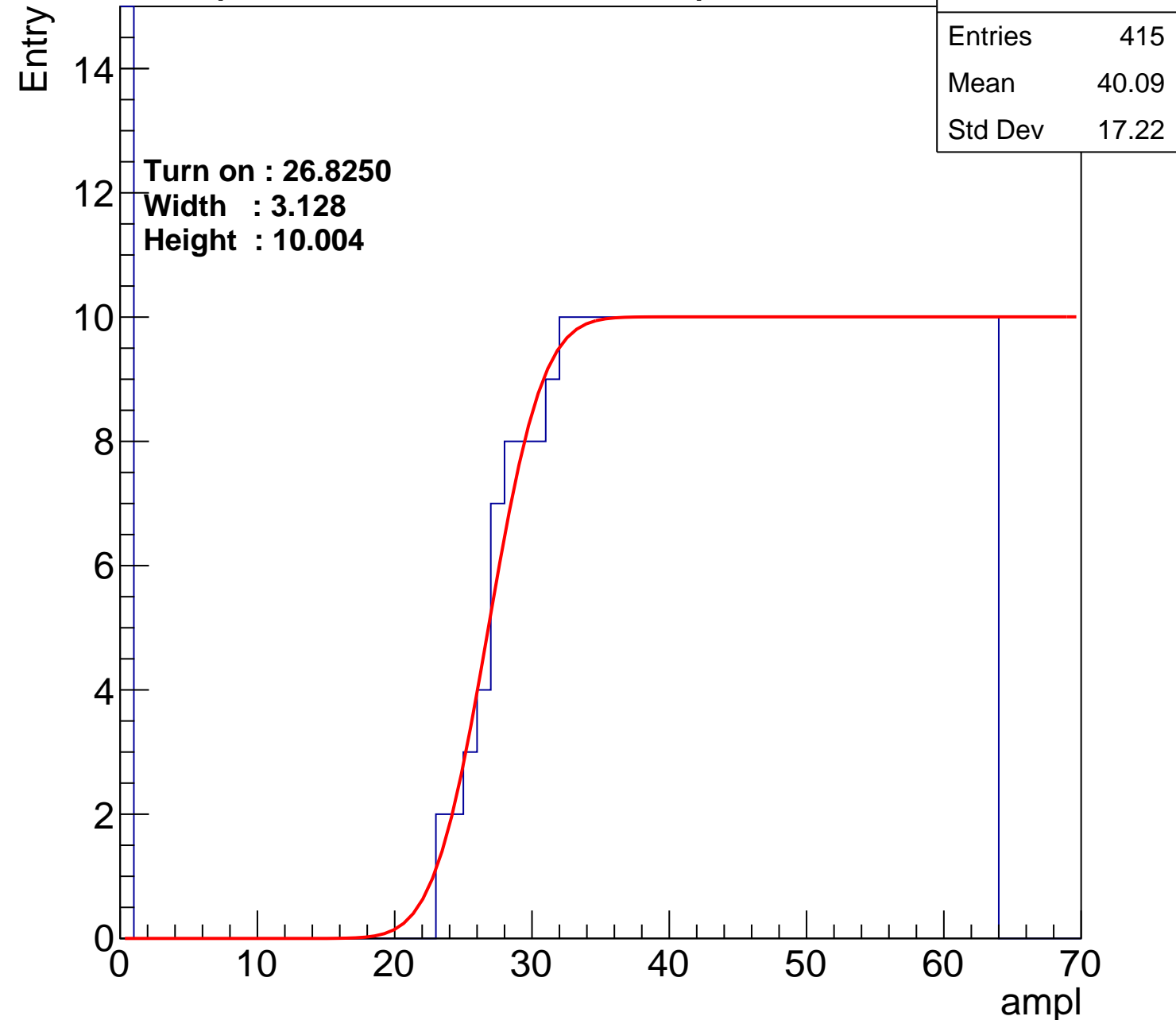
Width : 3.128

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch81

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	39.24
Std Dev	17.63

Turn on : 25.8508

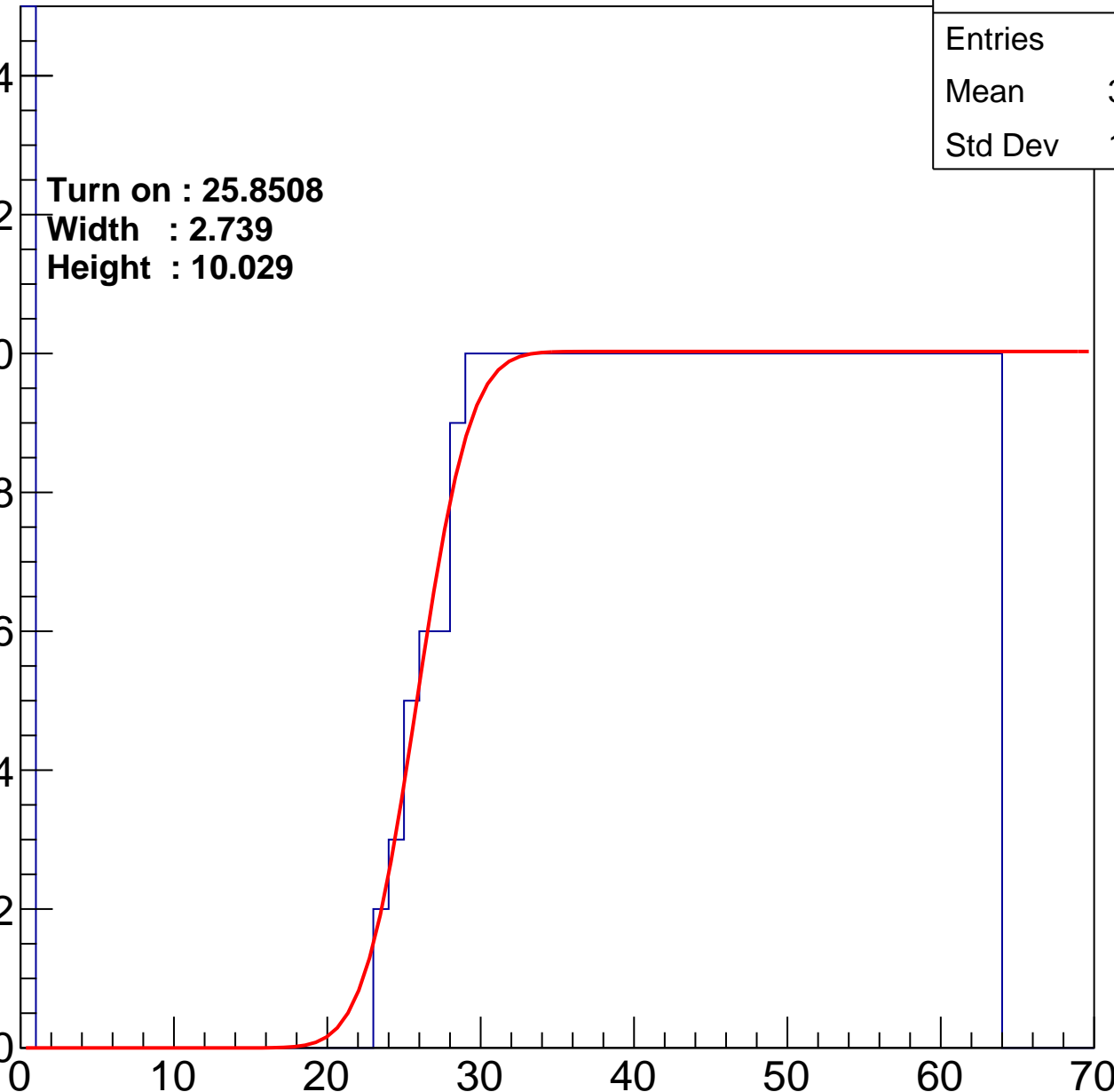
Width : 2.739

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch82

calib_packv5_041523_1651.root, FC#0, port C2

Entries	501
Mean	34.19
Std Dev	20.66

Turn on : 25.7866

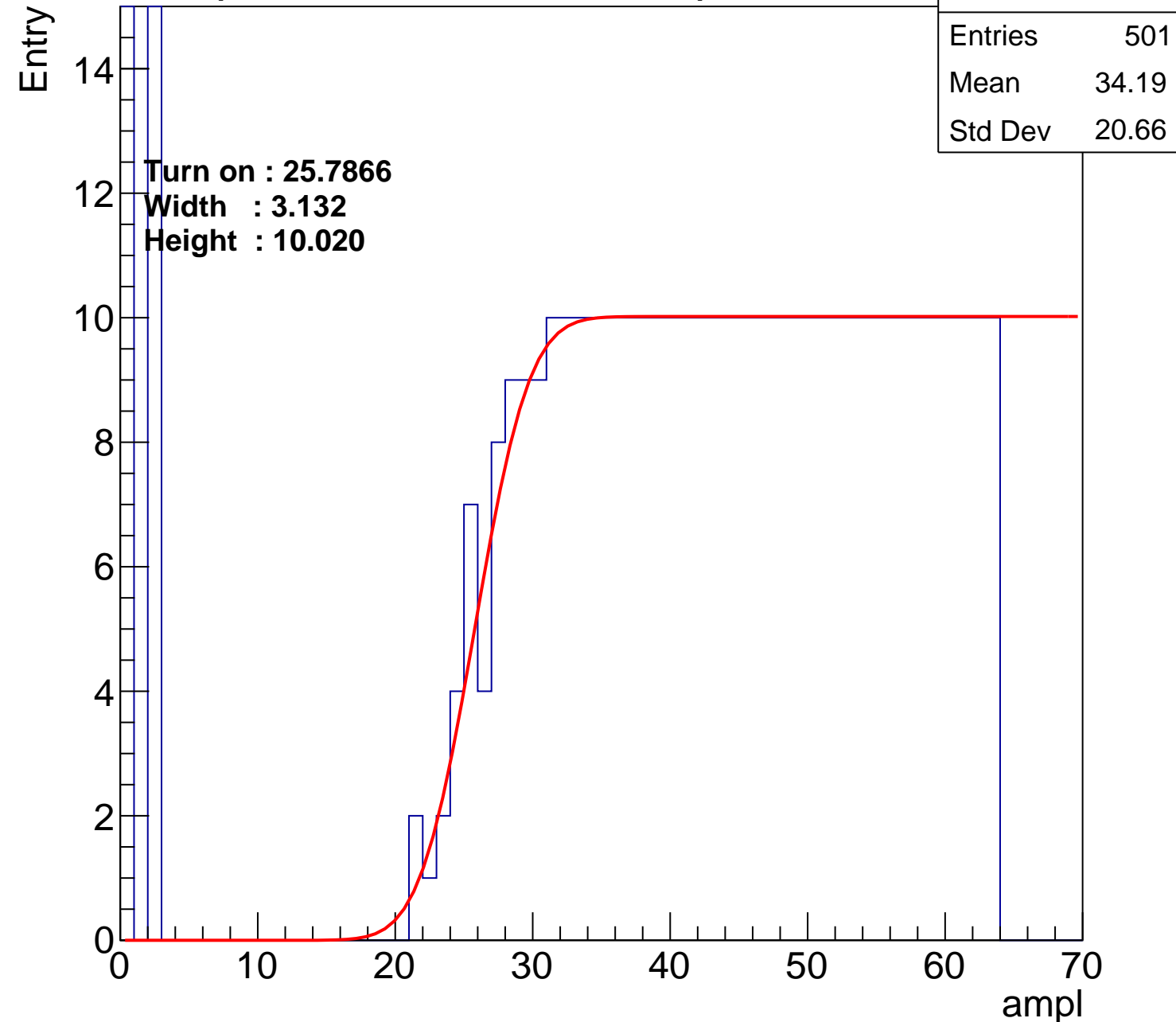
Width : 3.132

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch83

calib_packv5_041523_1651.root, FC#0, port C2

Entries	404
Mean	41.1
Std Dev	16.24

Turn on : 27.6050

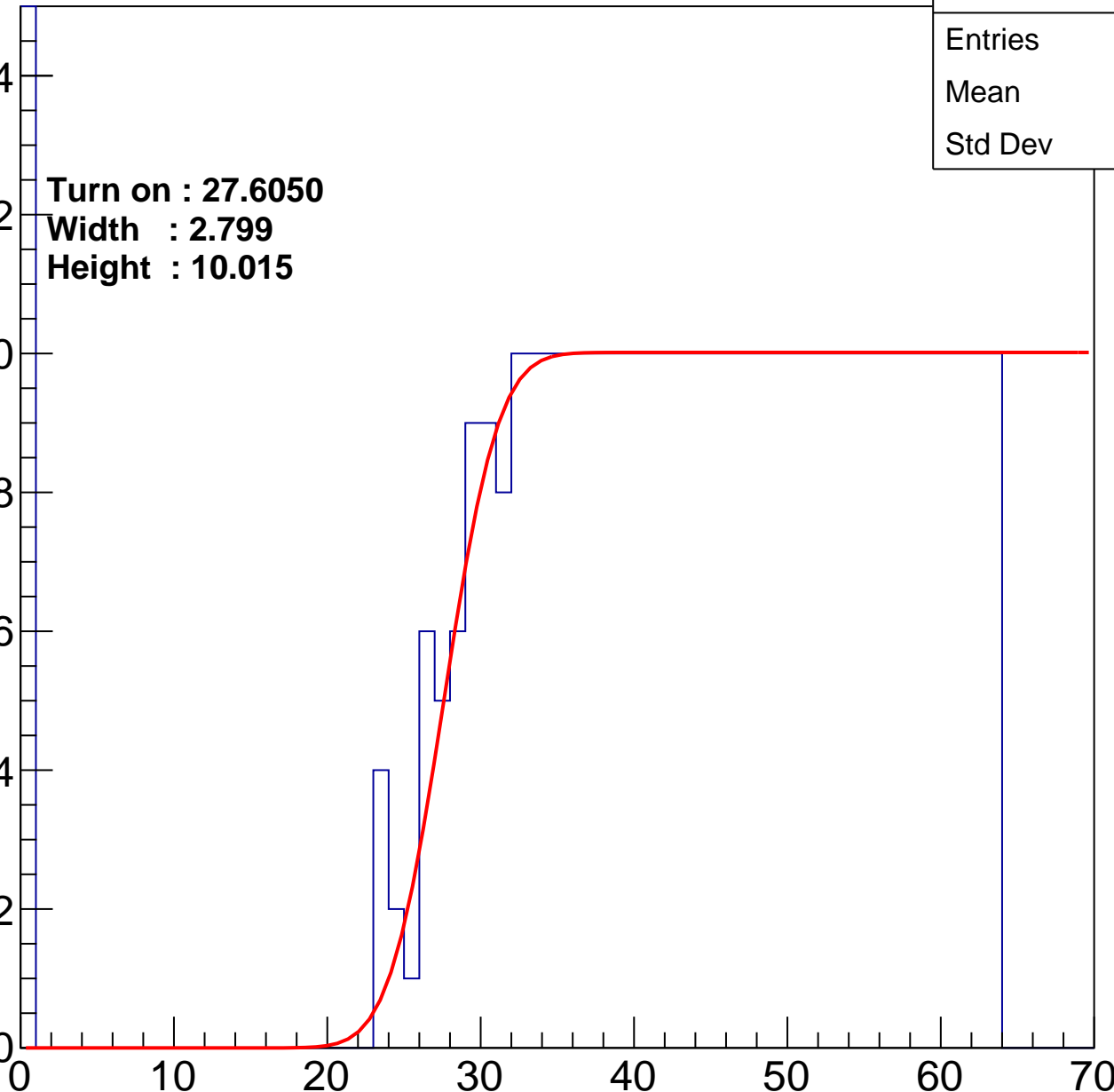
Width : 2.799

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch84

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	39
Std Dev	17.45

Turn on : 25.0517

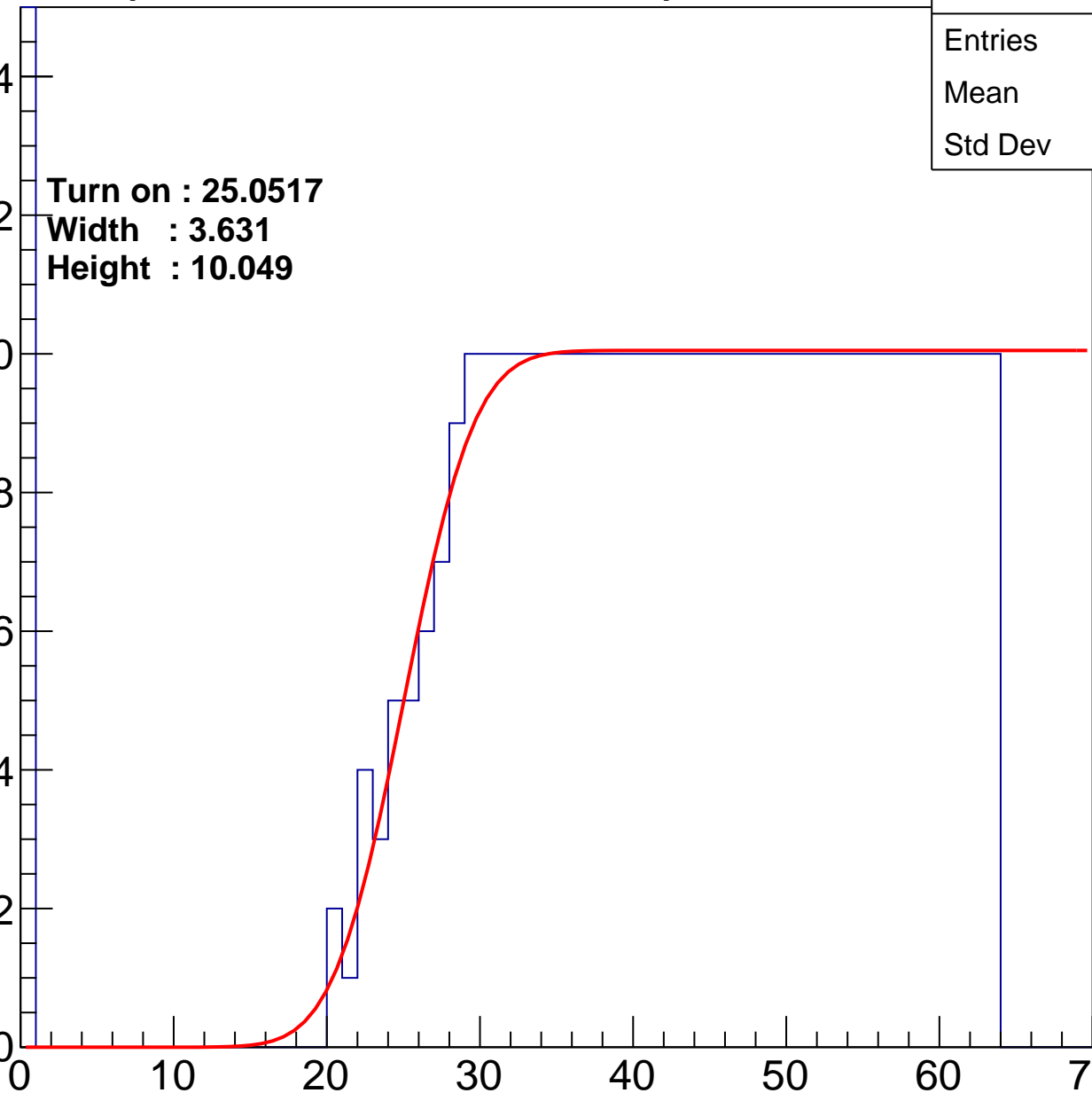
Width : 3.631

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch85

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	39.01
Std Dev	17.8

Turn on : 26.0884

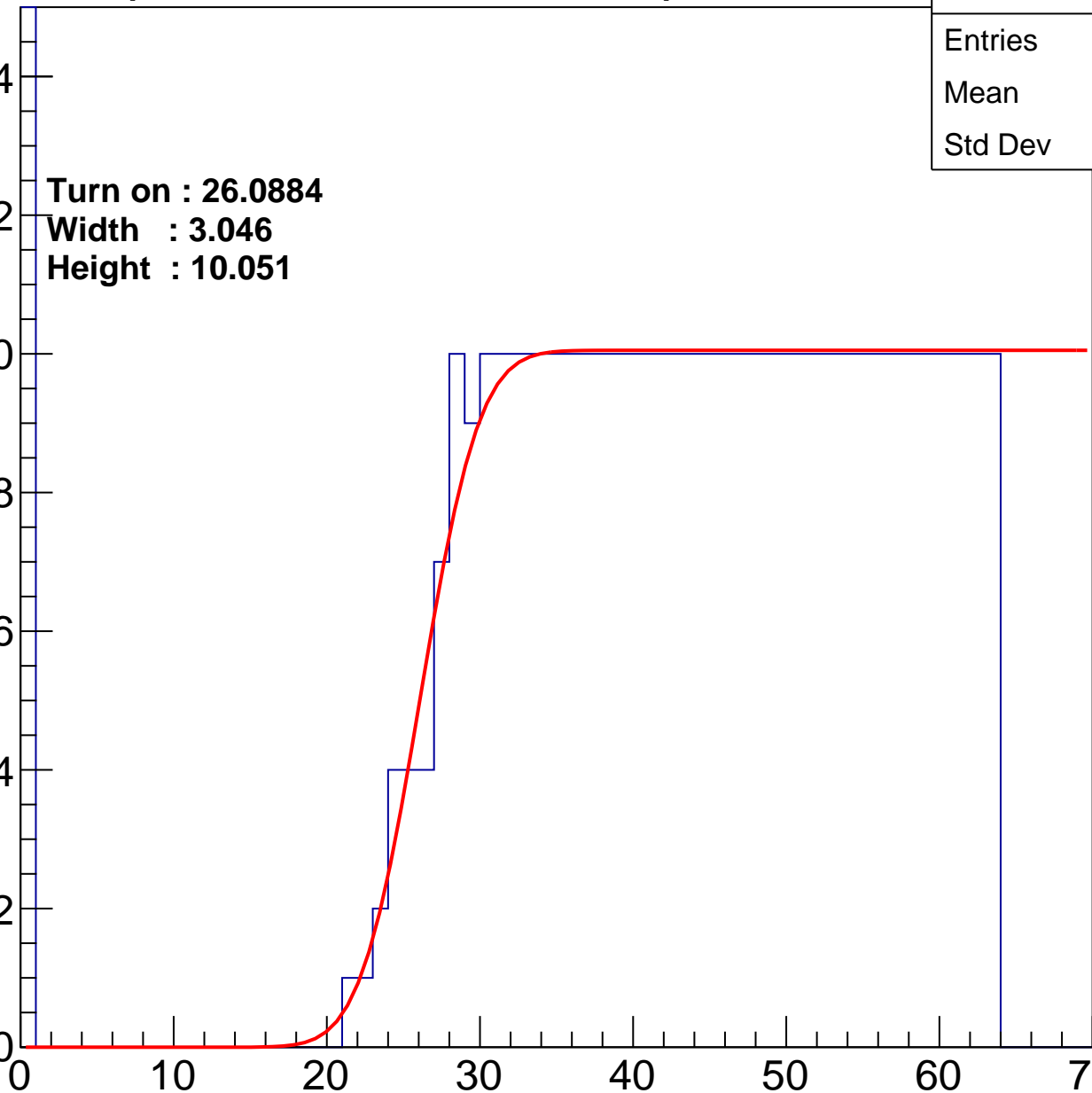
Width : 3.046

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch86

calib_packv5_041523_1651.root, FC#0, port C2

Entries	450
Mean	38.8
Std Dev	17.22

Turn on : 23.6615

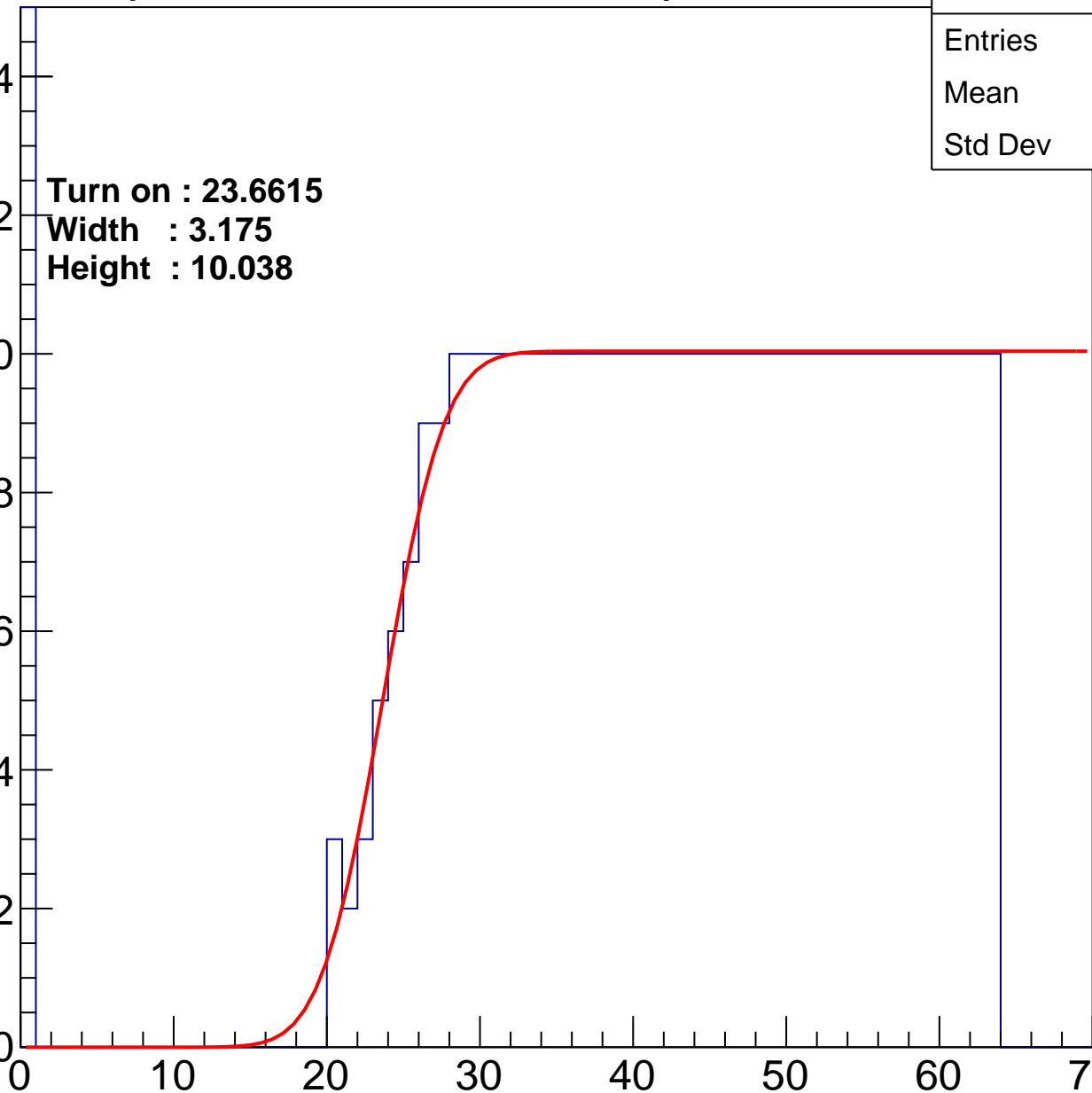
Width : 3.175

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch87

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	40.33
Std Dev	16.59

Turn on : 25.9013

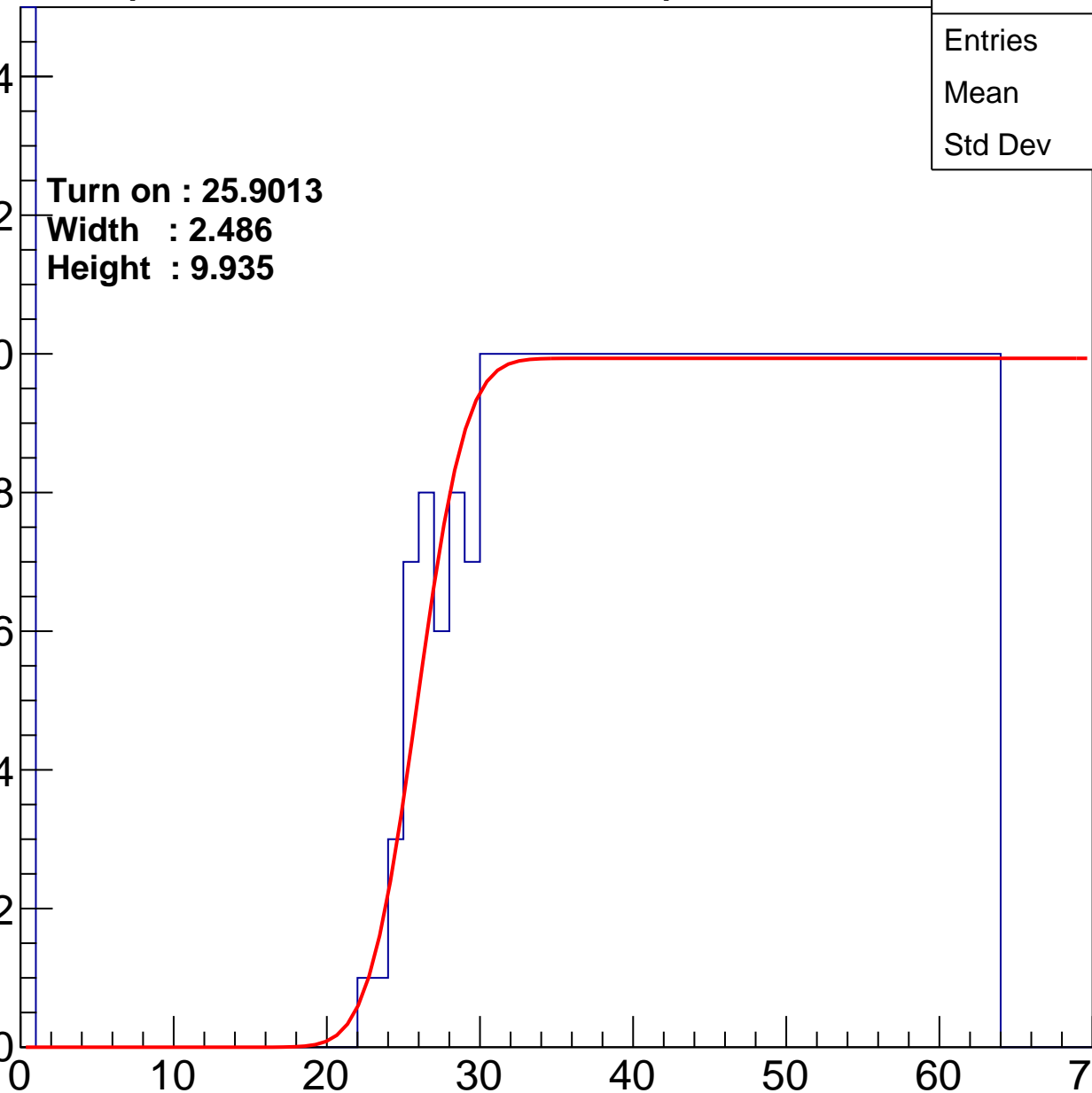
Width : 2.486

Height : 9.935

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch88

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	38.94
Std Dev	17.44

Turn on : 24.4318

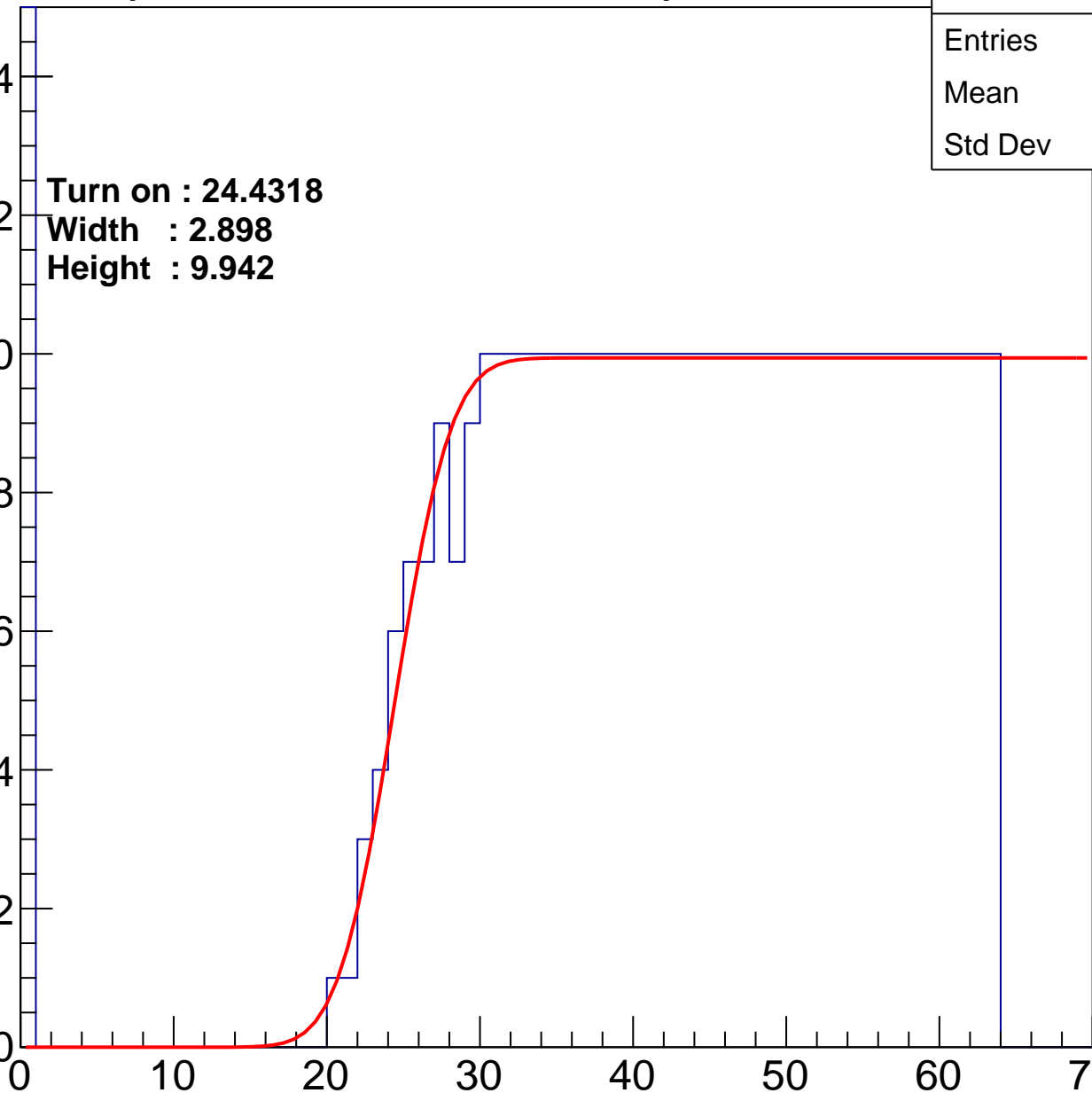
Width : 2.898

Height : 9.942

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch89

calib_packv5_041523_1651.root, FC#0, port C2

Entries	422
Mean	39.76
Std Dev	17.34

Turn on : 26.3708

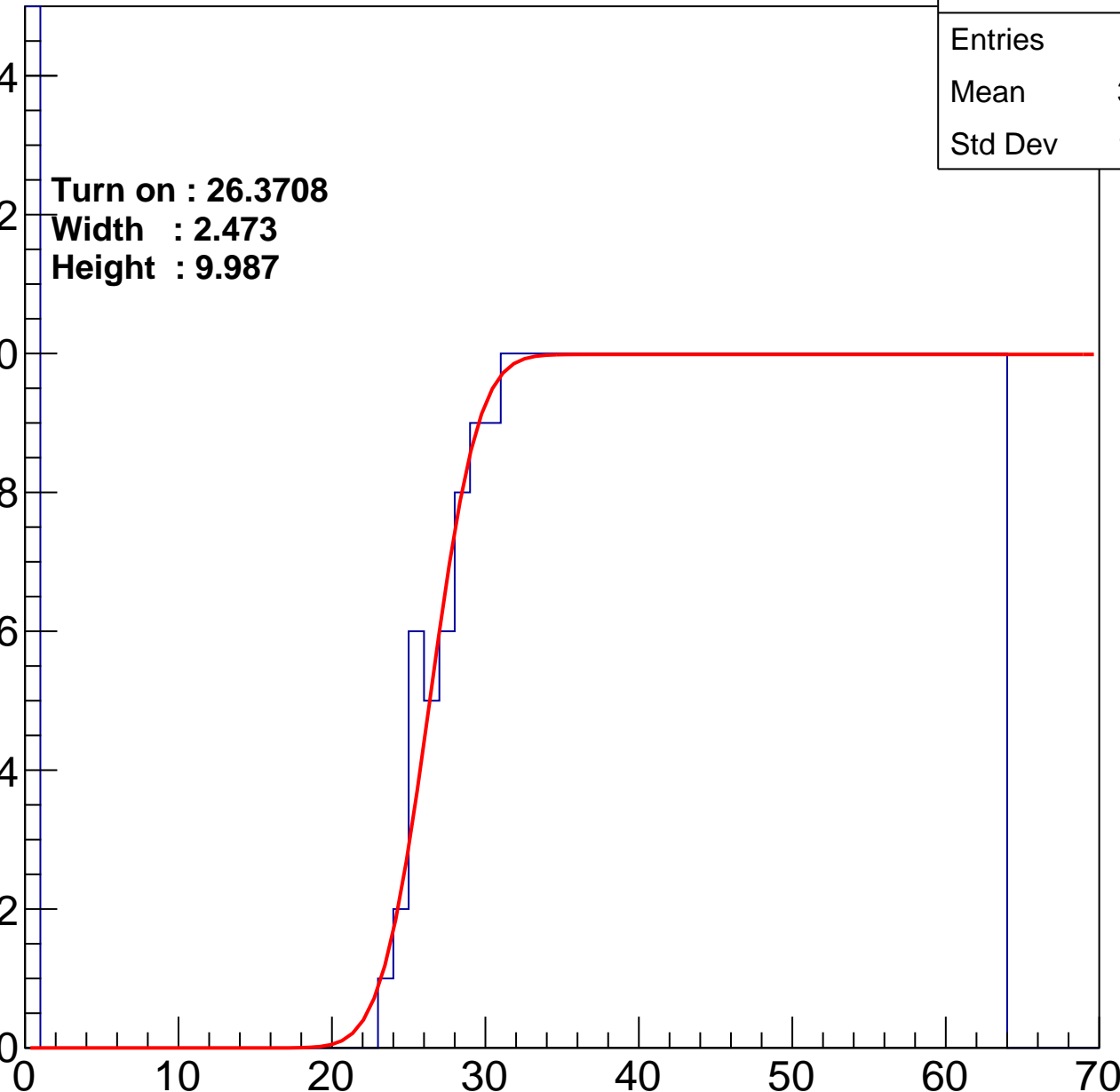
Width : 2.473

Height : 9.987

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch90

calib_packv5_041523_1651.root, FC#0, port C2

Entries	448
Mean	38.22
Std Dev	18.14

Turn on : 24.7207

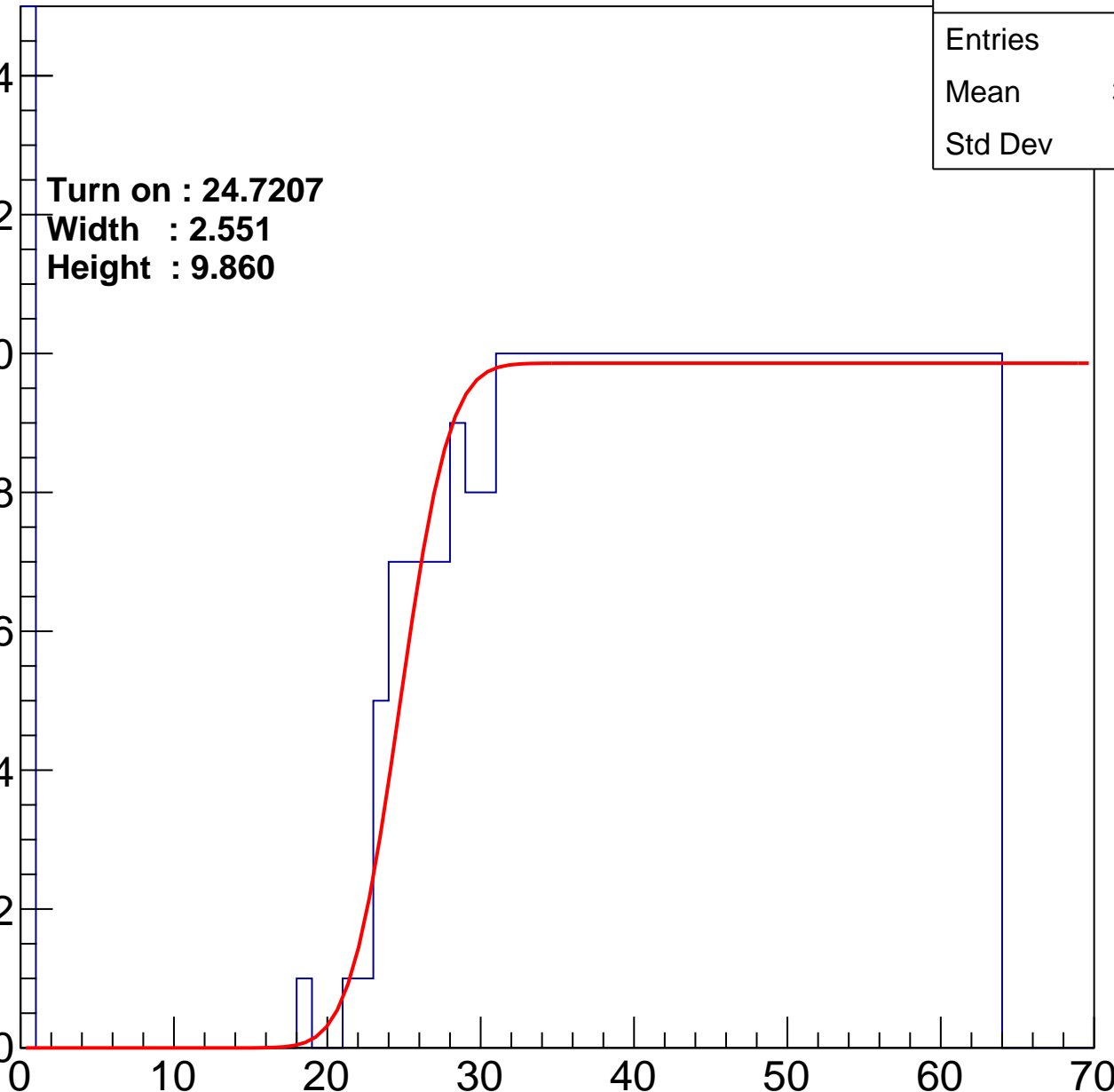
Width : 2.551

Height : 9.860

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch91

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	39.83
Std Dev	17.42

Turn on : 27.0071

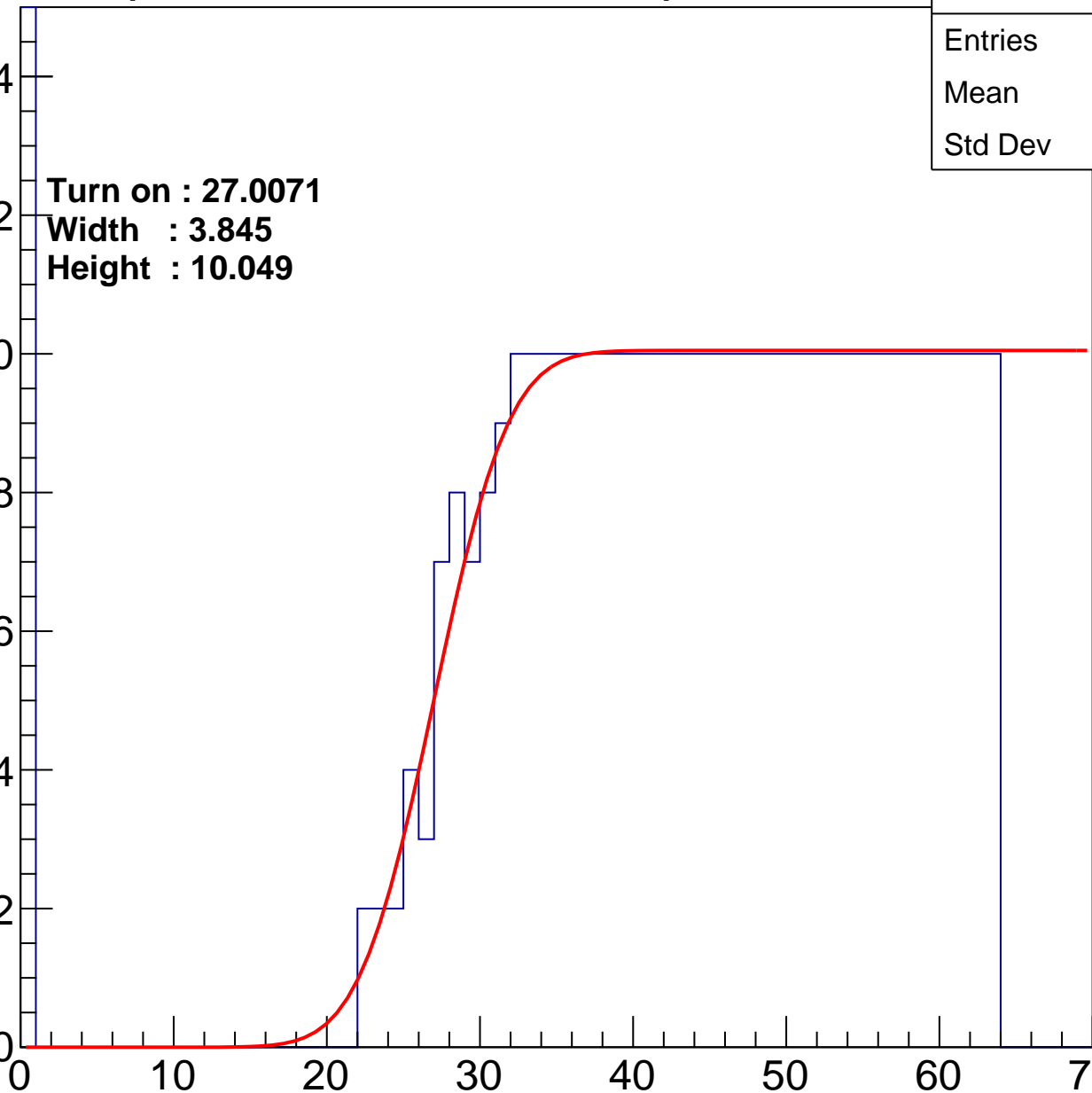
Width : 3.845

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch92

calib_packv5_041523_1651.root, FC#0, port C2

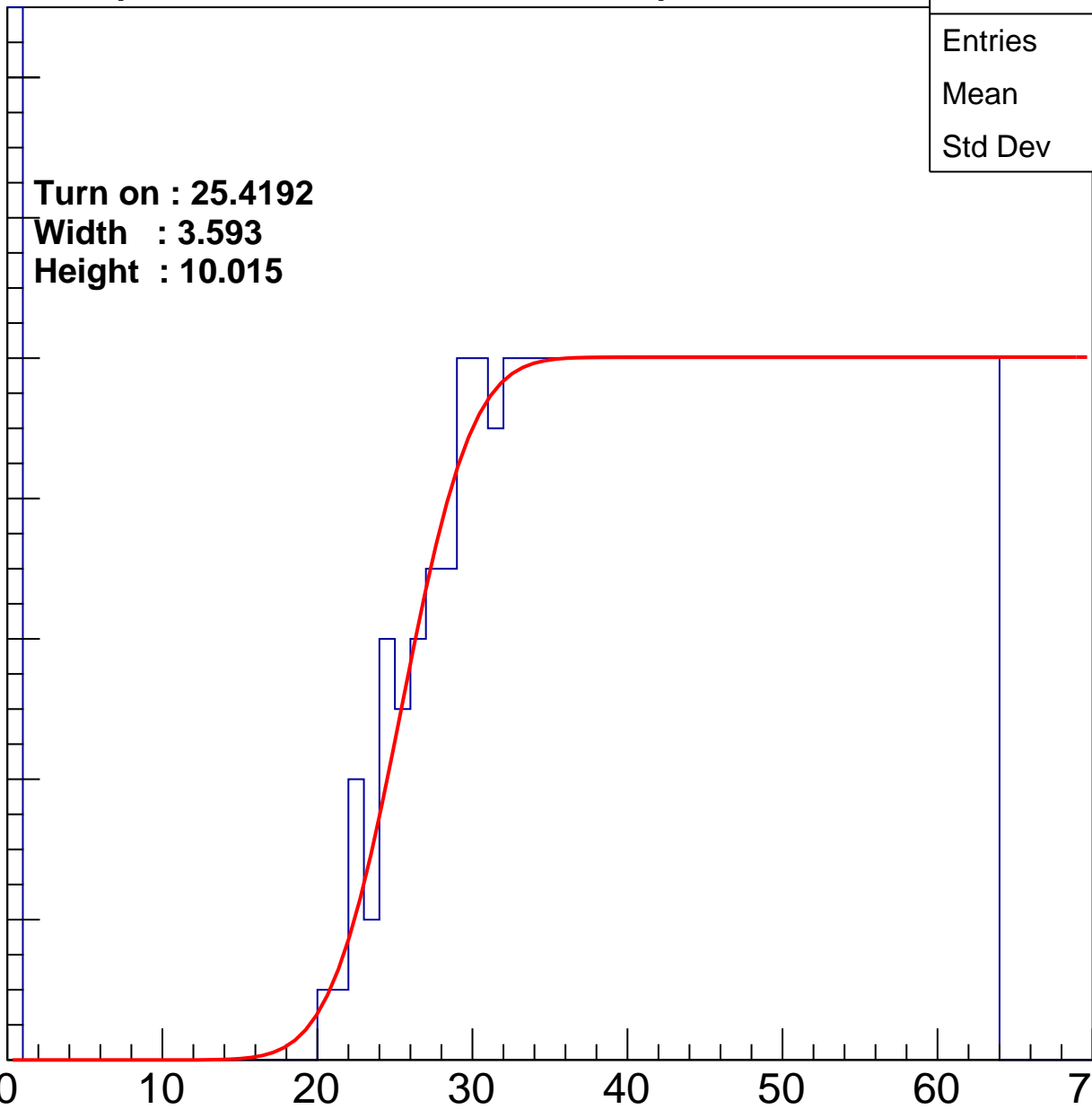
Entry

14
12
10
8
6
4
2
0

Turn on : 25.4192
Width : 3.593
Height : 10.015

Entries	440
Mean	38.76
Std Dev	17.8

ampl



B1L103S, U8-ch93

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.48
Std Dev	17.42

Turn on : 25.7283

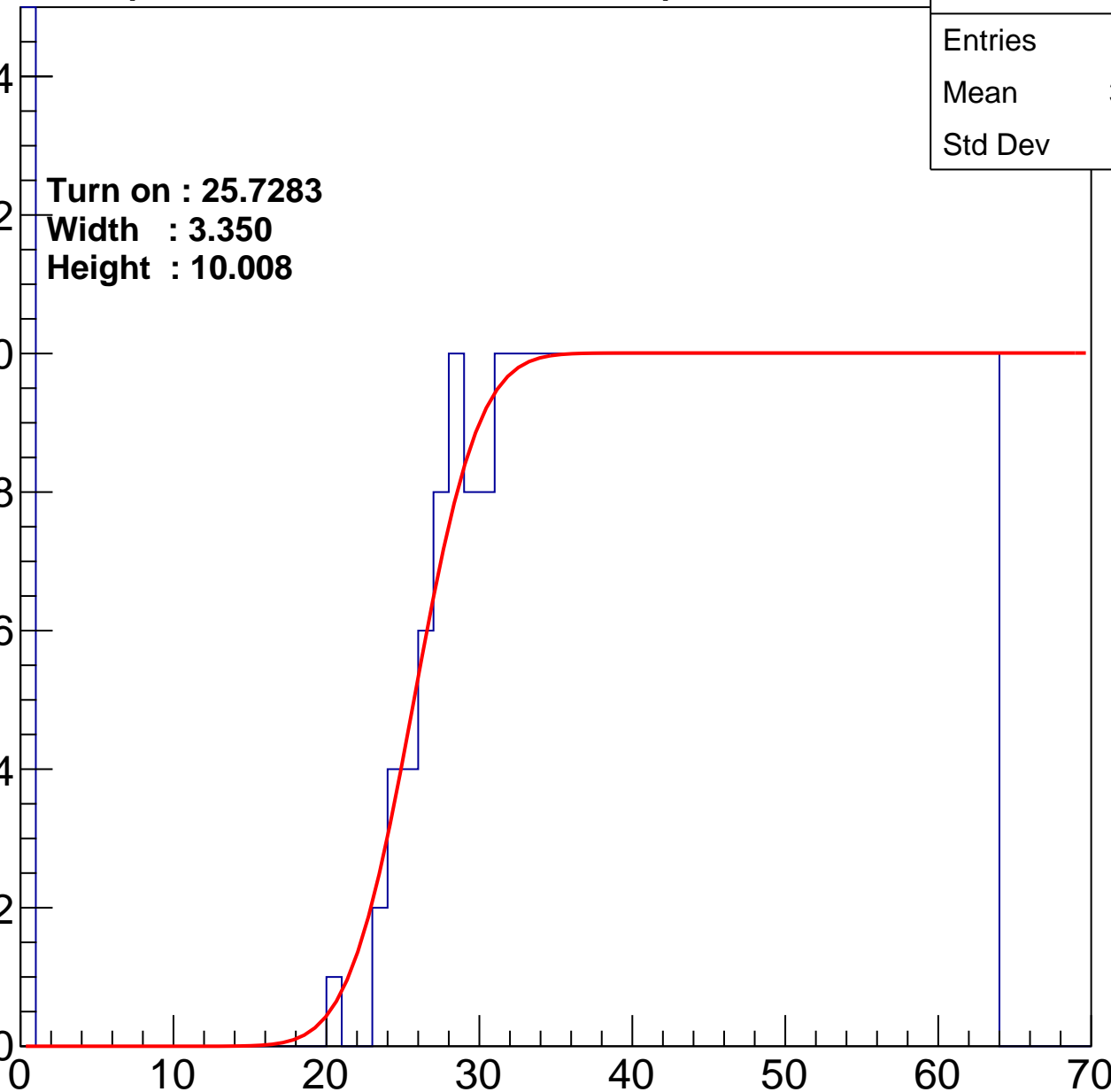
Width : 3.350

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch94

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	40.36
Std Dev	16.72

Turn on : 26.5428

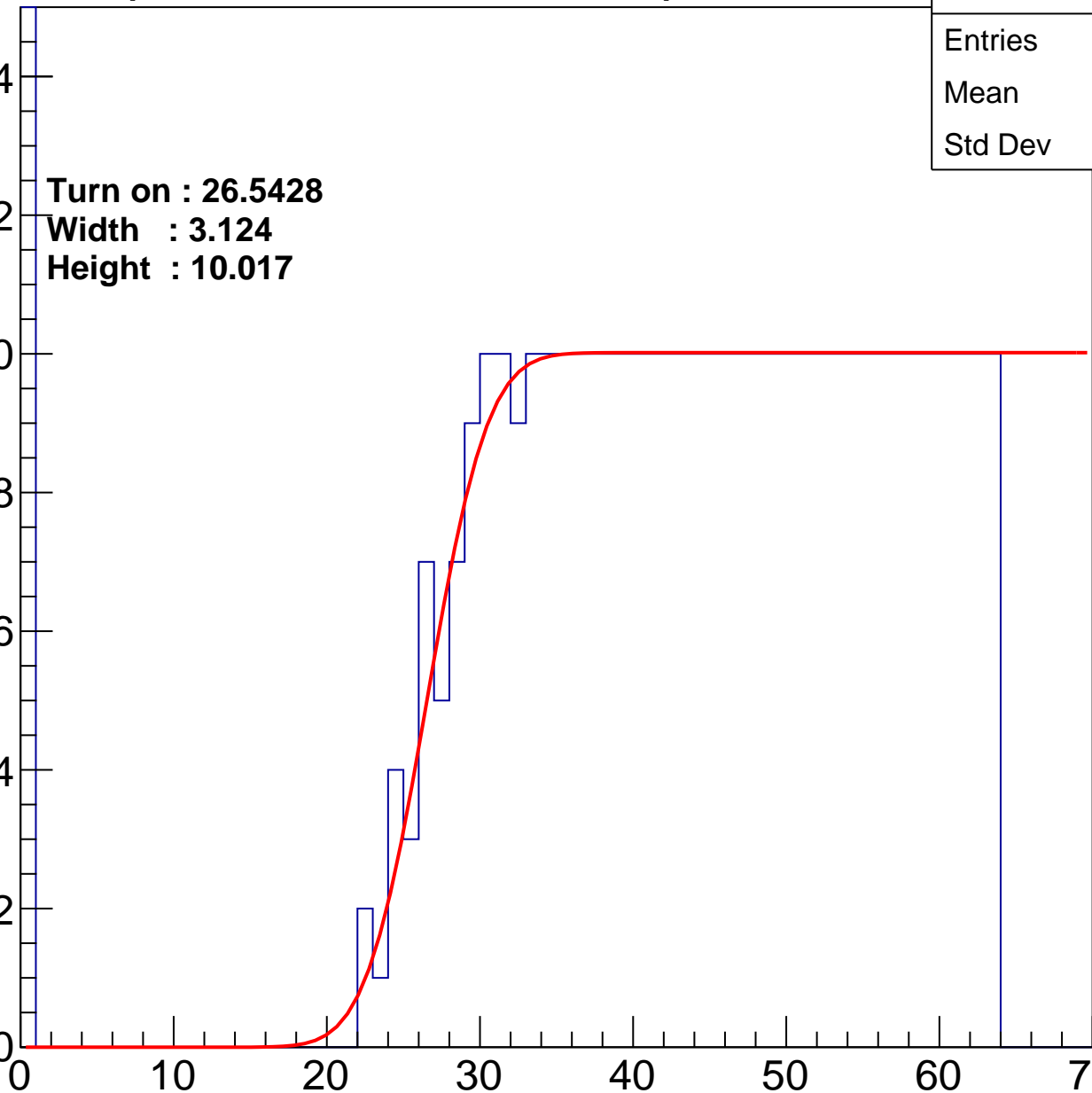
Width : 3.124

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch95

calib_packv5_041523_1651.root, FC#0, port C2

Entries	412
Mean	40.91
Std Dev	16.04

Turn on : 26.6650

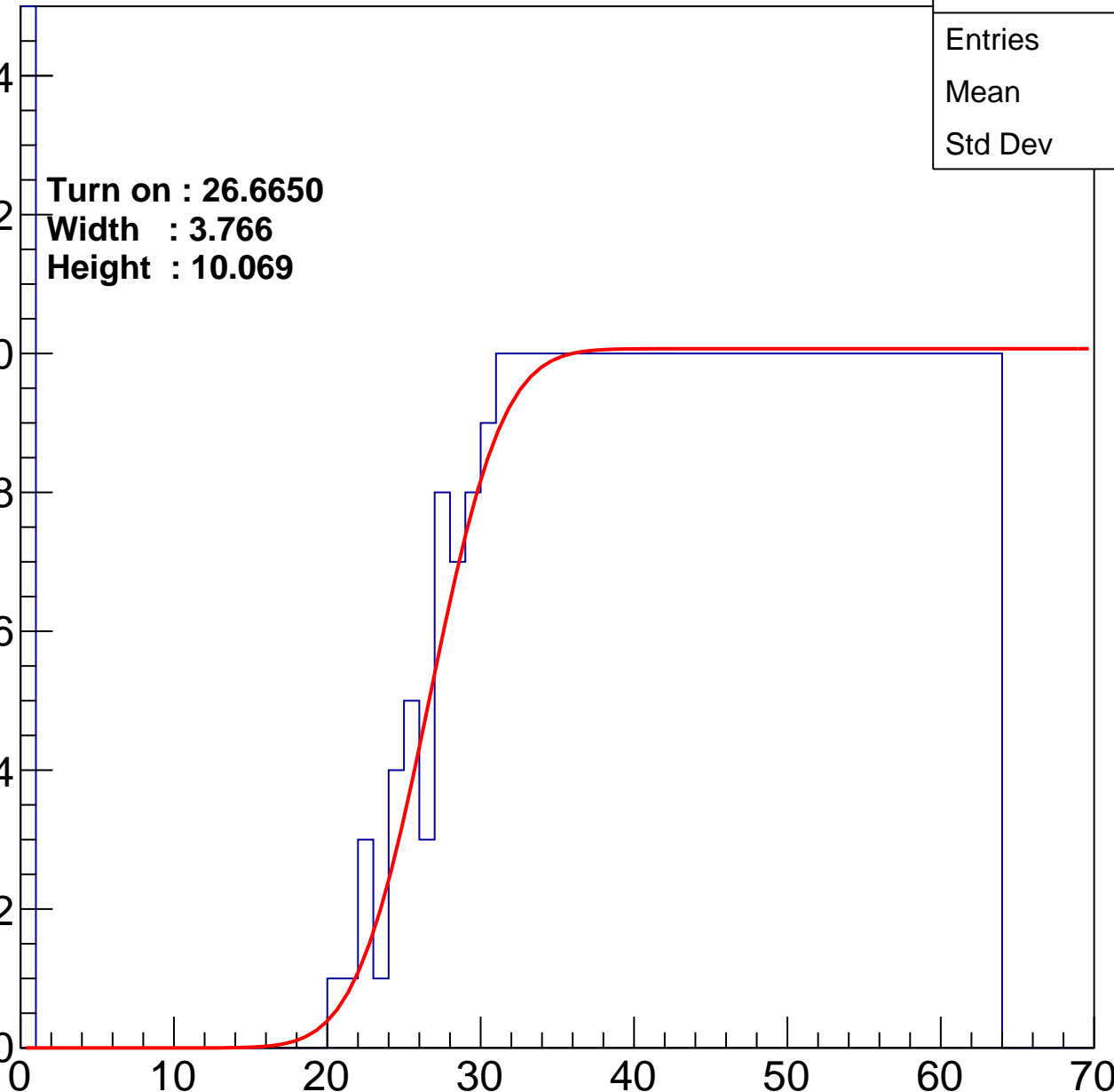
Width : 3.766

Height : 10.069

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch96

calib_packv5_041523_1651.root, FC#0, port C2

Entries	453
Mean	37.95
Std Dev	18.27

Turn on : 24.9183

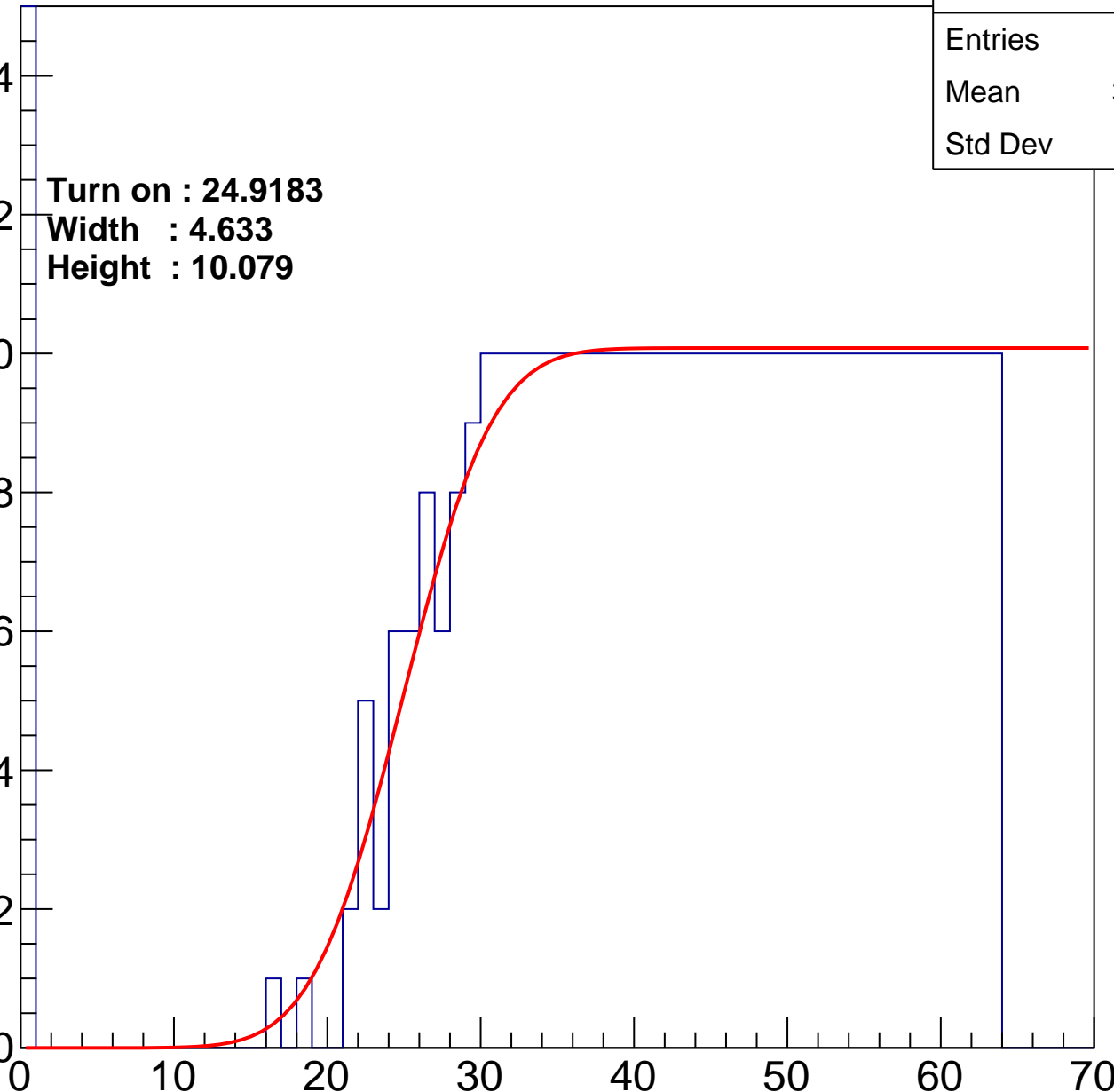
Width : 4.633

Height : 10.079

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch97

calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	39.09
Std Dev	17.72

Turn on : 25.9032

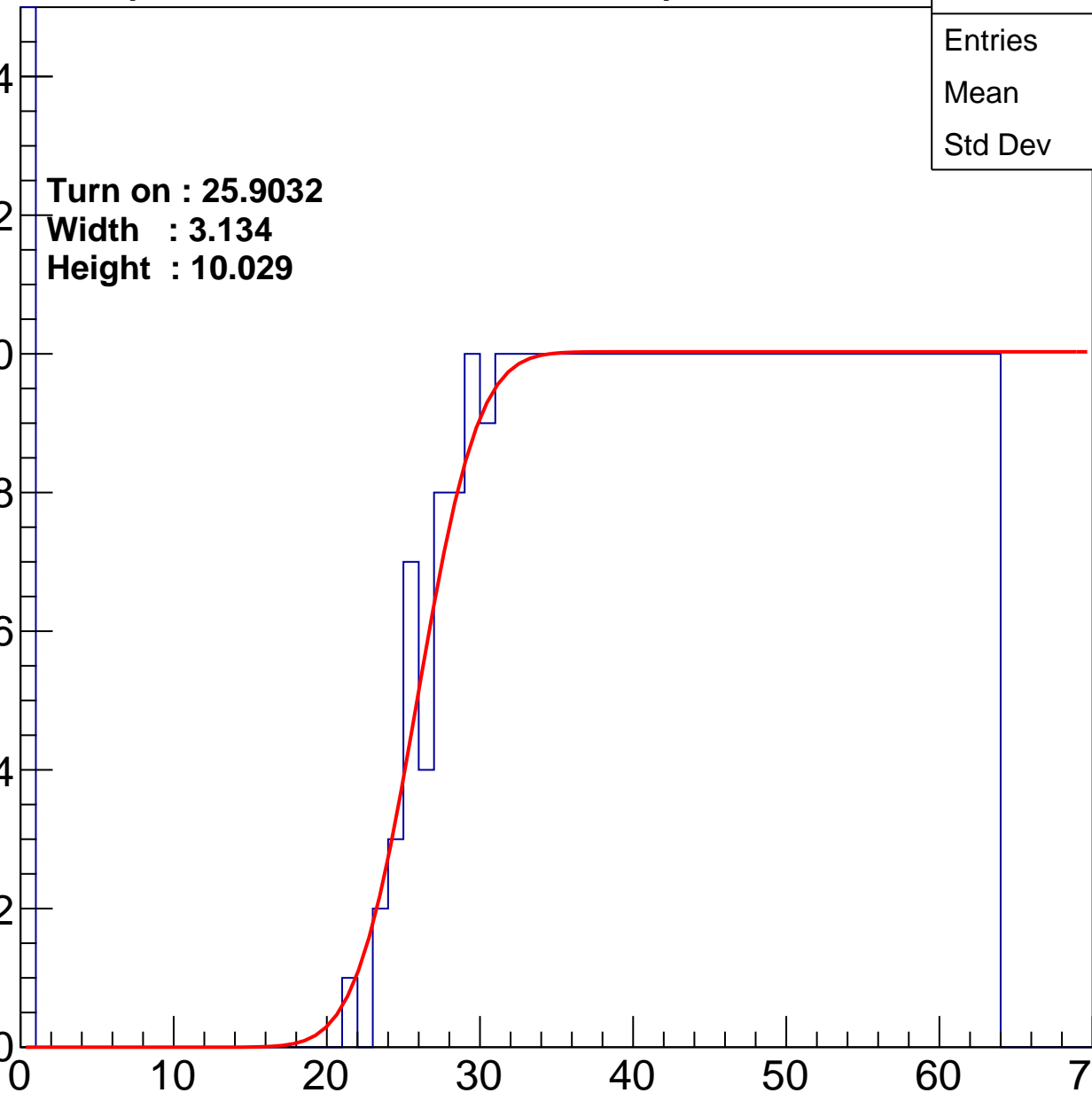
Width : 3.134

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl

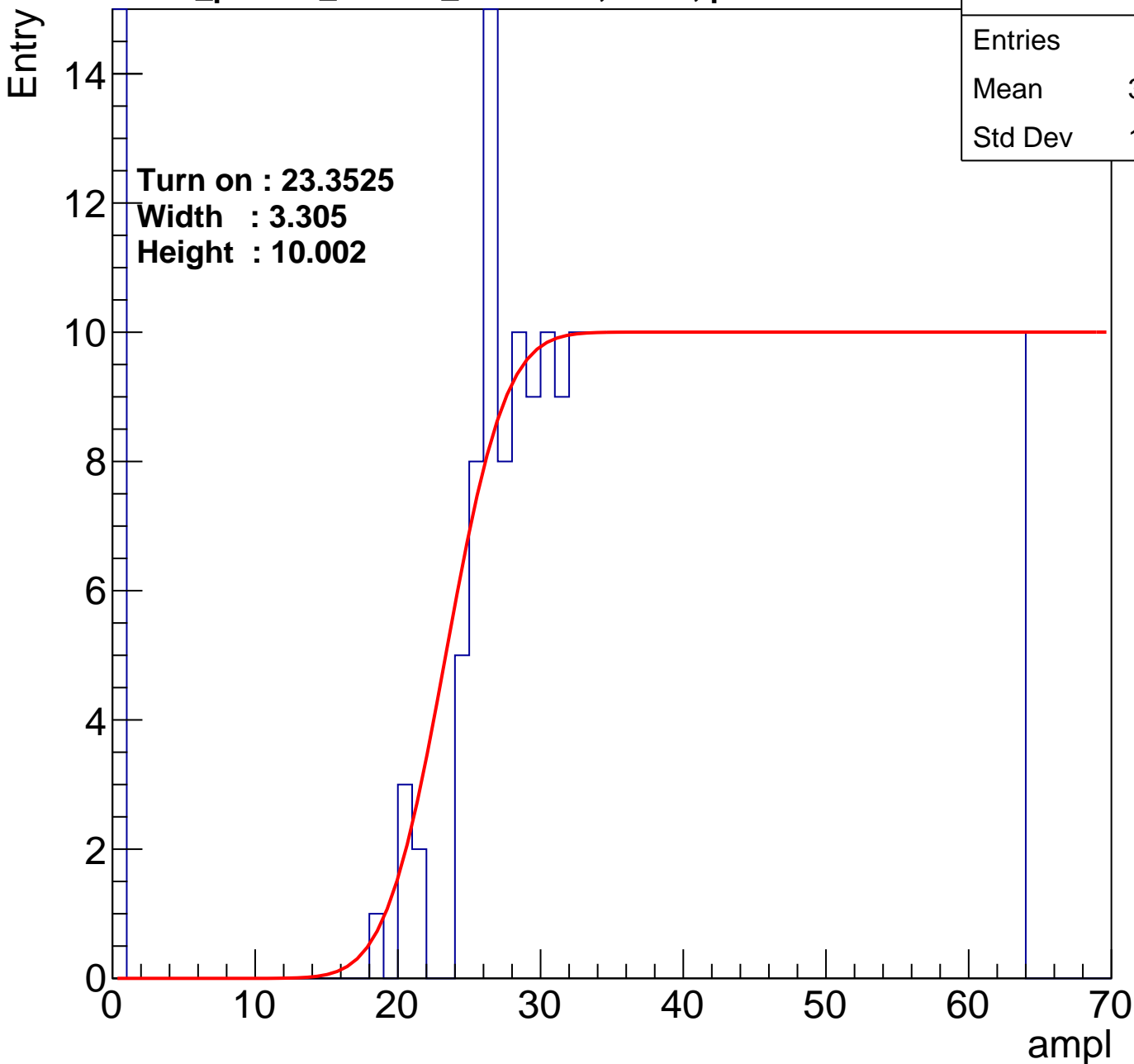


B1L103S, U8-ch98

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	39.74
Std Dev	16.47

Turn on : 23.3525
Width : 3.305
Height : 10.002



B1L103S, U8-ch99

calib_packv5_041523_1651.root, FC#0, port C2

Entries	422
Mean	39.54
Std Dev	17.65

Turn on : 26.7563

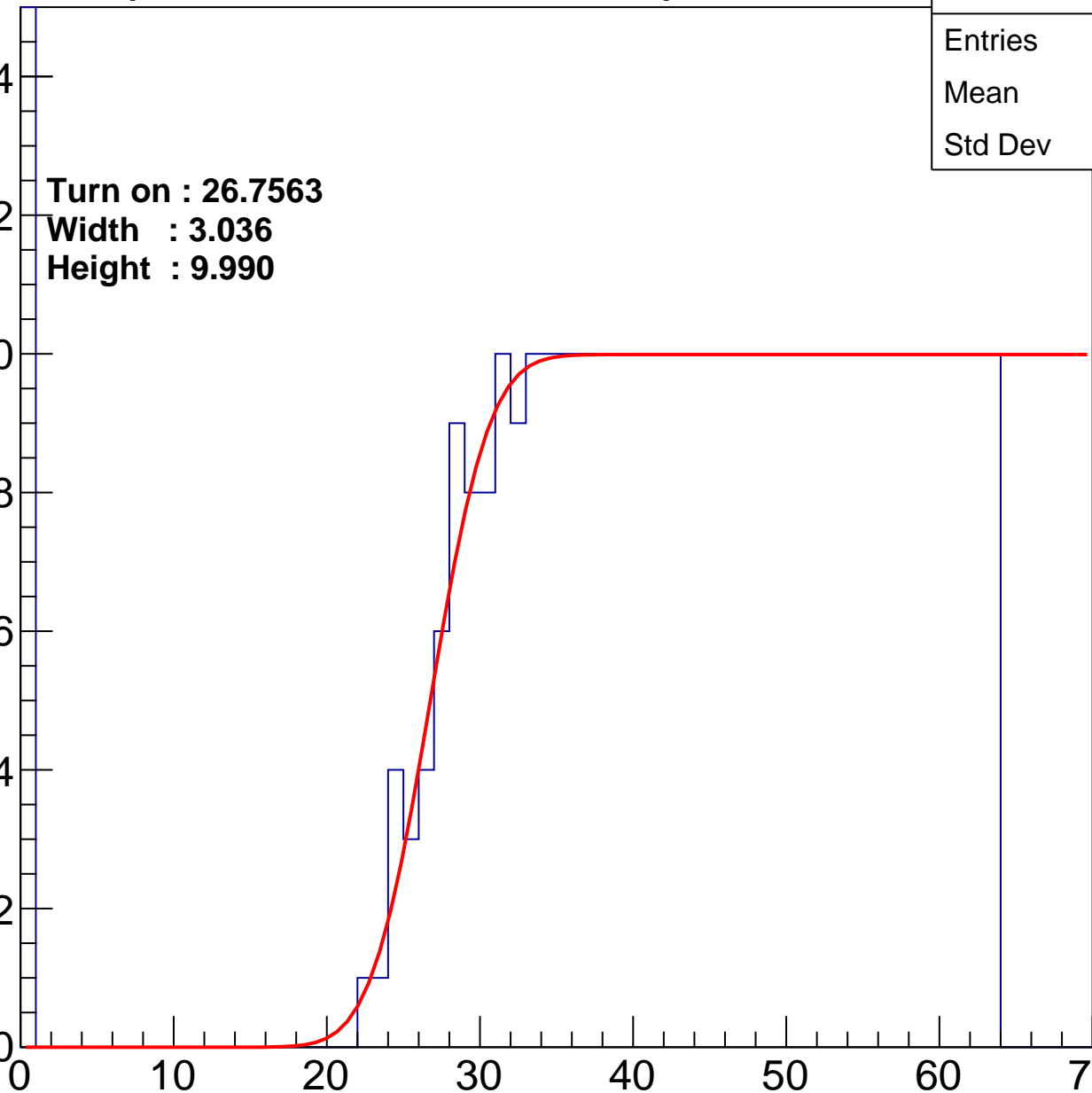
Width : 3.036

Height : 9.990

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch100

calib_packv5_041523_1651.root, FC#0, port C2

Entries	425
Mean	40.33
Std Dev	16.2

Turn on : 25.7636

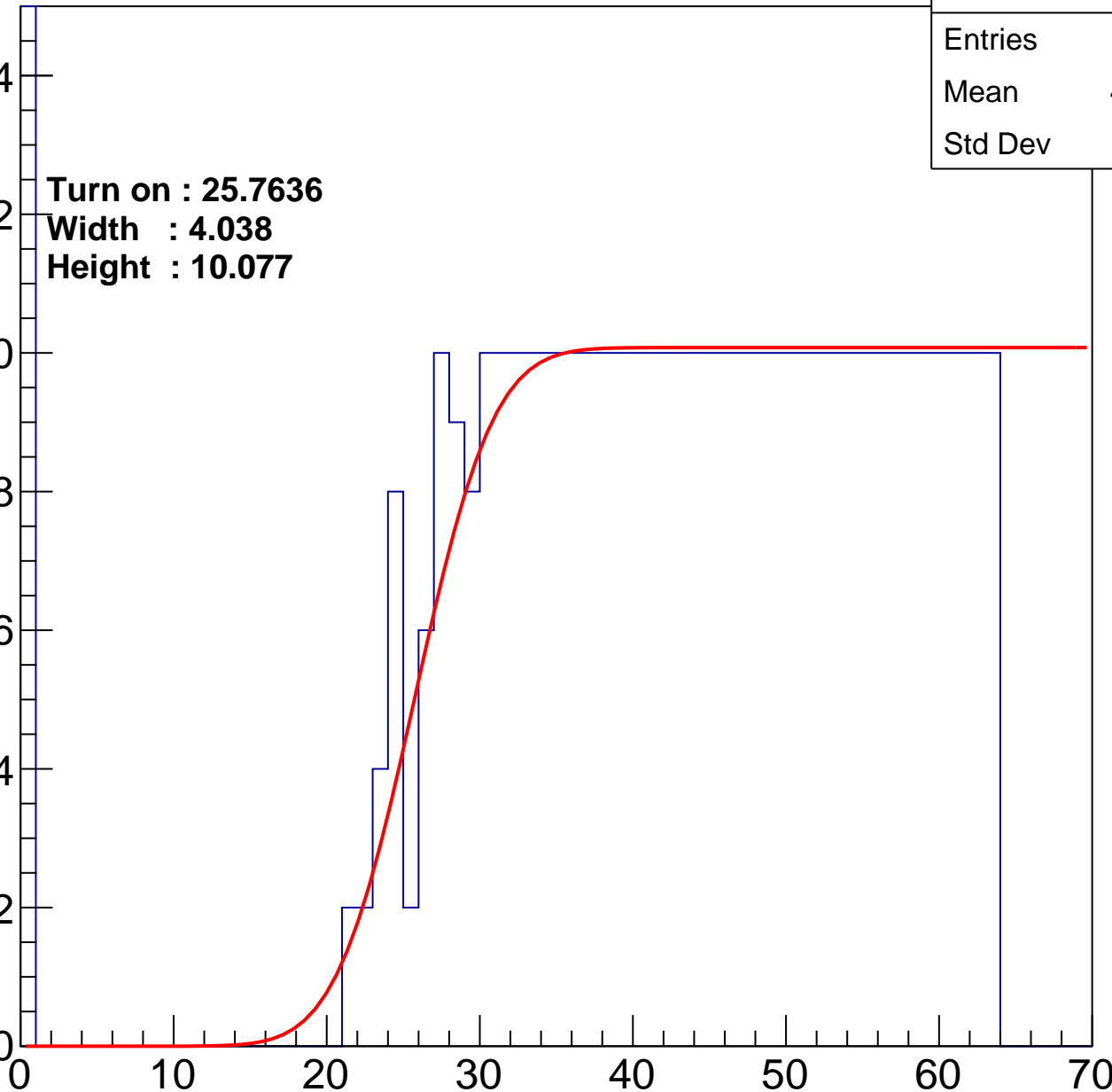
Width : 4.038

Height : 10.077

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch101

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	39.24
Std Dev	17.31

Turn on : 25.3257

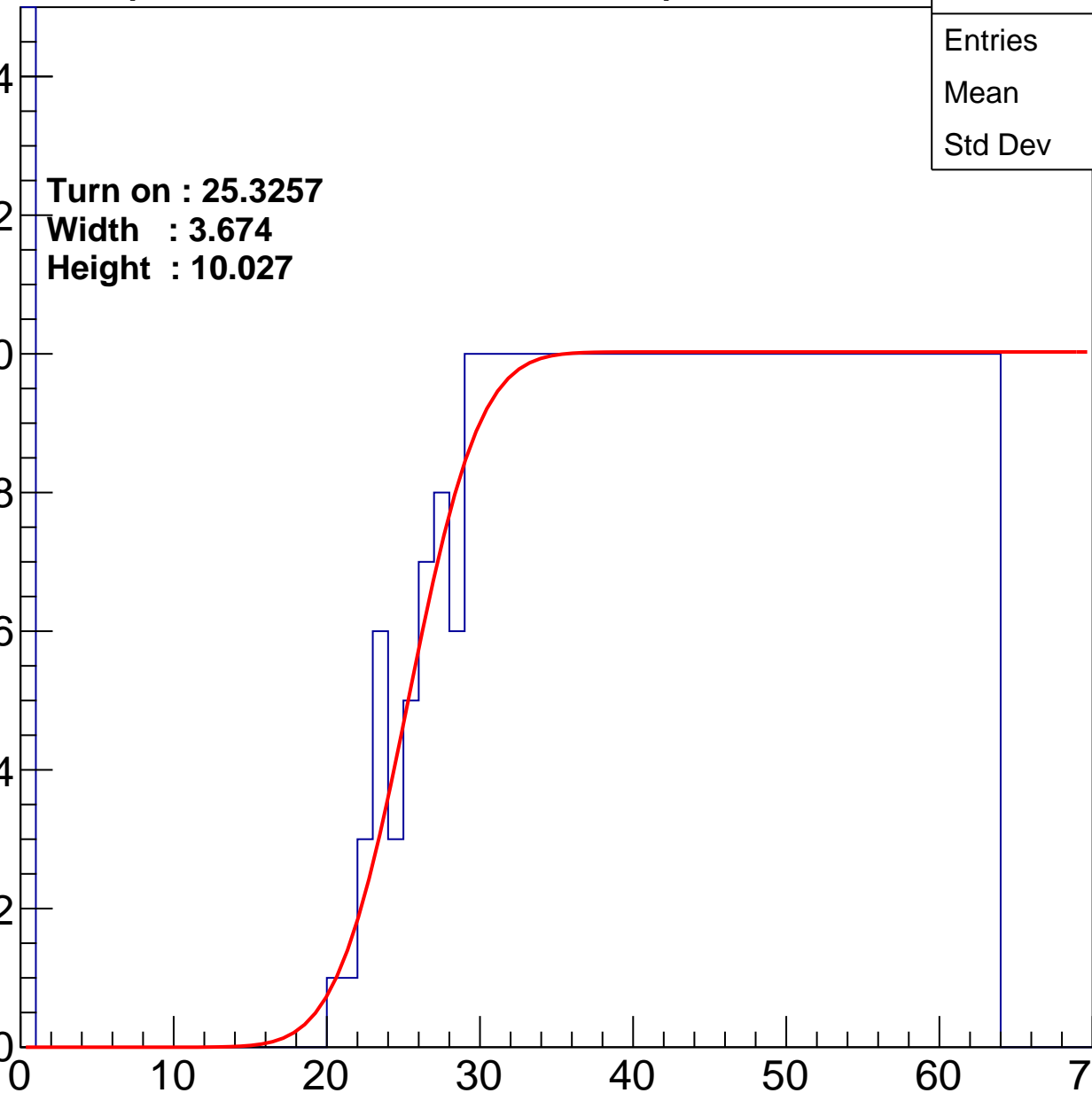
Width : 3.674

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch102

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	39.59
Std Dev	17.46

Turn on : 26.4391

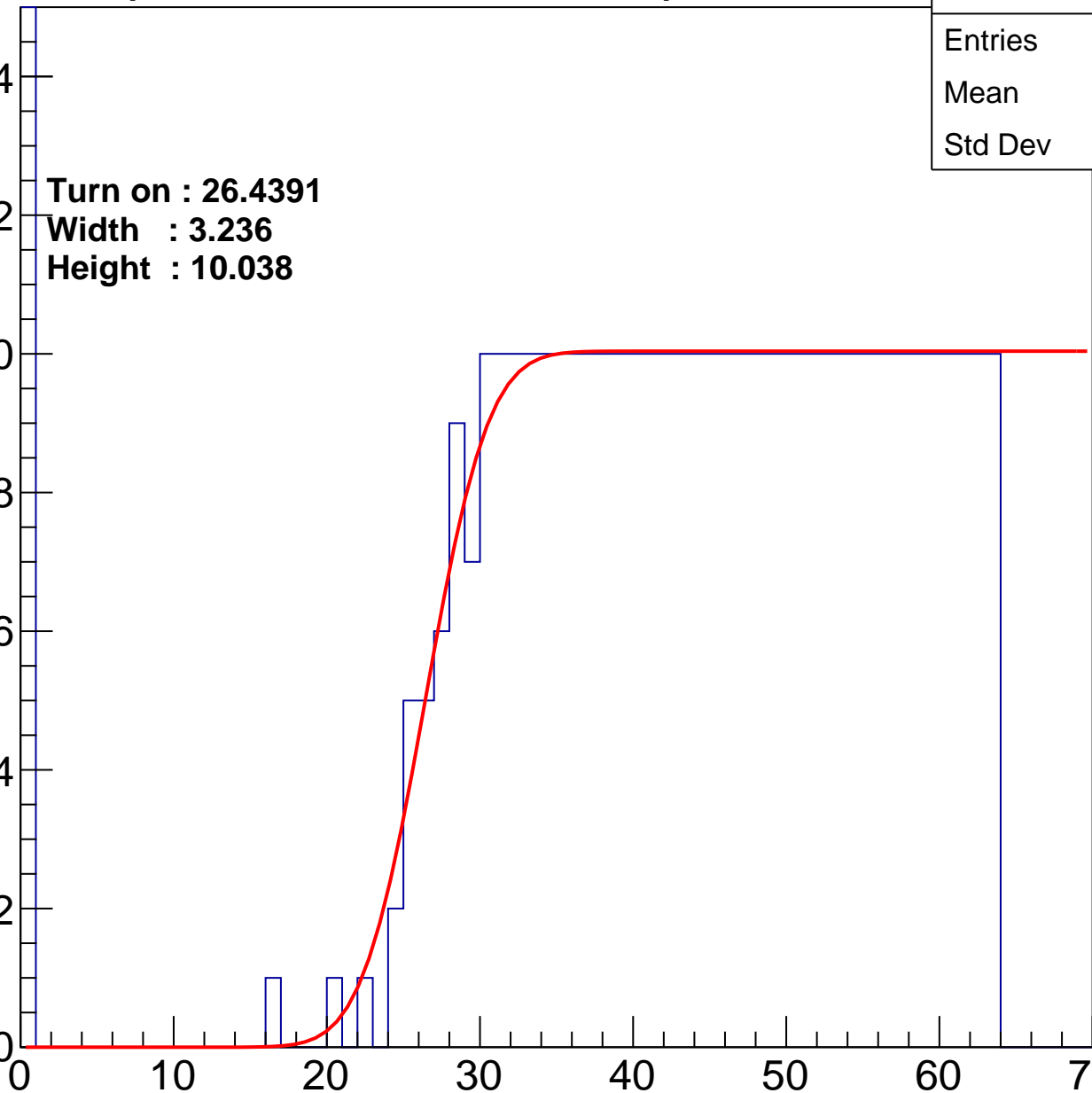
Width : 3.236

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch103

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	39.35
Std Dev	17.07

Turn on : 24.9884

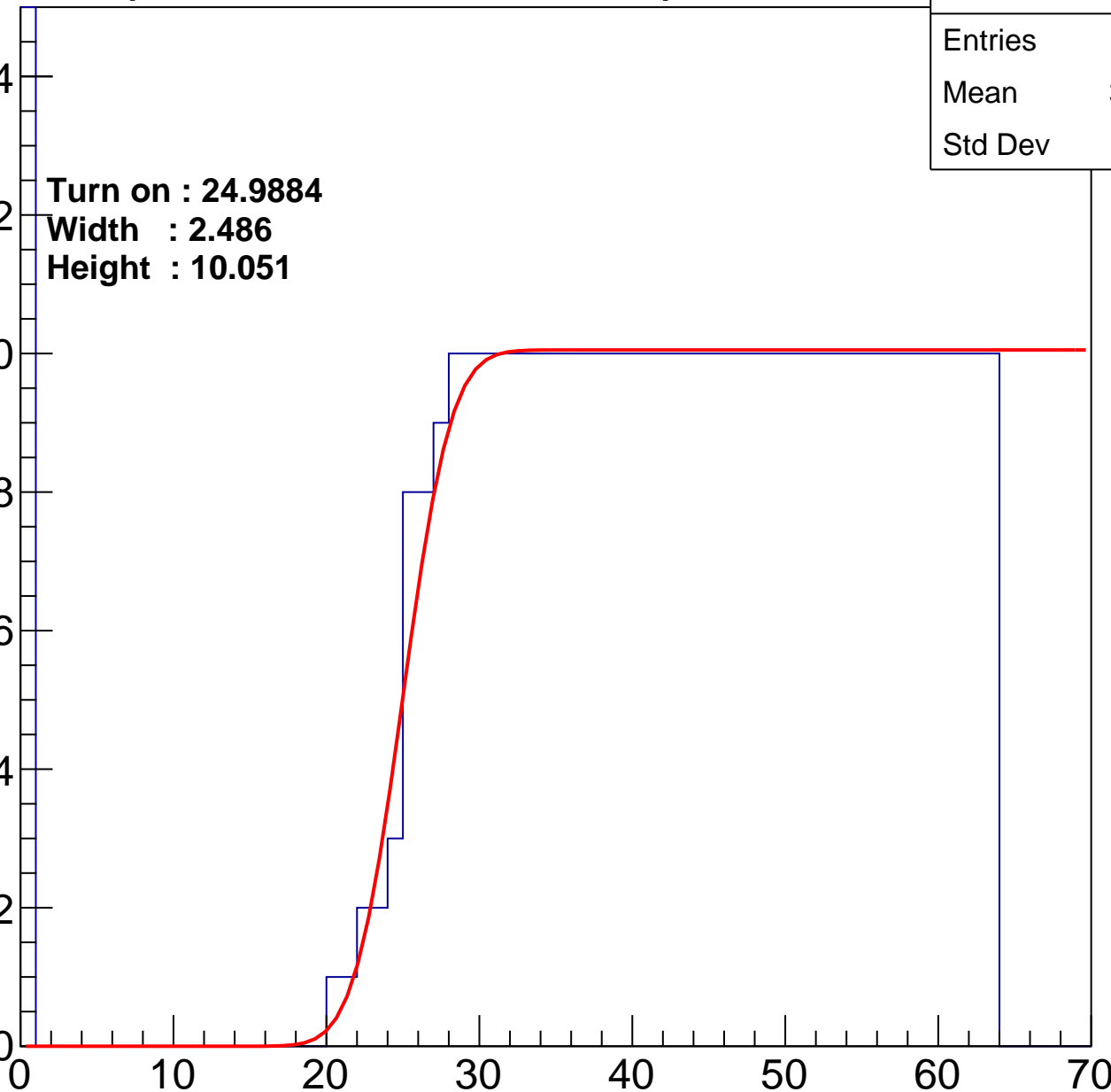
Width : 2.486

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch104

calib_packv5_041523_1651.root, FC#0, port C2

Entries	458
Mean	38.16
Std Dev	17.74

Turn on : 23.3989

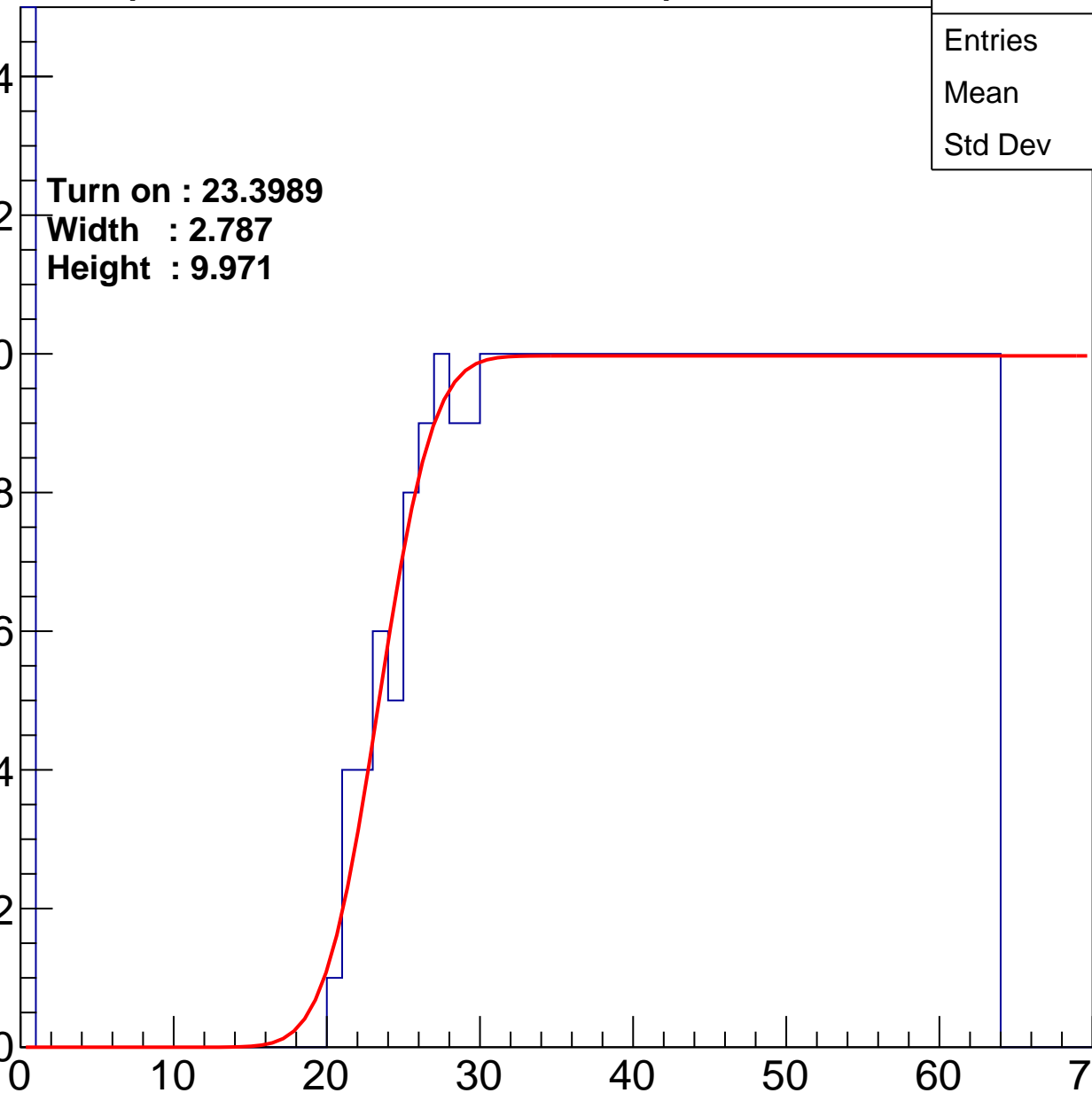
Width : 2.787

Height : 9.971

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch105

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	39.38
Std Dev	17.49

Turn on : 25.8492

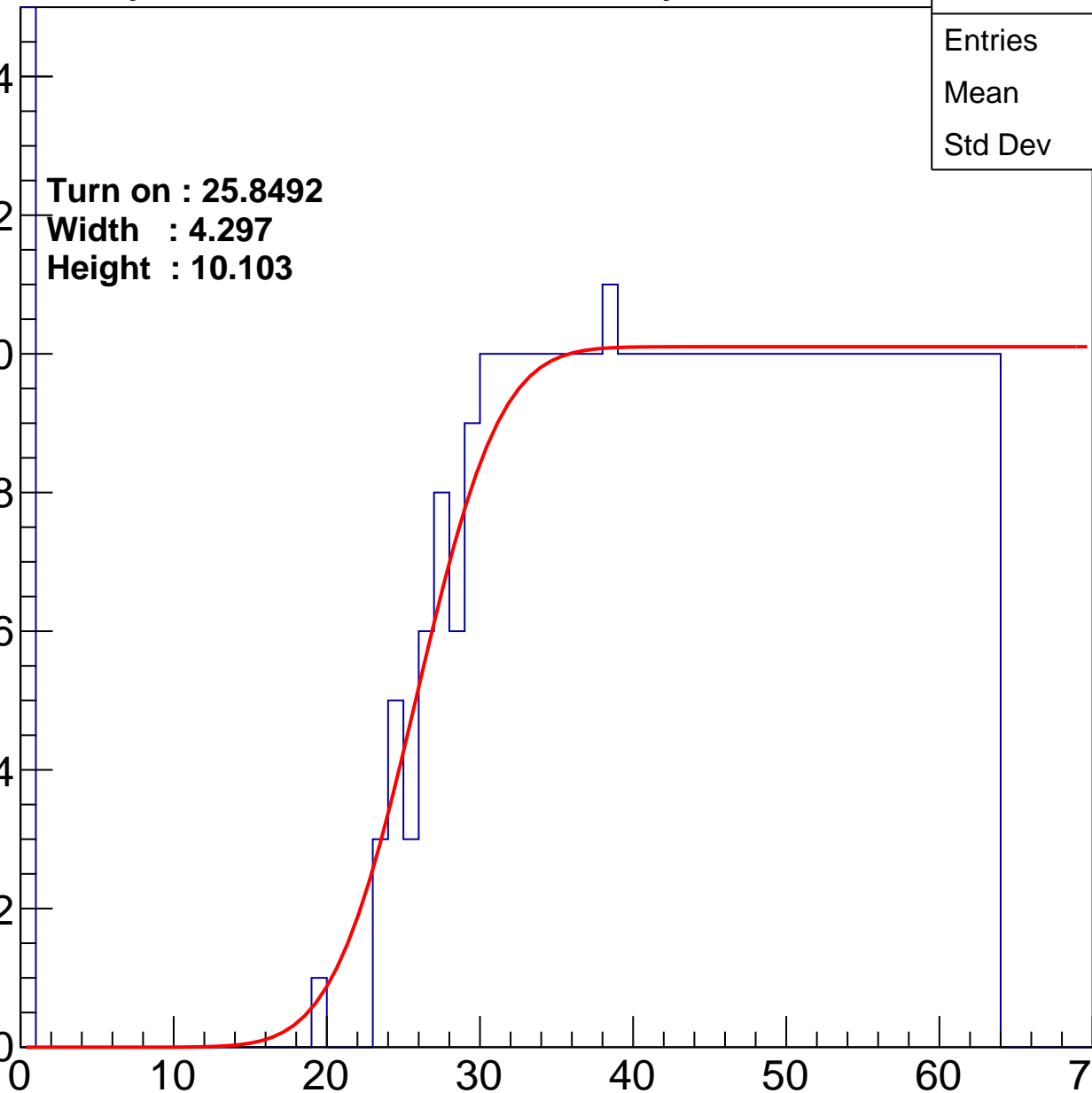
Width : 4.297

Height : 10.103

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch106

calib_packv5_041523_1651.root, FC#0, port C2

Entries	447
Mean	38.65
Std Dev	17.59

Turn on : 24.4640

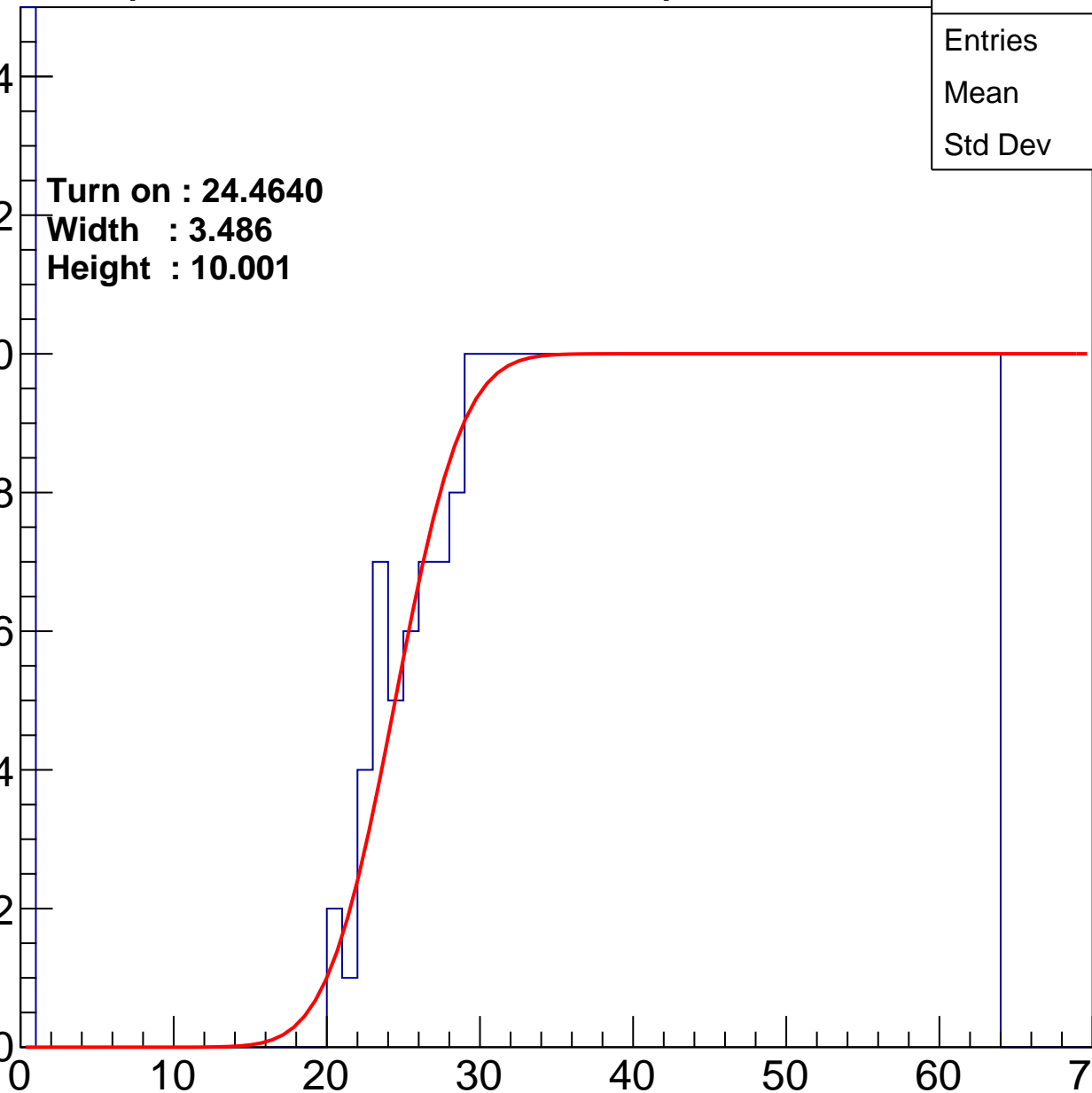
Width : 3.486

Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch107

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	40.07
Std Dev	16.59

Turn on : 25.3621

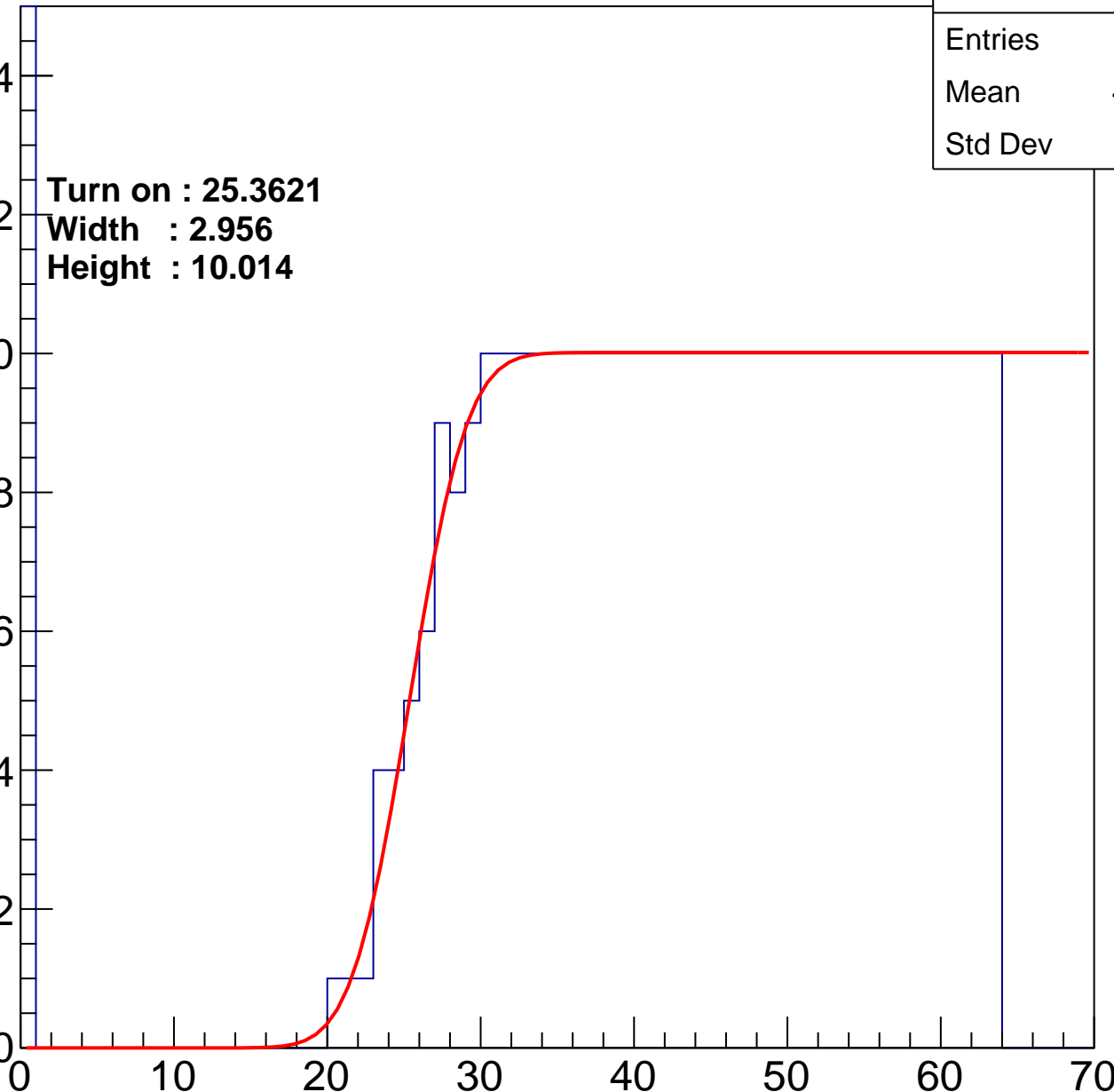
Width : 2.956

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch108

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	38.9
Std Dev	17.61

Turn on : 25.0193

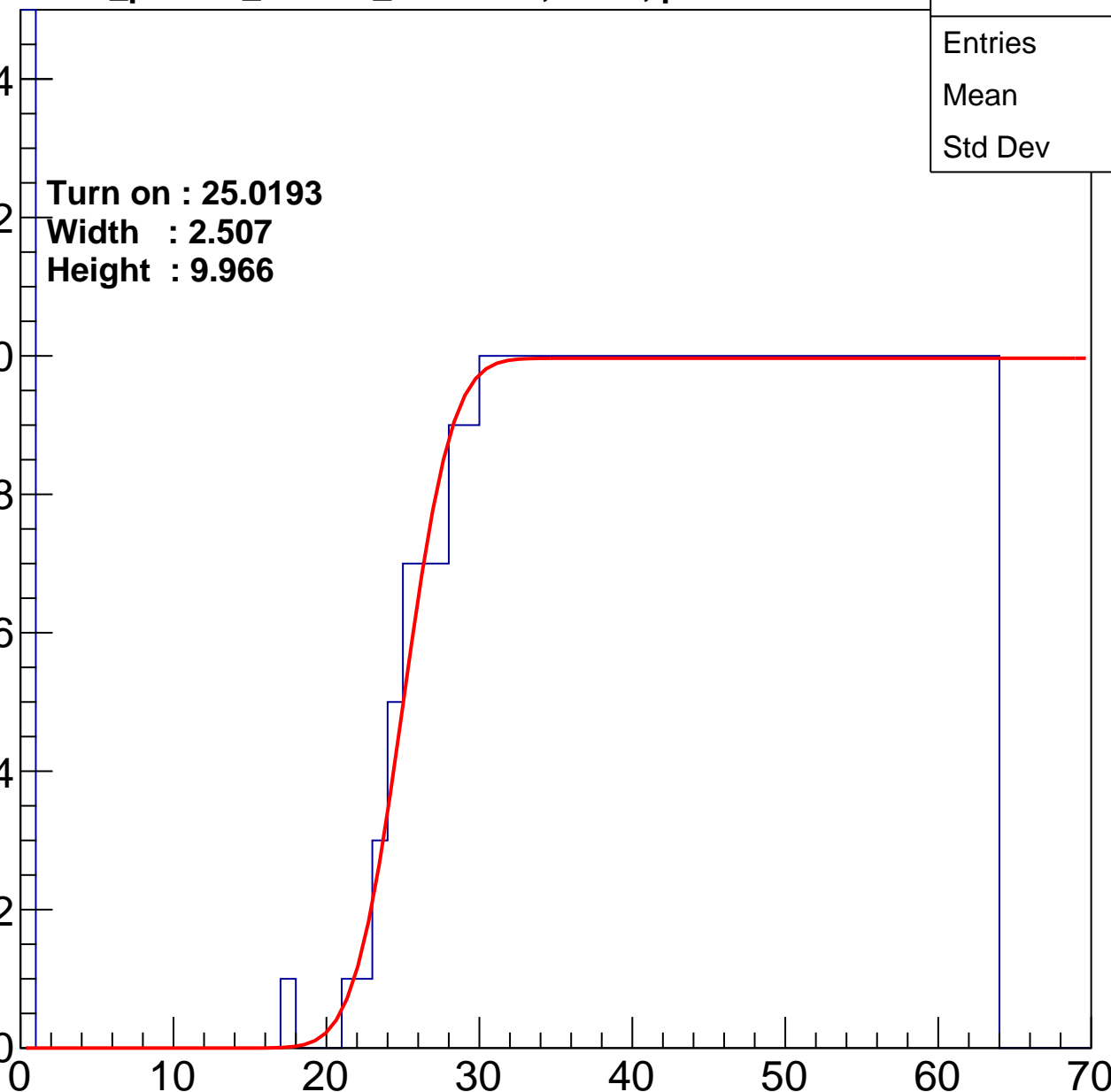
Width : 2.507

Height : 9.966

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch109

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	38.91
Std Dev	17.61

Turn on : 25.2519

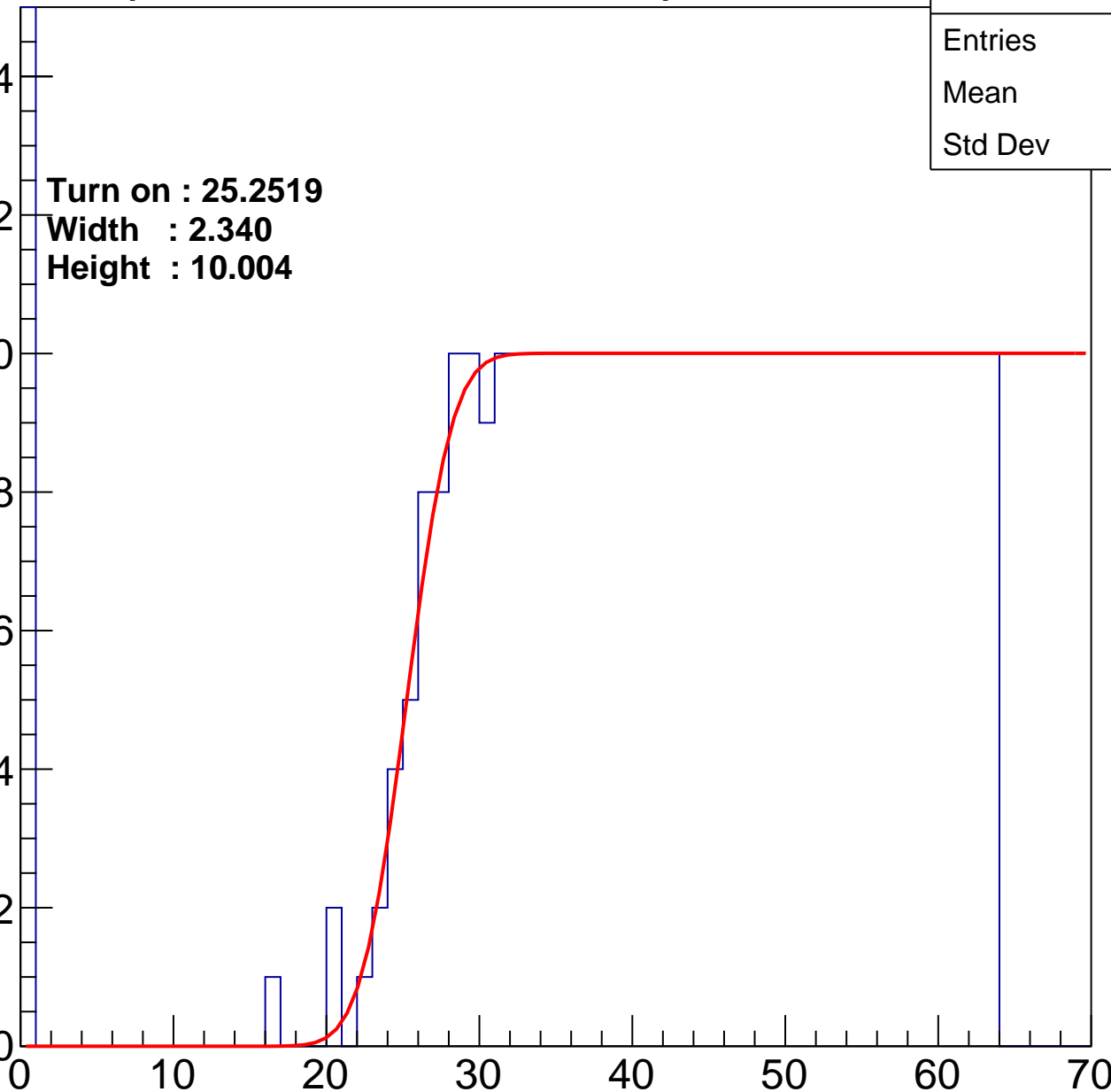
Width : 2.340

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch110

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	38.49
Std Dev	18.09

Turn on : 25.5232

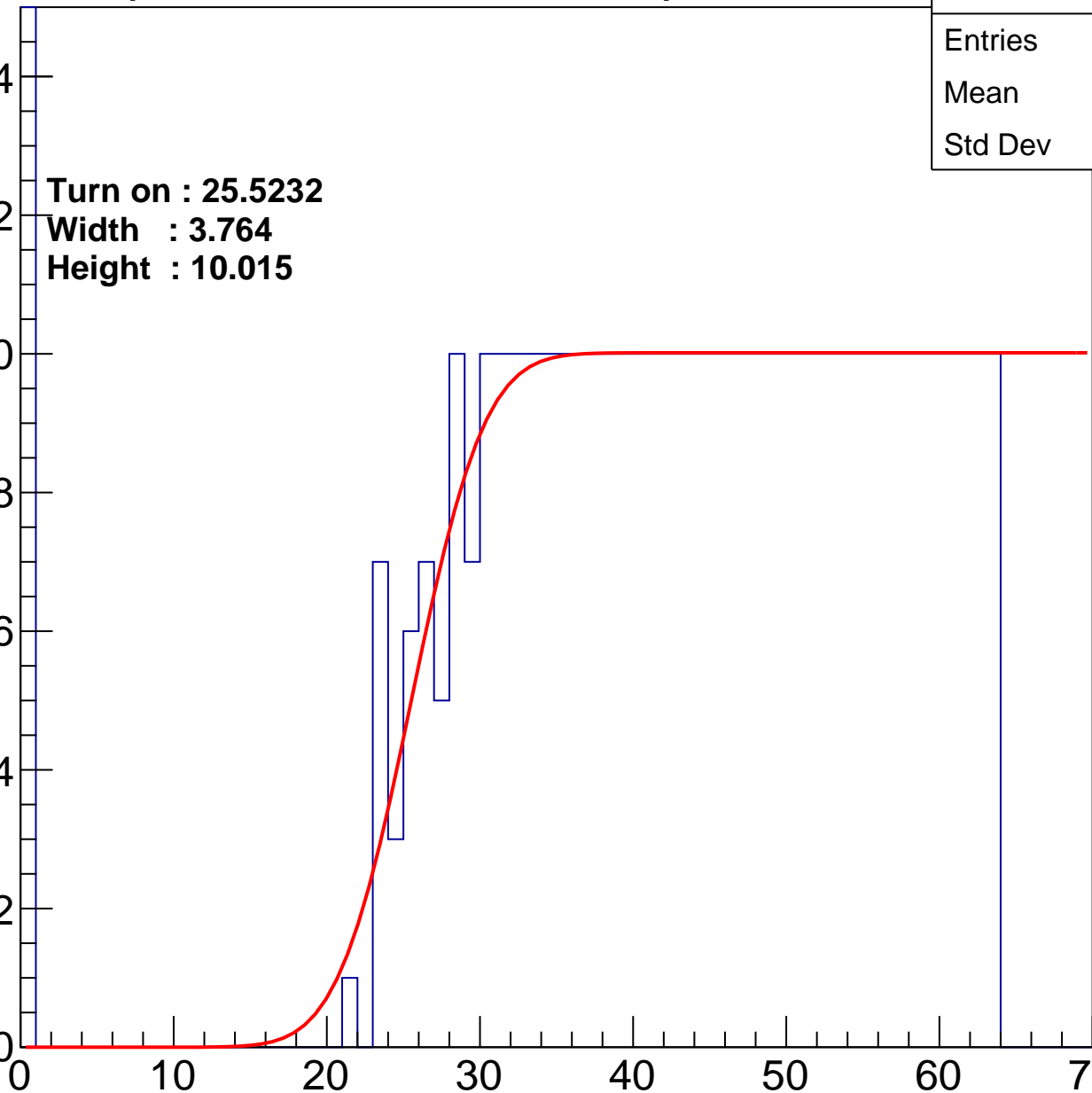
Width : 3.764

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch111

calib_packv5_041523_1651.root, FC#0, port C2

Entries	425
Mean	39.29
Std Dev	17.88

Turn on : 26.9734

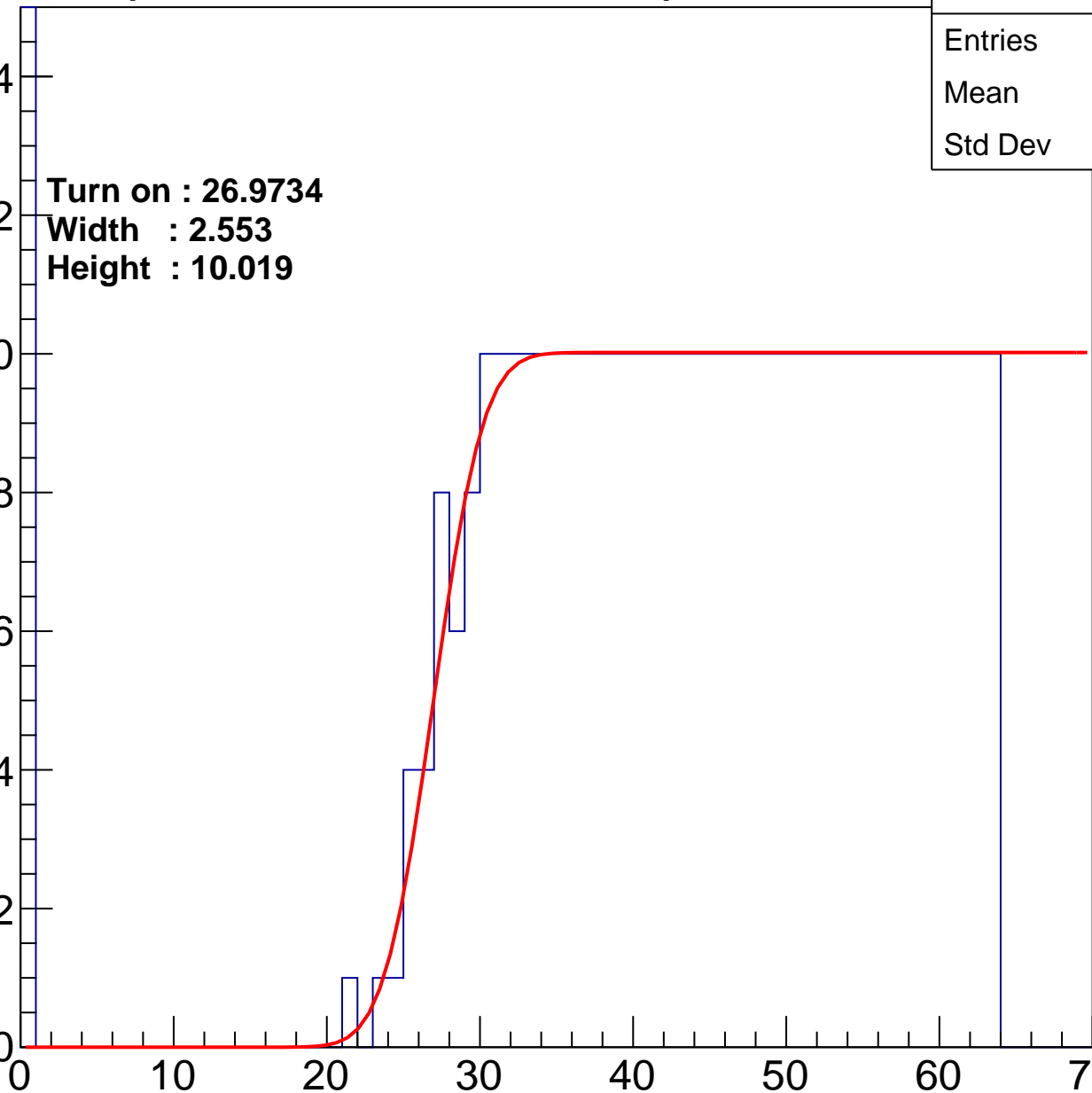
Width : 2.553

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch112

calib_packv5_041523_1651.root, FC#0, port C2

Entries	458
Mean	37.87
Std Dev	18.2

Turn on : 24.7311

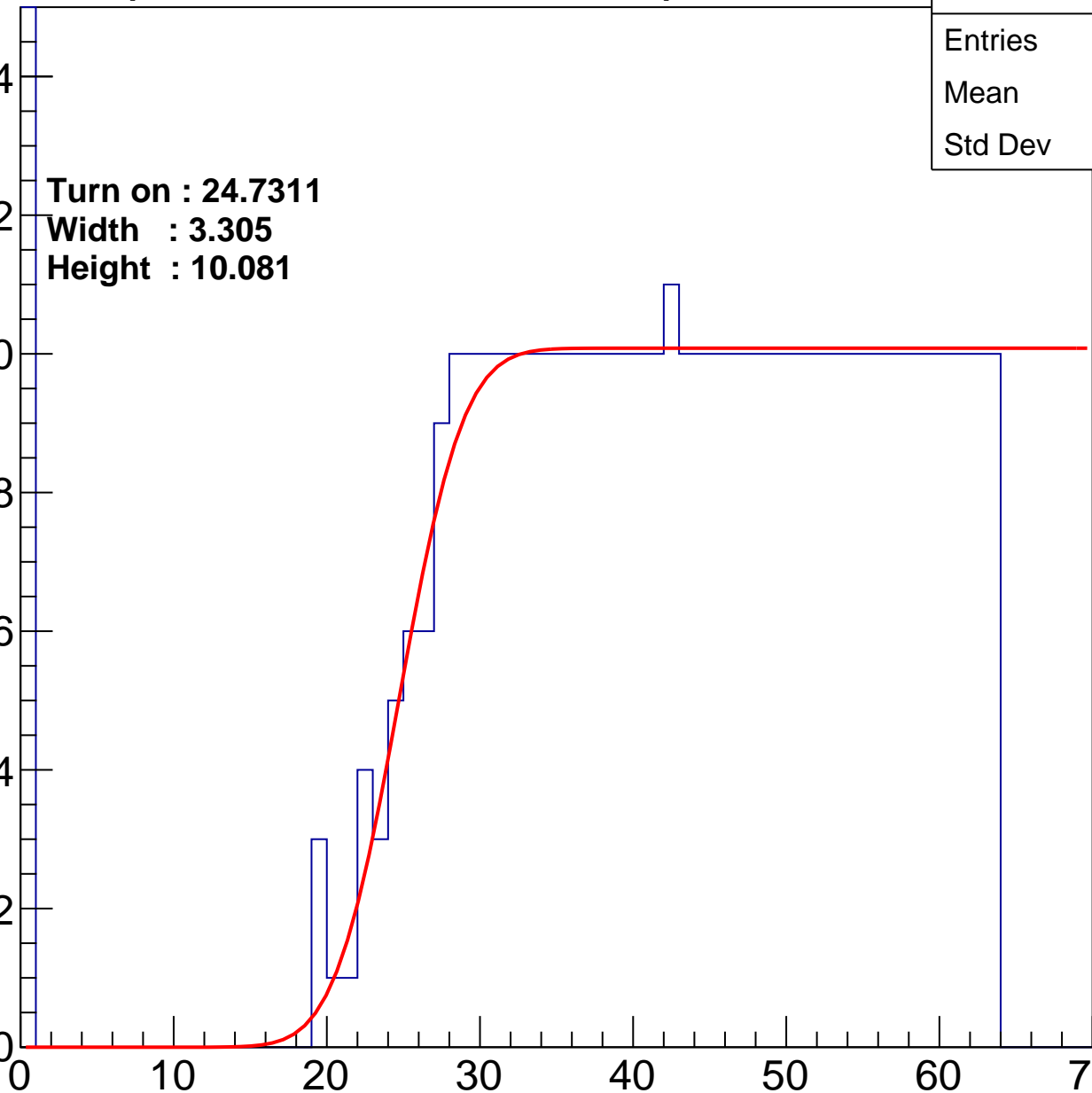
Width : 3.305

Height : 10.081

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch113

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	38.66
Std Dev	17.82

Turn on : 25.9193

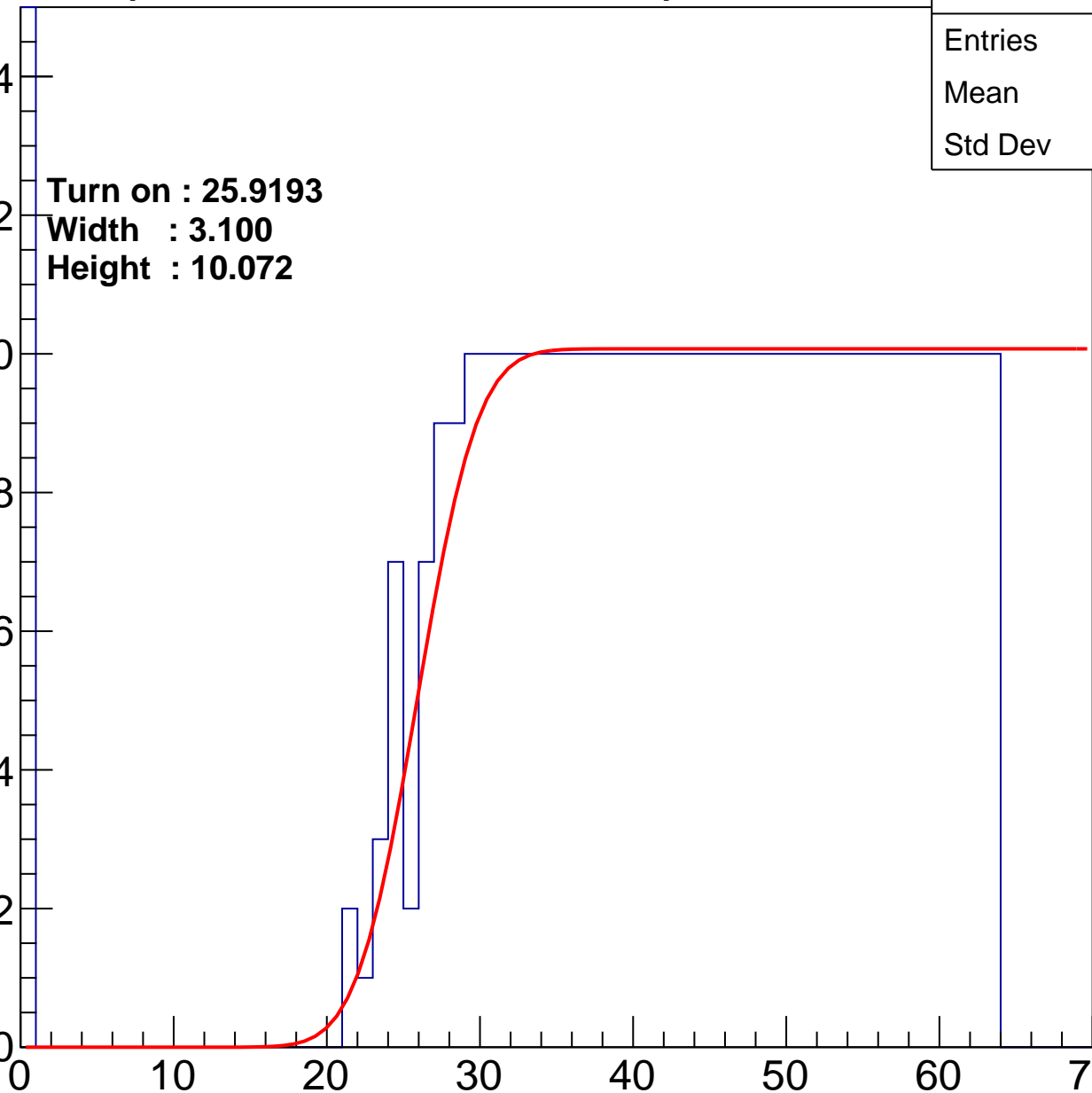
Width : 3.100

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch114

calib_packv5_041523_1651.root, FC#0, port C2

Entries	452
Mean	38.49
Std Dev	17.56

Turn on : 24.1936

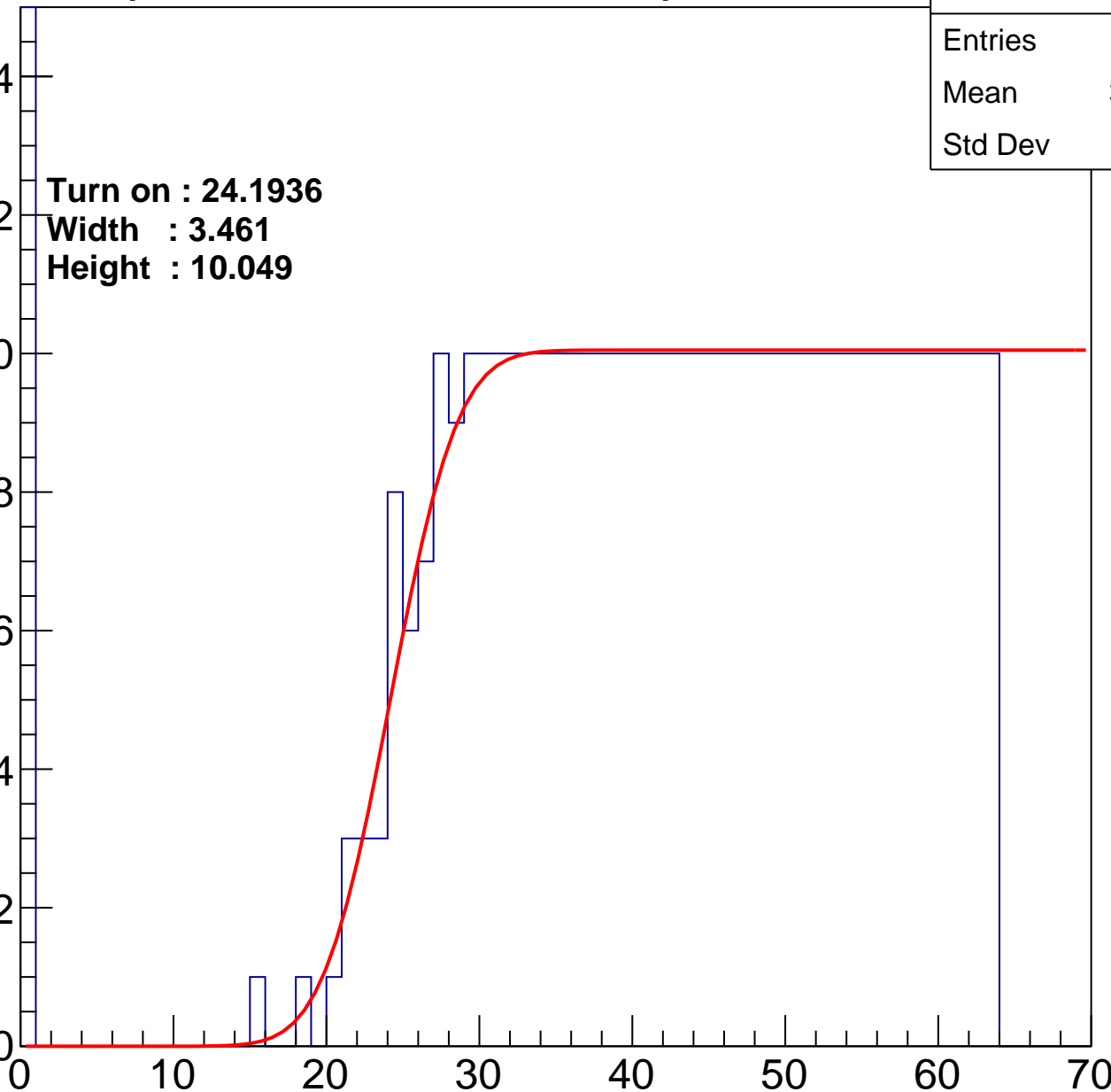
Width : 3.461

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch115

calib_packv5_041523_1651.root, FC#0, port C2

Entries	425
Mean	39.36
Std Dev	17.74

Turn on : 27.0584

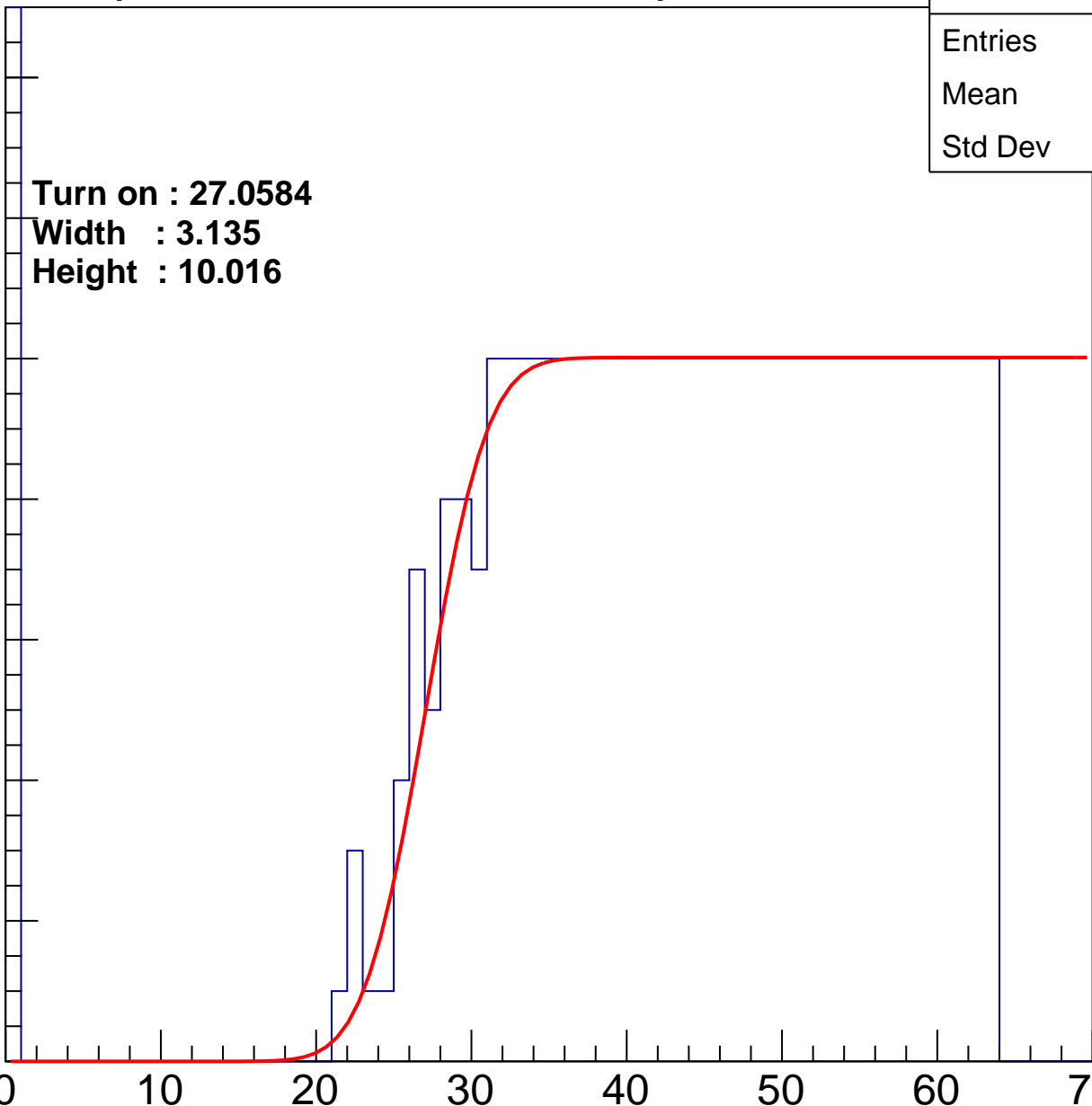
Width : 3.135

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch116

calib_packv5_041523_1651.root, FC#0, port C2

Entries	422
Mean	40.2
Std Dev	16.61

Turn on : 25.7766

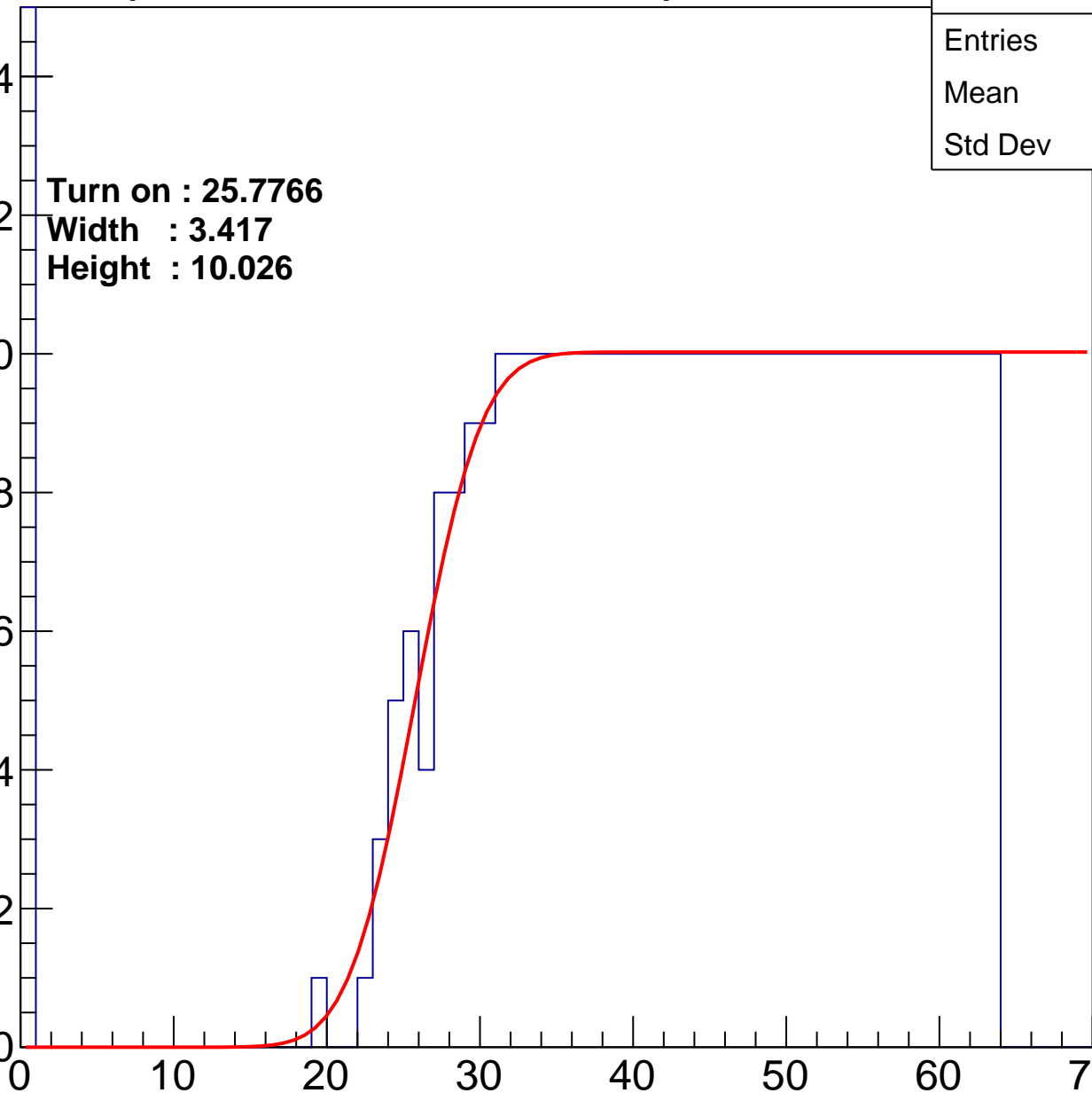
Width : 3.417

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch117

calib_packv5_041523_1651.root, FC#0, port C2

Entries	448
Mean	38.29
Std Dev	18.06

Turn on : 25.3649

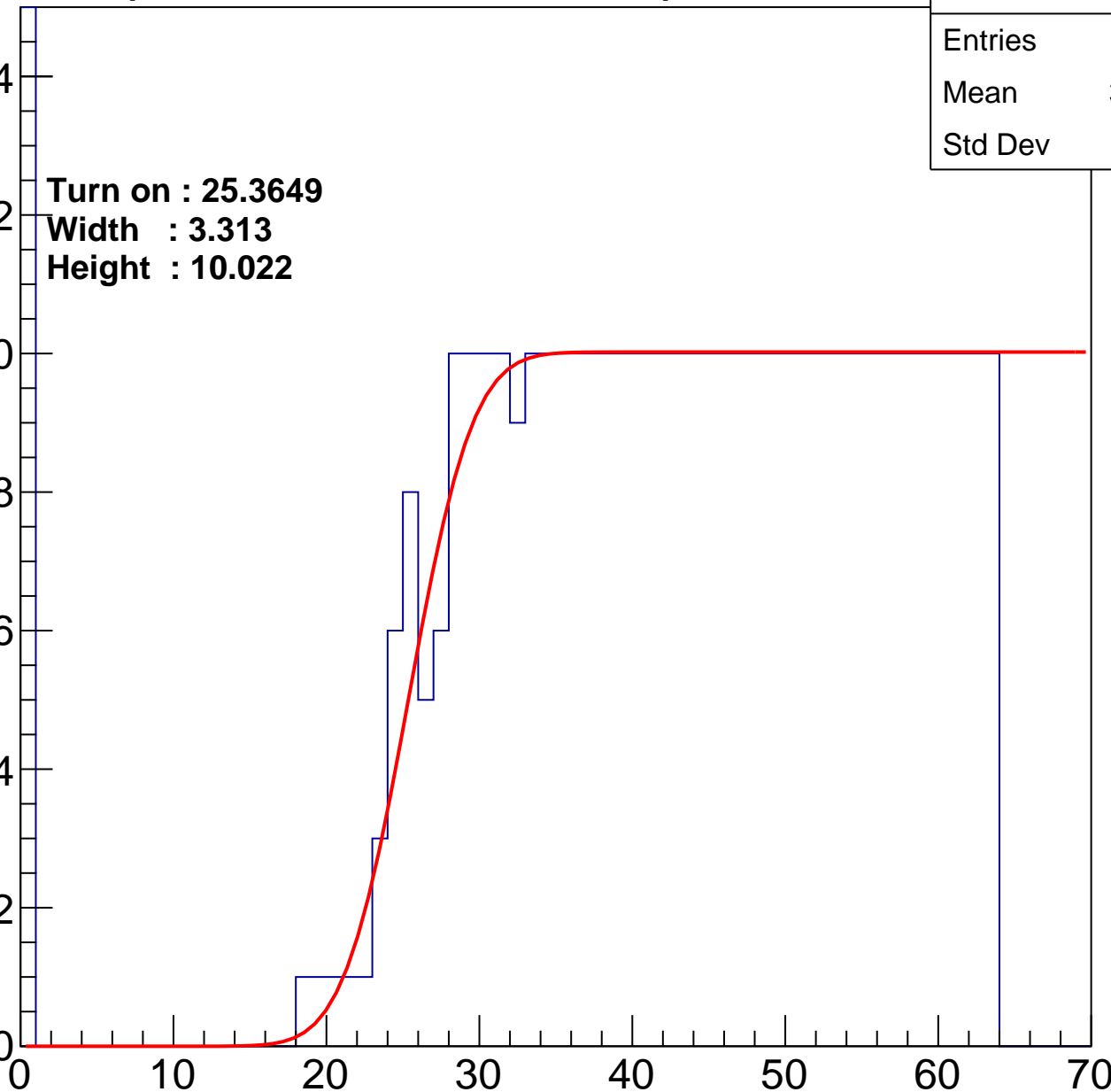
Width : 3.313

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch118

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	40.61
Std Dev	16.12

Turn on : 25.8308

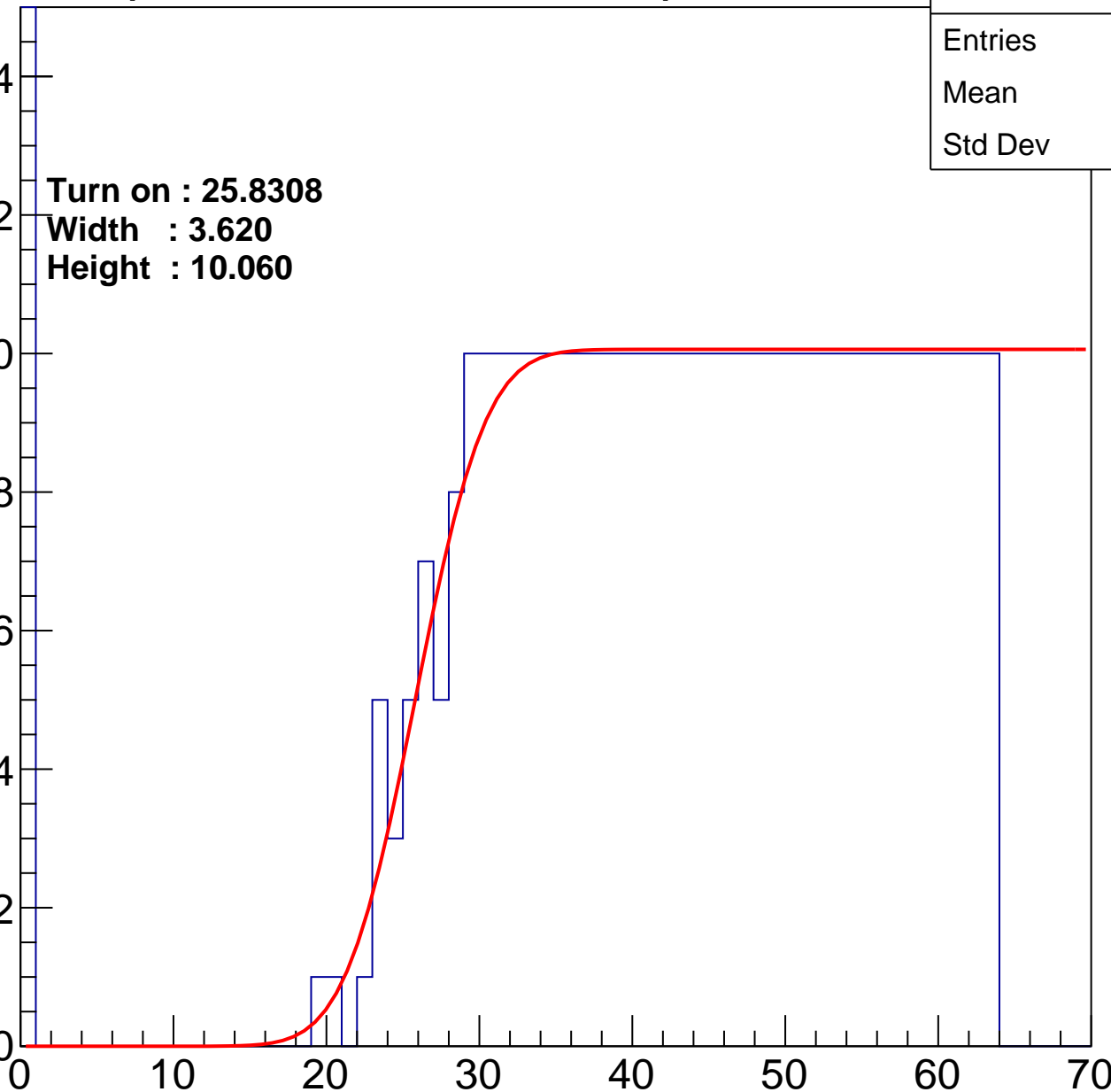
Width : 3.620

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch119

calib_packv5_041523_1651.root, FC#0, port C2

Entries	417
Mean	40.61
Std Dev	16.28

Turn on : 25.9626

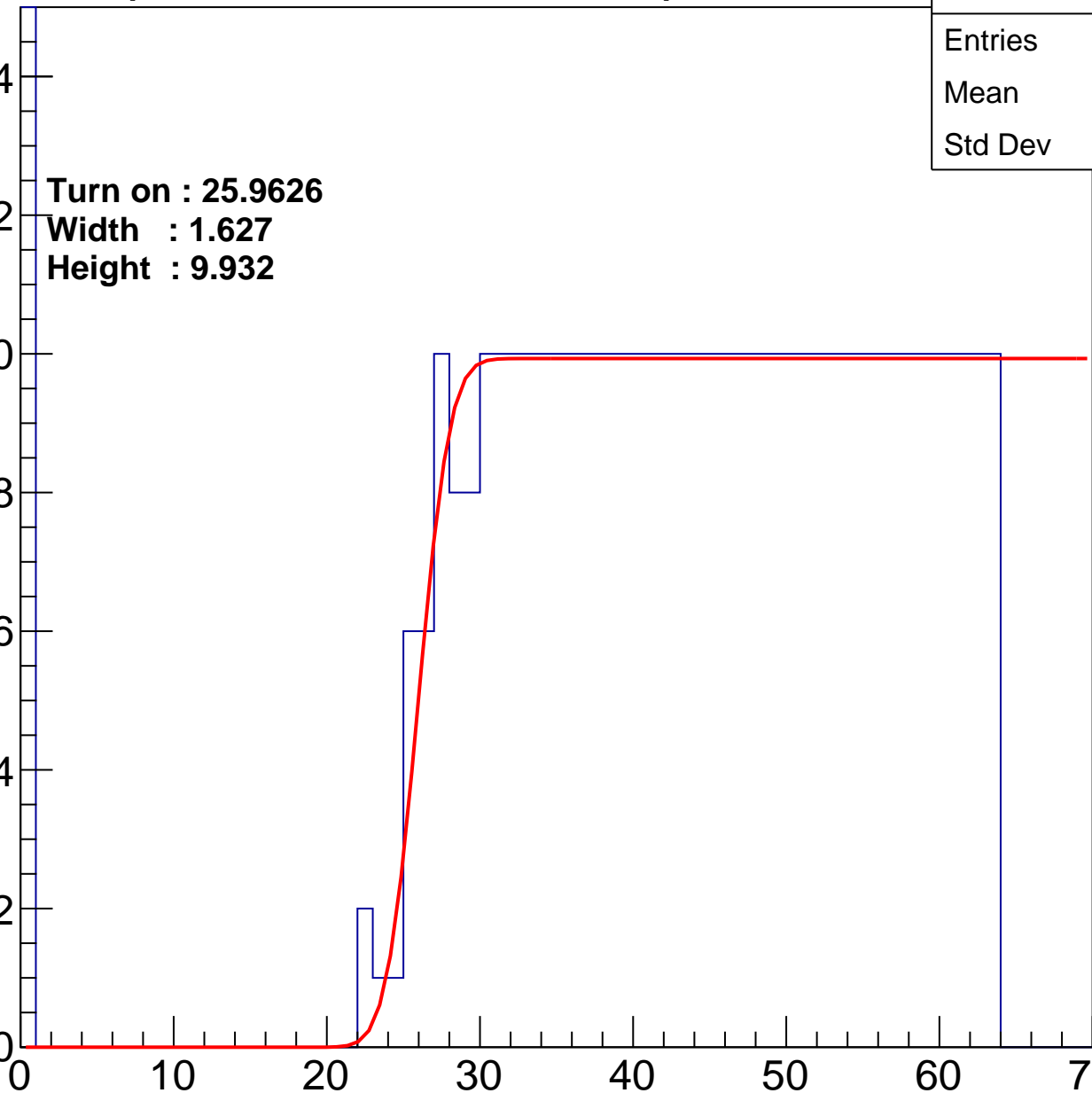
Width : 1.627

Height : 9.932

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch120

calib_packv5_041523_1651.root, FC#0, port C2

Entries	452
Mean	38.01
Std Dev	18.23

Turn on : 25.3604

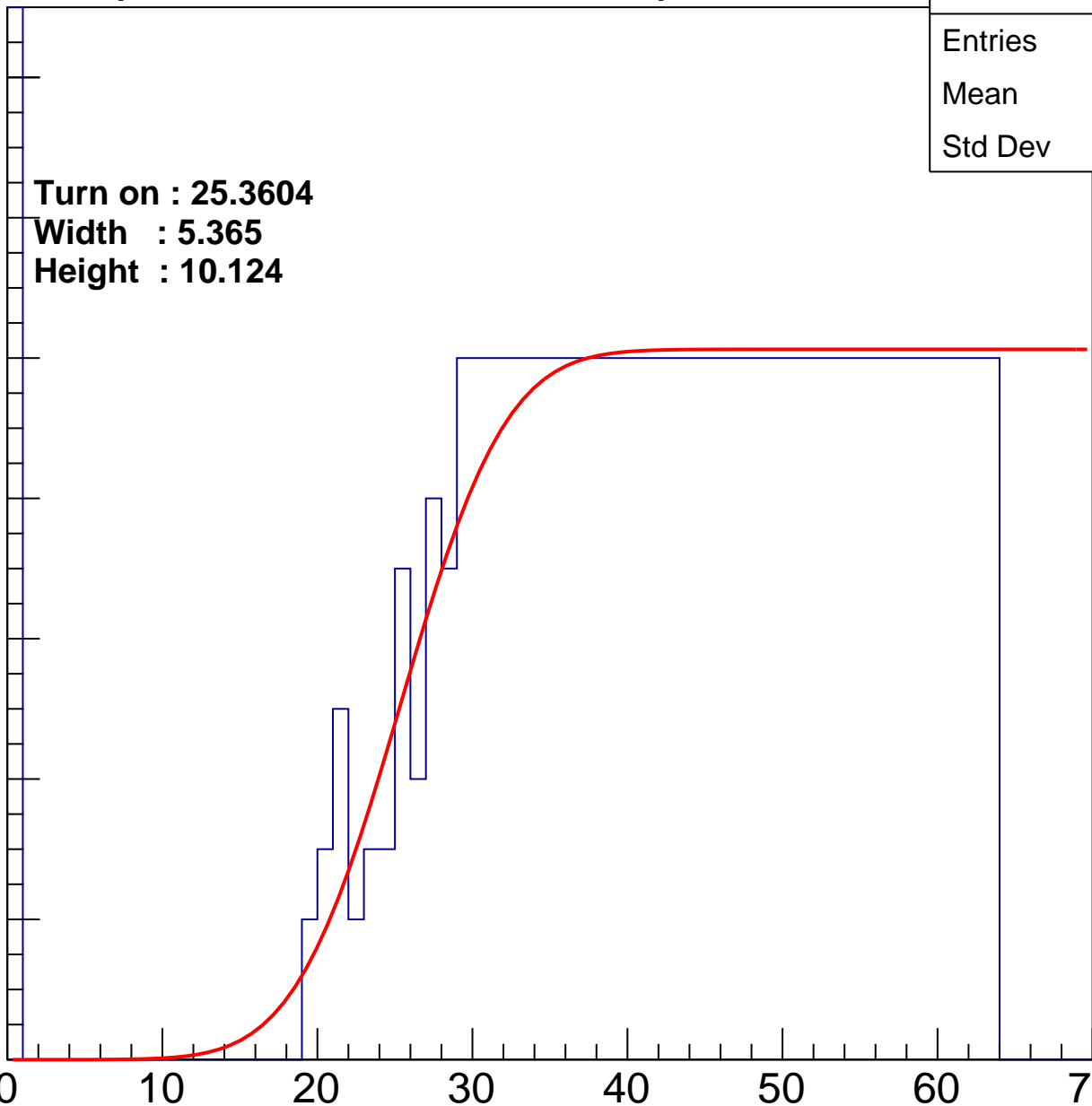
Width : 5.365

Height : 10.124

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch121

calib_packv5_041523_1651.root, FC#0, port C2

Entries	425
Mean	40.09
Std Dev	16.65

Turn on : 25.6385

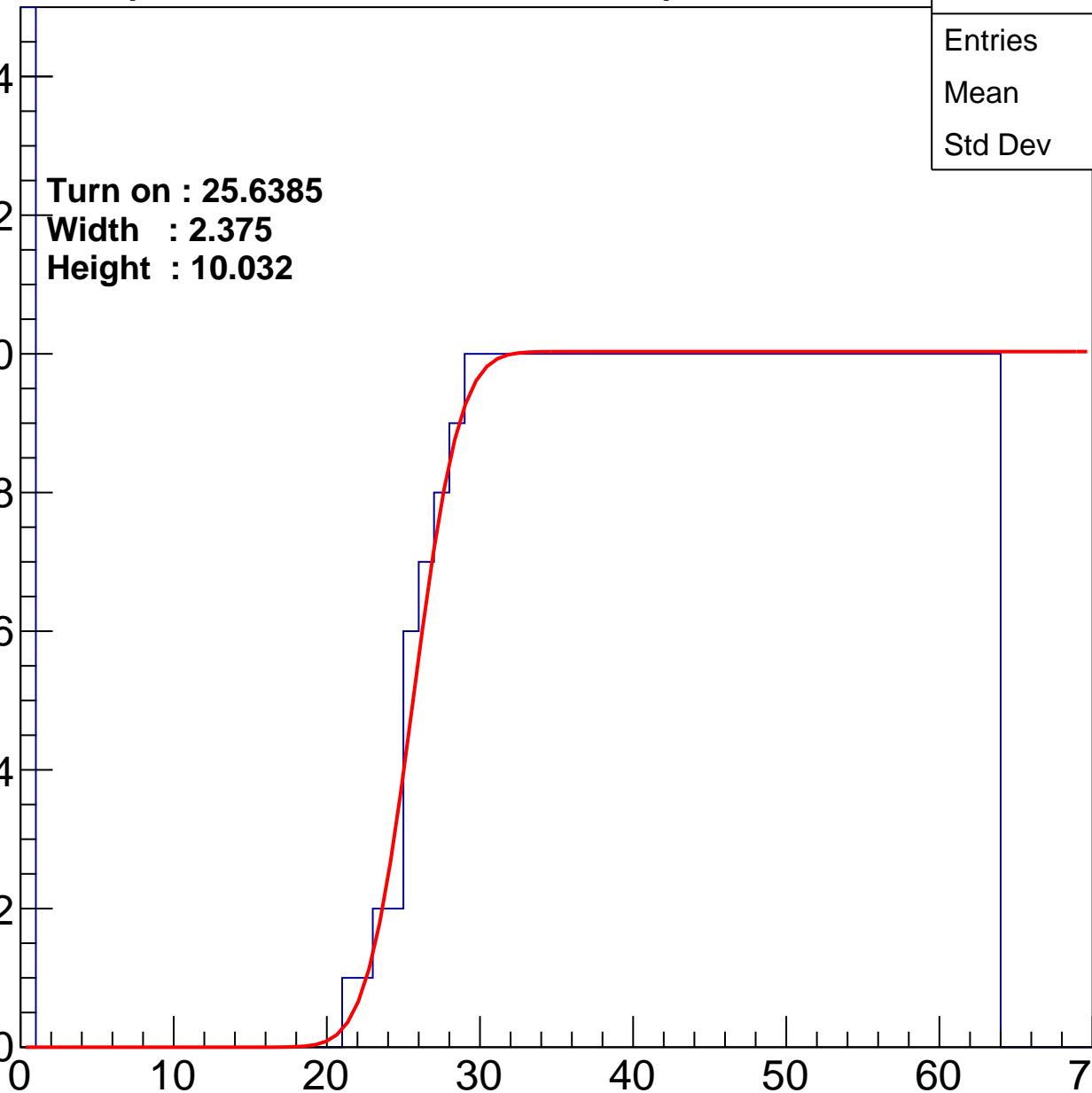
Width : 2.375

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch122

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	39.49
Std Dev	16.96

Turn on : 24.9536

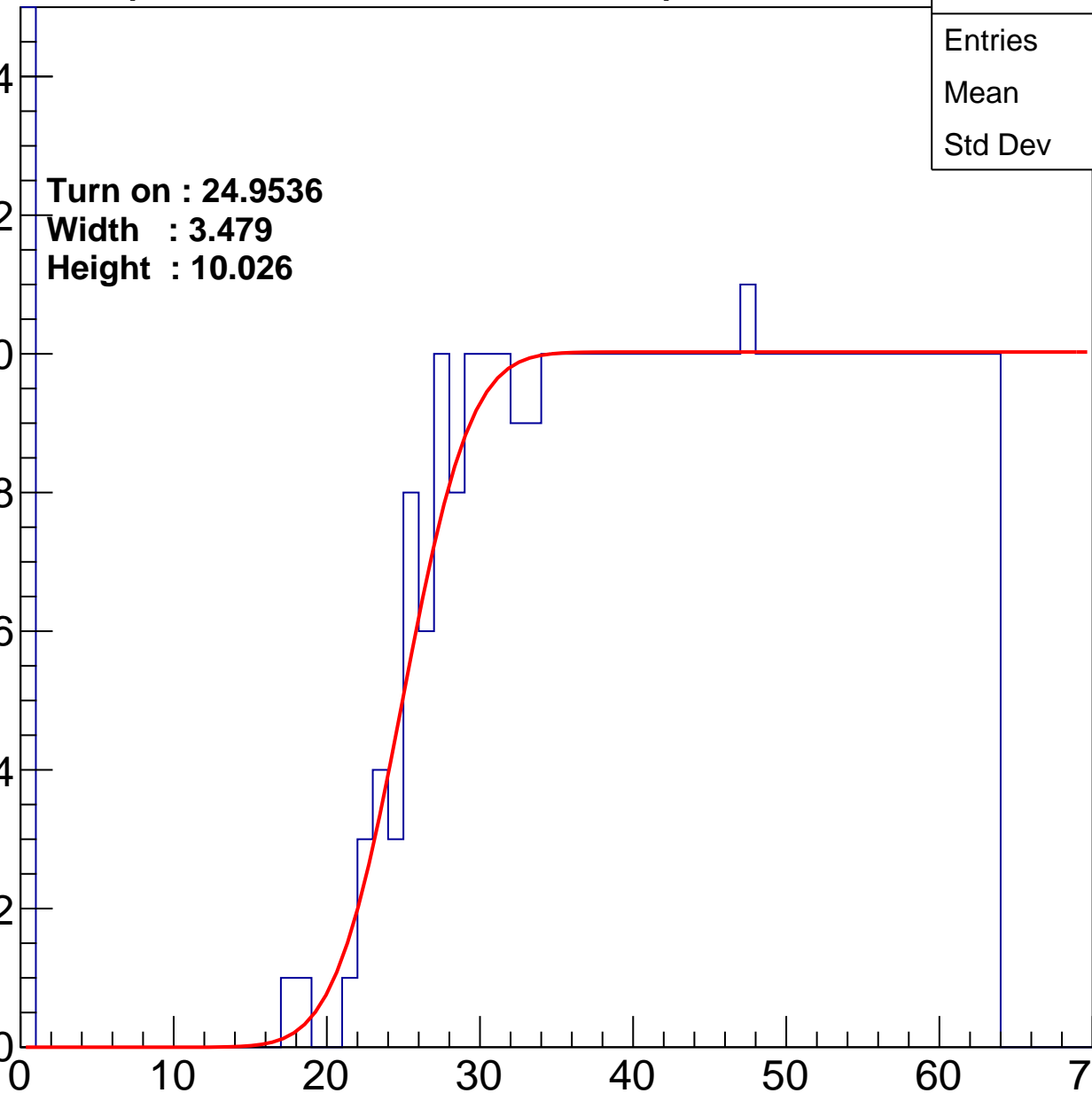
Width : 3.479

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch123

calib_packv5_041523_1651.root, FC#0, port C2

Entries	415
Mean	39.7
Std Dev	17.81

Turn on : 27.6090

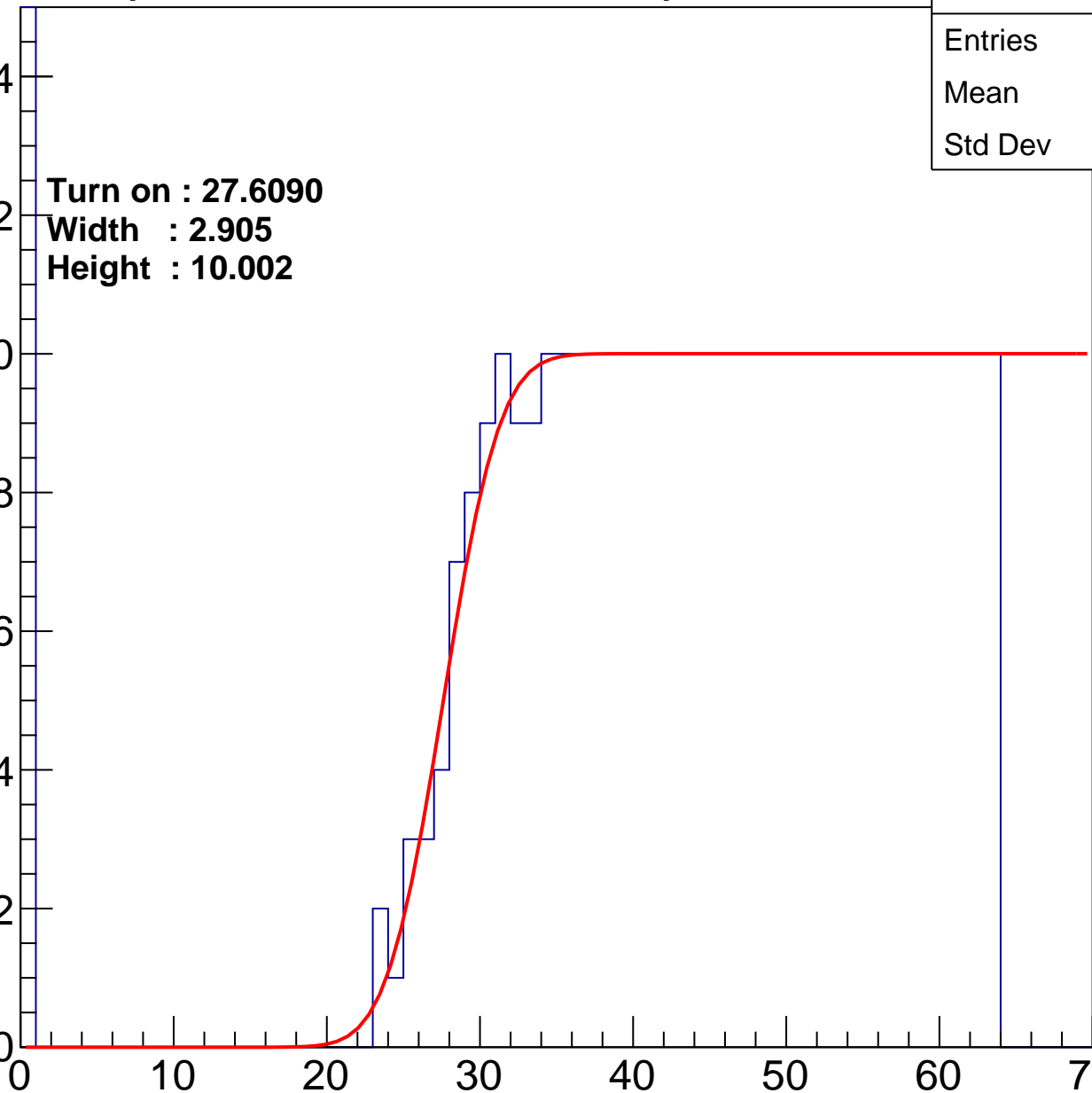
Width : 2.905

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch124

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.36
Std Dev	17.6

Turn on : 26.4000

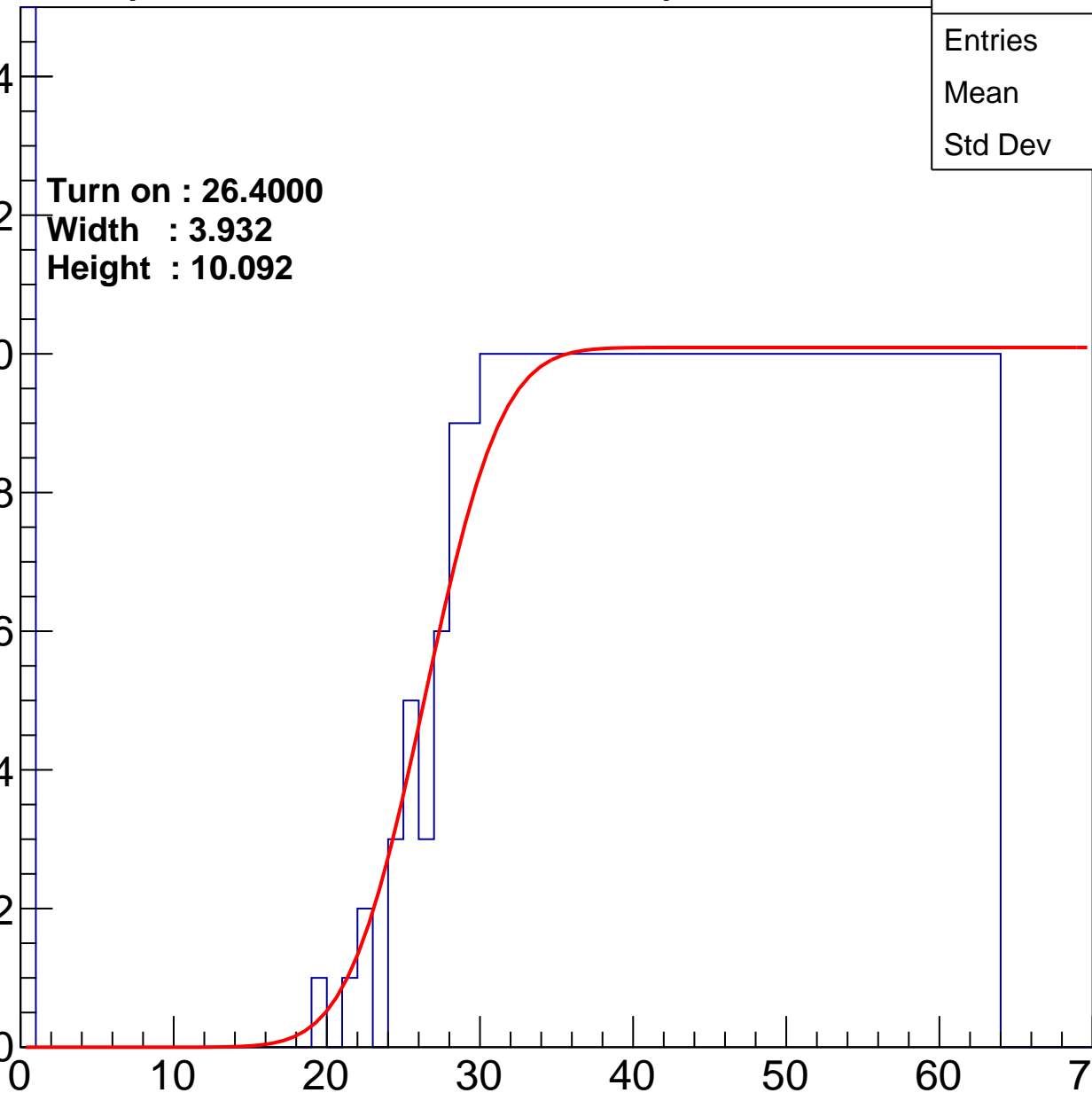
Width : 3.932

Height : 10.092

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch125

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	39.76
Std Dev	17.19

Turn on : 26.0674

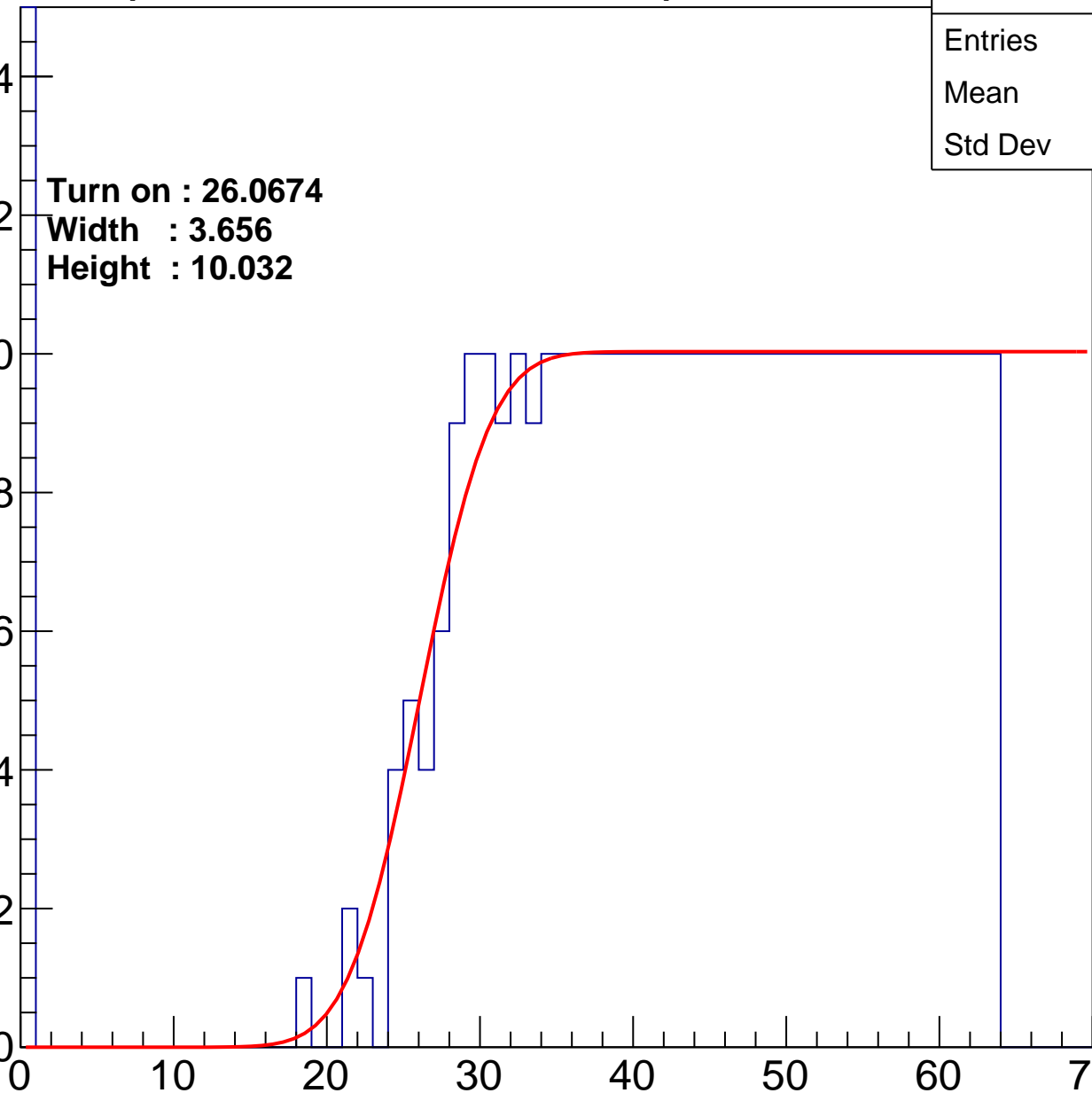
Width : 3.656

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch126

calib_packv5_041523_1651.root, FC#0, port C2

Entries	460
Mean	38.27
Std Dev	17.45

Turn on : 22.8872

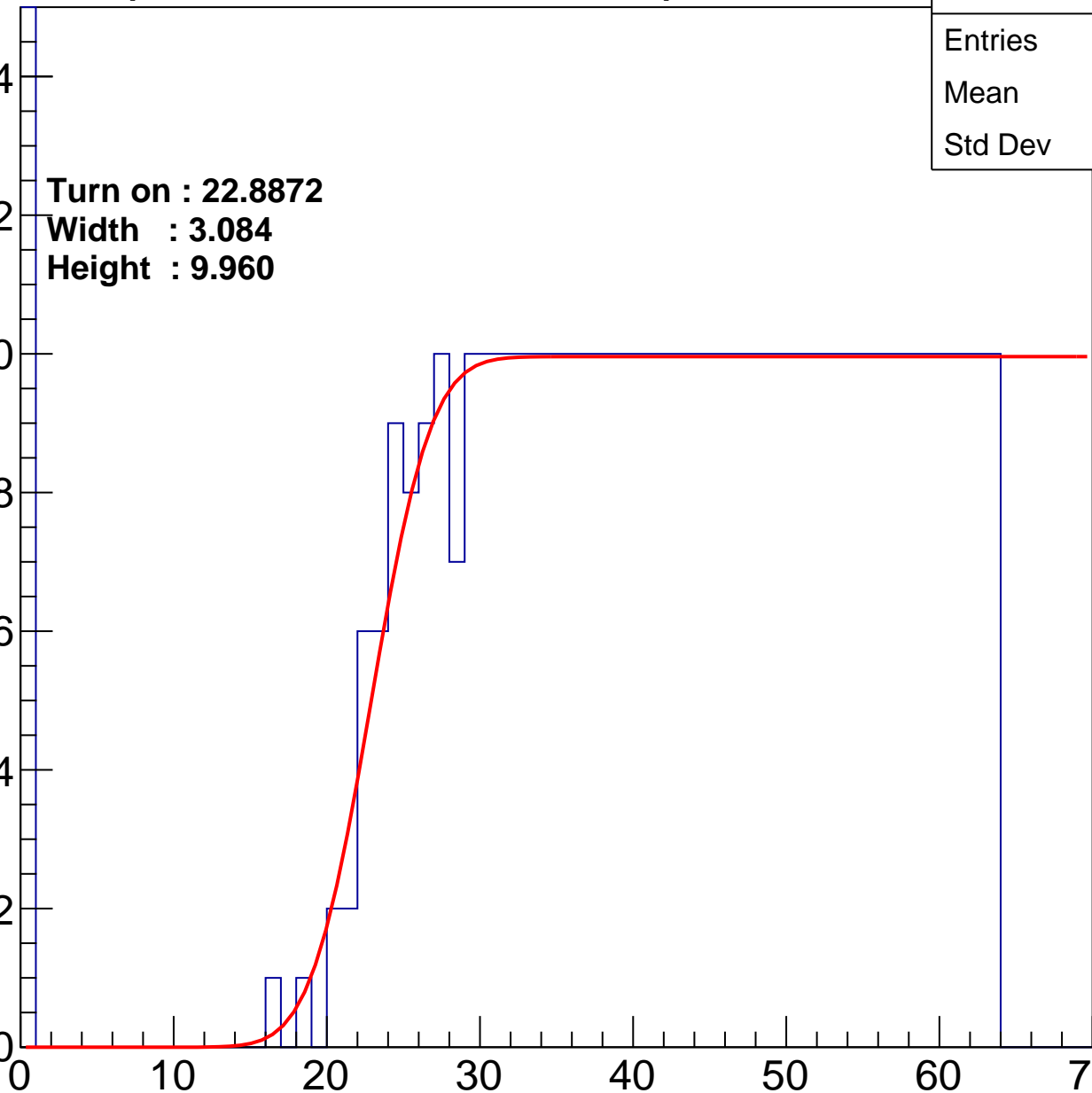
Width : 3.084

Height : 9.960

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch127

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.39
Std Dev	17.45

Turn on : 25.9792

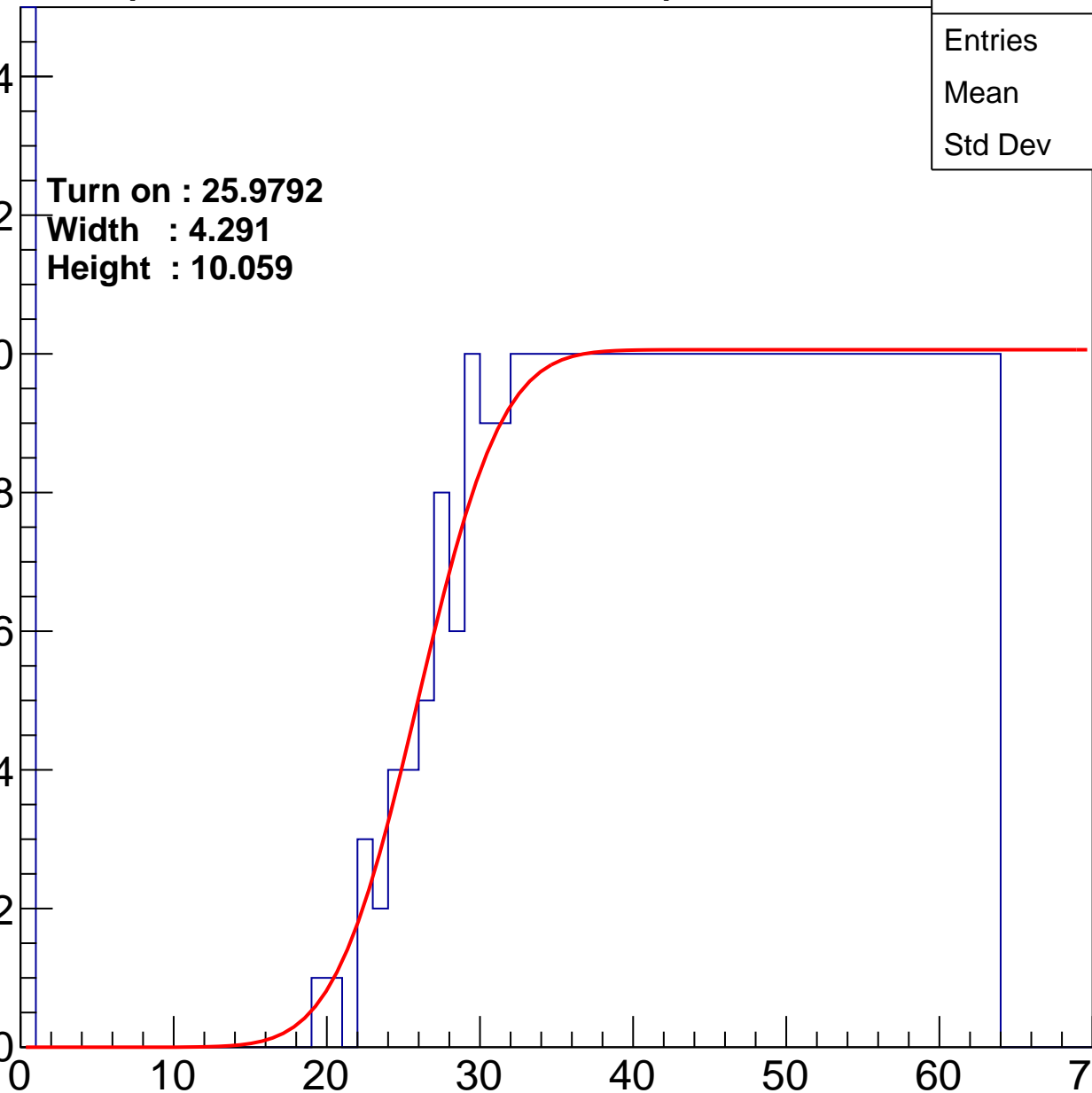
Width : 4.291

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U8-ch127

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.39
Std Dev	17.45

Turn on : 25.9792

Width : 4.291

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl

