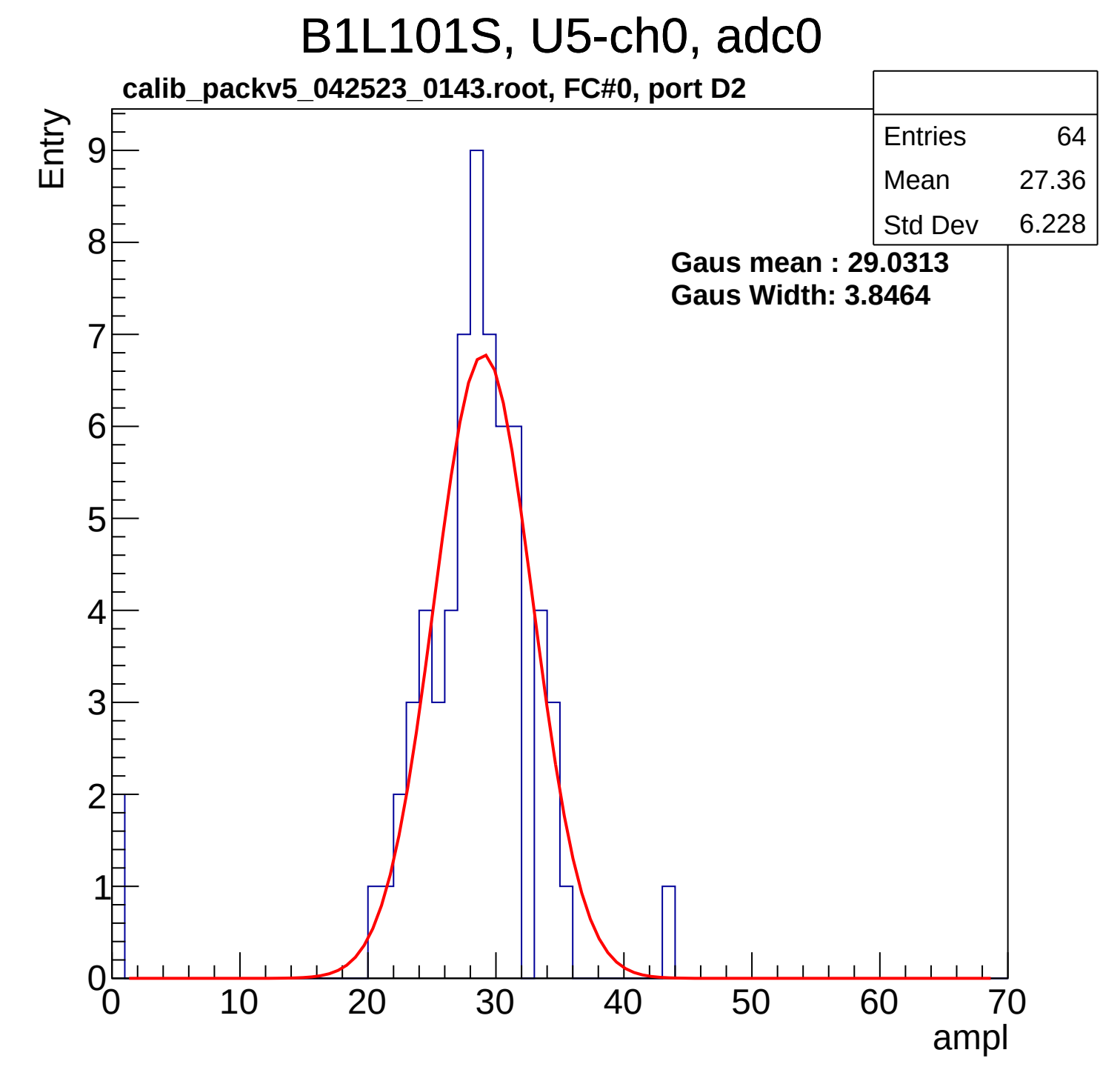
B1L101S, U5-ch0, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 27.36
Std Dev 6.228
Gaus mean : 29.0313
Gaus Width: 3.8464
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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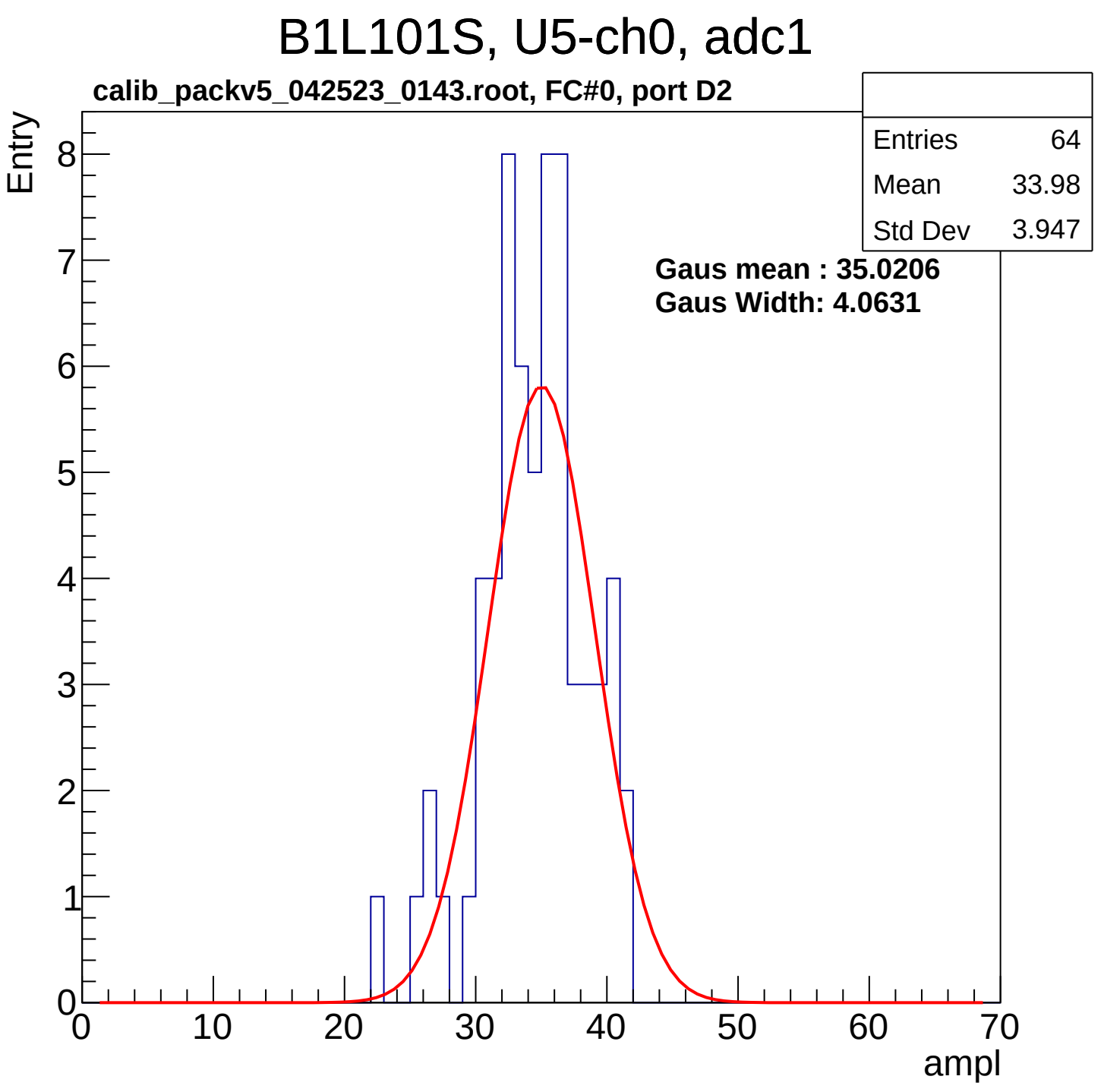
B1L101S, U5-ch0, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 33.98
Std Dev 3.947
Gaus mean : 35.0206
Gaus Width: 4.0631
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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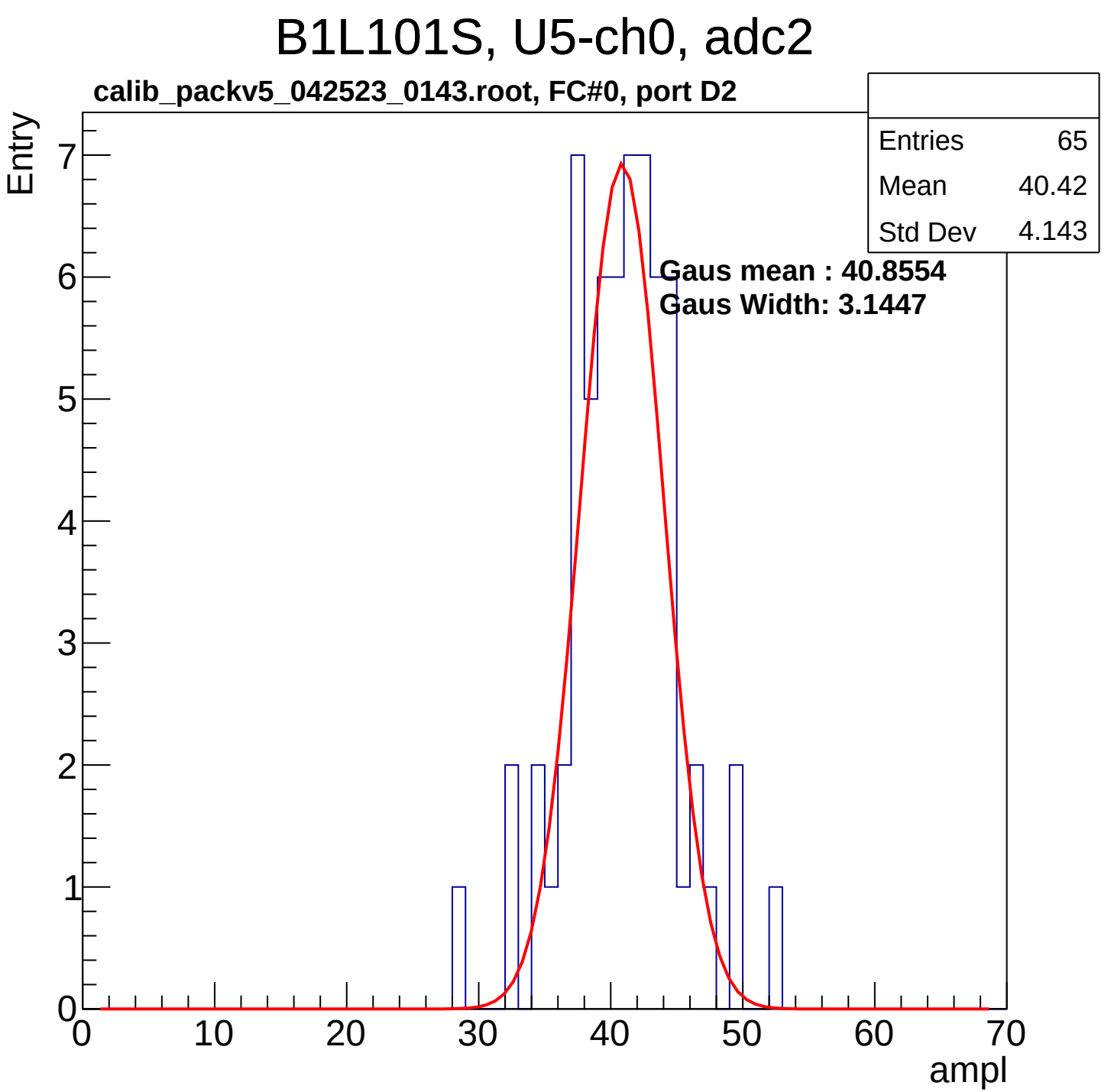
B1L101S, U5-ch0, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 40.42
Std Dev 4.143
Gaus mean : 40.8554
Gaus Width: 3.1447
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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60
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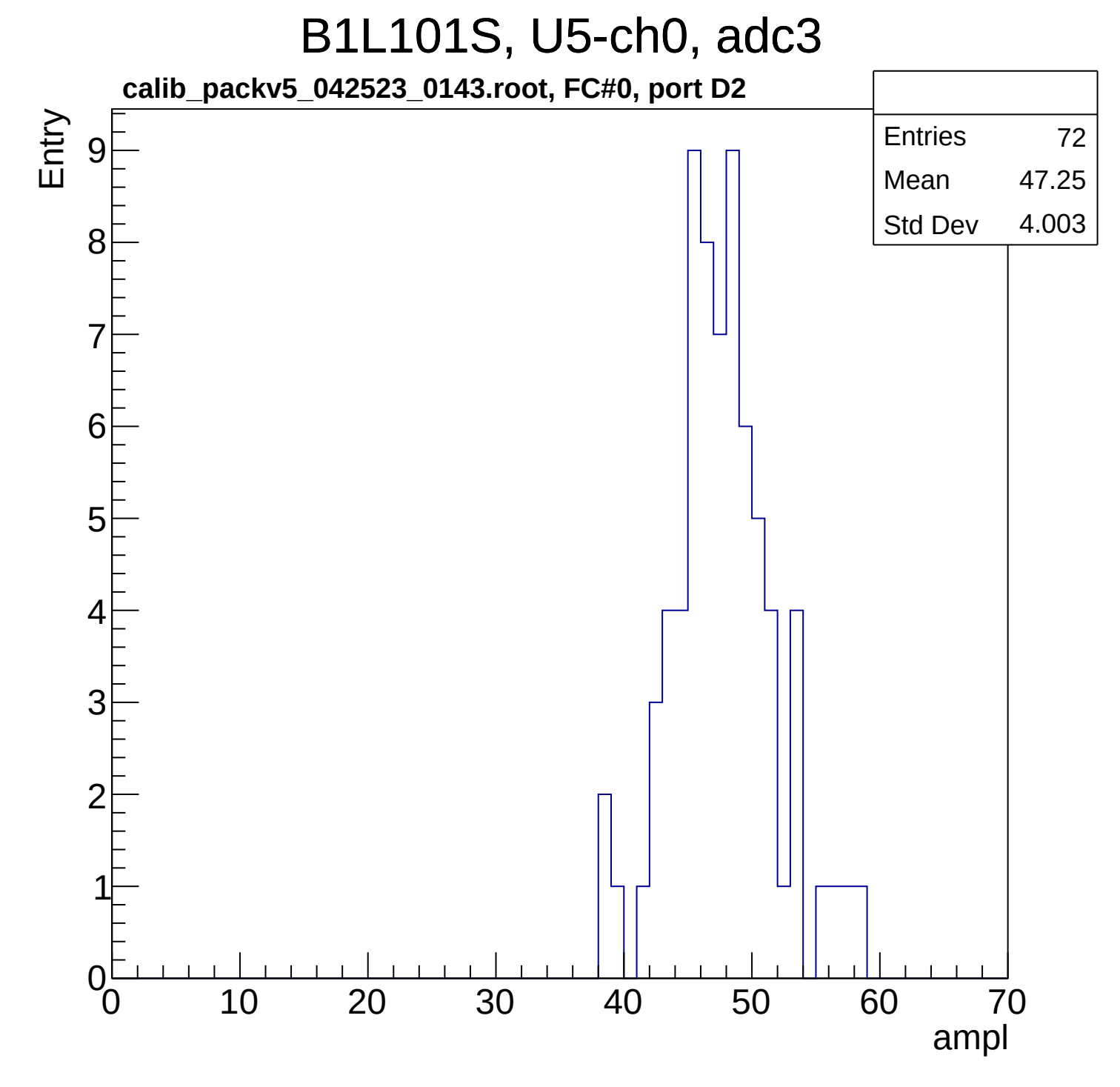
B1L101S, U5-ch0, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 47.25
Std Dev 4.003
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
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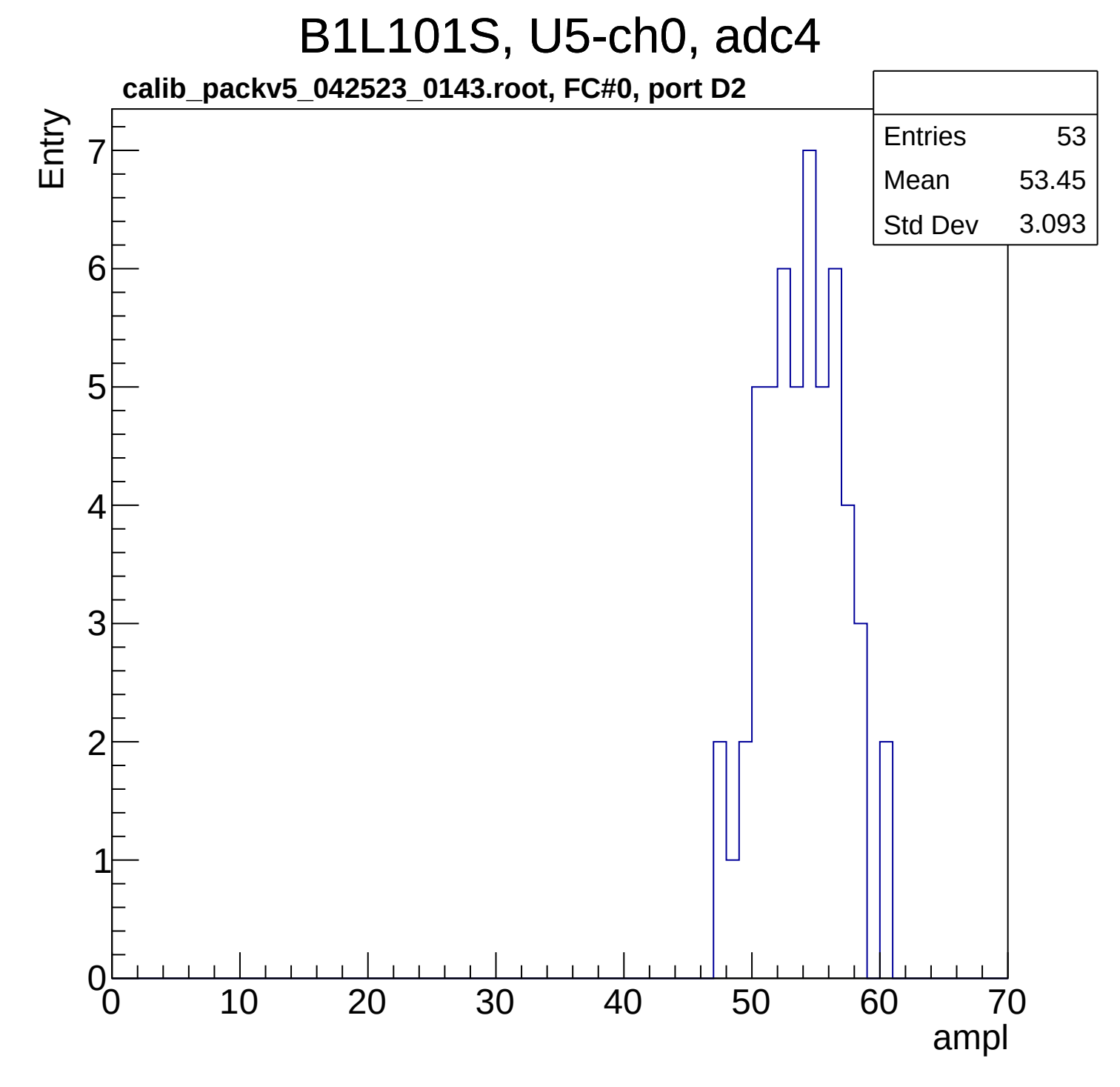
B1L101S, U5-ch0, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 53.45
Std Dev 3.093
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
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60
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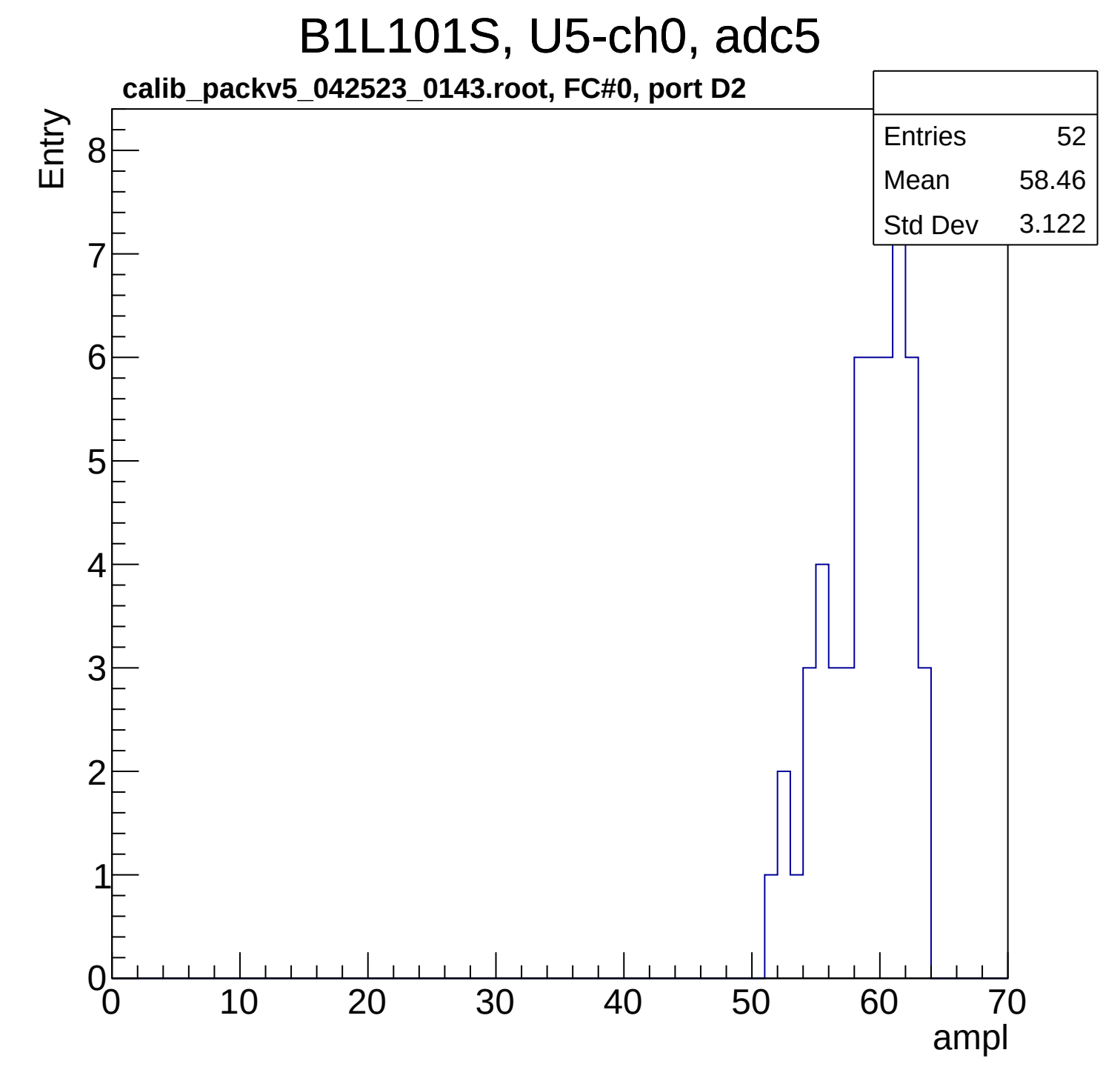
B1L101S, U5-ch0, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 58.46
Std Dev 3.122
Entry
ampl
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1
2
3
4
5
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7
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0
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60
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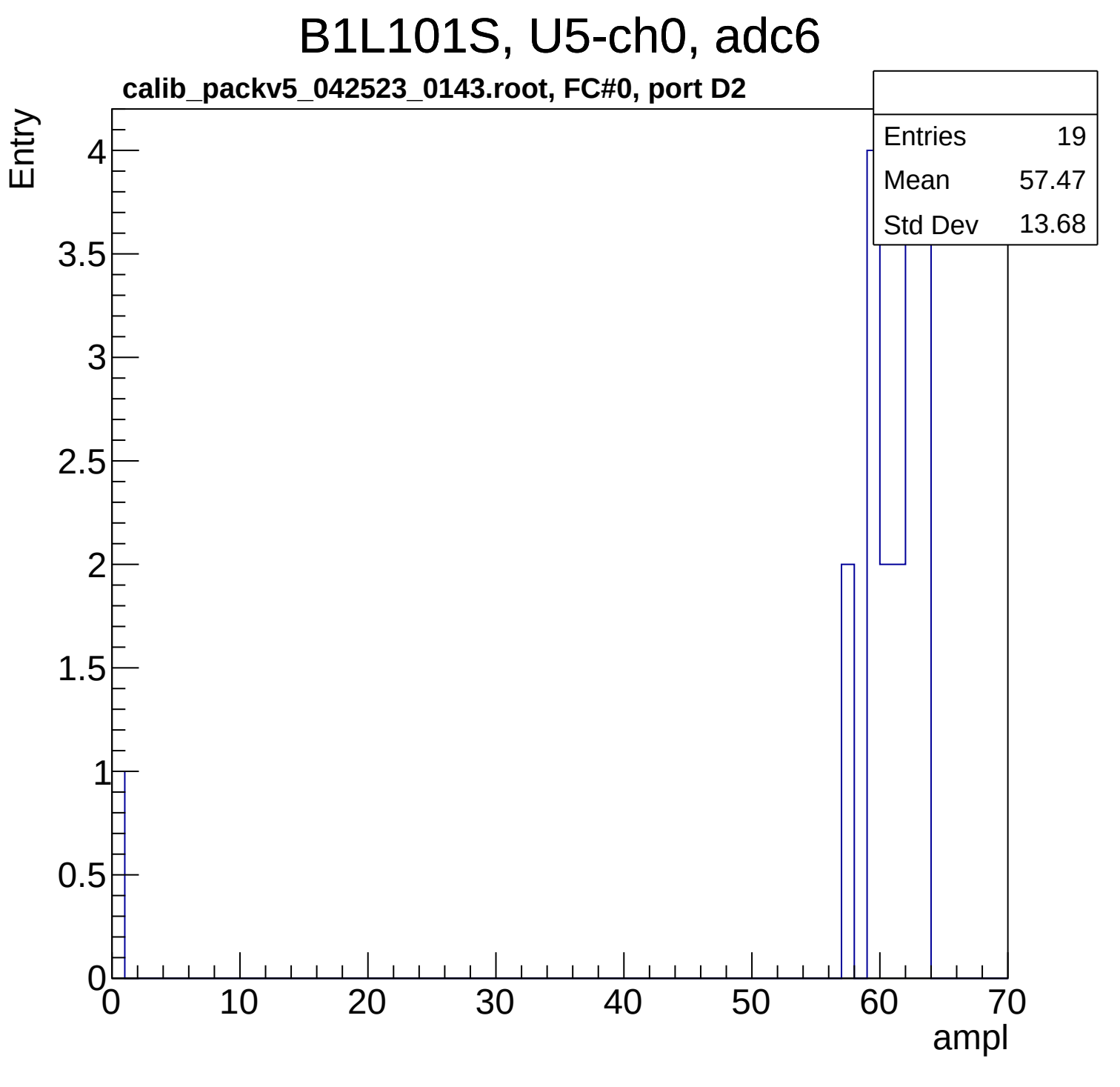
B1L101S, U5-ch0, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 19
Mean 57.47
Std Dev 13.68
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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60
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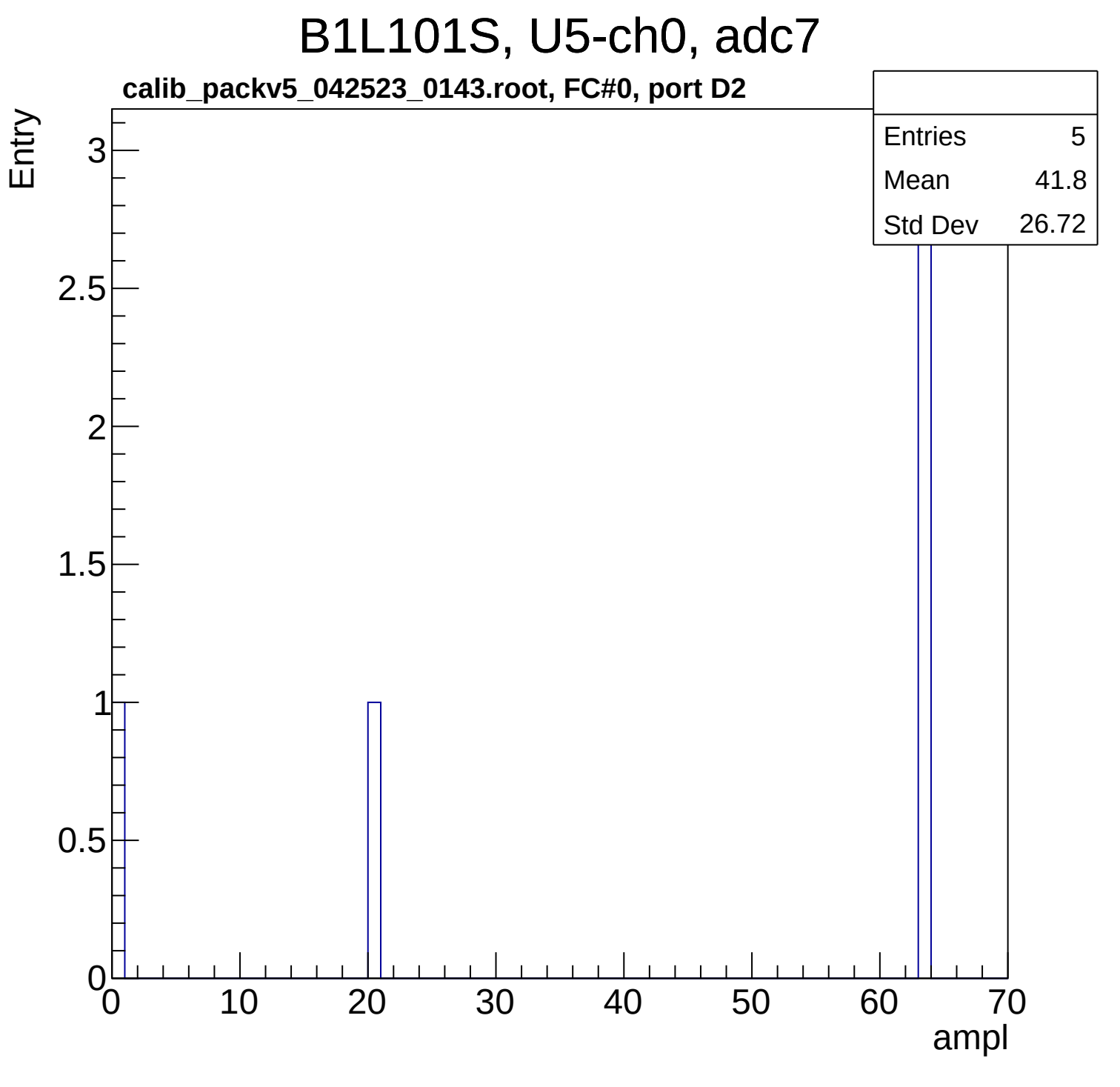
B1L101S, U5-ch0, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 41.8
Std Dev 26.72
Entry
ampl
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1.5
2
2.5
3
0
10
20
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40
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60
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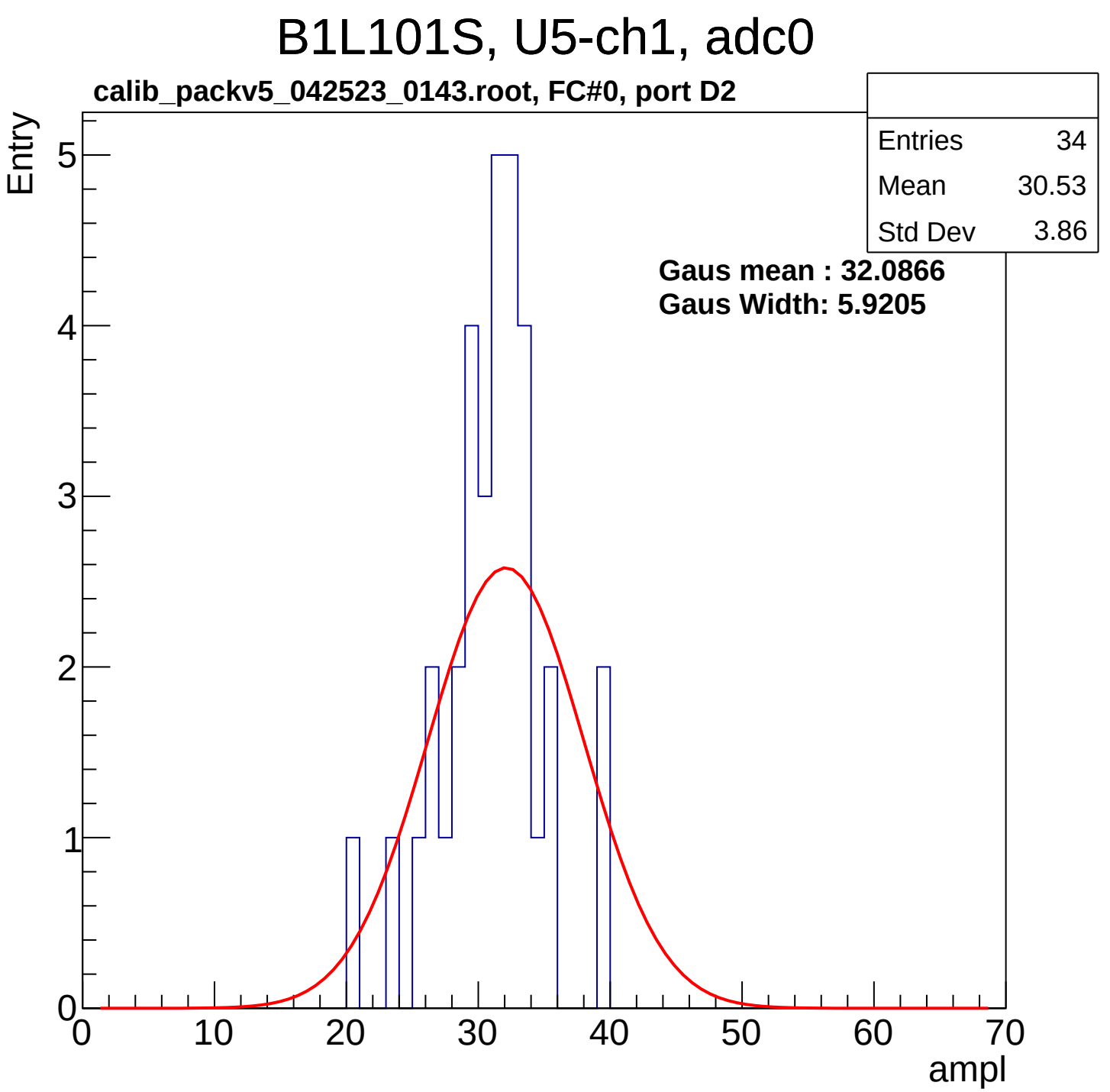
B1L101S, U5-ch1, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 34
Mean 30.53
Std Dev 3.86
Gaus mean : 32.0866
Gaus Width: 5.9205
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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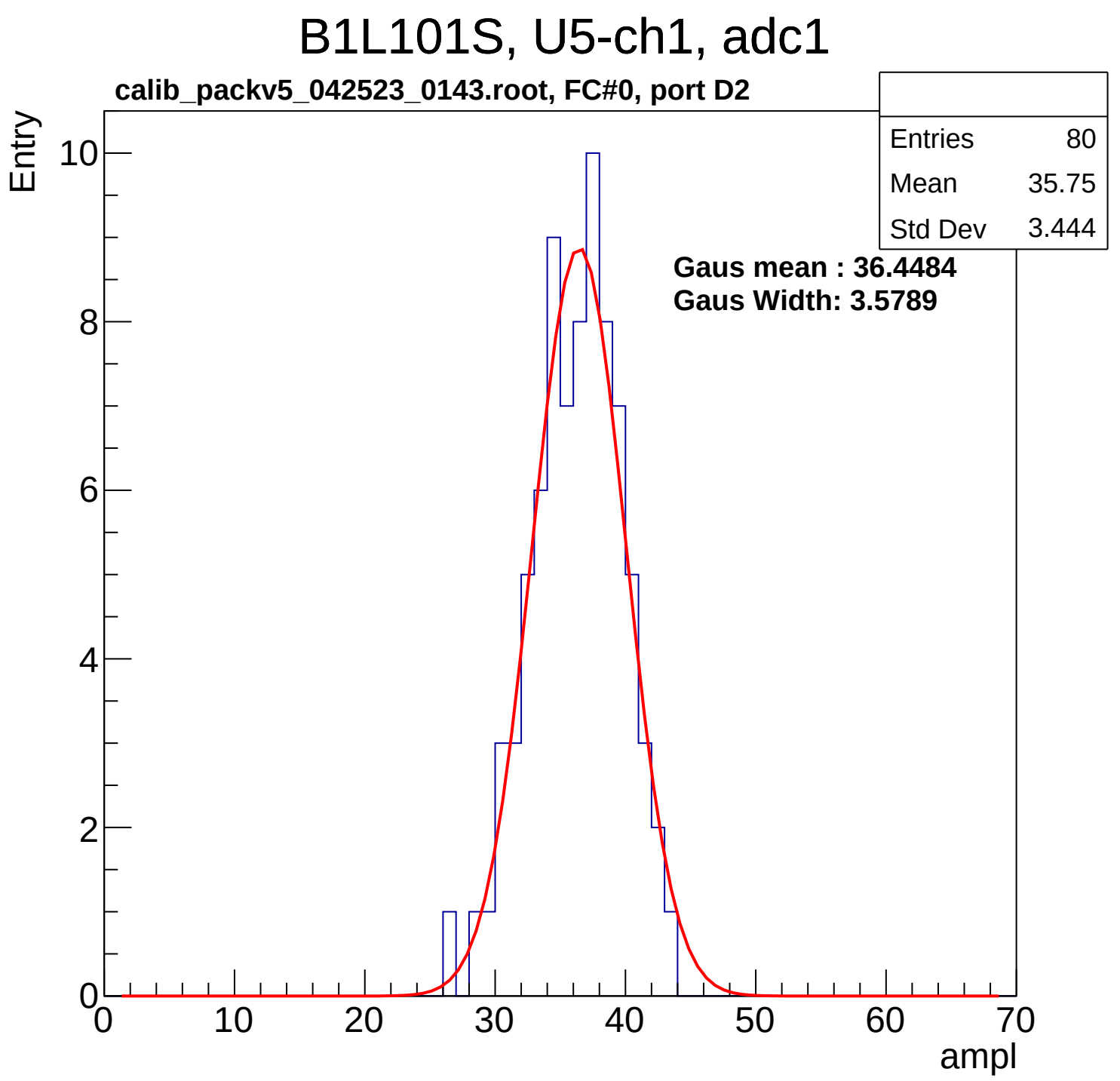
B1L101S, U5-ch1, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 80
Mean 35.75
Std Dev 3.444
Gaus mean : 36.4484
Gaus Width: 3.5789
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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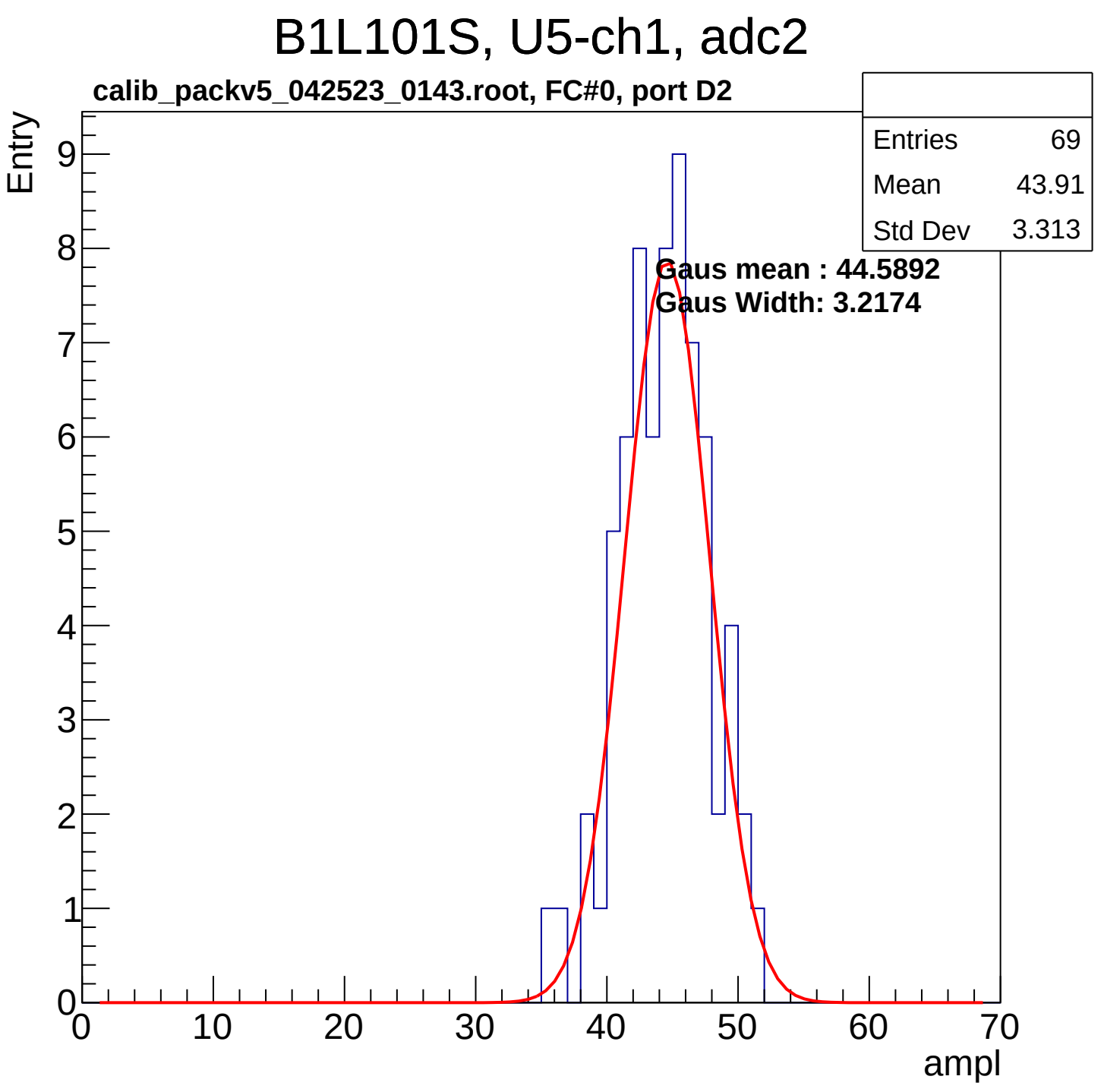
B1L101S, U5-ch1, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 43.91
Std Dev 3.313
Gaus mean : 44.5892
Gaus Width: 3.2174
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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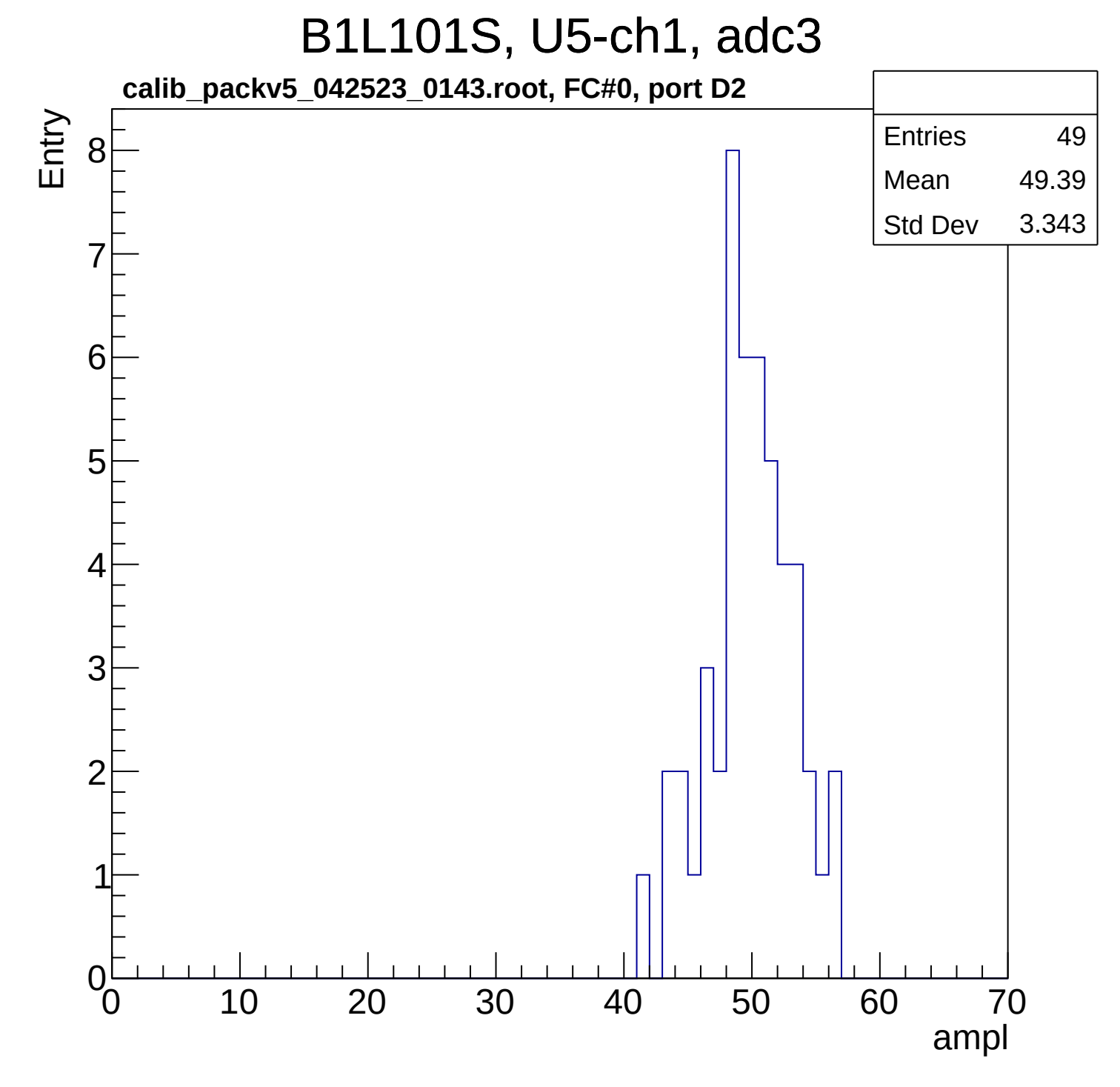
B1L101S, U5-ch1, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 49.39
Std Dev 3.343
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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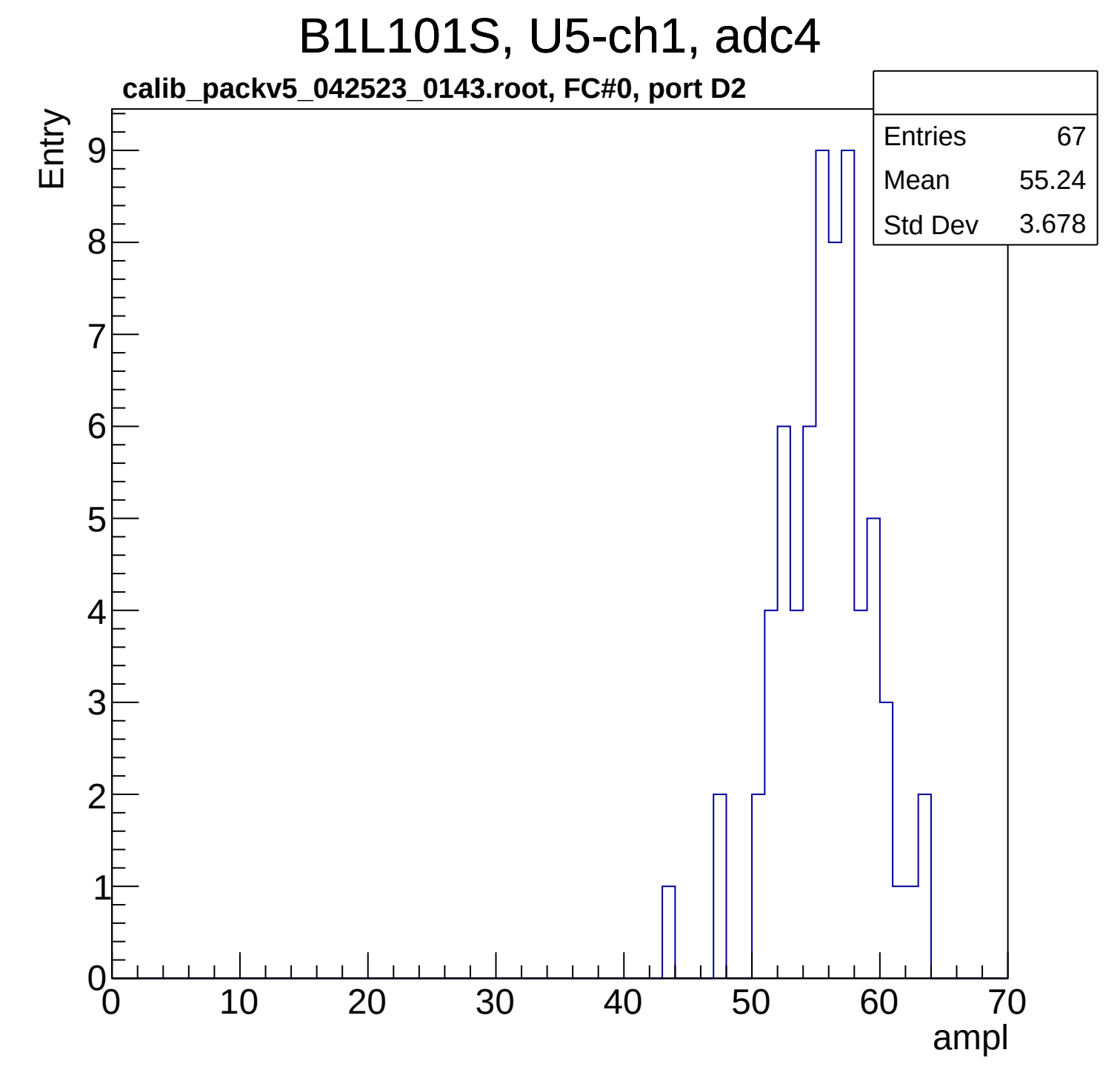
B1L101S, U5-ch1, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 55.24
Std Dev 3.678
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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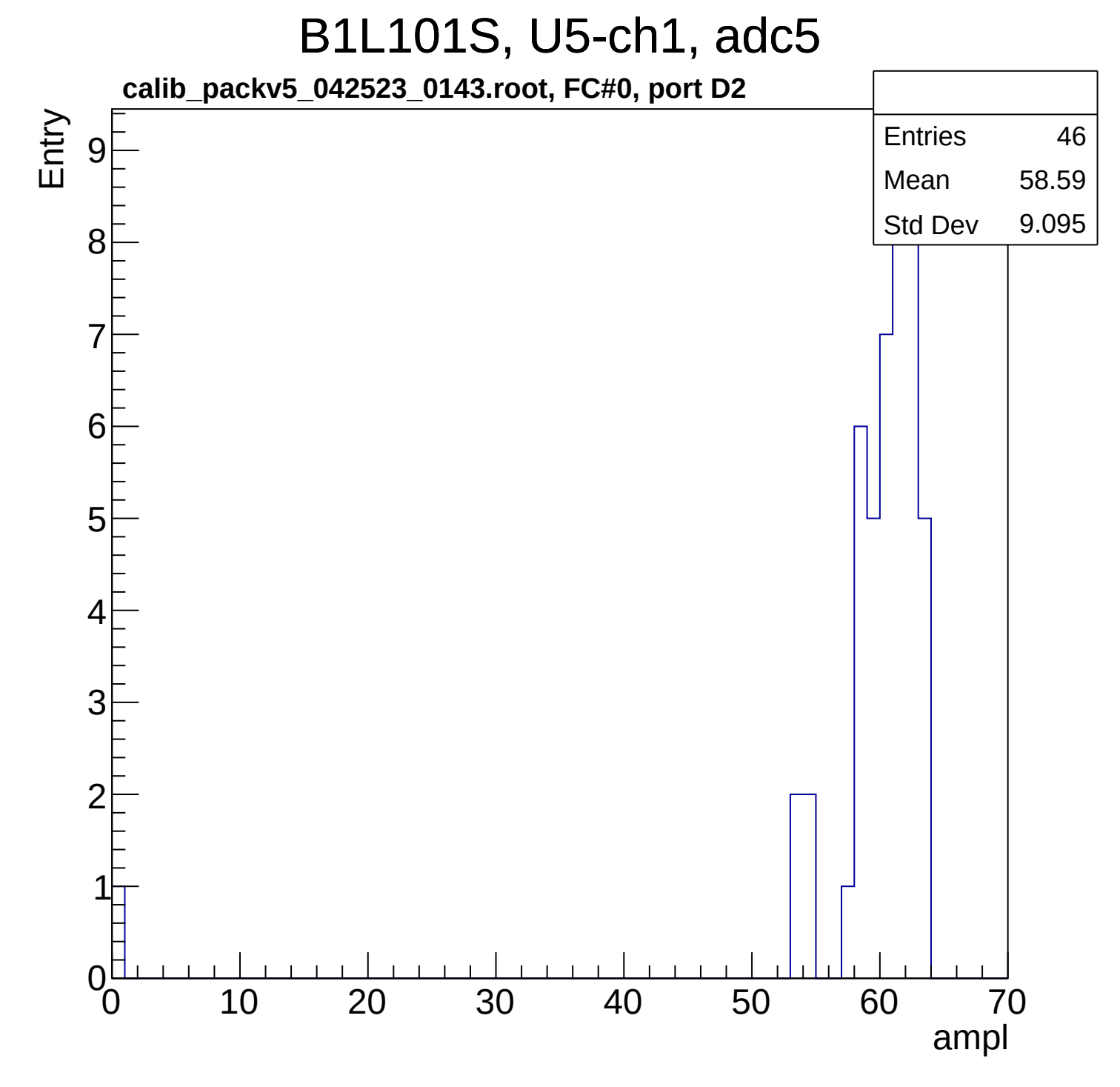
B1L101S, U5-ch1, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 58.59
Std Dev 9.095
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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60
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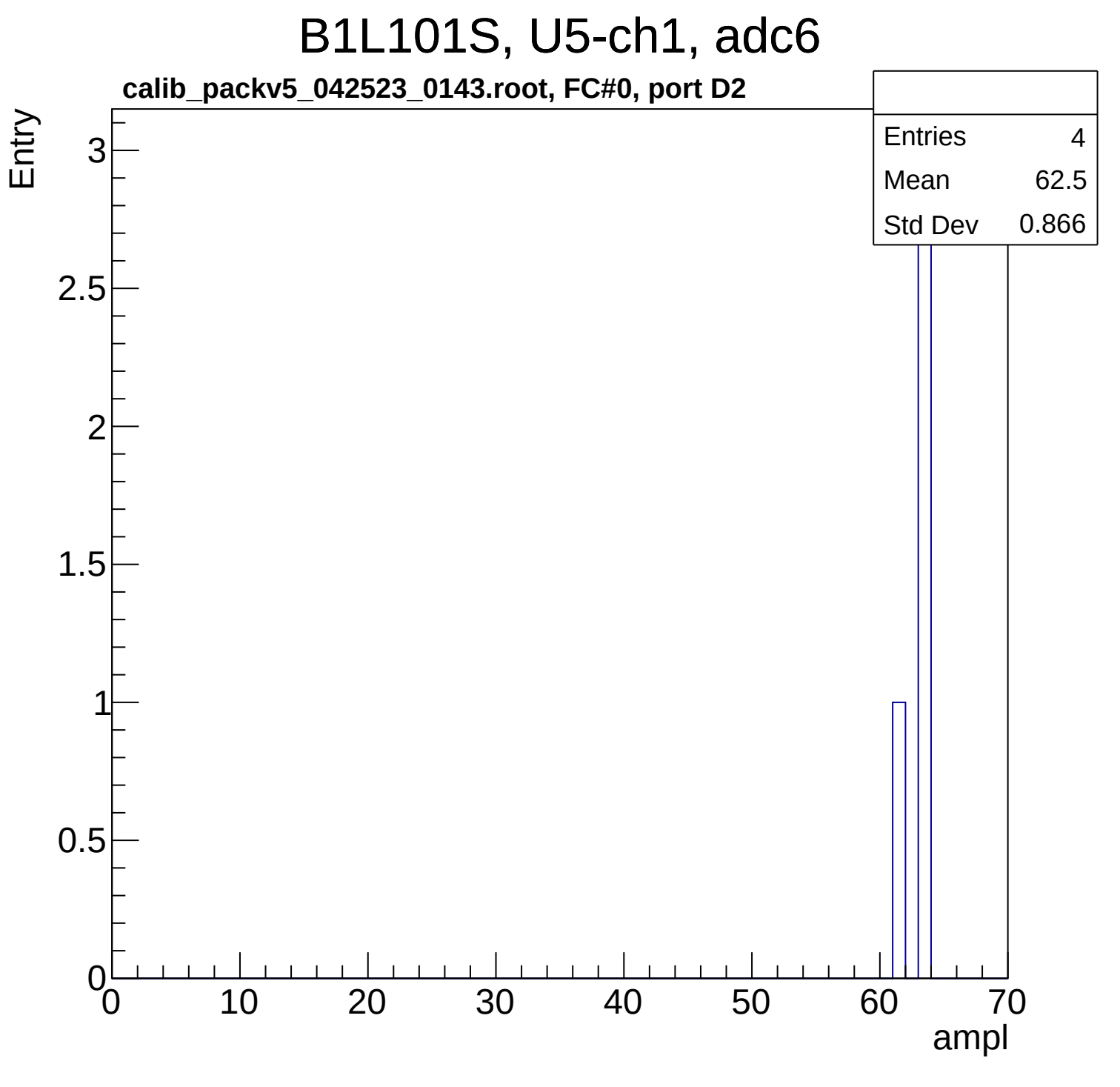
B1L101S, U5-ch1, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 62.5
Std Dev 0.866
Entry
ampl
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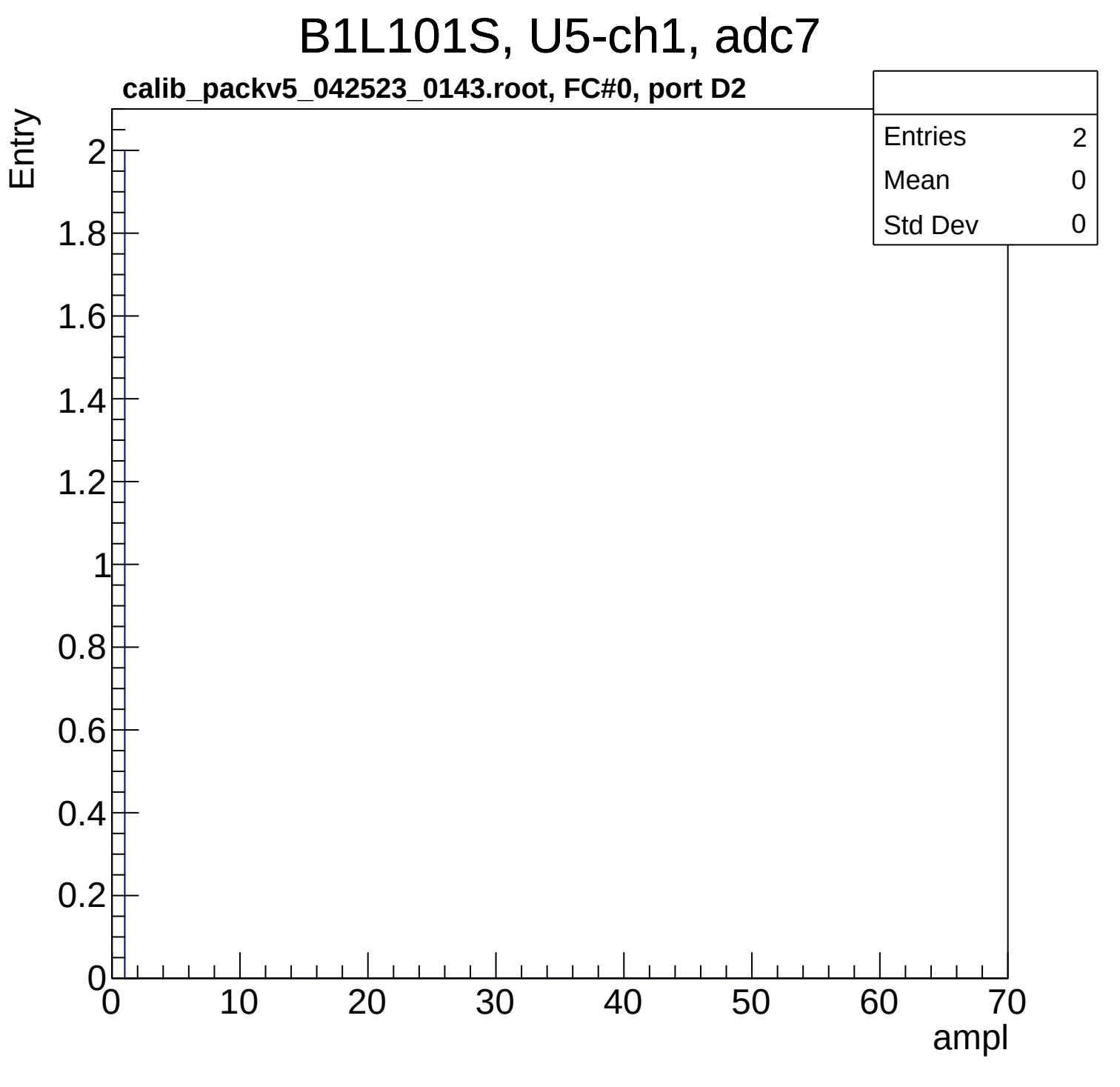
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U5-ch1, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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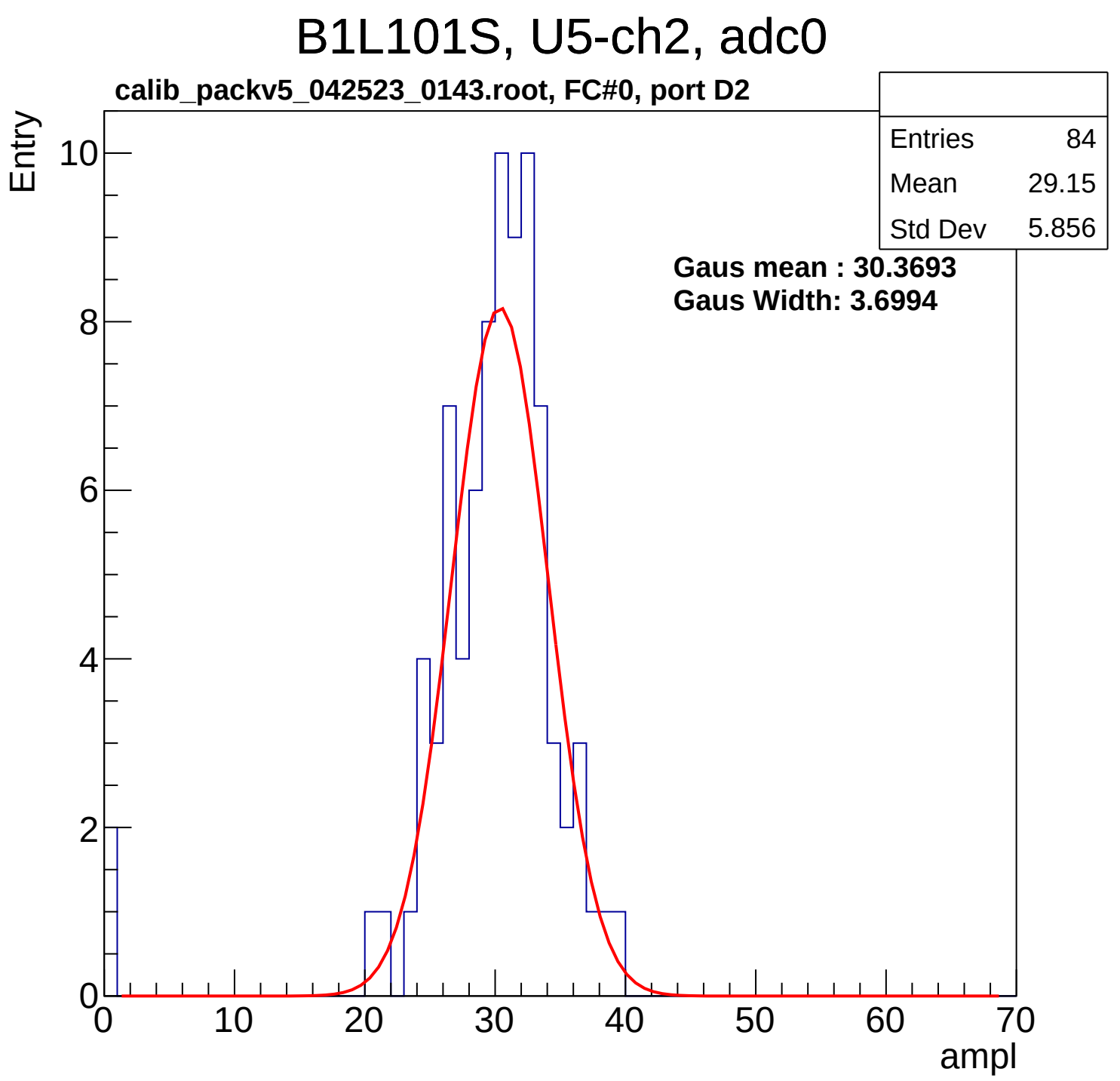
B1L101S, U5-ch2, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 84
Mean 29.15
Std Dev 5.856
Gaus mean : 30.3693
Gaus Width: 3.6994
Entry
ampl
0
2
4
6
8
10
0
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20
30
40
50
60
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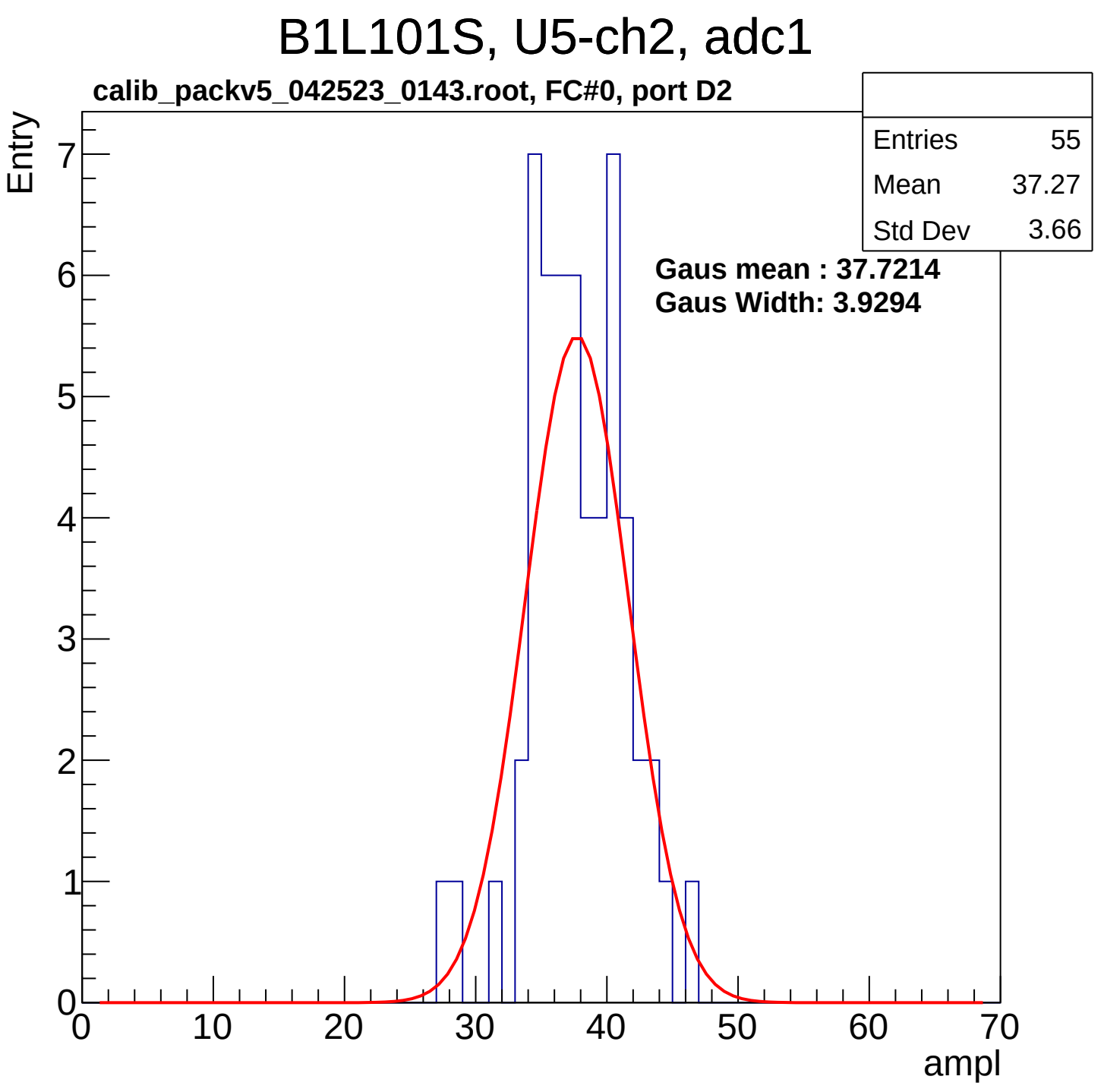
B1L101S, U5-ch2, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 37.27
Std Dev 3.66
Gaus mean : 37.7214
Gaus Width: 3.9294
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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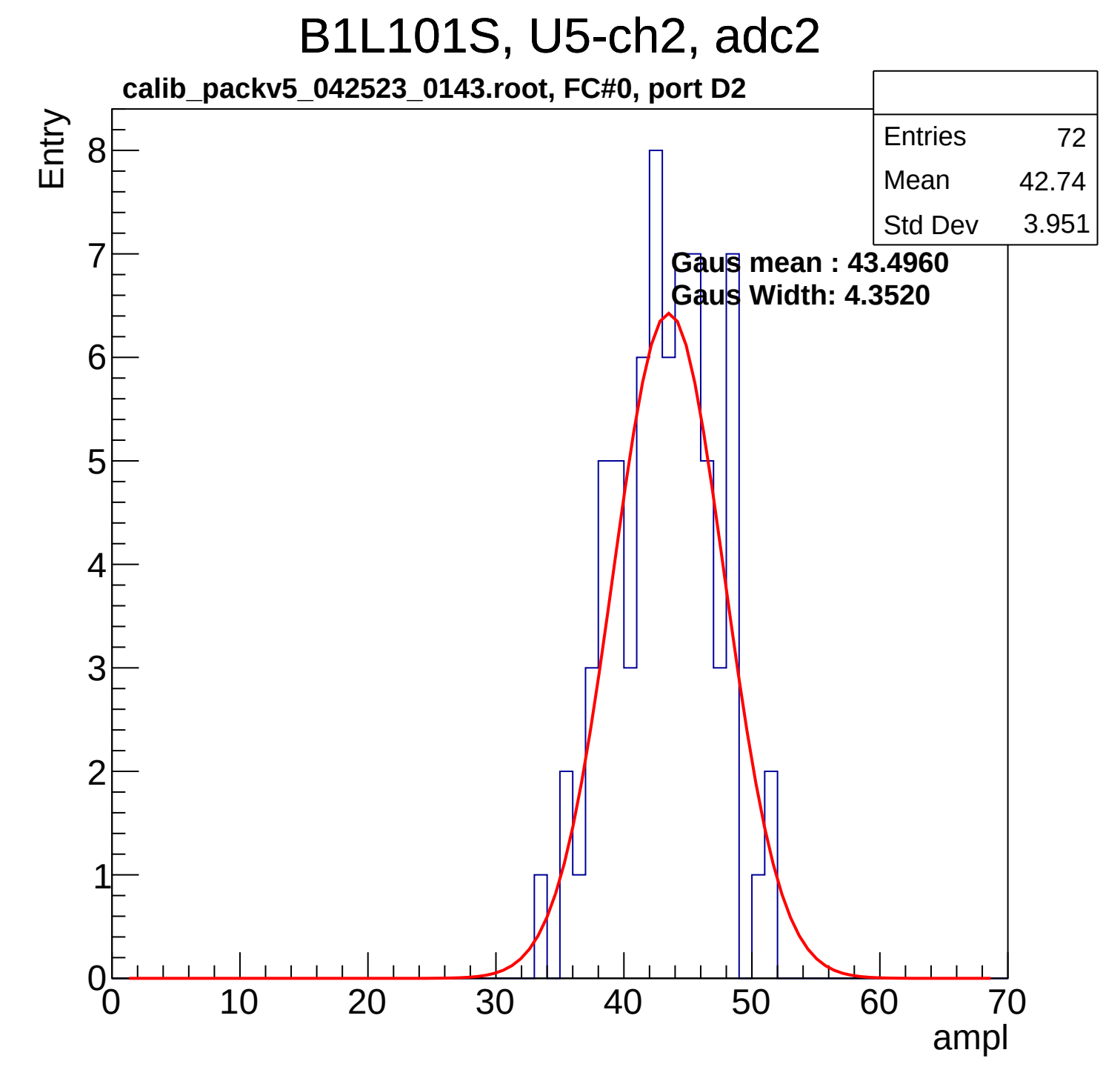
B1L101S, U5-ch2, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 42.74
Std Dev 3.951
Gaus mean : 43.4960
Gaus Width: 4.3520
Entry
ampl
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3
4
5
6
7
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0
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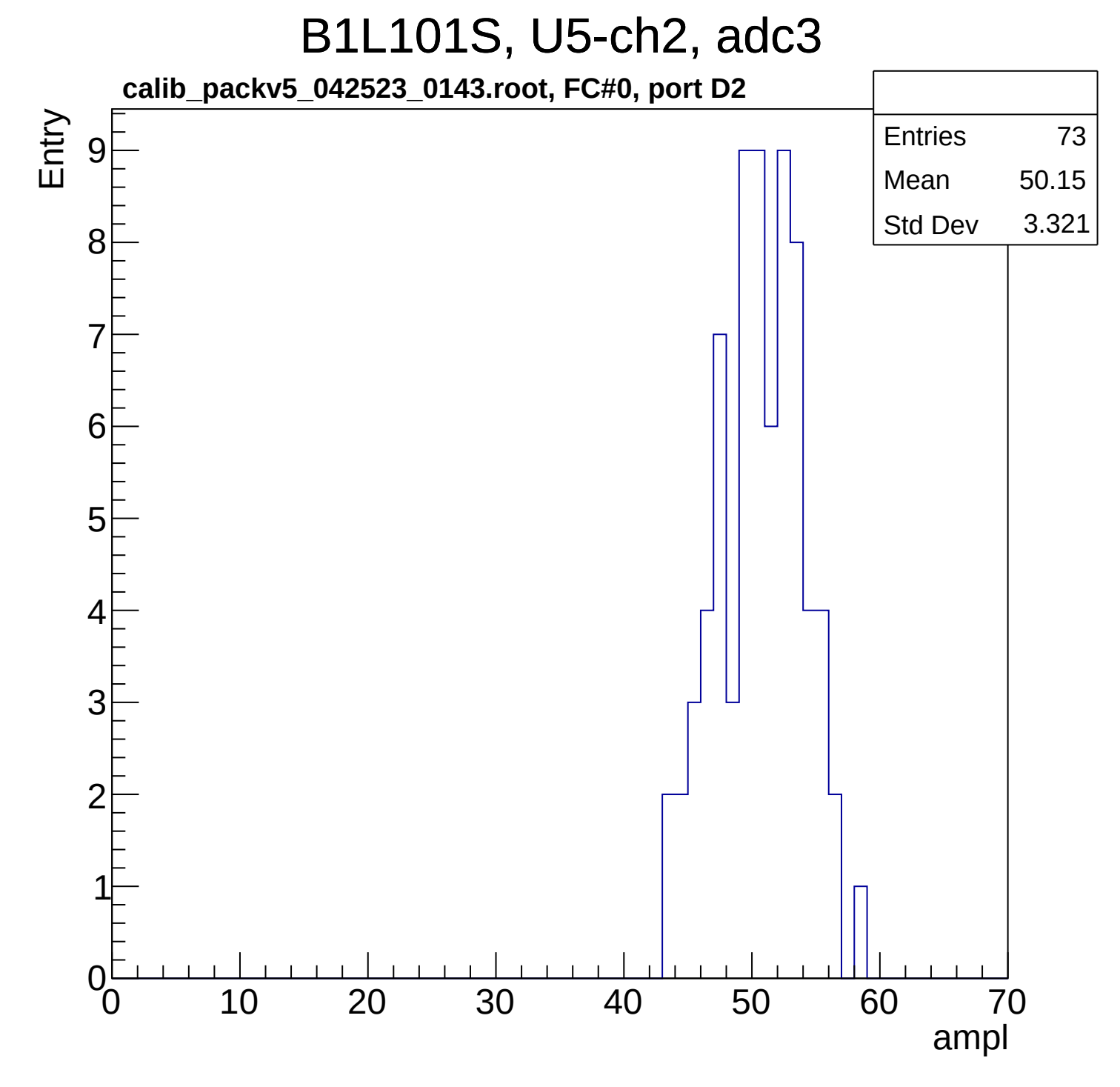
B1L101S, U5-ch2, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 50.15
Std Dev 3.321
Entry
ampl
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3
4
5
6
7
8
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0
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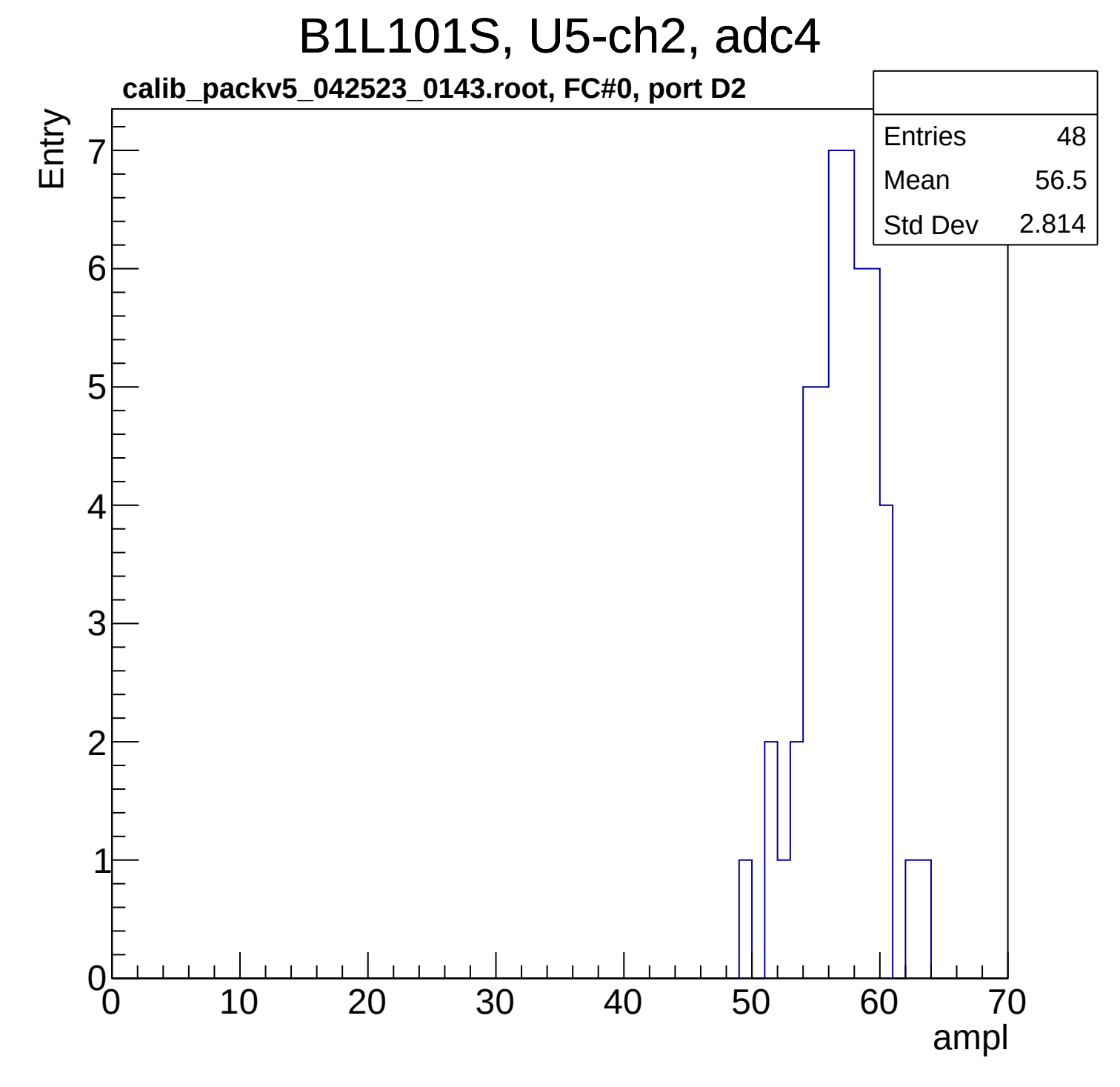
B1L101S, U5-ch2, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 56.5
Std Dev 2.814
Entry
ampl
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1
2
3
4
5
6
7
0
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60
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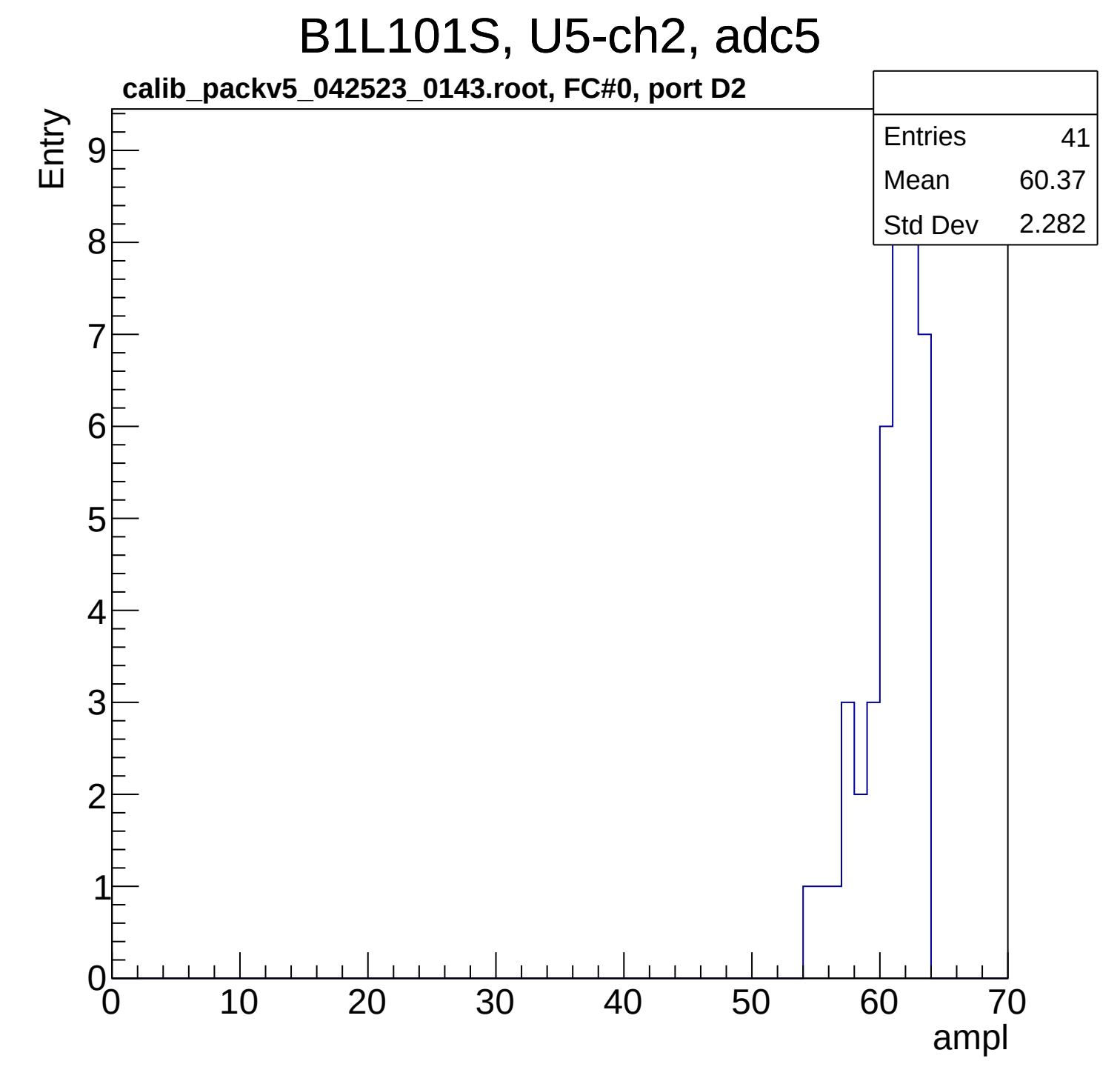
B1L101S, U5-ch2, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 41
Mean 60.37
Std Dev 2.282
Entry
ampl
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3
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5
6
7
8
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0
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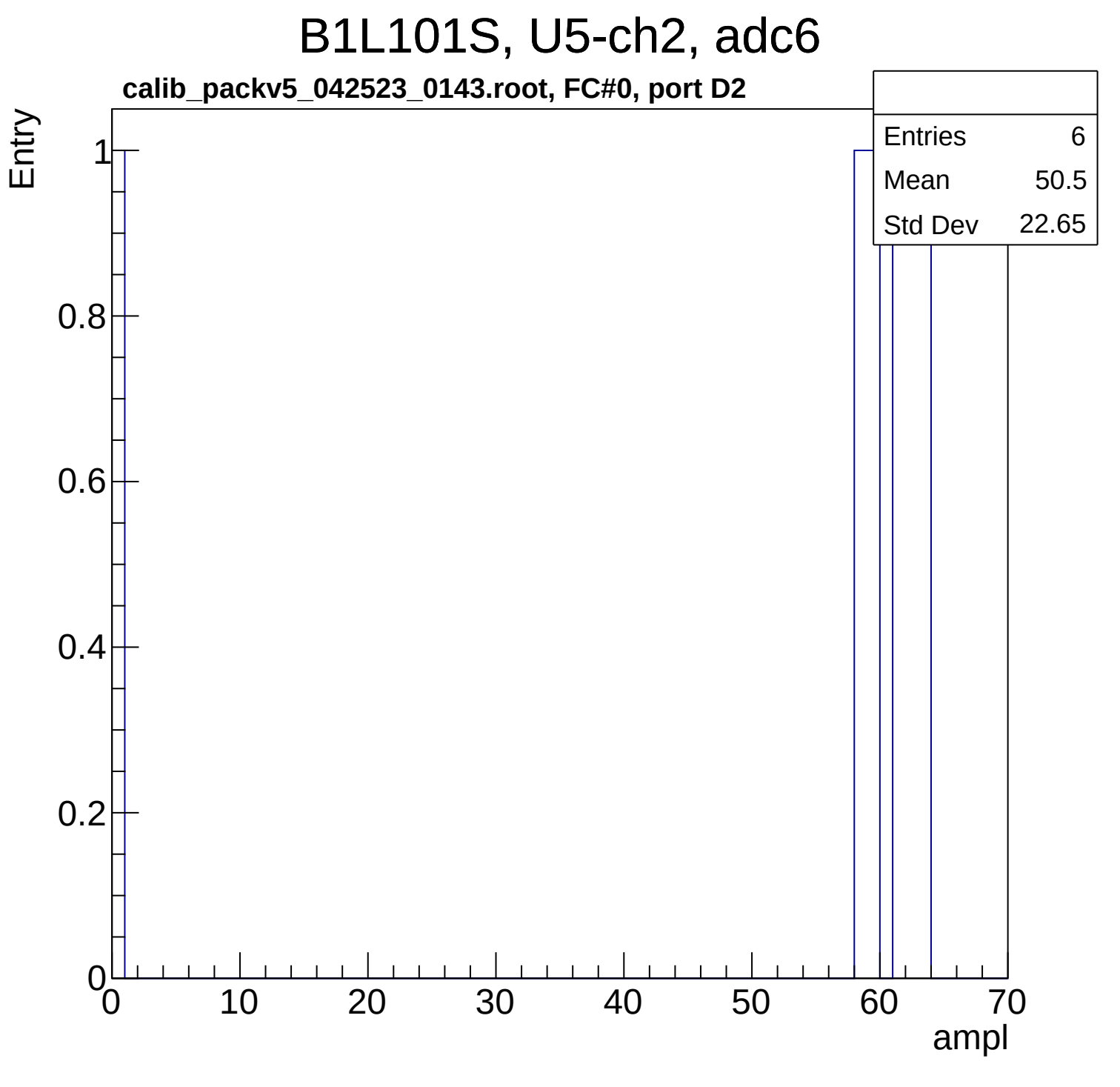
B1L101S, U5-ch2, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 50.5
Std Dev 22.65
Entry
ampl
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0.2
0.4
0.6
0.8
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0
10
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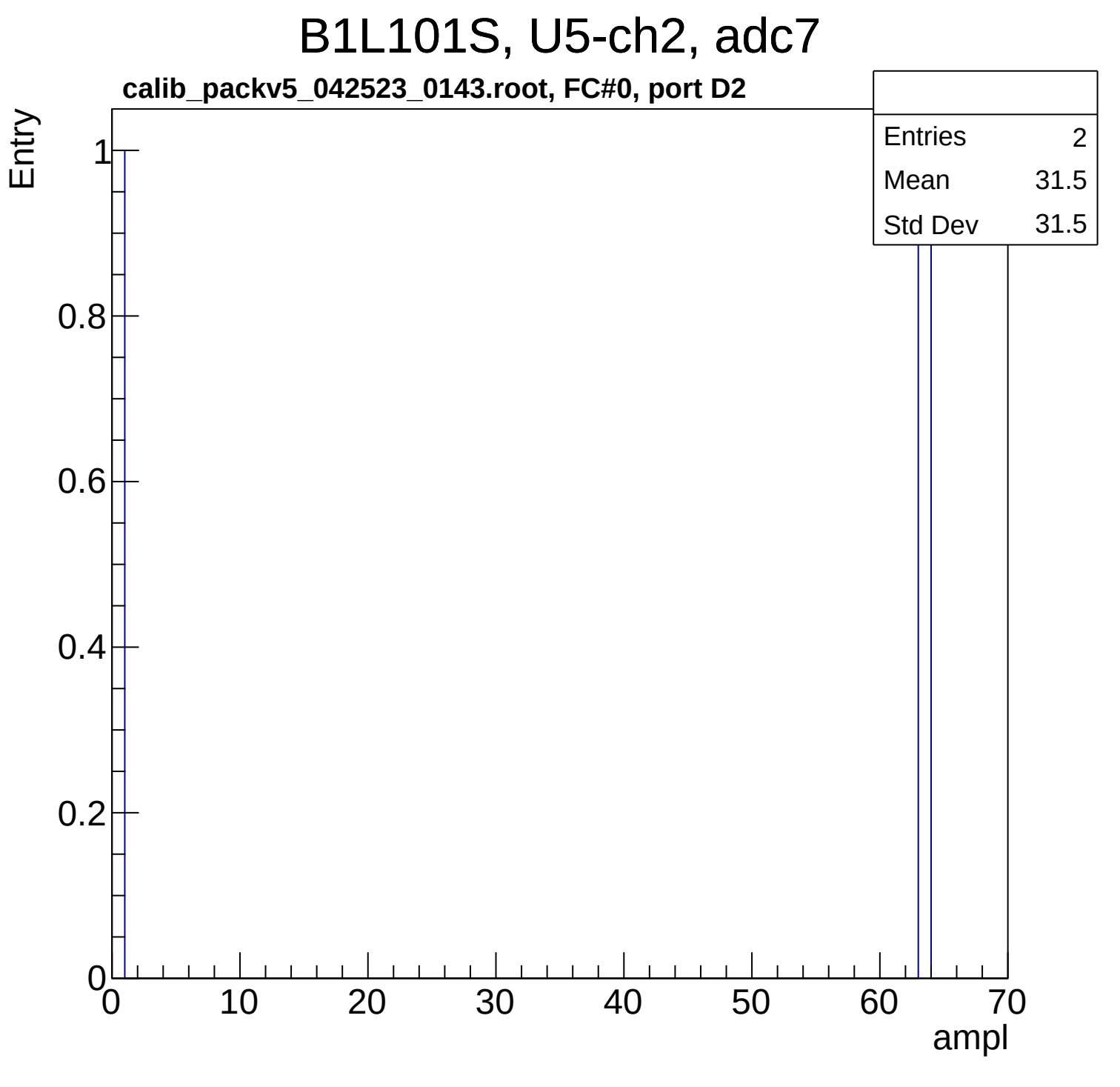
40
50
60
70


B1L101S, U5-ch2, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
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0.6
0.4
0.2
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10
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30
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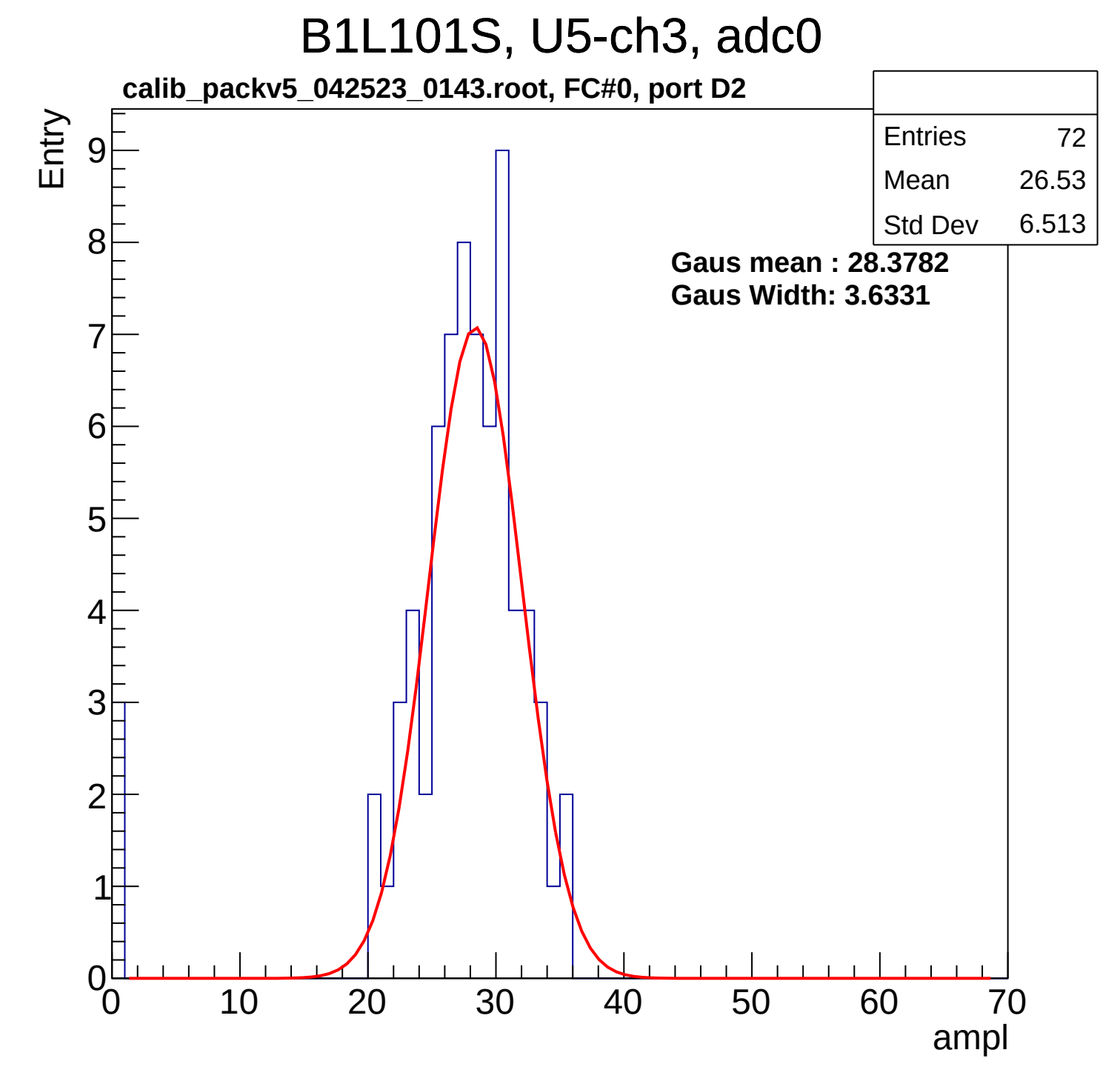
50
60
70
ampl


B1L101S, U5-ch3, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 26.53
Std Dev 6.513
Gaus mean : 28.3782
Gaus Width: 3.6331
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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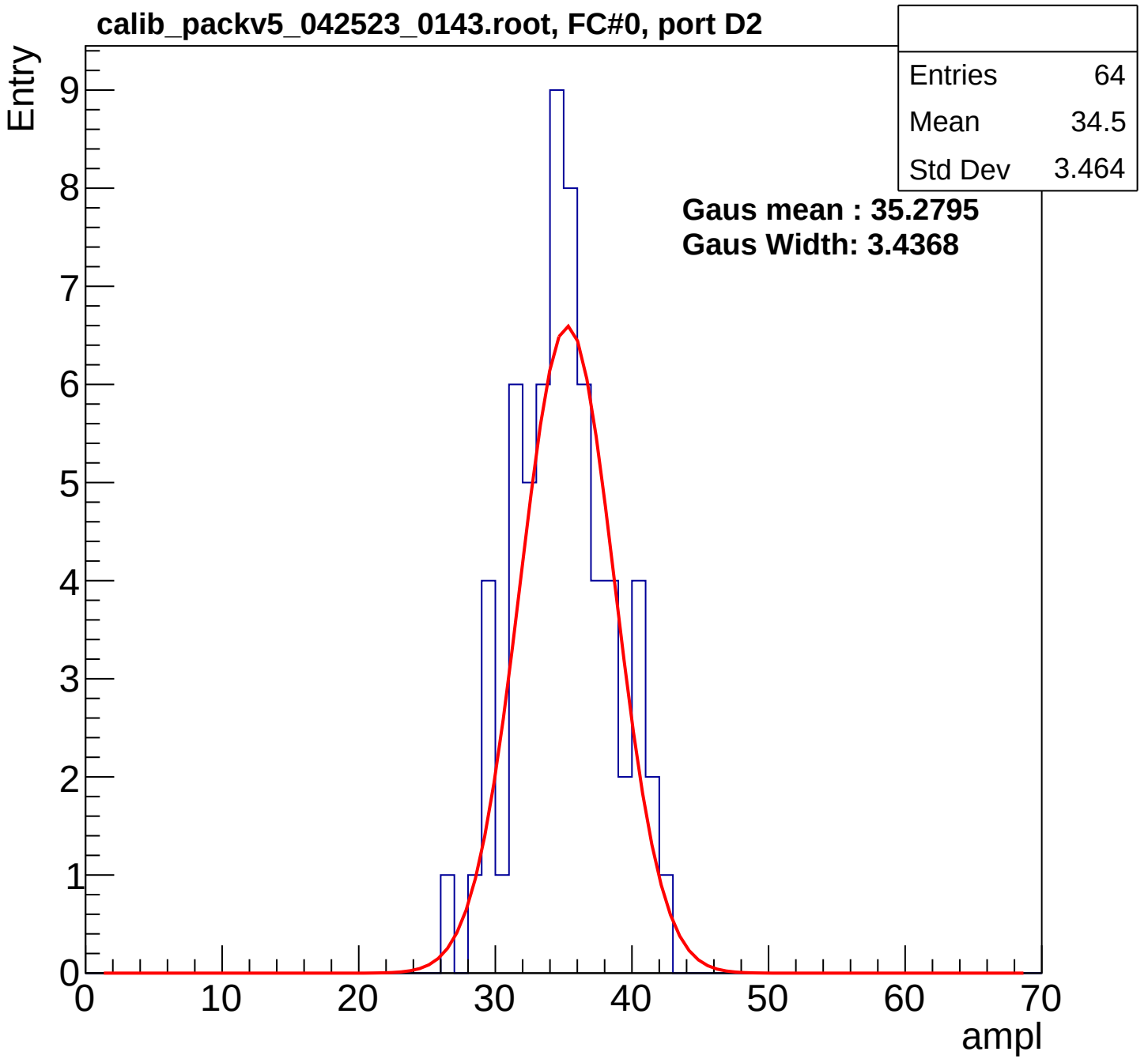
B1L101S, U5-ch3, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 34.5
Std Dev 3.464
Gaus mean : 35.2795
Gaus Width: 3.4368
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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60
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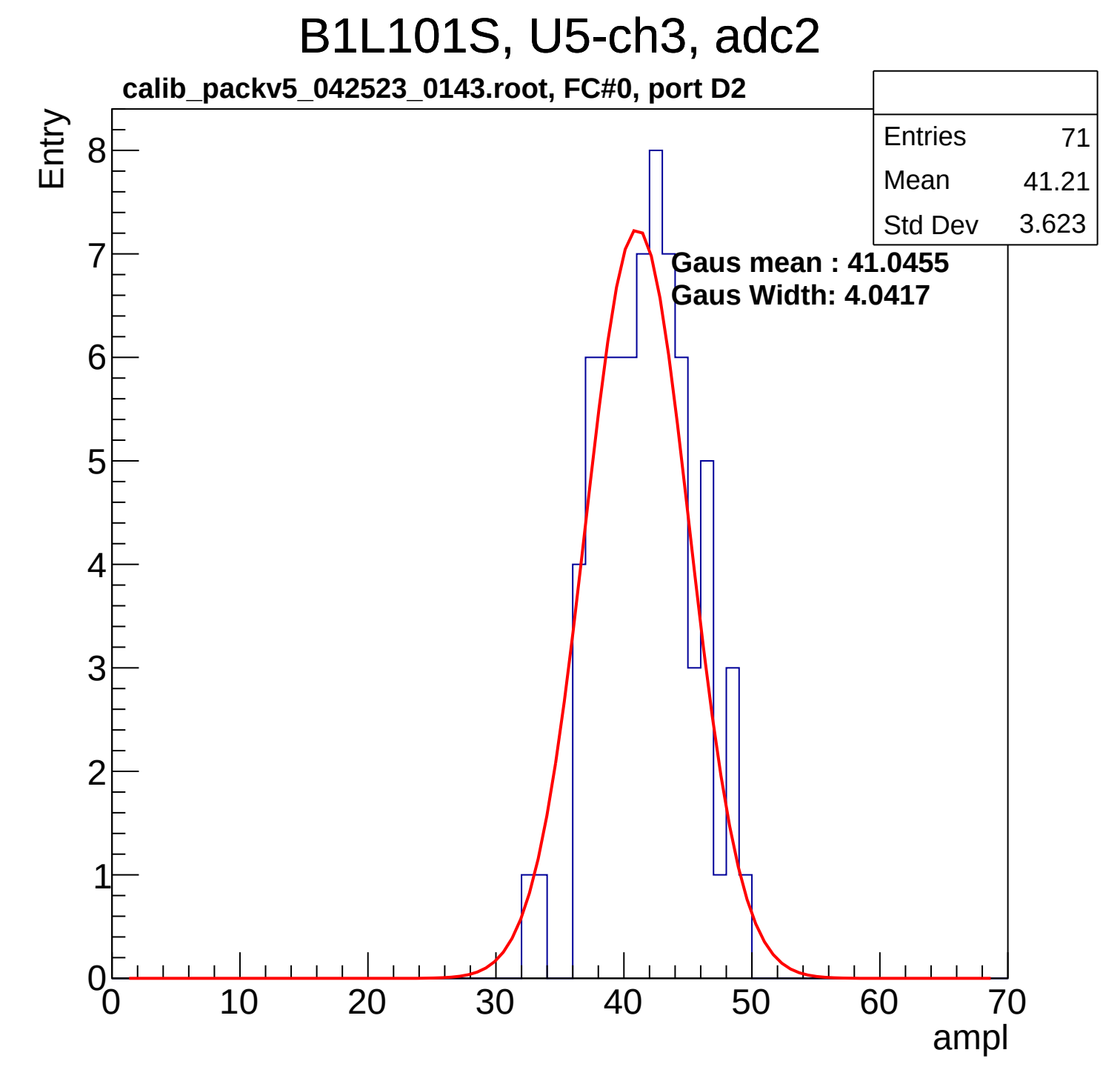
B1L101S, U5-ch3, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 41.21
Std Dev 3.623
Gaus mean : 41.0455
Gaus Width: 4.0417
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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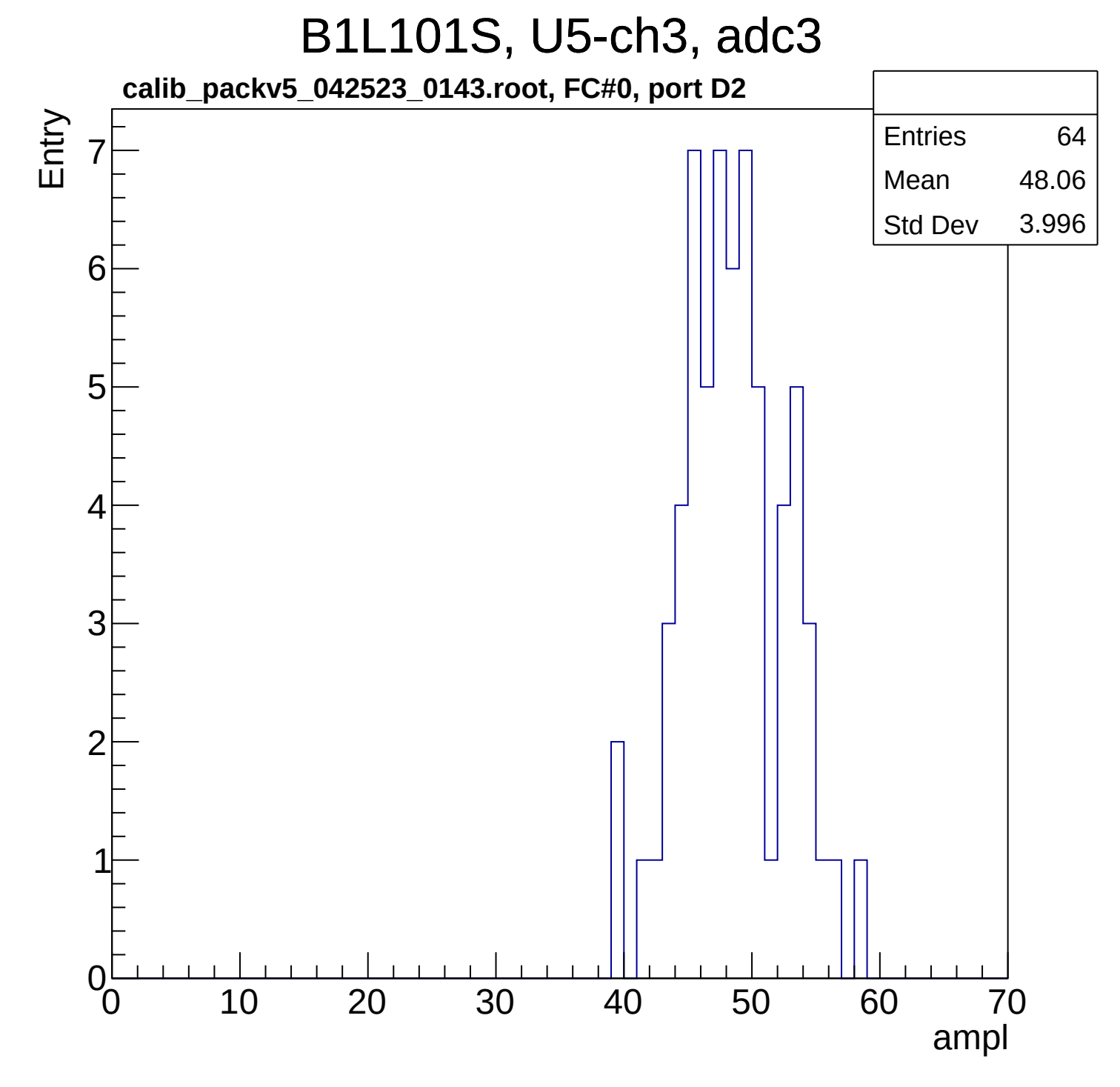
B1L101S, U5-ch3, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 48.06
Std Dev 3.996
Entry
ampl
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3
4
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7
0
10
20
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40
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60
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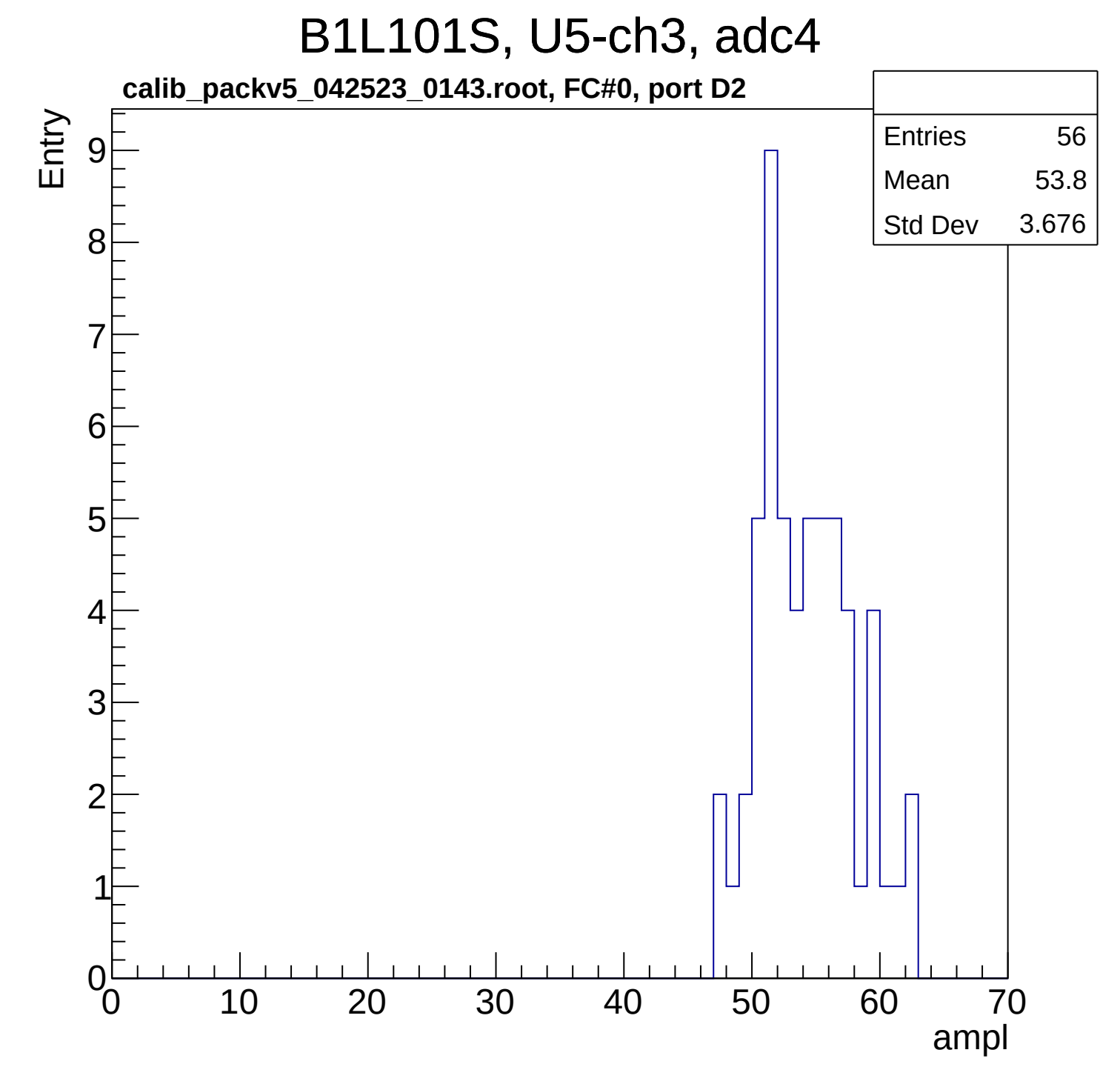
B1L101S, U5-ch3, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 53.8
Std Dev 3.676
Entry
ampl
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2
3
4
5
6
7
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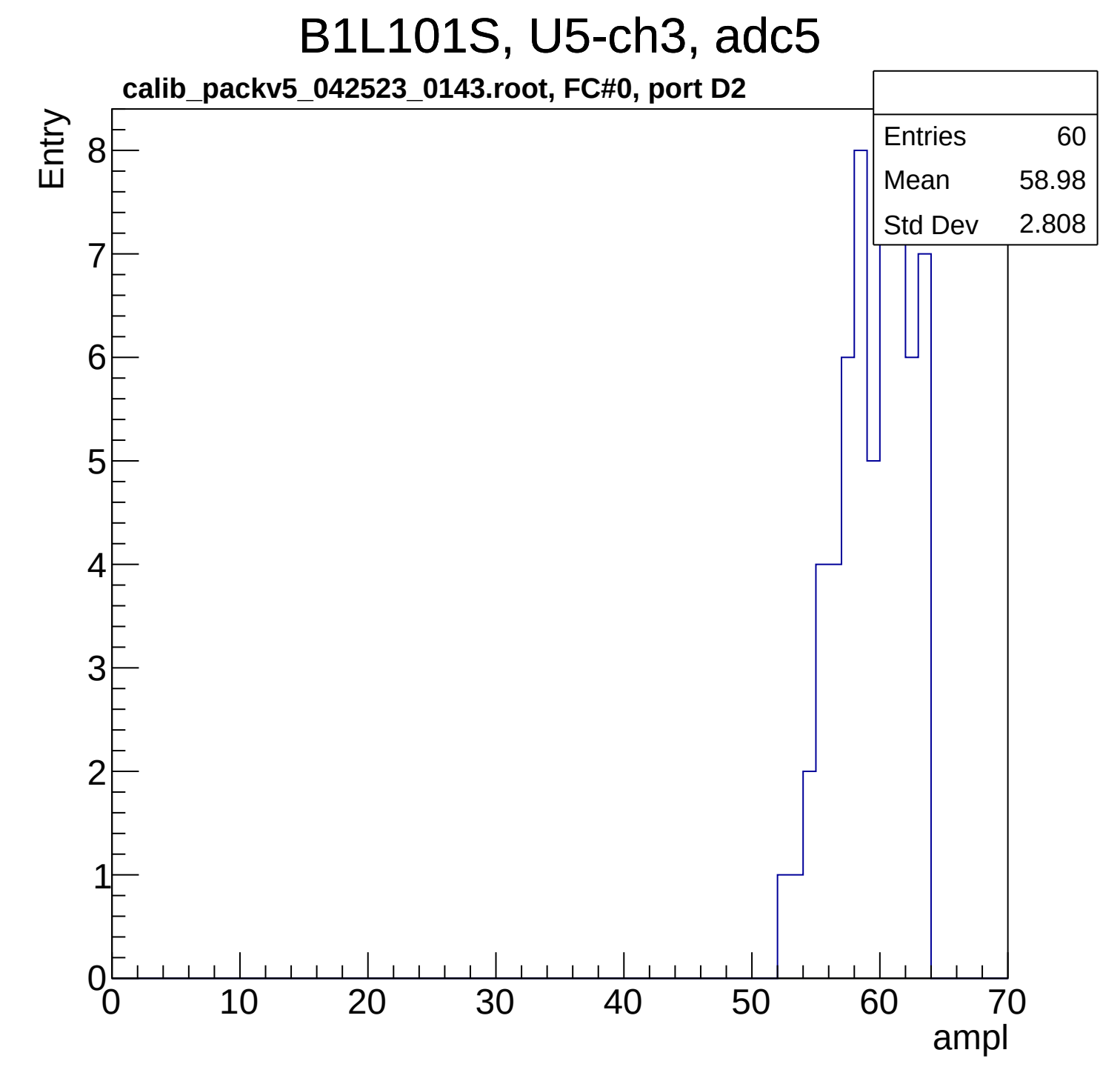
B1L101S, U5-ch3, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 58.98
Std Dev 2.808
Entry
ampl
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2
3
4
5
6
7
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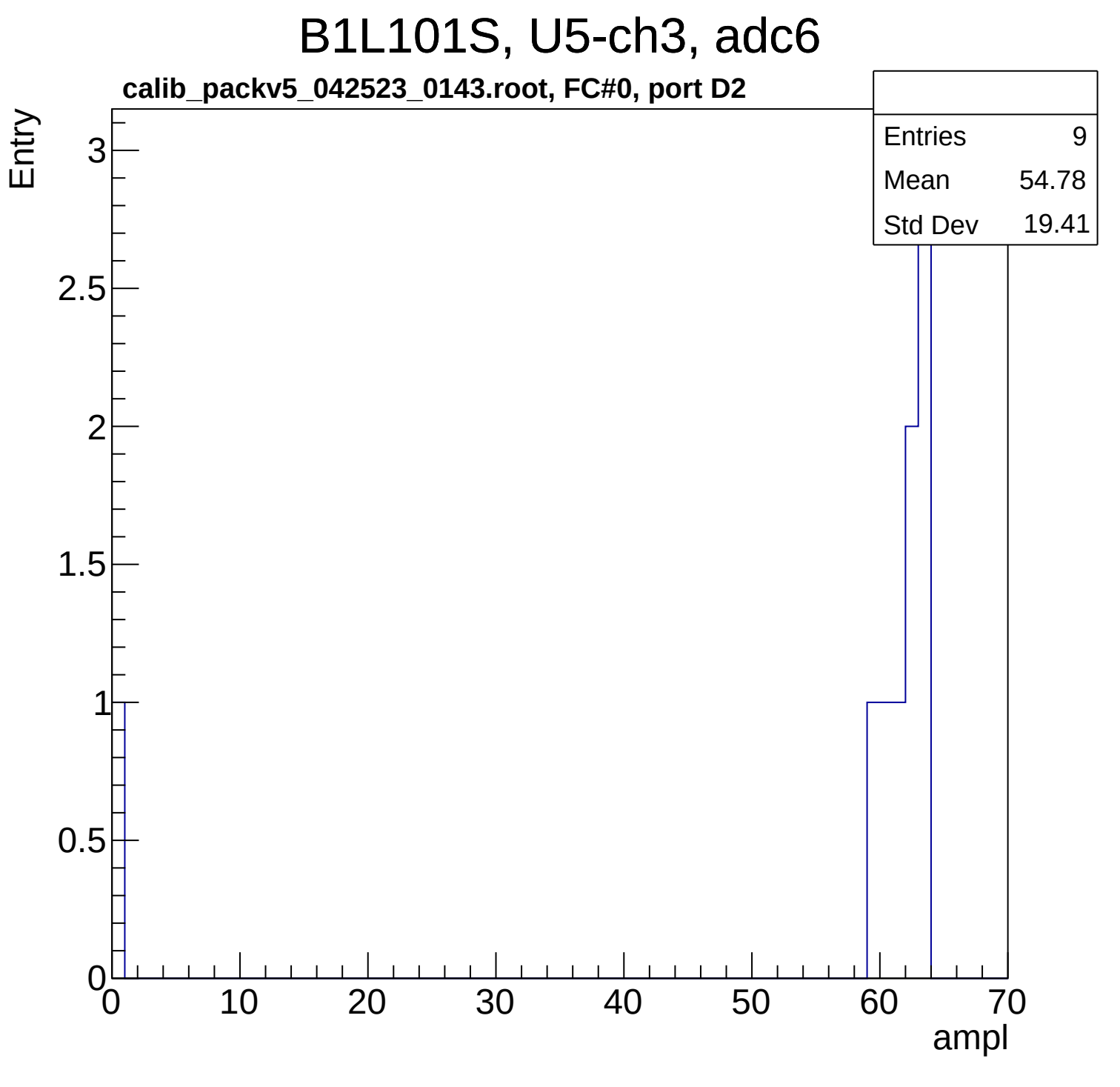
B1L101S, U5-ch3, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 54.78
Std Dev 19.41
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
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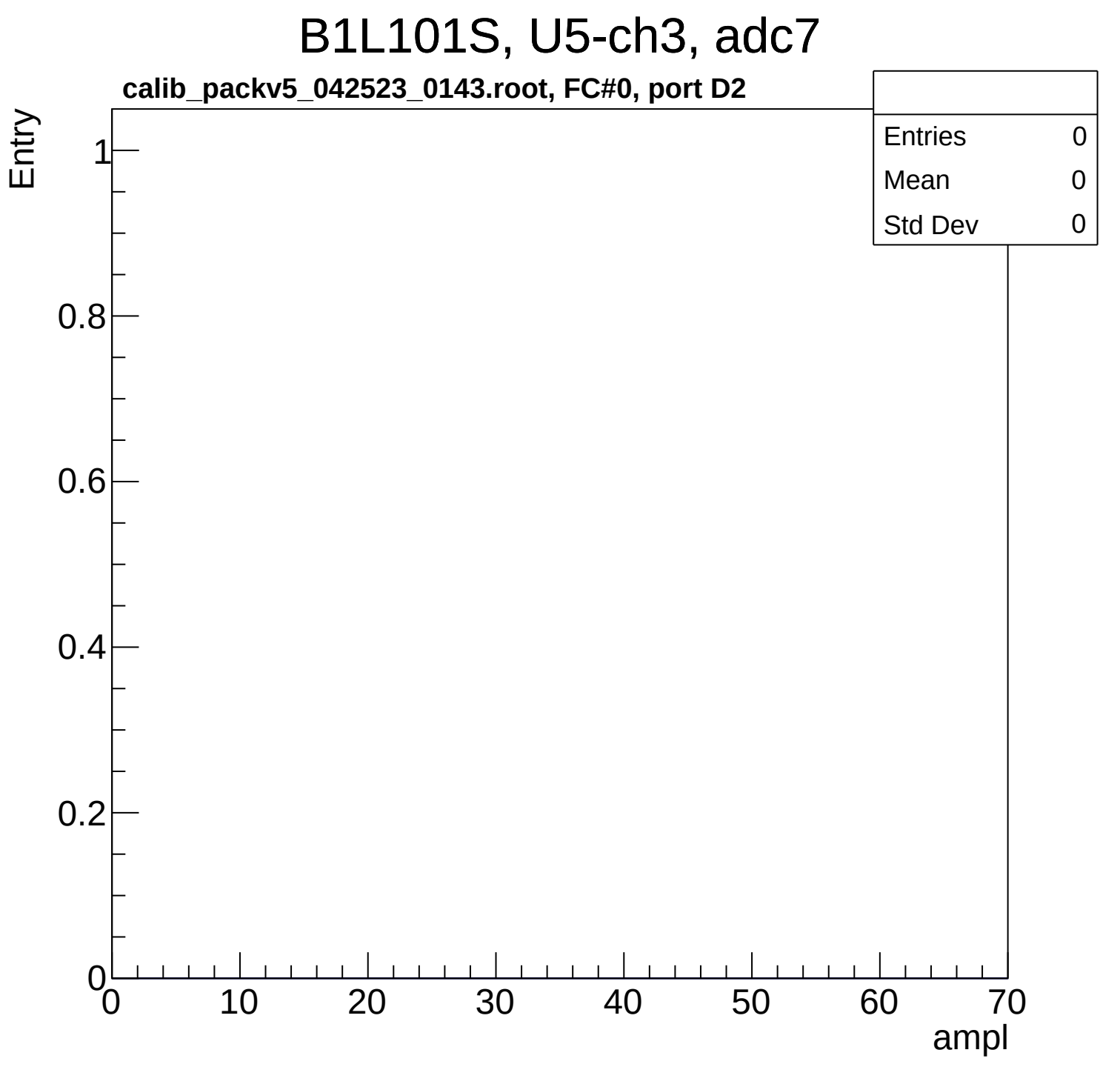
40
50
60
70


B1L101S, U5-ch3, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
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10
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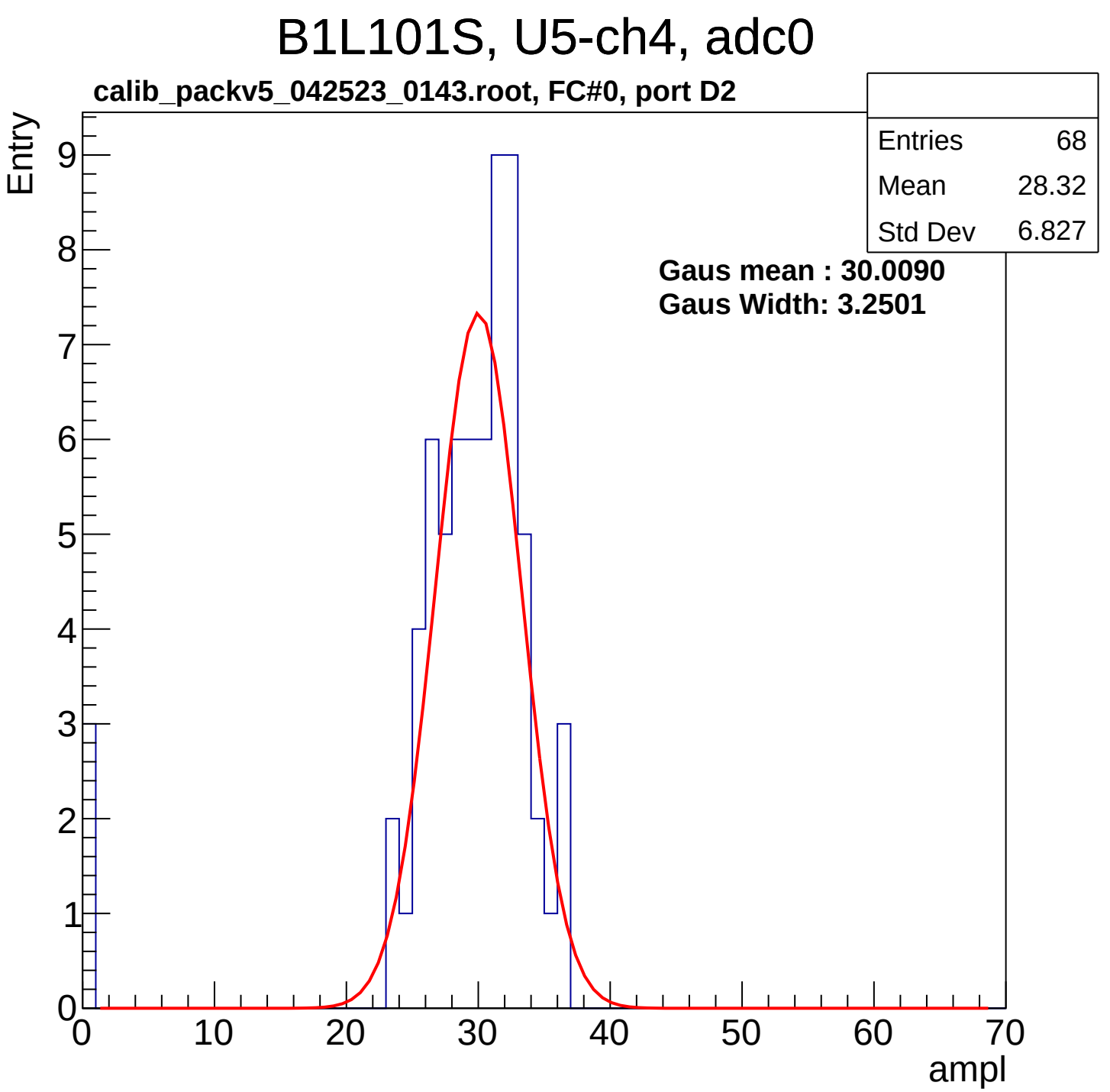
50
60
70
ampl


B1L101S, U5-ch4, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 28.32
Std Dev 6.827
Gaus mean : 30.0090
Gaus Width: 3.2501
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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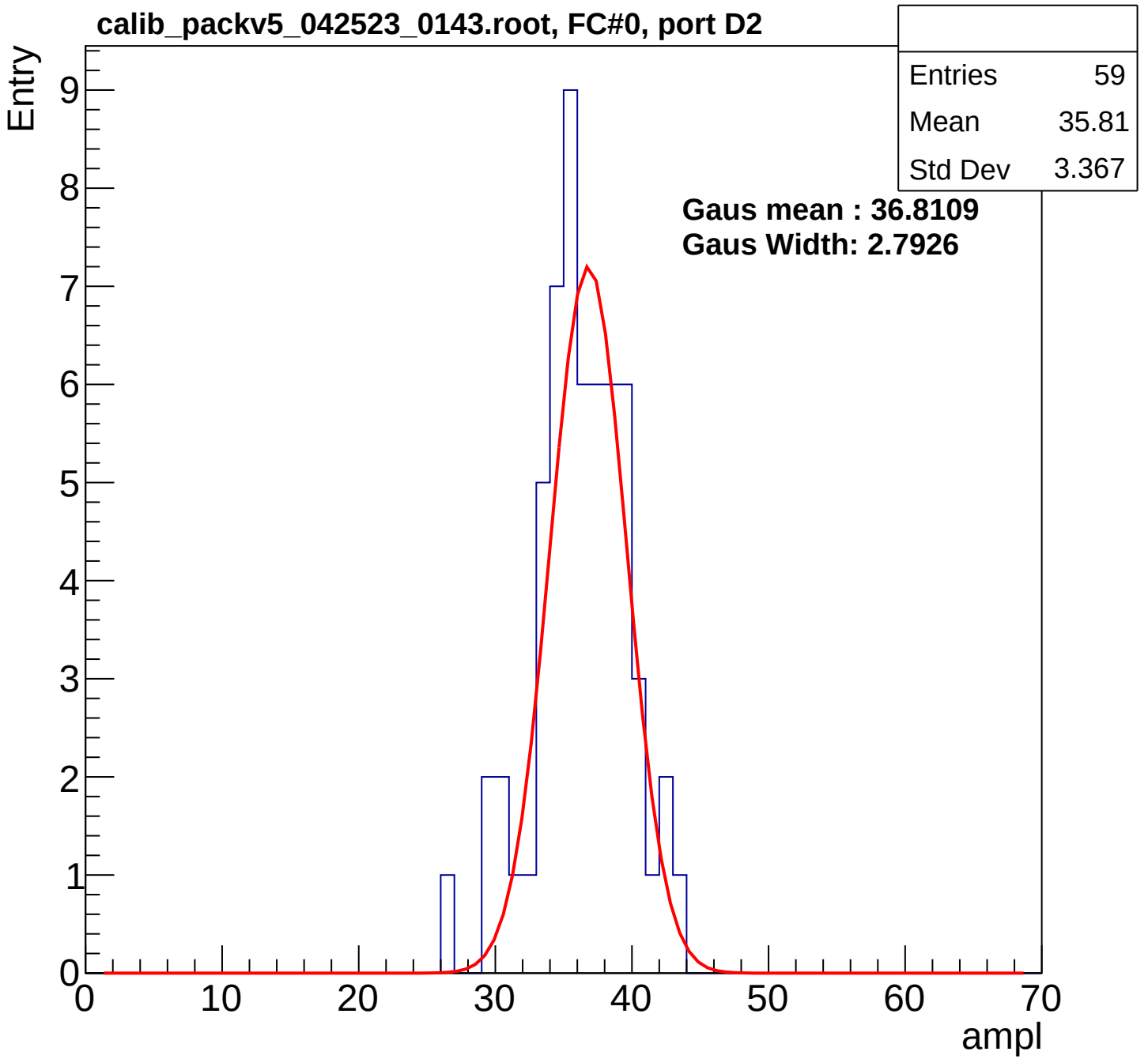
B1L101S, U5-ch4, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 35.81
Std Dev 3.367
Gaus mean : 36.8109
Gaus Width: 2.7926
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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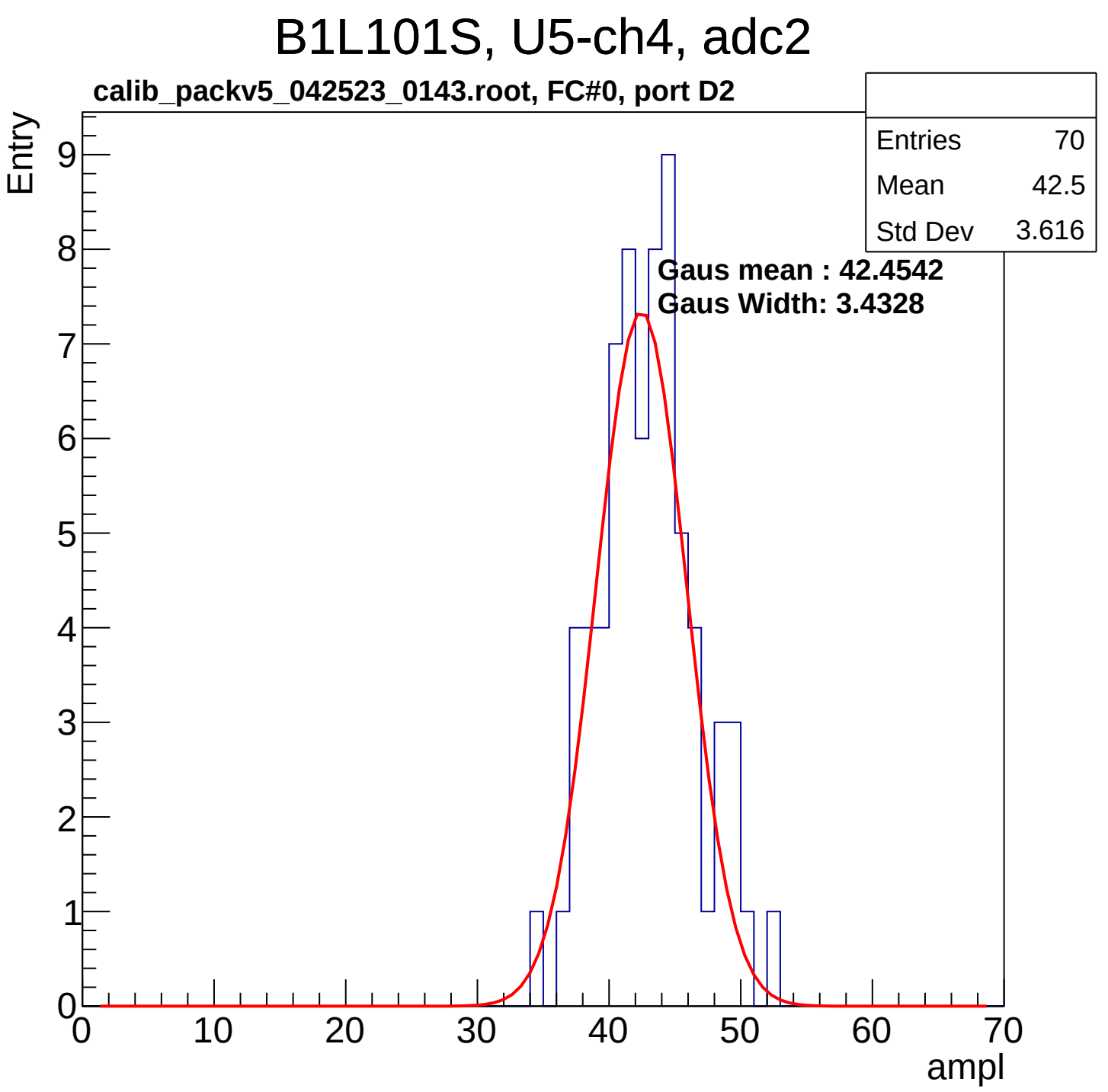
B1L101S, U5-ch4, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 42.5
Std Dev 3.616
Gaus mean : 42.4542
Gaus Width: 3.4328
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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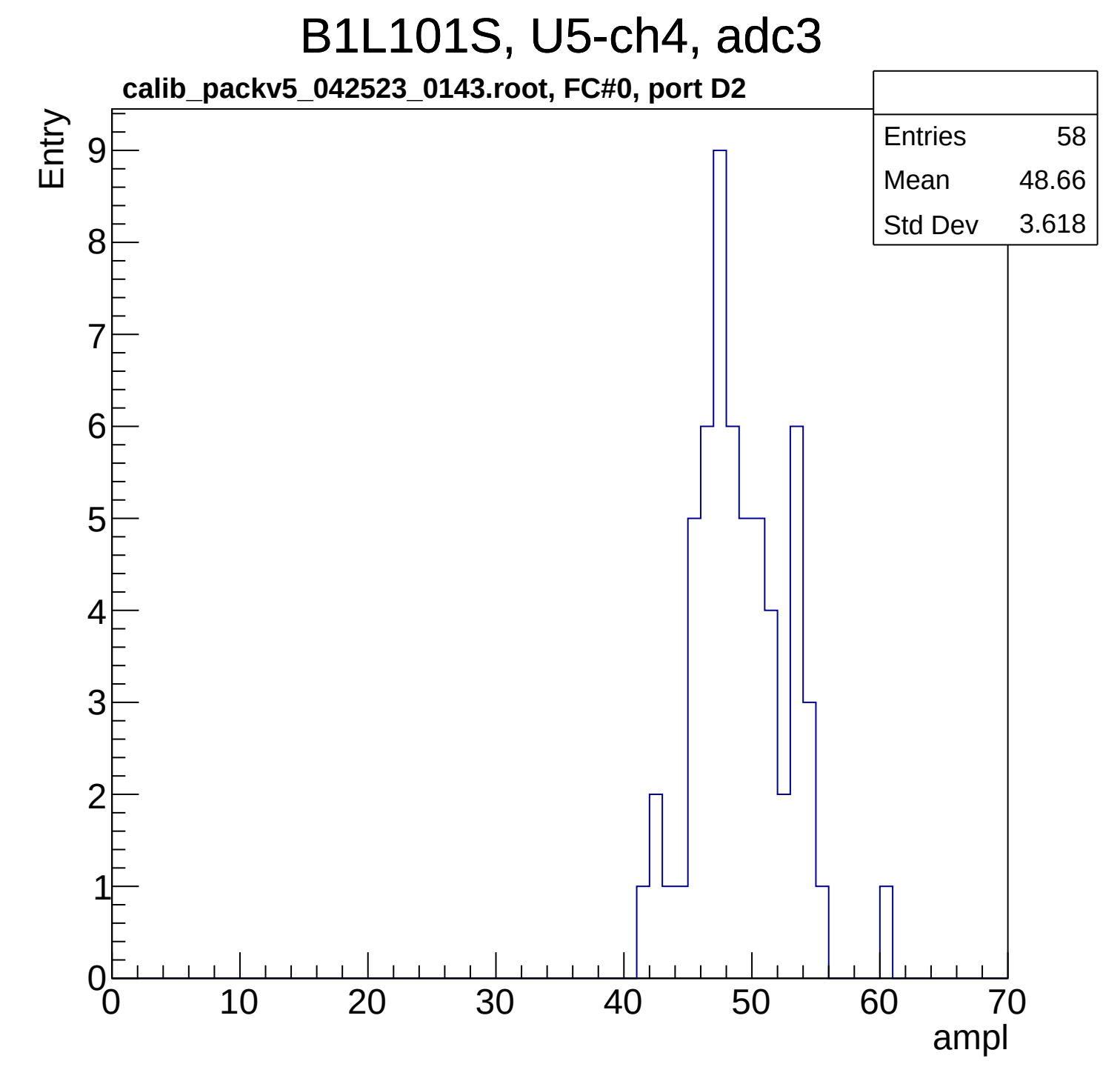
B1L101S, U5-ch4, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 48.66
Std Dev 3.618
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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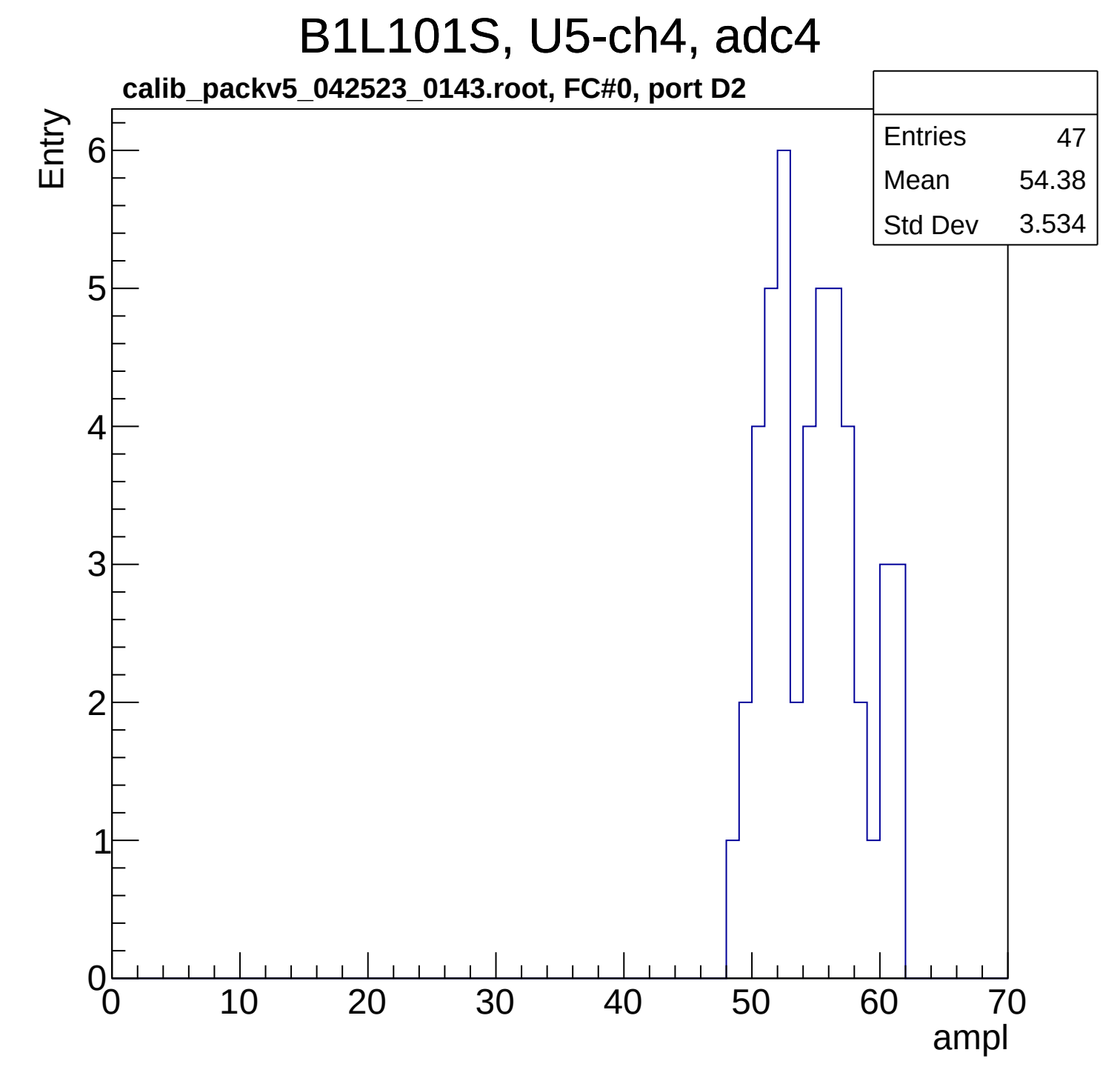
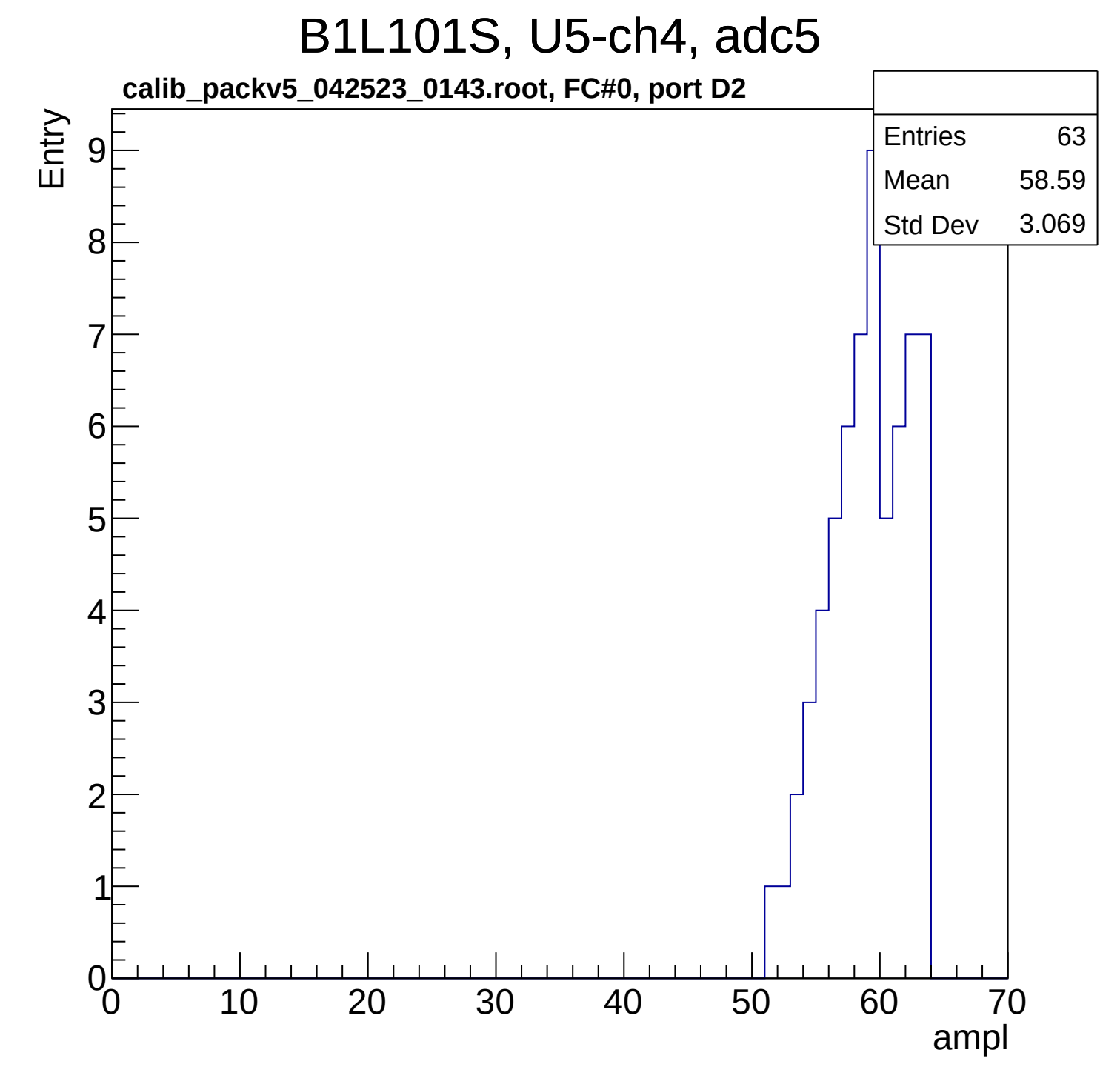

B1L101S, U5-ch4, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 54.38
Std Dev 3.534
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch4, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 58.59
Std Dev 3.069
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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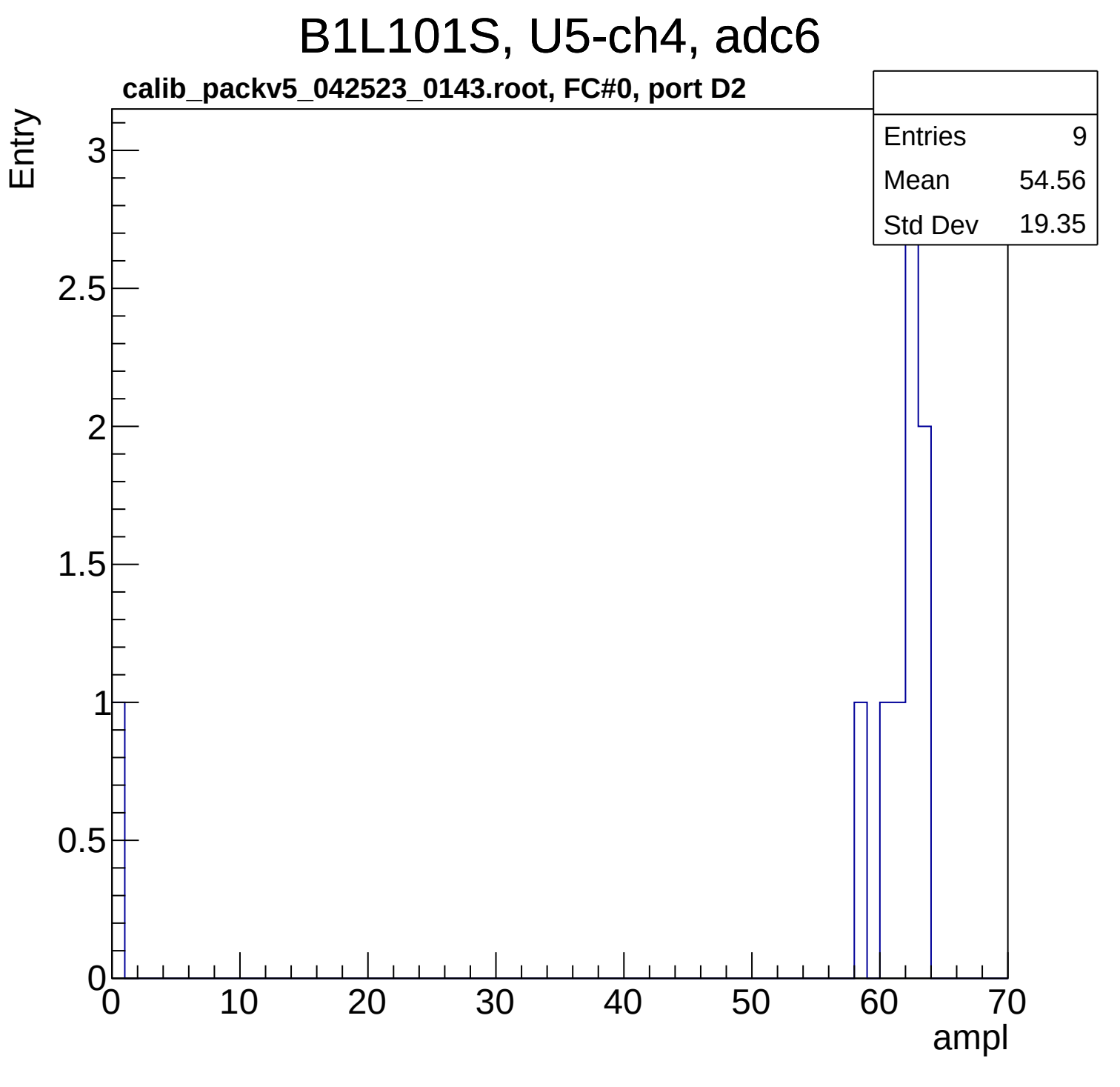
B1L101S, U5-ch4, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 54.56
Std Dev 19.35
Entry
ampl
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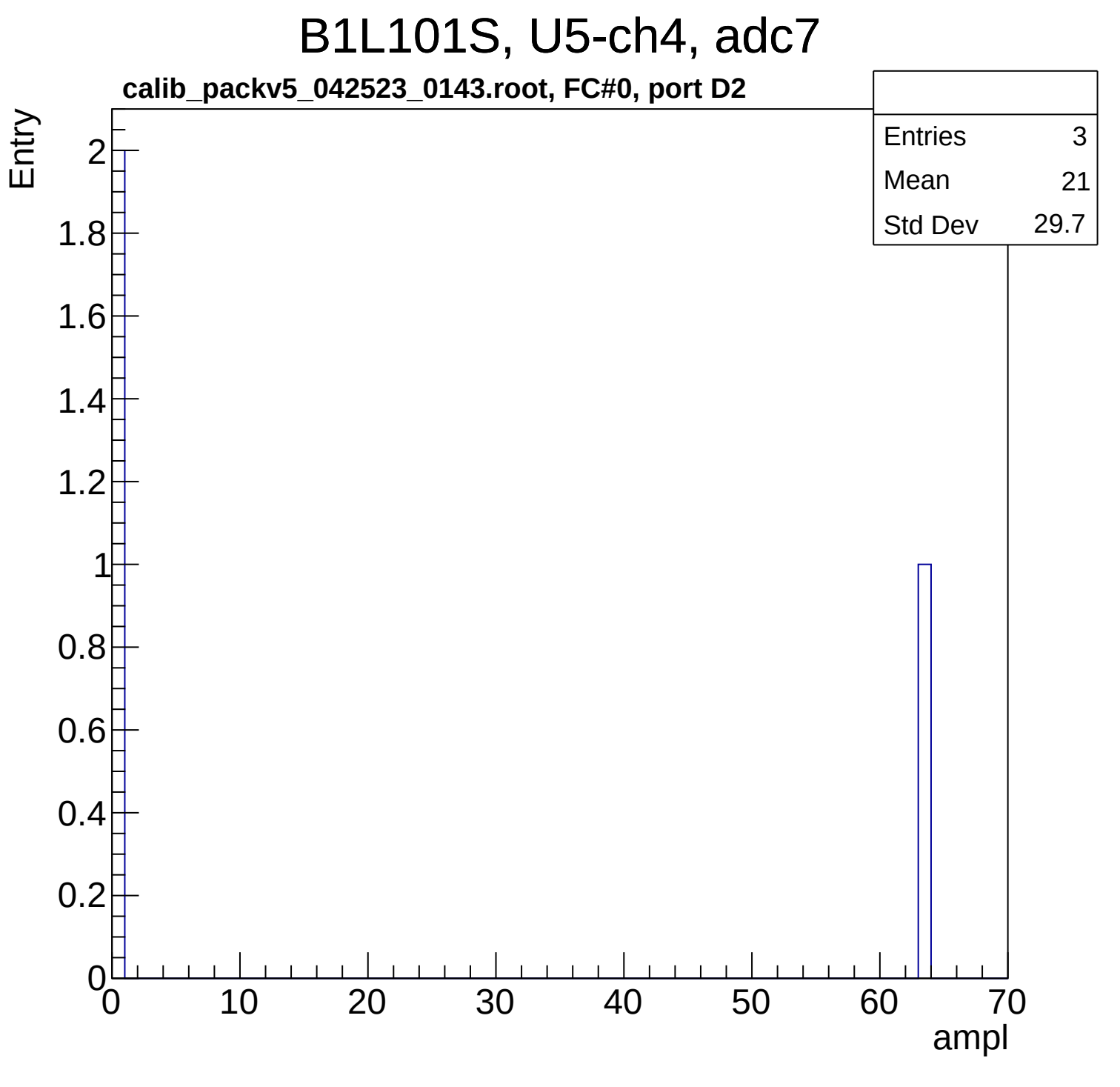
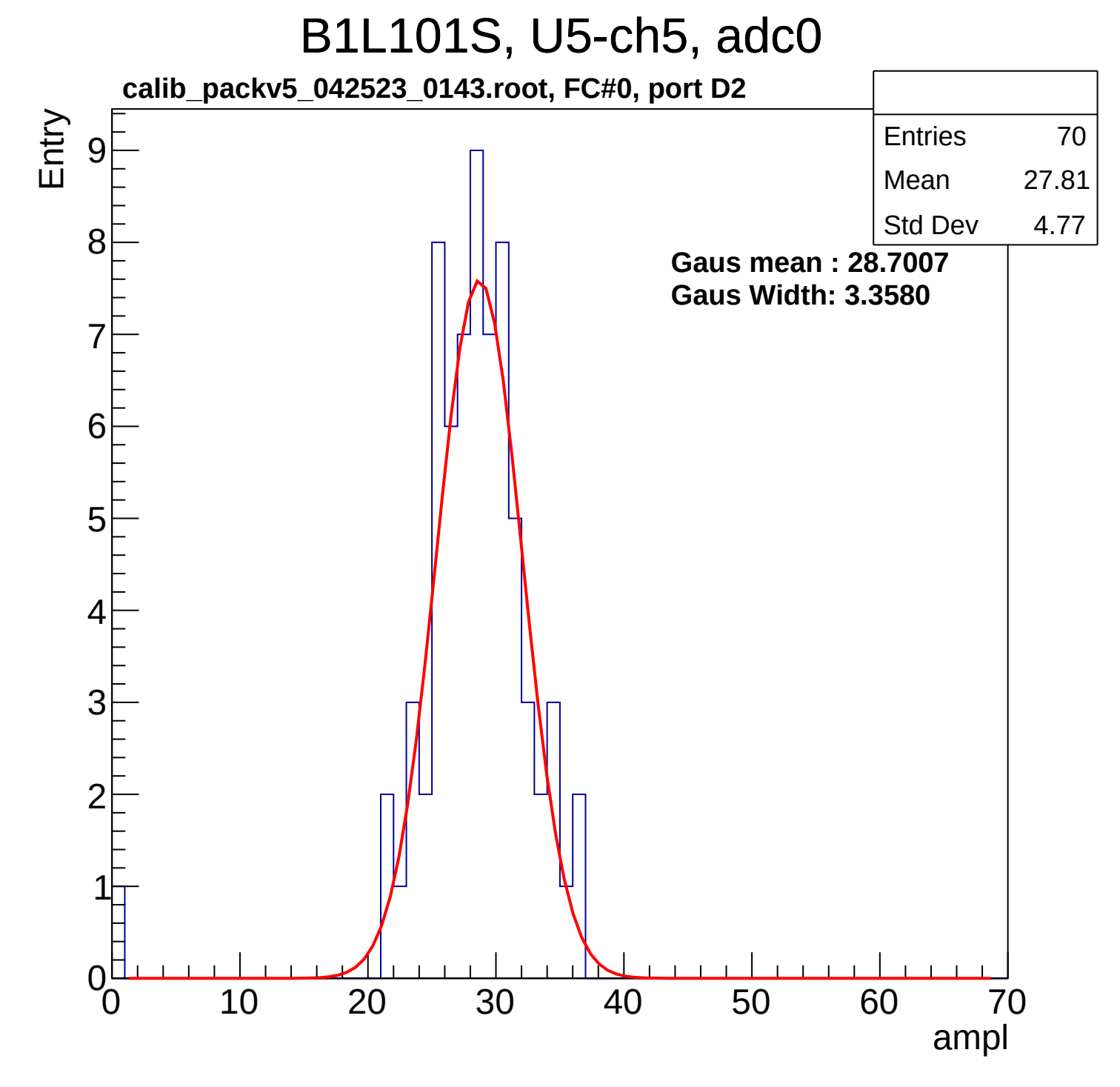
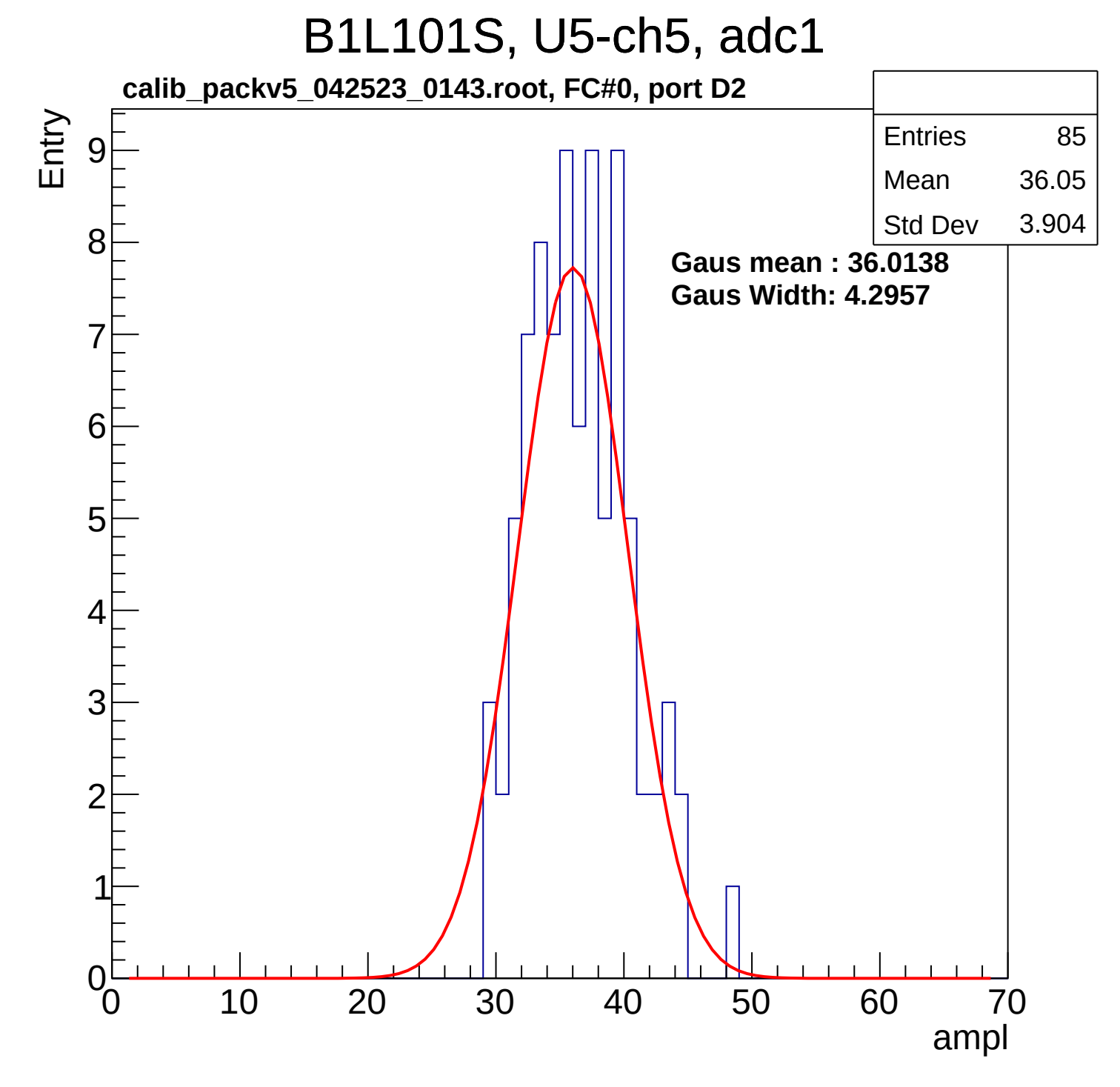
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U5-ch4, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 21
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U5-ch5, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 27.81
Std Dev 4.77
Gaus mean : 28.7007
Gaus Width: 3.3580
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch5, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 85
Mean 36.05
Std Dev 3.904
Gaus mean : 36.0138
Gaus Width: 4.2957
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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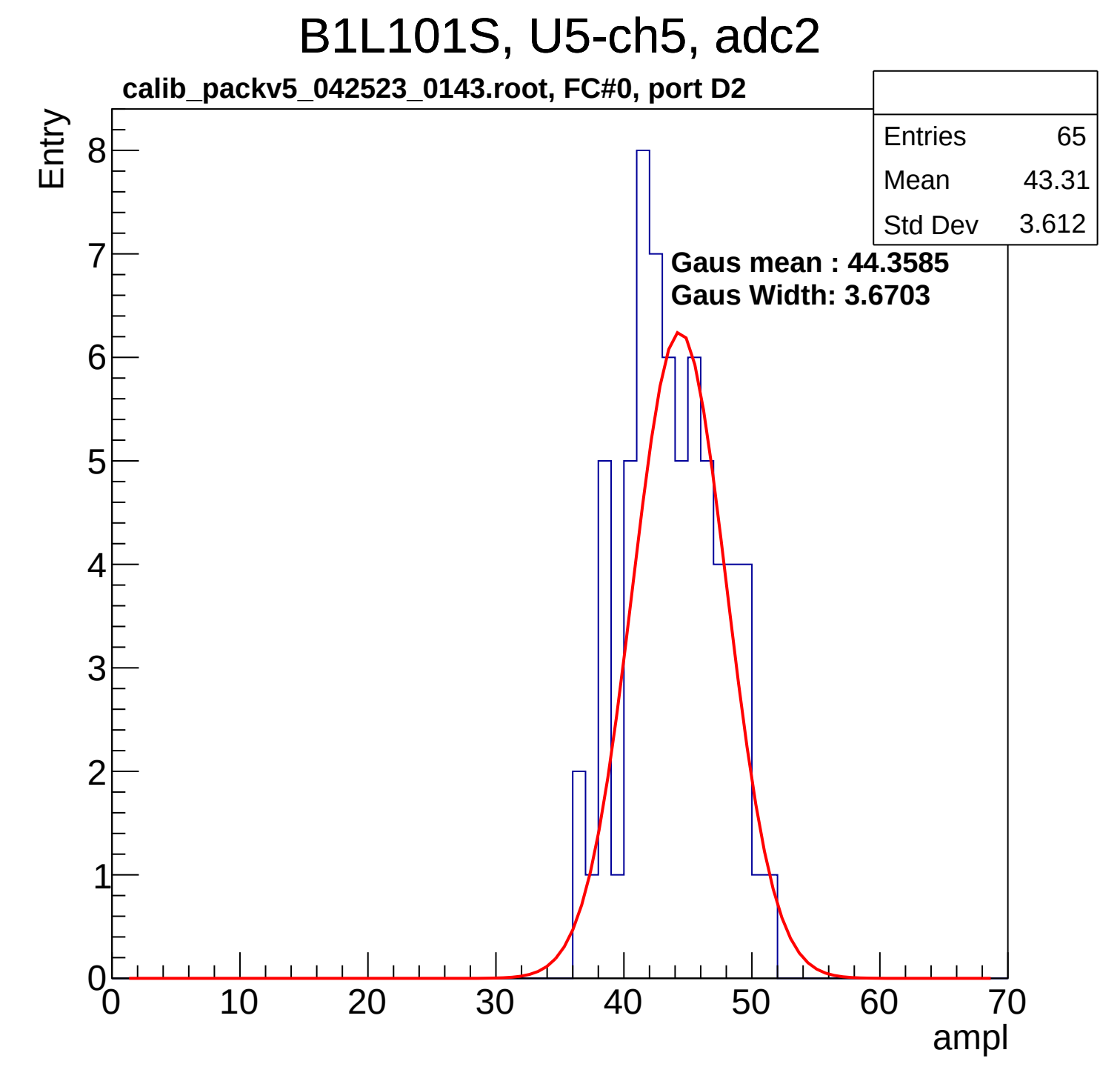
B1L101S, U5-ch5, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 43.31
Std Dev 3.612
Gaus mean : 44.3585
Gaus Width: 3.6703
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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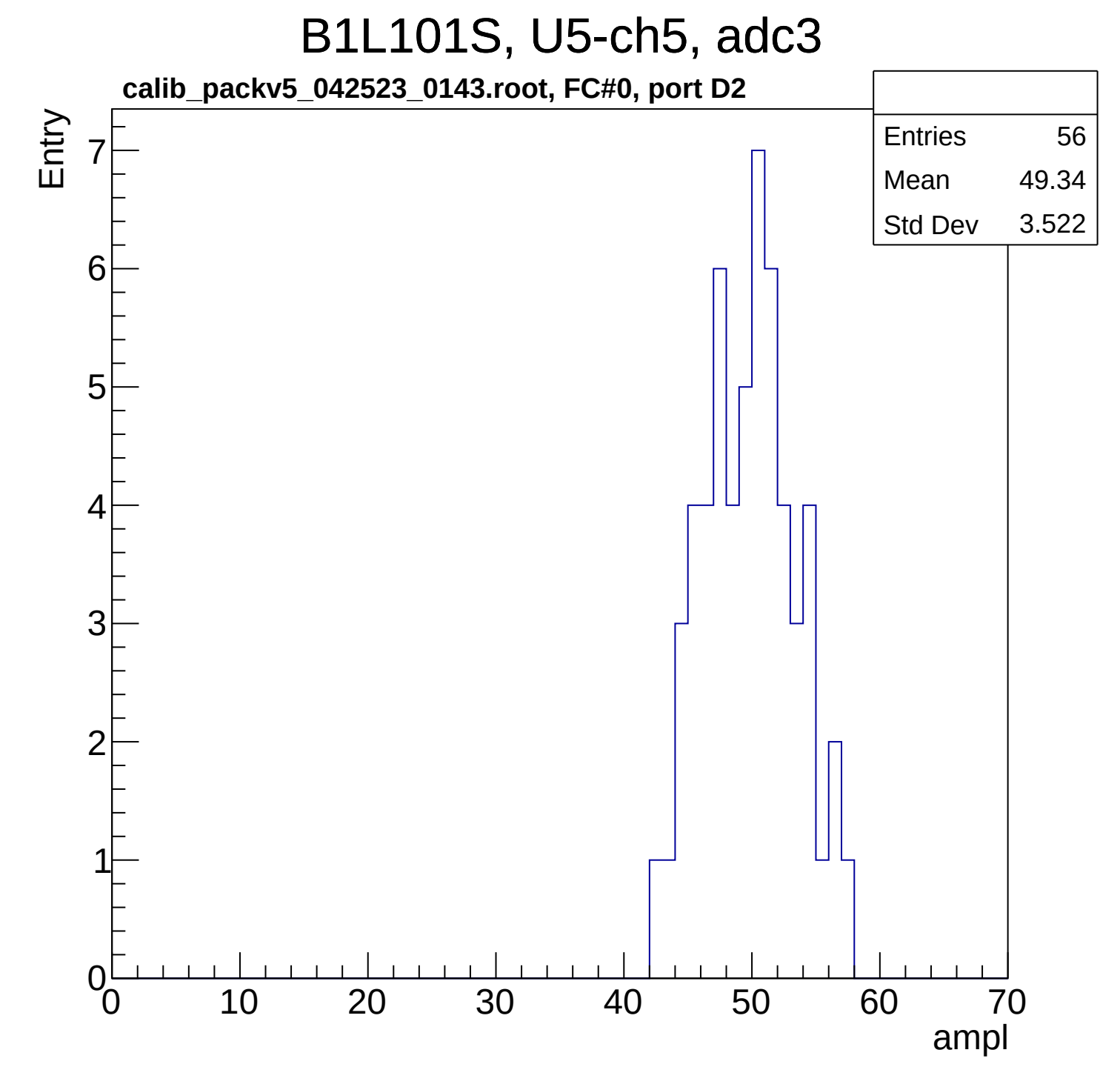
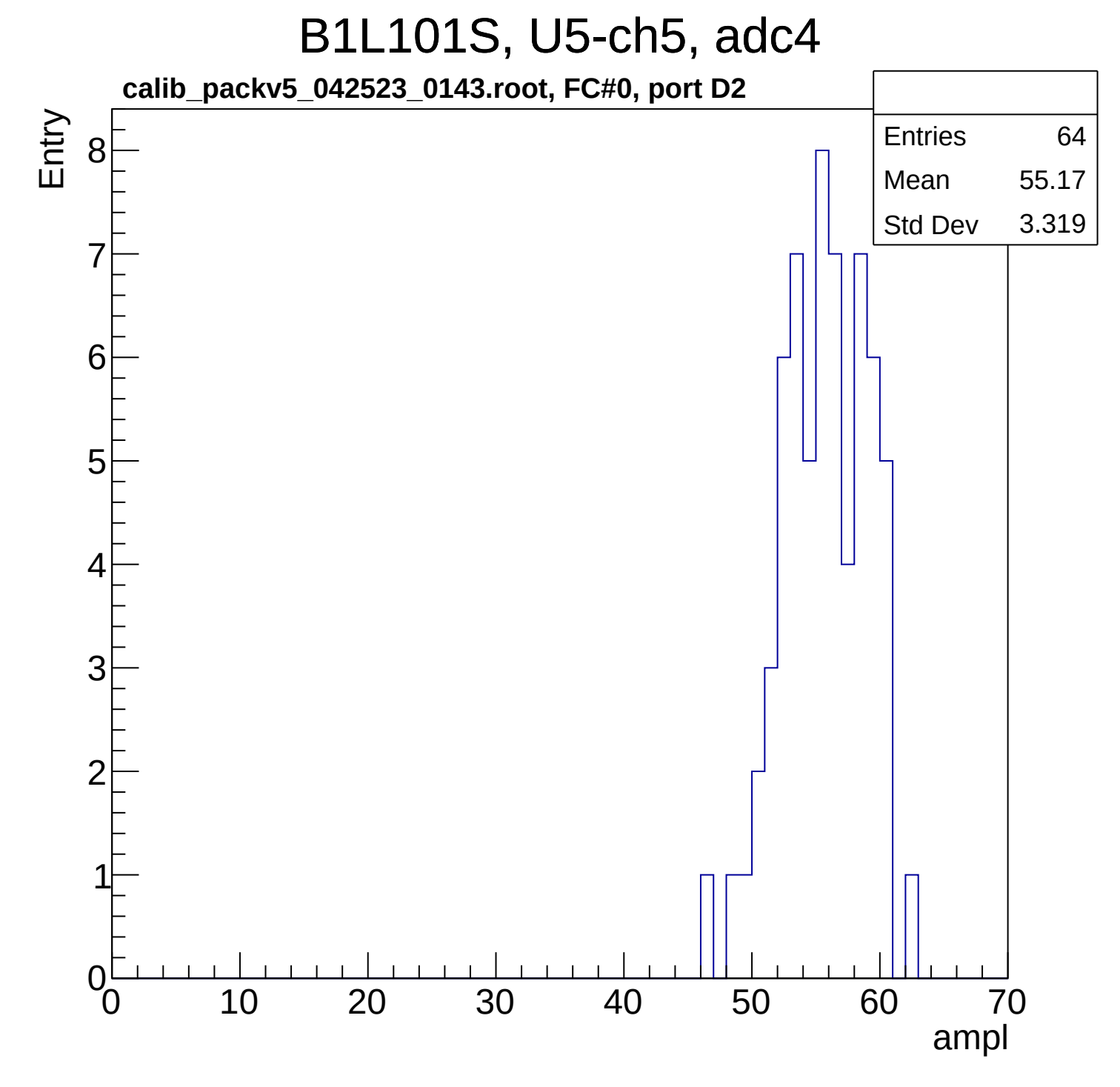

B1L101S, U5-ch5, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 49.34
Std Dev 3.522
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch5, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 55.17
Std Dev 3.319
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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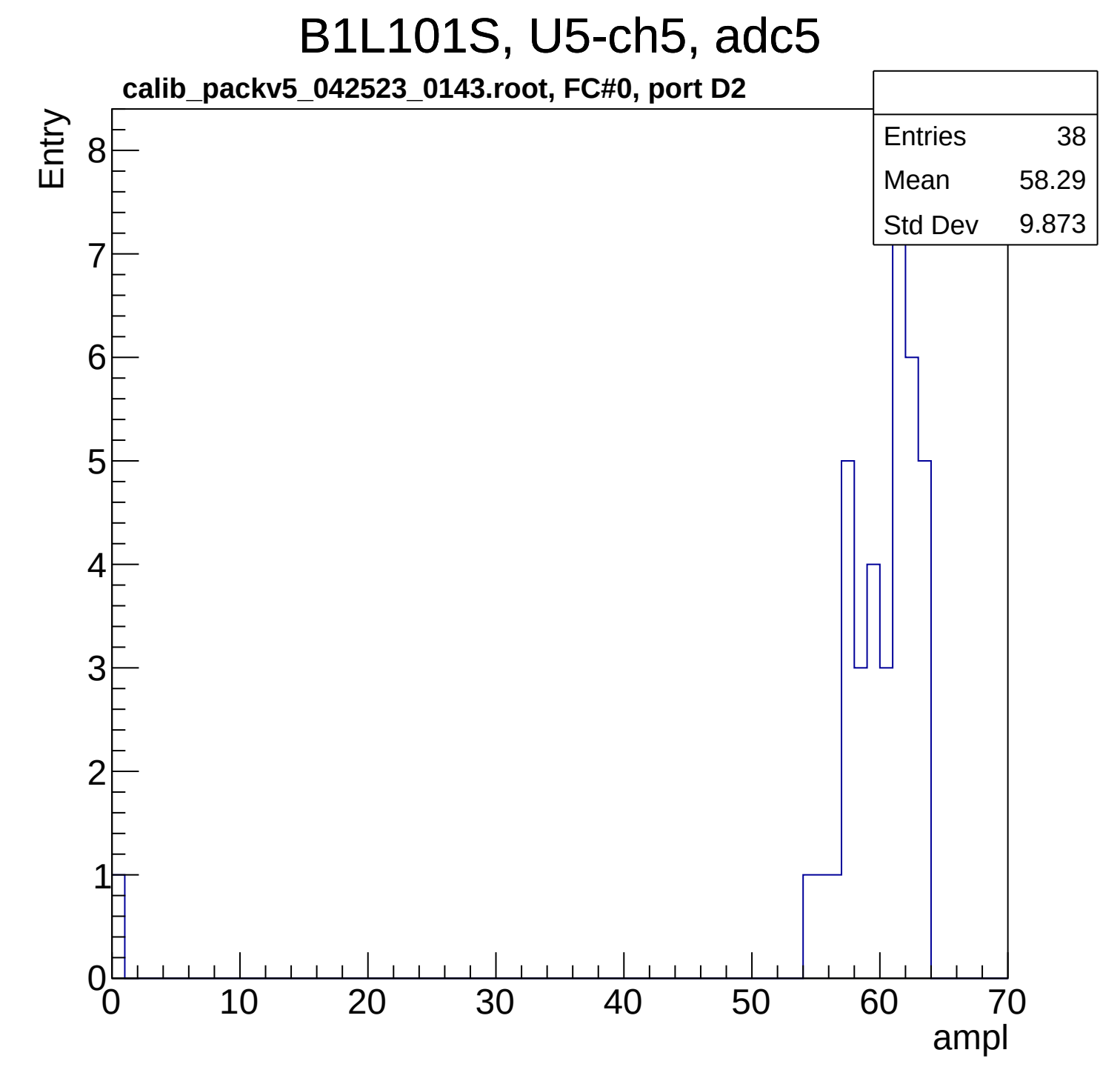
B1L101S, U5-ch5, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 38
Mean 58.29
Std Dev 9.873
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
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60
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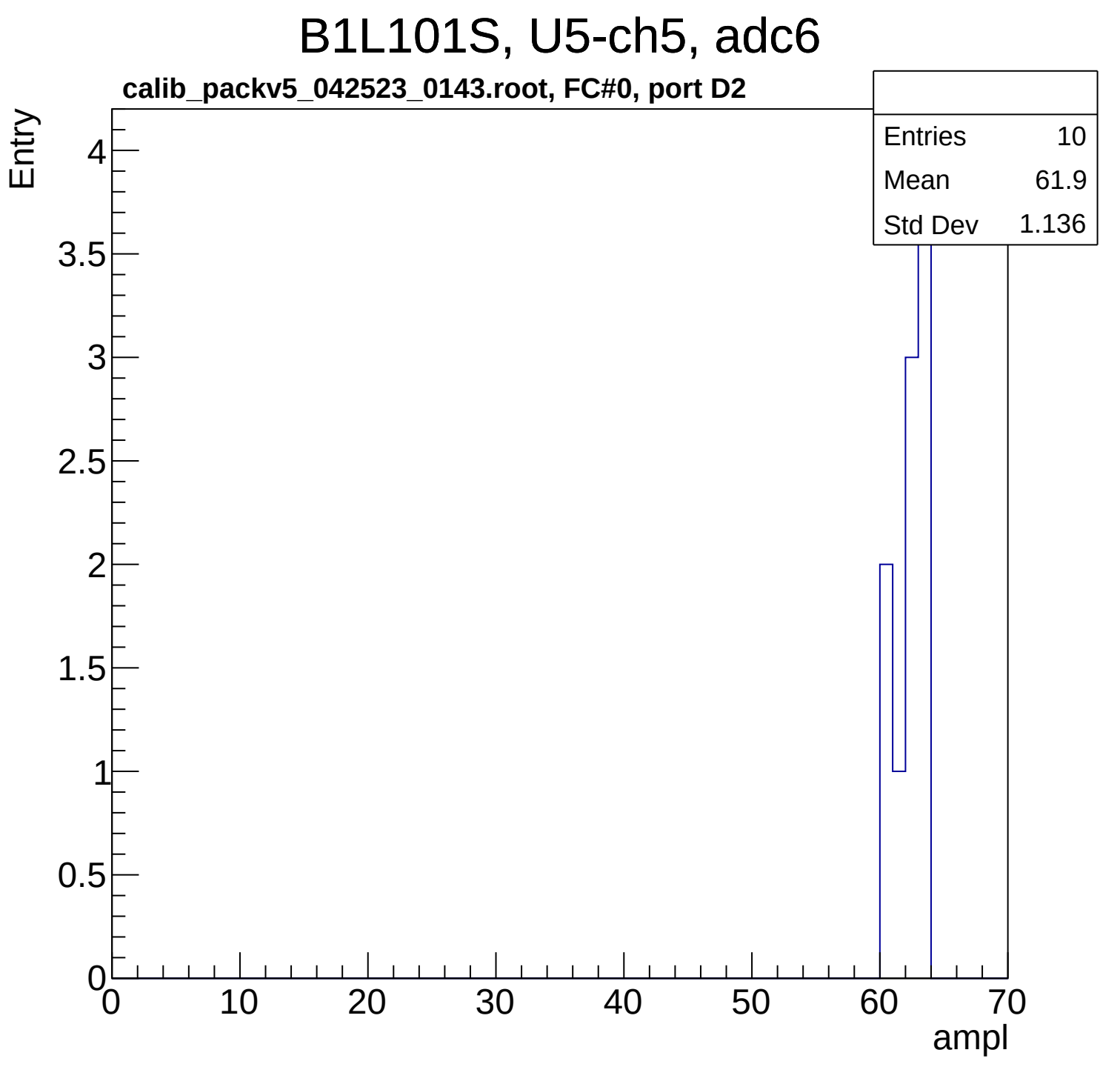
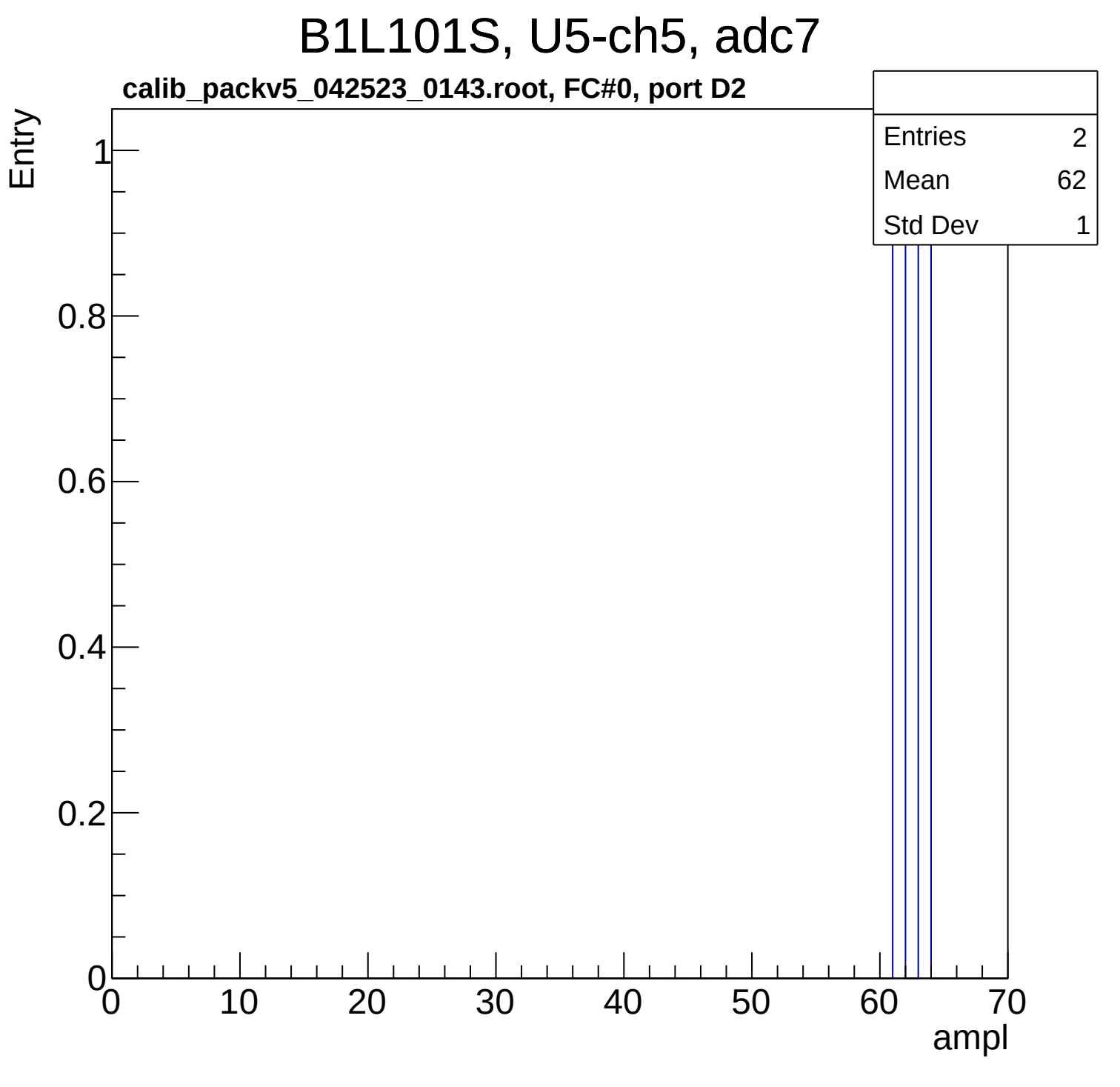
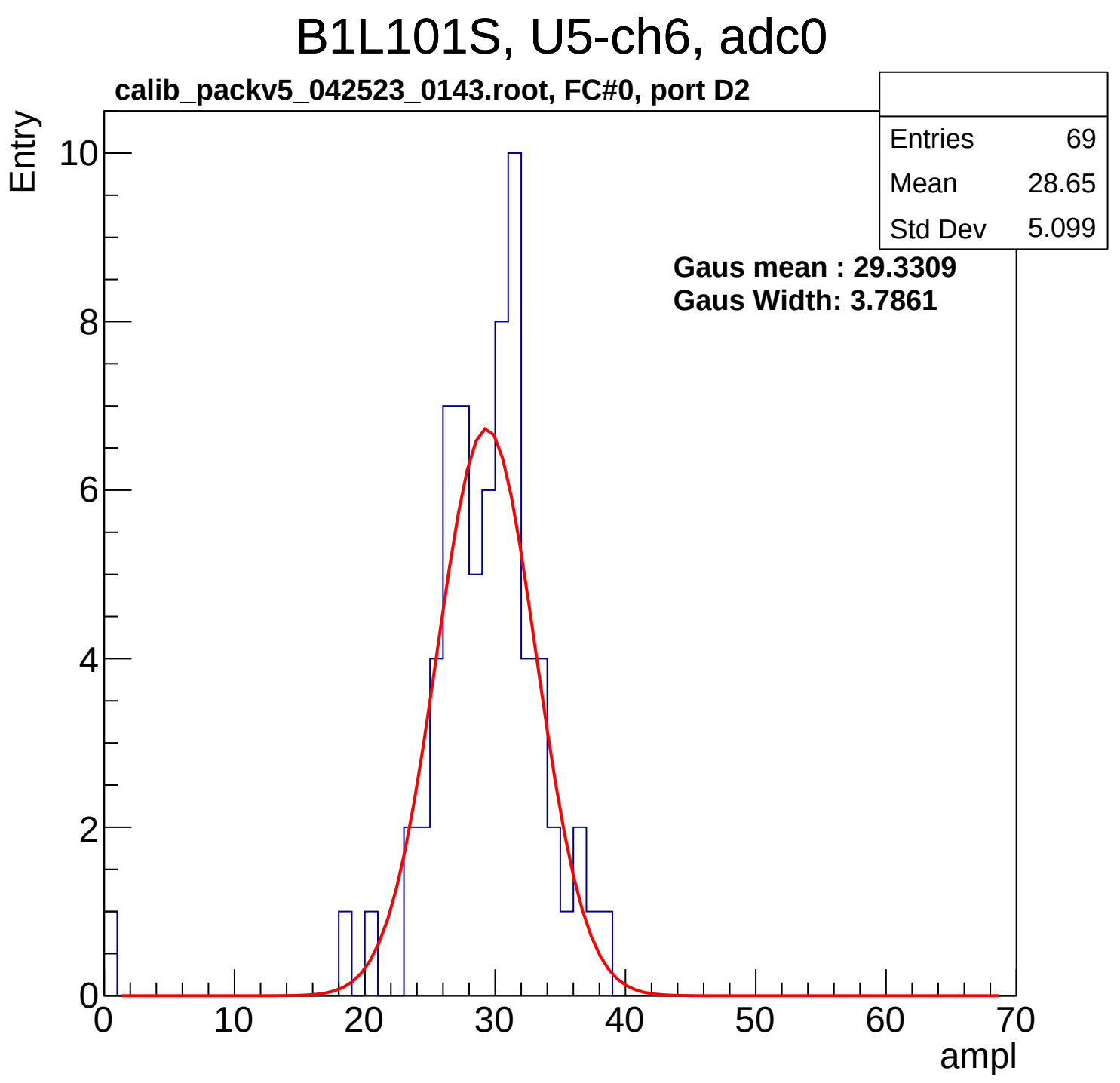
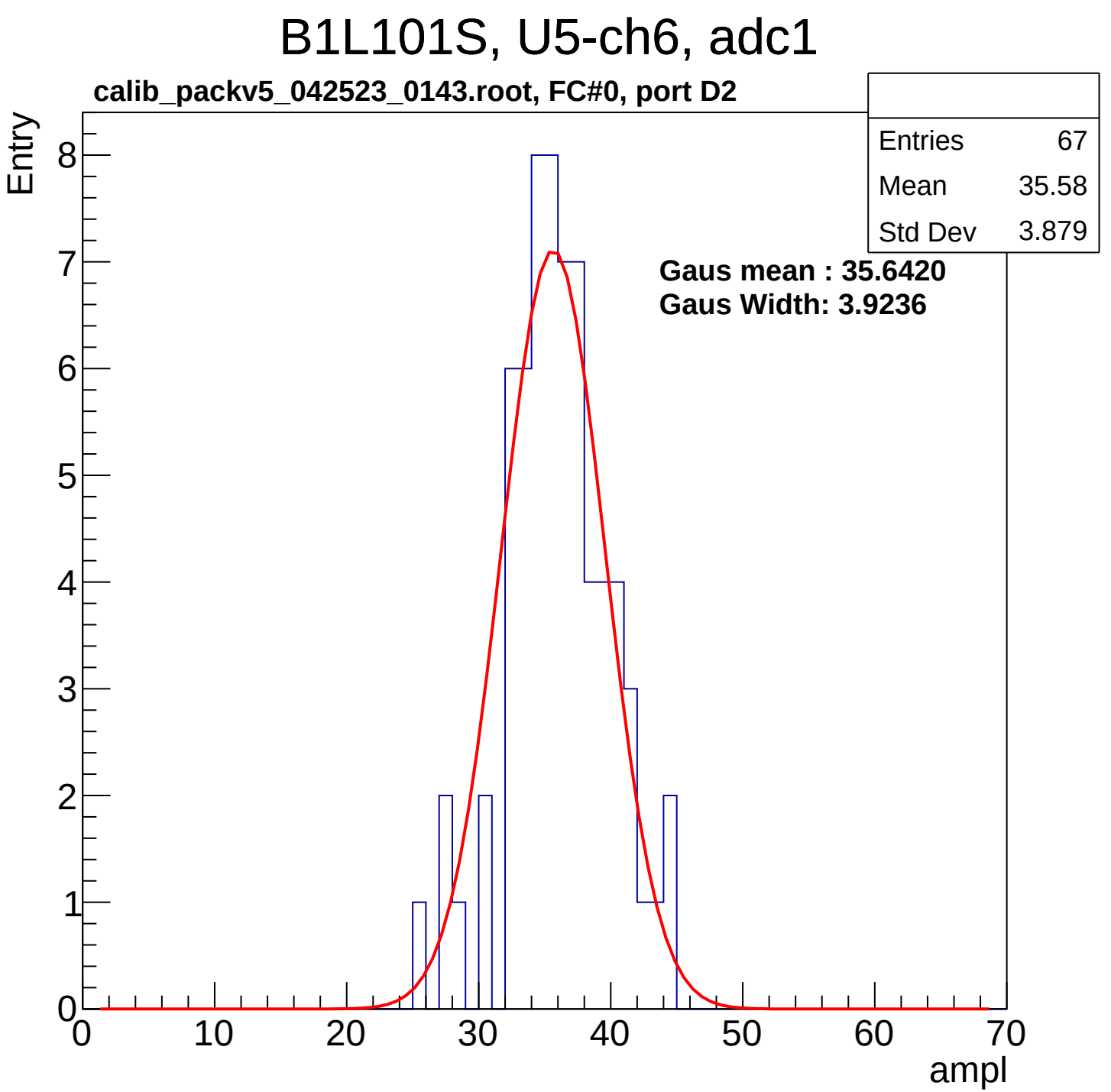
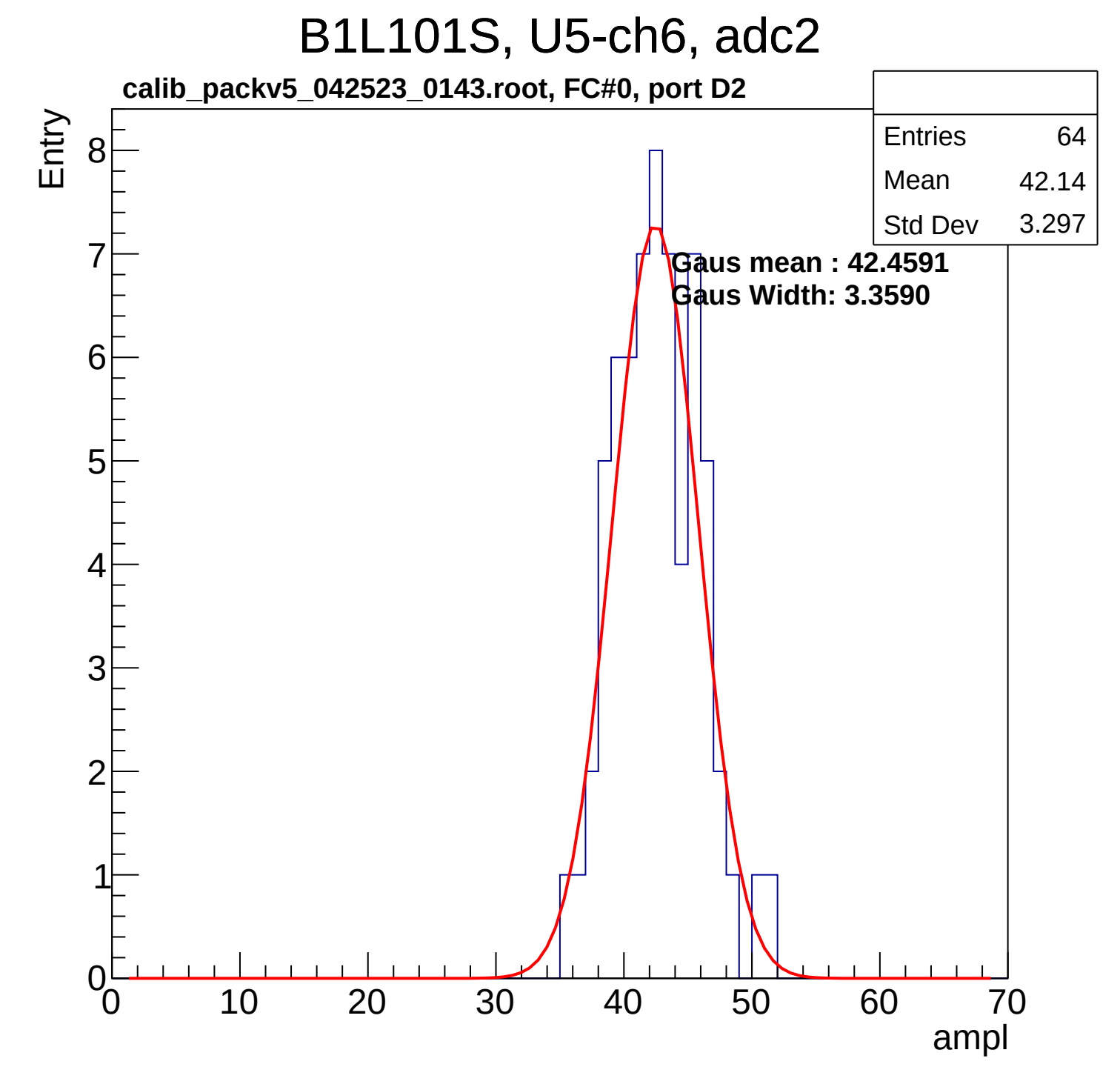

B1L101S, U5-ch5, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 61.9
Std Dev 1.136
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L101S, U5-ch5, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 62
Std Dev 1
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch6, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 28.65
Std Dev 5.099
Gaus mean : 29.3309
Gaus Width: 3.7861
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch6, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 35.58
Std Dev 3.879
Gaus mean : 35.6420
Gaus Width: 3.9236
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch6, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 42.14
Std Dev 3.297
Gaus mean : 42.4591
Gaus Width: 3.3590
Entry
ampl
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1
2
3
4
5
6
7
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0
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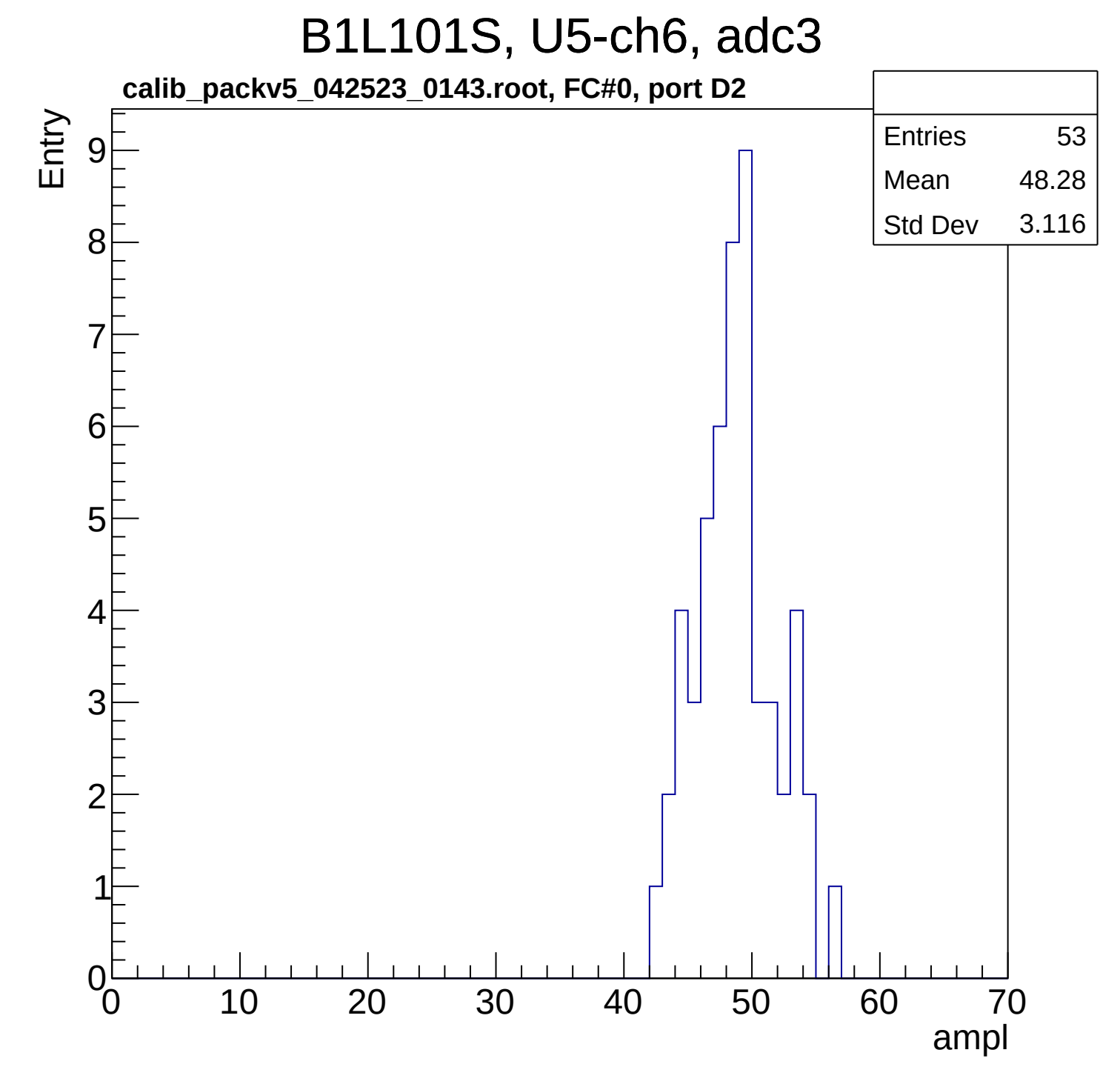
B1L101S, U5-ch6, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 48.28
Std Dev 3.116
Entry
ampl
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3
4
5
6
7
8
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0
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20
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40
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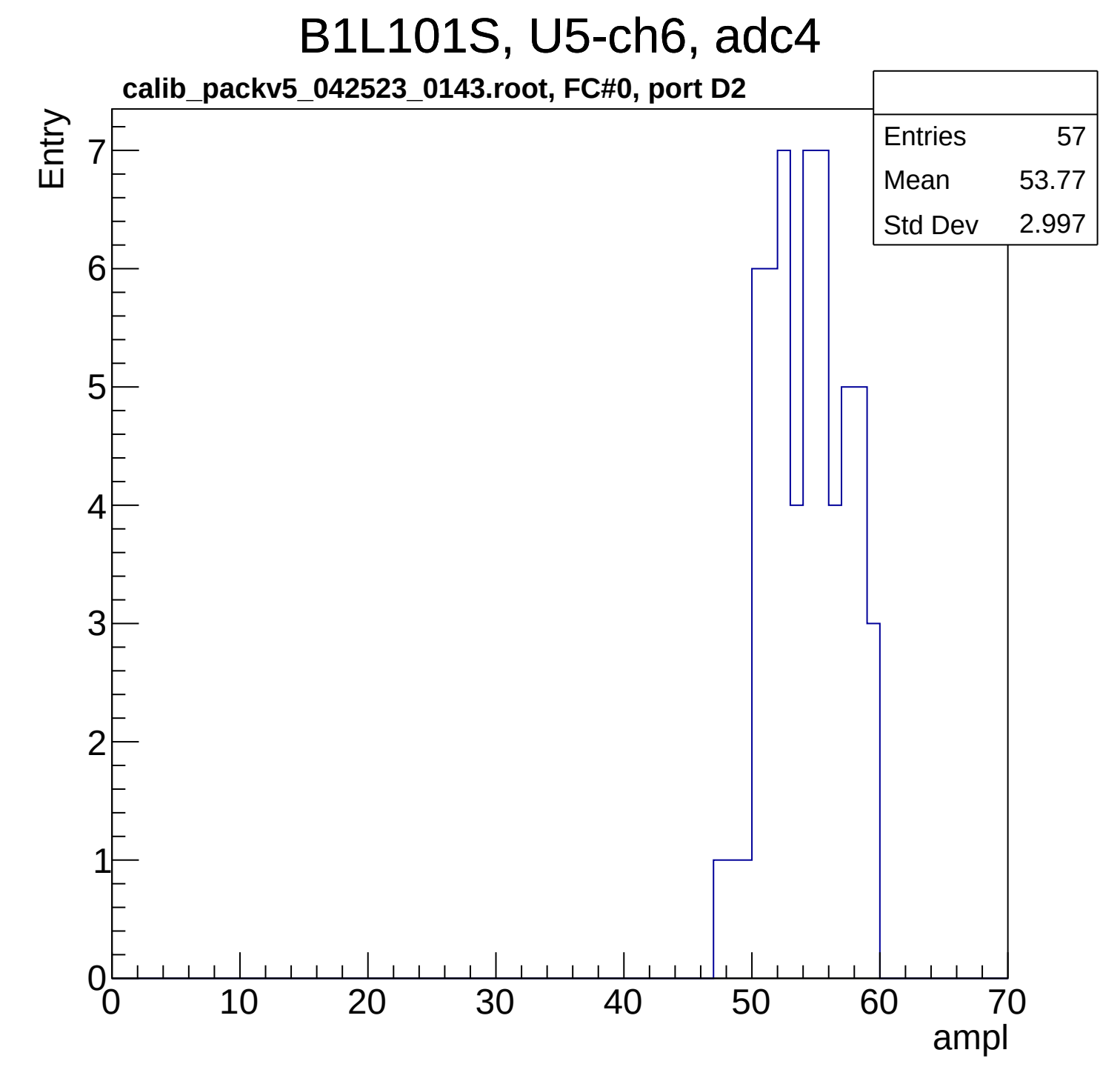
60
70


B1L101S, U5-ch6, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 53.77
Std Dev 2.997
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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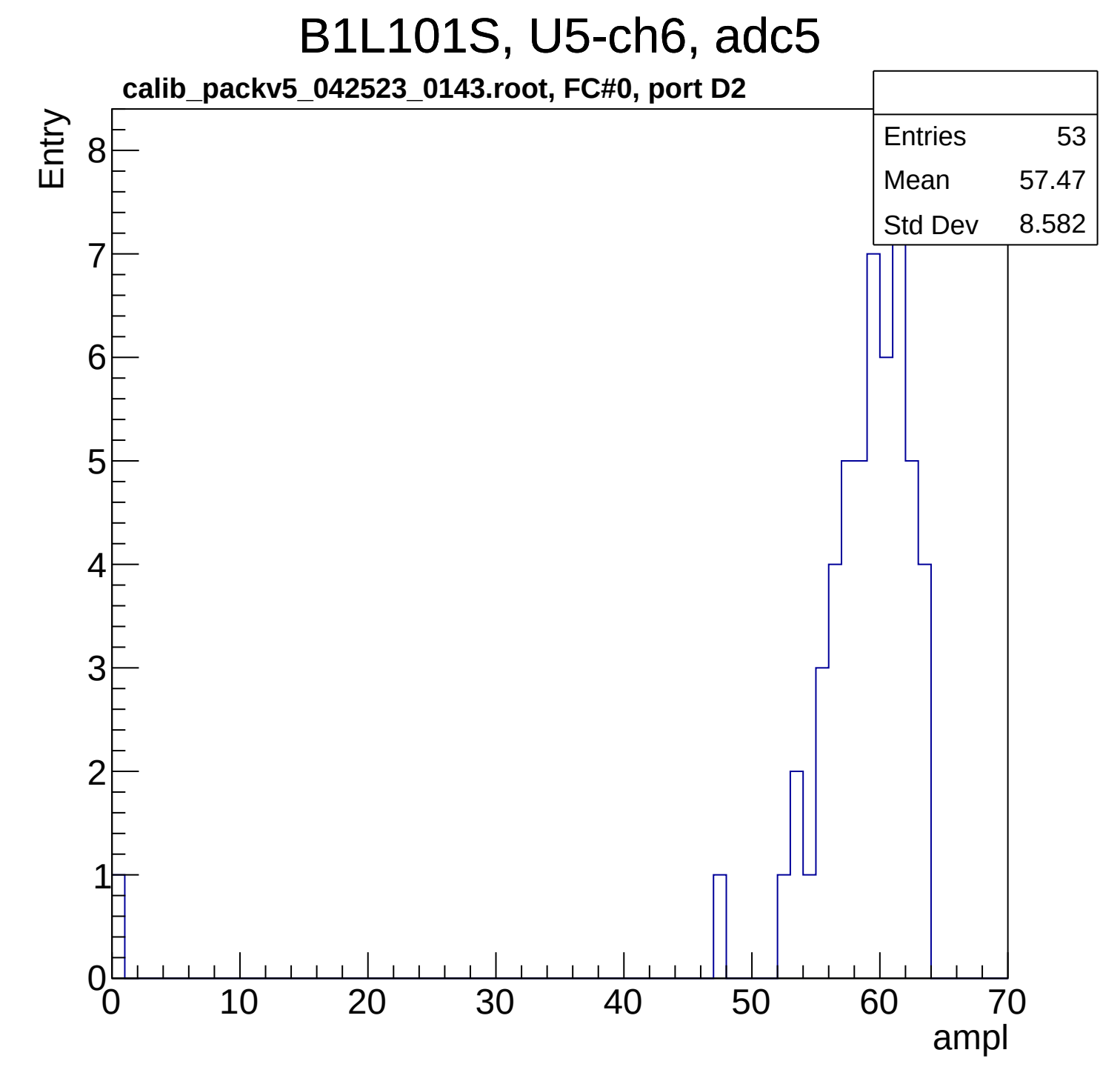
40
50
60
70


B1L101S, U5-ch6, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 57.47
Std Dev 8.582
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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40
50
60
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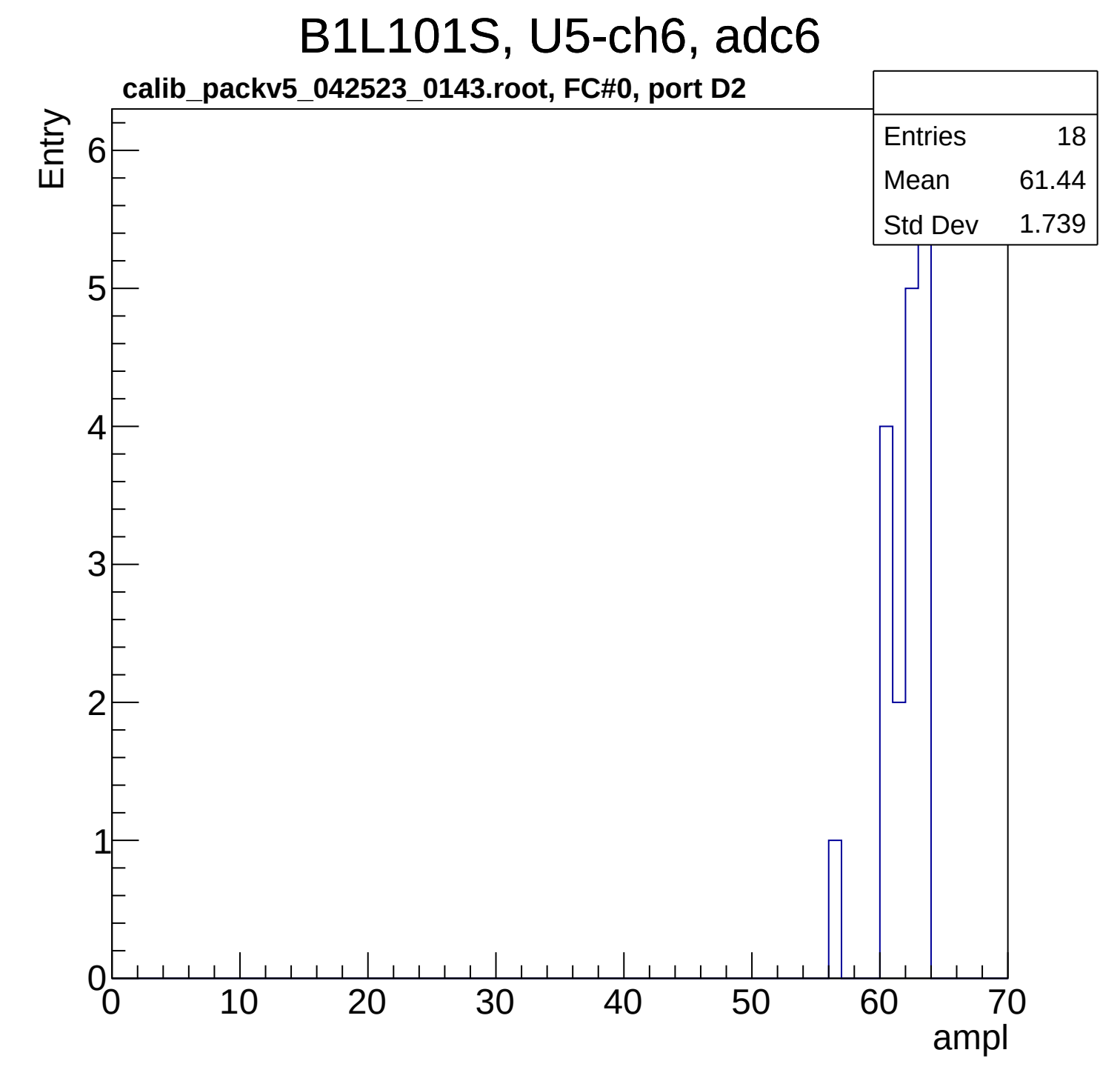
B1L101S, U5-ch6, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 18
Mean 61.44
Std Dev 1.739
Entry
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1
2
3
4
5
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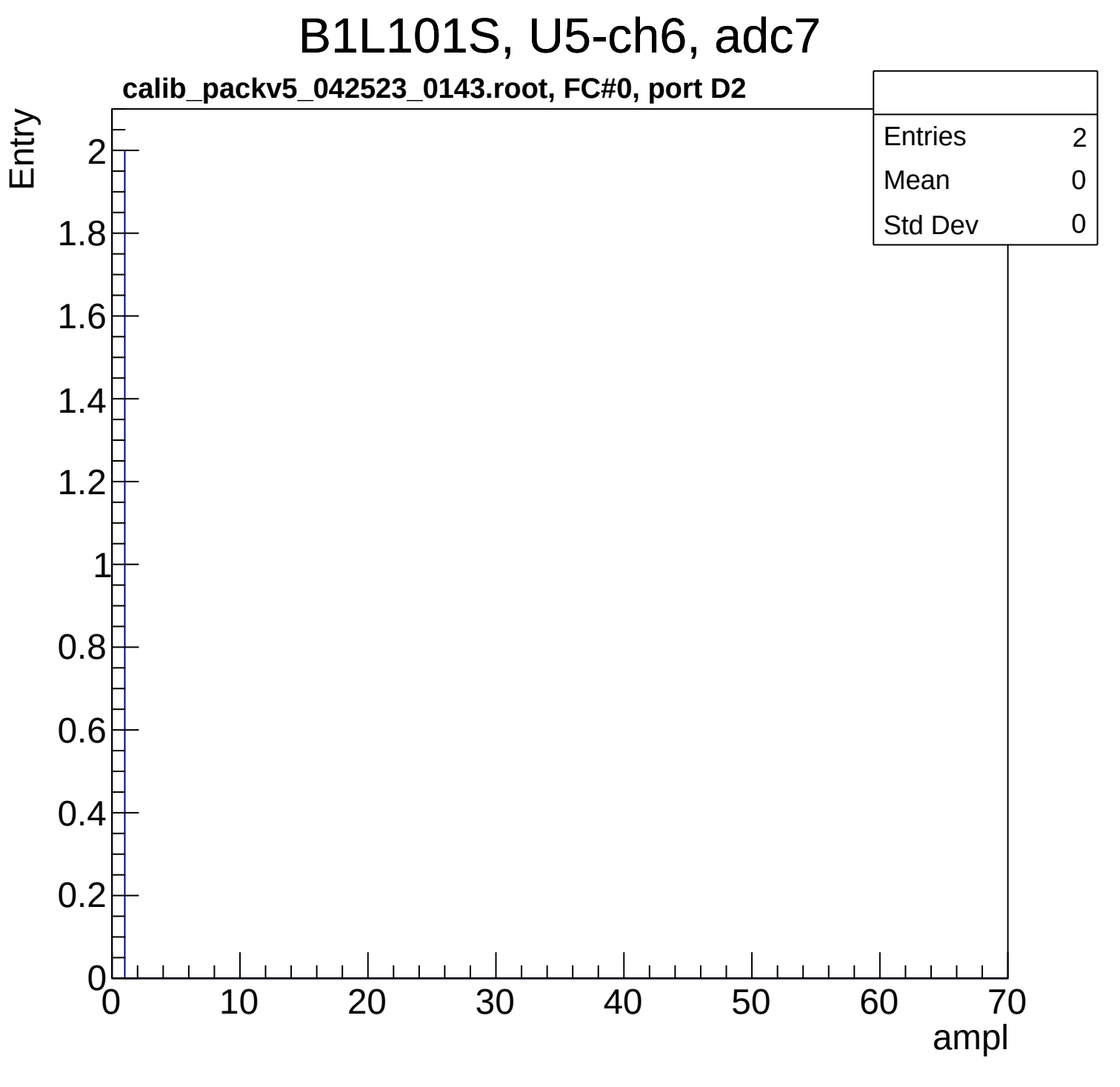
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch6, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
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1.2
1.4
1.6
1.8
2
0
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60
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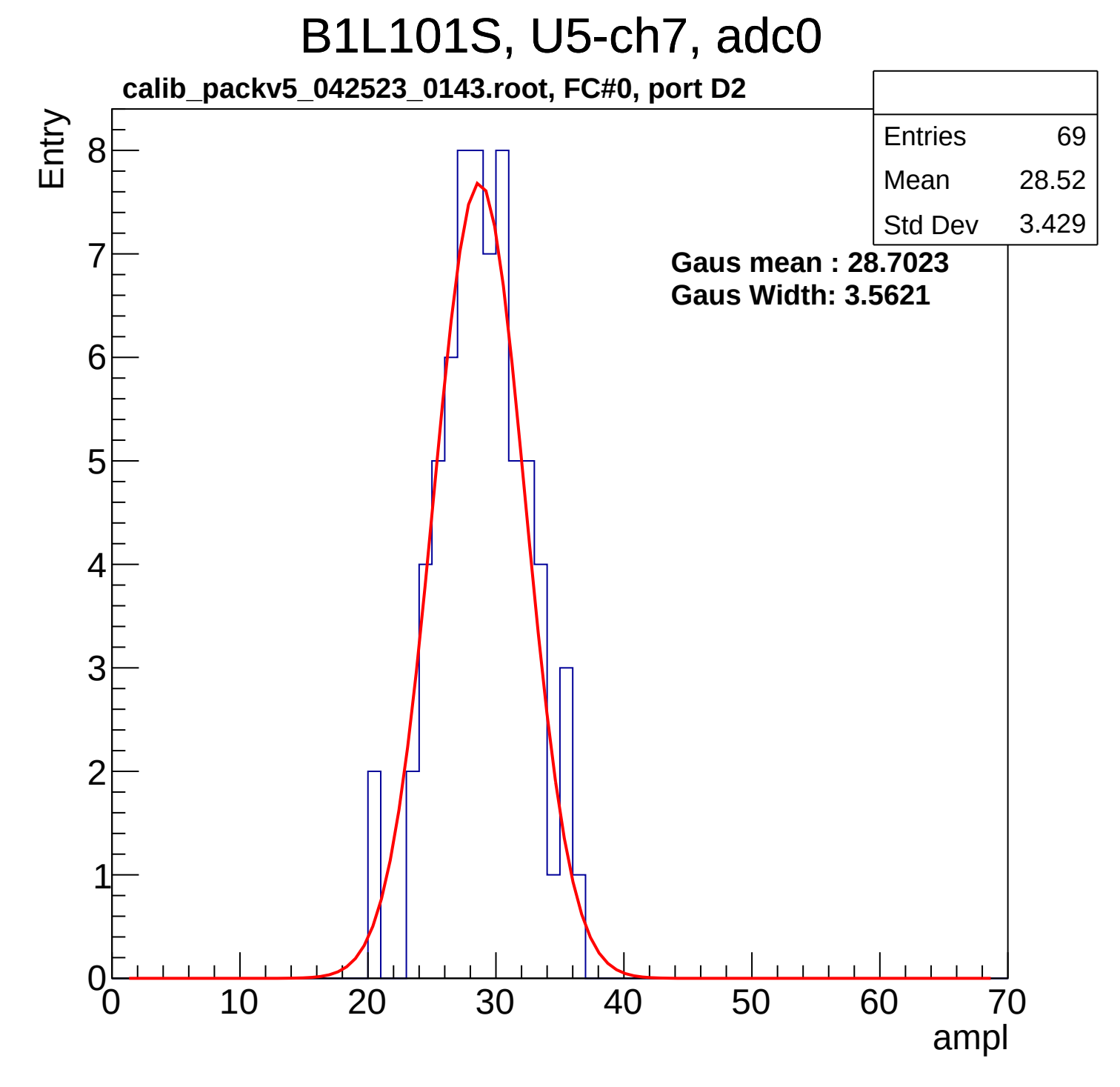
B1L101S, U5-ch7, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 28.52
Std Dev 3.429
Gaus mean : 28.7023
Gaus Width: 3.5621
Entry
ampl
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1
2
3
4
5
6
7
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0
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60
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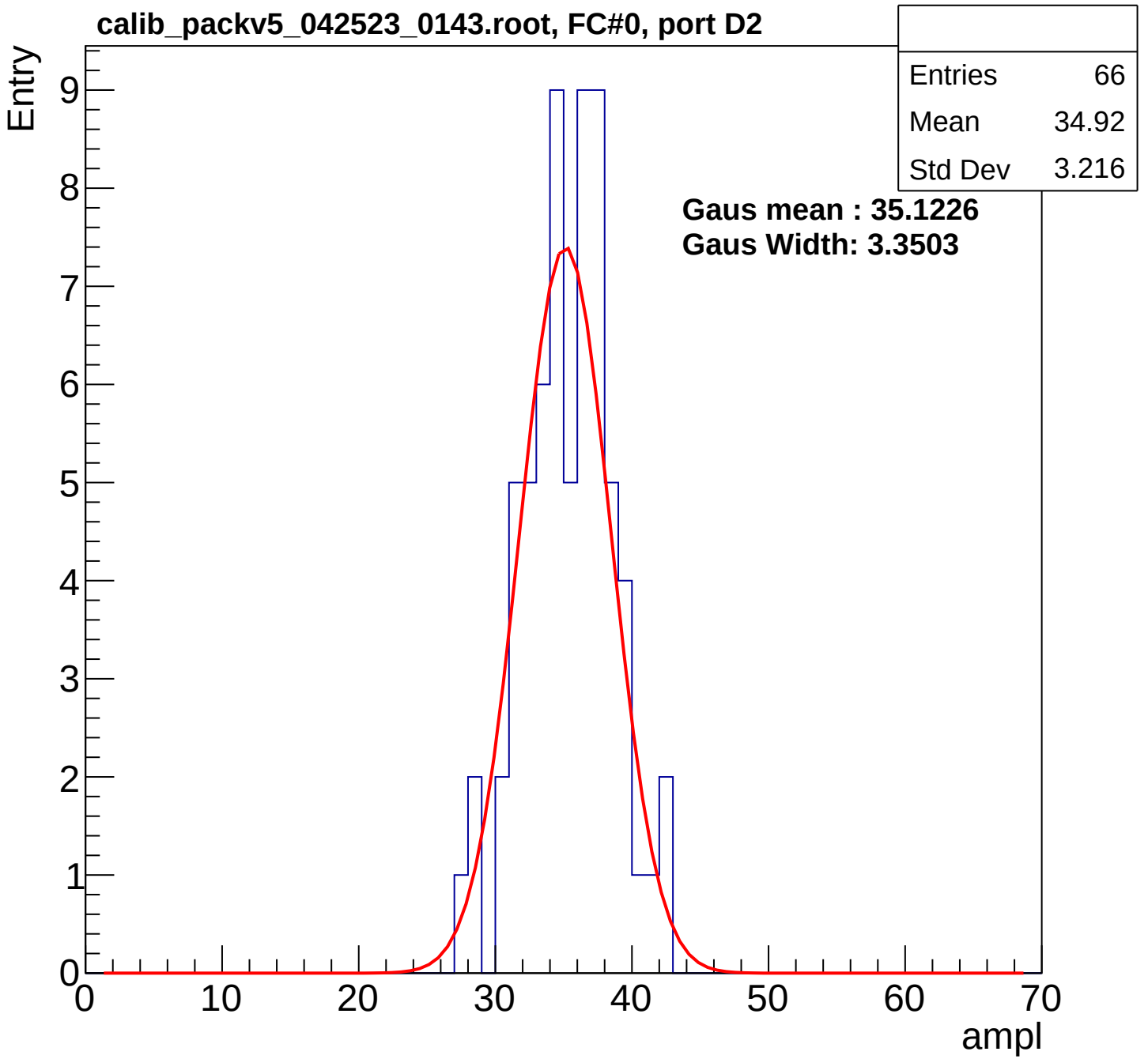
B1L101S, U5-ch7, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 34.92
Std Dev 3.216
Gaus mean : 35.1226
Gaus Width: 3.3503
Entry
ampl
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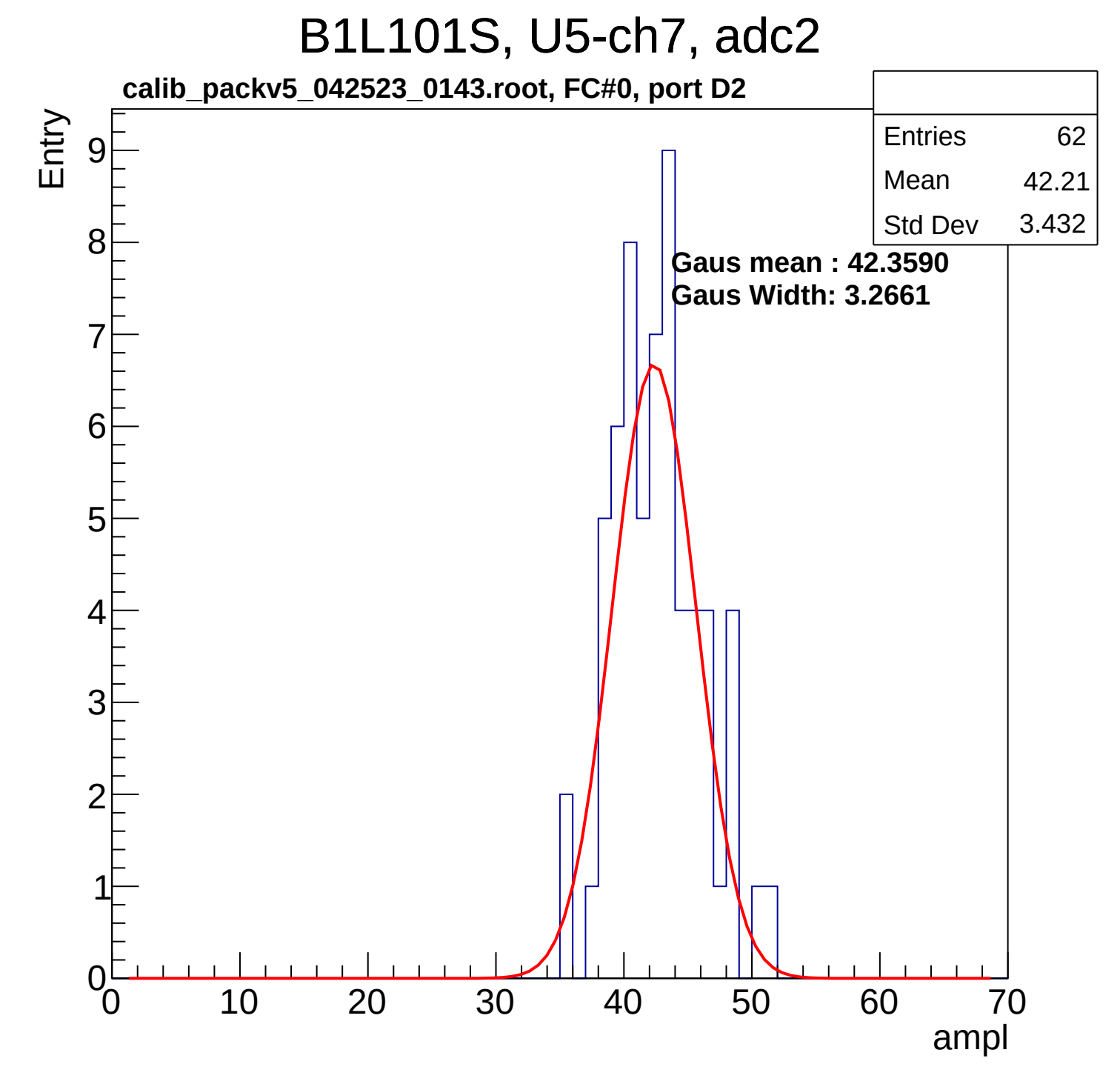
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch7, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 42.21
Std Dev 3.432
Gaus mean : 42.3590
Gaus Width: 3.2661
Entry
ampl
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10
20
30
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50
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2
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4
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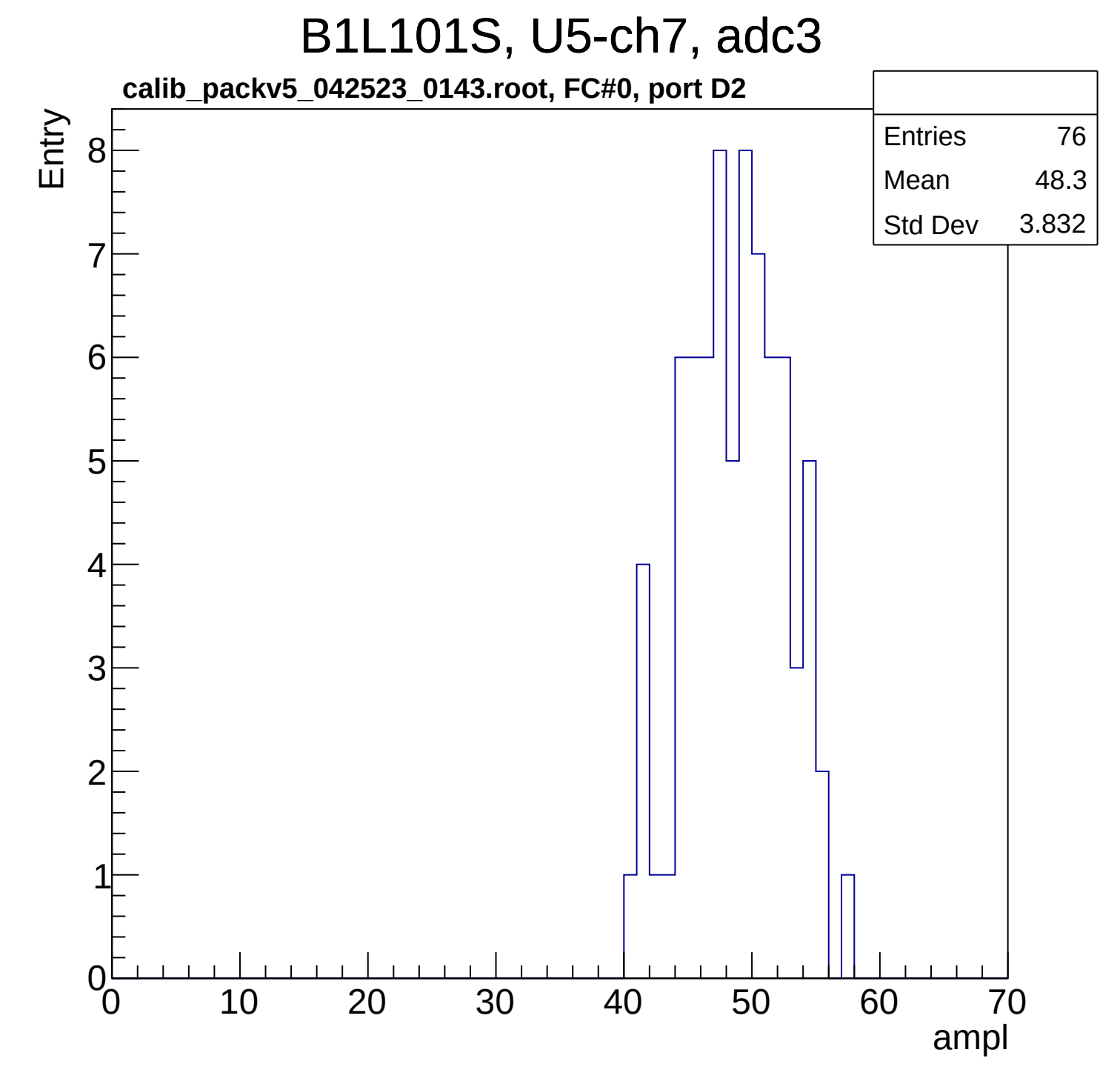
6
7
8
9


B1L101S, U5-ch7, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 48.3
Std Dev 3.832
Entry
ampl
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2
3
4
5
6
7
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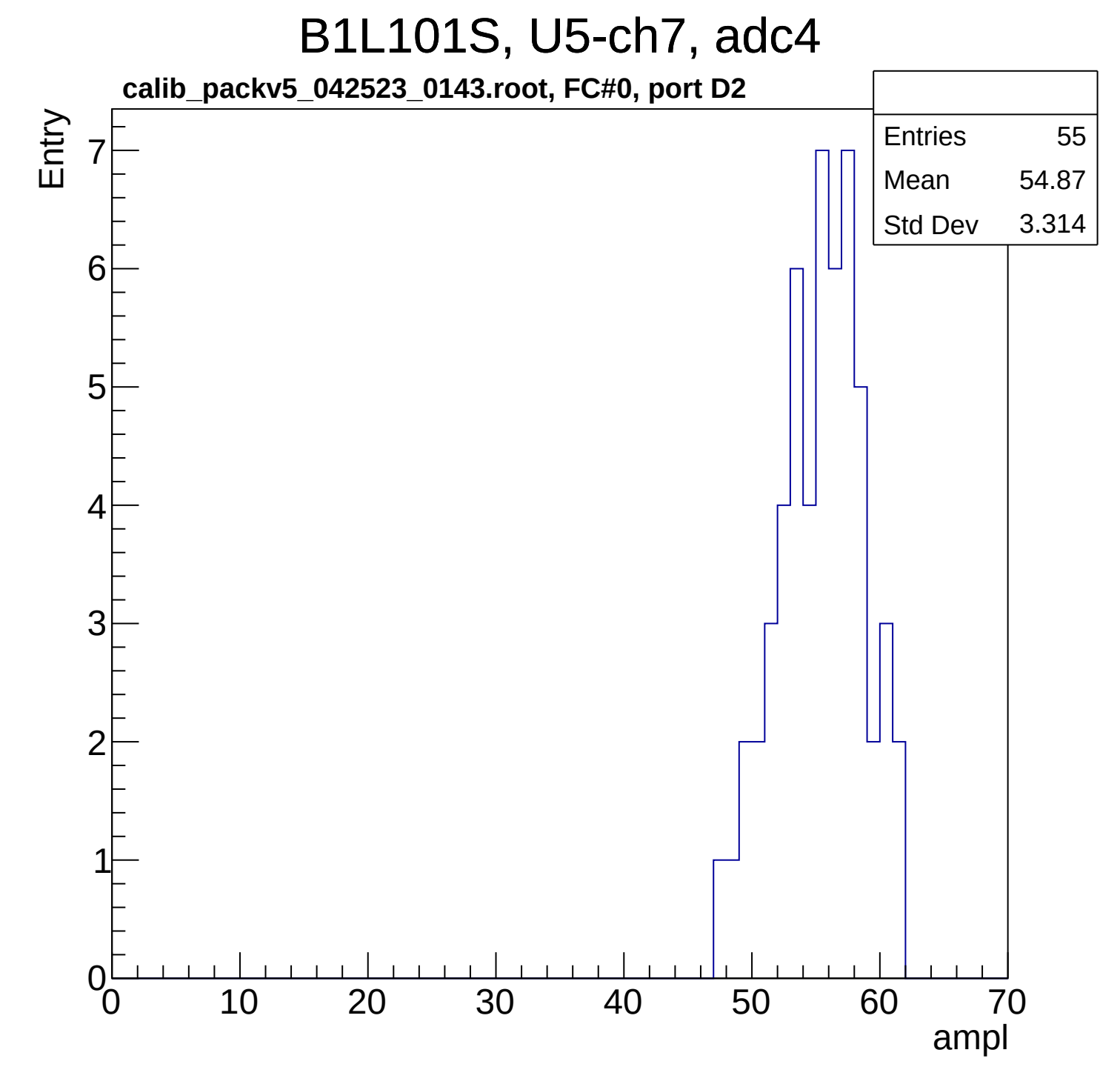
B1L101S, U5-ch7, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 54.87
Std Dev 3.314
Entry
ampl
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2
3
4
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0
10
20
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40
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60
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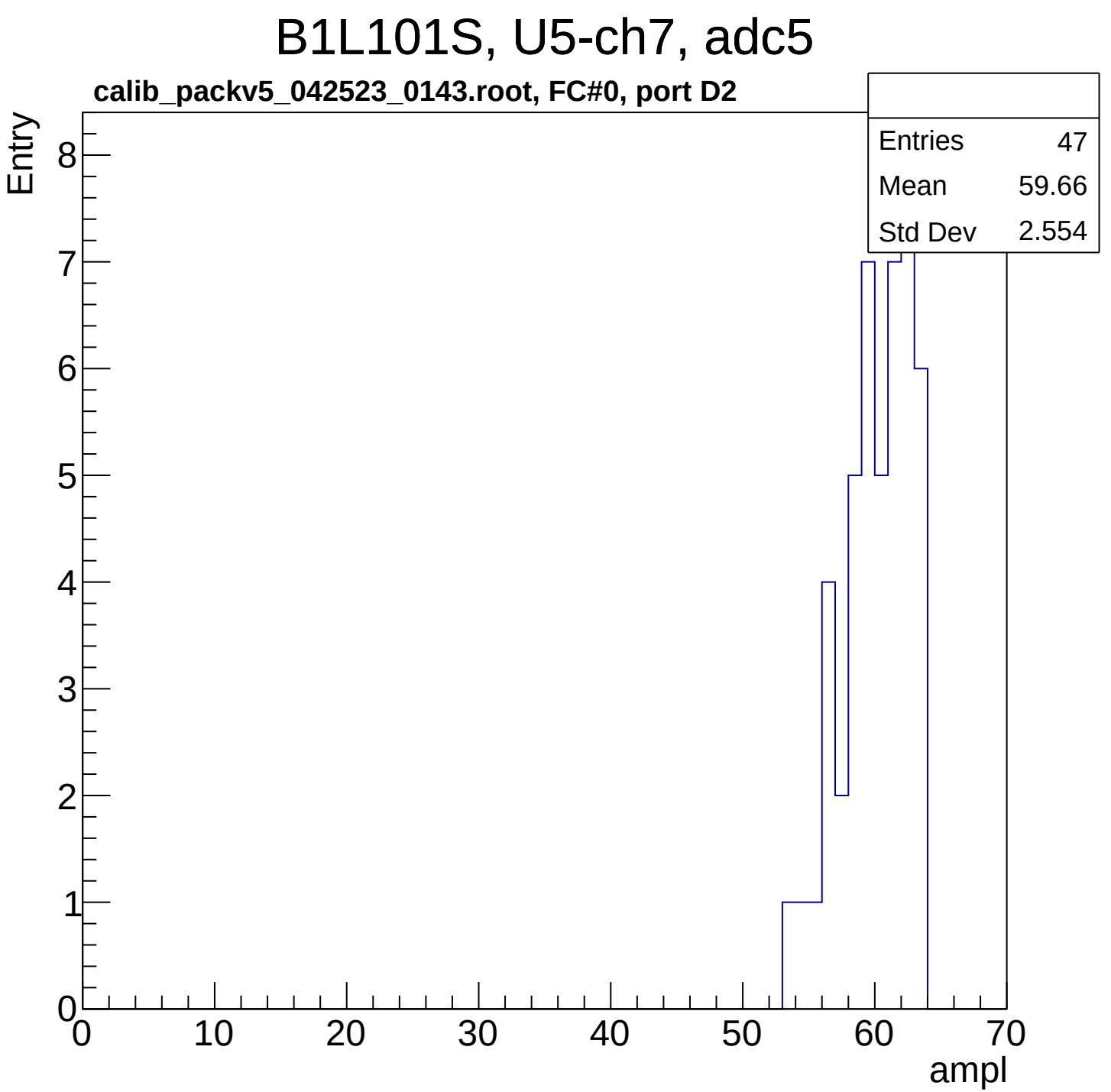
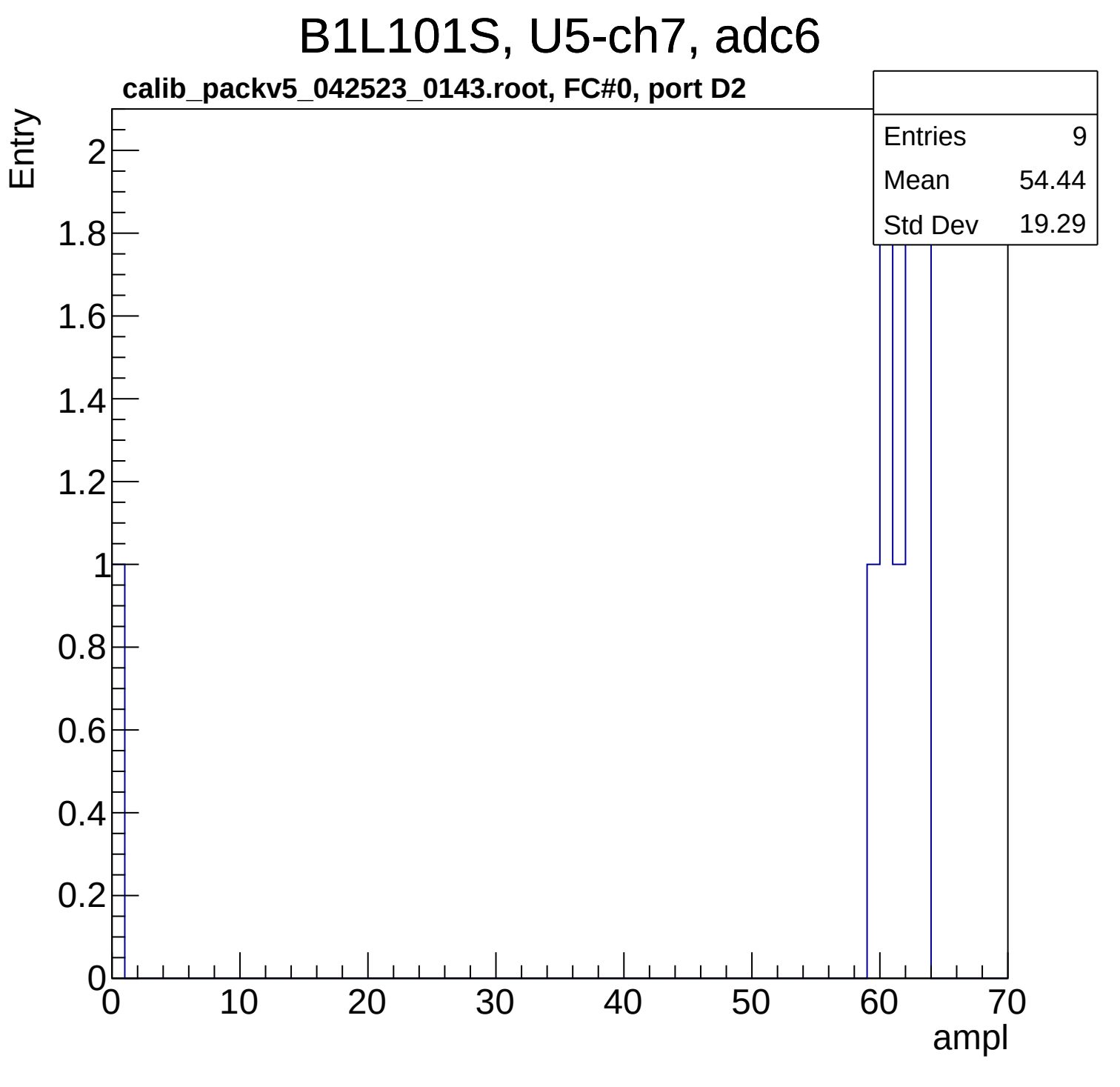

B1L101S, U5-ch7, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 59.66
Std Dev 2.554
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch7, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 54.44
Std Dev 19.29
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
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60
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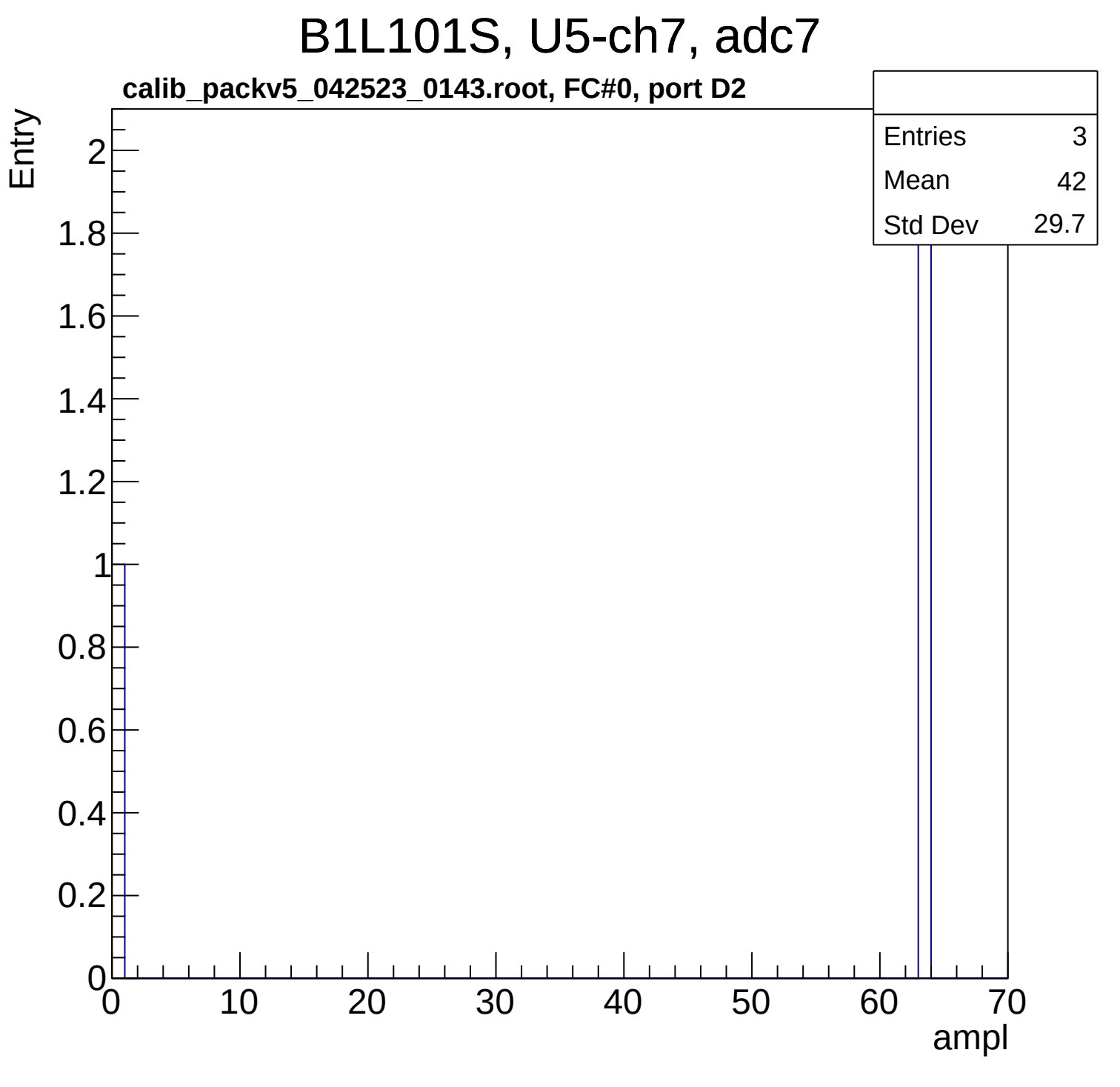
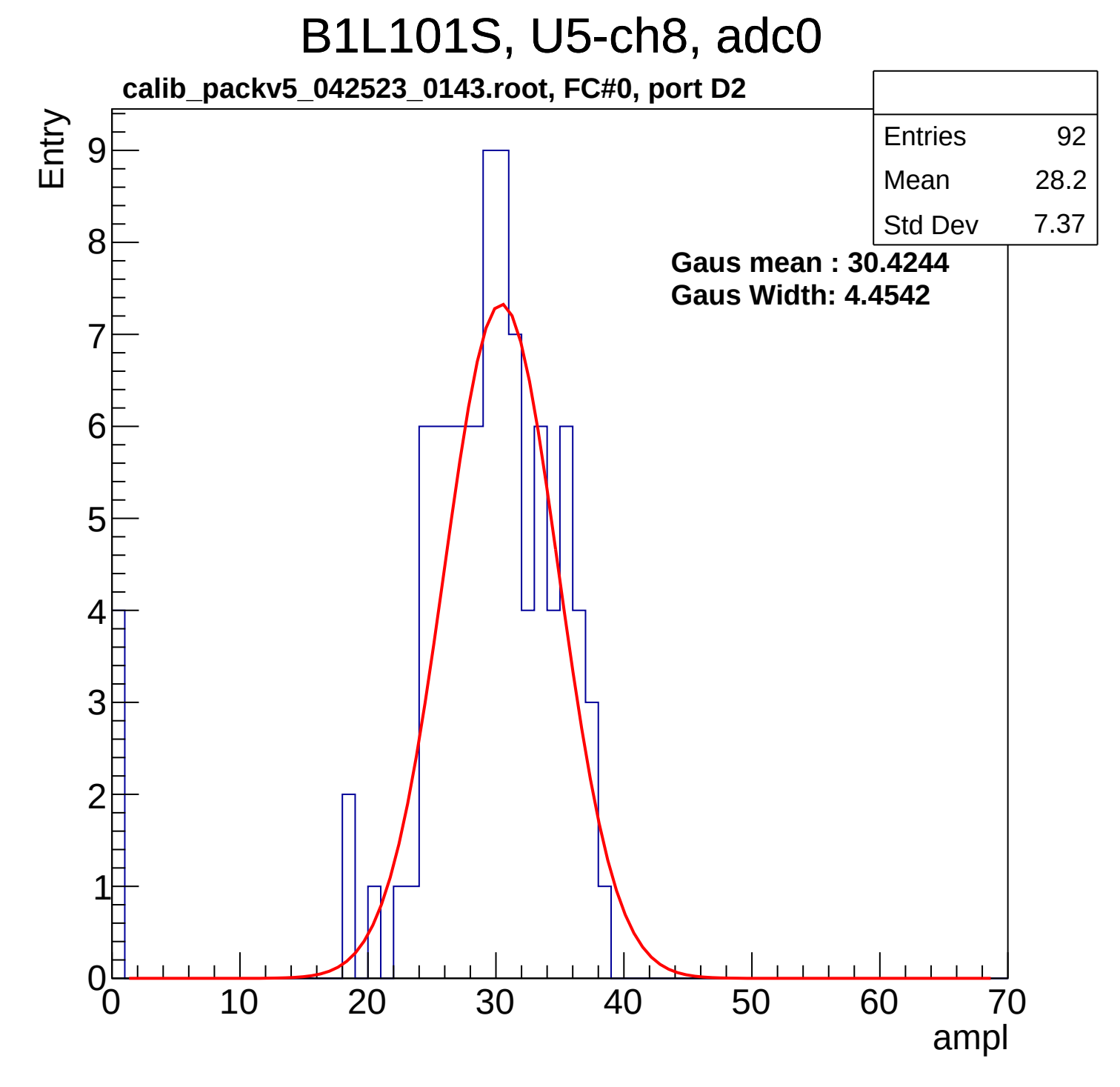
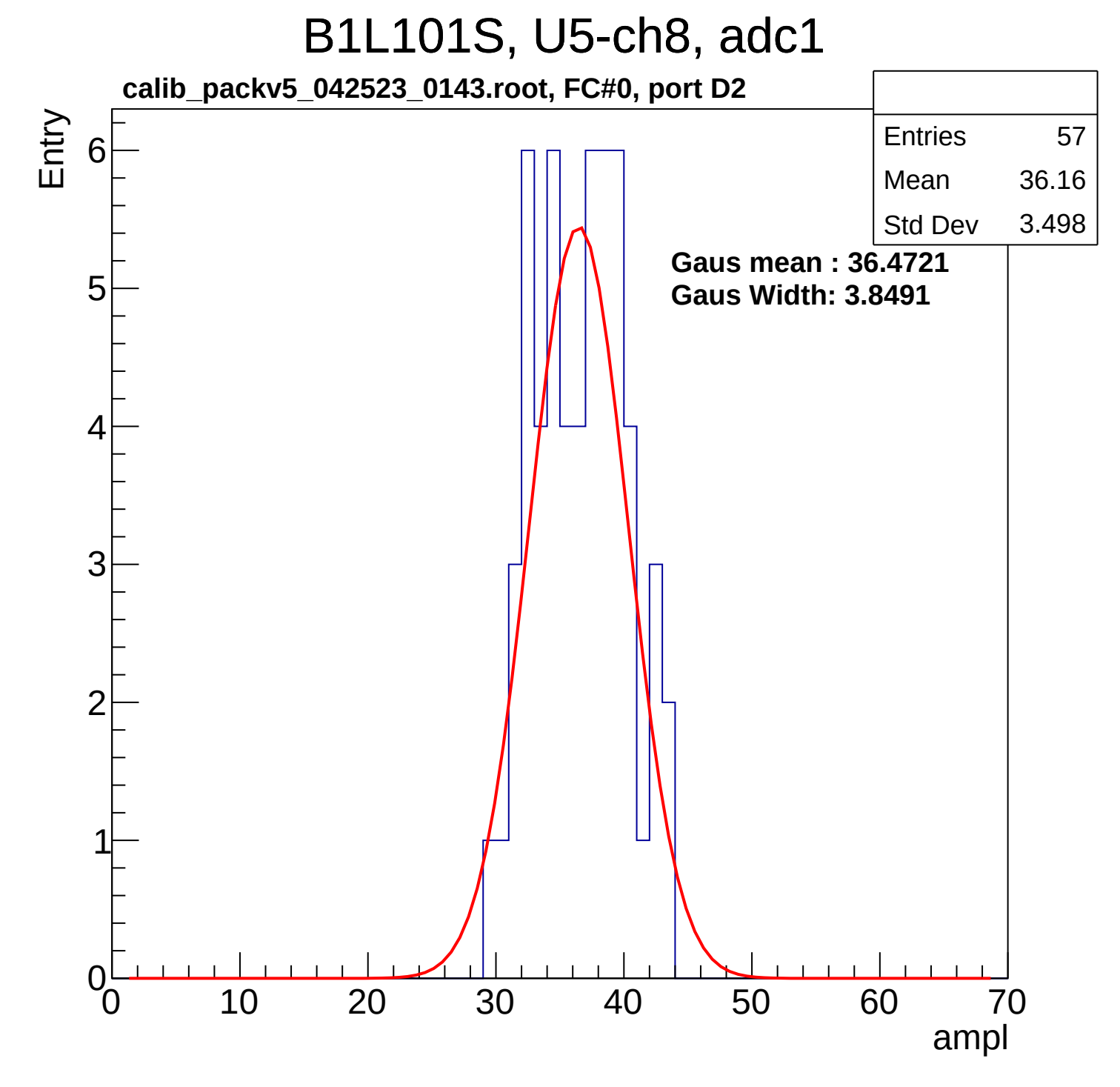
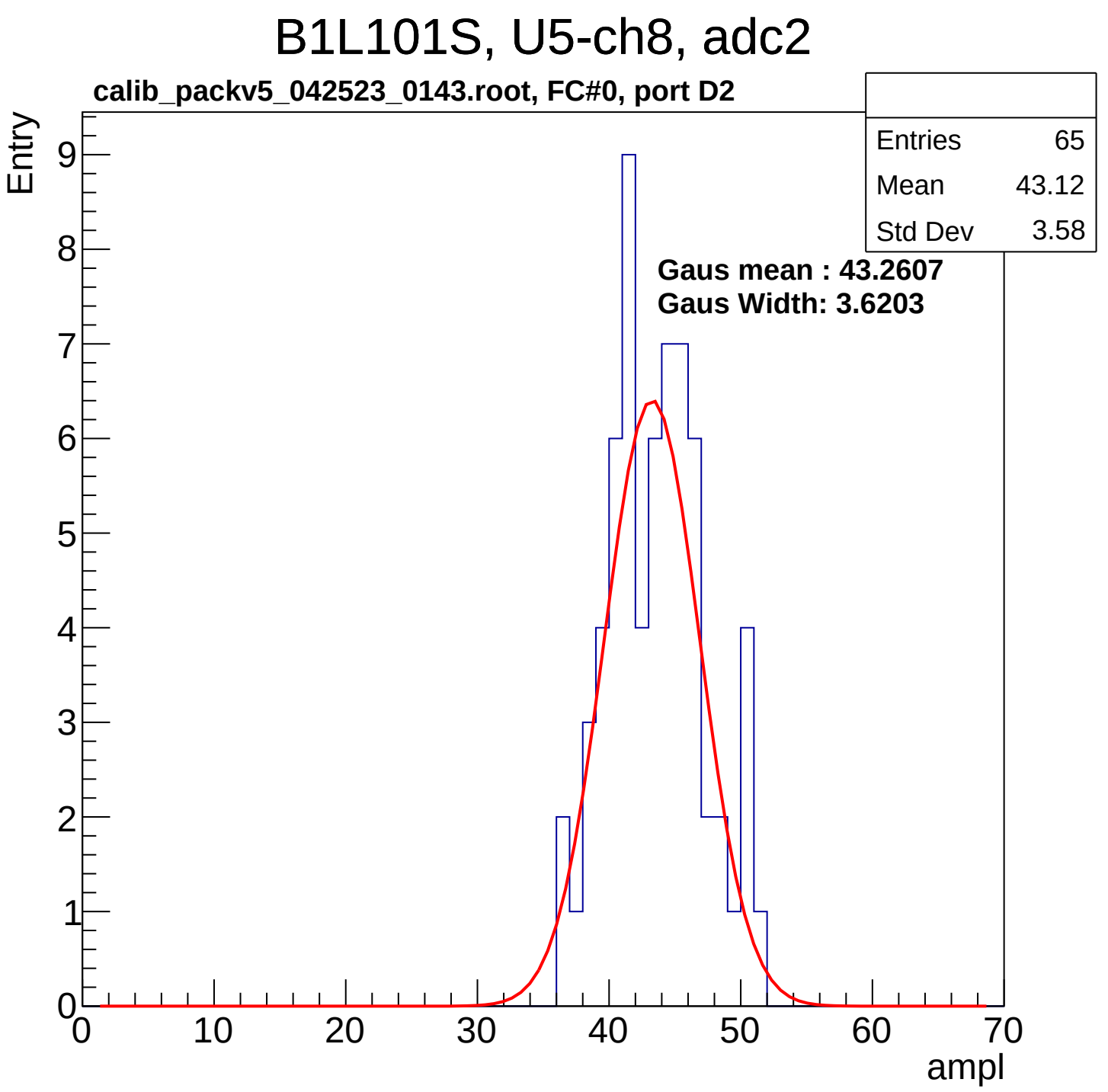
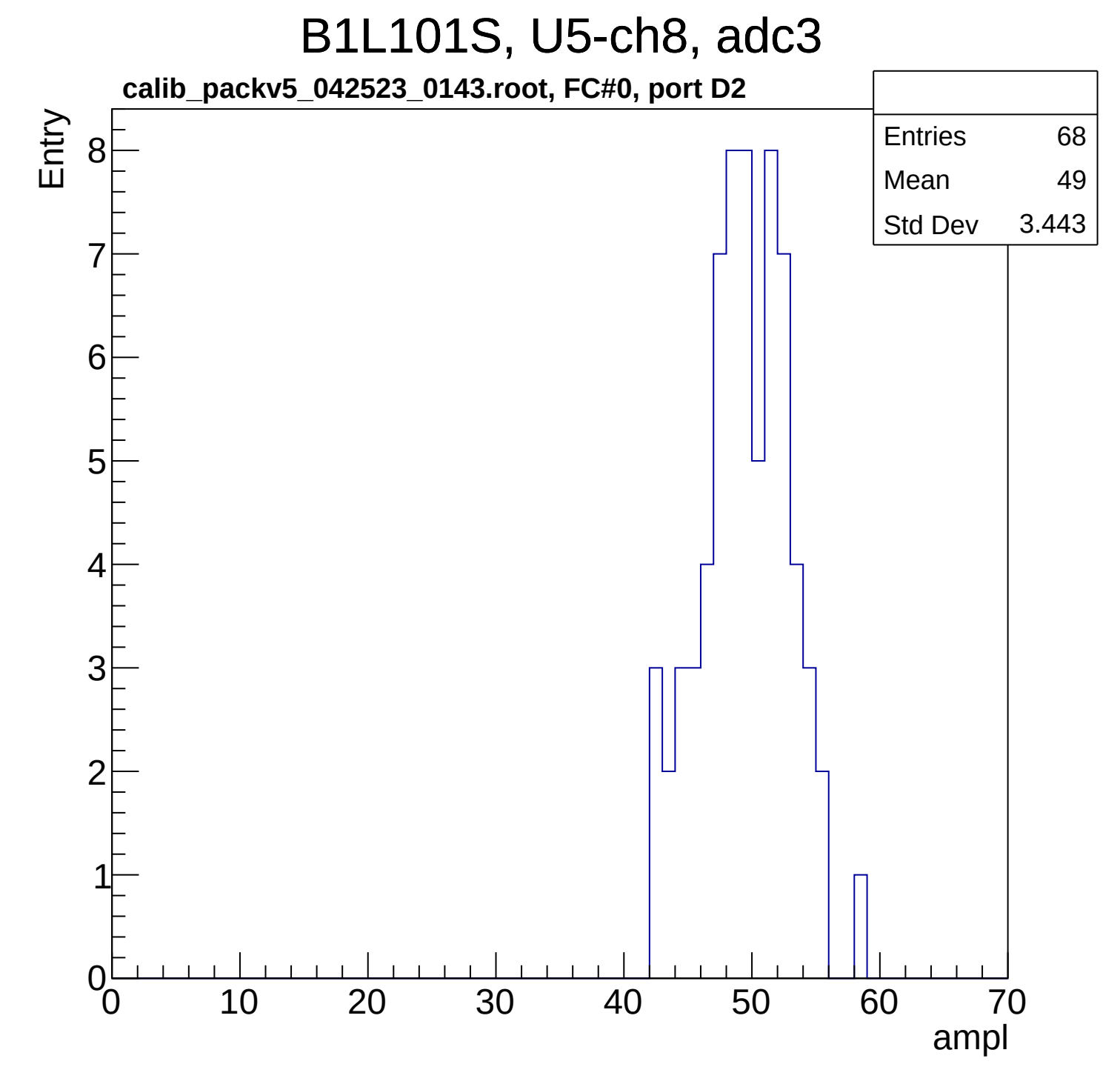
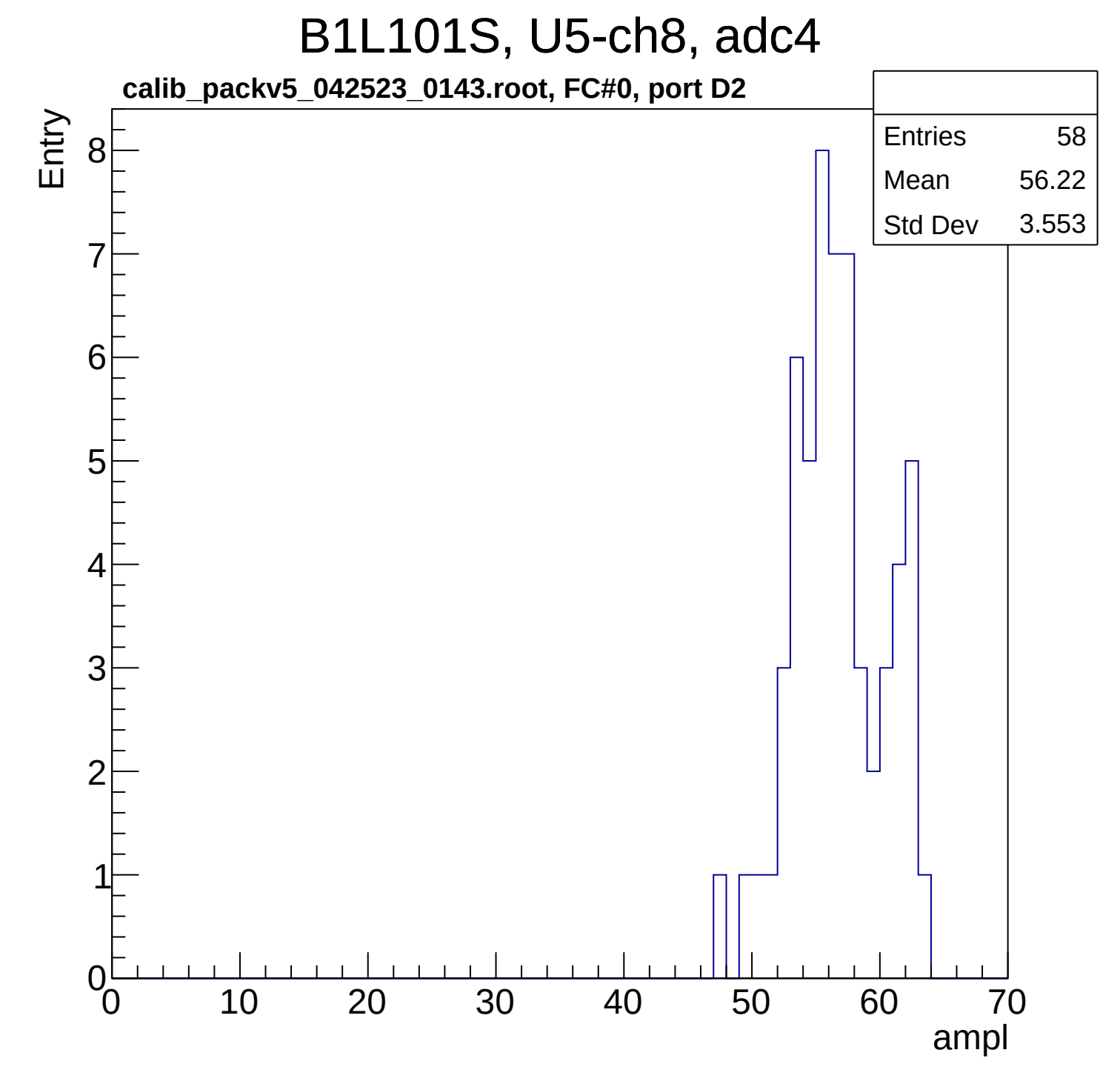

B1L101S, U5-ch7, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 42
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

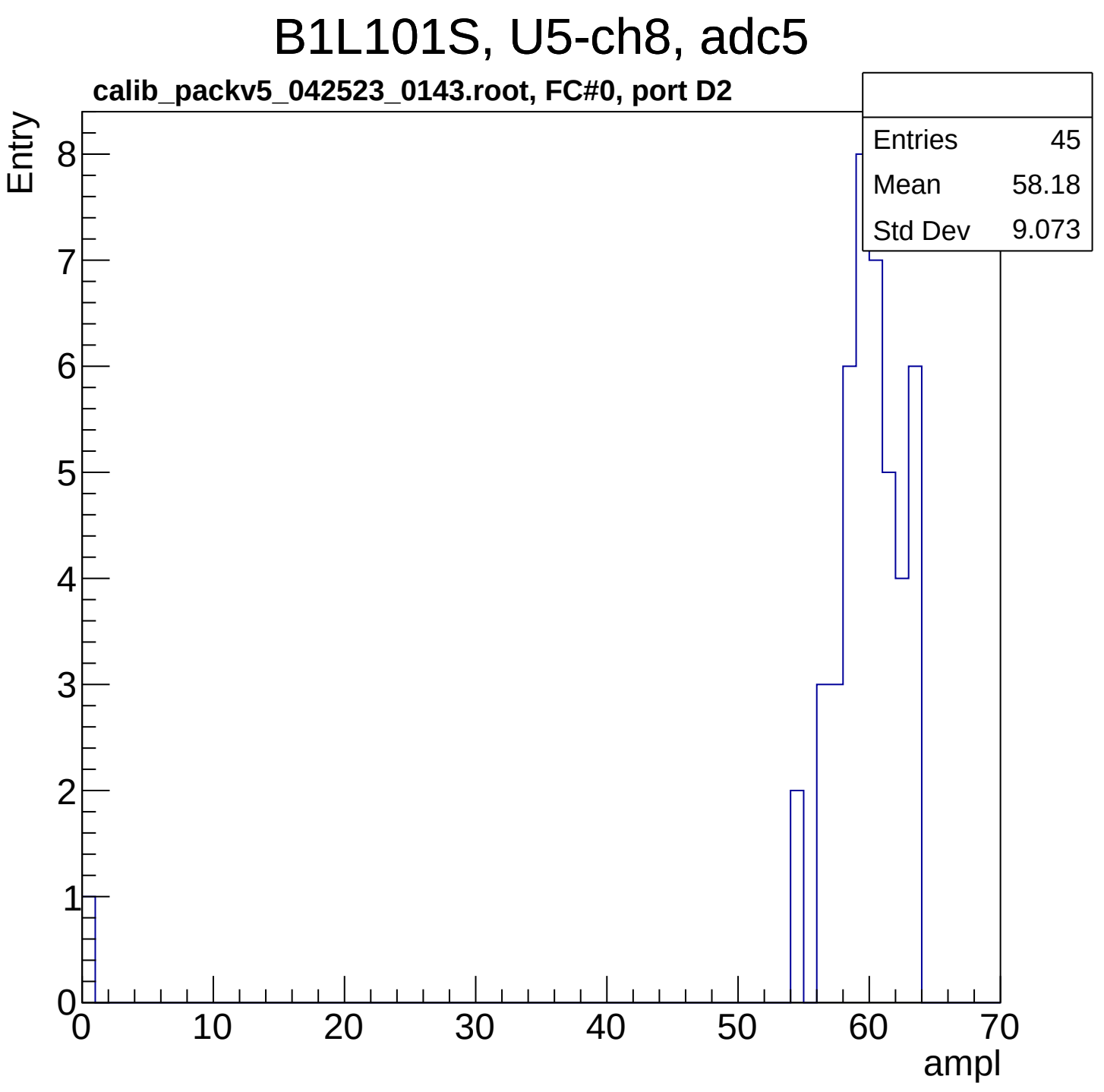

B1L101S, U5-ch8, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 92
Mean 28.2
Std Dev 7.37
Gaus mean : 30.4244
Gaus Width: 4.4542
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch8, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 36.16
Std Dev 3.498
Gaus mean : 36.4721
Gaus Width: 3.8491
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L101S, U5-ch8, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 43.12
Std Dev 3.58
Gaus mean : 43.2607
Gaus Width: 3.6203
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L101S, U5-ch8, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 49
Std Dev 3.443
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch8, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 56.22
Std Dev 3.553
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch8, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 58.18
Std Dev 9.073
Entry
ampl
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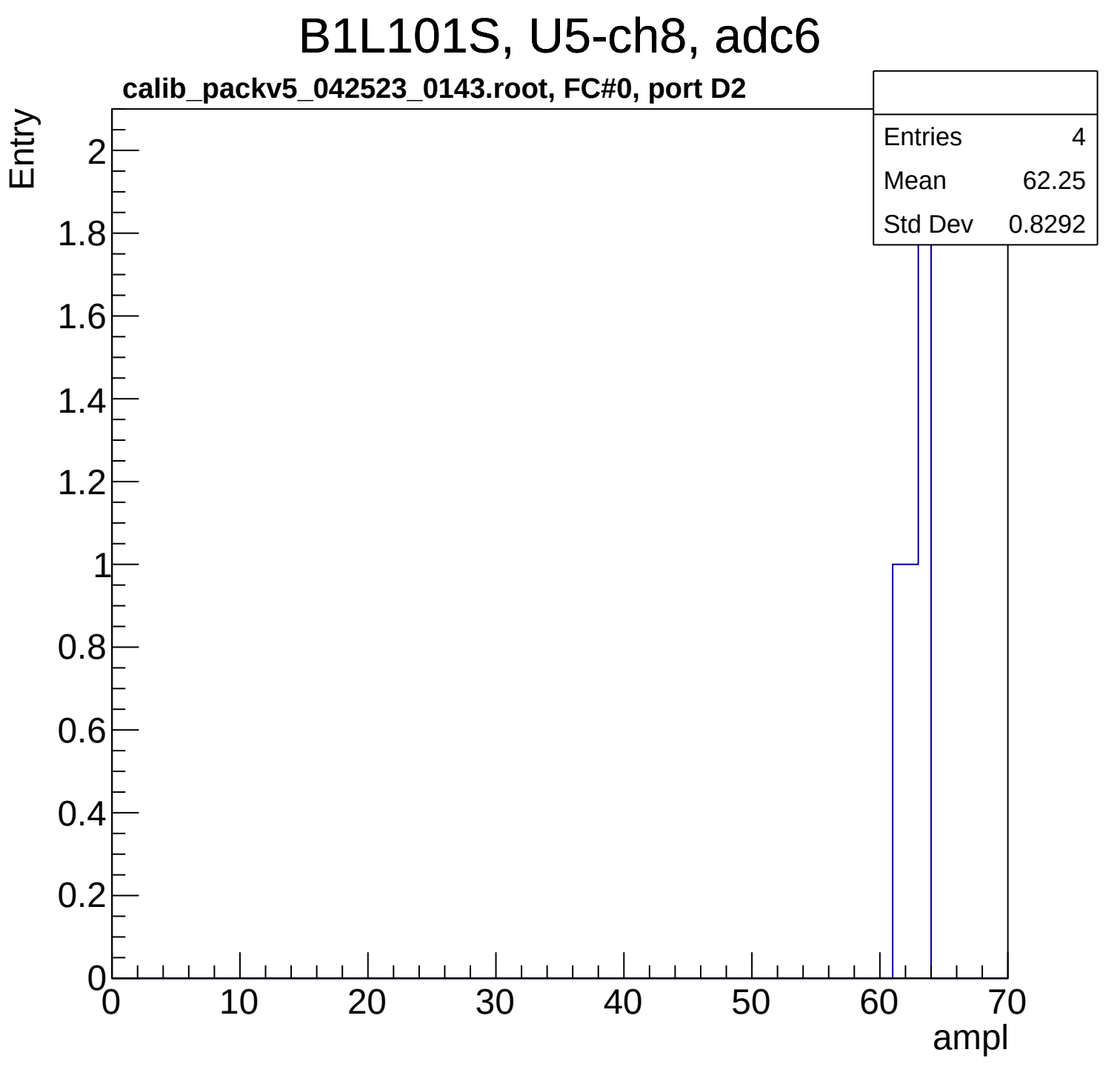
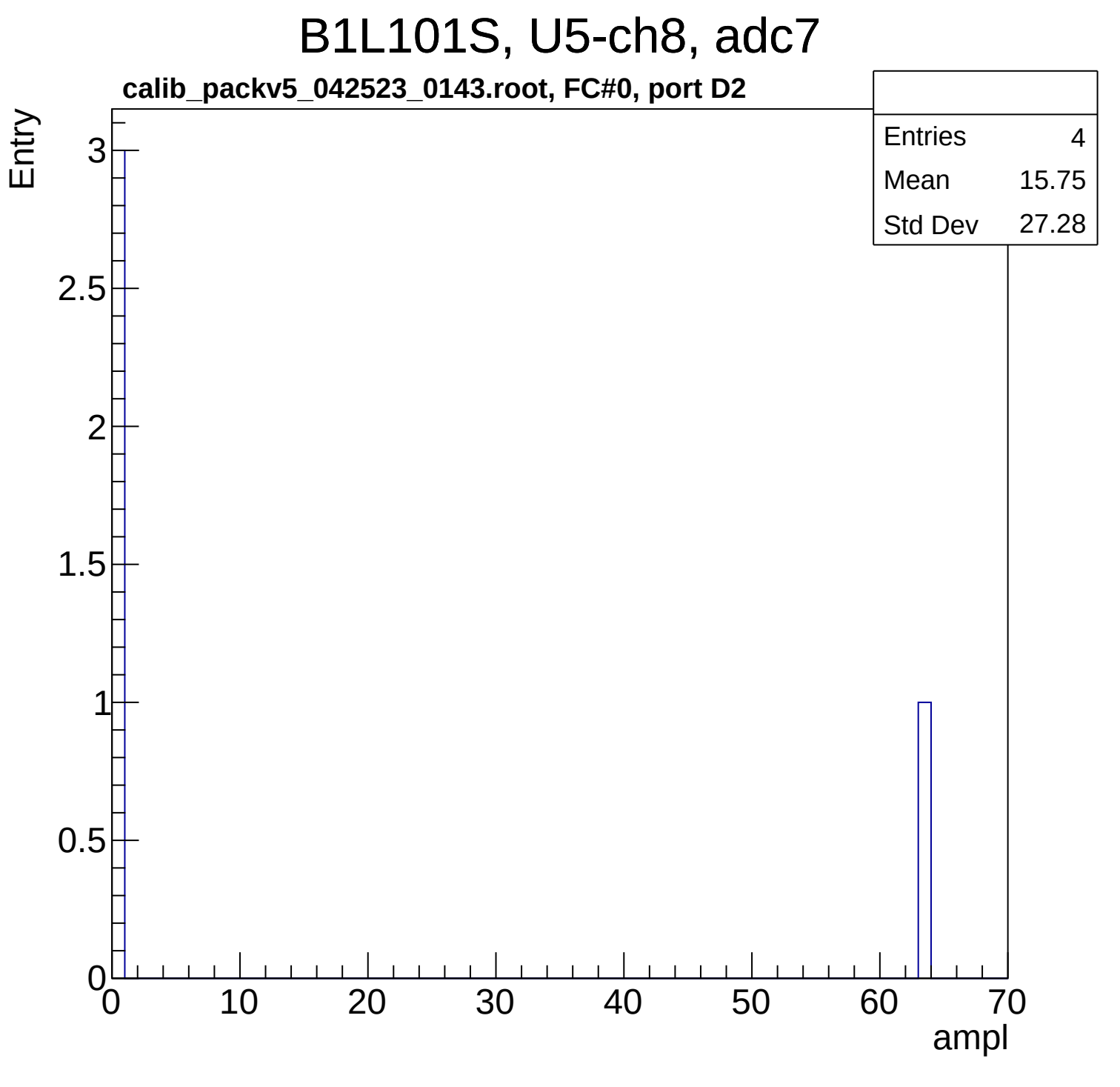
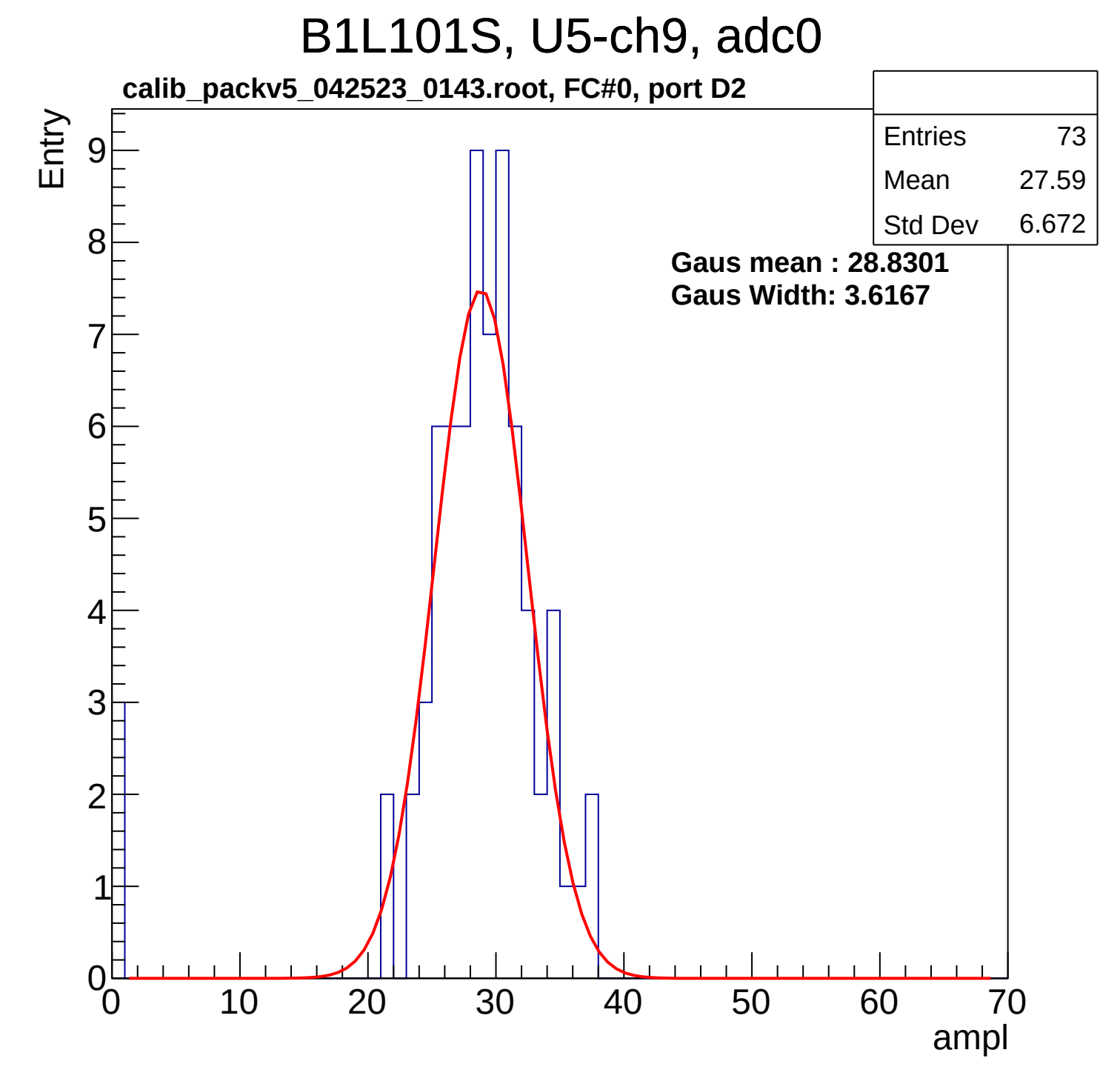
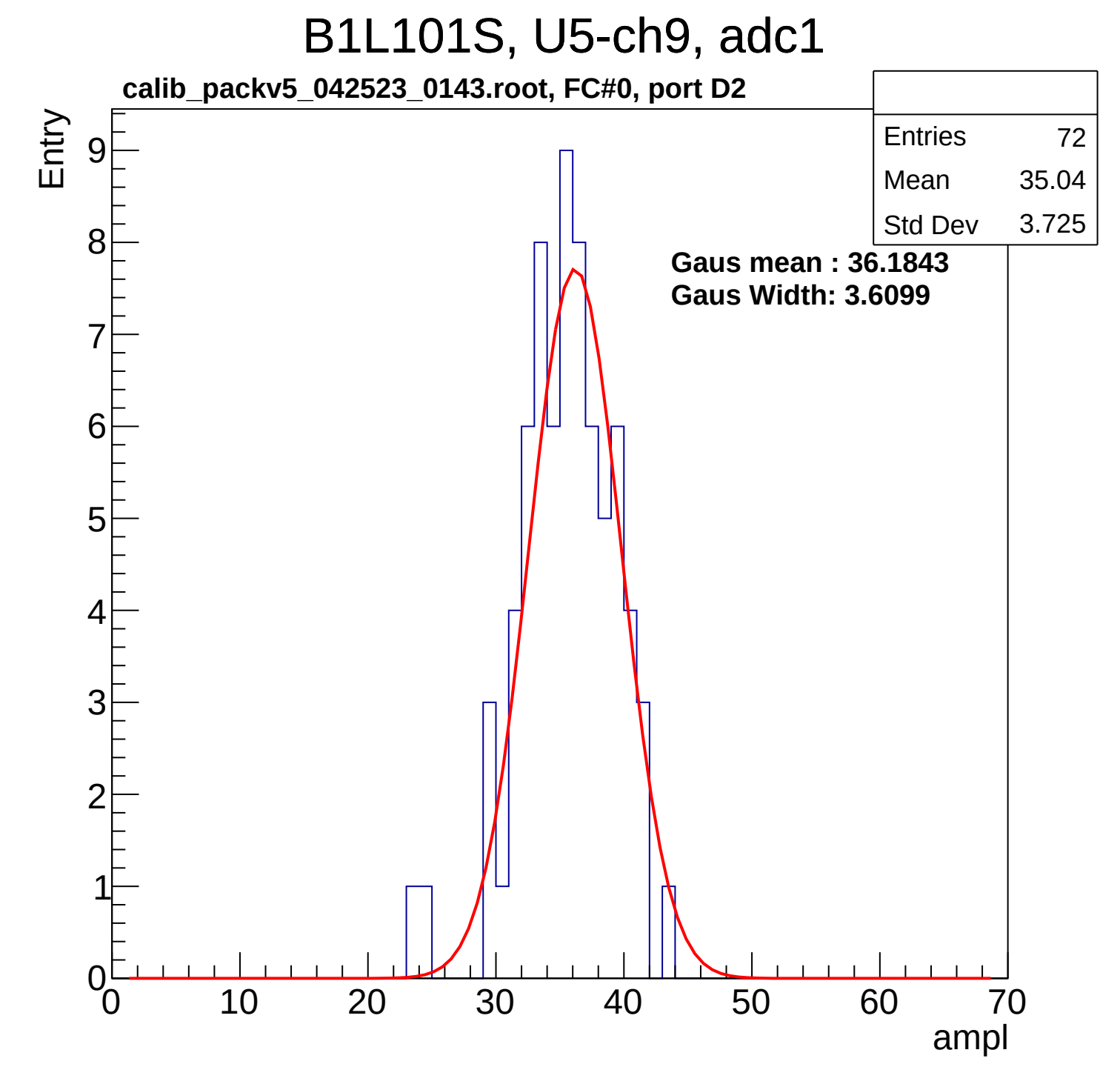
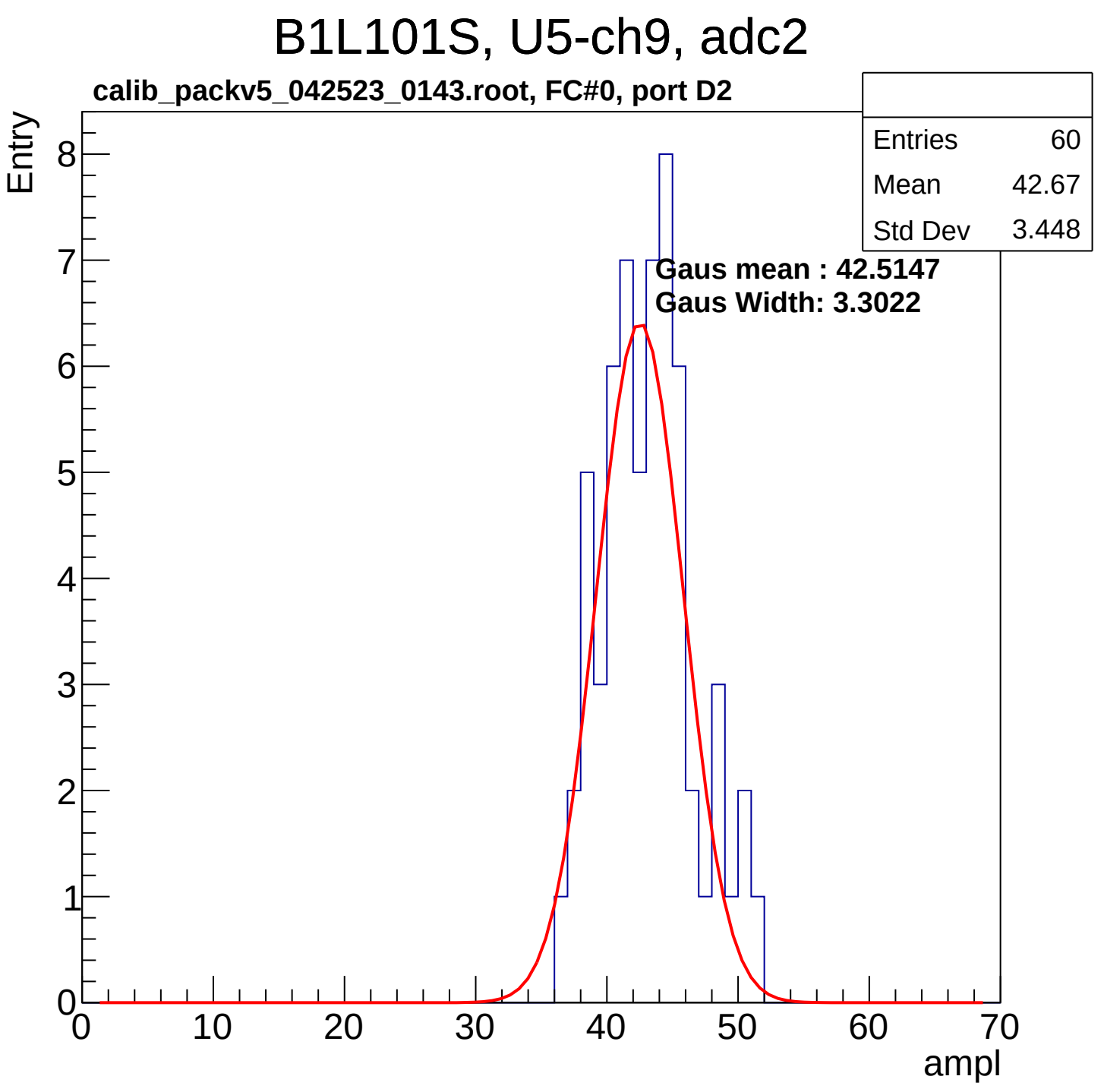
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

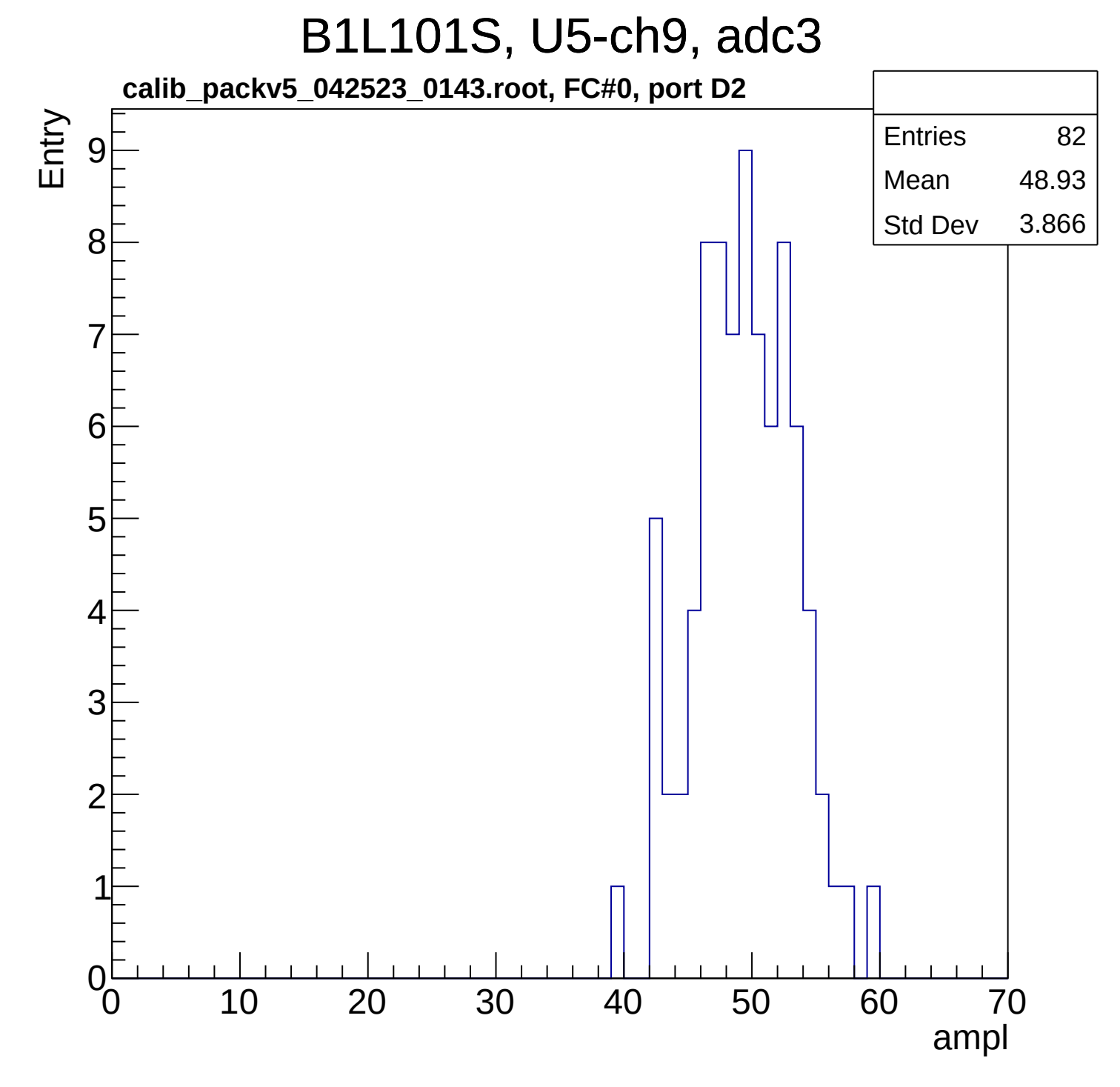

B1L101S, U5-ch8, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

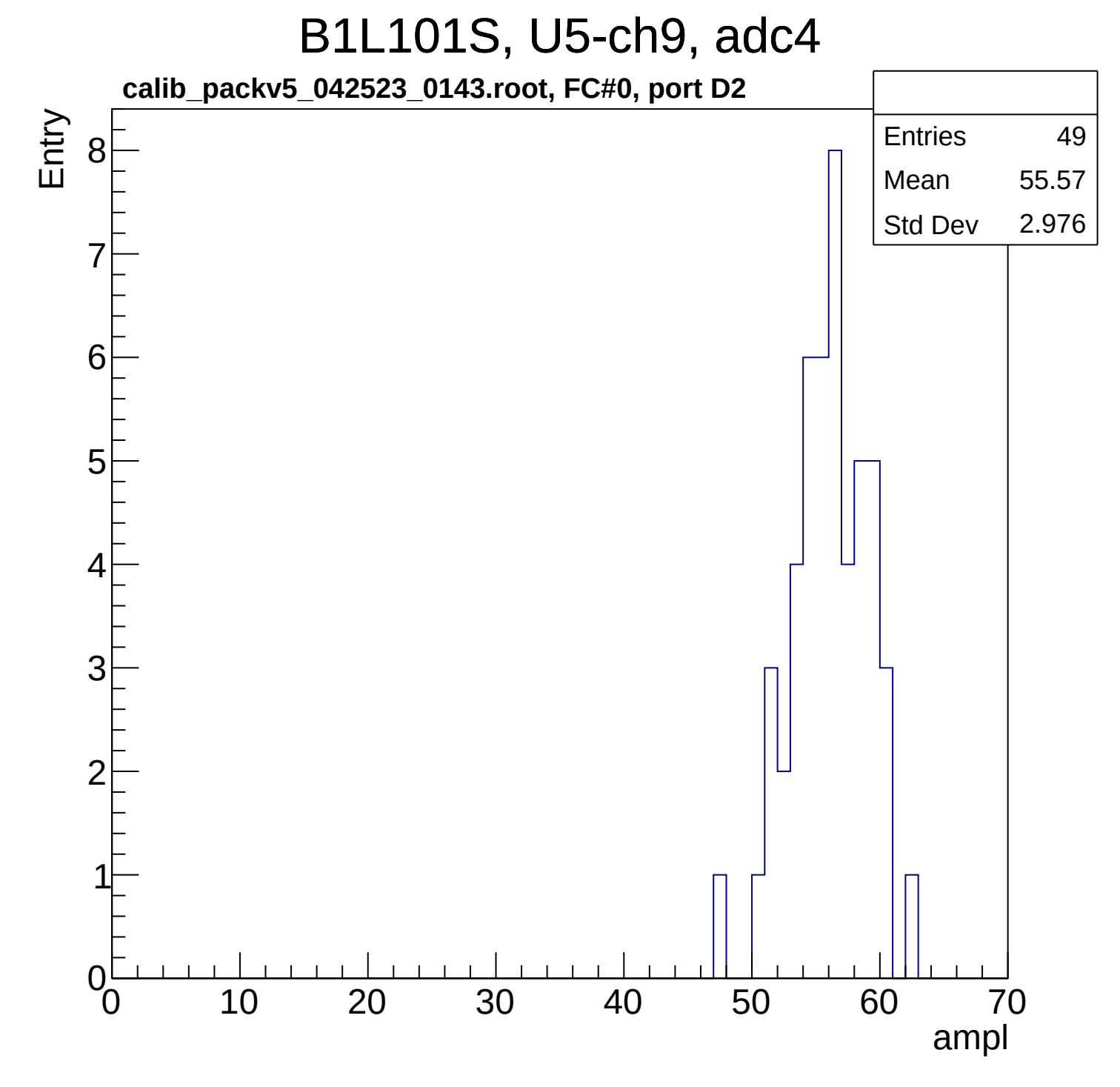

B1L101S, U5-ch8, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 15.75
Std Dev 27.28
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

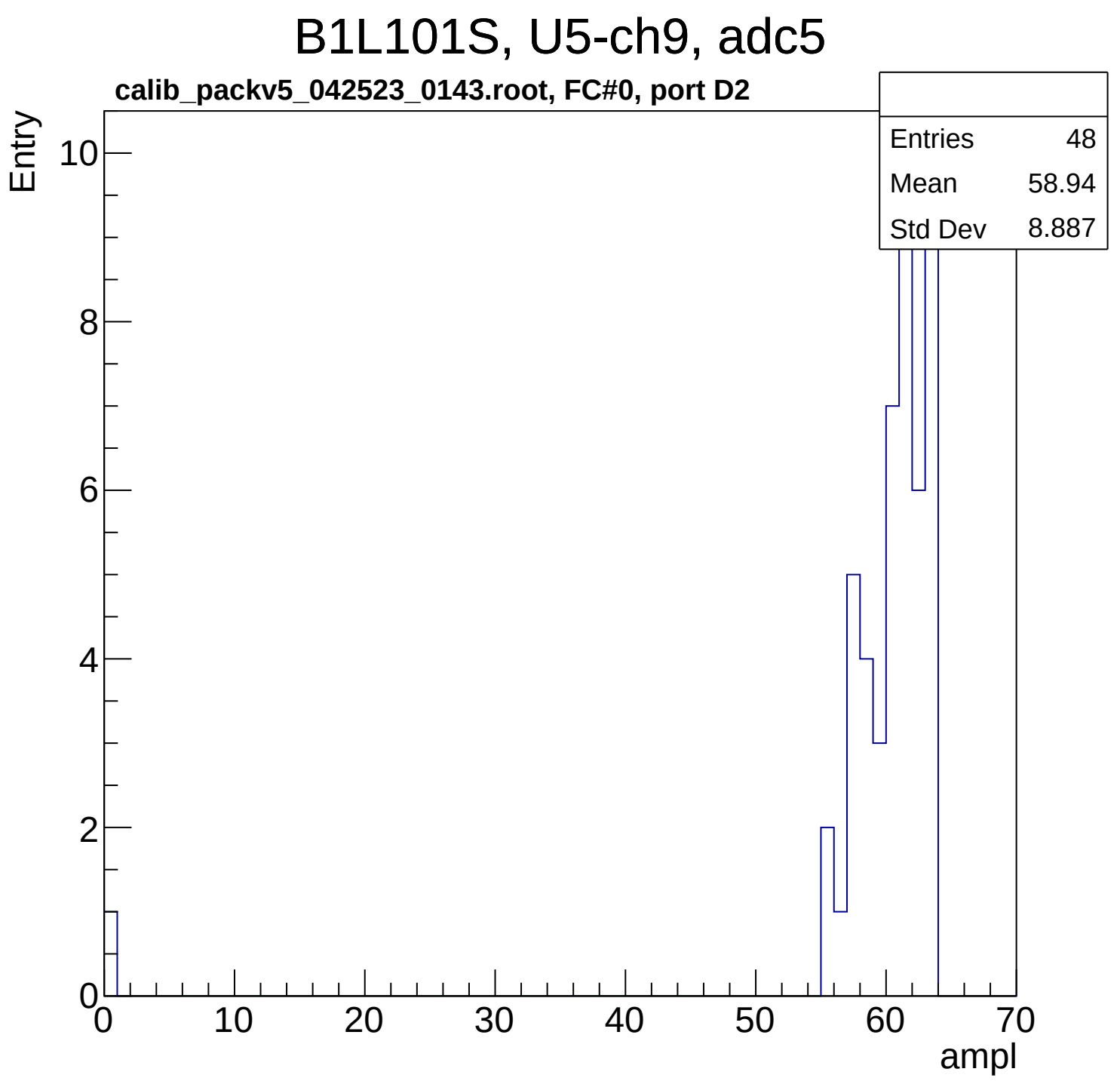

B1L101S, U5-ch9, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 27.59
Std Dev 6.672
Gaus mean : 28.8301
Gaus Width: 3.6167
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

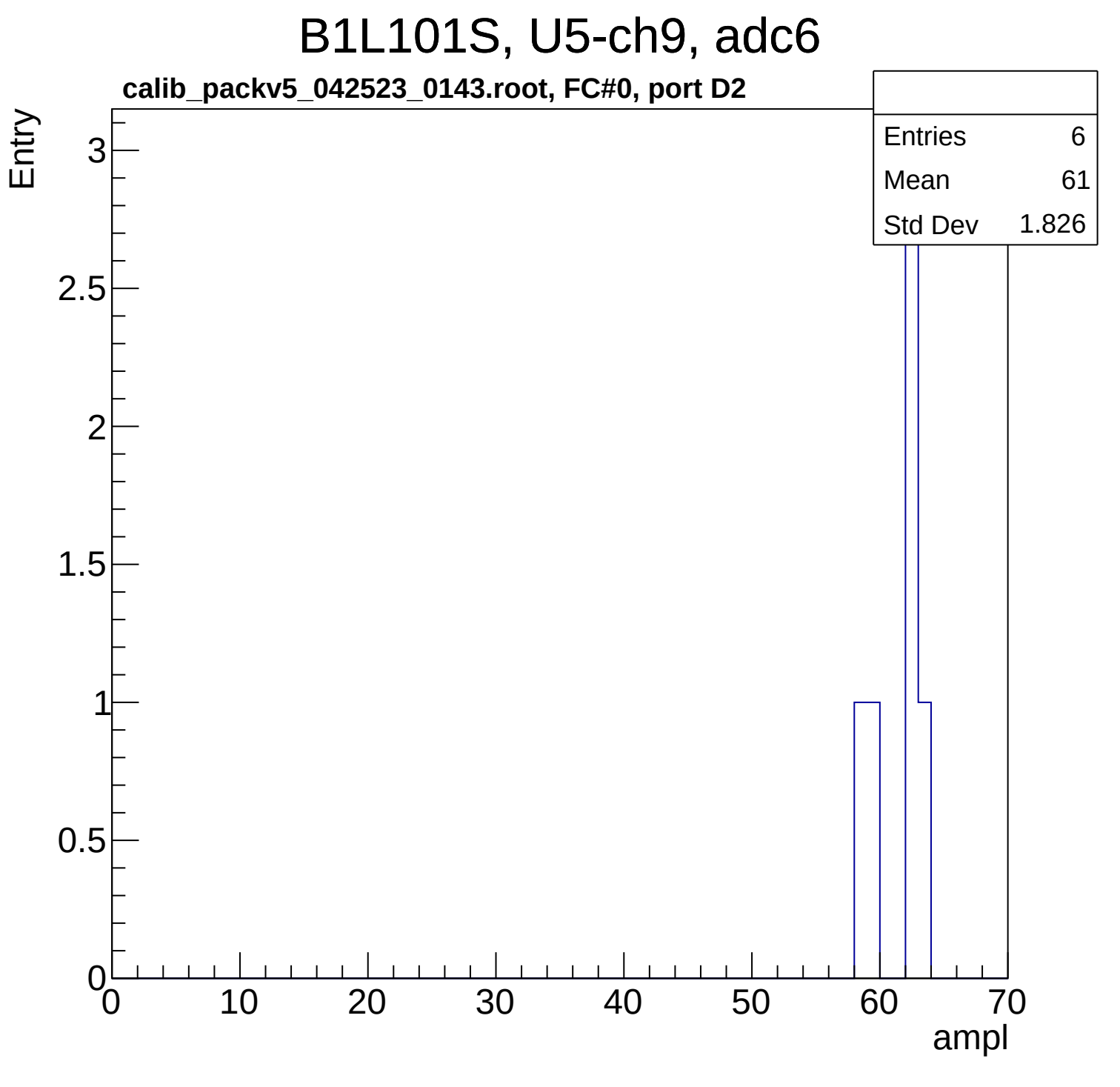

B1L101S, U5-ch9, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 35.04
Std Dev 3.725
Gaus mean : 36.1843
Gaus Width: 3.6099
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch9, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 42.67
Std Dev 3.448
Gaus mean : 42.5147
Gaus Width: 3.3022
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch9, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 82
Mean 48.93
Std Dev 3.866
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch9, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 55.57
Std Dev 2.976
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch9, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 58.94
Std Dev 8.887
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch9, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 61
Std Dev 1.826
Entry
ampl
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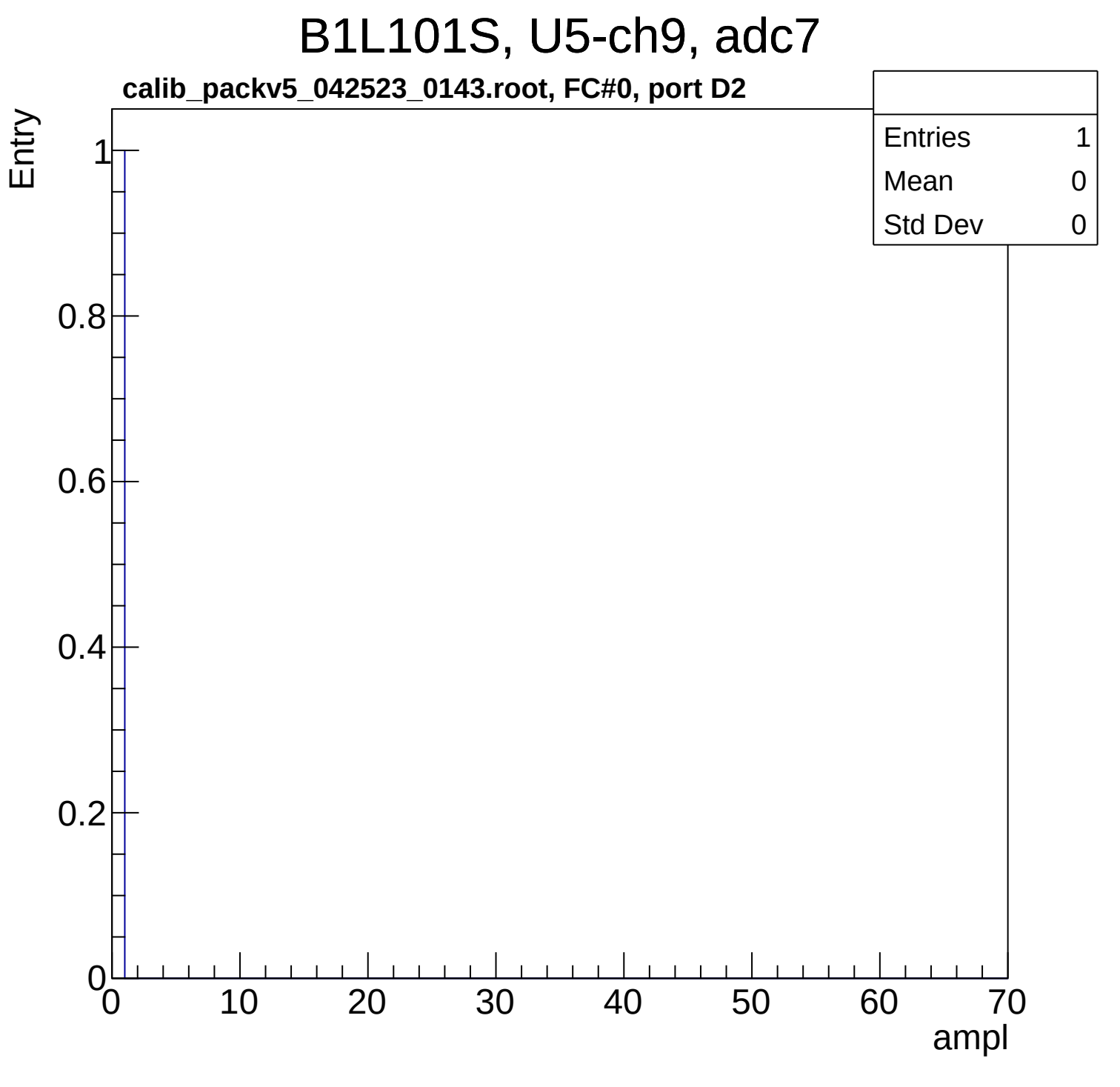
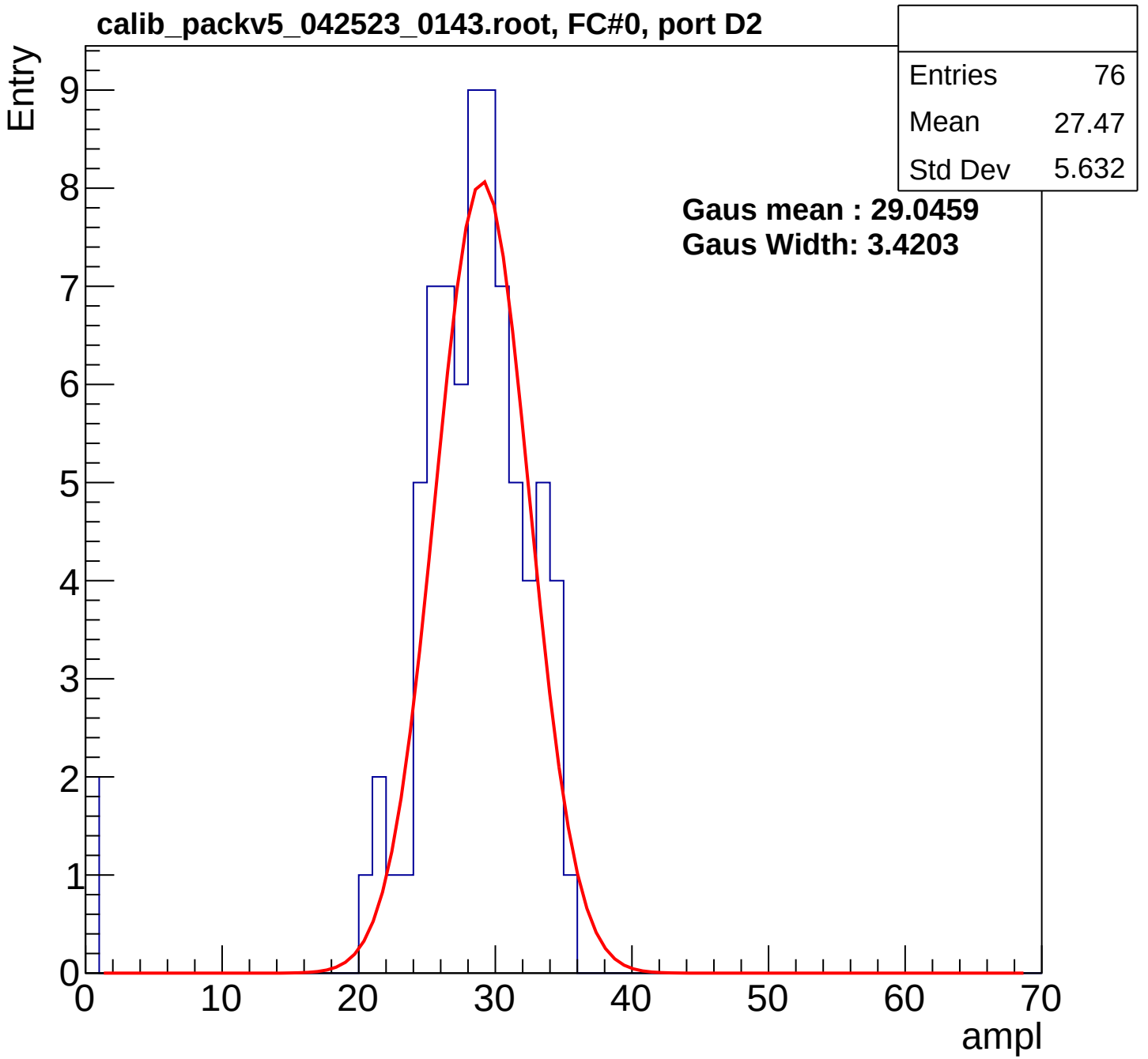
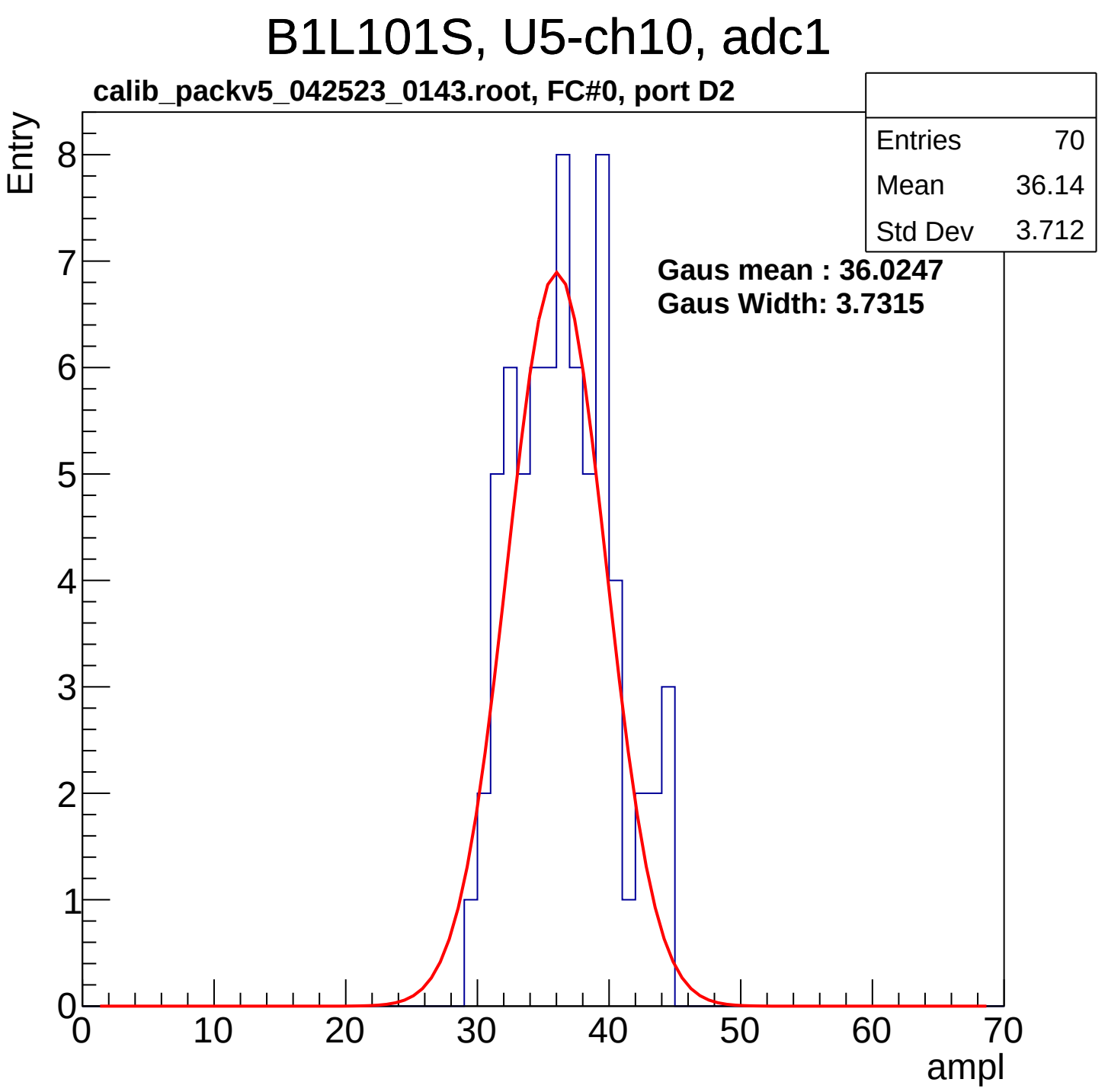
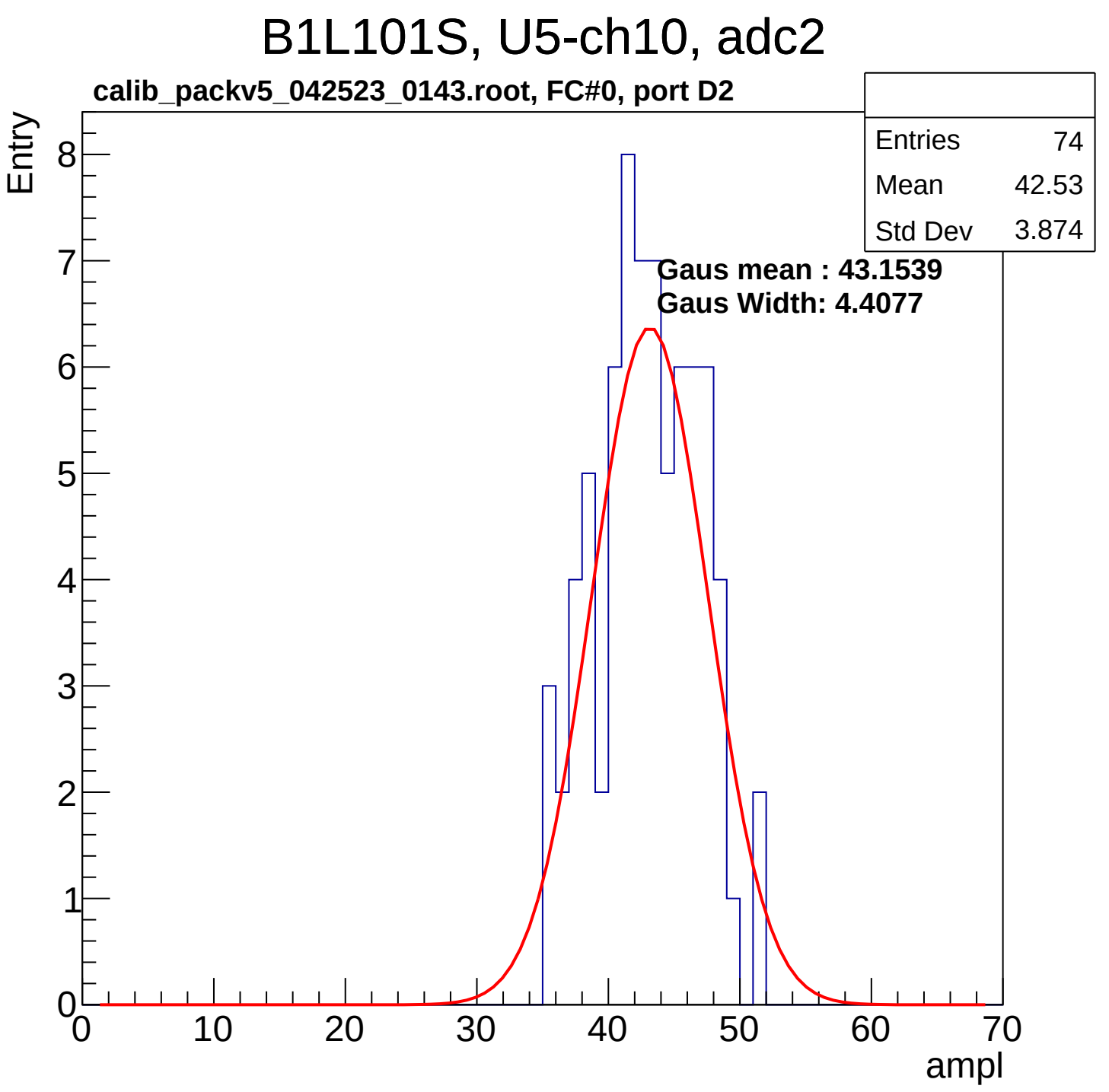
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U5-ch9, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch10, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 27.47
Std Dev 5.632
Gaus mean : 29.0459
Gaus Width: 3.4203
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch10, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 36.14
Std Dev 3.712
Gaus mean : 36.0247
Gaus Width: 3.7315
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch10, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 42.53
Std Dev 3.874
Gaus mean : 43.1539
Gaus Width: 4.4077
Entry
ampl
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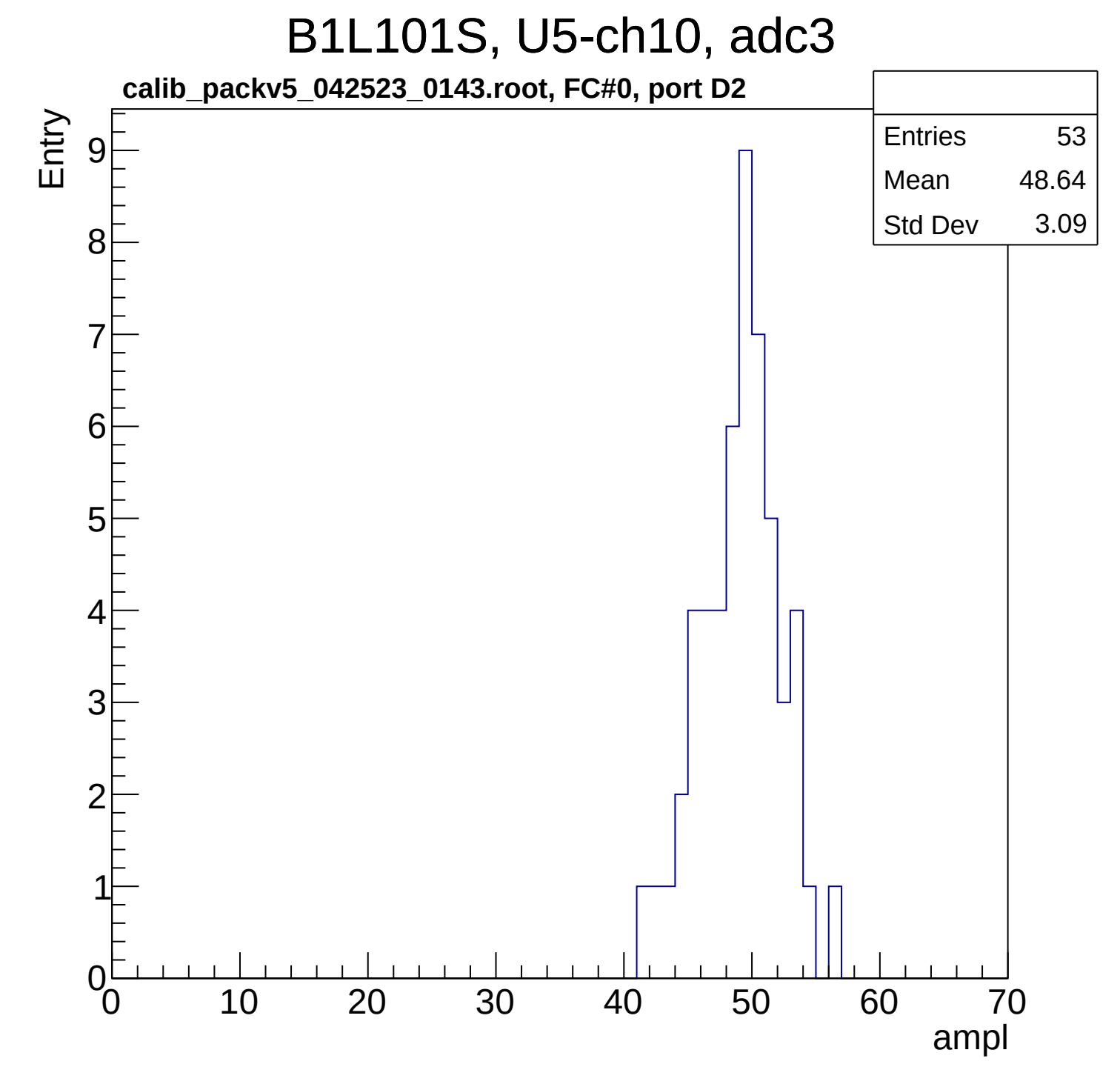
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch10, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 48.64
Std Dev 3.09
Entry
ampl
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0
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60
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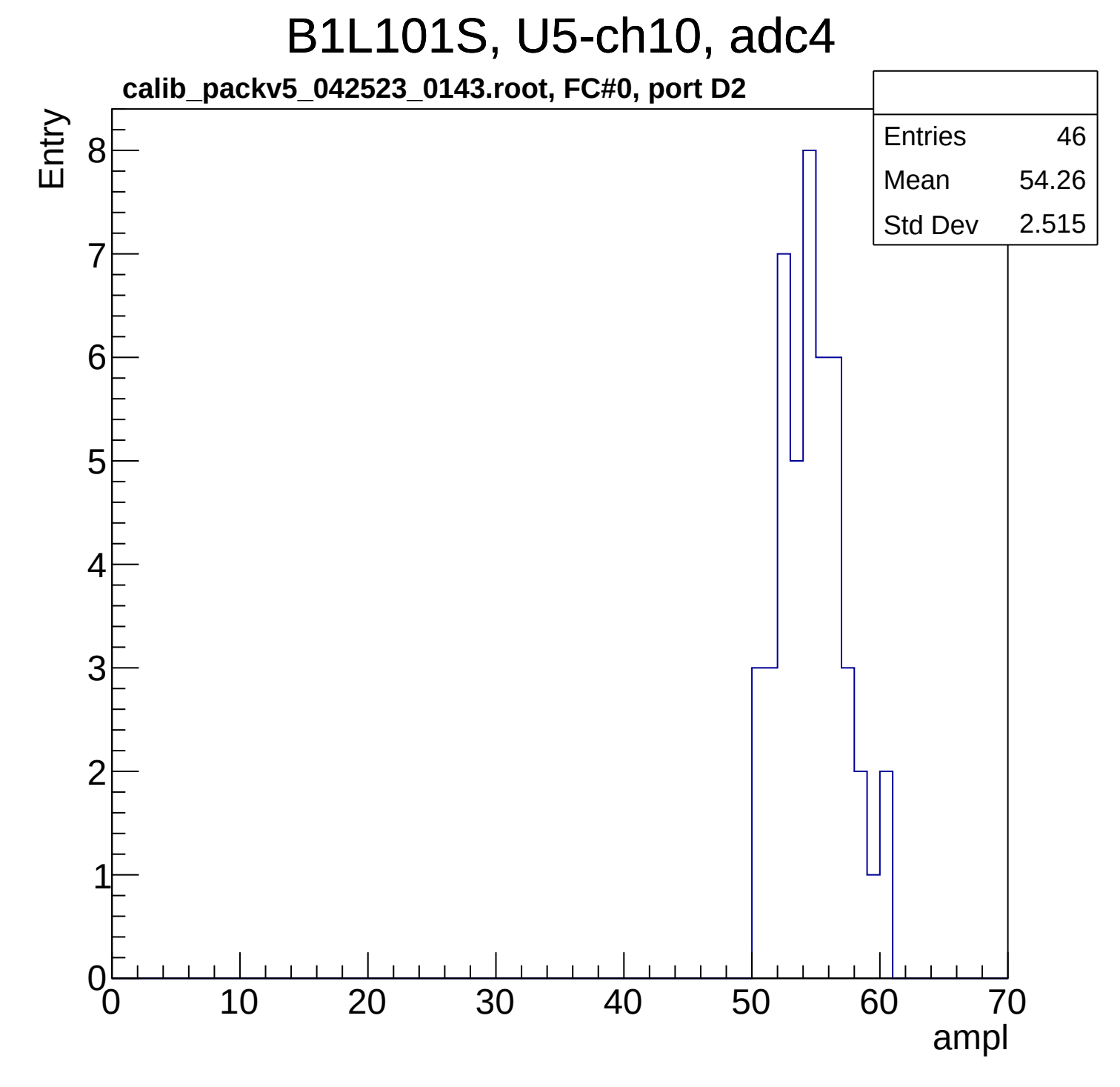
B1L101S, U5-ch10, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 54.26
Std Dev 2.515
Entry
ampl
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1
2
3
4
5
6
7
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0
10
20
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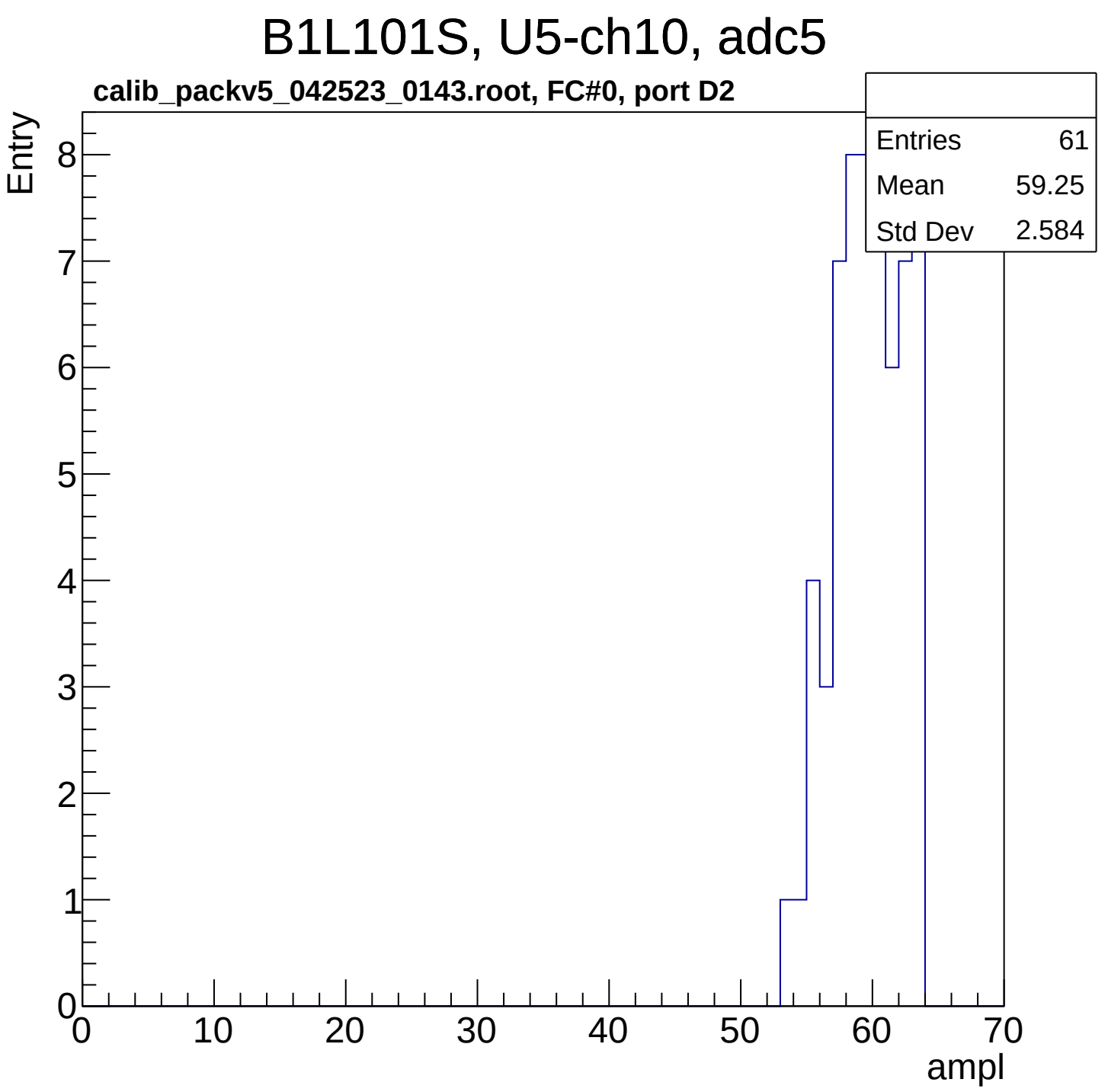
40
50
60
70


B1L101S, U5-ch10, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 59.25
Std Dev 2.584
Entry
ampl
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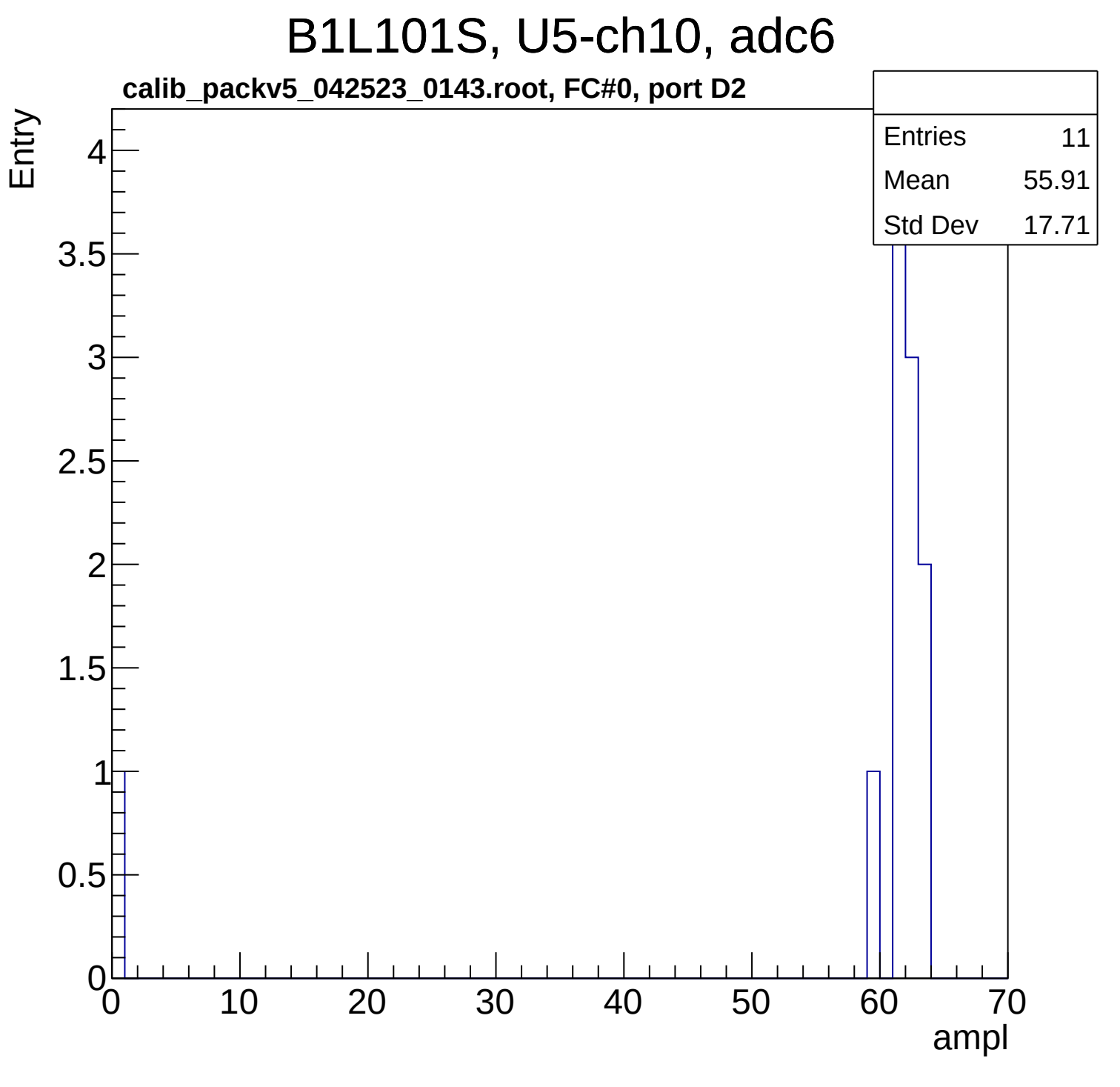
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch10, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 11
Mean 55.91
Std Dev 17.71
Entry
ampl
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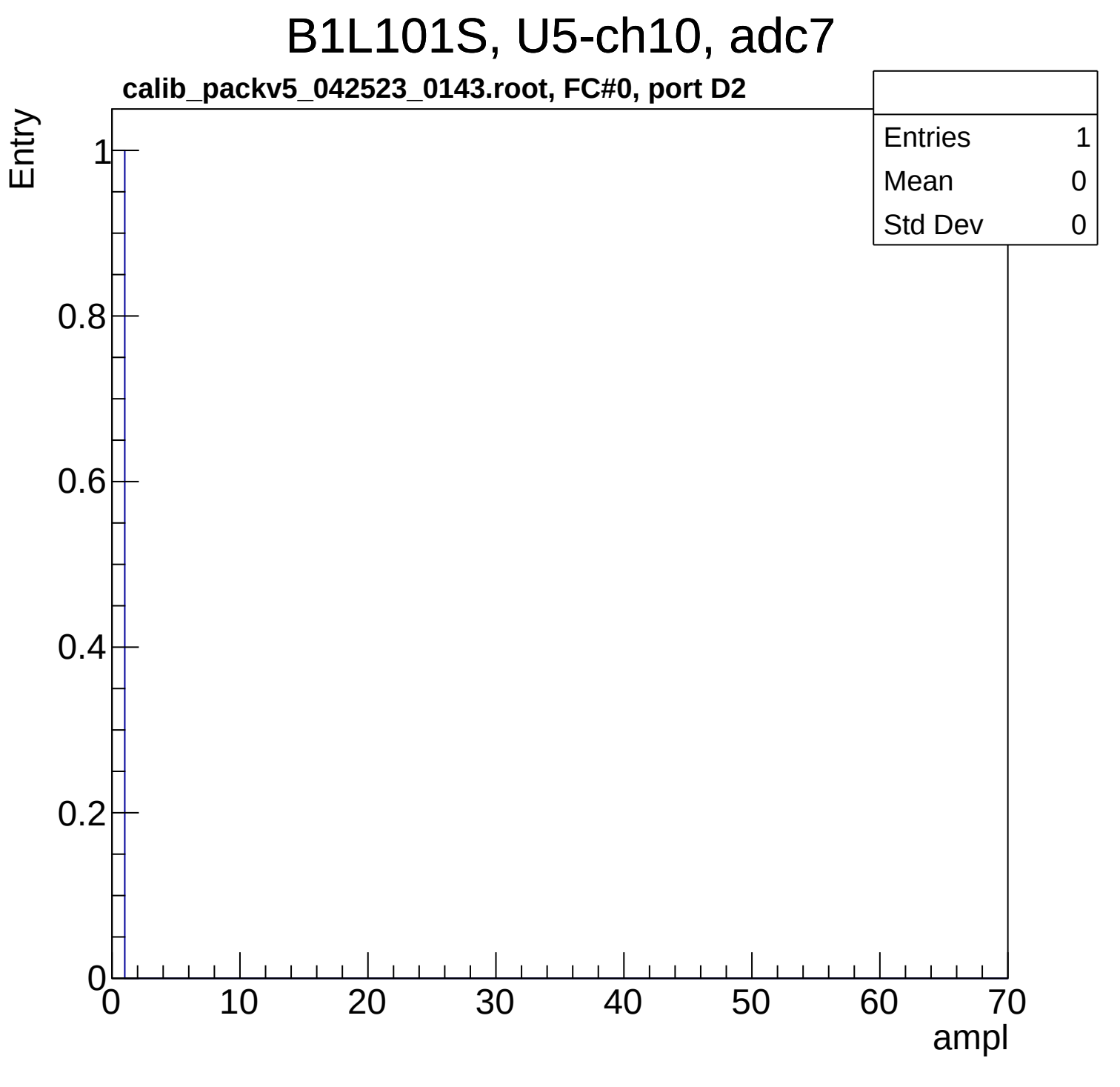
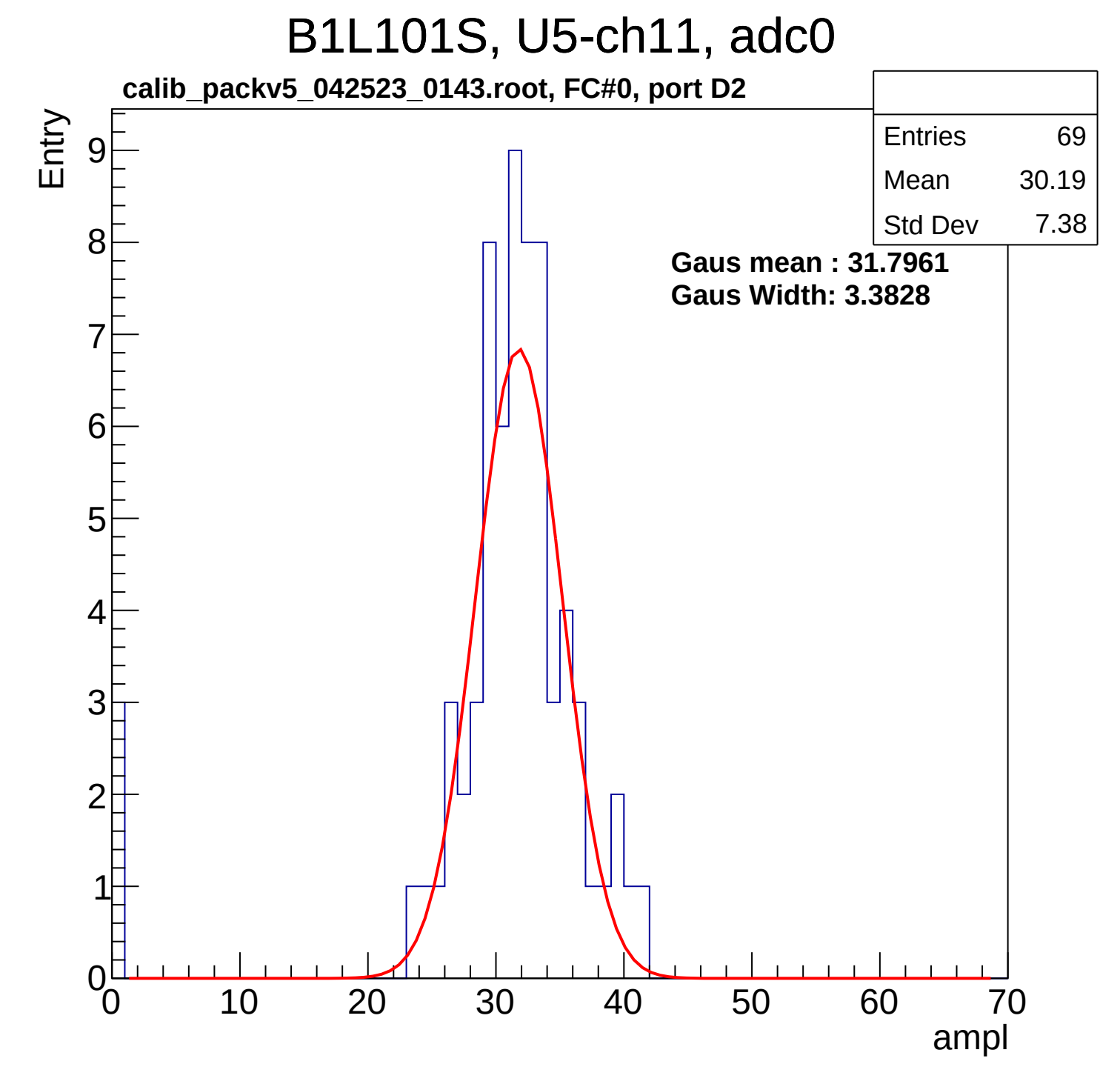
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L101S, U5-ch10, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch11, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 30.19
Std Dev 7.38
Gaus mean : 31.7961
Gaus Width: 3.3828
Entry
ampl
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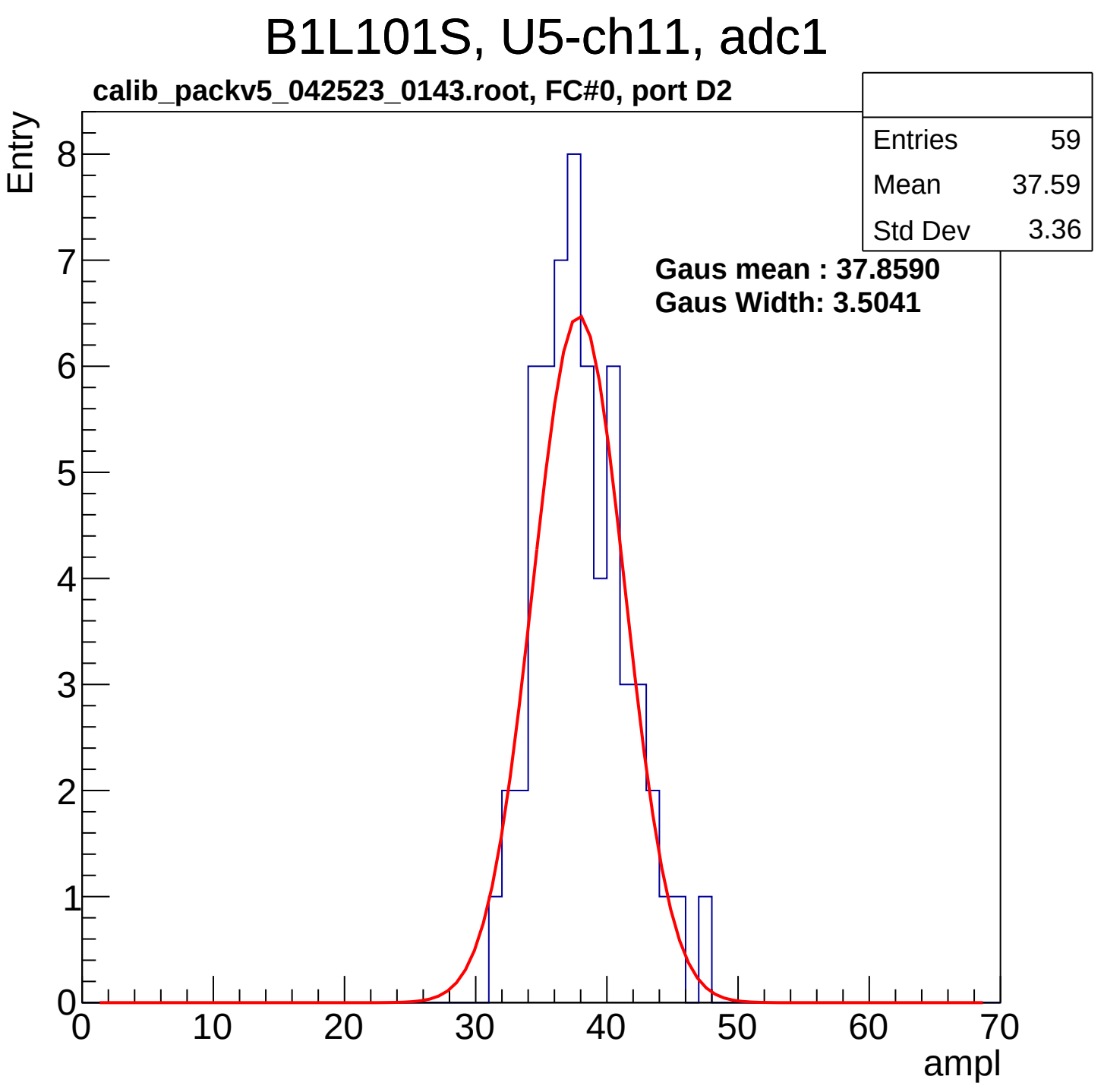
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch11, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 37.59
Std Dev 3.36
Gaus mean : 37.8590
Gaus Width: 3.5041
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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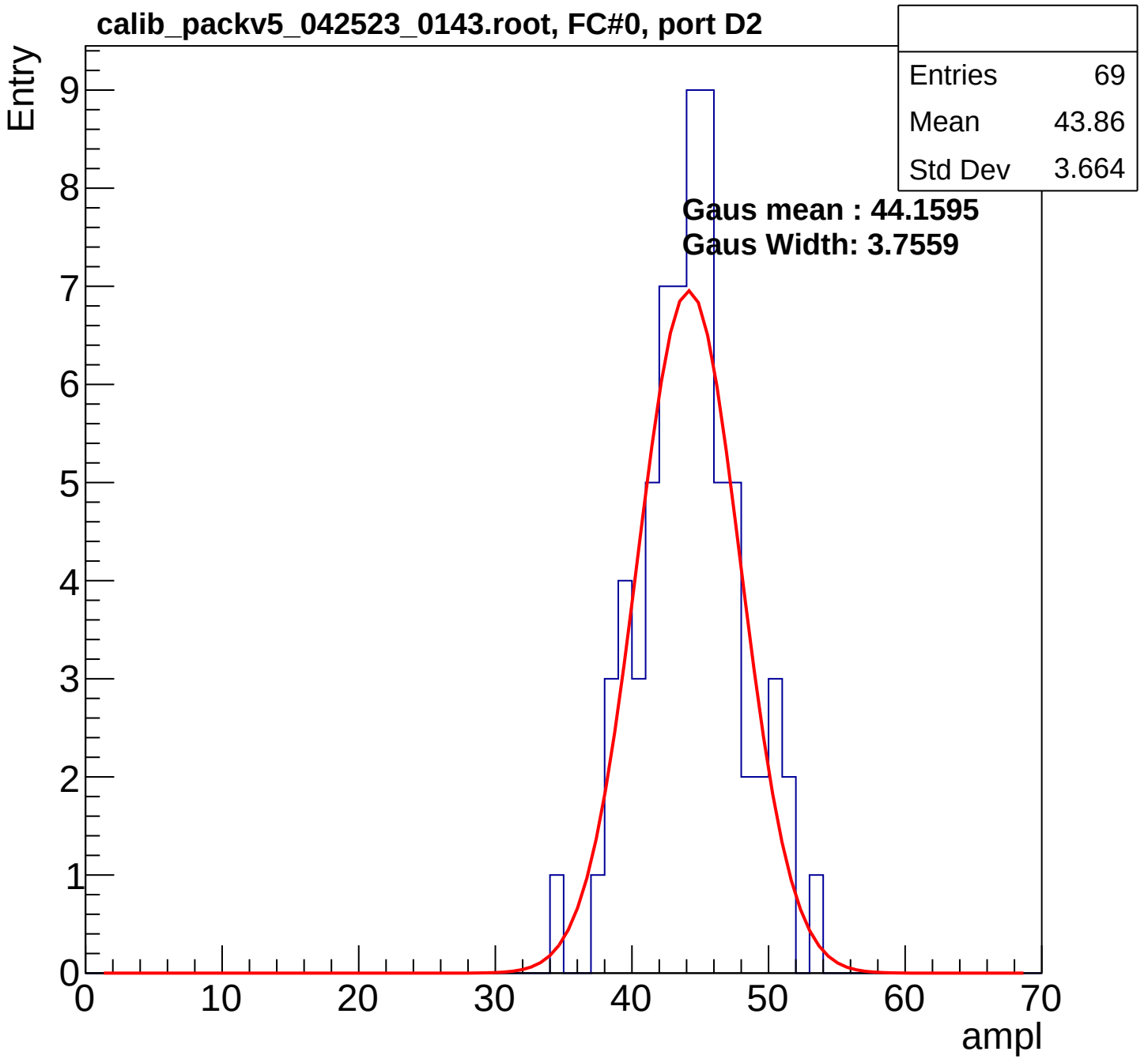
B1L101S, U5-ch11, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 43.86
Std Dev 3.664
Gaus mean : 44.1595
Gaus Width: 3.7559
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
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40
50
60
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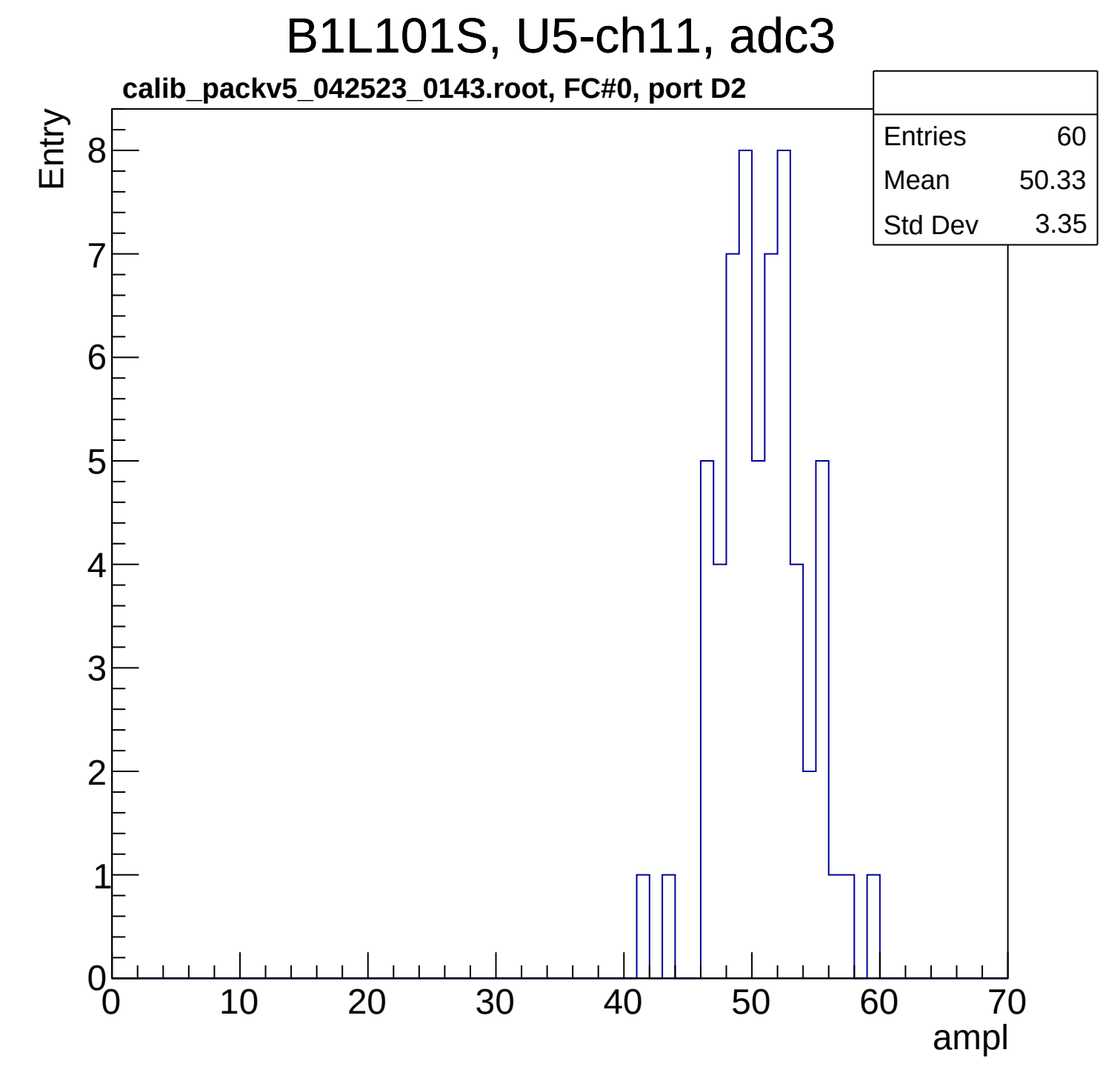
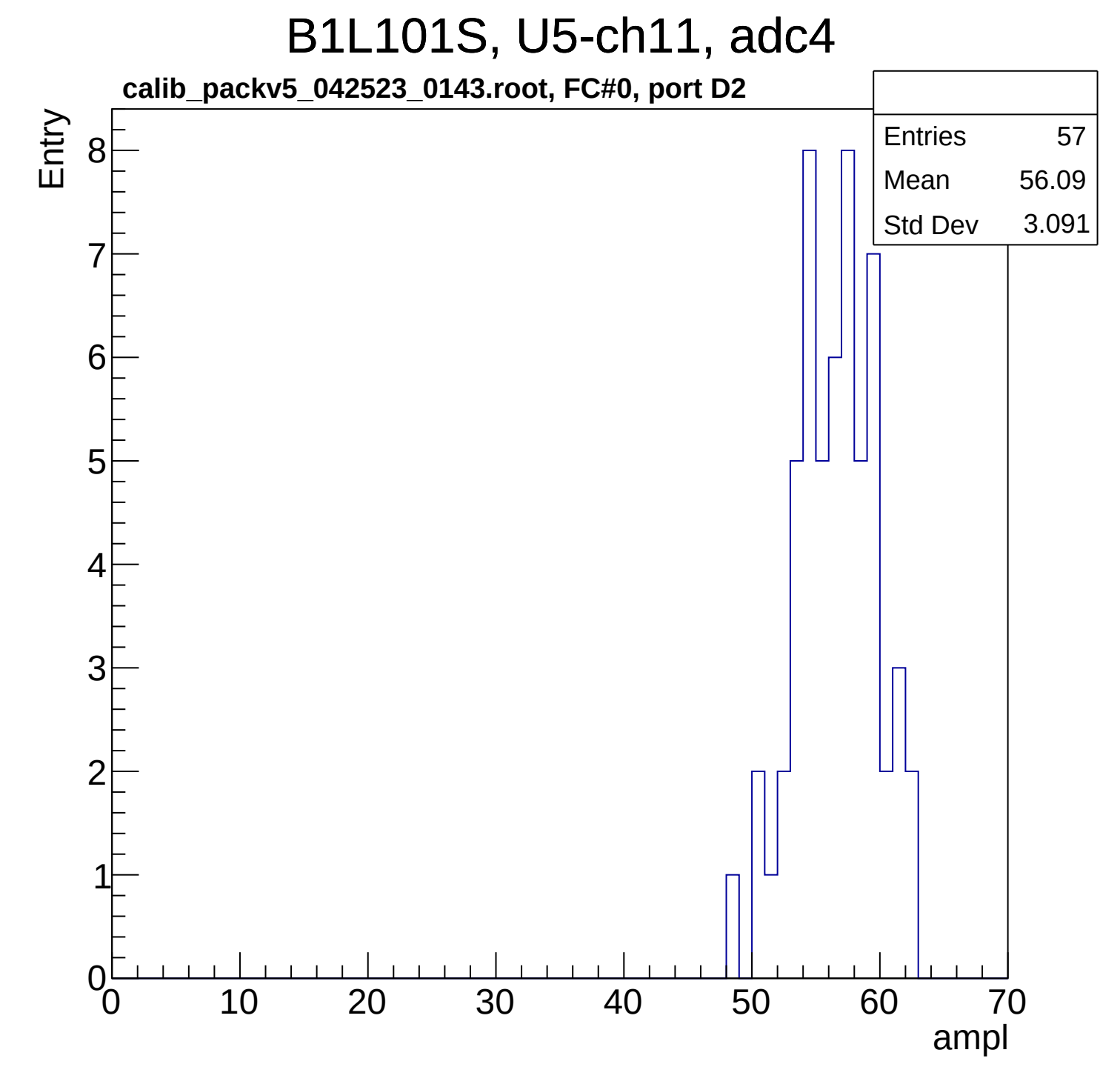

B1L101S, U5-ch11, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 50.33
Std Dev 3.35
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch11, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 56.09
Std Dev 3.091
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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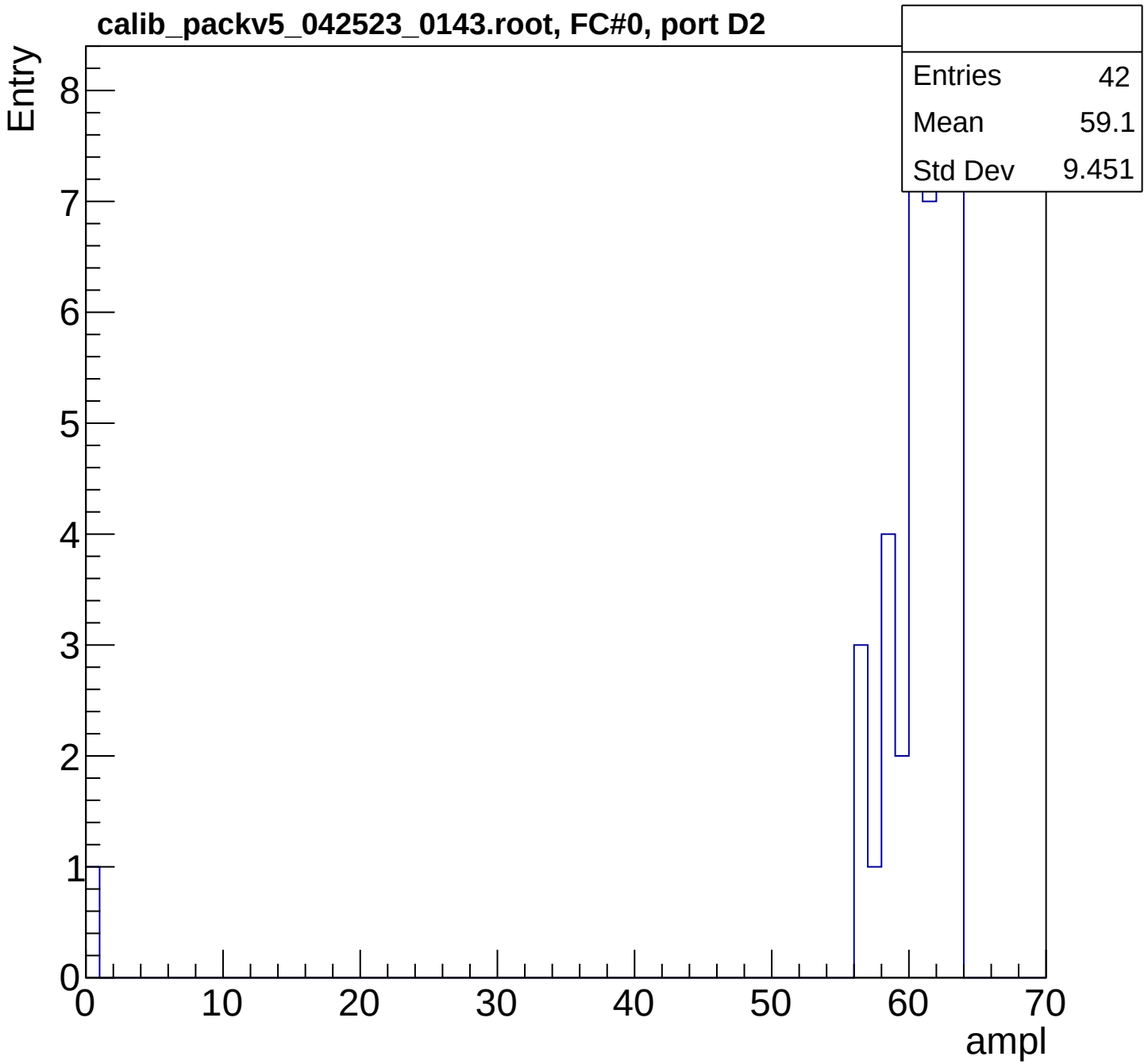
40
50
60
70


B1L101S, U5-ch11, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 59.1
Std Dev 9.451
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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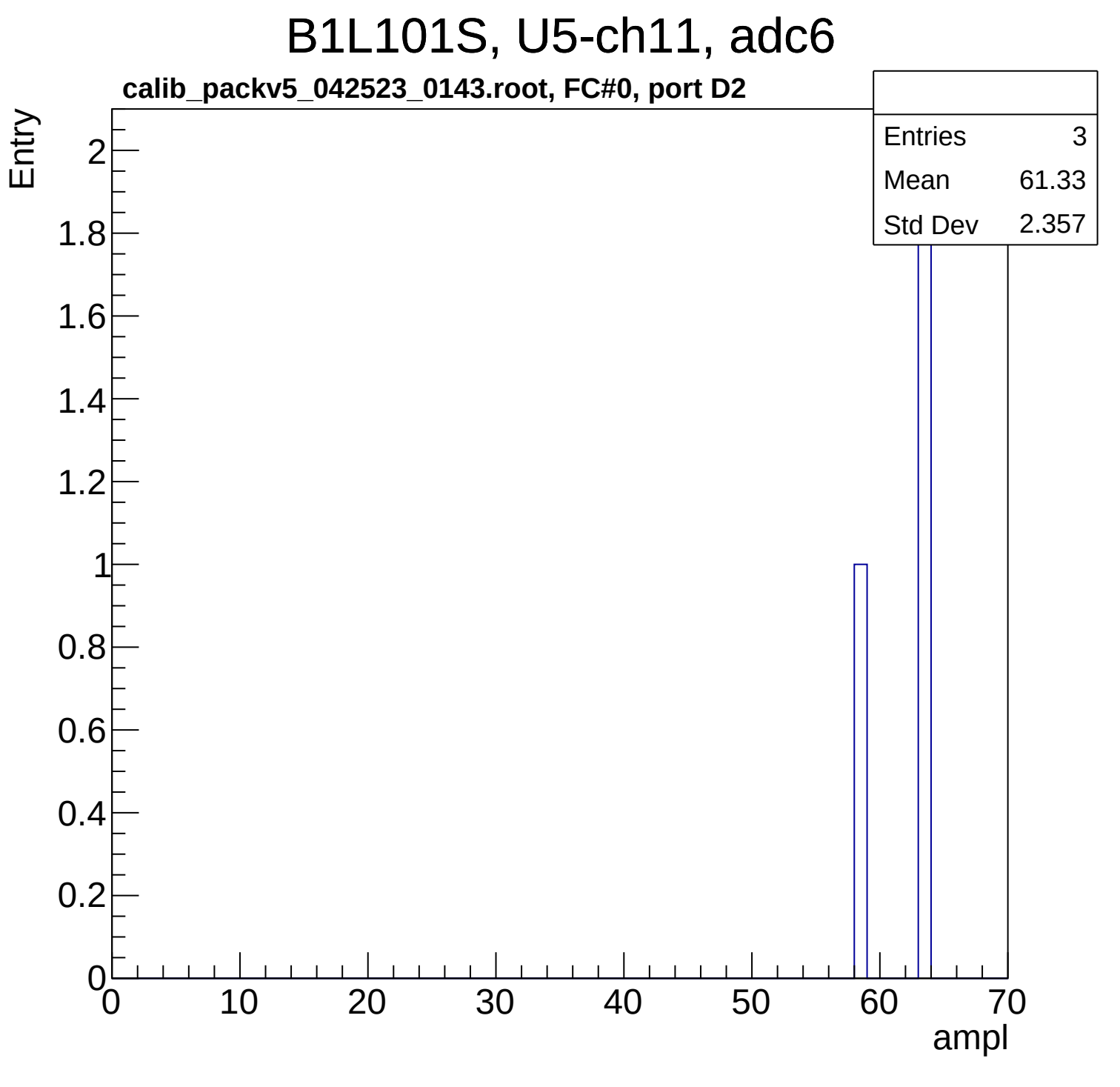
B1L101S, U5-ch11, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 61.33
Std Dev 2.357
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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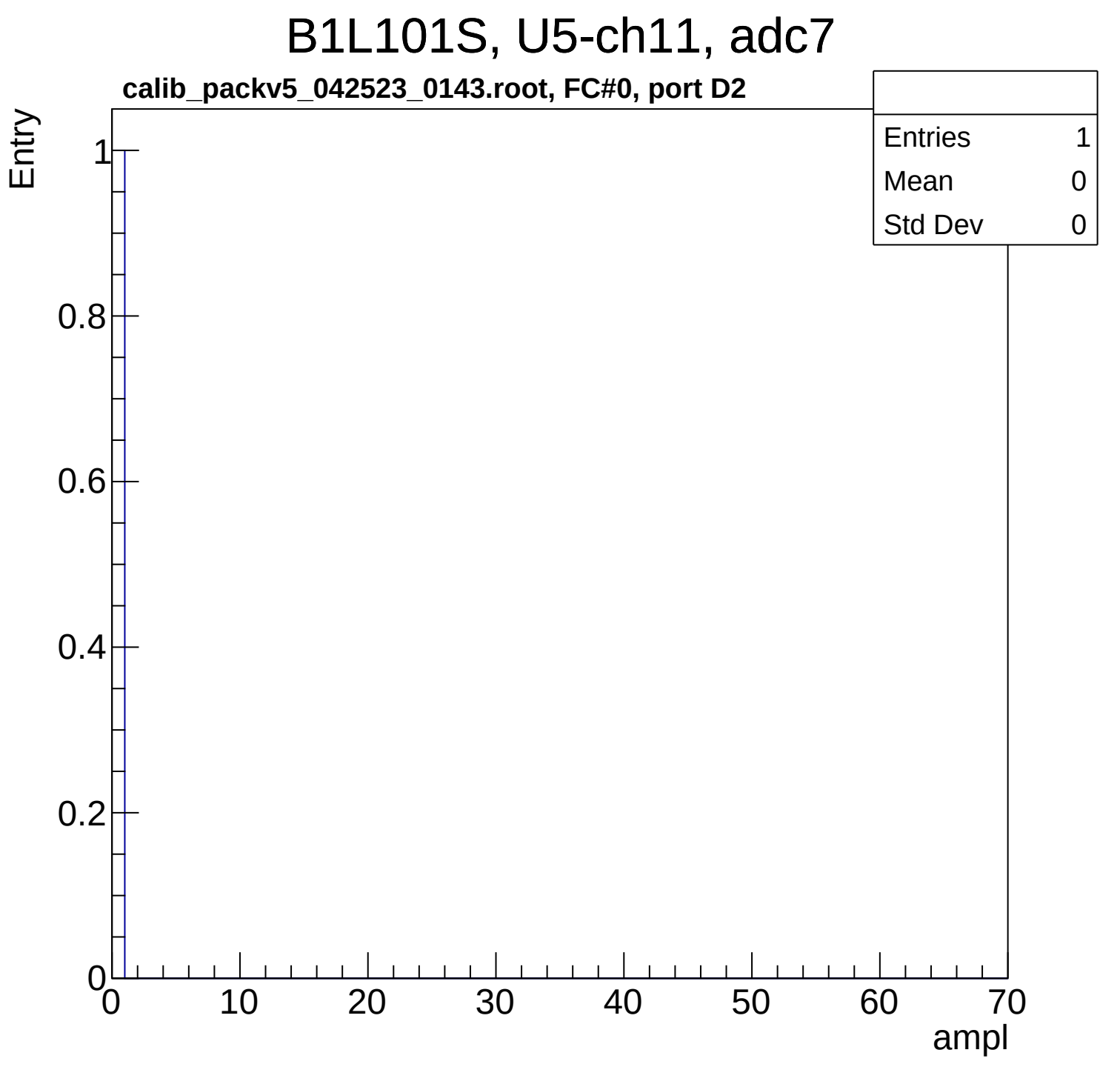
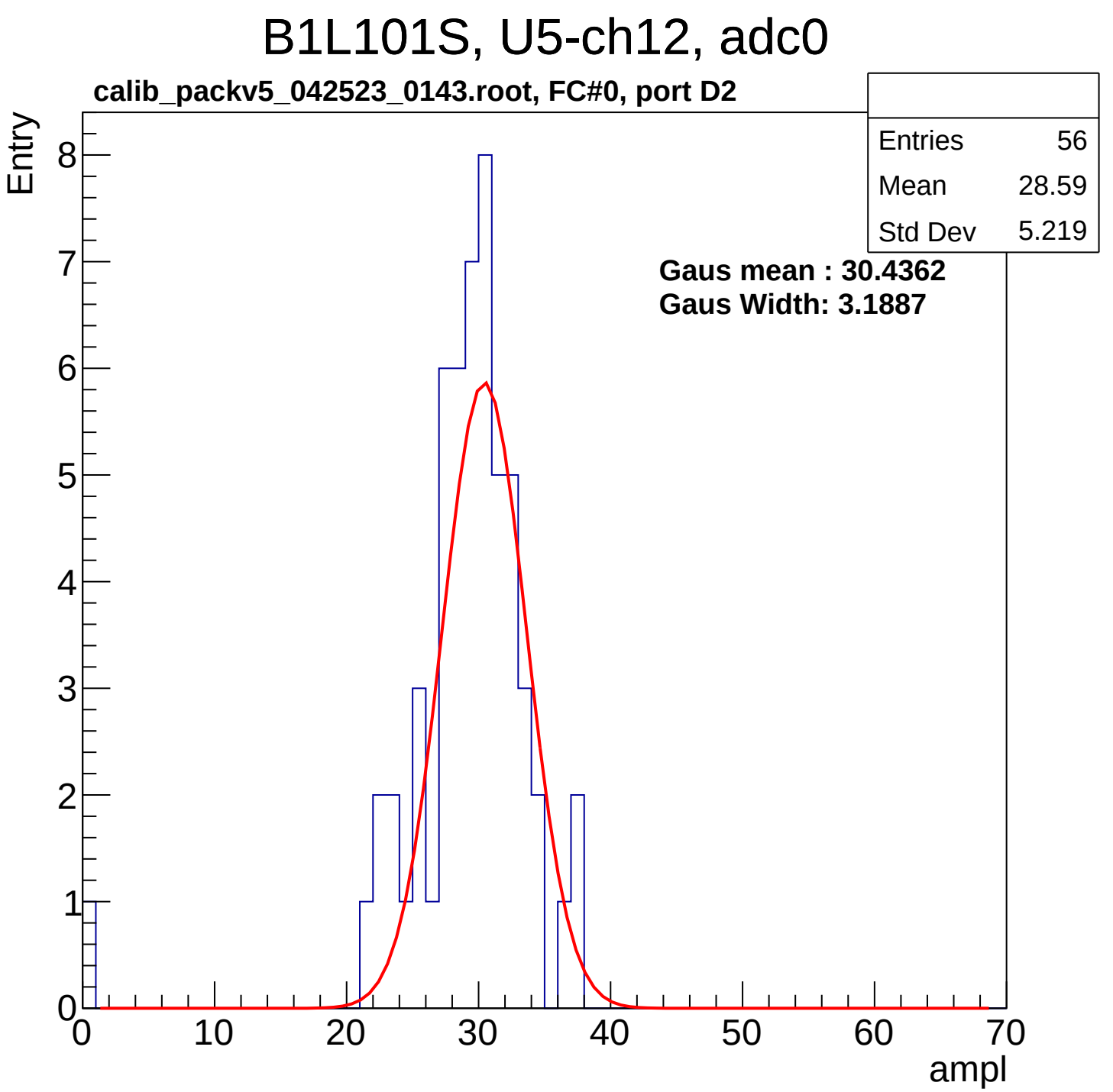
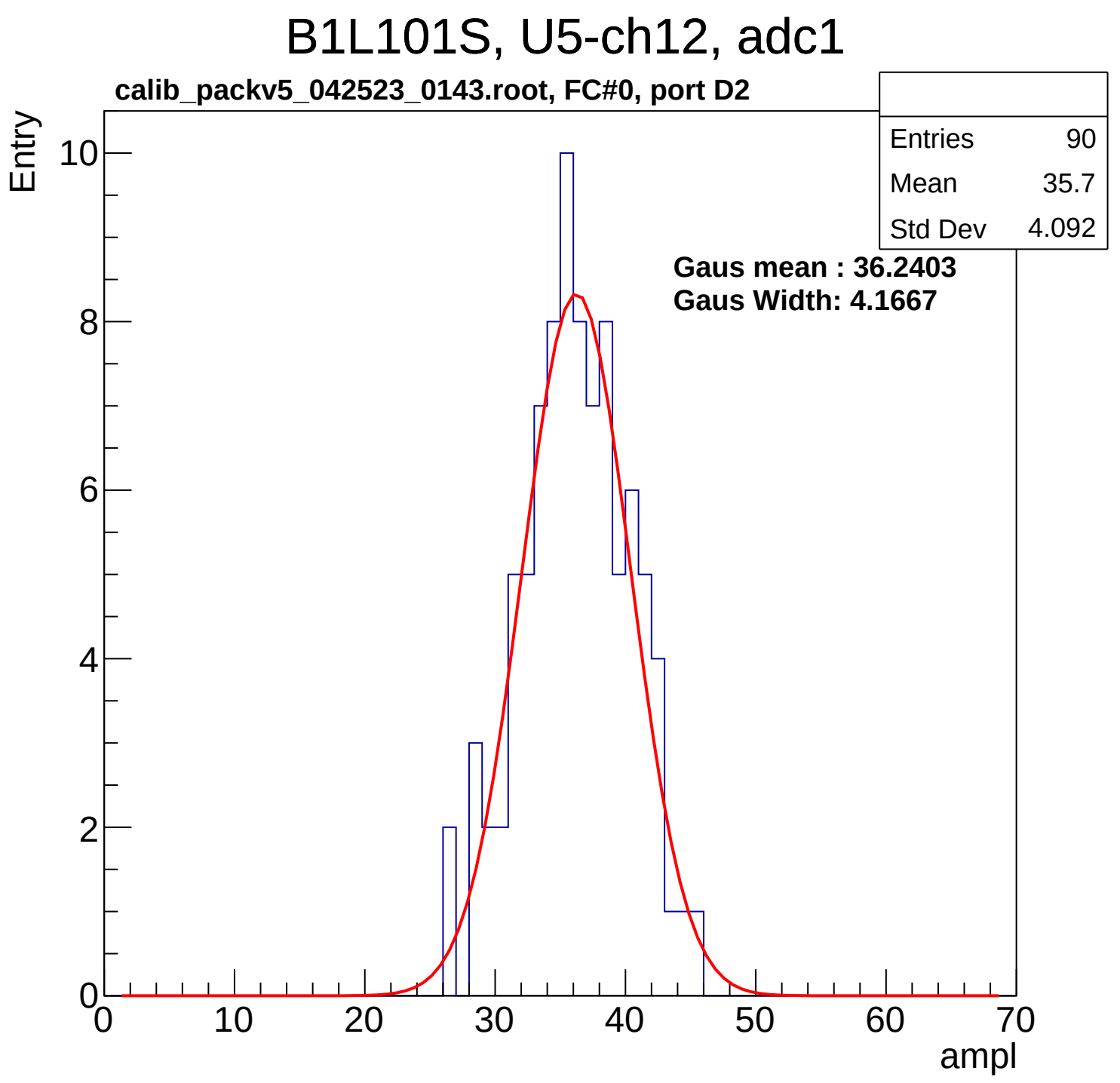
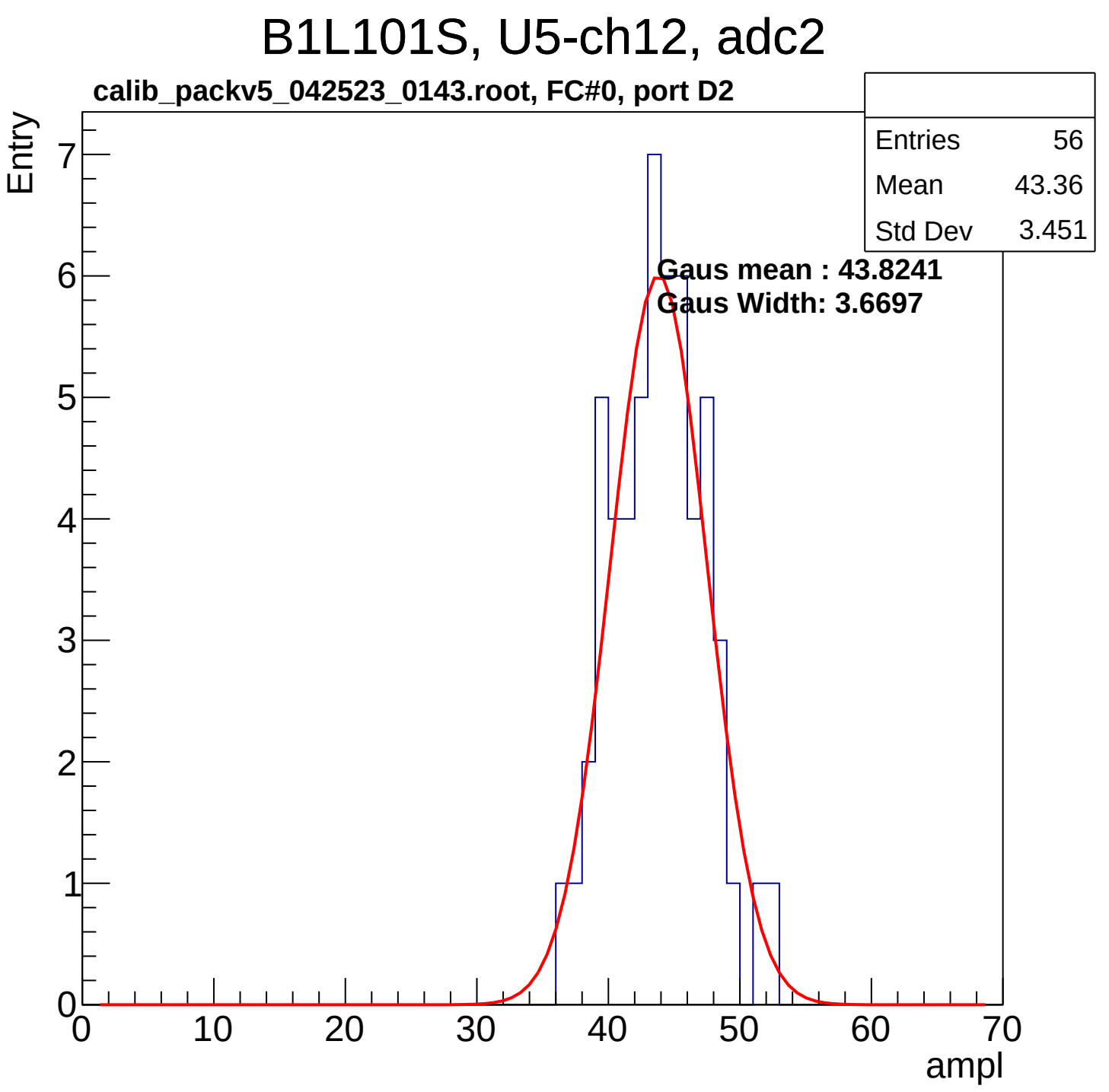

B1L101S, U5-ch11, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch12, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 28.59
Std Dev 5.219
Gaus mean : 30.4362
Gaus Width: 3.1887
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch12, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 90
Mean 35.7
Std Dev 4.092
Gaus mean : 36.2403
Gaus Width: 4.1667
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch12, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 43.36
Std Dev 3.451
Gaus mean : 43.8241
Gaus Width: 3.6697
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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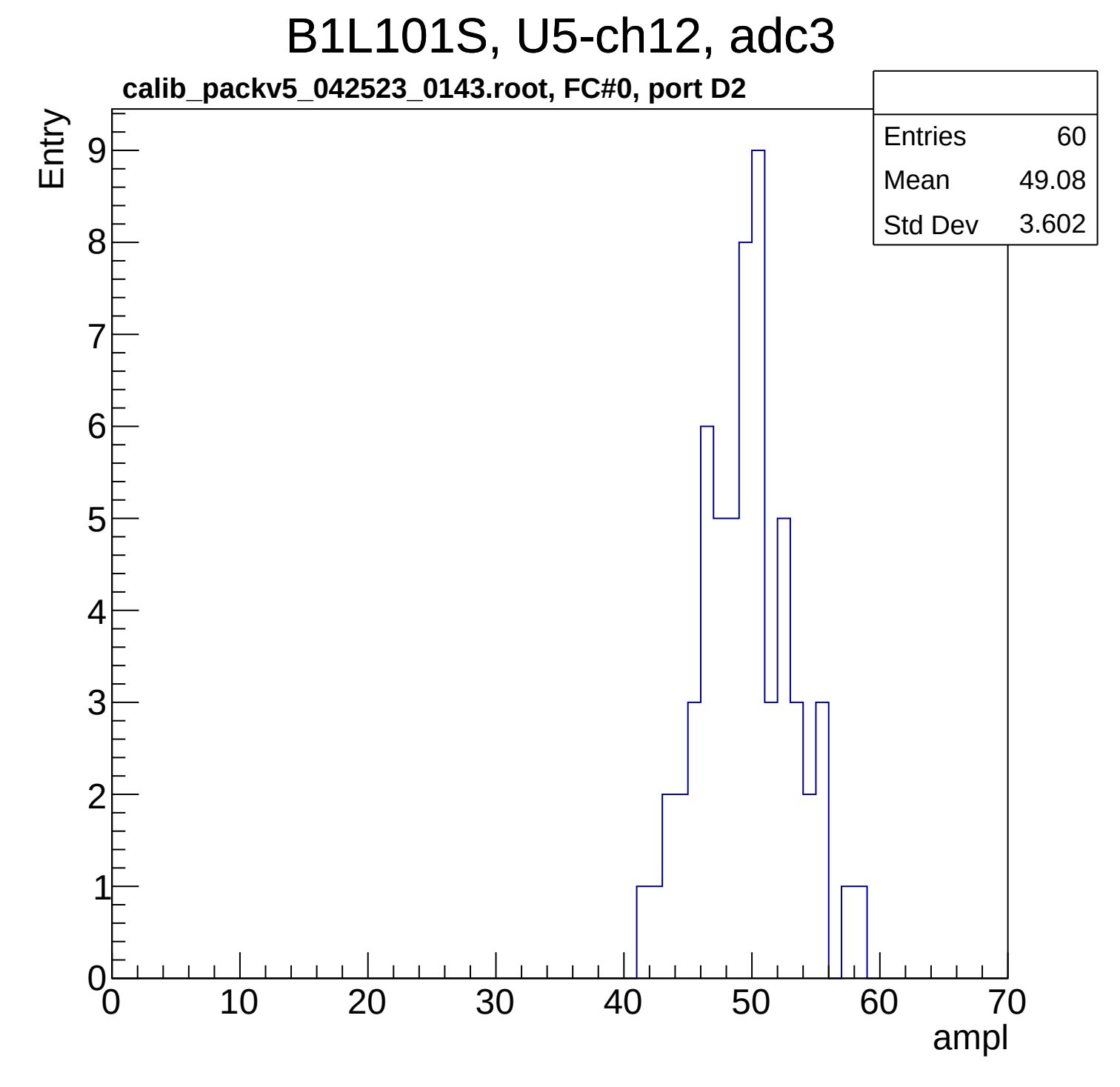
B1L101S, U5-ch12, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 49.08
Std Dev 3.602
Entry
ampl
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2
3
4
5
6
7
8
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0
10
20
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40
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60
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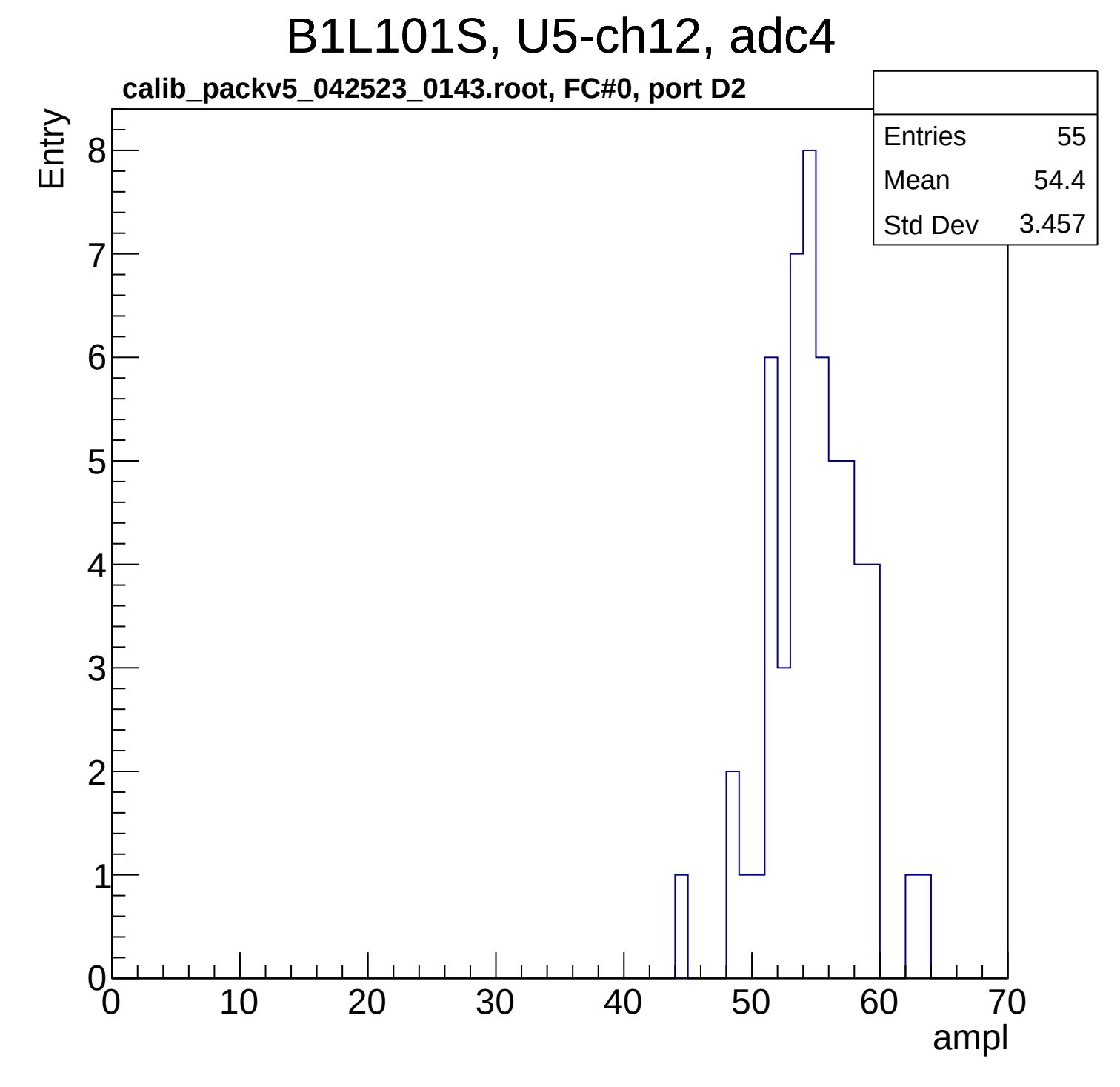
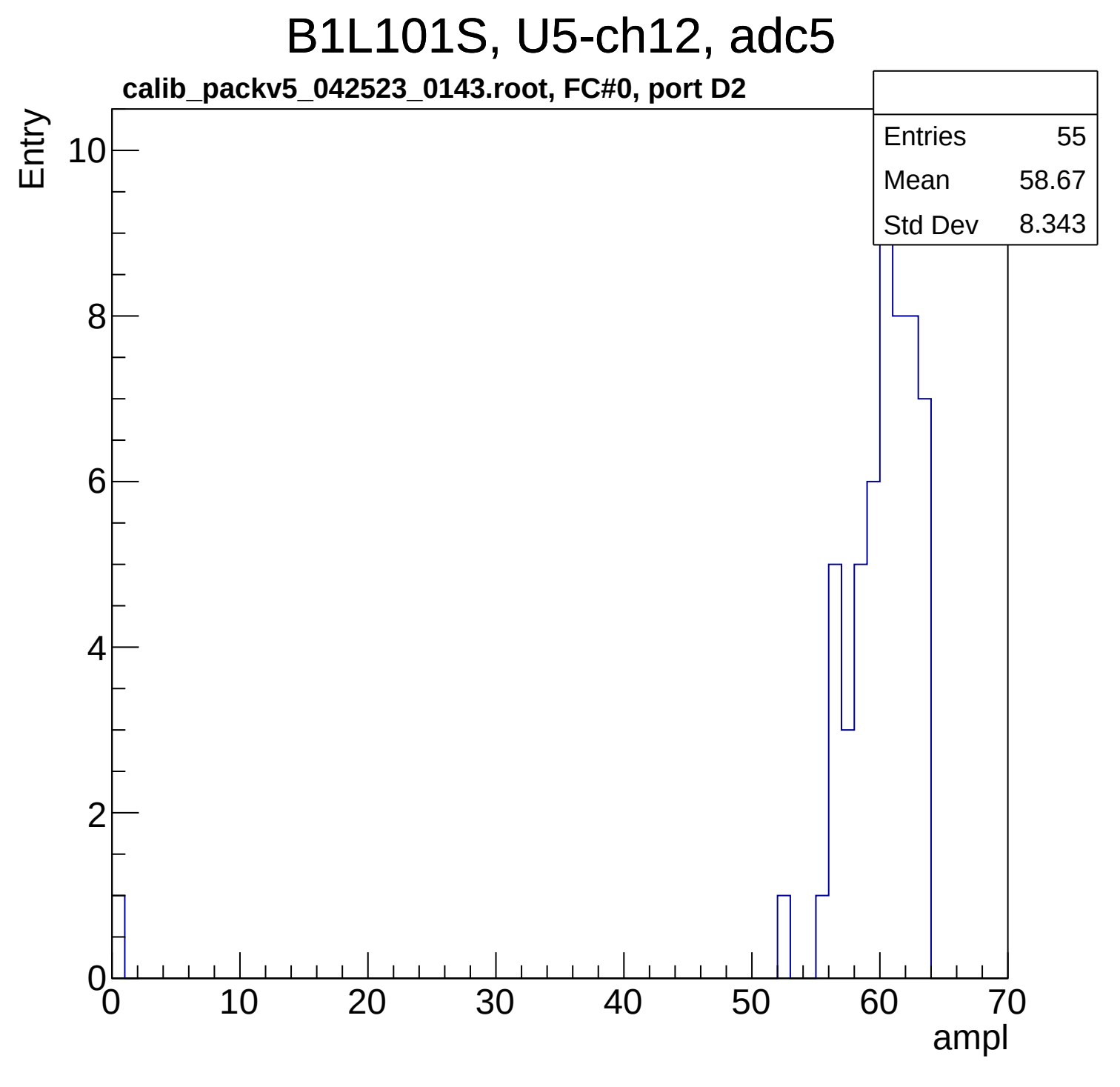
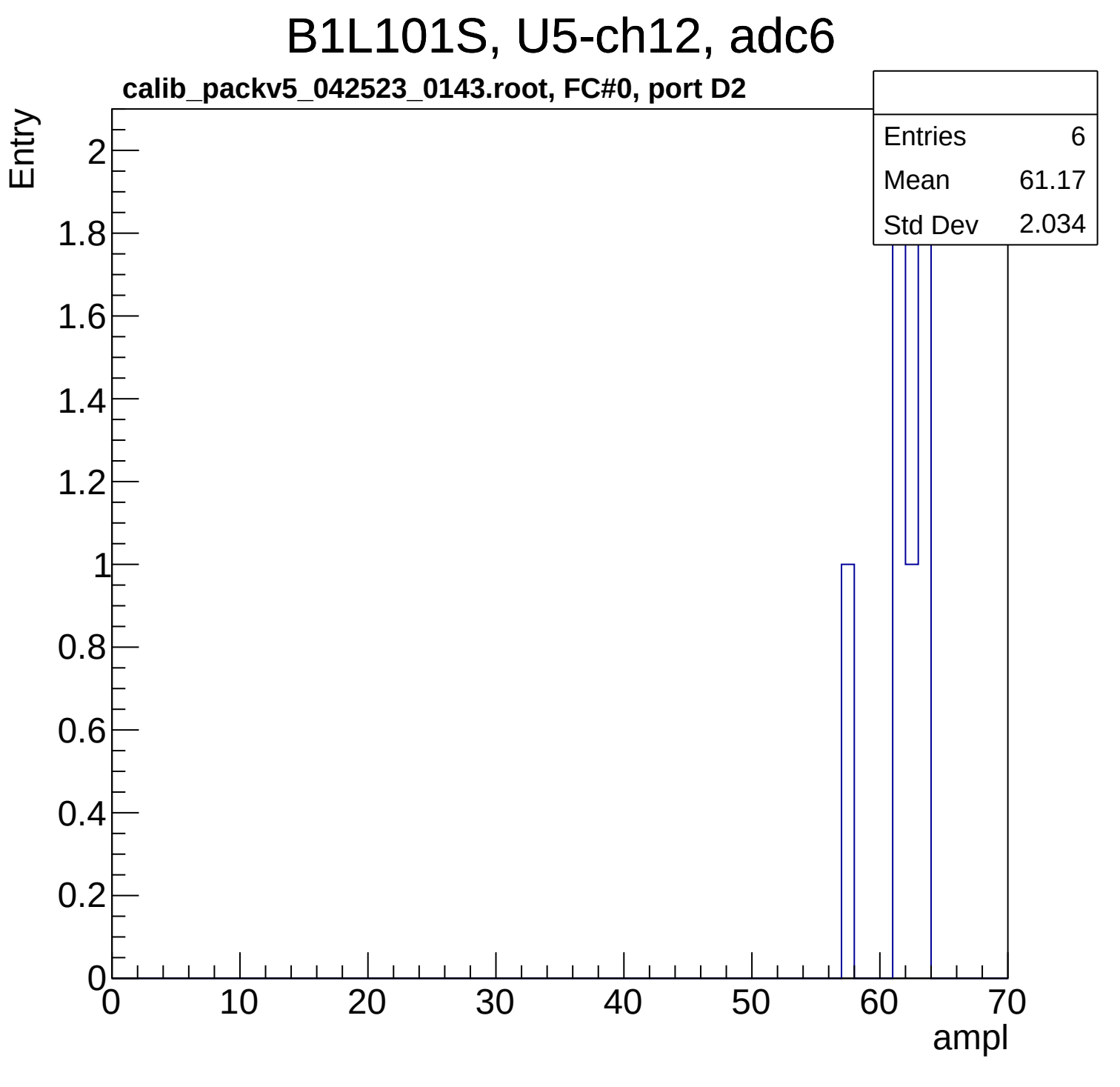
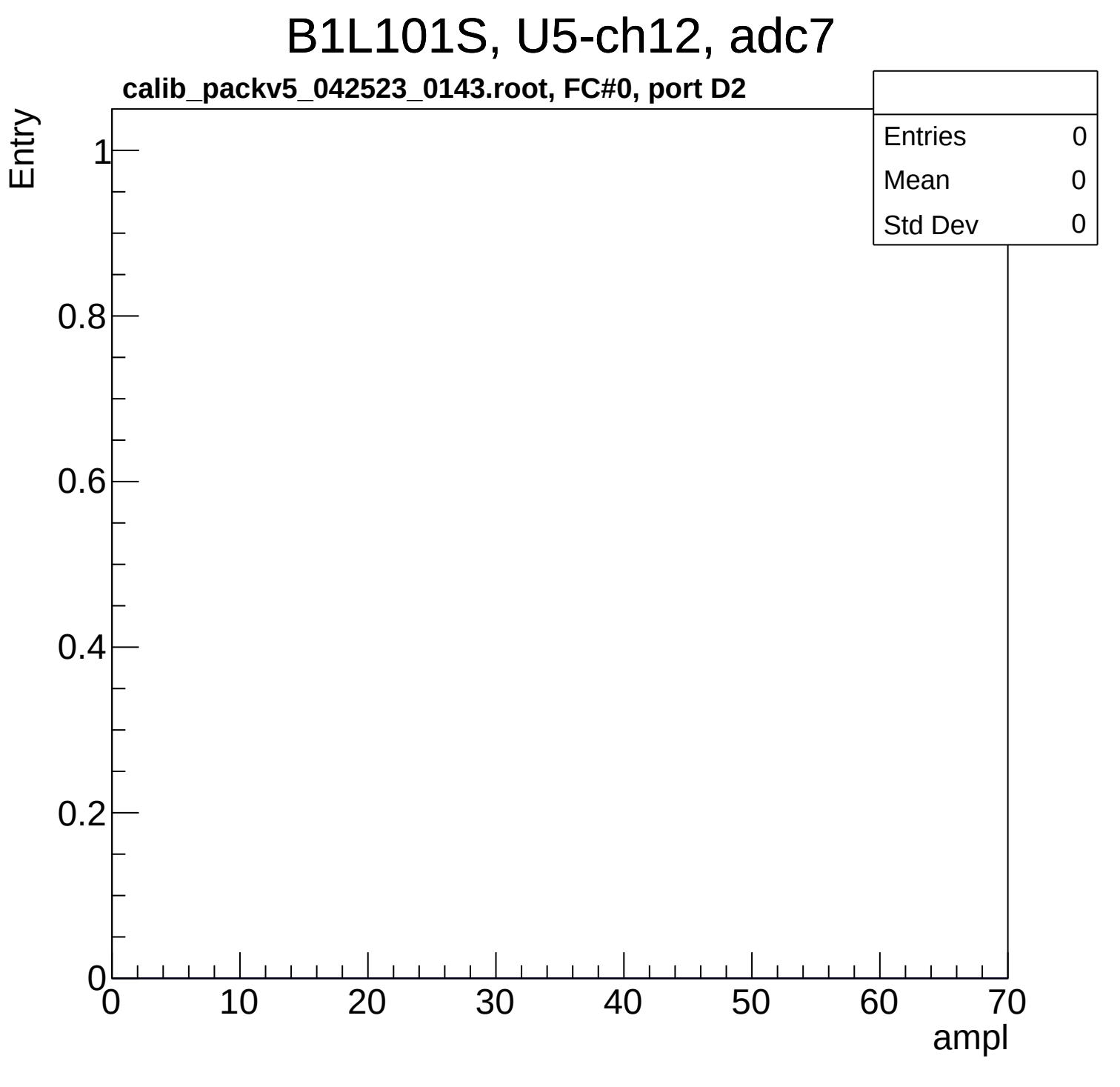
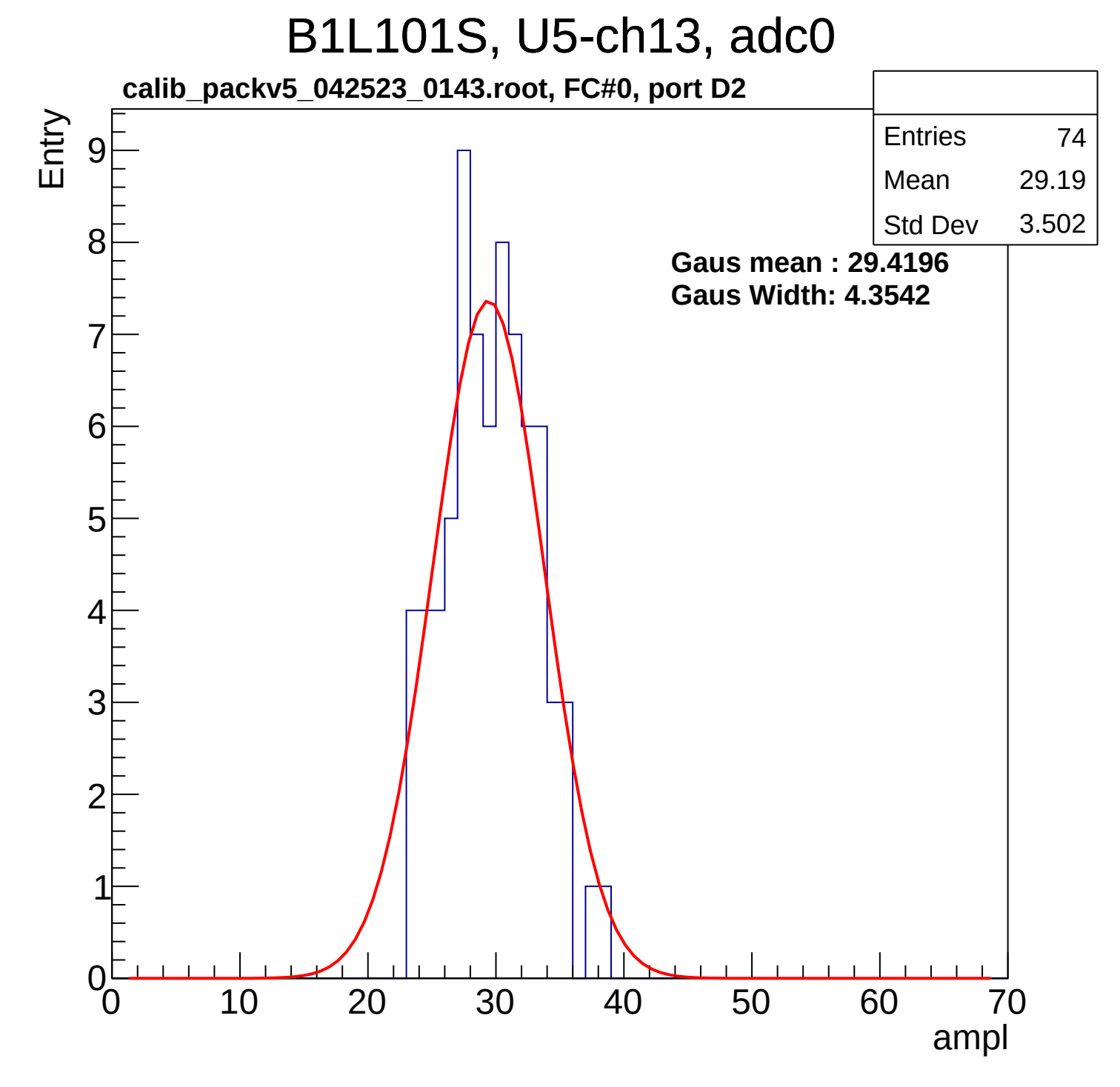
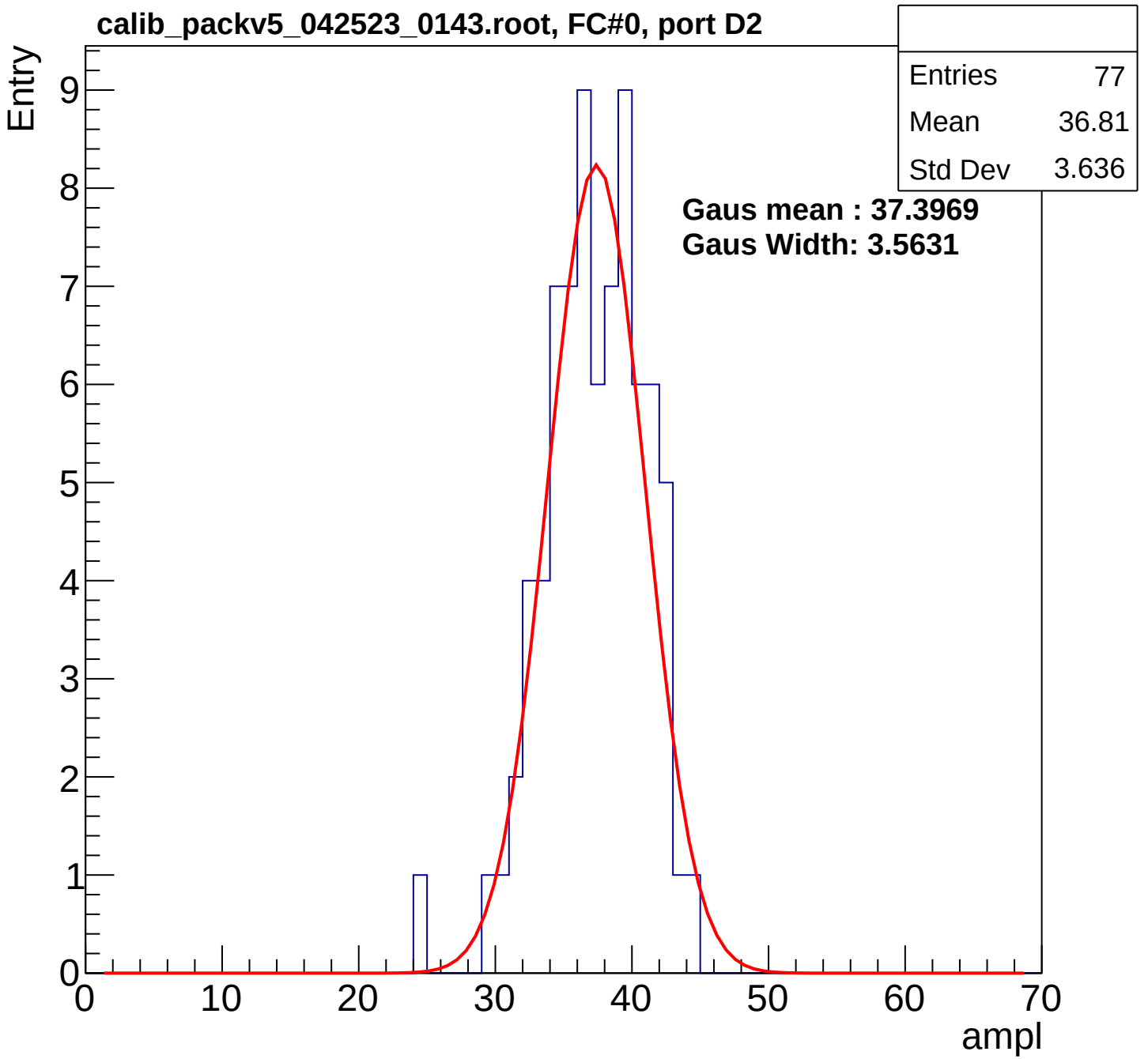

B1L101S, U5-ch12, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 54.4
Std Dev 3.457
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

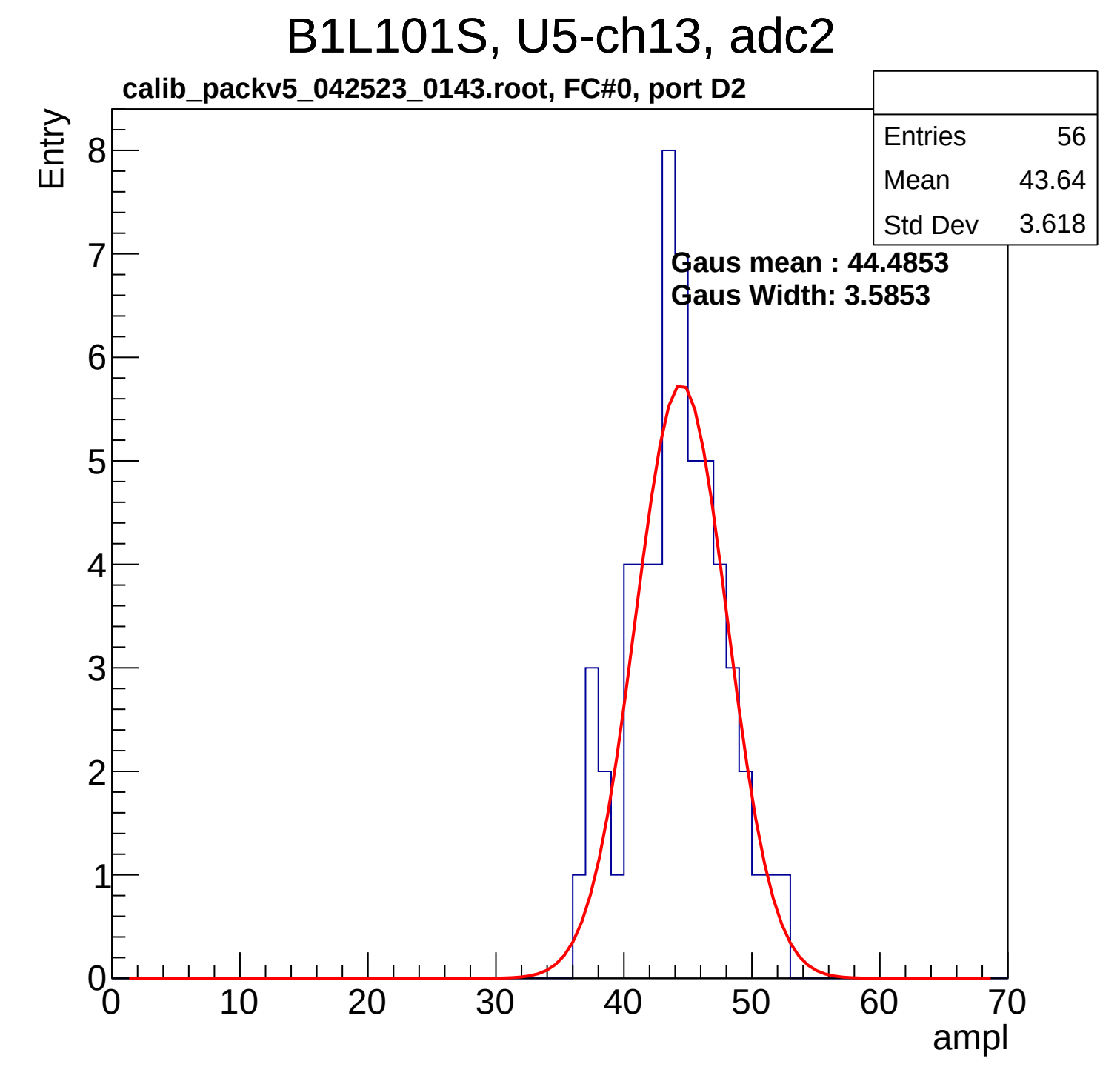

B1L101S, U5-ch12, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 58.67
Std Dev 8.343
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch12, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 61.17
Std Dev 2.034
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U5-ch12, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch13, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 29.19
Std Dev 3.502
Gaus mean : 29.4196
Gaus Width: 4.3542
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch13, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 36.81
Std Dev 3.636
Gaus mean : 37.3969
Gaus Width: 3.5631
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch13, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 43.64
Std Dev 3.618
Gaus mean : 44.4853
Gaus Width: 3.5853
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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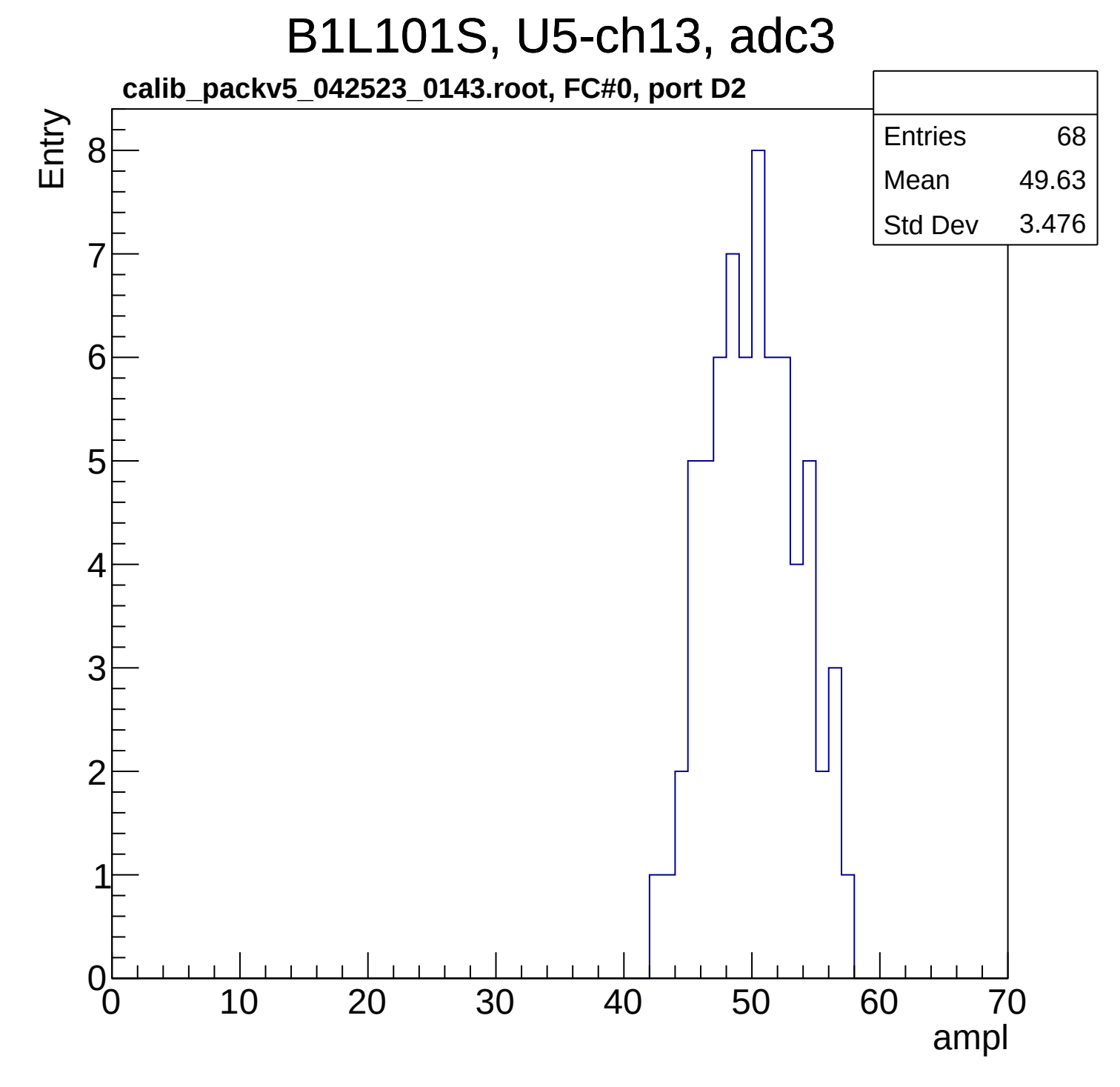
B1L101S, U5-ch13, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 49.63
Std Dev 3.476
Entry
ampl
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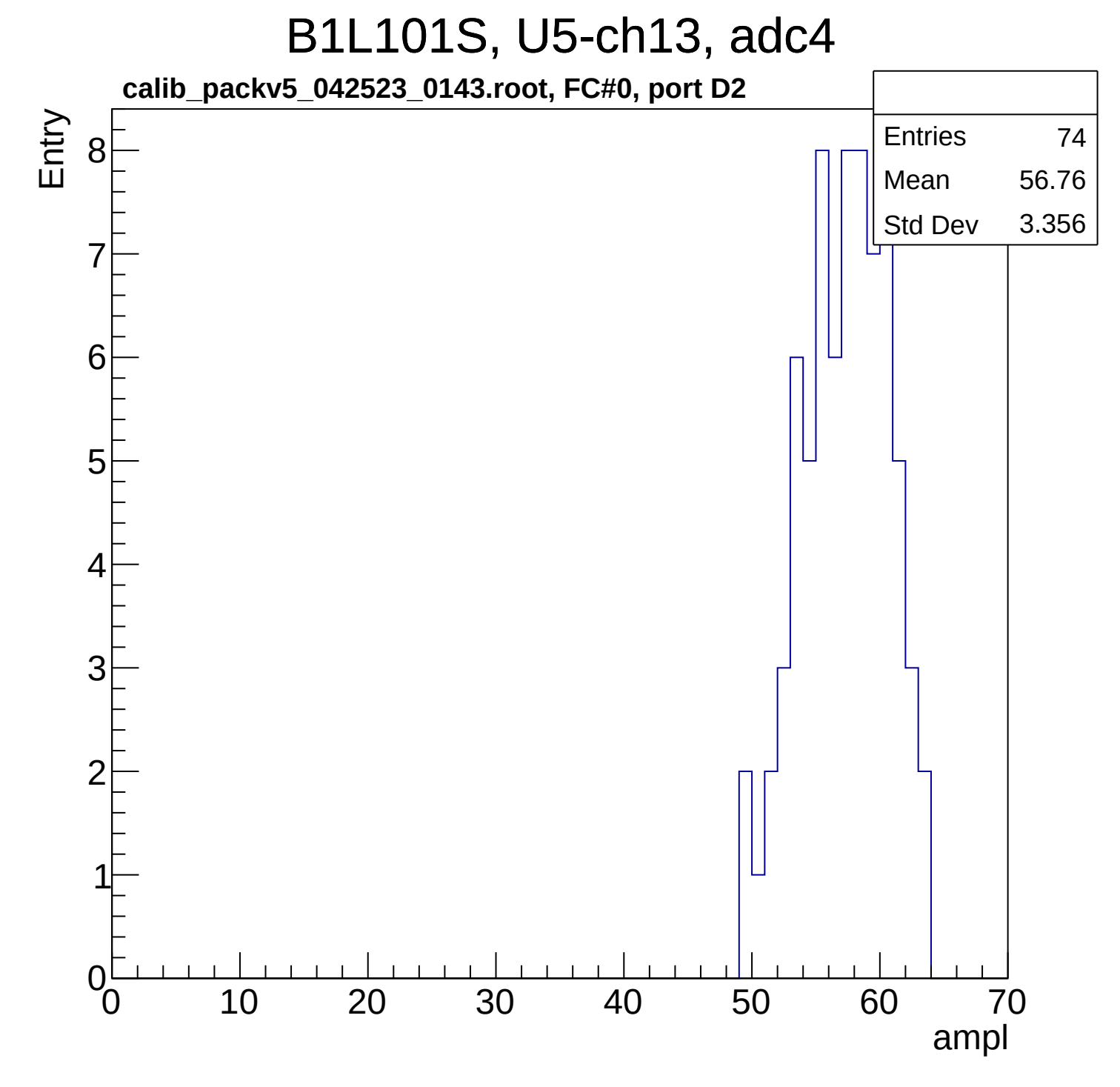
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch13, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 56.76
Std Dev 3.356
Entry
ampl
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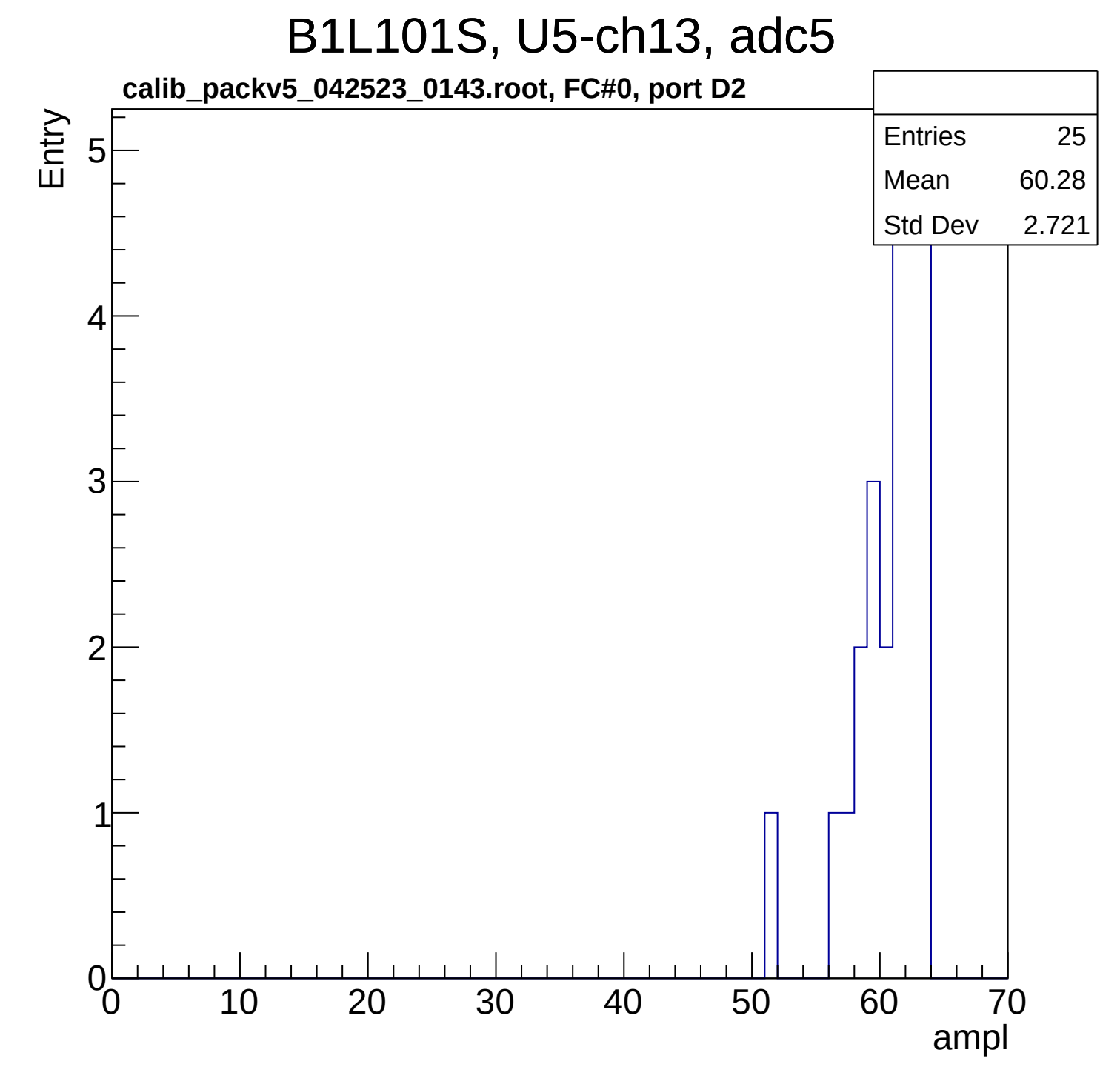
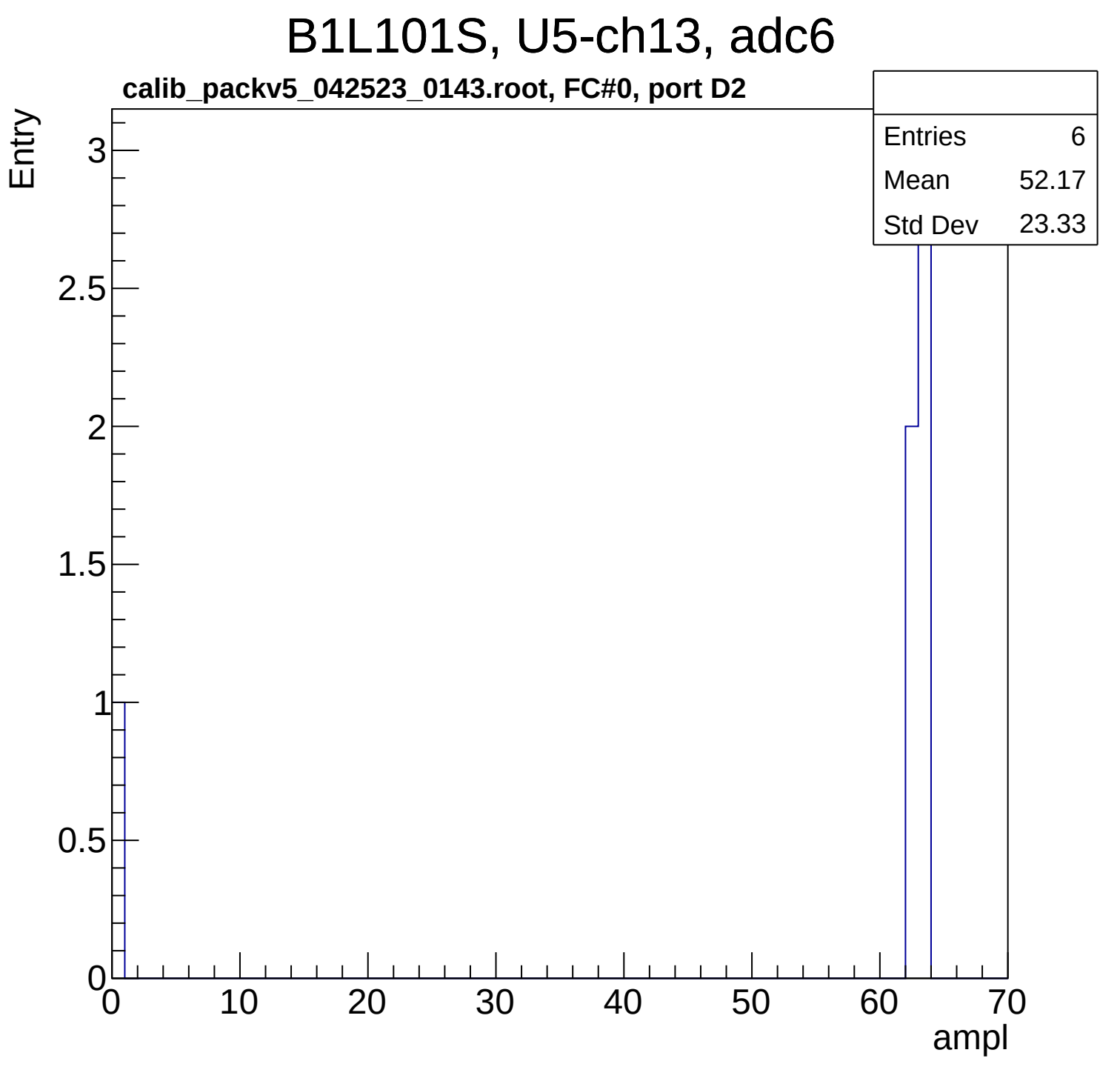
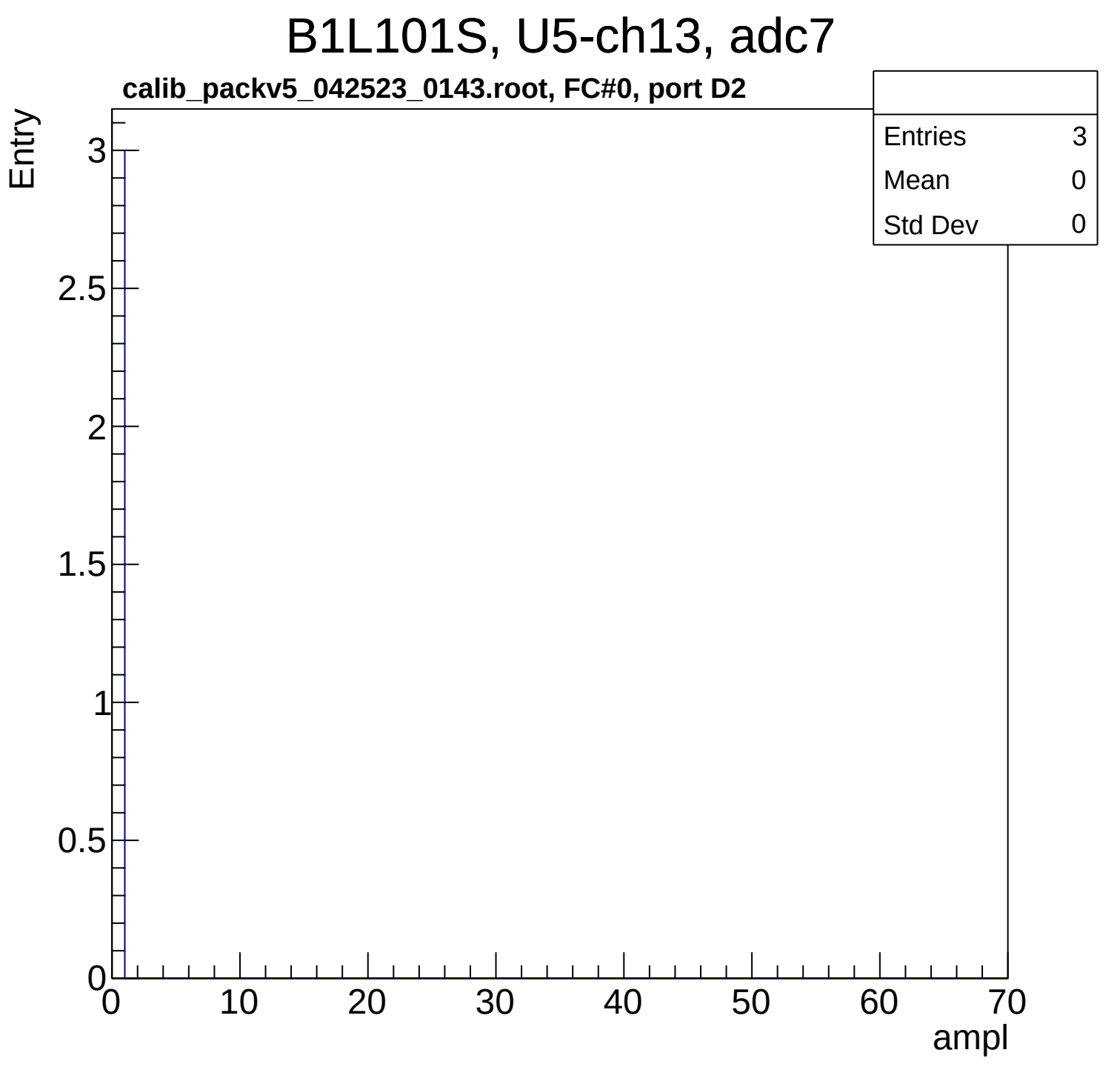
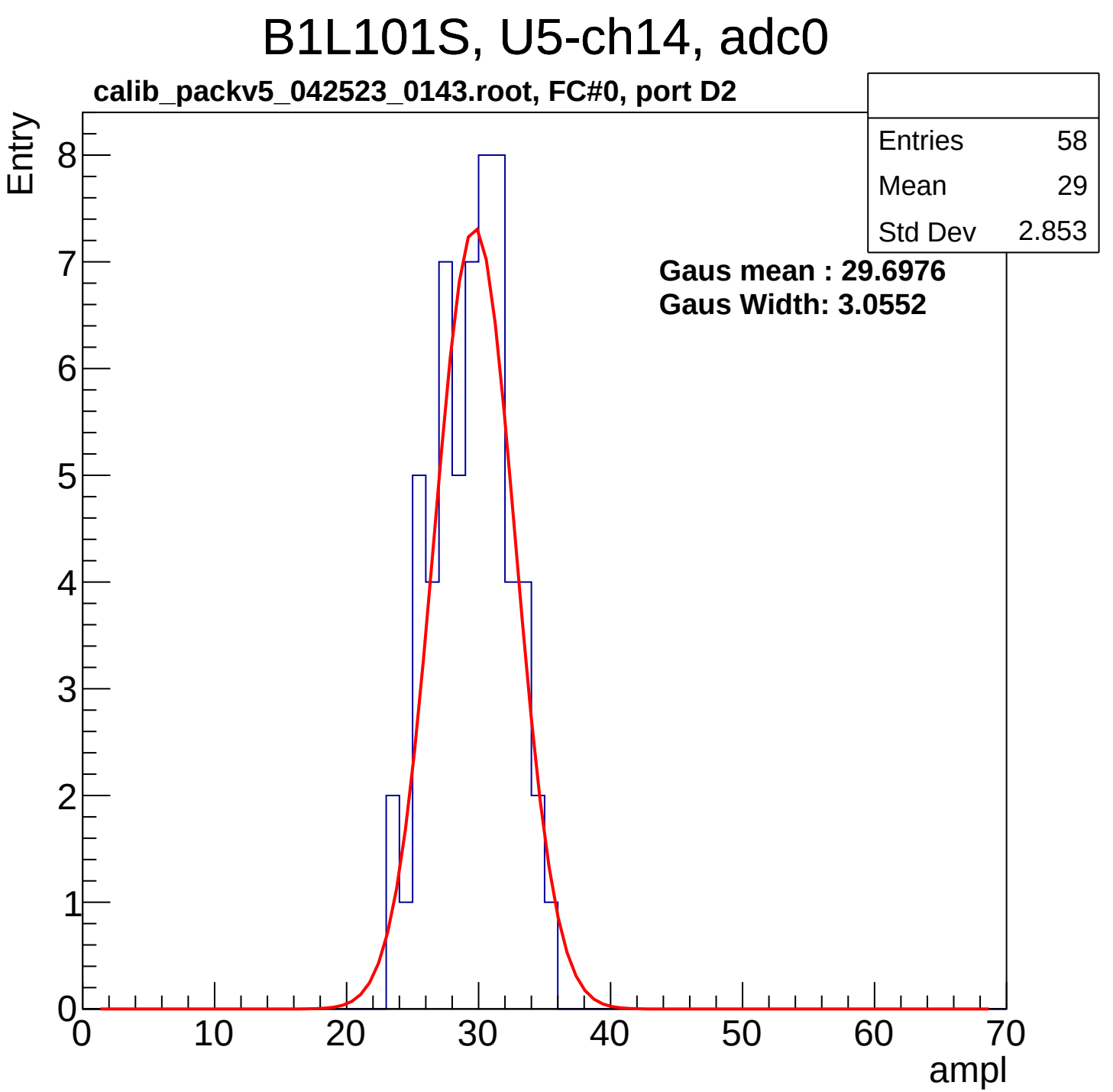
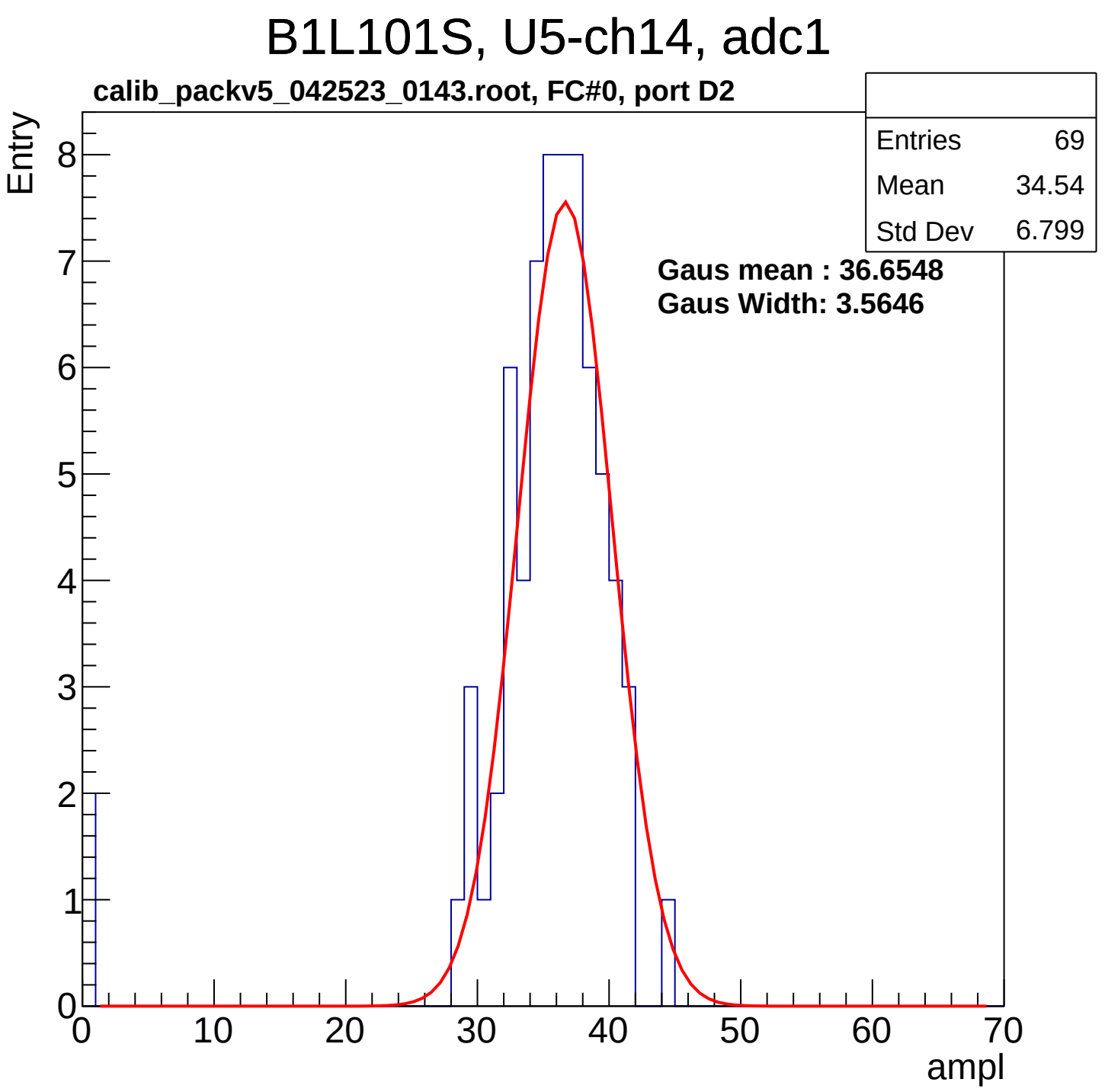
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

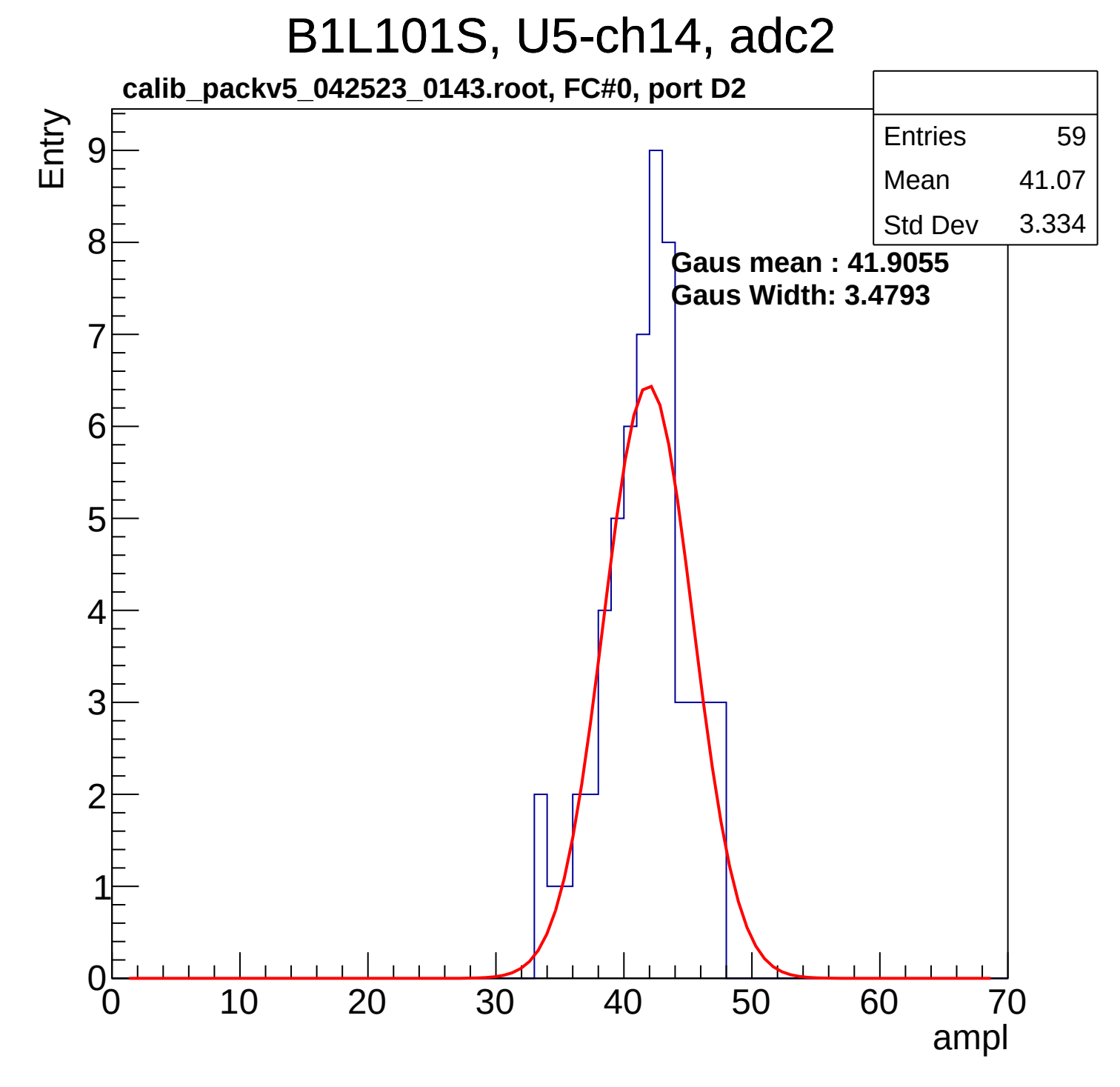

B1L101S, U5-ch13, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 25
Mean 60.28
Std Dev 2.721
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

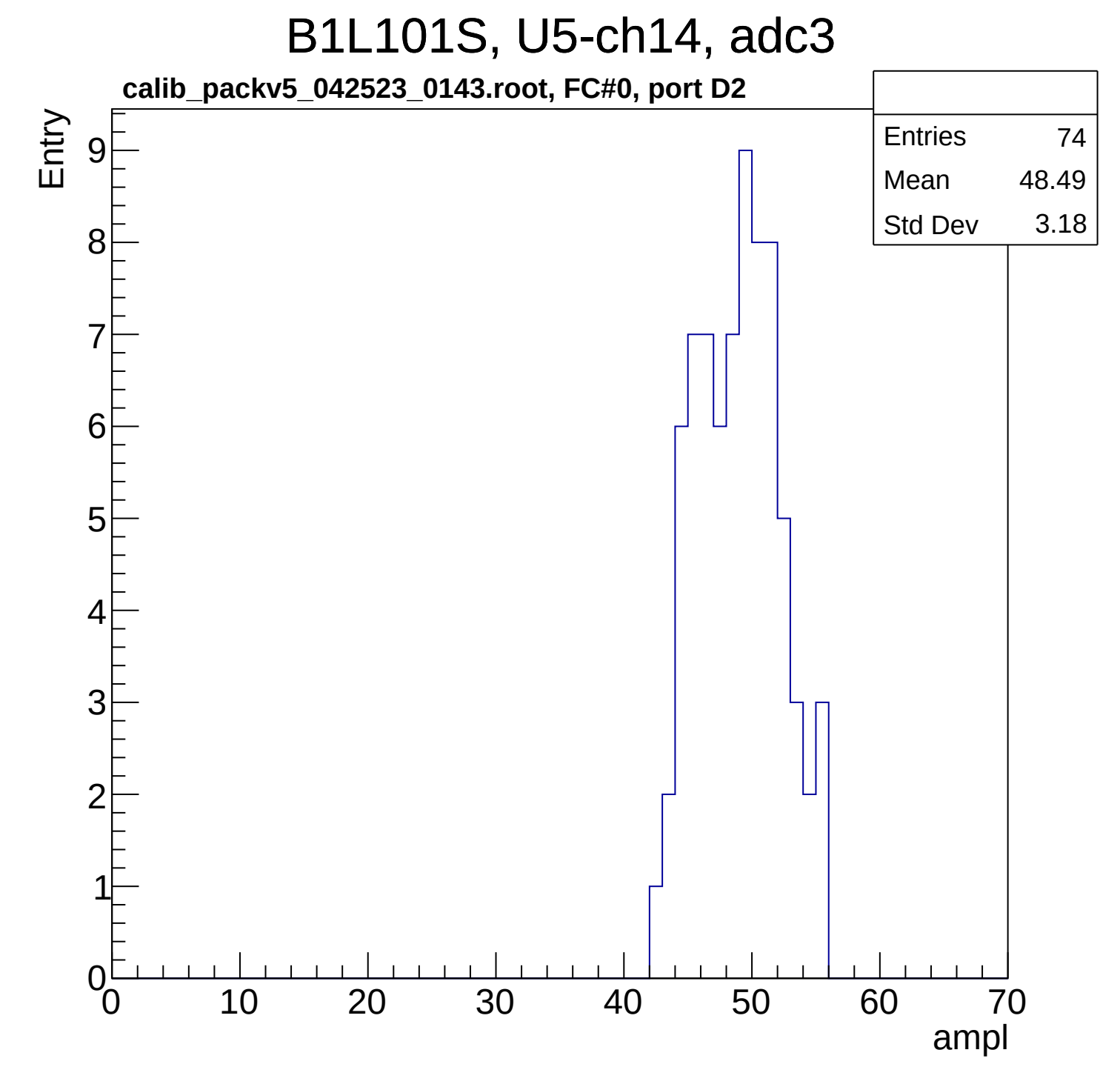

B1L101S, U5-ch13, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 52.17
Std Dev 23.33
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U5-ch13, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 0
Std Dev 0
Entry
3
2.5
2
1.5
1
0.5
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch14, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 29
Std Dev 2.853
Gaus mean : 29.6976
Gaus Width: 3.0552
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch14, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 34.54
Std Dev 6.799
Gaus mean : 36.6548
Gaus Width: 3.5646
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch14, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 41.07
Std Dev 3.334
Gaus mean : 41.9055
Gaus Width: 3.4793
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L101S, U5-ch14, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 48.49
Std Dev 3.18
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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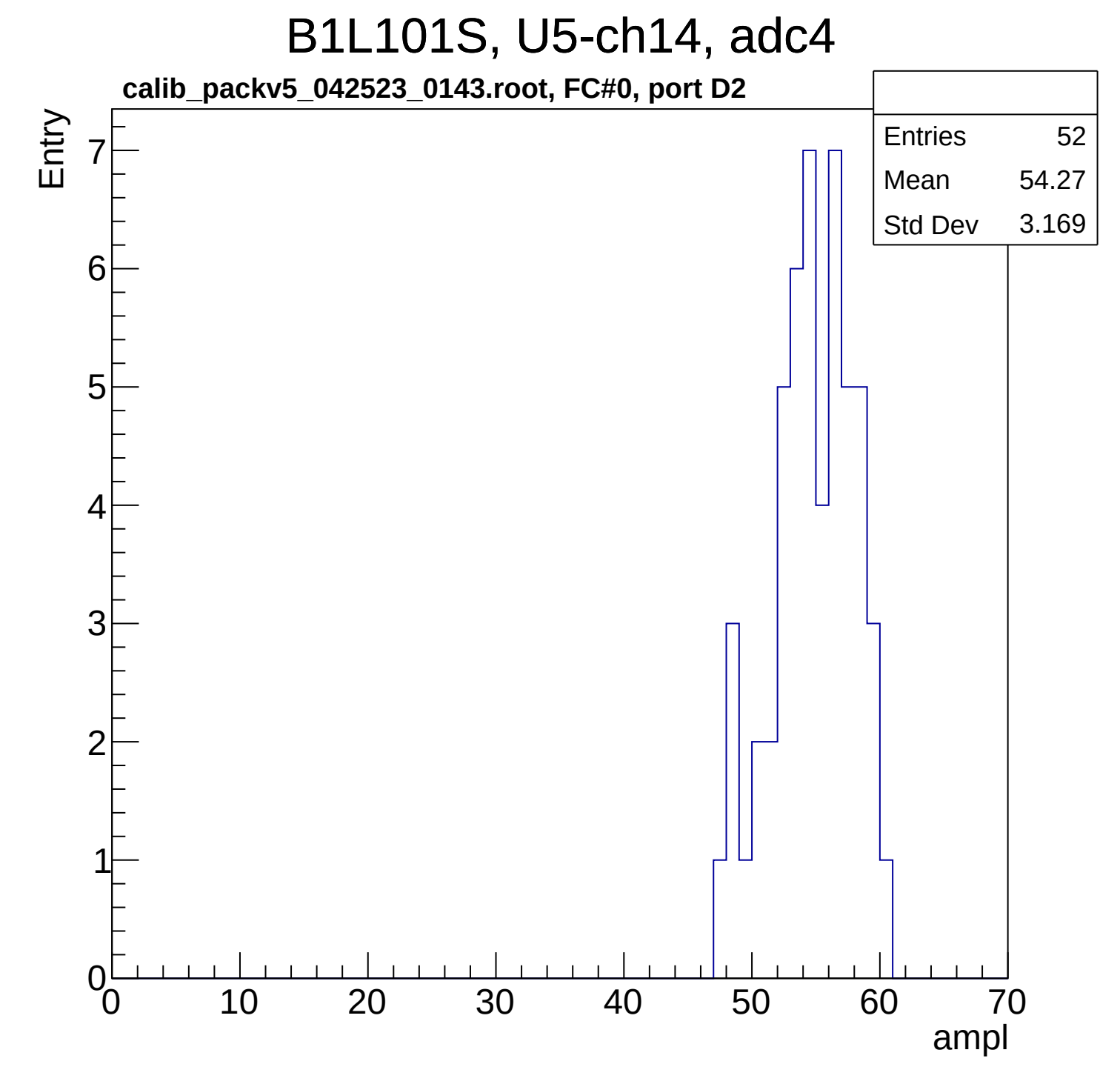
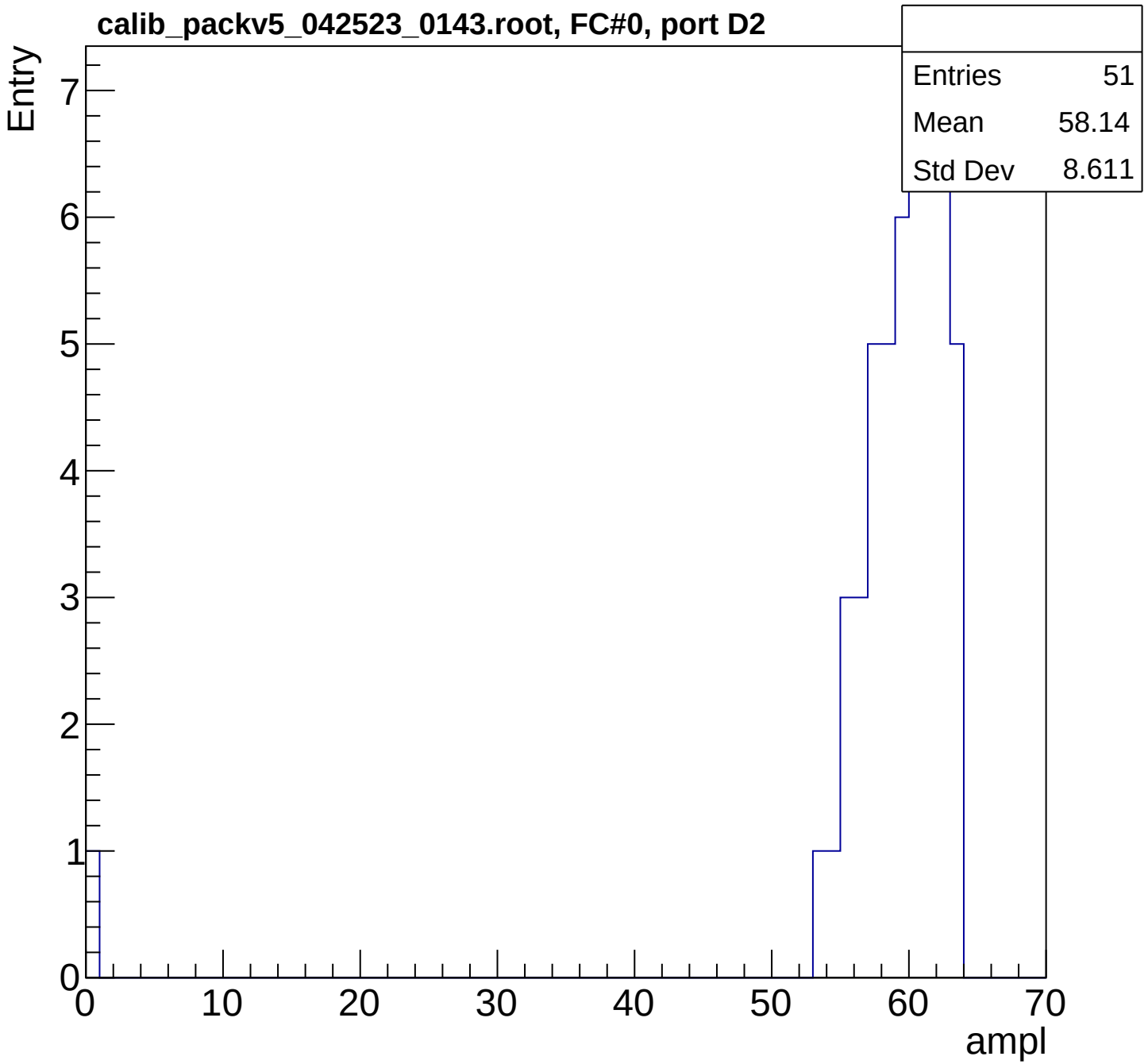

B1L101S, U5-ch14, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 54.27
Std Dev 3.169
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch14, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 58.14
Std Dev 8.611
Entry
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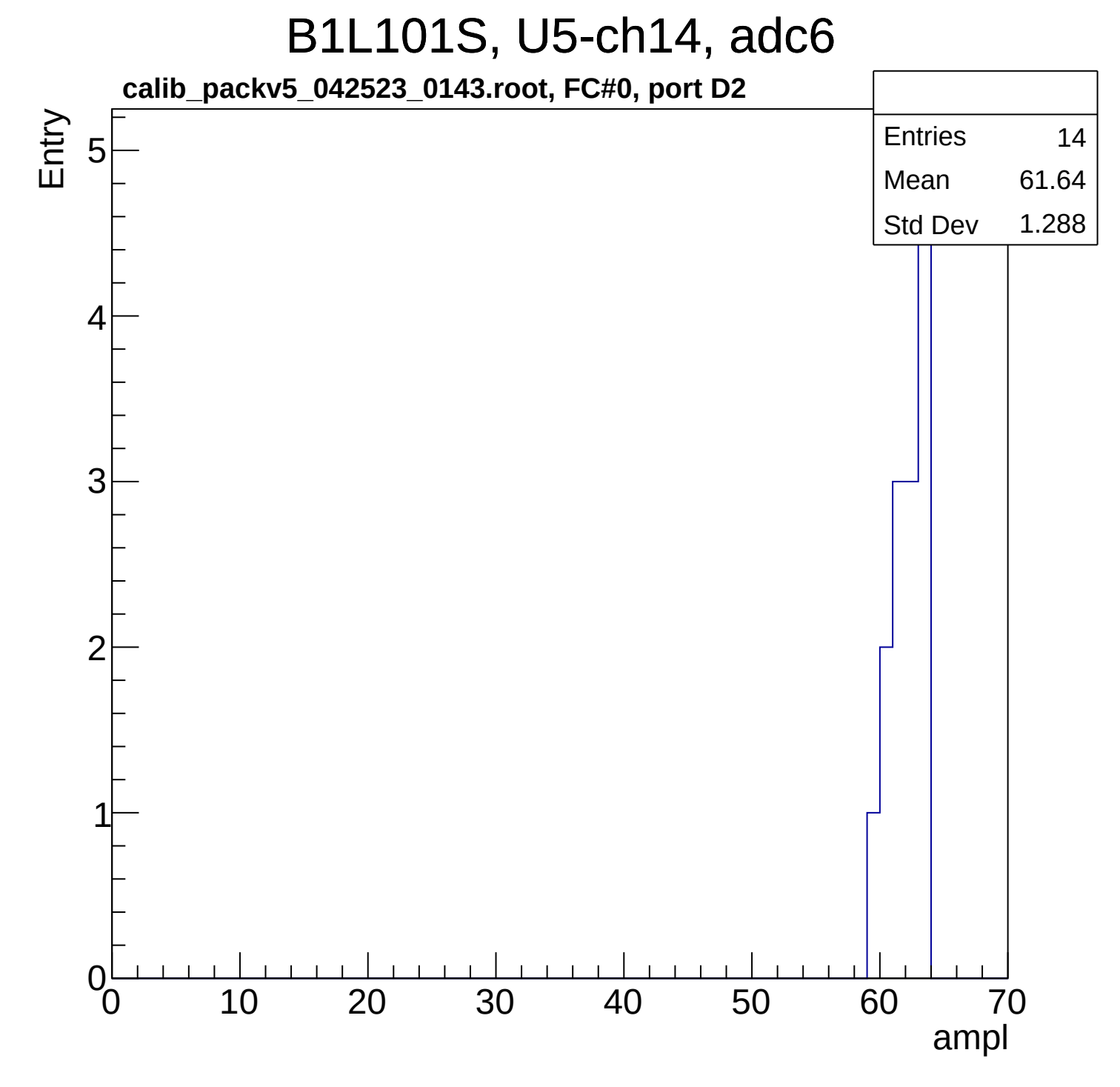
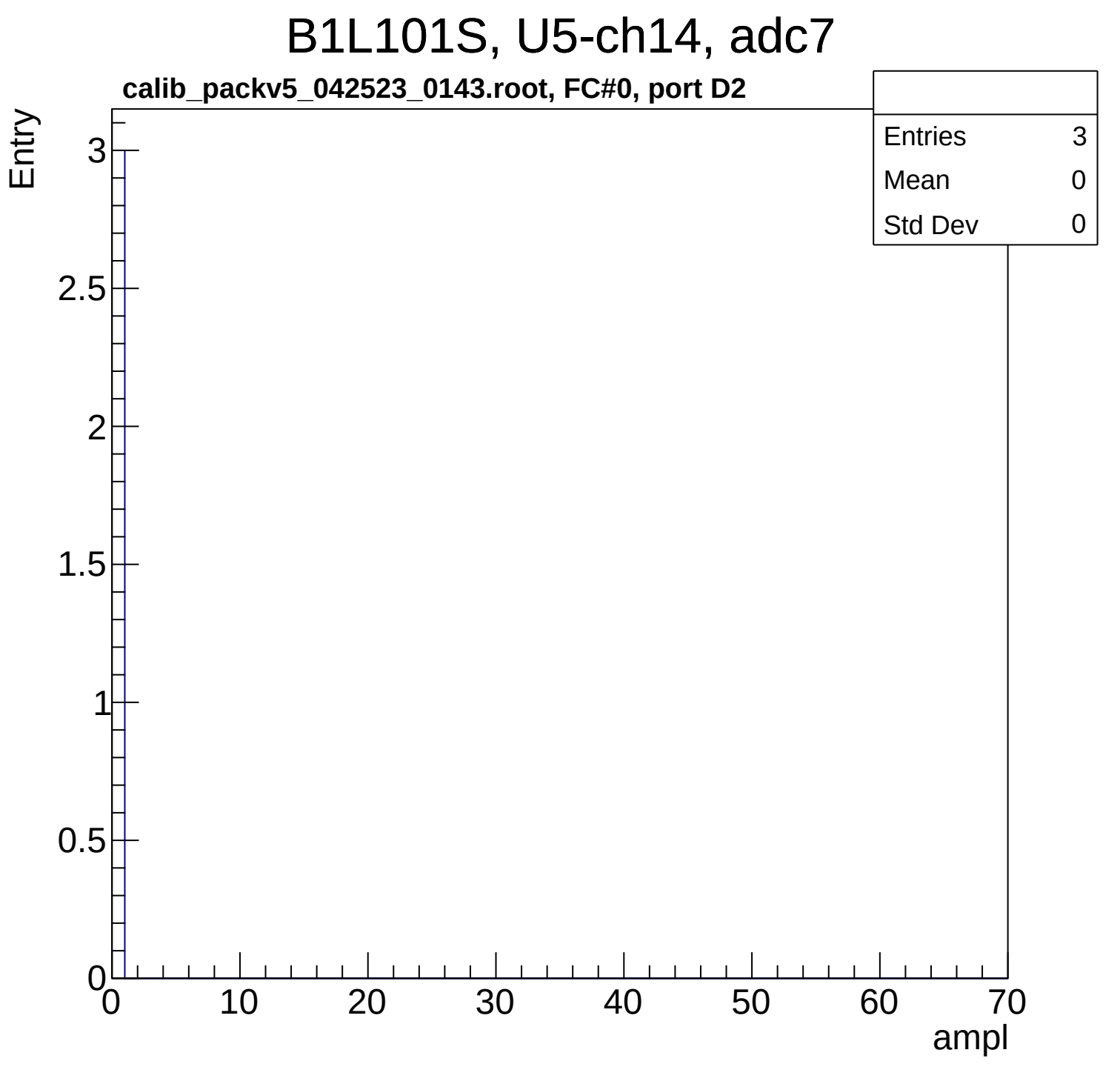
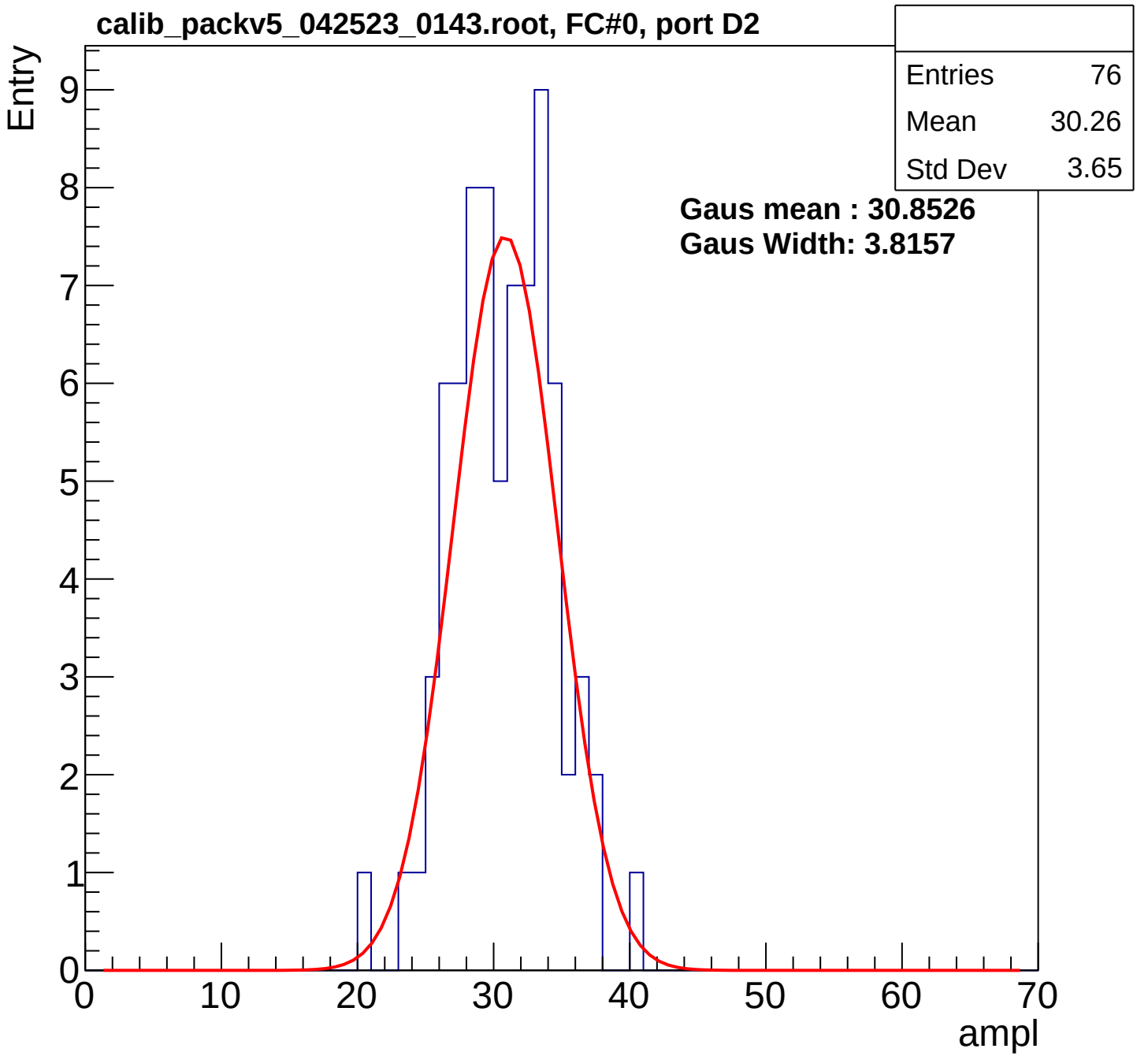
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch14, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 14
Mean 61.64
Std Dev 1.288
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch14, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 0
Std Dev 0
Entry
3
2.5
2
1.5
1
0.5
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch15, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 30.26
Std Dev 3.65
Gaus mean : 30.8526
Gaus Width: 3.8157
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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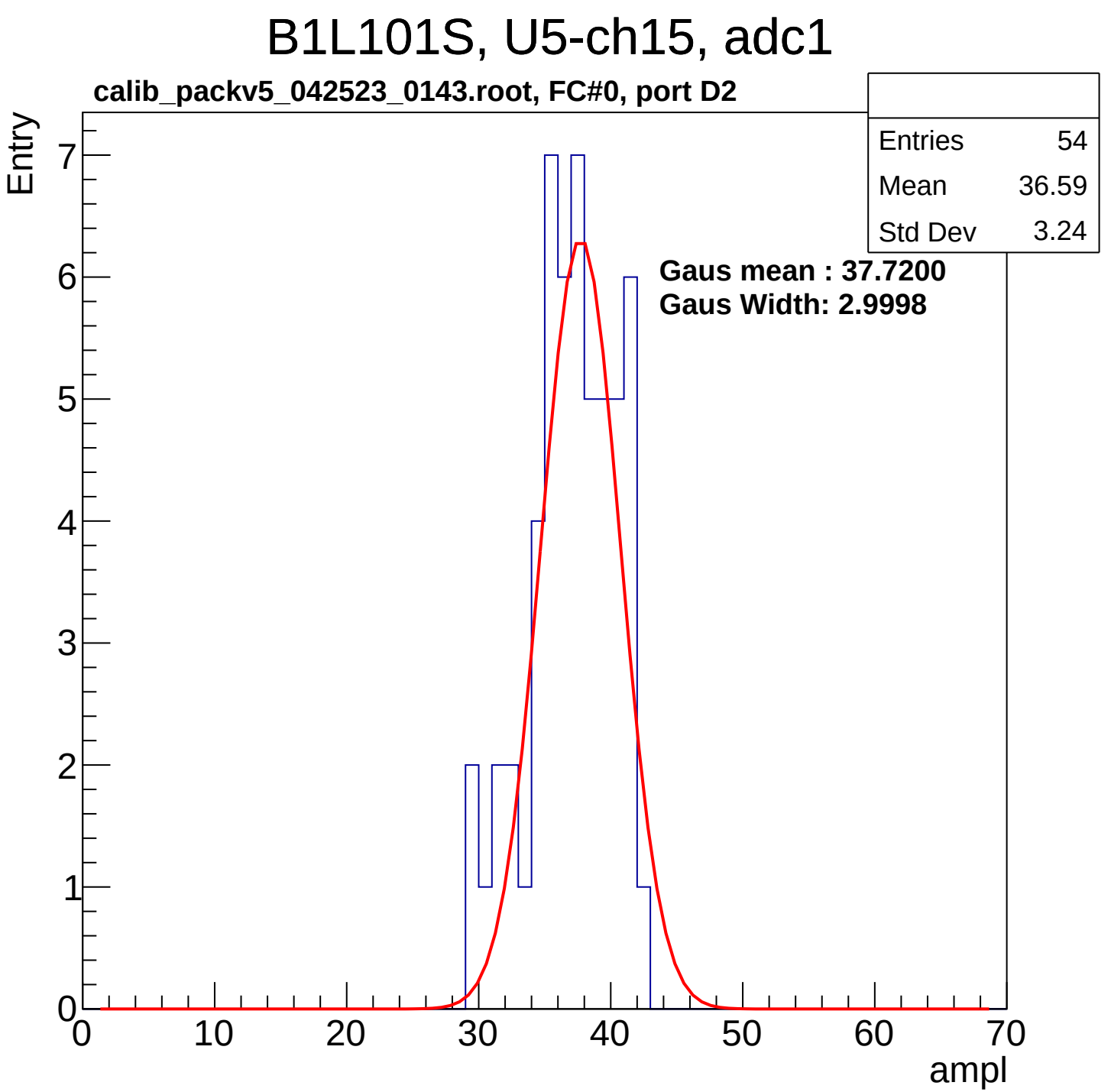
B1L101S, U5-ch15, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 36.59
Std Dev 3.24
Gaus mean : 37.7200
Gaus Width: 2.9998
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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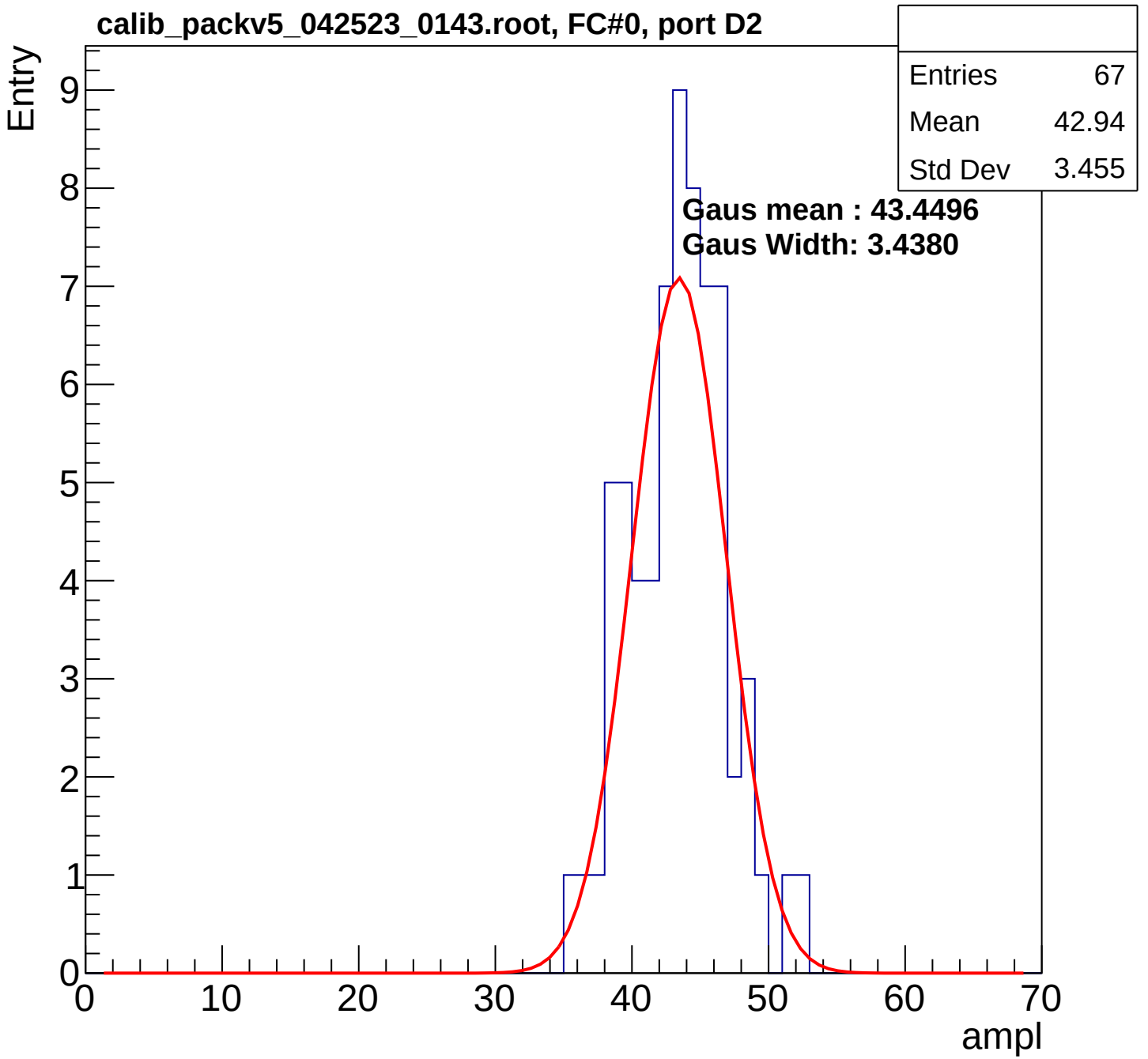
B1L101S, U5-ch15, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 42.94
Std Dev 3.455
Gaus mean : 43.4496
Gaus Width: 3.4380
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
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60
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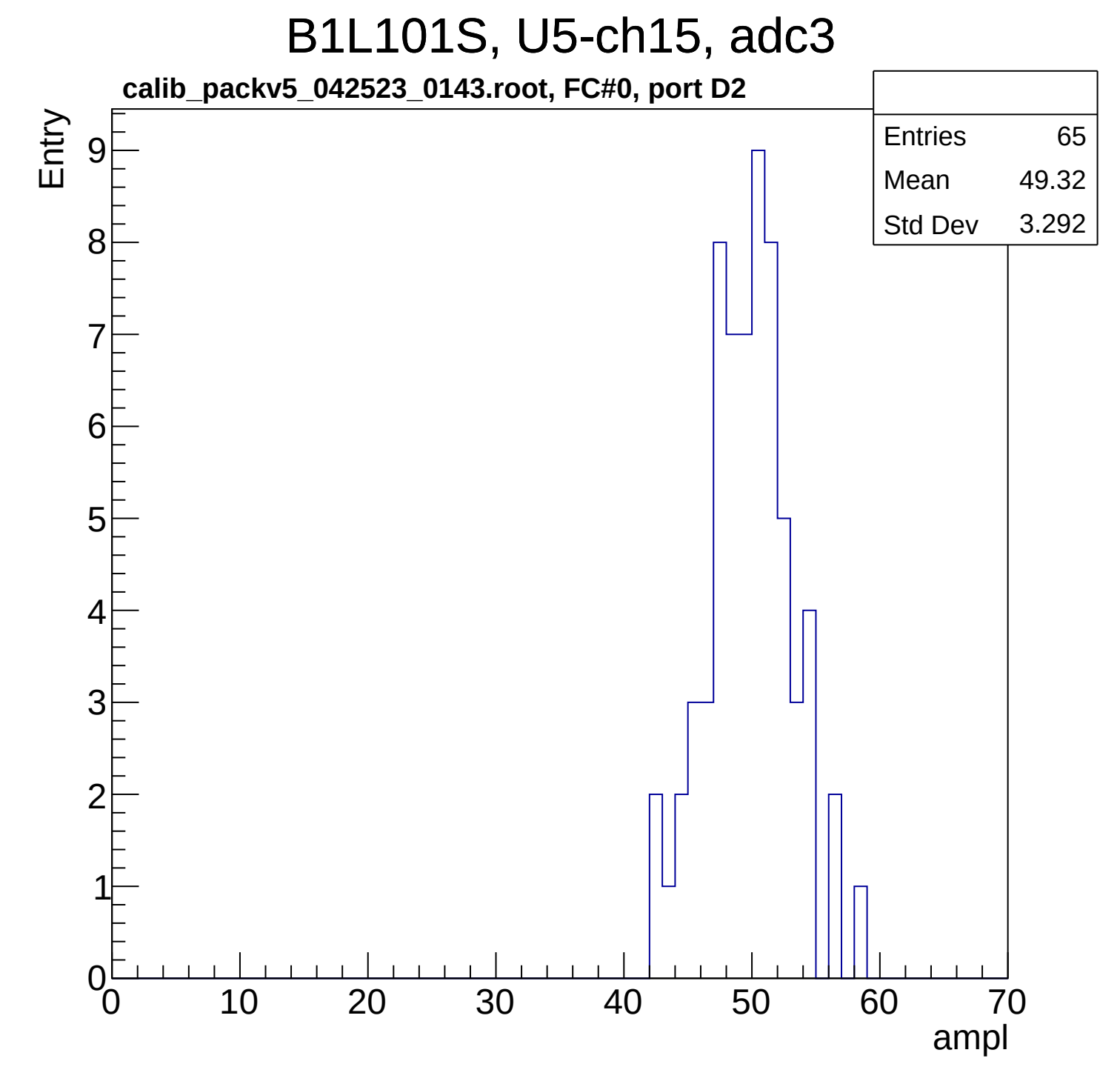
B1L101S, U5-ch15, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 49.32
Std Dev 3.292
Entry
ampl
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2
3
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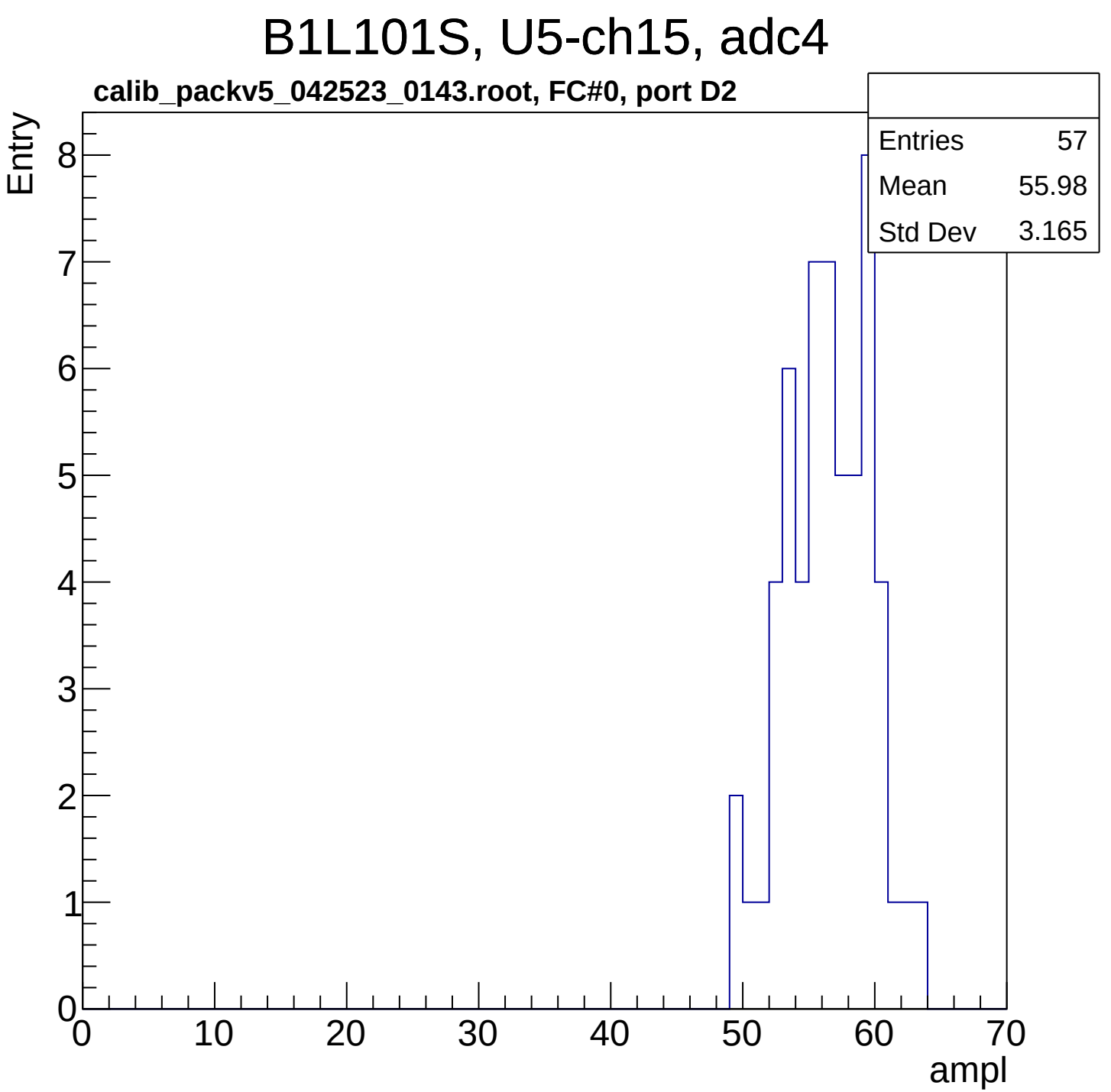
B1L101S, U5-ch15, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 55.98
Std Dev 3.165
Entry
ampl
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1
2
3
4
5
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7
8
0
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20
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40
50
60
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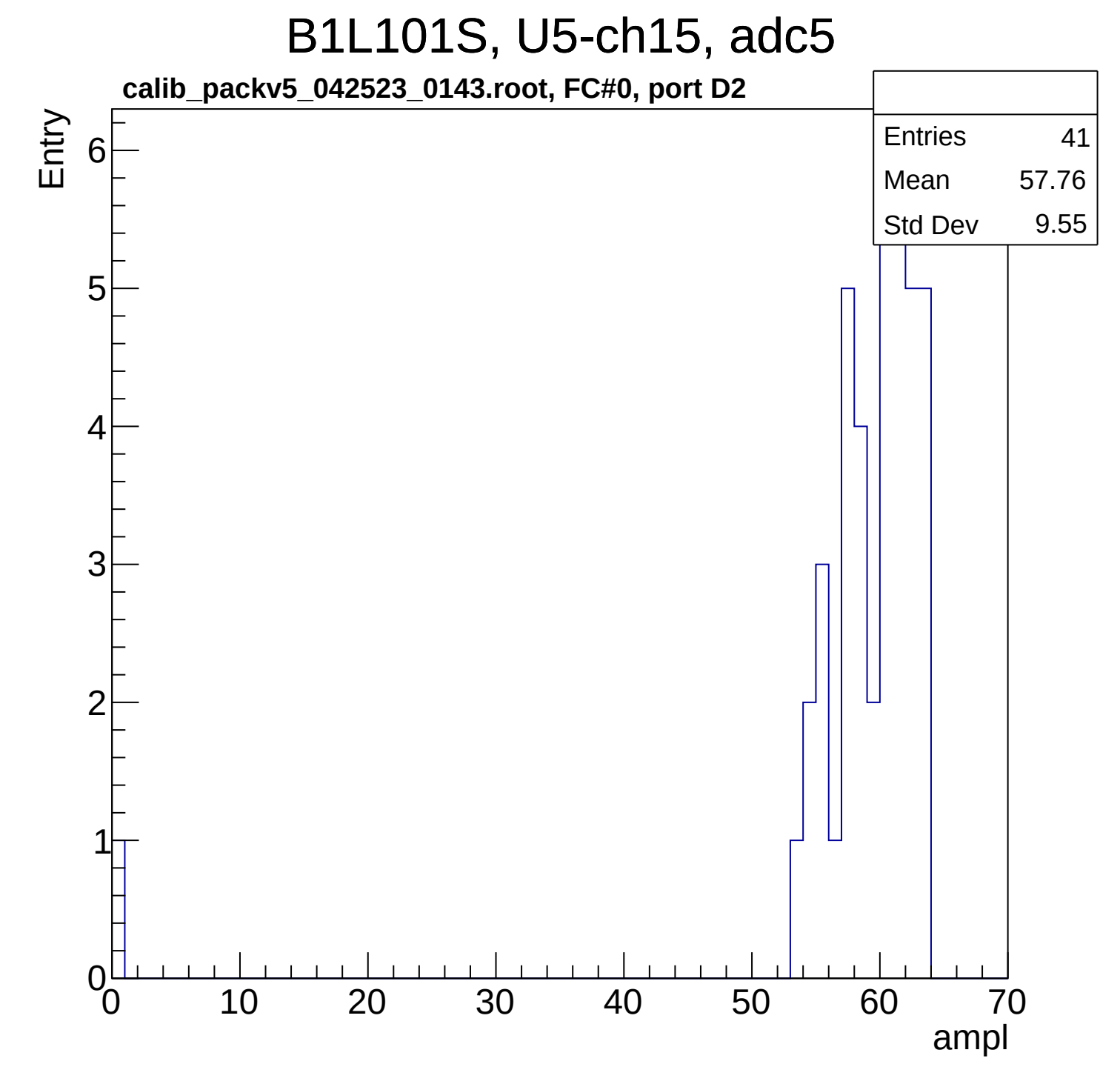
B1L101S, U5-ch15, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 41
Mean 57.76
Std Dev 9.55
Entry
0
1
2
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4
5
6
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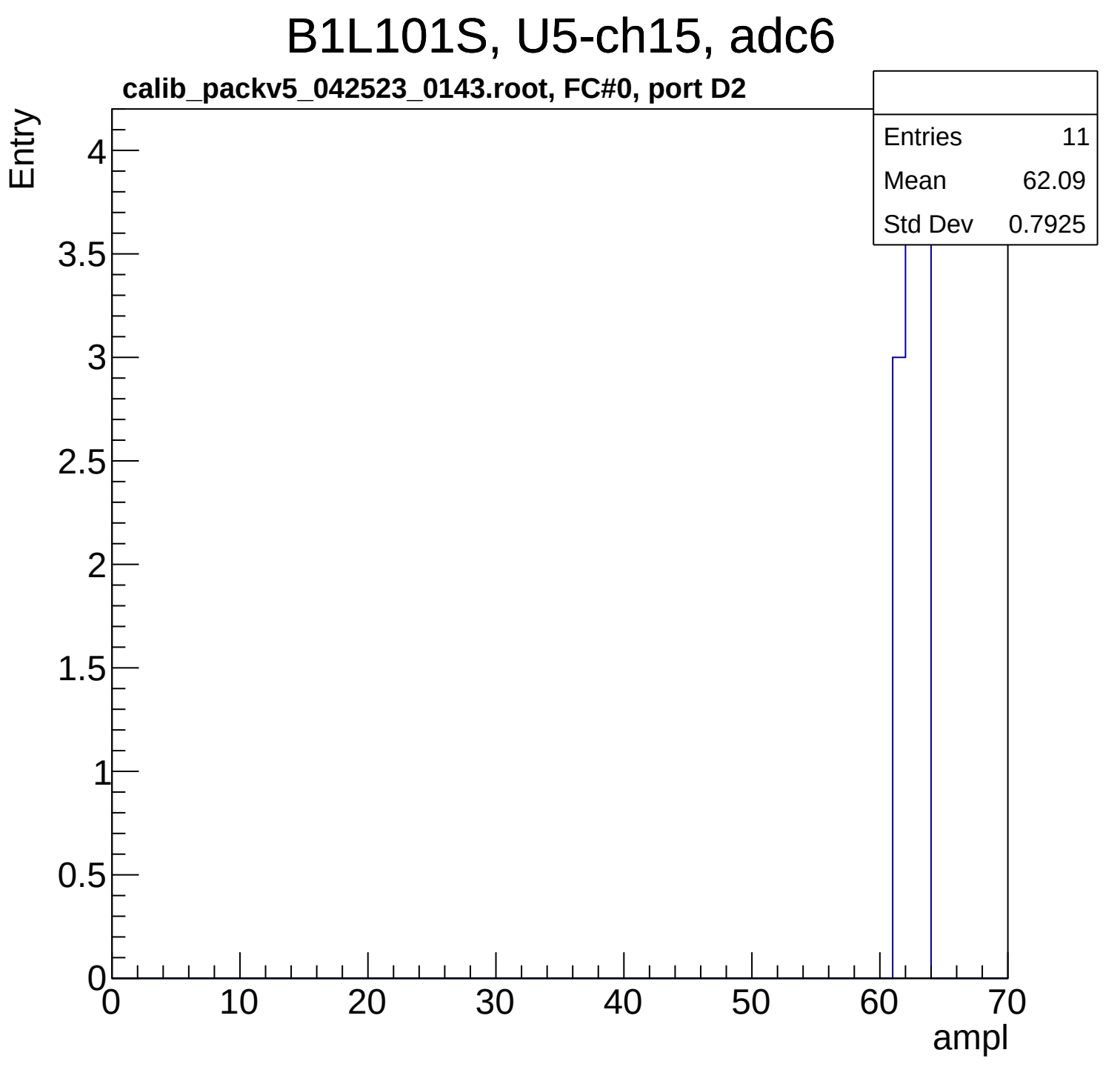
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch15, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 11
Mean 62.09
Std Dev 0.7925
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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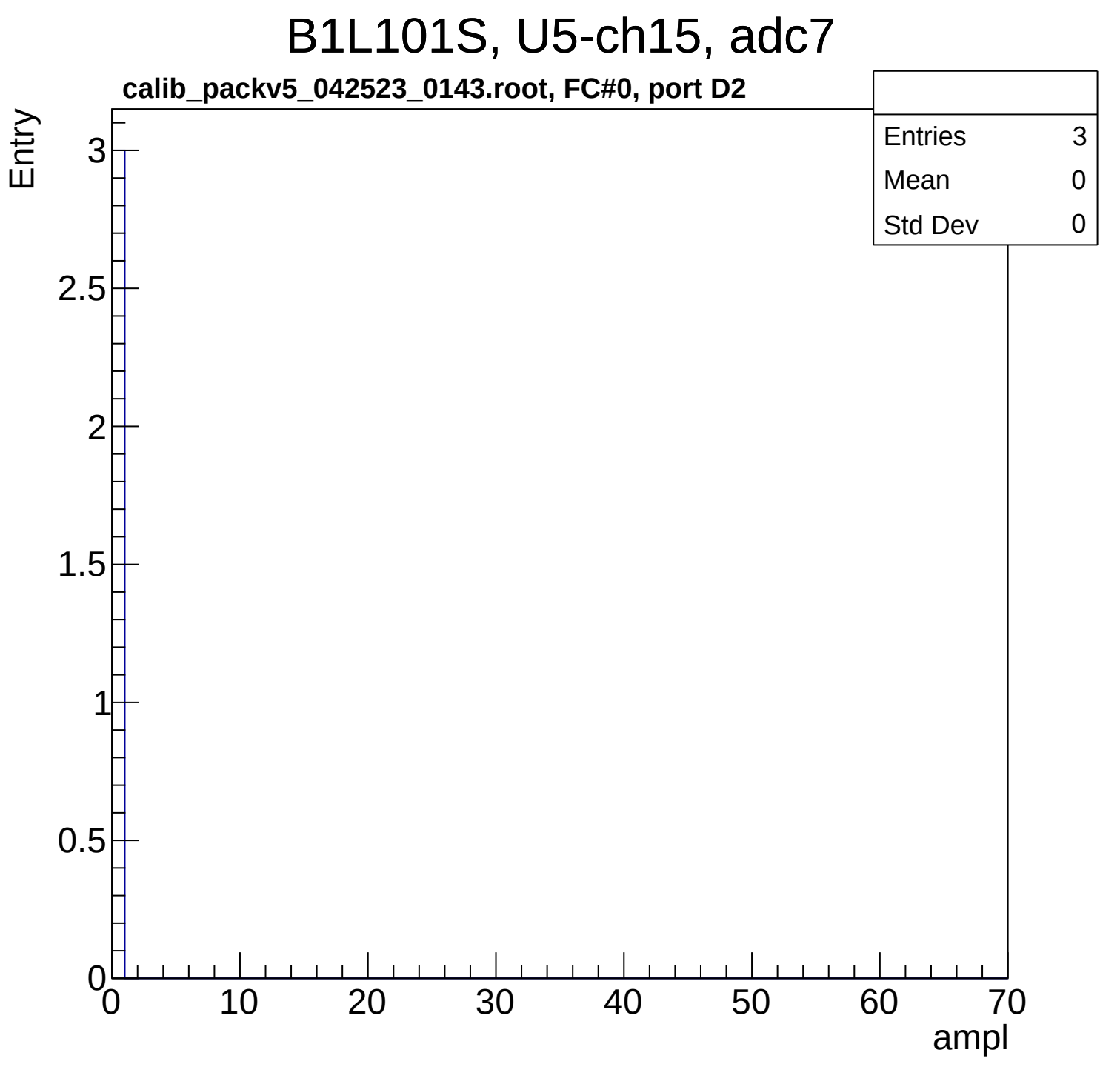
B1L101S, U5-ch15, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 0
Std Dev 0
Entry
3
2.5
2
1.5
1
0.5
0
0
10
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30
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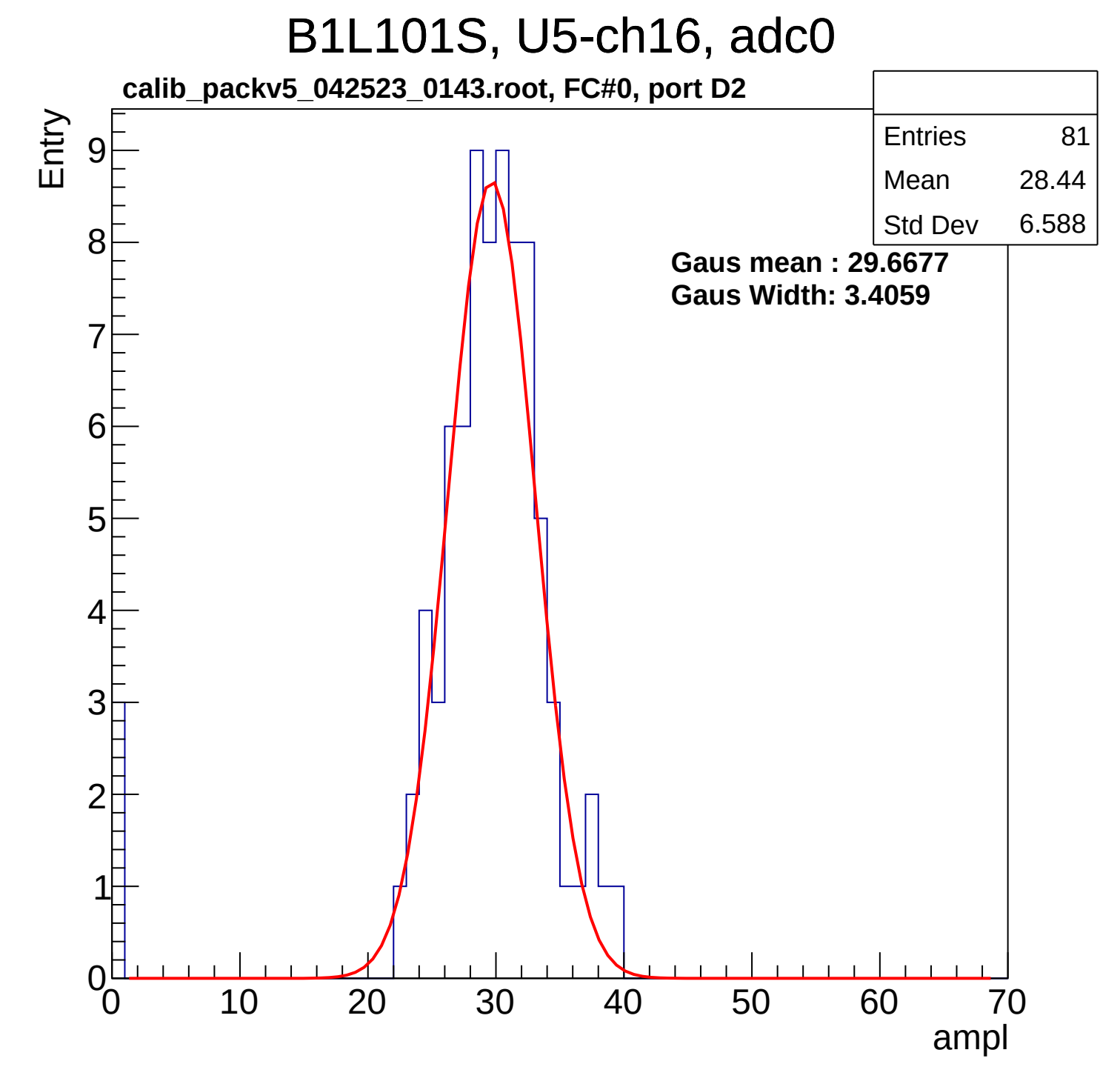
50
60
70
ampl


B1L101S, U5-ch16, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 81
Mean 28.44
Std Dev 6.588
Gaus mean : 29.6677
Gaus Width: 3.4059
Entry
ampl
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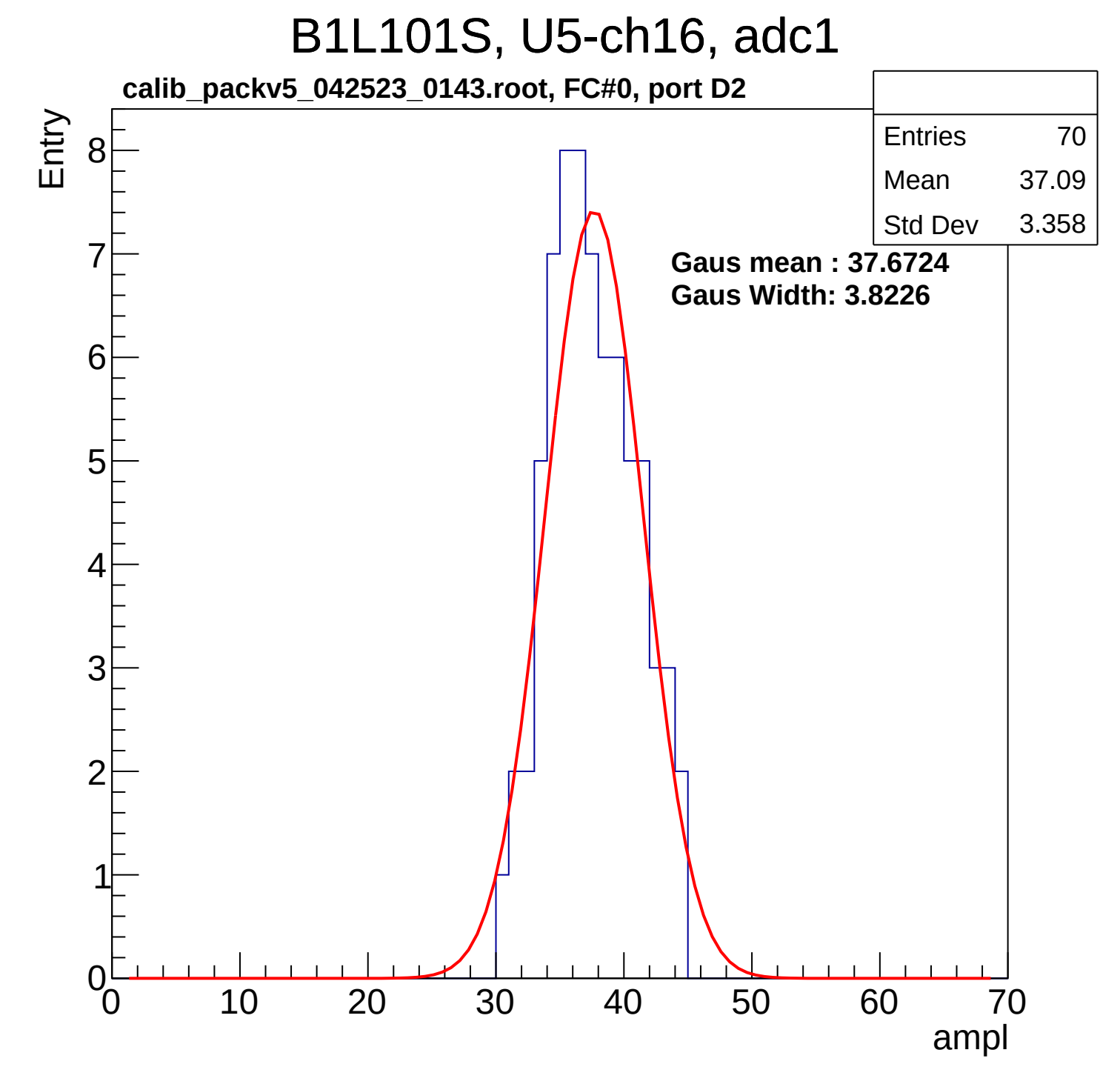
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L101S, U5-ch16, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 37.09
Std Dev 3.358
Gaus mean : 37.6724
Gaus Width: 3.8226
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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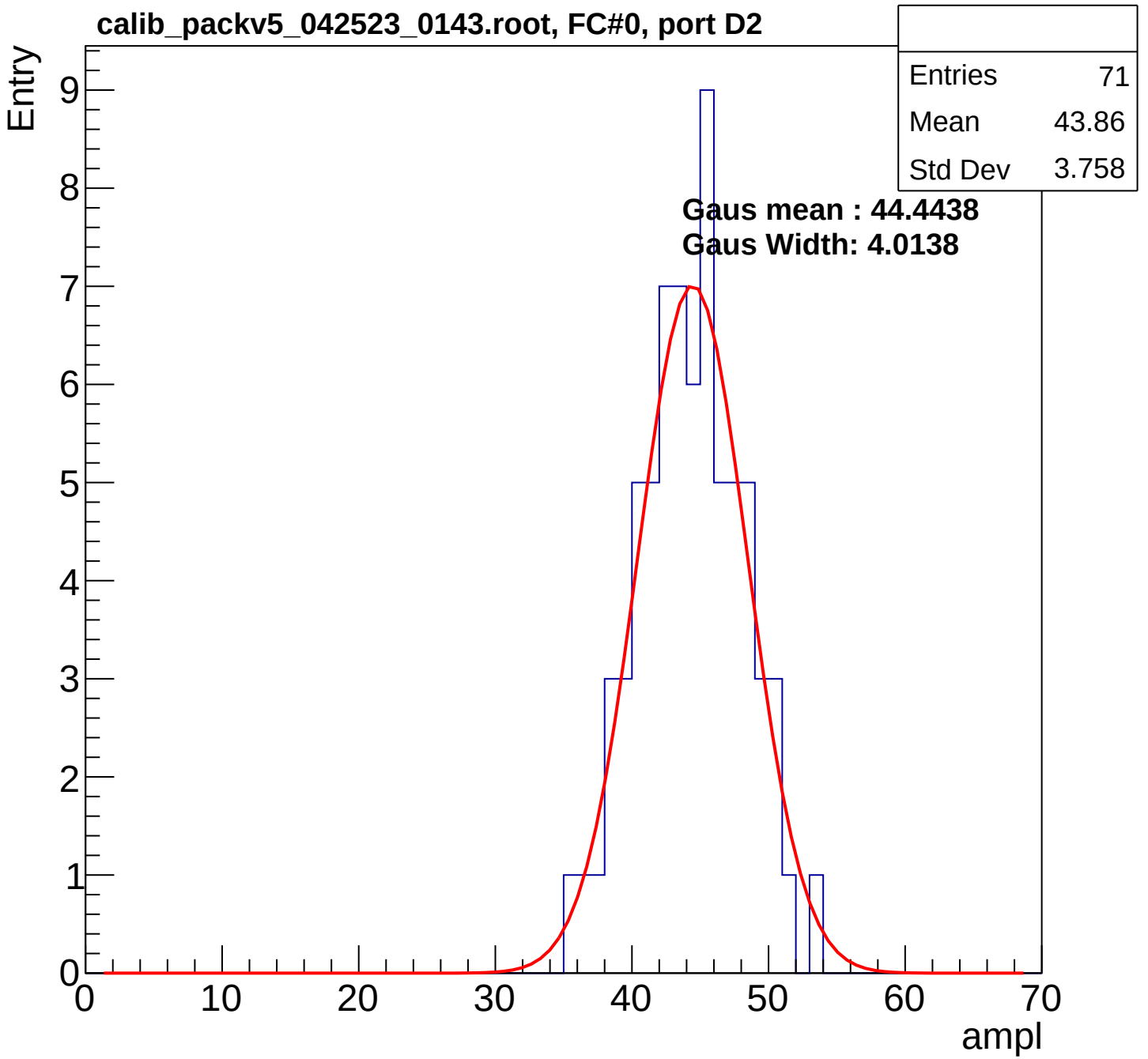
B1L101S, U5-ch16, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 43.86
Std Dev 3.758
Gaus mean : 44.4438
Gaus Width: 4.0138
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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60
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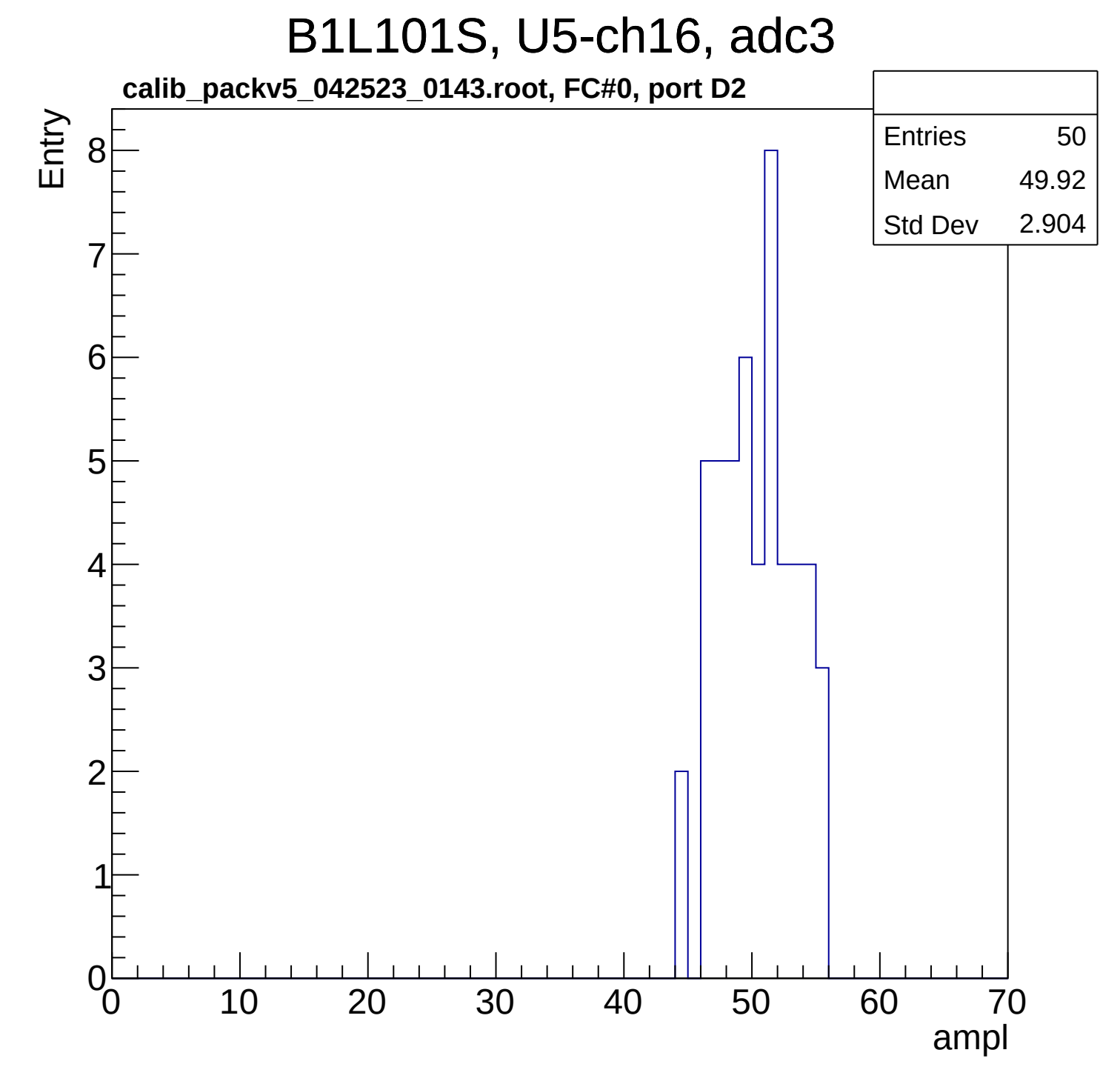
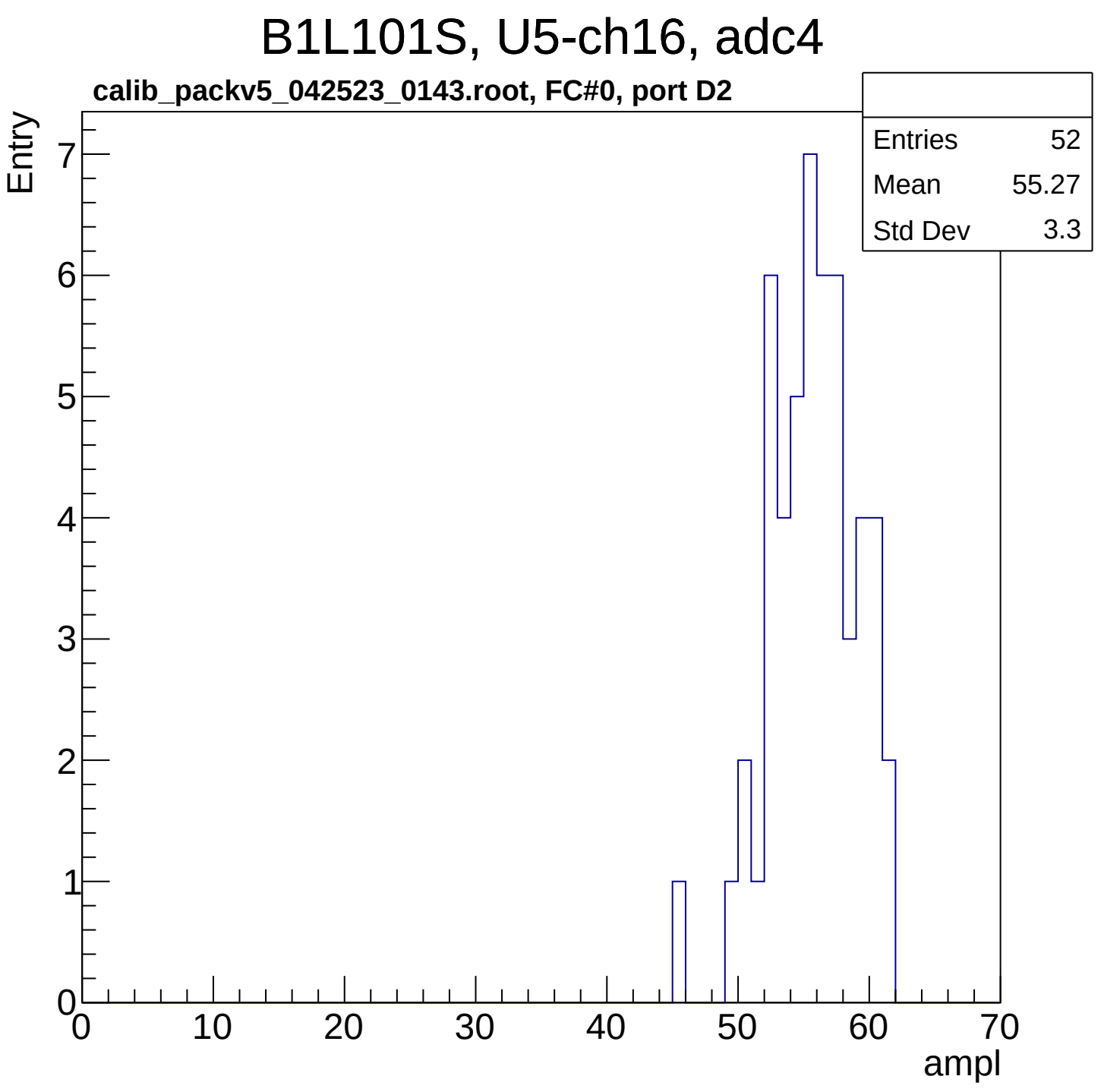
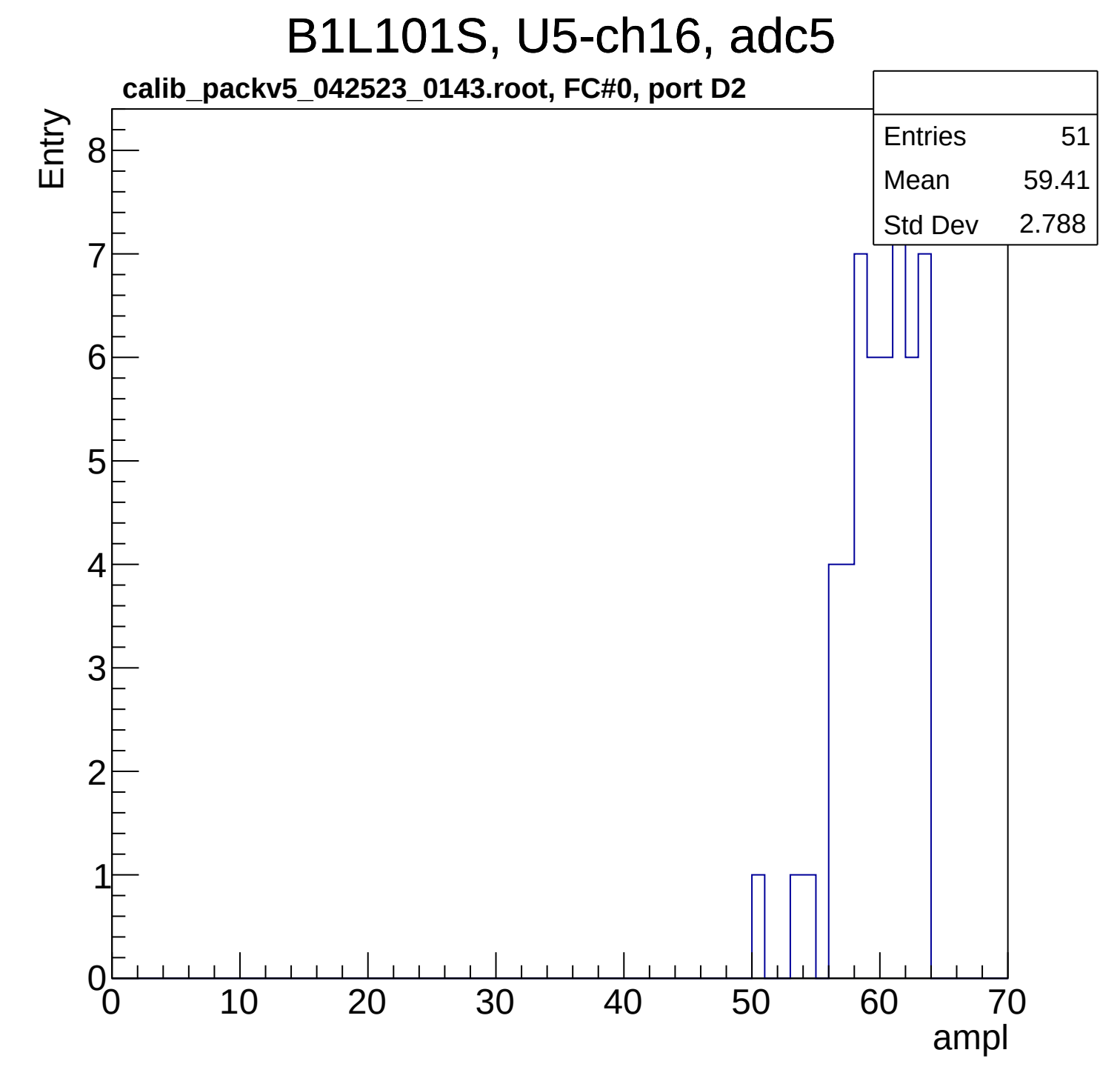

B1L101S, U5-ch16, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 49.92
Std Dev 2.904
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch16, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 55.27
Std Dev 3.3
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch16, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 59.41
Std Dev 2.788
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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20
30
40
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60
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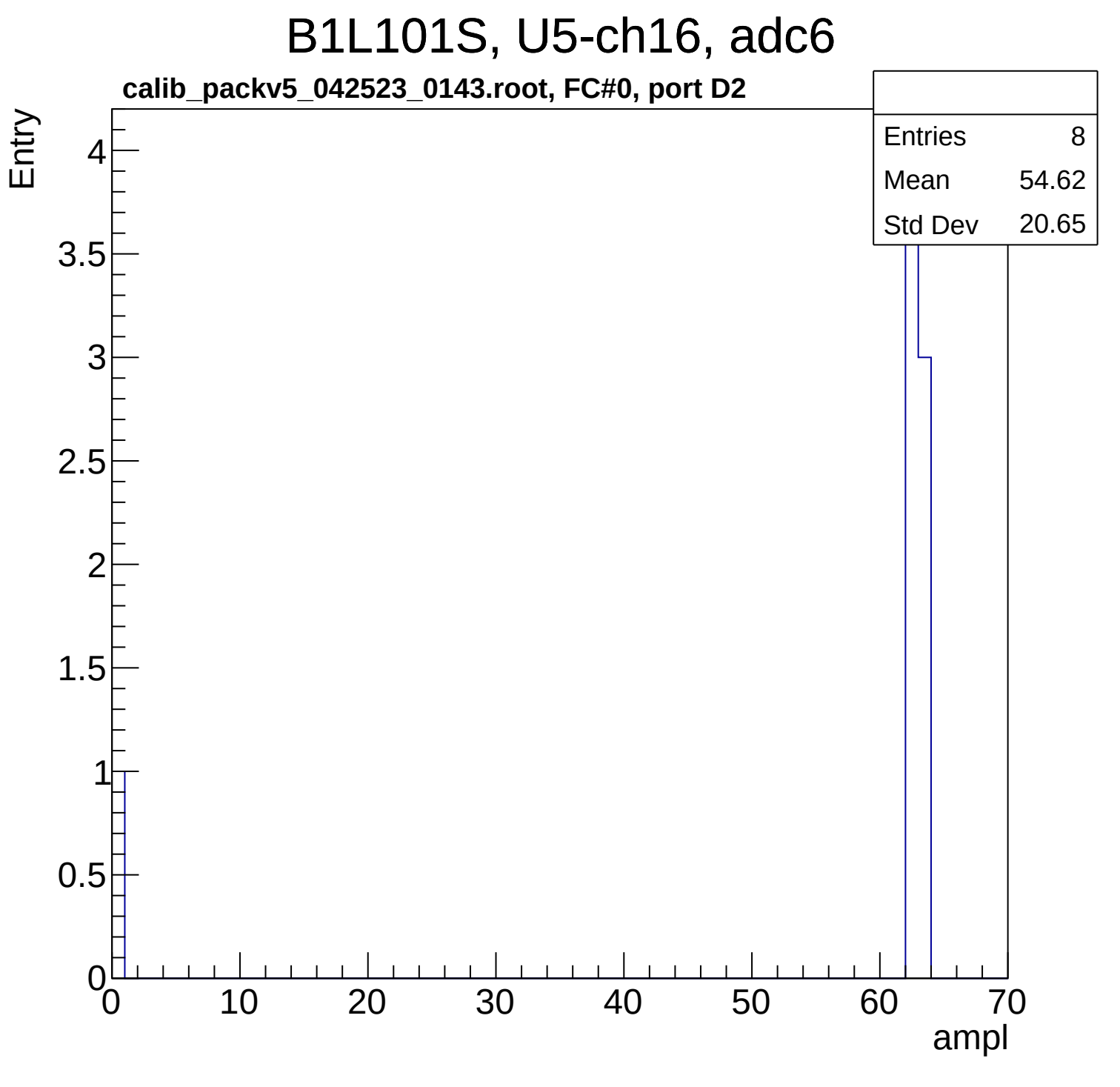
B1L101S, U5-ch16, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 54.62
Std Dev 20.65
Entry
ampl
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0.5
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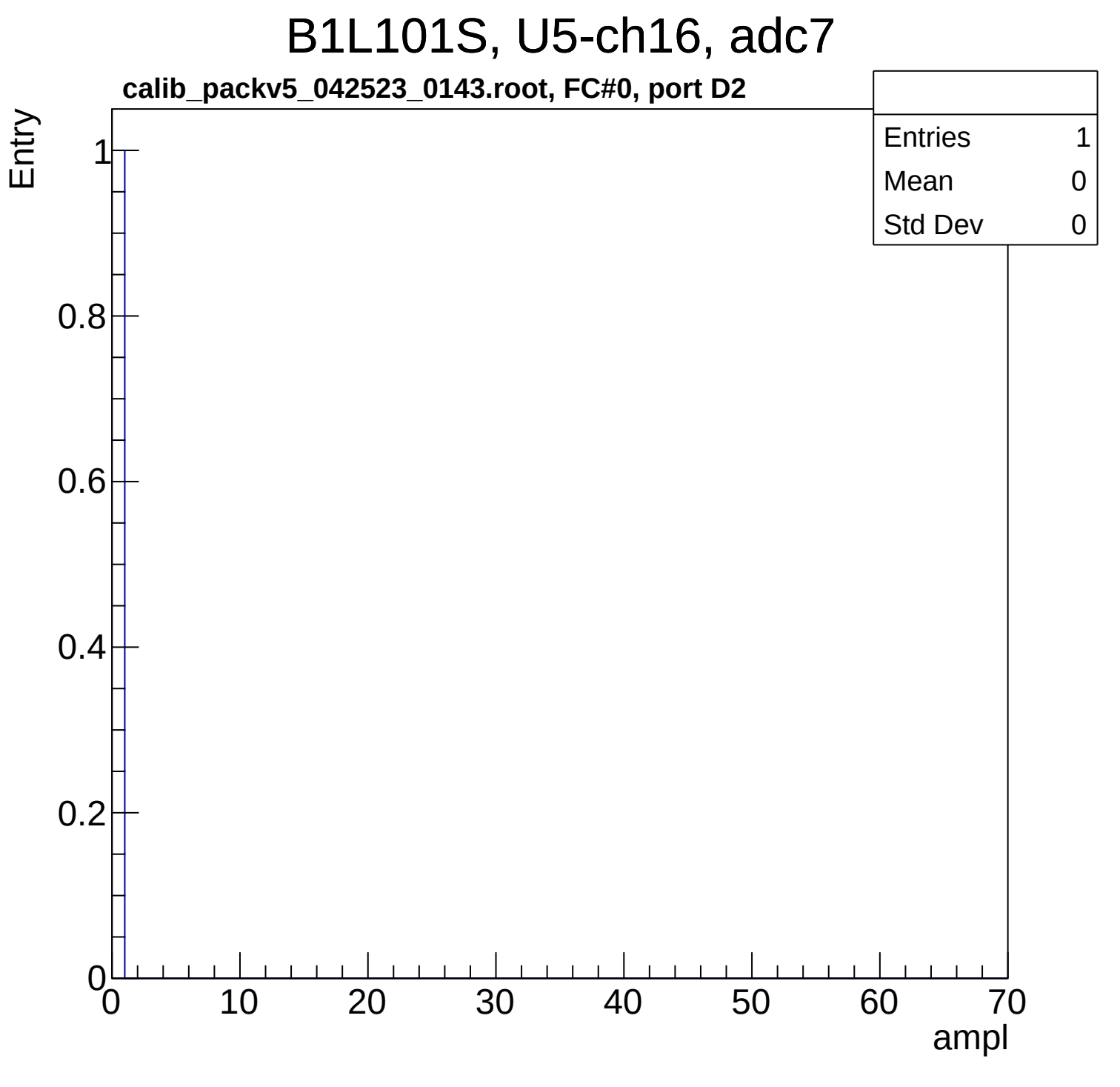
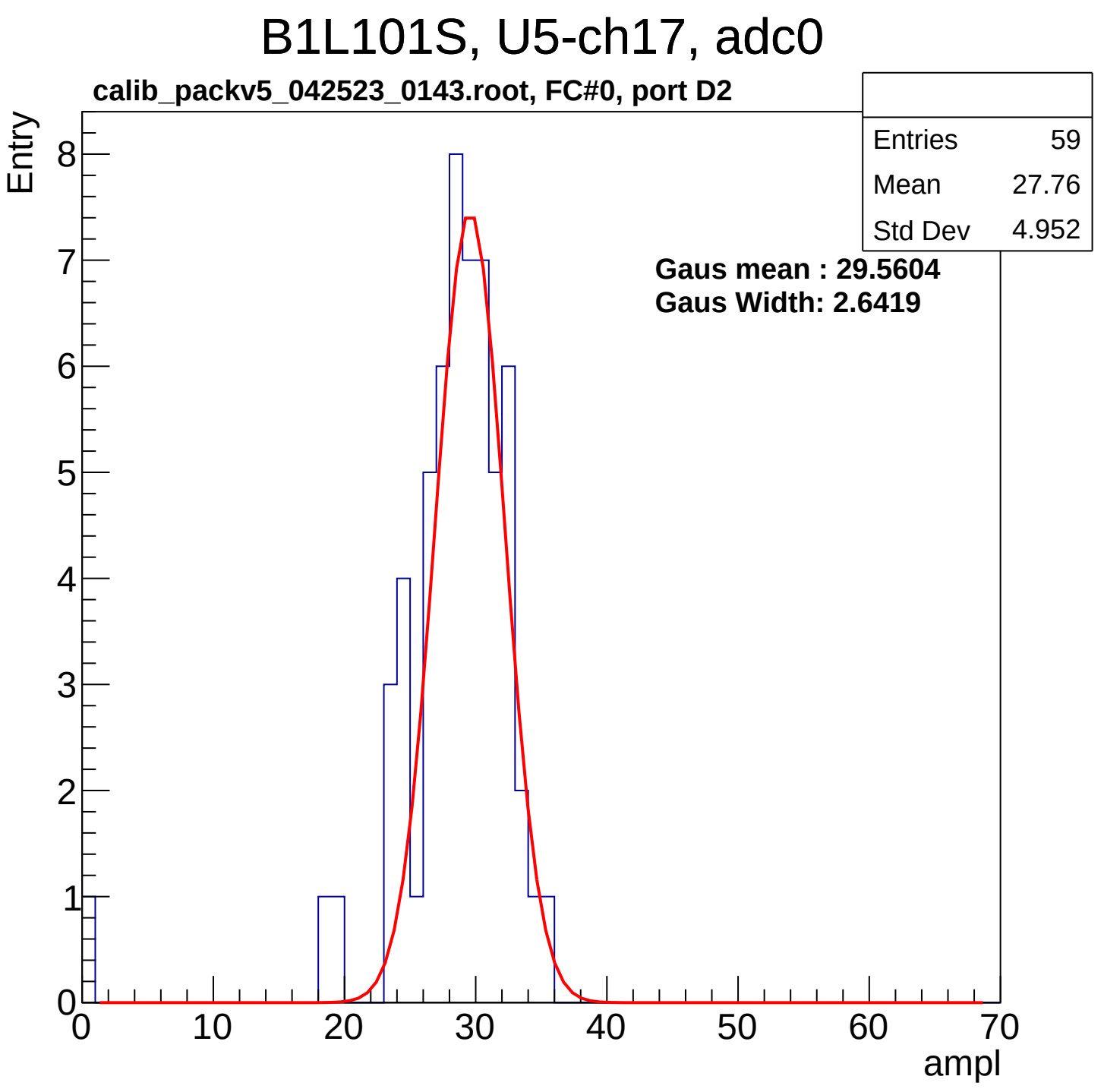
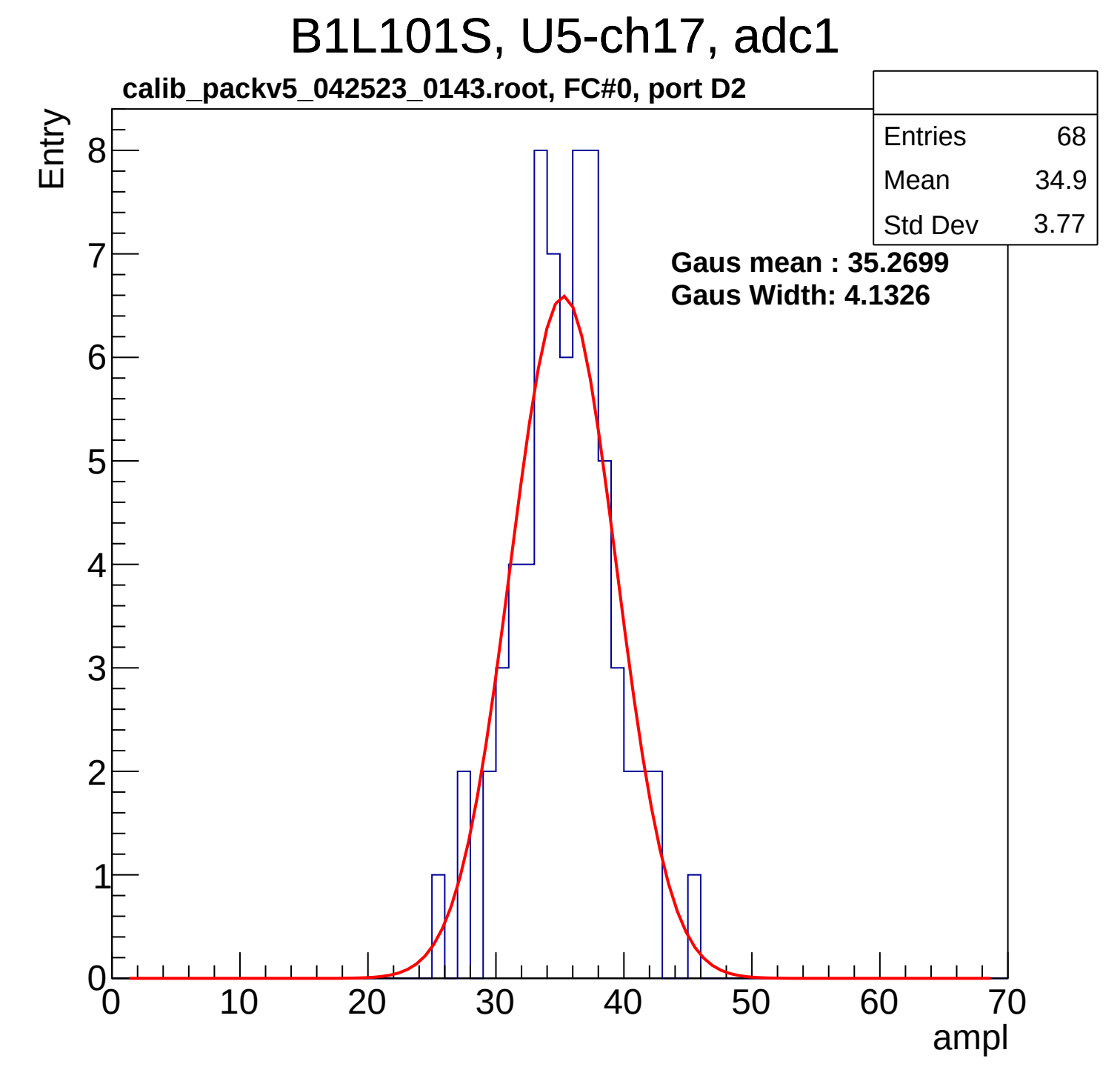
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L101S, U5-ch16, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch17, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 27.76
Std Dev 4.952
Gaus mean : 29.5604
Gaus Width: 2.6419
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch17, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 34.9
Std Dev 3.77
Gaus mean : 35.2699
Gaus Width: 4.1326
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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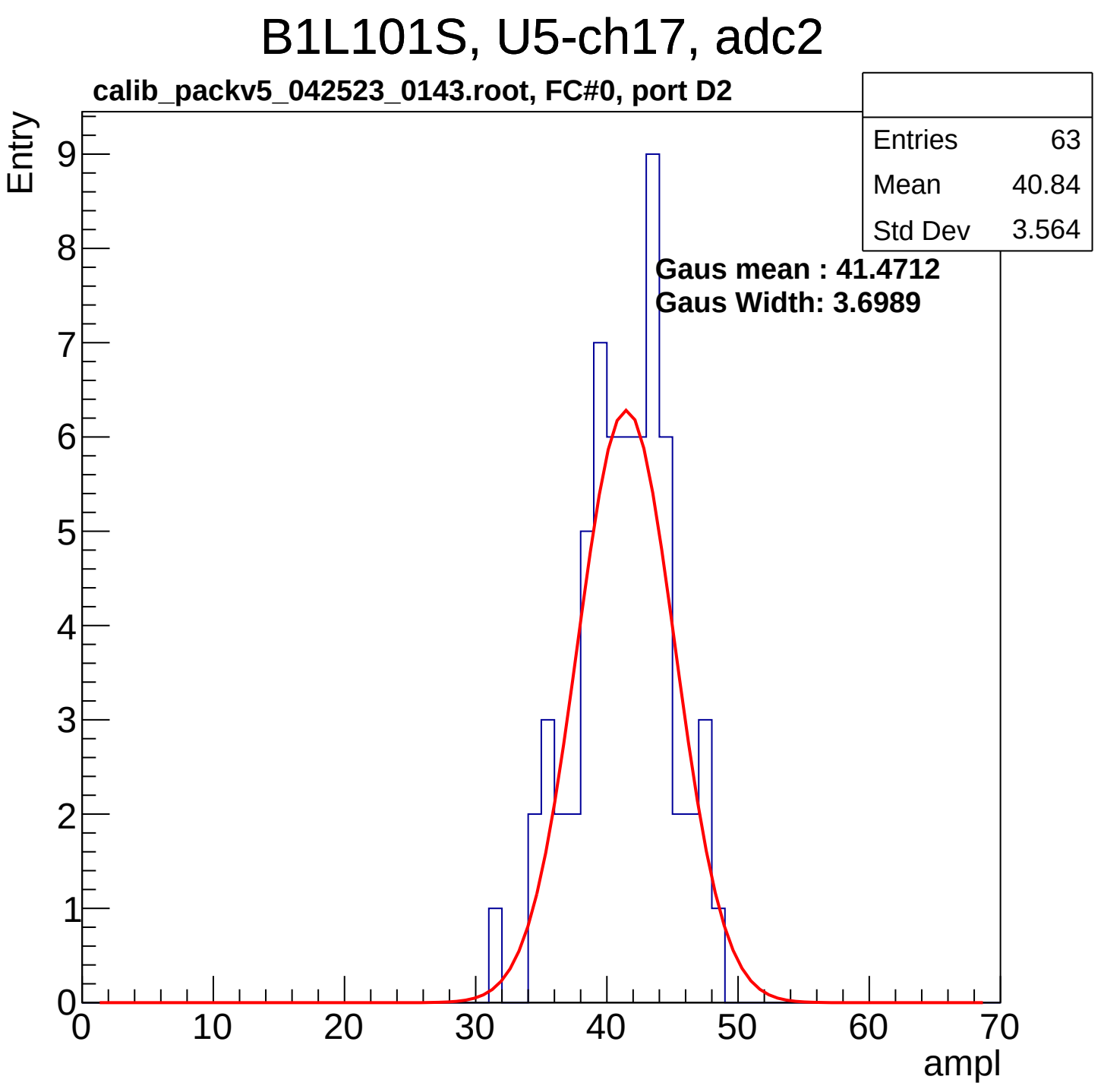
B1L101S, U5-ch17, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 40.84
Std Dev 3.564
Gaus mean : 41.4712
Gaus Width: 3.6989
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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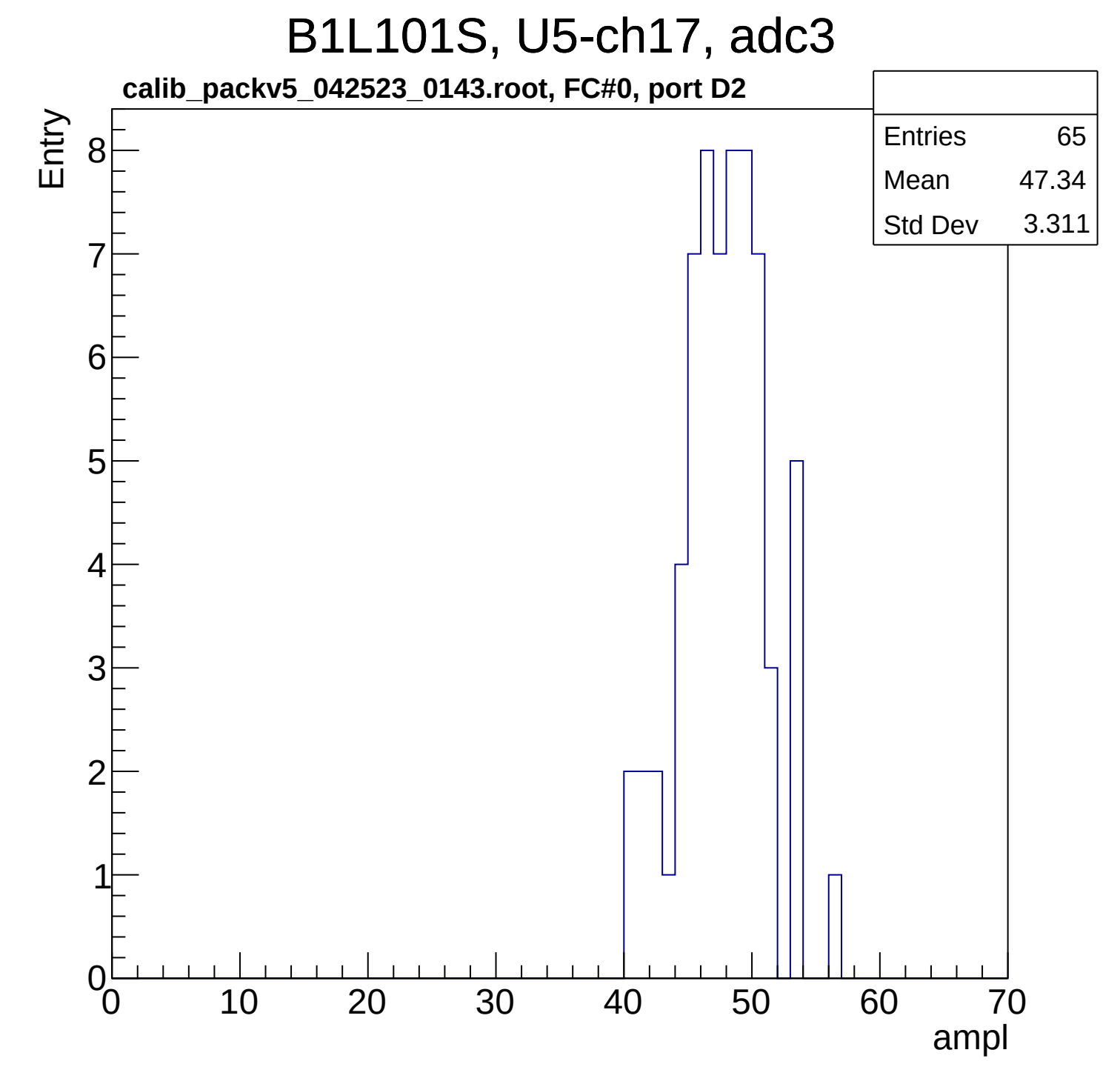
B1L101S, U5-ch17, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 47.34
Std Dev 3.311
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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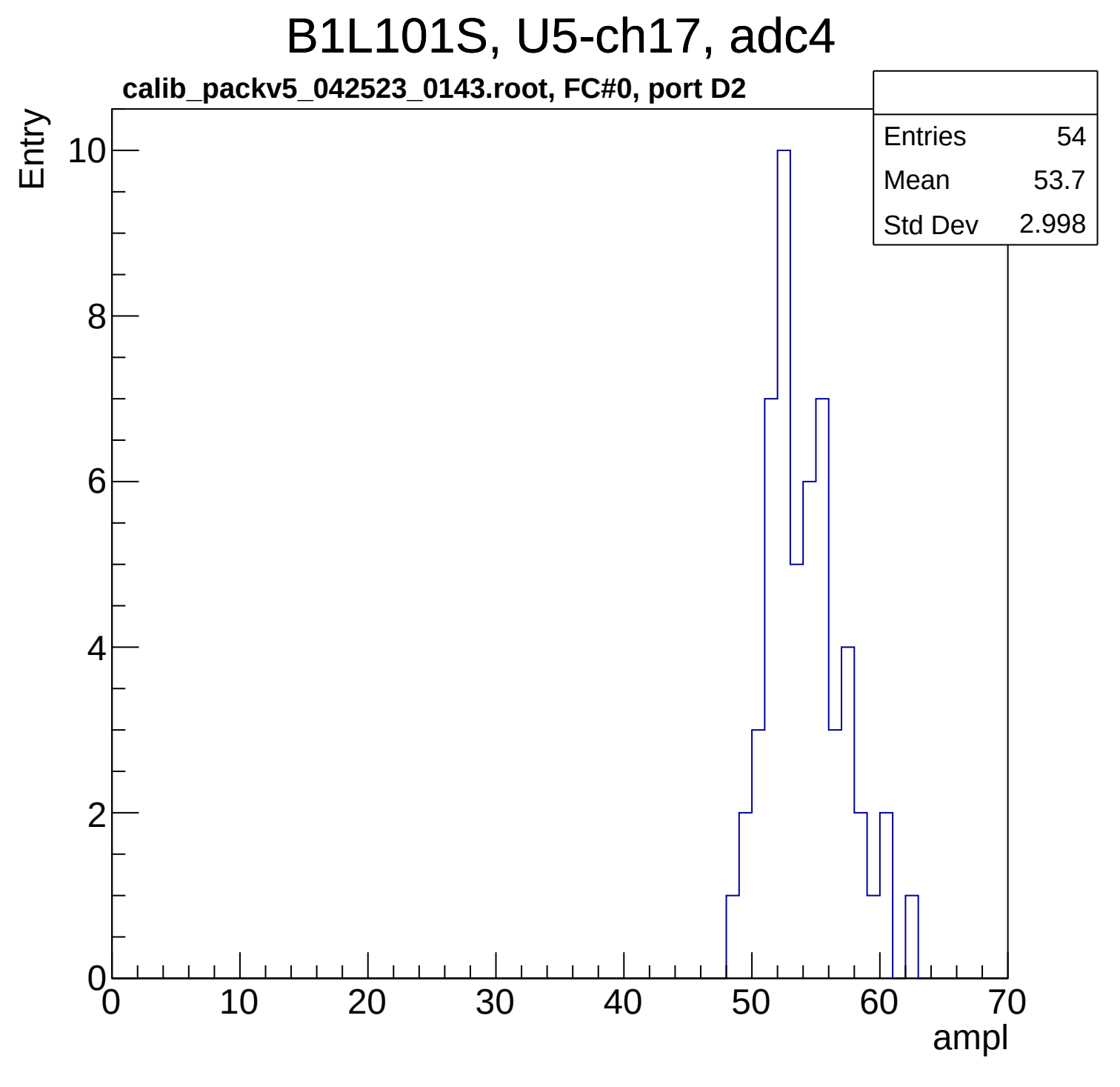
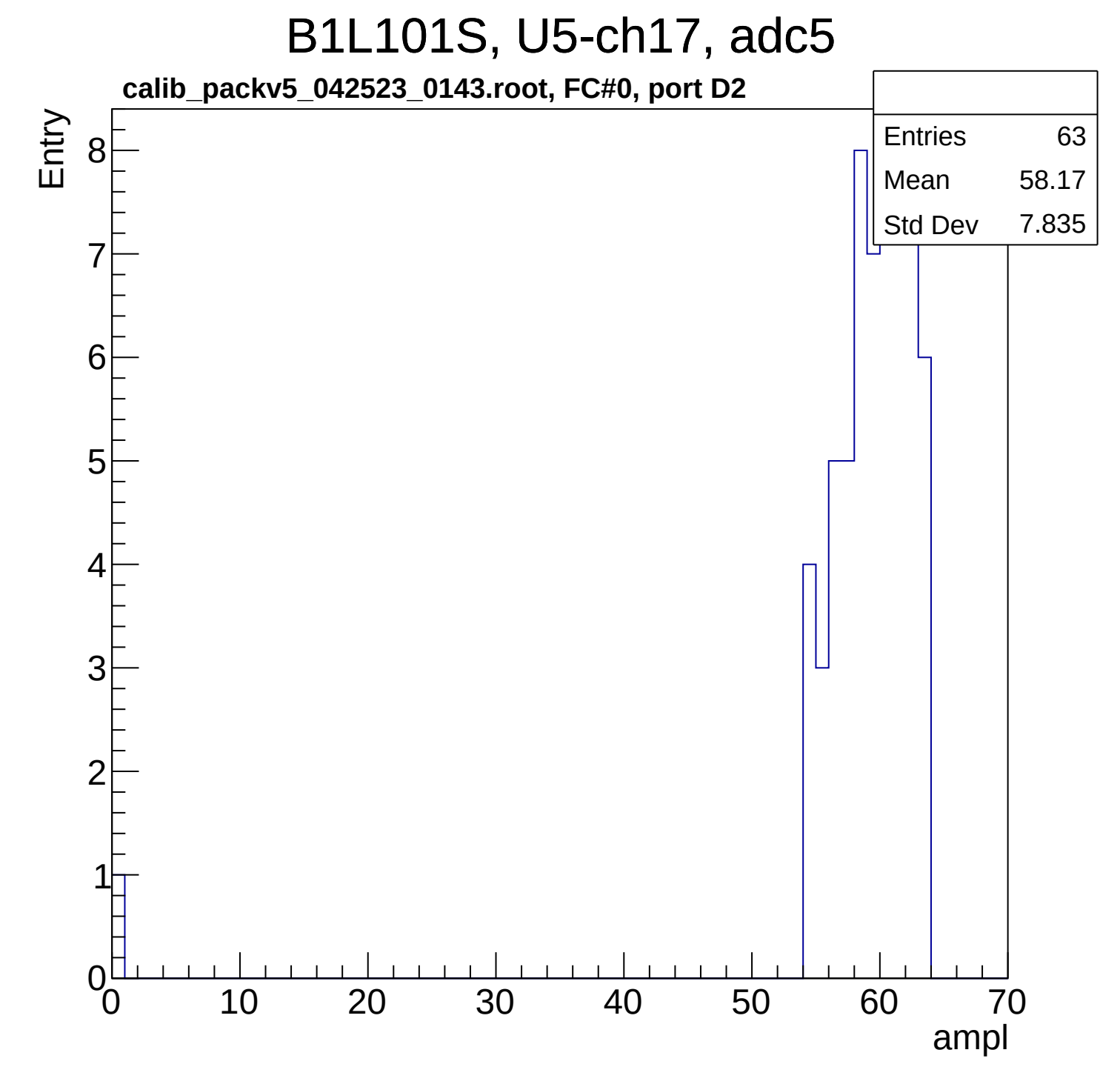
40
50
60
70


B1L101S, U5-ch17, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 53.7
Std Dev 2.998
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch17, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 58.17
Std Dev 7.835
Entry
ampl
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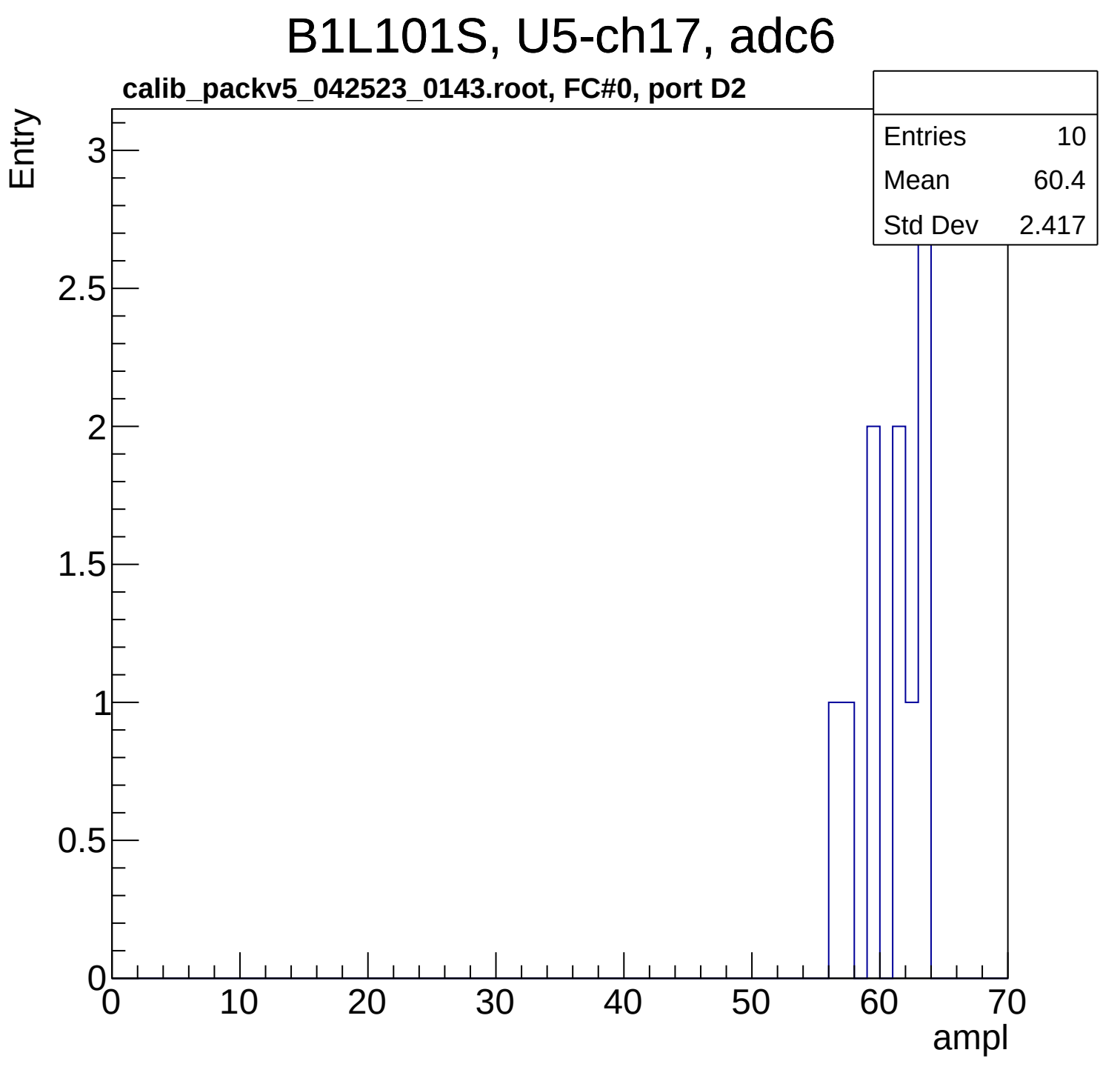
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch17, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 60.4
Std Dev 2.417
Entry
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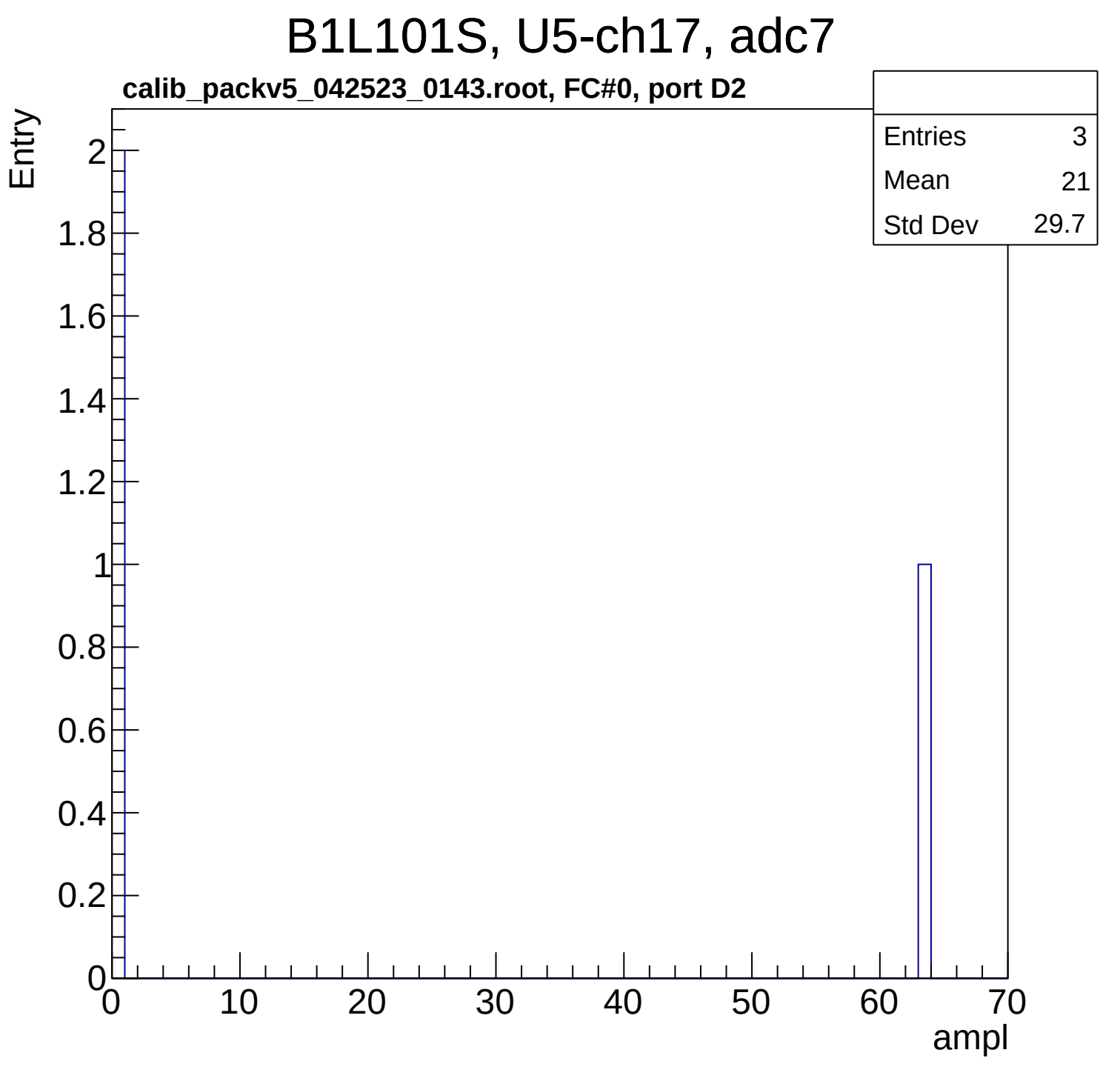
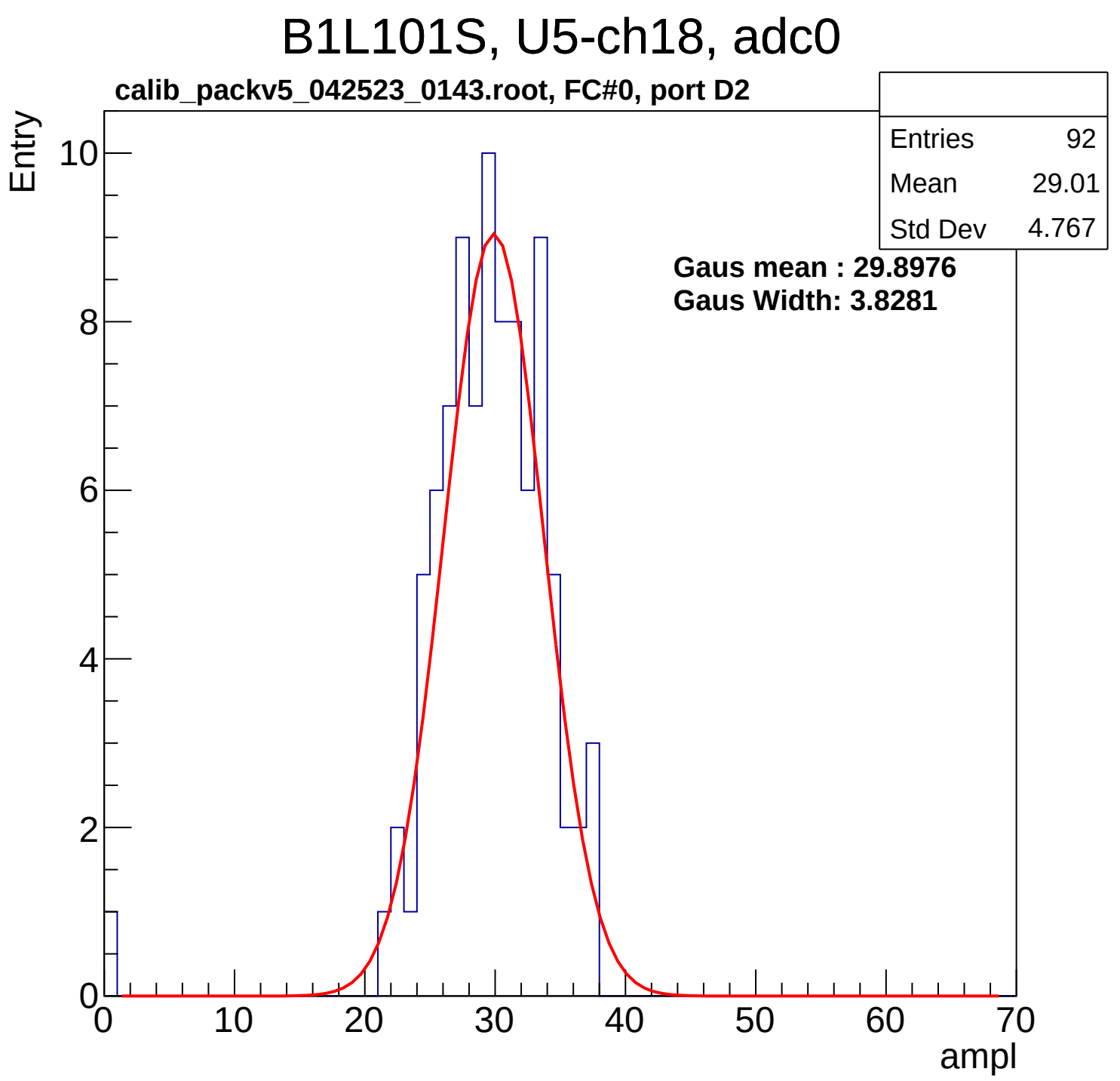
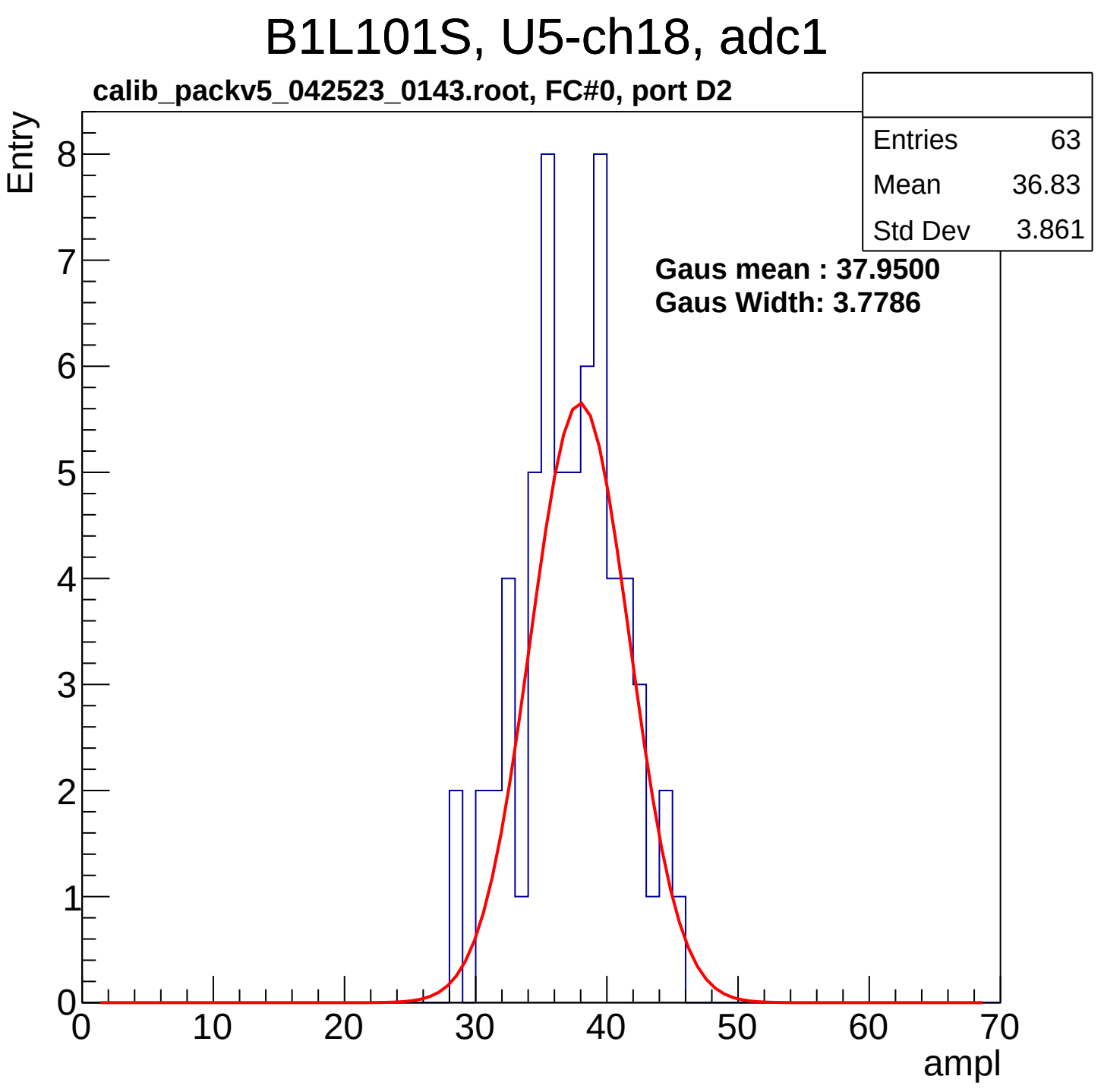
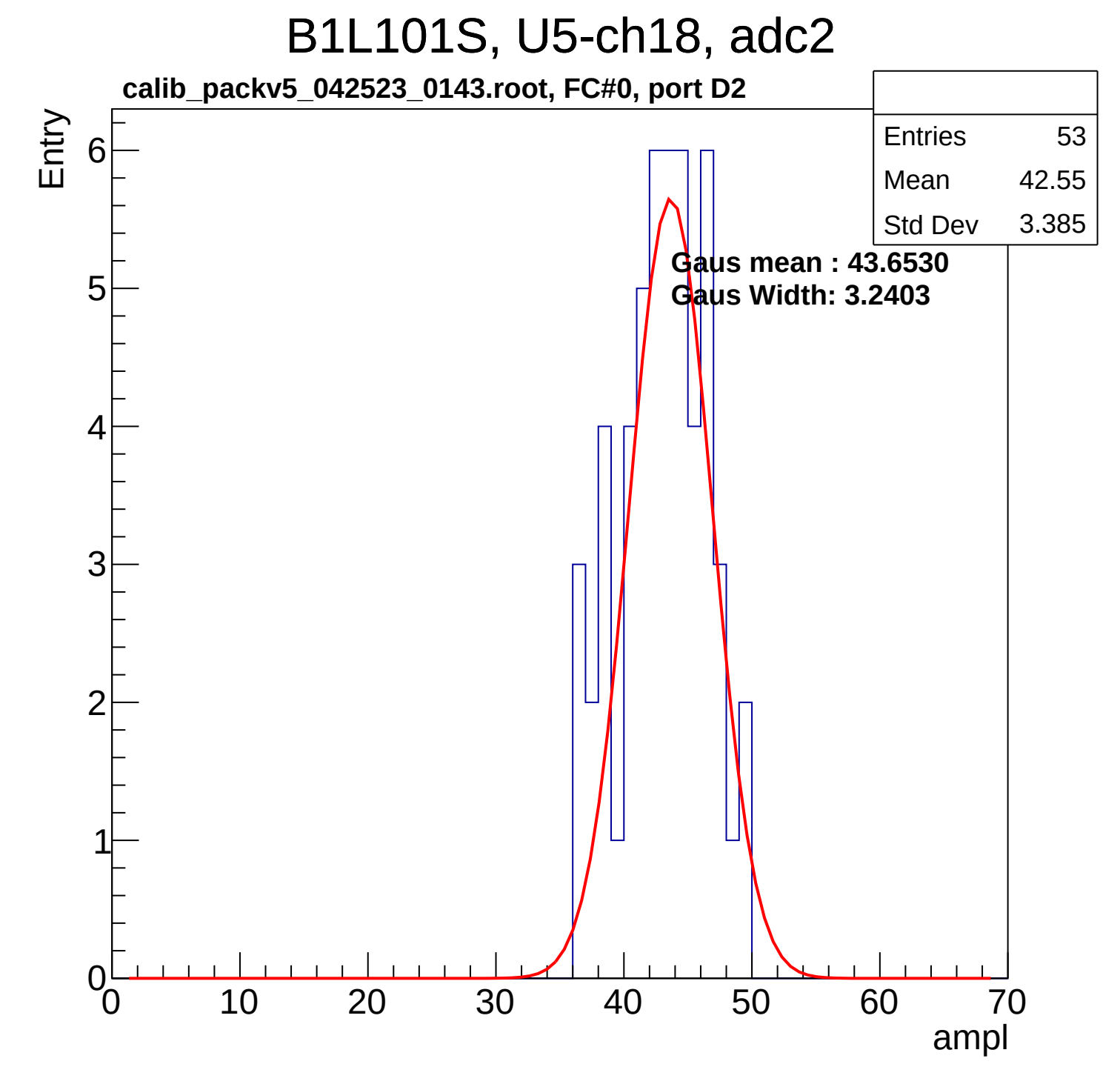
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch17, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 21
Std Dev 29.7
Entry
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch18, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 92
Mean 29.01
Std Dev 4.767
Gaus mean : 29.8976
Gaus Width: 3.8281
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch18, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 36.83
Std Dev 3.861
Gaus mean : 37.9500
Gaus Width: 3.7786
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch18, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 42.55
Std Dev 3.385
Gaus mean : 43.6530
Gaus Width: 3.2403
Entry
ampl
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1
2
3
4
5
6
0
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20
30
40
50
60
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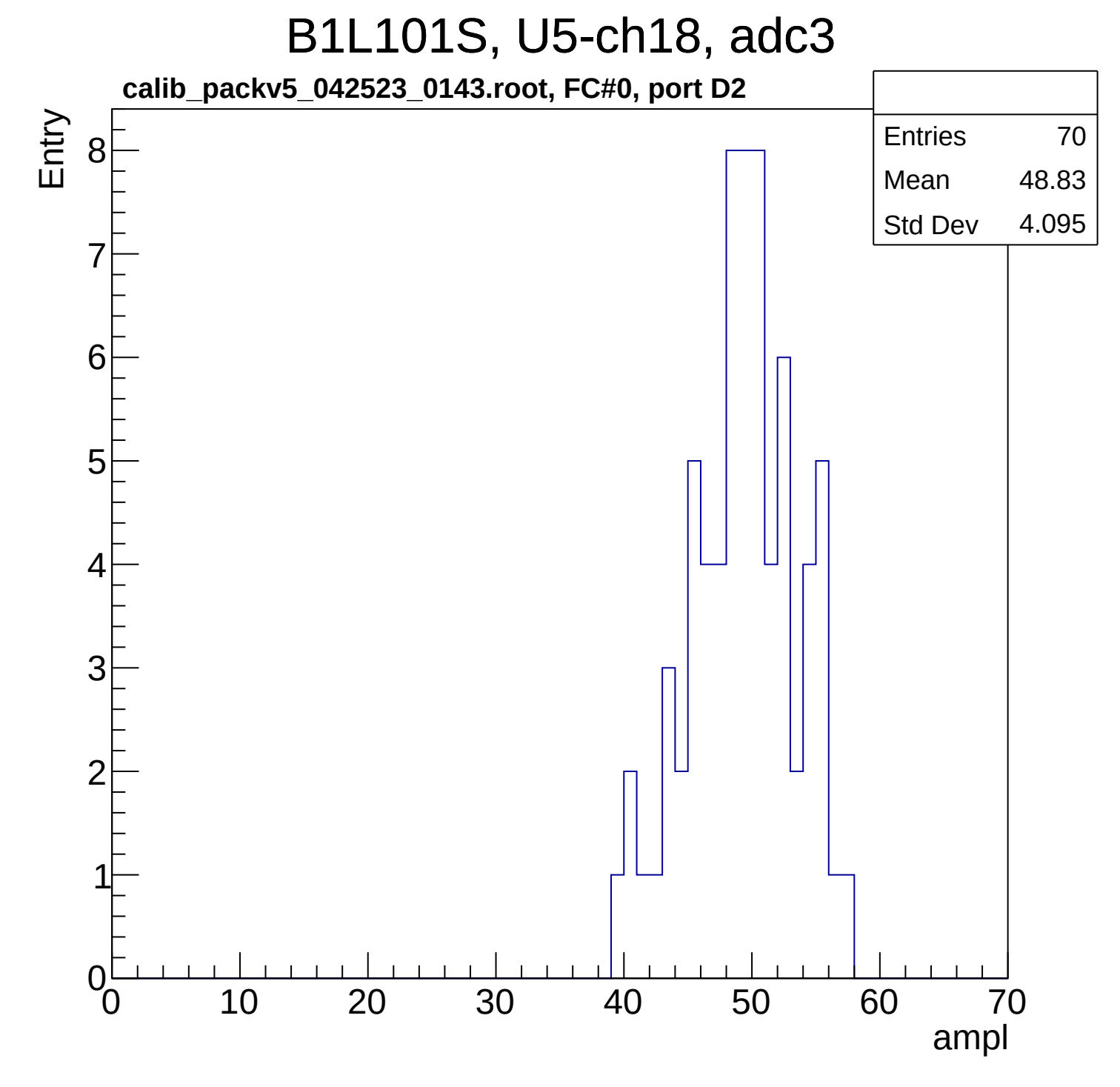
B1L101S, U5-ch18, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 48.83
Std Dev 4.095
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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60
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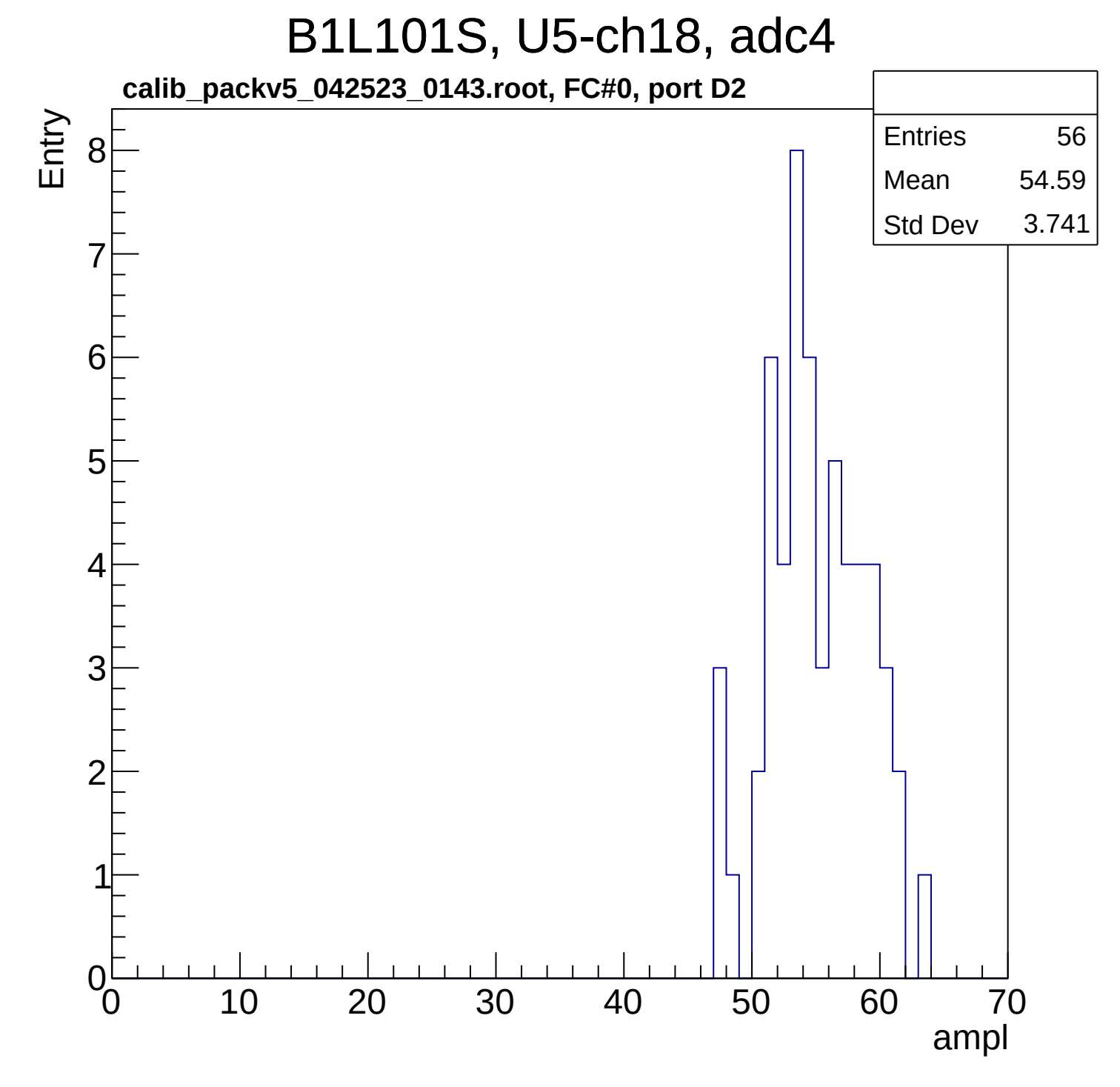
B1L101S, U5-ch18, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 54.59
Std Dev 3.741
Entry
ampl
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3
4
5
6
7
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60
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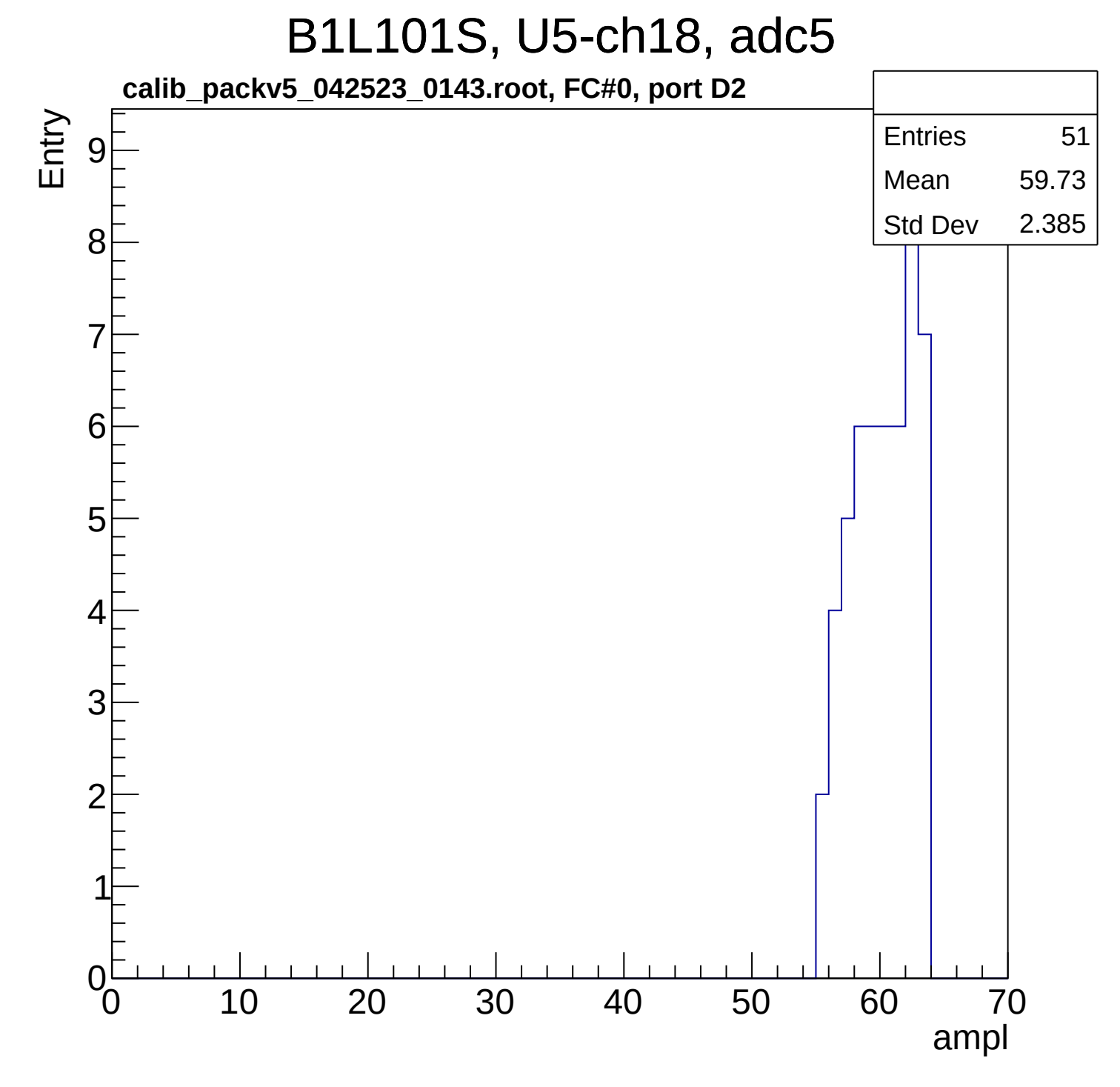
B1L101S, U5-ch18, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 59.73
Std Dev 2.385
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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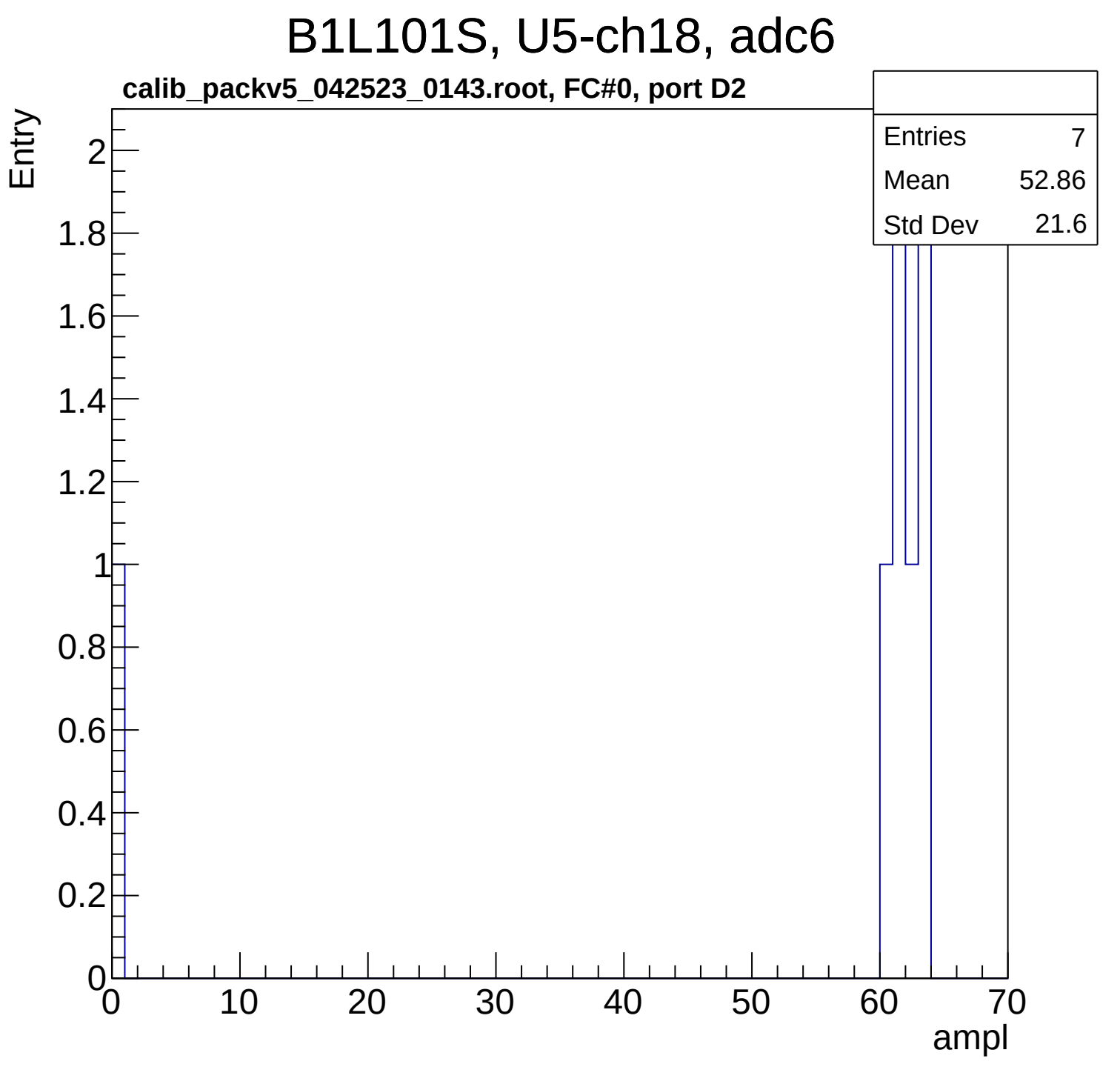
B1L101S, U5-ch18, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 52.86
Std Dev 21.6
Entry
ampl
0
0.2
0.4
0.6
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1.2
1.4
1.6
1.8
2
0
10
20
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40
50
60
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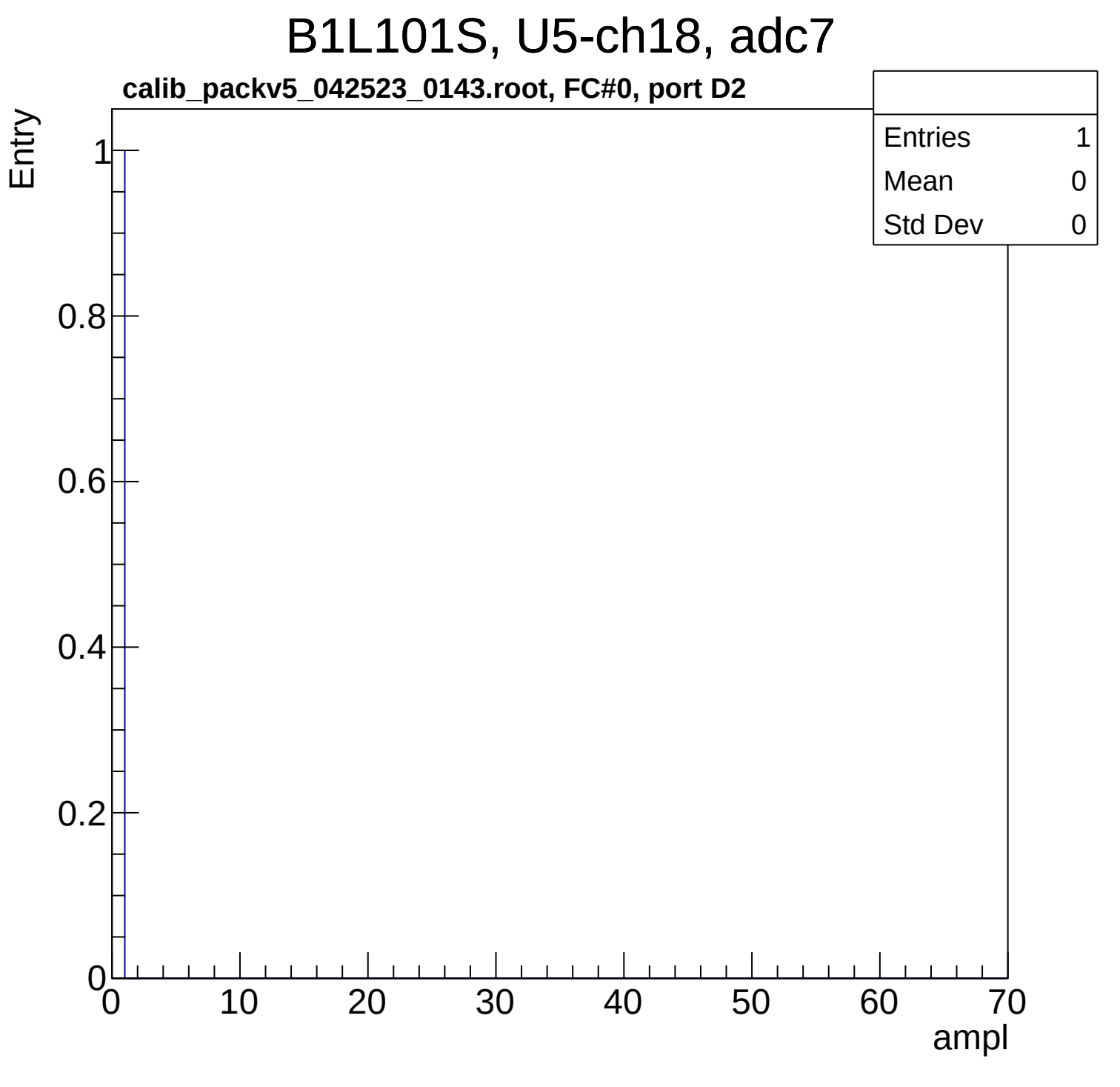
B1L101S, U5-ch18, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
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0.6
0.4
0.2
0
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10
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30
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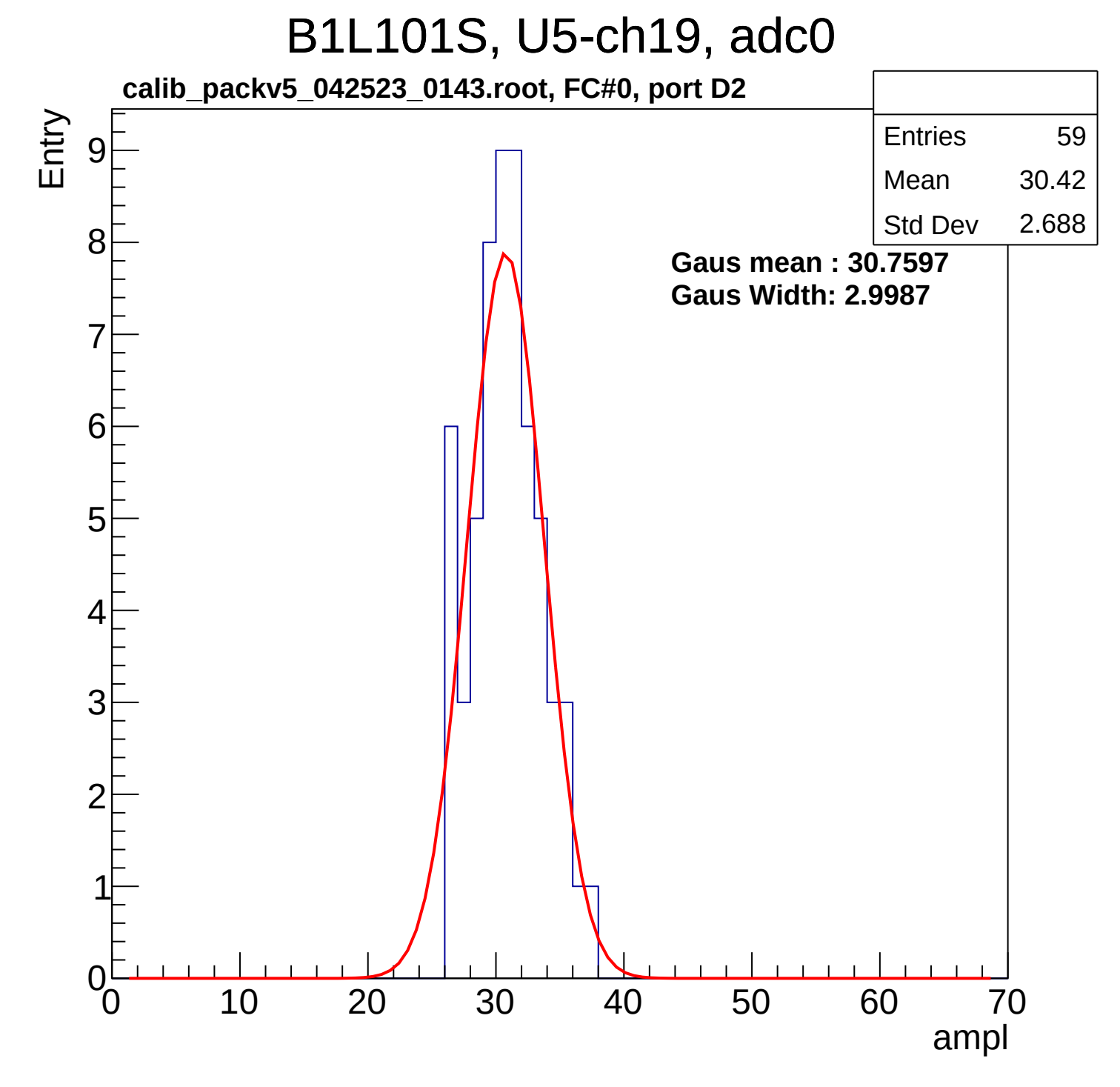
50
60
70
ampl


B1L101S, U5-ch19, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 30.42
Std Dev 2.688
Gaus mean : 30.7597
Gaus Width: 2.9987
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
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60
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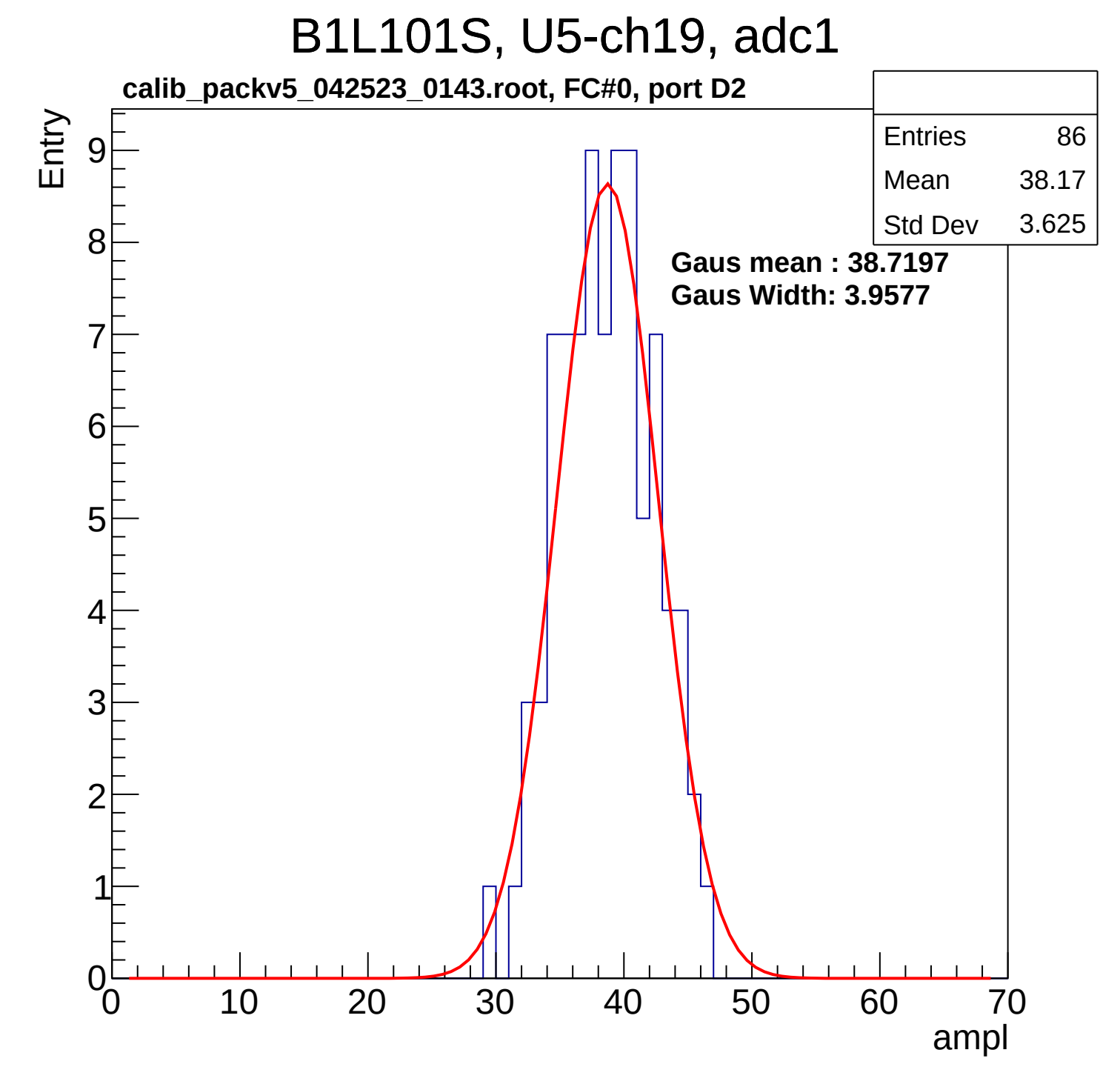
B1L101S, U5-ch19, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 86
Mean 38.17
Std Dev 3.625
Gaus mean : 38.7197
Gaus Width: 3.9577
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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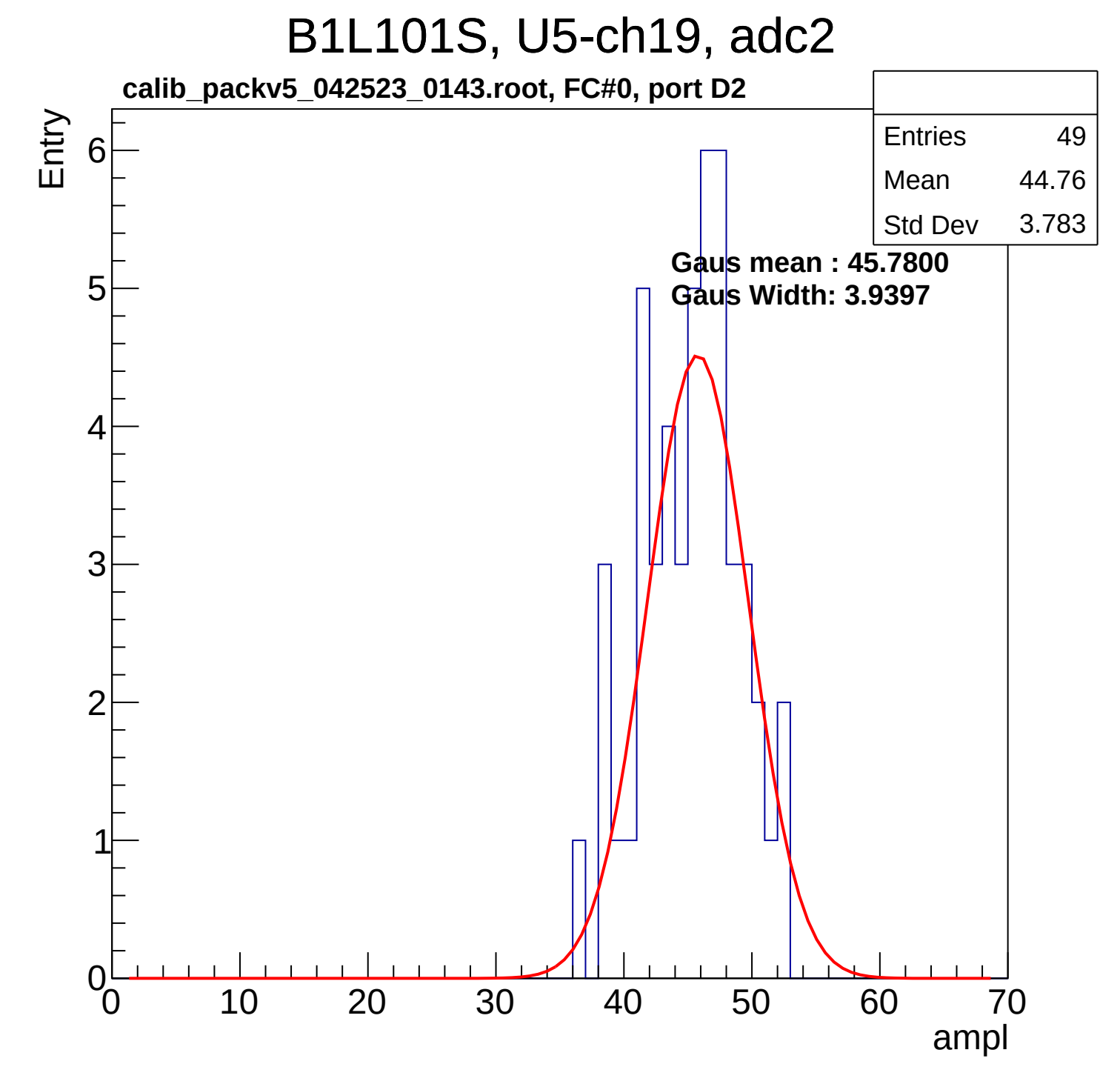
40
50
60
70


B1L101S, U5-ch19, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 44.76
Std Dev 3.783
Gaus mean : 45.7800
Gaus Width: 3.9397
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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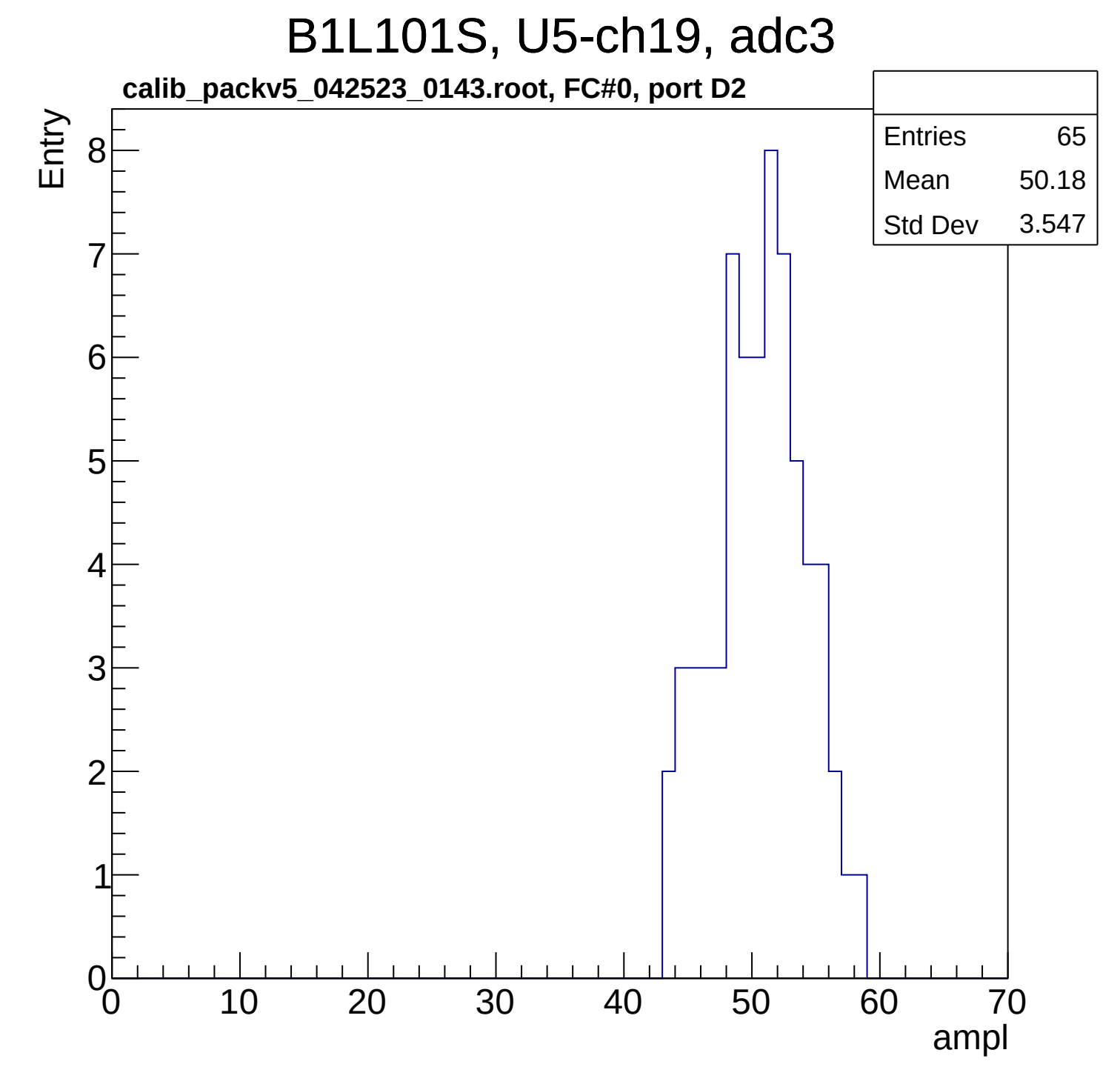
B1L101S, U5-ch19, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 50.18
Std Dev 3.547
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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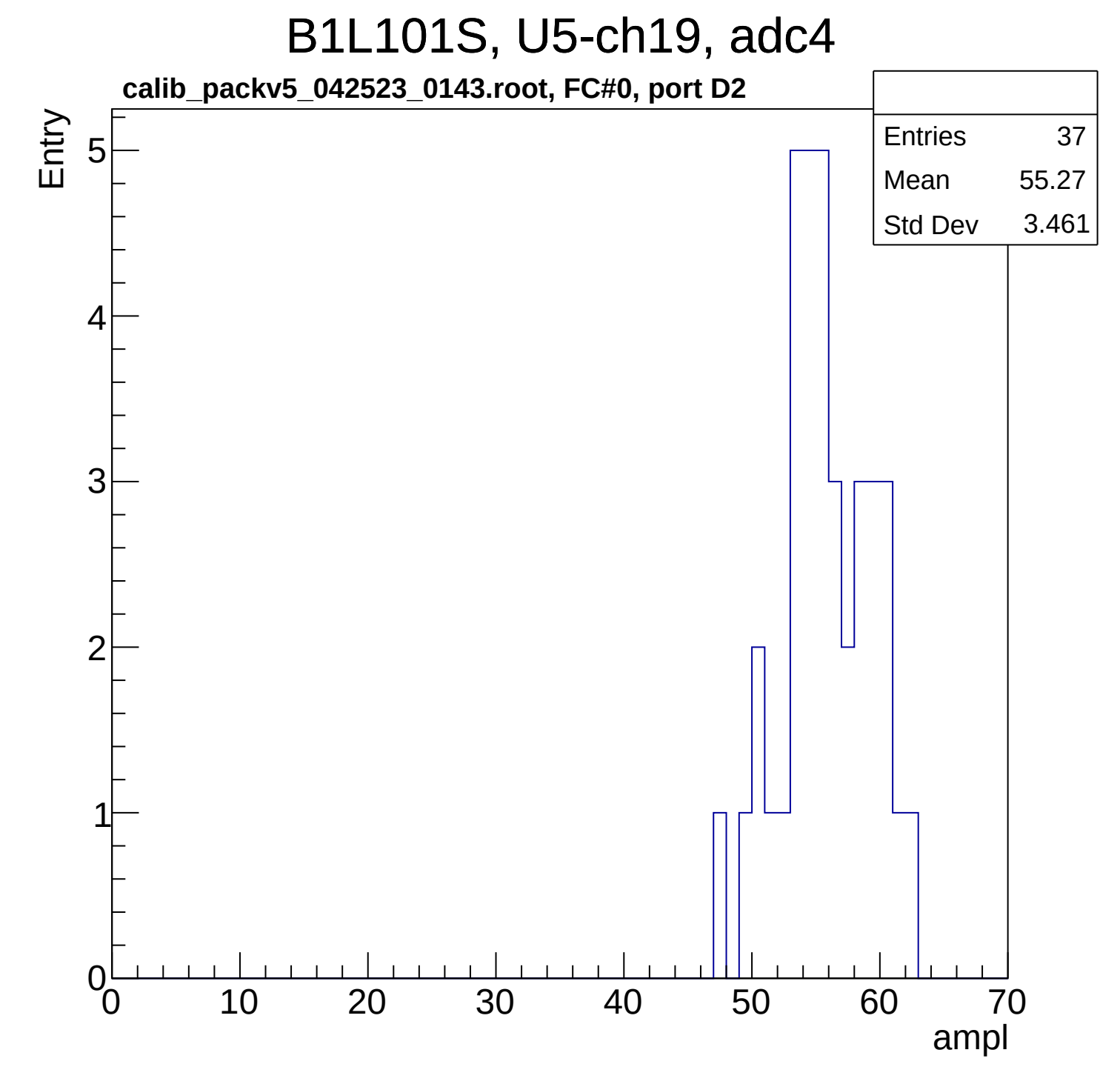
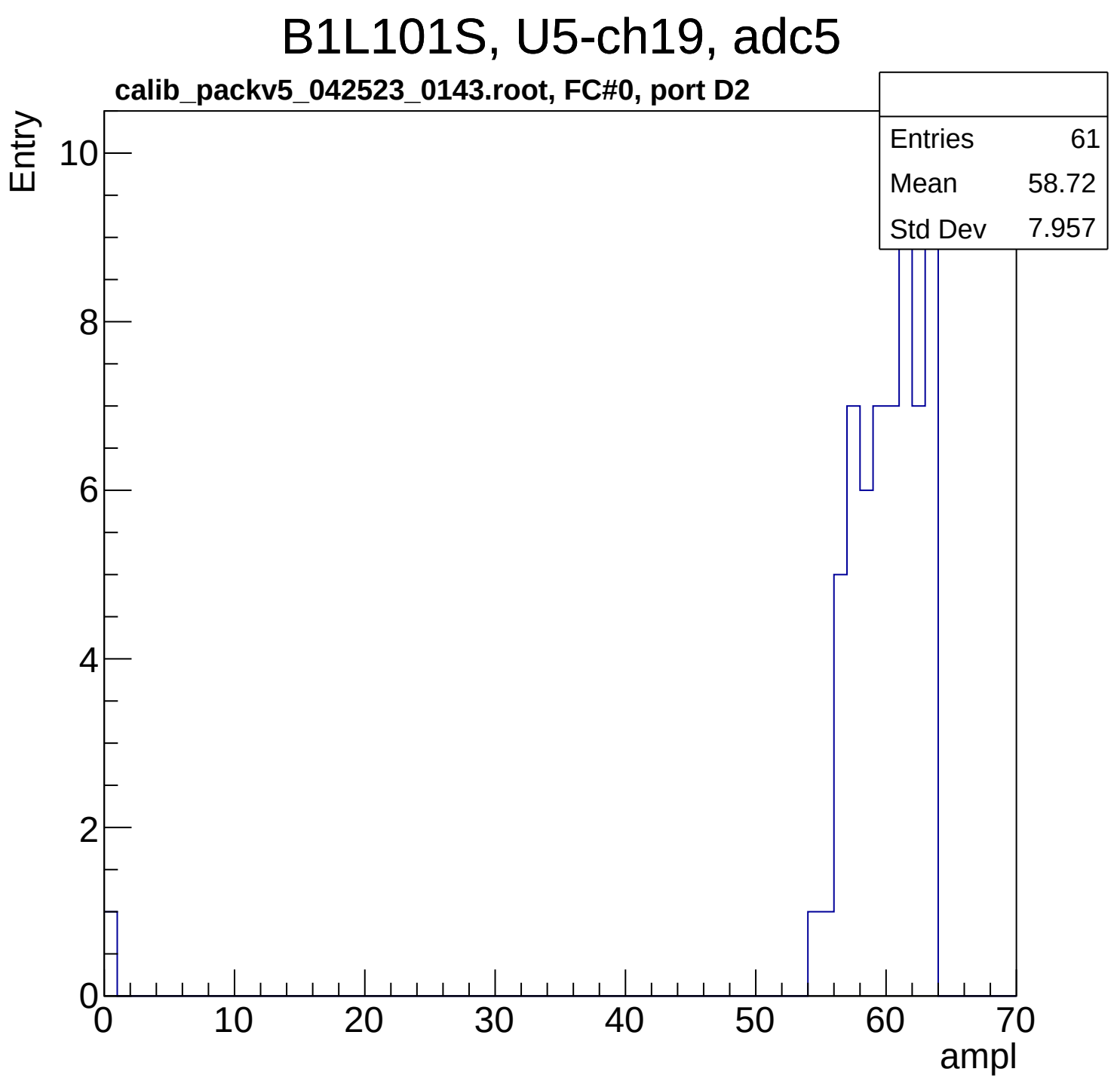
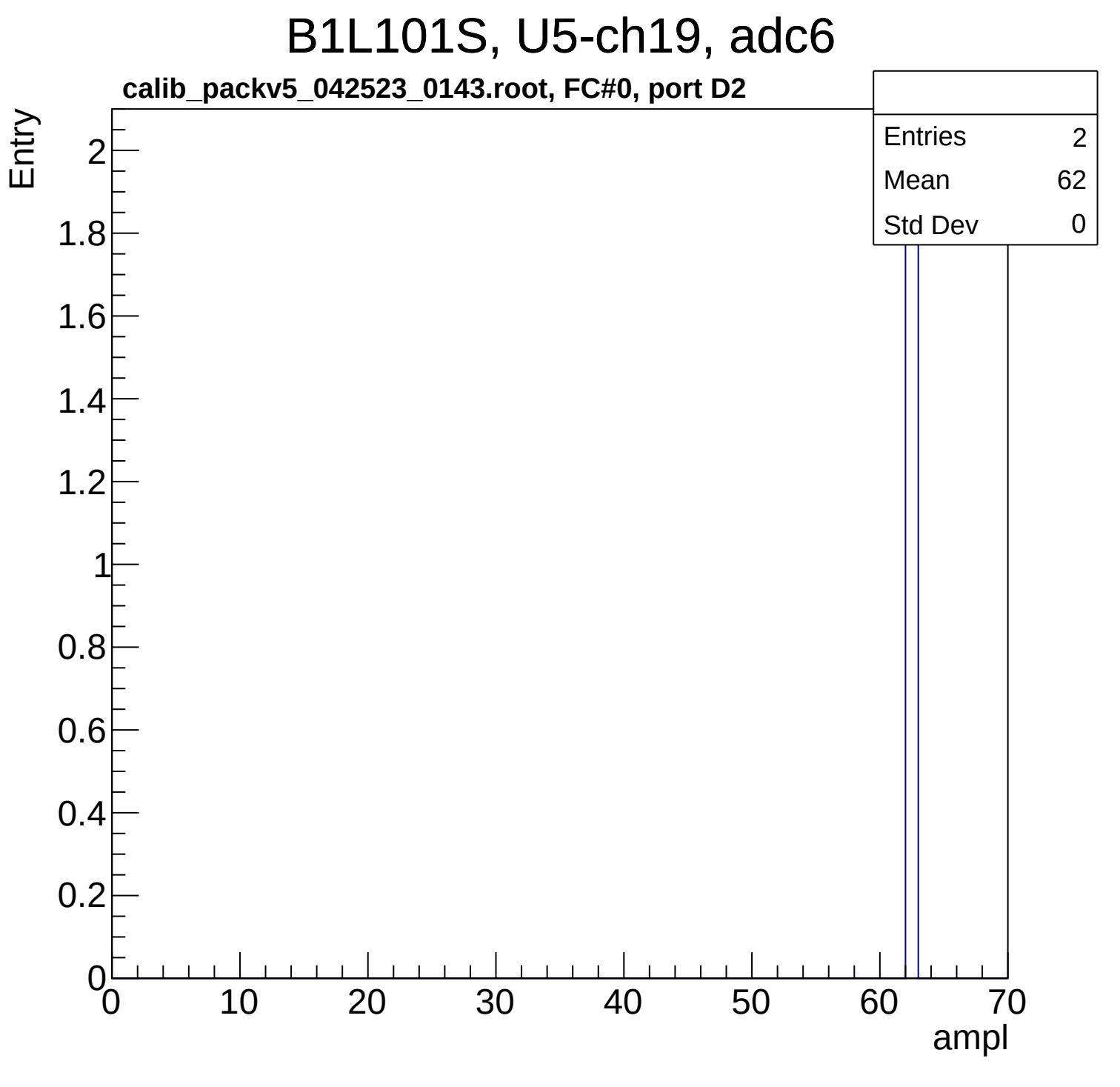
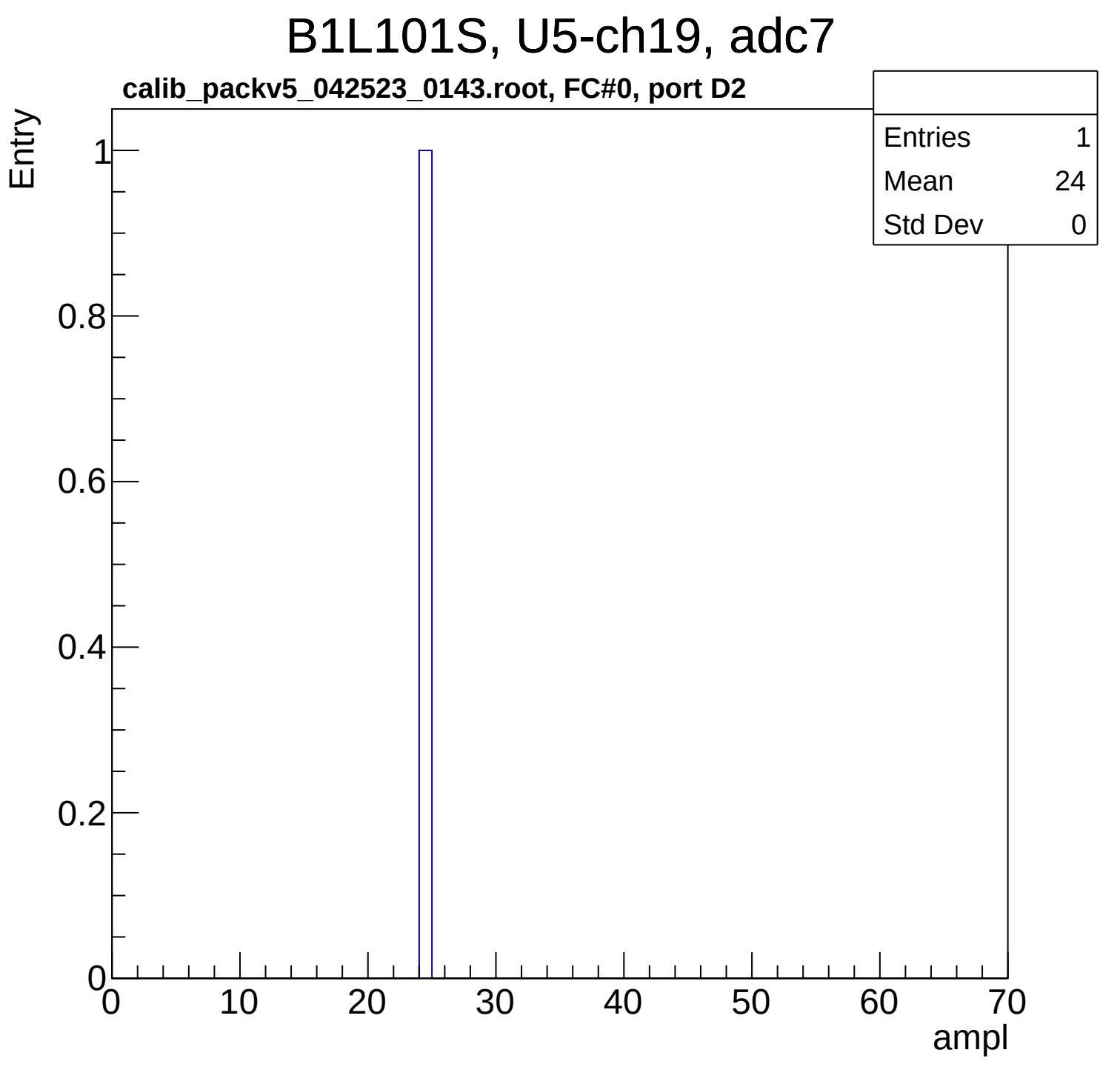
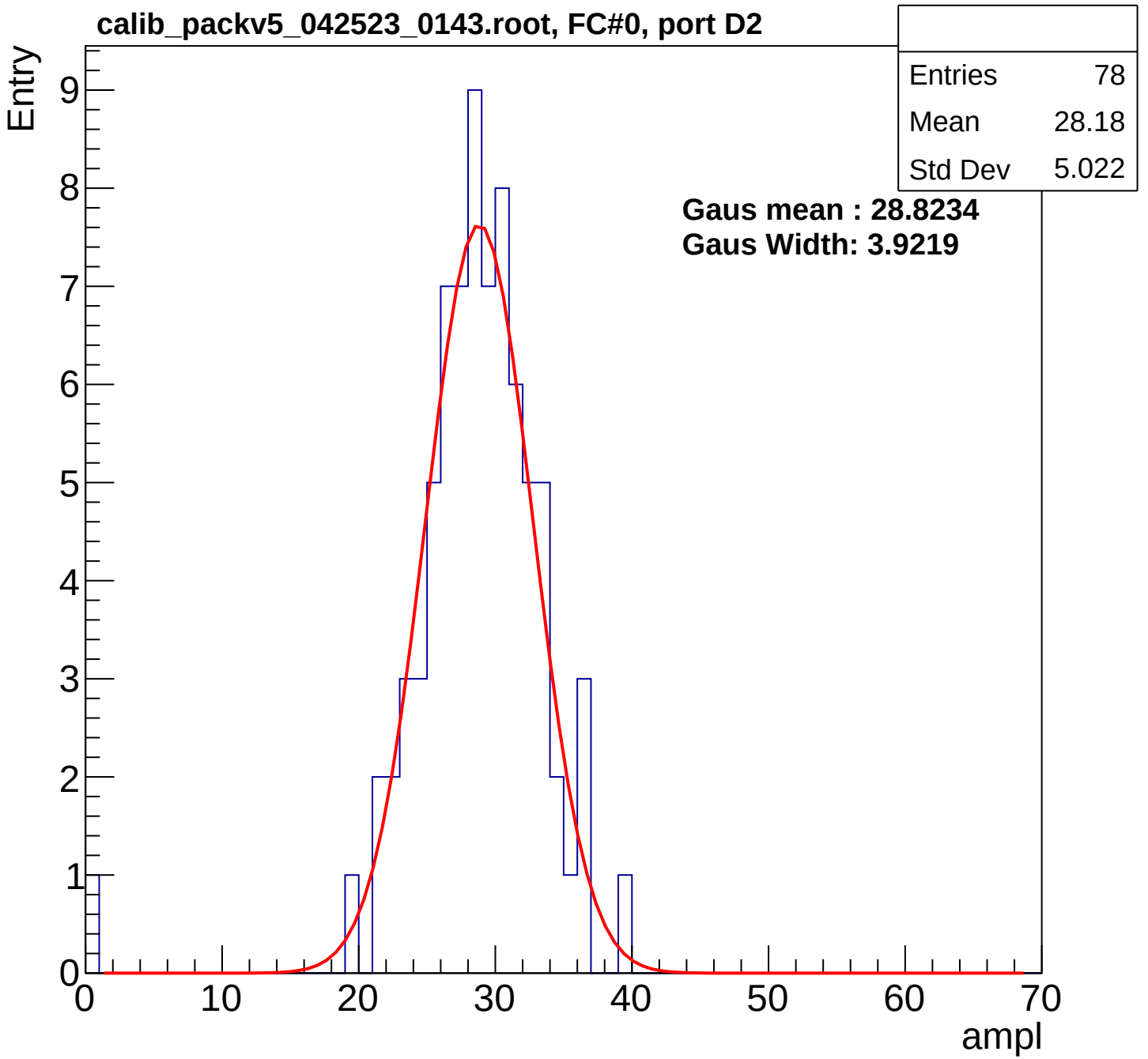
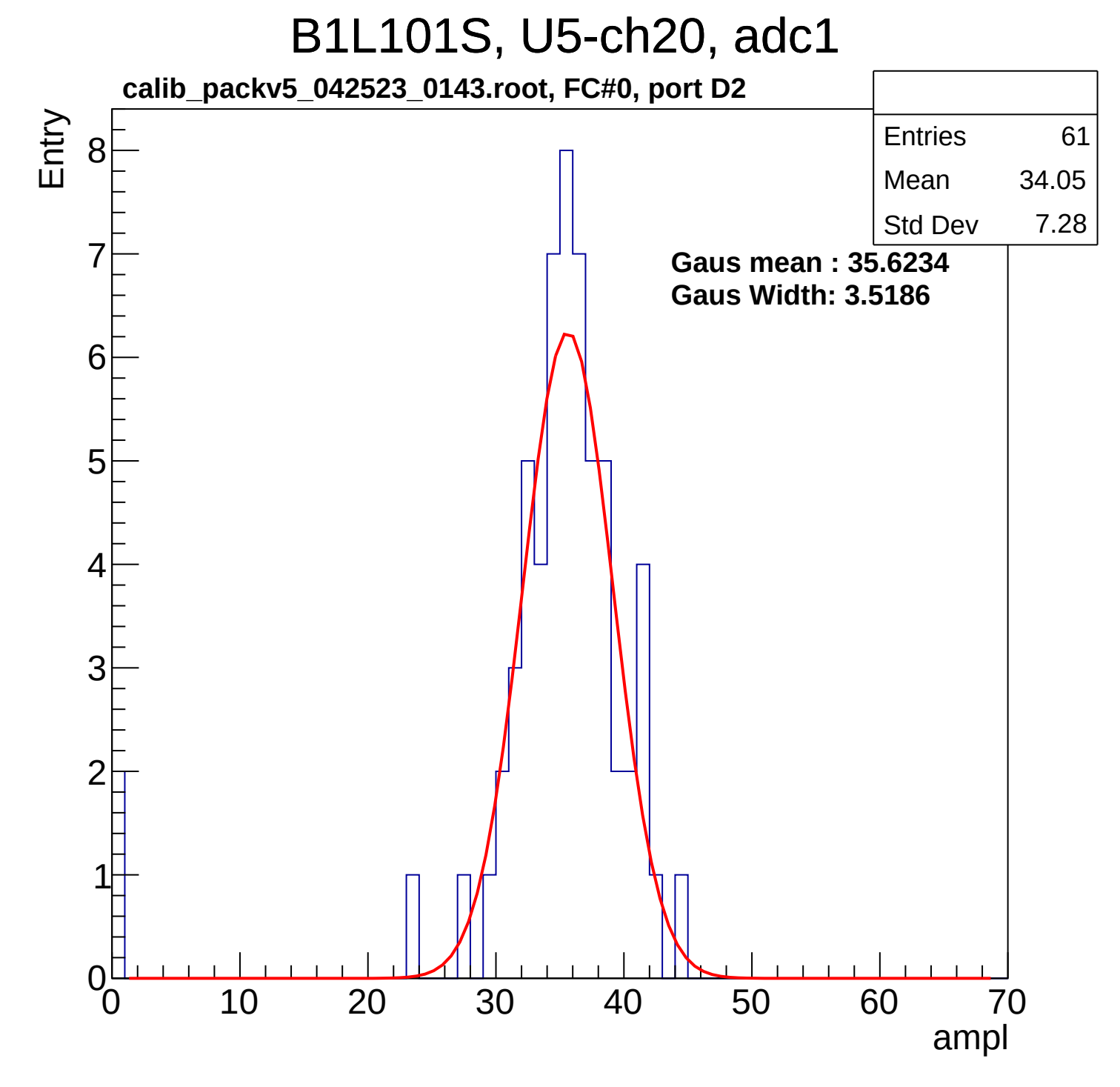

B1L101S, U5-ch19, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 37
Mean 55.27
Std Dev 3.461
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

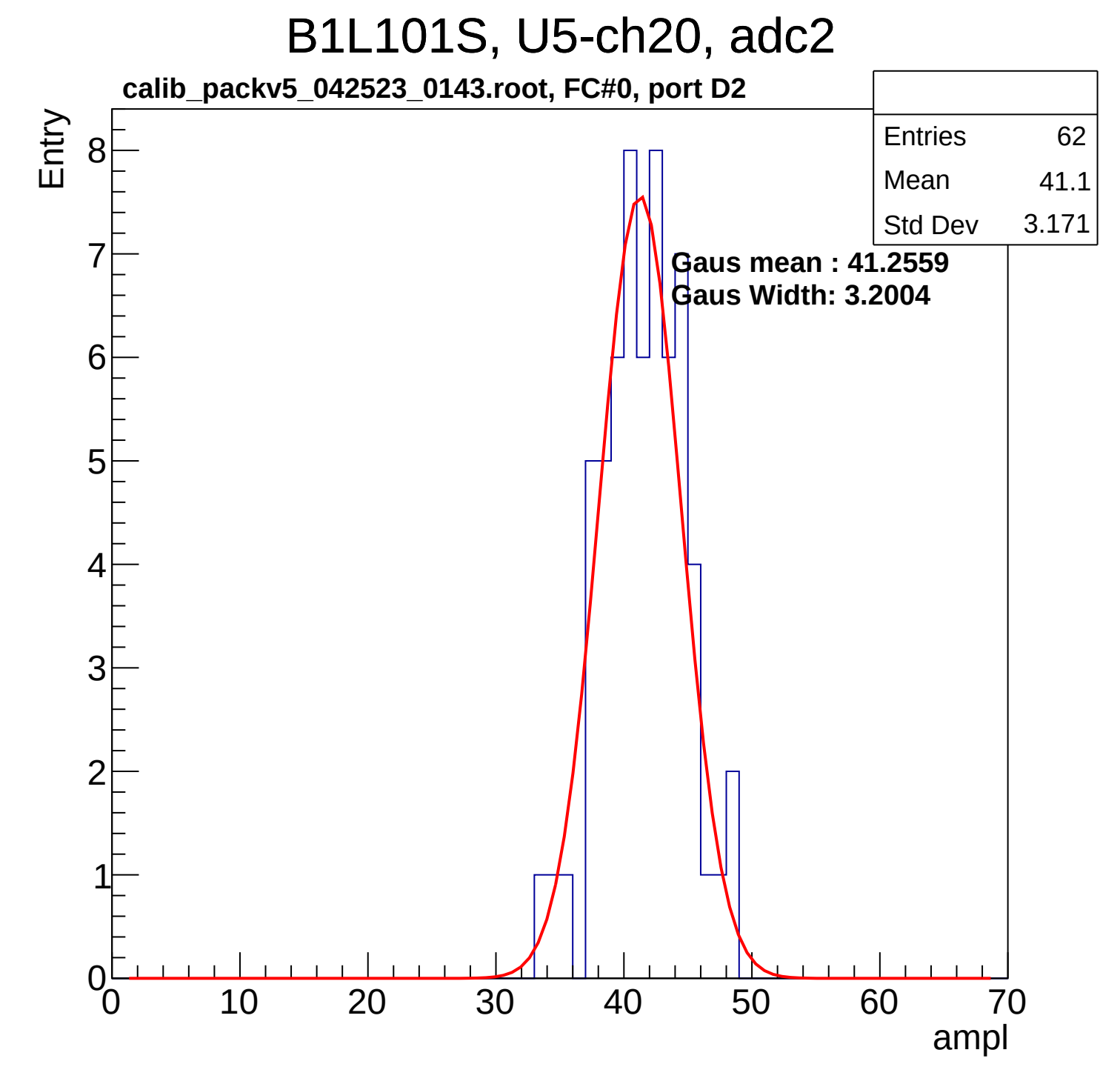

B1L101S, U5-ch19, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 58.72
Std Dev 7.957
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

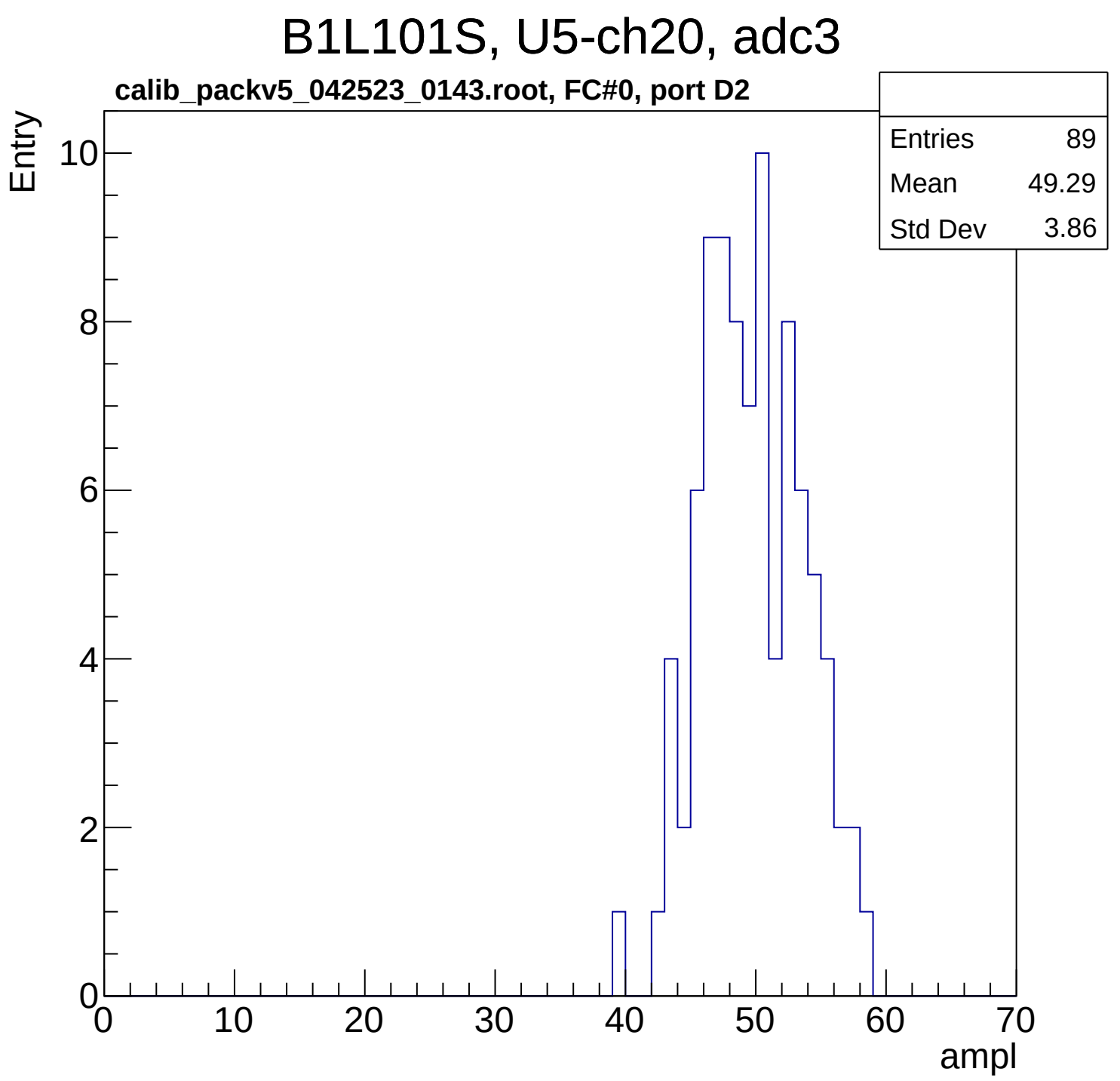

B1L101S, U5-ch19, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 62
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

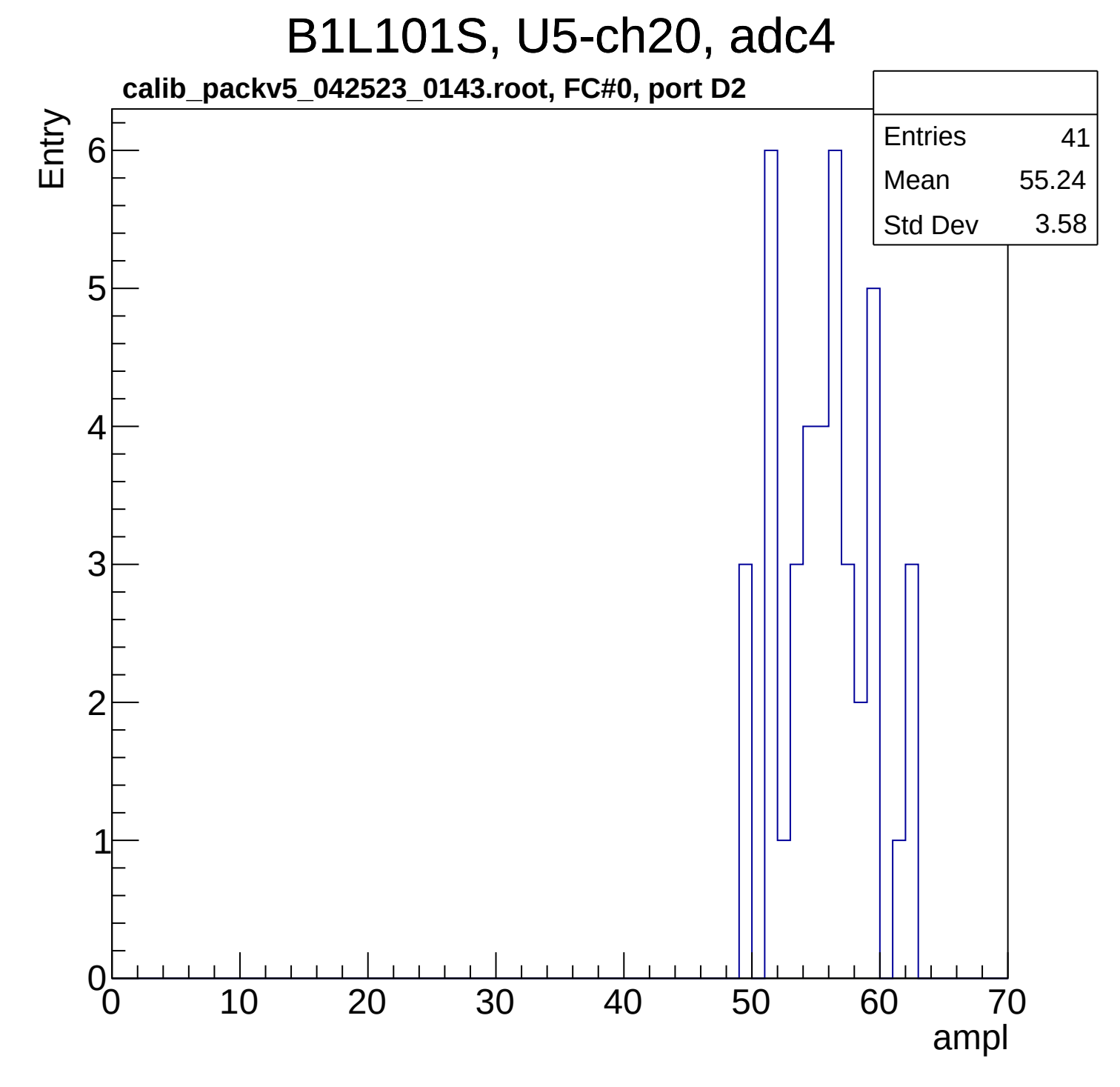

B1L101S, U5-ch19, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 24
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

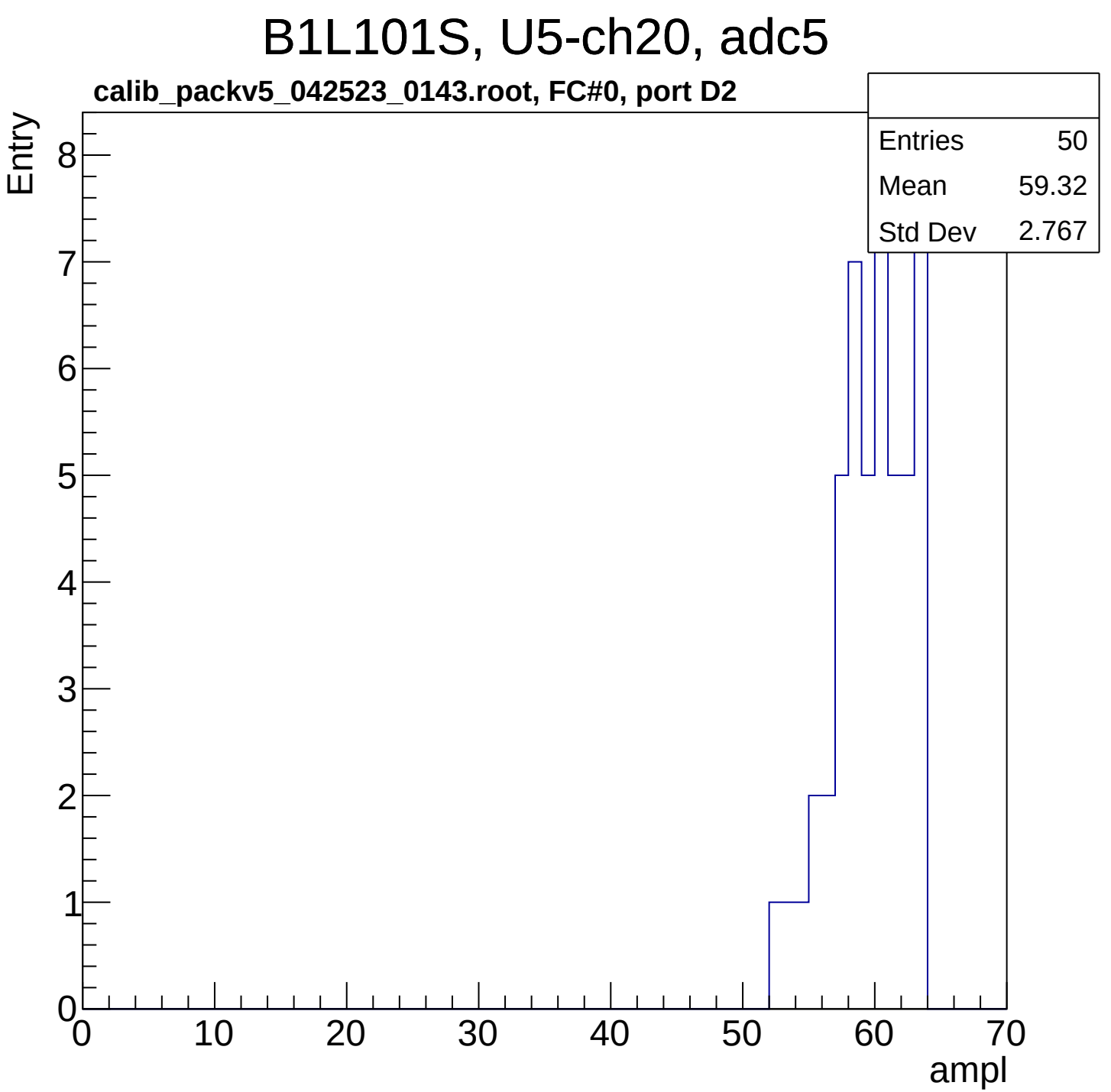

B1L101S, U5-ch20, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 28.18
Std Dev 5.022
Gaus mean : 28.8234
Gaus Width: 3.9219
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch20, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 34.05
Std Dev 7.28
Gaus mean : 35.6234
Gaus Width: 3.5186
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch20, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 41.1
Std Dev 3.171
Gaus mean : 41.2559
Gaus Width: 3.2004
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch20, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 89
Mean 49.29
Std Dev 3.86
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch20, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 41
Mean 55.24
Std Dev 3.58
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch20, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 59.32
Std Dev 2.767
Entry
ampl
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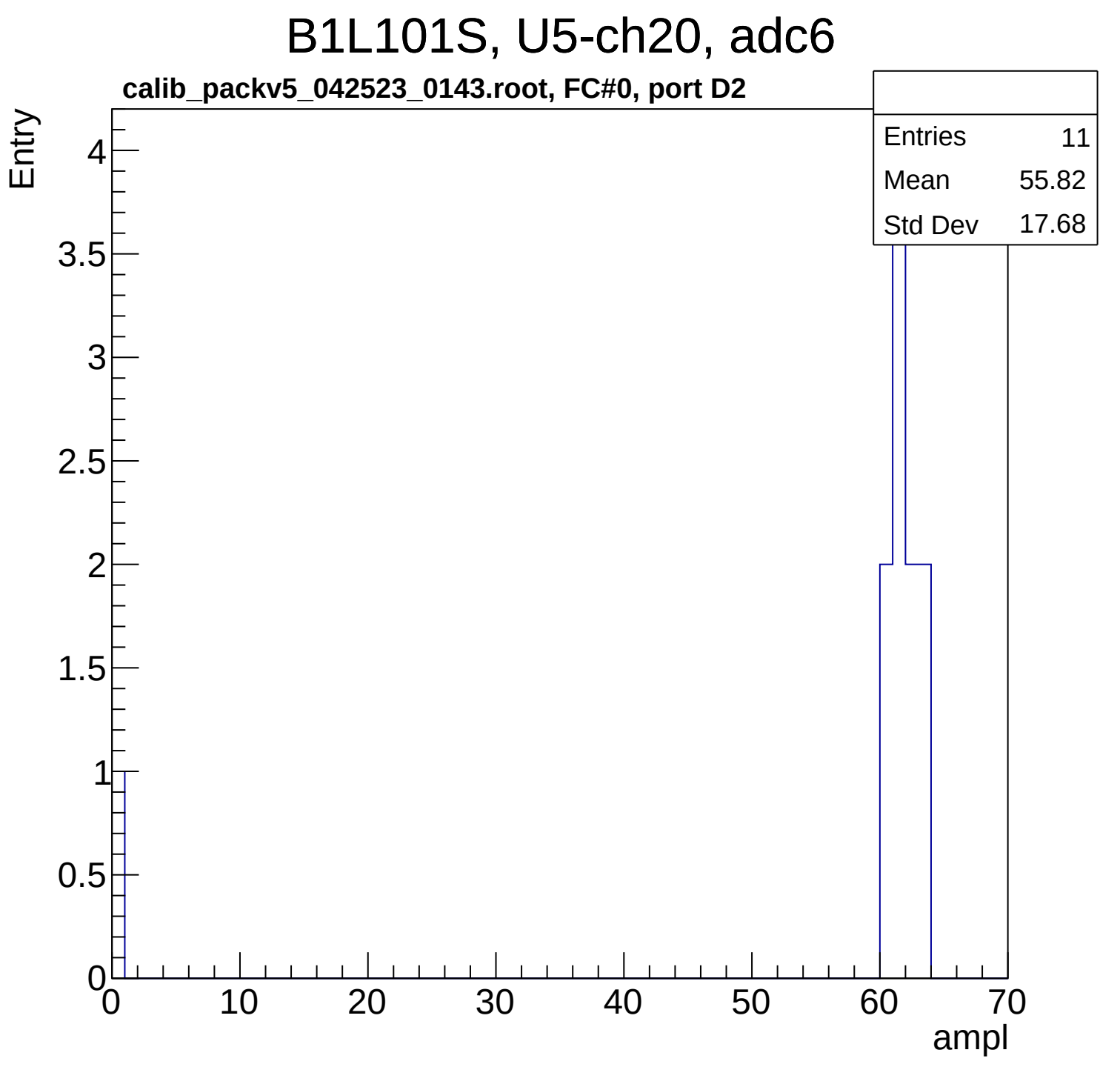
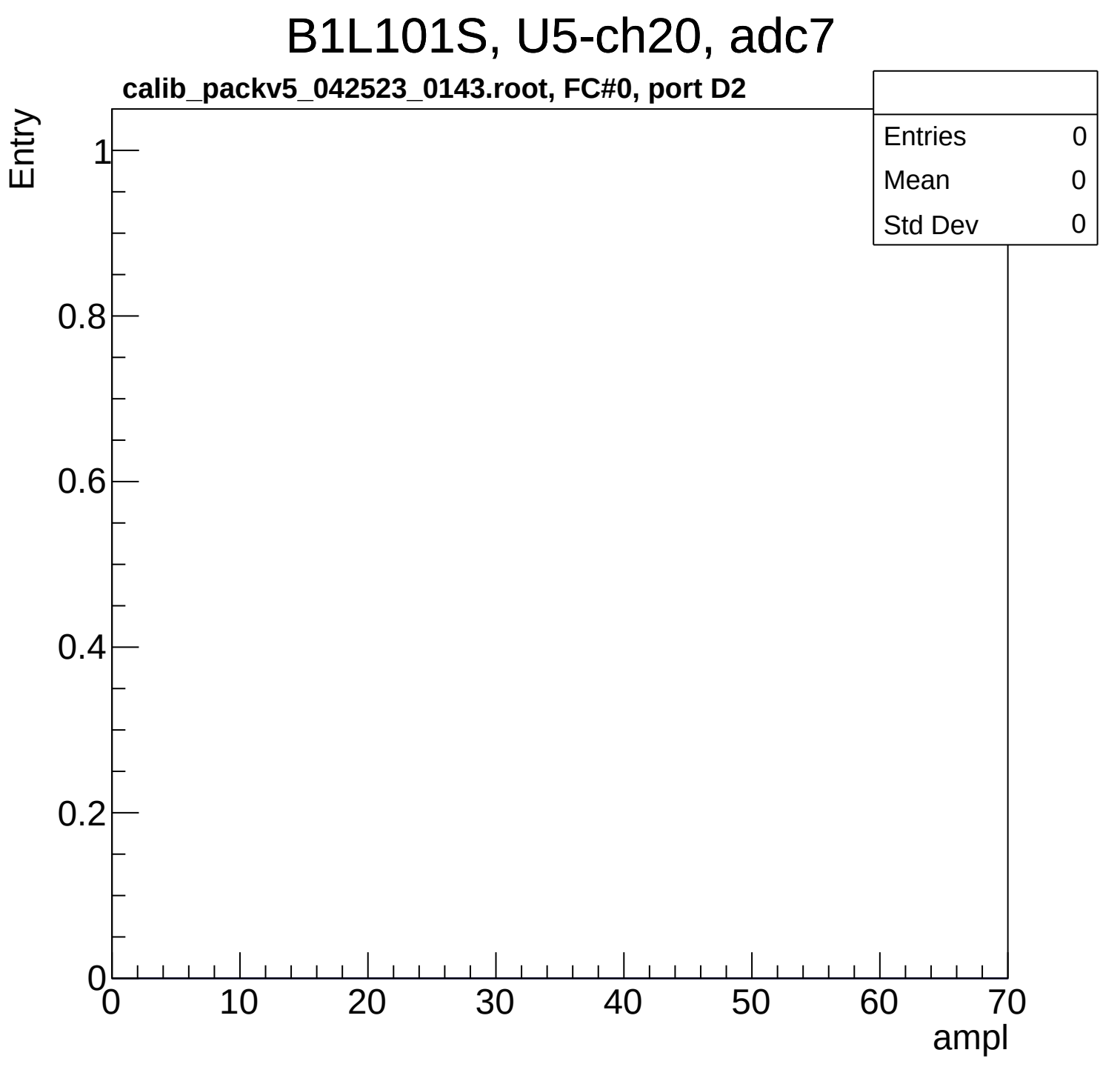
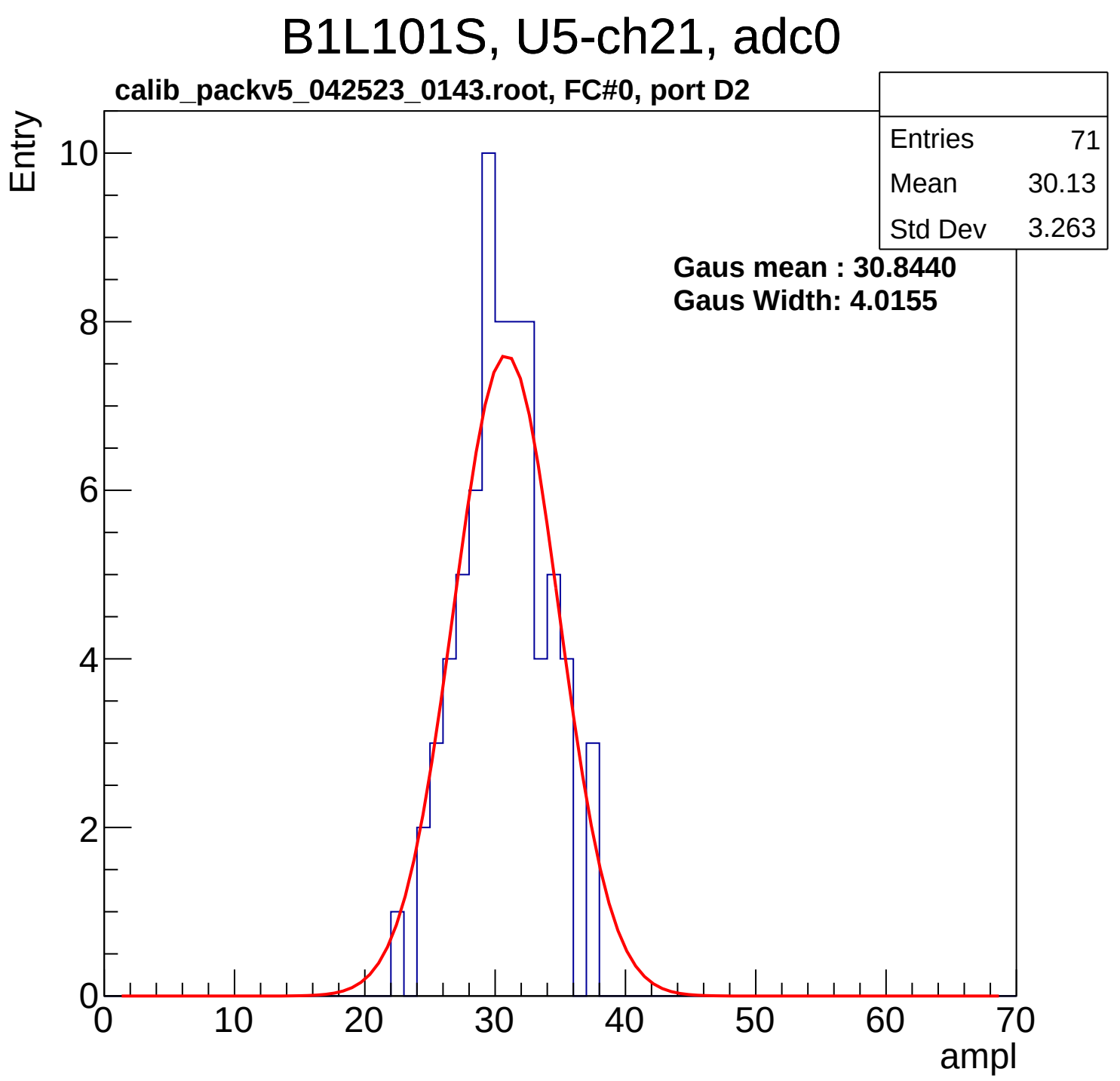
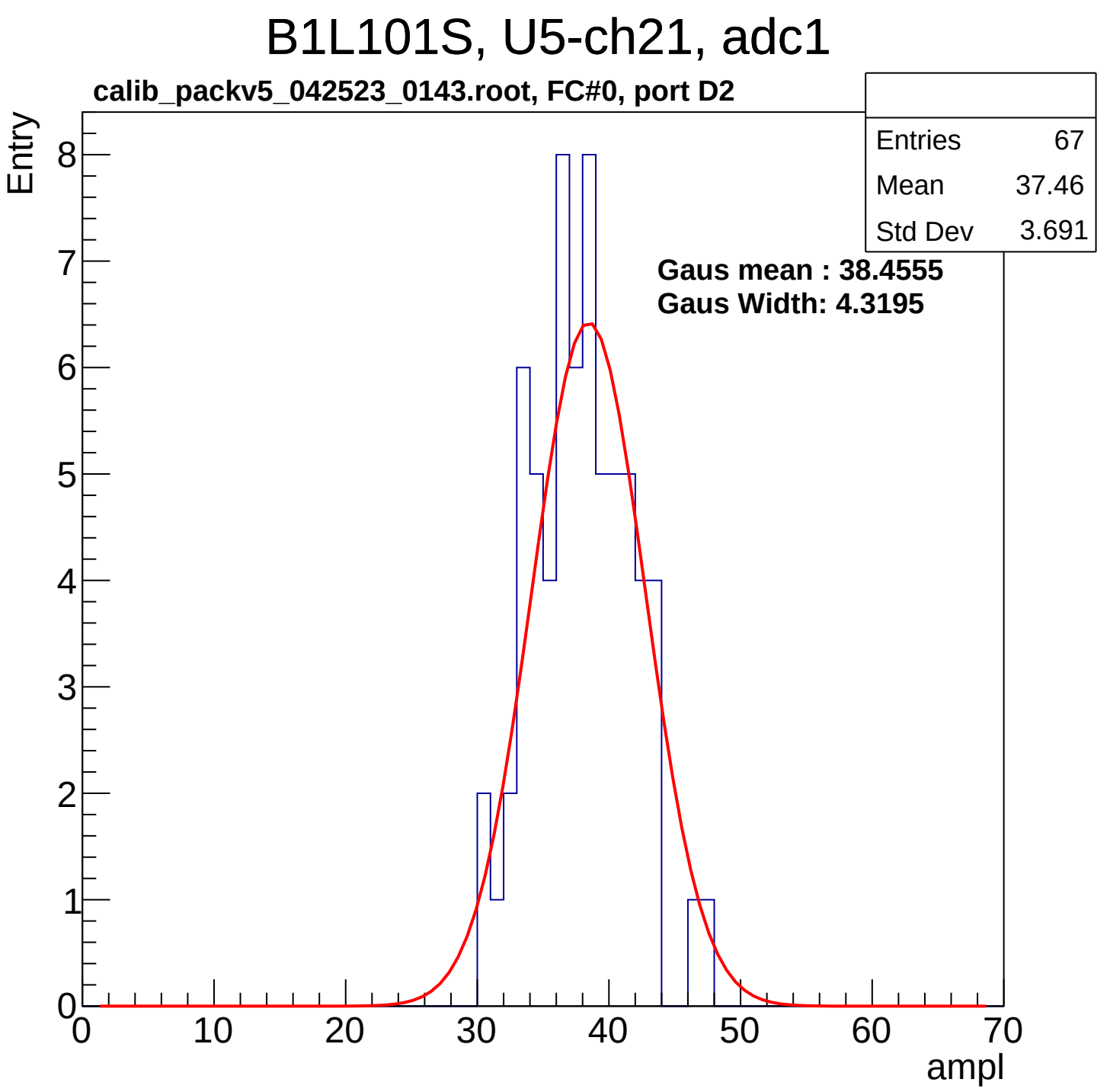
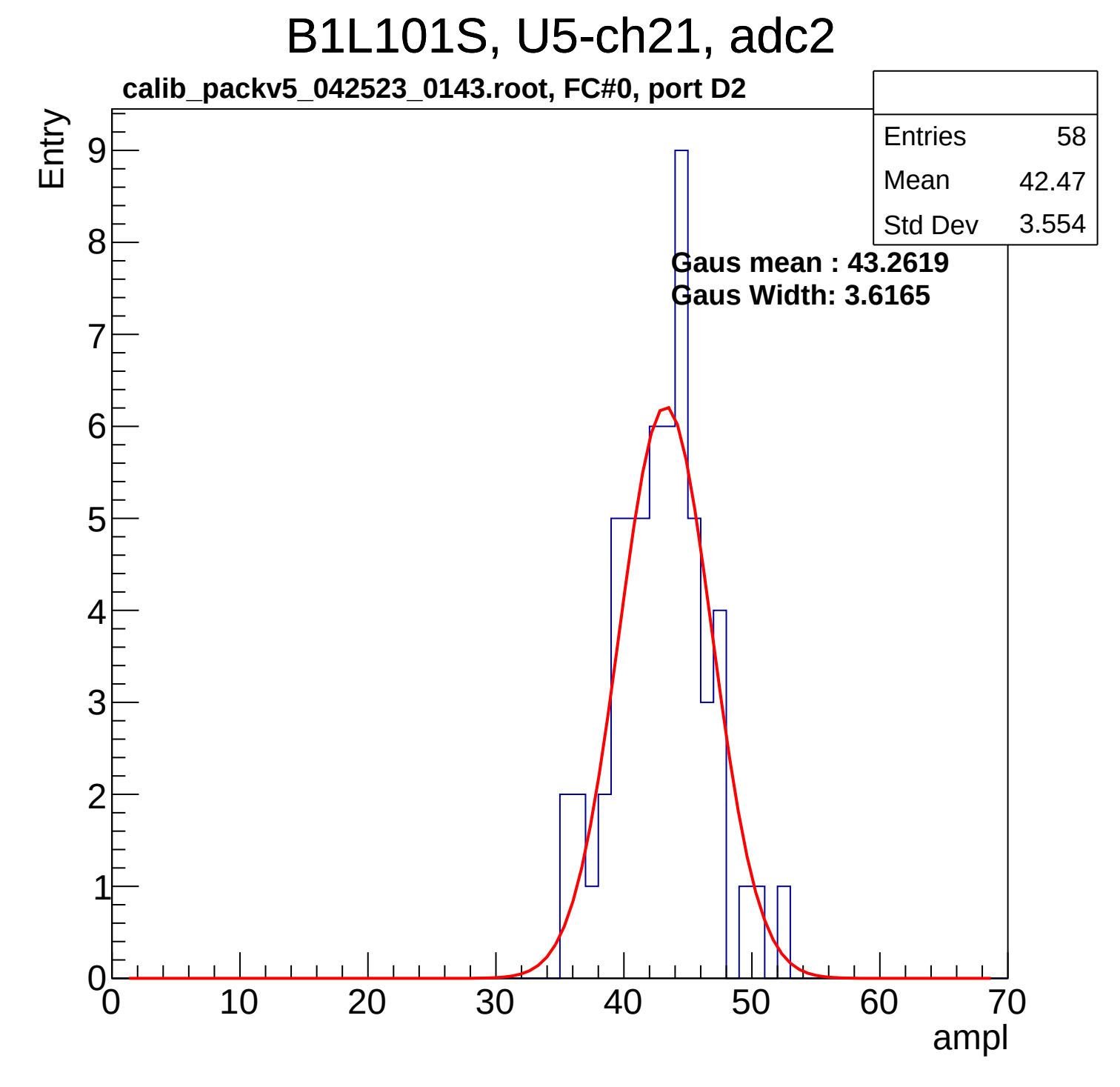
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

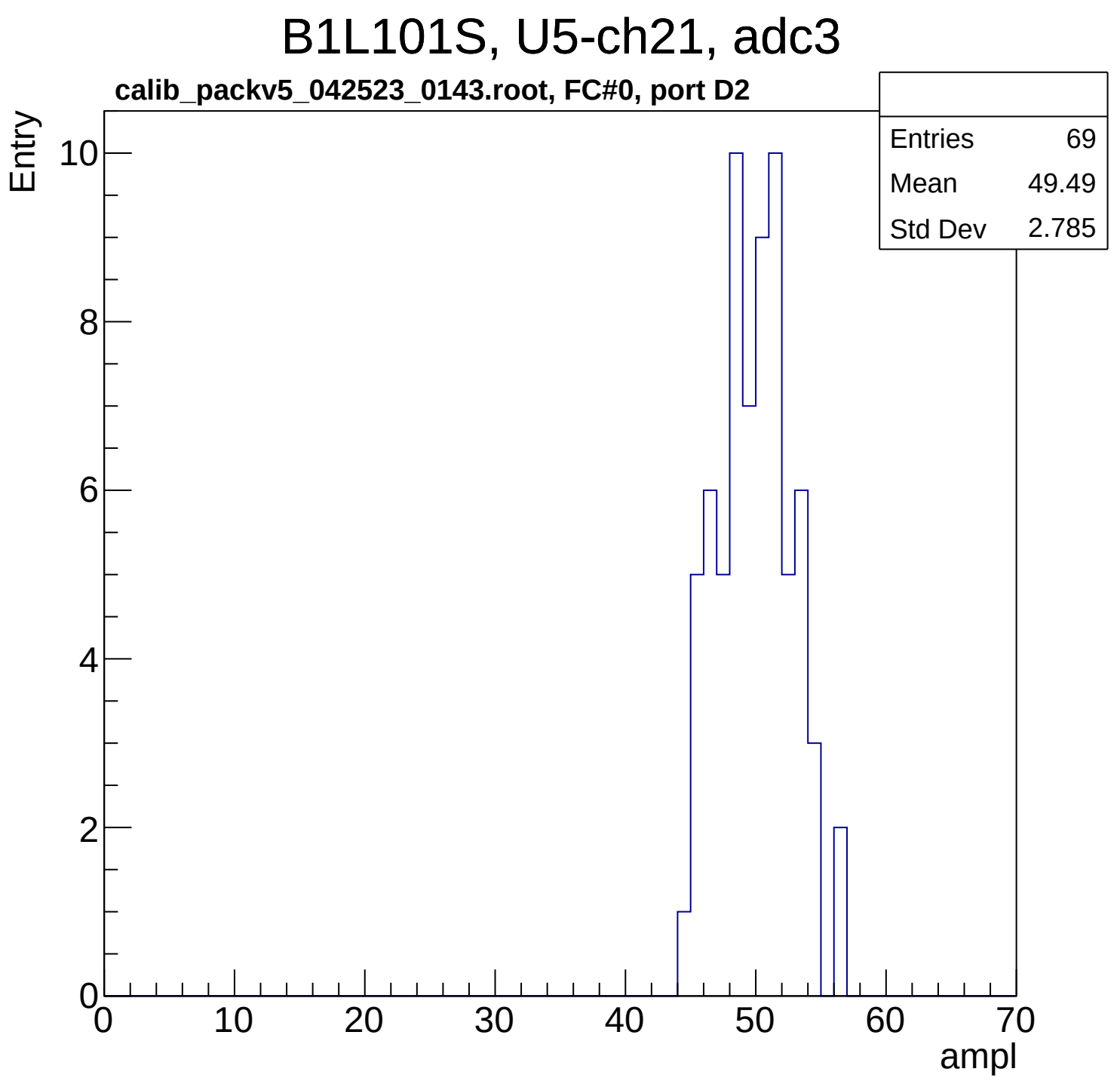

B1L101S, U5-ch20, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 11
Mean 55.82
Std Dev 17.68
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

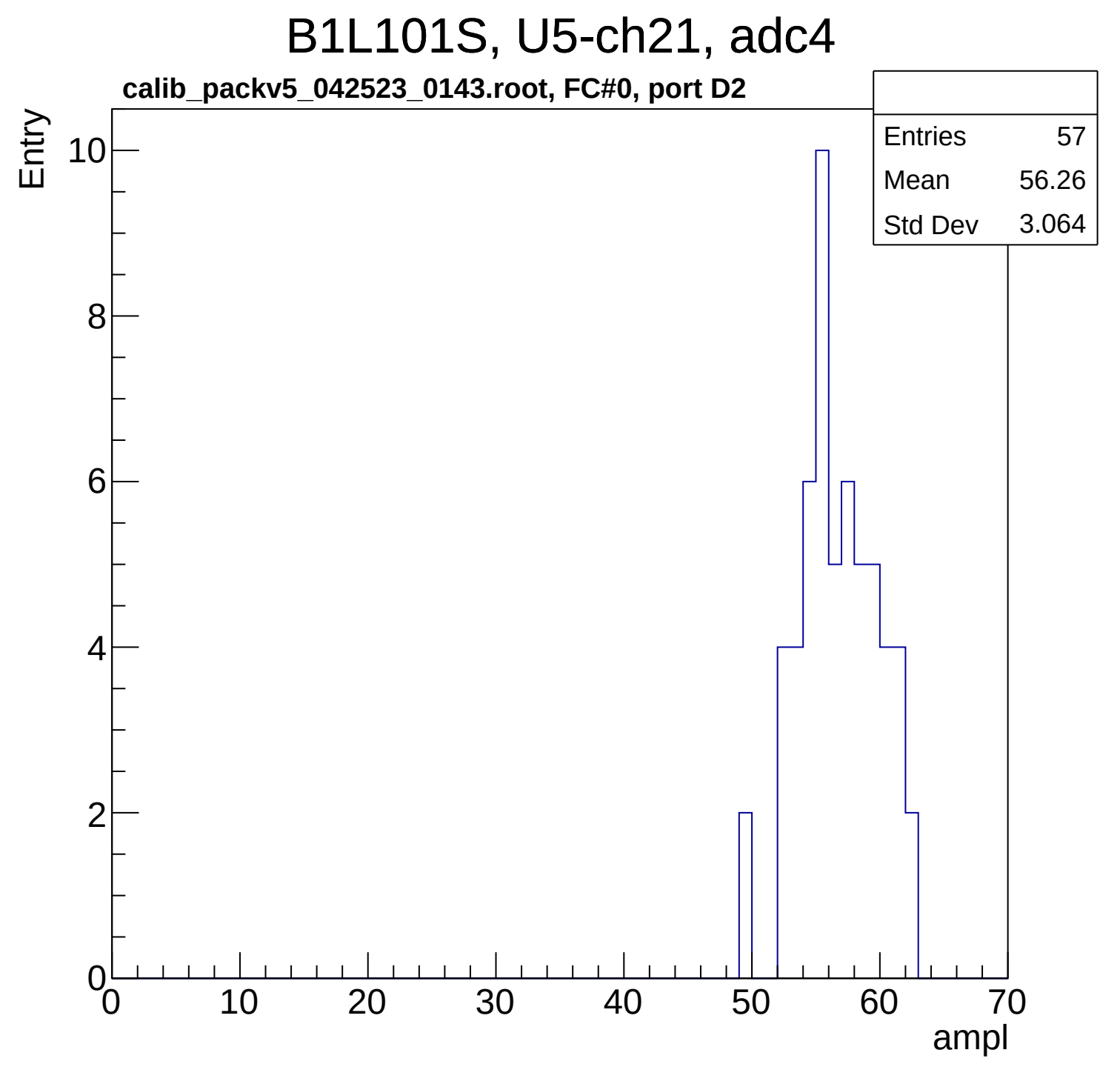

B1L101S, U5-ch20, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

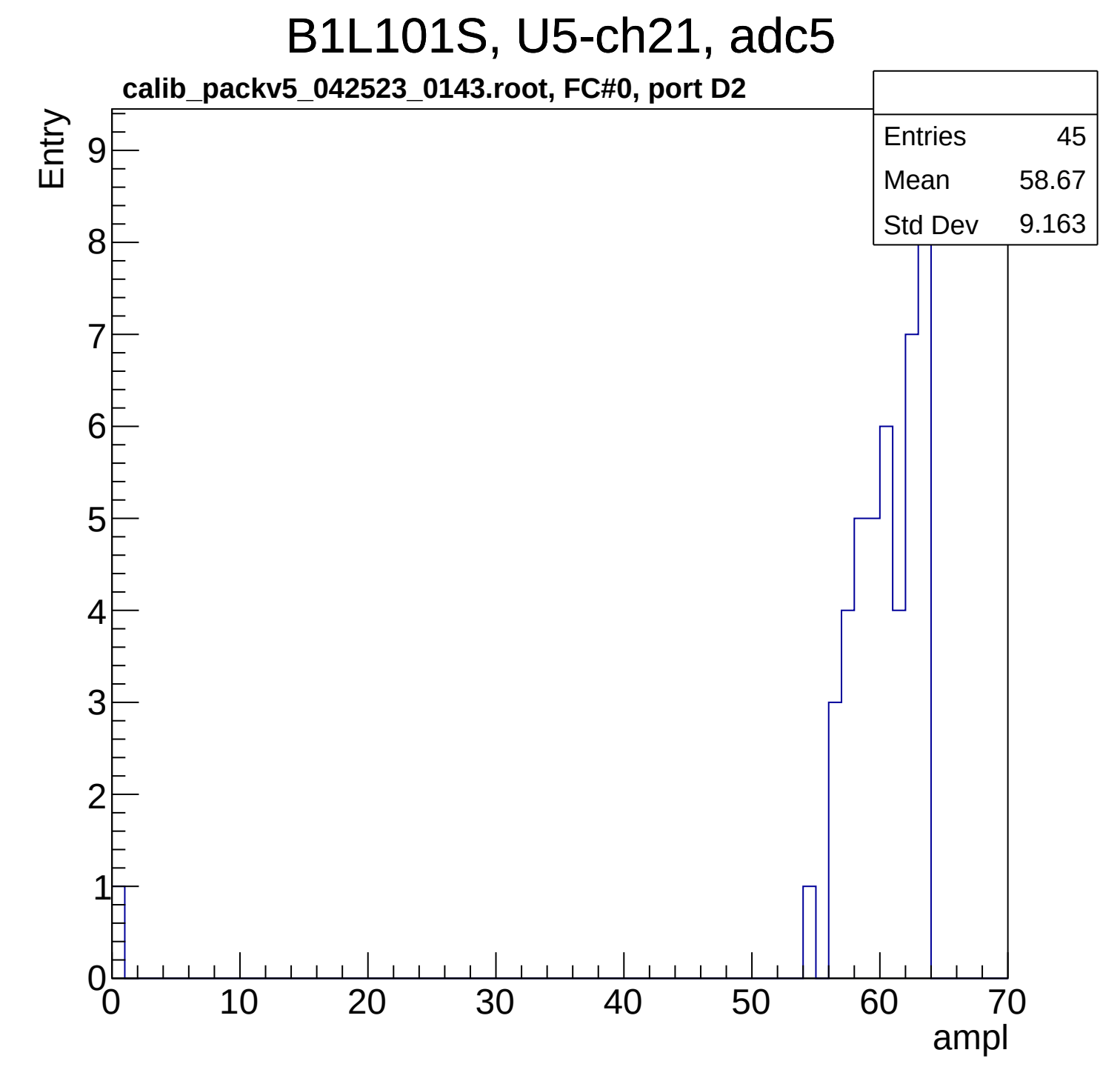

B1L101S, U5-ch21, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 30.13
Std Dev 3.263
Gaus mean : 30.8440
Gaus Width: 4.0155
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch21, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 37.46
Std Dev 3.691
Gaus mean : 38.4555
Gaus Width: 4.3195
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch21, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 42.47
Std Dev 3.554
Gaus mean : 43.2619
Gaus Width: 3.6165
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch21, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 49.49
Std Dev 2.785
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch21, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 56.26
Std Dev 3.064
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch21, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 58.67
Std Dev 9.163
Entry
ampl
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7
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0
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60
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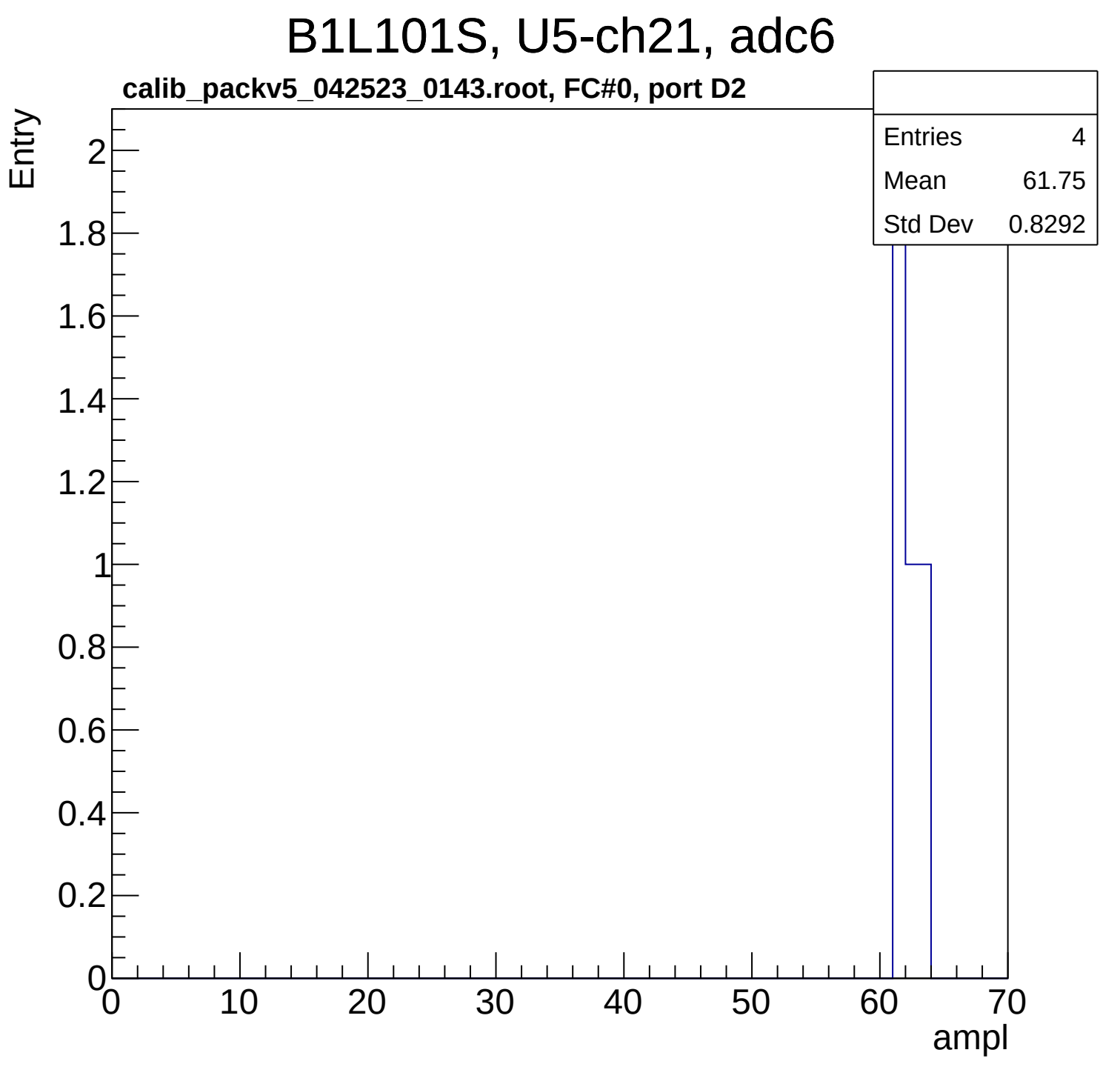
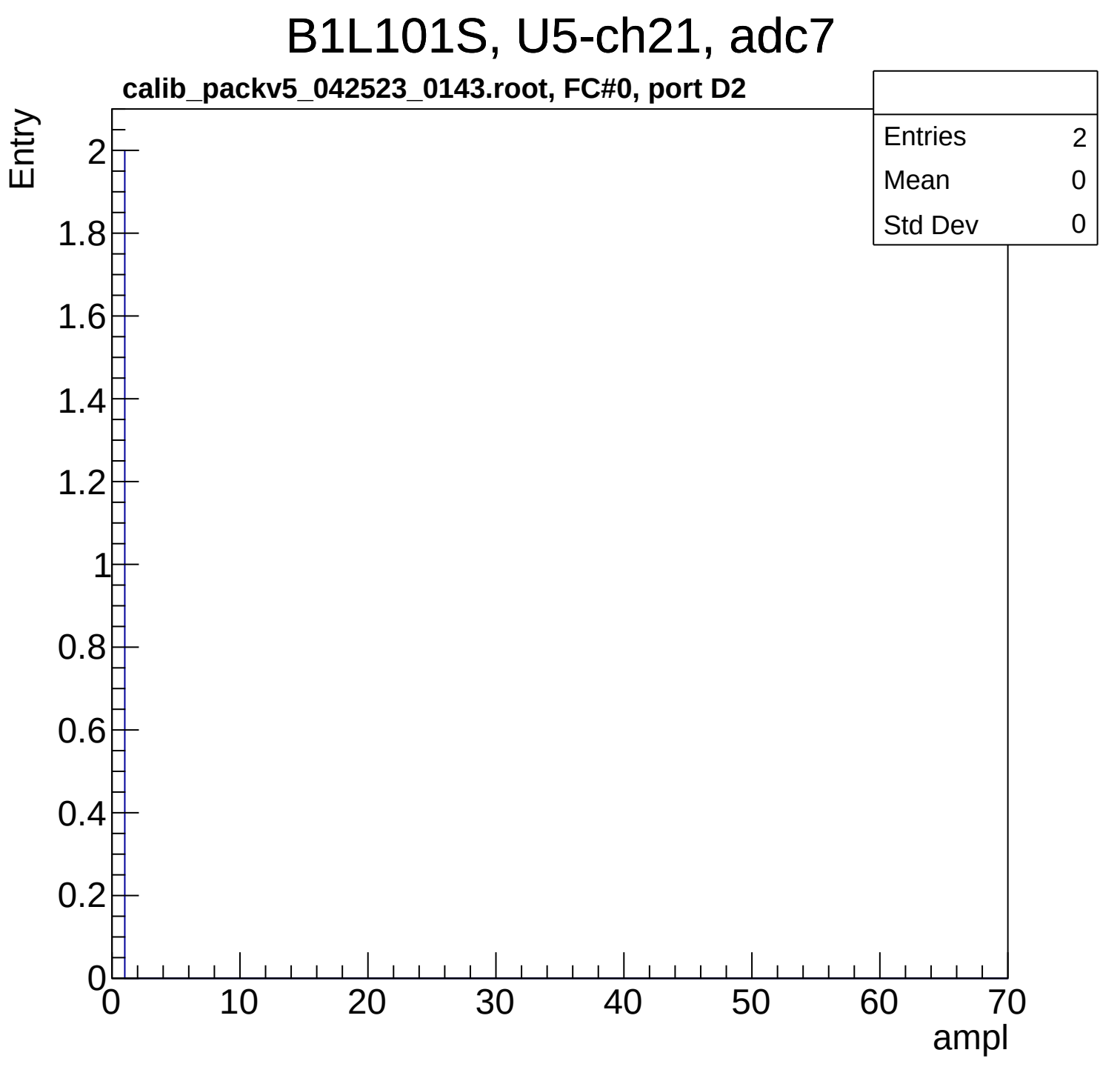
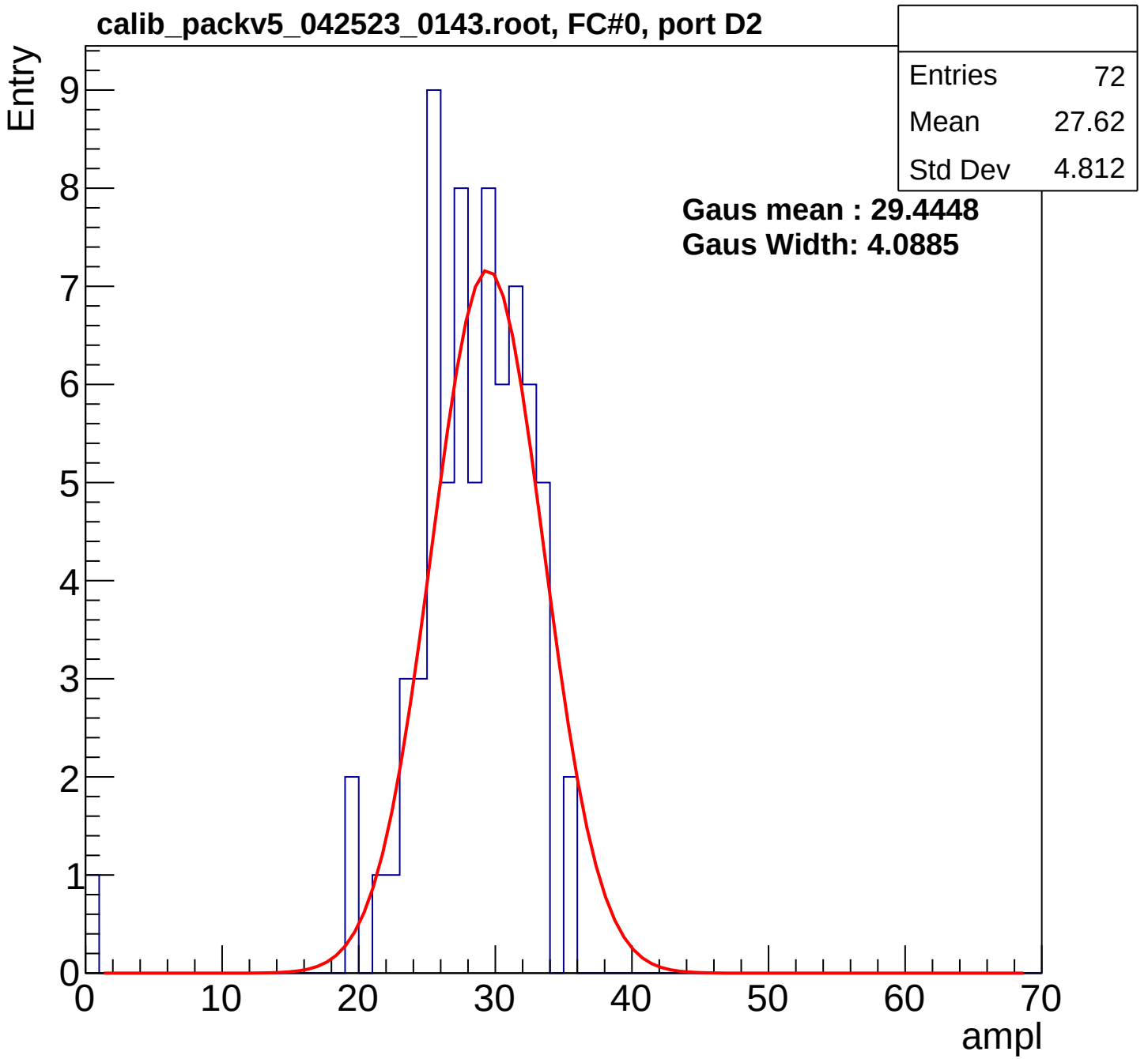
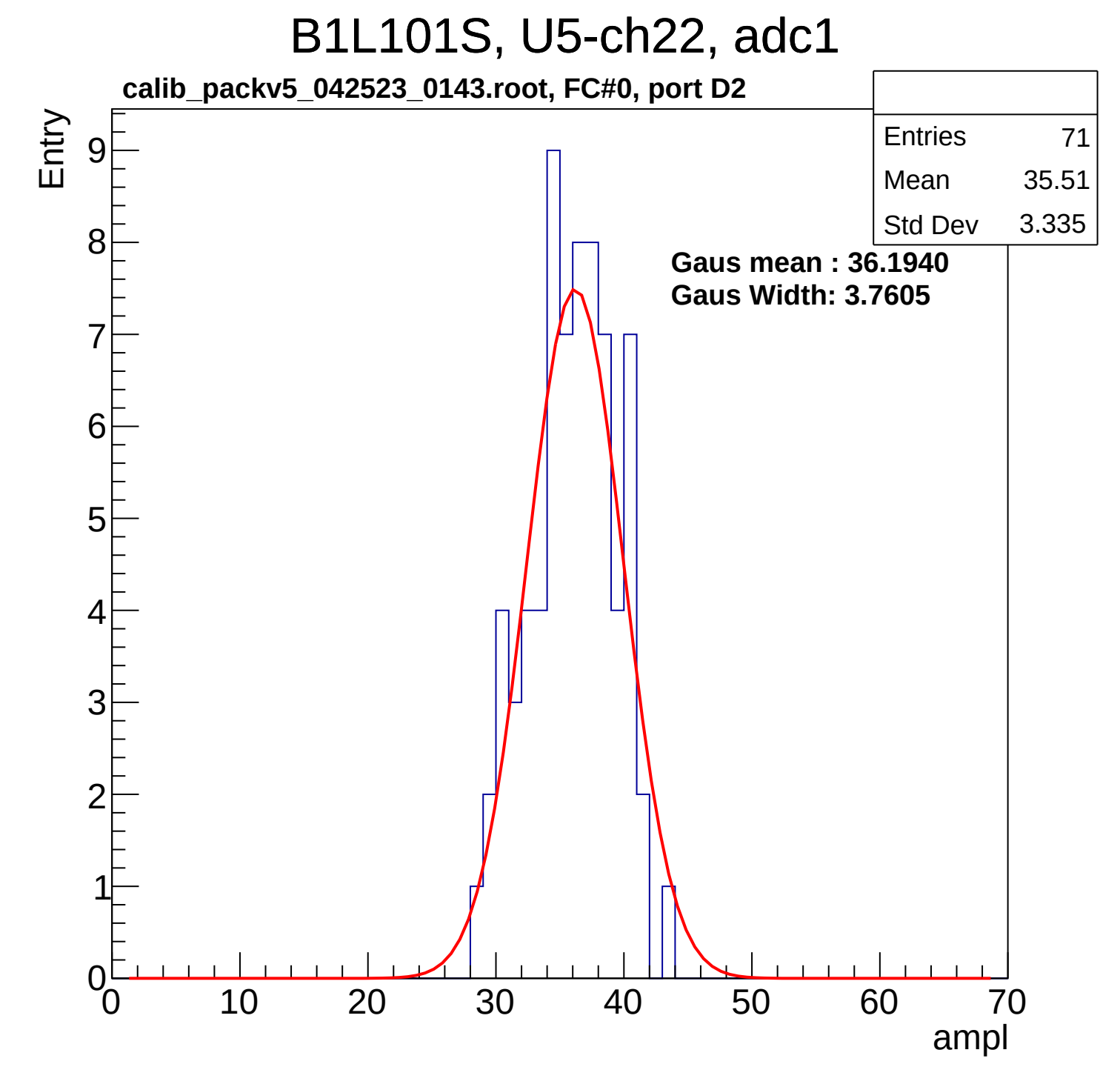
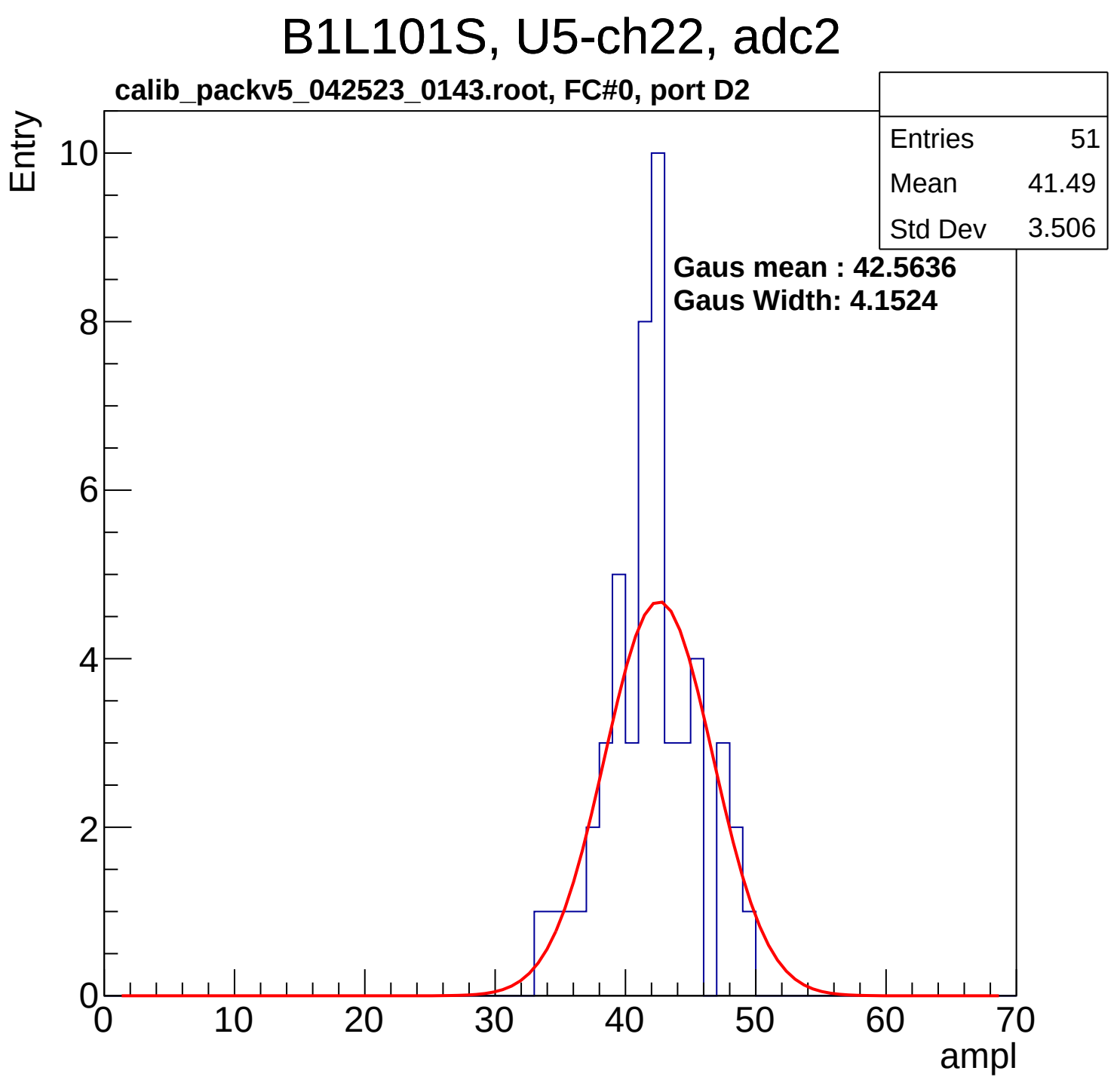

B1L101S, U5-ch21, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 61.75
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U5-ch21, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U5-ch22, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 27.62
Std Dev 4.812
Gaus mean : 29.4448
Gaus Width: 4.0885
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch22, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 35.51
Std Dev 3.335
Gaus mean : 36.1940
Gaus Width: 3.7605
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch22, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 41.49
Std Dev 3.506
Gaus mean : 42.5636
Gaus Width: 4.1524
Entry
ampl
0
2
4
6
8
10
0
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20
30
40
50
60
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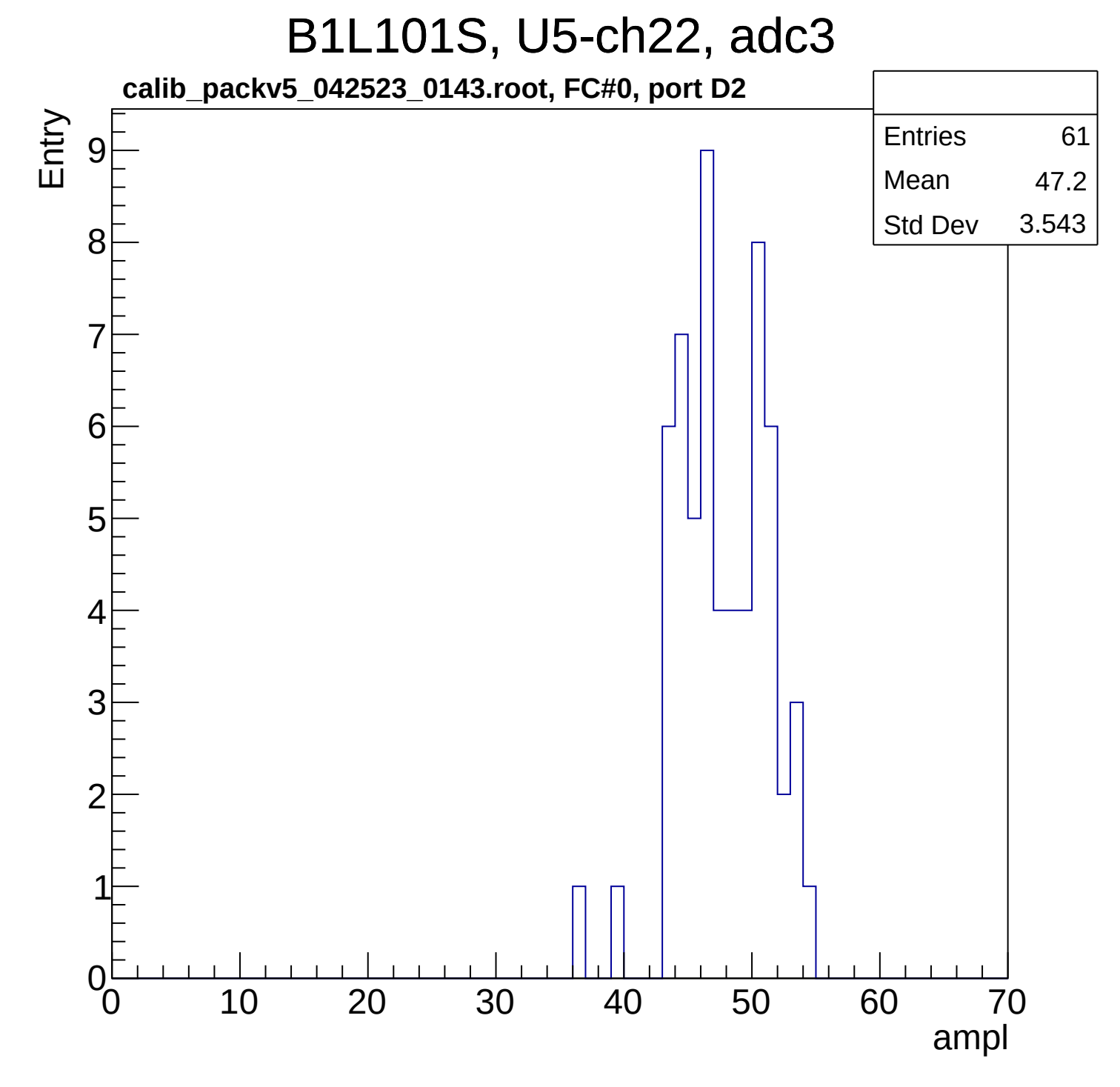
B1L101S, U5-ch22, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 47.2
Std Dev 3.543
Entry
ampl
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2
3
4
5
6
7
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0
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60
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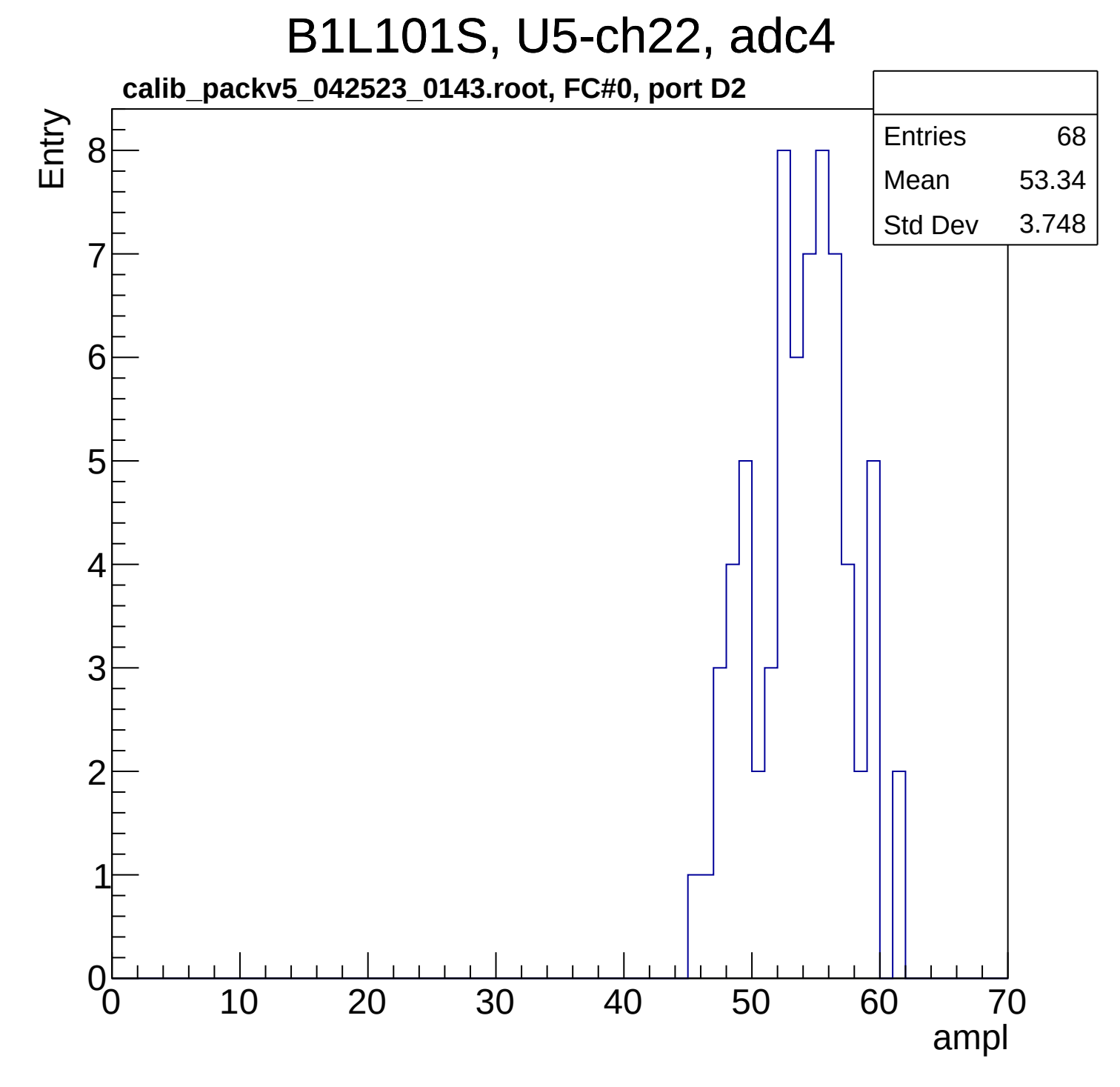
B1L101S, U5-ch22, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 53.34
Std Dev 3.748
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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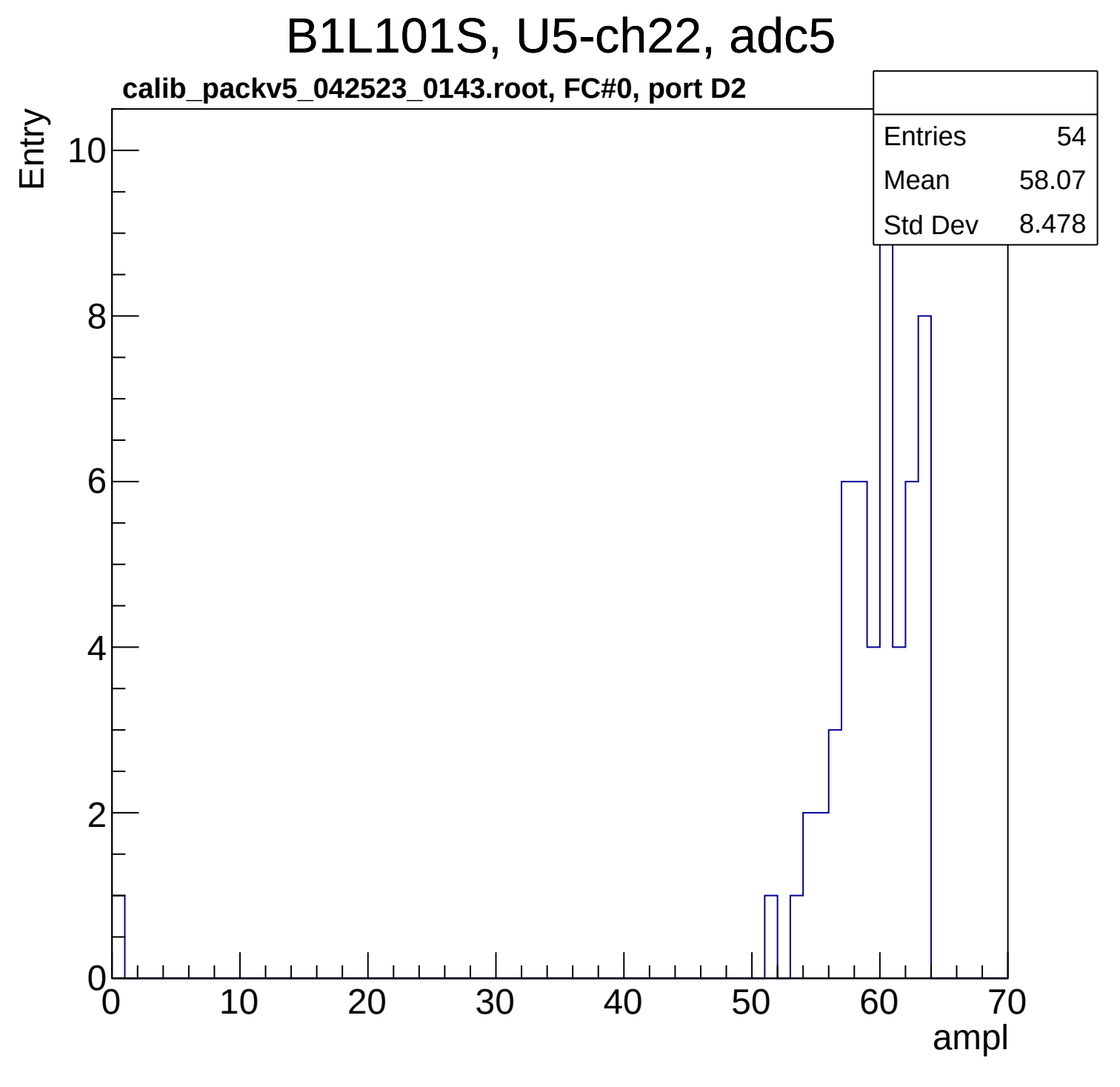
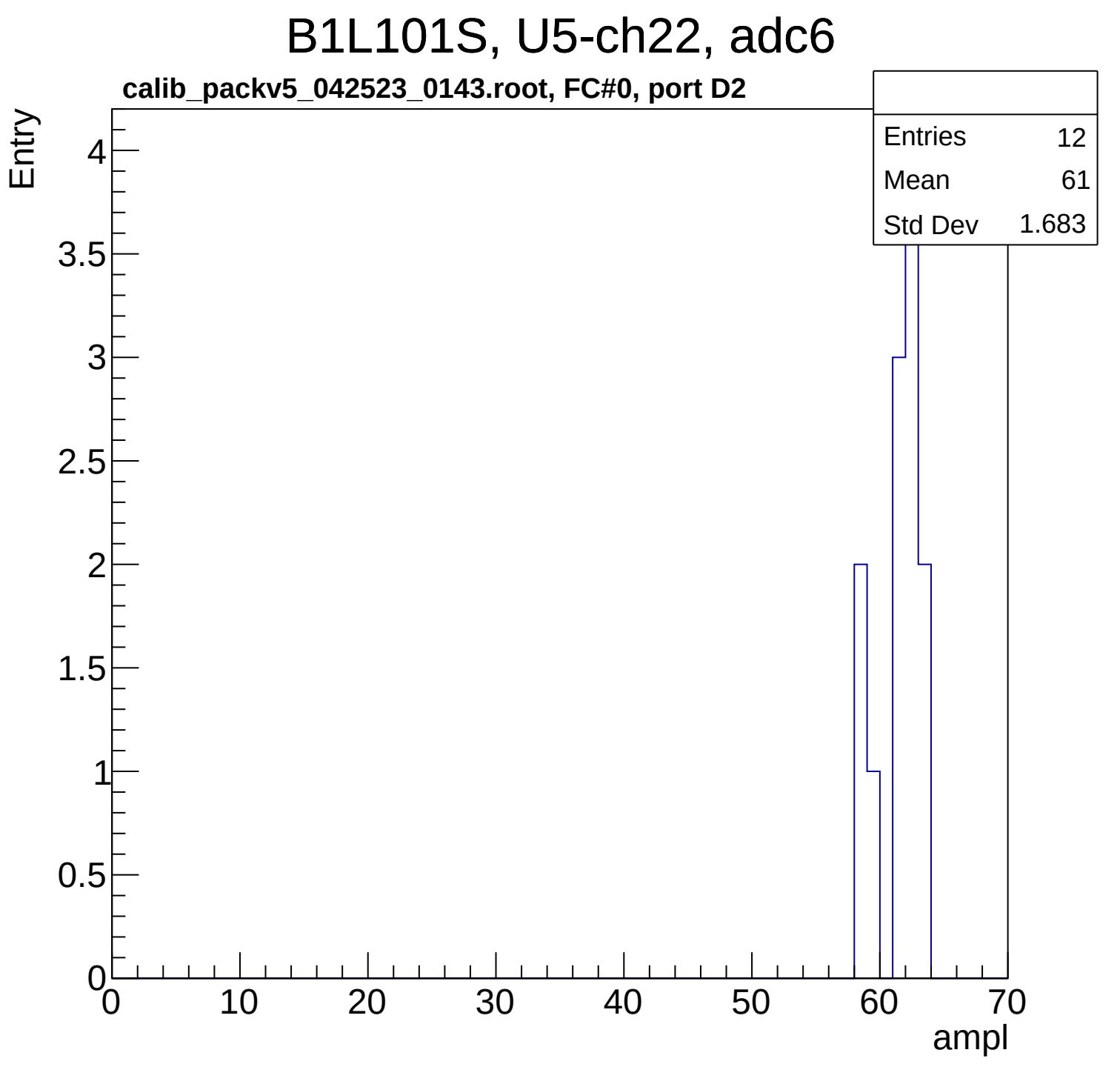

B1L101S, U5-ch22, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 58.07
Std Dev 8.478
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch22, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 12
Mean 61
Std Dev 1.683
Entry
ampl
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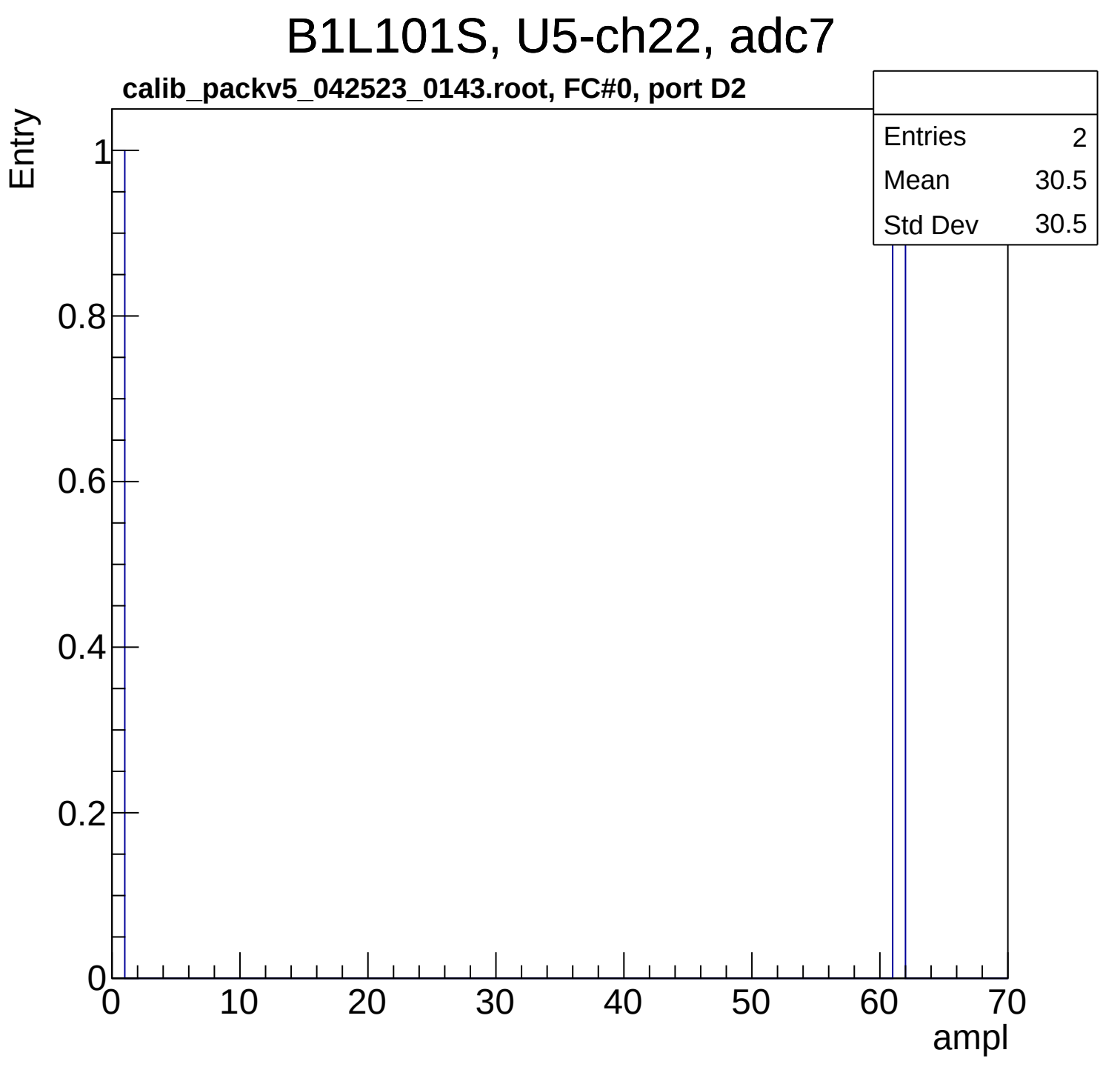
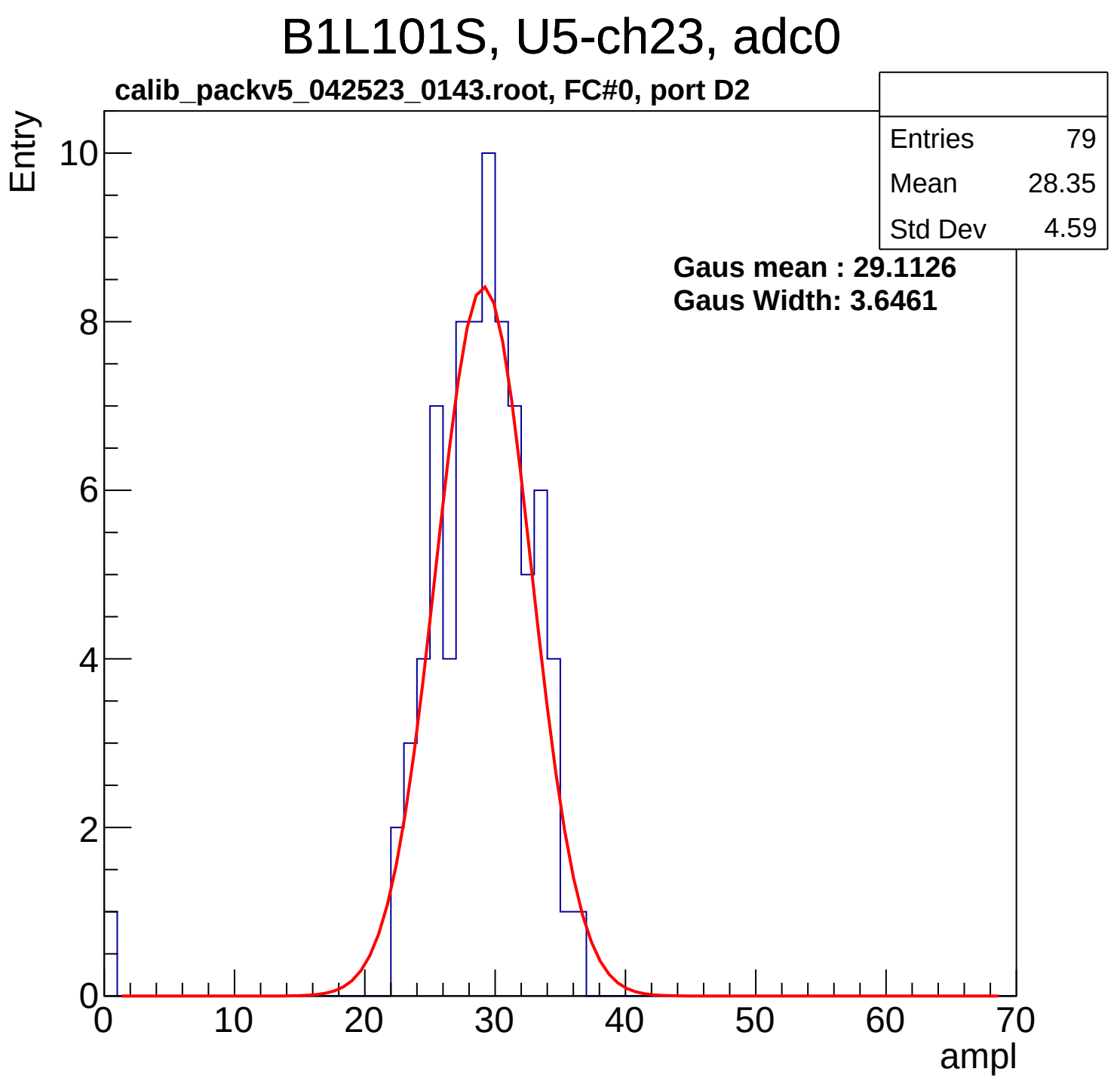
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L101S, U5-ch22, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 30.5
Std Dev 30.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch23, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 28.35
Std Dev 4.59
Gaus mean : 29.1126
Gaus Width: 3.6461
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
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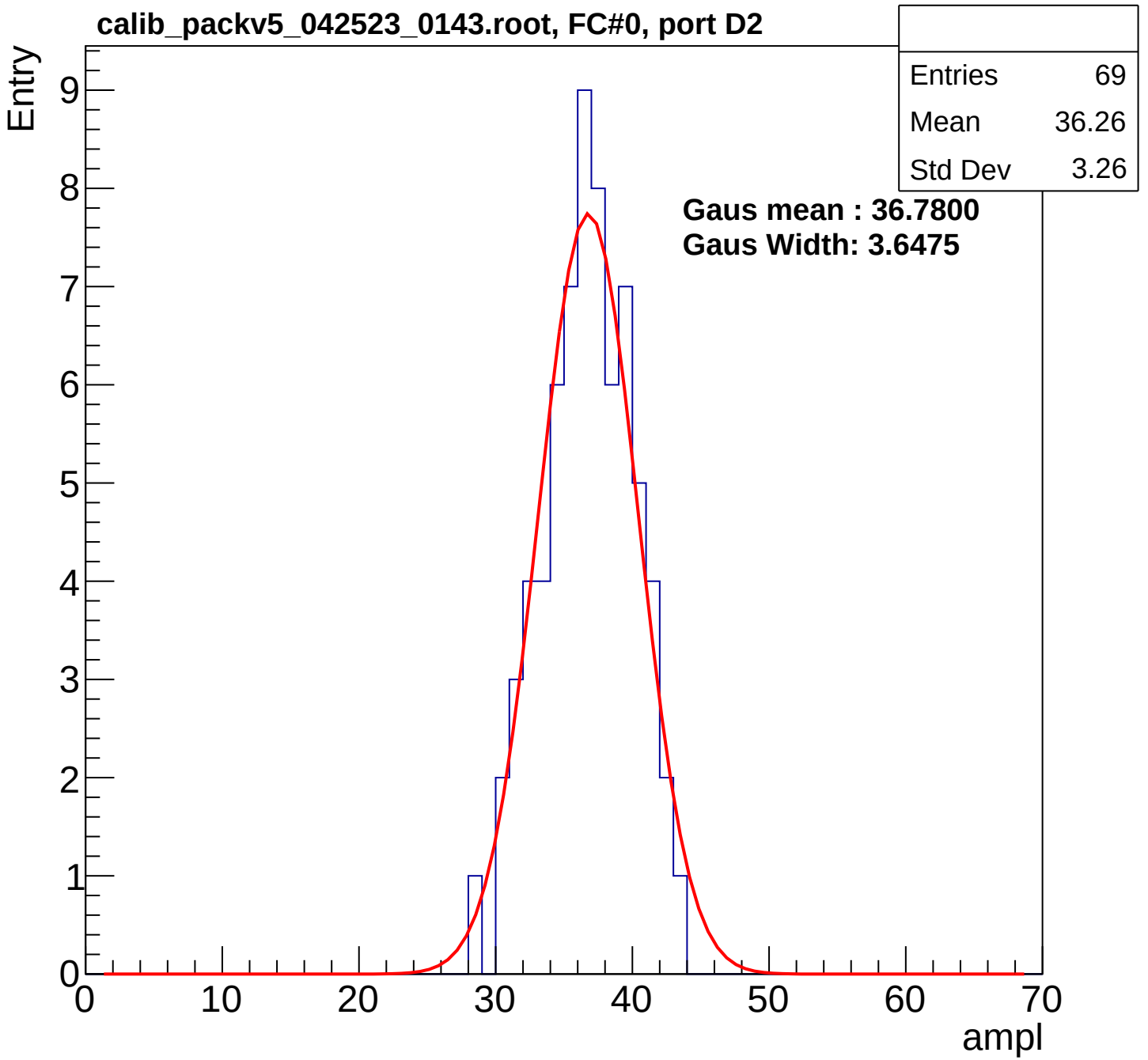
B1L101S, U5-ch23, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 36.26
Std Dev 3.26
Gaus mean : 36.7800
Gaus Width: 3.6475
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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60
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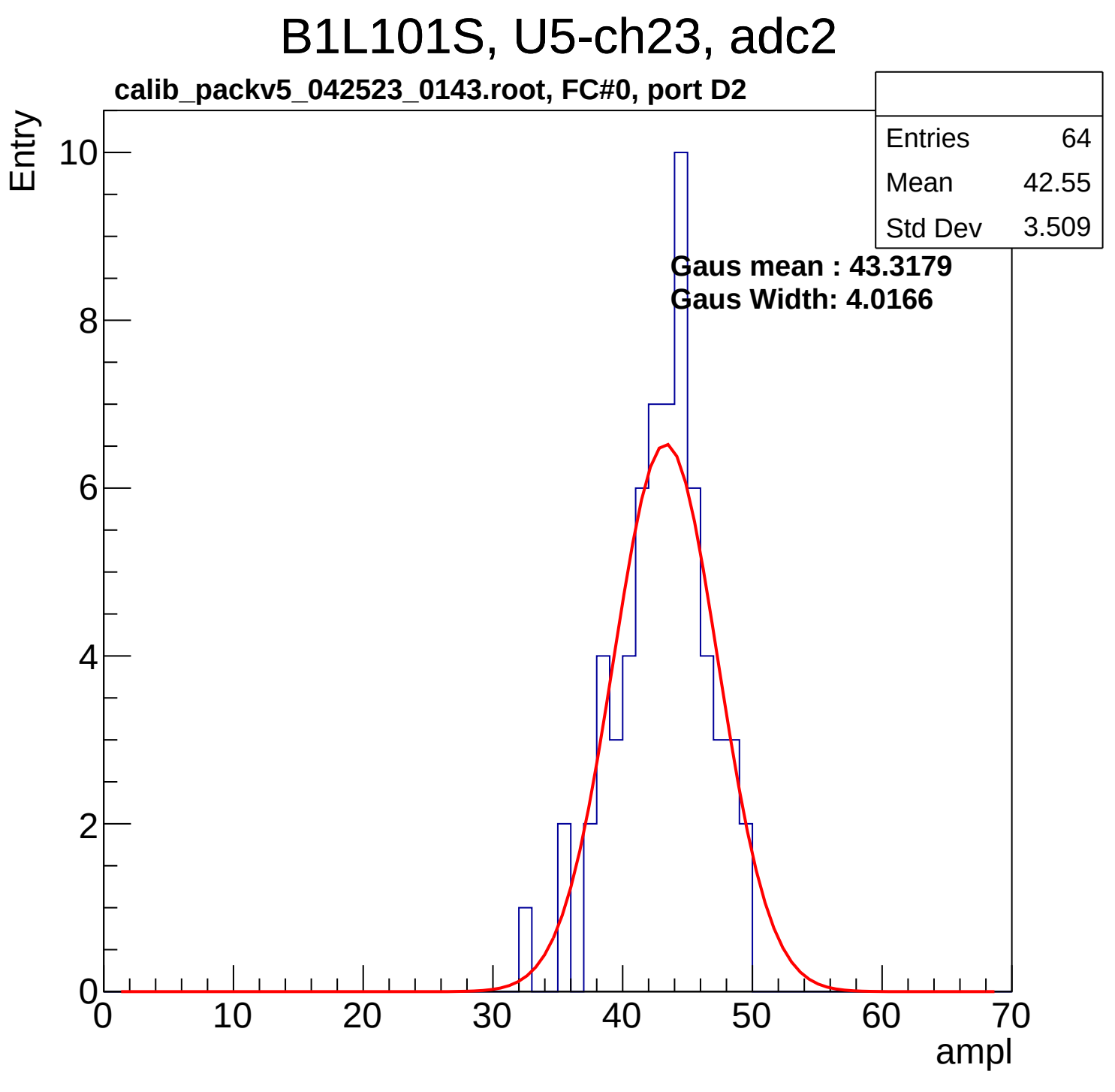
B1L101S, U5-ch23, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 42.55
Std Dev 3.509
Gaus mean : 43.3179
Gaus Width: 4.0166
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
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60
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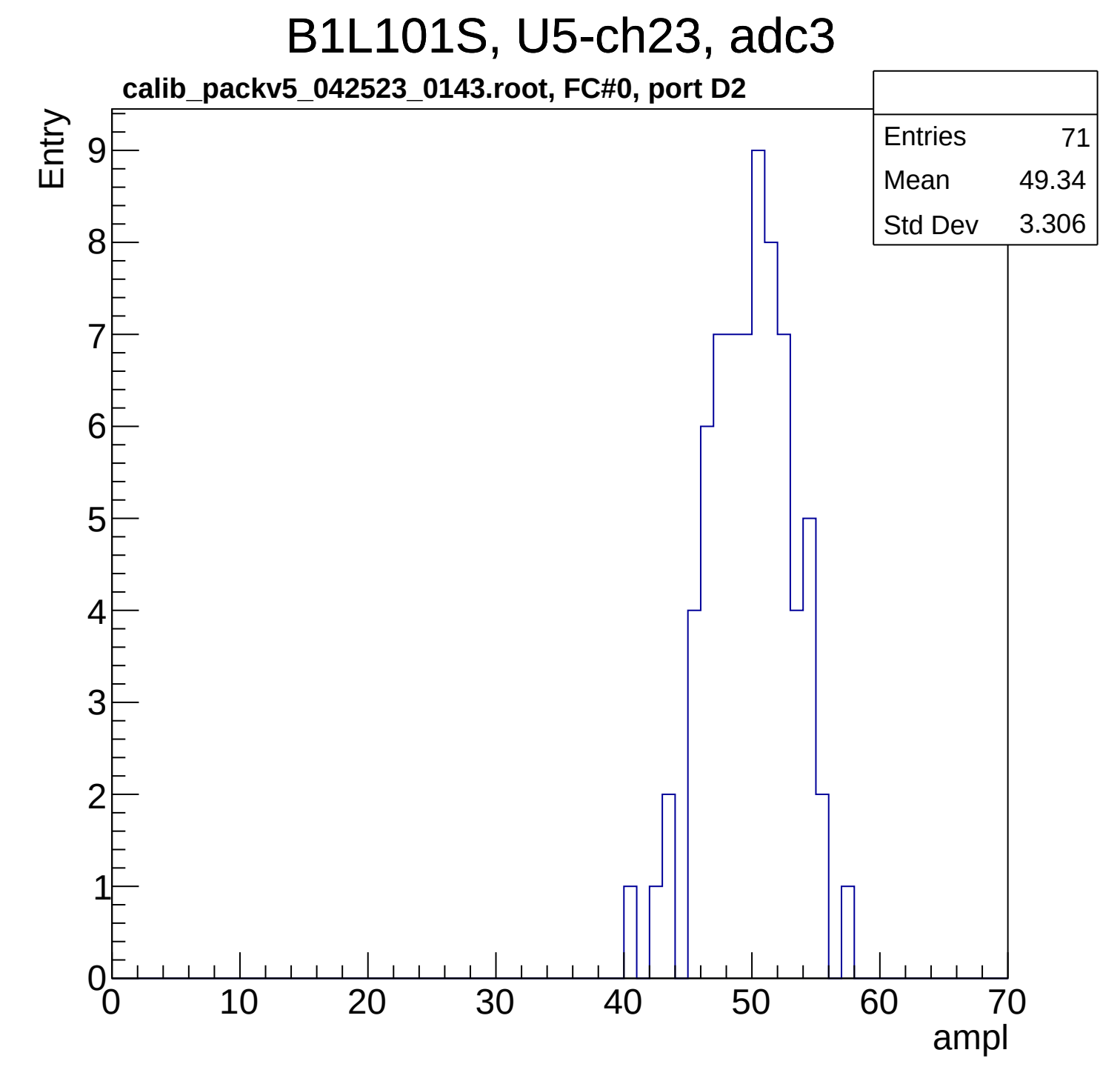
B1L101S, U5-ch23, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 49.34
Std Dev 3.306
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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60
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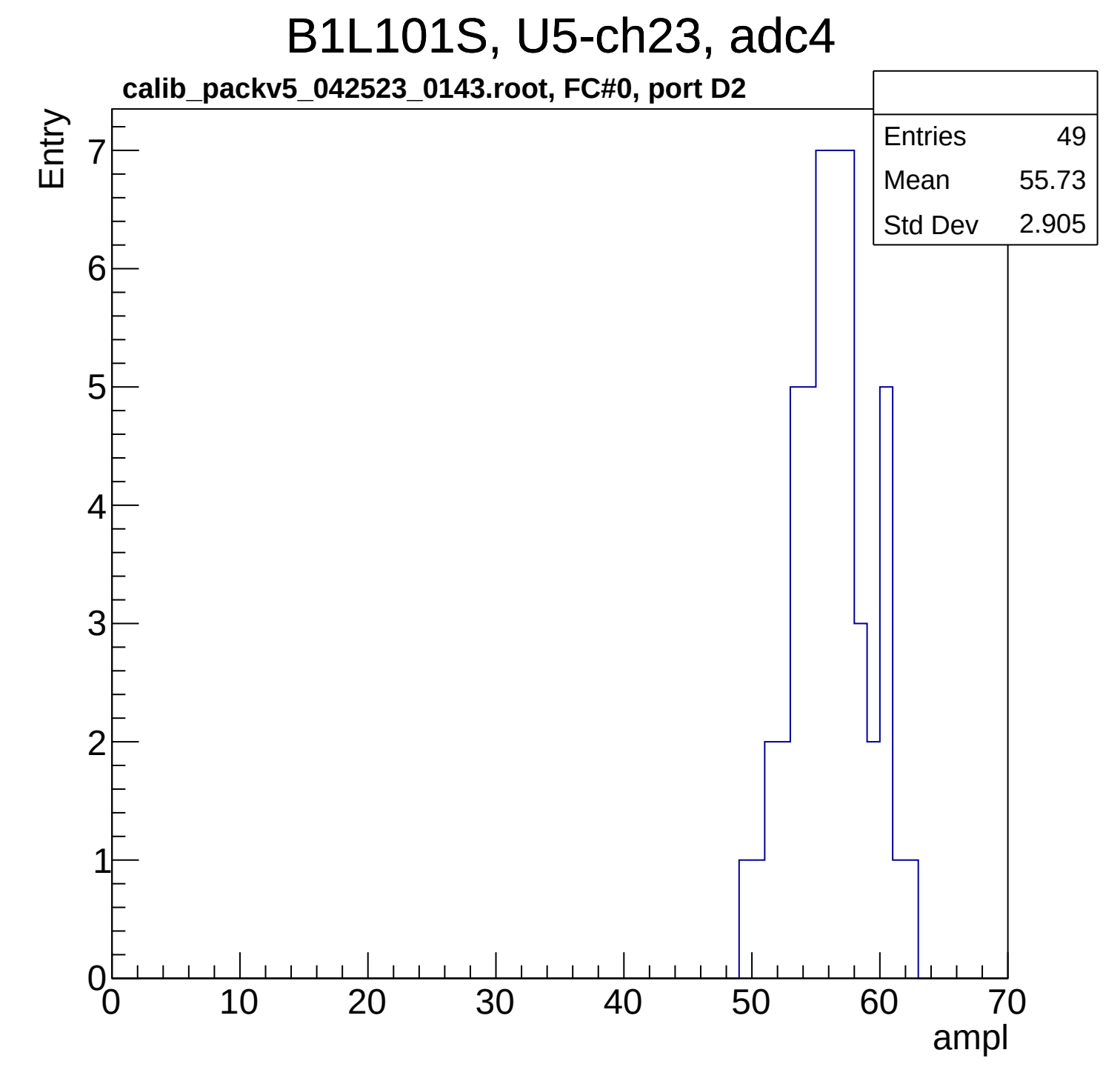
B1L101S, U5-ch23, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 55.73
Std Dev 2.905
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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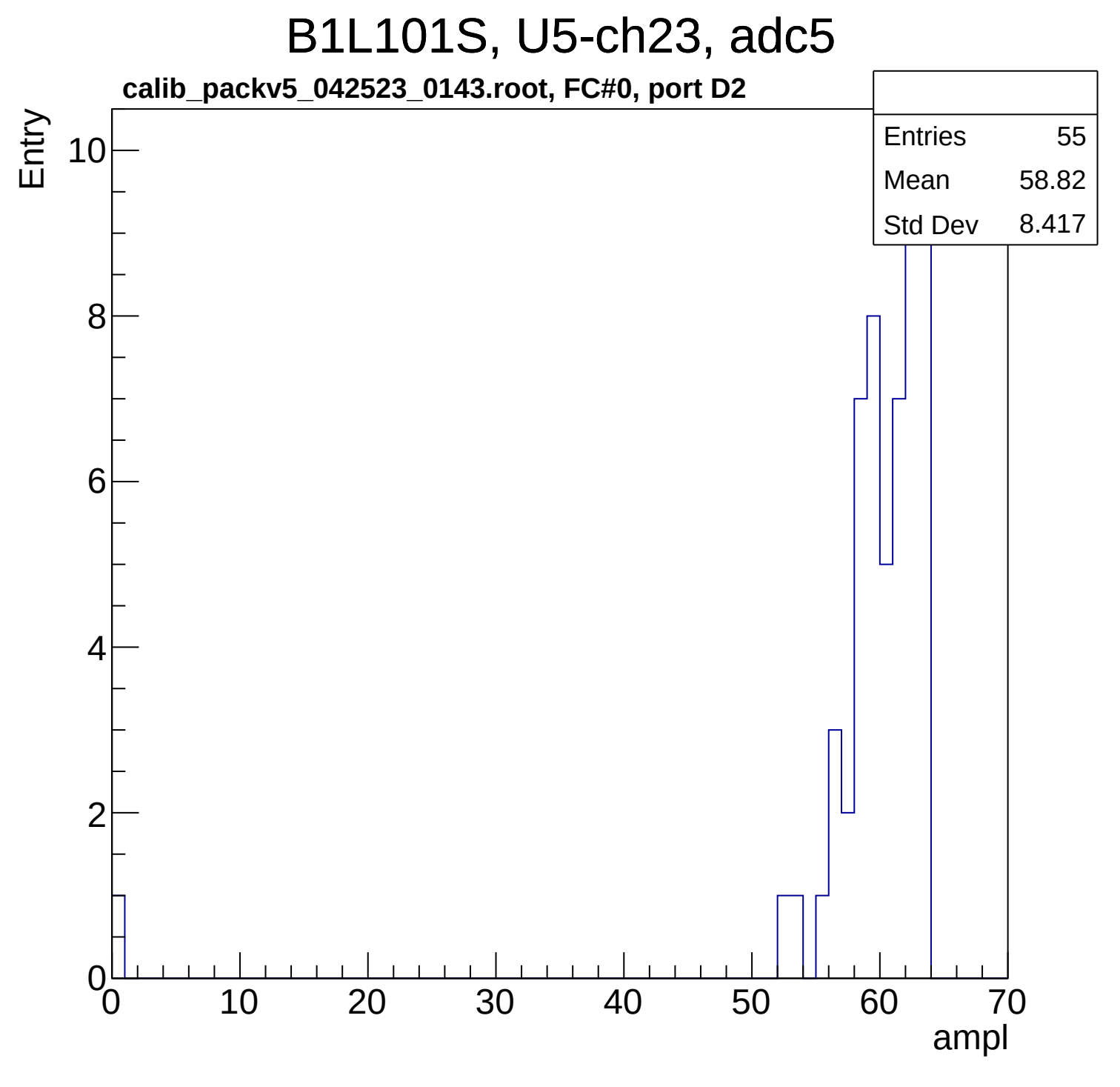
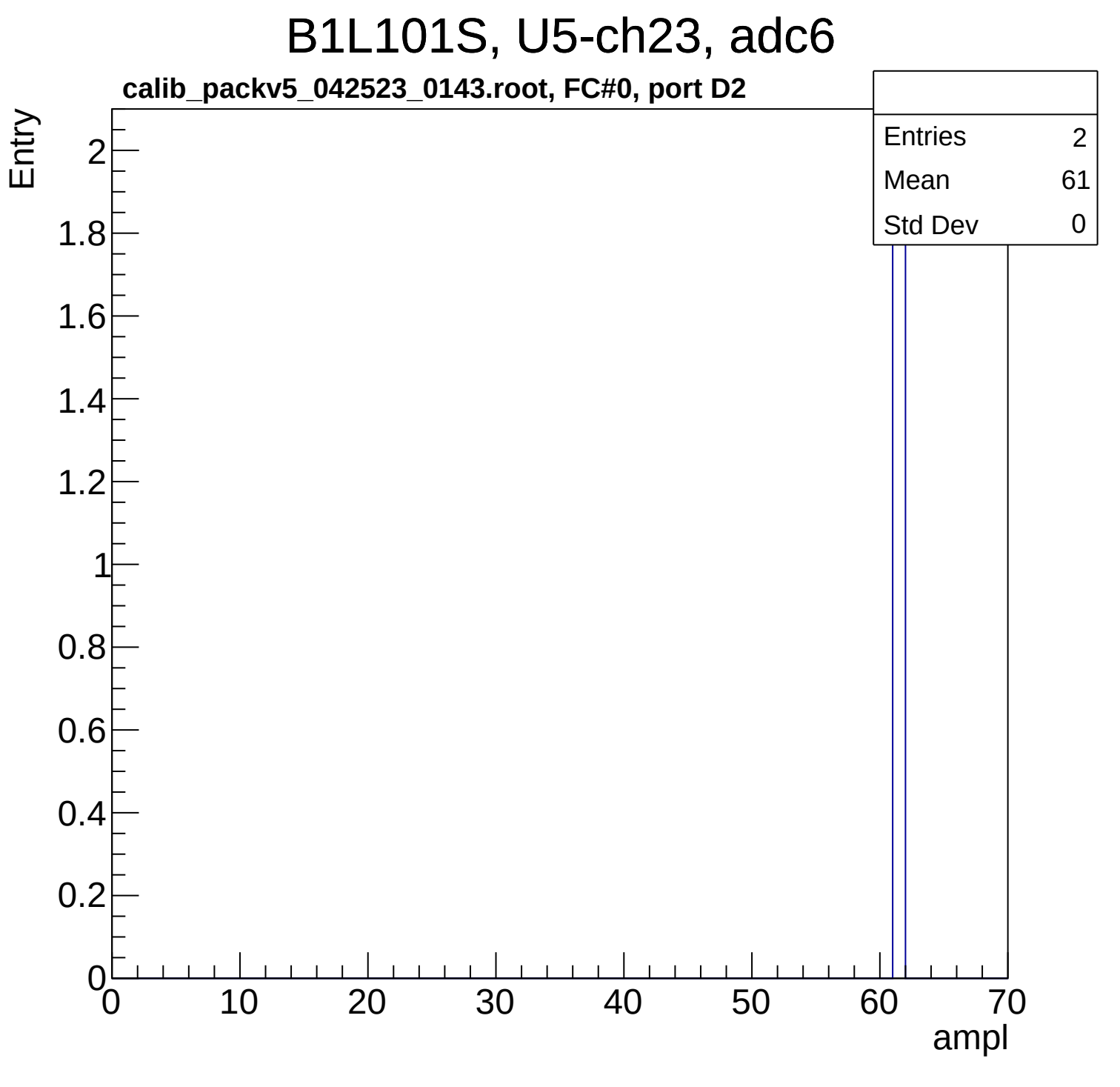

B1L101S, U5-ch23, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 58.82
Std Dev 8.417
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch23, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 61
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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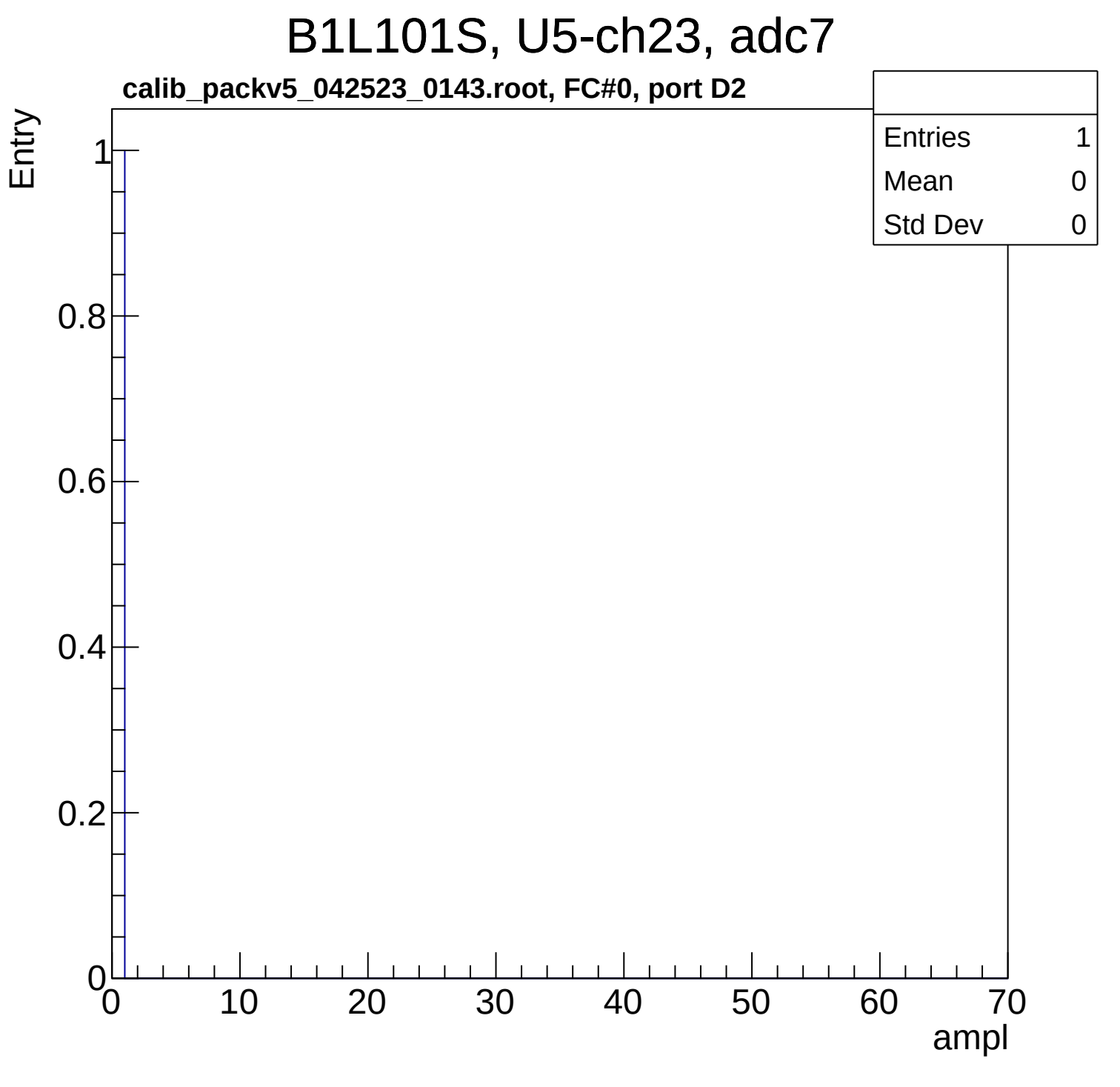
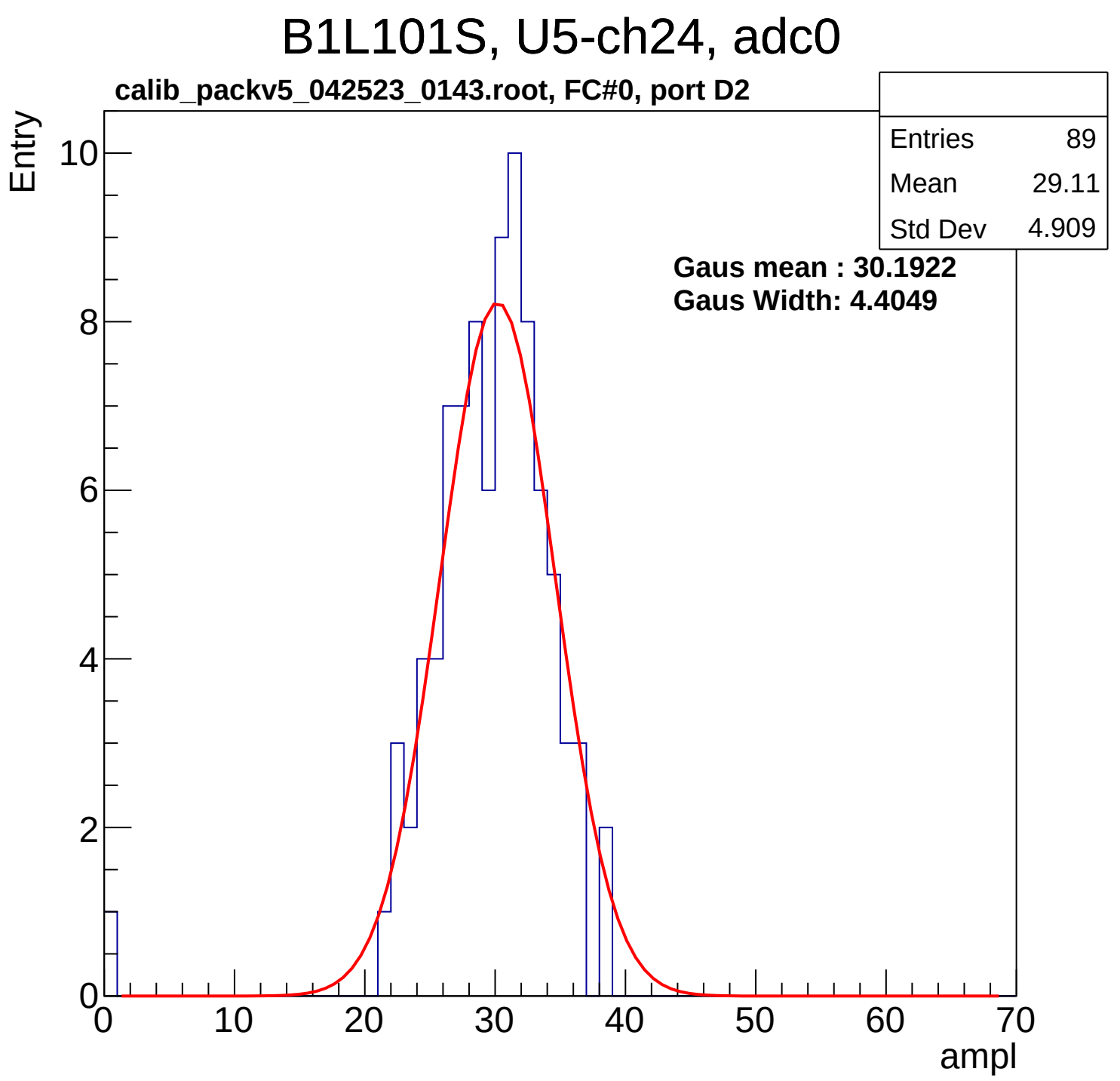
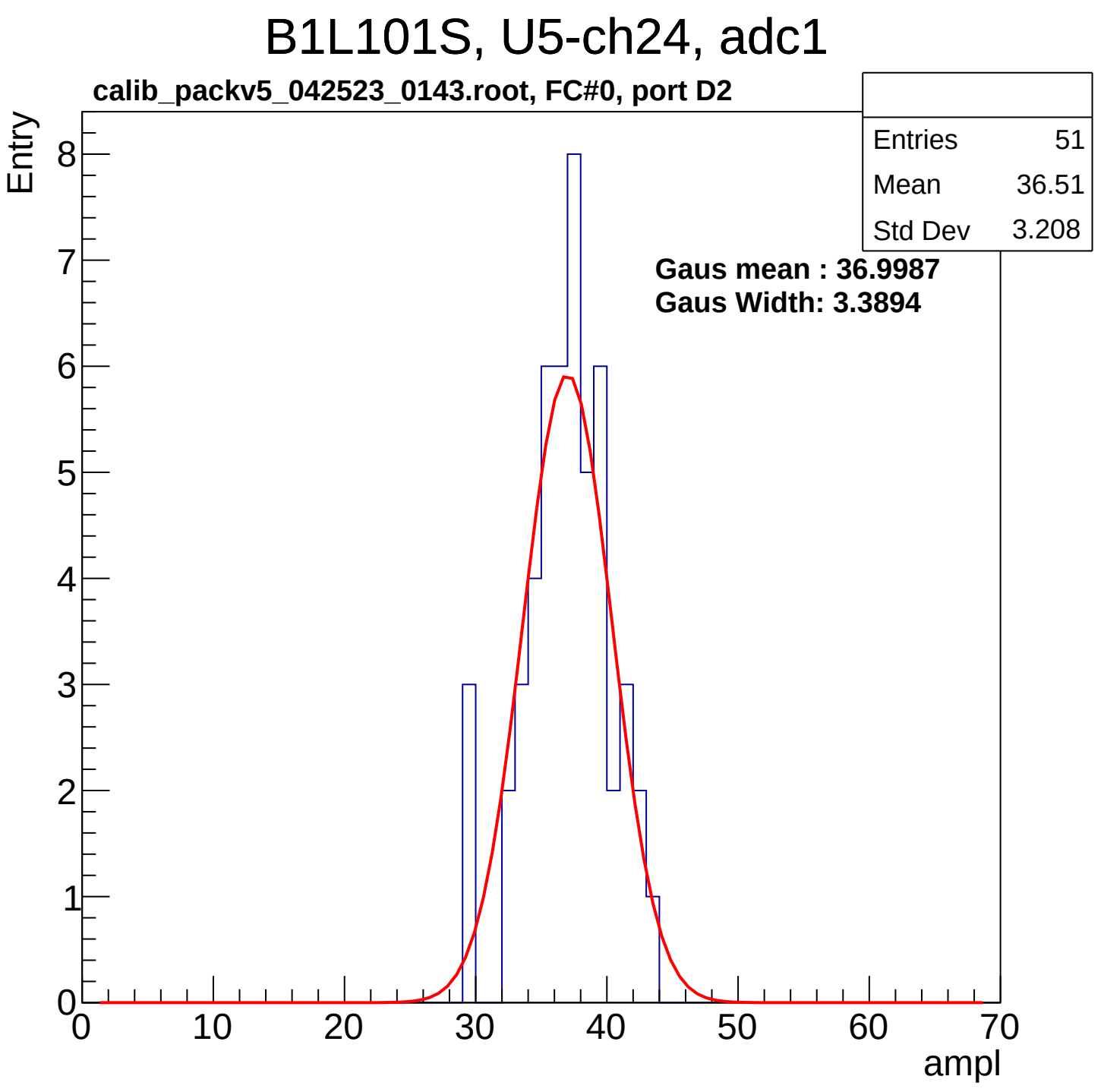
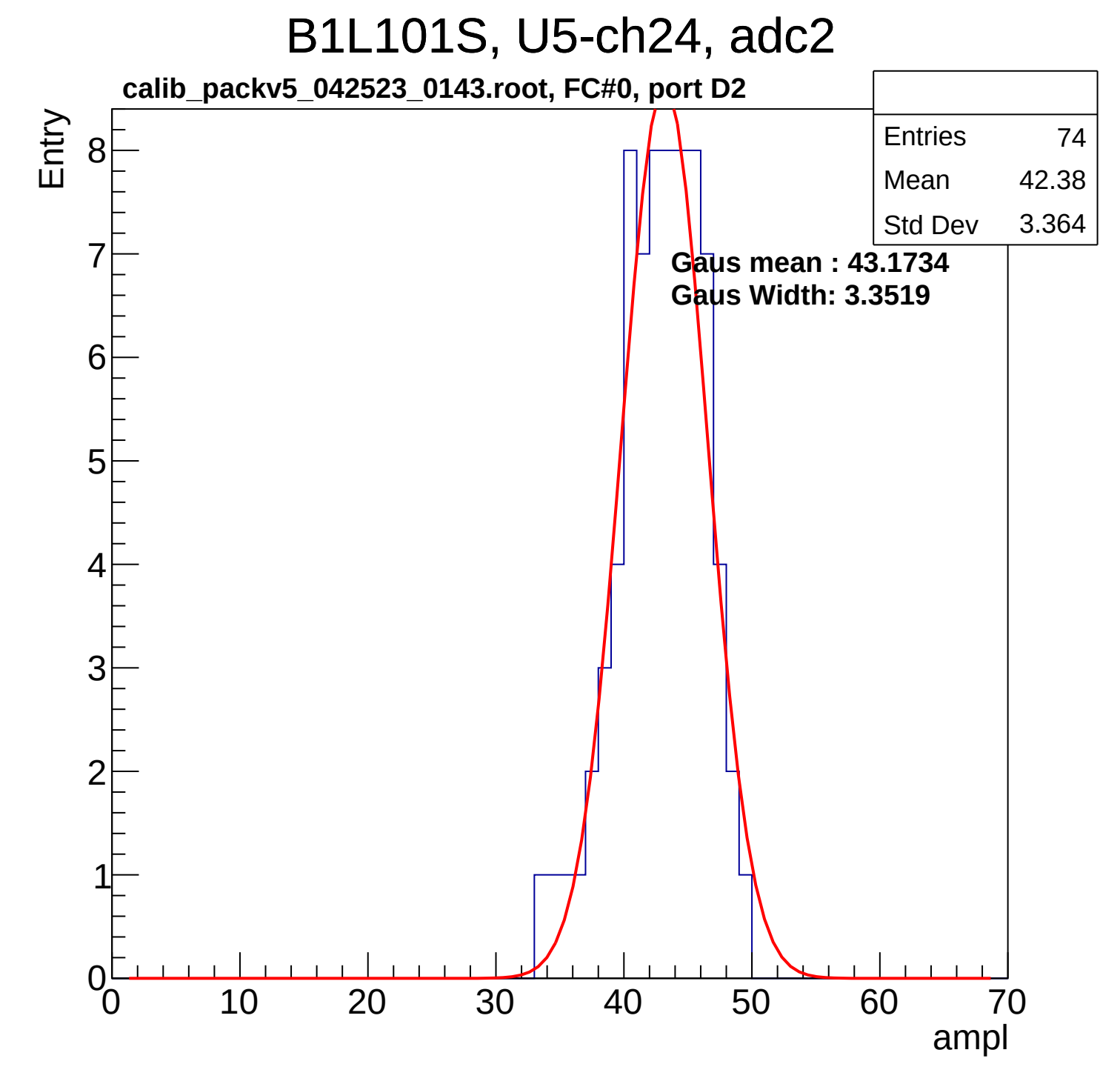

B1L101S, U5-ch23, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch24, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 89
Mean 29.11
Std Dev 4.909
Gaus mean : 30.1922
Gaus Width: 4.4049
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch24, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 36.51
Std Dev 3.208
Gaus mean : 36.9987
Gaus Width: 3.3894
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch24, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 42.38
Std Dev 3.364
Gaus mean : 43.1734
Gaus Width: 3.3519
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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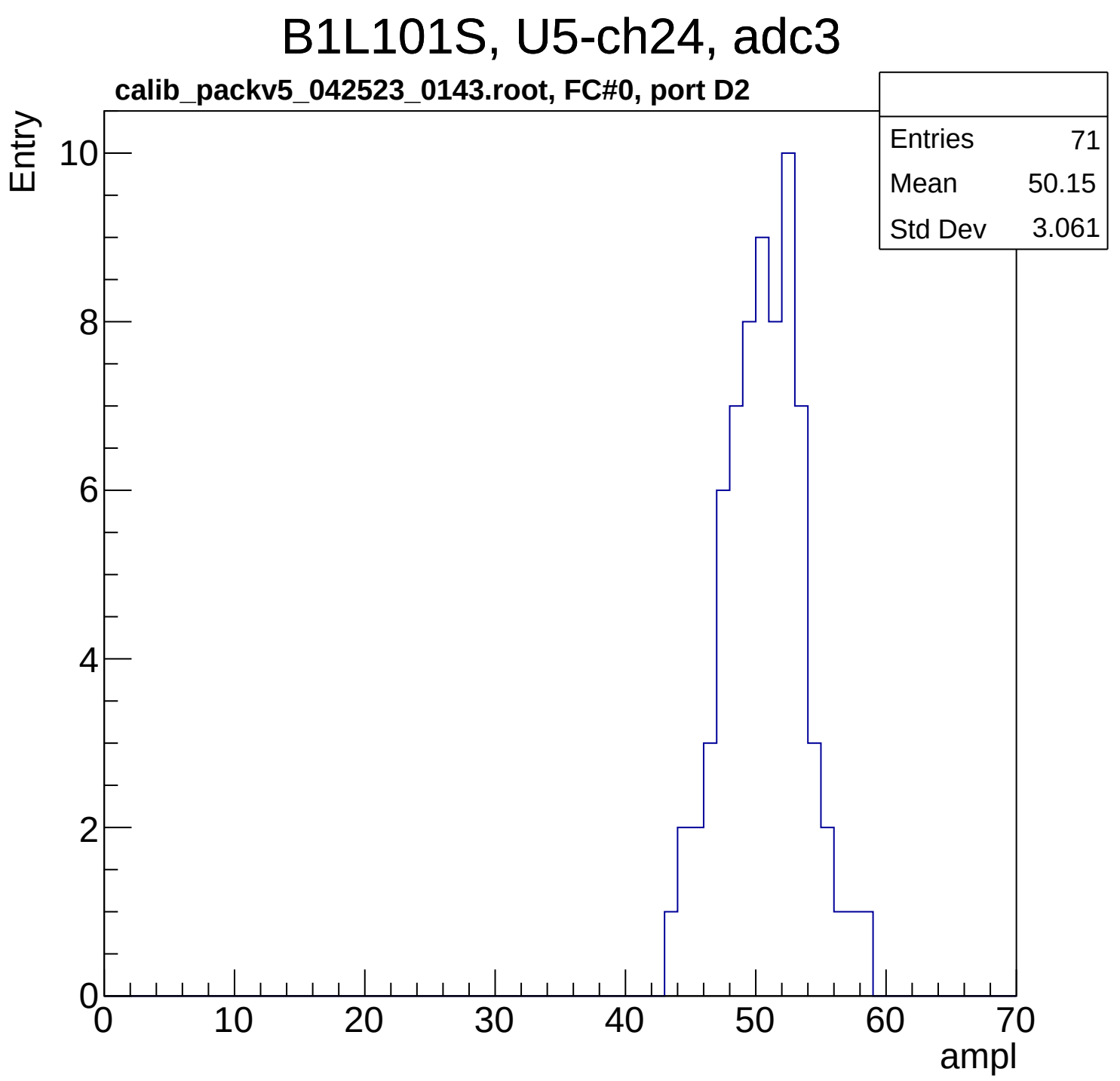
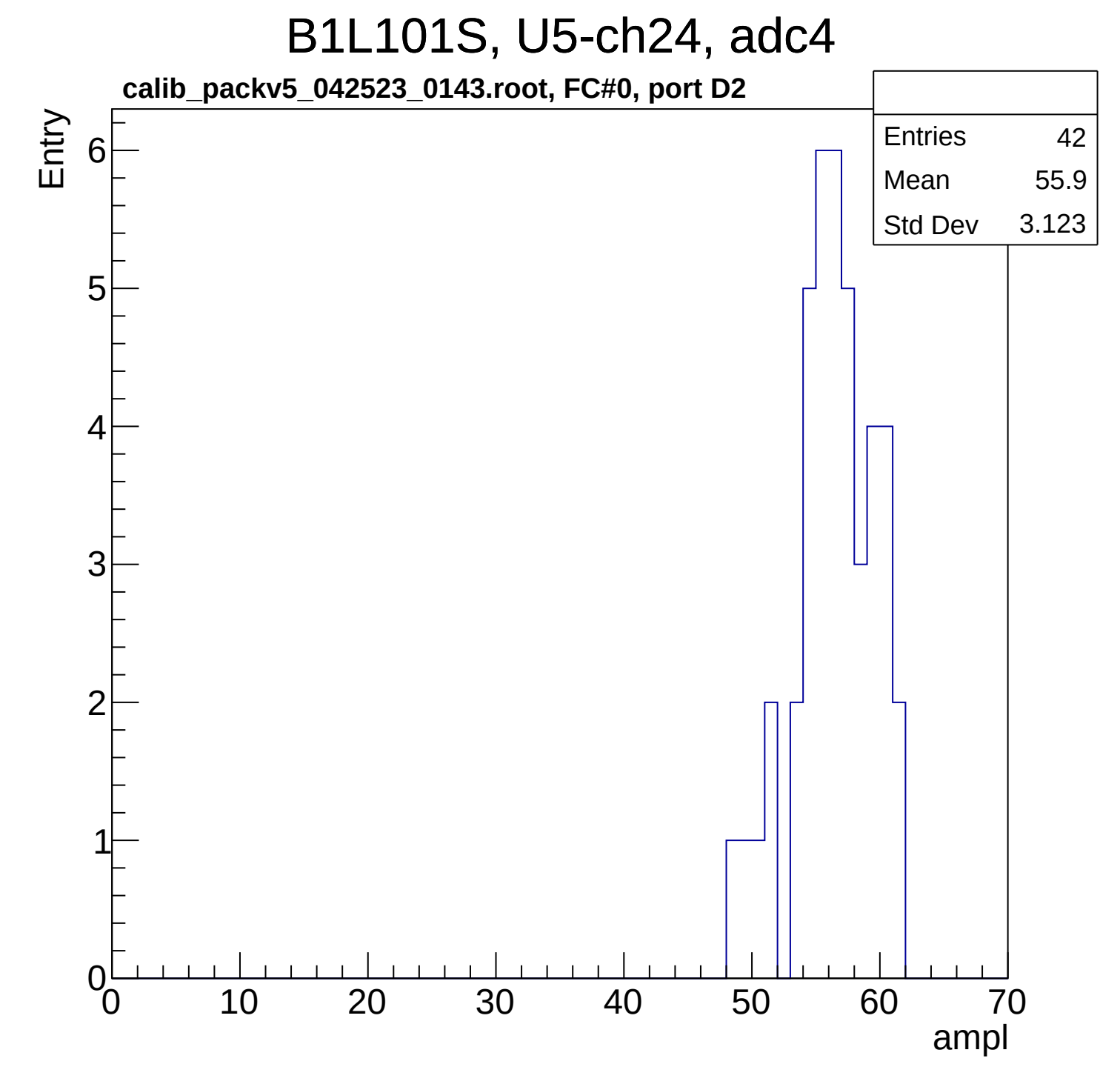
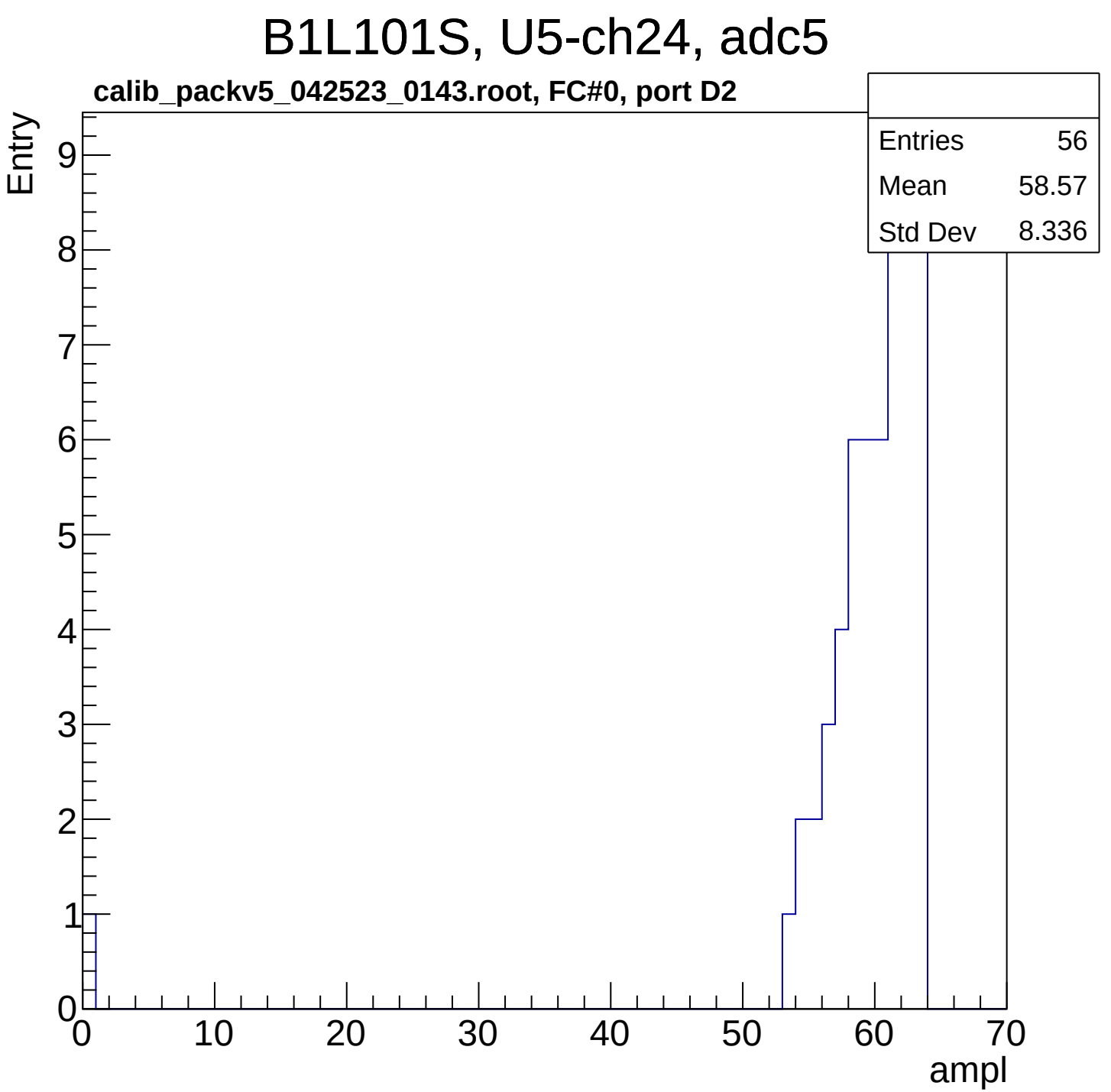

B1L101S, U5-ch24, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 50.15
Std Dev 3.061
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch24, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 55.9
Std Dev 3.123
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch24, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 58.57
Std Dev 8.336
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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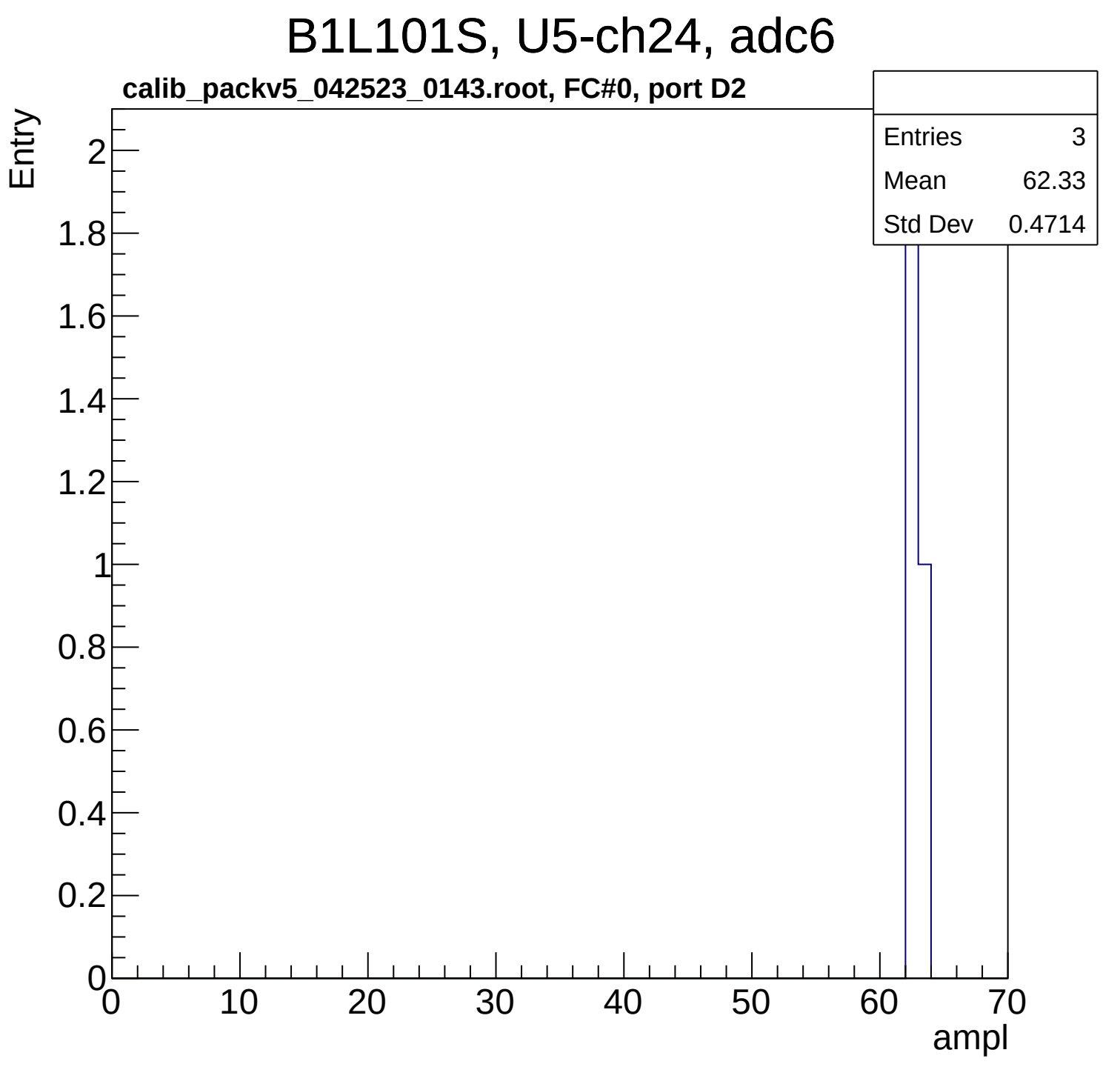
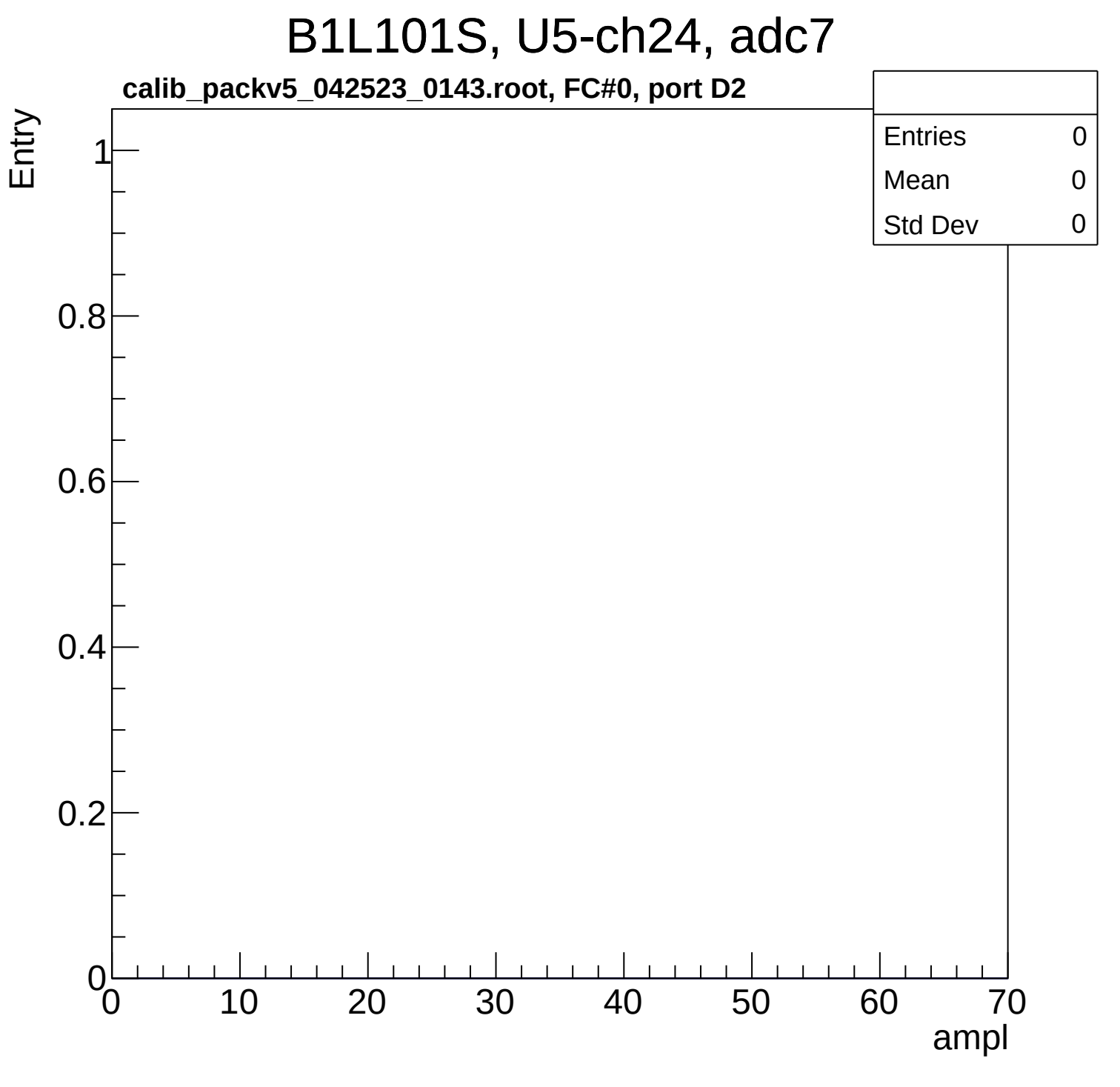

B1L101S, U5-ch24, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U5-ch24, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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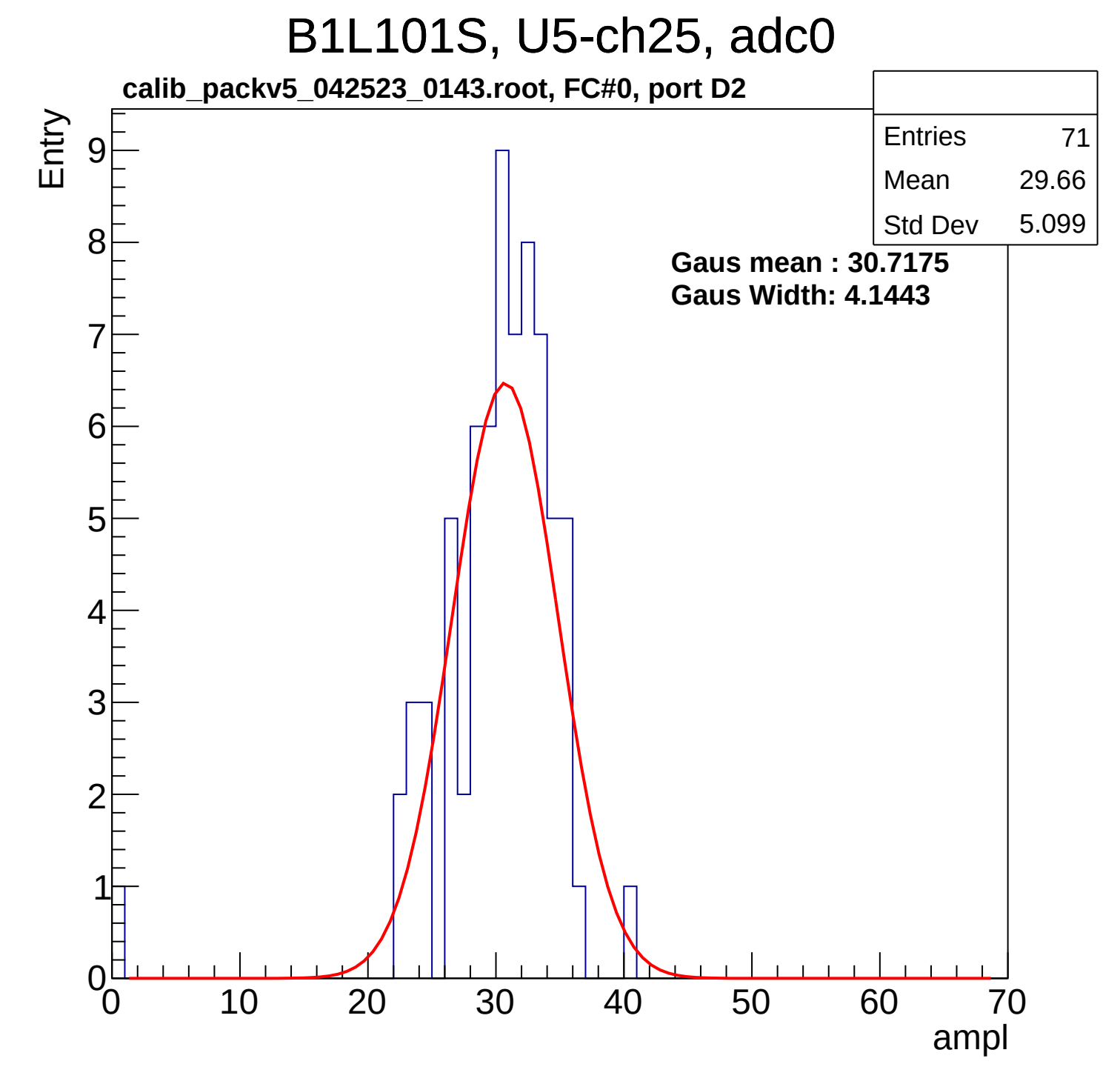
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch25, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 29.66
Std Dev 5.099
Gaus mean : 30.7175
Gaus Width: 4.1443
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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40
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60
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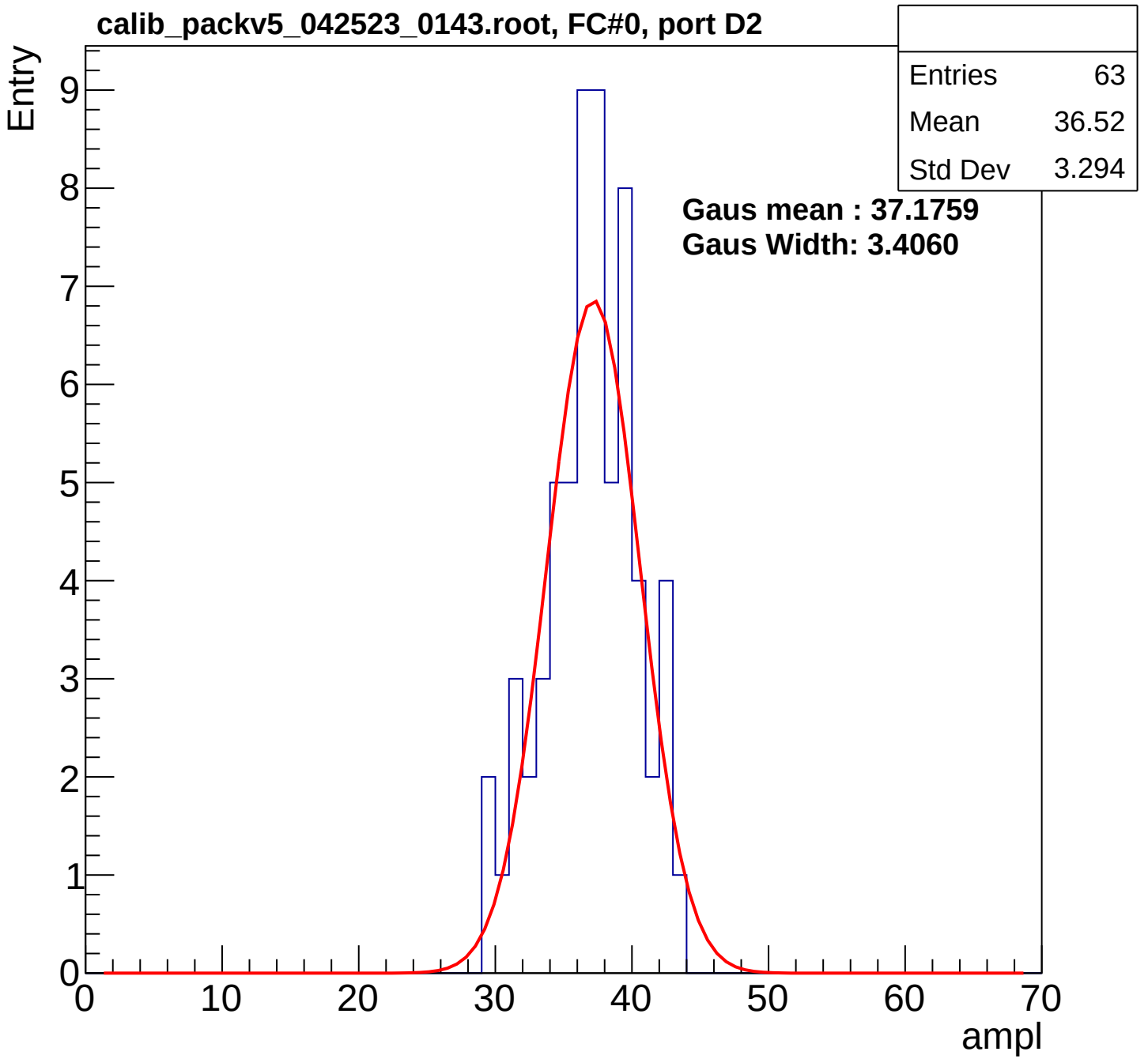
B1L101S, U5-ch25, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 36.52
Std Dev 3.294
Gaus mean : 37.1759
Gaus Width: 3.4060
Entry
ampl
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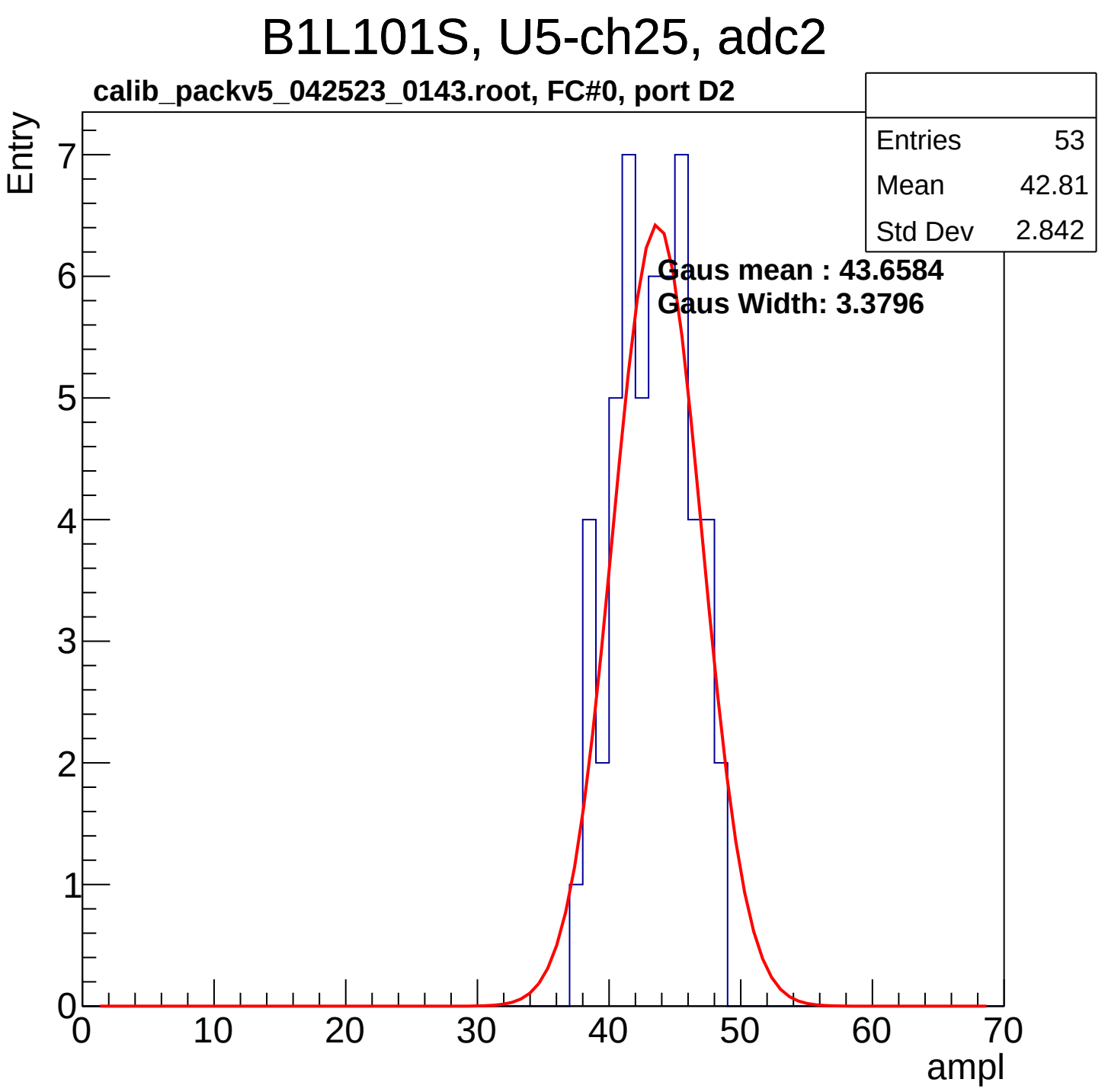
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch25, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 42.81
Std Dev 2.842
Gaus mean : 43.6584
Gaus Width: 3.3796
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
50
60
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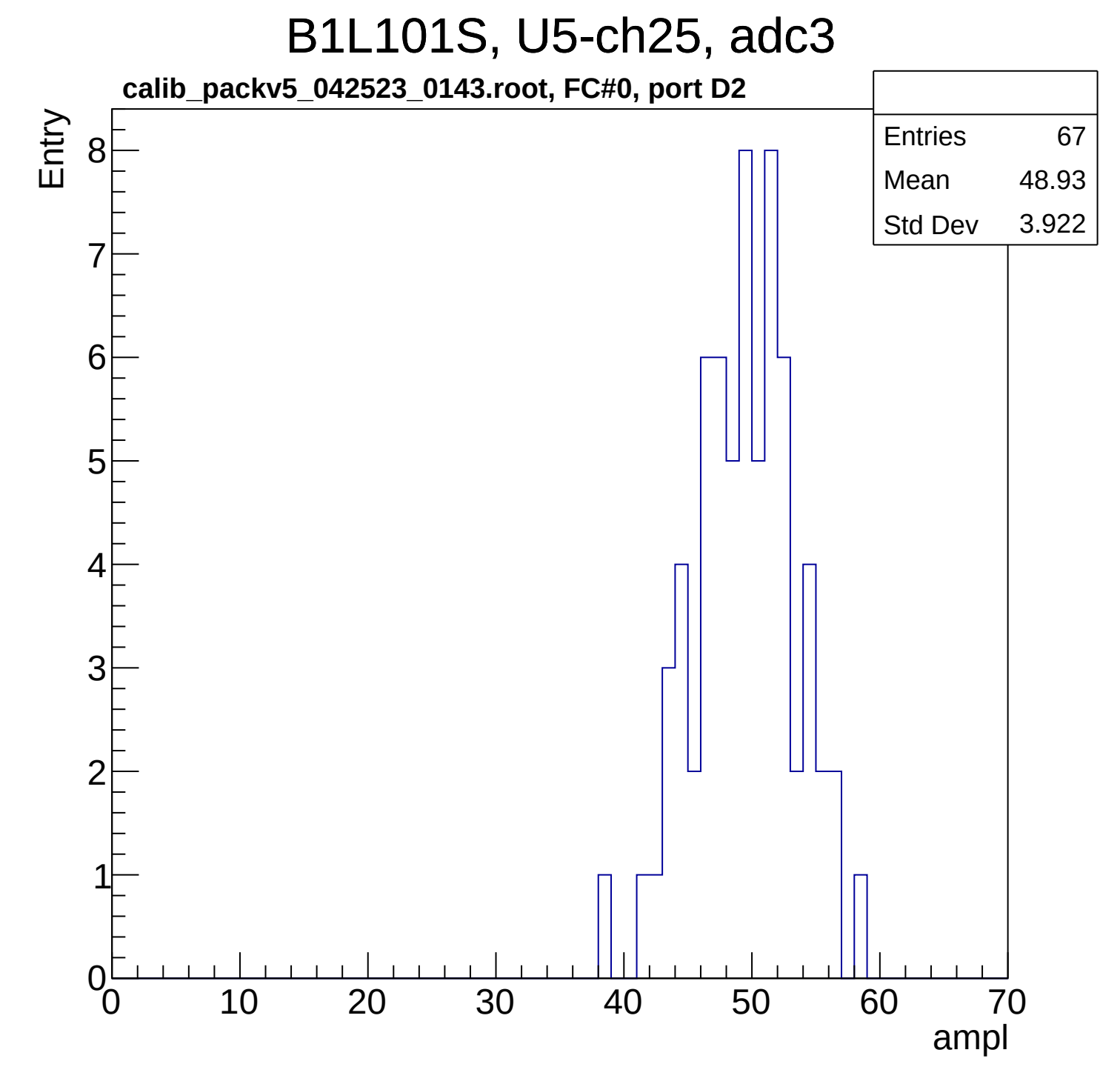
B1L101S, U5-ch25, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 48.93
Std Dev 3.922
Entry
ampl
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2
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5
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0
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60
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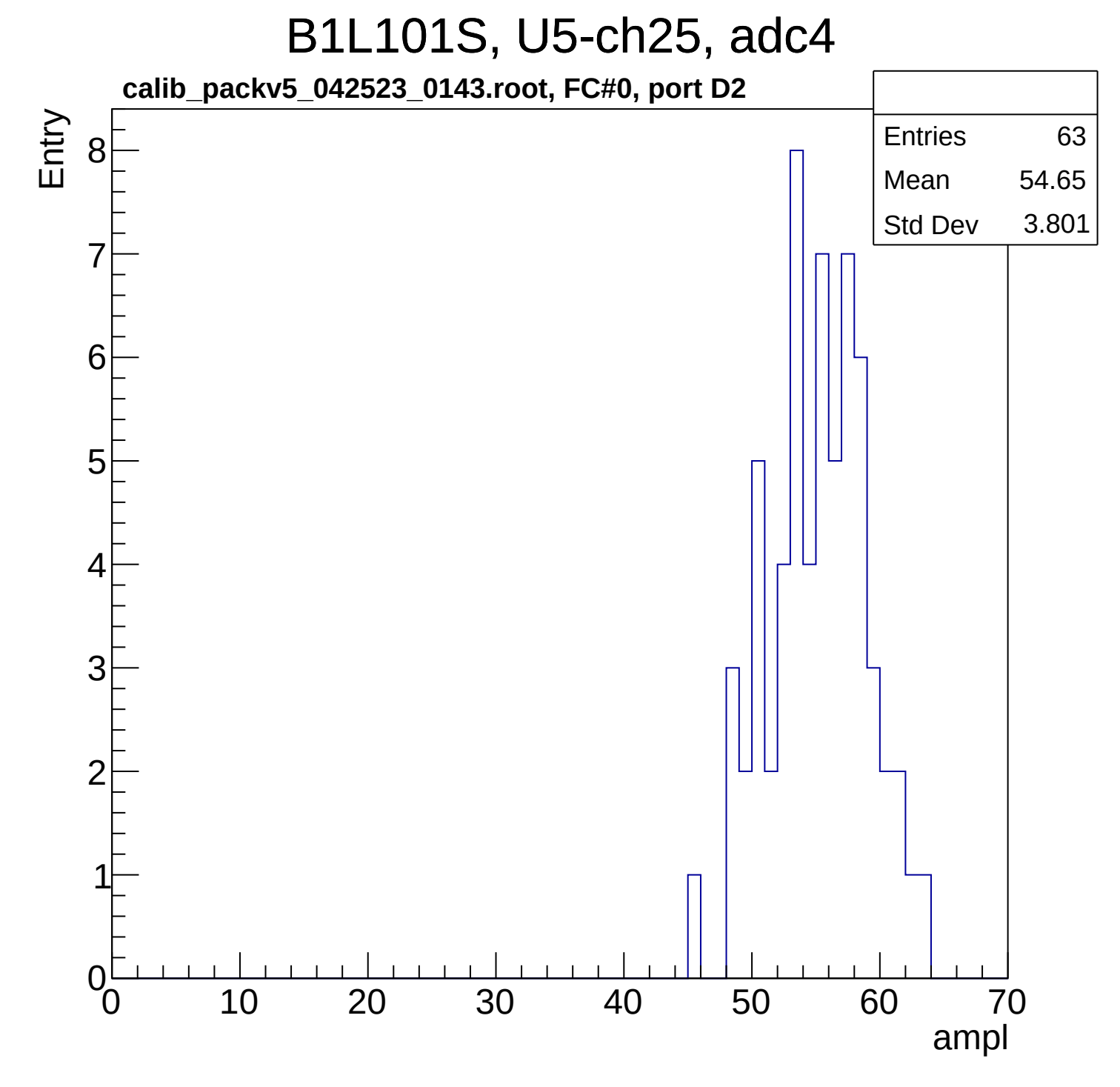
B1L101S, U5-ch25, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 54.65
Std Dev 3.801
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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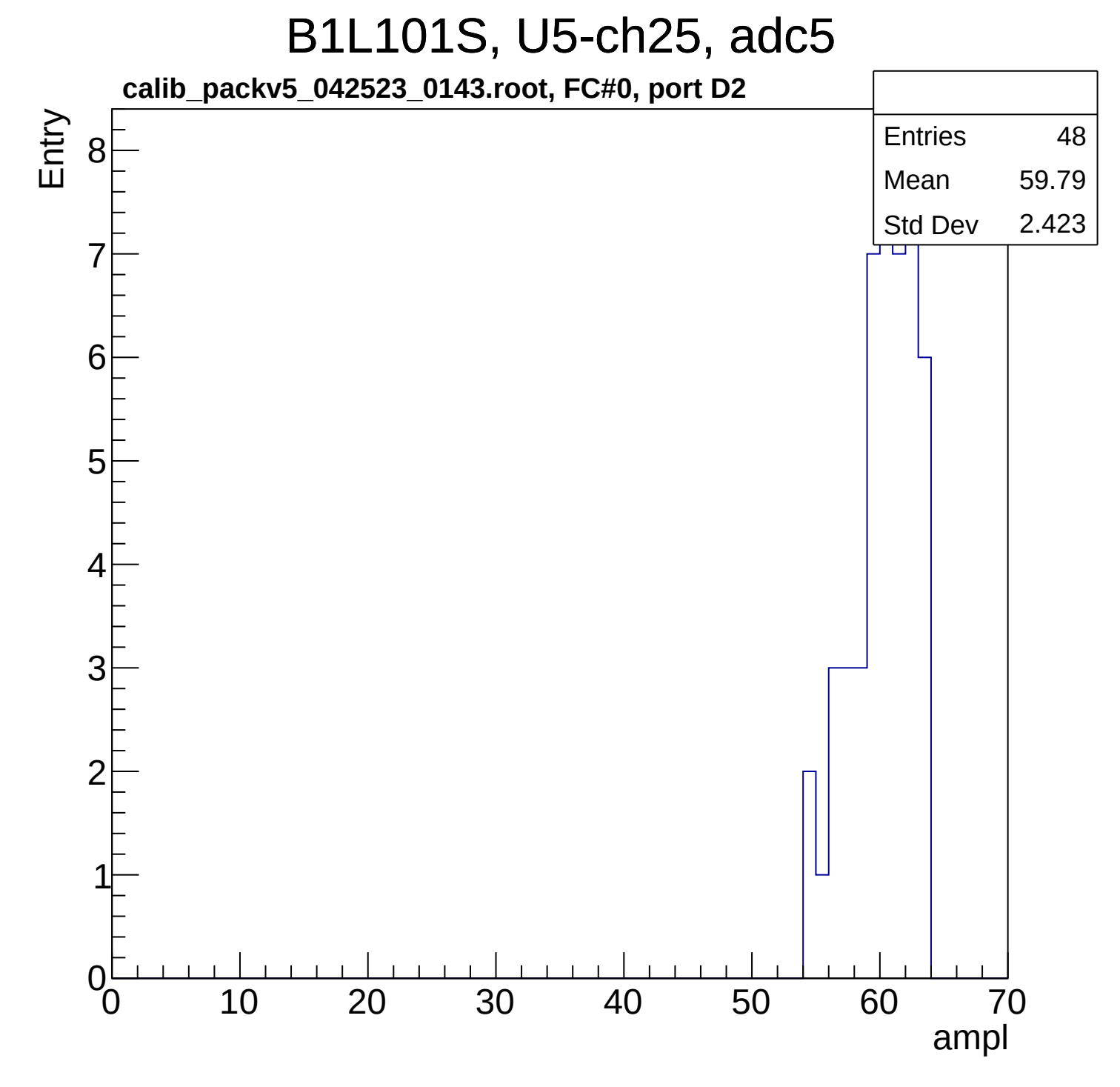
B1L101S, U5-ch25, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 59.79
Std Dev 2.423
Entry
ampl
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1
2
3
4
5
6
7
8
0
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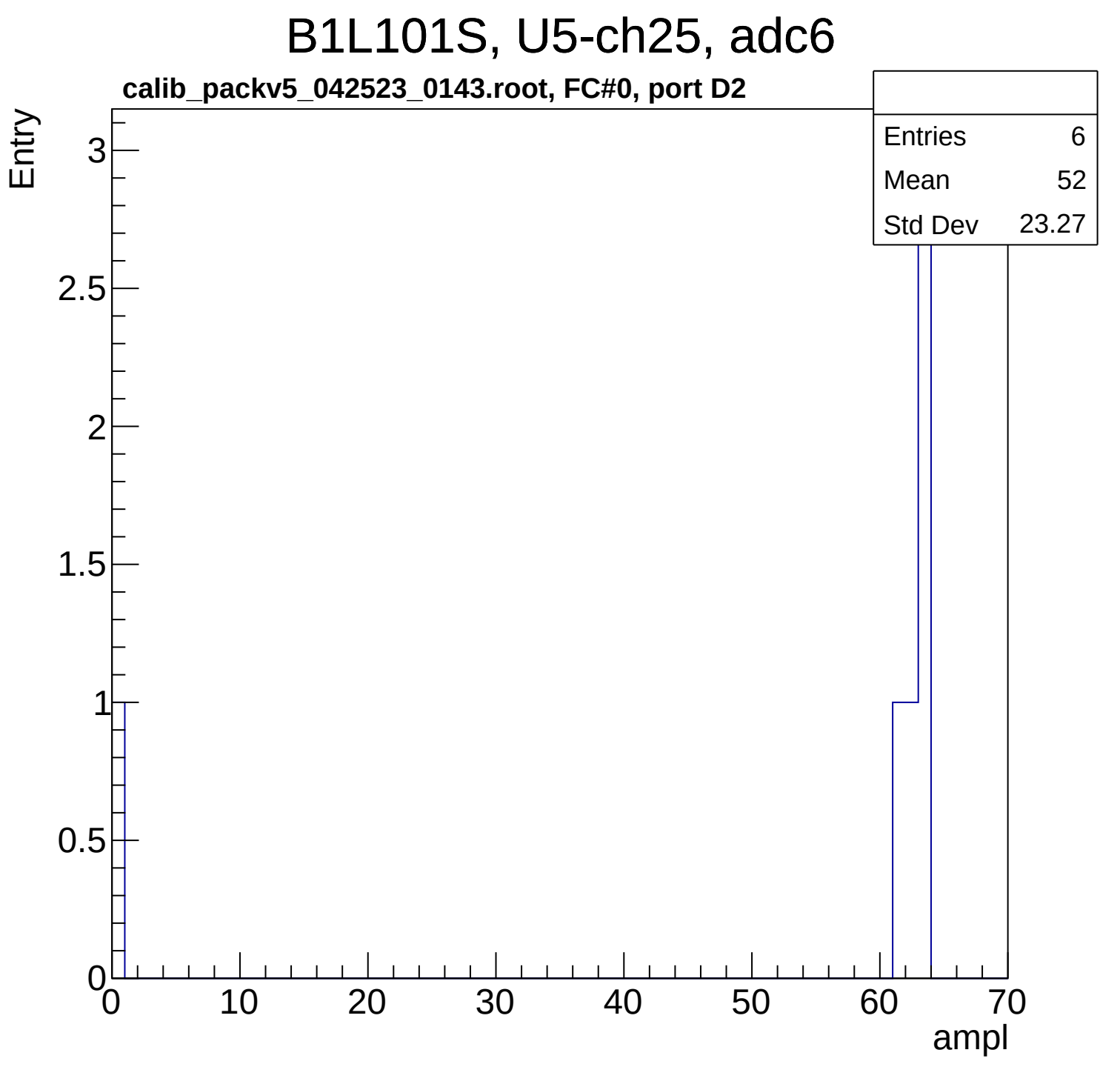
40
50
60
70


B1L101S, U5-ch25, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 52
Std Dev 23.27
Entry
ampl
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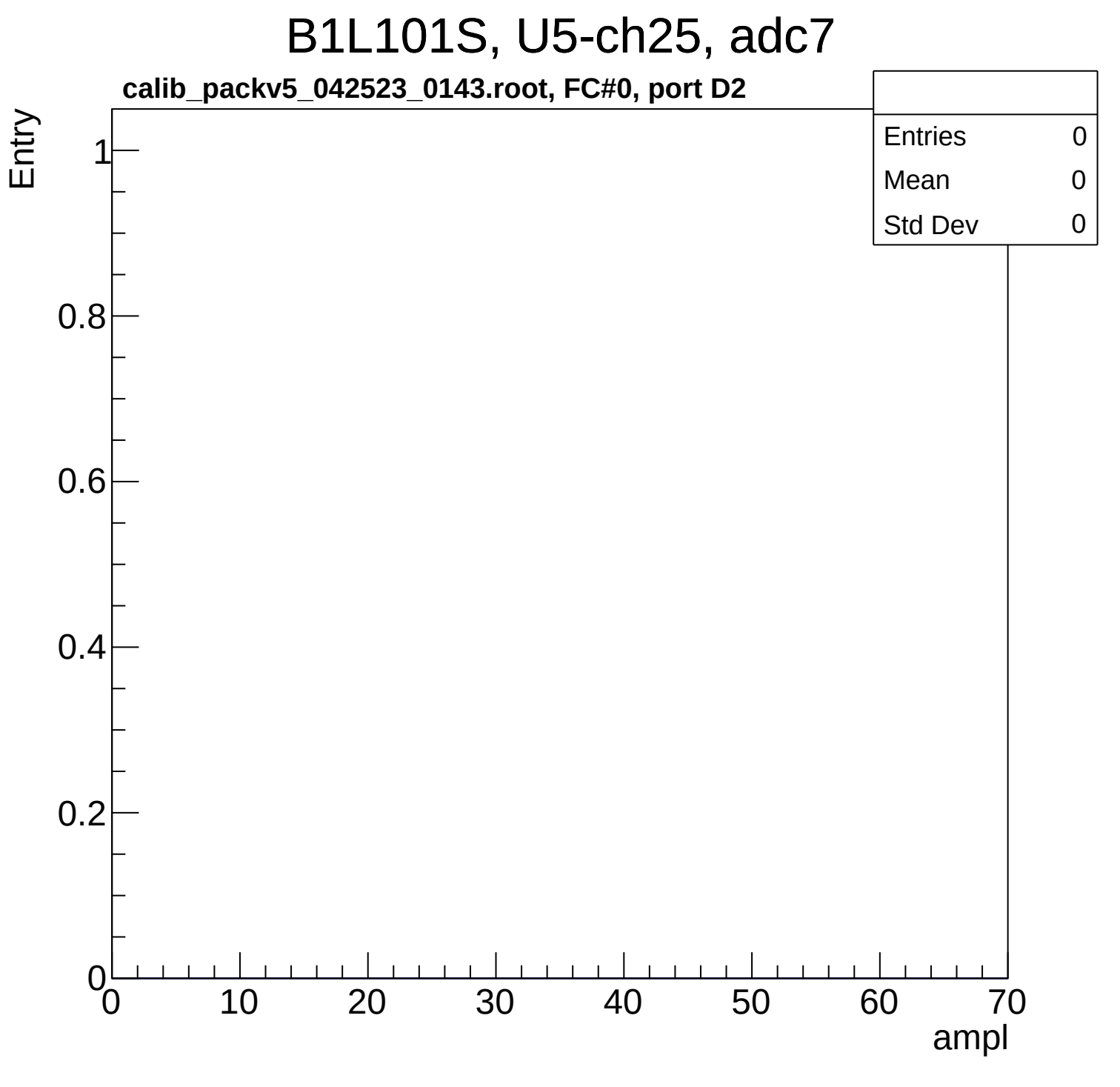
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U5-ch25, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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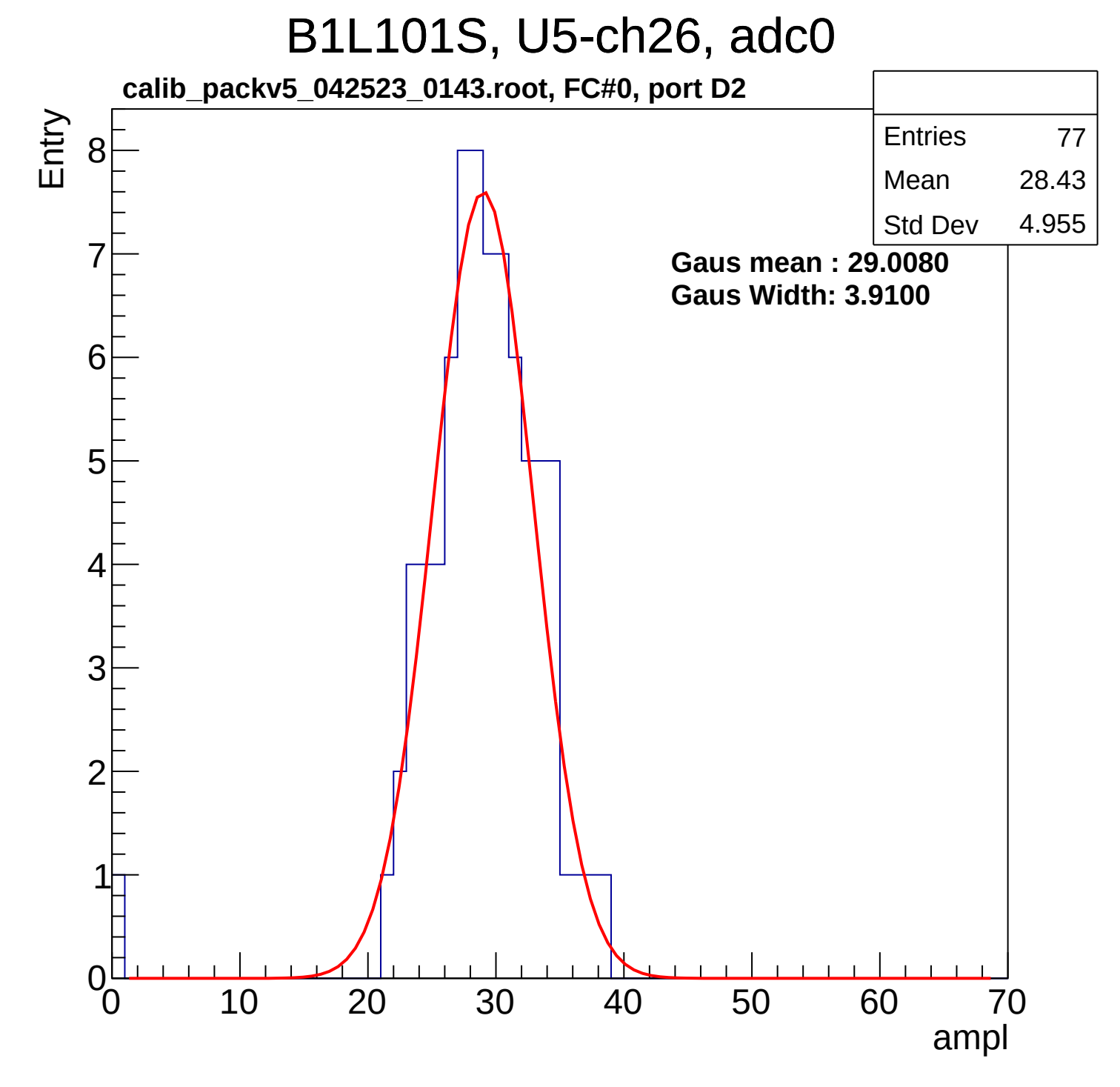
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch26, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 28.43
Std Dev 4.955
Gaus mean : 29.0080
Gaus Width: 3.9100
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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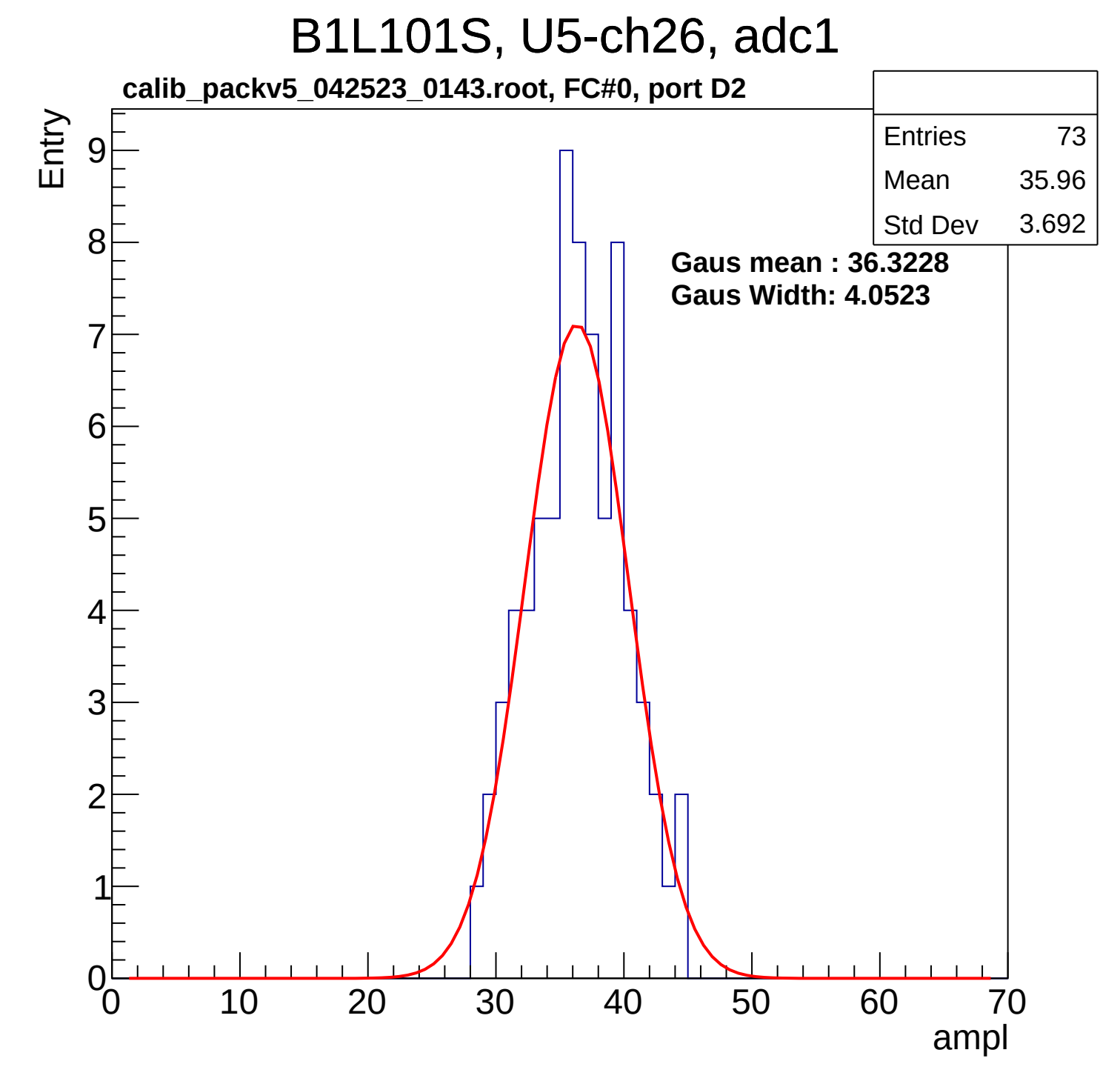
60
70


B1L101S, U5-ch26, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 35.96
Std Dev 3.692
Gaus mean : 36.3228
Gaus Width: 4.0523
Entry
ampl
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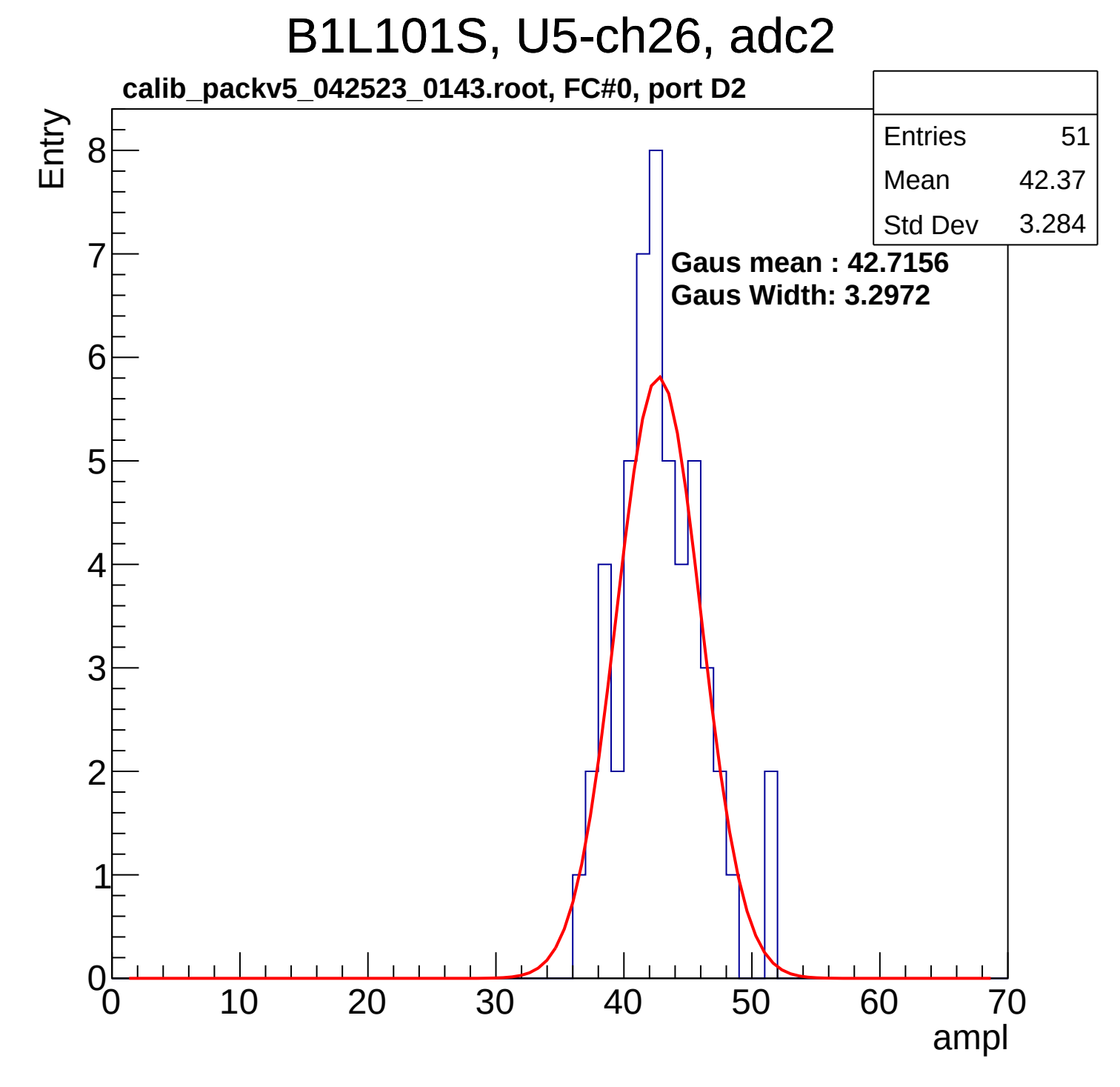
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch26, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 42.37
Std Dev 3.284
Gaus mean : 42.7156
Gaus Width: 3.2972
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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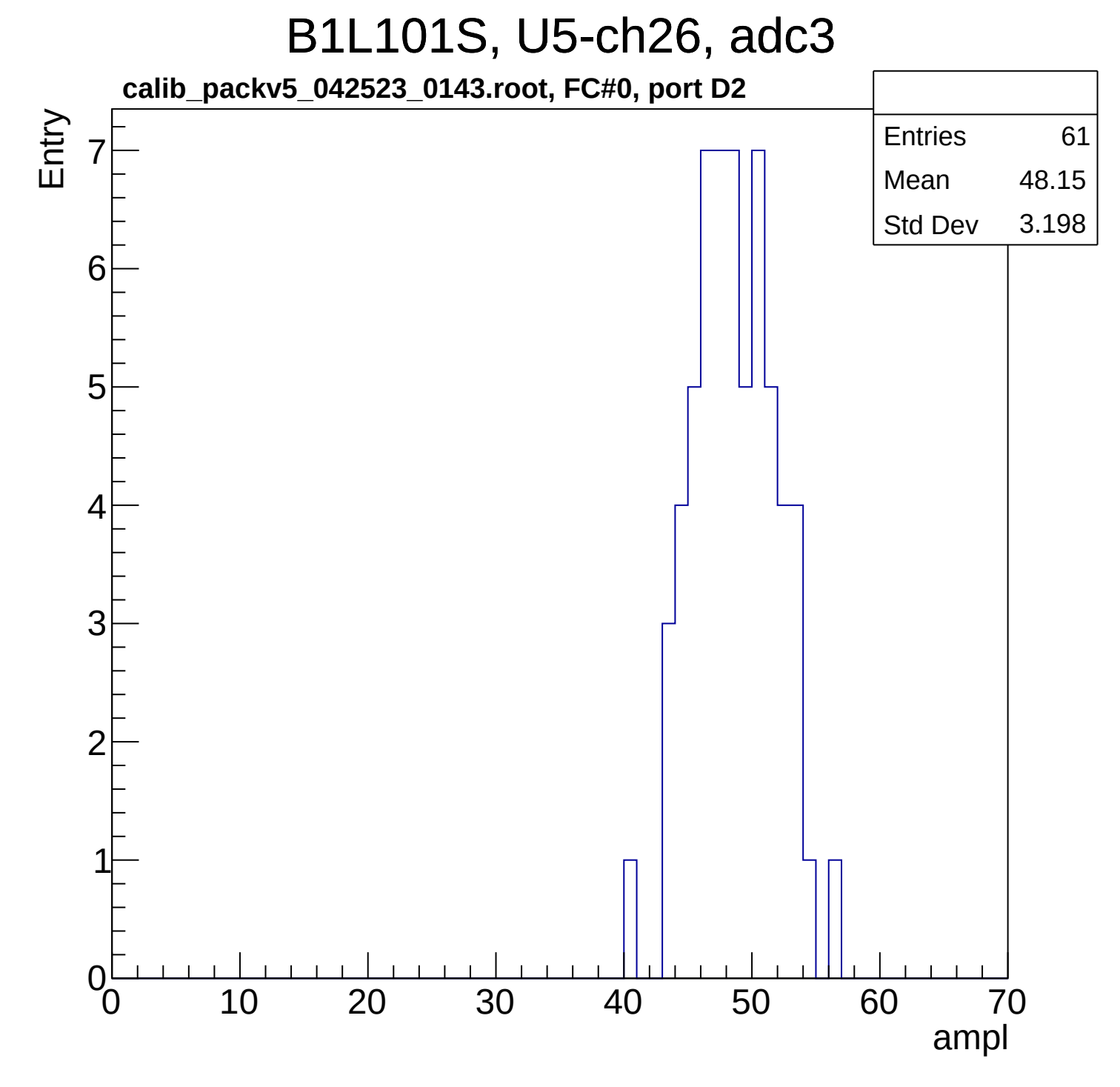
B1L101S, U5-ch26, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 48.15
Std Dev 3.198
Entry
ampl
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3
4
5
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0
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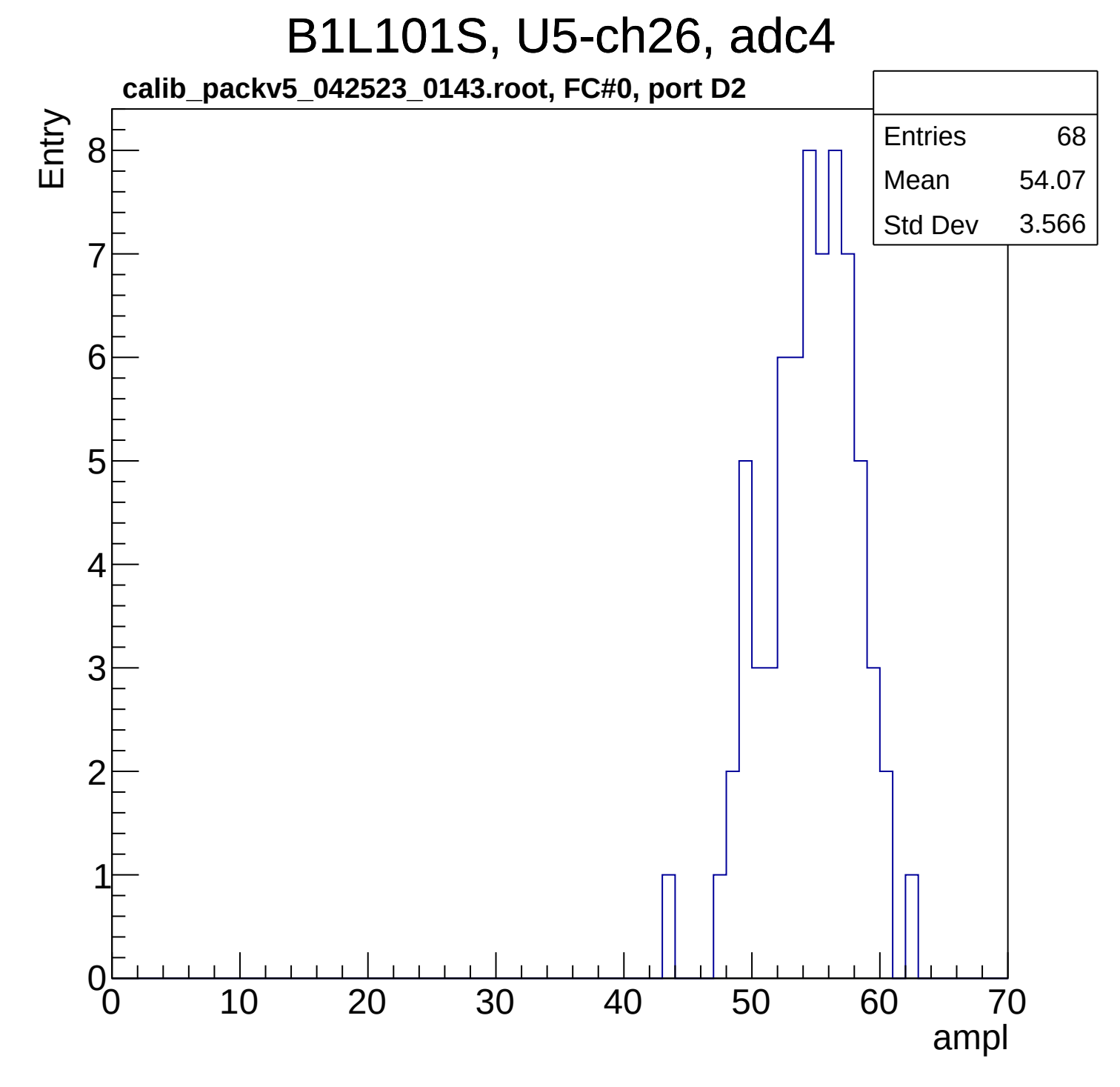
B1L101S, U5-ch26, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 54.07
Std Dev 3.566
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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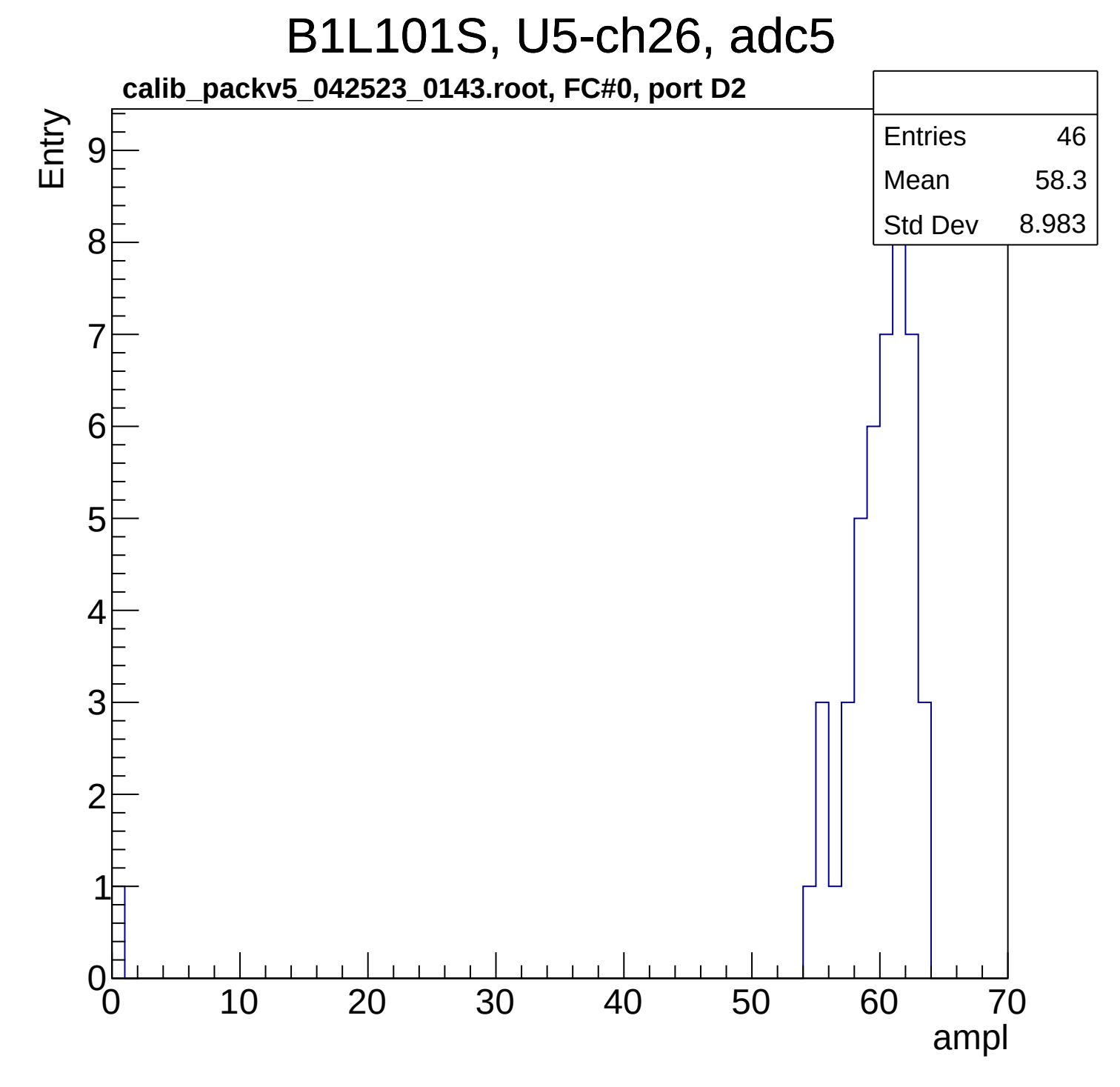
B1L101S, U5-ch26, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 58.3
Std Dev 8.983
Entry
ampl
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2
3
4
5
6
7
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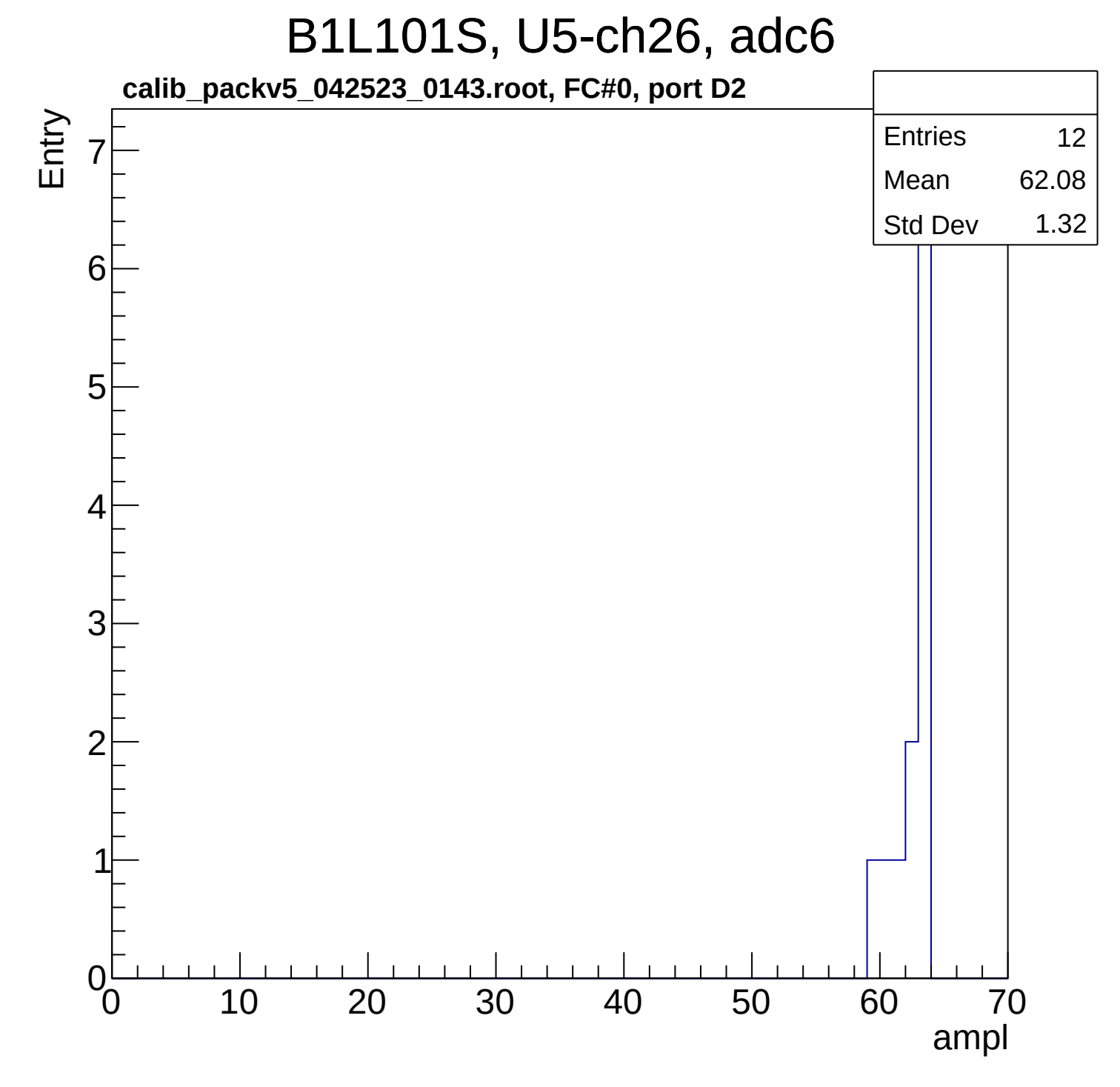
B1L101S, U5-ch26, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 12
Mean 62.08
Std Dev 1.32
Entry
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2
3
4
5
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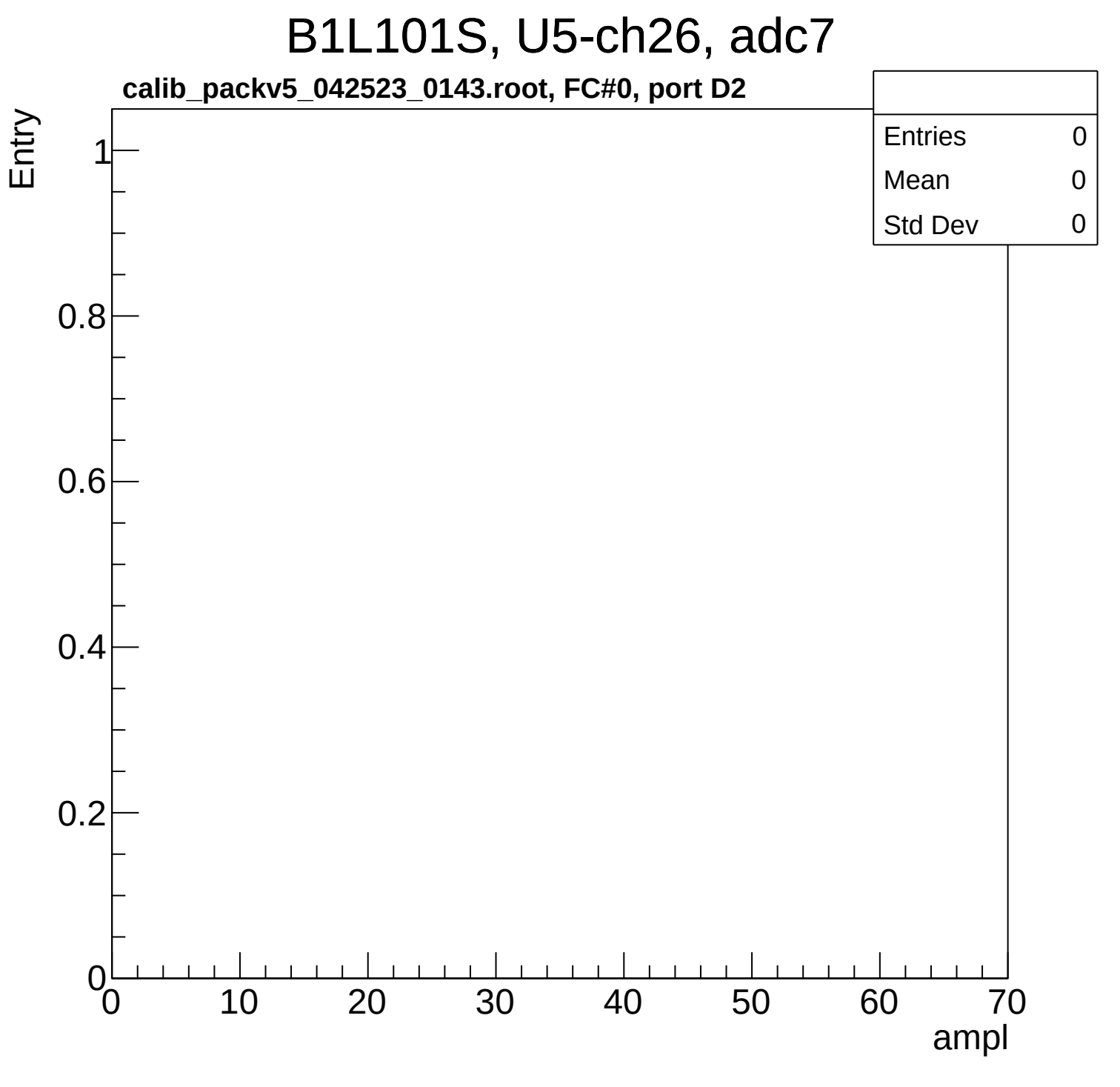
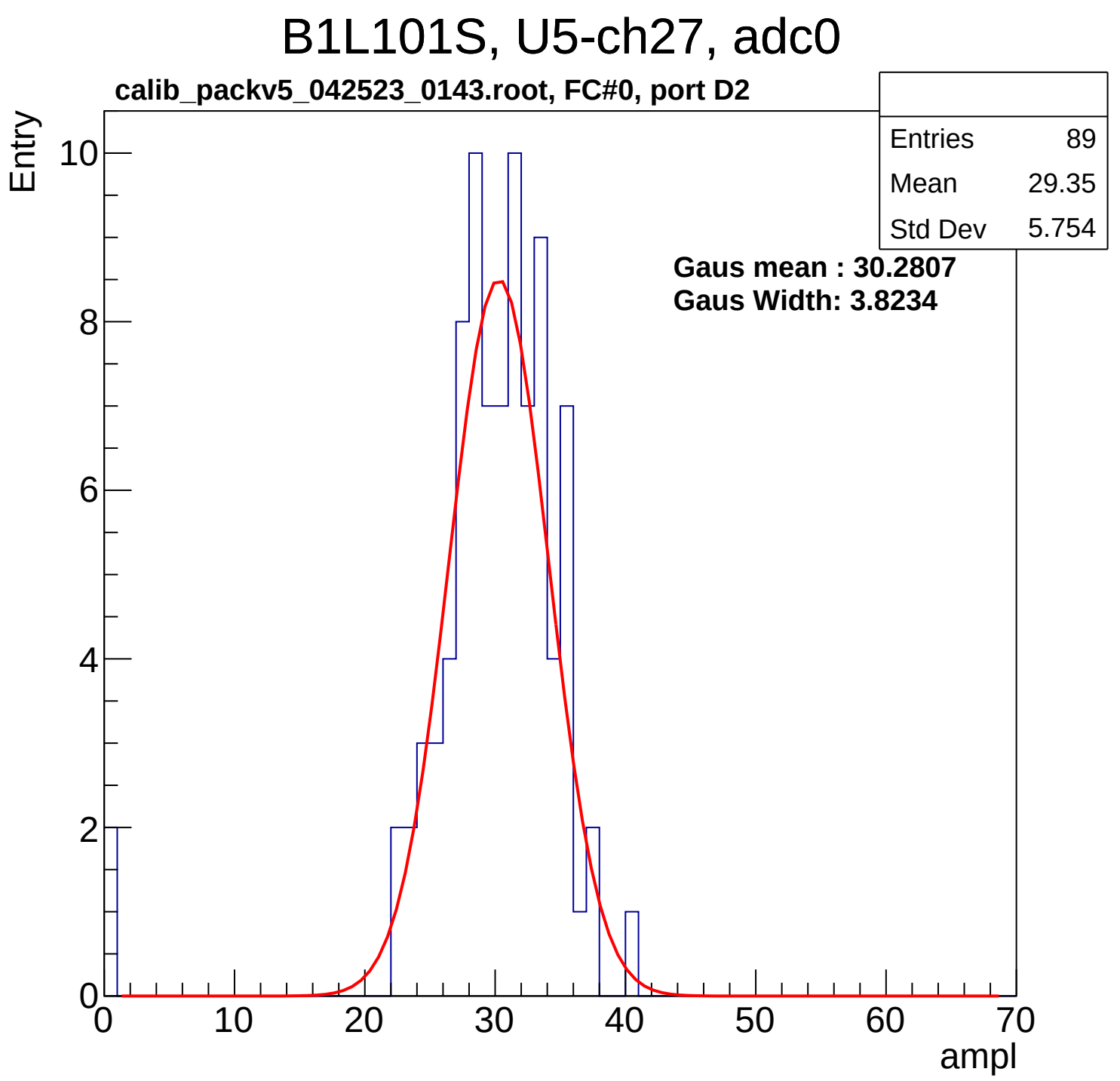
7
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch26, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch27, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 89
Mean 29.35
Std Dev 5.754
Gaus mean : 30.2807
Gaus Width: 3.8234
Entry
ampl
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2
4
6
8
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0
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40
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60
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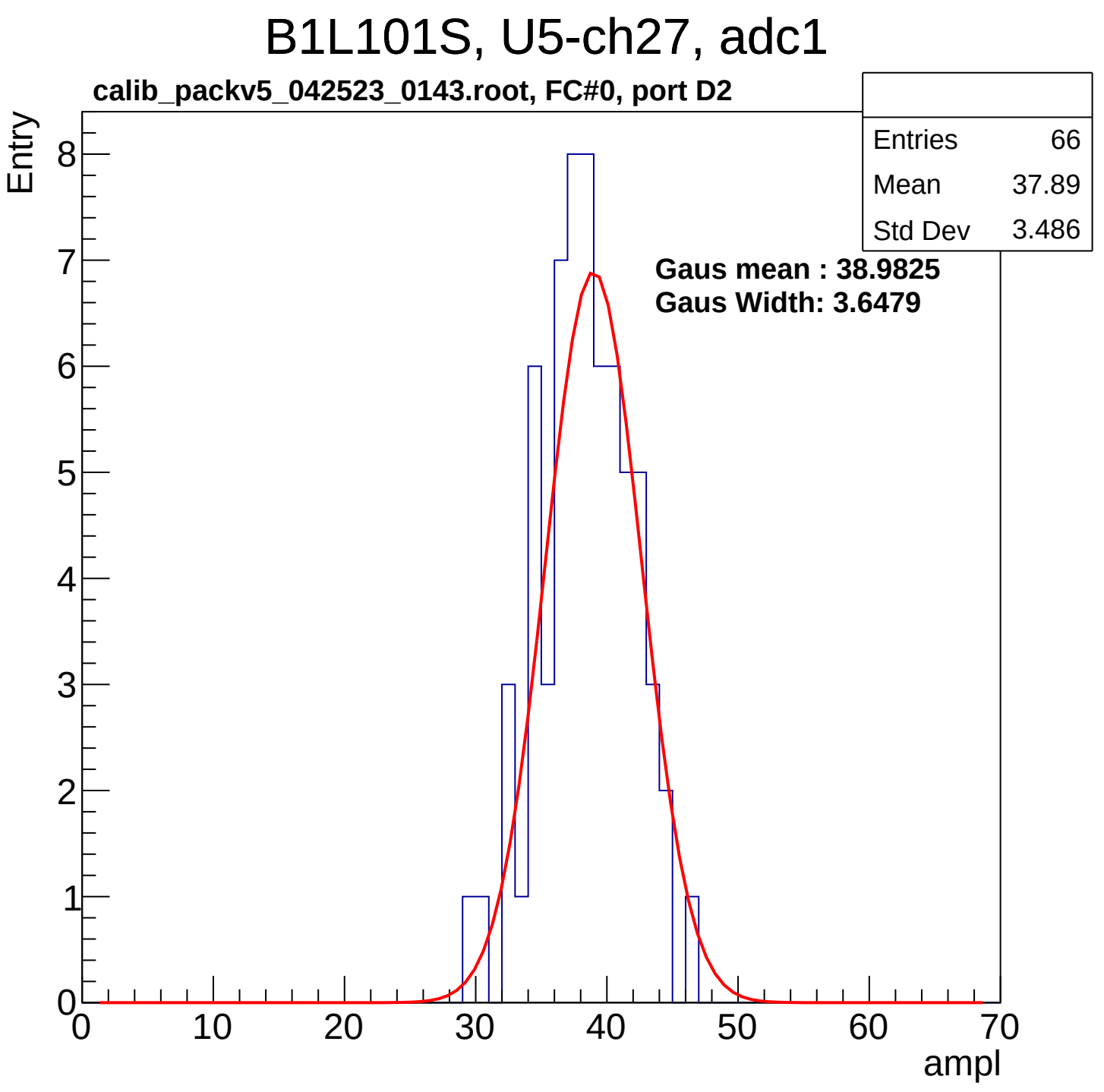
B1L101S, U5-ch27, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 37.89
Std Dev 3.486
Gaus mean : 38.9825
Gaus Width: 3.6479
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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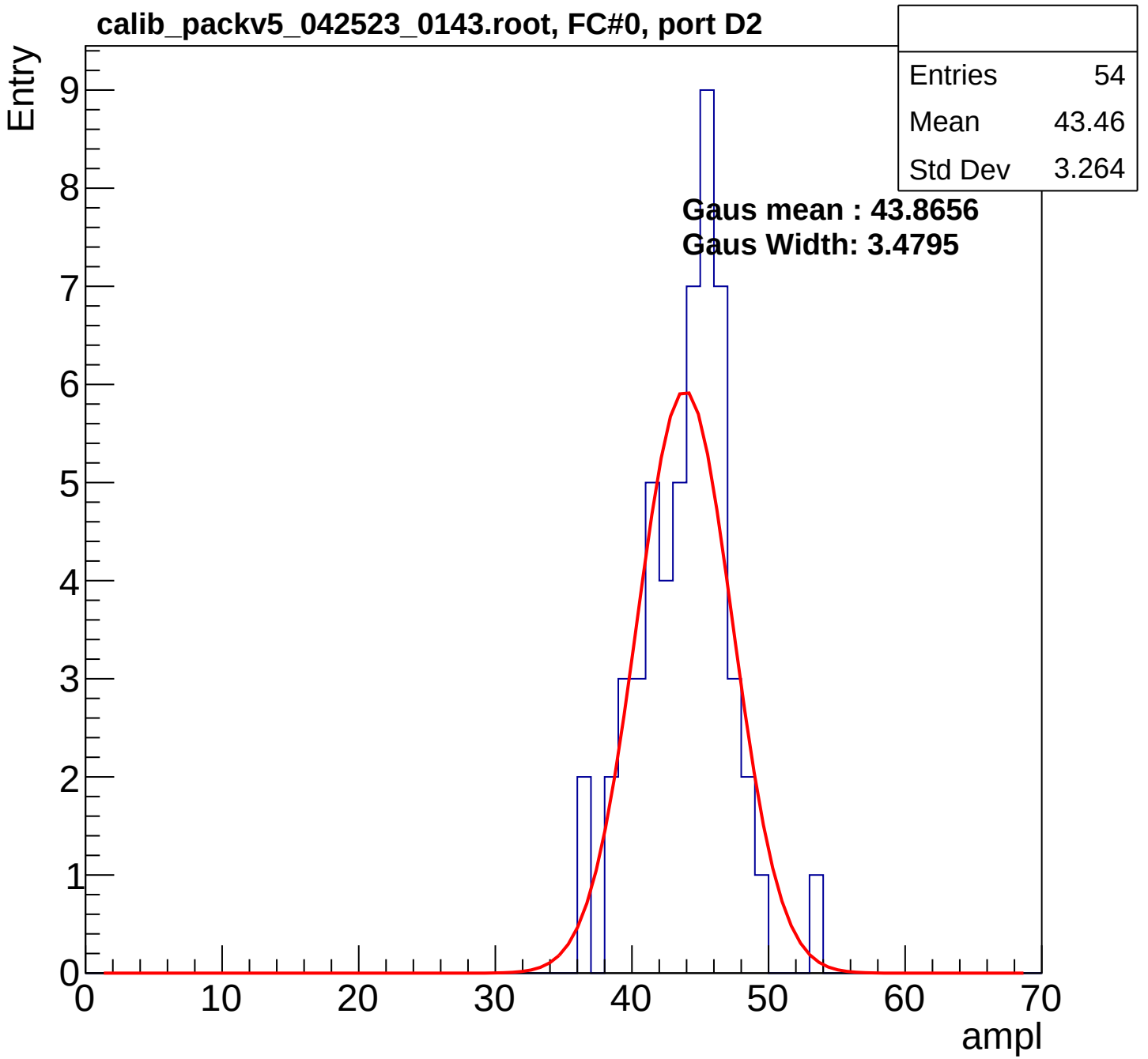
B1L101S, U5-ch27, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 43.46
Std Dev 3.264
Gaus mean : 43.8656
Gaus Width: 3.4795
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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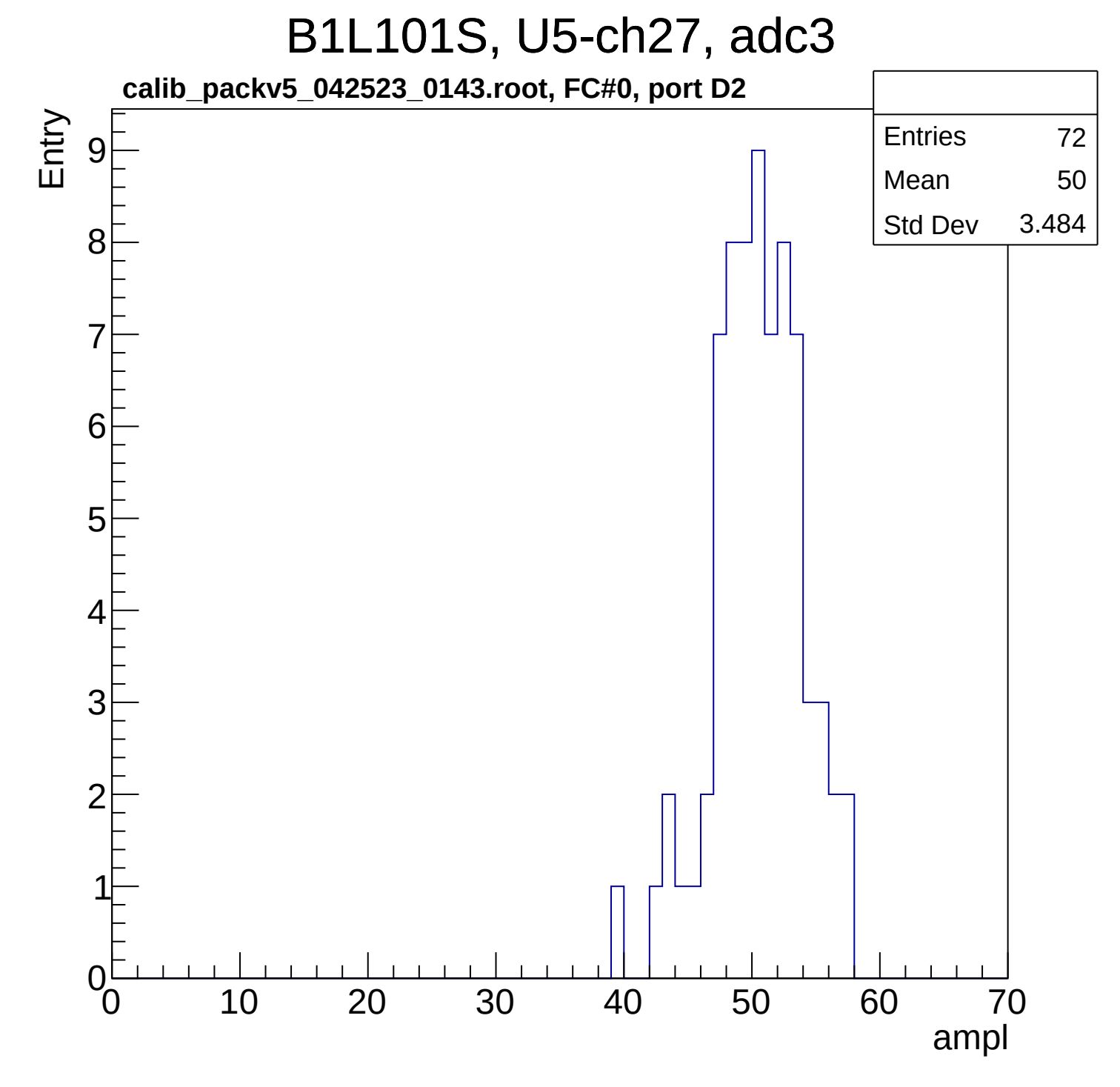
B1L101S, U5-ch27, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 50
Std Dev 3.484
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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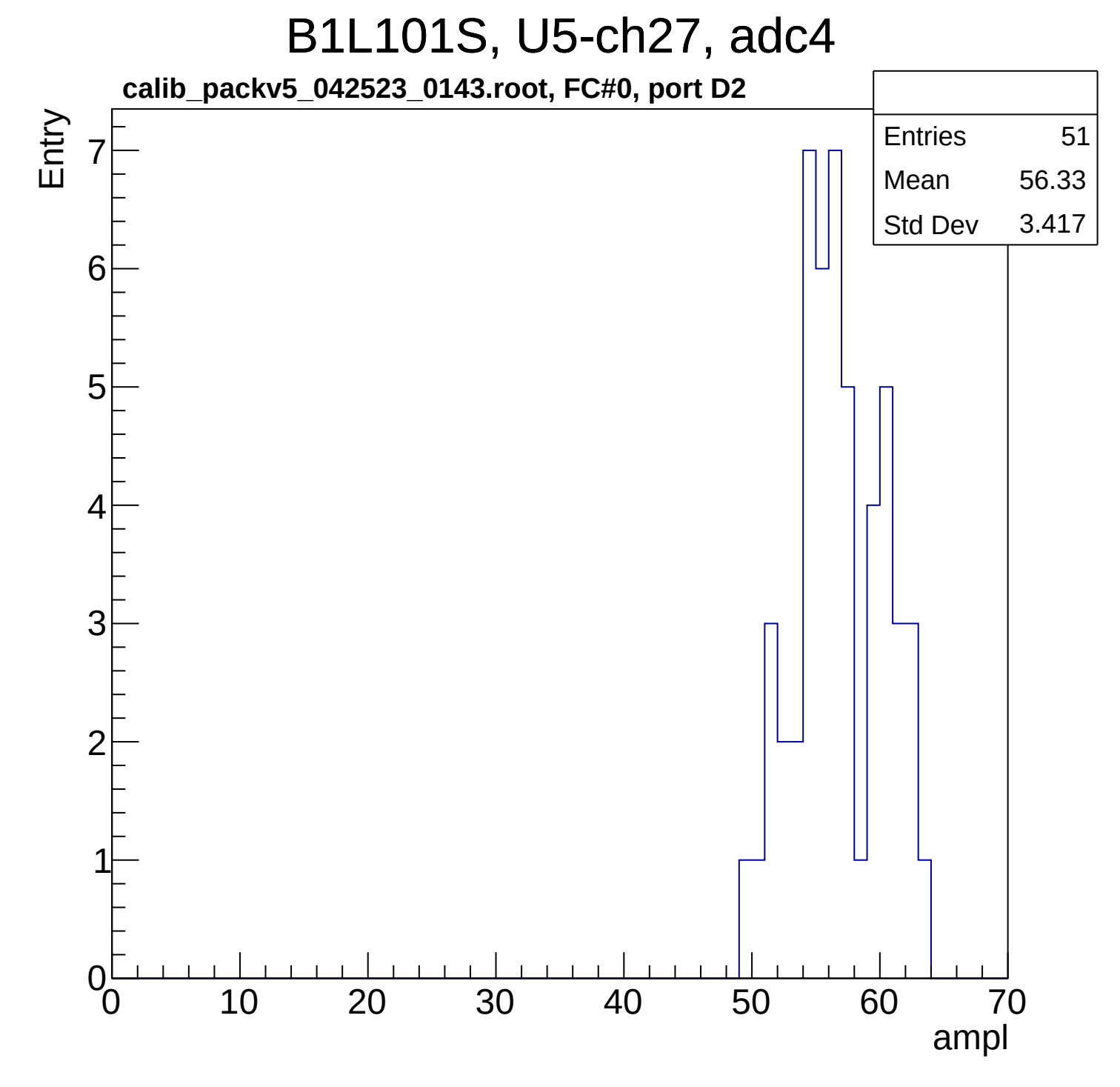
B1L101S, U5-ch27, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 56.33
Std Dev 3.417
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
50
60
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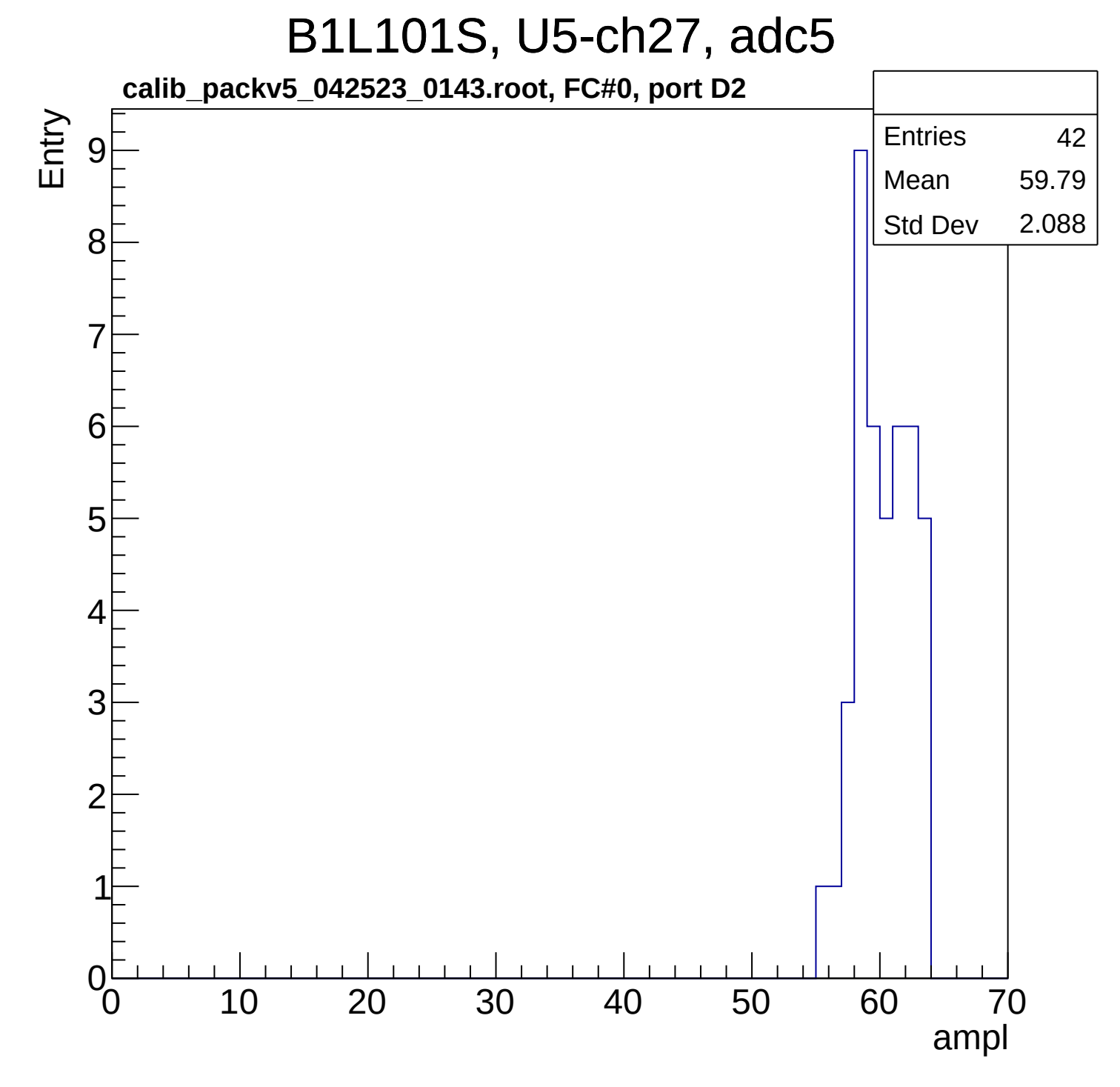
B1L101S, U5-ch27, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 59.79
Std Dev 2.088
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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60
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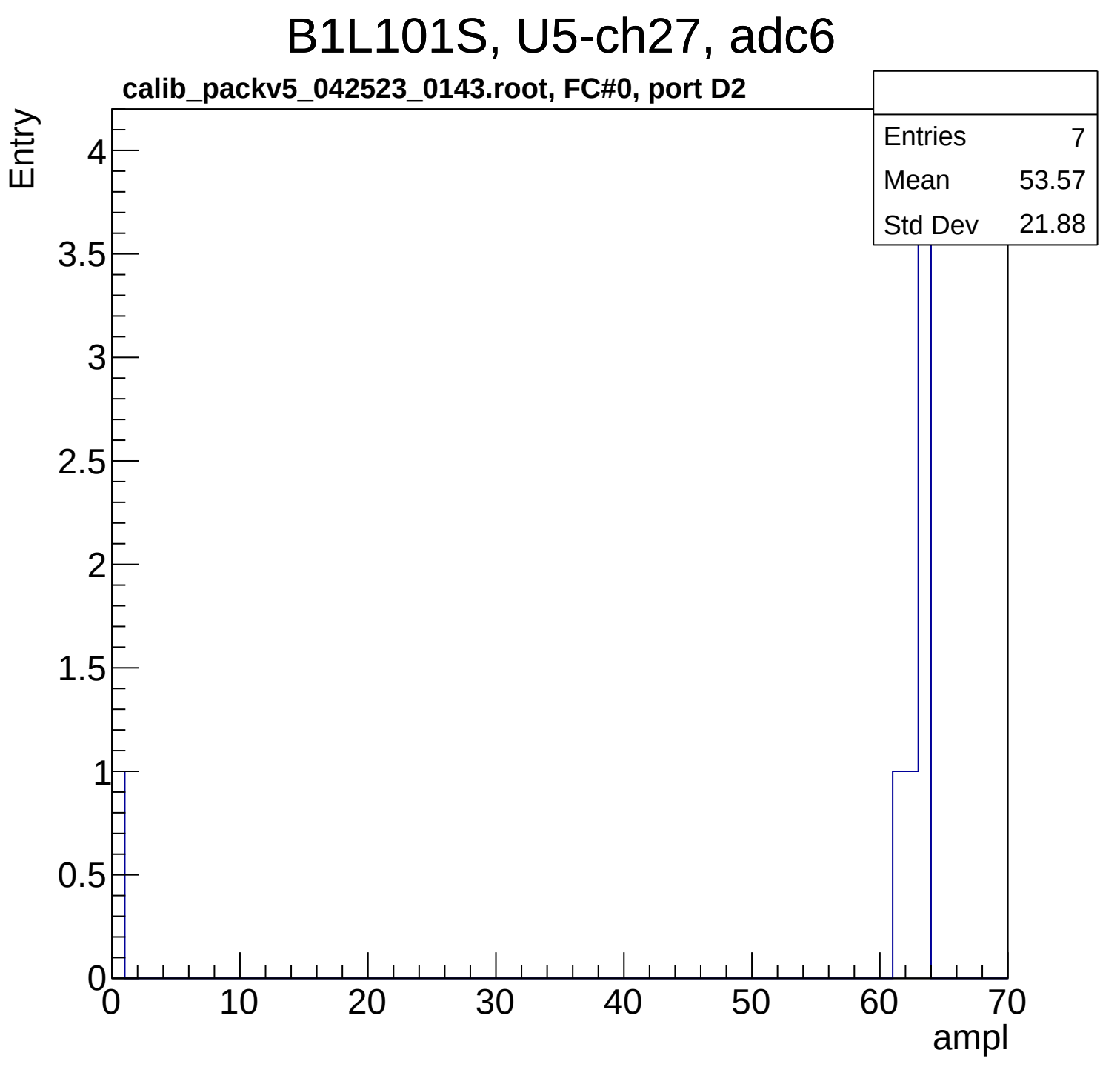
B1L101S, U5-ch27, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 53.57
Std Dev 21.88
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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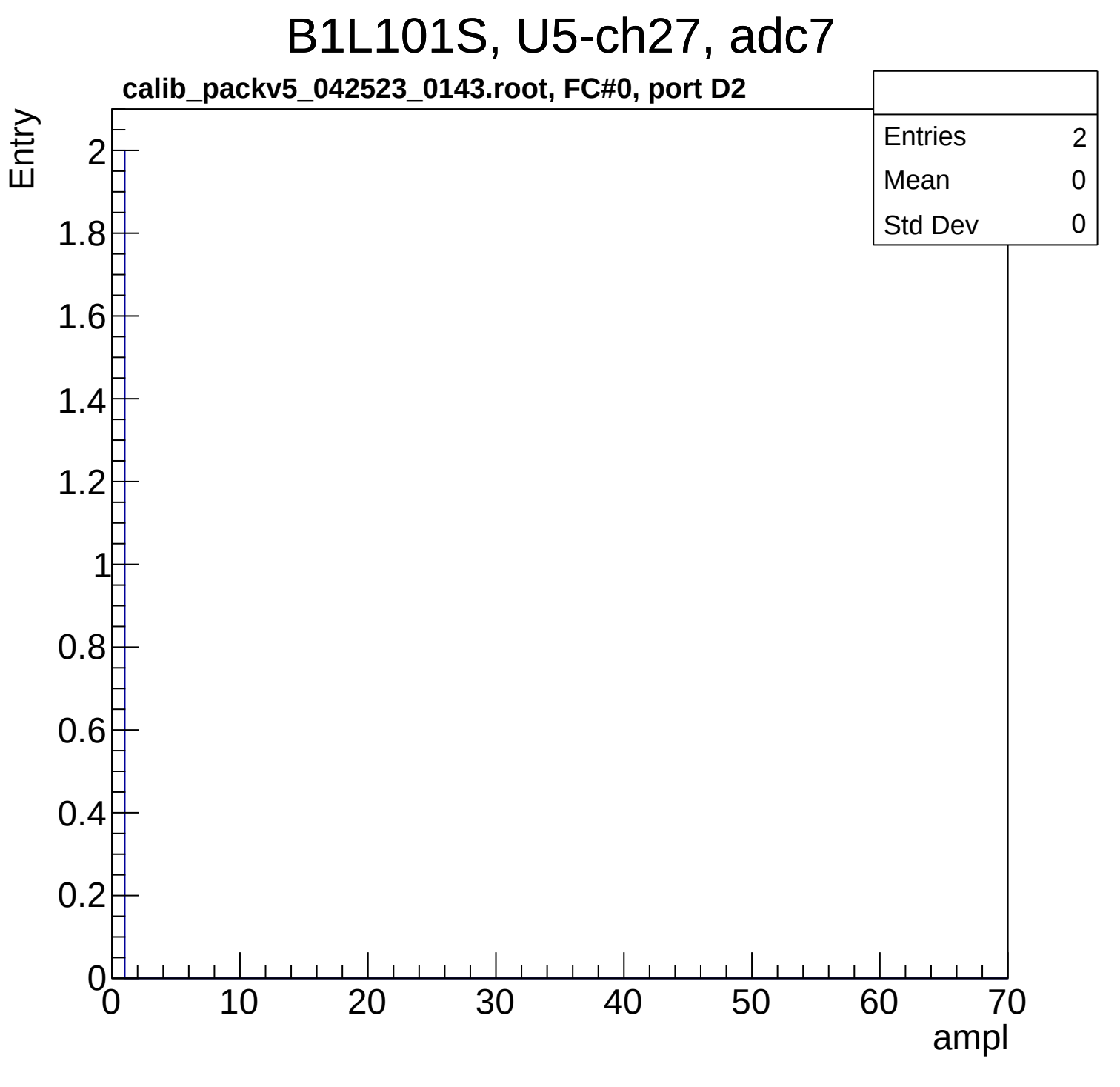
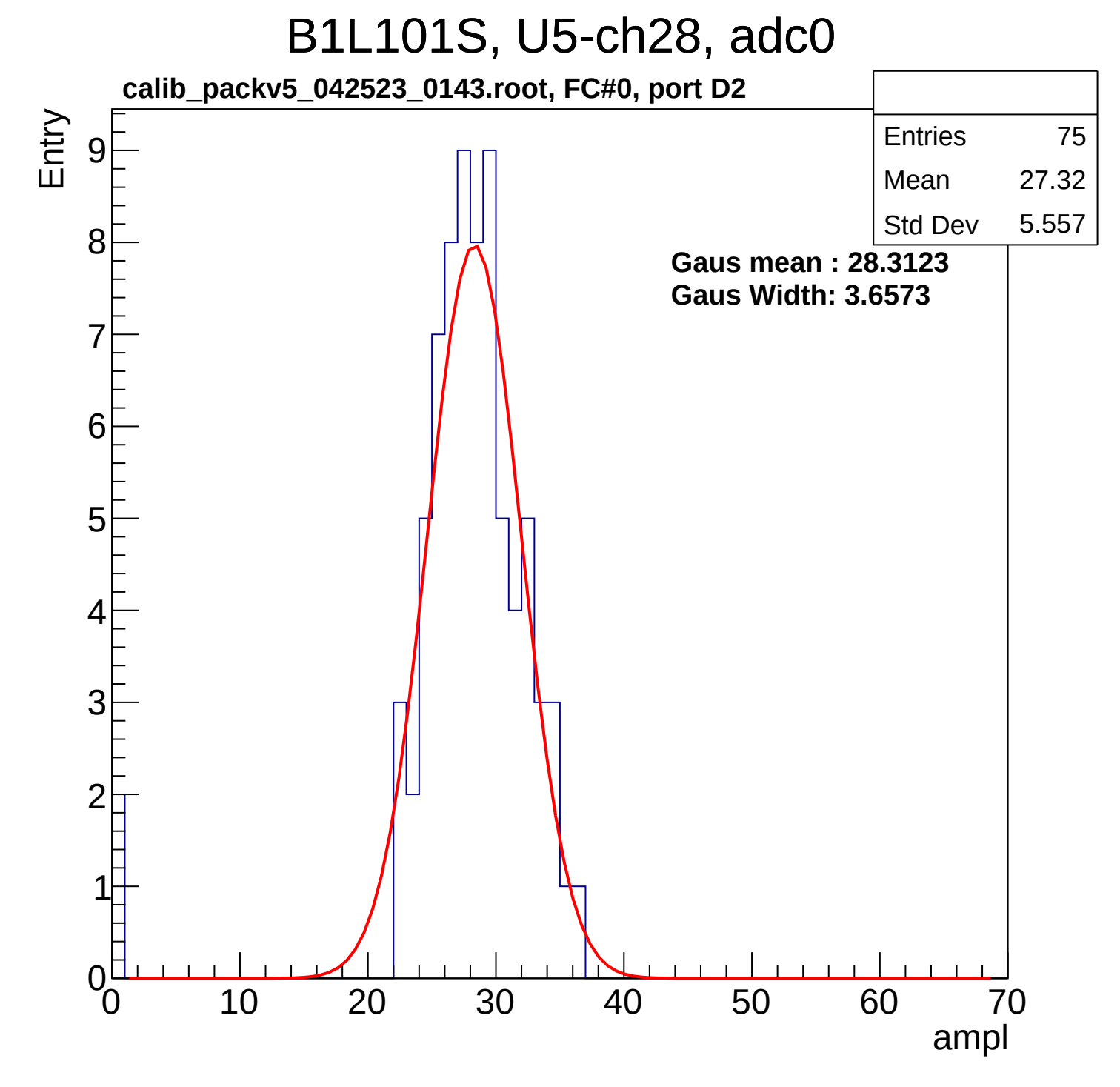

B1L101S, U5-ch27, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch28, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 27.32
Std Dev 5.557
Gaus mean : 28.3123
Gaus Width: 3.6573
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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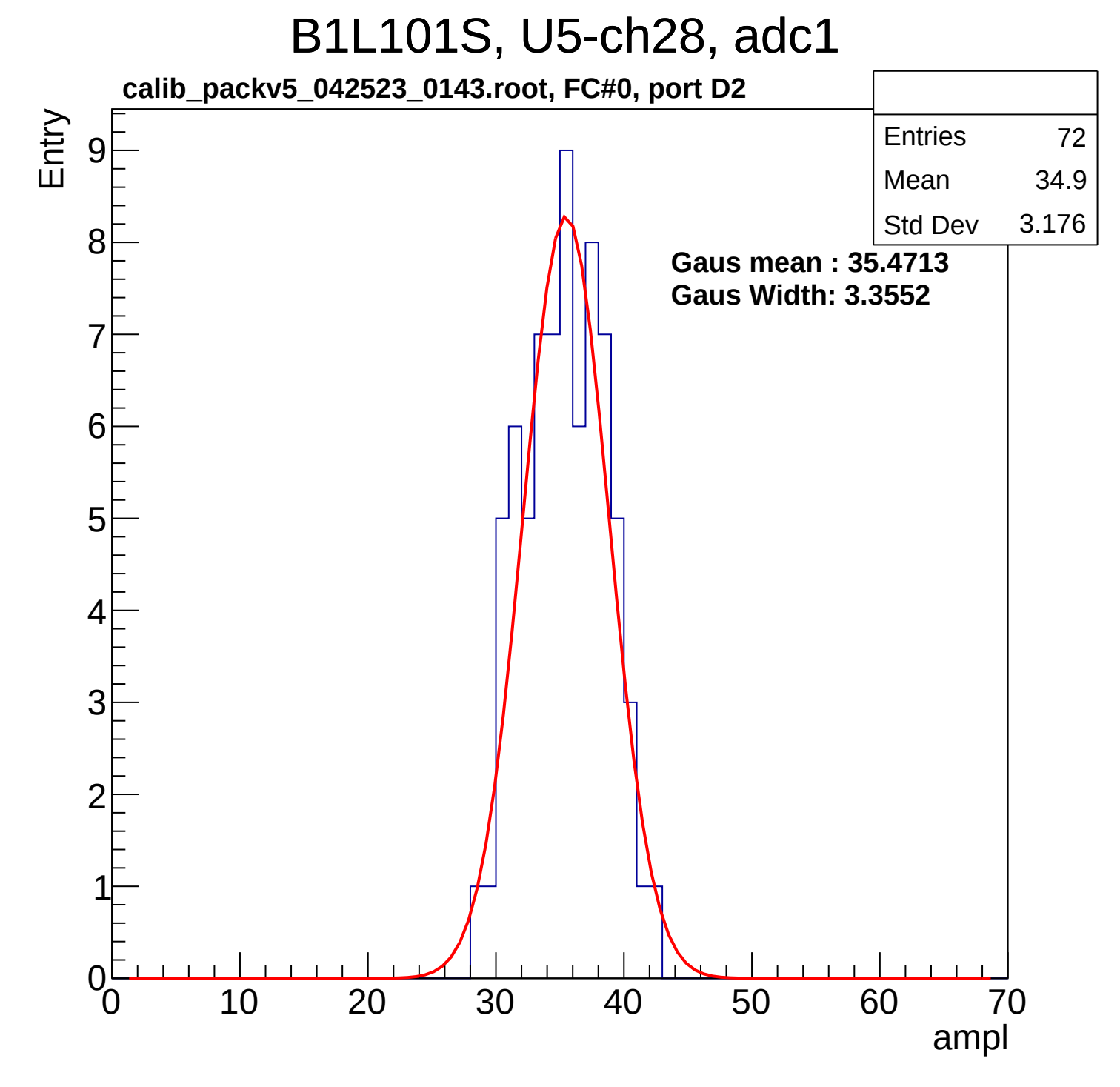
B1L101S, U5-ch28, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 34.9
Std Dev 3.176
Gaus mean : 35.4713
Gaus Width: 3.3552
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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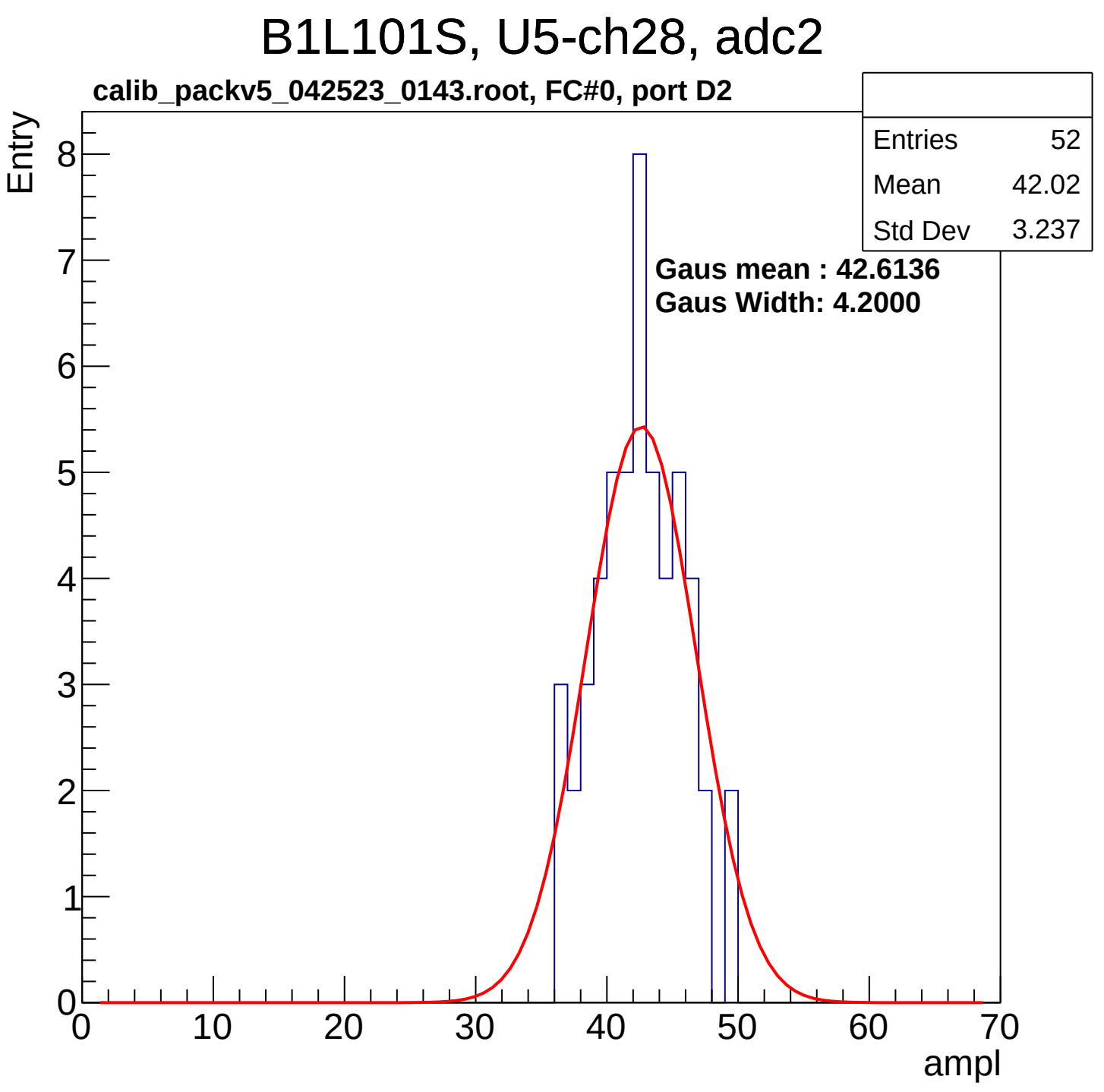
B1L101S, U5-ch28, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 42.02
Std Dev 3.237
Gaus mean : 42.6136
Gaus Width: 4.2000
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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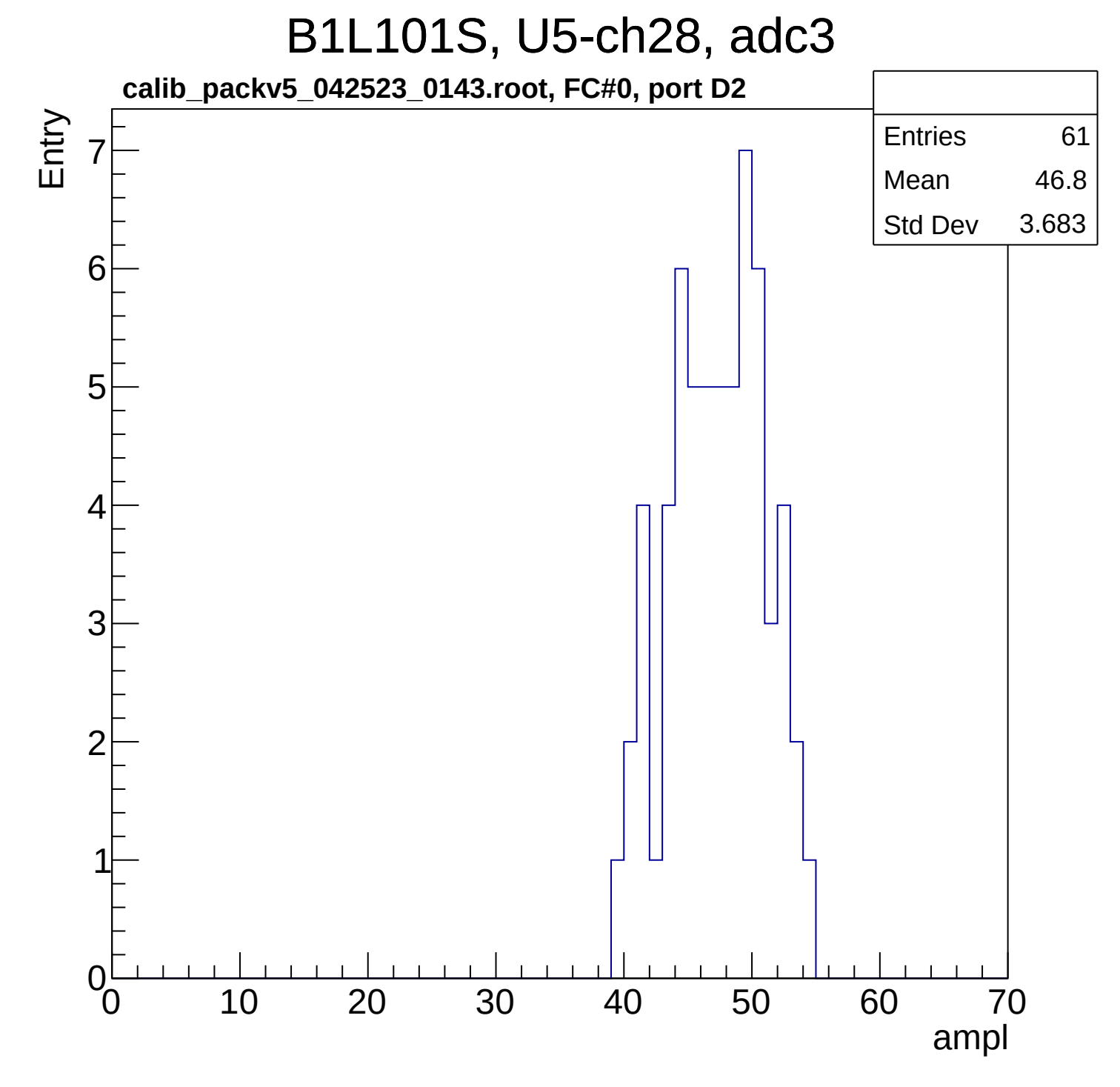
B1L101S, U5-ch28, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 46.8
Std Dev 3.683
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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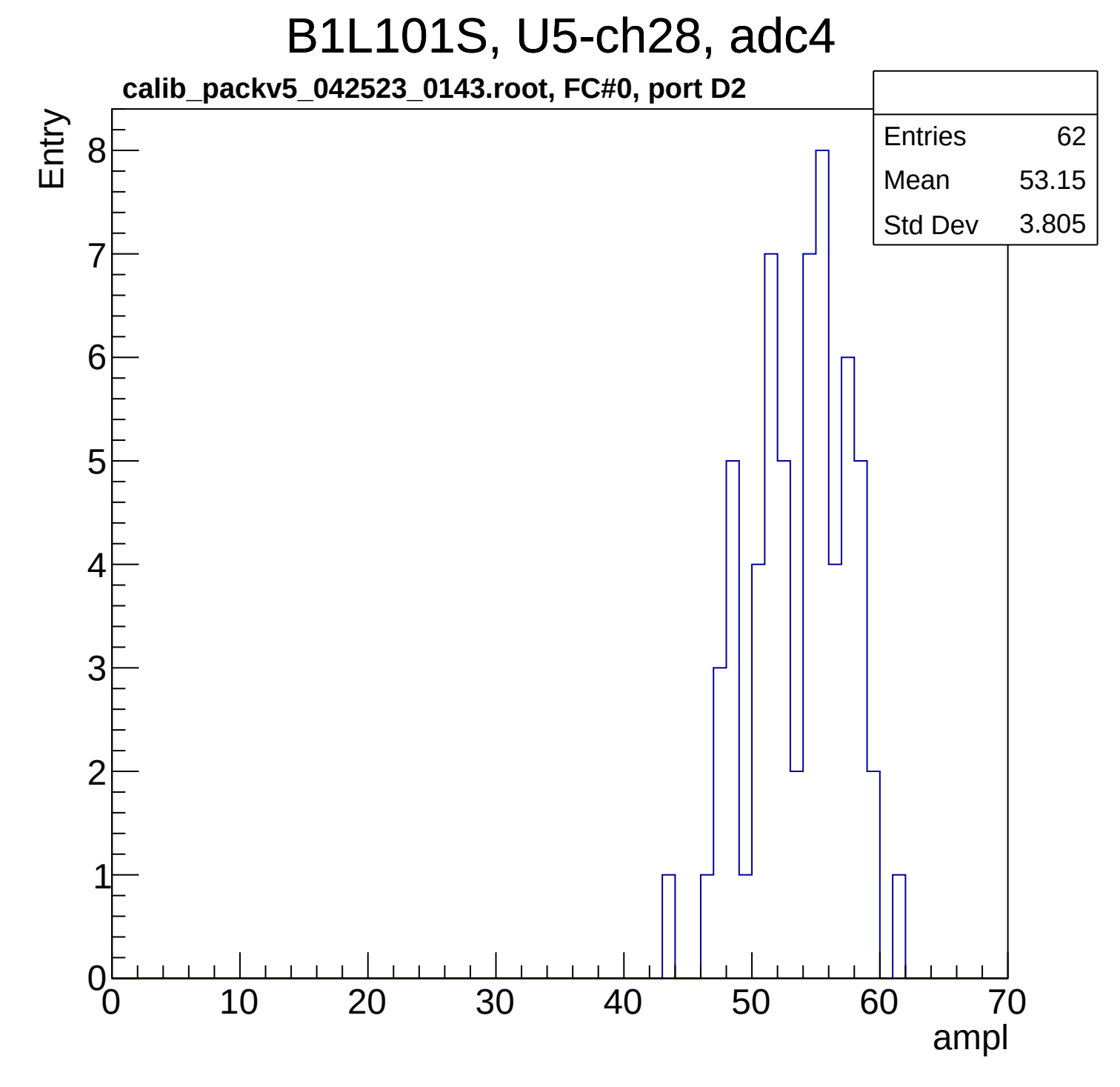
B1L101S, U5-ch28, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 53.15
Std Dev 3.805
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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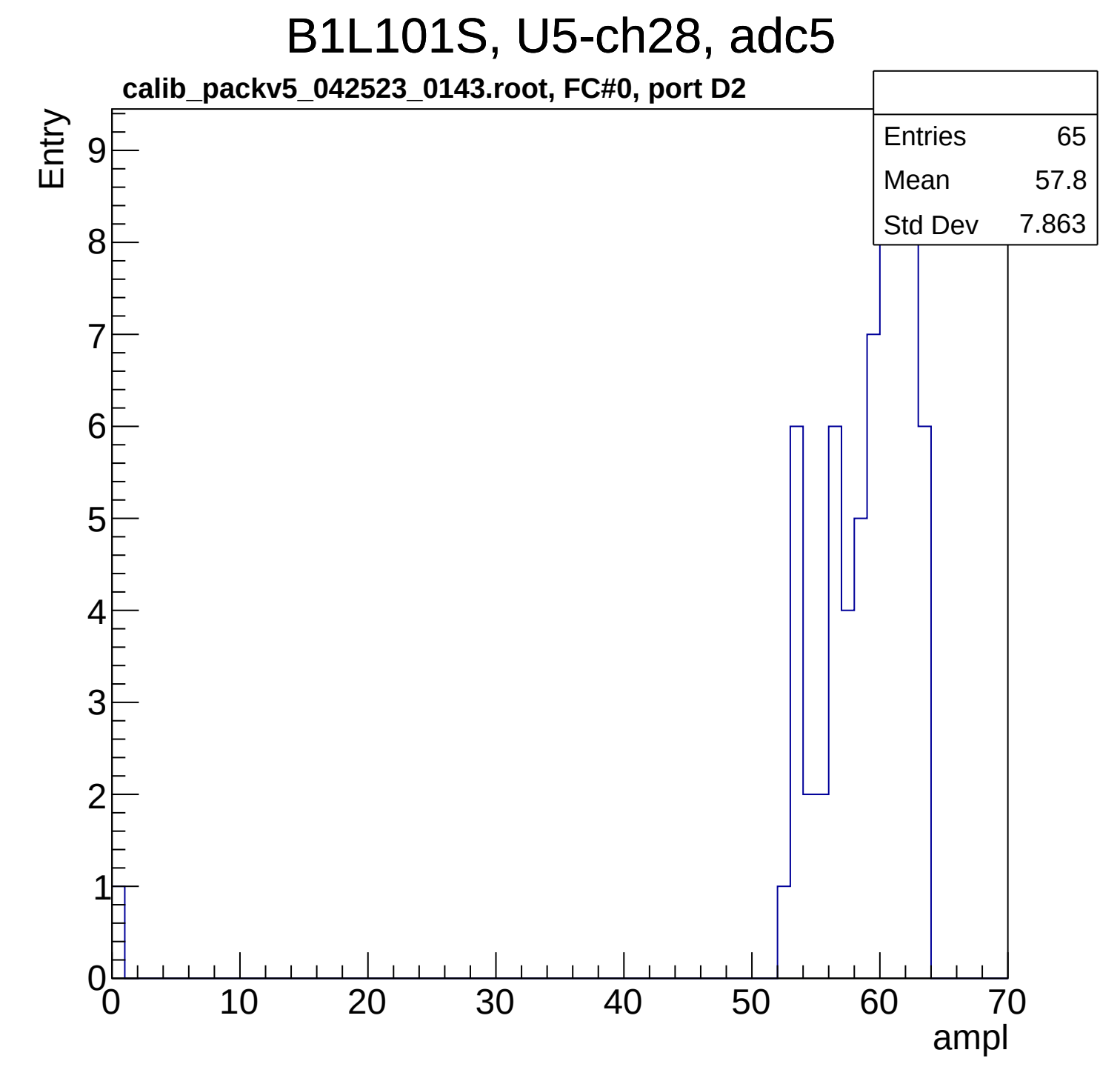
B1L101S, U5-ch28, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 57.8
Std Dev 7.863
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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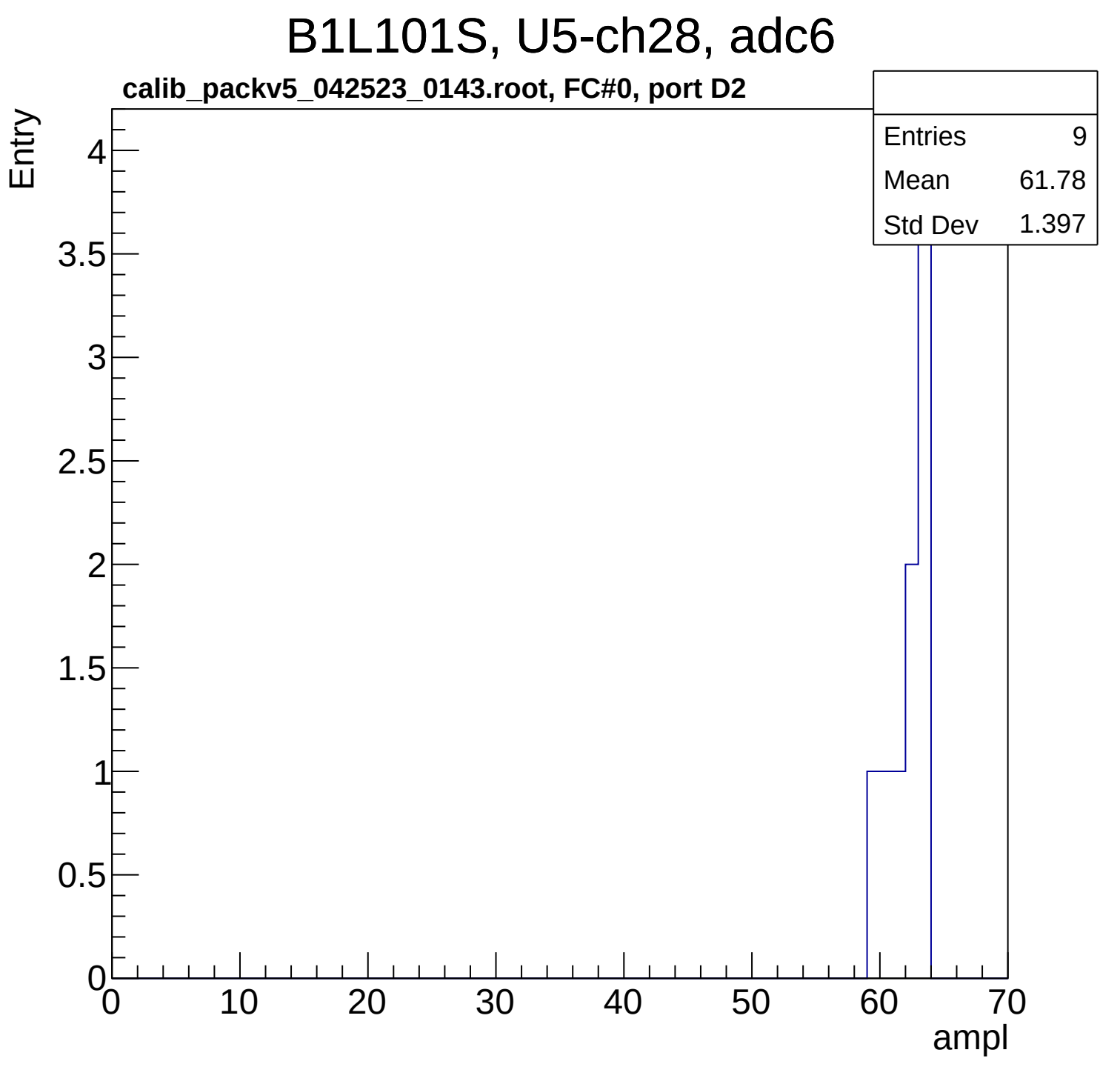
B1L101S, U5-ch28, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 61.78
Std Dev 1.397
Entry
ampl
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1
1.5
2
2.5
3
3.5
4
0
10
20
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40
50
60
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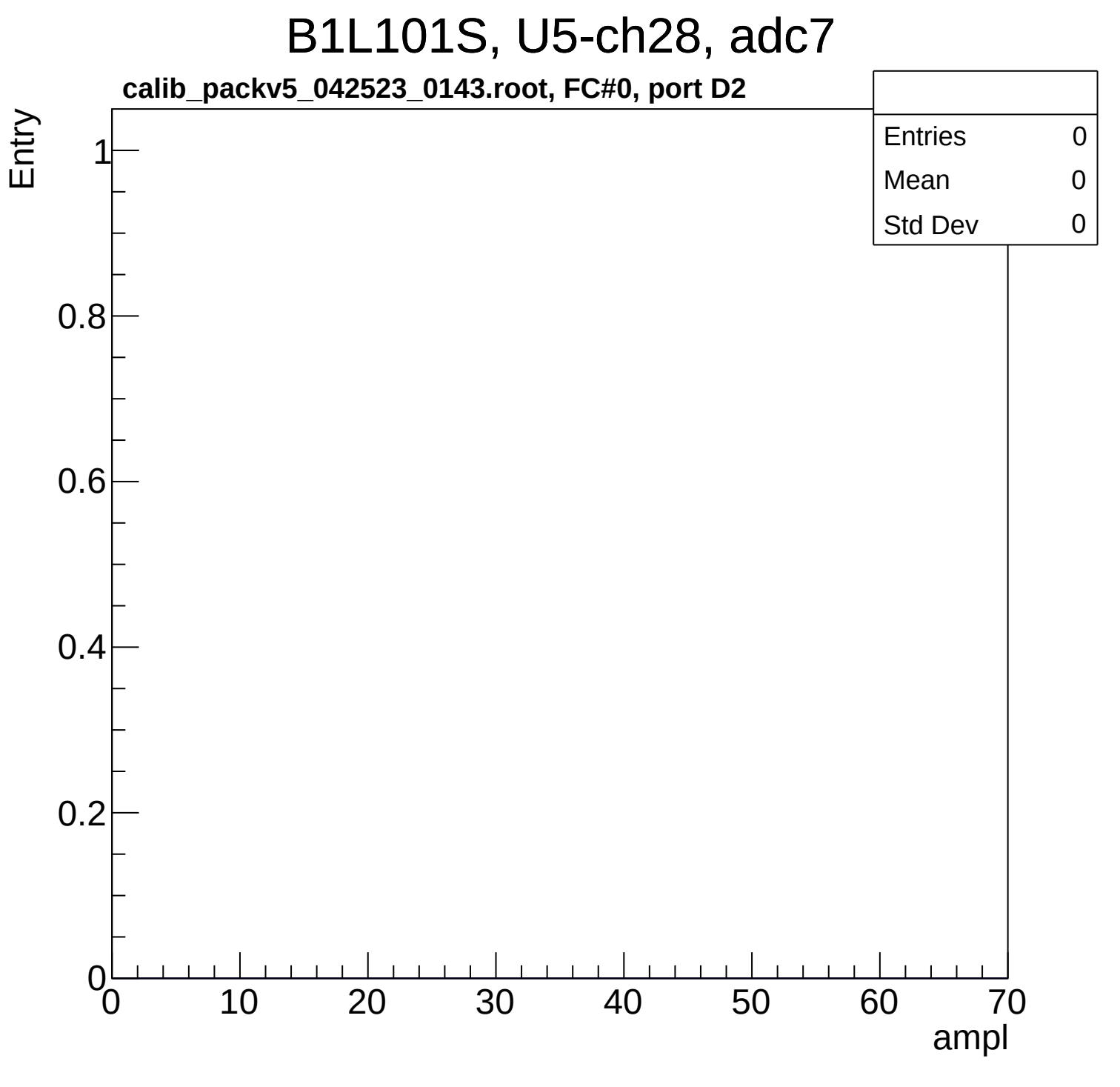
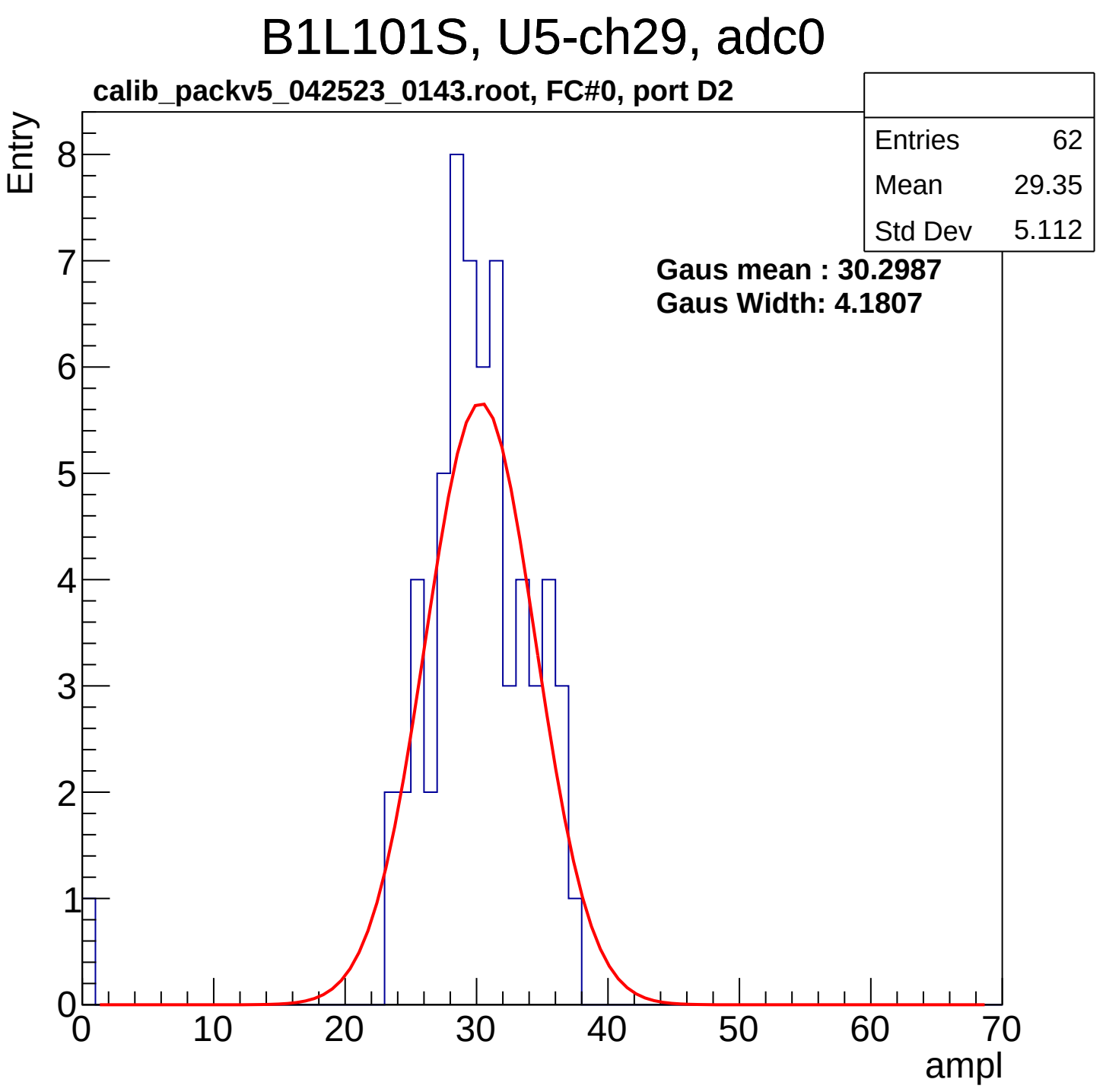

B1L101S, U5-ch28, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch29, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 29.35
Std Dev 5.112
Gaus mean : 30.2987
Gaus Width: 4.1807
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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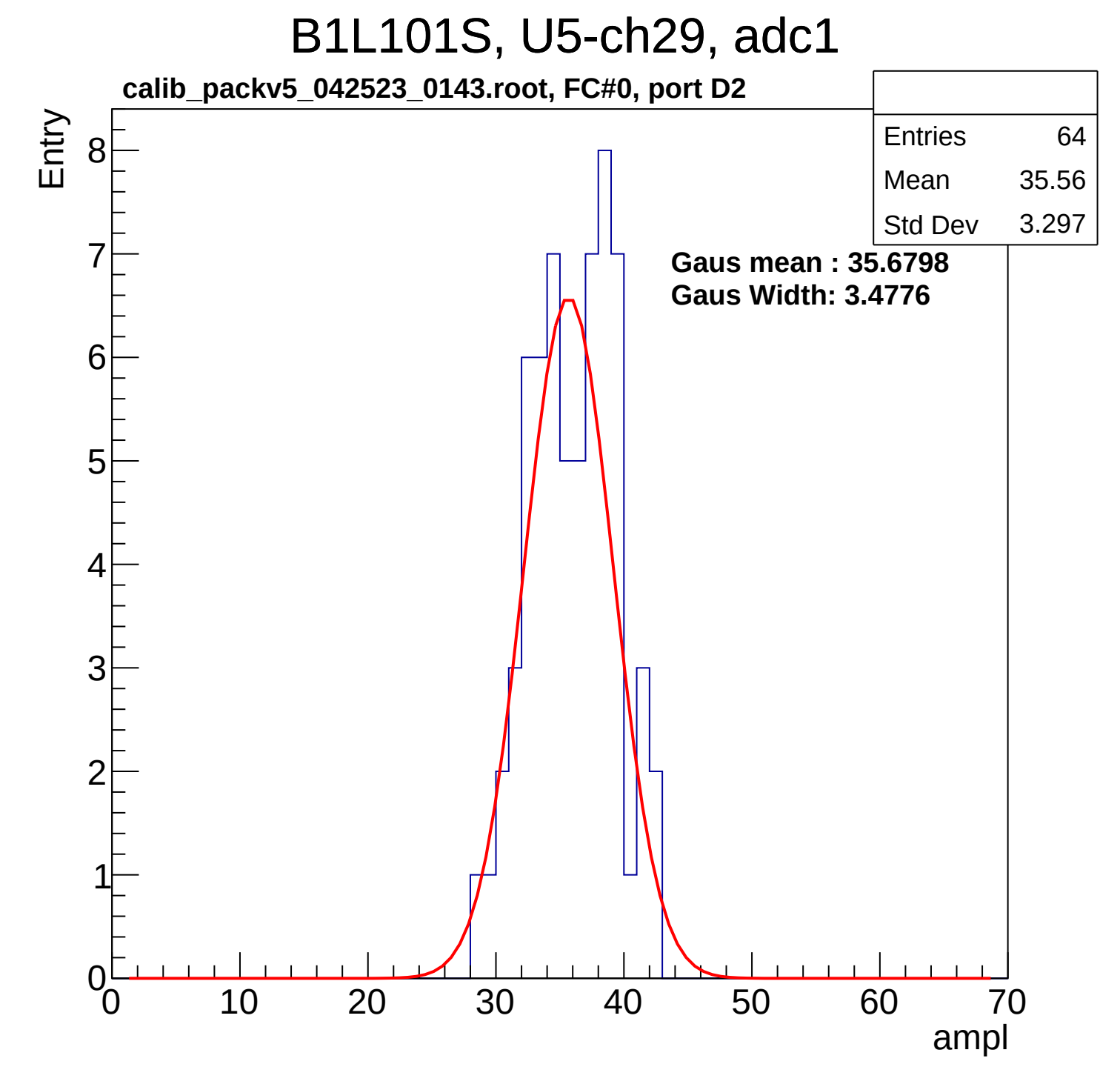
40
50
60
70


B1L101S, U5-ch29, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 35.56
Std Dev 3.297
Gaus mean : 35.6798
Gaus Width: 3.4776
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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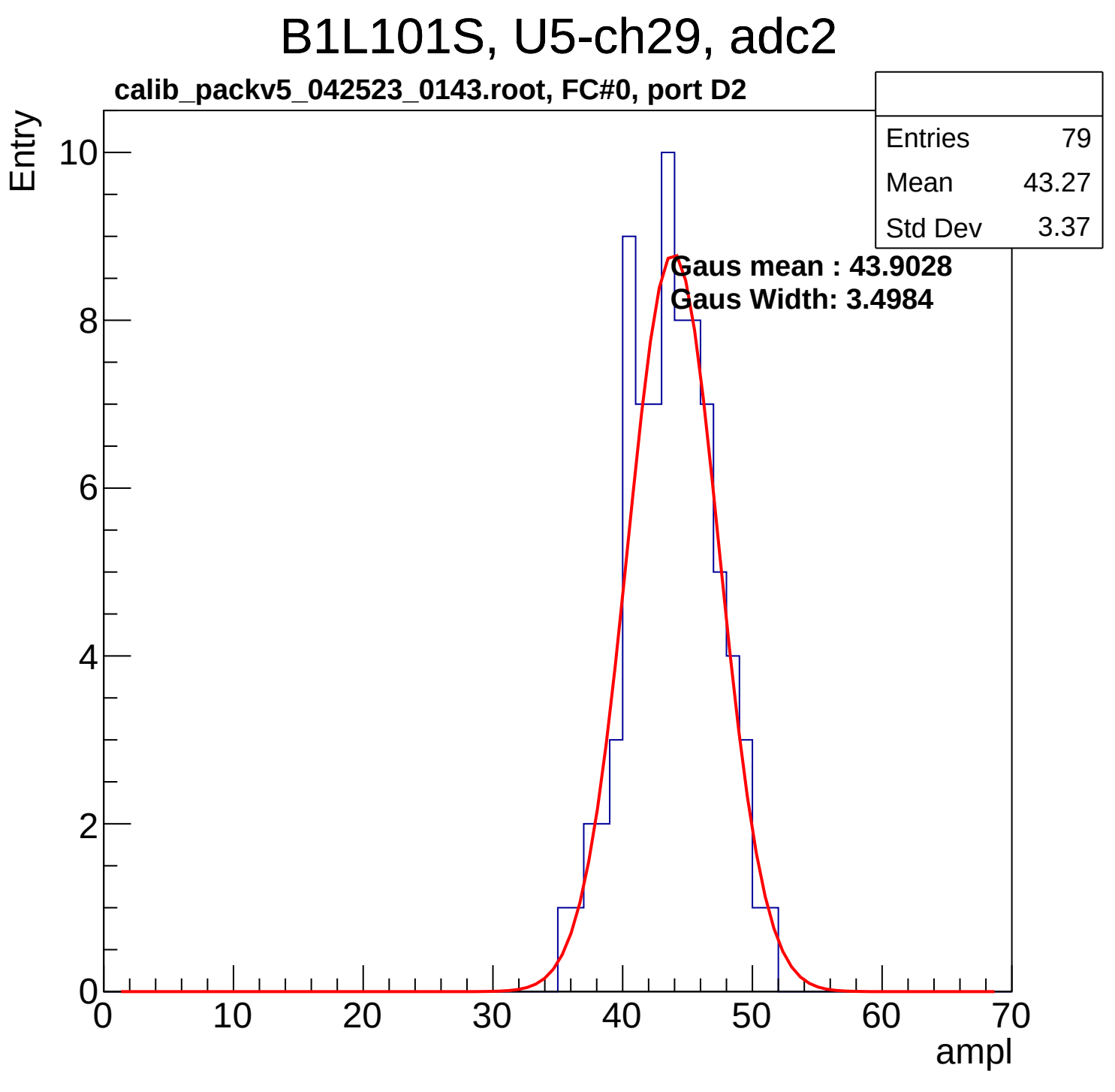
B1L101S, U5-ch29, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 43.27
Std Dev 3.37
Gaus mean : 43.9028
Gaus Width: 3.4984
Entry
ampl
0
2
4
6
8
10
0
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20
30
40
50
60
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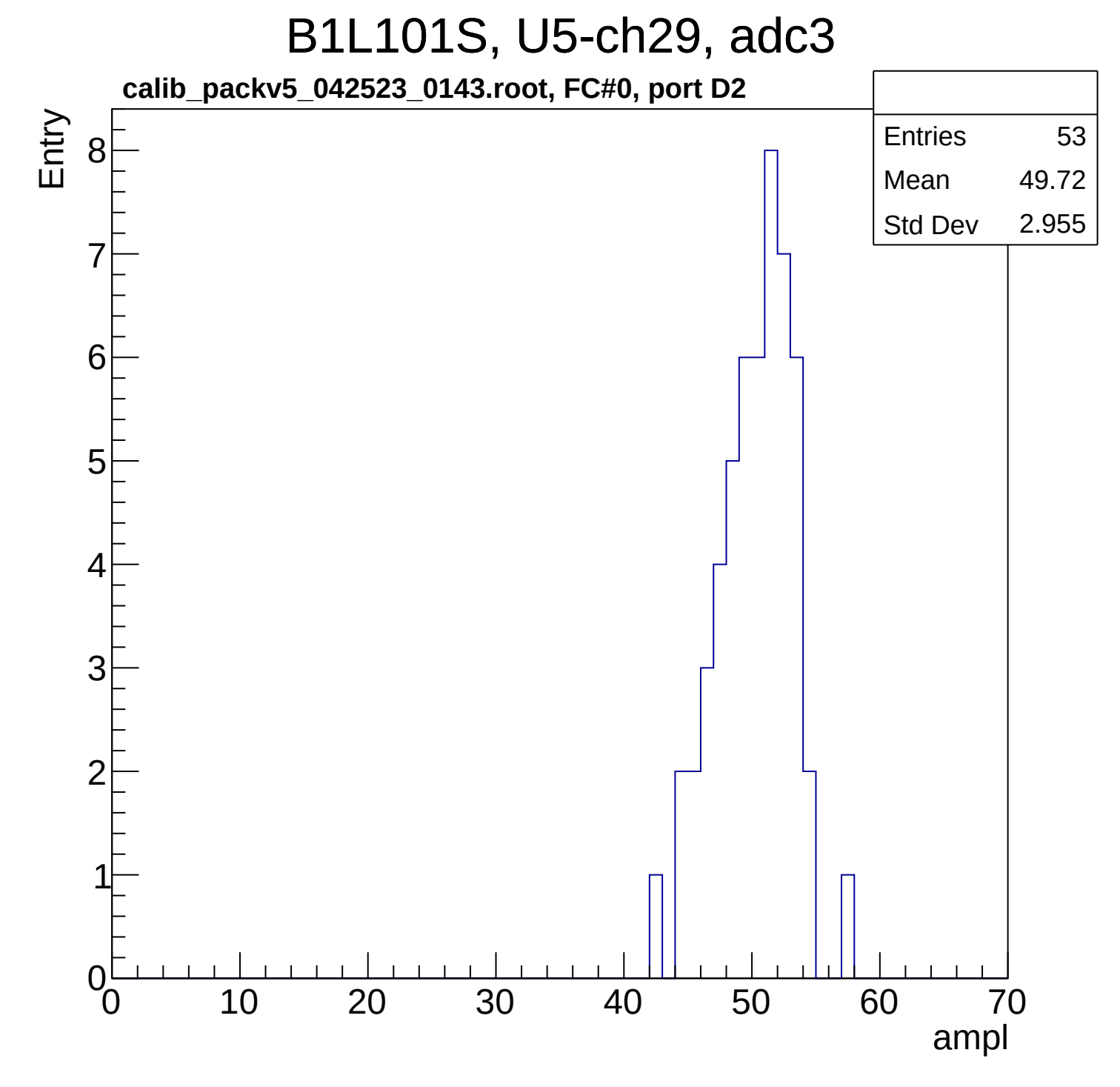
B1L101S, U5-ch29, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 49.72
Std Dev 2.955
Entry
ampl
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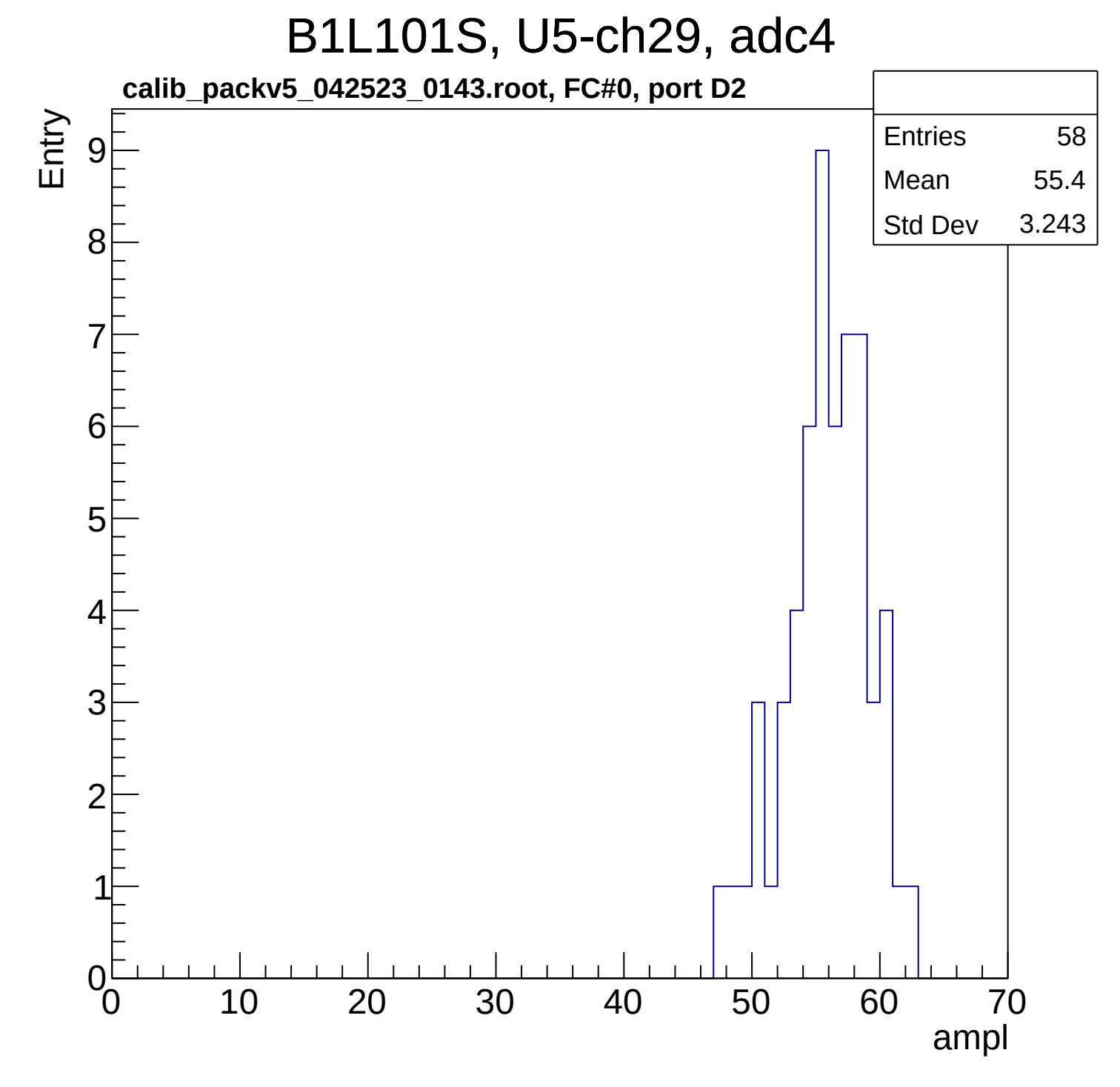
B1L101S, U5-ch29, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 55.4
Std Dev 3.243
Entry
ampl
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0
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60
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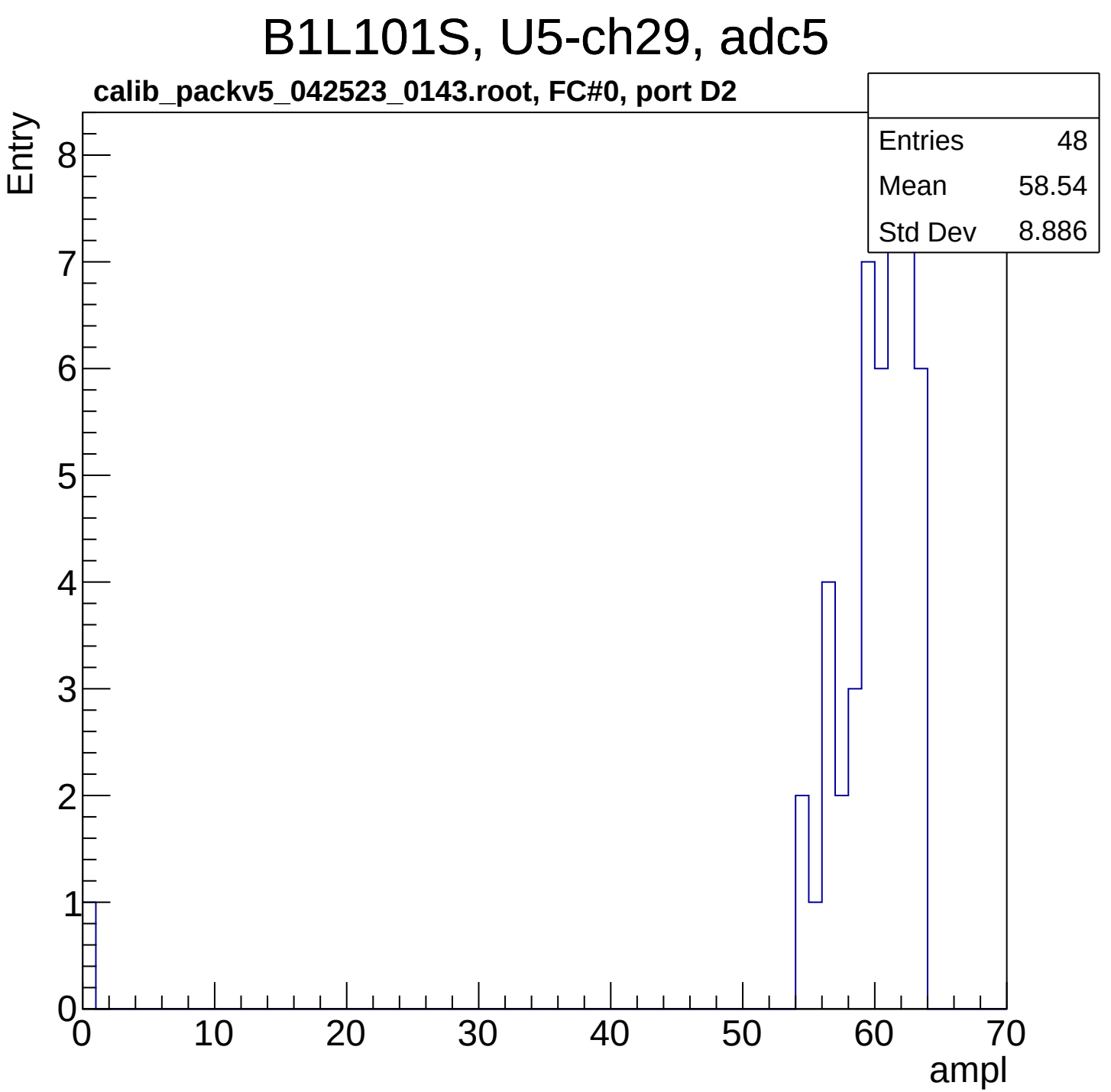
B1L101S, U5-ch29, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 58.54
Std Dev 8.886
Entry
ampl
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6
7
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0
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60
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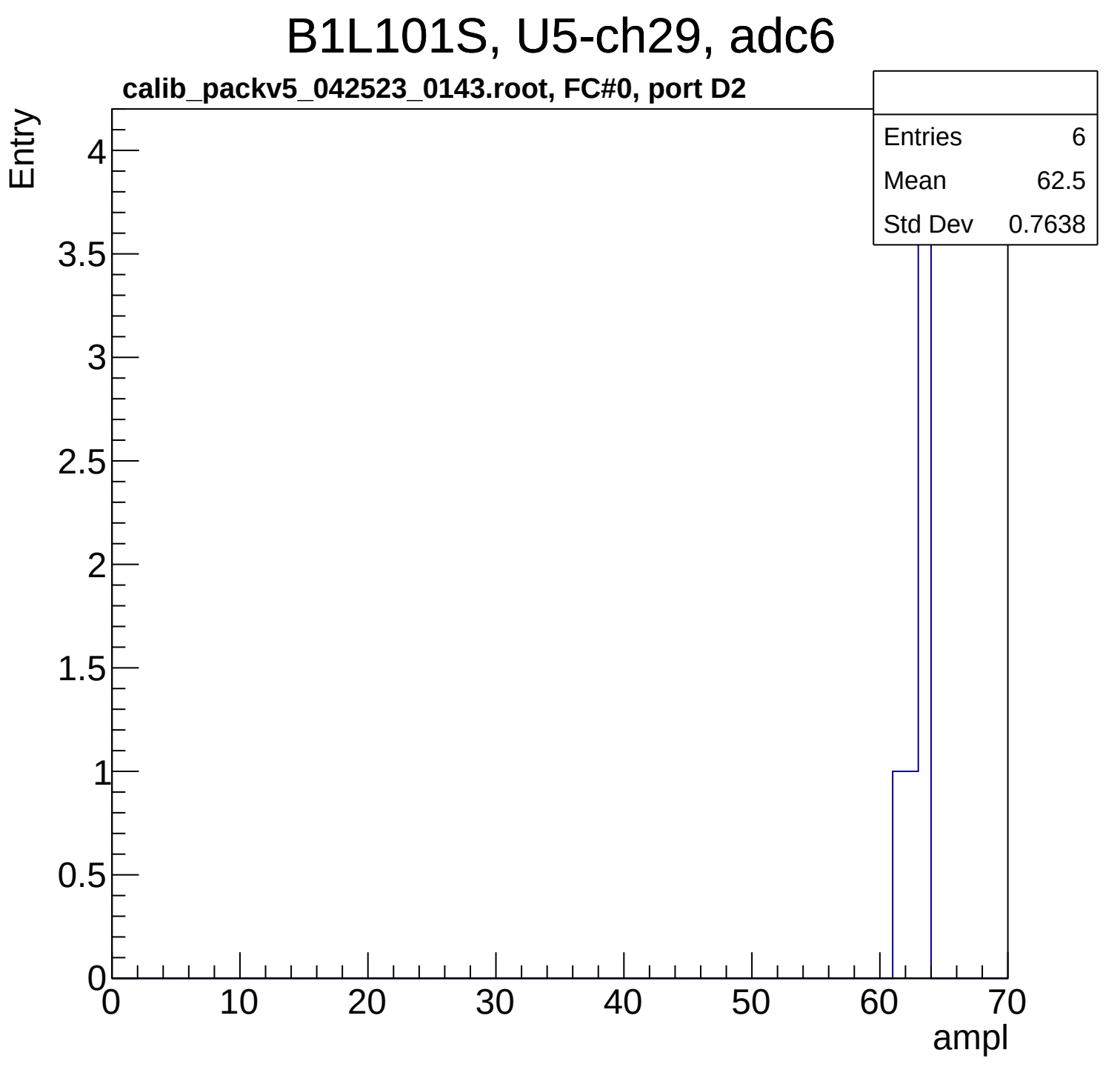
B1L101S, U5-ch29, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 62.5
Std Dev 0.7638
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
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20
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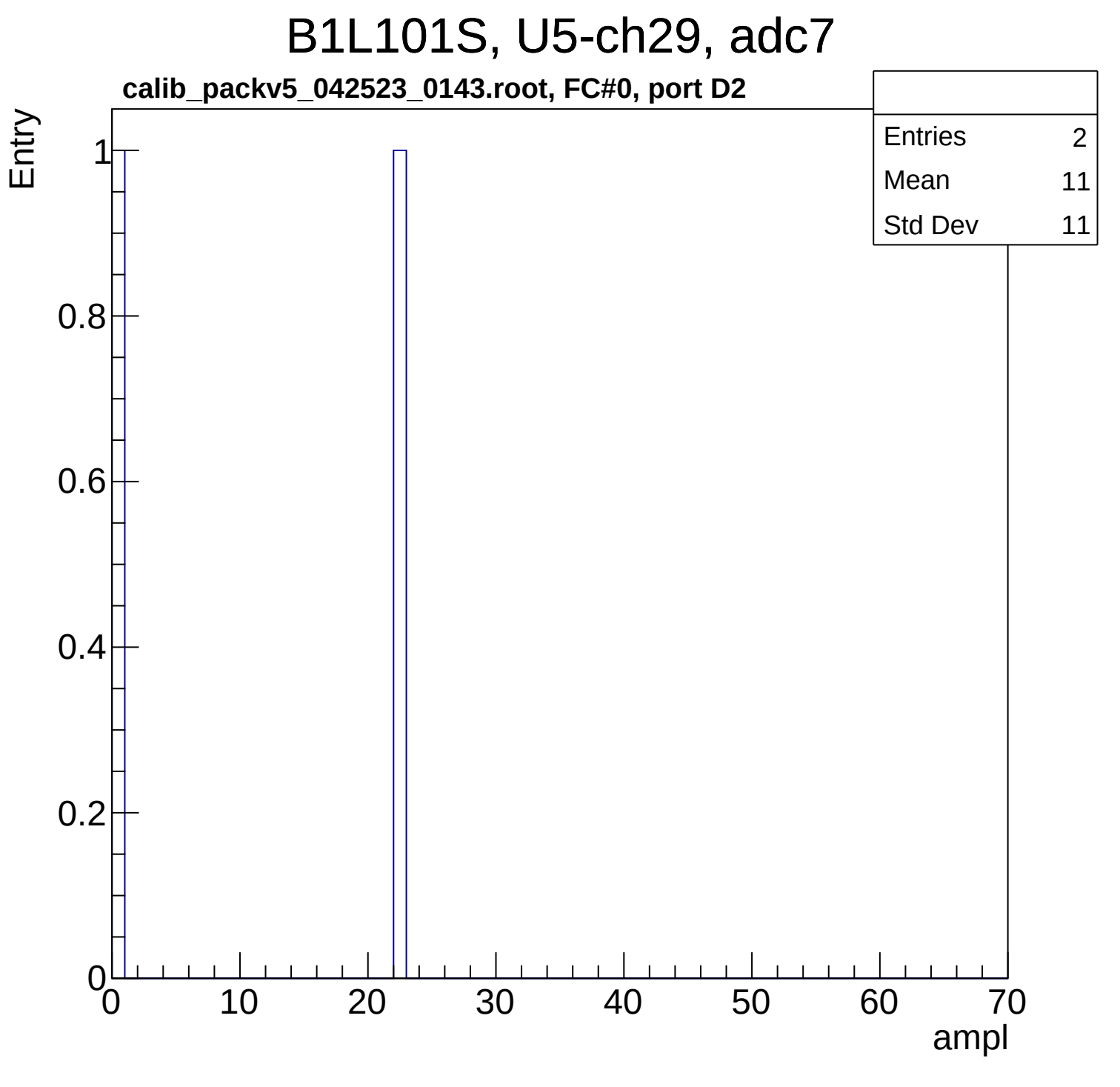
40
50
60
70


B1L101S, U5-ch29, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 11
Std Dev 11
Entry
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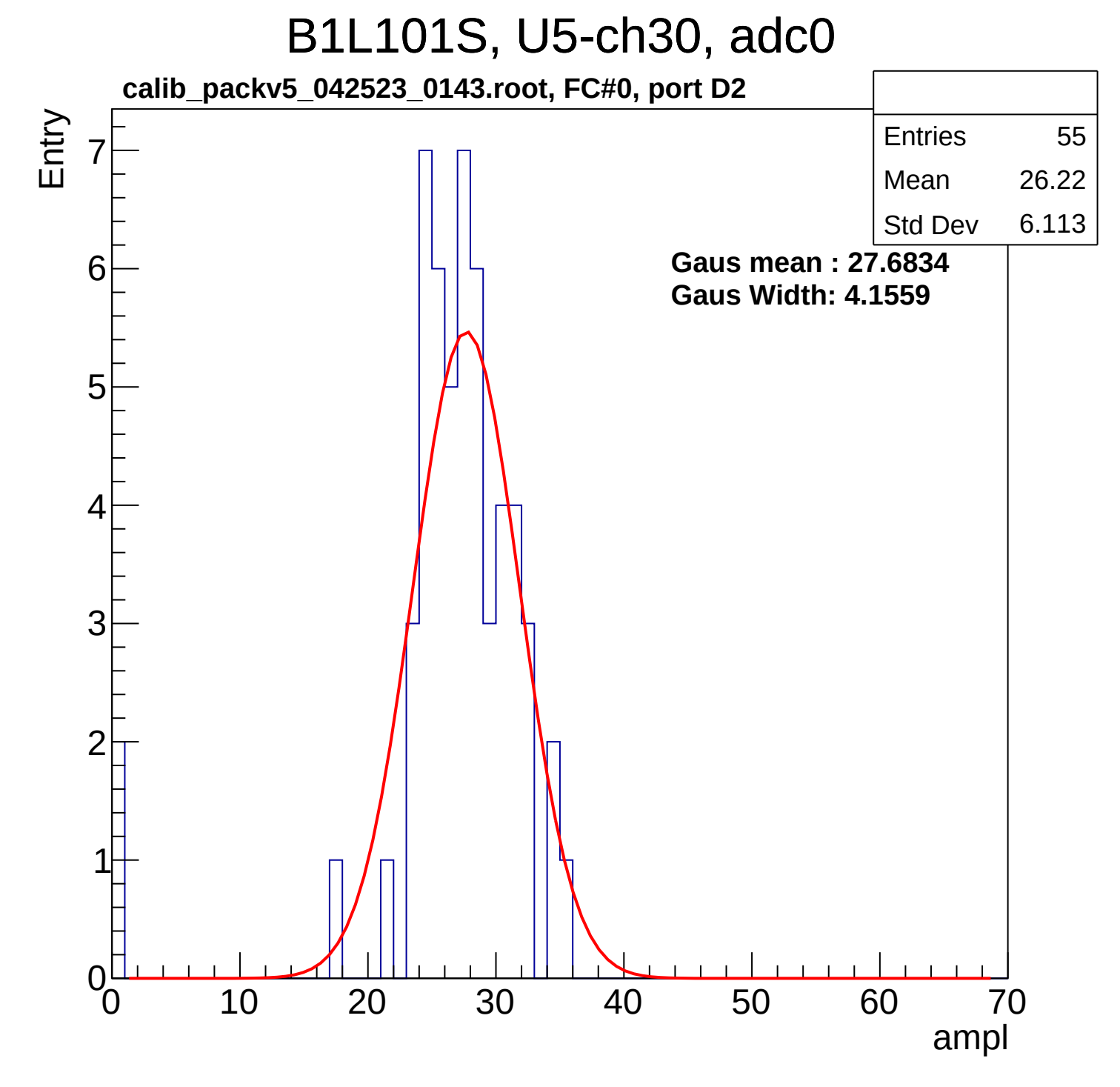
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch30, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 26.22
Std Dev 6.113
Gaus mean : 27.6834
Gaus Width: 4.1559
Entry
ampl
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1
2
3
4
5
6
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0
10
20
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40
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60
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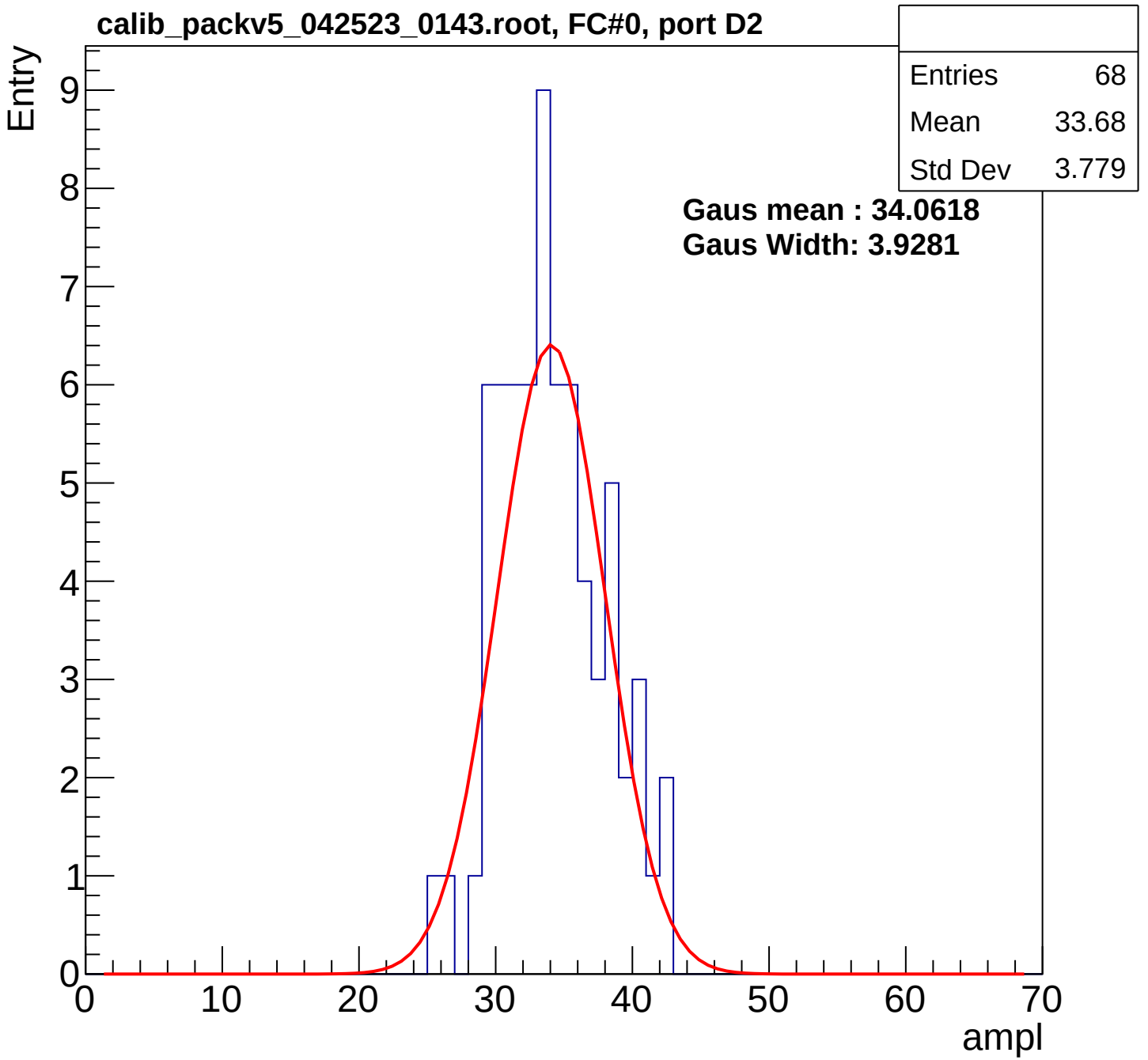
B1L101S, U5-ch30, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 33.68
Std Dev 3.779
Gaus mean : 34.0618
Gaus Width: 3.9281
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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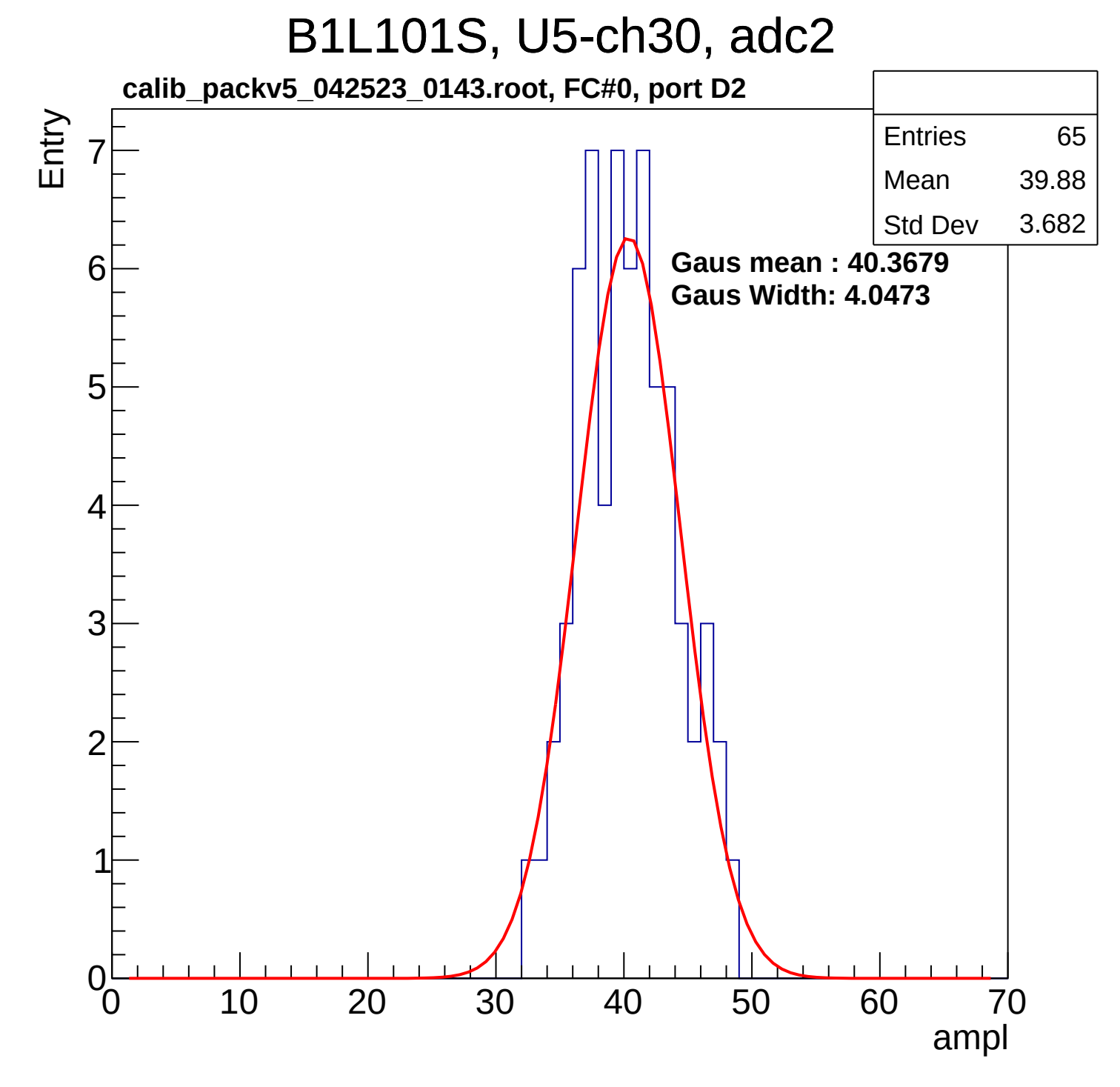
B1L101S, U5-ch30, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 39.88
Std Dev 3.682
Gaus mean : 40.3679
Gaus Width: 4.0473
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
30
40
50
60
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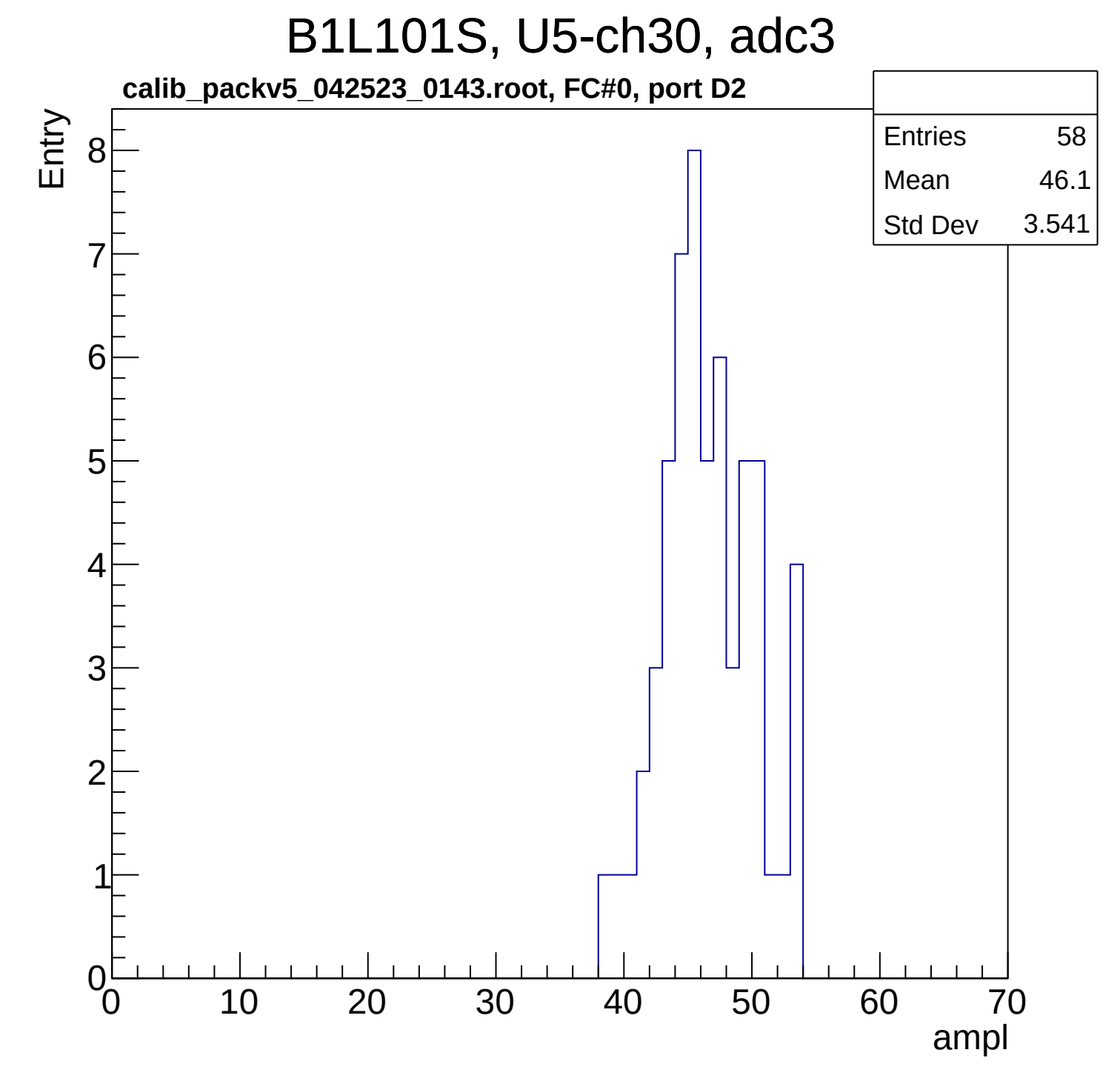
B1L101S, U5-ch30, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 46.1
Std Dev 3.541
Entry
ampl
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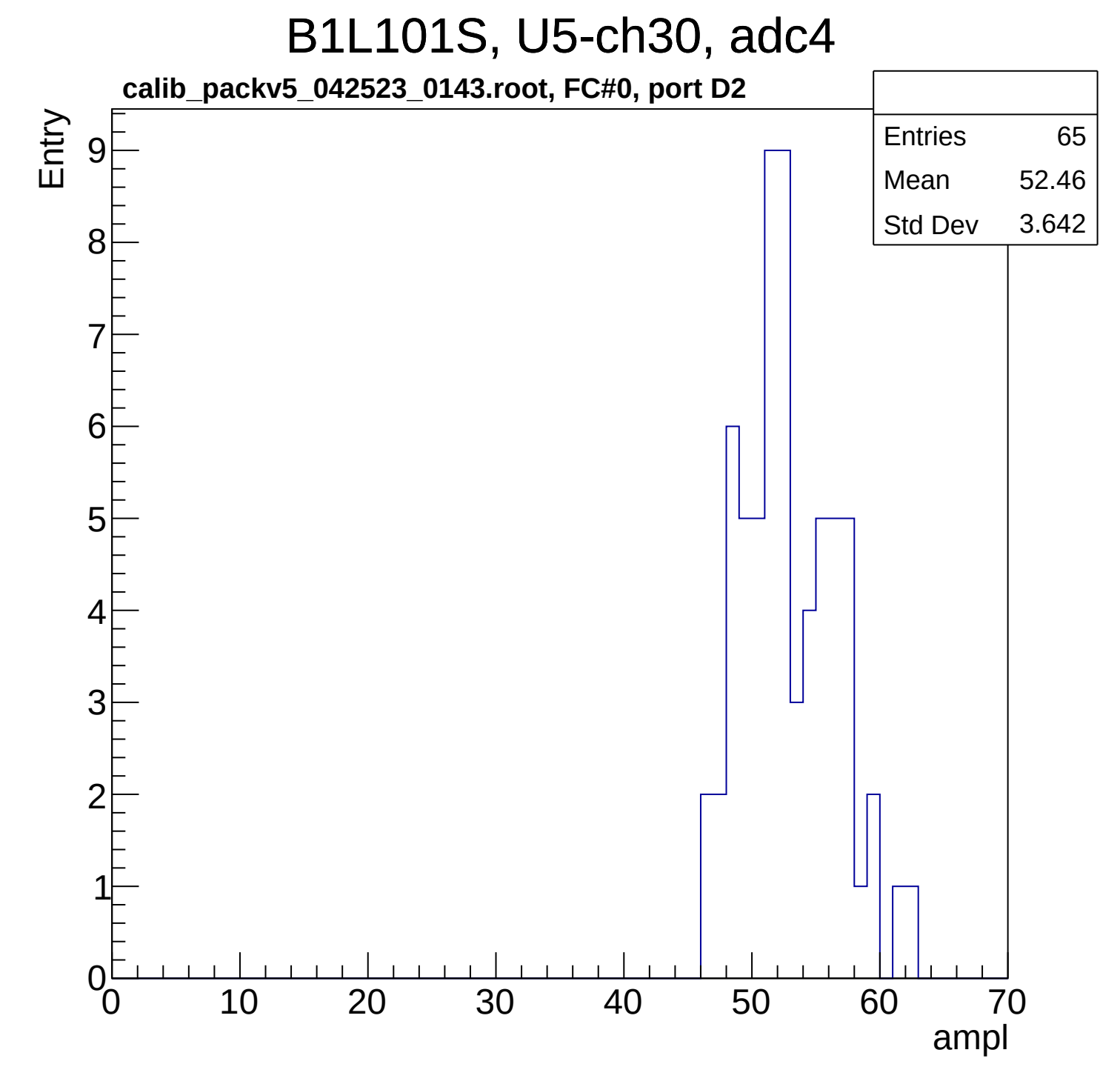
B1L101S, U5-ch30, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 52.46
Std Dev 3.642
Entry
ampl
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3
4
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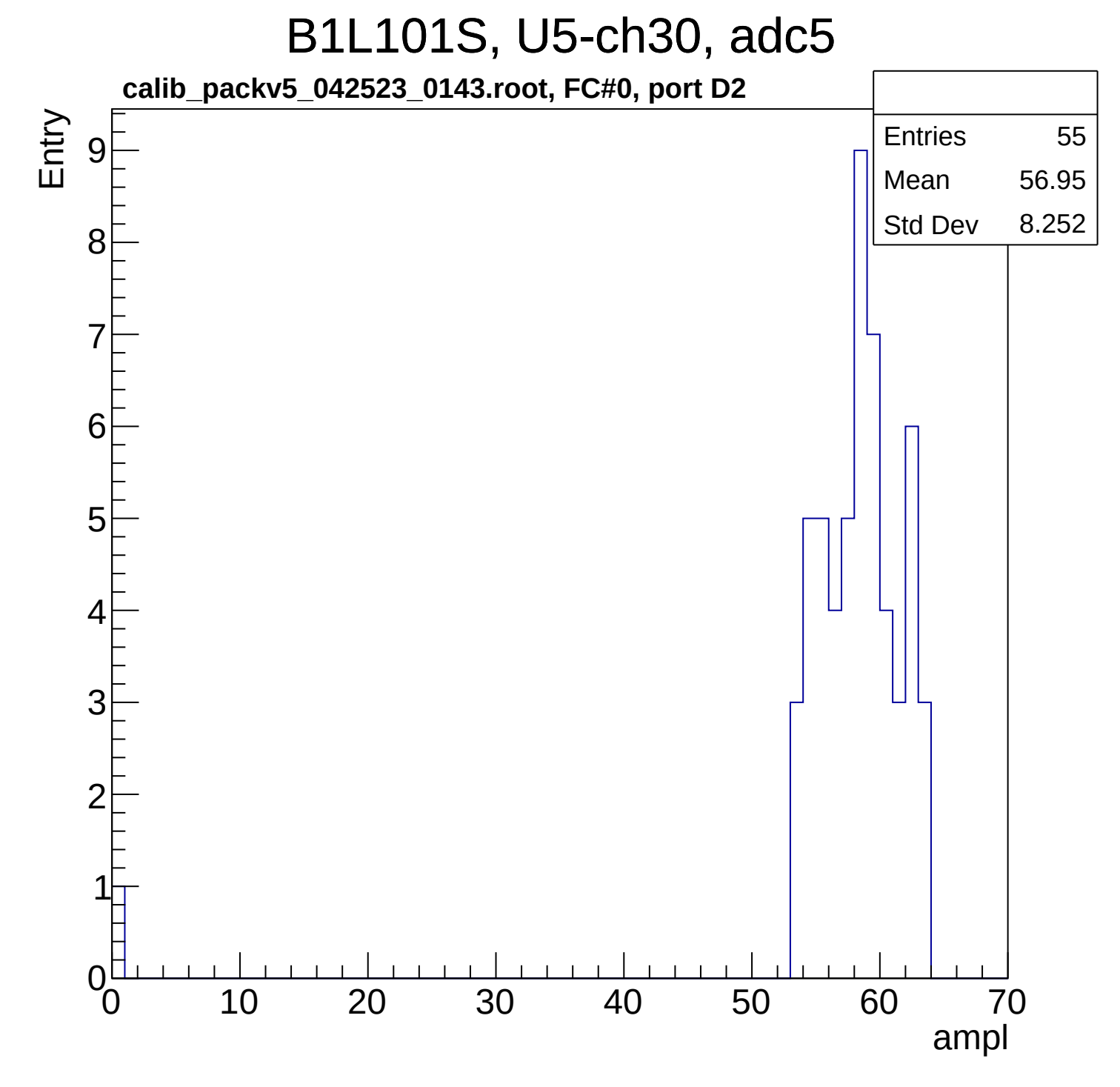
B1L101S, U5-ch30, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 56.95
Std Dev 8.252
Entry
ampl
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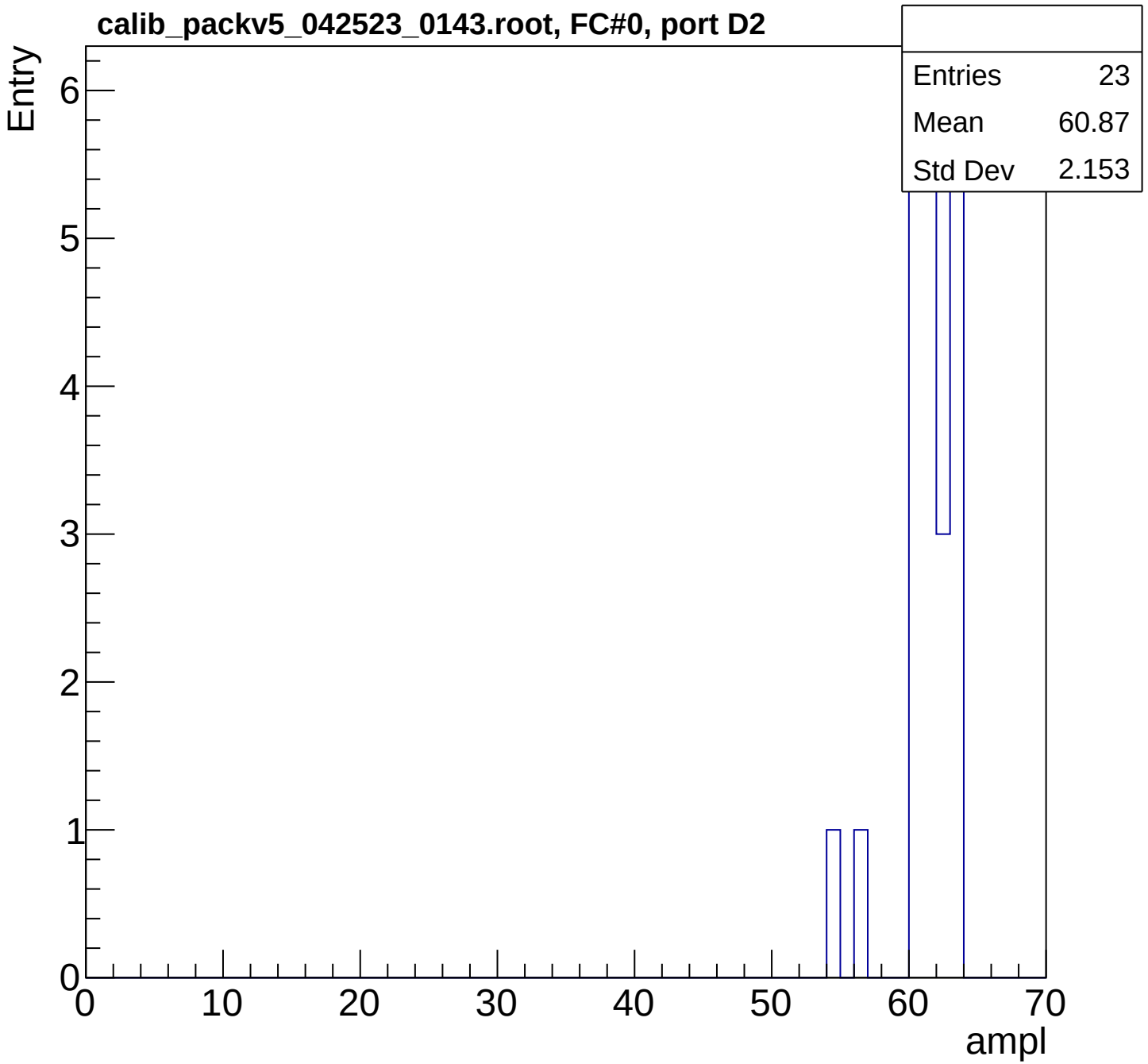
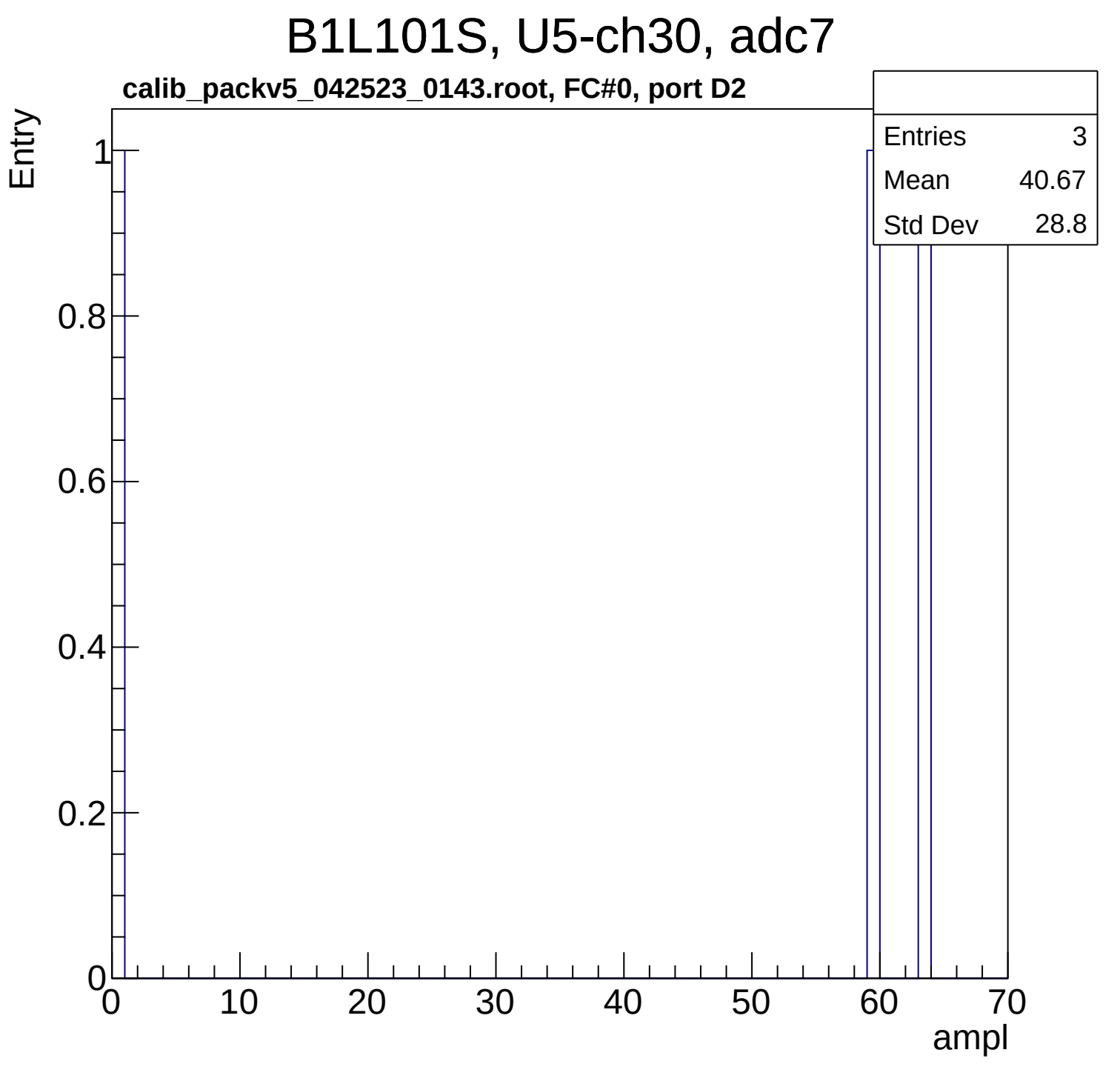

B1L101S, U5-ch30, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 23
Mean 60.87
Std Dev 2.153
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch30, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 40.67
Std Dev 28.8
Entry
ampl
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0.2
0.4
0.6
0.8
1
0
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60
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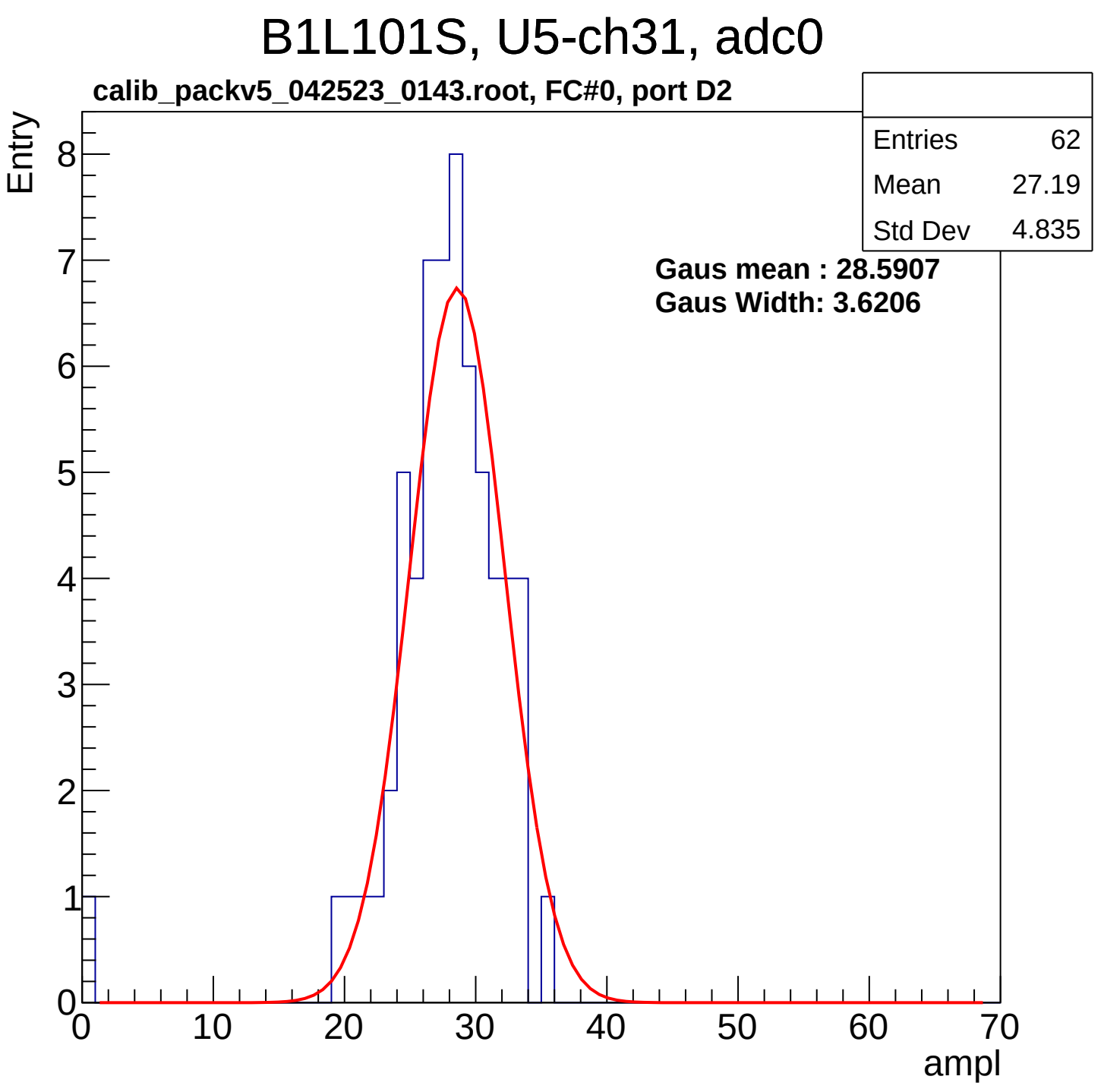
B1L101S, U5-ch31, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 27.19
Std Dev 4.835
Gaus mean : 28.5907
Gaus Width: 3.6206
Entry
ampl
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1
2
3
4
5
6
7
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0
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40
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60
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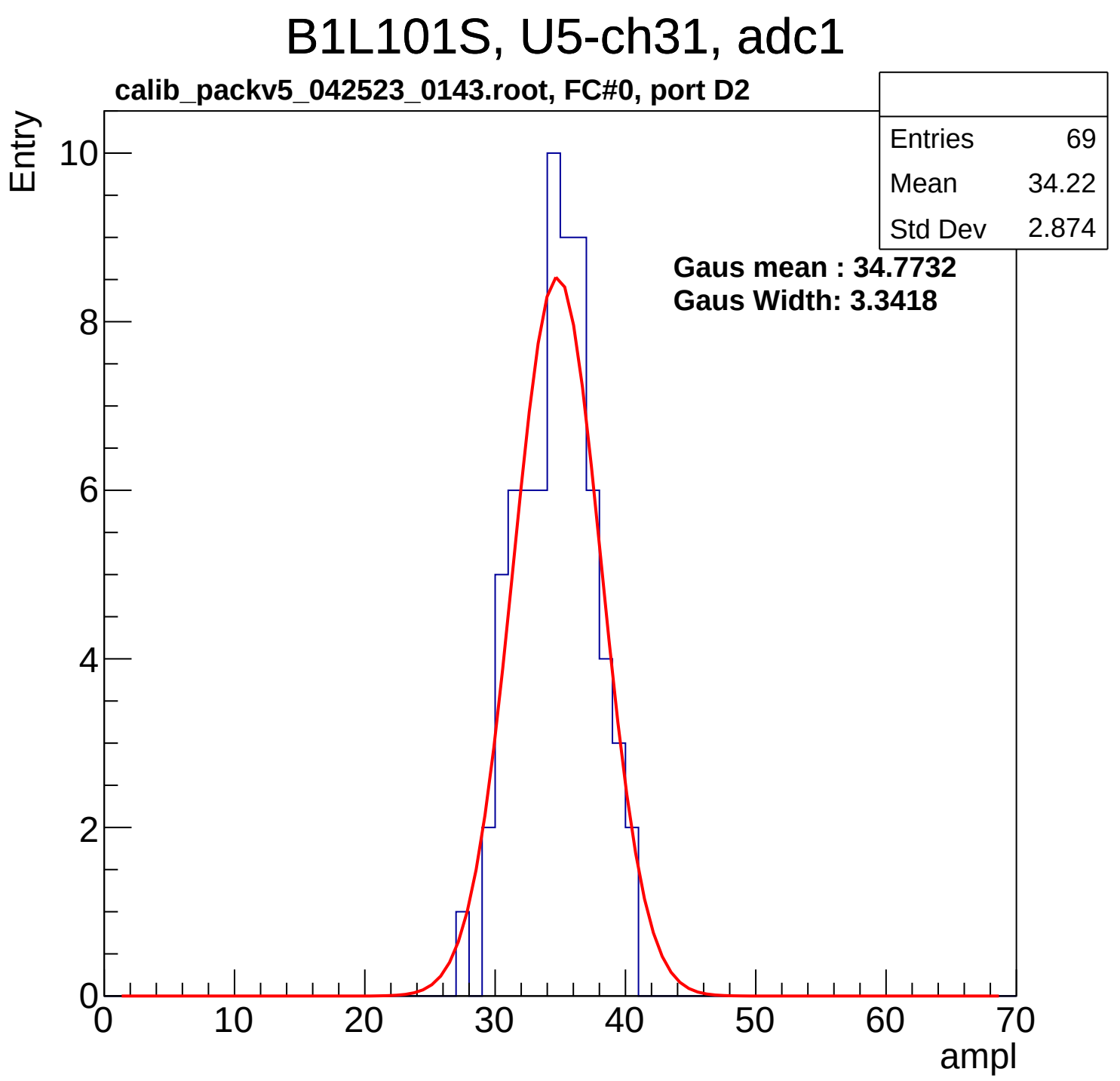
B1L101S, U5-ch31, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 34.22
Std Dev 2.874
Gaus mean : 34.7732
Gaus Width: 3.3418
Entry
ampl
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2
4
6
8
10
0
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20
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40
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60
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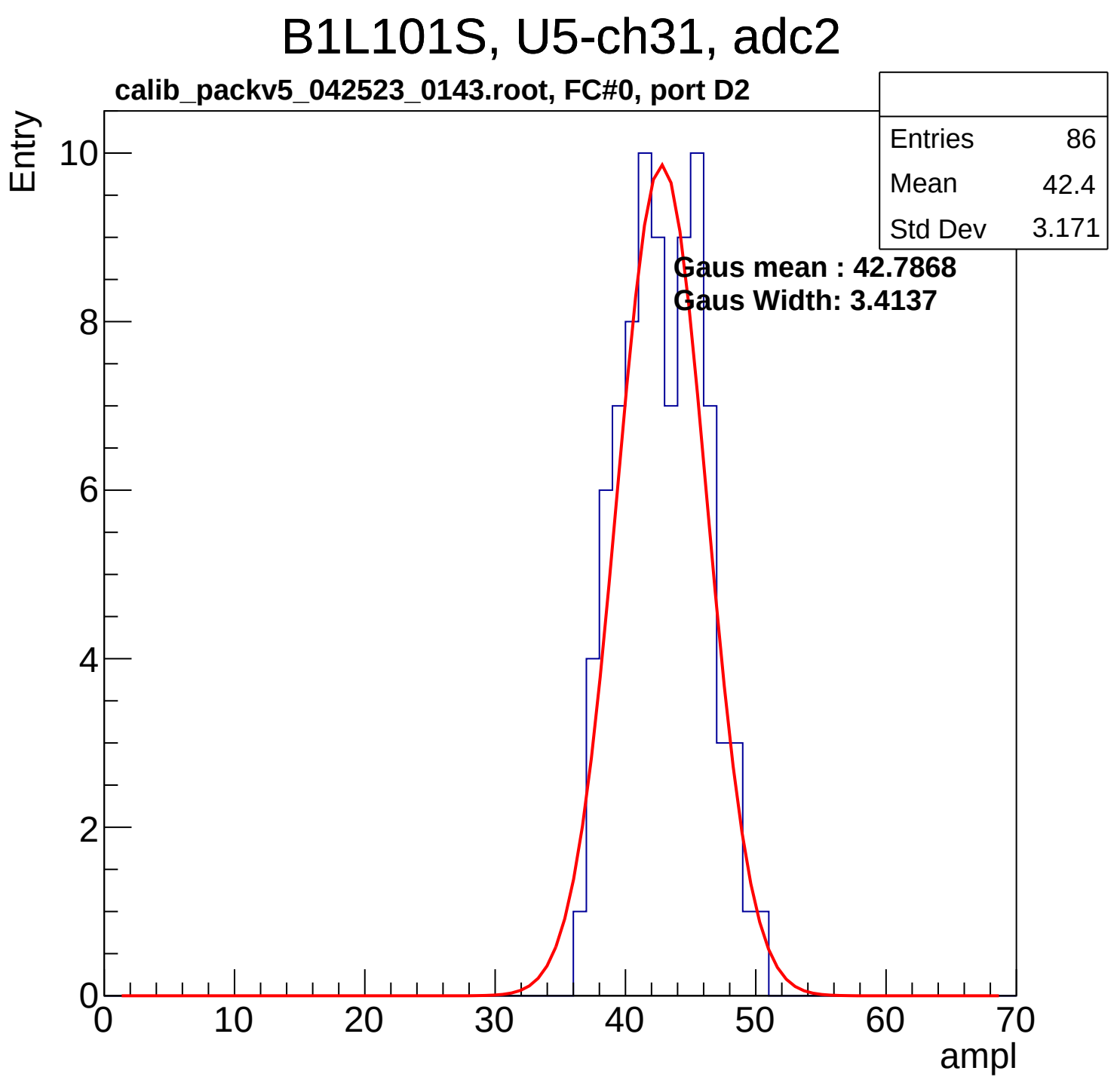
B1L101S, U5-ch31, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 86
Mean 42.4
Std Dev 3.171
Gaus mean : 42.7868
Gaus Width: 3.4137
Entry
ampl
0
2
4
6
8
10
0
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20
30
40
50
60
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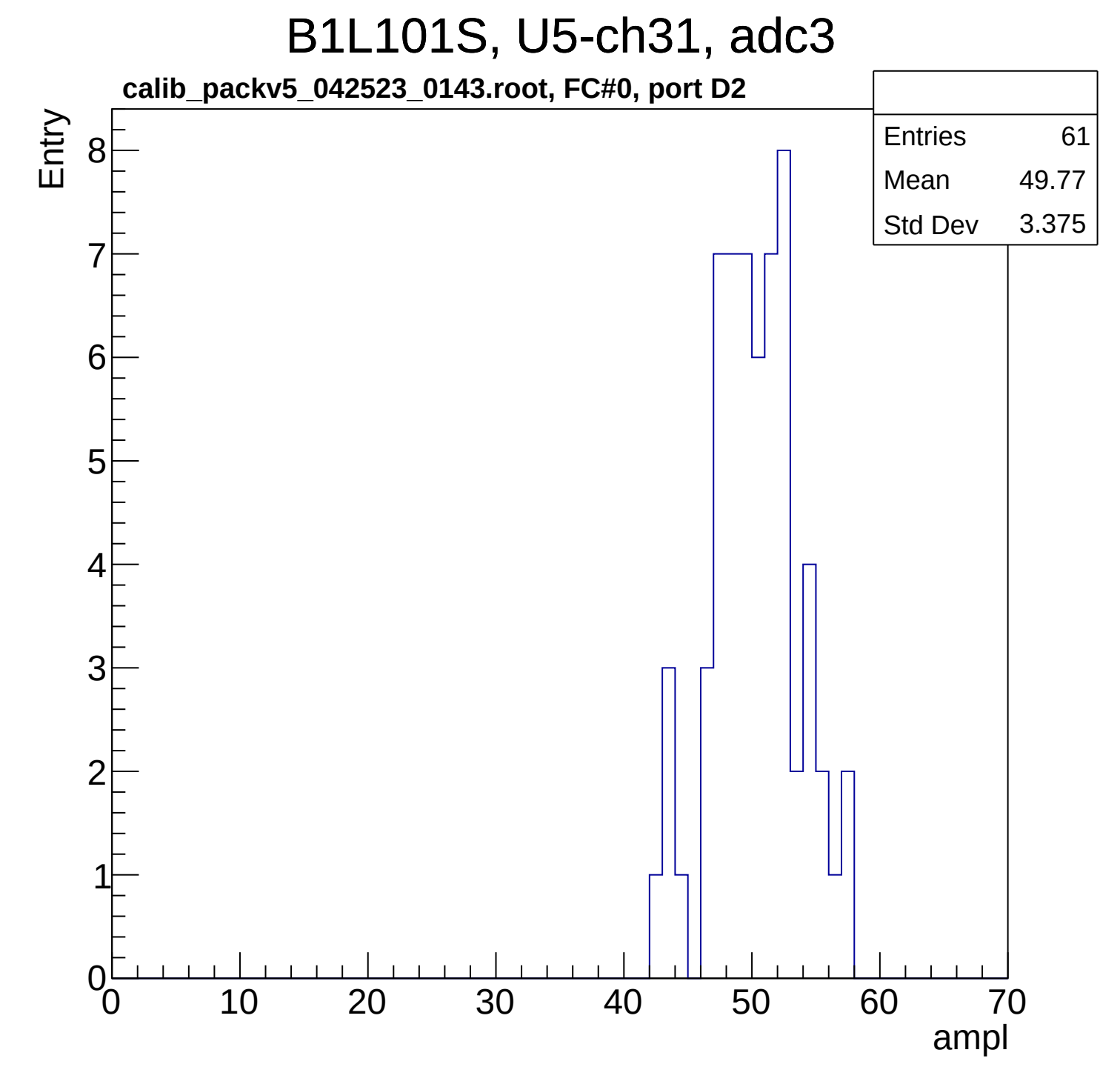
B1L101S, U5-ch31, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 49.77
Std Dev 3.375
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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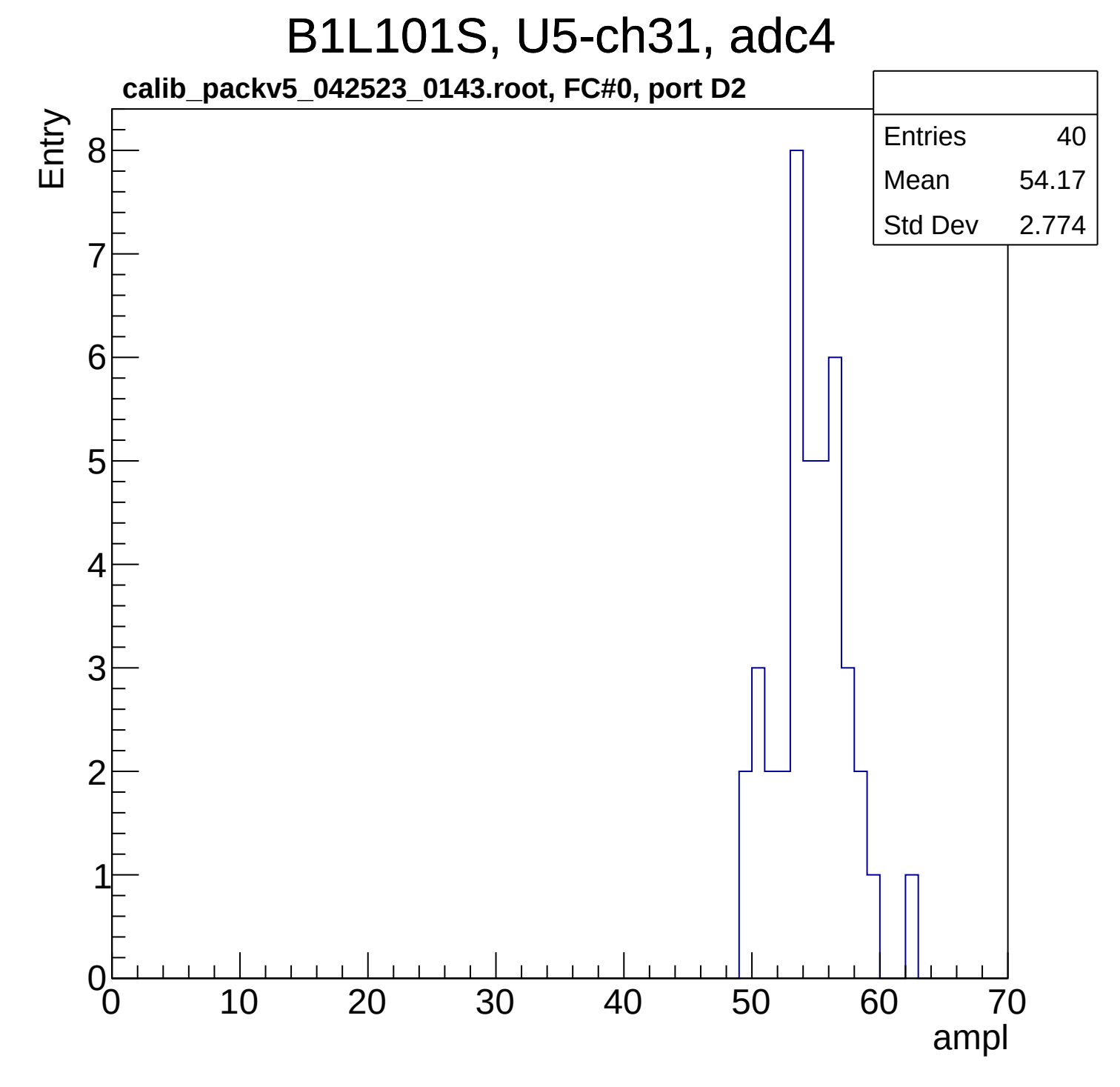
B1L101S, U5-ch31, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 40
Mean 54.17
Std Dev 2.774
Entry
ampl
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1
2
3
4
5
6
7
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0
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60
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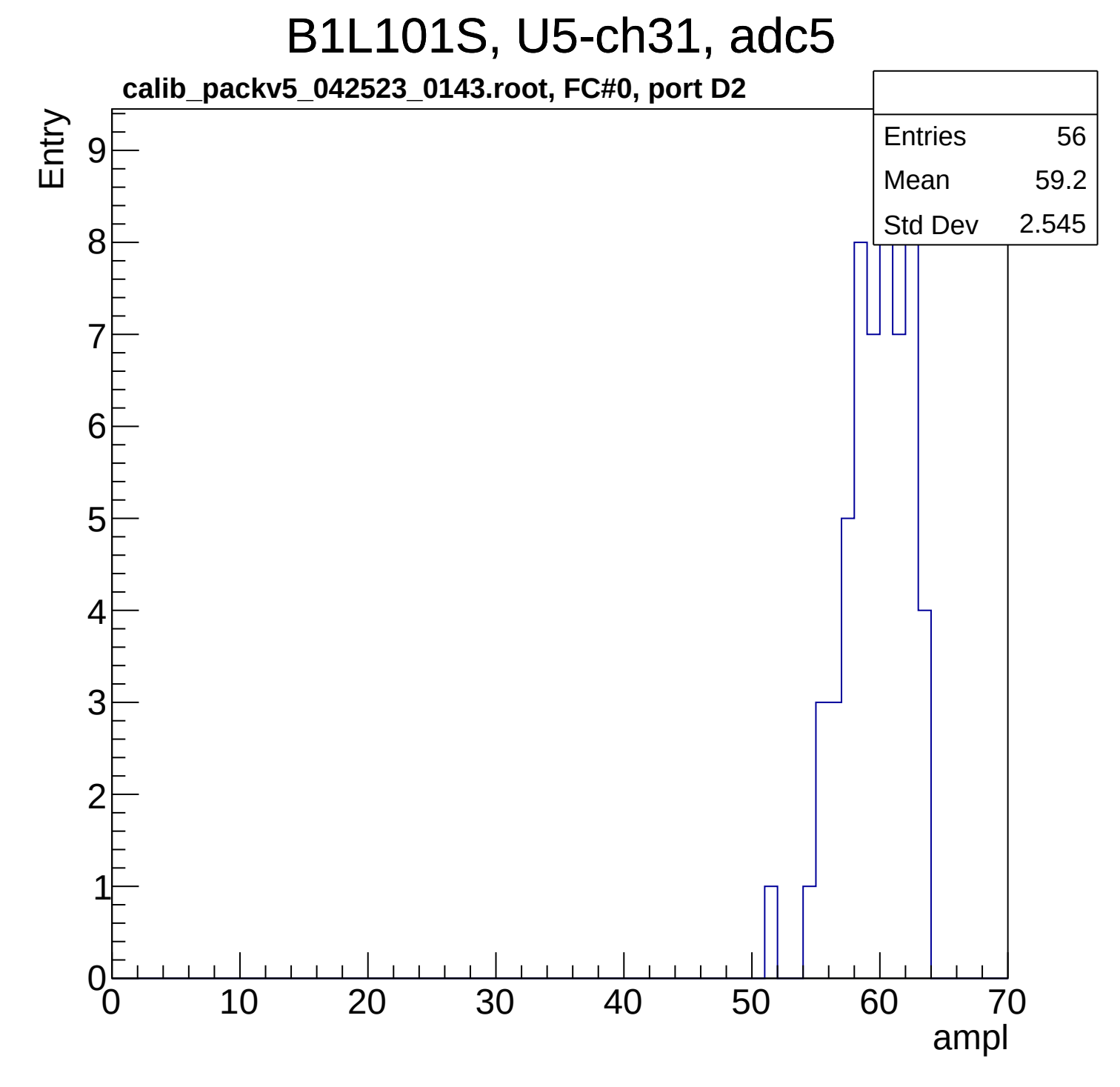
B1L101S, U5-ch31, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 59.2
Std Dev 2.545
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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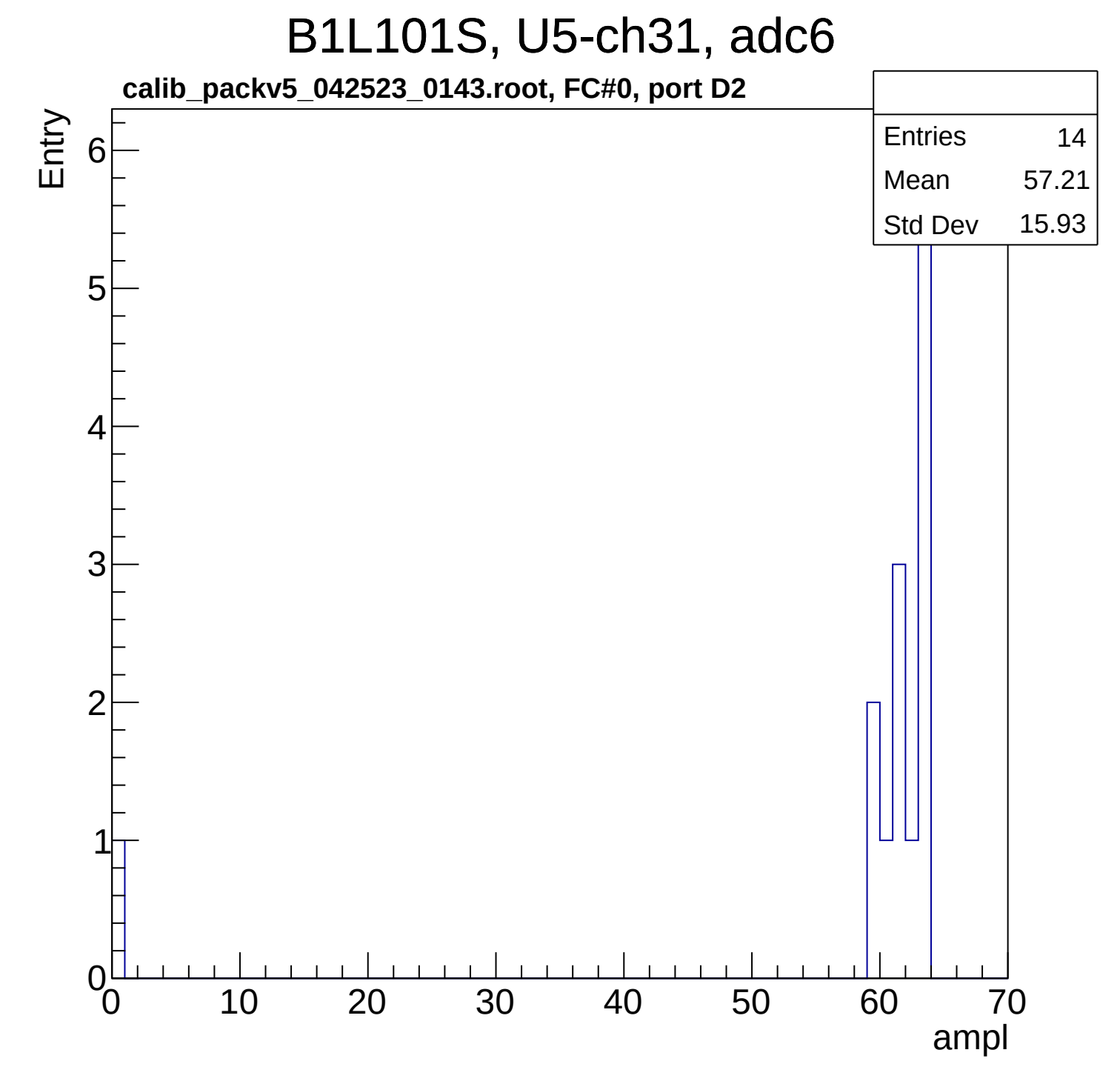
B1L101S, U5-ch31, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 14
Mean 57.21
Std Dev 15.93
Entry
ampl
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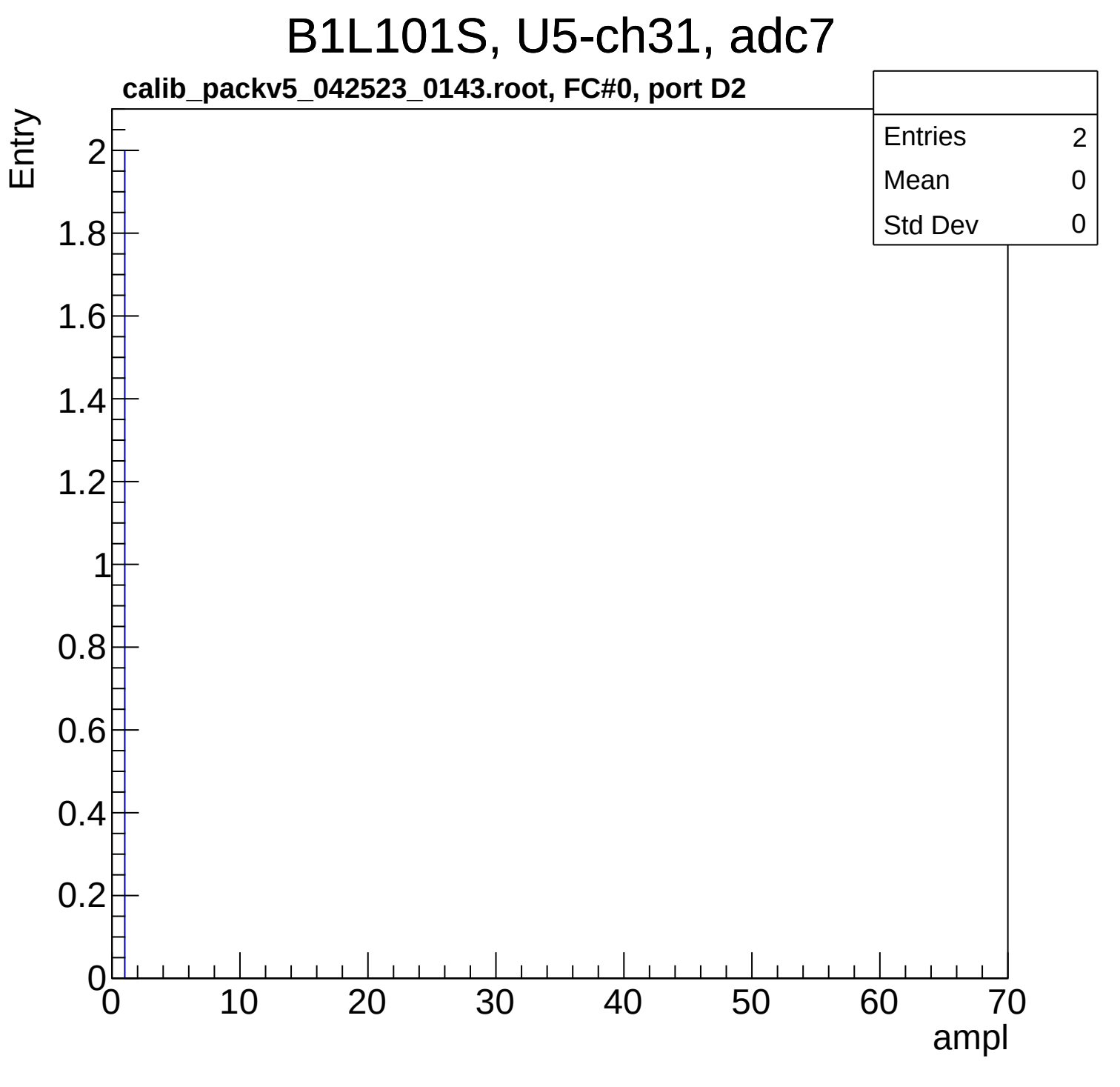
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L101S, U5-ch31, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
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1.2
1.4
1.6
1.8
2
0
10
20
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40
50
60
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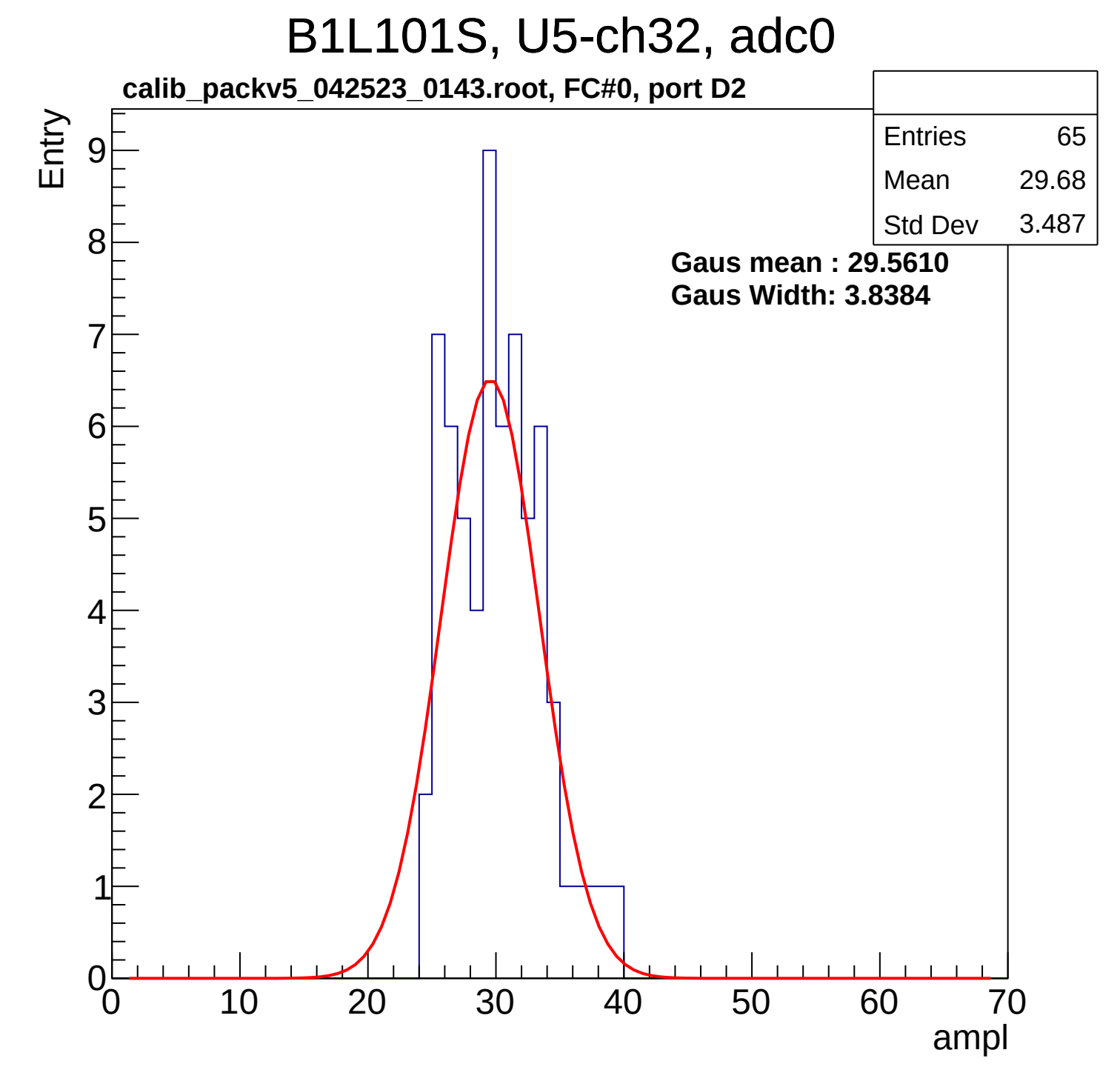
B1L101S, U5-ch32, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 29.68
Std Dev 3.487
Gaus mean : 29.5610
Gaus Width: 3.8384
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
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40
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60
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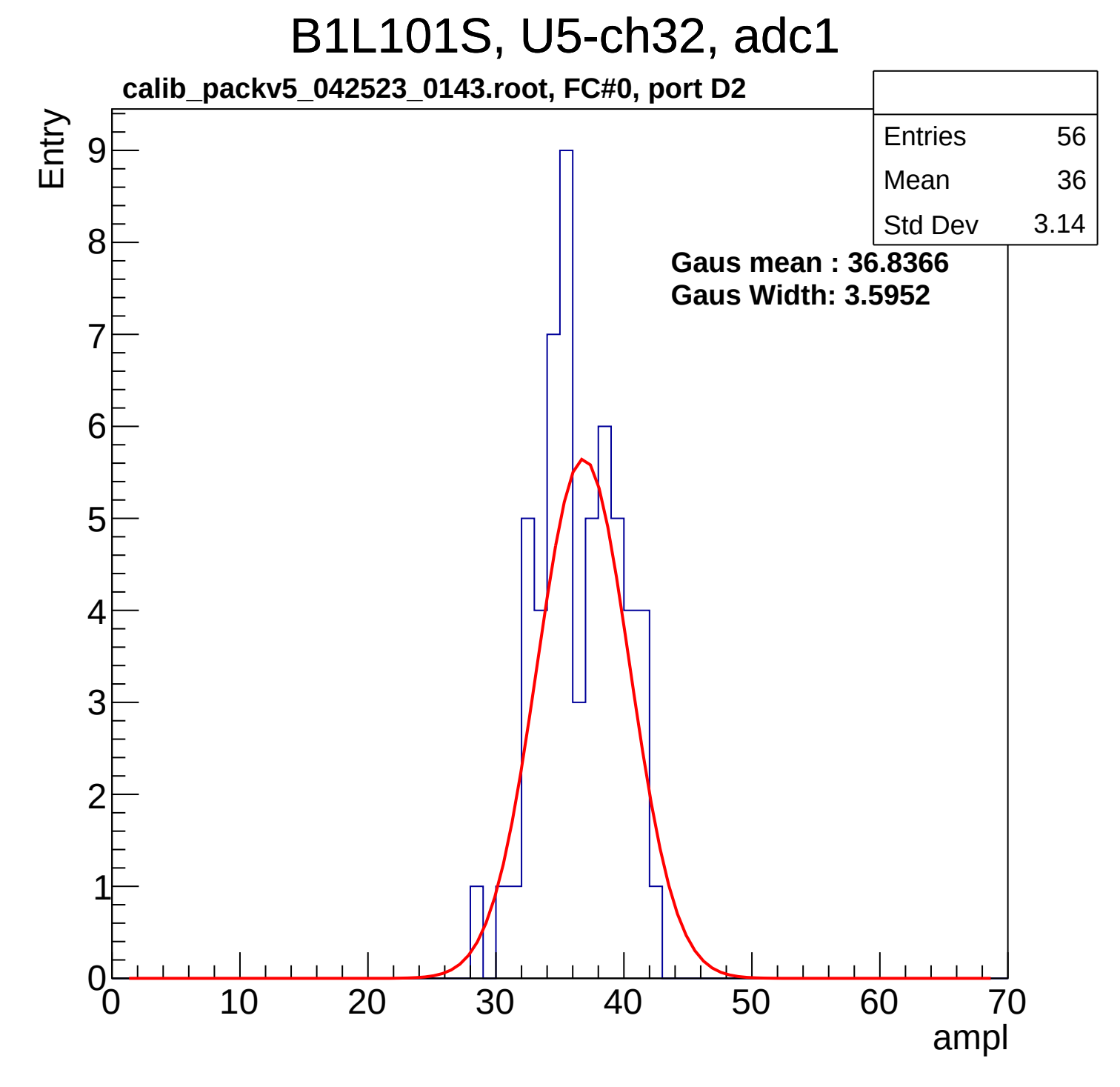
B1L101S, U5-ch32, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 36
Std Dev 3.14
Gaus mean : 36.8366
Gaus Width: 3.5952
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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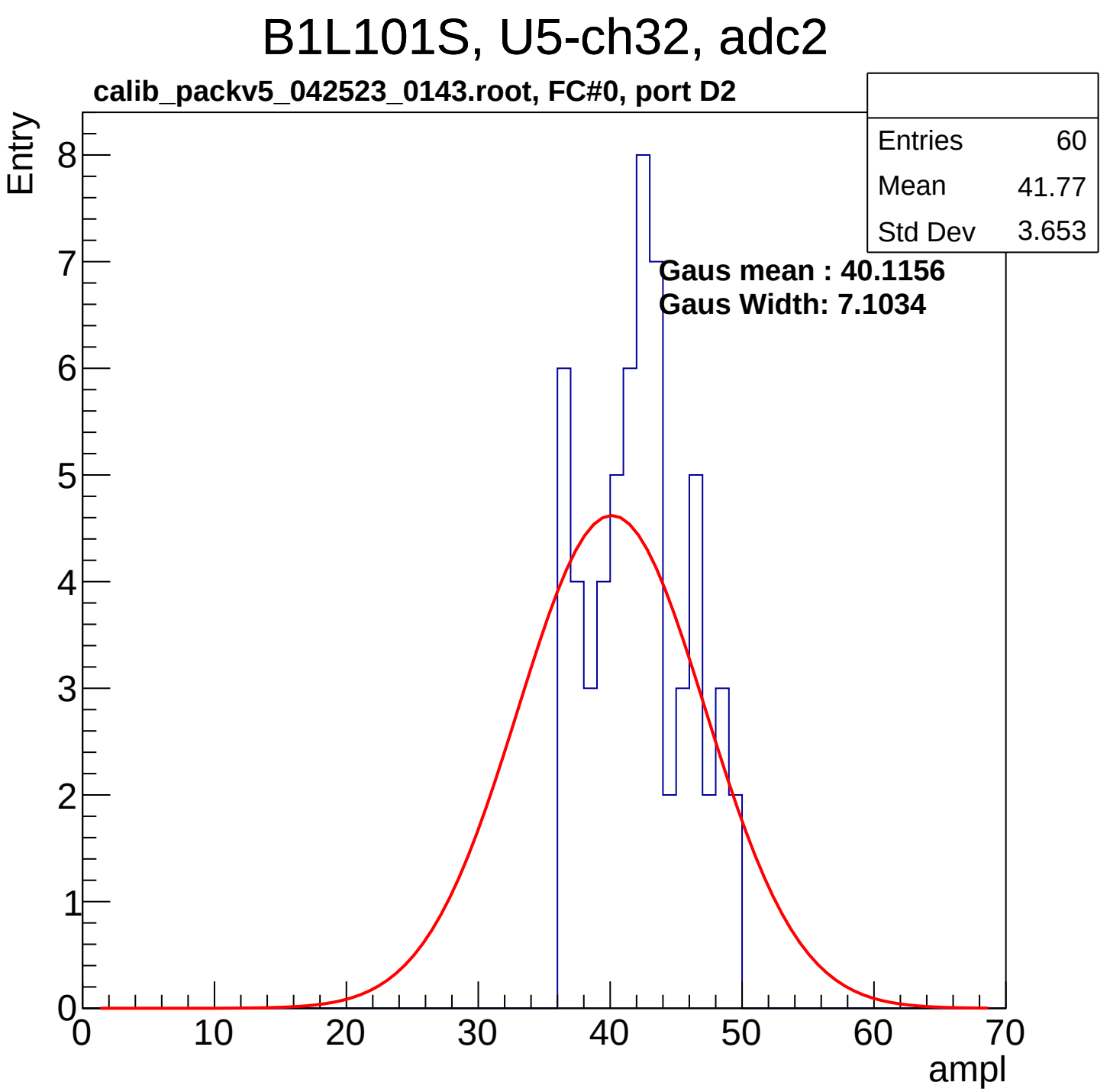
B1L101S, U5-ch32, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 41.77
Std Dev 3.653
Gaus mean : 40.1156
Gaus Width: 7.1034
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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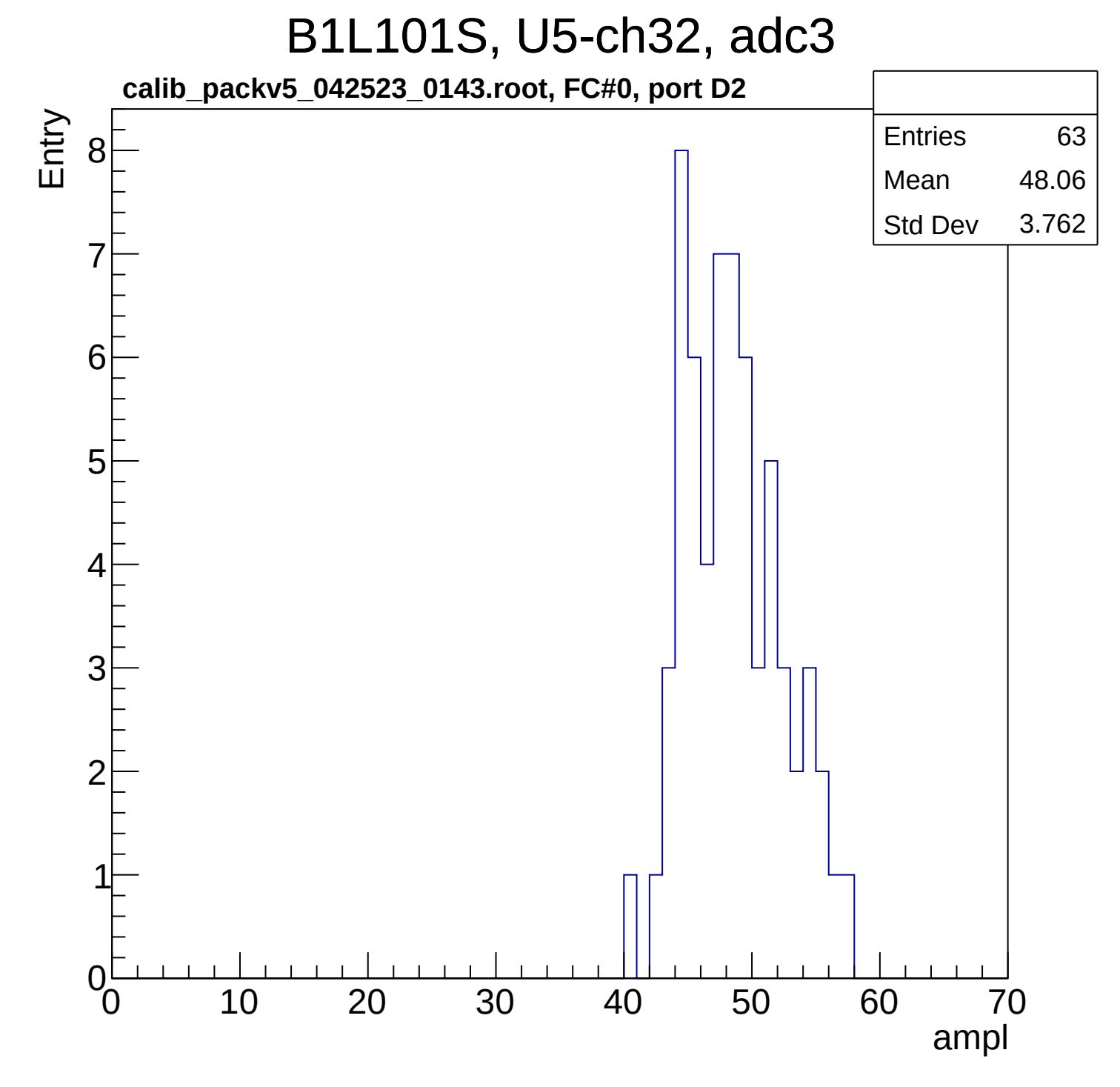
B1L101S, U5-ch32, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 48.06
Std Dev 3.762
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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60
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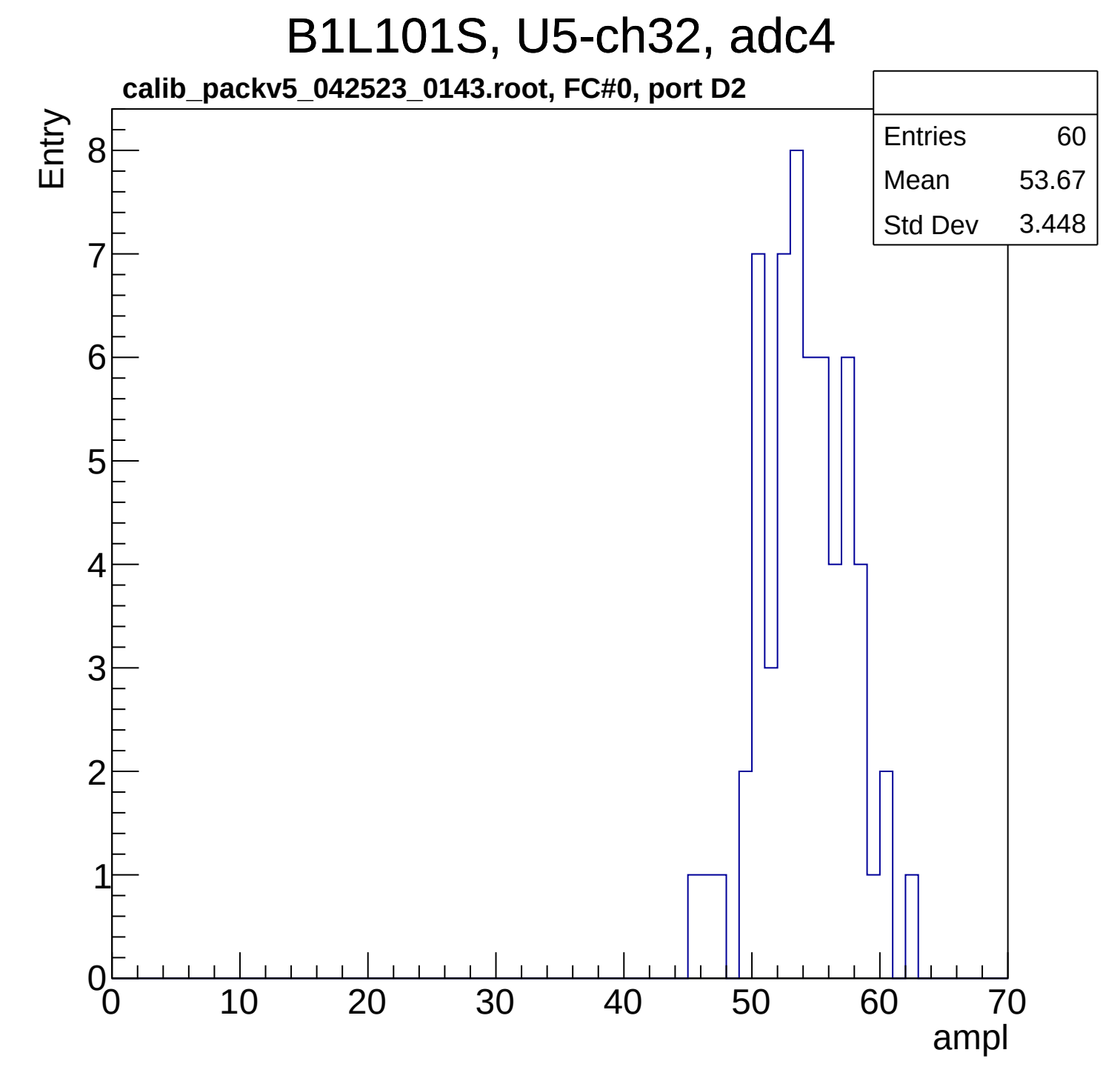
B1L101S, U5-ch32, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 53.67
Std Dev 3.448
Entry
ampl
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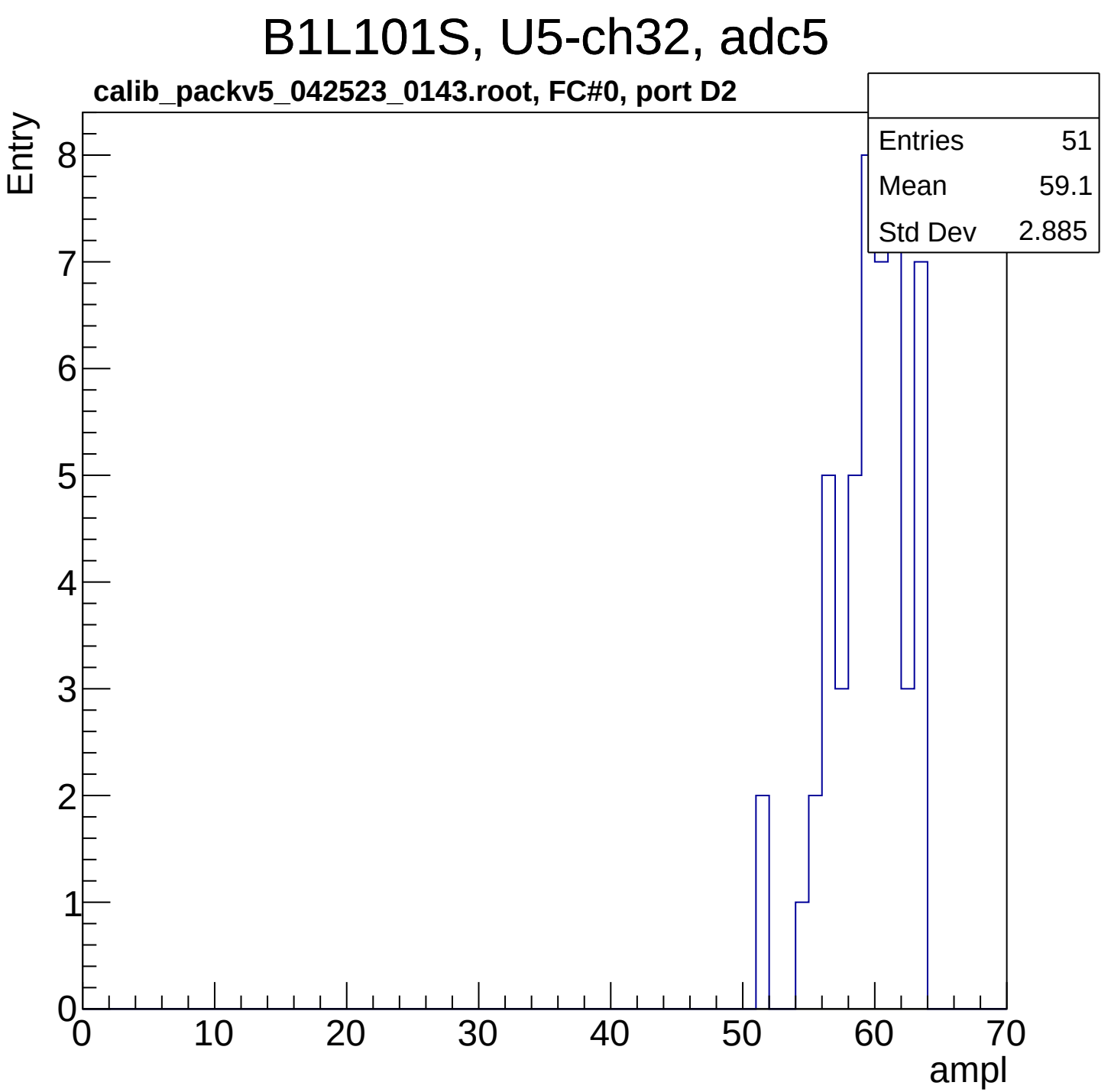
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch32, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 59.1
Std Dev 2.885
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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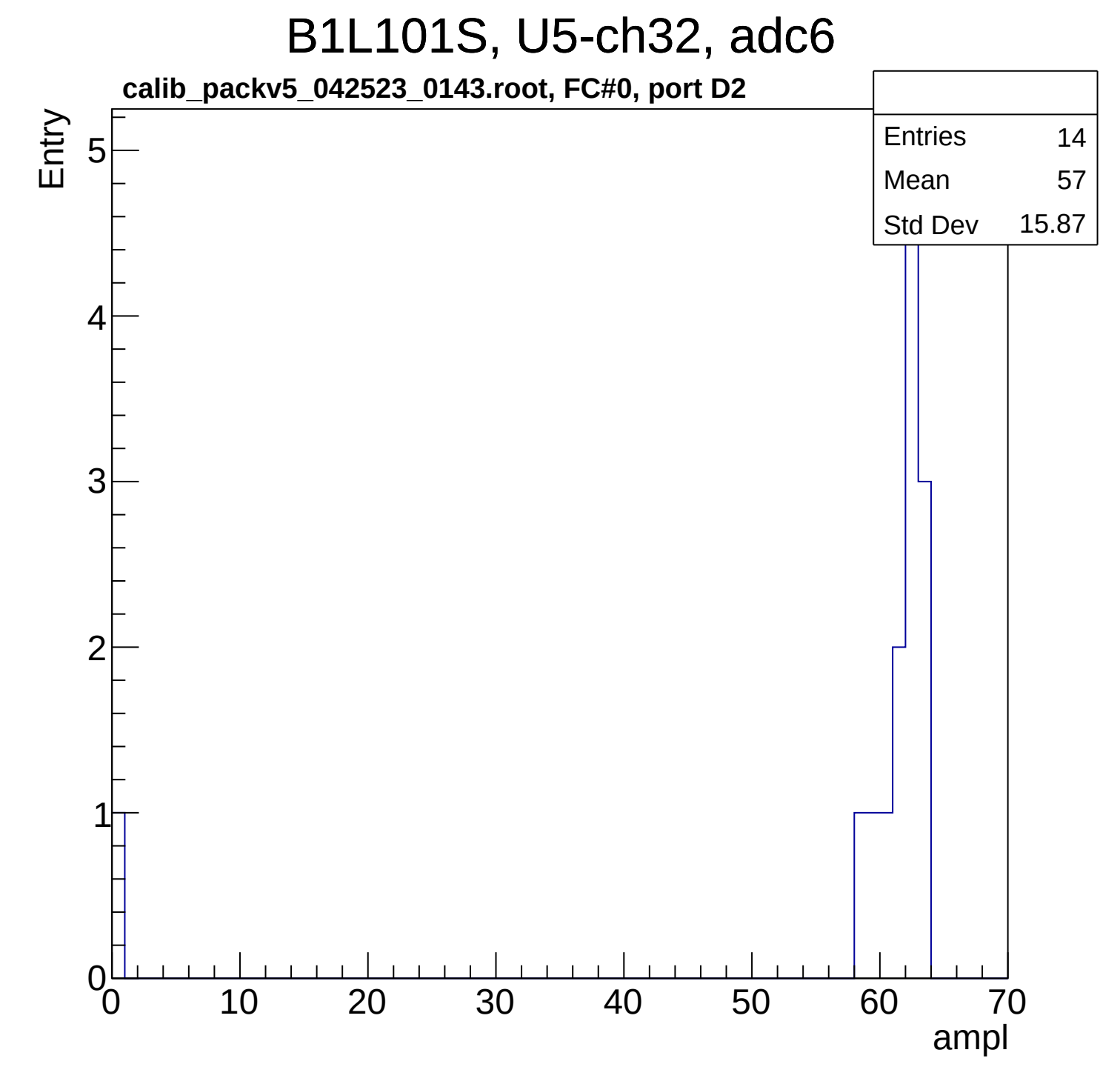
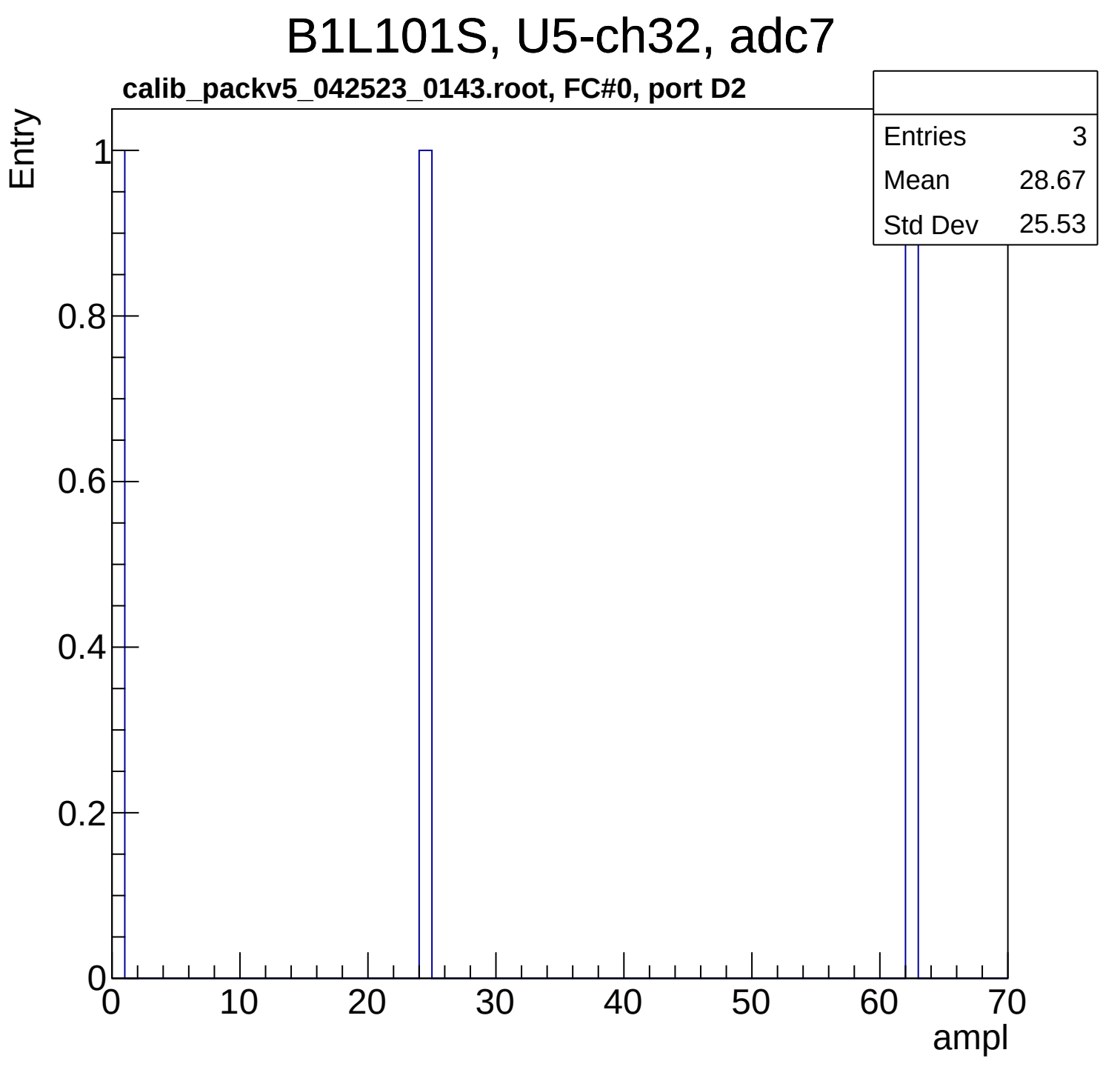
40
50
60
70


B1L101S, U5-ch32, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 14
Mean 57
Std Dev 15.87
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch32, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 28.67
Std Dev 25.53
Entry
ampl
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0.4
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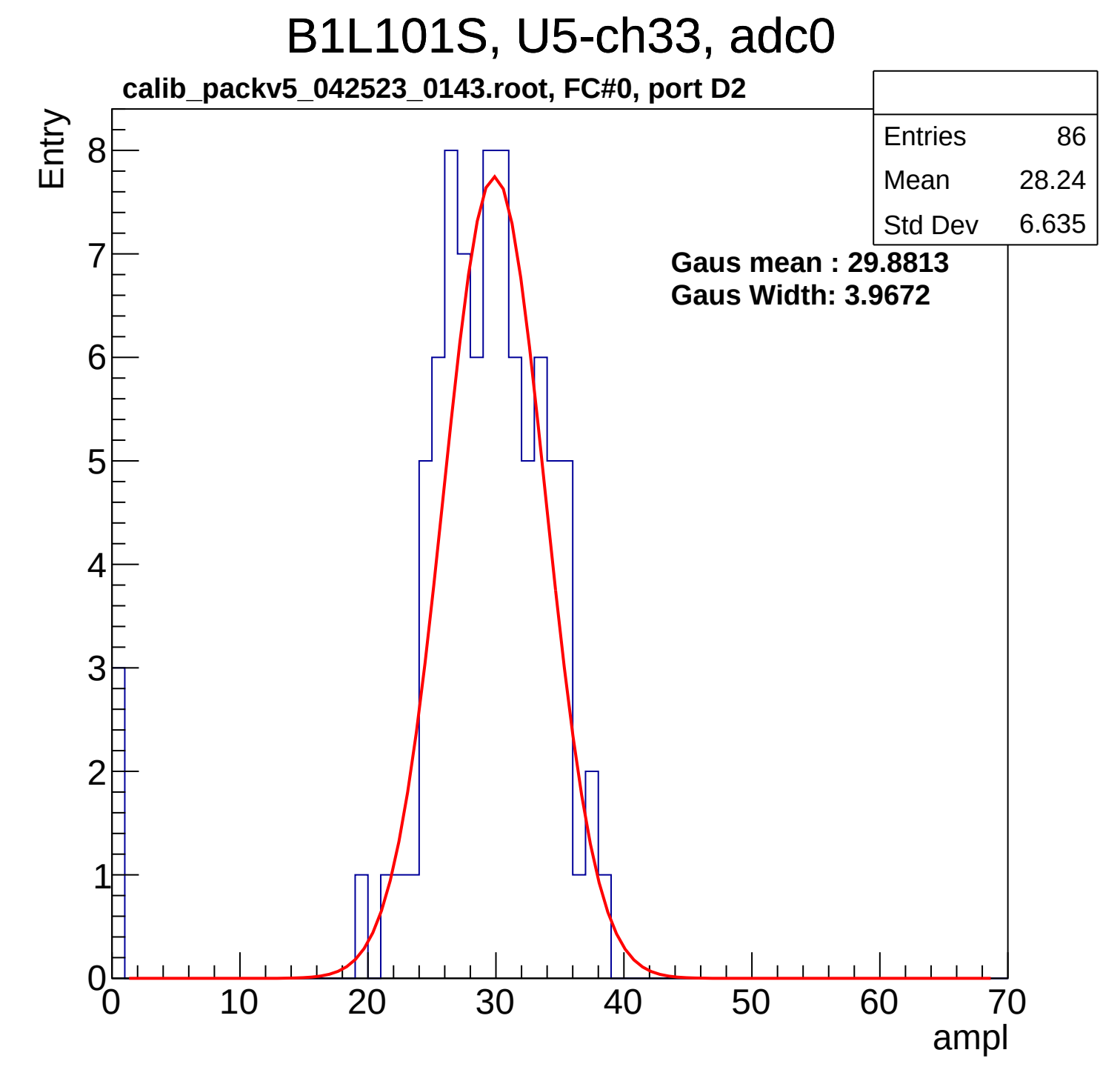
1
0
10
20
30
40
50
60
70


B1L101S, U5-ch33, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 86
Mean 28.24
Std Dev 6.635
Gaus mean : 29.8813
Gaus Width: 3.9672
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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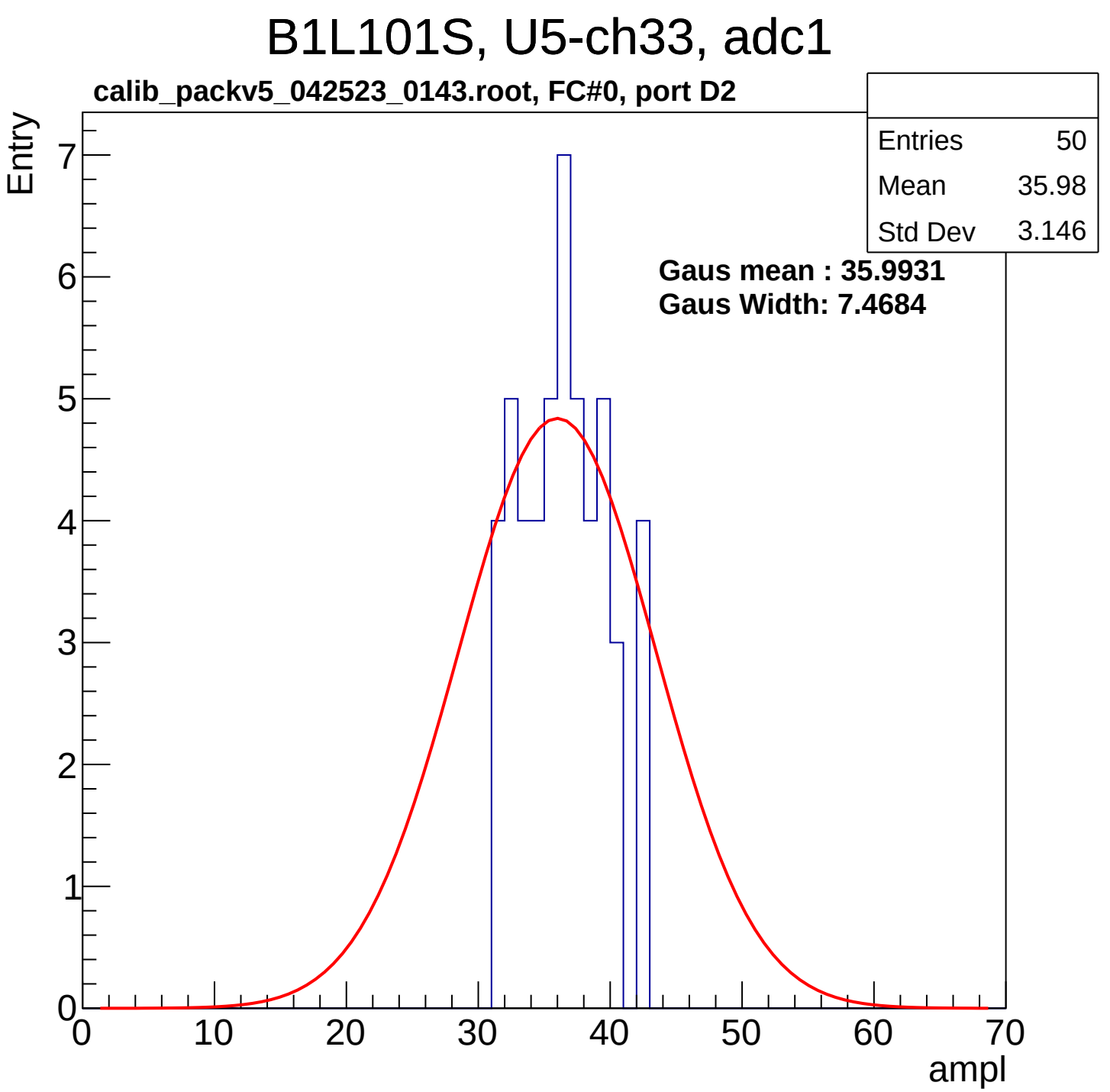
60
70


B1L101S, U5-ch33, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 35.98
Std Dev 3.146
Gaus mean : 35.9931
Gaus Width: 7.4684
Entry
ampl
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1
2
3
4
5
6
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0
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40
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60
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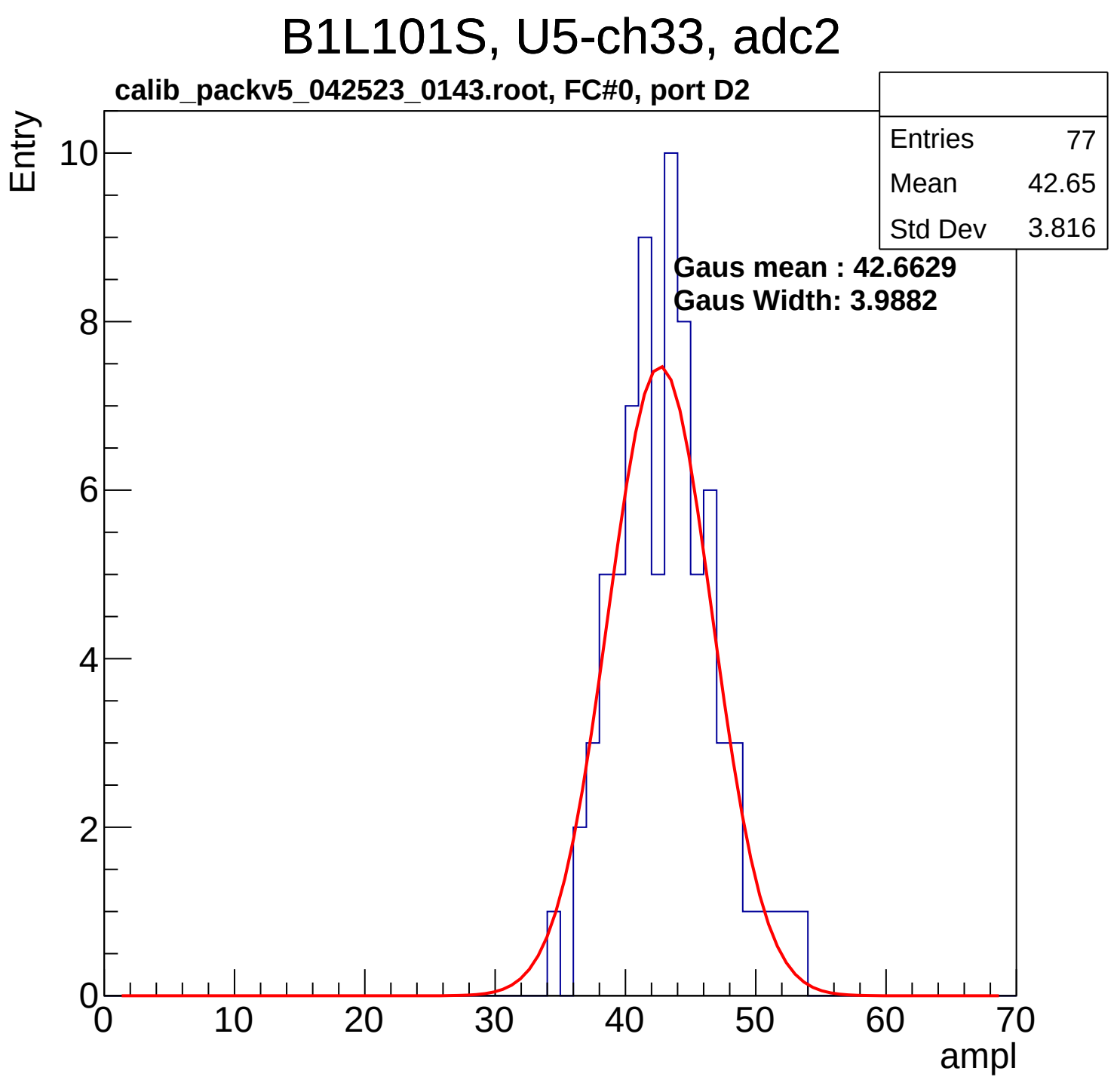
B1L101S, U5-ch33, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 42.65
Std Dev 3.816
Gaus mean : 42.6629
Gaus Width: 3.9882
Entry
ampl
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0
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40
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60
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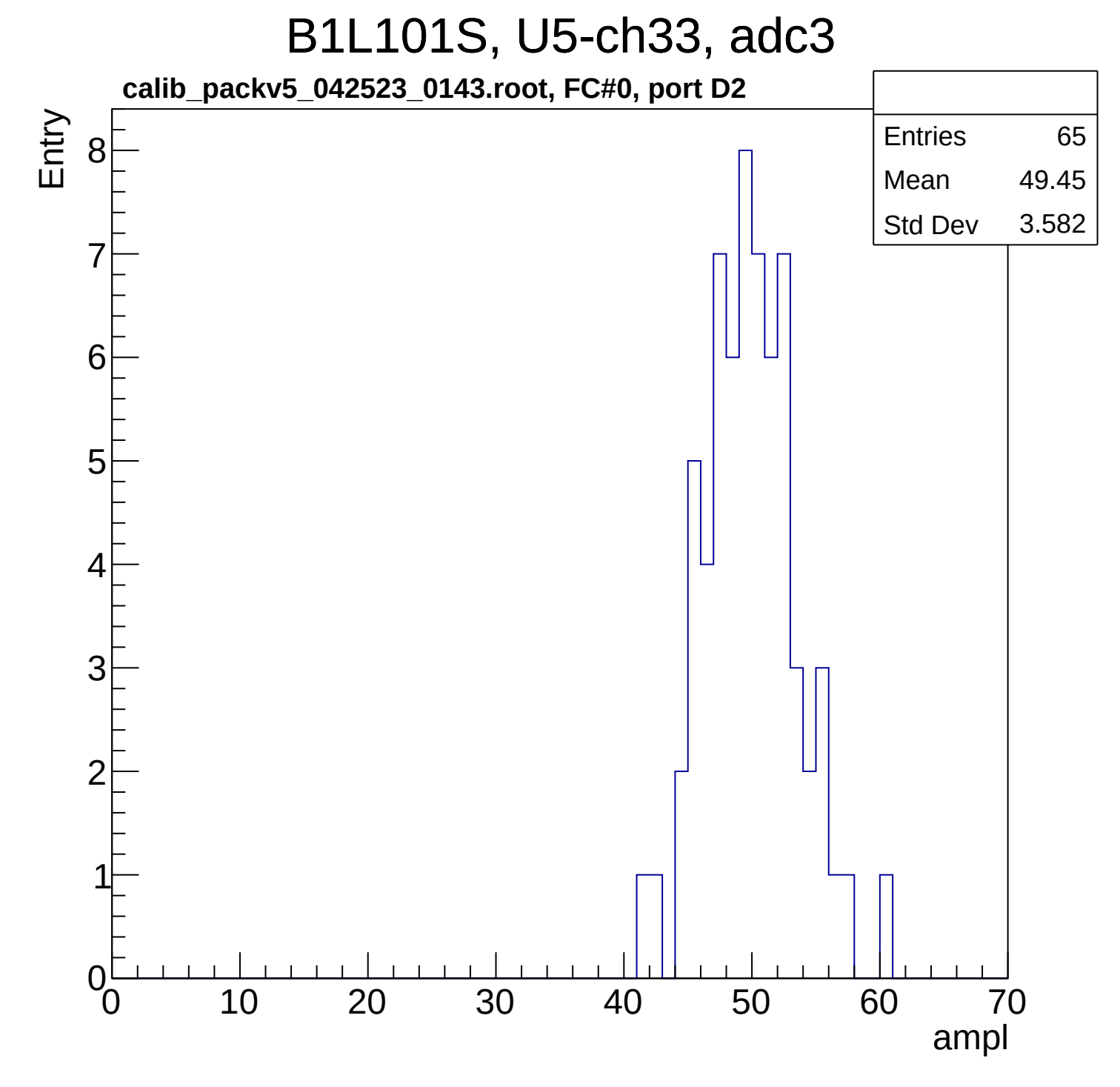
B1L101S, U5-ch33, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 49.45
Std Dev 3.582
Entry
ampl
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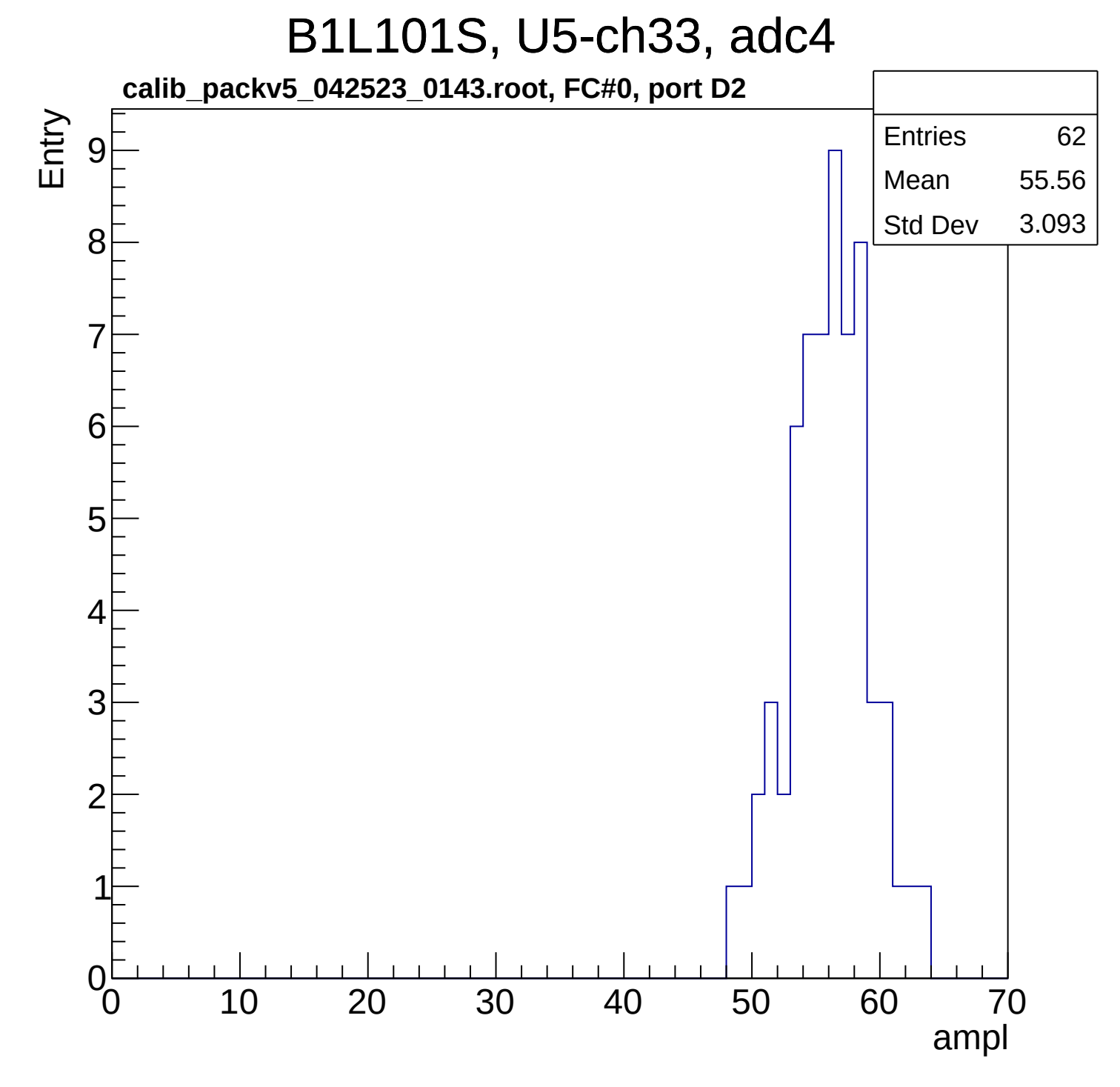
B1L101S, U5-ch33, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 55.56
Std Dev 3.093
Entry
ampl
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3
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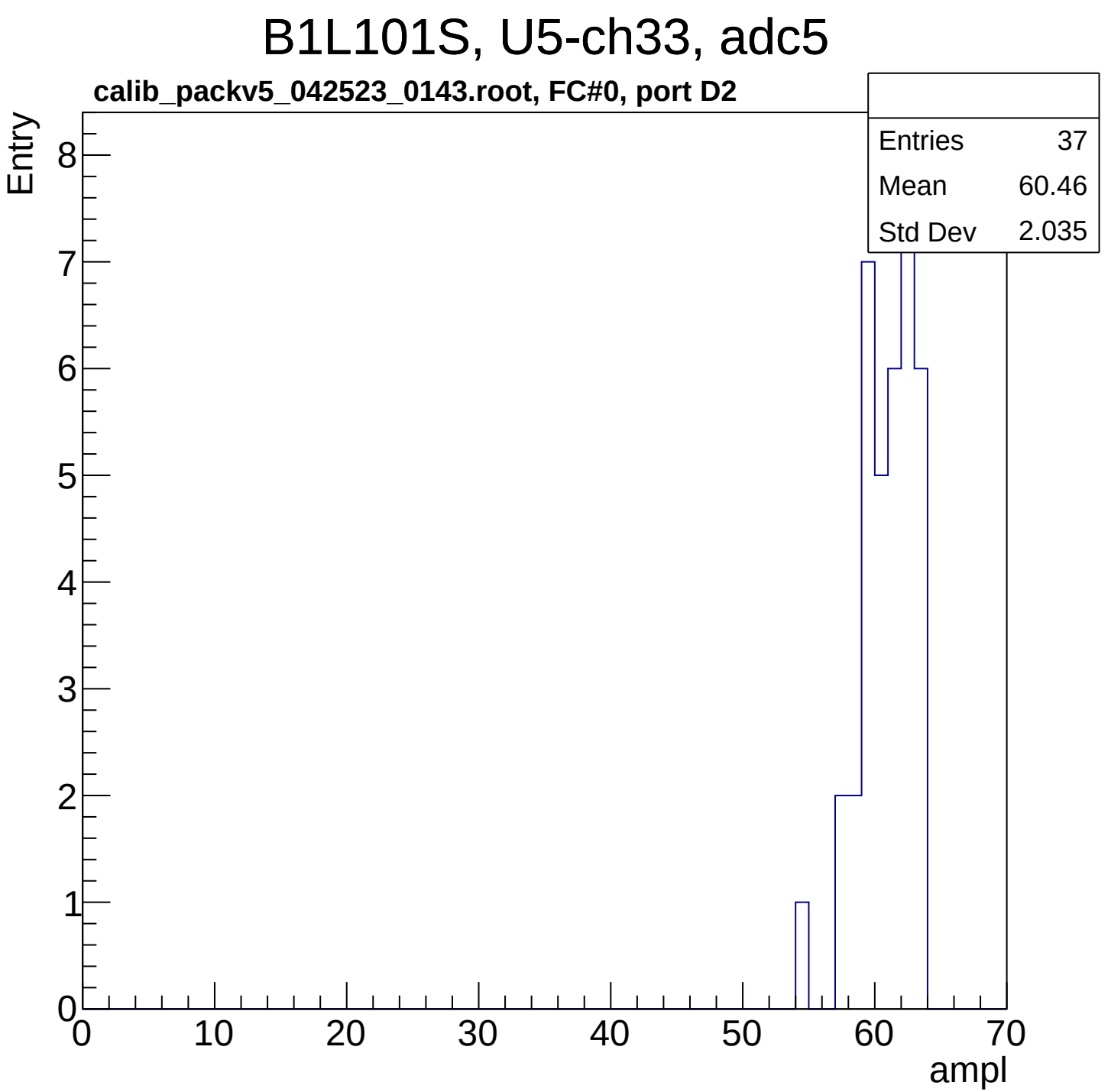
B1L101S, U5-ch33, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 37
Mean 60.46
Std Dev 2.035
Entry
ampl
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3
4
5
6
7
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60
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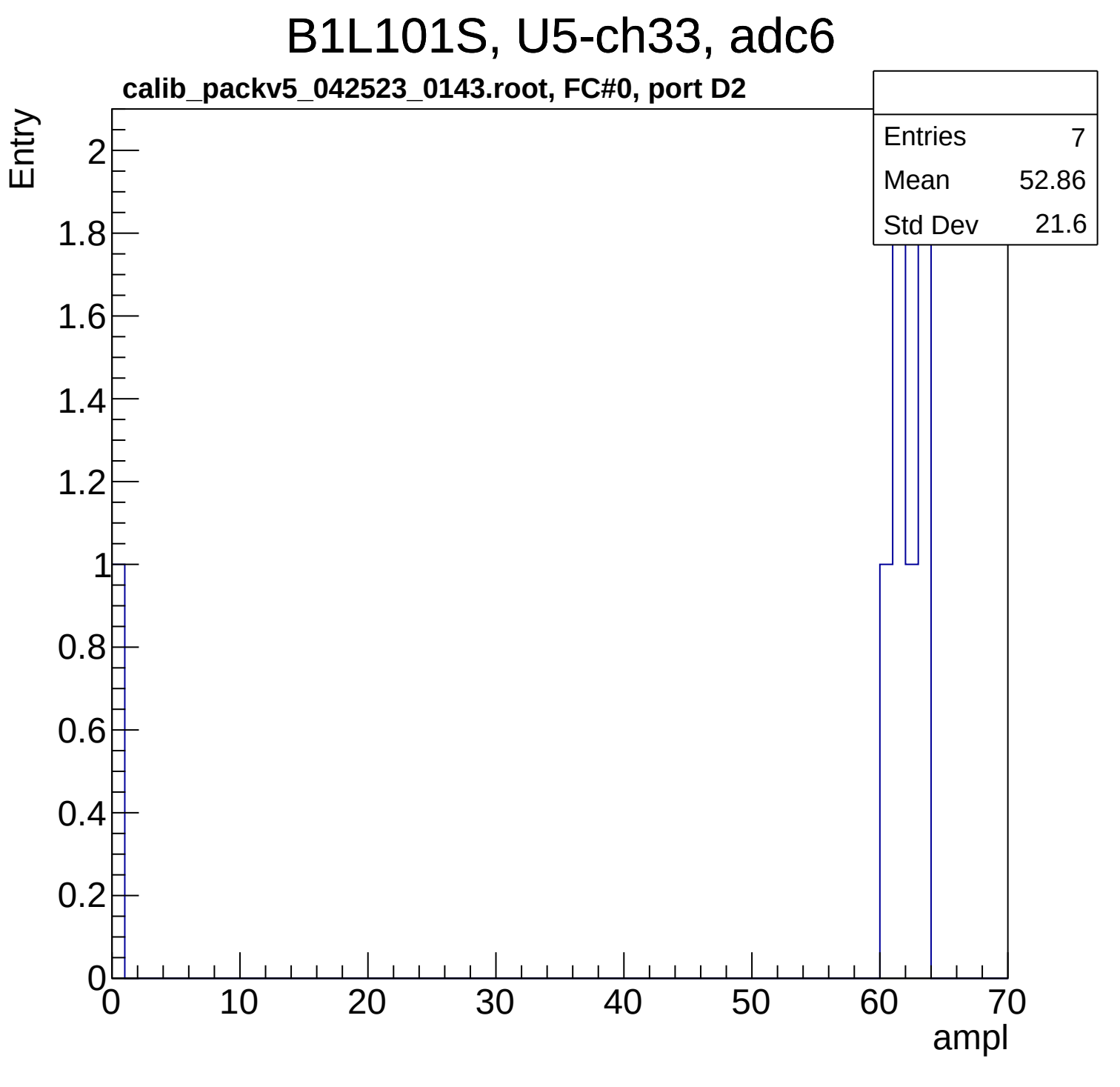
B1L101S, U5-ch33, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 52.86
Std Dev 21.6
Entry
ampl
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0.2
0.4
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1.2
1.4
1.6
1.8
2
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40
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60
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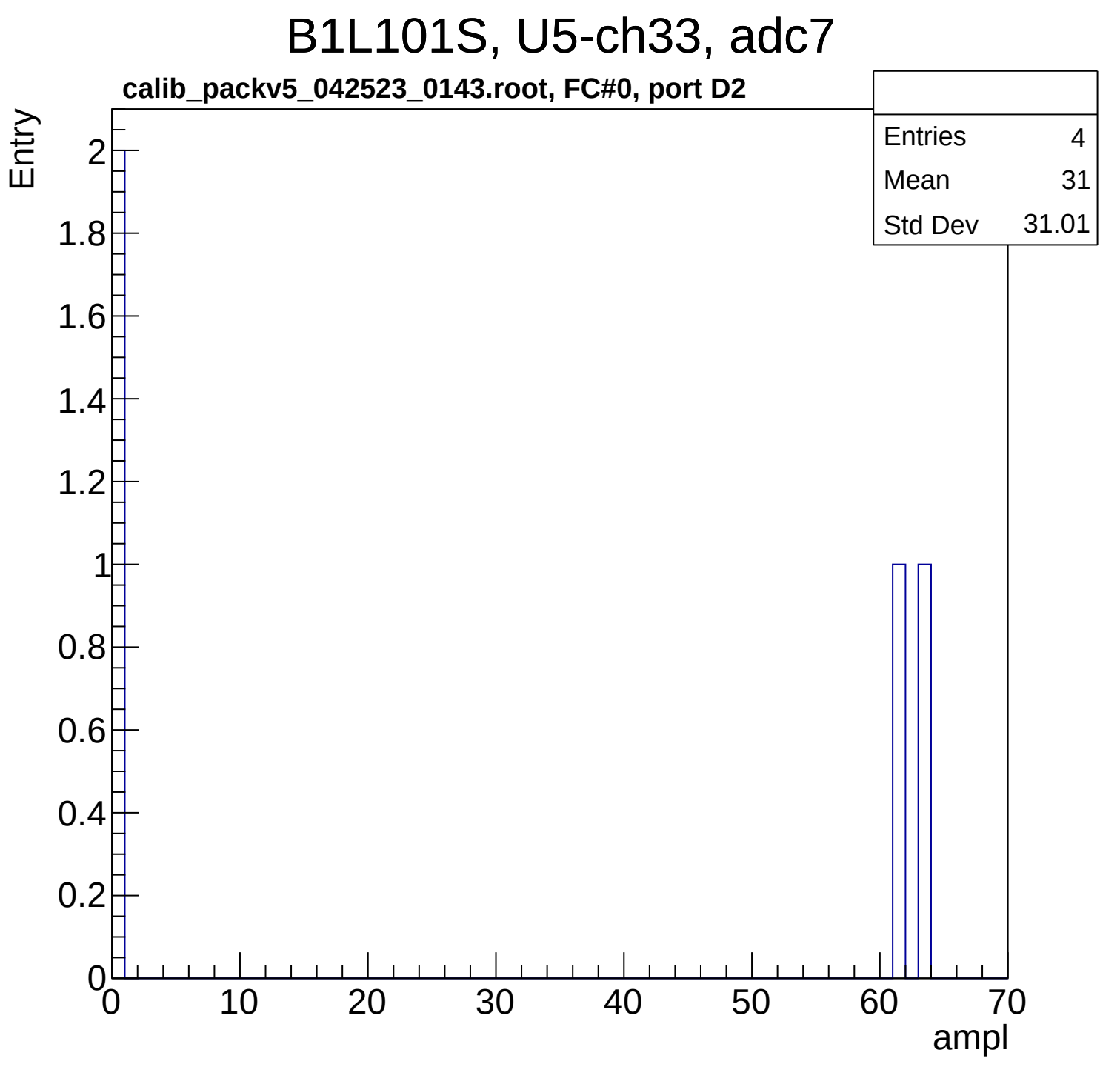
B1L101S, U5-ch33, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 31
Std Dev 31.01
Entry
ampl
0
0.2
0.4
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1.4
1.6
1.8
2
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40
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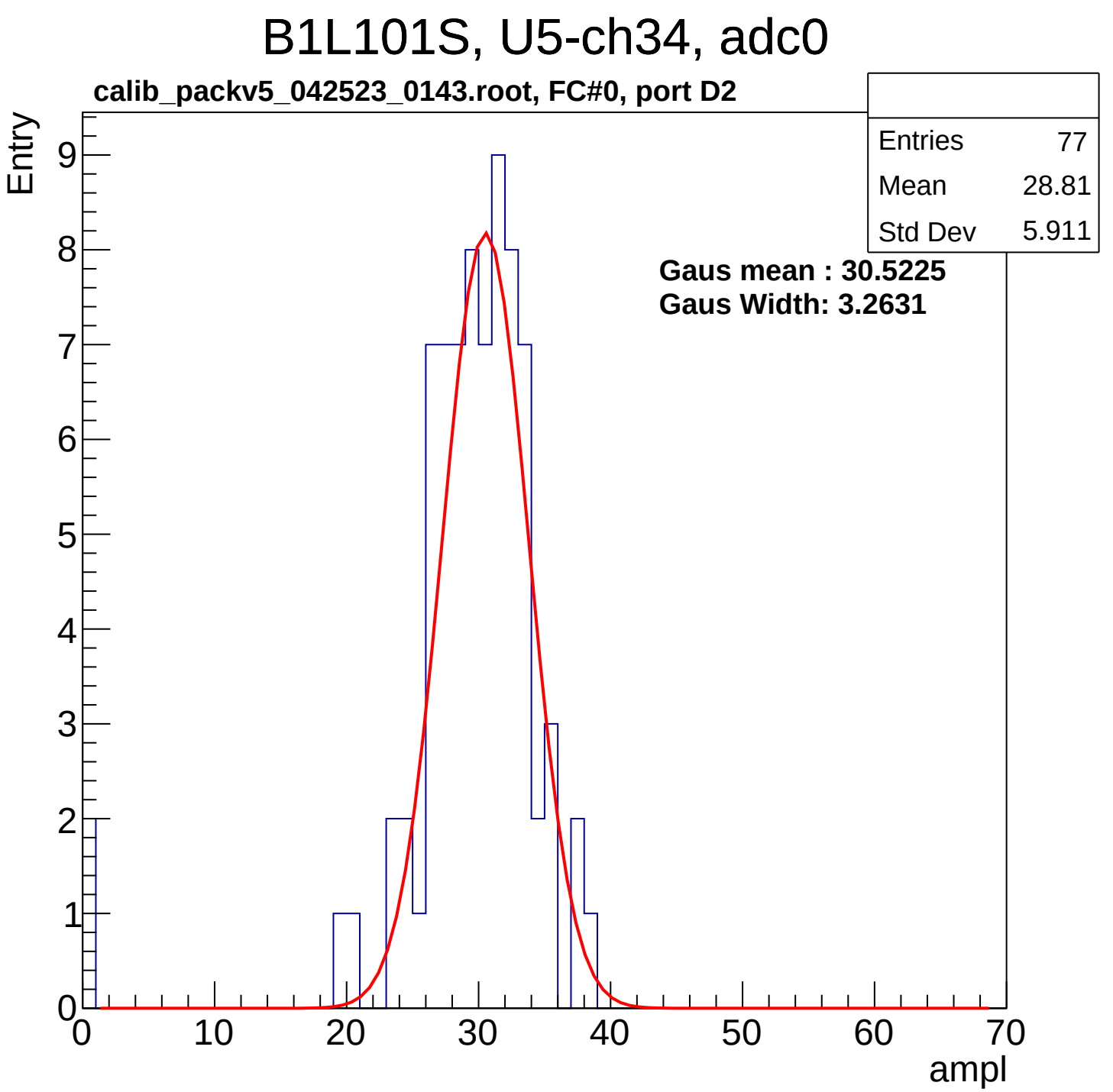
B1L101S, U5-ch34, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 28.81
Std Dev 5.911
Gaus mean : 30.5225
Gaus Width: 3.2631
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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60
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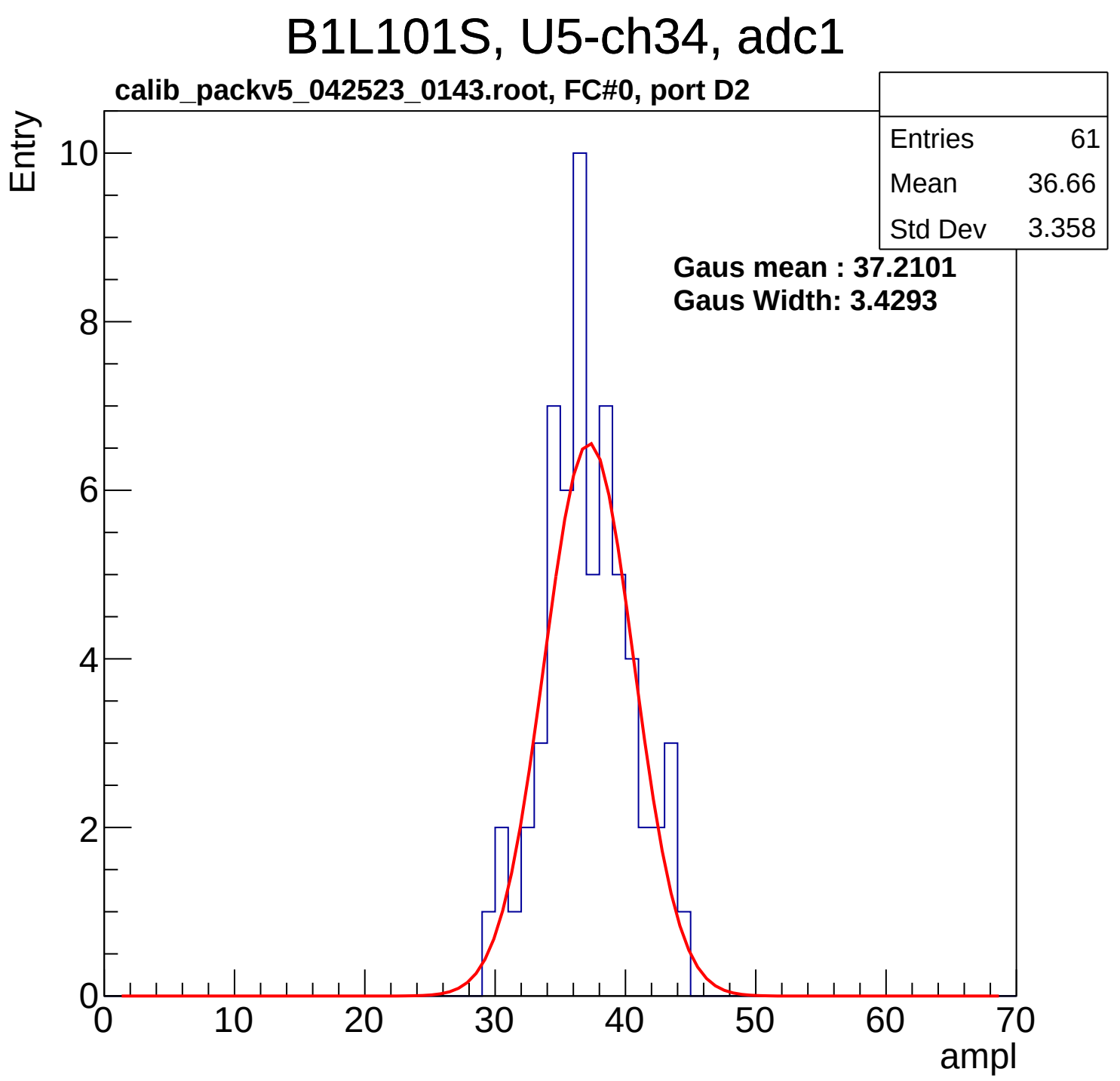
B1L101S, U5-ch34, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 36.66
Std Dev 3.358
Gaus mean : 37.2101
Gaus Width: 3.4293
Entry
ampl
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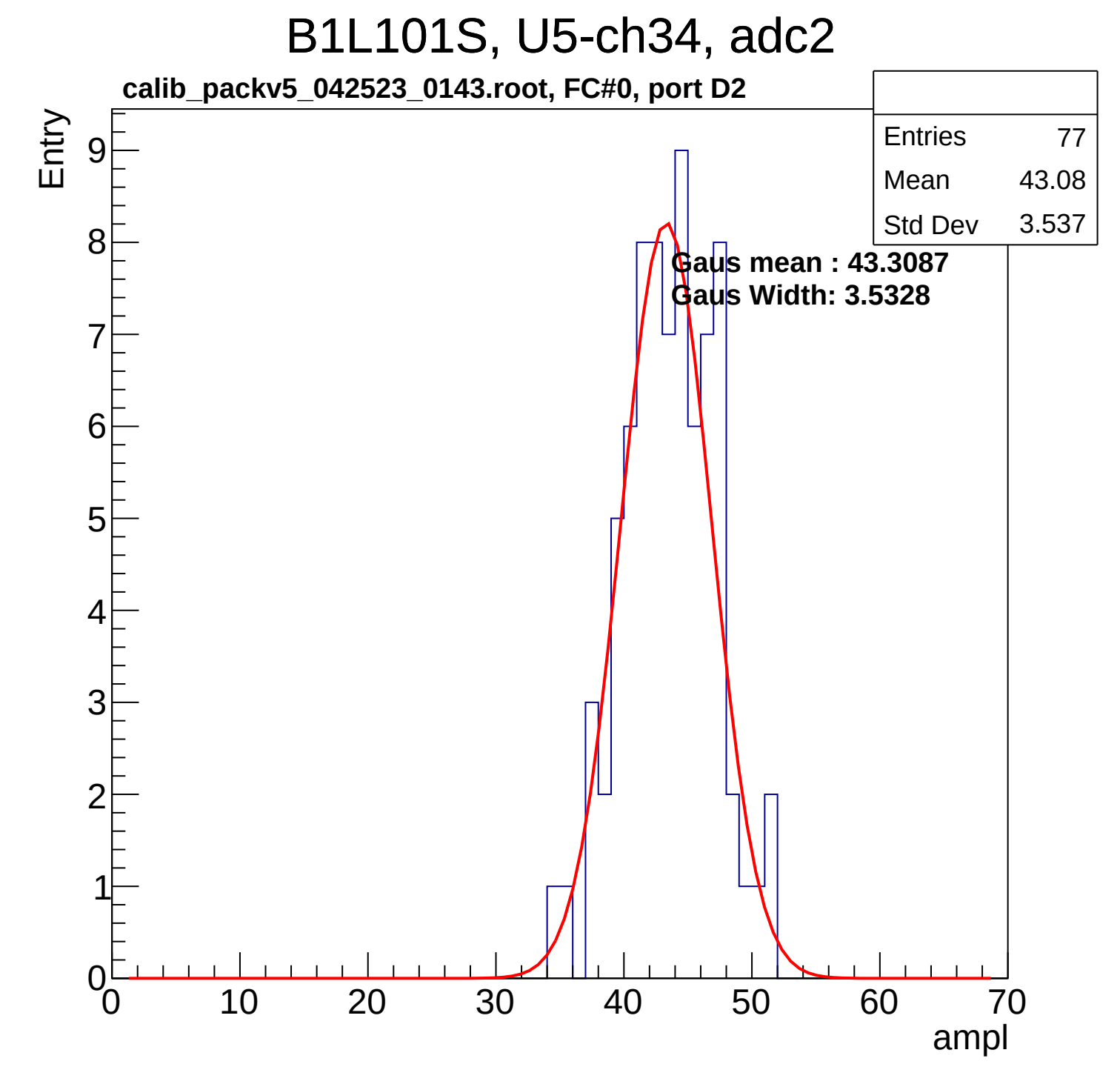
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch34, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 43.08
Std Dev 3.537
Gaus mean : 43.3087
Gaus Width: 3.5328
Entry
ampl
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6
7
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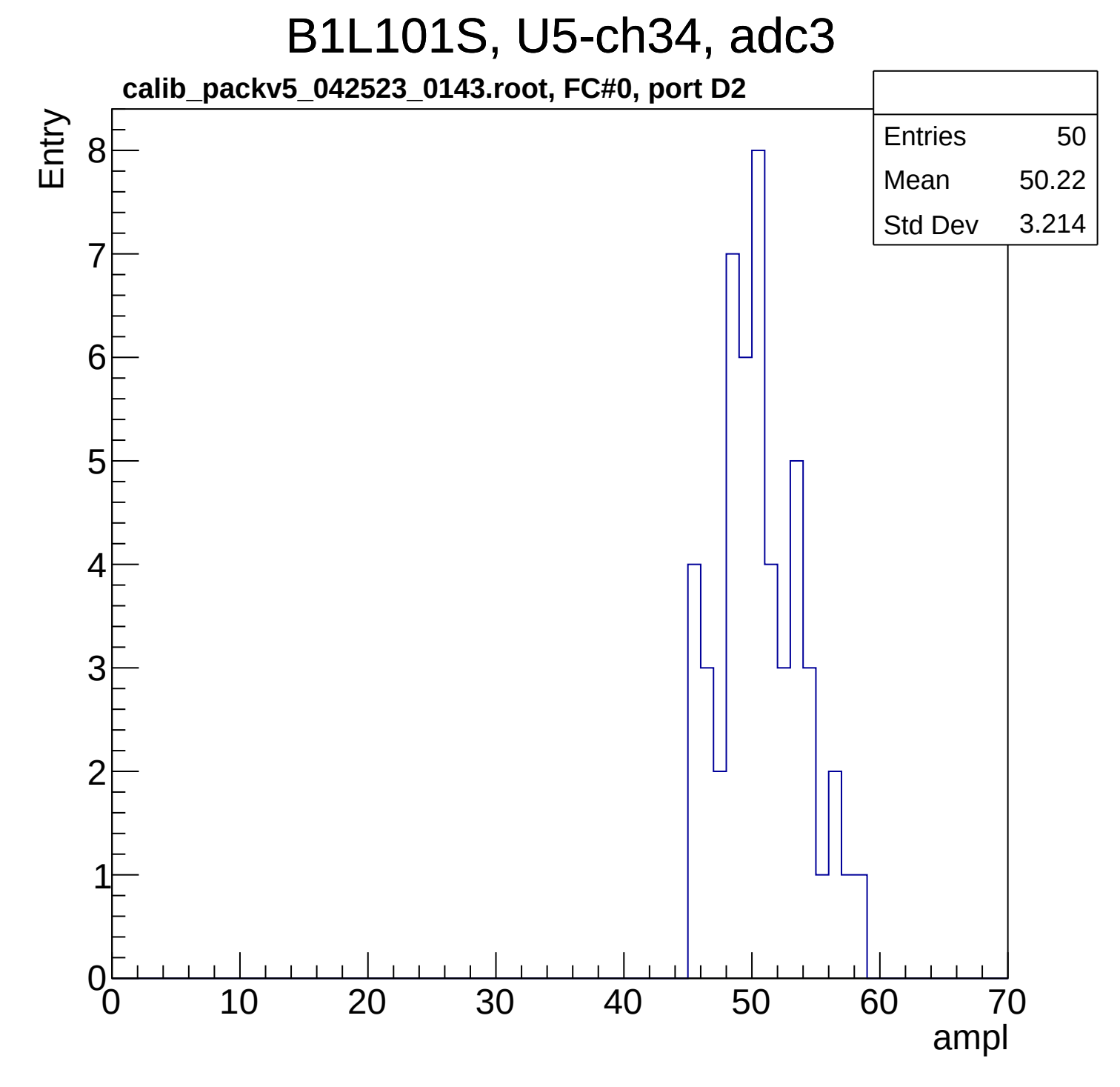
B1L101S, U5-ch34, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 50.22
Std Dev 3.214
Entry
ampl
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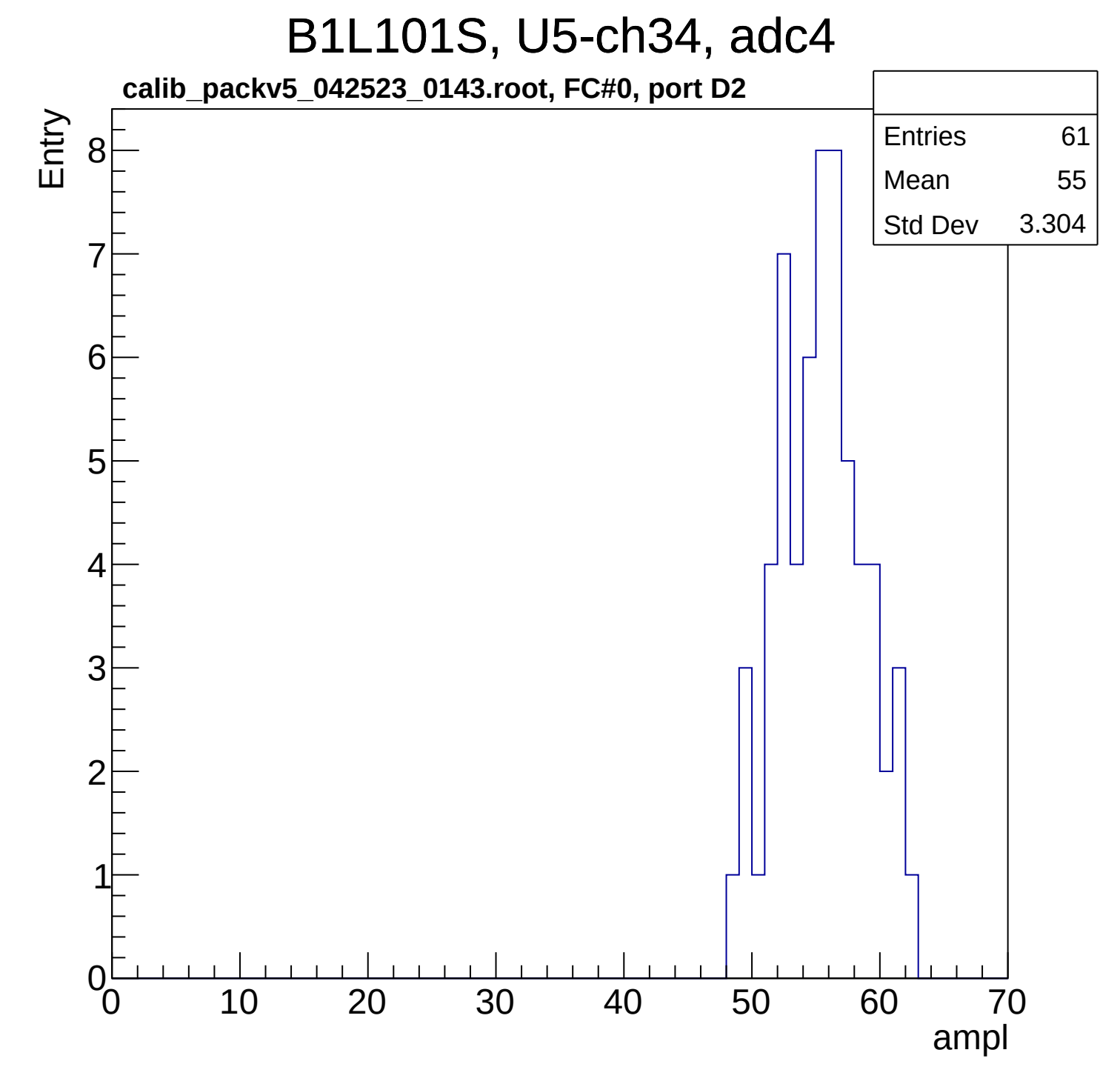
B1L101S, U5-ch34, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 55
Std Dev 3.304
Entry
ampl
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40
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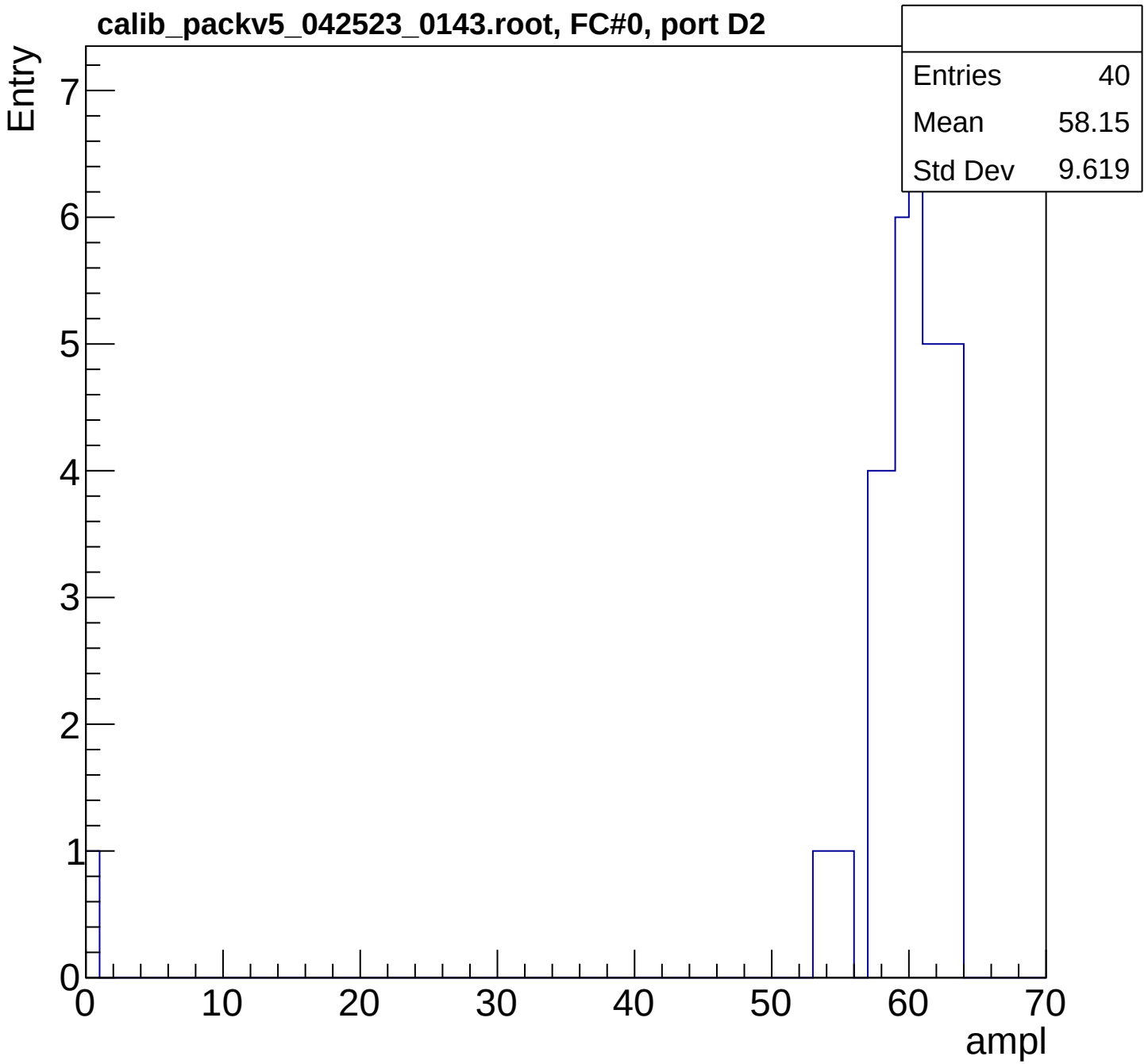
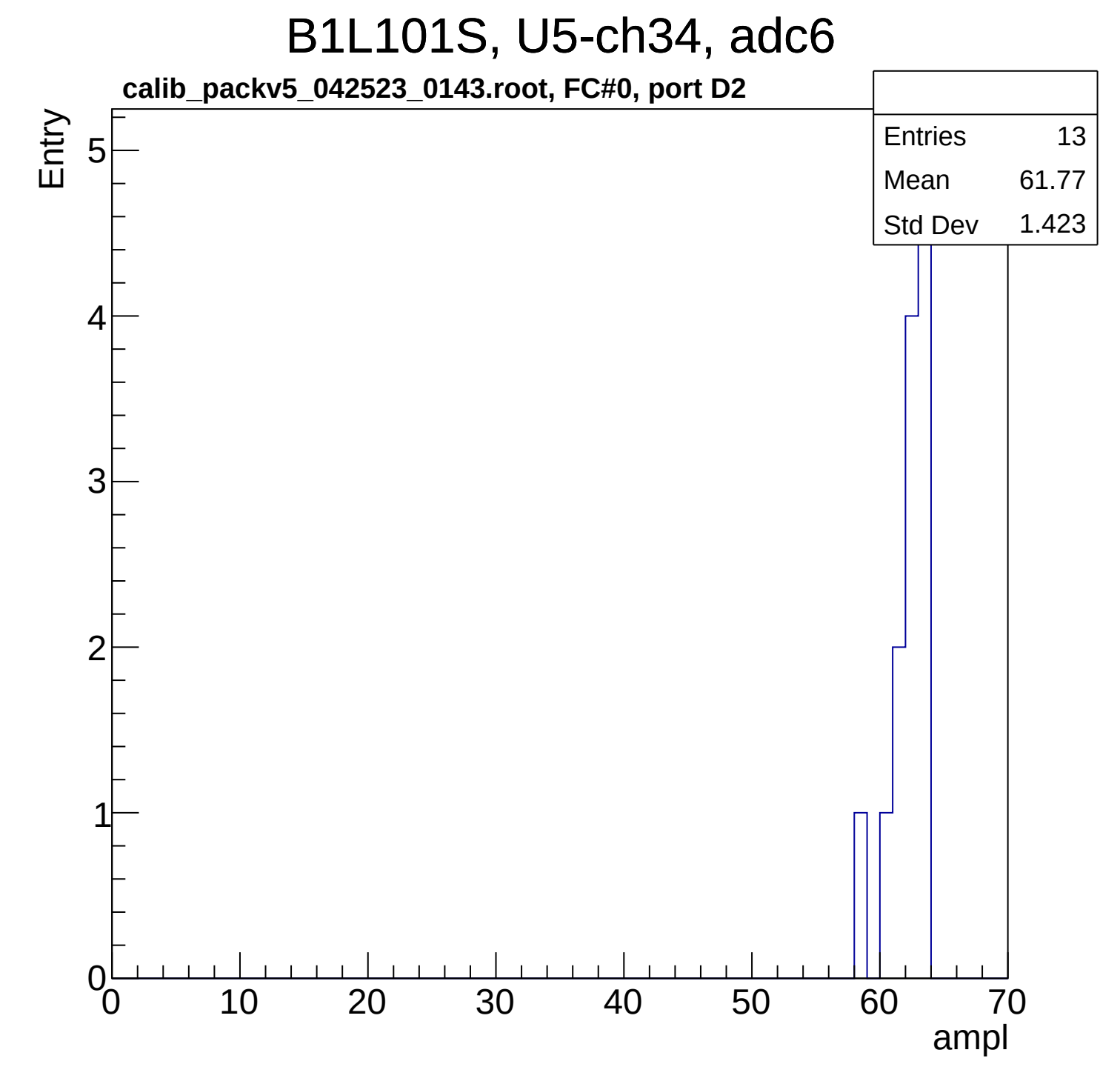
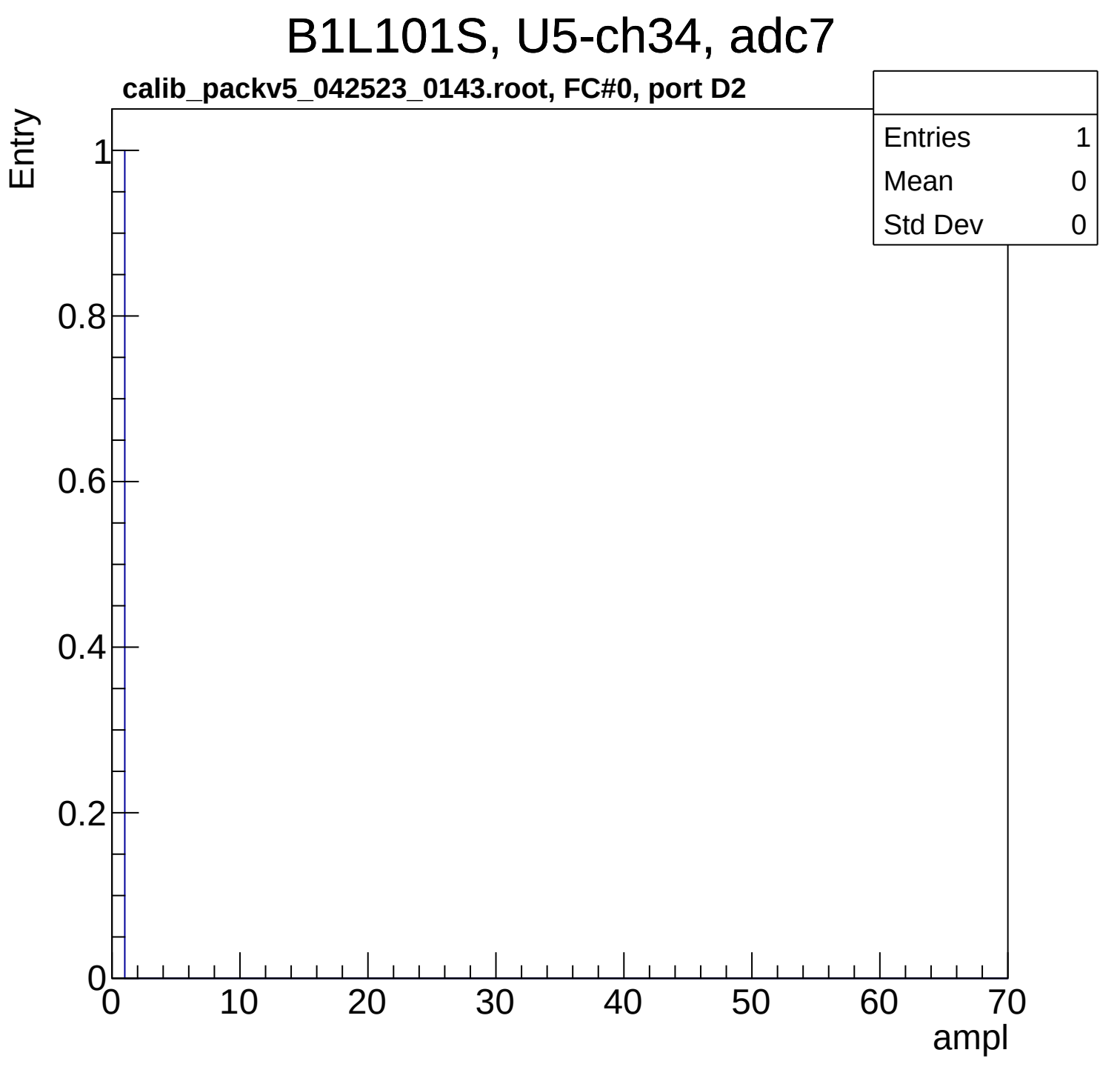

B1L101S, U5-ch34, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 40
Mean 58.15
Std Dev 9.619
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch34, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 13
Mean 61.77
Std Dev 1.423
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch34, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
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0.6
0.4
0.2
0
0
10
20
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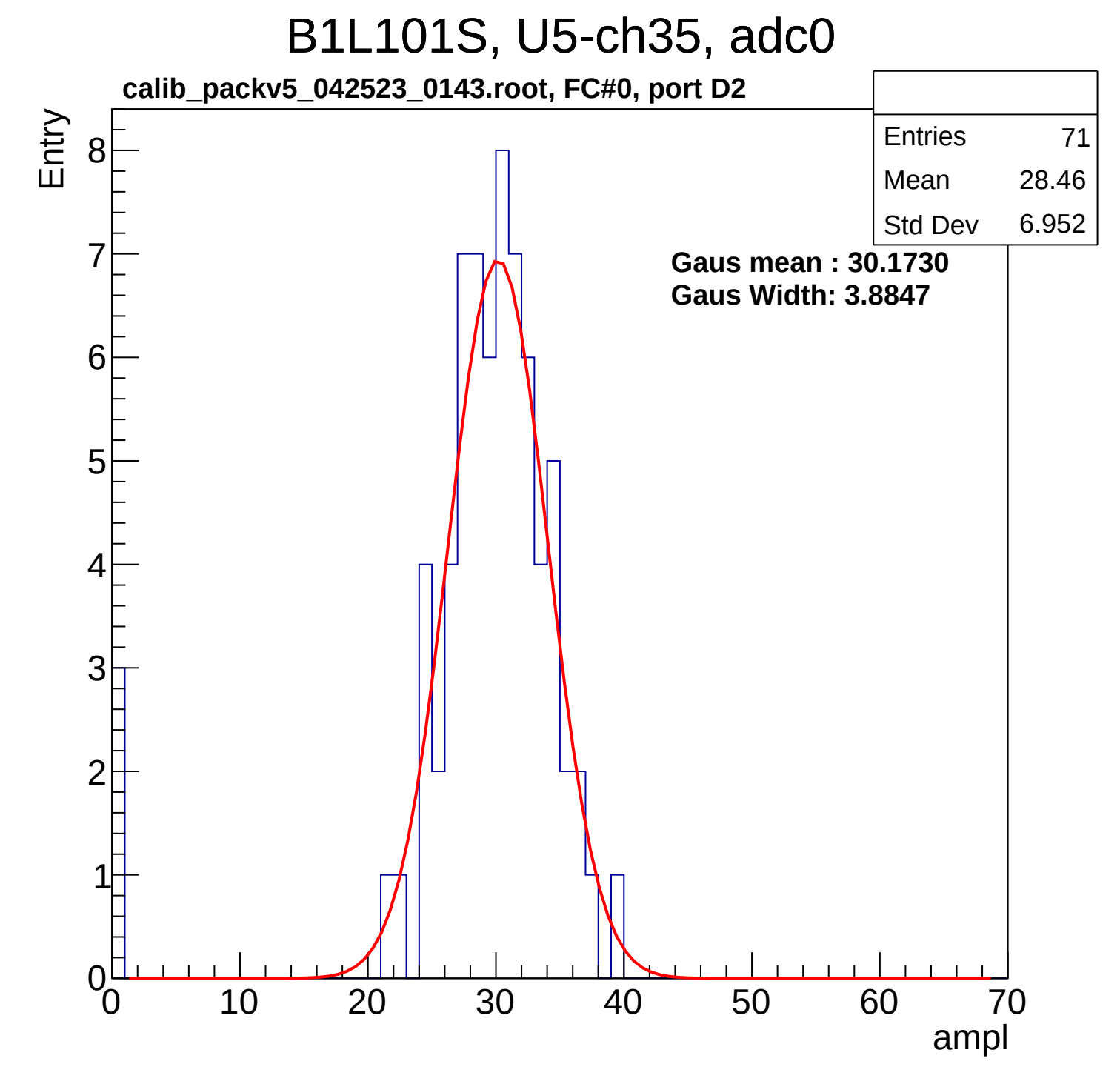
40
50
60
70
ampl


B1L101S, U5-ch35, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 28.46
Std Dev 6.952
Gaus mean : 30.1730
Gaus Width: 3.8847
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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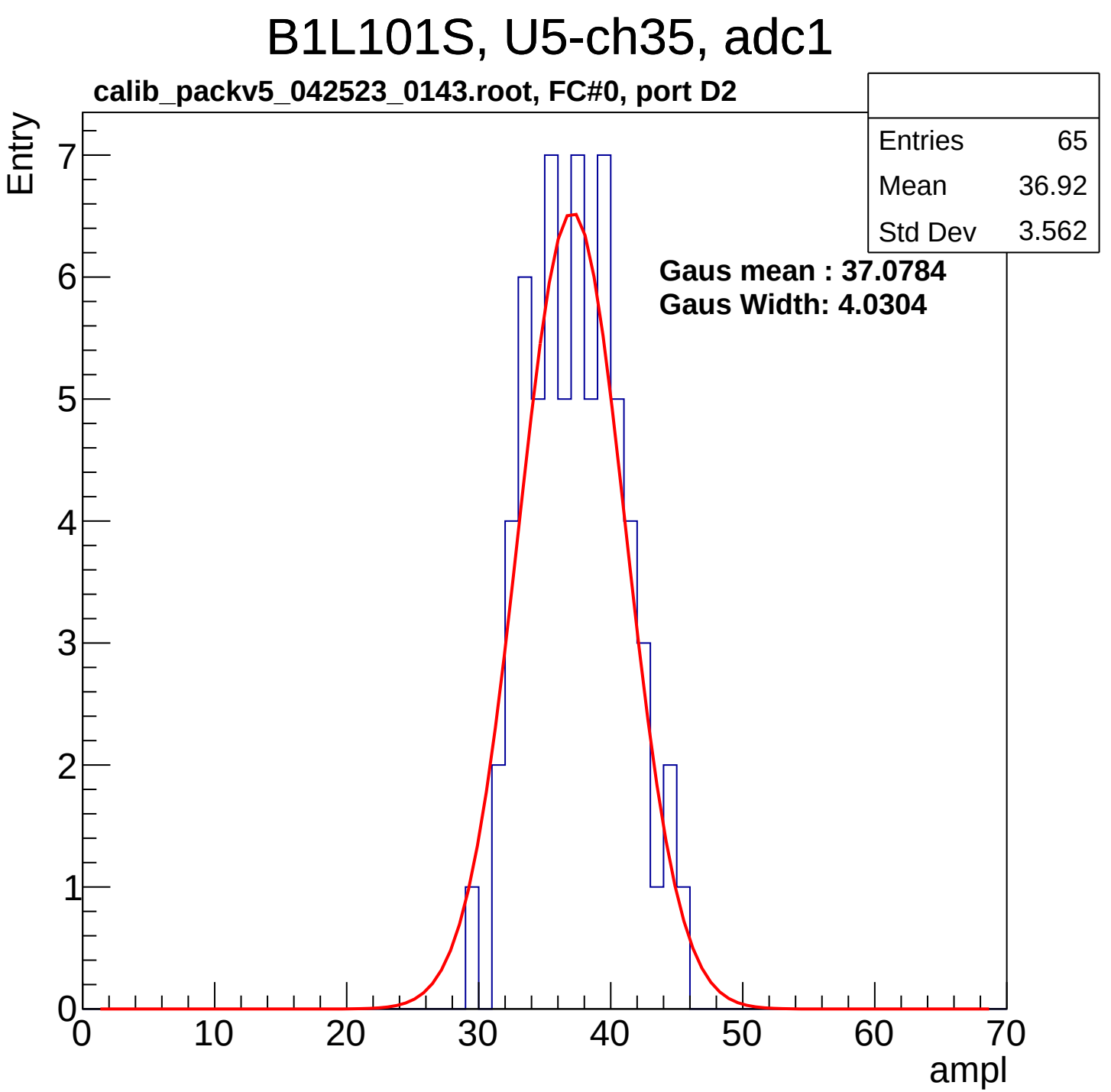
B1L101S, U5-ch35, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 36.92
Std Dev 3.562
Gaus mean : 37.0784
Gaus Width: 4.0304
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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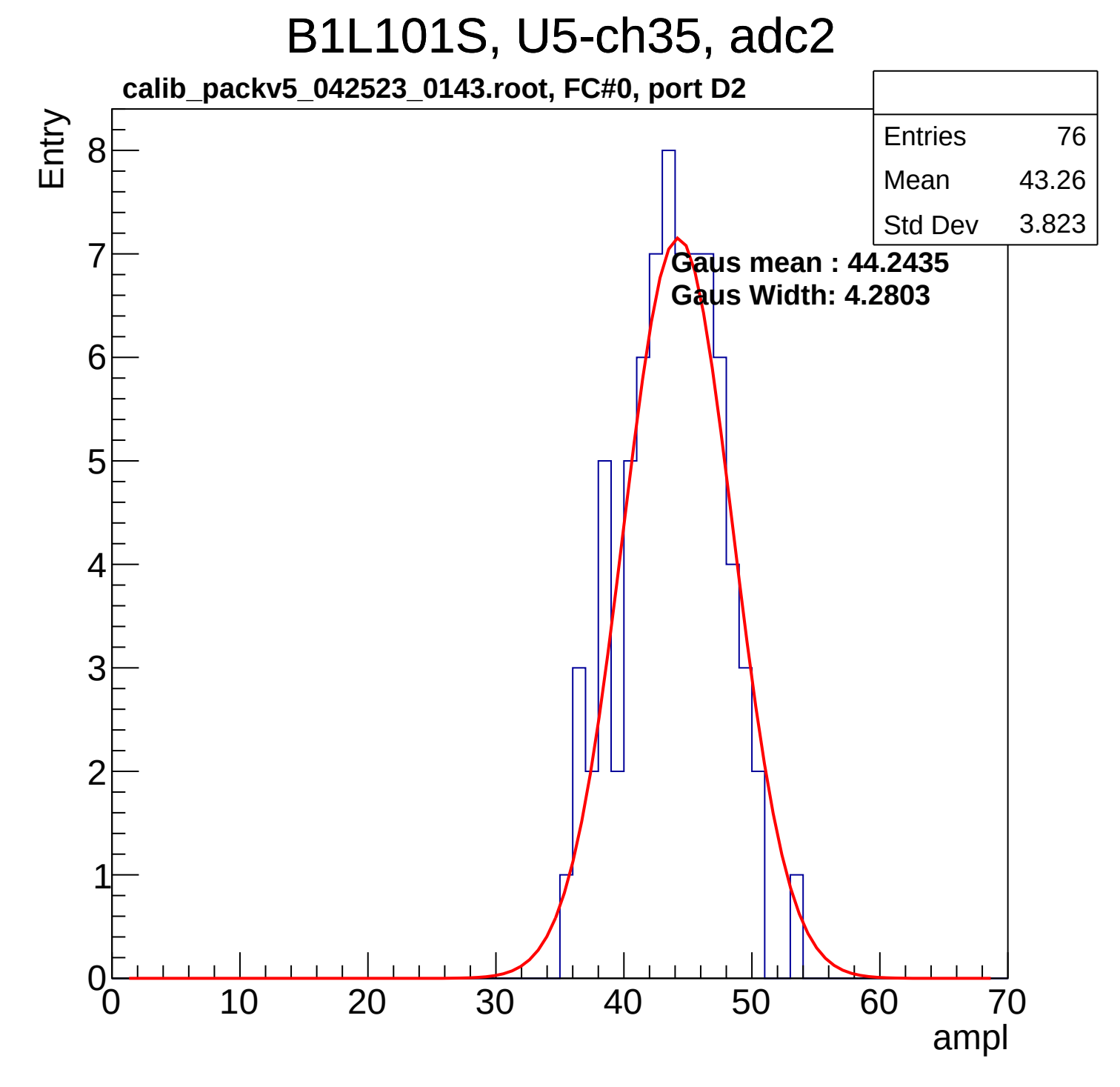
B1L101S, U5-ch35, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 43.26
Std Dev 3.823
Gaus mean : 44.2435
Gaus Width: 4.2803
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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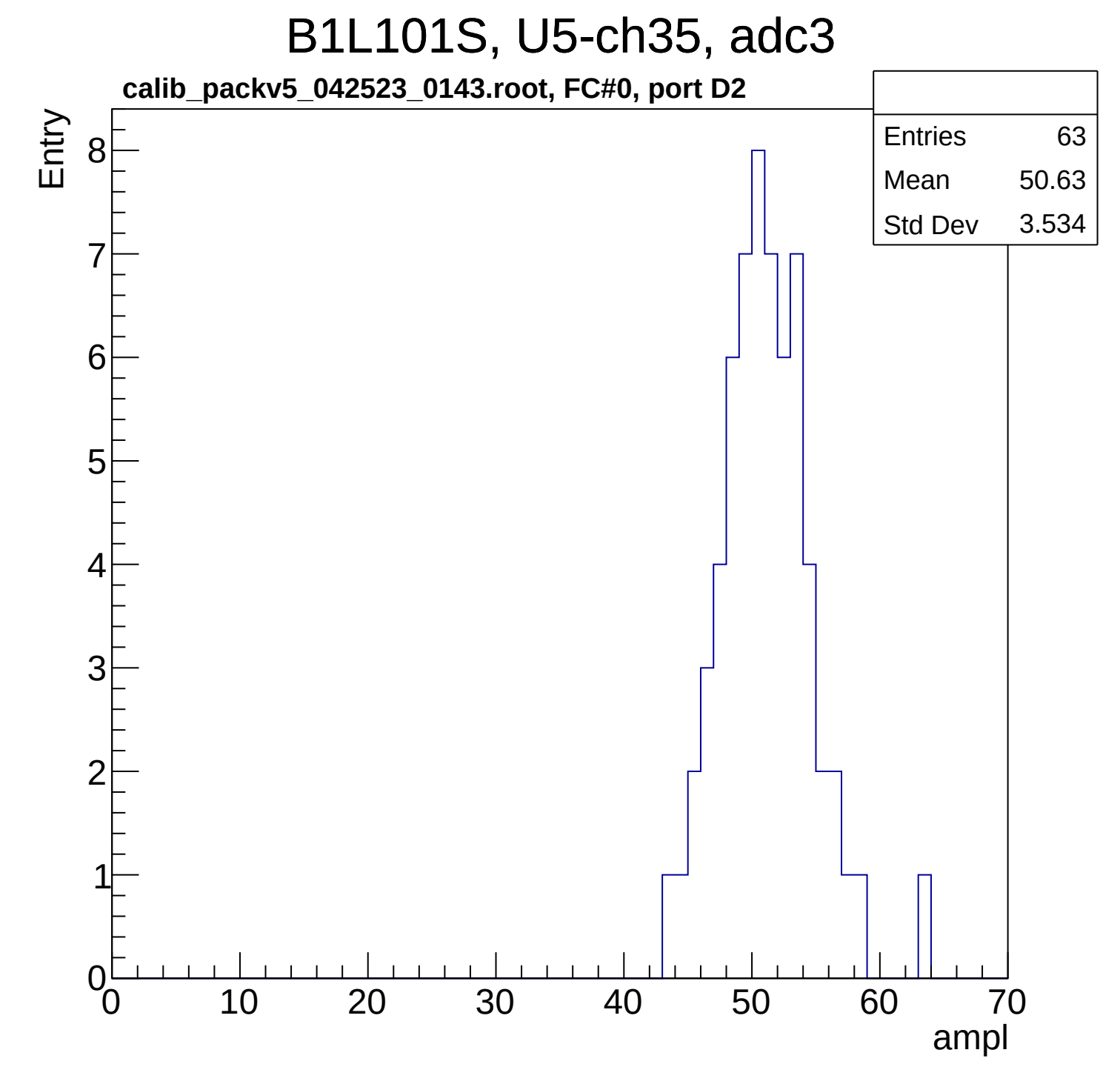
B1L101S, U5-ch35, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 50.63
Std Dev 3.534
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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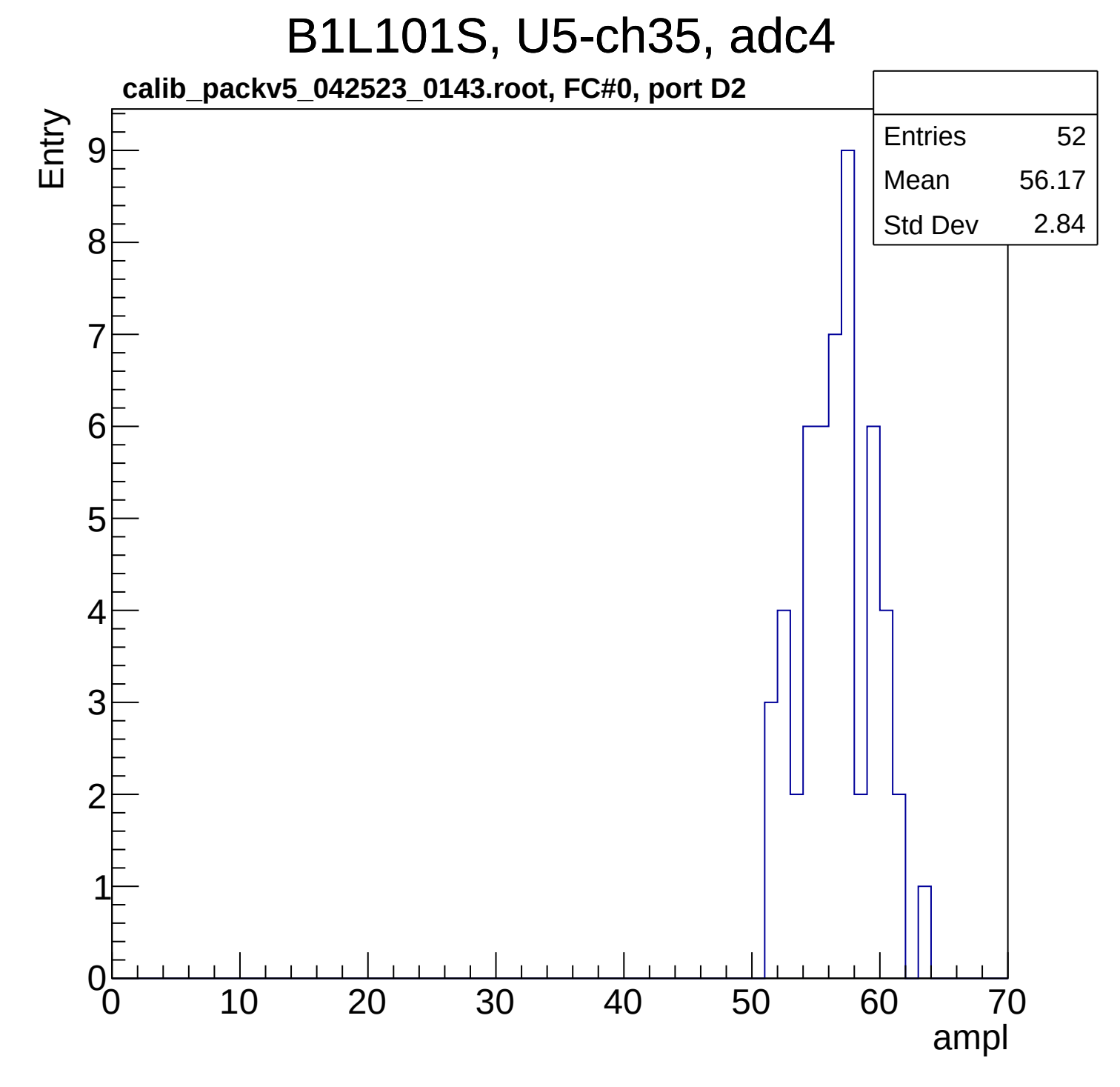
B1L101S, U5-ch35, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 56.17
Std Dev 2.84
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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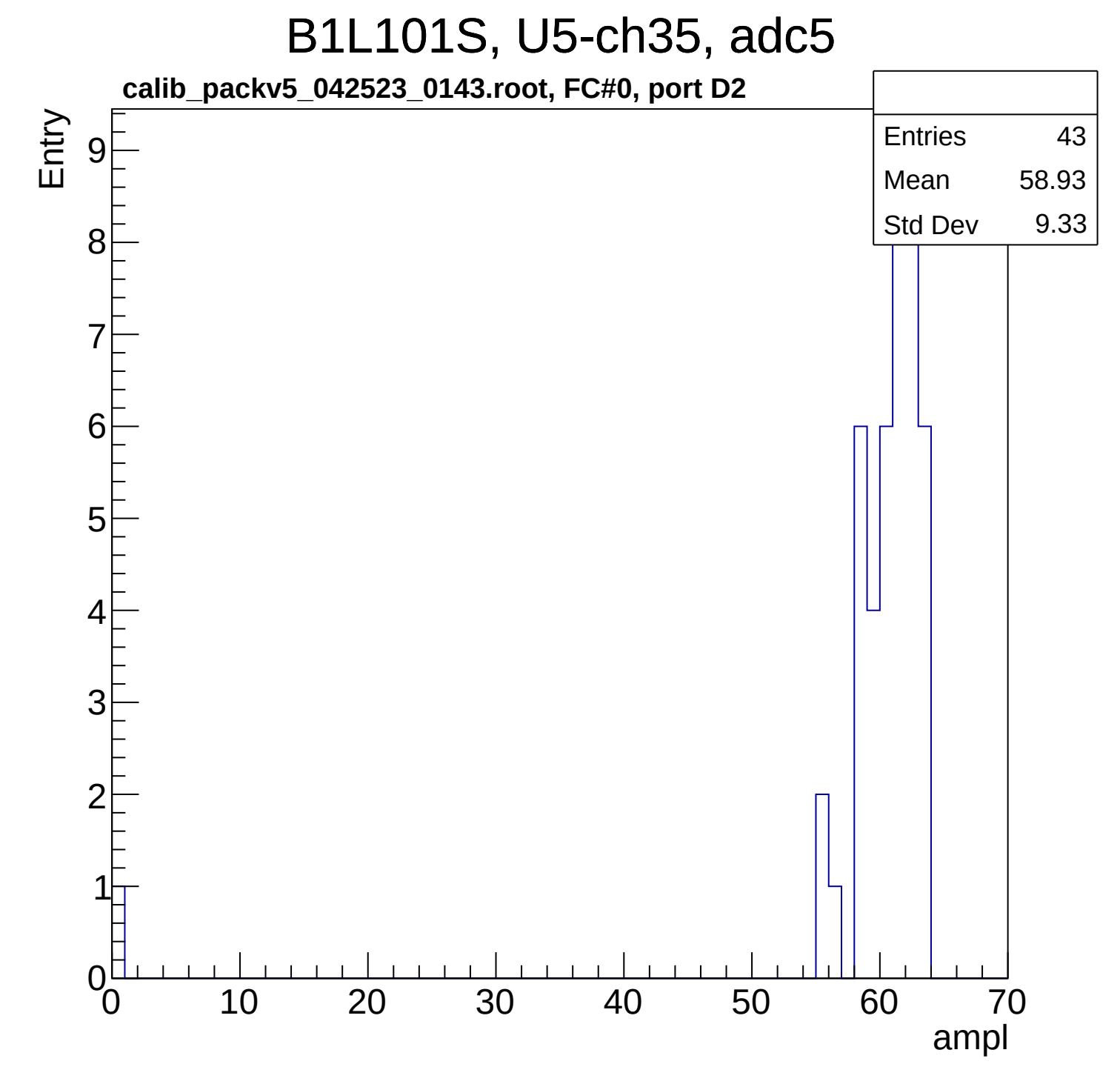
B1L101S, U5-ch35, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 43
Mean 58.93
Std Dev 9.33
Entry
ampl
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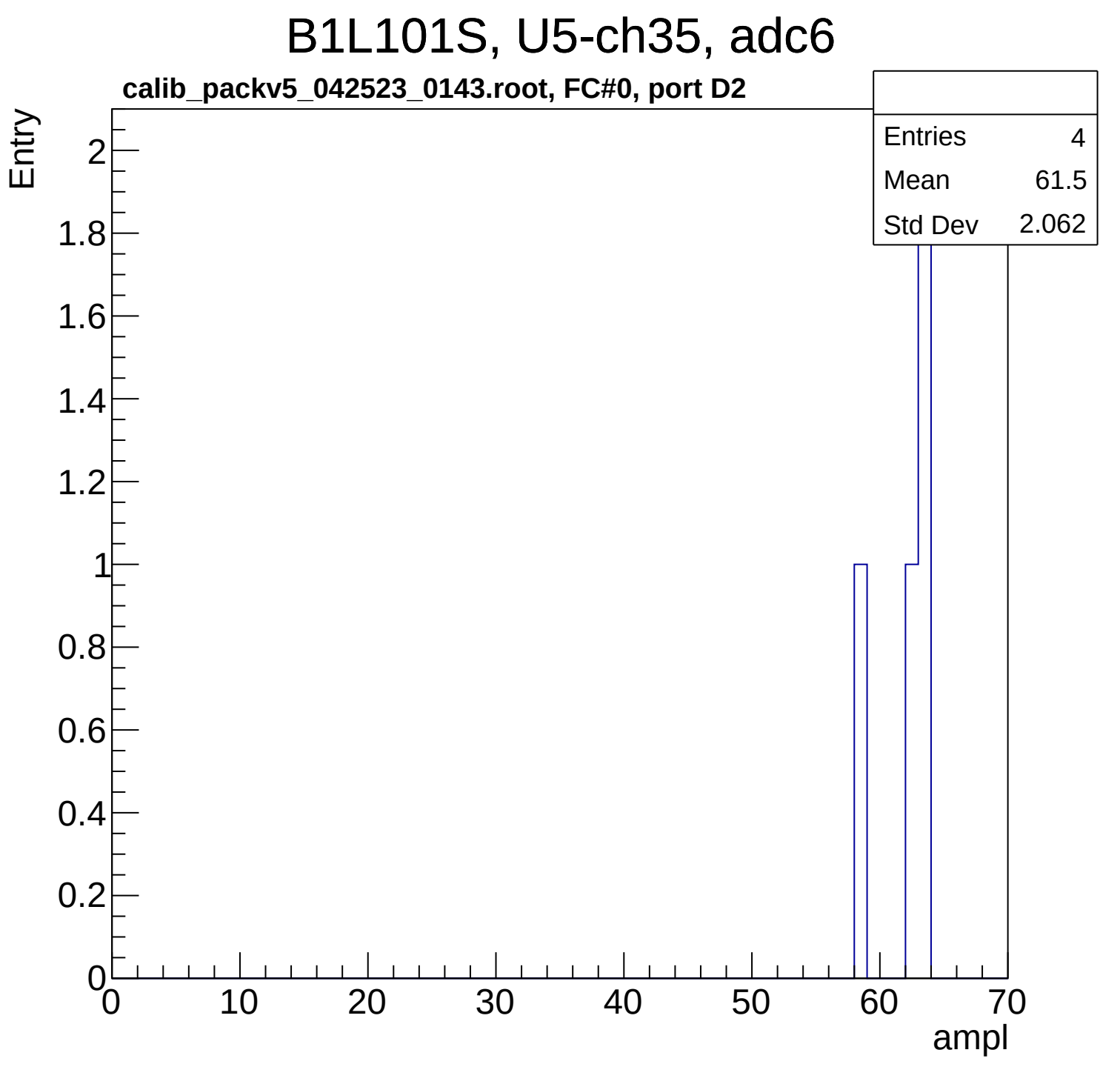
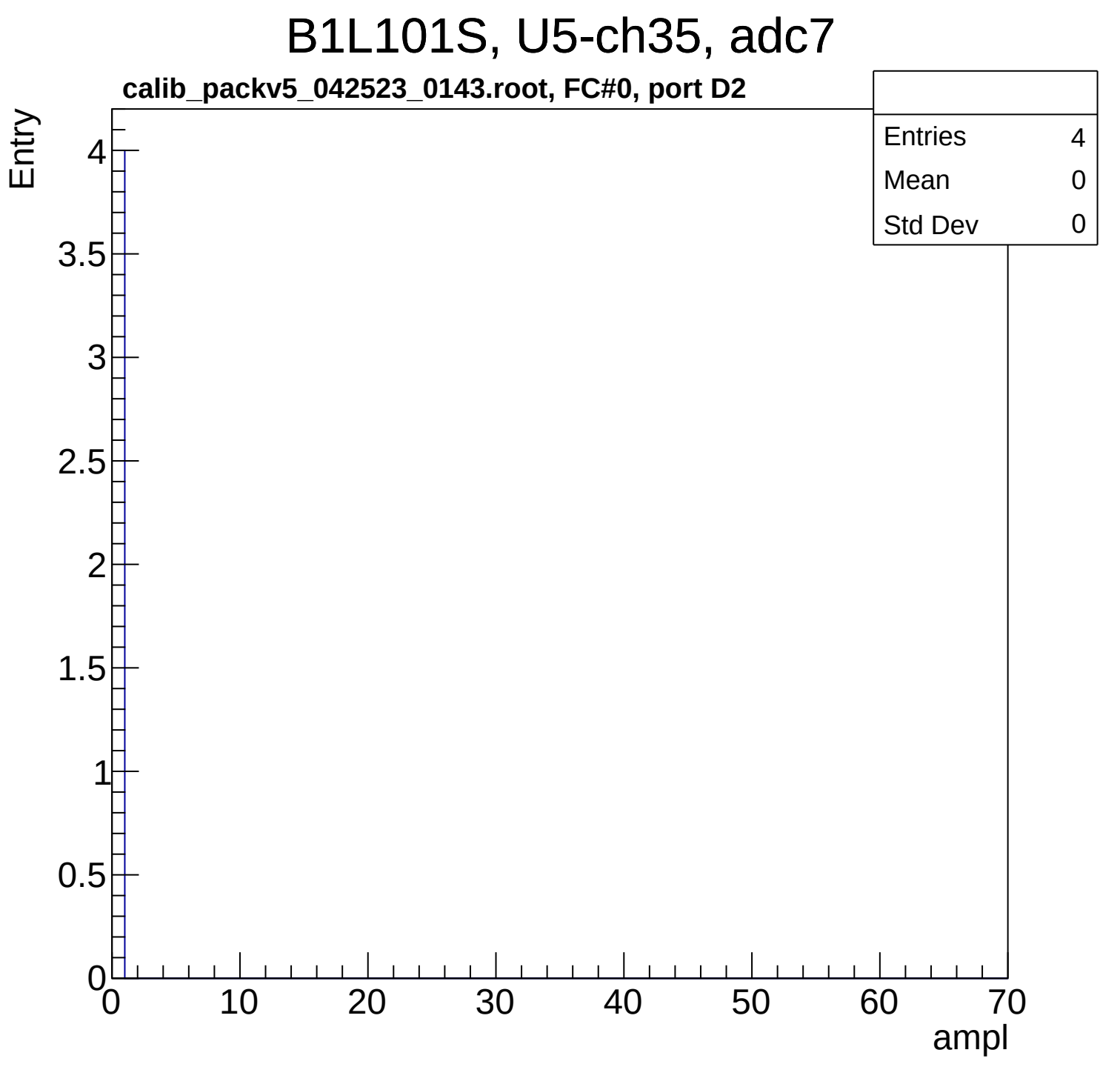
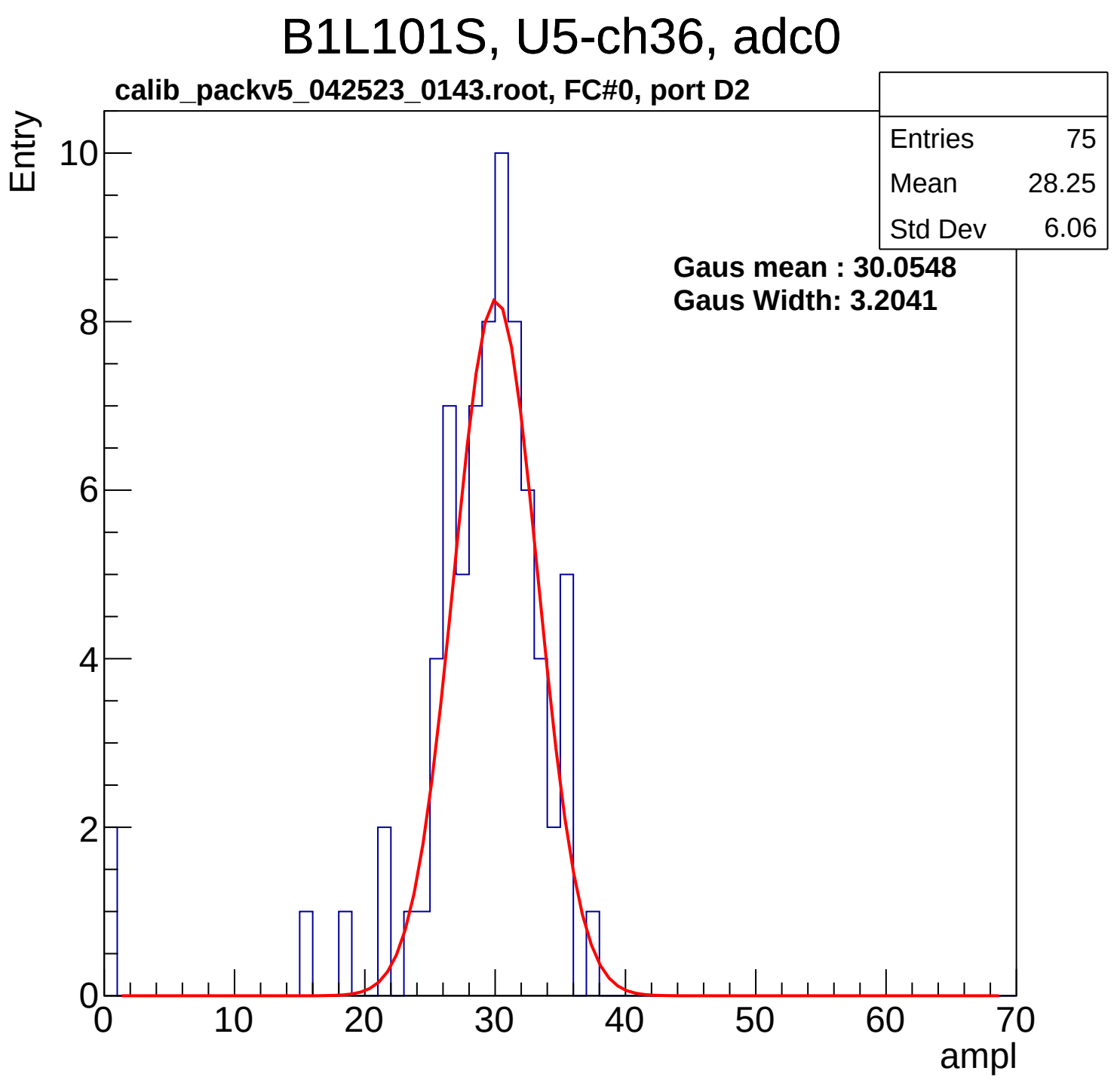
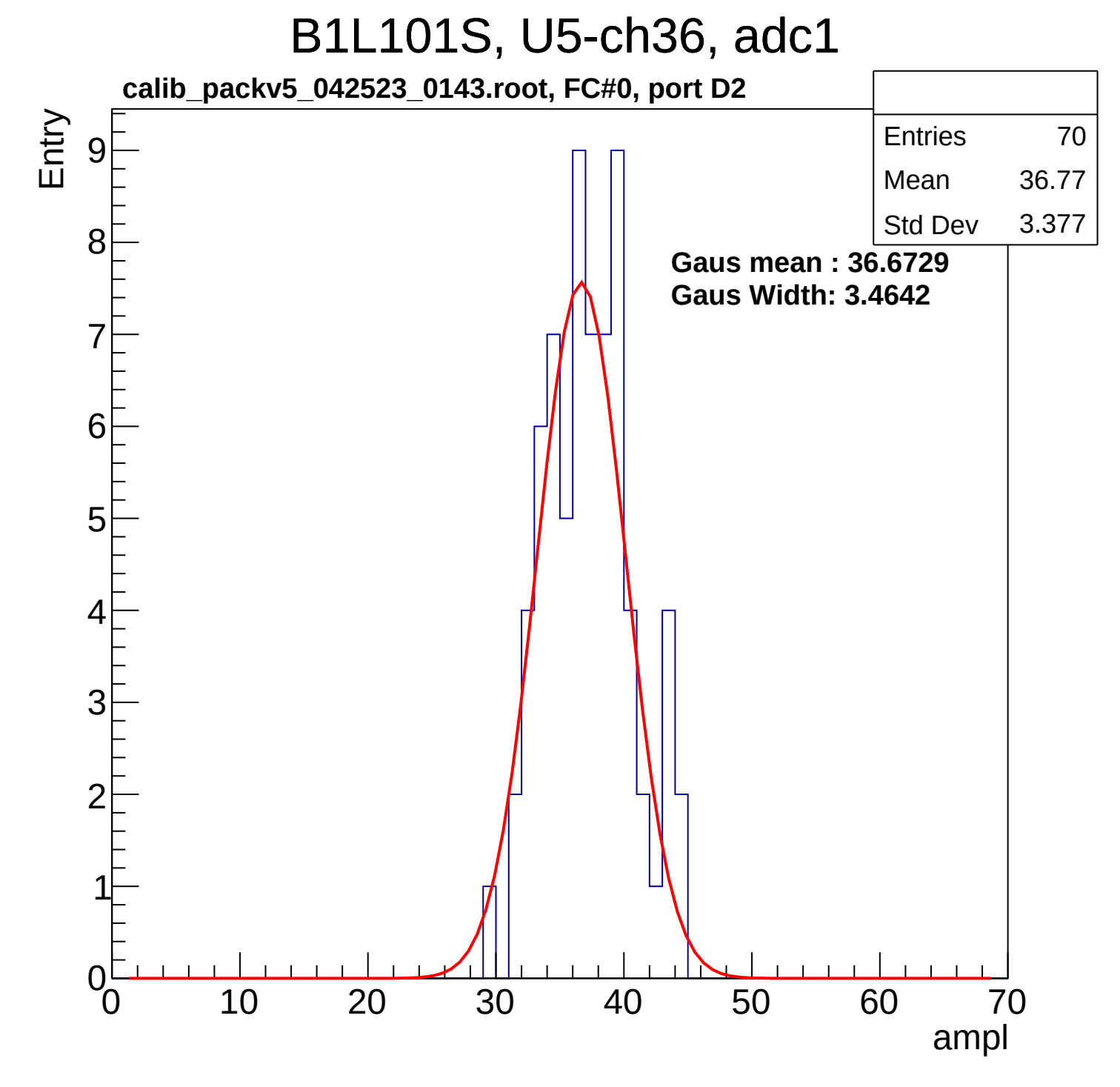
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L101S, U5-ch35, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 61.5
Std Dev 2.062
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U5-ch35, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 0
Std Dev 0
Entry
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch36, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 28.25
Std Dev 6.06
Gaus mean : 30.0548
Gaus Width: 3.2041
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch36, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 36.77
Std Dev 3.377
Gaus mean : 36.6729
Gaus Width: 3.4642
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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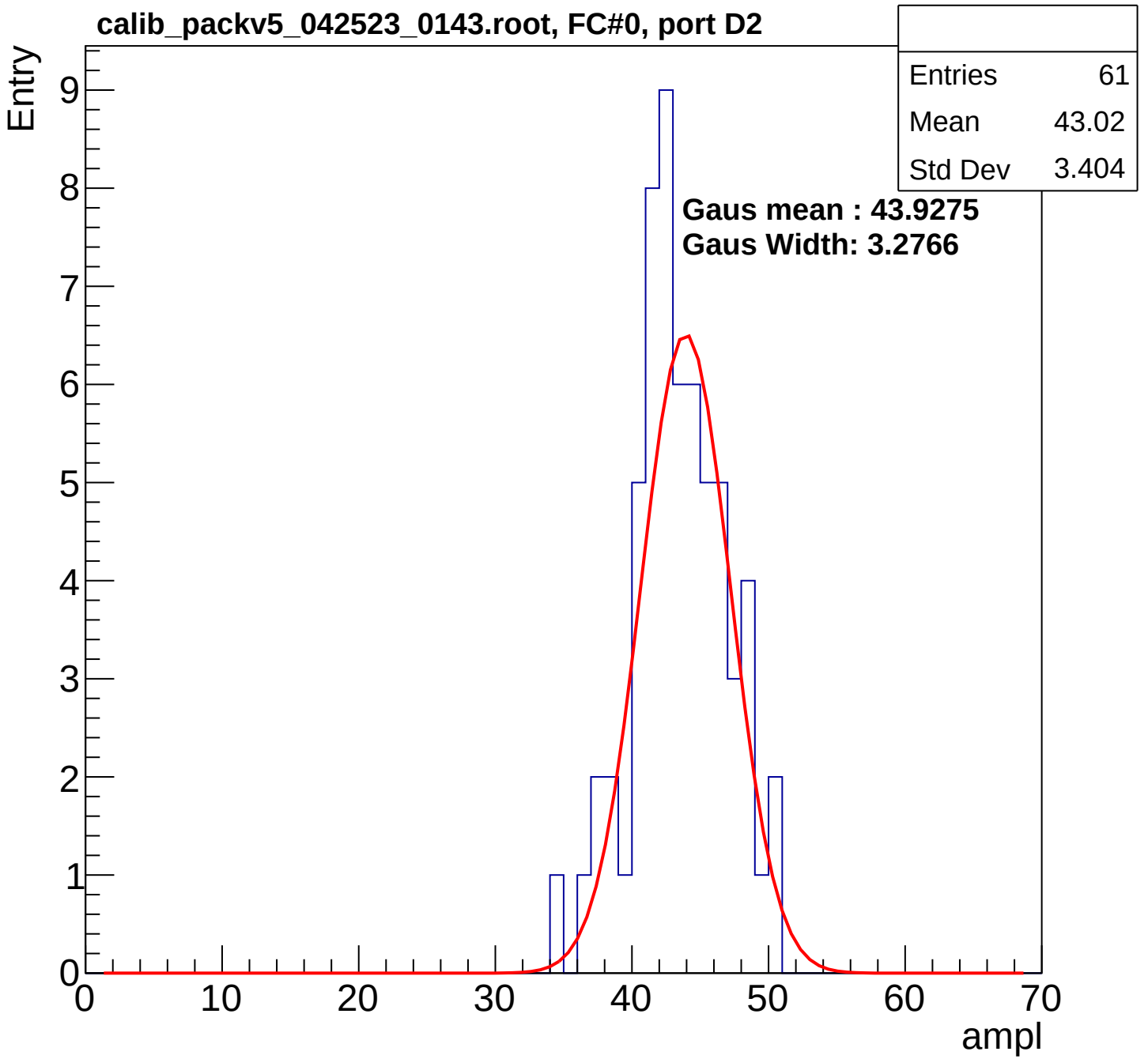
B1L101S, U5-ch36, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 43.02
Std Dev 3.404
Gaus mean : 43.9275
Gaus Width: 3.2766
Entry
ampl
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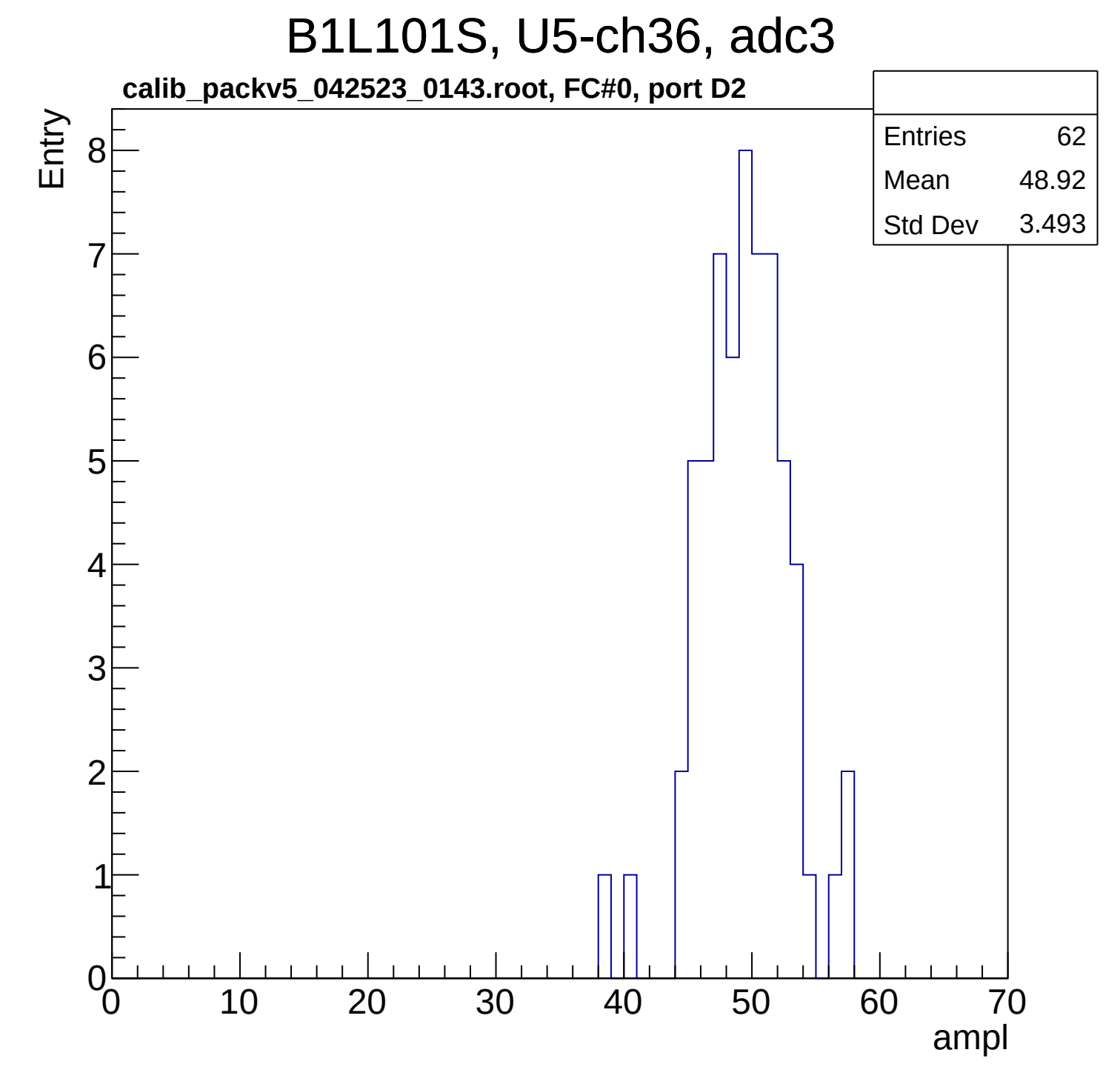
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L101S, U5-ch36, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 48.92
Std Dev 3.493
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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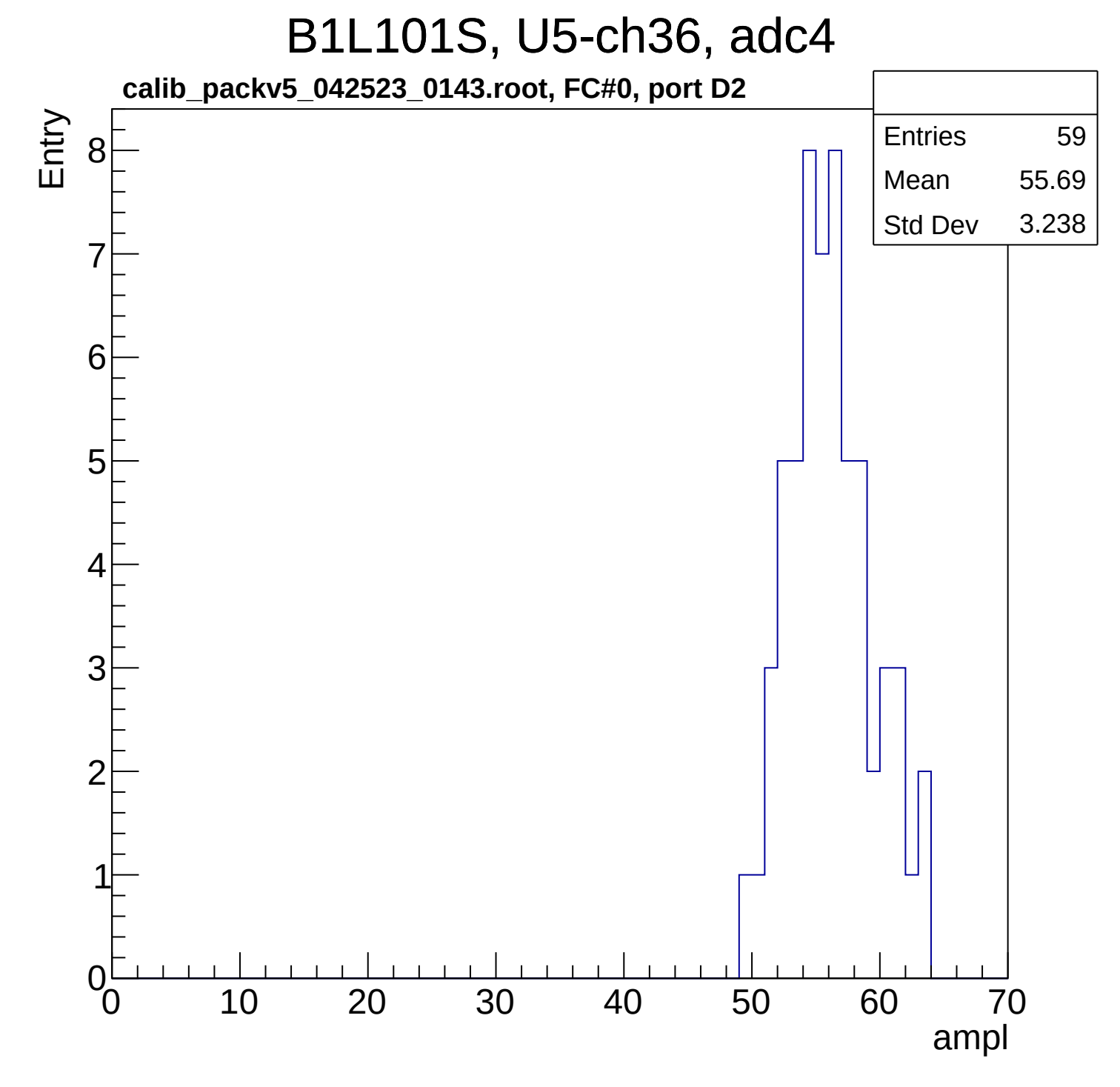
B1L101S, U5-ch36, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 55.69
Std Dev 3.238
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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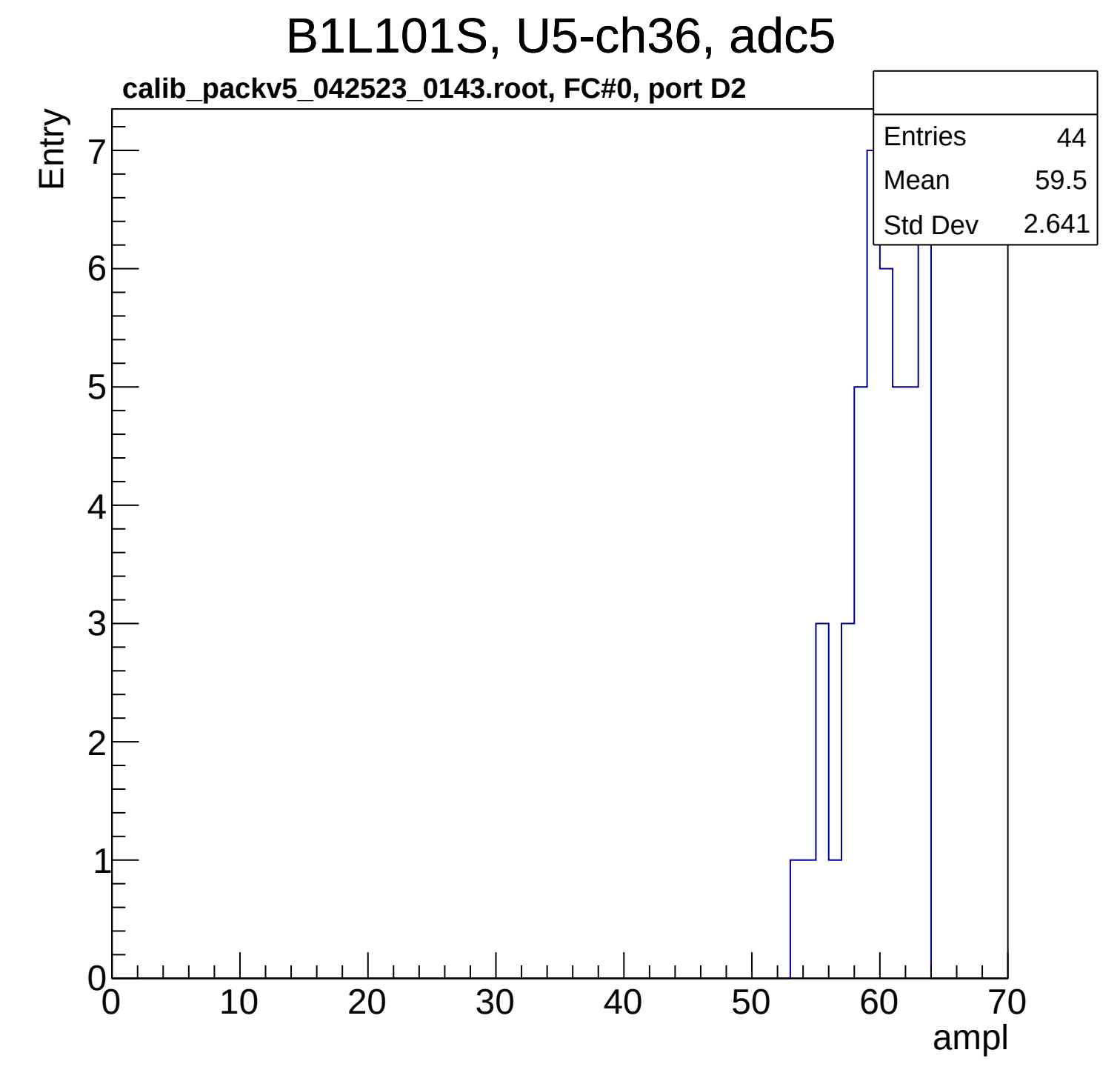
B1L101S, U5-ch36, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 44
Mean 59.5
Std Dev 2.641
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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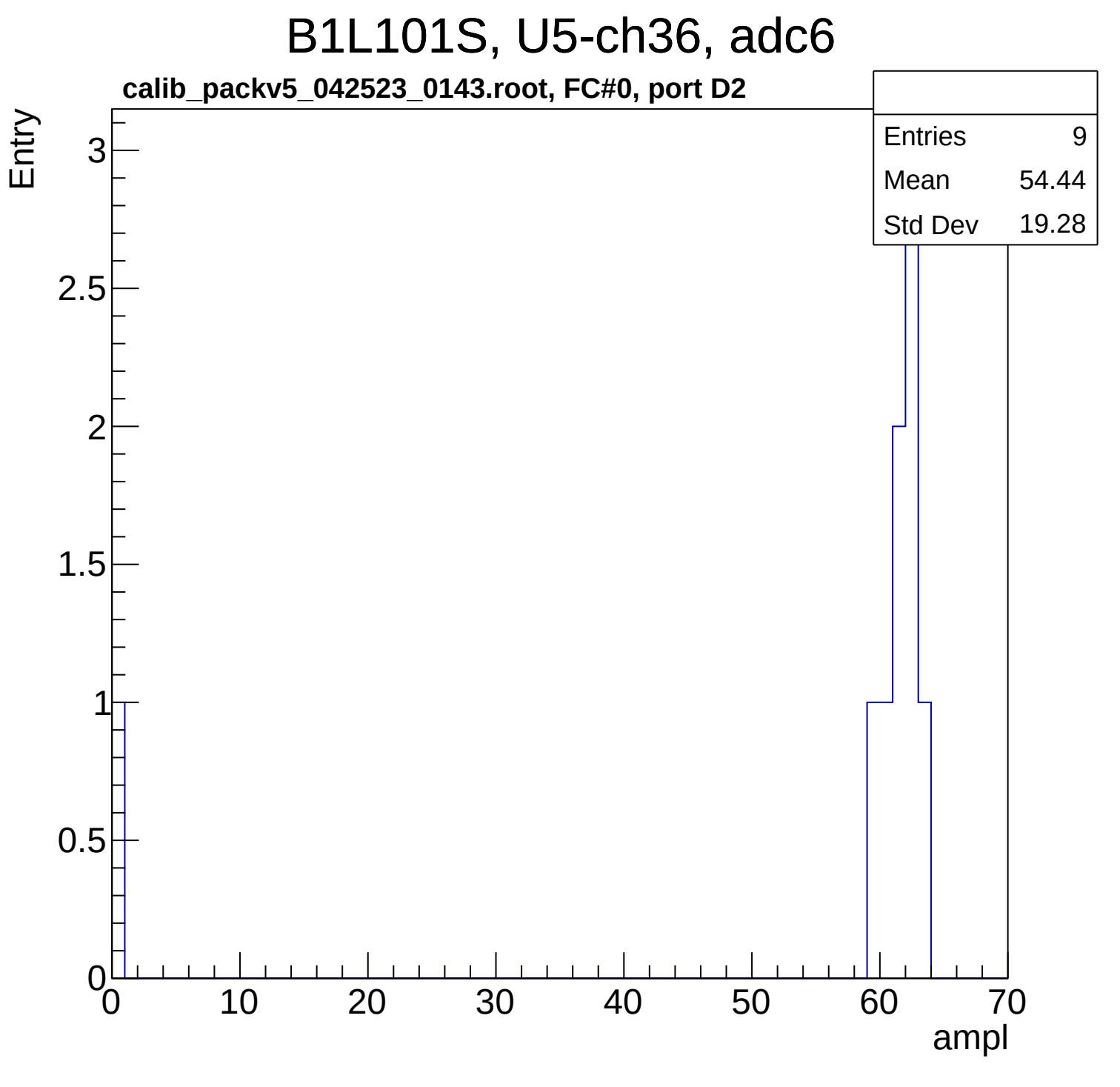
40
50
60
70


B1L101S, U5-ch36, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 54.44
Std Dev 19.28
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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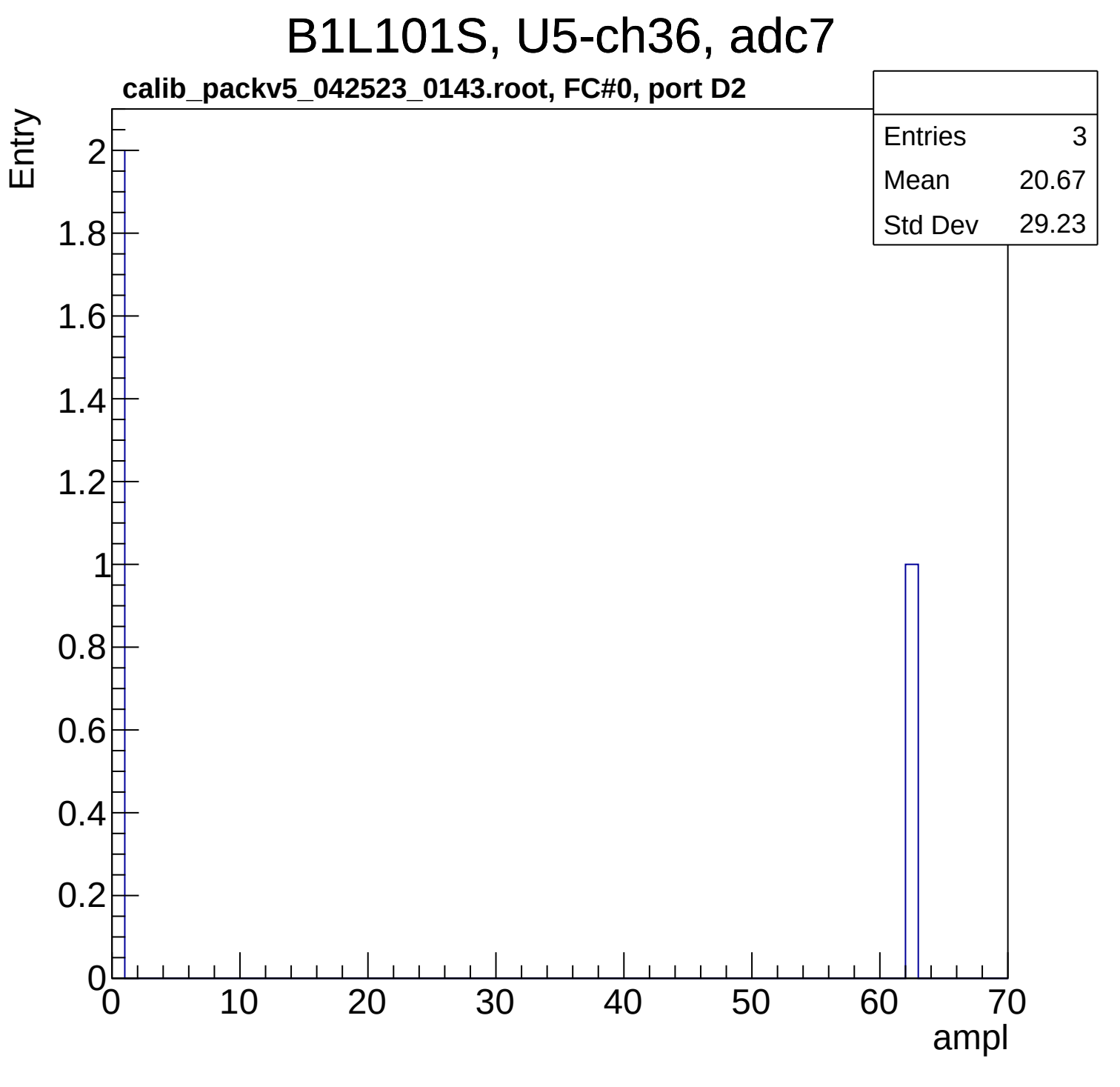
B1L101S, U5-ch36, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 20.67
Std Dev 29.23
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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30
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60
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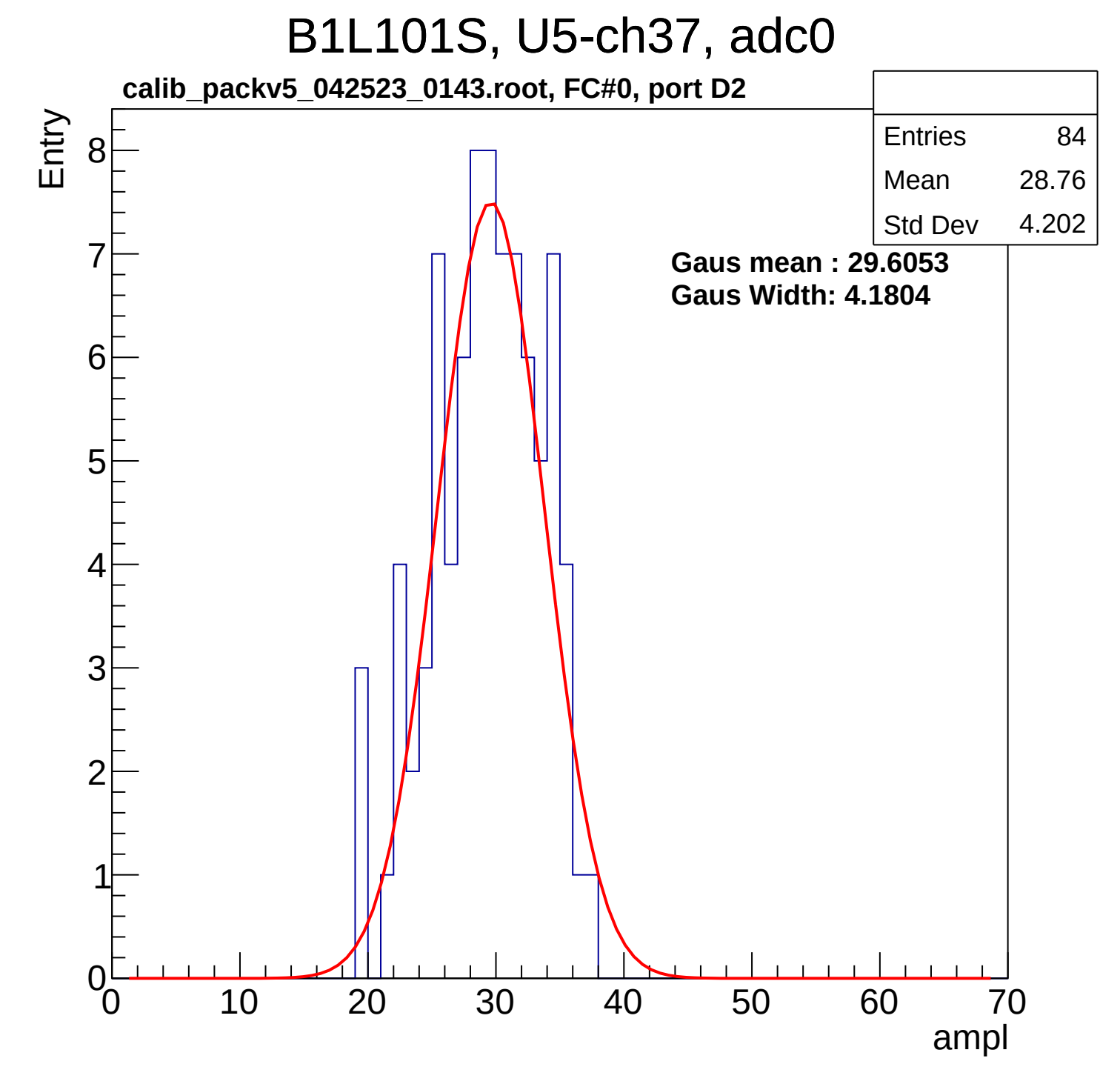
B1L101S, U5-ch37, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 84
Mean 28.76
Std Dev 4.202
Gaus mean : 29.6053
Gaus Width: 4.1804
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
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60
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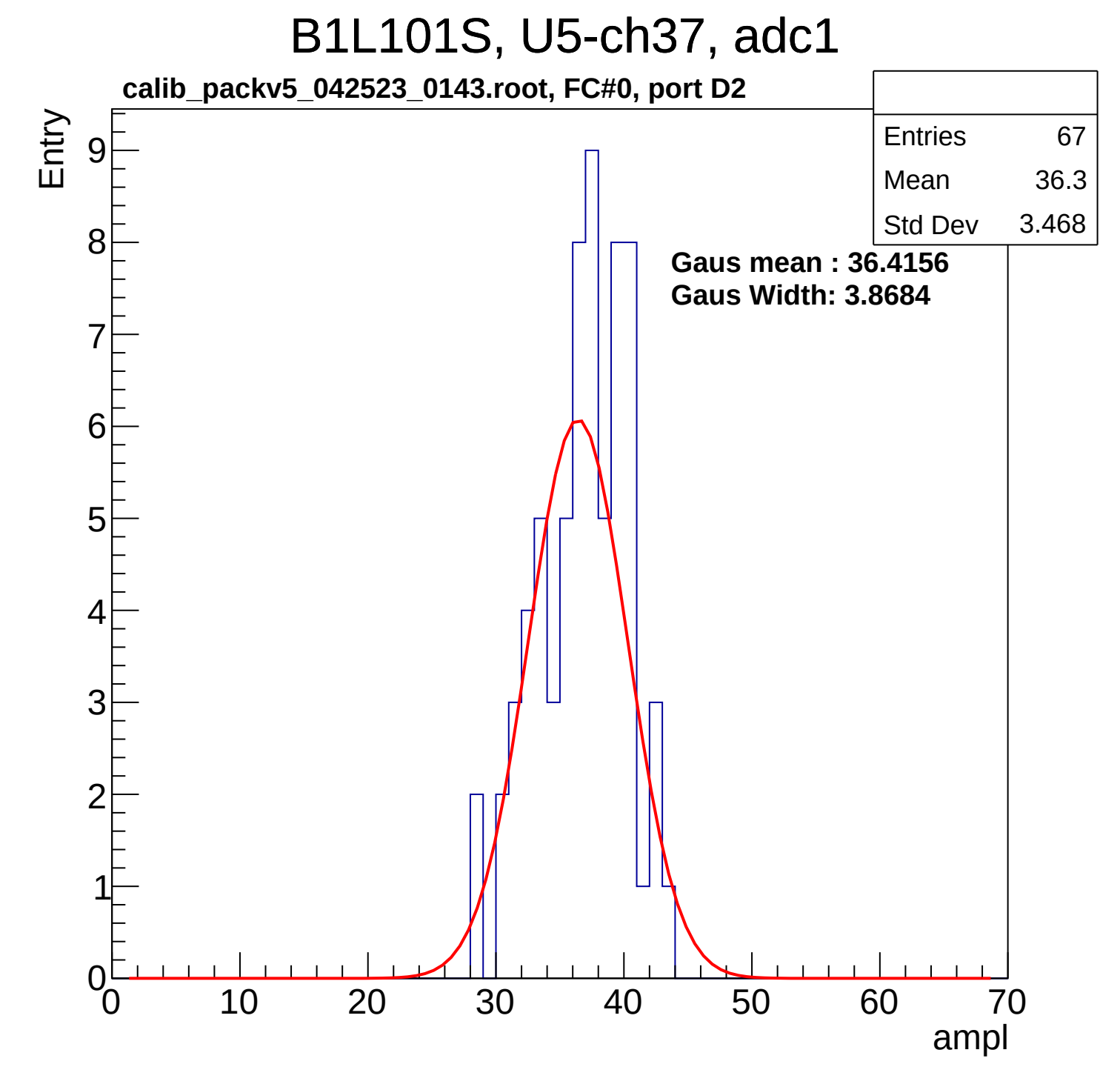
B1L101S, U5-ch37, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 36.3
Std Dev 3.468
Gaus mean : 36.4156
Gaus Width: 3.8684
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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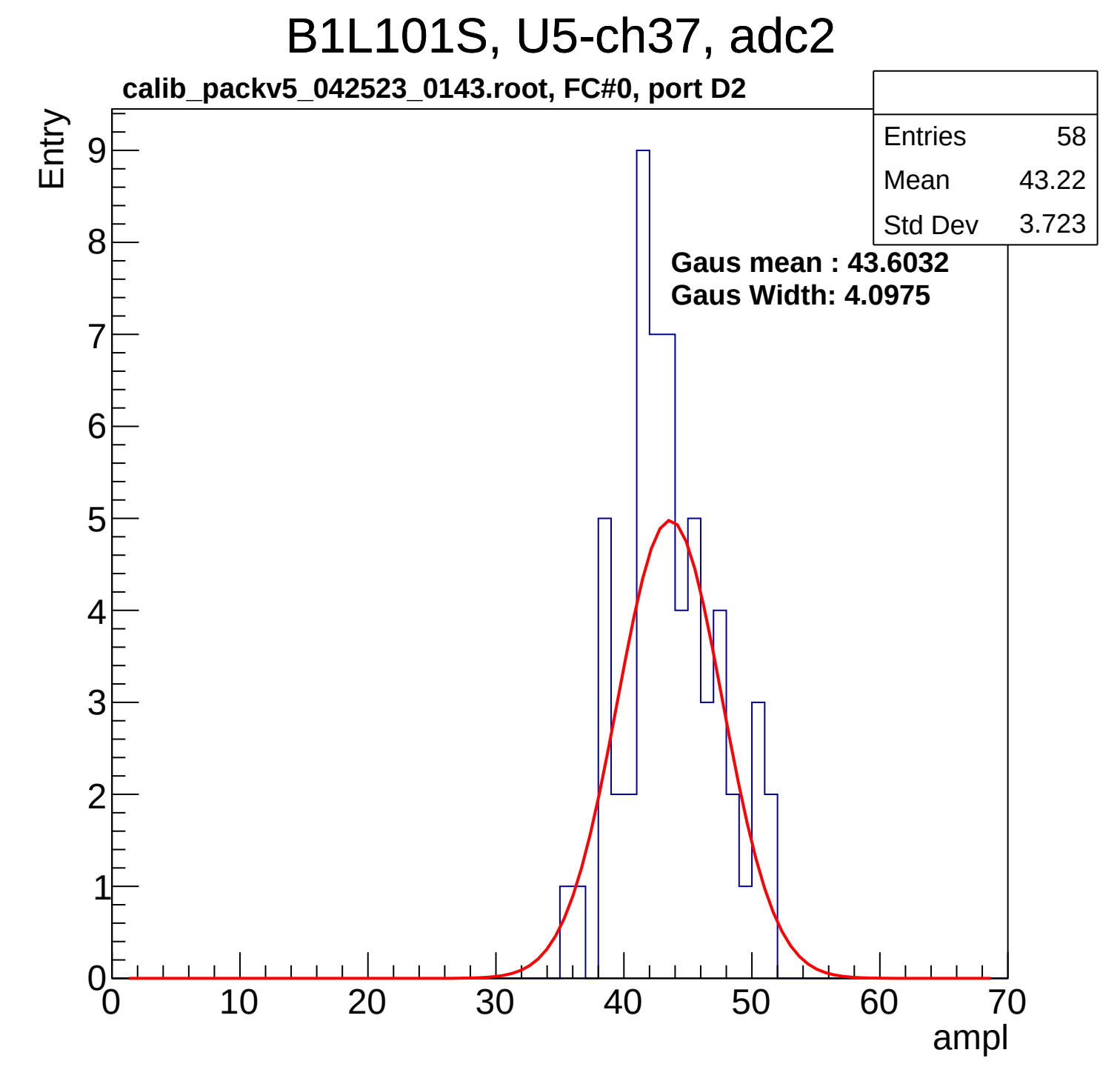
B1L101S, U5-ch37, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 43.22
Std Dev 3.723
Gaus mean : 43.6032
Gaus Width: 4.0975
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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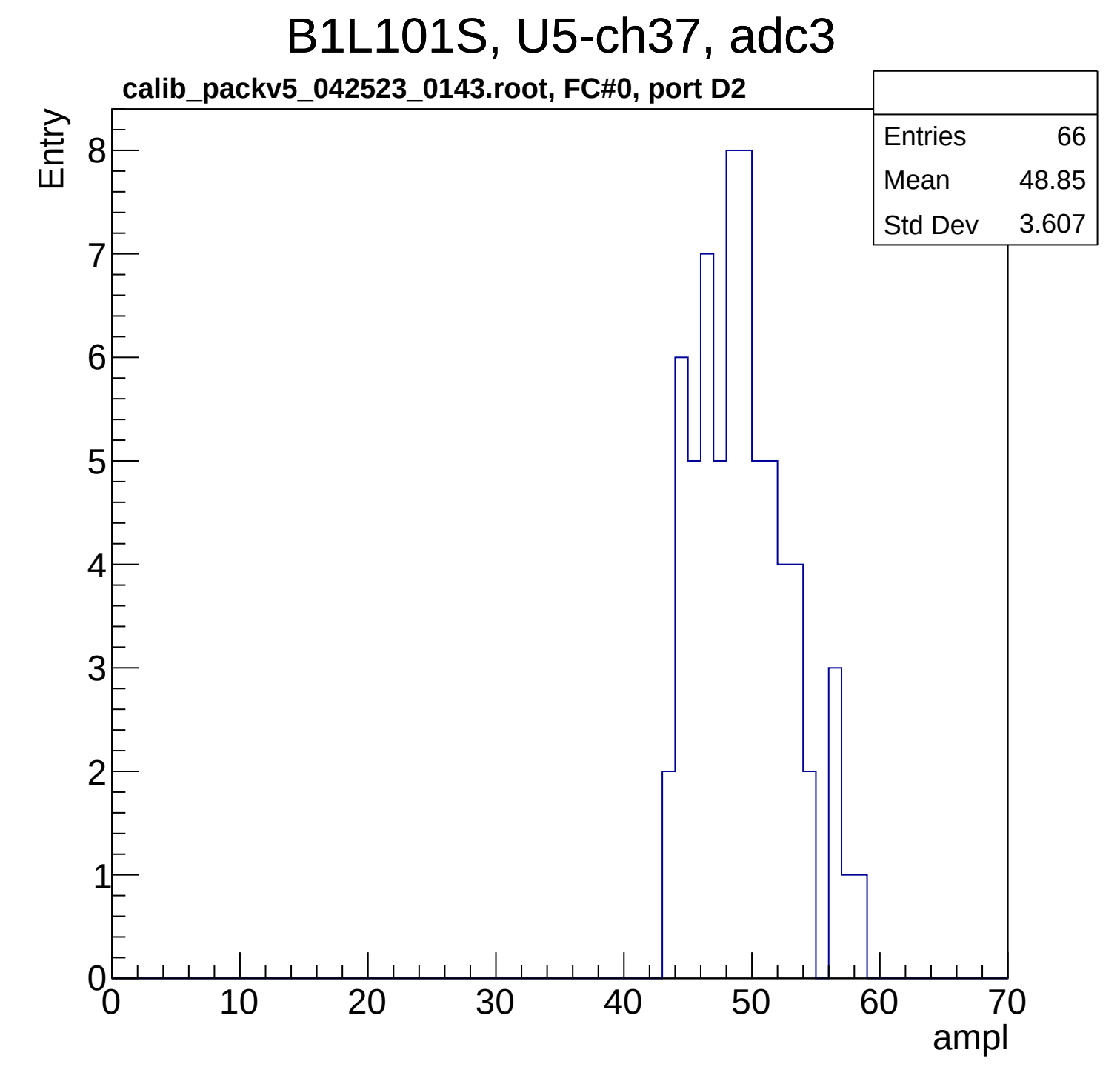
B1L101S, U5-ch37, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 48.85
Std Dev 3.607
Entry
ampl
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5
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7
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0
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60
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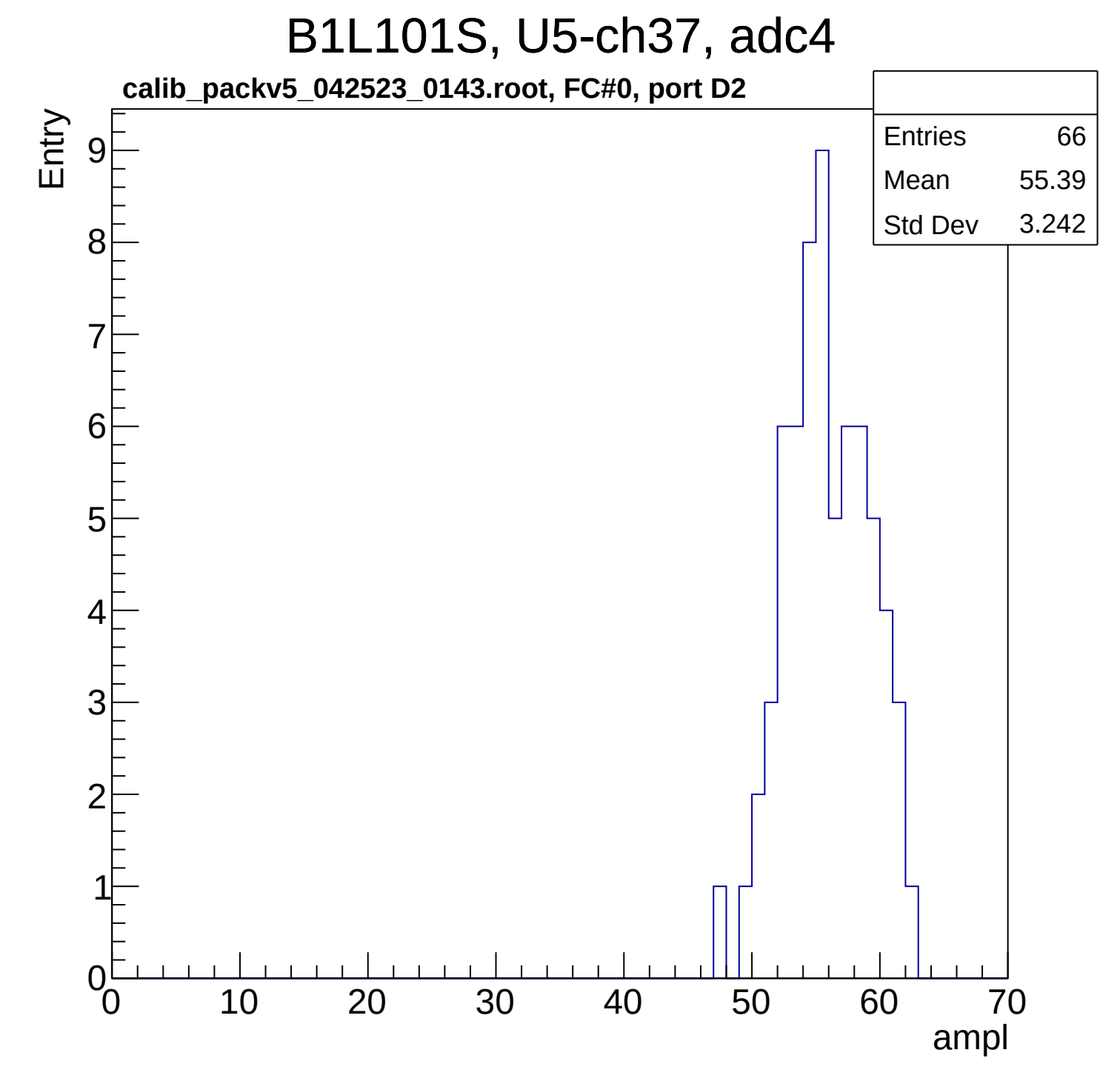
B1L101S, U5-ch37, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 55.39
Std Dev 3.242
Entry
ampl
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6
7
8
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0
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60
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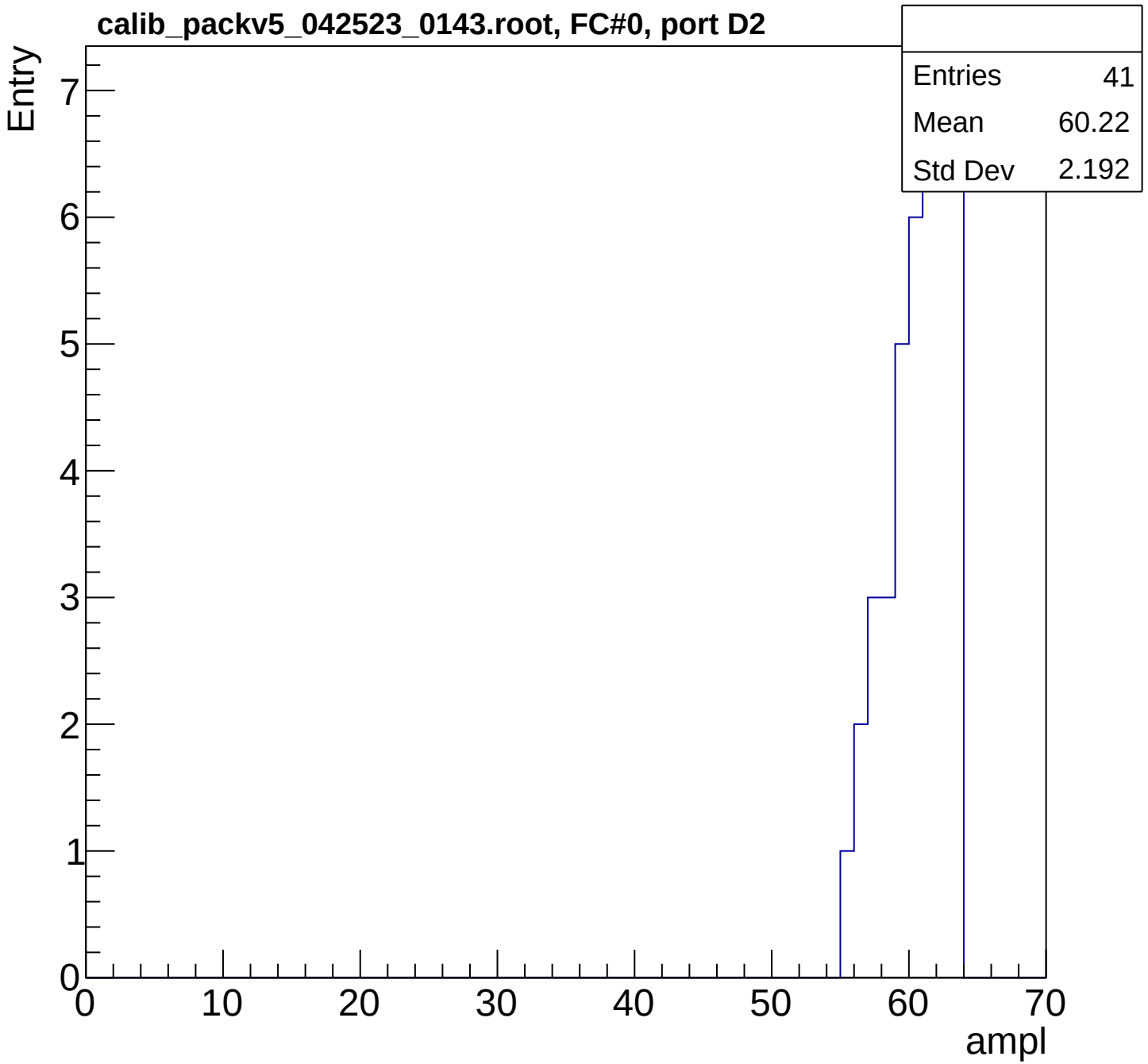
B1L101S, U5-ch37, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 41
Mean 60.22
Std Dev 2.192
Entry
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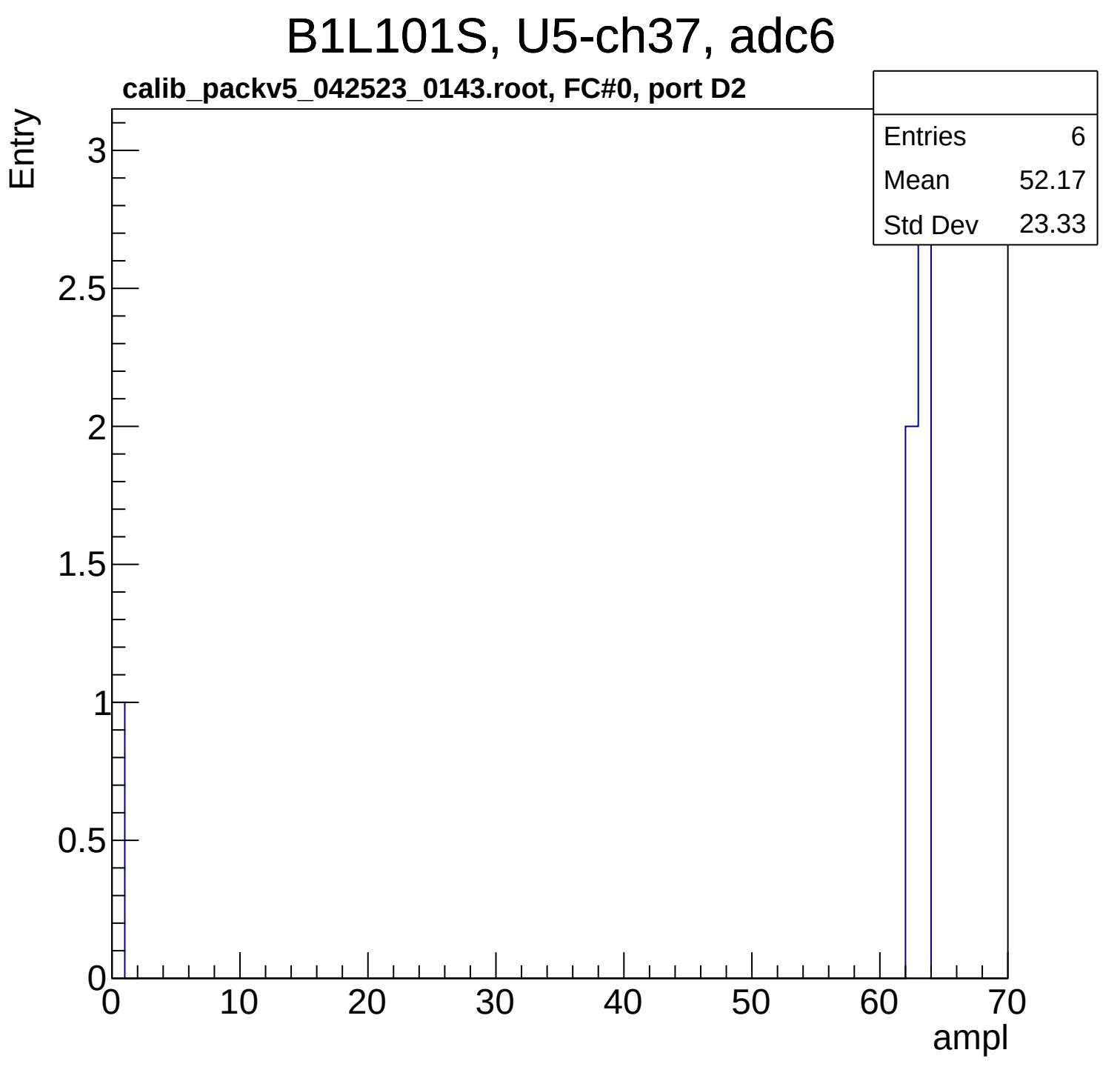
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch37, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 52.17
Std Dev 23.33
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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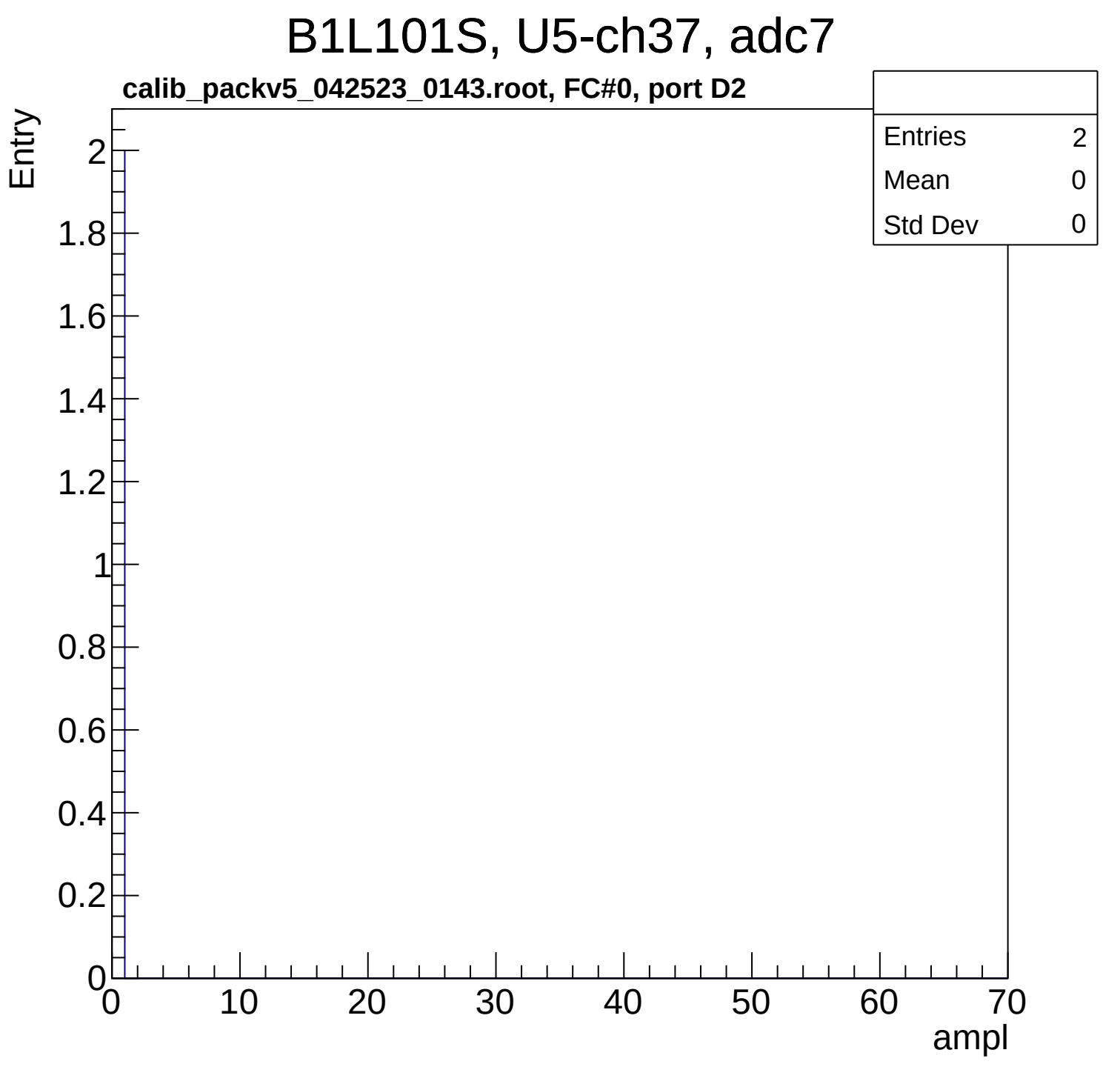
20
30
40
50
60
70


B1L101S, U5-ch37, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
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1.2
1.4
1.6
1.8
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0
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40
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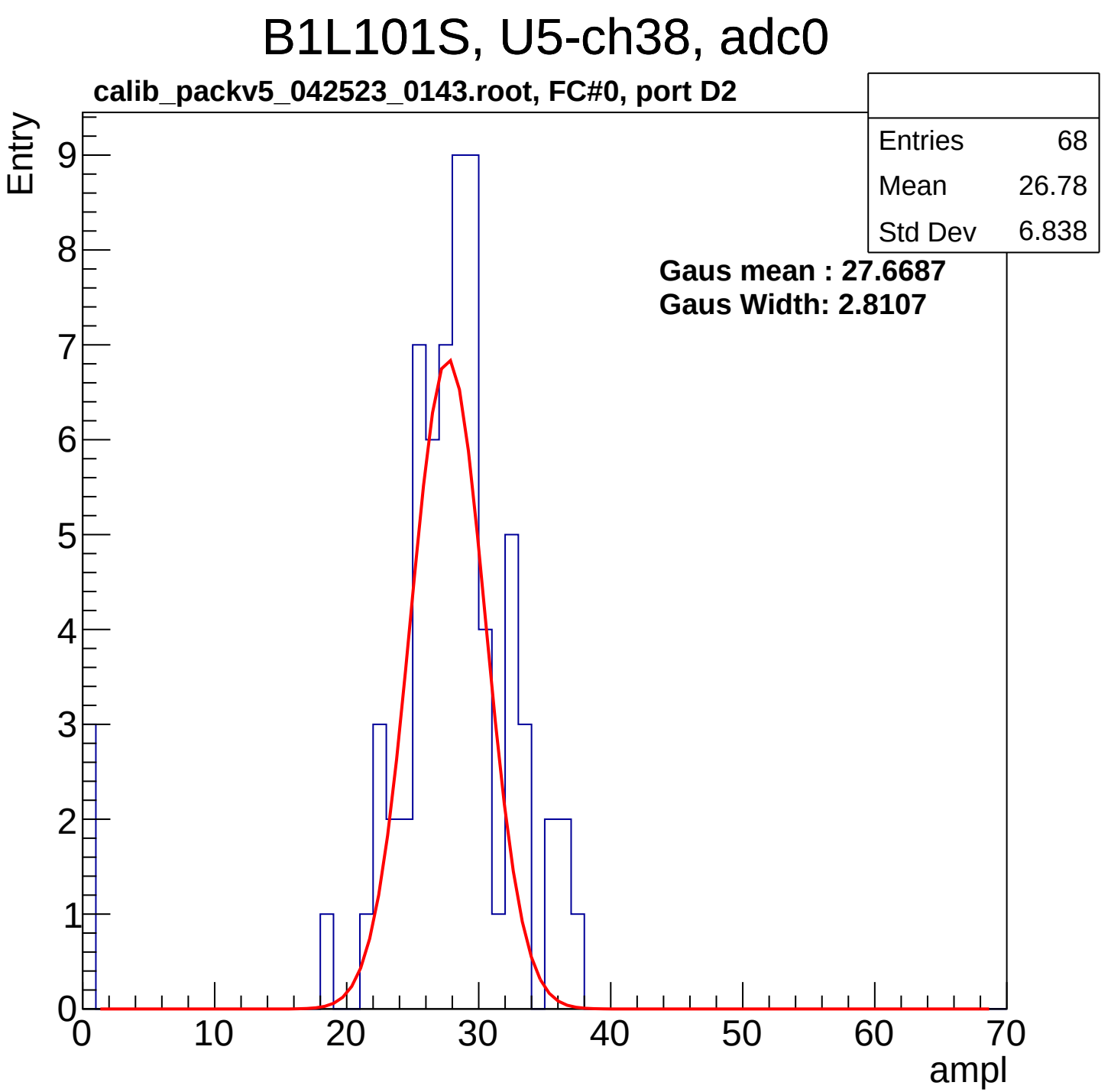
60
70


B1L101S, U5-ch38, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 26.78
Std Dev 6.838
Gaus mean : 27.6687
Gaus Width: 2.8107
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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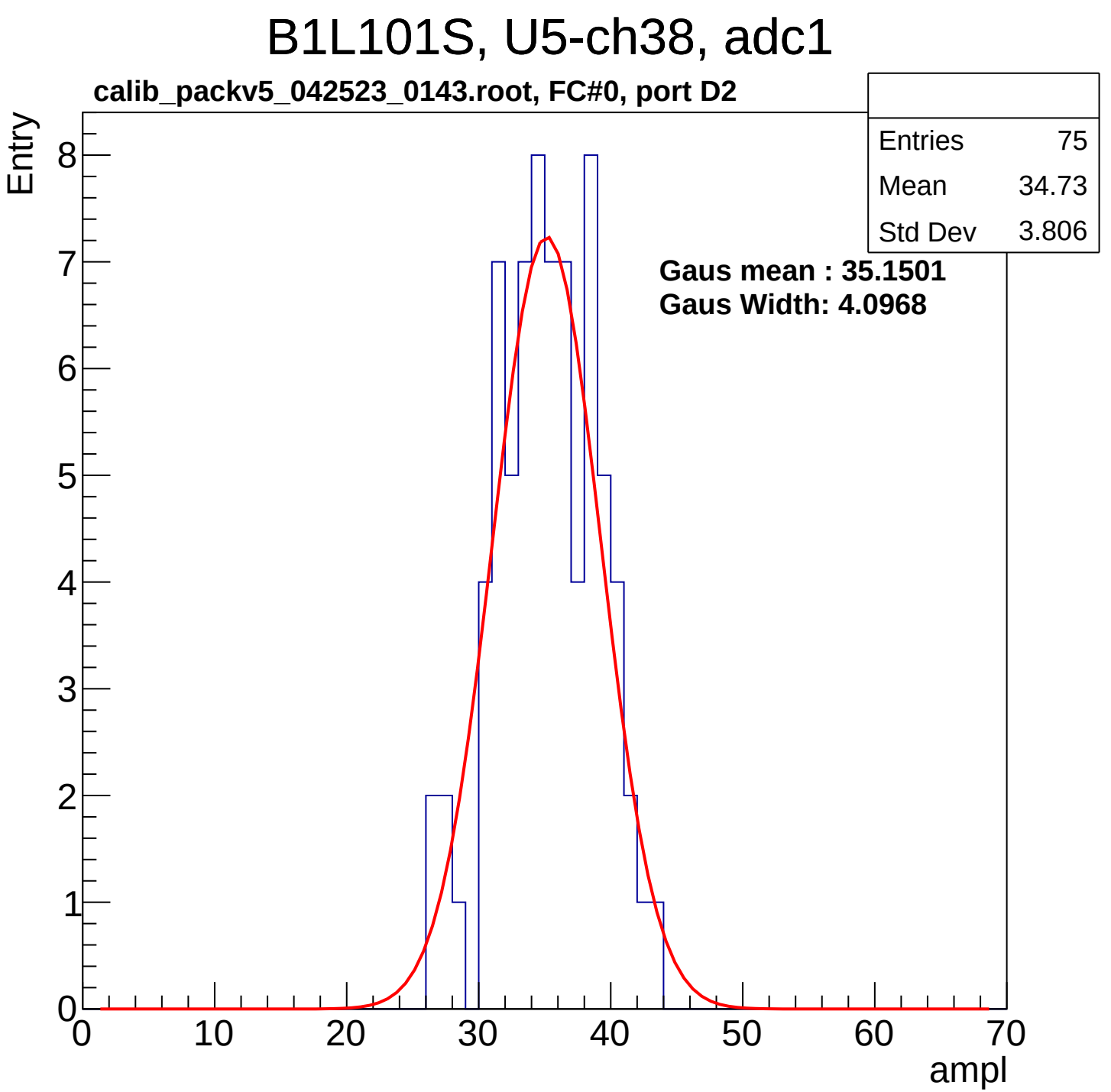
B1L101S, U5-ch38, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 34.73
Std Dev 3.806
Gaus mean : 35.1501
Gaus Width: 4.0968
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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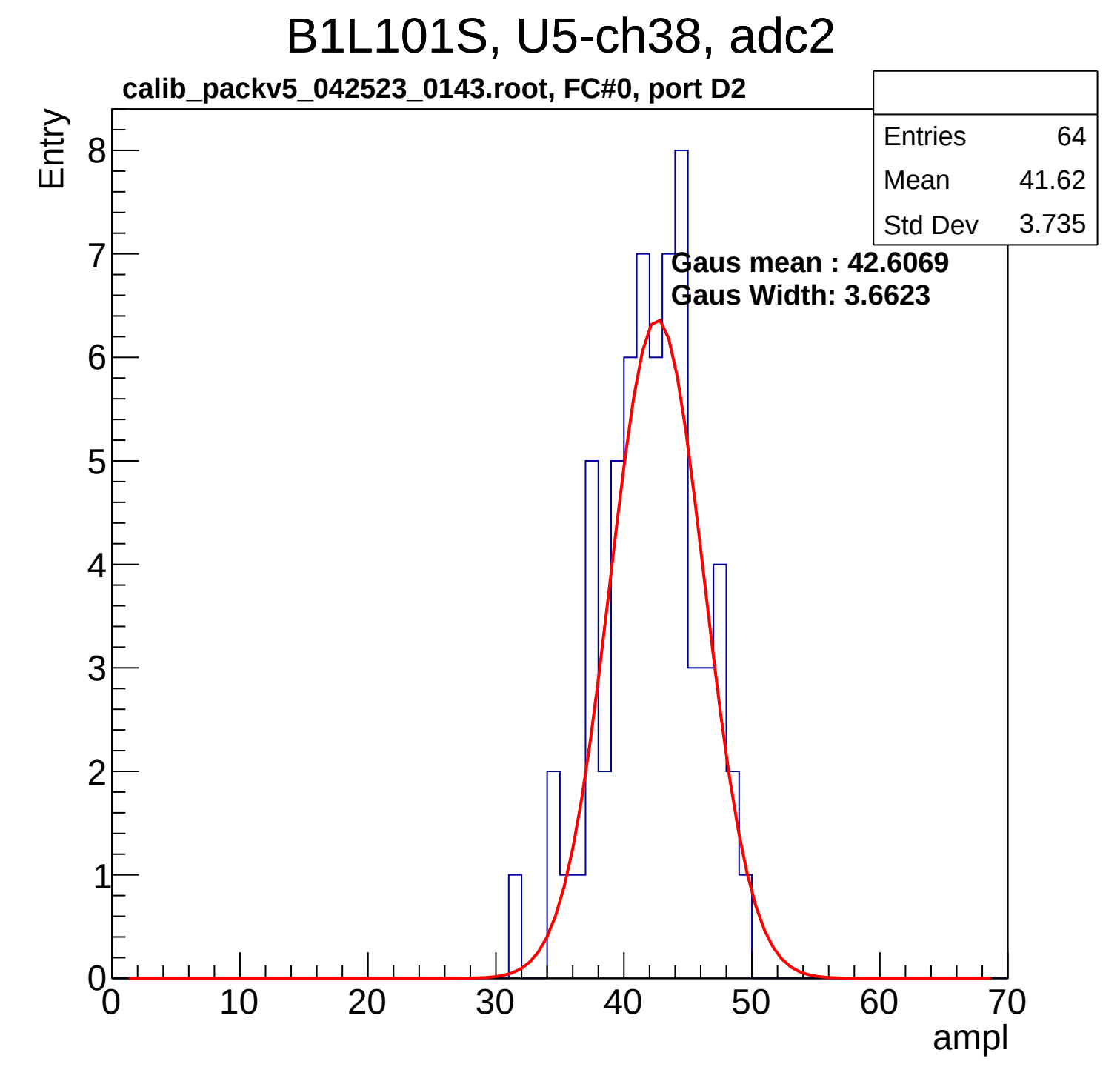
B1L101S, U5-ch38, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 41.62
Std Dev 3.735
Gaus mean : 42.6069
Gaus Width: 3.6623
Entry
ampl
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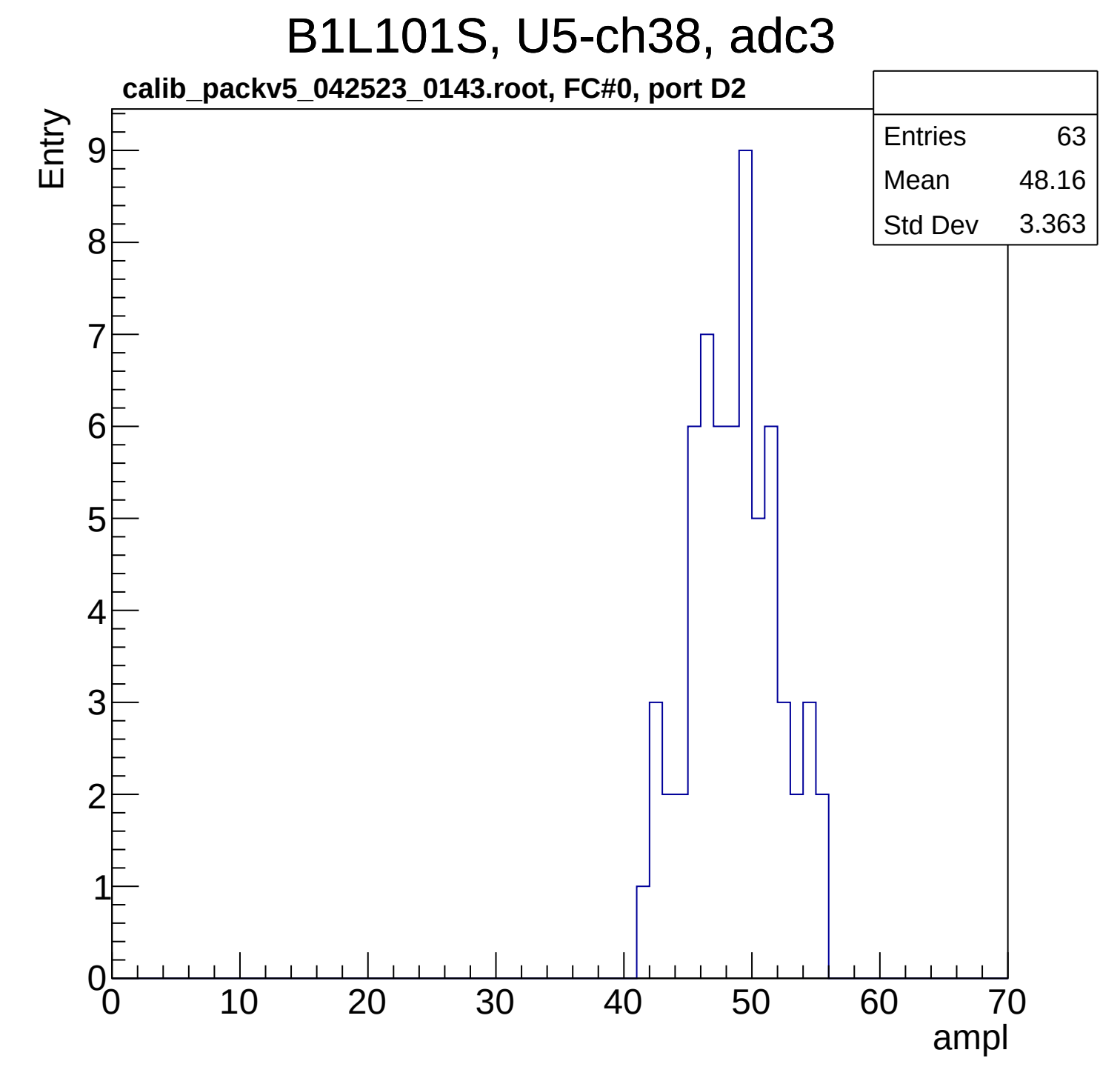
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch38, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 48.16
Std Dev 3.363
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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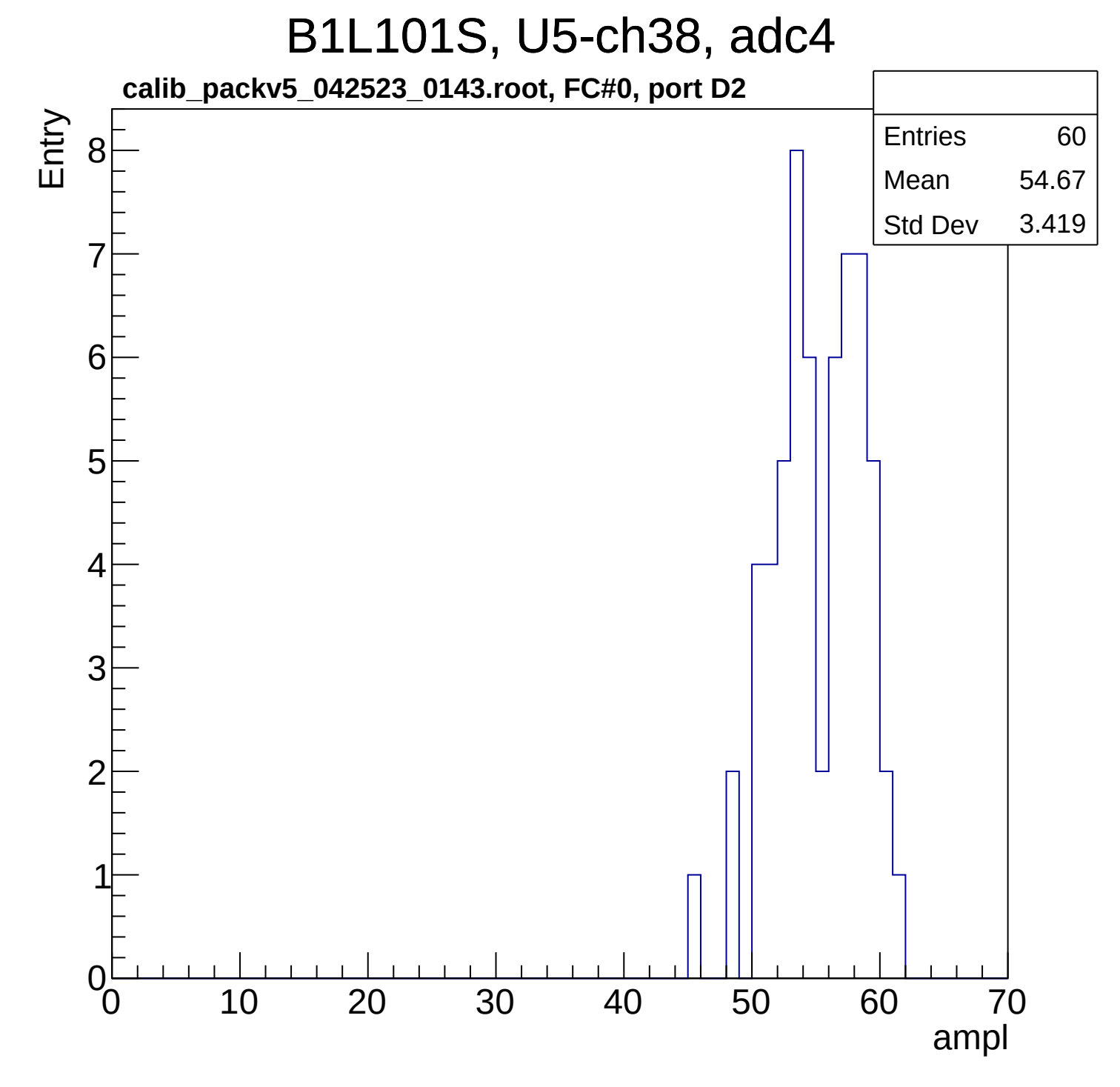
40
50
60
70


B1L101S, U5-ch38, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 54.67
Std Dev 3.419
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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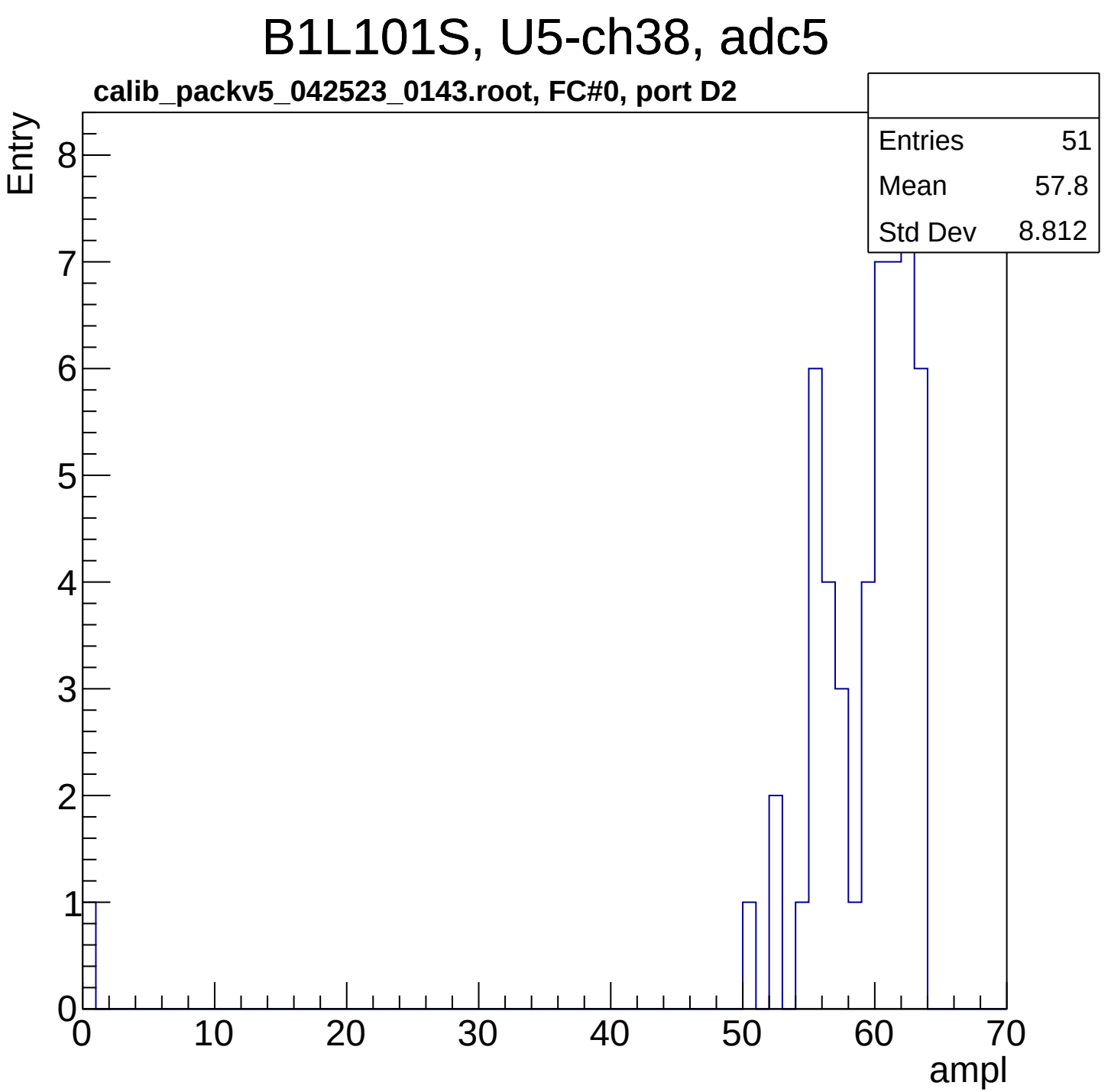
B1L101S, U5-ch38, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 57.8
Std Dev 8.812
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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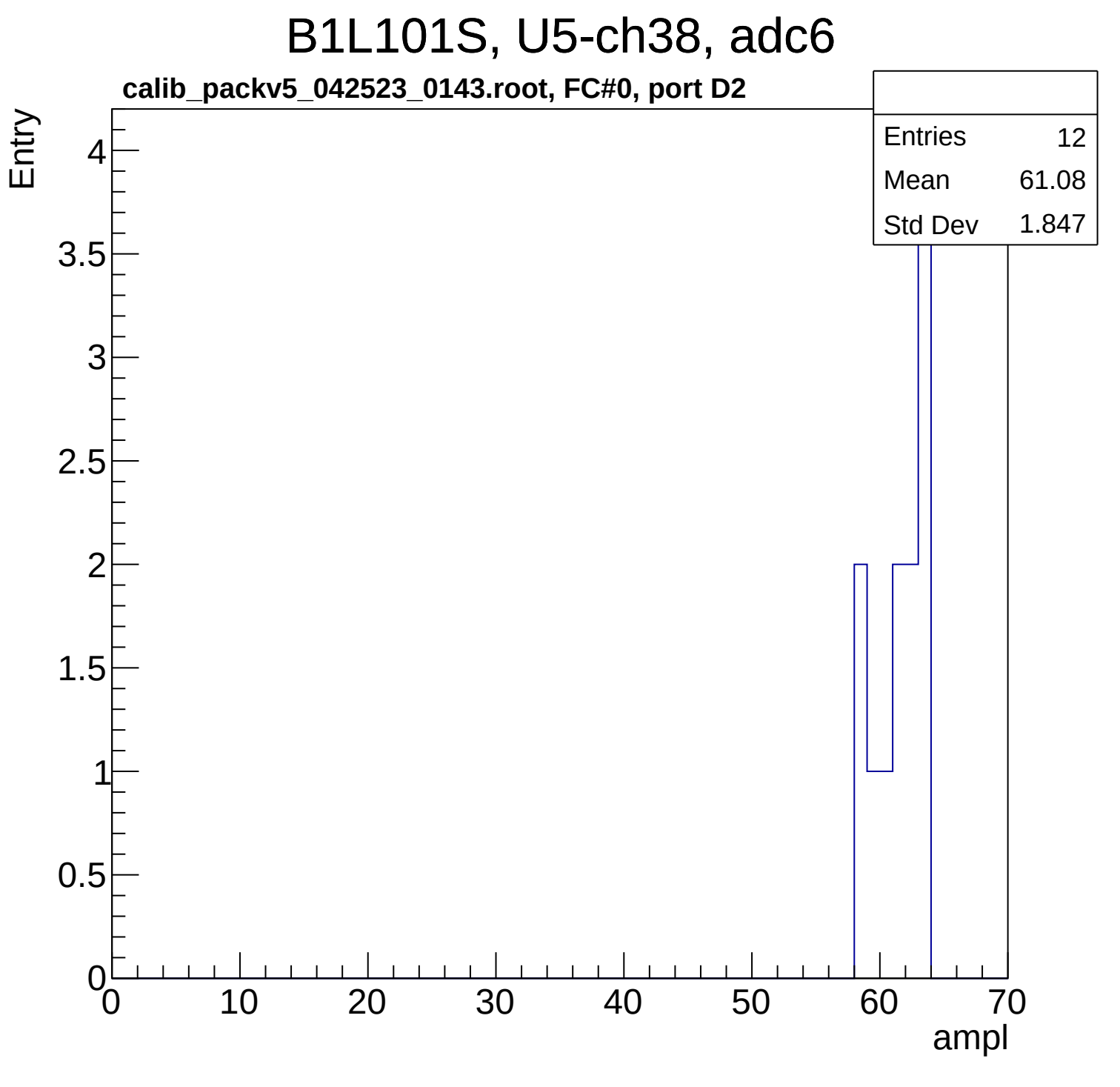
B1L101S, U5-ch38, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 12
Mean 61.08
Std Dev 1.847
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
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40
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60
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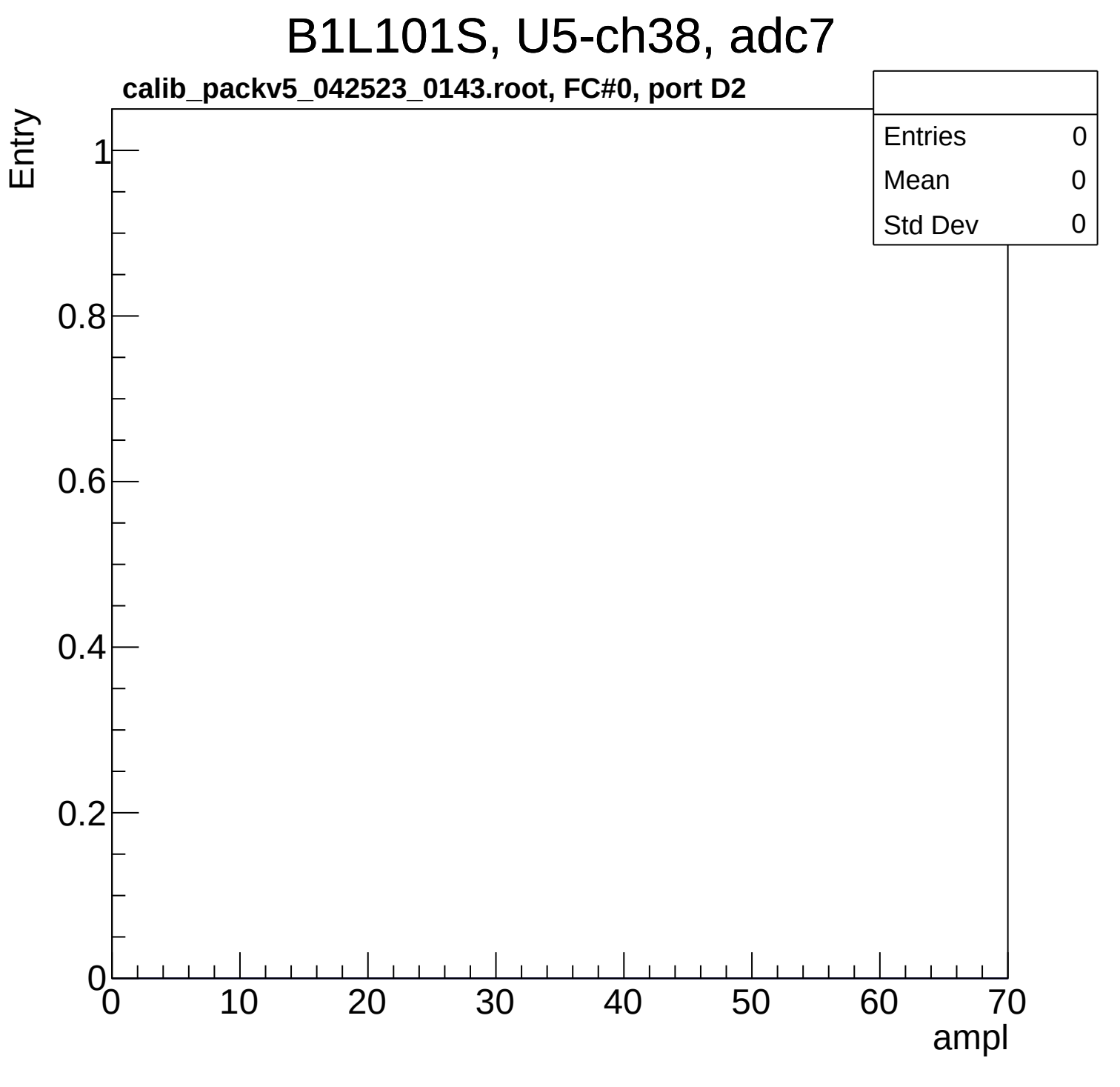
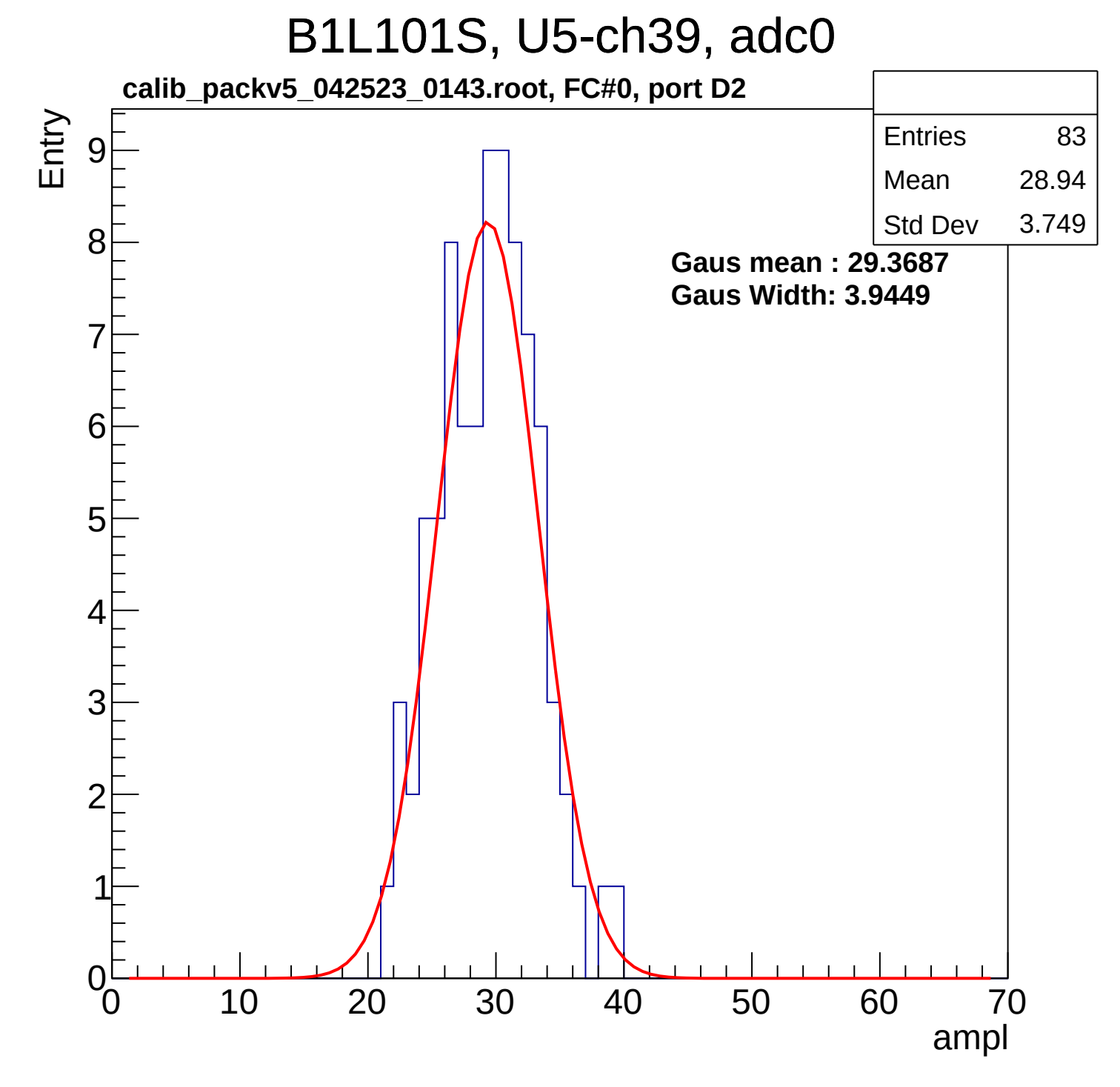
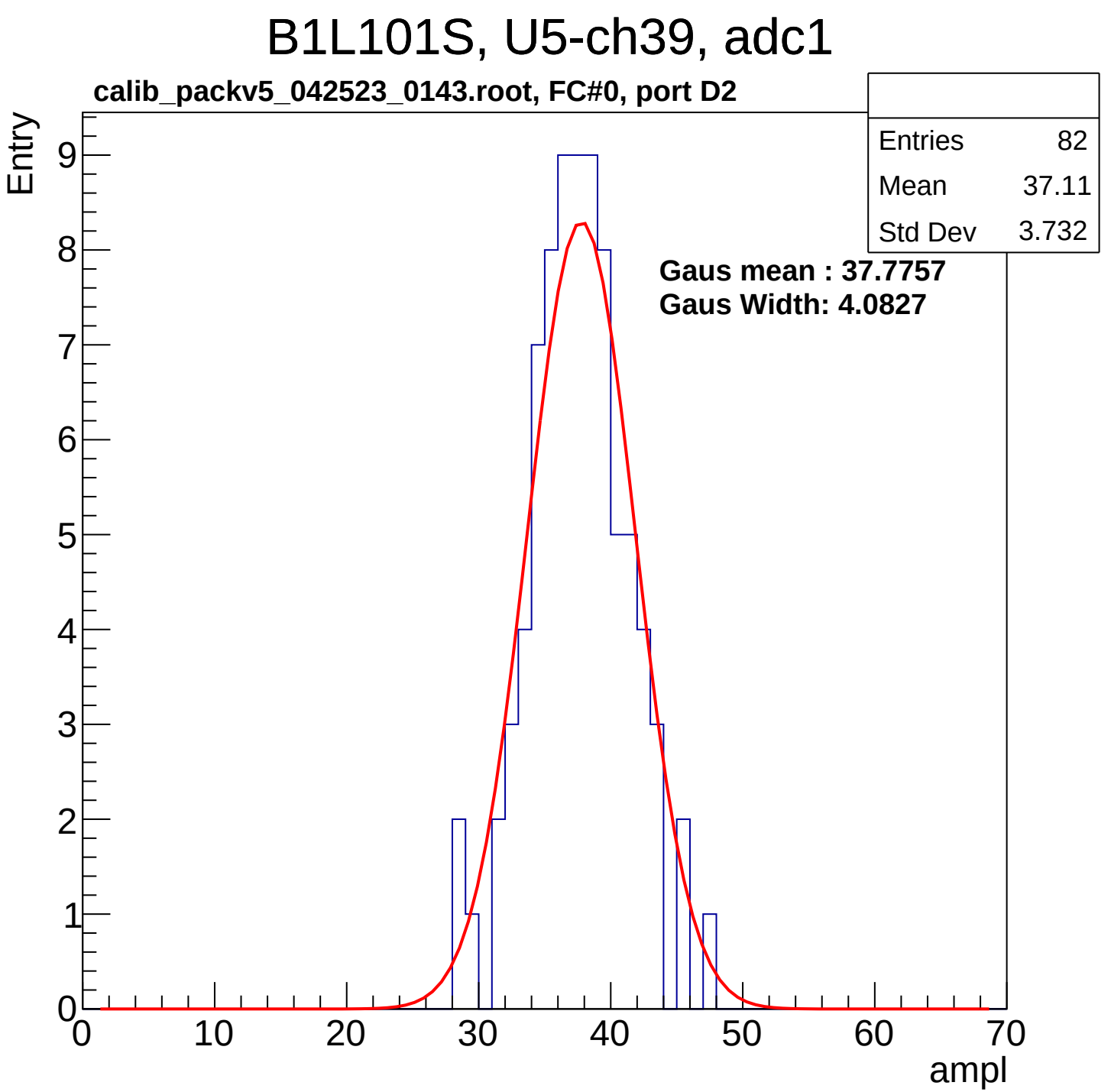

B1L101S, U5-ch38, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch39, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 83
Mean 28.94
Std Dev 3.749
Gaus mean : 29.3687
Gaus Width: 3.9449
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L101S, U5-ch39, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 82
Mean 37.11
Std Dev 3.732
Gaus mean : 37.7757
Gaus Width: 4.0827
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
30
40
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60
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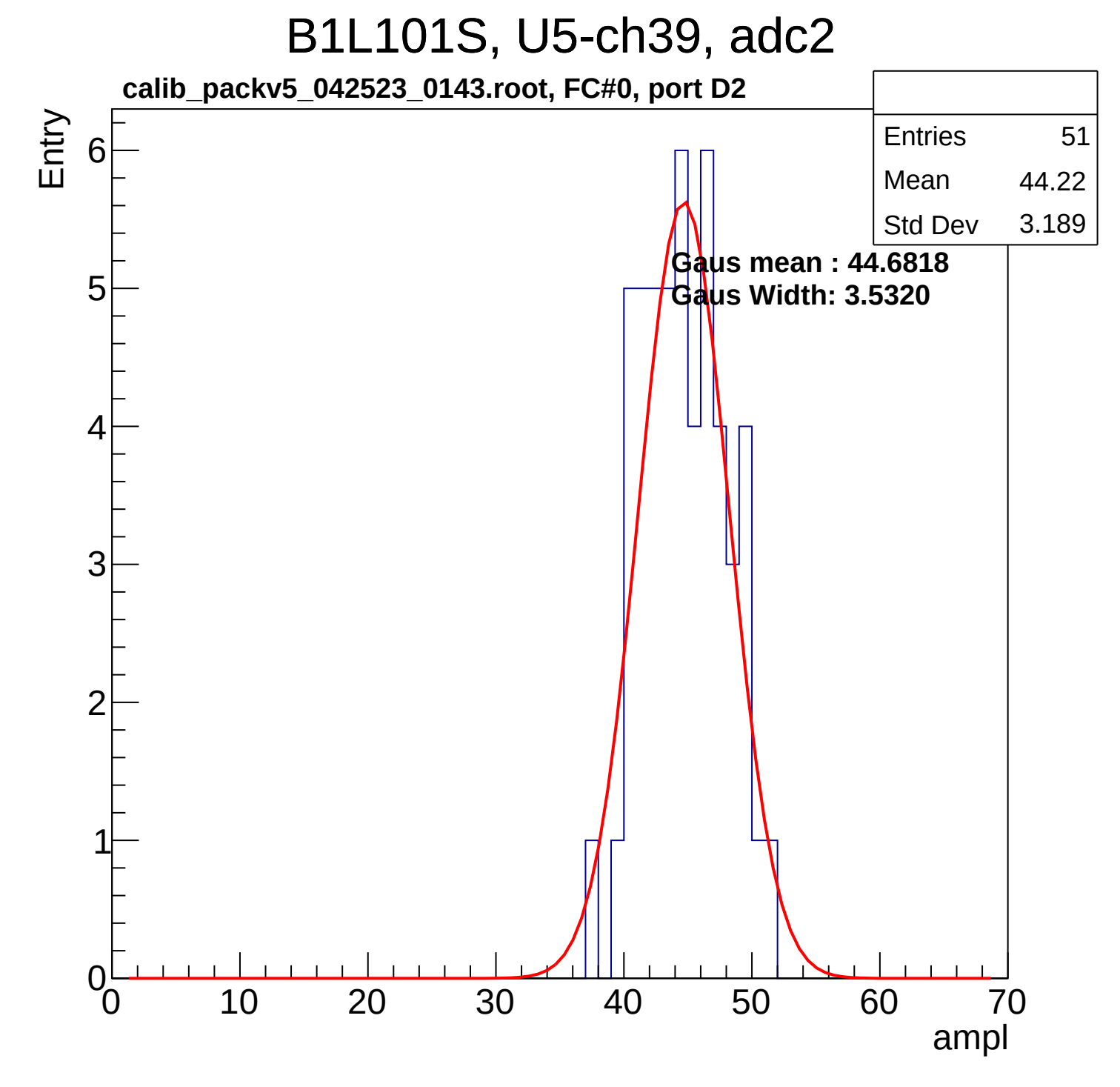
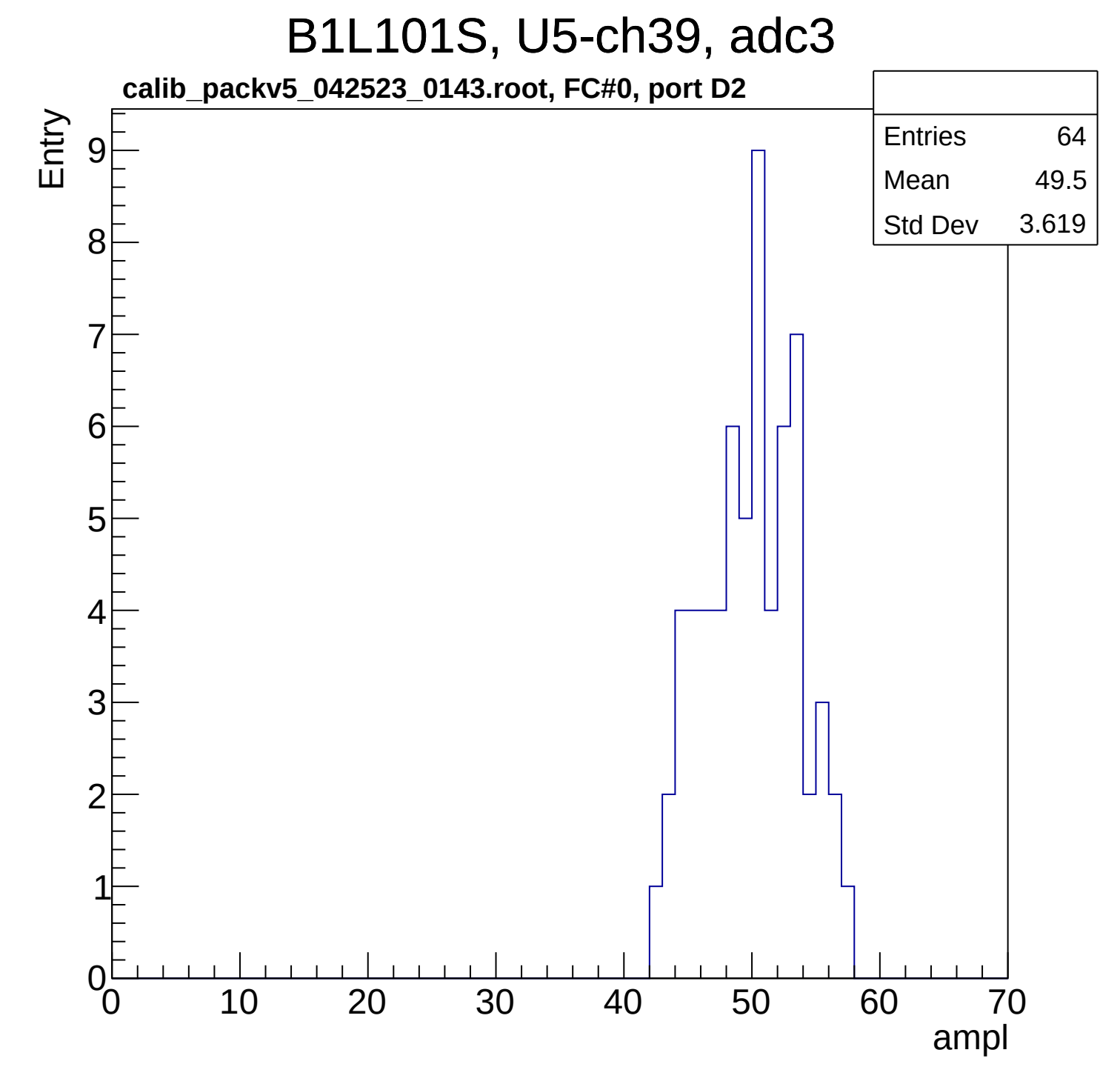

B1L101S, U5-ch39, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 44.22
Std Dev 3.189
Gaus mean : 44.6818
Gaus Width: 3.5320
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L101S, U5-ch39, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 49.5
Std Dev 3.619
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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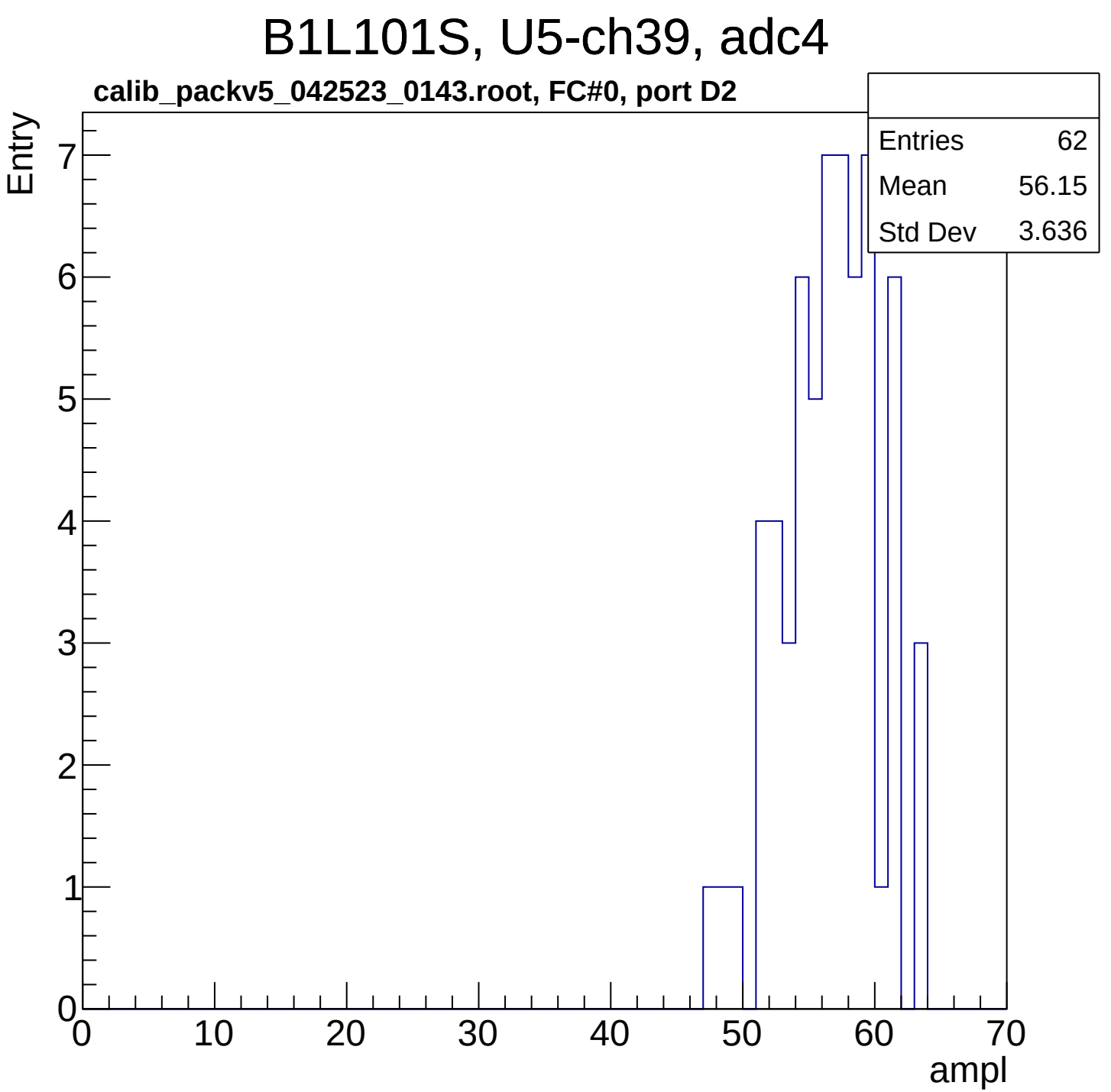
B1L101S, U5-ch39, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 56.15
Std Dev 3.636
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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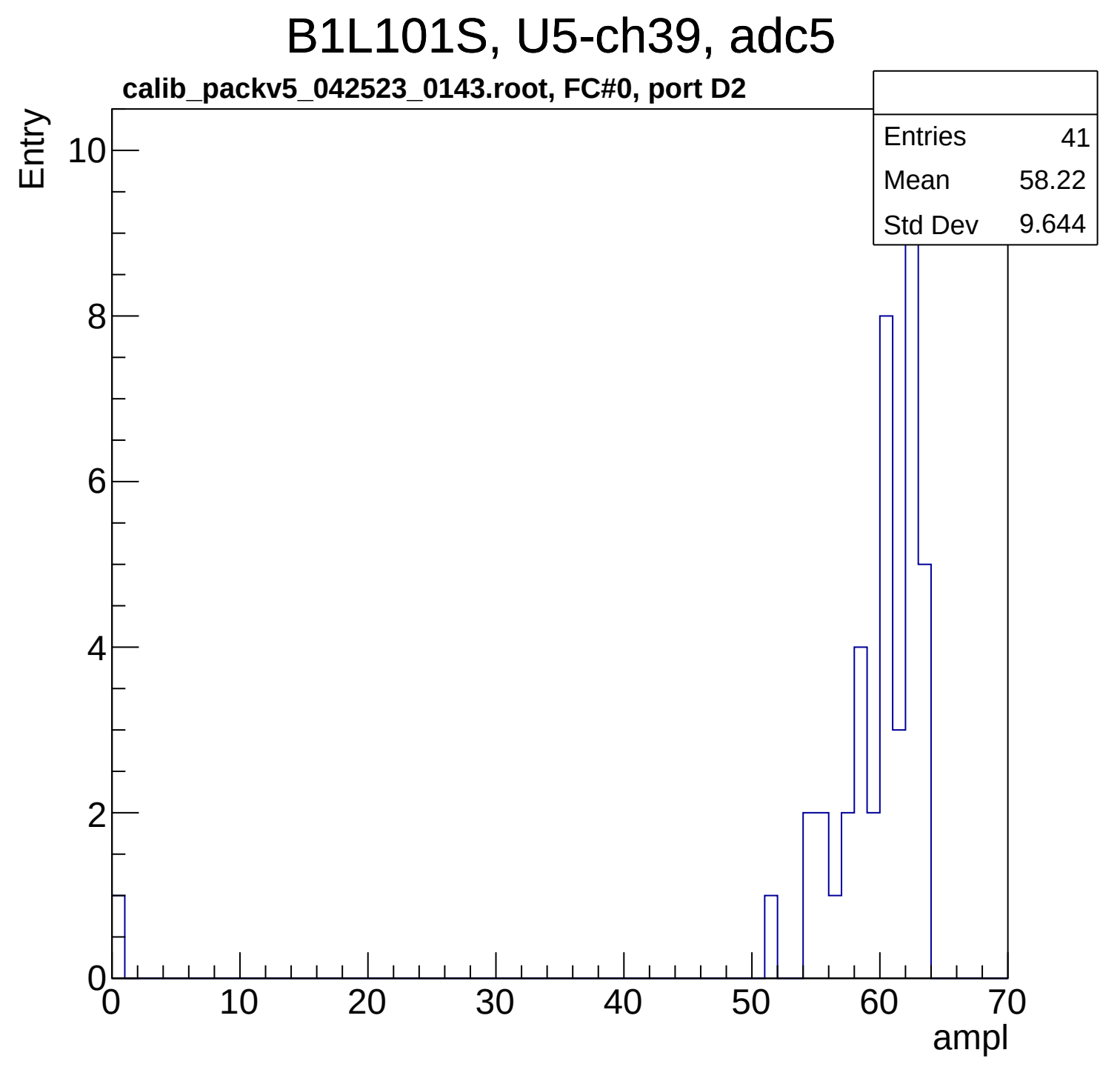
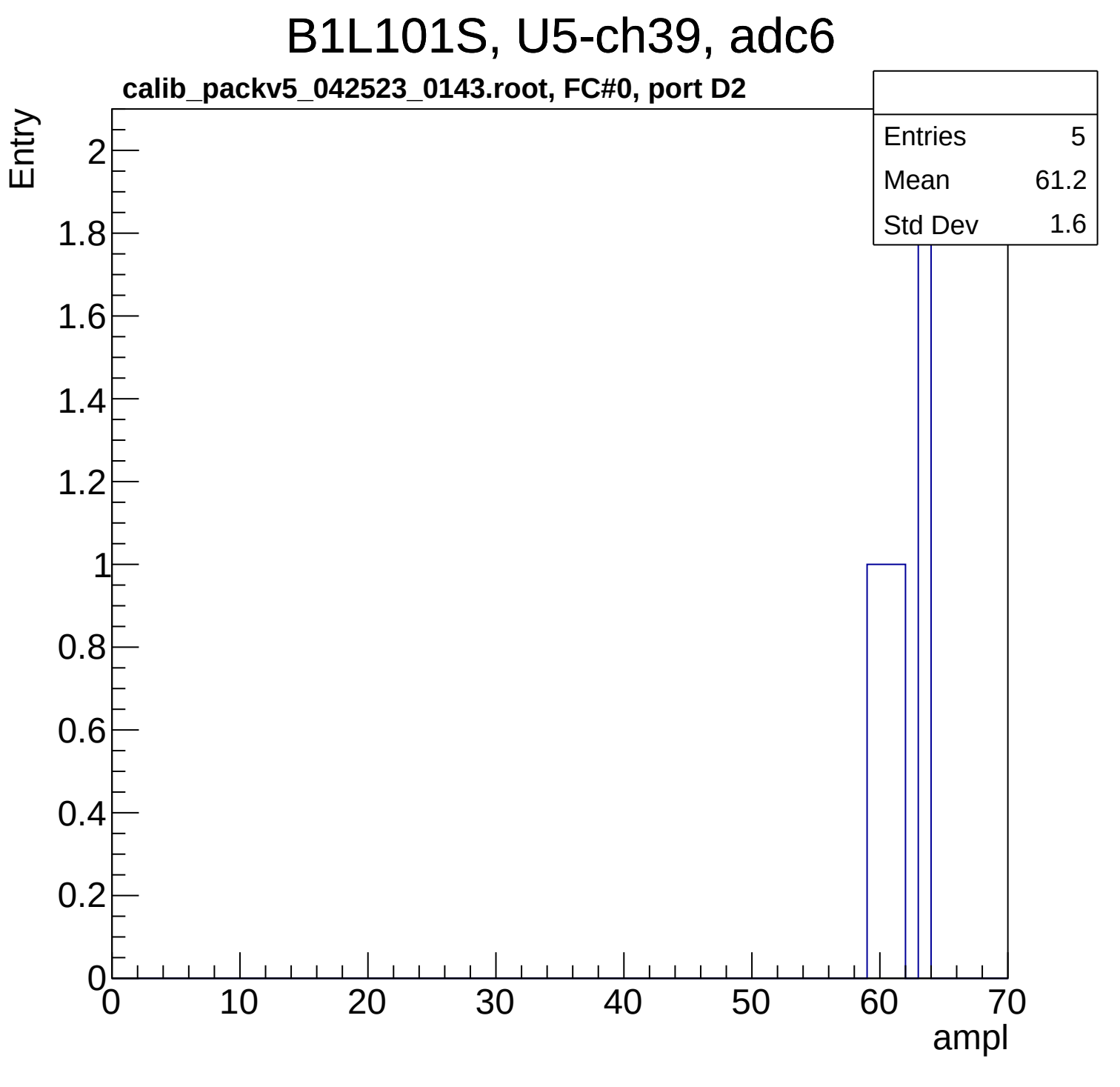
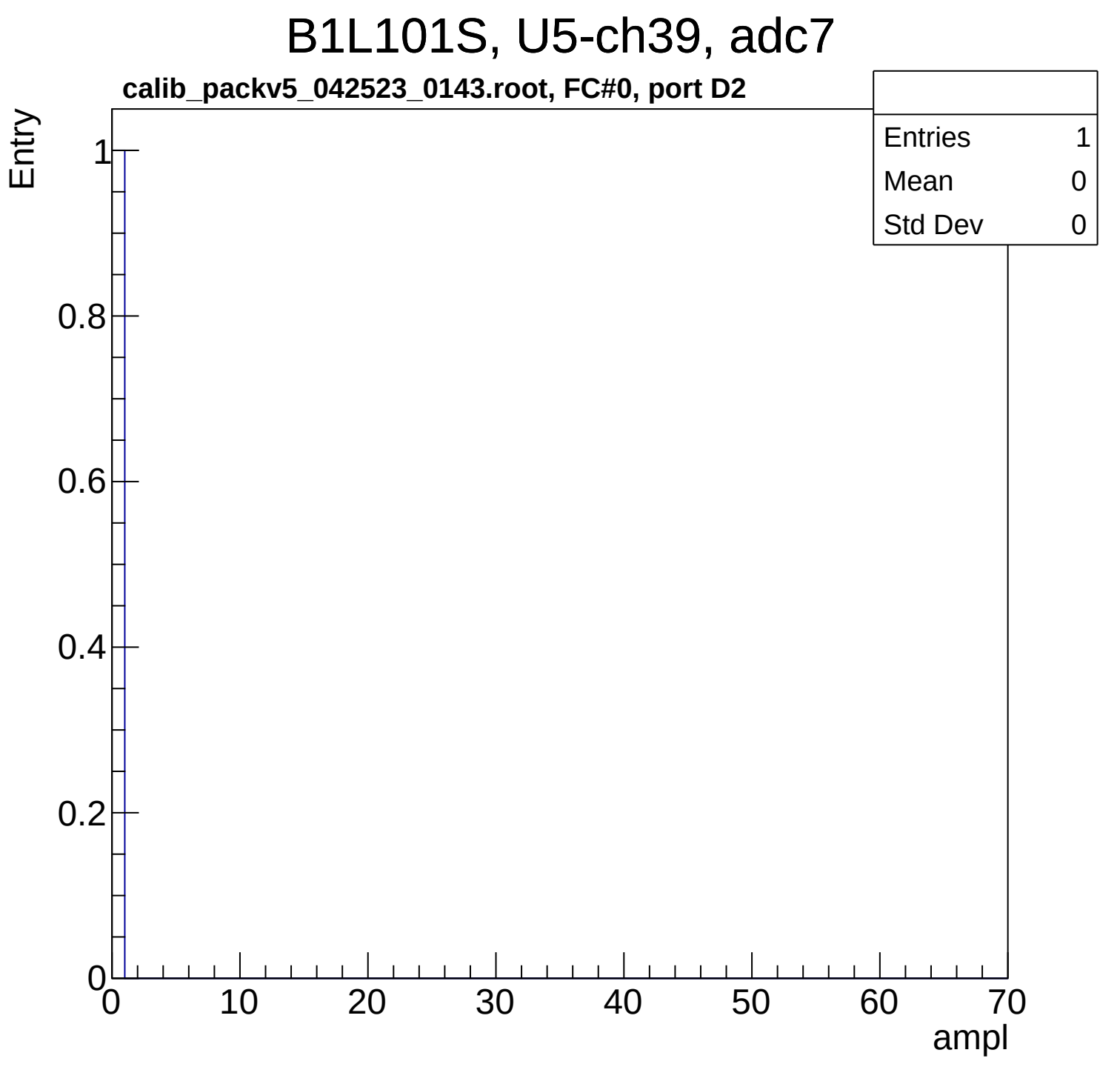
40
50
60
70


B1L101S, U5-ch39, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 41
Mean 58.22
Std Dev 9.644
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch39, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 61.2
Std Dev 1.6
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U5-ch39, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
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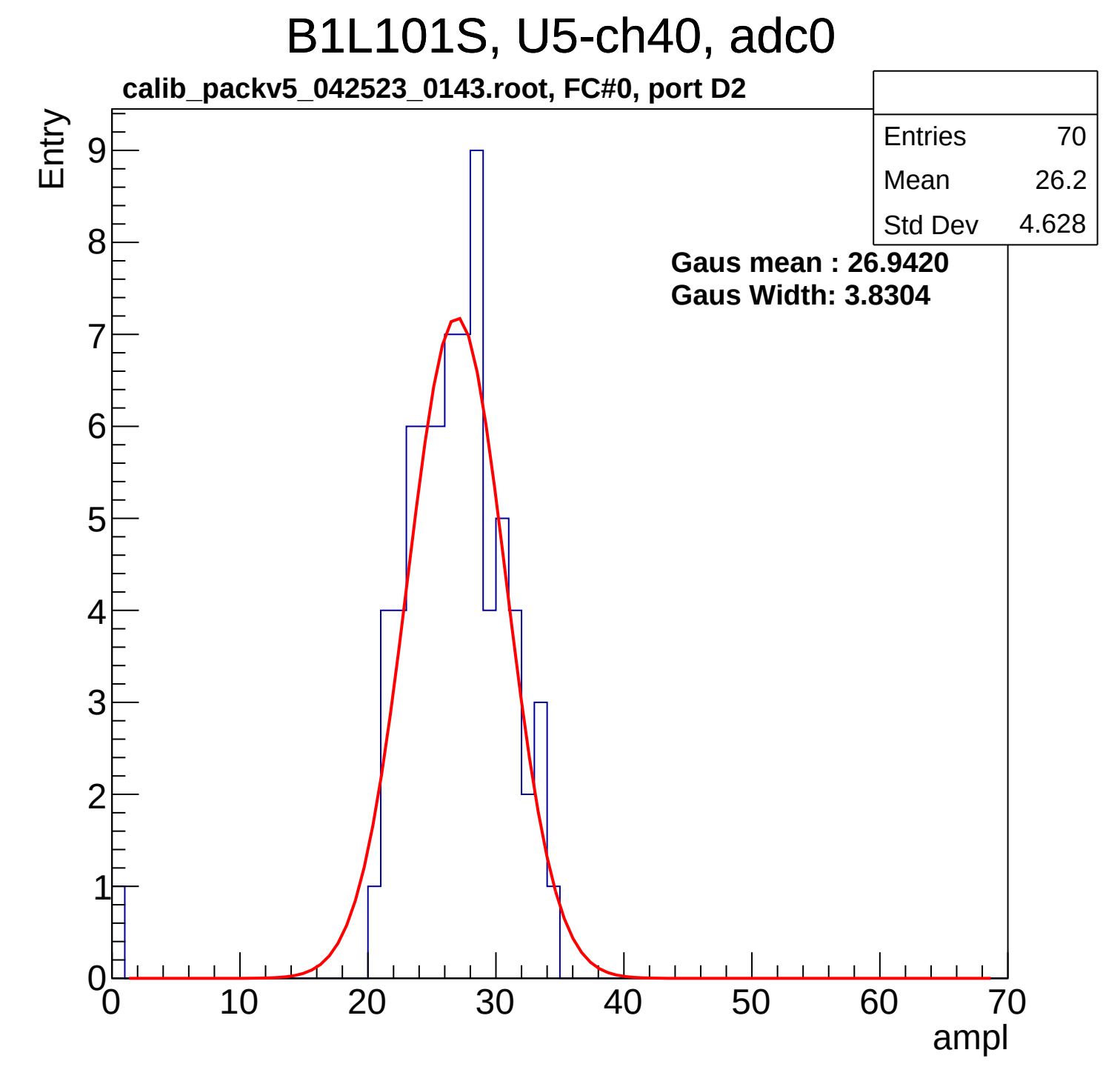
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch40, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 26.2
Std Dev 4.628
Gaus mean : 26.9420
Gaus Width: 3.8304
Entry
ampl
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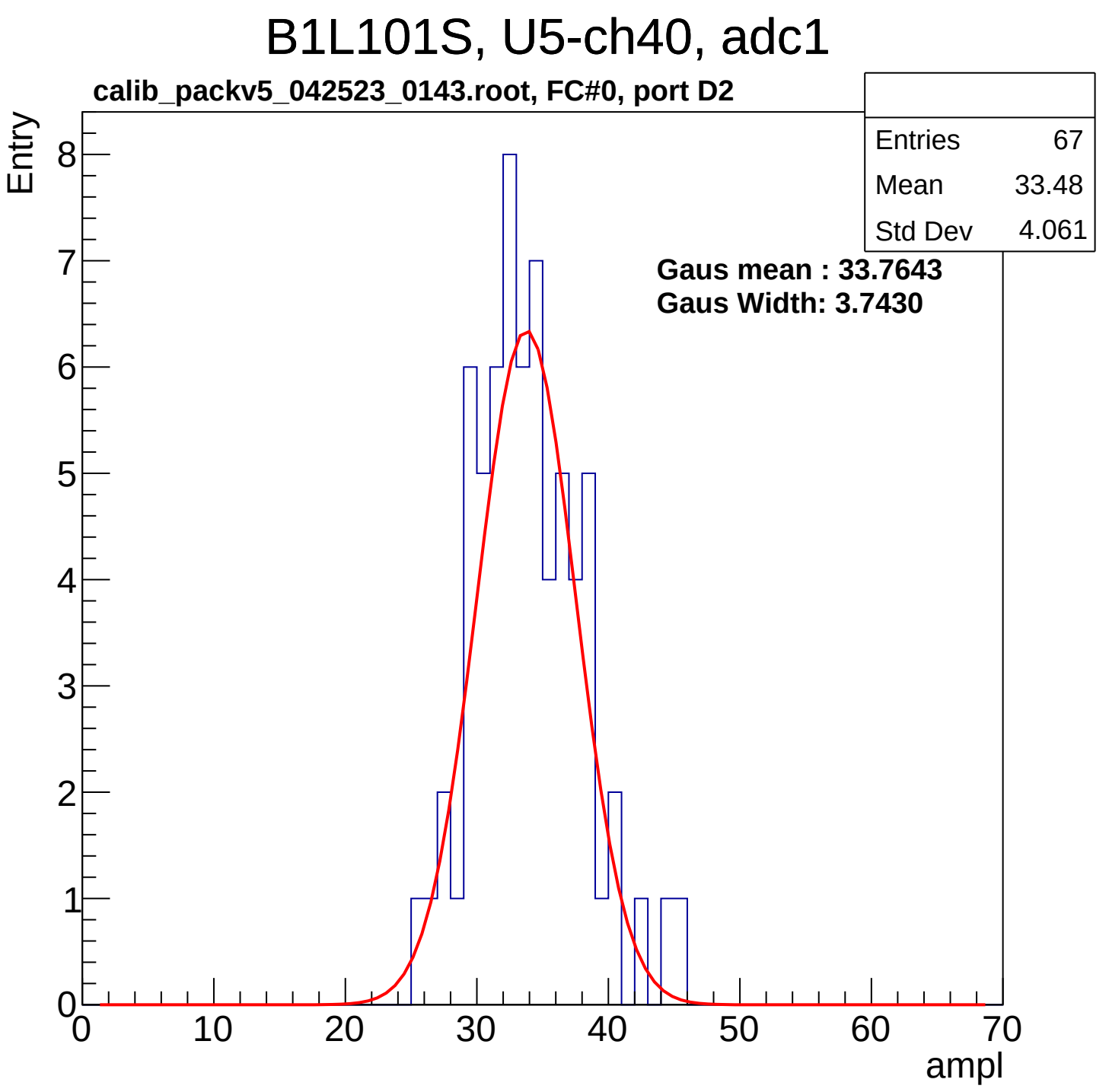
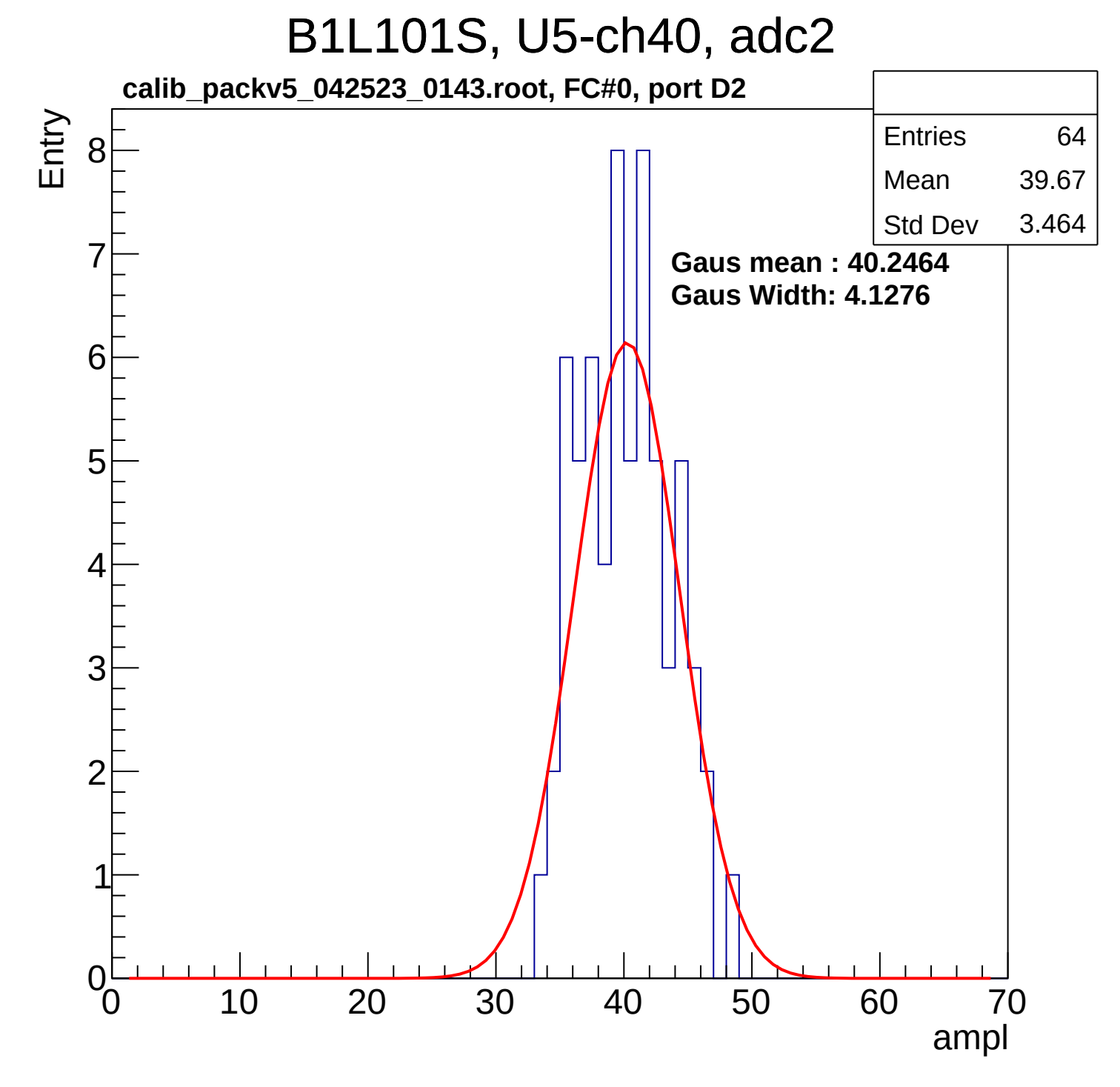
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch40, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 33.48
Std Dev 4.061
Gaus mean : 33.7643
Gaus Width: 3.7430
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch40, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 39.67
Std Dev 3.464
Gaus mean : 40.2464
Gaus Width: 4.1276
Entry
ampl
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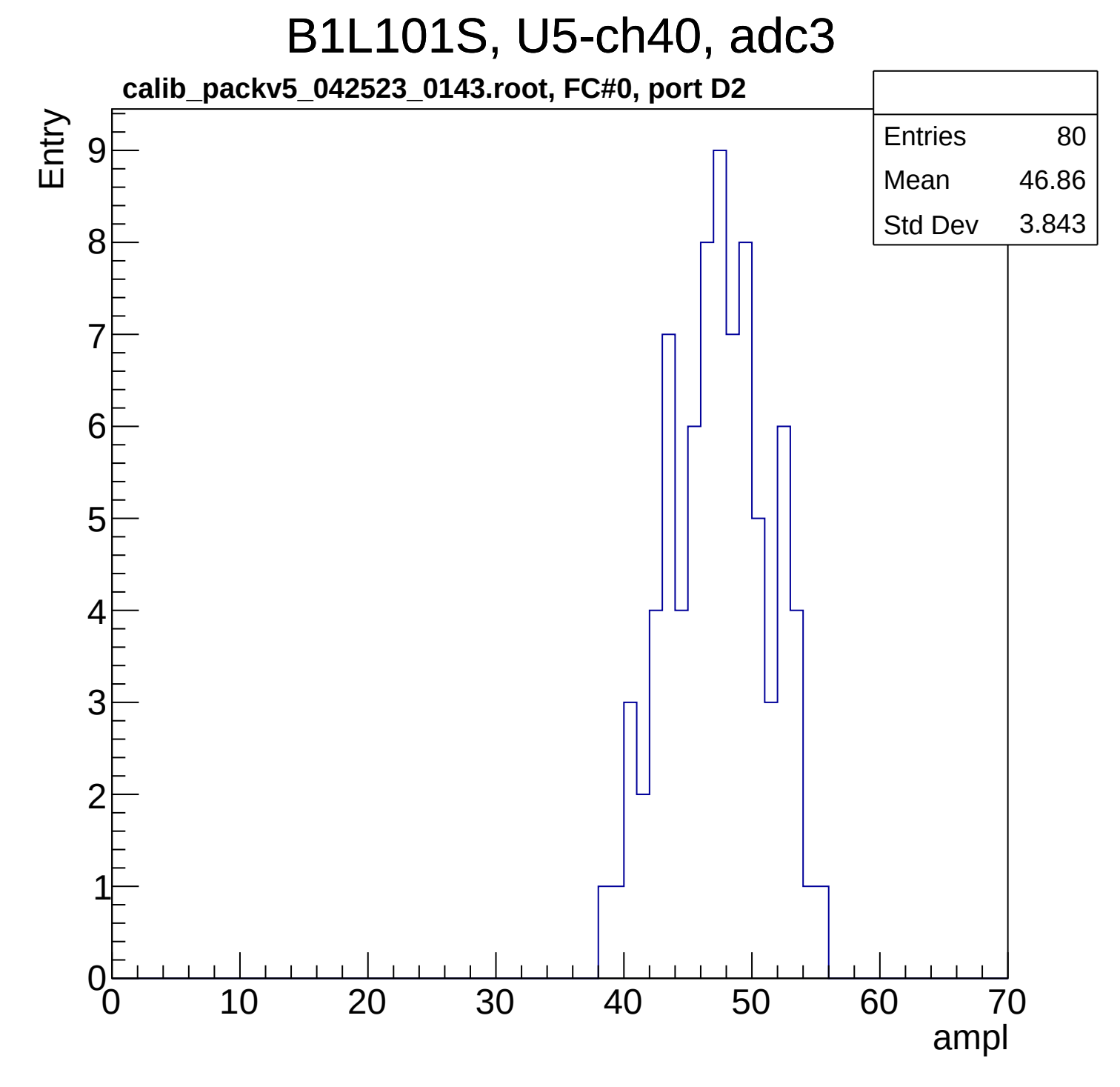
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch40, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 80
Mean 46.86
Std Dev 3.843
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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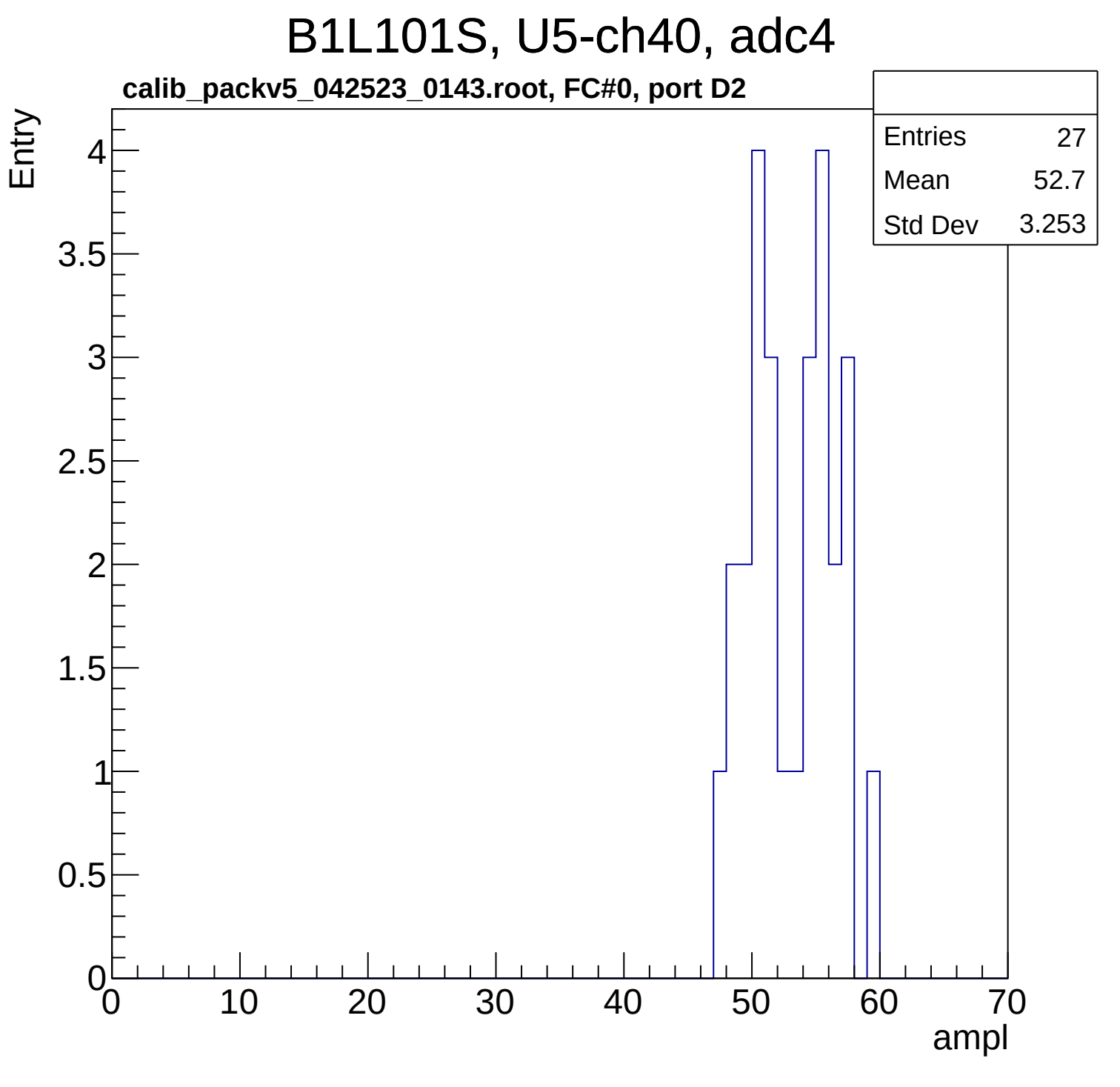
B1L101S, U5-ch40, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 27
Mean 52.7
Std Dev 3.253
Entry
ampl
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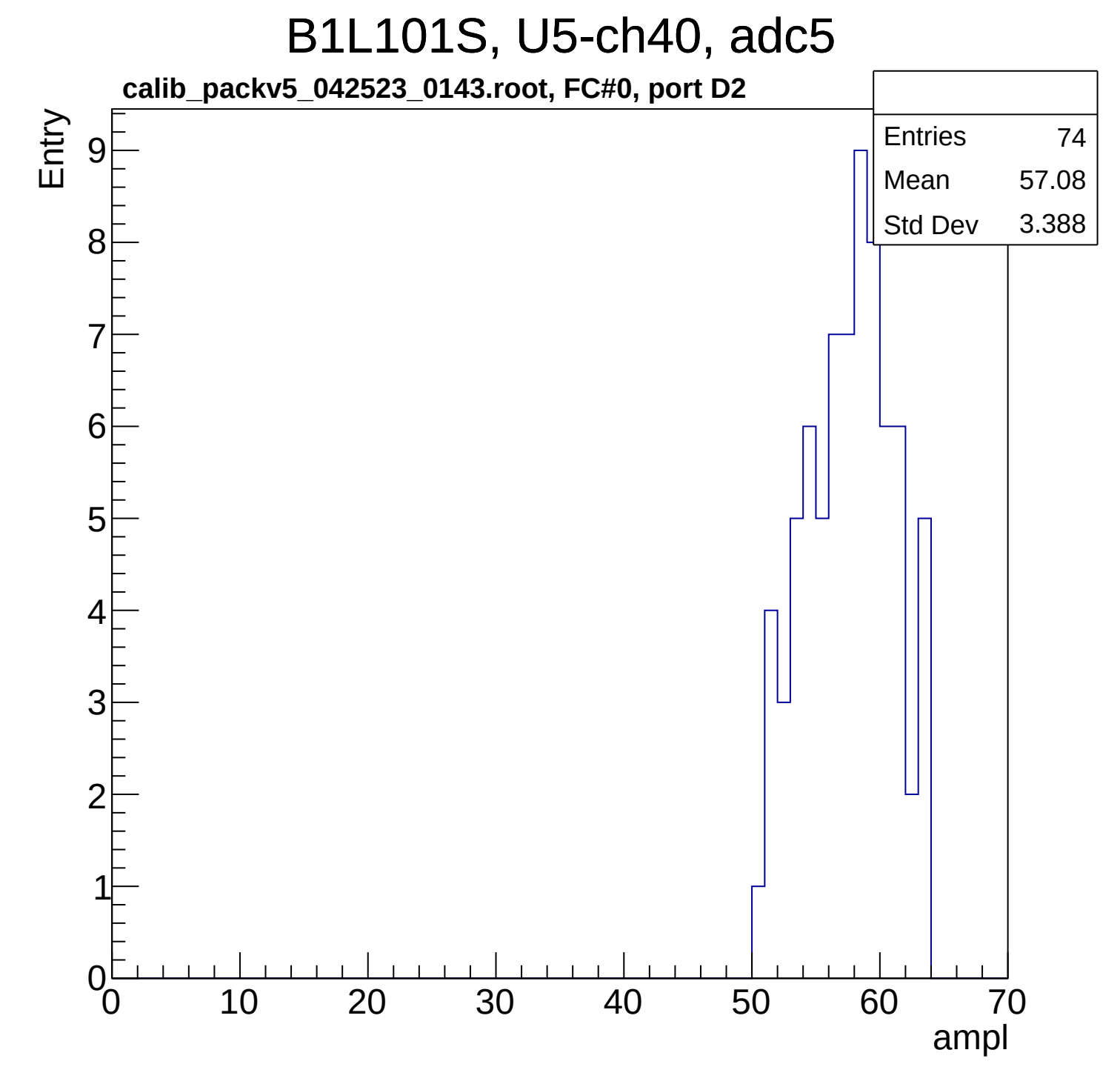
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L101S, U5-ch40, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 57.08
Std Dev 3.388
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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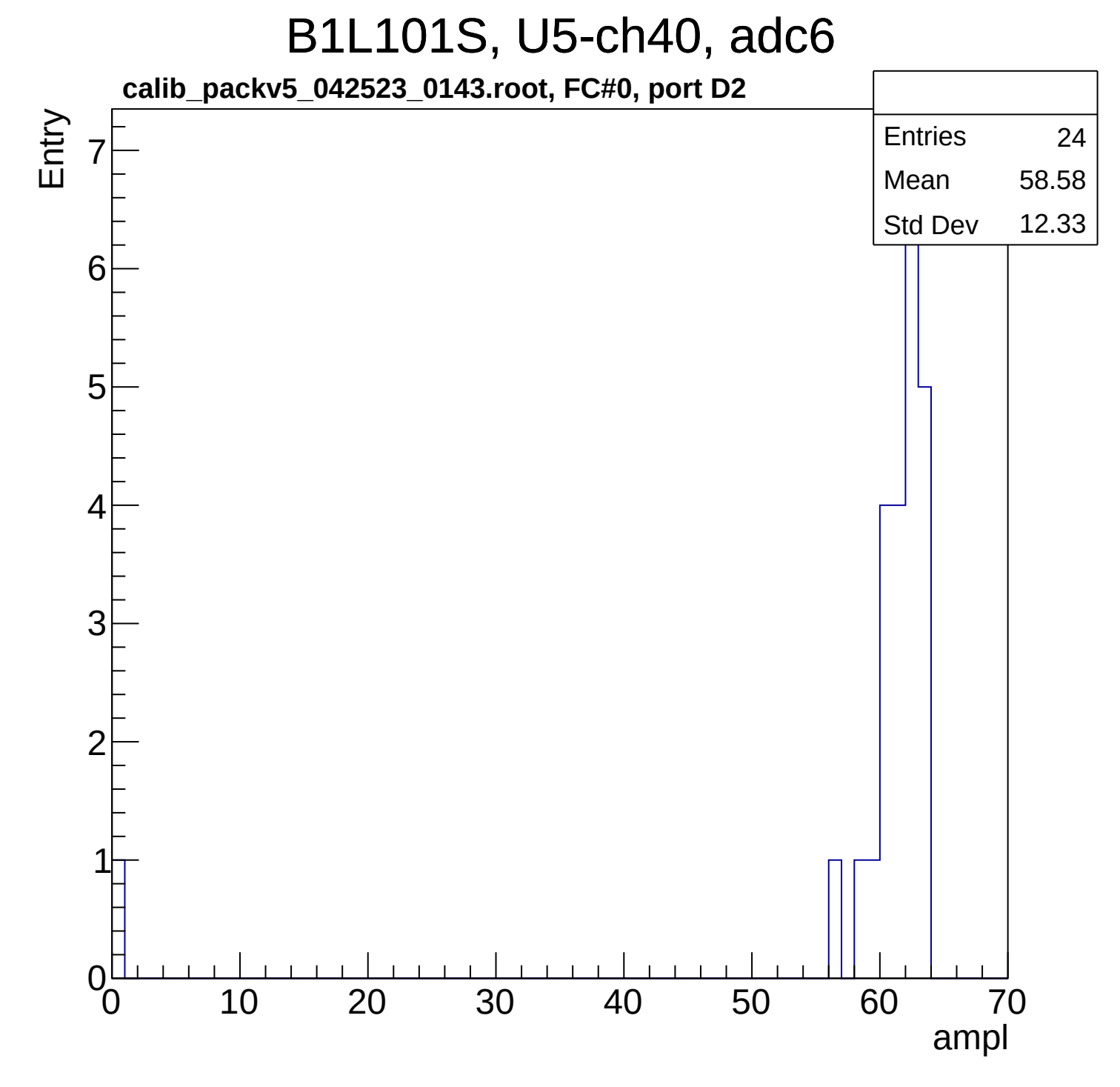
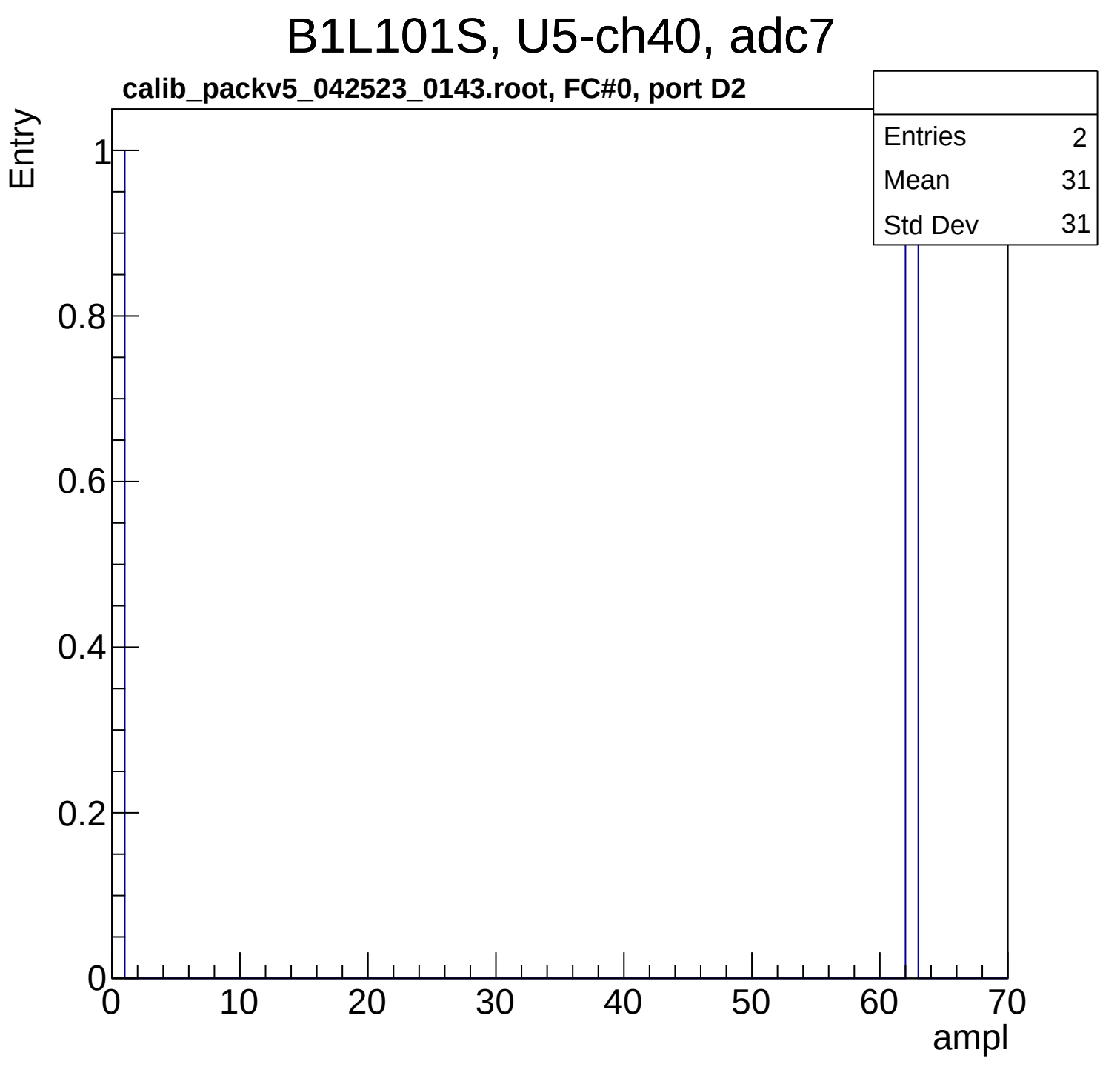
40
50
60
70


B1L101S, U5-ch40, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 24
Mean 58.58
Std Dev 12.33
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch40, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 31
Std Dev 31
Entry
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0.6
0.4
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0
0
10
20
30
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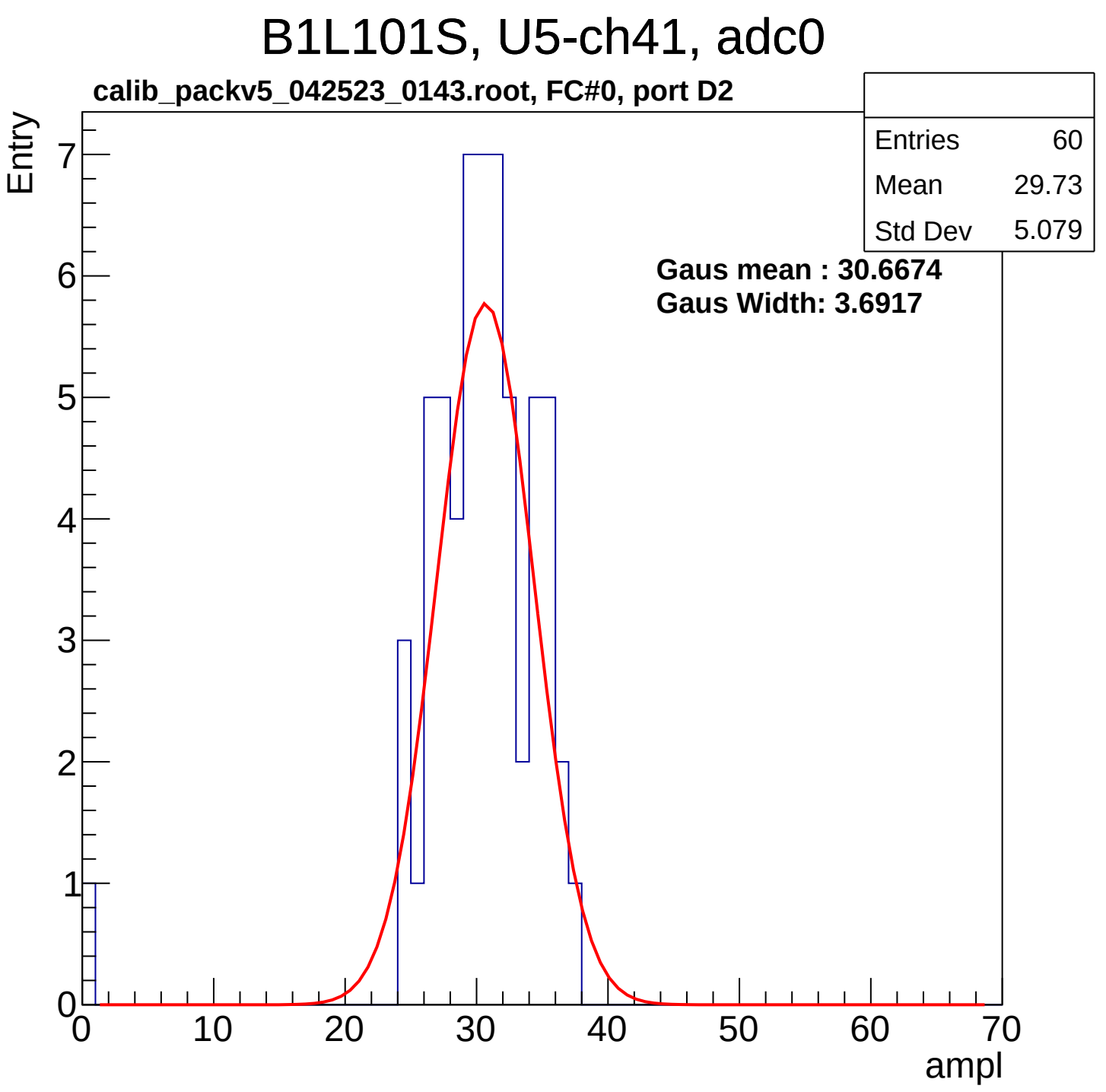
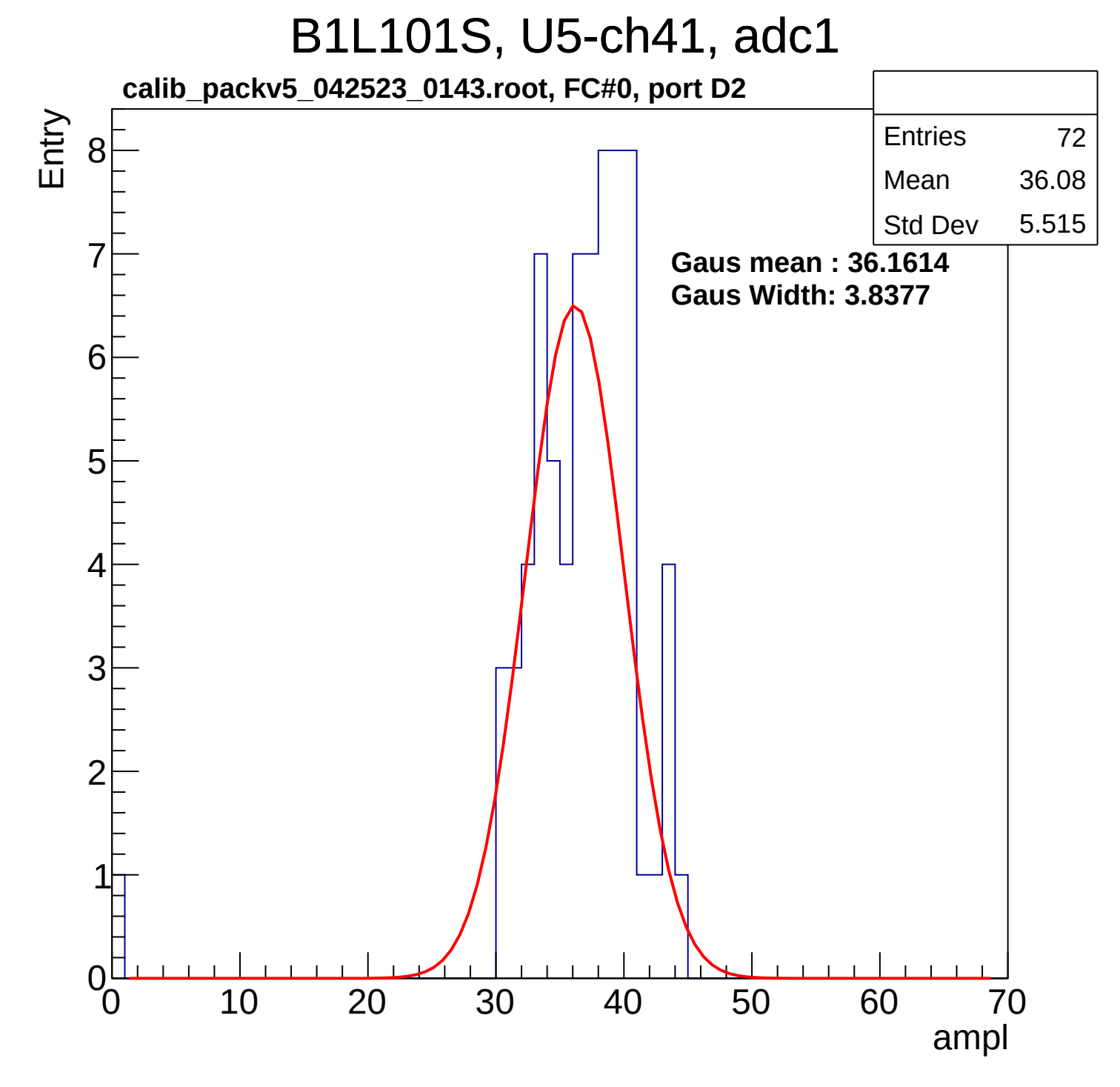
50
60
70
ampl


B1L101S, U5-ch41, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 29.73
Std Dev 5.079
Gaus mean : 30.6674
Gaus Width: 3.6917
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch41, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 36.08
Std Dev 5.515
Gaus mean : 36.1614
Gaus Width: 3.8377
Entry
ampl
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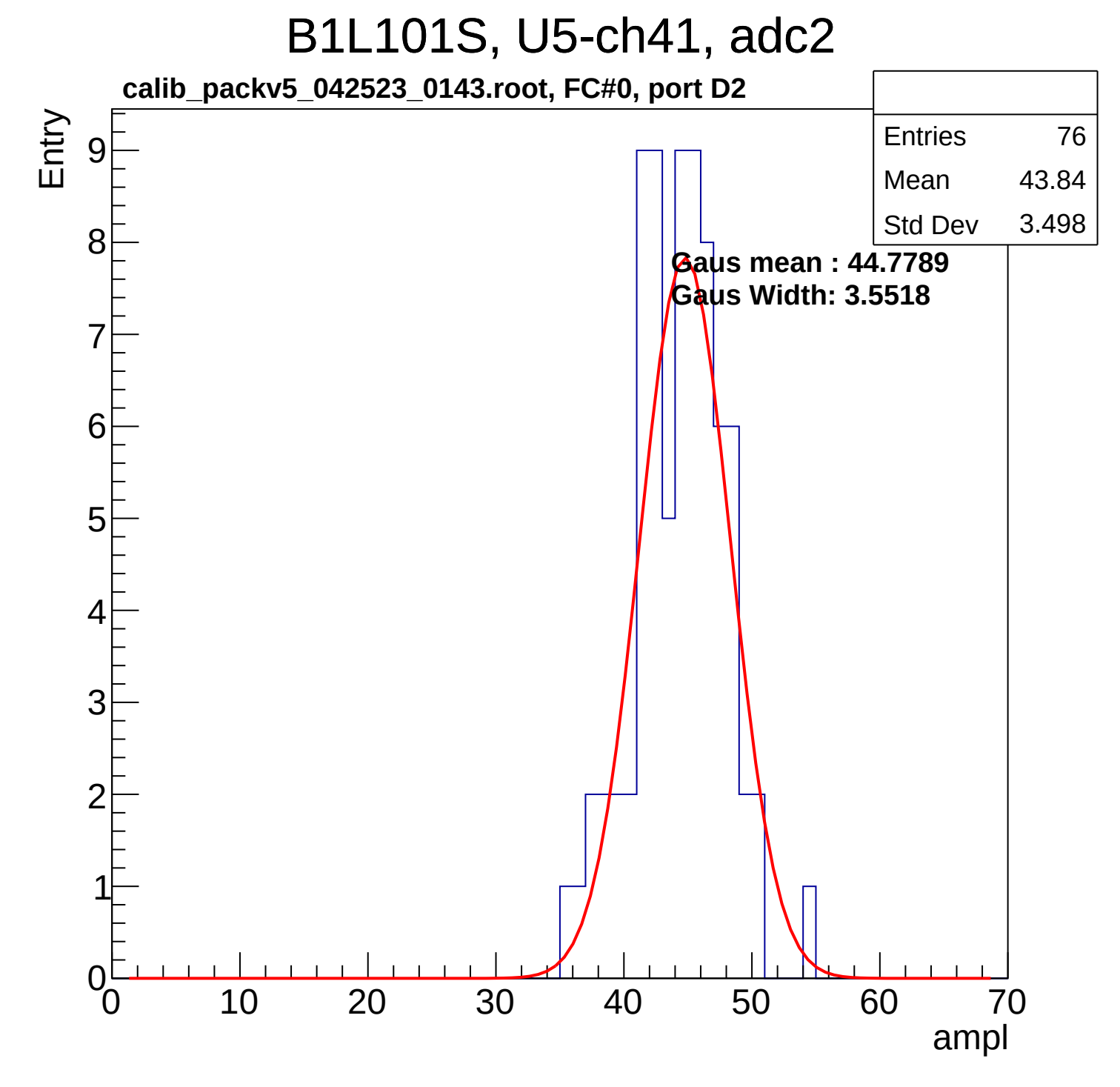
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch41, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 43.84
Std Dev 3.498
Gaus mean : 44.7789
Gaus Width: 3.5518
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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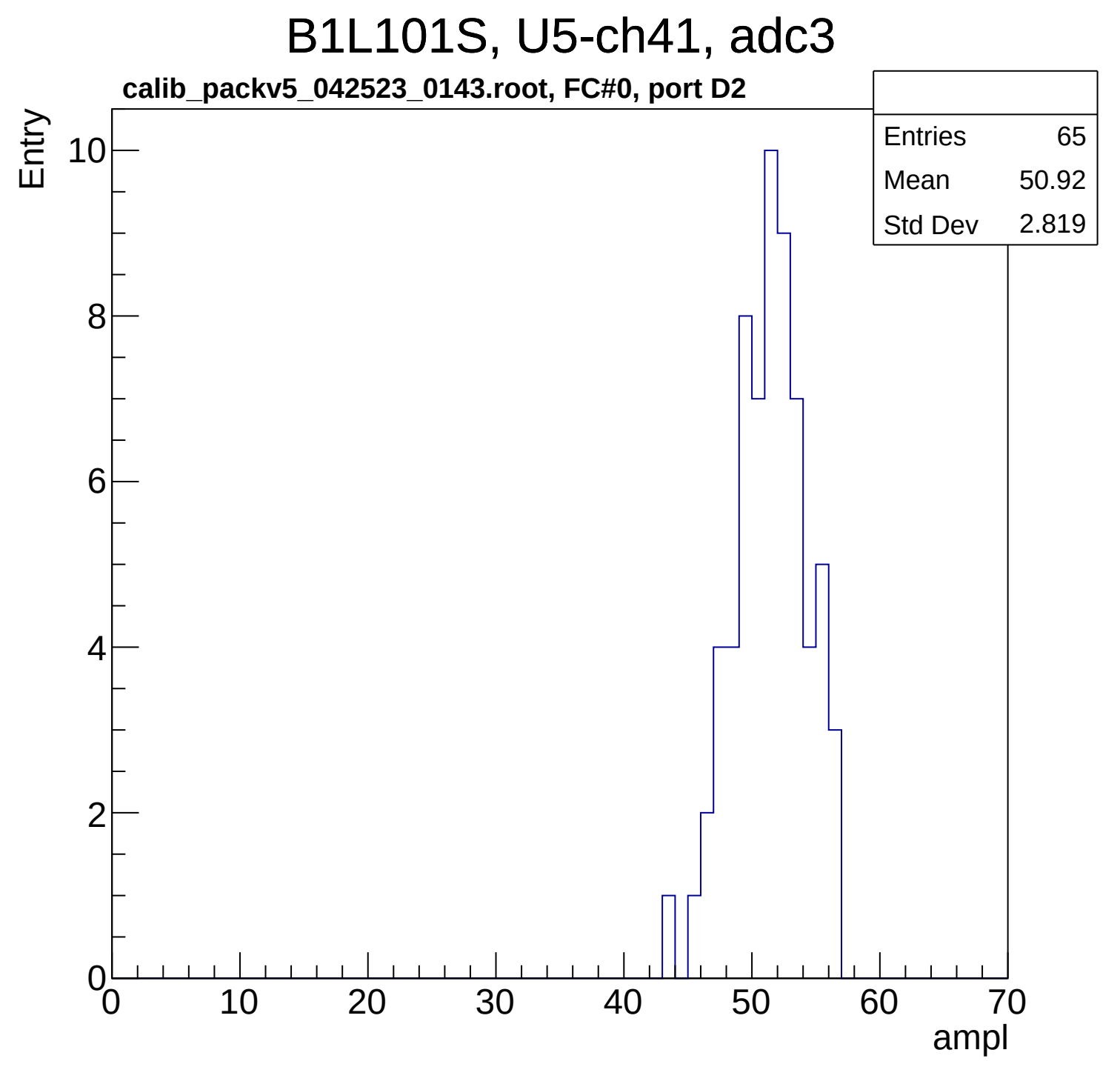
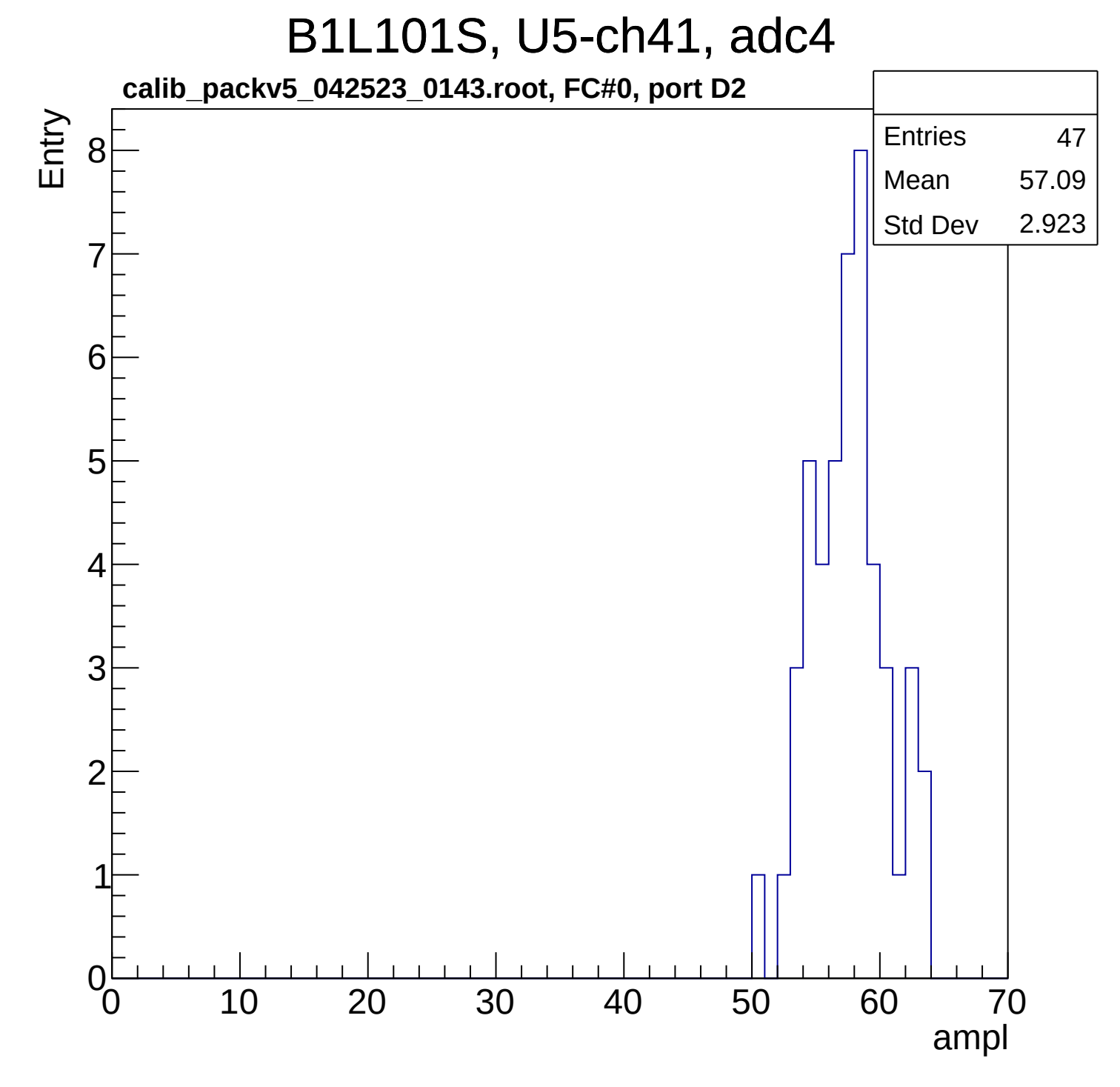

B1L101S, U5-ch41, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 50.92
Std Dev 2.819
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch41, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 57.09
Std Dev 2.923
Entry
ampl
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1
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3
4
5
6
7
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0
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20
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60
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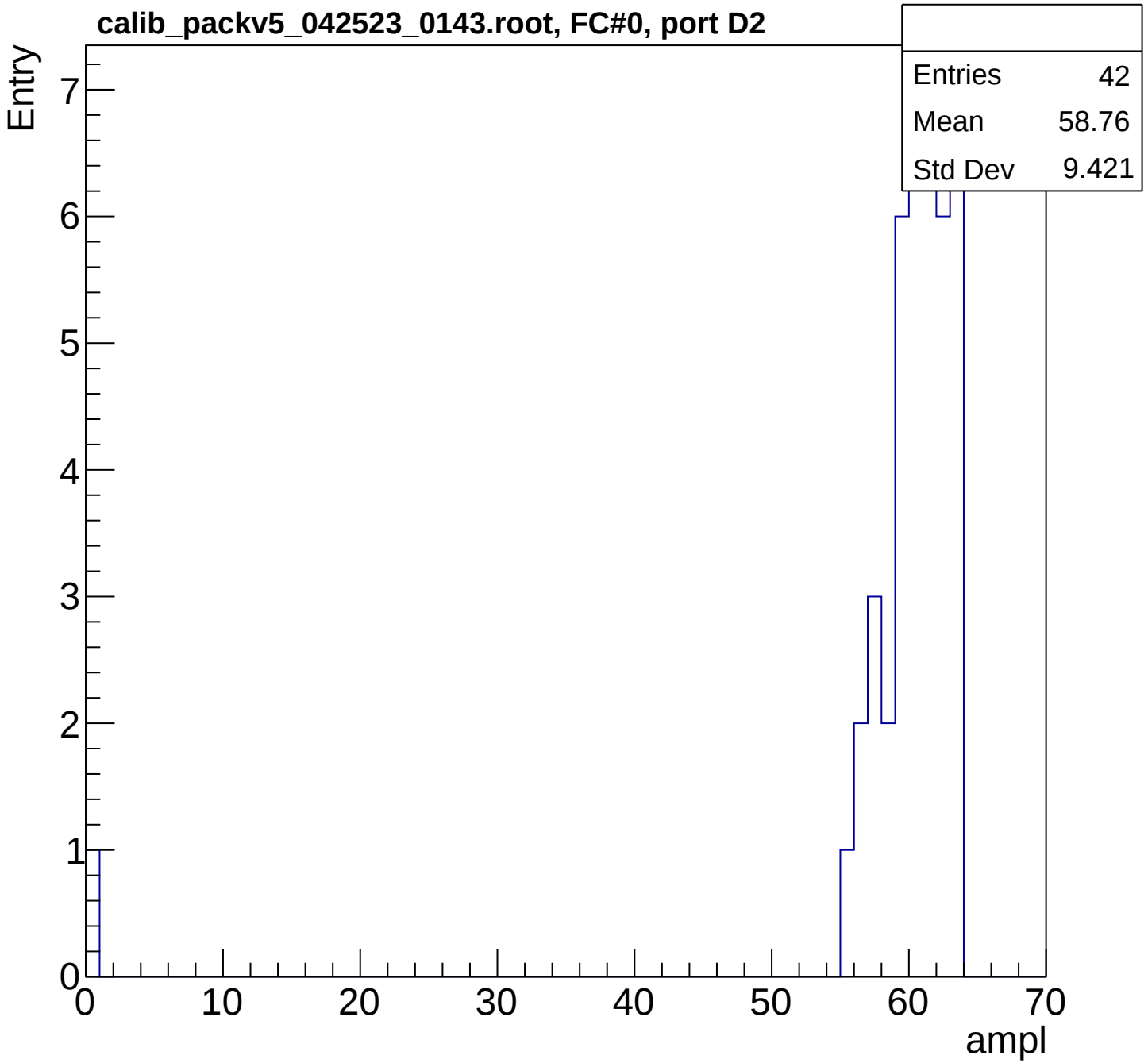
B1L101S, U5-ch41, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 58.76
Std Dev 9.421
Entry
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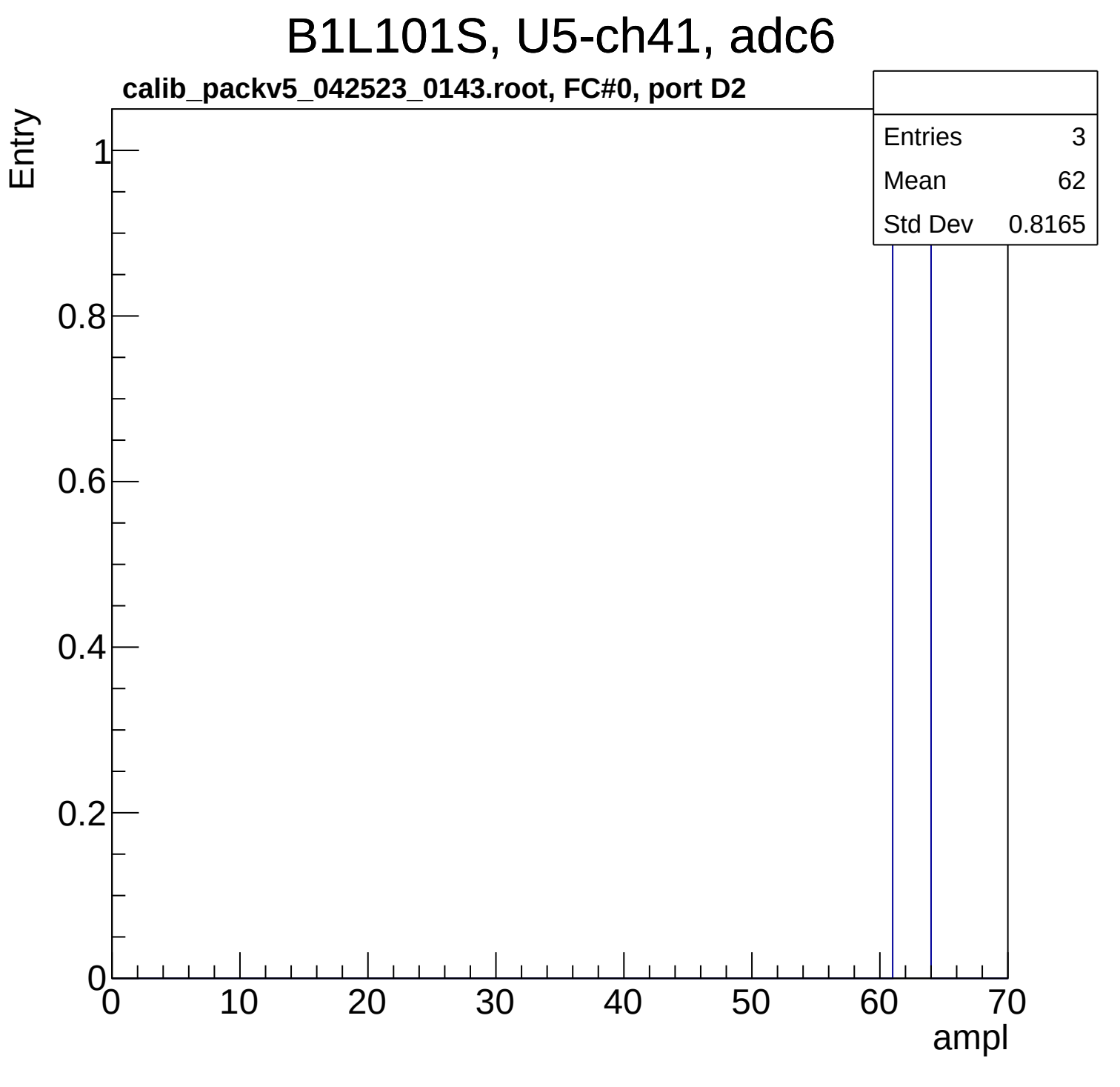
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch41, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 62
Std Dev 0.8165
Entry
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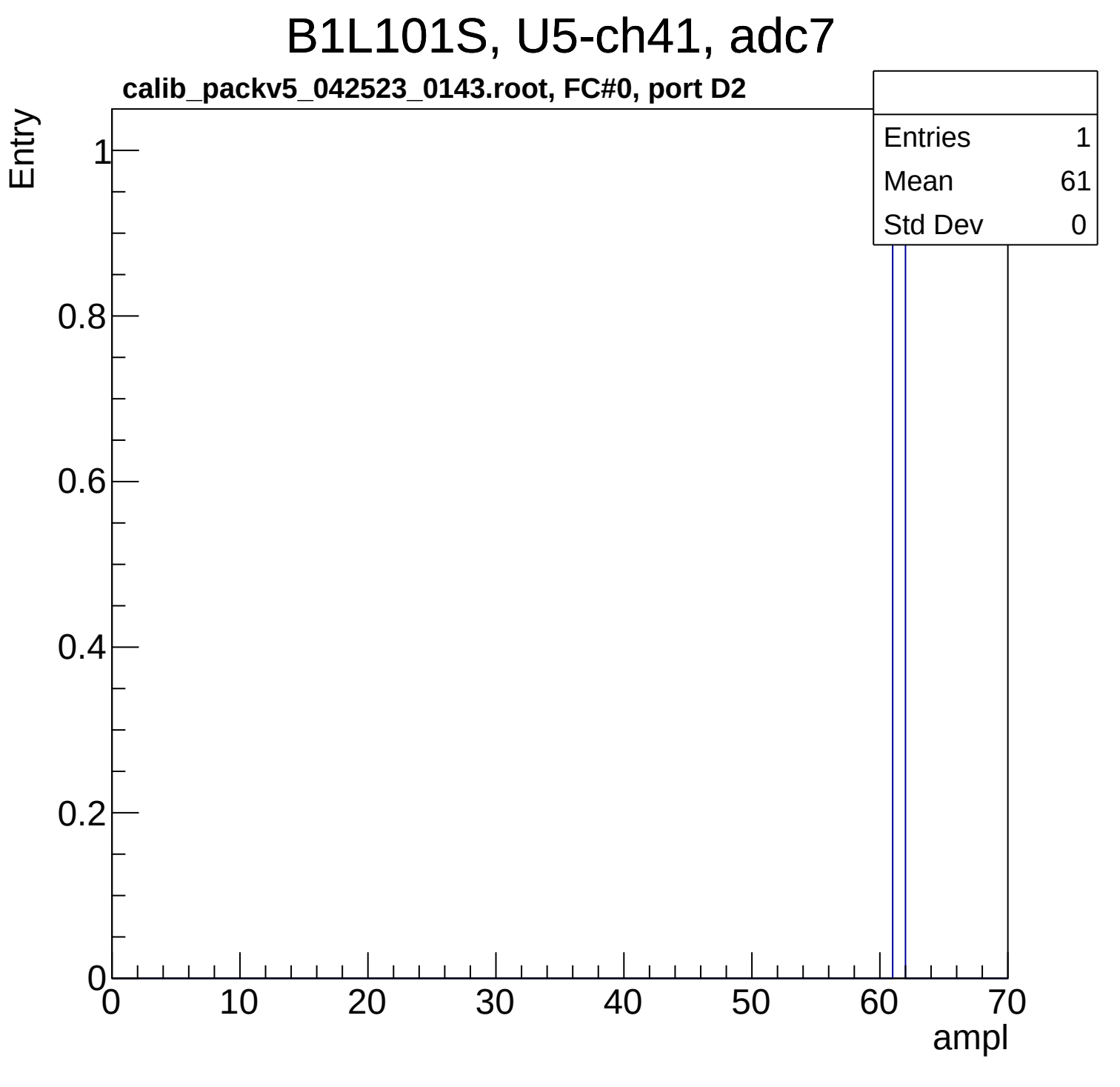
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch41, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 61
Std Dev 0
Entry
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0.6
0.4
0.2
0
0
10
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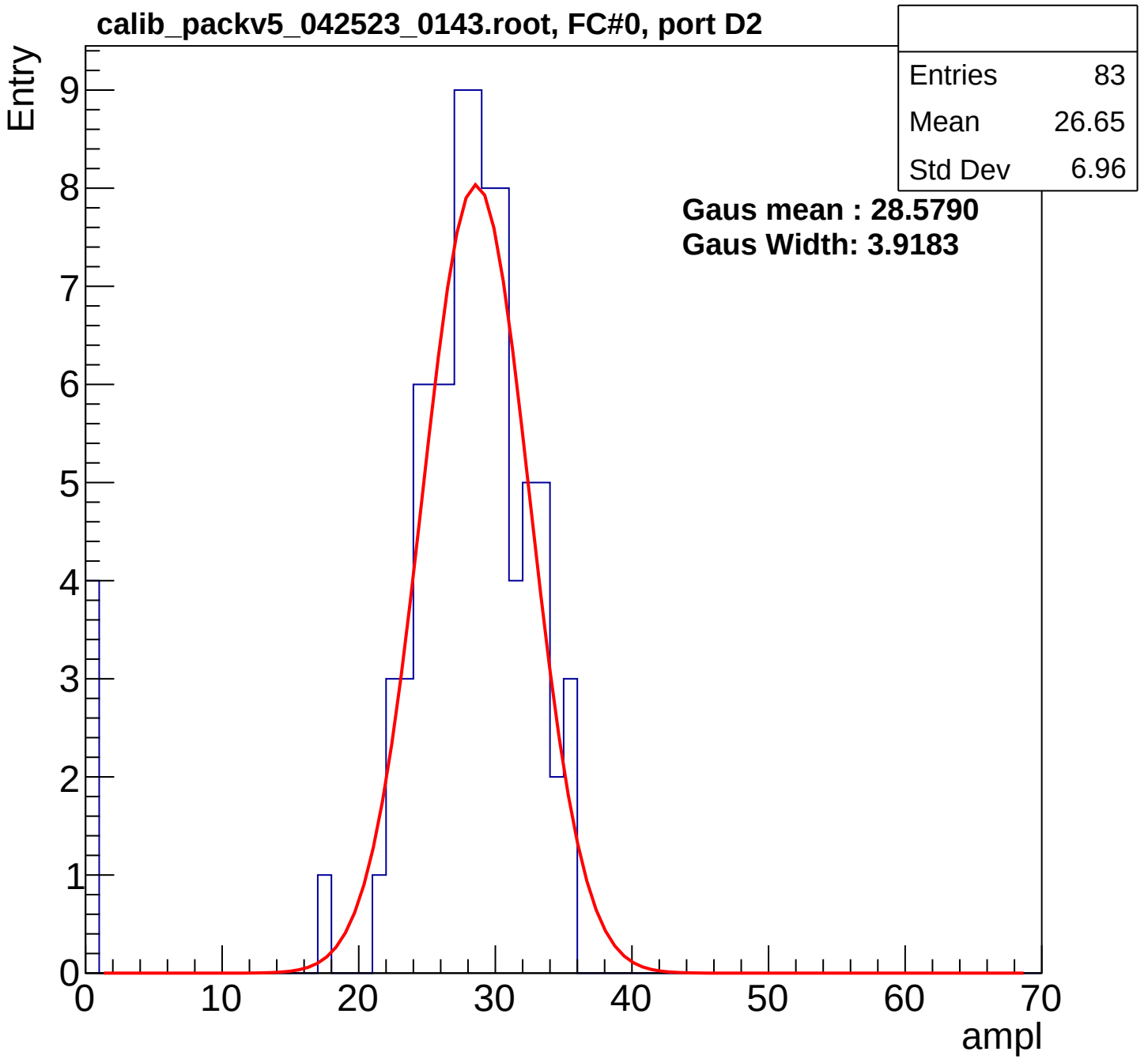
30
40
50
60
70
ampl


B1L101S, U5-ch42, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 83
Mean 26.65
Std Dev 6.96
Gaus mean : 28.5790
Gaus Width: 3.9183
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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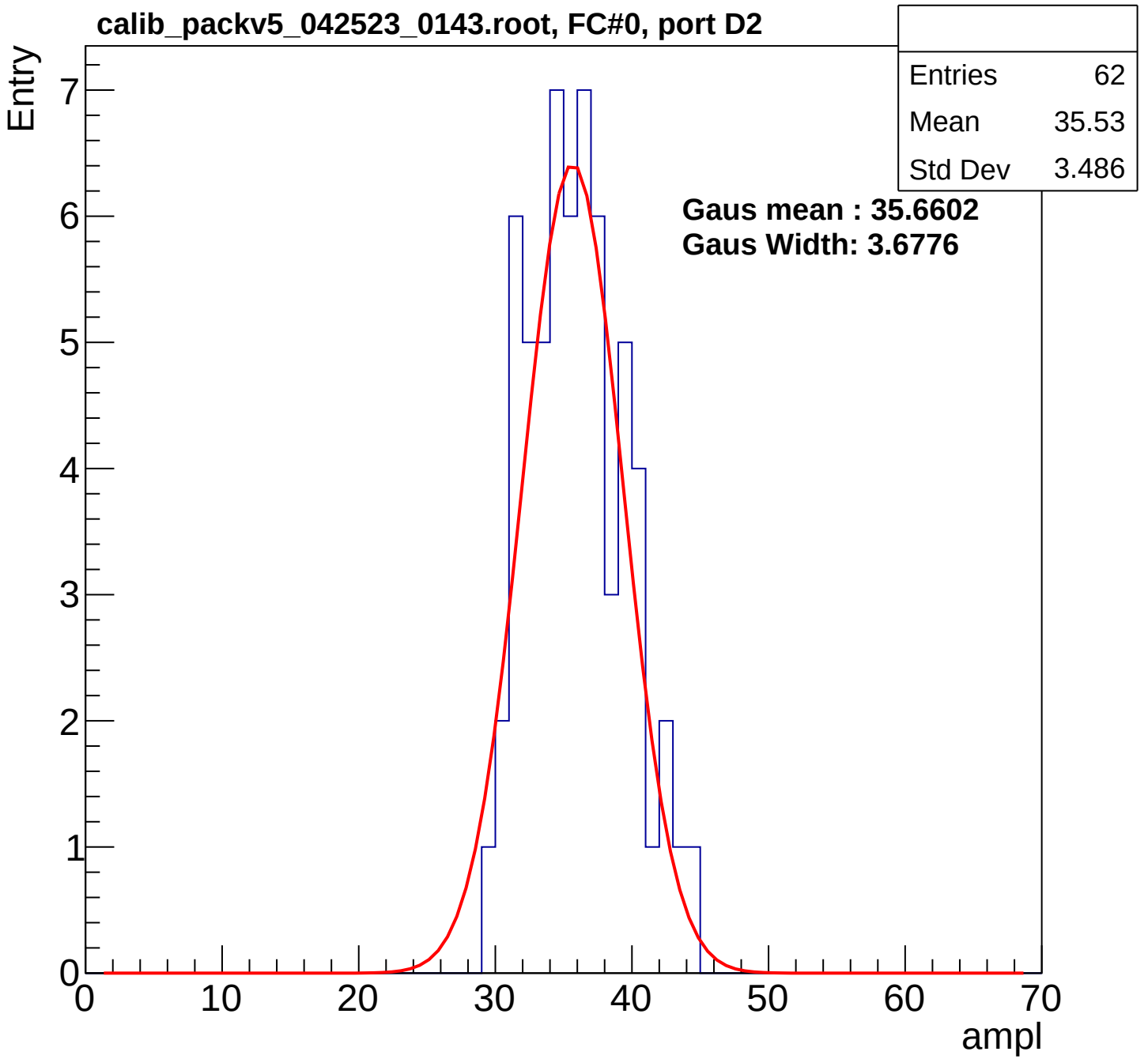
B1L101S, U5-ch42, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 35.53
Std Dev 3.486
Gaus mean : 35.6602
Gaus Width: 3.6776
Entry
ampl
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2
3
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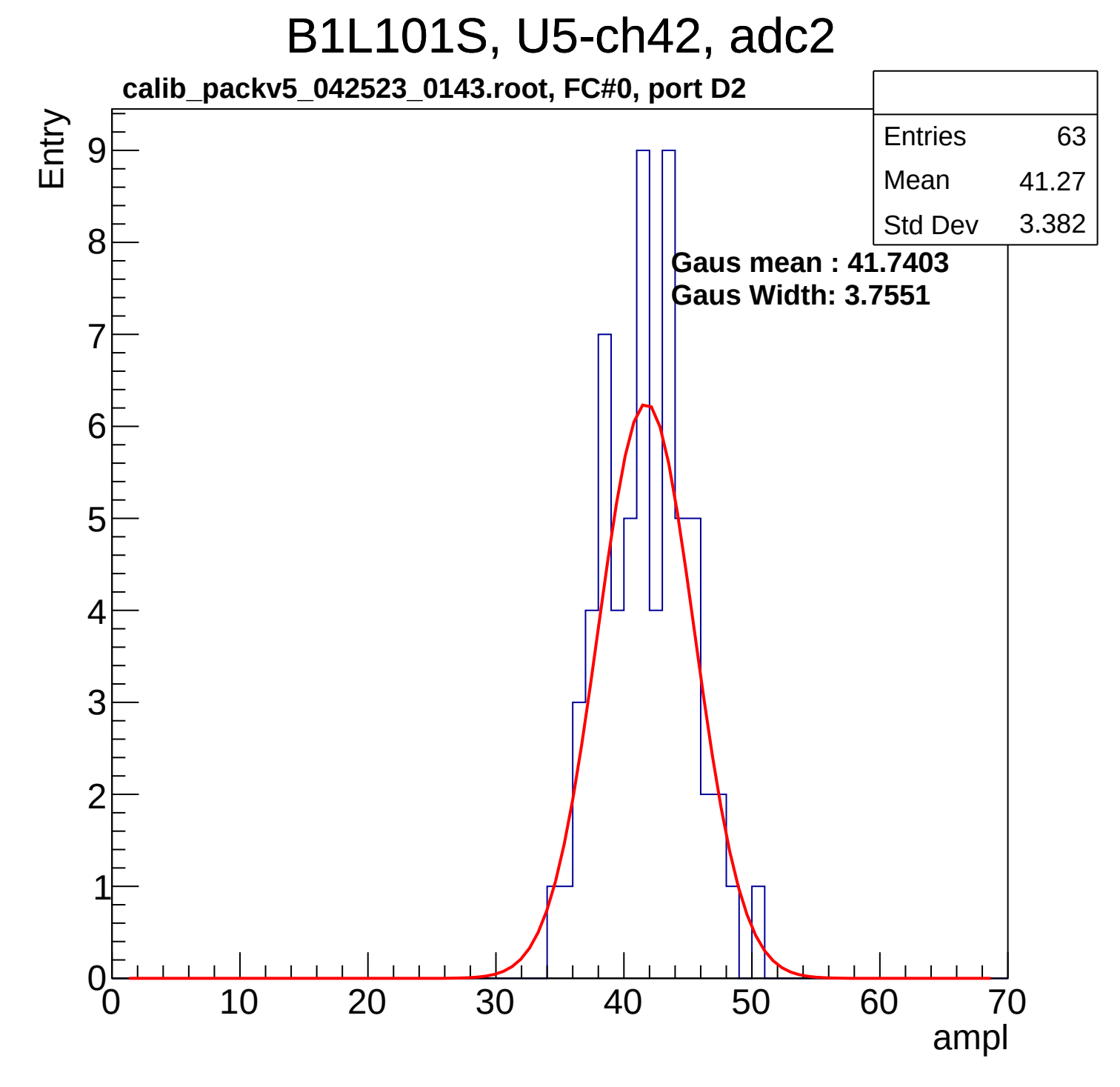
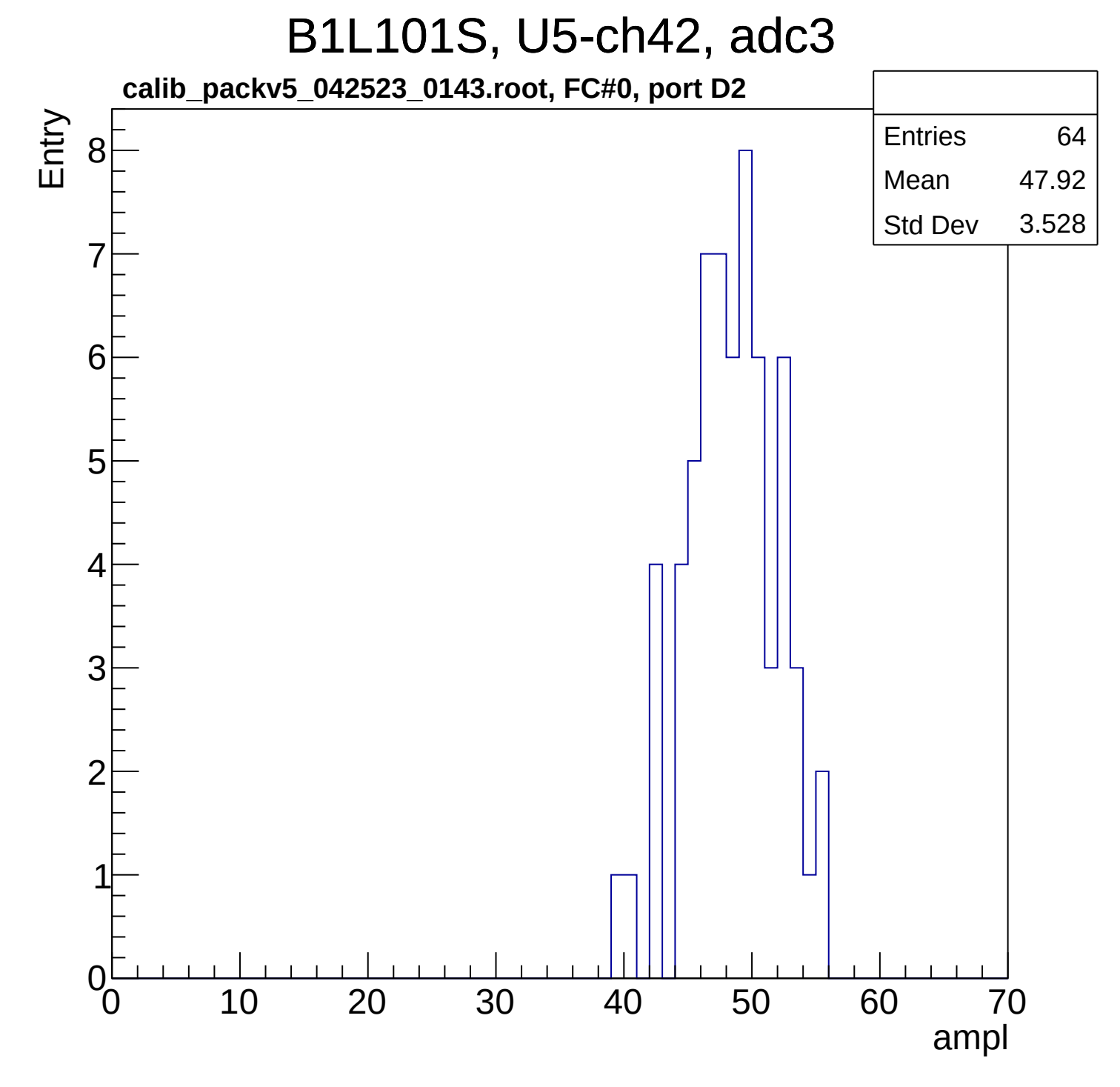

B1L101S, U5-ch42, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 41.27
Std Dev 3.382
Gaus mean : 41.7403
Gaus Width: 3.7551
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch42, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 47.92
Std Dev 3.528
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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60
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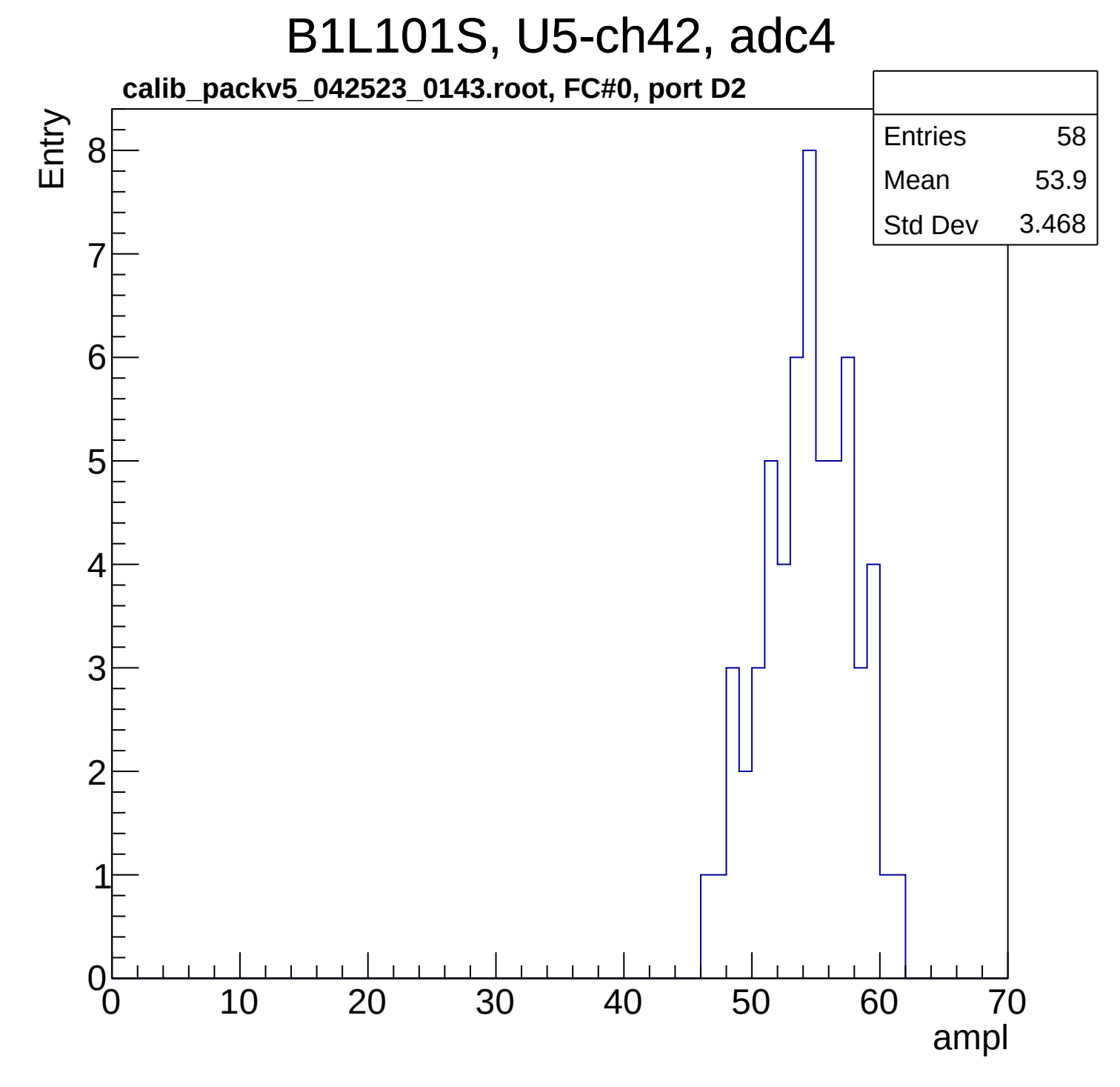
B1L101S, U5-ch42, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 53.9
Std Dev 3.468
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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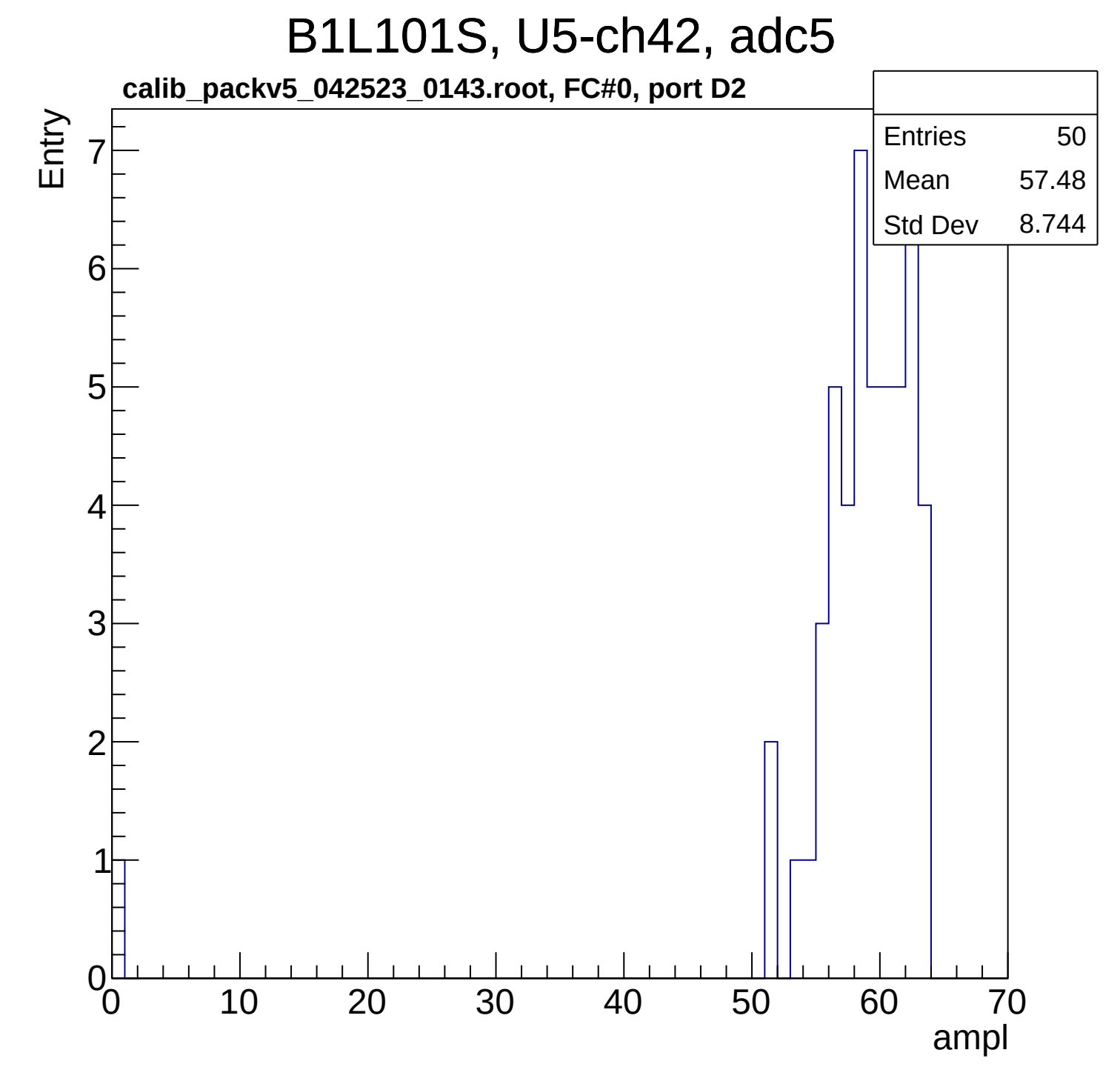
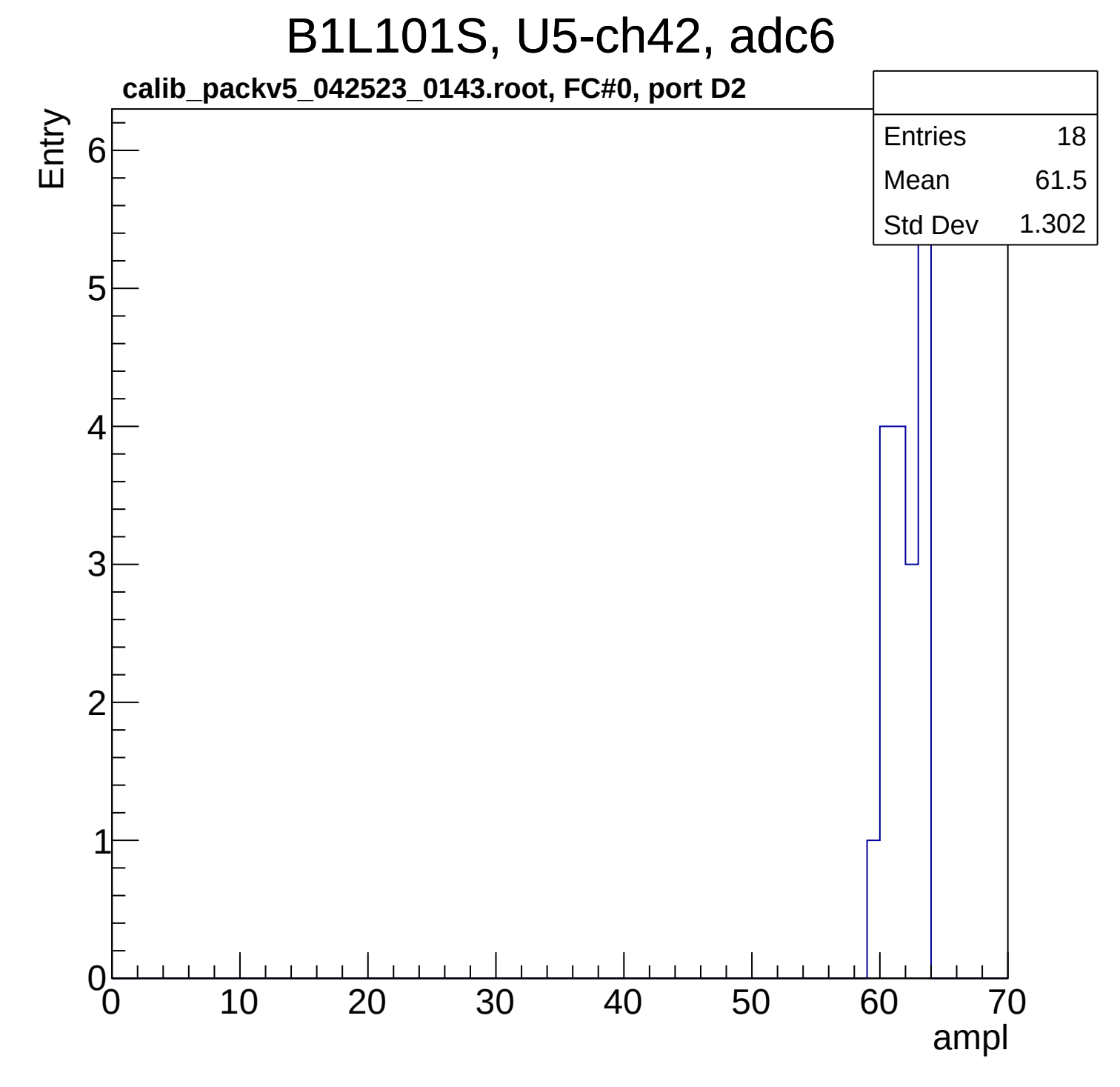
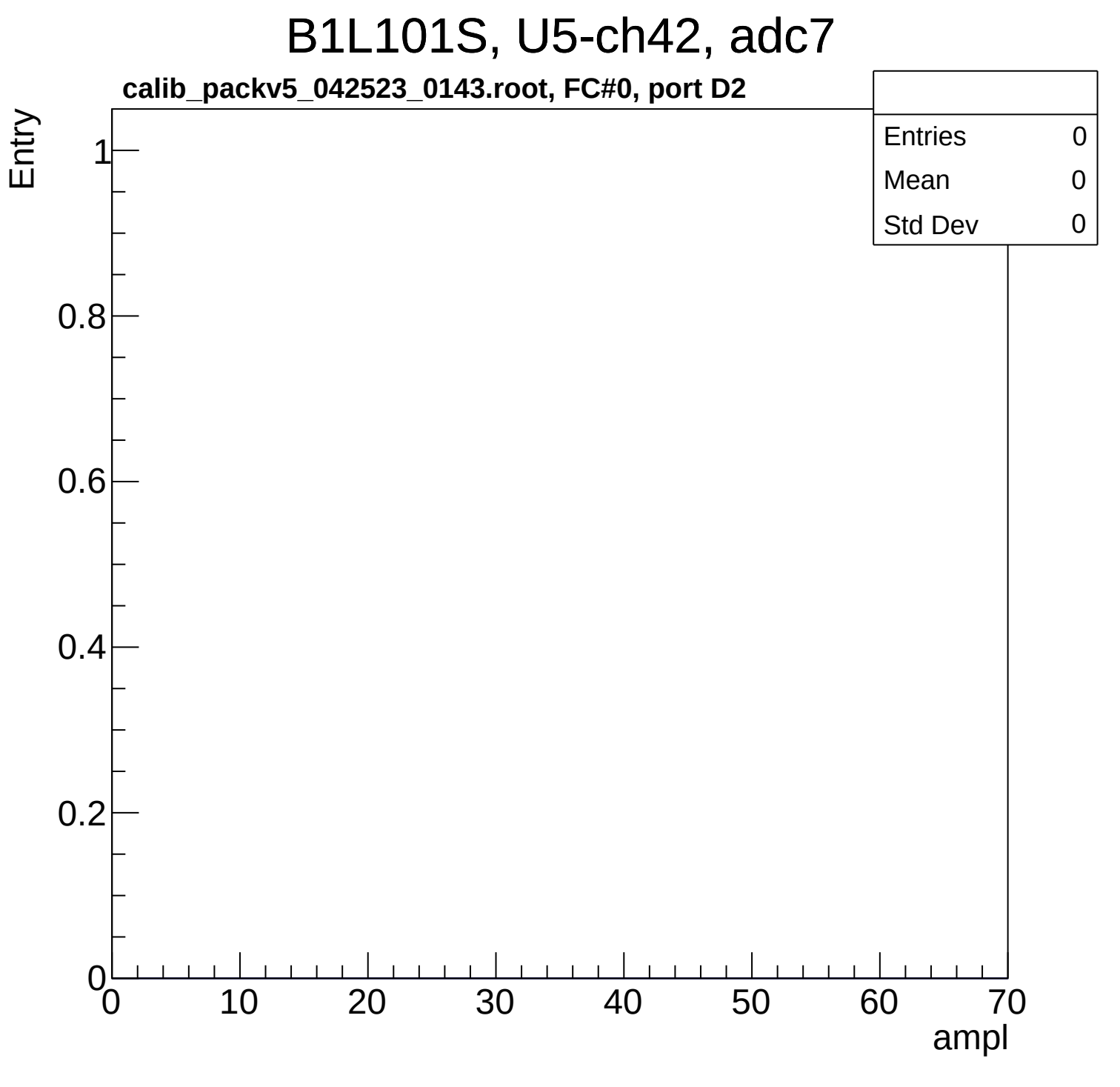
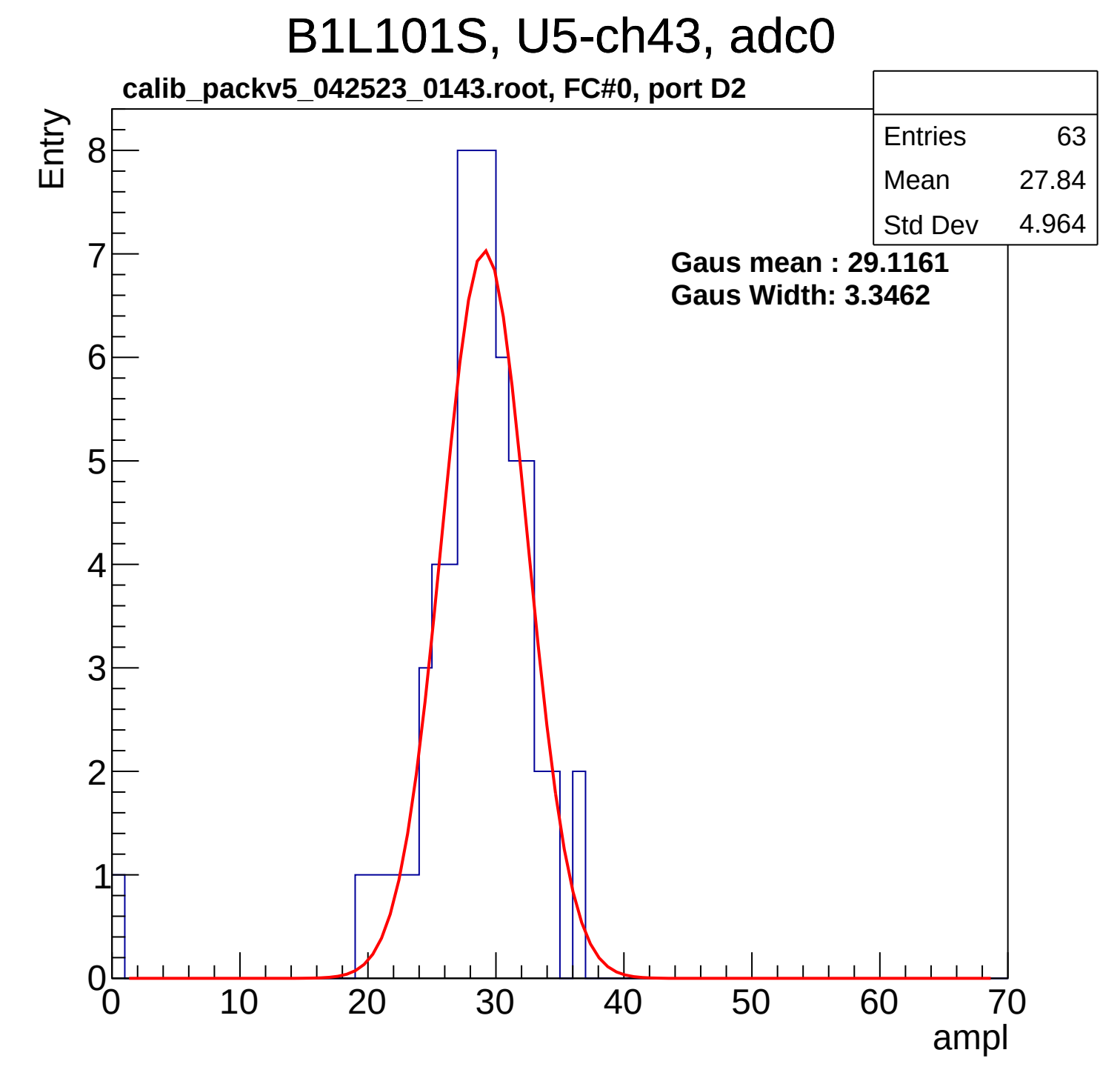

B1L101S, U5-ch42, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 57.48
Std Dev 8.744
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch42, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 18
Mean 61.5
Std Dev 1.302
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L101S, U5-ch42, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch43, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 27.84
Std Dev 4.964
Gaus mean : 29.1161
Gaus Width: 3.3462
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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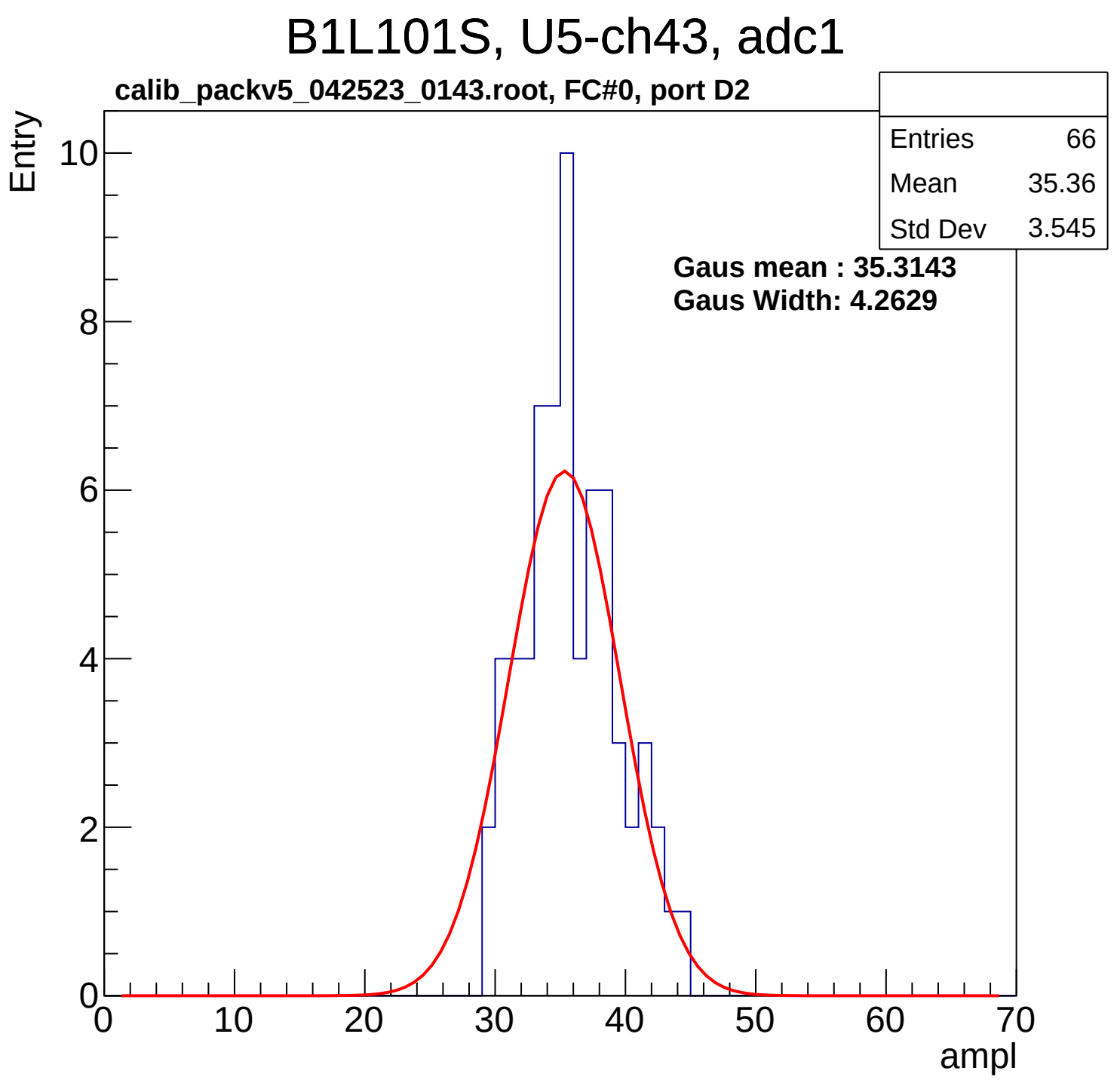
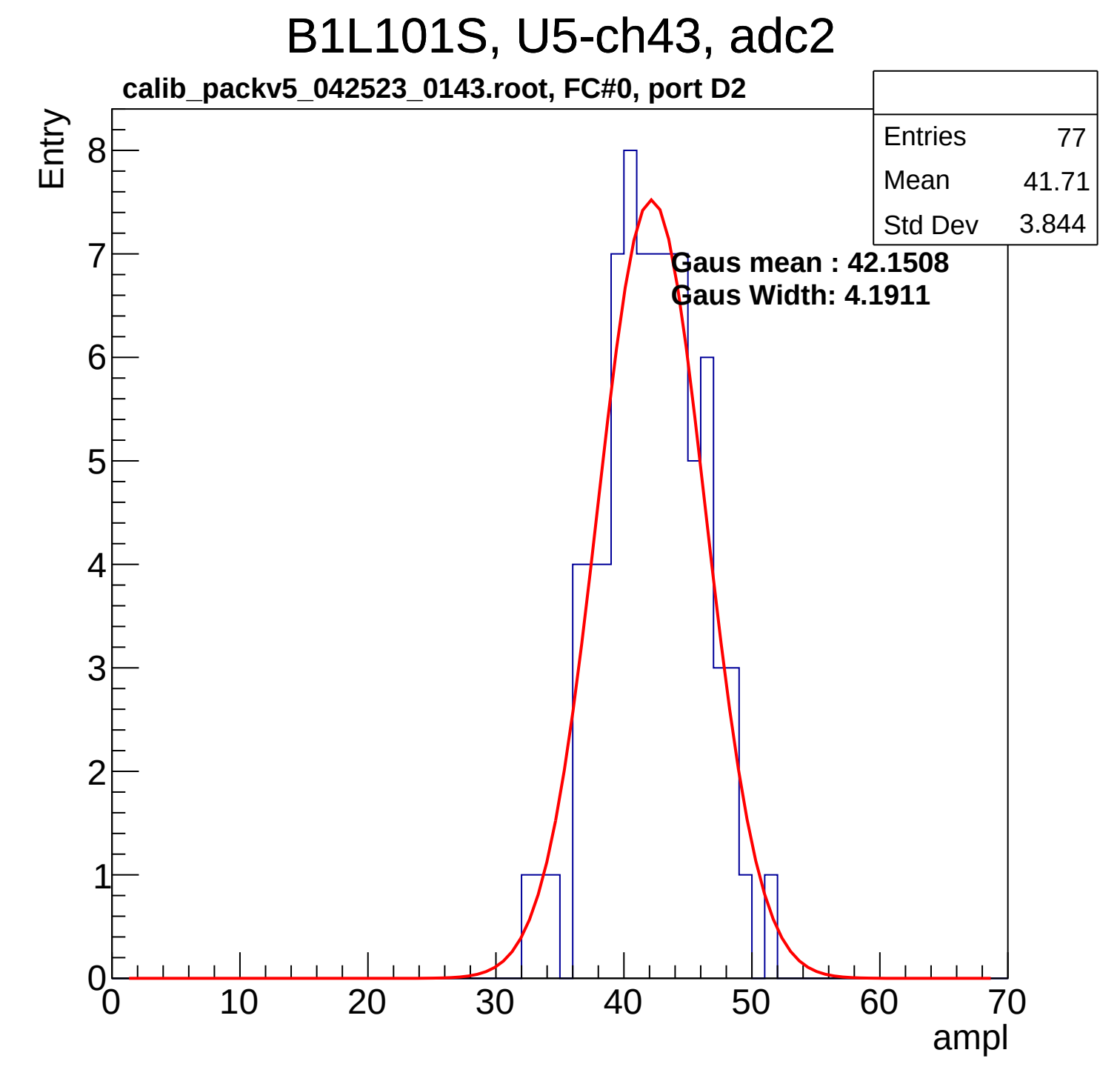

B1L101S, U5-ch43, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 35.36
Std Dev 3.545
Gaus mean : 35.3143
Gaus Width: 4.2629
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch43, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 41.71
Std Dev 3.844
Gaus mean : 42.1508
Gaus Width: 4.1911
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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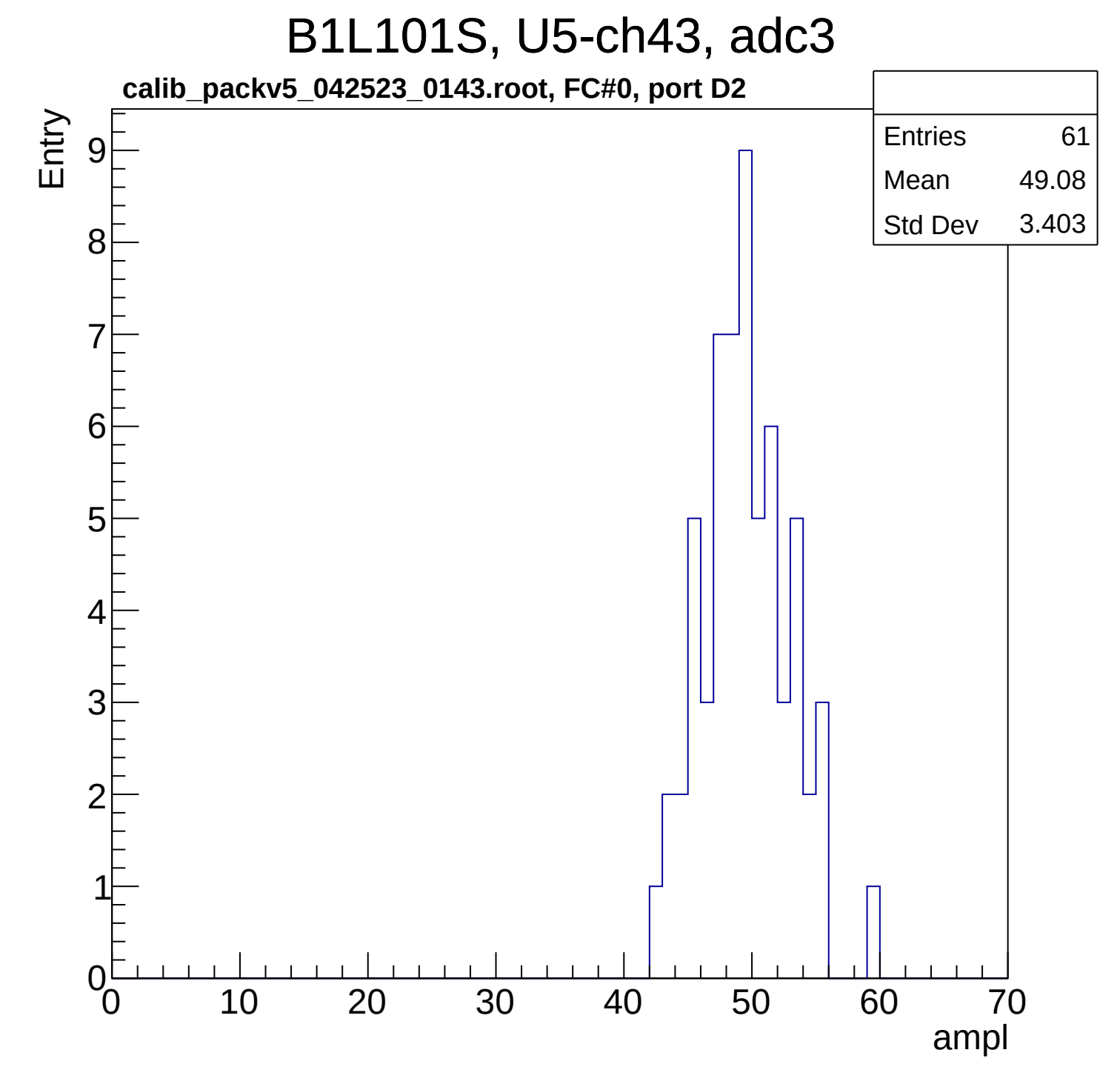
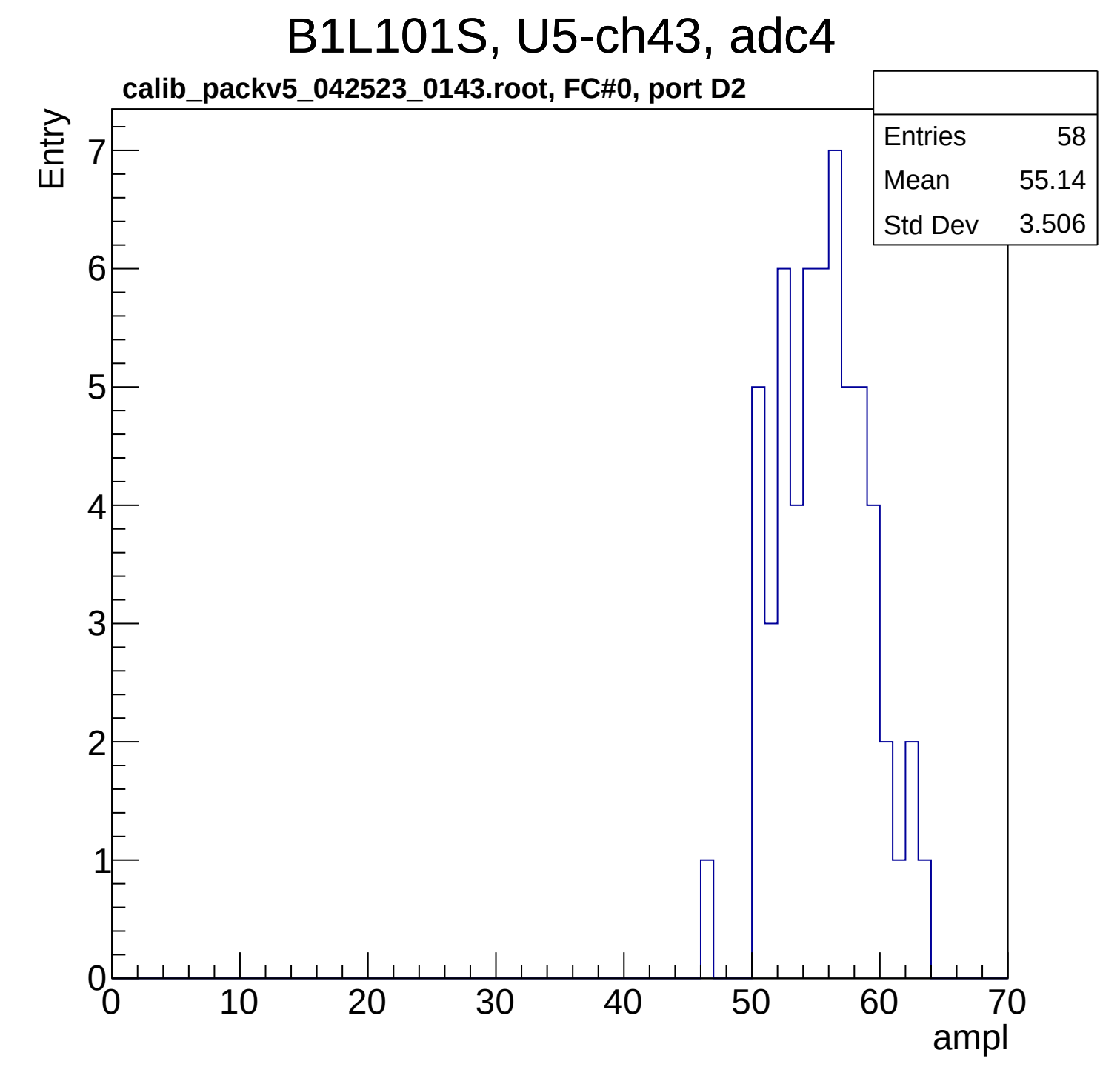
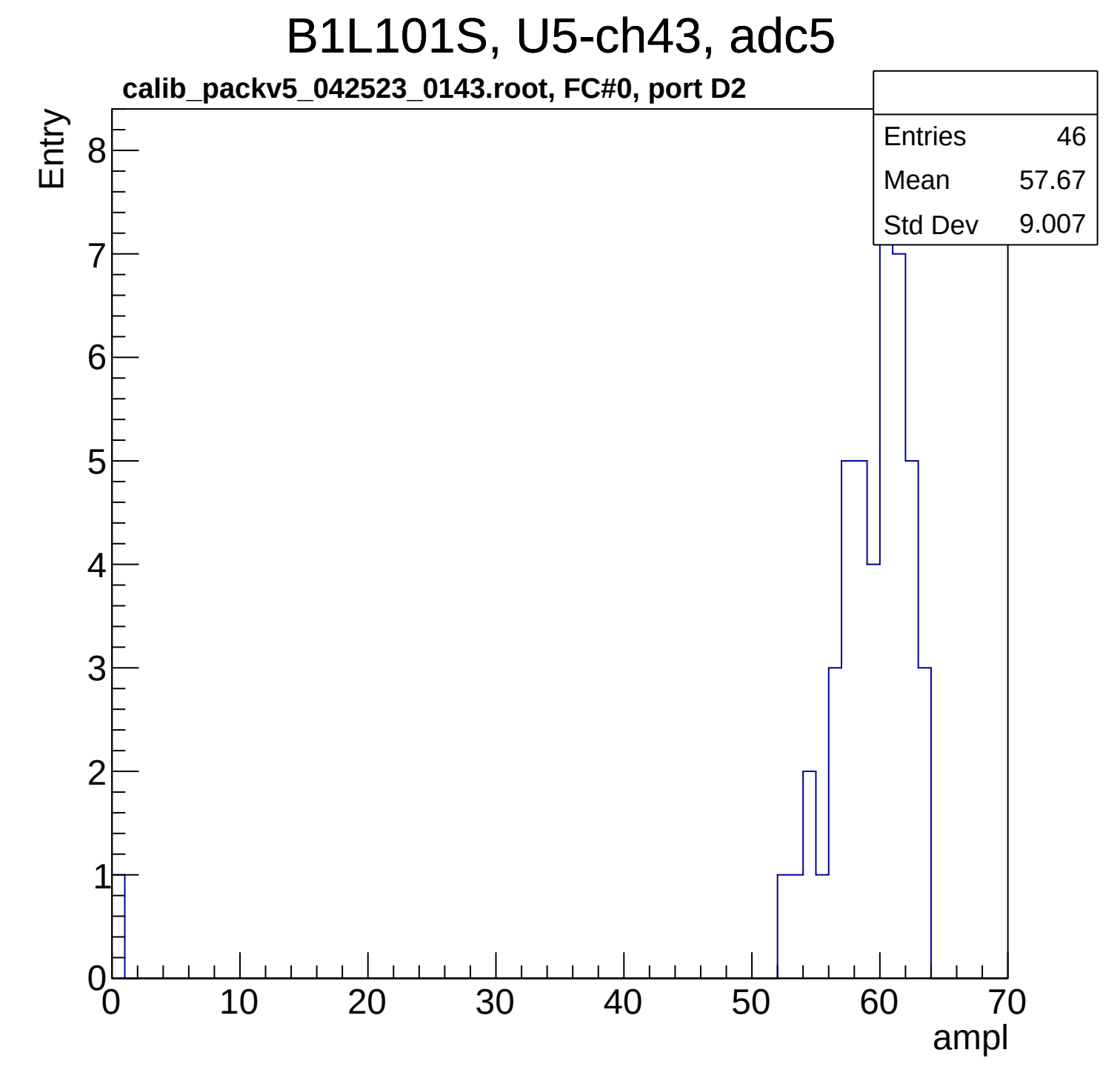
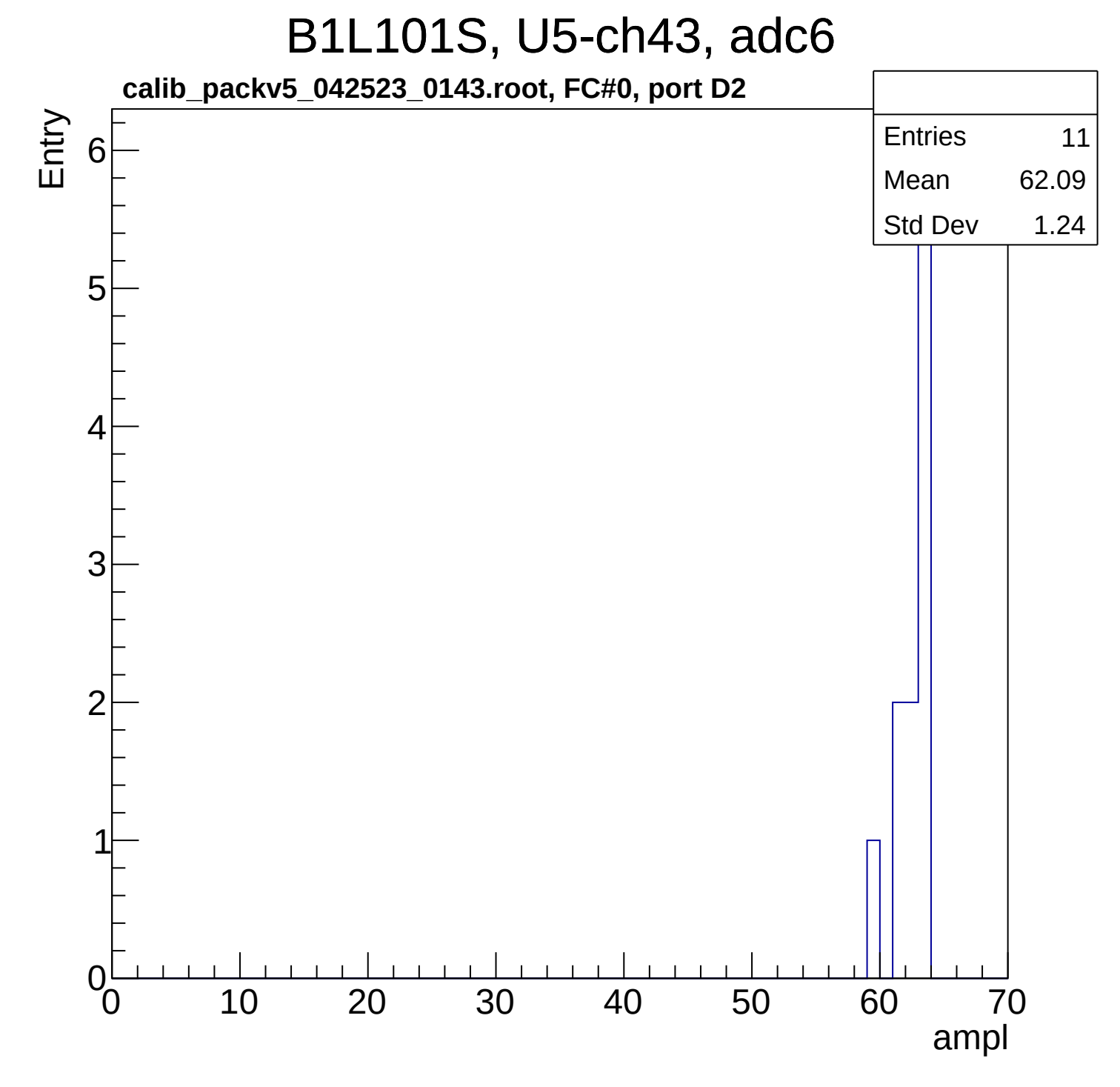
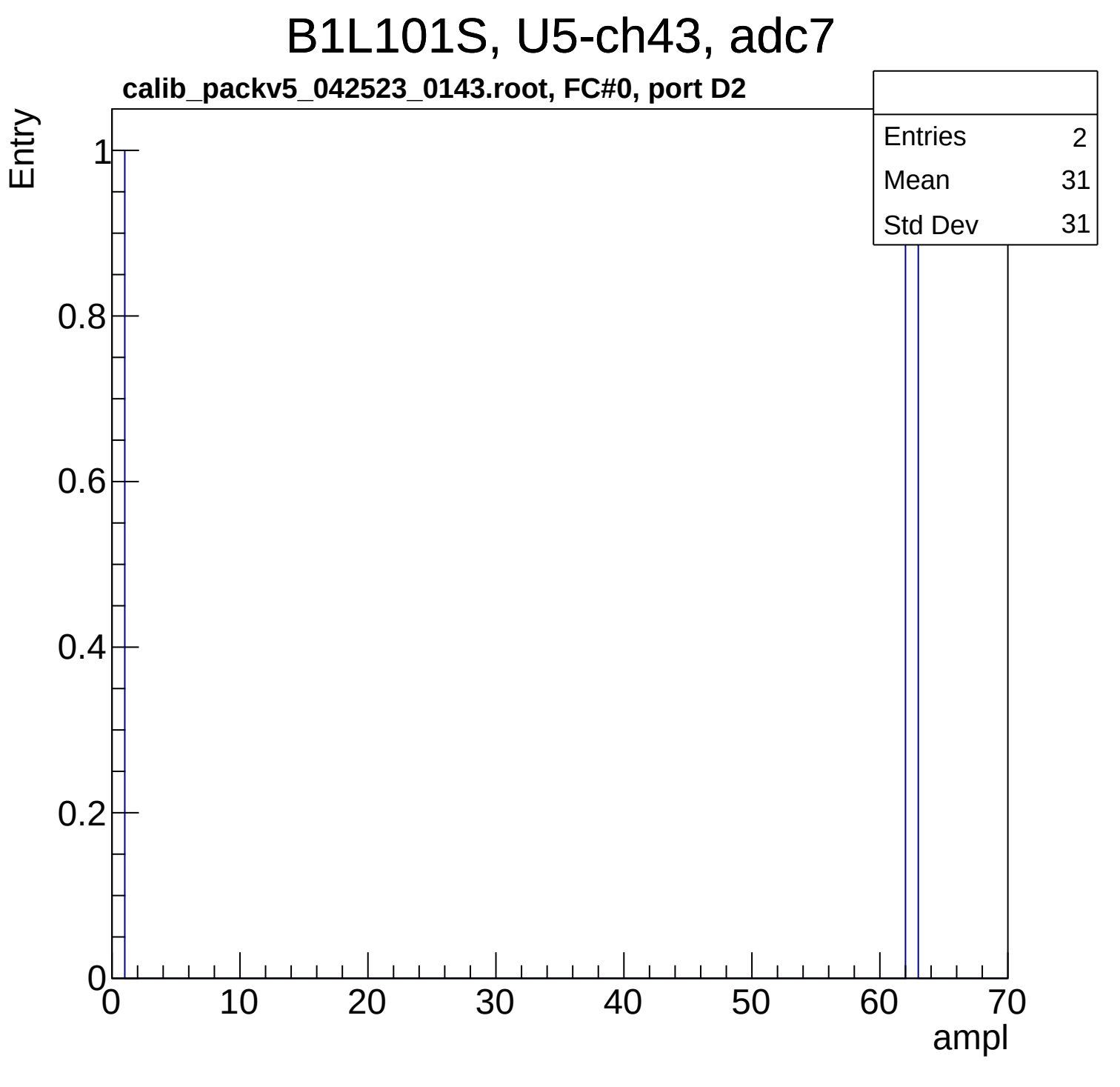
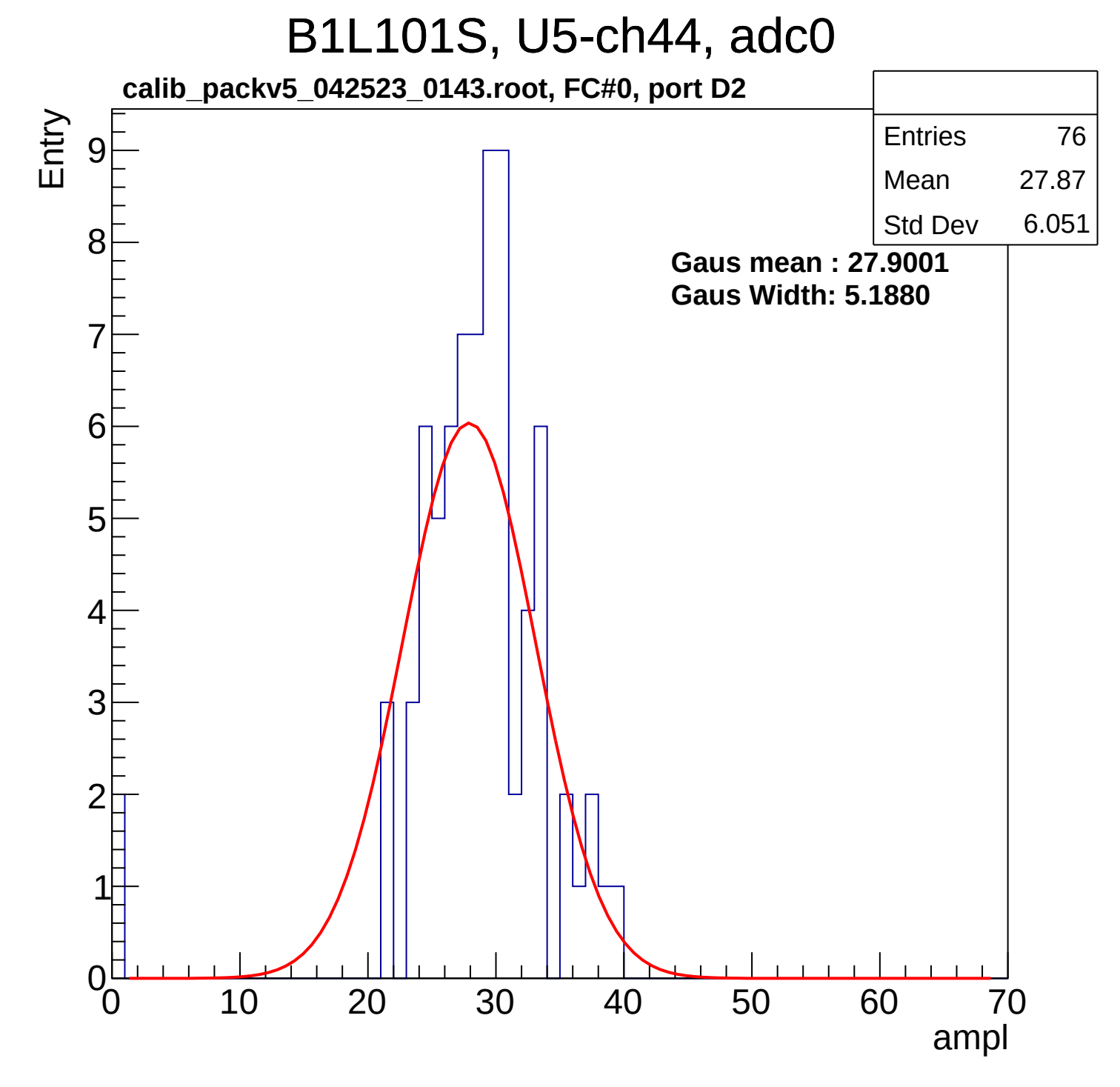

B1L101S, U5-ch43, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 49.08
Std Dev 3.403
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

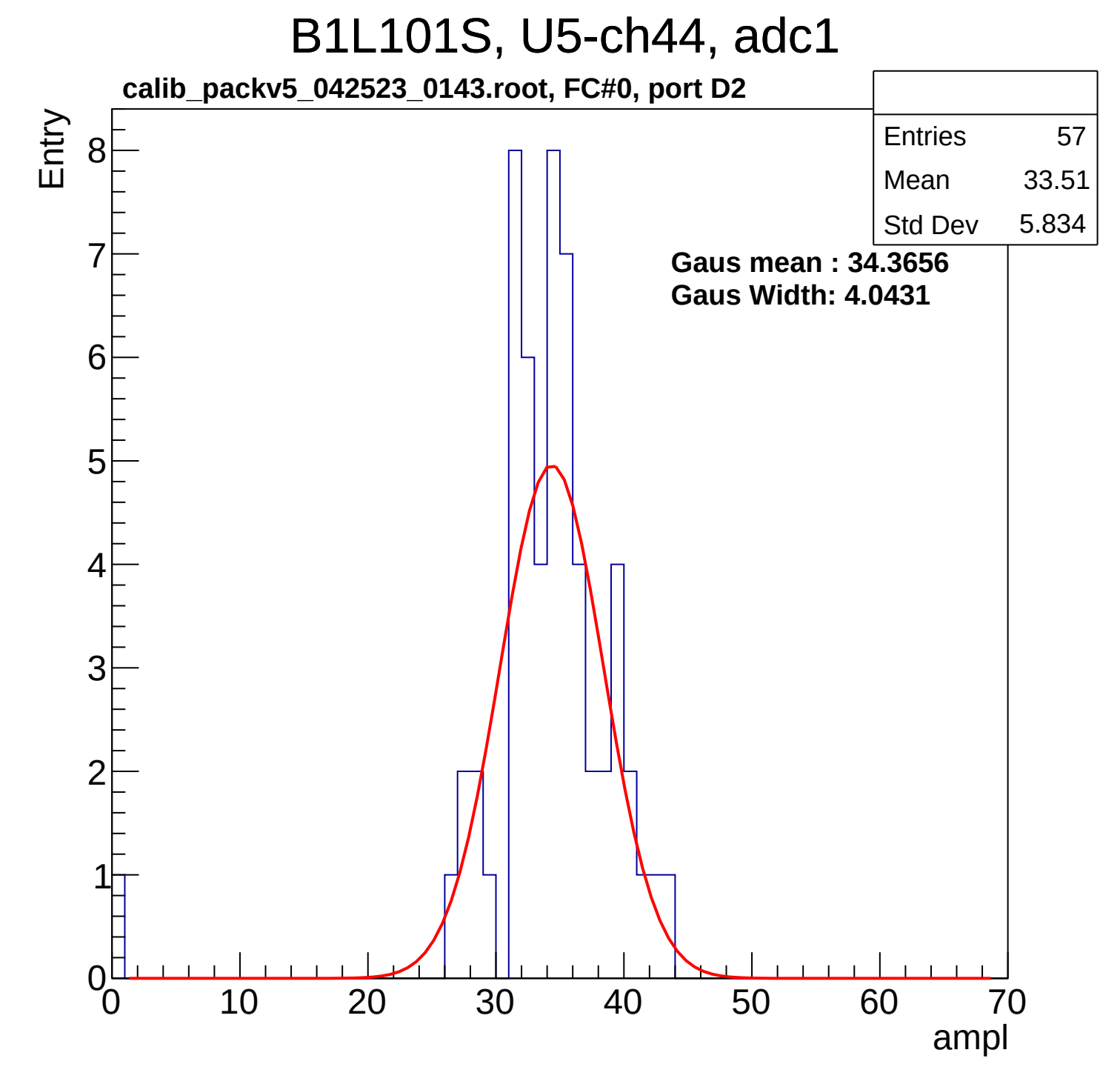

B1L101S, U5-ch43, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 55.14
Std Dev 3.506
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

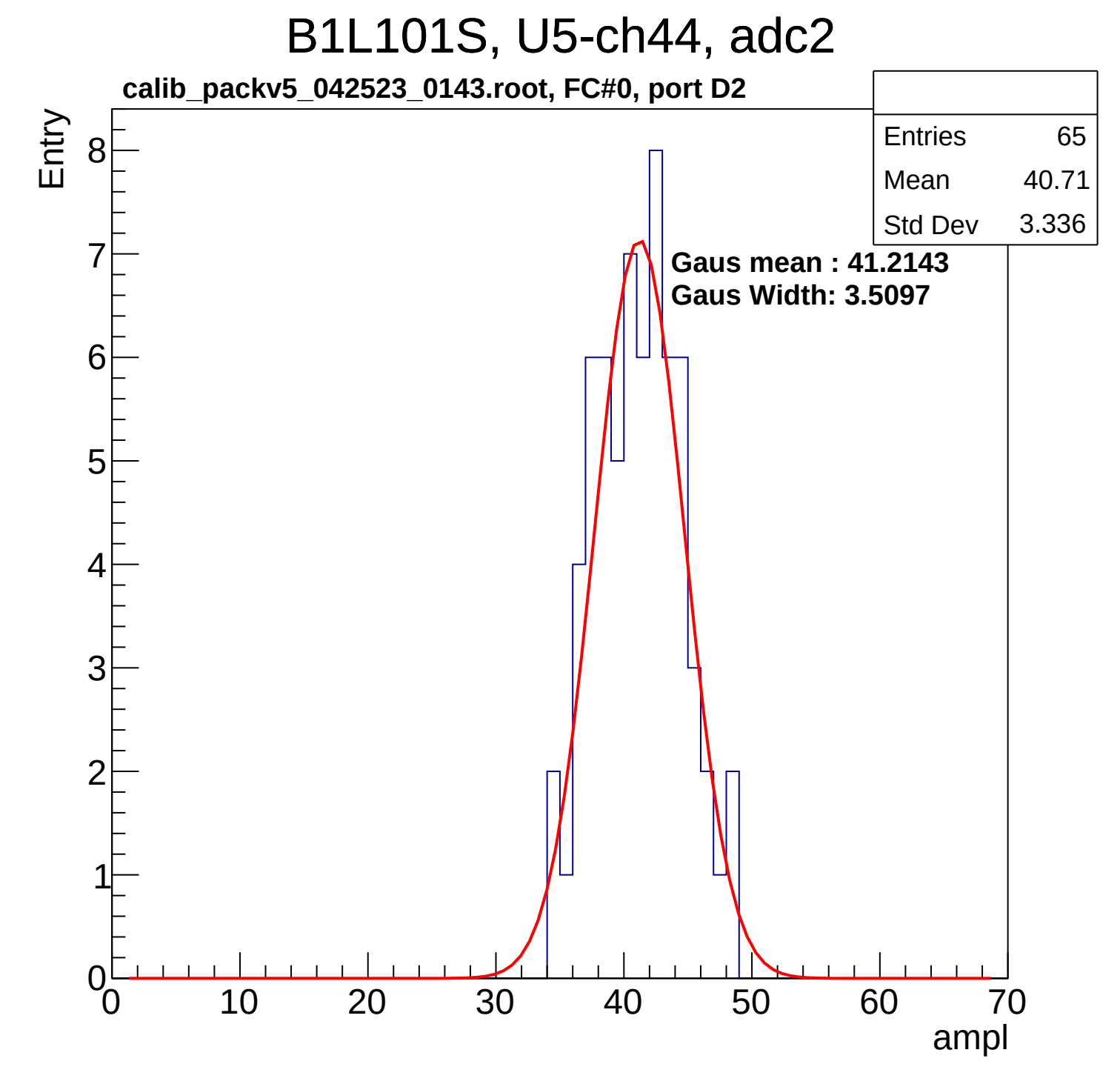

B1L101S, U5-ch43, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 57.67
Std Dev 9.007
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

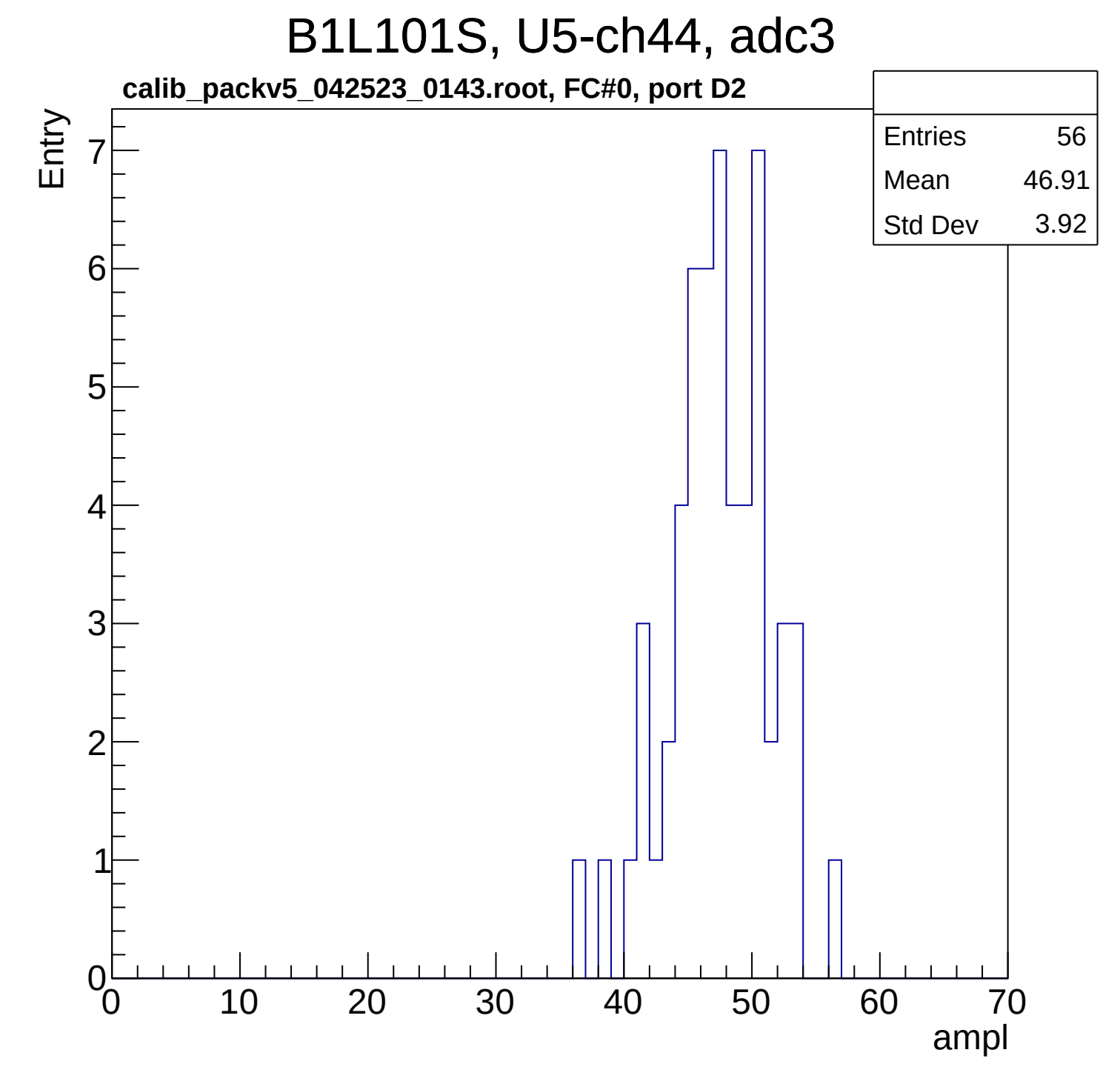

B1L101S, U5-ch43, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 11
Mean 62.09
Std Dev 1.24
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

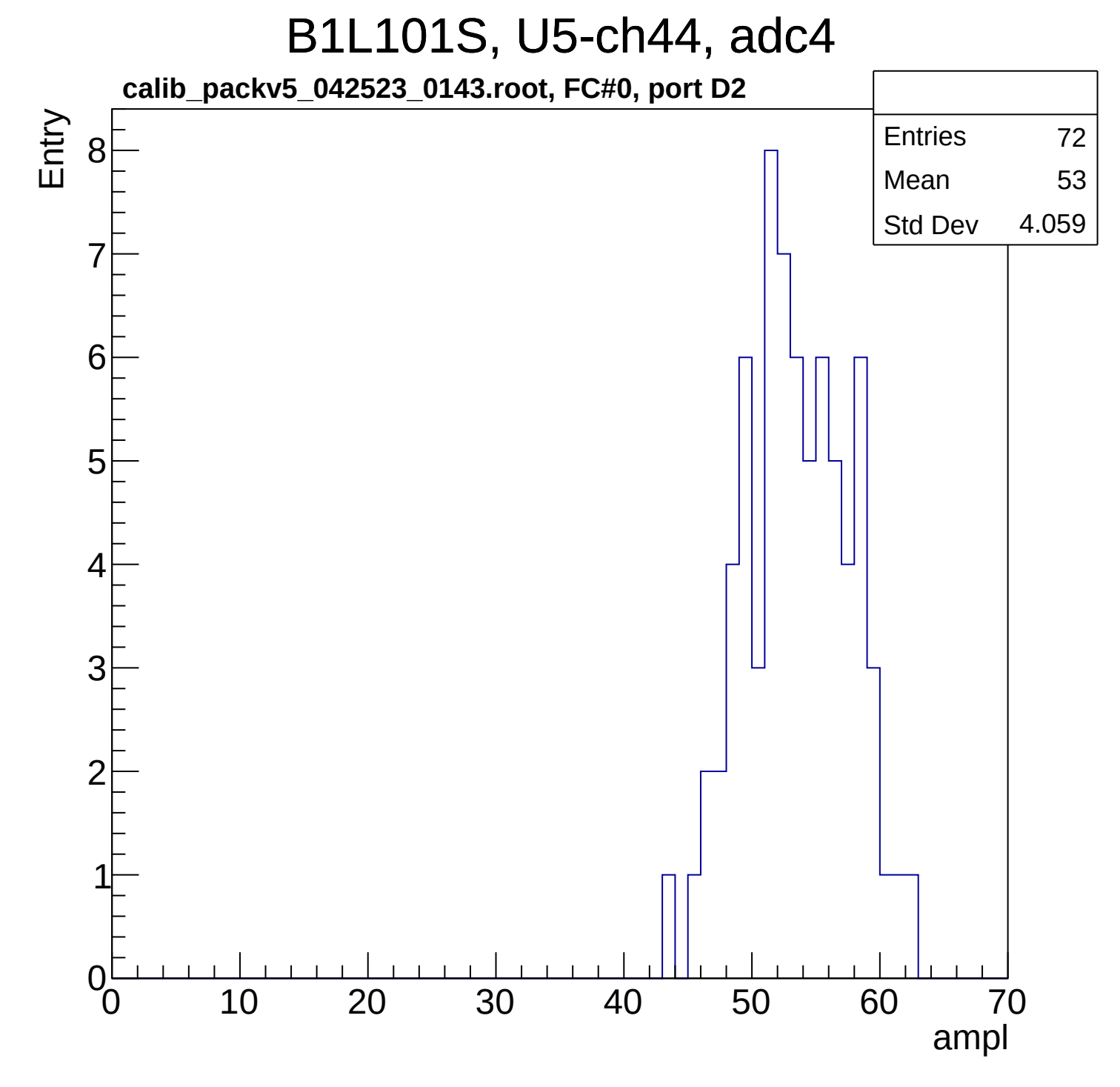

B1L101S, U5-ch43, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 31
Std Dev 31
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

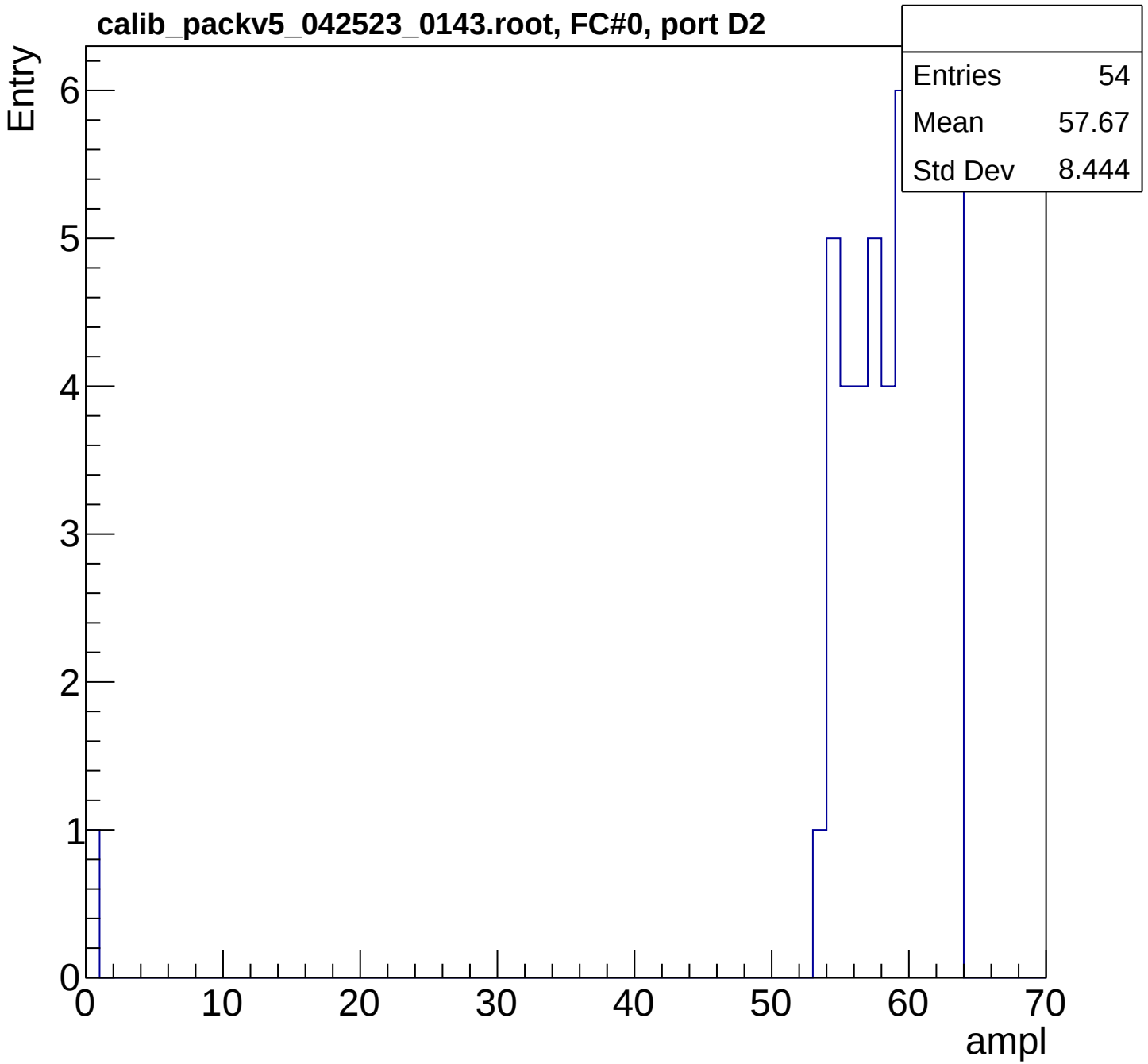

B1L101S, U5-ch44, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 27.87
Std Dev 6.051
Gaus mean : 27.9001
Gaus Width: 5.1880
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

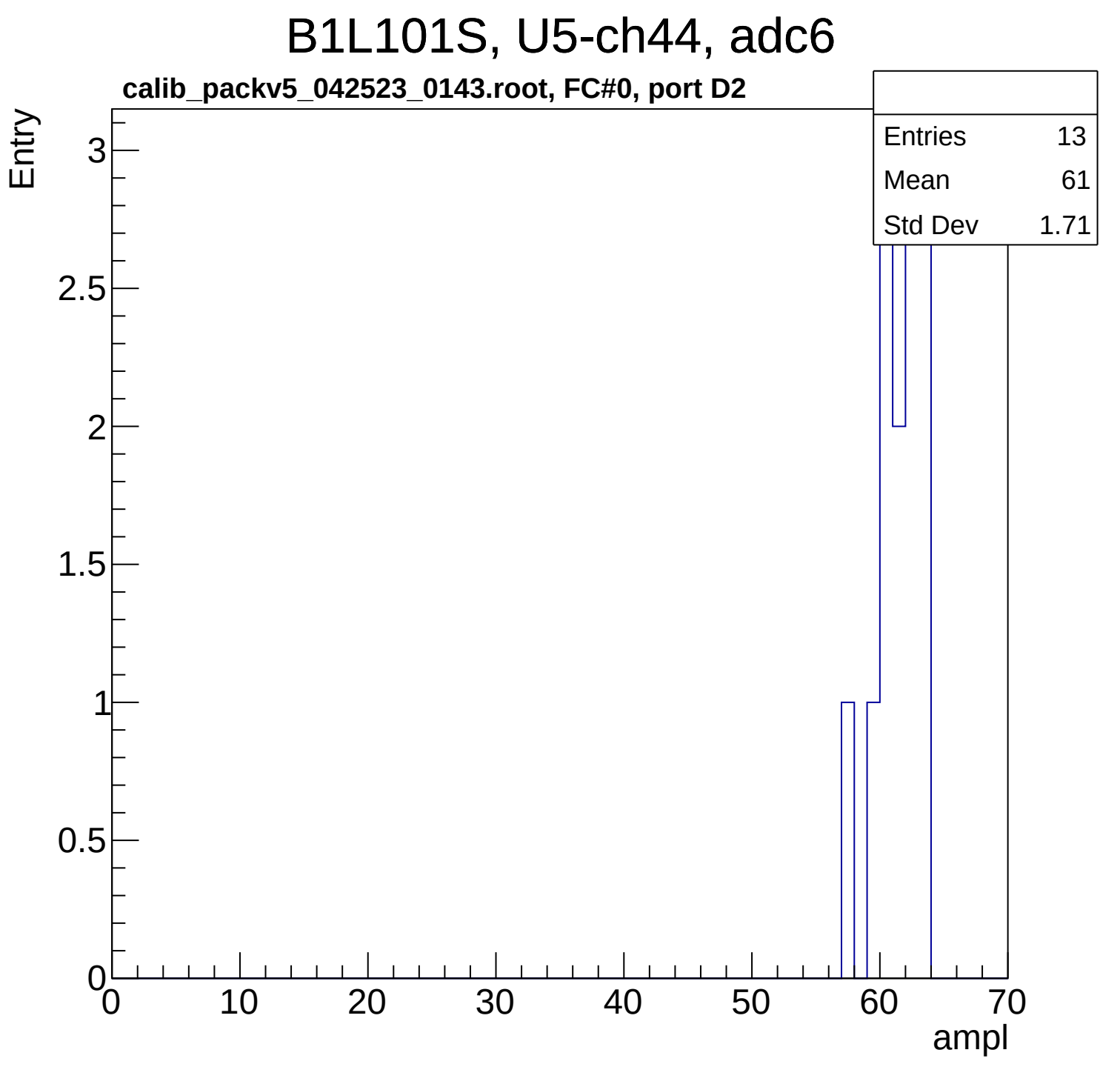

B1L101S, U5-ch44, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 33.51
Std Dev 5.834
Gaus mean : 34.3656
Gaus Width: 4.0431
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch44, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 40.71
Std Dev 3.336
Gaus mean : 41.2143
Gaus Width: 3.5097
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch44, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 46.91
Std Dev 3.92
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch44, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 53
Std Dev 4.059
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch44, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 57.67
Std Dev 8.444
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch44, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 13
Mean 61
Std Dev 1.71
Entry
ampl
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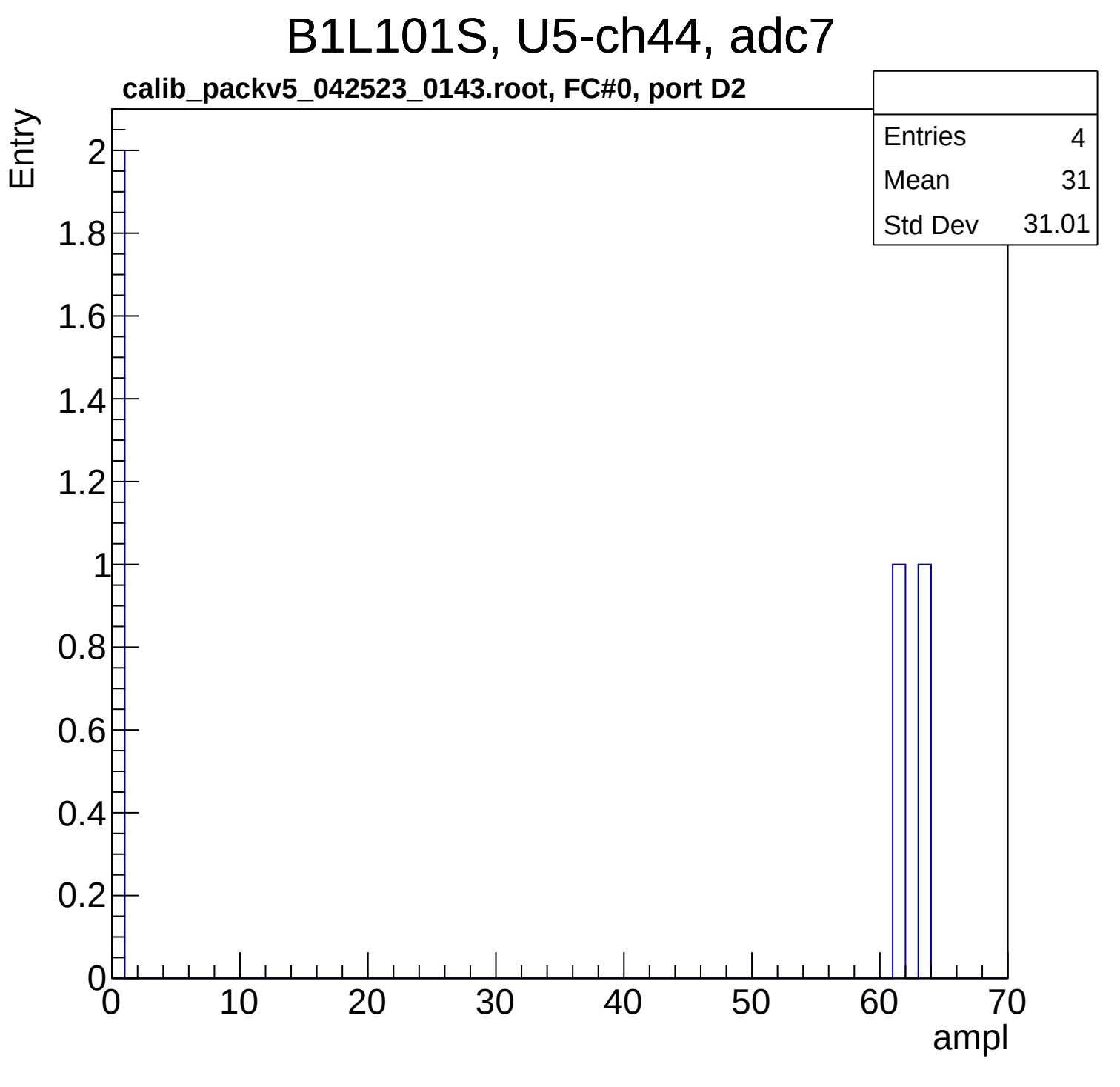
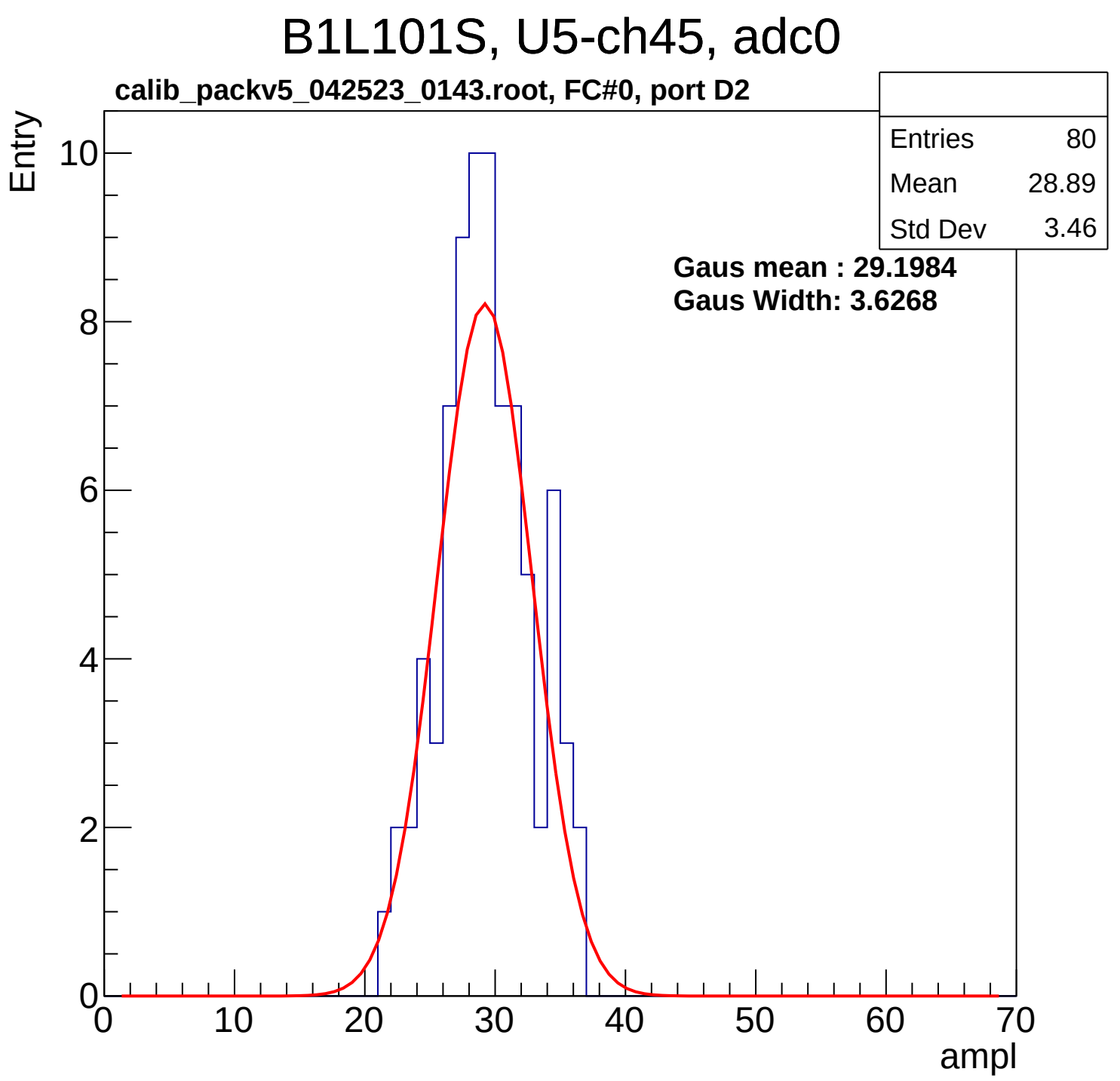
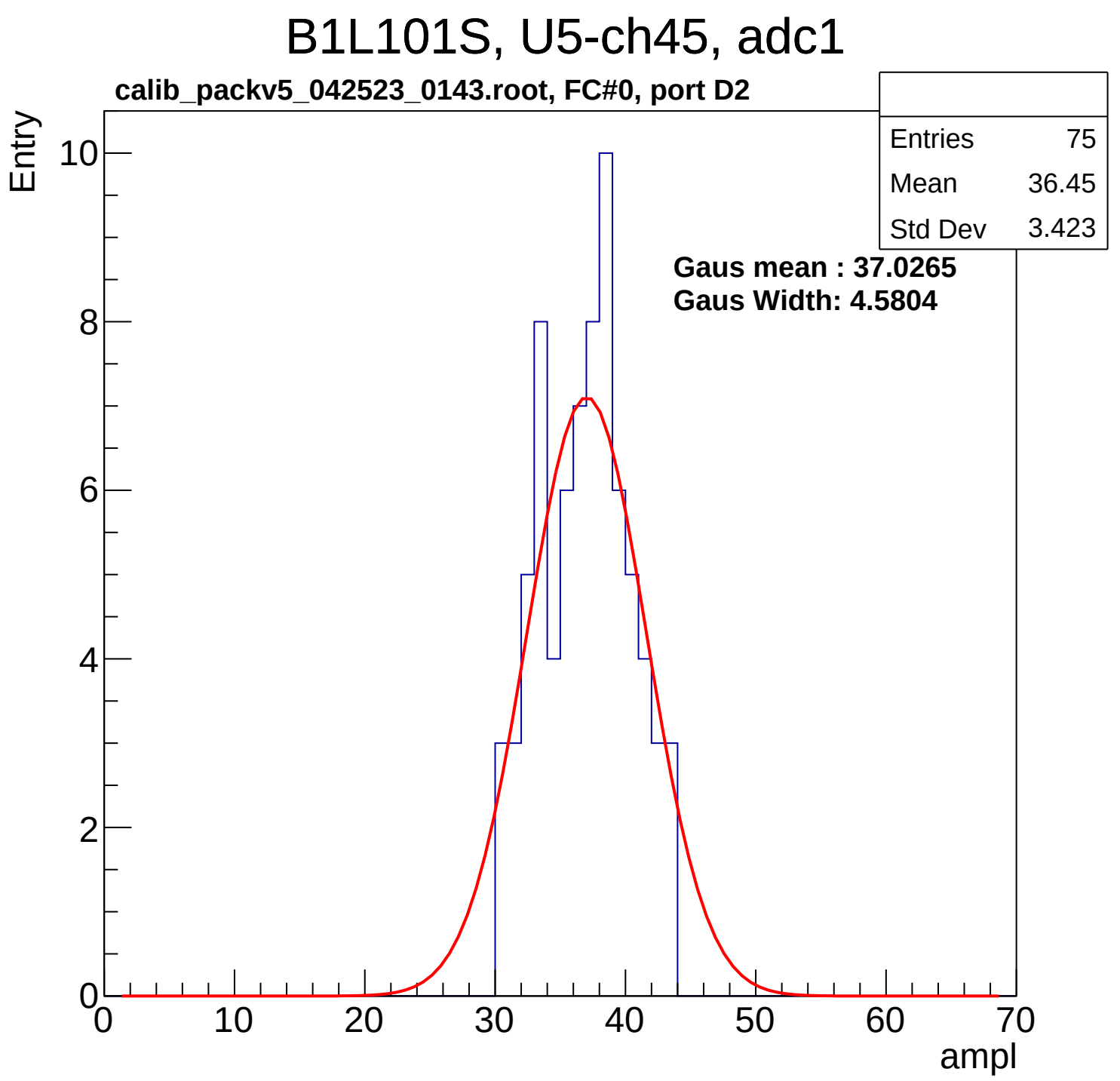
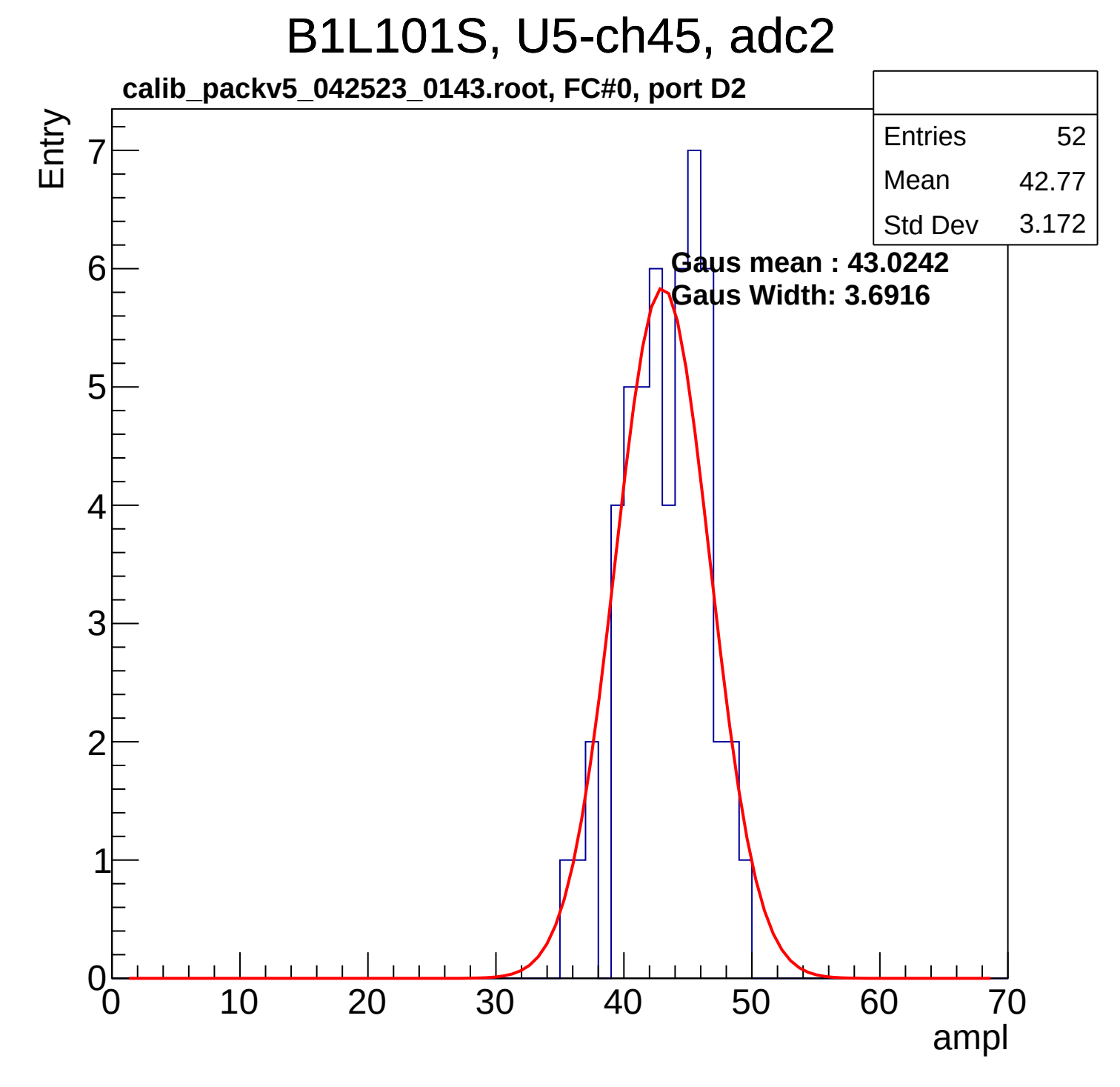
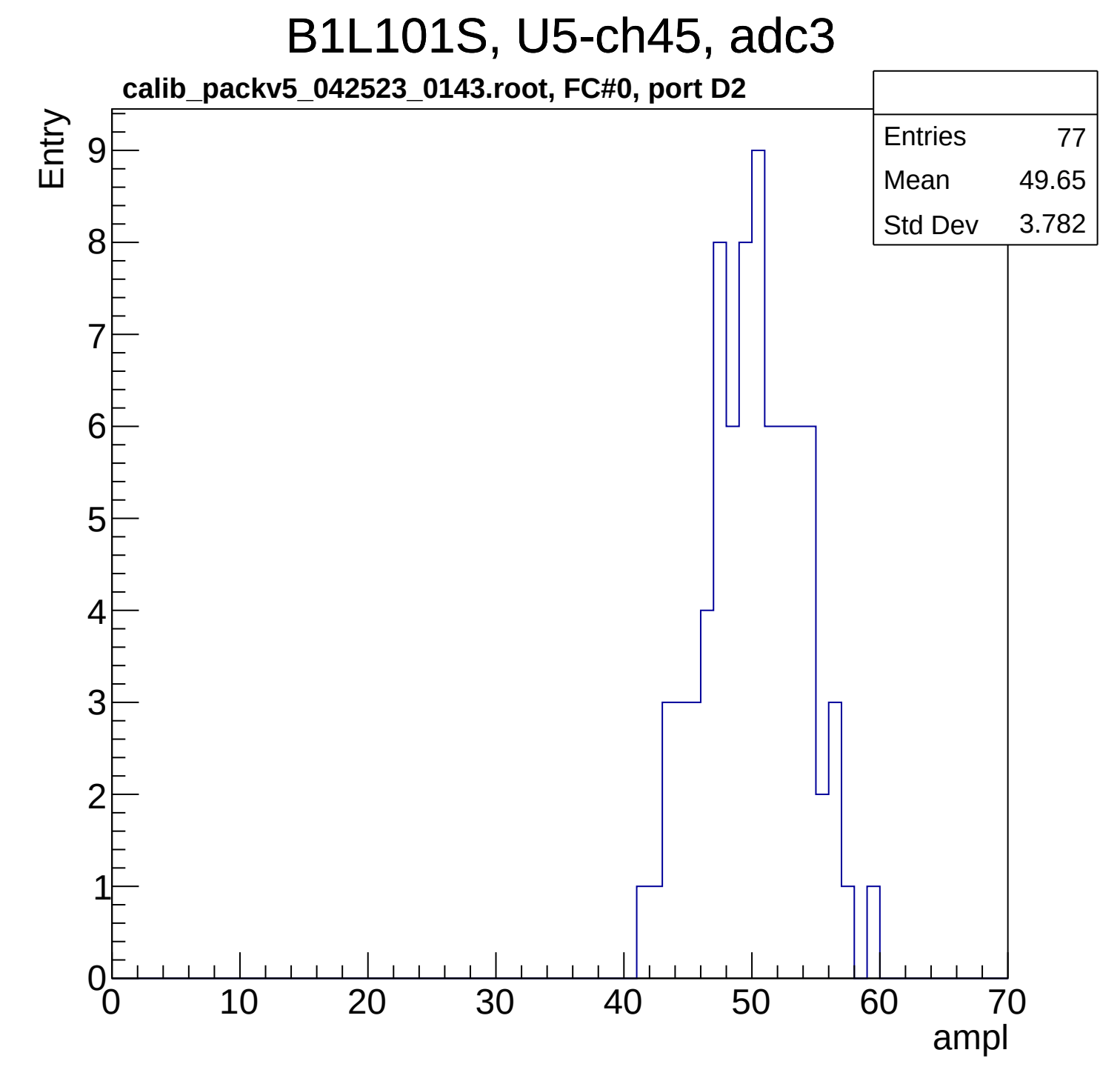
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U5-ch44, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 31
Std Dev 31.01
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U5-ch45, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 80
Mean 28.89
Std Dev 3.46
Gaus mean : 29.1984
Gaus Width: 3.6268
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch45, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 36.45
Std Dev 3.423
Gaus mean : 37.0265
Gaus Width: 4.5804
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch45, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 42.77
Std Dev 3.172
Gaus mean : 43.0242
Gaus Width: 3.6916
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch45, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 49.65
Std Dev 3.782
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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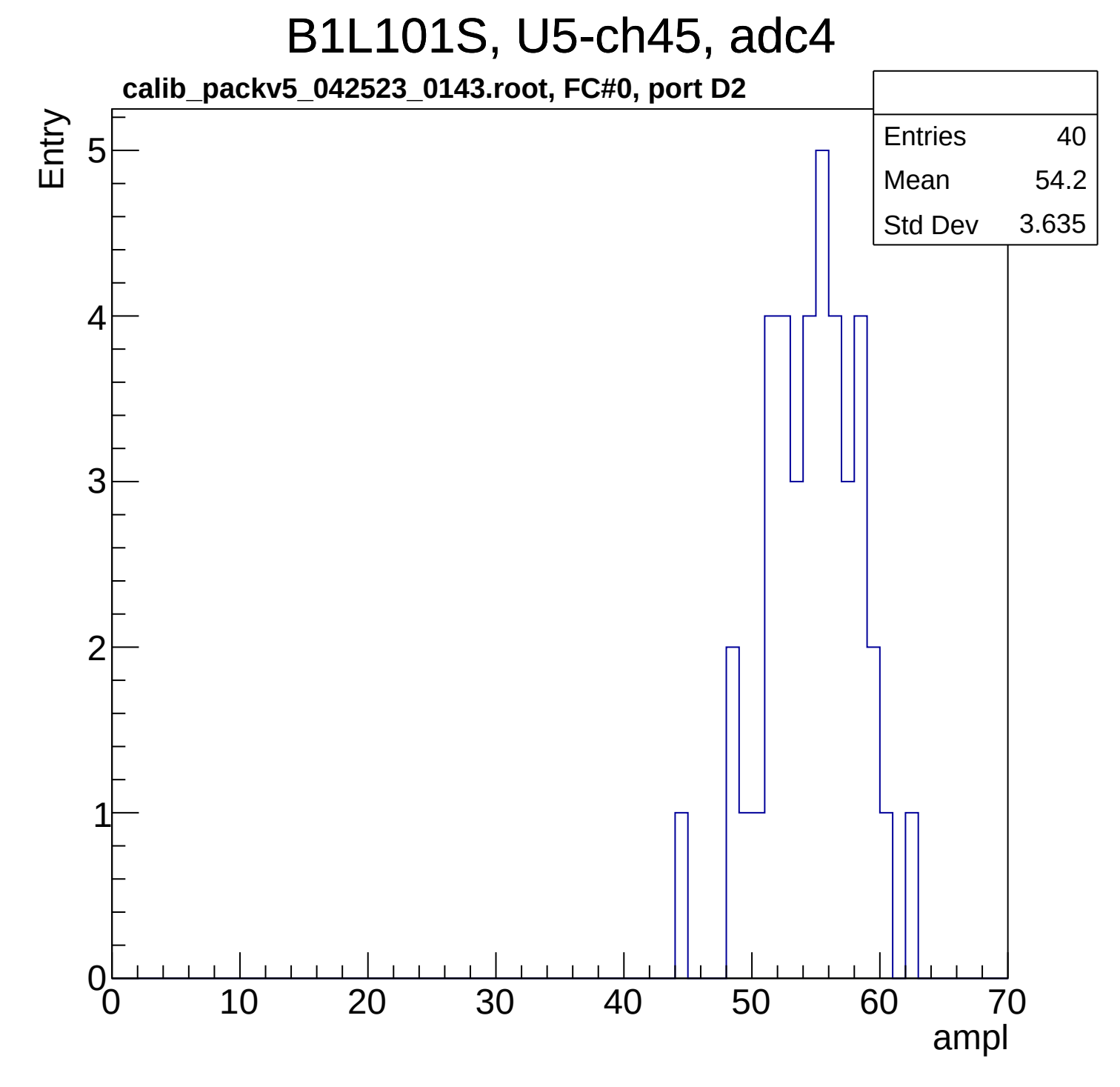
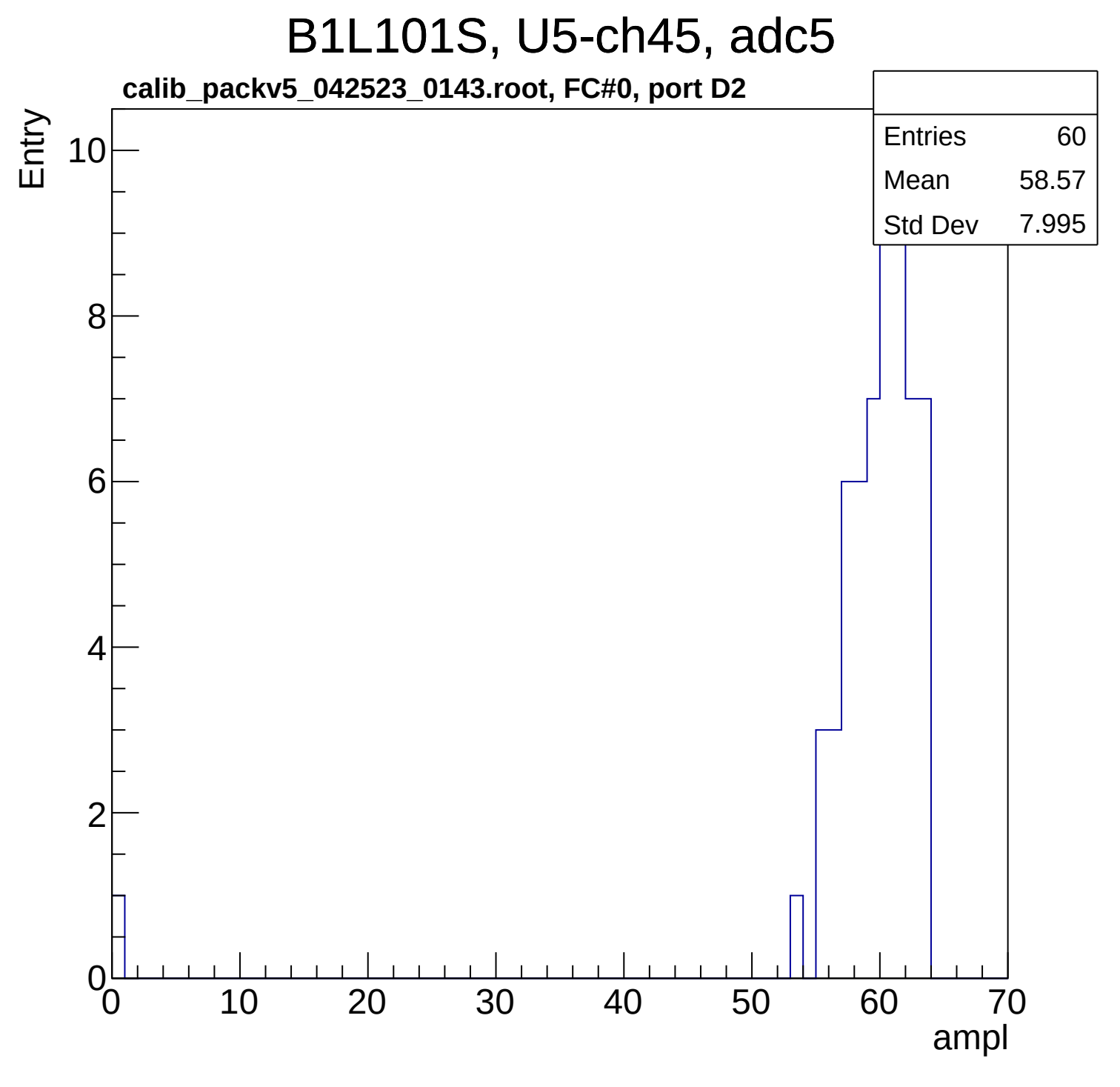
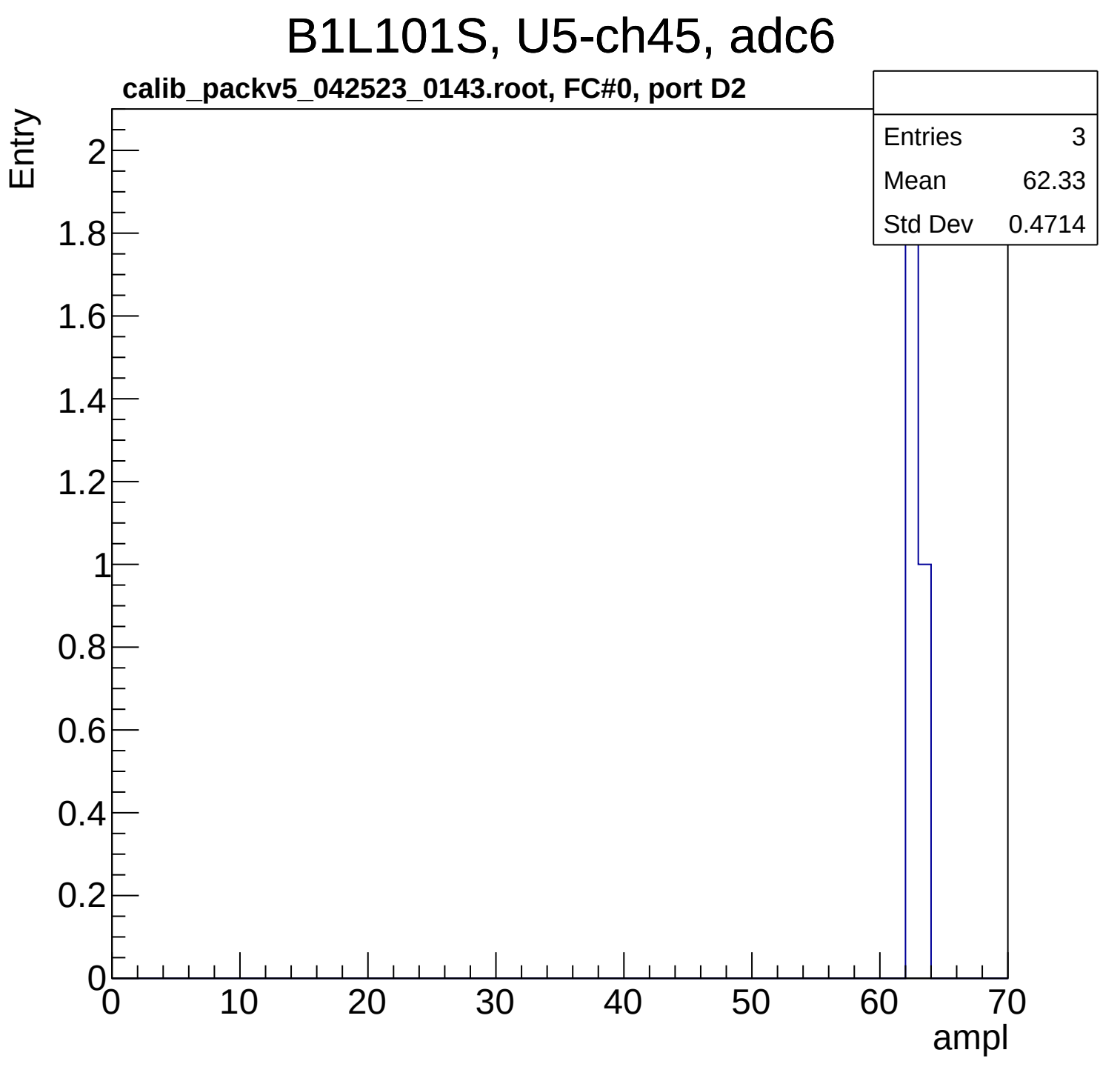
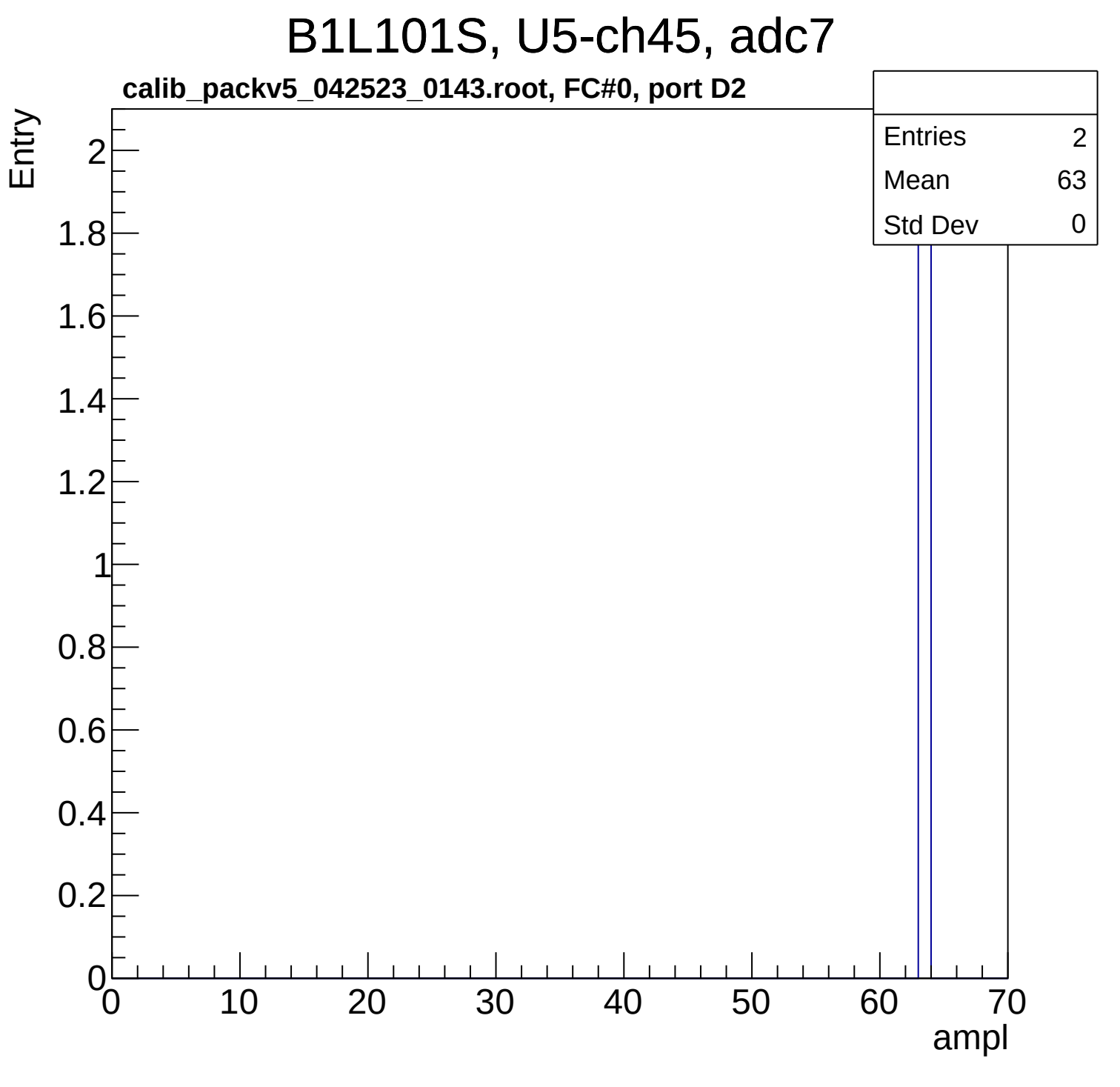

B1L101S, U5-ch45, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 40
Mean 54.2
Std Dev 3.635
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch45, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 58.57
Std Dev 7.995
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch45, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U5-ch45, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
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60
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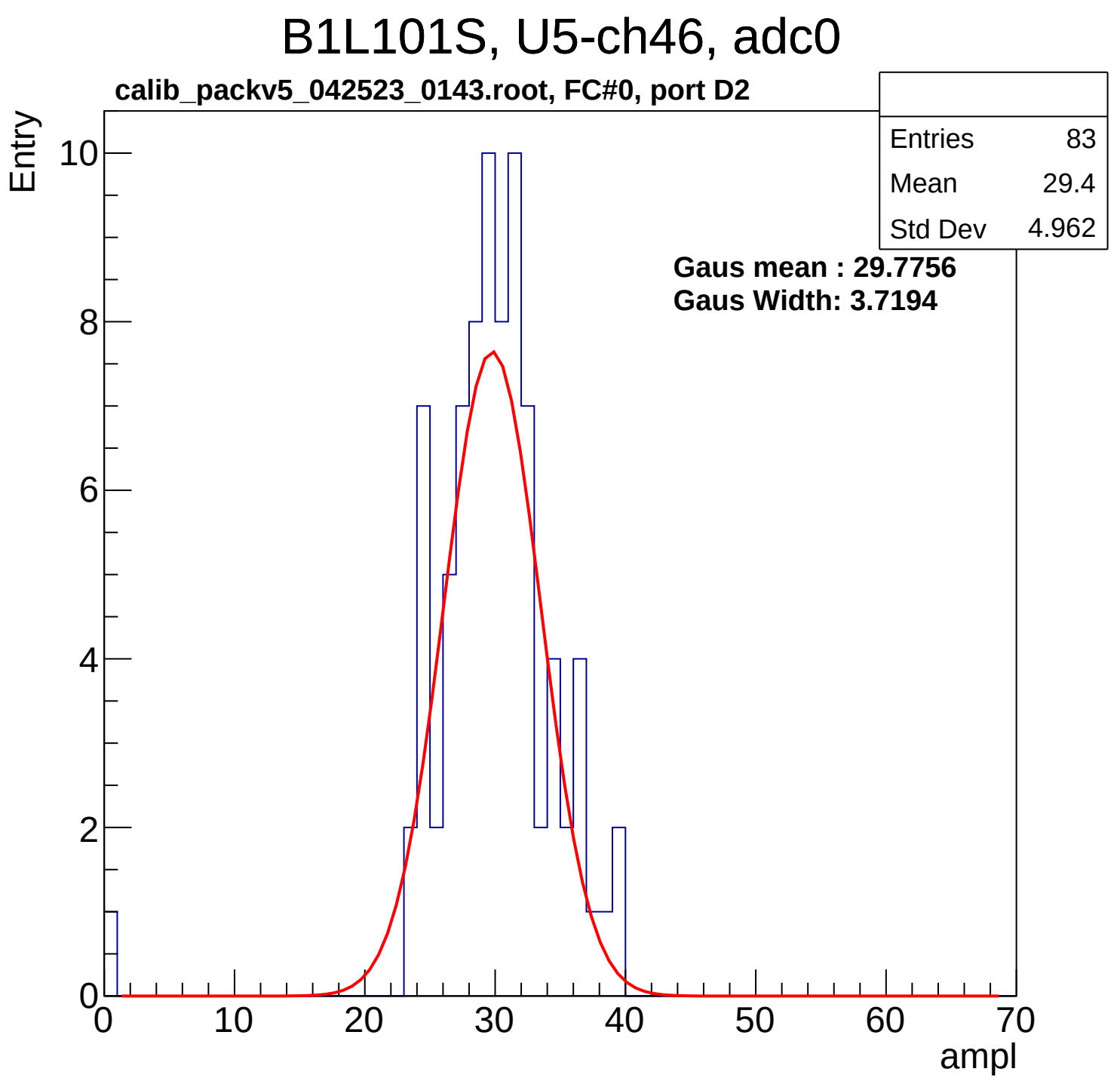
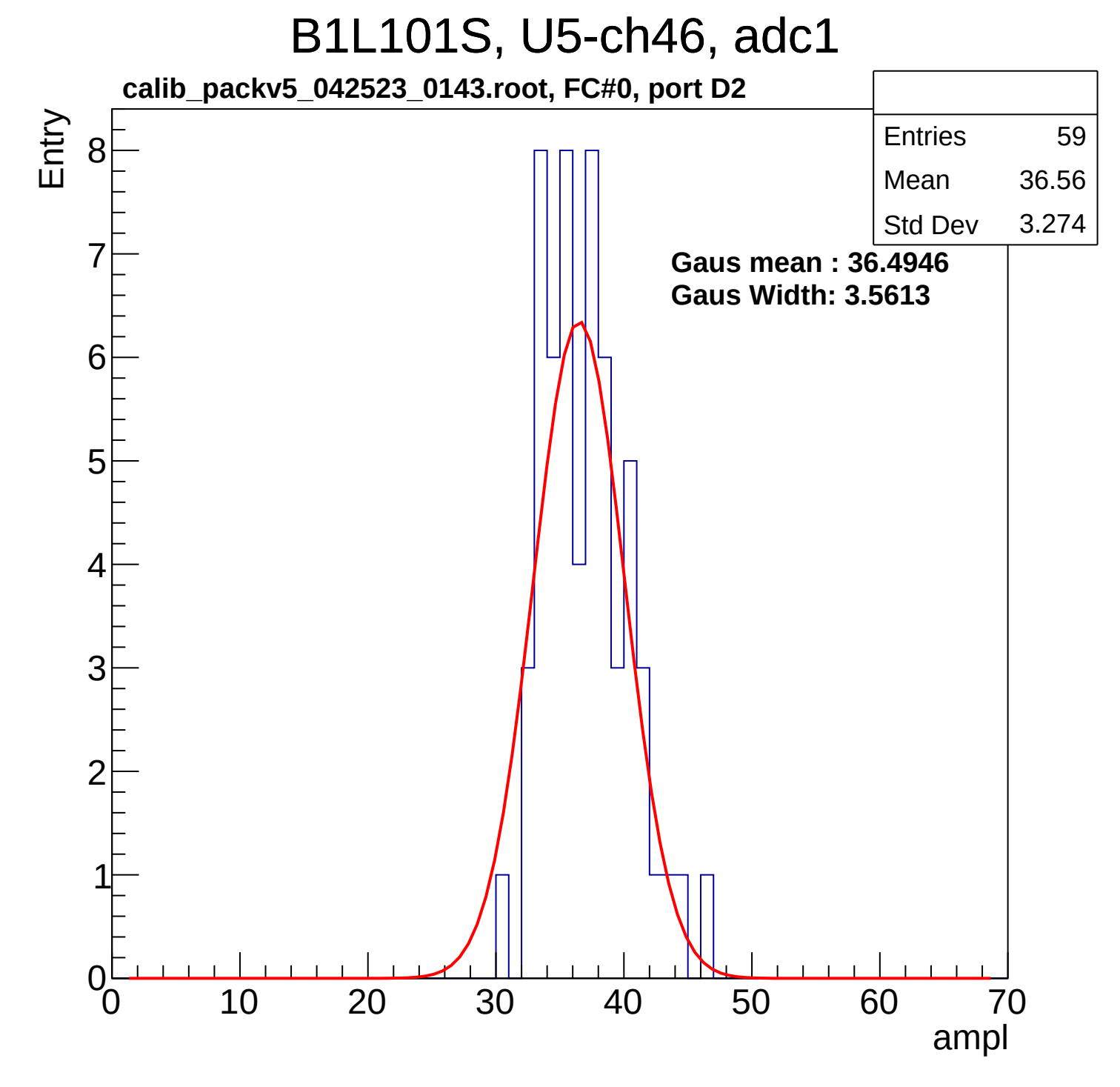
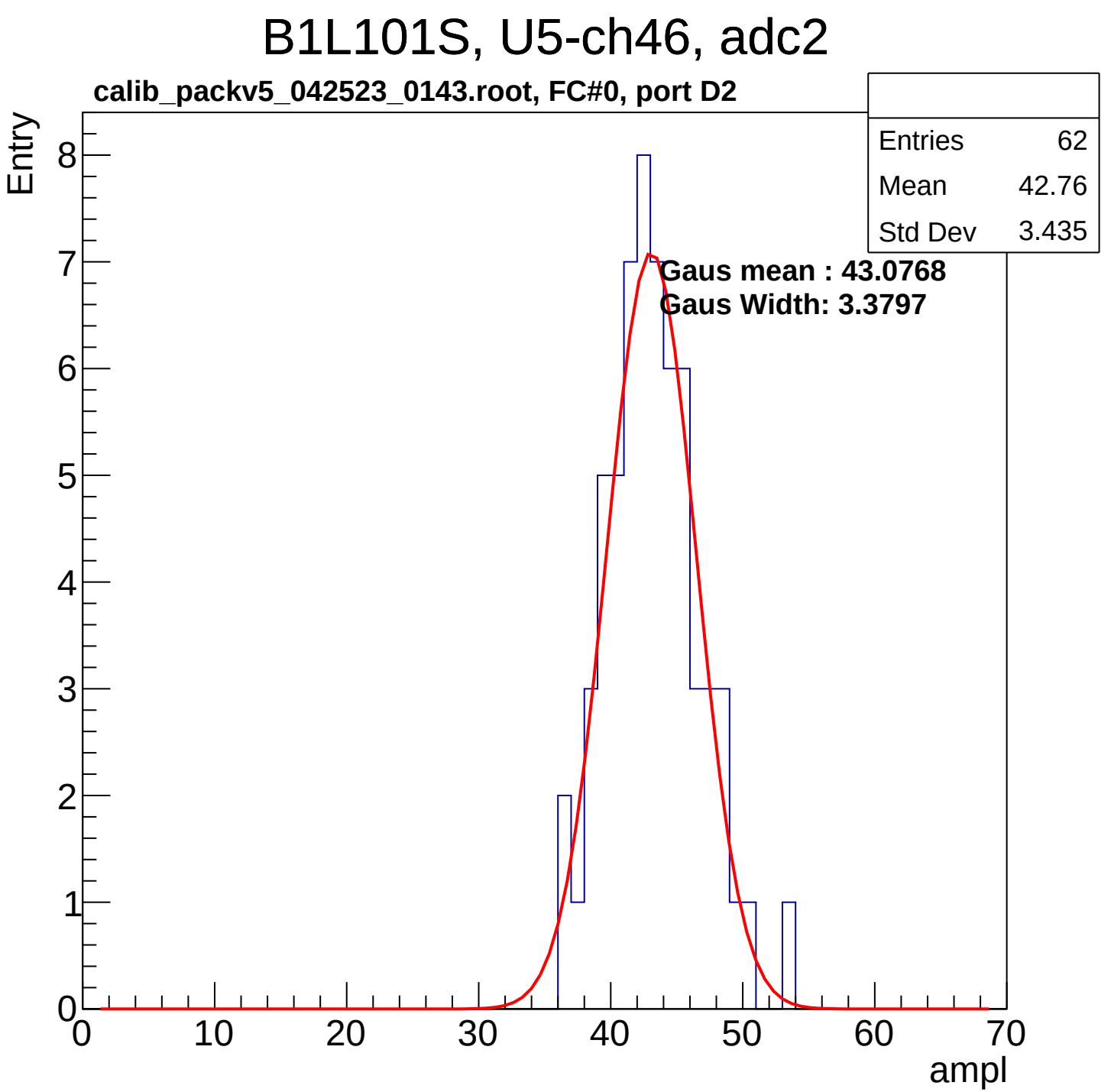

B1L101S, U5-ch46, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 83
Mean 29.4
Std Dev 4.962
Gaus mean : 29.7756
Gaus Width: 3.7194
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch46, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 36.56
Std Dev 3.274
Gaus mean : 36.4946
Gaus Width: 3.5613
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch46, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 42.76
Std Dev 3.435
Gaus mean : 43.0768
Gaus Width: 3.3797
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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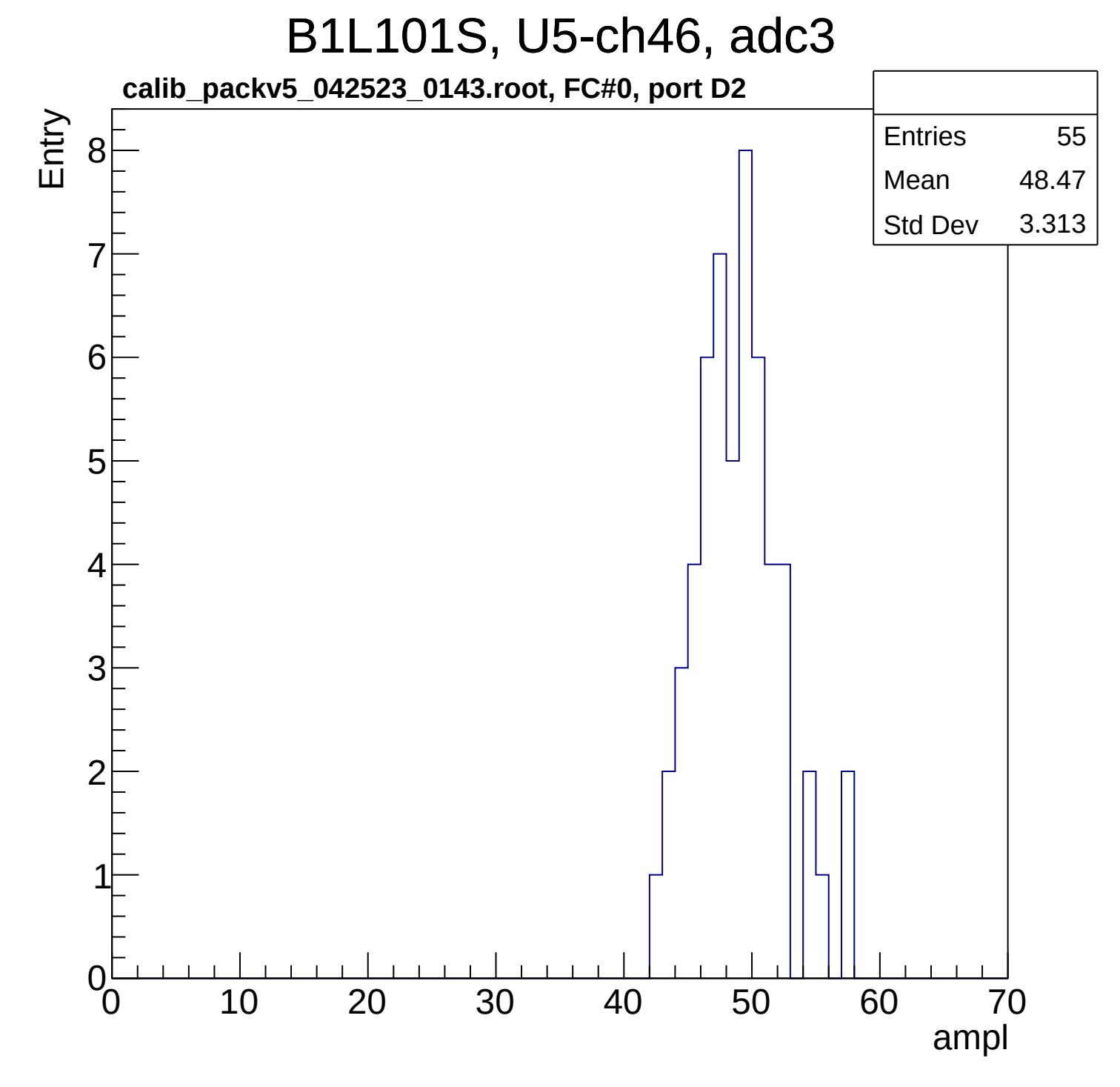
B1L101S, U5-ch46, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 48.47
Std Dev 3.313
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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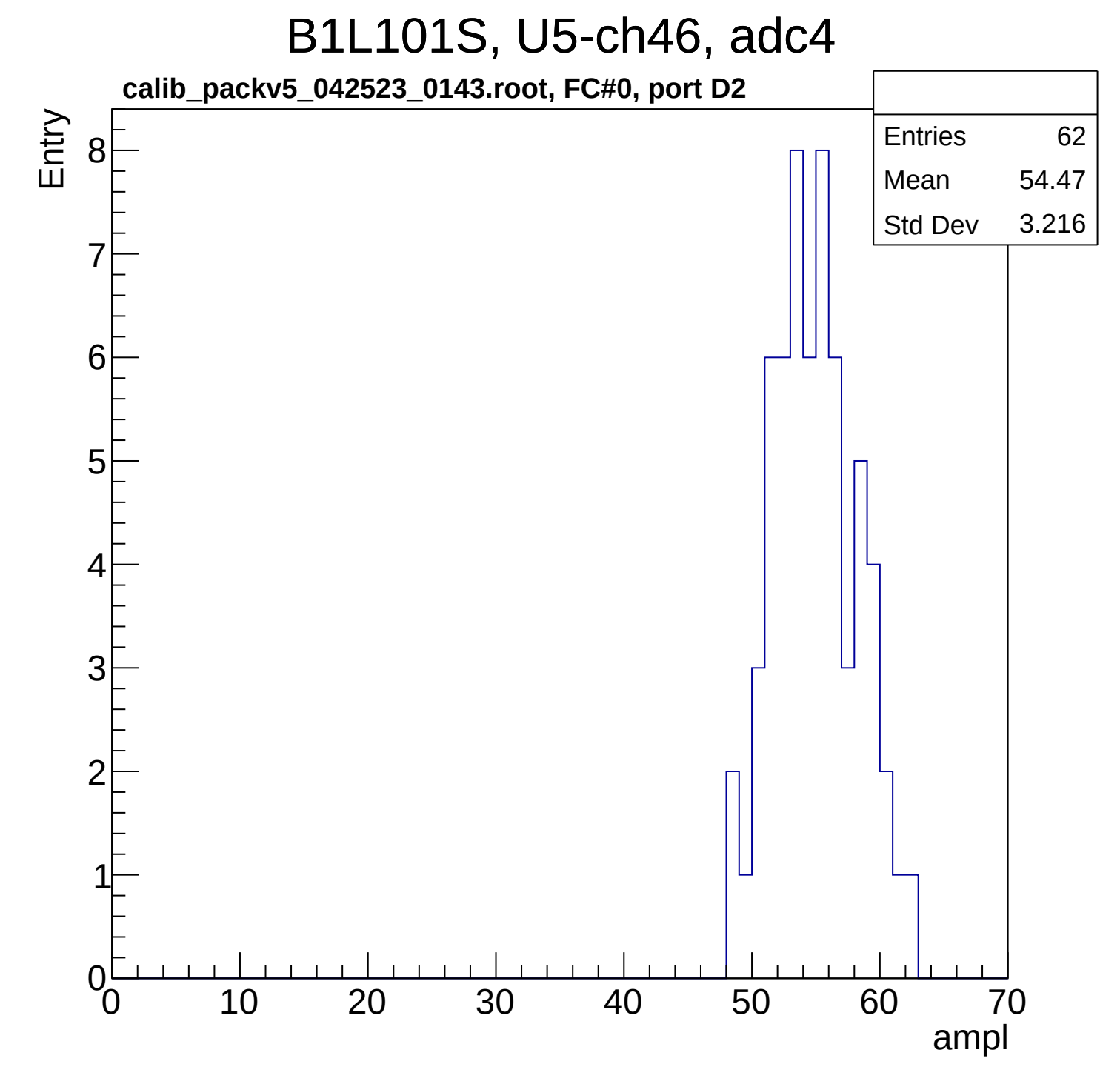
B1L101S, U5-ch46, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 54.47
Std Dev 3.216
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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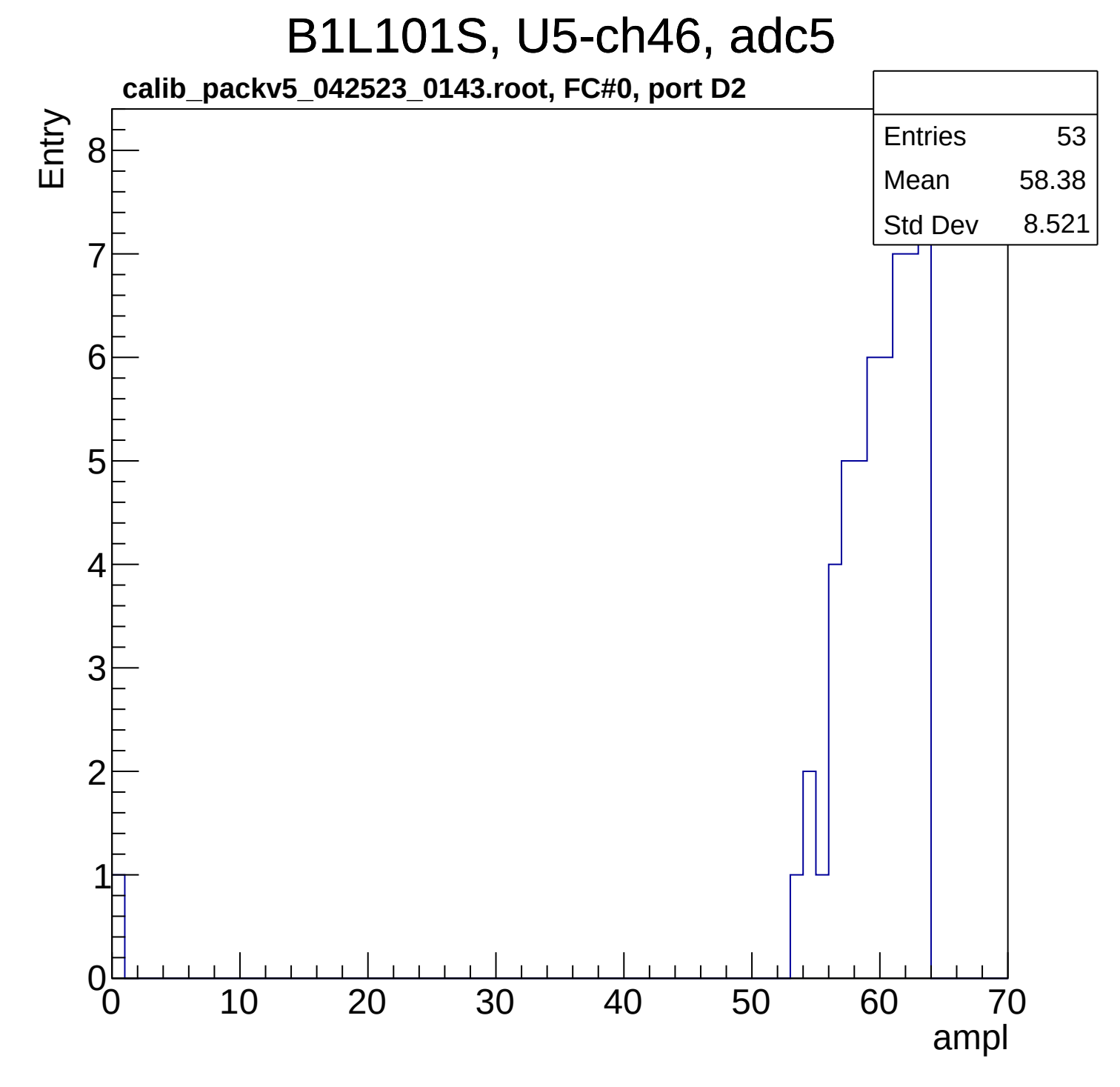
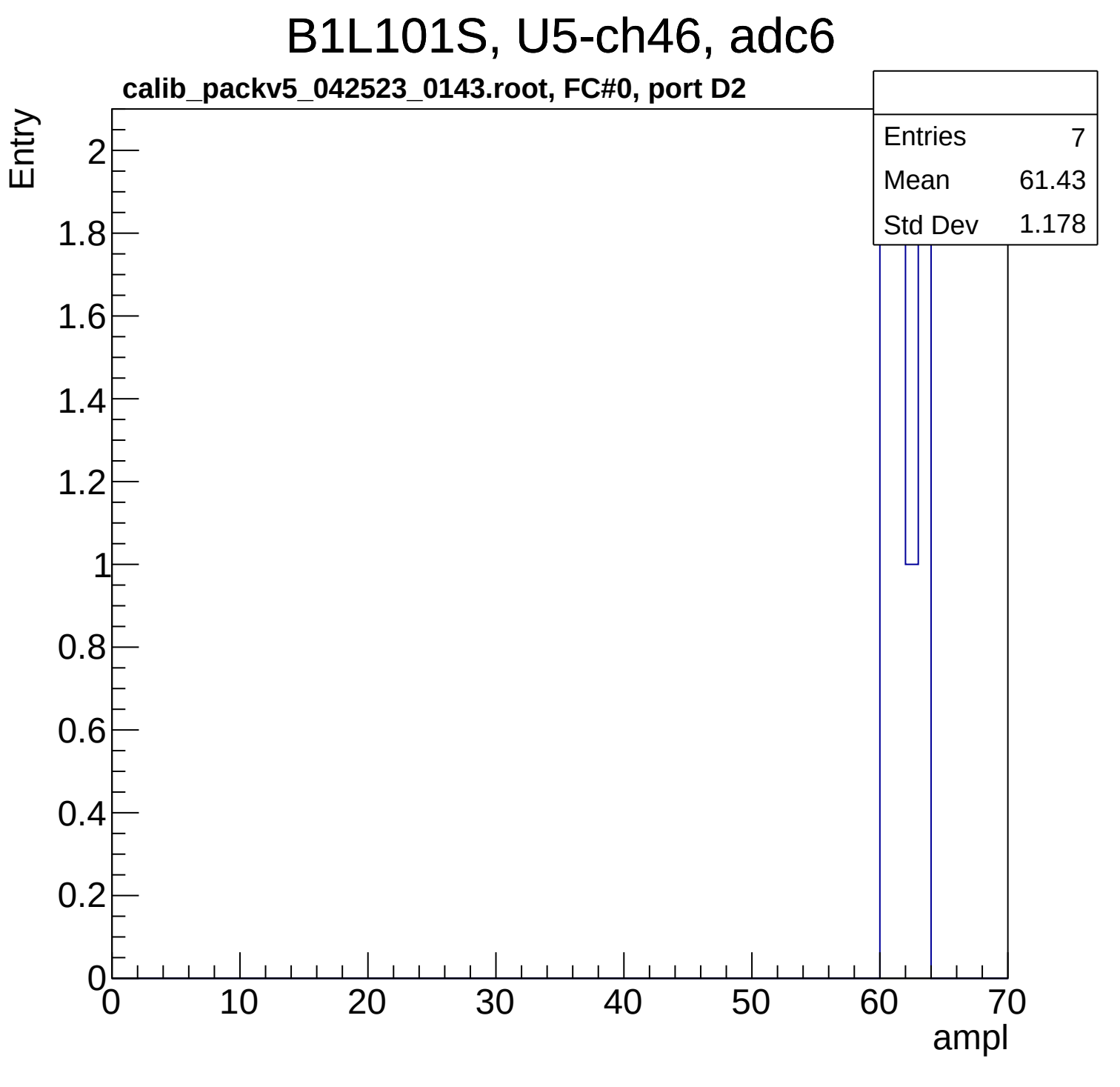
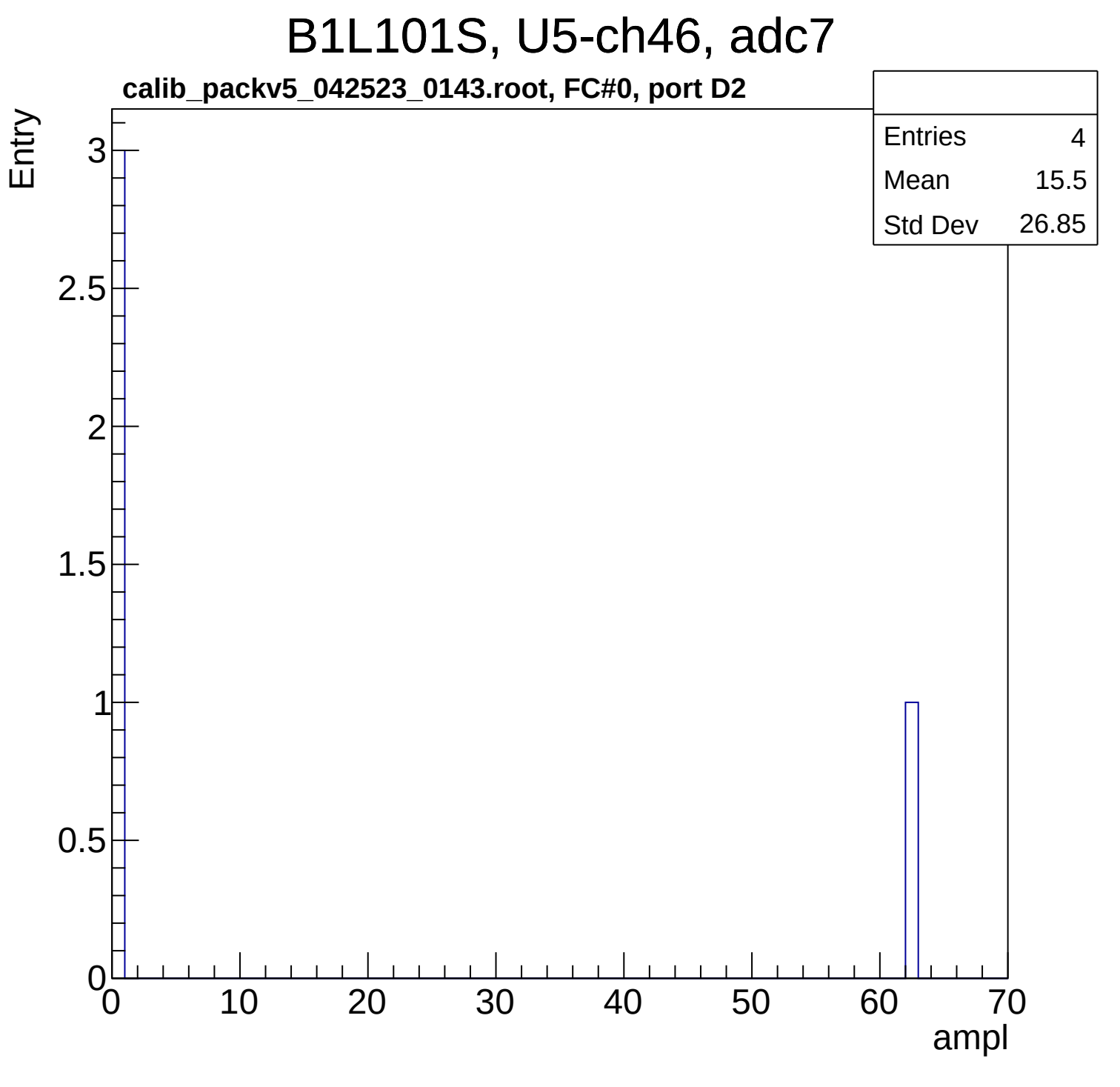

B1L101S, U5-ch46, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 58.38
Std Dev 8.521
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch46, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 61.43
Std Dev 1.178
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U5-ch46, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 15.5
Std Dev 26.85
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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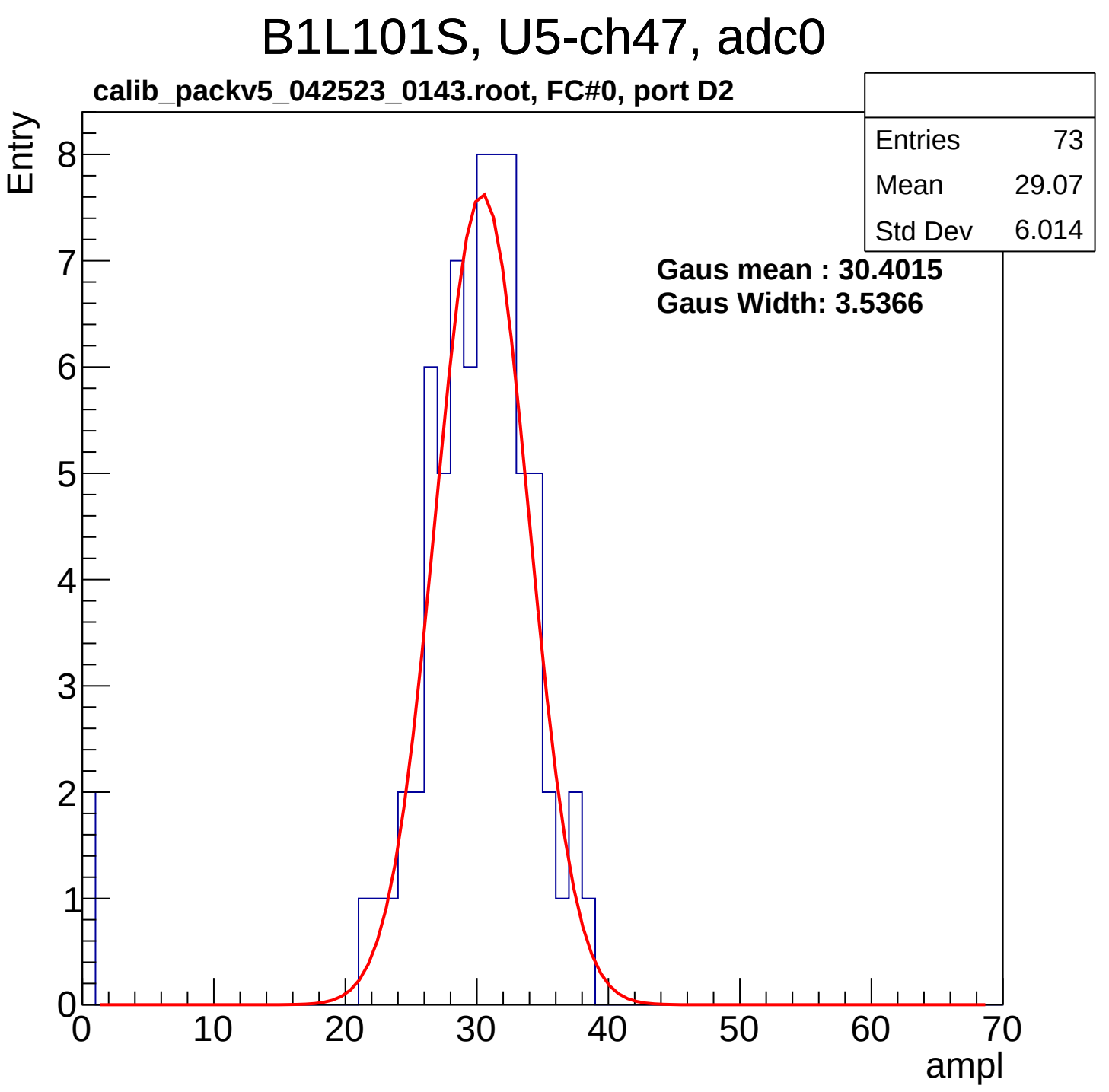
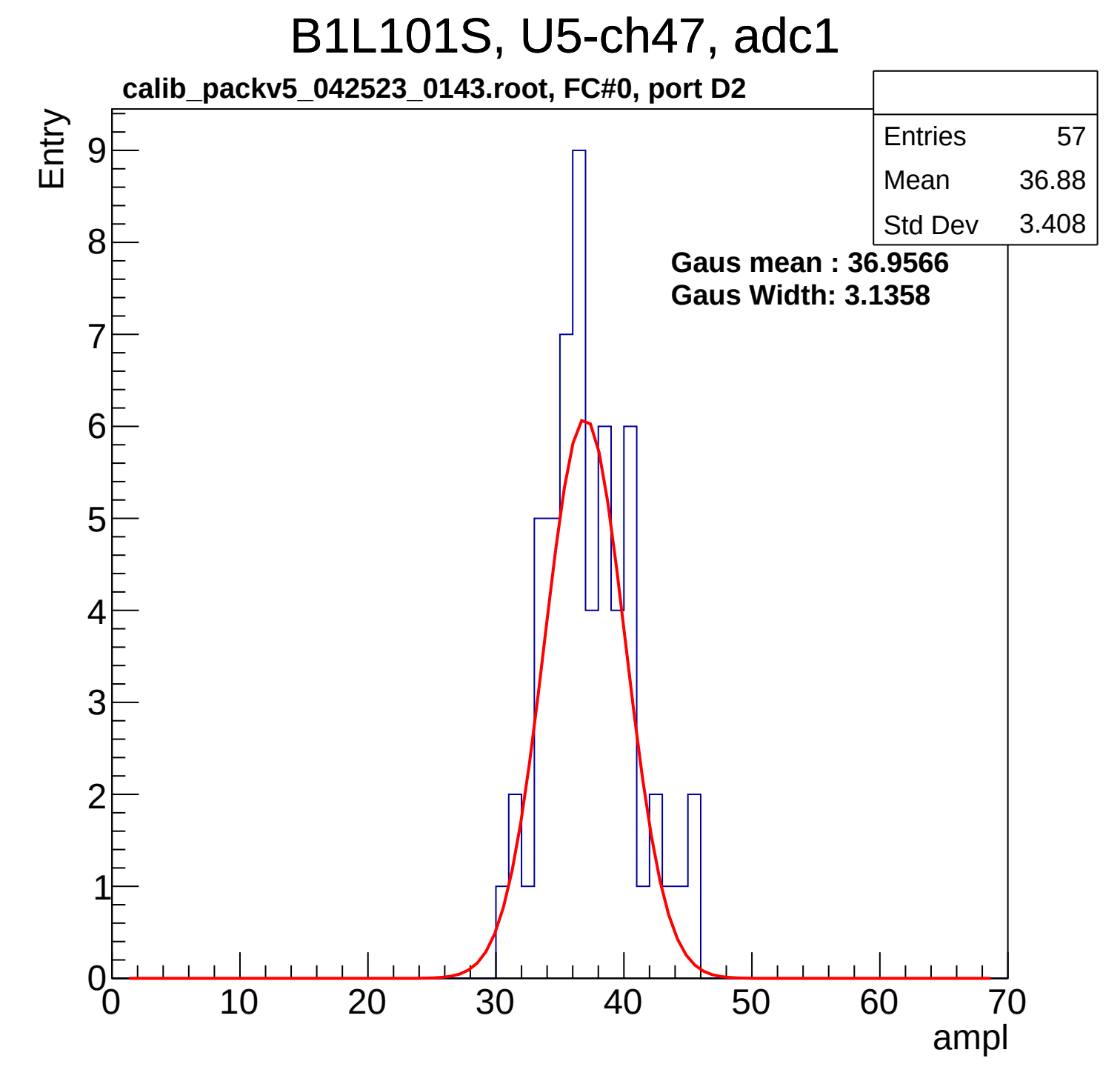
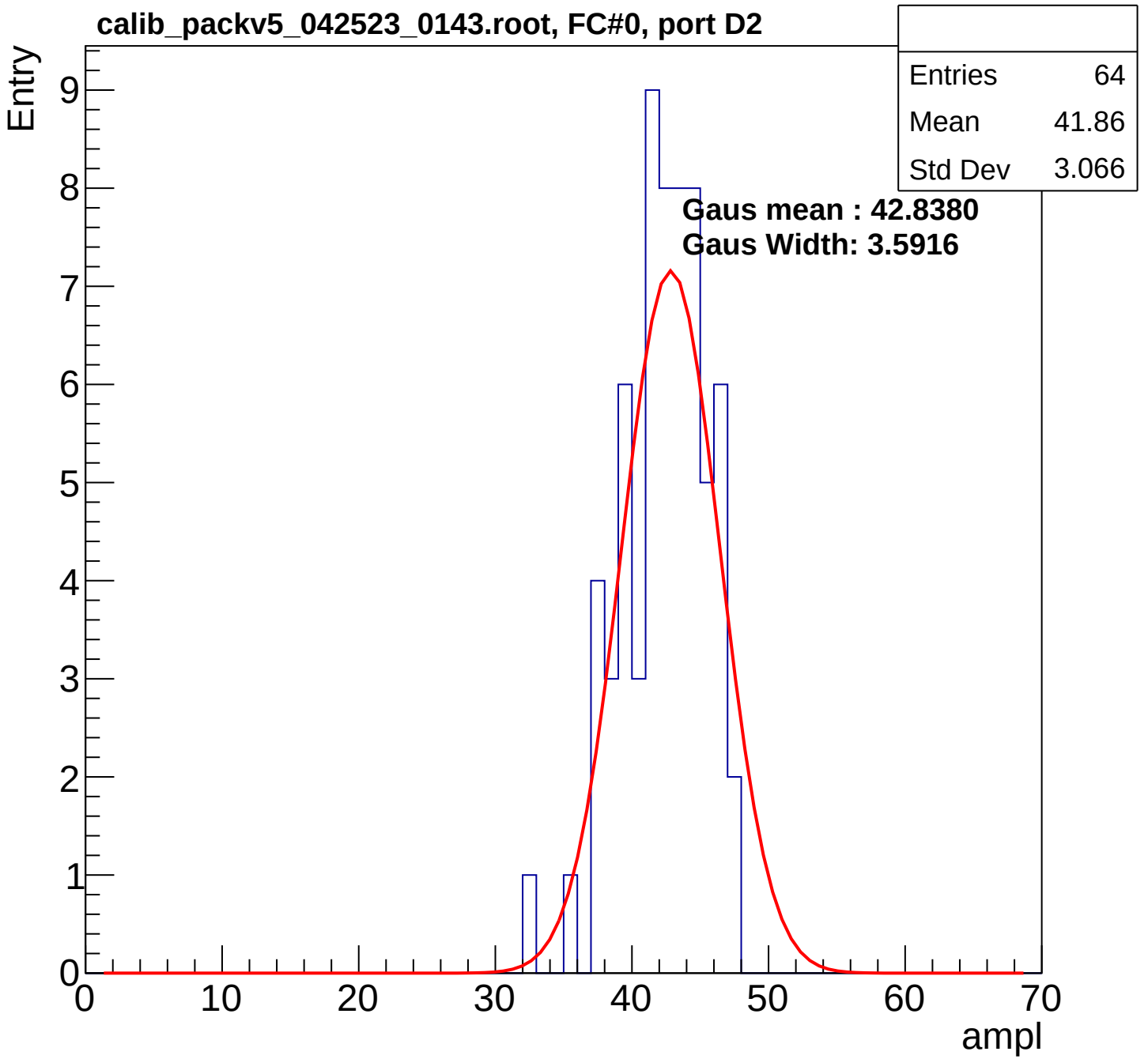
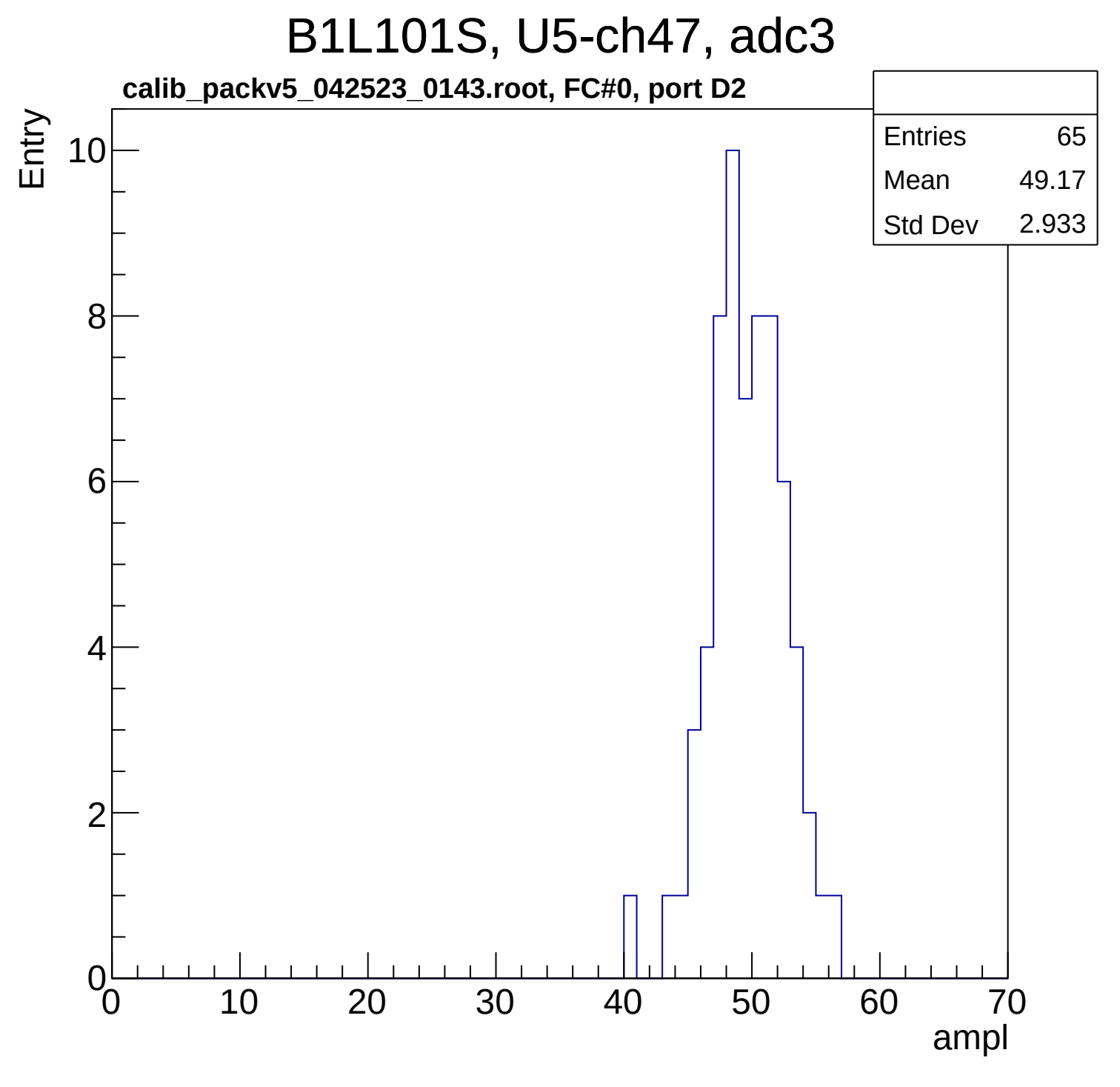
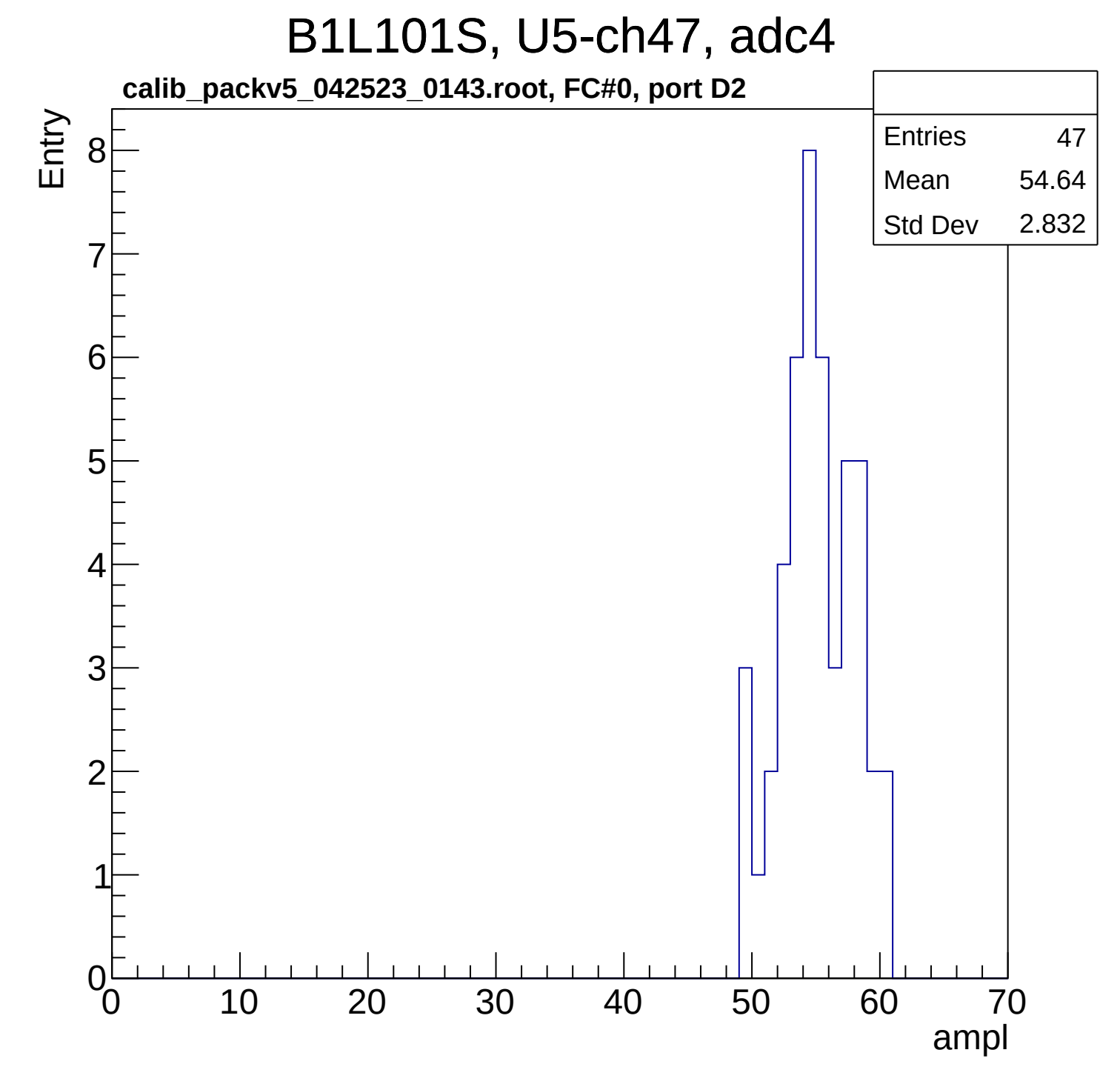
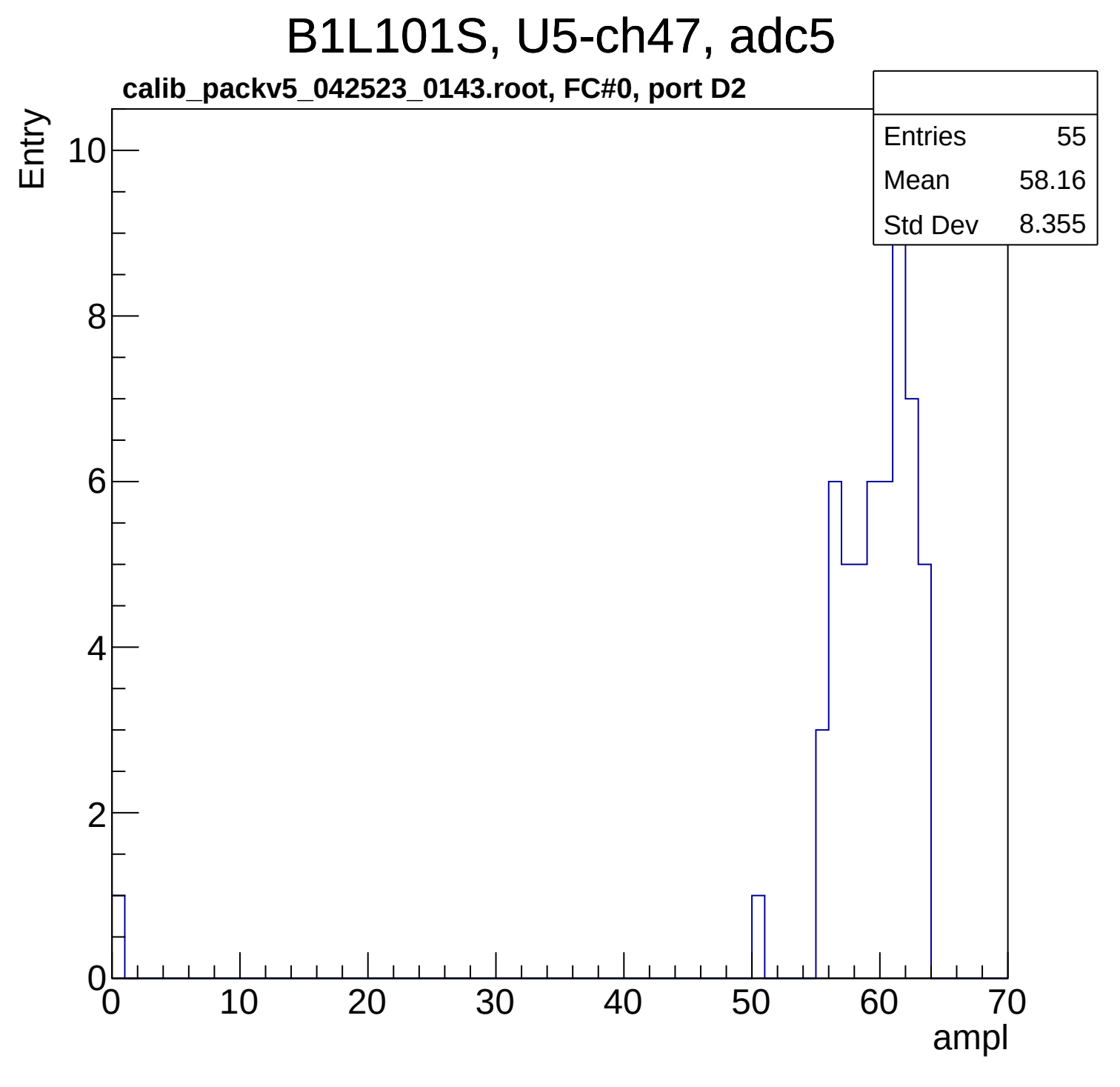

B1L101S, U5-ch47, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 29.07
Std Dev 6.014
Gaus mean : 30.4015
Gaus Width: 3.5366
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

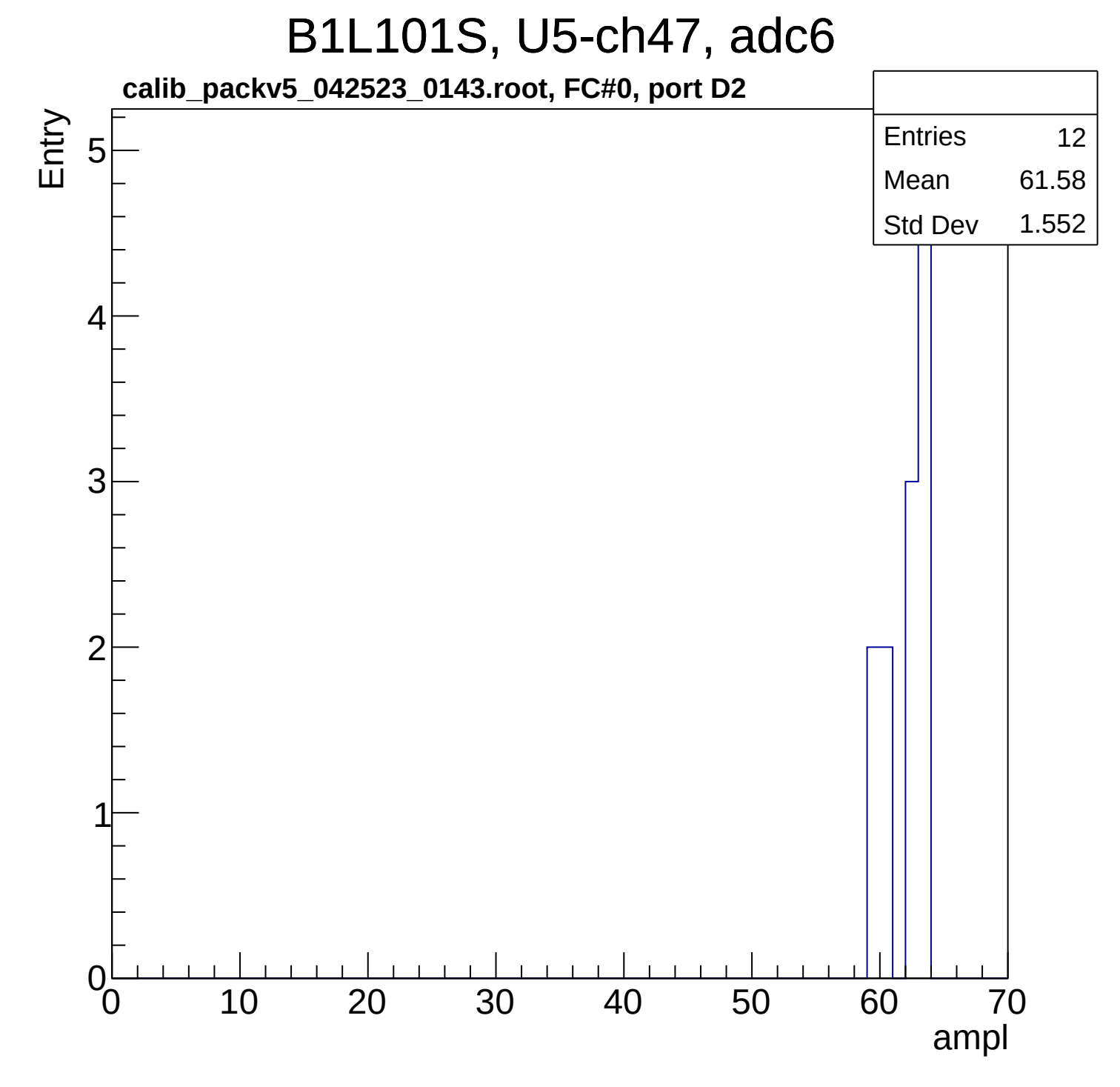

B1L101S, U5-ch47, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 36.88
Std Dev 3.408
Gaus mean : 36.9566
Gaus Width: 3.1358
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

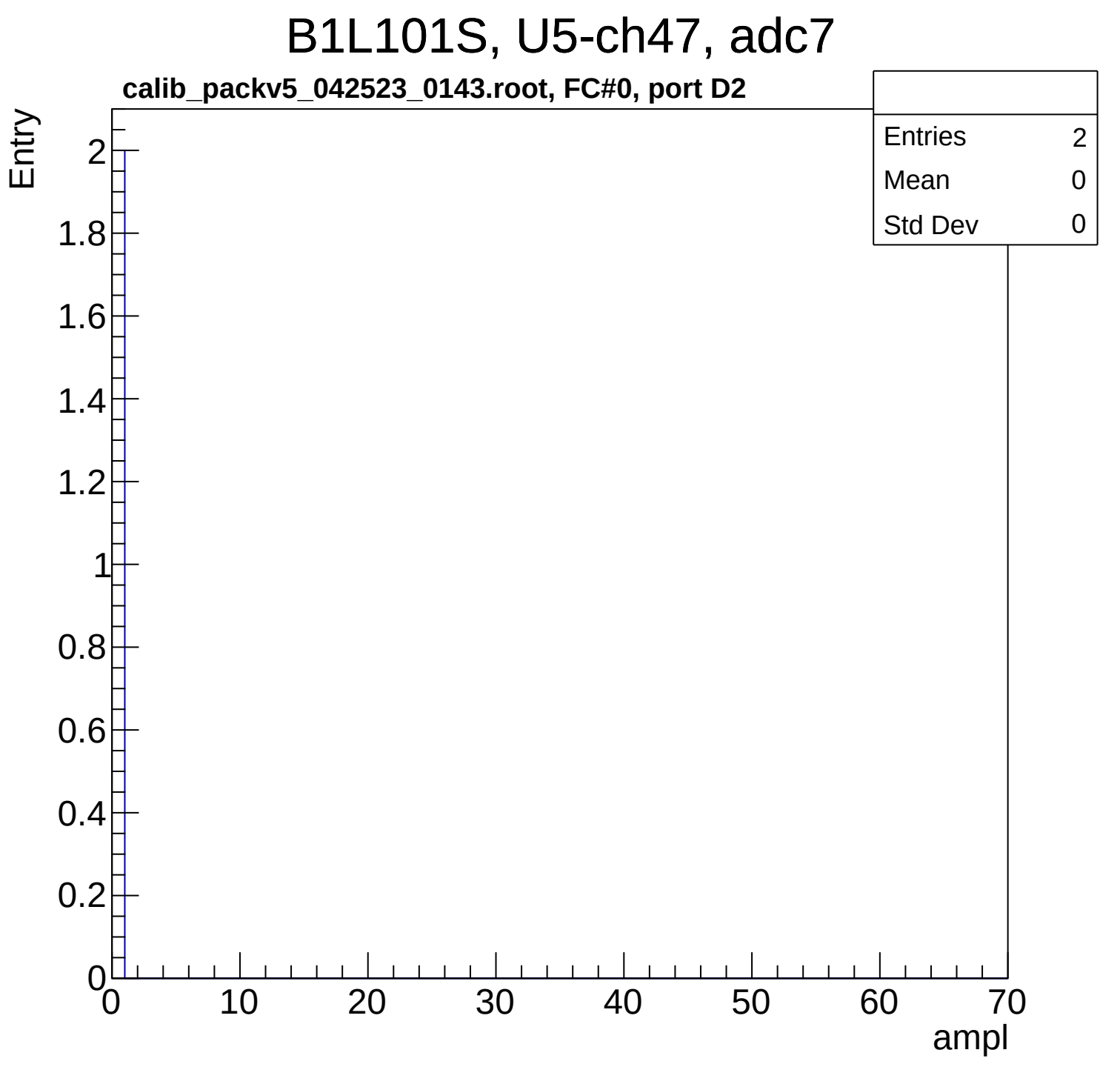

B1L101S, U5-ch47, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 41.86
Std Dev 3.066
Gaus mean : 42.8380
Gaus Width: 3.5916
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

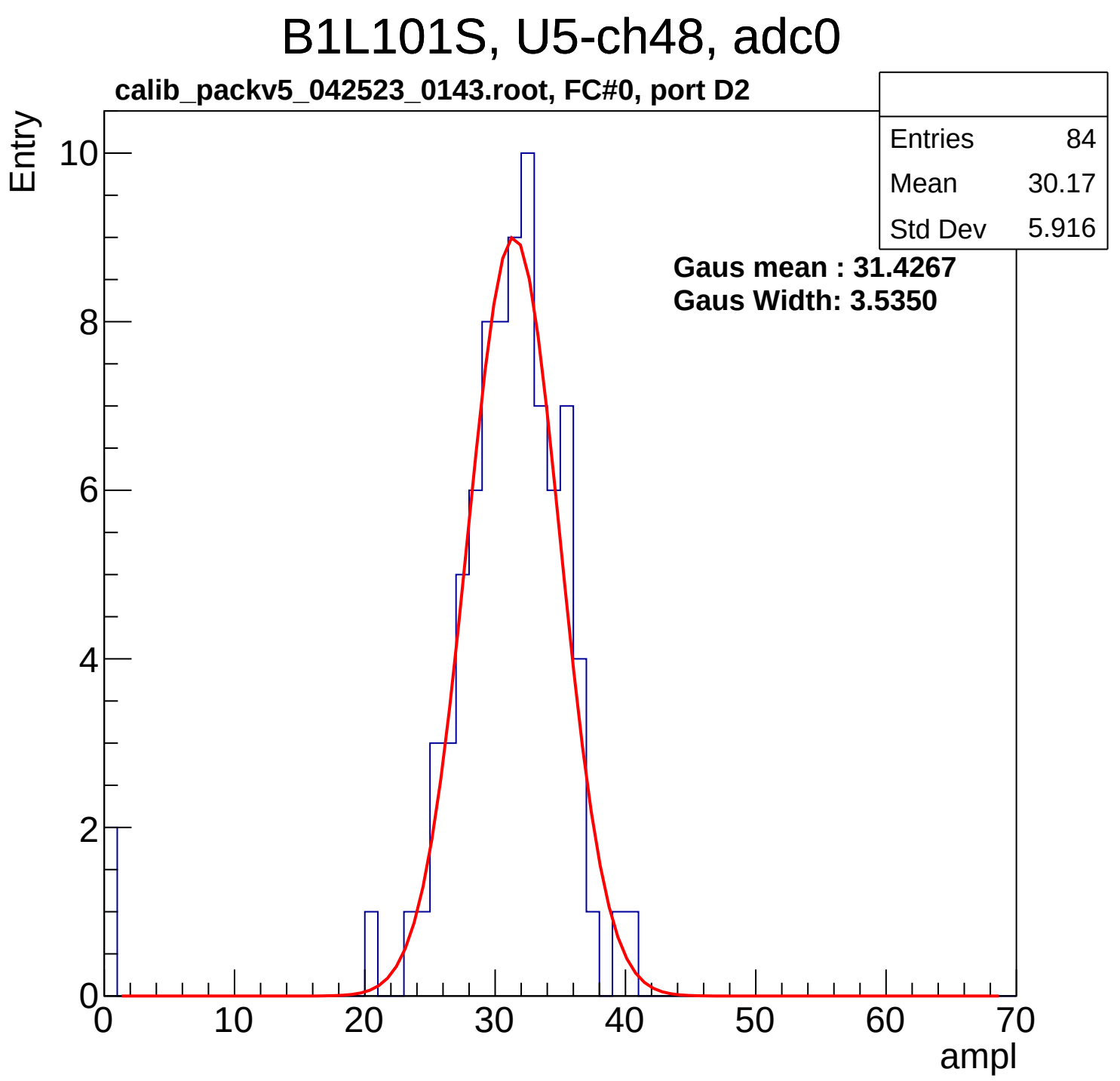

B1L101S, U5-ch47, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 49.17
Std Dev 2.933
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

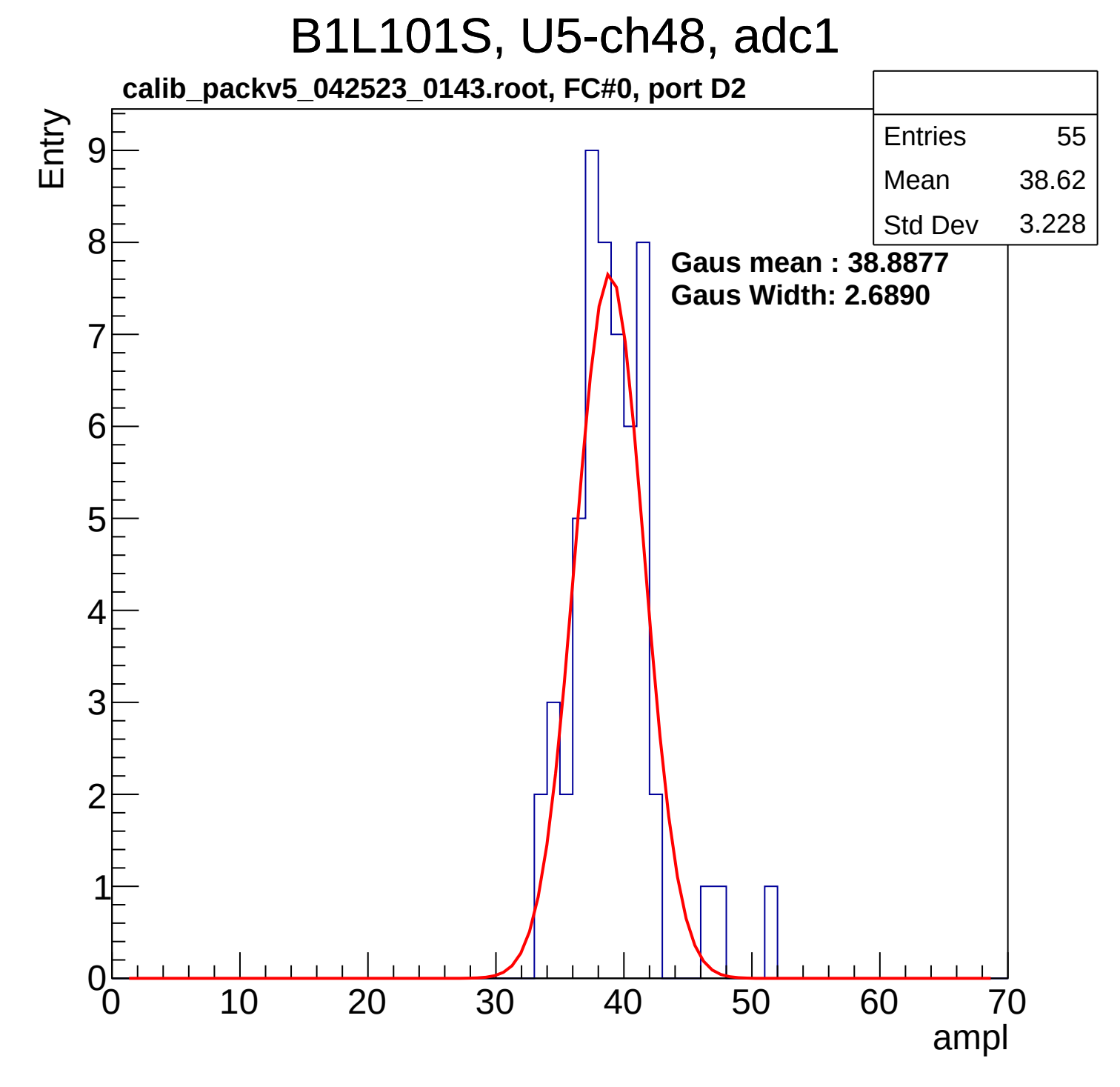

B1L101S, U5-ch47, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 54.64
Std Dev 2.832
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

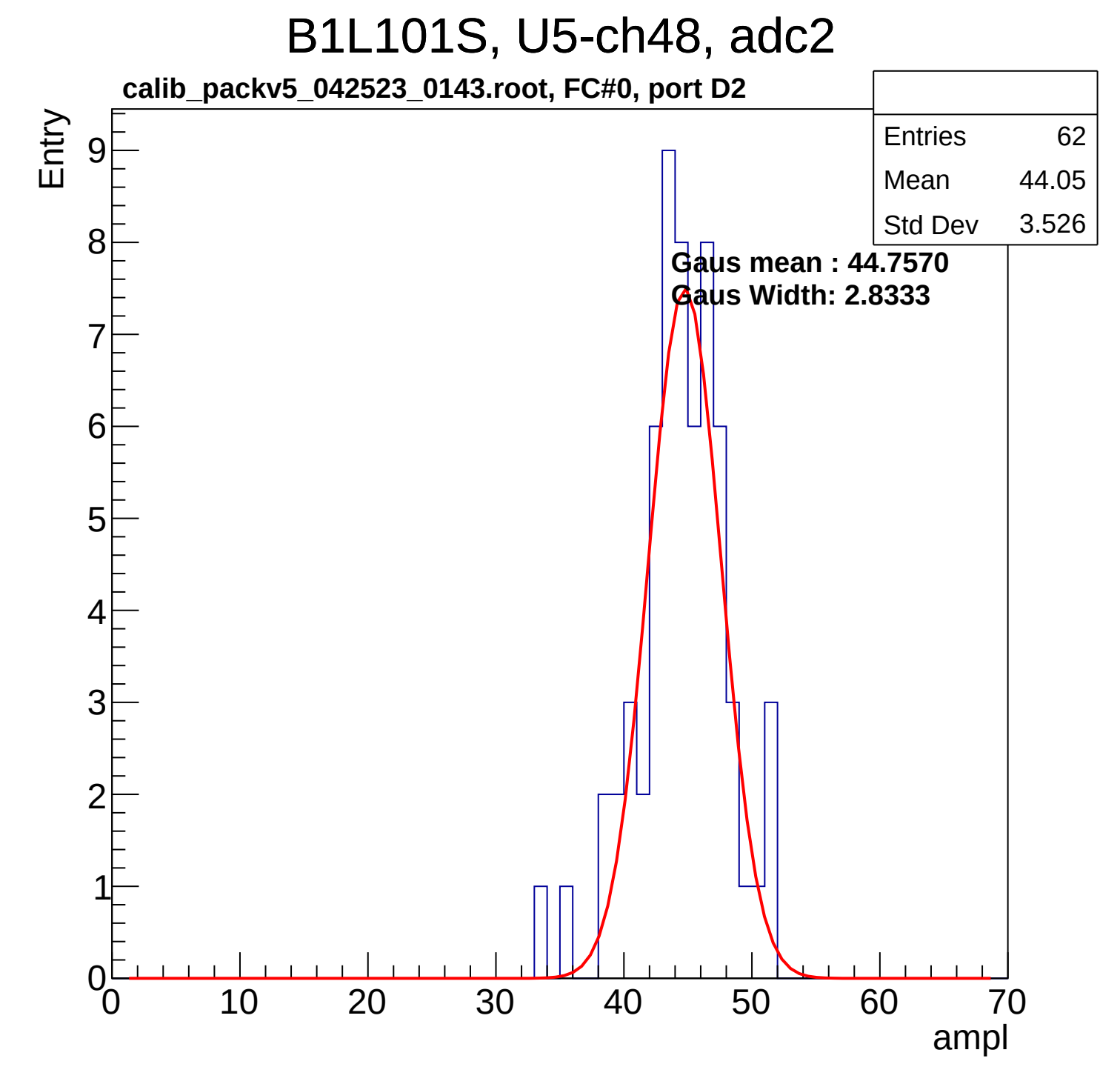

B1L101S, U5-ch47, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 58.16
Std Dev 8.355
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

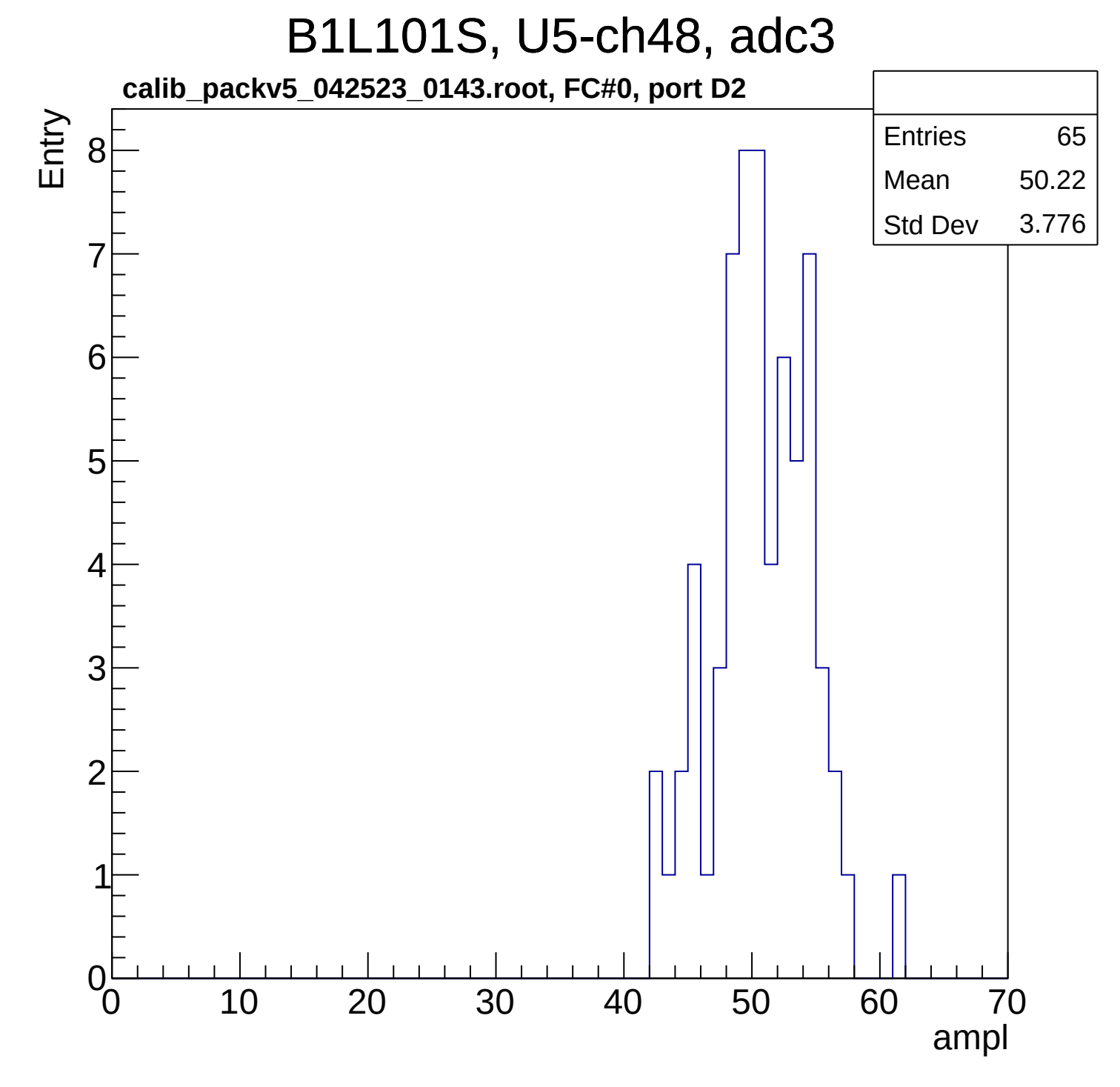

B1L101S, U5-ch47, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 12
Mean 61.58
Std Dev 1.552
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

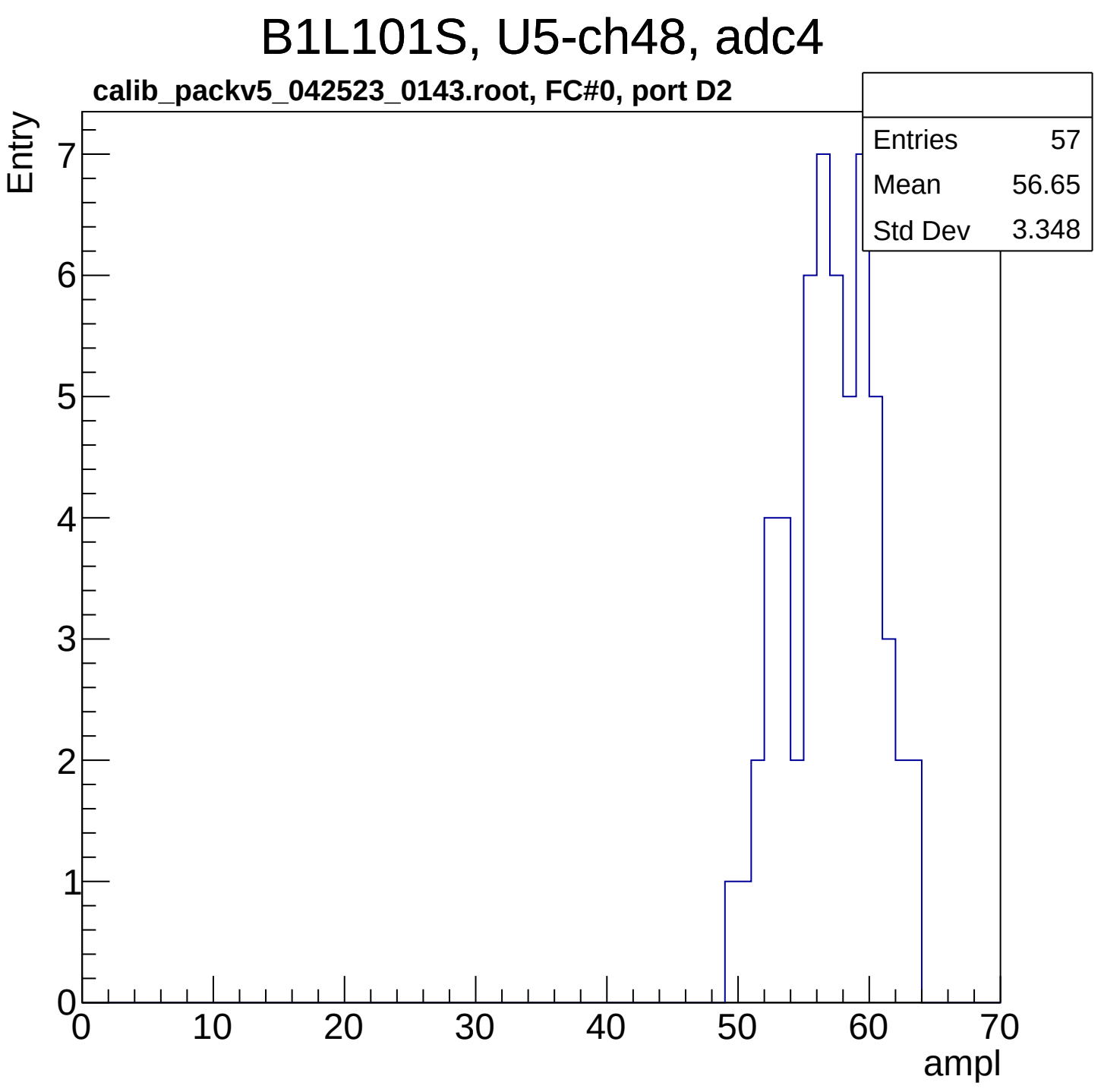

B1L101S, U5-ch47, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

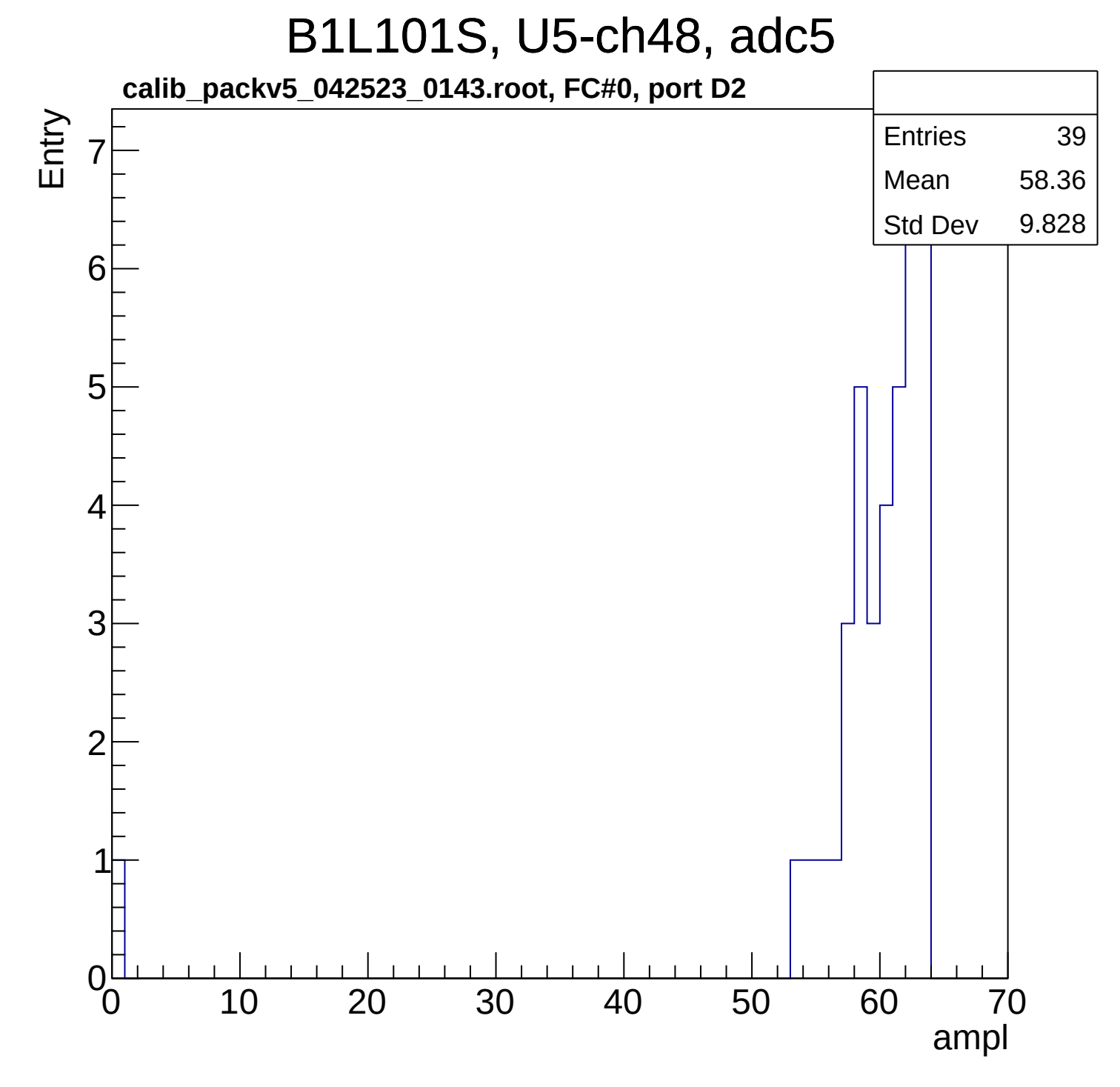

B1L101S, U5-ch48, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 84
Mean 30.17
Std Dev 5.916
Gaus mean : 31.4267
Gaus Width: 3.5350
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

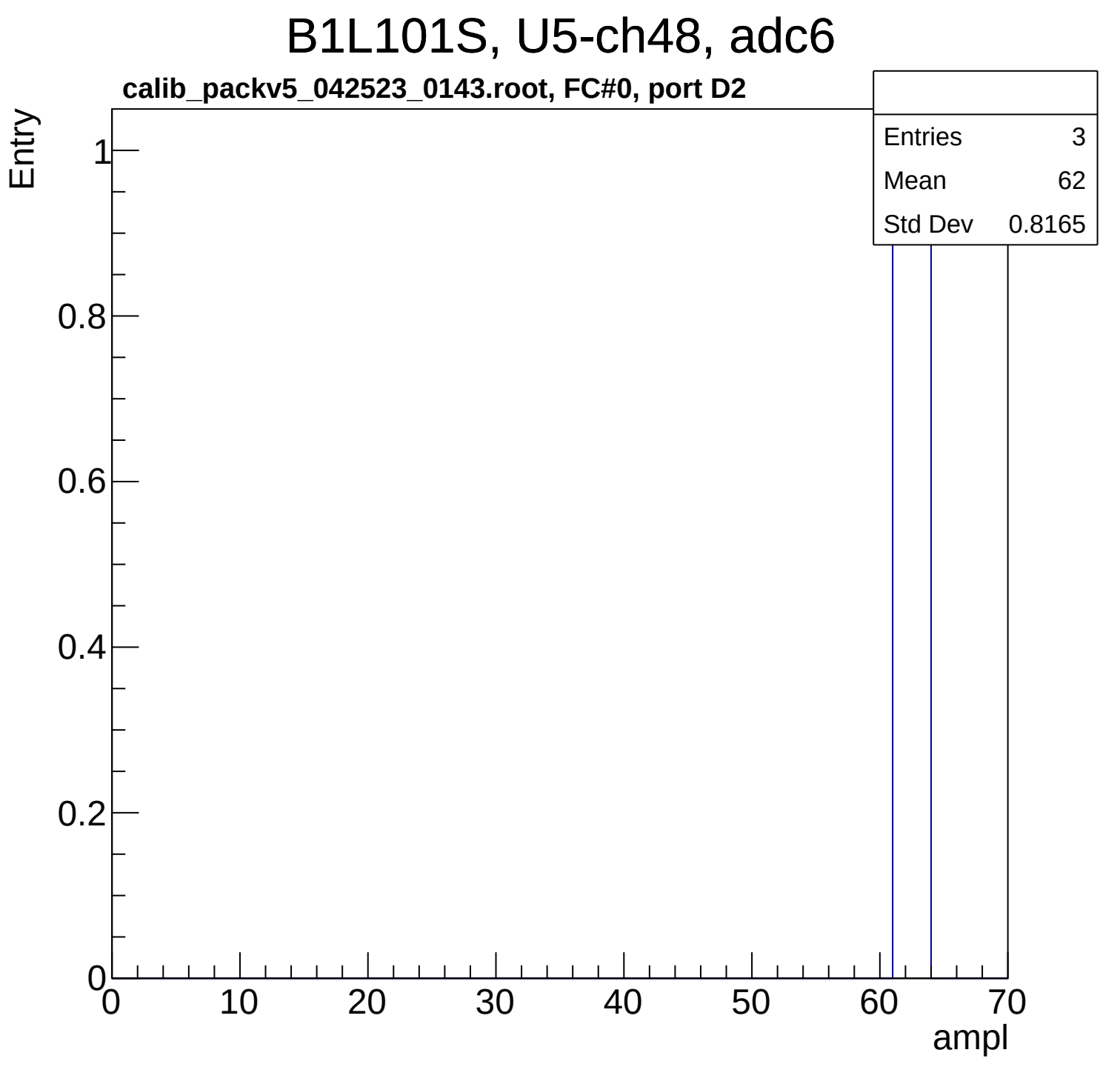

B1L101S, U5-ch48, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 38.62
Std Dev 3.228
Gaus mean : 38.8877
Gaus Width: 2.6890
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

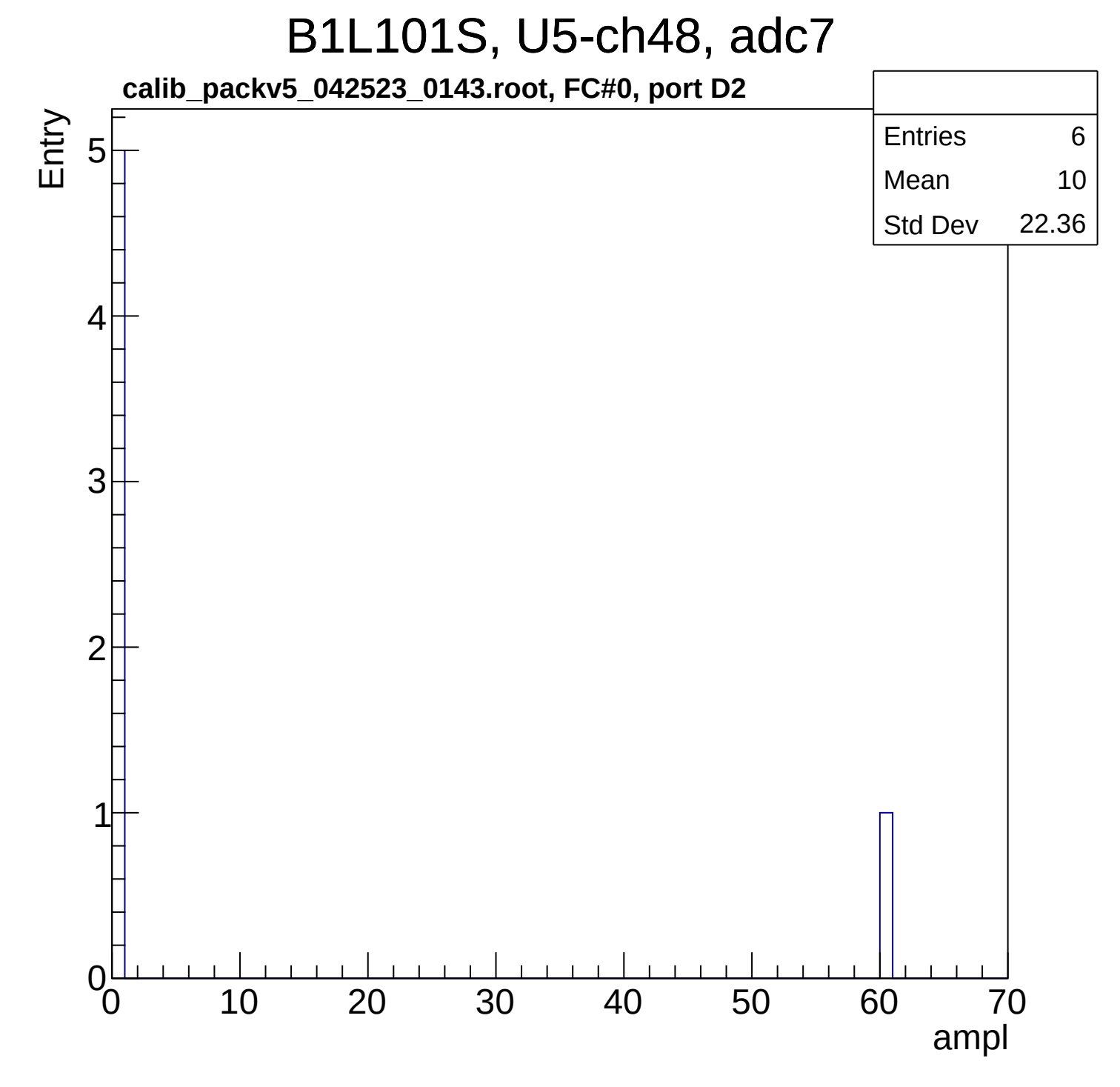

B1L101S, U5-ch48, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 44.05
Std Dev 3.526
Gaus mean : 44.7570
Gaus Width: 2.8333
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

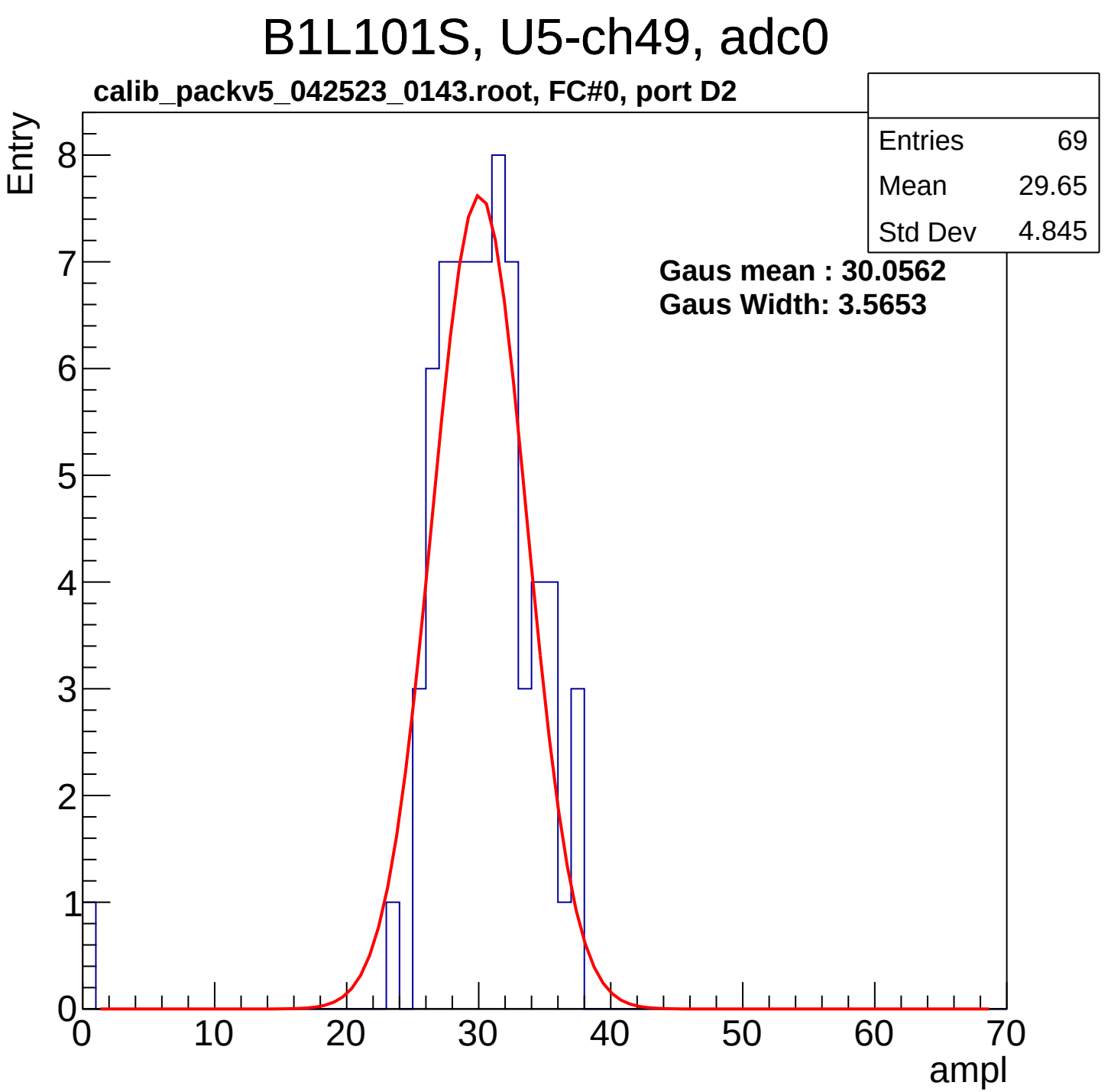

B1L101S, U5-ch48, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 50.22
Std Dev 3.776
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

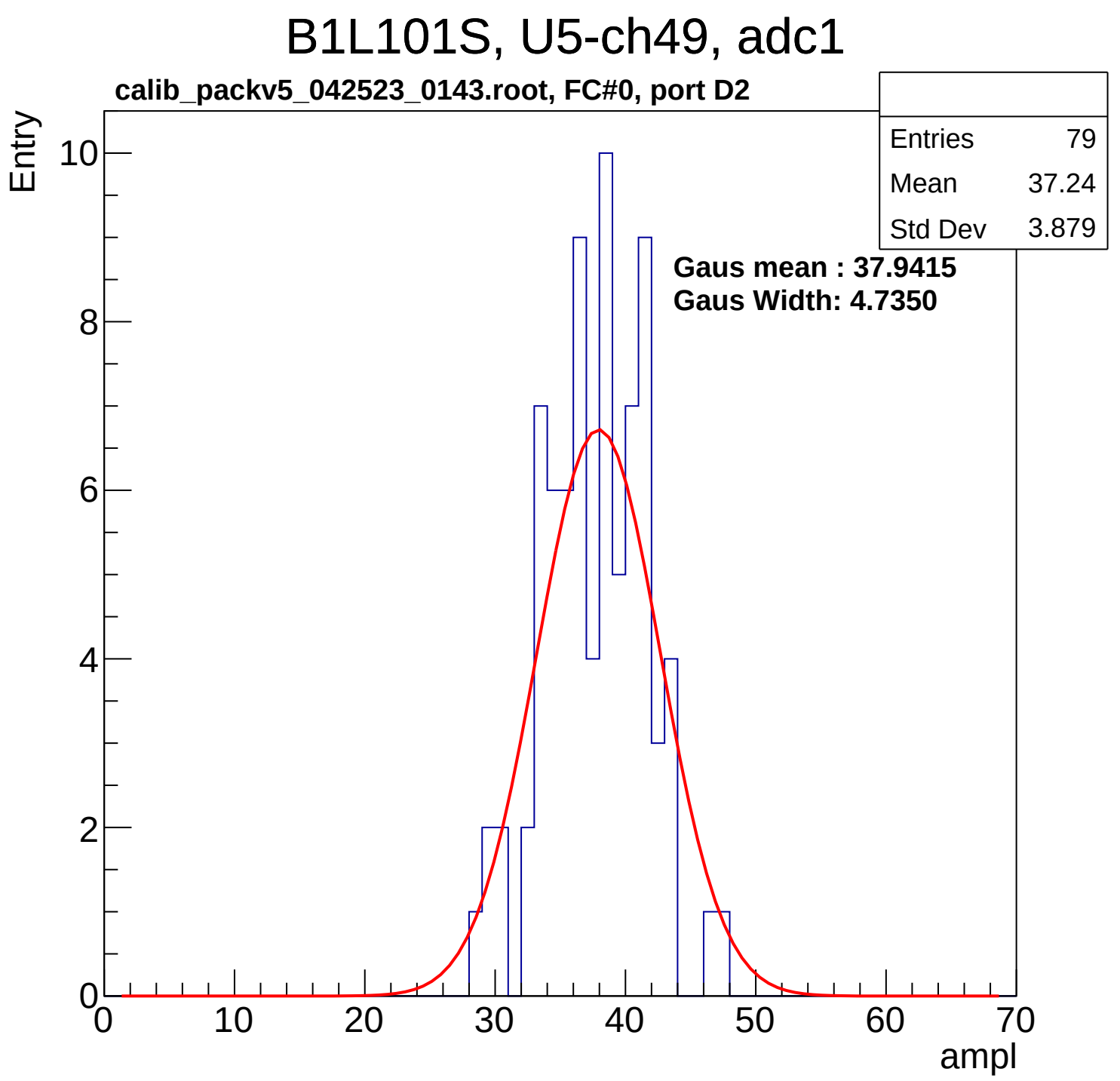

B1L101S, U5-ch48, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 56.65
Std Dev 3.348
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

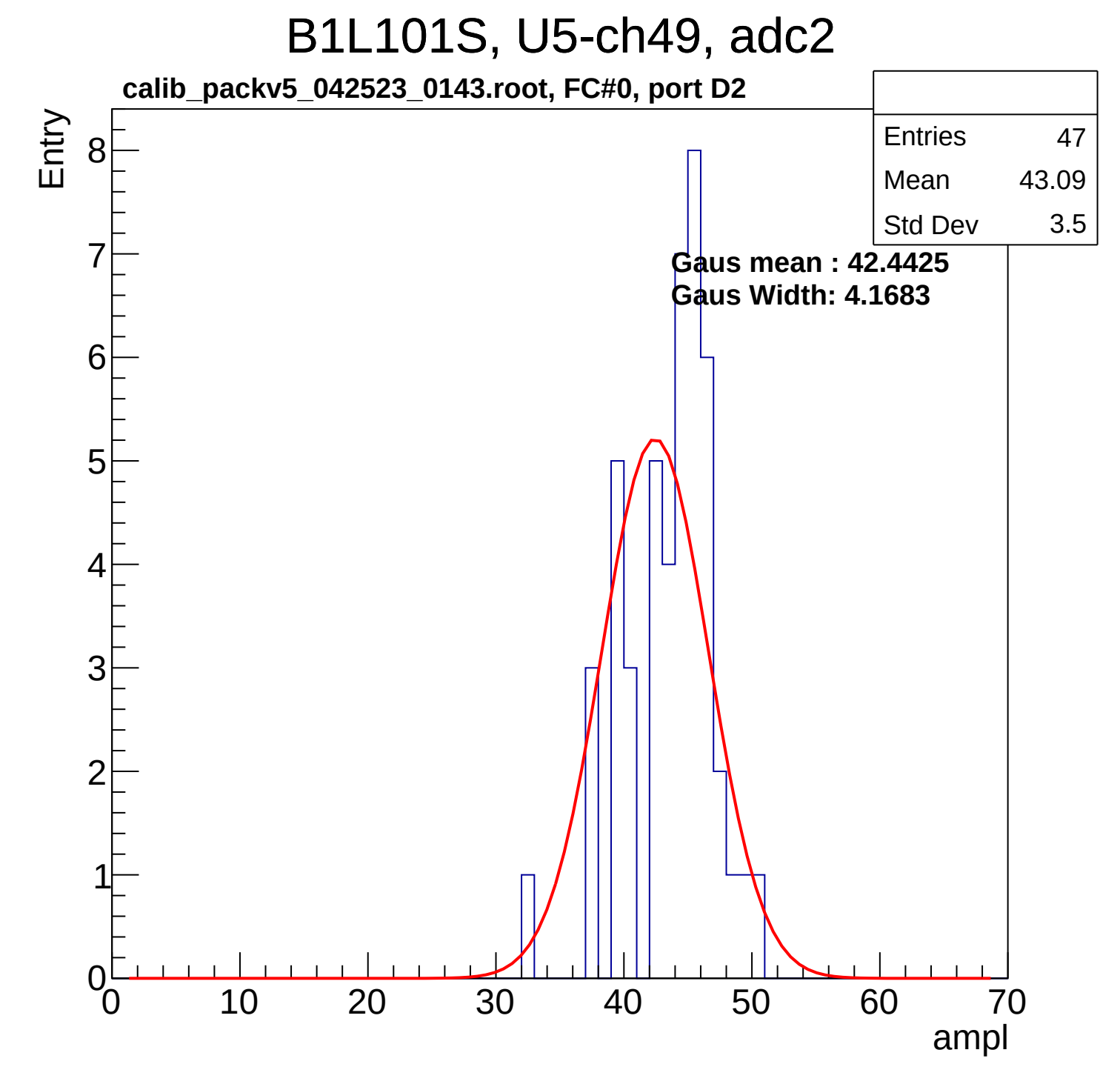

B1L101S, U5-ch48, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 39
Mean 58.36
Std Dev 9.828
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

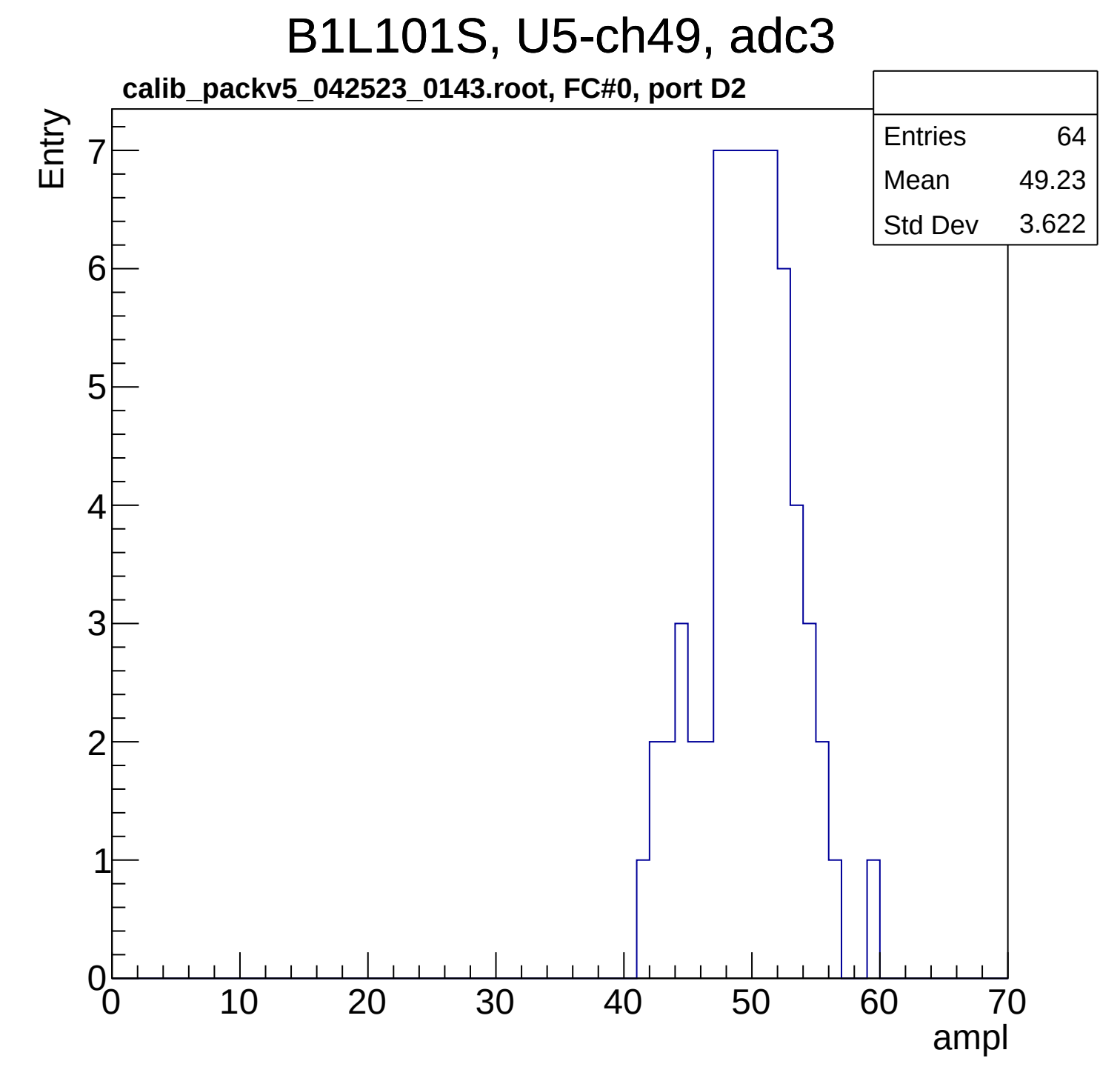

B1L101S, U5-ch48, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 62
Std Dev 0.8165
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

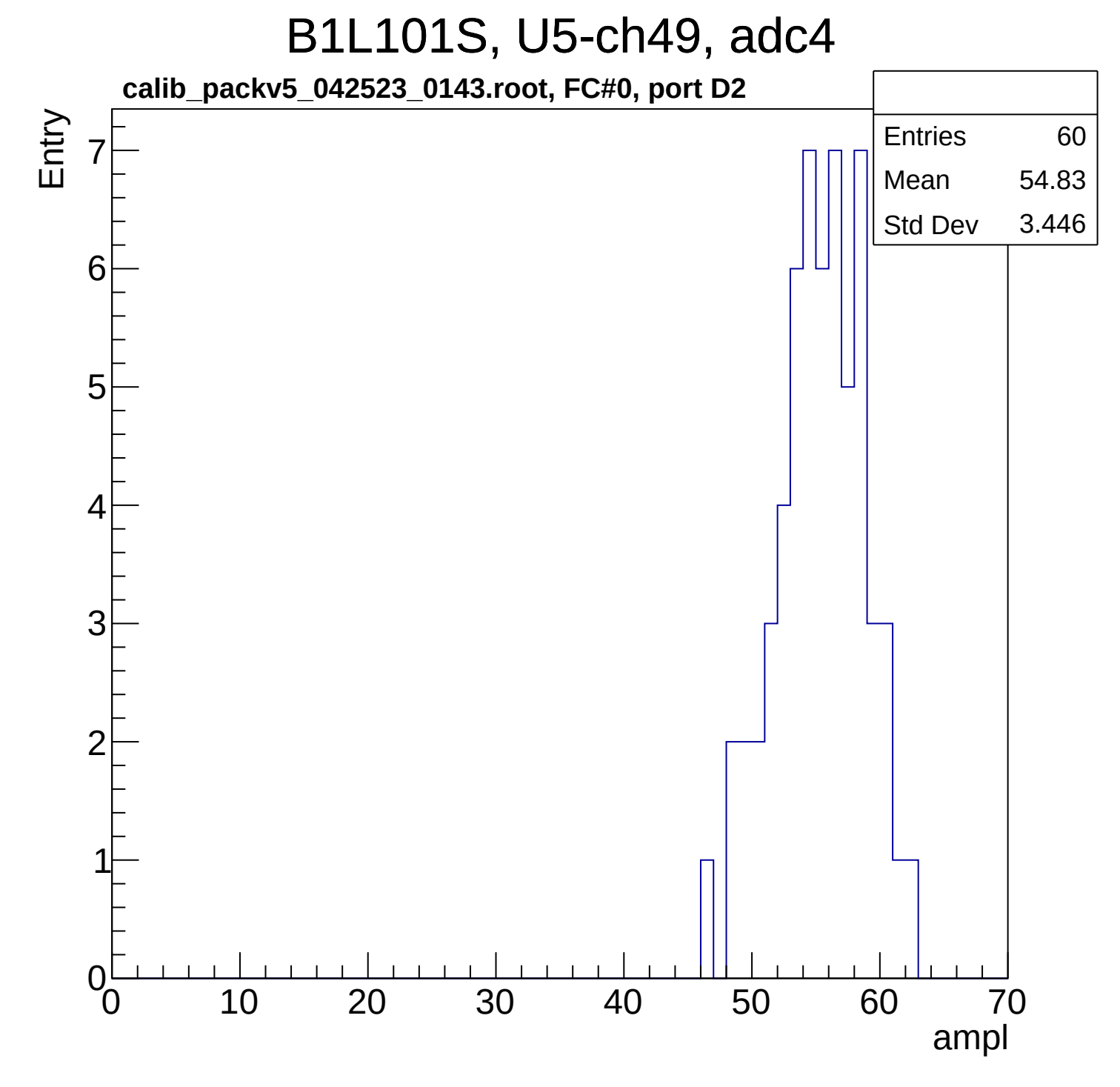

B1L101S, U5-ch48, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 10
Std Dev 22.36
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

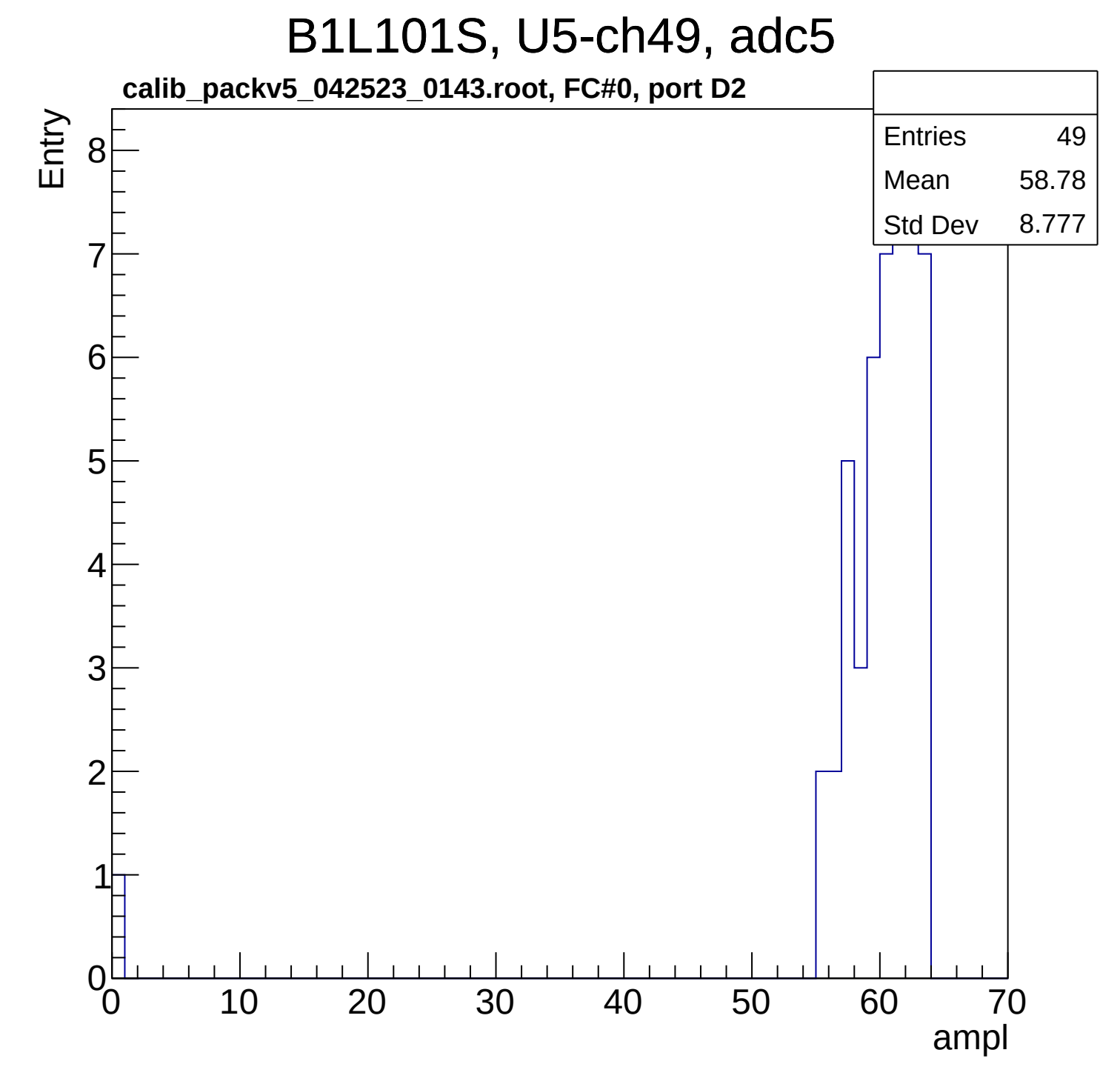

B1L101S, U5-ch49, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 29.65
Std Dev 4.845
Gaus mean : 30.0562
Gaus Width: 3.5653
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

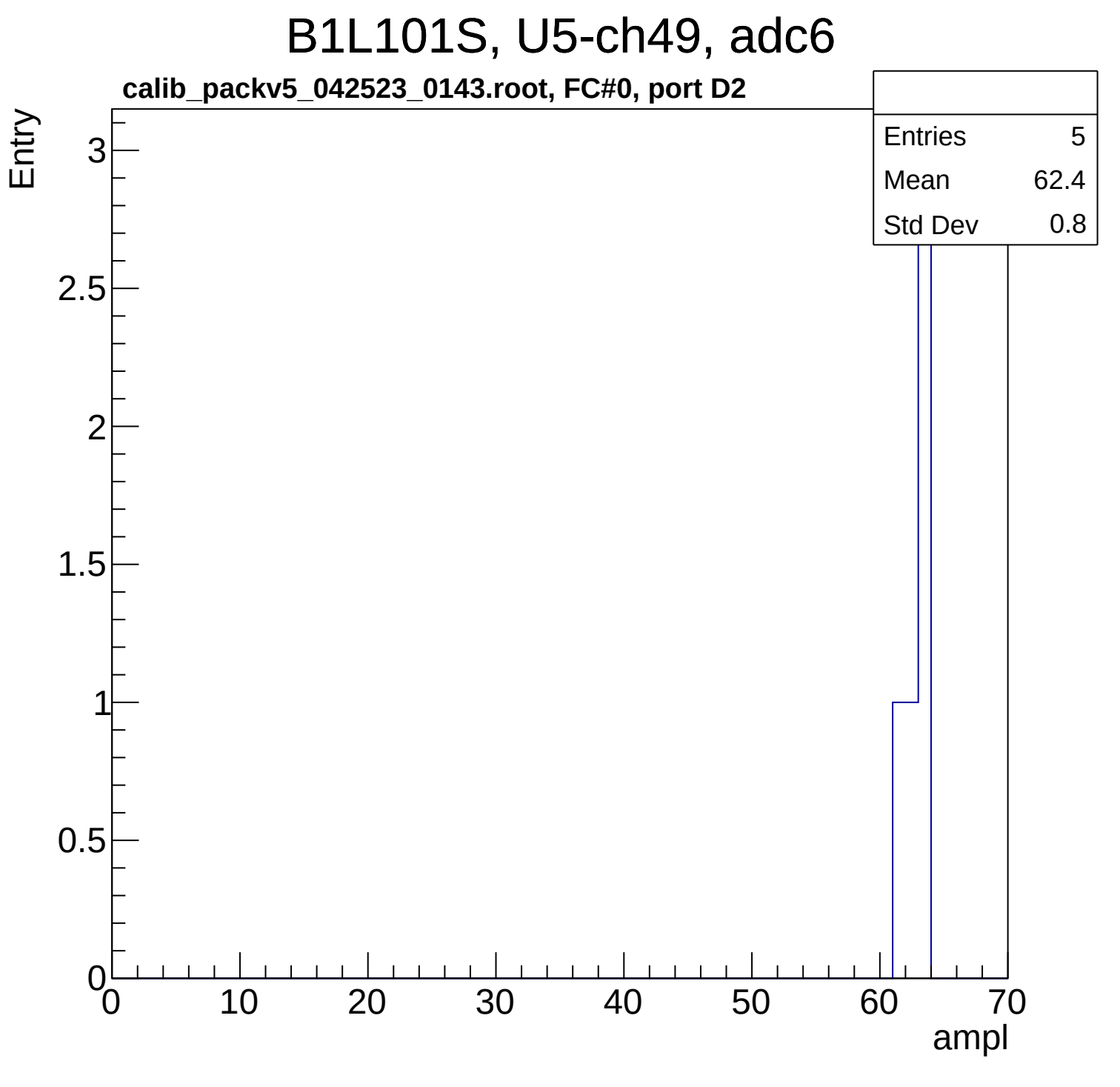

B1L101S, U5-ch49, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 37.24
Std Dev 3.879
Gaus mean : 37.9415
Gaus Width: 4.7350
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

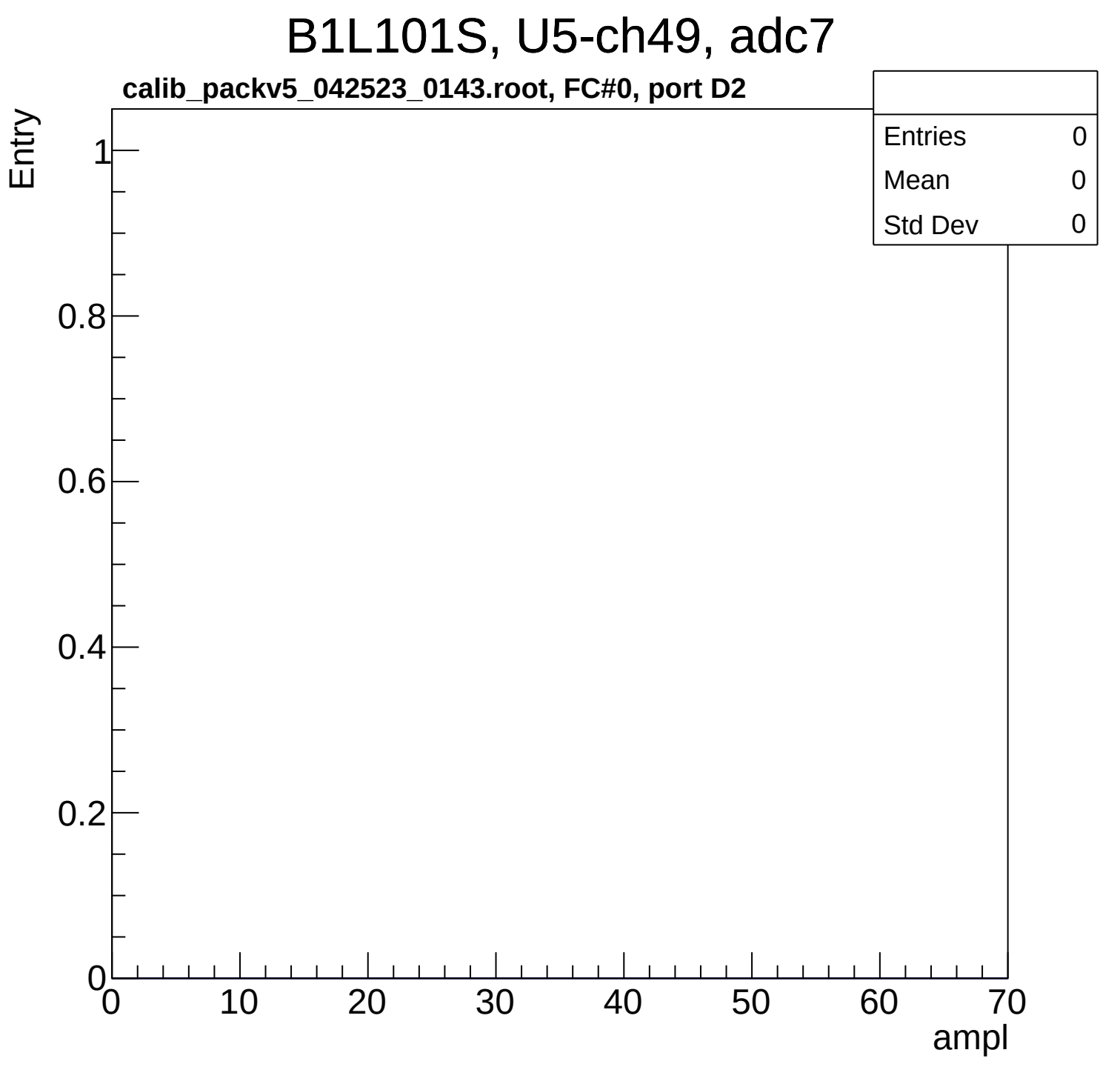

B1L101S, U5-ch49, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 43.09
Std Dev 3.5
Gaus mean : 42.4425
Gaus Width: 4.1683
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

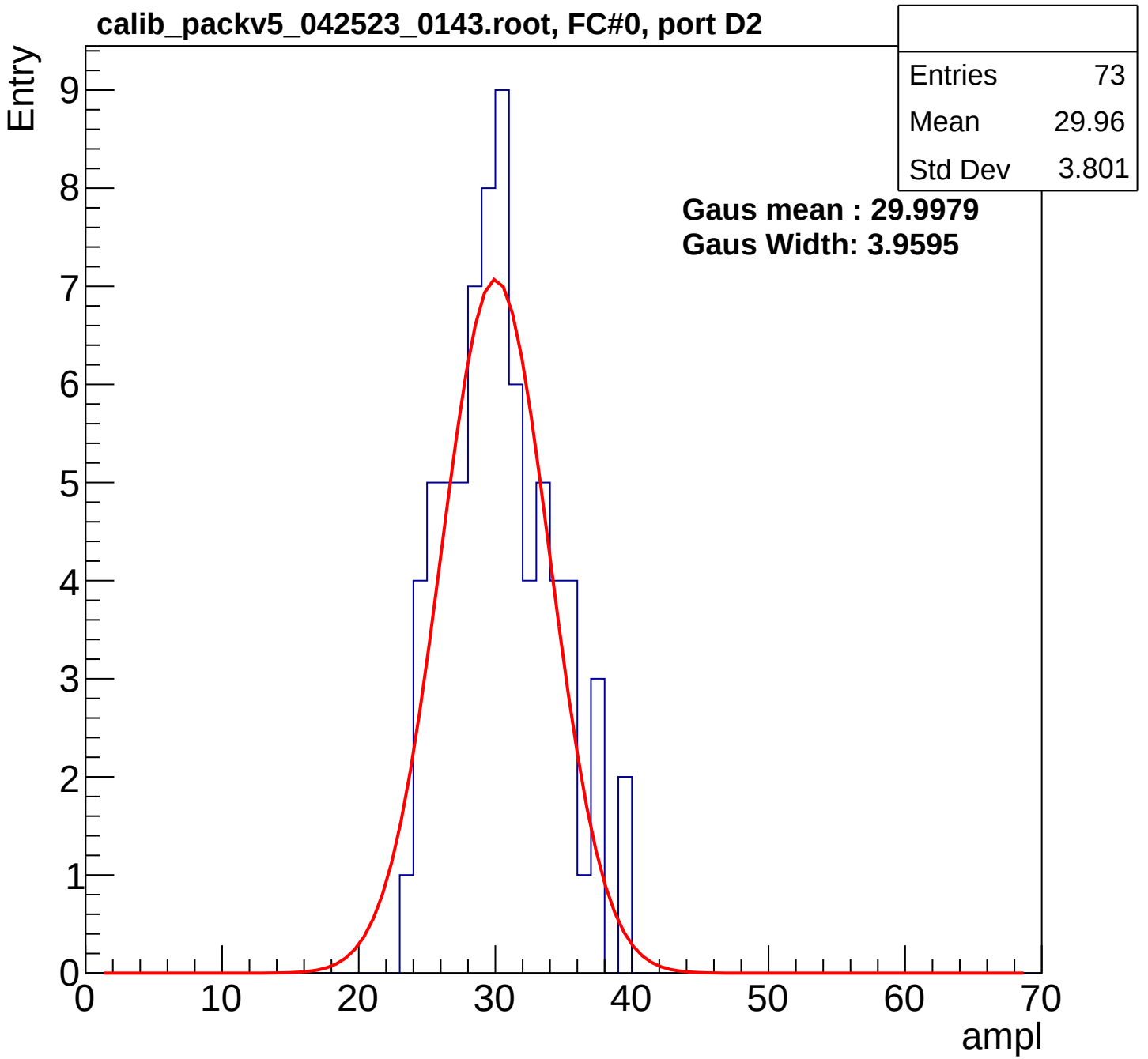

B1L101S, U5-ch49, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 49.23
Std Dev 3.622
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch49, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 54.83
Std Dev 3.446
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch49, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 58.78
Std Dev 8.777
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch49, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 62.4
Std Dev 0.8
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U5-ch49, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch50, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 29.96
Std Dev 3.801
Gaus mean : 29.9979
Gaus Width: 3.9595
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
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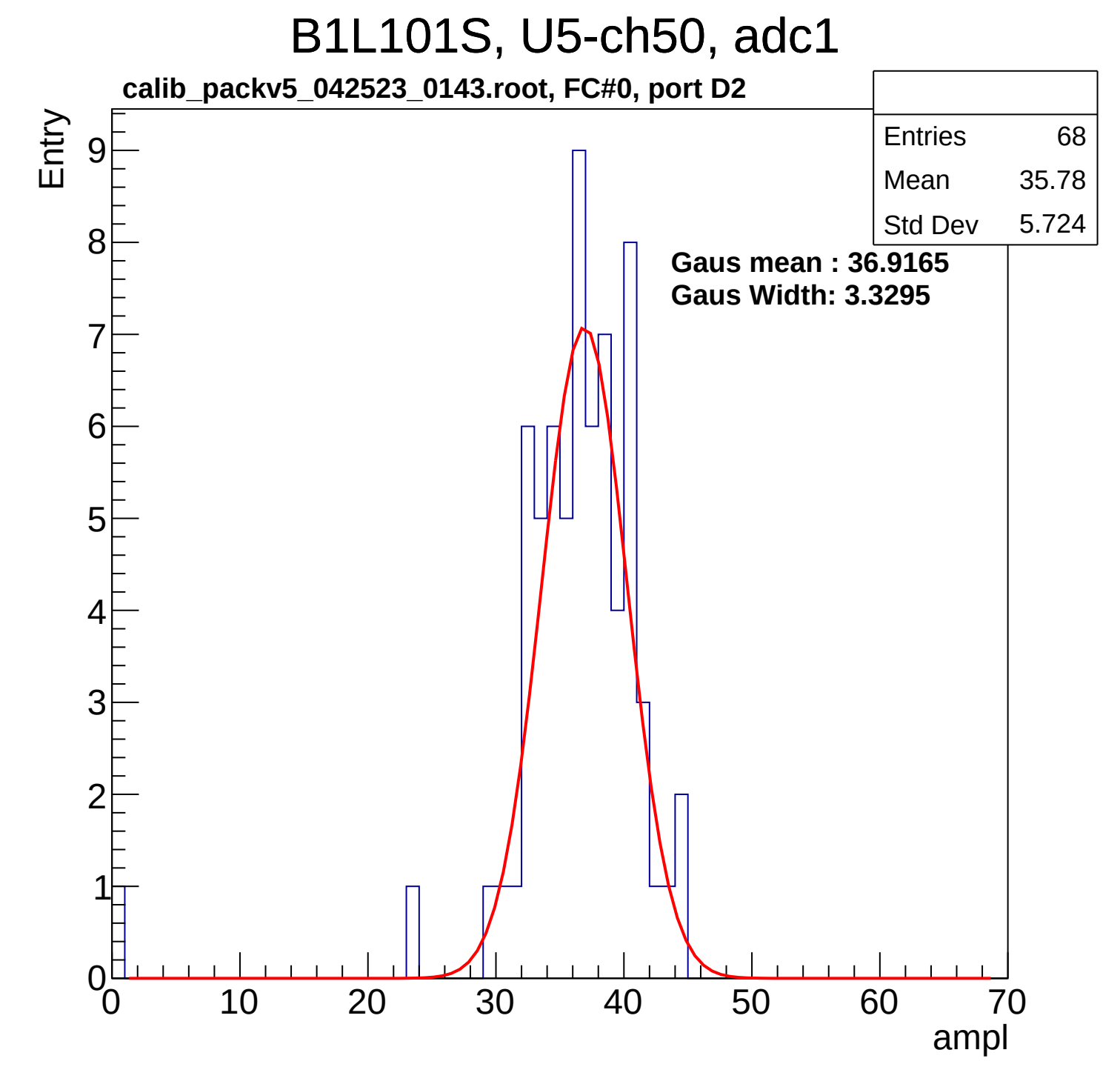
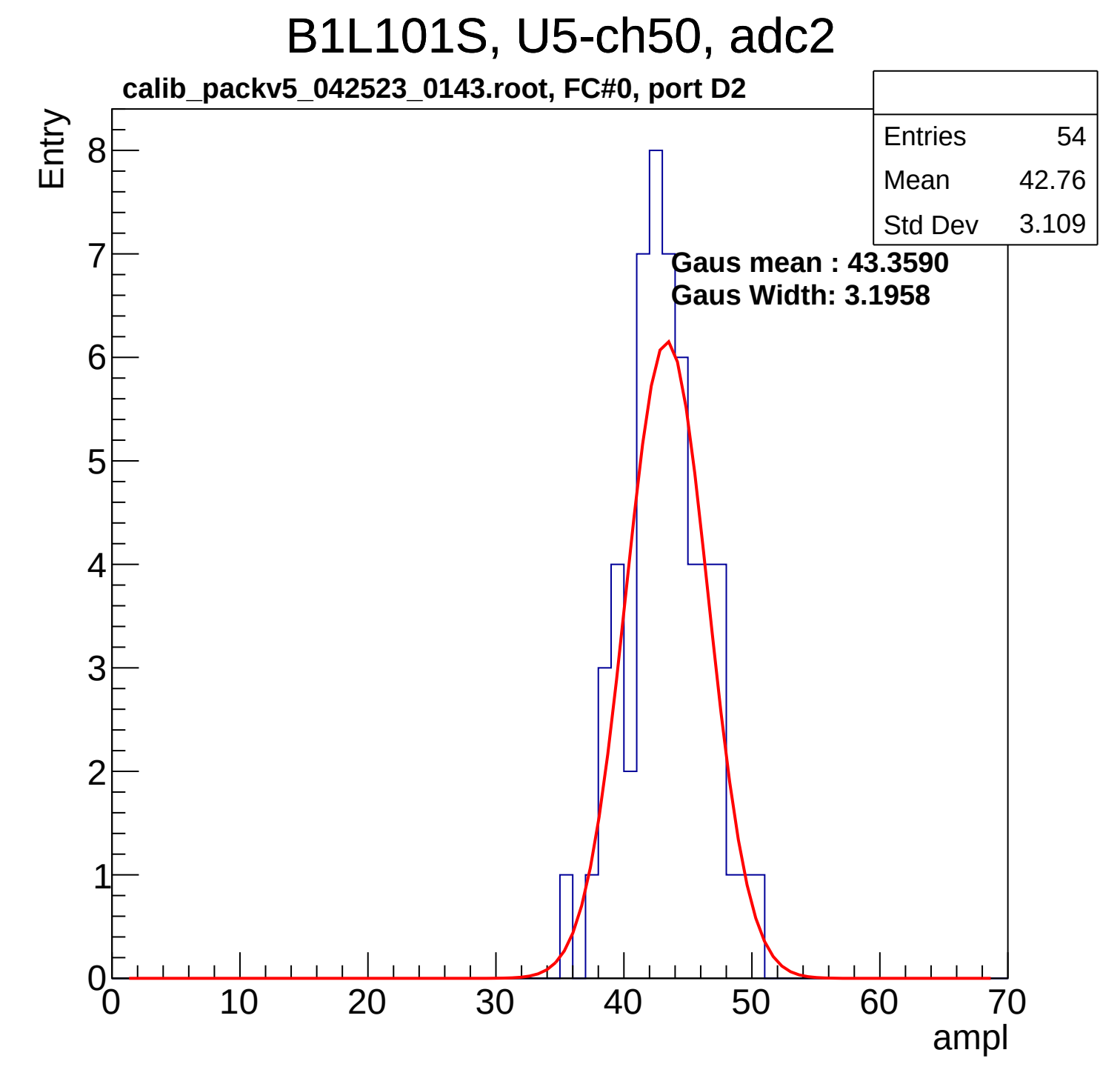
6
7
8
9


B1L101S, U5-ch50, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 35.78
Std Dev 5.724
Gaus mean : 36.9165
Gaus Width: 3.3295
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L101S, U5-ch50, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 42.76
Std Dev 3.109
Gaus mean : 43.3590
Gaus Width: 3.1958
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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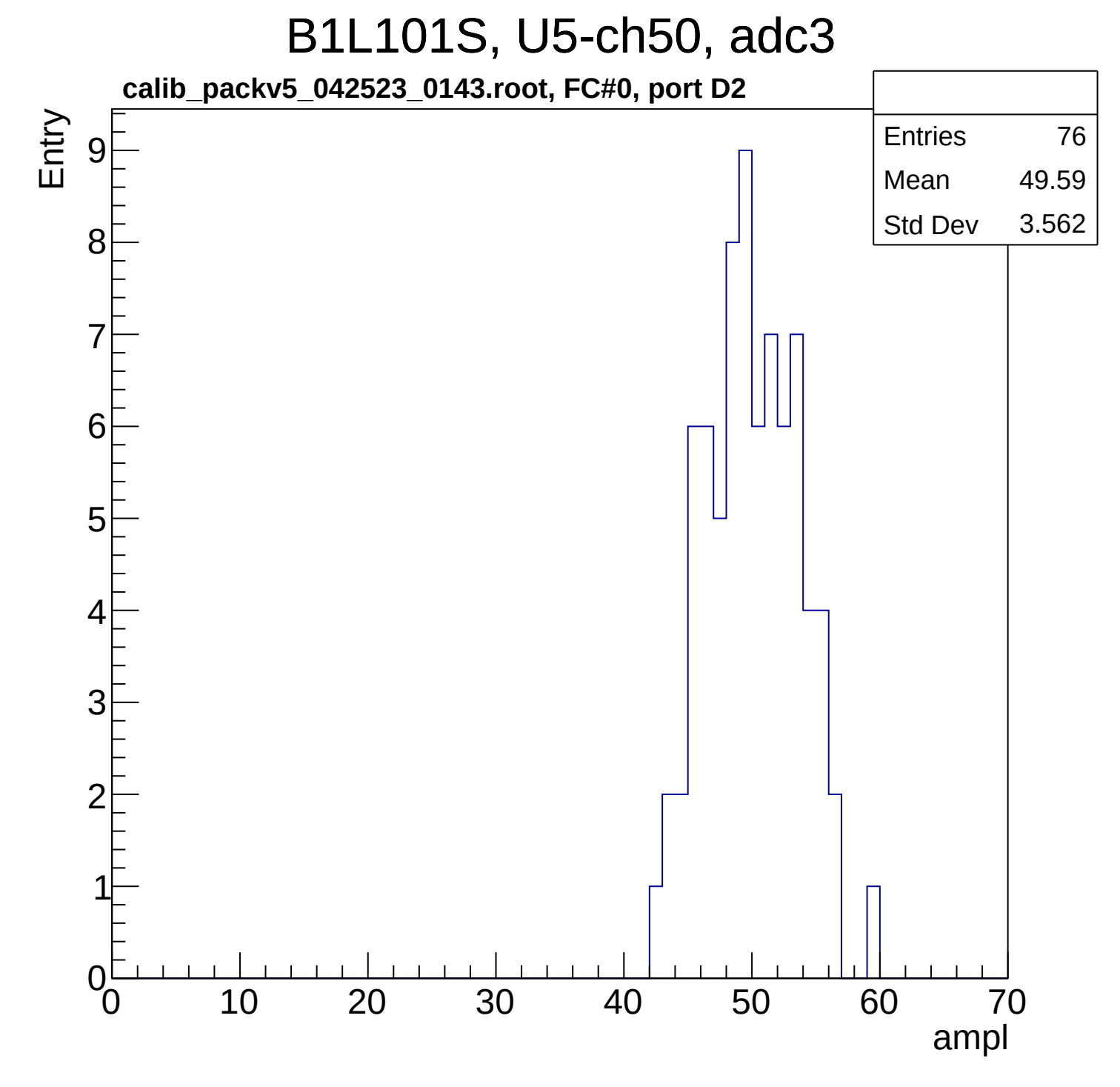
B1L101S, U5-ch50, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 49.59
Std Dev 3.562
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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60
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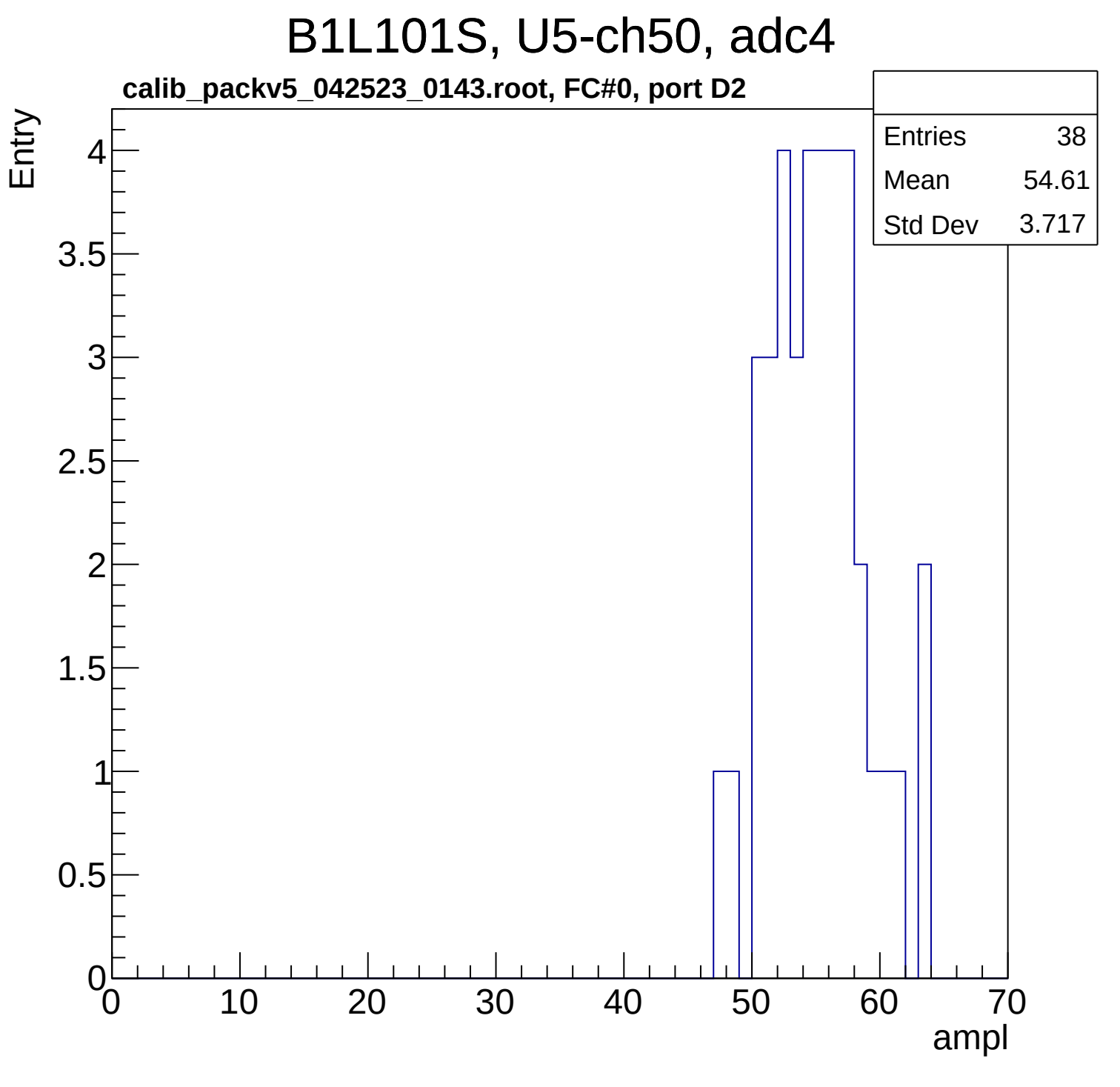
B1L101S, U5-ch50, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 38
Mean 54.61
Std Dev 3.717
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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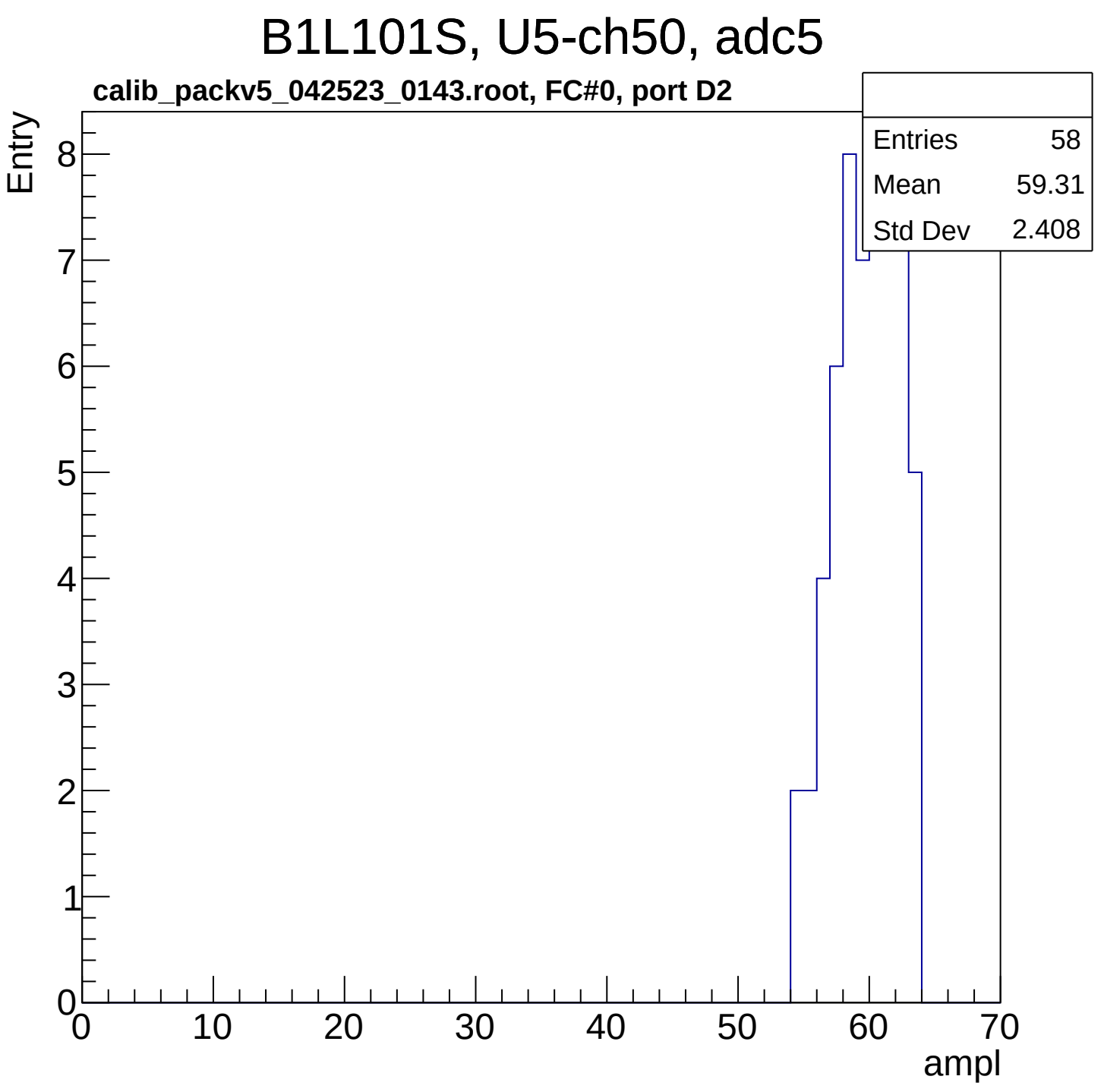
B1L101S, U5-ch50, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 59.31
Std Dev 2.408
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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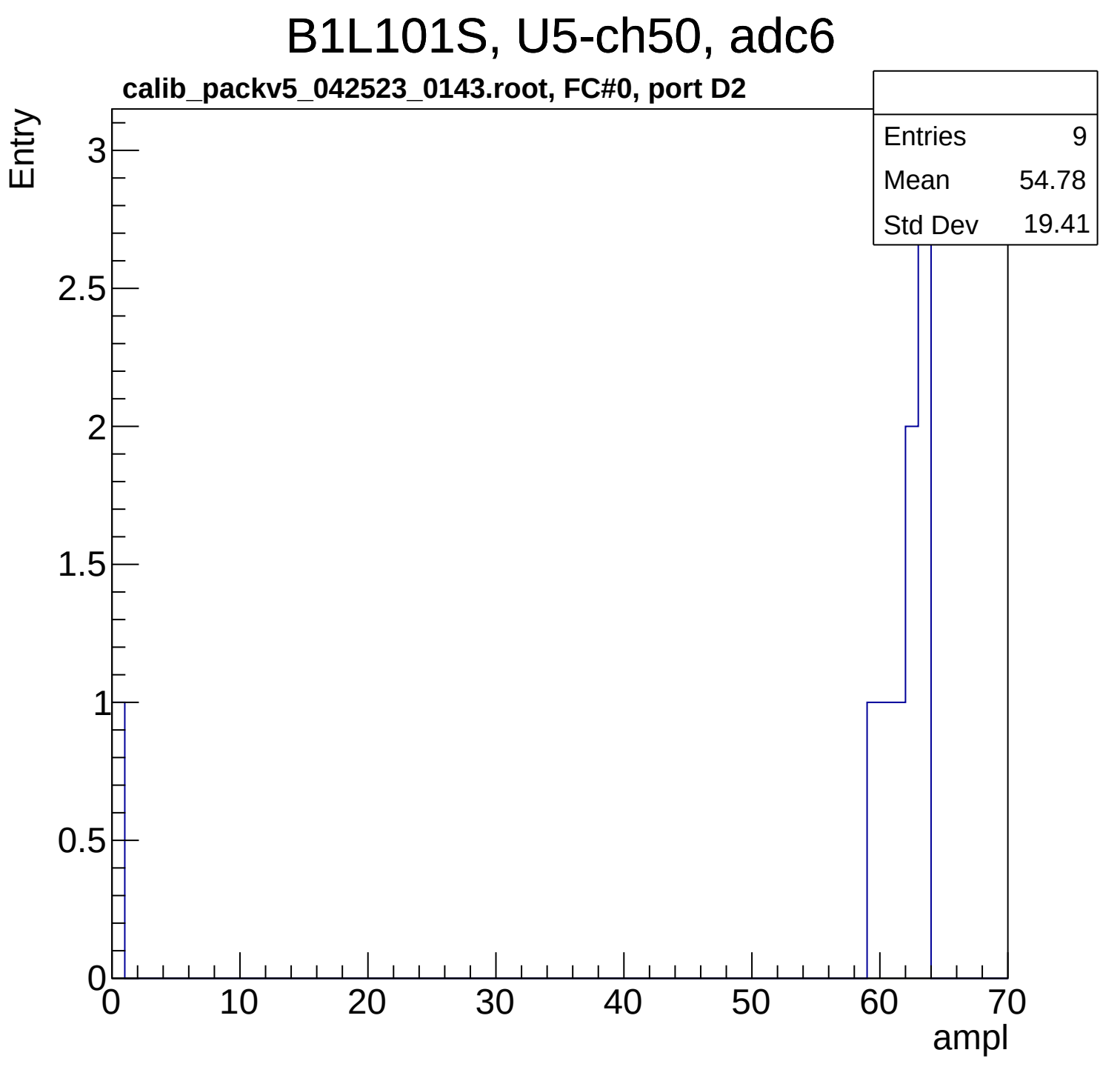
B1L101S, U5-ch50, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 54.78
Std Dev 19.41
Entry
ampl
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1.5
2
2.5
3
0
10
20
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40
50
60
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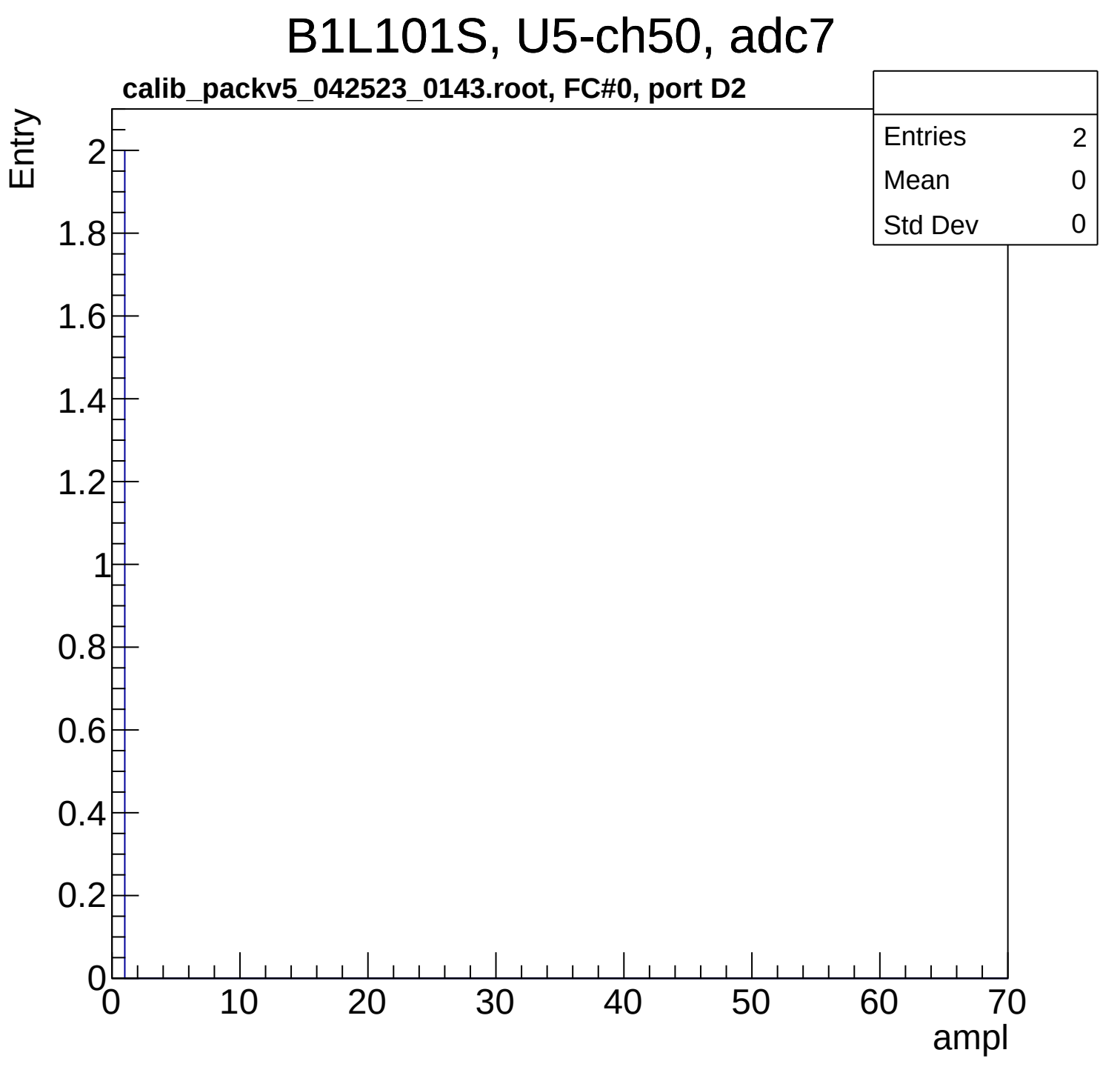
B1L101S, U5-ch50, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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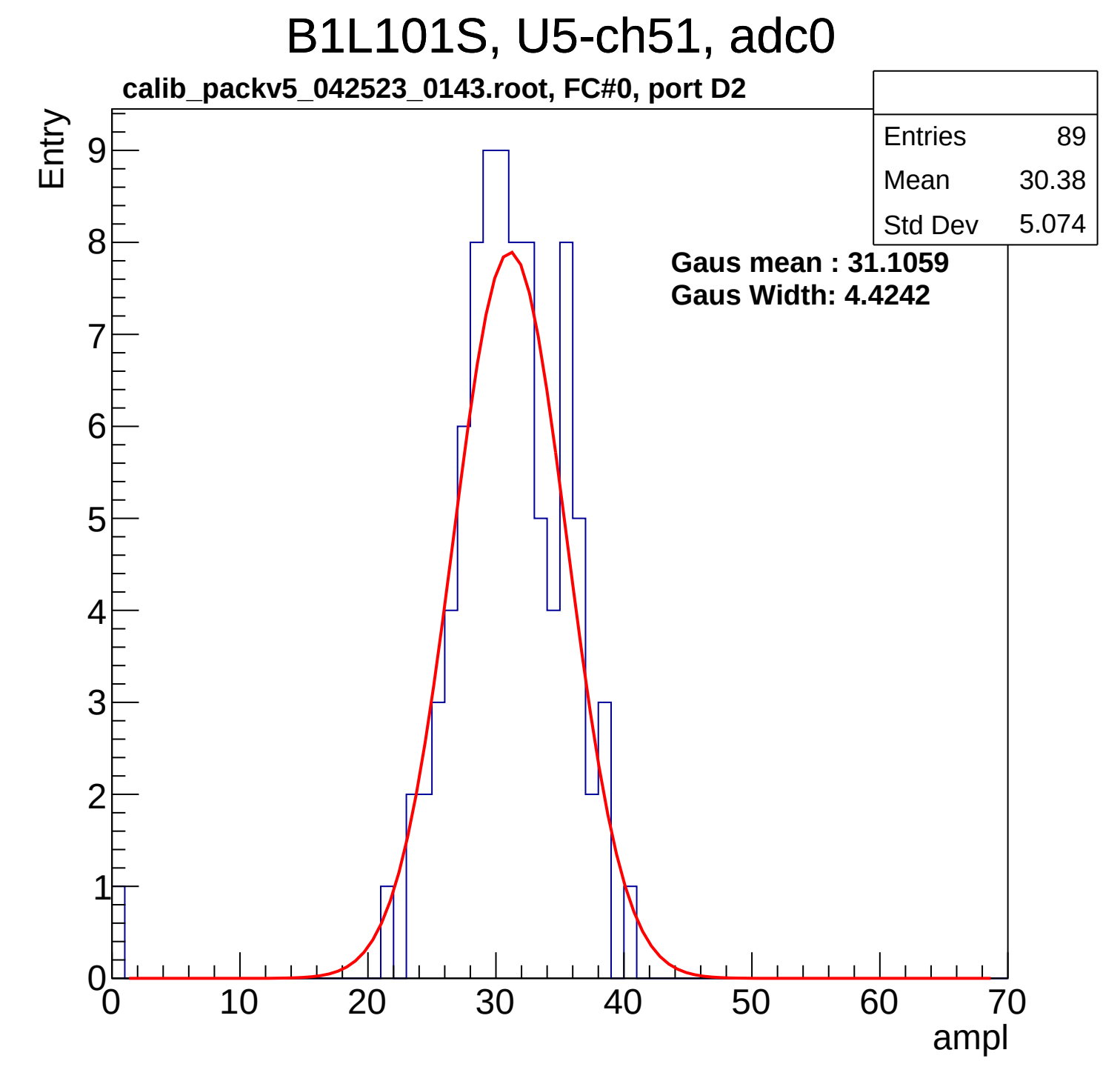
B1L101S, U5-ch51, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 89
Mean 30.38
Std Dev 5.074
Gaus mean : 31.1059
Gaus Width: 4.4242
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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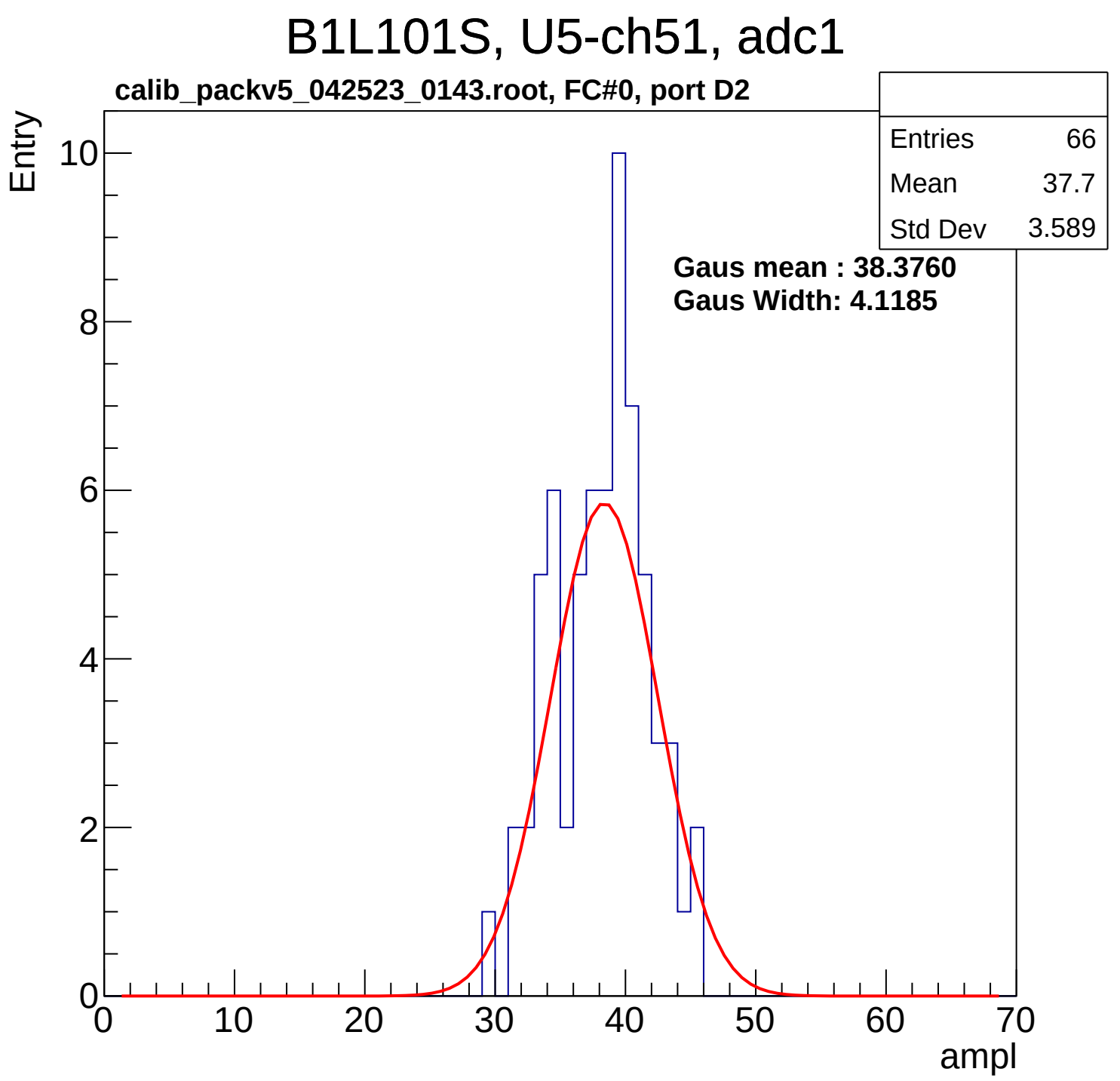
B1L101S, U5-ch51, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 37.7
Std Dev 3.589
Gaus mean : 38.3760
Gaus Width: 4.1185
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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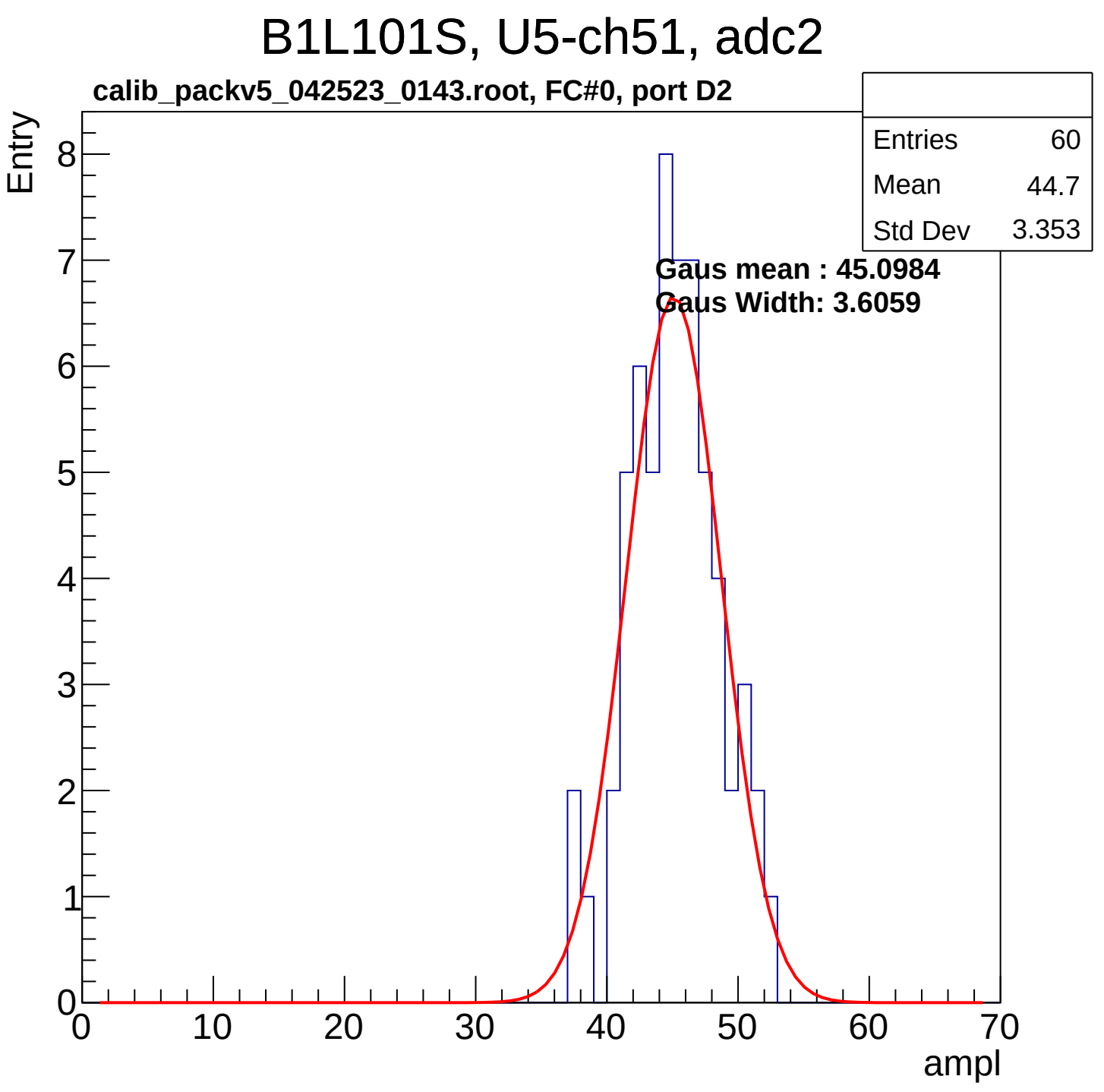
B1L101S, U5-ch51, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 44.7
Std Dev 3.353
Gaus mean : 45.0984
Gaus Width: 3.6059
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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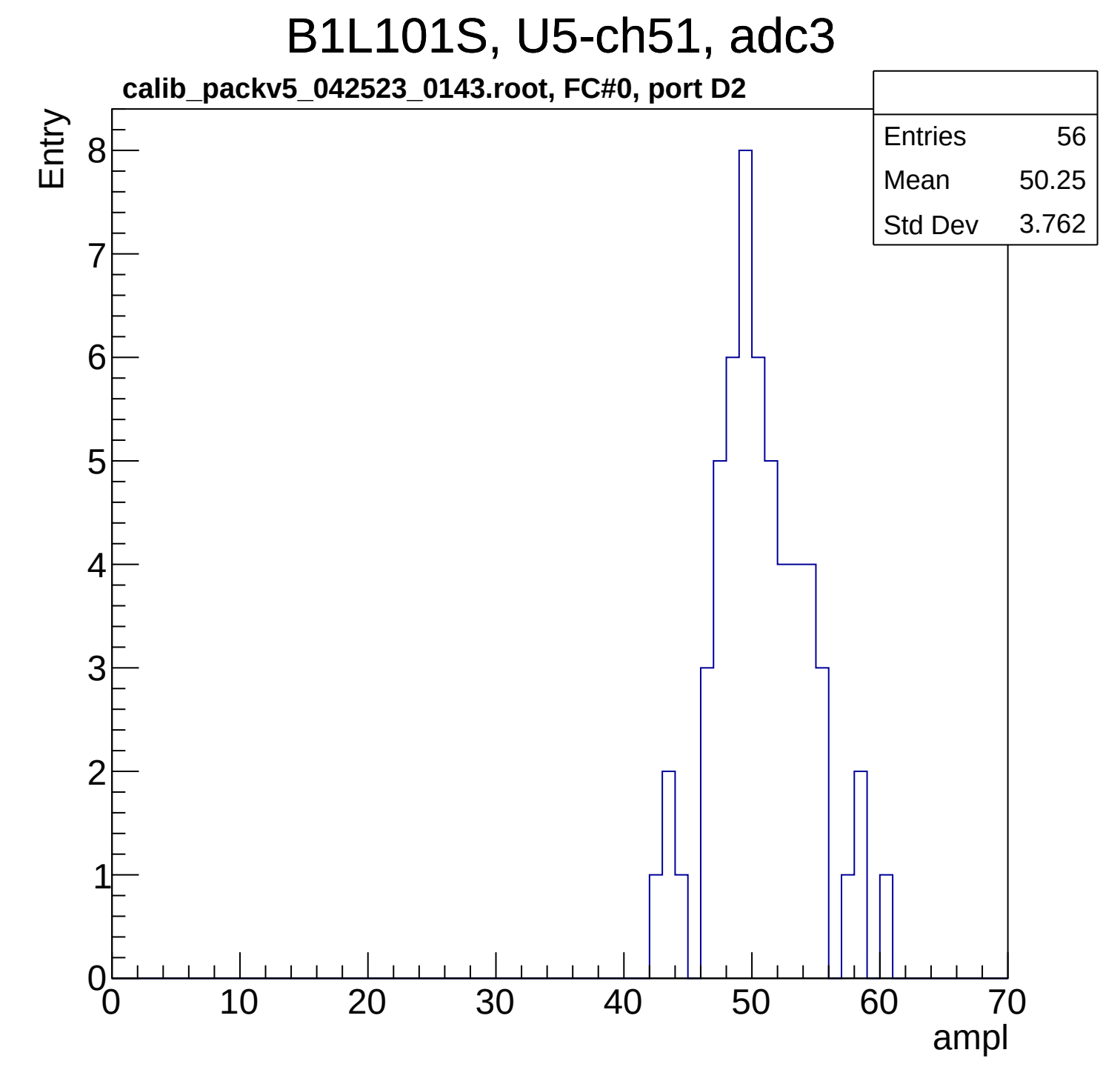
B1L101S, U5-ch51, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 50.25
Std Dev 3.762
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
50
60
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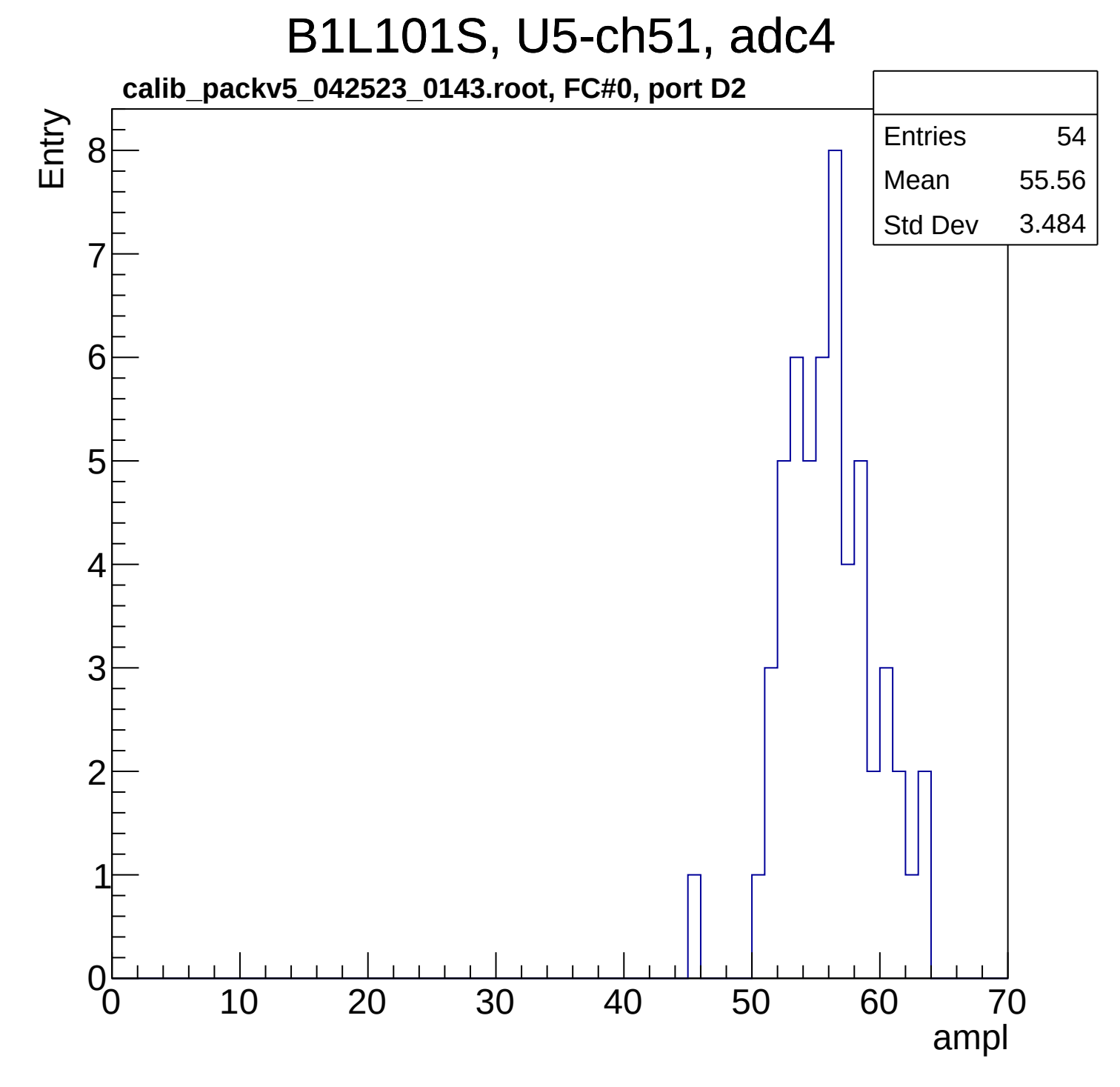
B1L101S, U5-ch51, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 55.56
Std Dev 3.484
Entry
ampl
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3
4
5
6
7
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0
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20
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40
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60
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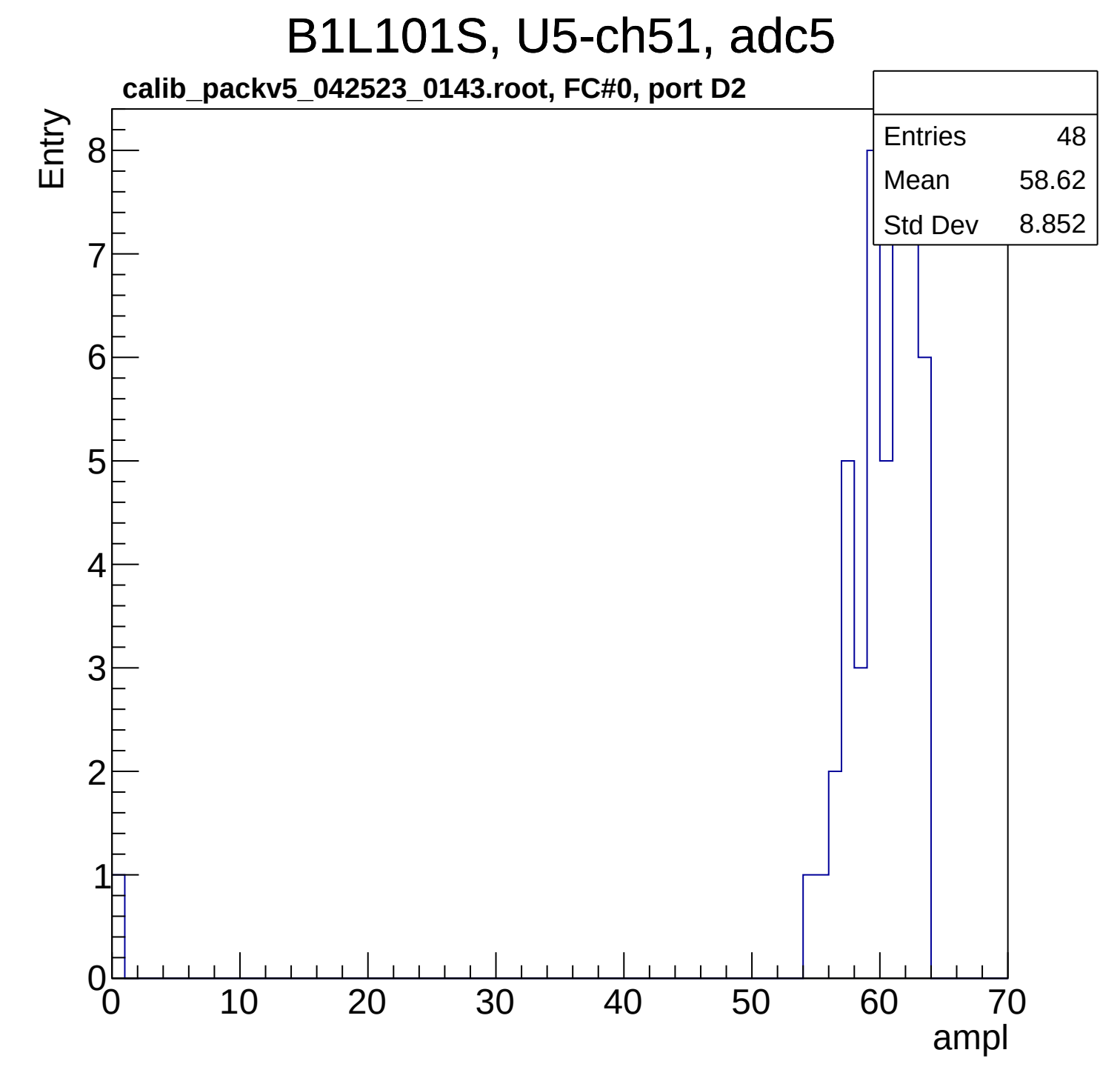
B1L101S, U5-ch51, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 58.62
Std Dev 8.852
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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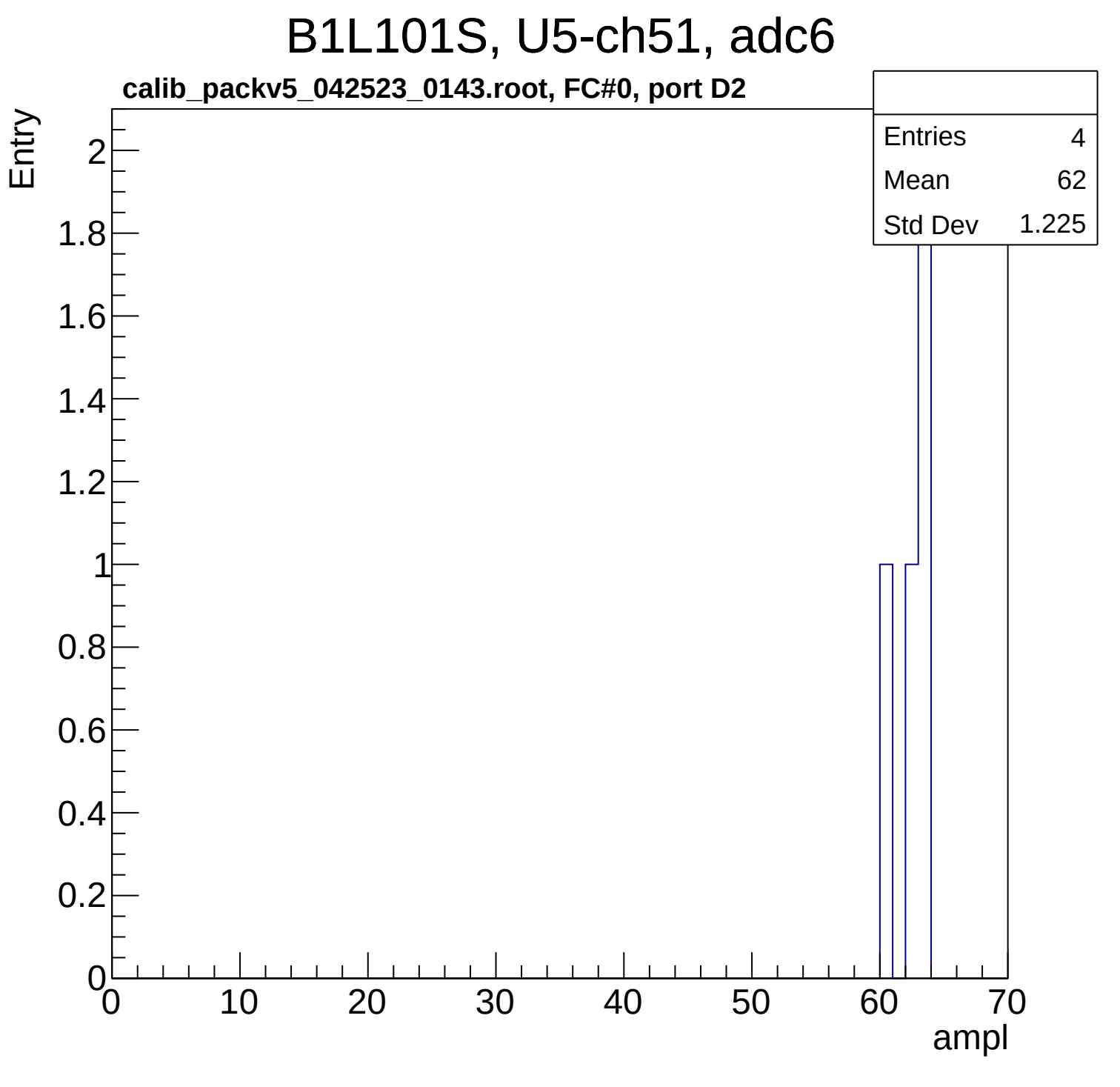
B1L101S, U5-ch51, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 62
Std Dev 1.225
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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20
30
40
50
60
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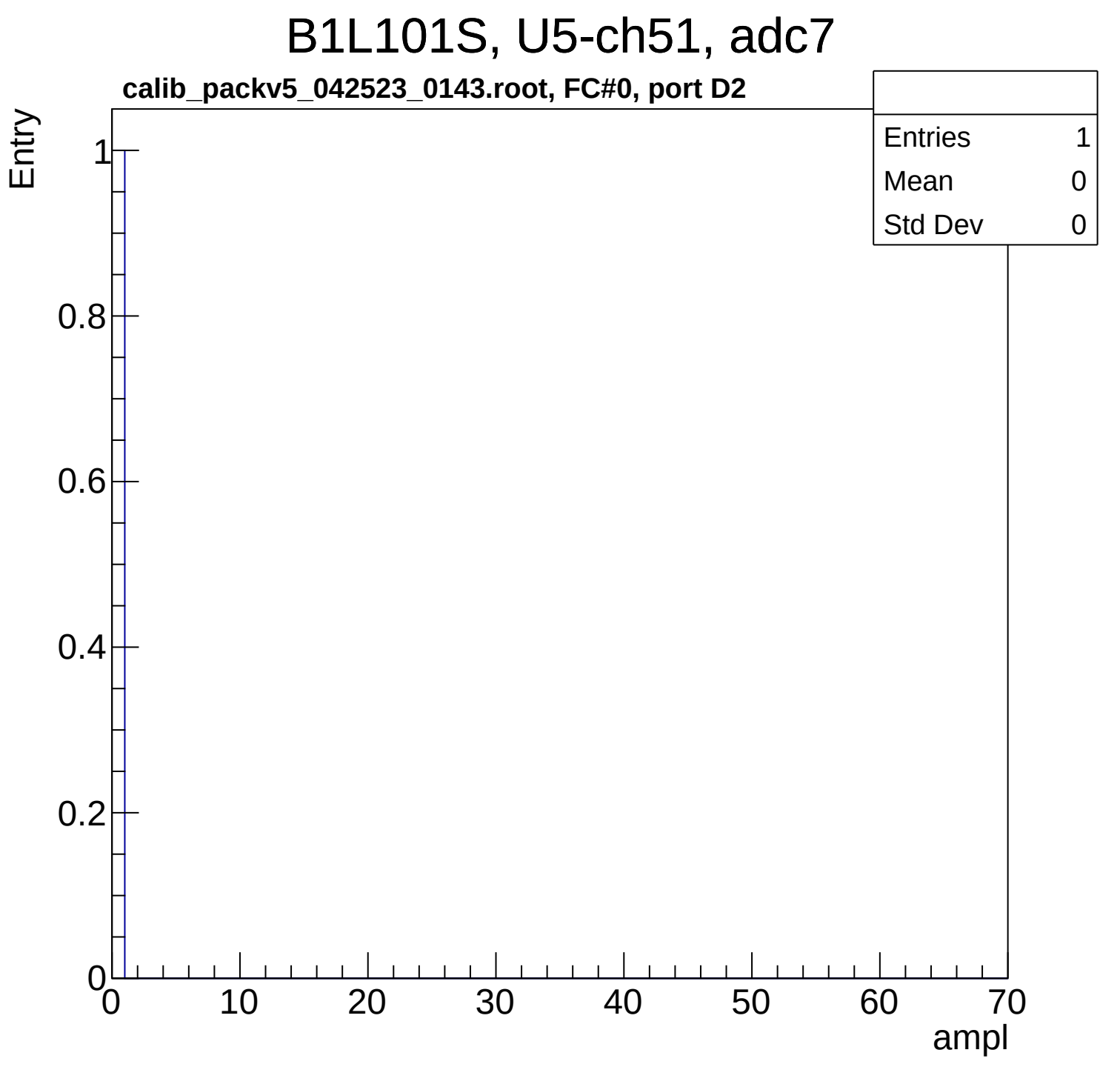
B1L101S, U5-ch51, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
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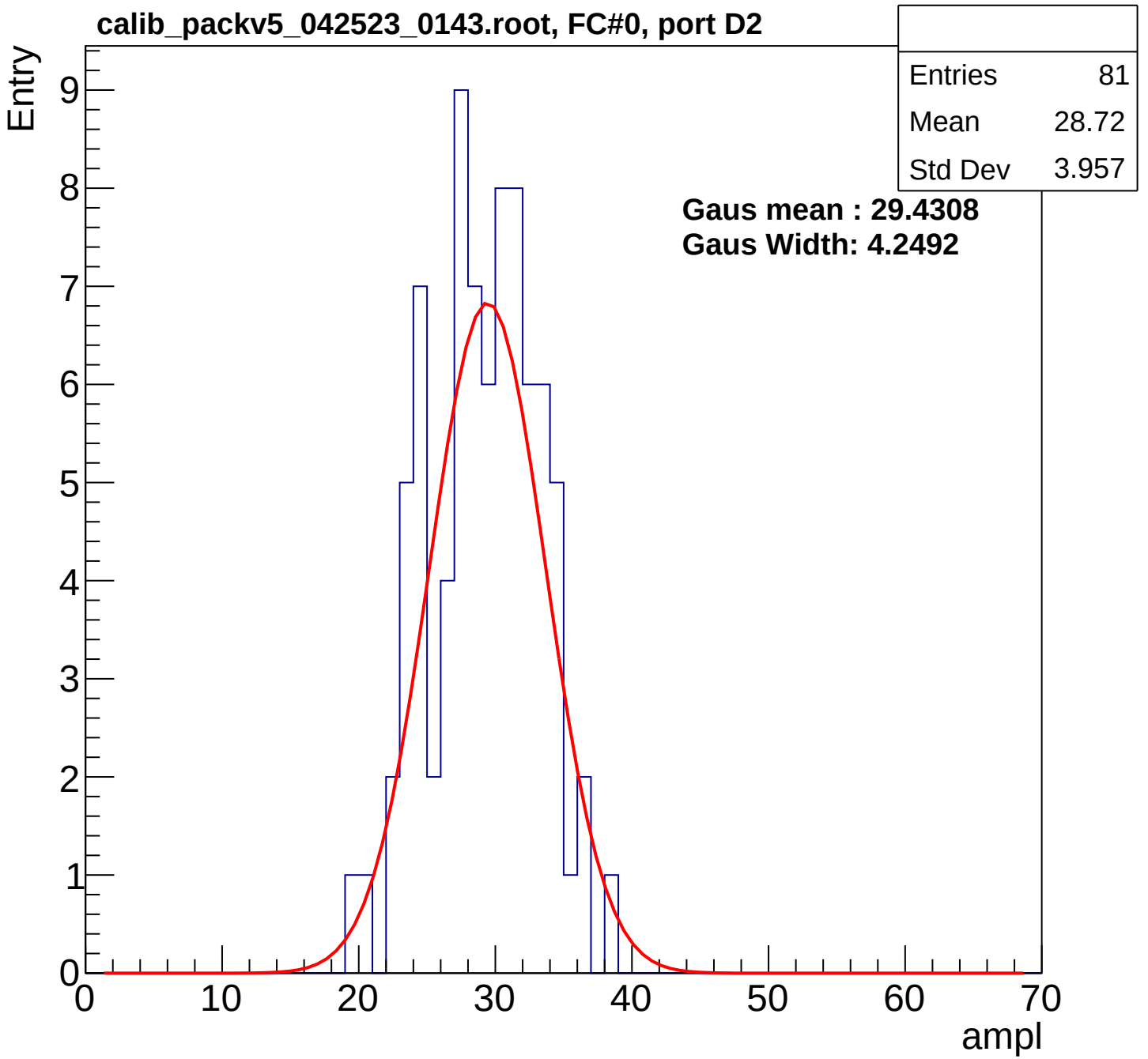
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch52, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 81
Mean 28.72
Std Dev 3.957
Gaus mean : 29.4308
Gaus Width: 4.2492
Entry
ampl
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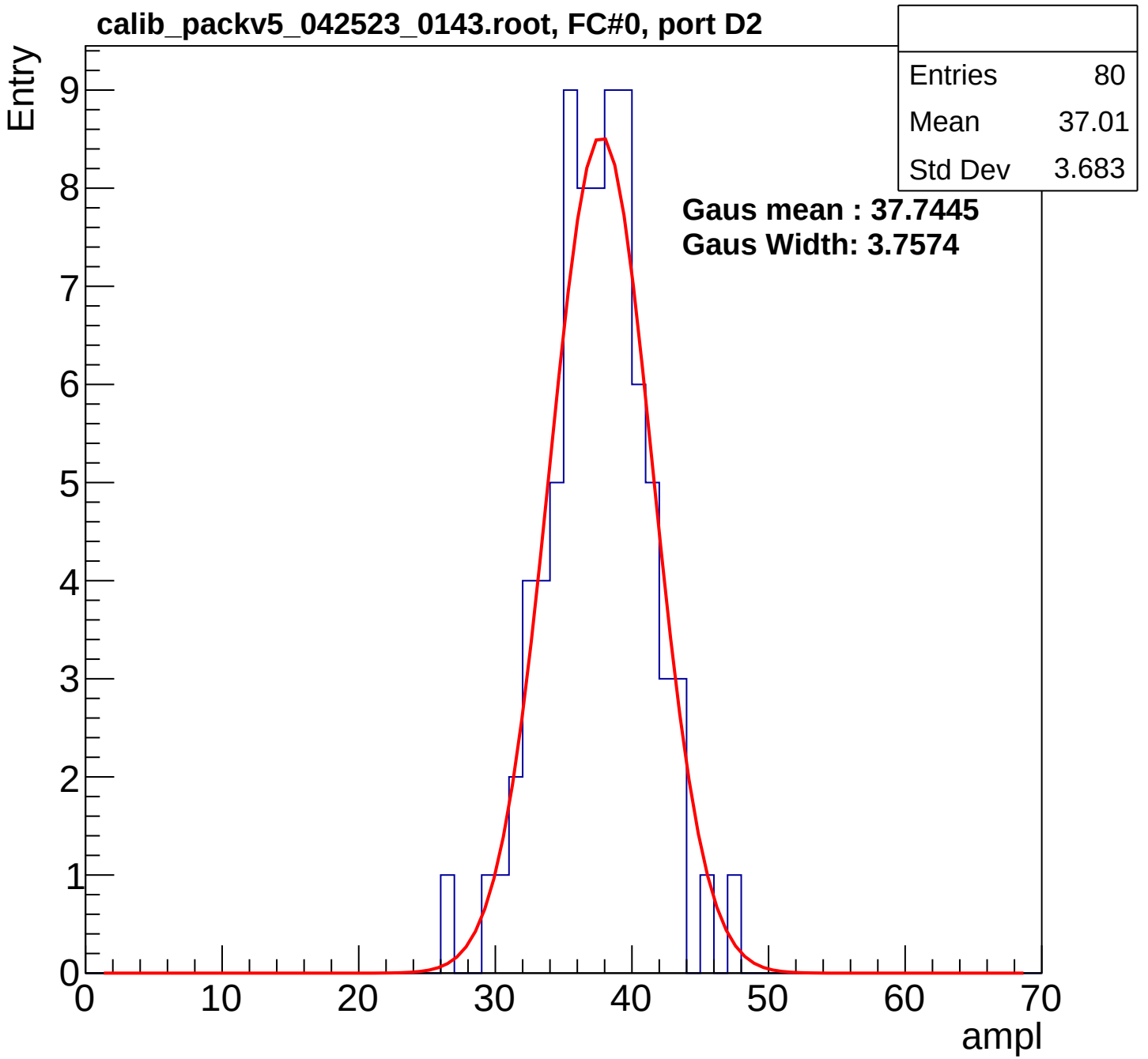
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L101S, U5-ch52, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 80
Mean 37.01
Std Dev 3.683
Gaus mean : 37.7445
Gaus Width: 3.7574
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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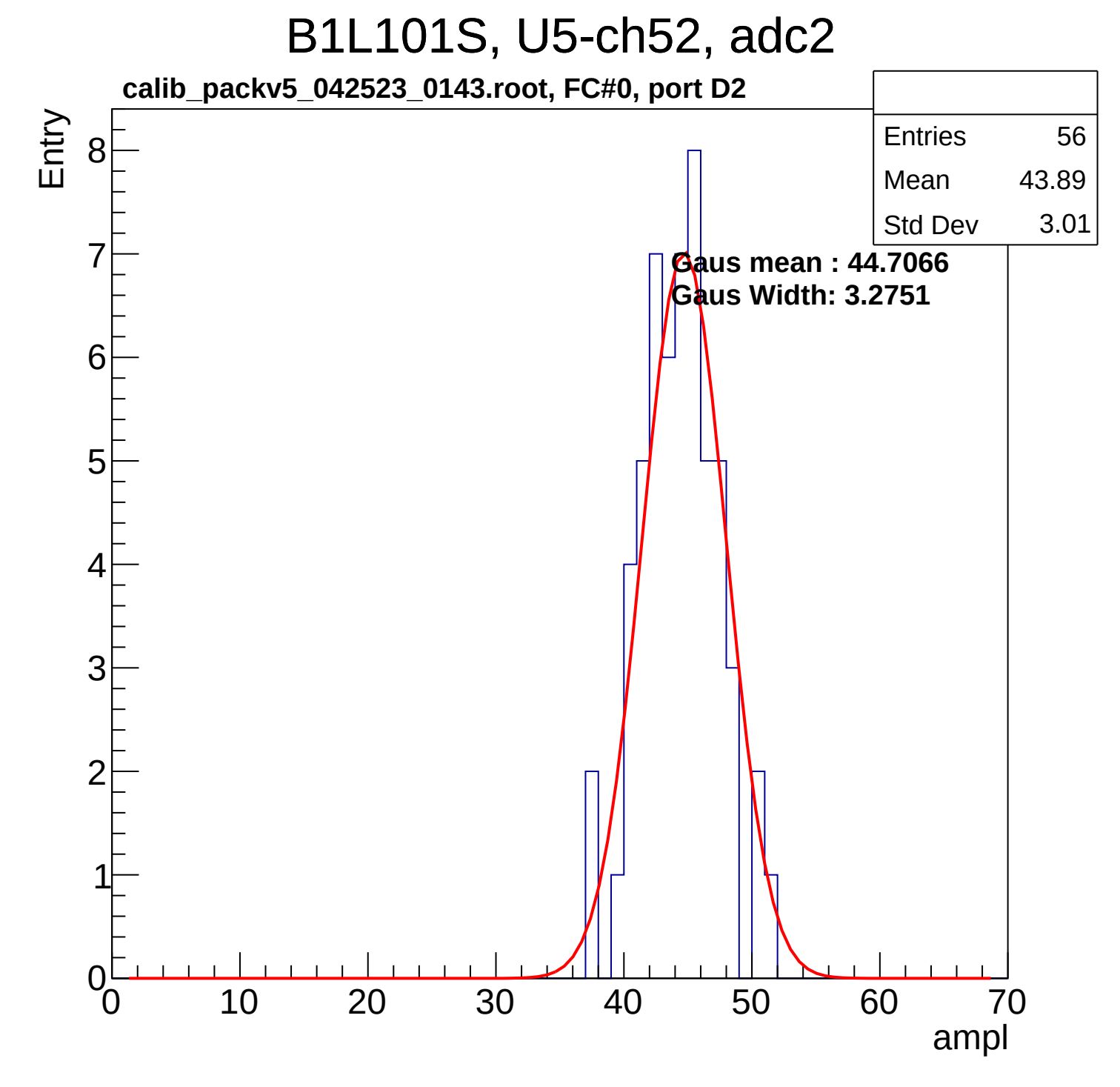
B1L101S, U5-ch52, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 43.89
Std Dev 3.01
Gaus mean : 44.7066
Gaus Width: 3.2751
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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60
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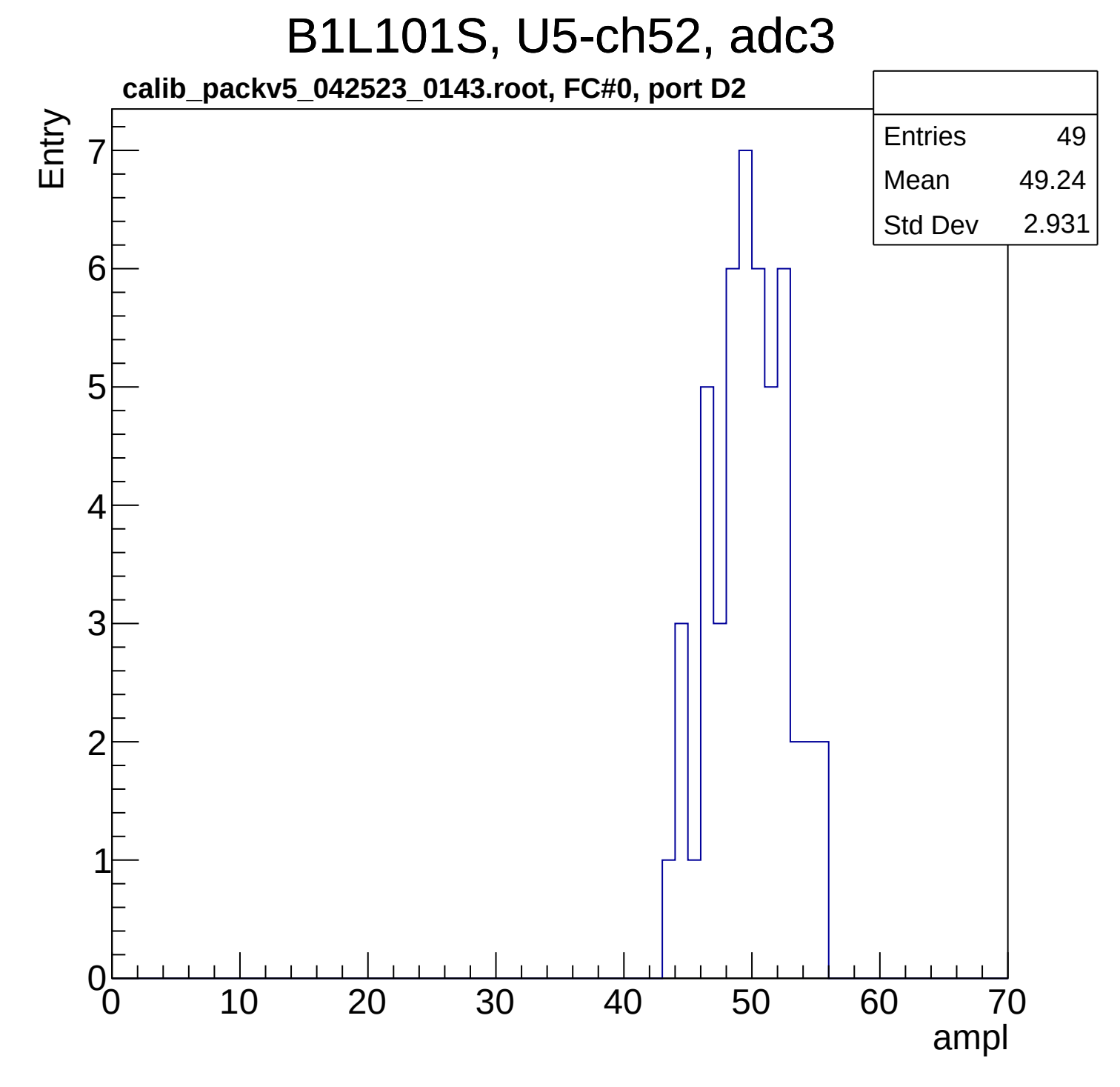
B1L101S, U5-ch52, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 49.24
Std Dev 2.931
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
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60
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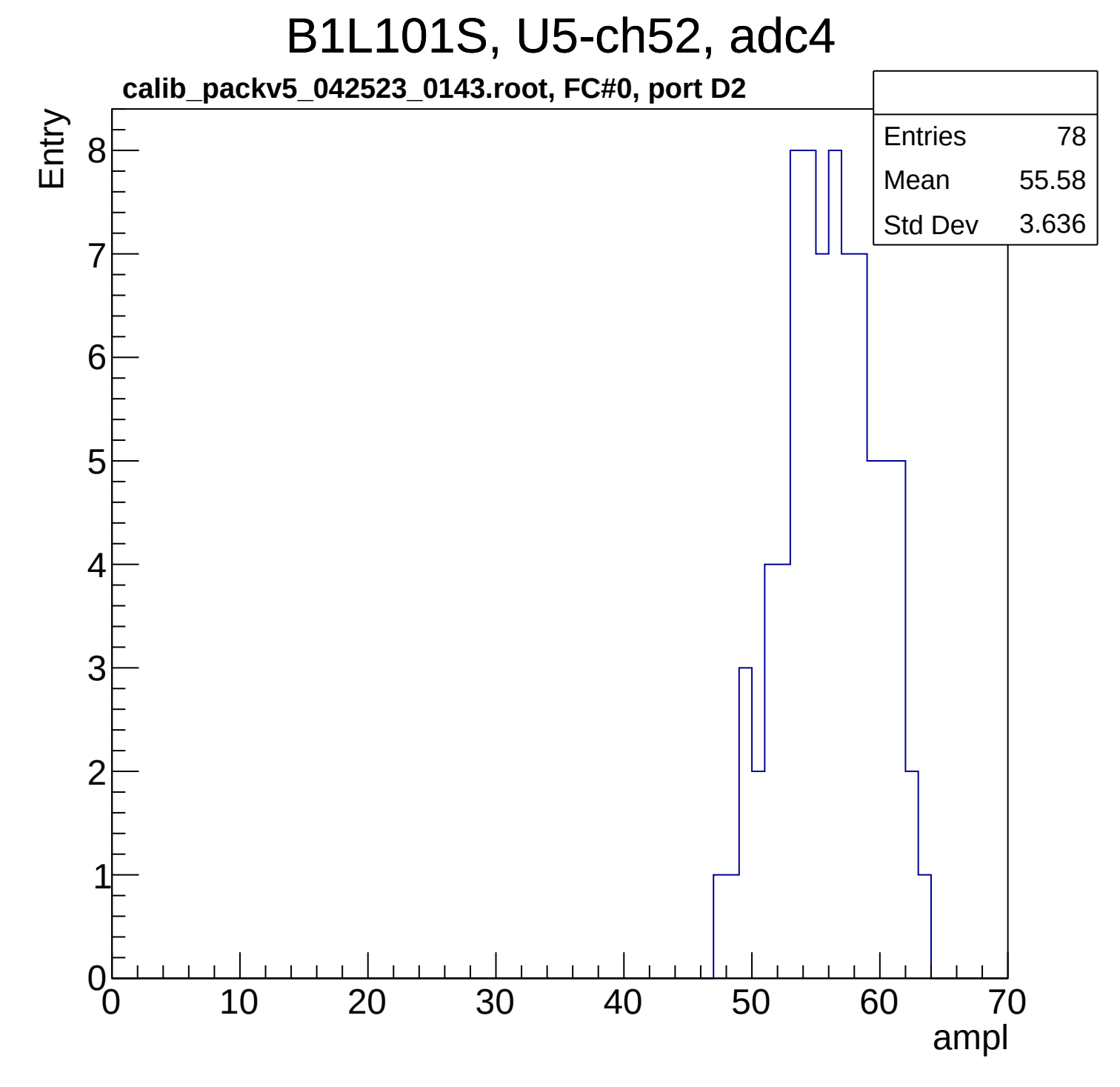
B1L101S, U5-ch52, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 55.58
Std Dev 3.636
Entry
ampl
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2
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4
5
6
7
8
0
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60
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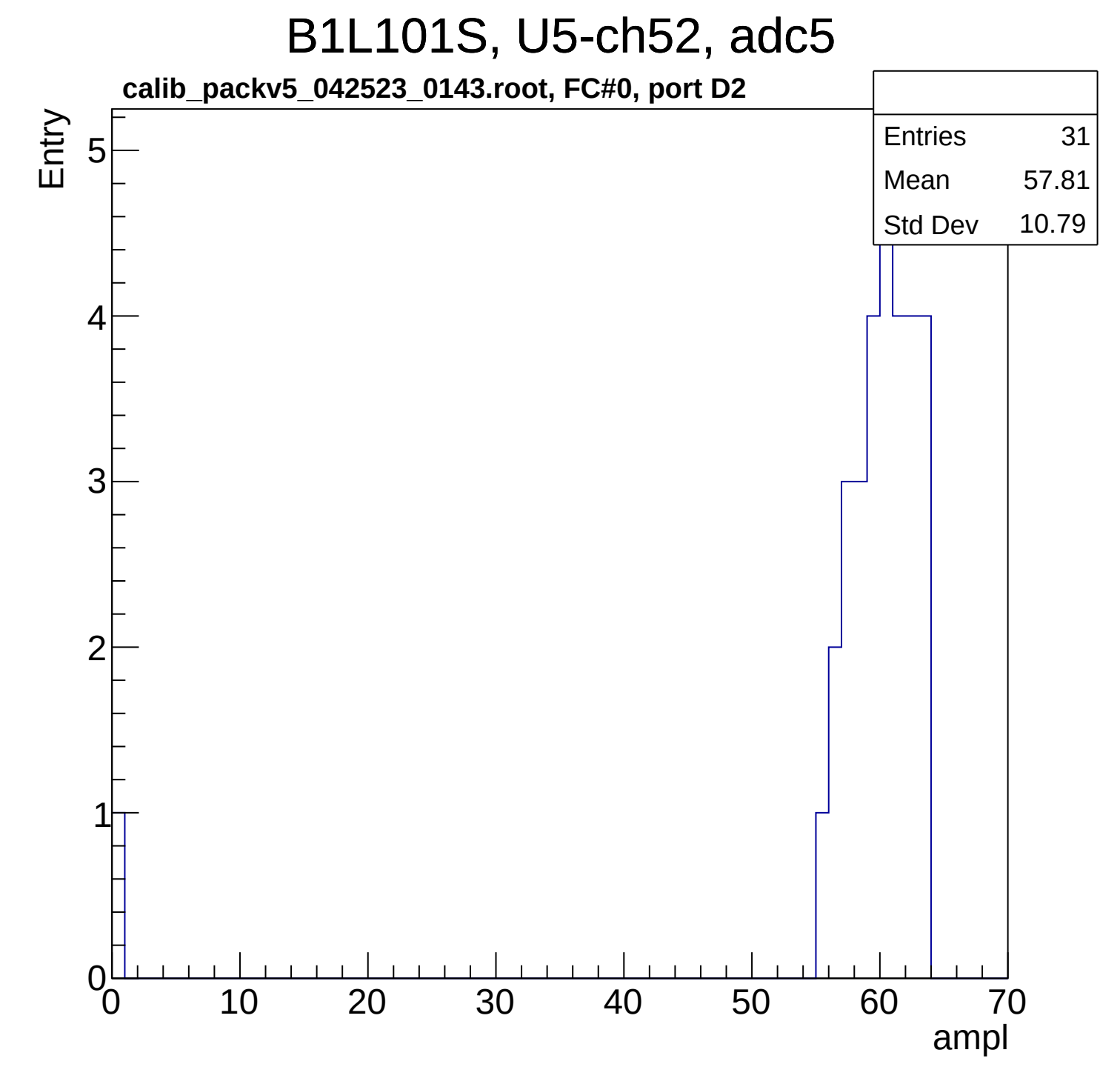
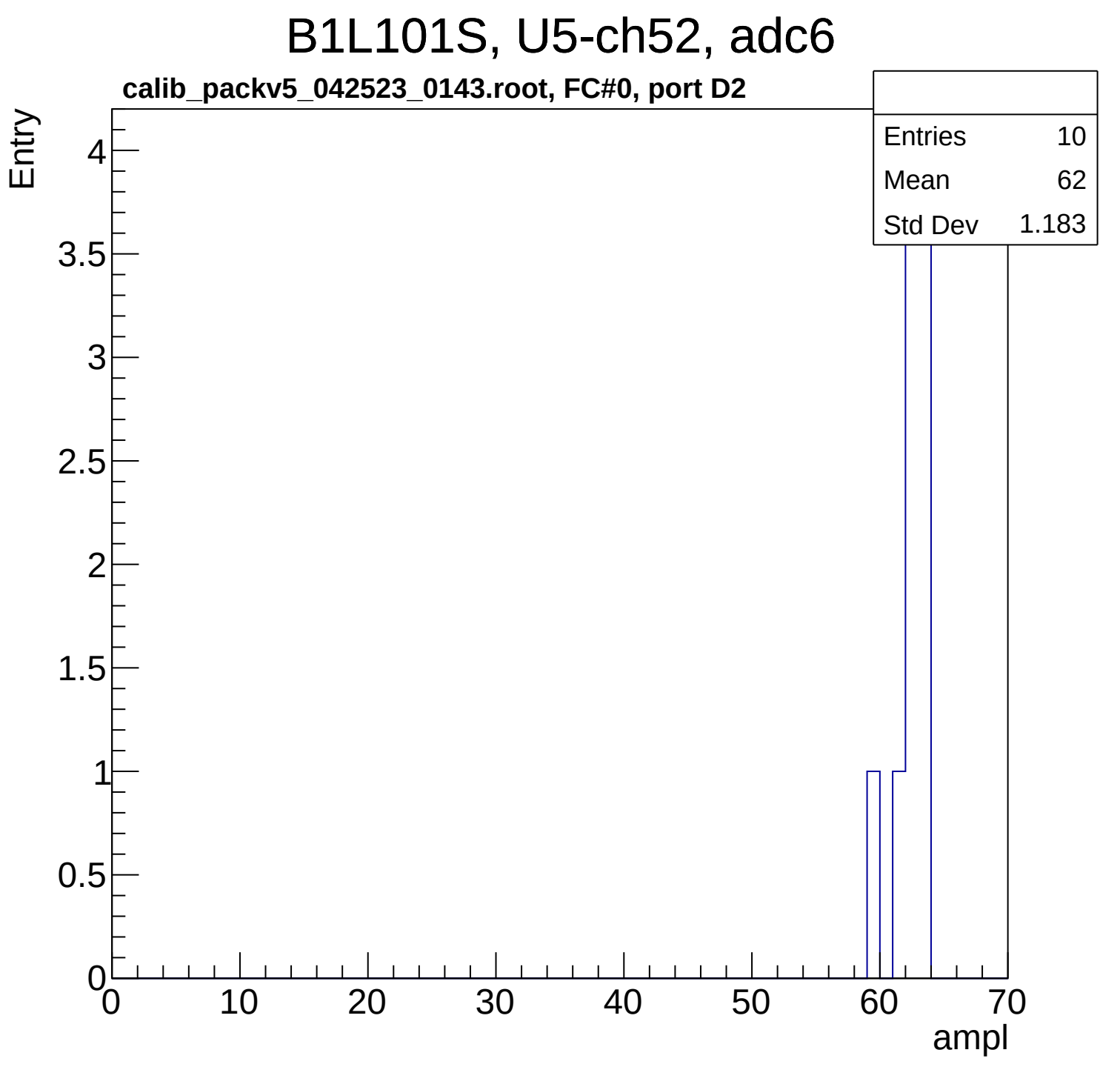

B1L101S, U5-ch52, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 31
Mean 57.81
Std Dev 10.79
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch52, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 62
Std Dev 1.183
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
10
20
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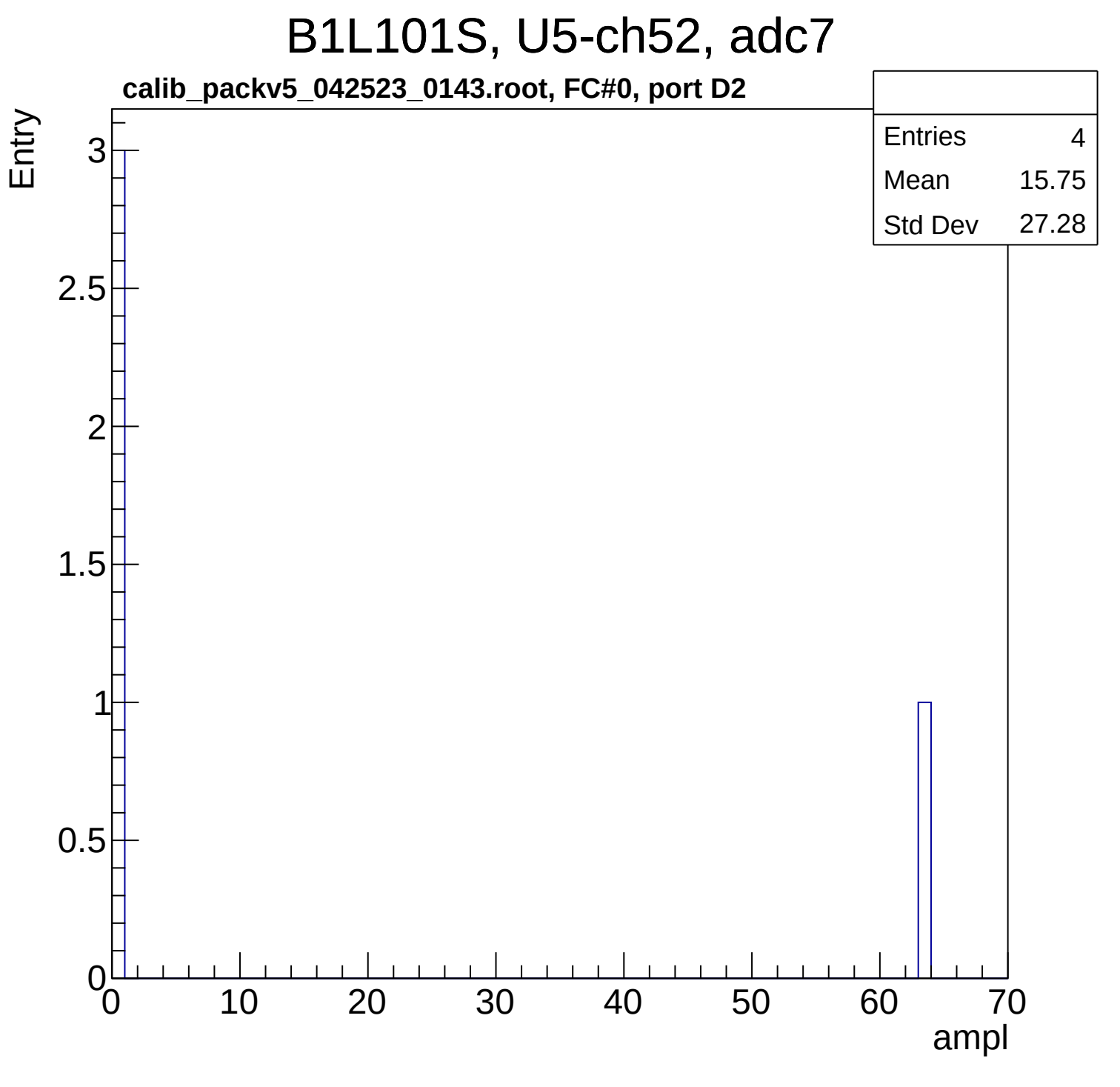
40
50
60
70


B1L101S, U5-ch52, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 15.75
Std Dev 27.28
Entry
ampl
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1
1.5
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2.5
3
0
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20
30
40
50
60
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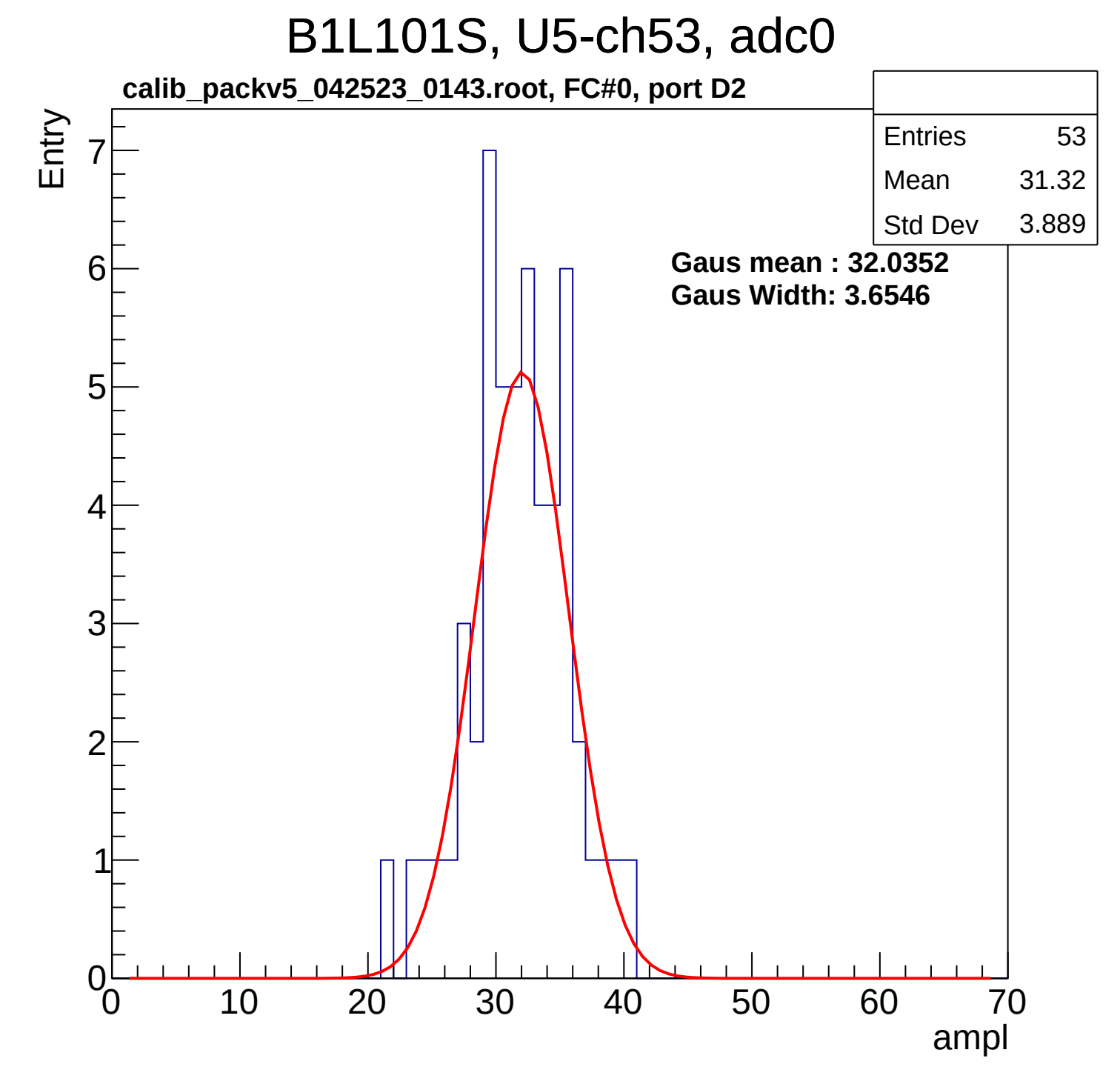
B1L101S, U5-ch53, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 31.32
Std Dev 3.889
Gaus mean : 32.0352
Gaus Width: 3.6546
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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40
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60
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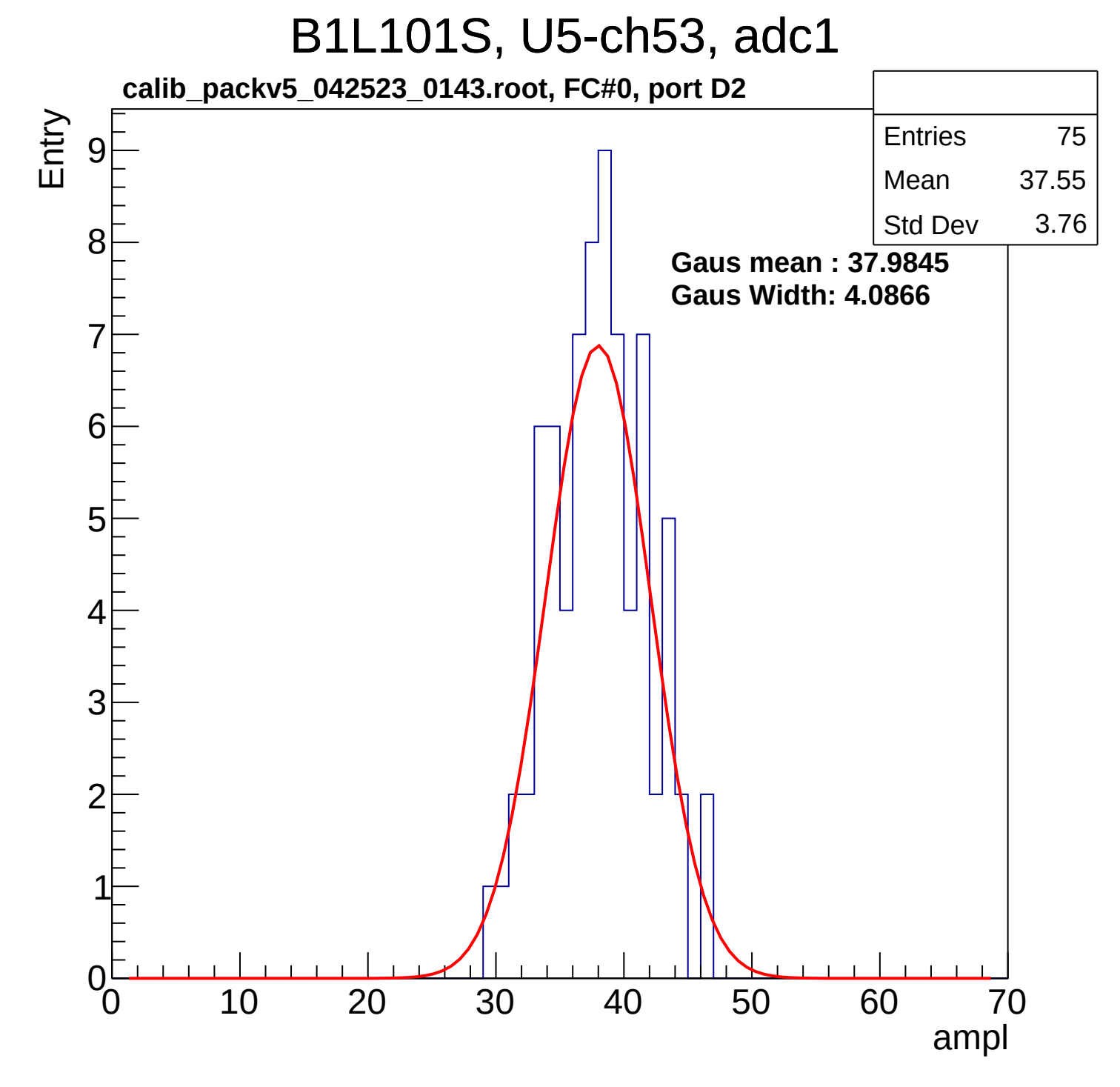
B1L101S, U5-ch53, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 37.55
Std Dev 3.76
Gaus mean : 37.9845
Gaus Width: 4.0866
Entry
ampl
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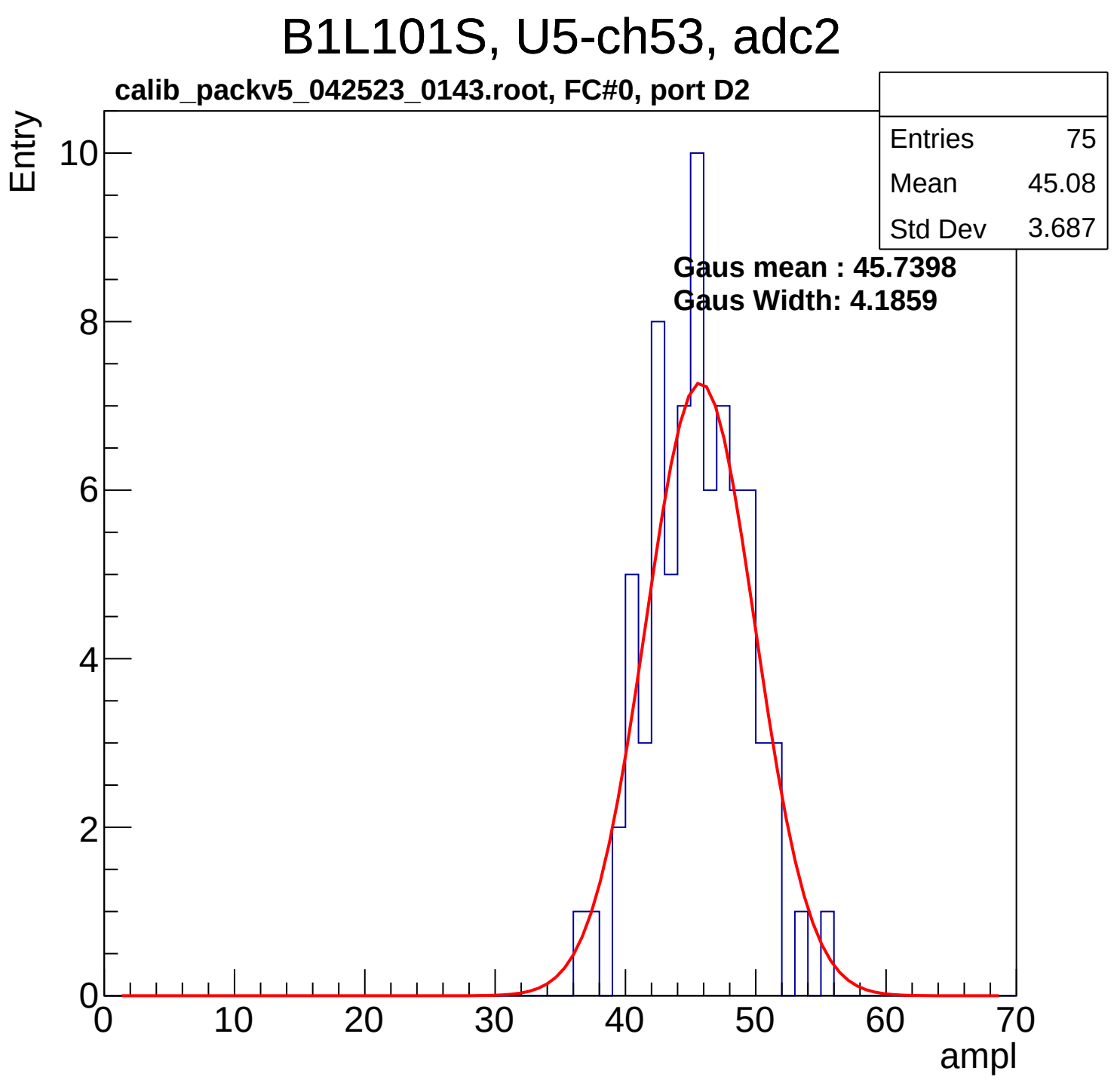
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L101S, U5-ch53, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 45.08
Std Dev 3.687
Gaus mean : 45.7398
Gaus Width: 4.1859
Entry
ampl
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4
6
8
10
0
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20
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40
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60
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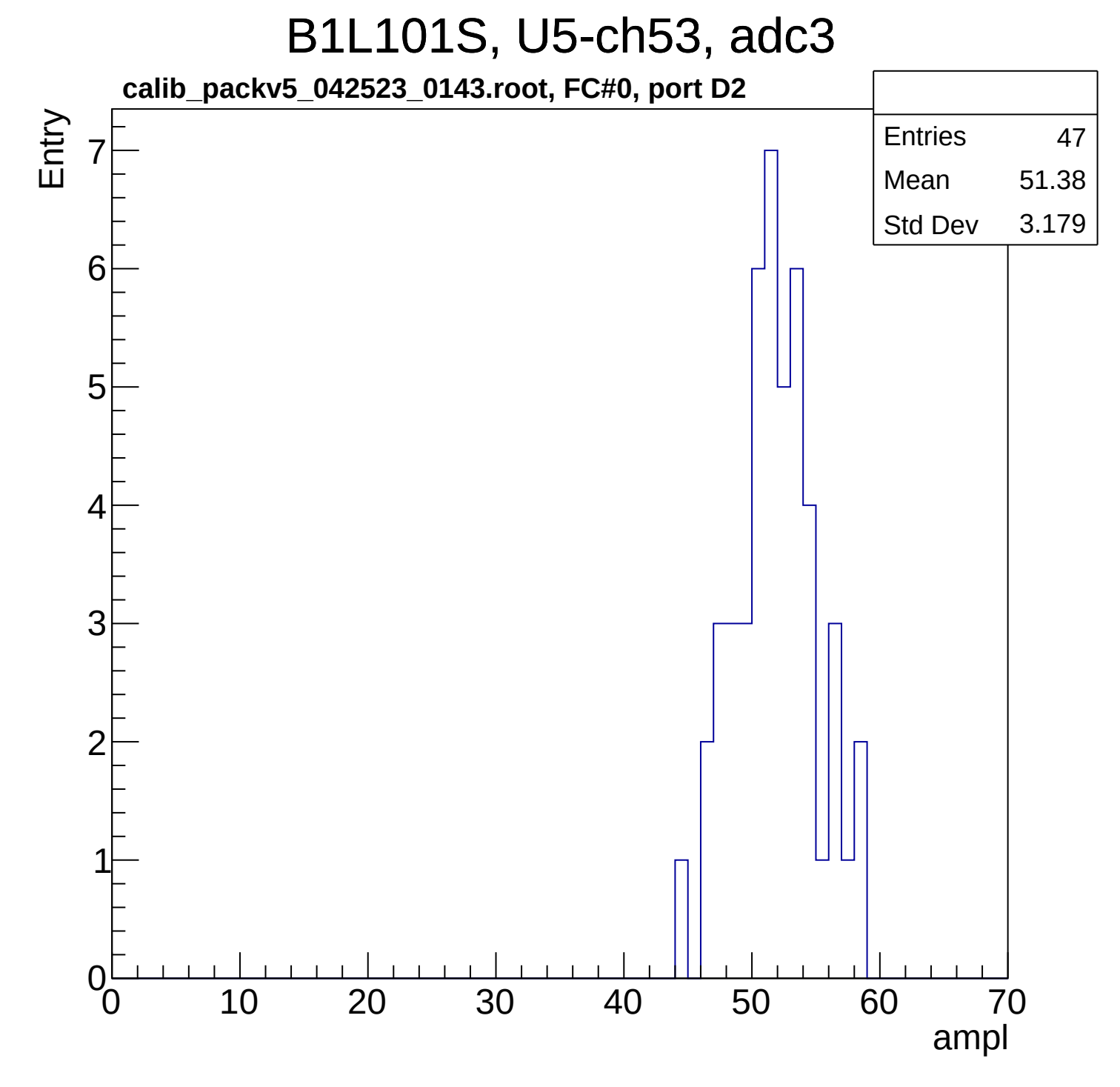
B1L101S, U5-ch53, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 51.38
Std Dev 3.179
Entry
ampl
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3
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5
6
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0
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50
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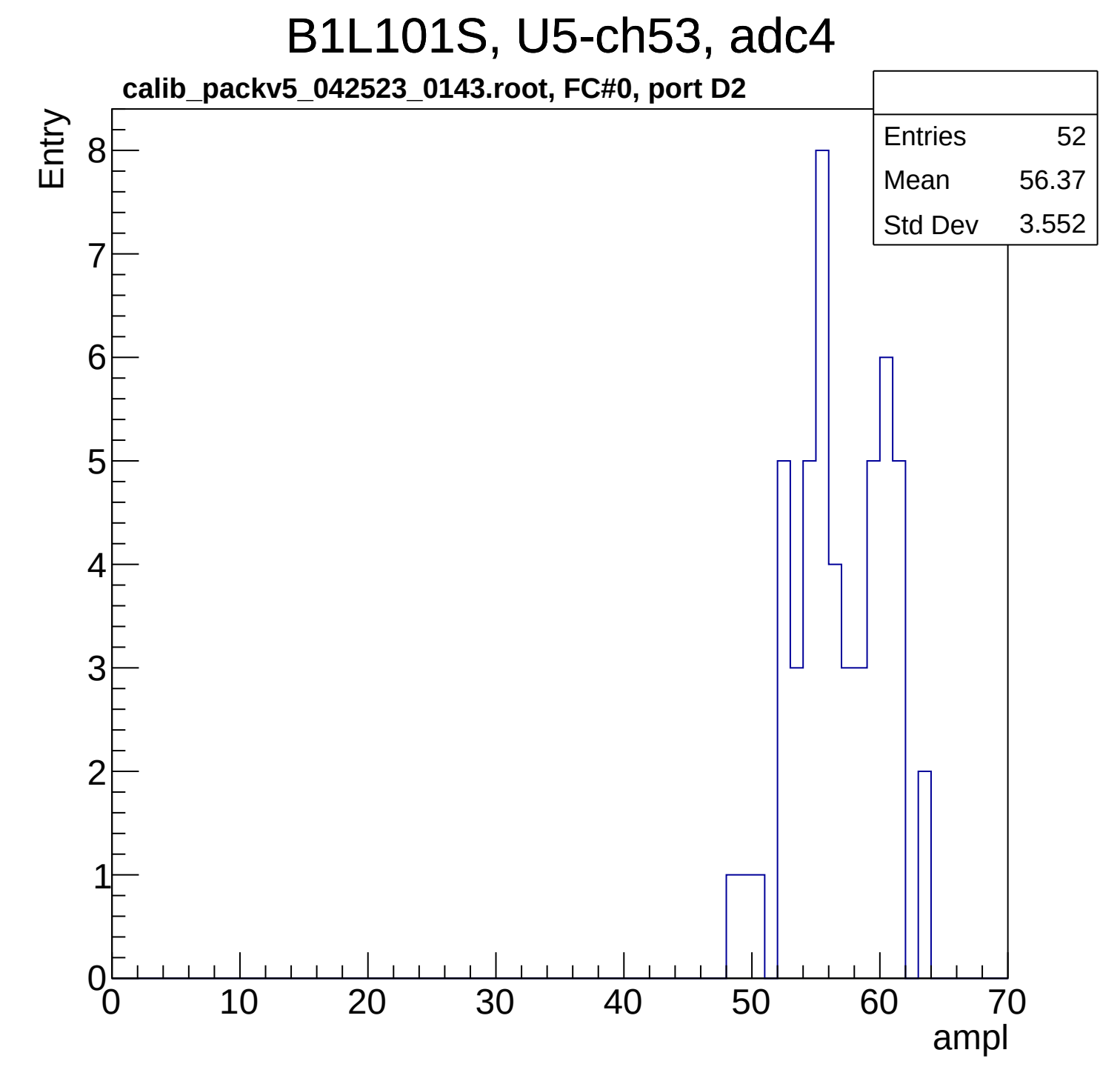
B1L101S, U5-ch53, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 56.37
Std Dev 3.552
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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40
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60
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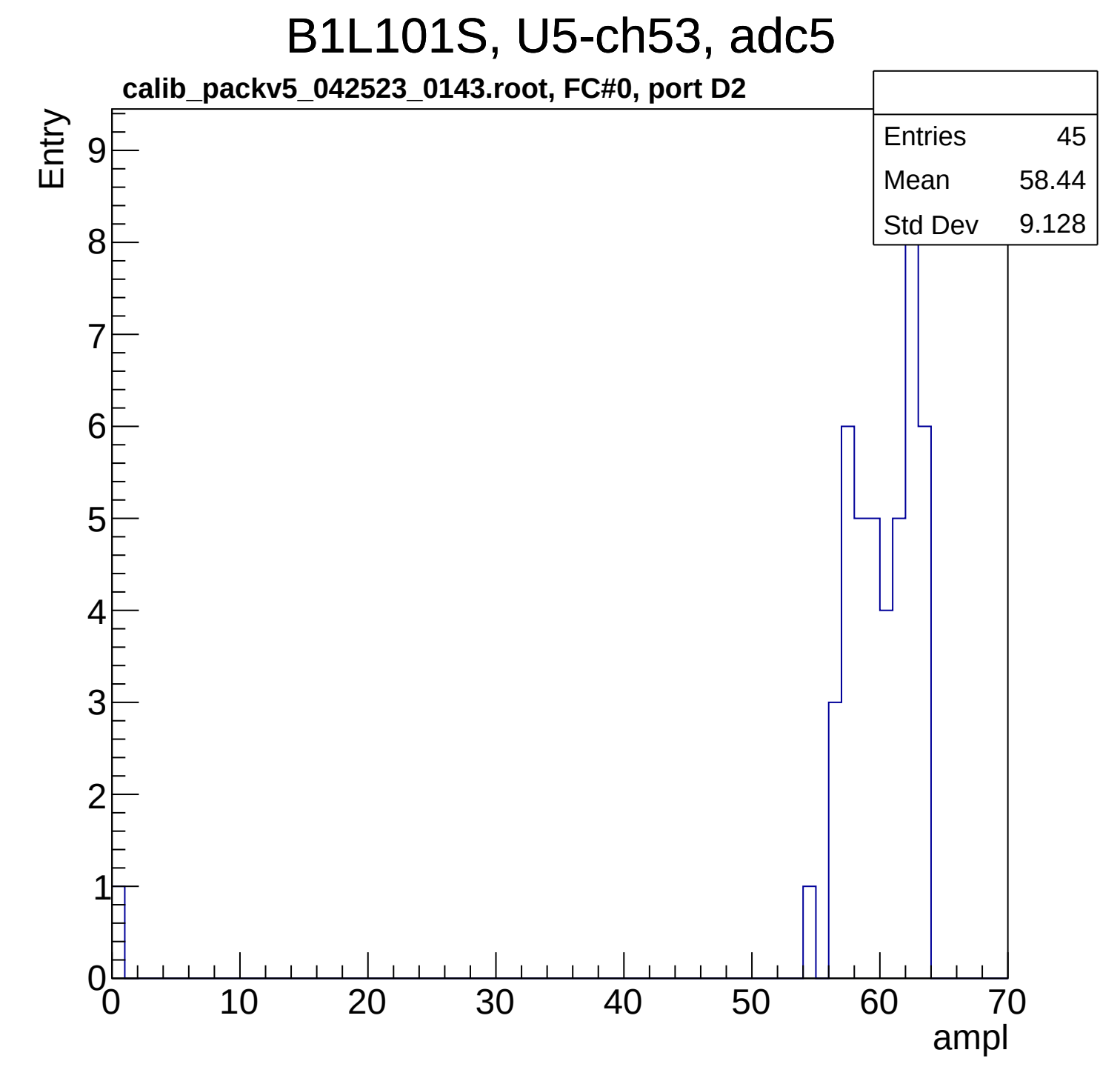
B1L101S, U5-ch53, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 58.44
Std Dev 9.128
Entry
ampl
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2
3
4
5
6
7
8
9
0
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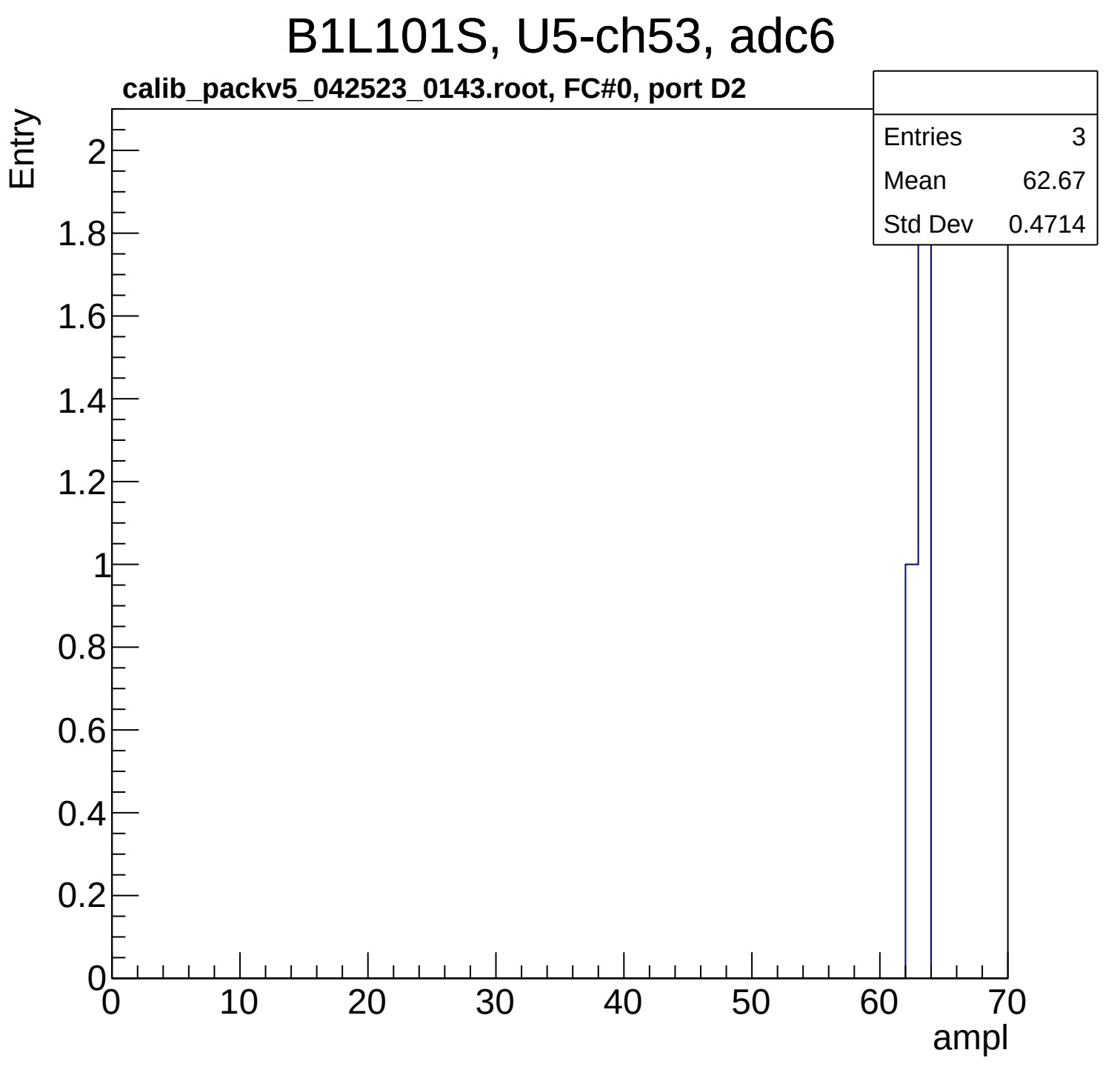
B1L101S, U5-ch53, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
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40
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60
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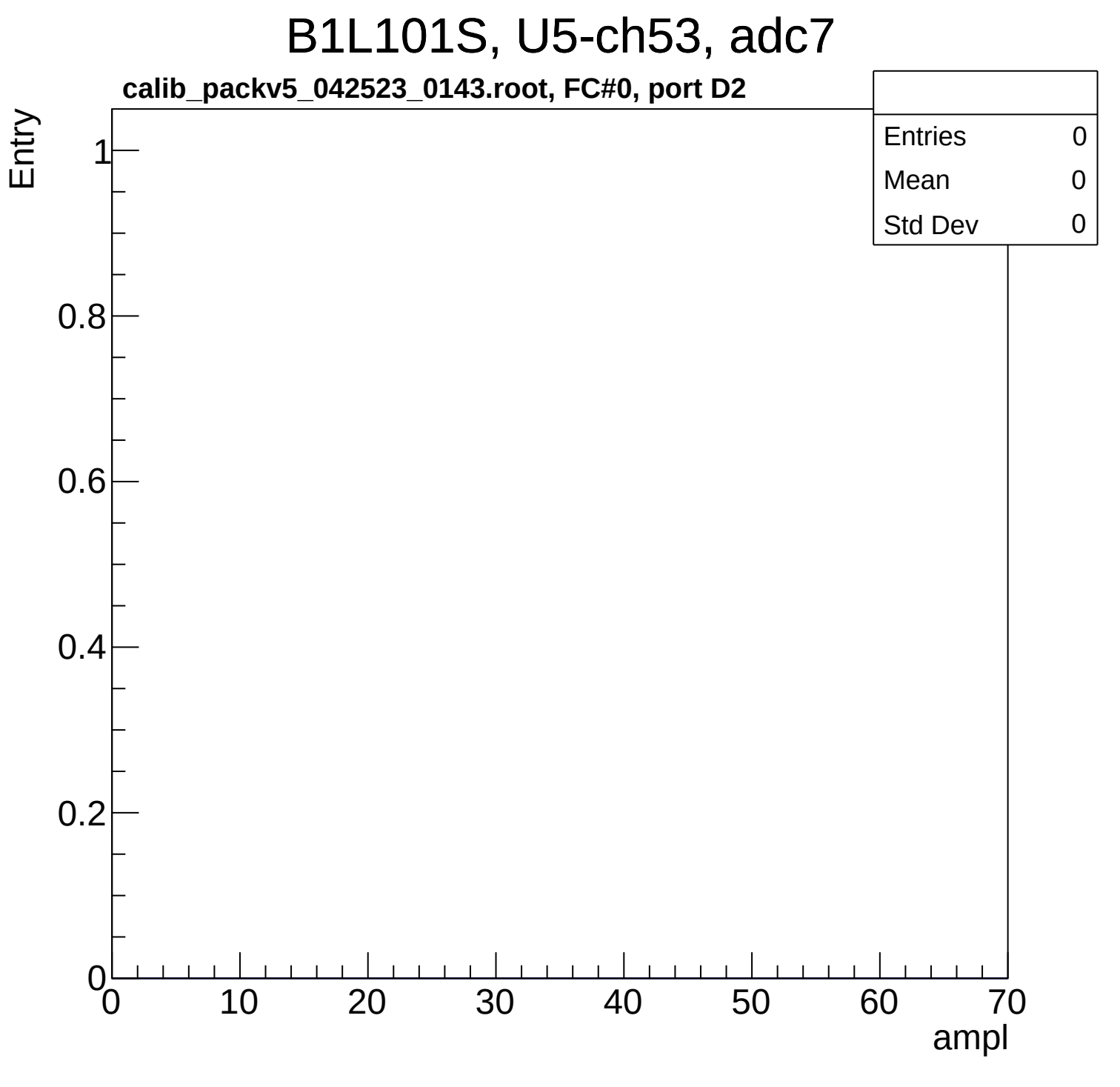
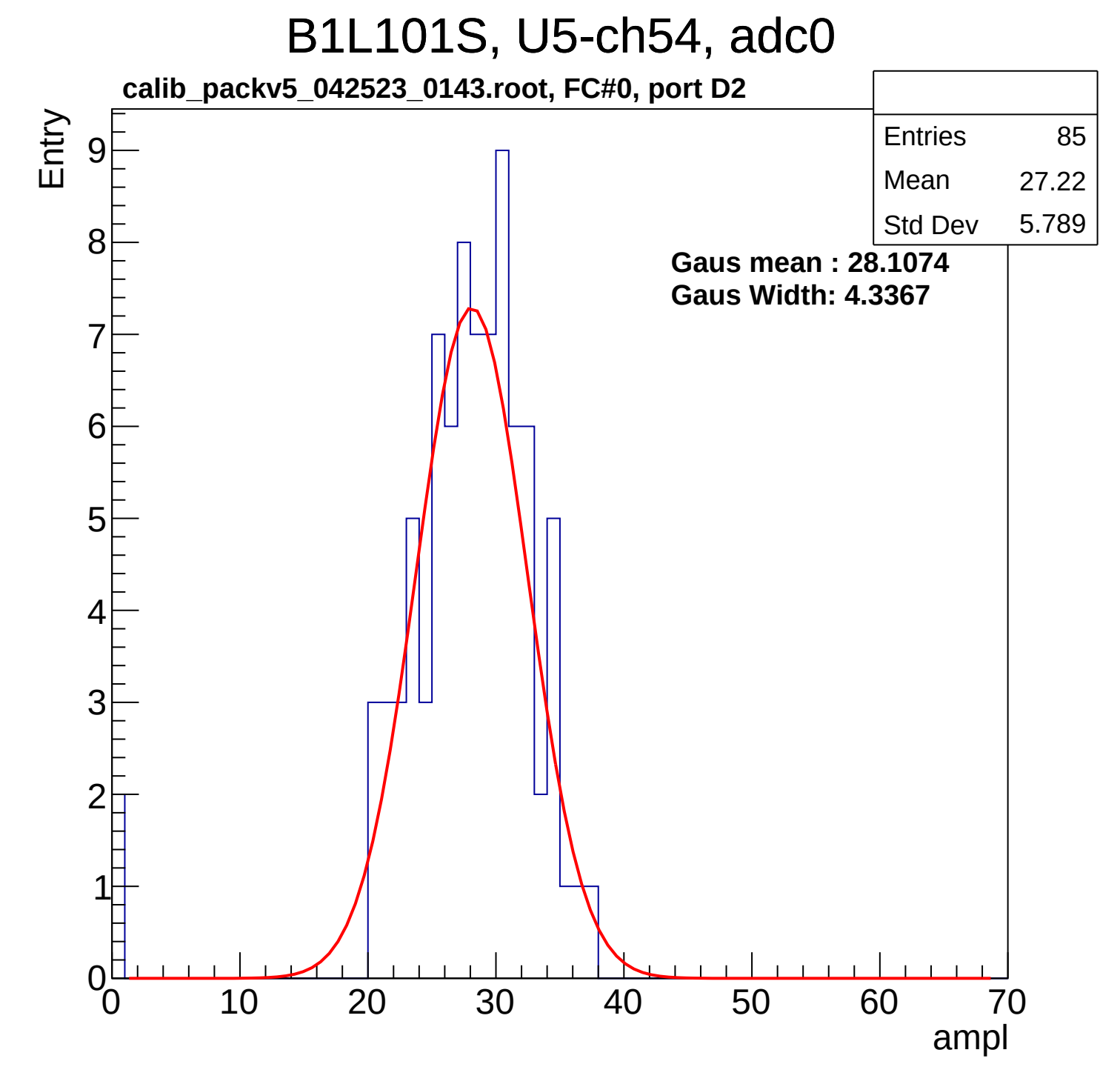

B1L101S, U5-ch53, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch54, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 85
Mean 27.22
Std Dev 5.789
Gaus mean : 28.1074
Gaus Width: 4.3367
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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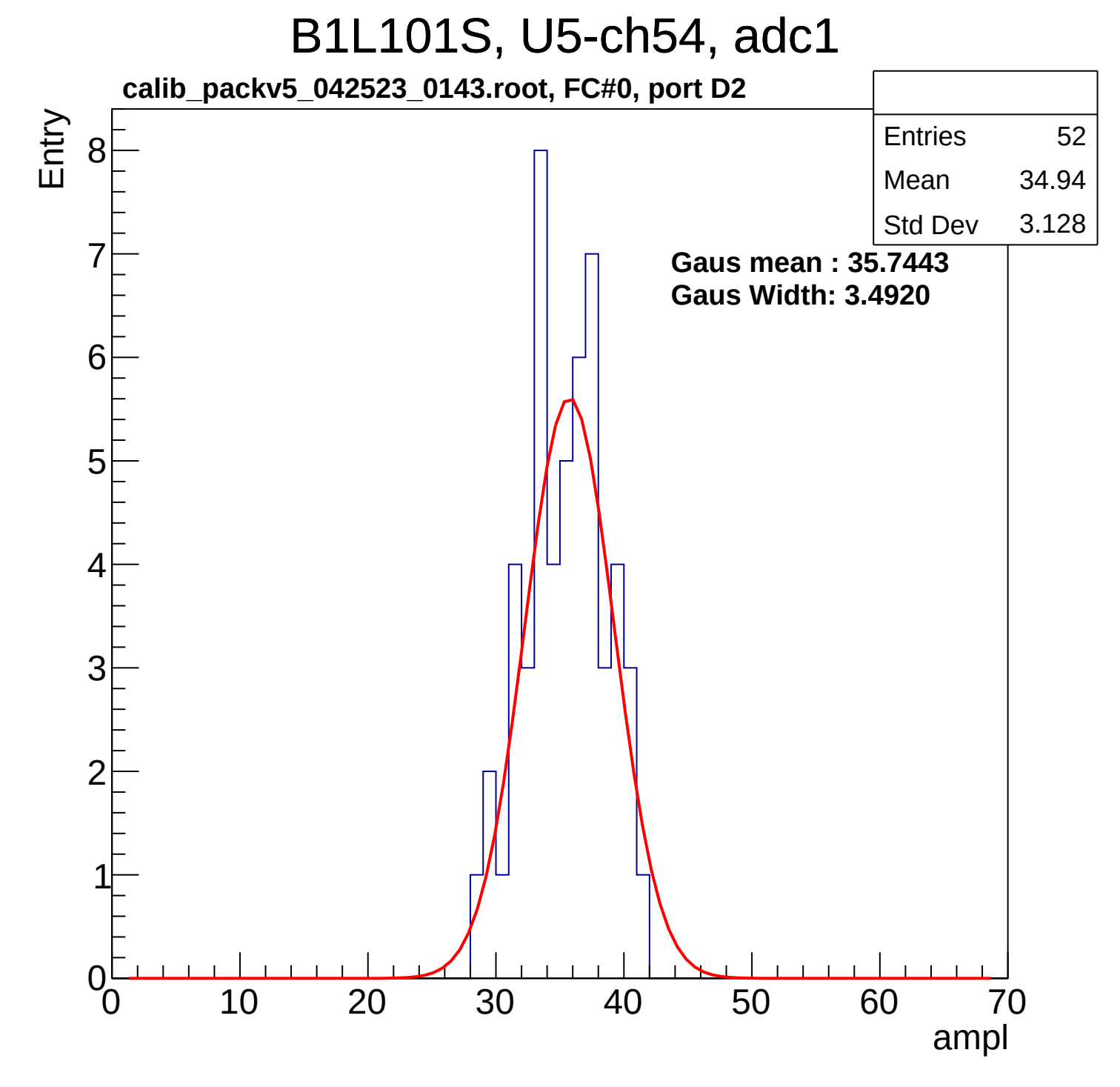
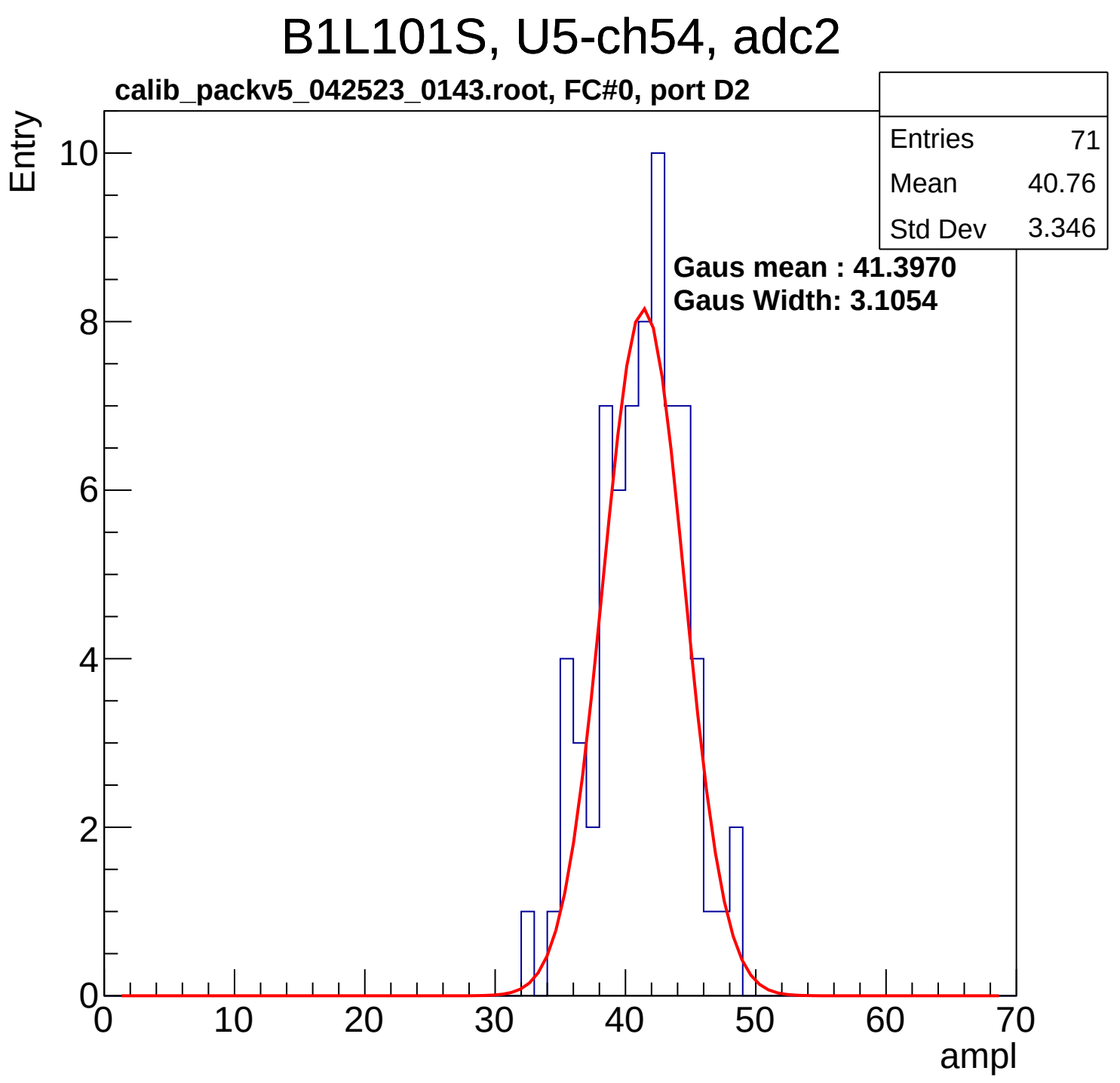
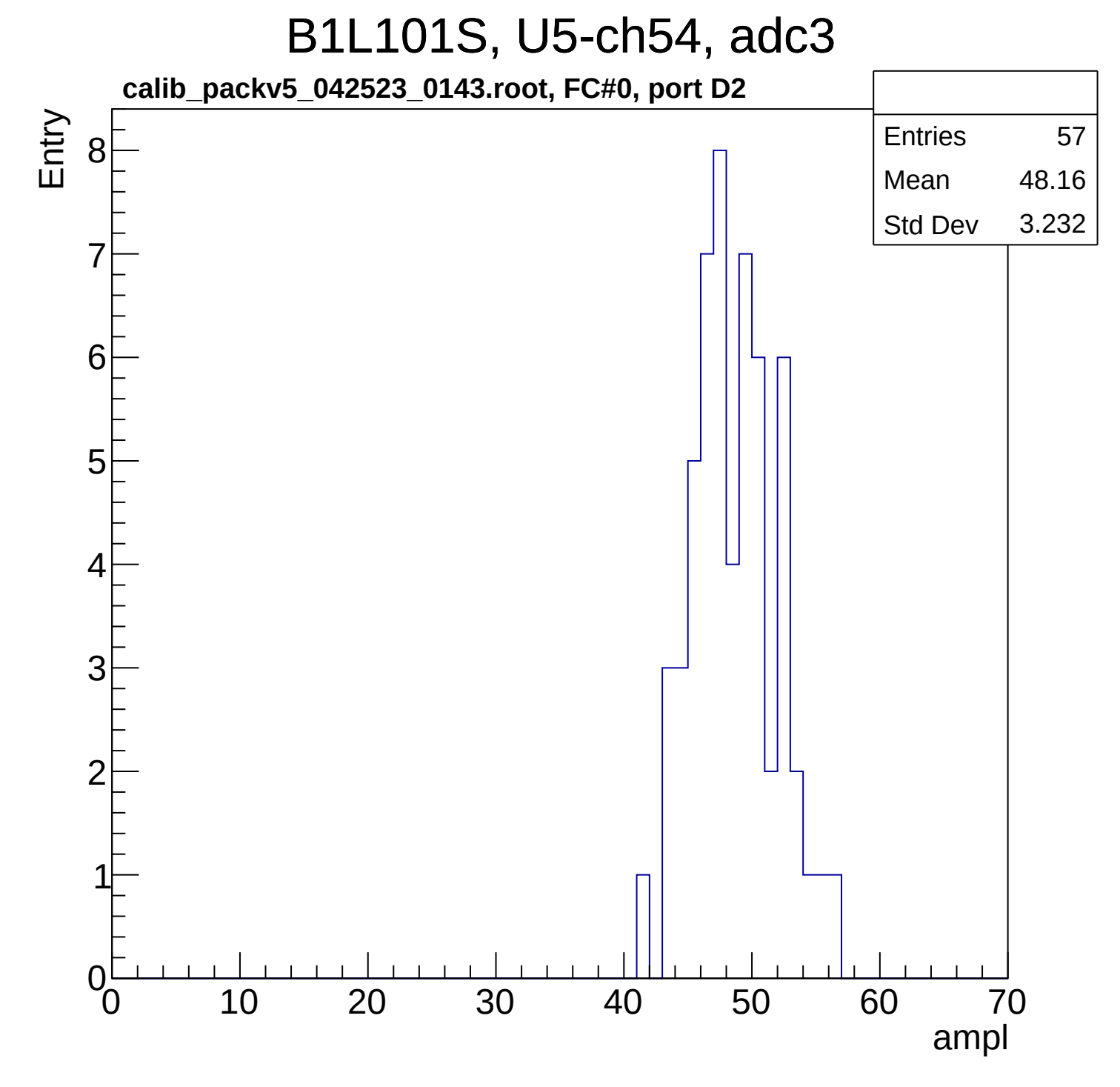
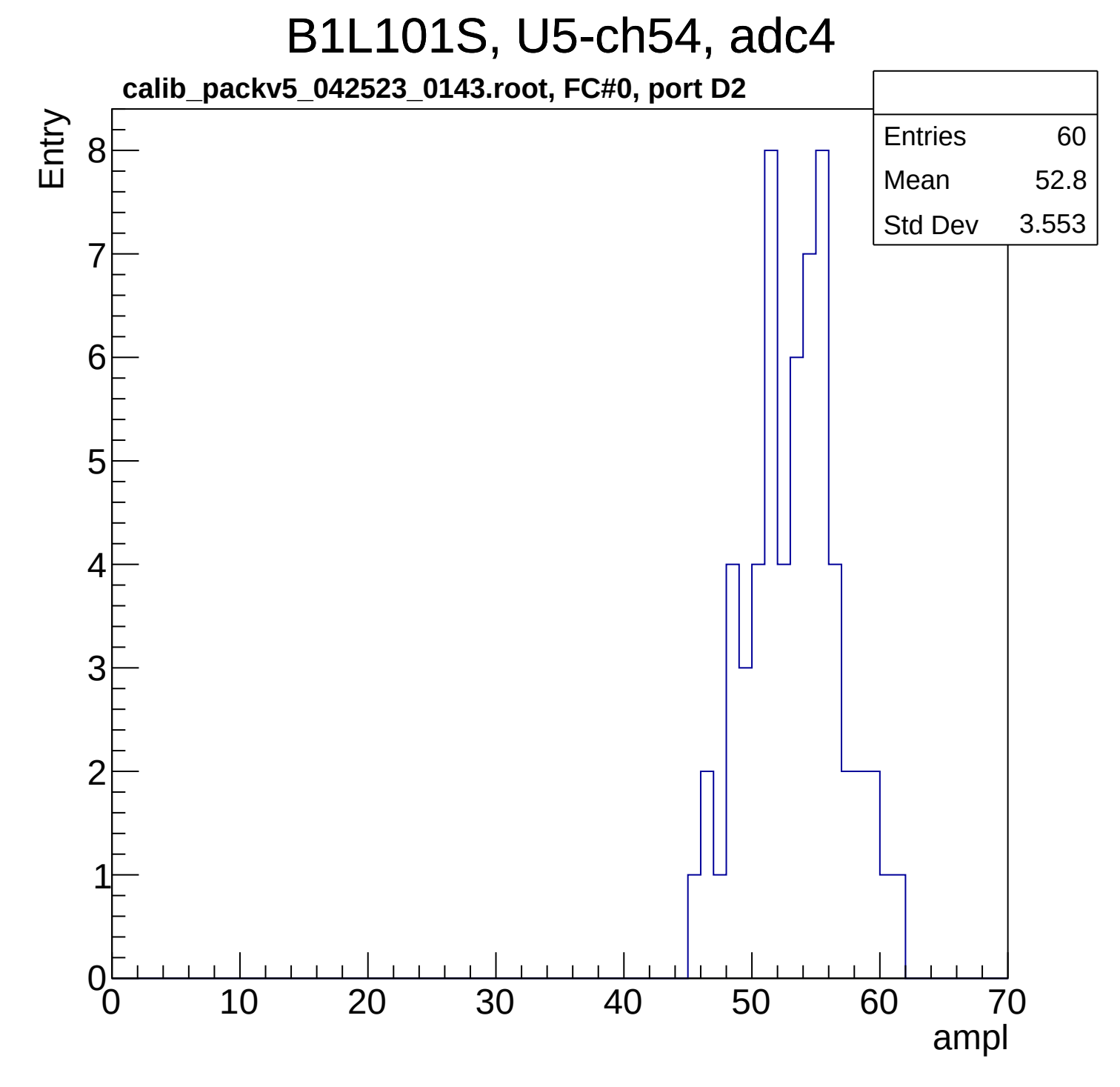

B1L101S, U5-ch54, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 34.94
Std Dev 3.128
Gaus mean : 35.7443
Gaus Width: 3.4920
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch54, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 40.76
Std Dev 3.346
Gaus mean : 41.3970
Gaus Width: 3.1054
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch54, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 48.16
Std Dev 3.232
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch54, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 52.8
Std Dev 3.553
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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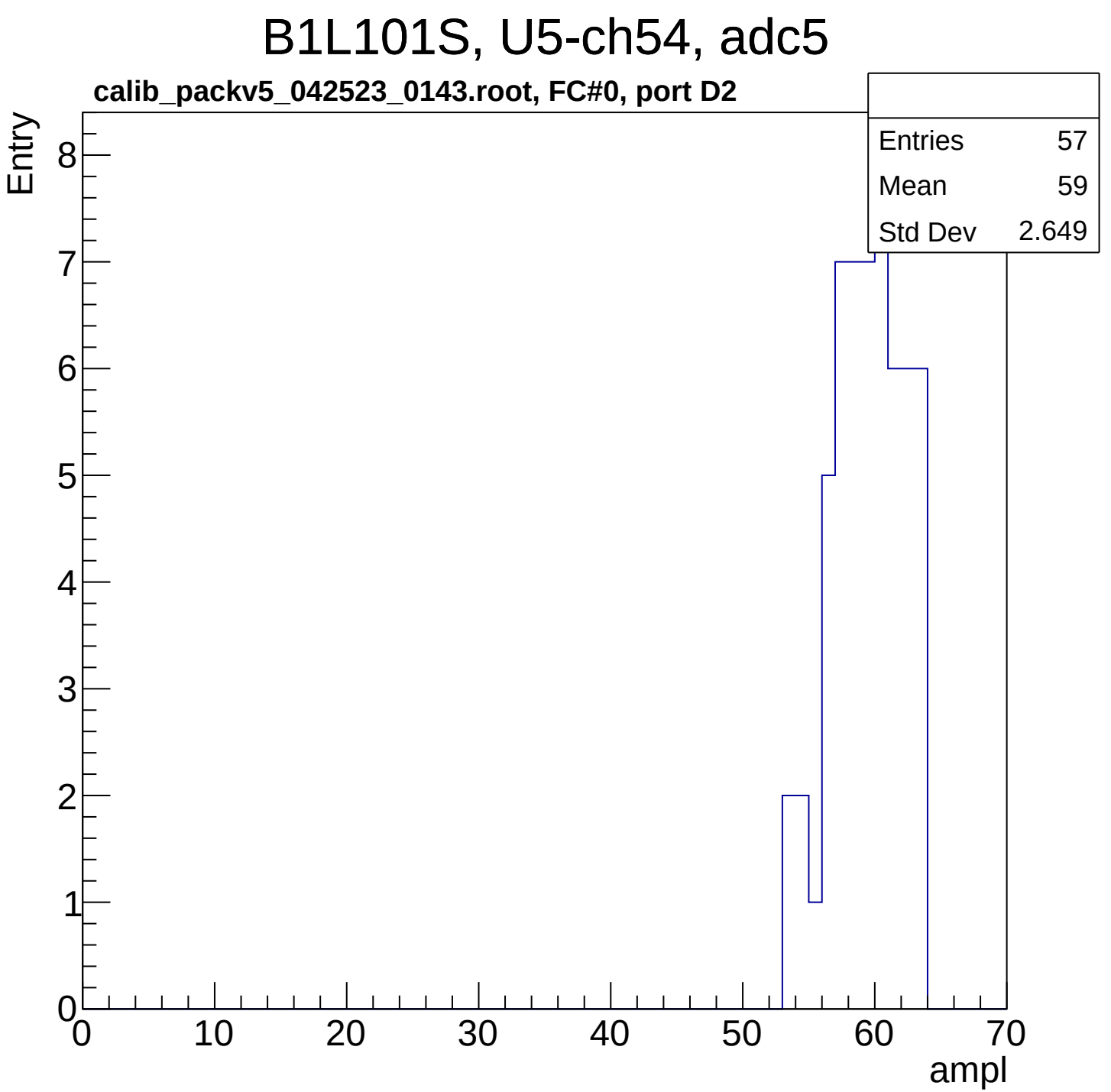
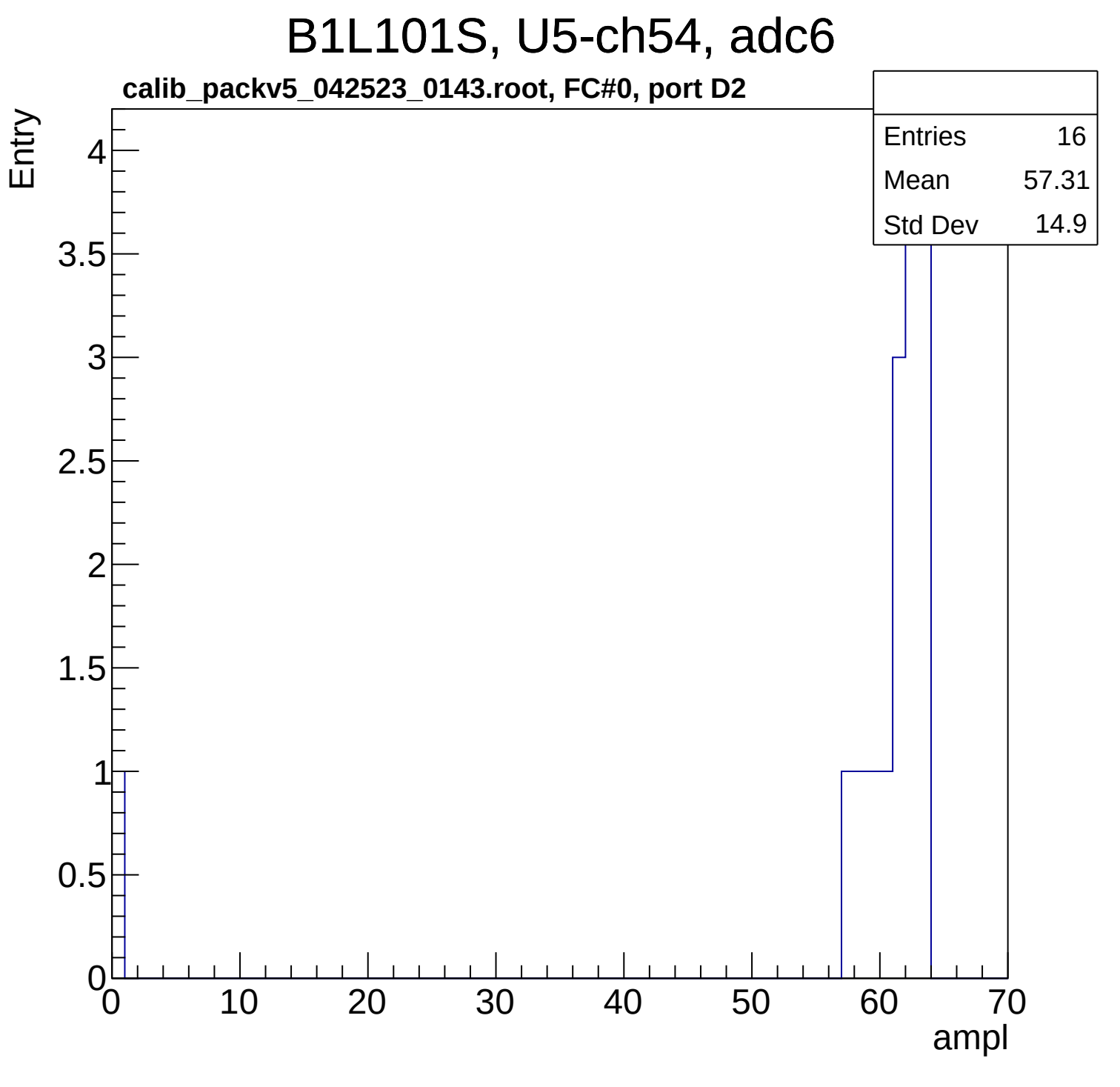

B1L101S, U5-ch54, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 59
Std Dev 2.649
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch54, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 16
Mean 57.31
Std Dev 14.9
Entry
ampl
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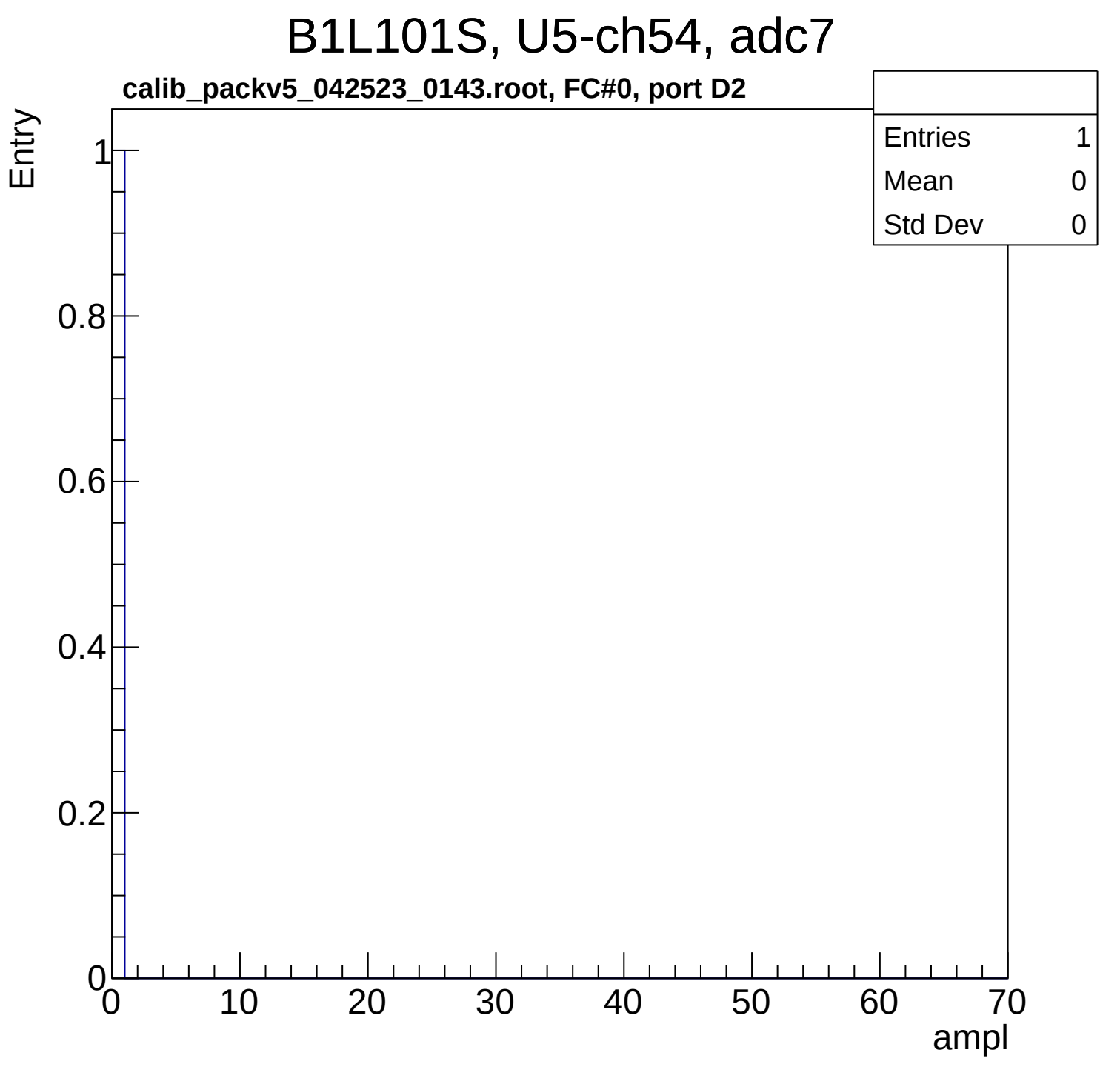
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L101S, U5-ch54, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
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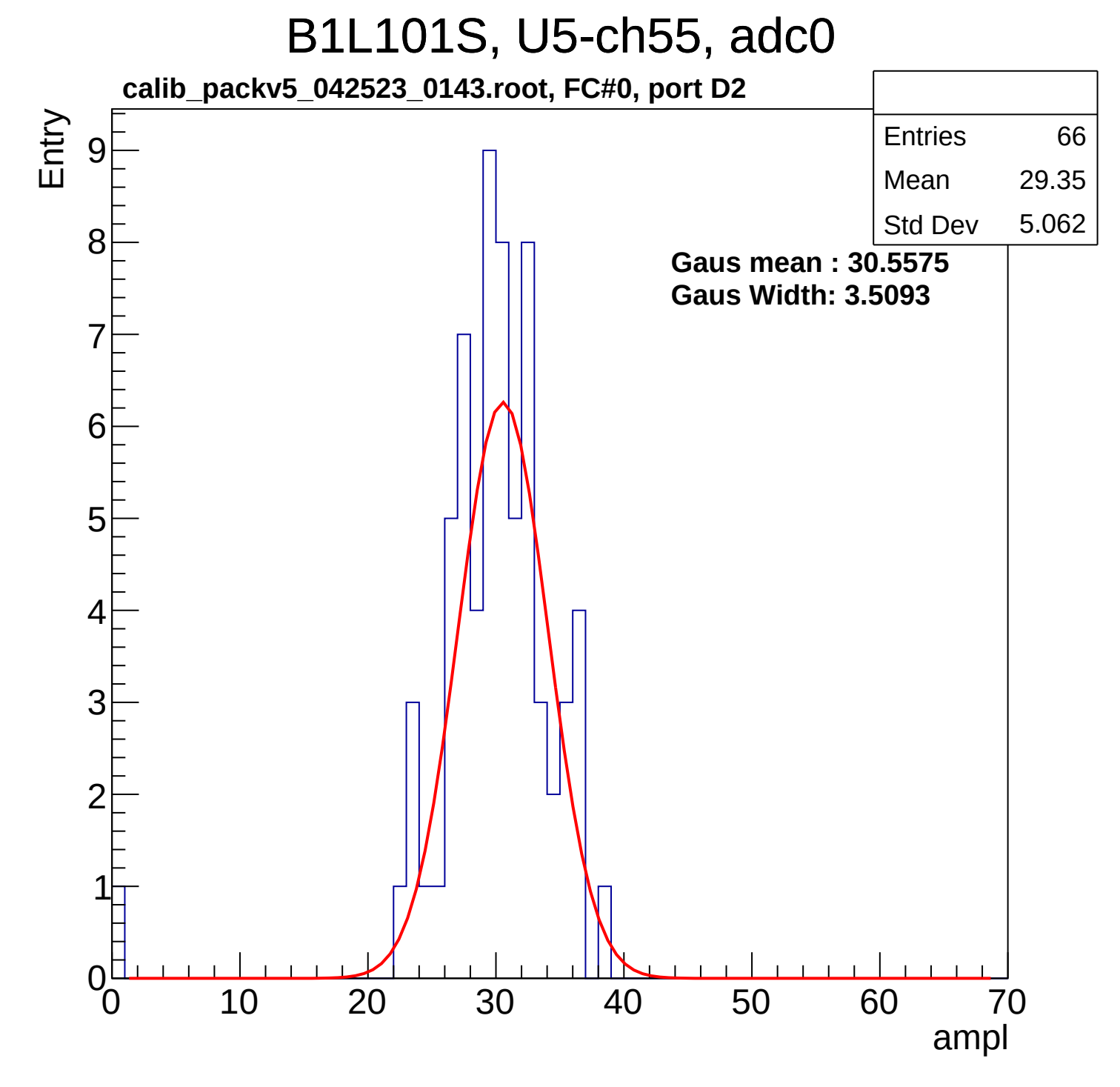
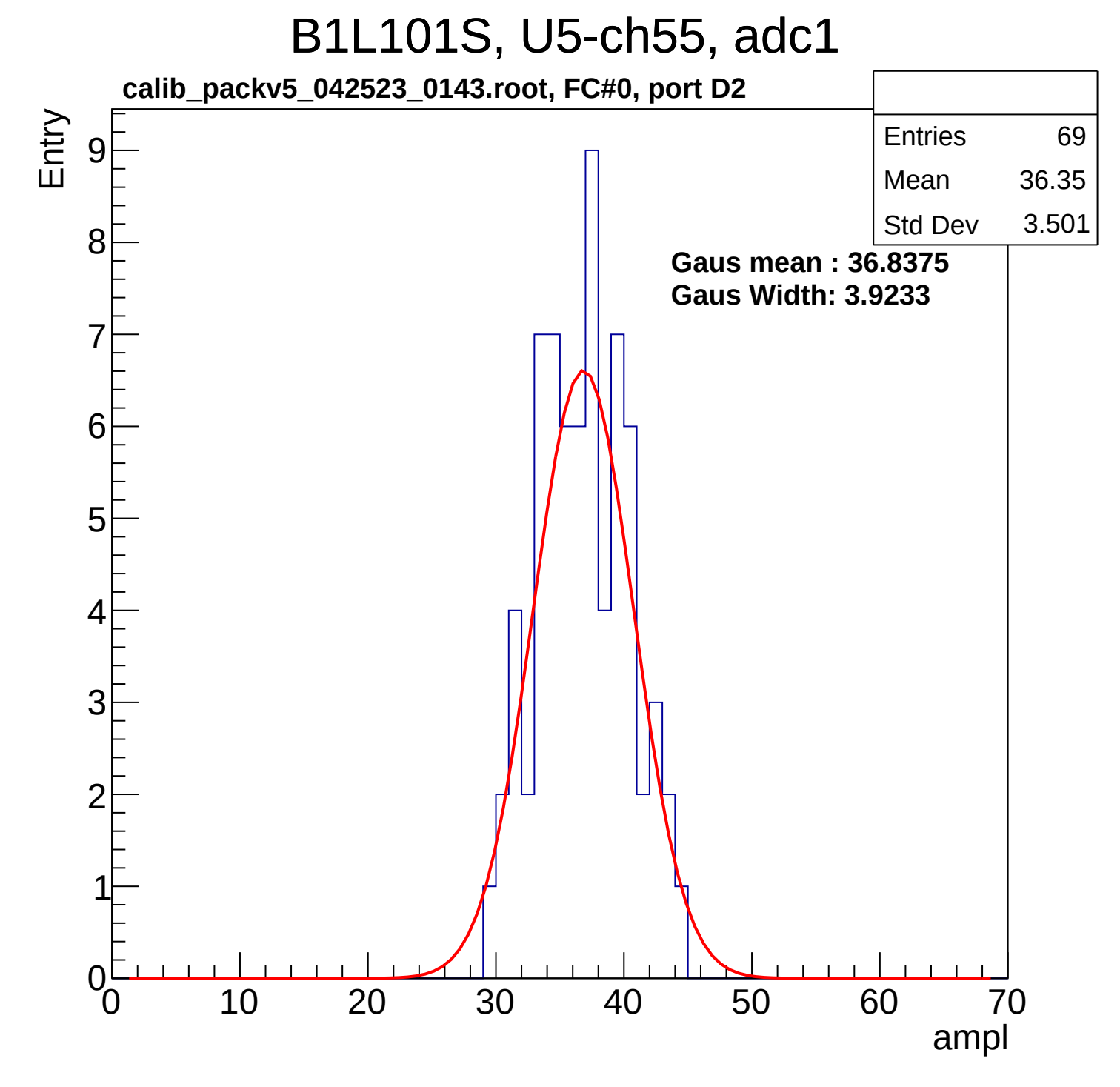
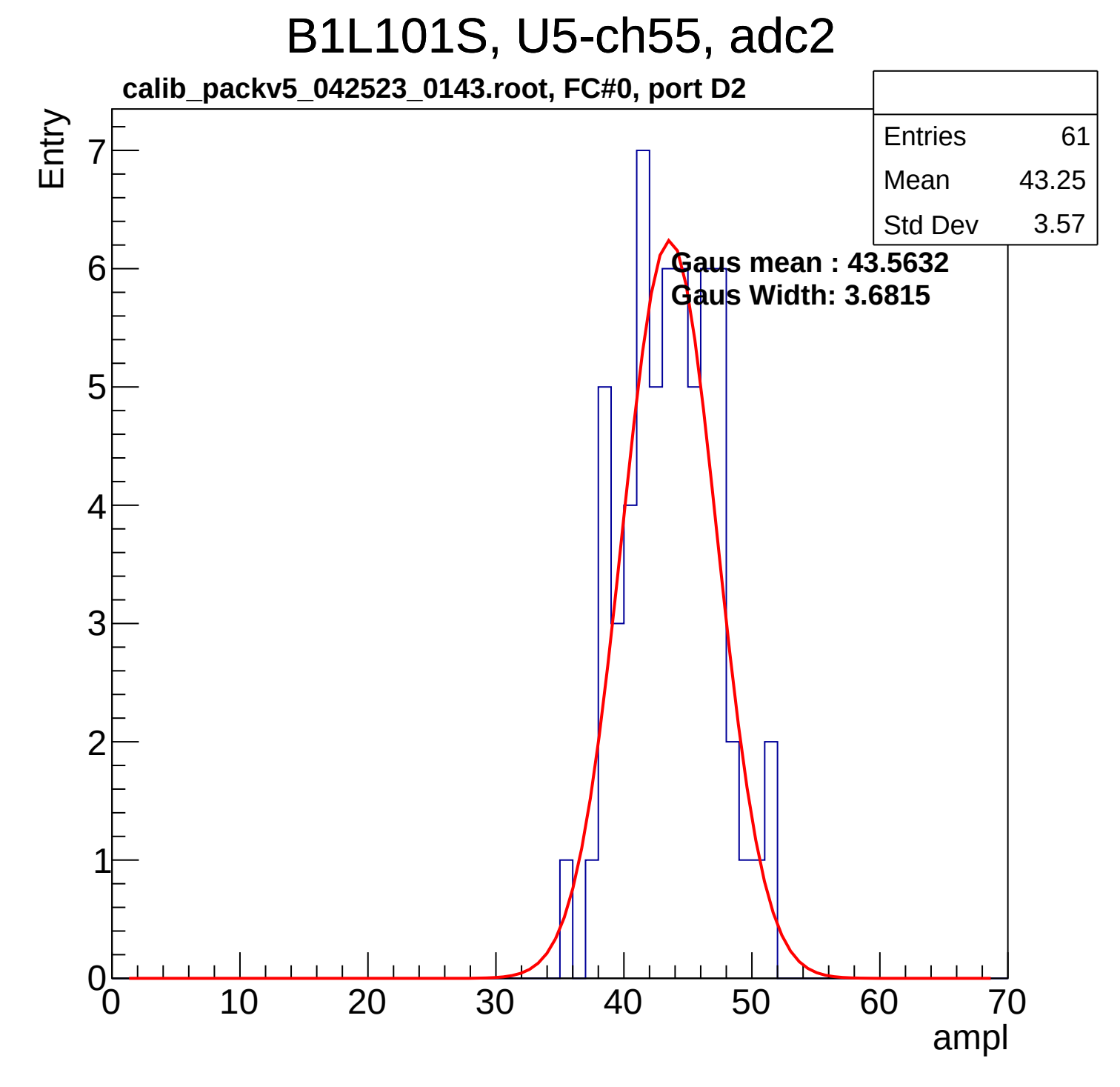
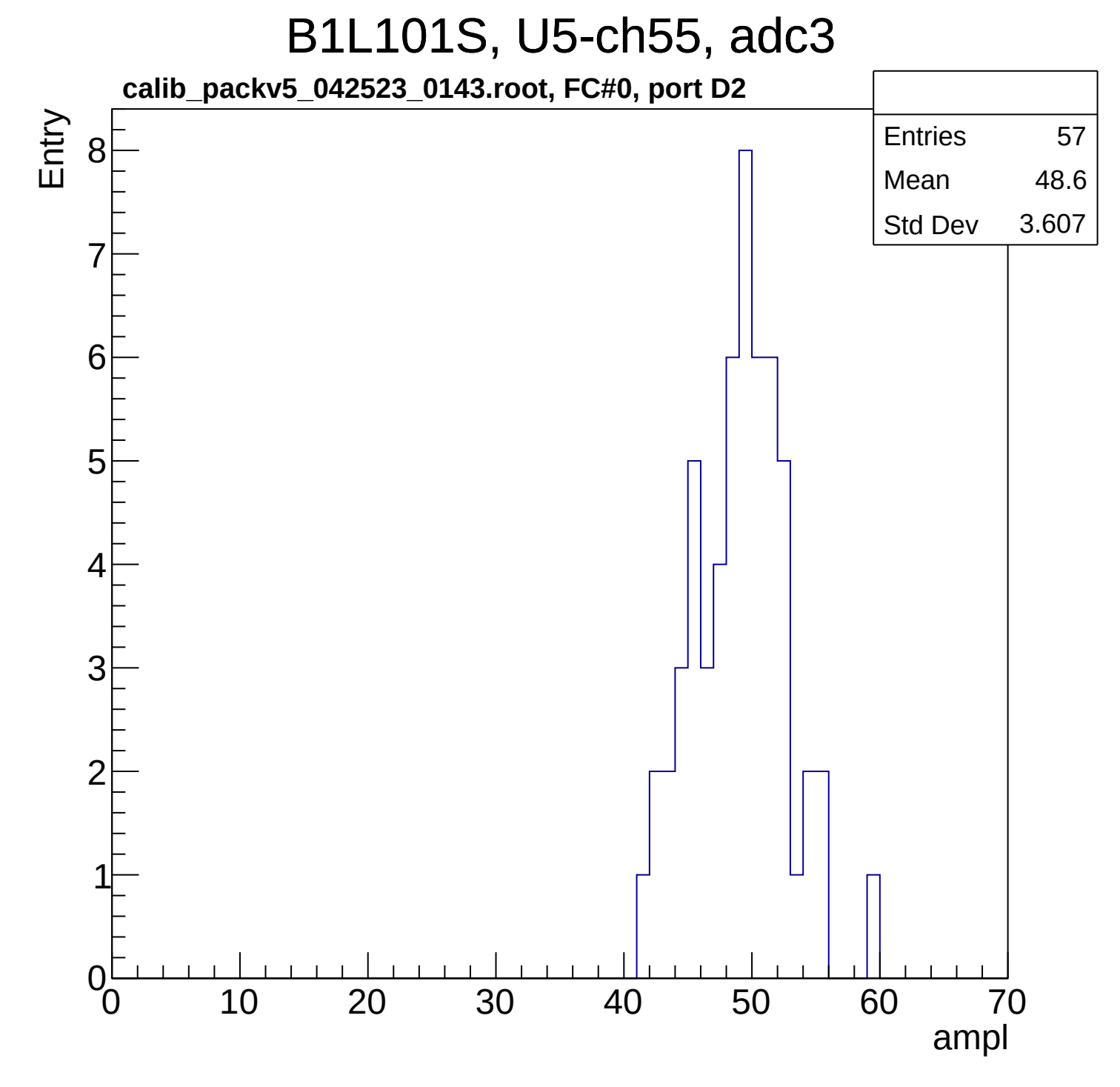
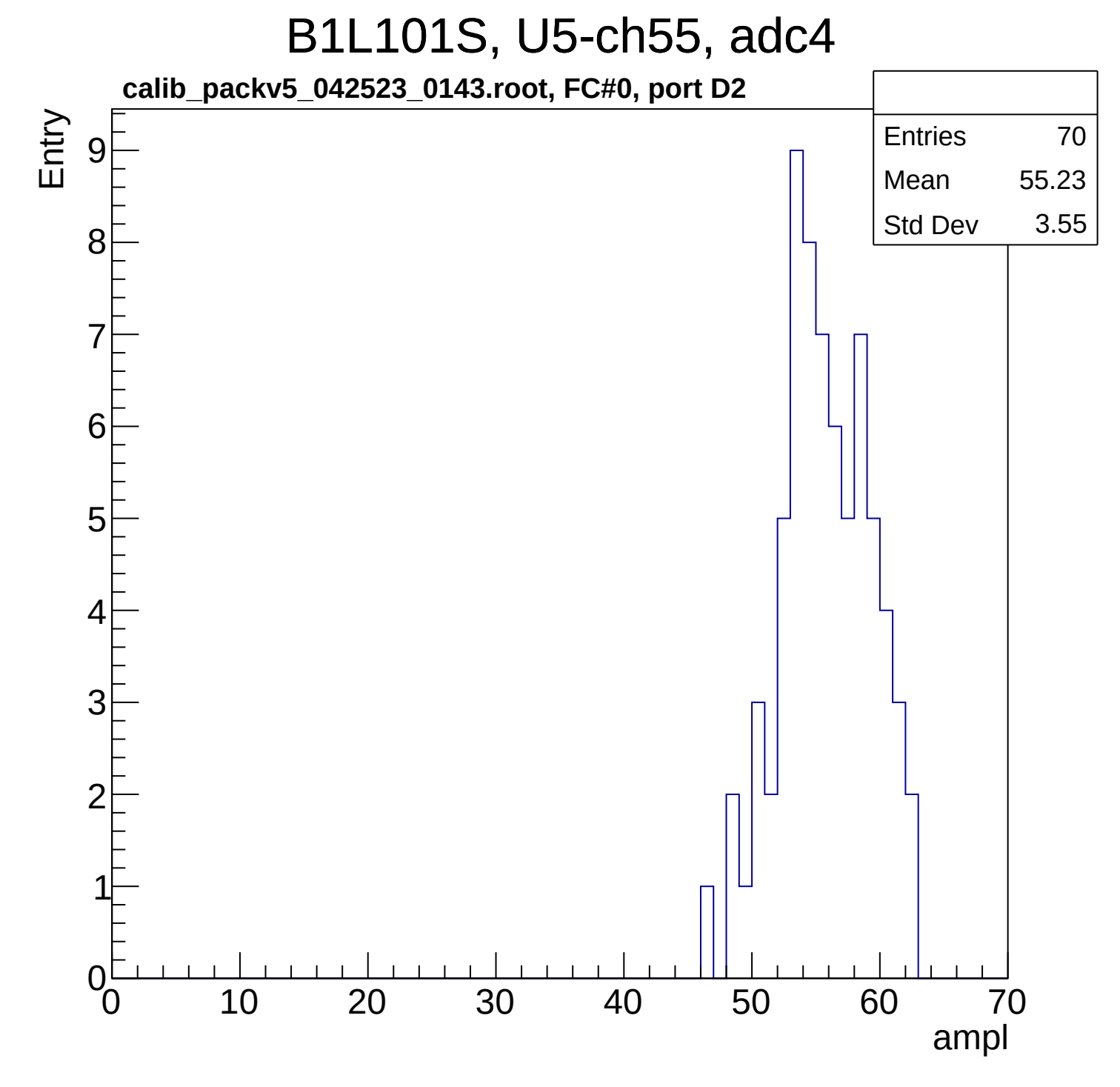
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

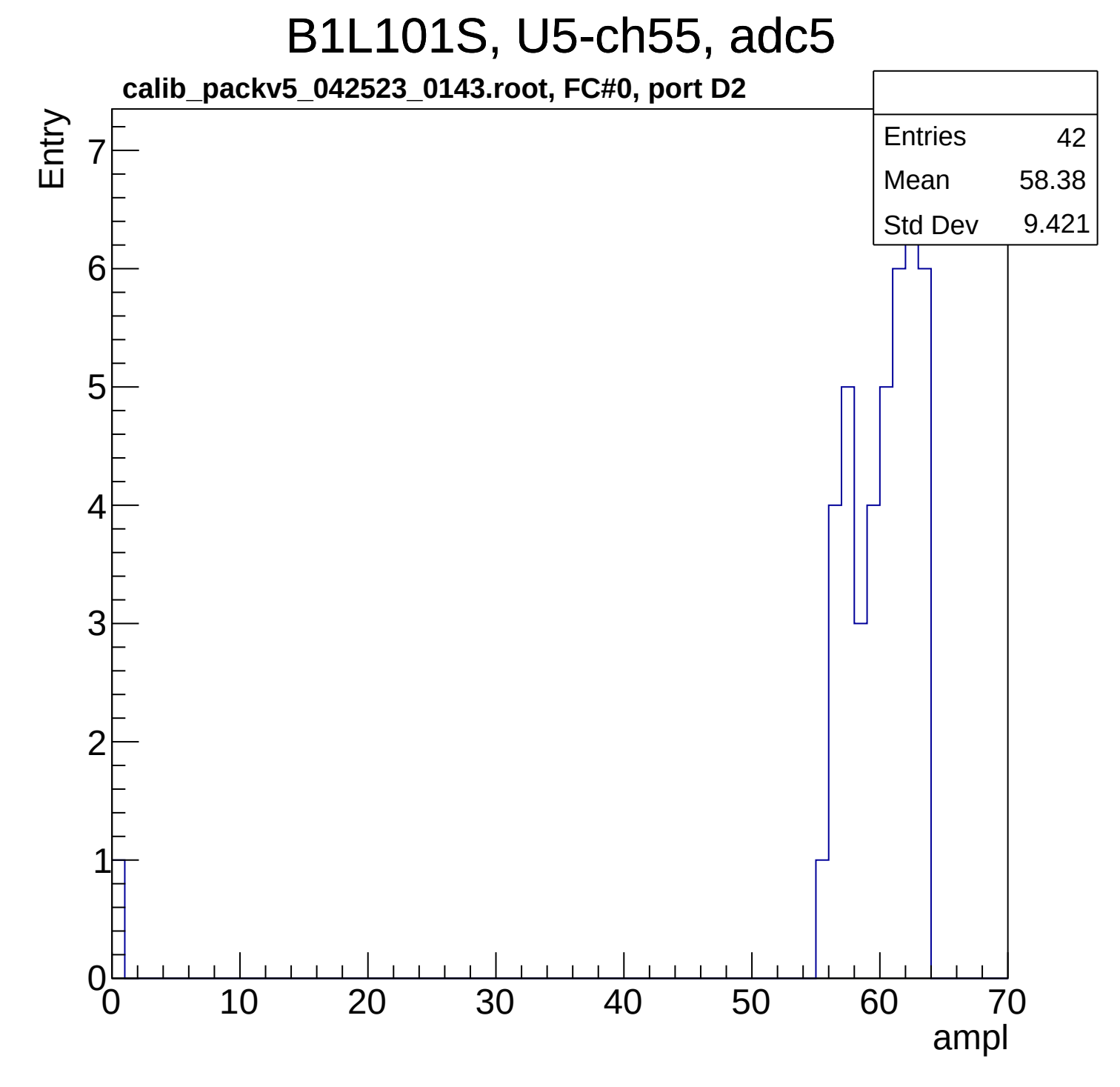

B1L101S, U5-ch55, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 29.35
Std Dev 5.062
Gaus mean : 30.5575
Gaus Width: 3.5093
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

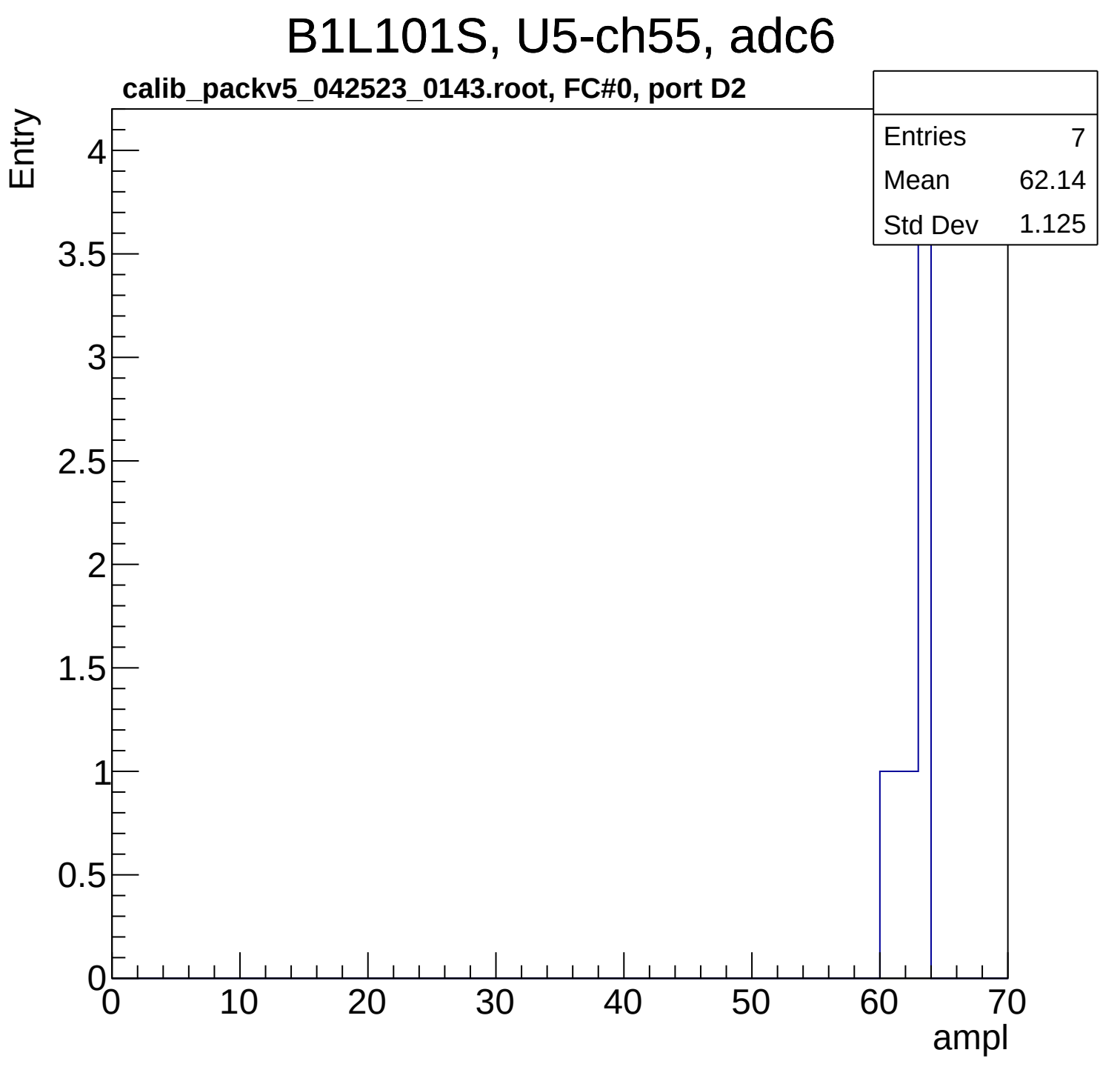

B1L101S, U5-ch55, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 36.35
Std Dev 3.501
Gaus mean : 36.8375
Gaus Width: 3.9233
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

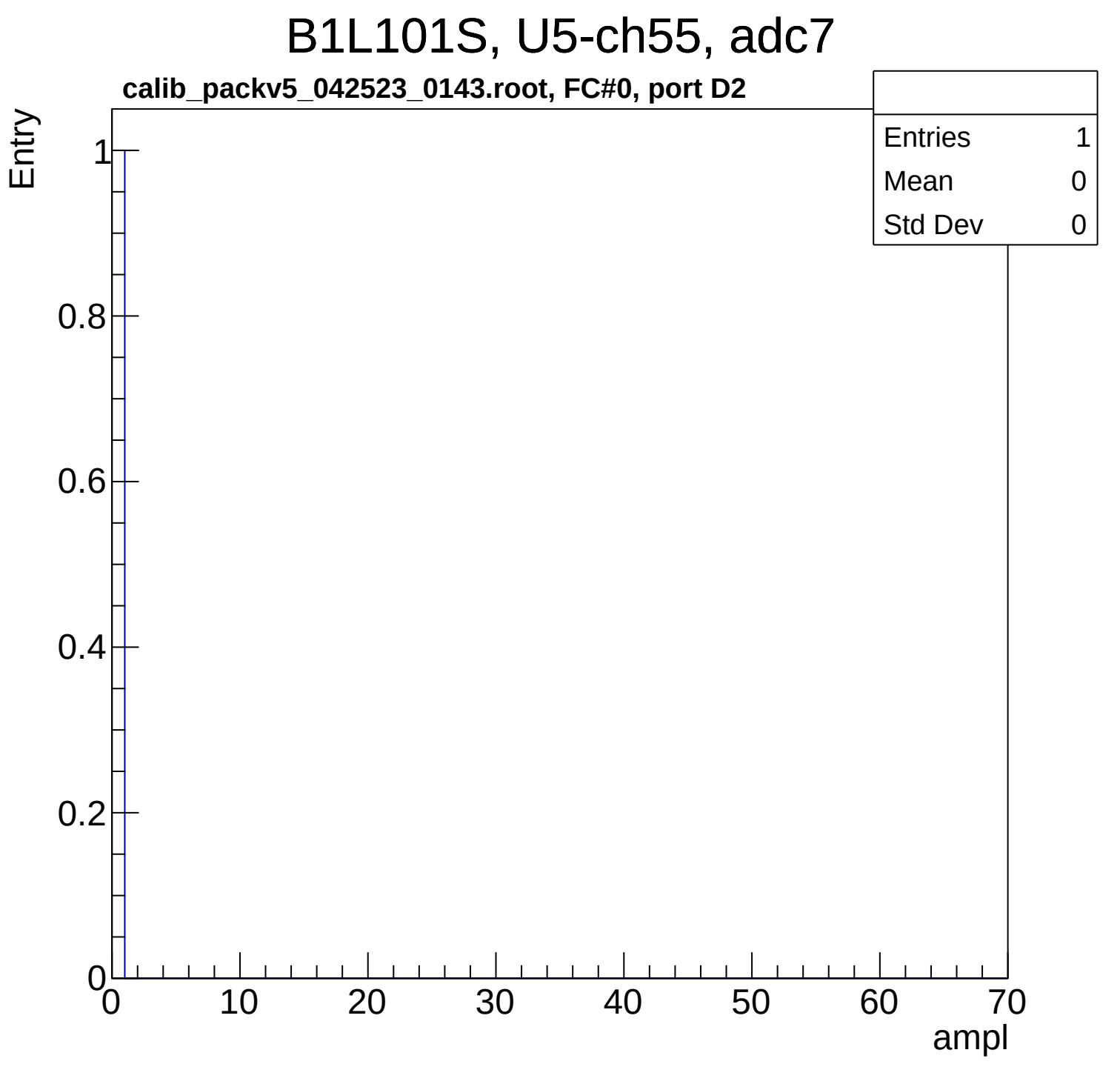

B1L101S, U5-ch55, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 43.25
Std Dev 3.57
Gaus mean : 43.5632
Gaus Width: 3.6815
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

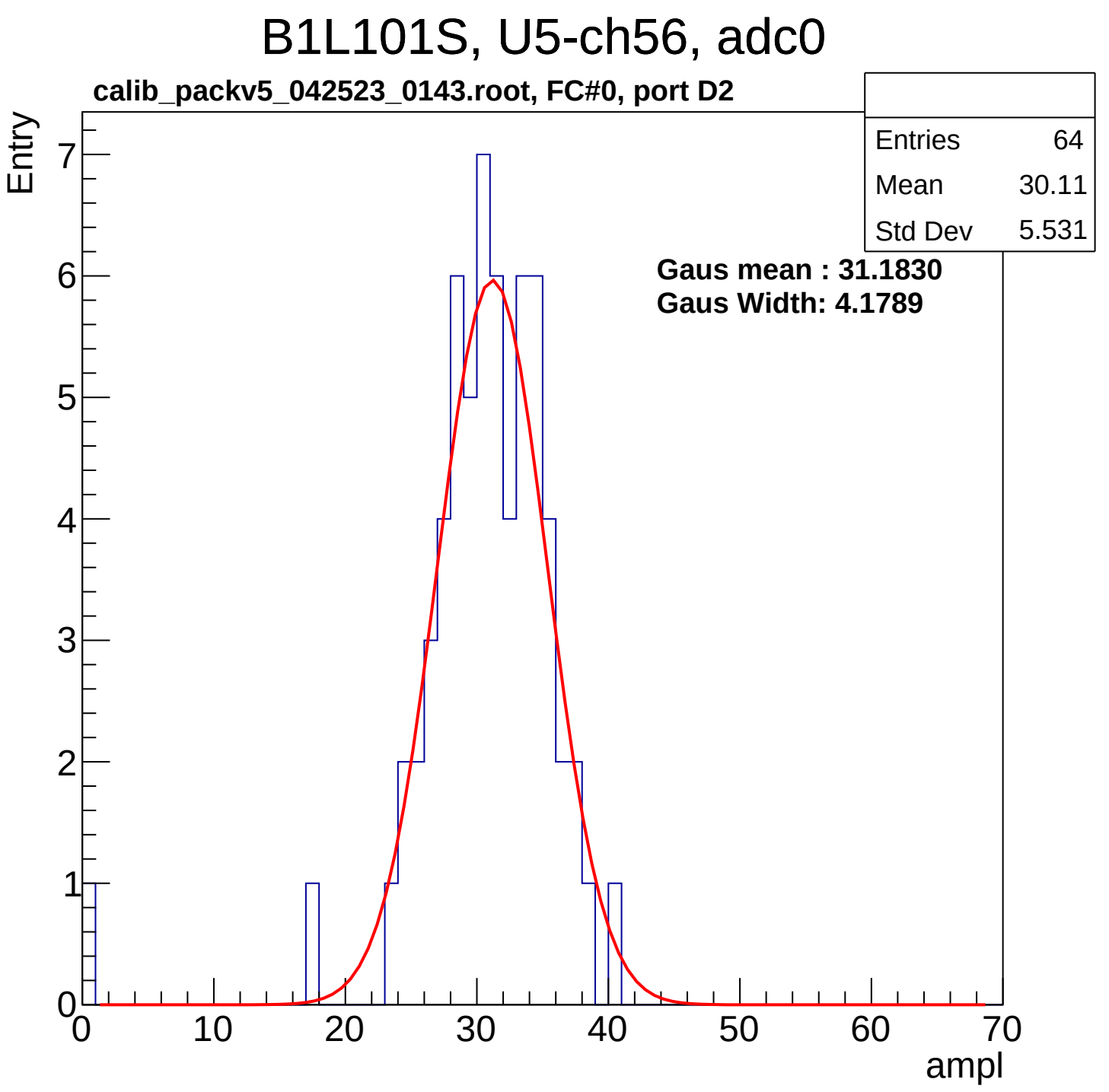

B1L101S, U5-ch55, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 48.6
Std Dev 3.607
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

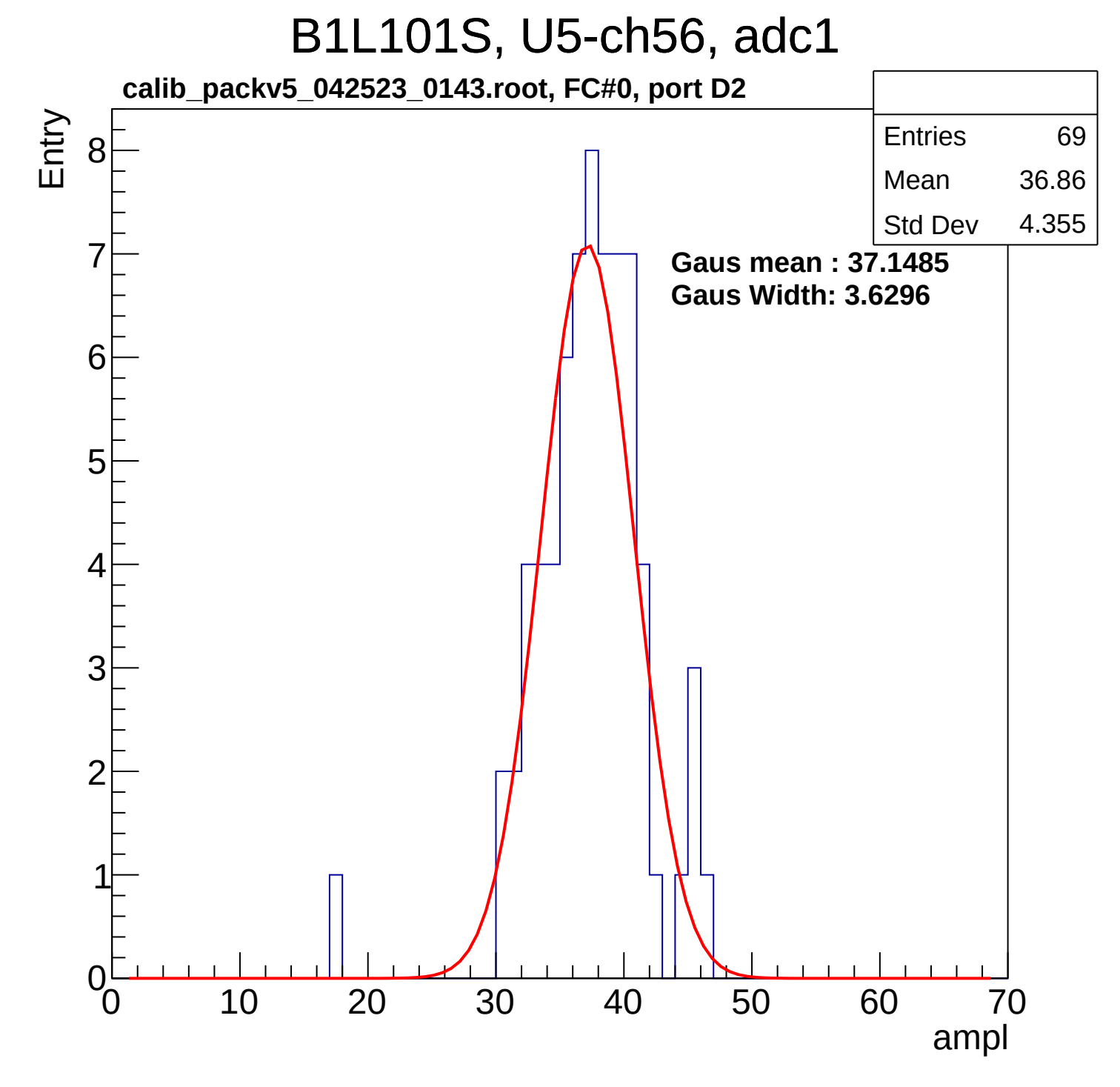

B1L101S, U5-ch55, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 55.23
Std Dev 3.55
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch55, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 58.38
Std Dev 9.421
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch55, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 62.14
Std Dev 1.125
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L101S, U5-ch55, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch56, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 30.11
Std Dev 5.531
Gaus mean : 31.1830
Gaus Width: 4.1789
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch56, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 36.86
Std Dev 4.355
Gaus mean : 37.1485
Gaus Width: 3.6296
Entry
ampl
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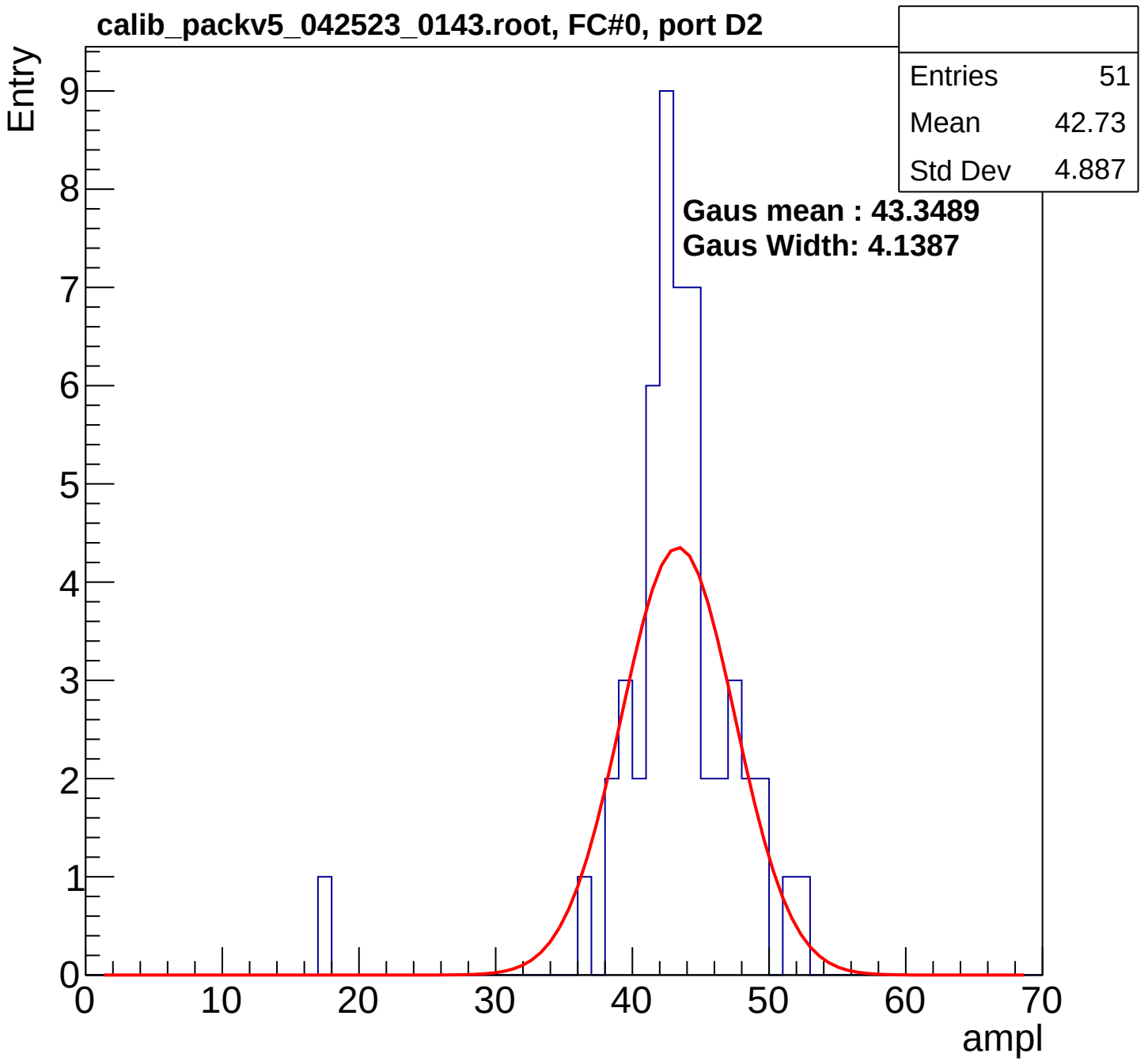
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch56, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 42.73
Std Dev 4.887
Gaus mean : 43.3489
Gaus Width: 4.1387
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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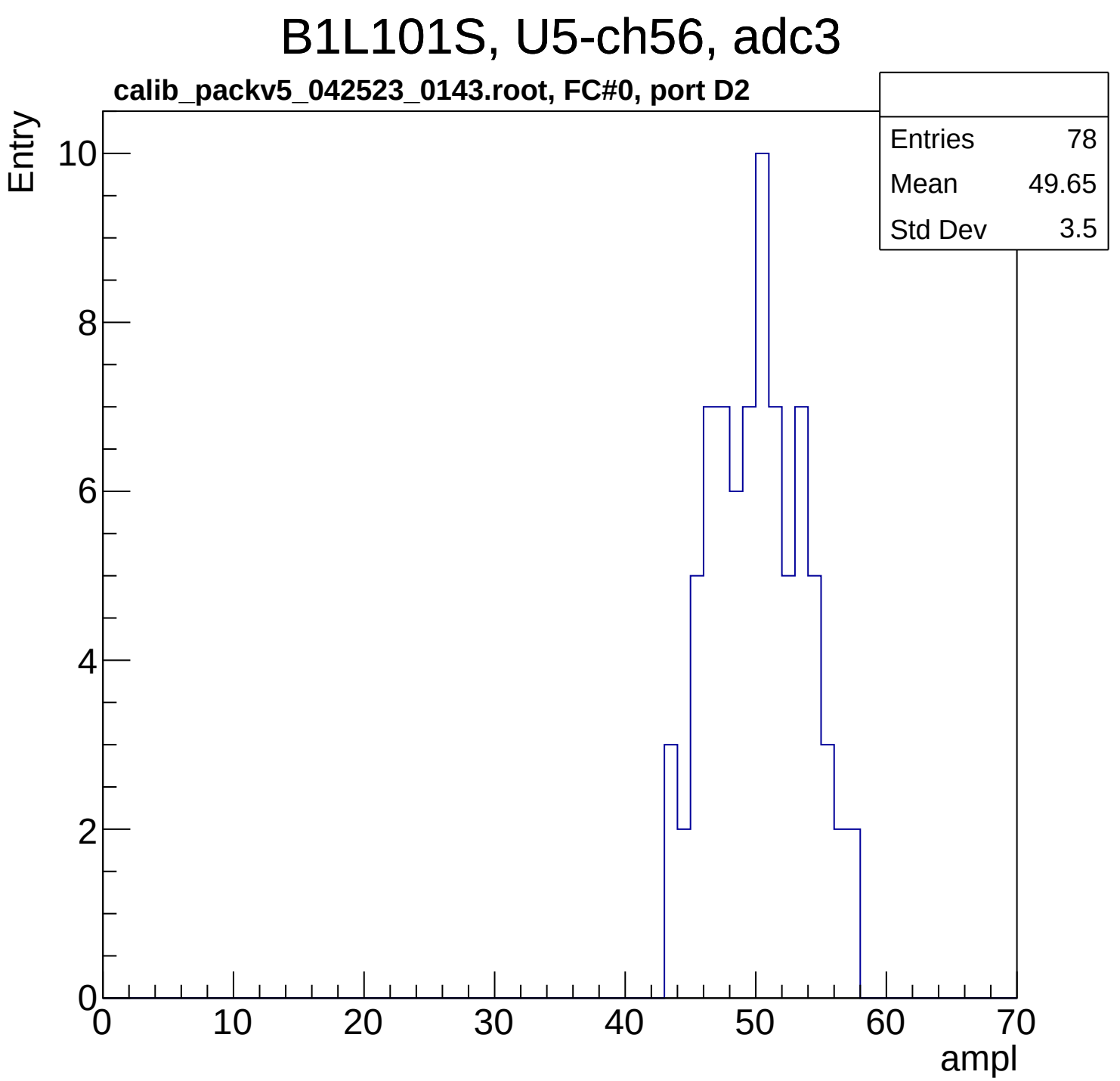
60
70


B1L101S, U5-ch56, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 49.65
Std Dev 3.5
Entry
0
2
4
6
8
10
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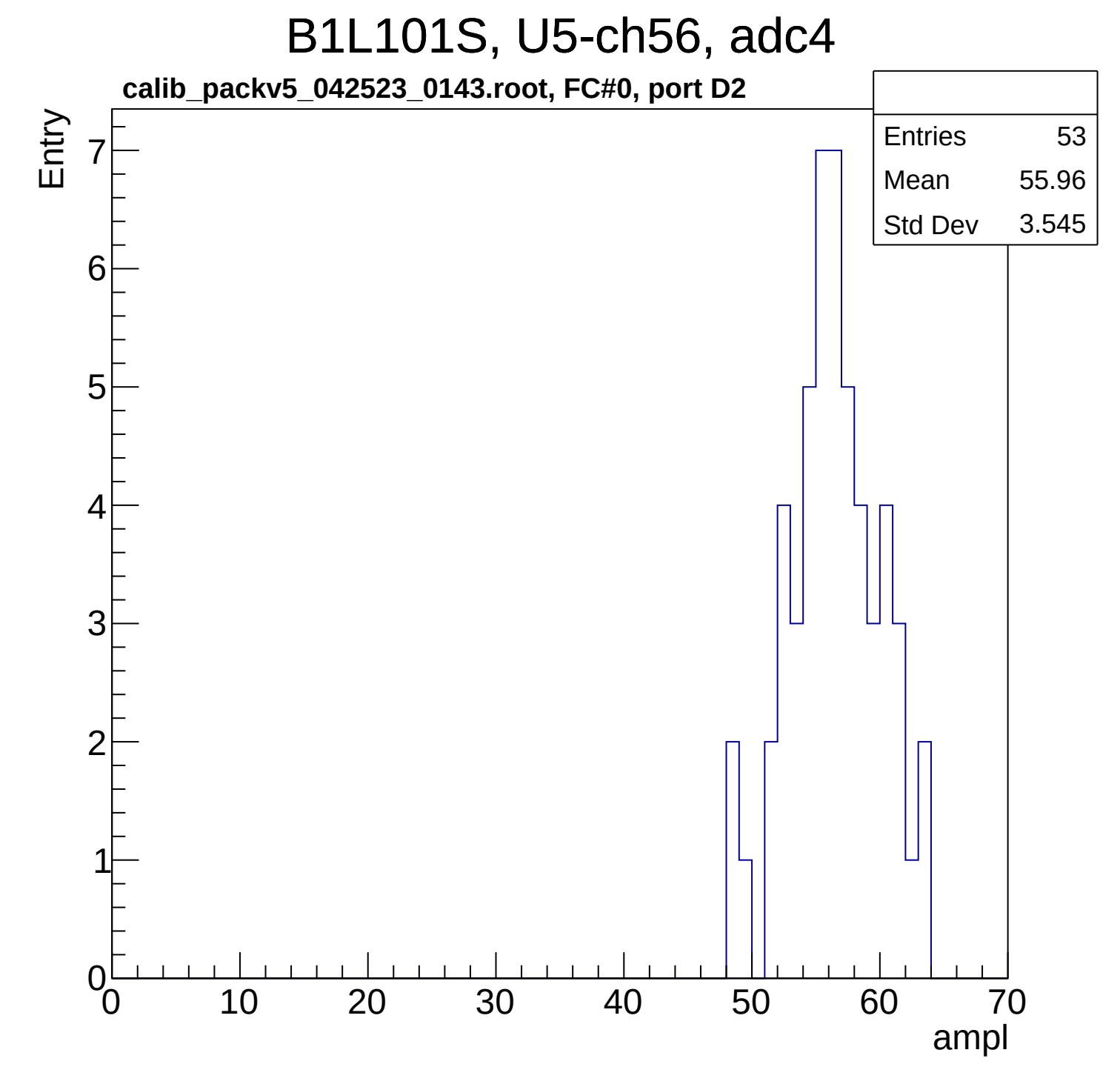
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch56, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 55.96
Std Dev 3.545
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
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60
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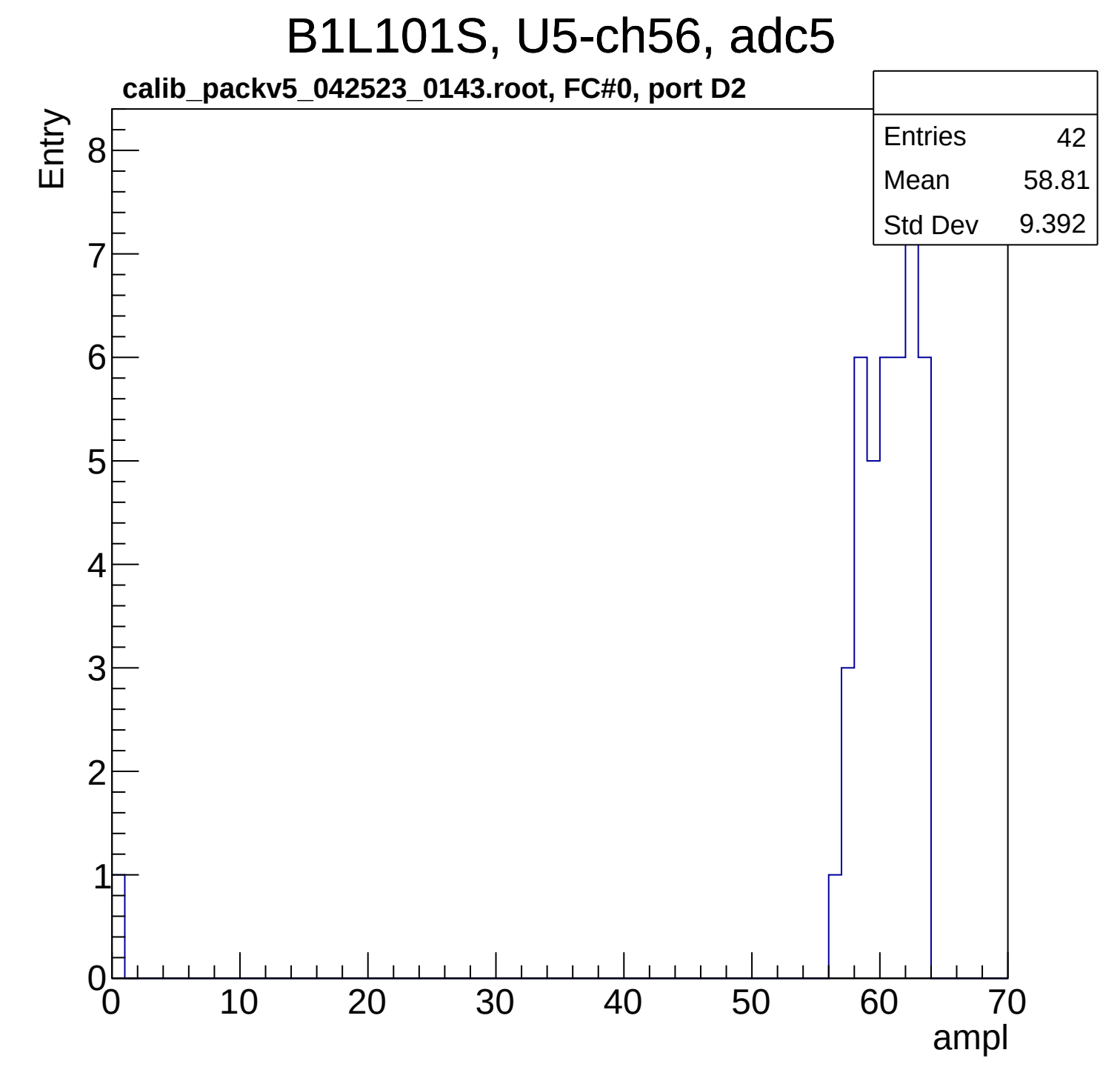
B1L101S, U5-ch56, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 58.81
Std Dev 9.392
Entry
ampl
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1
2
3
4
5
6
7
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0
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60
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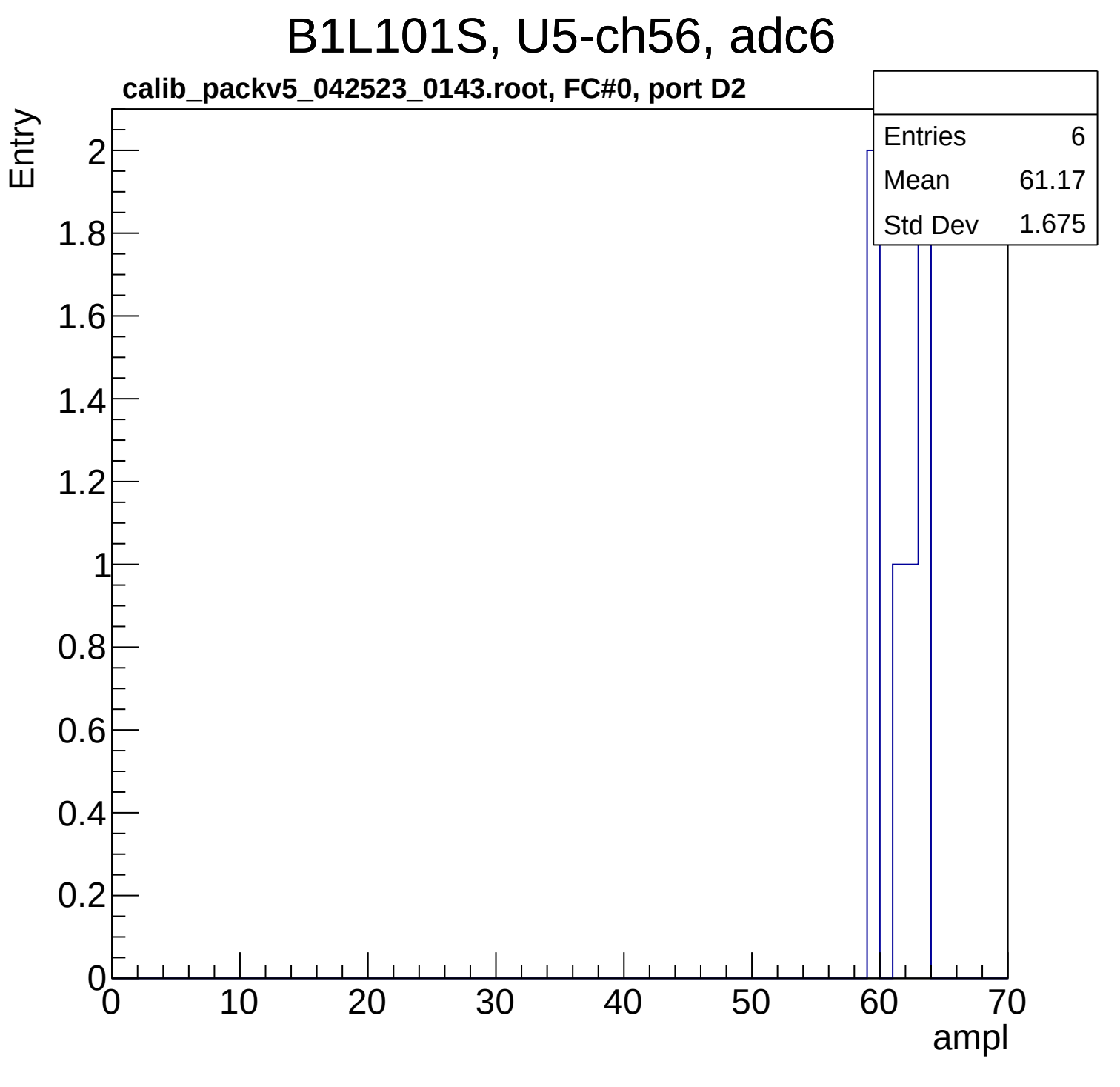
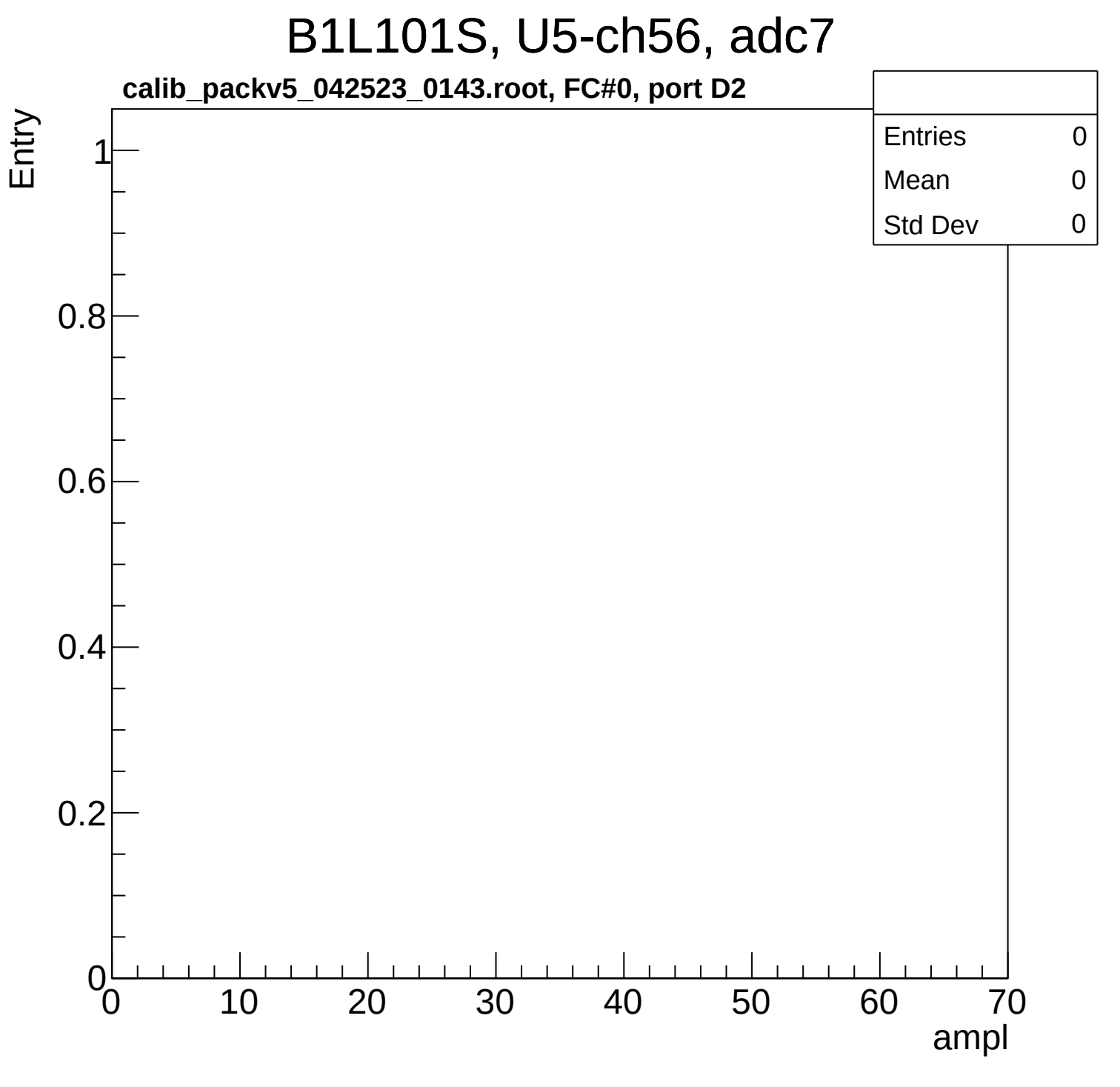

B1L101S, U5-ch56, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 61.17
Std Dev 1.675
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U5-ch56, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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0.8
0.6
0.4
0.2
0
0
10
20
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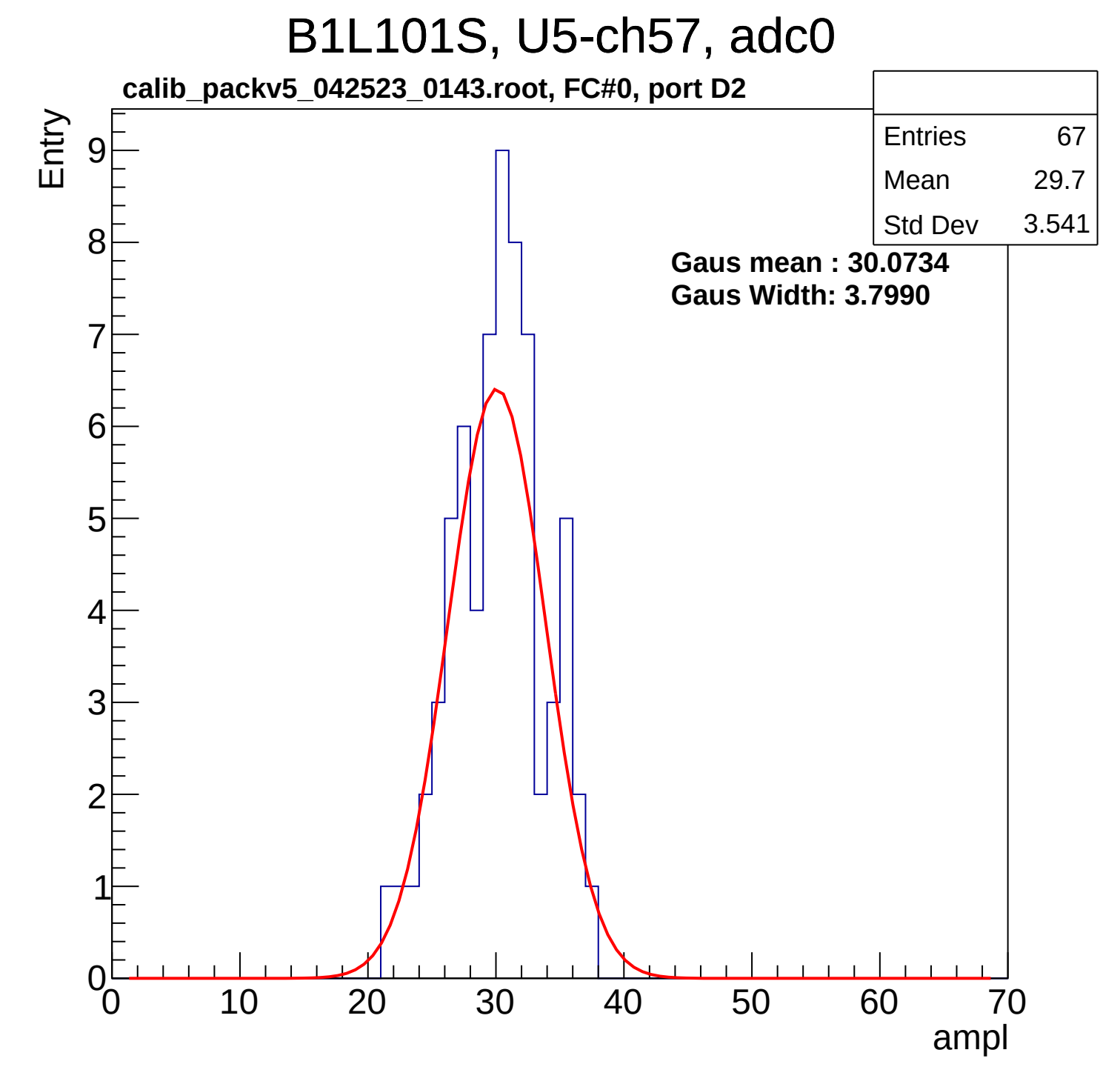
50
60
70
ampl


B1L101S, U5-ch57, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 29.7
Std Dev 3.541
Gaus mean : 30.0734
Gaus Width: 3.7990
Entry
ampl
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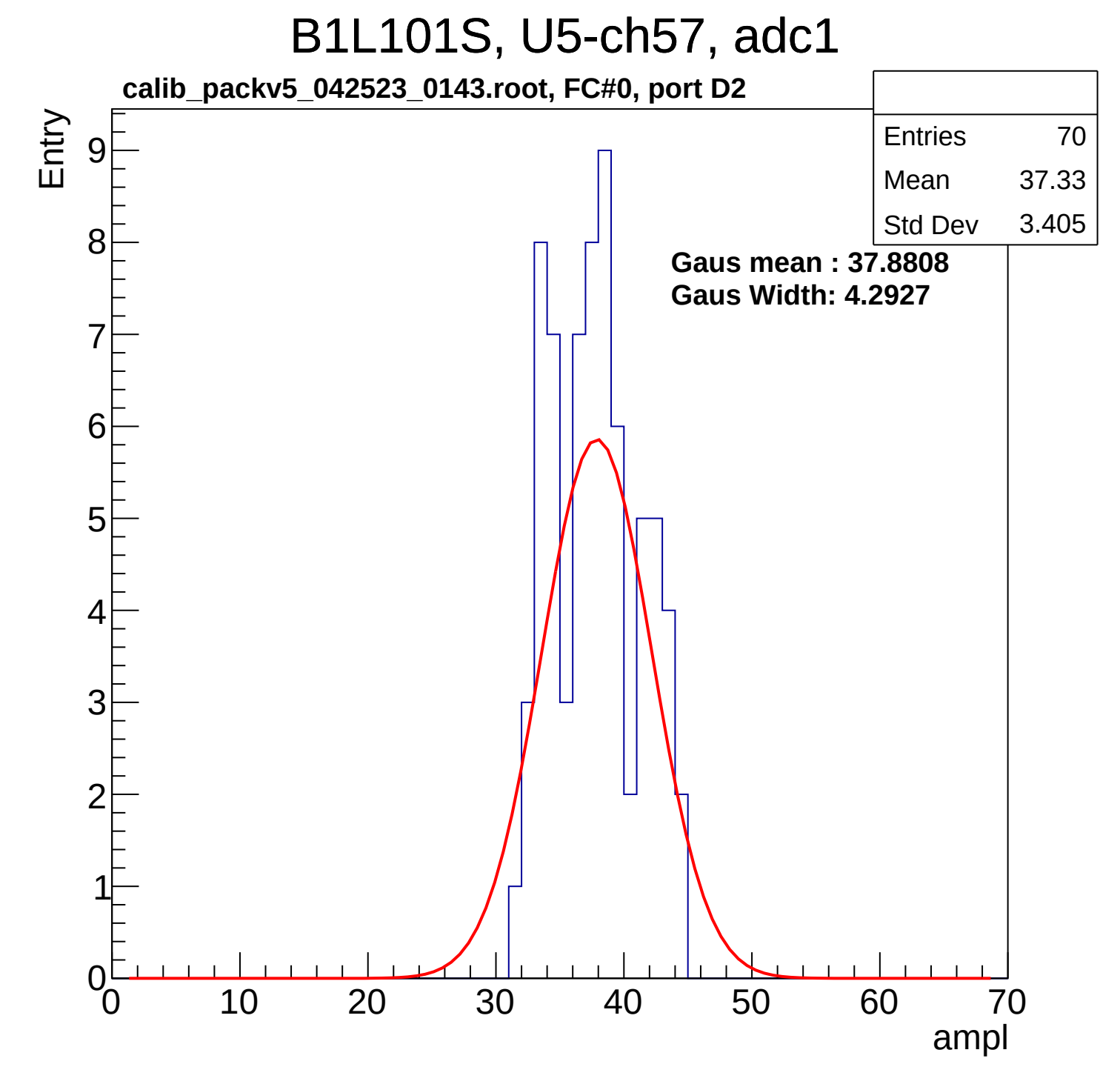
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch57, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 37.33
Std Dev 3.405
Gaus mean : 37.8808
Gaus Width: 4.2927
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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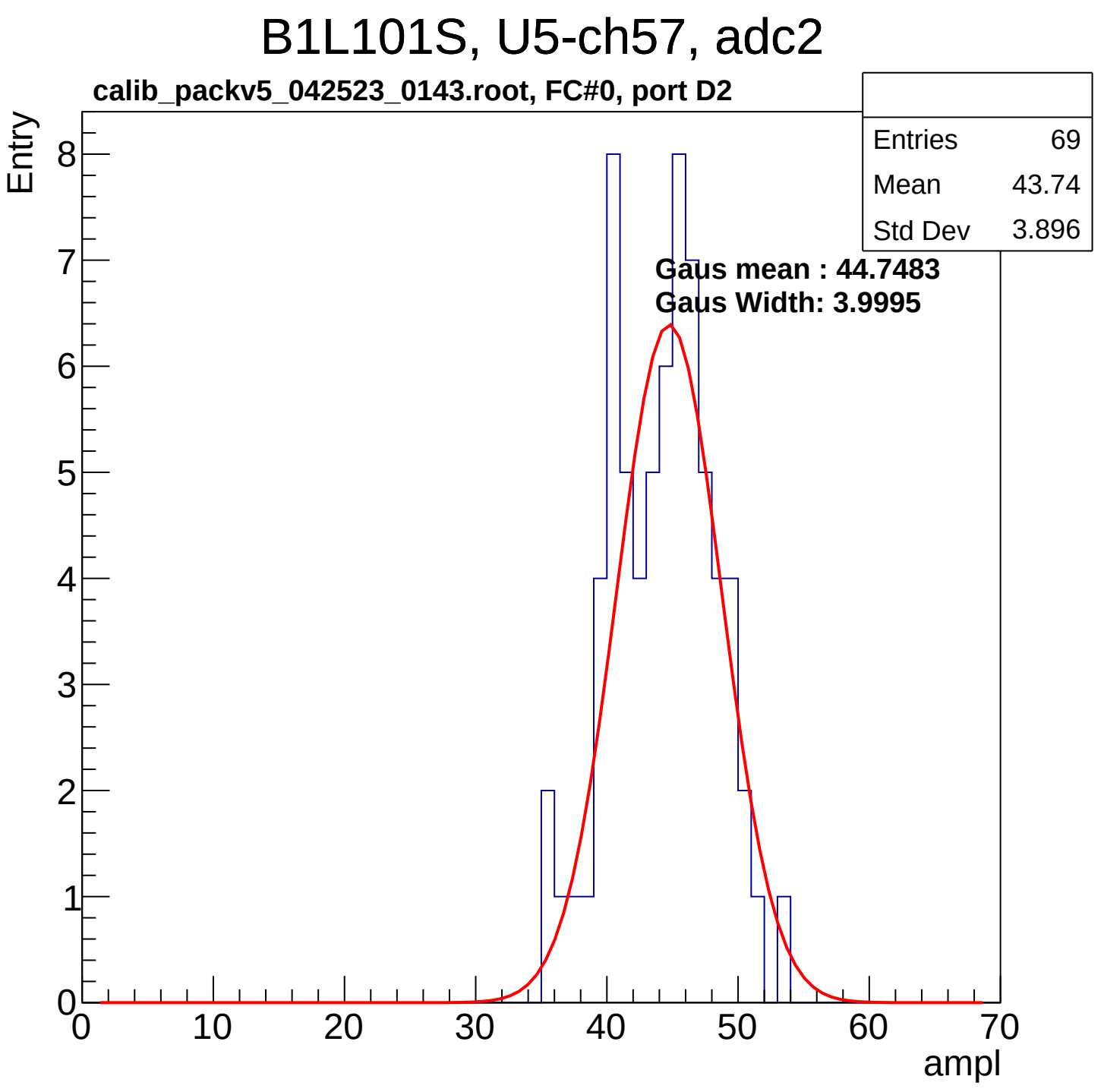
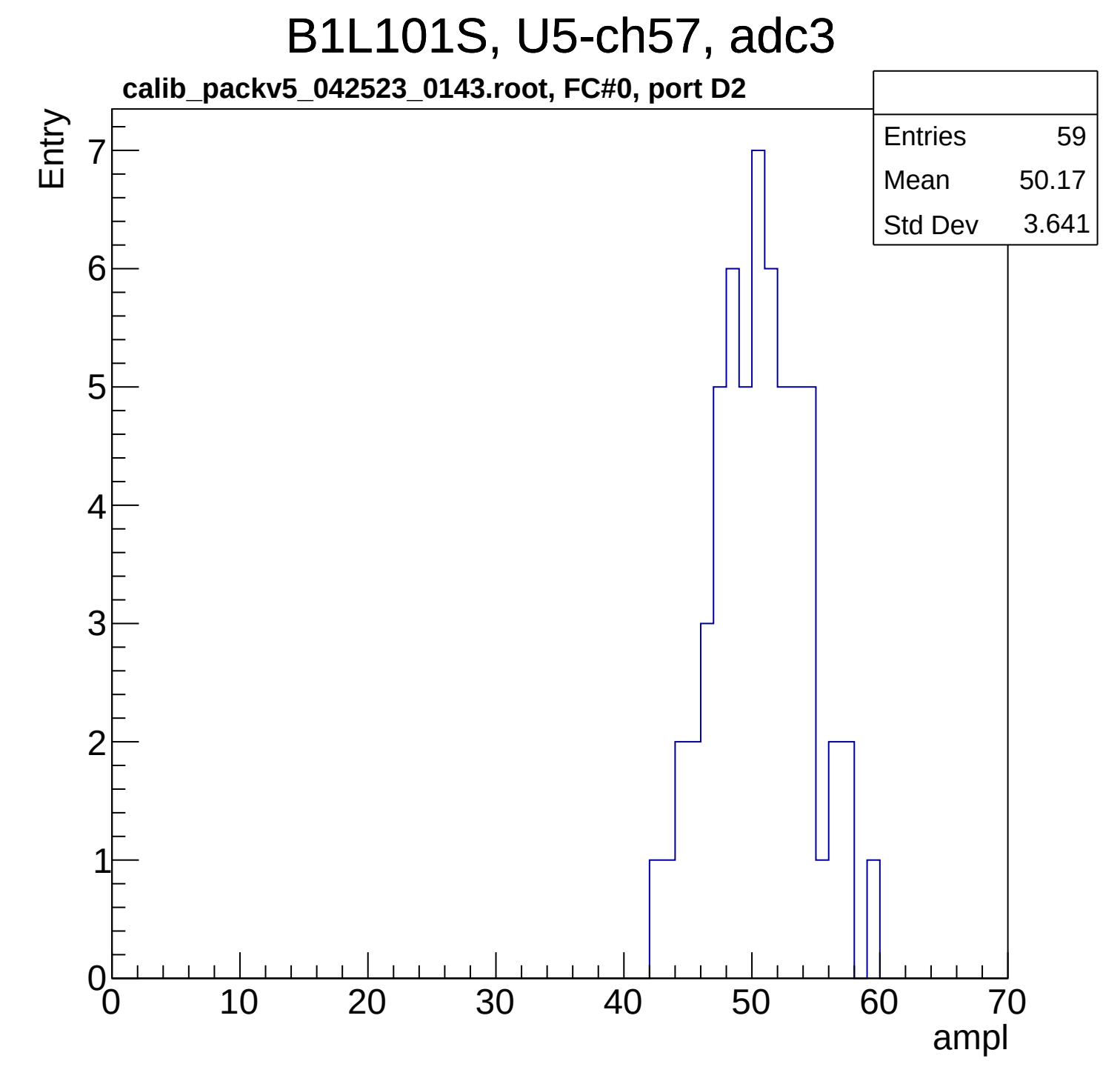

B1L101S, U5-ch57, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 43.74
Std Dev 3.896
Gaus mean : 44.7483
Gaus Width: 3.9995
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch57, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 50.17
Std Dev 3.641
Entry
ampl
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1
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3
4
5
6
7
0
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20
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40
50
60
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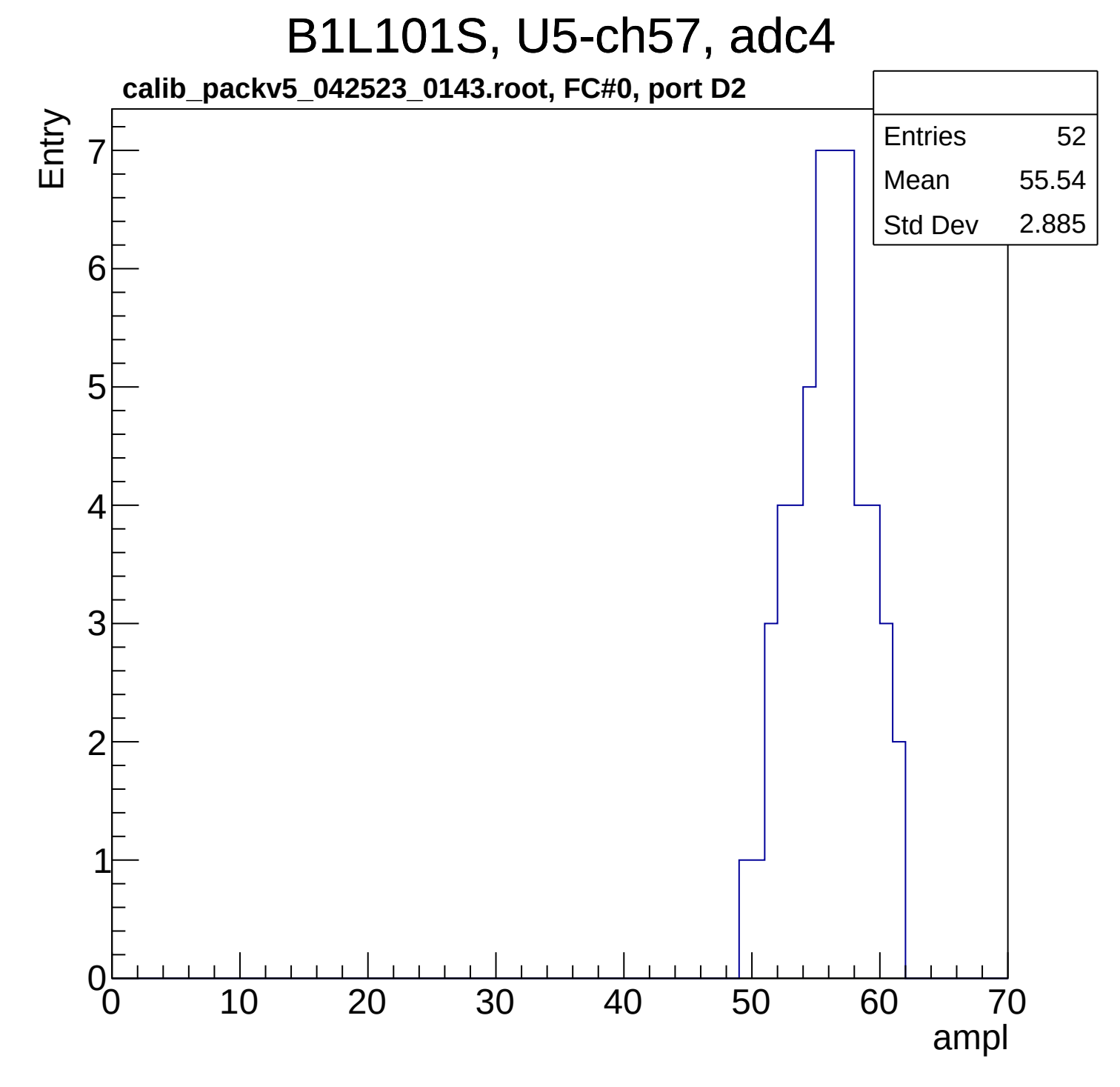
B1L101S, U5-ch57, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 55.54
Std Dev 2.885
Entry
ampl
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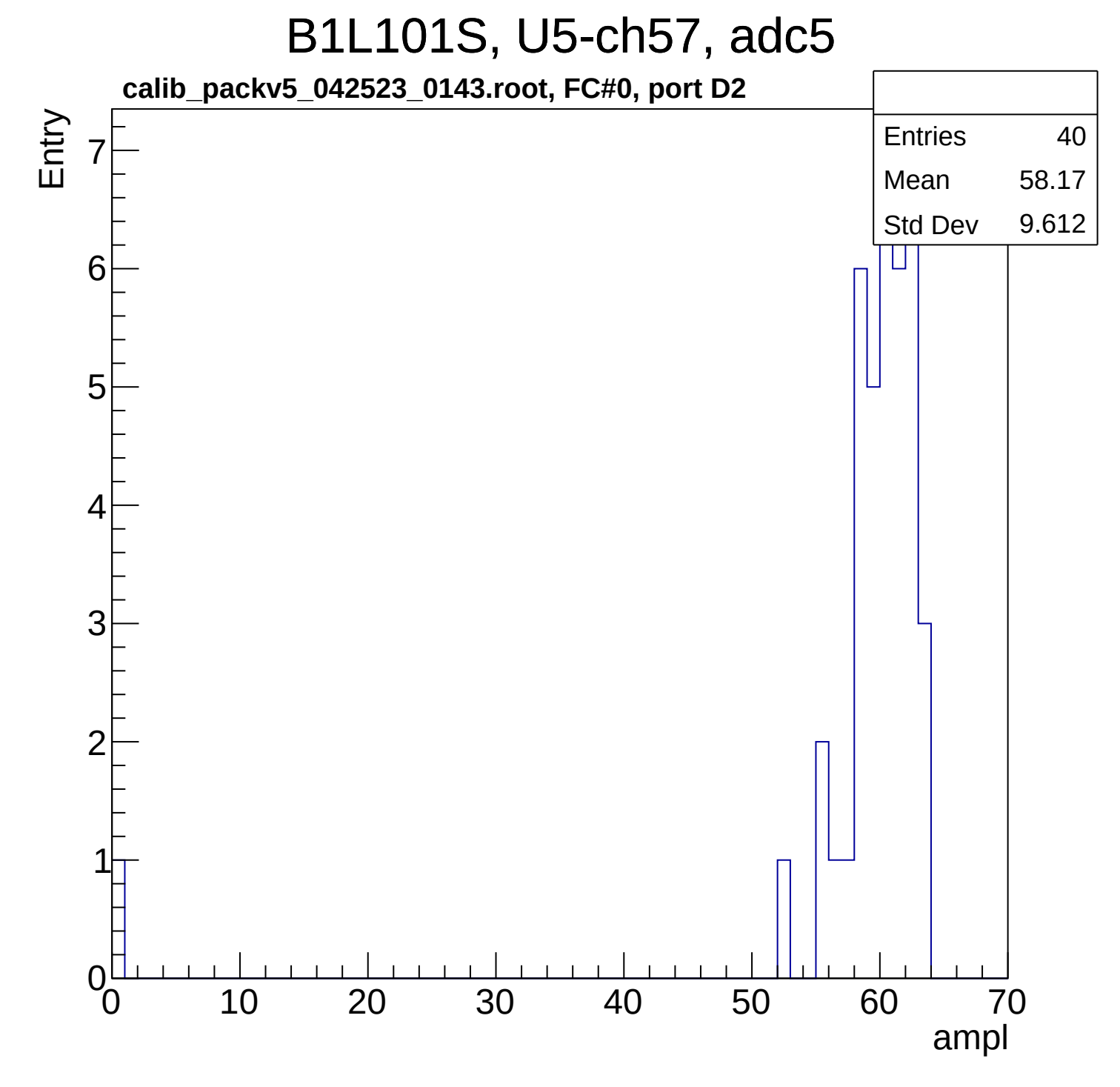
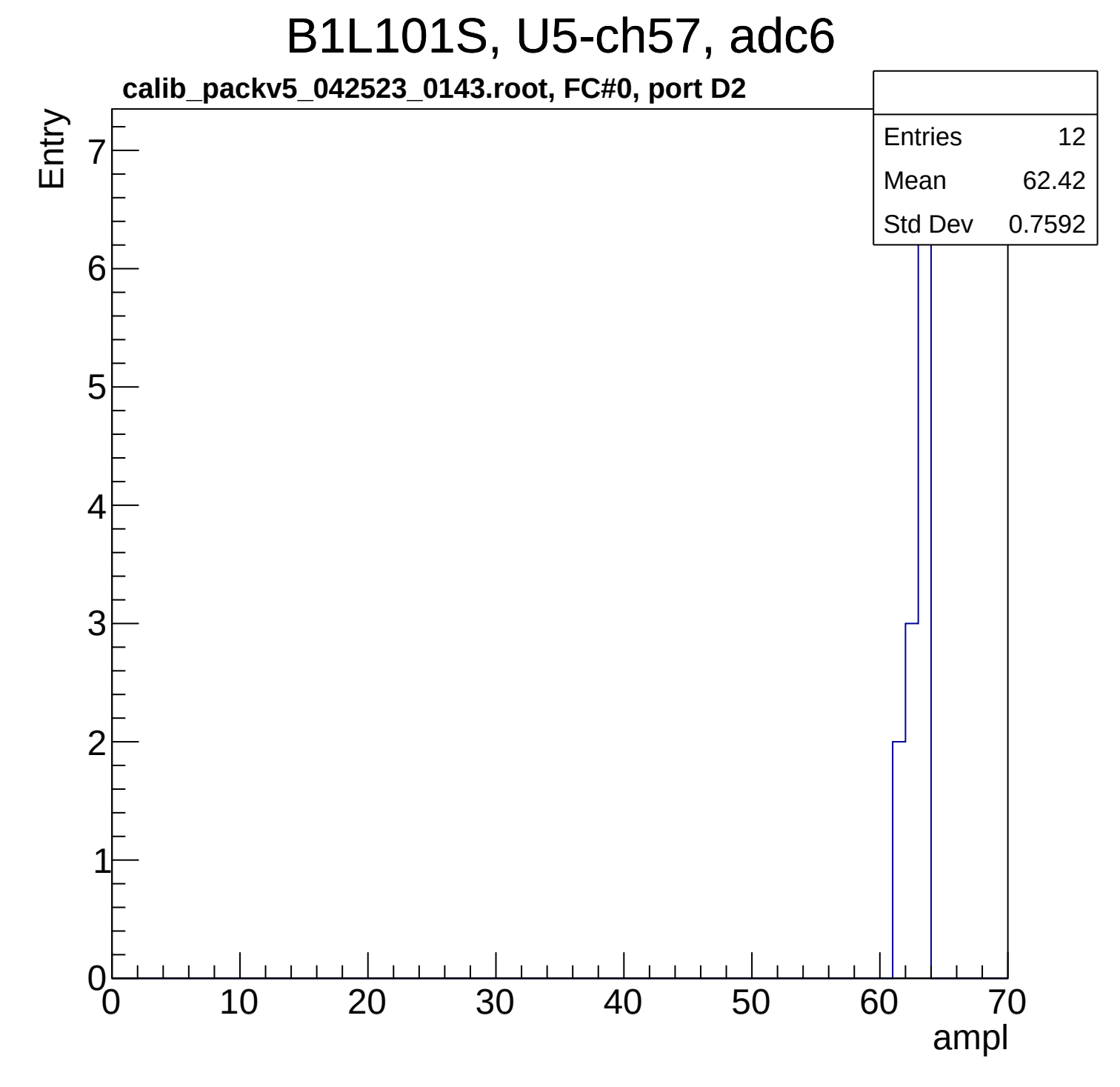
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch57, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 40
Mean 58.17
Std Dev 9.612
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch57, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 12
Mean 62.42
Std Dev 0.7592
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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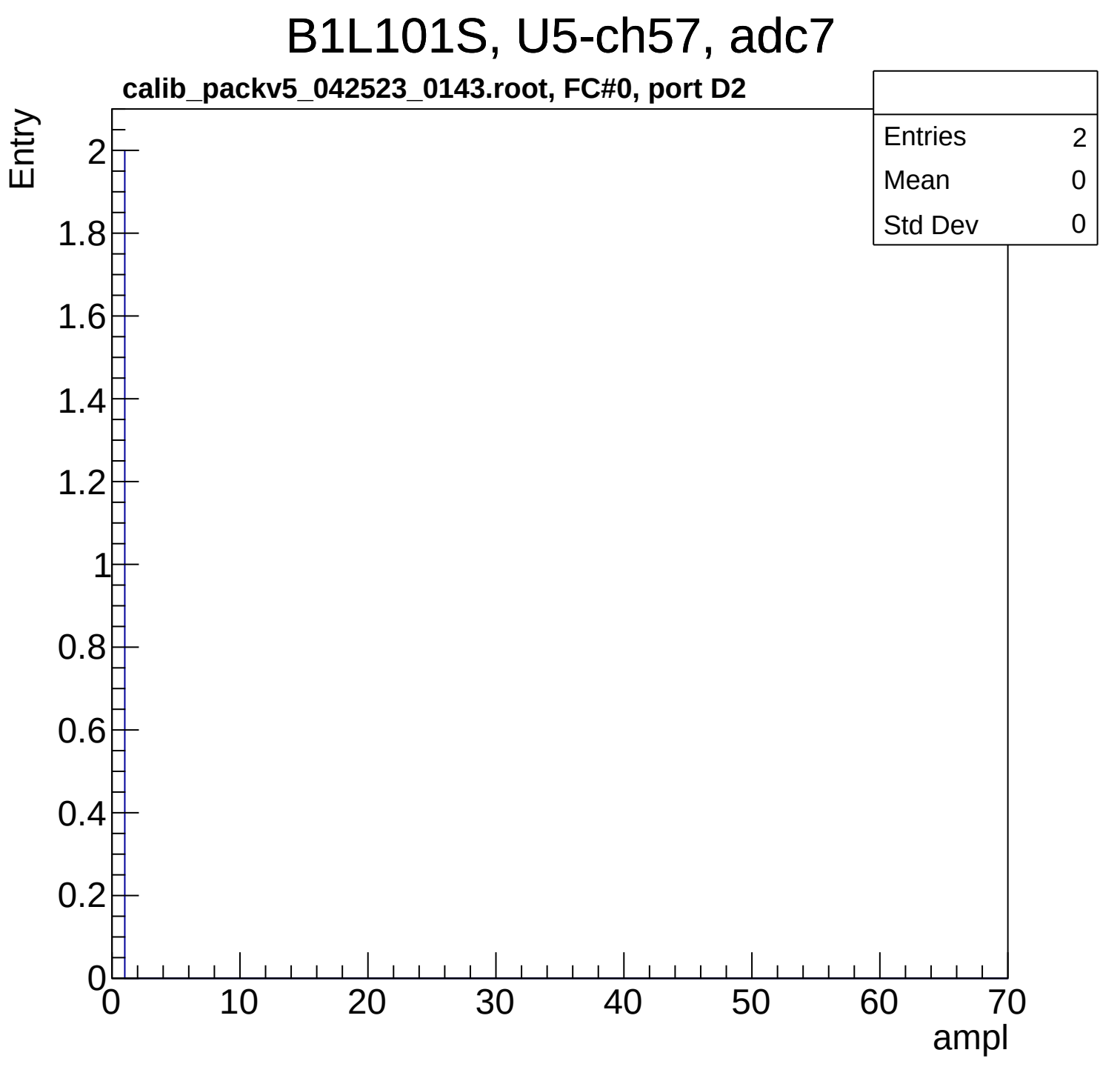
B1L101S, U5-ch57, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
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60
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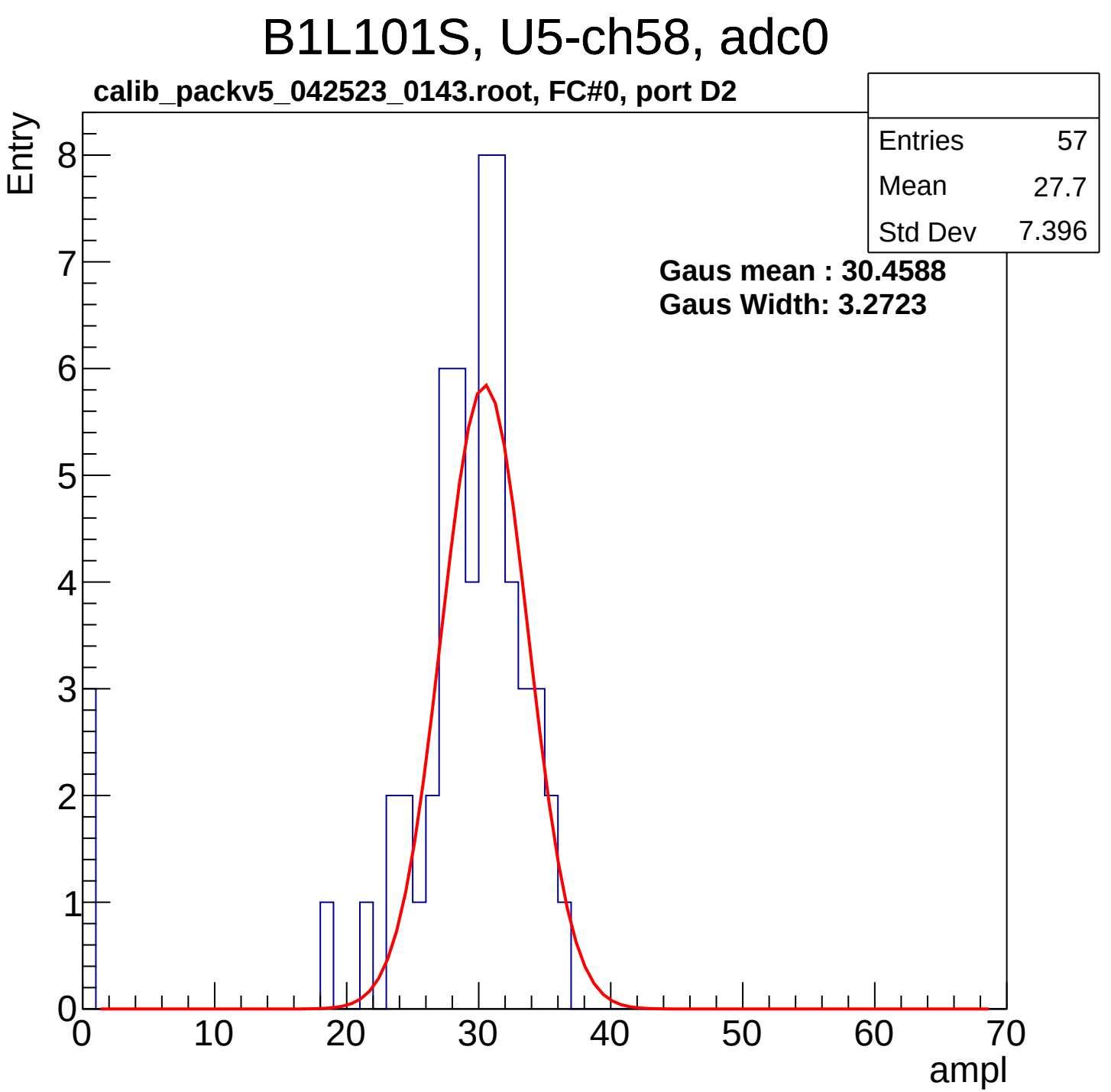
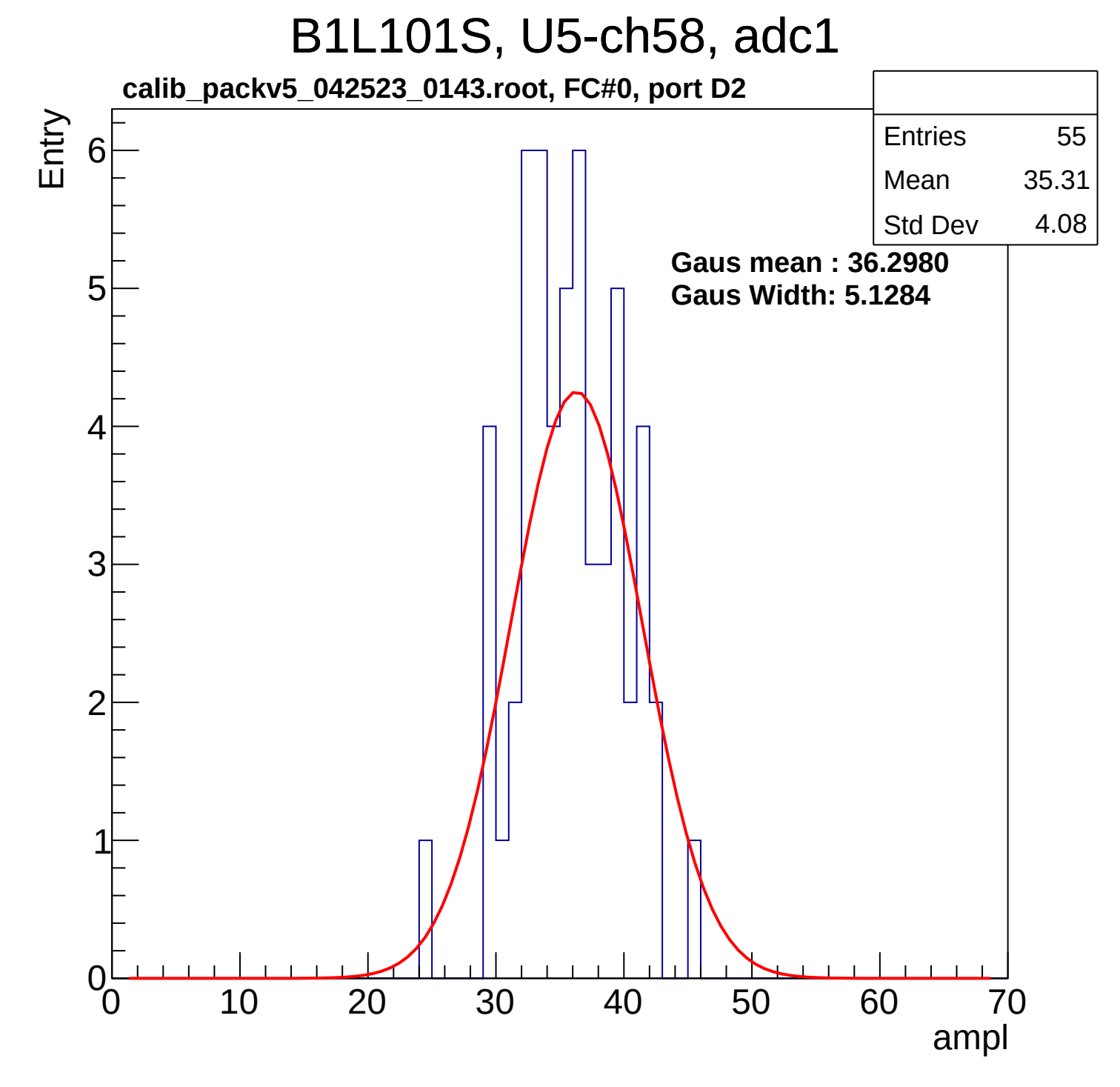

B1L101S, U5-ch58, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 27.7
Std Dev 7.396
Gaus mean : 30.4588
Gaus Width: 3.2723
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch58, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 35.31
Std Dev 4.08
Gaus mean : 36.2980
Gaus Width: 5.1284
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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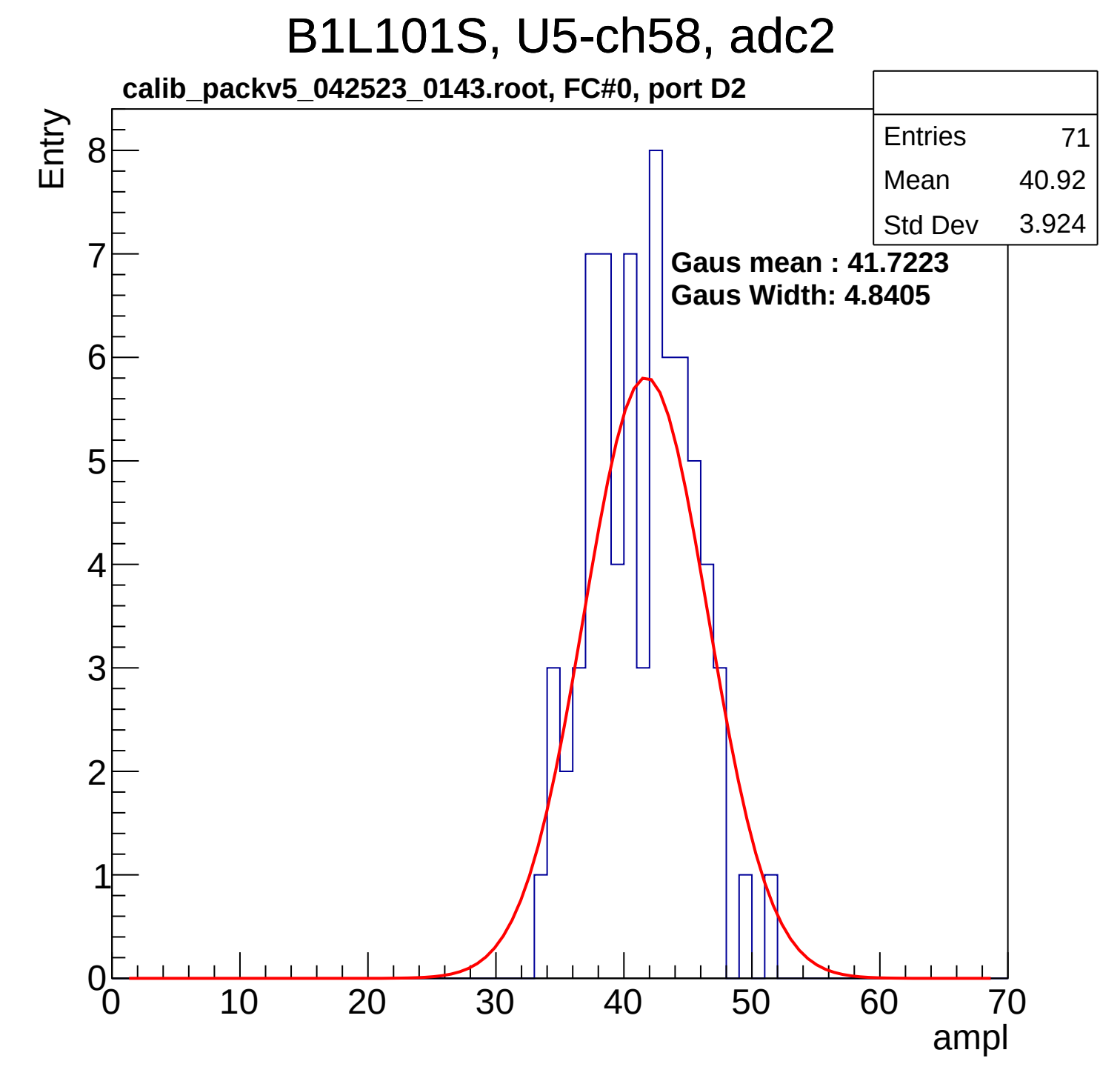
B1L101S, U5-ch58, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 40.92
Std Dev 3.924
Gaus mean : 41.7223
Gaus Width: 4.8405
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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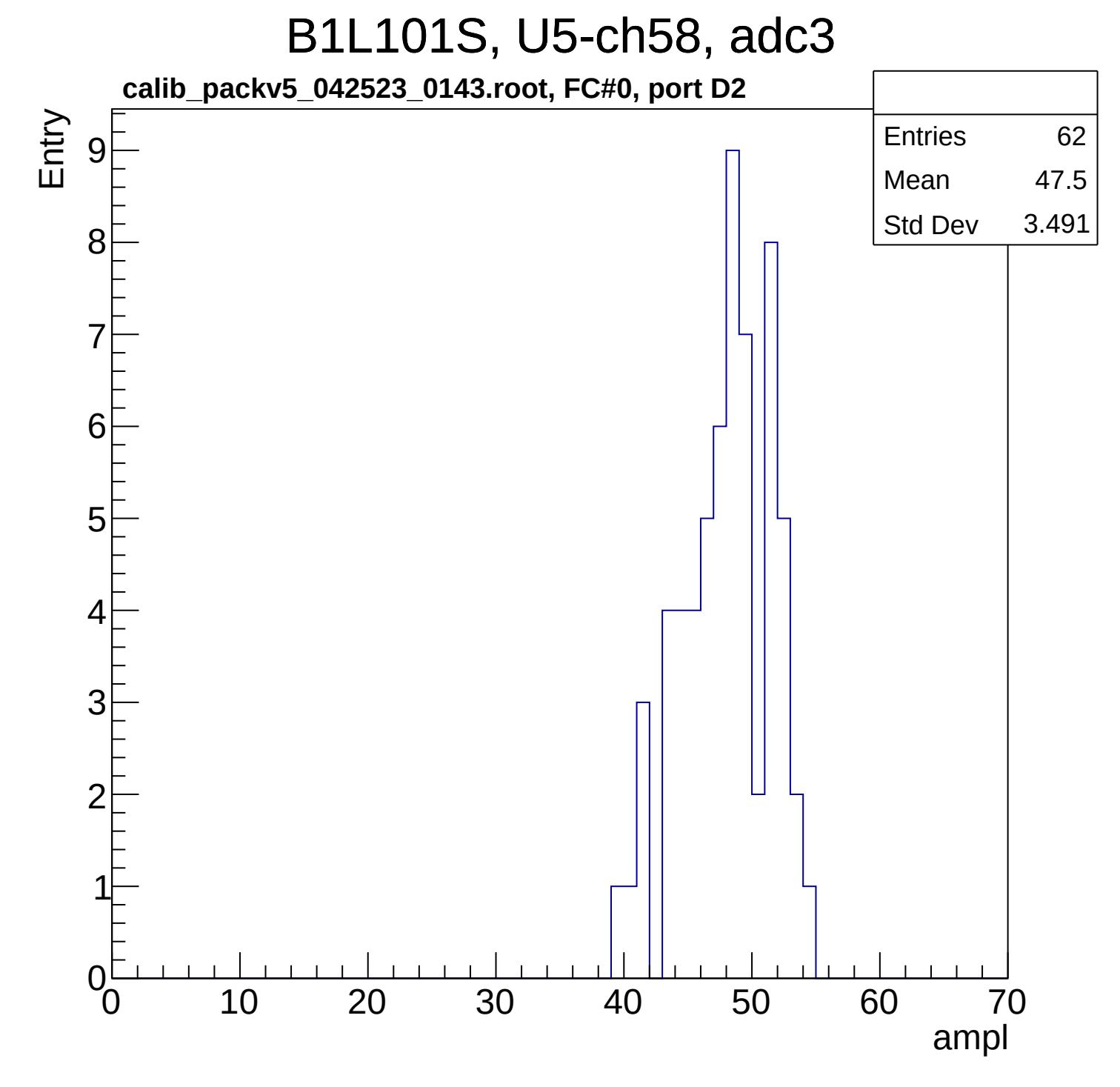
B1L101S, U5-ch58, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 47.5
Std Dev 3.491
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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60
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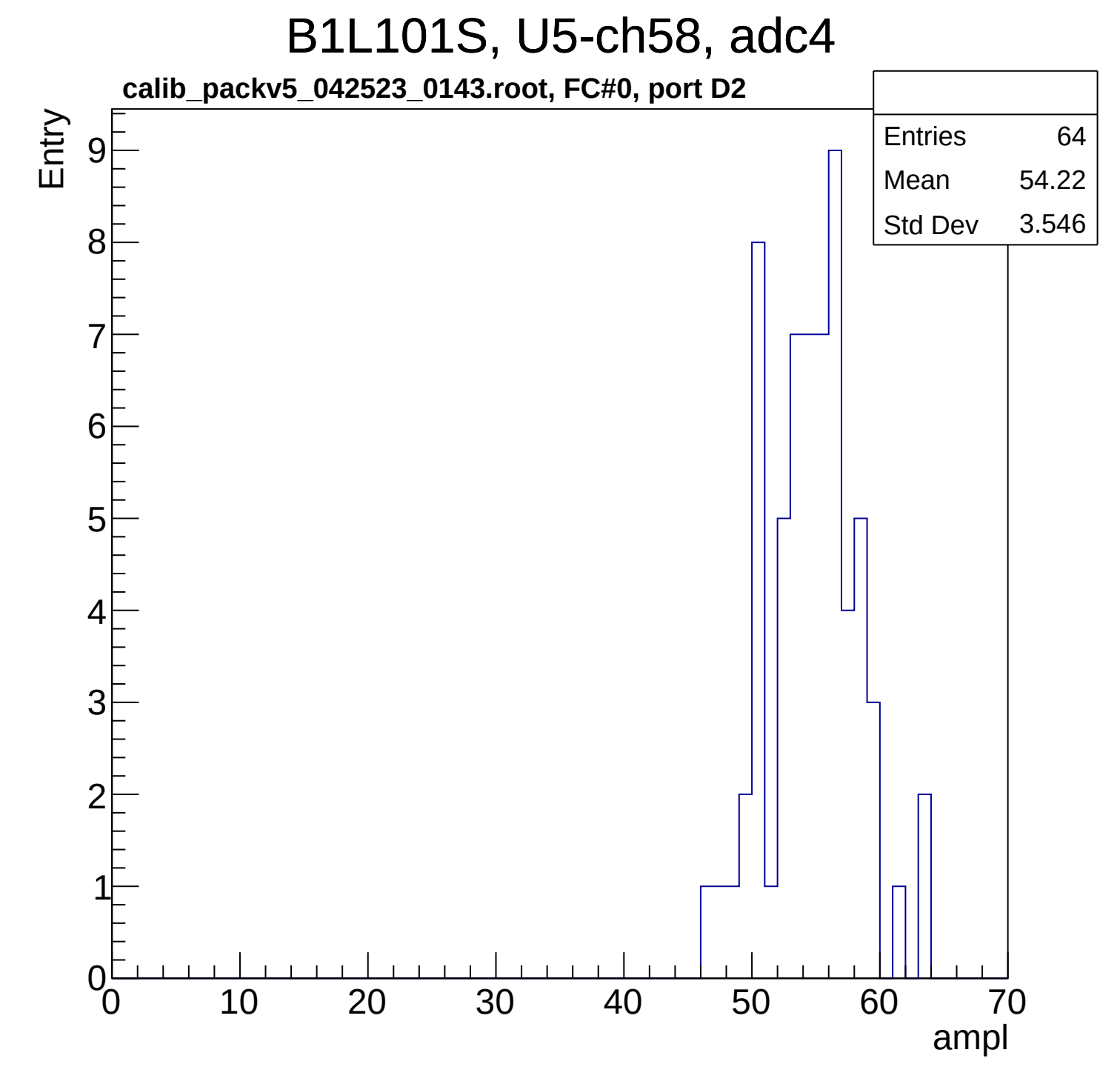
B1L101S, U5-ch58, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 54.22
Std Dev 3.546
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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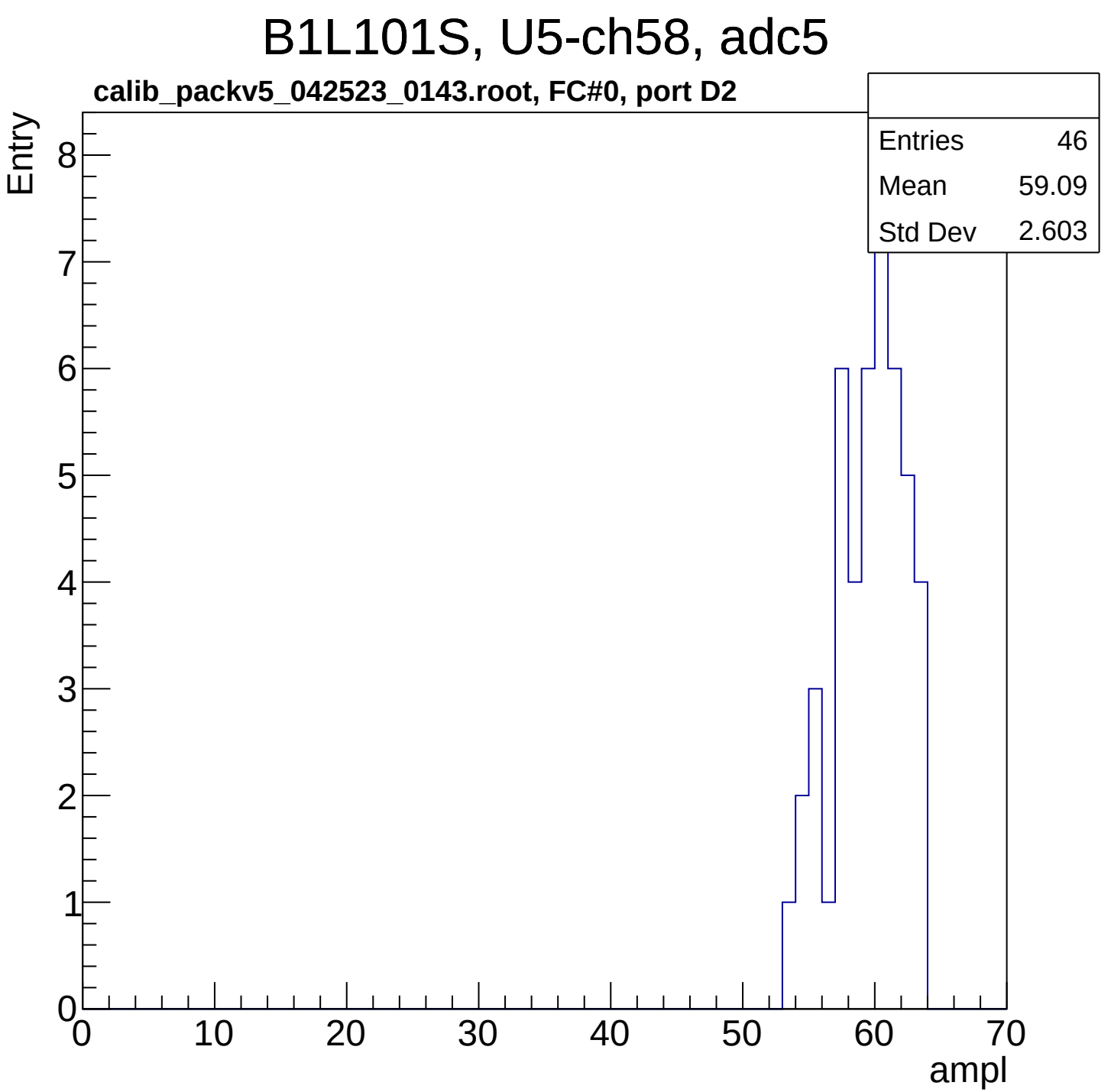
B1L101S, U5-ch58, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 59.09
Std Dev 2.603
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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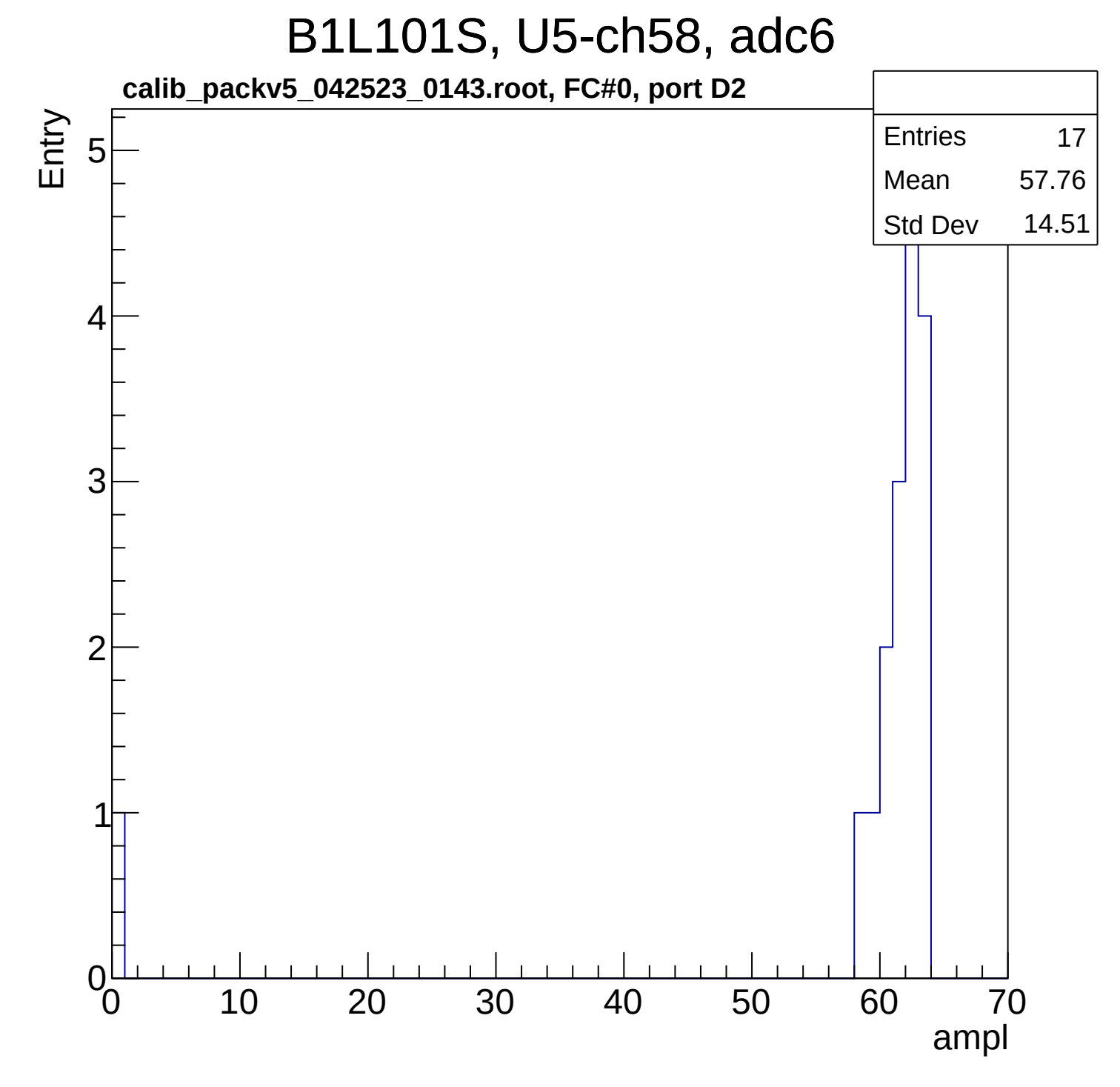
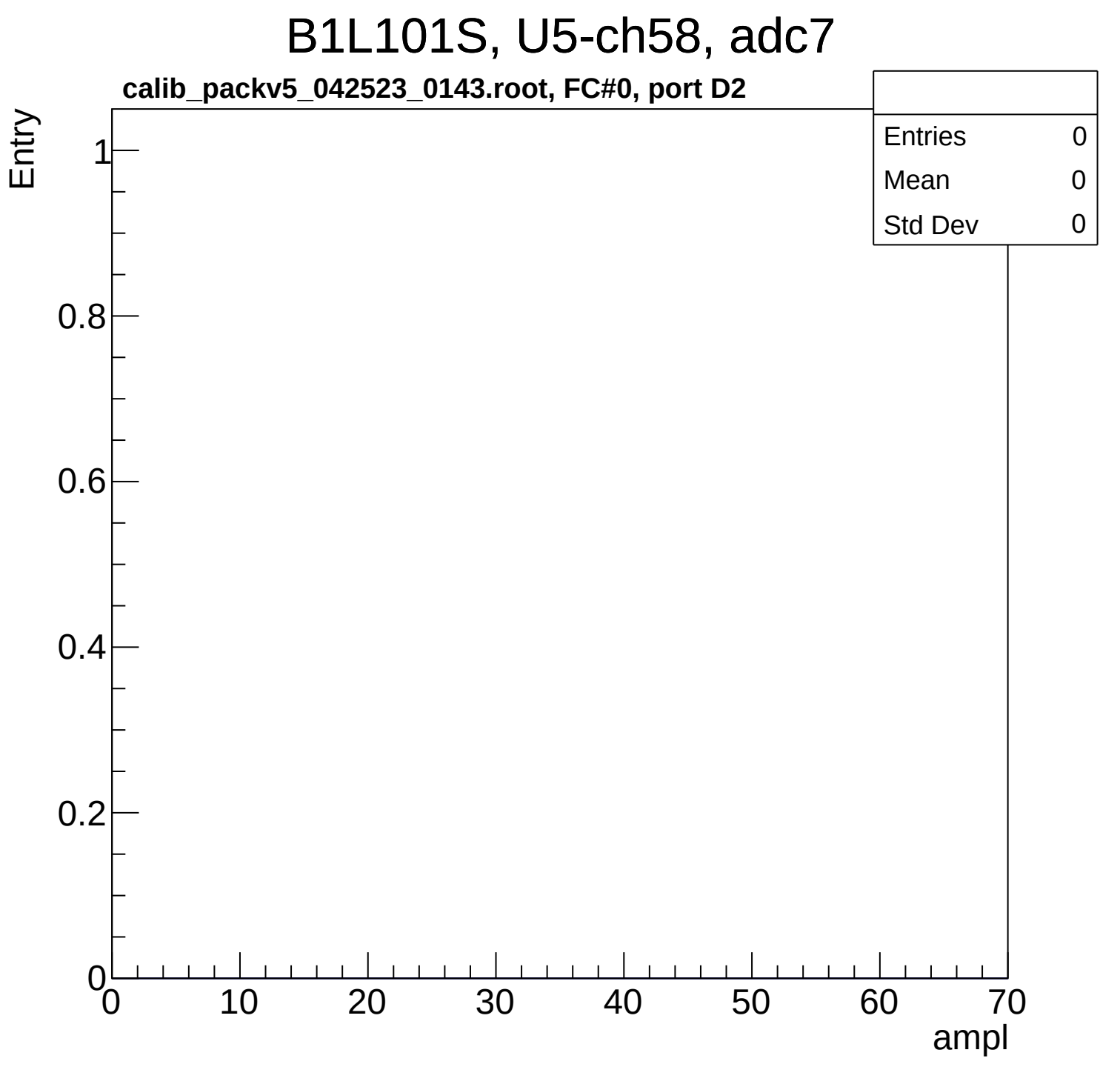
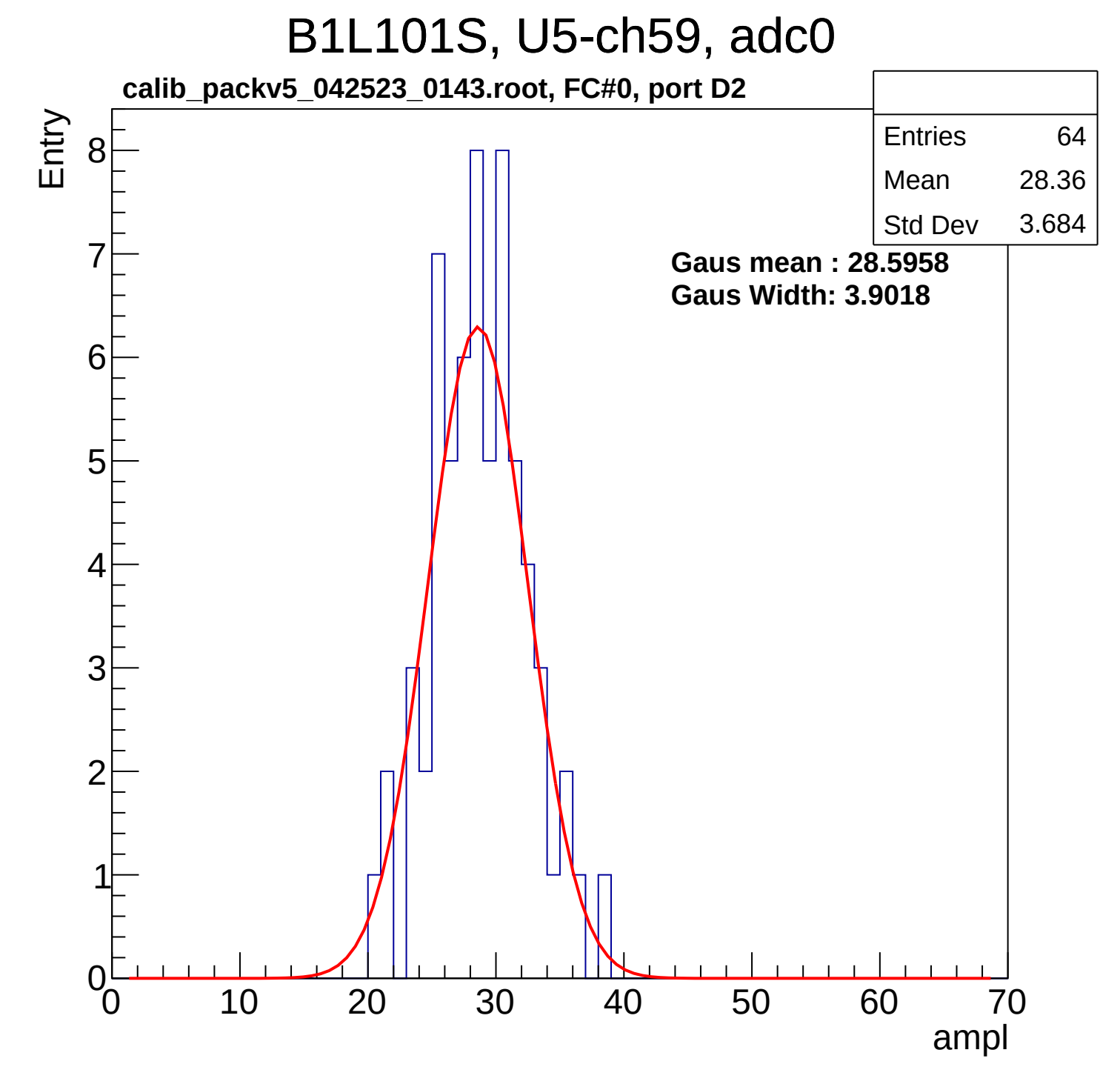
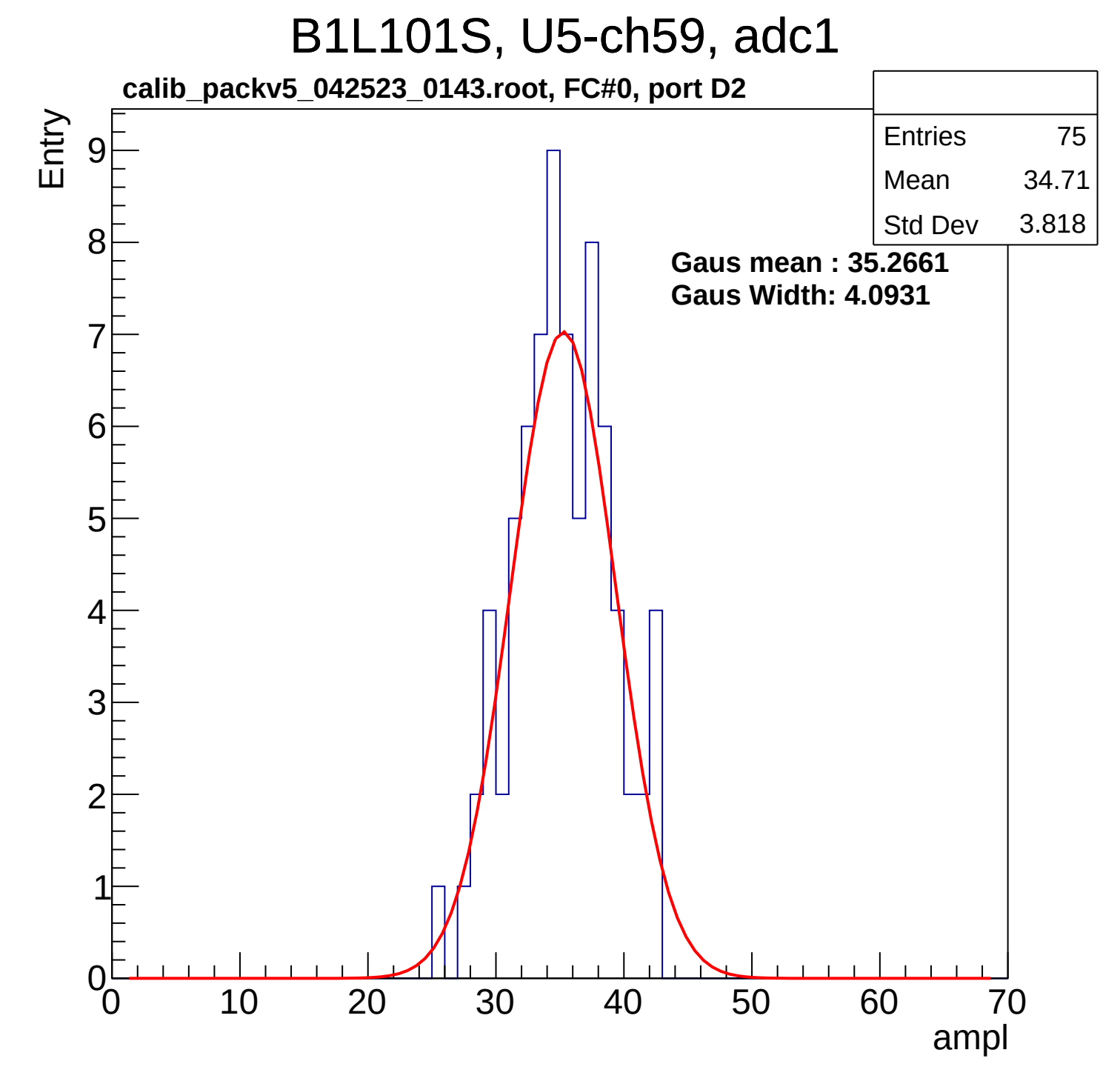
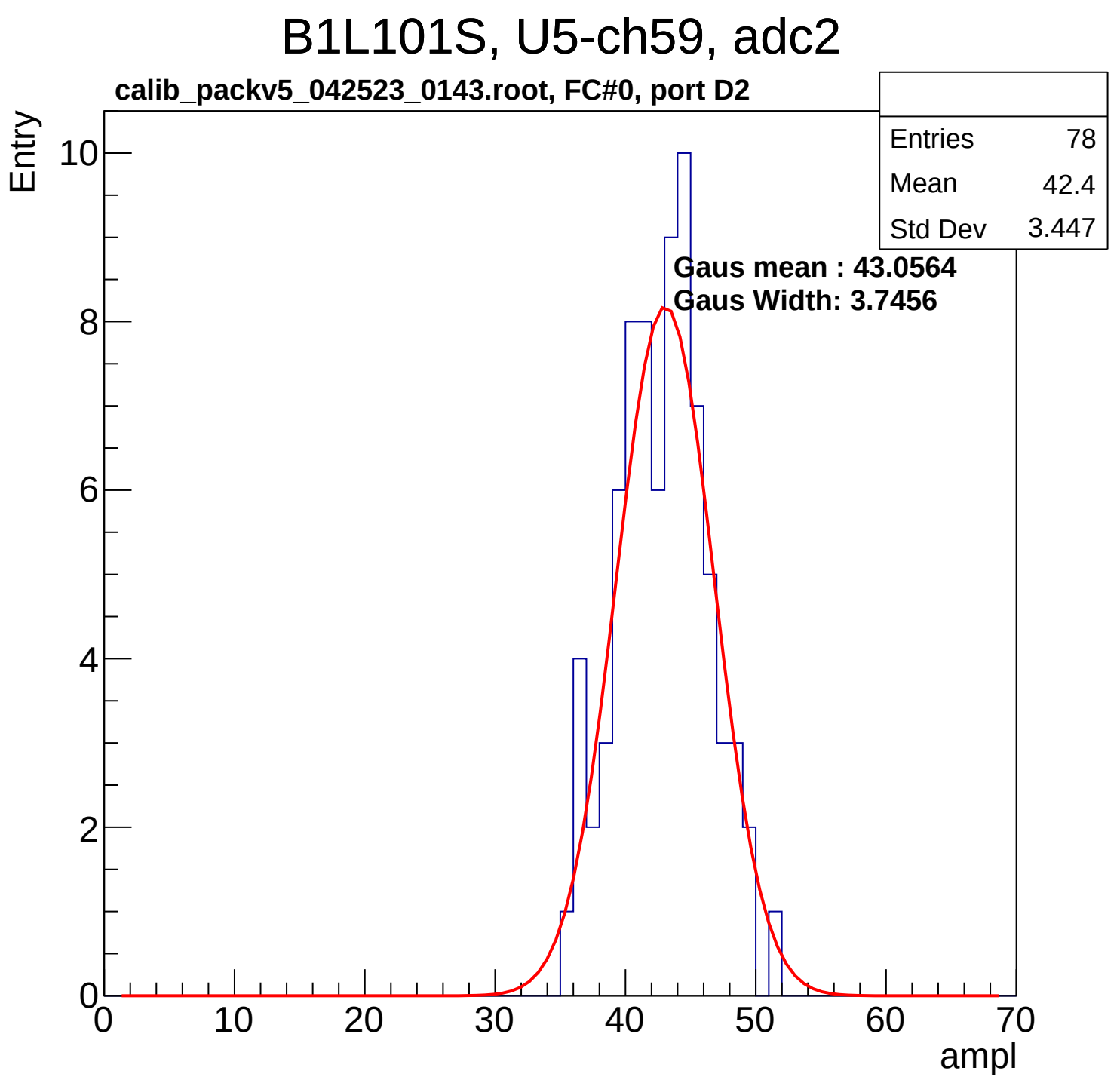
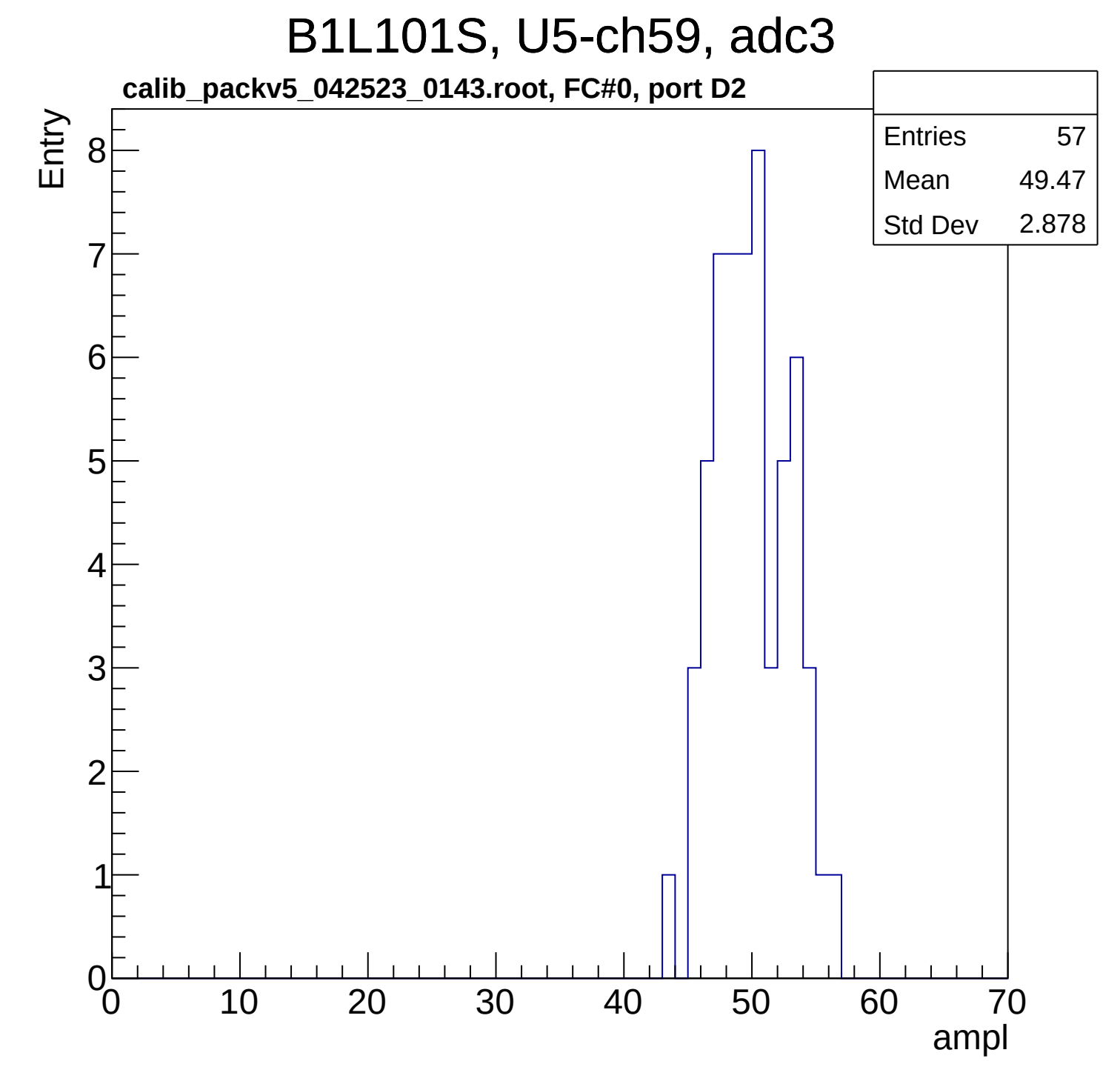

B1L101S, U5-ch58, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 17
Mean 57.76
Std Dev 14.51
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

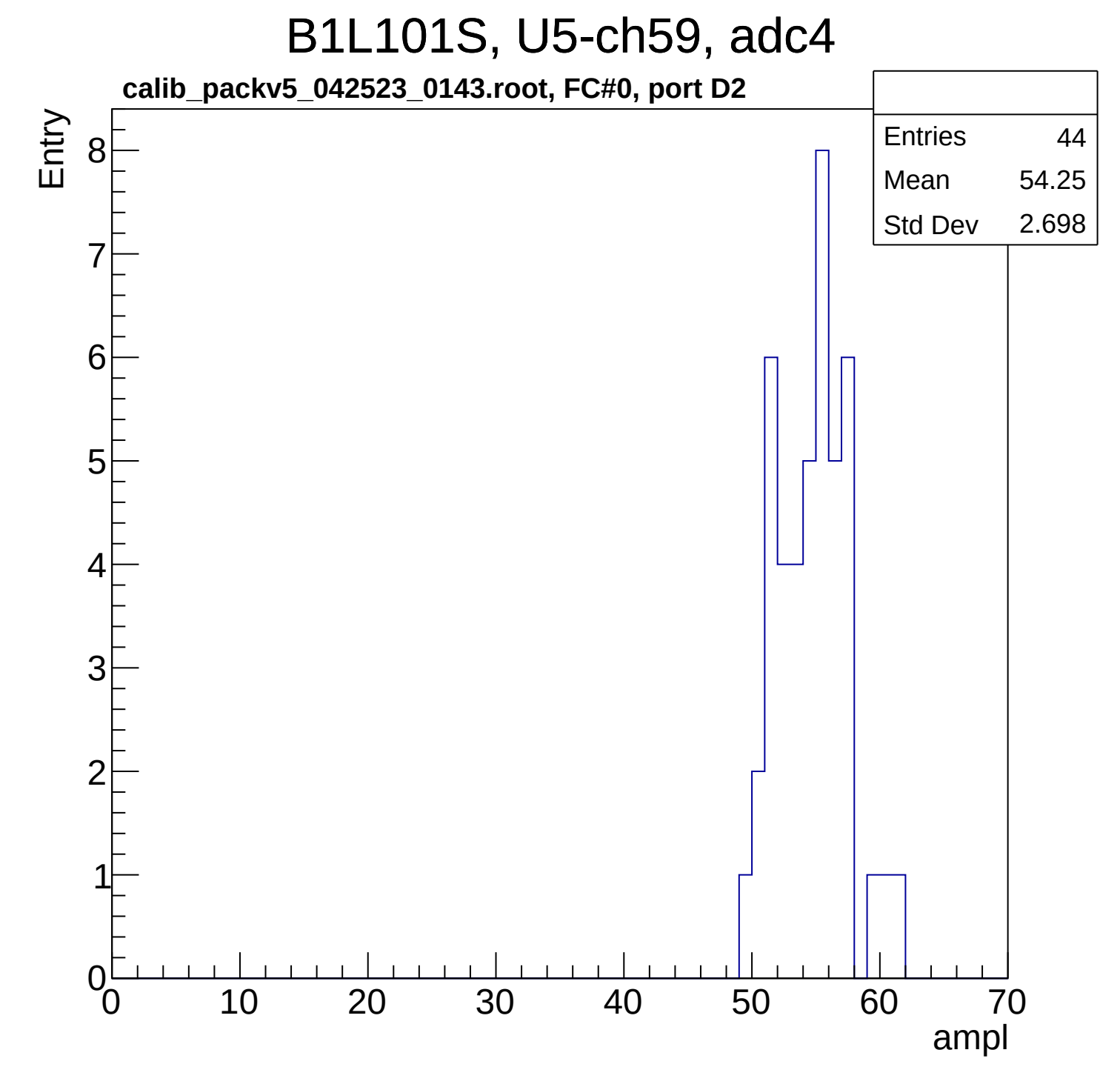

B1L101S, U5-ch58, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch59, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 28.36
Std Dev 3.684
Gaus mean : 28.5958
Gaus Width: 3.9018
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch59, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 34.71
Std Dev 3.818
Gaus mean : 35.2661
Gaus Width: 4.0931
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch59, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 42.4
Std Dev 3.447
Gaus mean : 43.0564
Gaus Width: 3.7456
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch59, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 49.47
Std Dev 2.878
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch59, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 44
Mean 54.25
Std Dev 2.698
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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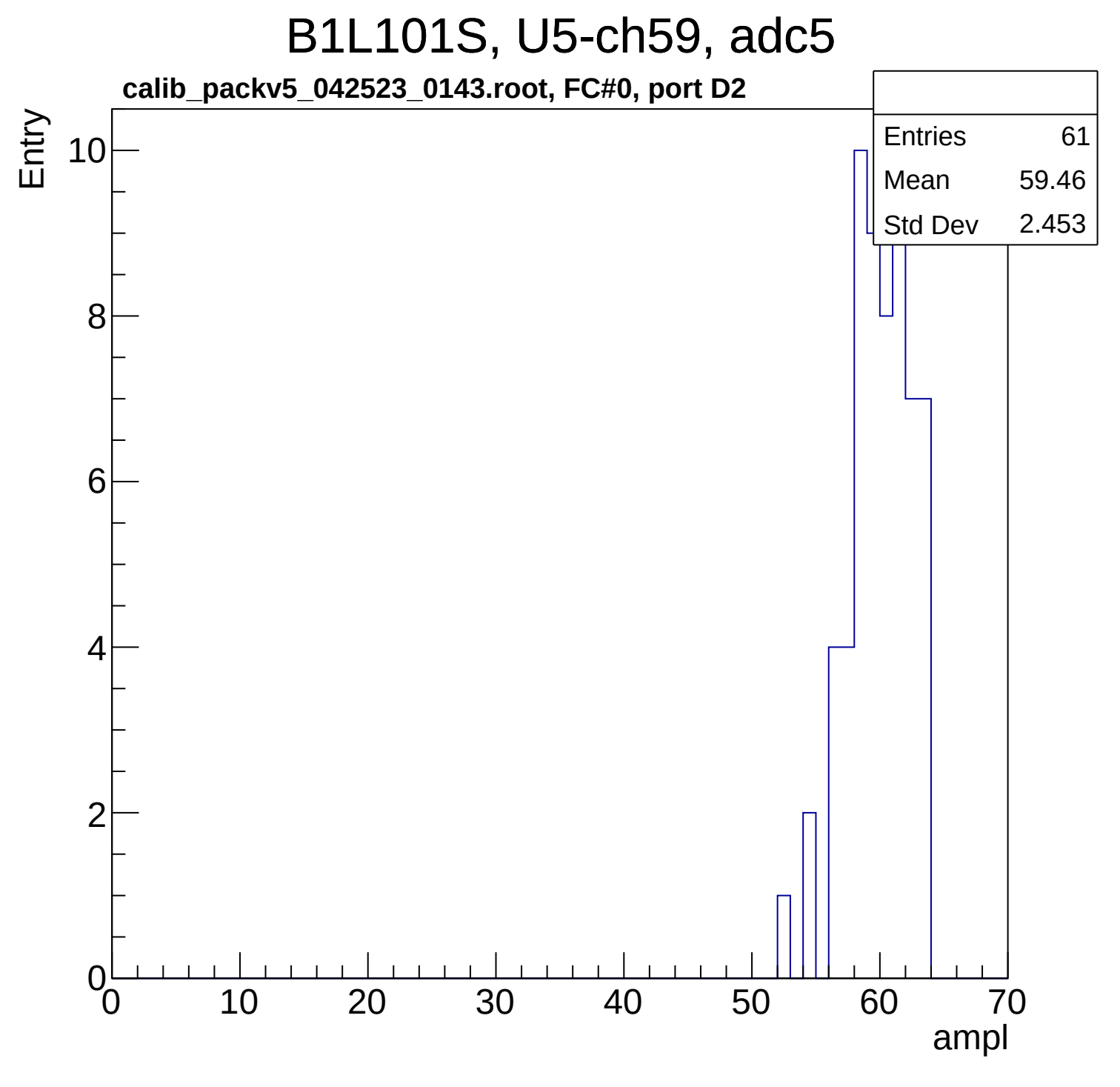
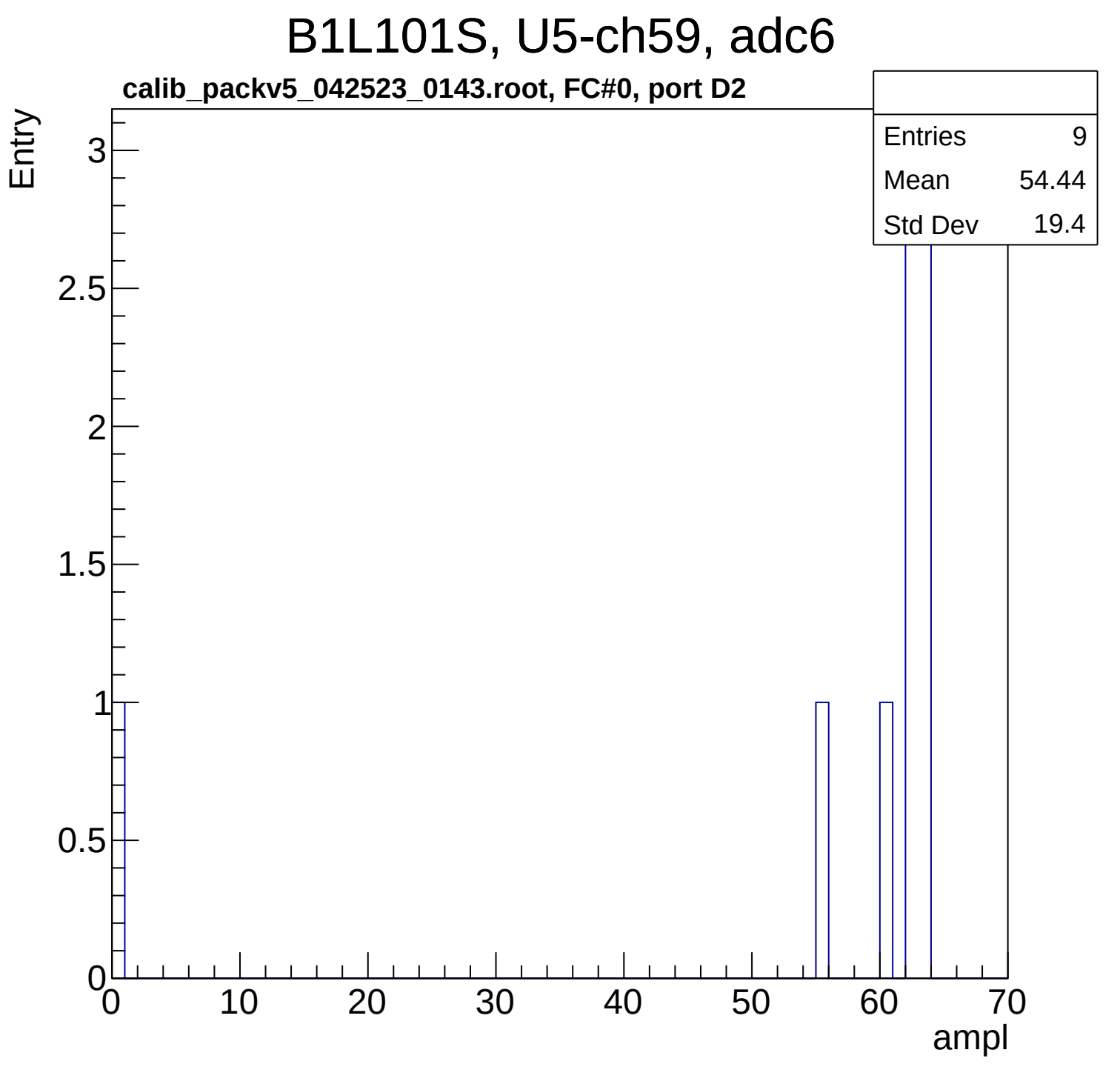
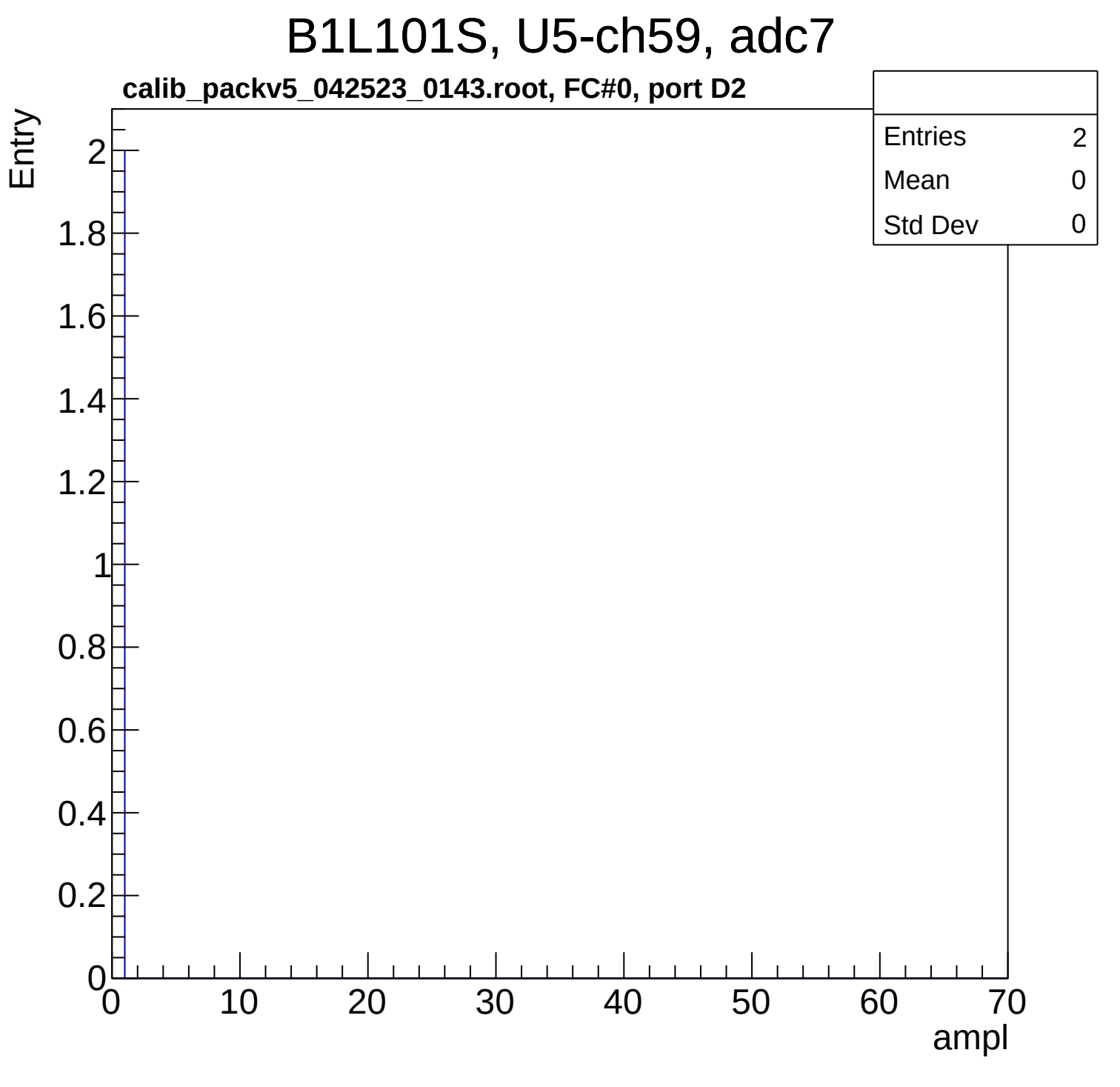
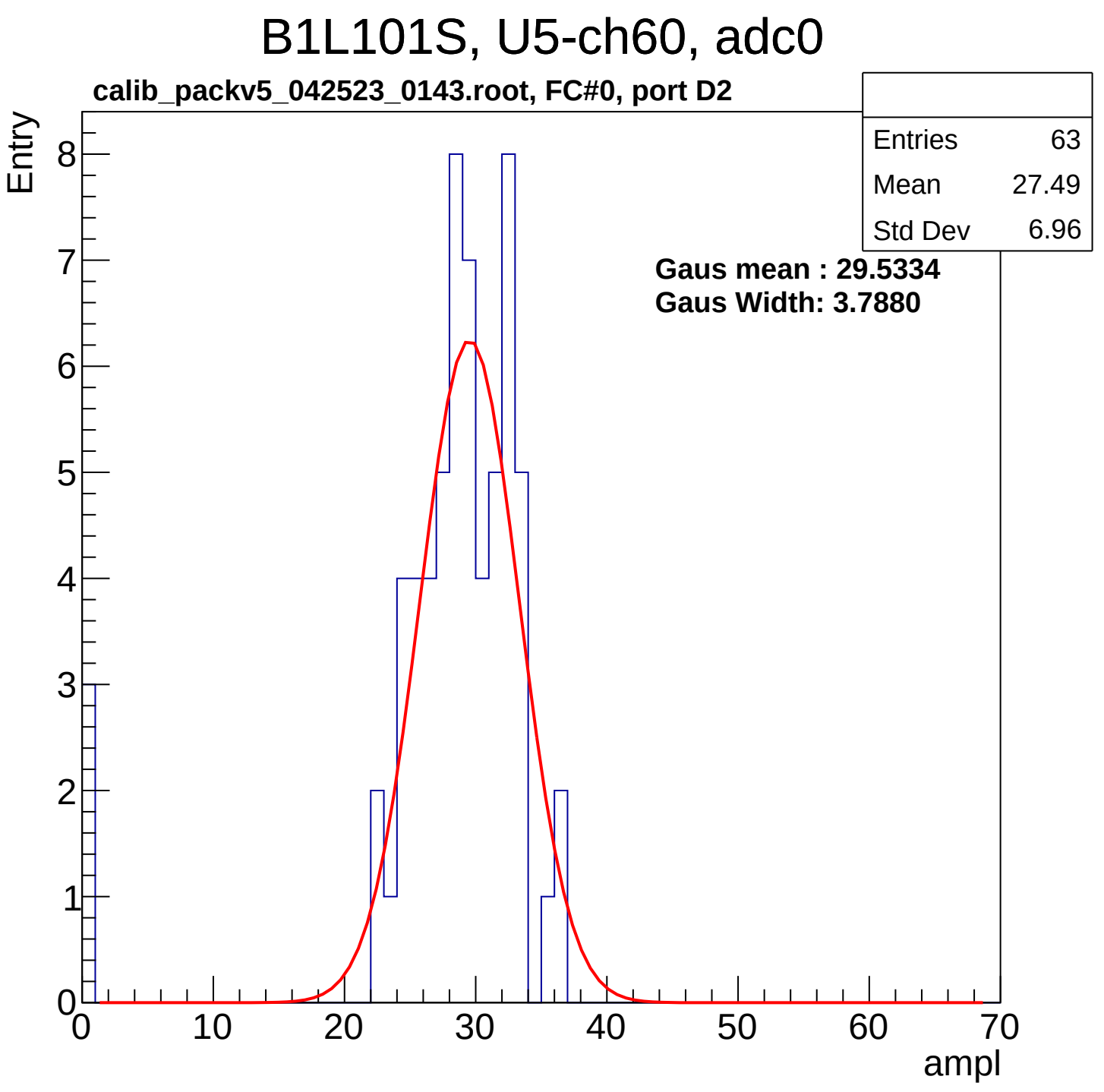
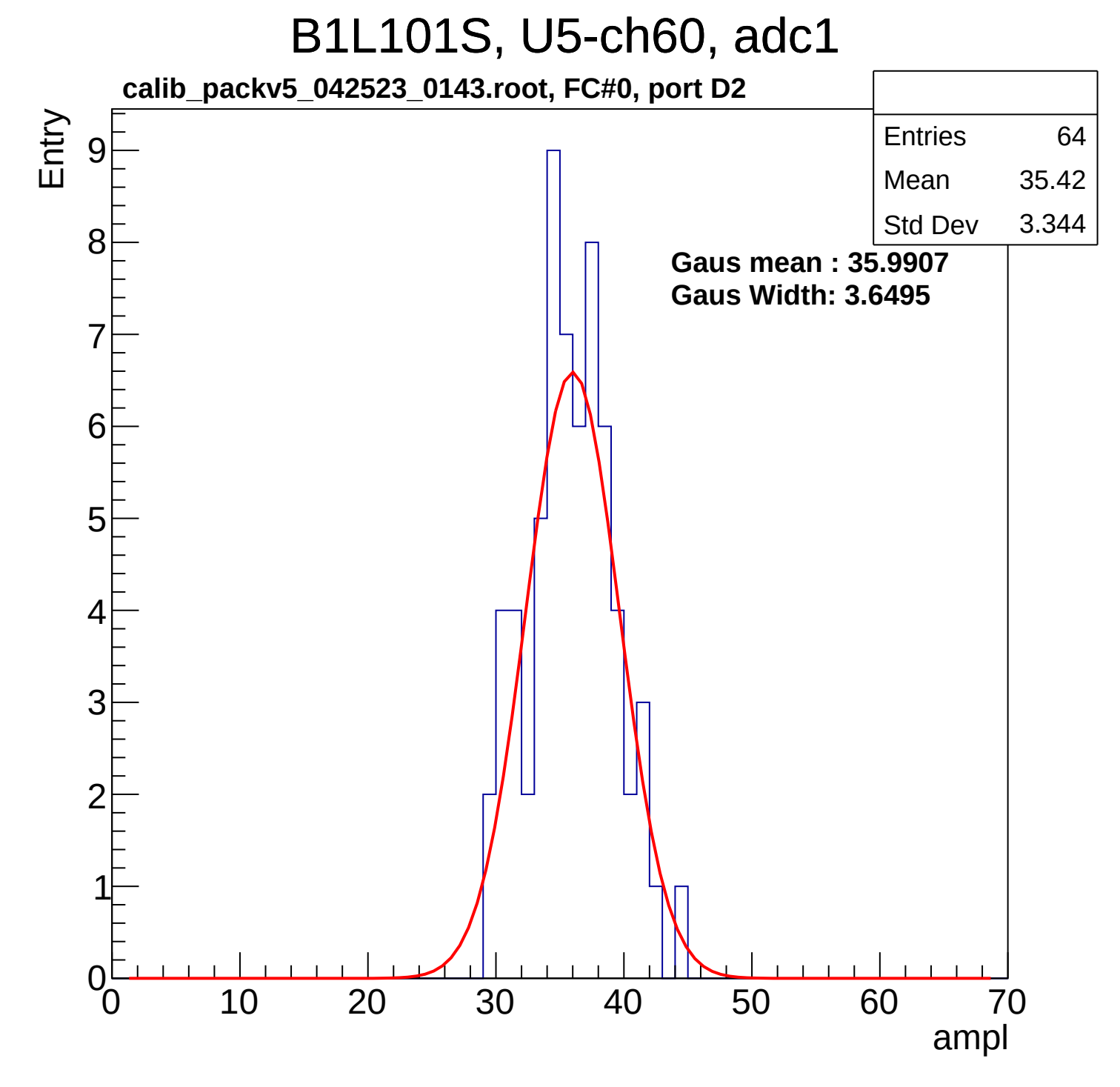

B1L101S, U5-ch59, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 59.46
Std Dev 2.453
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch59, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 54.44
Std Dev 19.4
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U5-ch59, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch60, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 27.49
Std Dev 6.96
Gaus mean : 29.5334
Gaus Width: 3.7880
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch60, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 35.42
Std Dev 3.344
Gaus mean : 35.9907
Gaus Width: 3.6495
Entry
ampl
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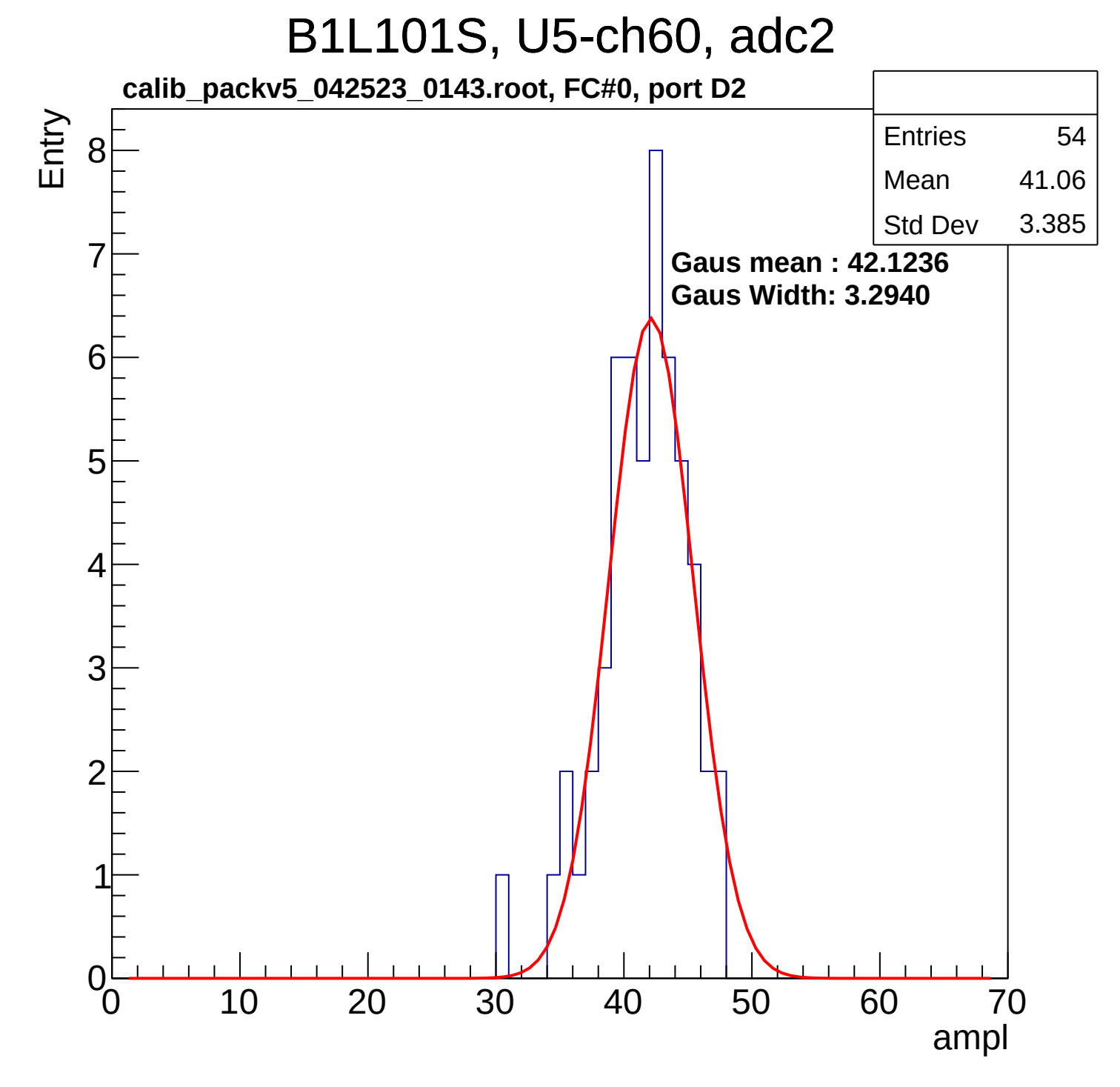
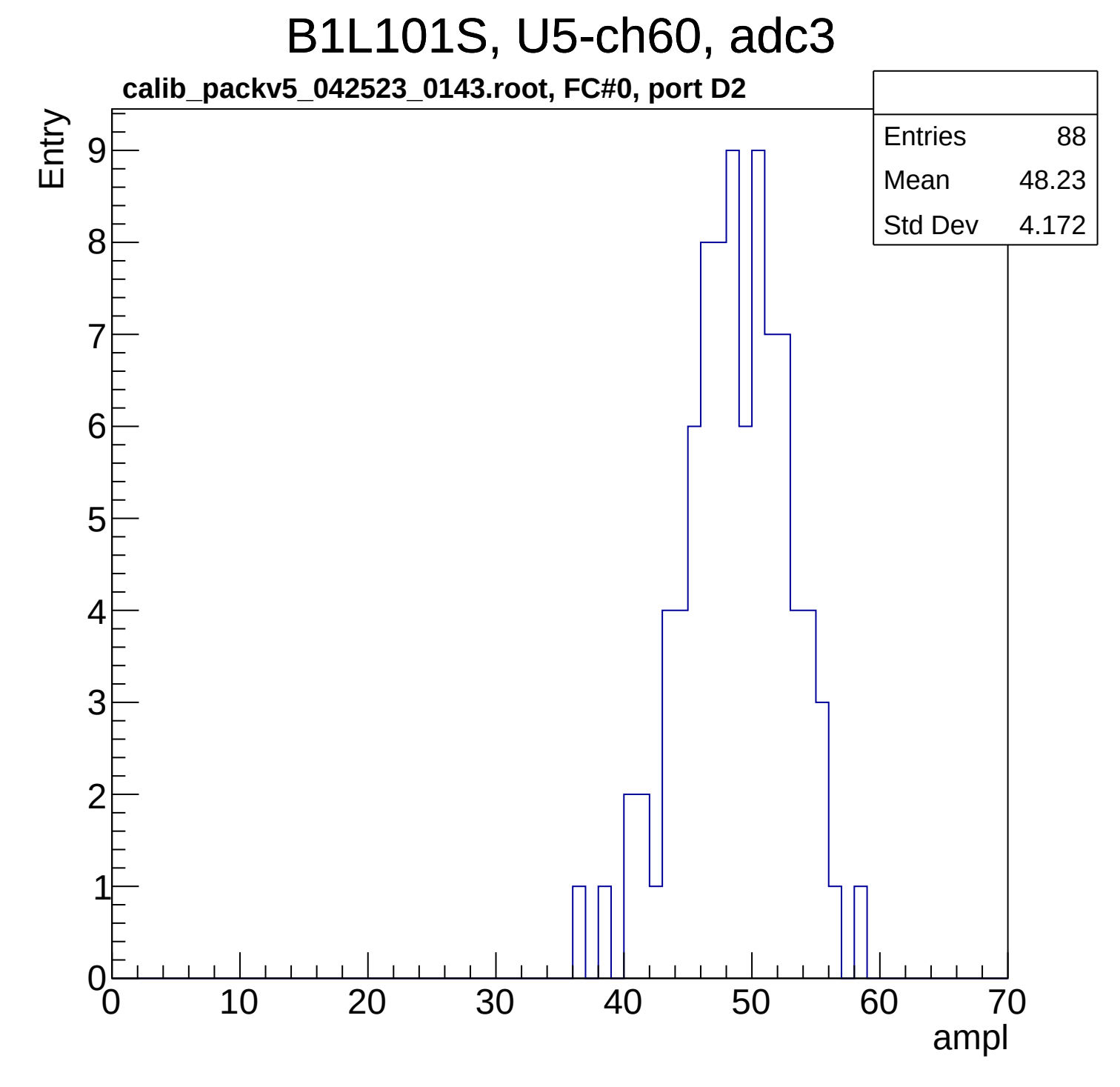
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L101S, U5-ch60, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 41.06
Std Dev 3.385
Gaus mean : 42.1236
Gaus Width: 3.2940
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch60, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 88
Mean 48.23
Std Dev 4.172
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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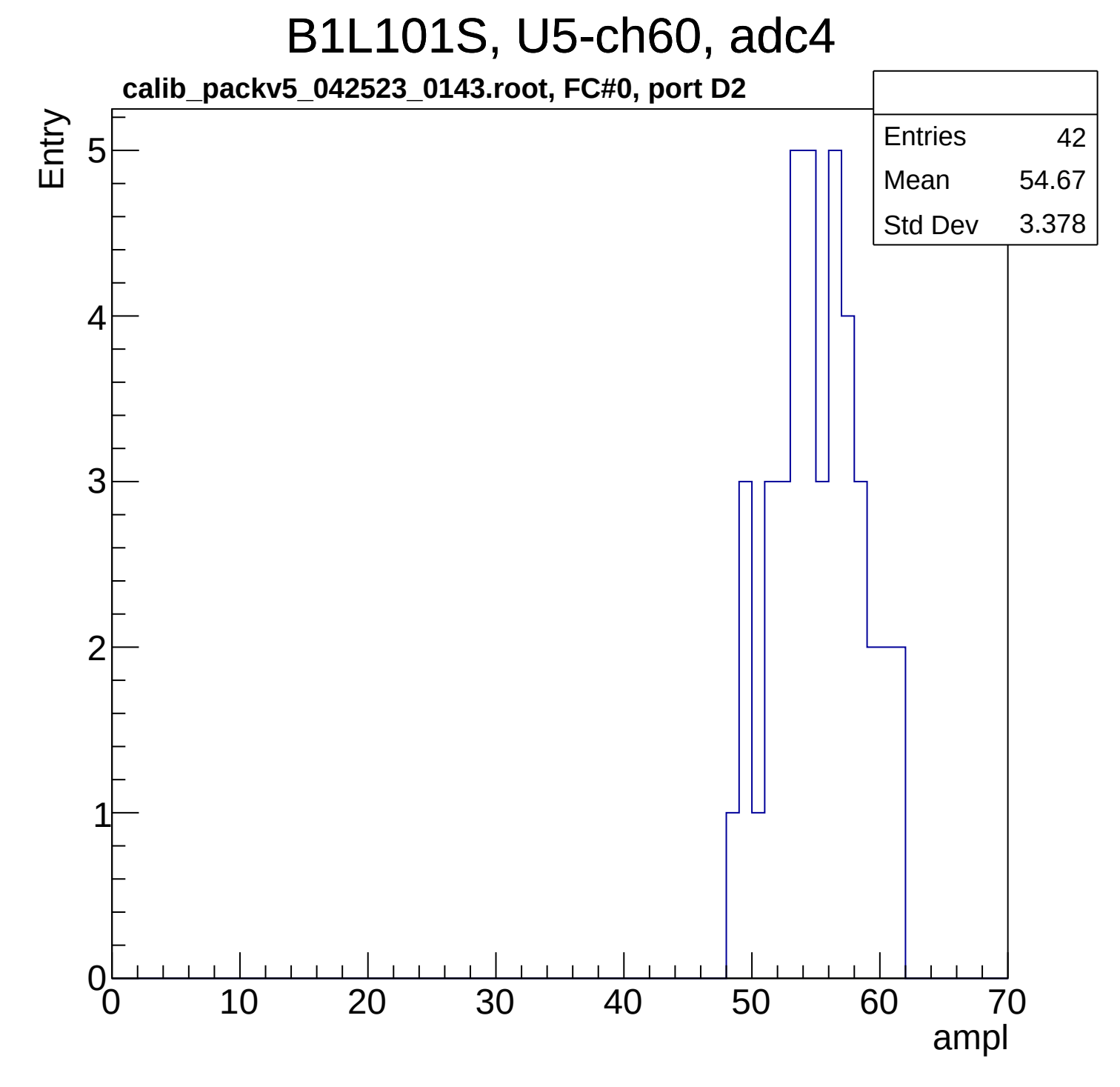
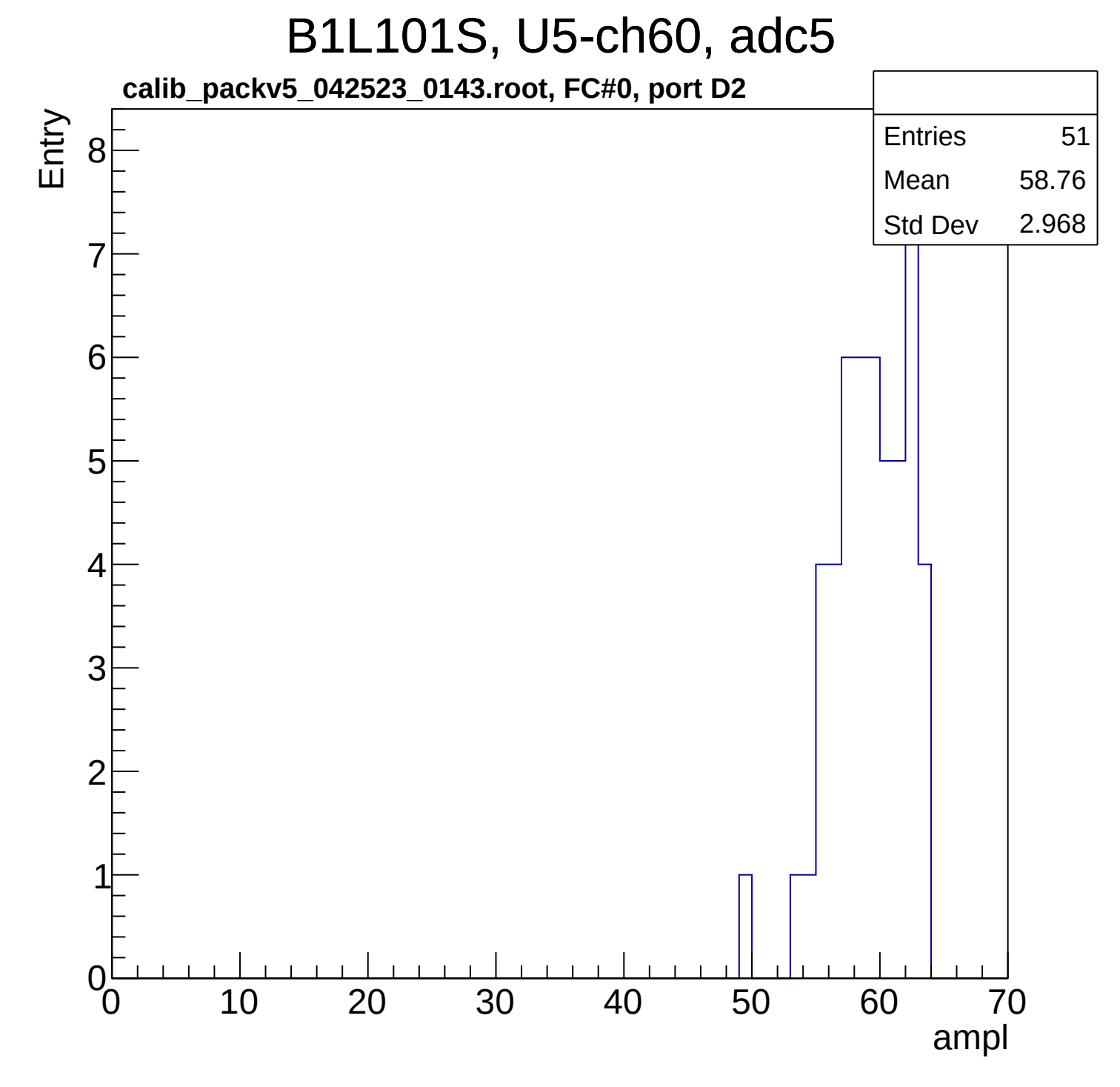
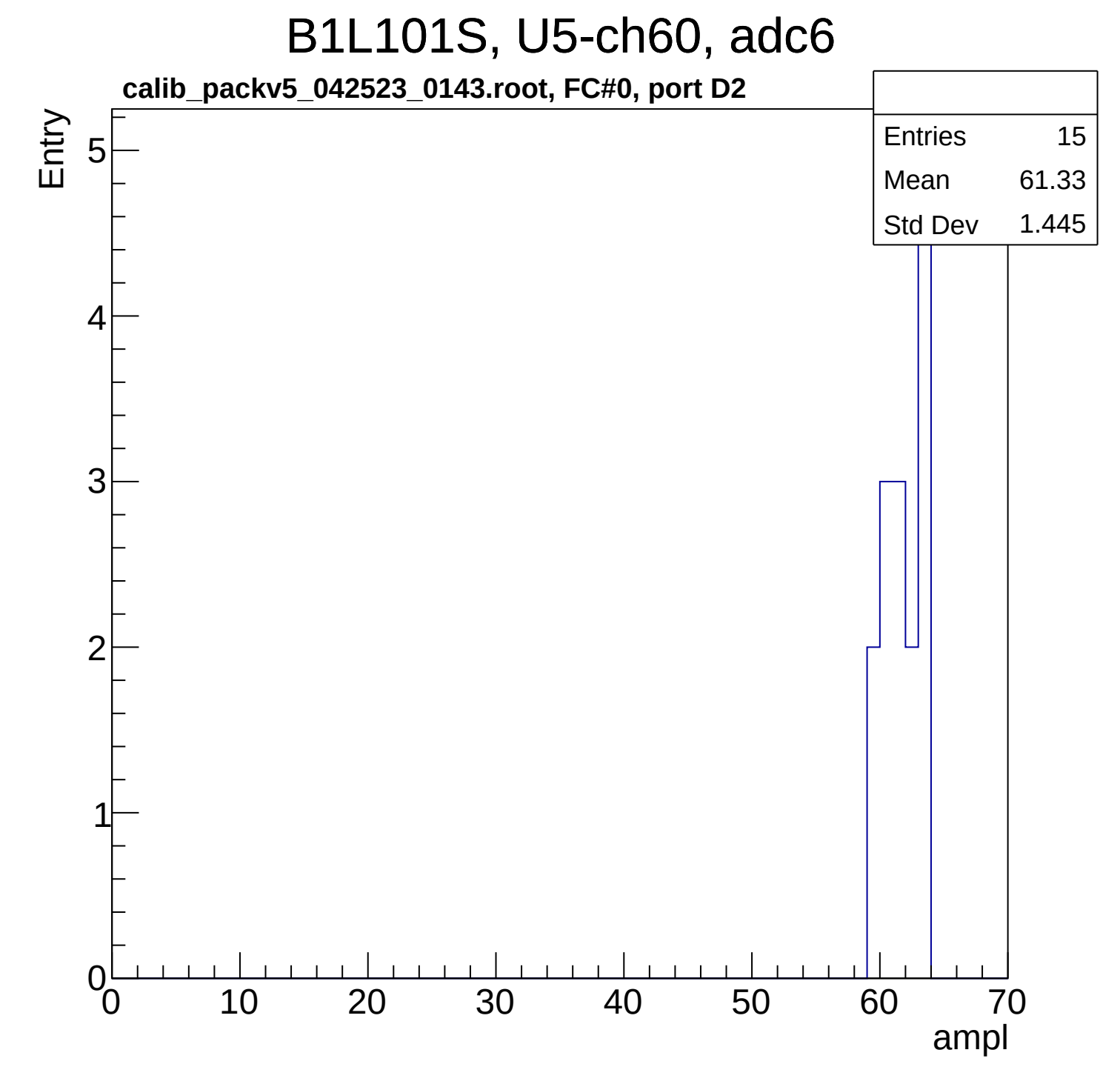
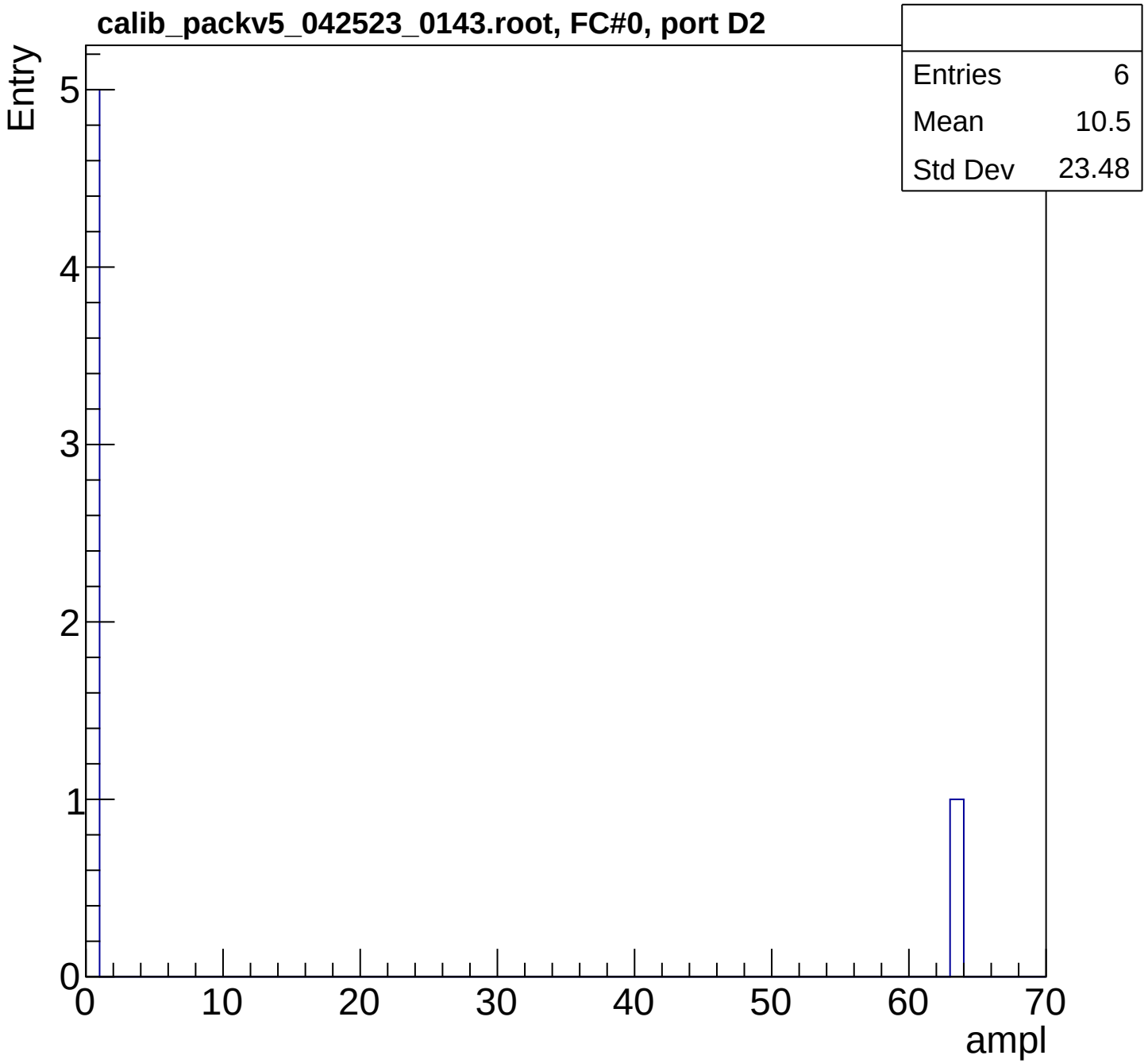
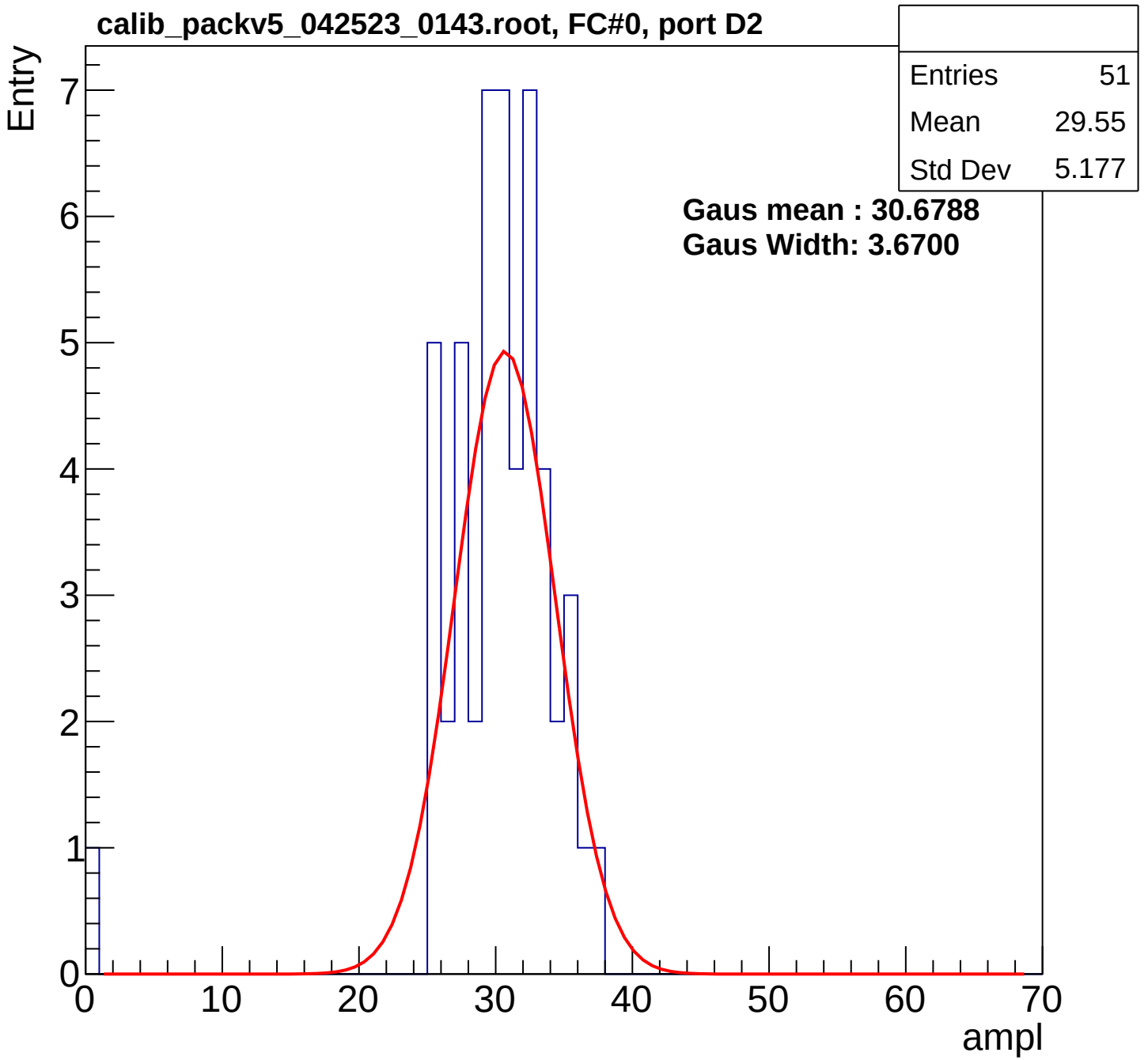
60
70

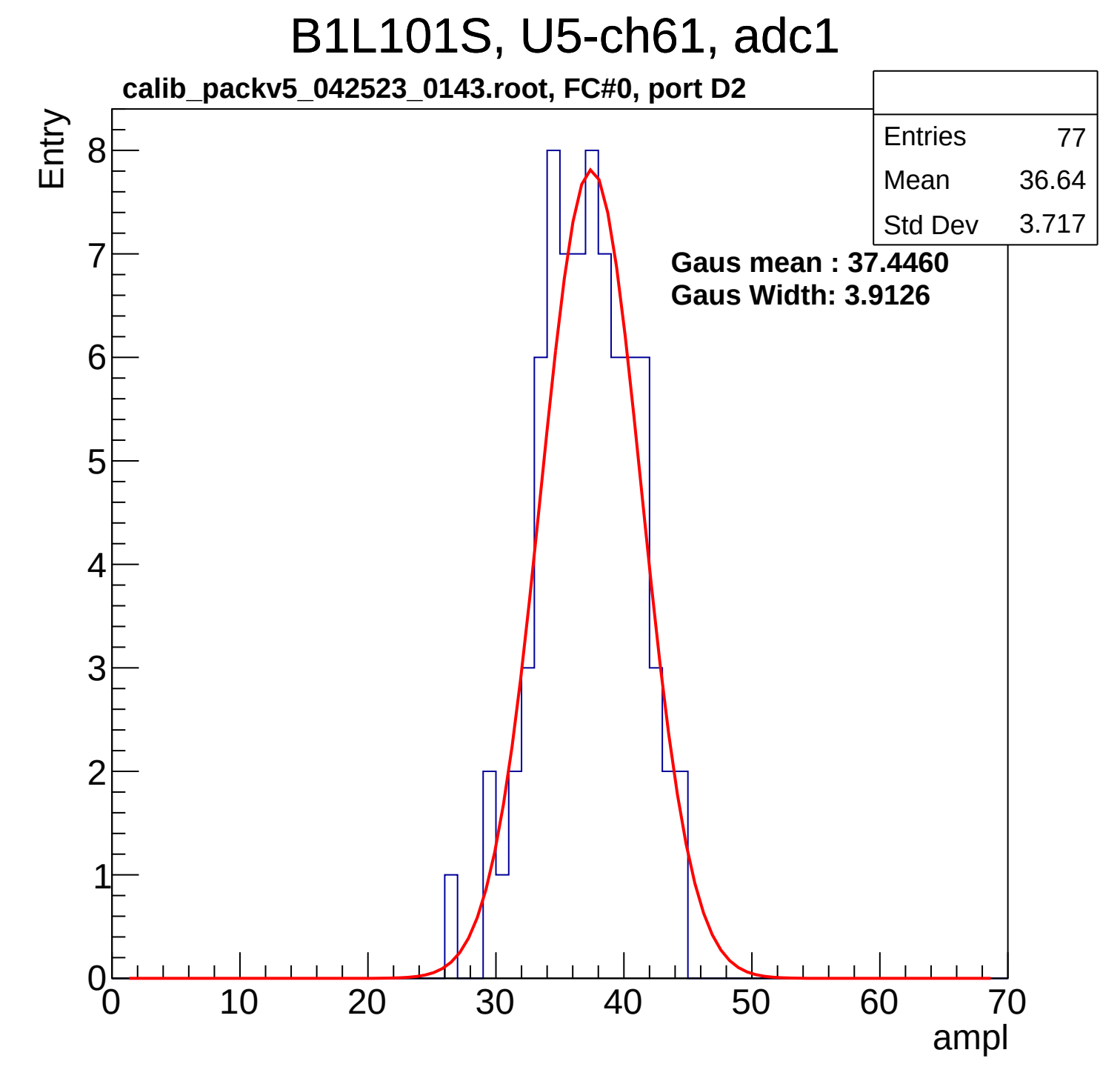

B1L101S, U5-ch60, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 54.67
Std Dev 3.378
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L101S, U5-ch60, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 58.76
Std Dev 2.968
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch60, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 15
Mean 61.33
Std Dev 1.445
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch60, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 10.5
Std Dev 23.48
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch61, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 29.55
Std Dev 5.177
Gaus mean : 30.6788
Gaus Width: 3.6700
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch61, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 36.64
Std Dev 3.717
Gaus mean : 37.4460
Gaus Width: 3.9126
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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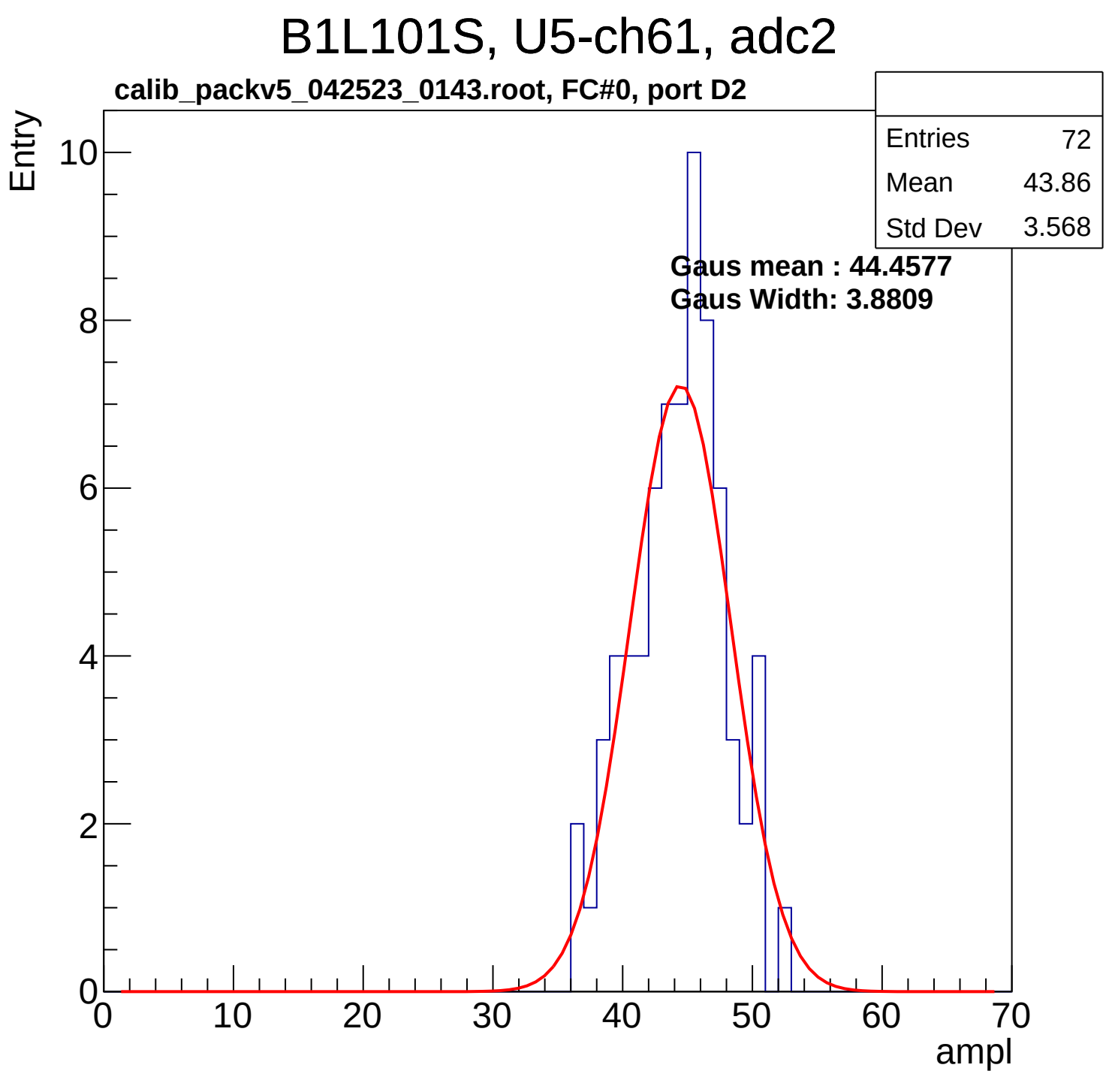
B1L101S, U5-ch61, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 43.86
Std Dev 3.568
Gaus mean : 44.4577
Gaus Width: 3.8809
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
50
60
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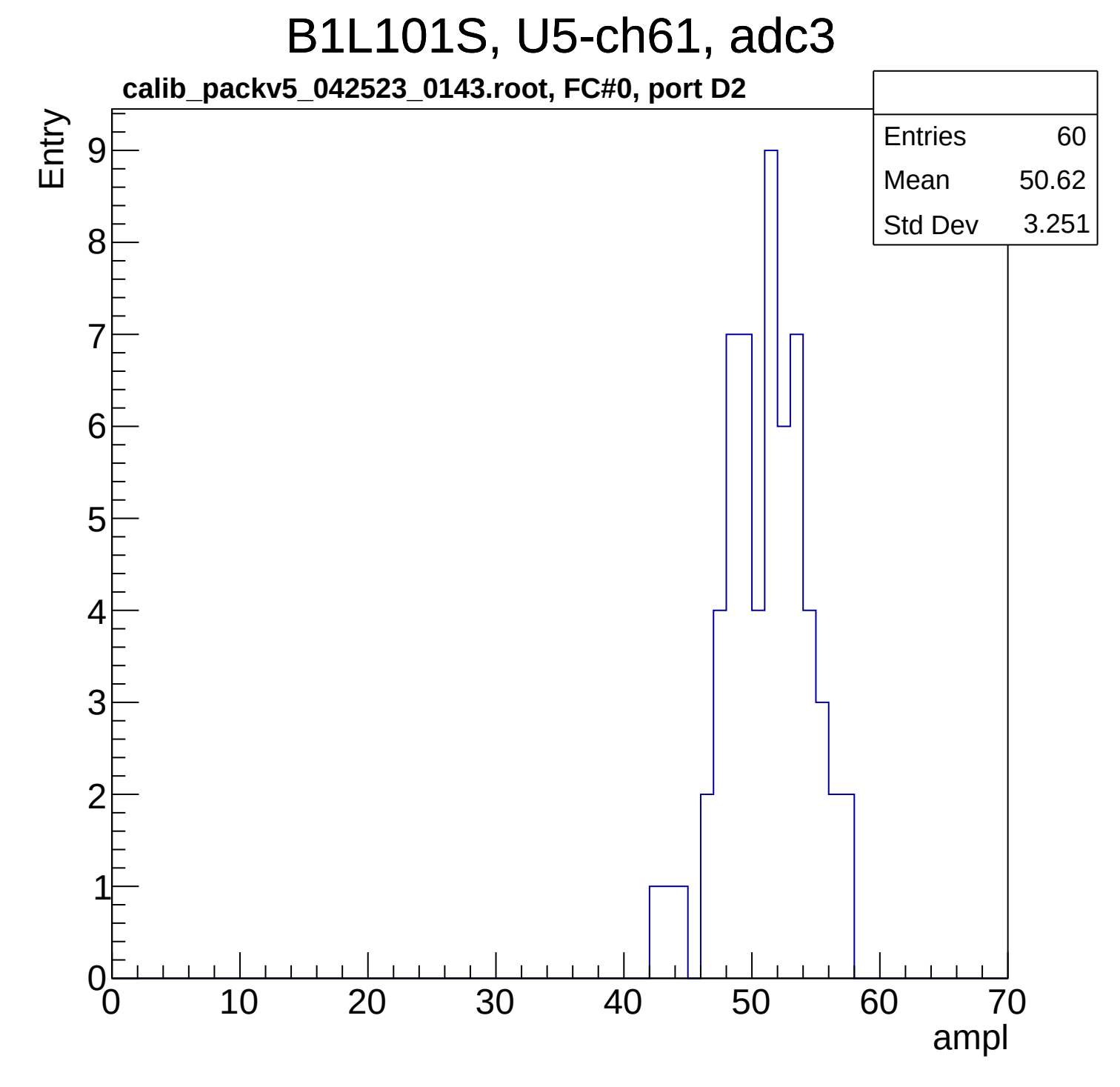
B1L101S, U5-ch61, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 50.62
Std Dev 3.251
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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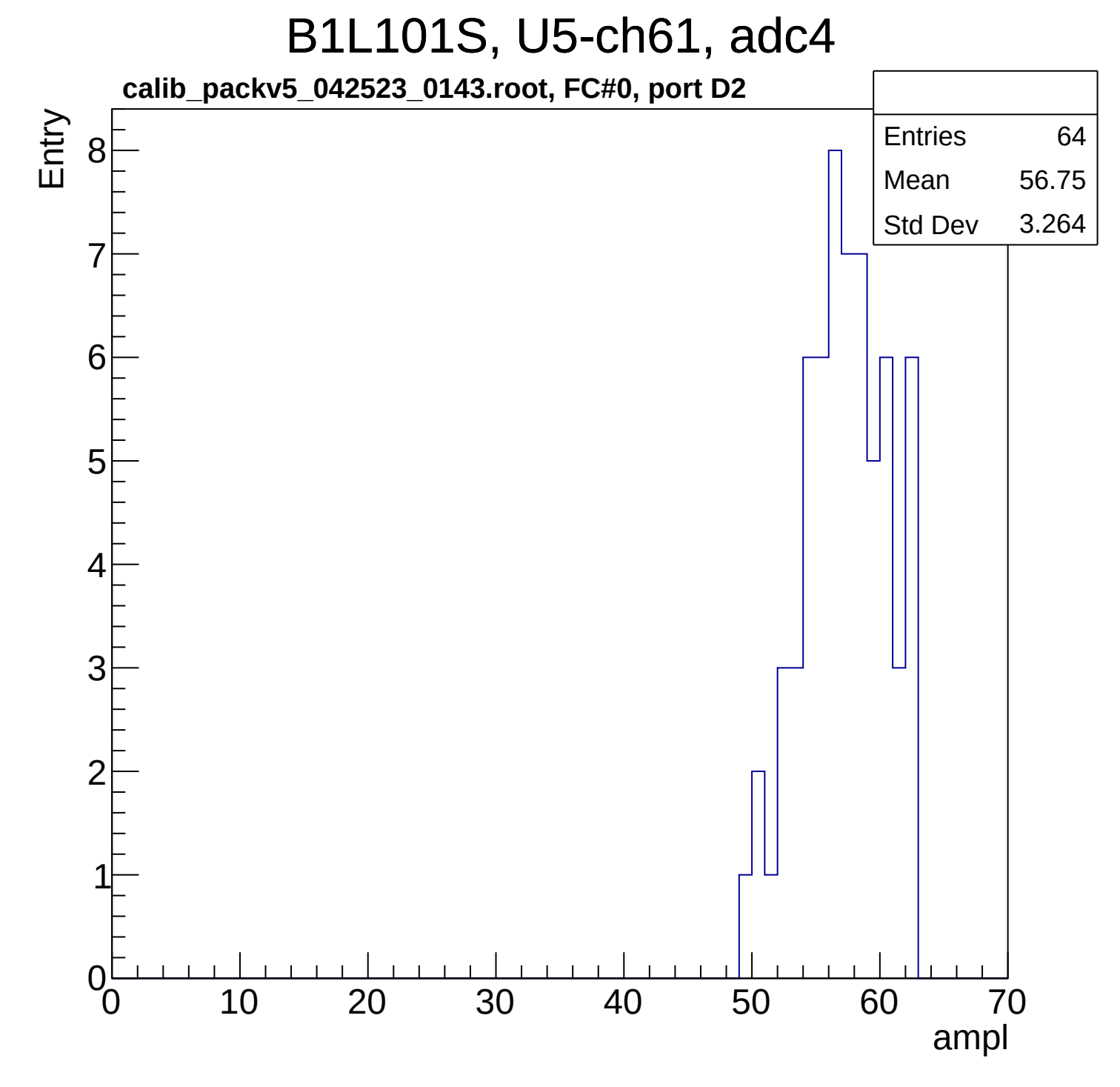
B1L101S, U5-ch61, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 56.75
Std Dev 3.264
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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60
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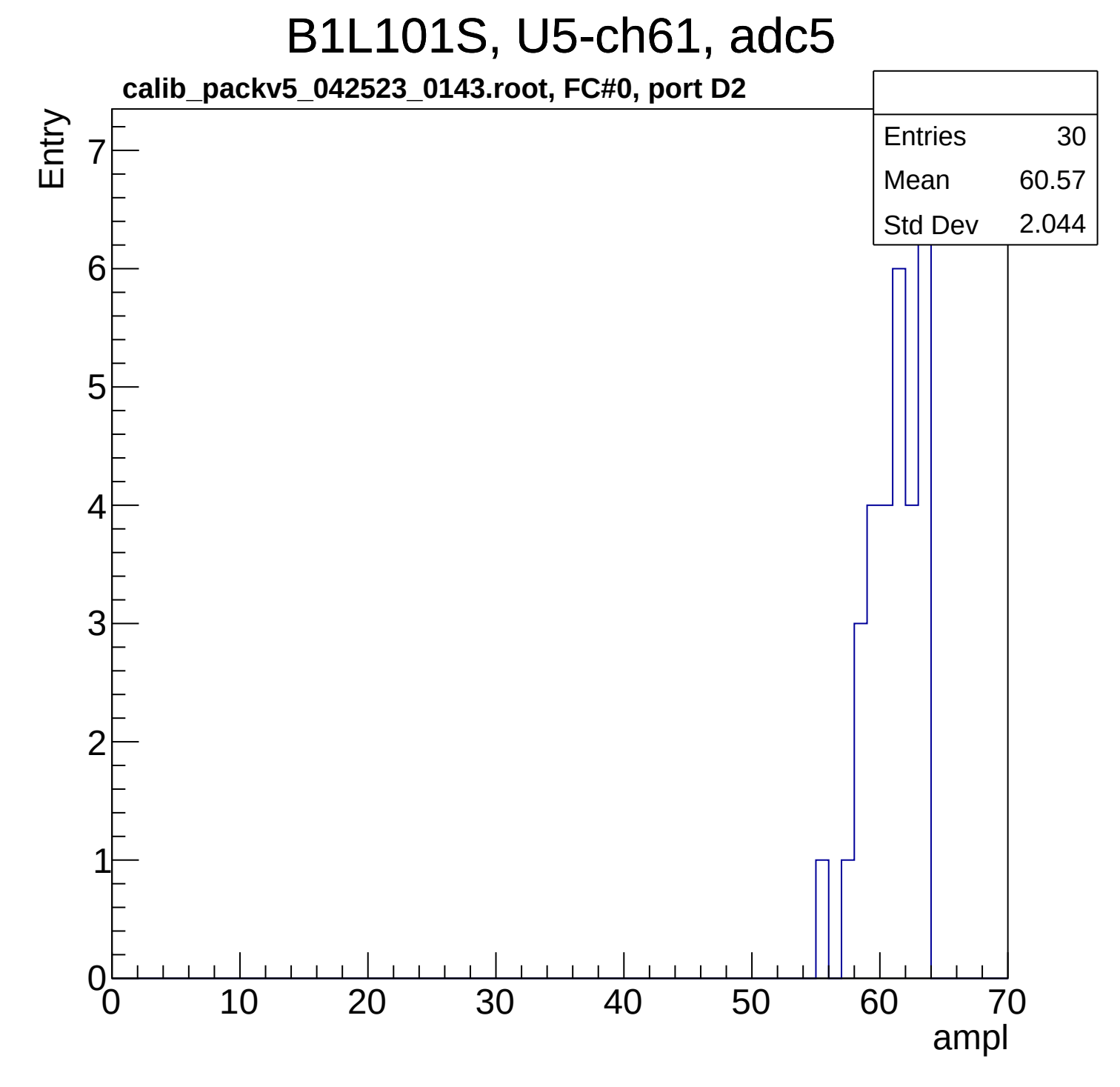
B1L101S, U5-ch61, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 30
Mean 60.57
Std Dev 2.044
Entry
ampl
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1
2
3
4
5
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0
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60
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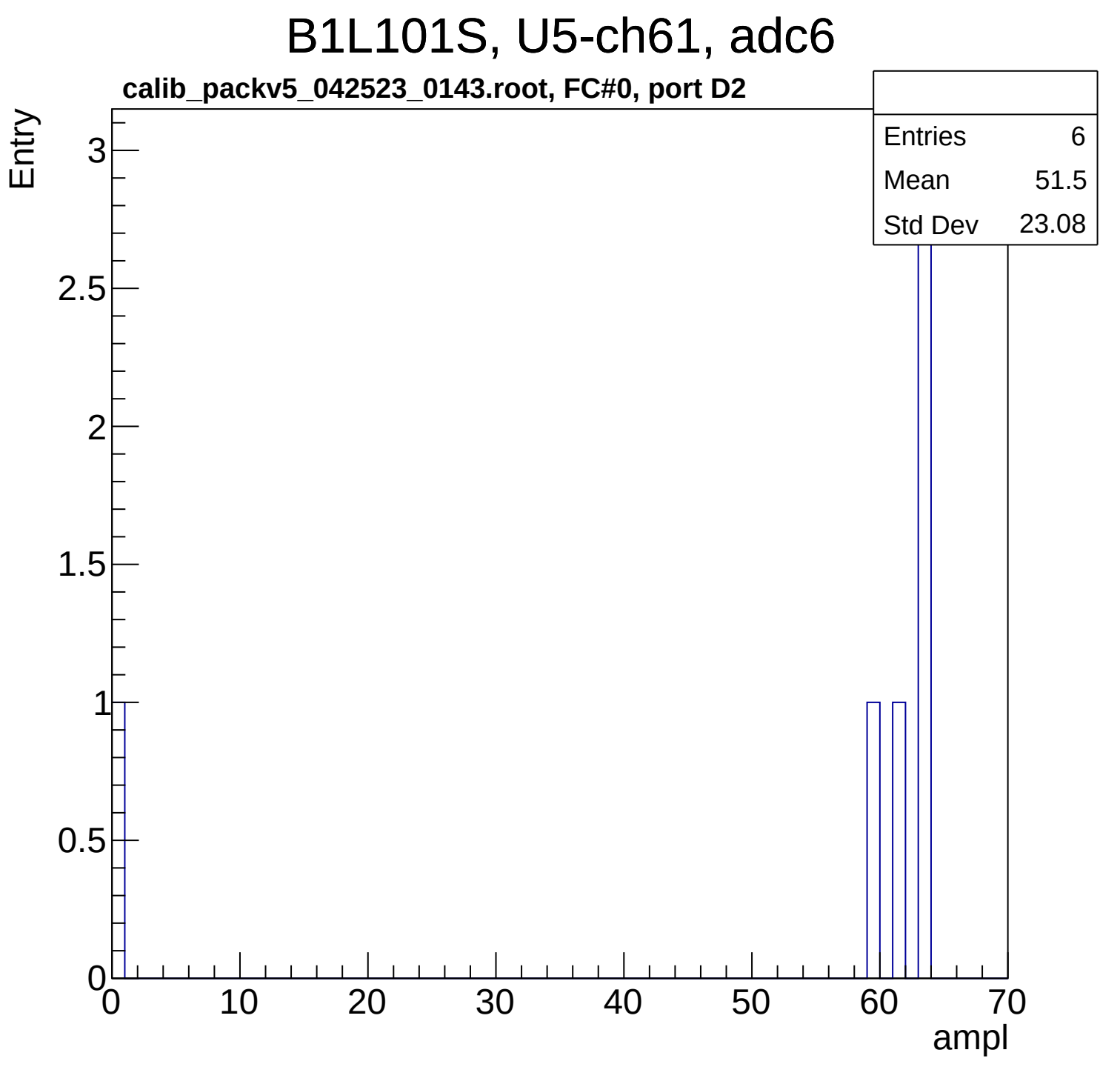
B1L101S, U5-ch61, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 51.5
Std Dev 23.08
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
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20
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40
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60
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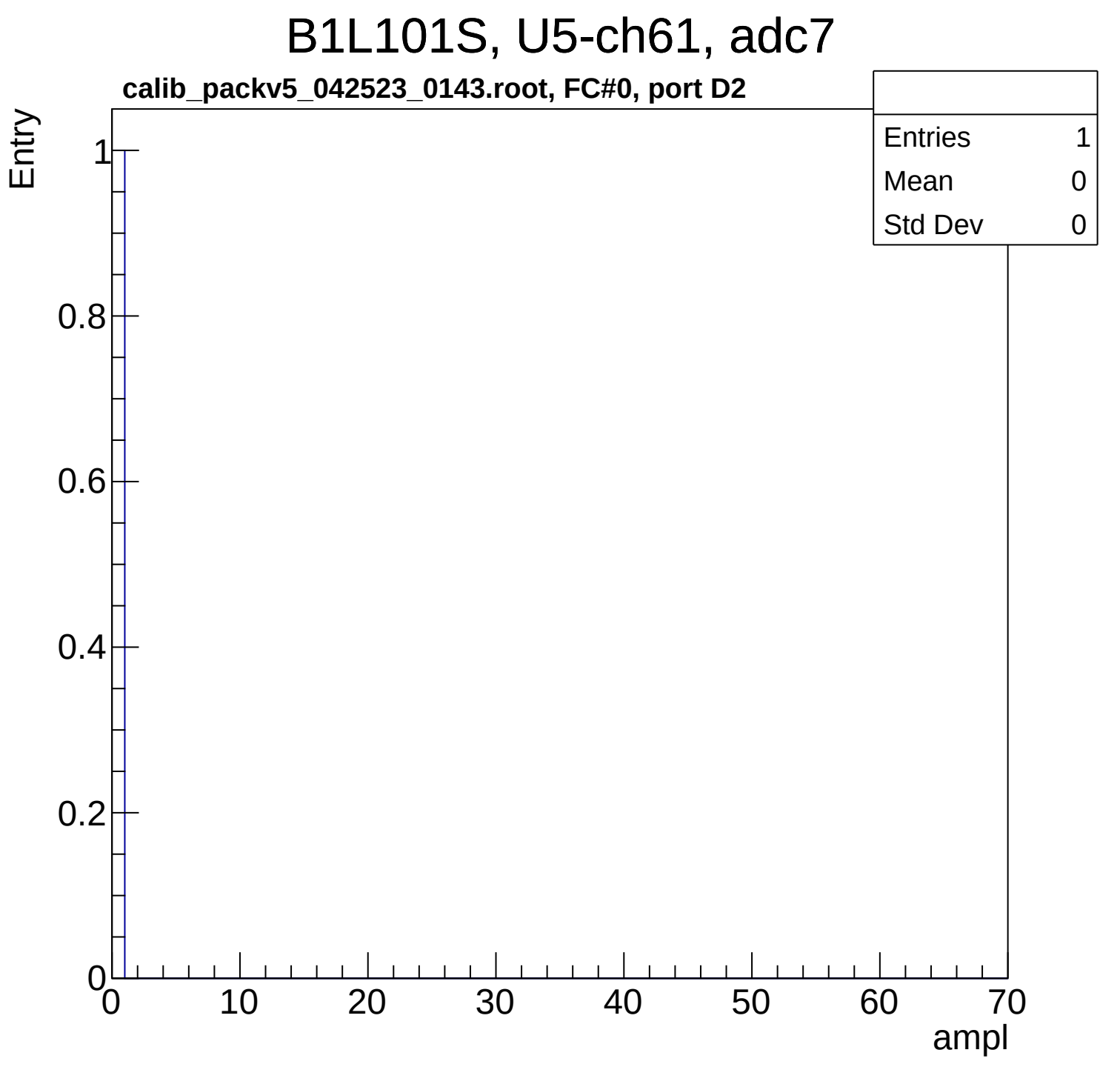
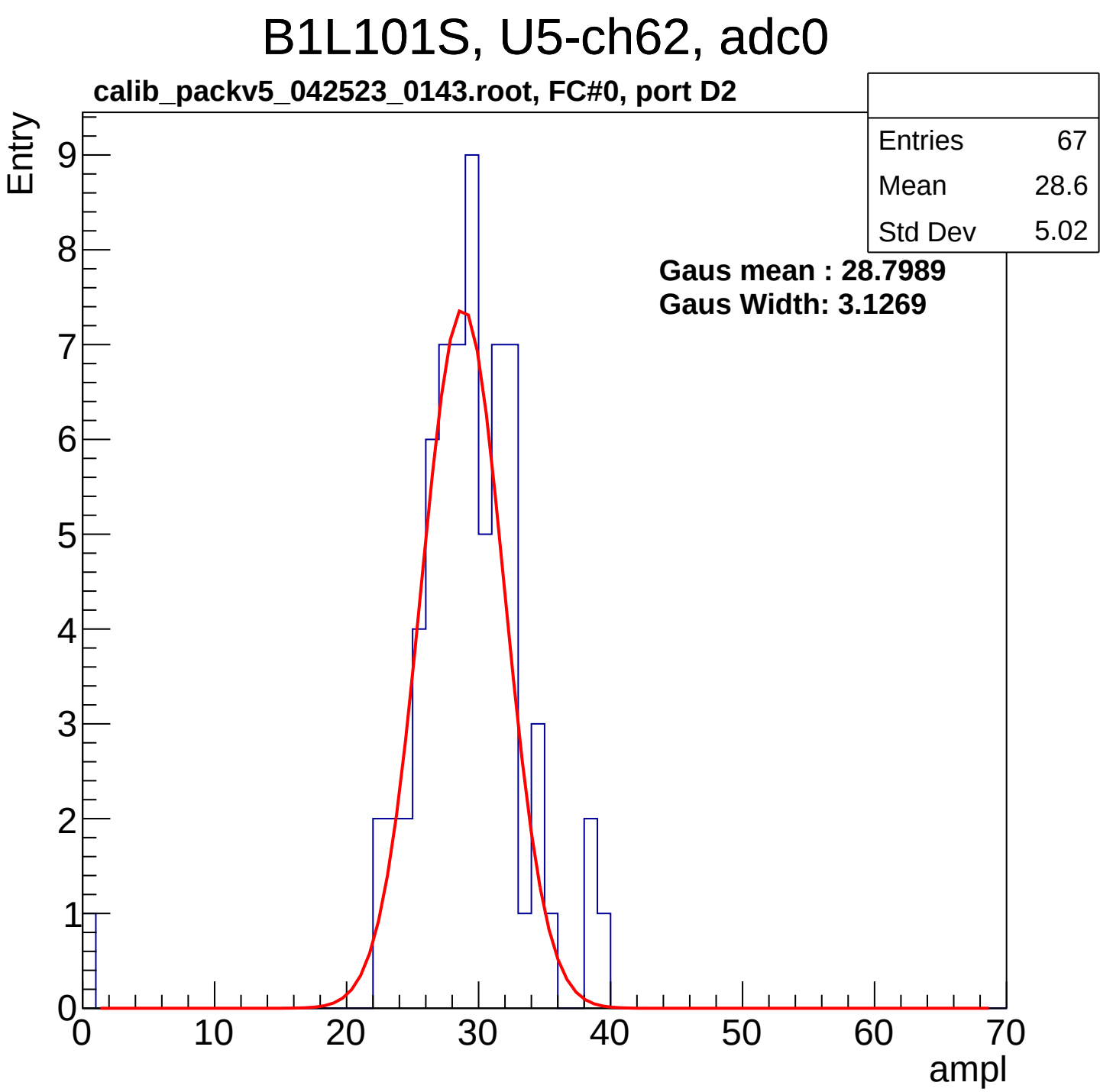

B1L101S, U5-ch61, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch62, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 28.6
Std Dev 5.02
Gaus mean : 28.7989
Gaus Width: 3.1269
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
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60
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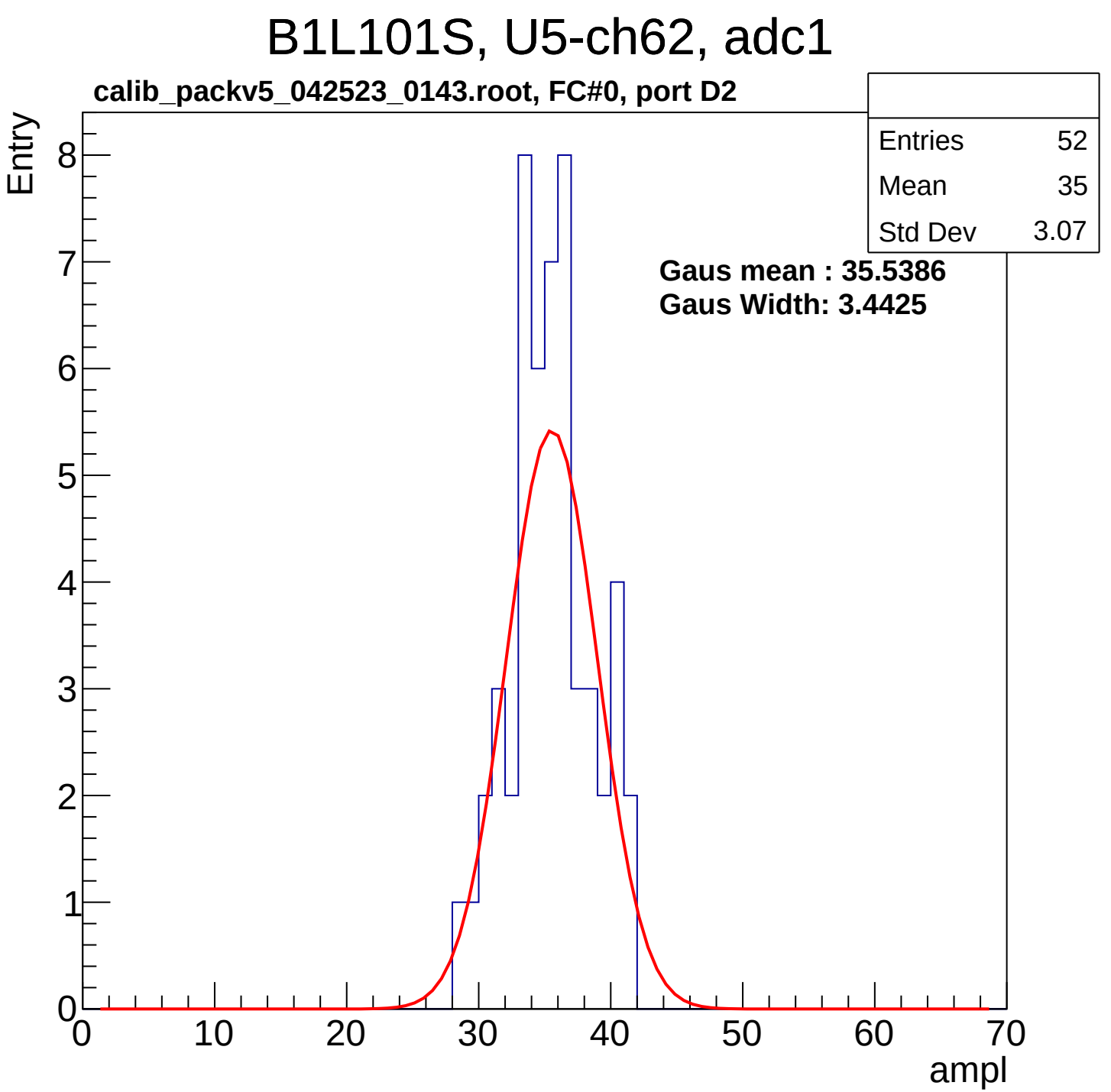
B1L101S, U5-ch62, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 35
Std Dev 3.07
Gaus mean : 35.5386
Gaus Width: 3.4425
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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40
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60
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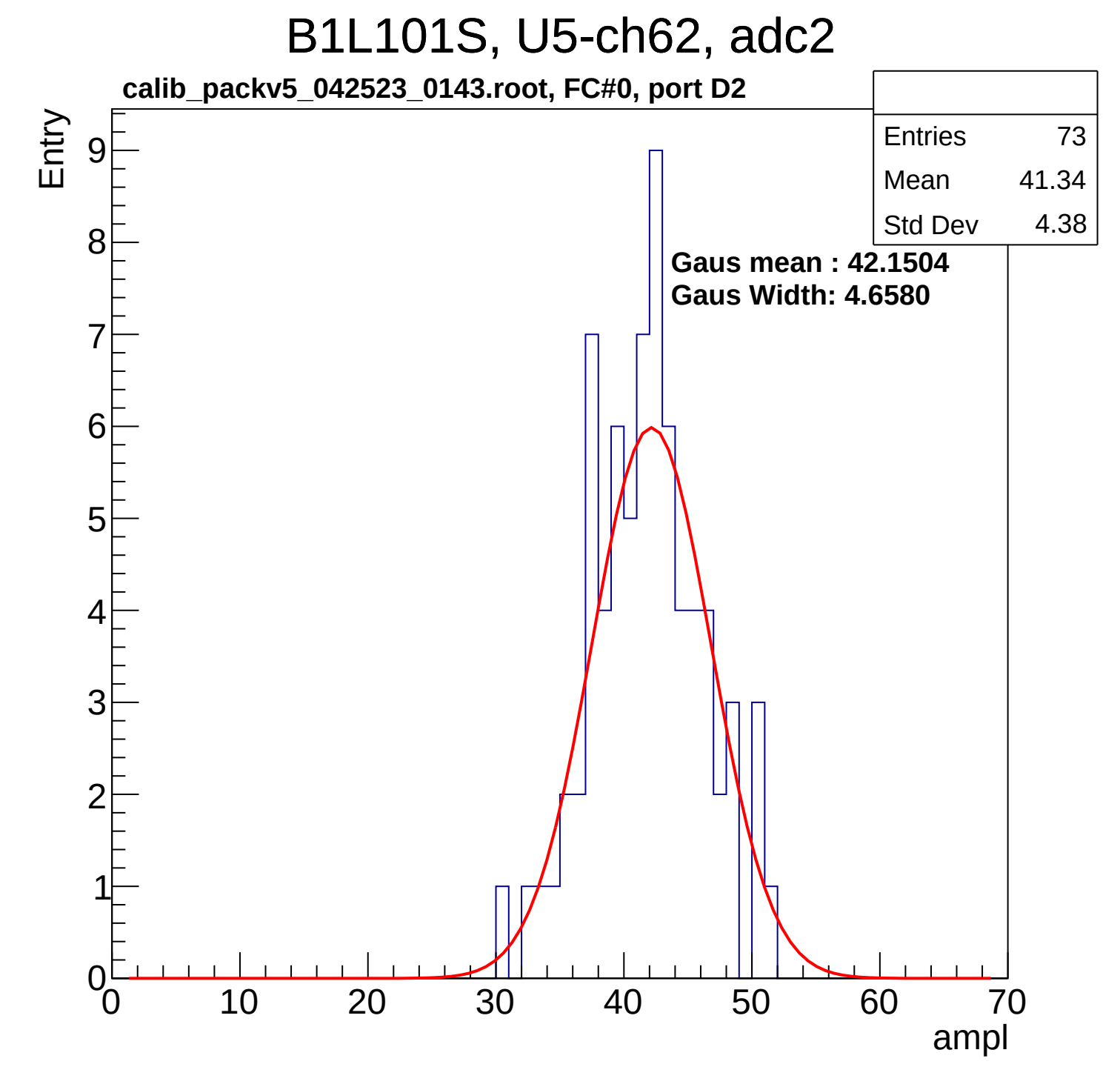
B1L101S, U5-ch62, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 41.34
Std Dev 4.38
Gaus mean : 42.1504
Gaus Width: 4.6580
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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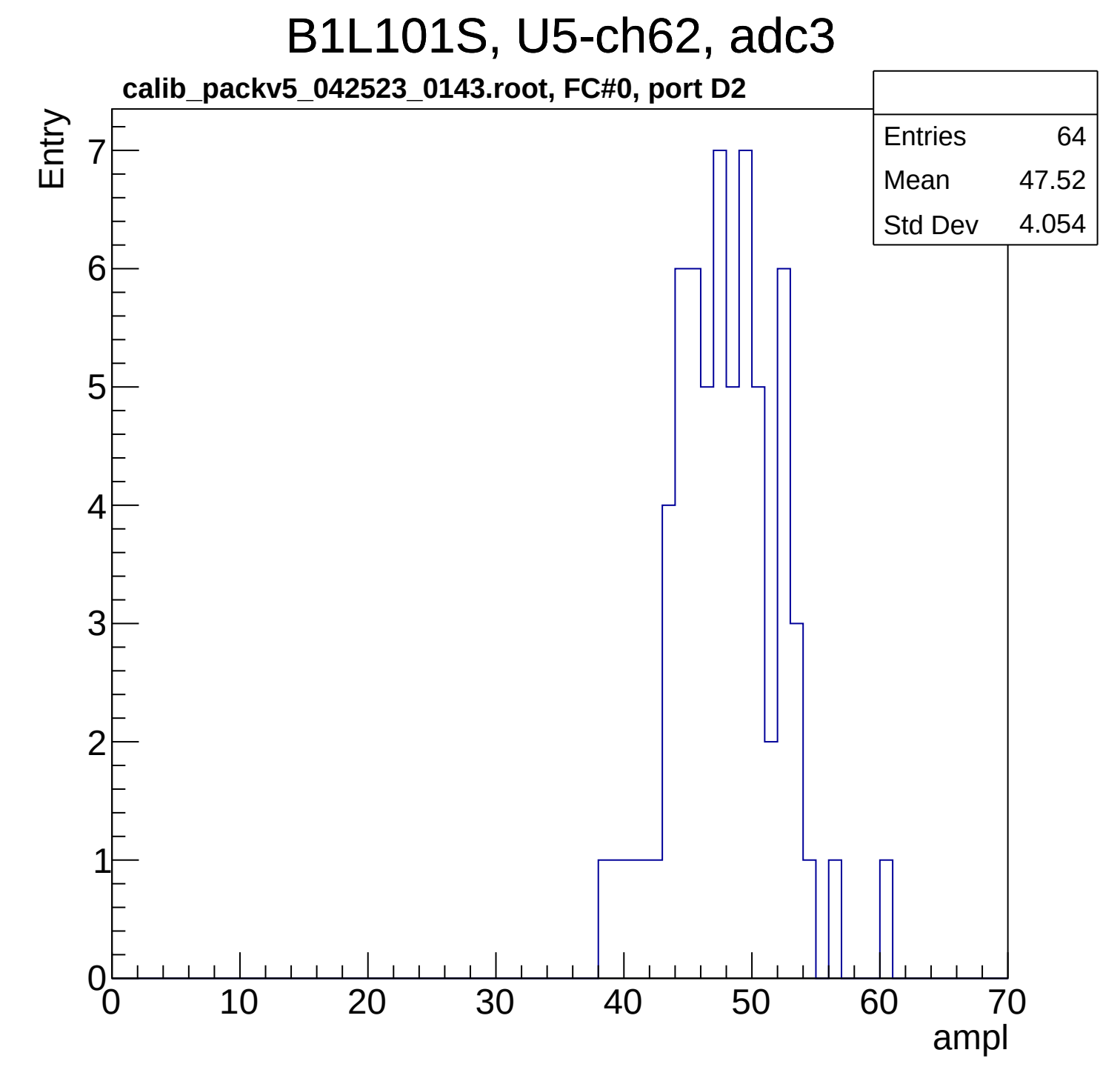
B1L101S, U5-ch62, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 47.52
Std Dev 4.054
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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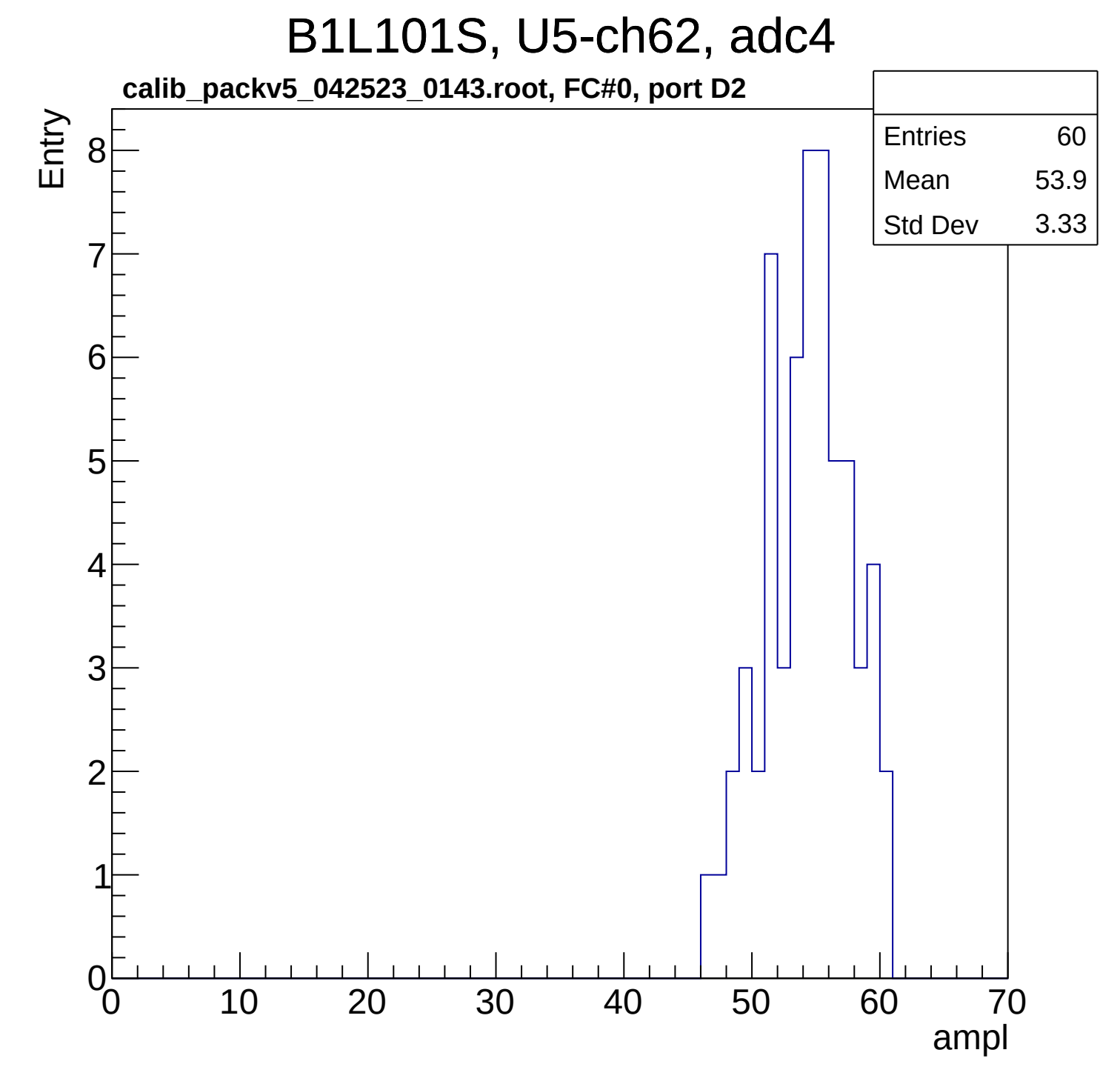
B1L101S, U5-ch62, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 53.9
Std Dev 3.33
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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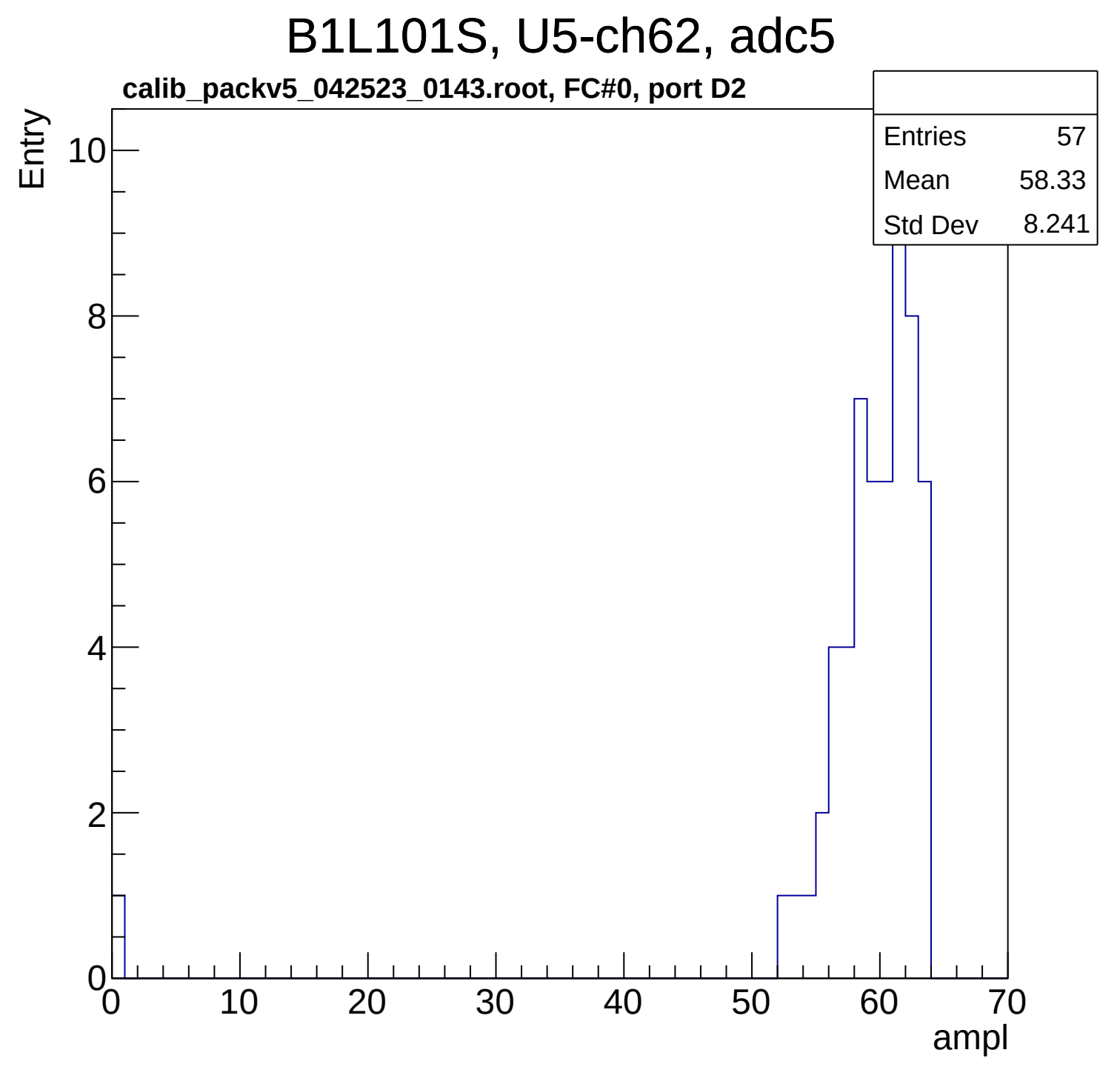
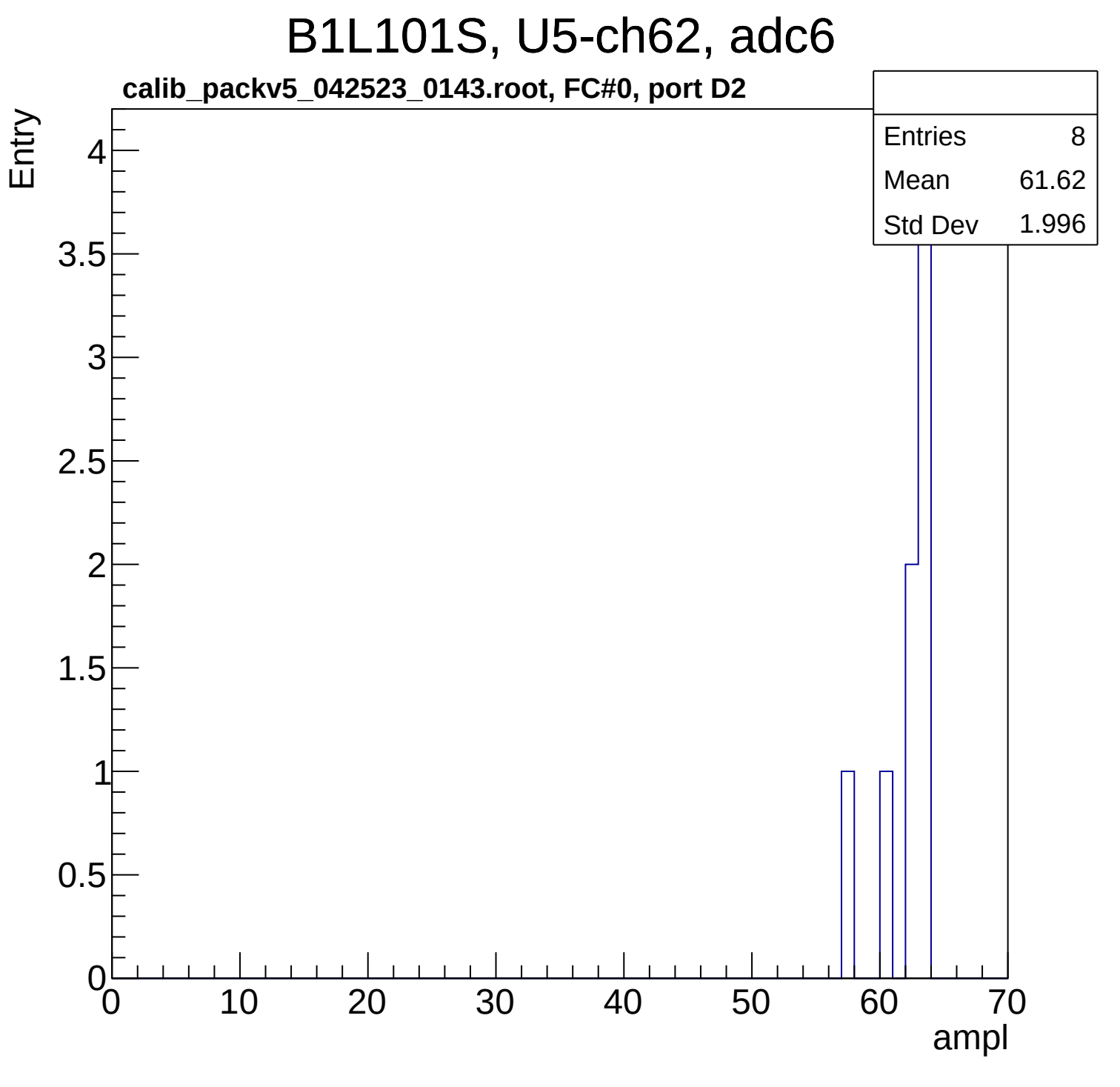
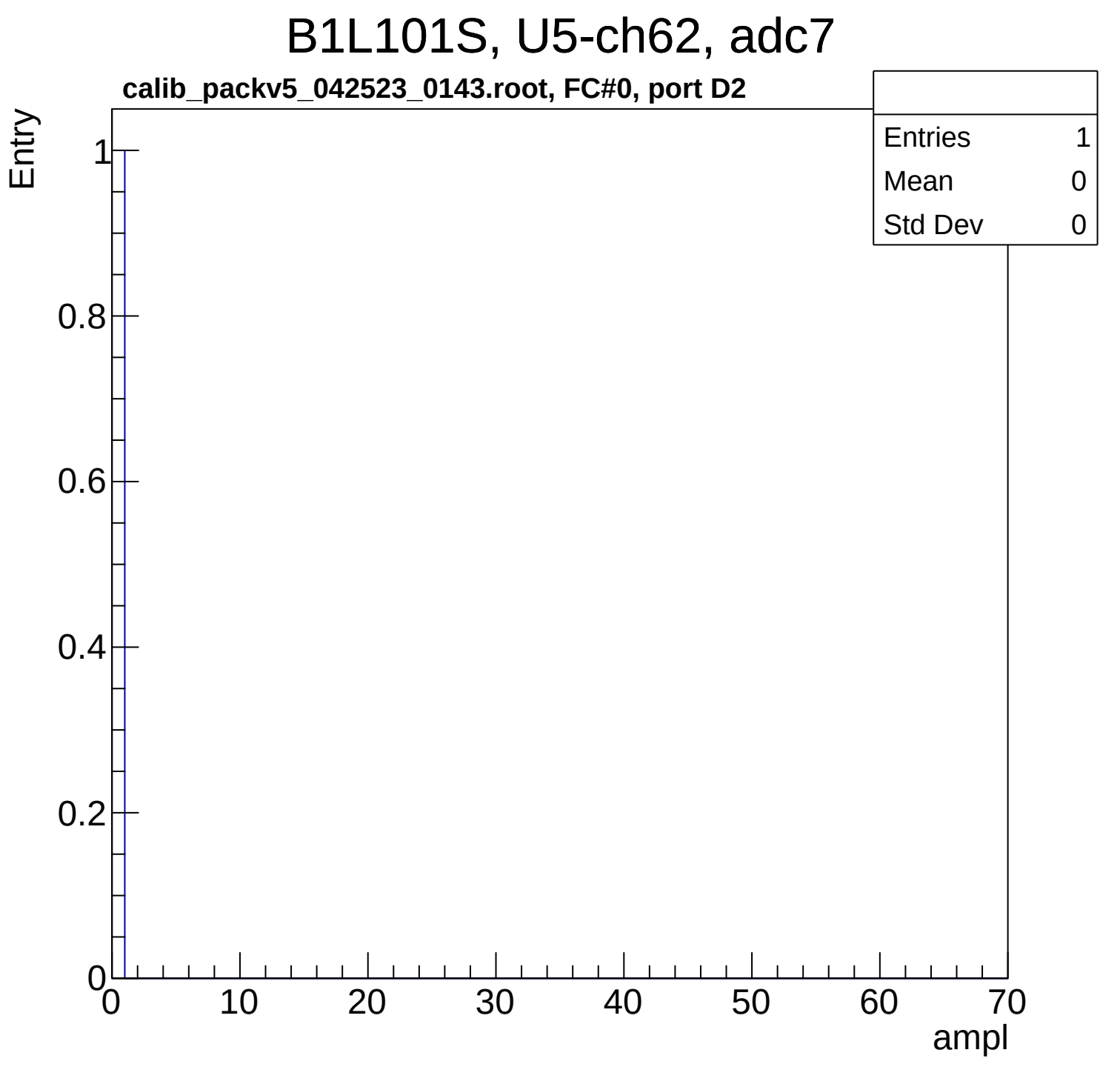
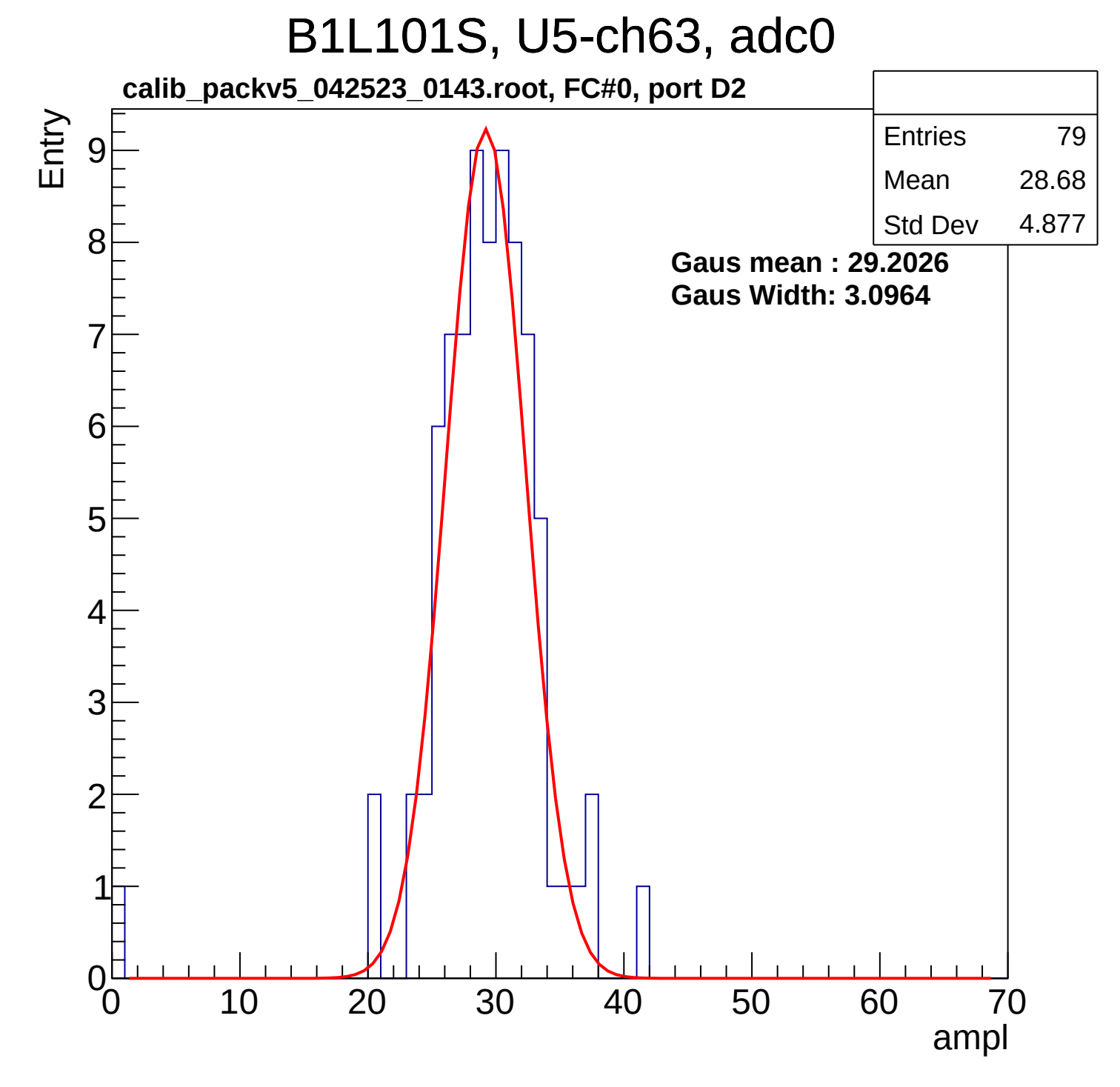

B1L101S, U5-ch62, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 58.33
Std Dev 8.241
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch62, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 61.62
Std Dev 1.996
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L101S, U5-ch62, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch63, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 28.68
Std Dev 4.877
Gaus mean : 29.2026
Gaus Width: 3.0964
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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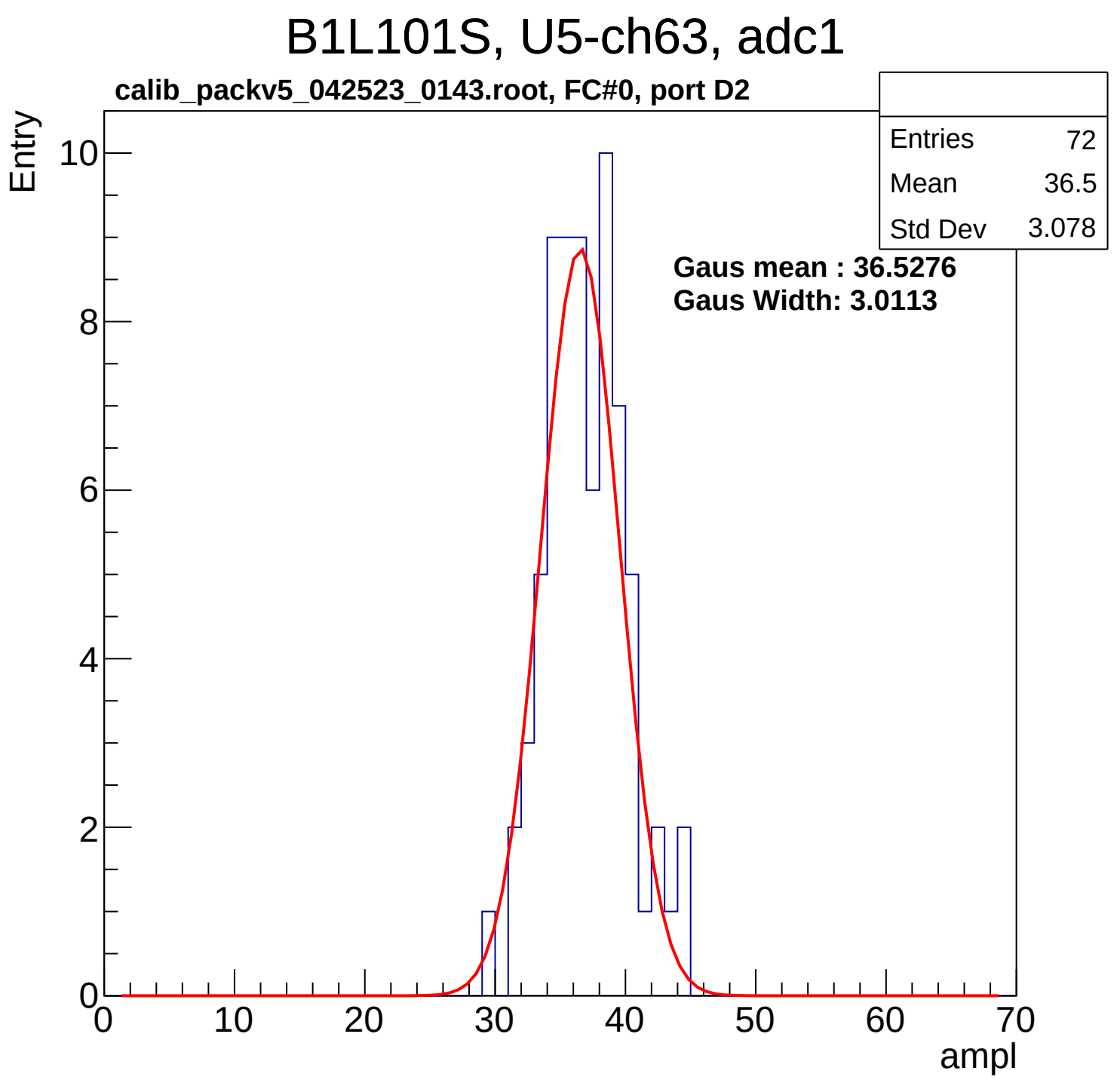
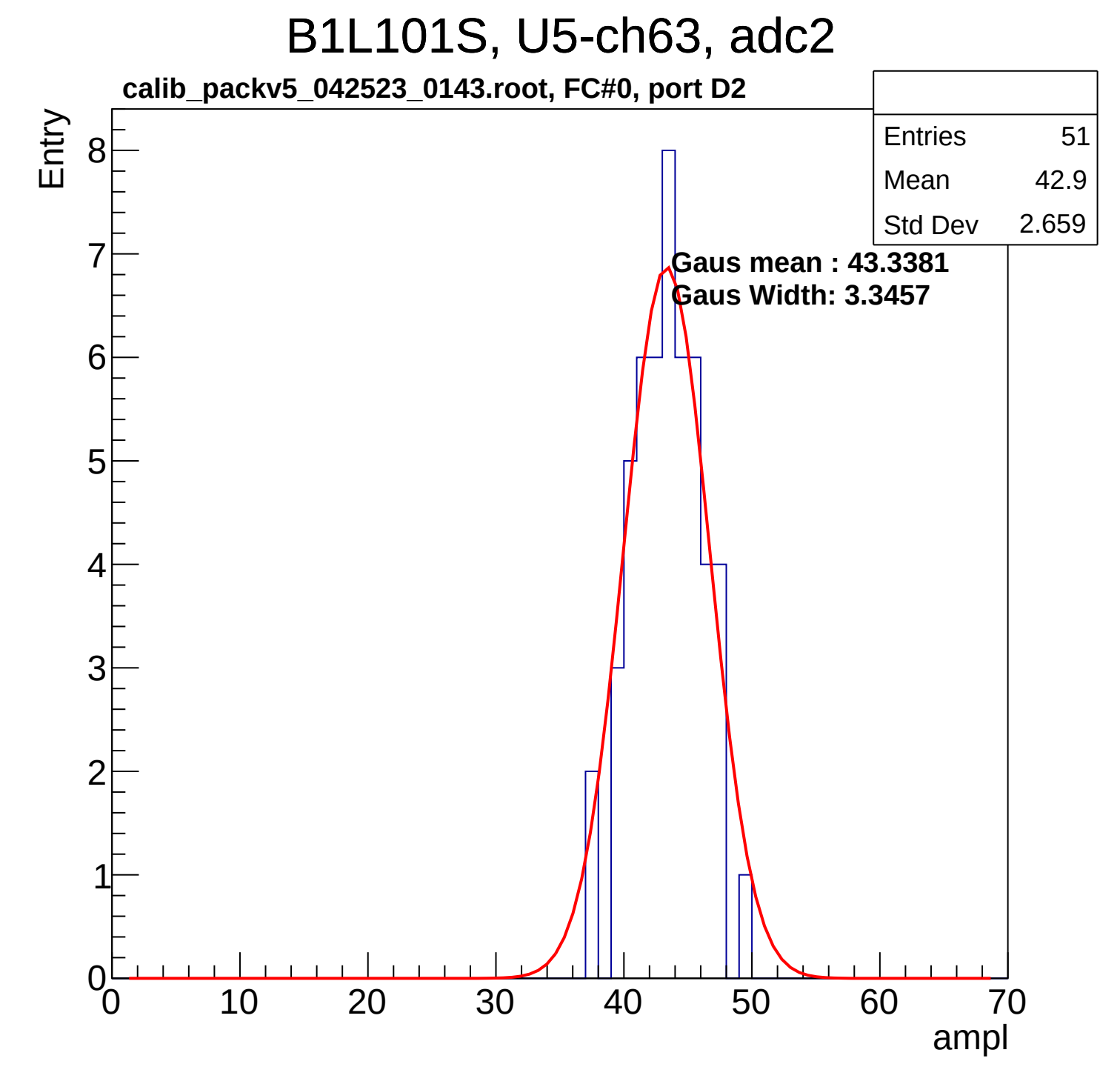
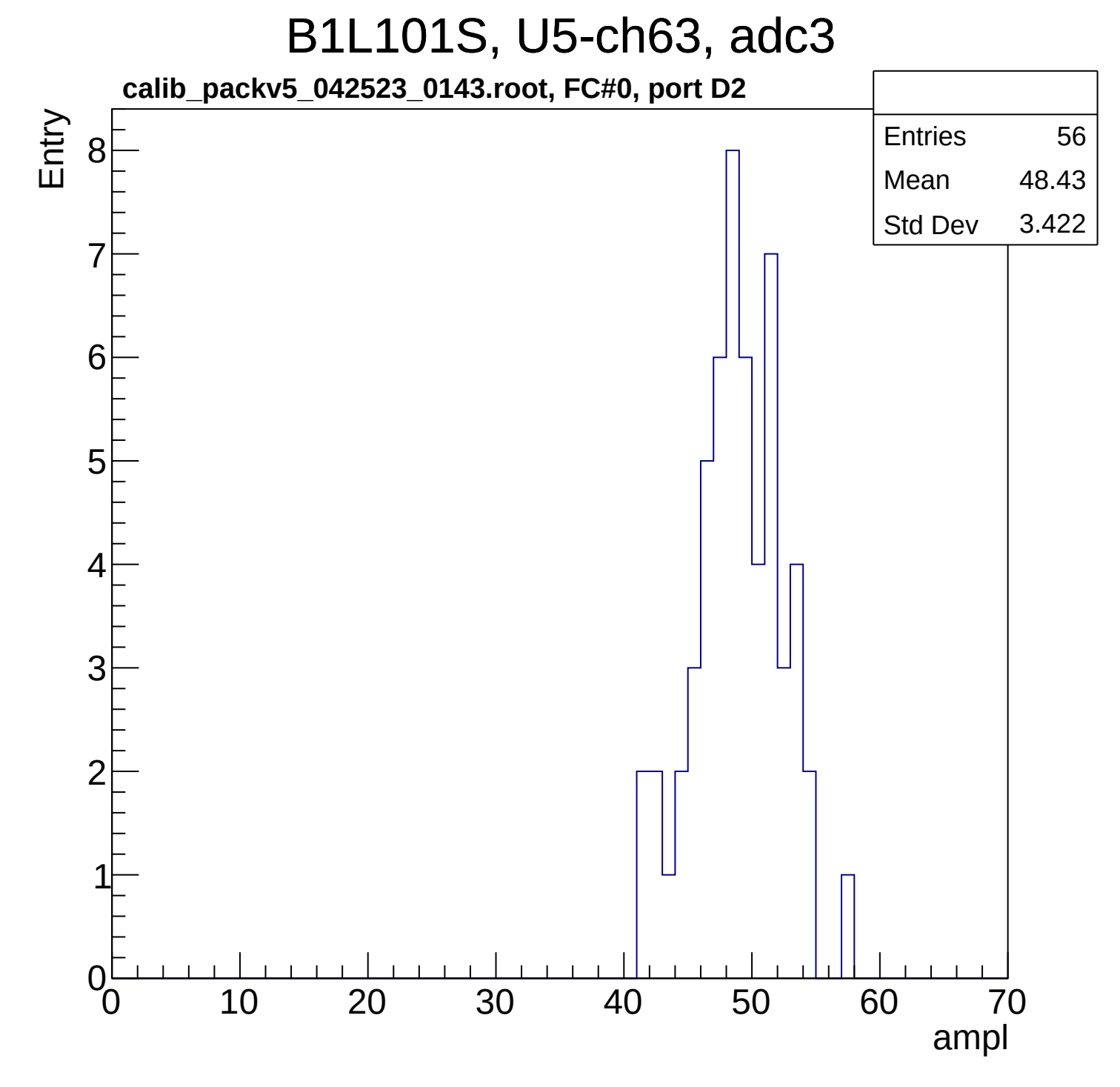

B1L101S, U5-ch63, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 36.5
Std Dev 3.078
Gaus mean : 36.5276
Gaus Width: 3.0113
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch63, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 42.9
Std Dev 2.659
Gaus mean : 43.3381
Gaus Width: 3.3457
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch63, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 48.43
Std Dev 3.422
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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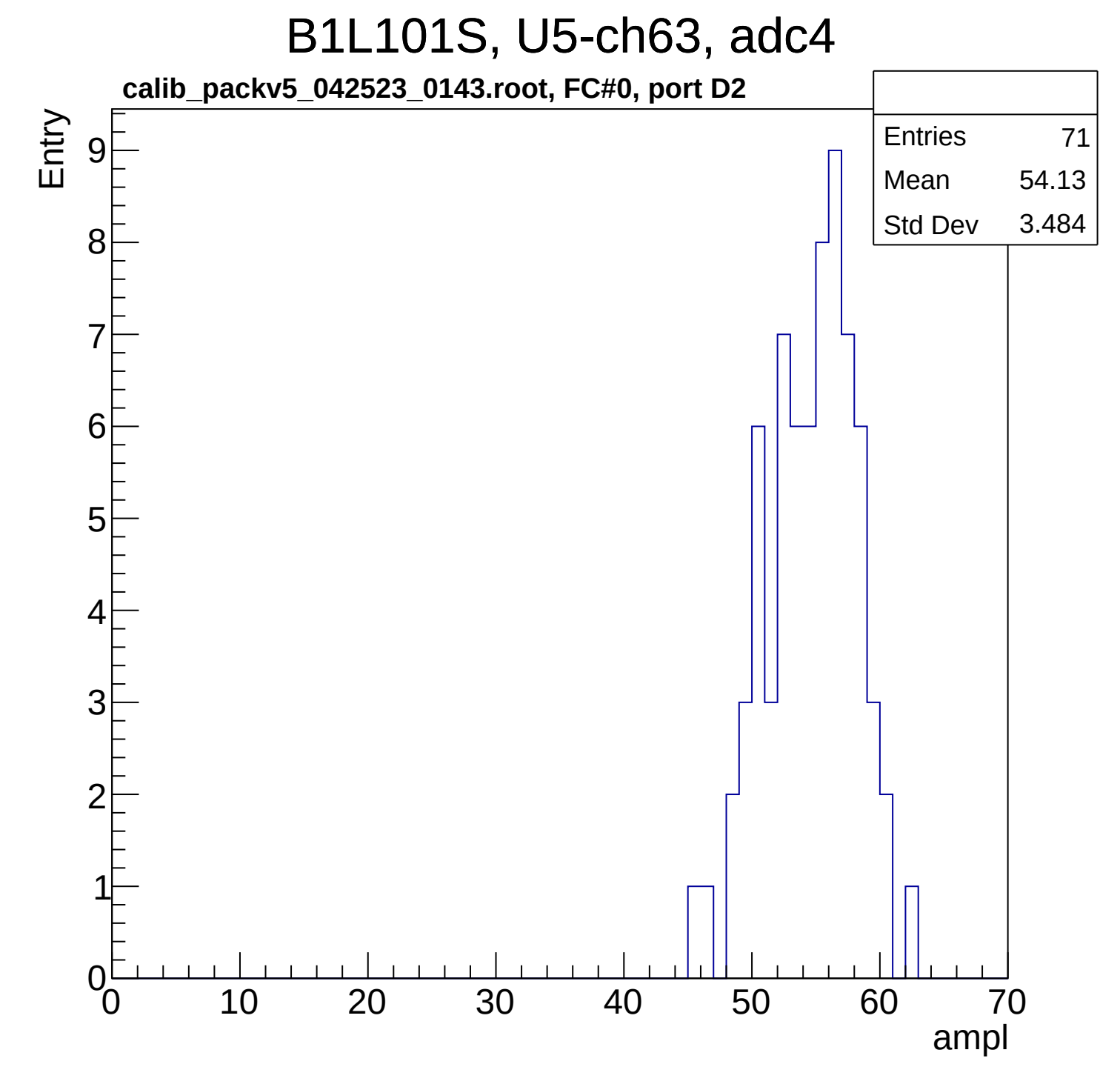
B1L101S, U5-ch63, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 54.13
Std Dev 3.484
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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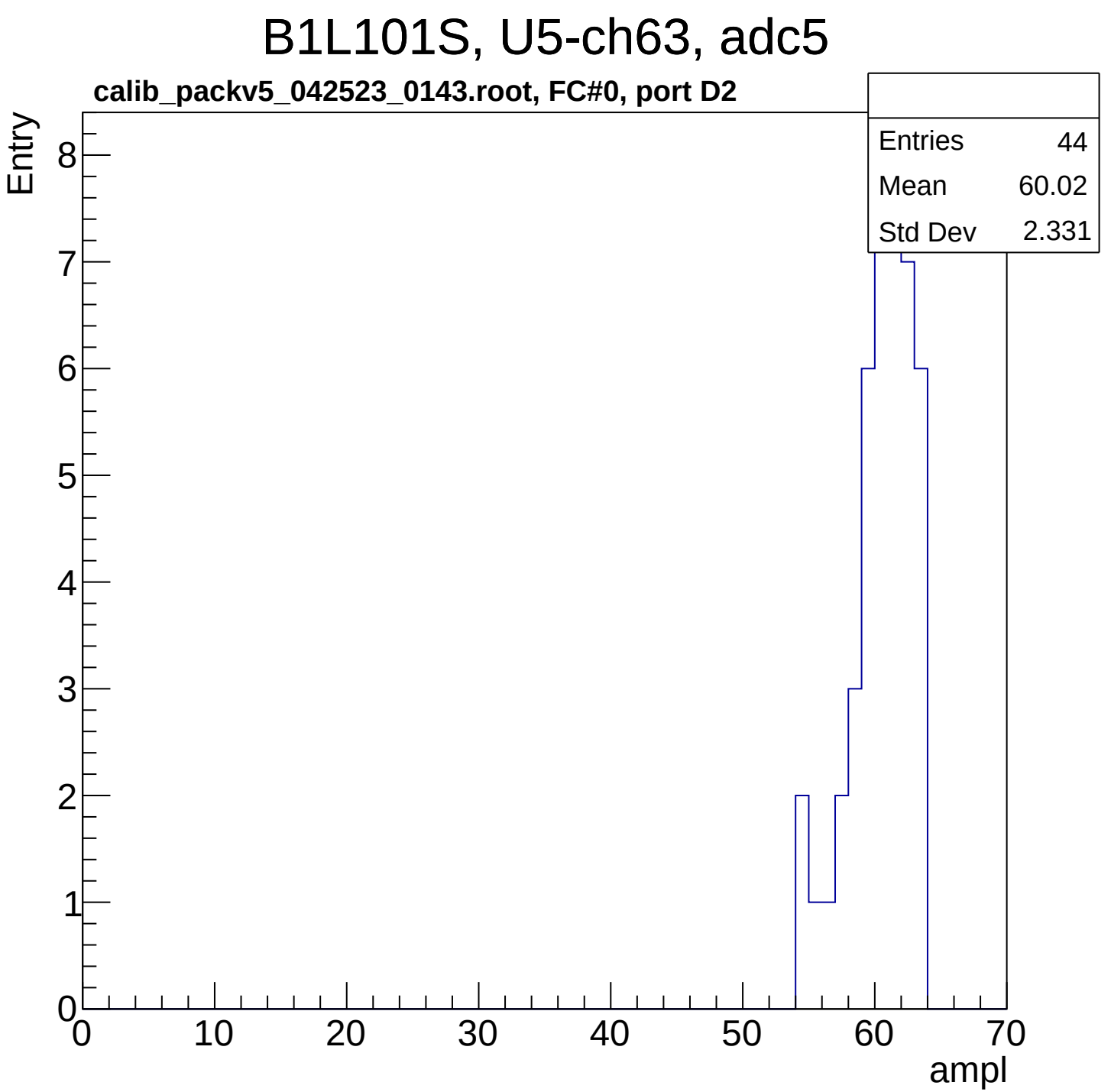
B1L101S, U5-ch63, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 44
Mean 60.02
Std Dev 2.331
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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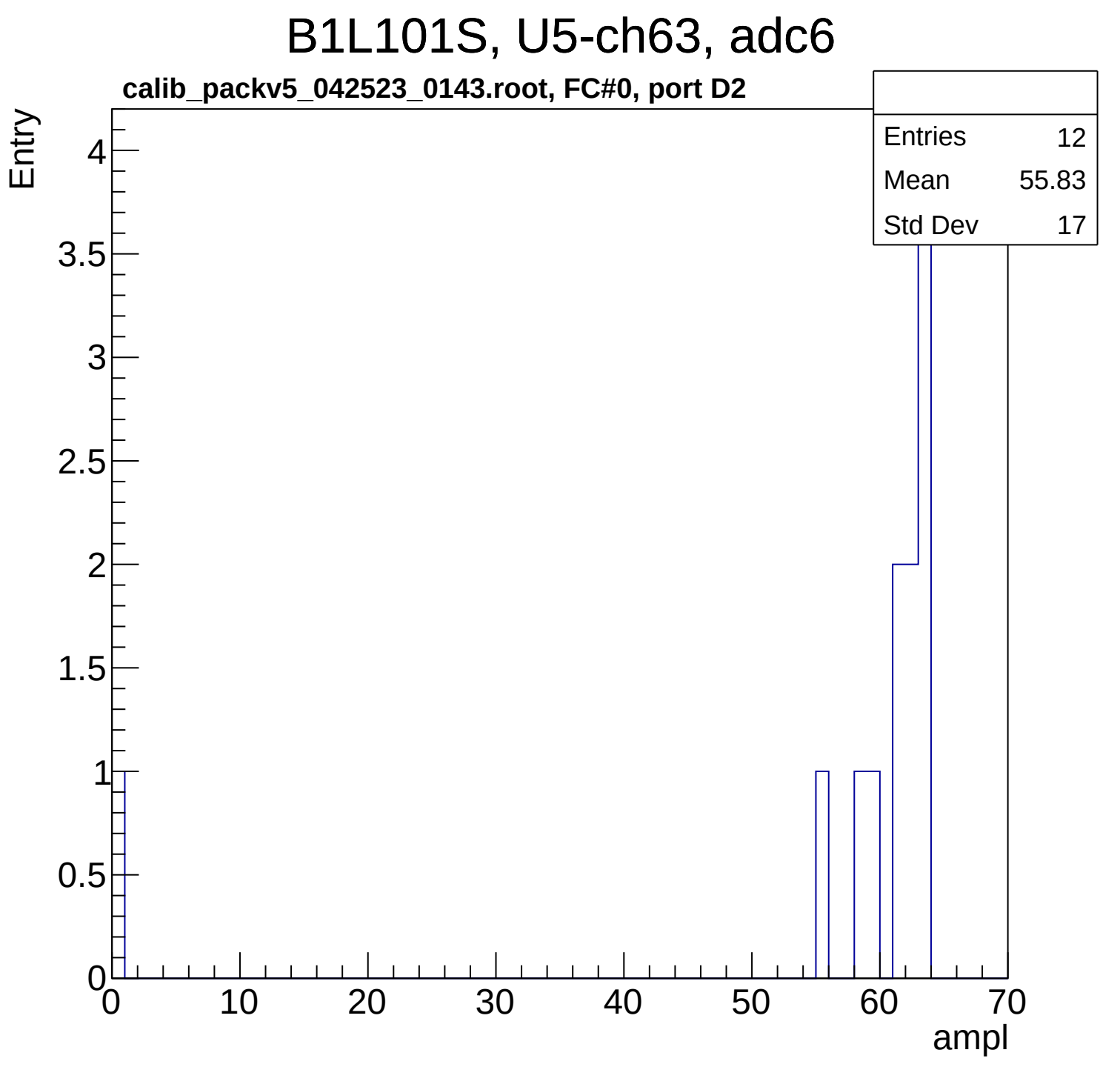
40
50
60
70


B1L101S, U5-ch63, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 12
Mean 55.83
Std Dev 17
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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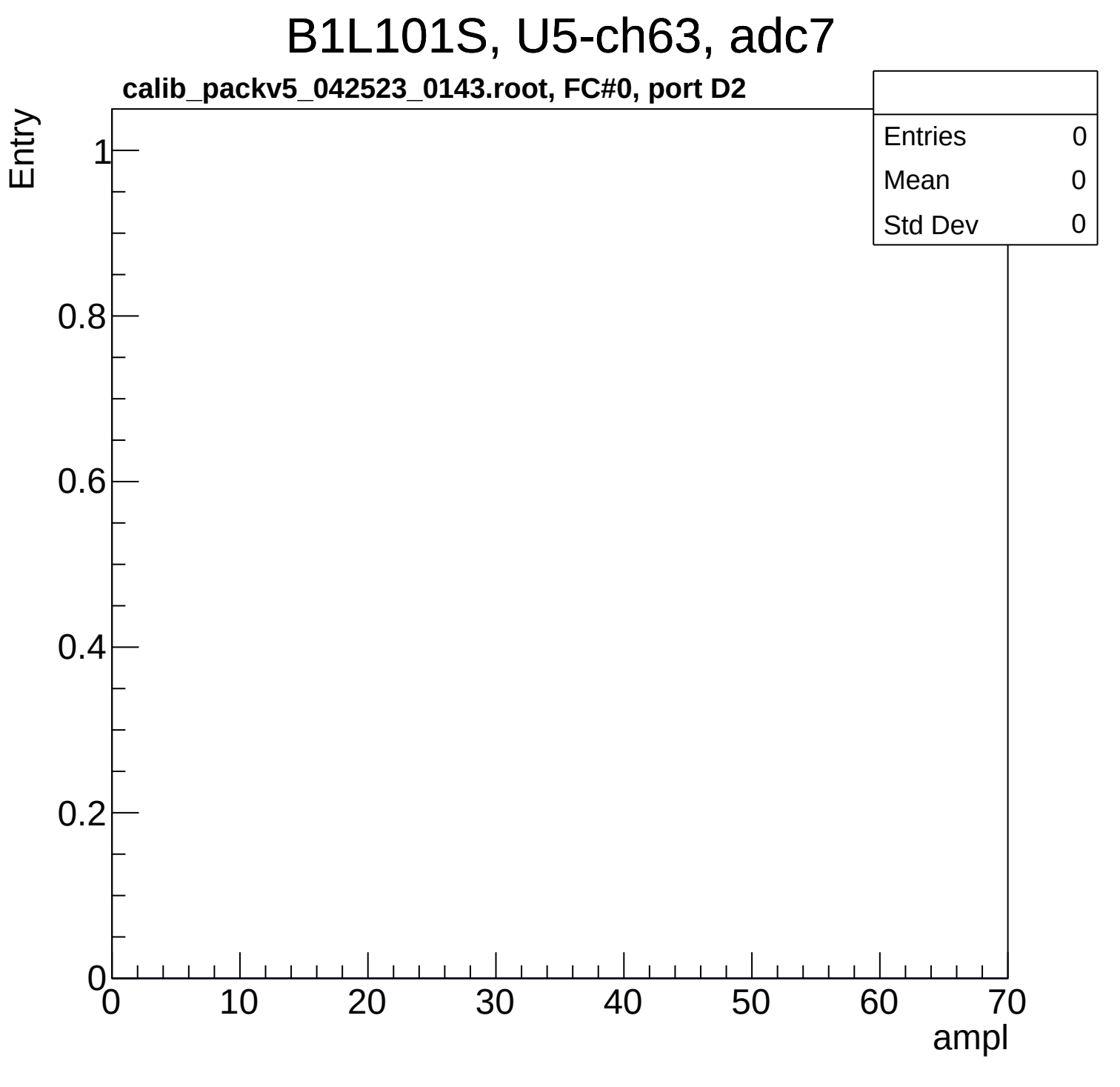
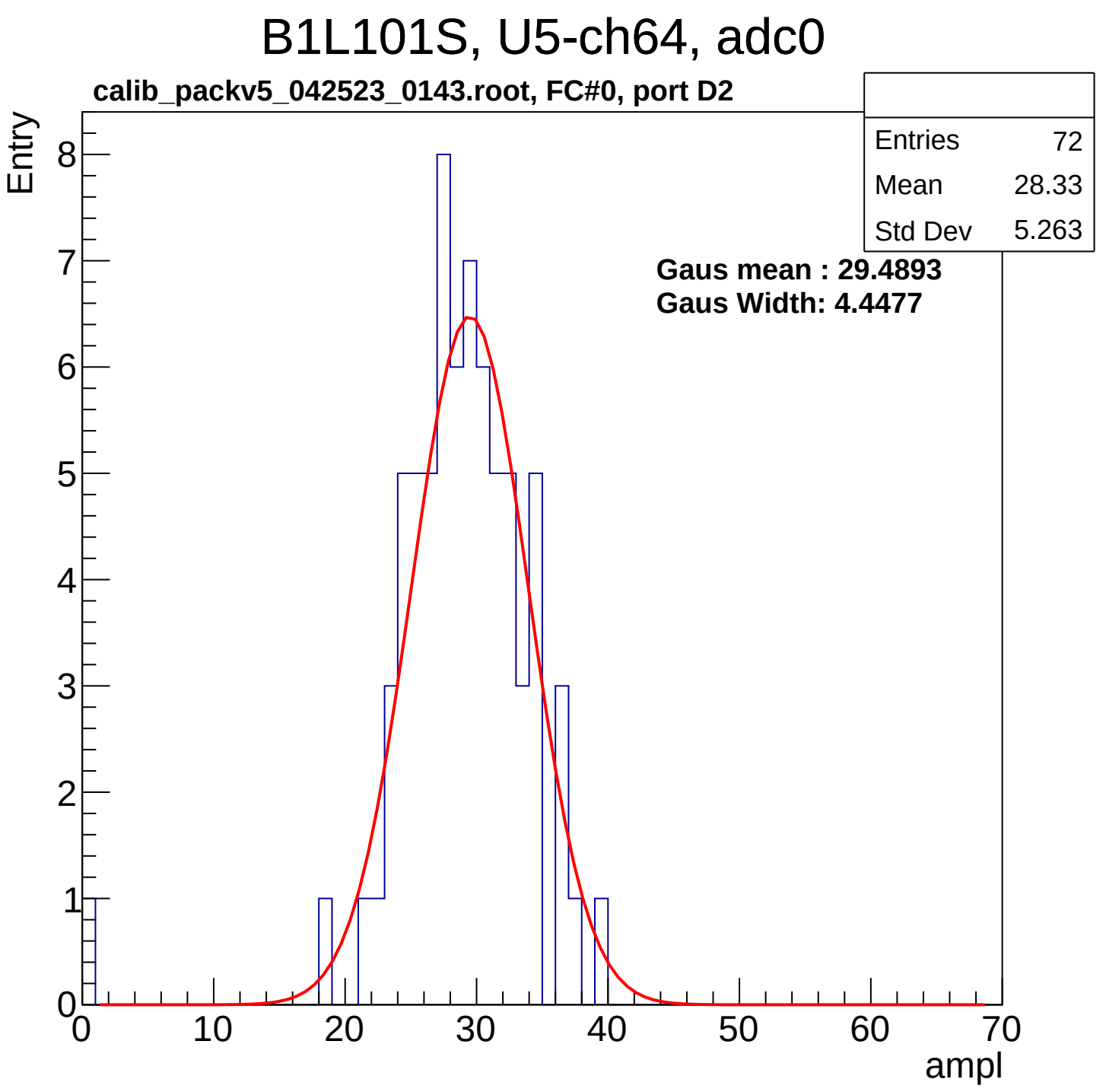

B1L101S, U5-ch63, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch64, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 28.33
Std Dev 5.263
Gaus mean : 29.4893
Gaus Width: 4.4477
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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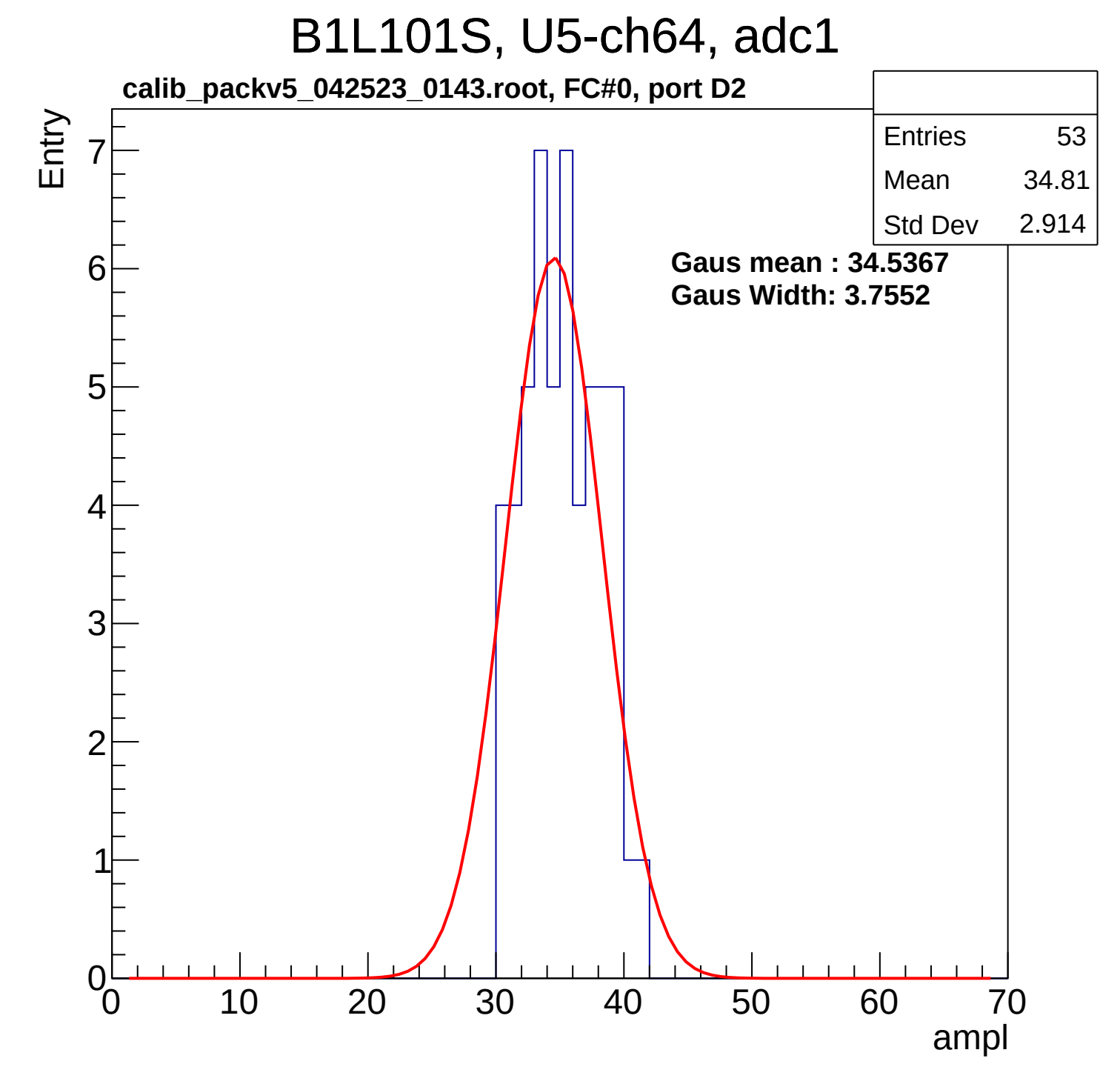
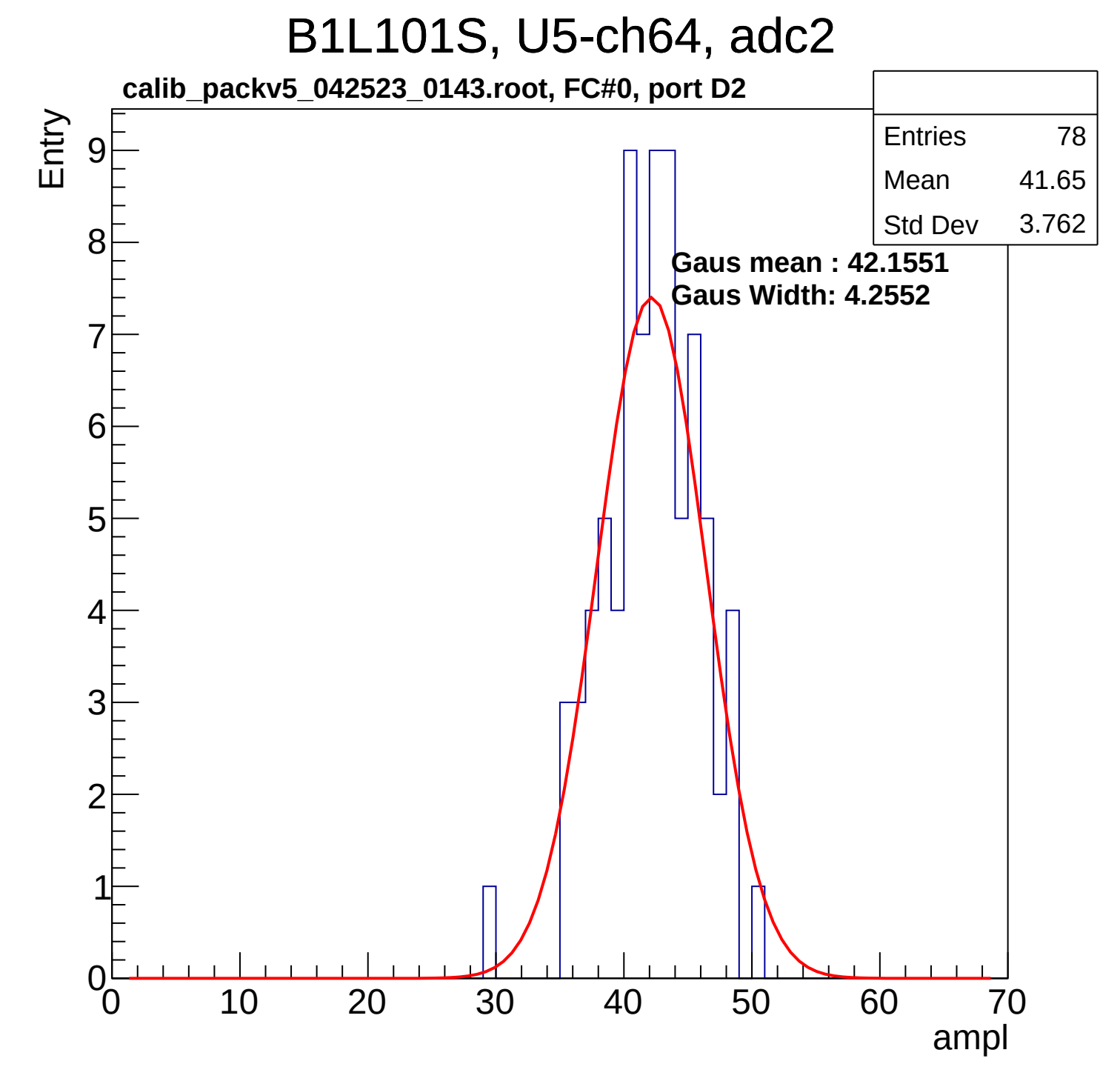

B1L101S, U5-ch64, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 34.81
Std Dev 2.914
Gaus mean : 34.5367
Gaus Width: 3.7552
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch64, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 41.65
Std Dev 3.762
Gaus mean : 42.1551
Gaus Width: 4.2552
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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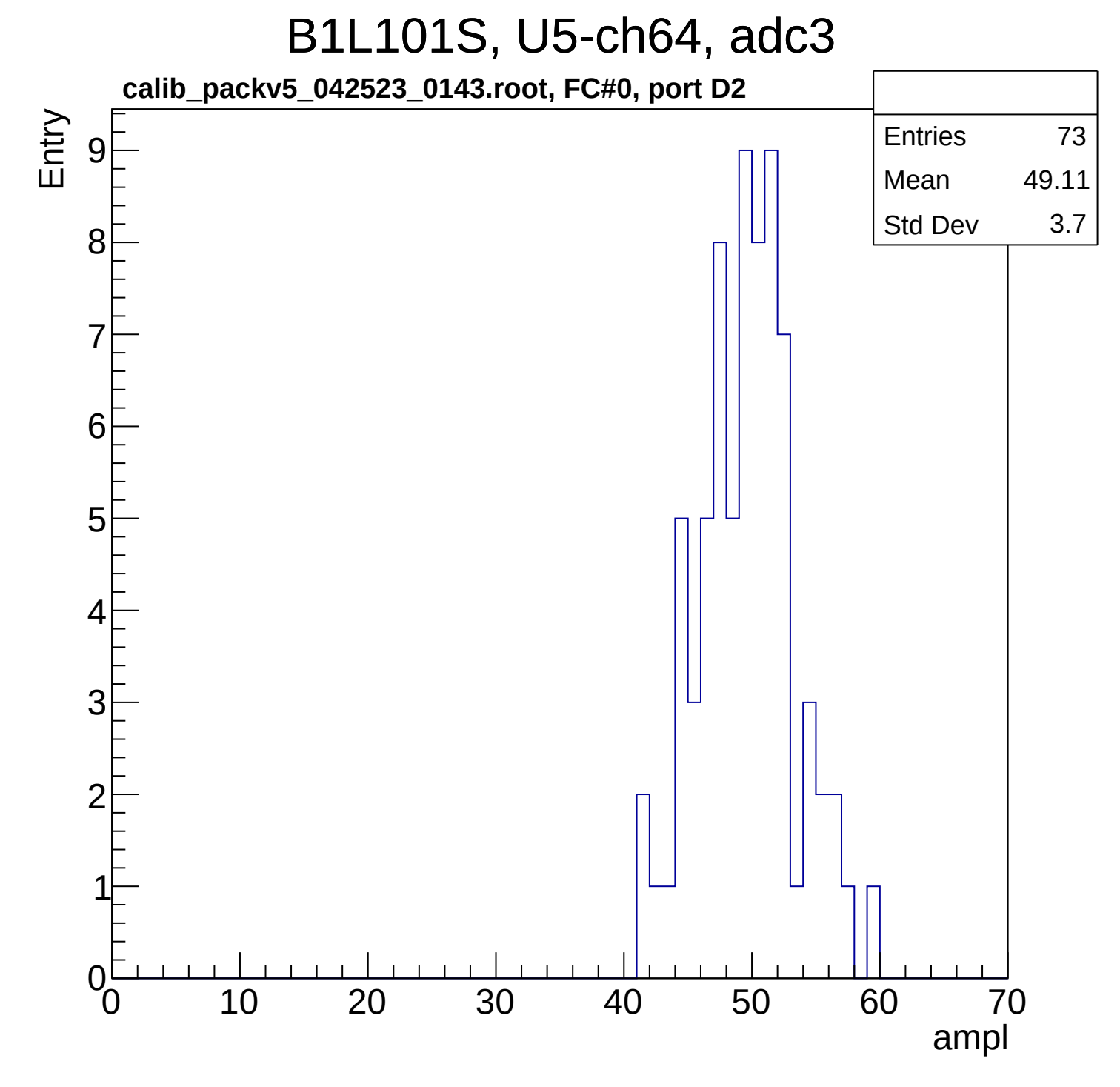
20
30
40
50
60
70


B1L101S, U5-ch64, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 49.11
Std Dev 3.7
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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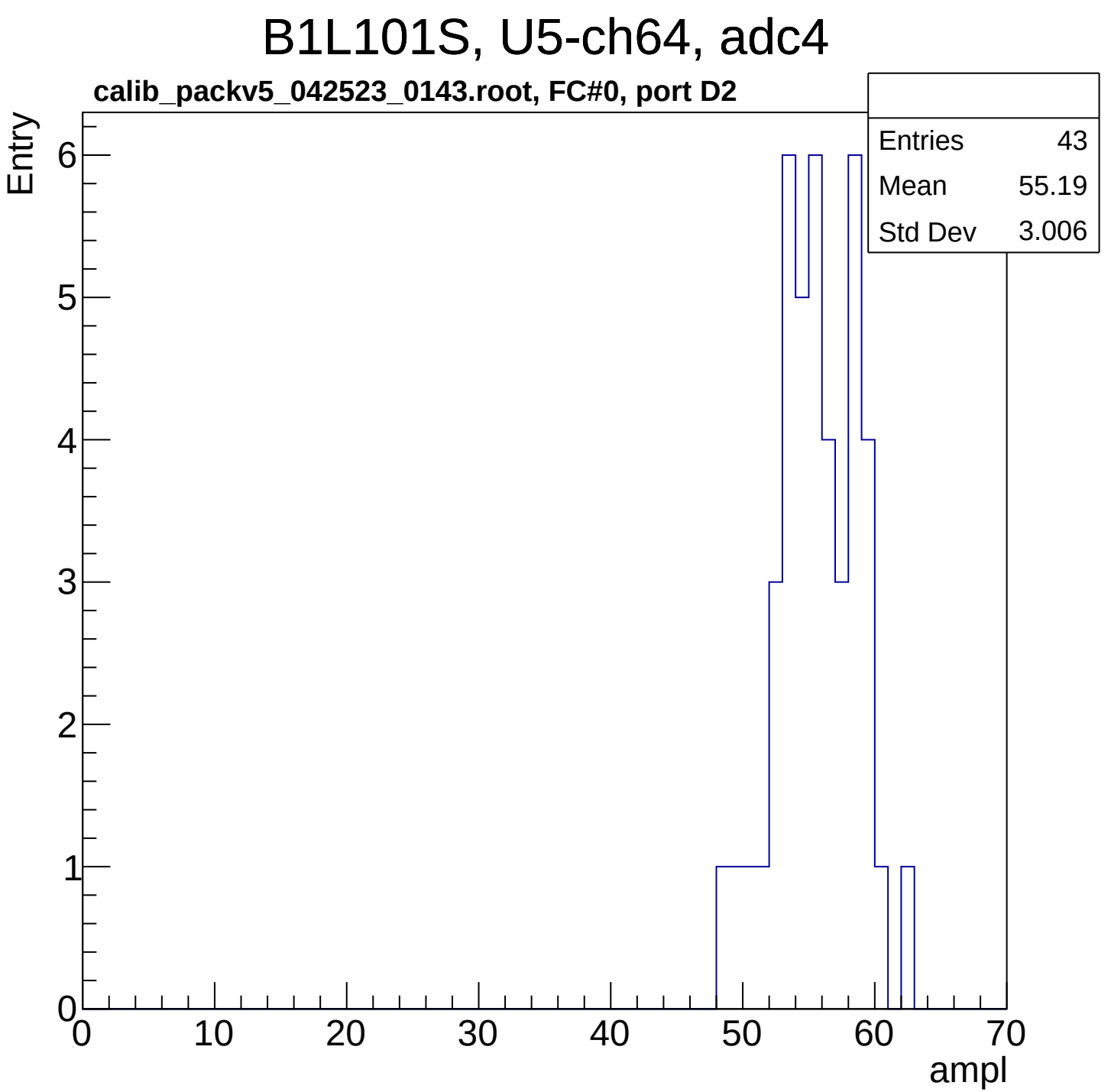
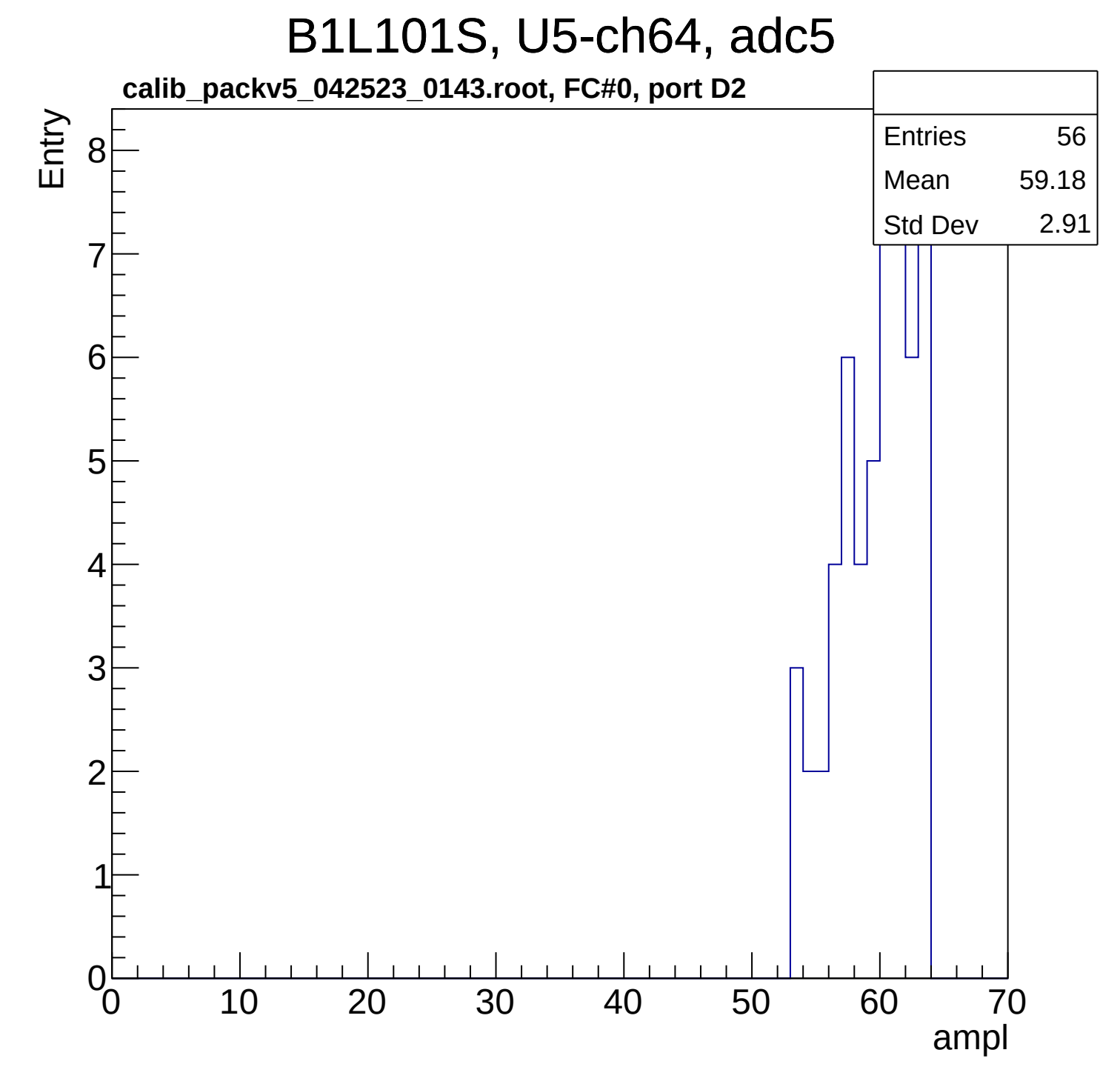

B1L101S, U5-ch64, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 43
Mean 55.19
Std Dev 3.006
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch64, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 59.18
Std Dev 2.91
Entry
ampl
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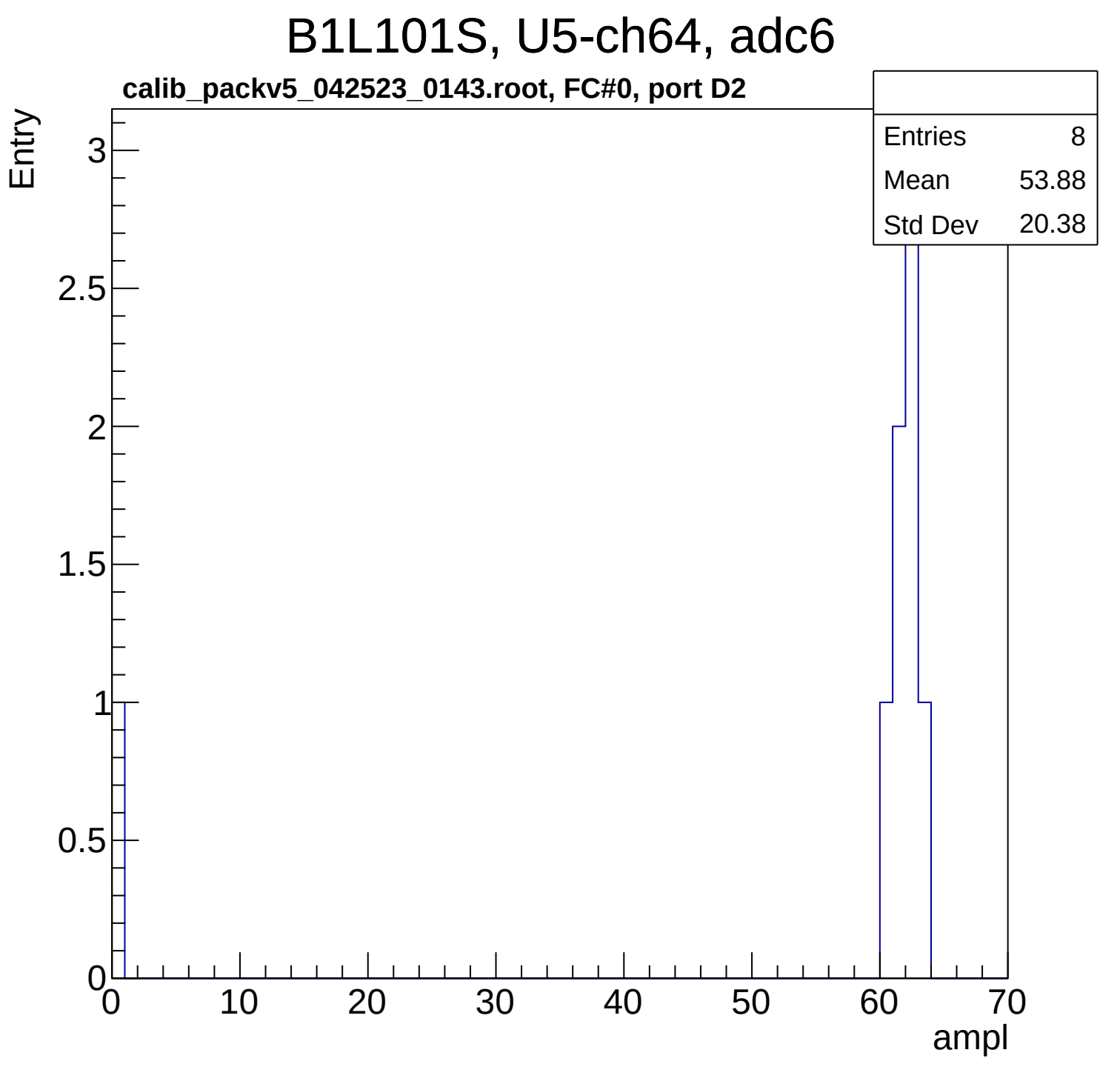
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch64, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 53.88
Std Dev 20.38
Entry
ampl
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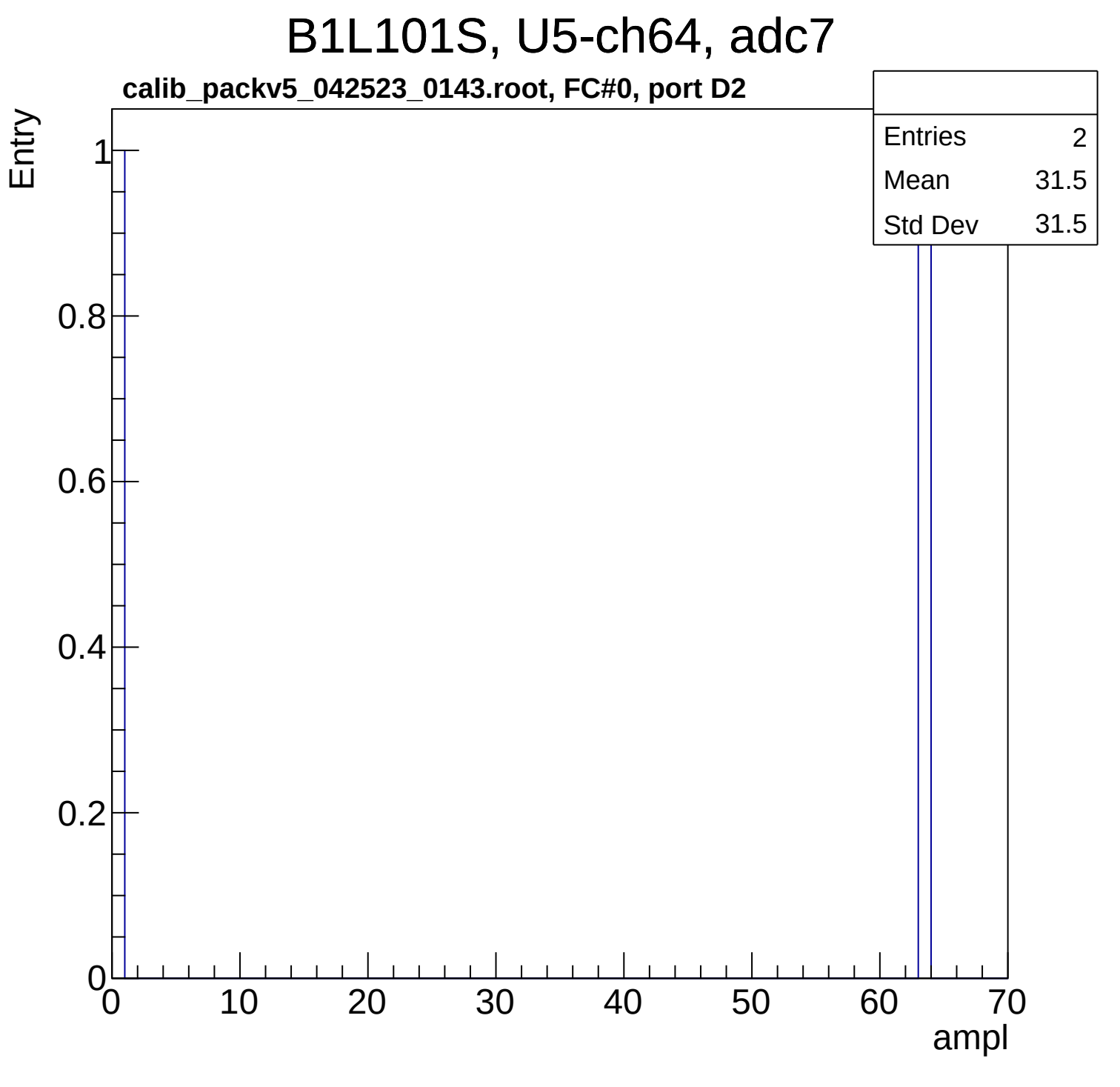
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U5-ch64, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
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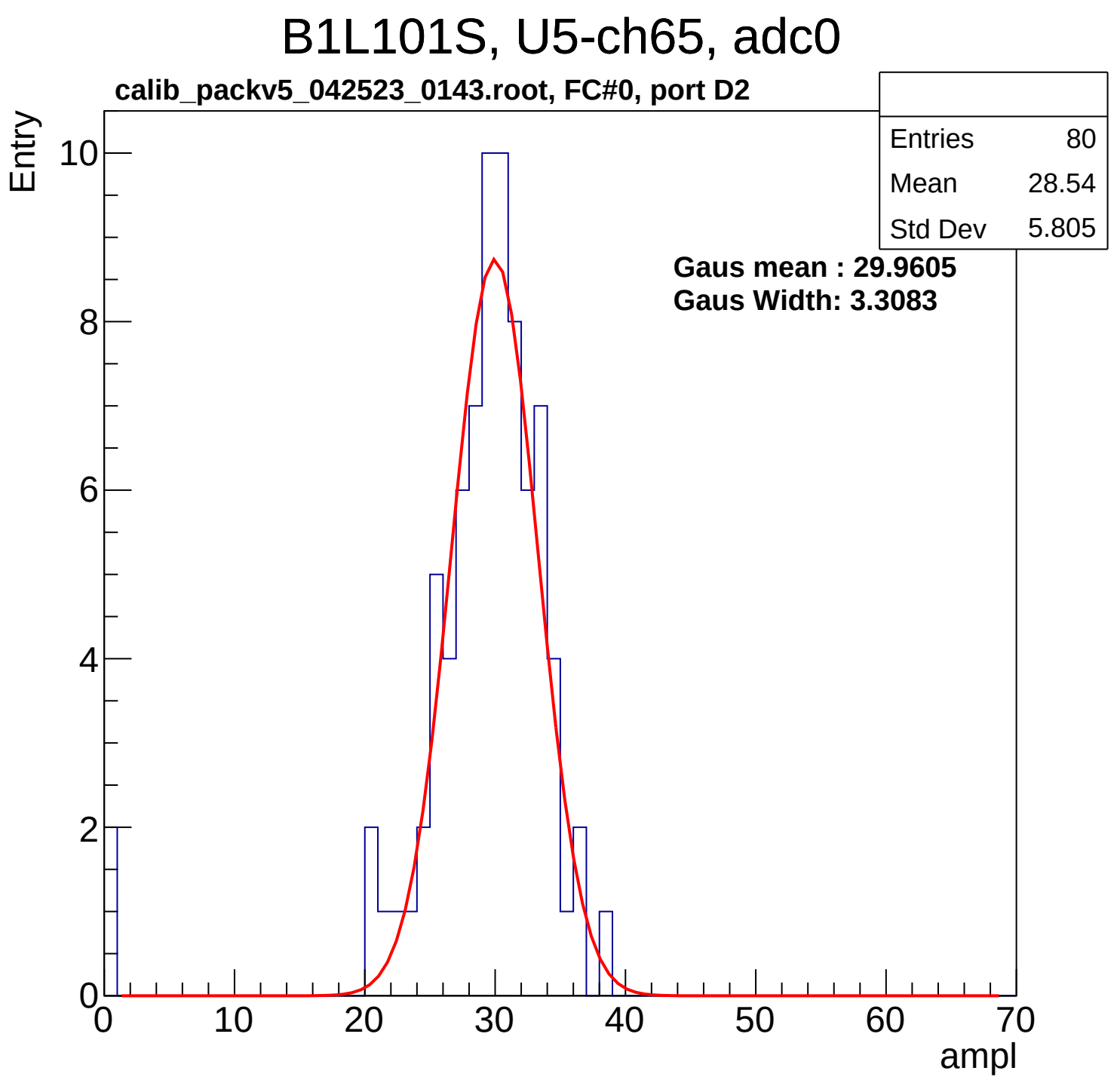
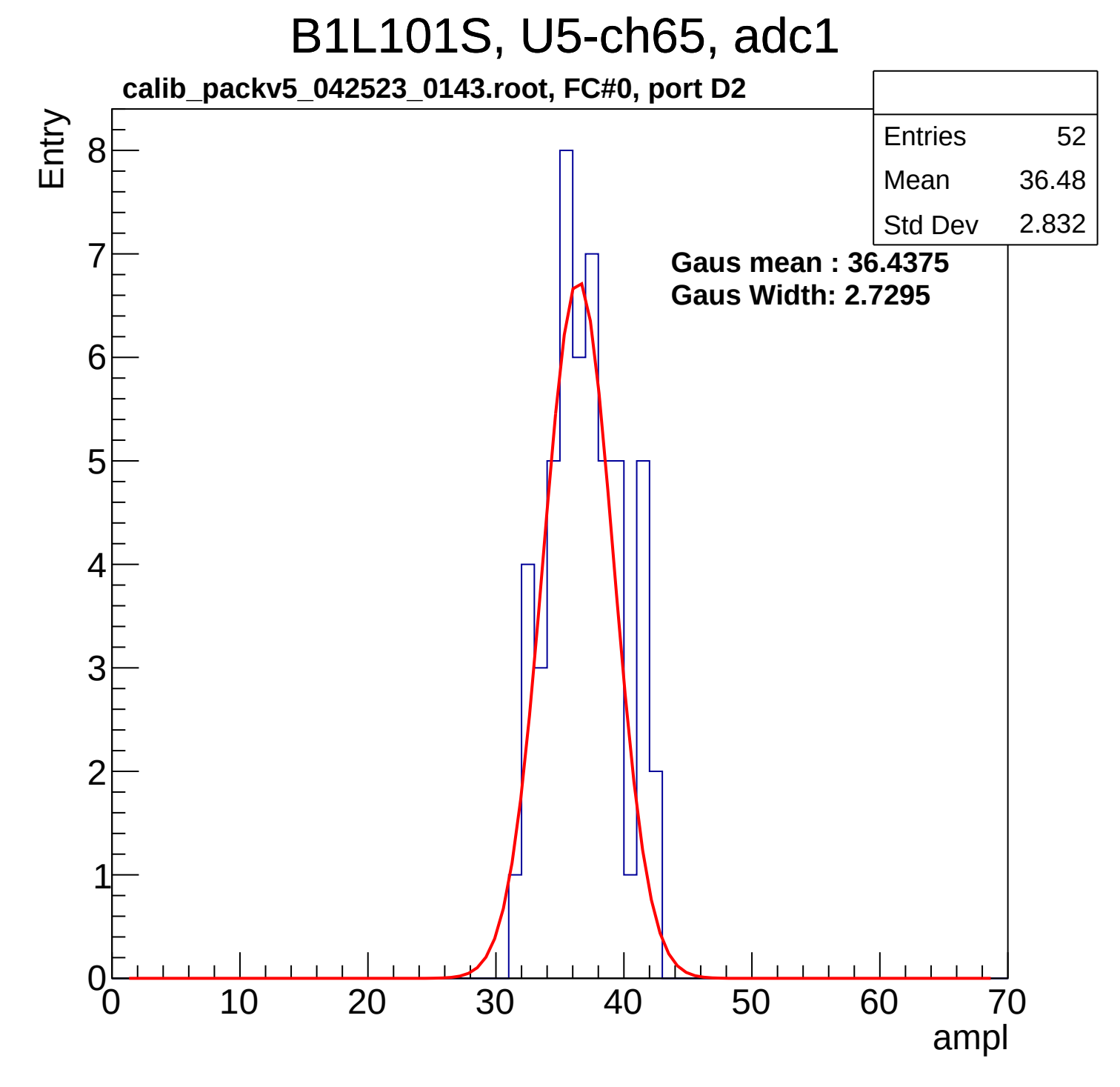
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch65, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 80
Mean 28.54
Std Dev 5.805
Gaus mean : 29.9605
Gaus Width: 3.3083
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch65, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 36.48
Std Dev 2.832
Gaus mean : 36.4375
Gaus Width: 2.7295
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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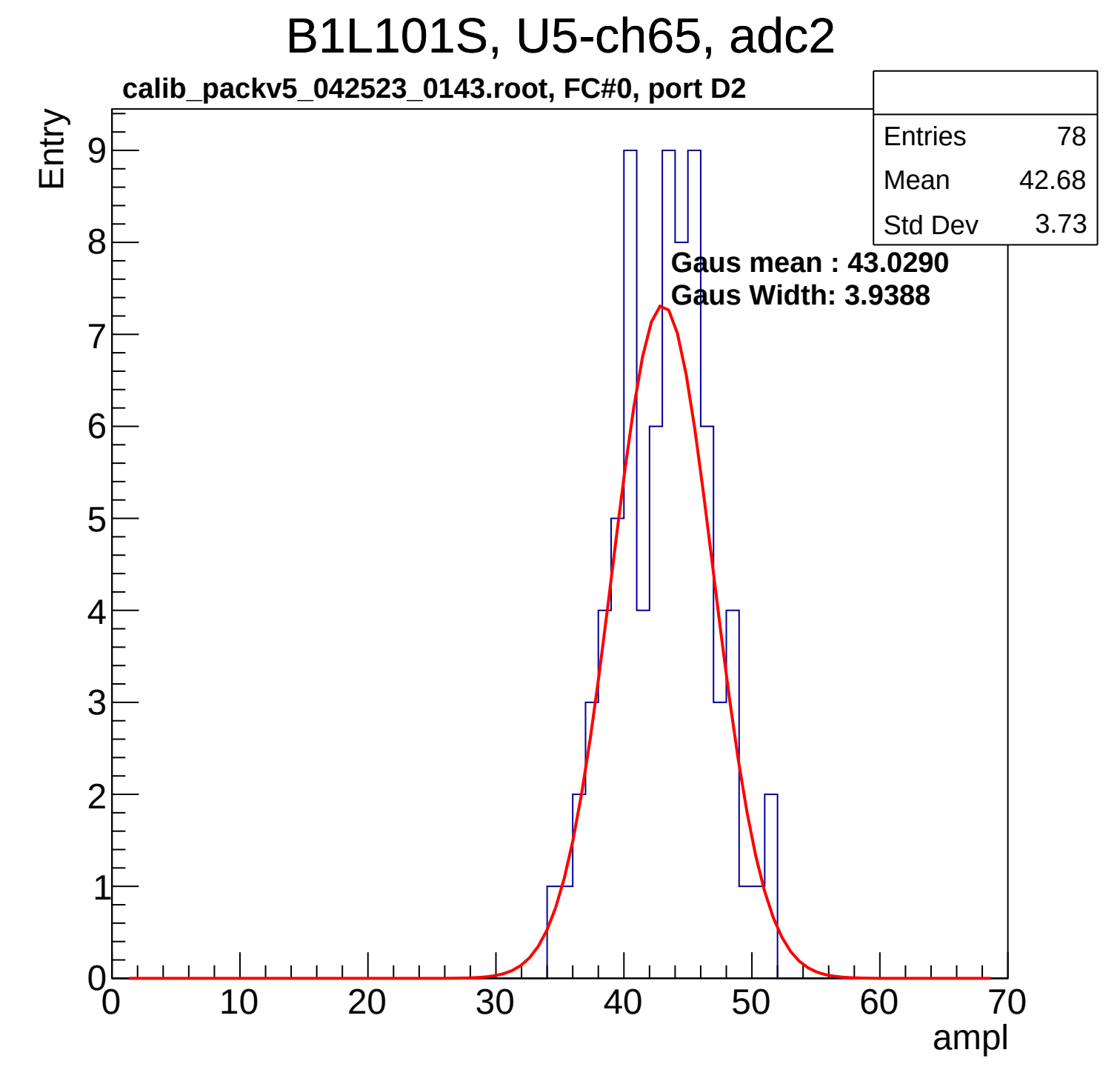
B1L101S, U5-ch65, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 42.68
Std Dev 3.73
Gaus mean : 43.0290
Gaus Width: 3.9388
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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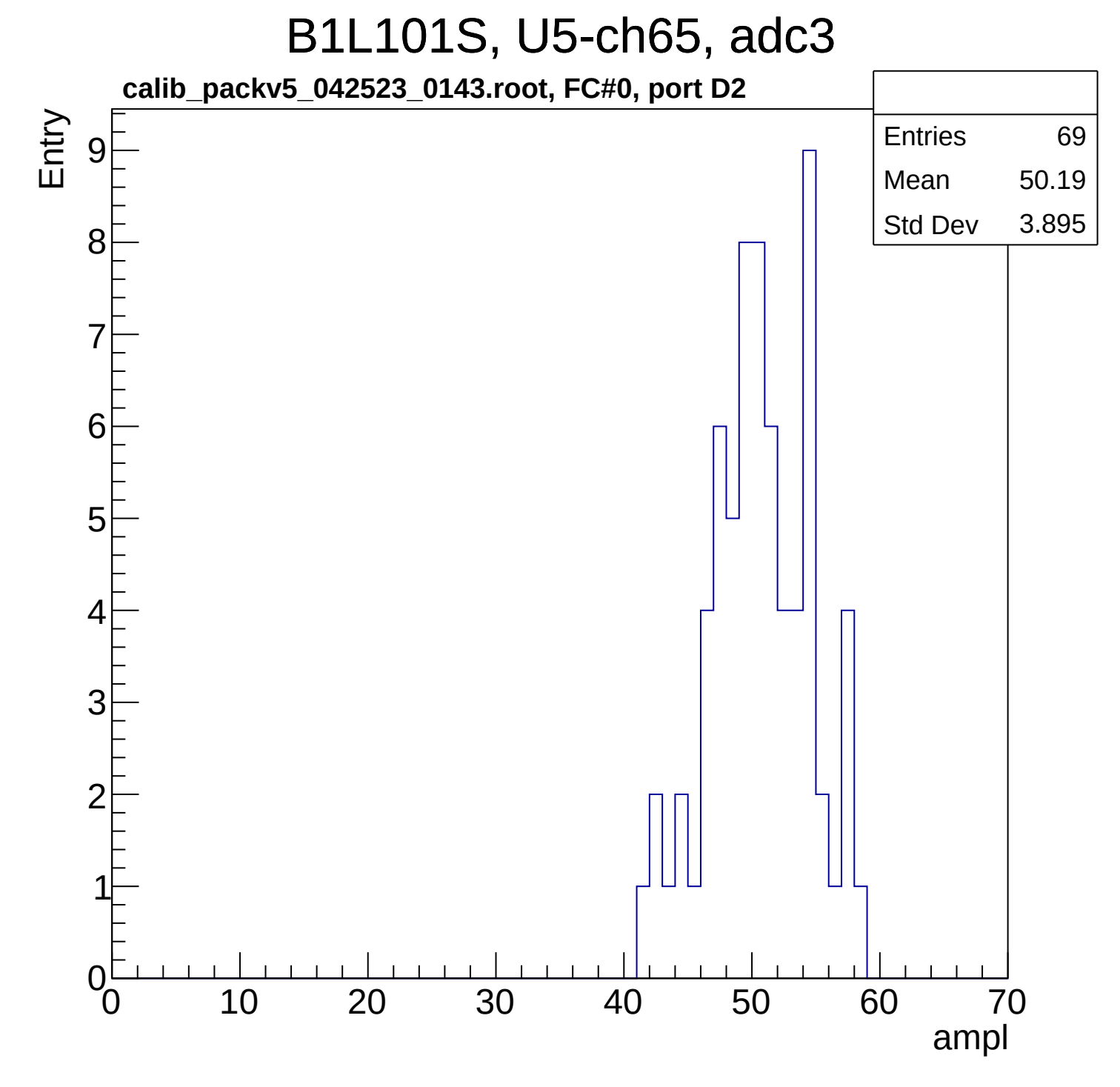
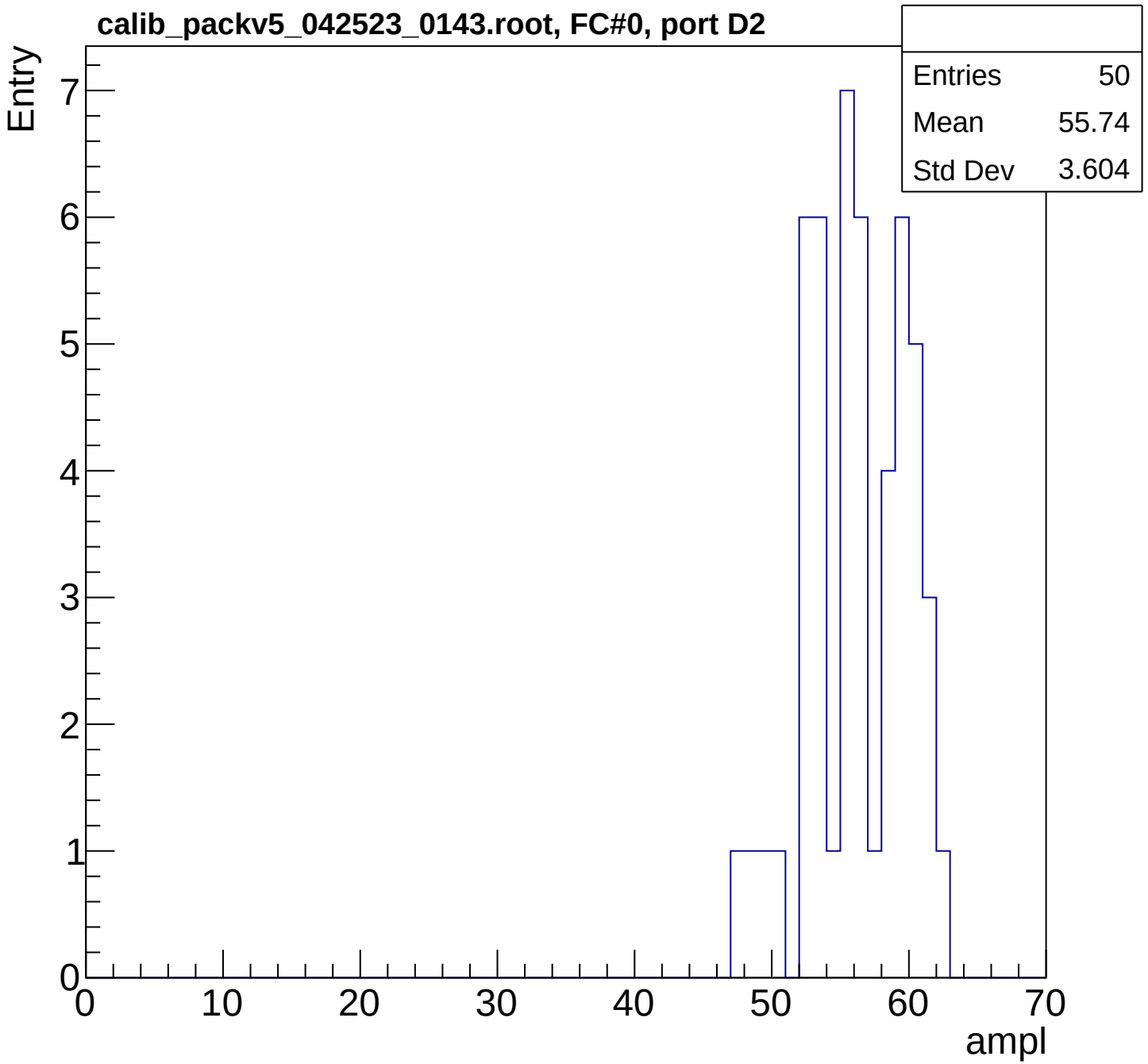

B1L101S, U5-ch65, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 50.19
Std Dev 3.895
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch65, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 55.74
Std Dev 3.604
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
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60
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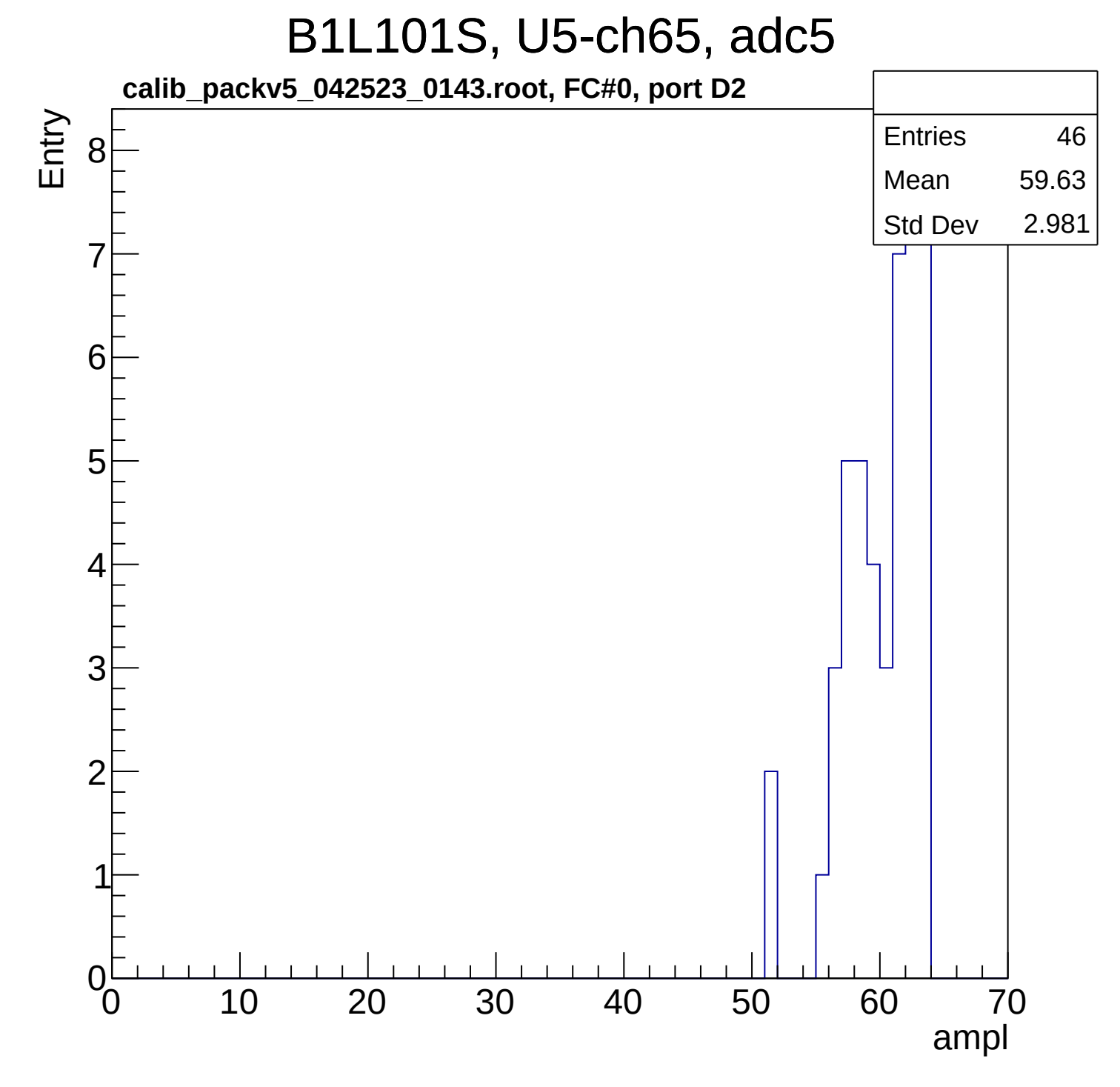
B1L101S, U5-ch65, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 59.63
Std Dev 2.981
Entry
ampl
0
1
2
3
4
5
6
7
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0
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40
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60
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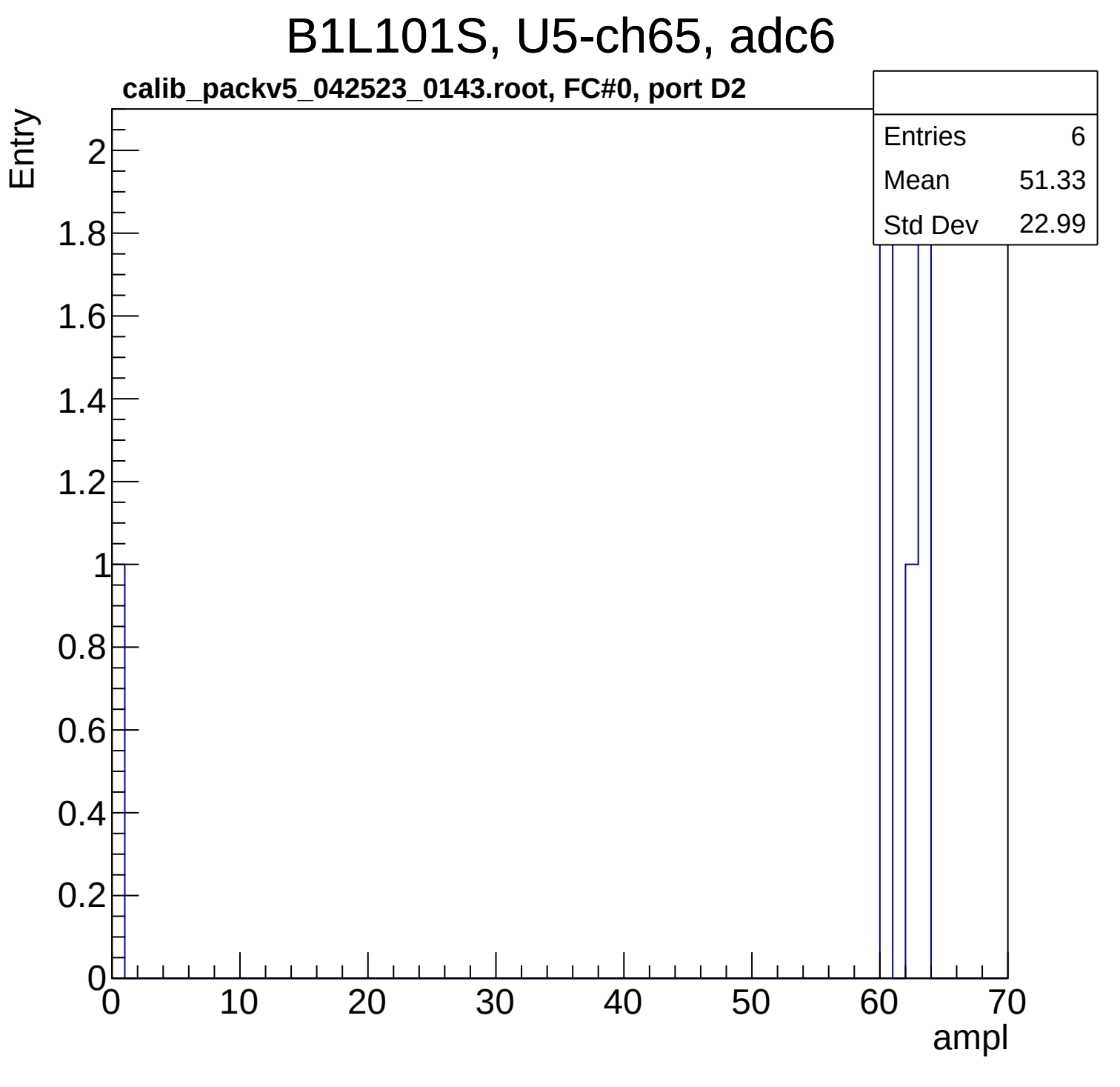
B1L101S, U5-ch65, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 51.33
Std Dev 22.99
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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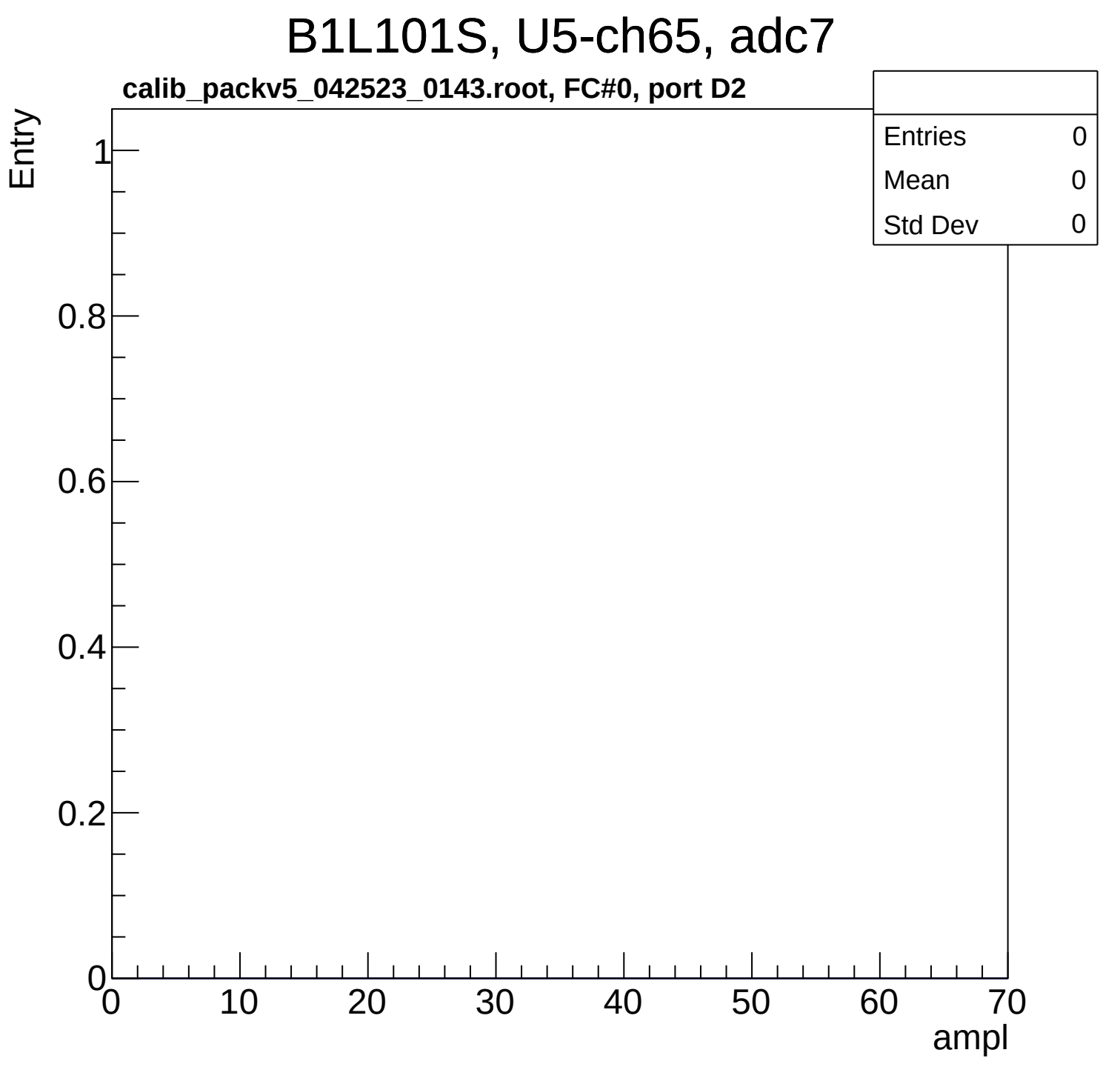
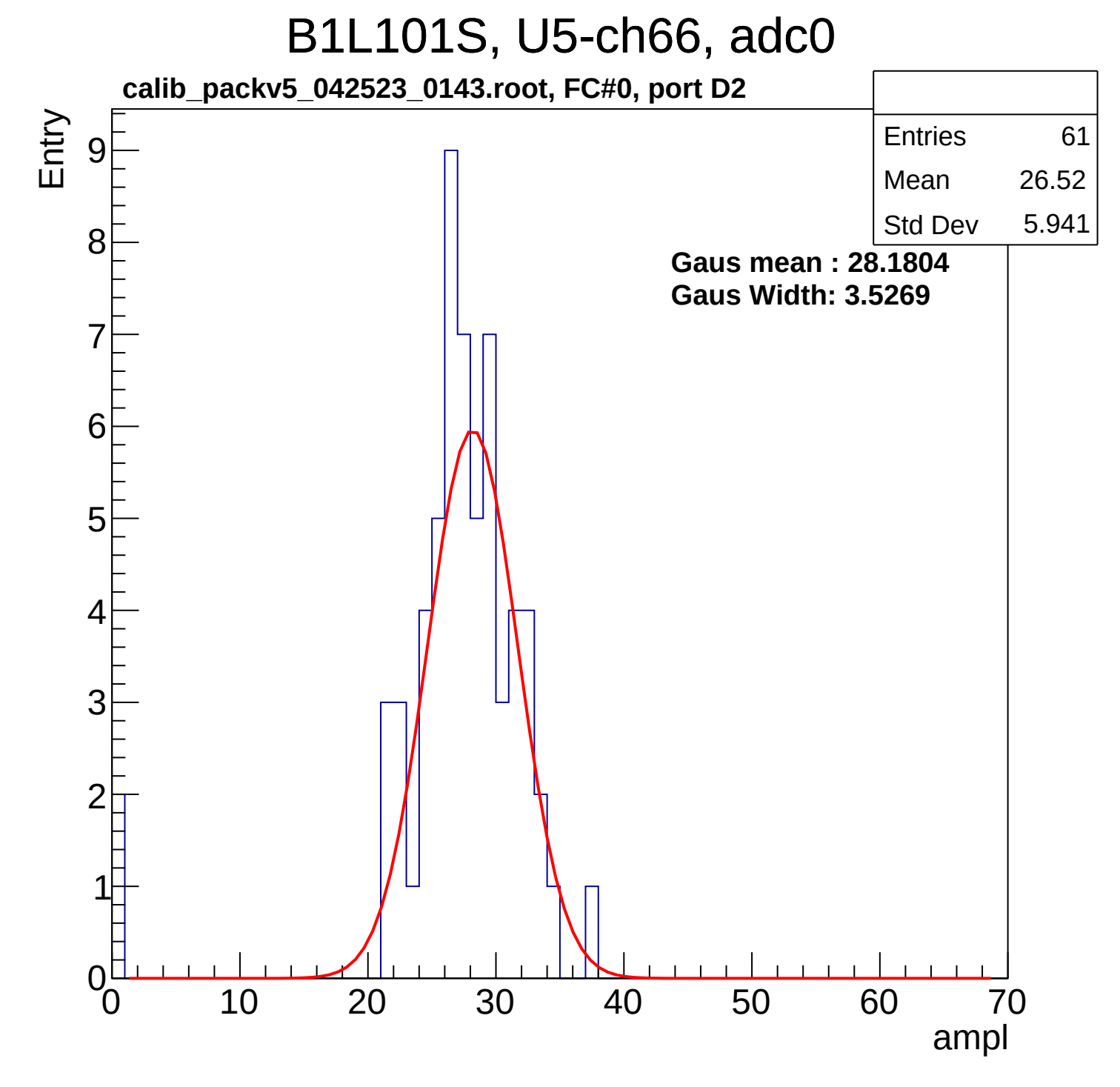

B1L101S, U5-ch65, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch66, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 26.52
Std Dev 5.941
Gaus mean : 28.1804
Gaus Width: 3.5269
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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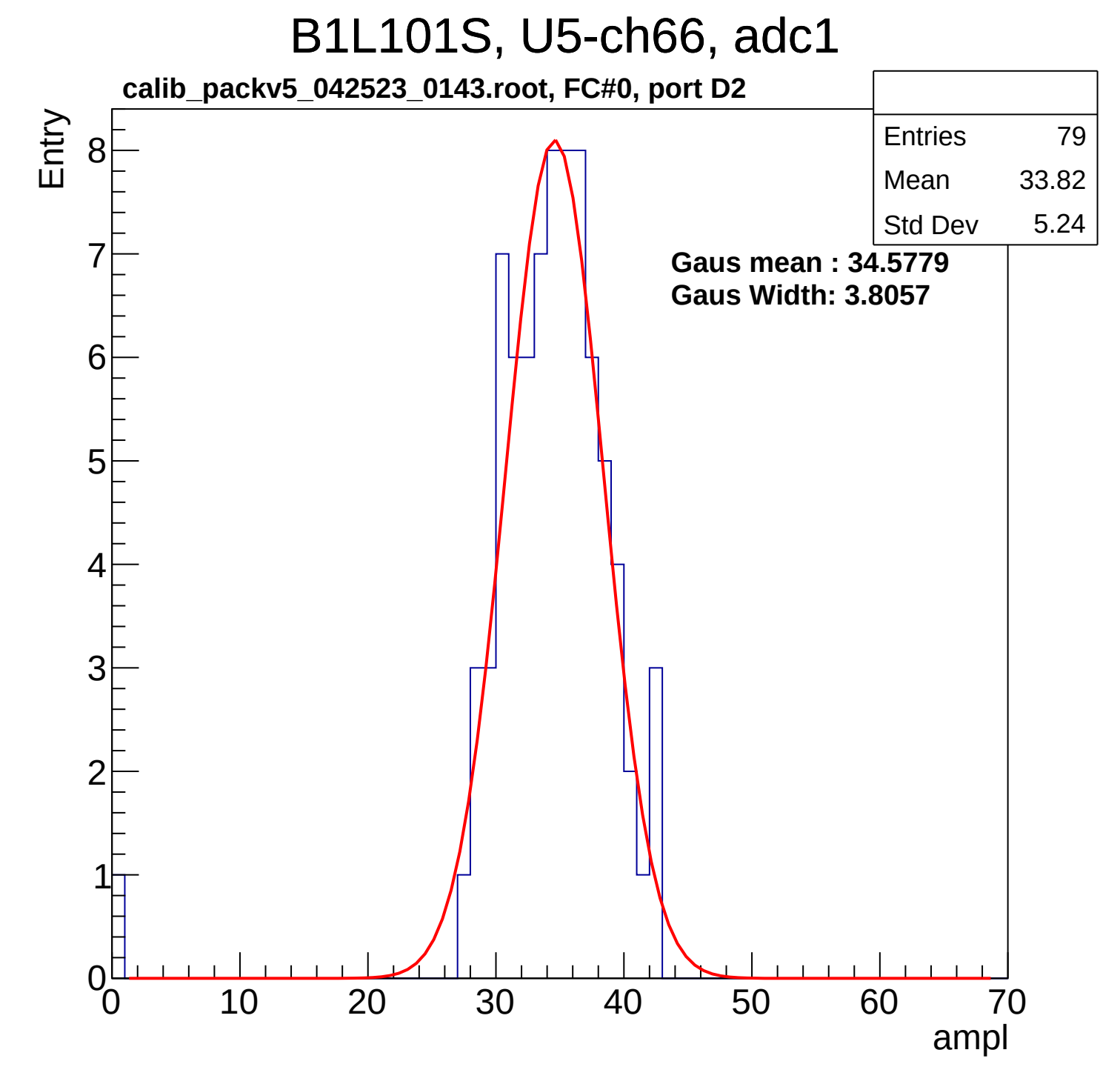
B1L101S, U5-ch66, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 33.82
Std Dev 5.24
Gaus mean : 34.5779
Gaus Width: 3.8057
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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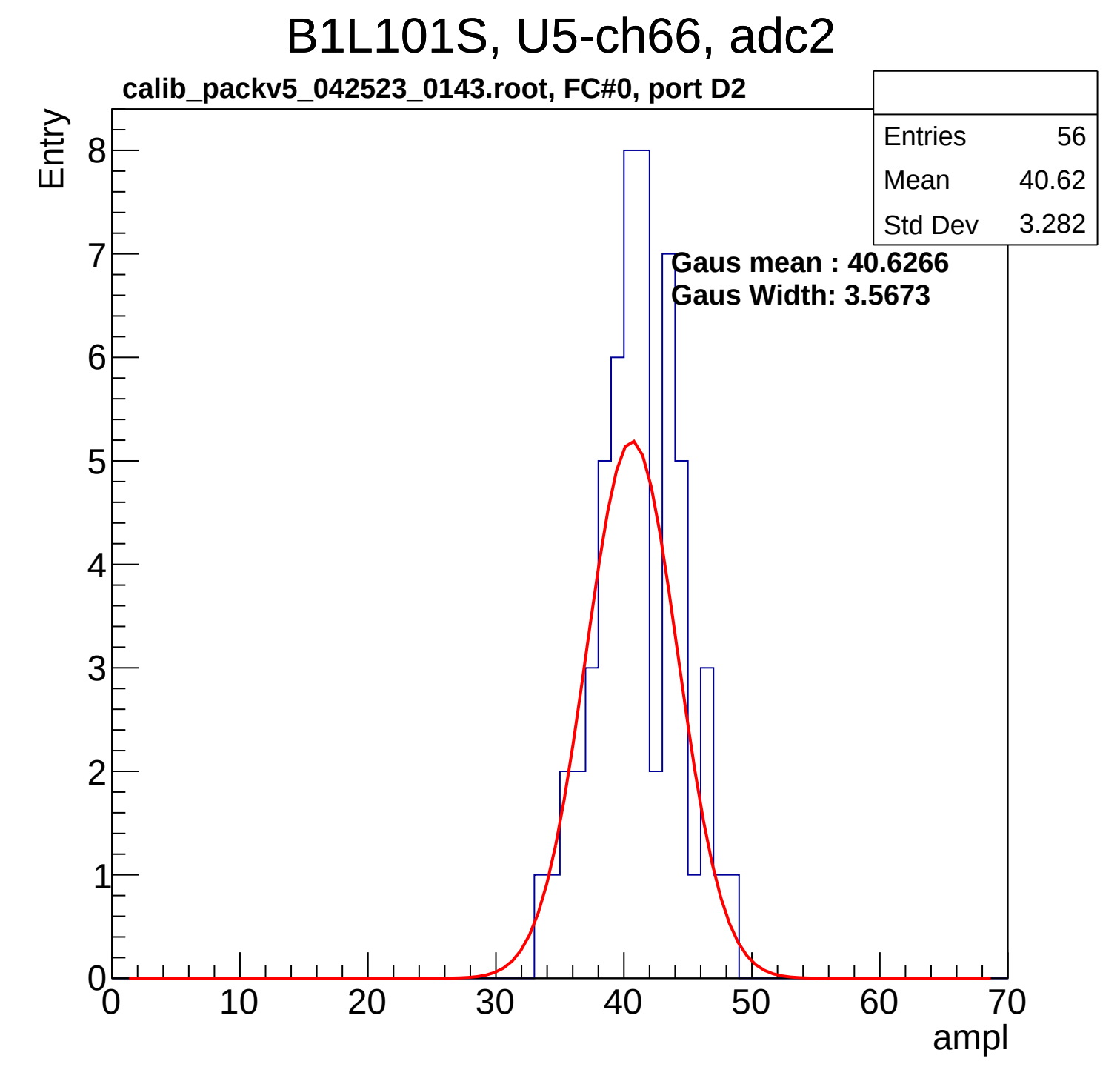
B1L101S, U5-ch66, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 40.62
Std Dev 3.282
Gaus mean : 40.6266
Gaus Width: 3.5673
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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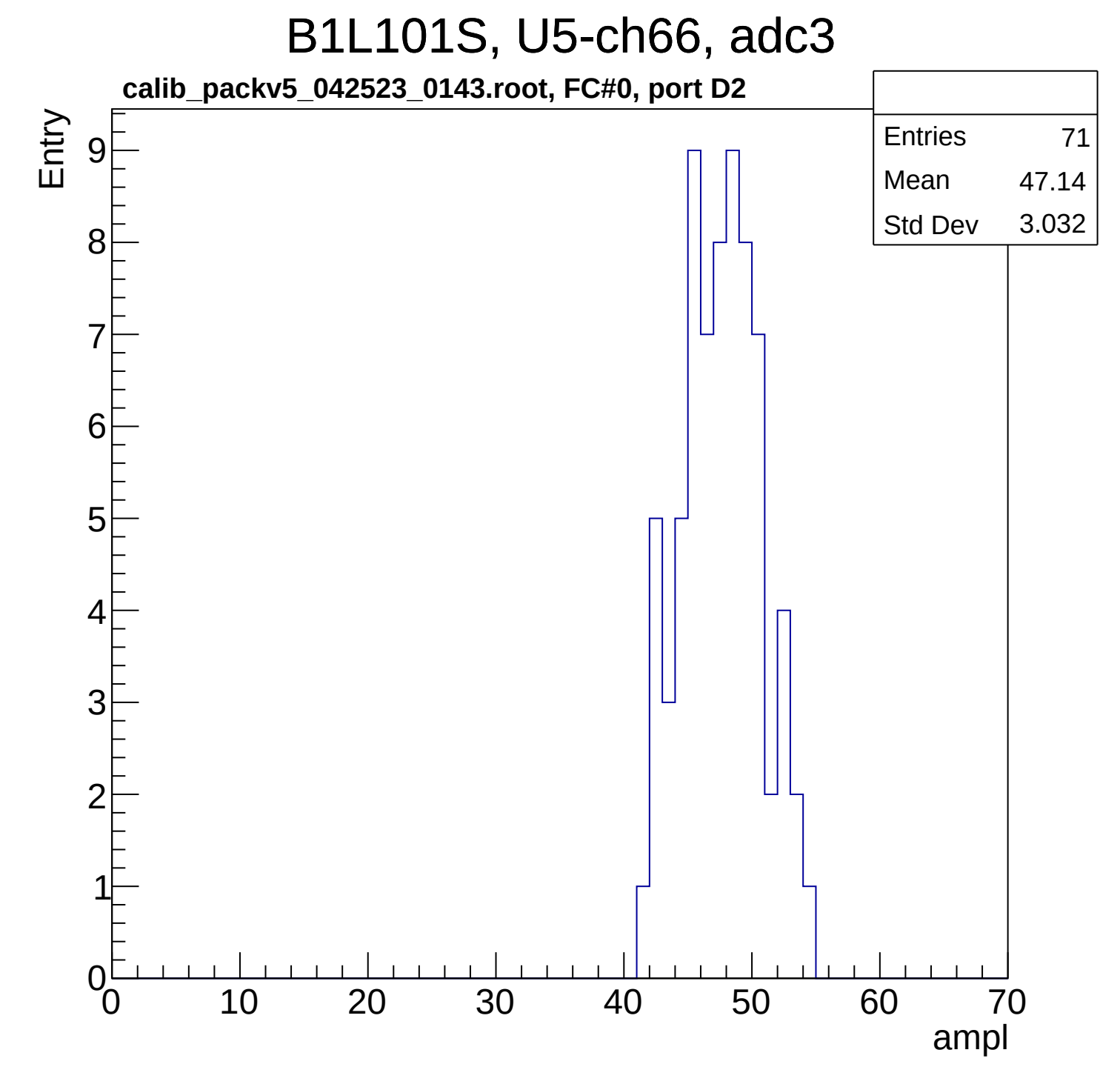
B1L101S, U5-ch66, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 47.14
Std Dev 3.032
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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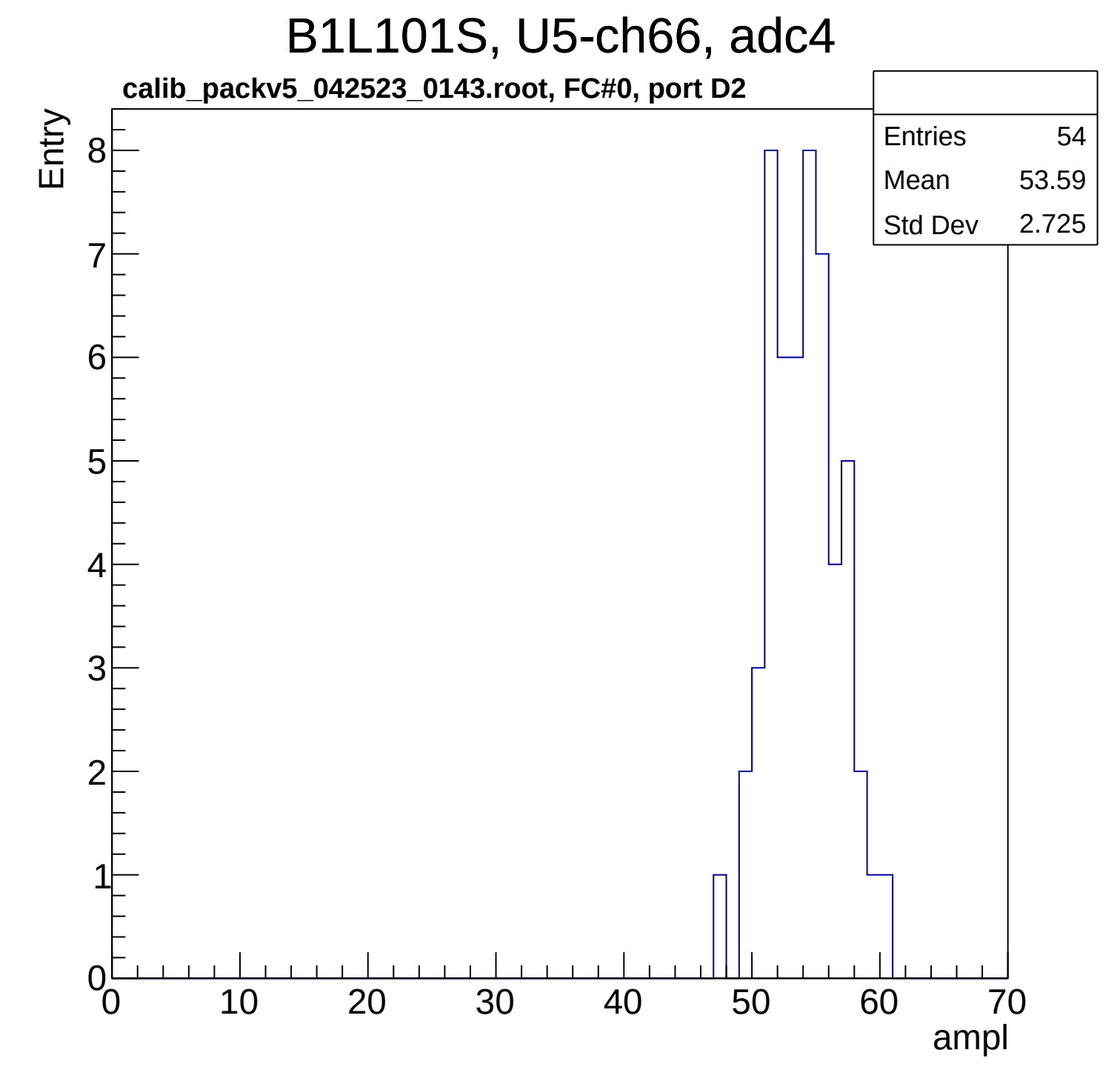
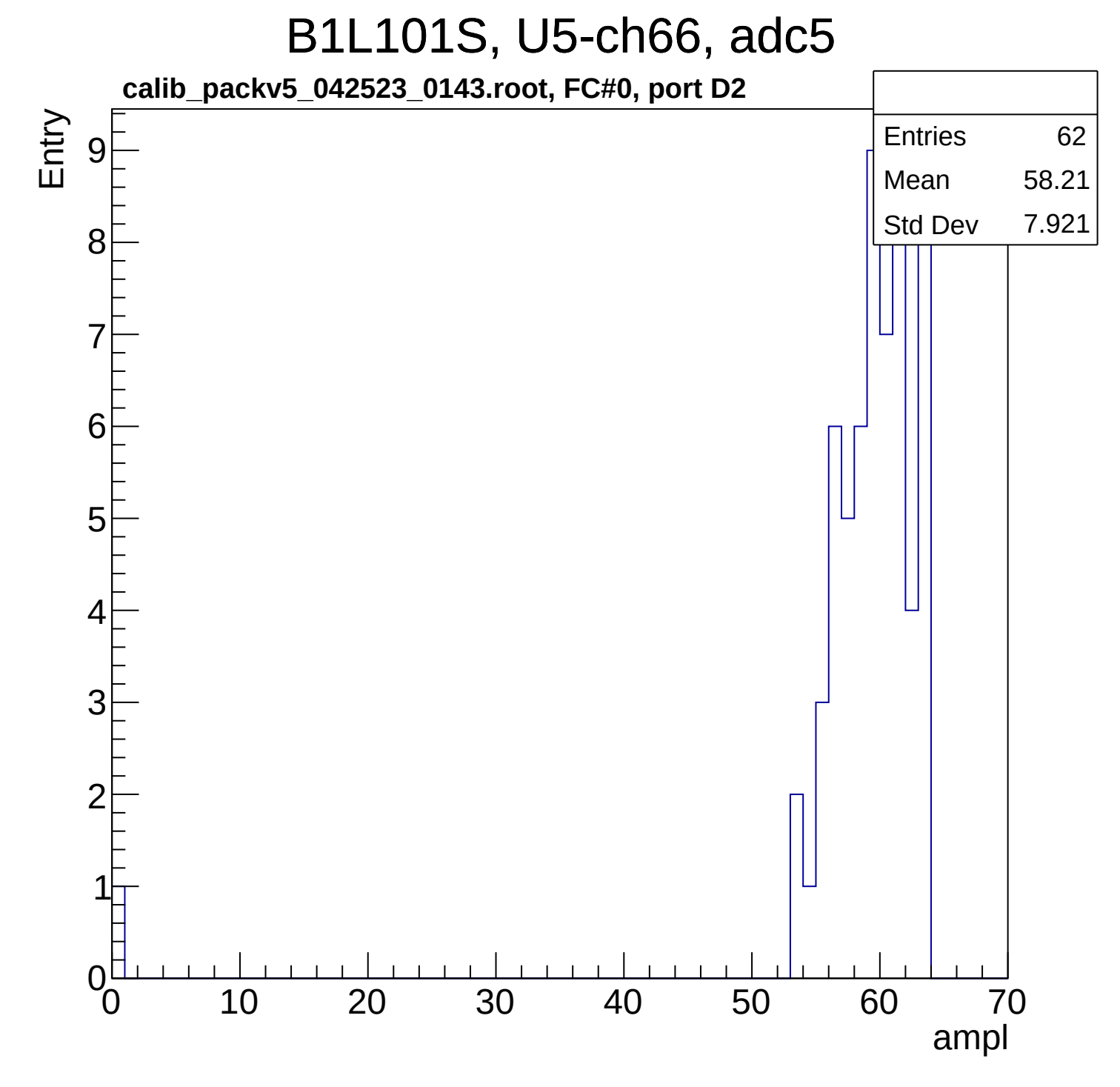
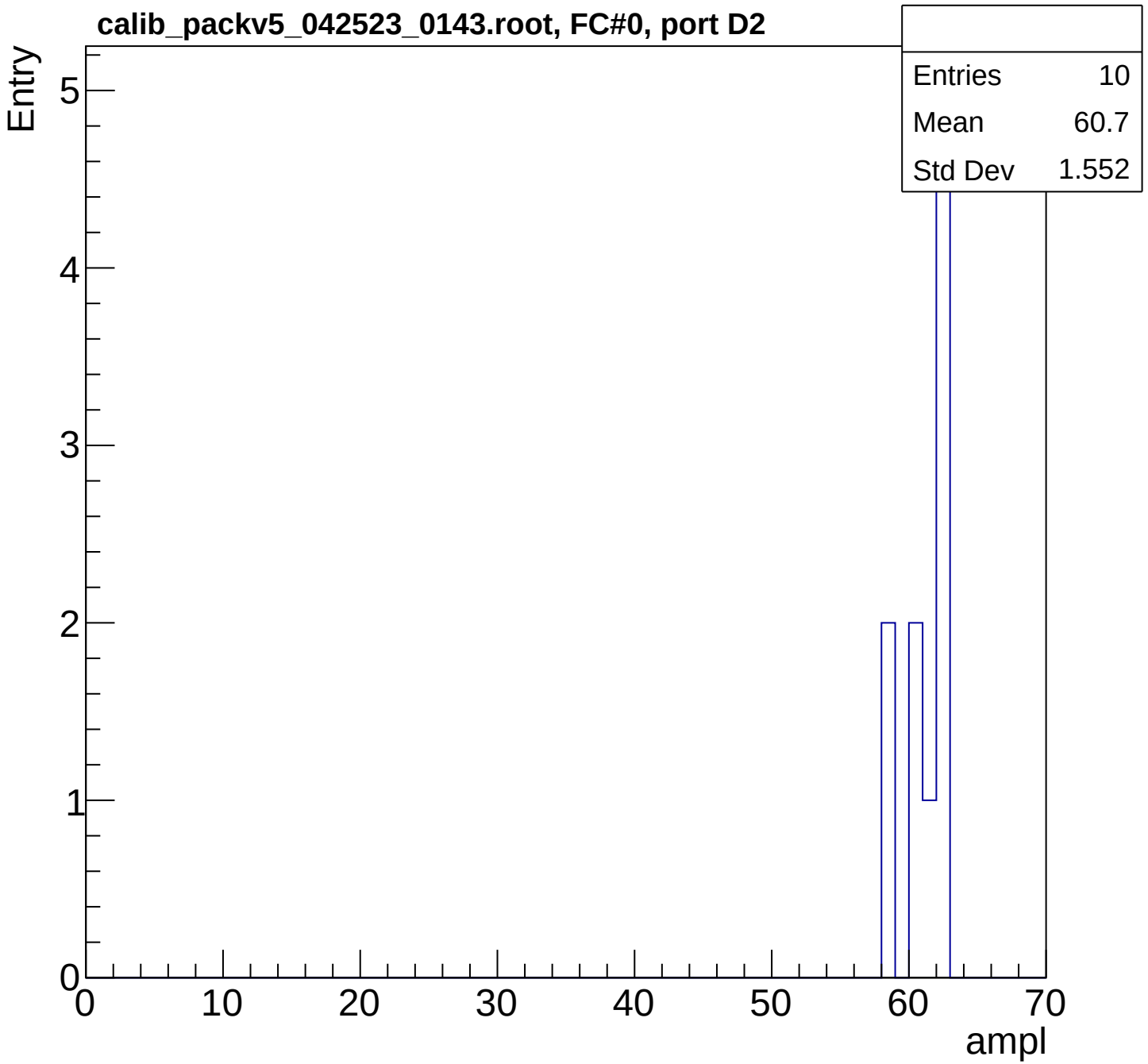
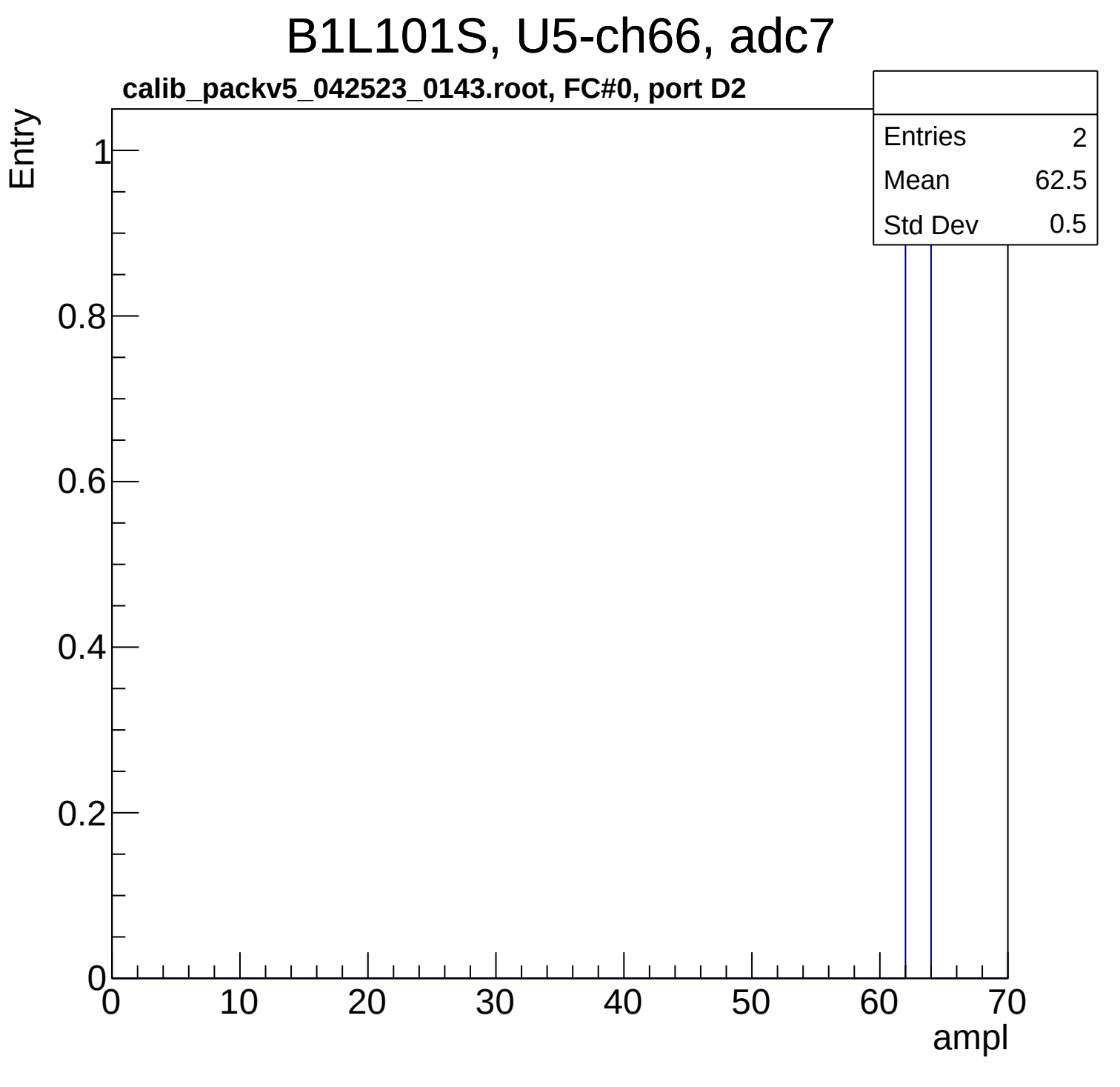
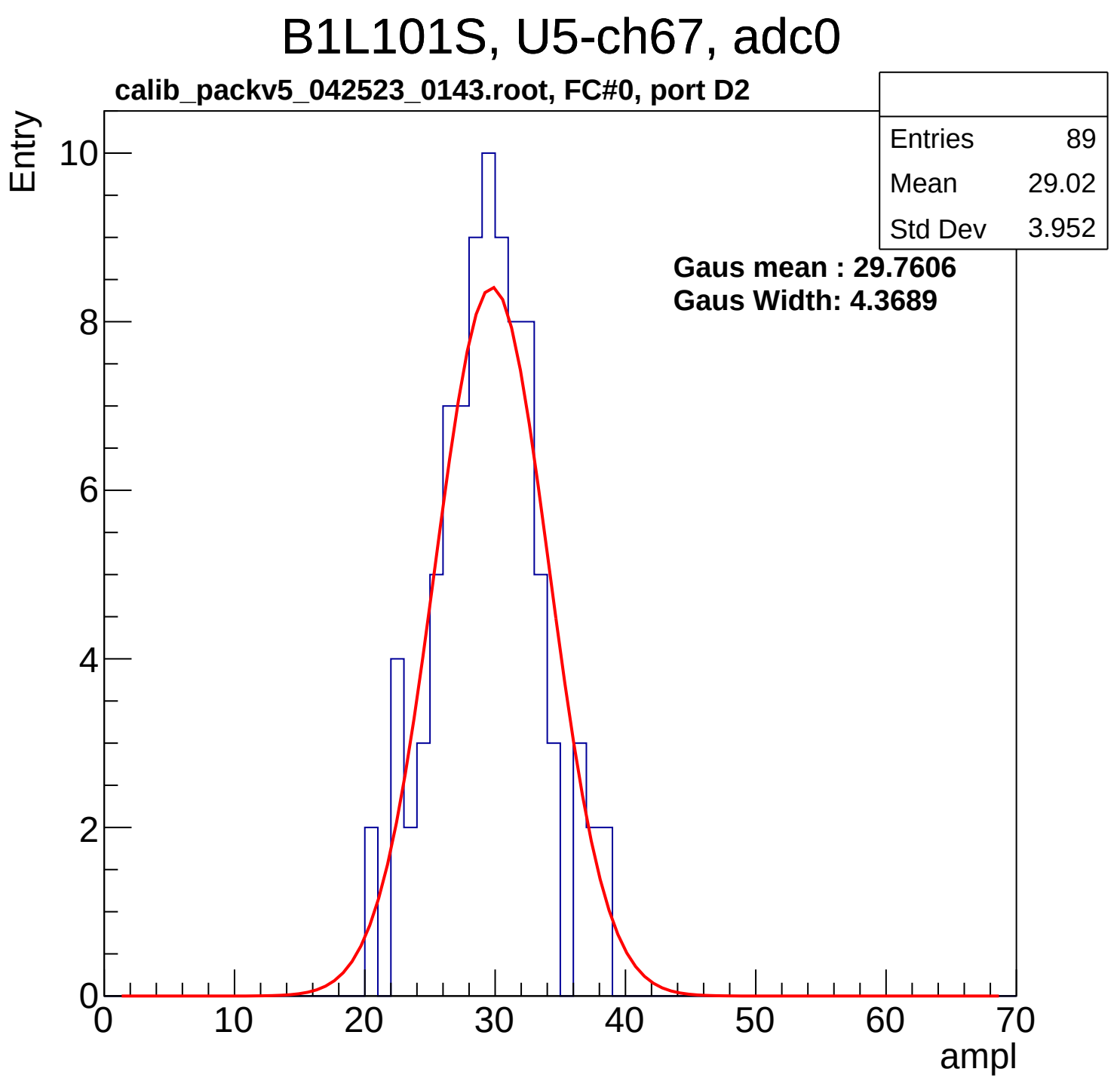
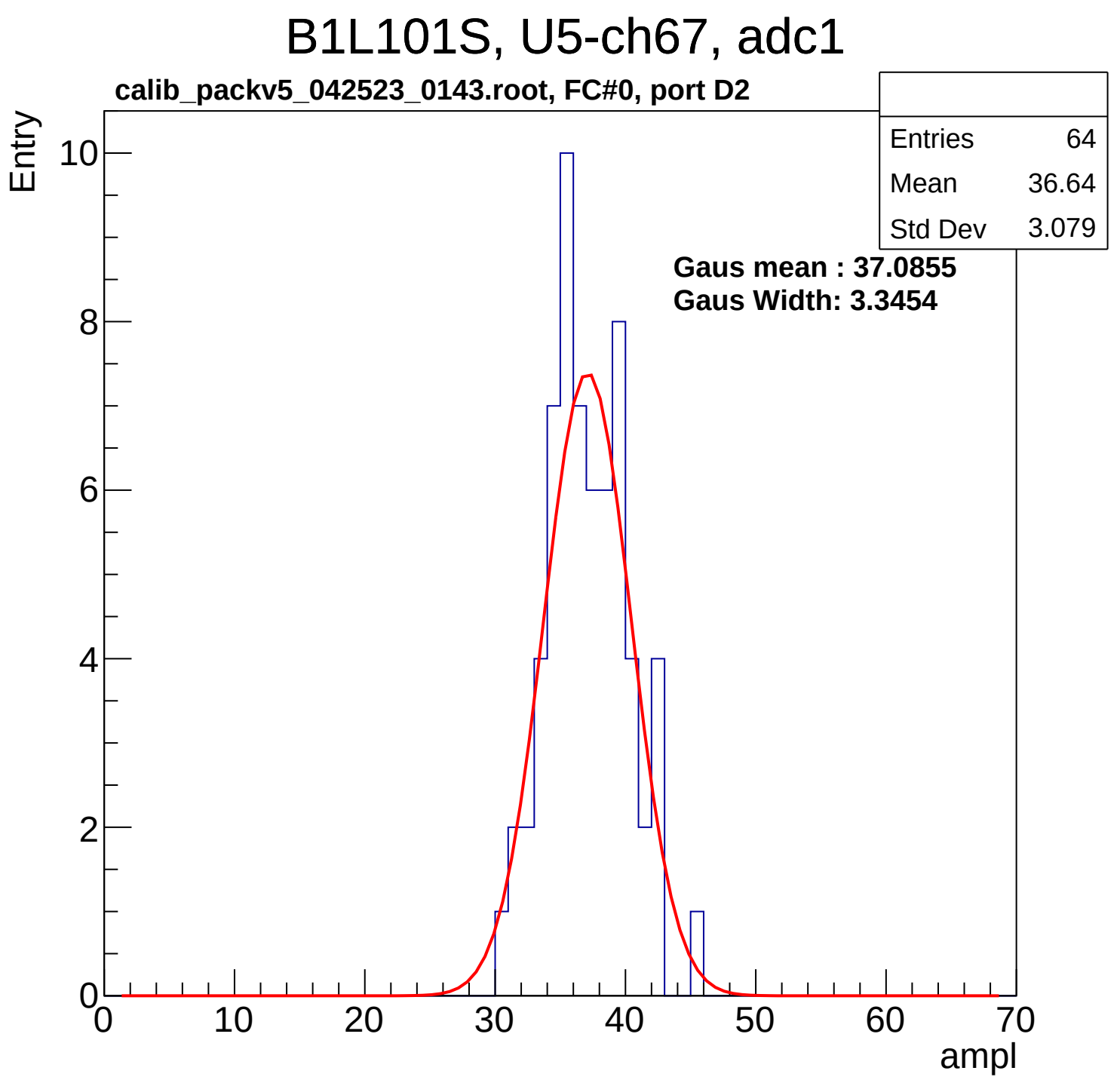

B1L101S, U5-ch66, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 53.59
Std Dev 2.725
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

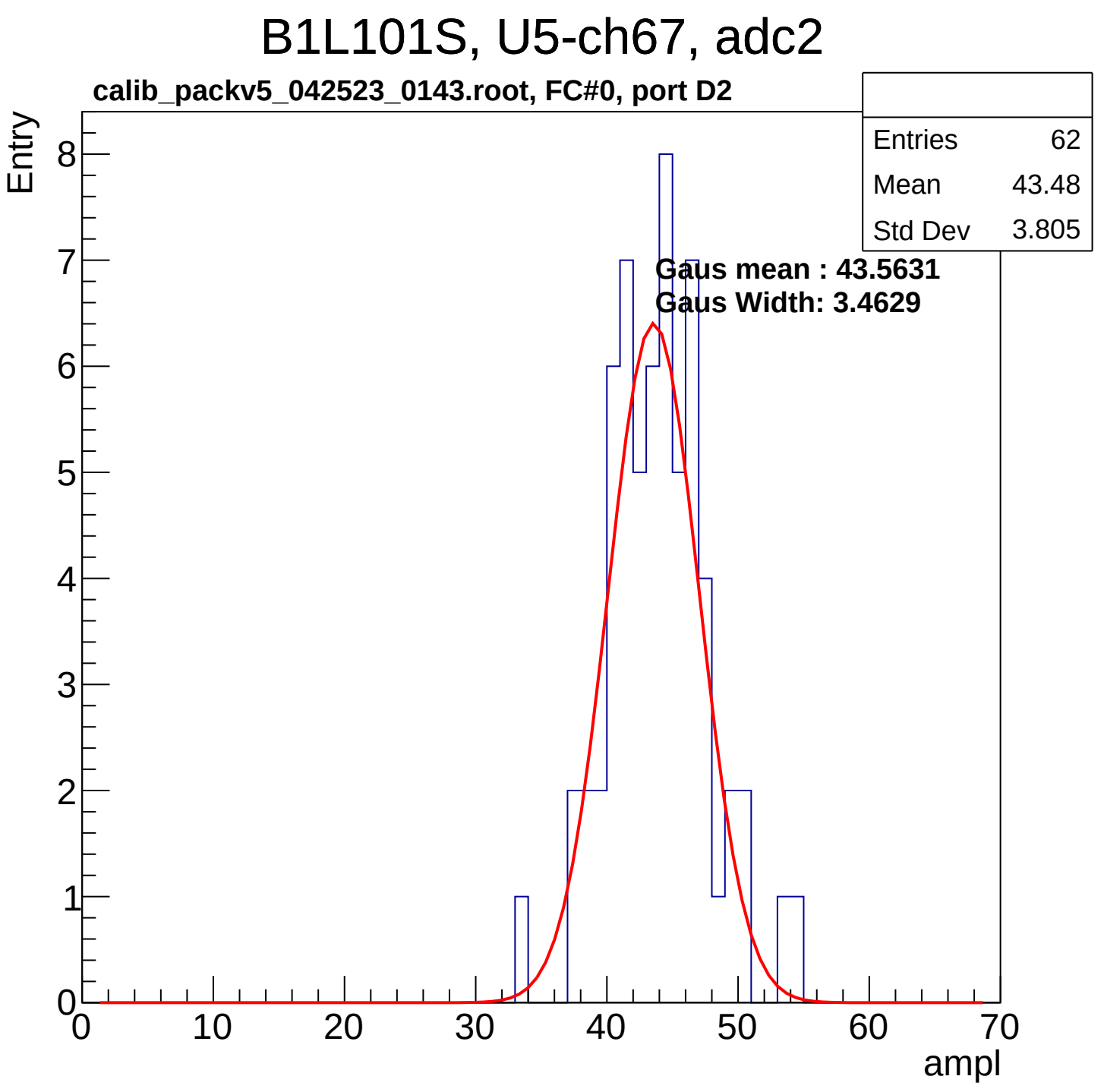

B1L101S, U5-ch66, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 58.21
Std Dev 7.921
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch66, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 60.7
Std Dev 1.552
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch66, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch67, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 89
Mean 29.02
Std Dev 3.952
Gaus mean : 29.7606
Gaus Width: 4.3689
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch67, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 36.64
Std Dev 3.079
Gaus mean : 37.0855
Gaus Width: 3.3454
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch67, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 43.48
Std Dev 3.805
Gaus mean : 43.5631
Gaus Width: 3.4629
Entry
ampl
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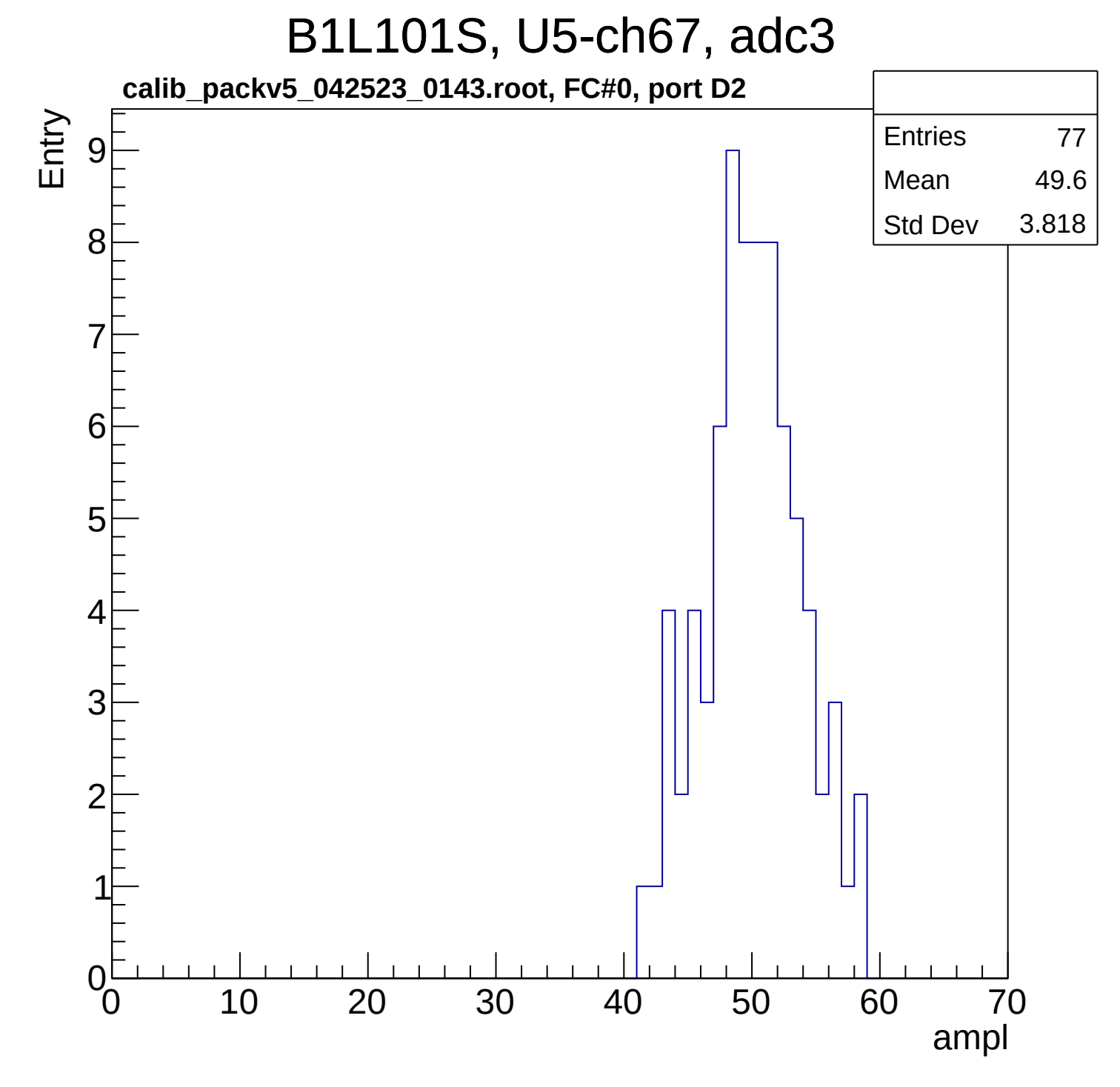
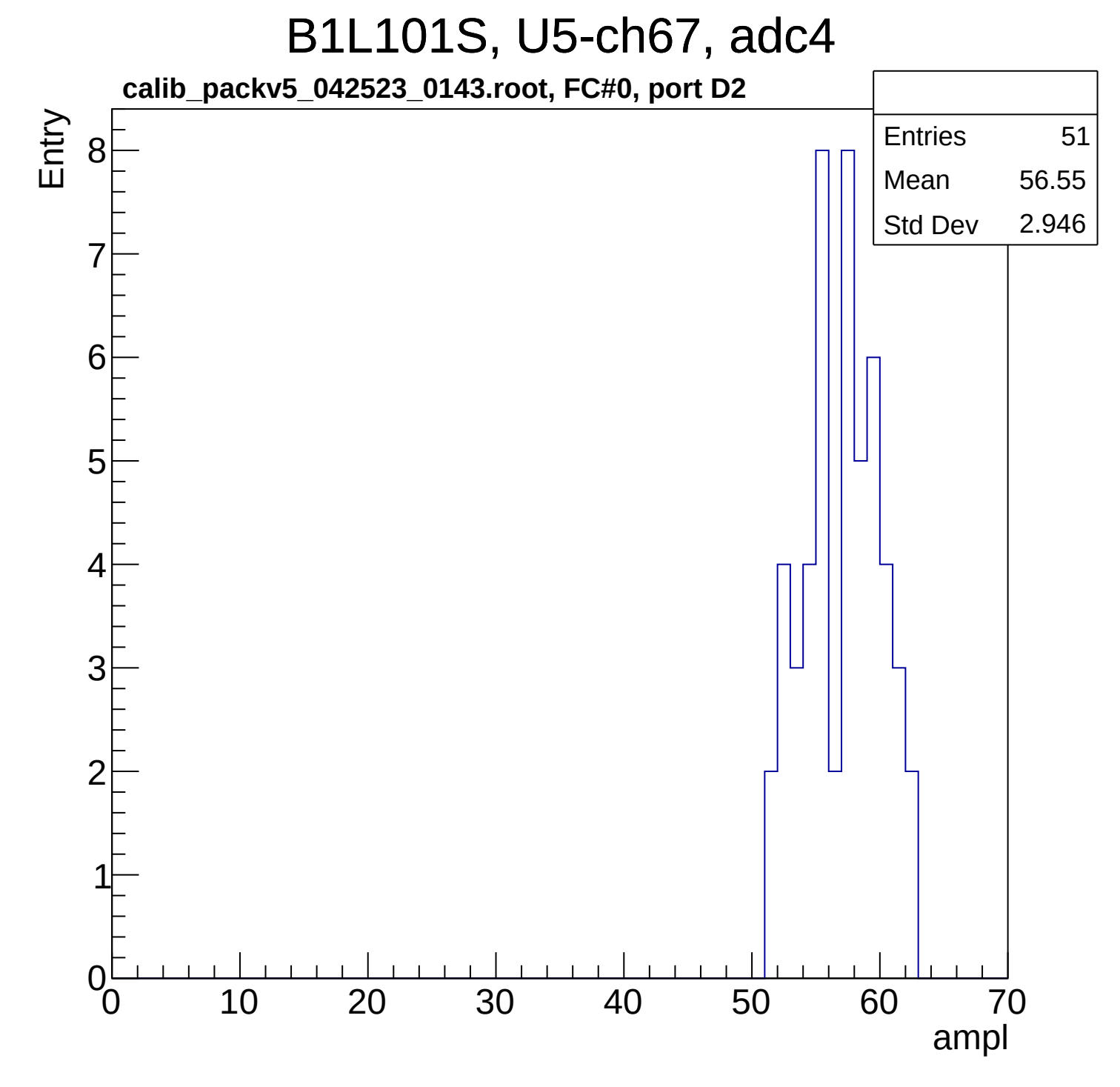
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch67, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 49.6
Std Dev 3.818
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch67, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 56.55
Std Dev 2.946
Entry
ampl
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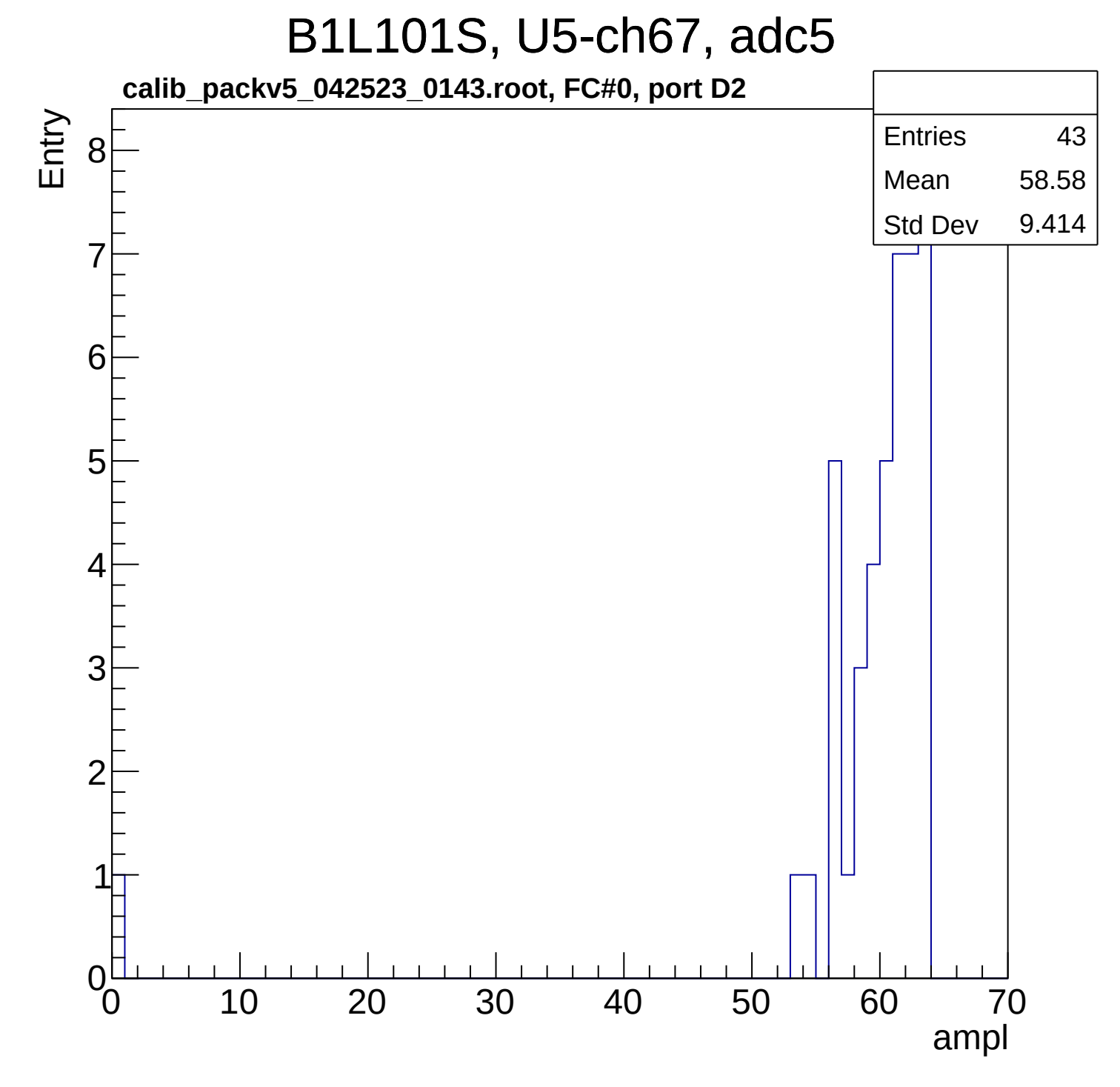
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch67, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 43
Mean 58.58
Std Dev 9.414
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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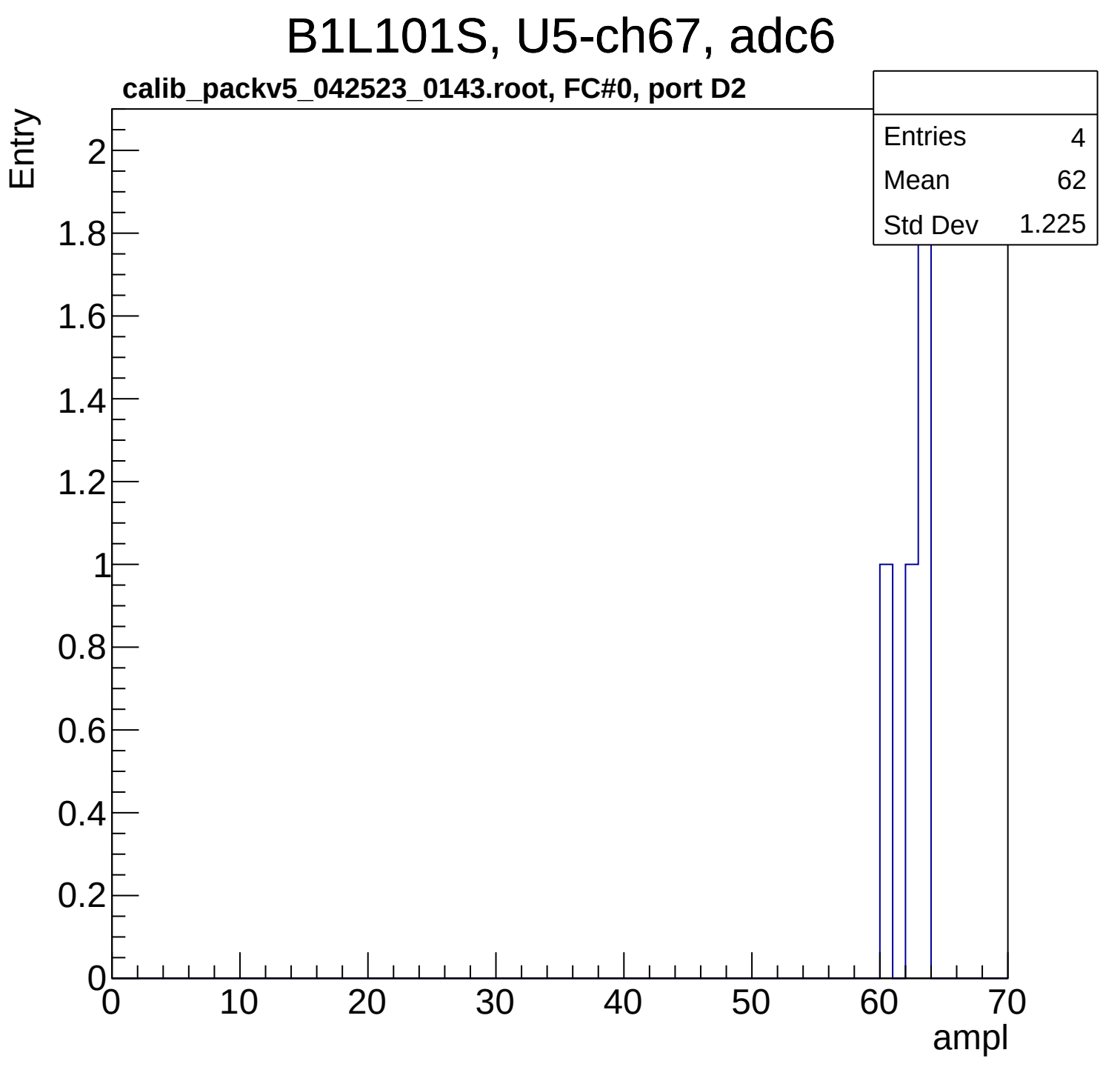
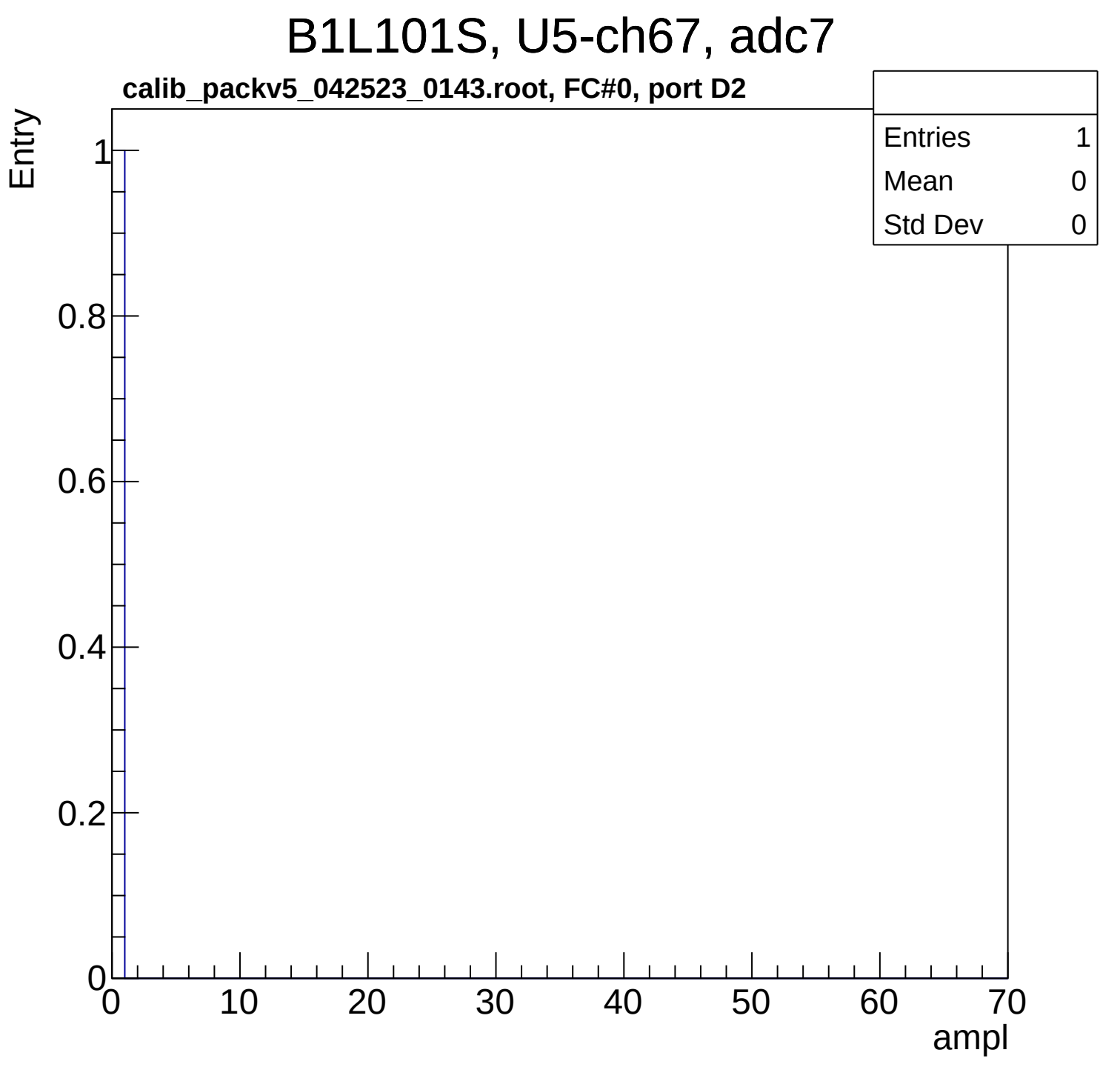
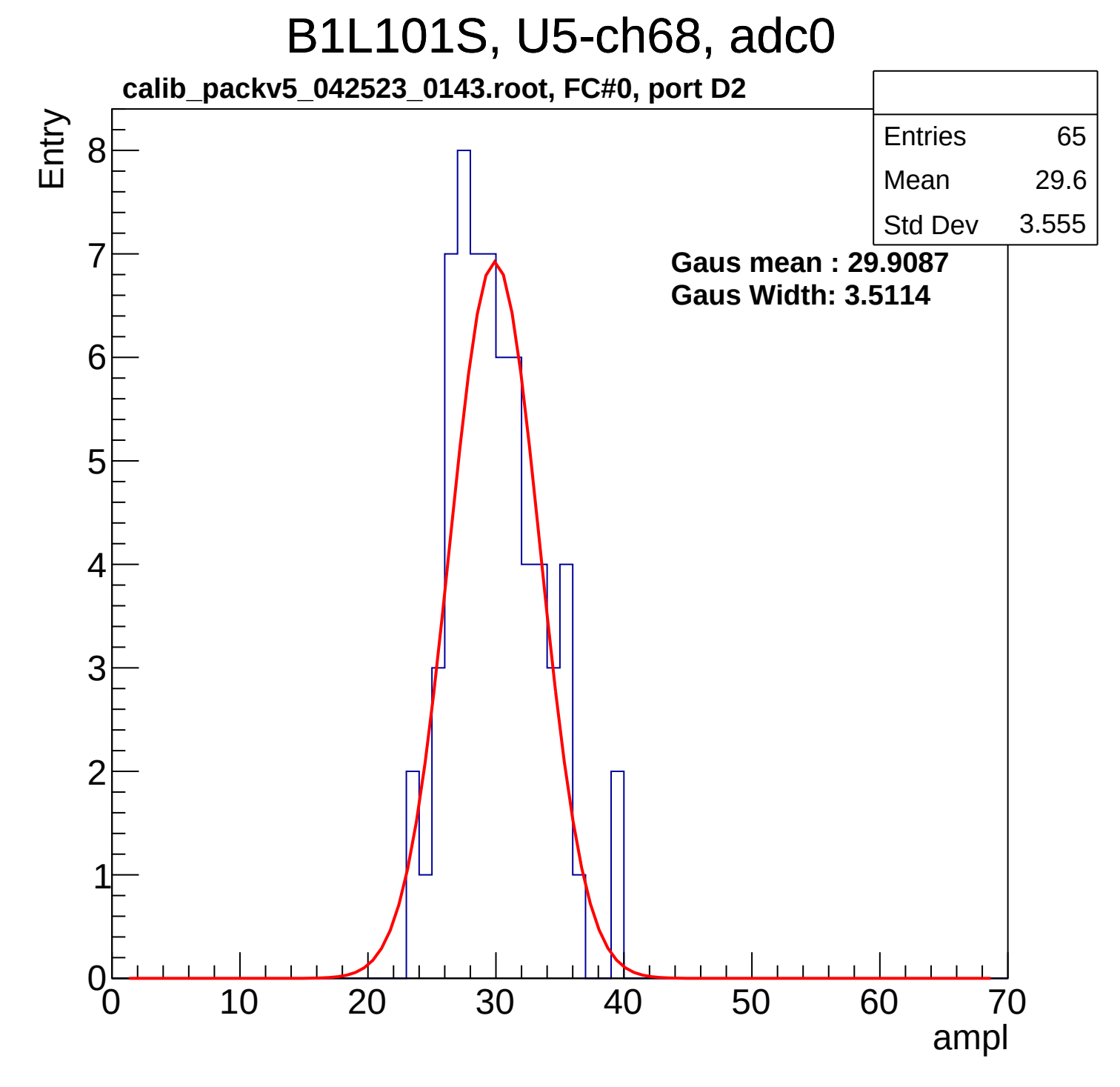

B1L101S, U5-ch67, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 62
Std Dev 1.225
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U5-ch67, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch68, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 29.6
Std Dev 3.555
Gaus mean : 29.9087
Gaus Width: 3.5114
Entry
ampl
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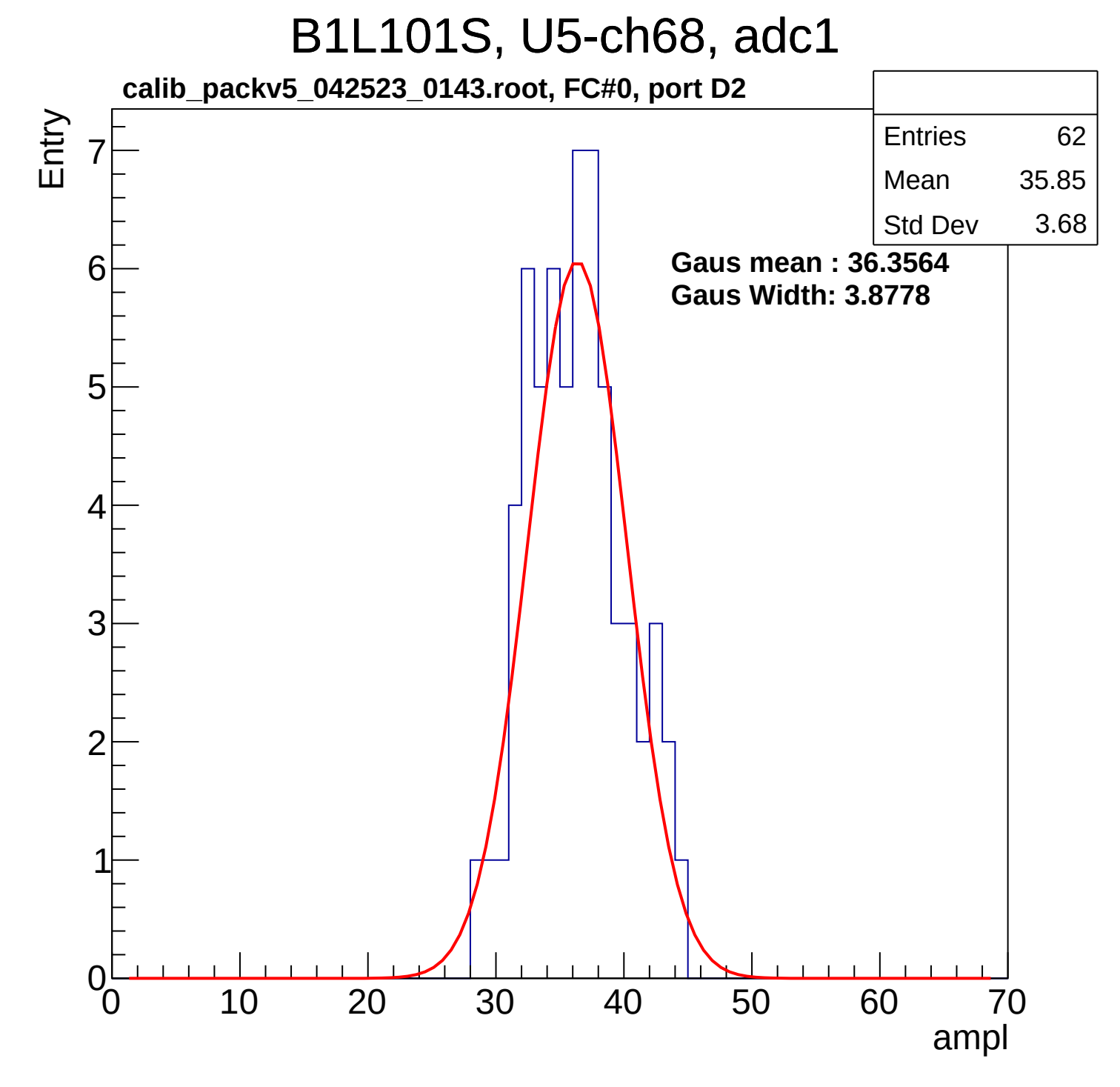
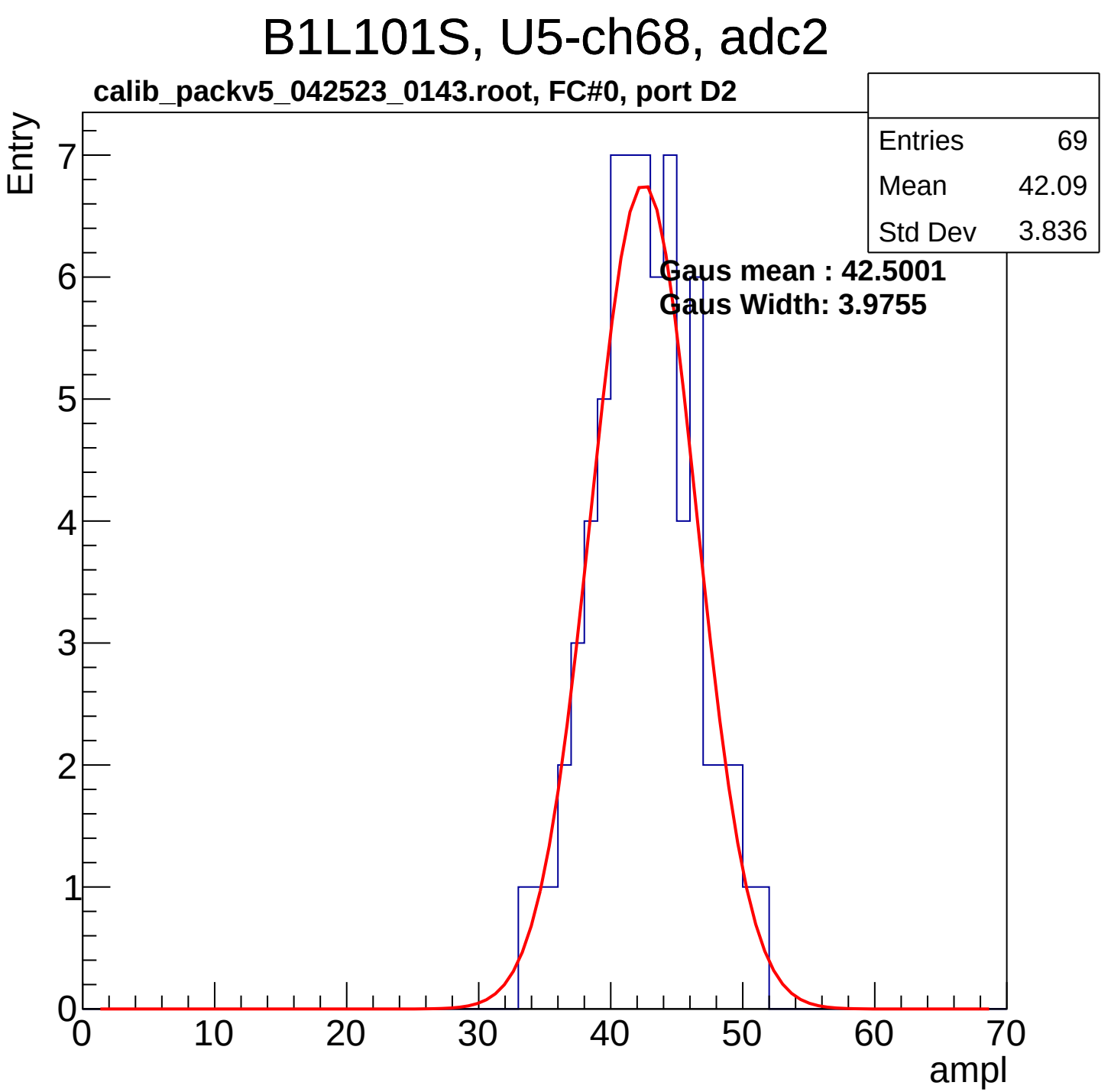
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch68, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 35.85
Std Dev 3.68
Gaus mean : 36.3564
Gaus Width: 3.8778
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch68, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 42.09
Std Dev 3.836
Gaus mean : 42.5001
Gaus Width: 3.9755
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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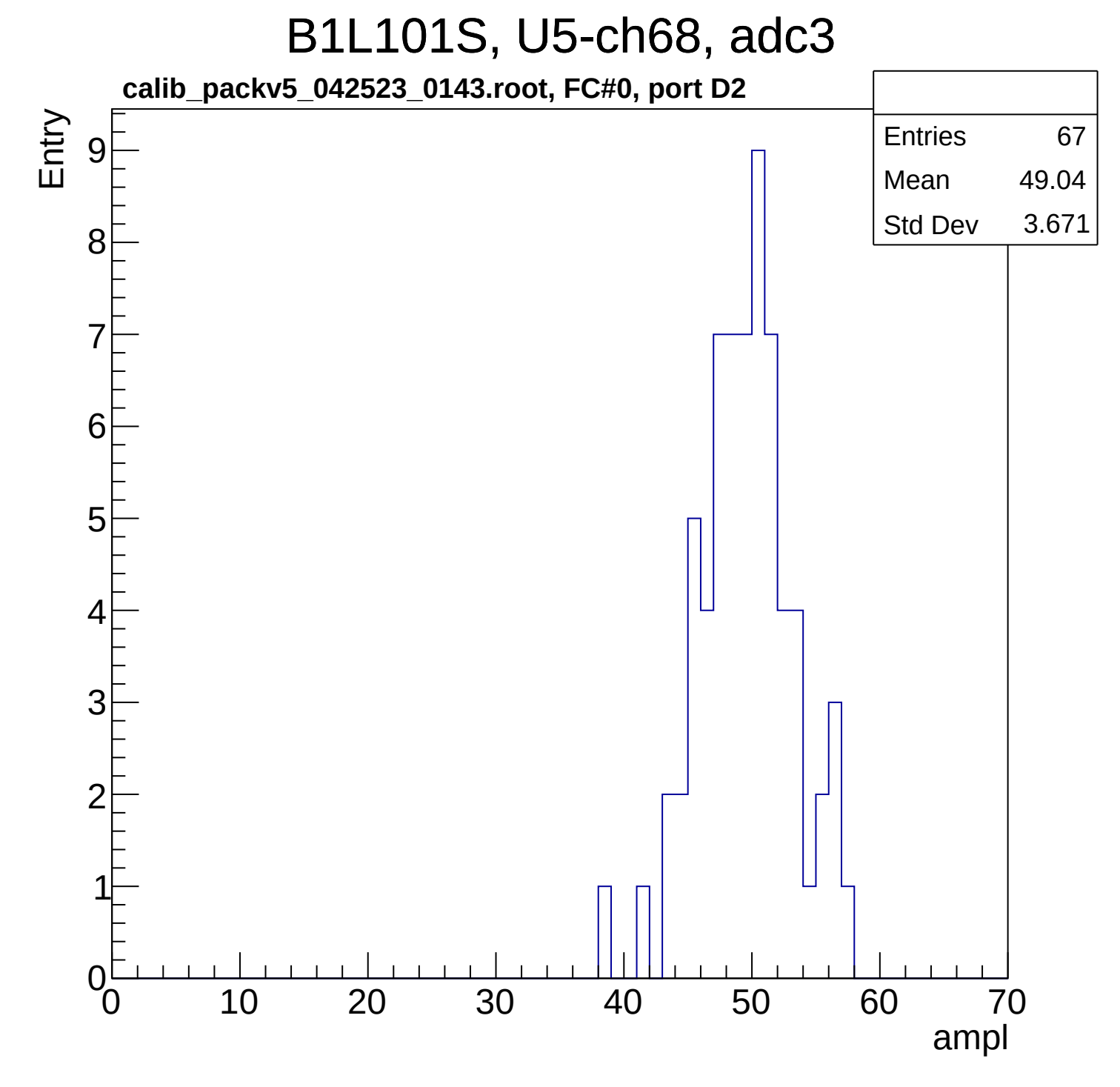
B1L101S, U5-ch68, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 49.04
Std Dev 3.671
Entry
ampl
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3
4
5
6
7
8
9
0
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60
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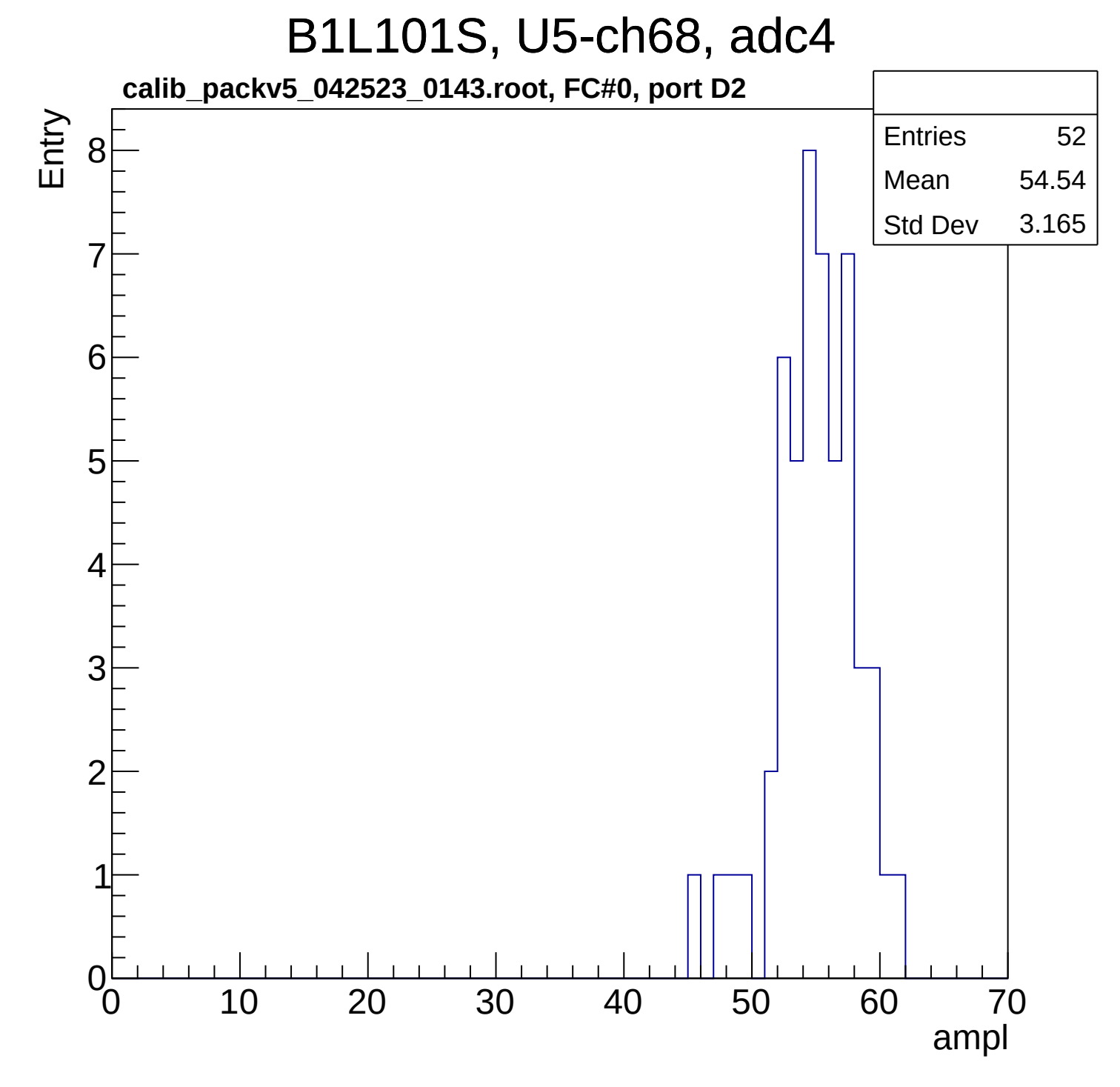
B1L101S, U5-ch68, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 54.54
Std Dev 3.165
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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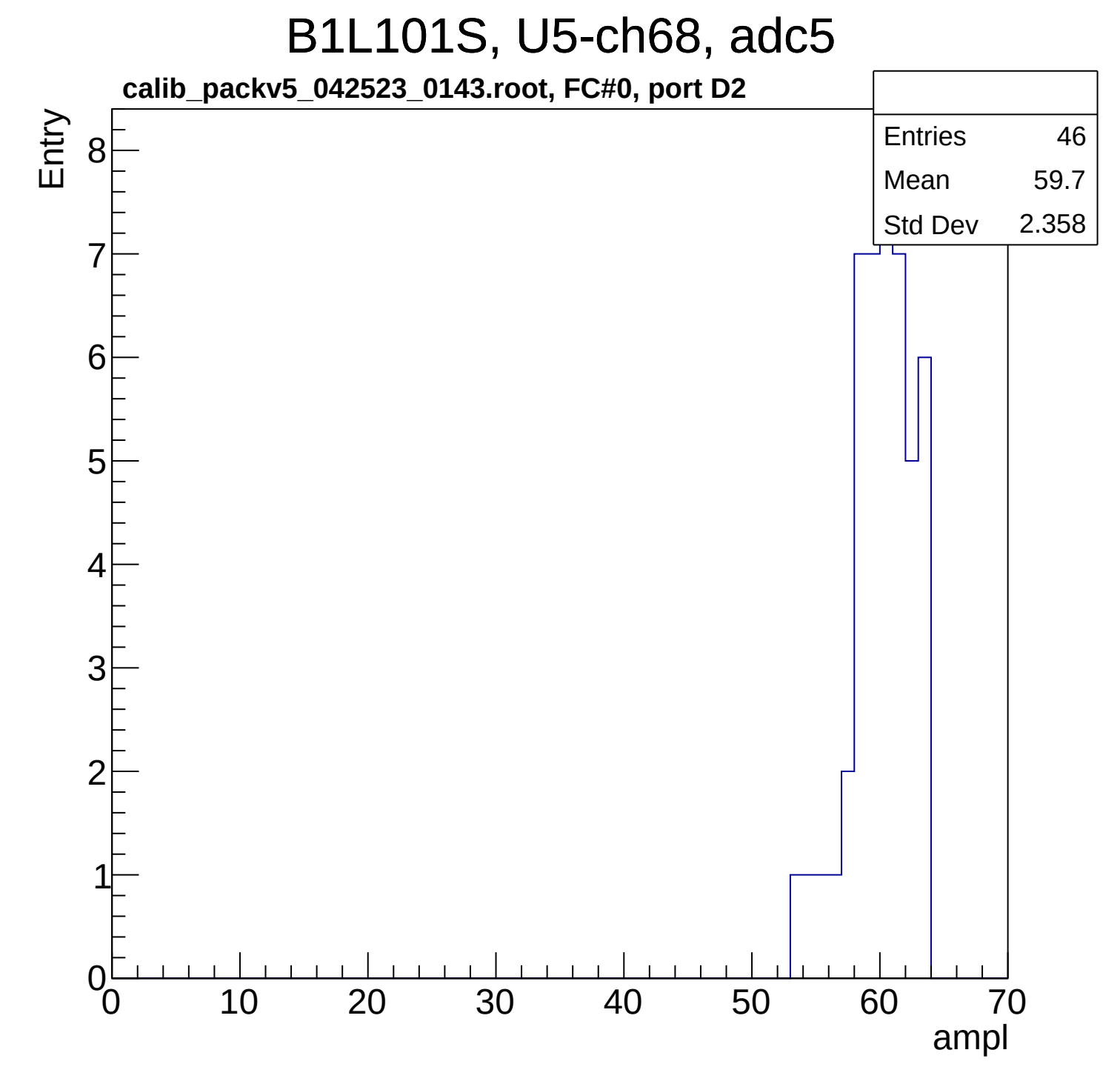
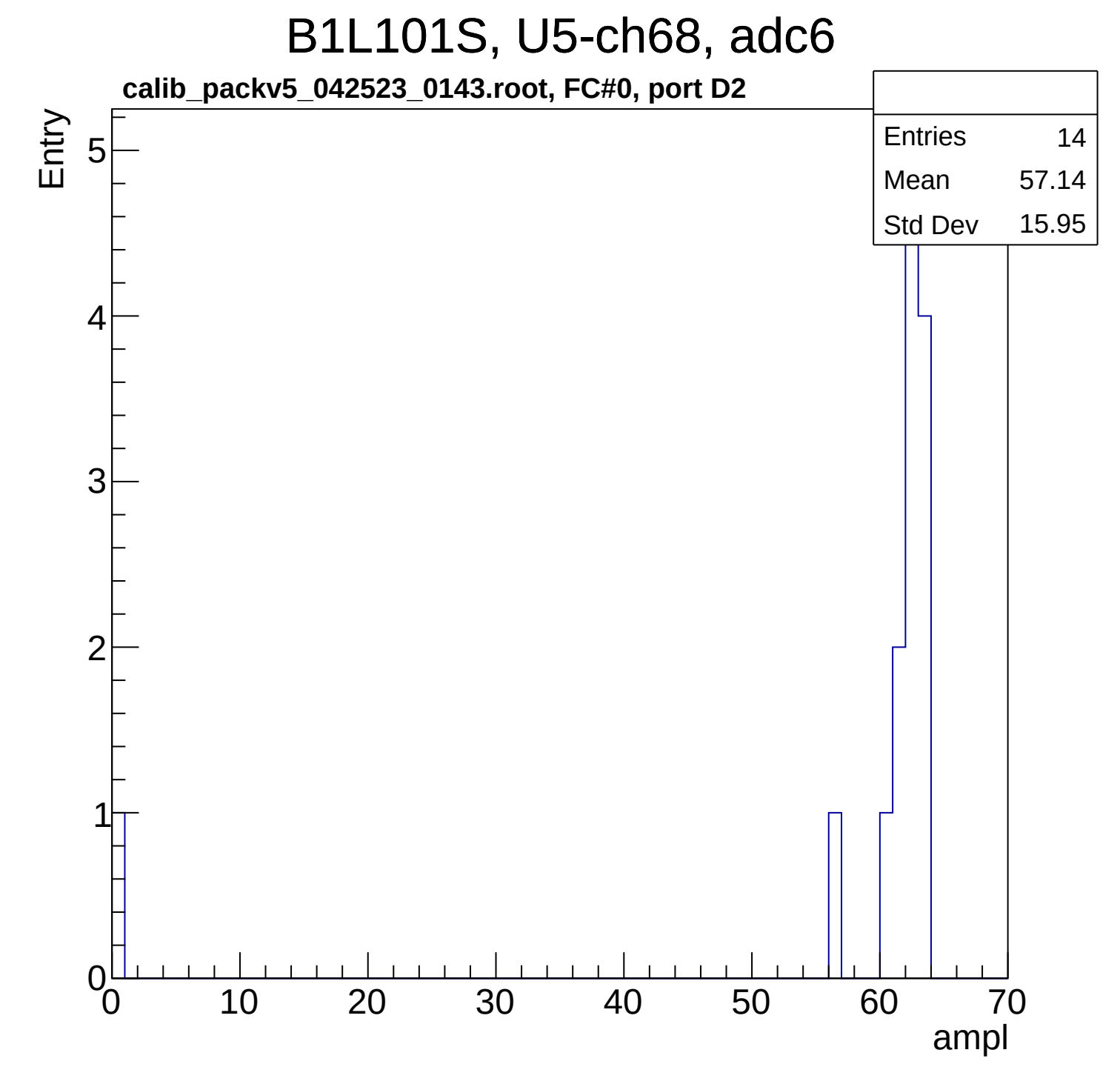

B1L101S, U5-ch68, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 59.7
Std Dev 2.358
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch68, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 14
Mean 57.14
Std Dev 15.95
Entry
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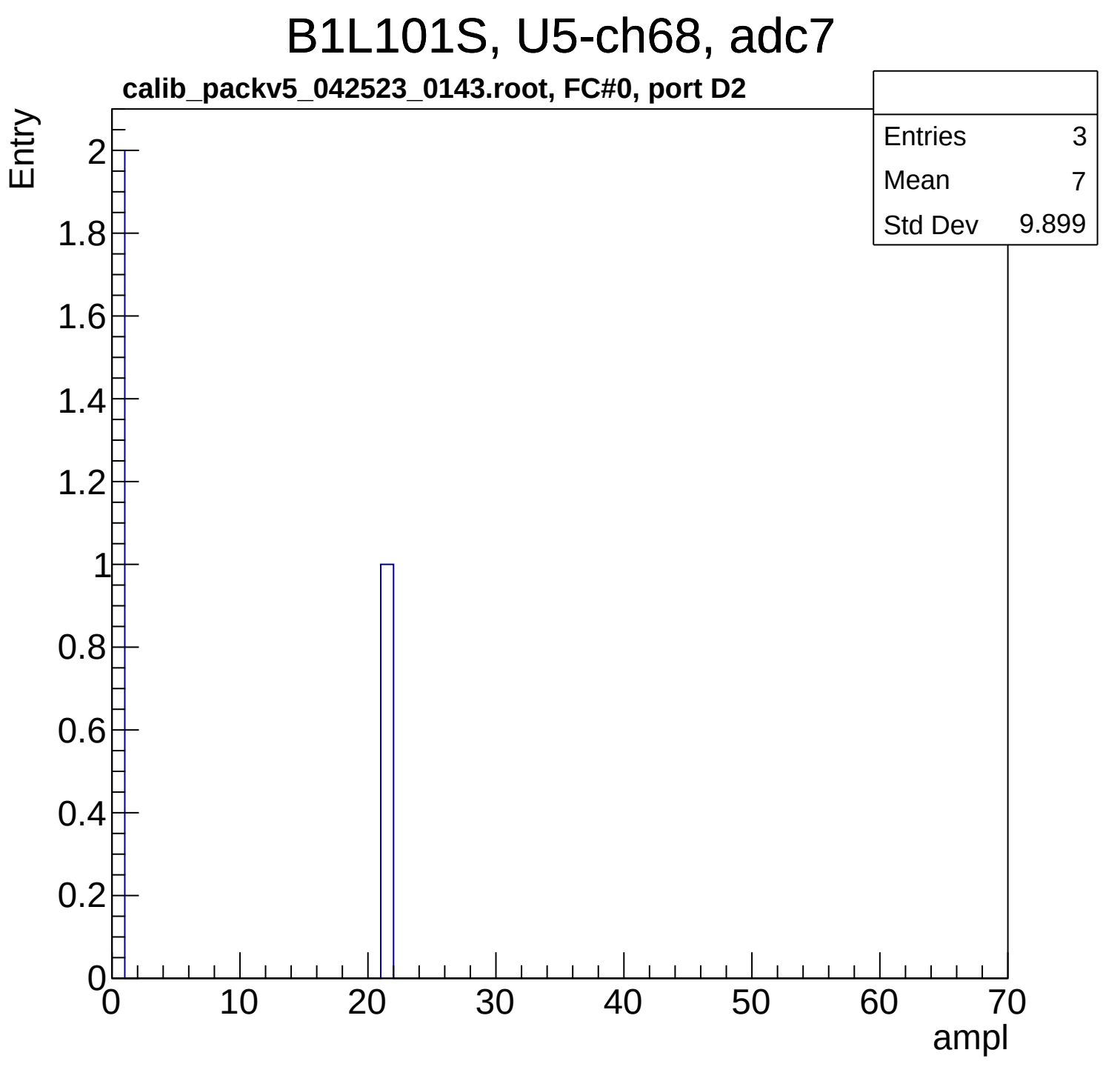
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch68, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 7
Std Dev 9.899
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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20
30
40
50
60
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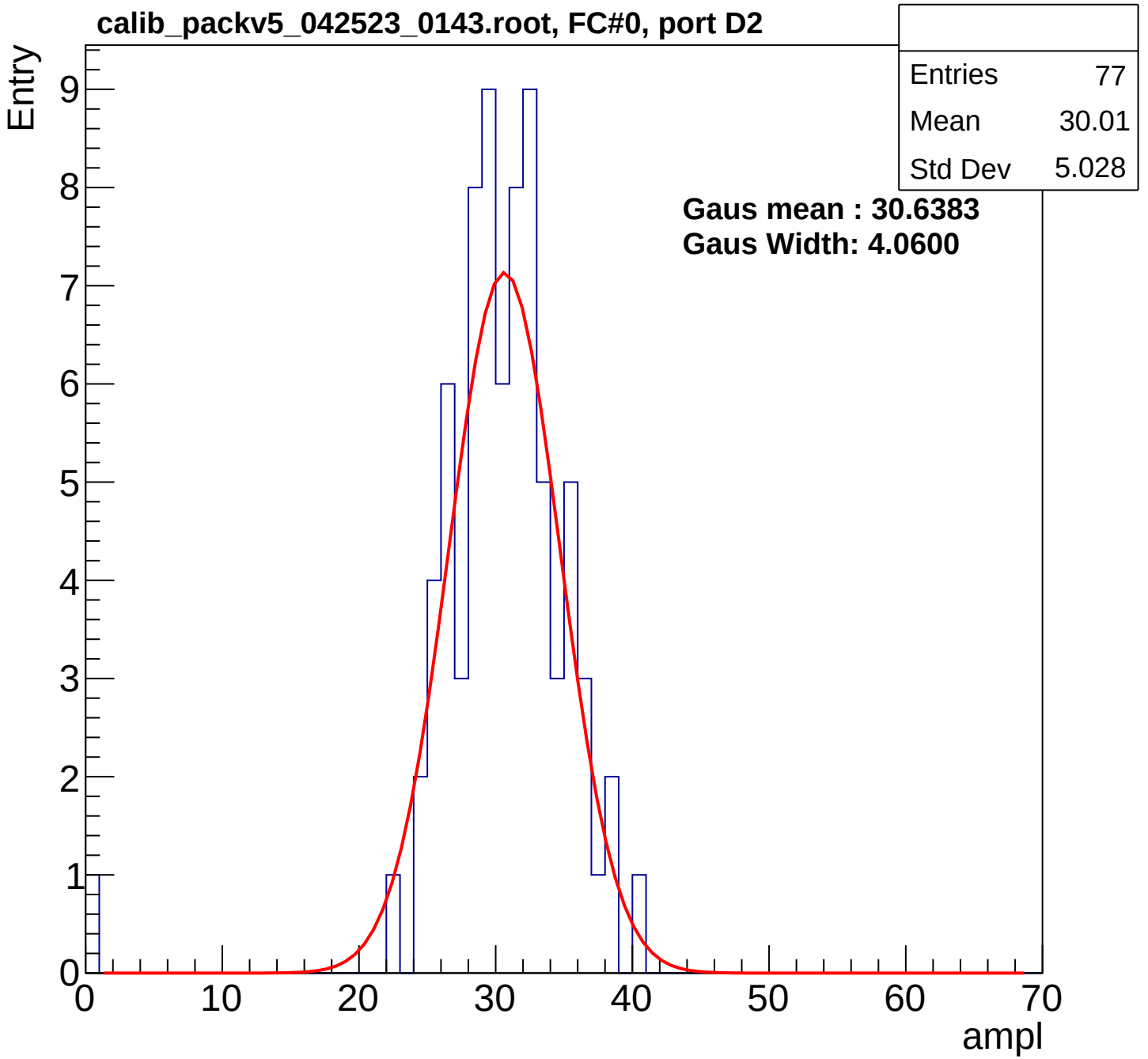
B1L101S, U5-ch69, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 30.01
Std Dev 5.028
Gaus mean : 30.6383
Gaus Width: 4.0600
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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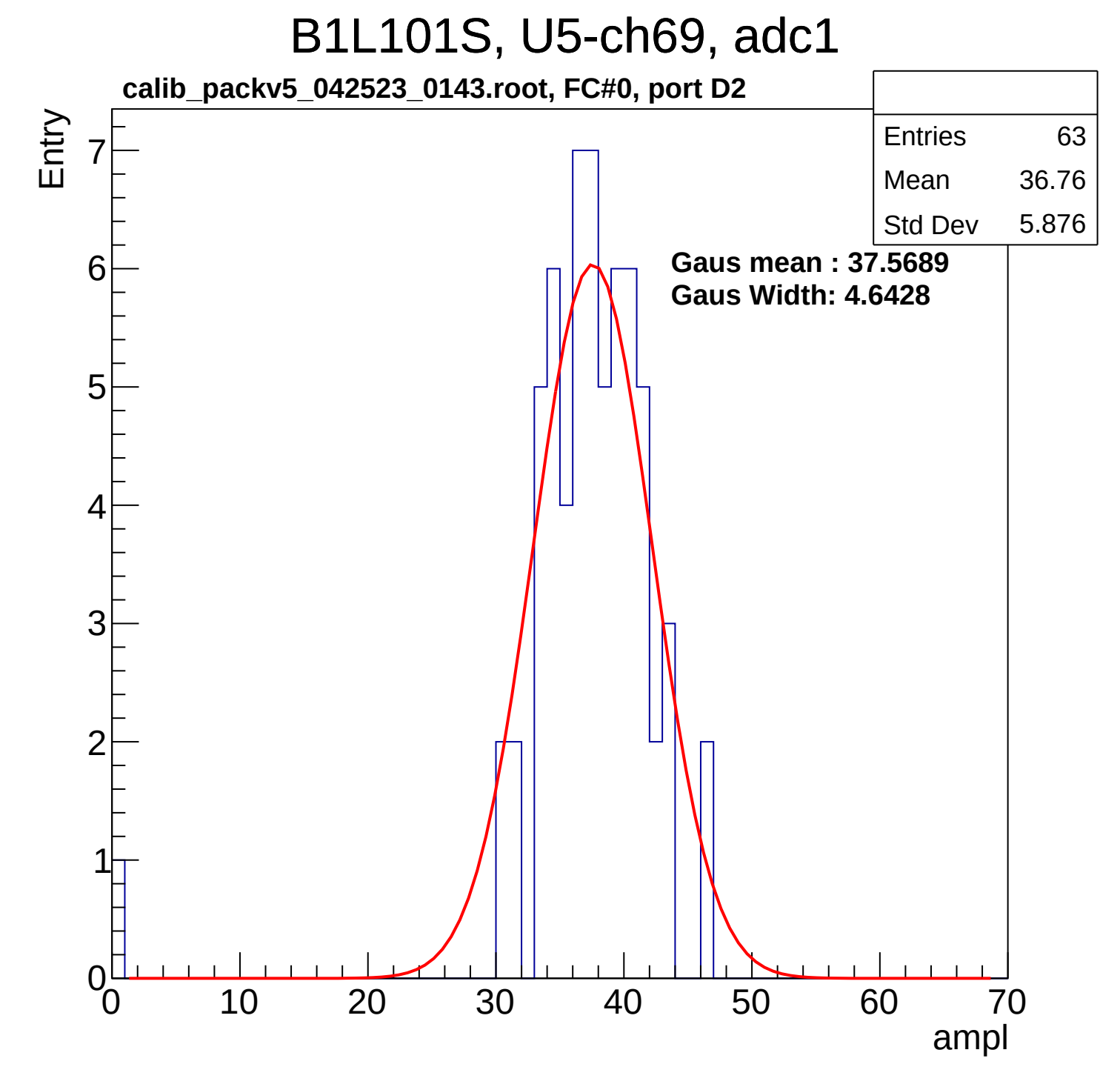
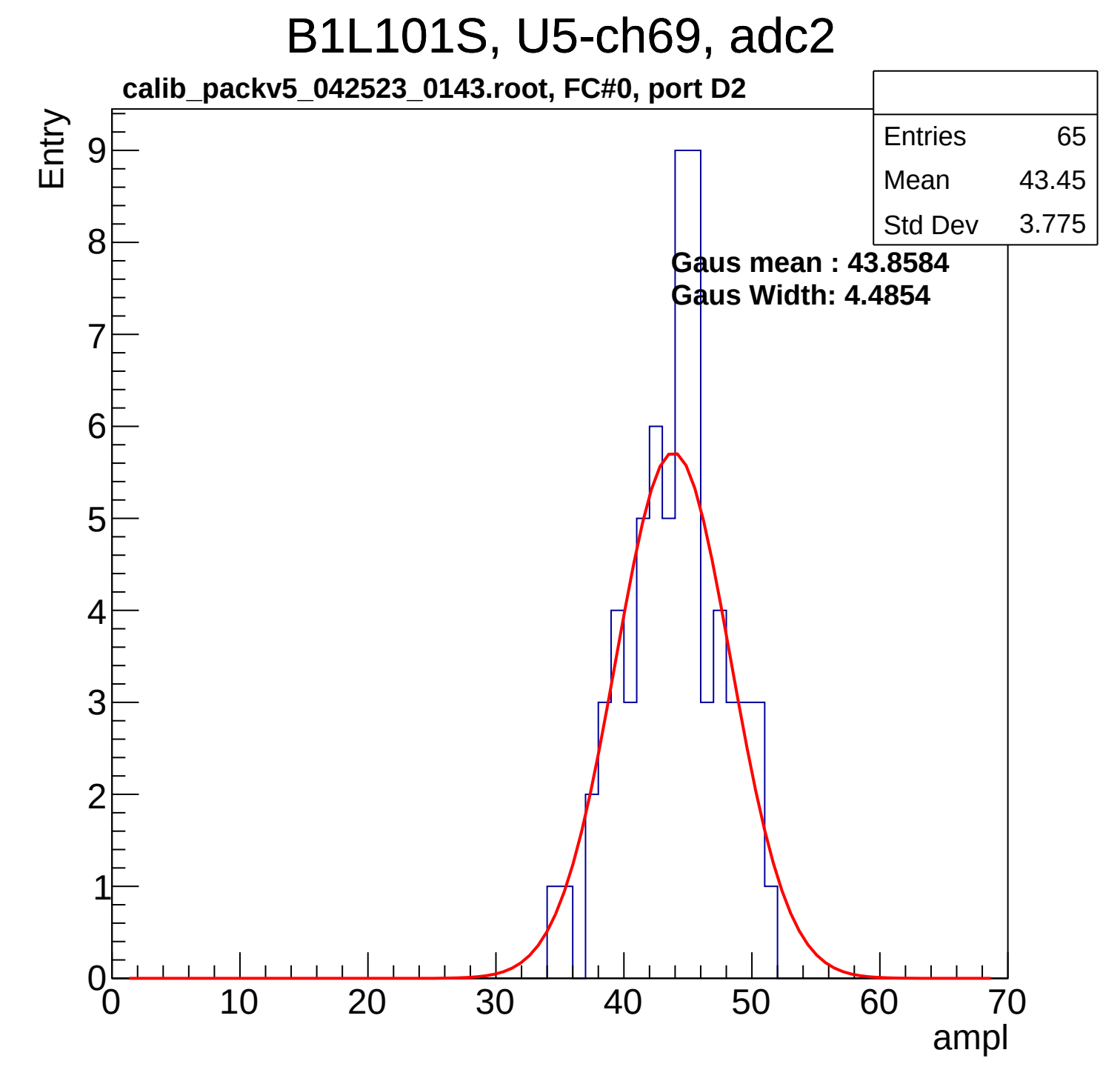

B1L101S, U5-ch69, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 36.76
Std Dev 5.876
Gaus mean : 37.5689
Gaus Width: 4.6428
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch69, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 43.45
Std Dev 3.775
Gaus mean : 43.8584
Gaus Width: 4.4854
Entry
ampl
0
1
2
3
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6
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0
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60
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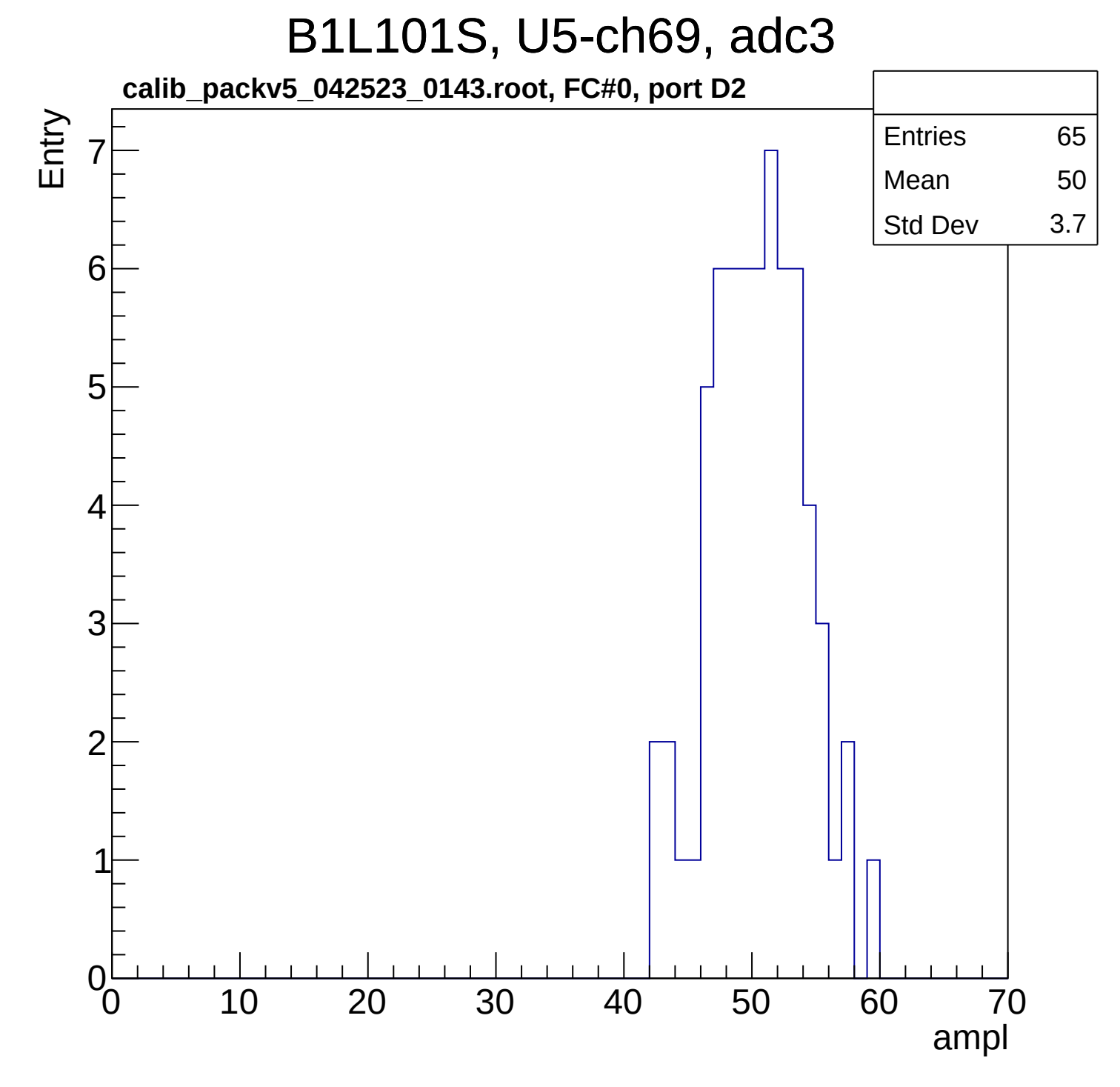
B1L101S, U5-ch69, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 50
Std Dev 3.7
Entry
ampl
0
1
2
3
4
5
6
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0
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60
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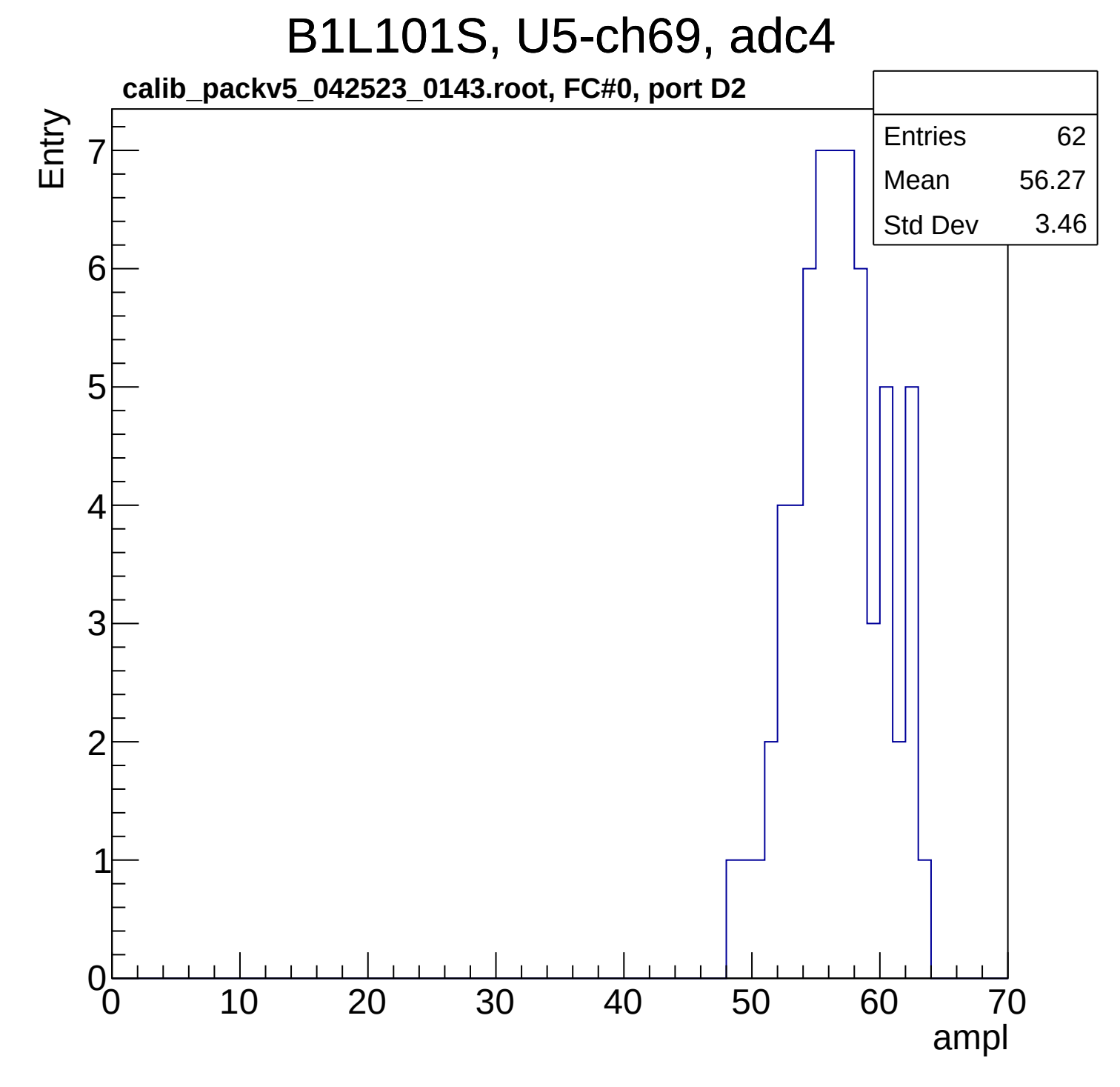
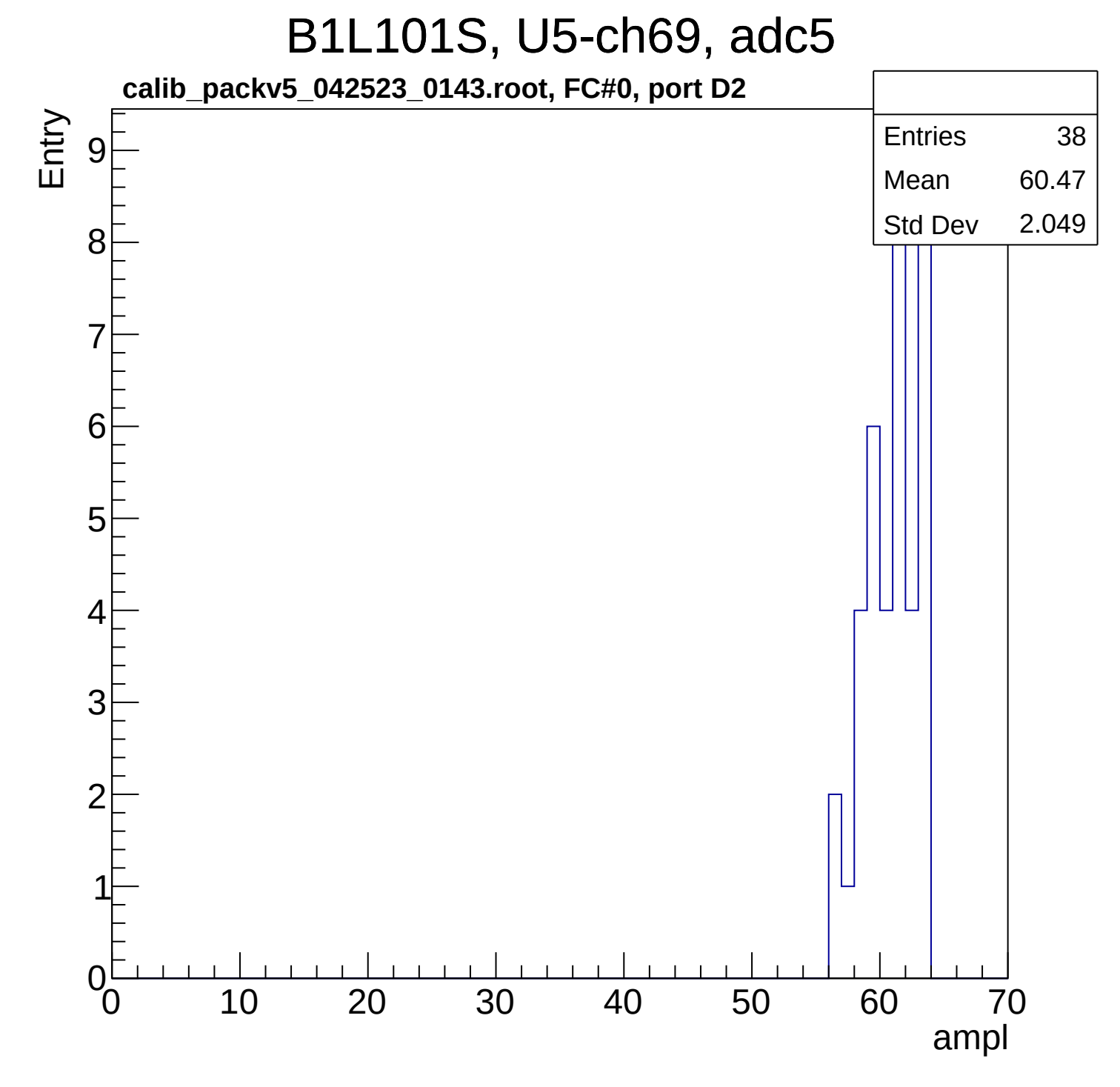

B1L101S, U5-ch69, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 56.27
Std Dev 3.46
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch69, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 38
Mean 60.47
Std Dev 2.049
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
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60
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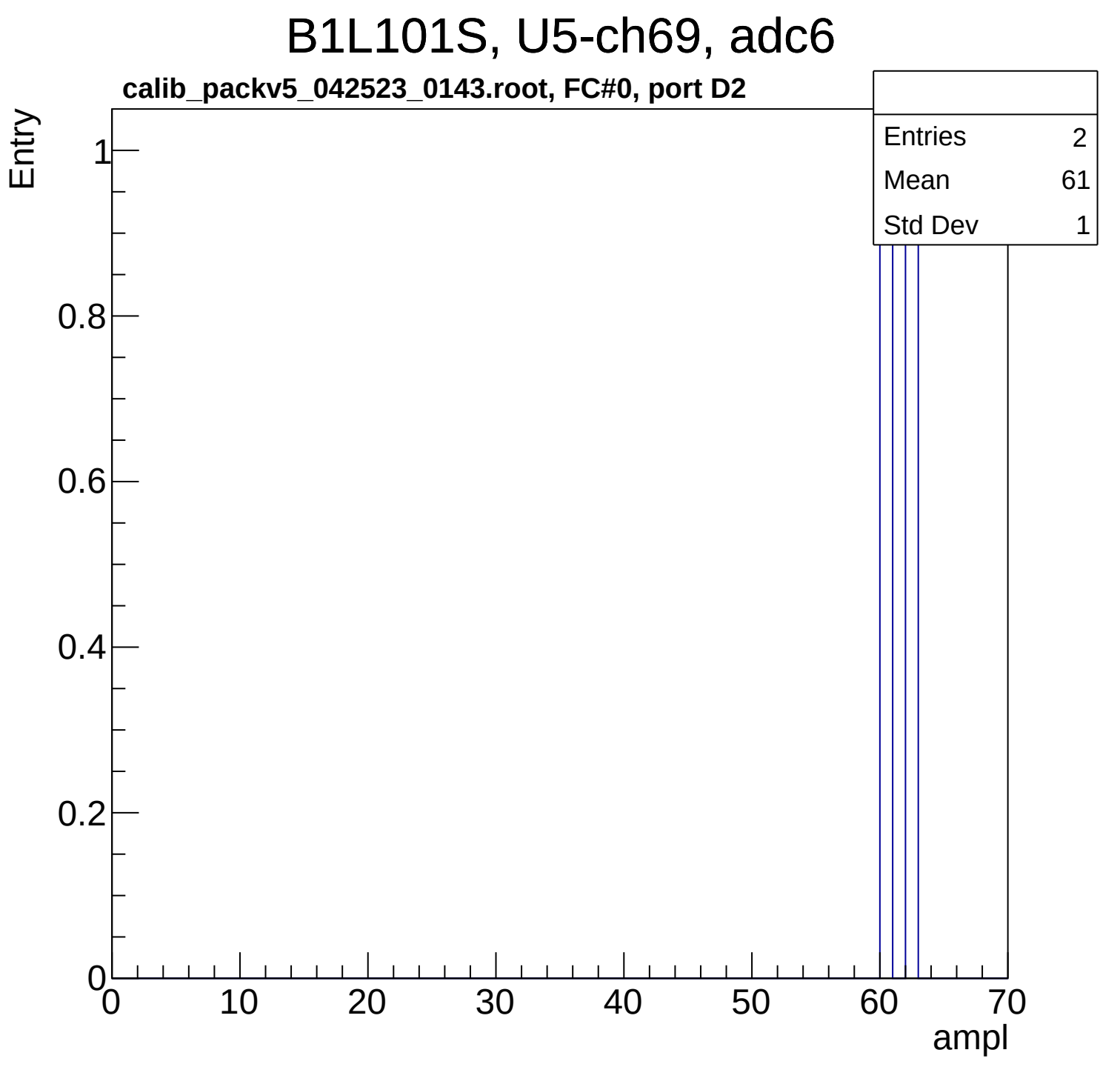
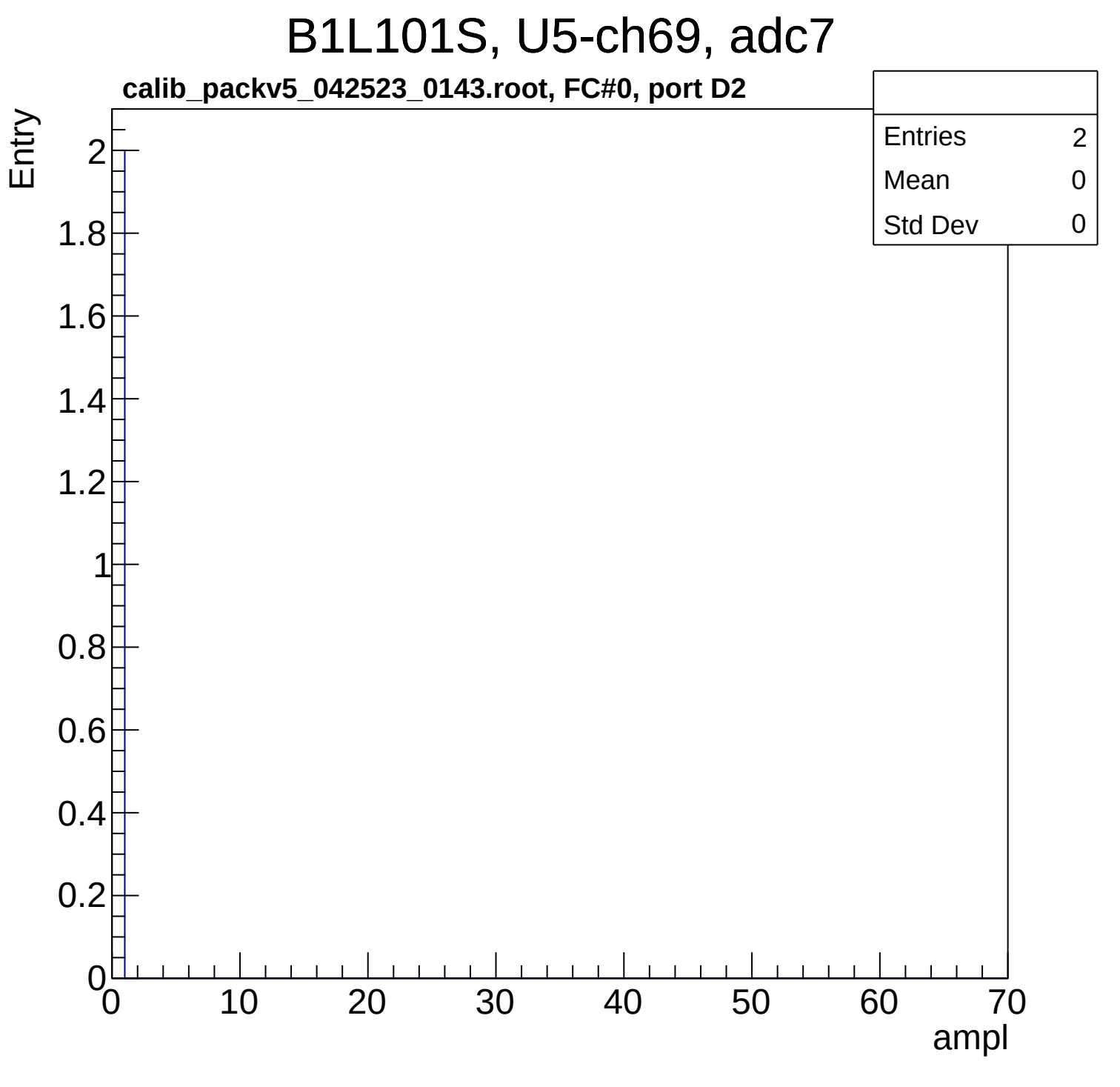

B1L101S, U5-ch69, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 61
Std Dev 1
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch69, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
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40
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60
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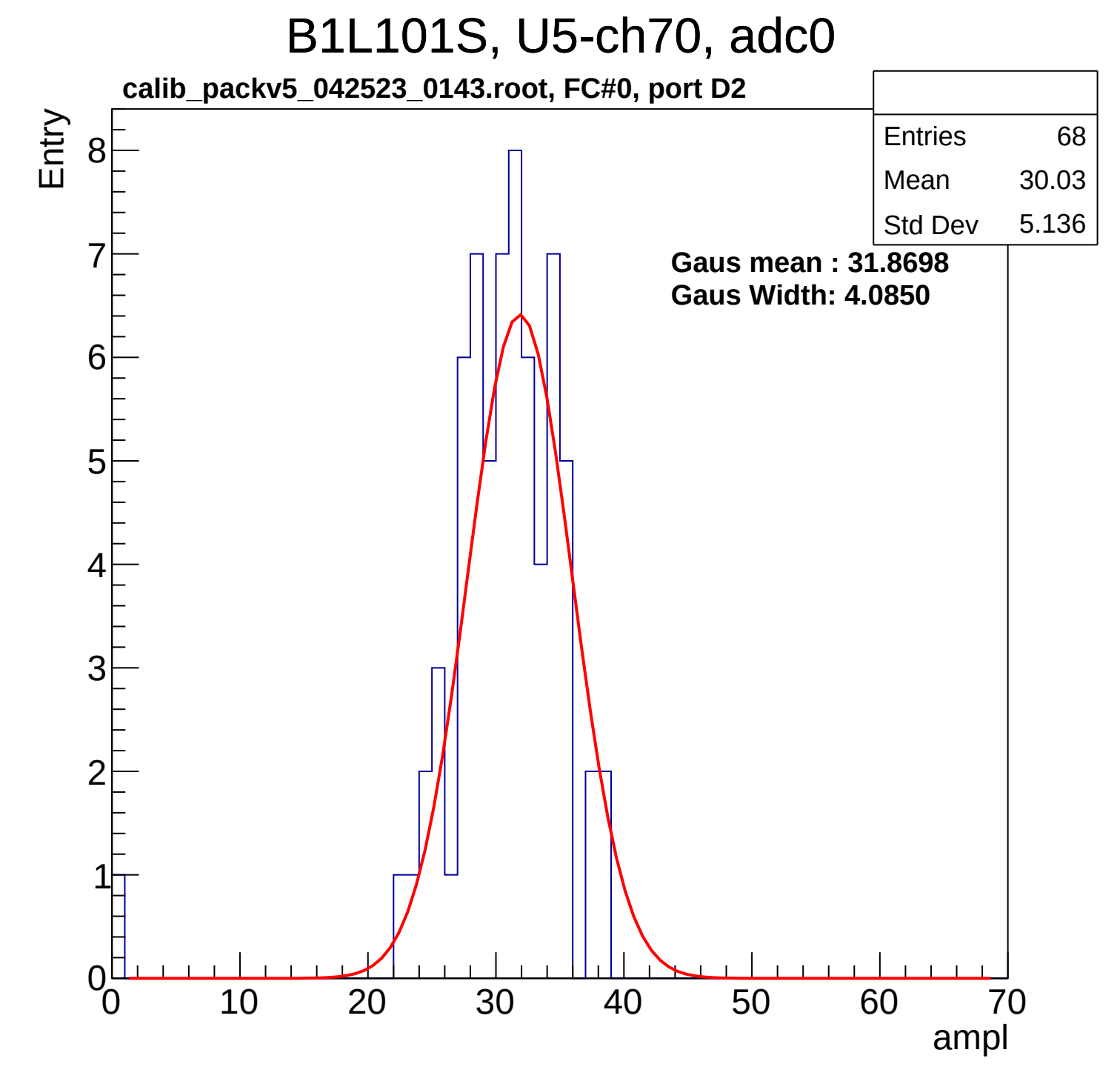
B1L101S, U5-ch70, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 30.03
Std Dev 5.136
Gaus mean : 31.8698
Gaus Width: 4.0850
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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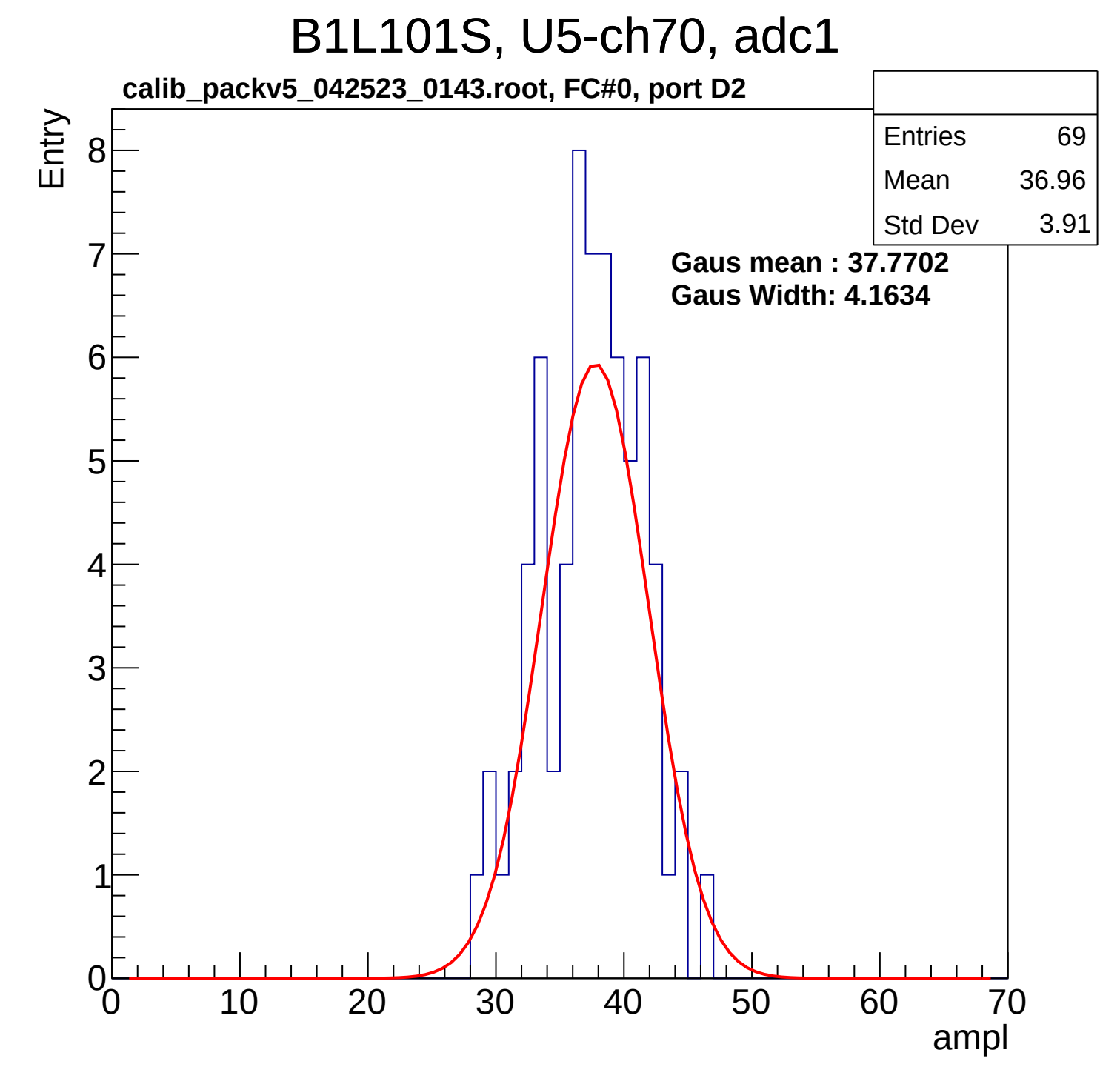
B1L101S, U5-ch70, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 36.96
Std Dev 3.91
Gaus mean : 37.7702
Gaus Width: 4.1634
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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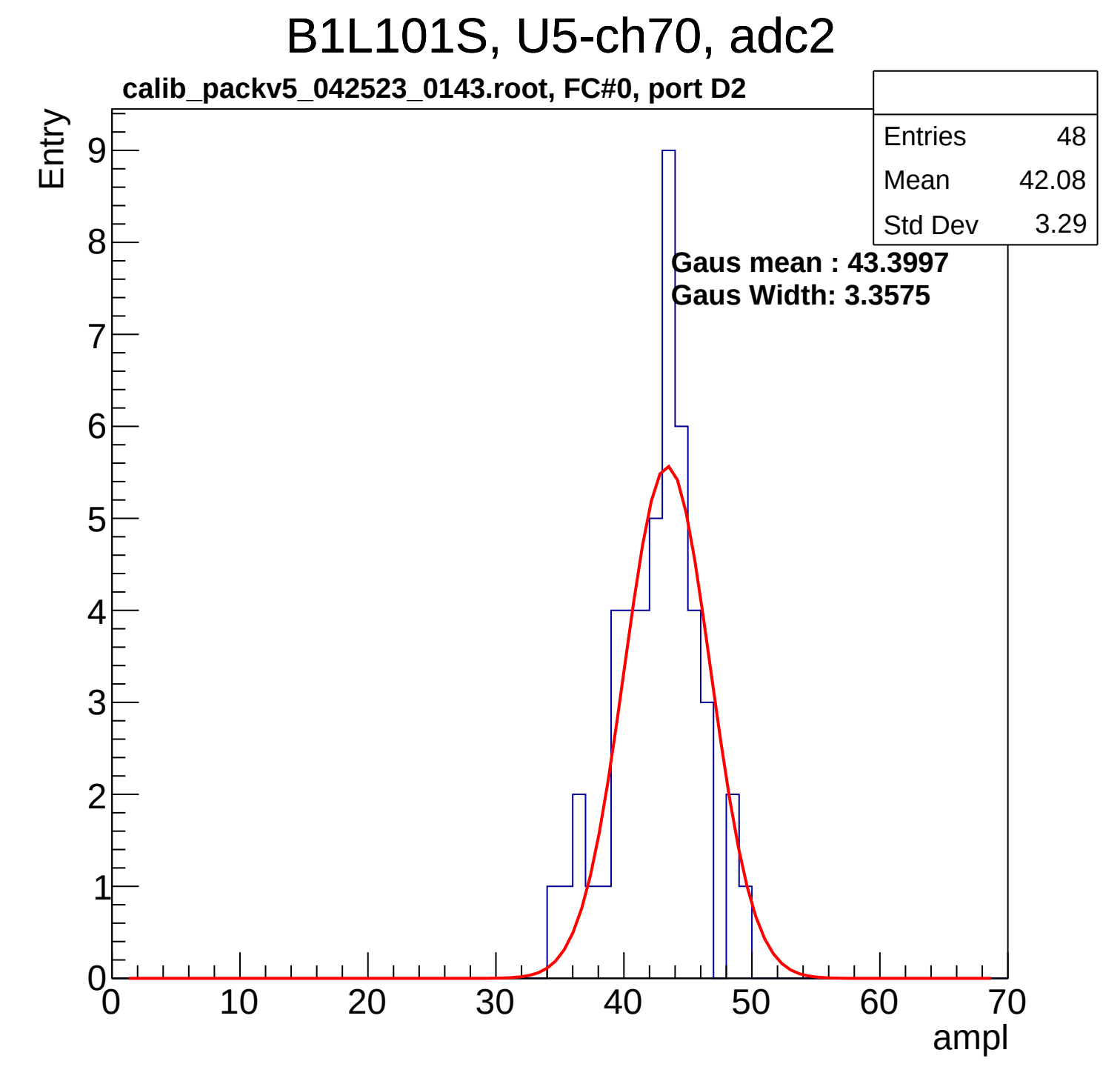
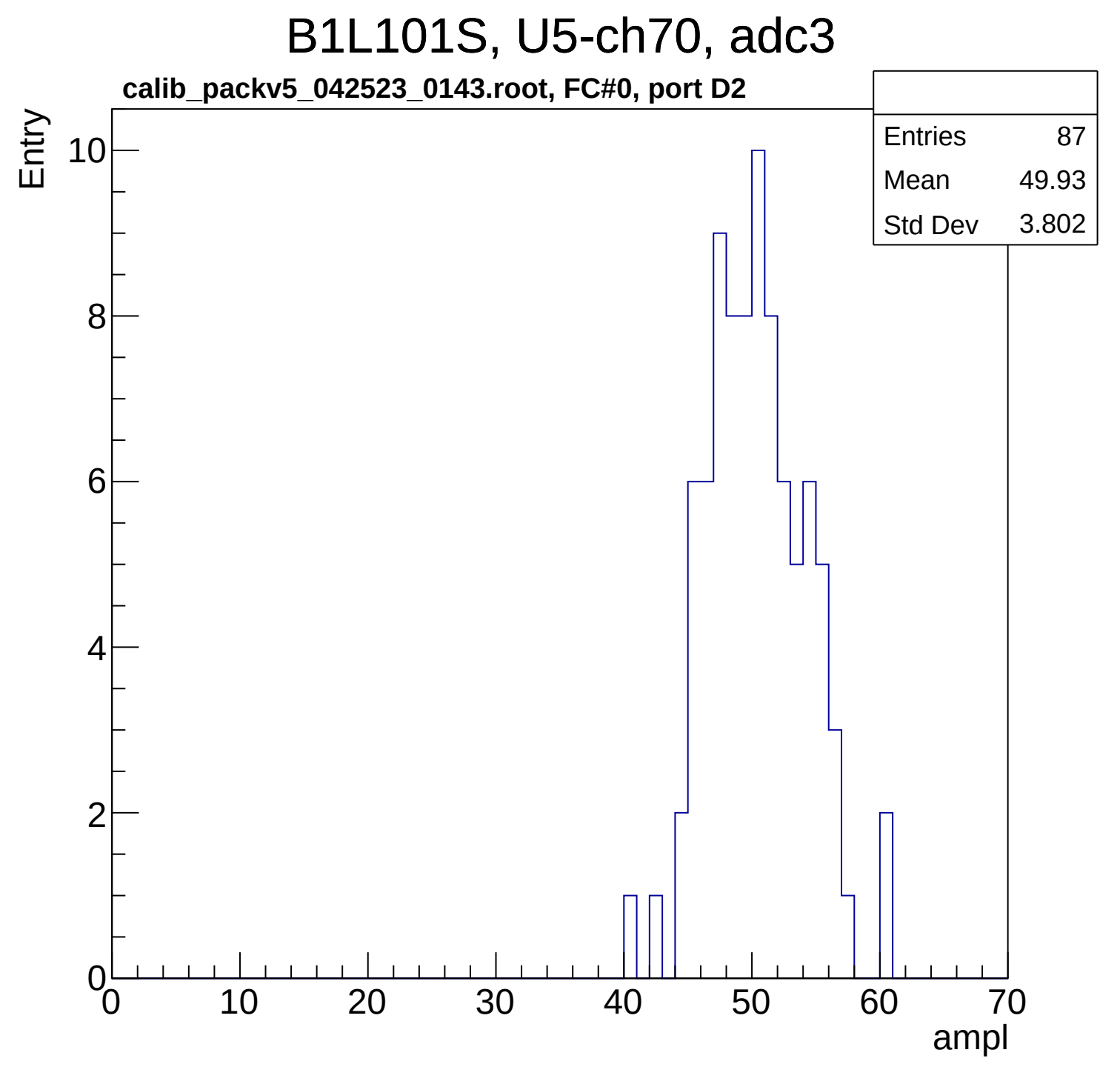
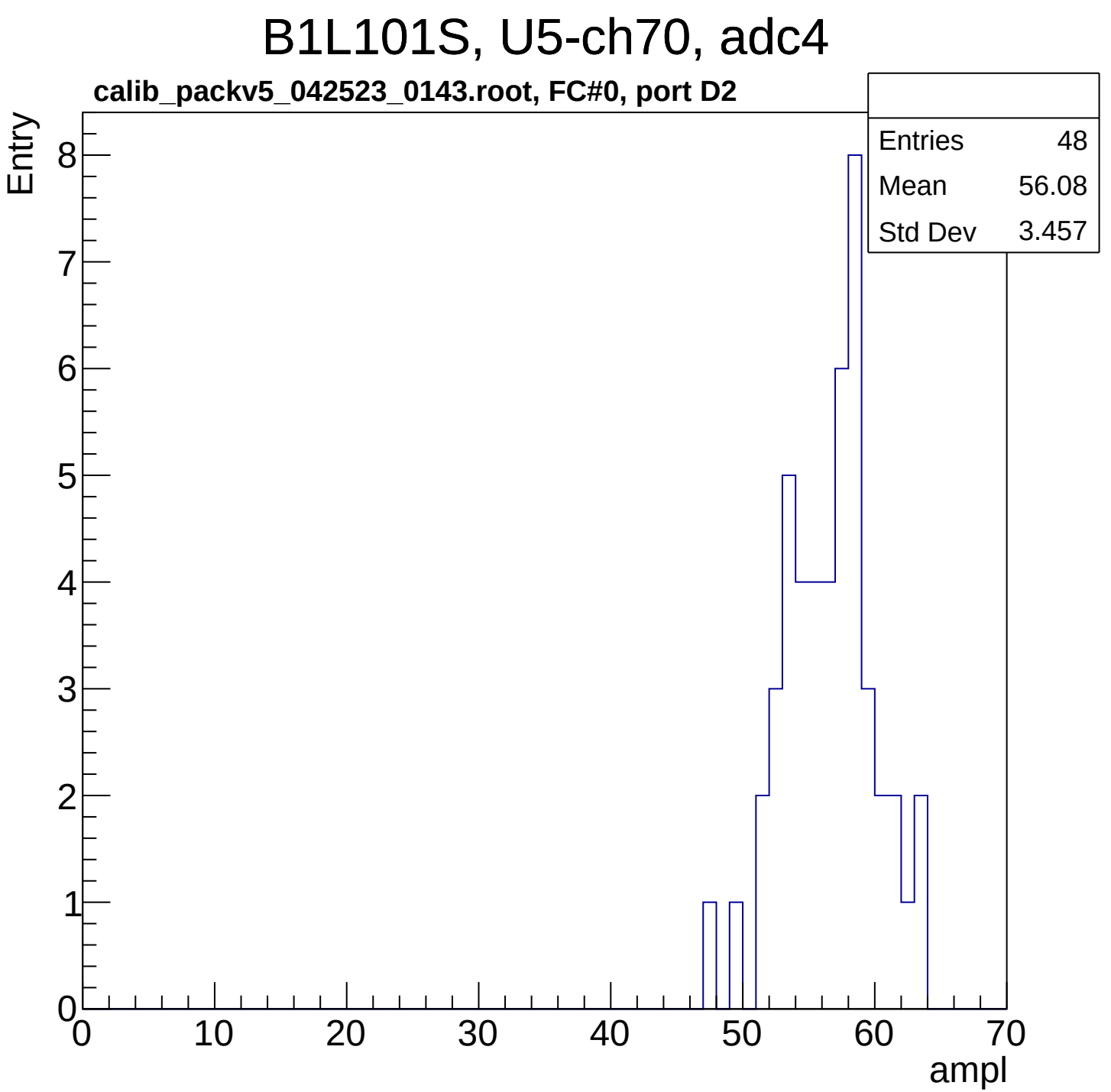
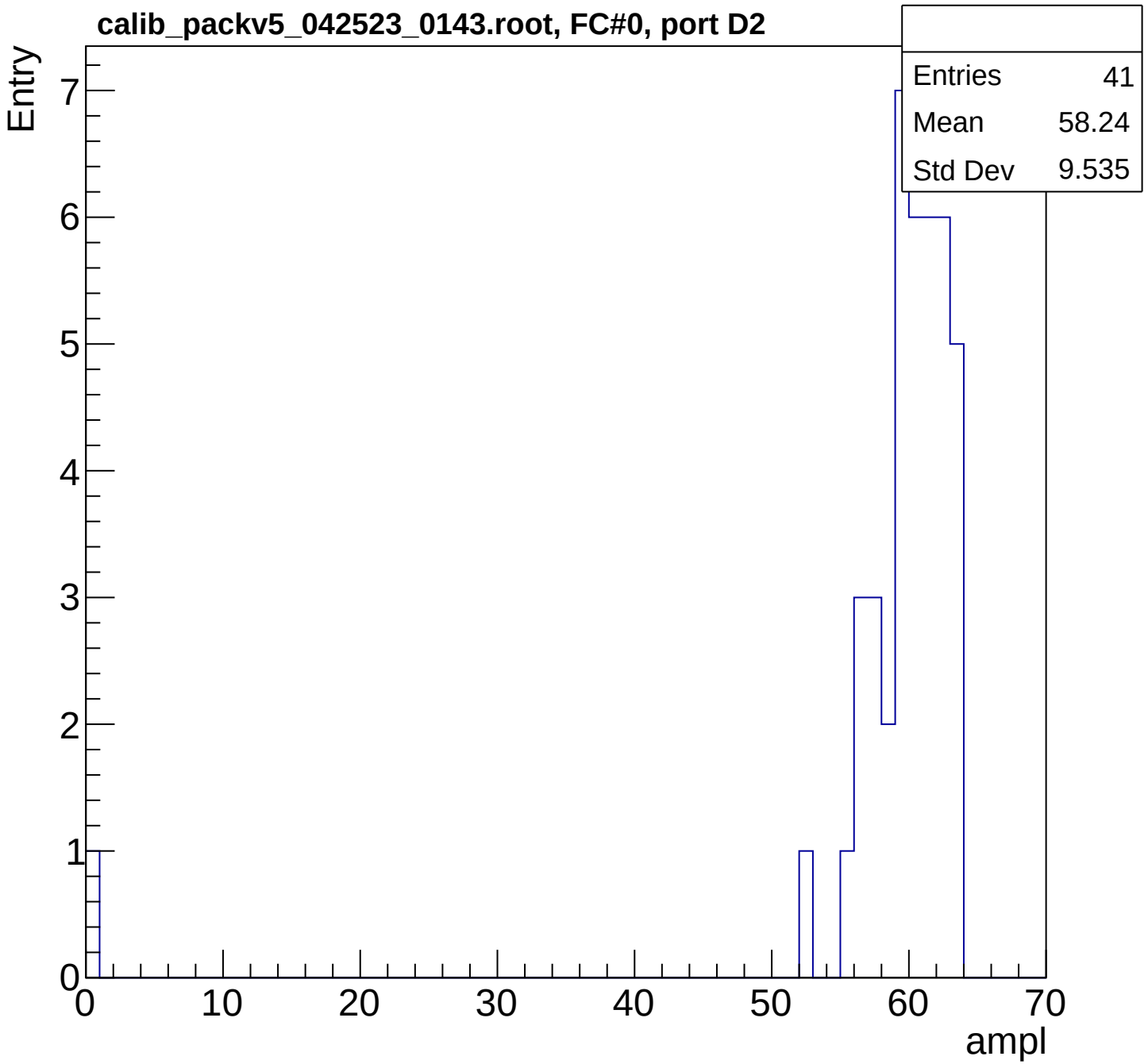
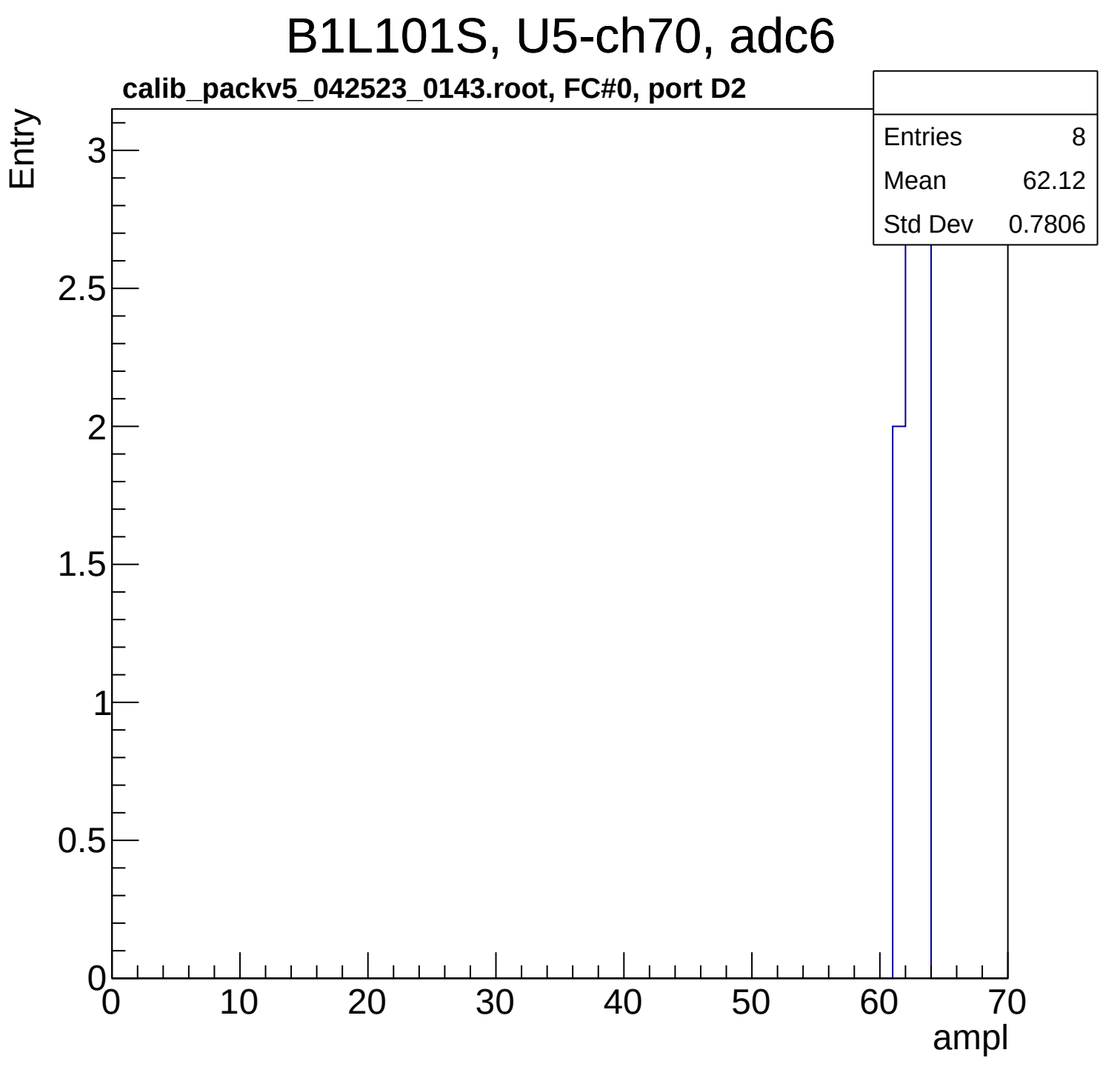

B1L101S, U5-ch70, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 42.08
Std Dev 3.29
Gaus mean : 43.3997
Gaus Width: 3.3575
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch70, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 87
Mean 49.93
Std Dev 3.802
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch70, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 56.08
Std Dev 3.457
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch70, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 41
Mean 58.24
Std Dev 9.535
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch70, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 62.12
Std Dev 0.7806
Entry
ampl
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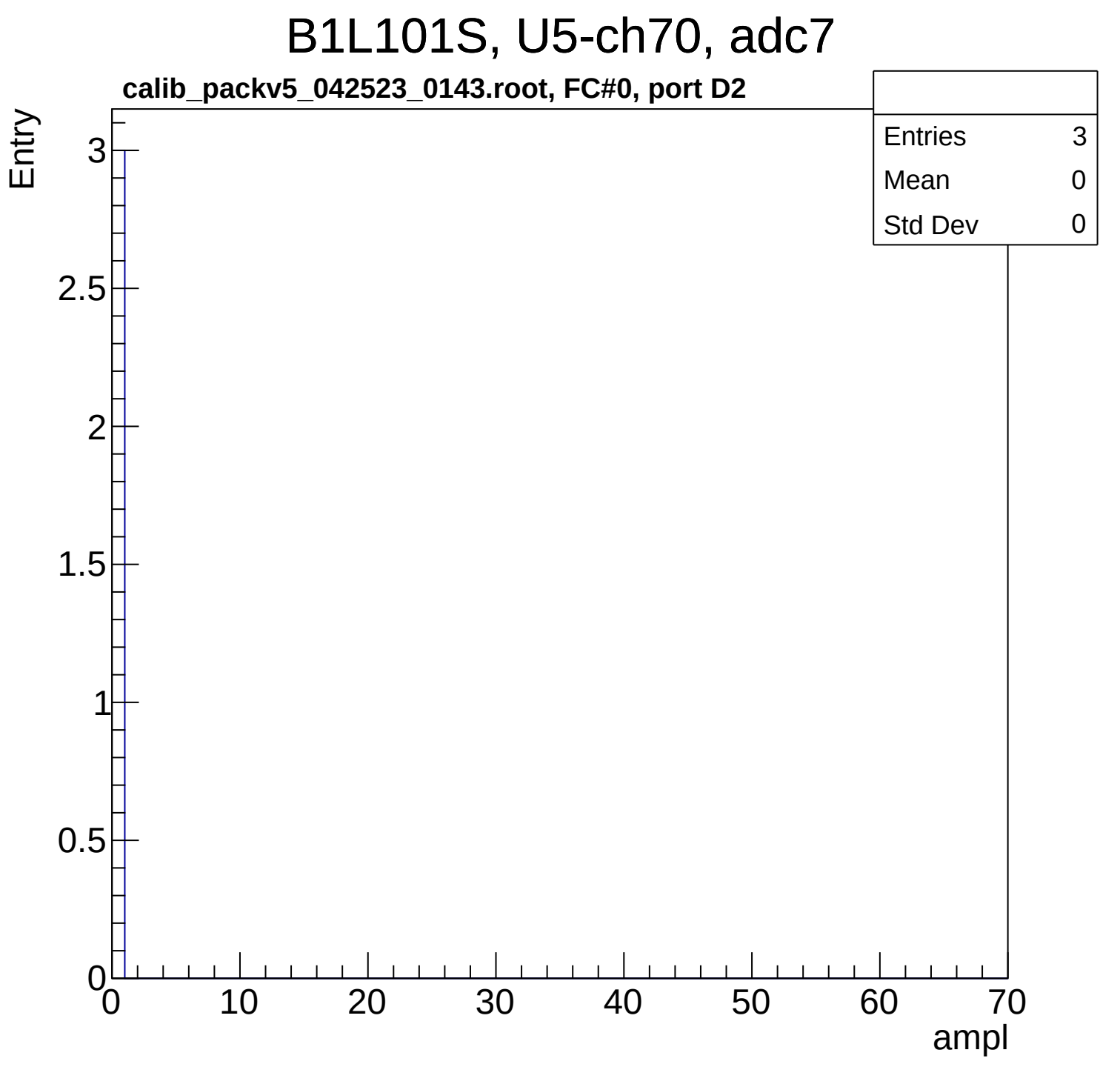
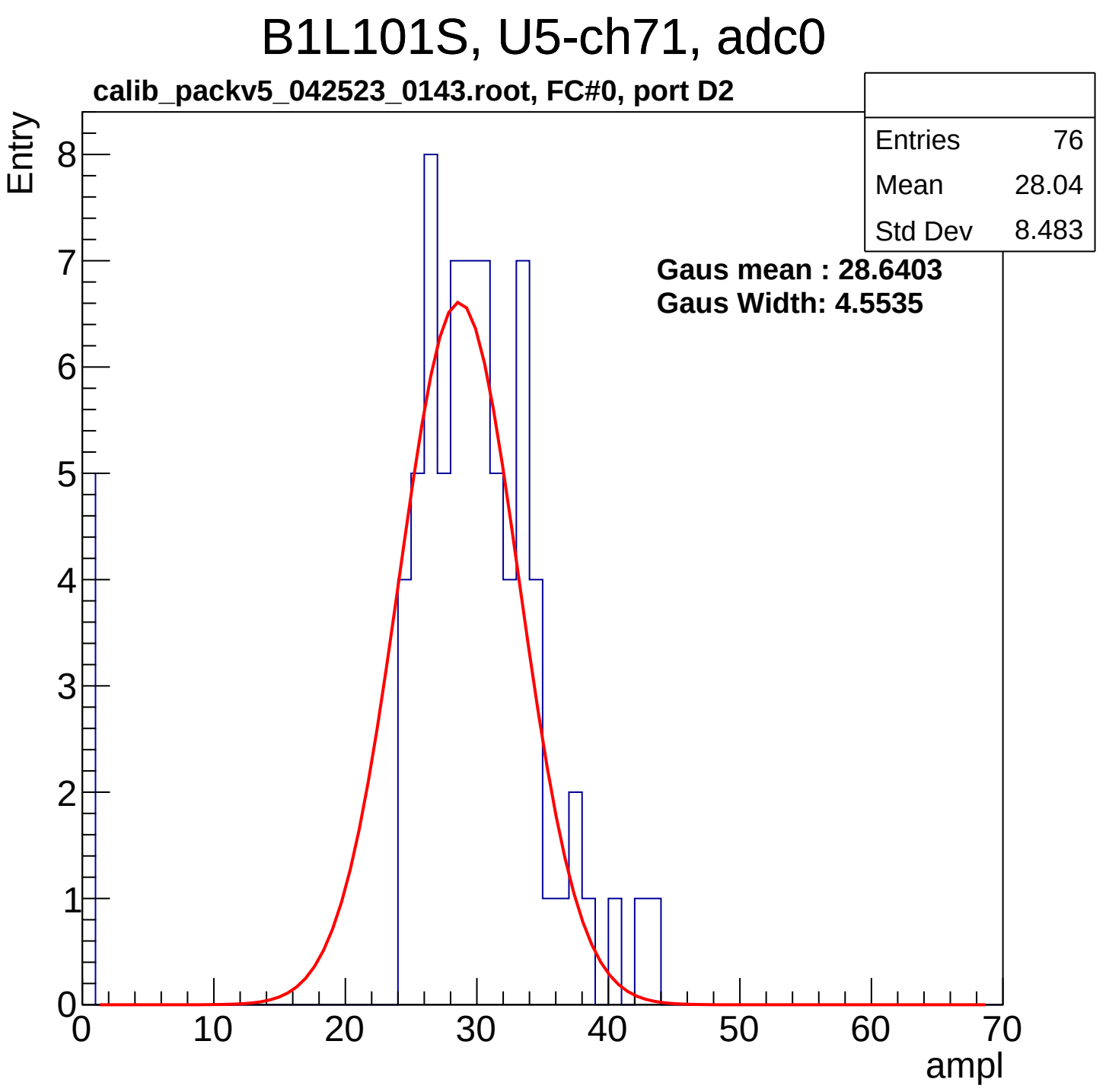
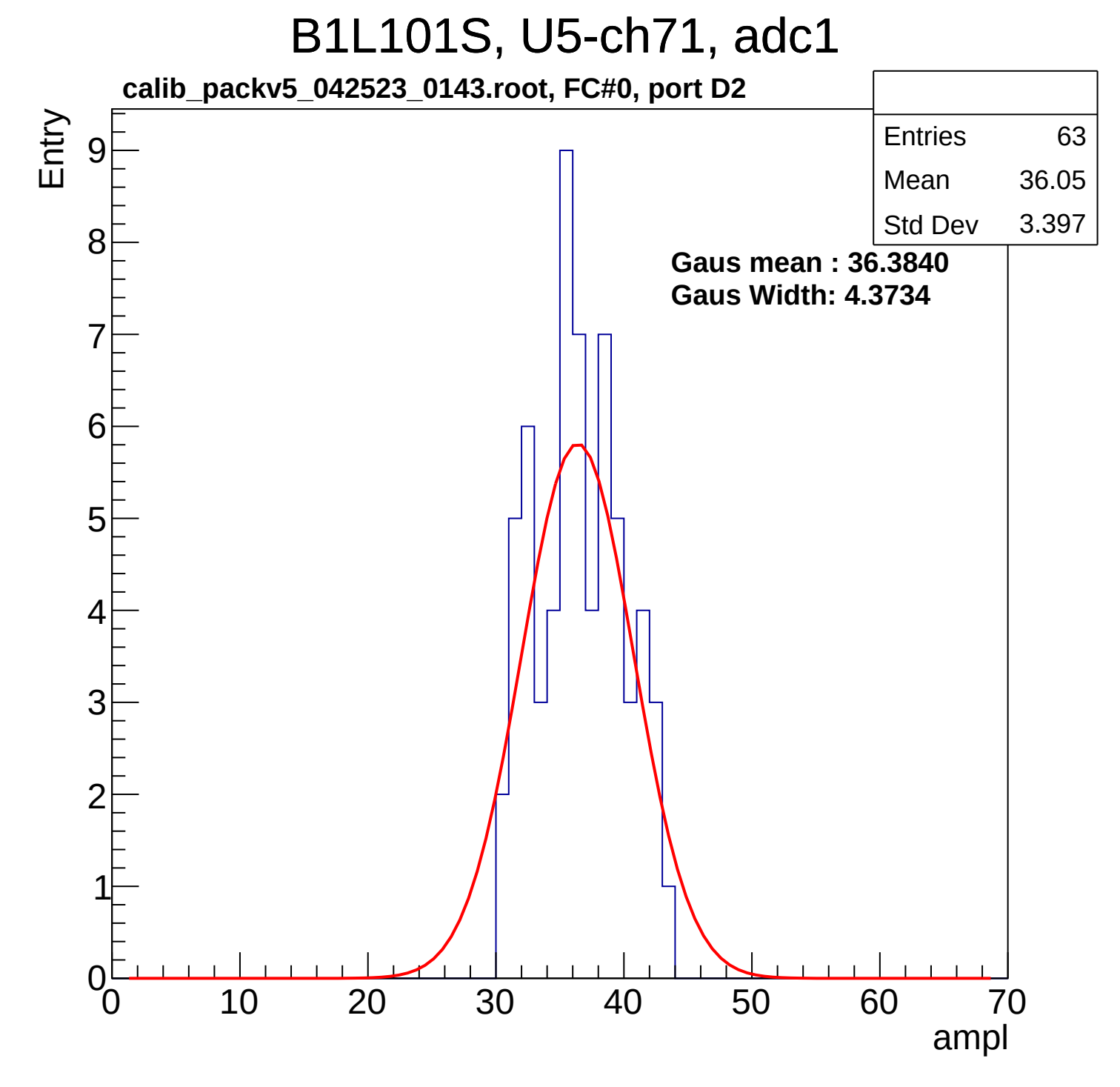
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U5-ch70, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 0
Std Dev 0
Entry
3
2.5
2
1.5
1
0.5
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch71, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 28.04
Std Dev 8.483
Gaus mean : 28.6403
Gaus Width: 4.5535
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch71, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 36.05
Std Dev 3.397
Gaus mean : 36.3840
Gaus Width: 4.3734
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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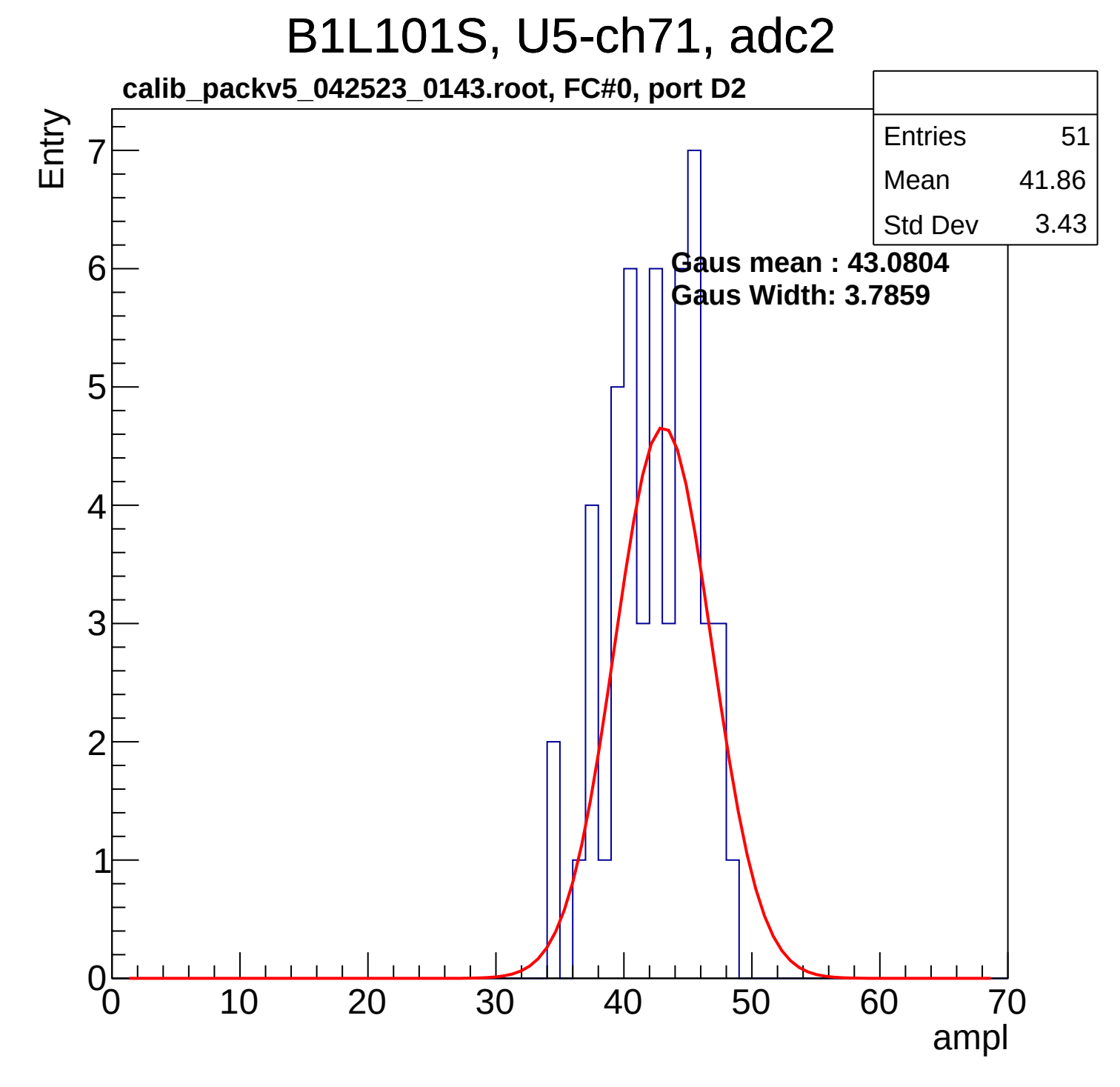
B1L101S, U5-ch71, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 41.86
Std Dev 3.43
Gaus mean : 43.0804
Gaus Width: 3.7859
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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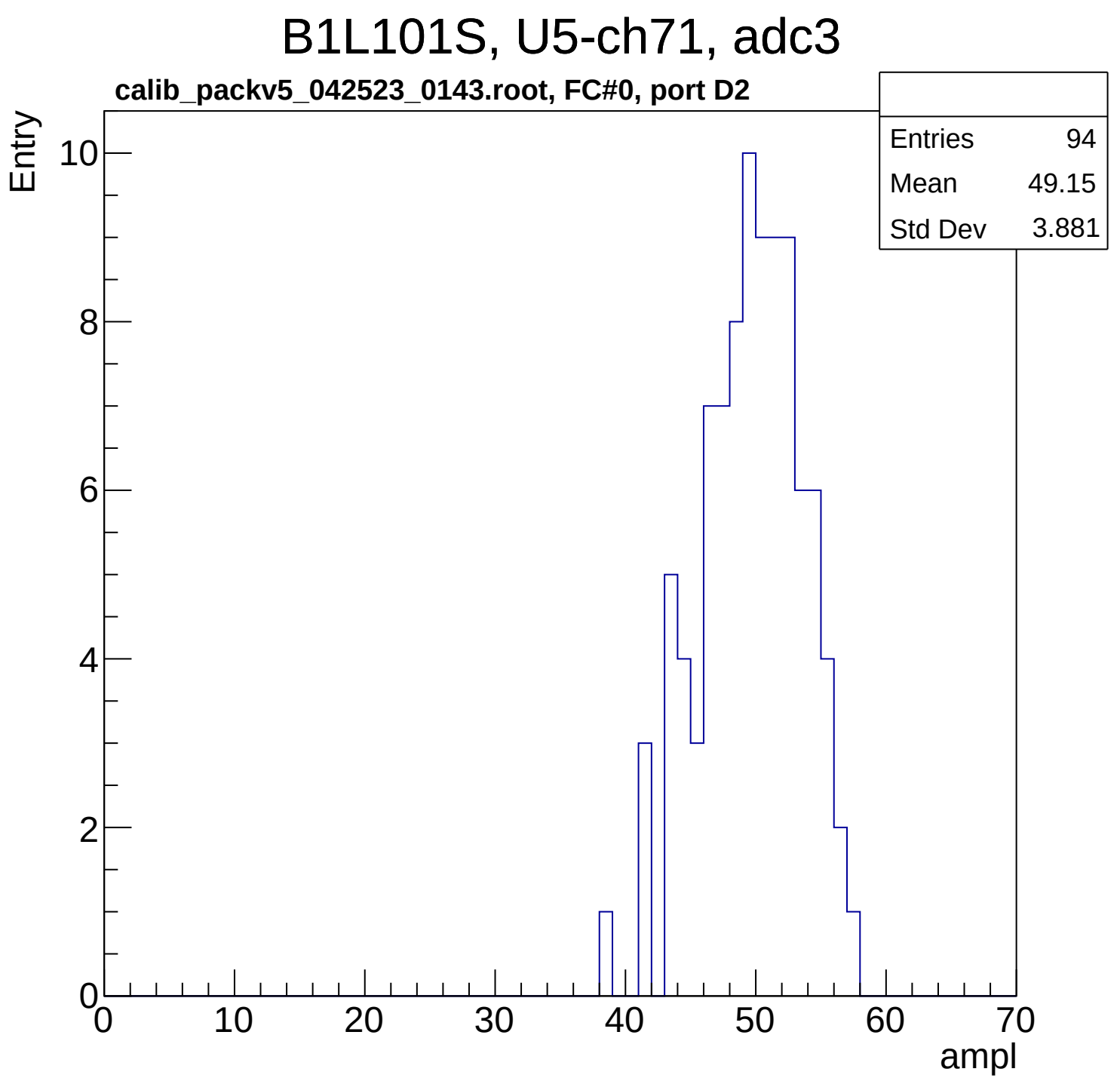
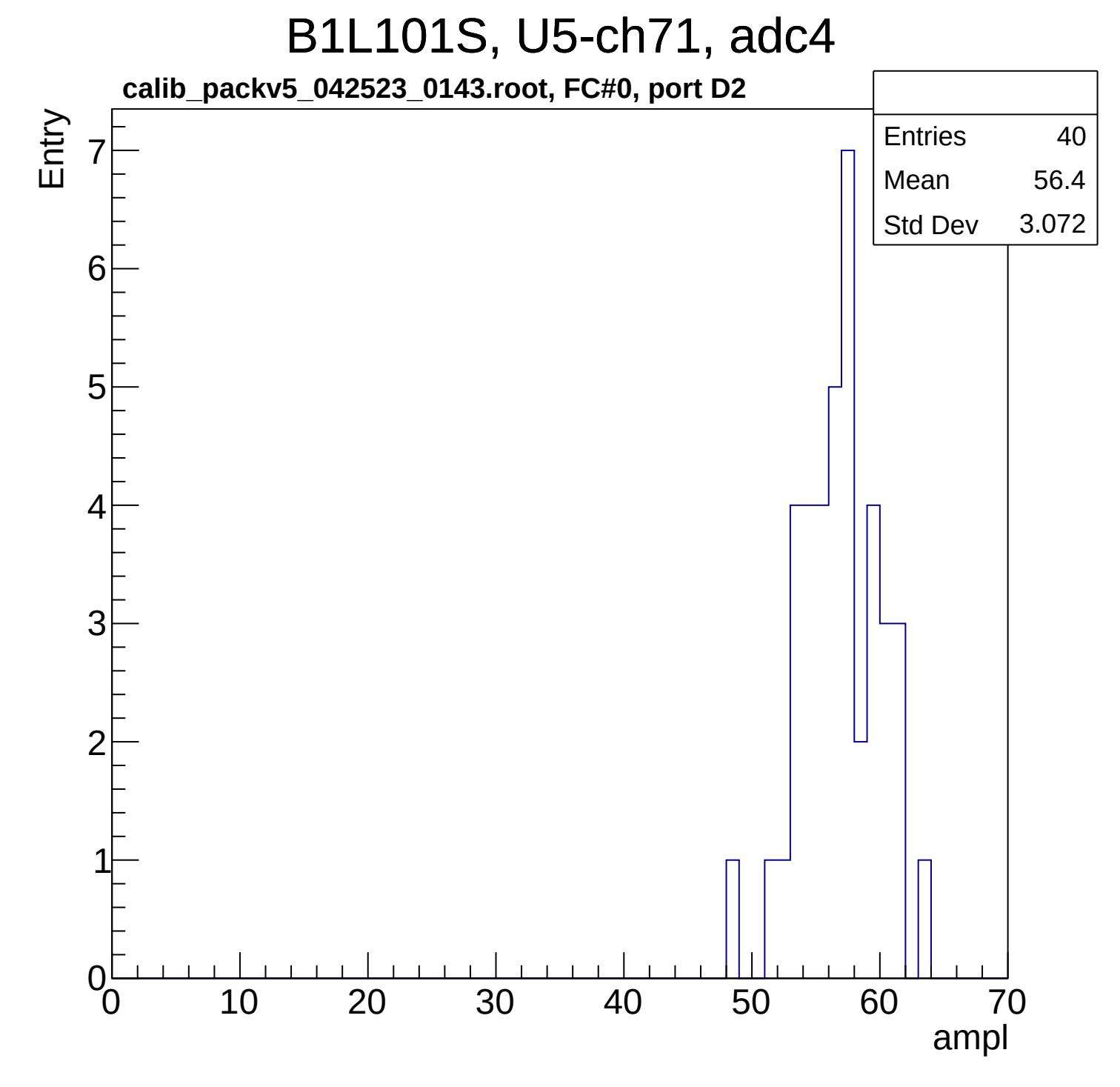

B1L101S, U5-ch71, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 94
Mean 49.15
Std Dev 3.881
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch71, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 40
Mean 56.4
Std Dev 3.072
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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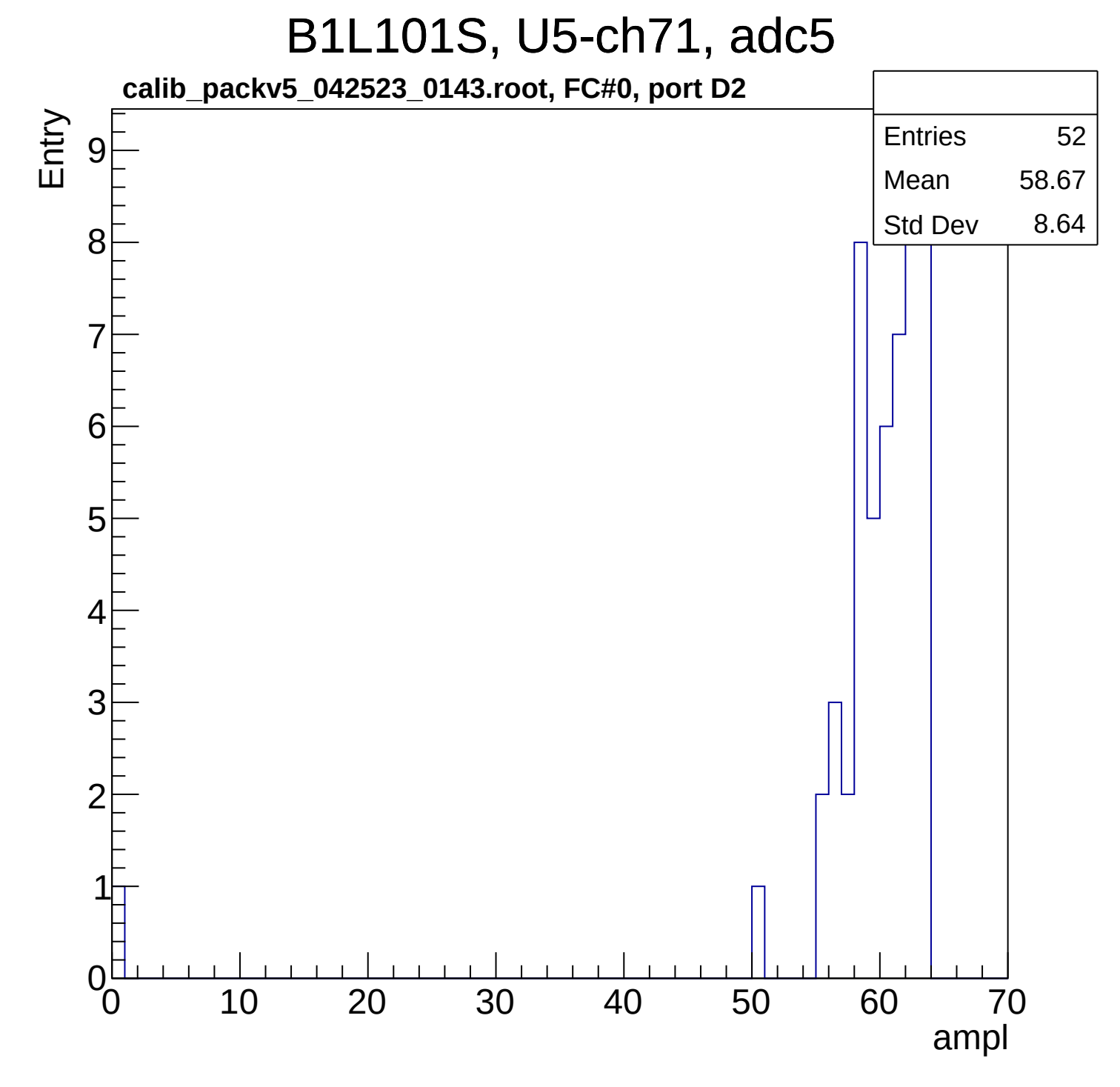
B1L101S, U5-ch71, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 58.67
Std Dev 8.64
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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60
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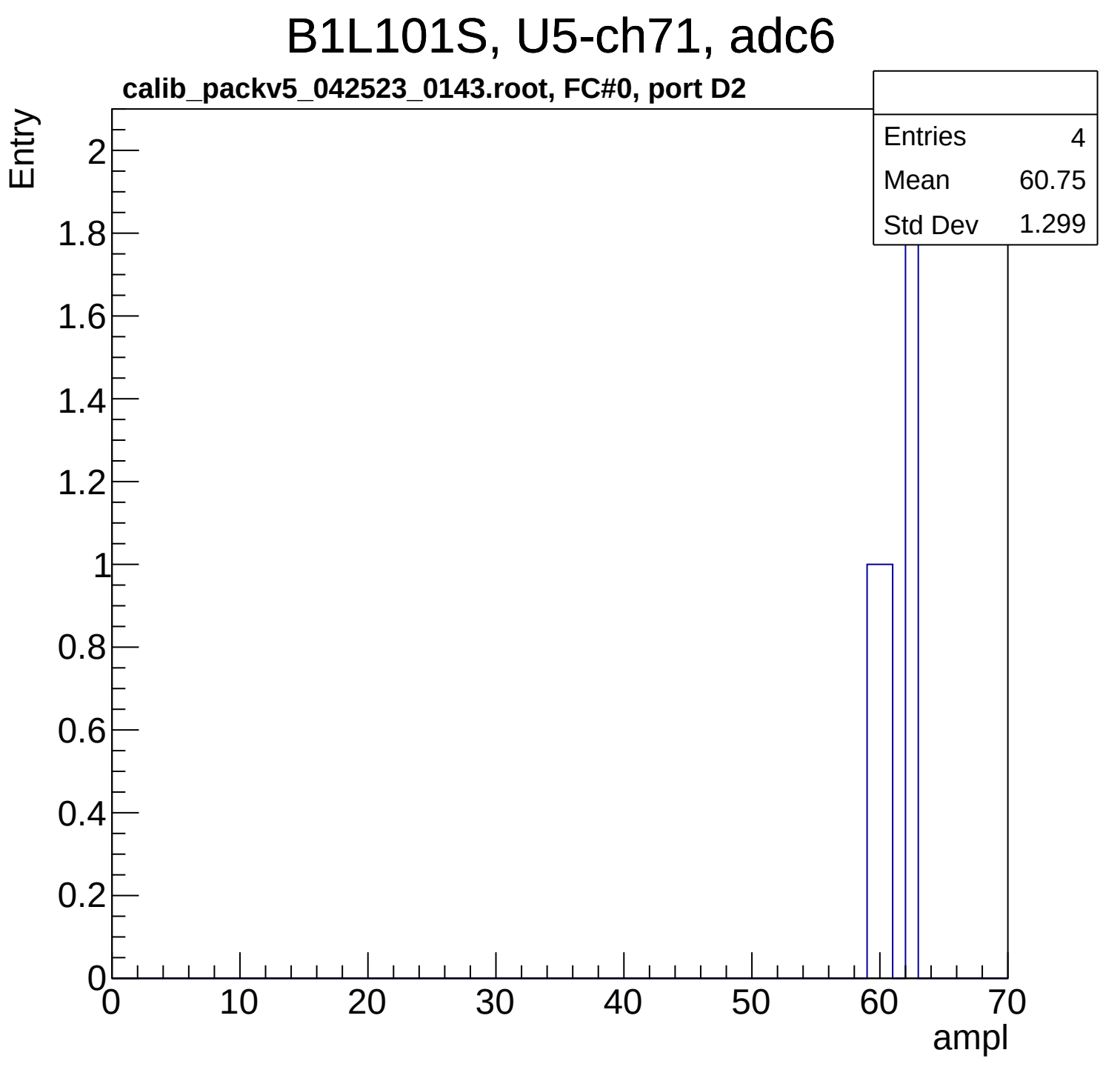
B1L101S, U5-ch71, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 60.75
Std Dev 1.299
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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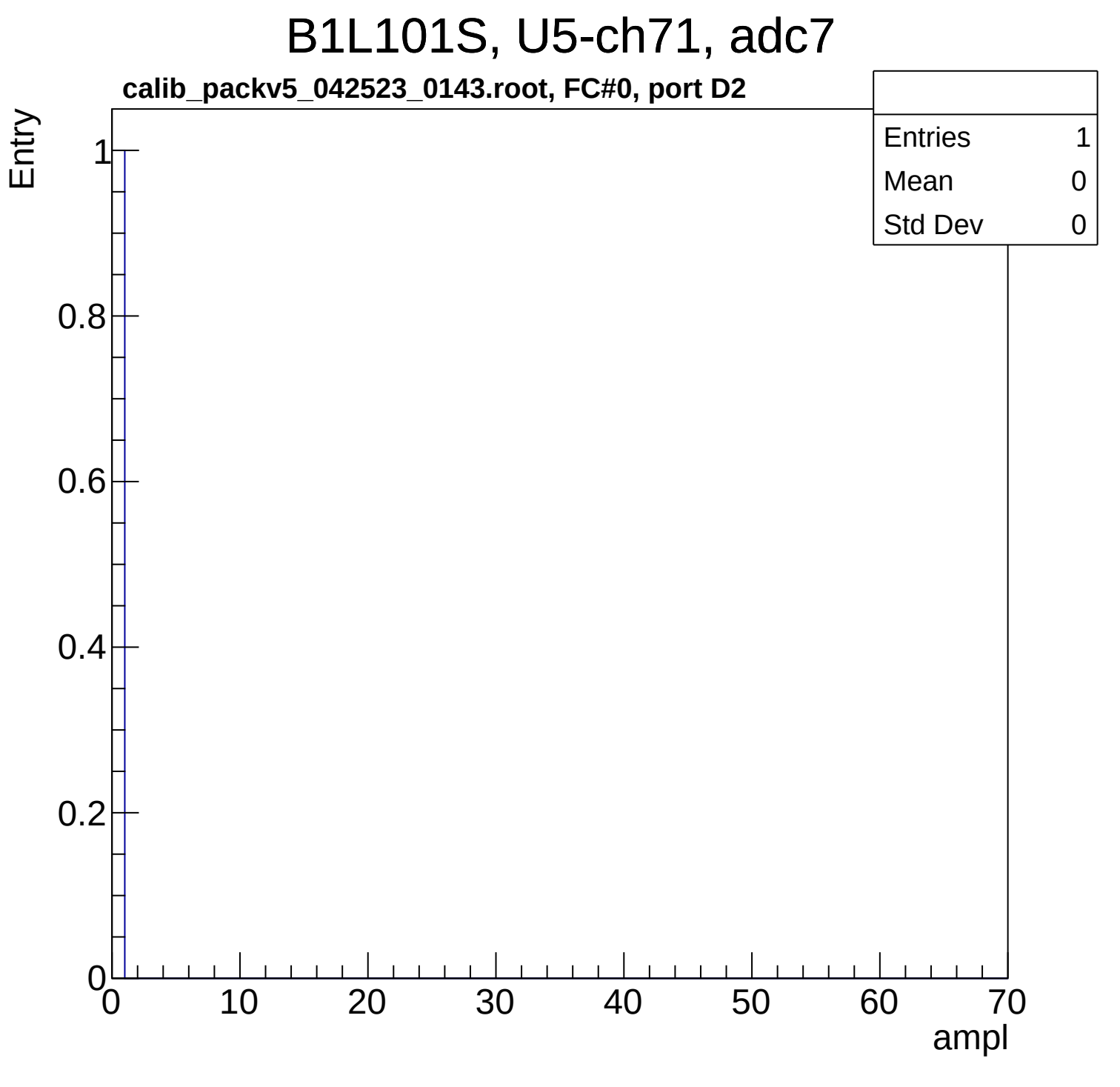
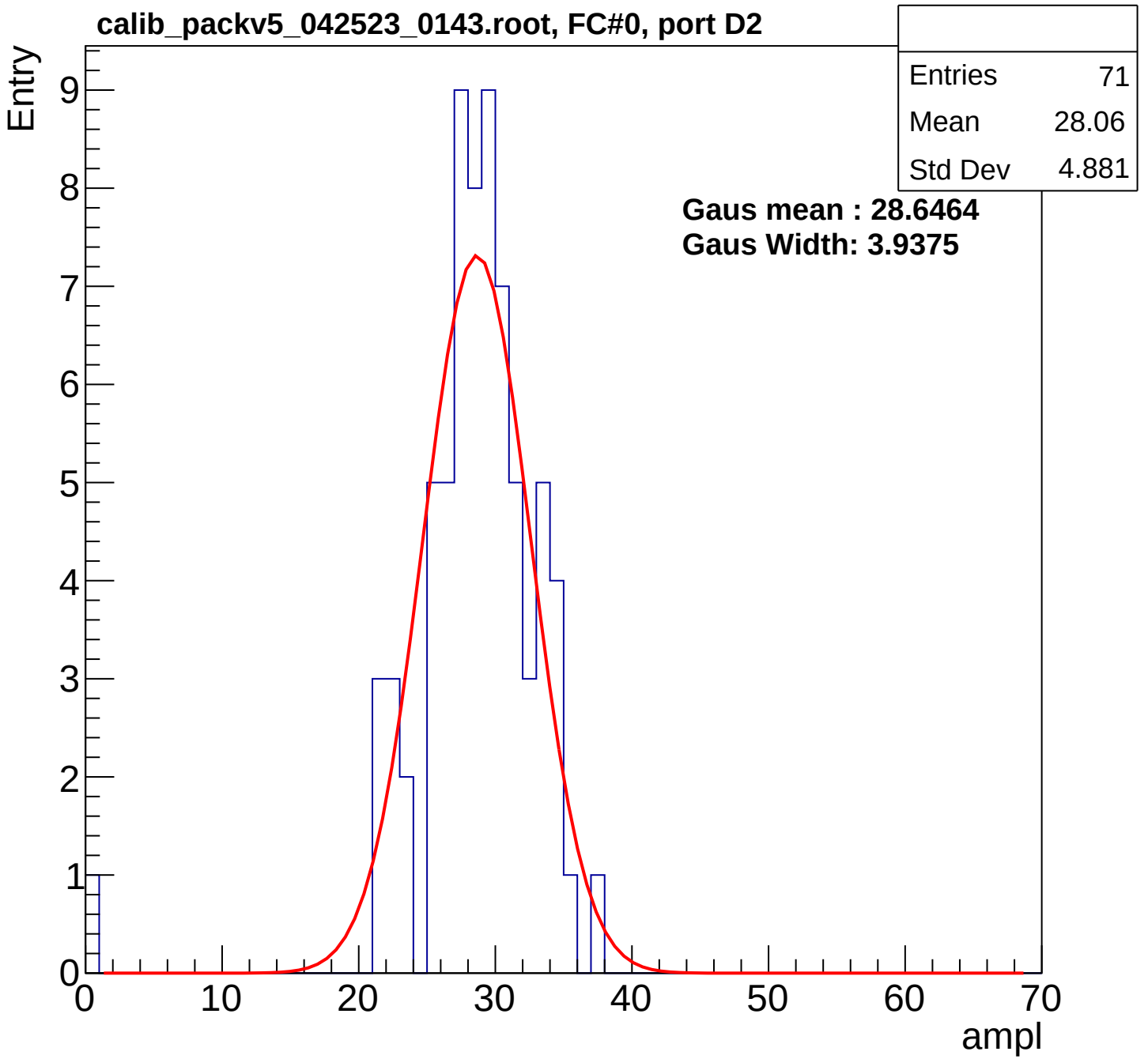
50
60
70


B1L101S, U5-ch71, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch72, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 28.06
Std Dev 4.881
Gaus mean : 28.6464
Gaus Width: 3.9375
Entry
ampl
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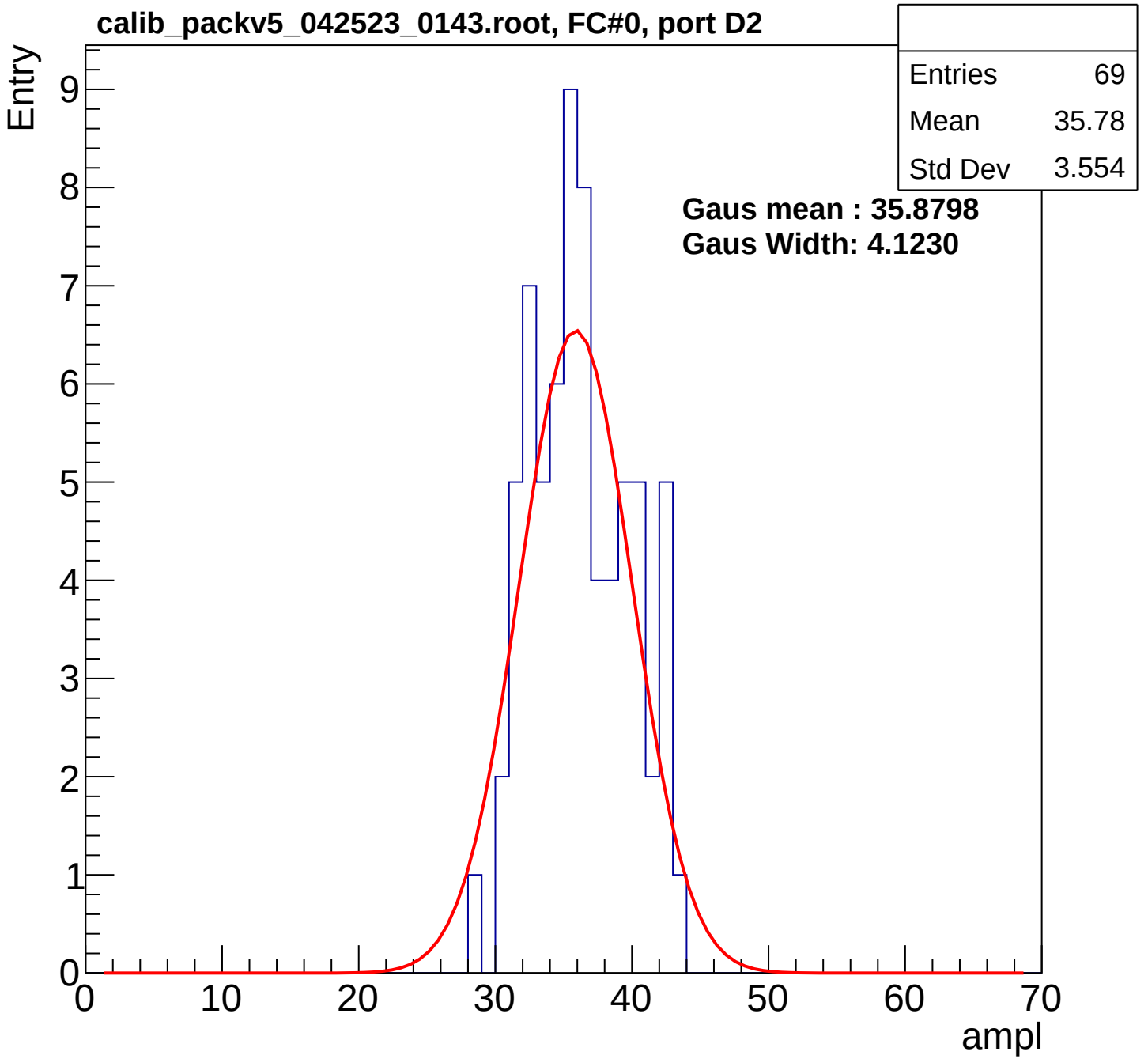
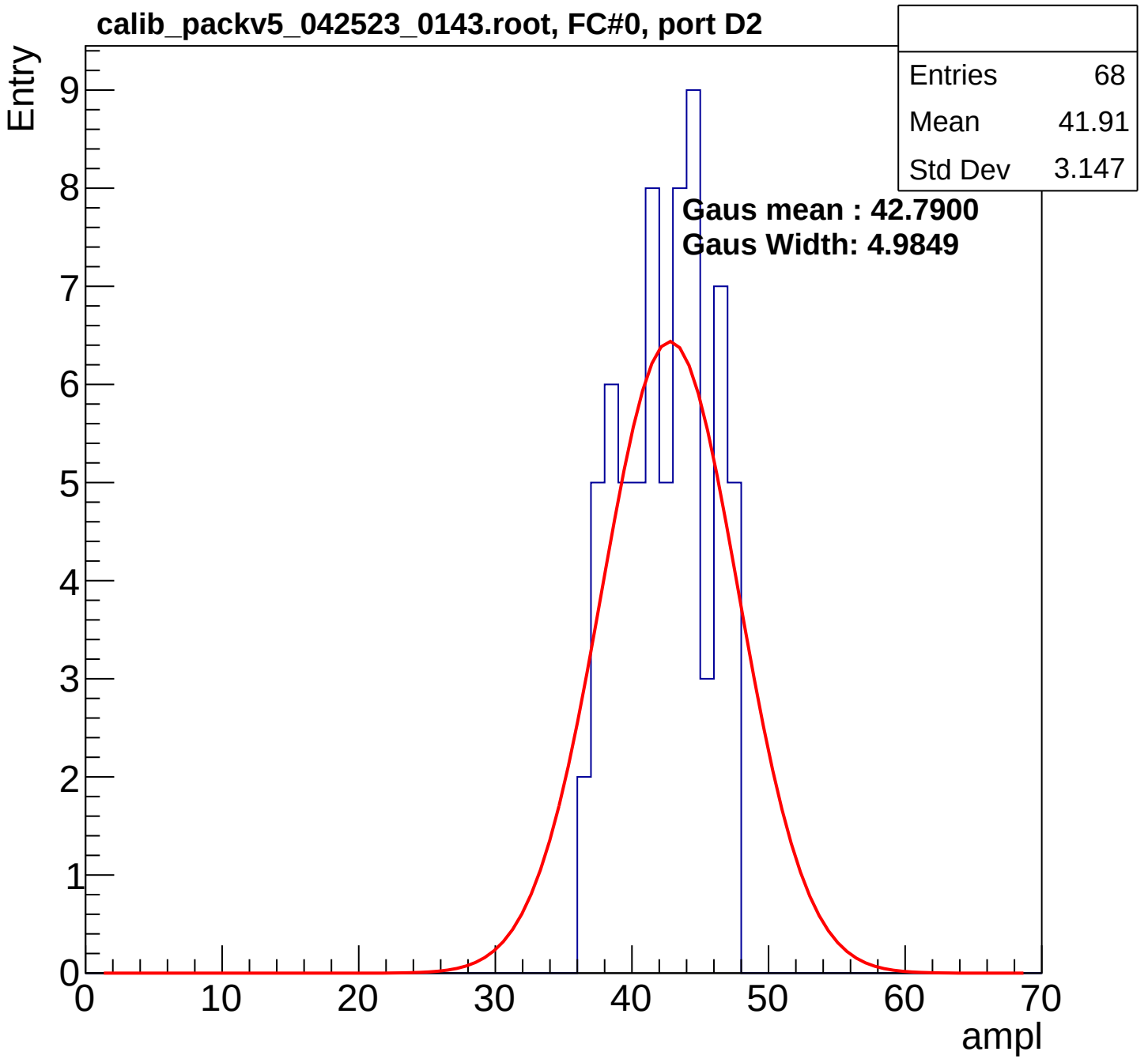
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch72, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 35.78
Std Dev 3.554
Gaus mean : 35.8798
Gaus Width: 4.1230
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch72, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 41.91
Std Dev 3.147
Gaus mean : 42.7900
Gaus Width: 4.9849
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
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60
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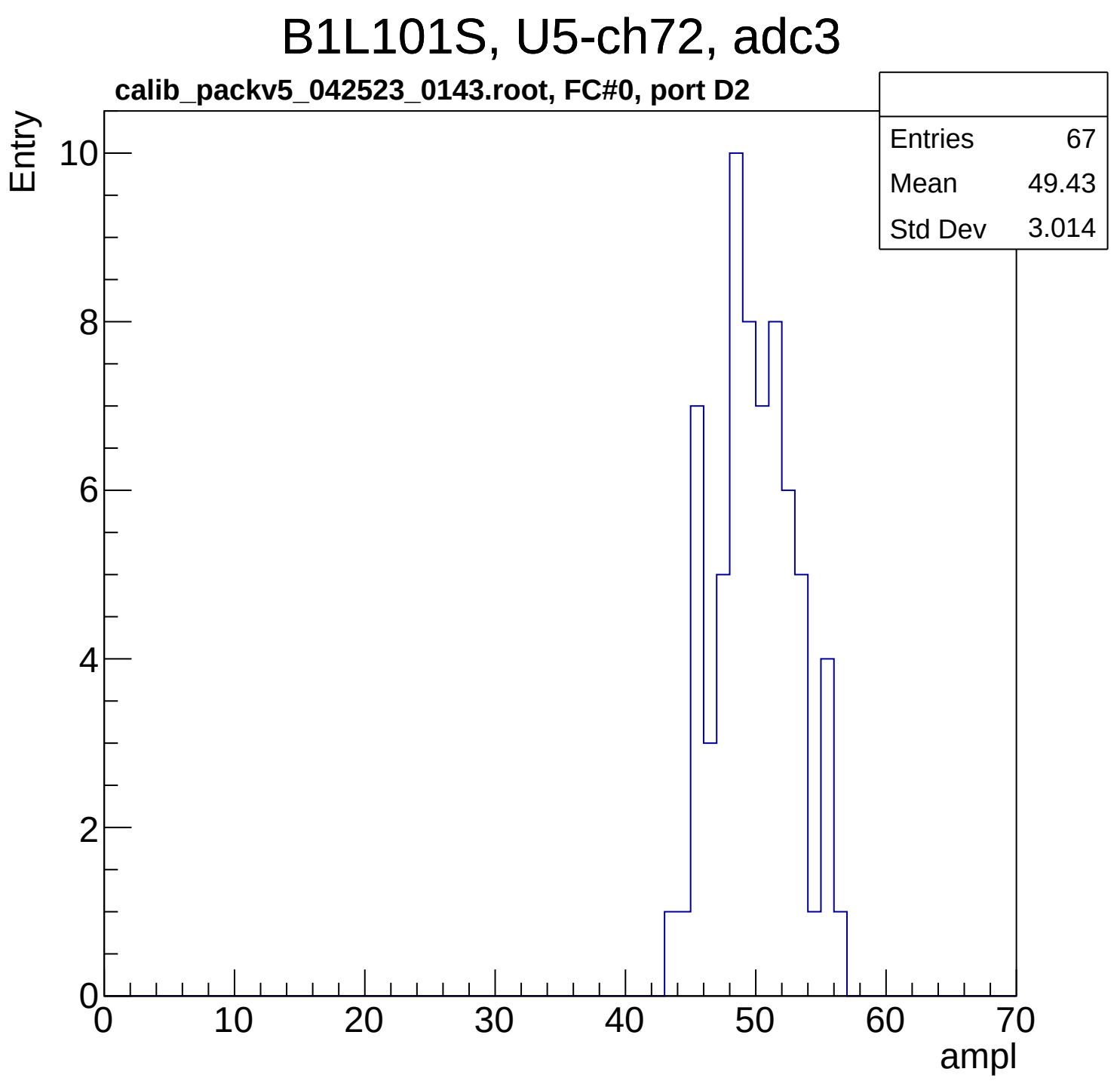
B1L101S, U5-ch72, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 49.43
Std Dev 3.014
Entry
ampl
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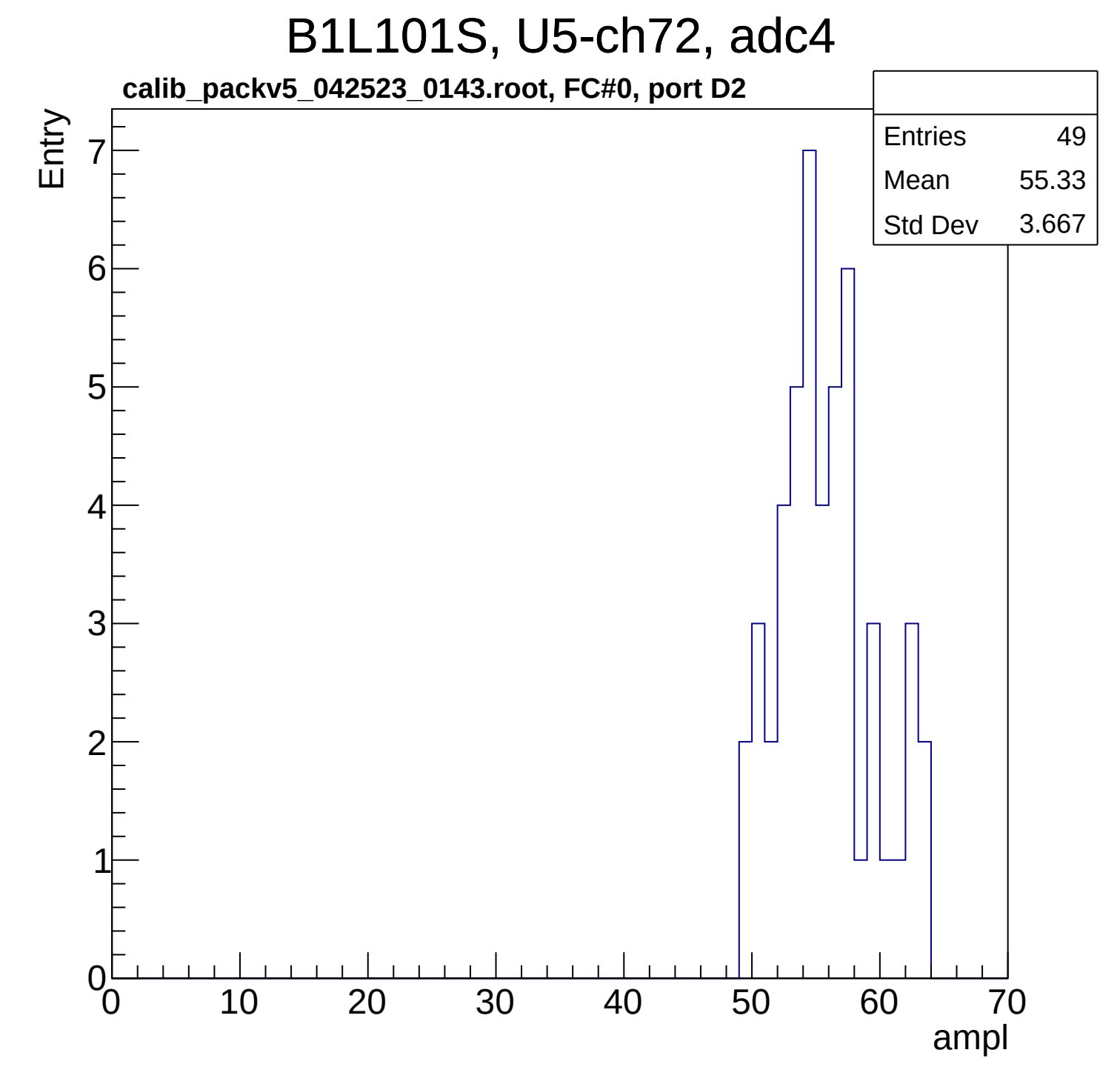
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch72, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 55.33
Std Dev 3.667
Entry
ampl
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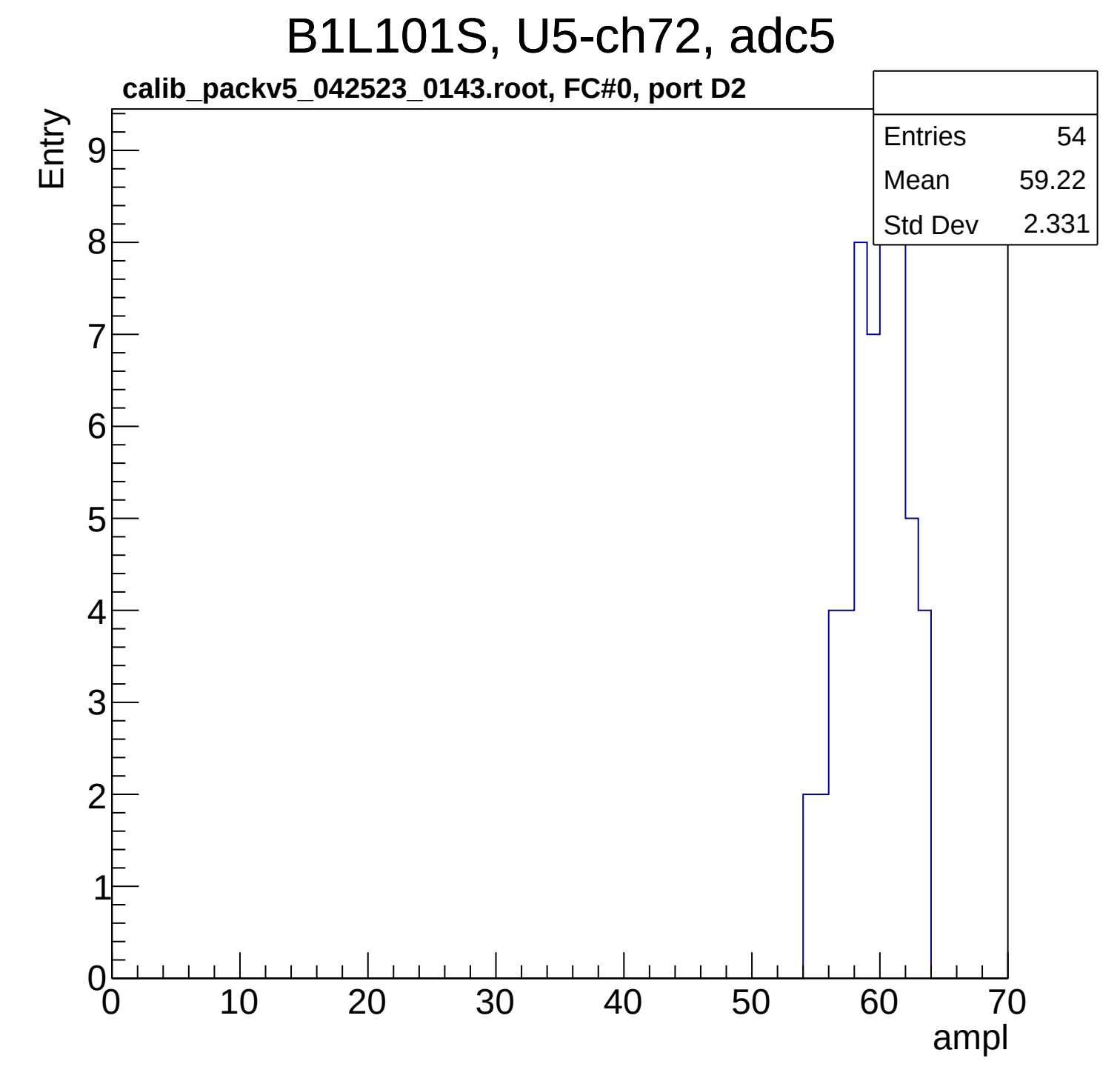
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch72, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 59.22
Std Dev 2.331
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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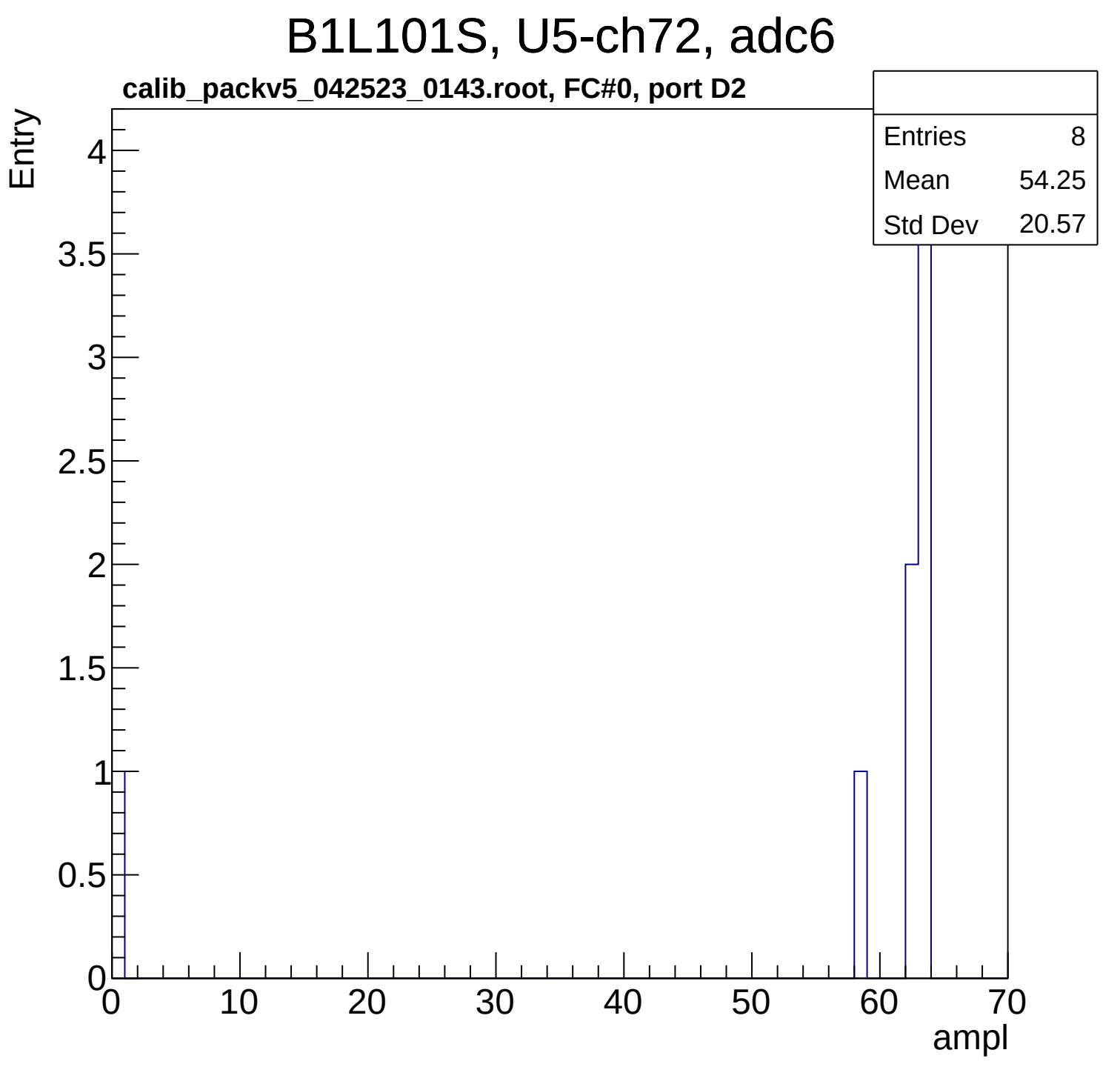
B1L101S, U5-ch72, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 54.25
Std Dev 20.57
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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20
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60
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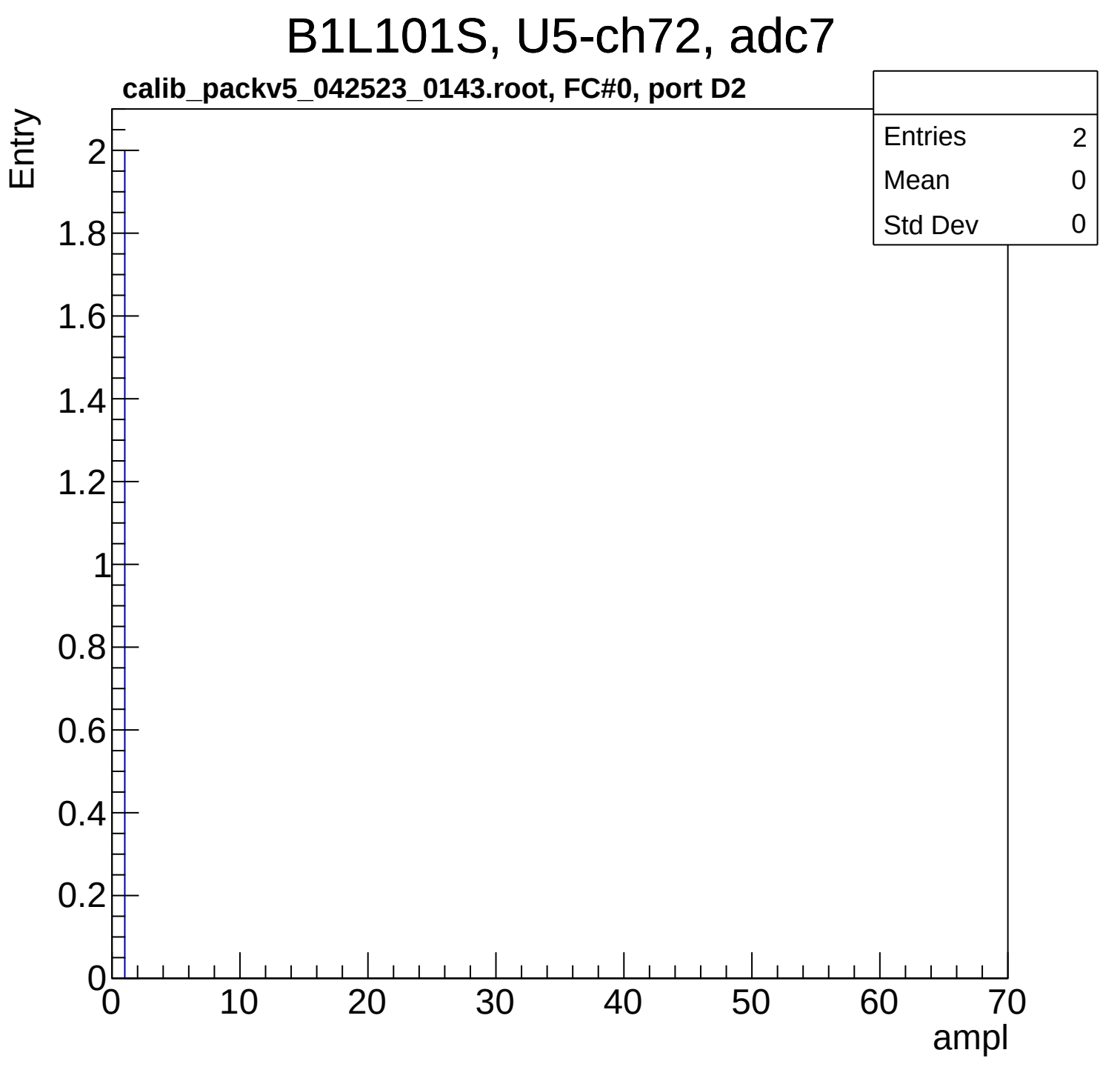
B1L101S, U5-ch72, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
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1.2
1.4
1.6
1.8
2
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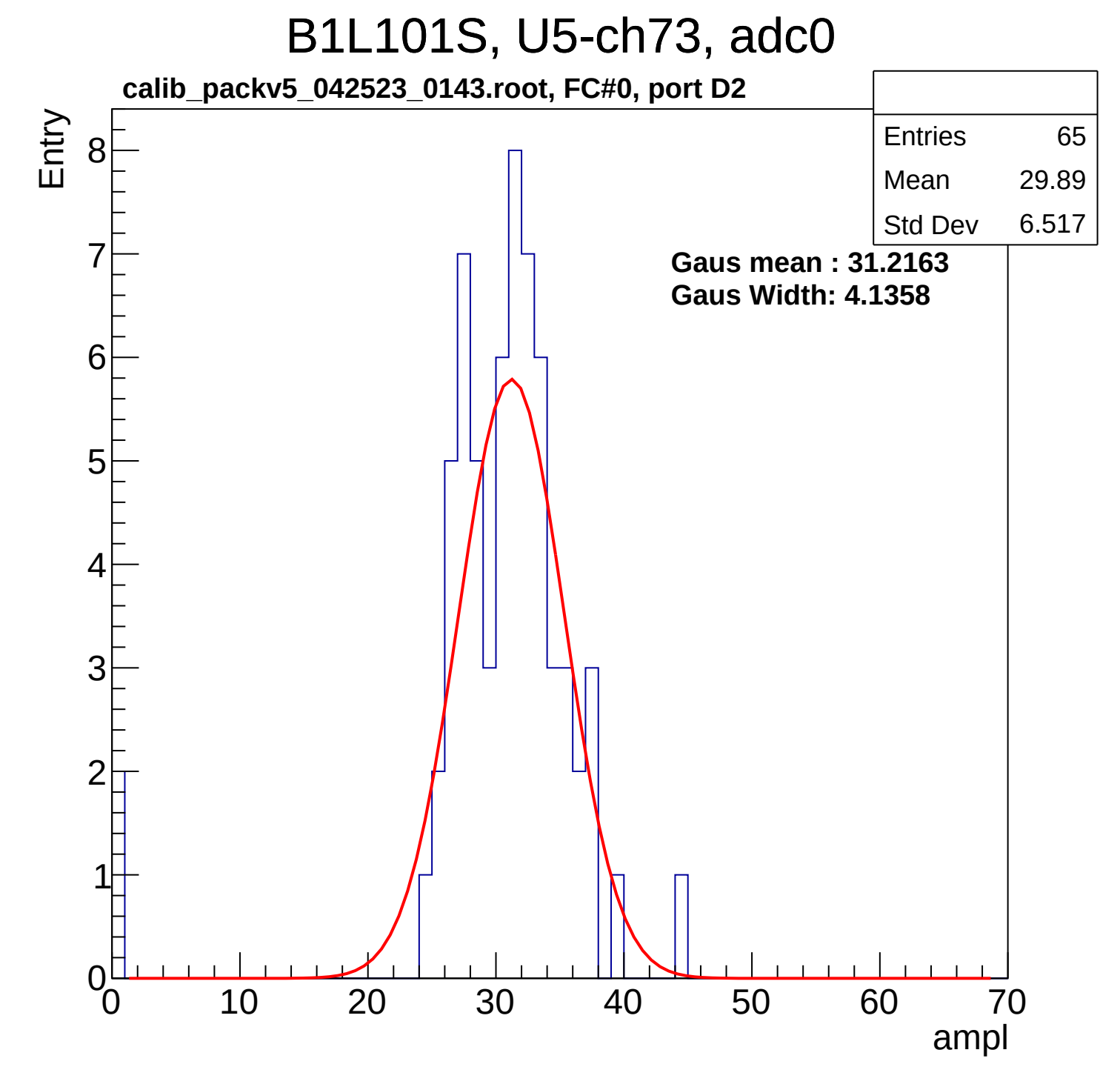
B1L101S, U5-ch73, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 29.89
Std Dev 6.517
Gaus mean : 31.2163
Gaus Width: 4.1358
Entry
ampl
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1
2
3
4
5
6
7
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0
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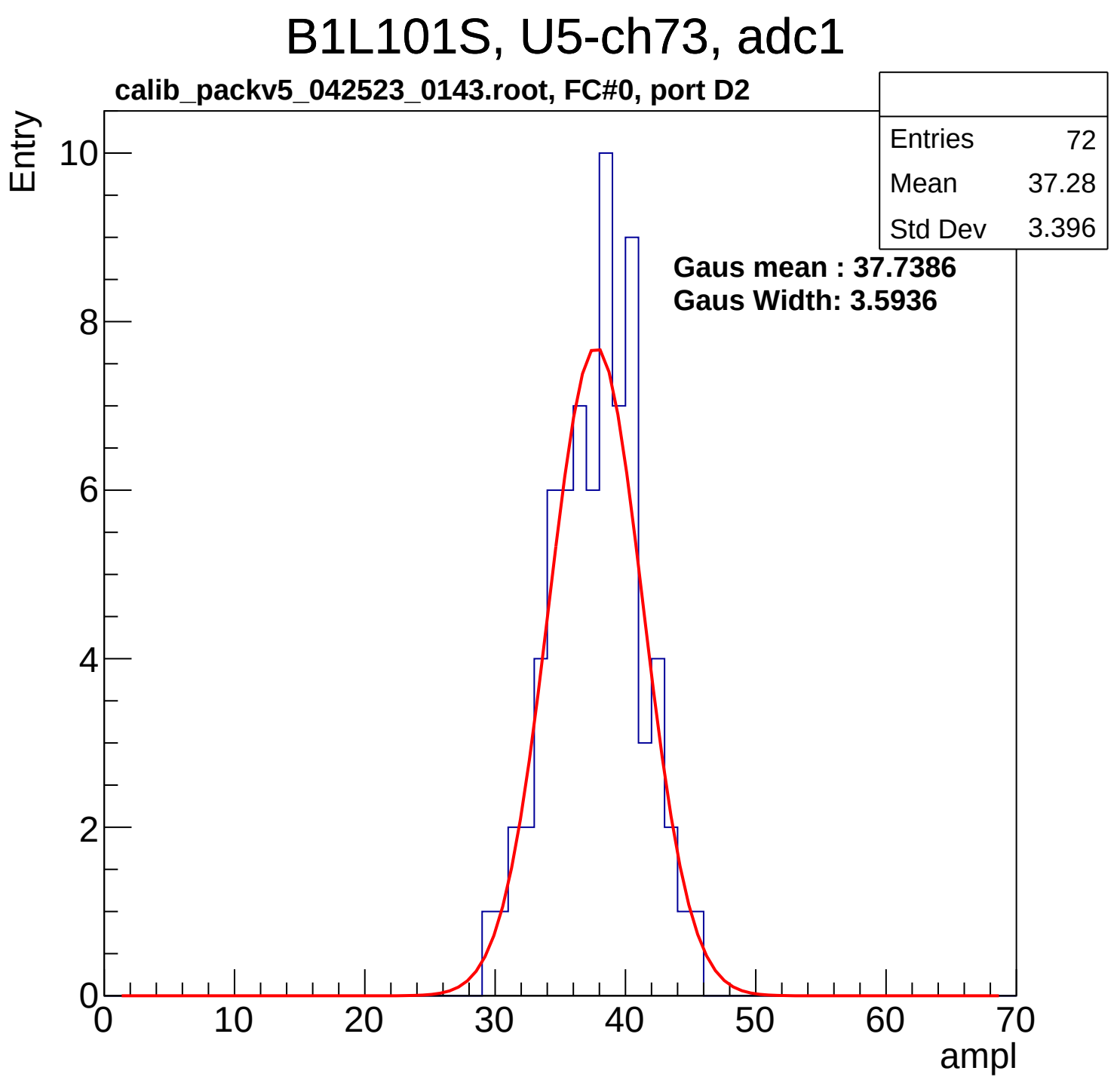
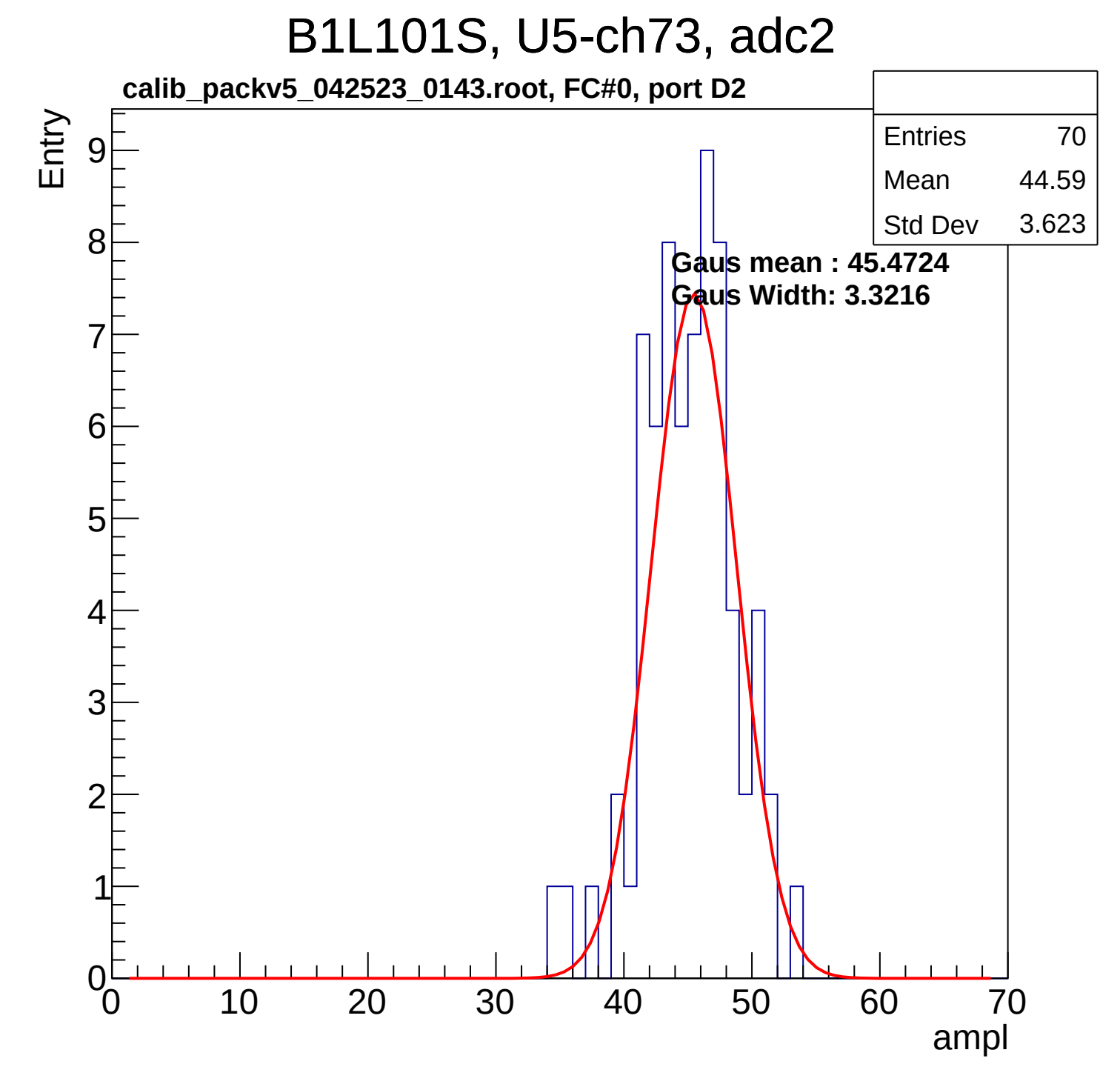
40
50
60
70


B1L101S, U5-ch73, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 37.28
Std Dev 3.396
Gaus mean : 37.7386
Gaus Width: 3.5936
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch73, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 44.59
Std Dev 3.623
Gaus mean : 45.4724
Gaus Width: 3.3216
Entry
ampl
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2
3
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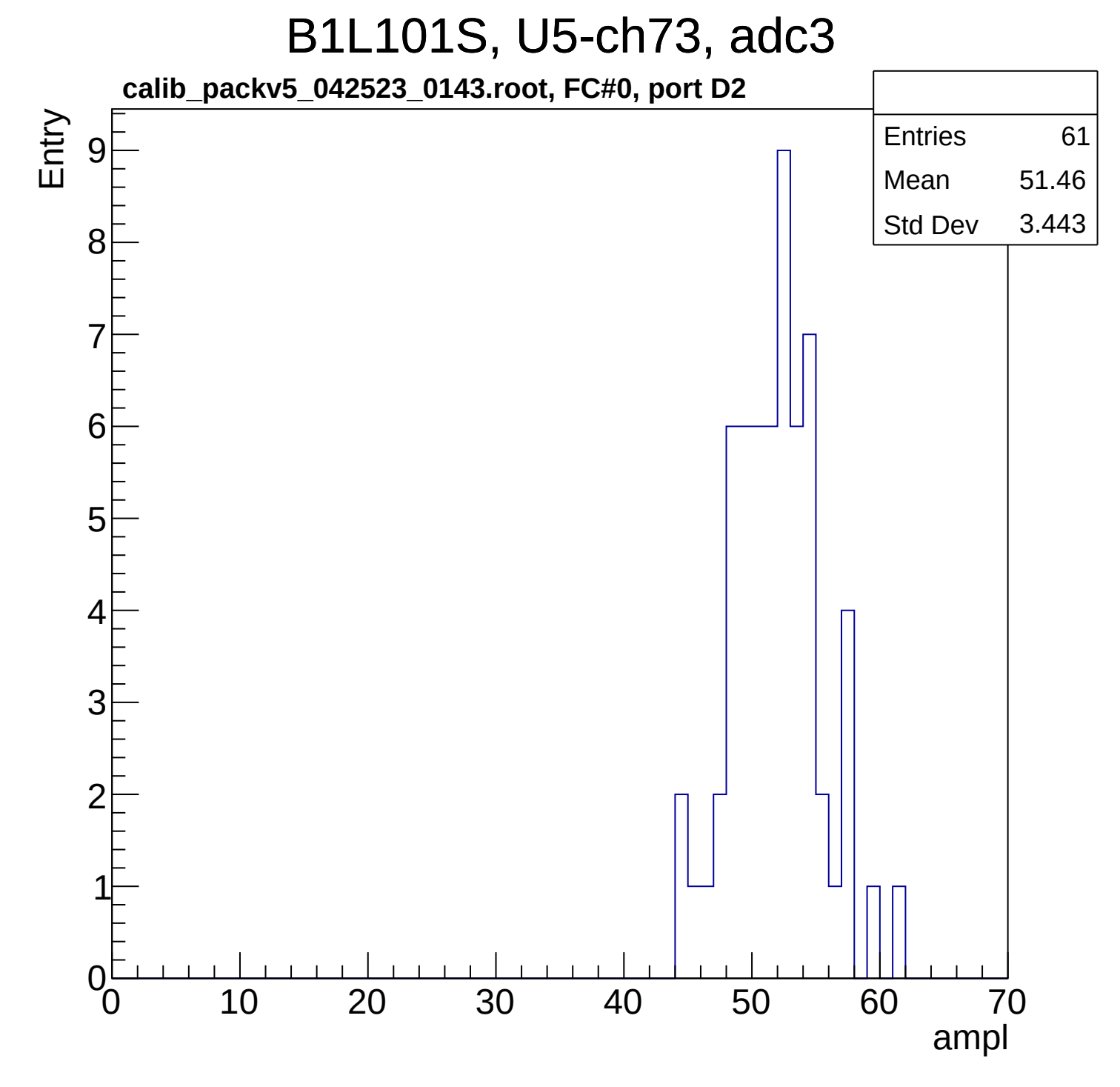
B1L101S, U5-ch73, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 51.46
Std Dev 3.443
Entry
ampl
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3
4
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6
7
8
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0
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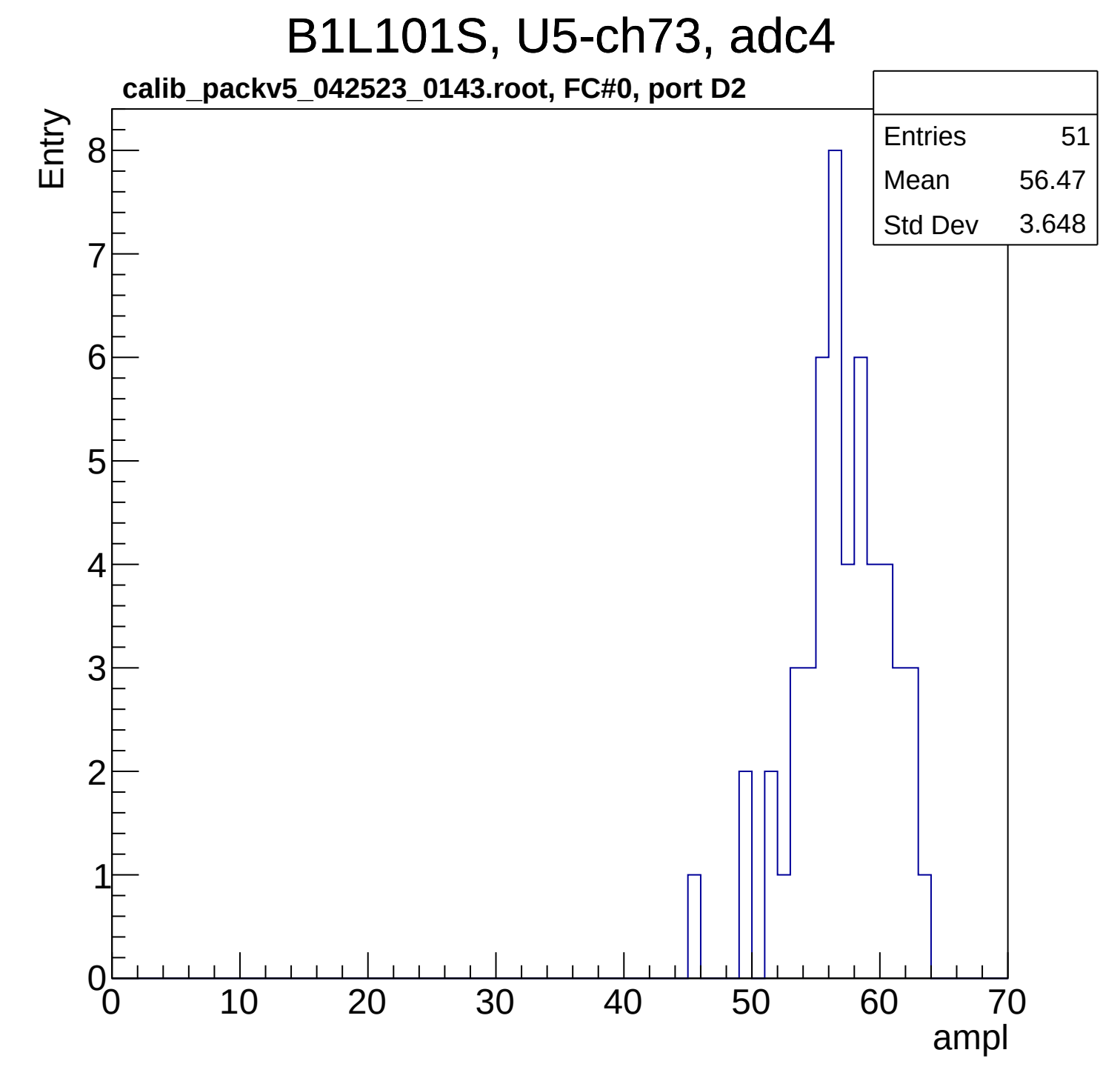
B1L101S, U5-ch73, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 56.47
Std Dev 3.648
Entry
ampl
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1
2
3
4
5
6
7
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0
10
20
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40
50
60
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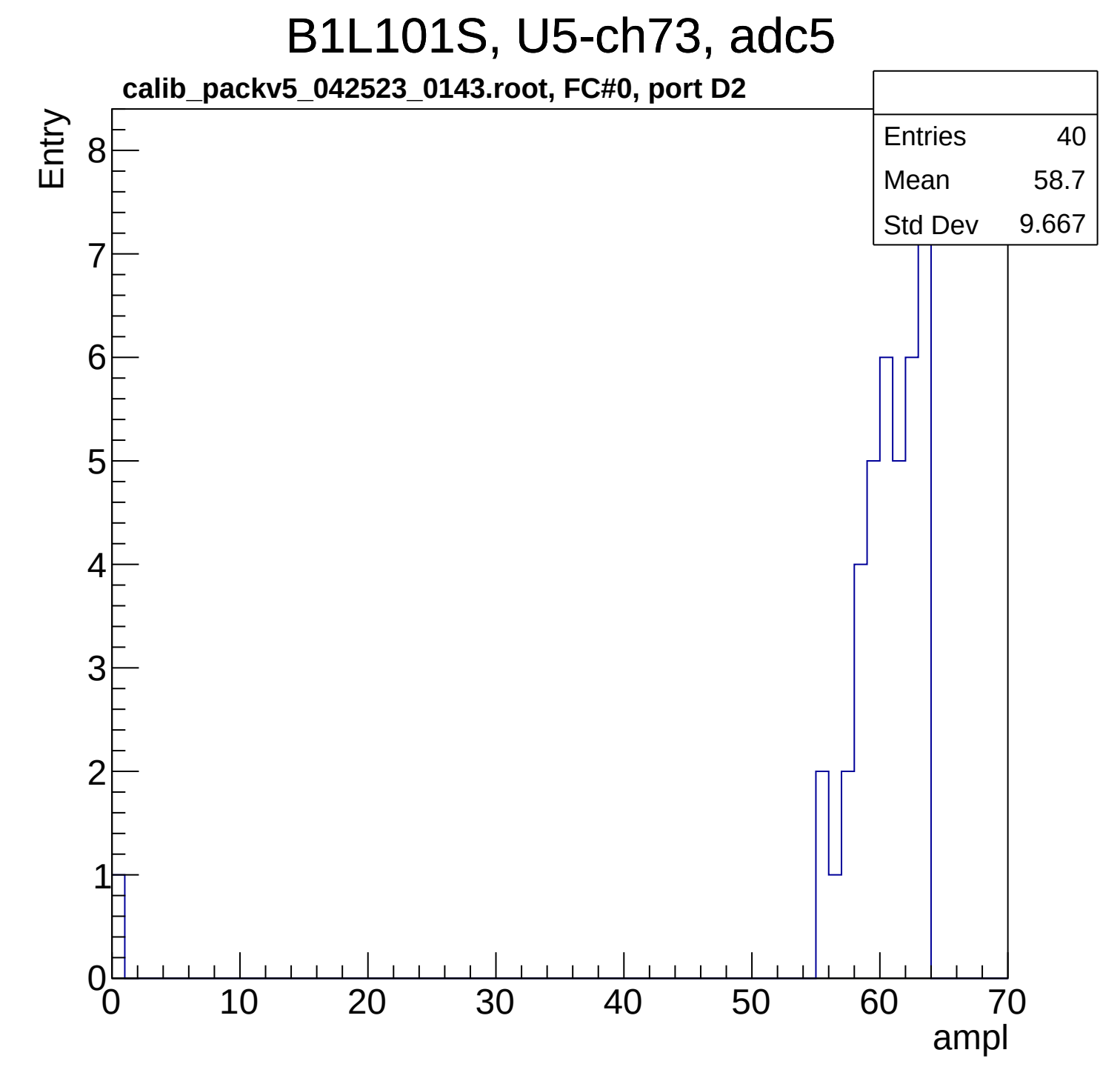
B1L101S, U5-ch73, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 40
Mean 58.7
Std Dev 9.667
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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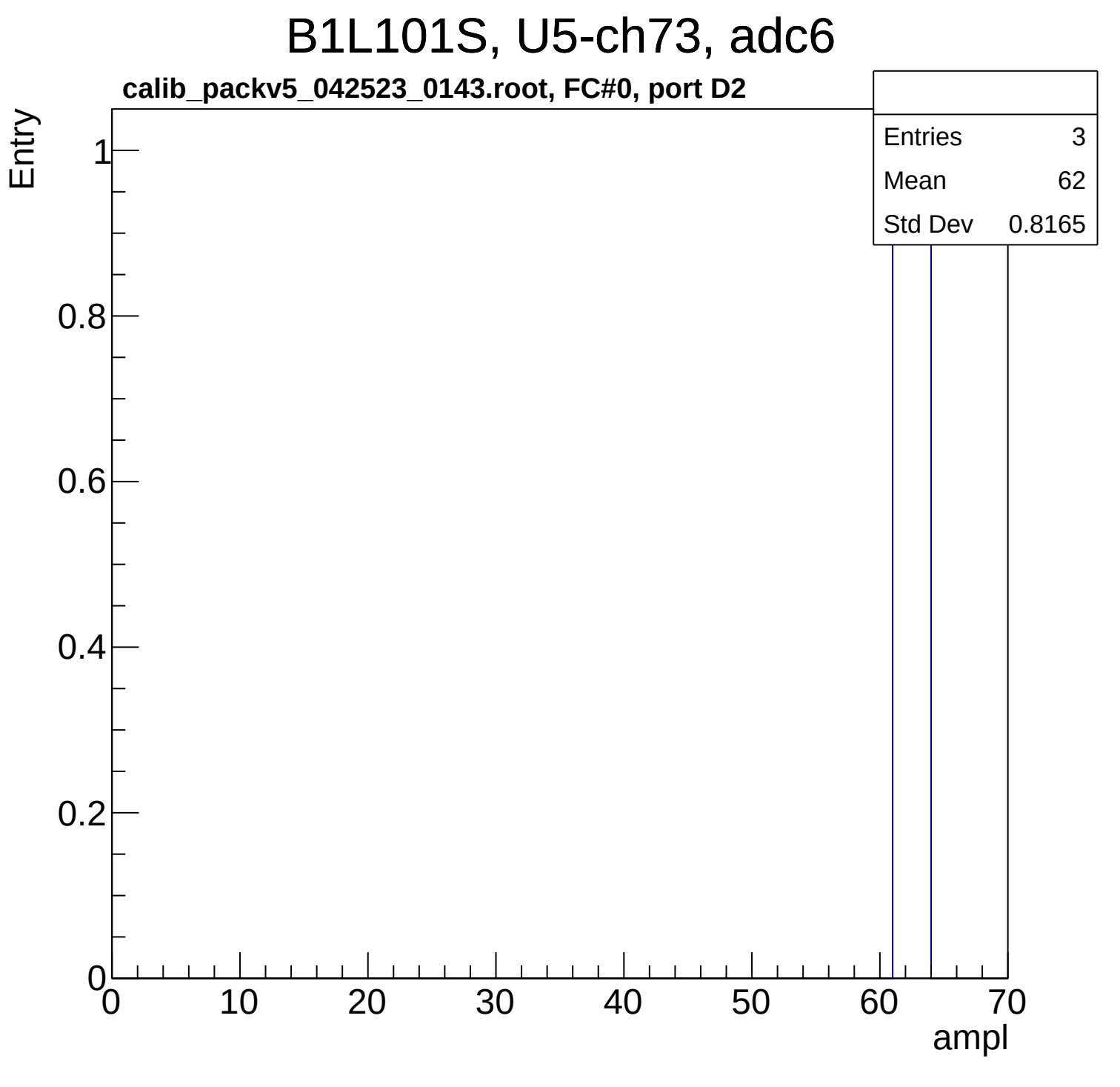
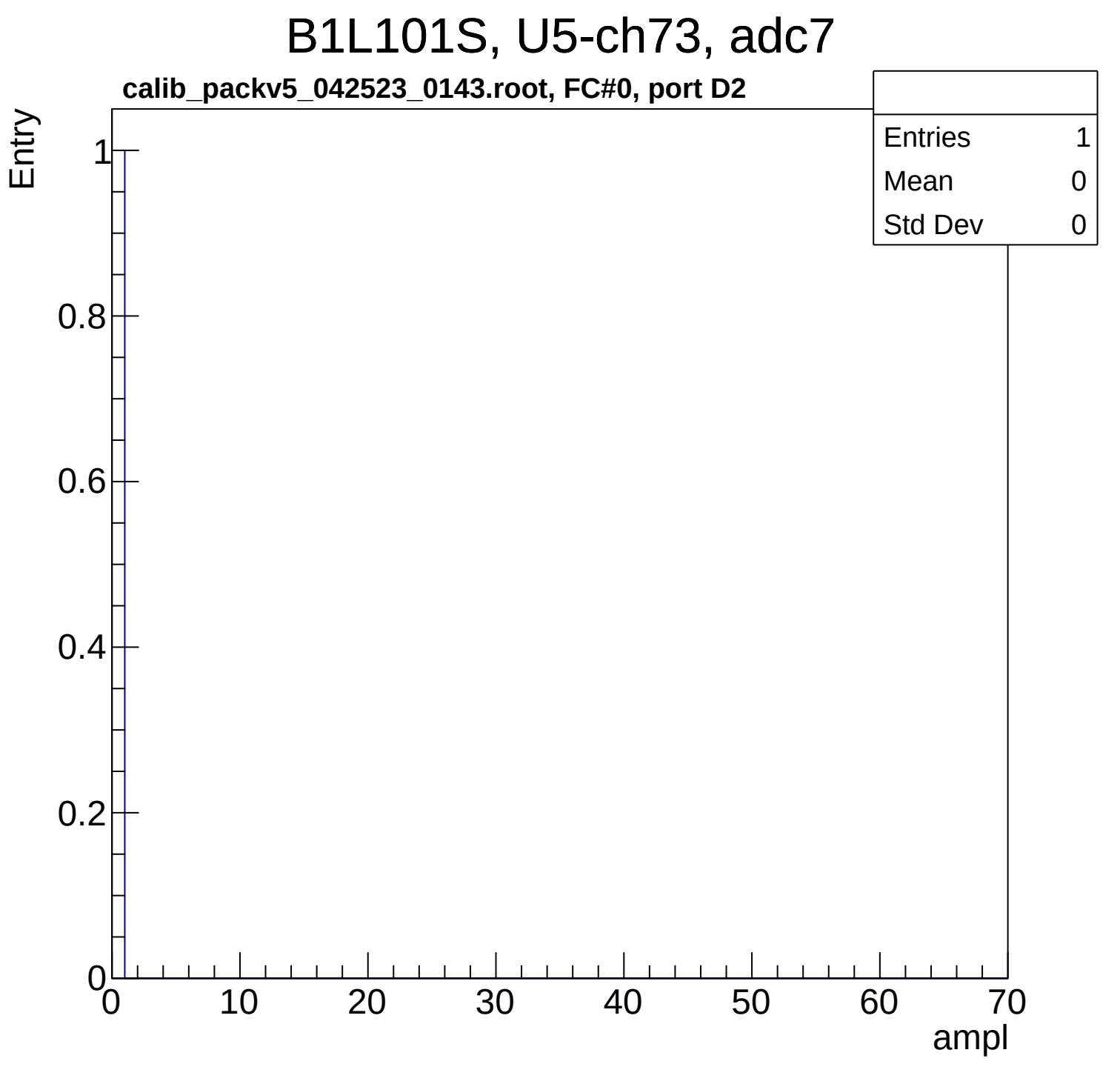
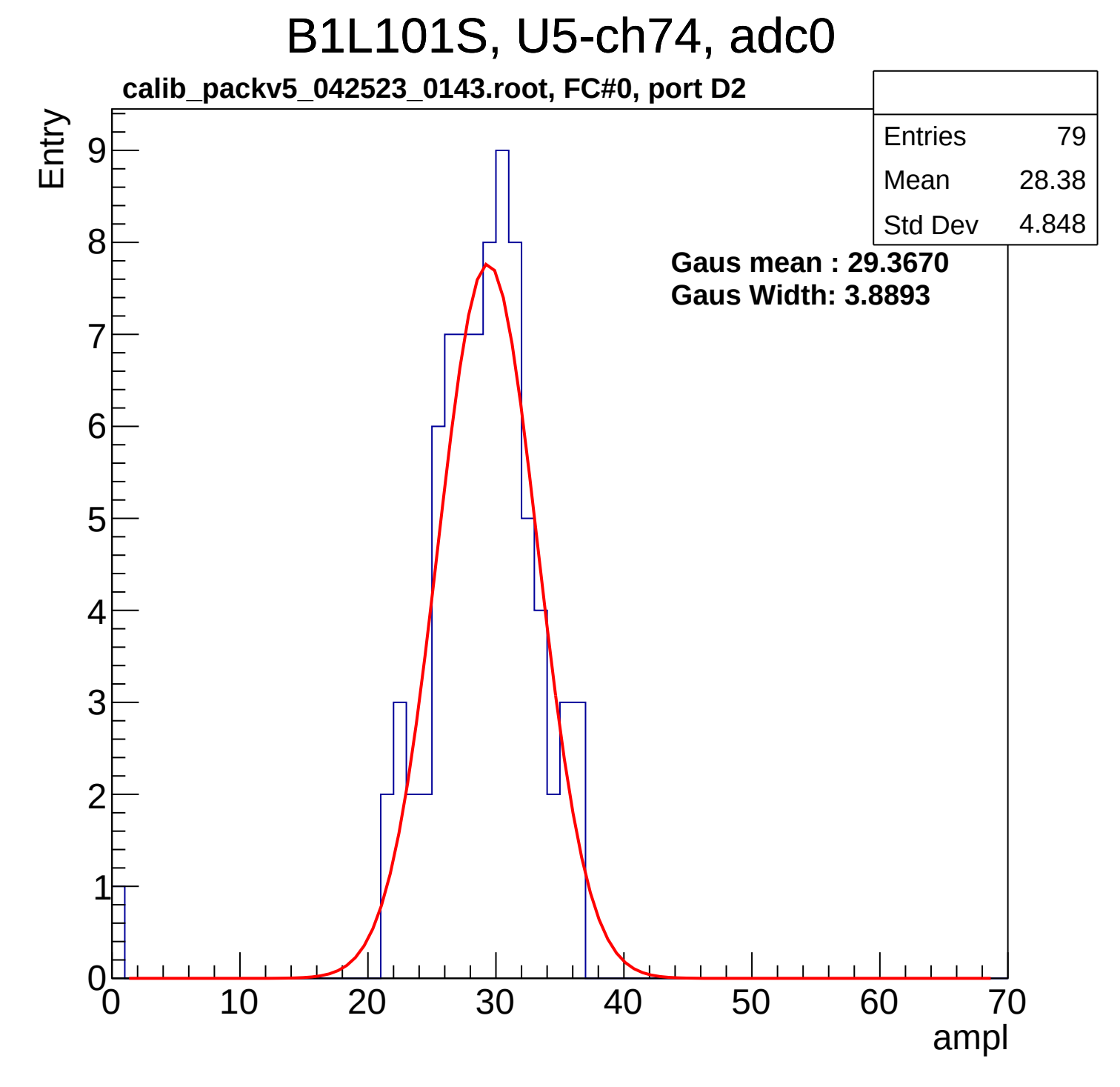

B1L101S, U5-ch73, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 62
Std Dev 0.8165
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch73, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch74, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 28.38
Std Dev 4.848
Gaus mean : 29.3670
Gaus Width: 3.8893
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
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60
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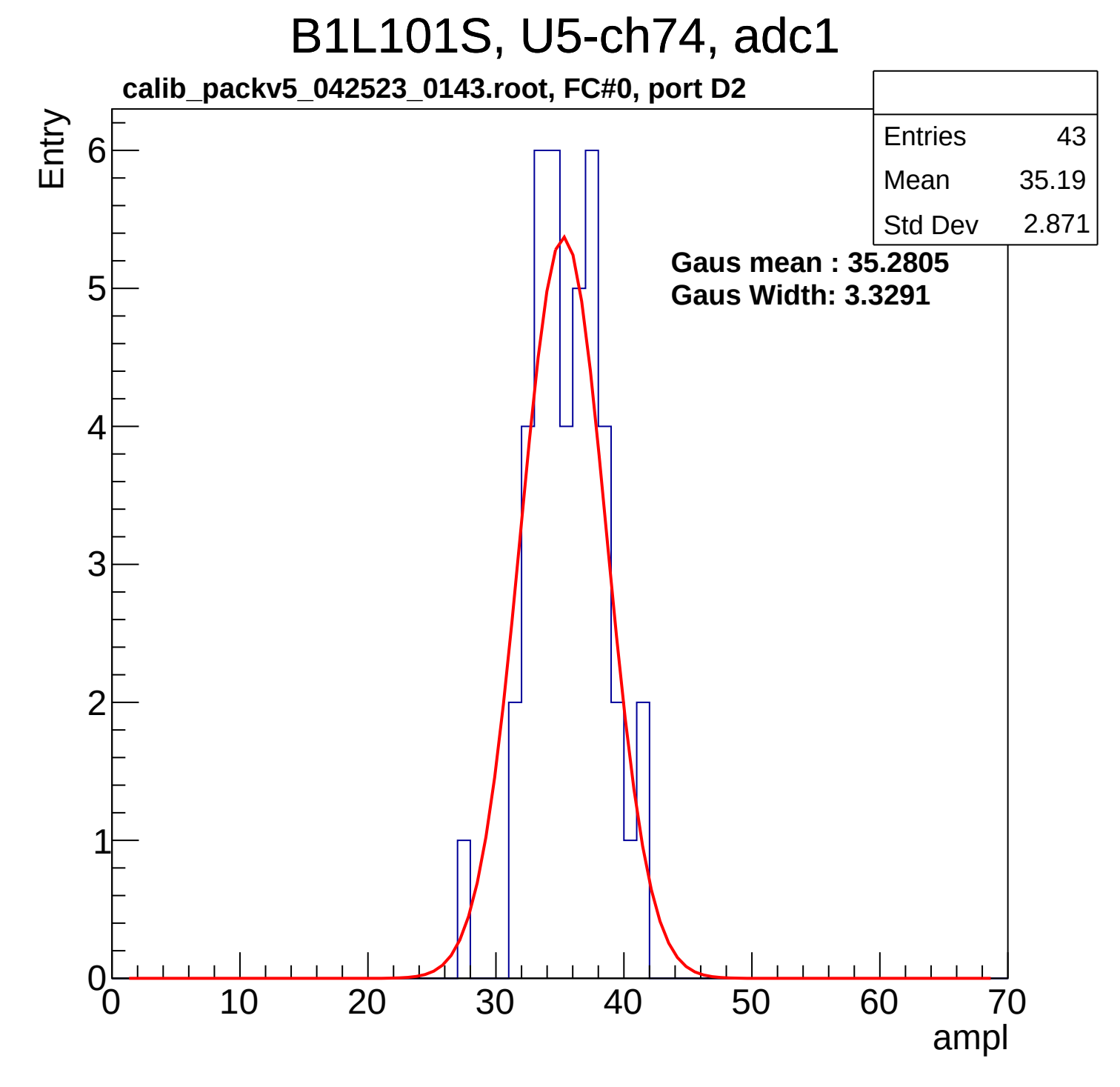
B1L101S, U5-ch74, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 43
Mean 35.19
Std Dev 2.871
Gaus mean : 35.2805
Gaus Width: 3.3291
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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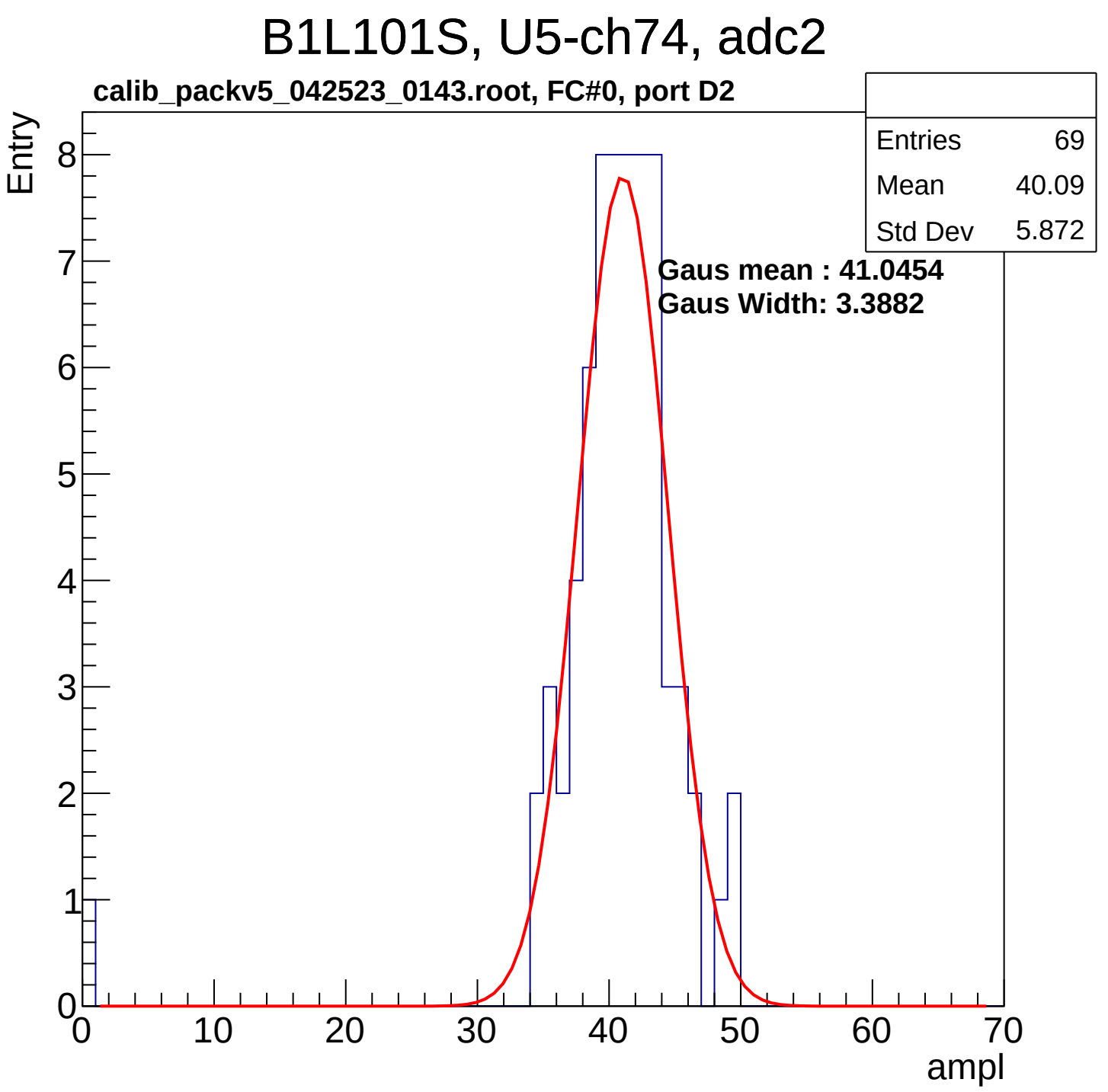
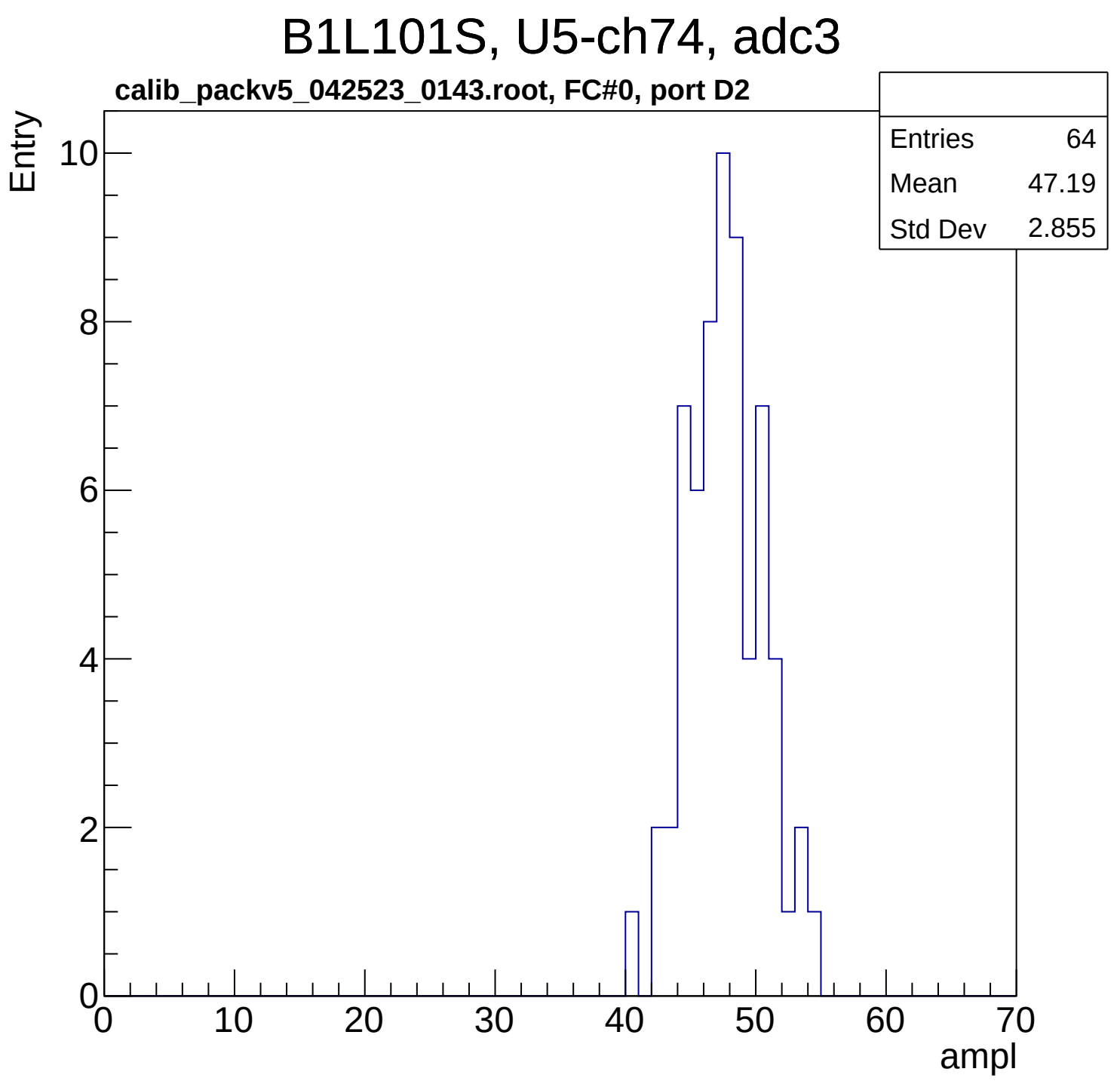
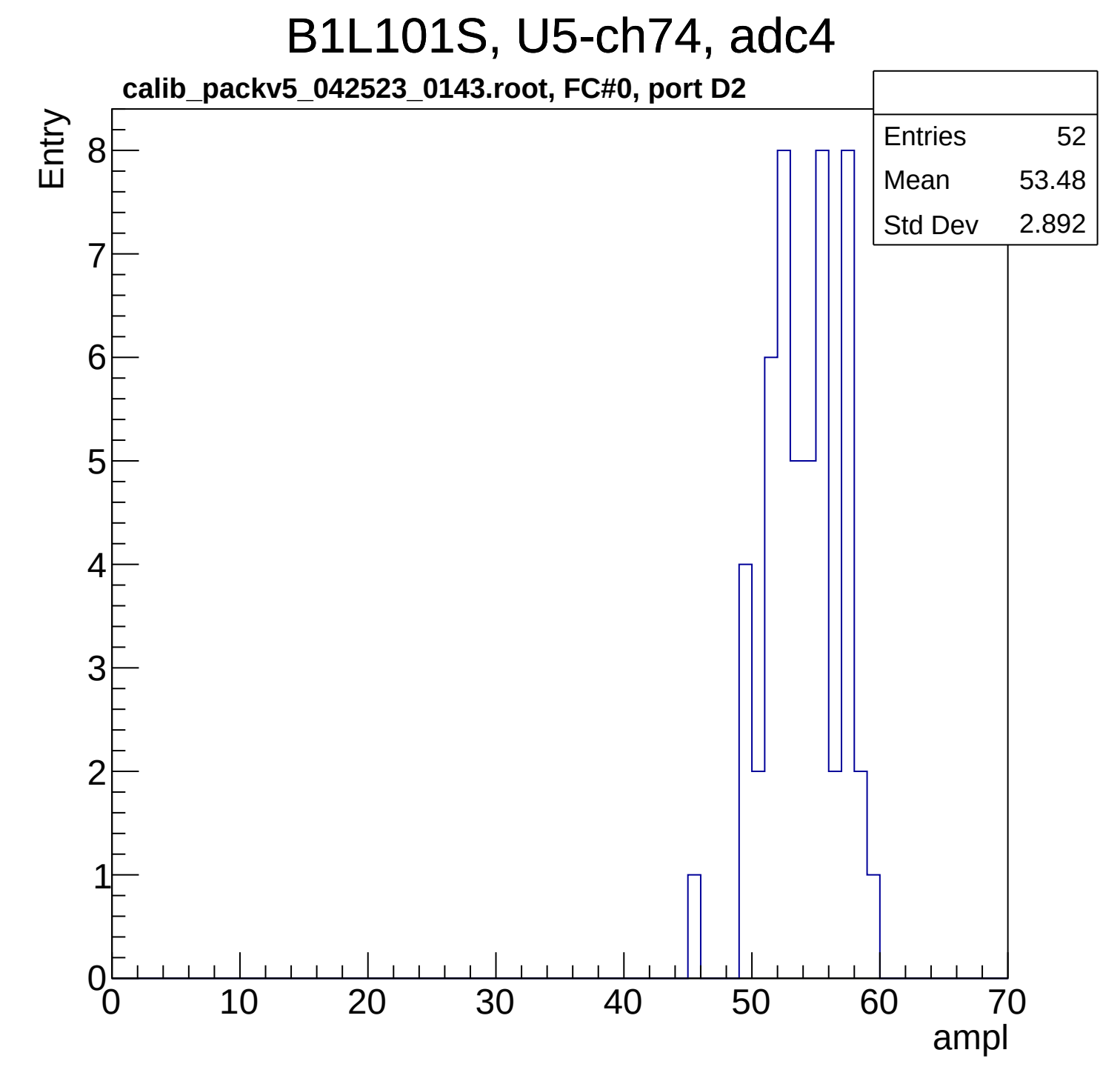

B1L101S, U5-ch74, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 40.09
Std Dev 5.872
Gaus mean : 41.0454
Gaus Width: 3.3882
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch74, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 47.19
Std Dev 2.855
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch74, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 53.48
Std Dev 2.892
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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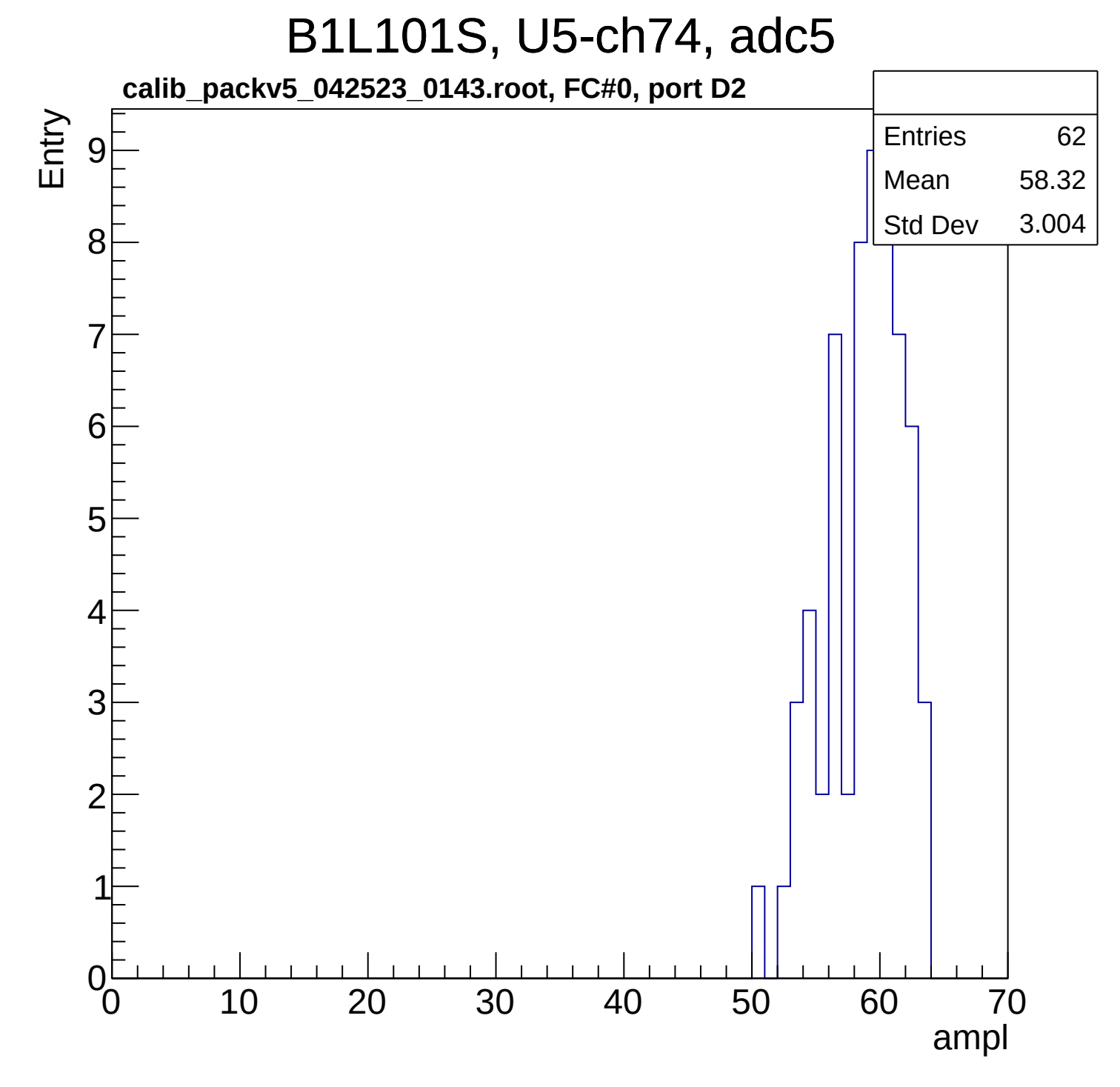
B1L101S, U5-ch74, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 58.32
Std Dev 3.004
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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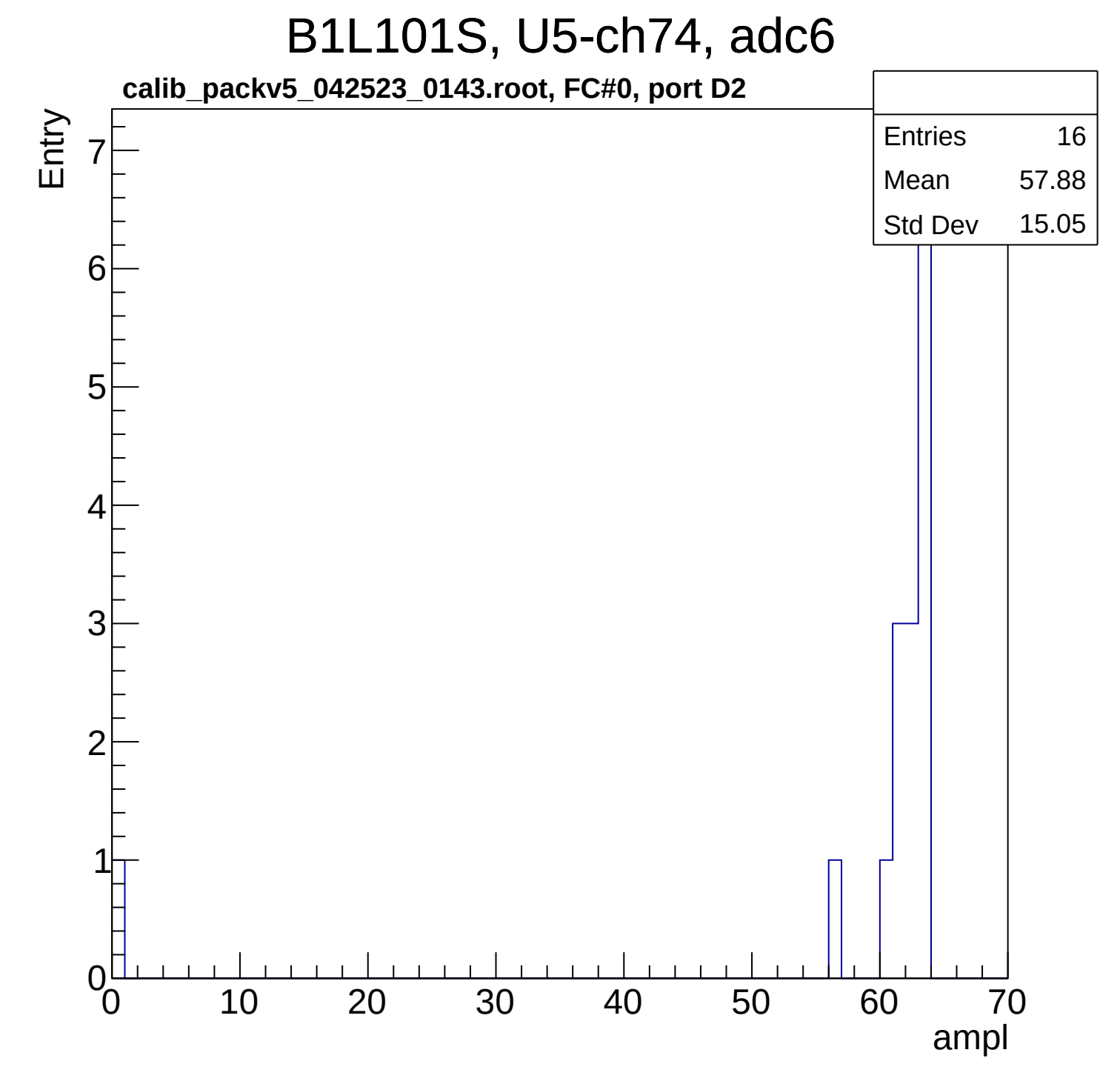
B1L101S, U5-ch74, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 16
Mean 57.88
Std Dev 15.05
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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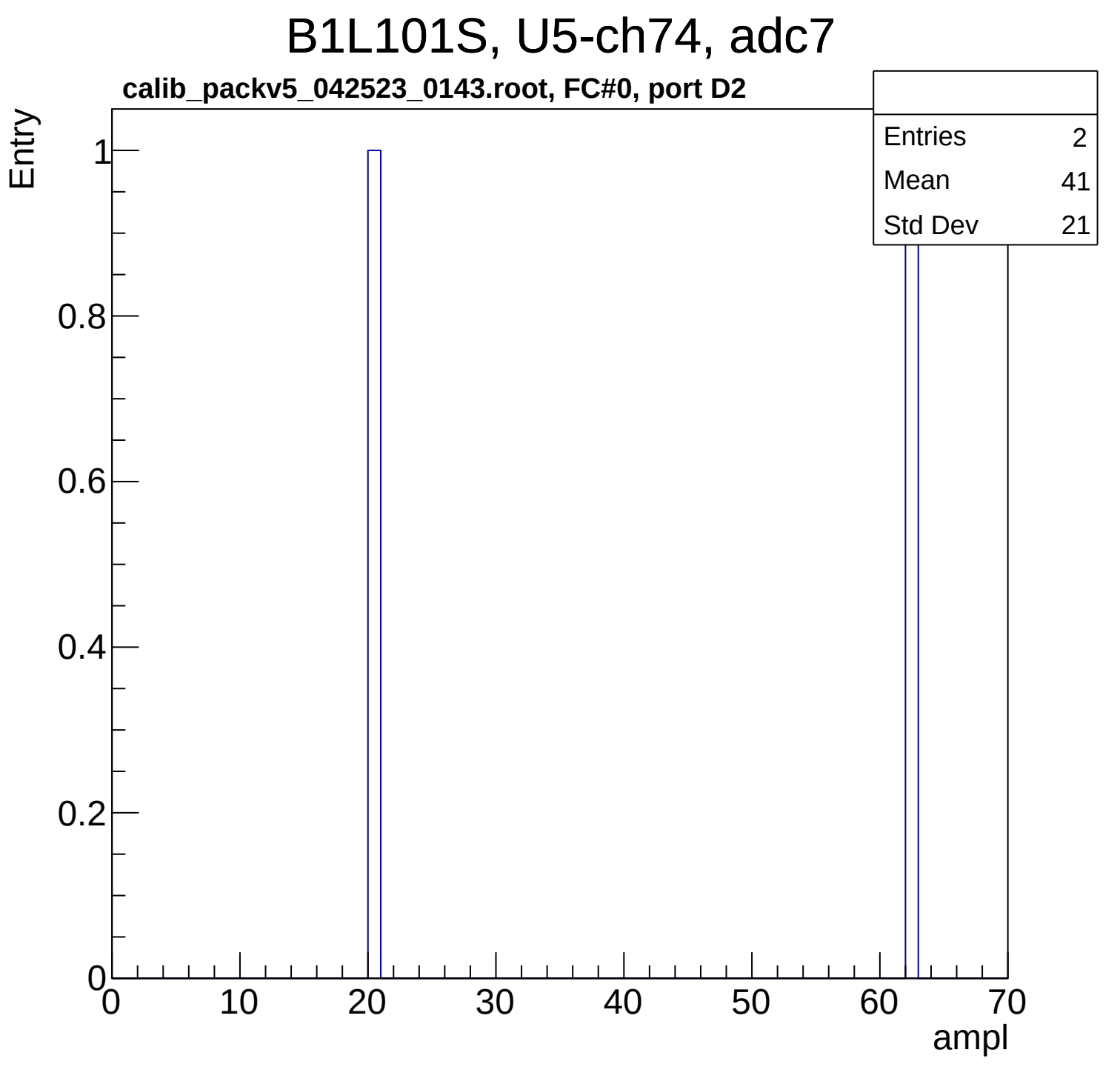
B1L101S, U5-ch74, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 41
Std Dev 21
Entry
ampl
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0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
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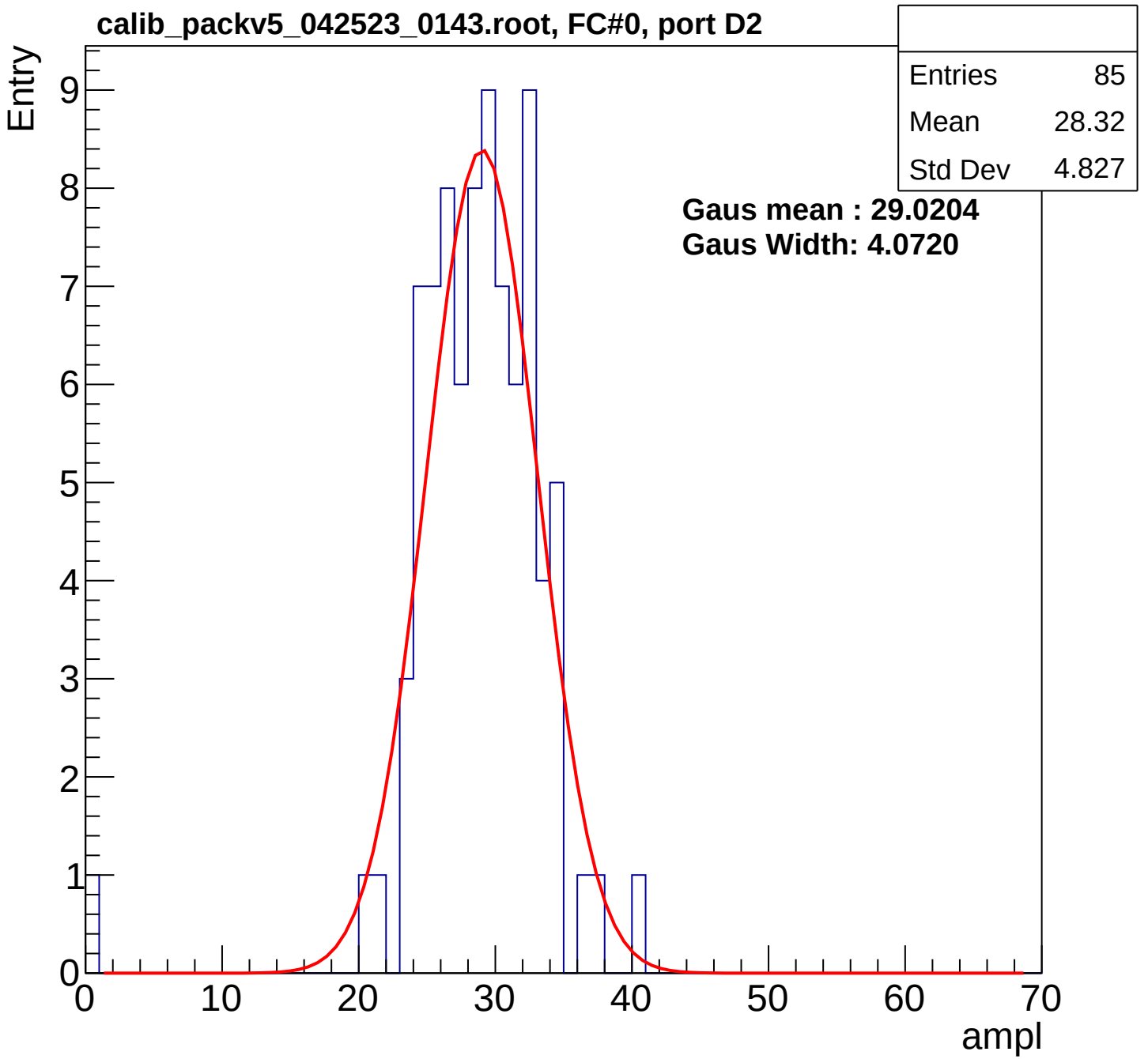
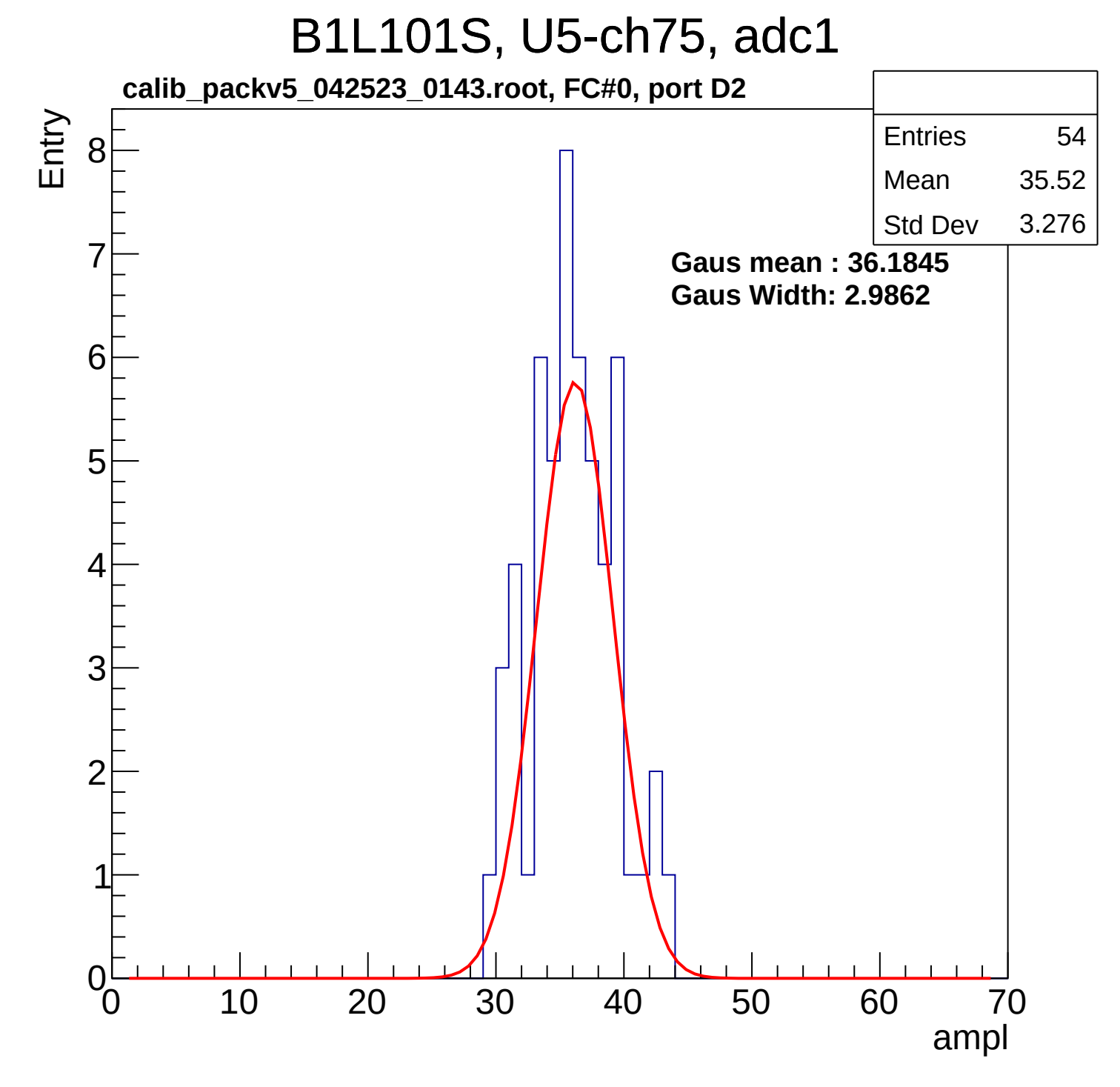

B1L101S, U5-ch75, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 85
Mean 28.32
Std Dev 4.827
Gaus mean : 29.0204
Gaus Width: 4.0720
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch75, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 35.52
Std Dev 3.276
Gaus mean : 36.1845
Gaus Width: 2.9862
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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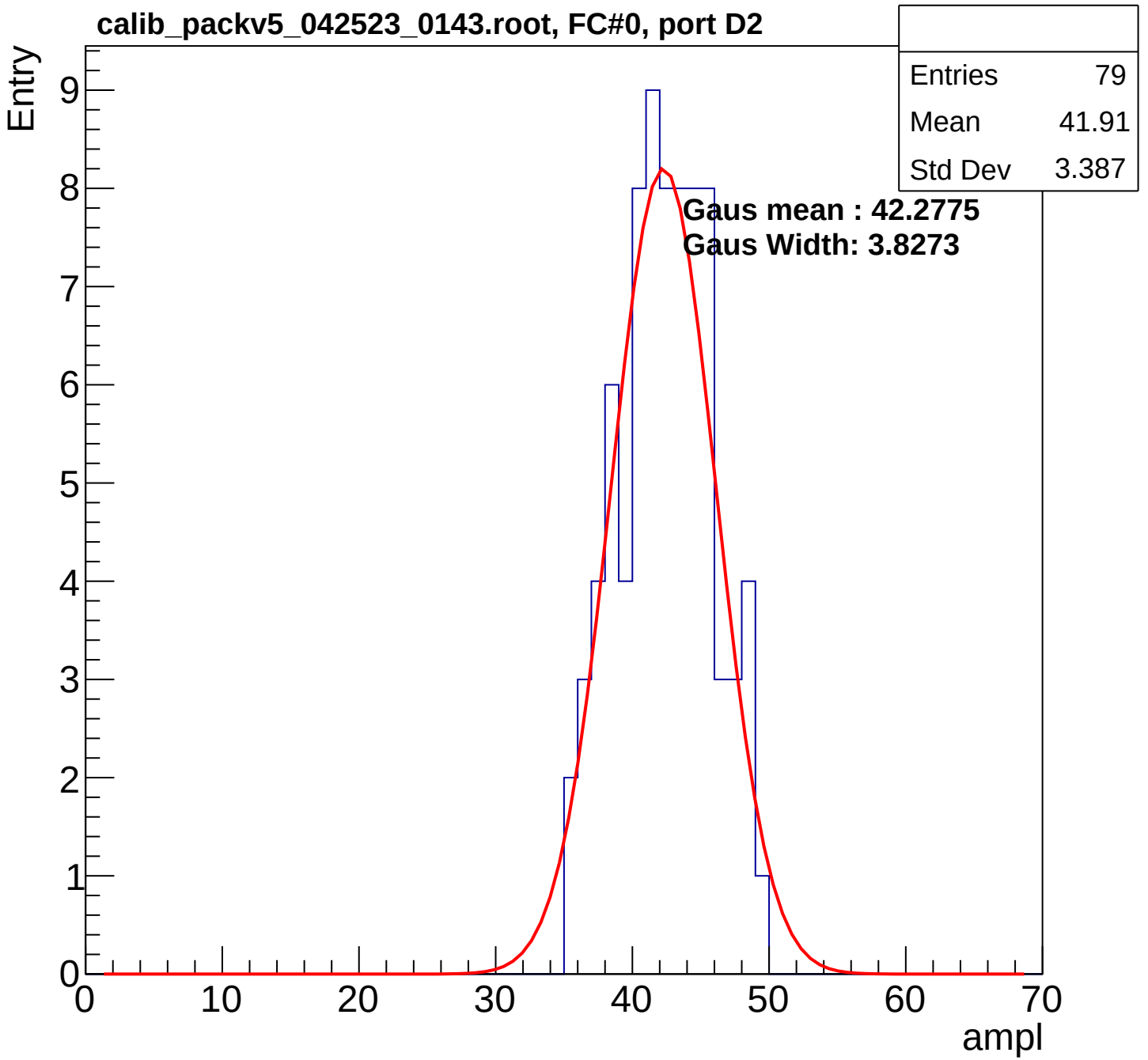
B1L101S, U5-ch75, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 41.91
Std Dev 3.387
Gaus mean : 42.2775
Gaus Width: 3.8273
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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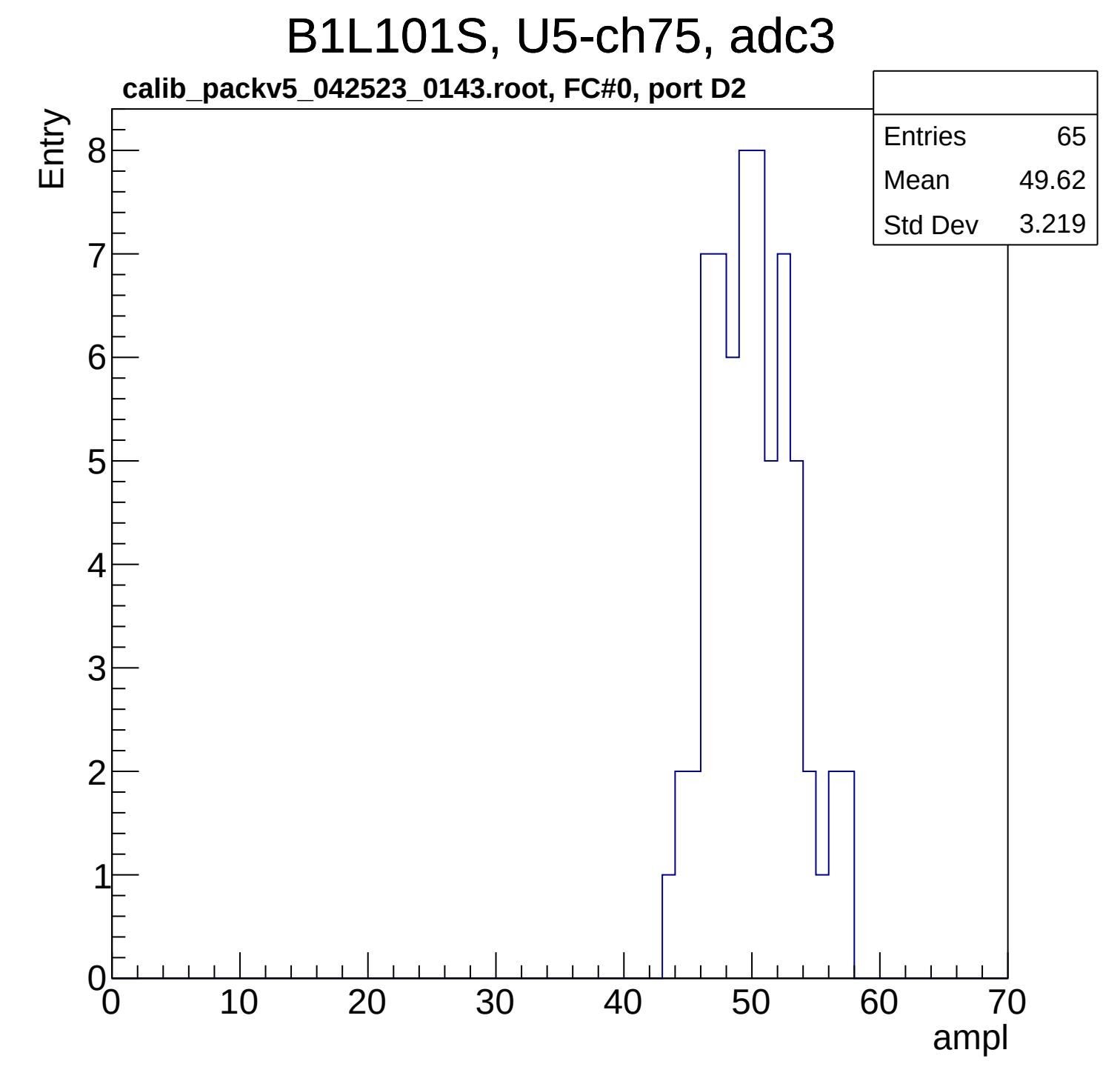
60
70


B1L101S, U5-ch75, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 49.62
Std Dev 3.219
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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60
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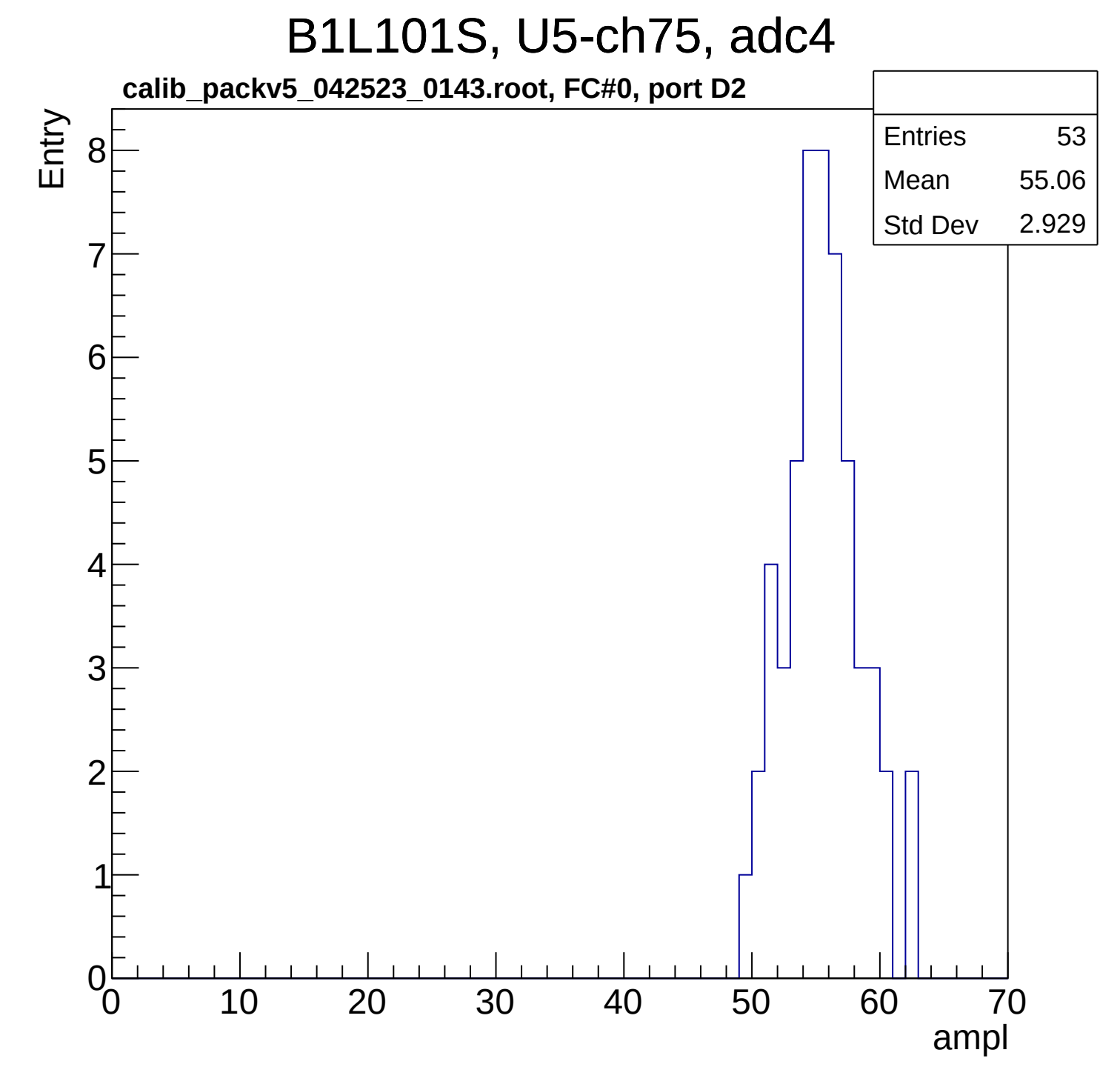
B1L101S, U5-ch75, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 55.06
Std Dev 2.929
Entry
ampl
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5
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0
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40
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60
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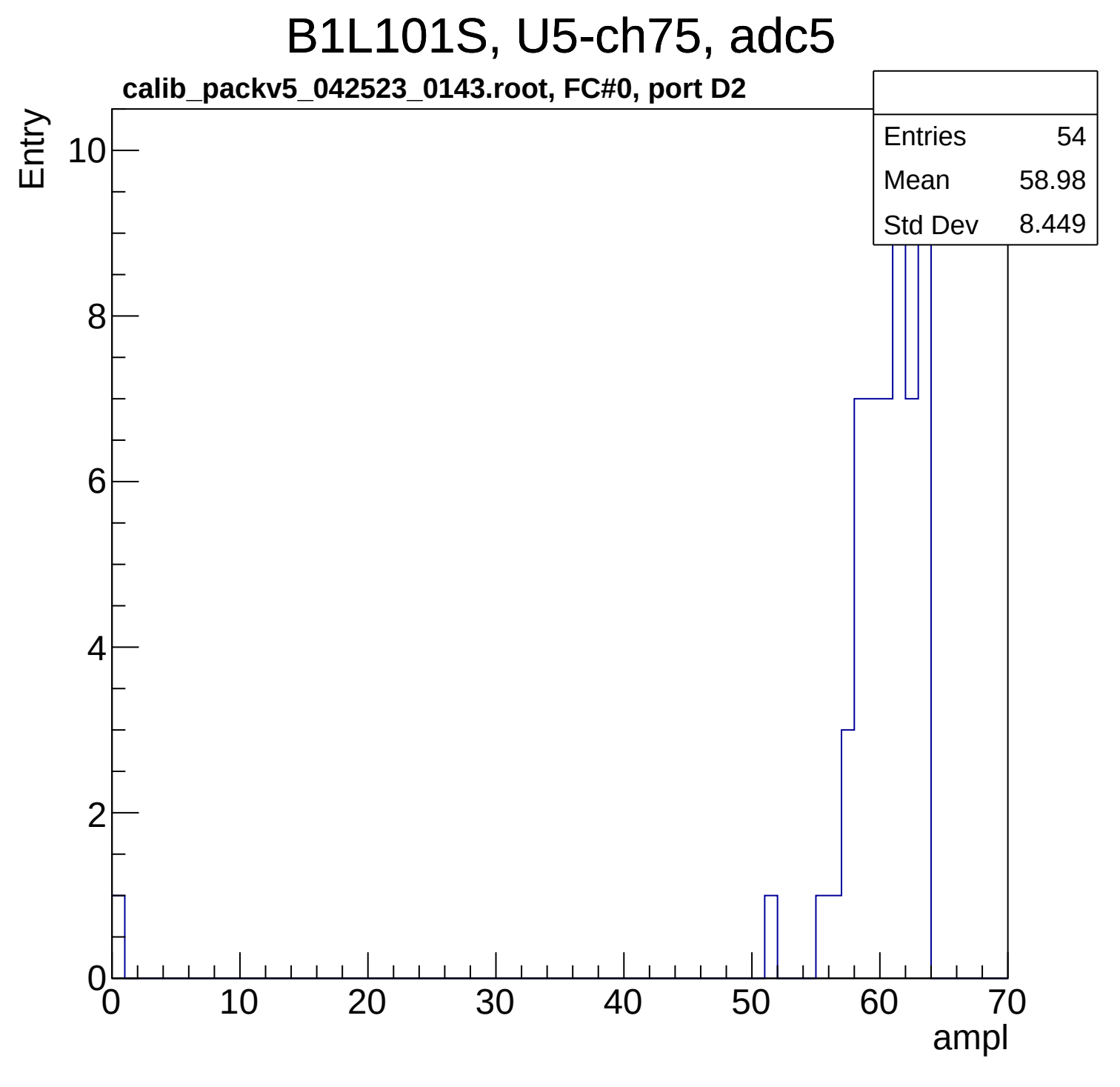
B1L101S, U5-ch75, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 58.98
Std Dev 8.449
Entry
ampl
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60
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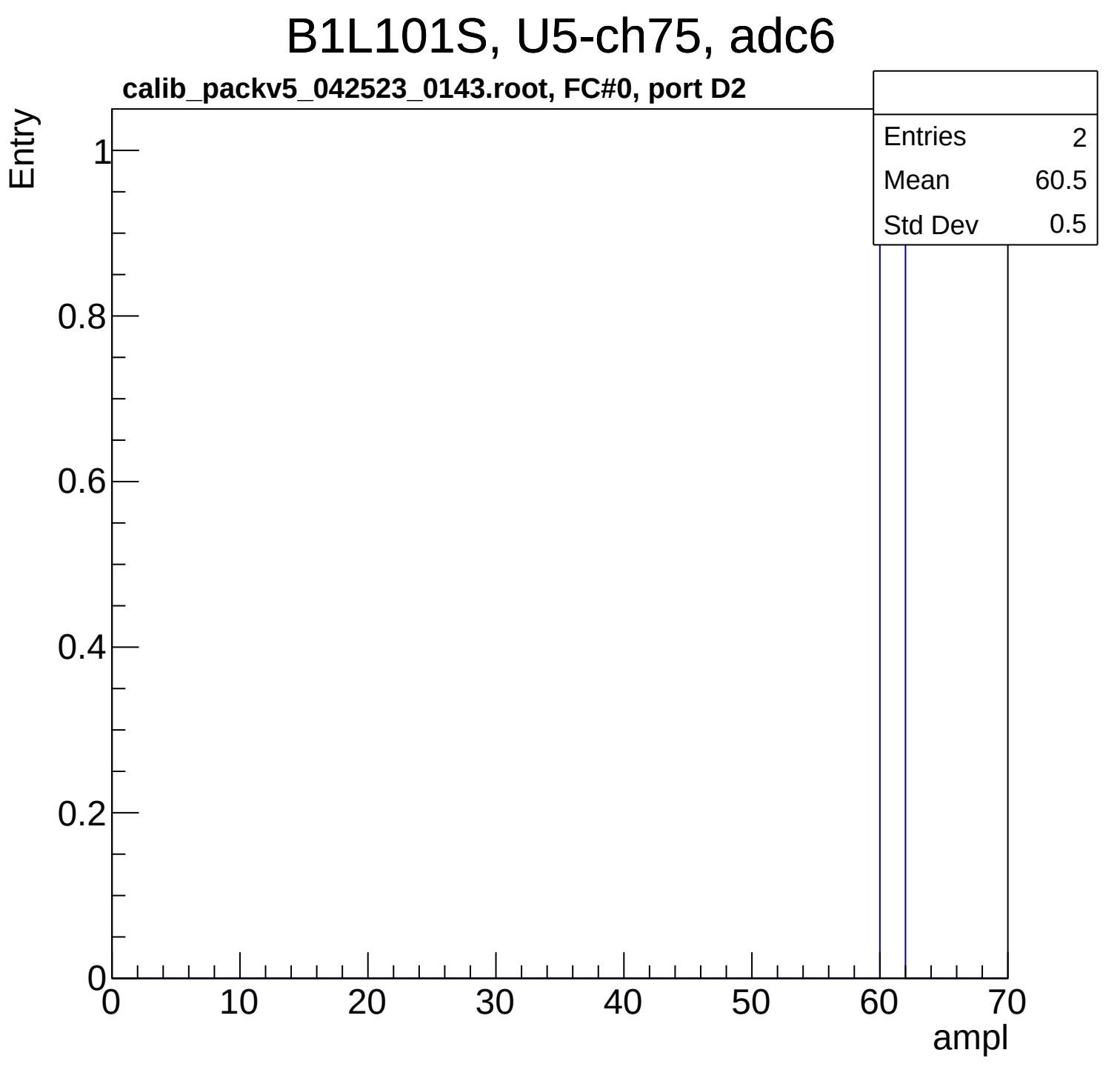
B1L101S, U5-ch75, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 60.5
Std Dev 0.5
Entry
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0.6
0.4
0.2
0
0
10
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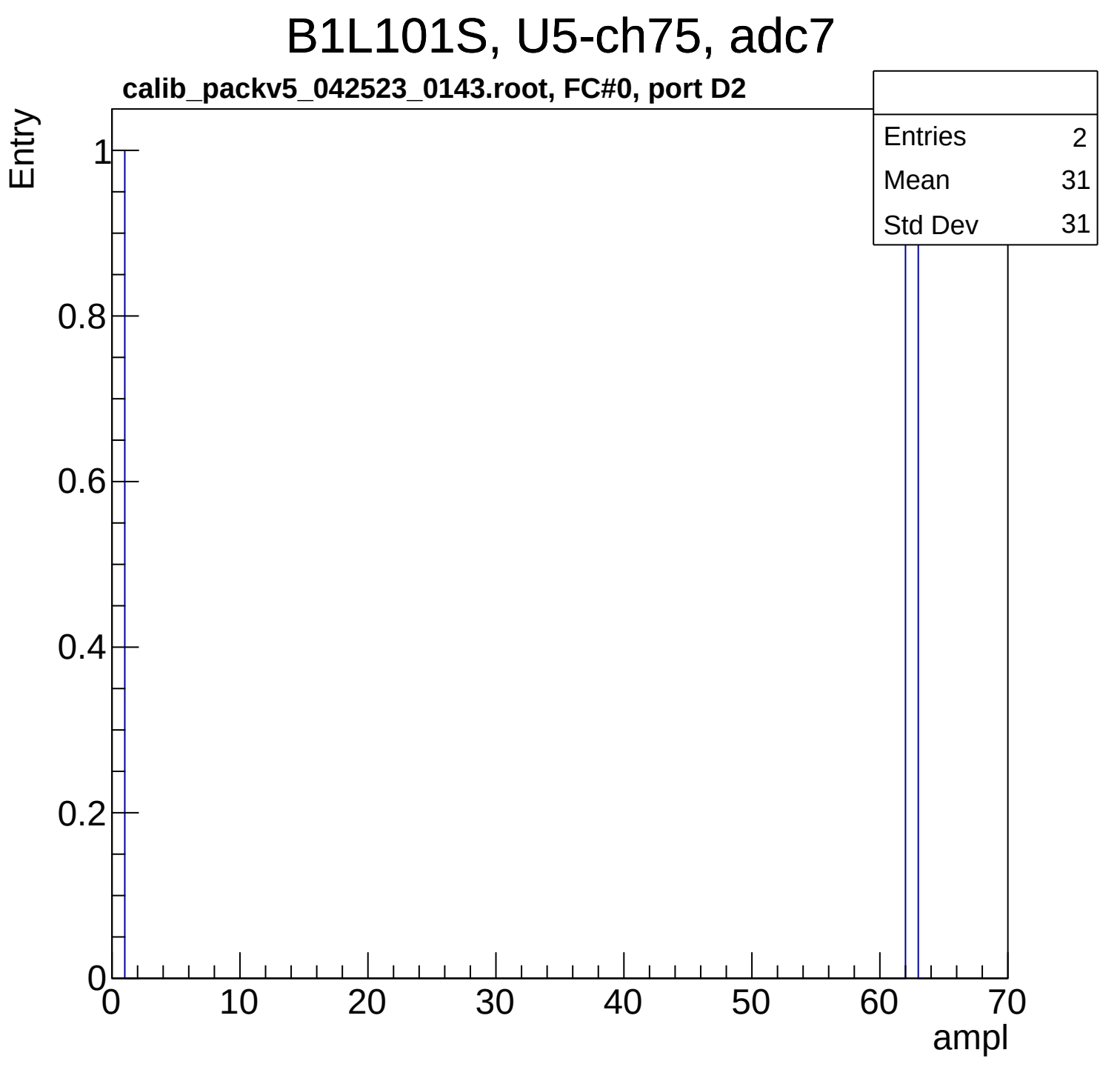
40
50
60
70
ampl


B1L101S, U5-ch75, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 31
Std Dev 31
Entry
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0.6
0.4
0.2
0
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10
20
30
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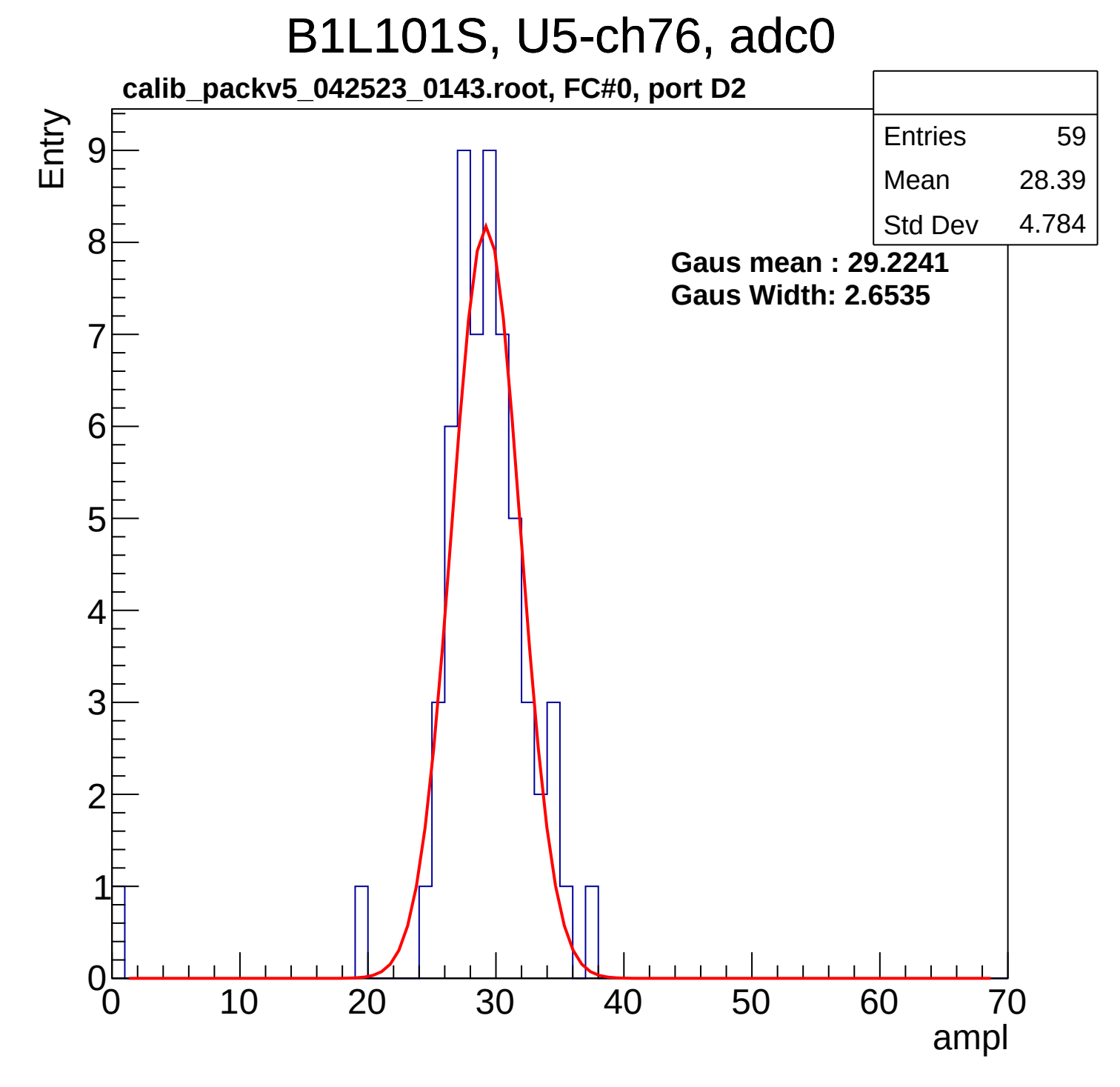
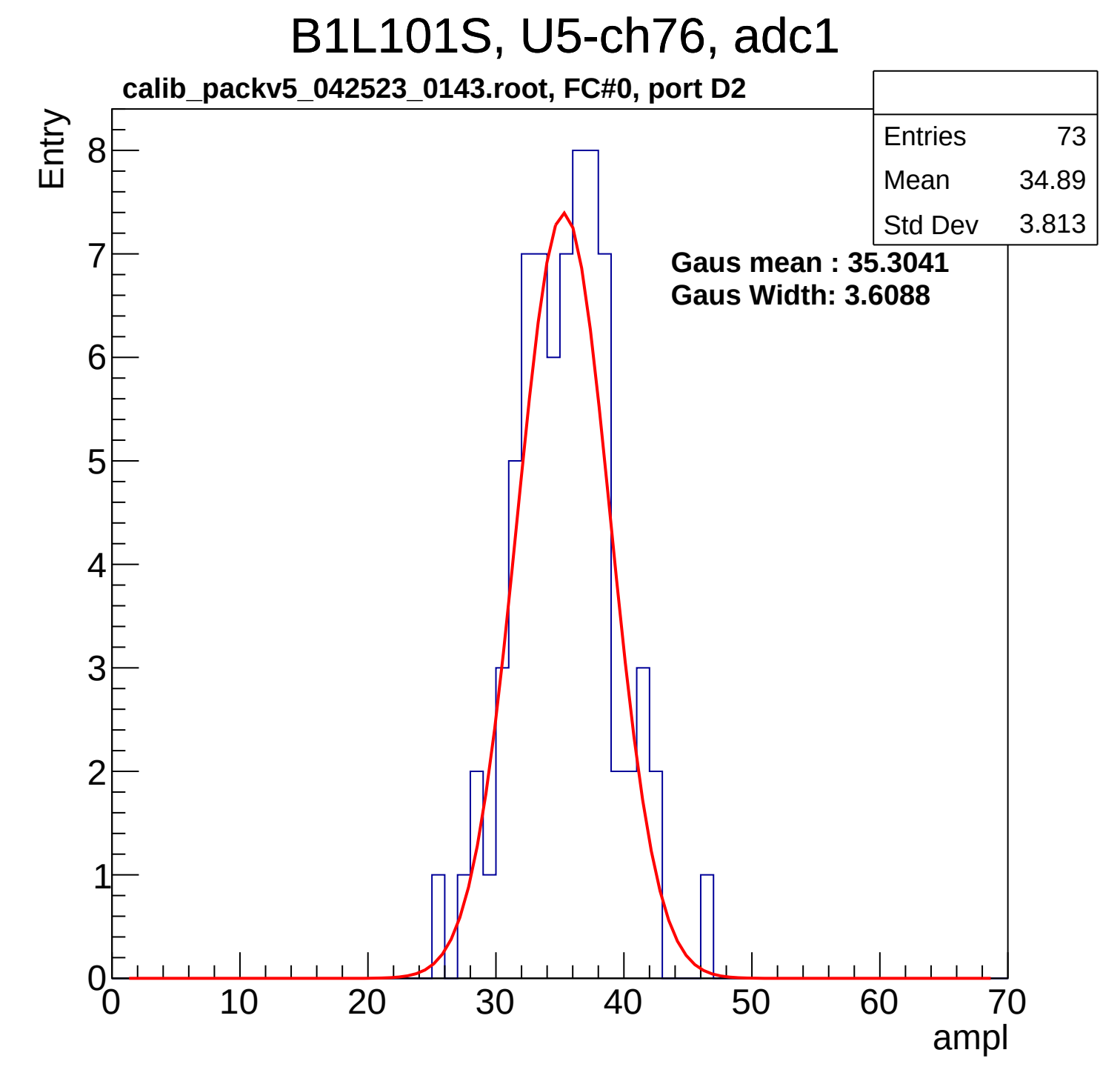
50
60
70
ampl


B1L101S, U5-ch76, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 28.39
Std Dev 4.784
Gaus mean : 29.2241
Gaus Width: 2.6535
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch76, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 34.89
Std Dev 3.813
Gaus mean : 35.3041
Gaus Width: 3.6088
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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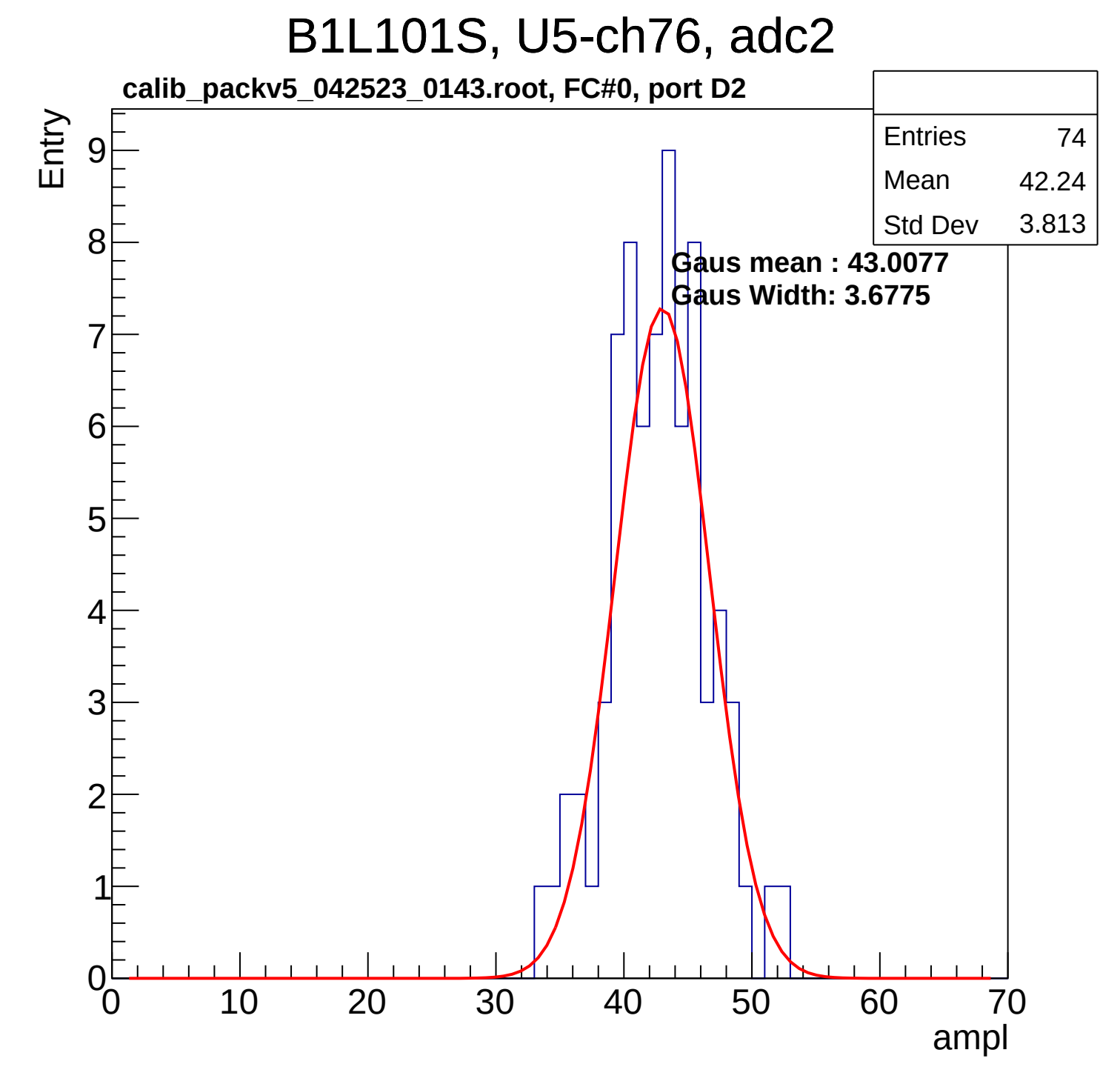
B1L101S, U5-ch76, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 42.24
Std Dev 3.813
Gaus mean : 43.0077
Gaus Width: 3.6775
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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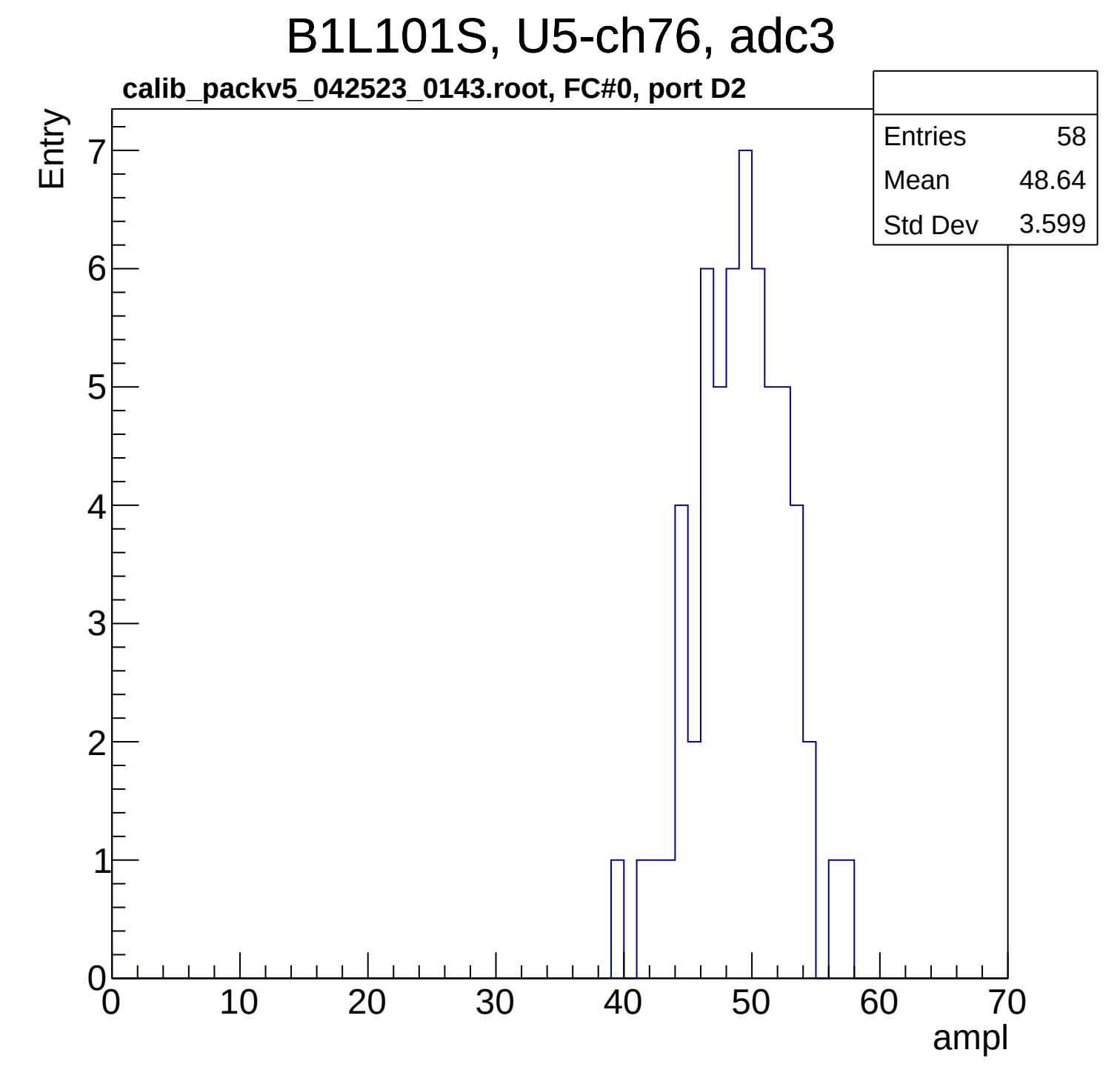
B1L101S, U5-ch76, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 48.64
Std Dev 3.599
Entry
ampl
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2
3
4
5
6
7
0
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60
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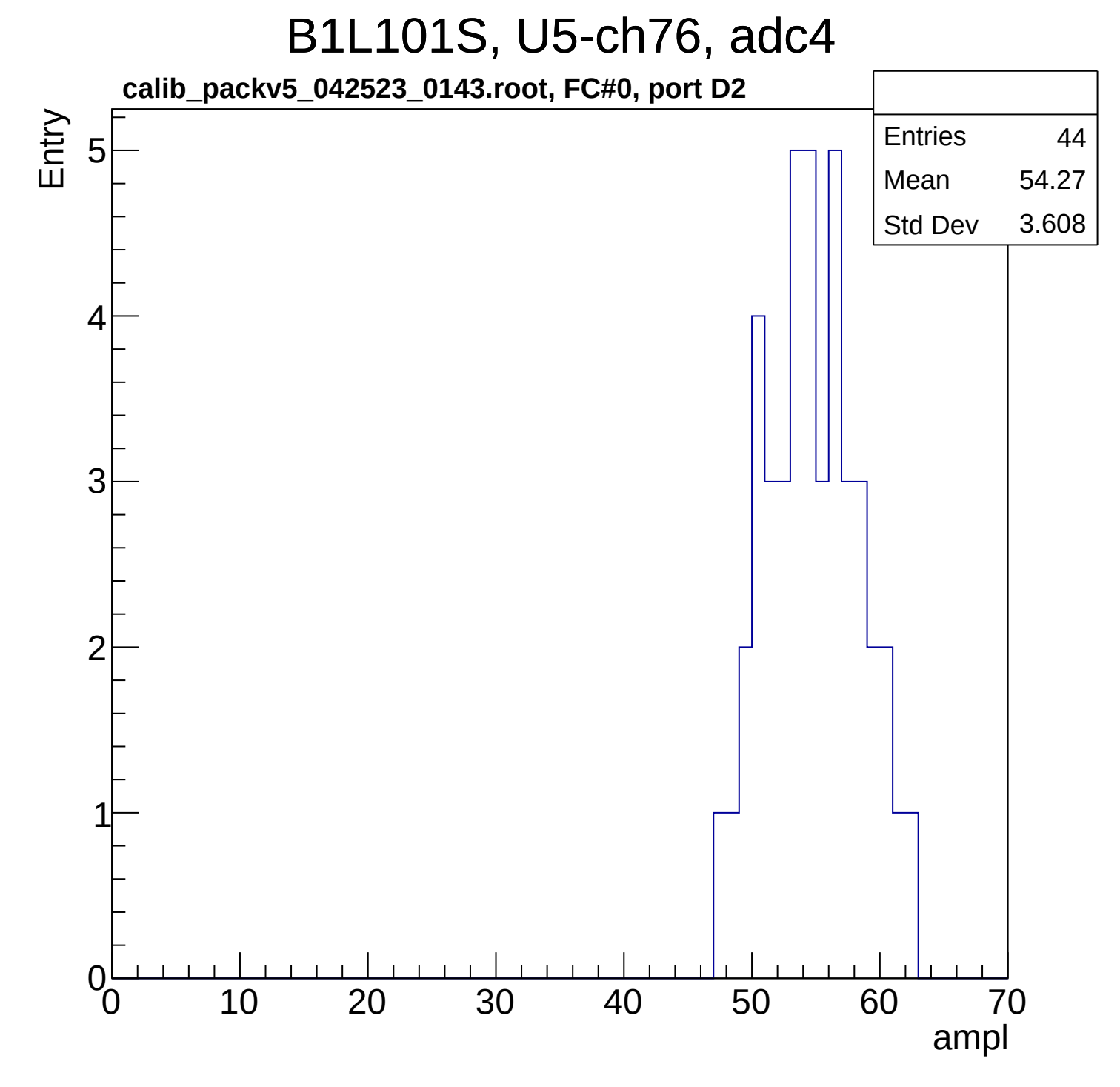
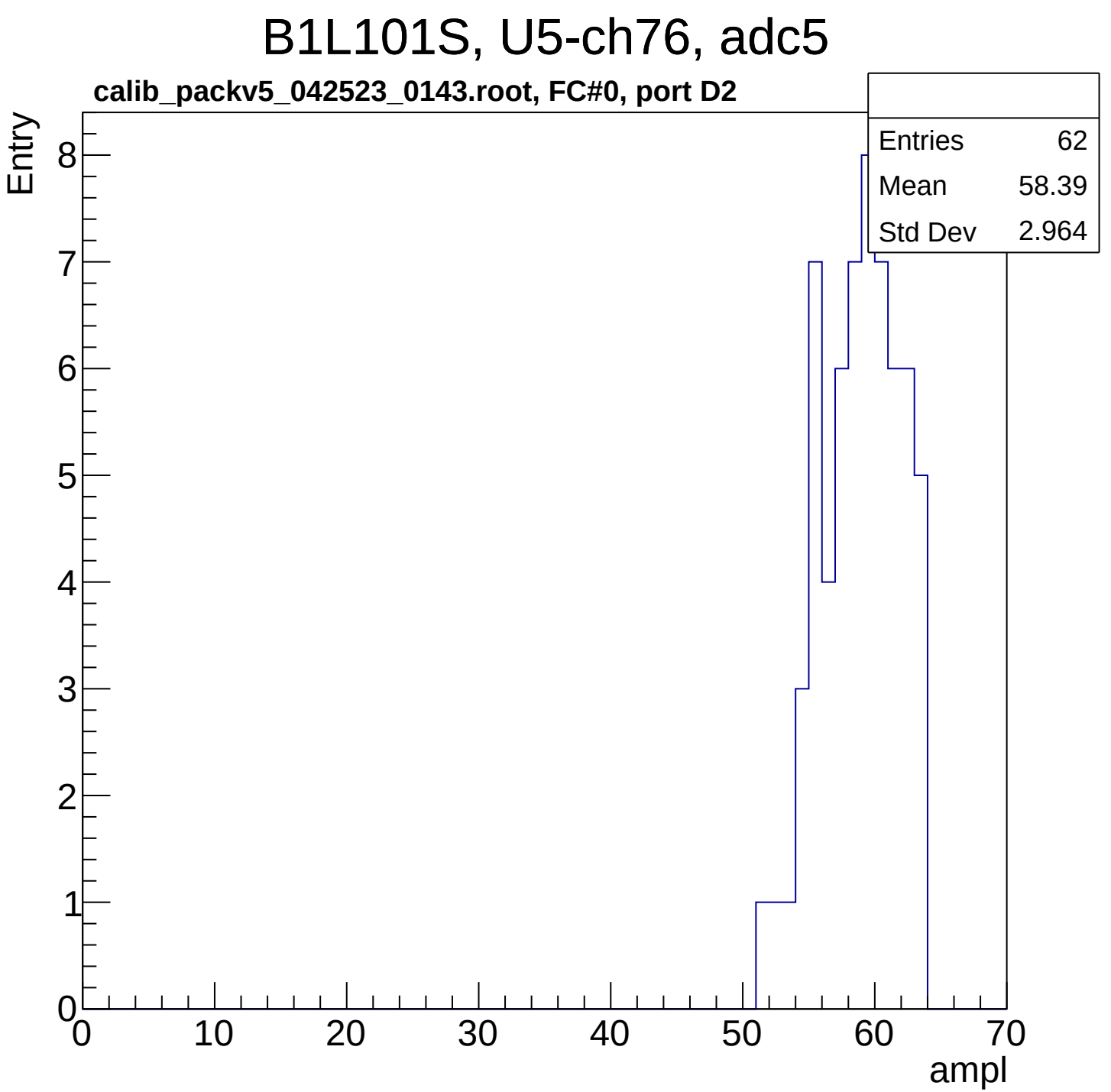

B1L101S, U5-ch76, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 44
Mean 54.27
Std Dev 3.608
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch76, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 58.39
Std Dev 2.964
Entry
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2
3
4
5
6
7
8
0
10
20
30
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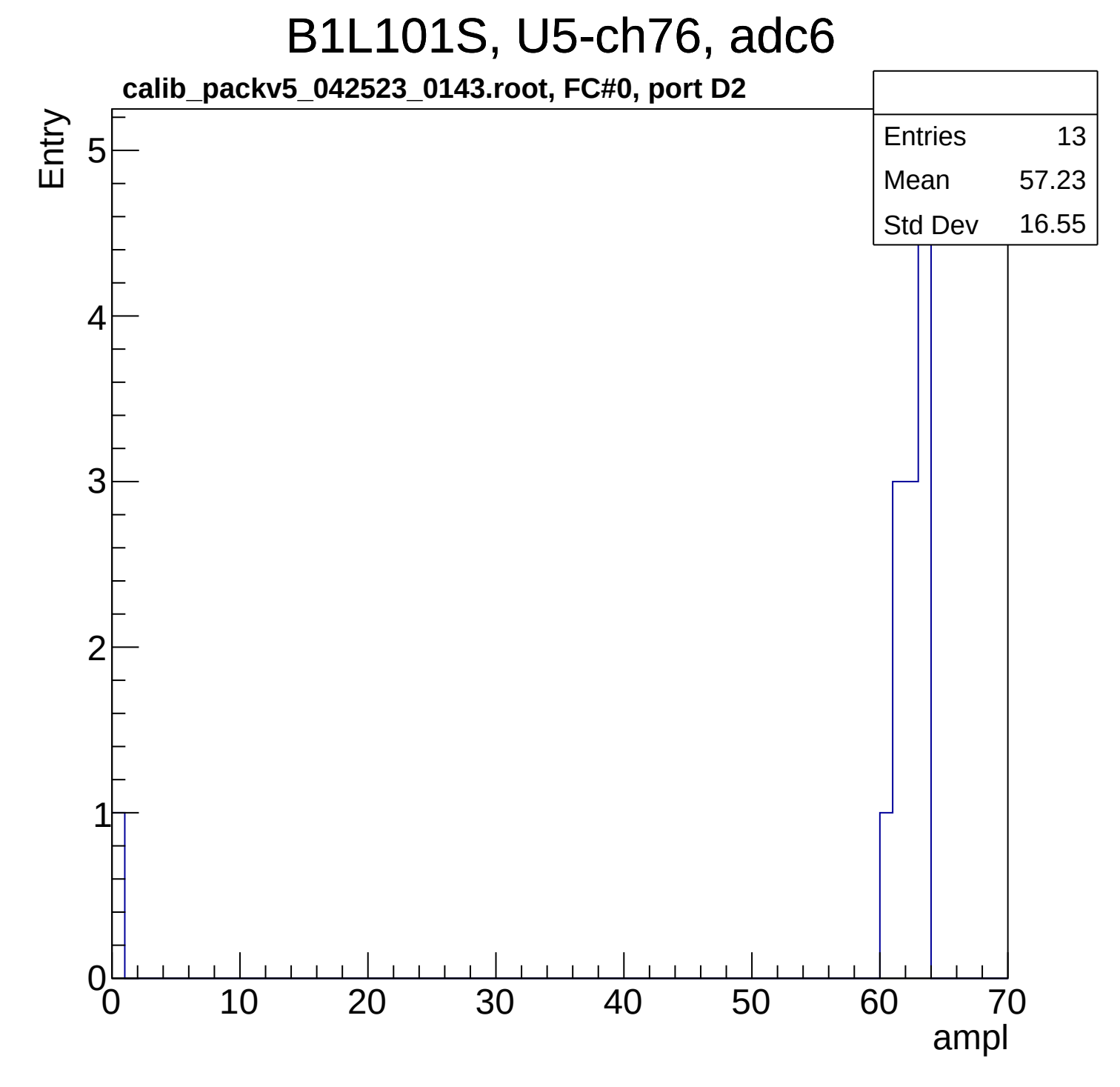
60
70
ampl


B1L101S, U5-ch76, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 13
Mean 57.23
Std Dev 16.55
Entry
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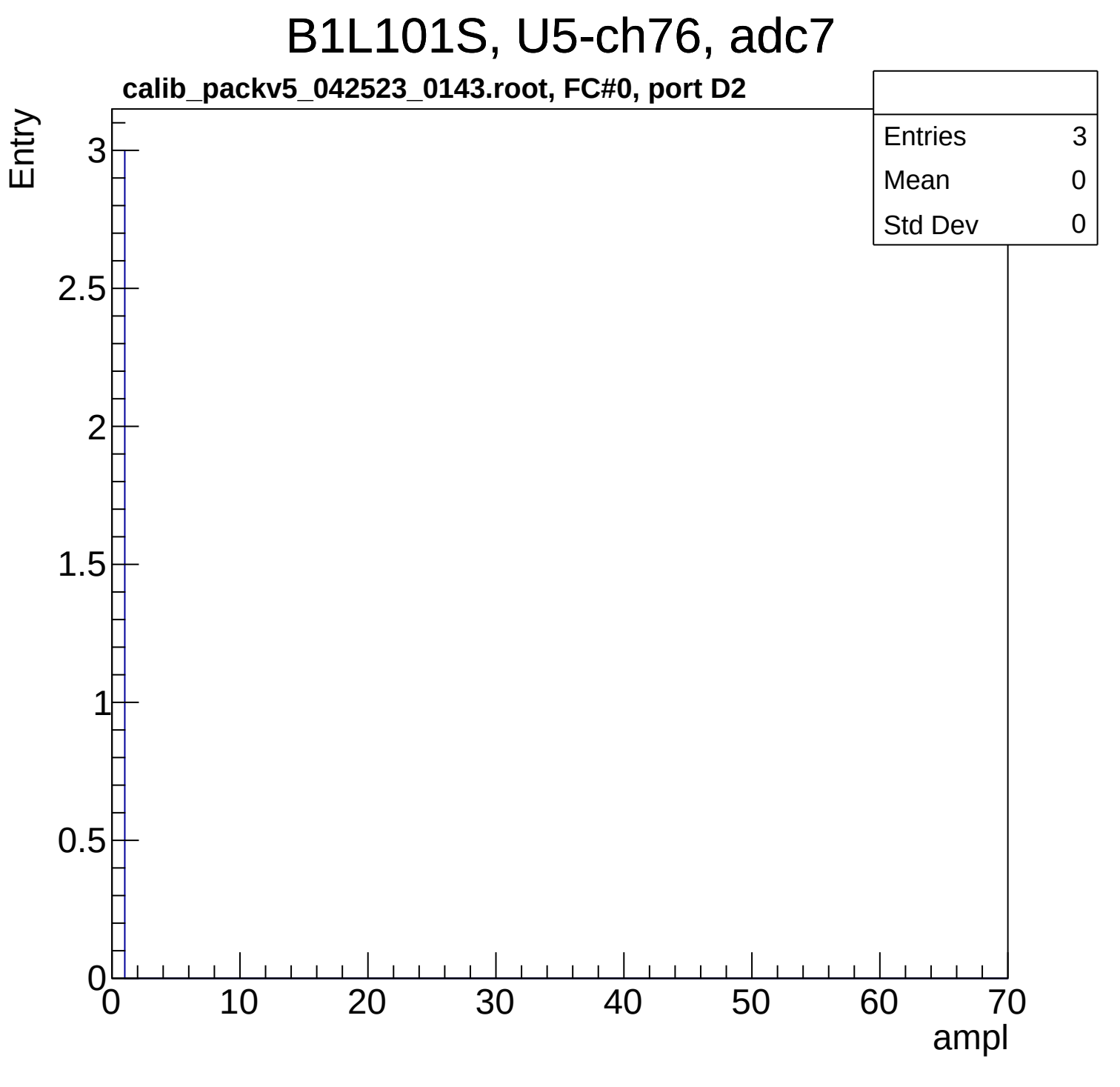
70
ampl


B1L101S, U5-ch76, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 0
Std Dev 0
Entry
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2.5
2
1.5
1
0.5
0
0
10
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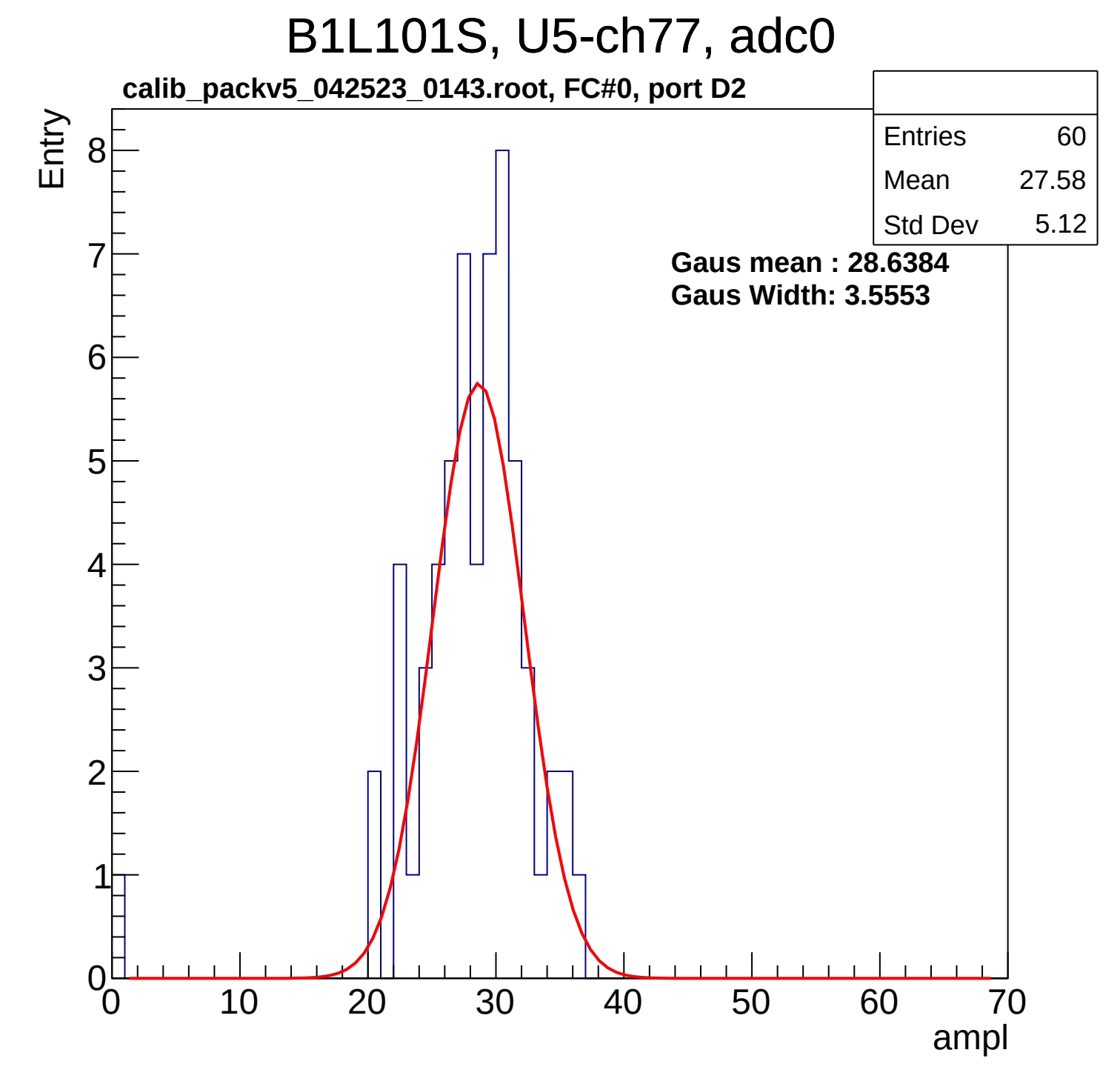
50
60
70
ampl


B1L101S, U5-ch77, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 27.58
Std Dev 5.12
Gaus mean : 28.6384
Gaus Width: 3.5553
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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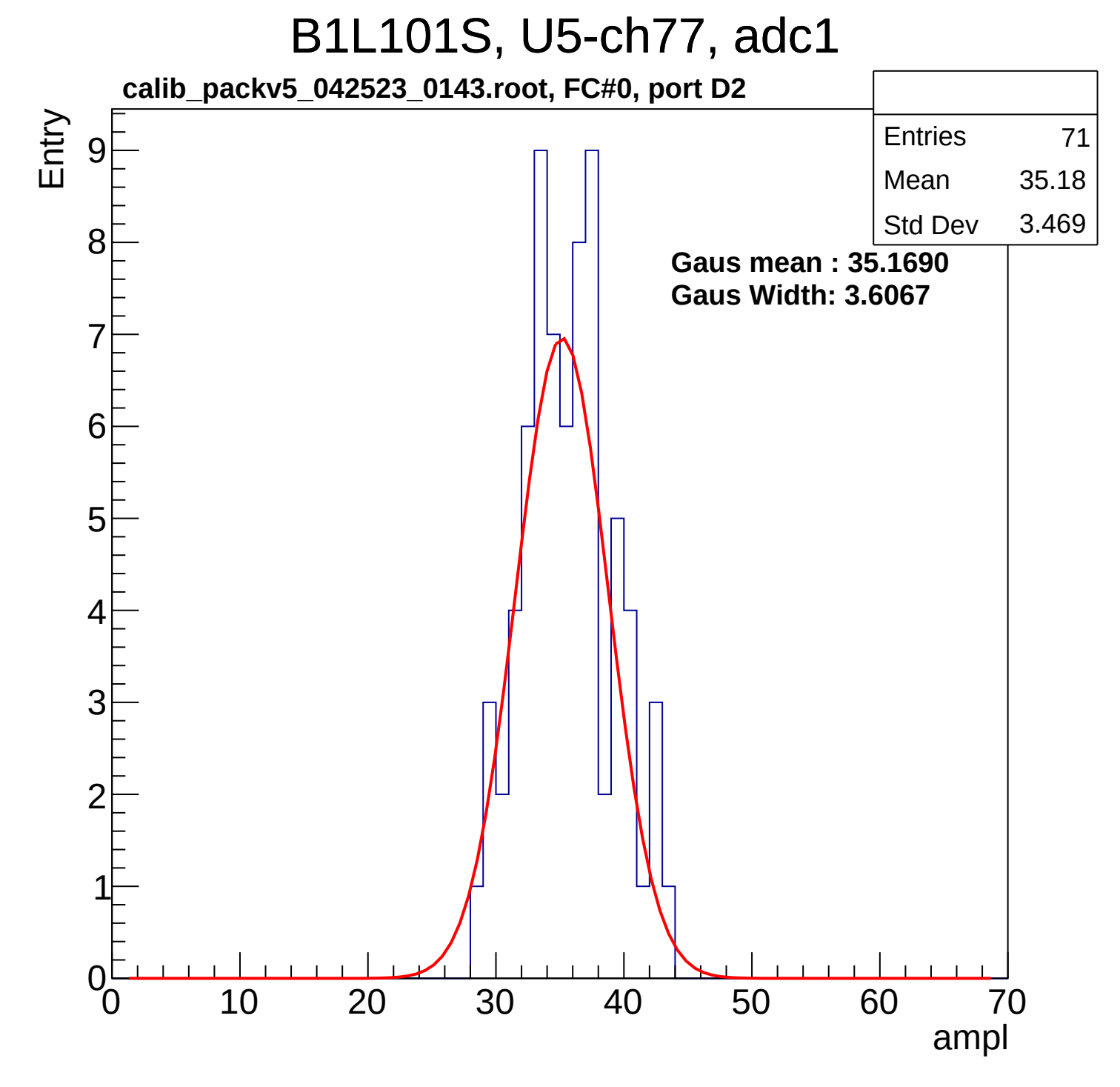
40
50
60
70


B1L101S, U5-ch77, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 35.18
Std Dev 3.469
Gaus mean : 35.1690
Gaus Width: 3.6067
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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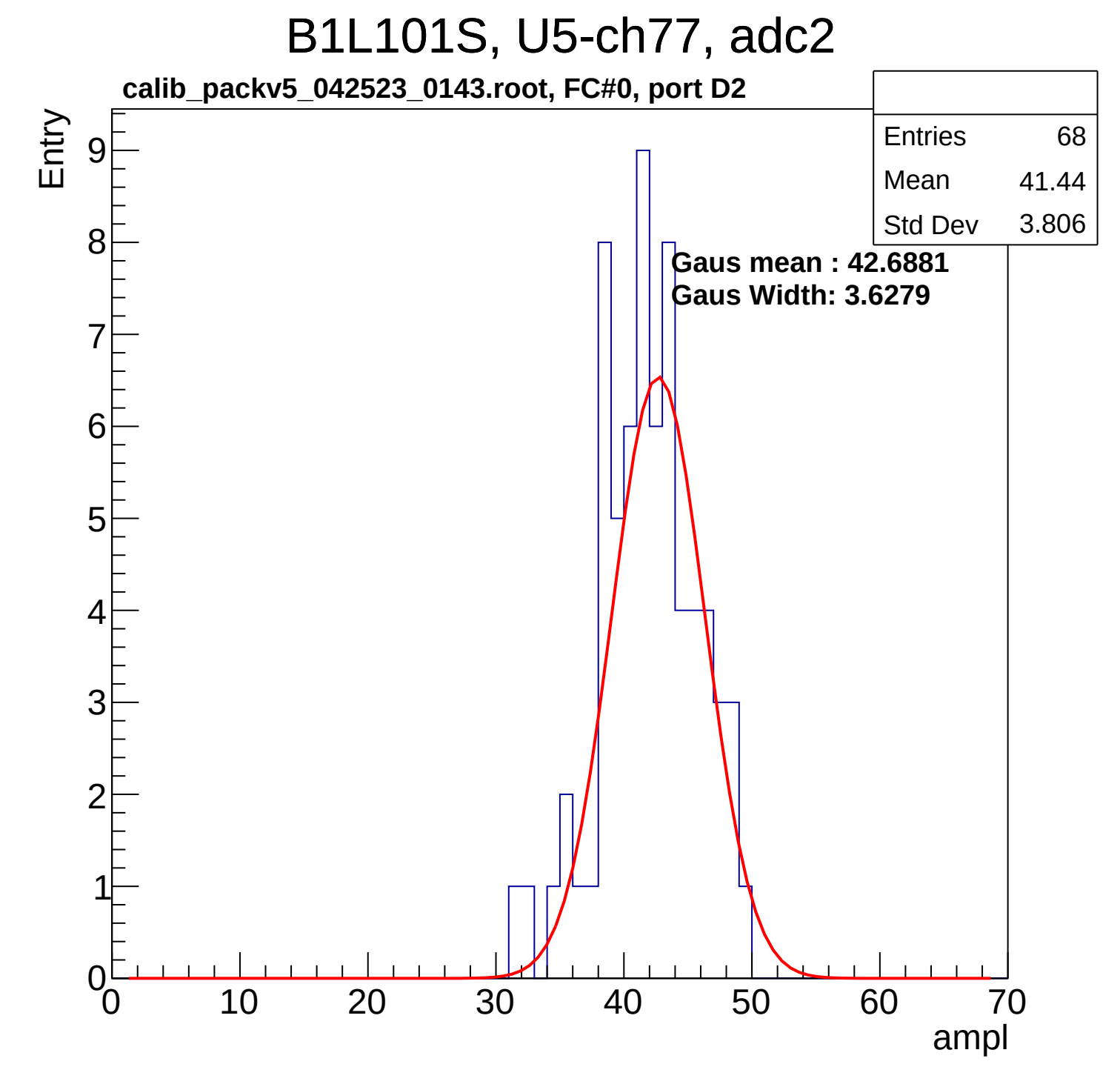
B1L101S, U5-ch77, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 41.44
Std Dev 3.806
Gaus mean : 42.6881
Gaus Width: 3.6279
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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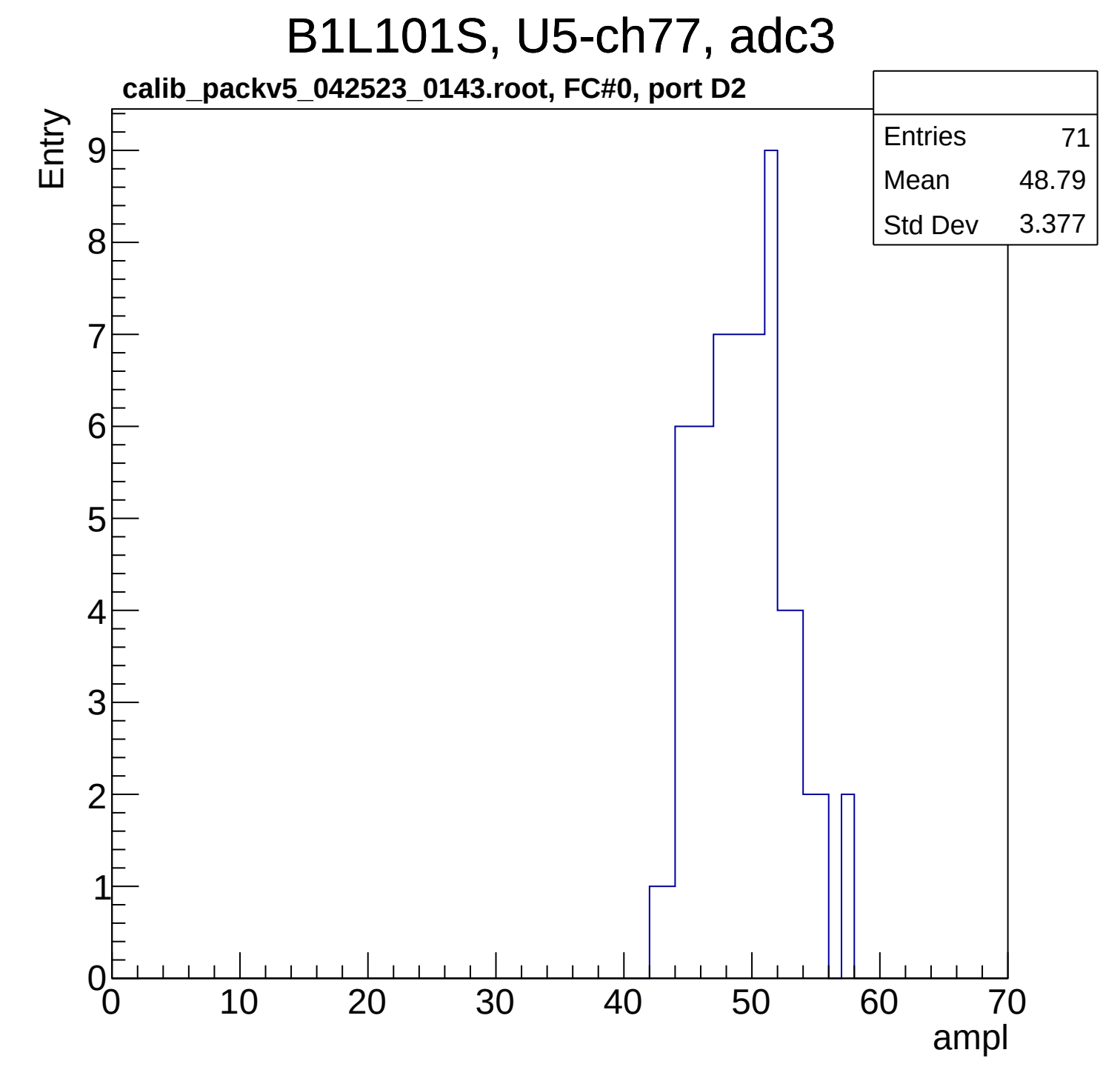
B1L101S, U5-ch77, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 48.79
Std Dev 3.377
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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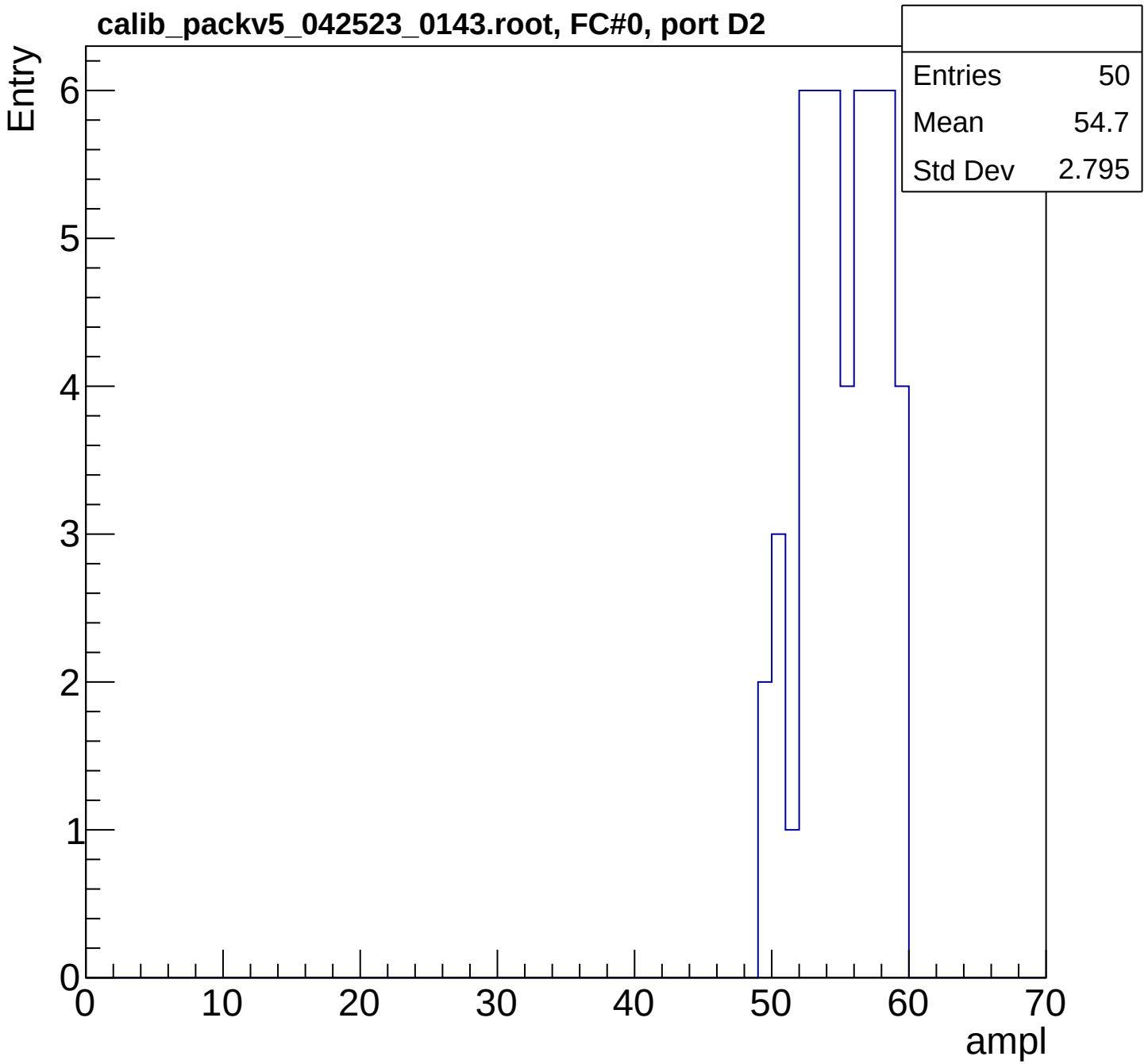
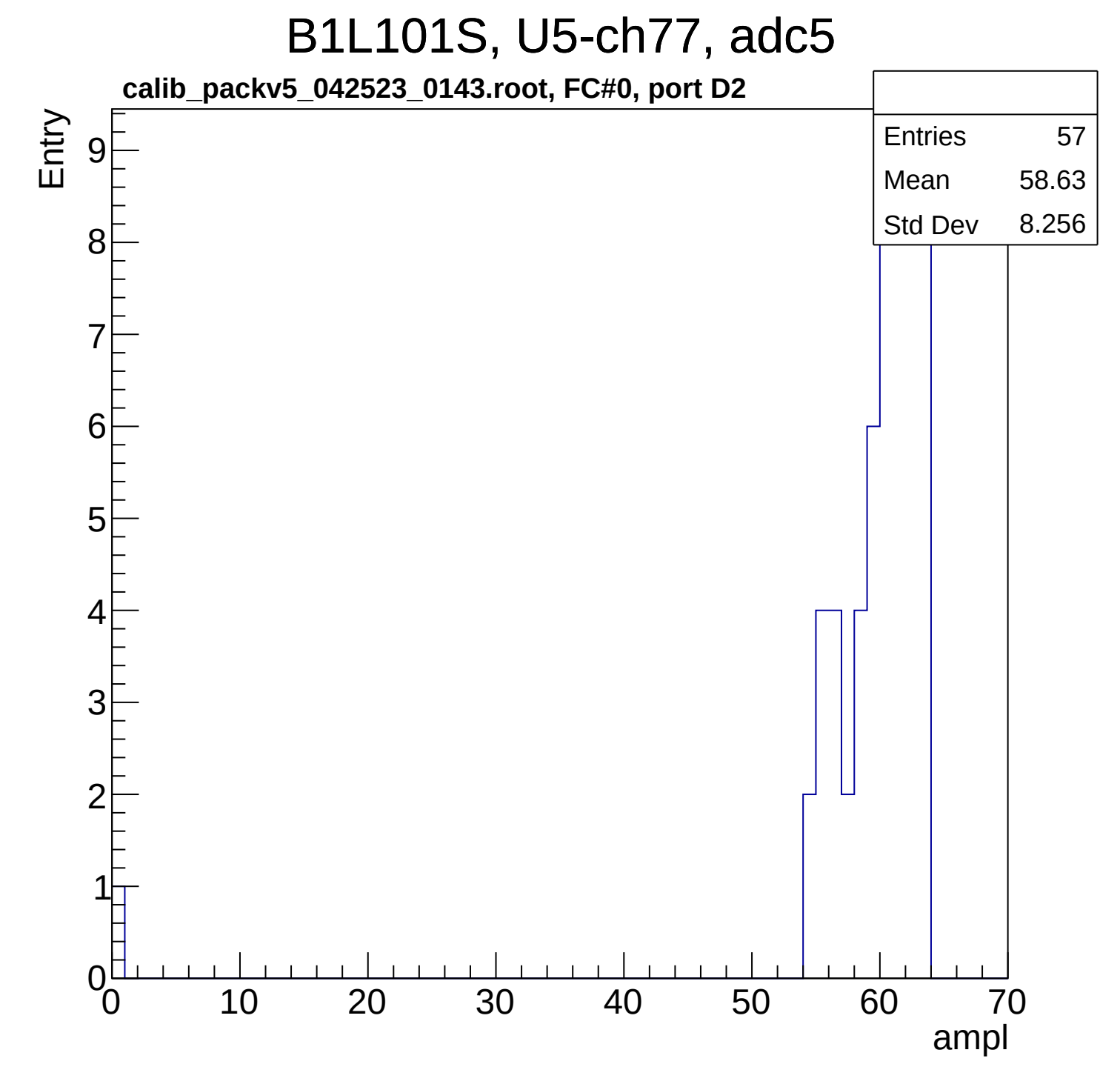

B1L101S, U5-ch77, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 54.7
Std Dev 2.795
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch77, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 58.63
Std Dev 8.256
Entry
ampl
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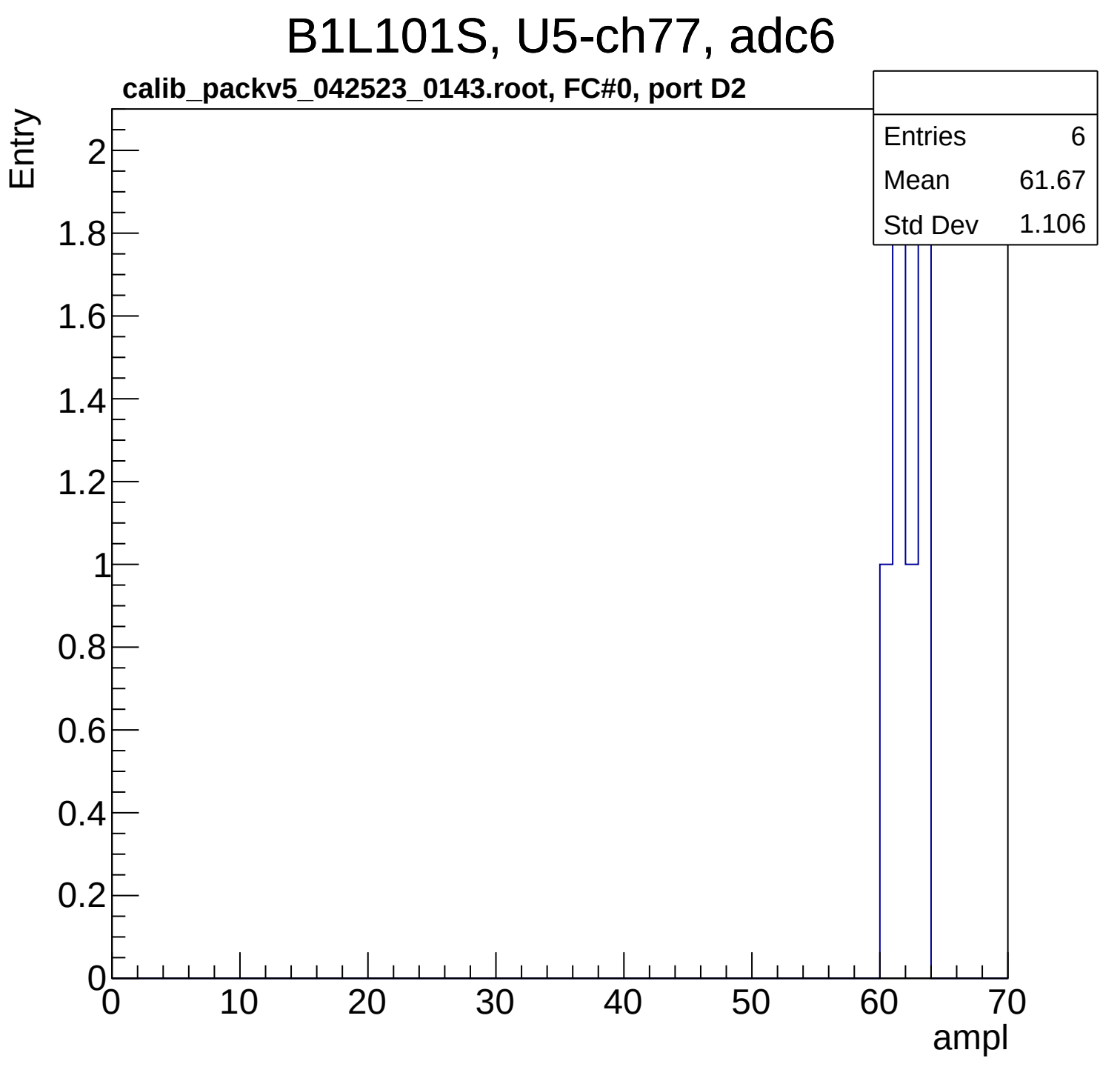
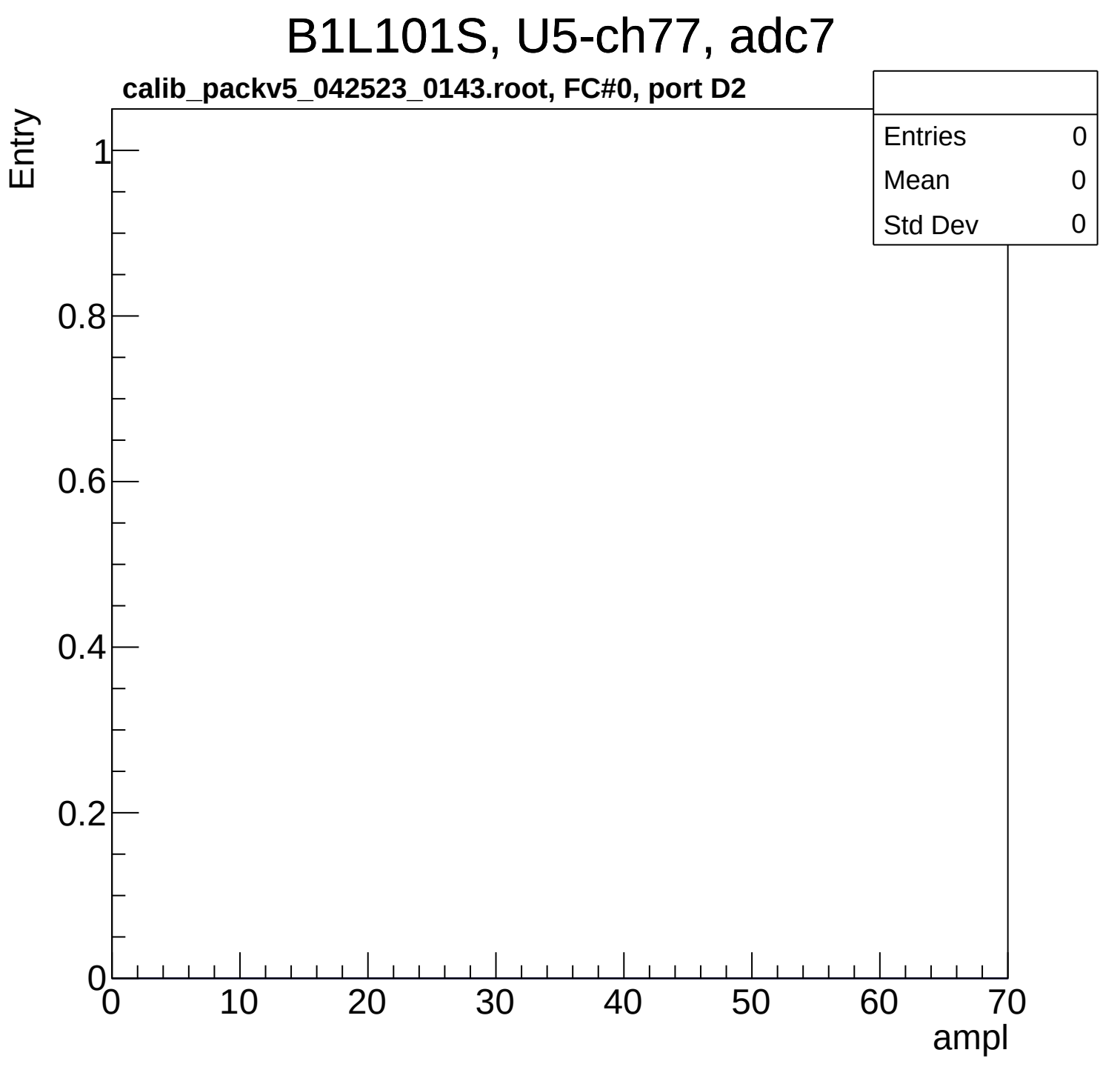
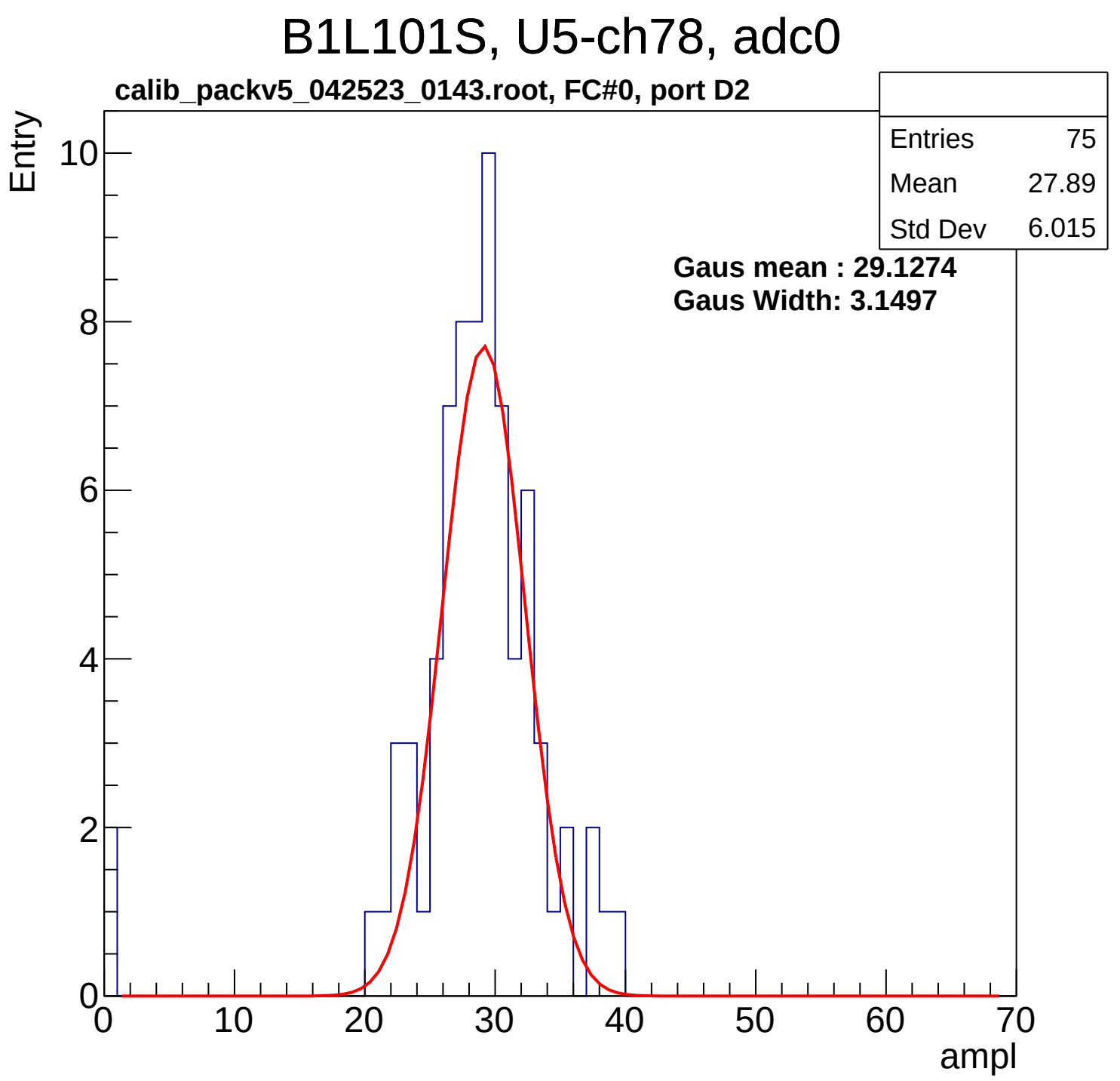
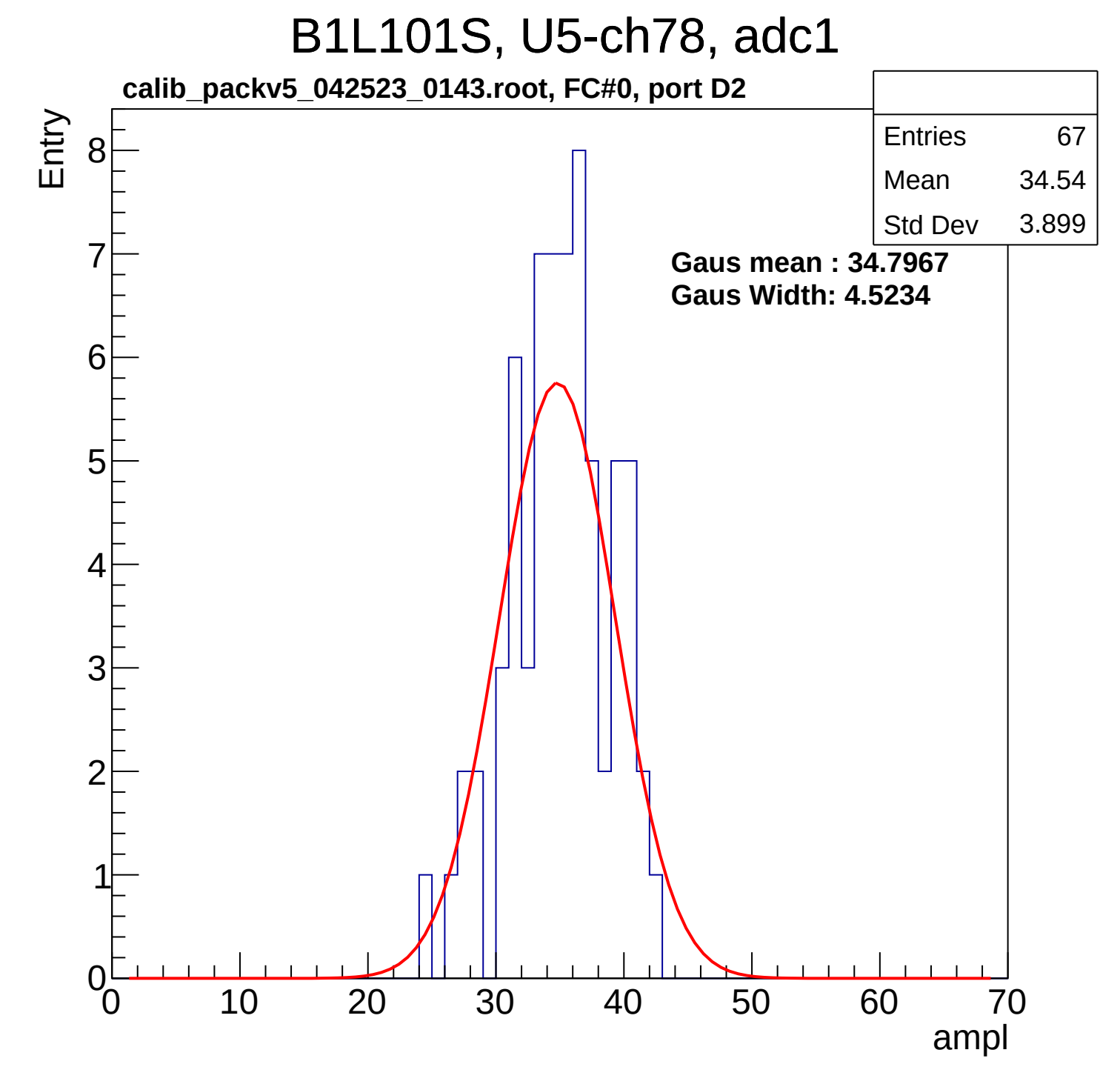
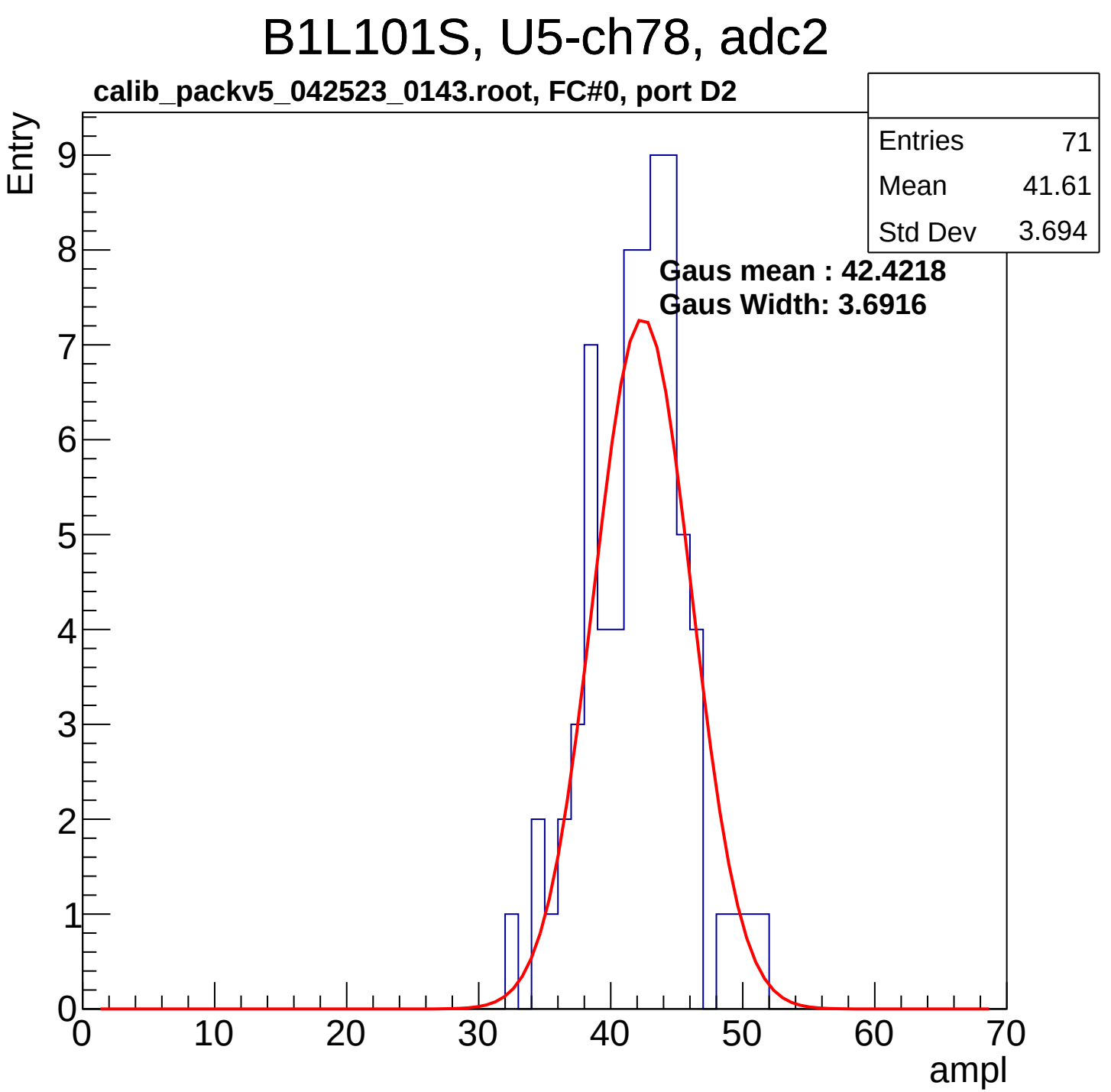
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch77, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 61.67
Std Dev 1.106
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U5-ch77, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch78, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 27.89
Std Dev 6.015
Gaus mean : 29.1274
Gaus Width: 3.1497
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch78, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 34.54
Std Dev 3.899
Gaus mean : 34.7967
Gaus Width: 4.5234
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch78, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 41.61
Std Dev 3.694
Gaus mean : 42.4218
Gaus Width: 3.6916
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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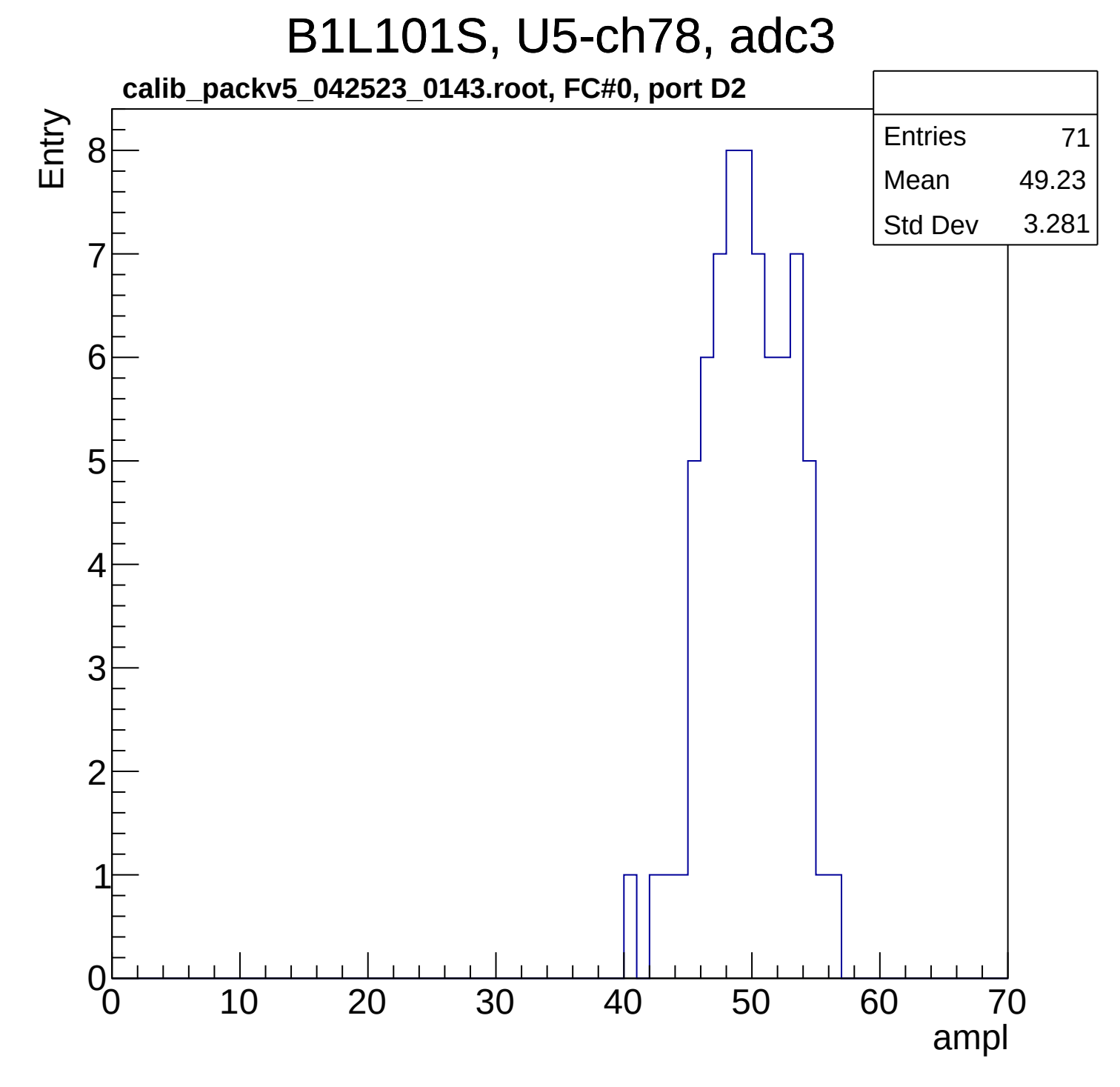
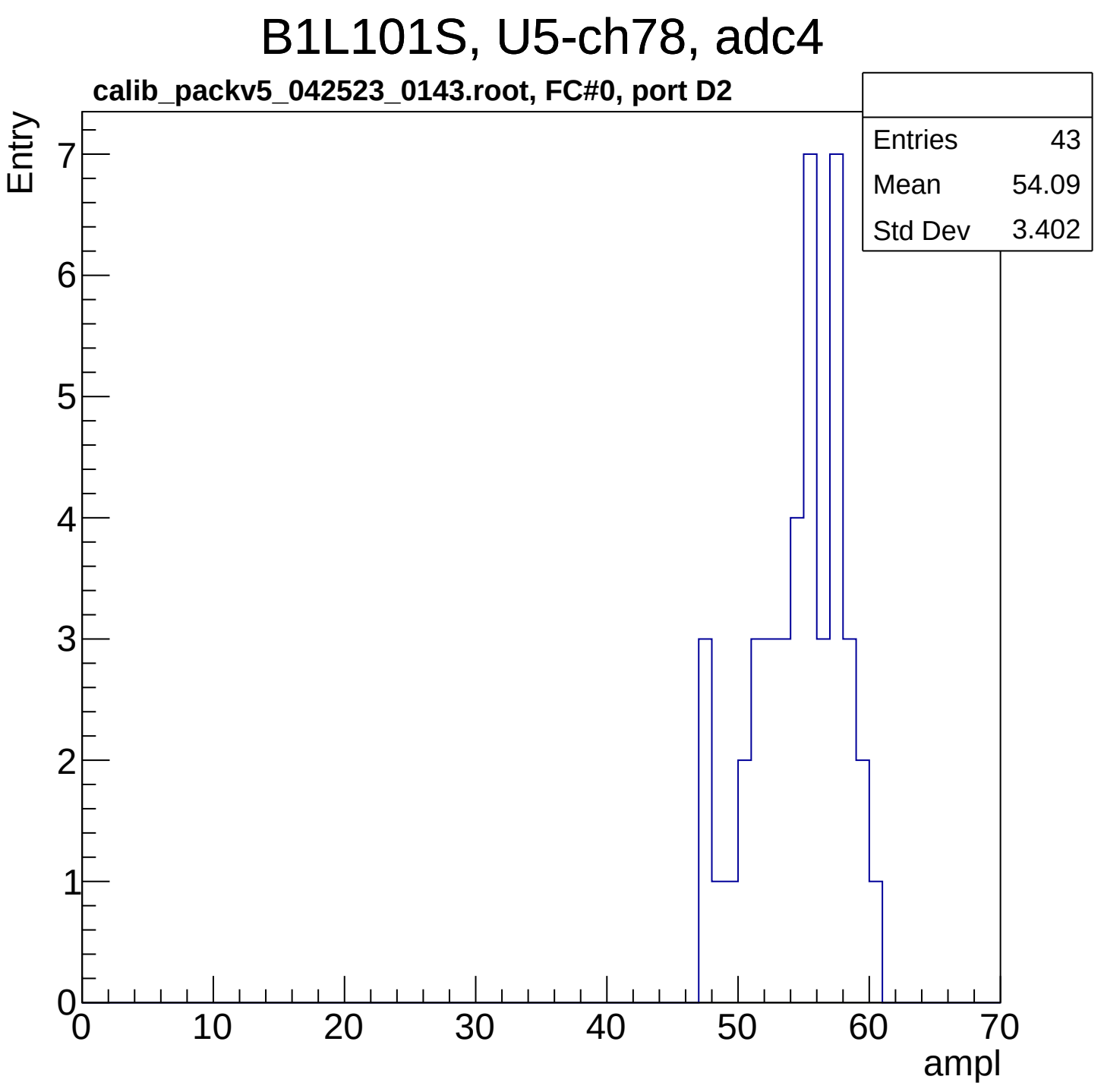
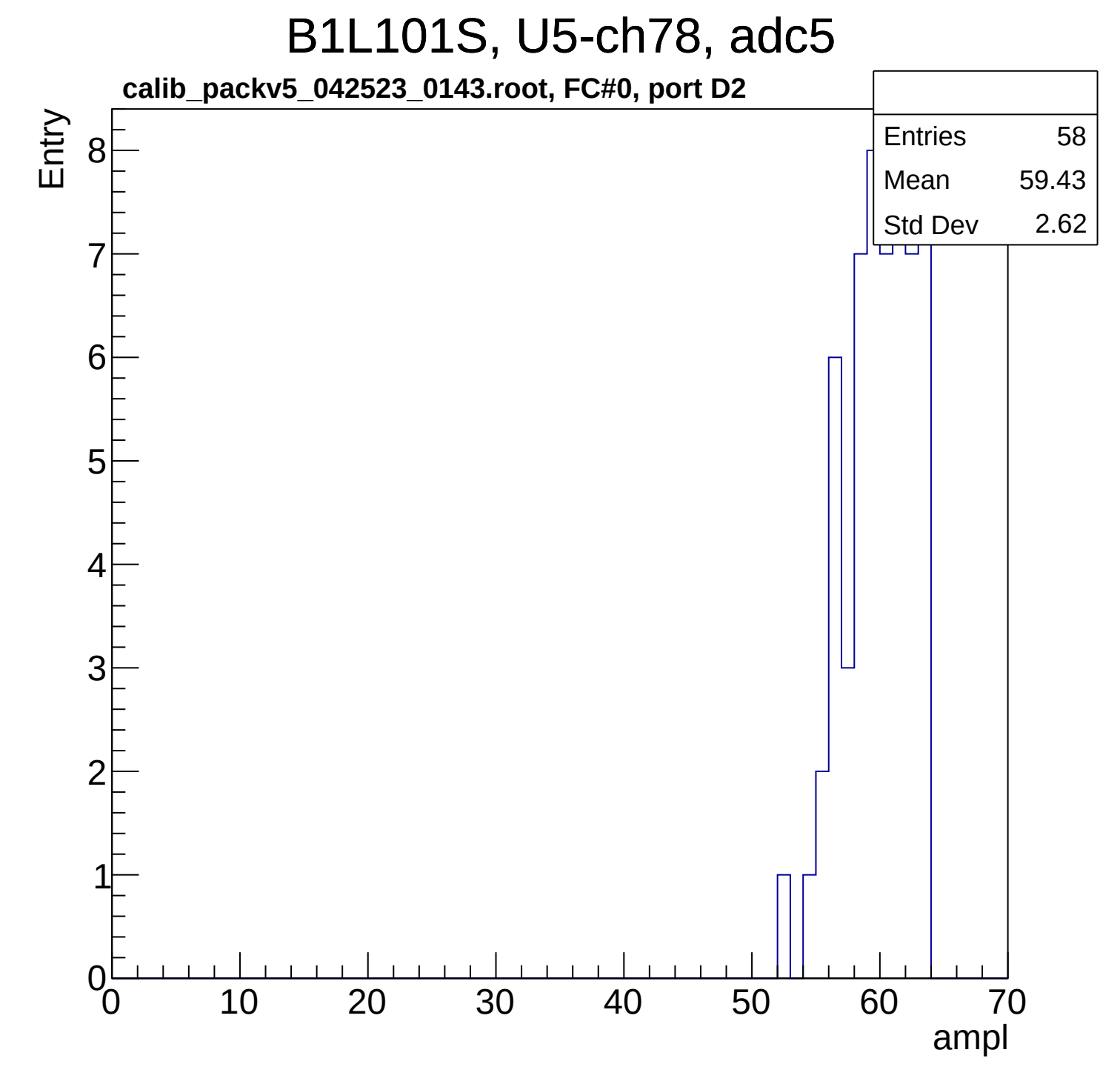
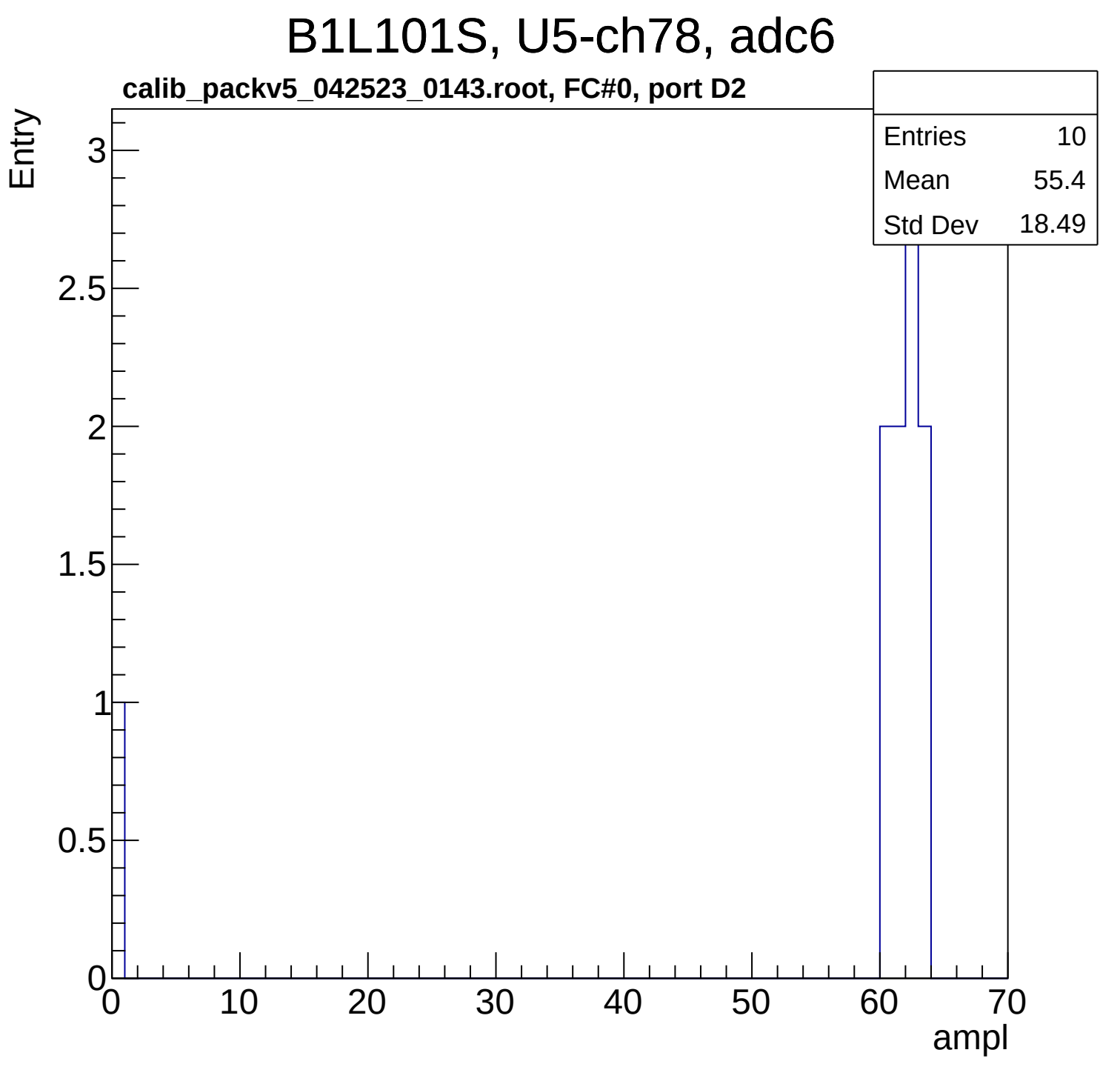
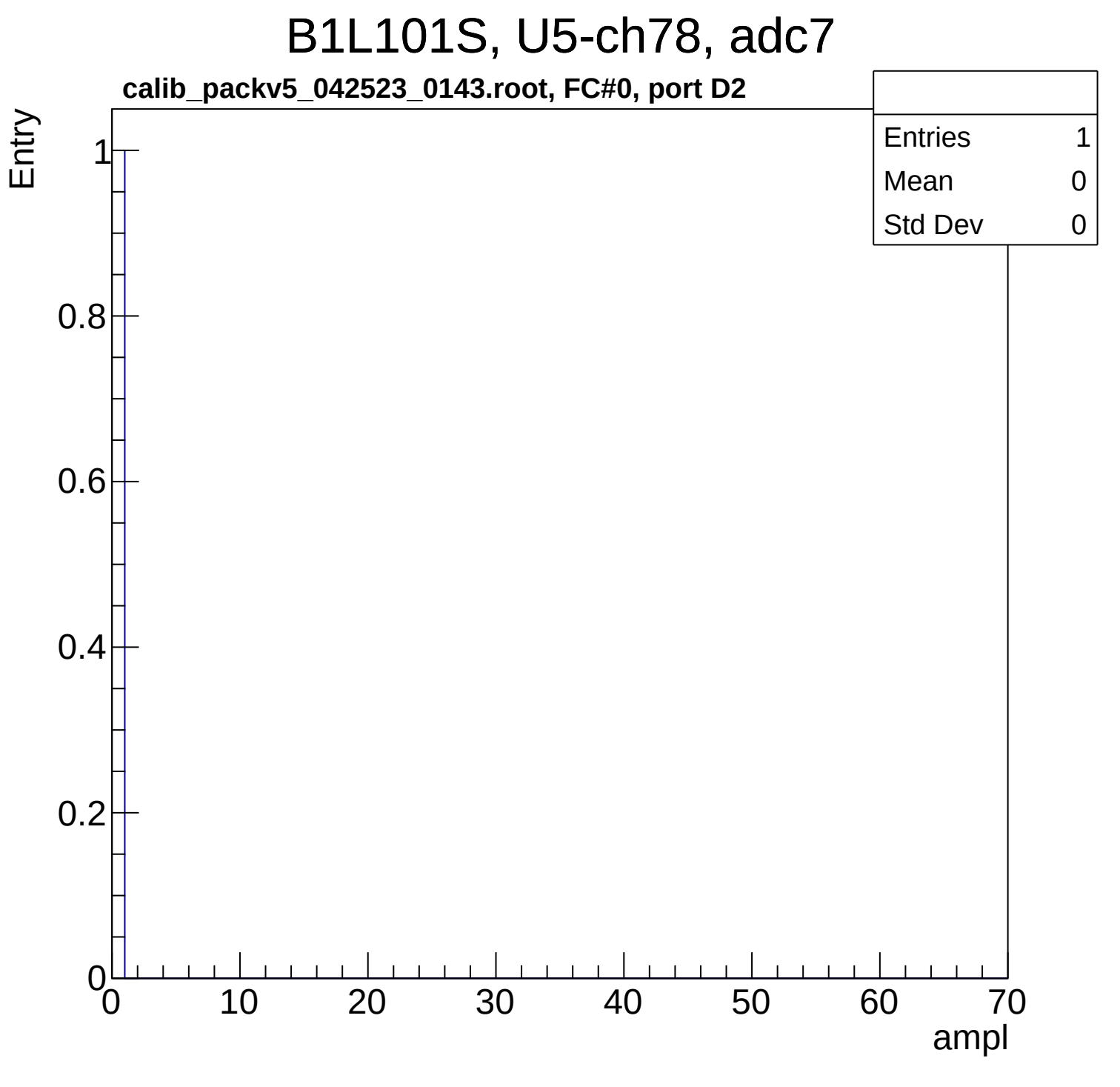
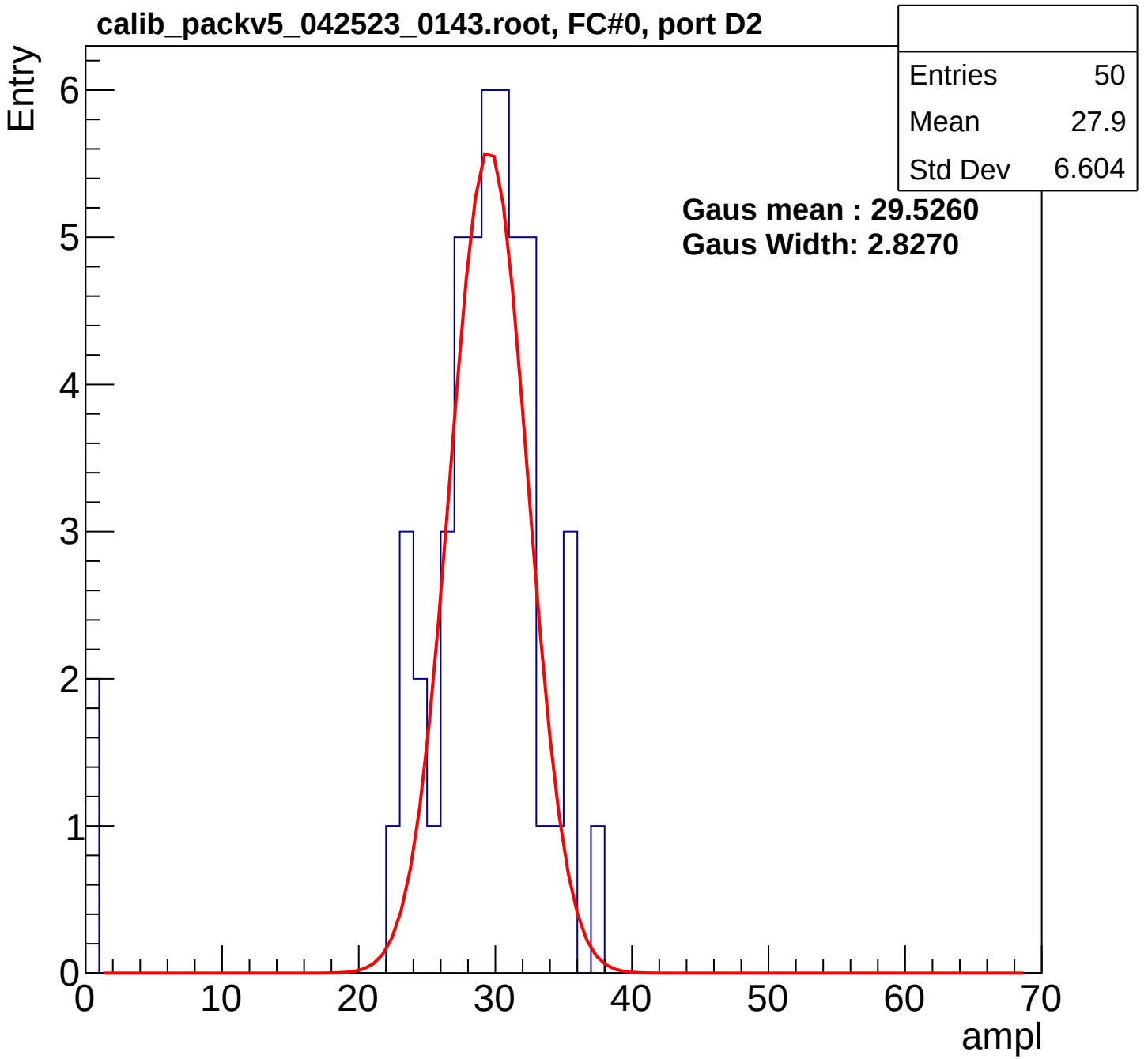

B1L101S, U5-ch78, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 49.23
Std Dev 3.281
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

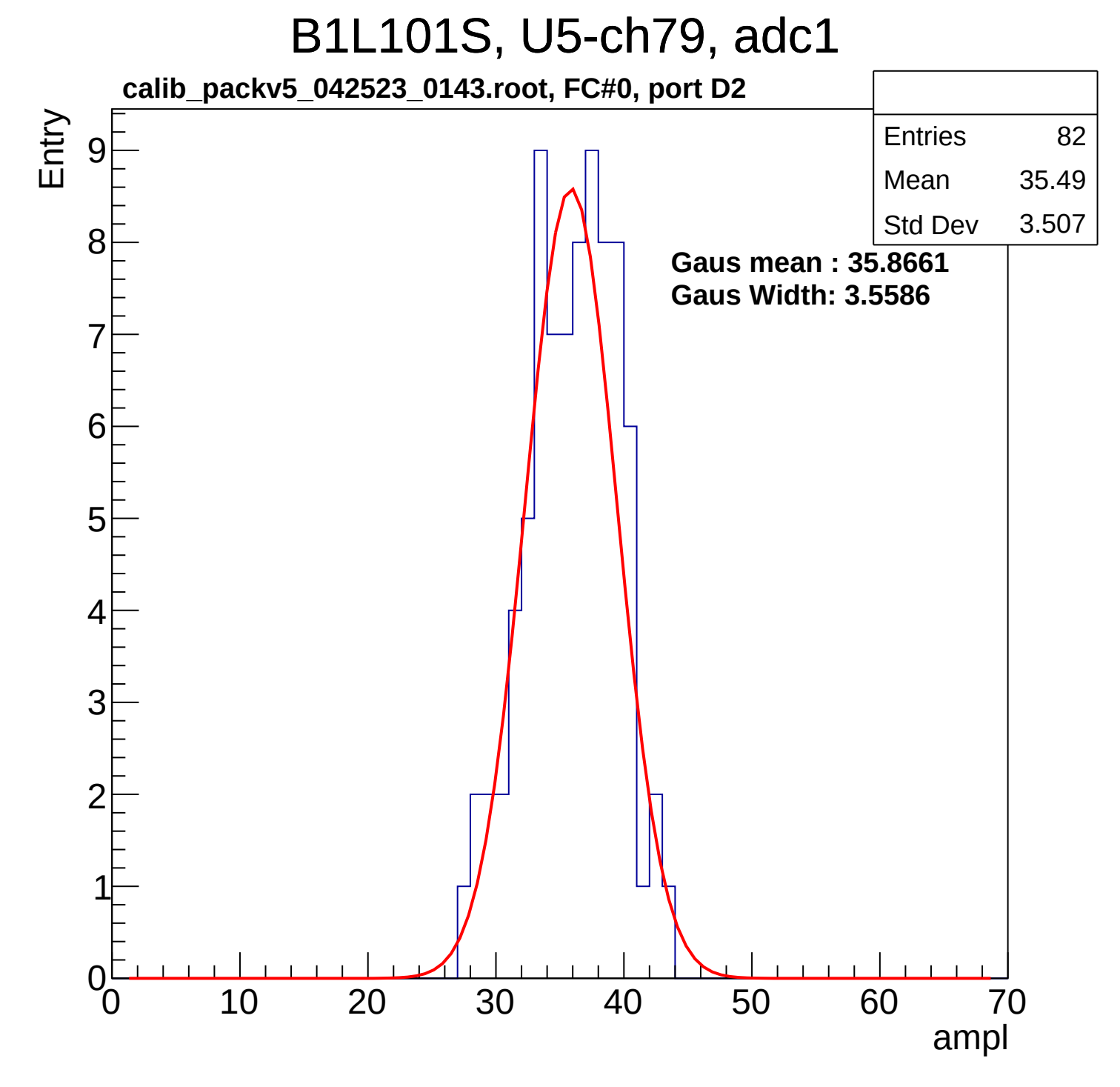

B1L101S, U5-ch78, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 43
Mean 54.09
Std Dev 3.402
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

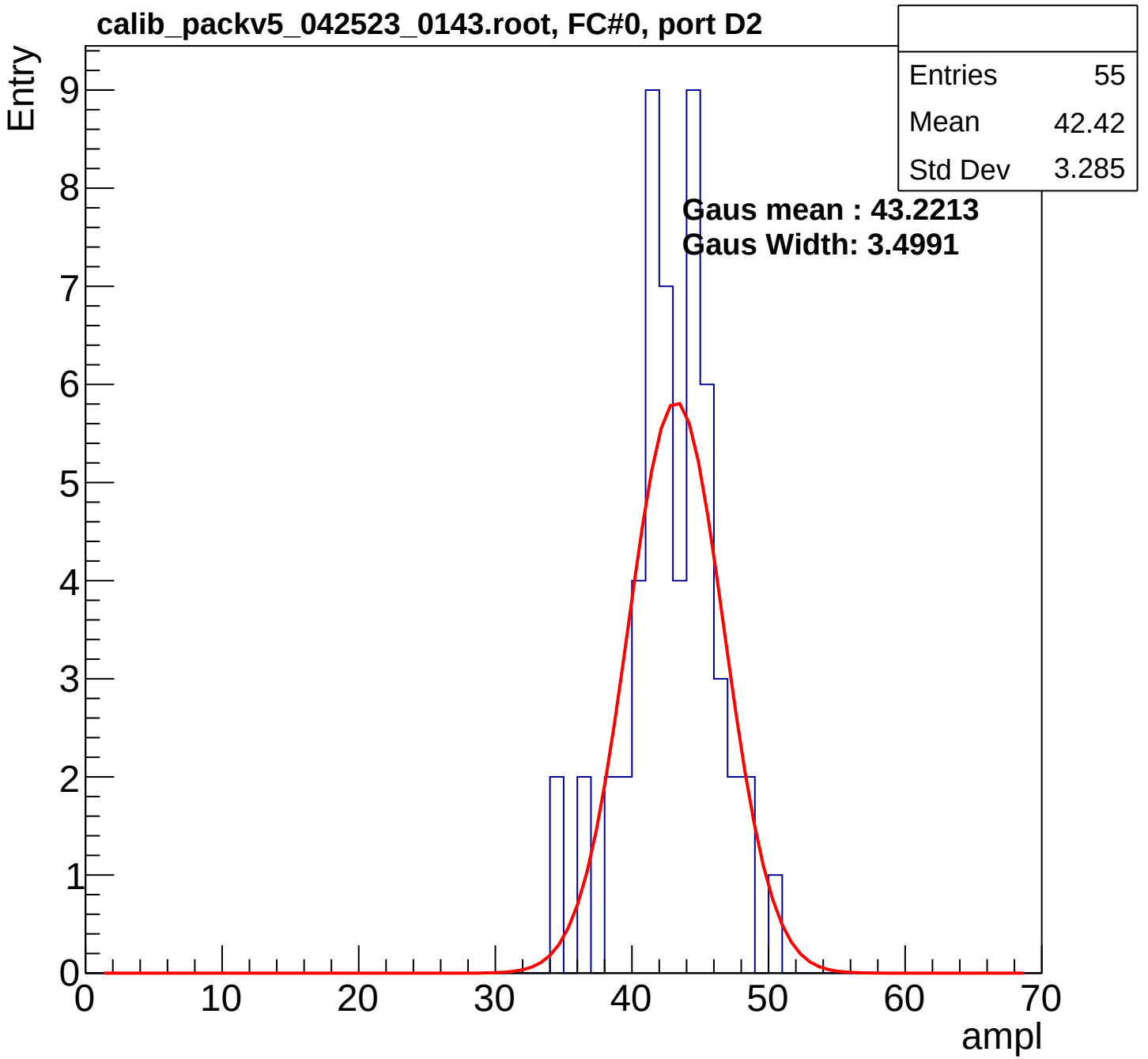

B1L101S, U5-ch78, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 59.43
Std Dev 2.62
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch78, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 55.4
Std Dev 18.49
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch78, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch79, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 27.9
Std Dev 6.604
Gaus mean : 29.5260
Gaus Width: 2.8270
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L101S, U5-ch79, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 82
Mean 35.49
Std Dev 3.507
Gaus mean : 35.8661
Gaus Width: 3.5586
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch79, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 42.42
Std Dev 3.285
Gaus mean : 43.2213
Gaus Width: 3.4991
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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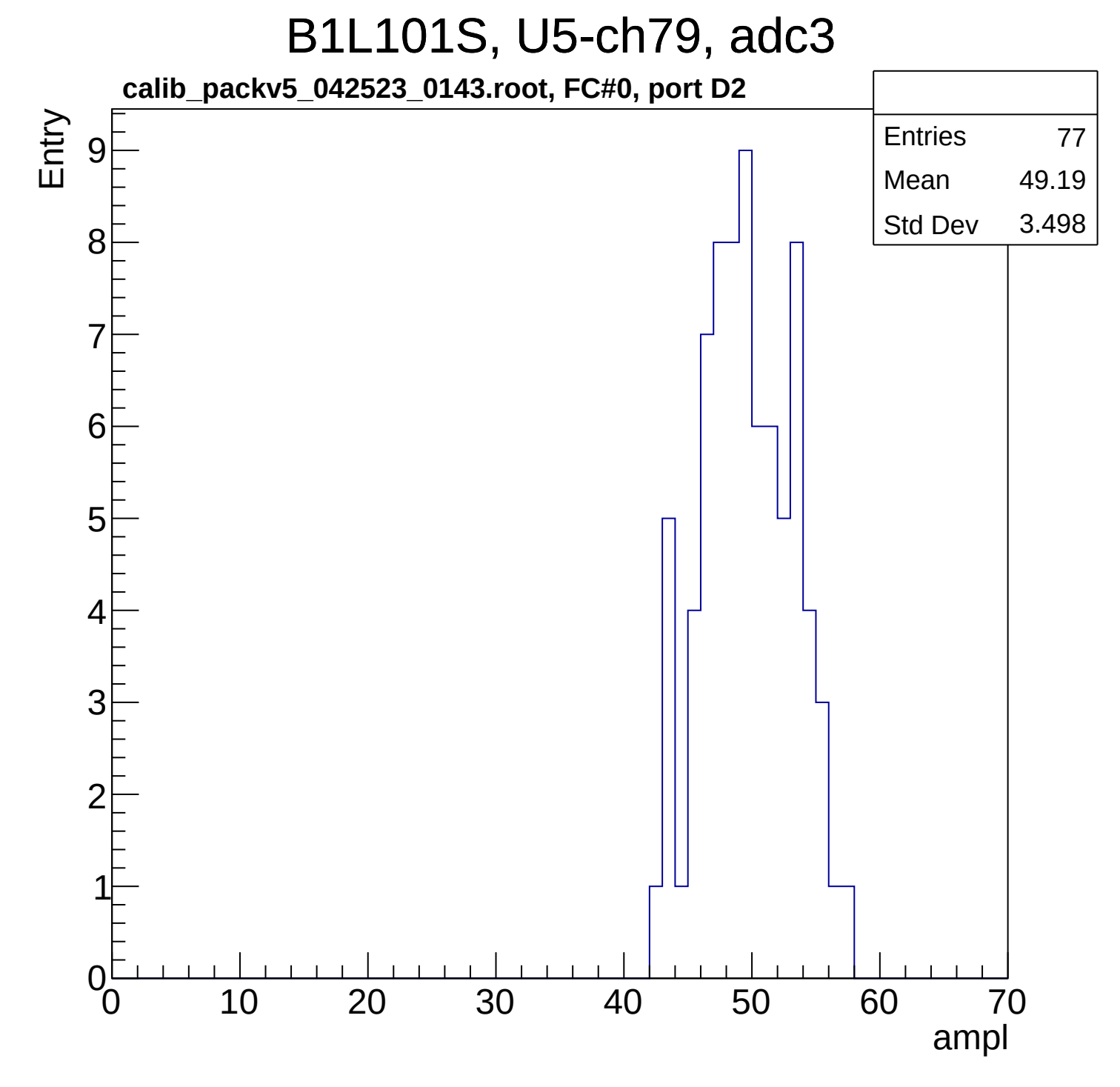
B1L101S, U5-ch79, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 49.19
Std Dev 3.498
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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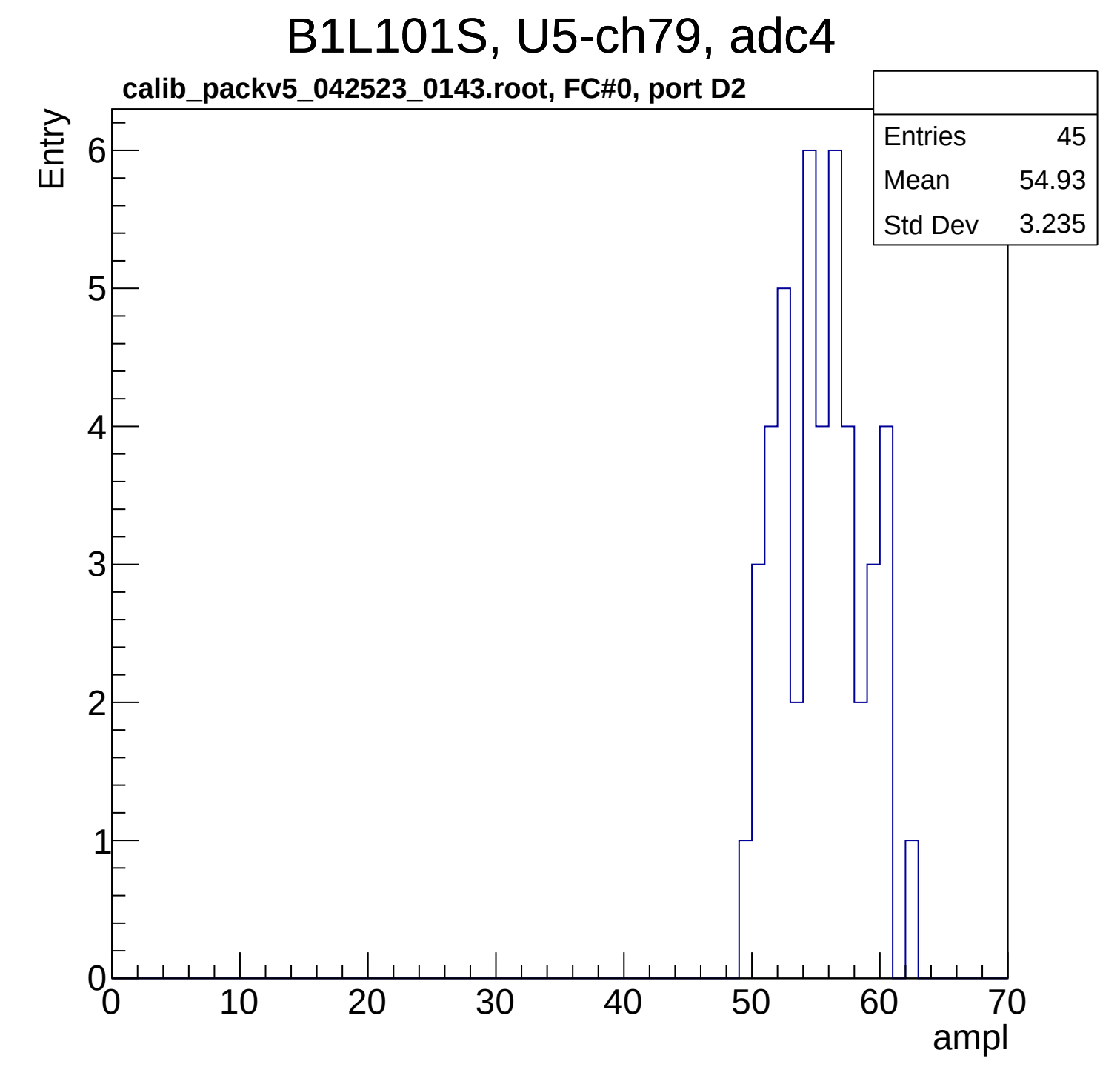
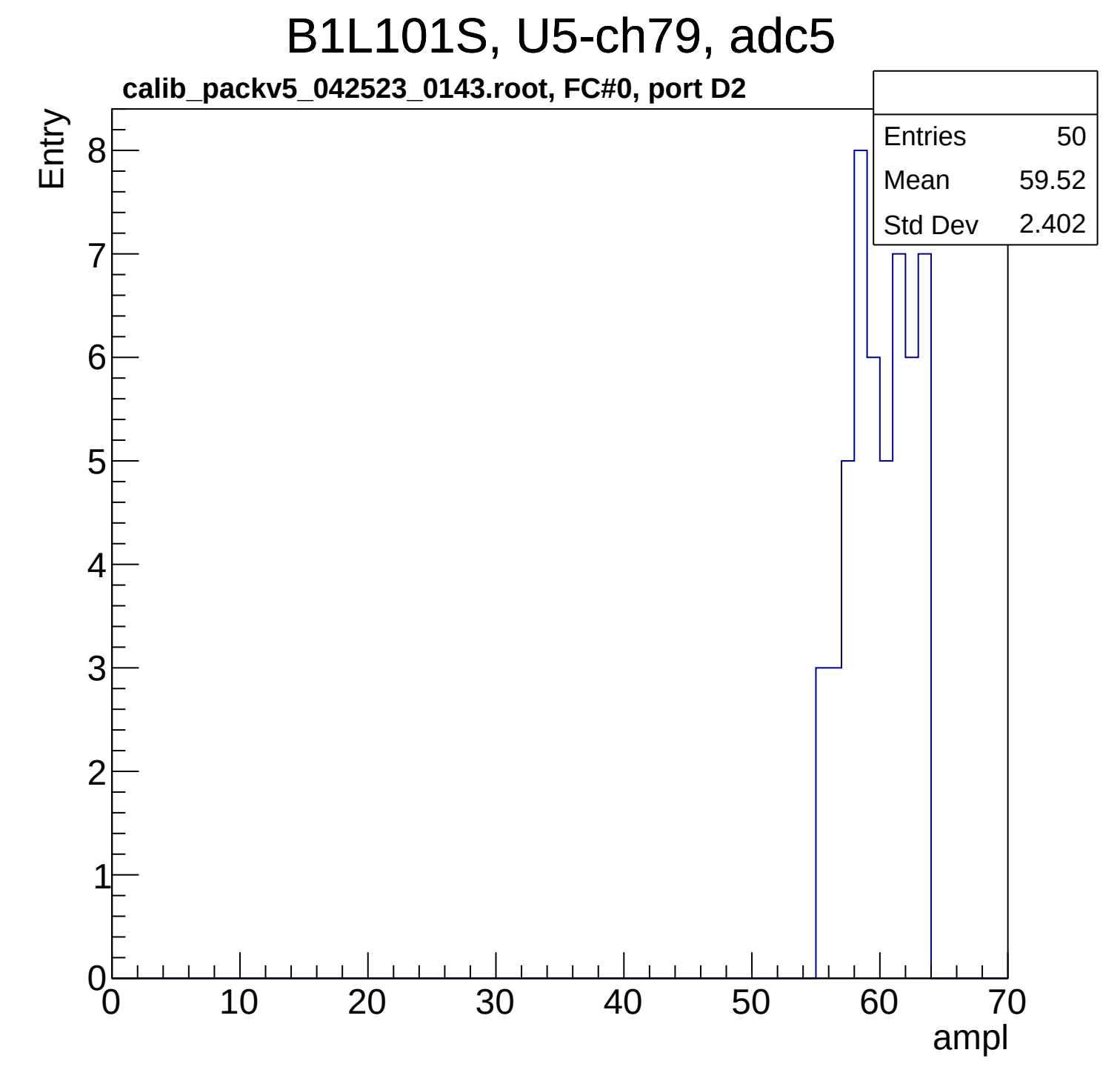

B1L101S, U5-ch79, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 54.93
Std Dev 3.235
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L101S, U5-ch79, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 59.52
Std Dev 2.402
Entry
ampl
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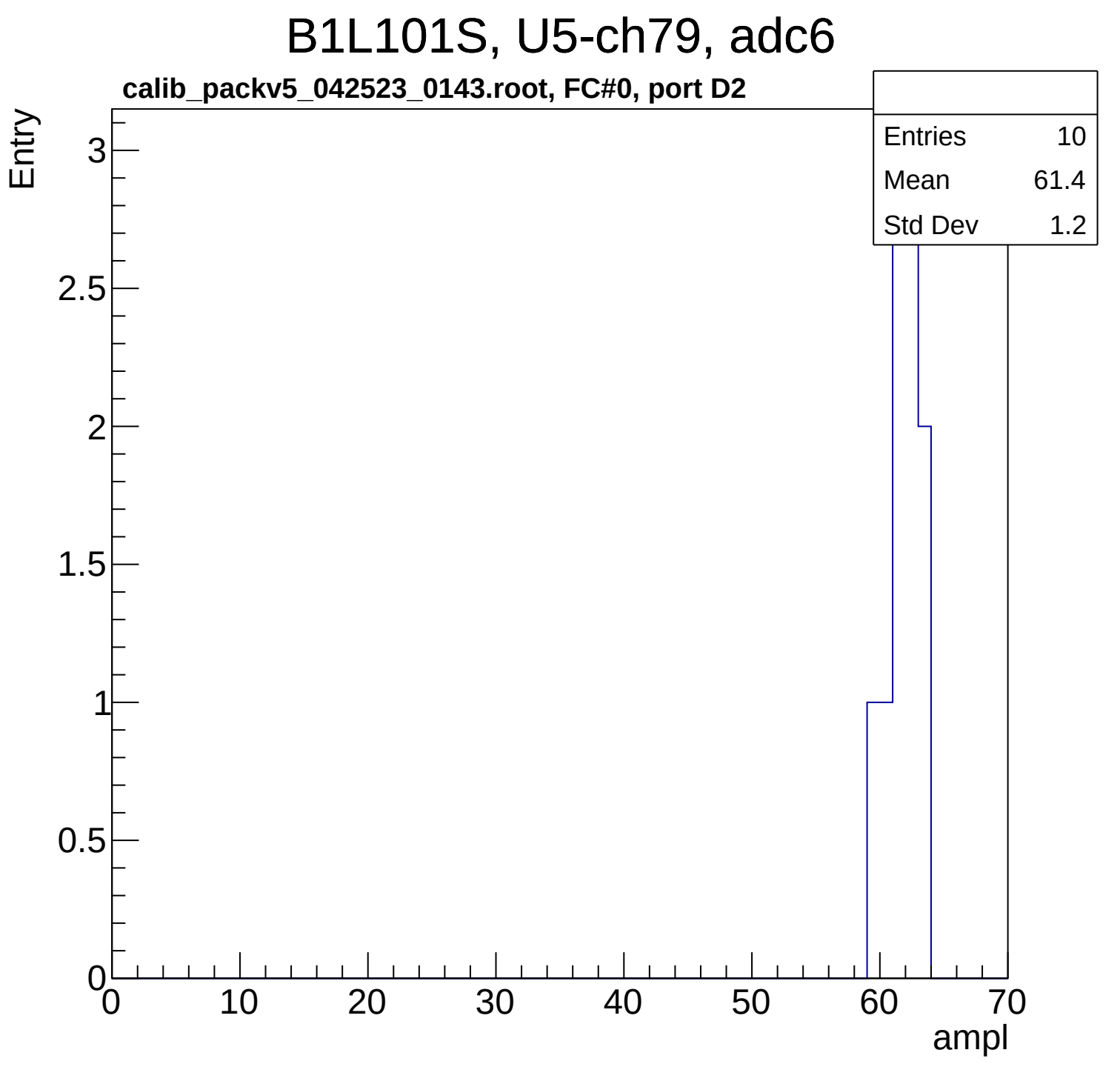
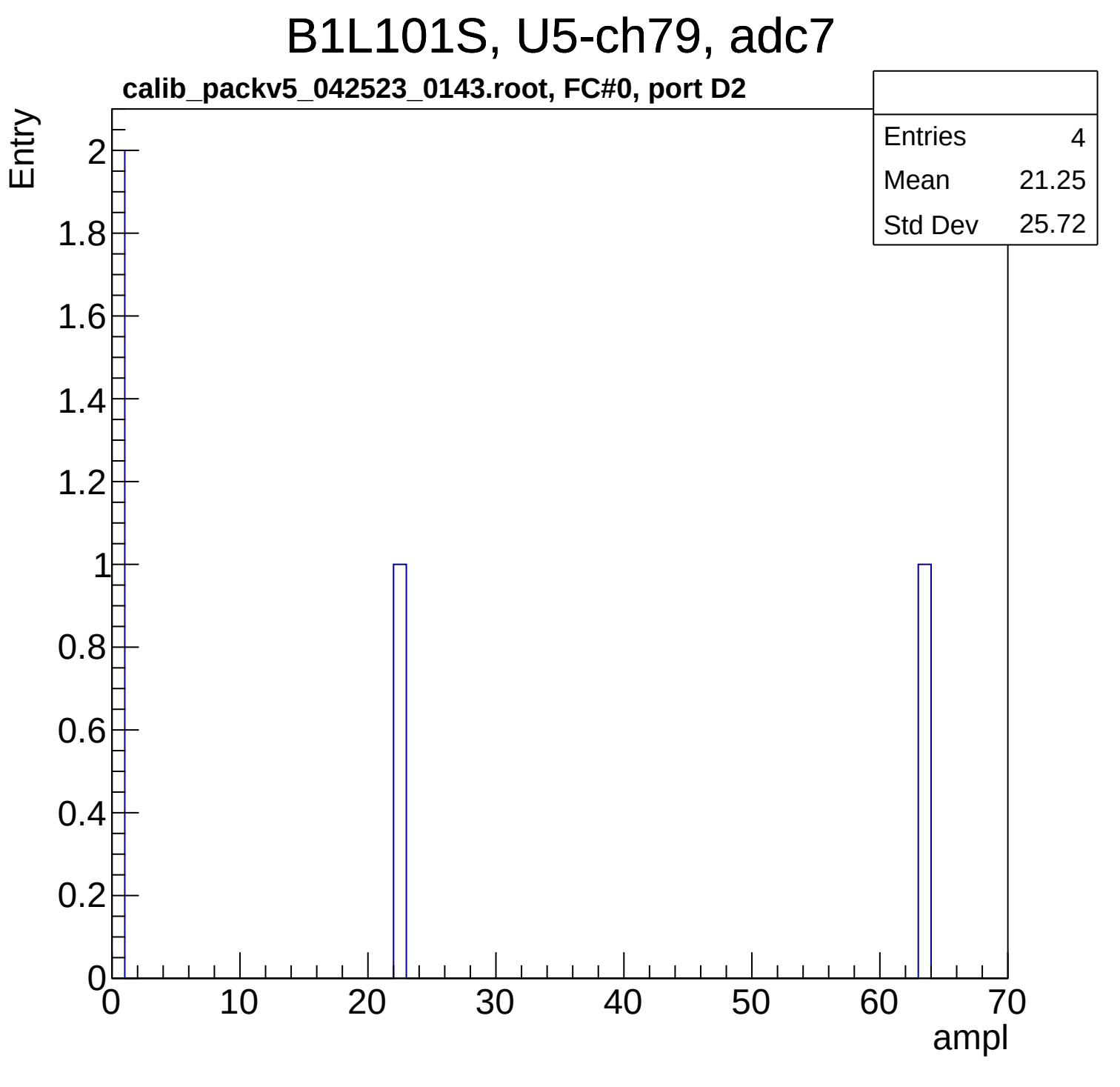
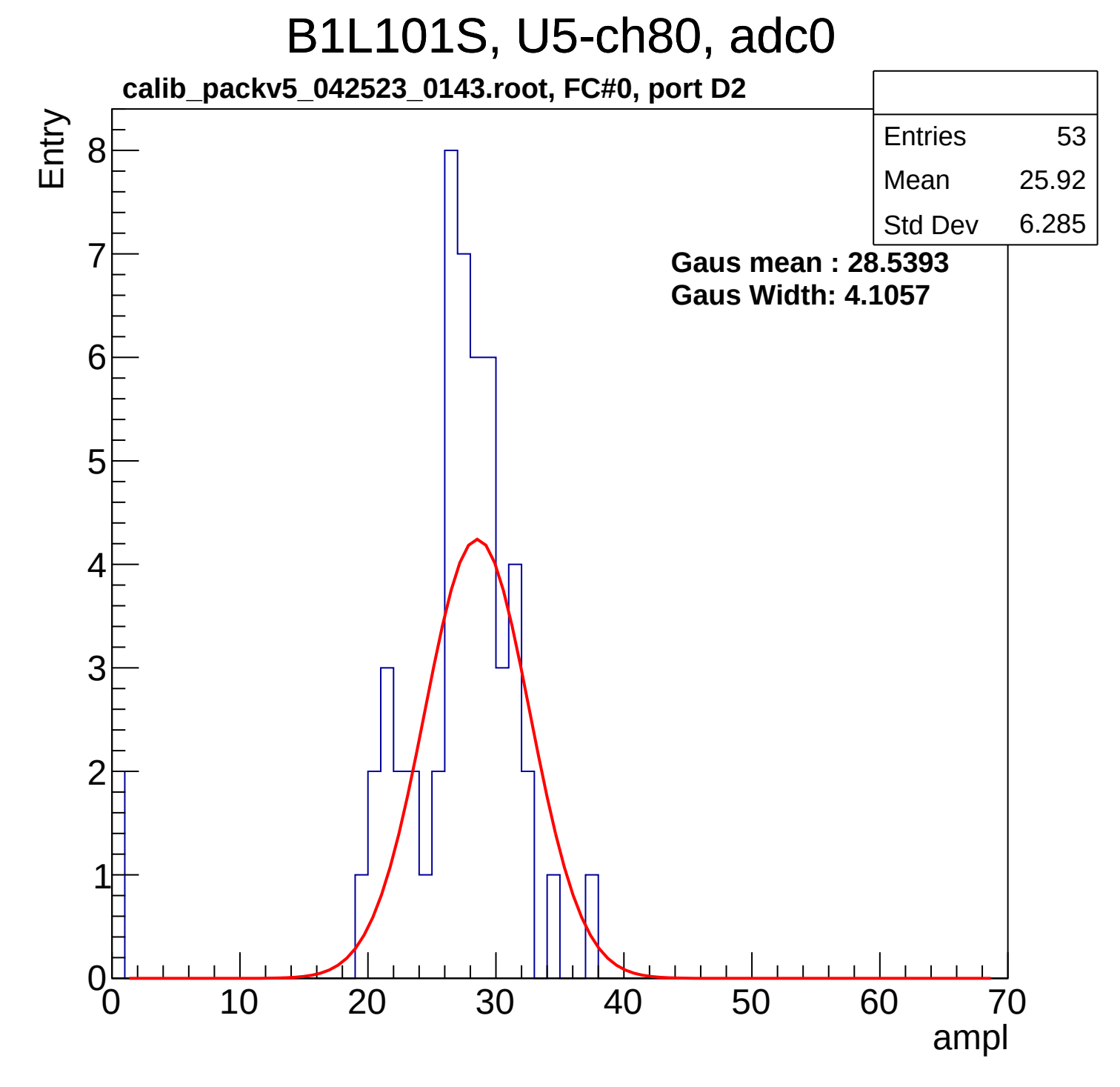
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch79, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 61.4
Std Dev 1.2
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch79, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 21.25
Std Dev 25.72
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U5-ch80, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 25.92
Std Dev 6.285
Gaus mean : 28.5393
Gaus Width: 4.1057
Entry
ampl
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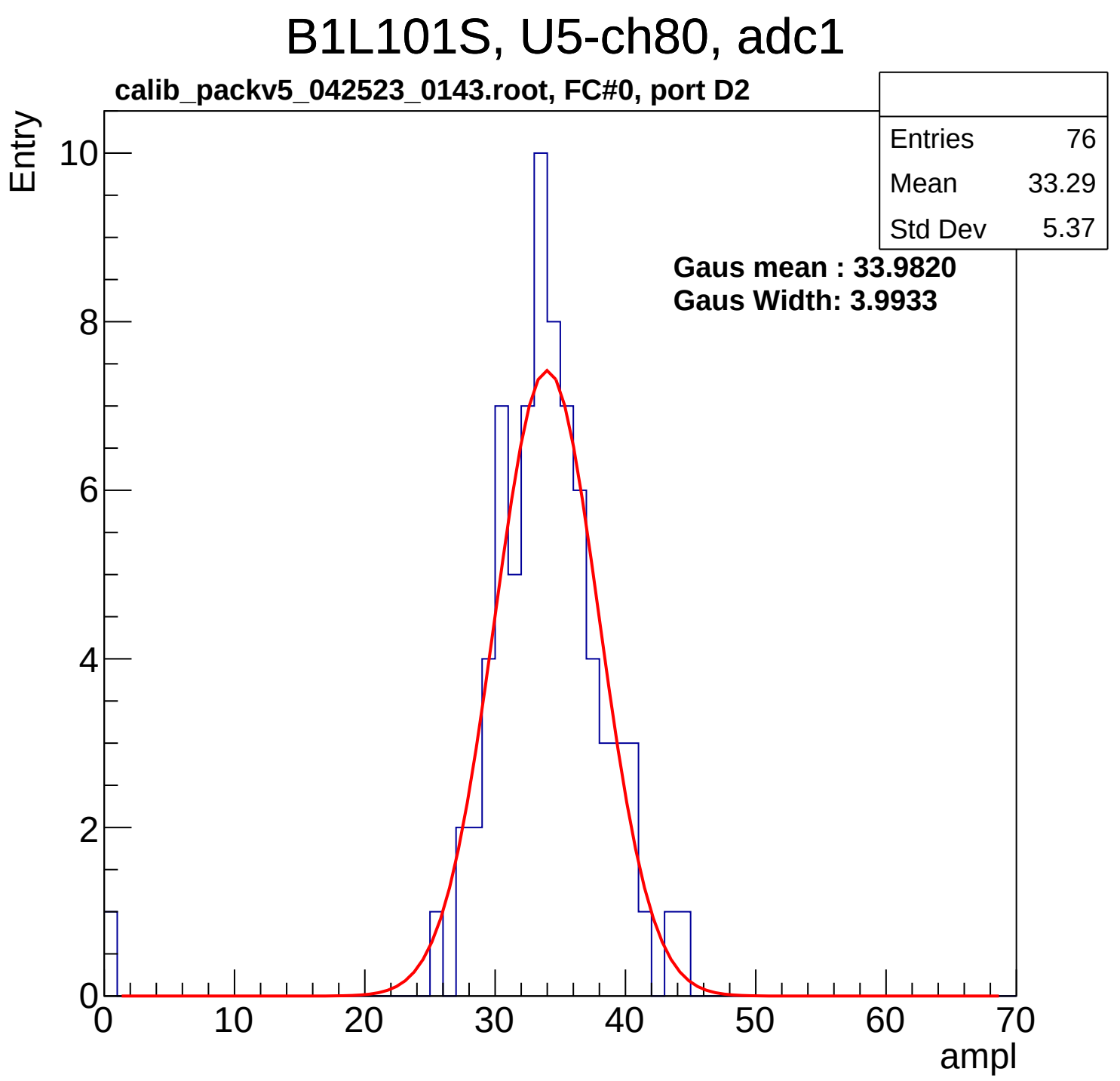
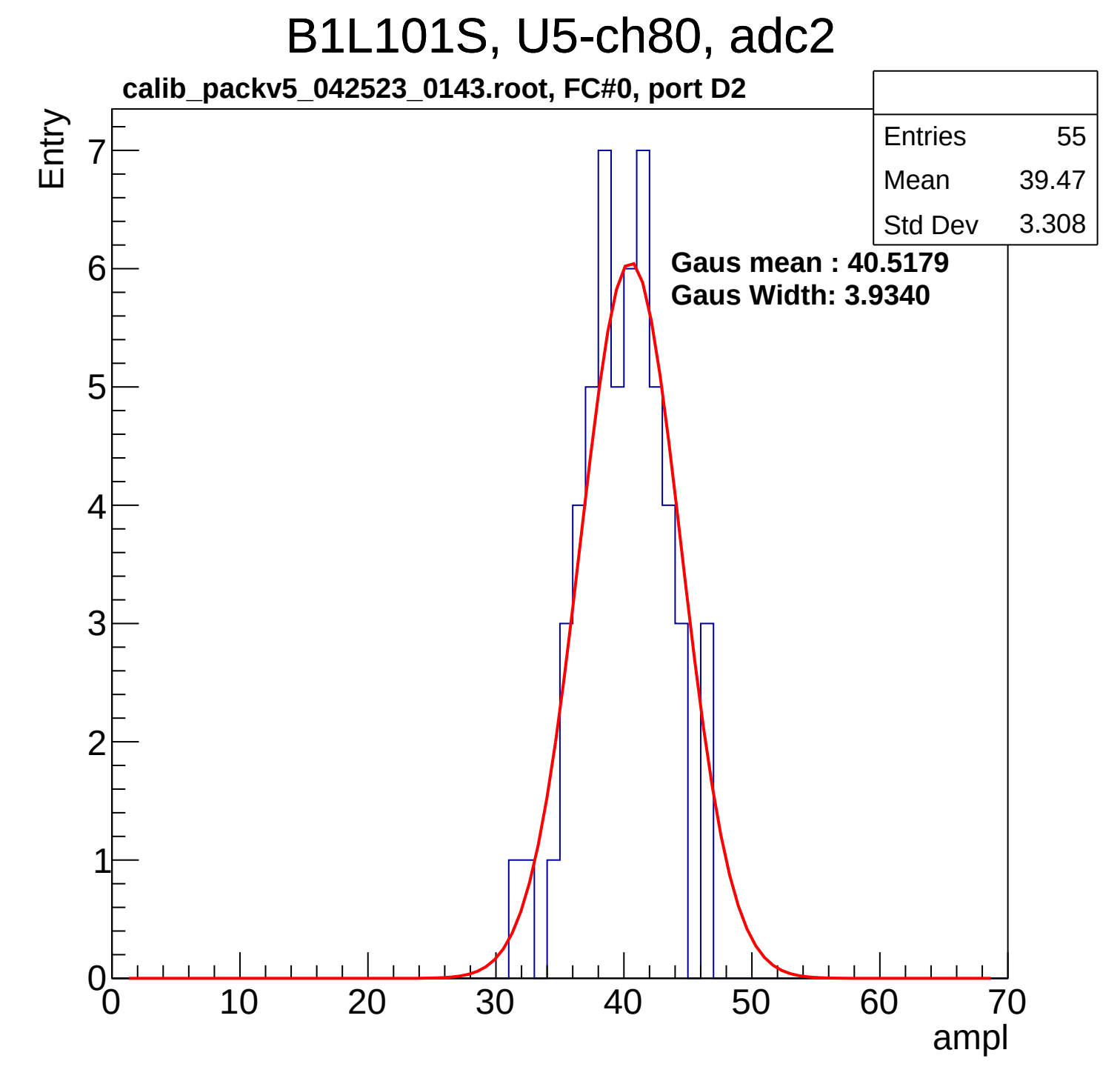
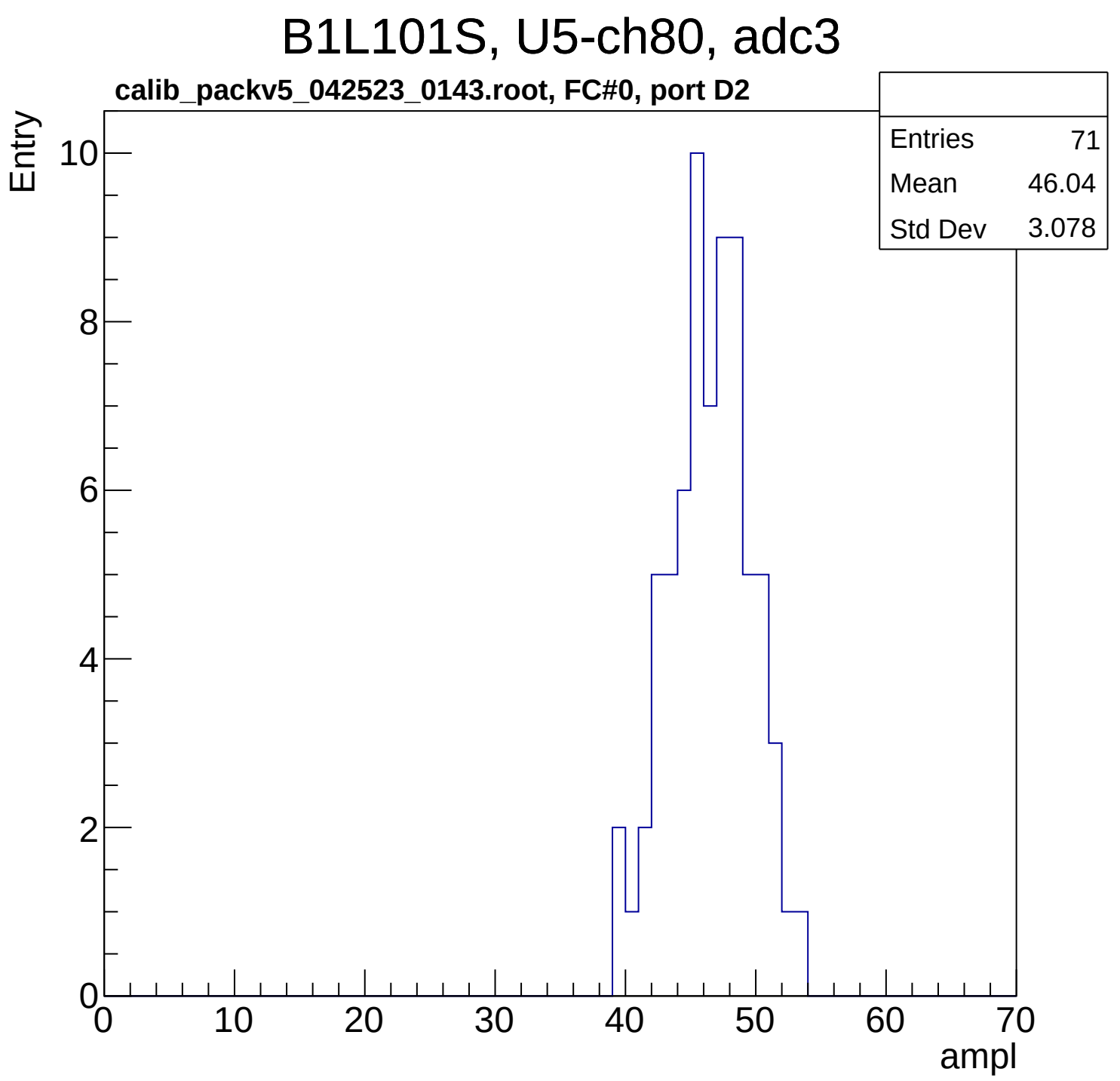
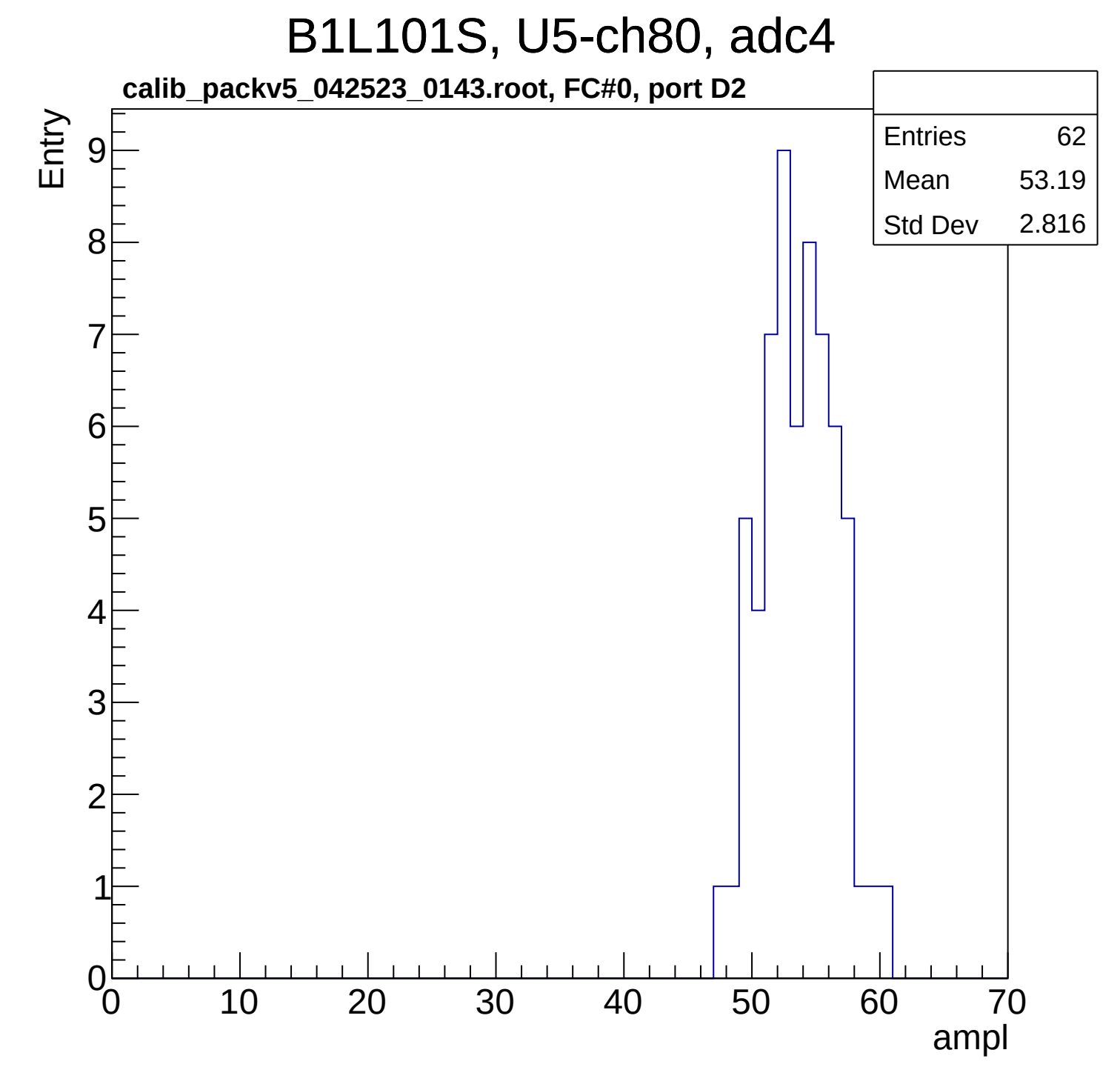
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch80, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 33.29
Std Dev 5.37
Gaus mean : 33.9820
Gaus Width: 3.9933
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch80, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 39.47
Std Dev 3.308
Gaus mean : 40.5179
Gaus Width: 3.9340
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch80, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 46.04
Std Dev 3.078
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch80, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 53.19
Std Dev 2.816
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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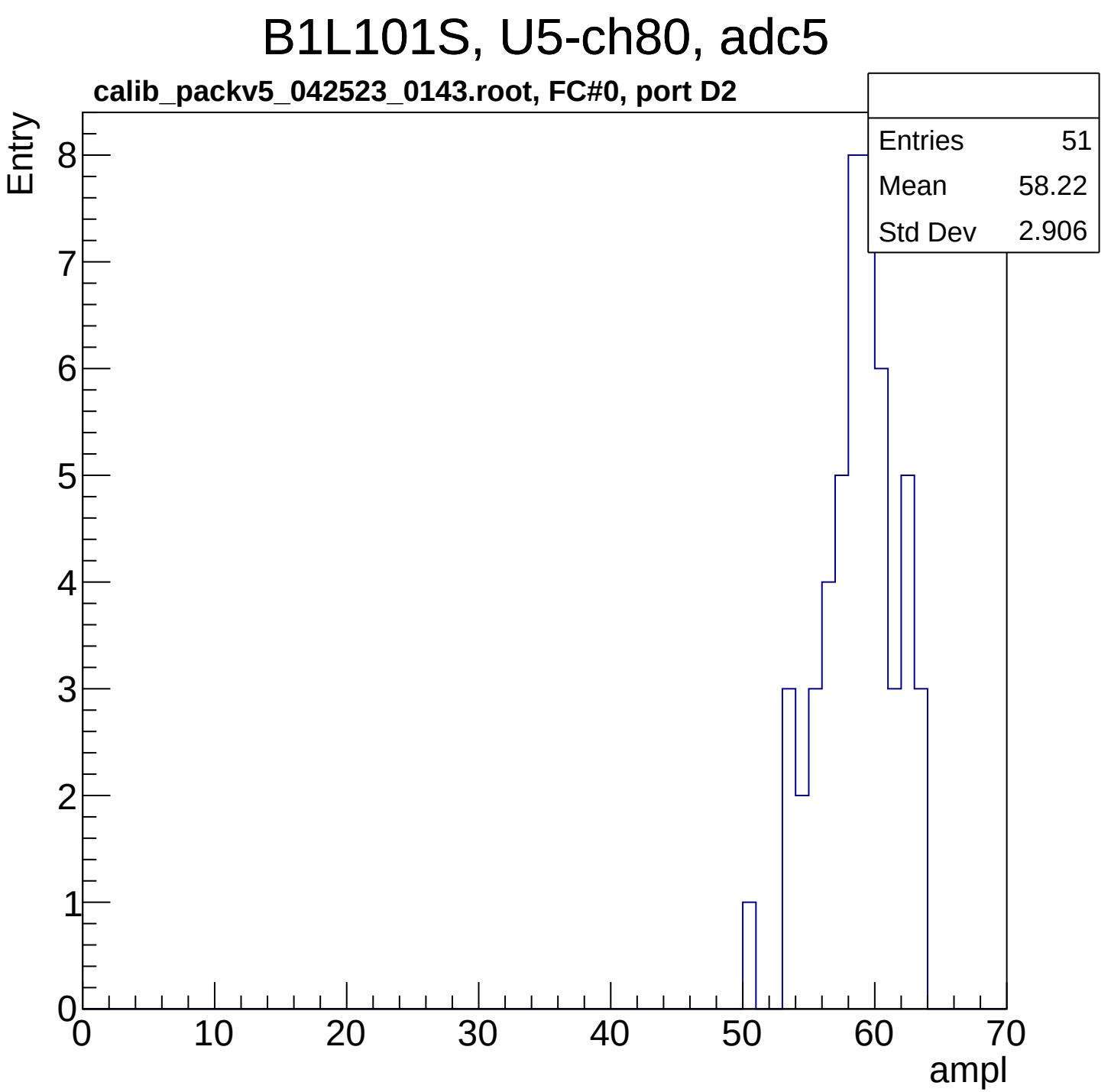
B1L101S, U5-ch80, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 58.22
Std Dev 2.906
Entry
ampl
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1
2
3
4
5
6
7
8
0
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50
60
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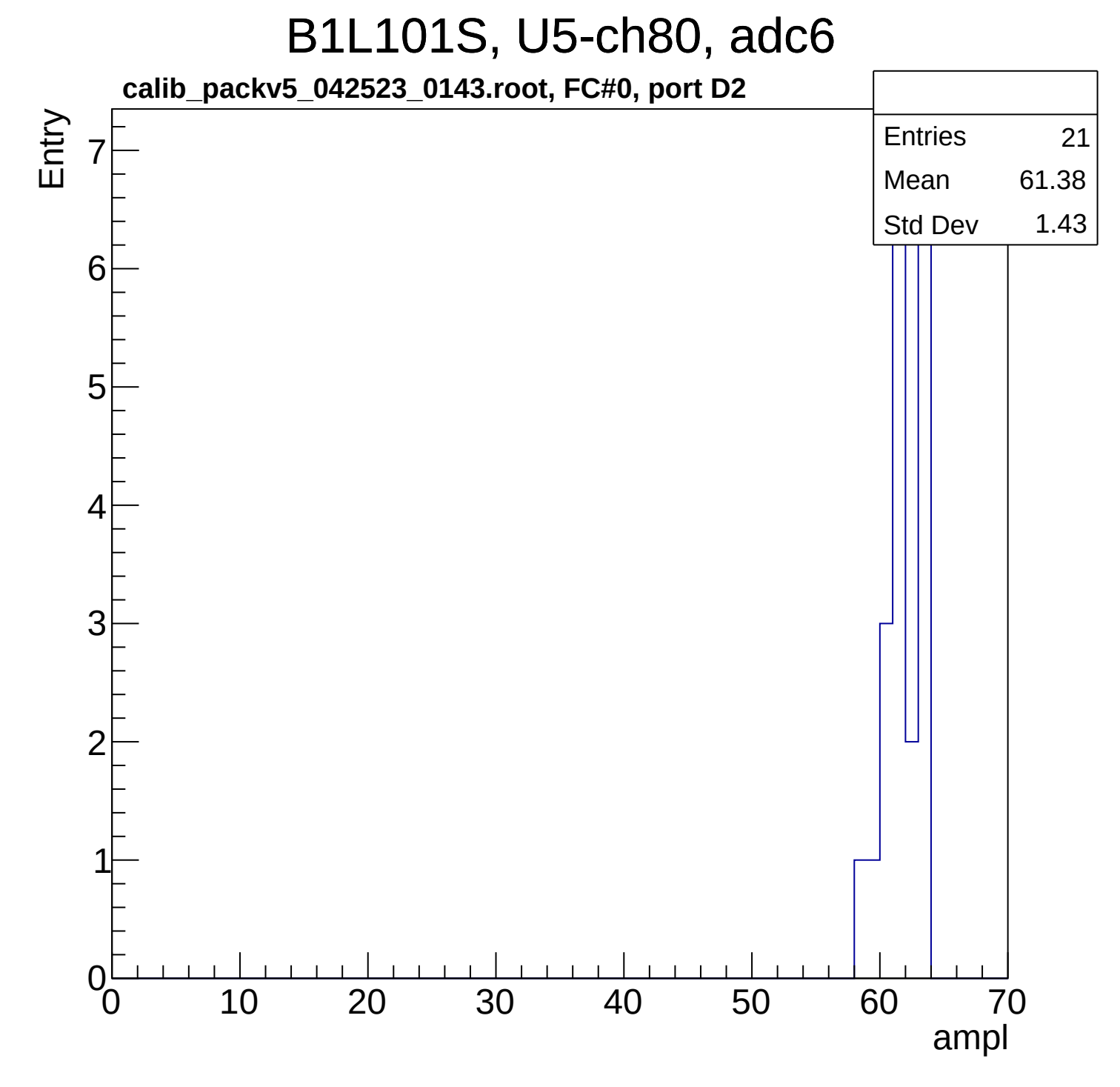
B1L101S, U5-ch80, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 21
Mean 61.38
Std Dev 1.43
Entry
ampl
0
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3
4
5
6
7
0
10
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40
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60
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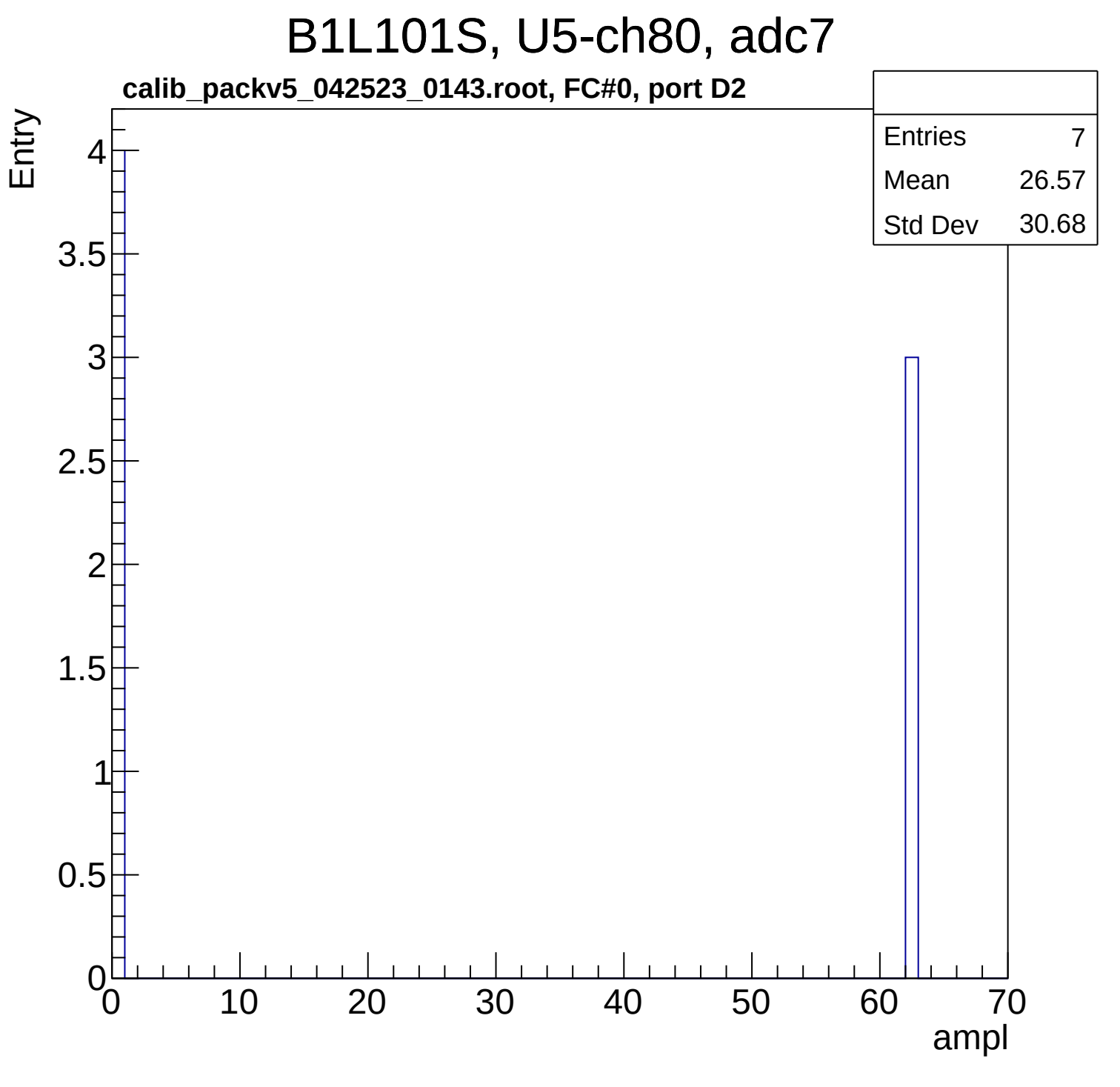
B1L101S, U5-ch80, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 26.57
Std Dev 30.68
Entry
ampl
0
0.5
1
1.5
2
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3
3.5
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60
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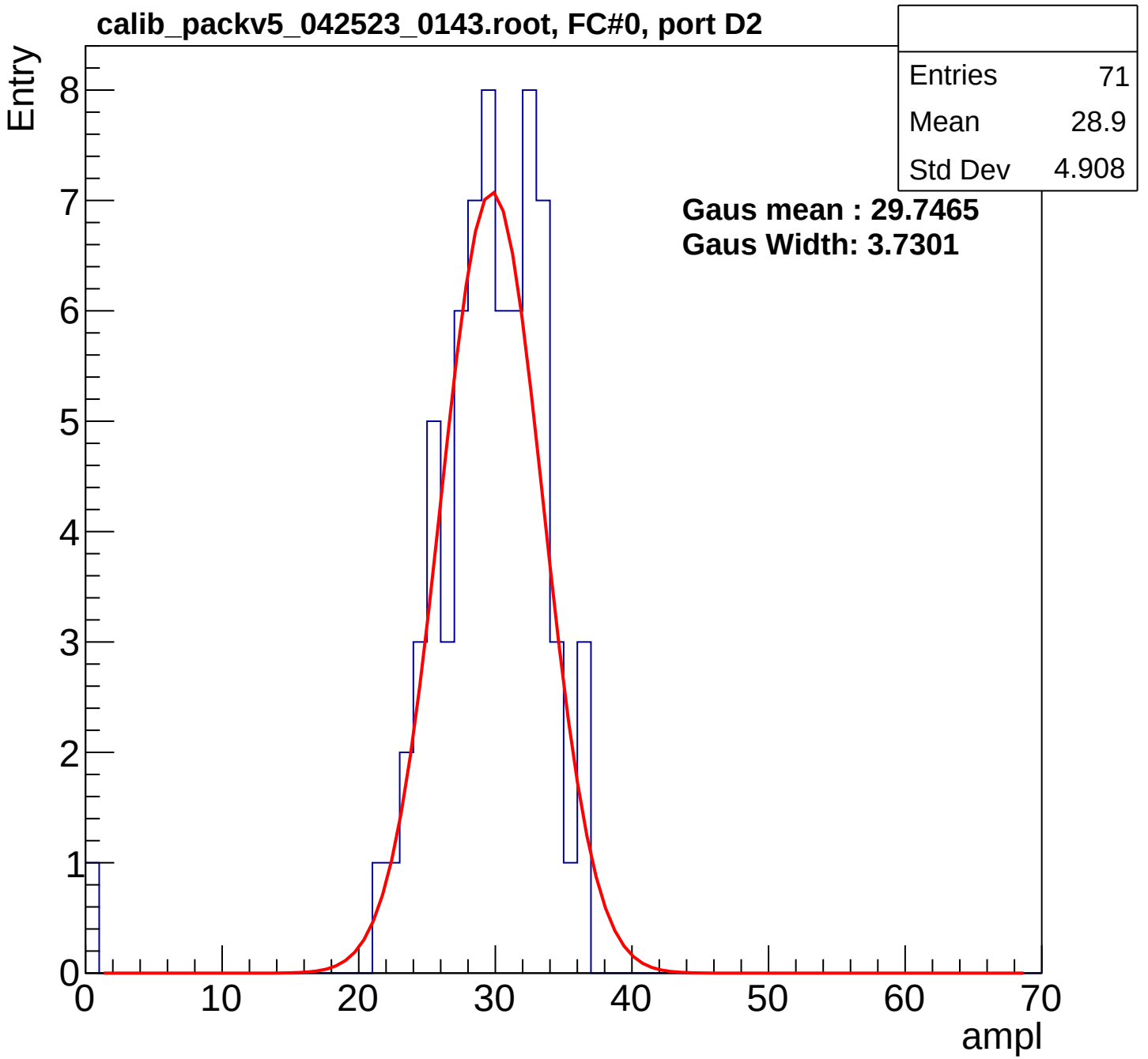
B1L101S, U5-ch81, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 28.9
Std Dev 4.908
Gaus mean : 29.7465
Gaus Width: 3.7301
Entry
ampl
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2
3
4
5
6
7
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0
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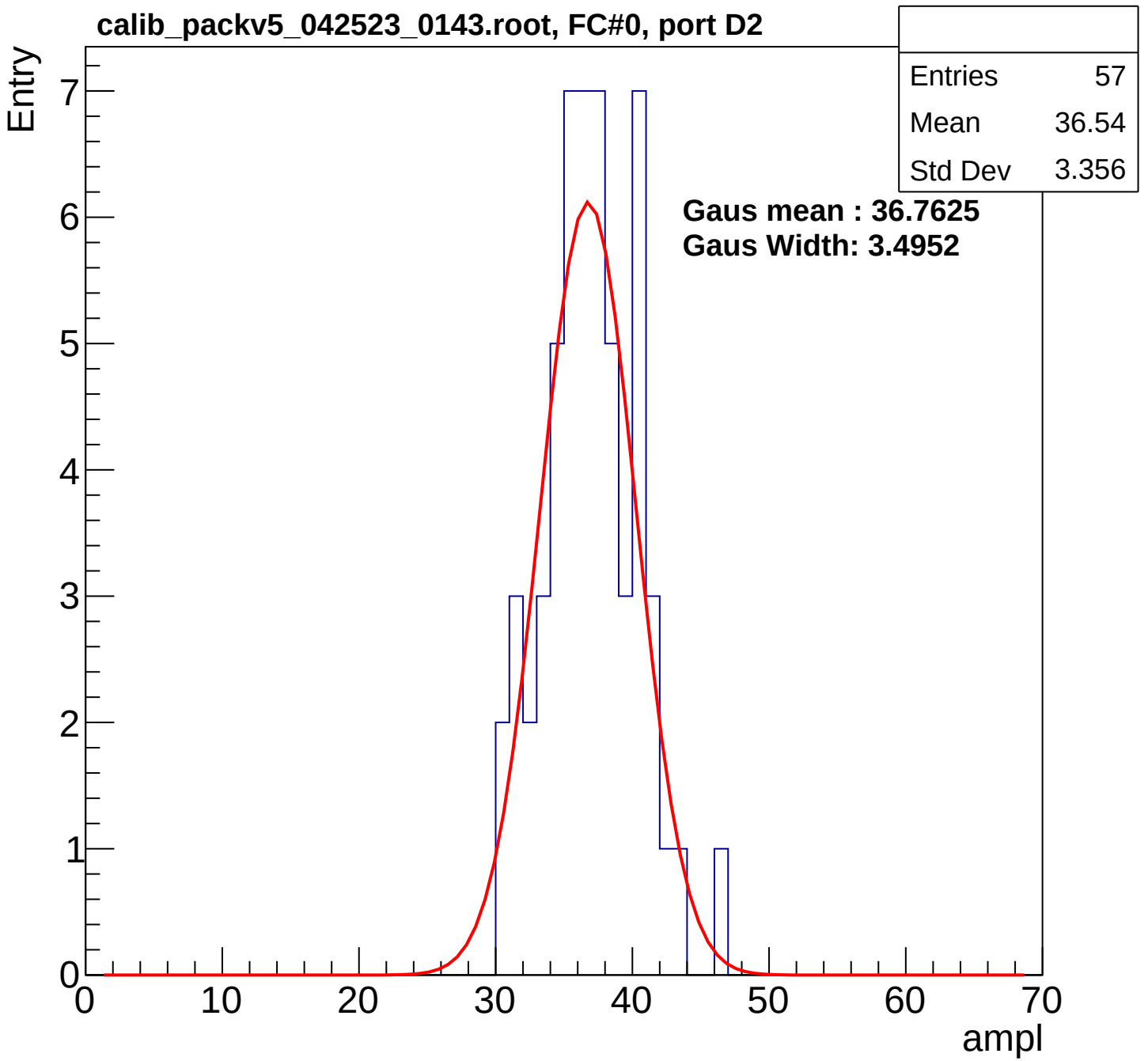
B1L101S, U5-ch81, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 36.54
Std Dev 3.356
Gaus mean : 36.7625
Gaus Width: 3.4952
Entry
ampl
0
1
2
3
4
5
6
7
0
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40
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60
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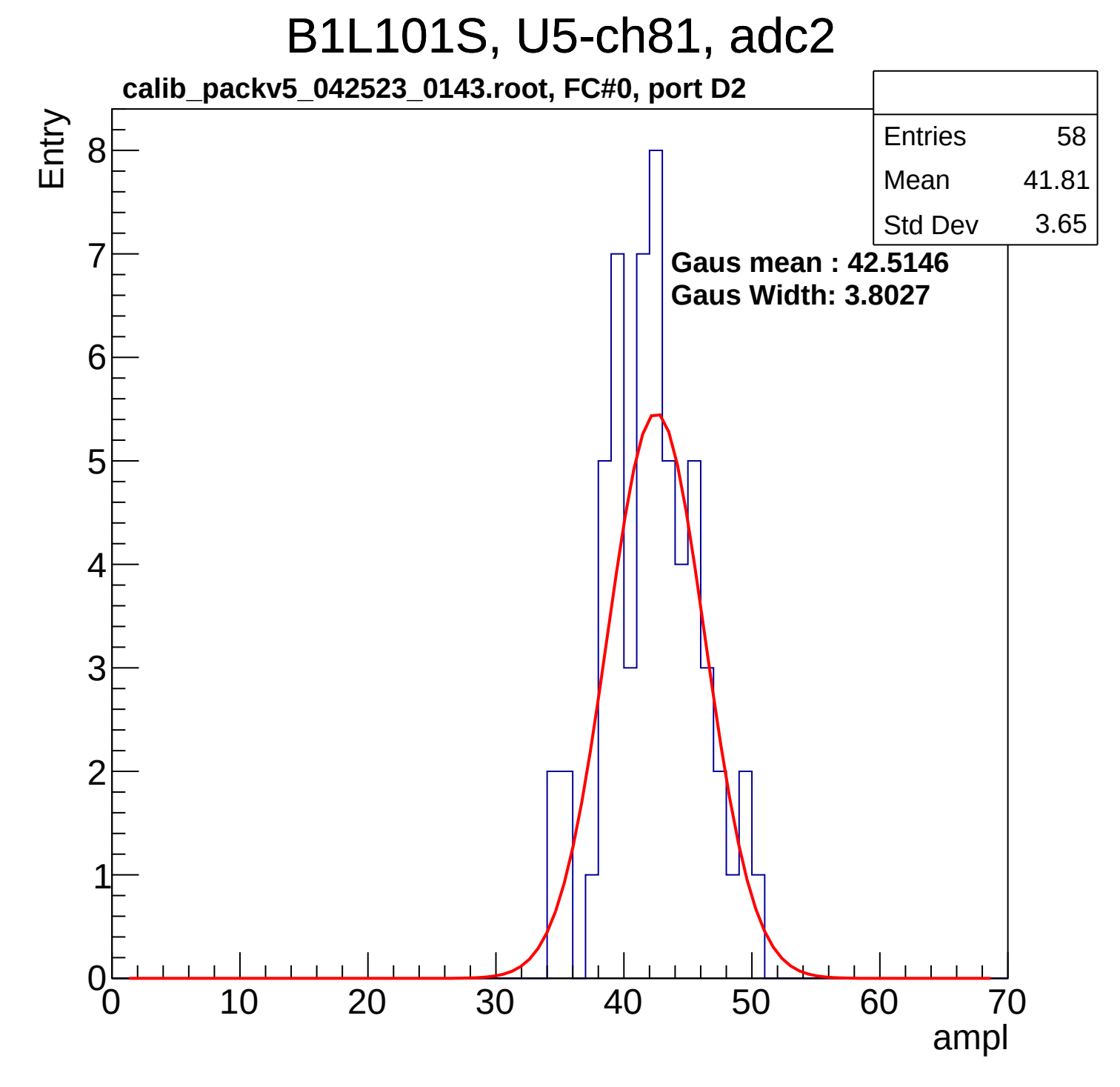
B1L101S, U5-ch81, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 41.81
Std Dev 3.65
Gaus mean : 42.5146
Gaus Width: 3.8027
Entry
ampl
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1
2
3
4
5
6
7
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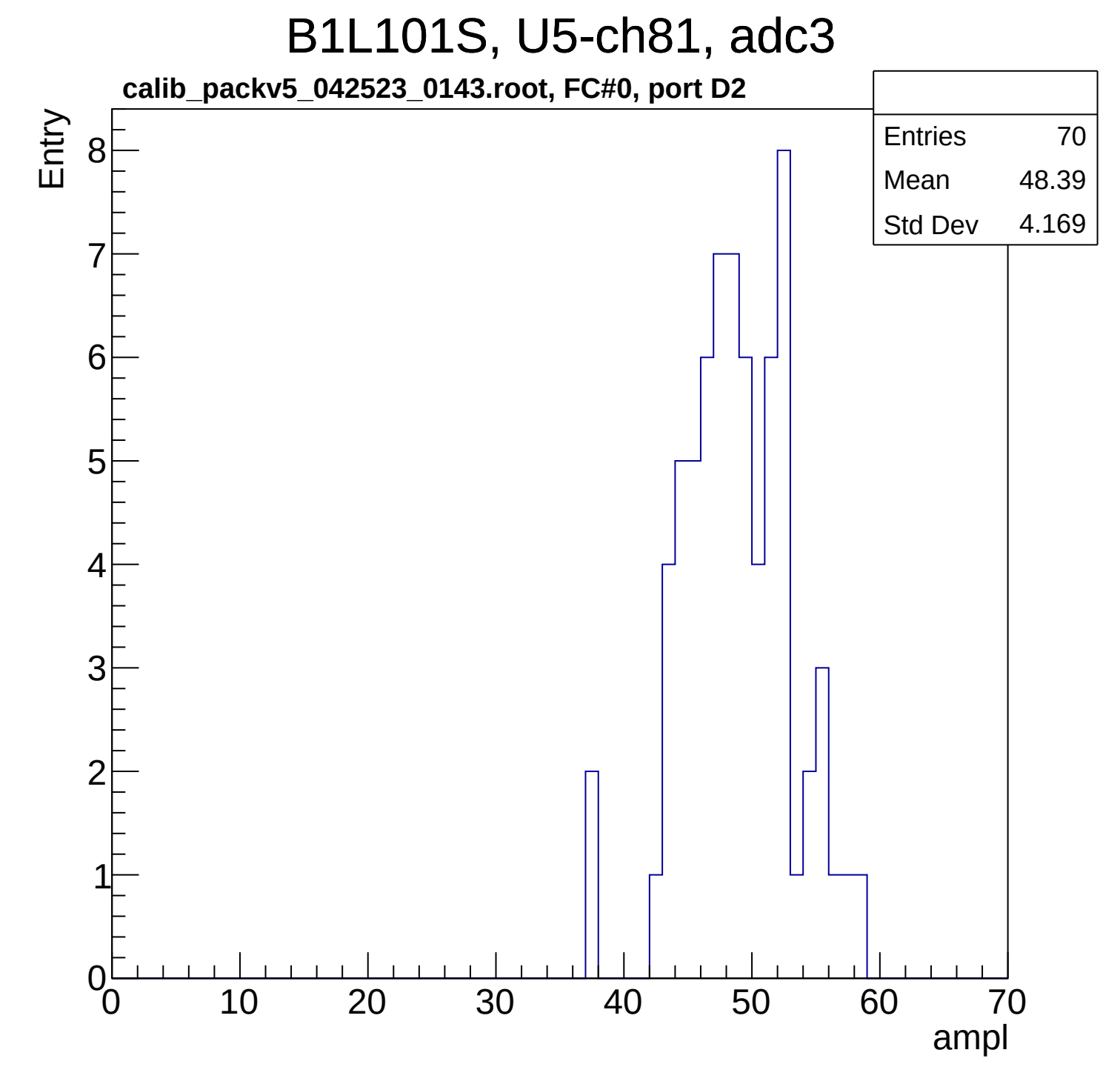
B1L101S, U5-ch81, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 48.39
Std Dev 4.169
Entry
ampl
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2
3
4
5
6
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0
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60
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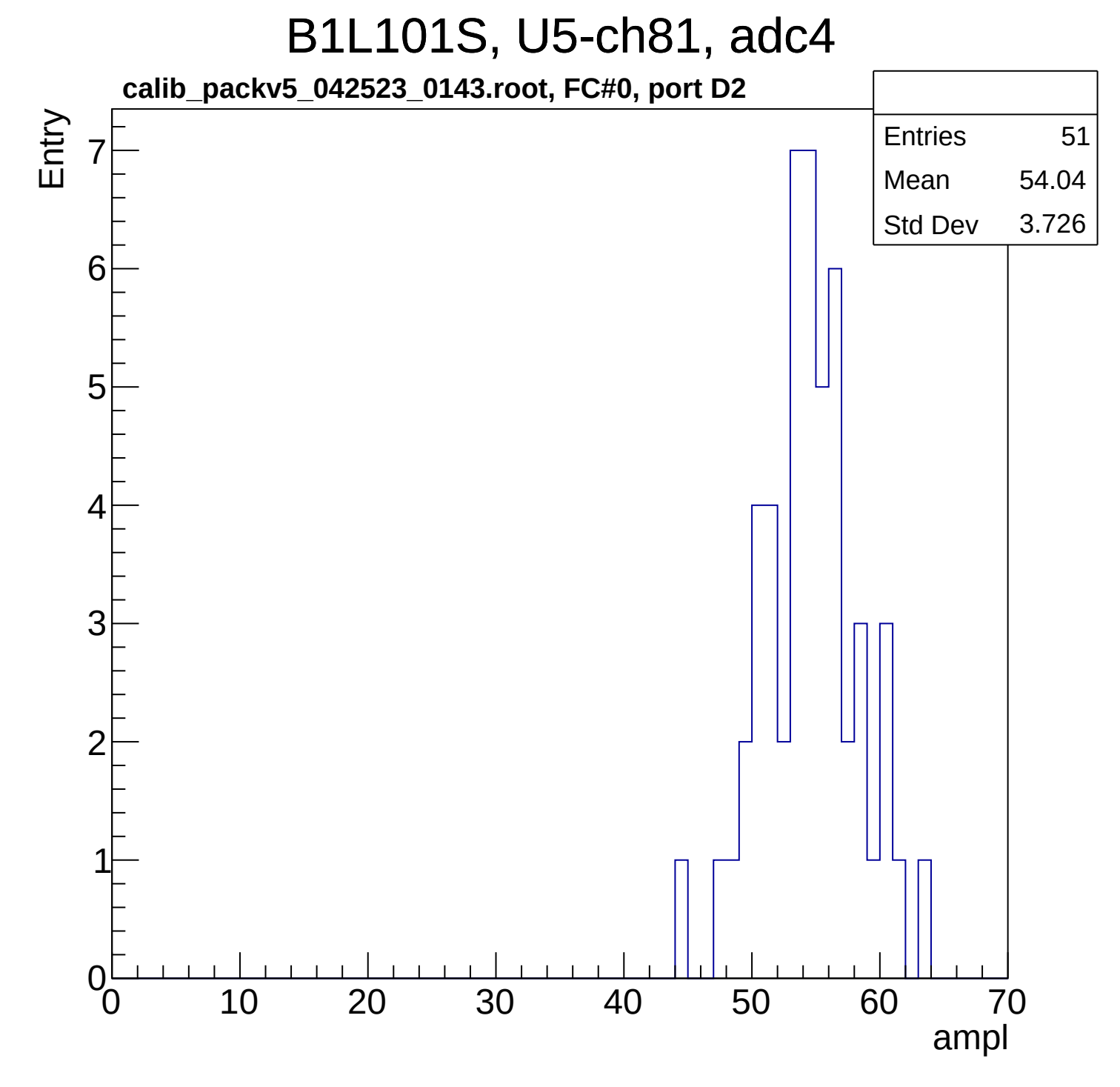
B1L101S, U5-ch81, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 54.04
Std Dev 3.726
Entry
ampl
0
1
2
3
4
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6
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0
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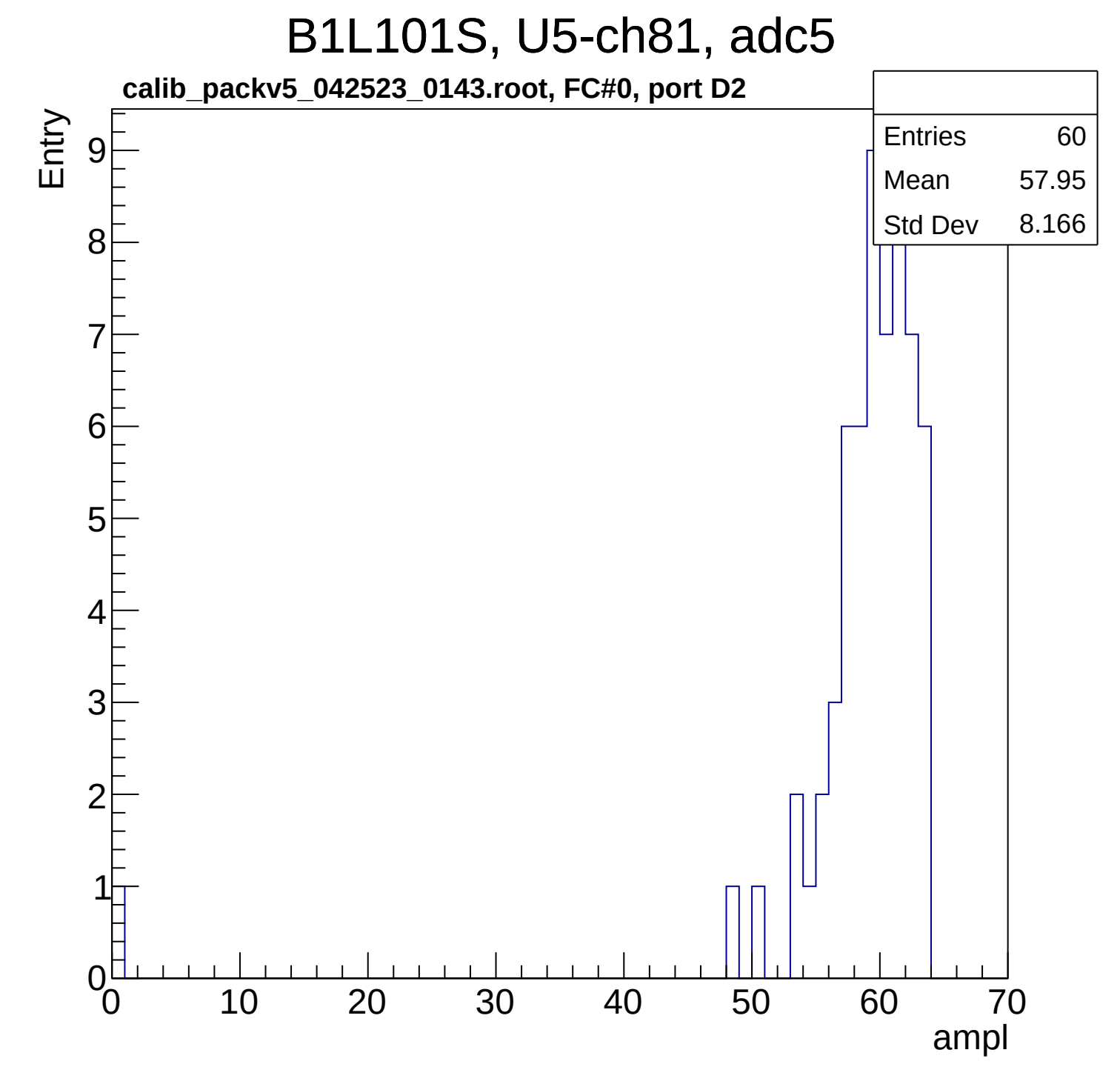
B1L101S, U5-ch81, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 57.95
Std Dev 8.166
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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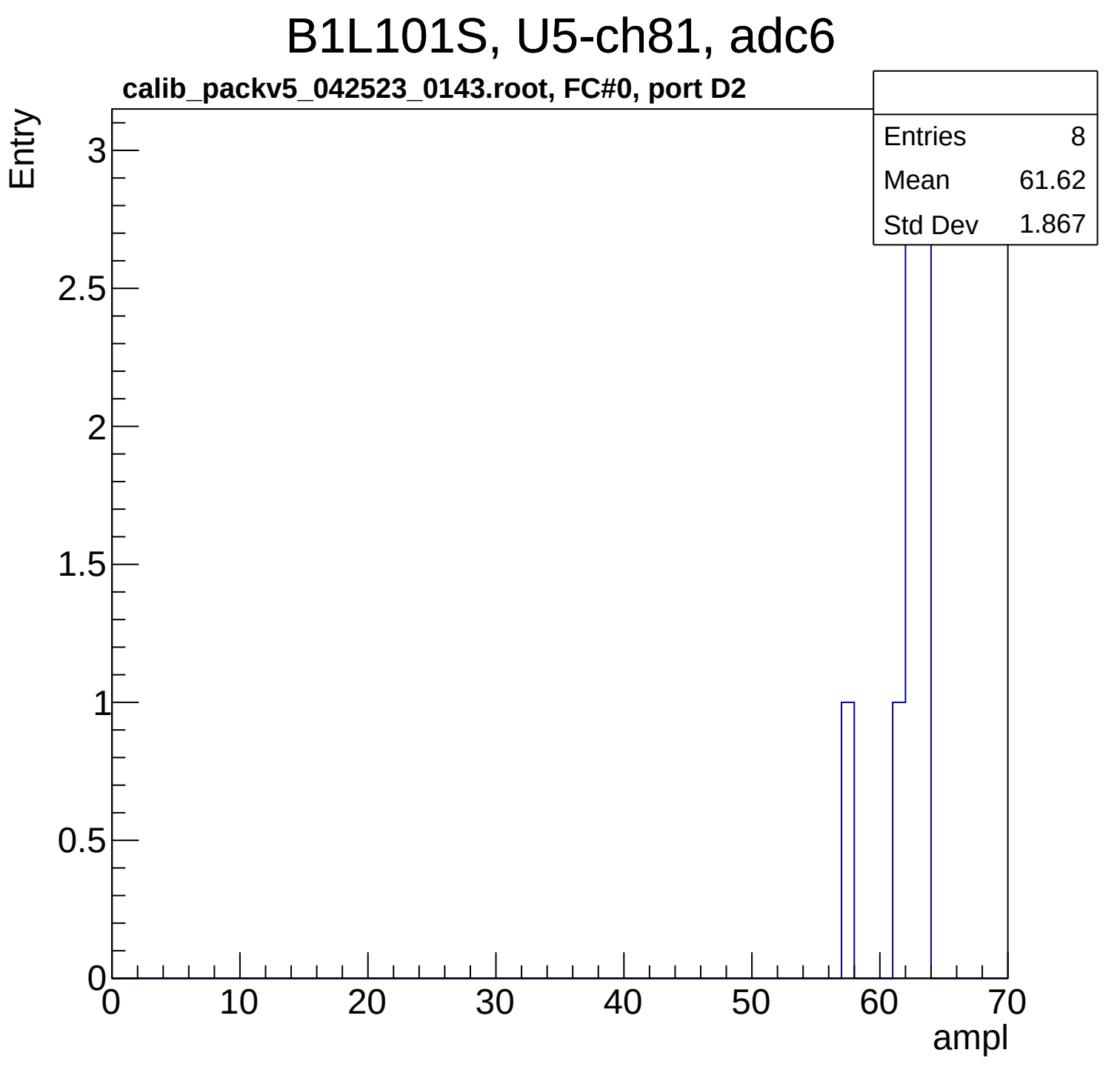
B1L101S, U5-ch81, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 61.62
Std Dev 1.867
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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40
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60
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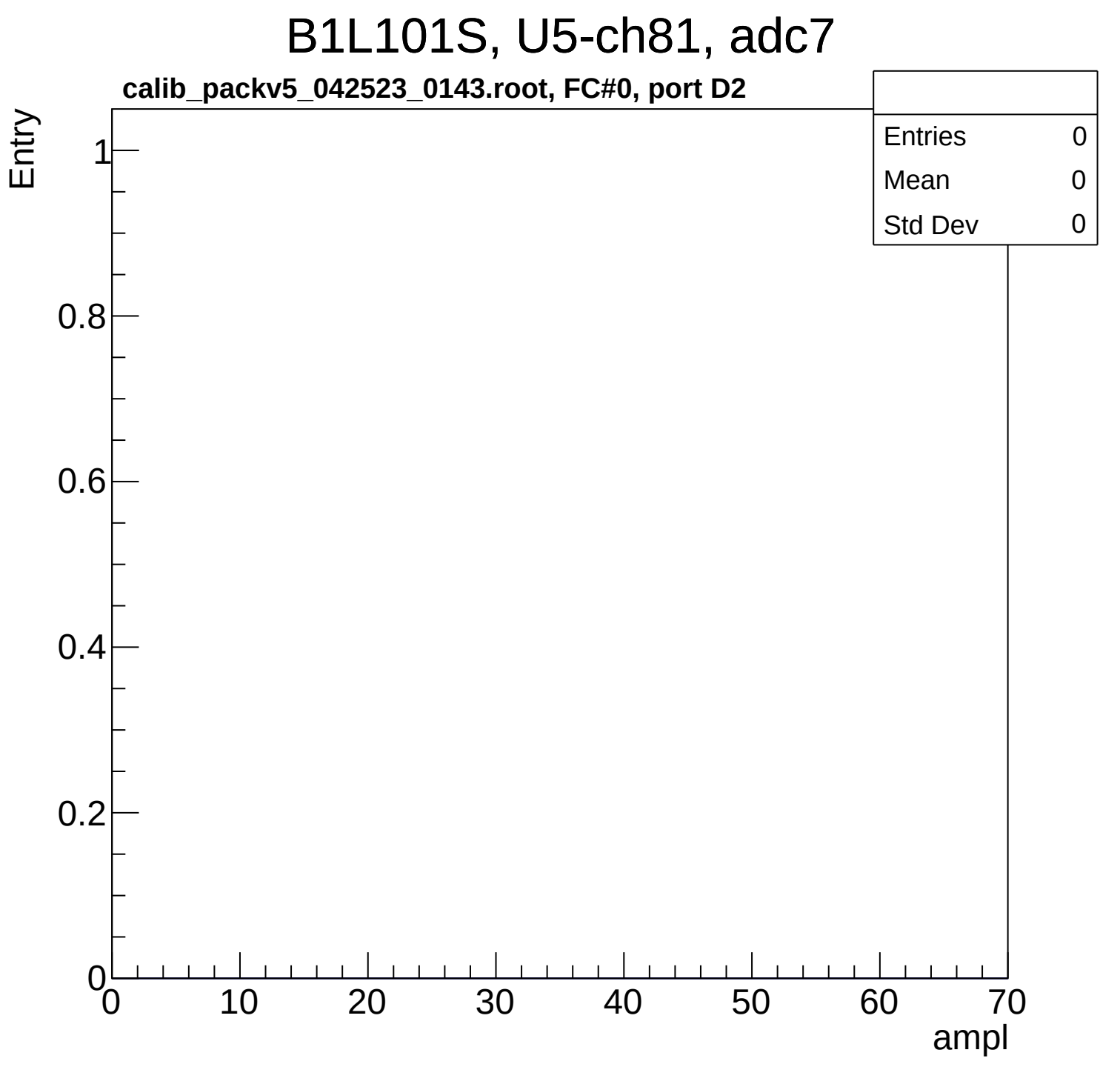
B1L101S, U5-ch81, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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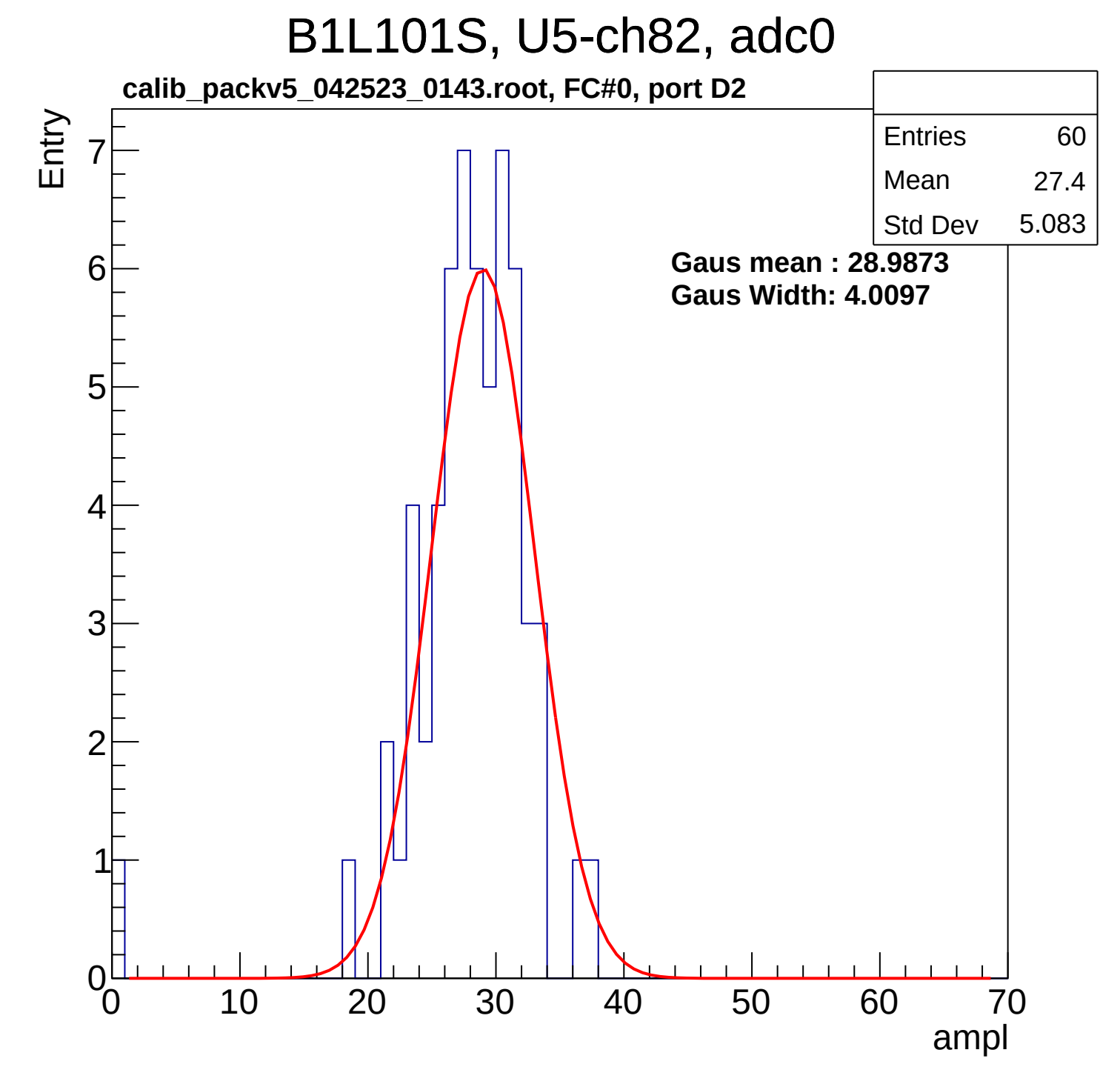
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch82, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 27.4
Std Dev 5.083
Gaus mean : 28.9873
Gaus Width: 4.0097
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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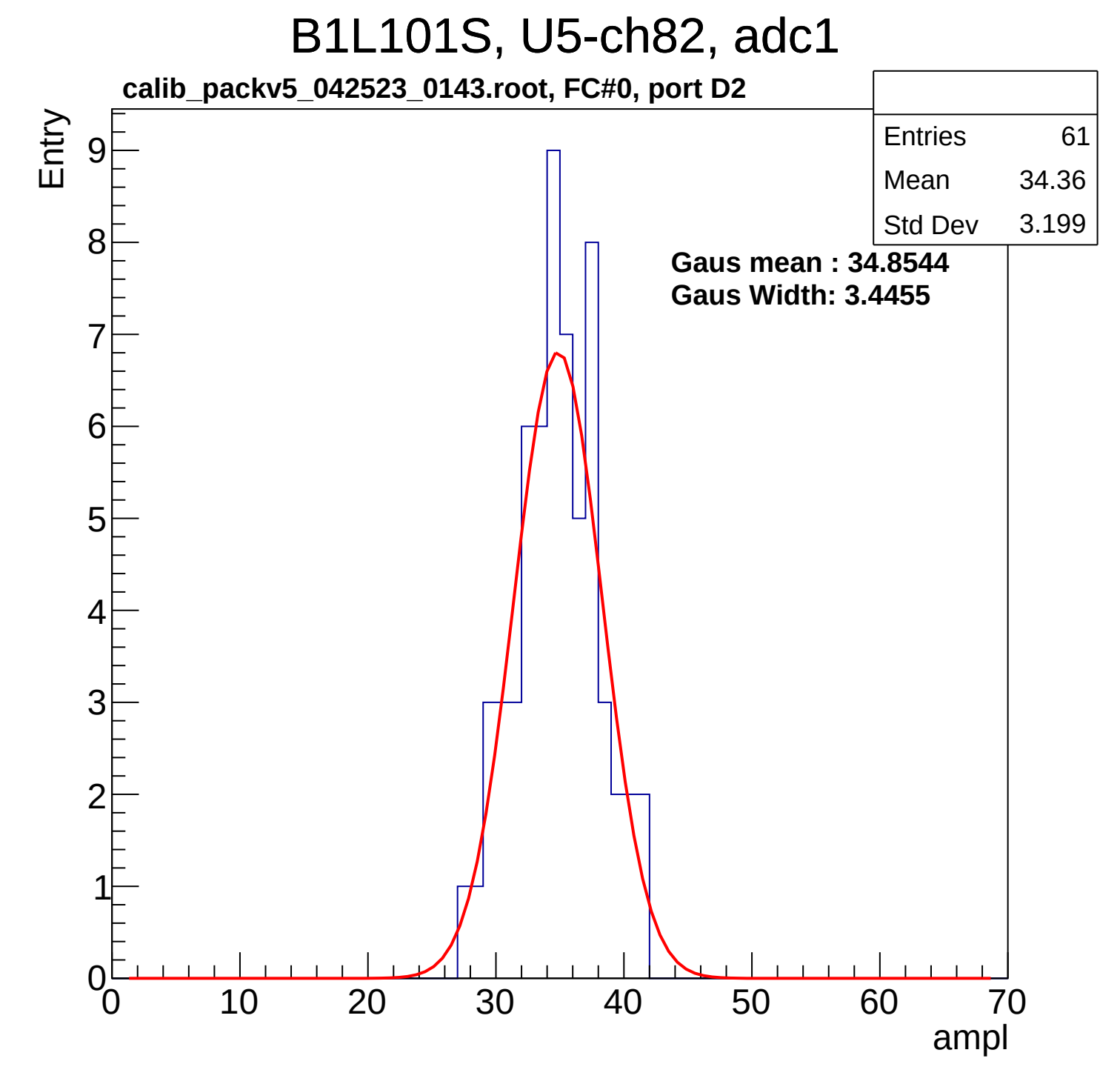
B1L101S, U5-ch82, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 34.36
Std Dev 3.199
Gaus mean : 34.8544
Gaus Width: 3.4455
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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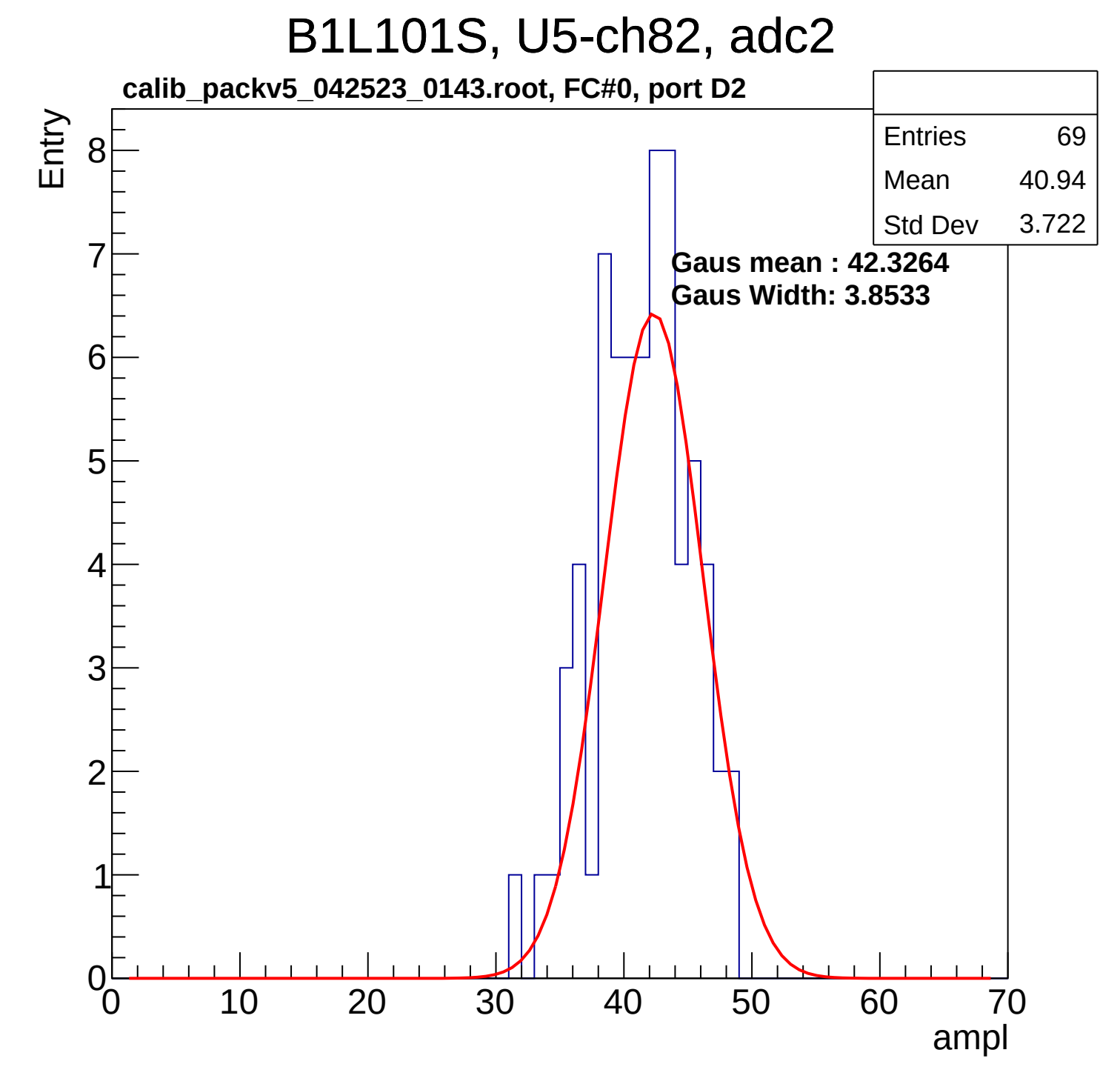
B1L101S, U5-ch82, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 40.94
Std Dev 3.722
Gaus mean : 42.3264
Gaus Width: 3.8533
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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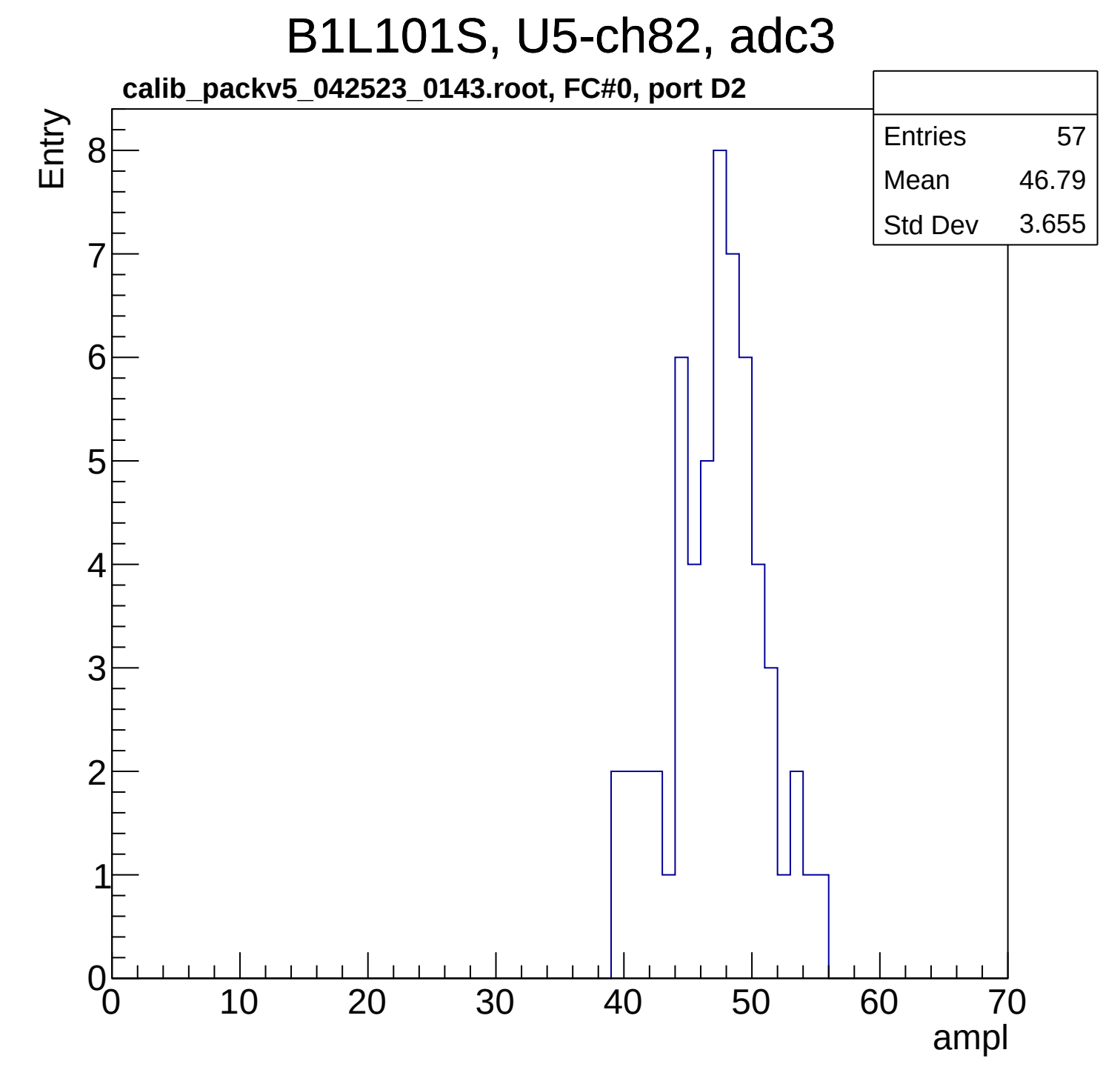
B1L101S, U5-ch82, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 46.79
Std Dev 3.655
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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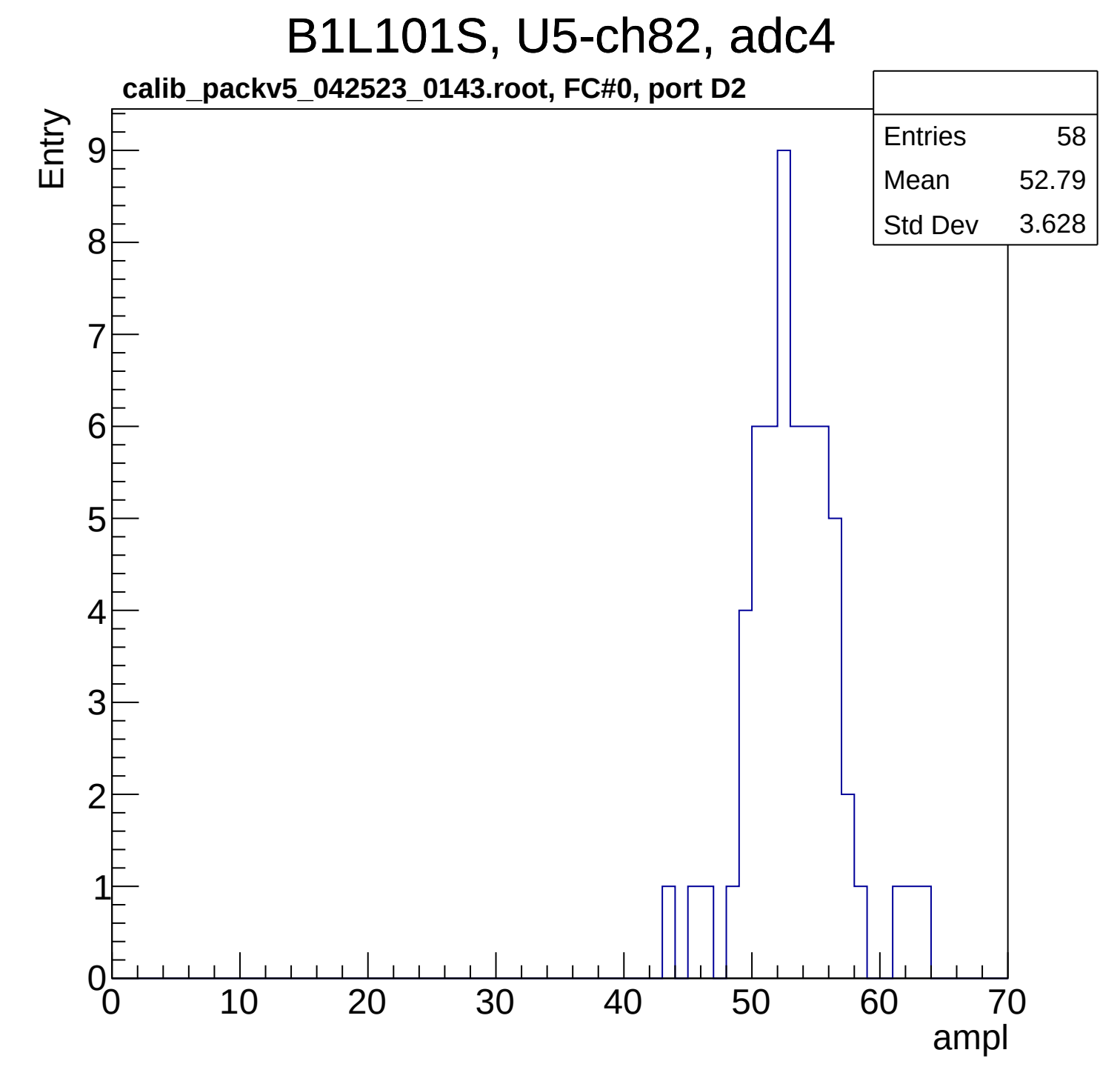
B1L101S, U5-ch82, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 52.79
Std Dev 3.628
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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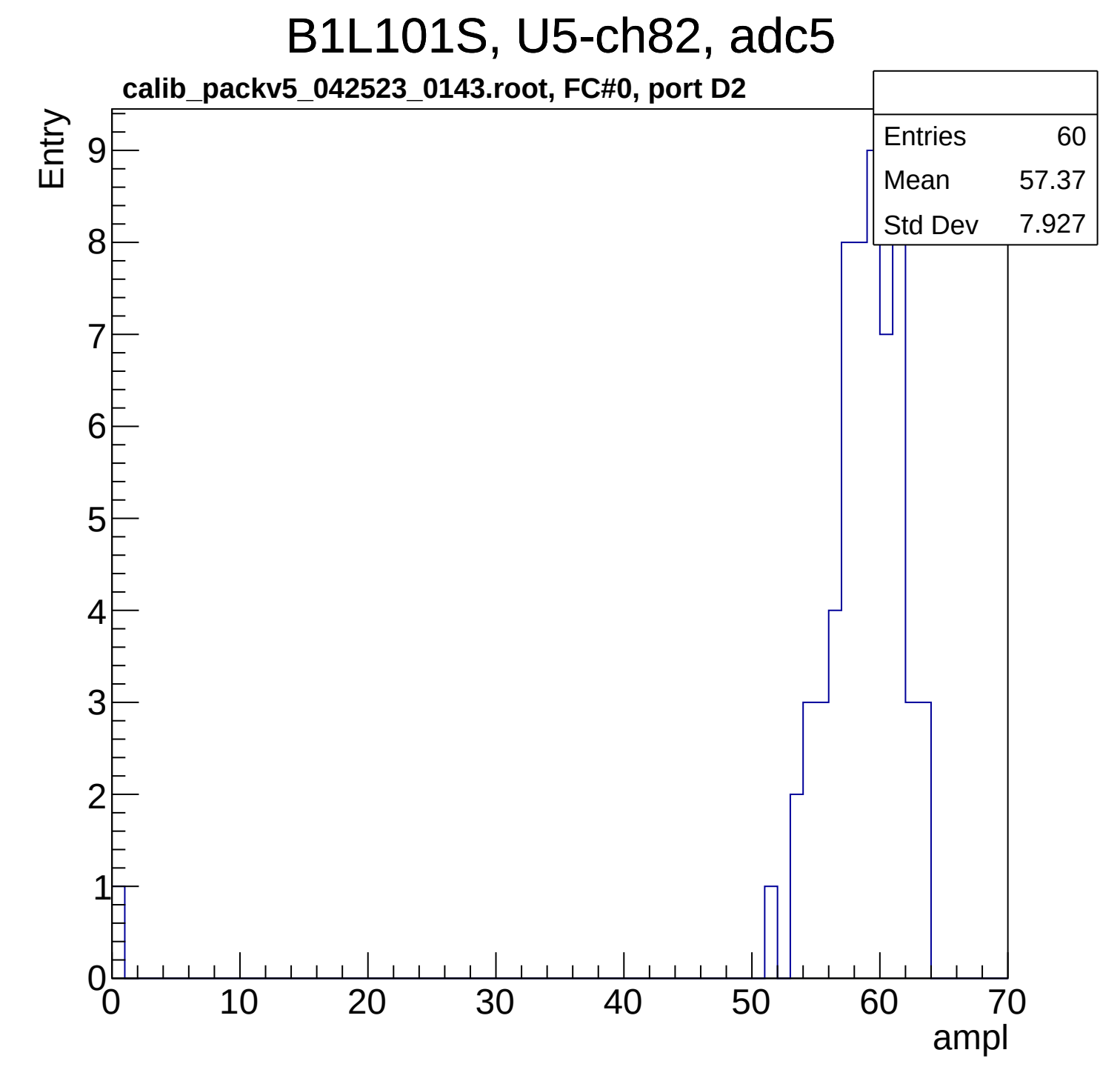
B1L101S, U5-ch82, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 57.37
Std Dev 7.927
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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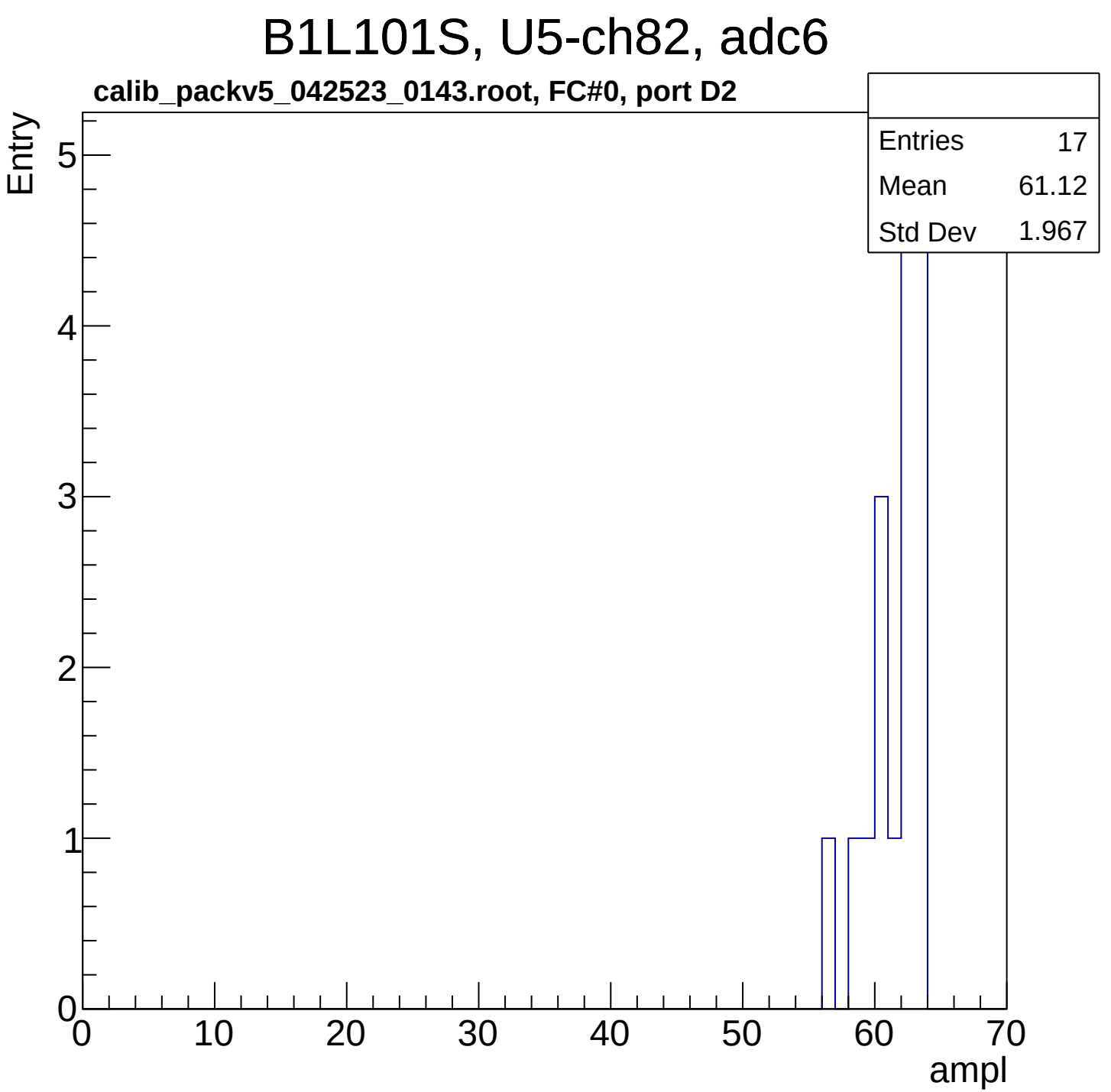
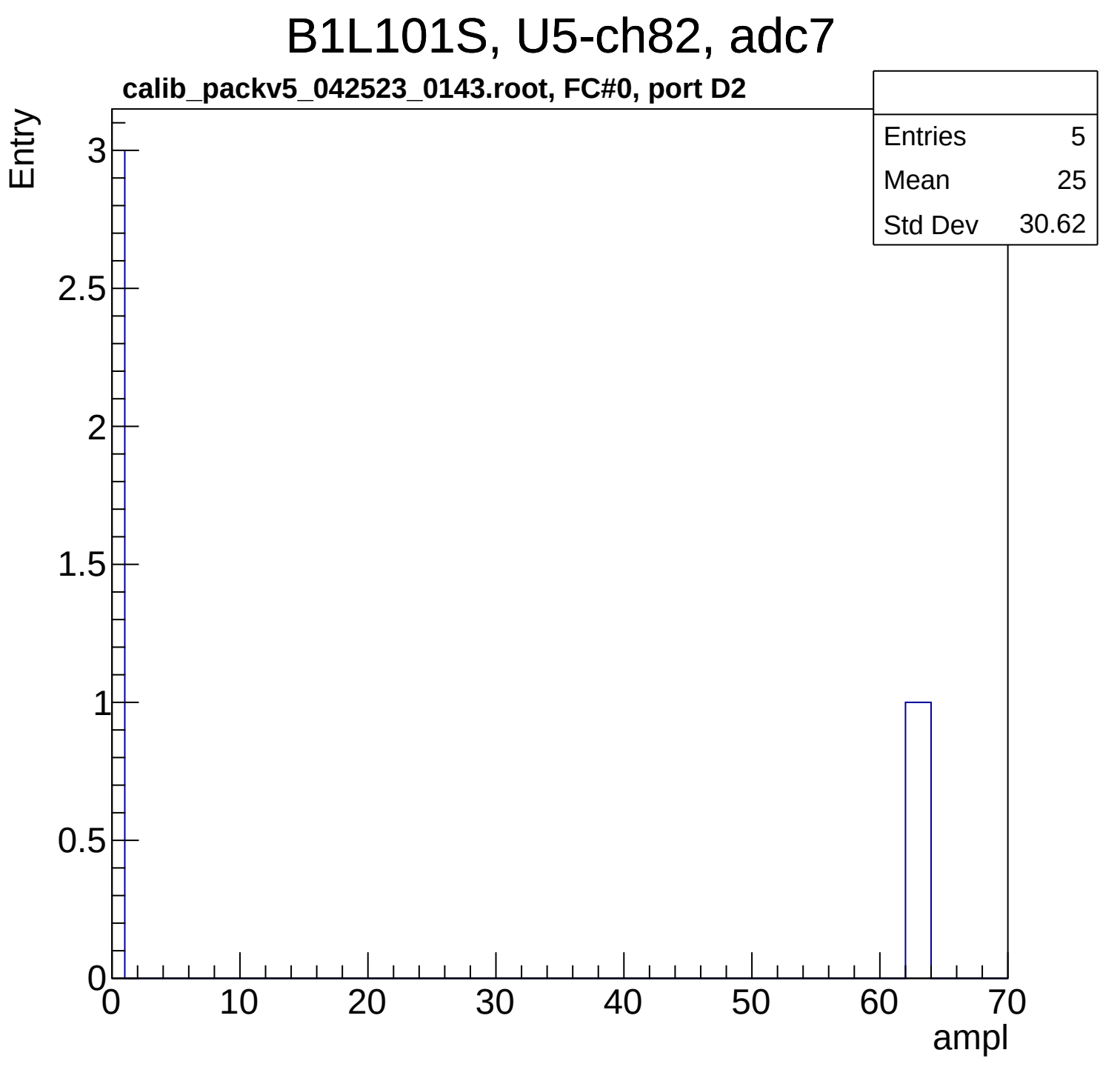

B1L101S, U5-ch82, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 17
Mean 61.12
Std Dev 1.967
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch82, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 25
Std Dev 30.62
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
50
60
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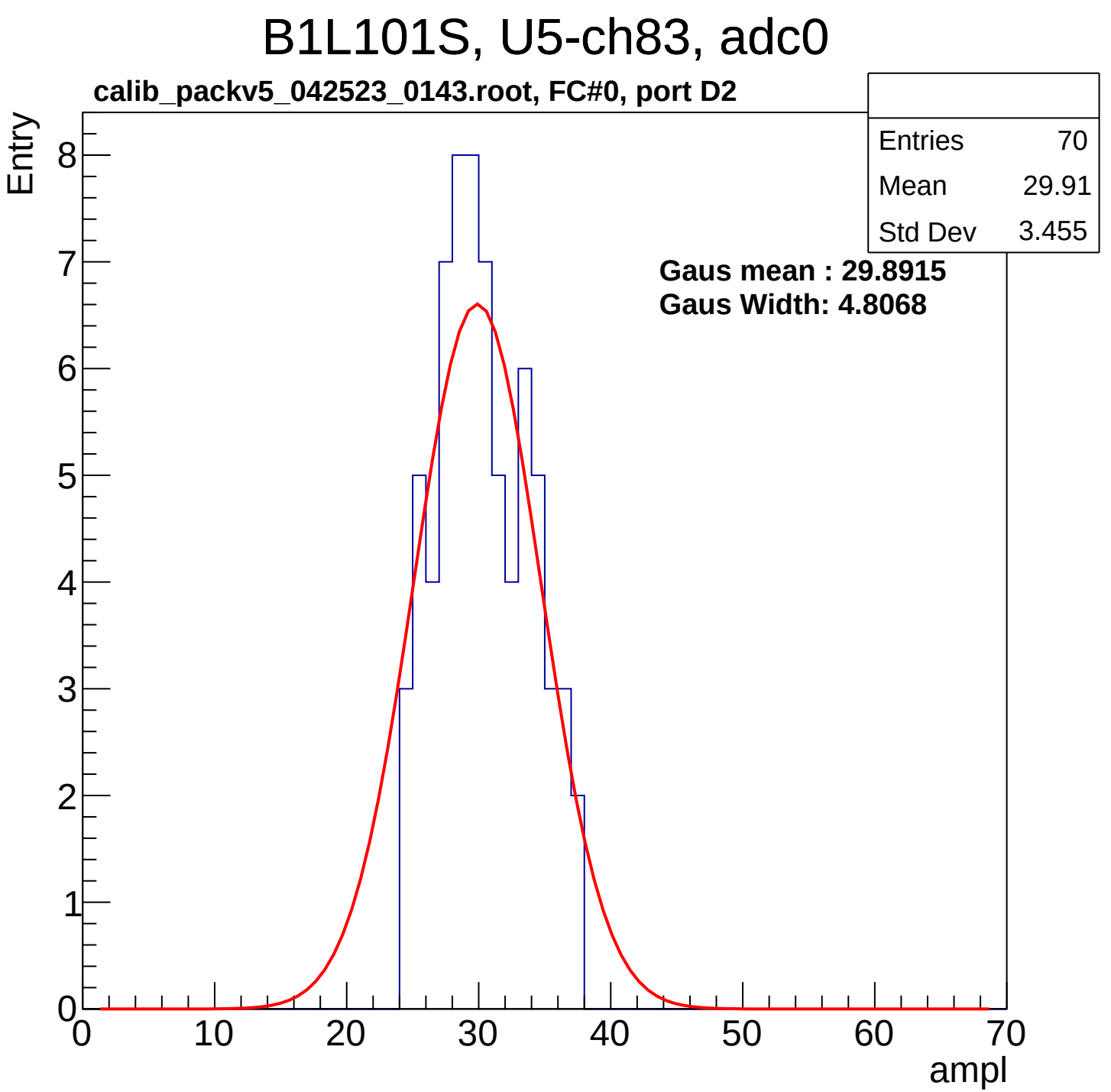
B1L101S, U5-ch83, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 29.91
Std Dev 3.455
Gaus mean : 29.8915
Gaus Width: 4.8068
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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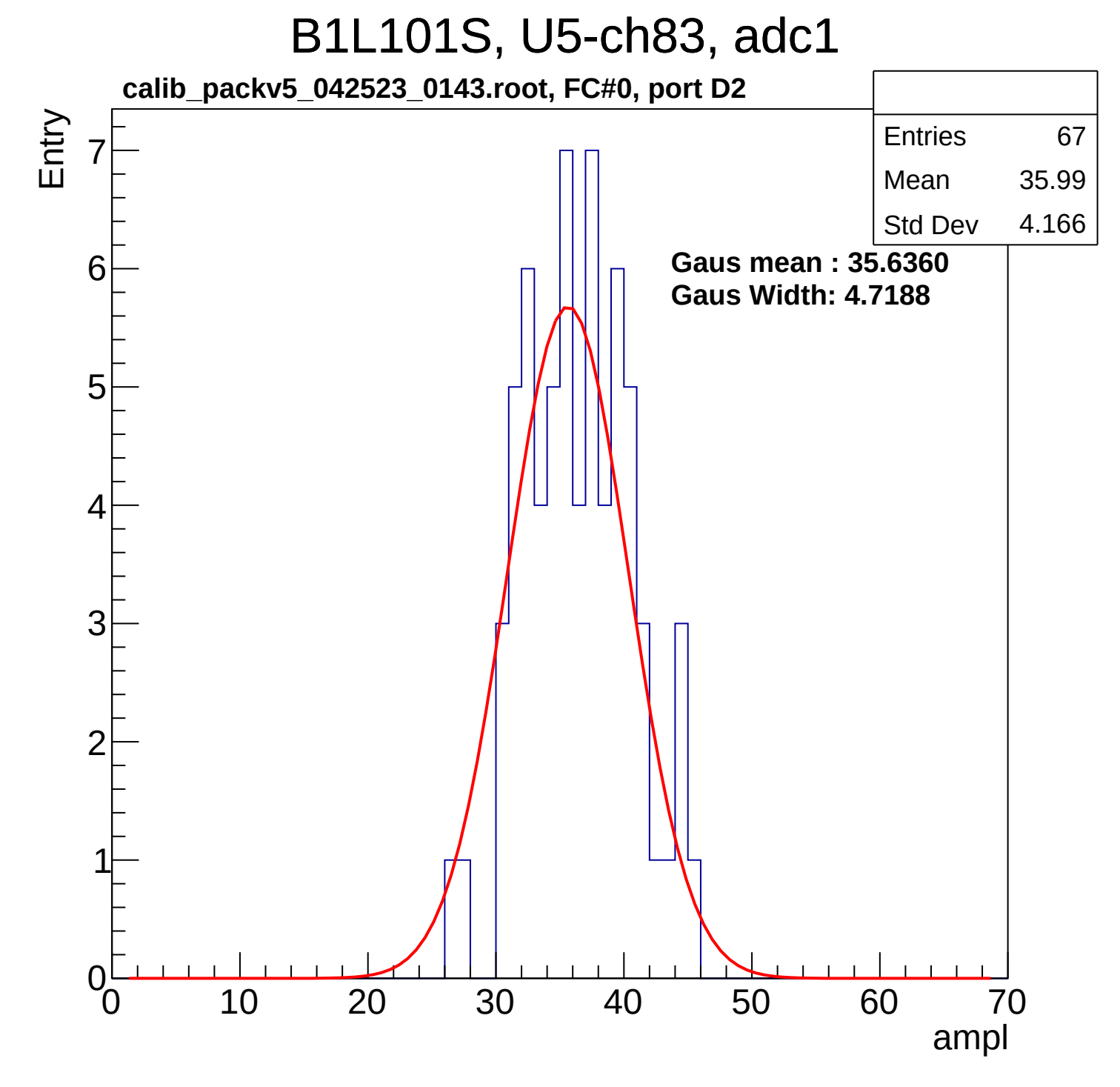
40
50
60
70


B1L101S, U5-ch83, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 35.99
Std Dev 4.166
Gaus mean : 35.6360
Gaus Width: 4.7188
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
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60
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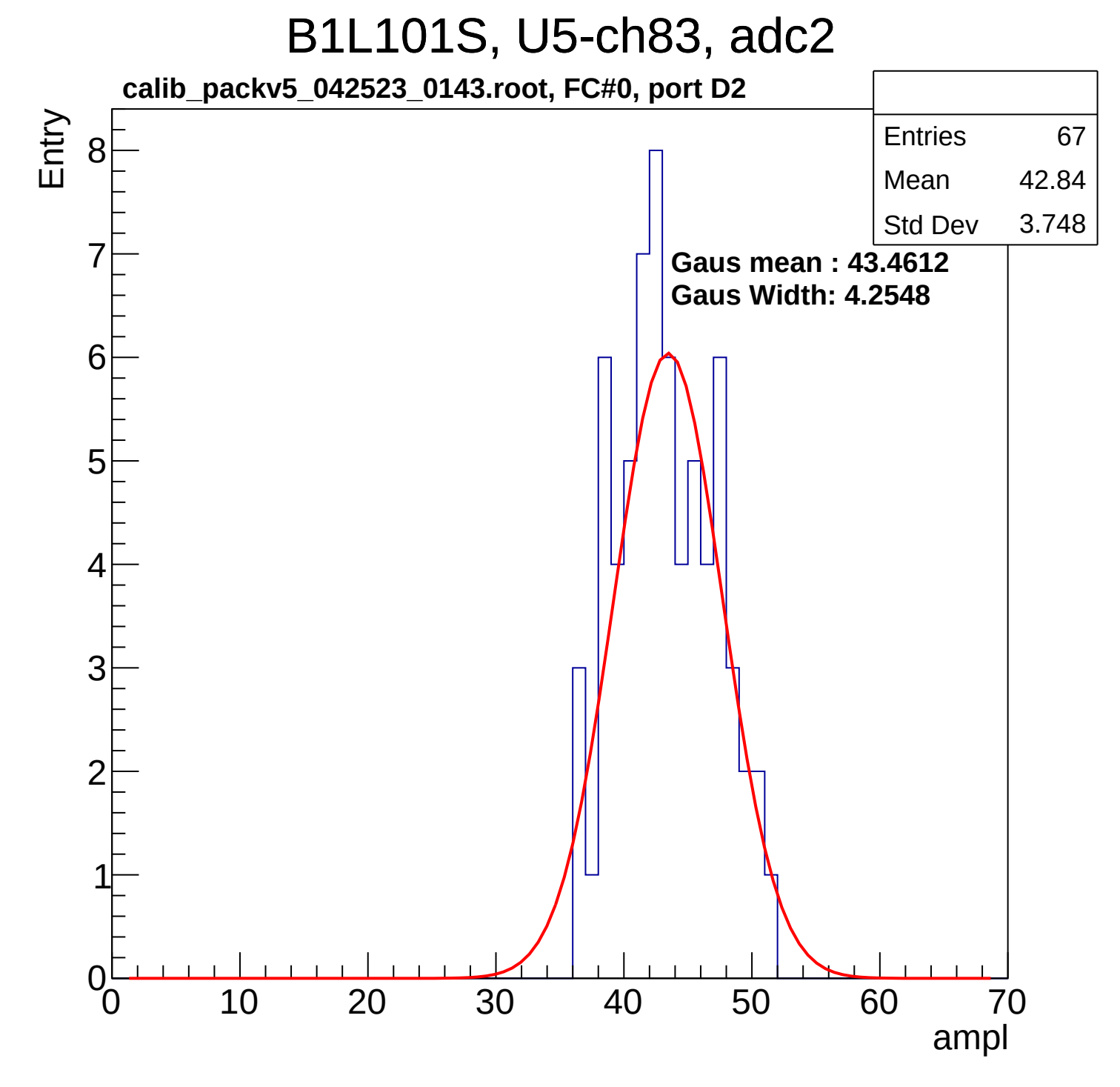
B1L101S, U5-ch83, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 42.84
Std Dev 3.748
Gaus mean : 43.4612
Gaus Width: 4.2548
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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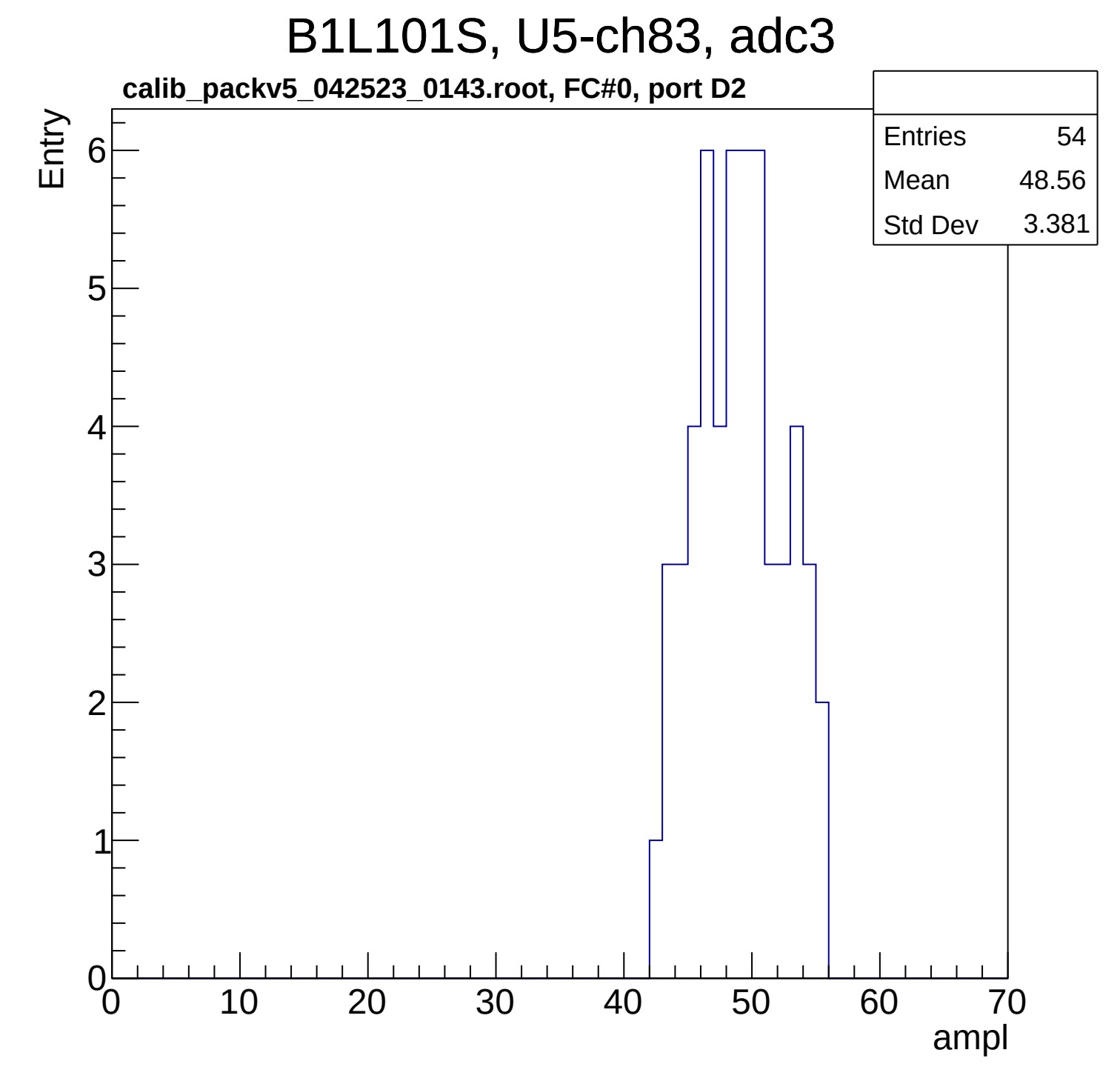
B1L101S, U5-ch83, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 48.56
Std Dev 3.381
Entry
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3
4
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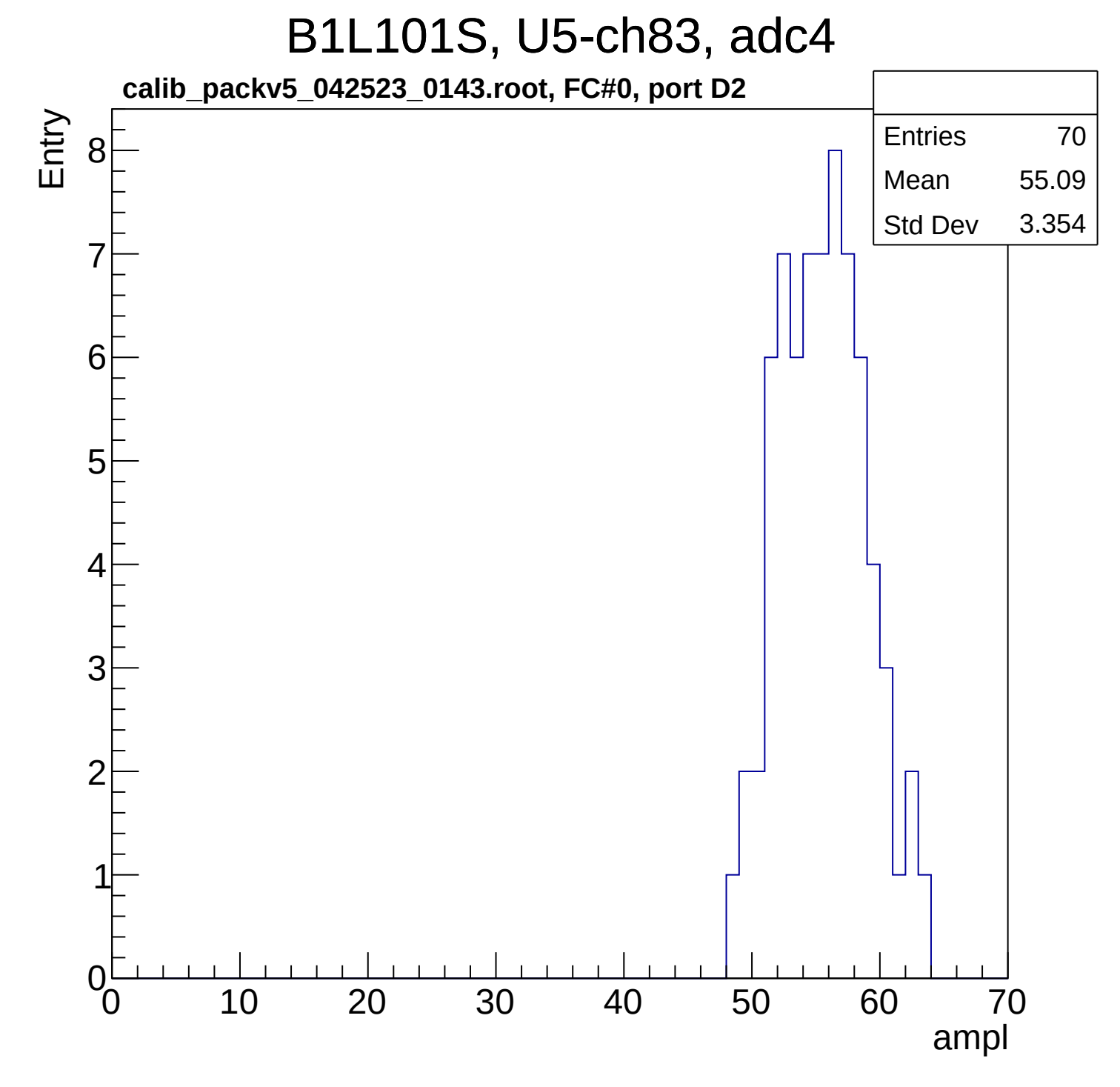
50
60
70
ampl


B1L101S, U5-ch83, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 55.09
Std Dev 3.354
Entry
ampl
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0
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60
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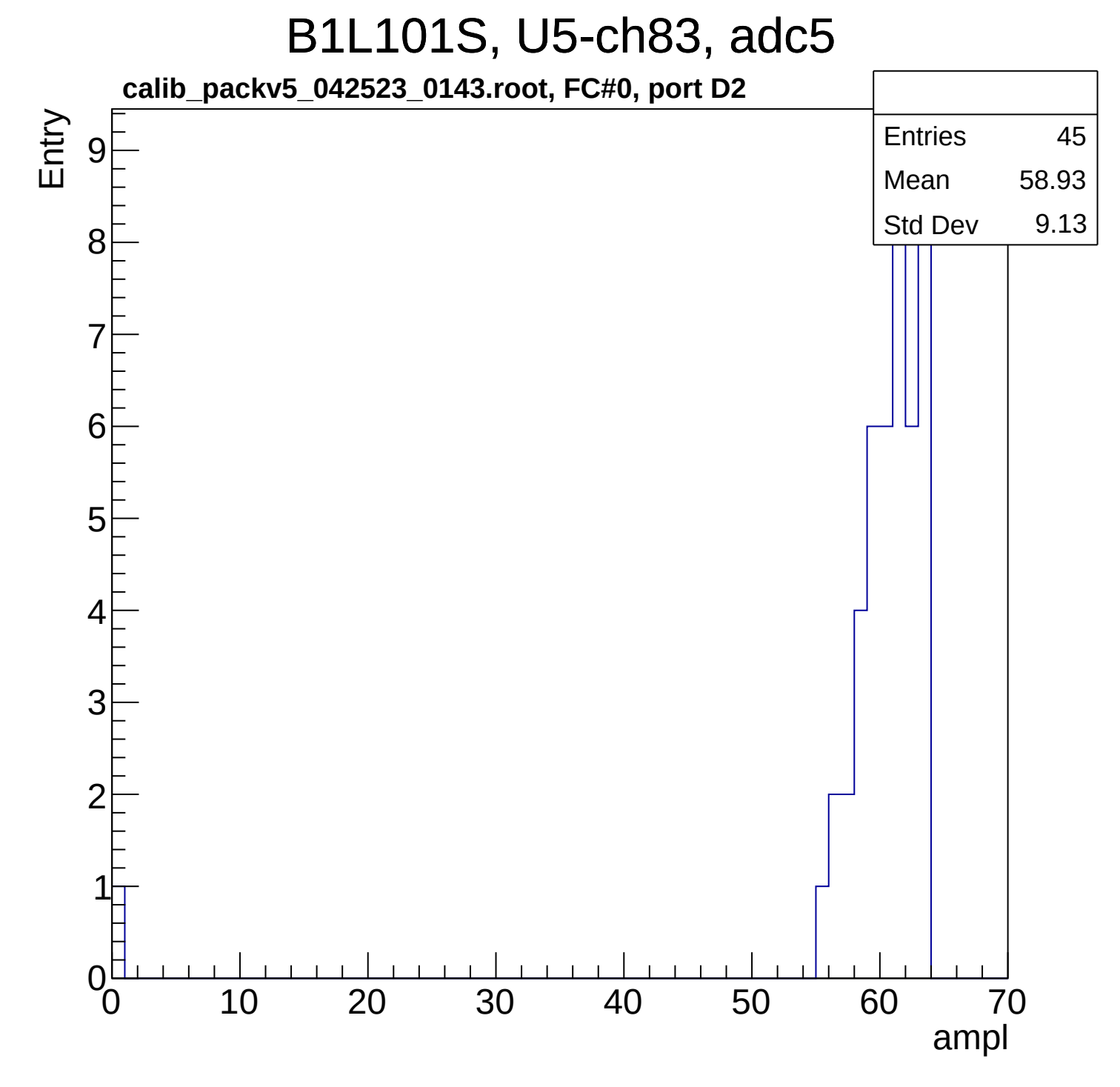
B1L101S, U5-ch83, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 58.93
Std Dev 9.13
Entry
ampl
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30
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50
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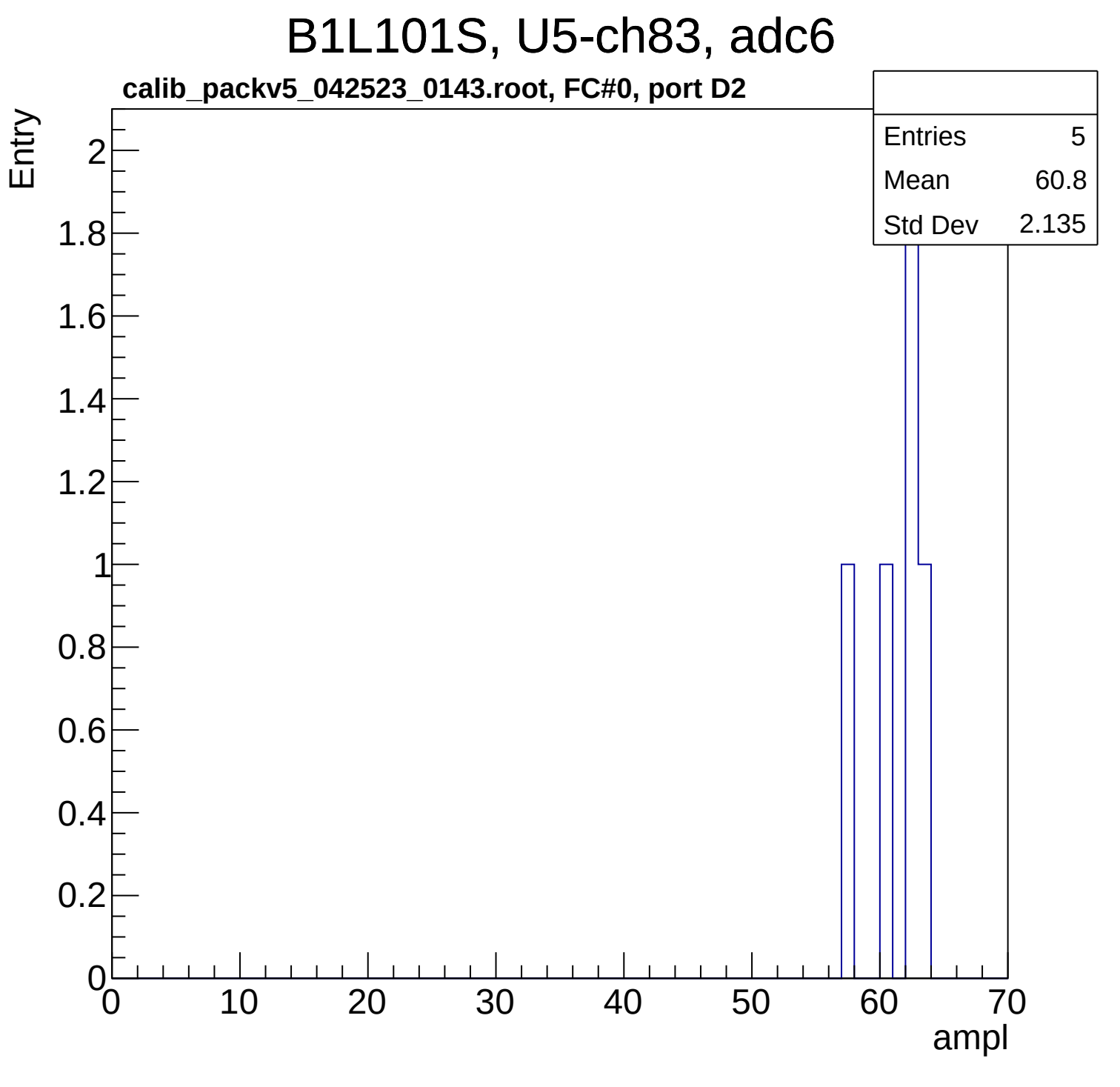
1
2
3
4
5
6
7
8
9


B1L101S, U5-ch83, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 60.8
Std Dev 2.135
Entry
ampl
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0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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40
50
60
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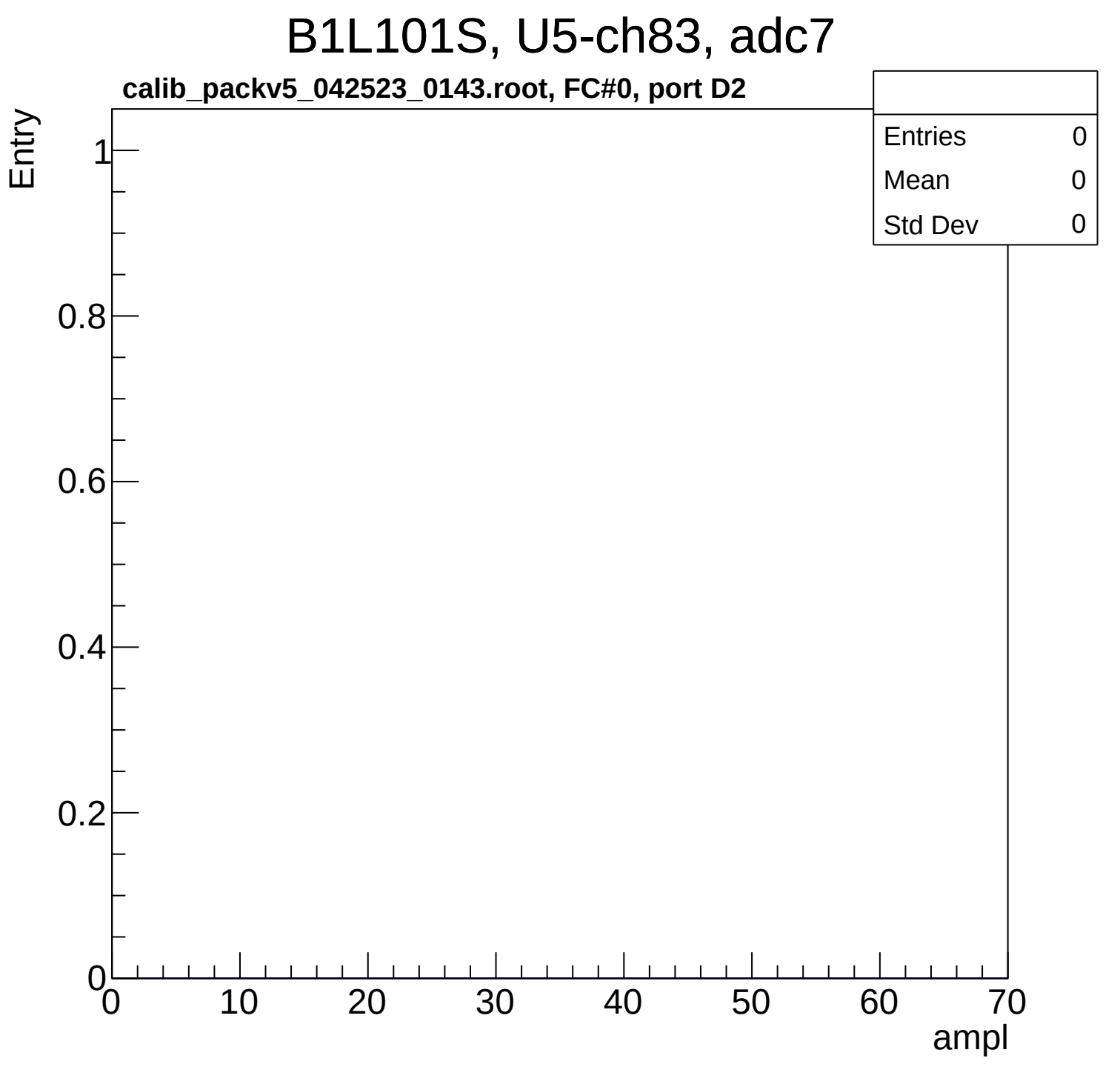
B1L101S, U5-ch83, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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0.6
0.4
0.2
0
0
10
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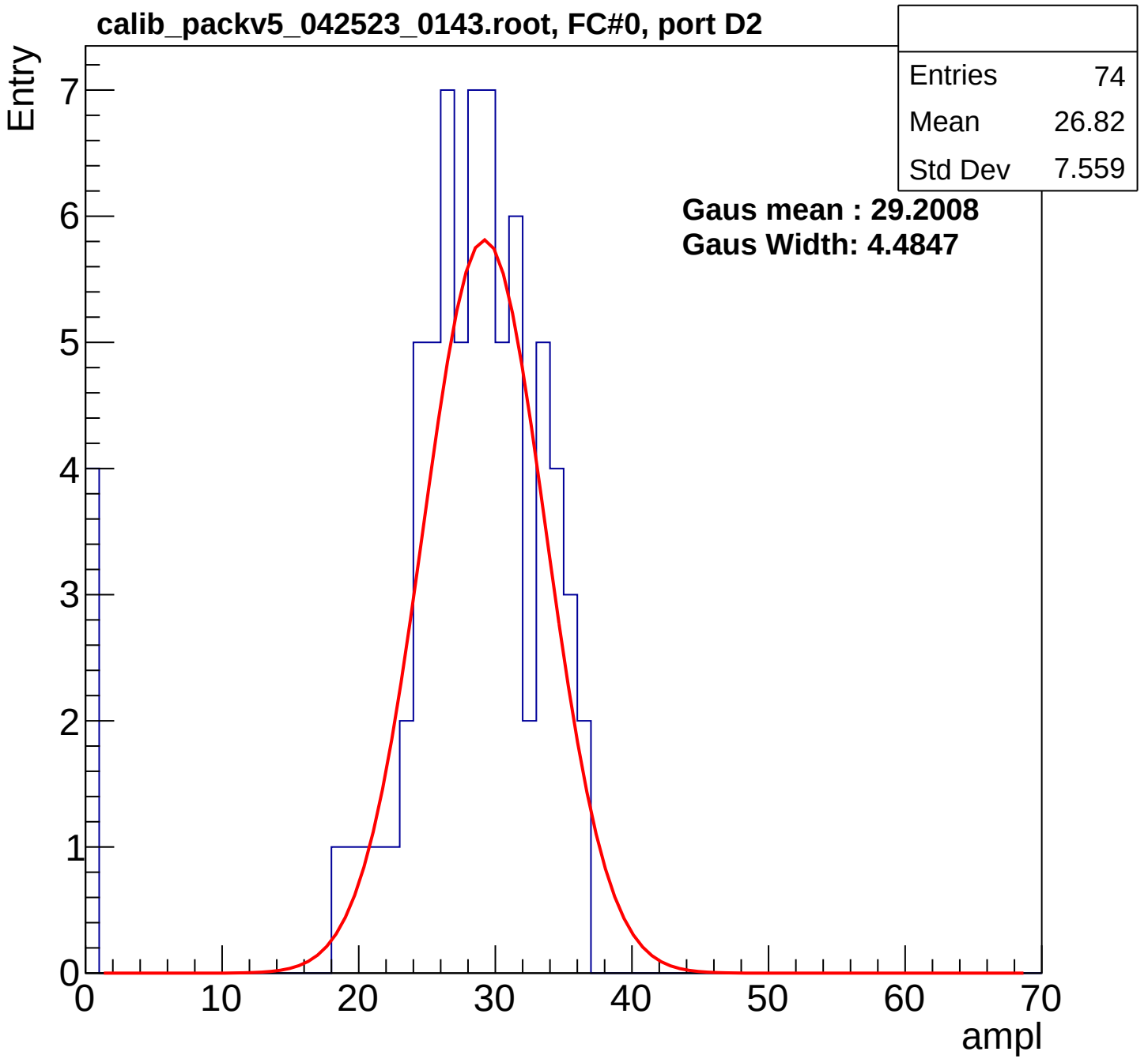
50
60
70
ampl


B1L101S, U5-ch84, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 26.82
Std Dev 7.559
Gaus mean : 29.2008
Gaus Width: 4.4847
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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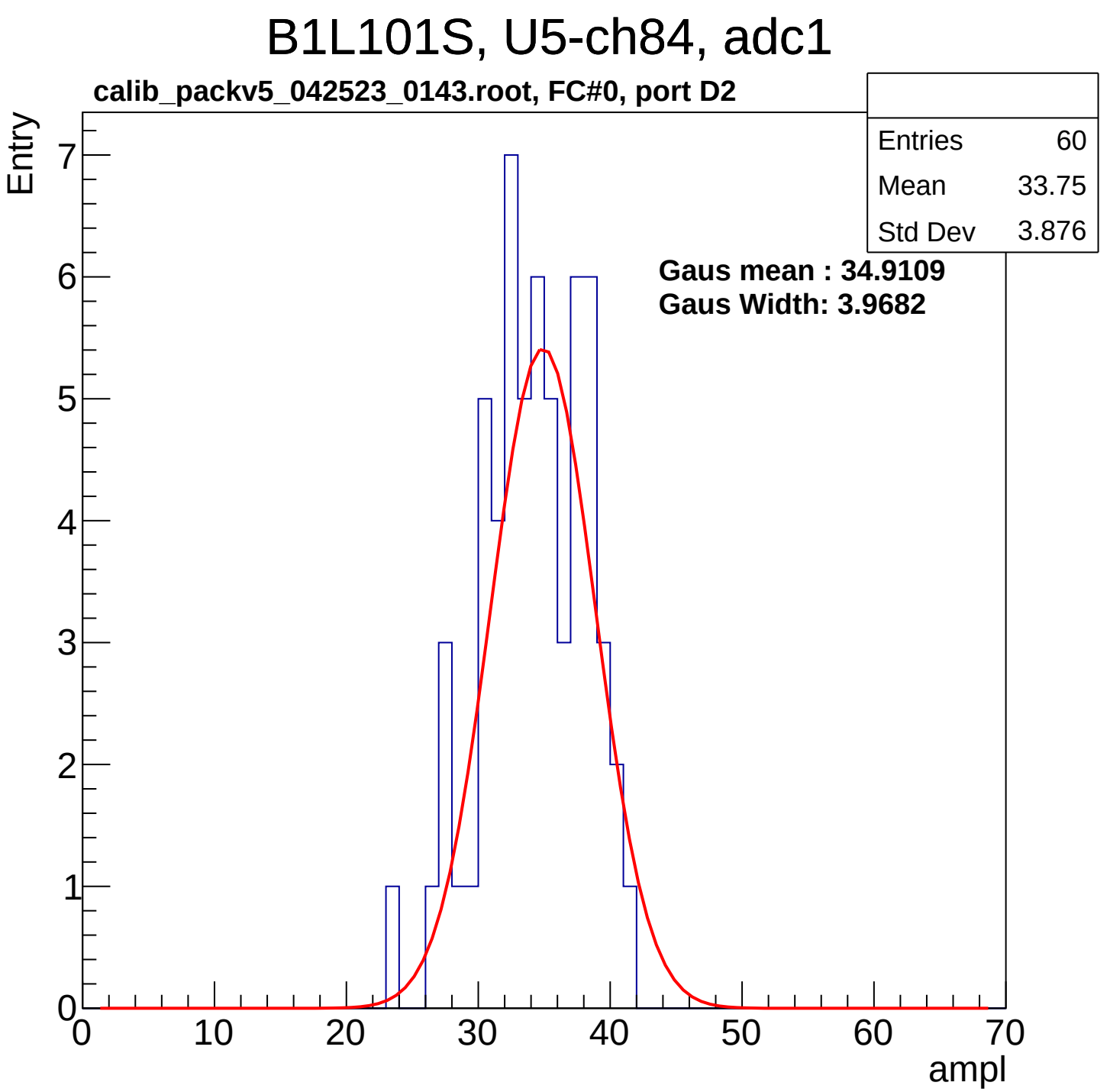
60
70


B1L101S, U5-ch84, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 33.75
Std Dev 3.876
Gaus mean : 34.9109
Gaus Width: 3.9682
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
50
60
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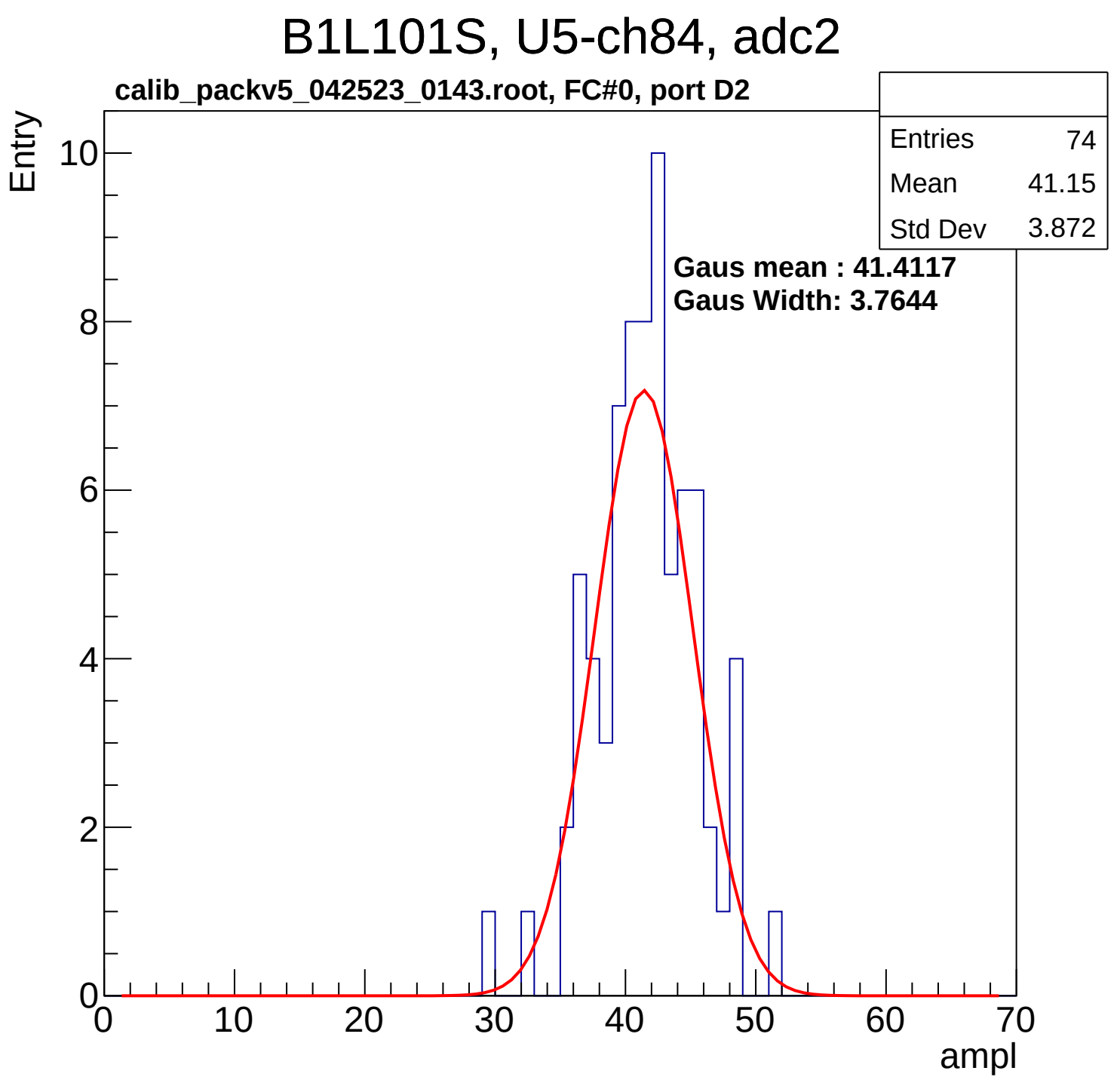
B1L101S, U5-ch84, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 41.15
Std Dev 3.872
Gaus mean : 41.4117
Gaus Width: 3.7644
Entry
ampl
0
2
4
6
8
10
0
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20
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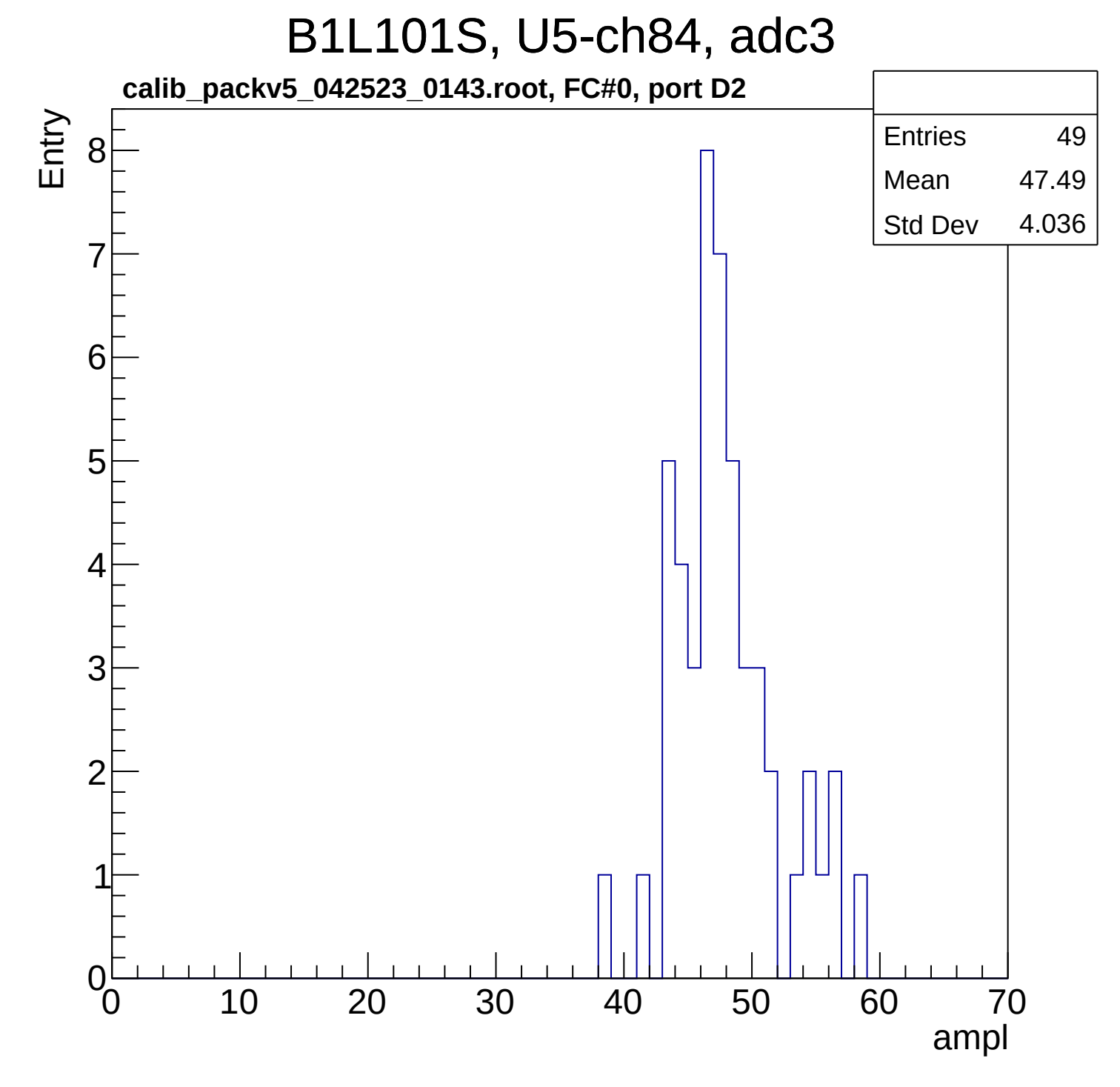
40
50
60
70


B1L101S, U5-ch84, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 47.49
Std Dev 4.036
Entry
ampl
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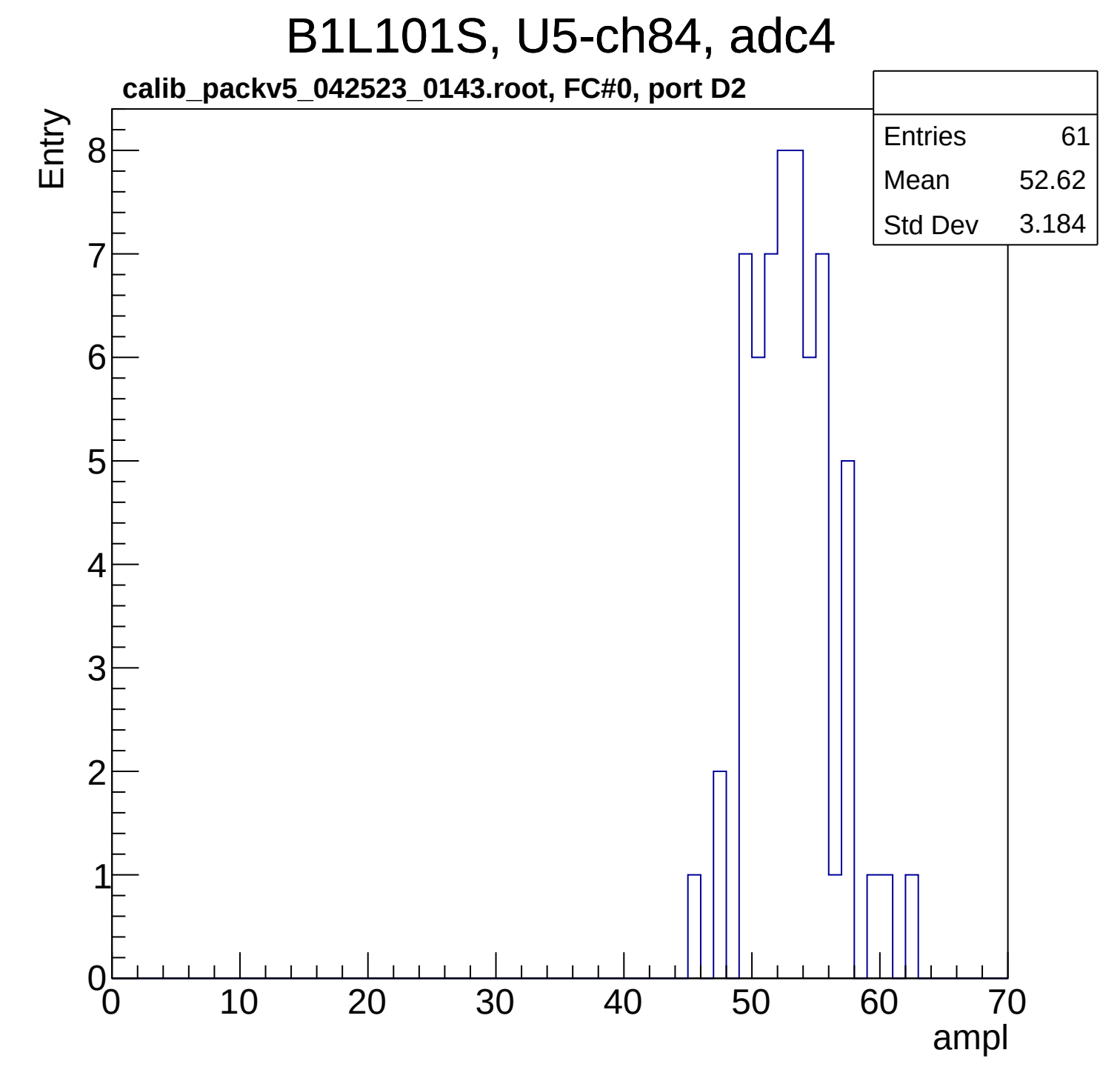
B1L101S, U5-ch84, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 52.62
Std Dev 3.184
Entry
ampl
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3
4
5
6
7
8
0
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60
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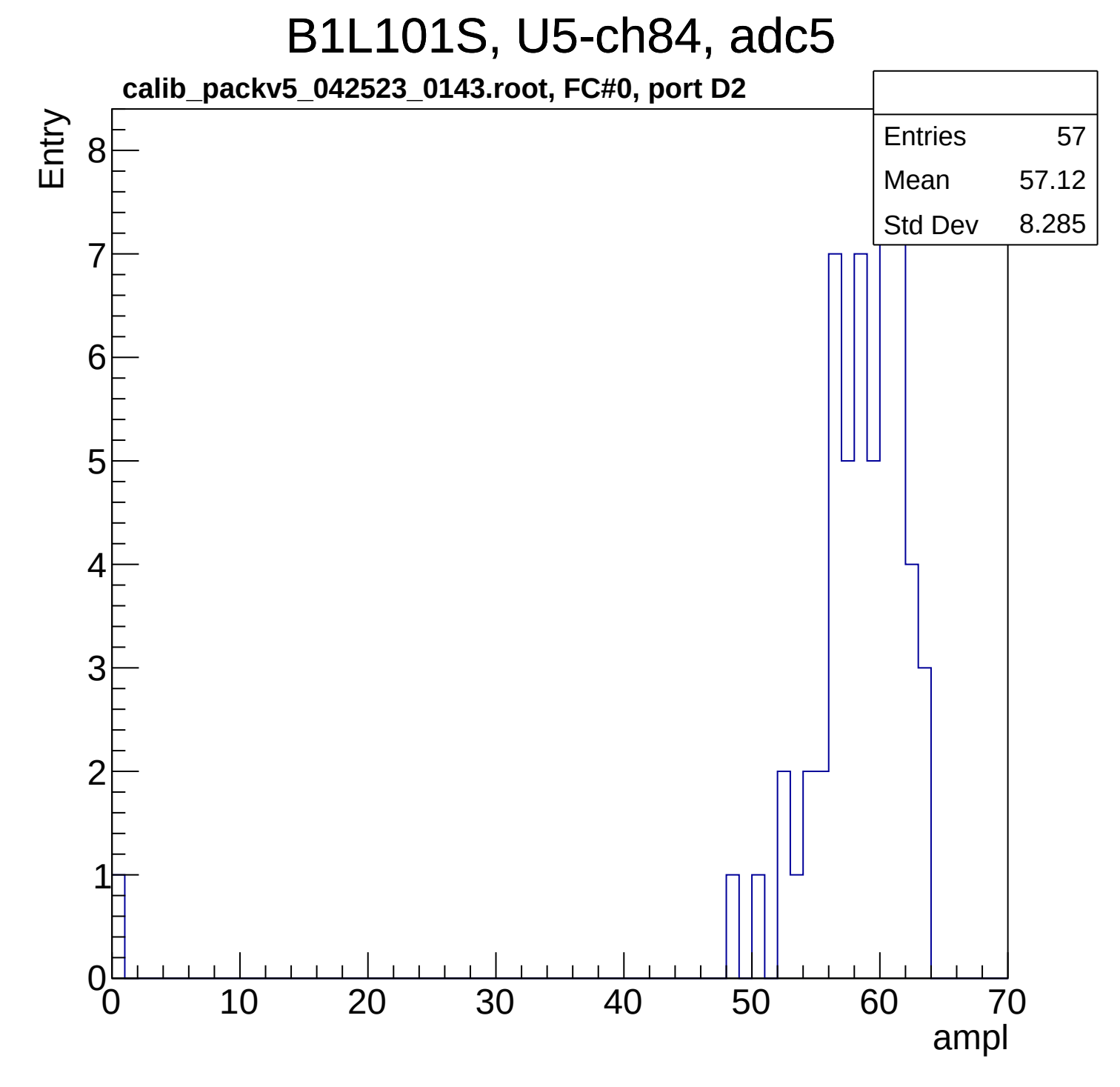
B1L101S, U5-ch84, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 57.12
Std Dev 8.285
Entry
ampl
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3
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7
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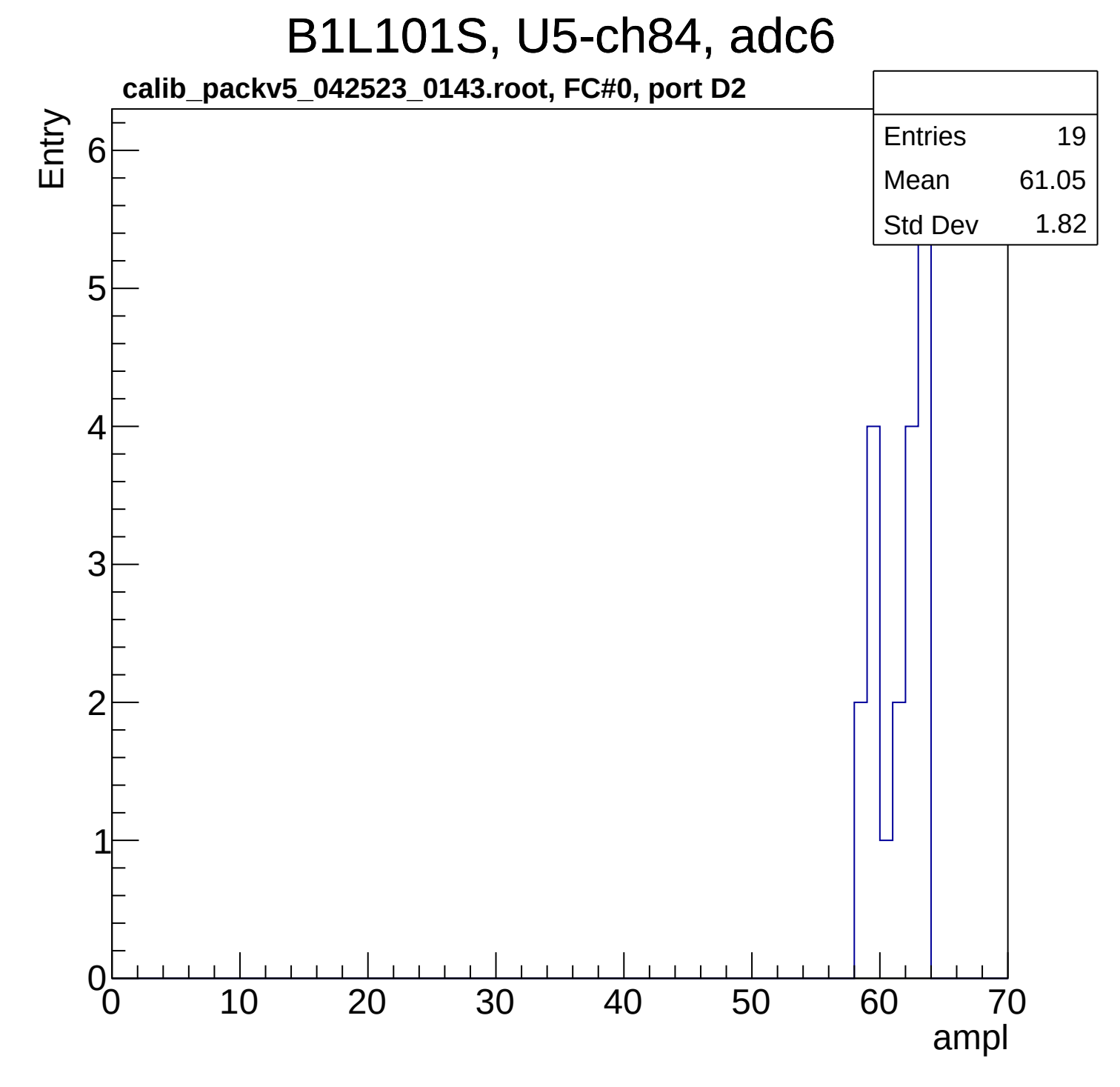
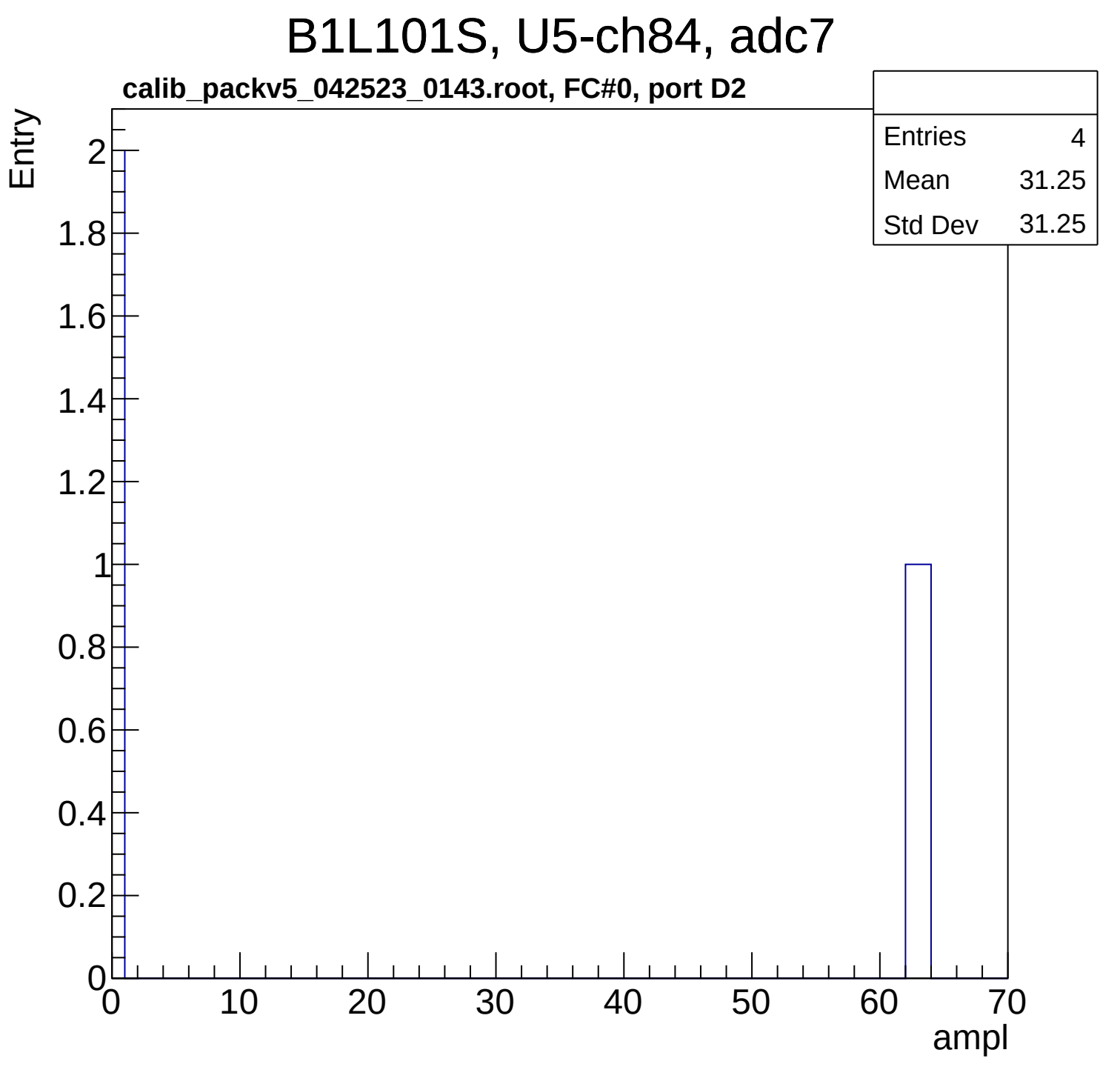

B1L101S, U5-ch84, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 19
Mean 61.05
Std Dev 1.82
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch84, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 31.25
Std Dev 31.25
Entry
ampl
0
0.2
0.4
0.6
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1.2
1.4
1.6
1.8
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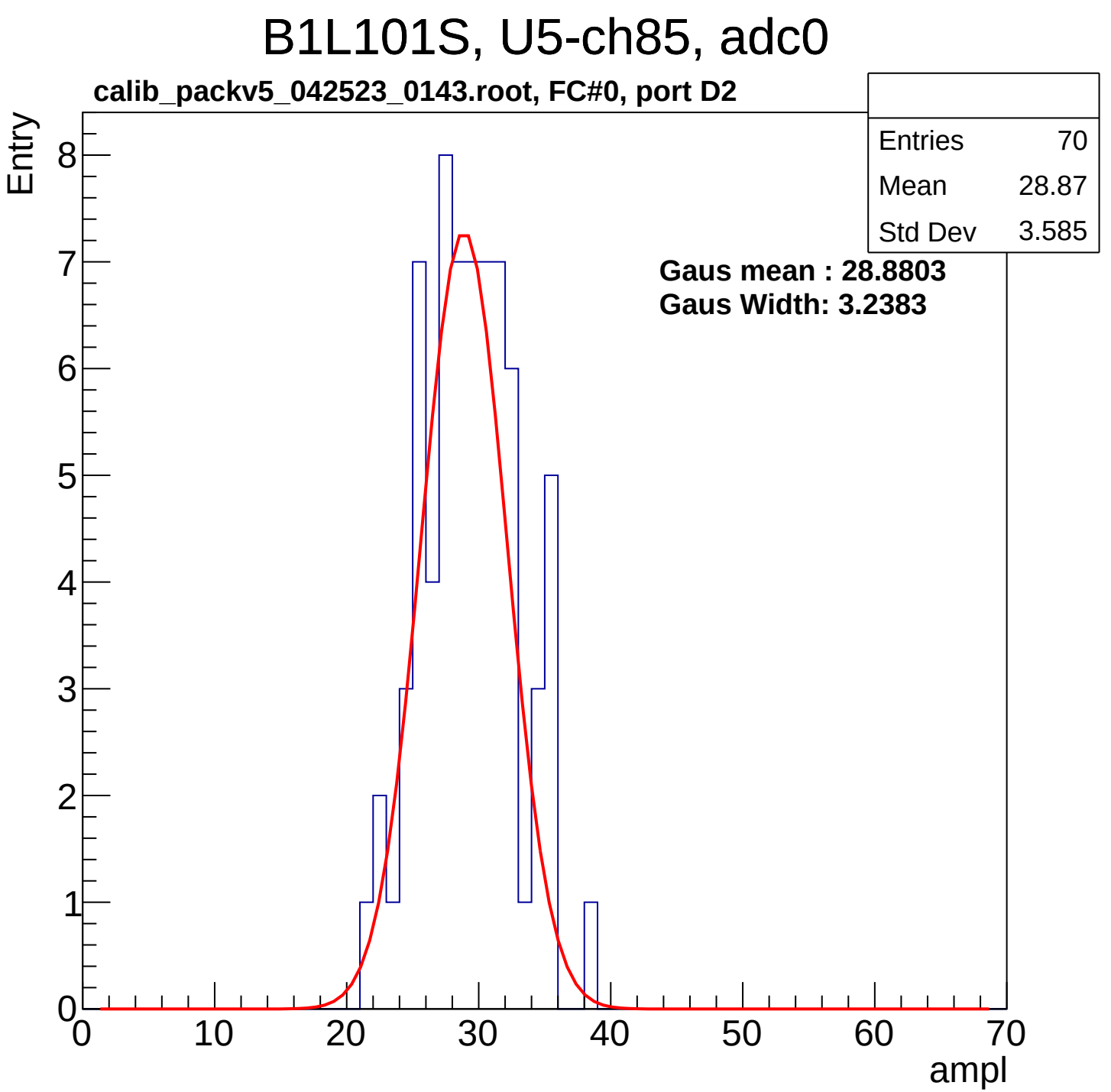
B1L101S, U5-ch85, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 28.87
Std Dev 3.585
Gaus mean : 28.8803
Gaus Width: 3.2383
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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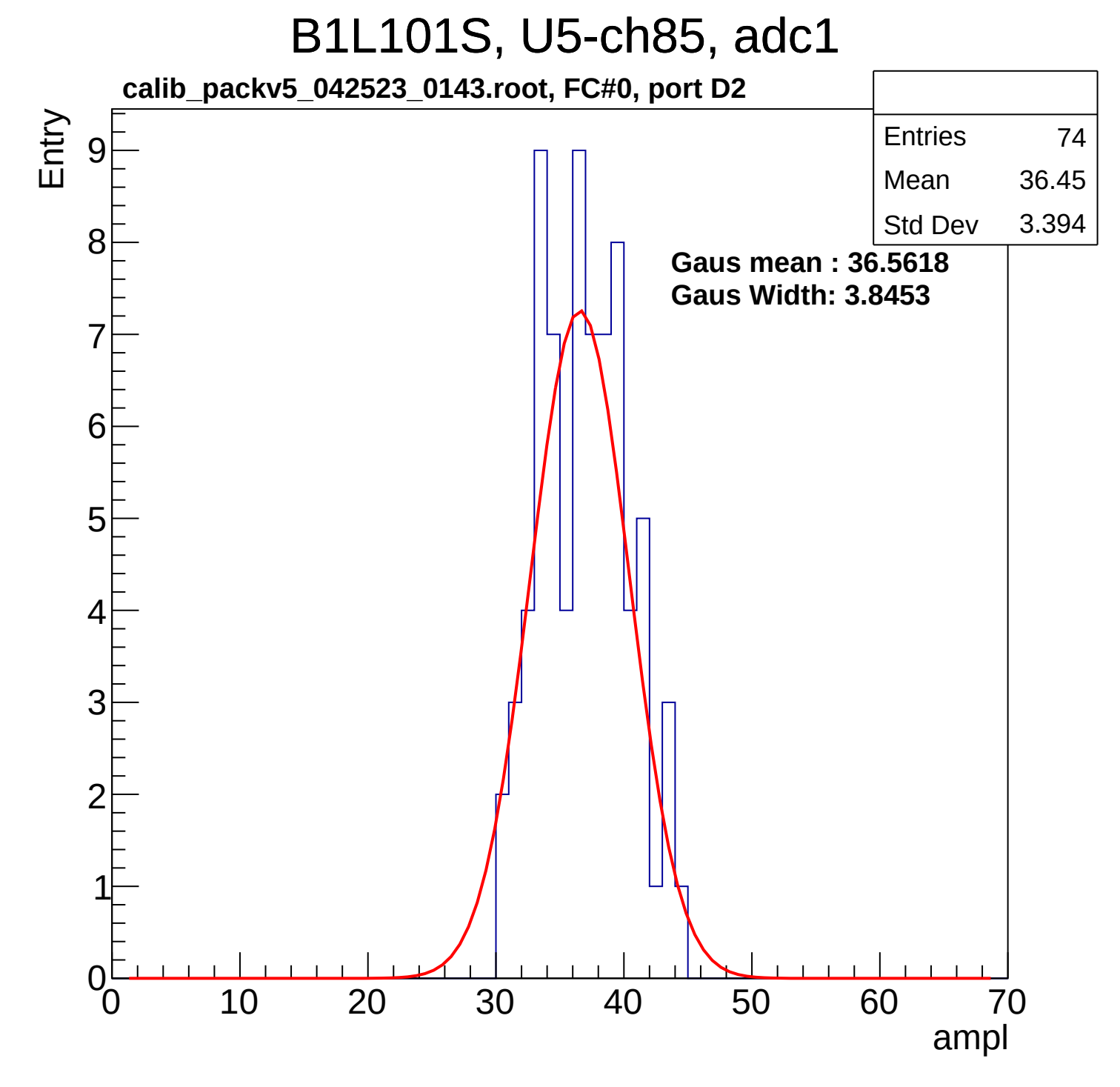
B1L101S, U5-ch85, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 36.45
Std Dev 3.394
Gaus mean : 36.5618
Gaus Width: 3.8453
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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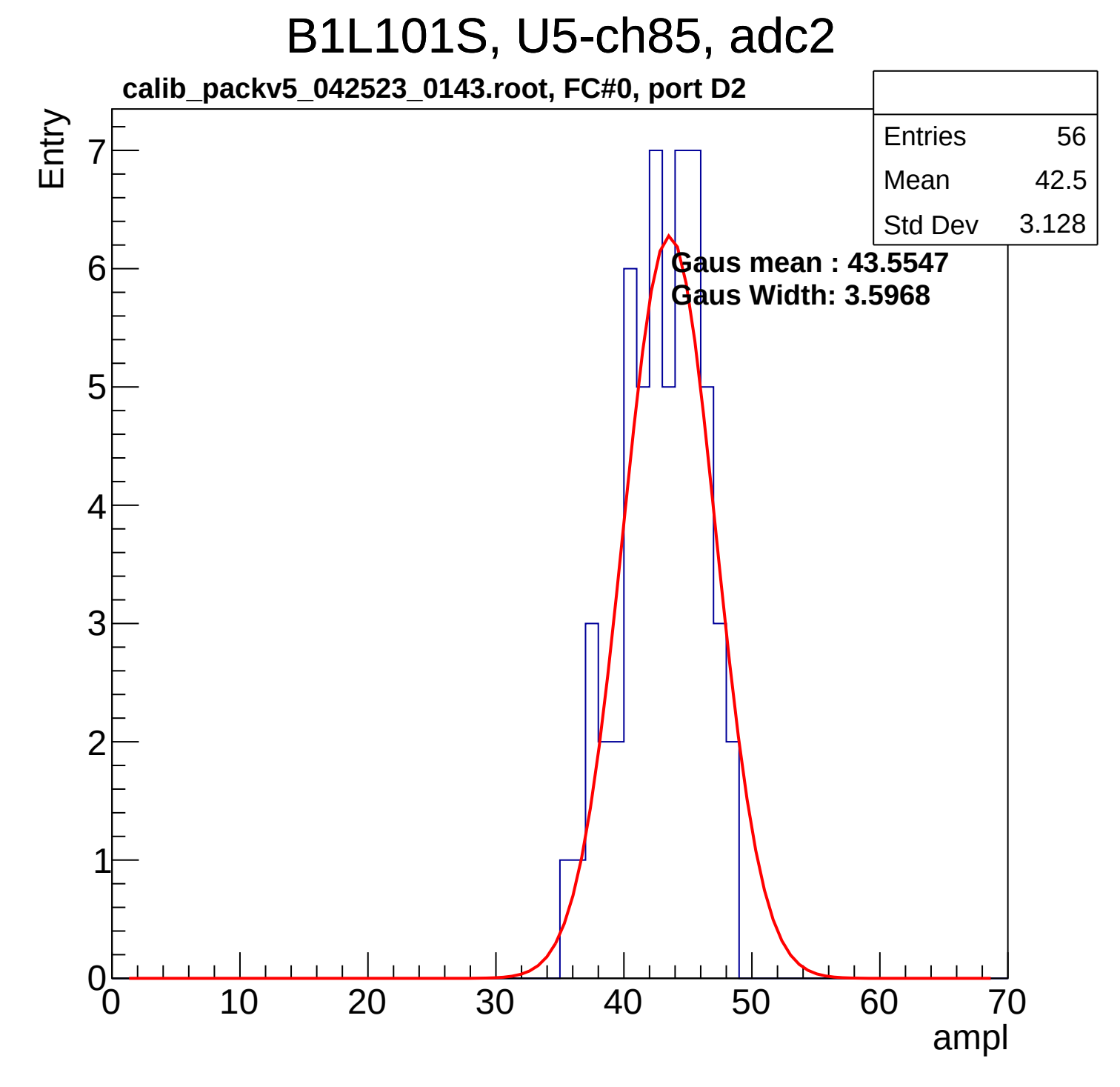
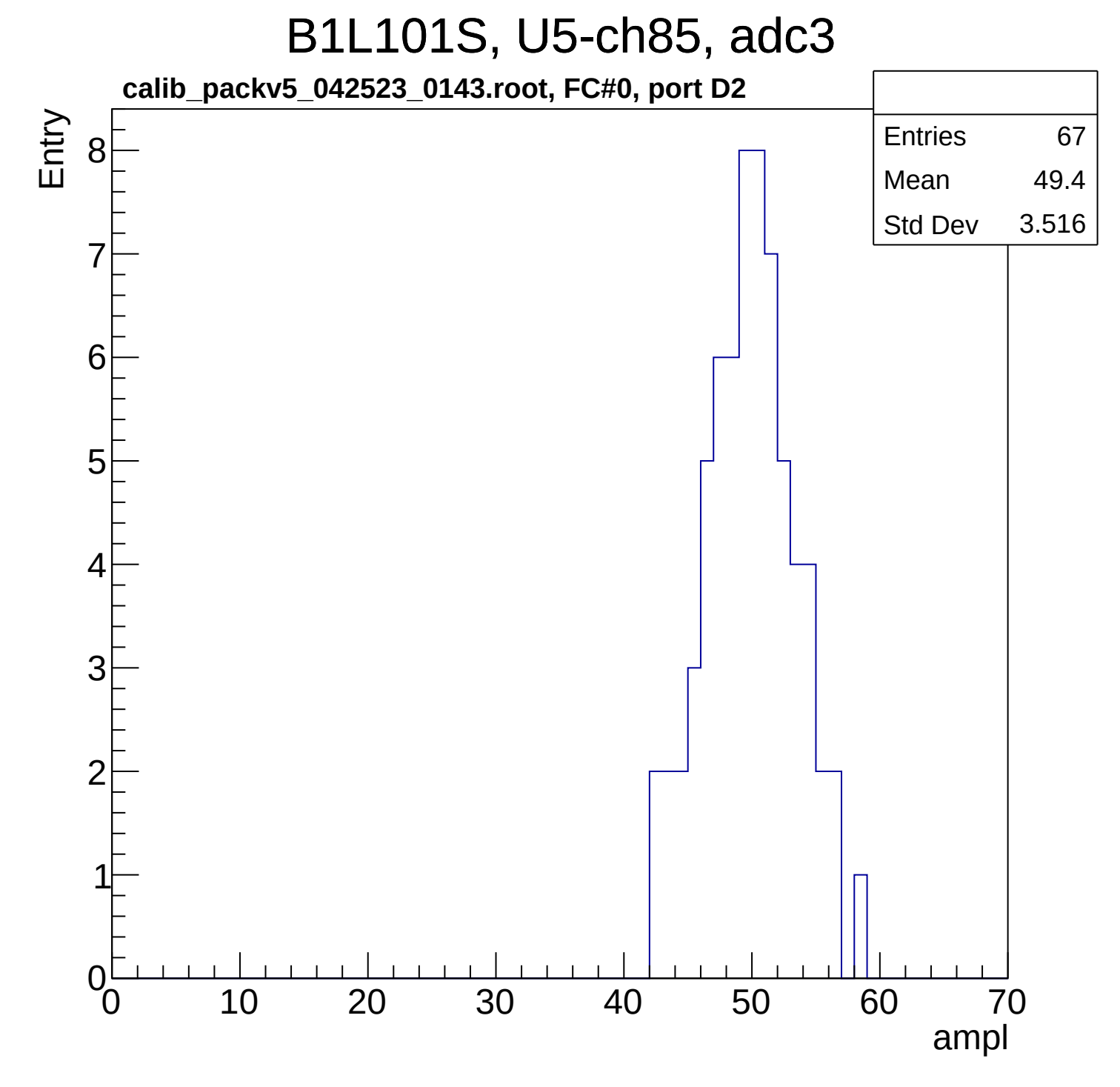

B1L101S, U5-ch85, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 42.5
Std Dev 3.128
Gaus mean : 43.5547
Gaus Width: 3.5968
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch85, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 49.4
Std Dev 3.516
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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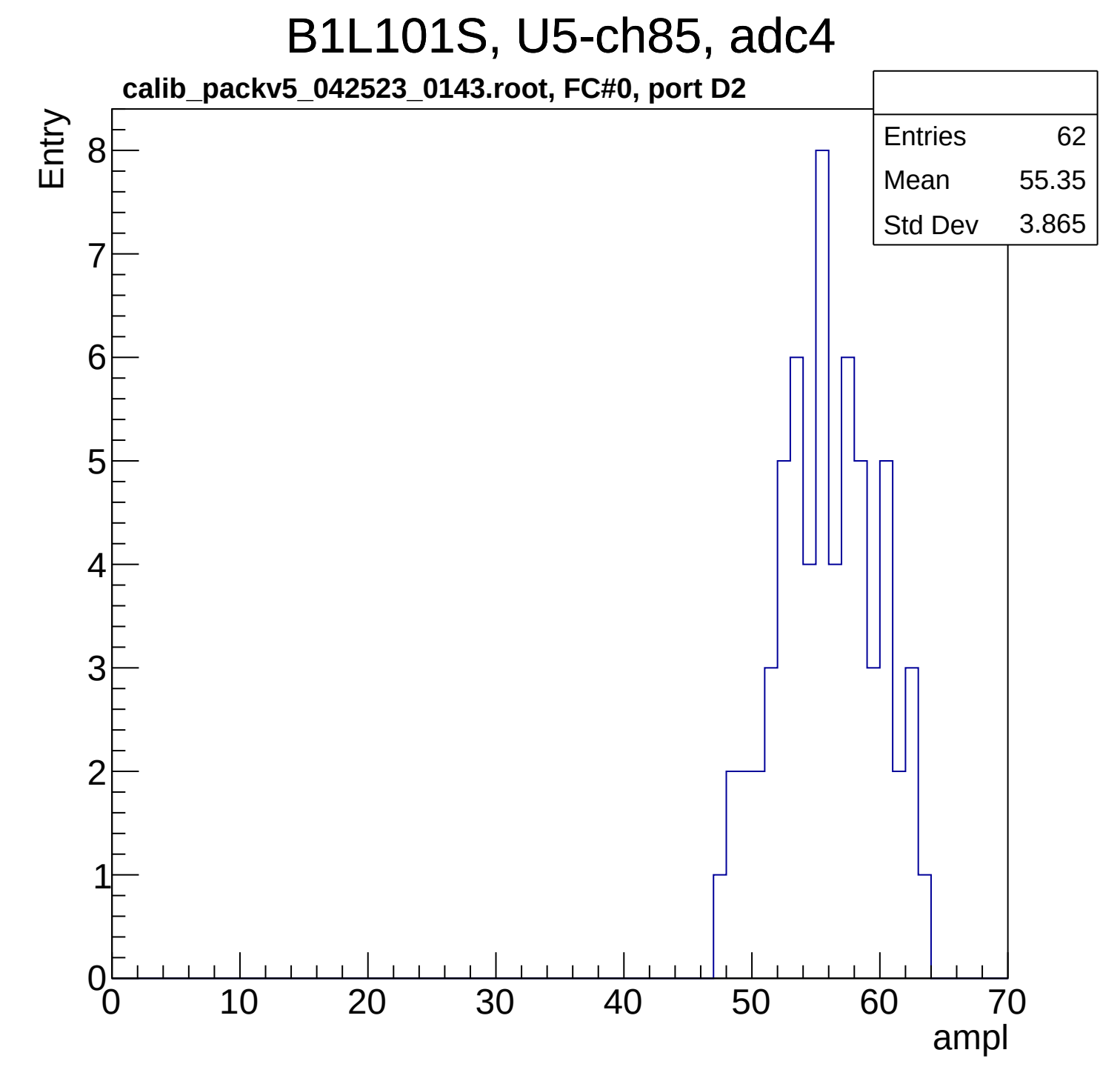
B1L101S, U5-ch85, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 55.35
Std Dev 3.865
Entry
ampl
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2
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4
5
6
7
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0
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40
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60
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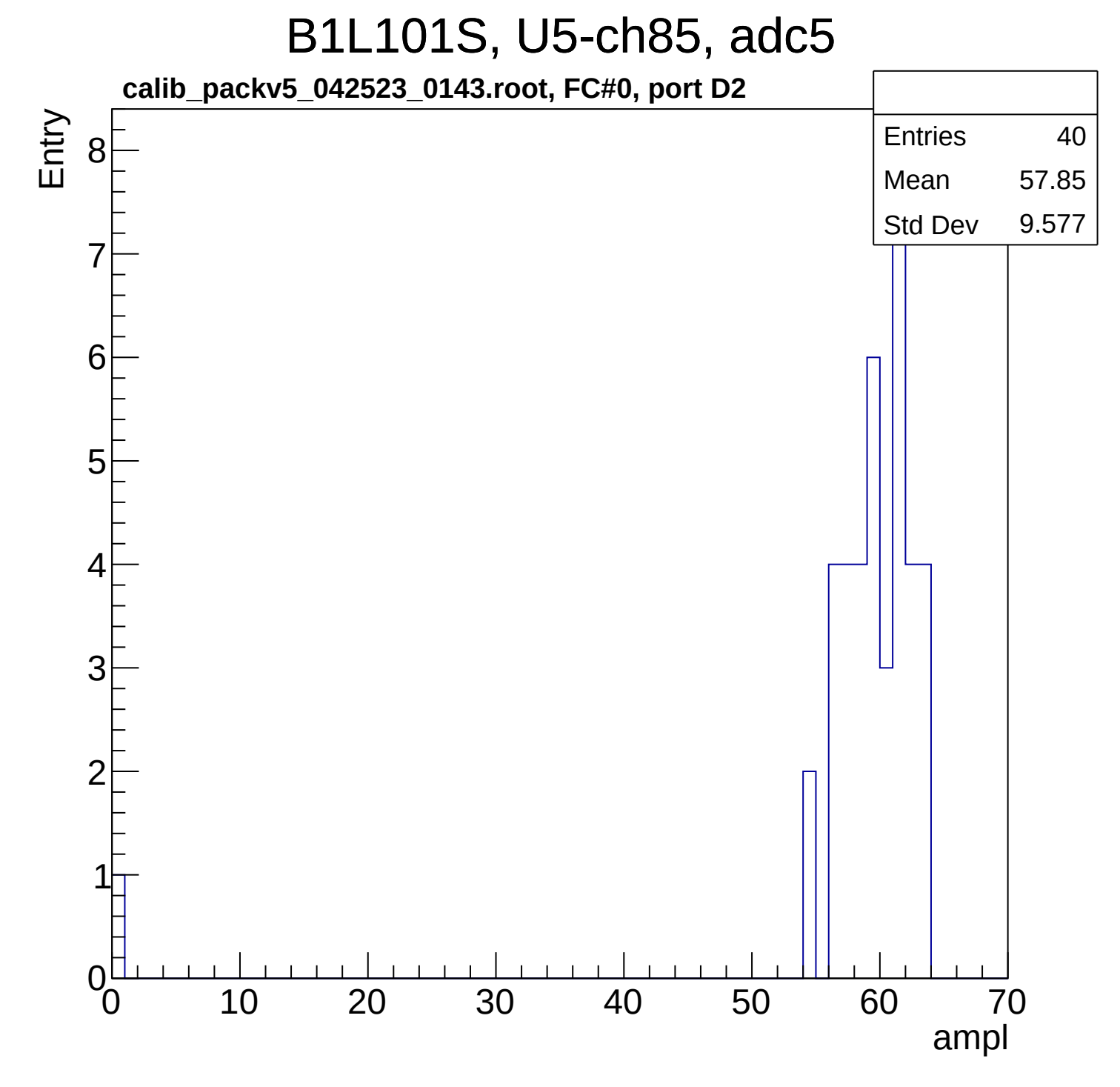
B1L101S, U5-ch85, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 40
Mean 57.85
Std Dev 9.577
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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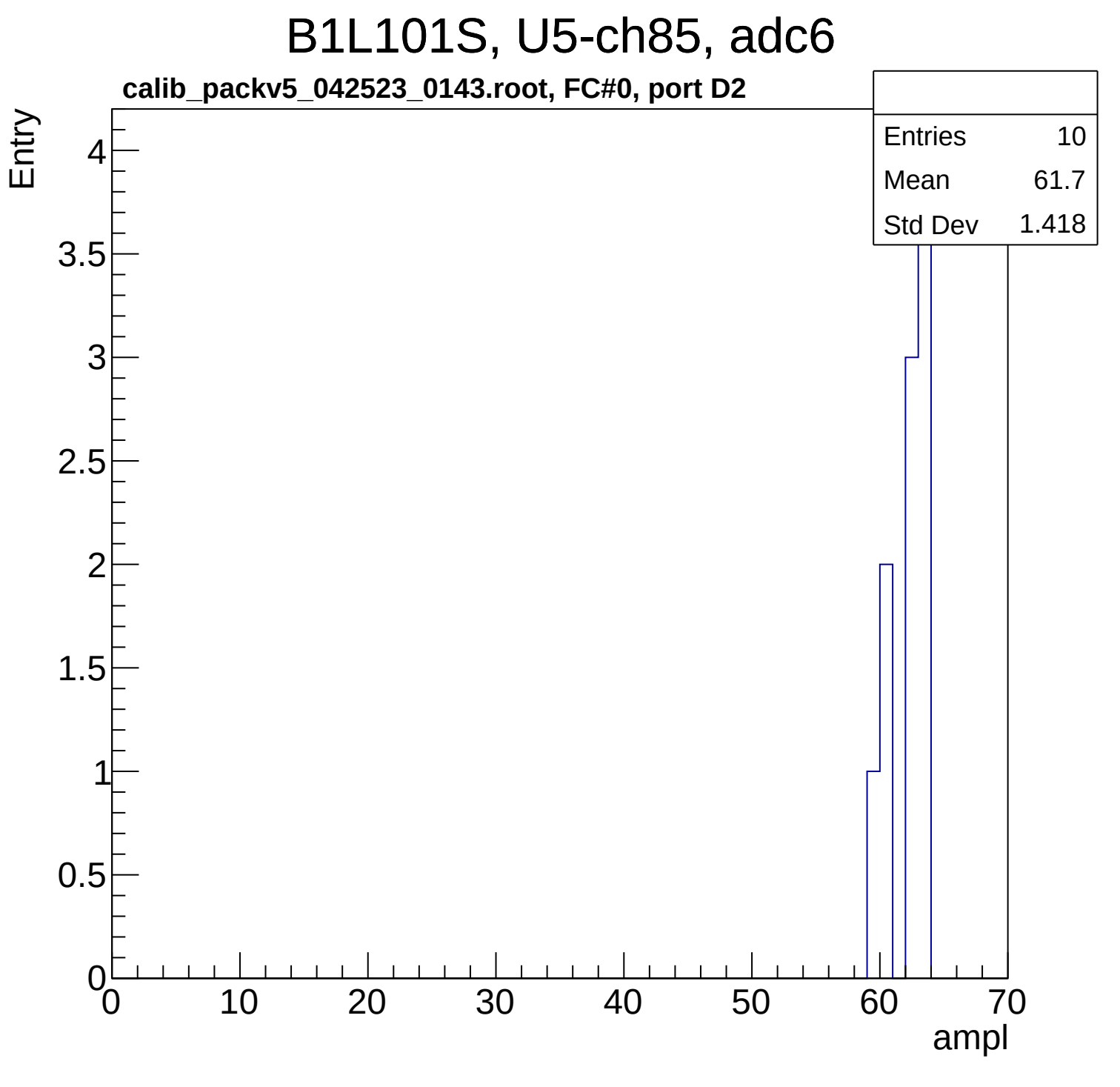
B1L101S, U5-ch85, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 61.7
Std Dev 1.418
Entry
ampl
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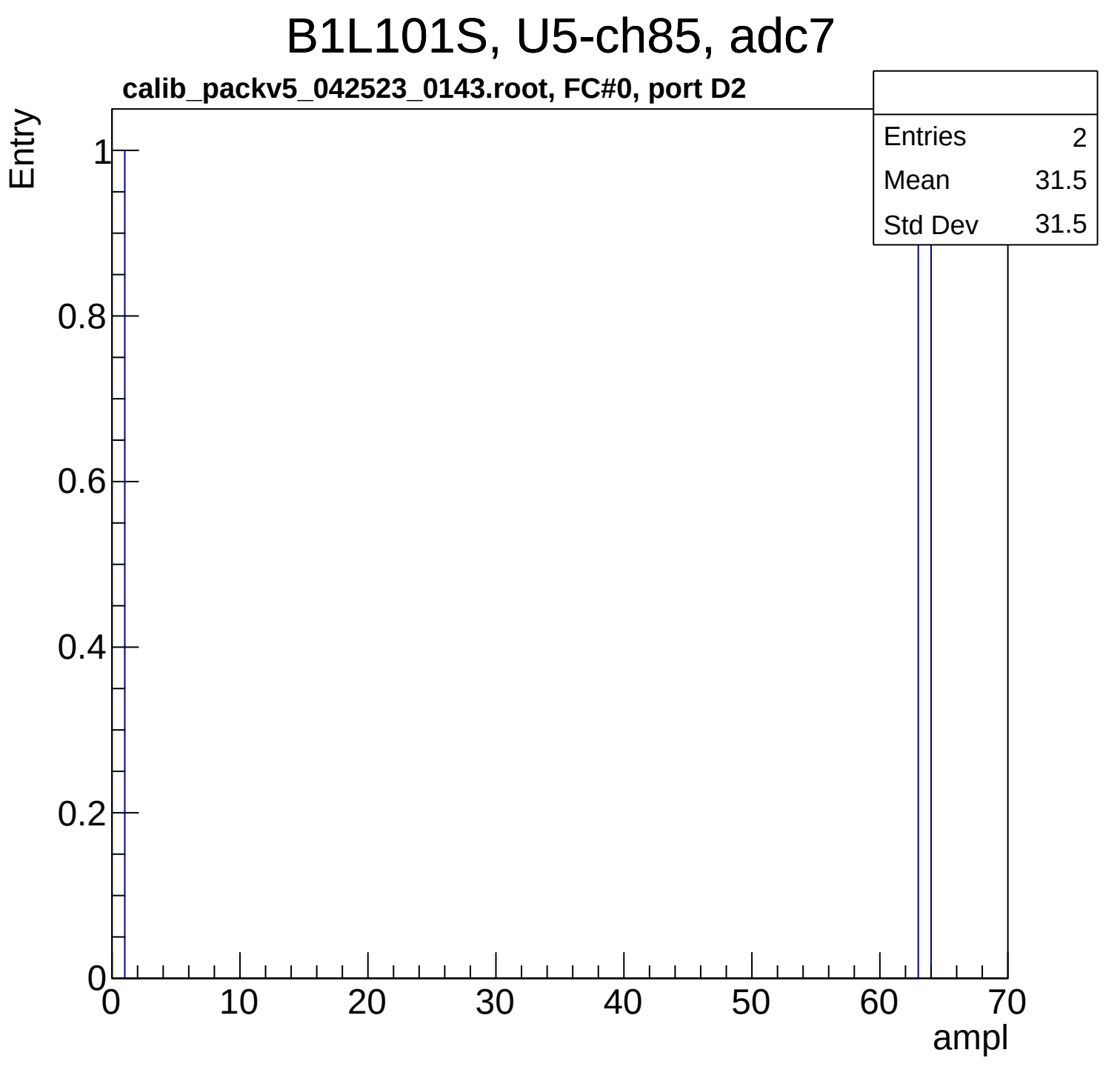
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L101S, U5-ch85, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
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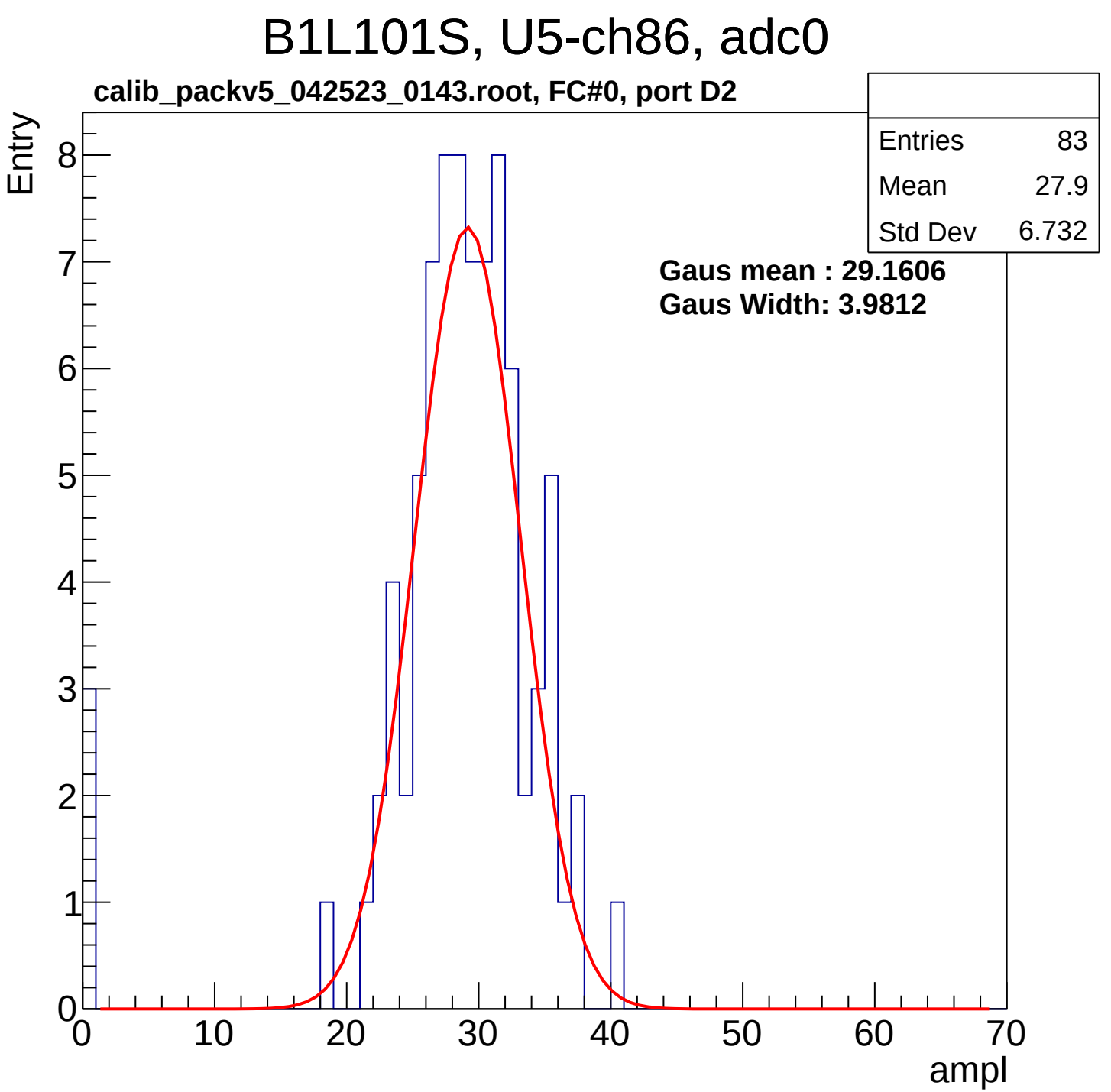
50
60
70
ampl


B1L101S, U5-ch86, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 83
Mean 27.9
Std Dev 6.732
Gaus mean : 29.1606
Gaus Width: 3.9812
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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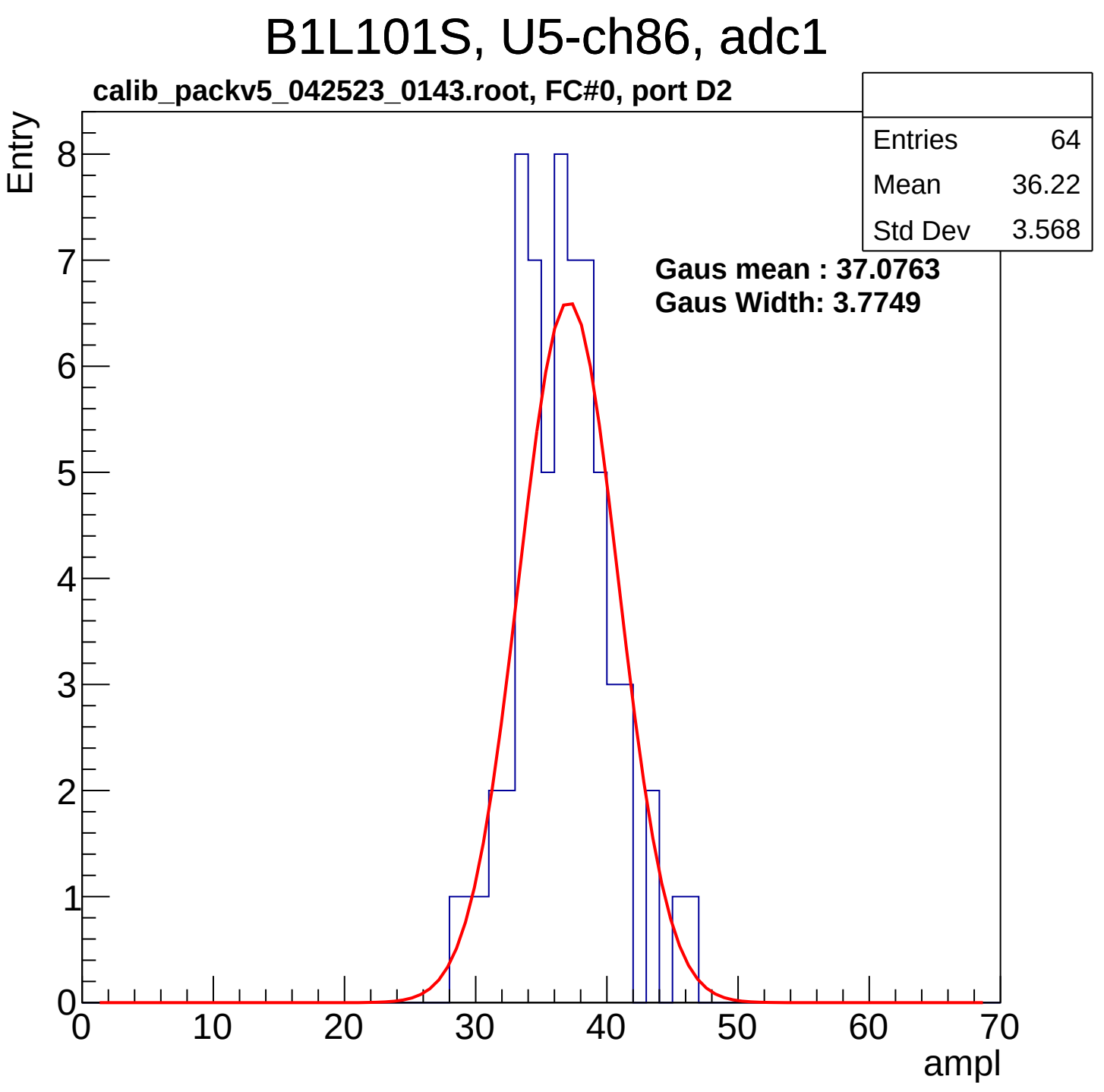
B1L101S, U5-ch86, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 36.22
Std Dev 3.568
Gaus mean : 37.0763
Gaus Width: 3.7749
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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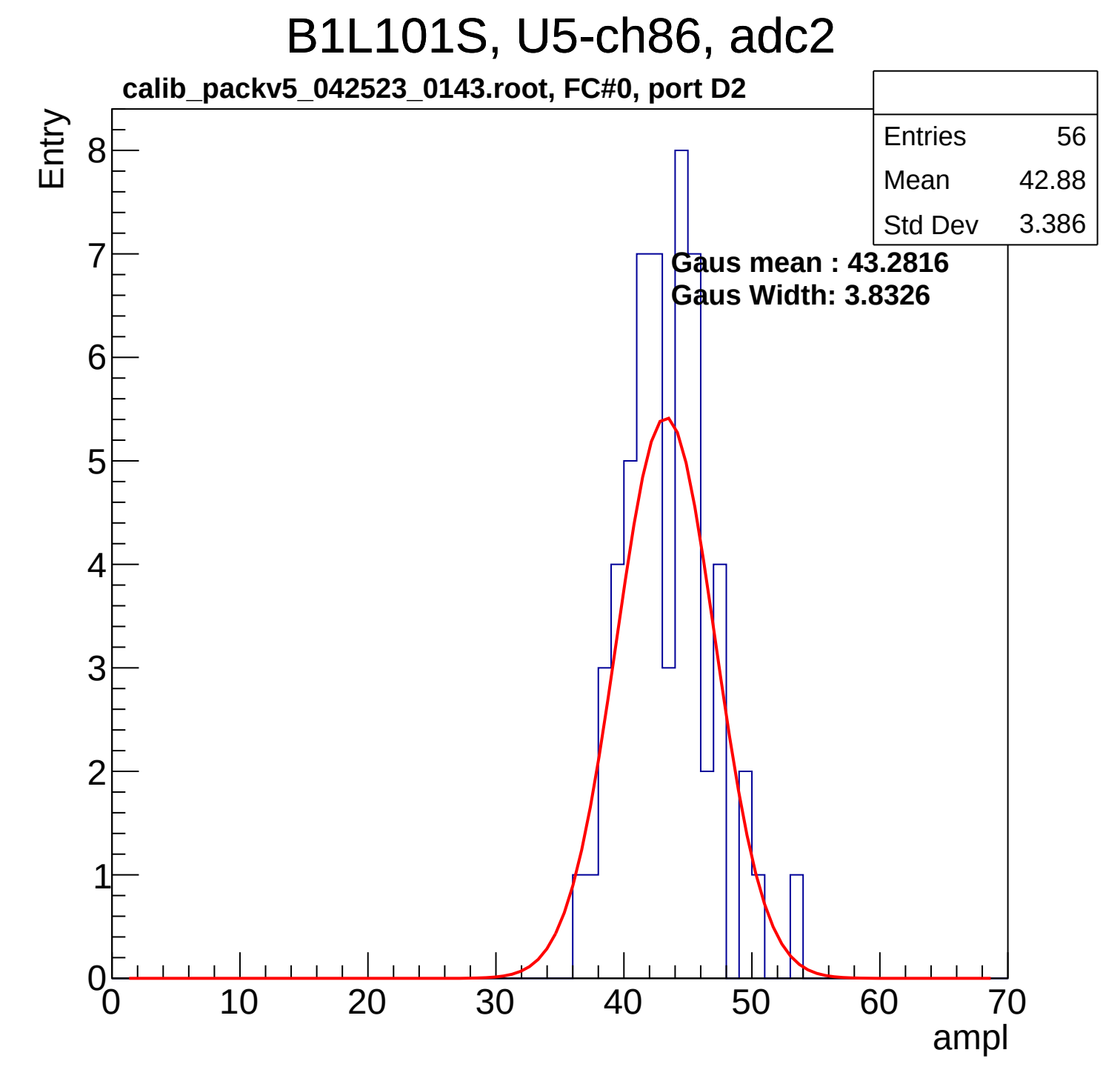
B1L101S, U5-ch86, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 42.88
Std Dev 3.386
Gaus mean : 43.2816
Gaus Width: 3.8326
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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40
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60
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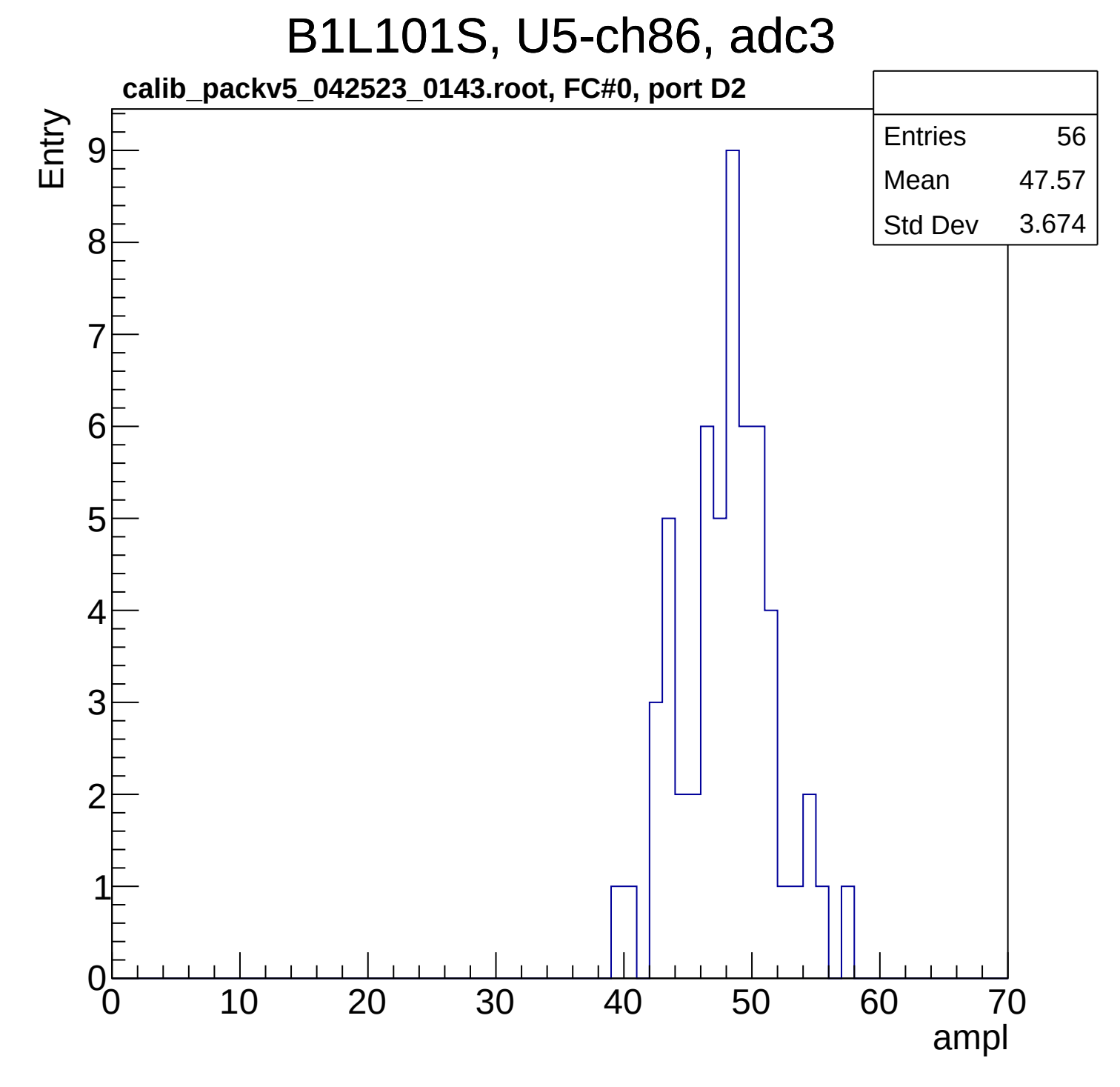
B1L101S, U5-ch86, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 47.57
Std Dev 3.674
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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60
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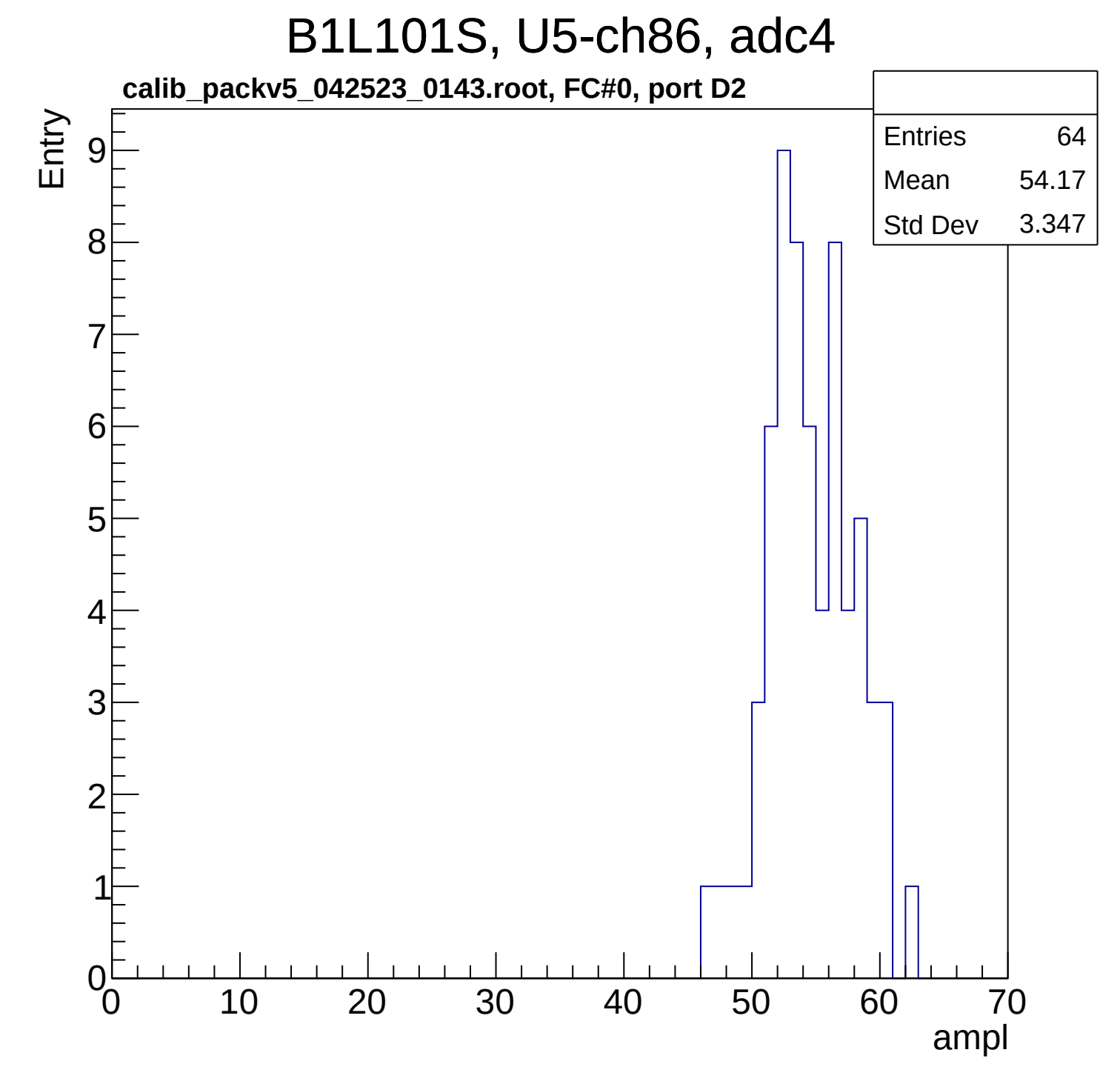
B1L101S, U5-ch86, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 54.17
Std Dev 3.347
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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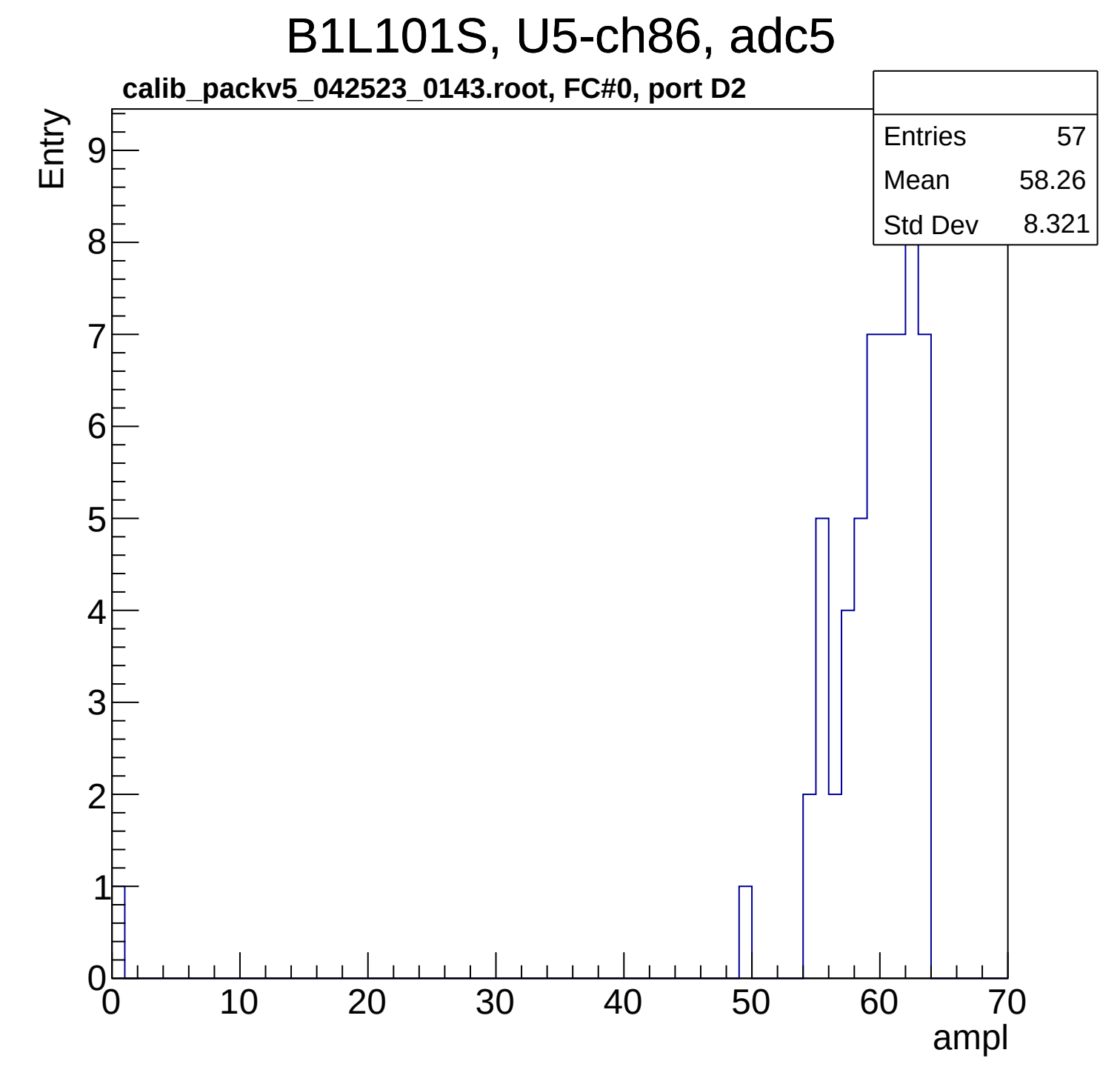
B1L101S, U5-ch86, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 58.26
Std Dev 8.321
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
50
60
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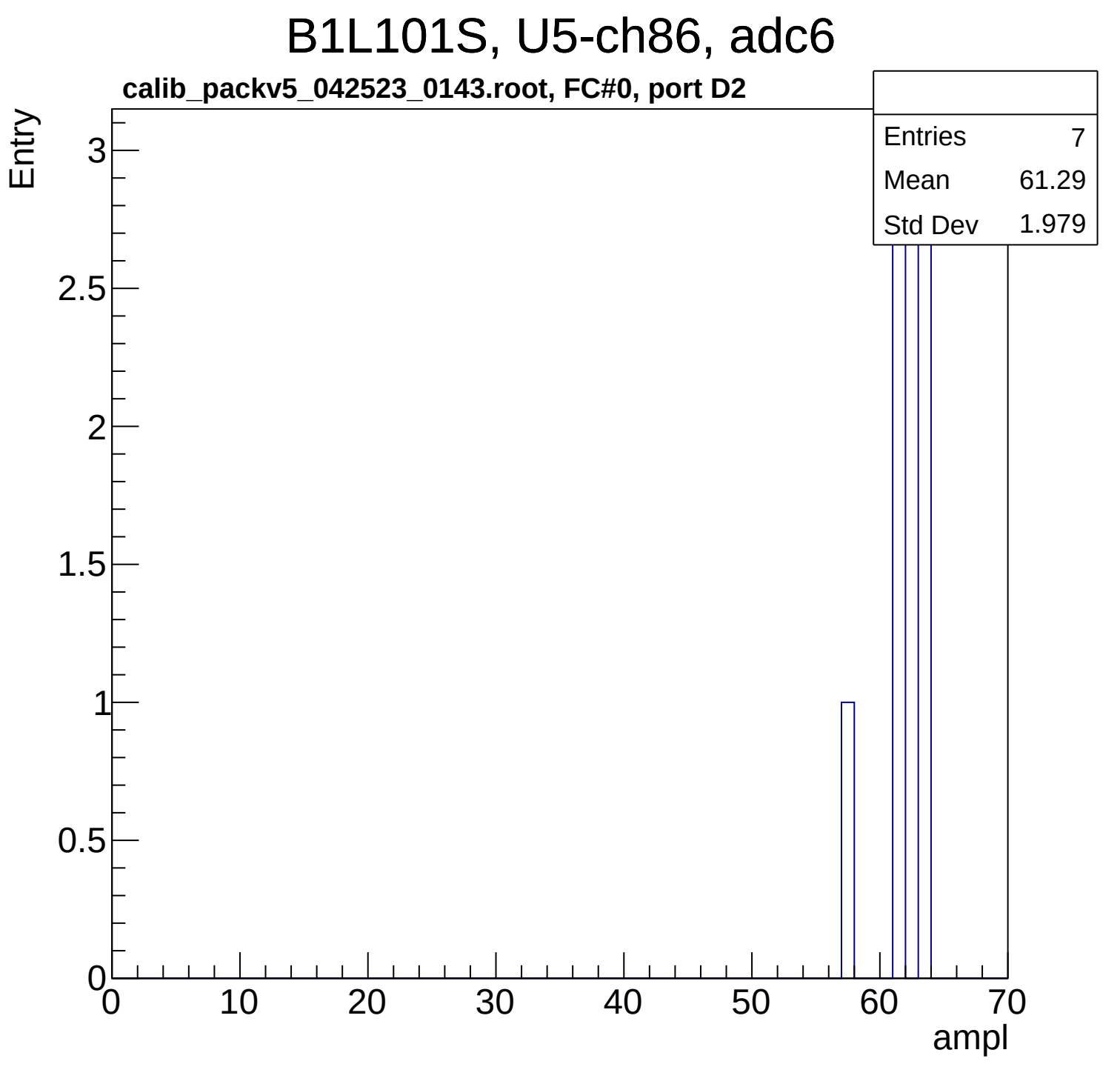
B1L101S, U5-ch86, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 61.29
Std Dev 1.979
Entry
ampl
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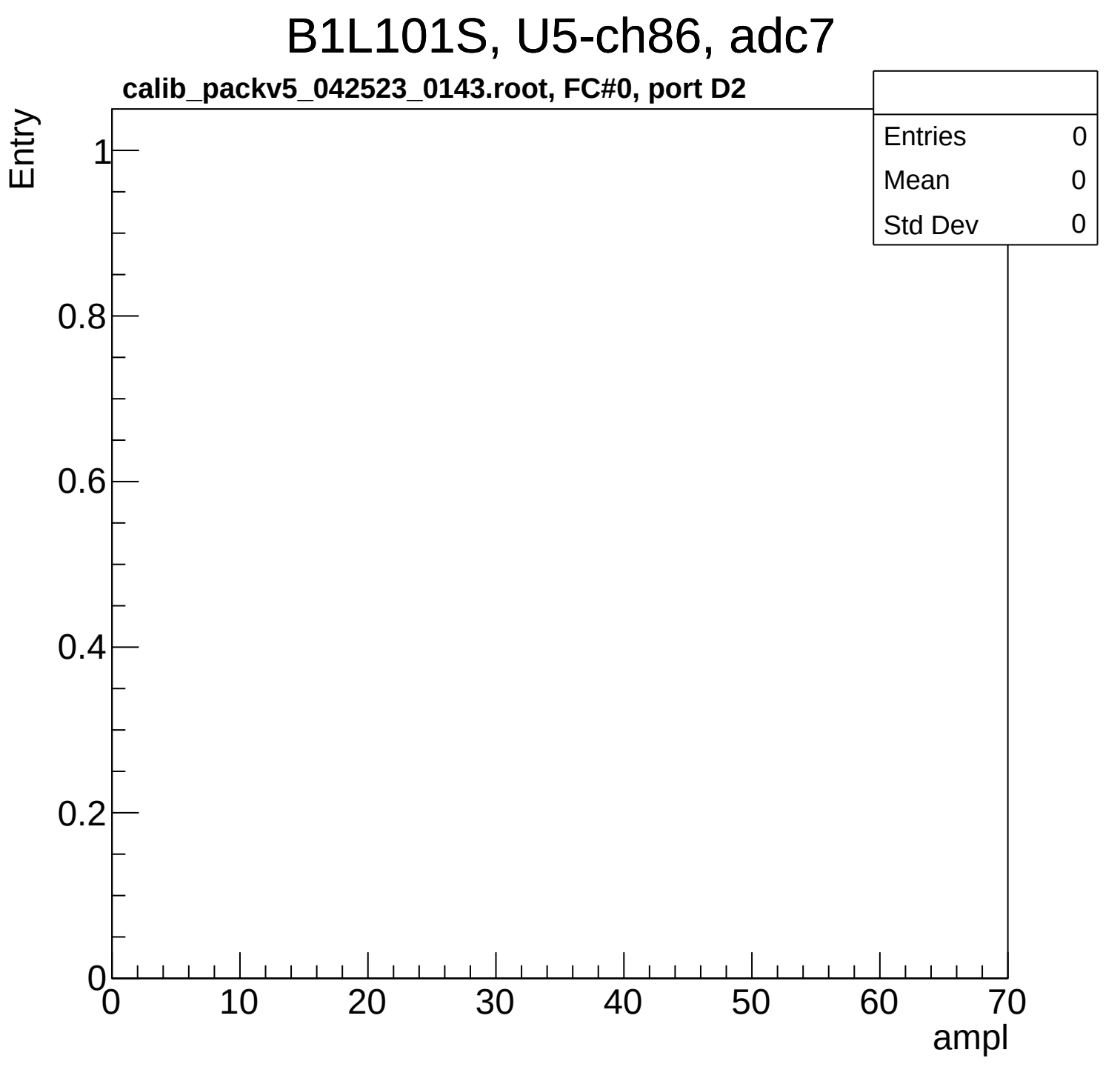
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U5-ch86, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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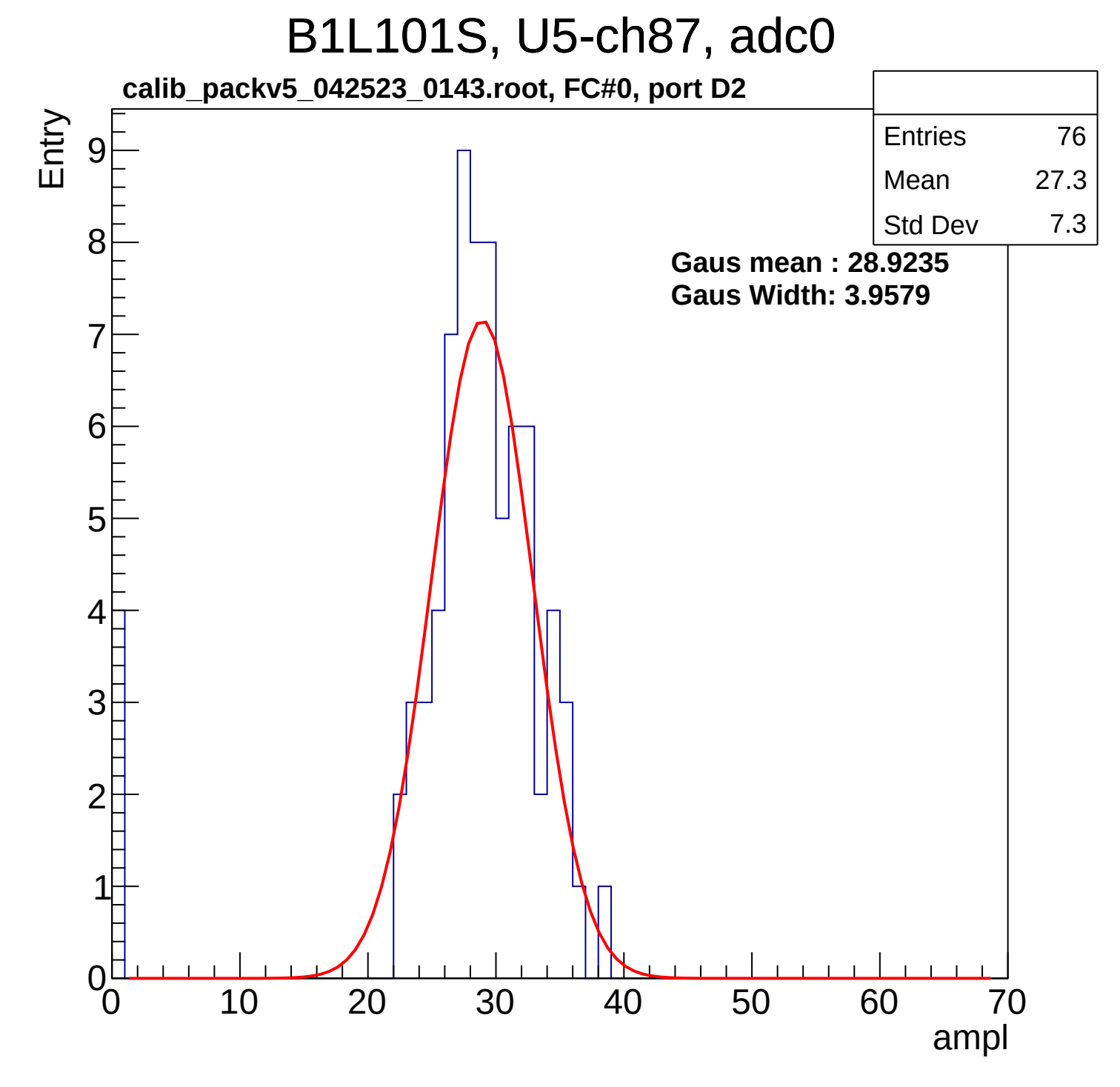
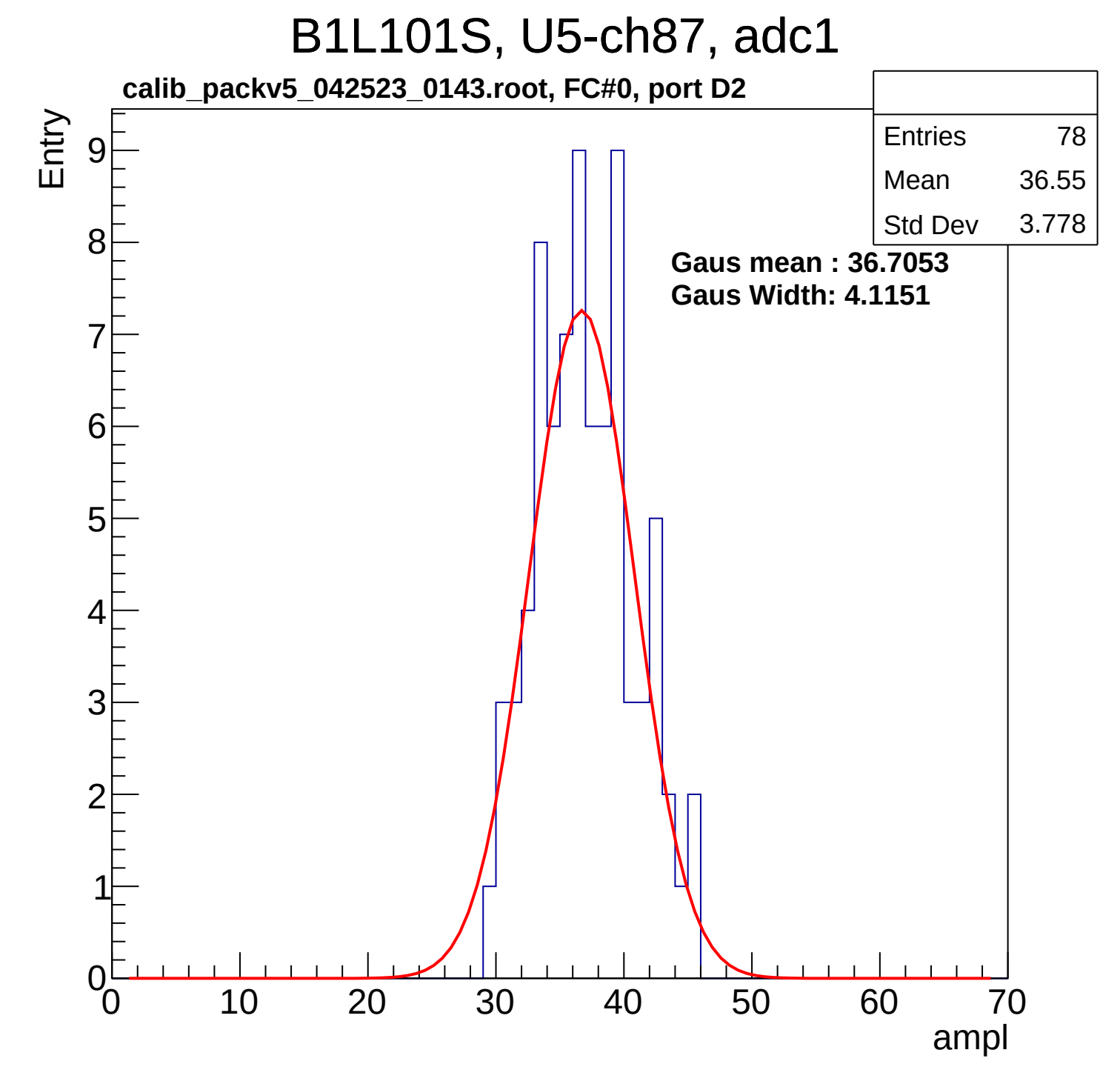
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch87, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 27.3
Std Dev 7.3
Gaus mean : 28.9235
Gaus Width: 3.9579
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch87, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 36.55
Std Dev 3.778
Gaus mean : 36.7053
Gaus Width: 4.1151
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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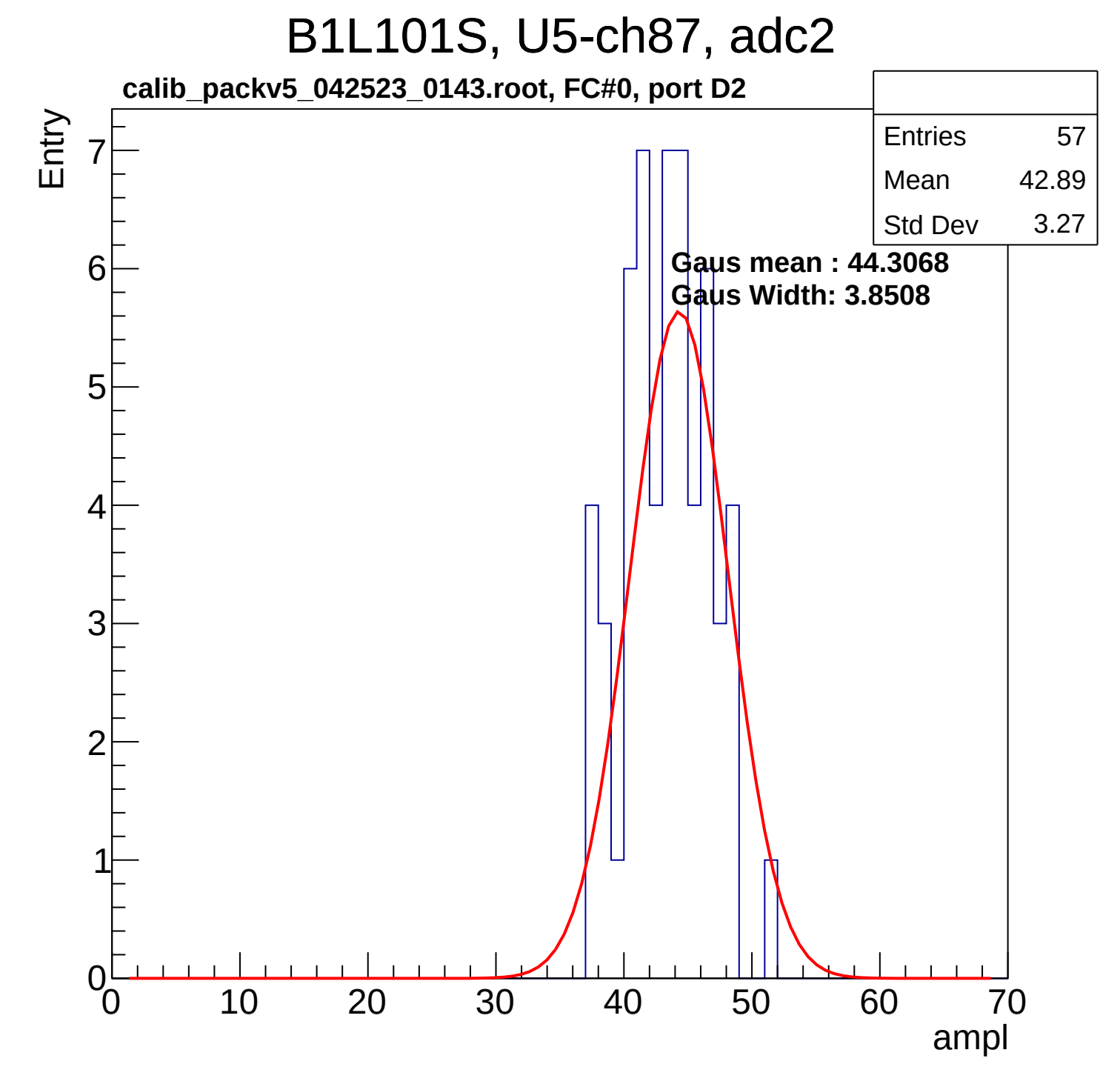
B1L101S, U5-ch87, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 42.89
Std Dev 3.27
Gaus mean : 44.3068
Gaus Width: 3.8508
Entry
ampl
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1
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3
4
5
6
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0
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60
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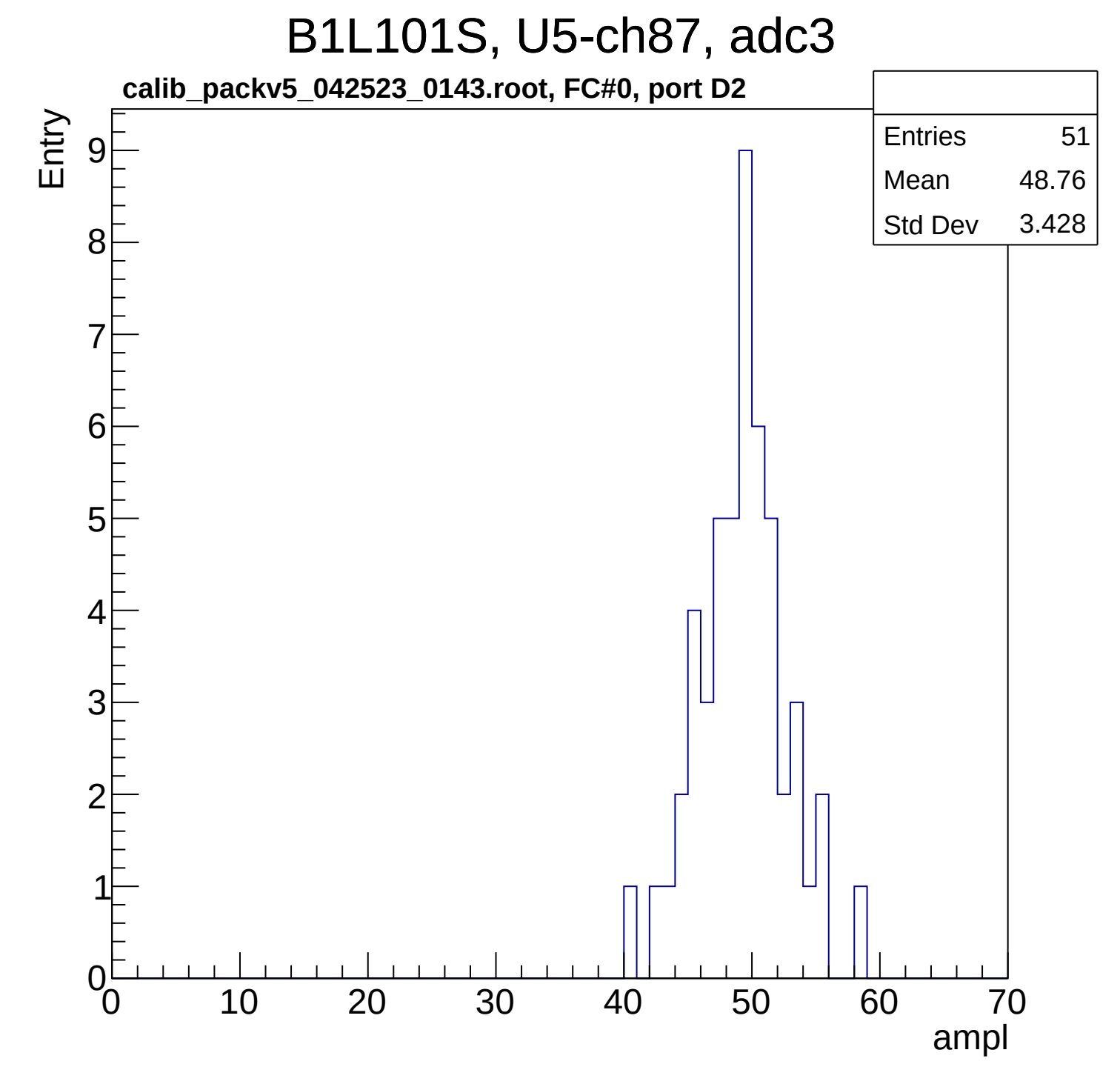
B1L101S, U5-ch87, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 48.76
Std Dev 3.428
Entry
ampl
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5
6
7
8
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0
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40
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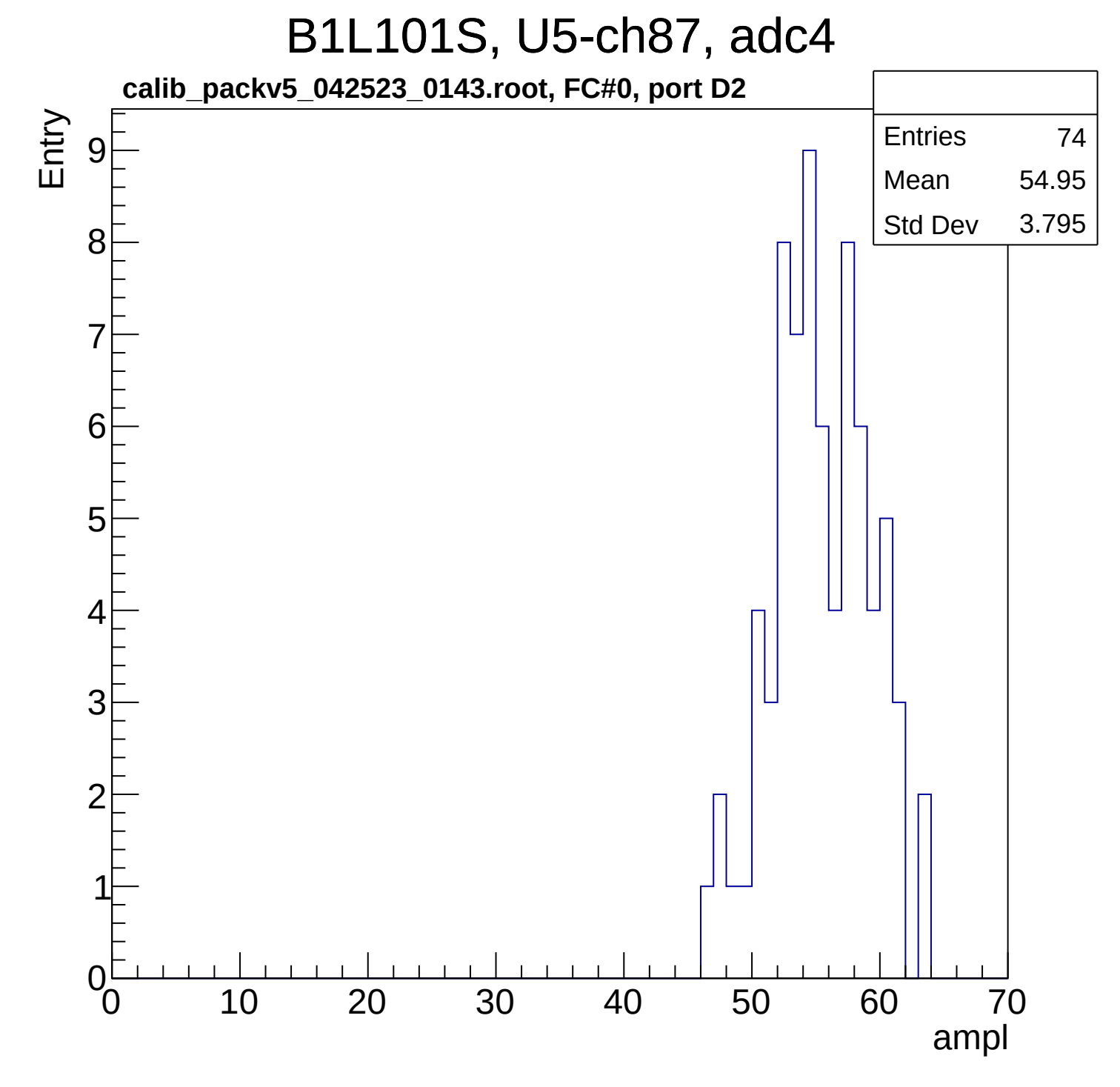
60
70


B1L101S, U5-ch87, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 54.95
Std Dev 3.795
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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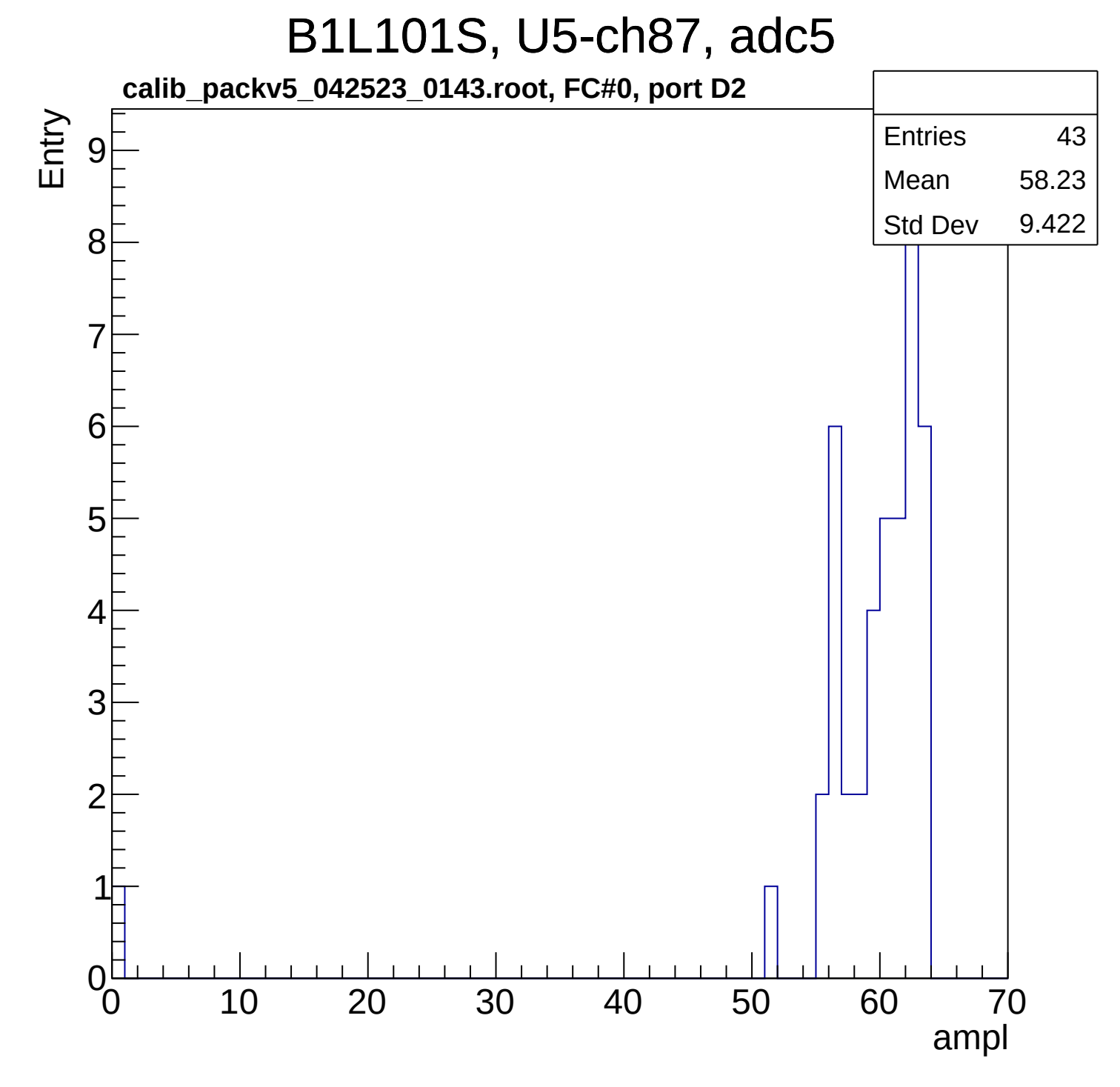
B1L101S, U5-ch87, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 43
Mean 58.23
Std Dev 9.422
Entry
ampl
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3
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5
6
7
8
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60
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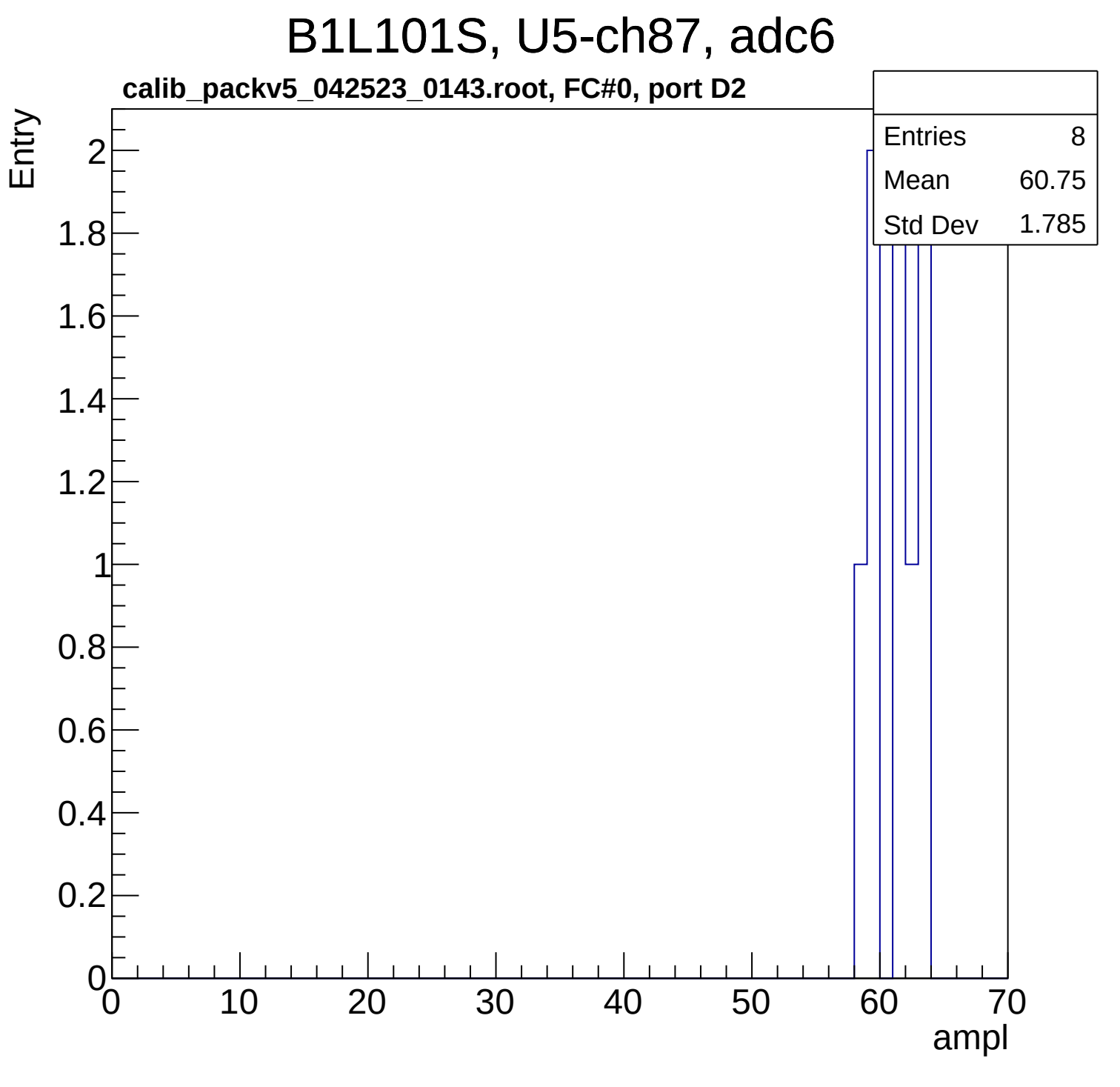
B1L101S, U5-ch87, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 60.75
Std Dev 1.785
Entry
ampl
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0.2
0.4
0.6
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1.2
1.4
1.6
1.8
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0
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40
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60
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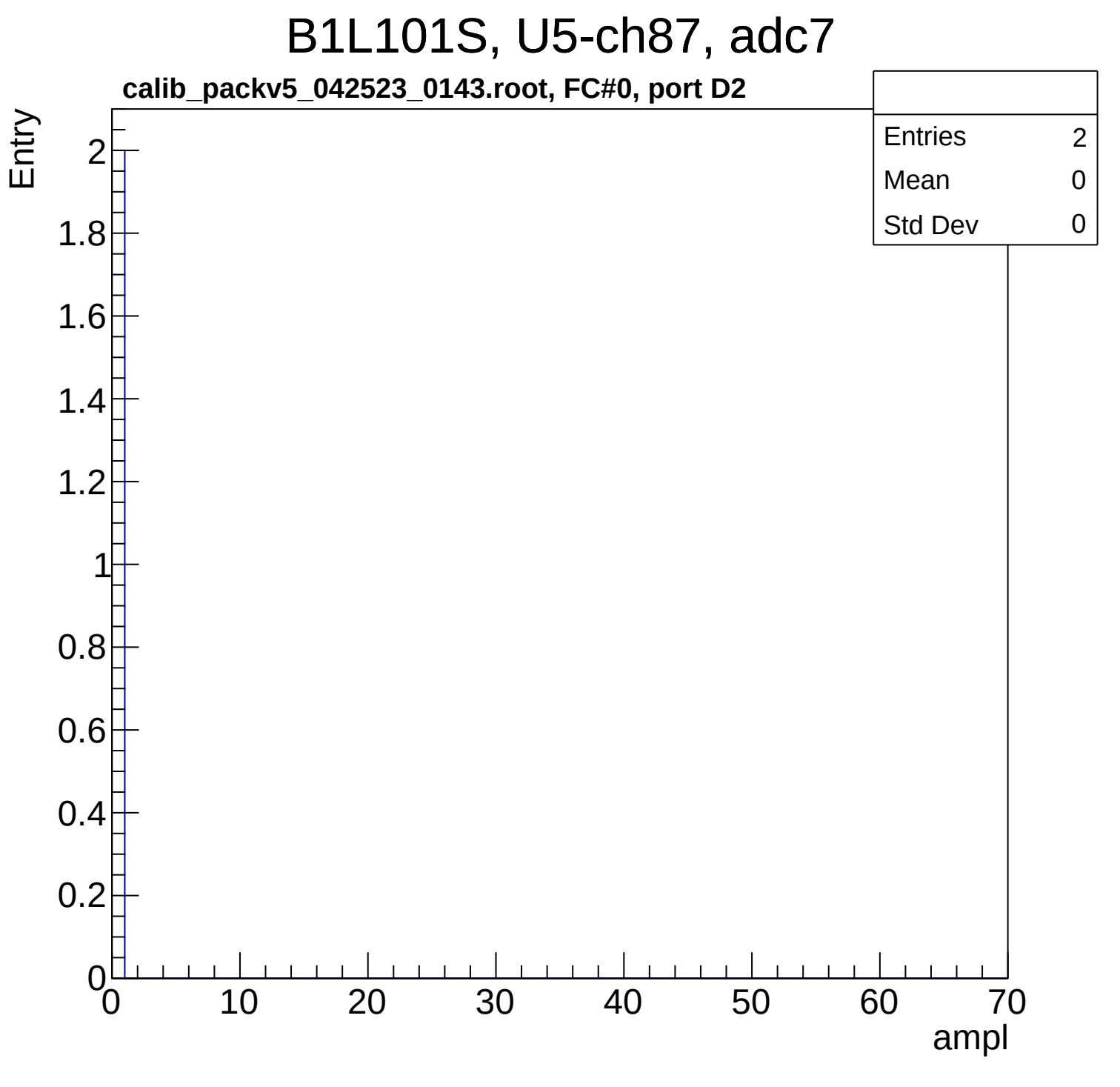
B1L101S, U5-ch87, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
0
0.2
0.4
0.6
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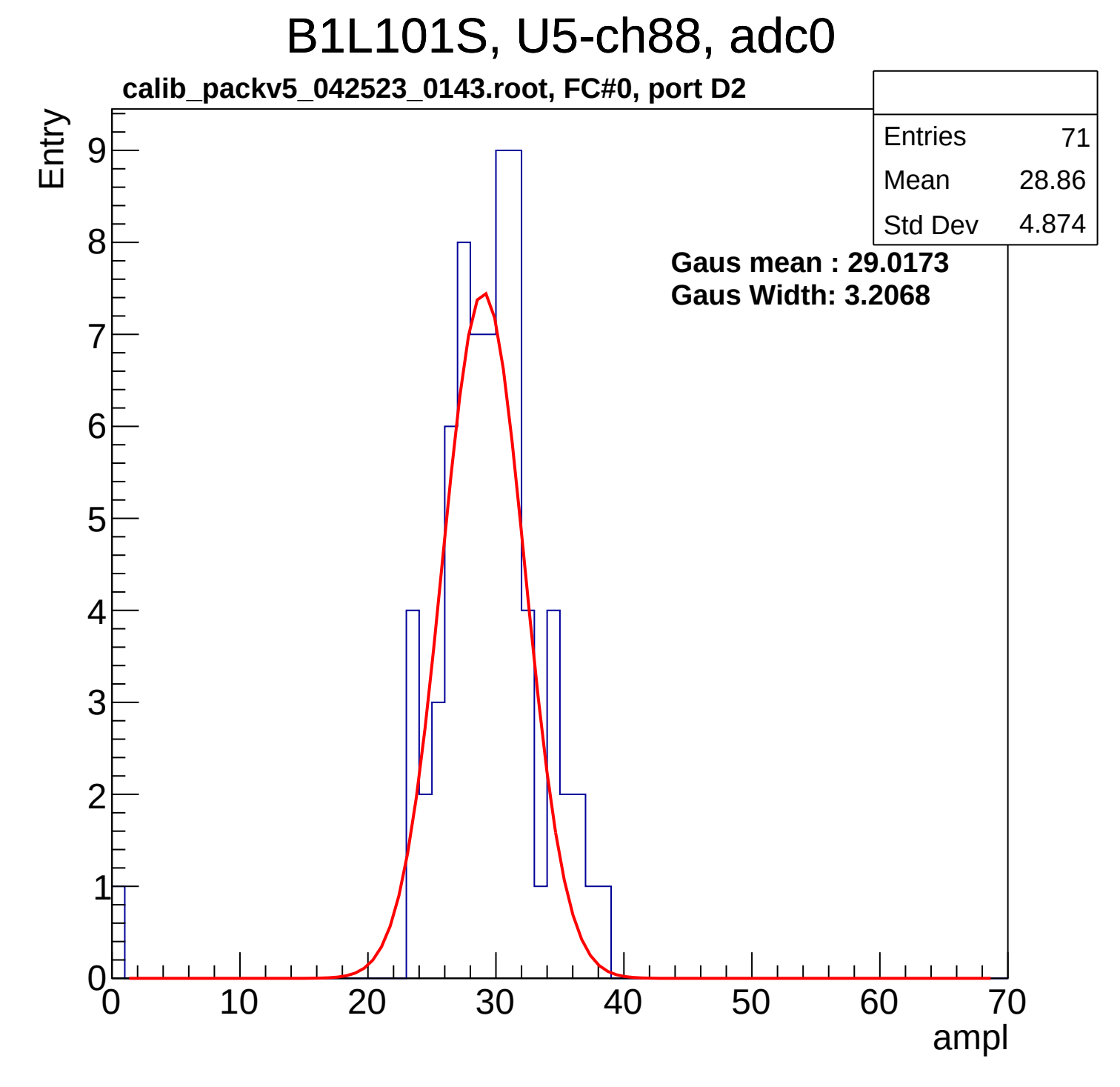
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch88, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 28.86
Std Dev 4.874
Gaus mean : 29.0173
Gaus Width: 3.2068
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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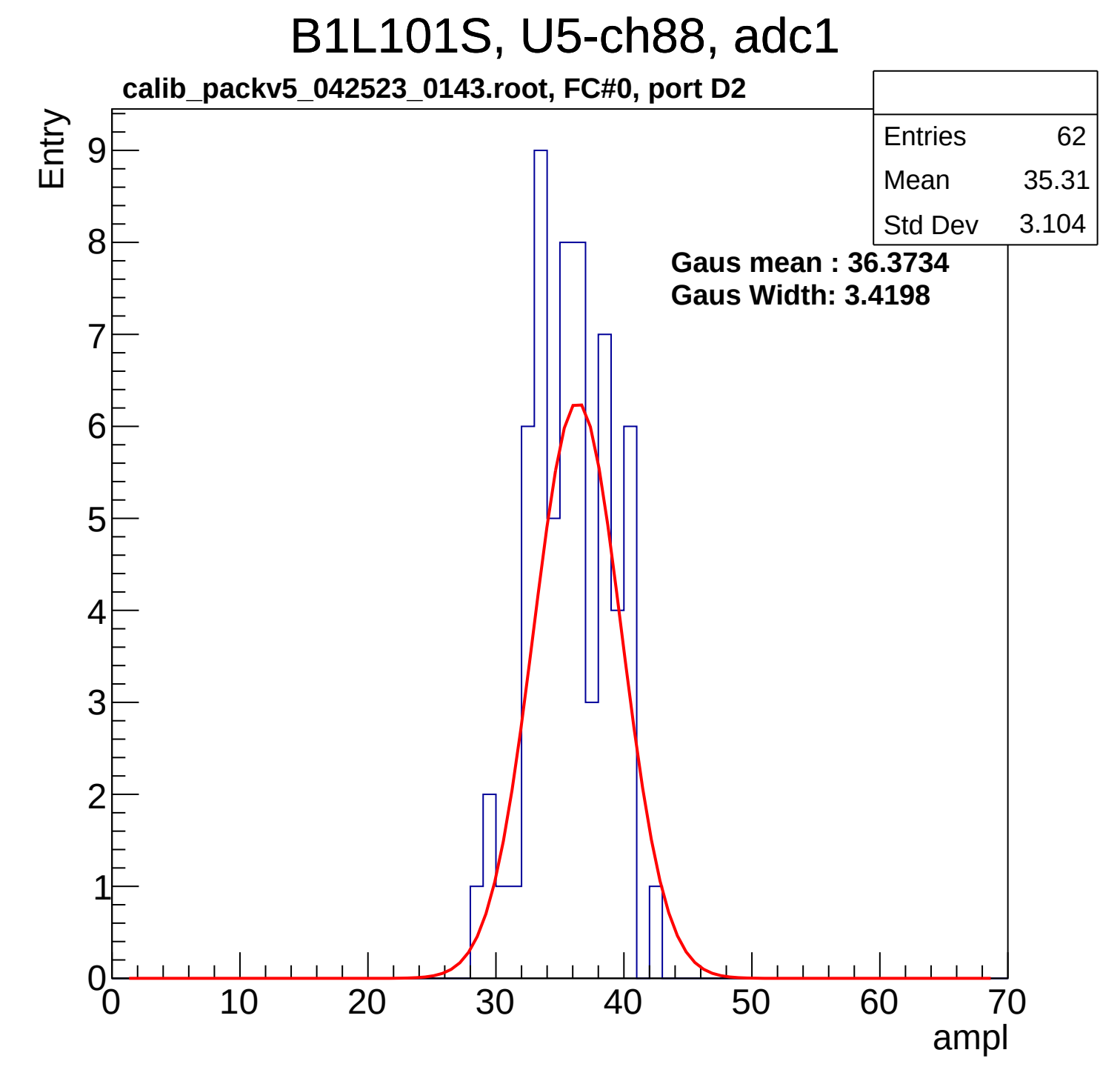
B1L101S, U5-ch88, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 35.31
Std Dev 3.104
Gaus mean : 36.3734
Gaus Width: 3.4198
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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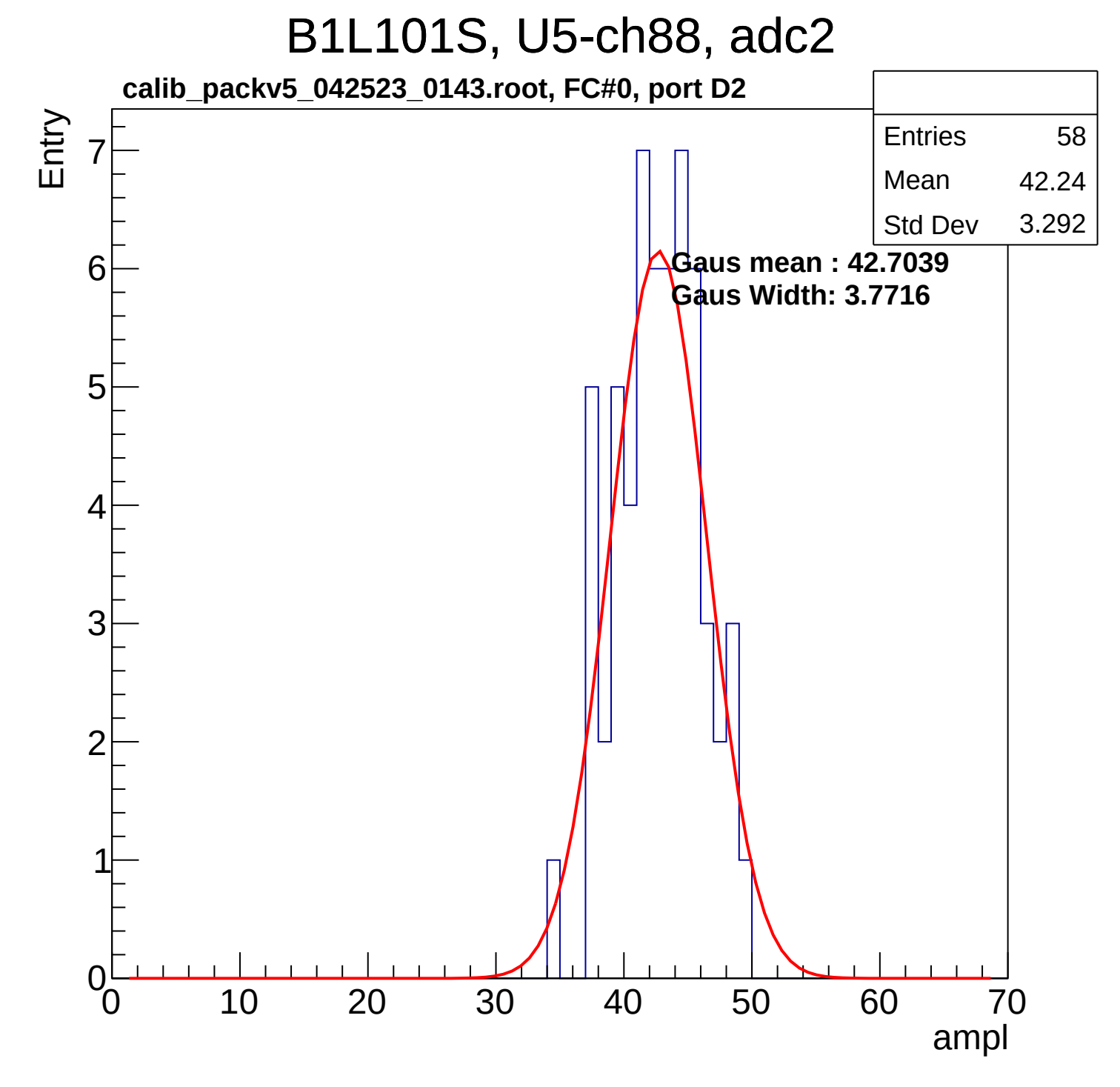
B1L101S, U5-ch88, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 42.24
Std Dev 3.292
Gaus mean : 42.7039
Gaus Width: 3.7716
Entry
ampl
0
1
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3
4
5
6
7
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40
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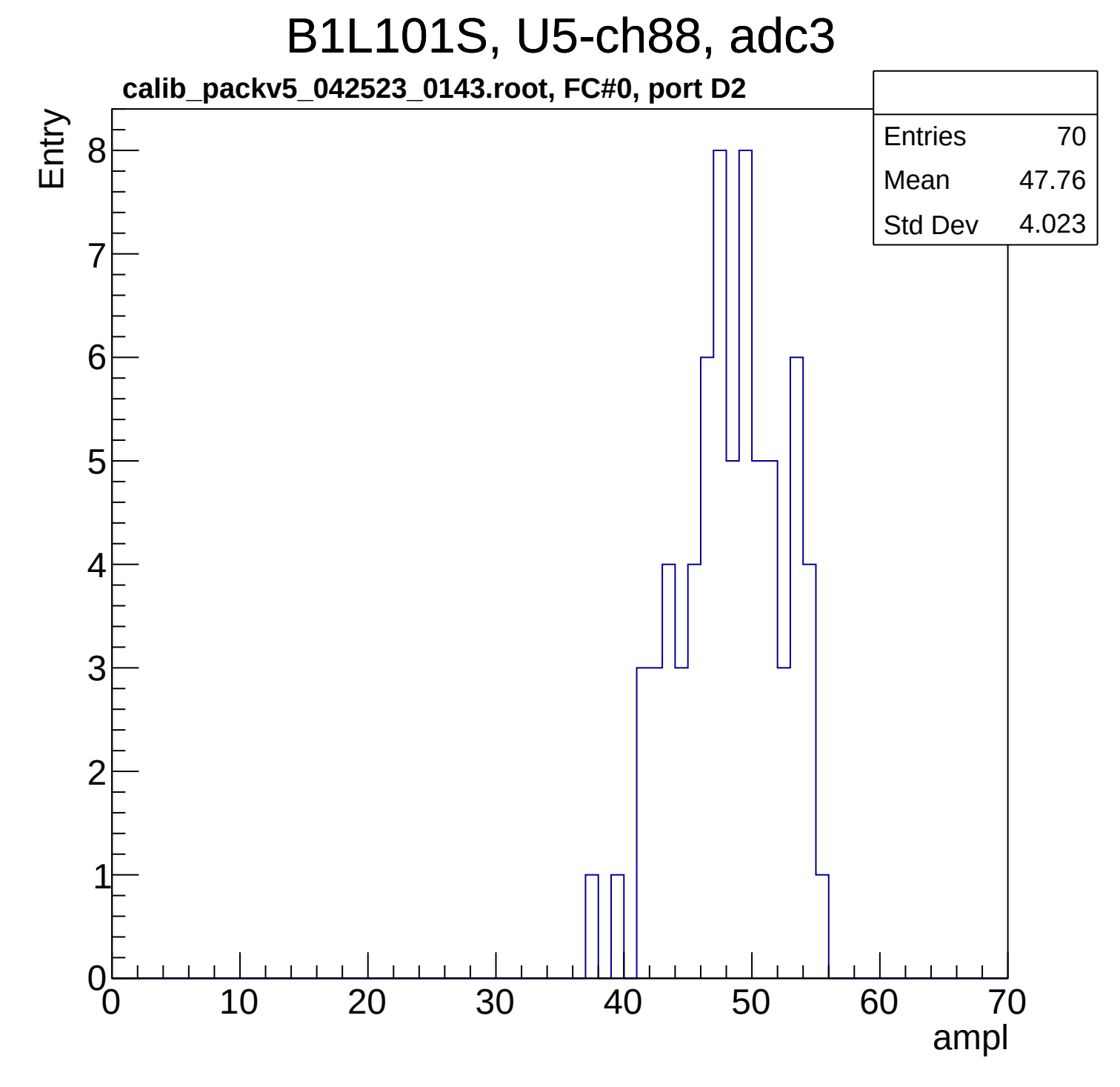
B1L101S, U5-ch88, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 47.76
Std Dev 4.023
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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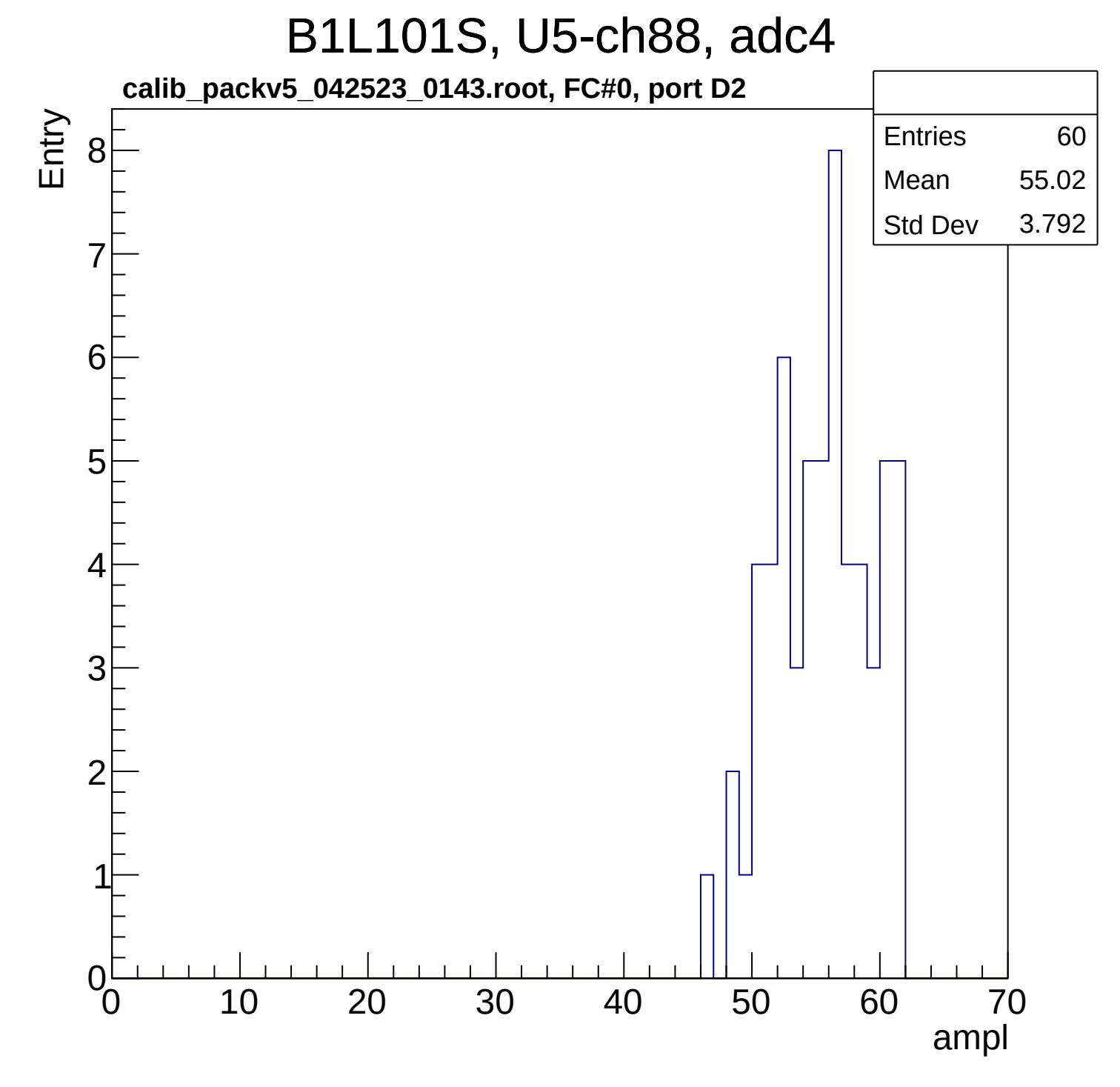
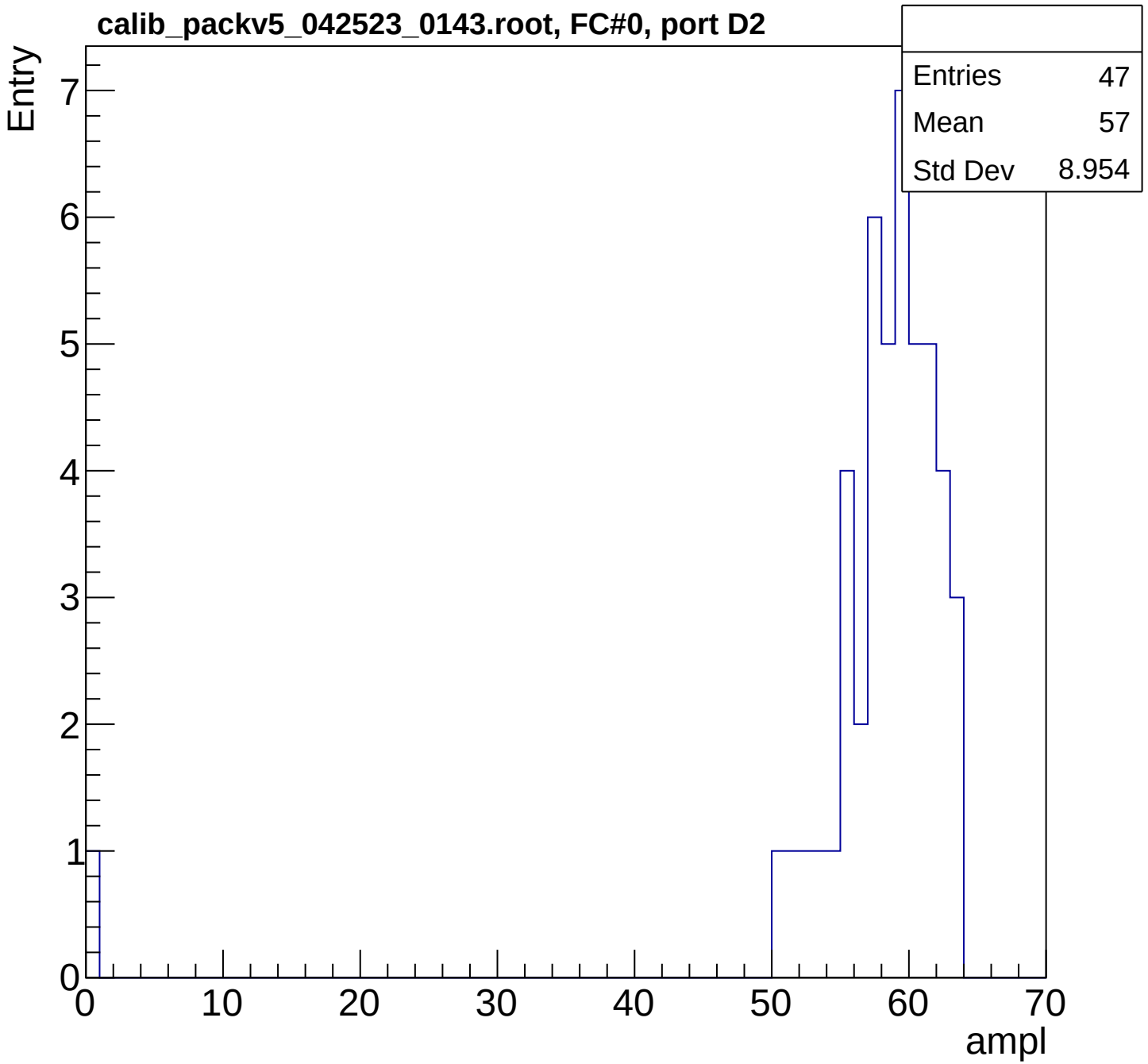
40
50
60
70


B1L101S, U5-ch88, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 55.02
Std Dev 3.792
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch88, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 57
Std Dev 8.954
Entry
ampl
0
1
2
3
4
5
6
7
0
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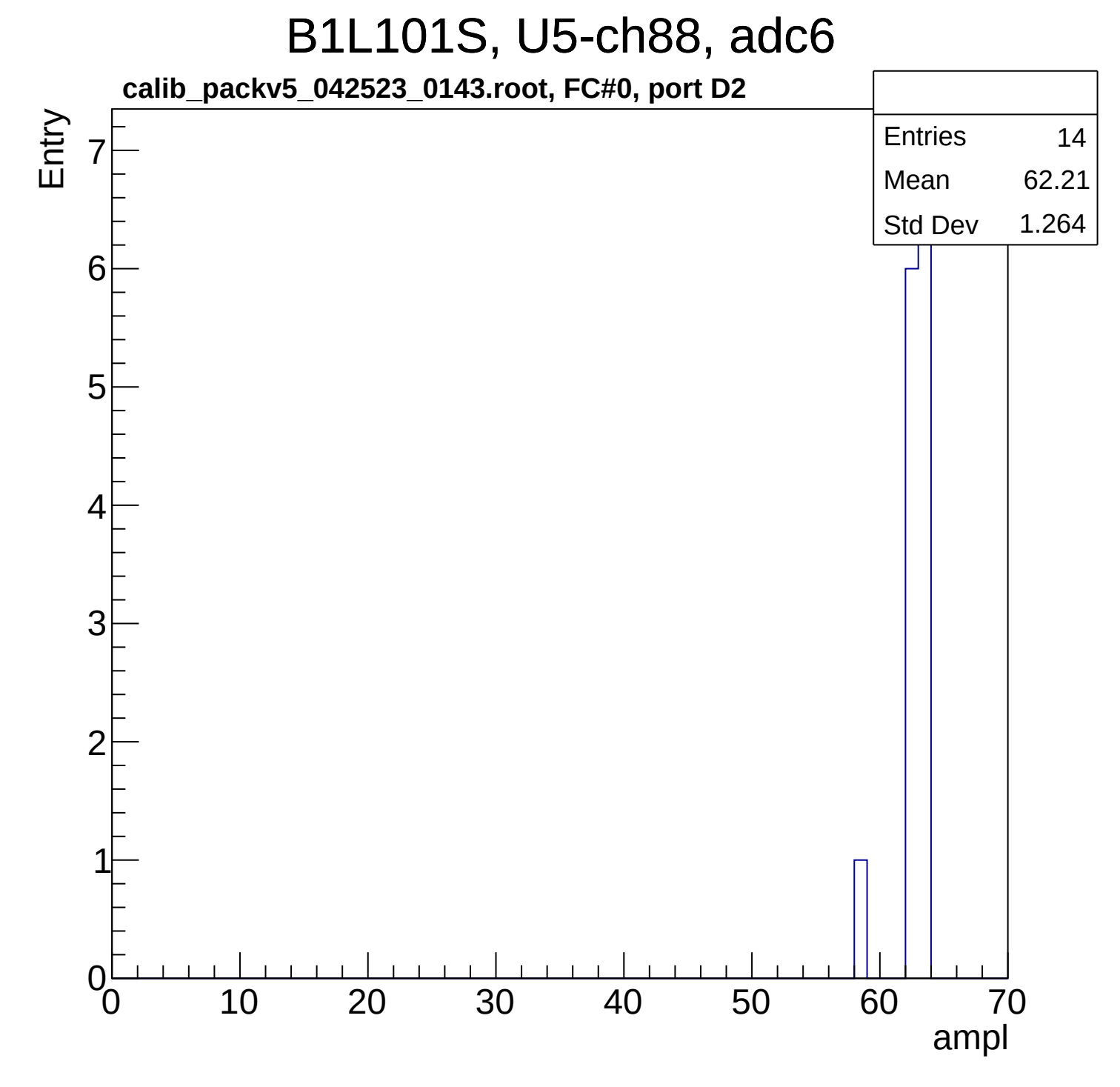
20
30
40
50
60
70


B1L101S, U5-ch88, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 14
Mean 62.21
Std Dev 1.264
Entry
ampl
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1
2
3
4
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0
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60
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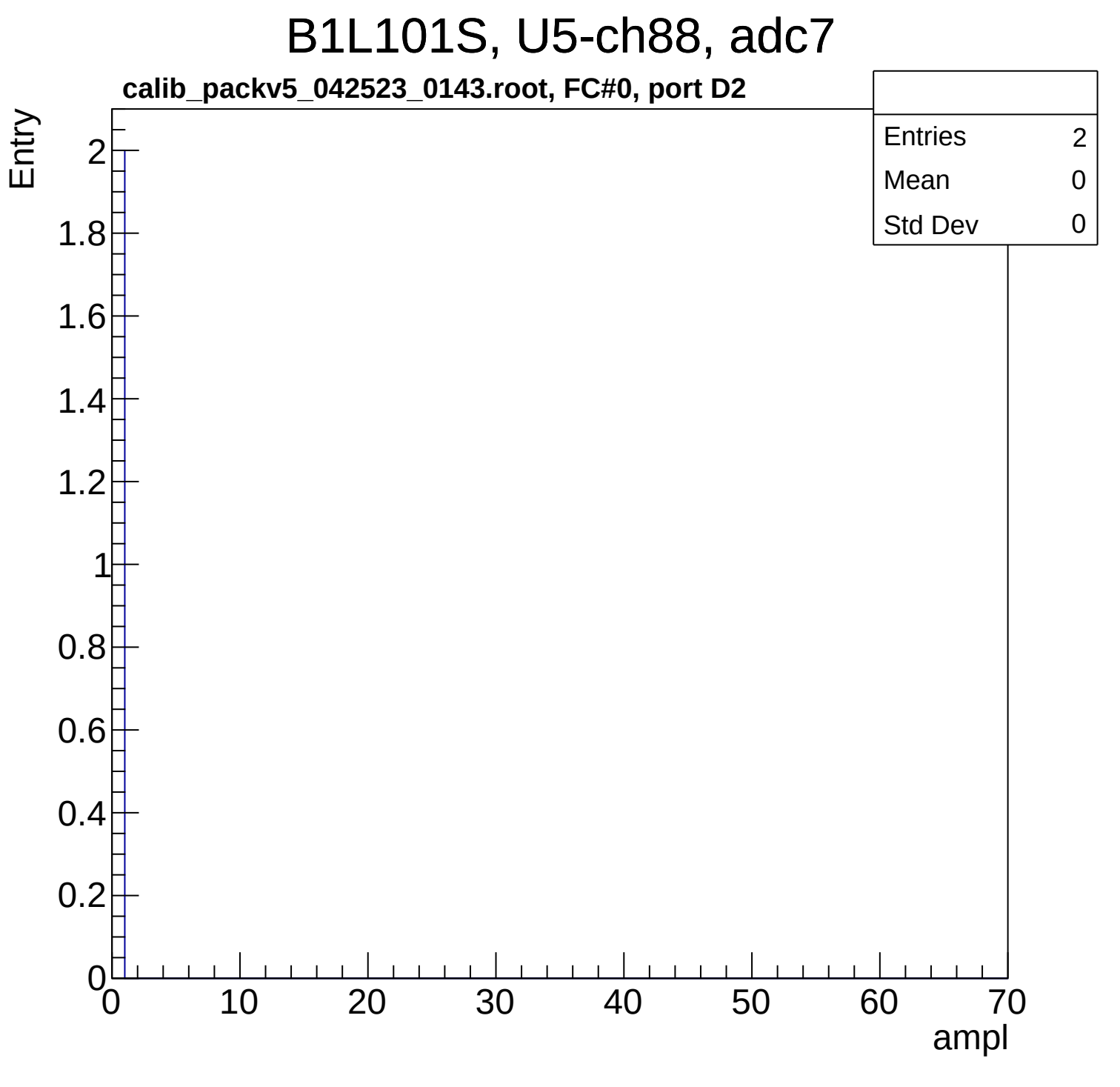
B1L101S, U5-ch88, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
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1.2
1.4
1.6
1.8
2
0
10
20
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40
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60
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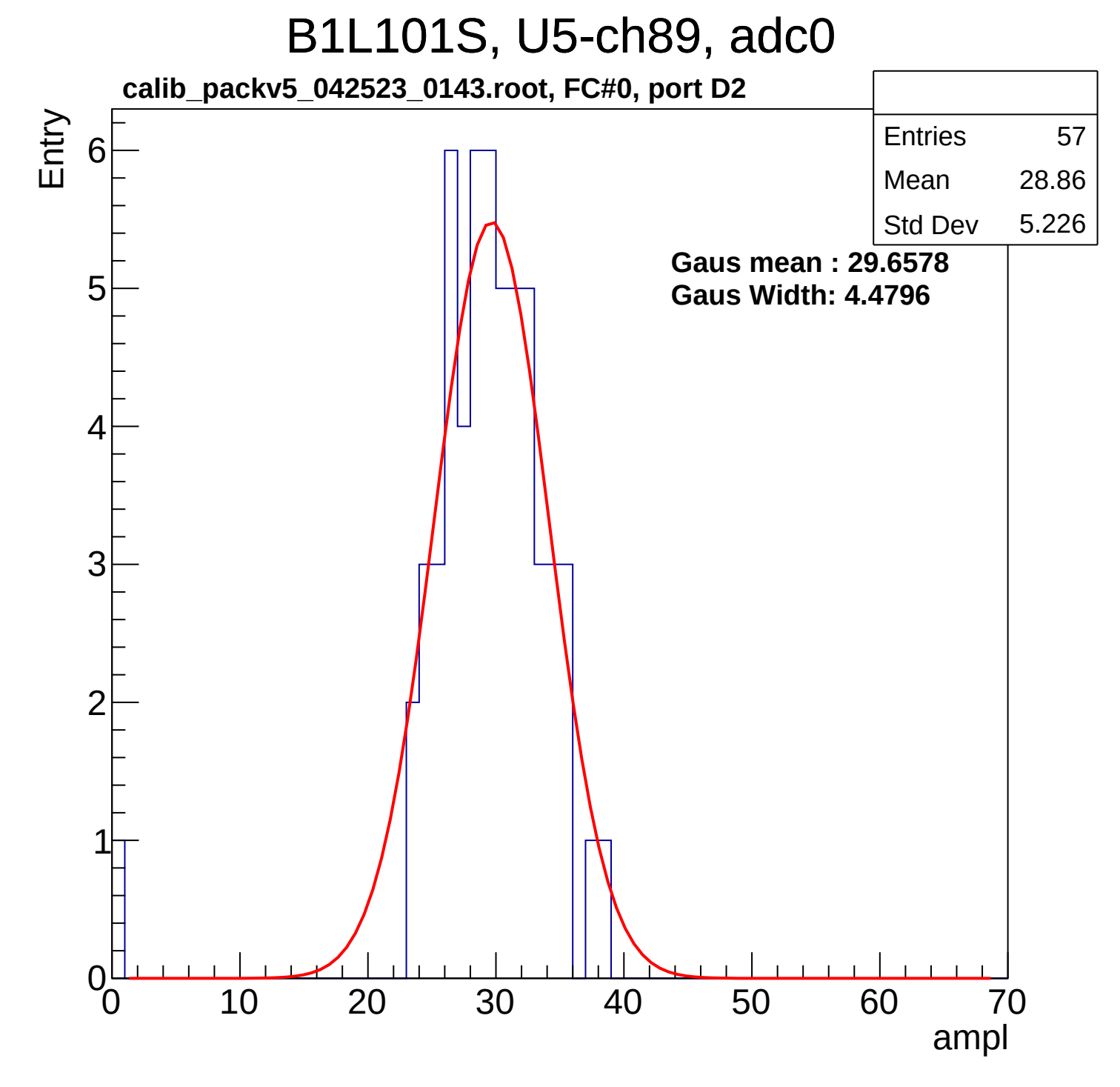
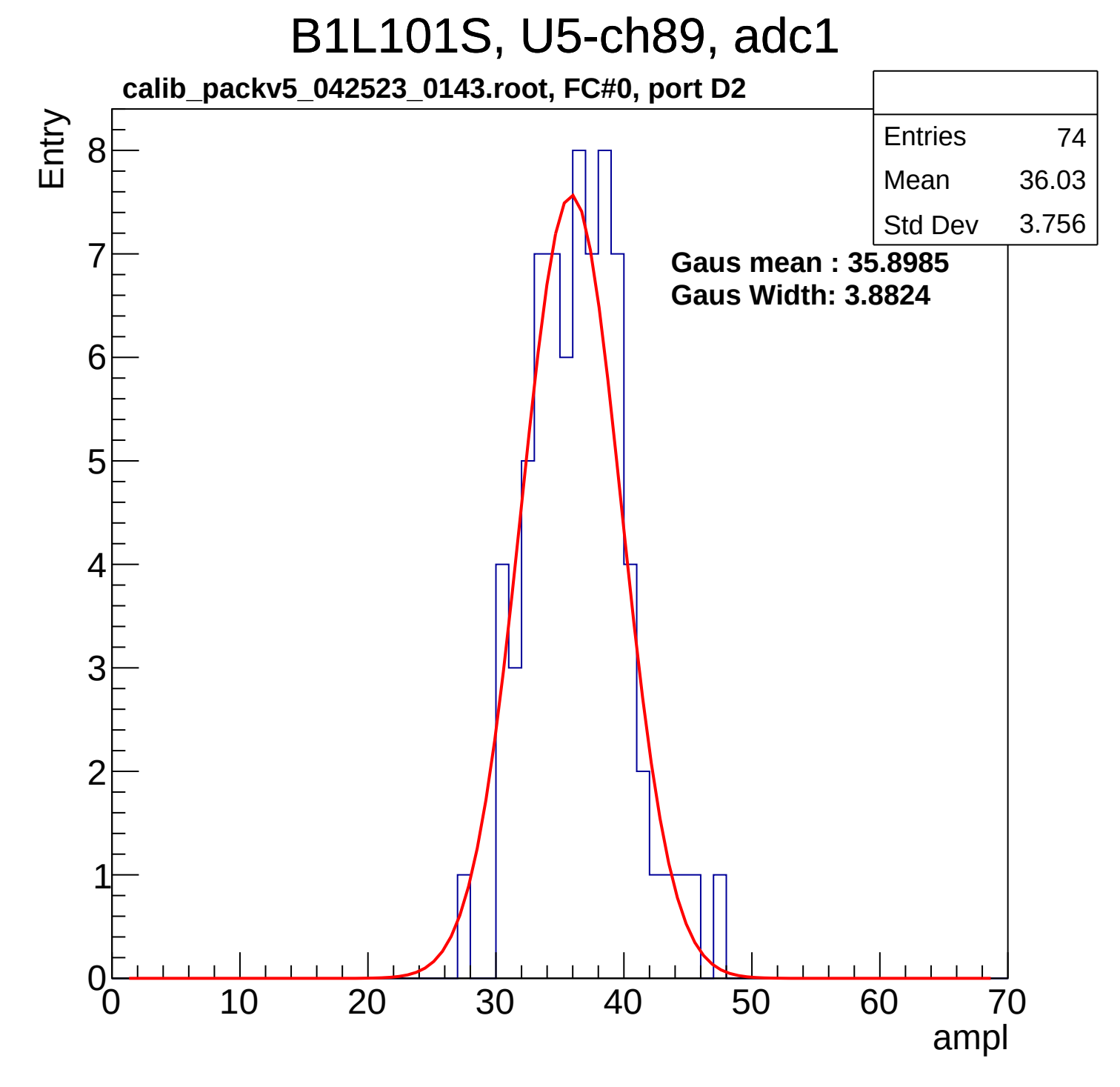

B1L101S, U5-ch89, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 28.86
Std Dev 5.226
Gaus mean : 29.6578
Gaus Width: 4.4796
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L101S, U5-ch89, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 36.03
Std Dev 3.756
Gaus mean : 35.8985
Gaus Width: 3.8824
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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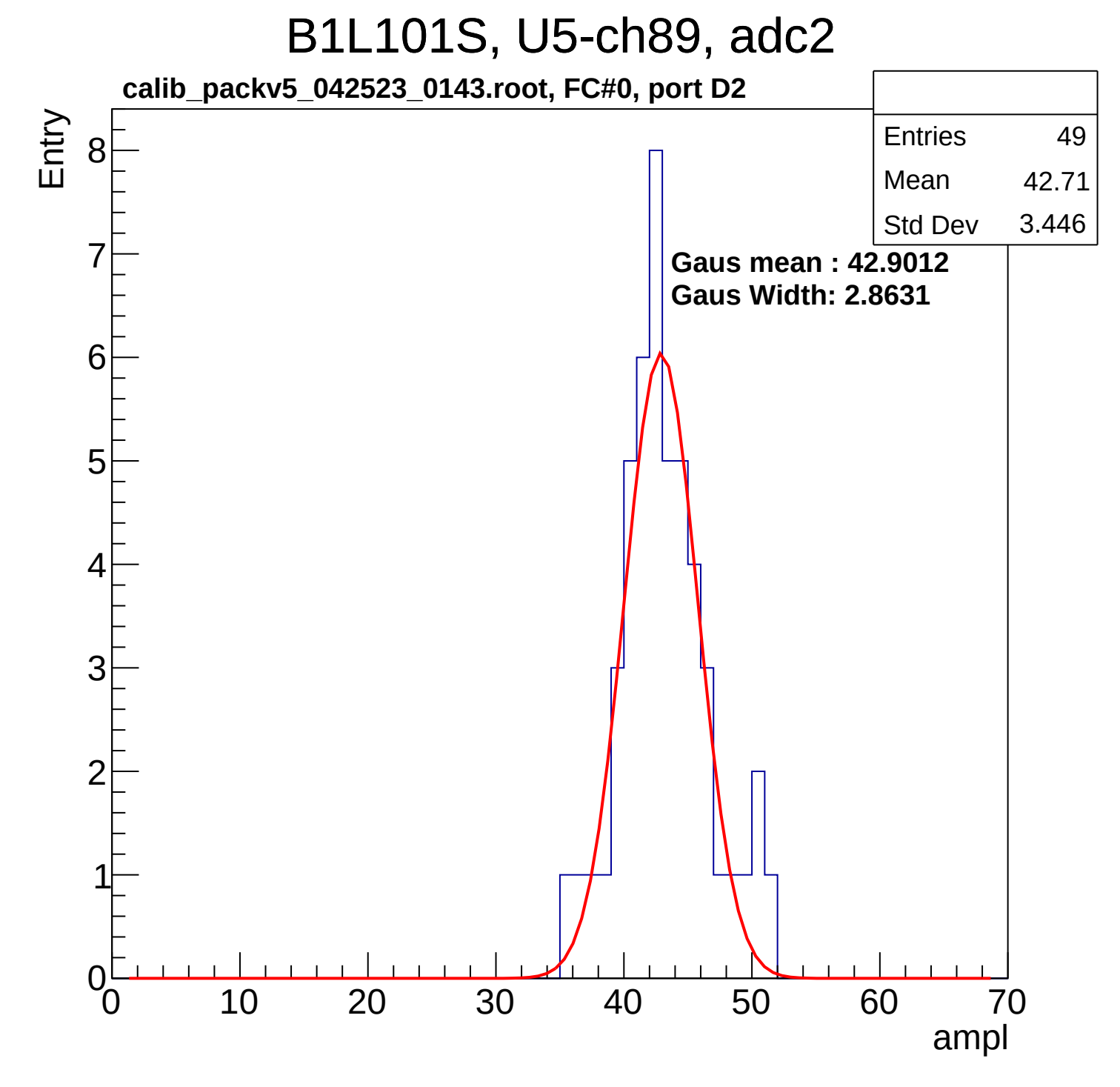
B1L101S, U5-ch89, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 42.71
Std Dev 3.446
Gaus mean : 42.9012
Gaus Width: 2.8631
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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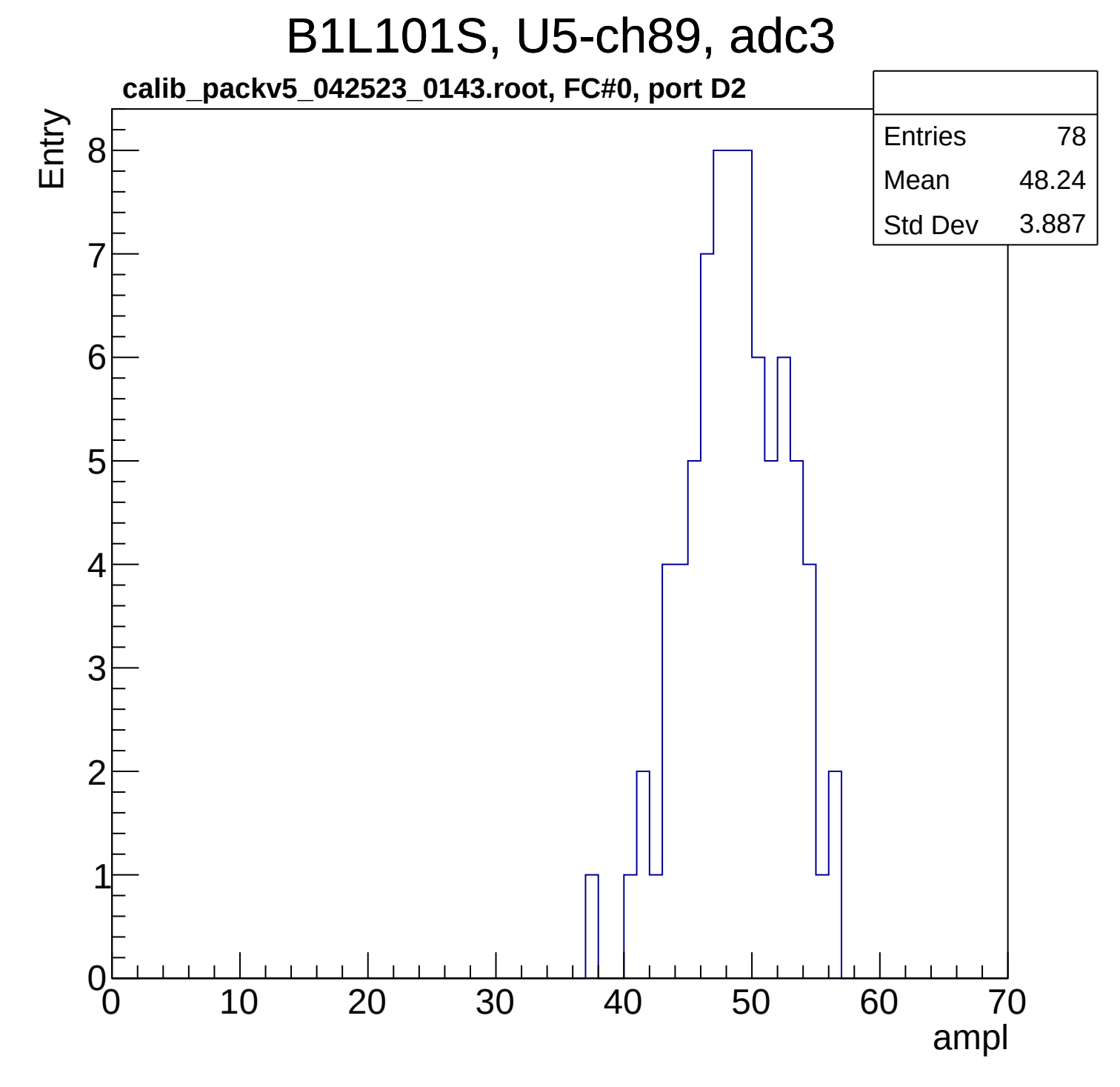
B1L101S, U5-ch89, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 48.24
Std Dev 3.887
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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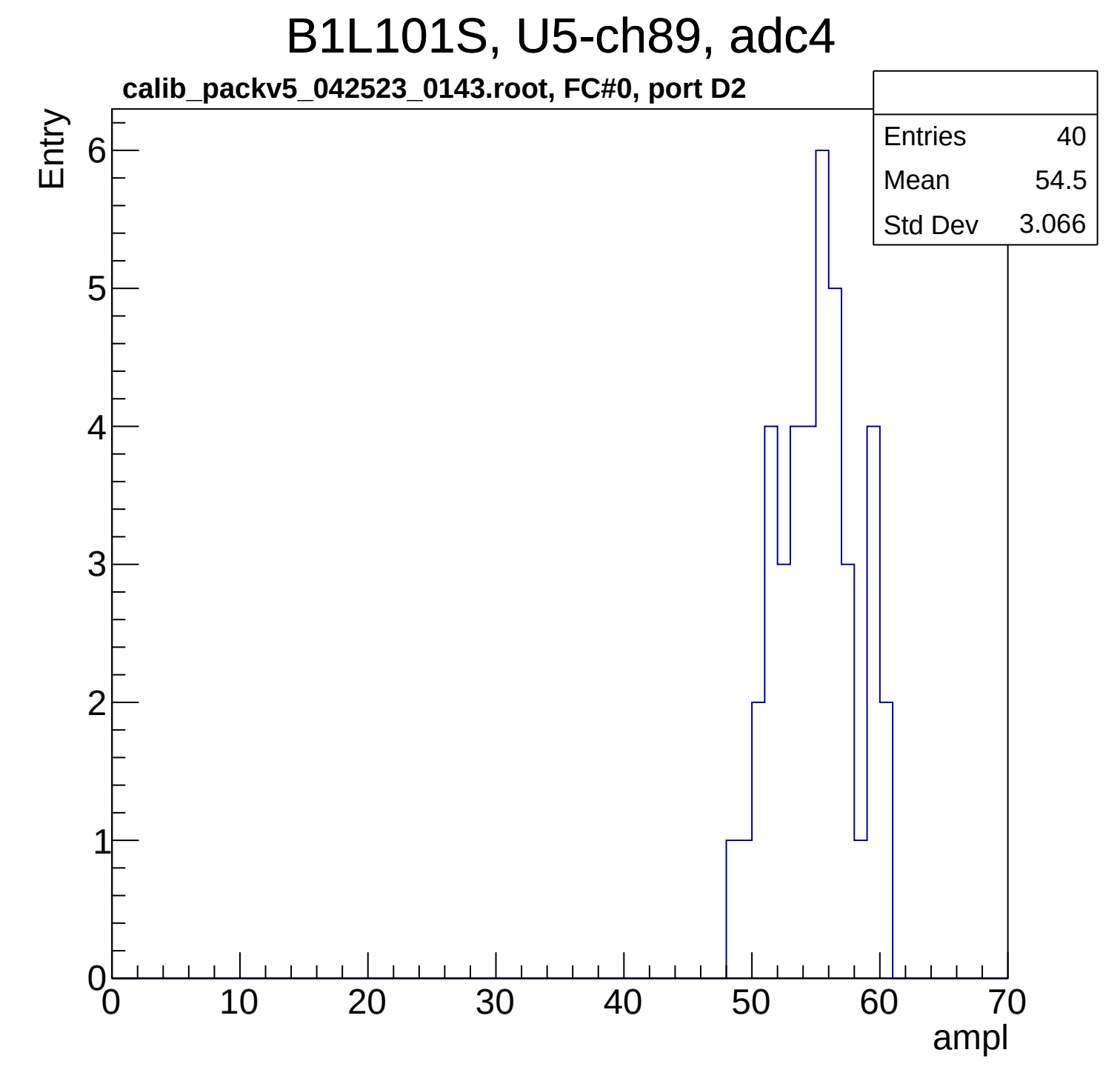
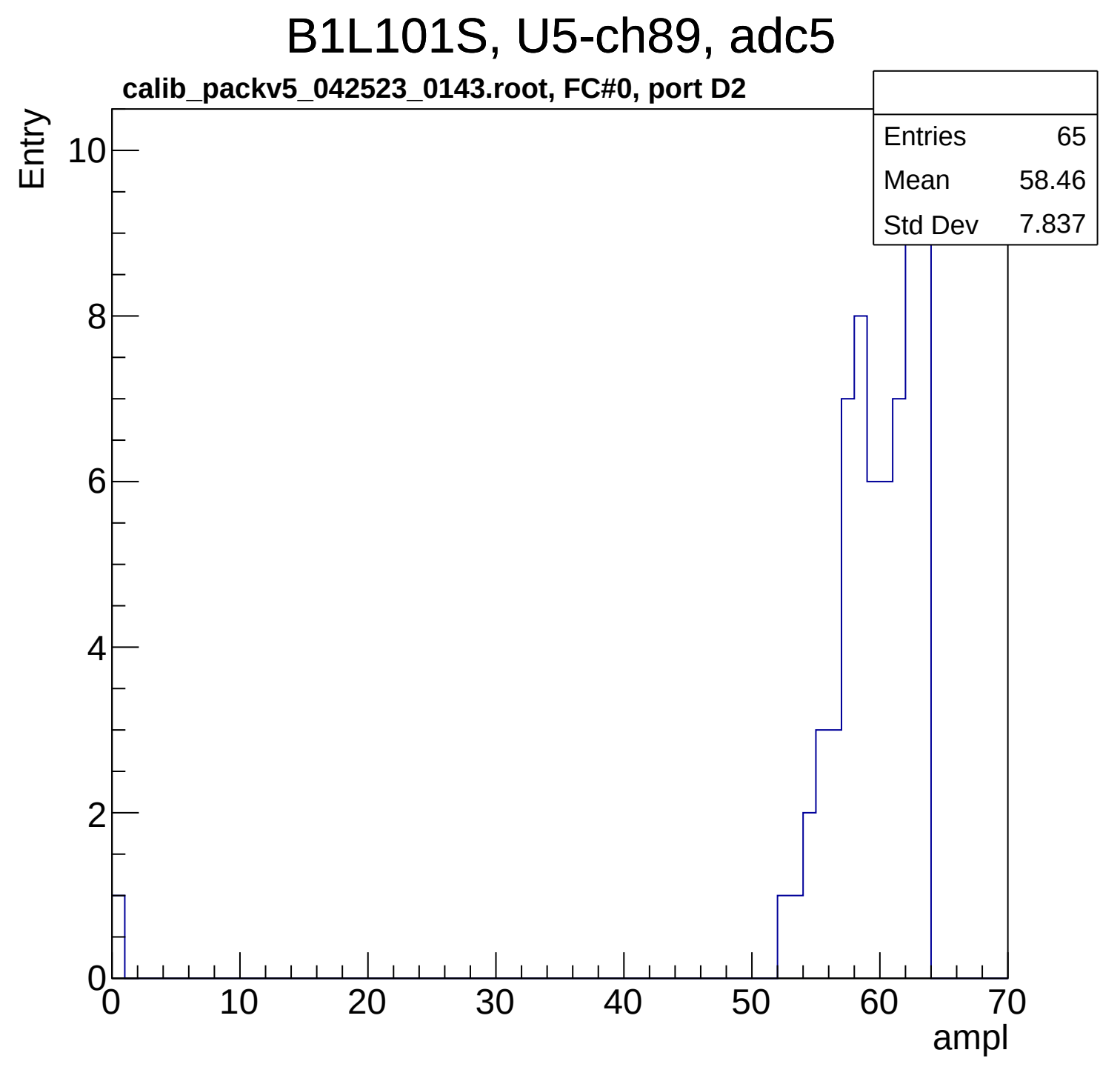
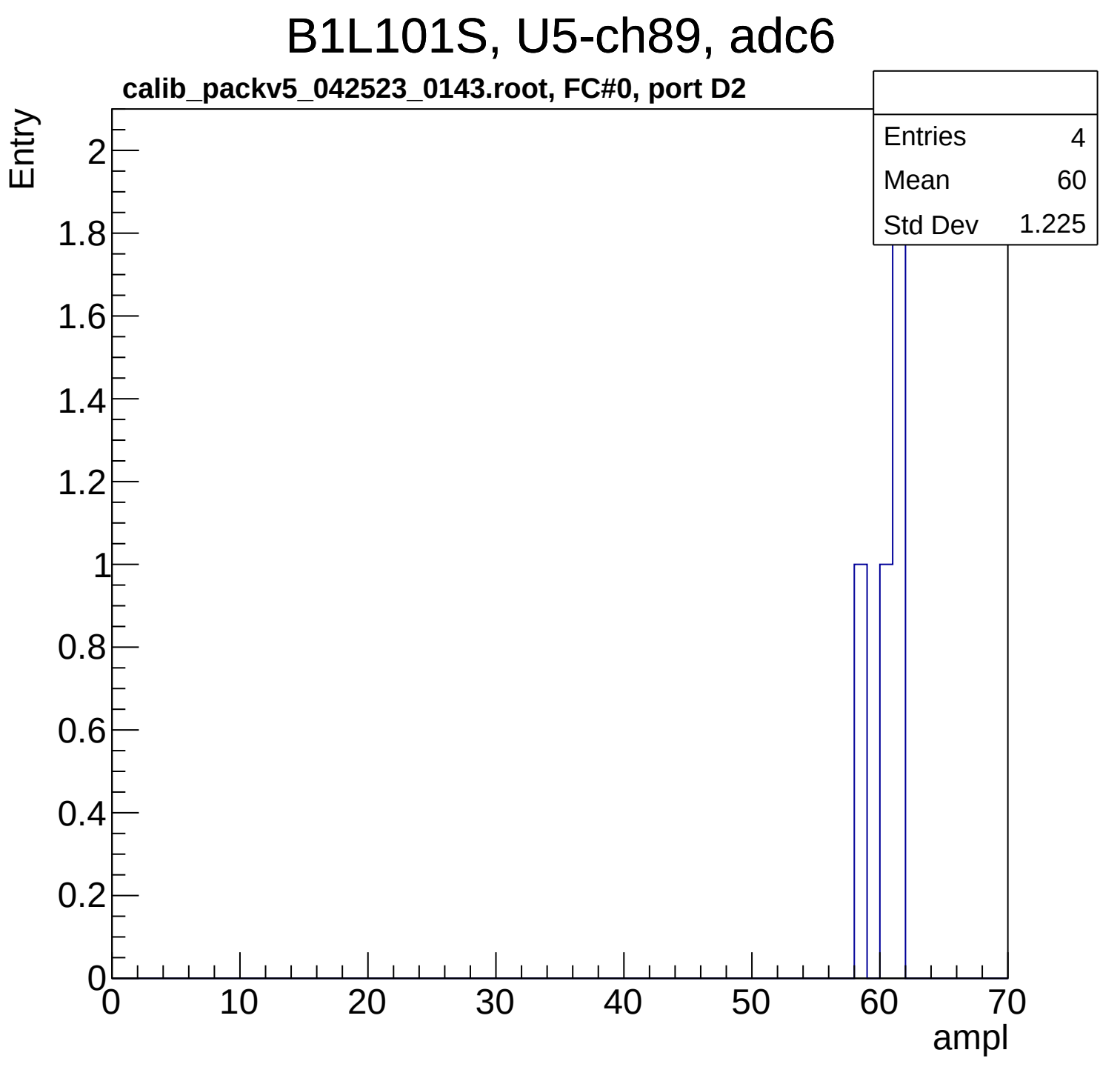
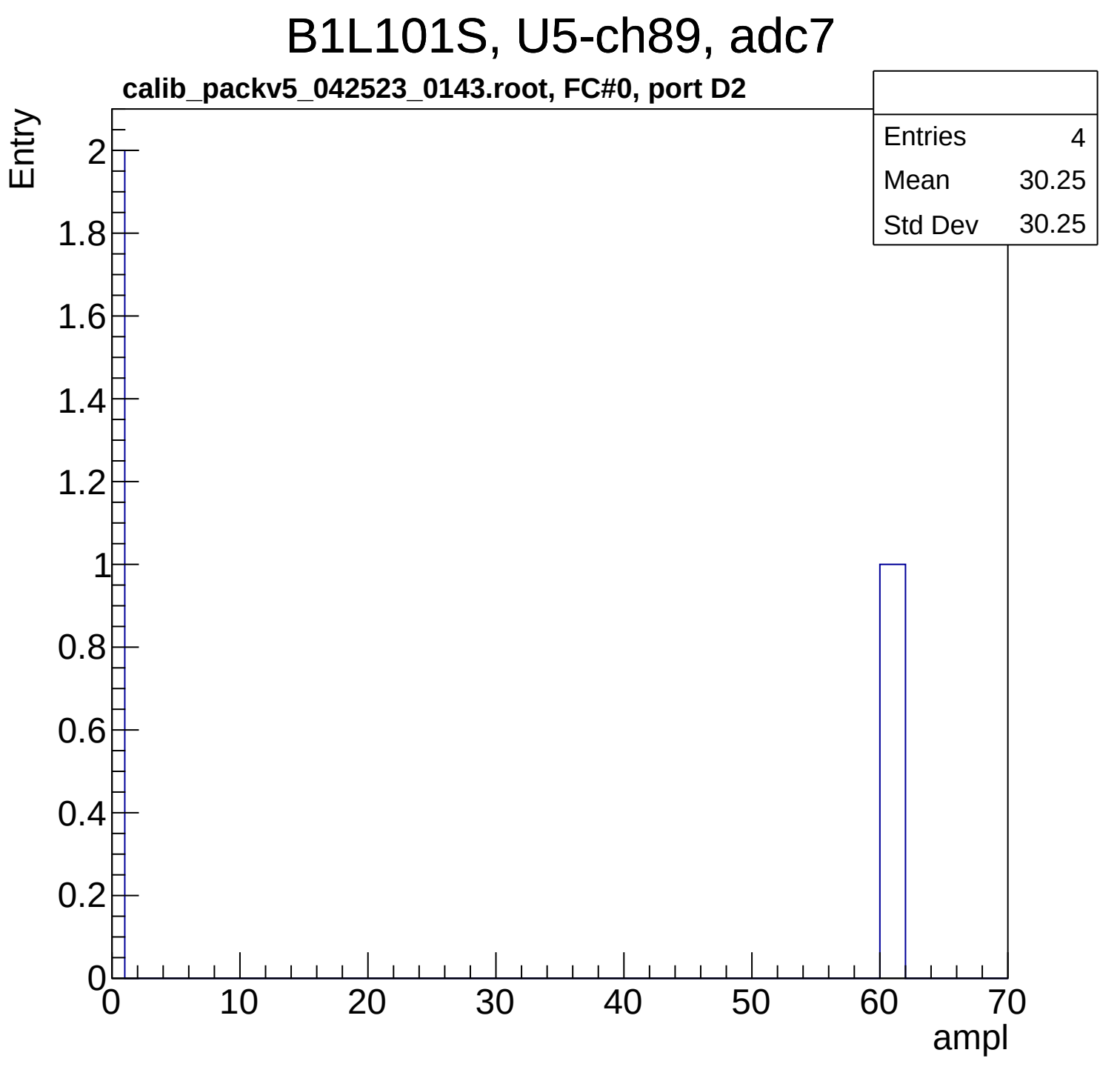

B1L101S, U5-ch89, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 40
Mean 54.5
Std Dev 3.066
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch89, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 58.46
Std Dev 7.837
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch89, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 60
Std Dev 1.225
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U5-ch89, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 30.25
Std Dev 30.25
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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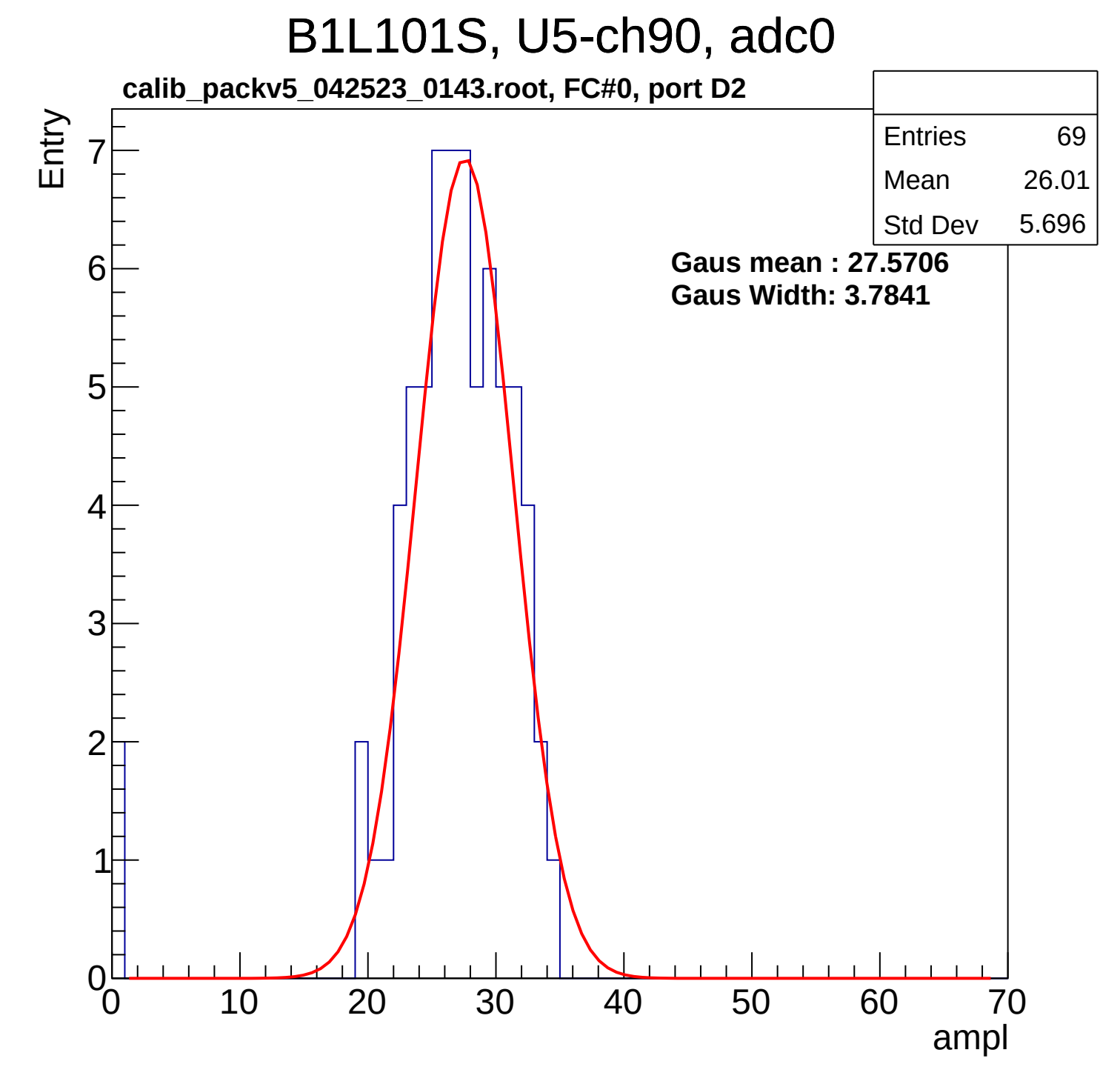
B1L101S, U5-ch90, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 26.01
Std Dev 5.696
Gaus mean : 27.5706
Gaus Width: 3.7841
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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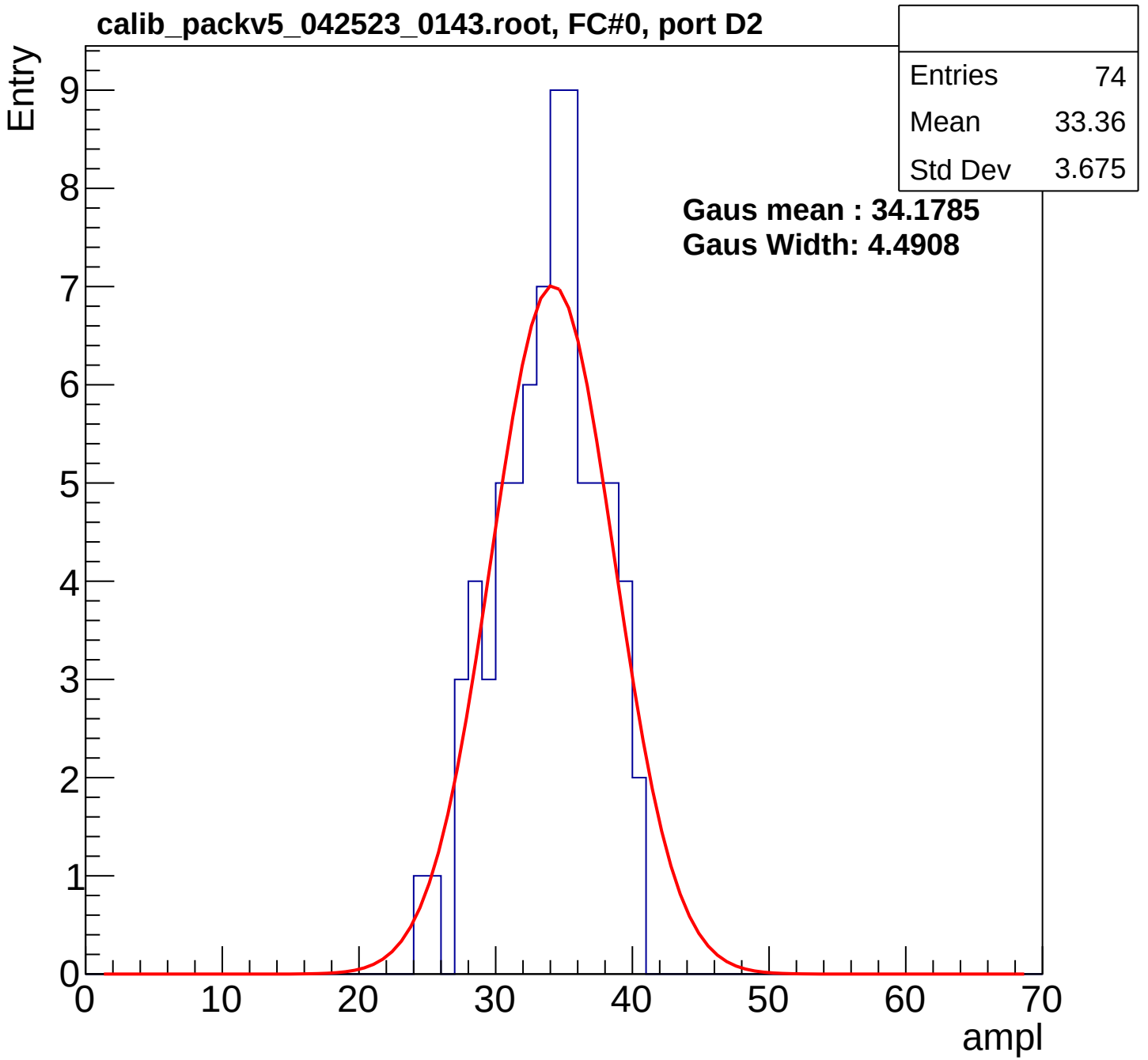
B1L101S, U5-ch90, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 33.36
Std Dev 3.675
Gaus mean : 34.1785
Gaus Width: 4.4908
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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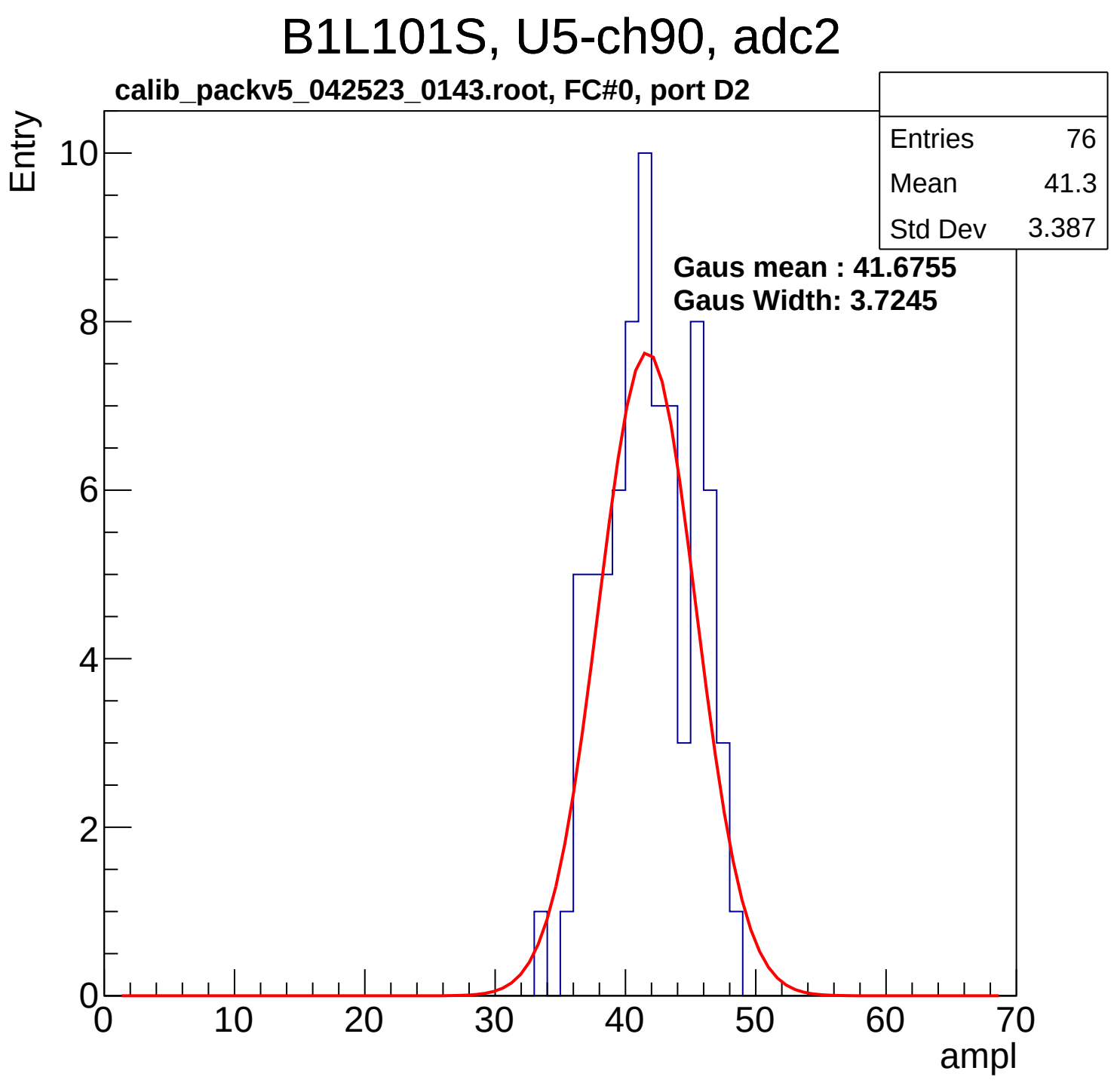
B1L101S, U5-ch90, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 41.3
Std Dev 3.387
Gaus mean : 41.6755
Gaus Width: 3.7245
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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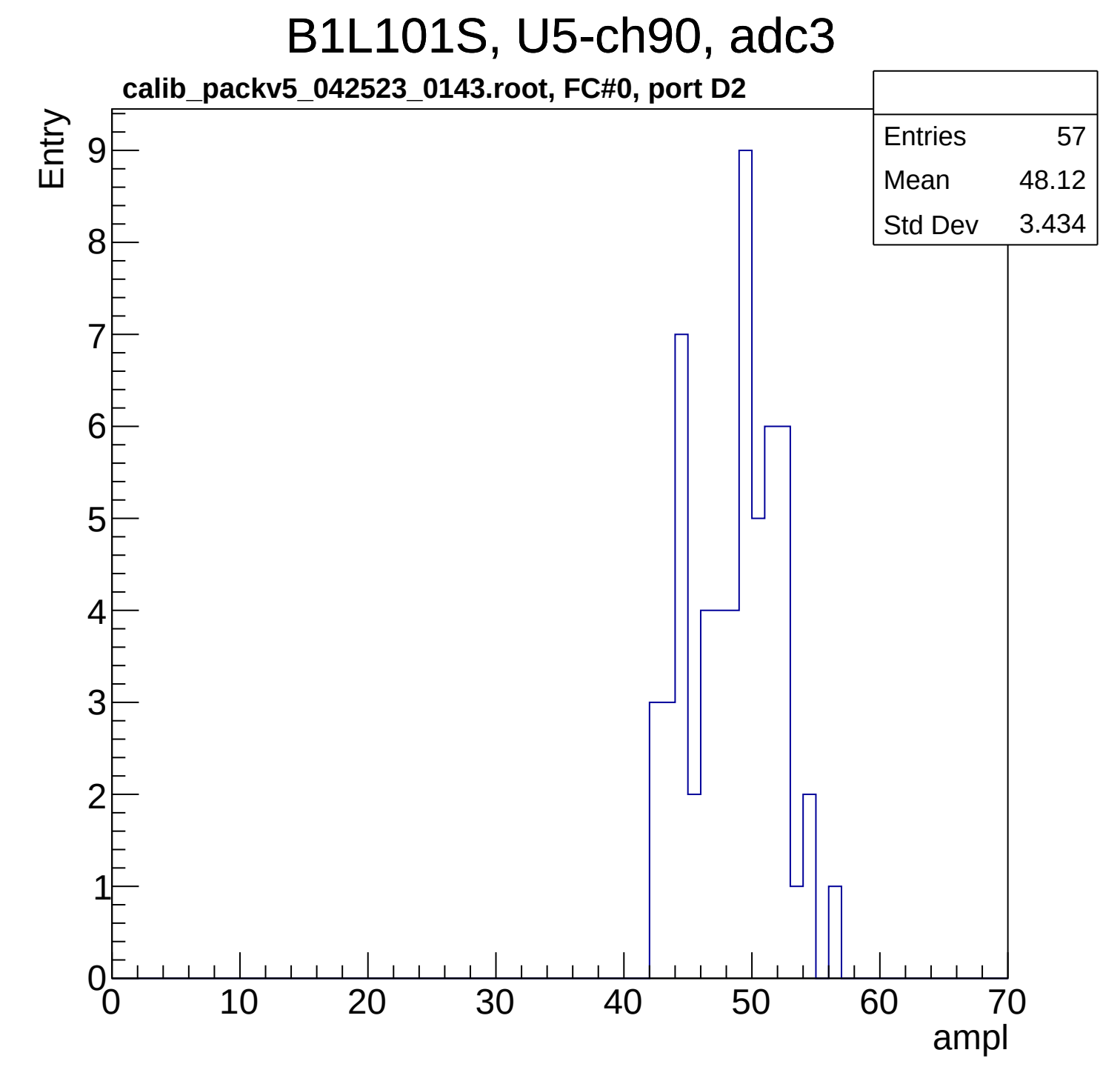
B1L101S, U5-ch90, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 48.12
Std Dev 3.434
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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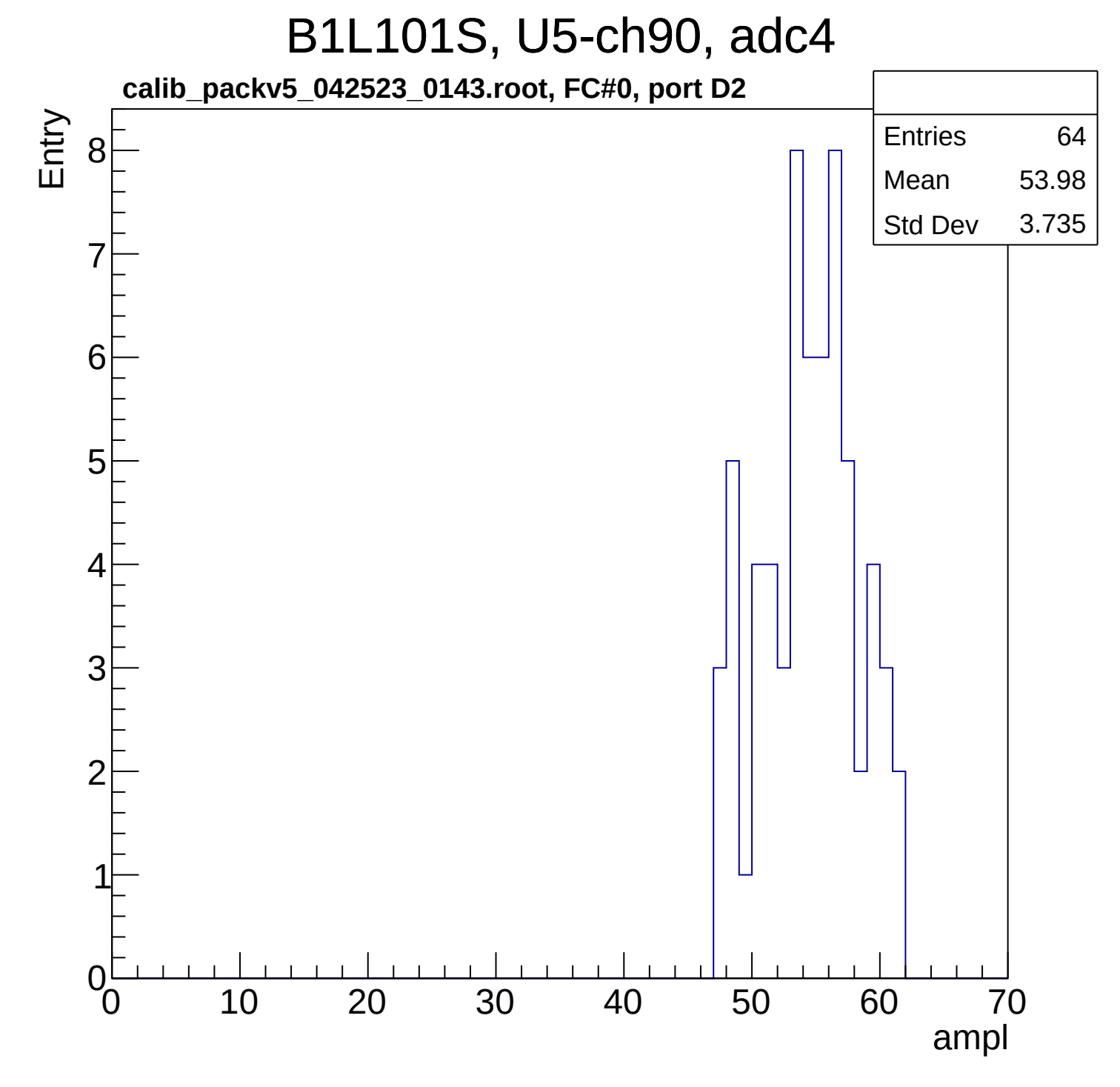
B1L101S, U5-ch90, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 53.98
Std Dev 3.735
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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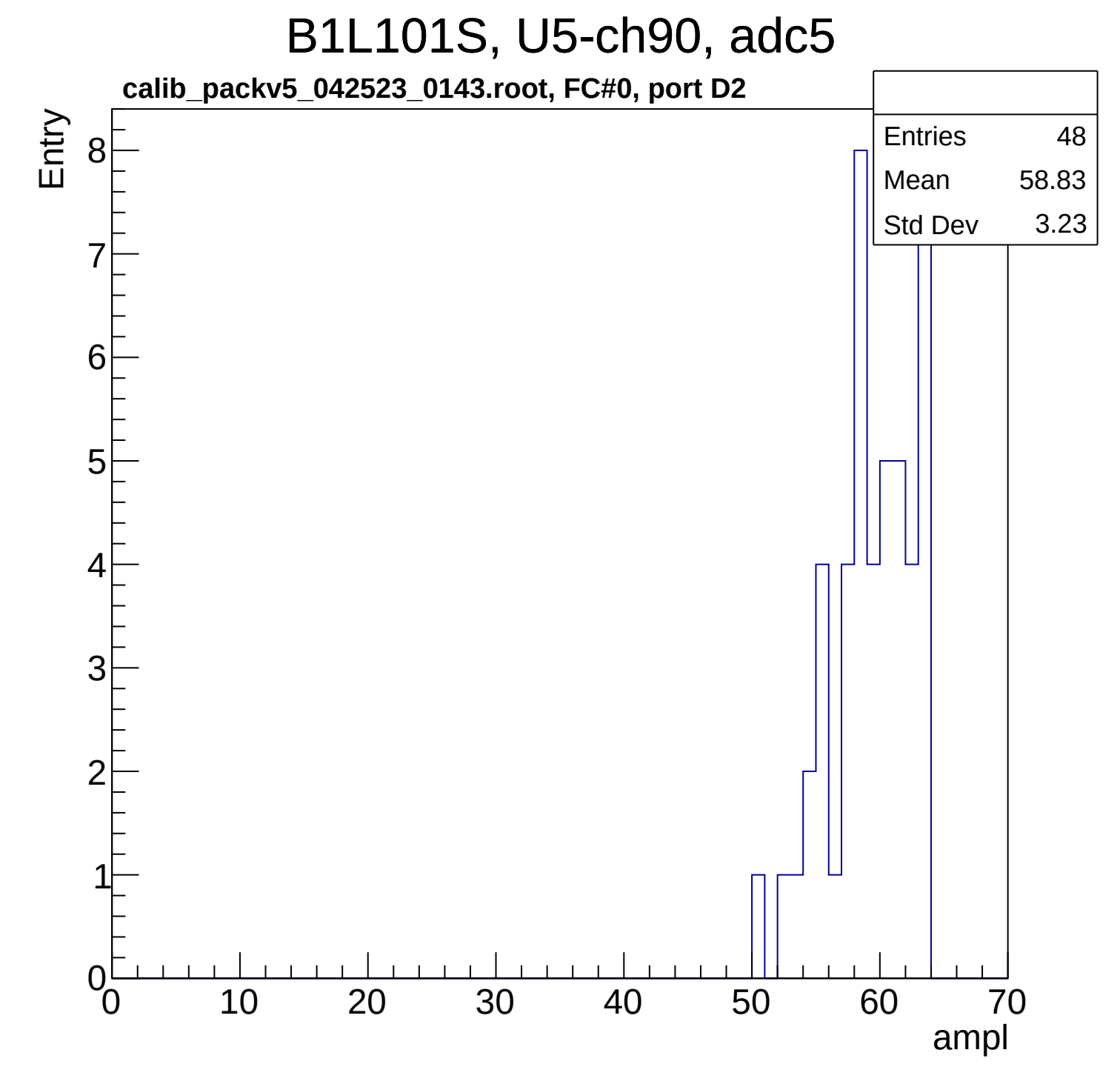
B1L101S, U5-ch90, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 58.83
Std Dev 3.23
Entry
ampl
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1
2
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5
6
7
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0
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40
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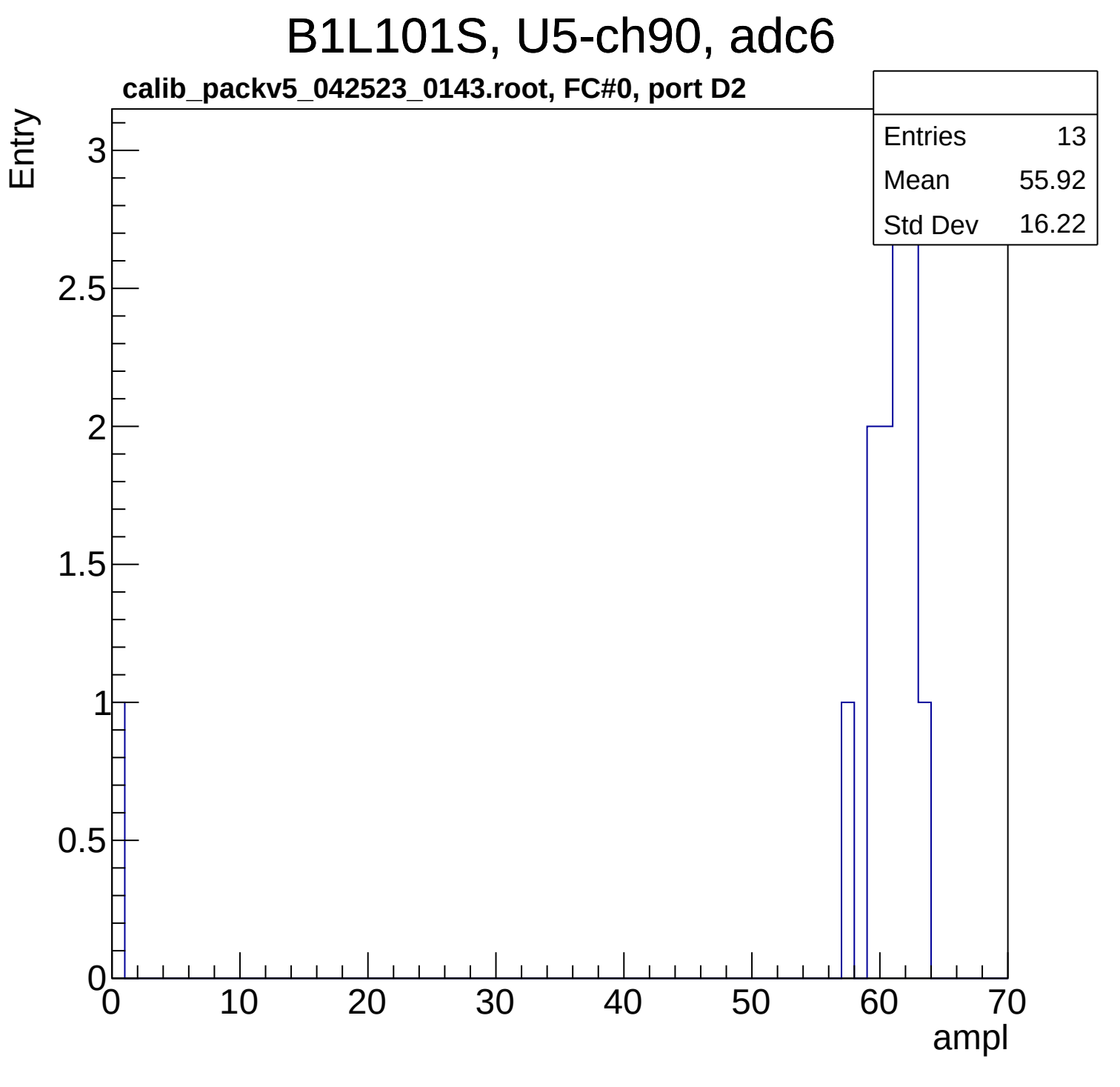
60
70


B1L101S, U5-ch90, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 13
Mean 55.92
Std Dev 16.22
Entry
ampl
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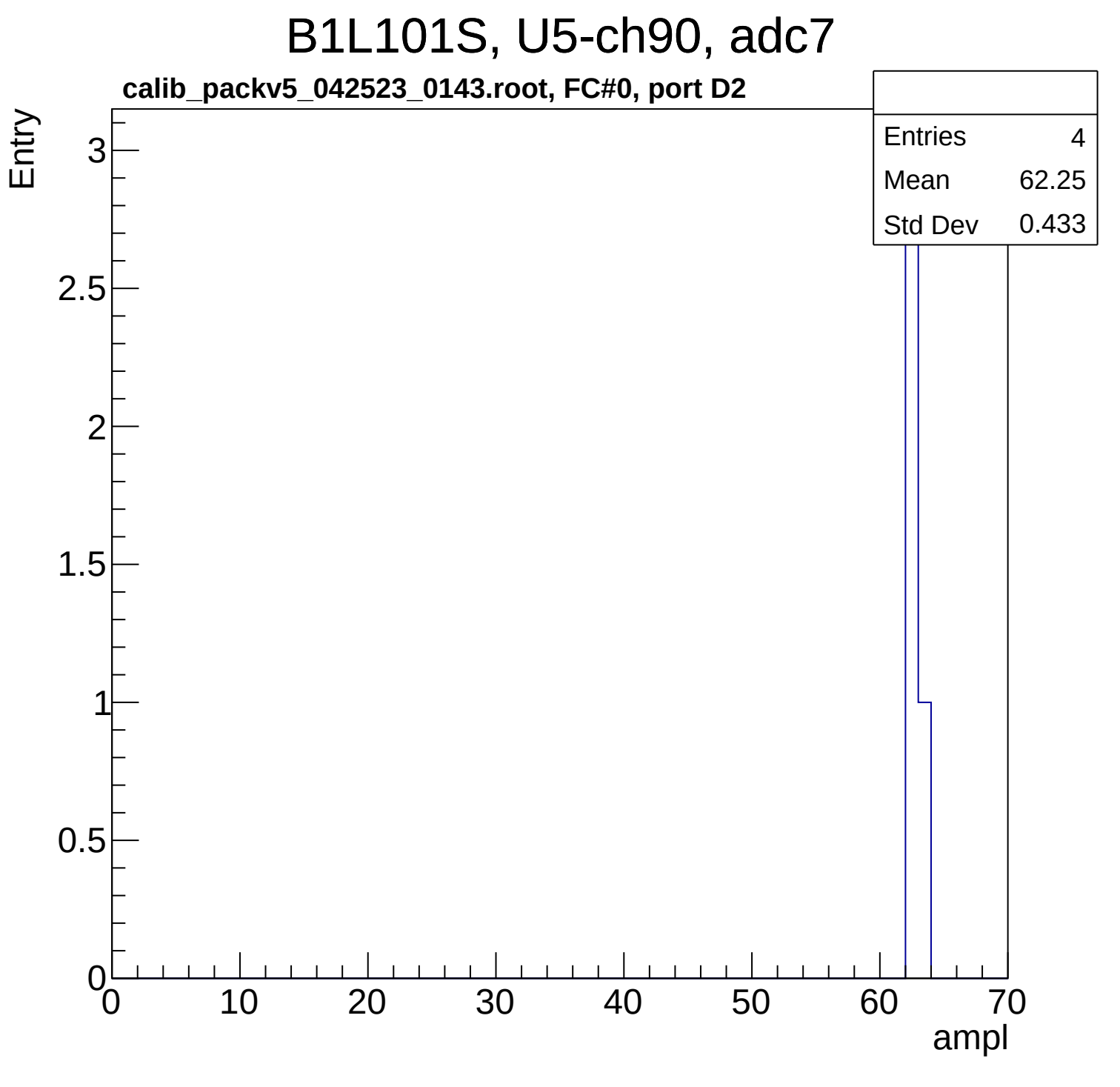
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U5-ch90, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 62.25
Std Dev 0.433
Entry
ampl
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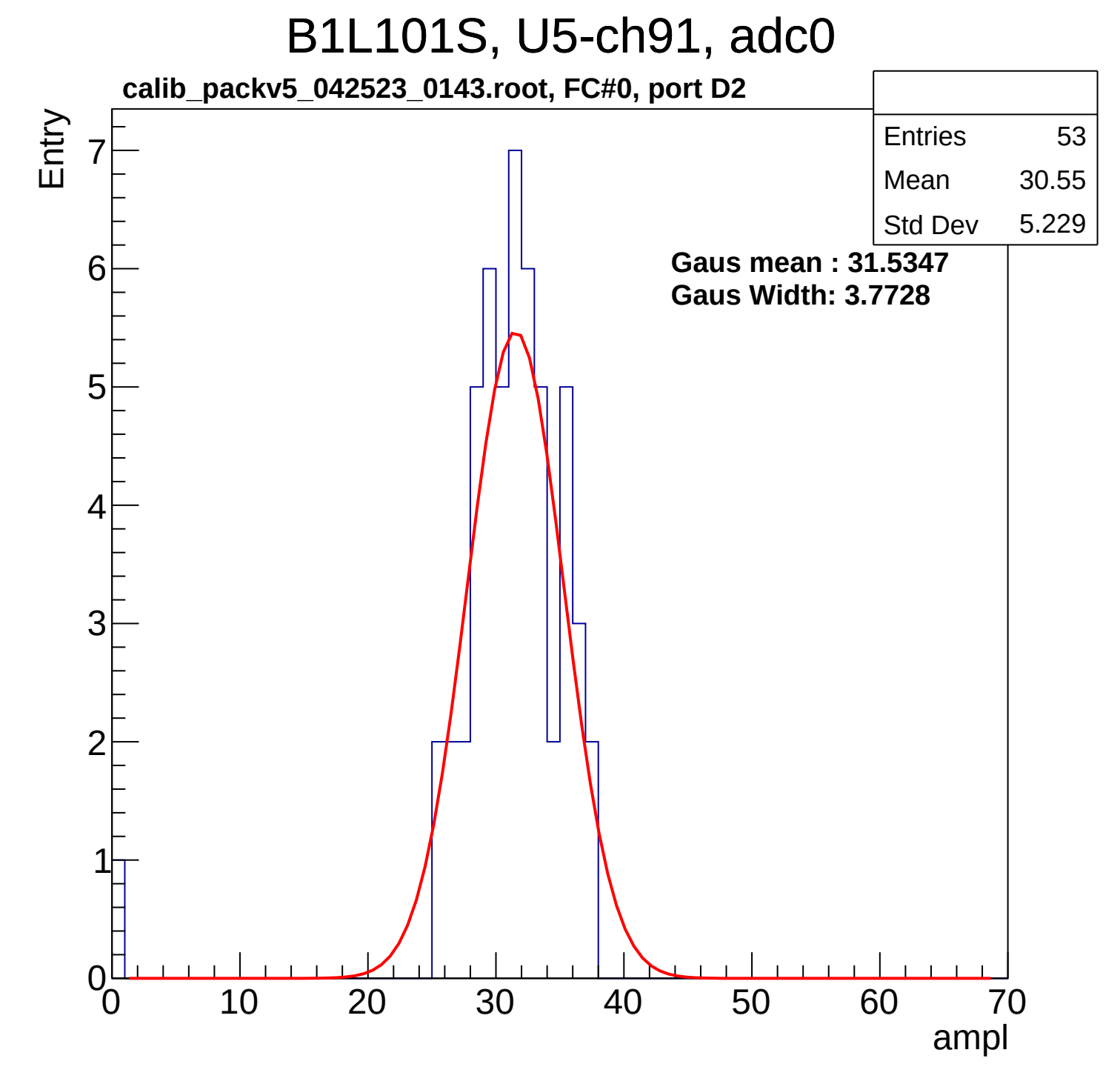
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U5-ch91, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 30.55
Std Dev 5.229
Gaus mean : 31.5347
Gaus Width: 3.7728
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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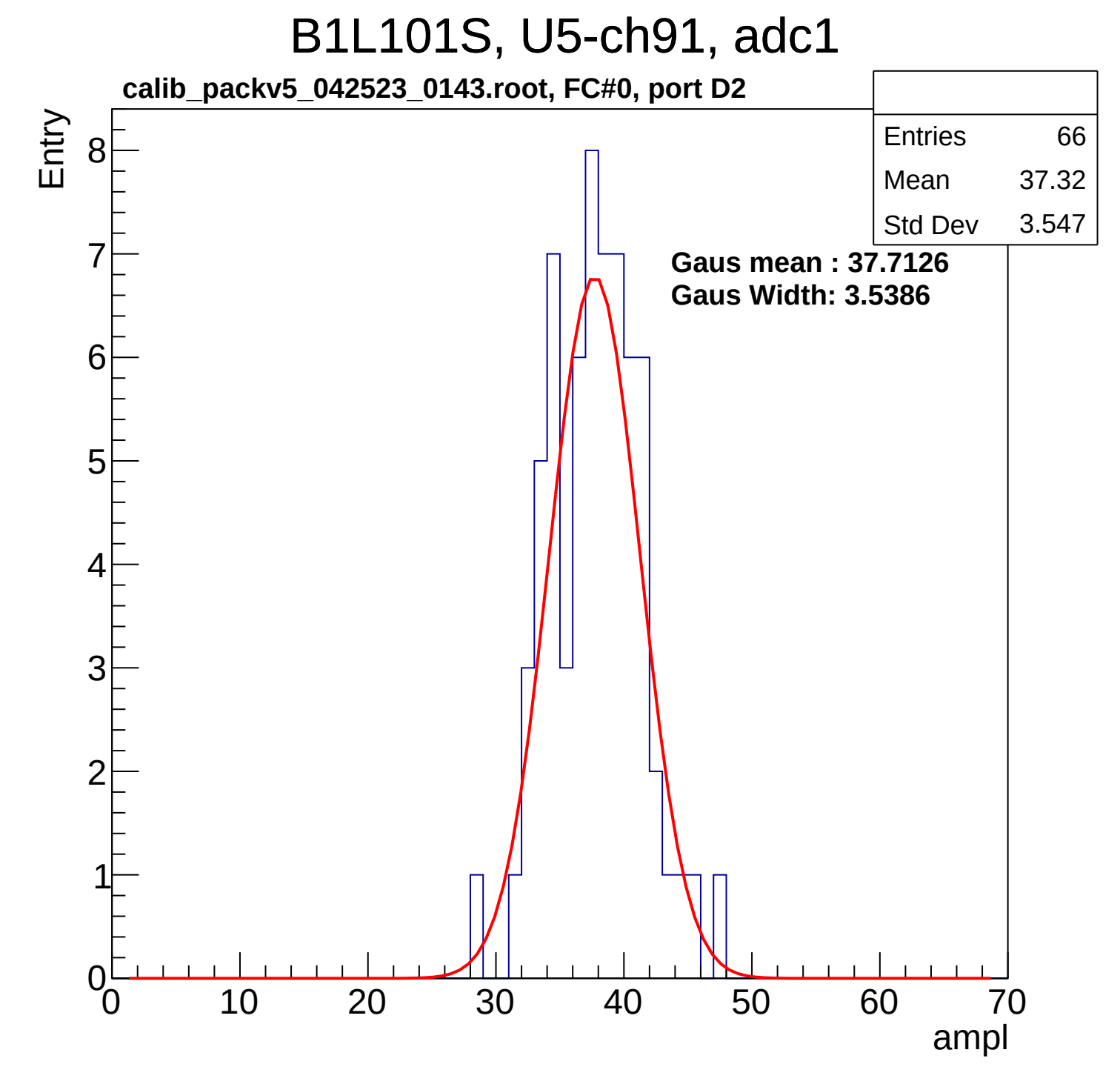
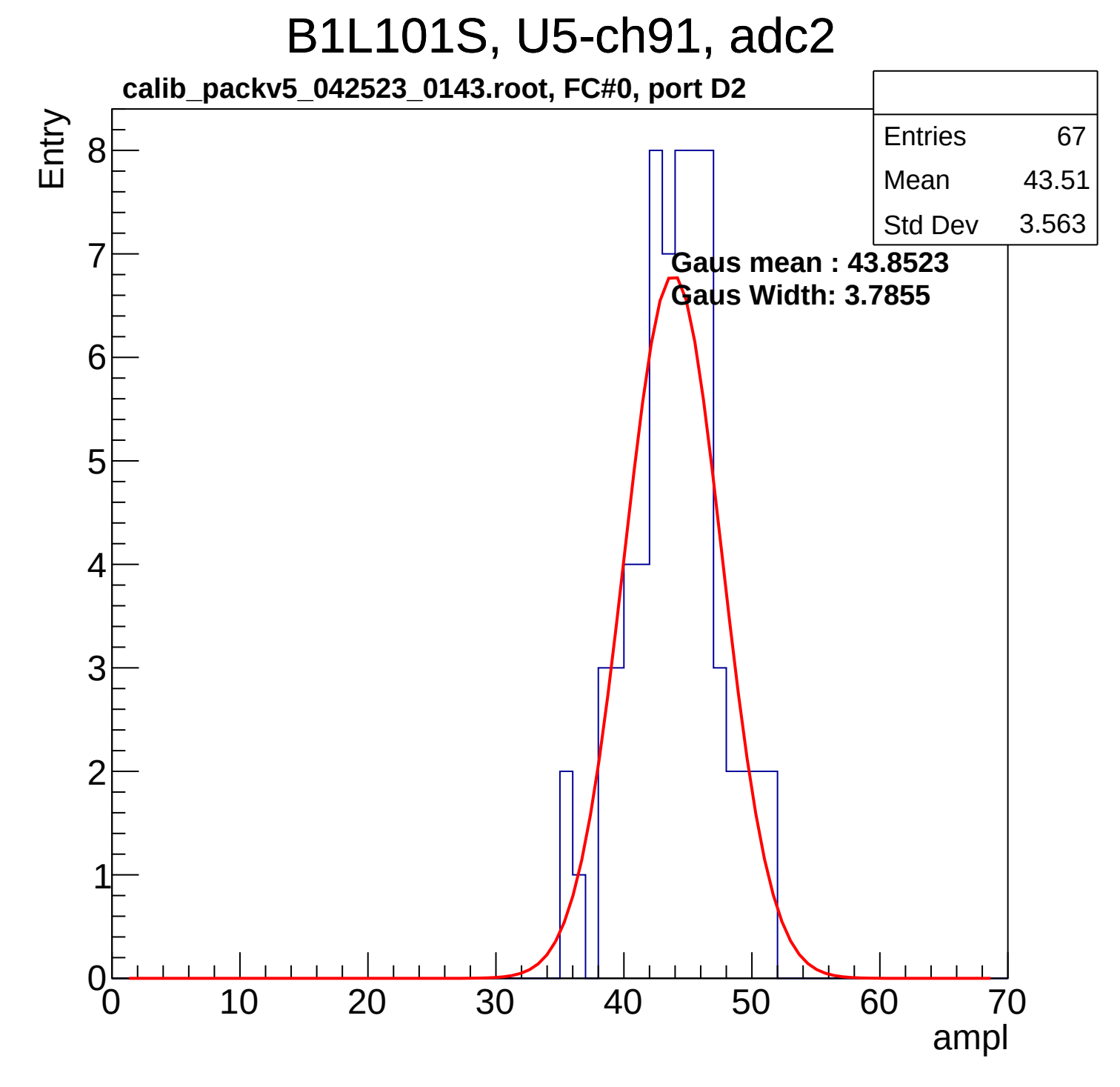

B1L101S, U5-ch91, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 37.32
Std Dev 3.547
Gaus mean : 37.7126
Gaus Width: 3.5386
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch91, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 43.51
Std Dev 3.563
Gaus mean : 43.8523
Gaus Width: 3.7855
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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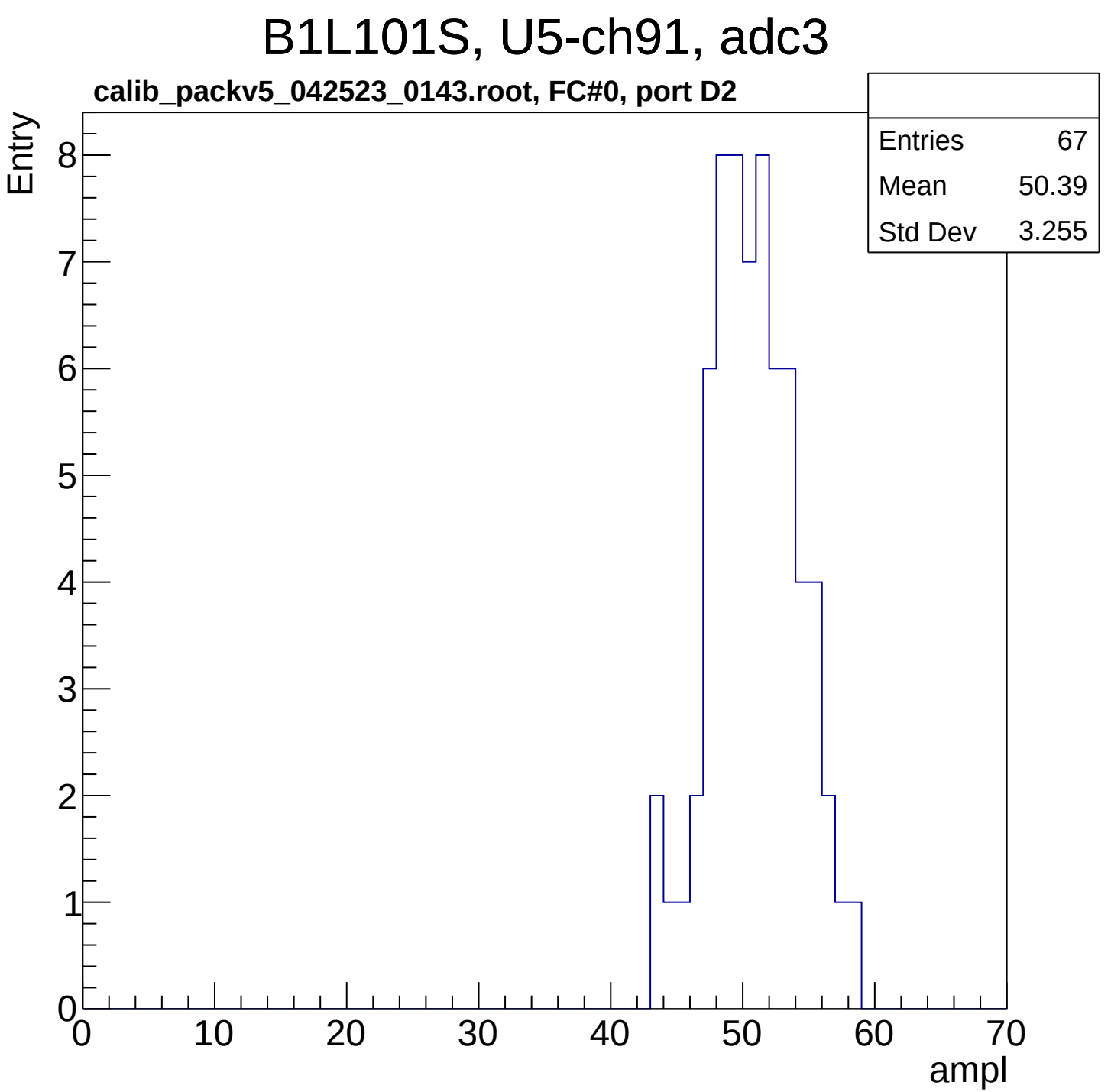
B1L101S, U5-ch91, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 50.39
Std Dev 3.255
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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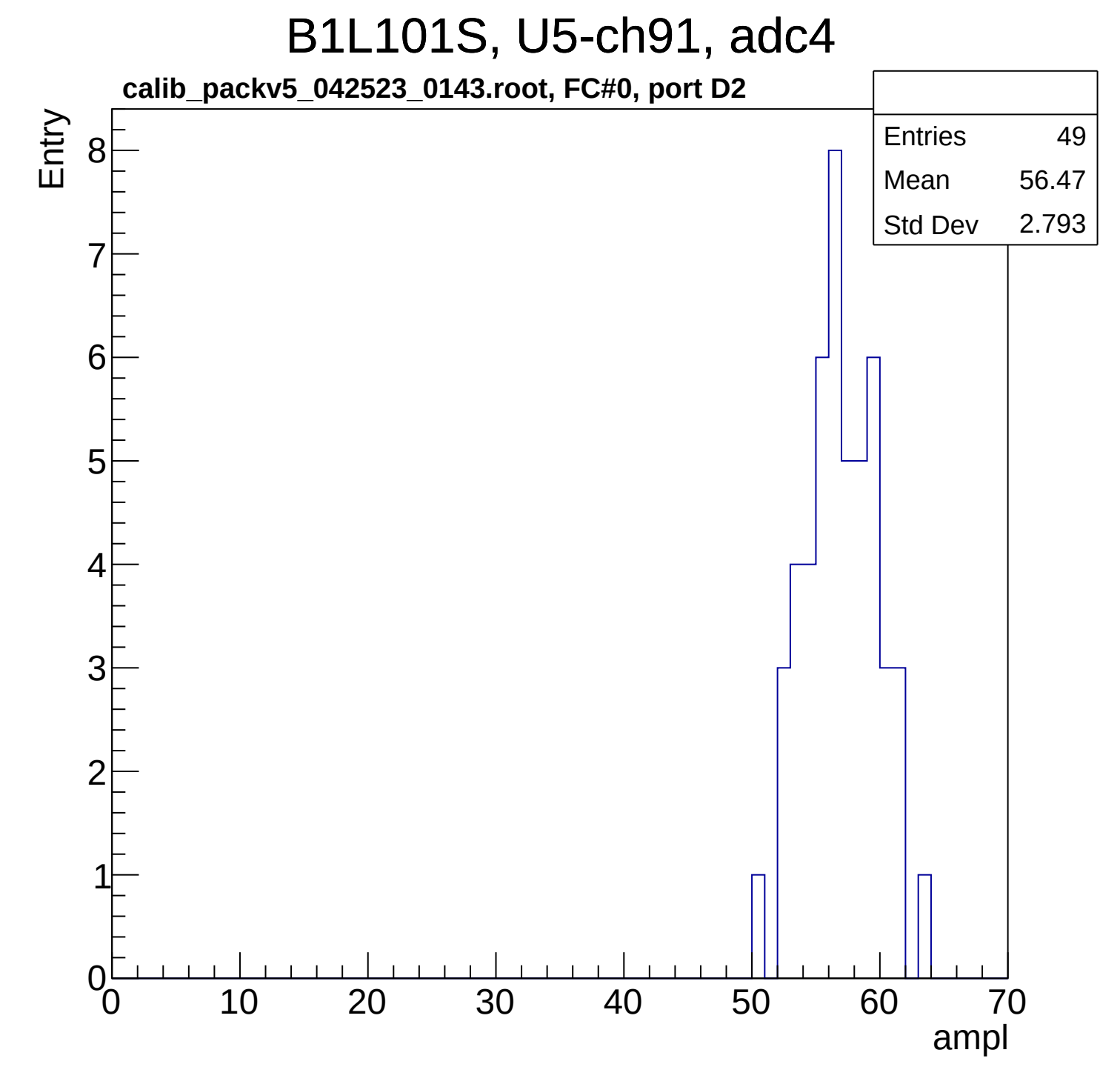
40
50
60
70


B1L101S, U5-ch91, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 56.47
Std Dev 2.793
Entry
ampl
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1
2
3
4
5
6
7
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0
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40
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60
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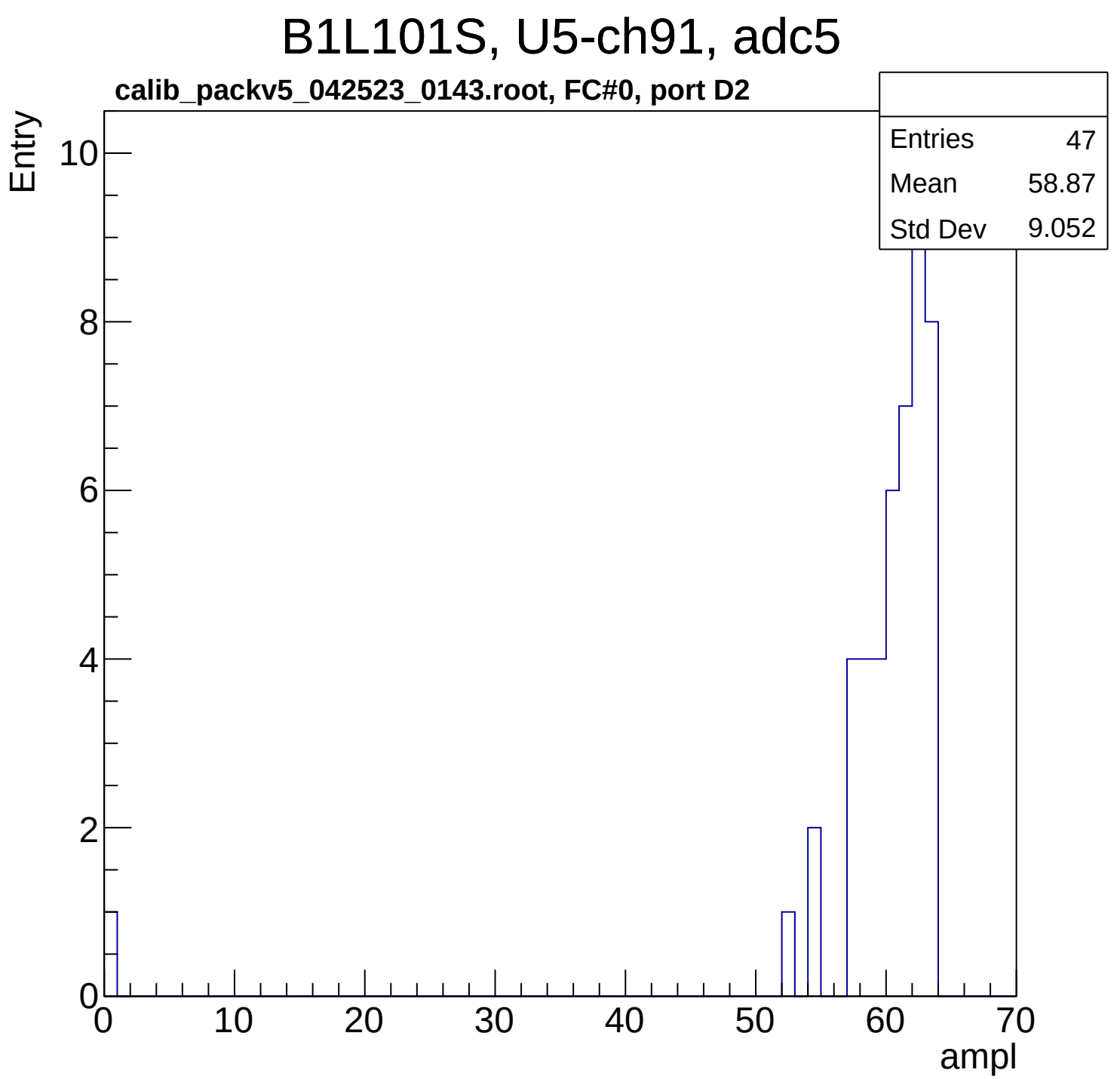
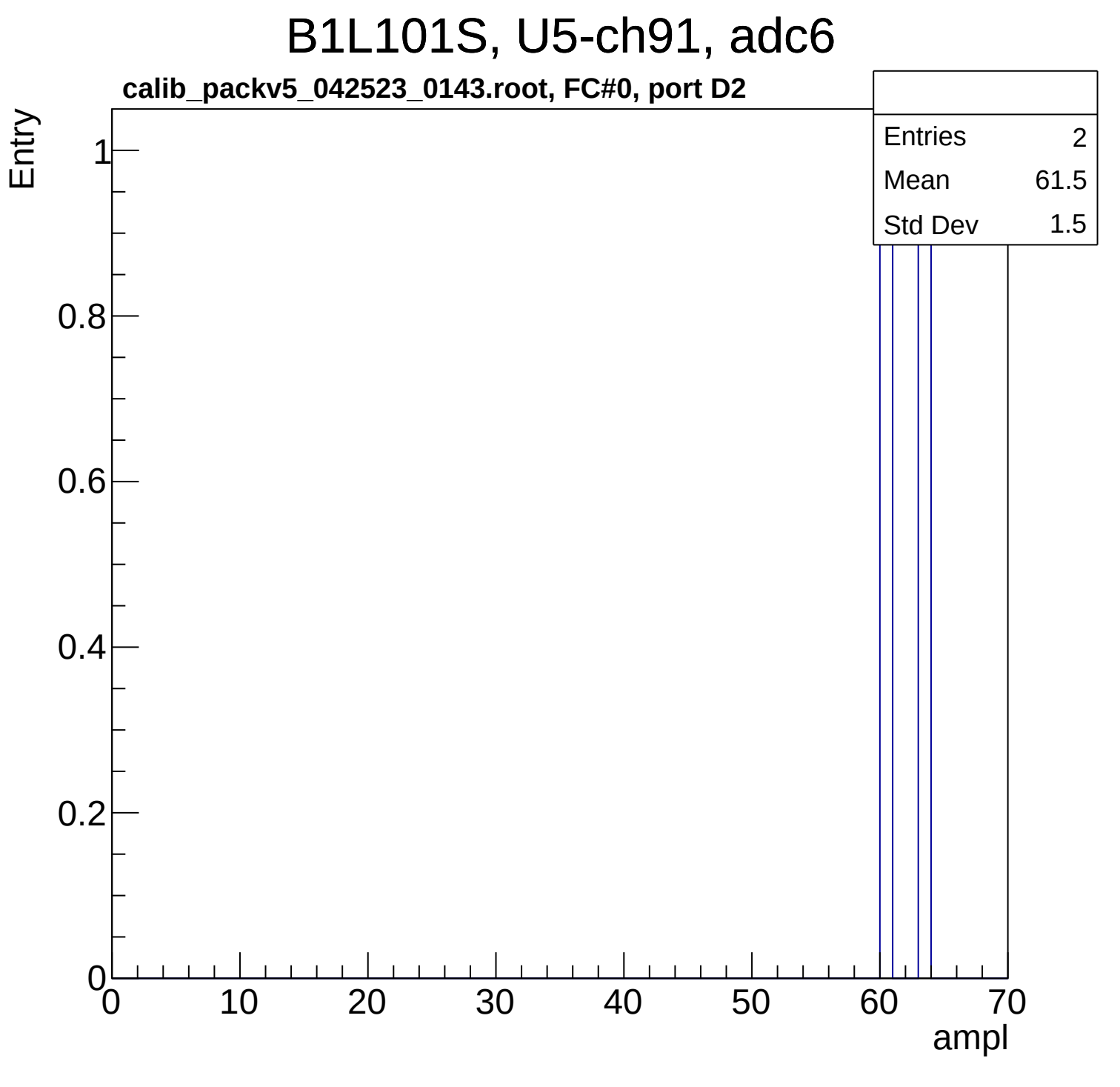

B1L101S, U5-ch91, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 58.87
Std Dev 9.052
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch91, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 61.5
Std Dev 1.5
Entry
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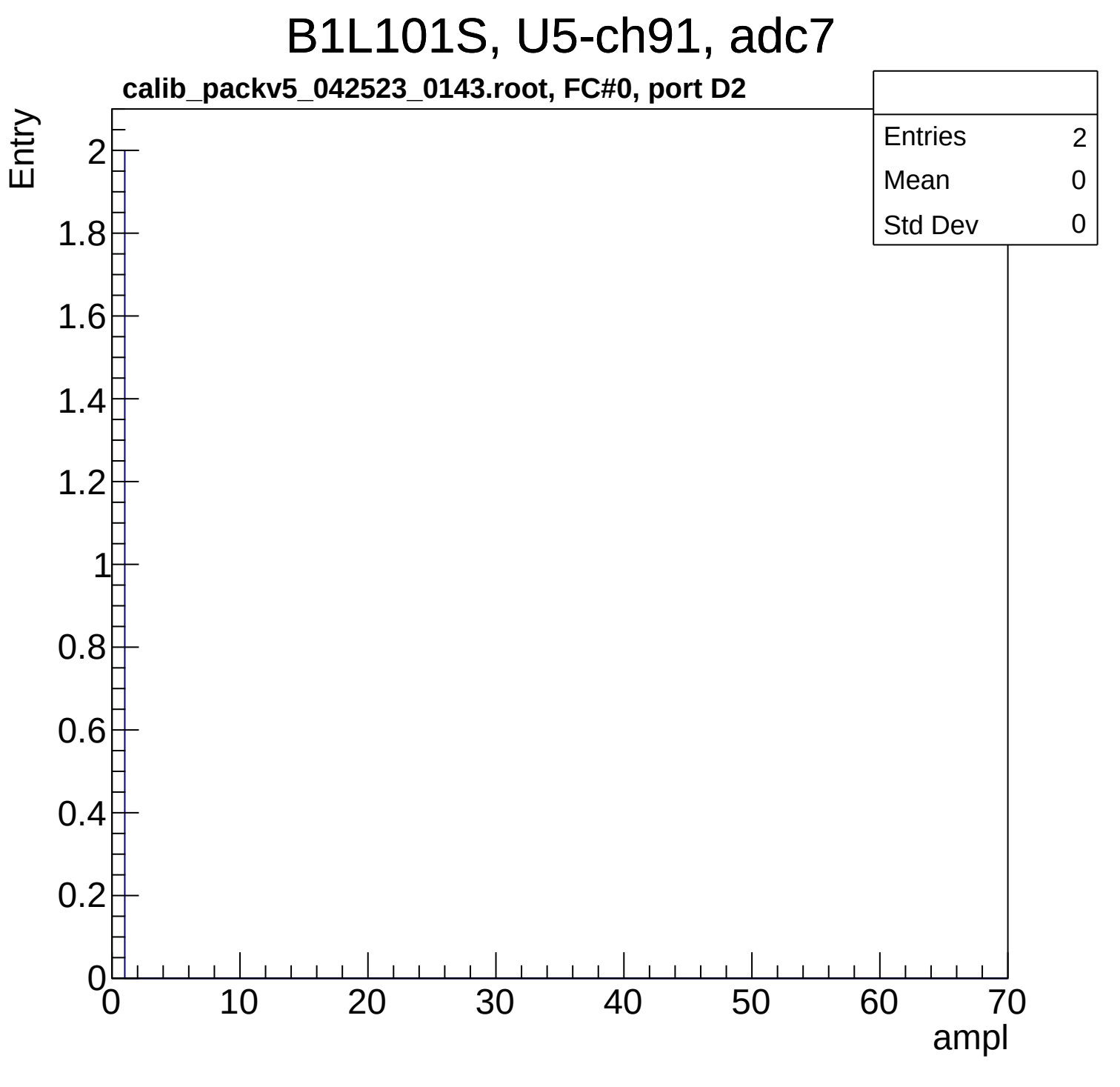
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch91, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
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1.2
1.4
1.6
1.8
2
0
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40
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60
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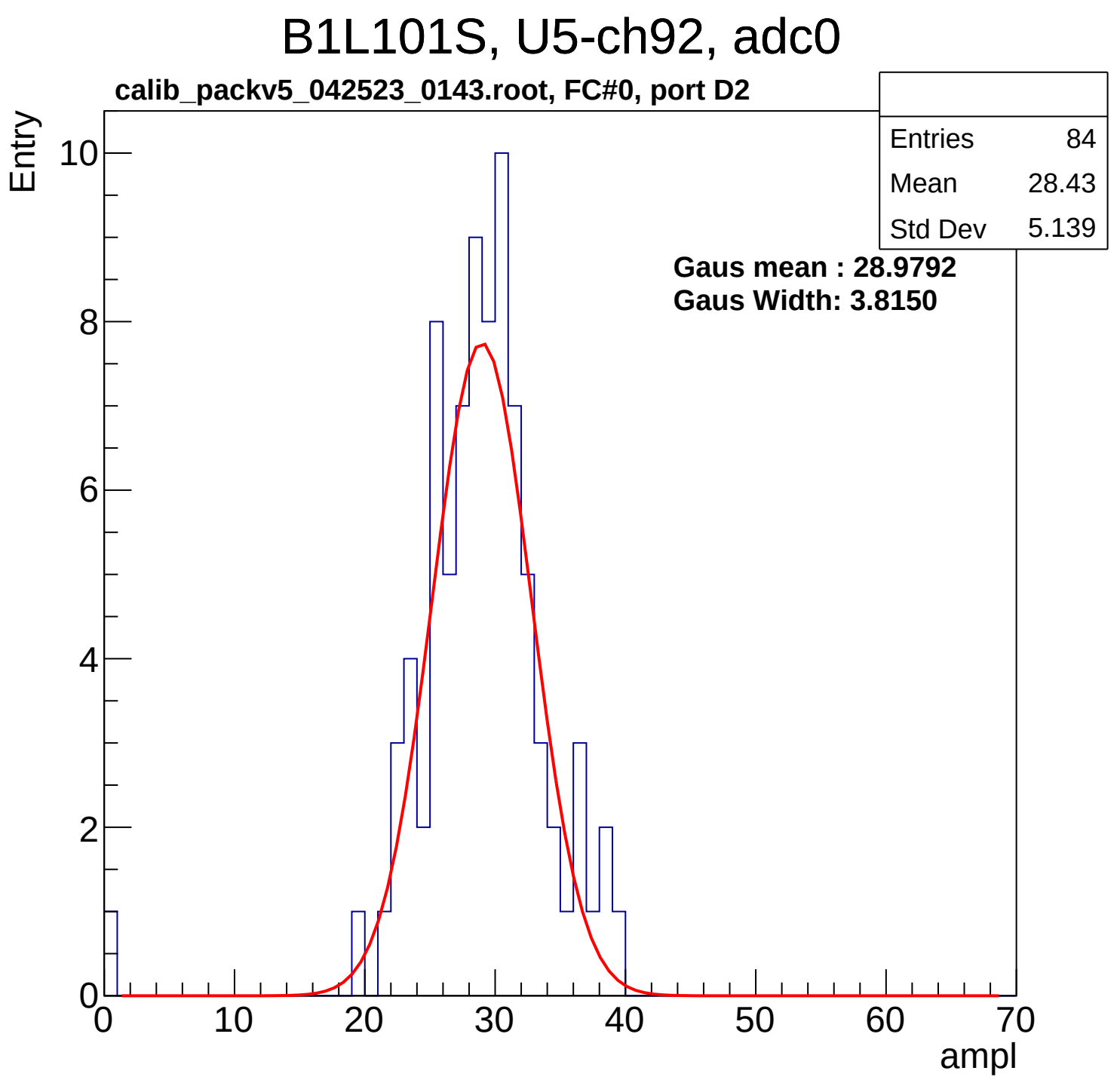
B1L101S, U5-ch92, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 84
Mean 28.43
Std Dev 5.139
Gaus mean : 28.9792
Gaus Width: 3.8150
Entry
ampl
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2
4
6
8
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0
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20
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40
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60
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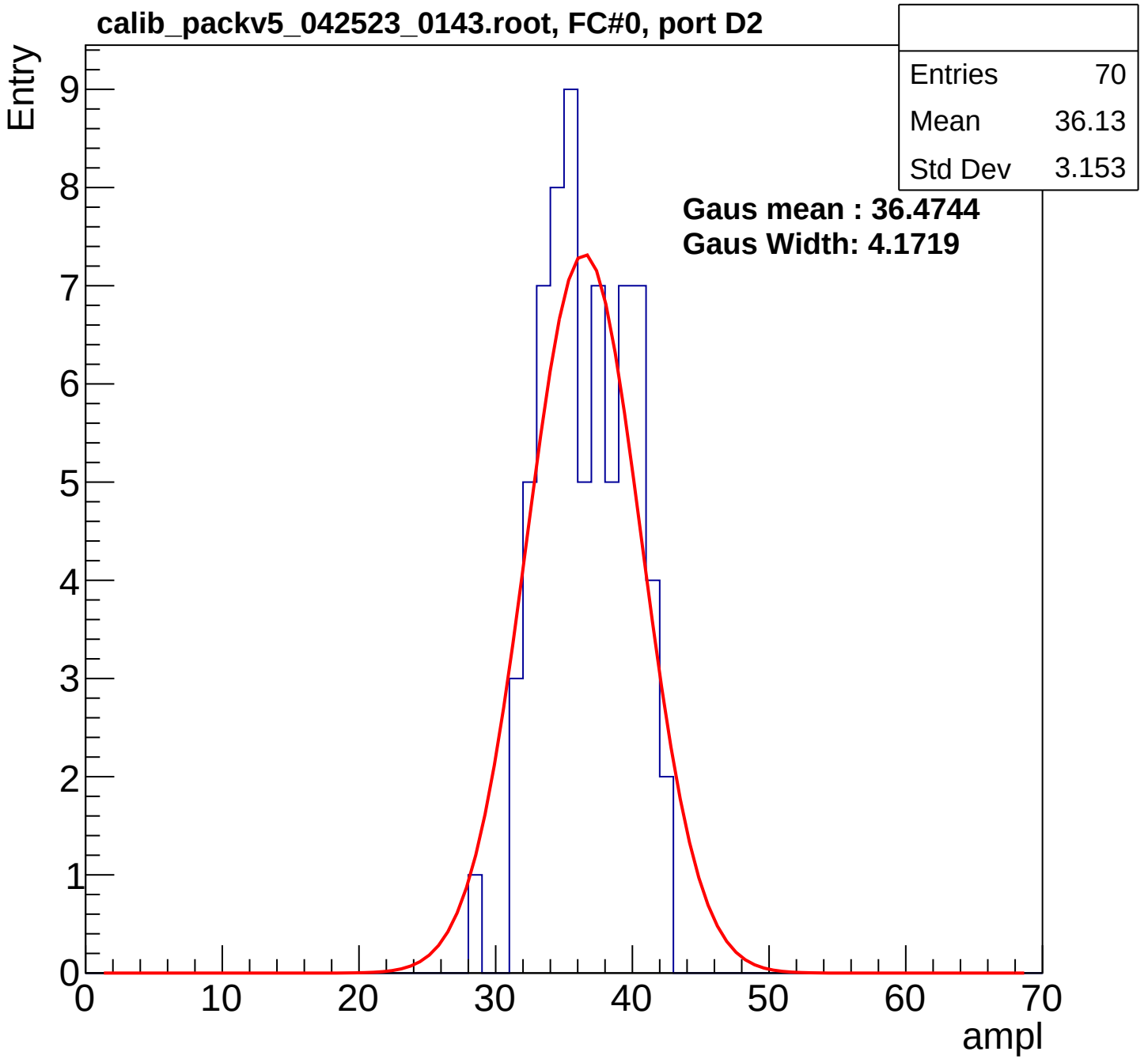
B1L101S, U5-ch92, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 36.13
Std Dev 3.153
Gaus mean : 36.4744
Gaus Width: 4.1719
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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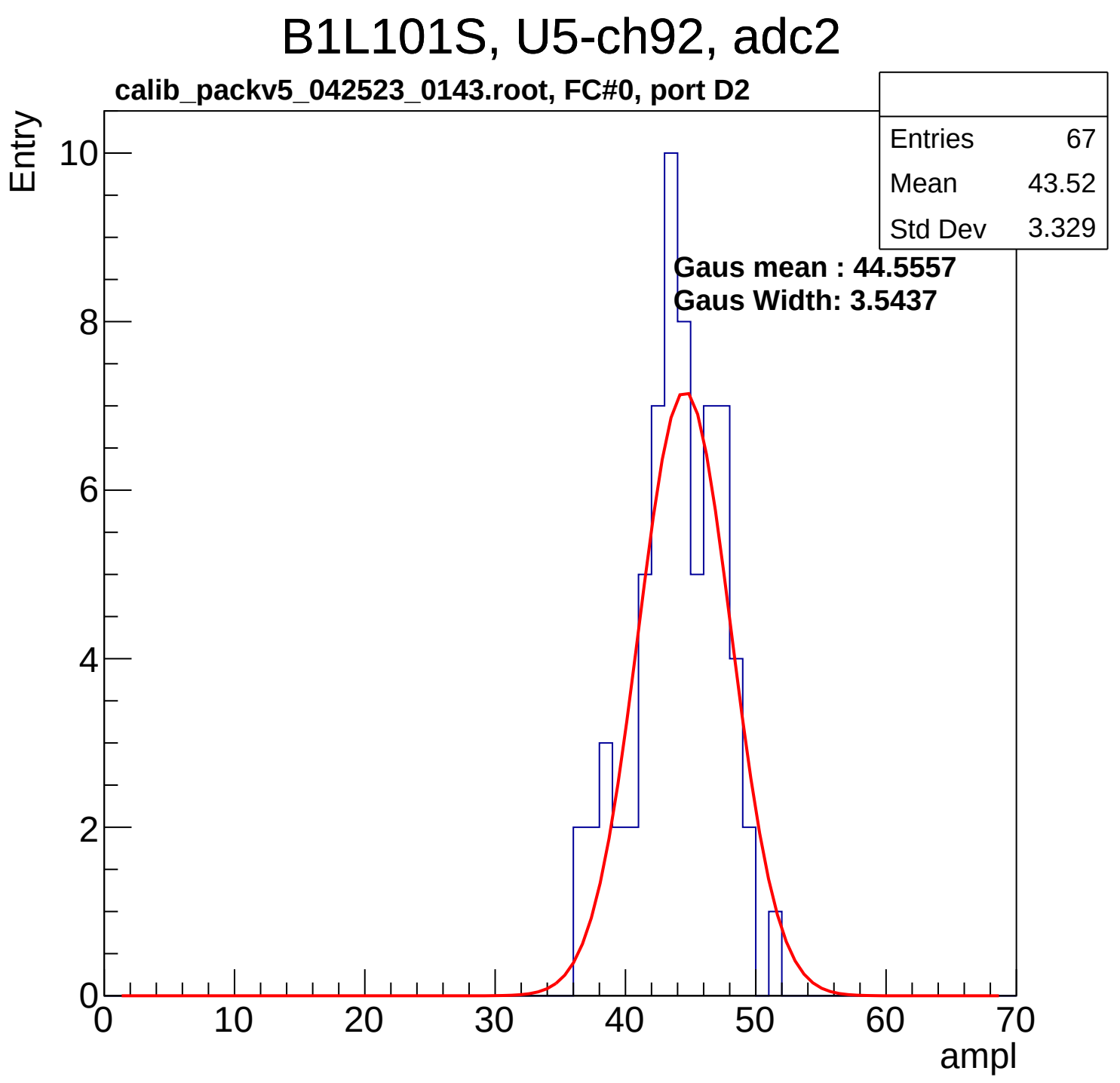
B1L101S, U5-ch92, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 43.52
Std Dev 3.329
Gaus mean : 44.5557
Gaus Width: 3.5437
Entry
ampl
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4
6
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10
0
10
20
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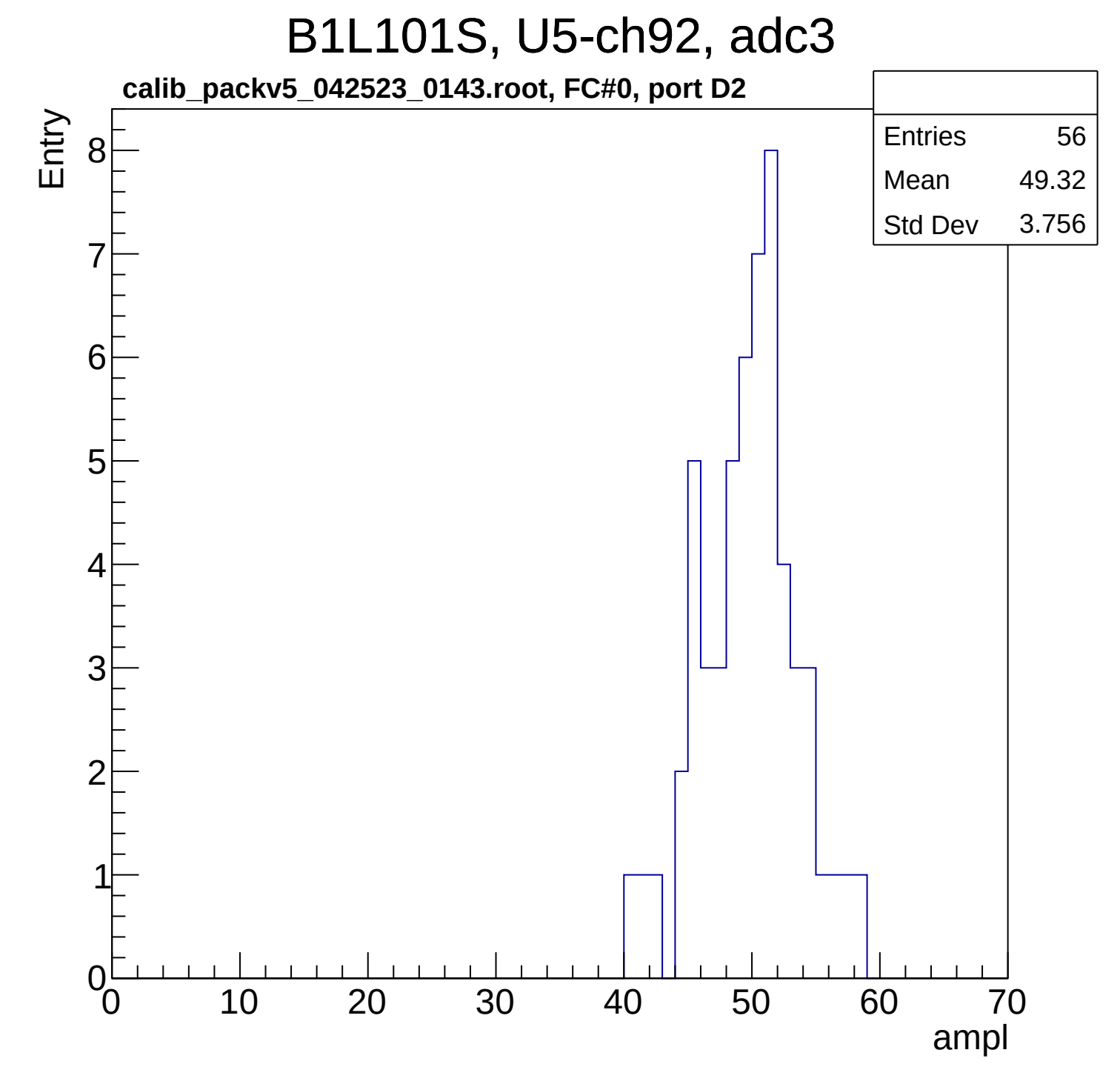
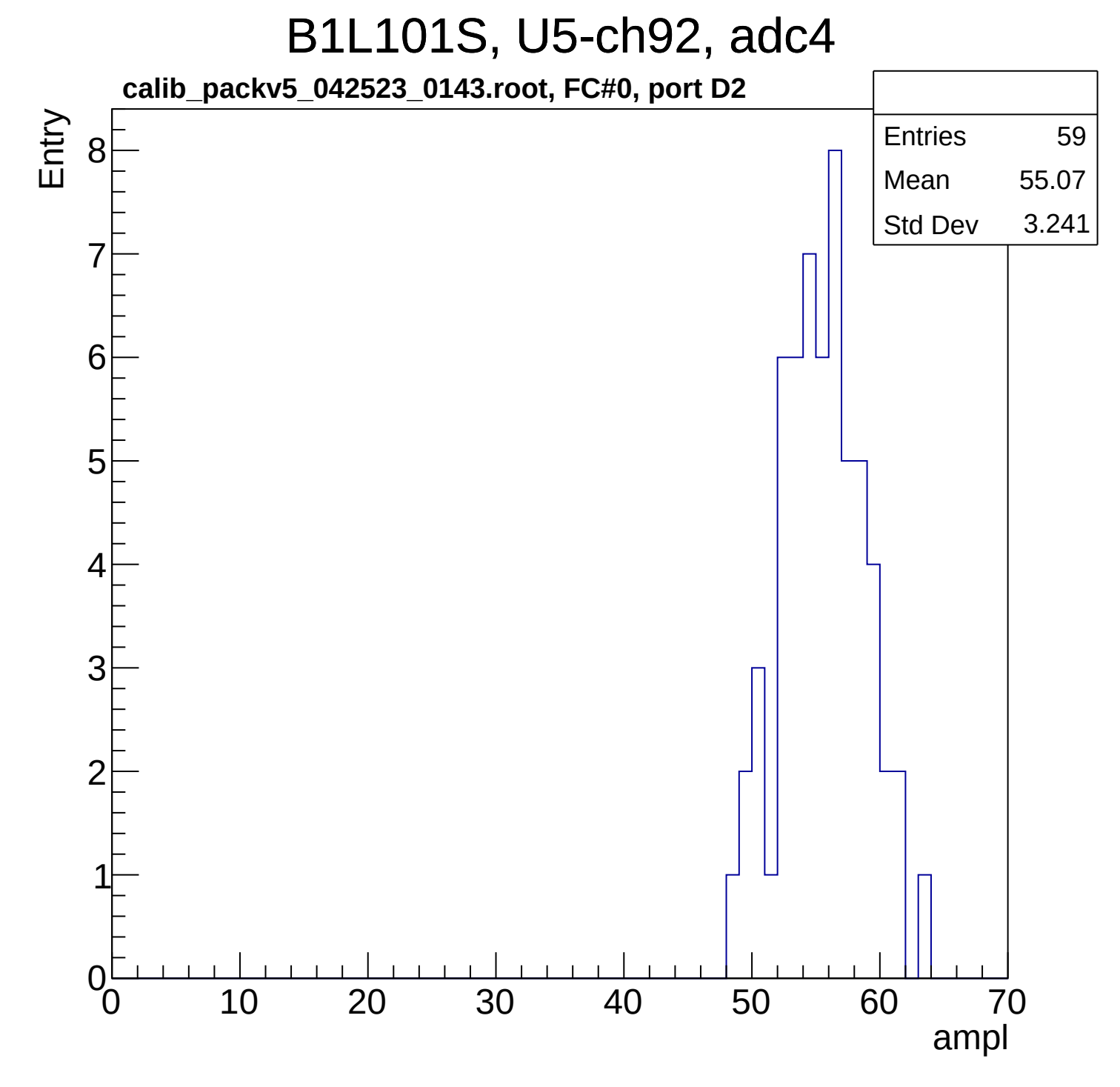
40
50
60
70


B1L101S, U5-ch92, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 49.32
Std Dev 3.756
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch92, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 55.07
Std Dev 3.241
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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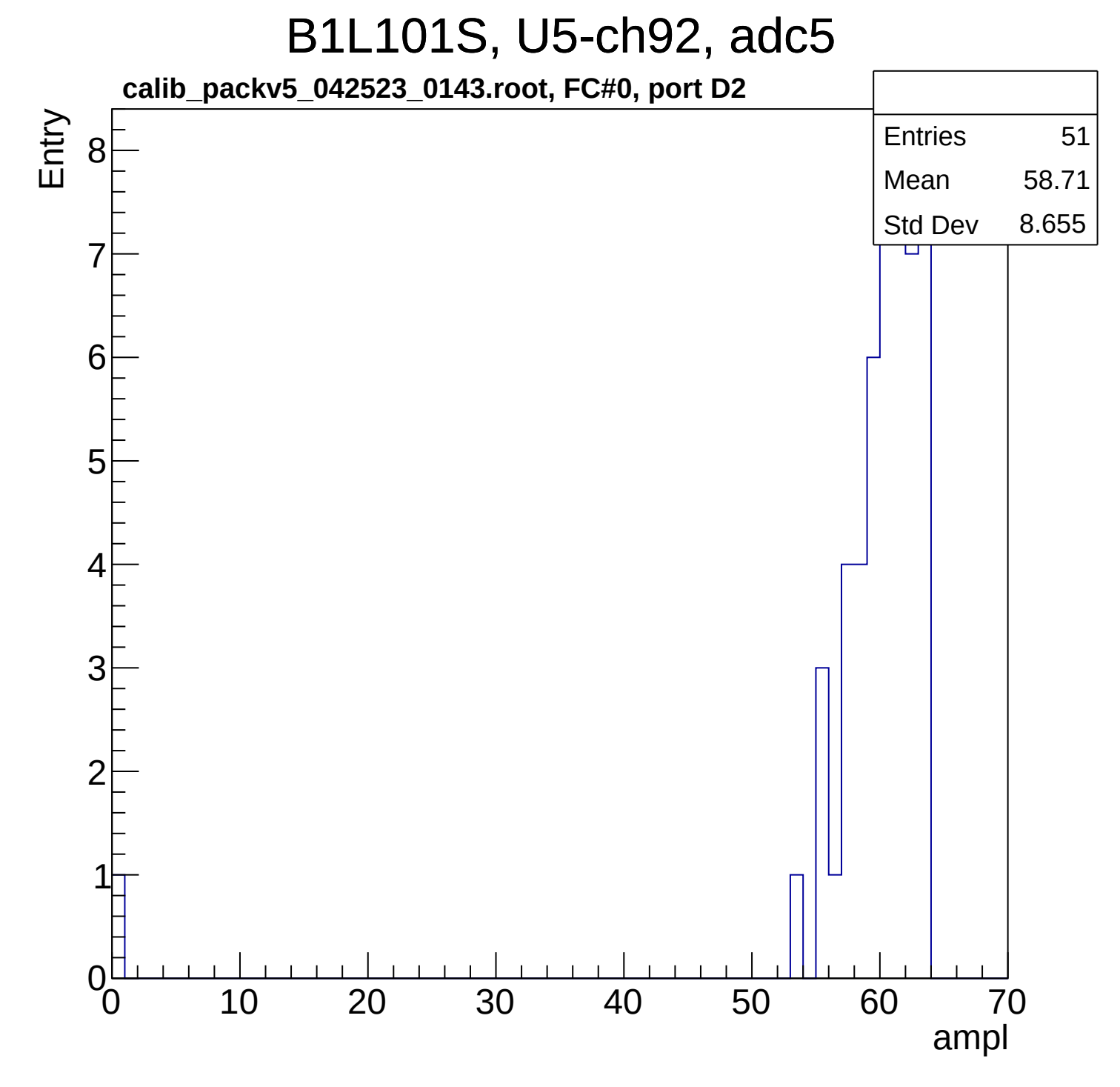
40
50
60
70


B1L101S, U5-ch92, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 58.71
Std Dev 8.655
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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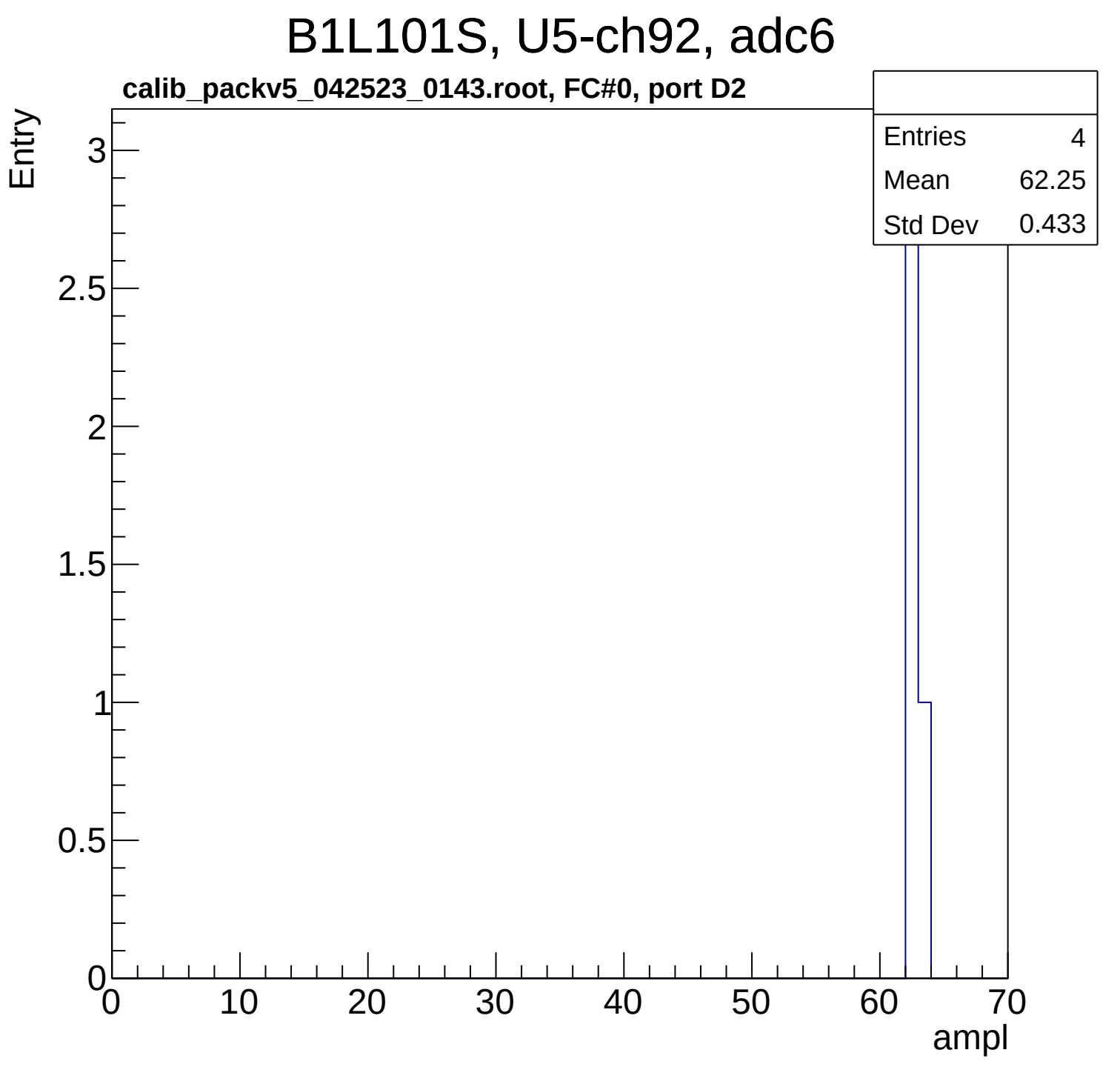
B1L101S, U5-ch92, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 62.25
Std Dev 0.433
Entry
ampl
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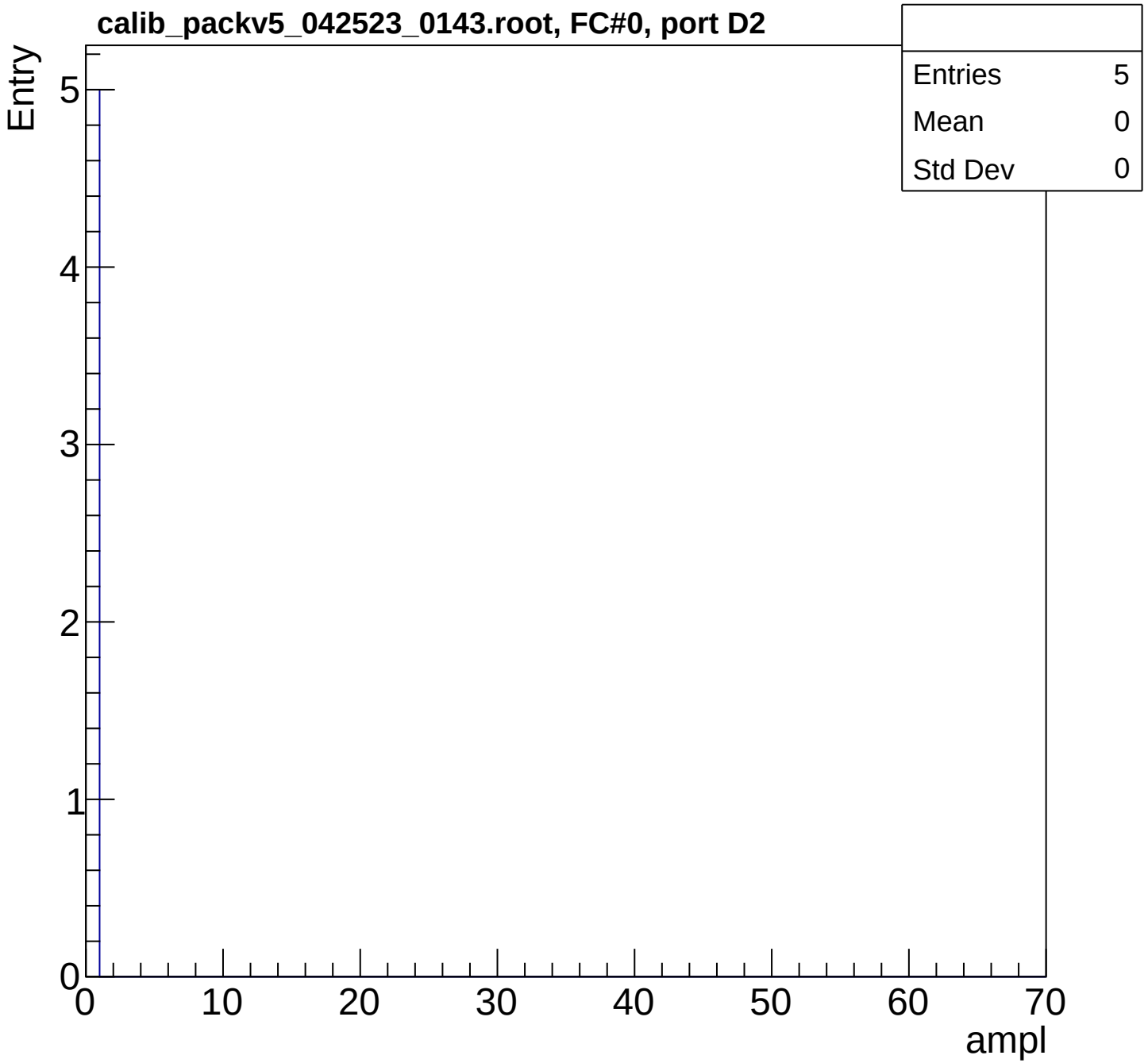
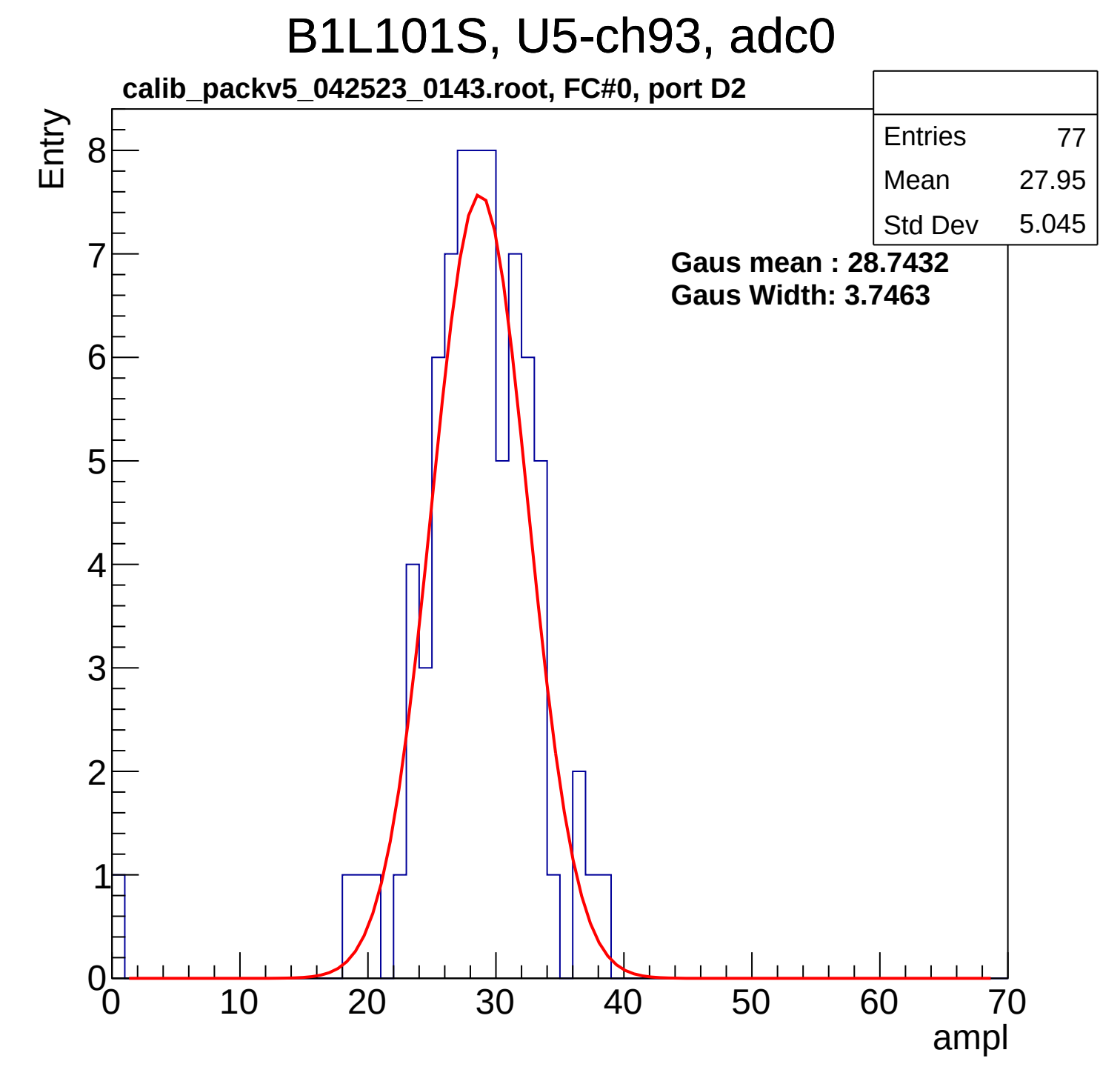
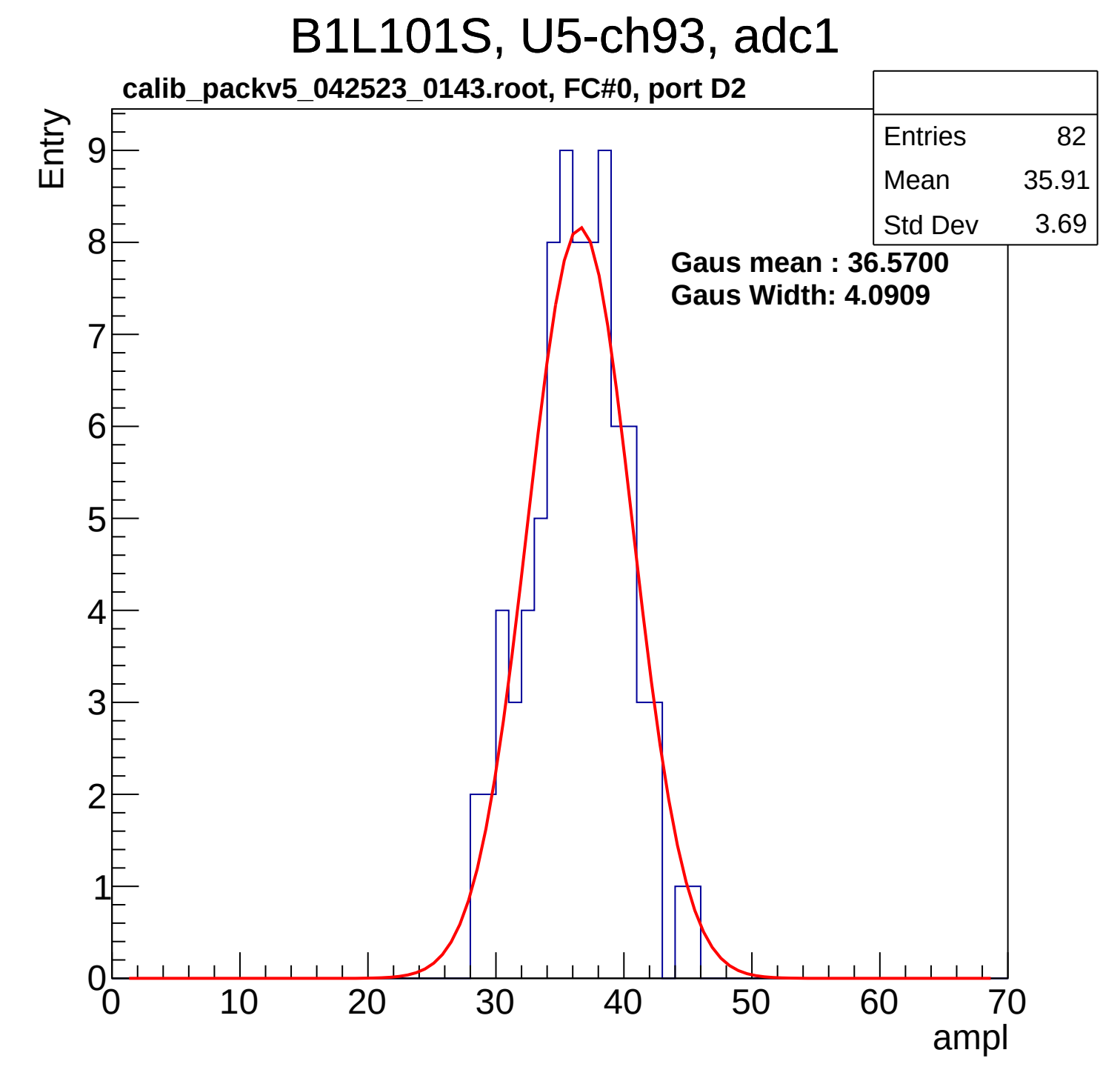
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U5-ch92, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 0
Std Dev 0
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch93, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 27.95
Std Dev 5.045
Gaus mean : 28.7432
Gaus Width: 3.7463
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch93, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 82
Mean 35.91
Std Dev 3.69
Gaus mean : 36.5700
Gaus Width: 4.0909
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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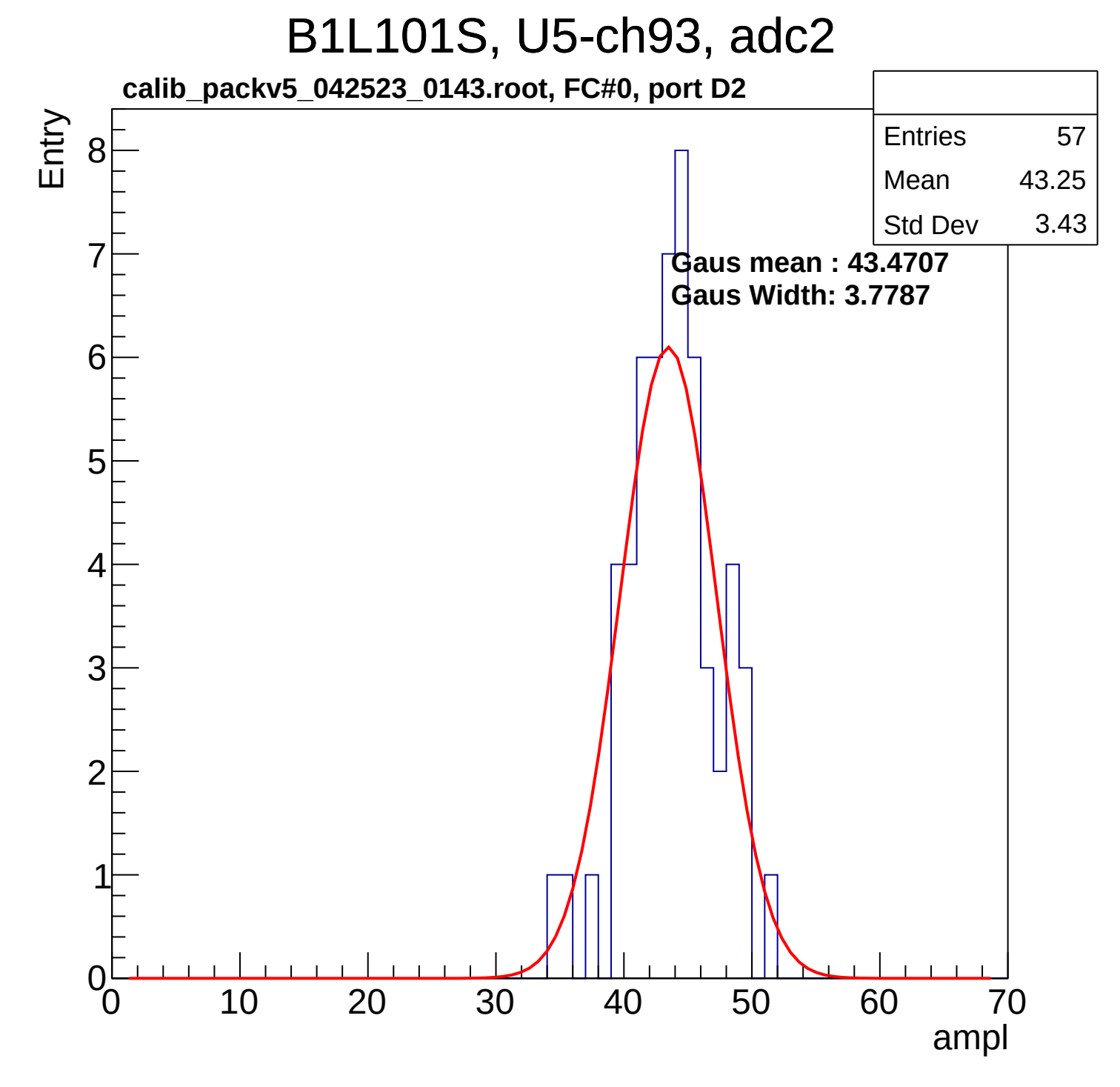
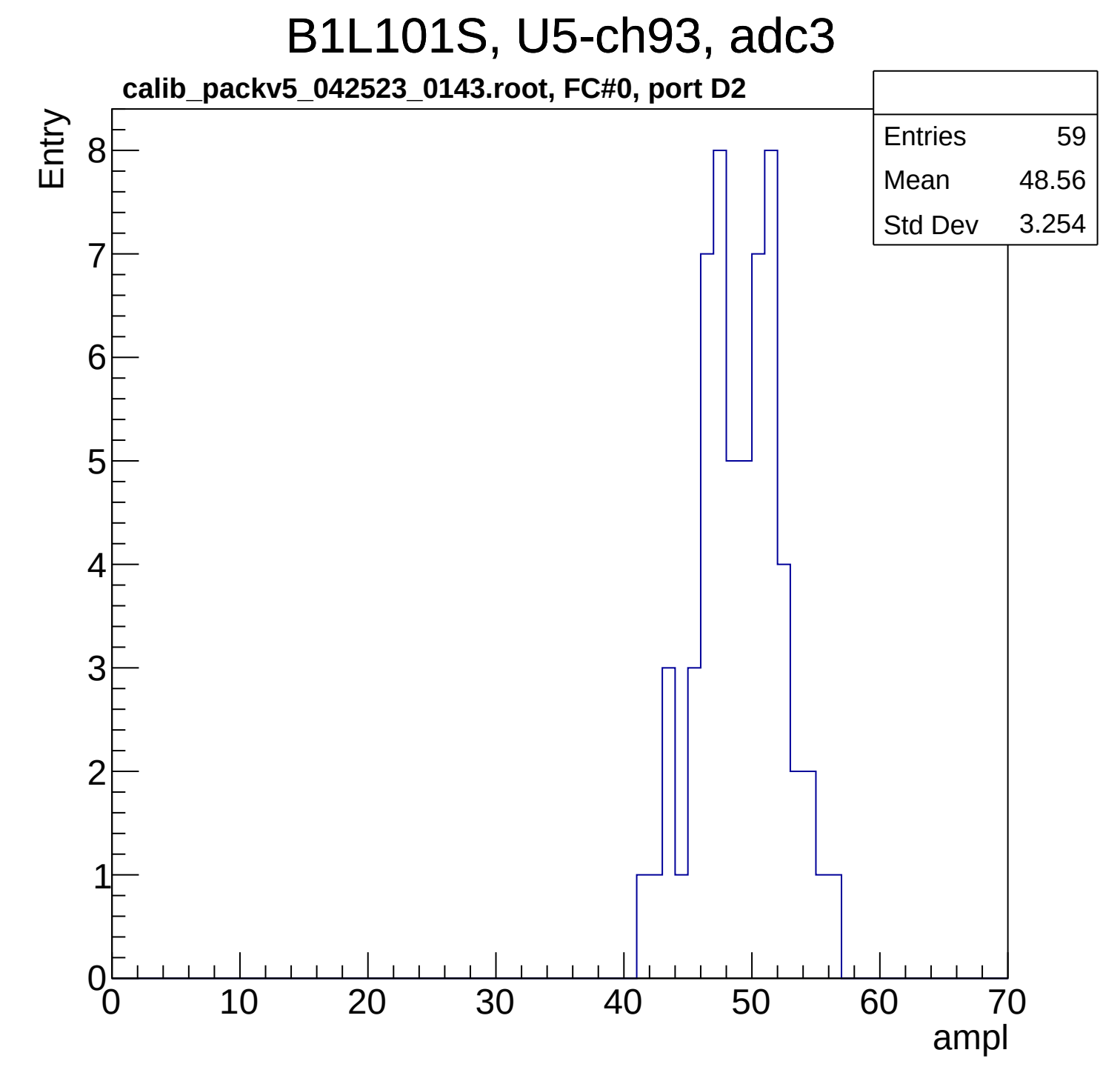
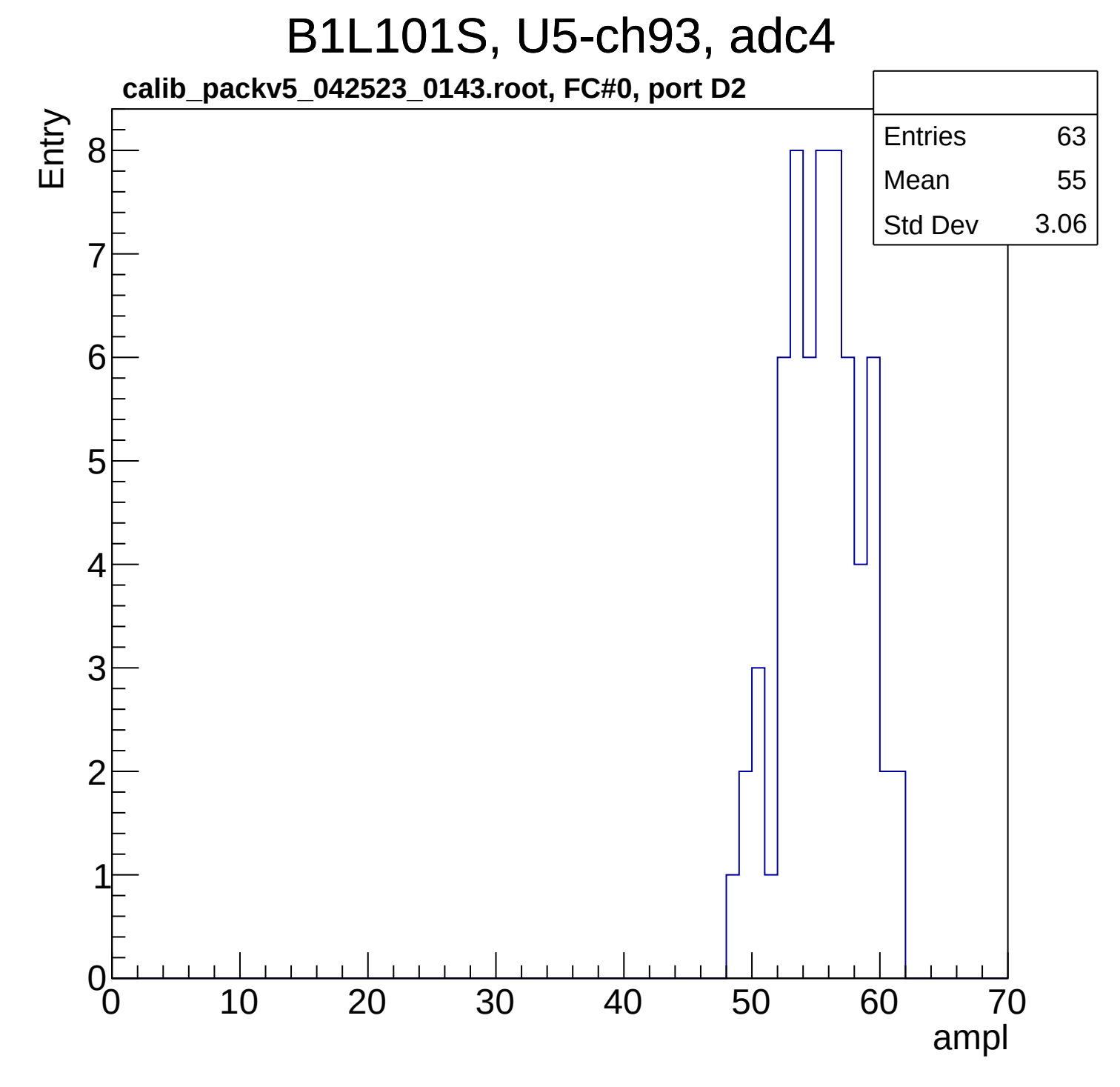
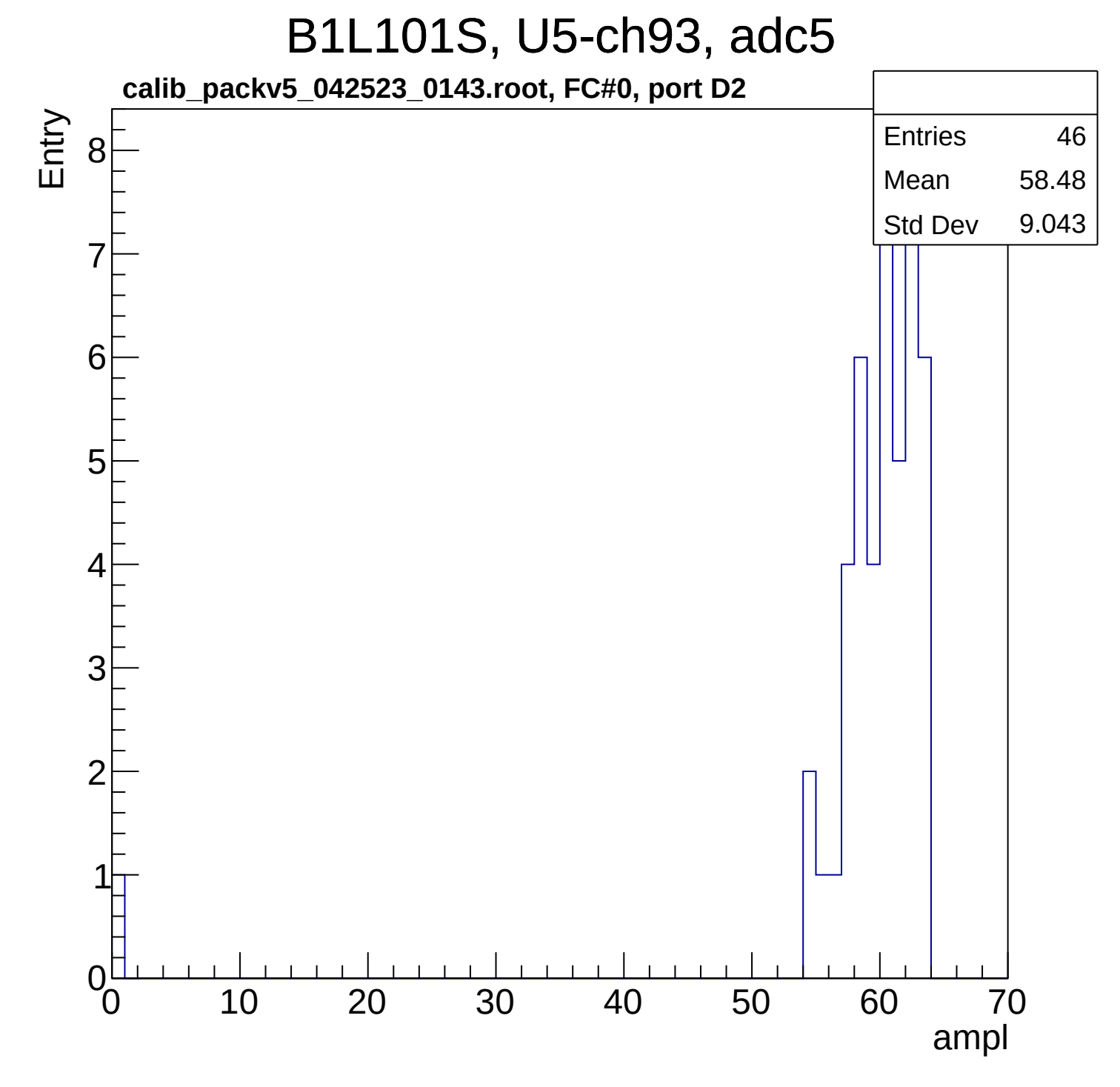

B1L101S, U5-ch93, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 43.25
Std Dev 3.43
Gaus mean : 43.4707
Gaus Width: 3.7787
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch93, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 48.56
Std Dev 3.254
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch93, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 55
Std Dev 3.06
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch93, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 58.48
Std Dev 9.043
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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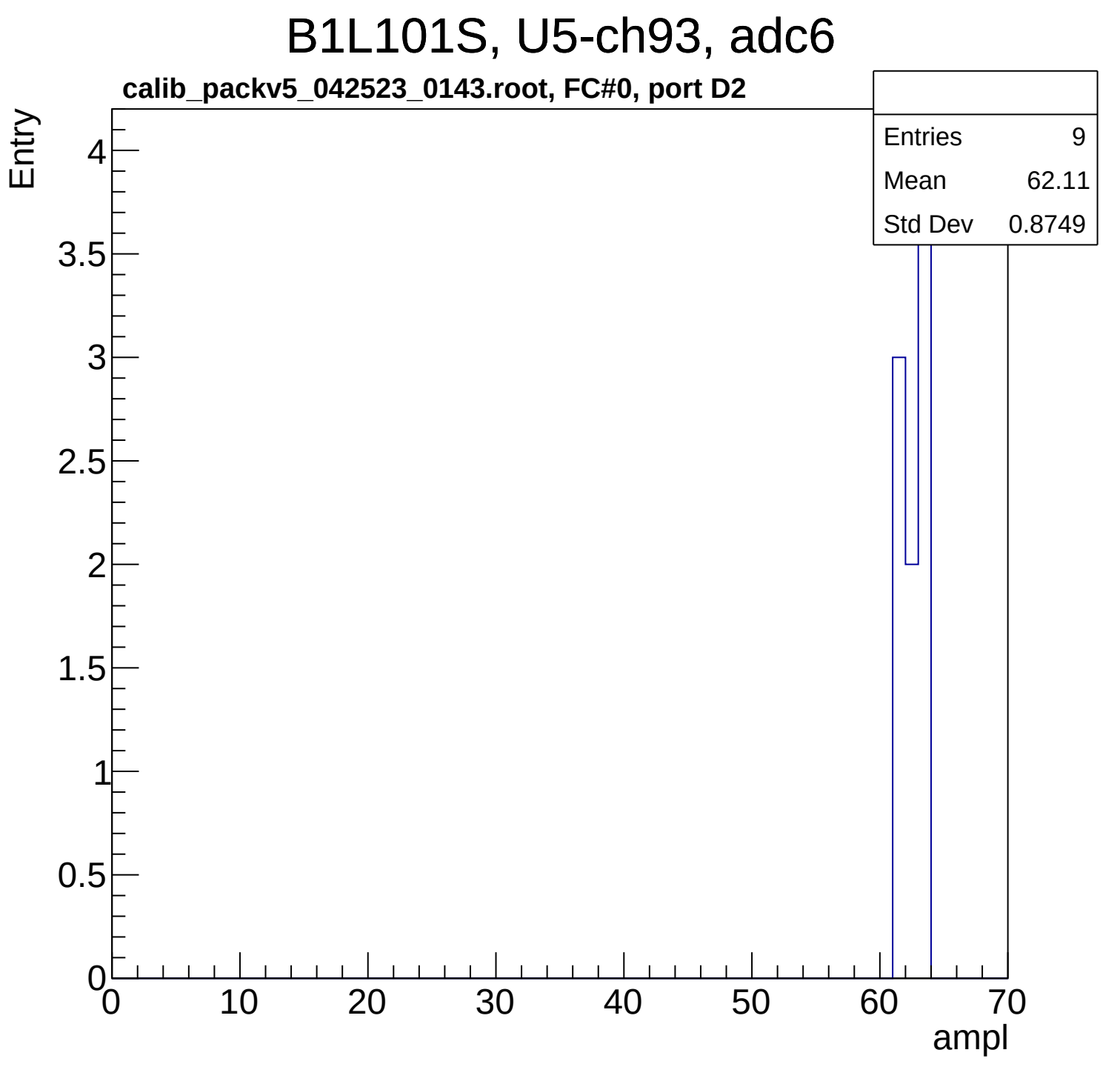
B1L101S, U5-ch93, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 62.11
Std Dev 0.8749
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
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60
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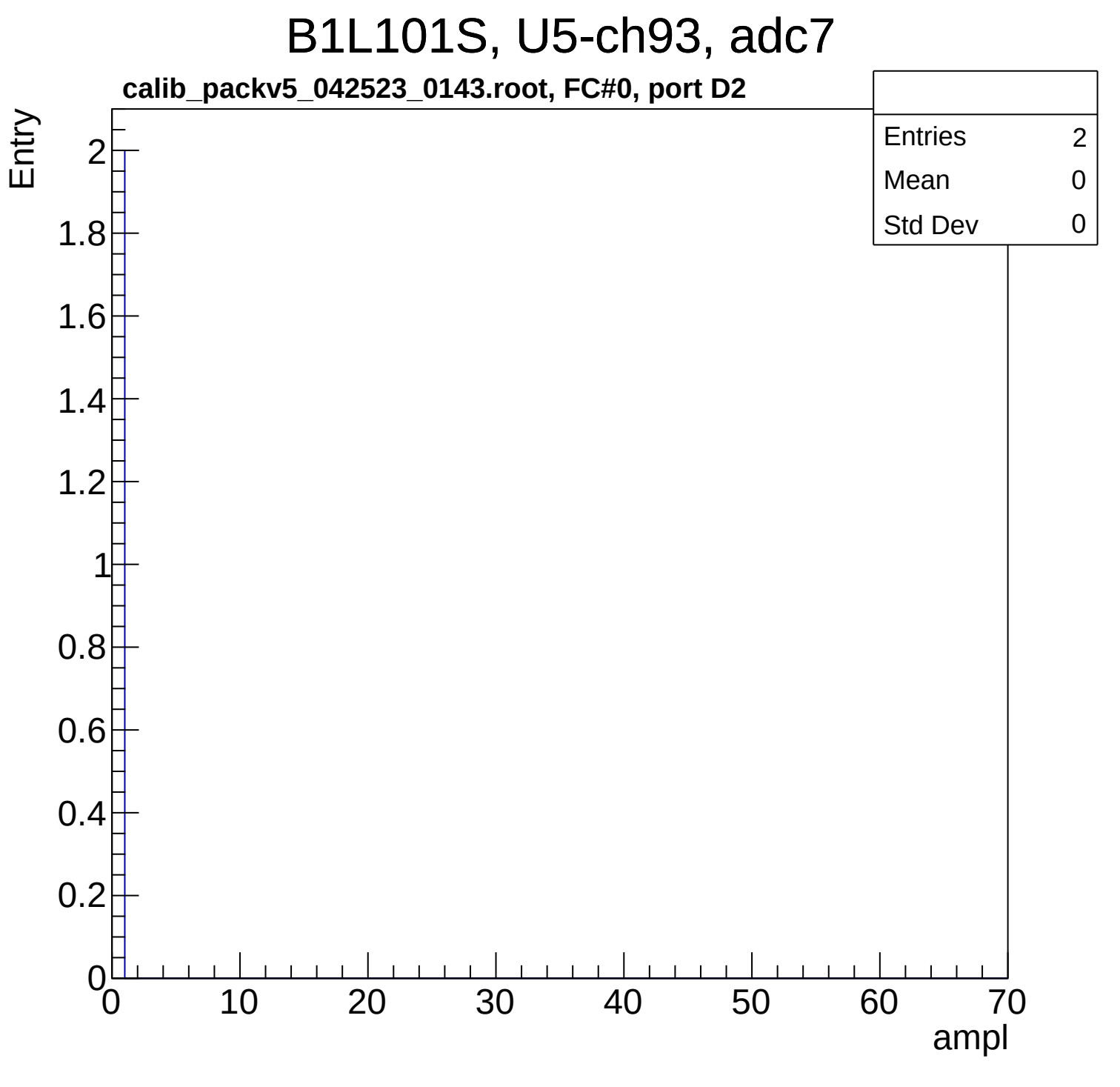
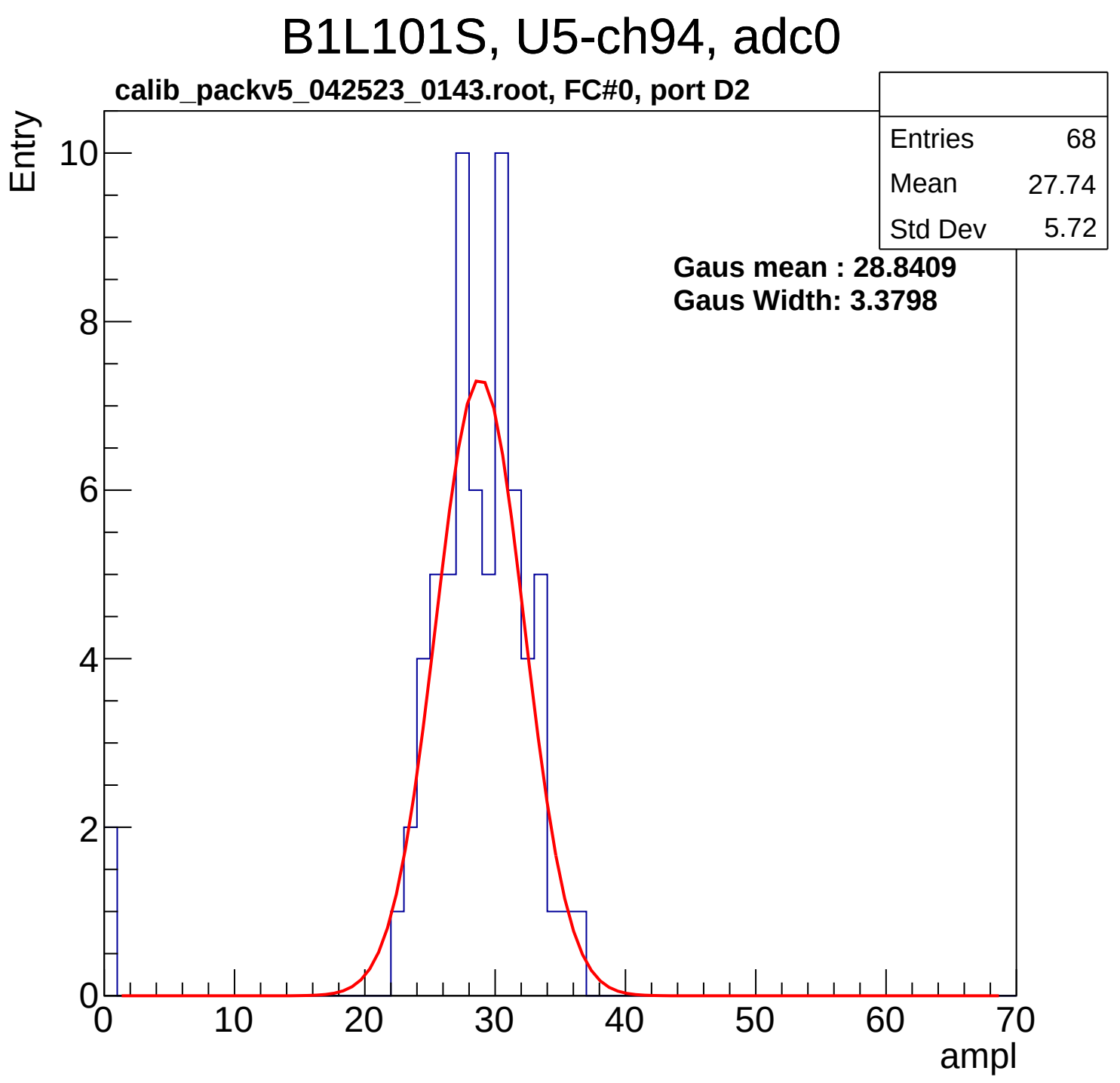
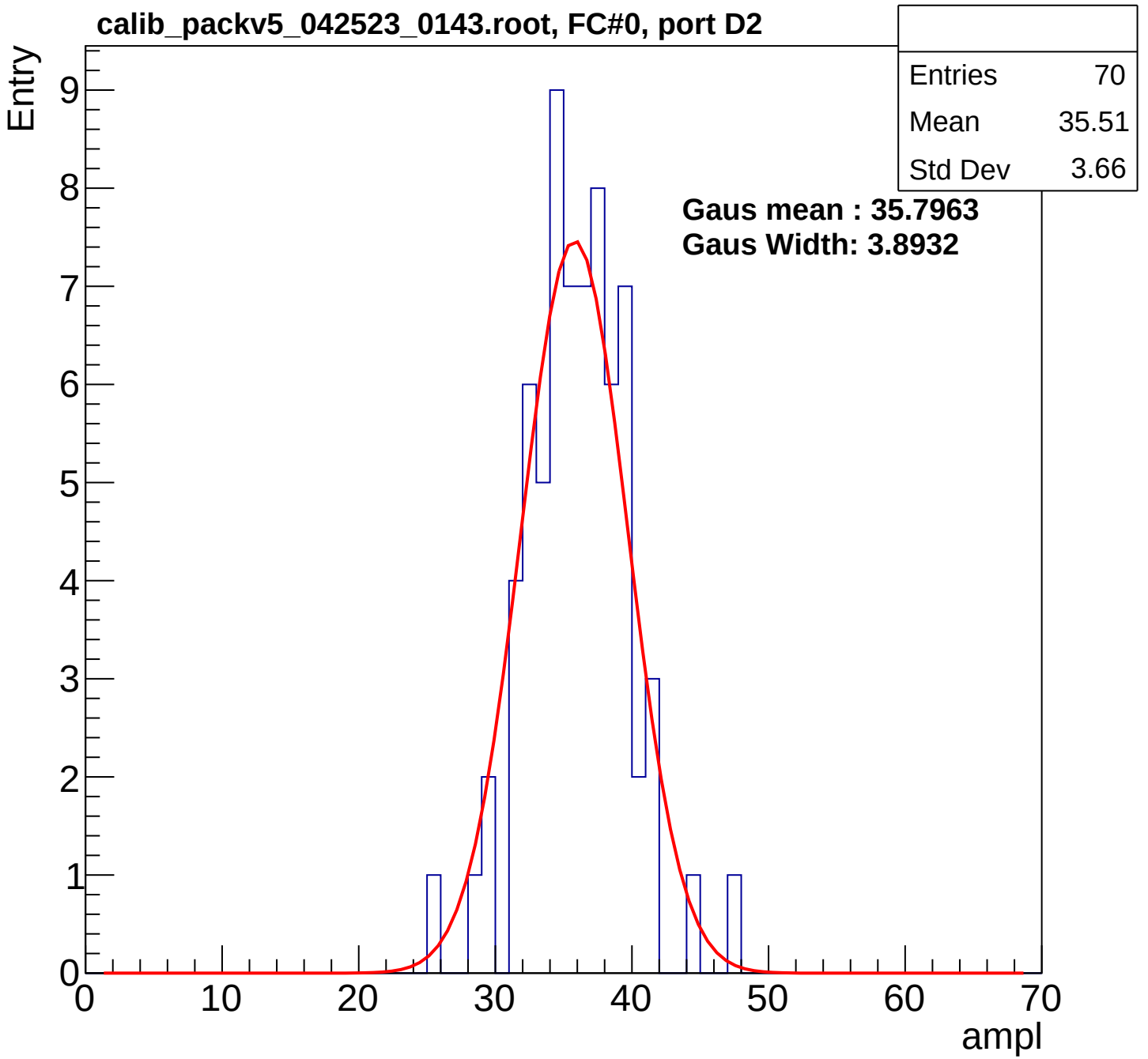
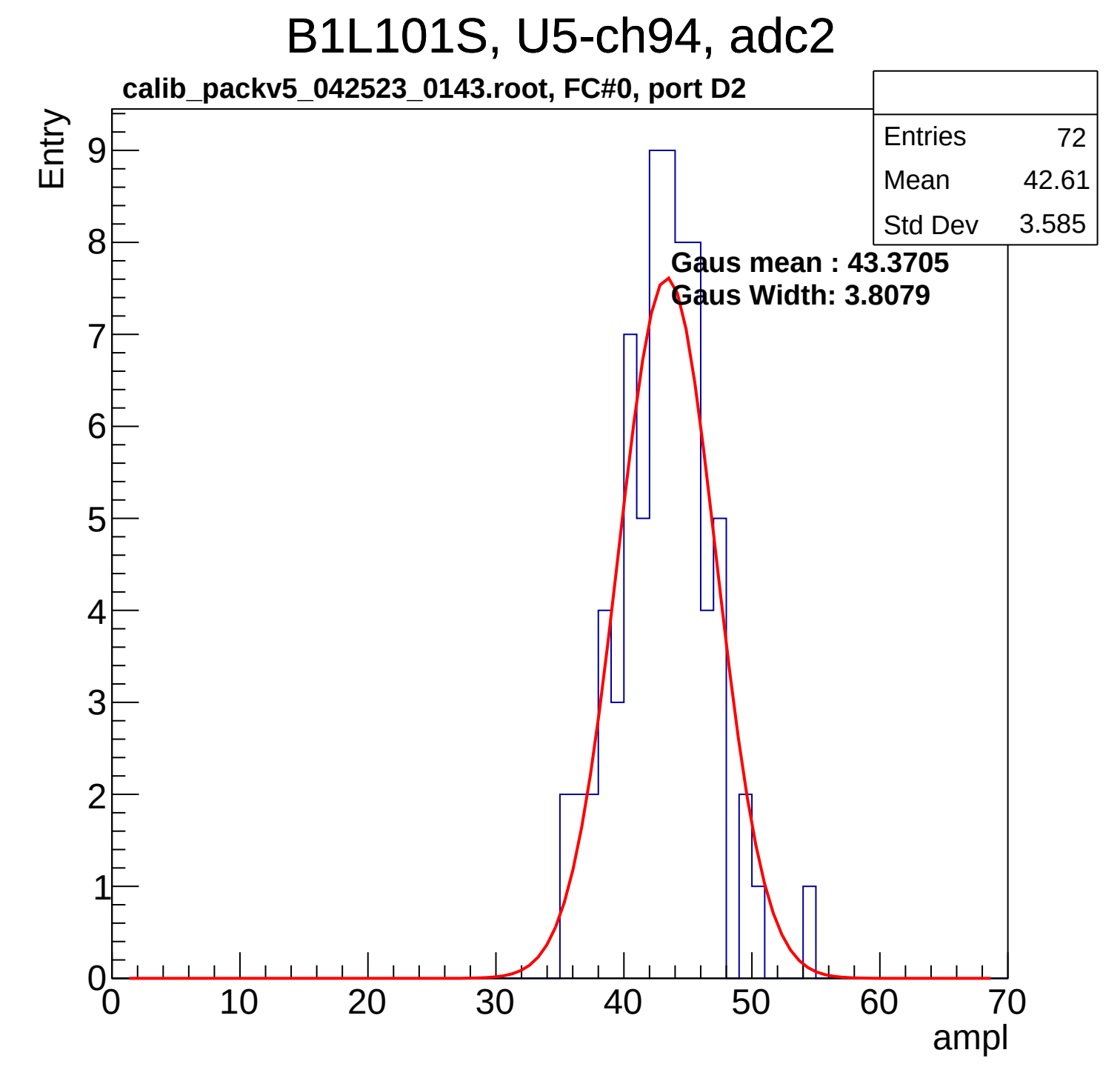
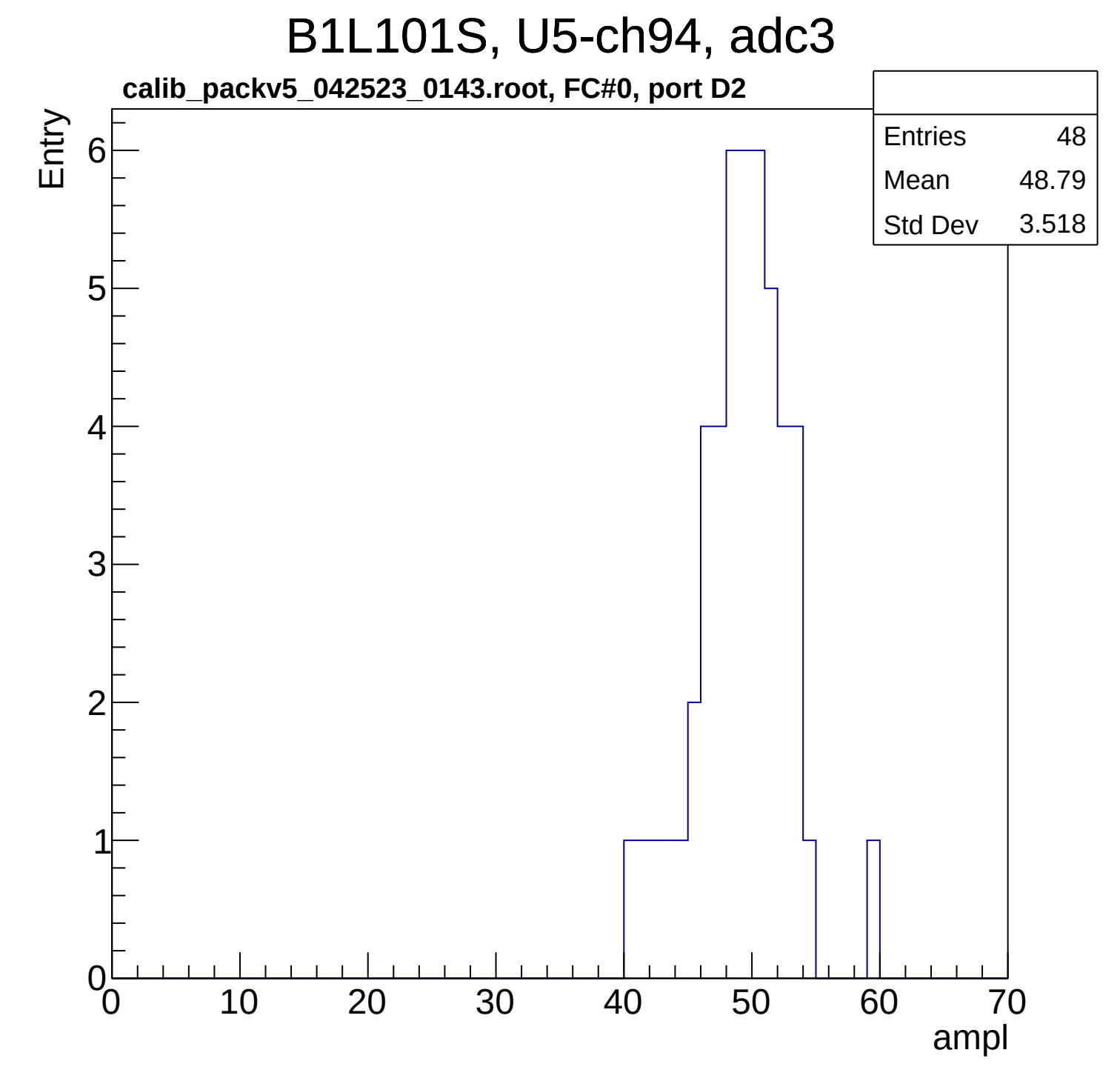
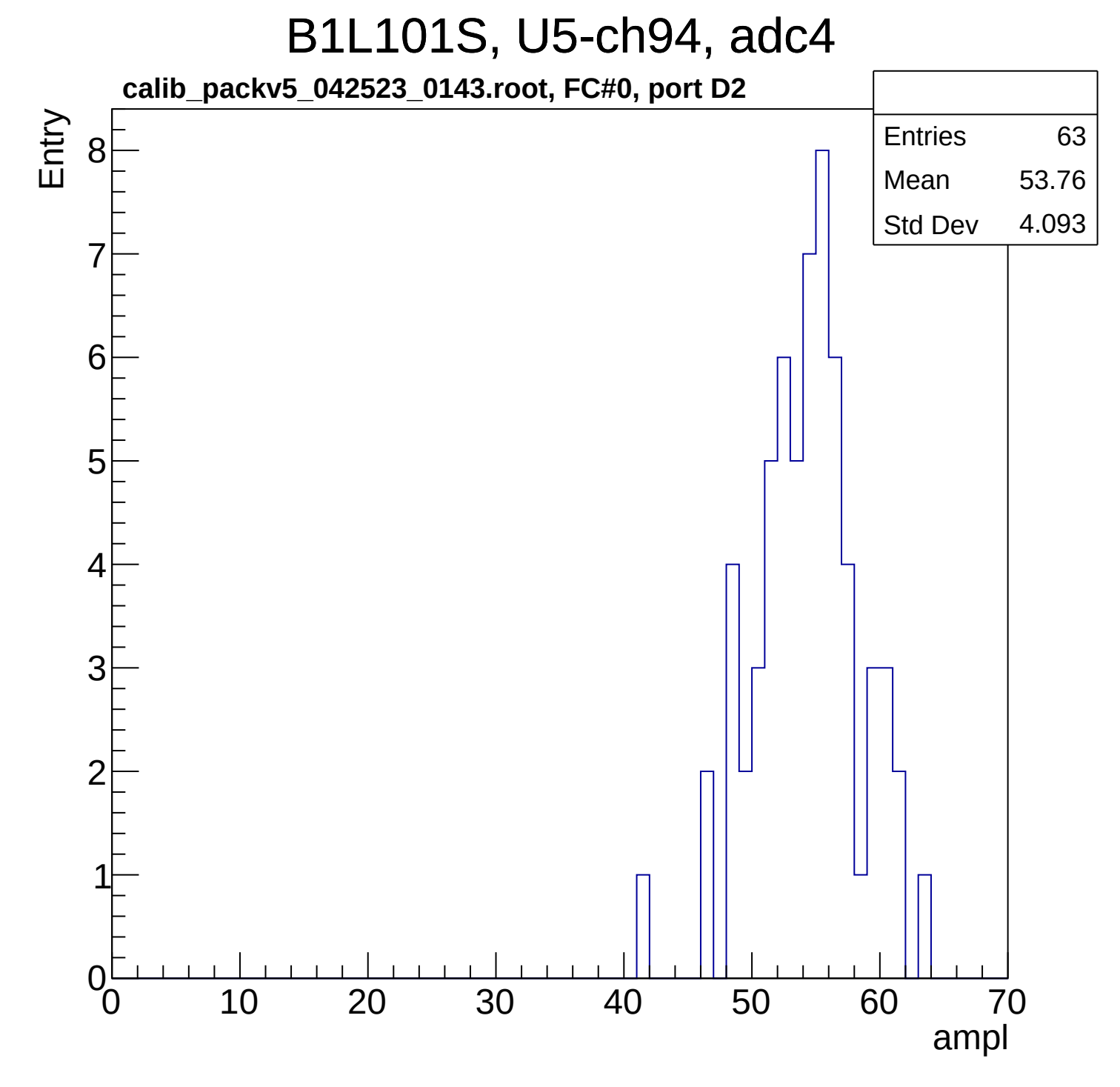

B1L101S, U5-ch93, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

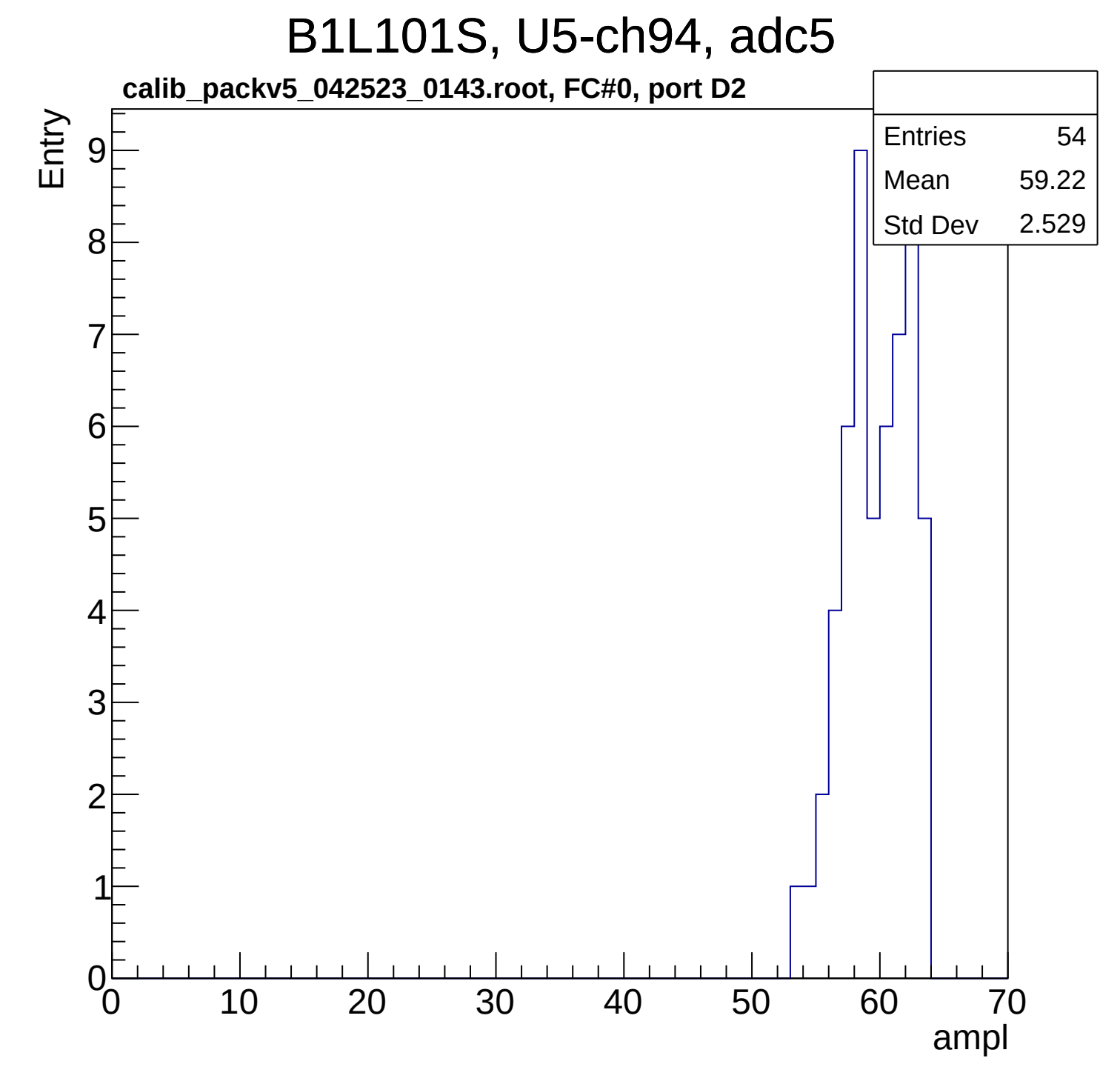

B1L101S, U5-ch94, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 27.74
Std Dev 5.72
Gaus mean : 28.8409
Gaus Width: 3.3798
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch94, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 35.51
Std Dev 3.66
Gaus mean : 35.7963
Gaus Width: 3.8932
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L101S, U5-ch94, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 42.61
Std Dev 3.585
Gaus mean : 43.3705
Gaus Width: 3.8079
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L101S, U5-ch94, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 48.79
Std Dev 3.518
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch94, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 53.76
Std Dev 4.093
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch94, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 59.22
Std Dev 2.529
Entry
ampl
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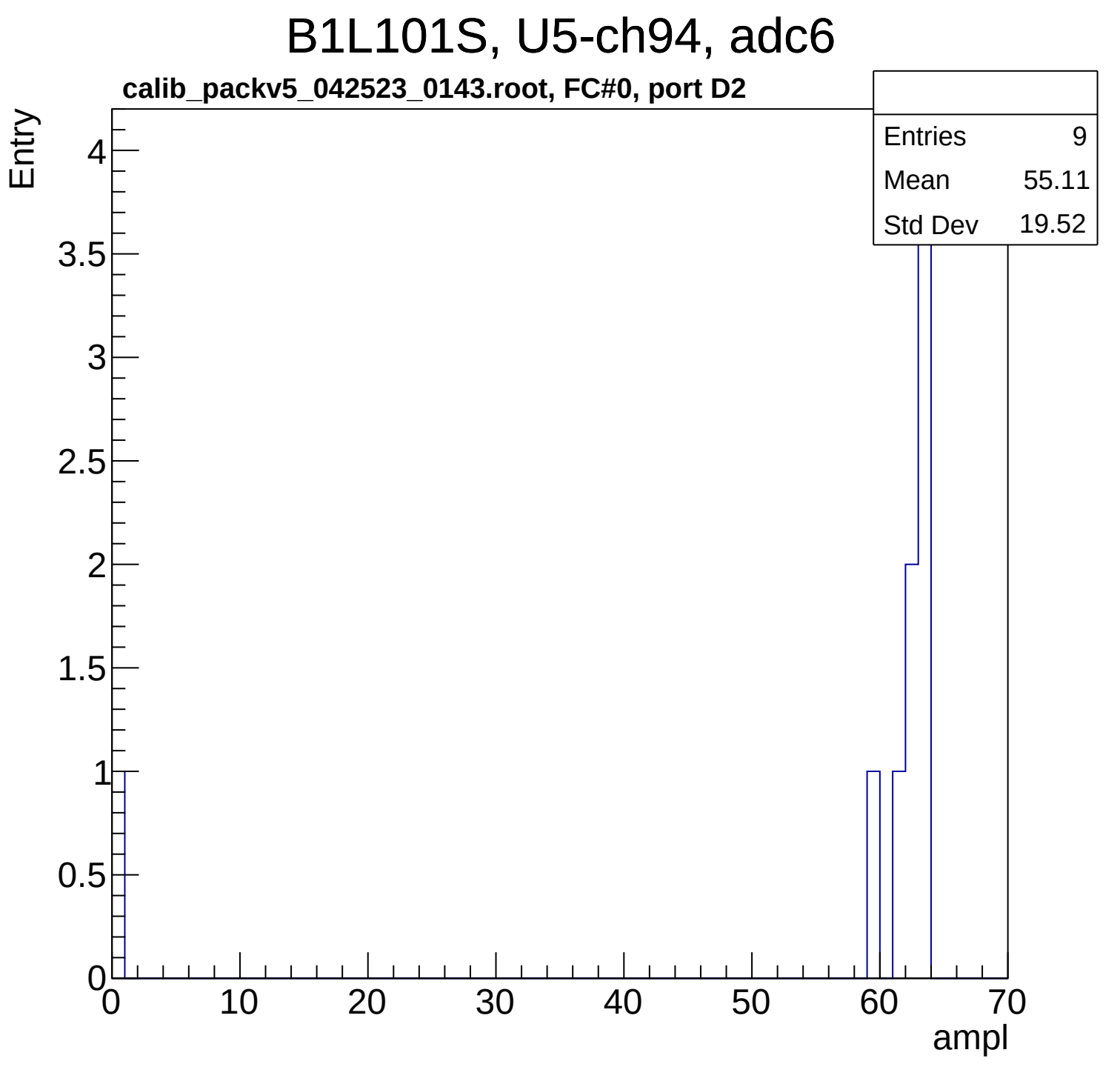
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L101S, U5-ch94, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 55.11
Std Dev 19.52
Entry
ampl
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1
1.5
2
2.5
3
3.5
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0
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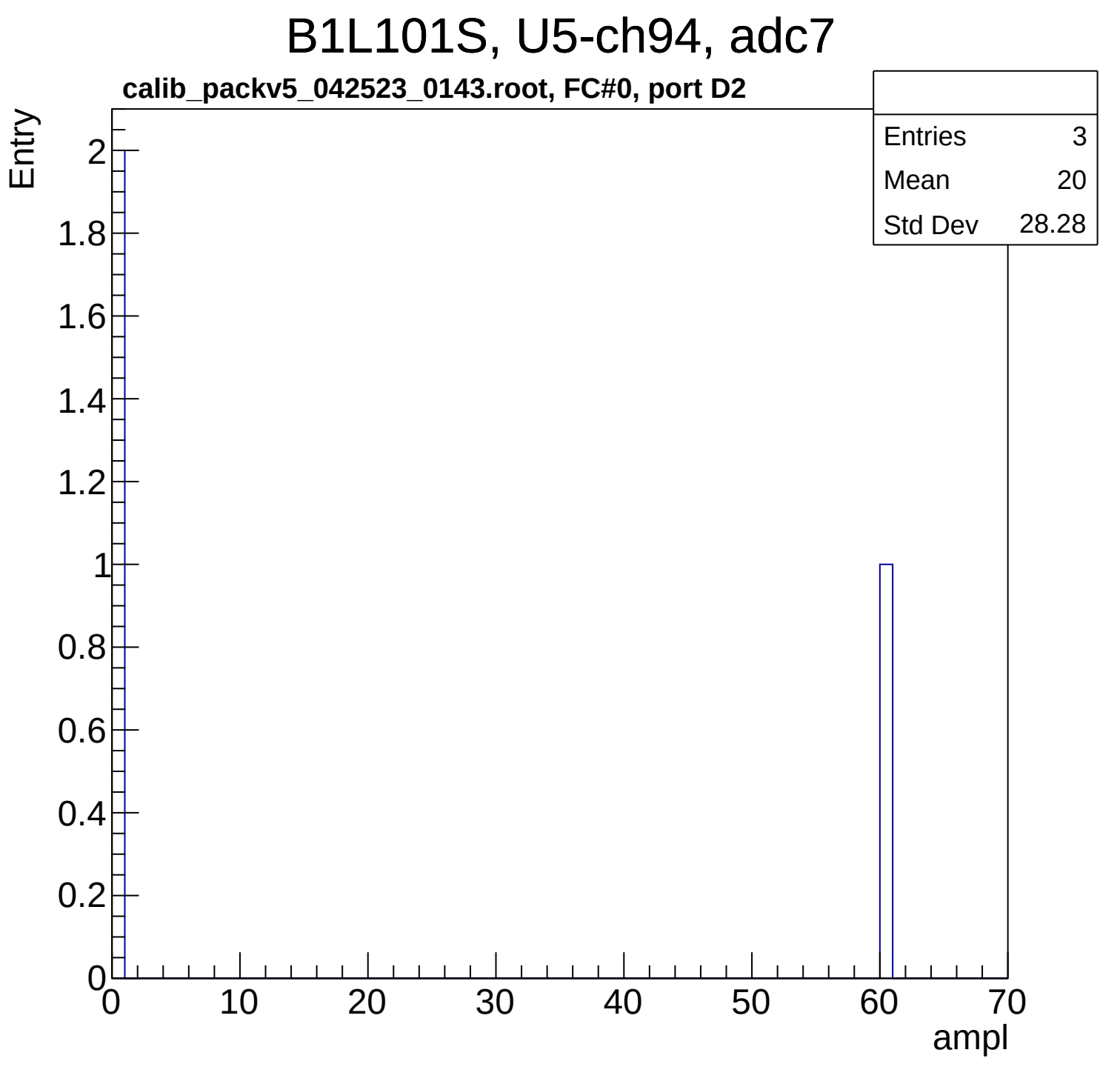
B1L101S, U5-ch94, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 20
Std Dev 28.28
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
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60
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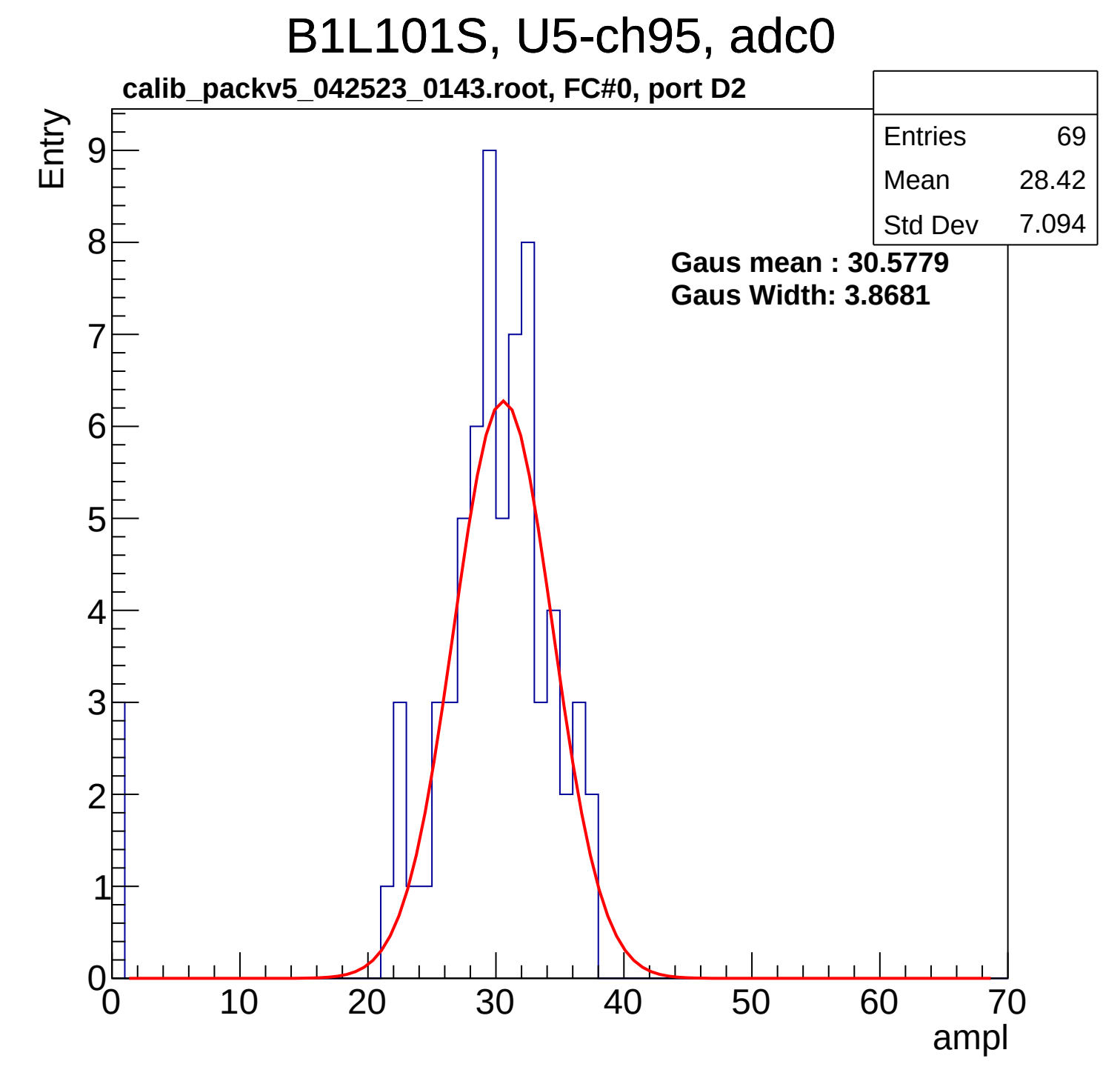
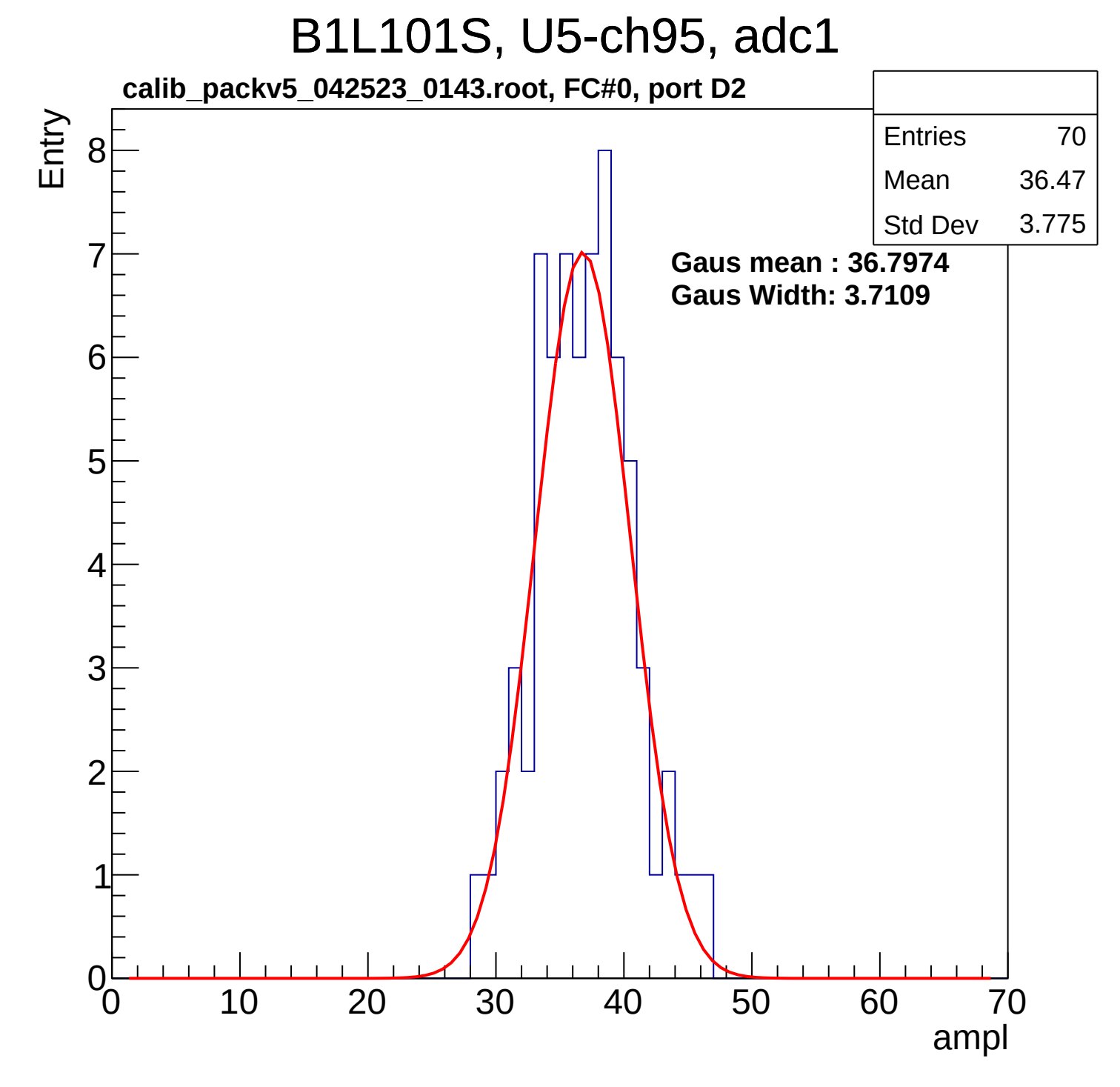
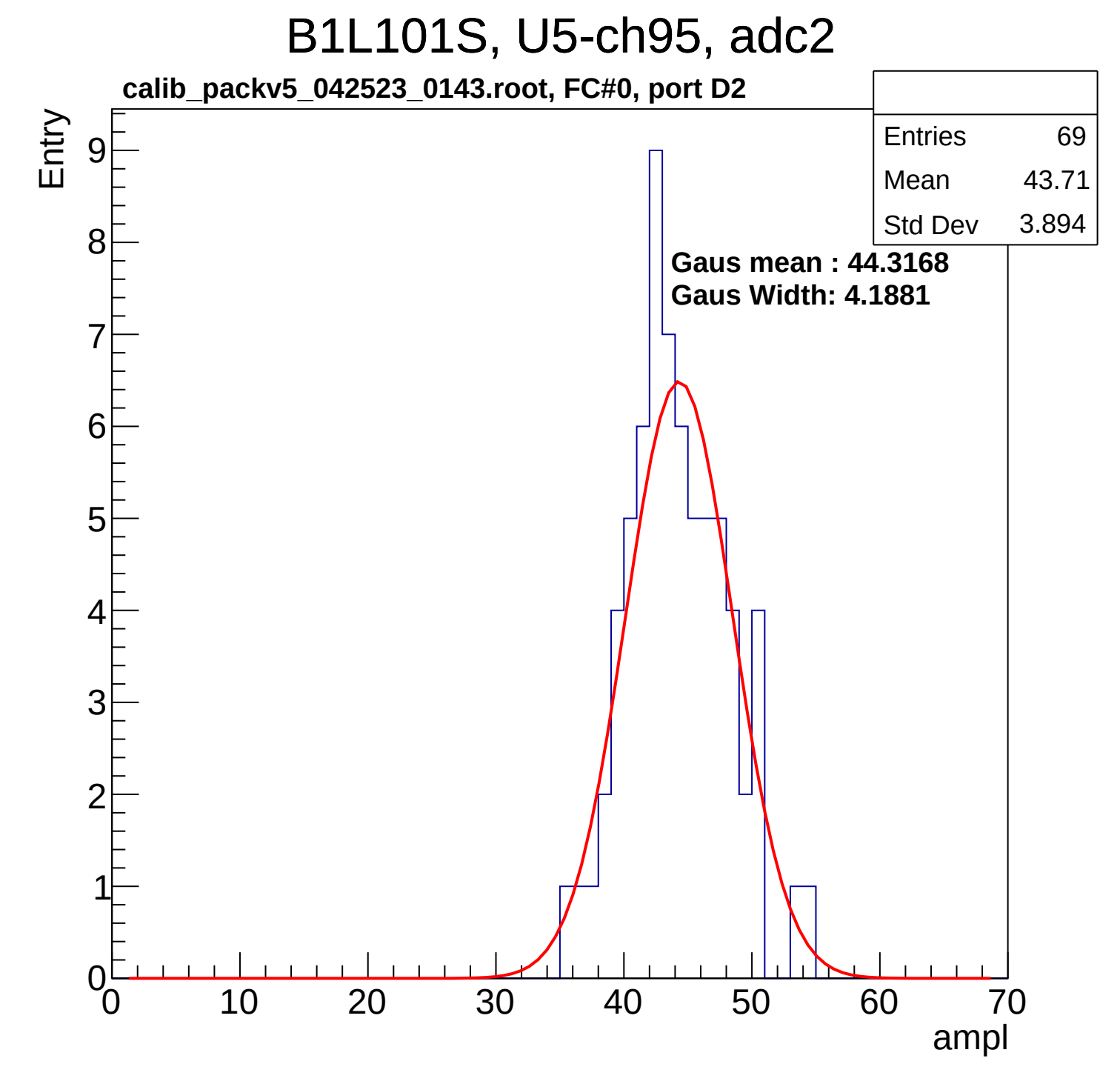

B1L101S, U5-ch95, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 28.42
Std Dev 7.094
Gaus mean : 30.5779
Gaus Width: 3.8681
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch95, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 36.47
Std Dev 3.775
Gaus mean : 36.7974
Gaus Width: 3.7109
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch95, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 43.71
Std Dev 3.894
Gaus mean : 44.3168
Gaus Width: 4.1881
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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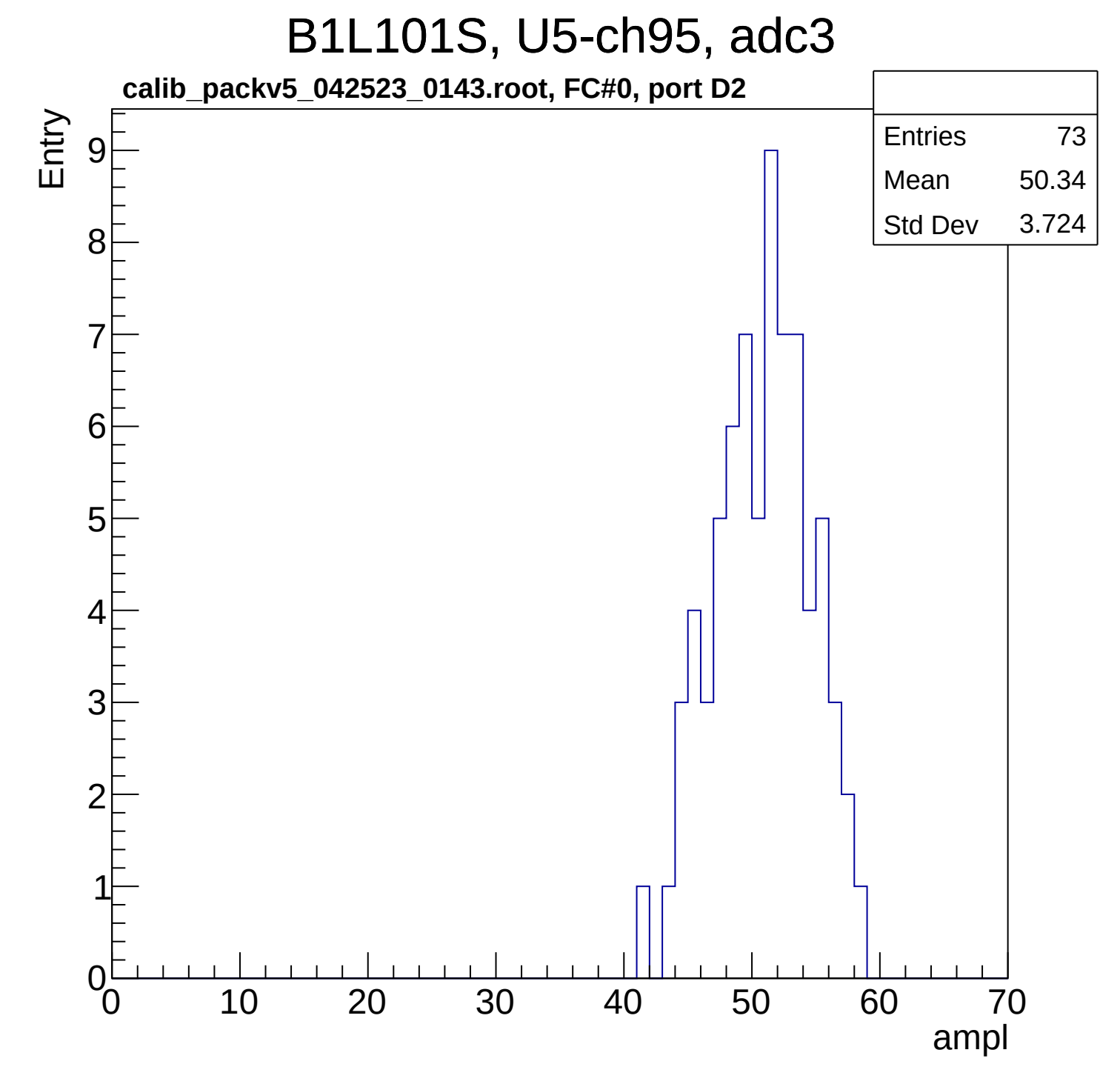
B1L101S, U5-ch95, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 50.34
Std Dev 3.724
Entry
ampl
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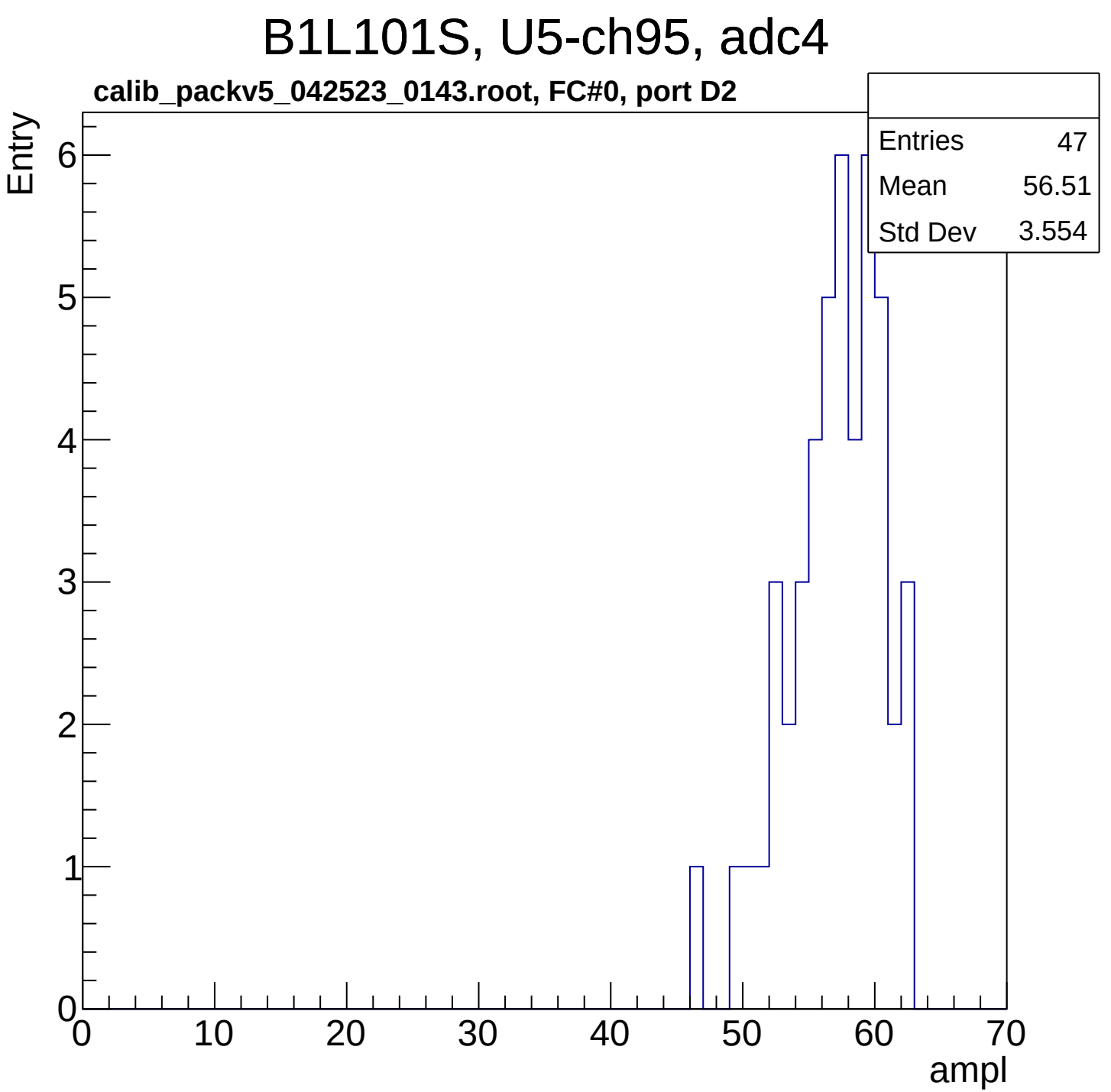
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch95, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 56.51
Std Dev 3.554
Entry
ampl
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1
2
3
4
5
6
0
10
20
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40
50
60
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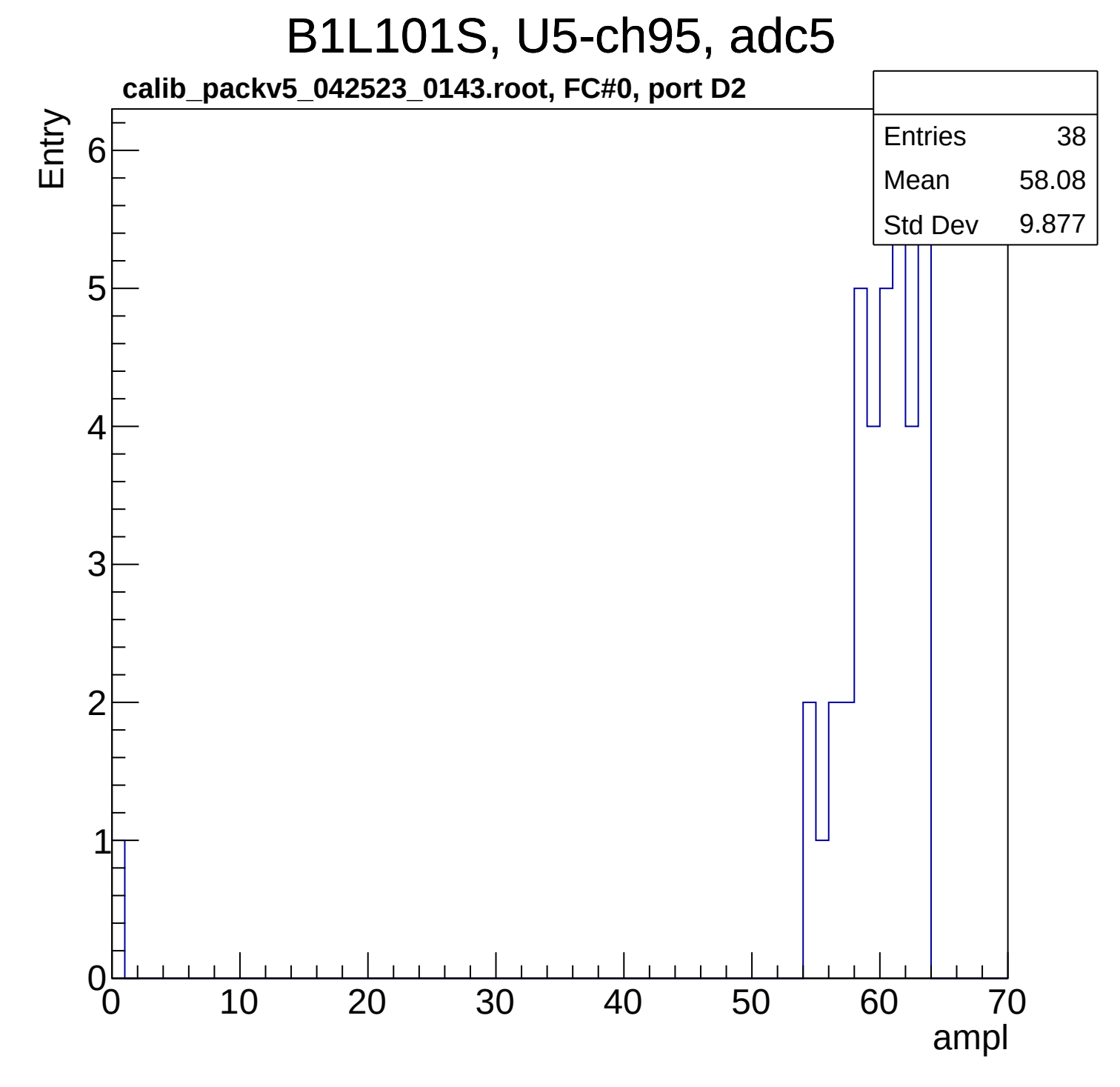
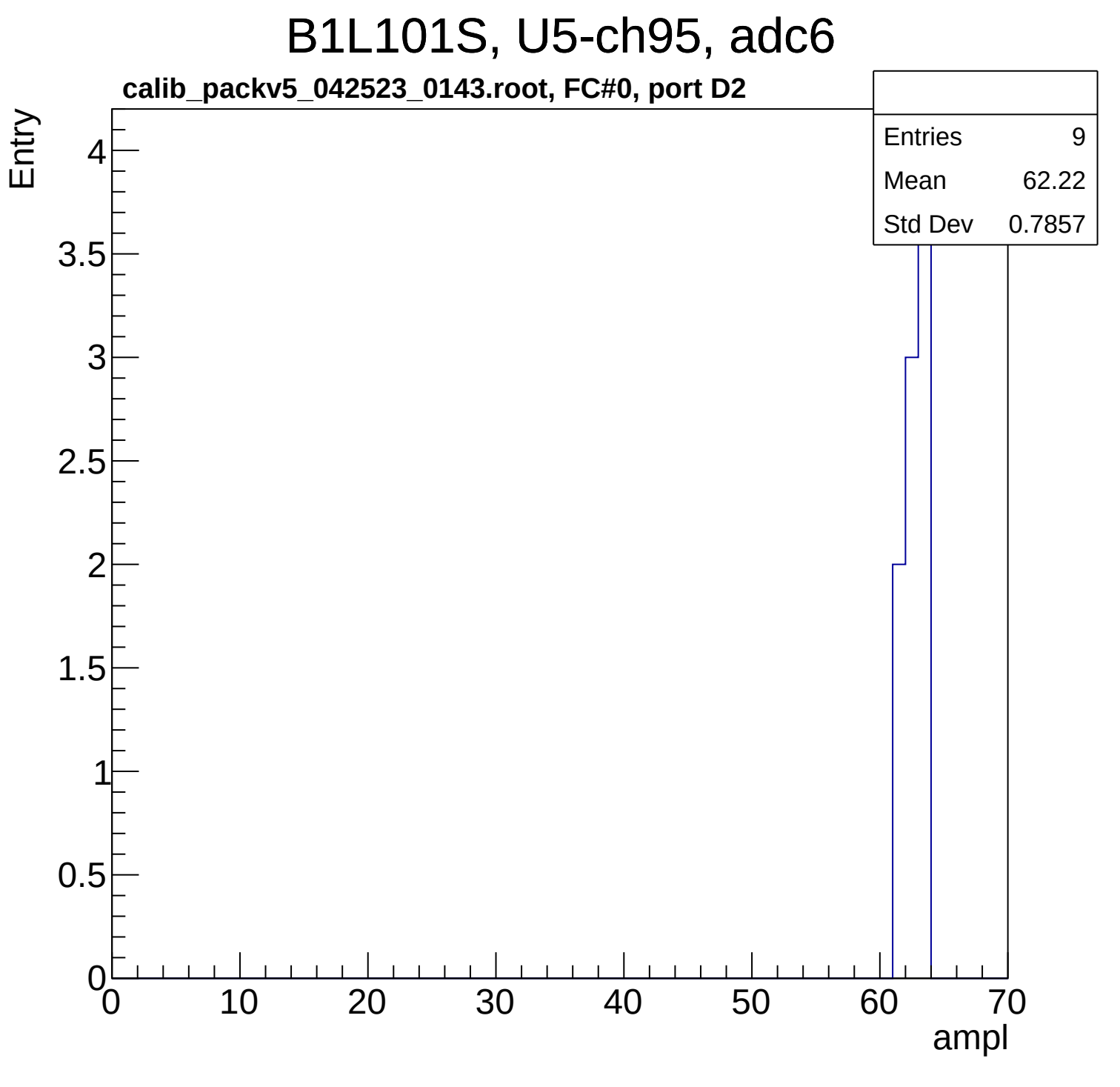

B1L101S, U5-ch95, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 38
Mean 58.08
Std Dev 9.877
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L101S, U5-ch95, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 62.22
Std Dev 0.7857
Entry
ampl
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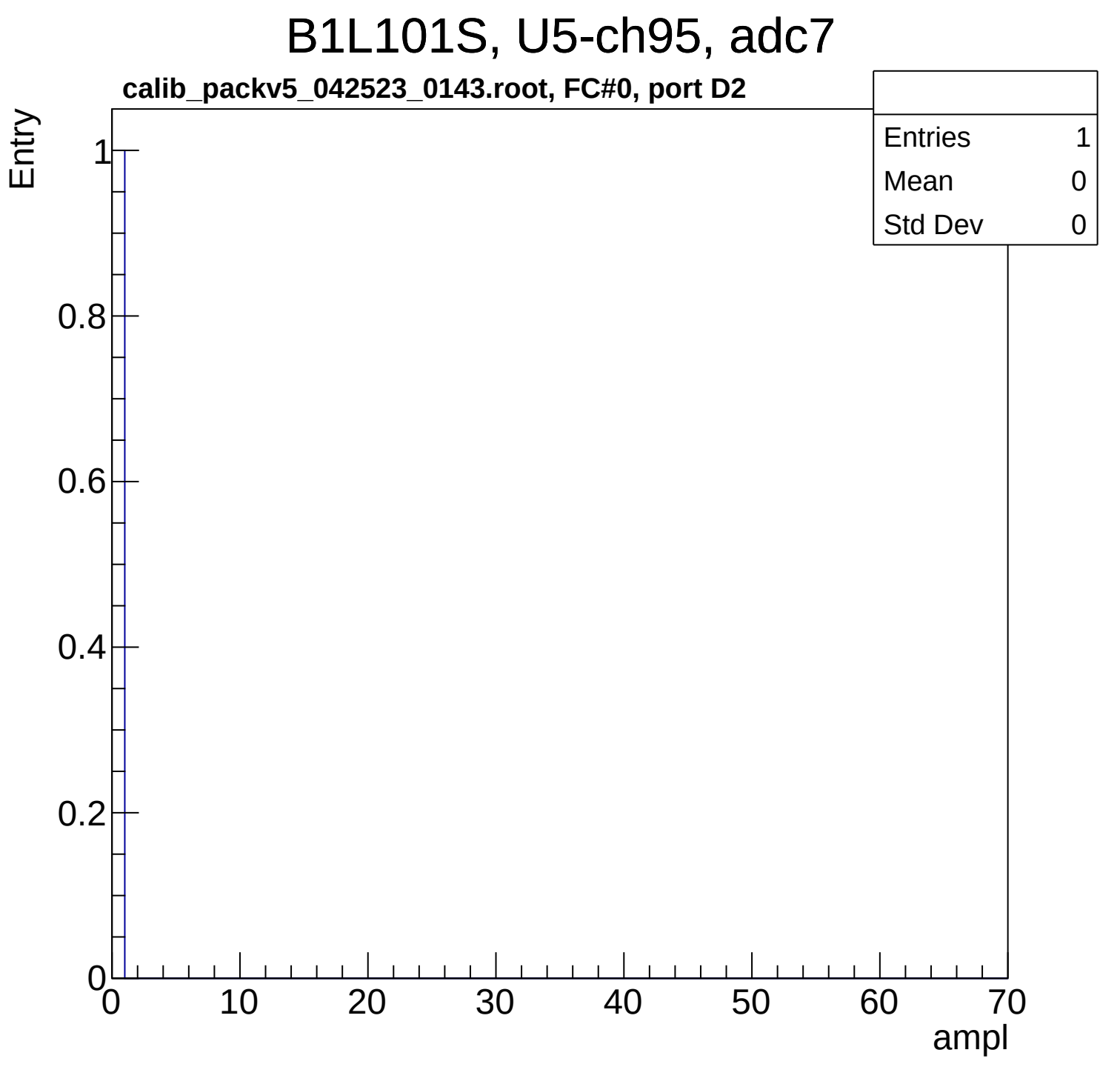
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L101S, U5-ch95, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
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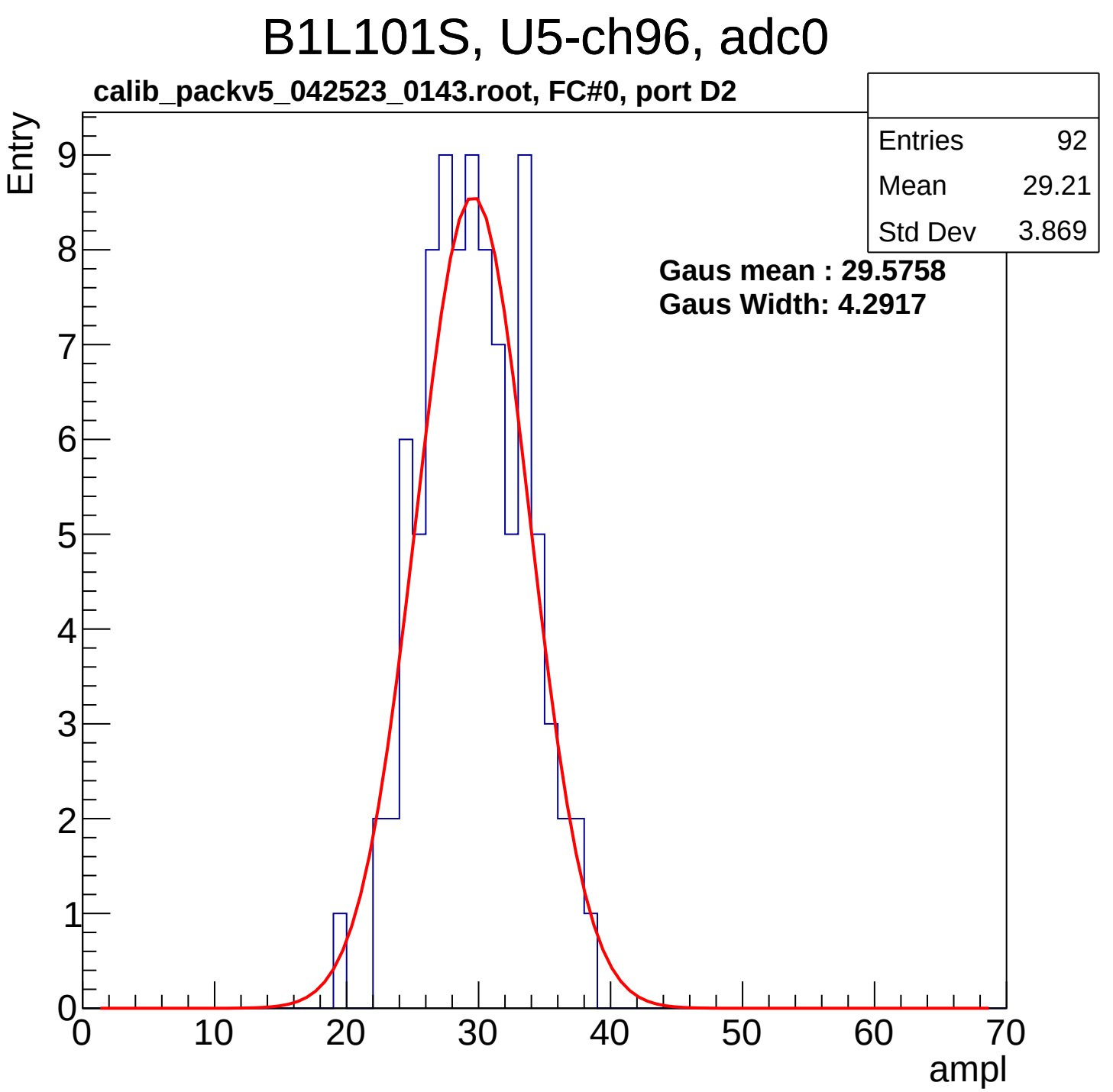
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch96, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 92
Mean 29.21
Std Dev 3.869
Gaus mean : 29.5758
Gaus Width: 4.2917
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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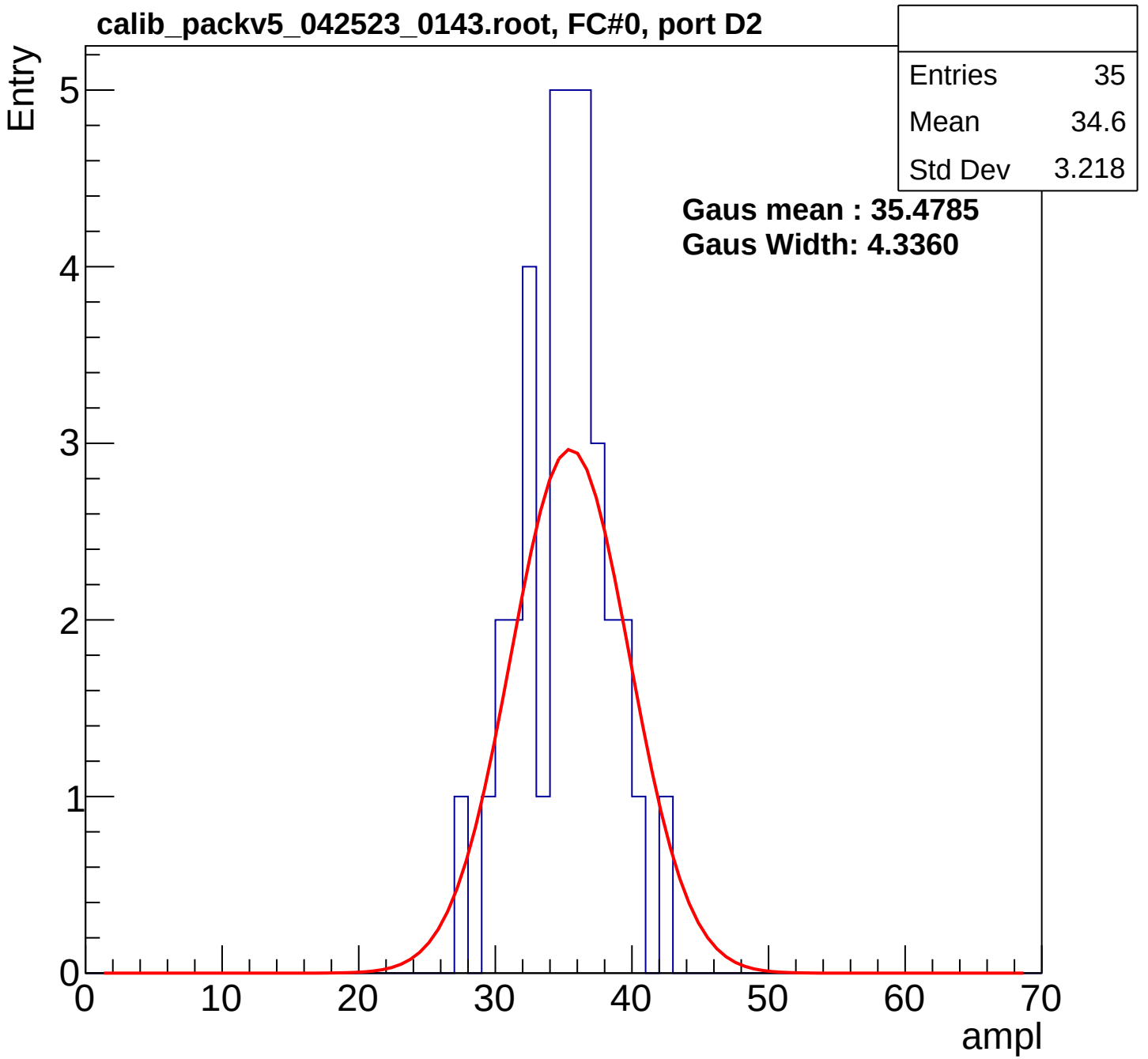
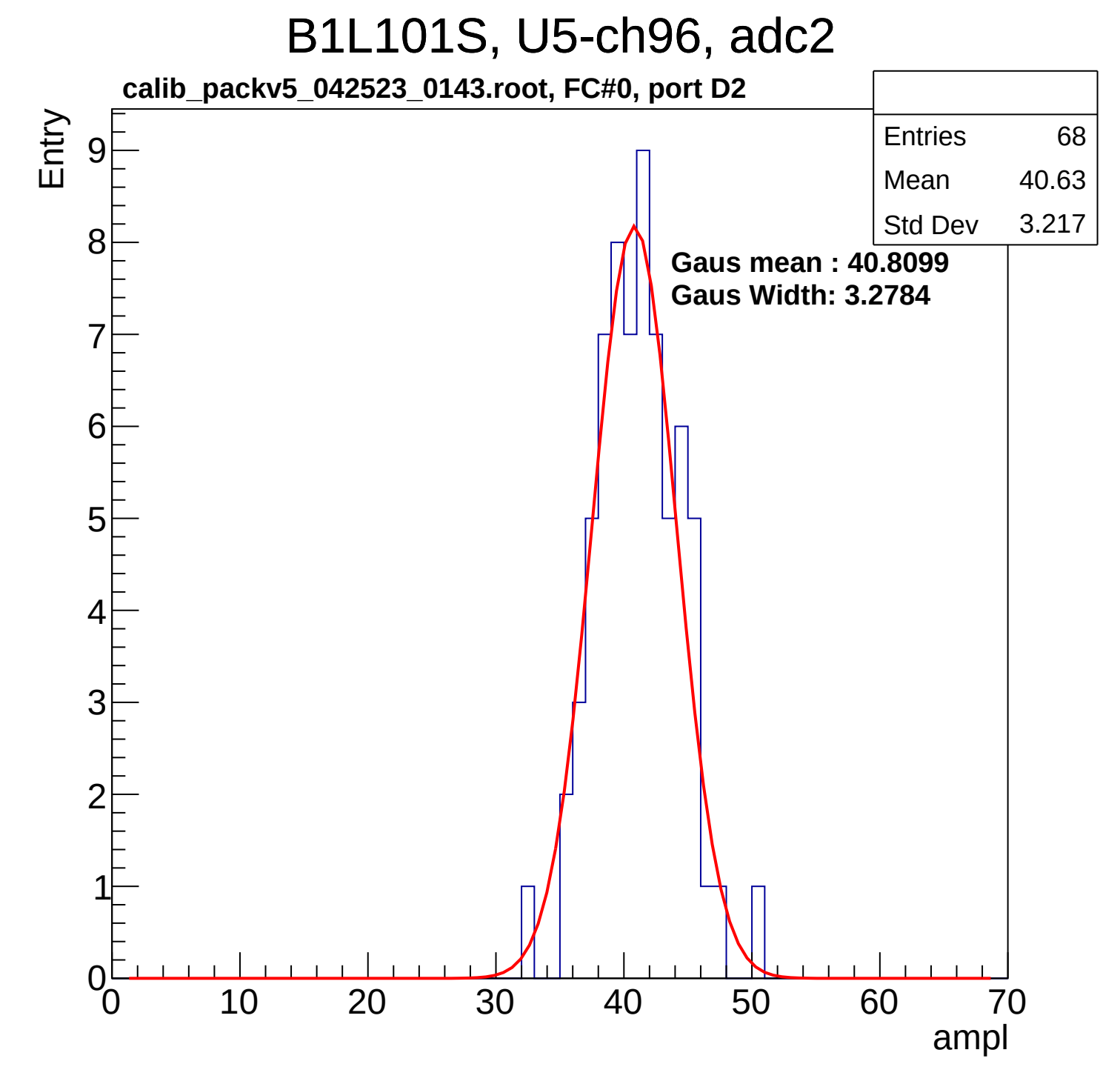
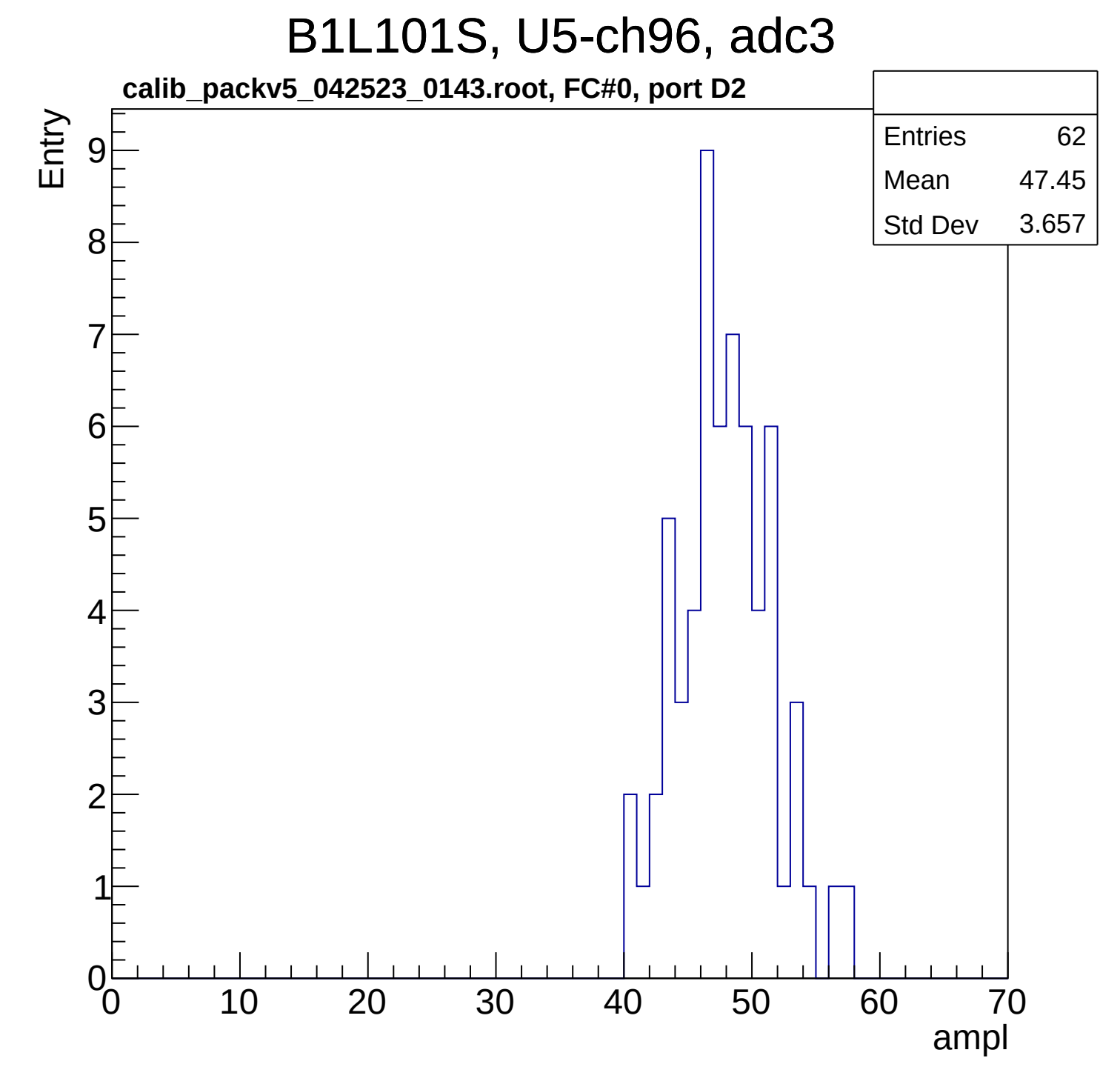

B1L101S, U5-ch96, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 35
Mean 34.6
Std Dev 3.218
Gaus mean : 35.4785
Gaus Width: 4.3360
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L101S, U5-ch96, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 40.63
Std Dev 3.217
Gaus mean : 40.8099
Gaus Width: 3.2784
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch96, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 47.45
Std Dev 3.657
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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60
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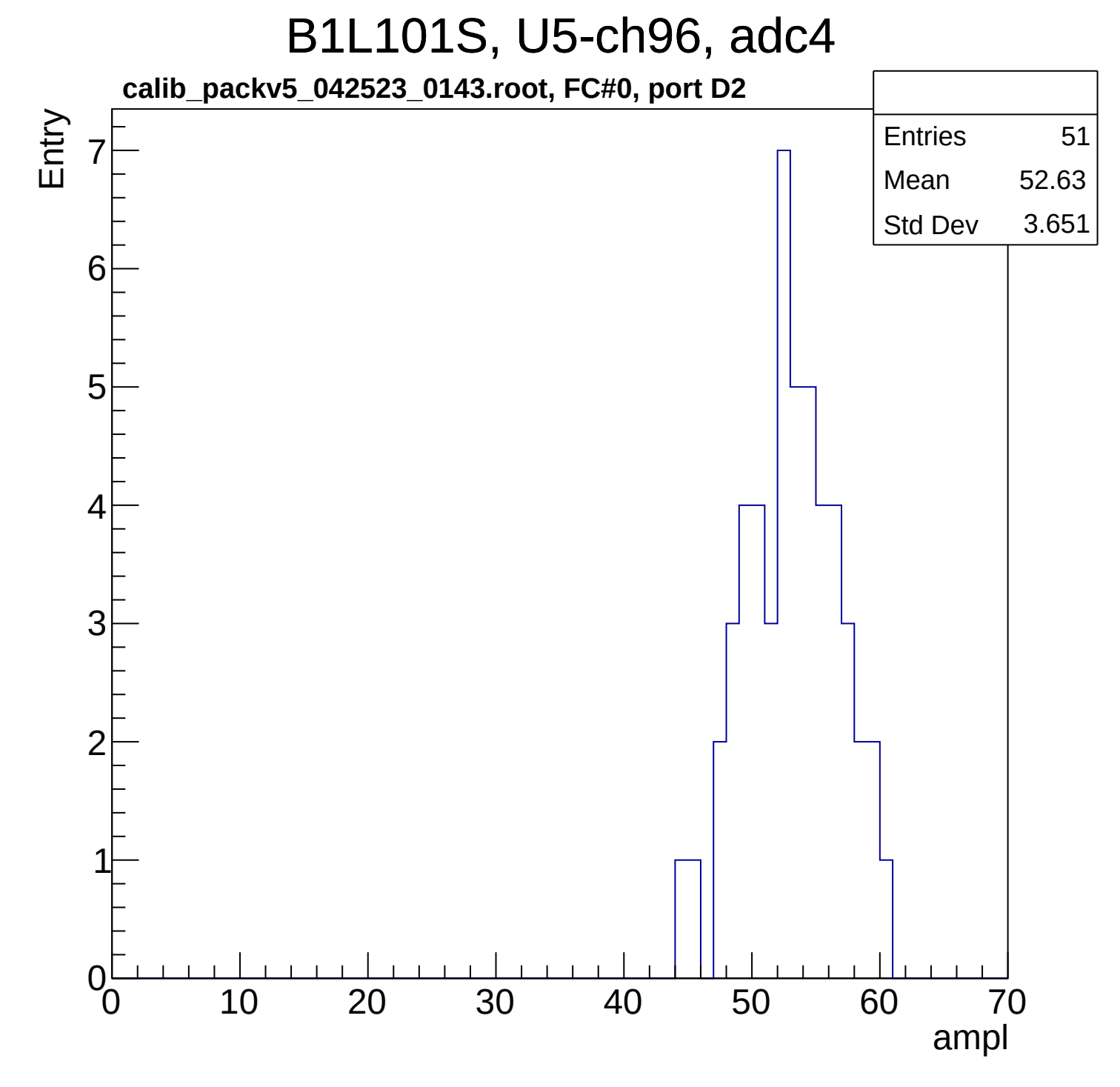
B1L101S, U5-ch96, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 52.63
Std Dev 3.651
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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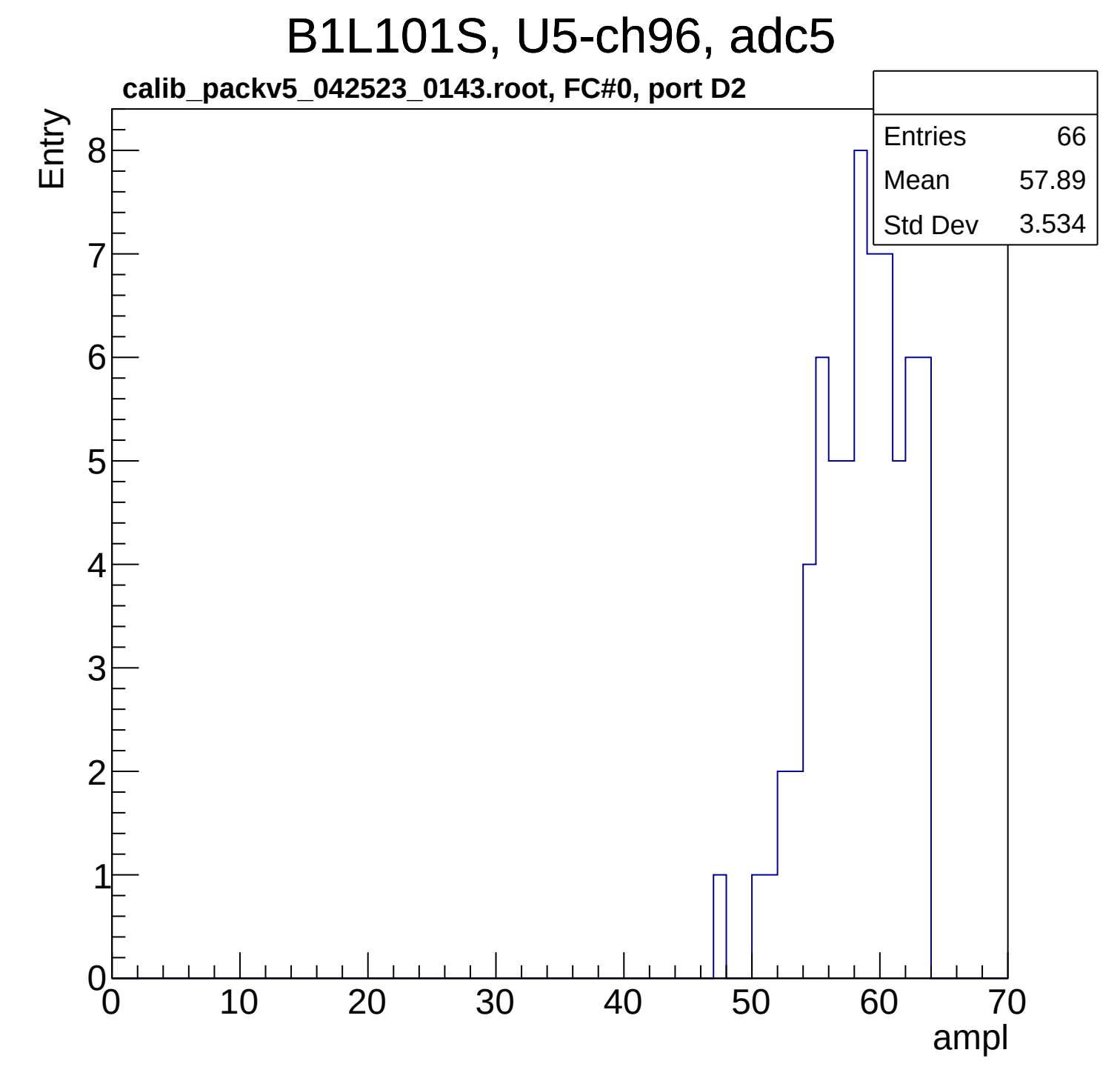
B1L101S, U5-ch96, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 57.89
Std Dev 3.534
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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40
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60
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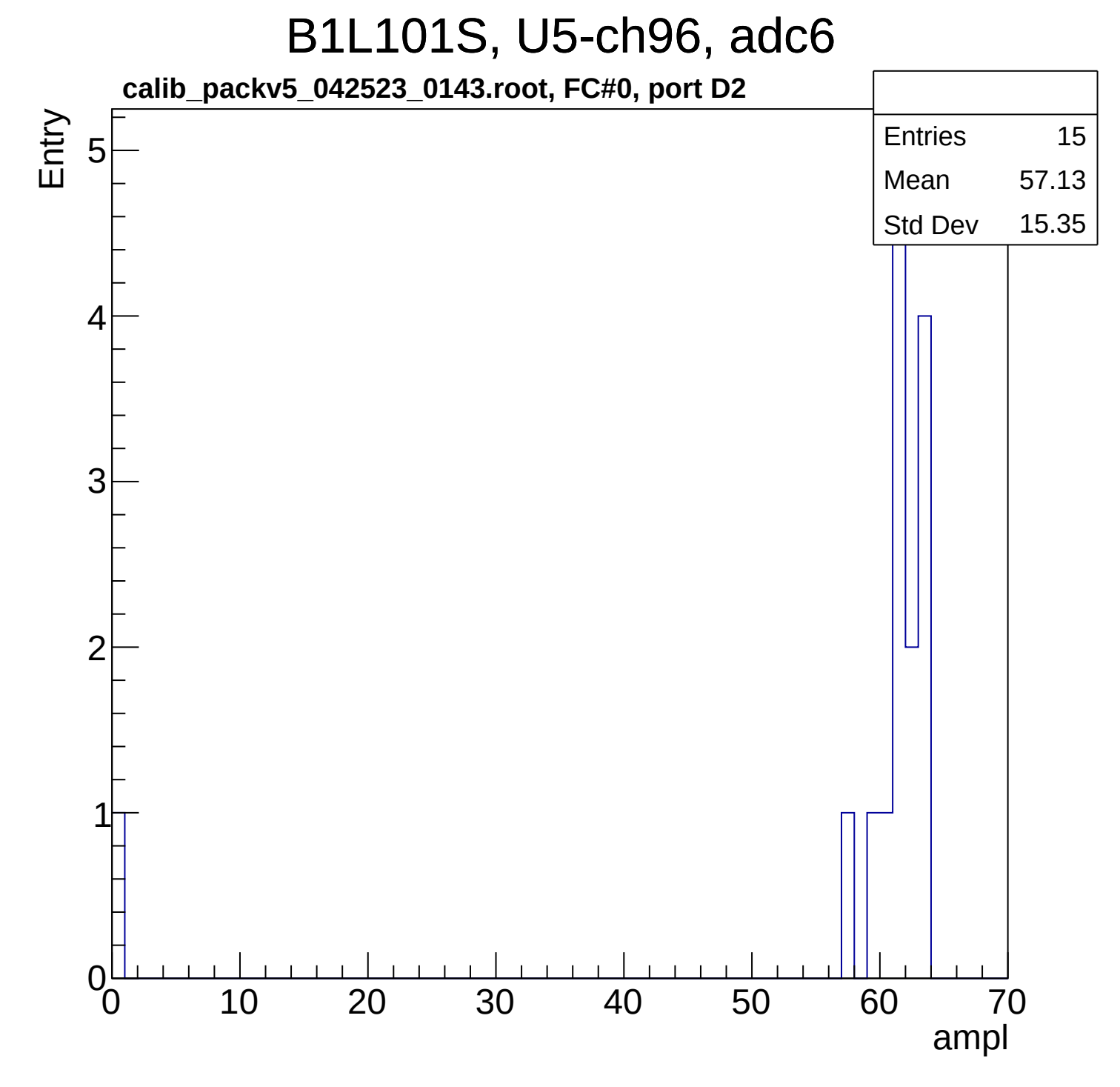
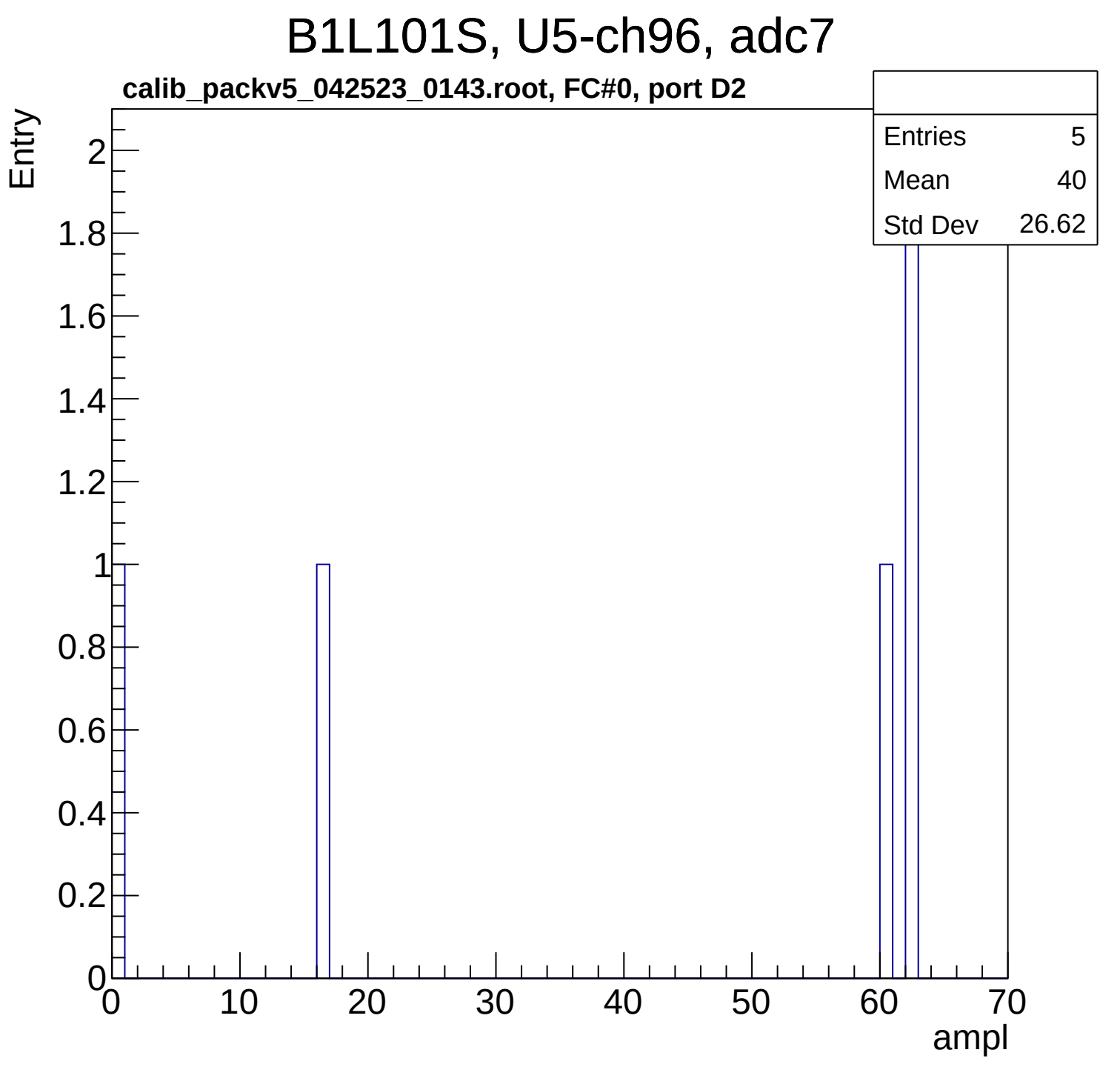

B1L101S, U5-ch96, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 15
Mean 57.13
Std Dev 15.35
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L101S, U5-ch96, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 40
Std Dev 26.62
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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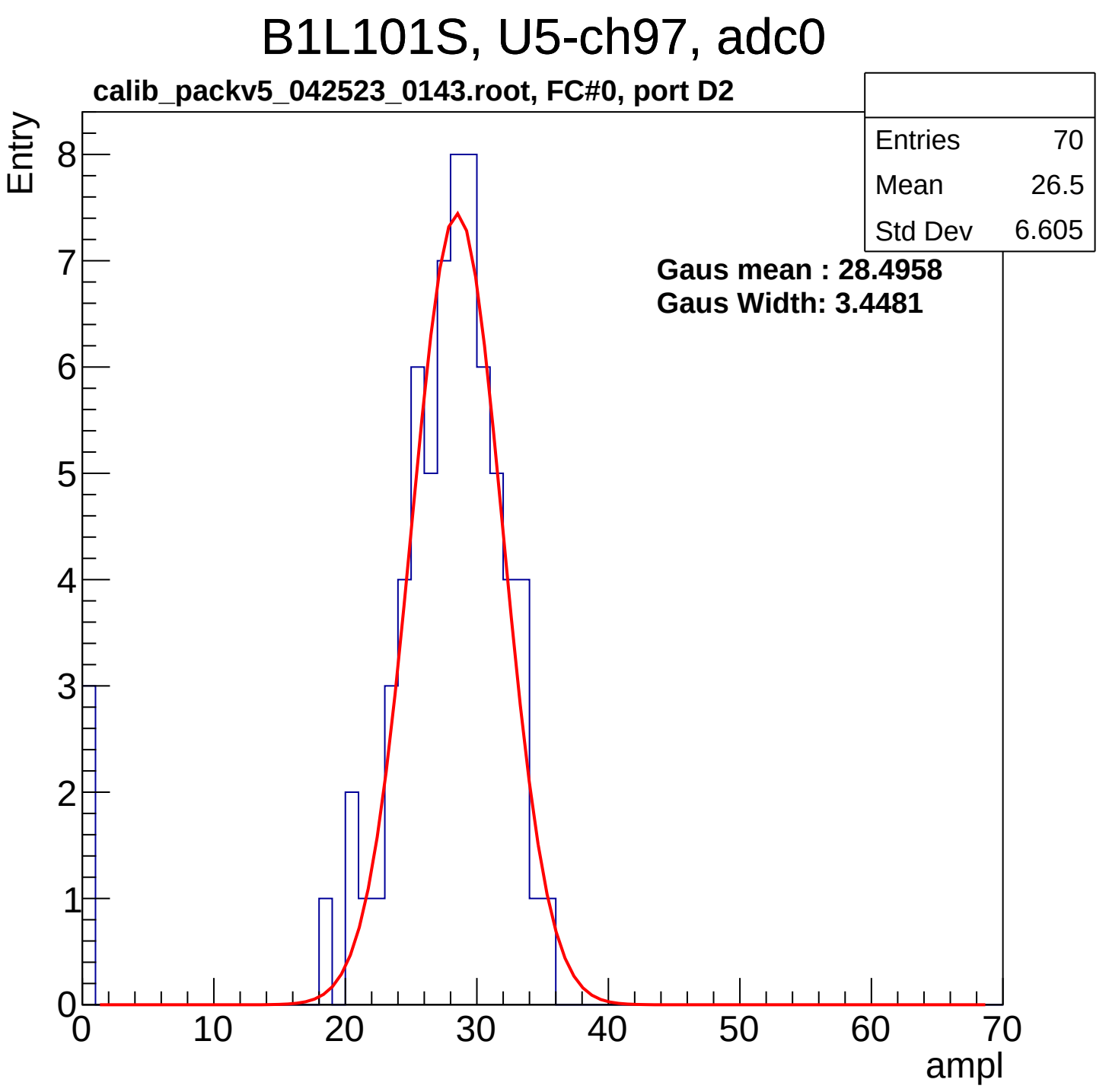
B1L101S, U5-ch97, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 26.5
Std Dev 6.605
Gaus mean : 28.4958
Gaus Width: 3.4481
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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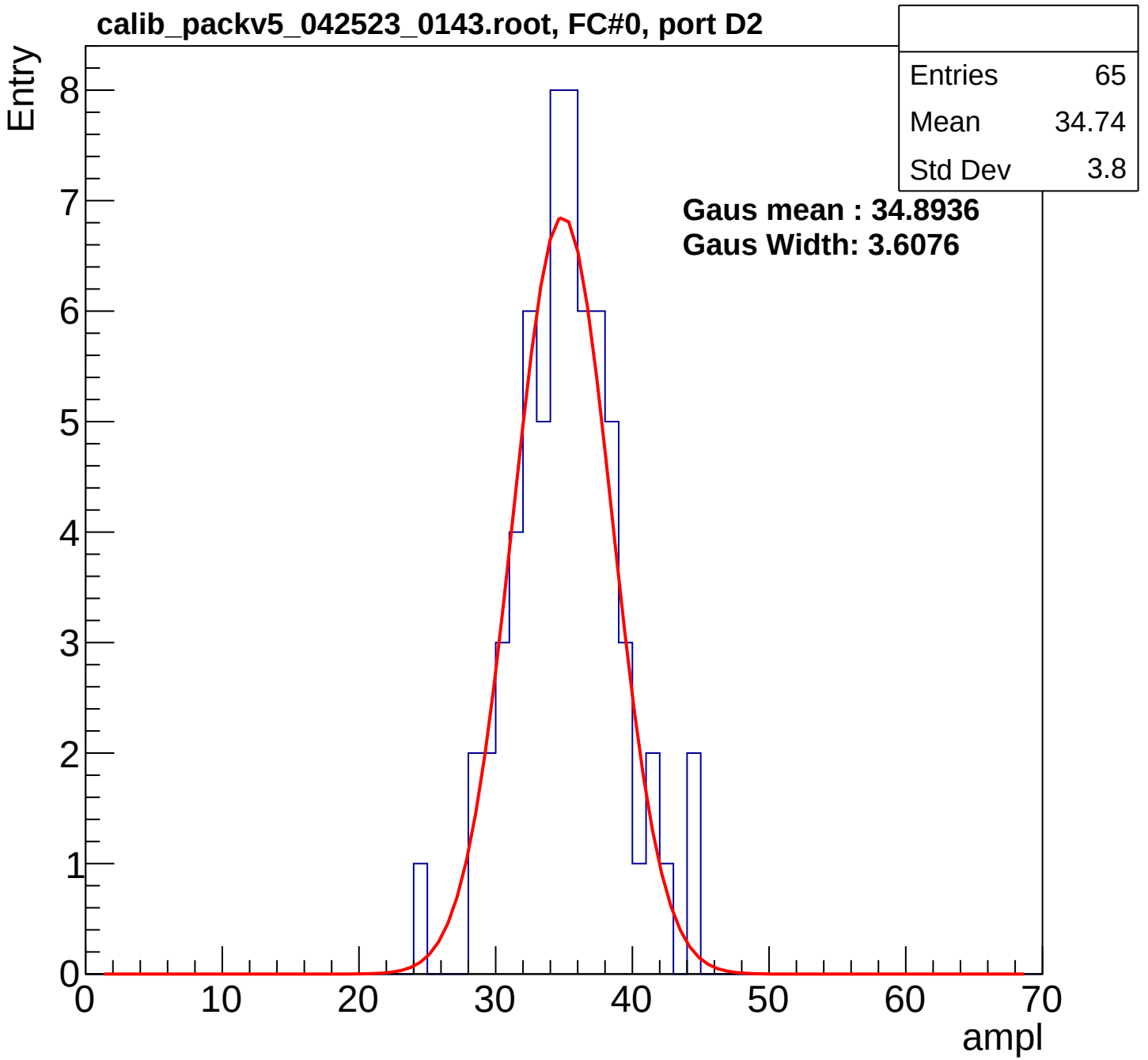
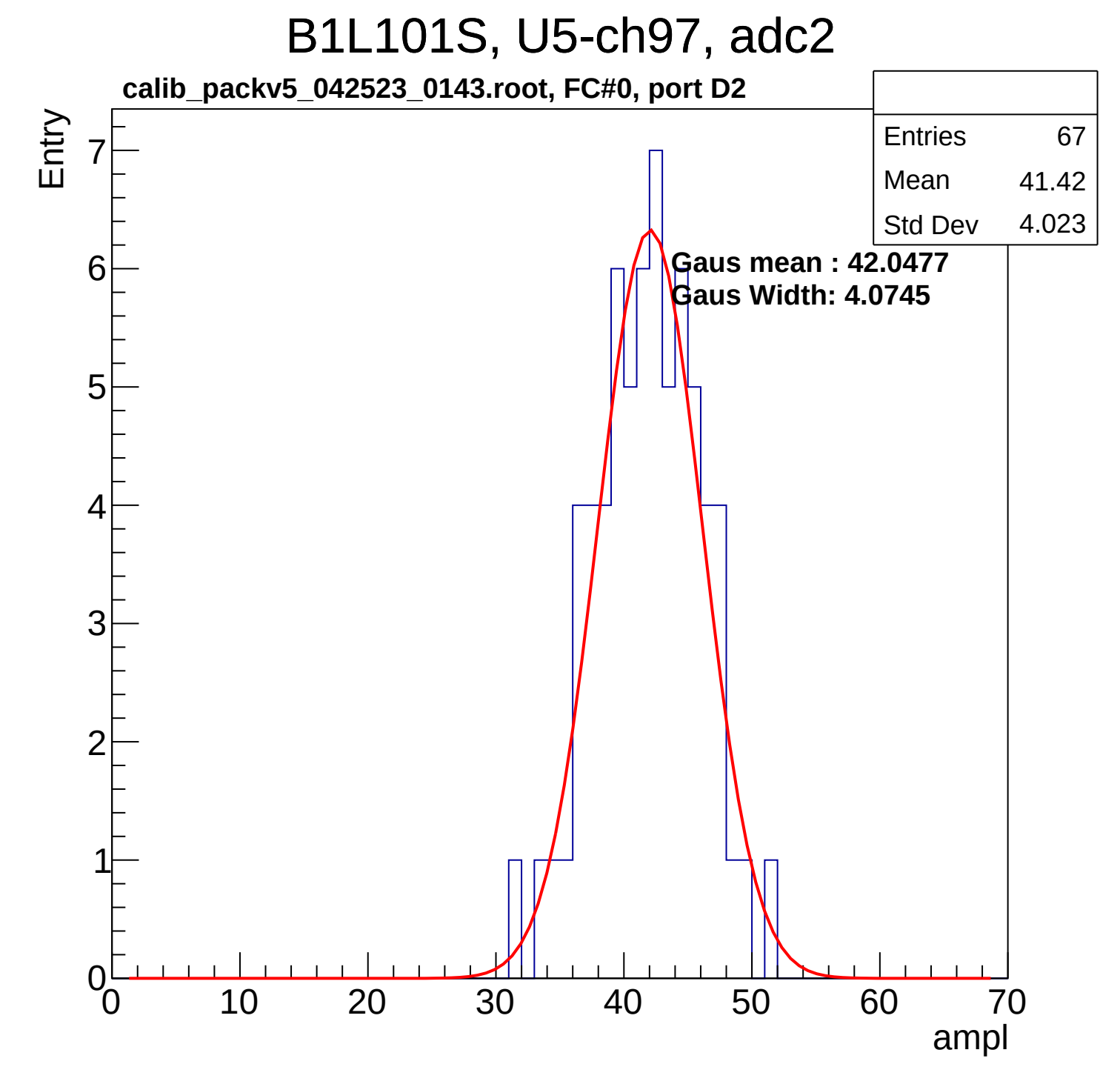

B1L101S, U5-ch97, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 34.74
Std Dev 3.8
Gaus mean : 34.8936
Gaus Width: 3.6076
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch97, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 41.42
Std Dev 4.023
Gaus mean : 42.0477
Gaus Width: 4.0745
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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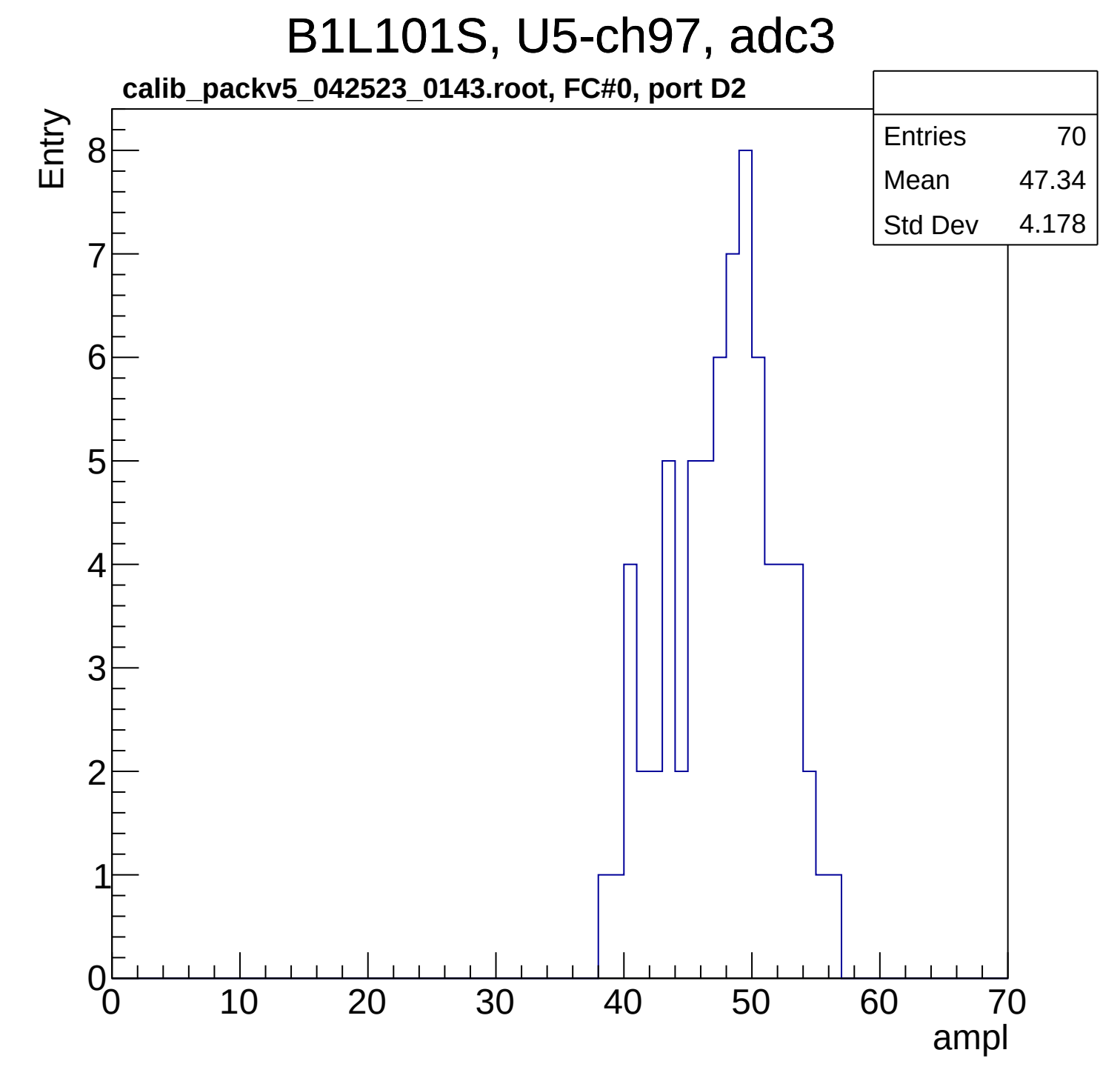
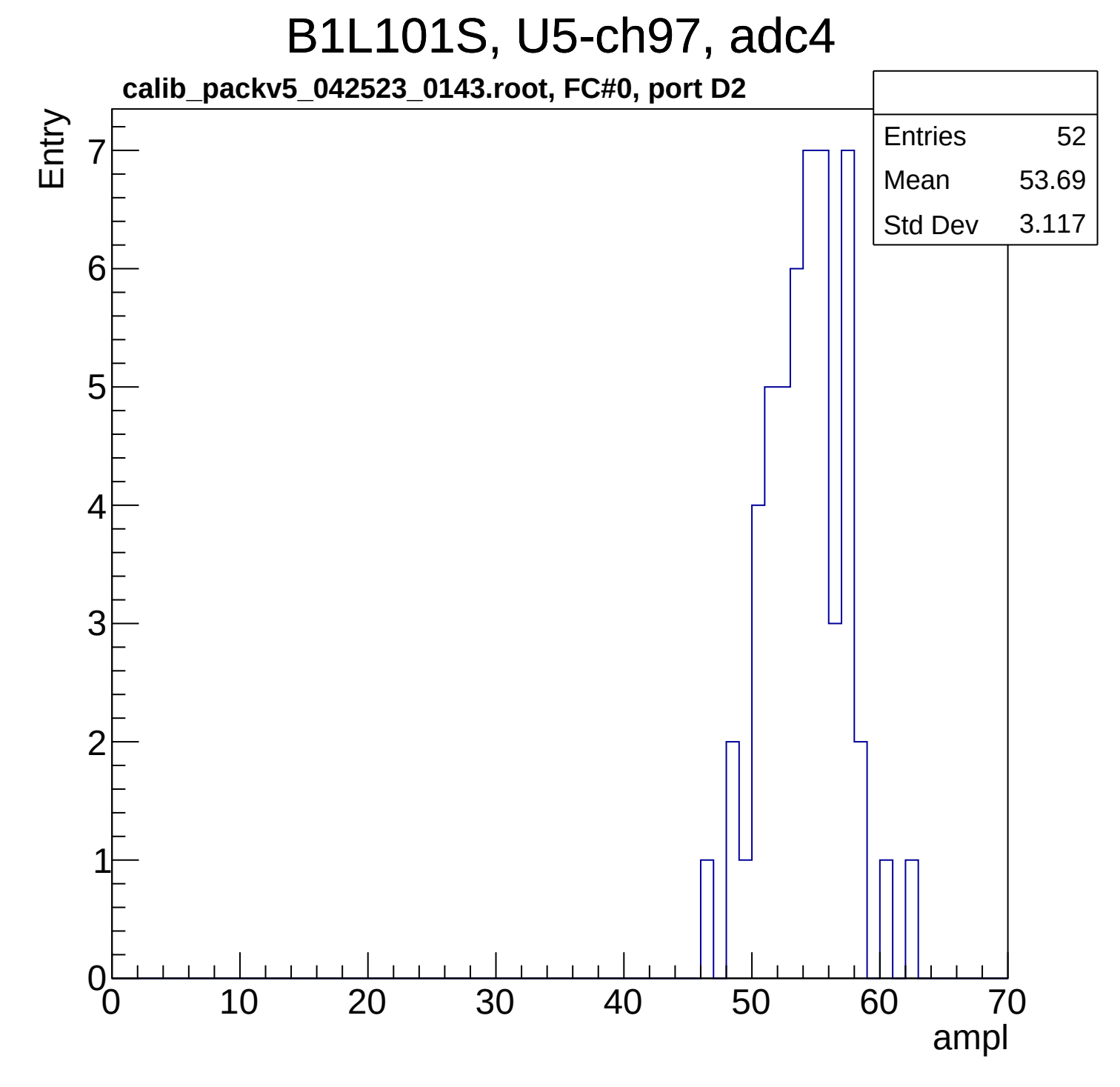

B1L101S, U5-ch97, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 47.34
Std Dev 4.178
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch97, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 53.69
Std Dev 3.117
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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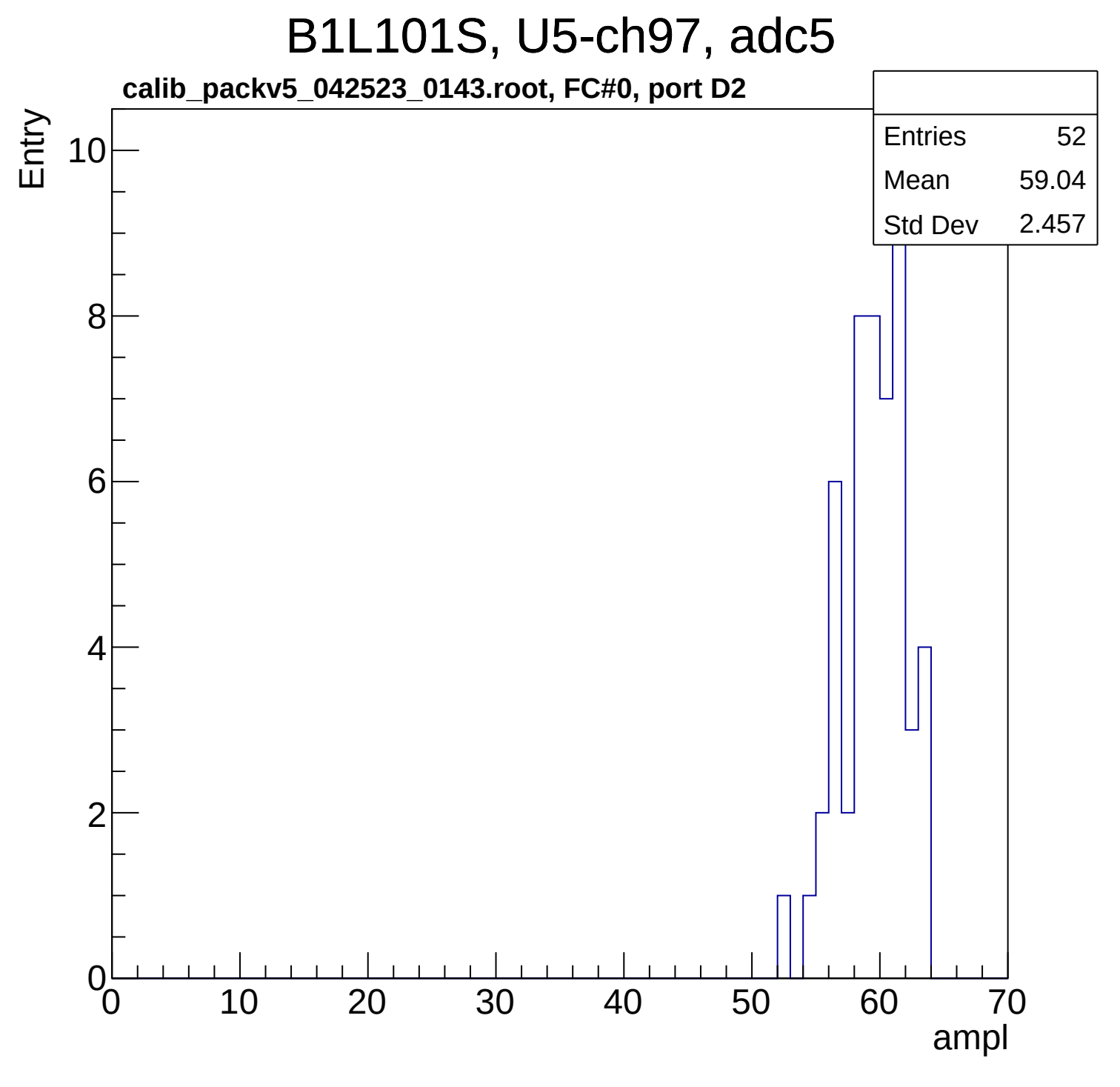
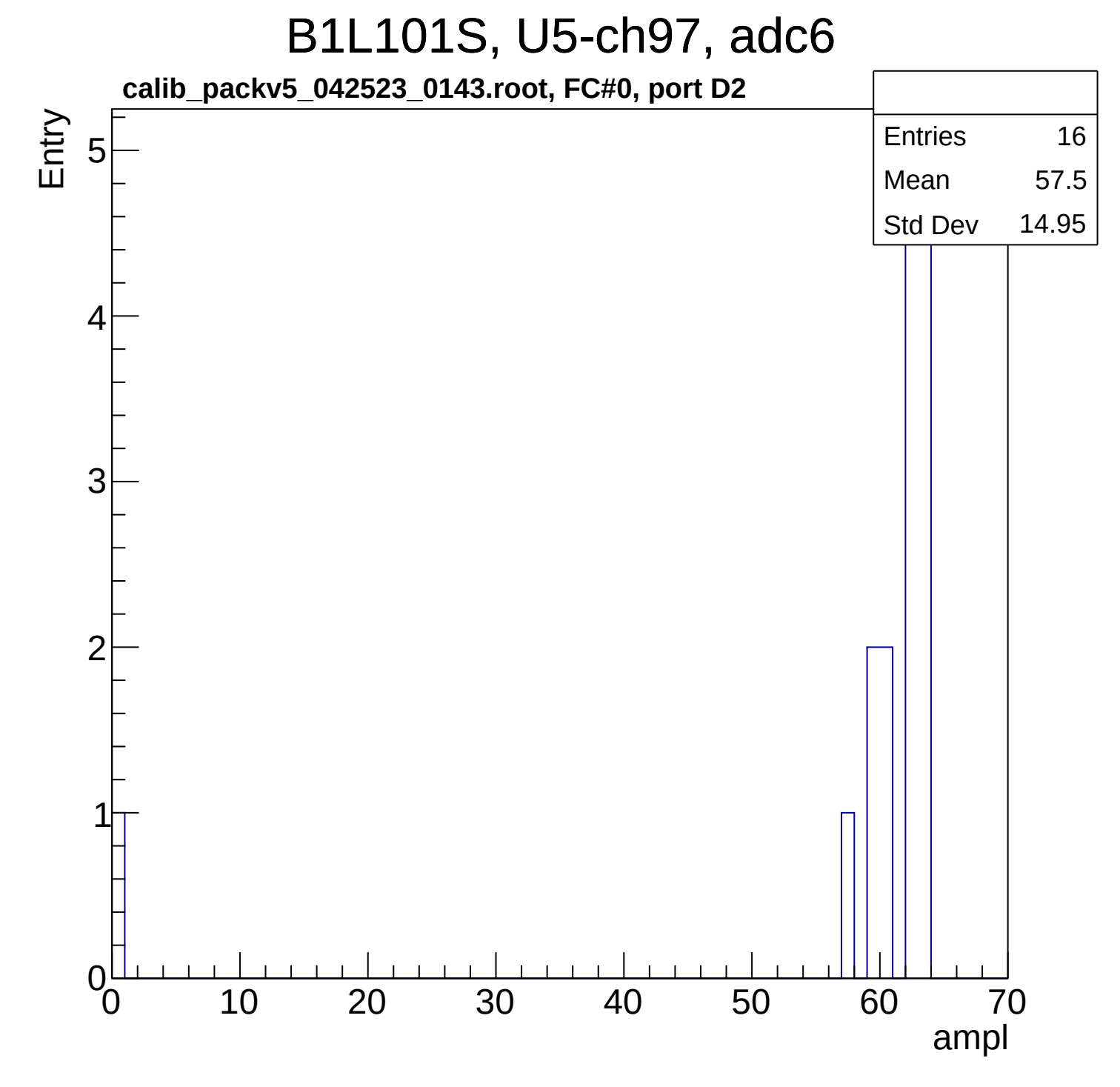
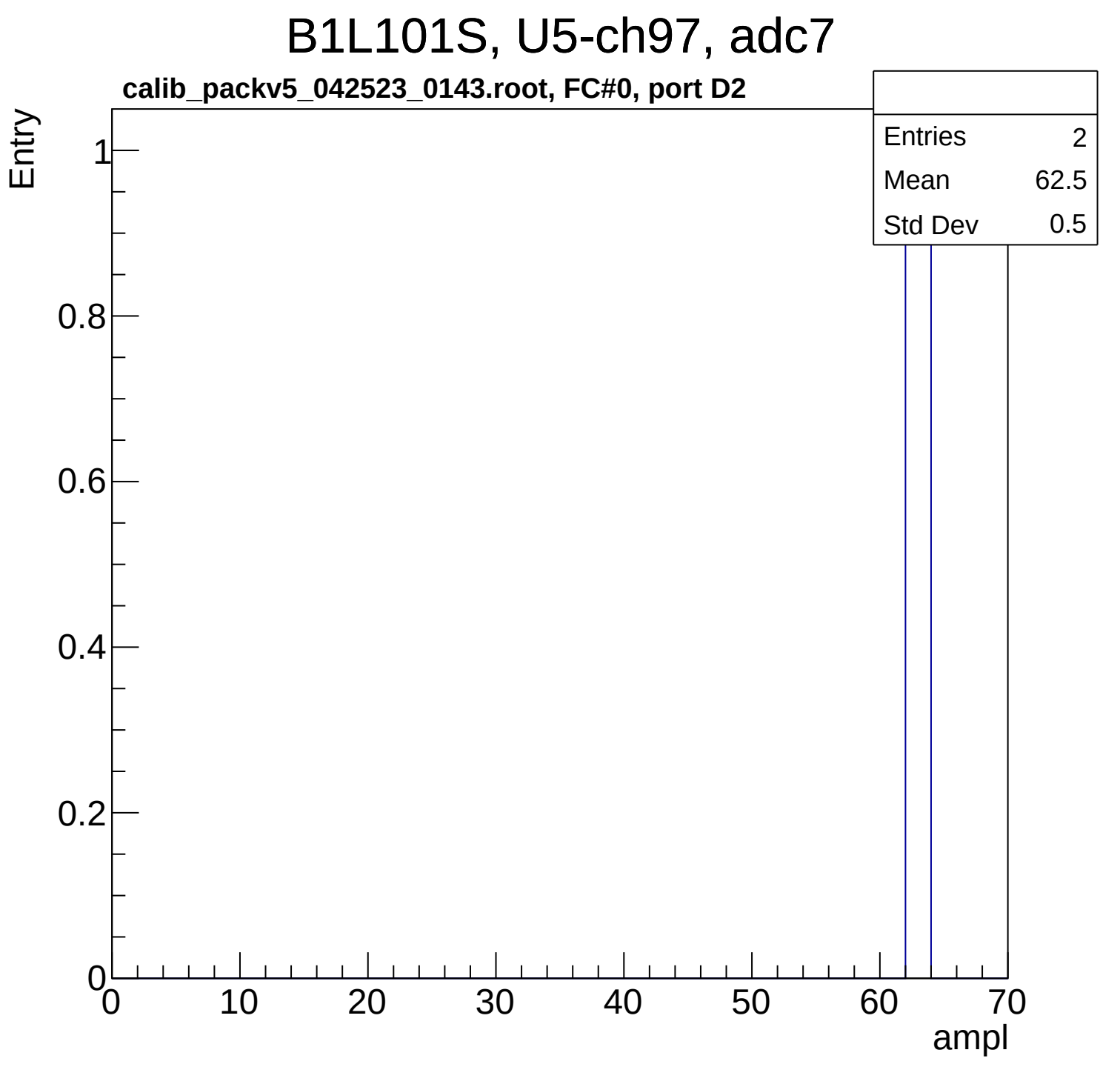
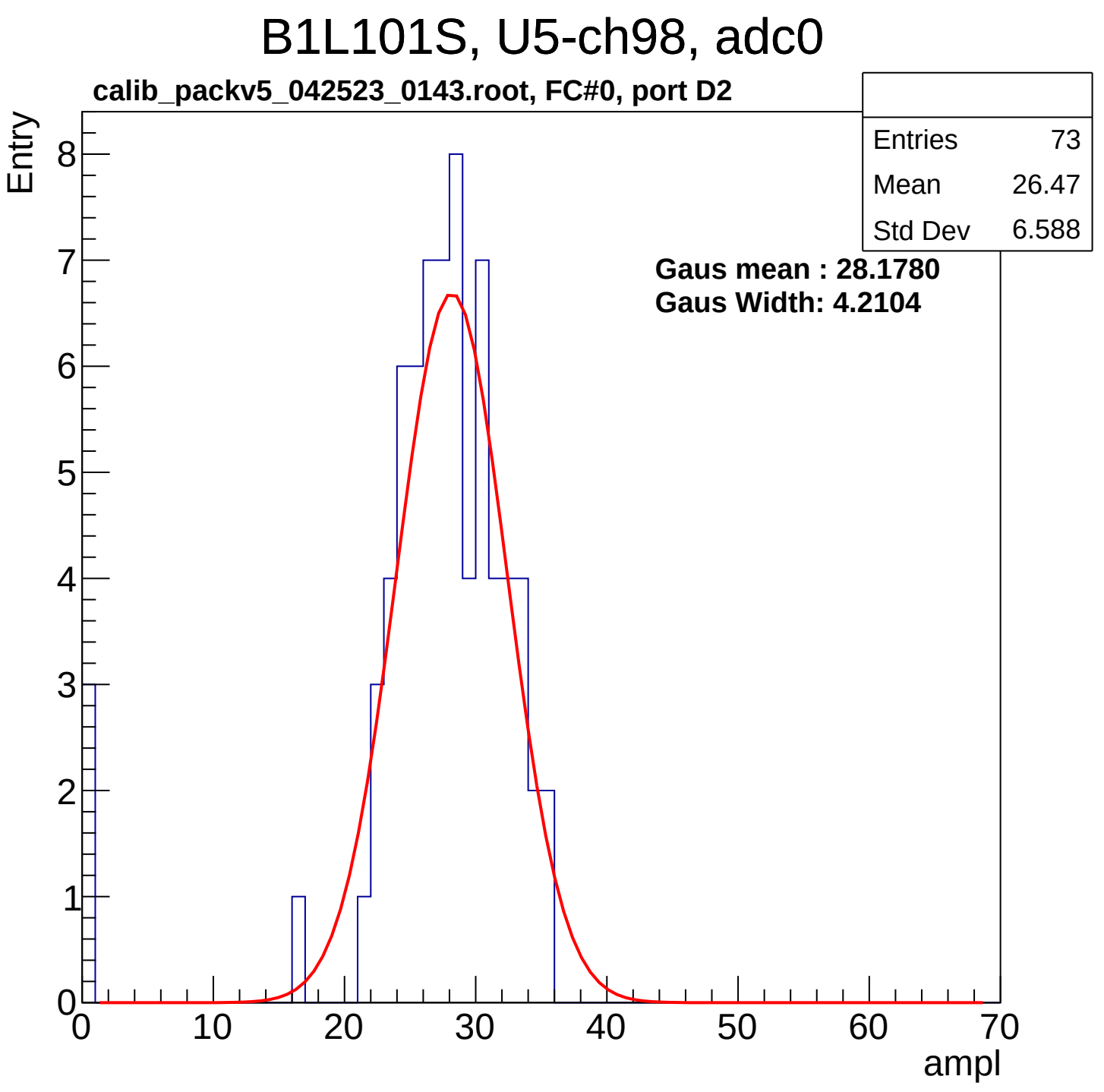
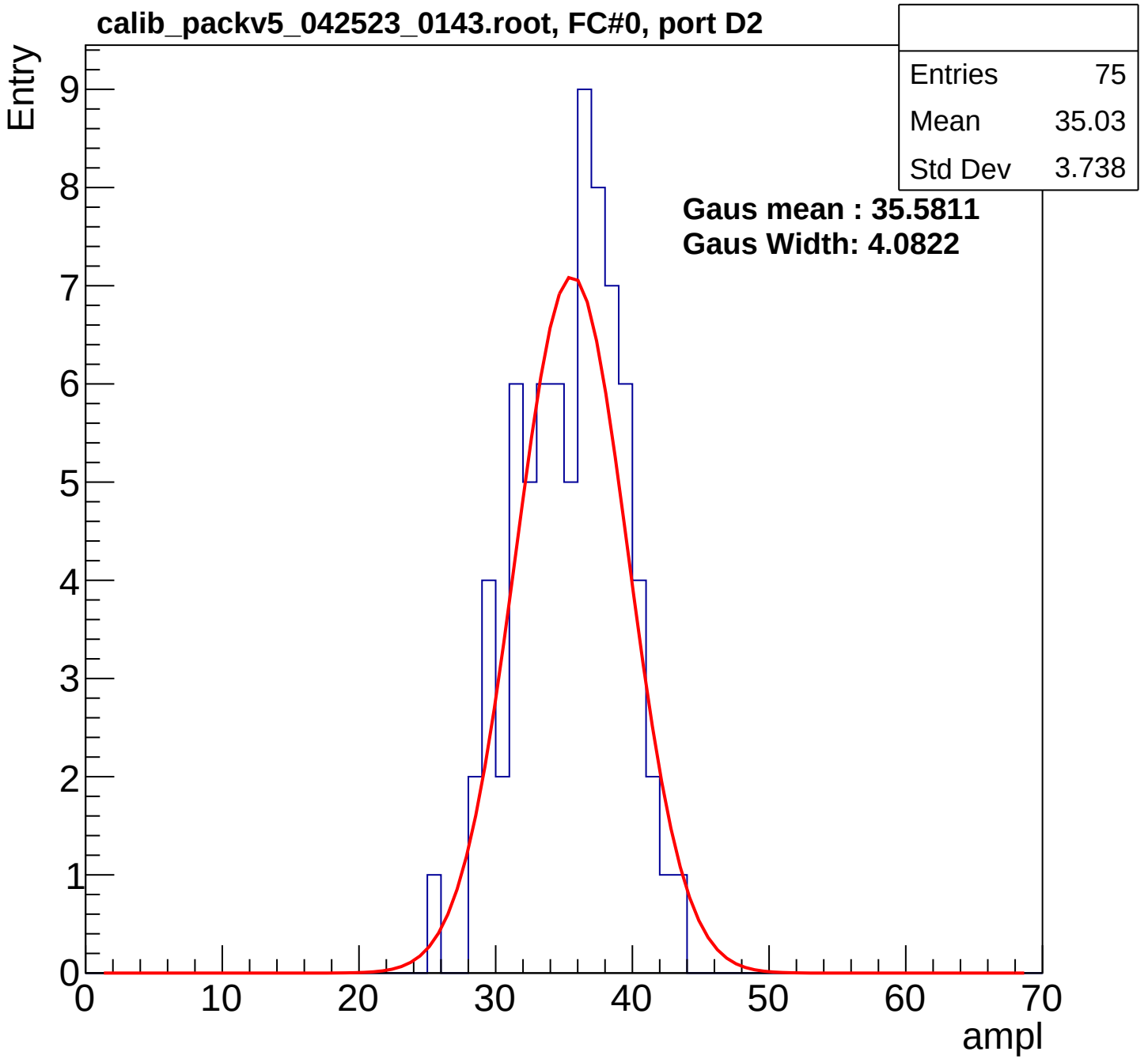
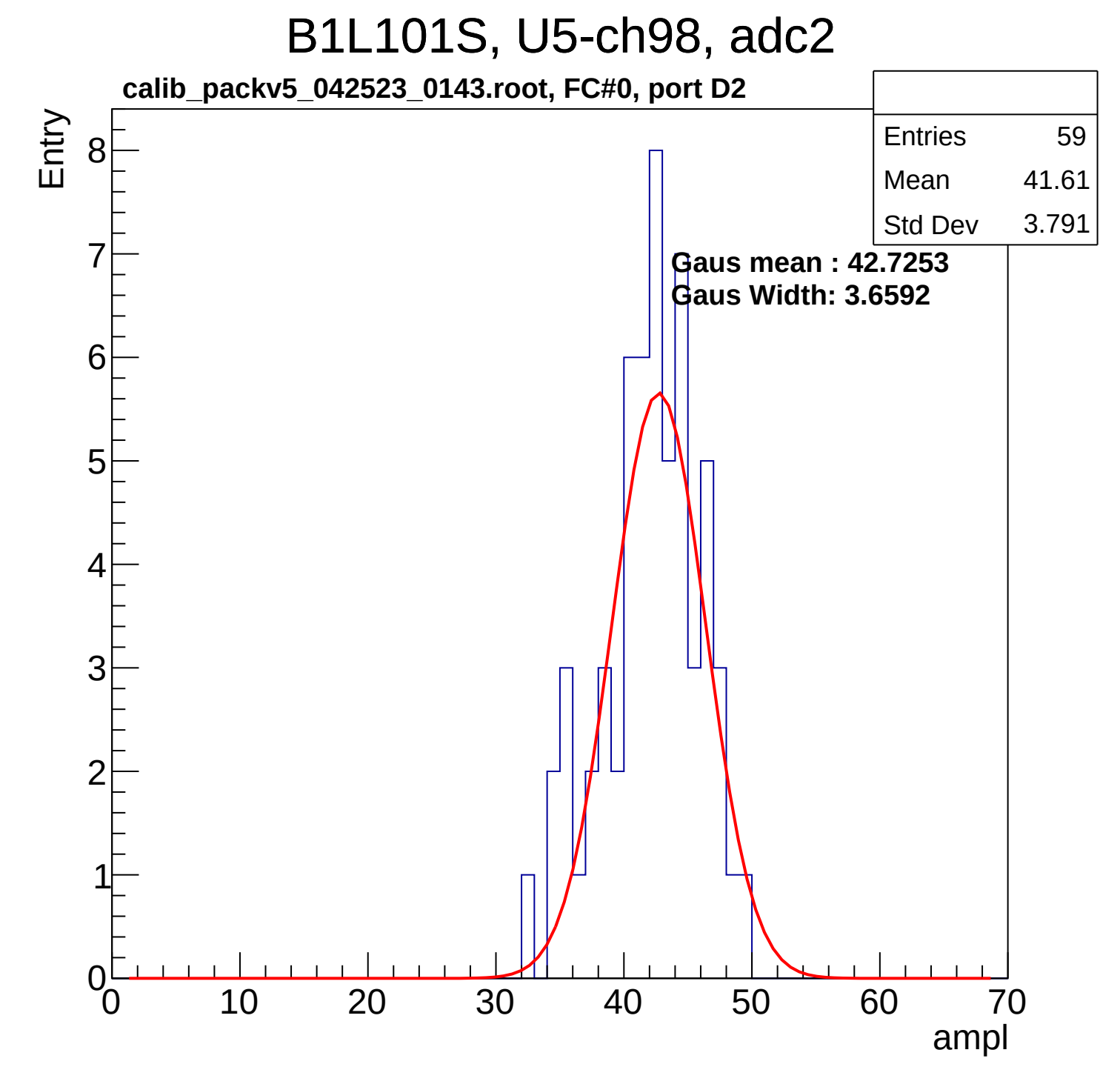

B1L101S, U5-ch97, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 59.04
Std Dev 2.457
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch97, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 16
Mean 57.5
Std Dev 14.95
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L101S, U5-ch97, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch98, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 26.47
Std Dev 6.588
Gaus mean : 28.1780
Gaus Width: 4.2104
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch98, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 35.03
Std Dev 3.738
Gaus mean : 35.5811
Gaus Width: 4.0822
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch98, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 41.61
Std Dev 3.791
Gaus mean : 42.7253
Gaus Width: 3.6592
Entry
ampl
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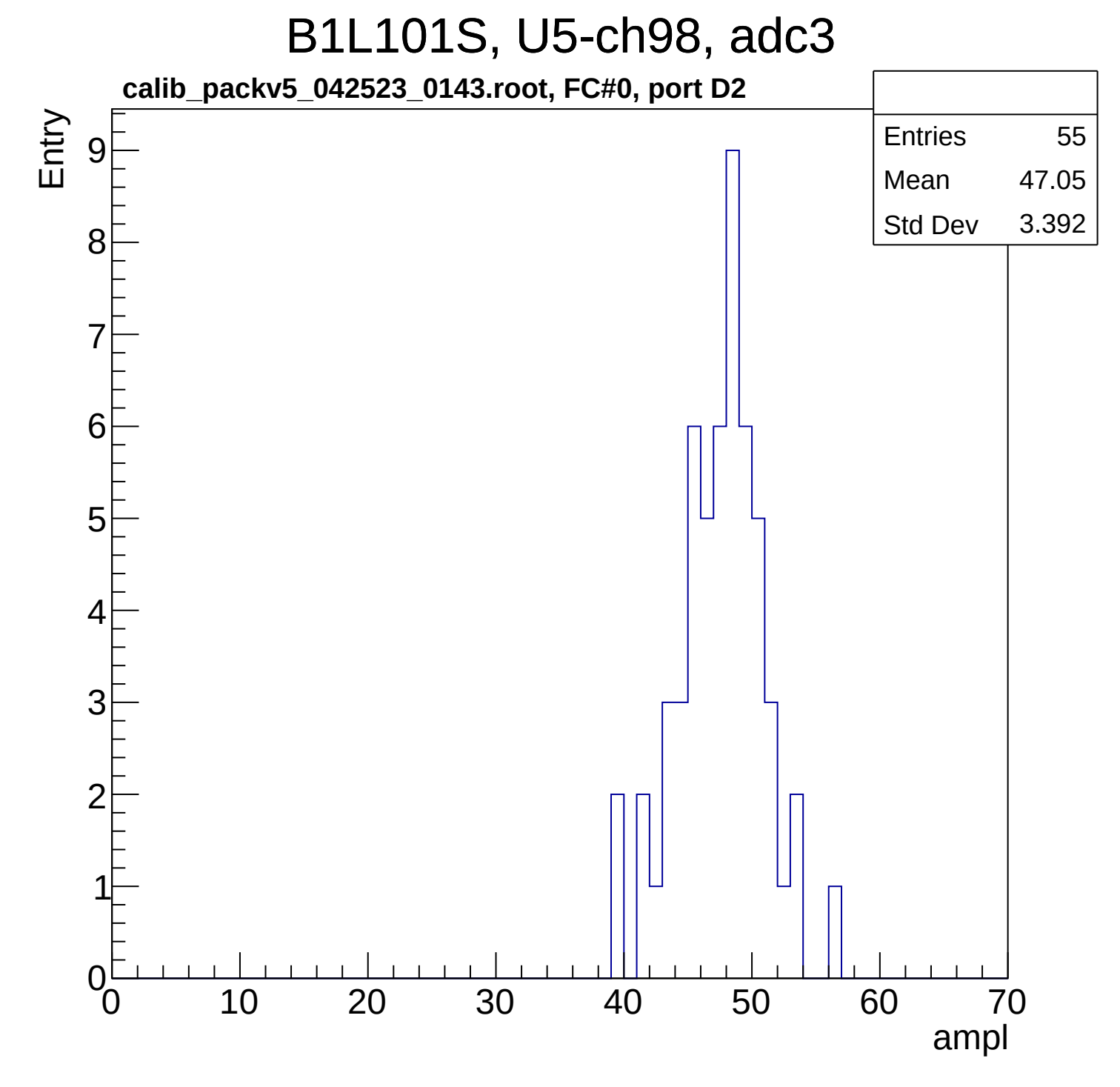
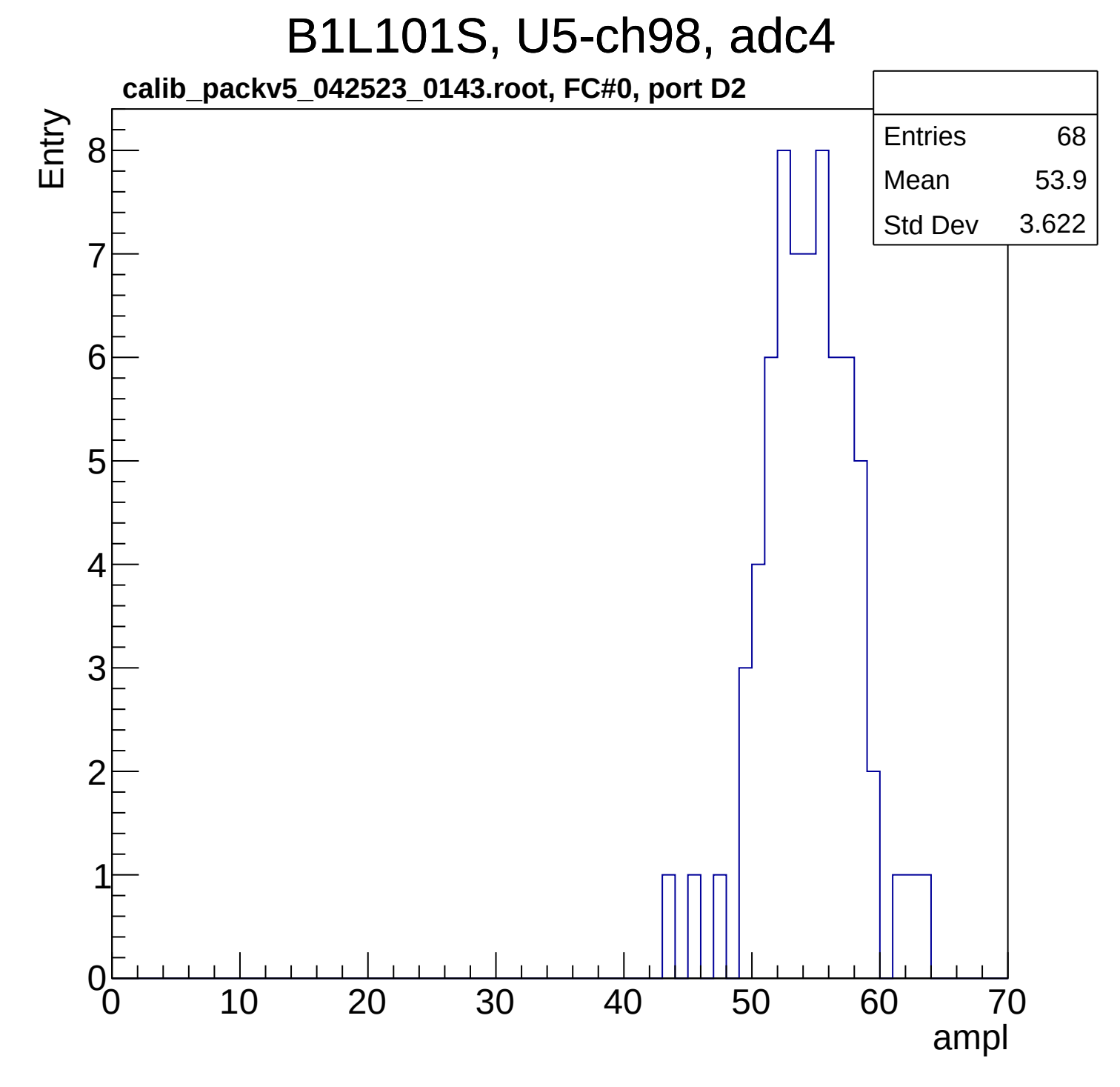
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch98, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 47.05
Std Dev 3.392
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch98, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 53.9
Std Dev 3.622
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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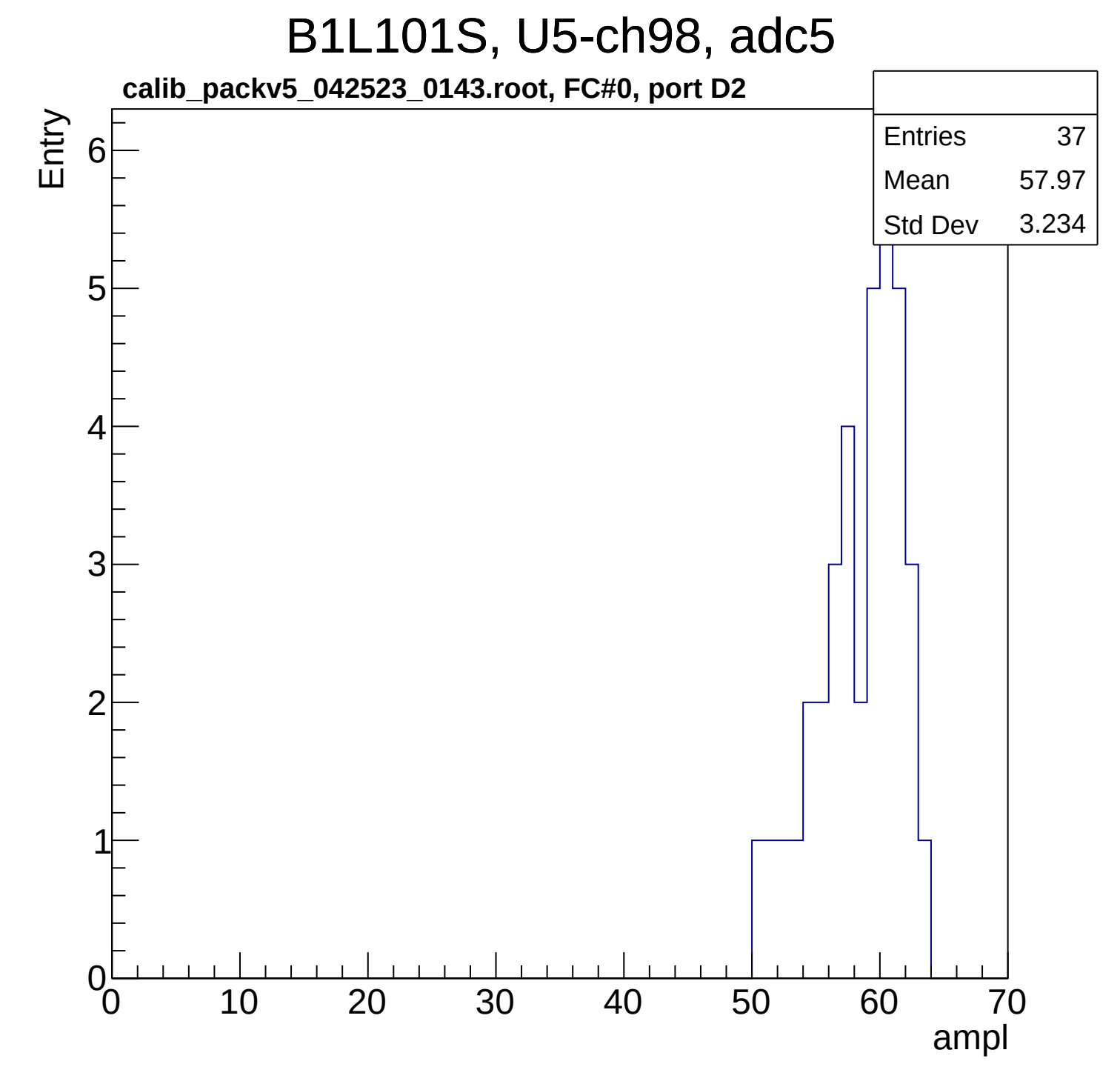
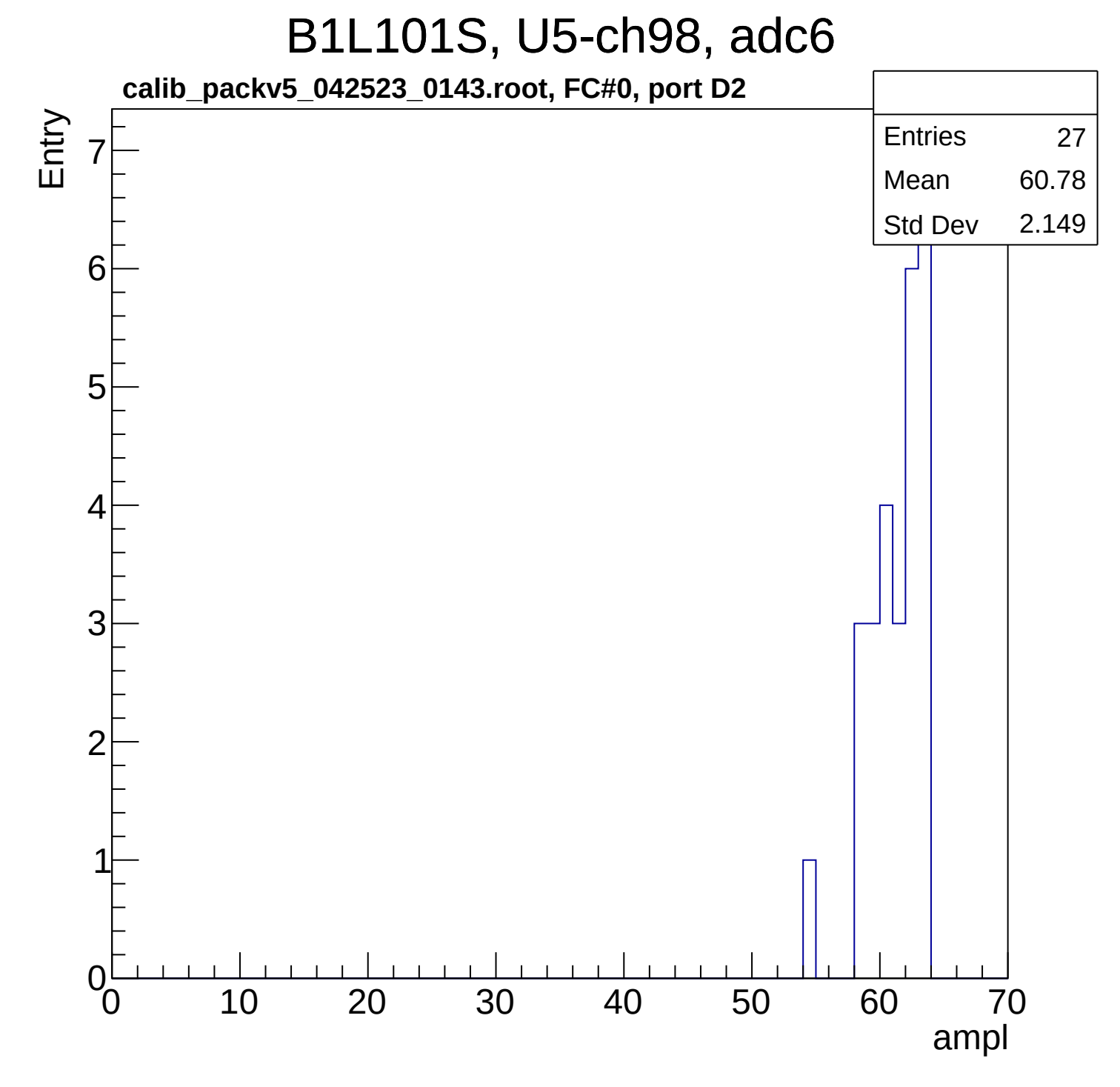

B1L101S, U5-ch98, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 37
Mean 57.97
Std Dev 3.234
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L101S, U5-ch98, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 27
Mean 60.78
Std Dev 2.149
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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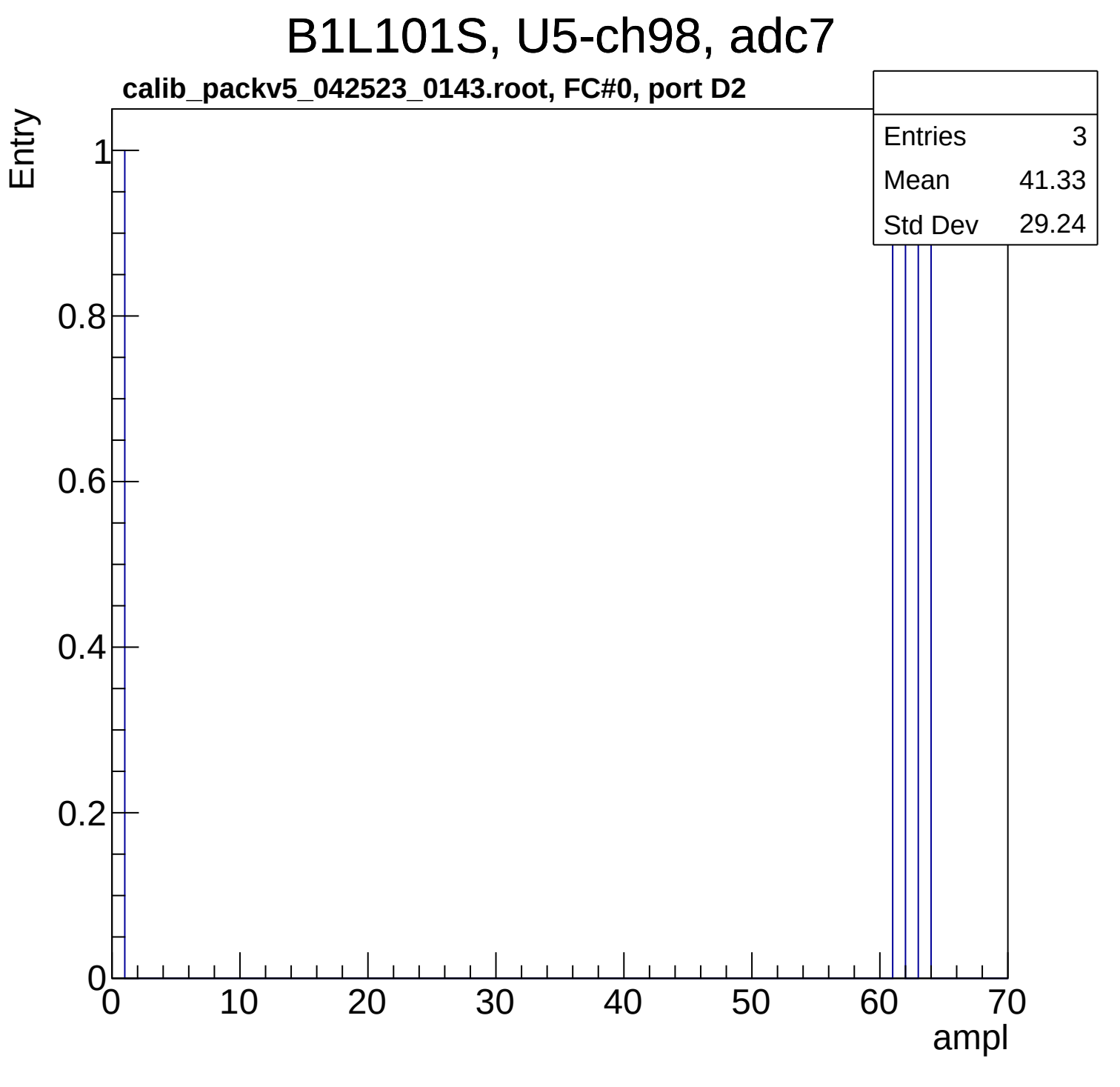
B1L101S, U5-ch98, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 41.33
Std Dev 29.24
Entry
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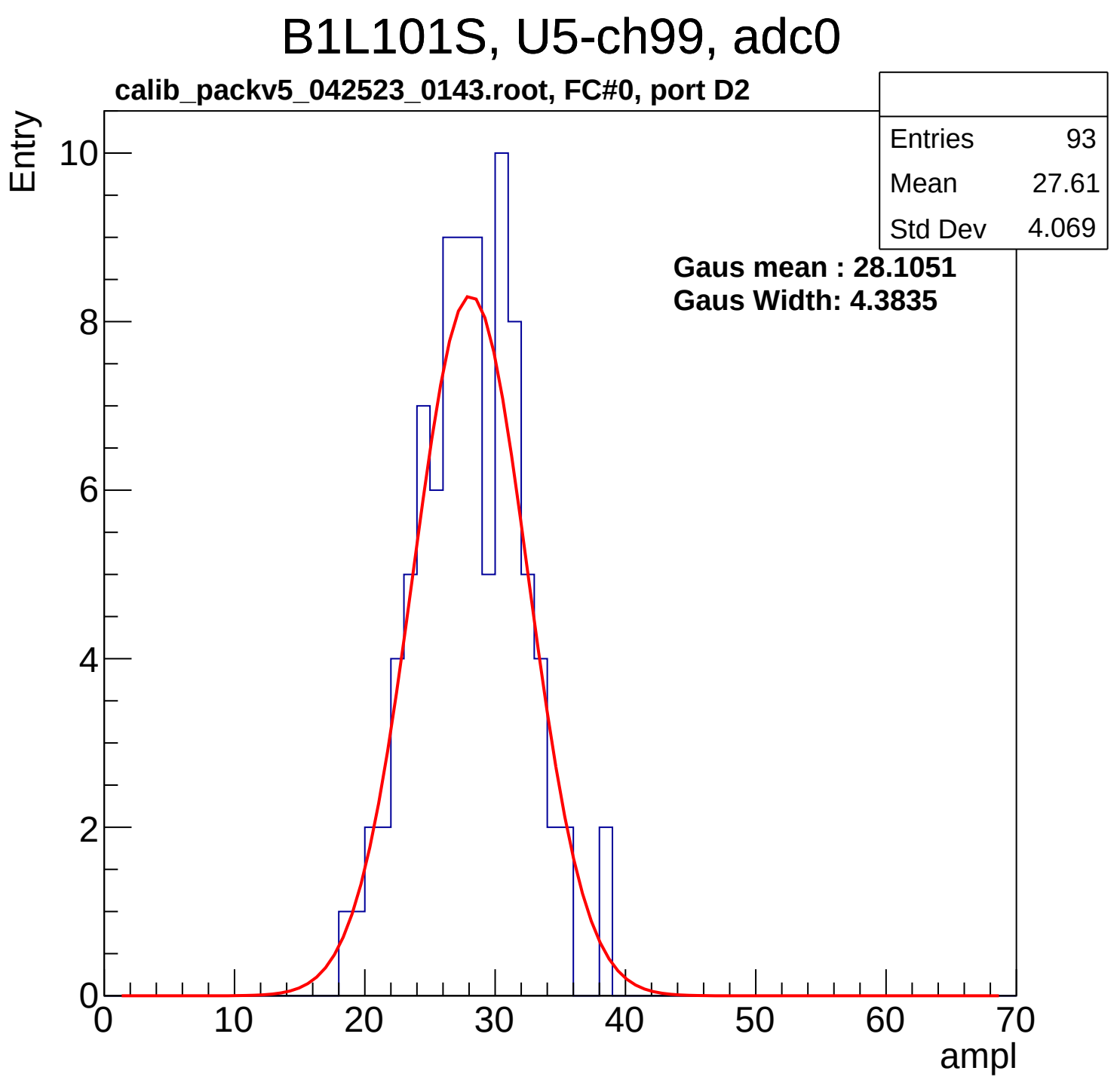
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch99, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 93
Mean 27.61
Std Dev 4.069
Gaus mean : 28.1051
Gaus Width: 4.3835
Entry
ampl
0
2
4
6
8
10
0
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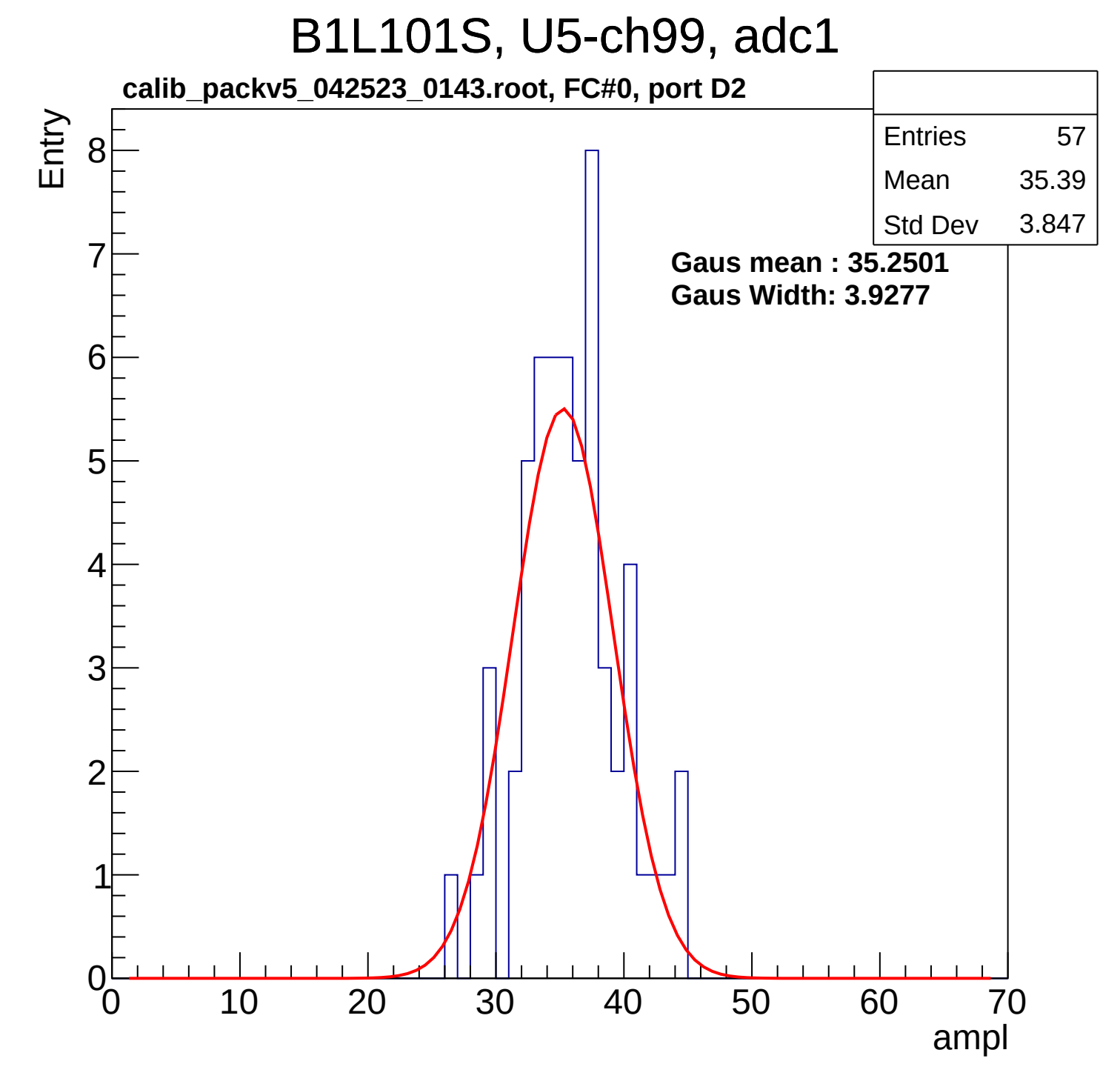
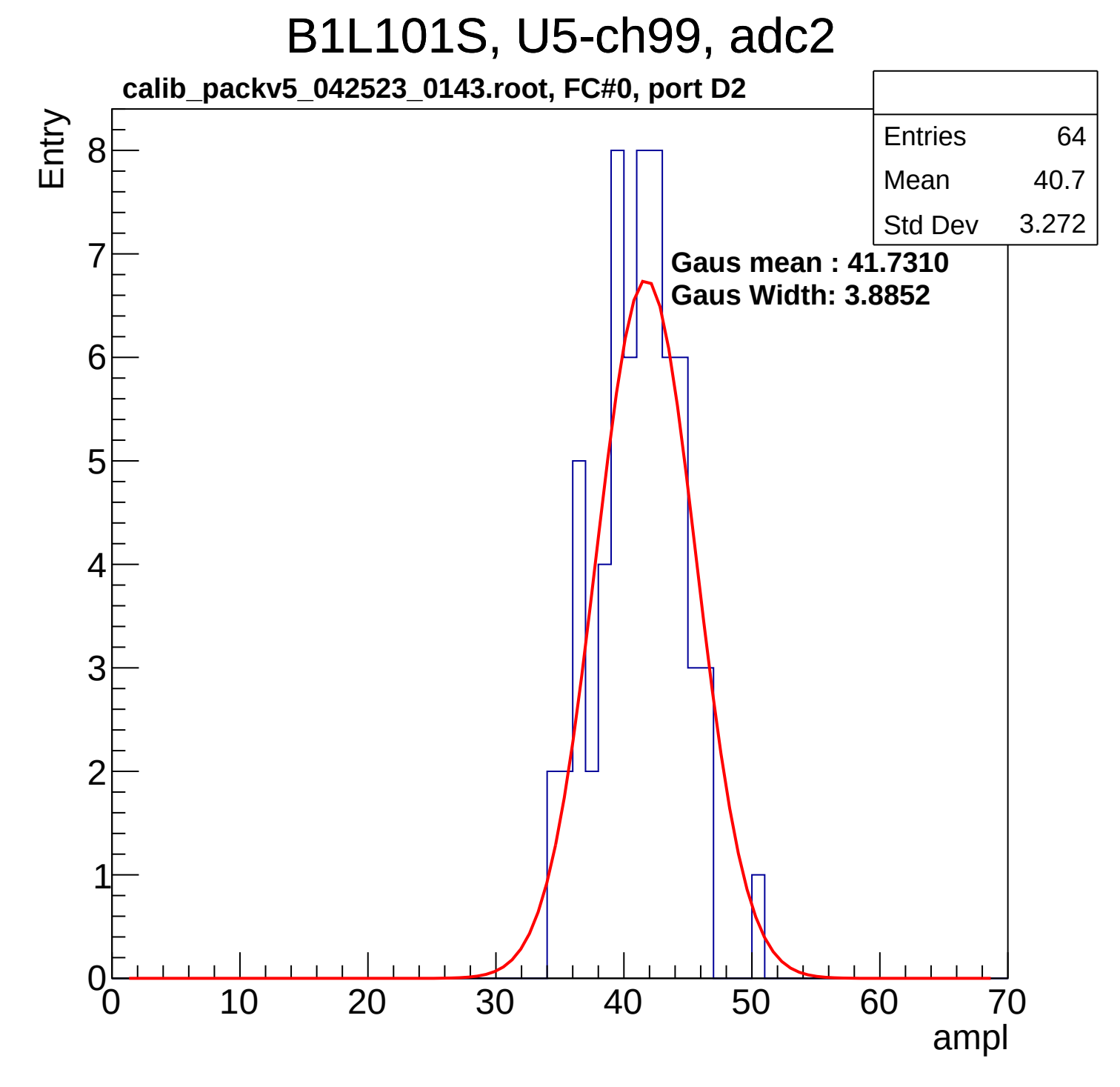
20
30
40
50
60
70


B1L101S, U5-ch99, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 35.39
Std Dev 3.847
Gaus mean : 35.2501
Gaus Width: 3.9277
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch99, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 40.7
Std Dev 3.272
Gaus mean : 41.7310
Gaus Width: 3.8852
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
50
60
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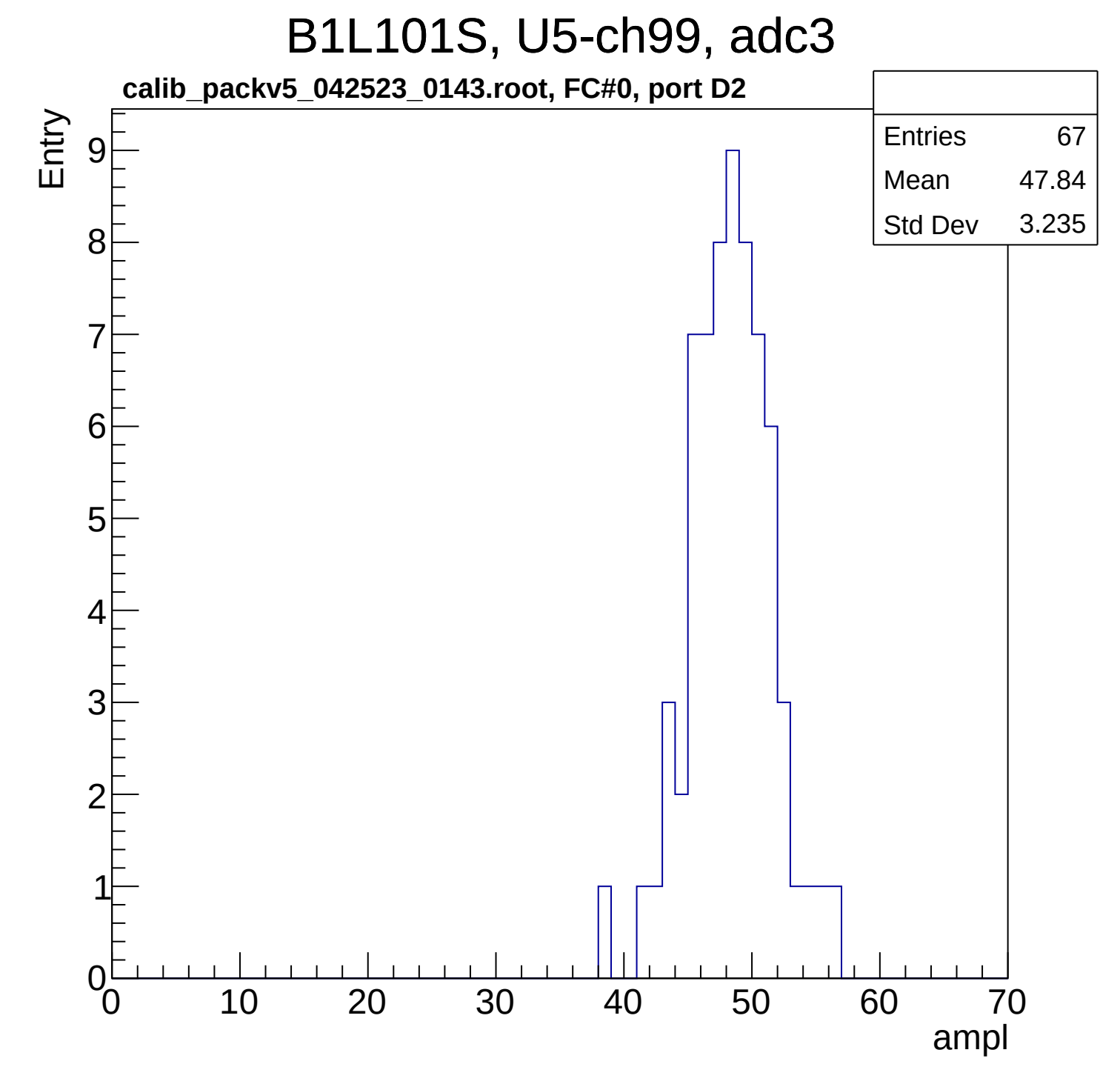
B1L101S, U5-ch99, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 47.84
Std Dev 3.235
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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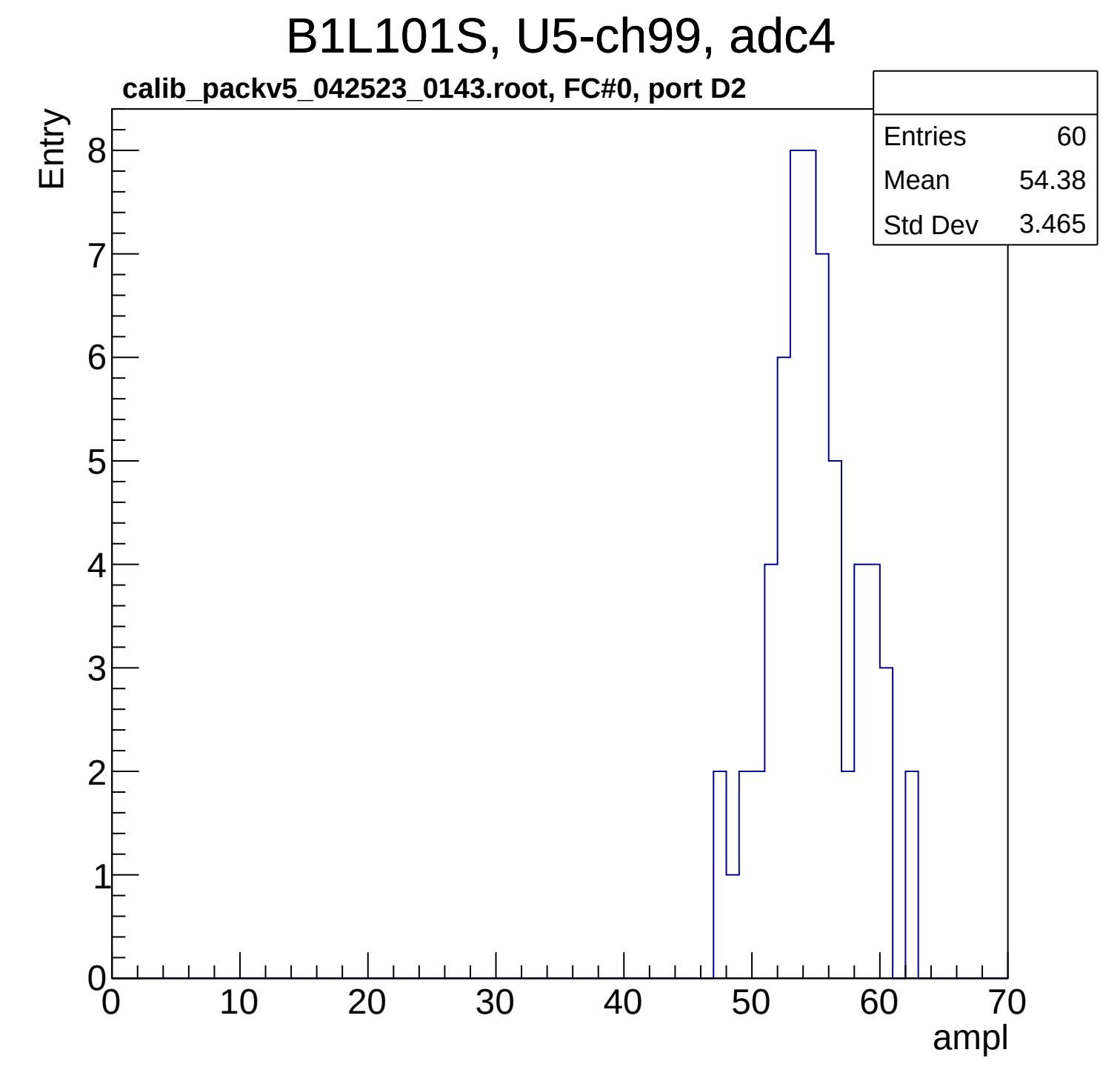
B1L101S, U5-ch99, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 54.38
Std Dev 3.465
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
50
60
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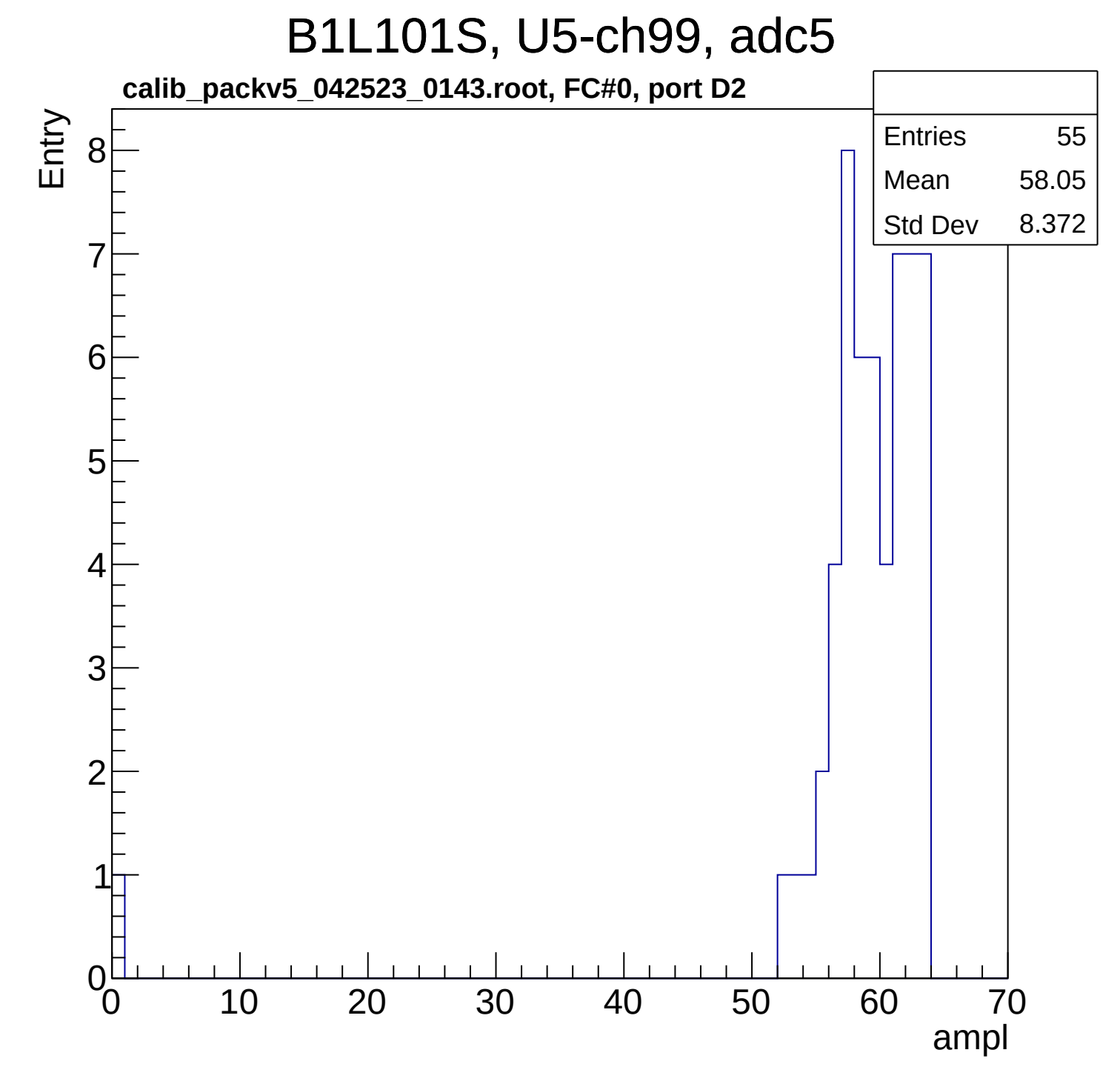
B1L101S, U5-ch99, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 58.05
Std Dev 8.372
Entry
ampl
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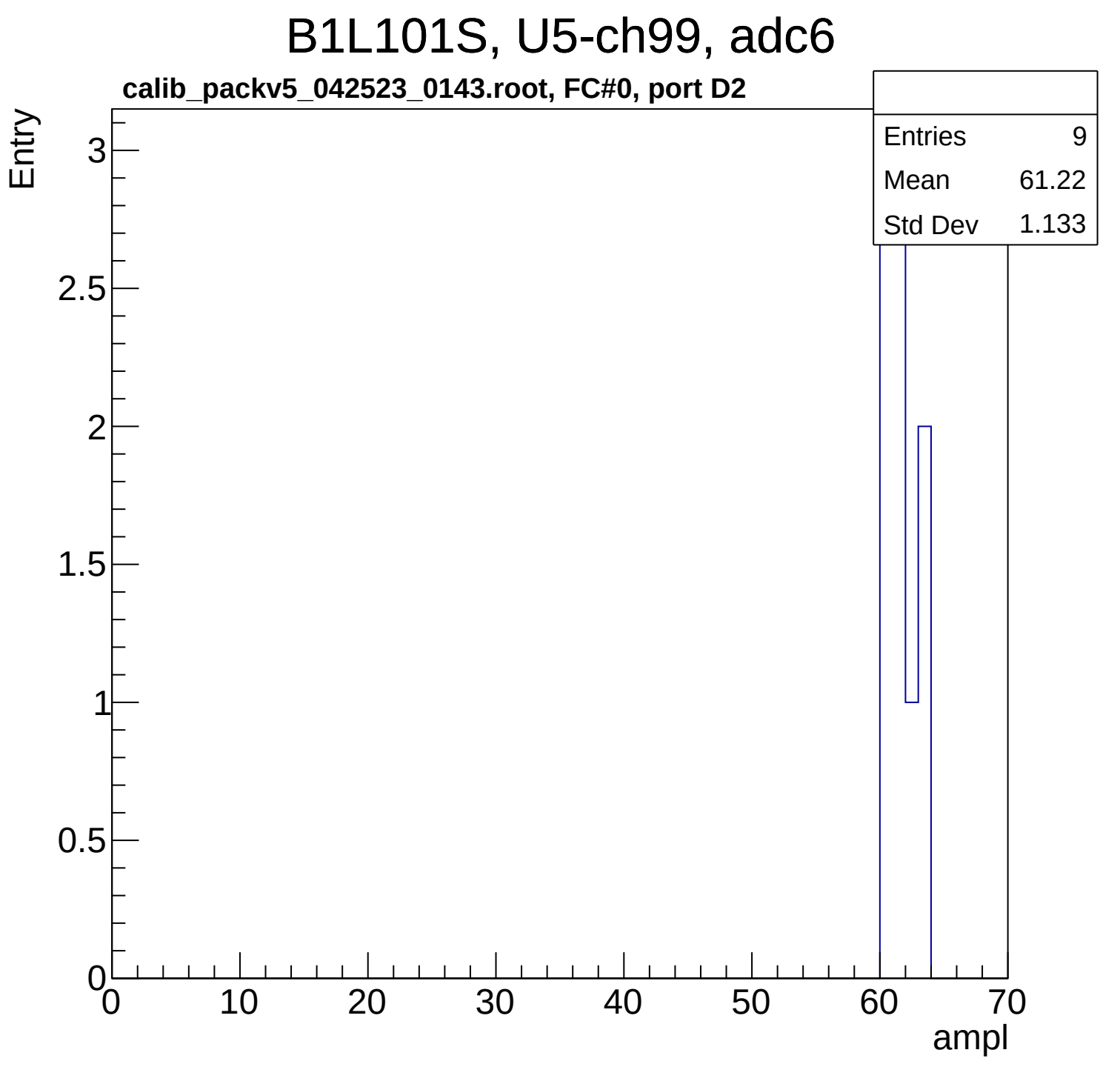
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch99, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 61.22
Std Dev 1.133
Entry
ampl
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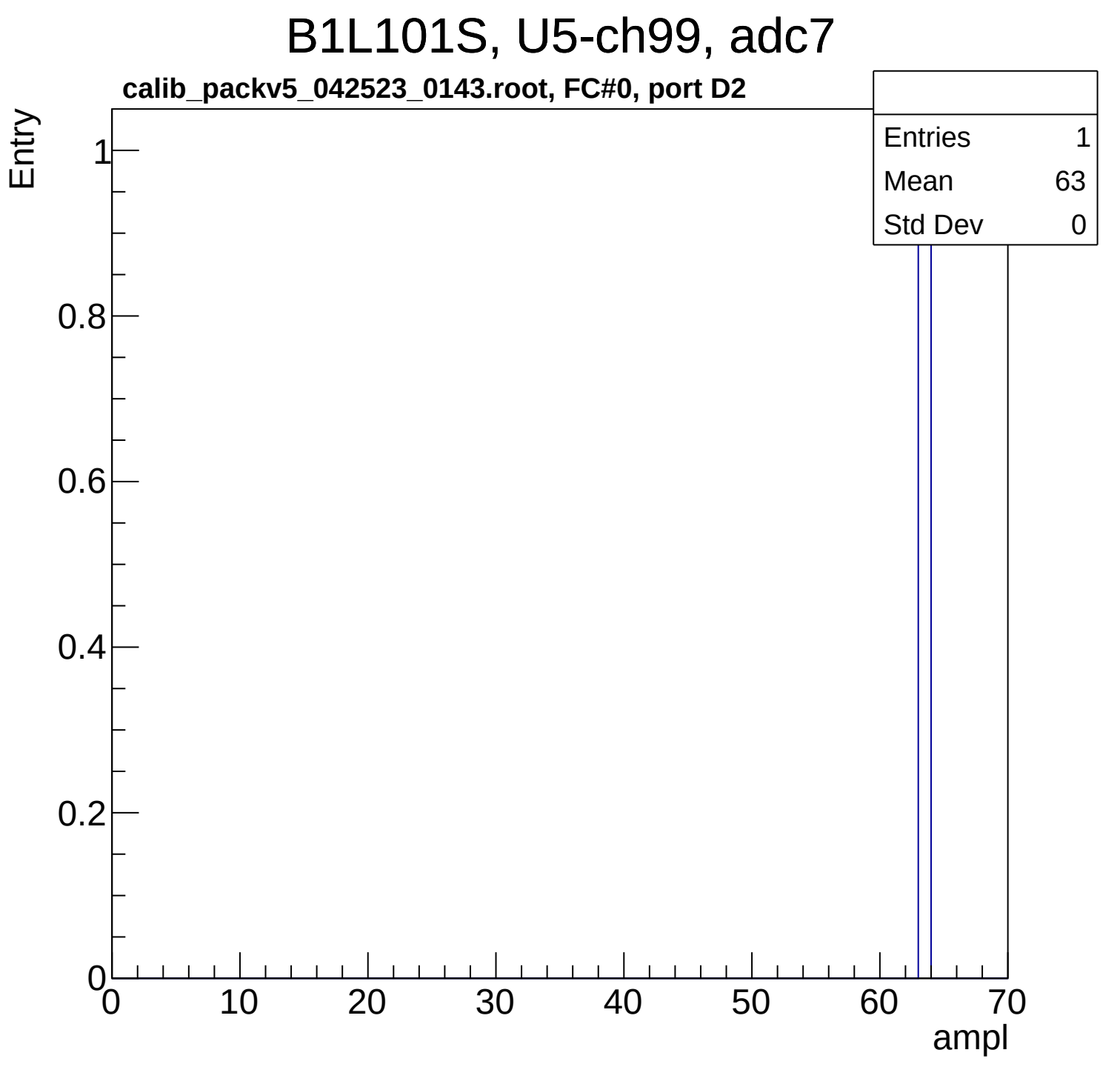
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U5-ch99, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 63
Std Dev 0
Entry
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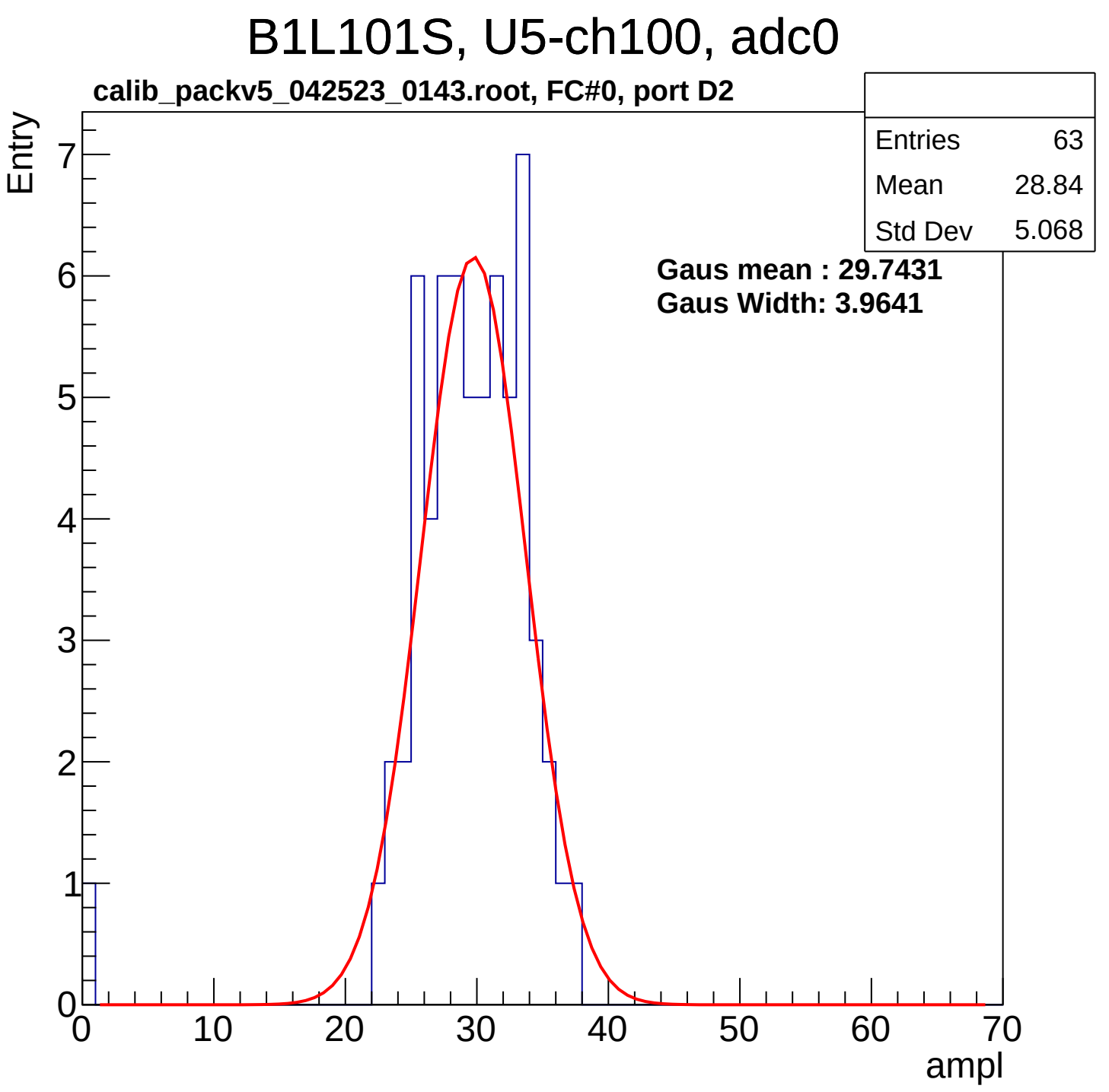
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch100, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 28.84
Std Dev 5.068
Gaus mean : 29.7431
Gaus Width: 3.9641
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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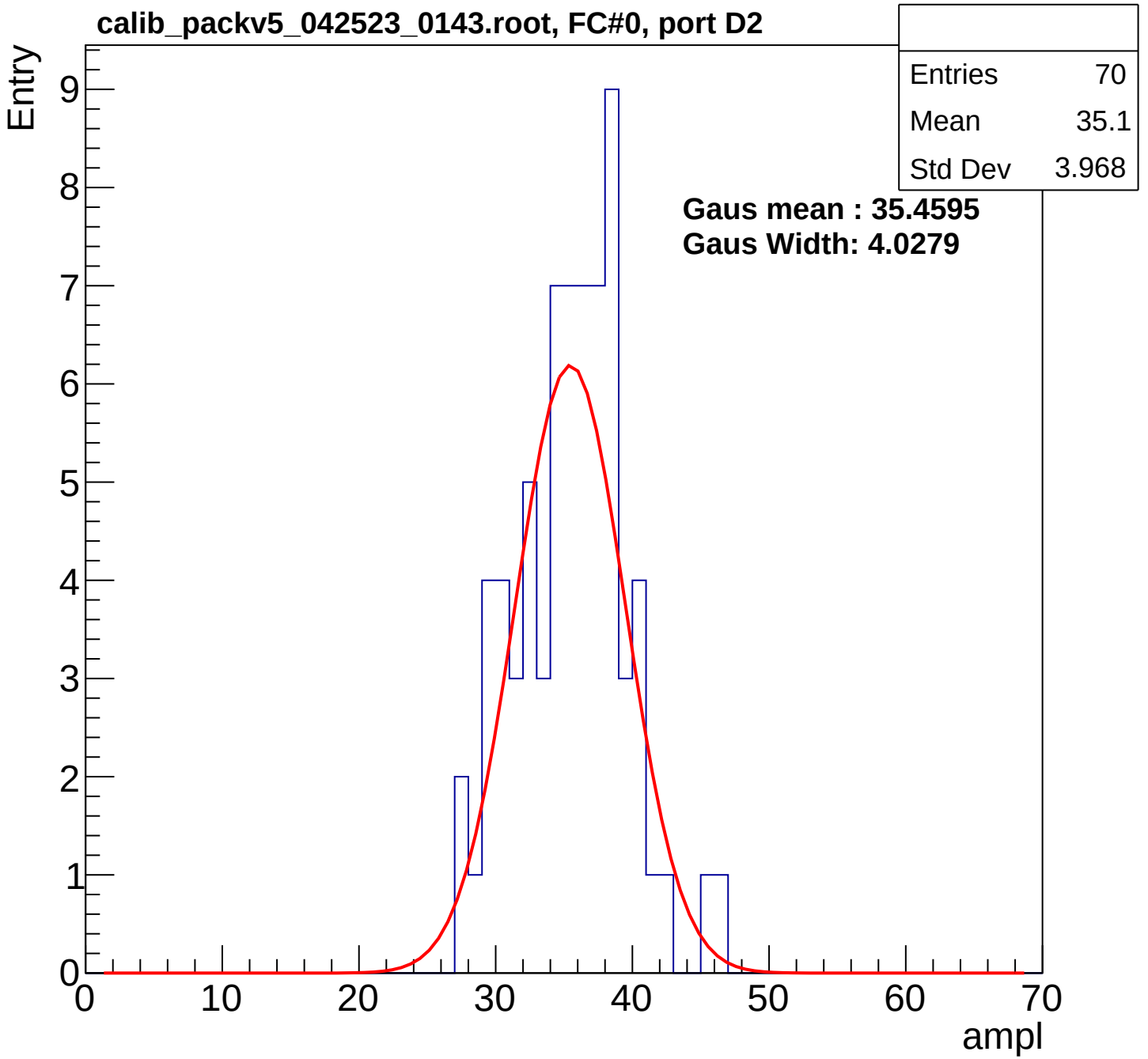
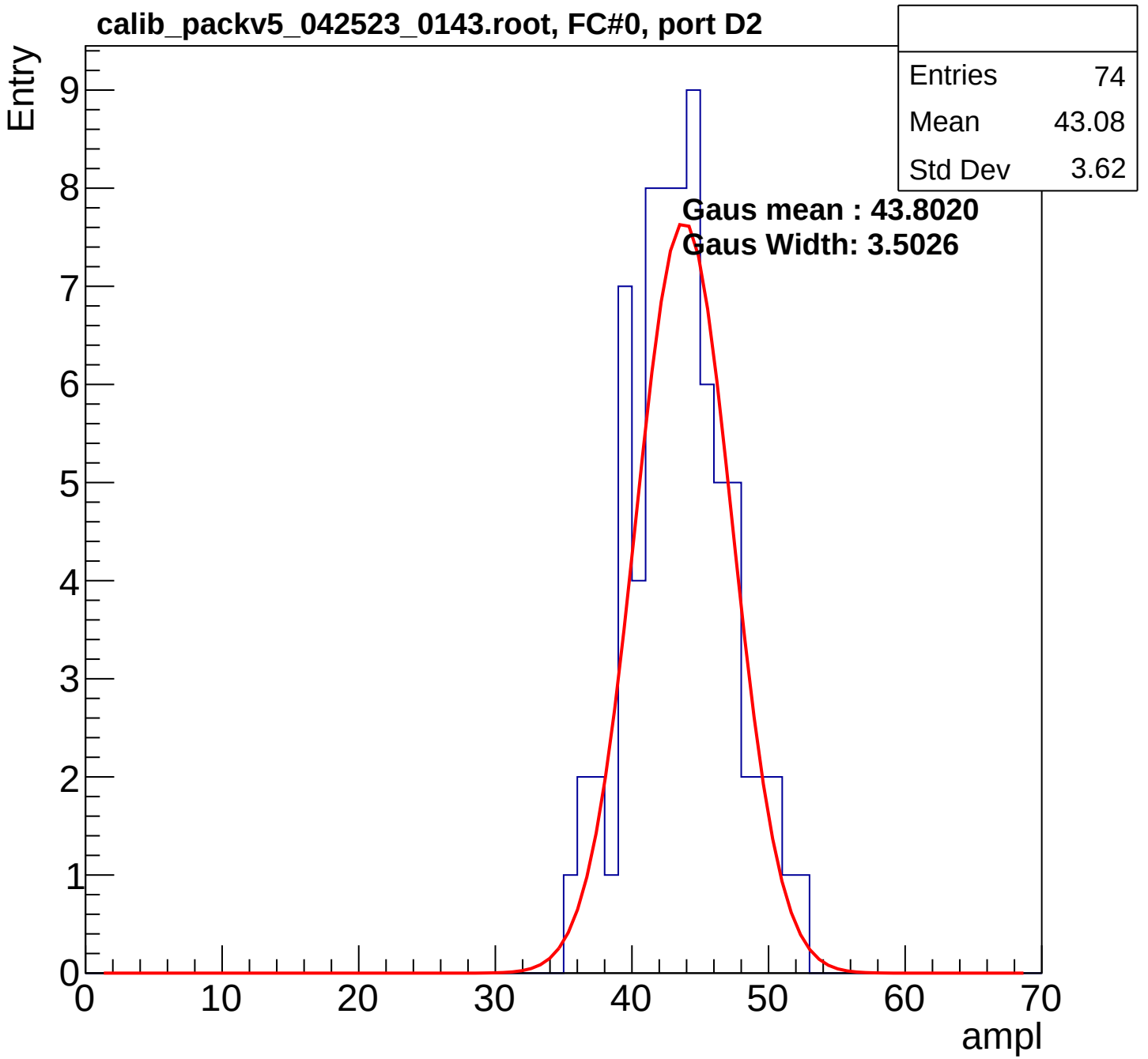

B1L101S, U5-ch100, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 35.1
Std Dev 3.968
Gaus mean : 35.4595
Gaus Width: 4.0279
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch100, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 43.08
Std Dev 3.62
Gaus mean : 43.8020
Gaus Width: 3.5026
Entry
ampl
0
1
2
3
4
5
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8
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0
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60
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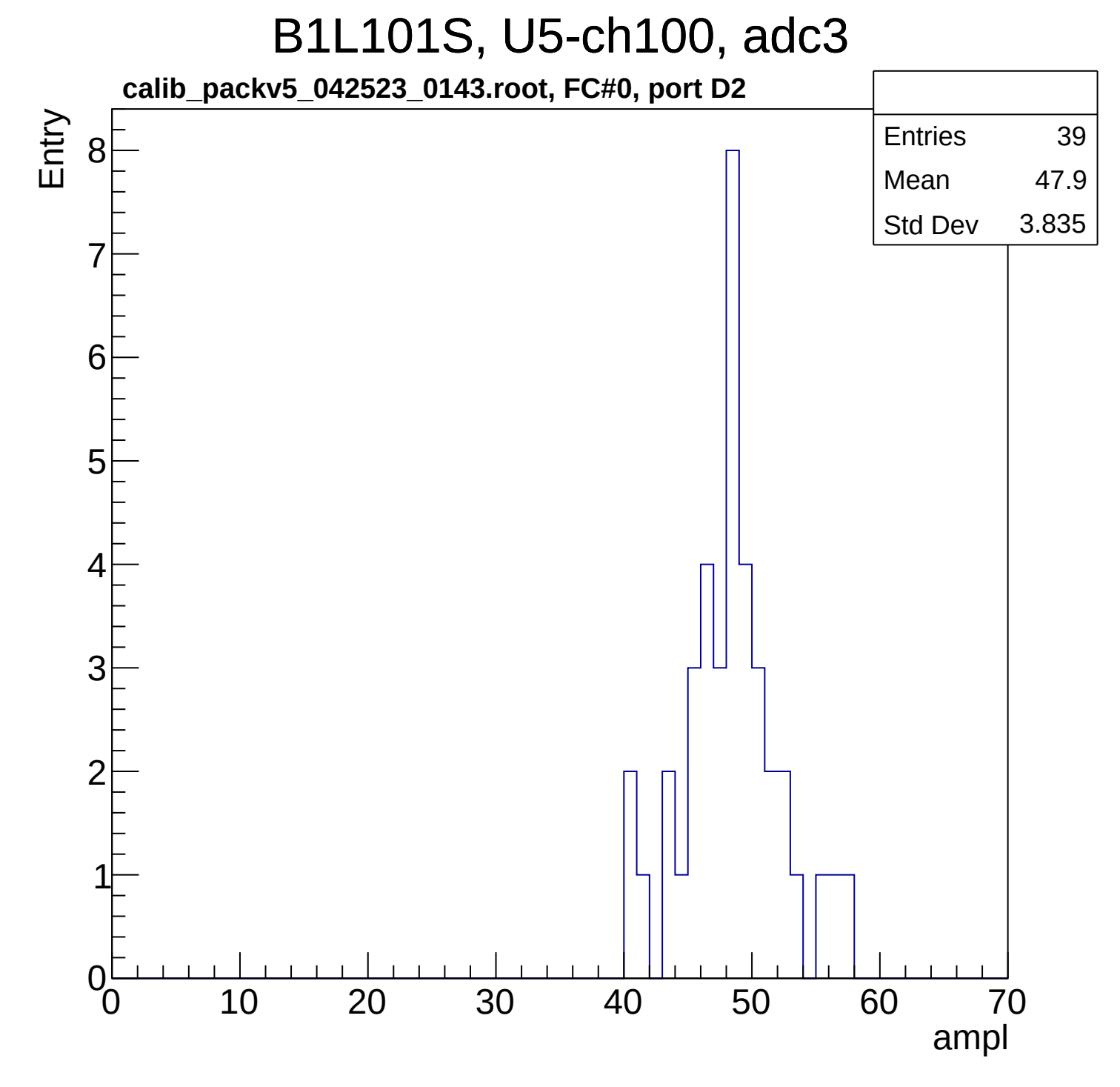
B1L101S, U5-ch100, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 39
Mean 47.9
Std Dev 3.835
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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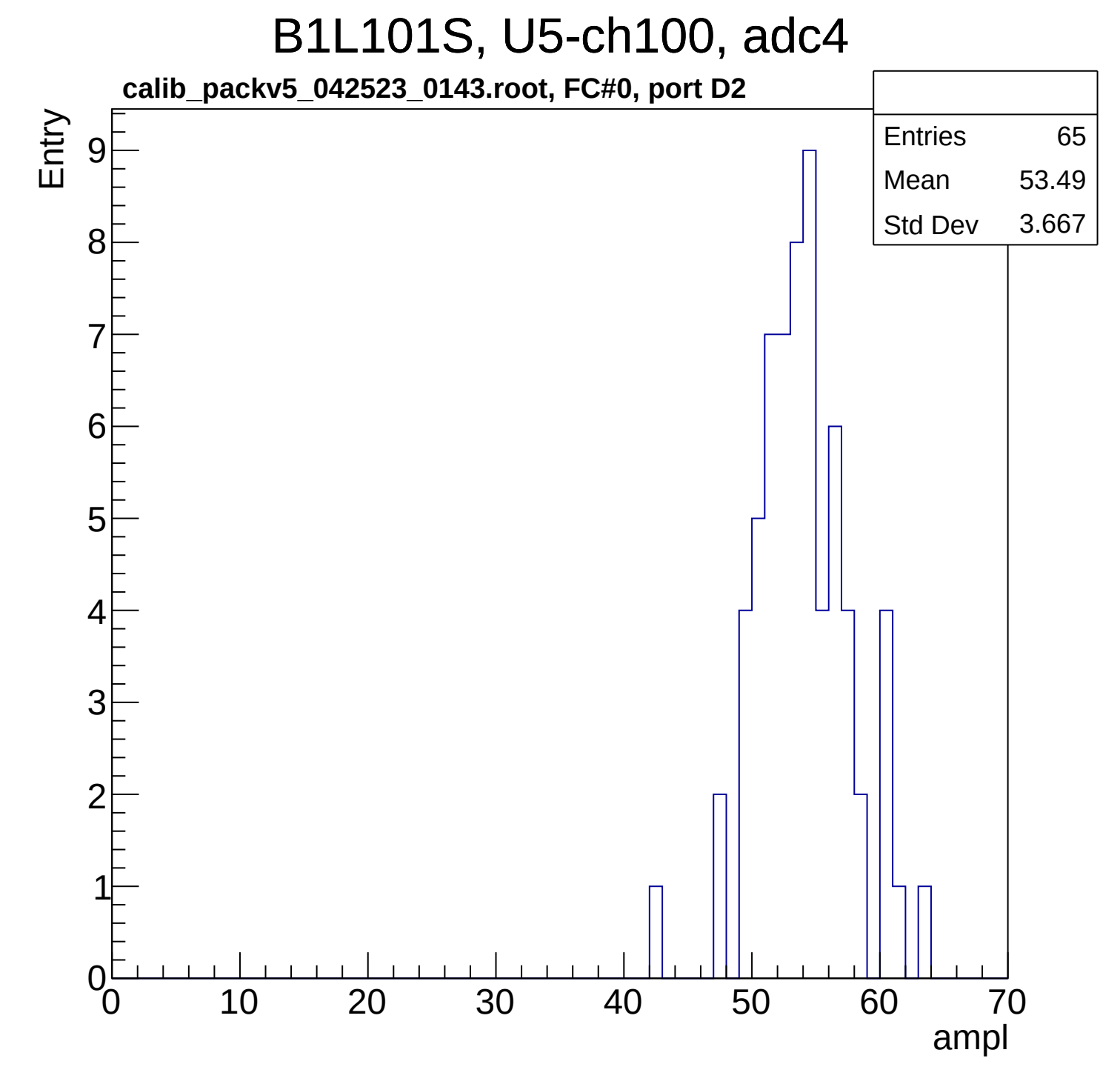
B1L101S, U5-ch100, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 53.49
Std Dev 3.667
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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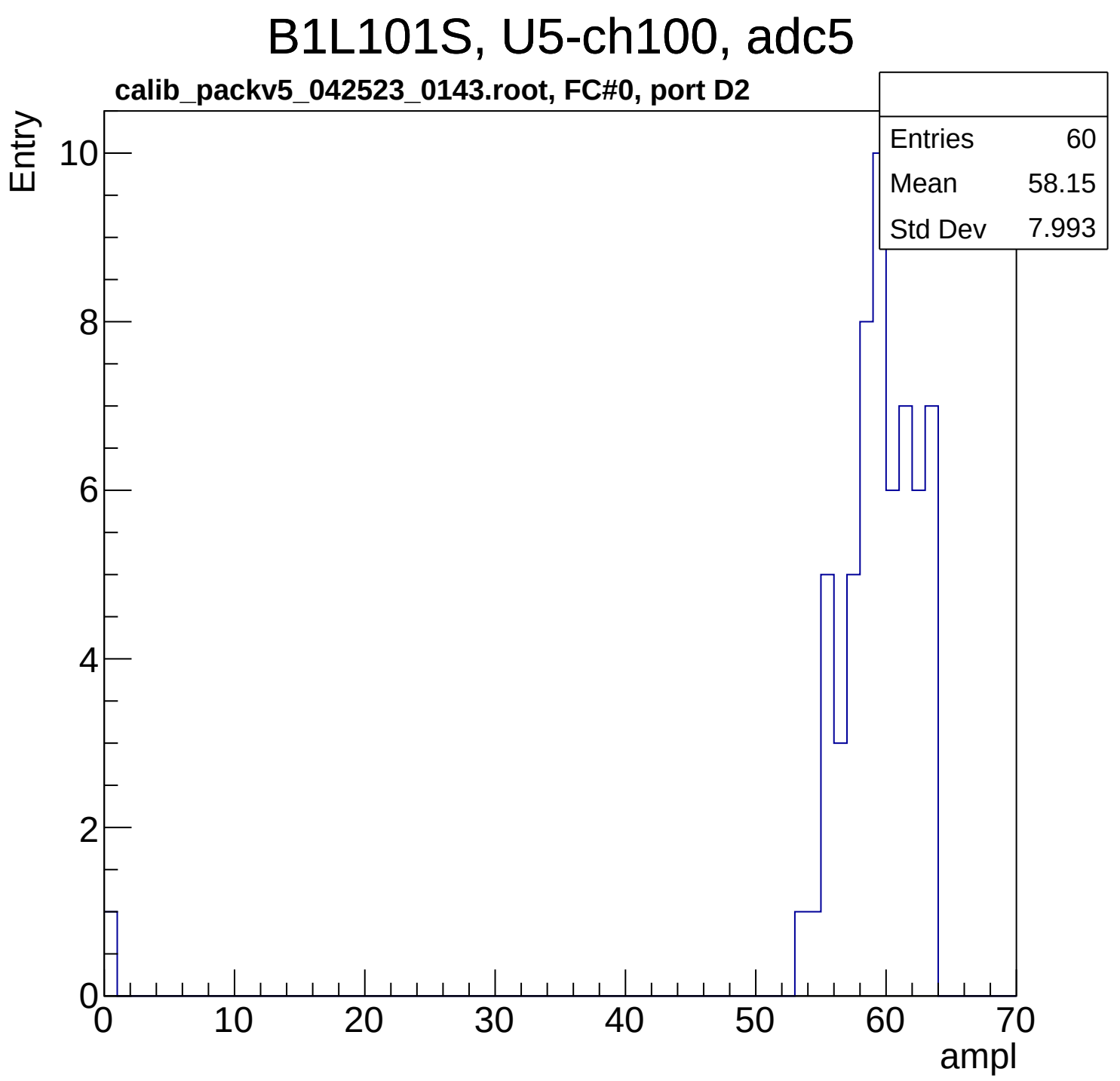
B1L101S, U5-ch100, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 58.15
Std Dev 7.993
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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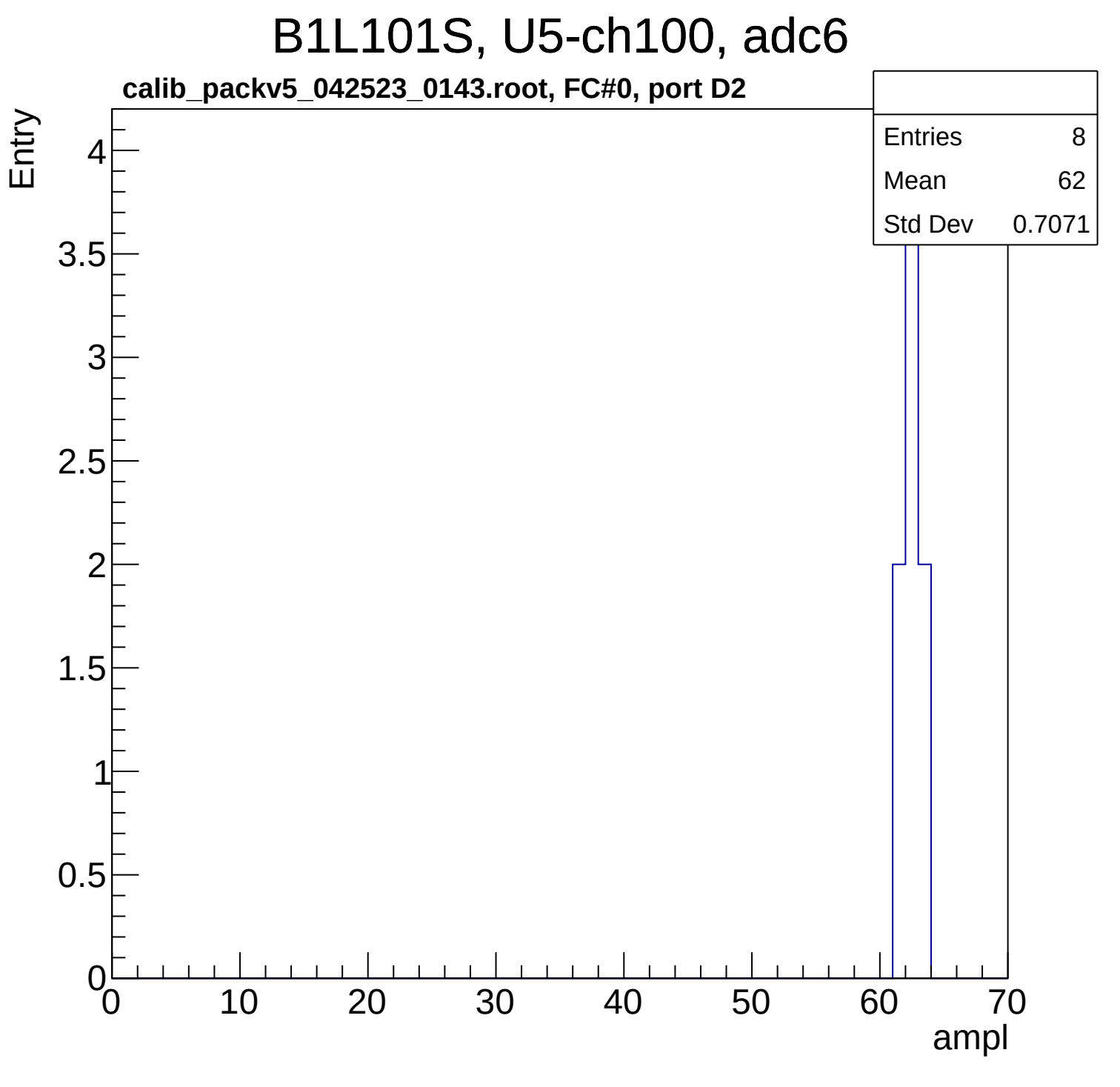
B1L101S, U5-ch100, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 62
Std Dev 0.7071
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
50
60
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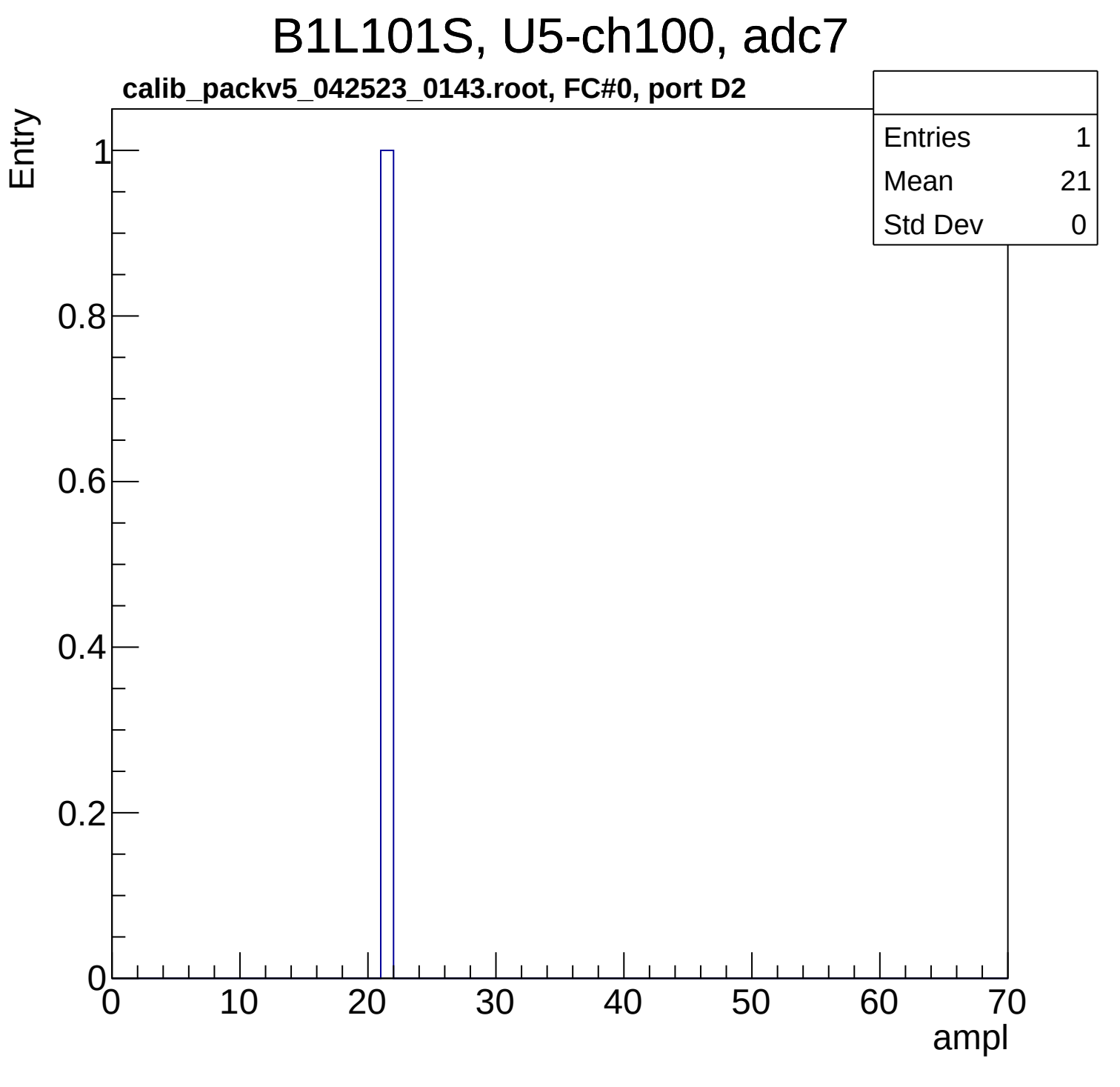
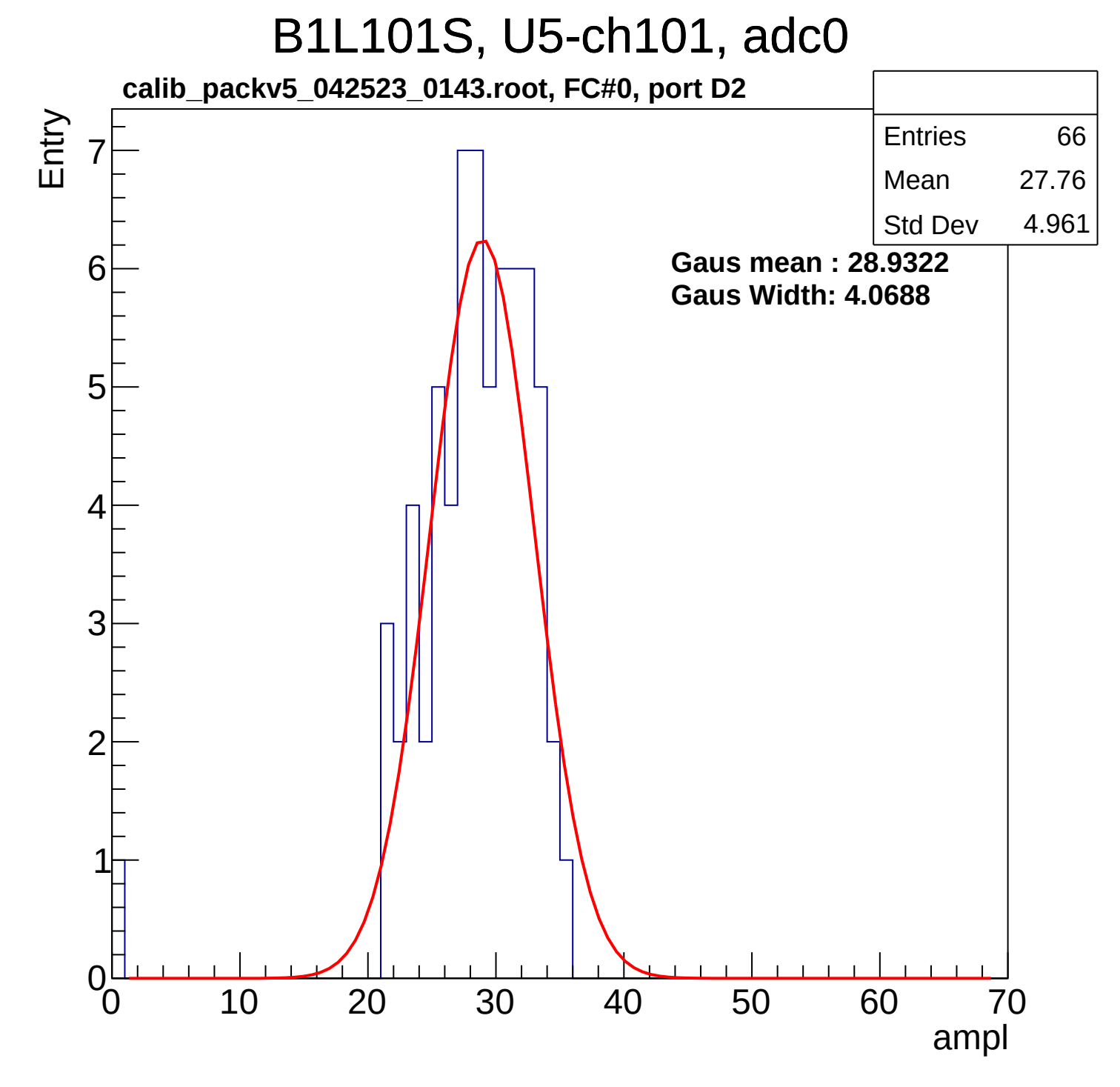
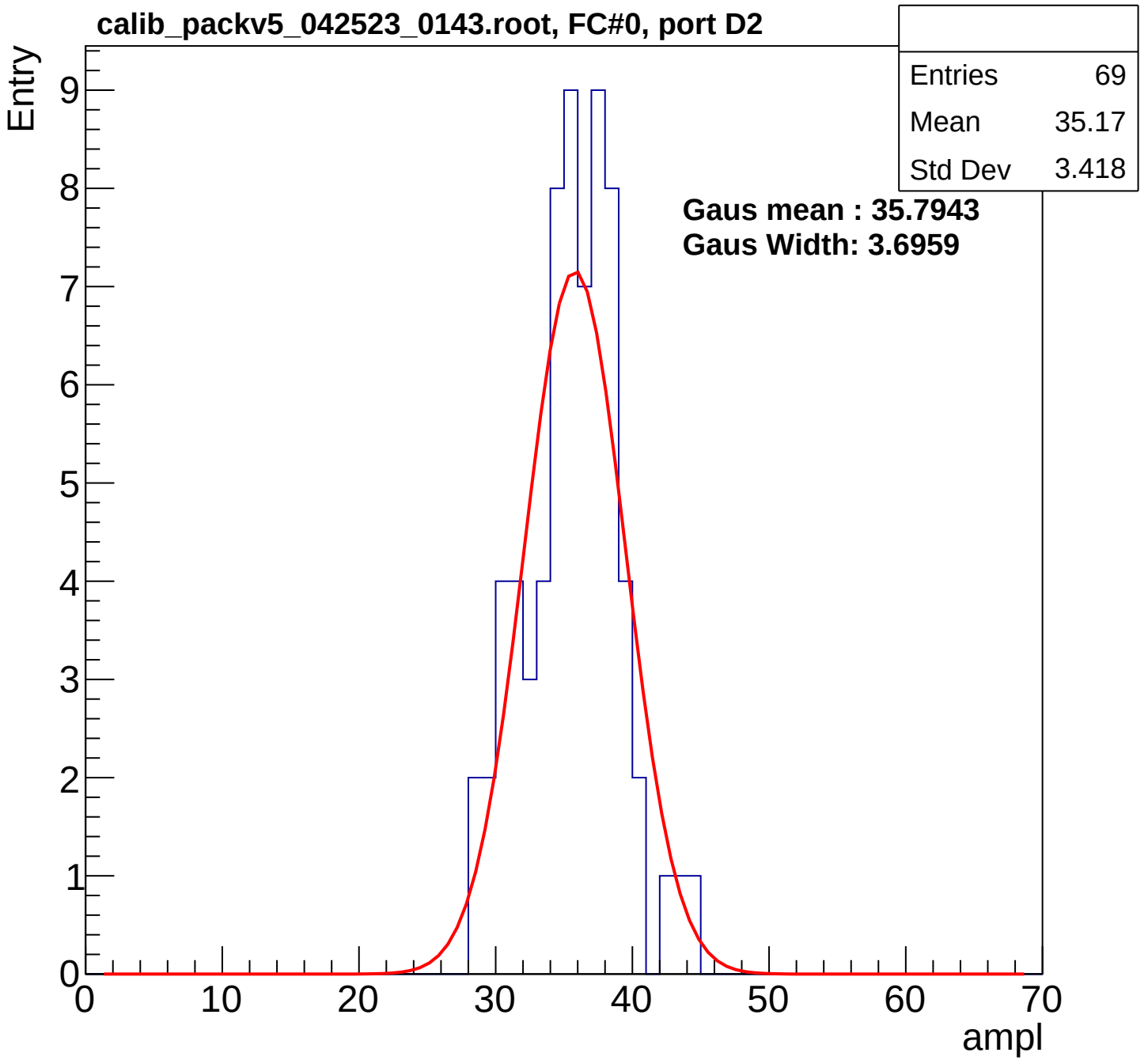

B1L101S, U5-ch100, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 21
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch101, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 27.76
Std Dev 4.961
Gaus mean : 28.9322
Gaus Width: 4.0688
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch101, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 35.17
Std Dev 3.418
Gaus mean : 35.7943
Gaus Width: 3.6959
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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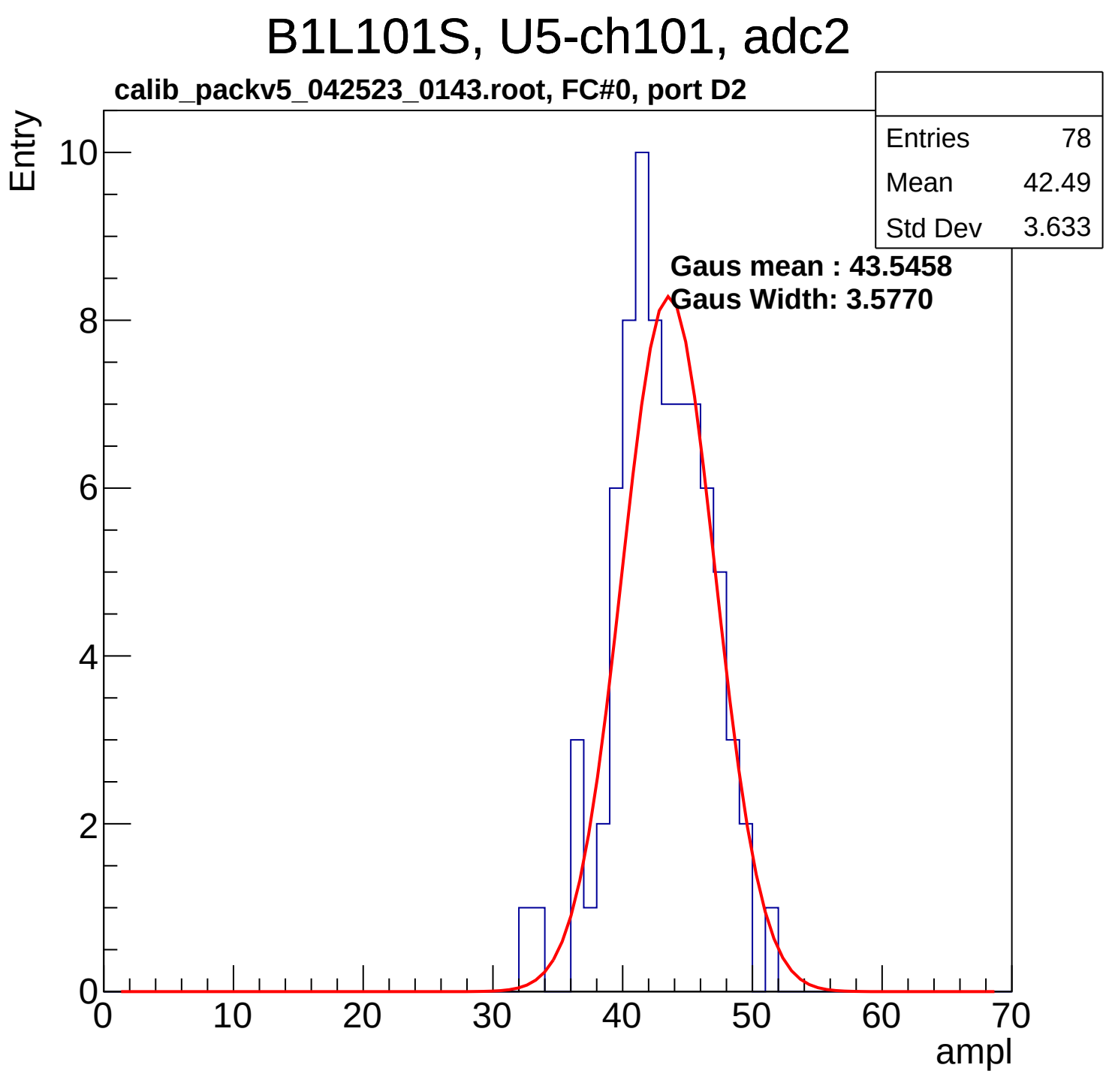
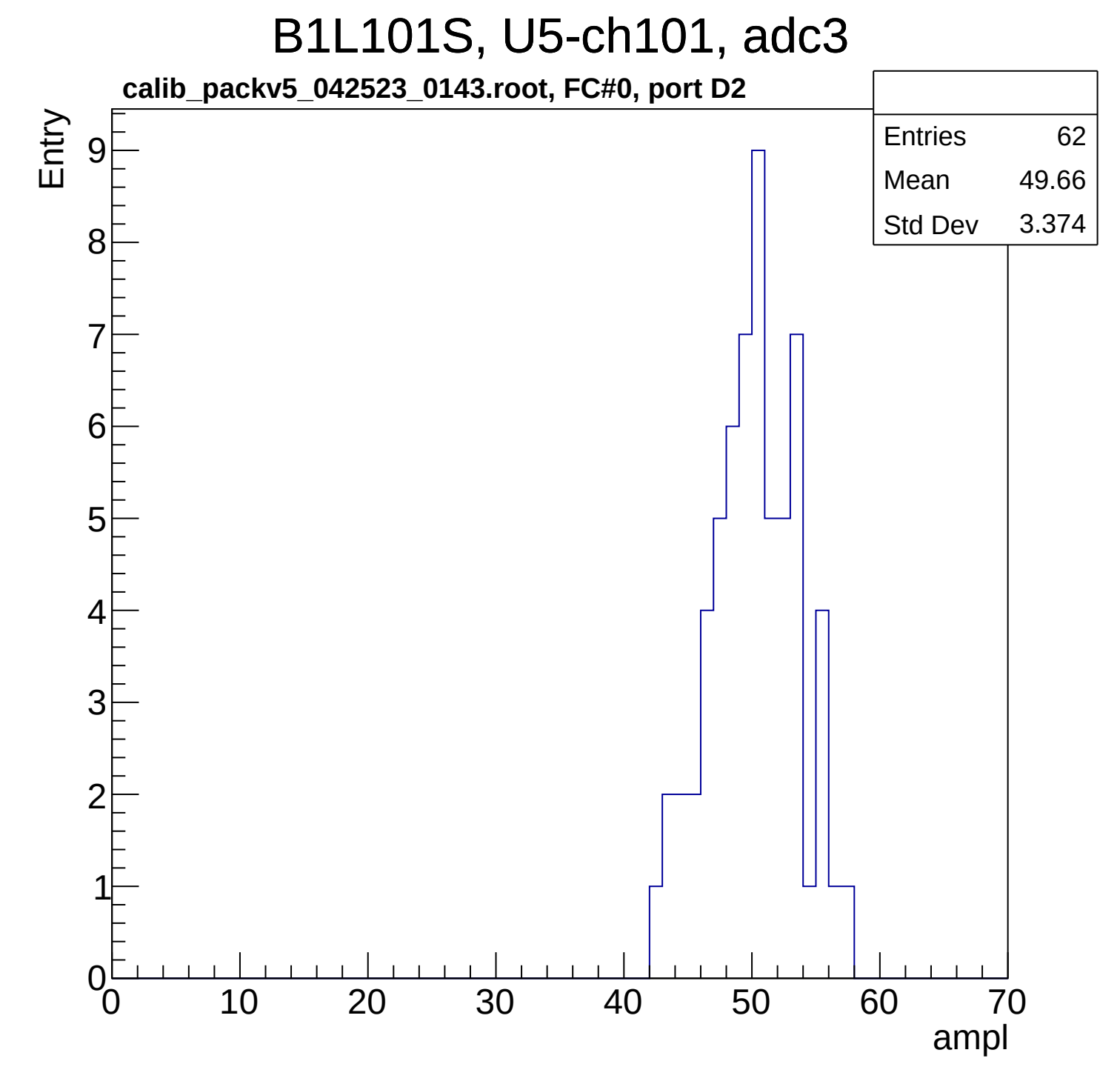

B1L101S, U5-ch101, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 42.49
Std Dev 3.633
Gaus mean : 43.5458
Gaus Width: 3.5770
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch101, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 49.66
Std Dev 3.374
Entry
ampl
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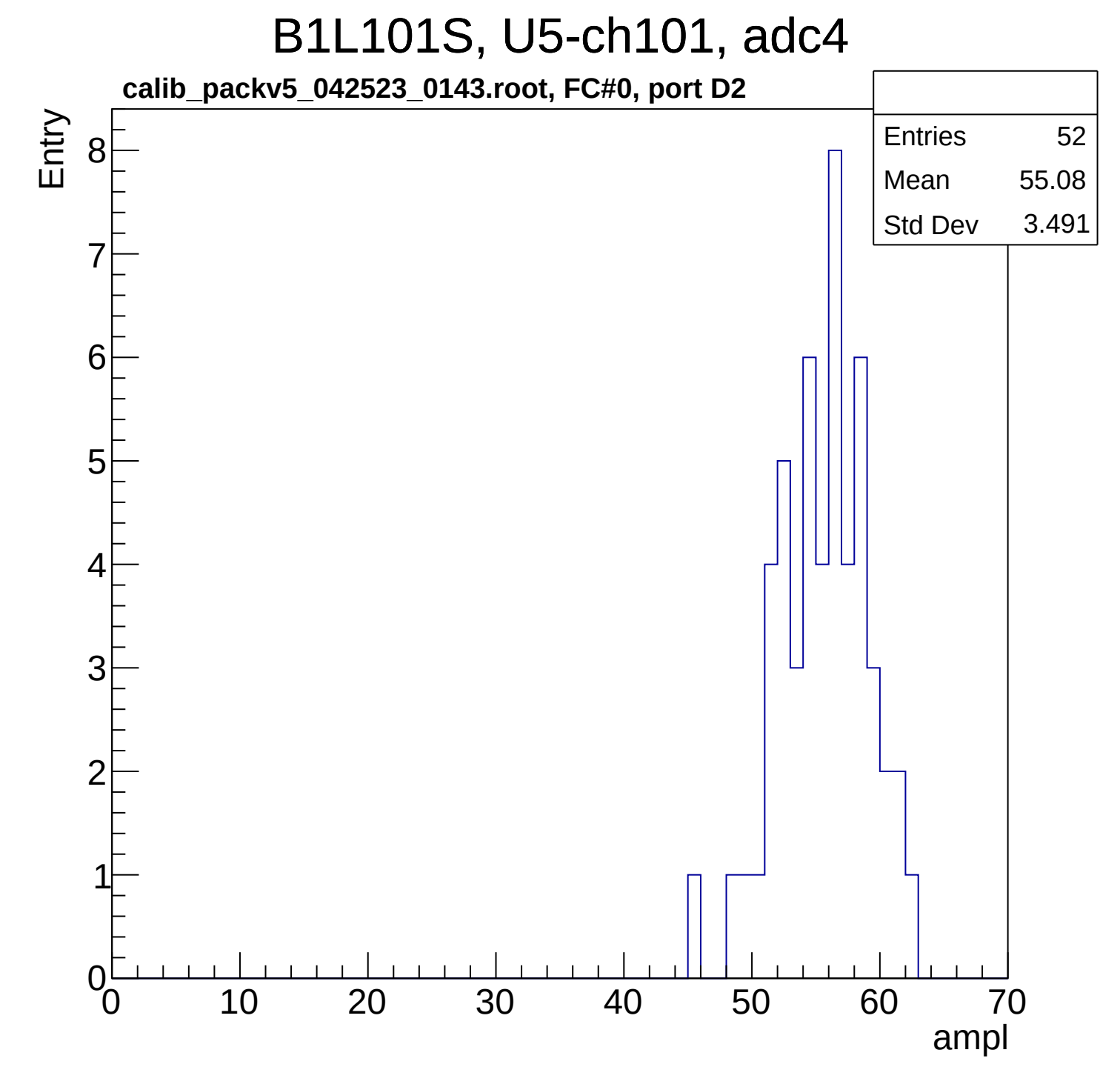
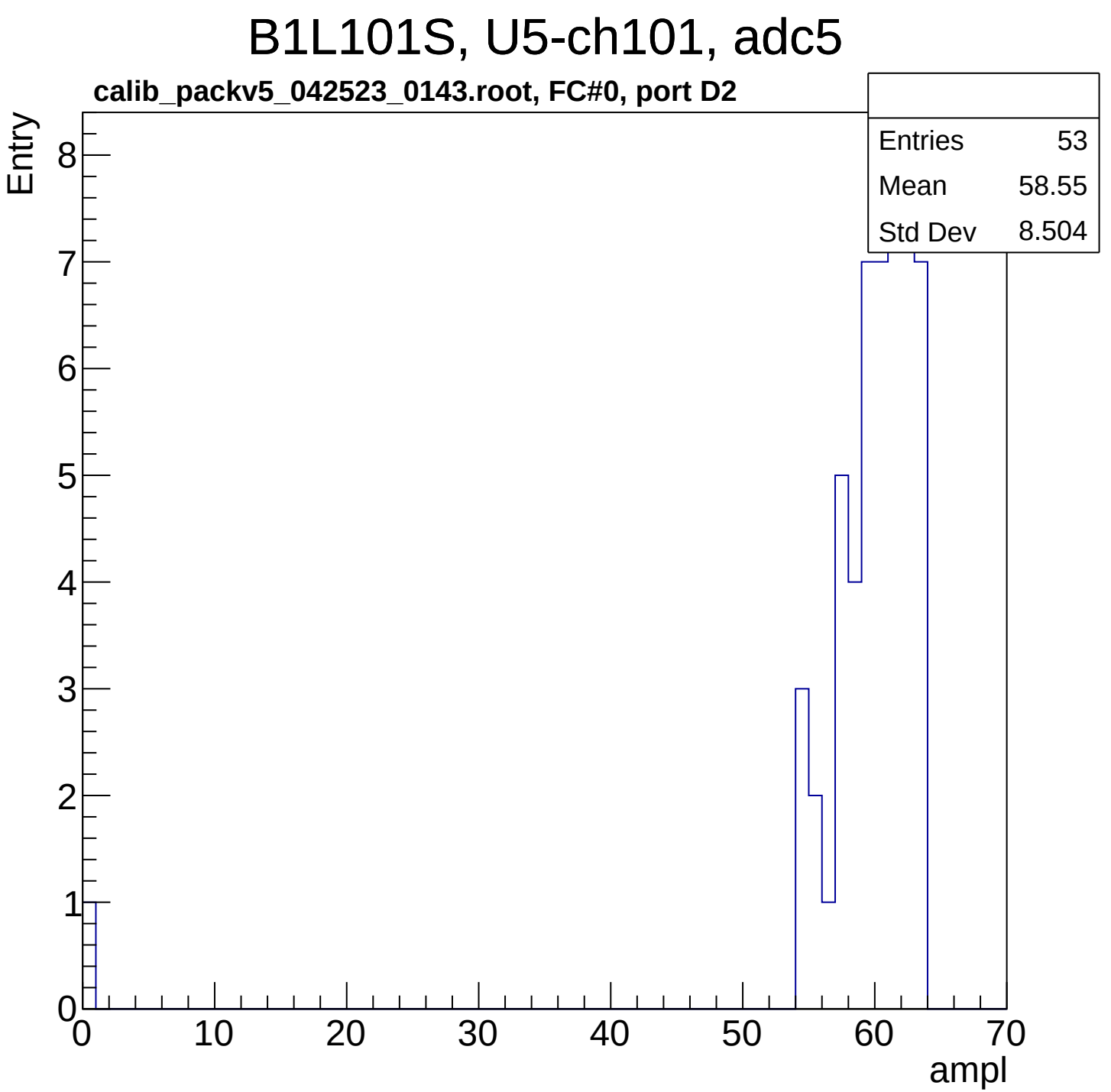
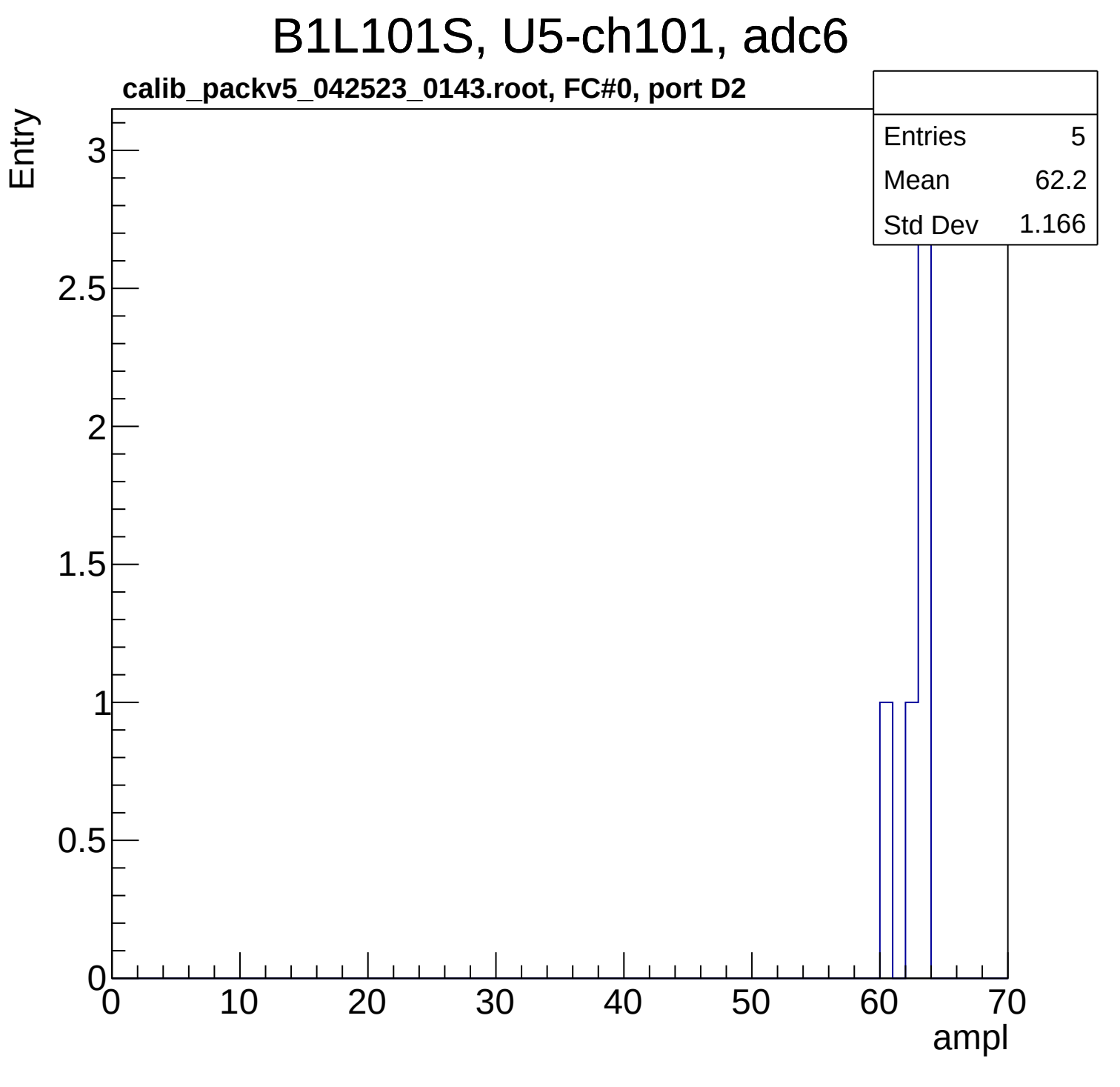
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch101, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 55.08
Std Dev 3.491
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch101, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 58.55
Std Dev 8.504
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch101, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 62.2
Std Dev 1.166
Entry
ampl
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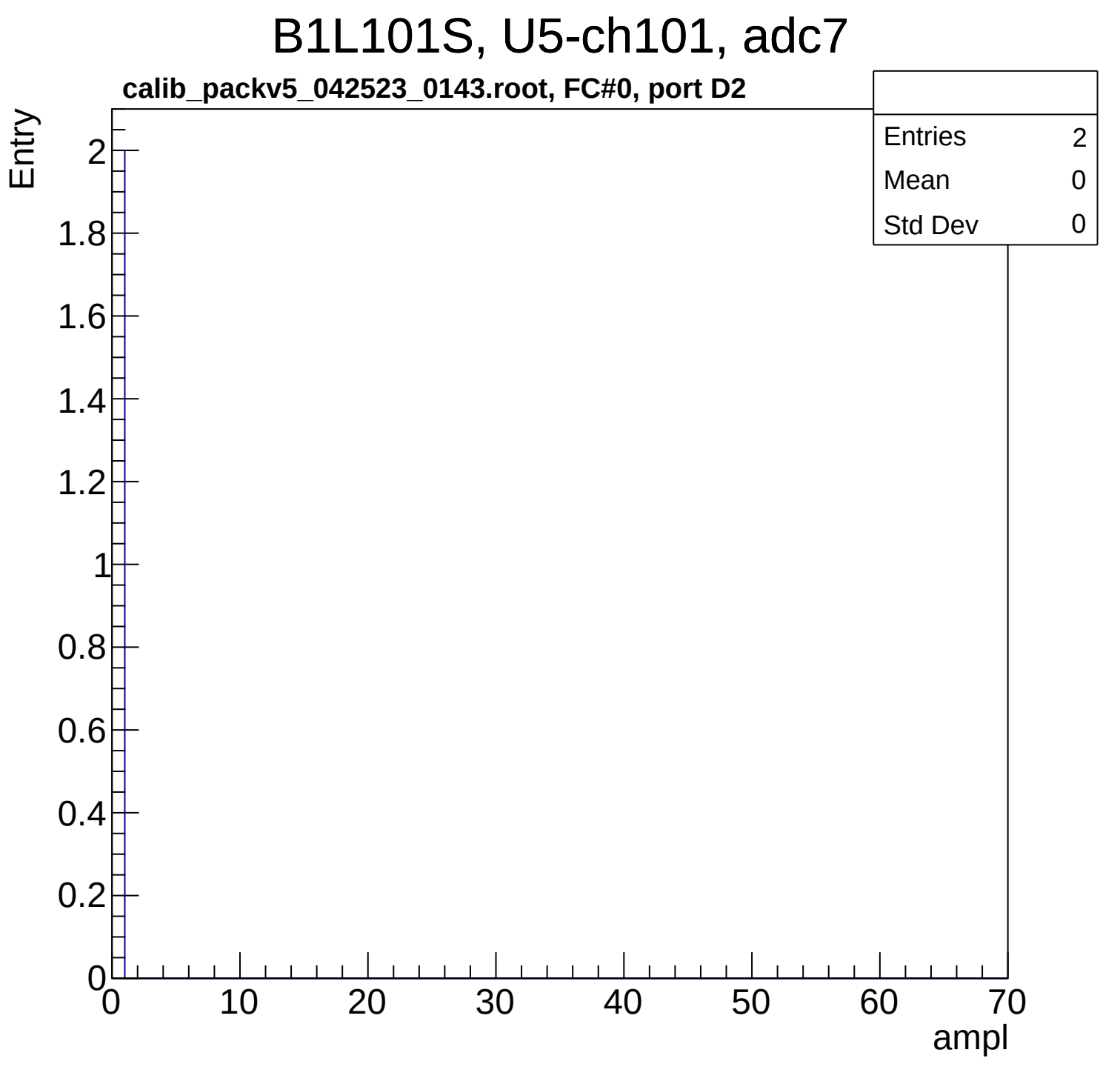
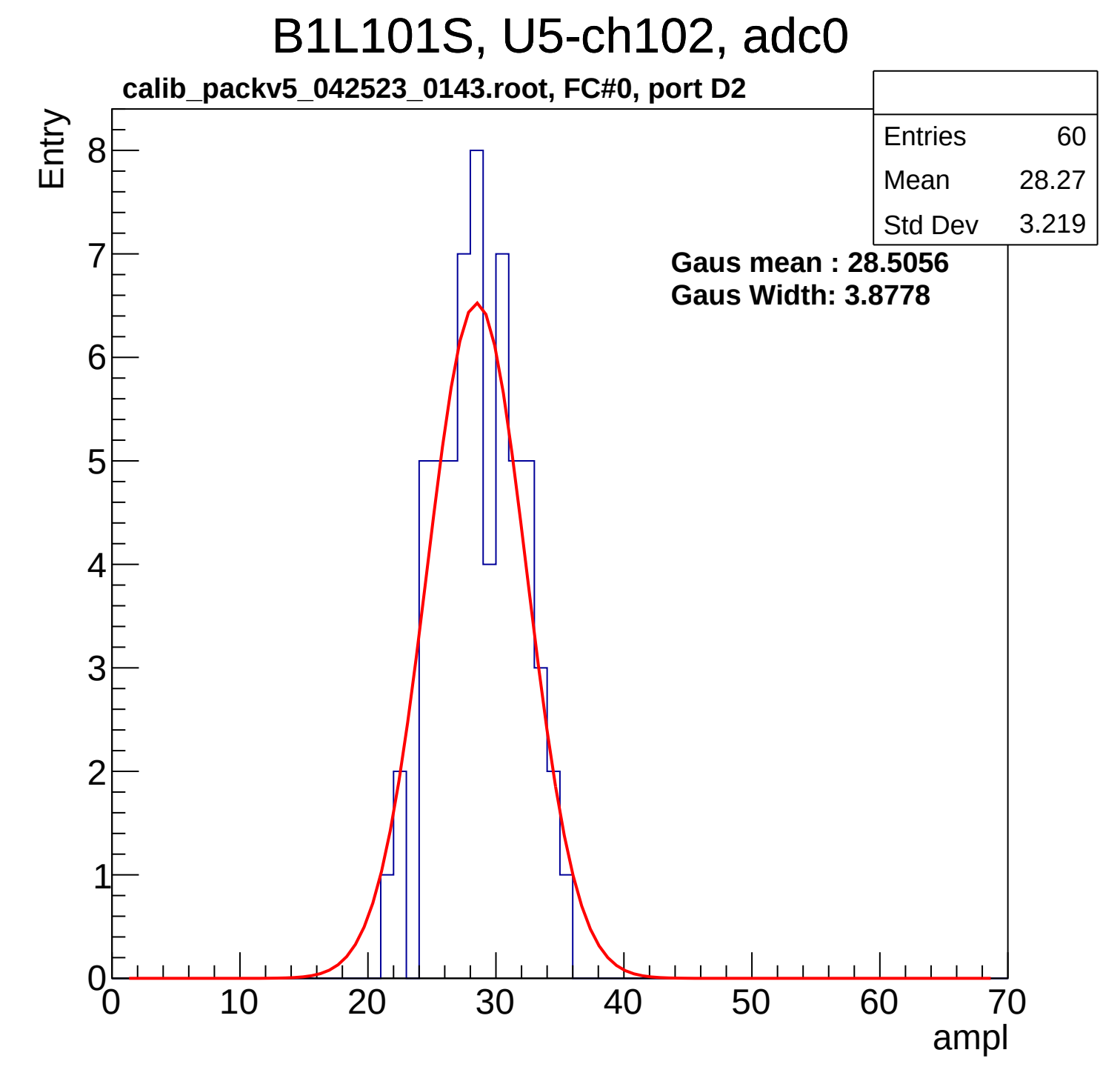
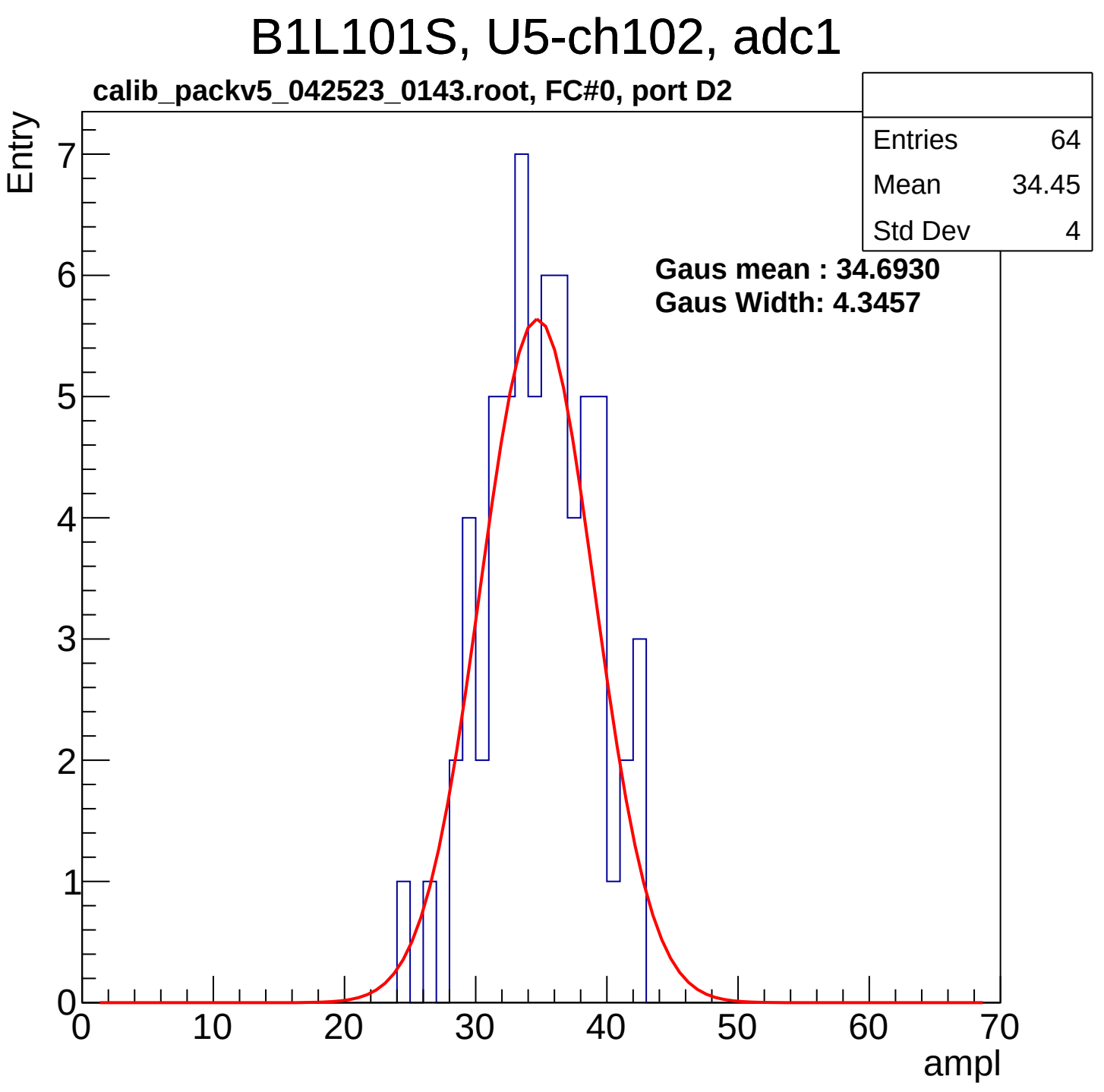
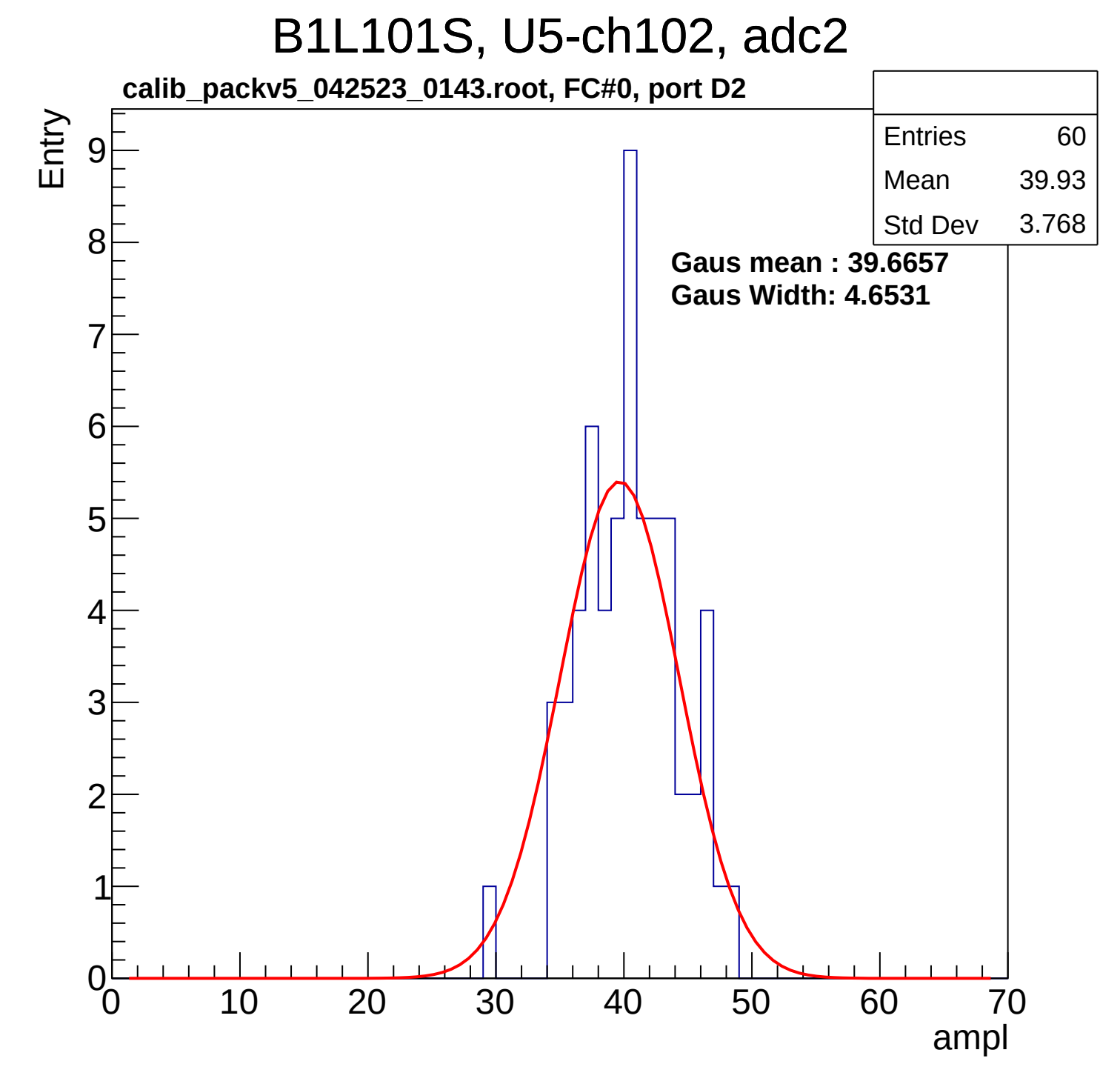
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U5-ch101, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch102, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 28.27
Std Dev 3.219
Gaus mean : 28.5056
Gaus Width: 3.8778
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch102, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 34.45
Std Dev 4
Gaus mean : 34.6930
Gaus Width: 4.3457
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch102, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 39.93
Std Dev 3.768
Gaus mean : 39.6657
Gaus Width: 4.6531
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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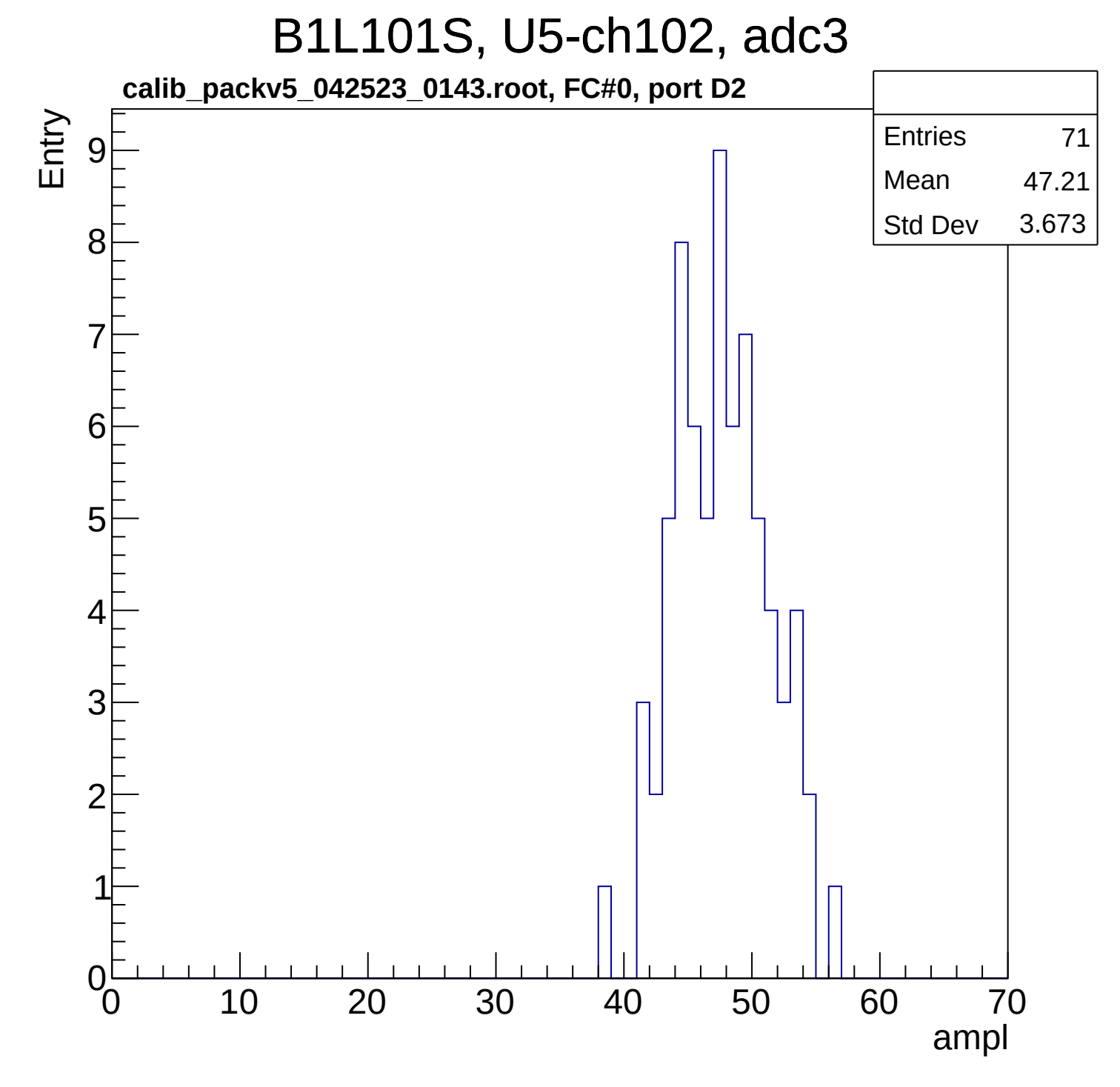
B1L101S, U5-ch102, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 47.21
Std Dev 3.673
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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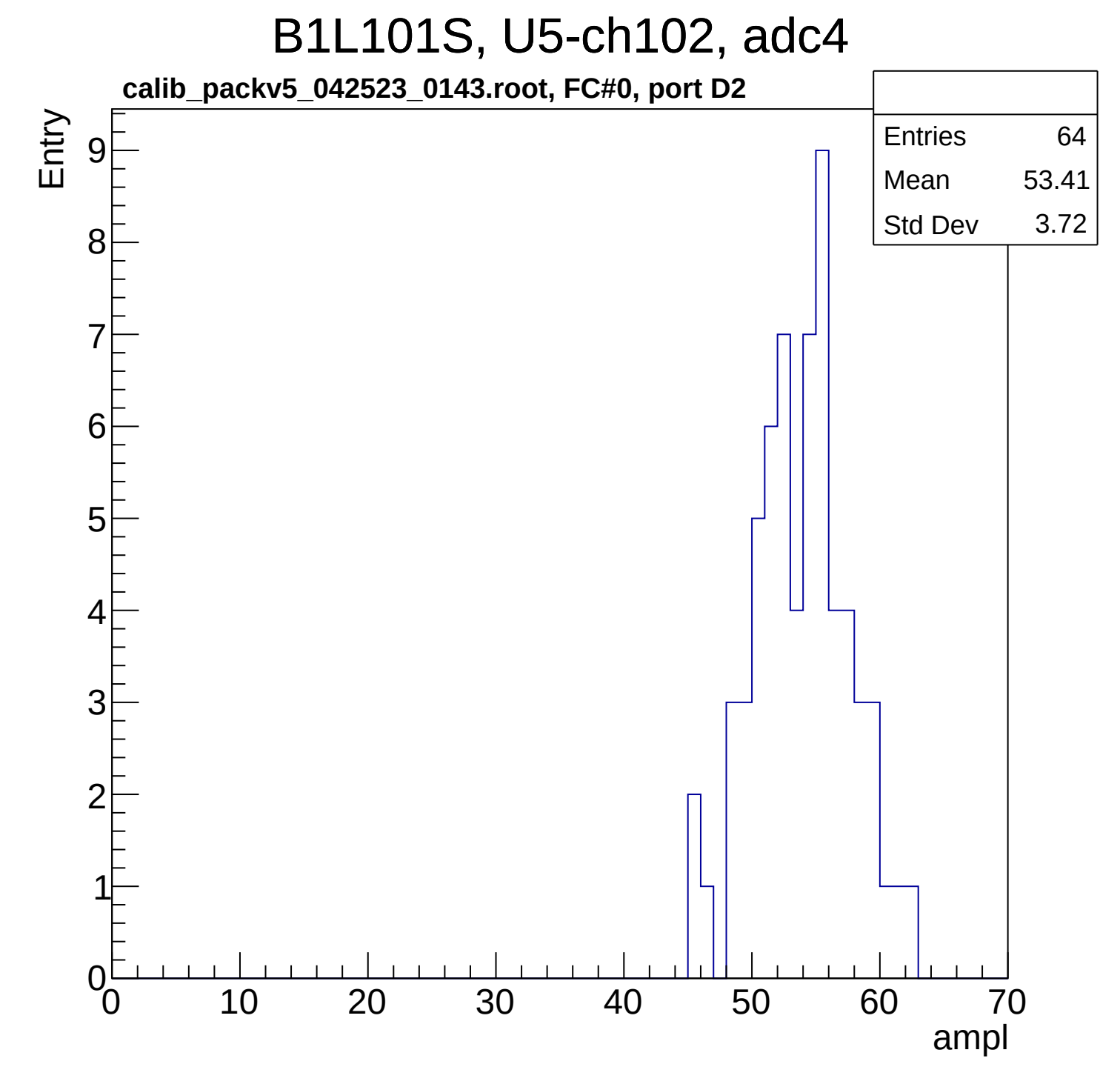
B1L101S, U5-ch102, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 53.41
Std Dev 3.72
Entry
ampl
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3
4
5
6
7
8
9
0
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20
30
40
50
60
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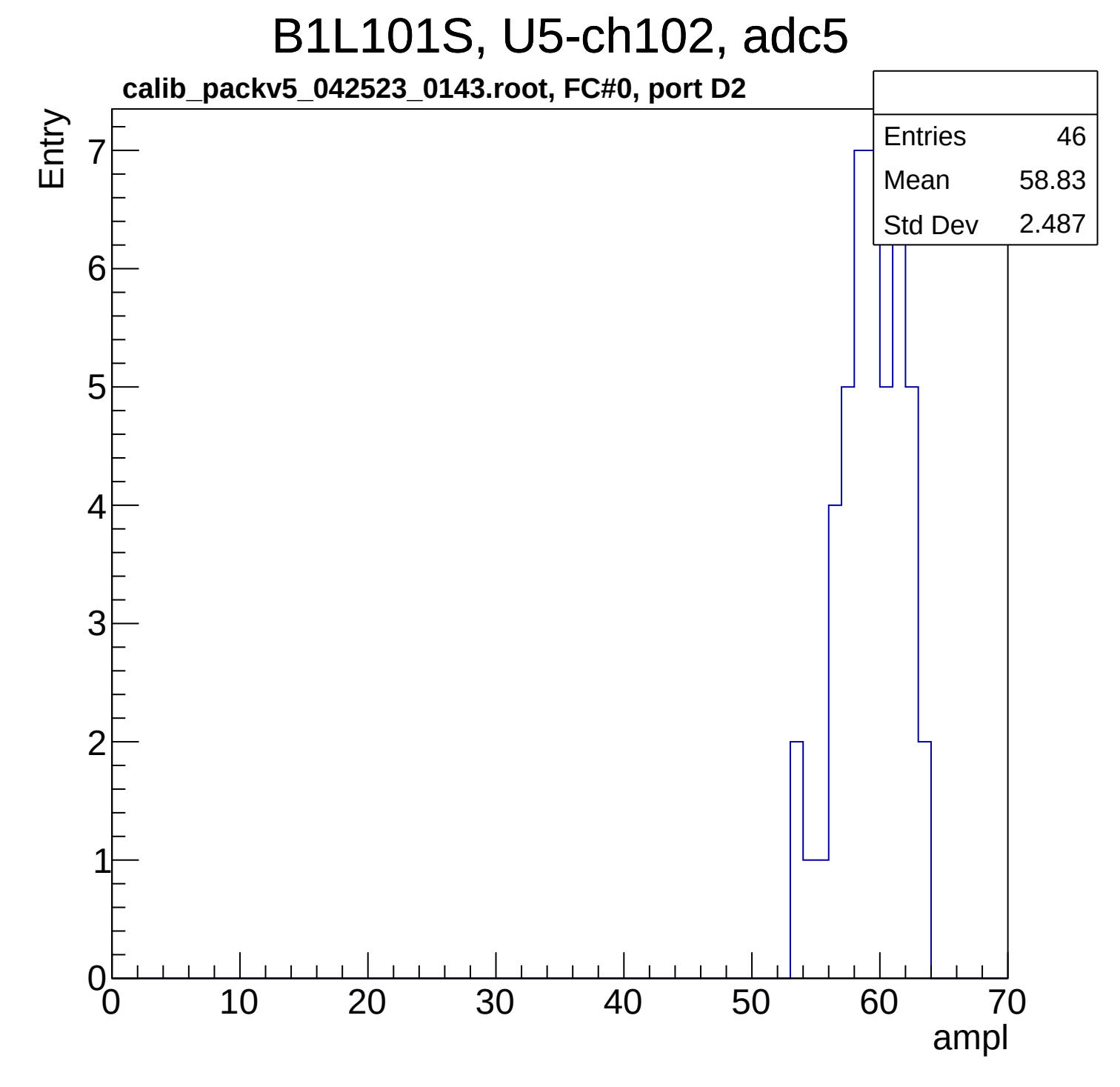
B1L101S, U5-ch102, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 58.83
Std Dev 2.487
Entry
ampl
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1
2
3
4
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6
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20
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40
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60
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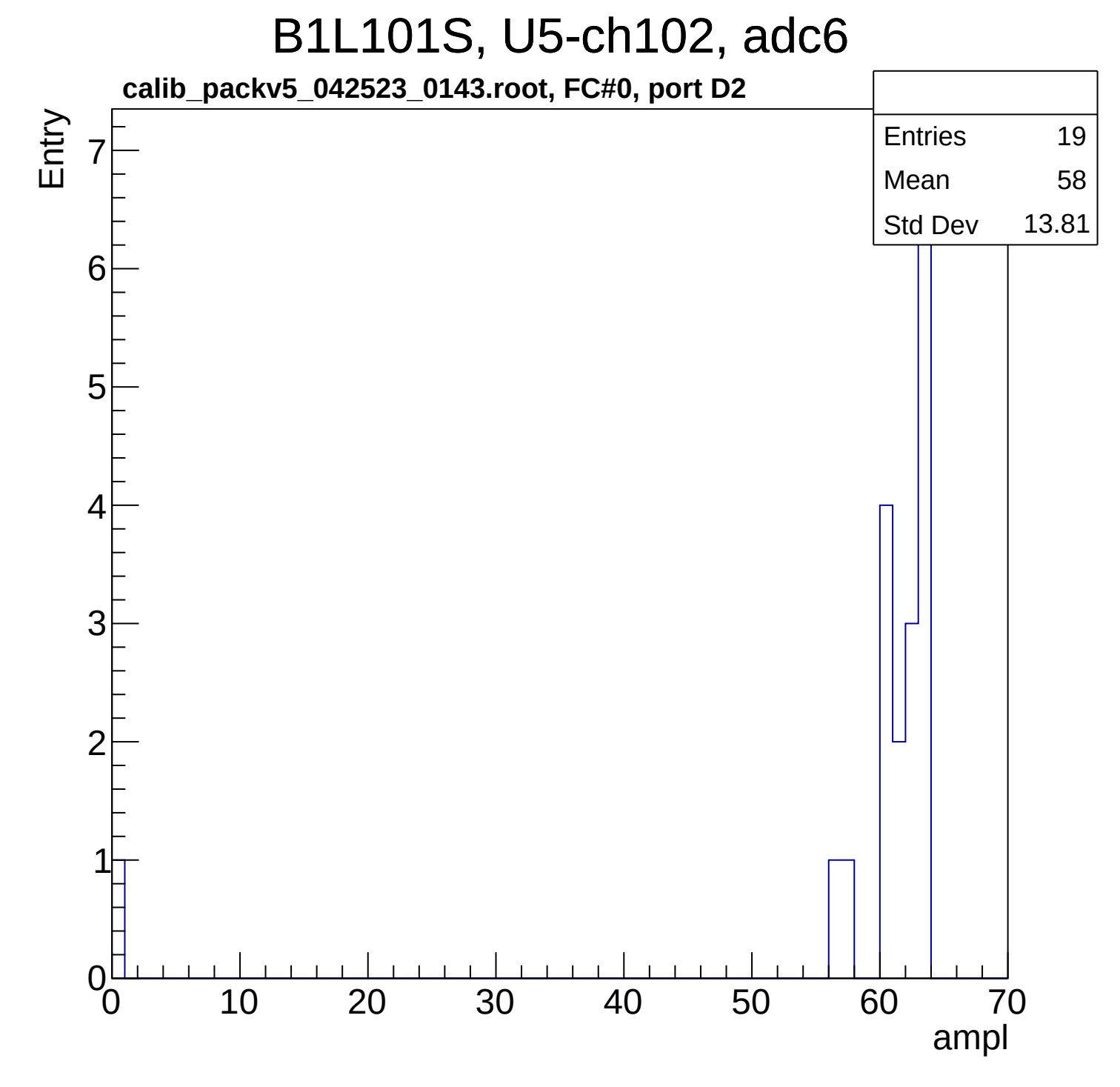
B1L101S, U5-ch102, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 19
Mean 58
Std Dev 13.81
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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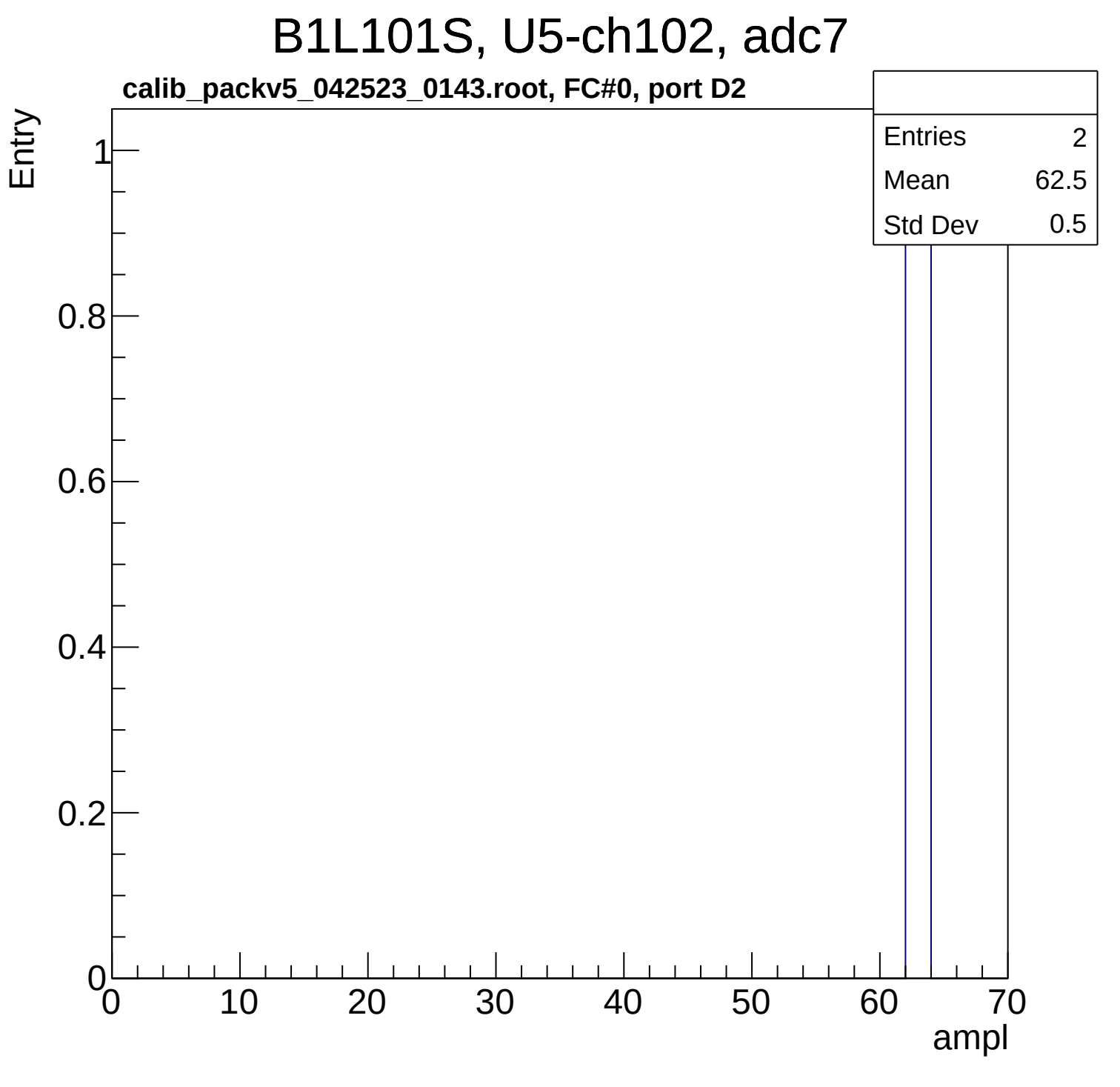
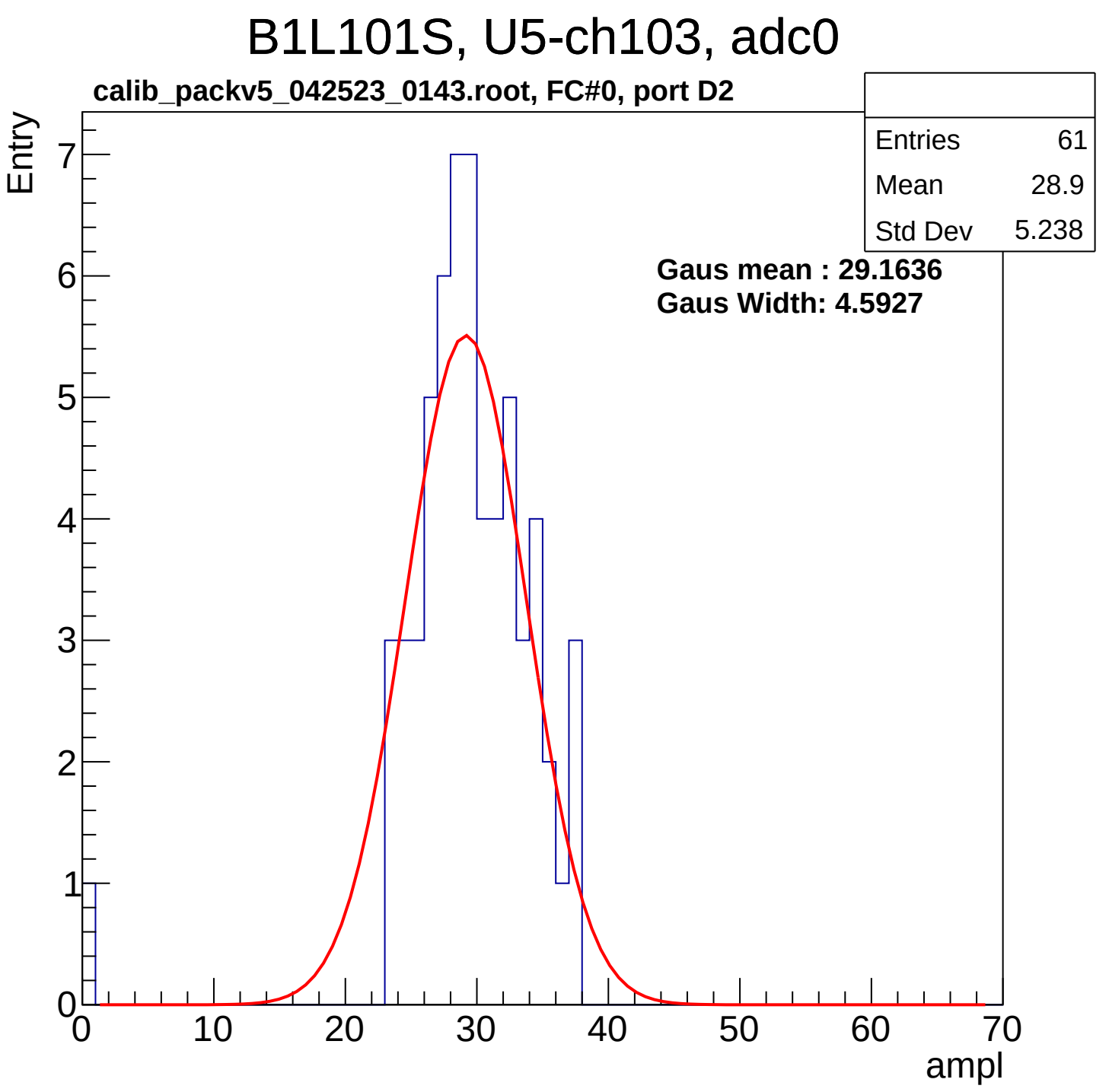
40
50
60
70


B1L101S, U5-ch102, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch103, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 28.9
Std Dev 5.238
Gaus mean : 29.1636
Gaus Width: 4.5927
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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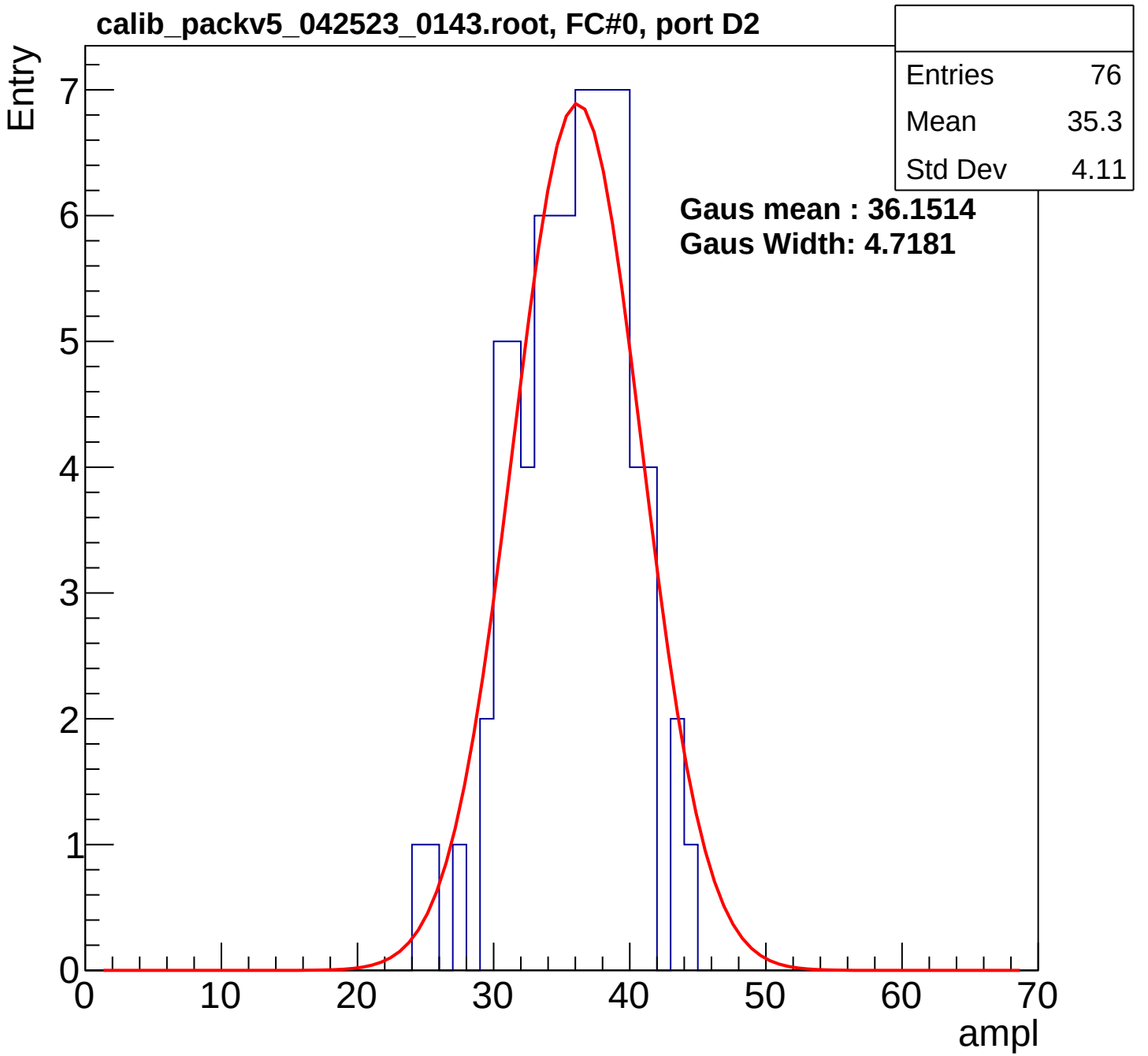
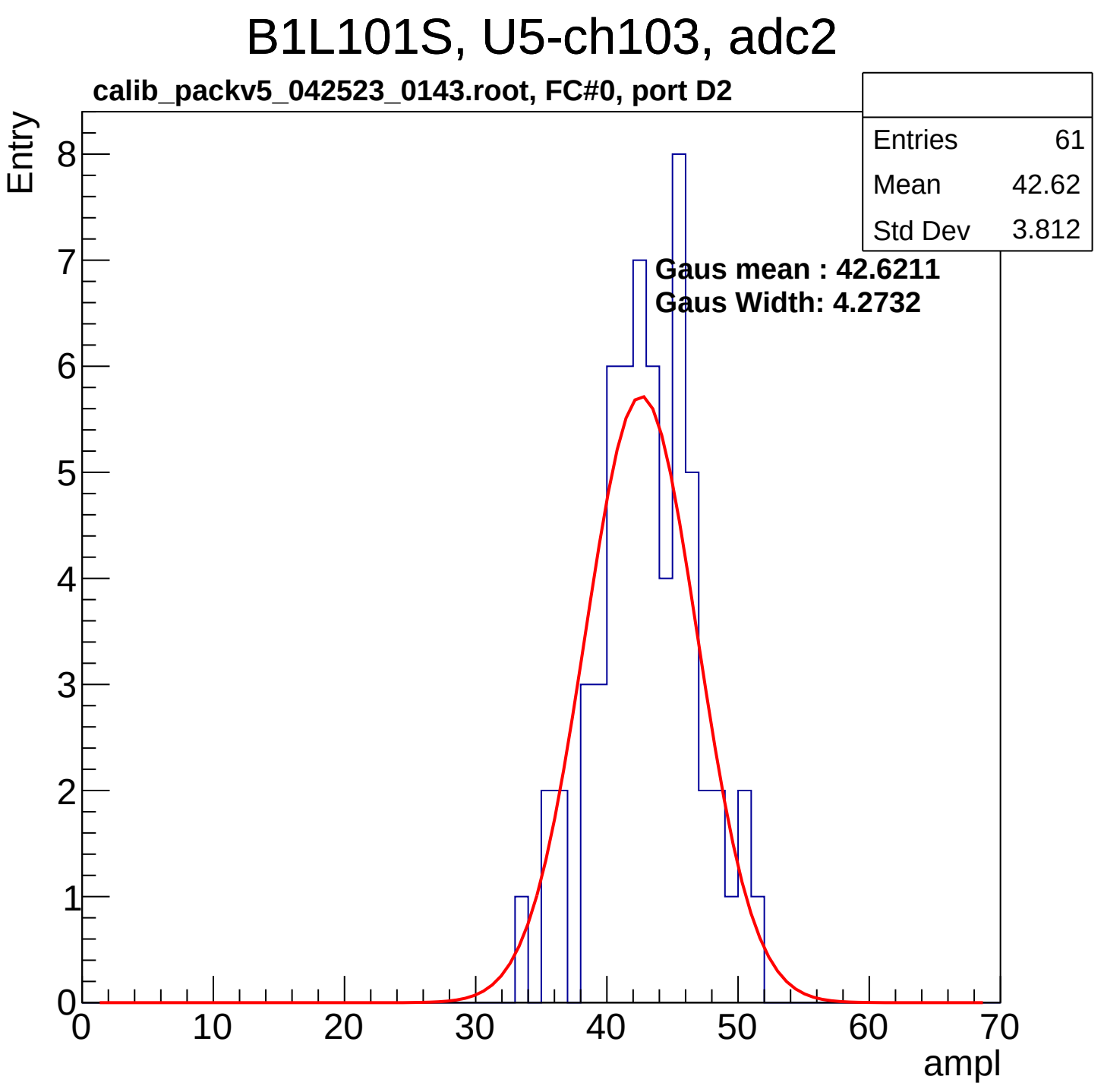
40
50
60
70


B1L101S, U5-ch103, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 35.3
Std Dev 4.11
Gaus mean : 36.1514
Gaus Width: 4.7181
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch103, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 42.62
Std Dev 3.812
Gaus mean : 42.6211
Gaus Width: 4.2732
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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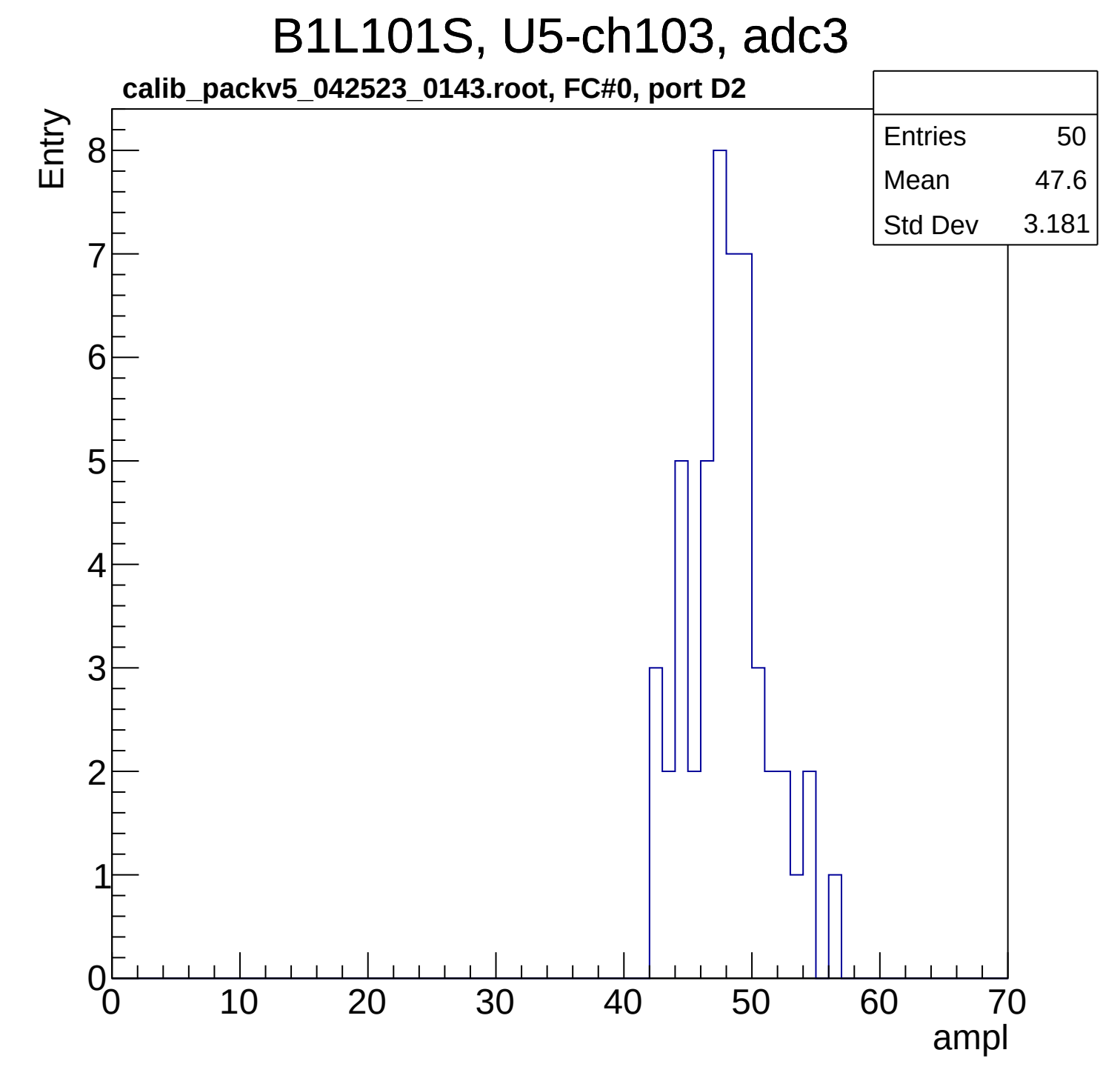
B1L101S, U5-ch103, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 47.6
Std Dev 3.181
Entry
ampl
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1
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3
4
5
6
7
8
0
10
20
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40
50
60
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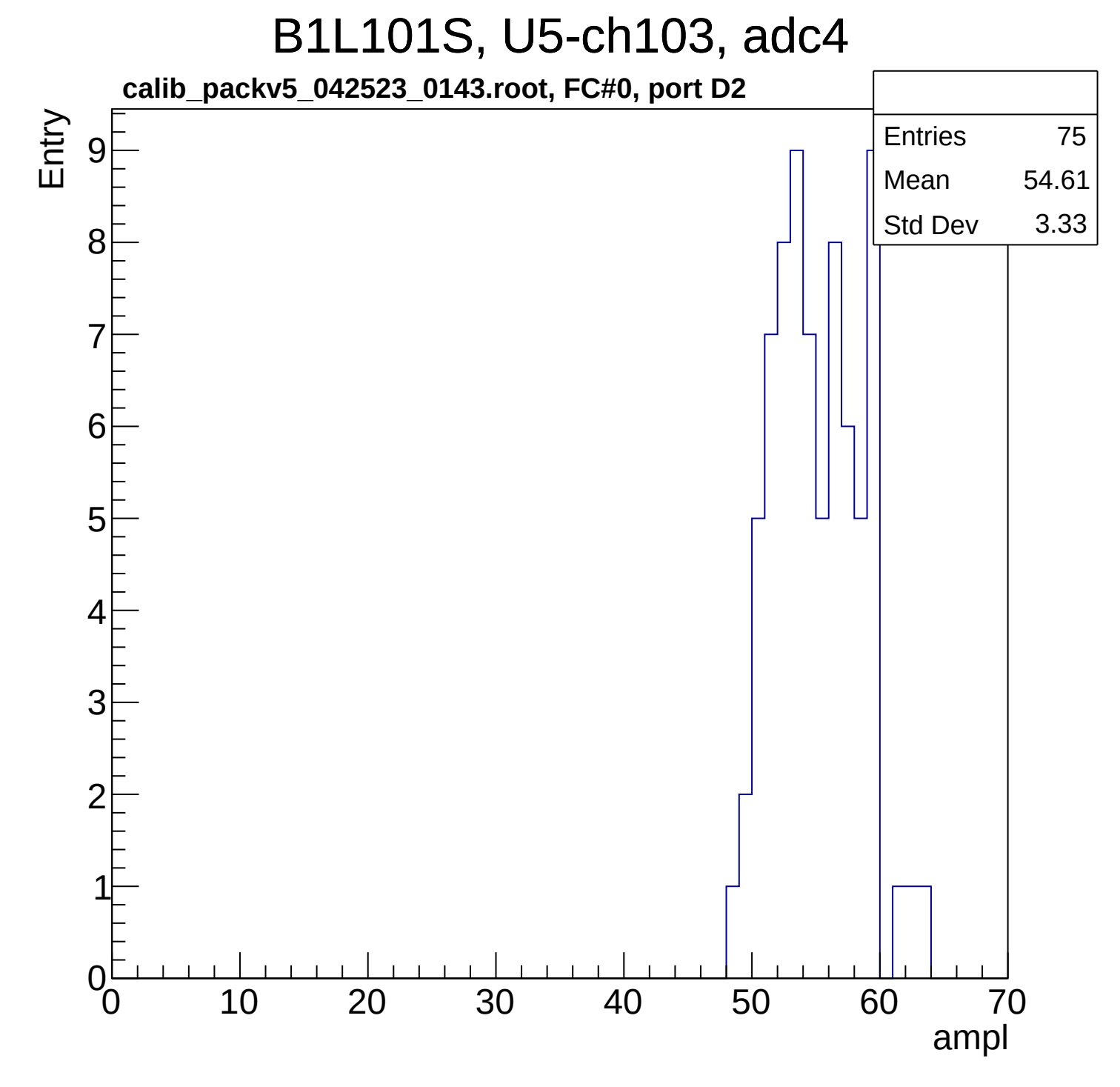
B1L101S, U5-ch103, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 54.61
Std Dev 3.33
Entry
ampl
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3
4
5
6
7
8
9
0
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60
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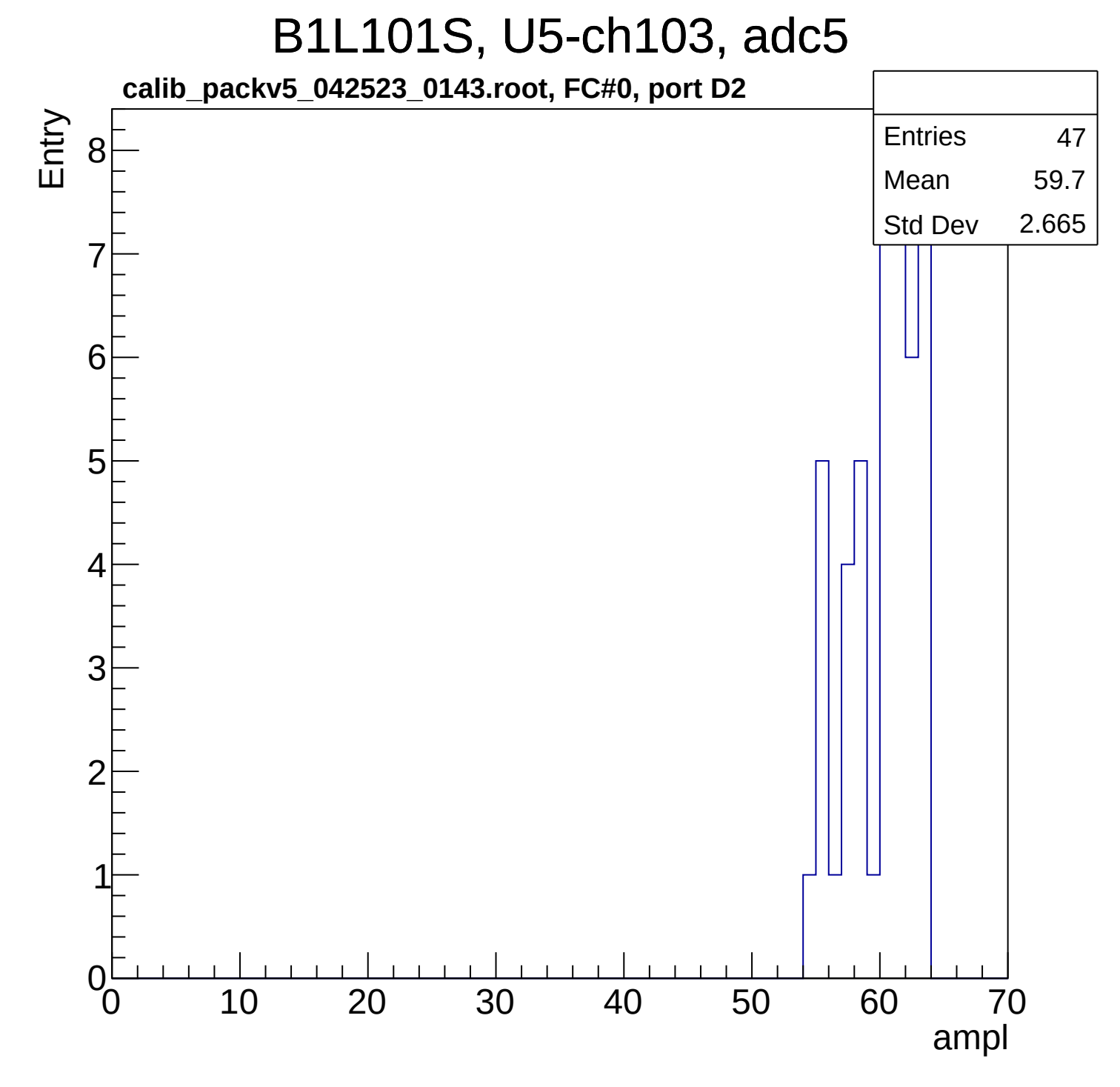
B1L101S, U5-ch103, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 59.7
Std Dev 2.665
Entry
ampl
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4
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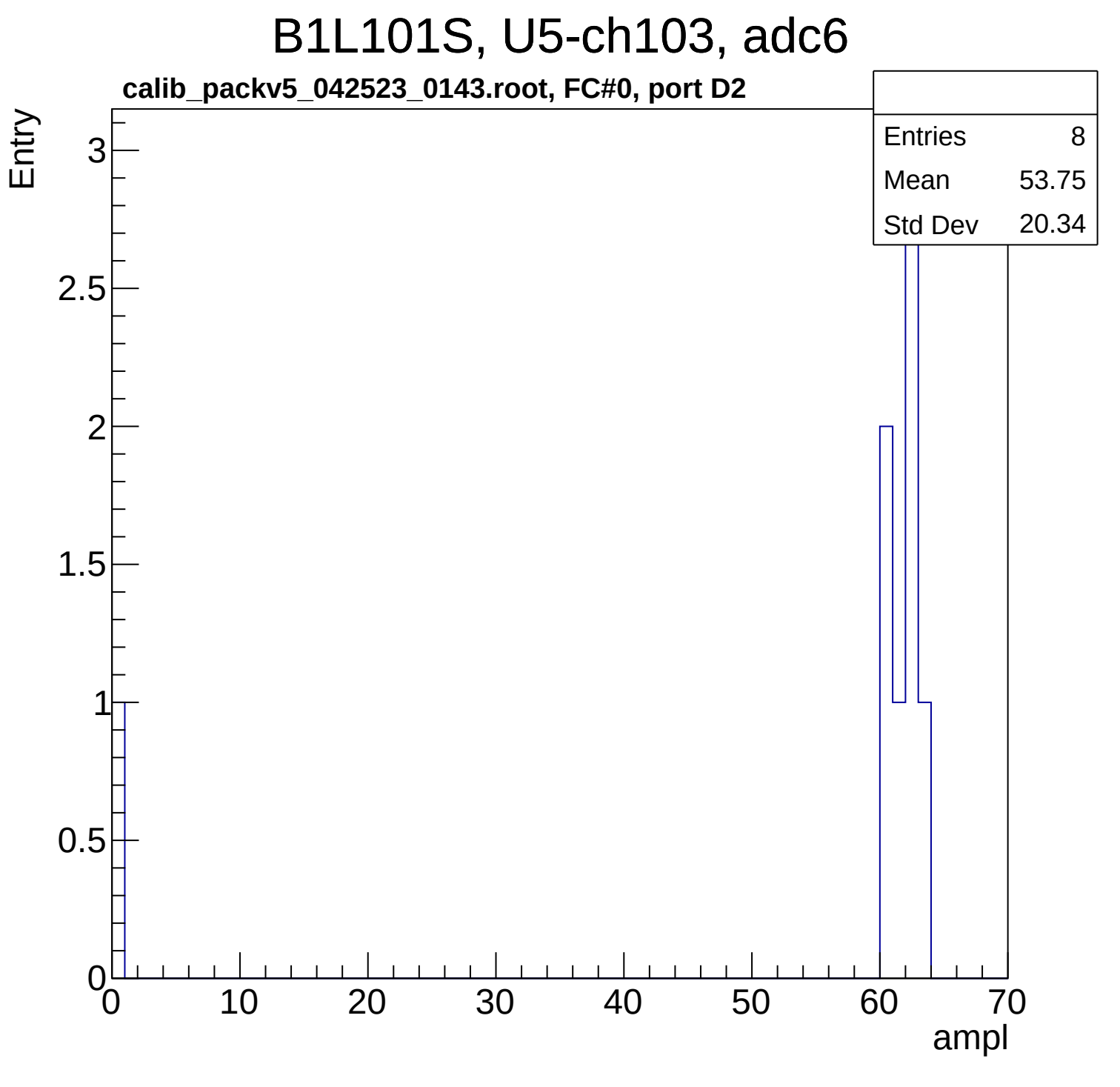
B1L101S, U5-ch103, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 53.75
Std Dev 20.34
Entry
ampl
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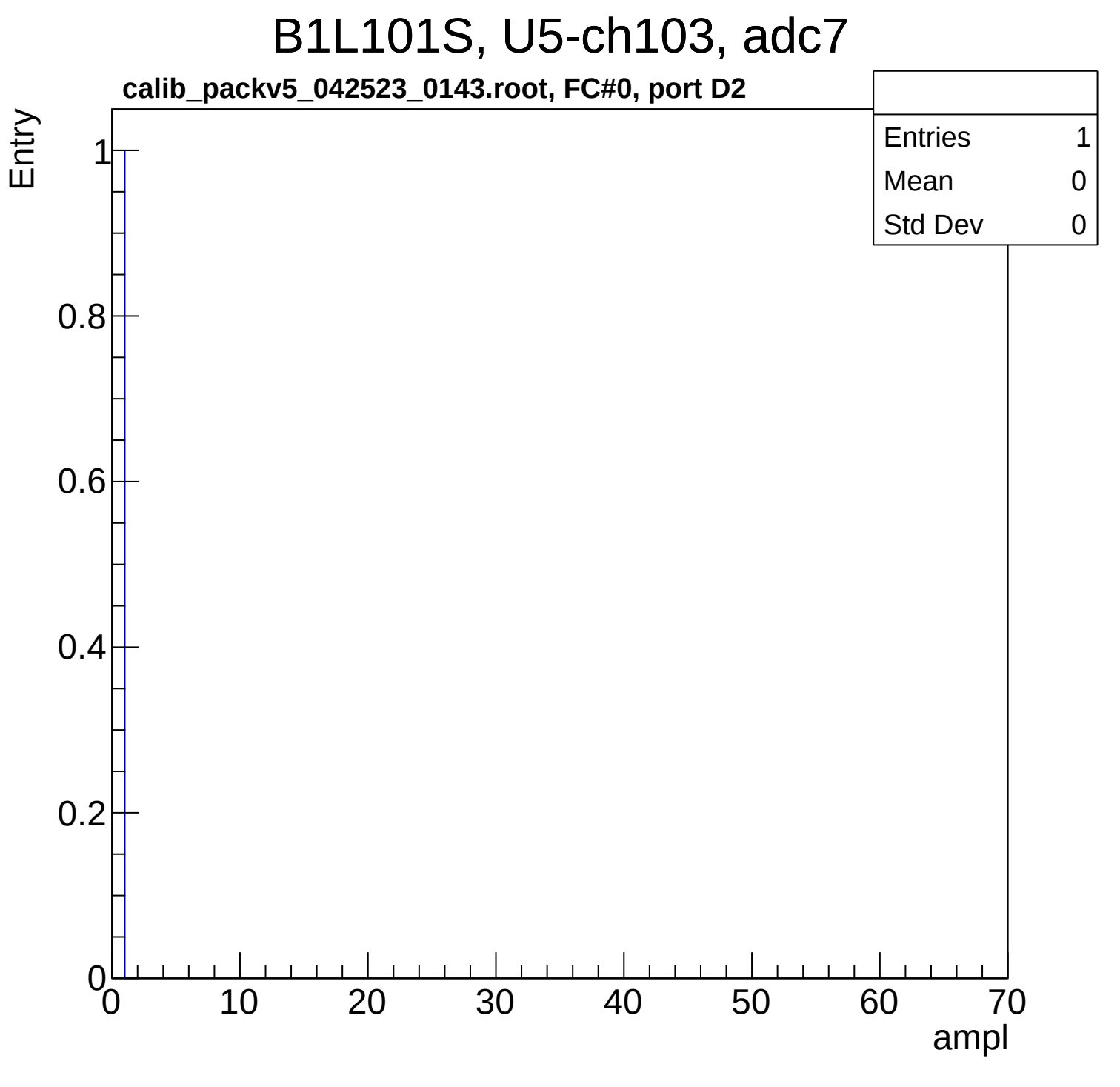
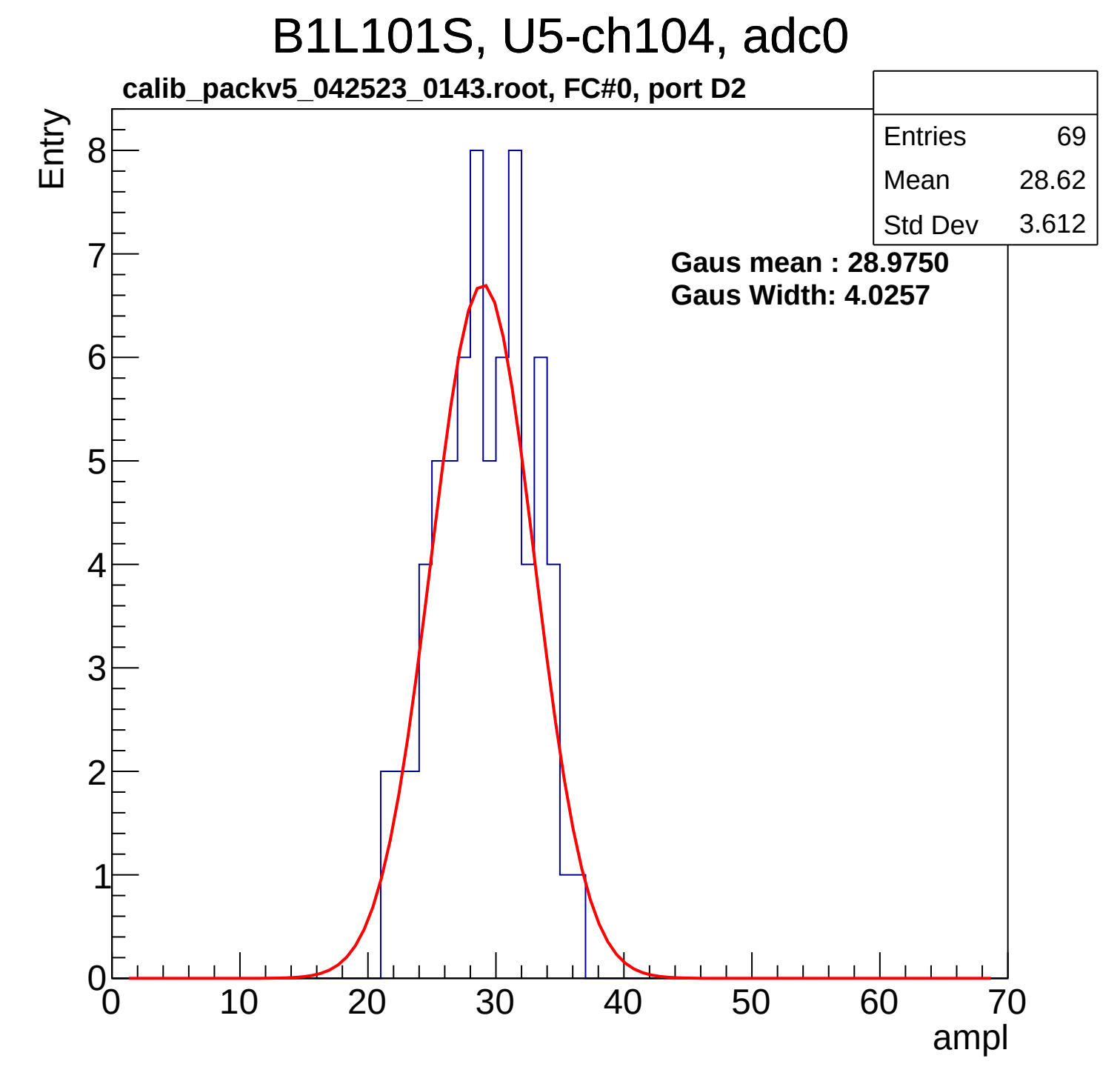
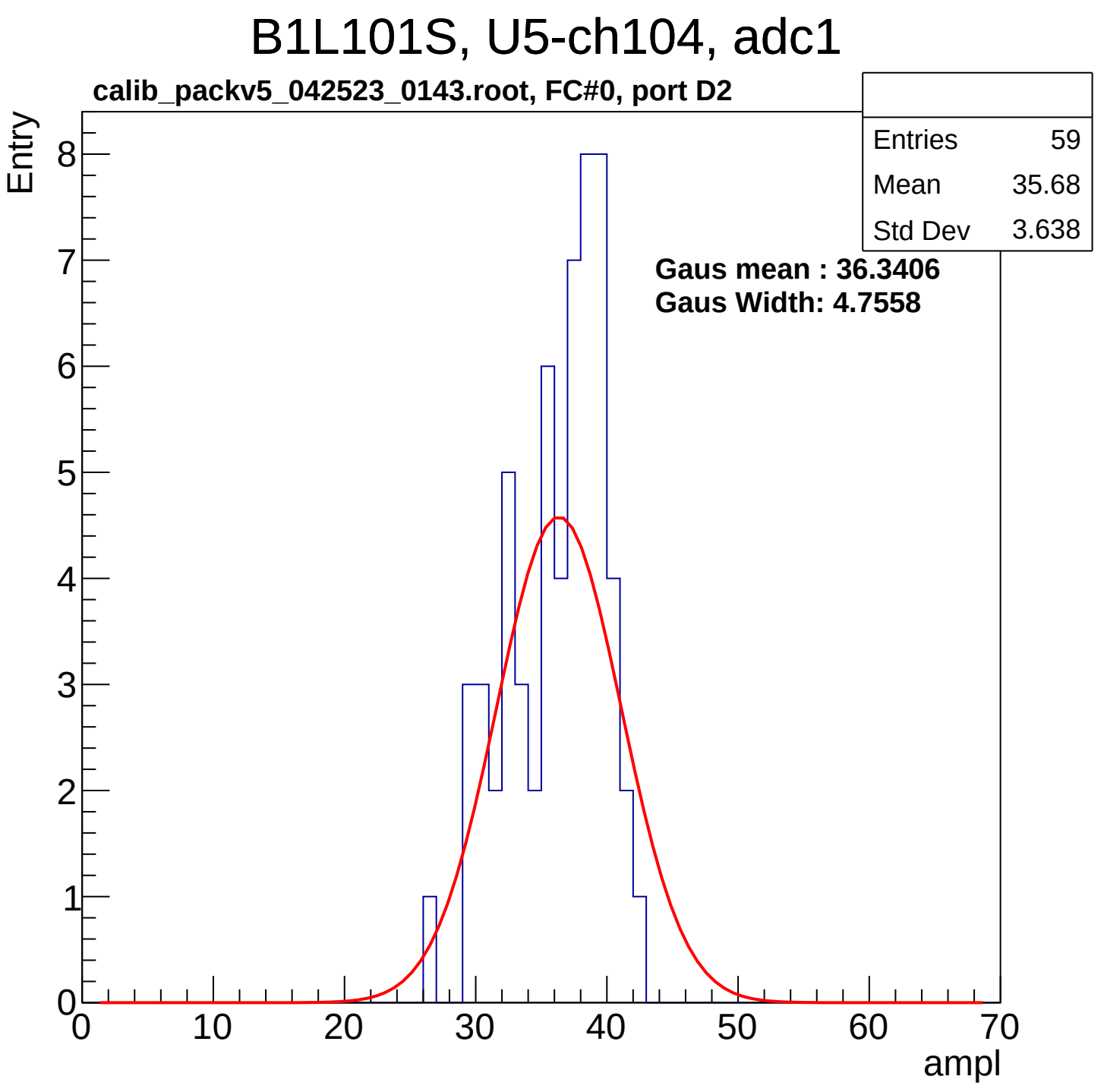
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U5-ch103, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch104, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 28.62
Std Dev 3.612
Gaus mean : 28.9750
Gaus Width: 4.0257
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch104, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 35.68
Std Dev 3.638
Gaus mean : 36.3406
Gaus Width: 4.7558
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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40
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60
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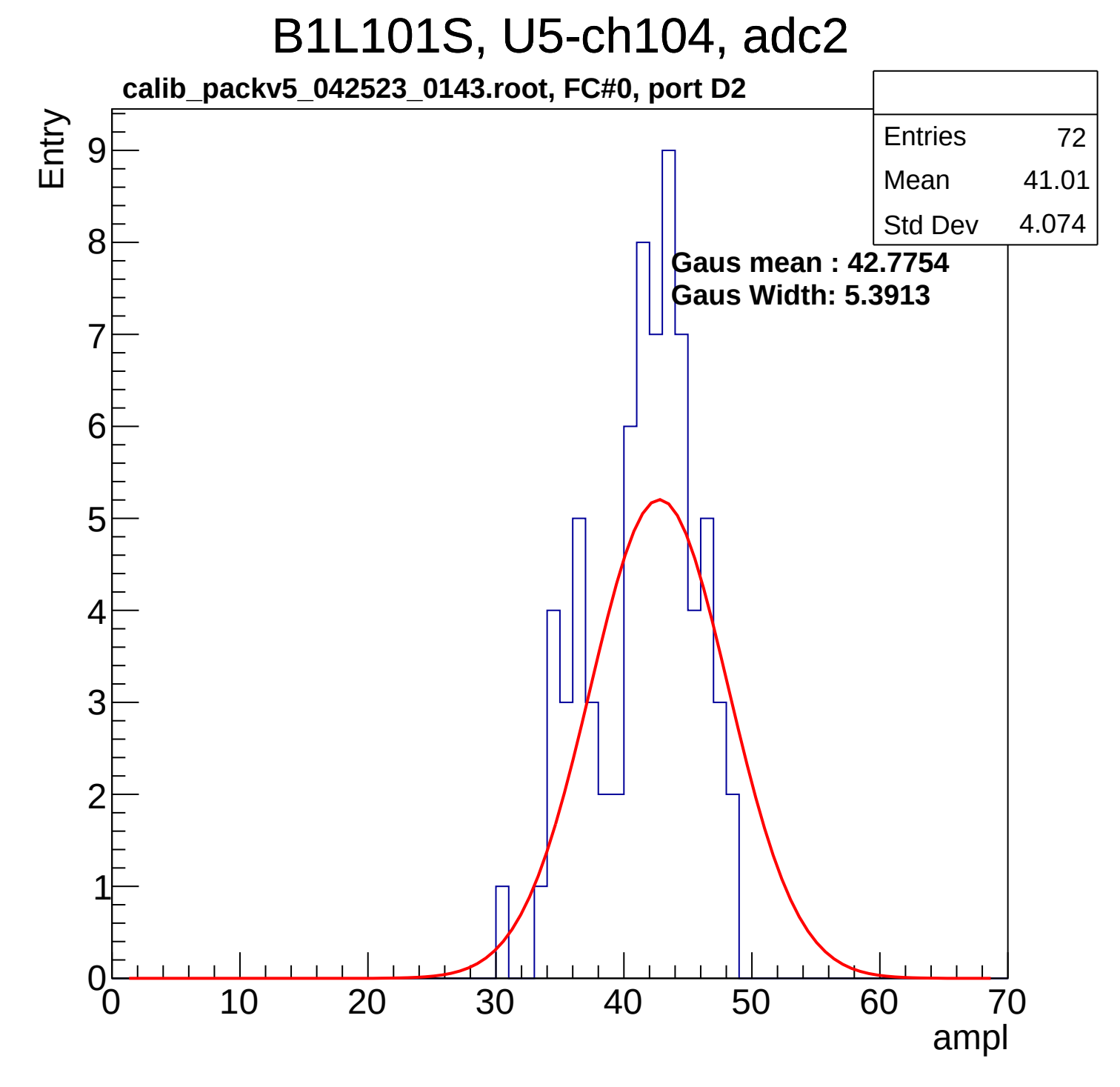
B1L101S, U5-ch104, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 41.01
Std Dev 4.074
Gaus mean : 42.7754
Gaus Width: 5.3913
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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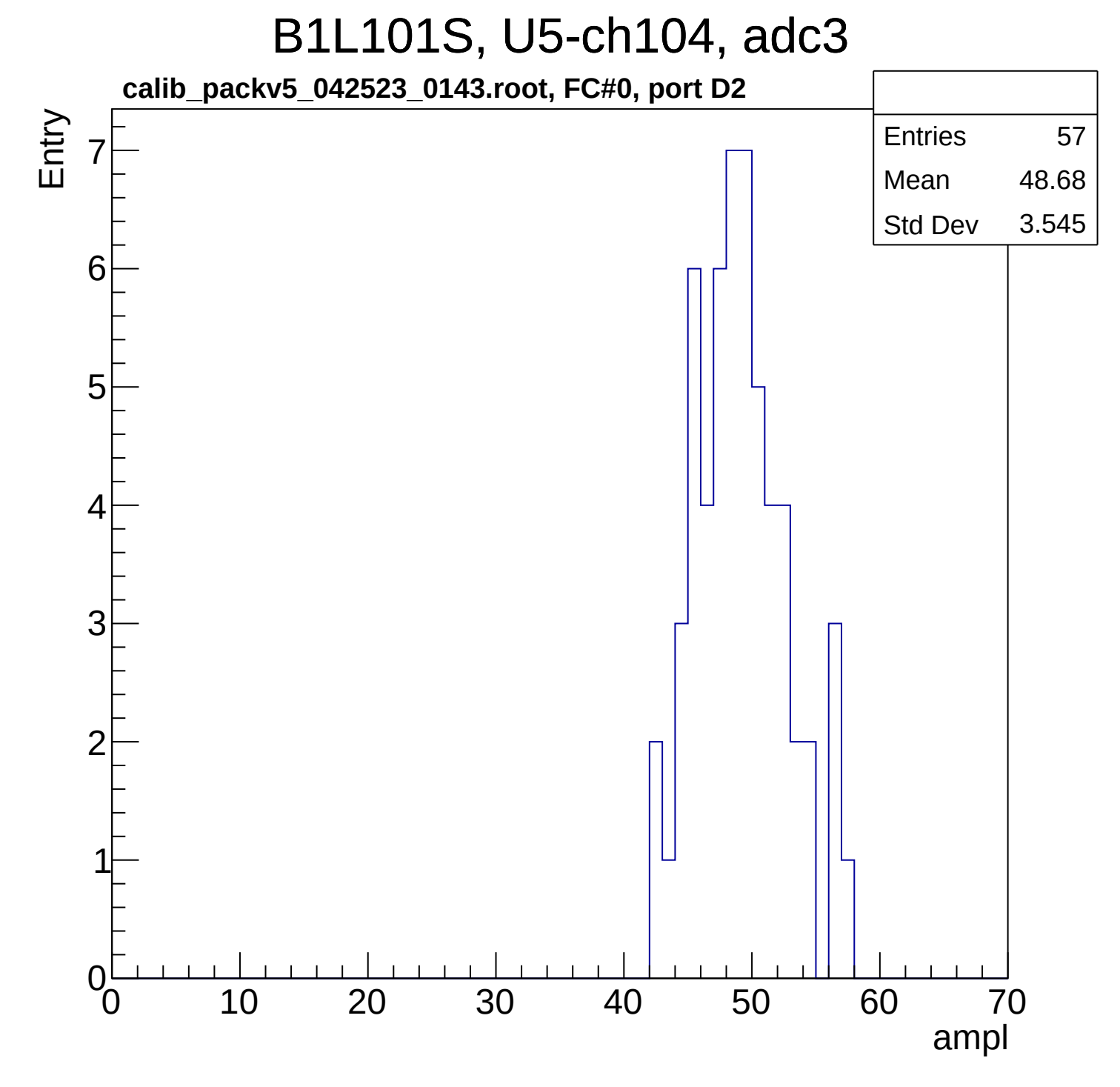
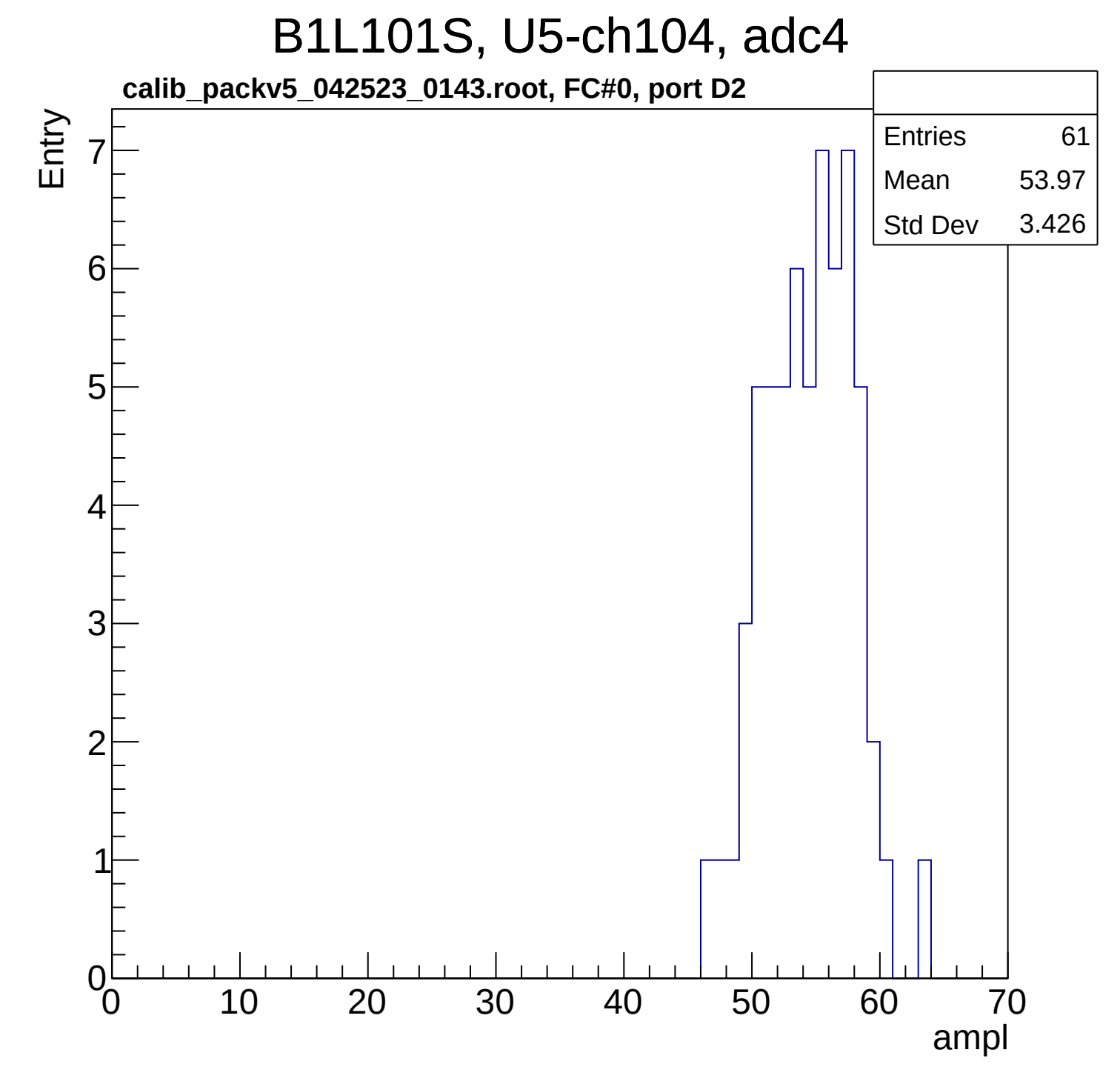
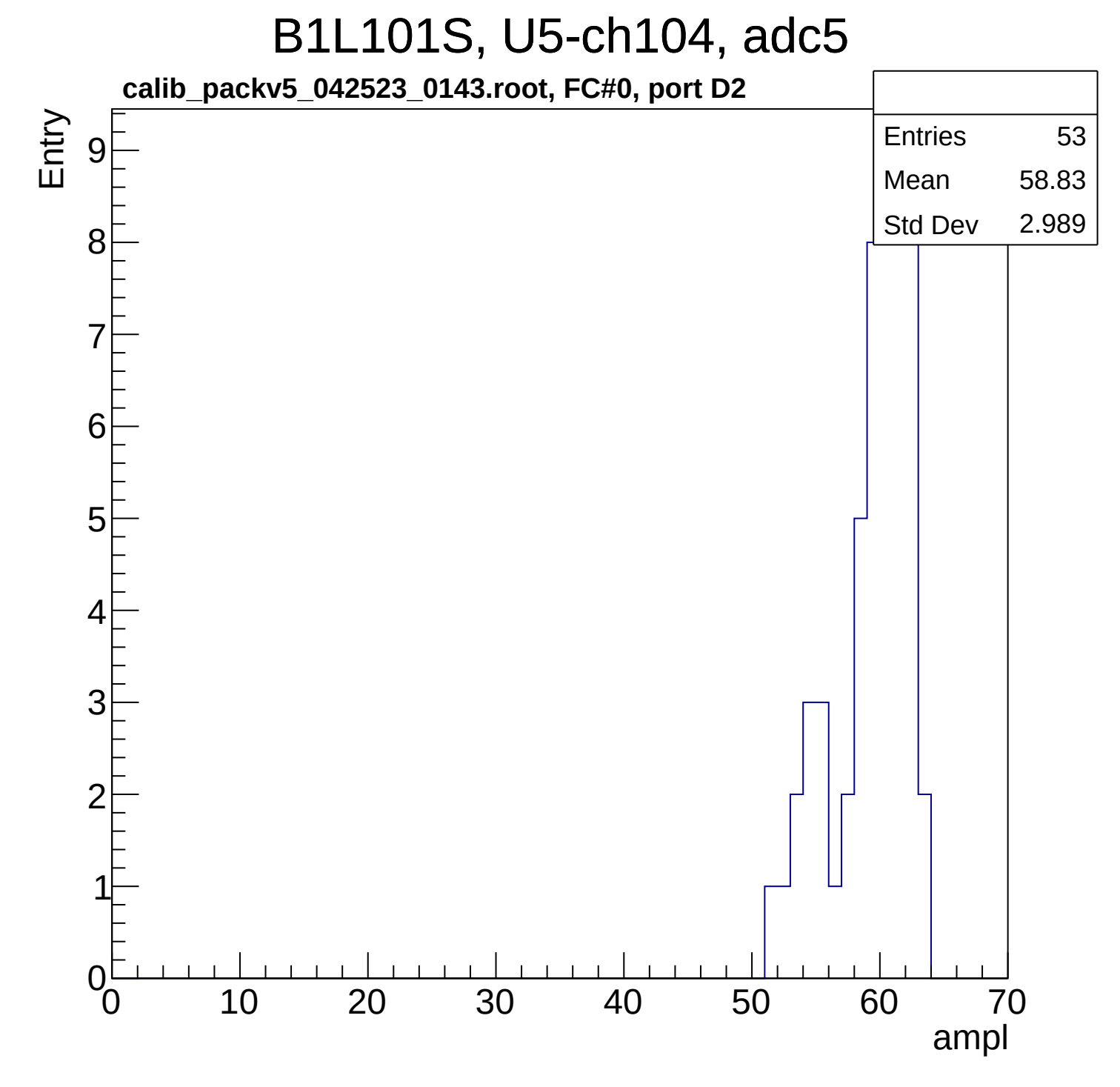

B1L101S, U5-ch104, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 48.68
Std Dev 3.545
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch104, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 53.97
Std Dev 3.426
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch104, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 58.83
Std Dev 2.989
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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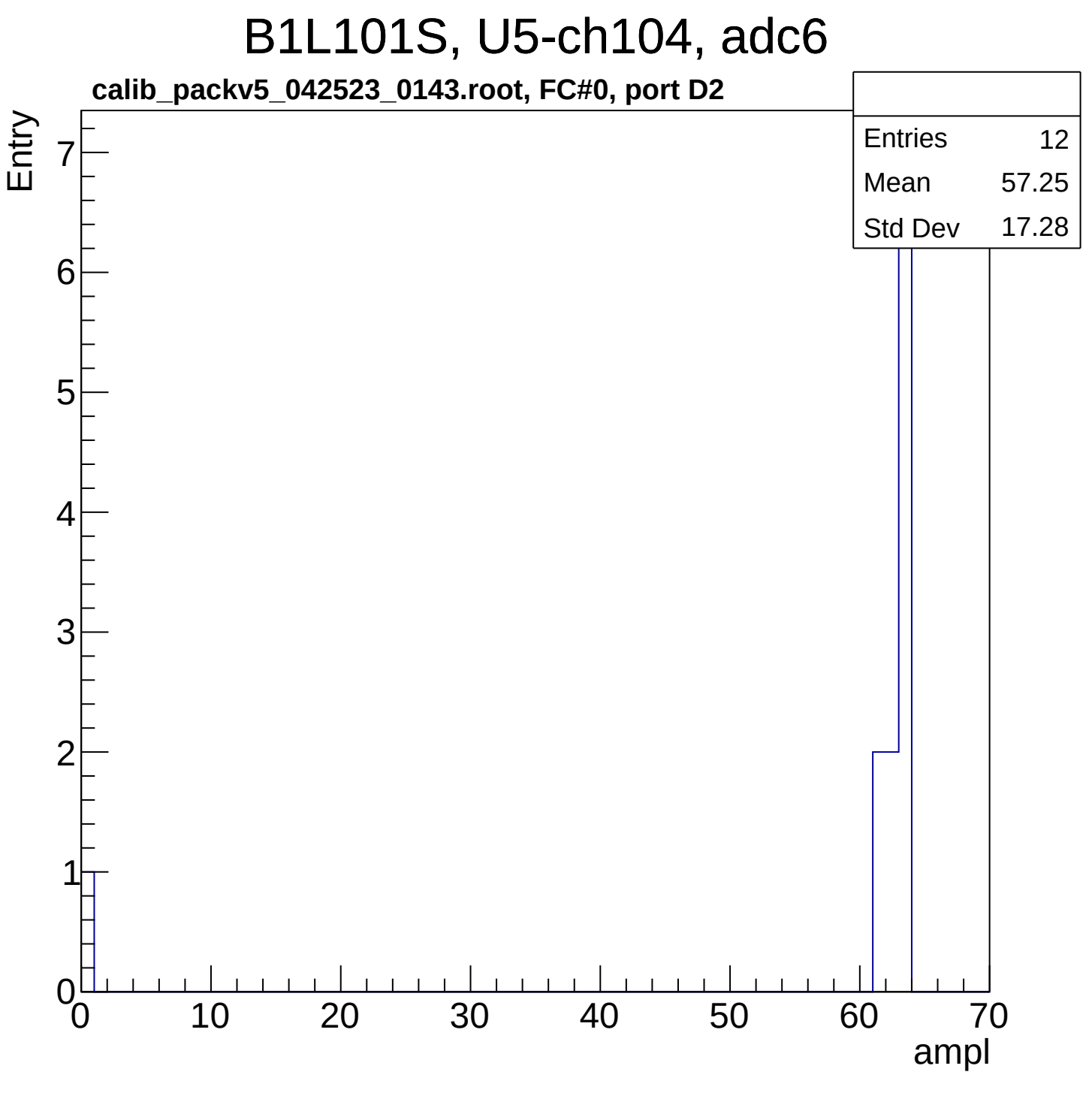
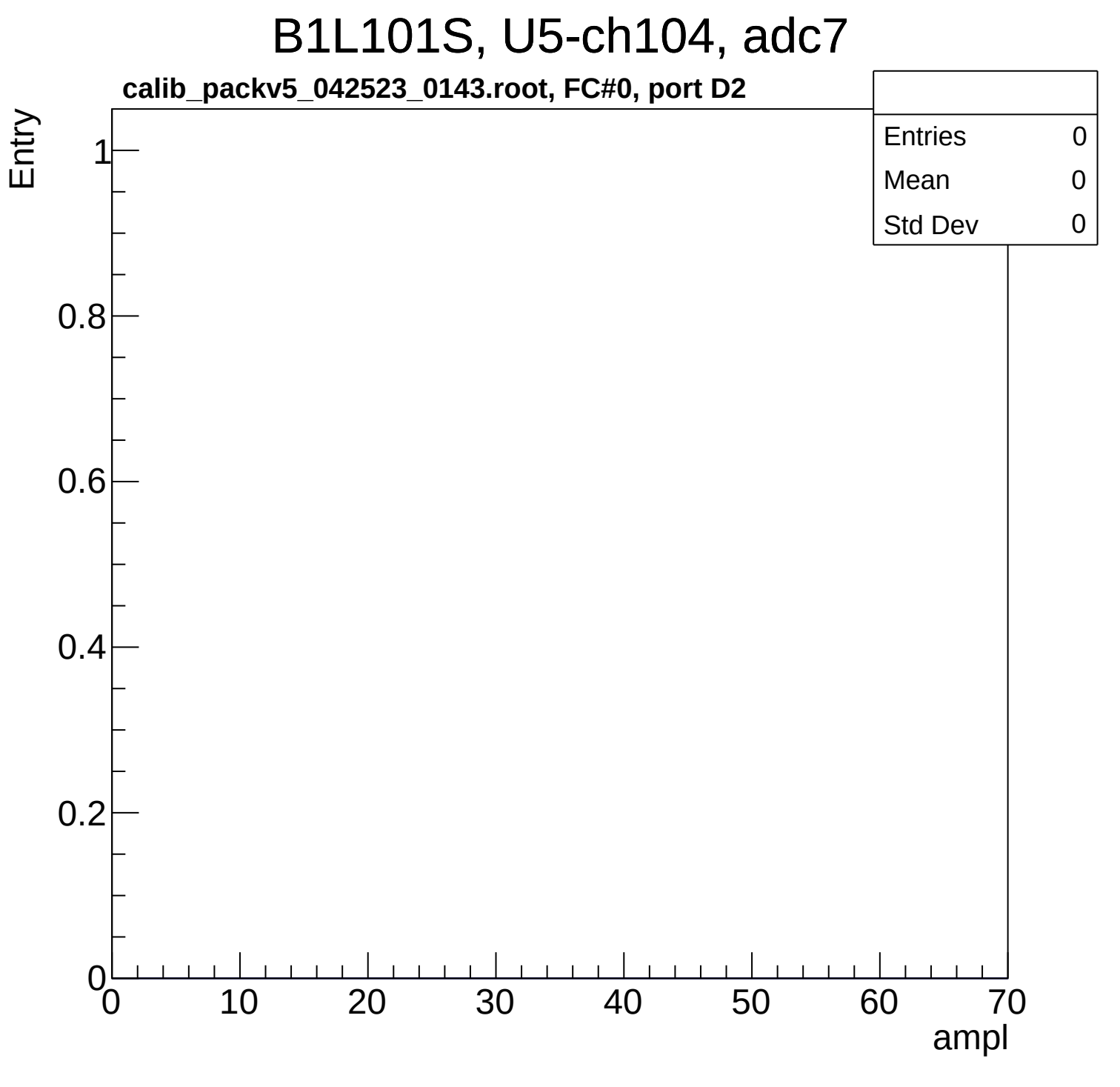
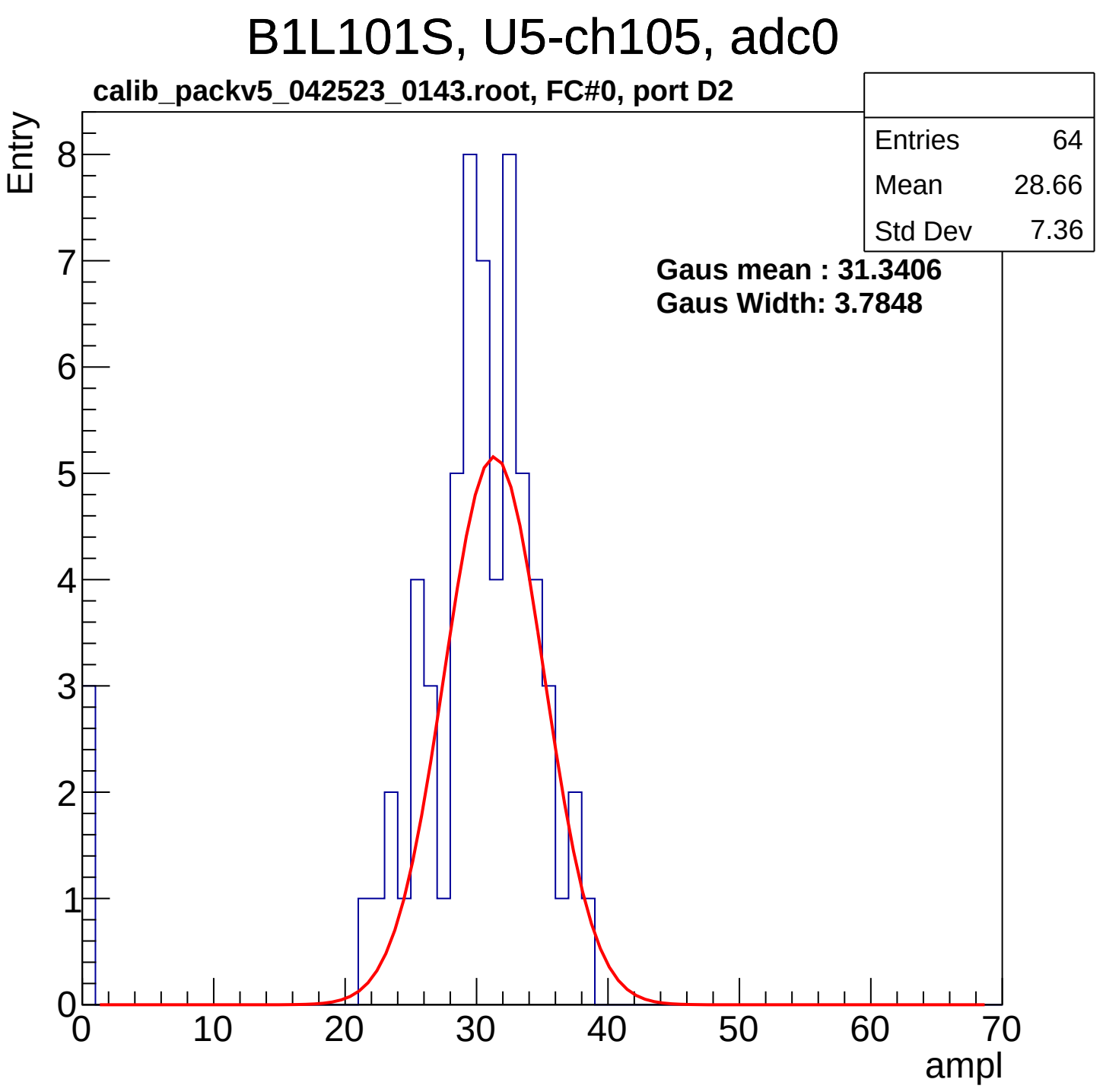
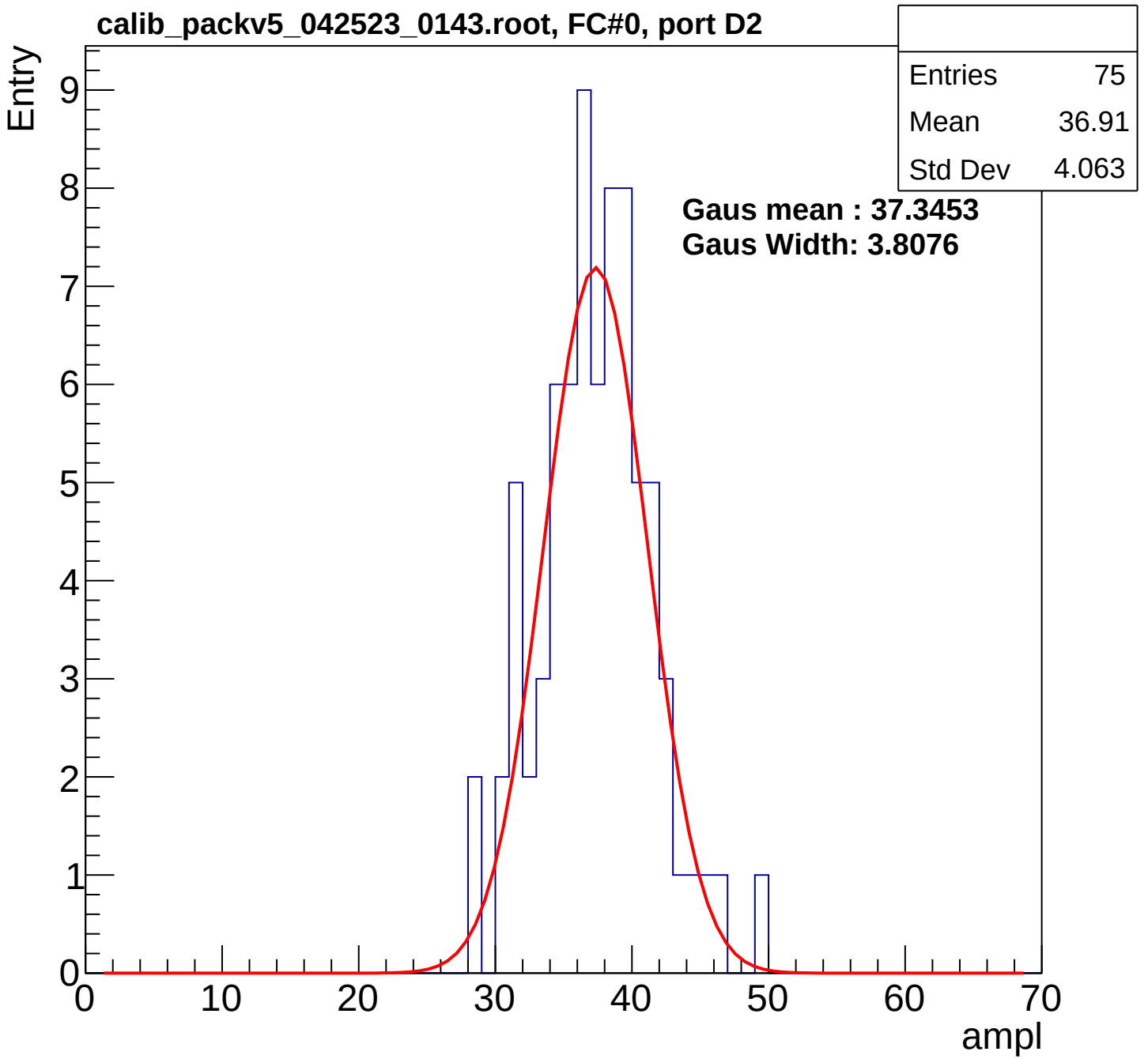

B1L101S, U5-ch104, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 12
Mean 57.25
Std Dev 17.28
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch104, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch105, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 28.66
Std Dev 7.36
Gaus mean : 31.3406
Gaus Width: 3.7848
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch105, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 36.91
Std Dev 4.063
Gaus mean : 37.3453
Gaus Width: 3.8076
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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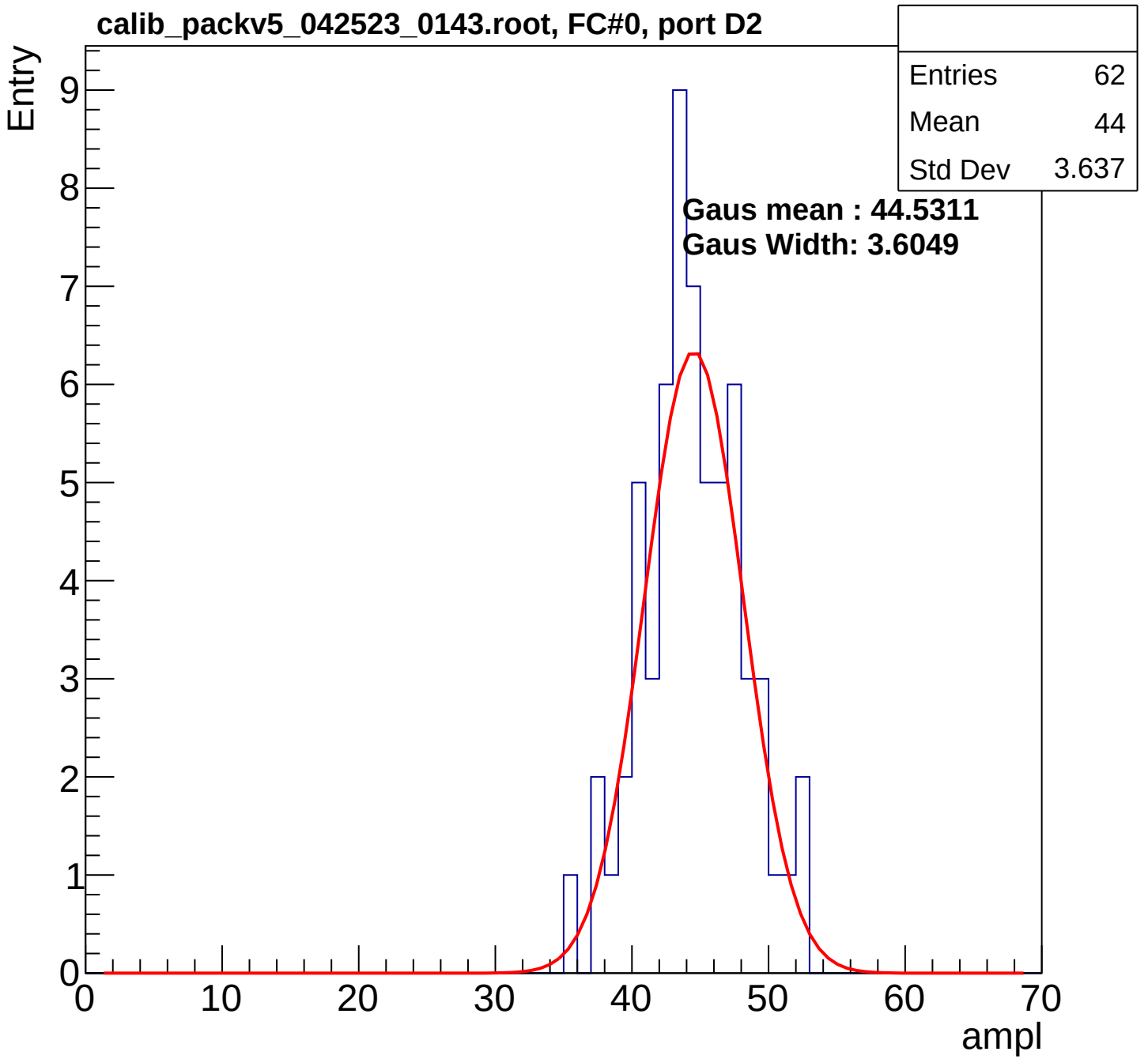
B1L101S, U5-ch105, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 44
Std Dev 3.637
Gaus mean : 44.5311
Gaus Width: 3.6049
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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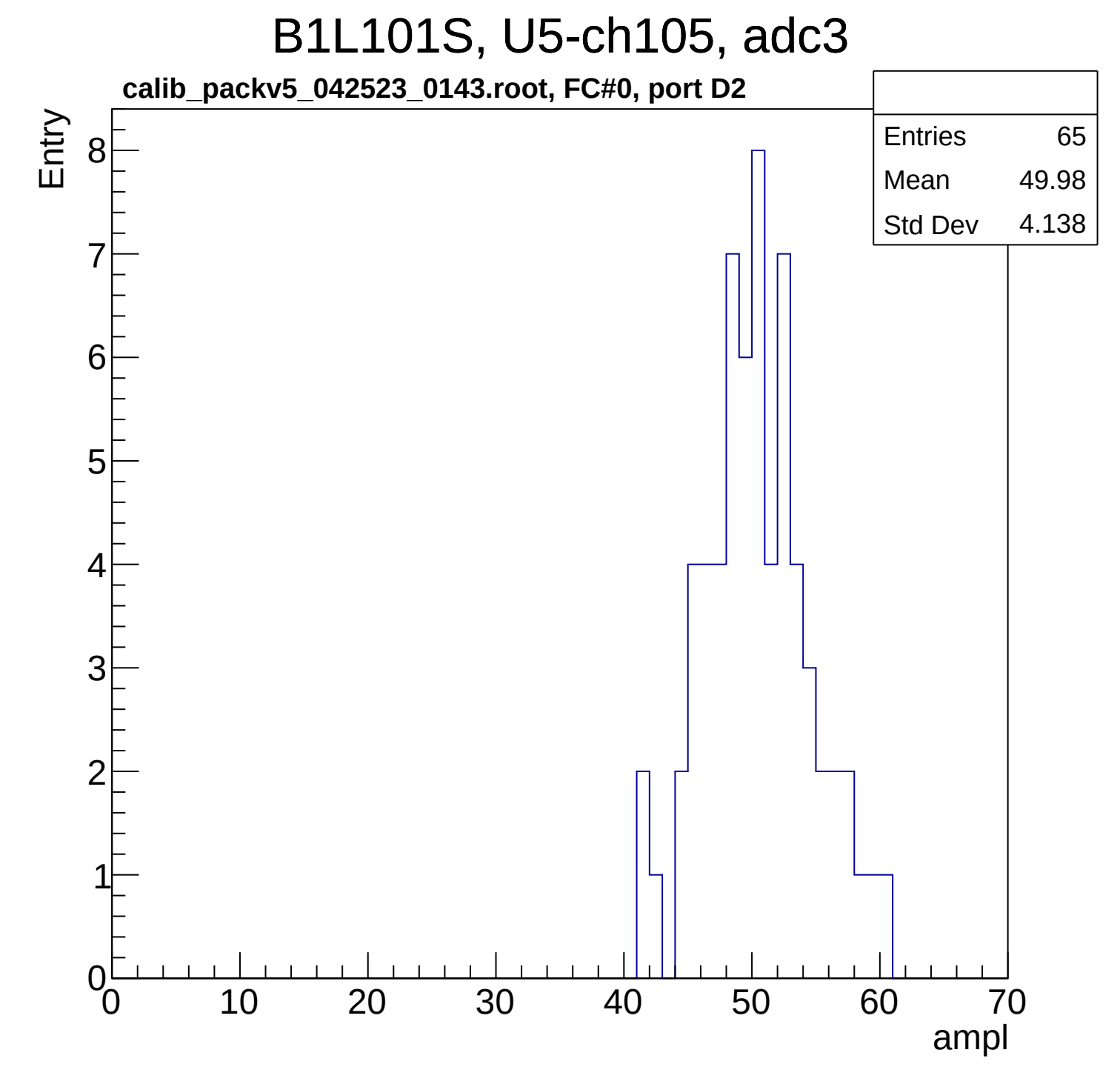
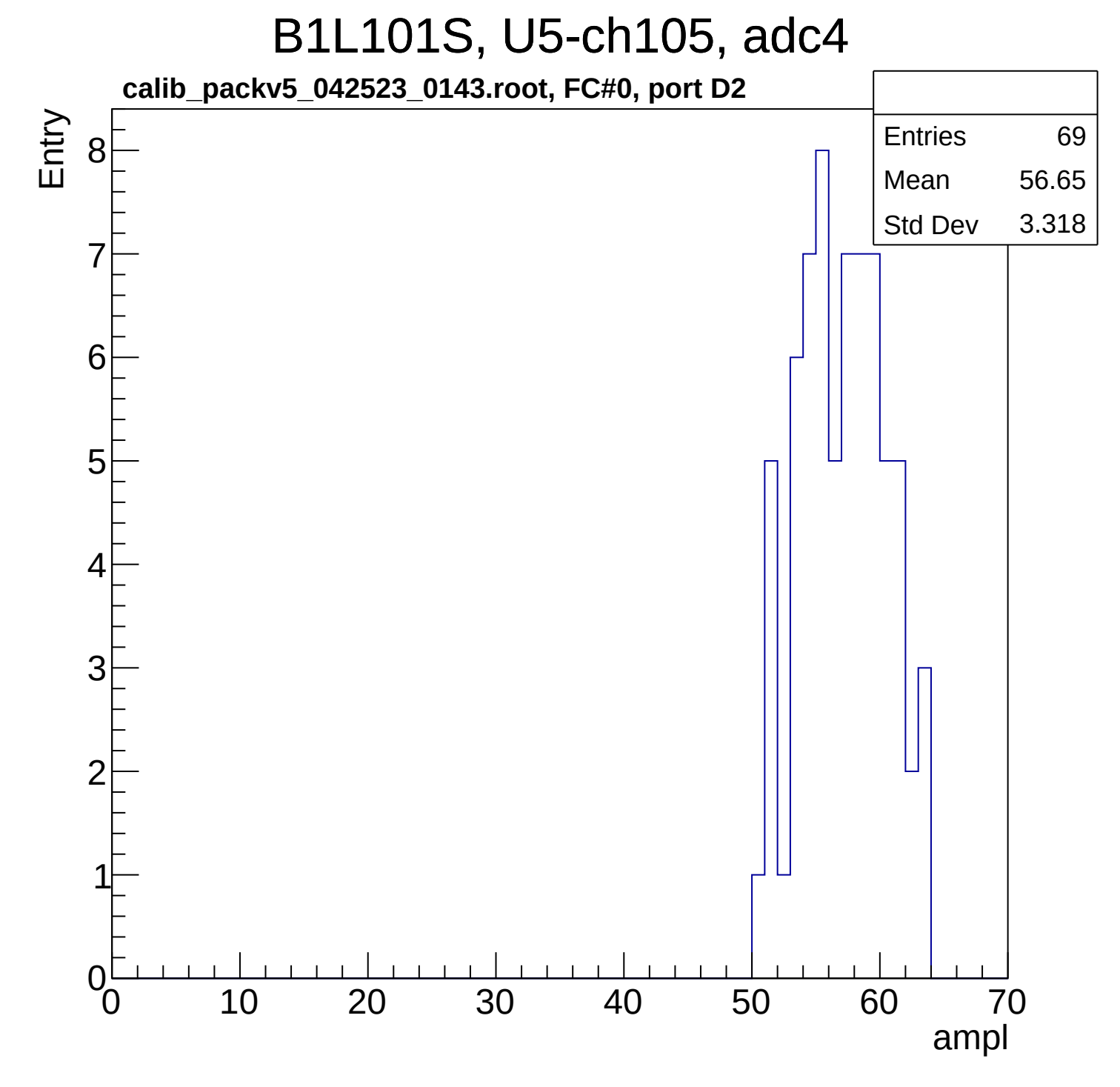

B1L101S, U5-ch105, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 49.98
Std Dev 4.138
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch105, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 56.65
Std Dev 3.318
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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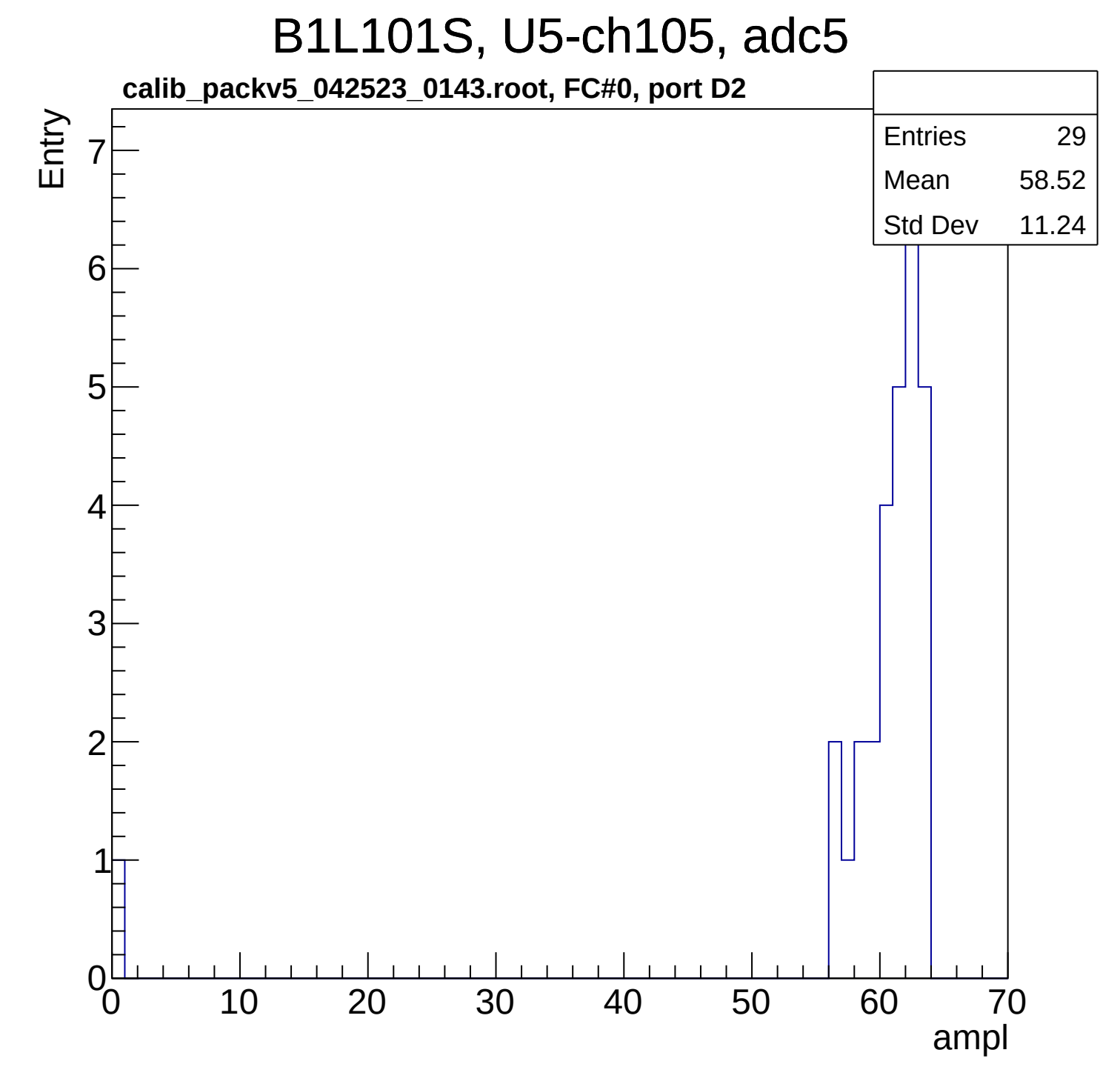
B1L101S, U5-ch105, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 29
Mean 58.52
Std Dev 11.24
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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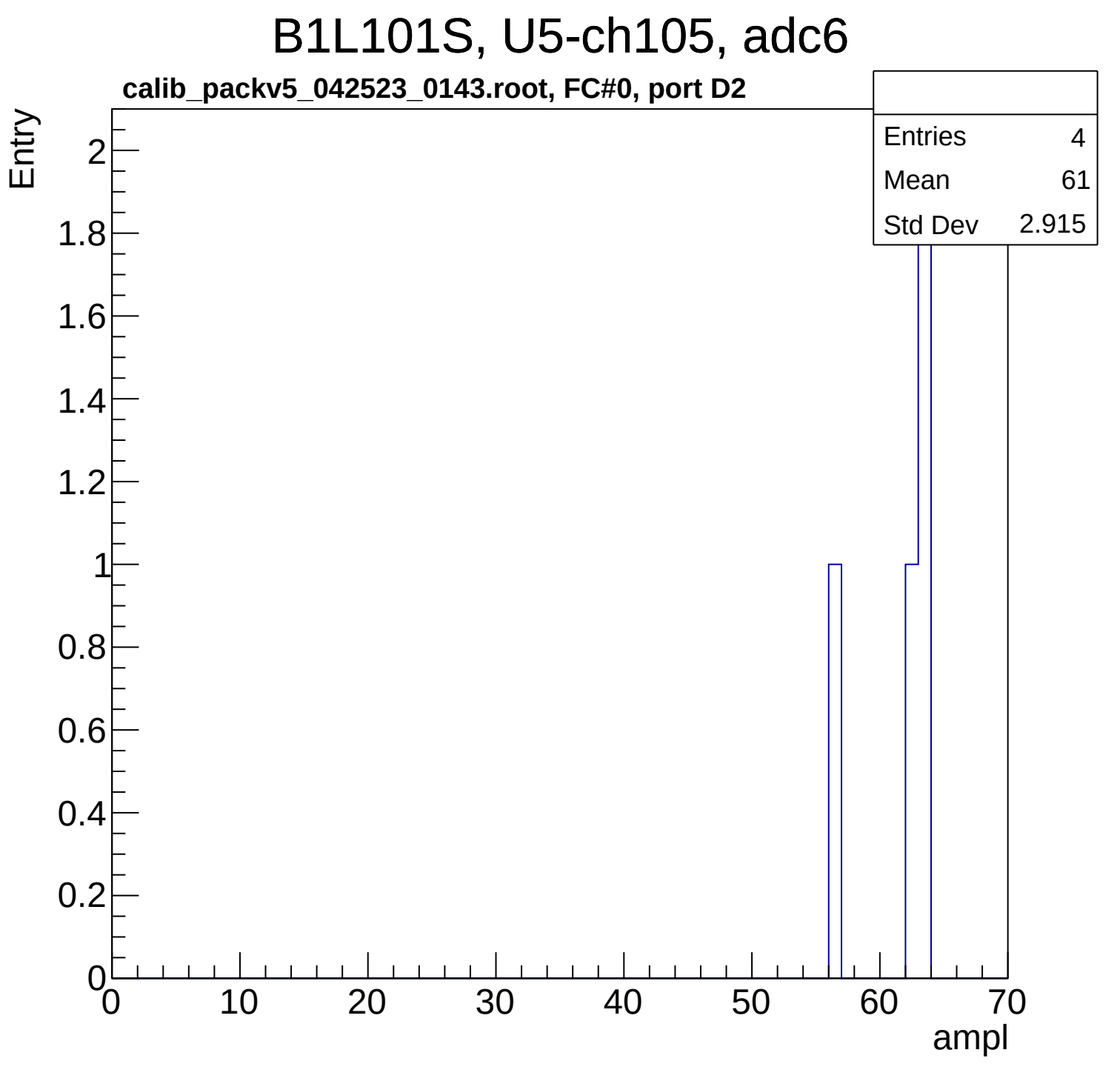
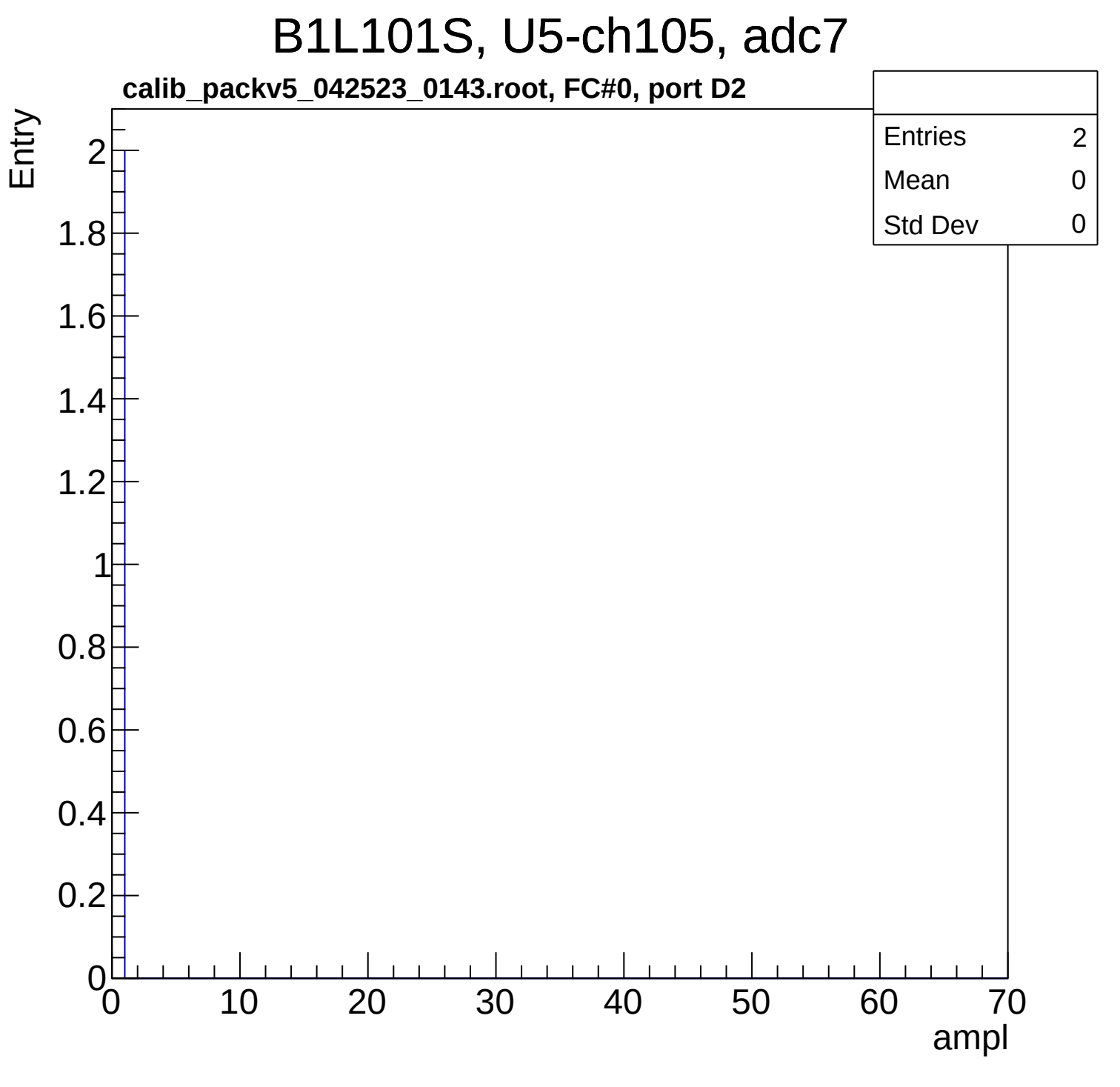

B1L101S, U5-ch105, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 61
Std Dev 2.915
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U5-ch105, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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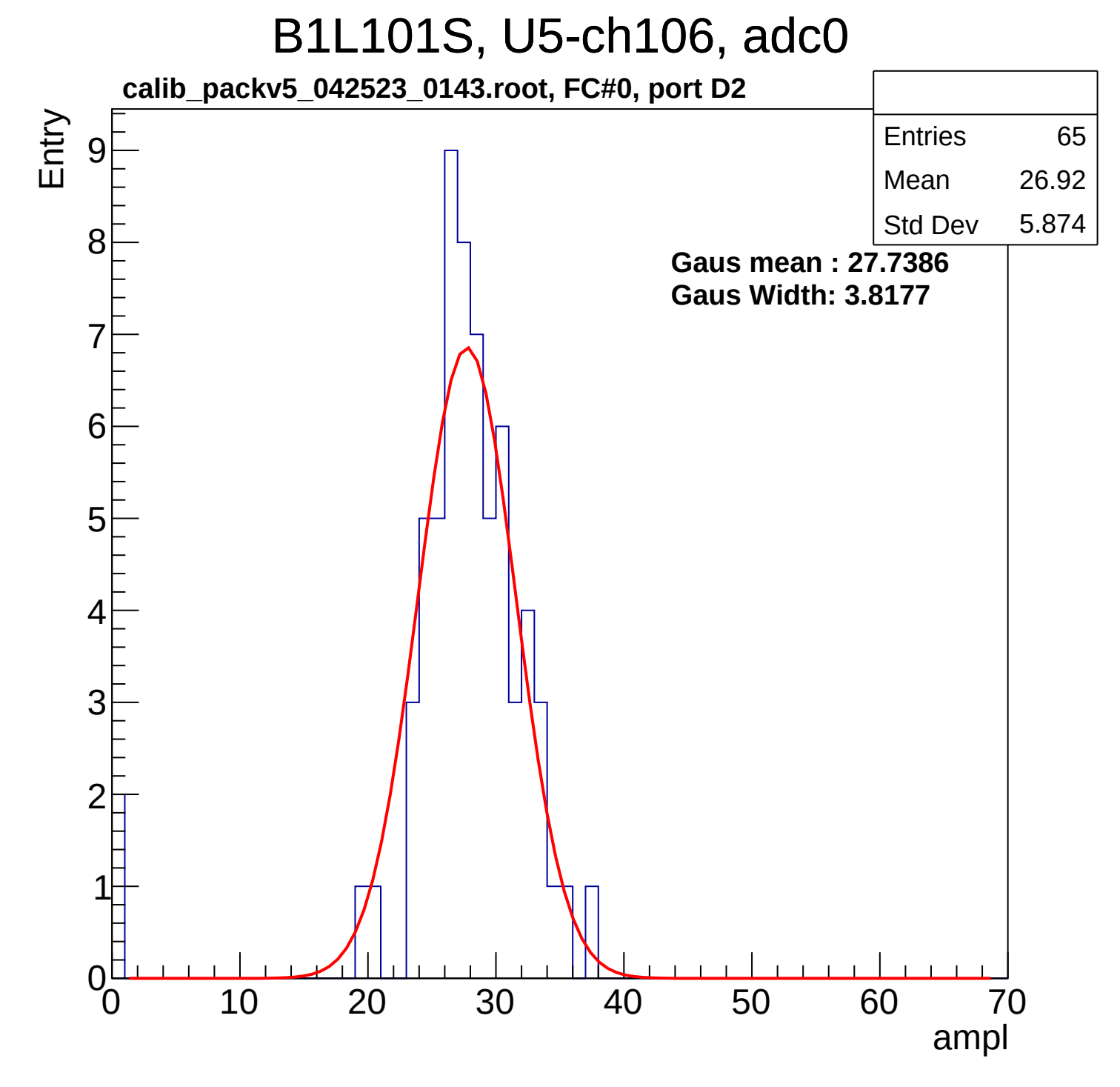
B1L101S, U5-ch106, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 26.92
Std Dev 5.874
Gaus mean : 27.7386
Gaus Width: 3.8177
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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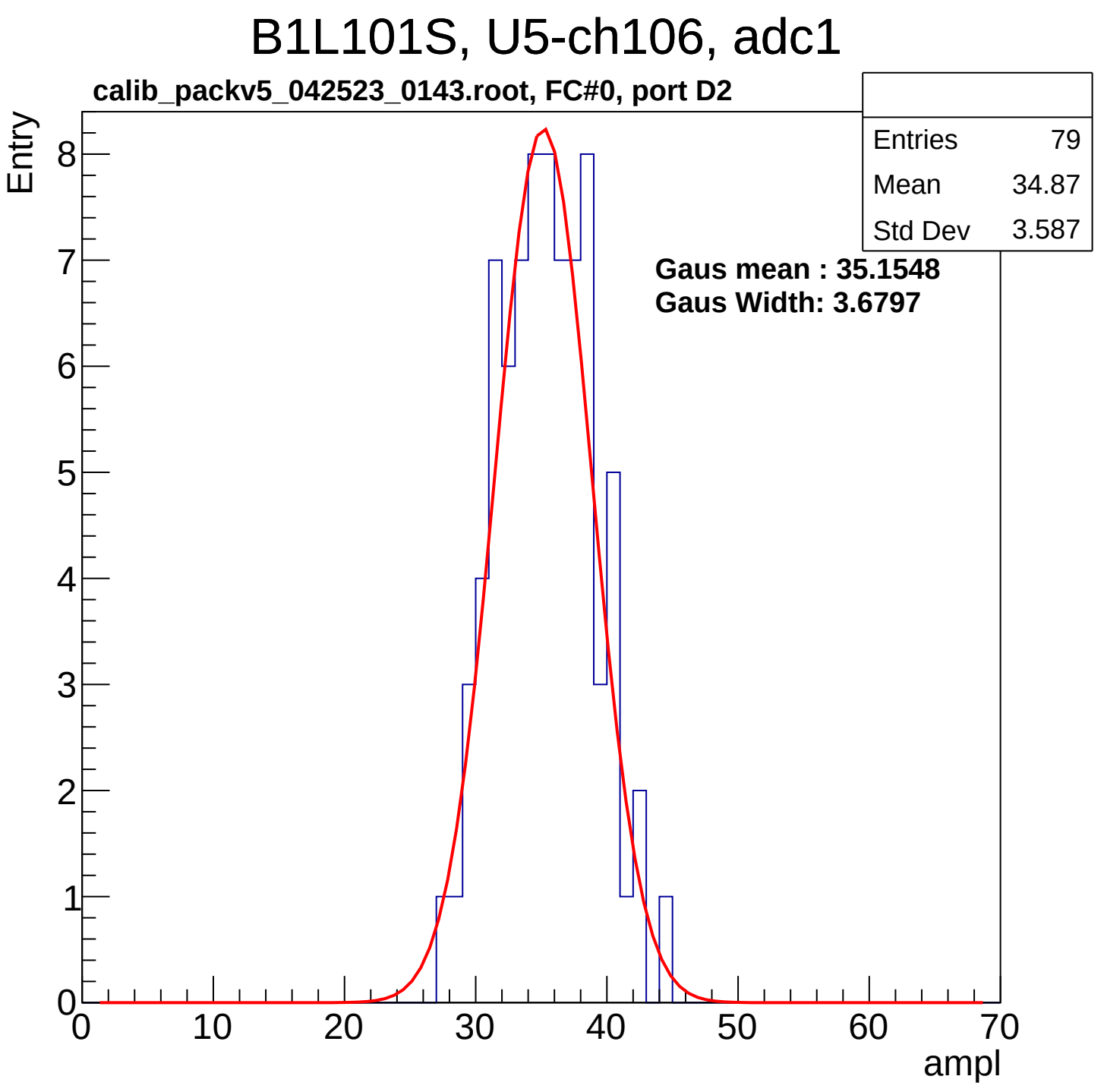
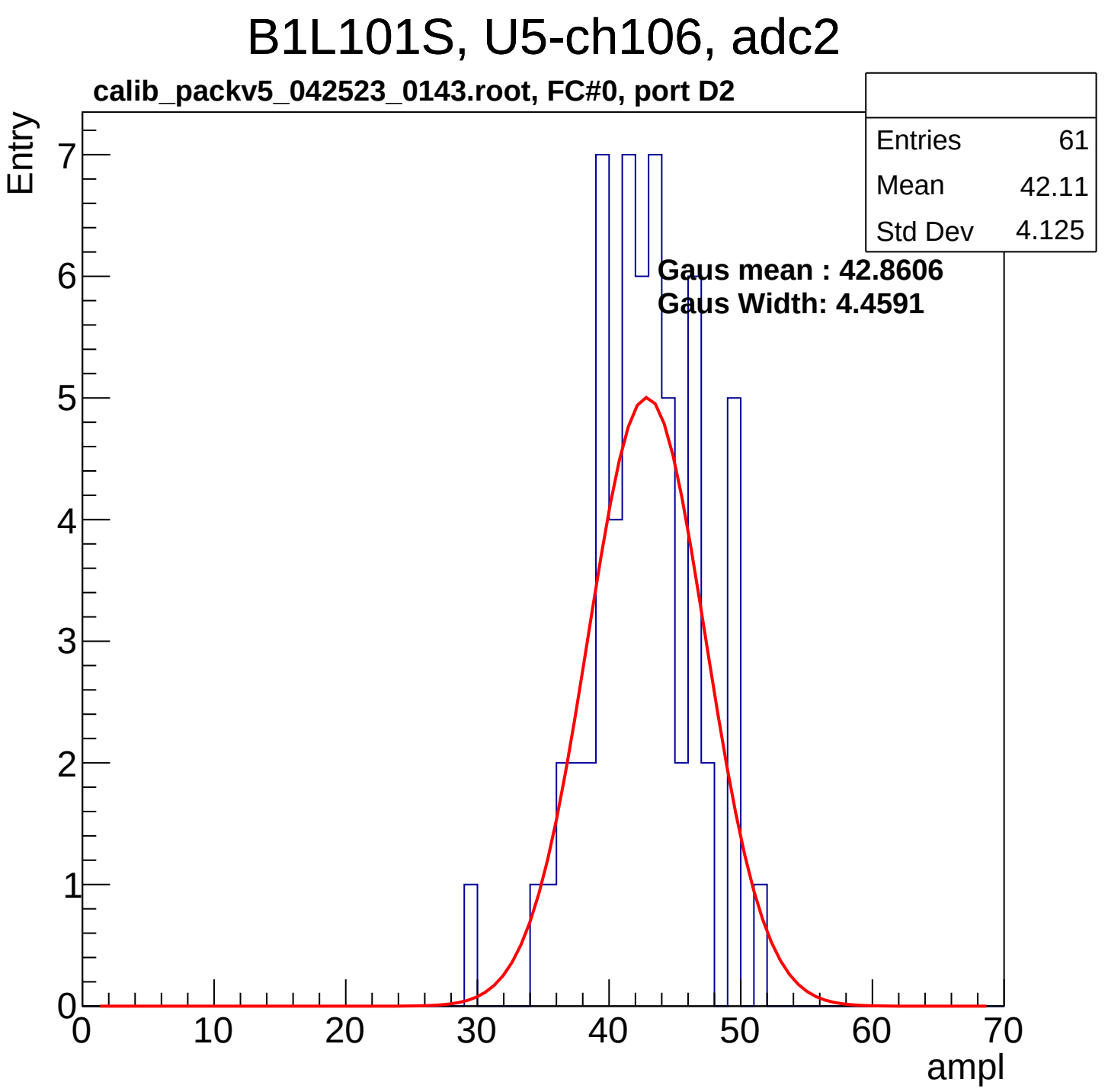

B1L101S, U5-ch106, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 34.87
Std Dev 3.587
Gaus mean : 35.1548
Gaus Width: 3.6797
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch106, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 42.11
Std Dev 4.125
Gaus mean : 42.8606
Gaus Width: 4.4591
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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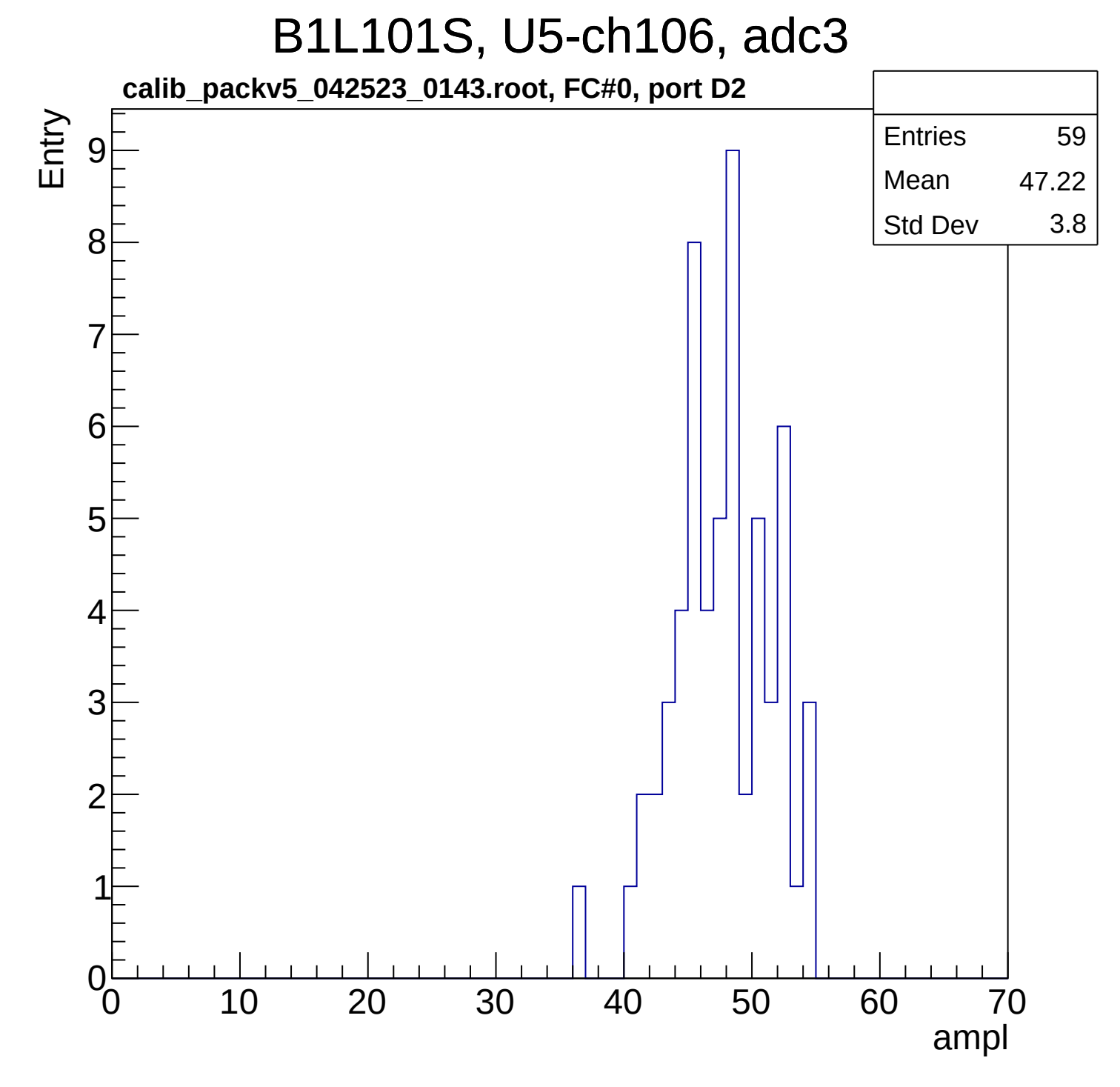
B1L101S, U5-ch106, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 47.22
Std Dev 3.8
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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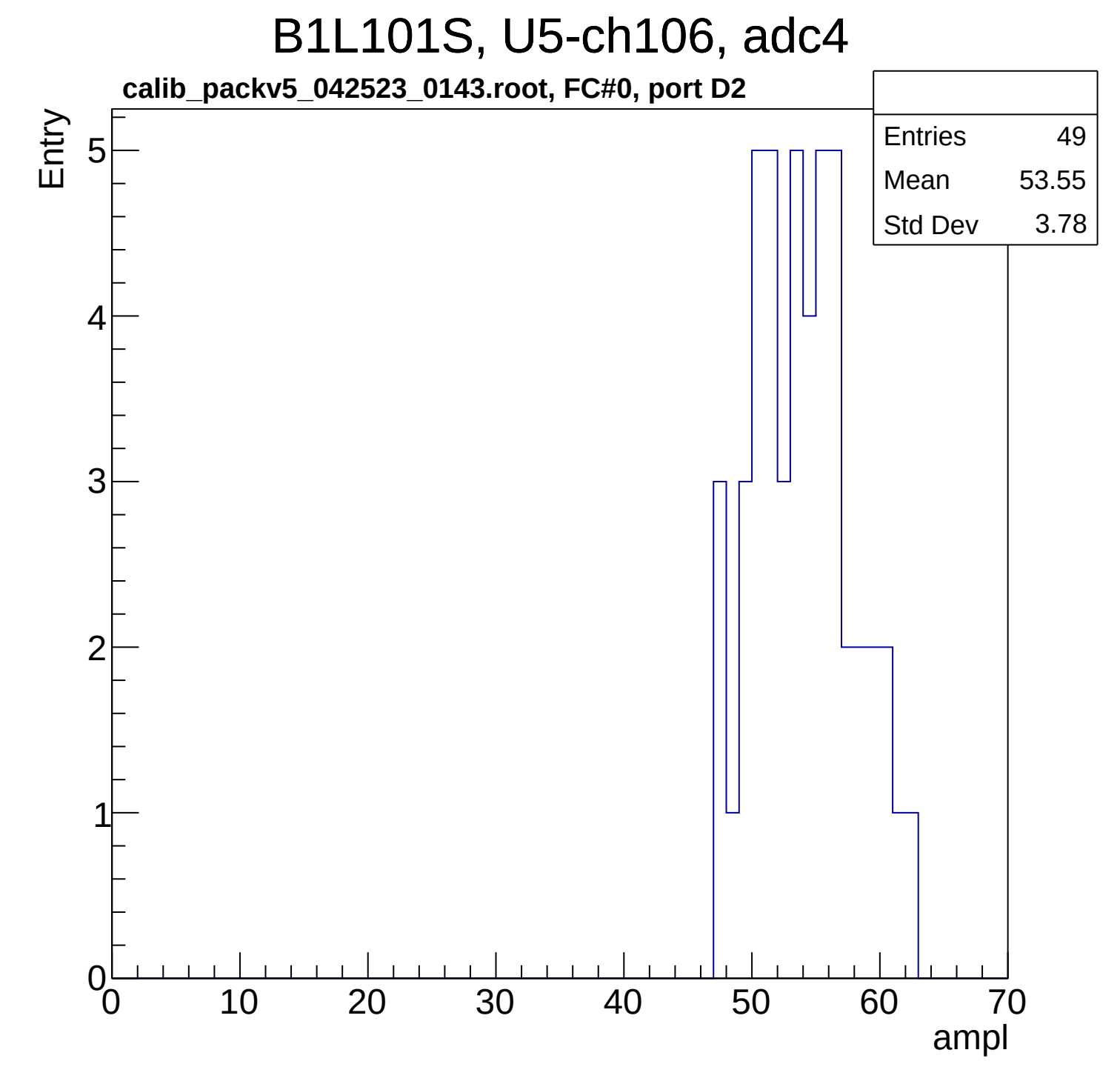
B1L101S, U5-ch106, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 53.55
Std Dev 3.78
Entry
ampl
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1
2
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4
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0
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20
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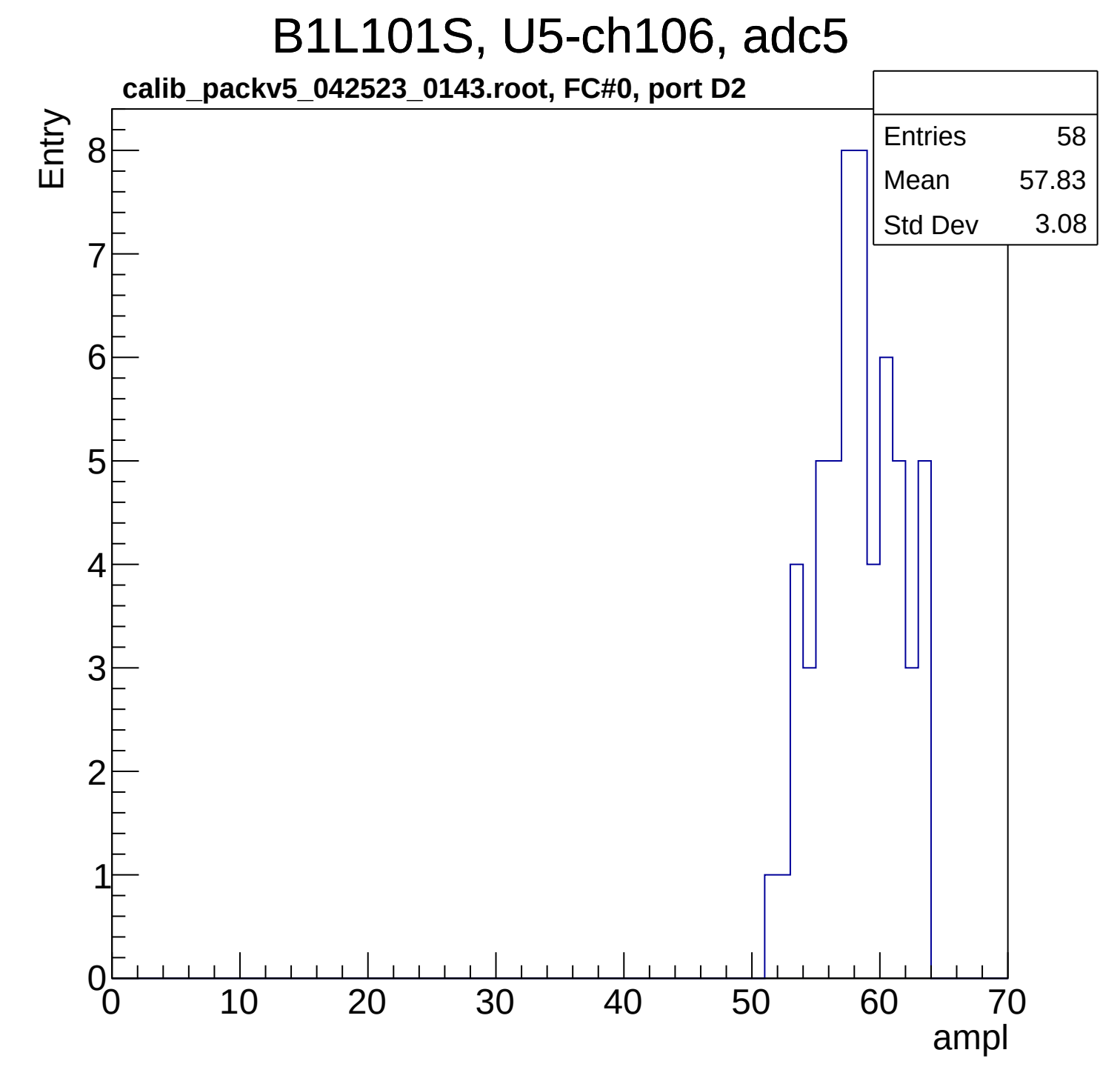
40
50
60
70


B1L101S, U5-ch106, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 57.83
Std Dev 3.08
Entry
ampl
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1
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5
6
7
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0
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40
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60
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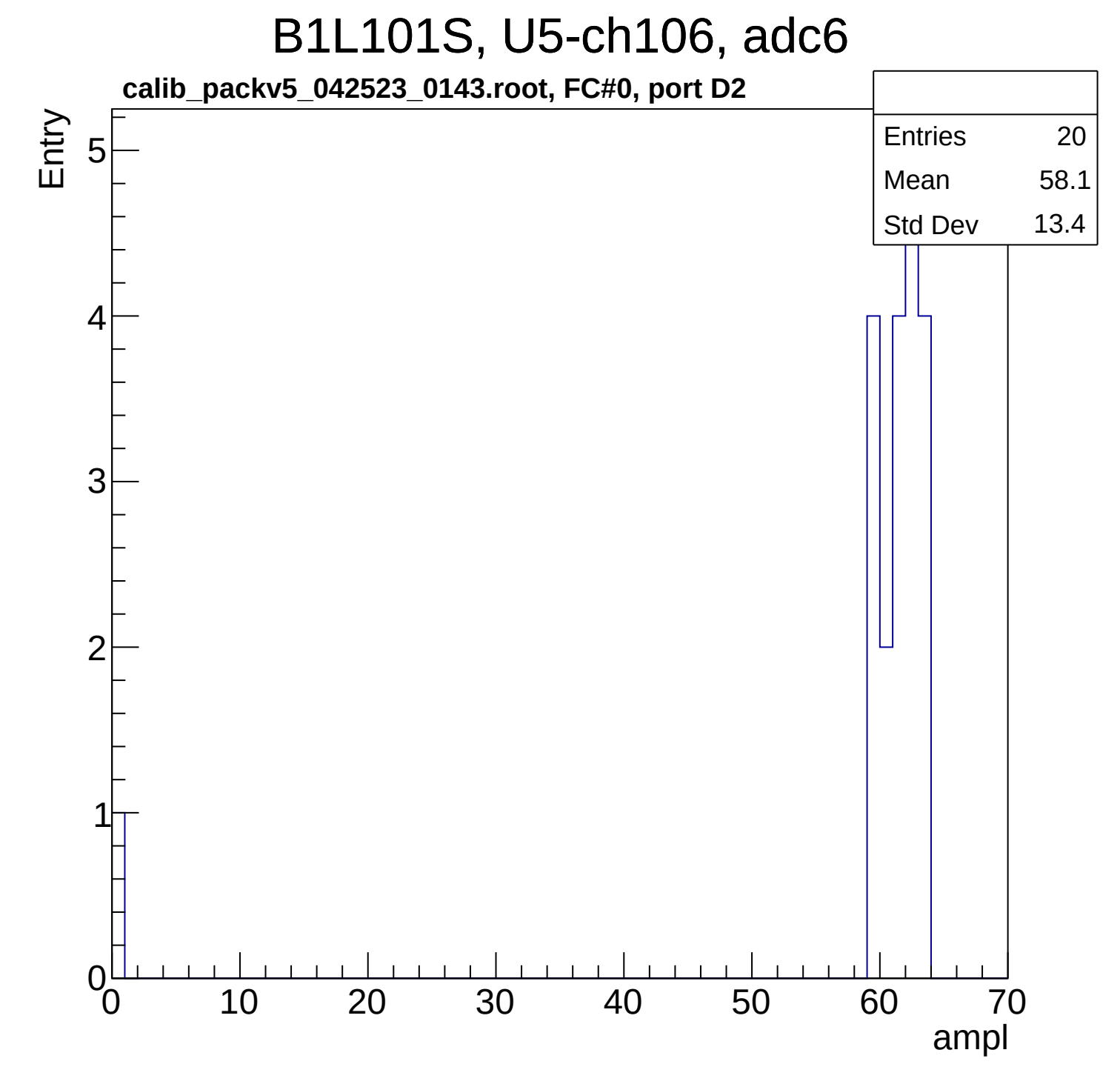
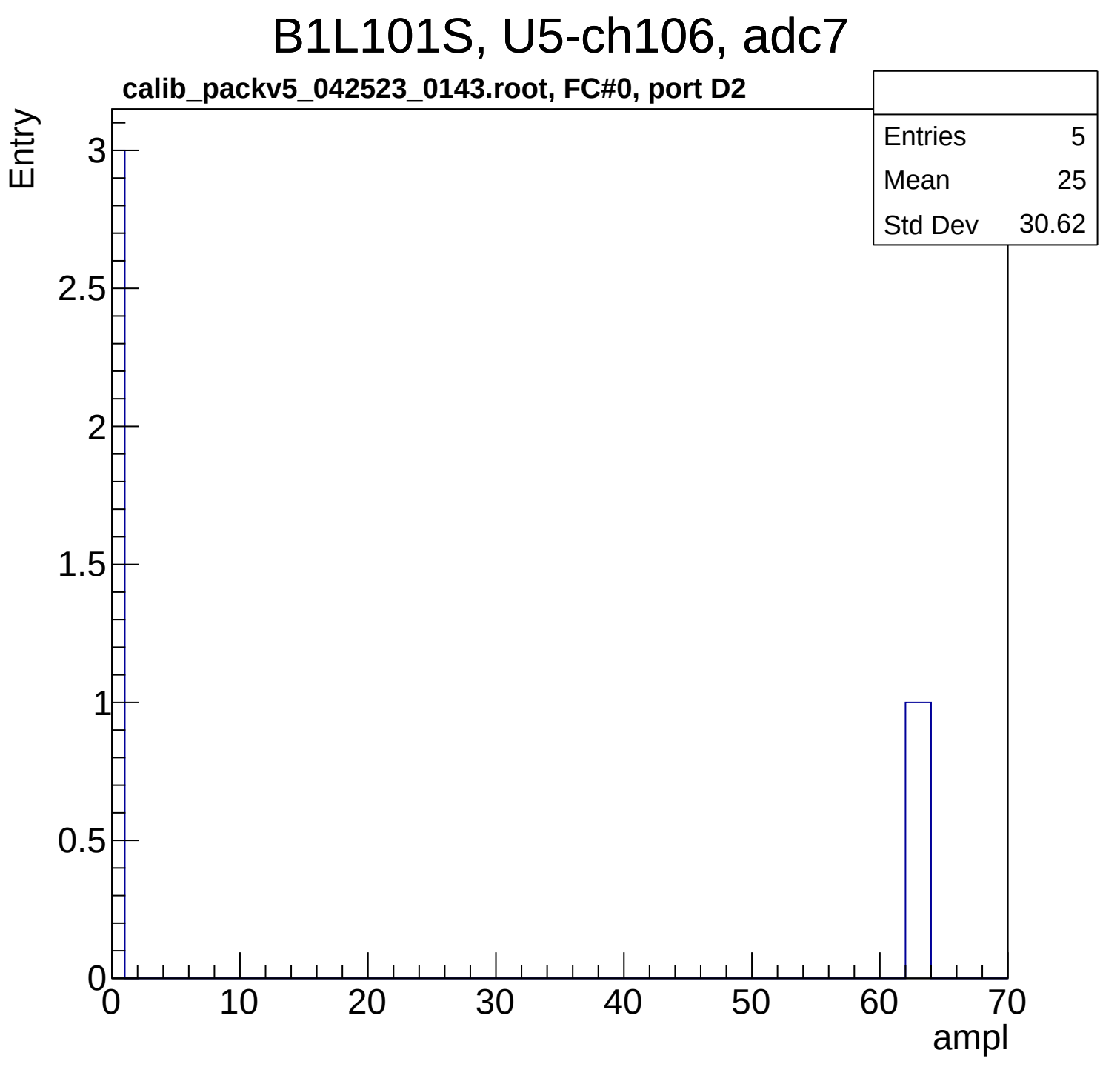

B1L101S, U5-ch106, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 20
Mean 58.1
Std Dev 13.4
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch106, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 25
Std Dev 30.62
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
50
60
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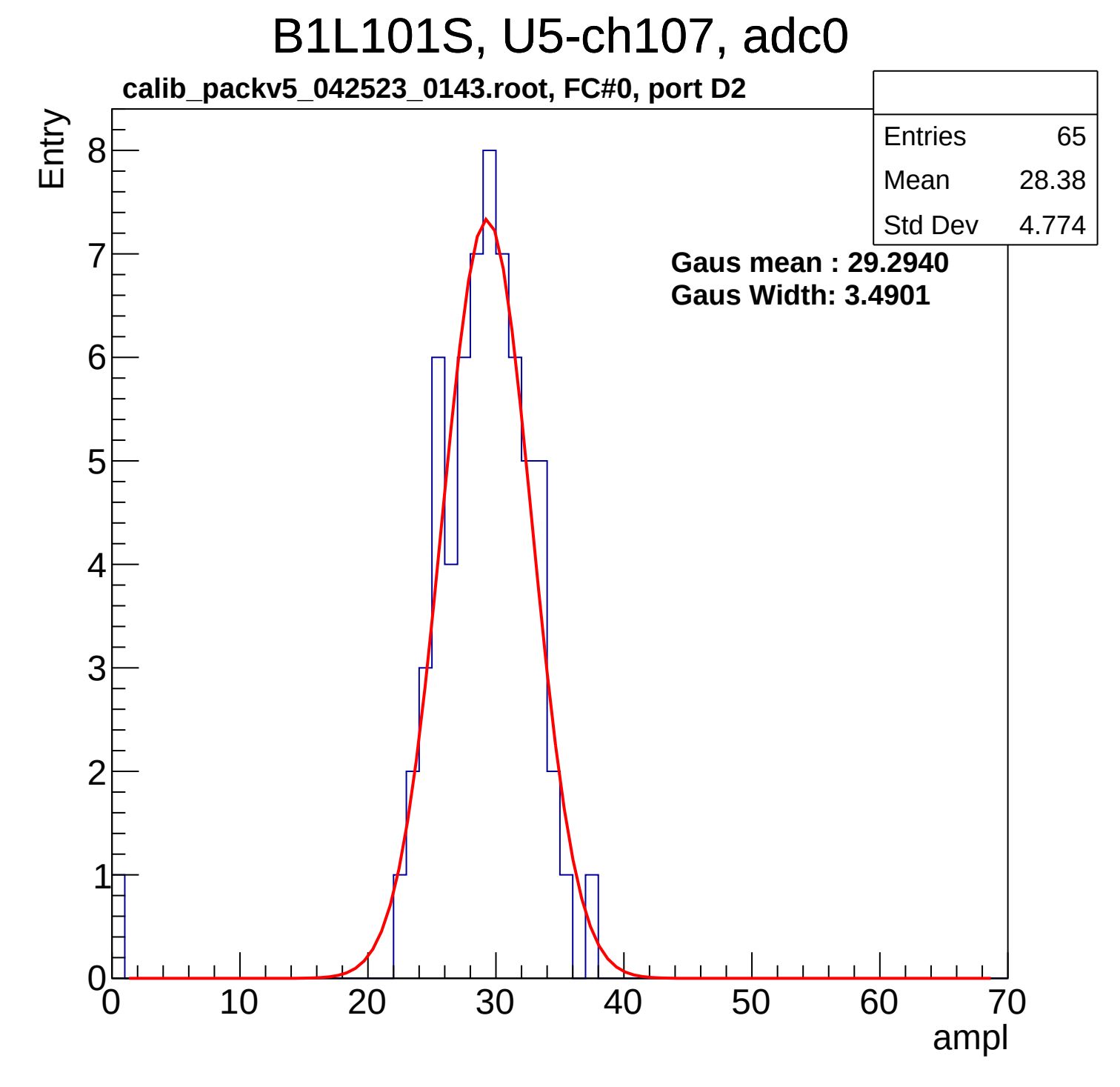
B1L101S, U5-ch107, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 28.38
Std Dev 4.774
Gaus mean : 29.2940
Gaus Width: 3.4901
Entry
ampl
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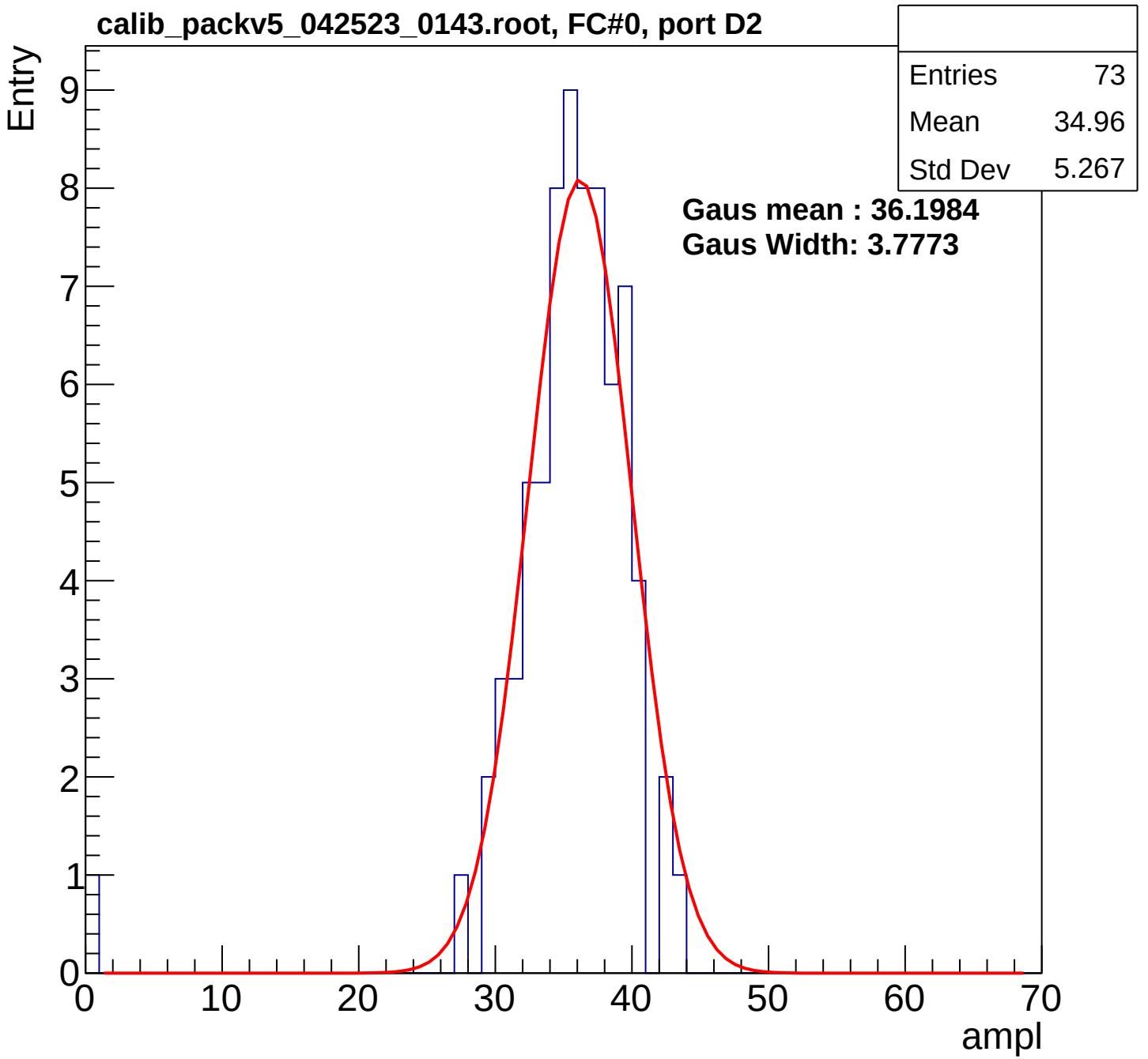
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch107, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 34.96
Std Dev 5.267
Gaus mean : 36.1984
Gaus Width: 3.7773
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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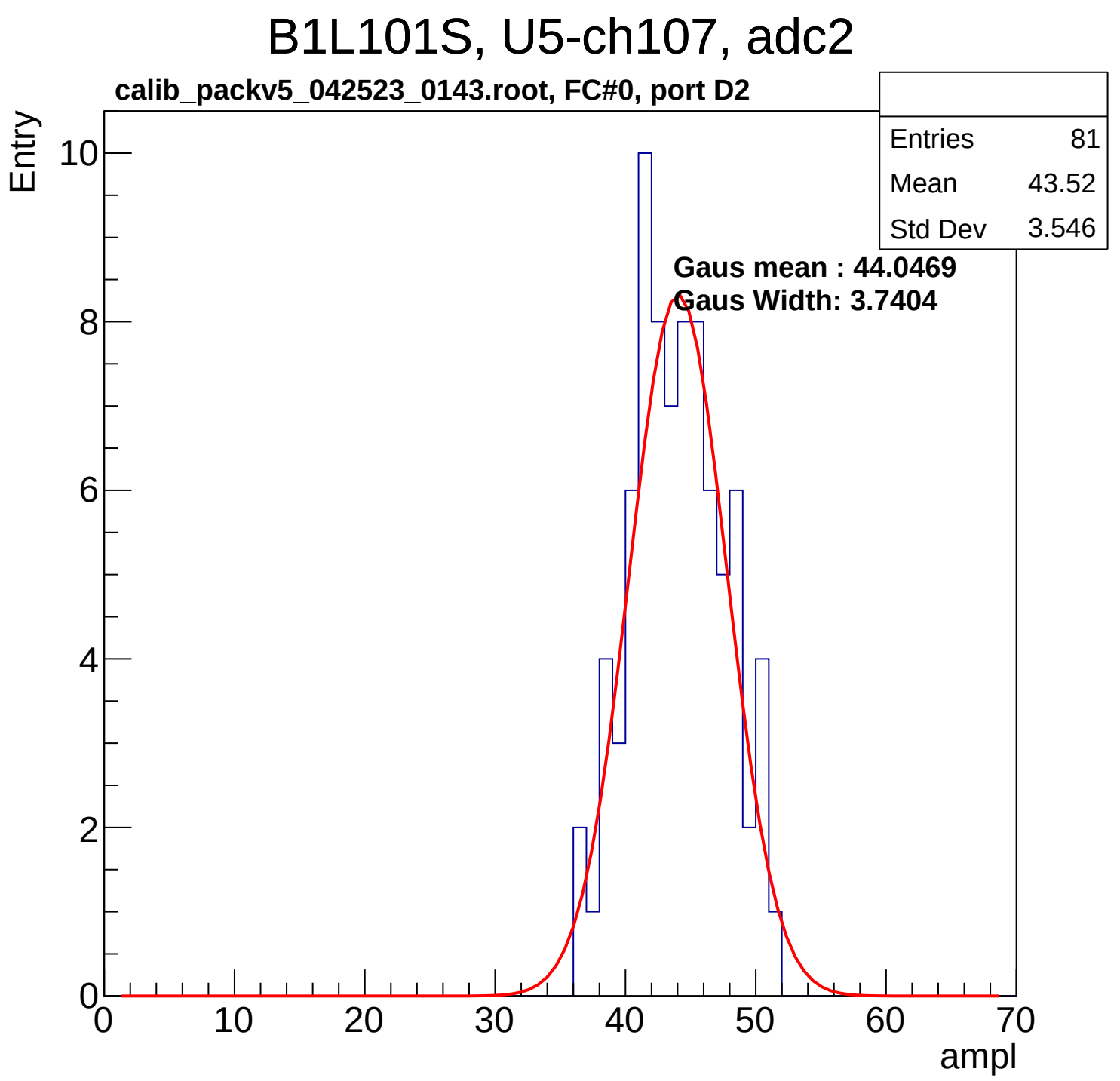
B1L101S, U5-ch107, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 81
Mean 43.52
Std Dev 3.546
Gaus mean : 44.0469
Gaus Width: 3.7404
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
50
60
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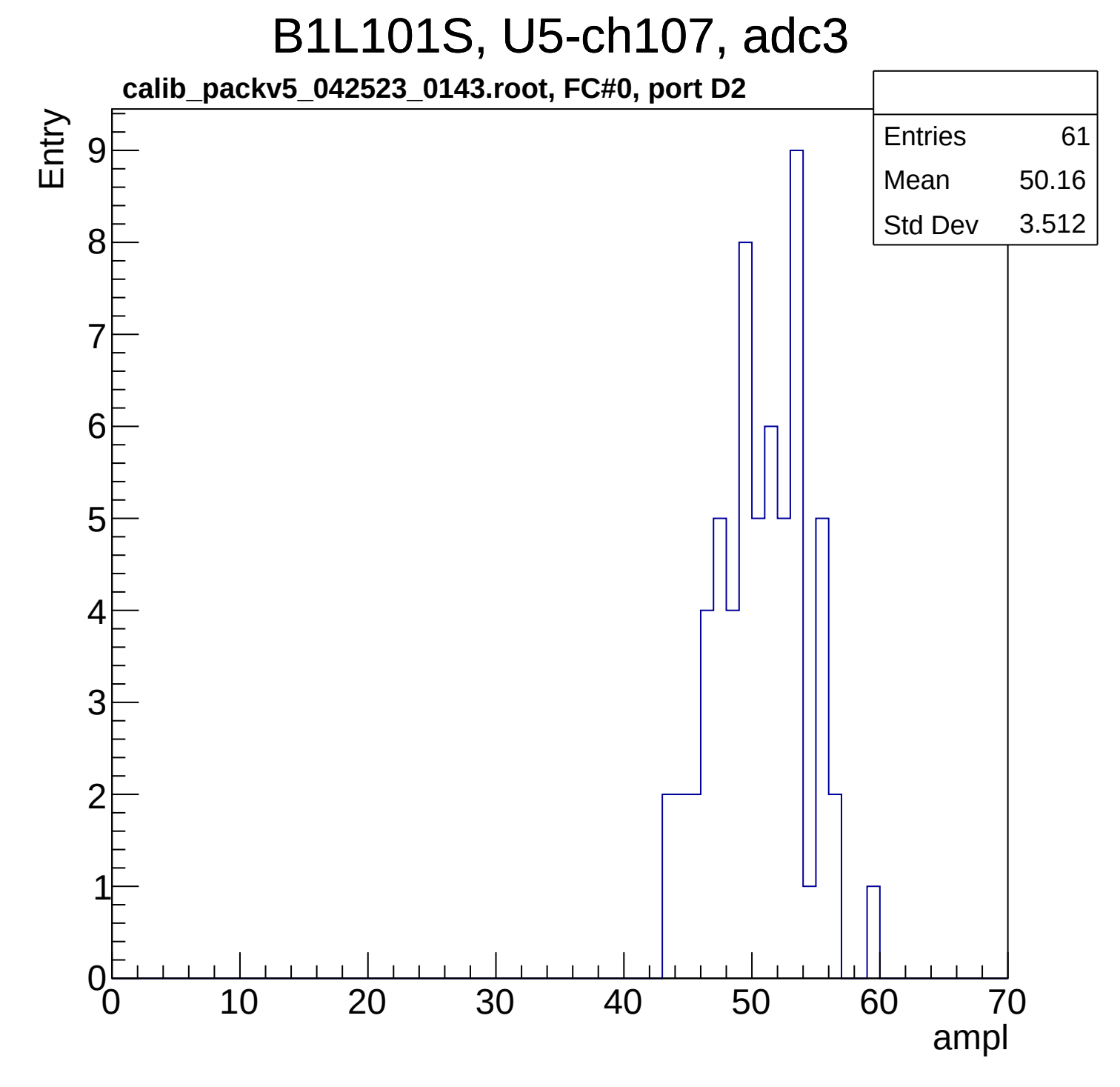
B1L101S, U5-ch107, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 50.16
Std Dev 3.512
Entry
ampl
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4
5
6
7
8
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0
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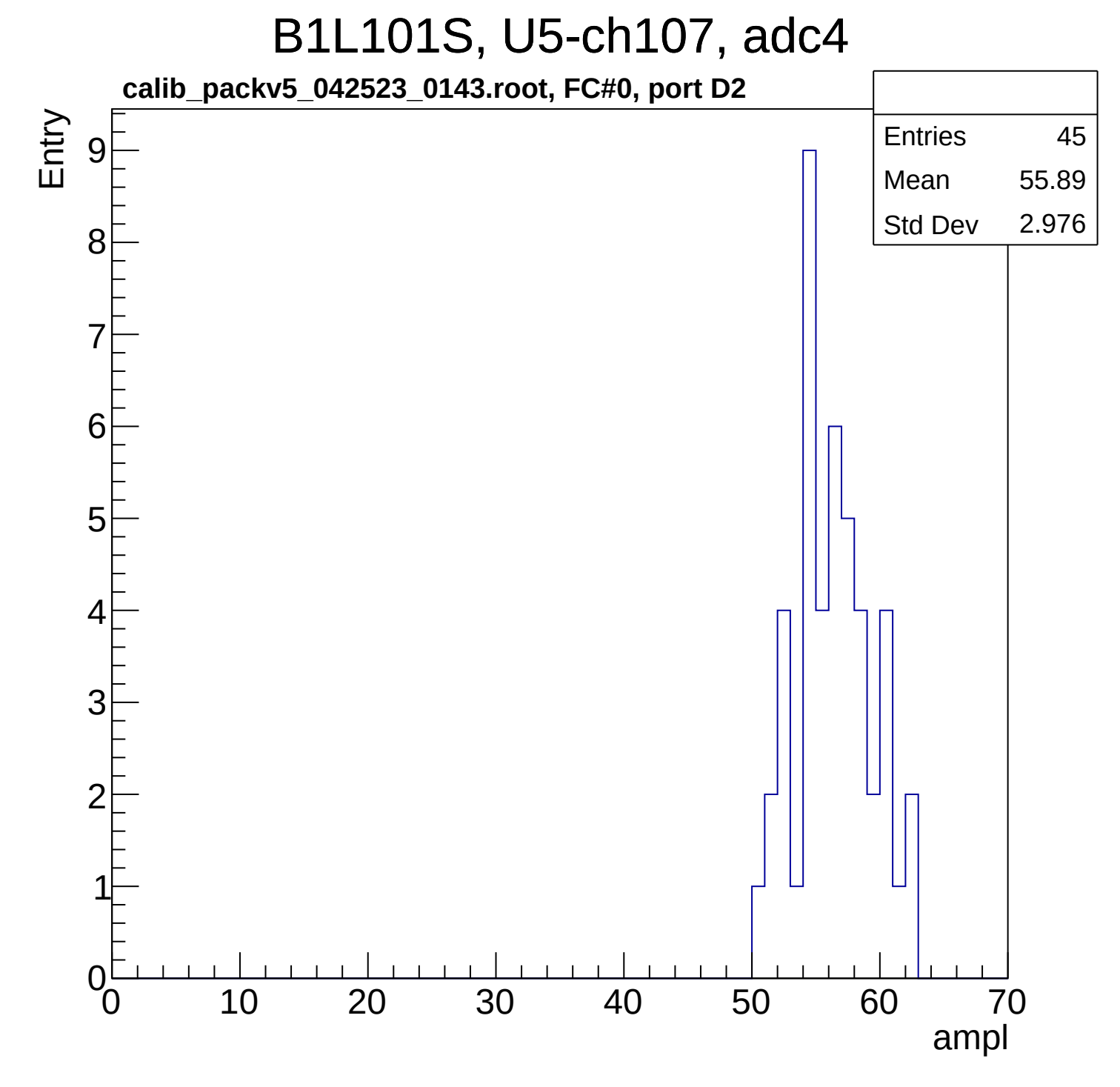
B1L101S, U5-ch107, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 55.89
Std Dev 2.976
Entry
ampl
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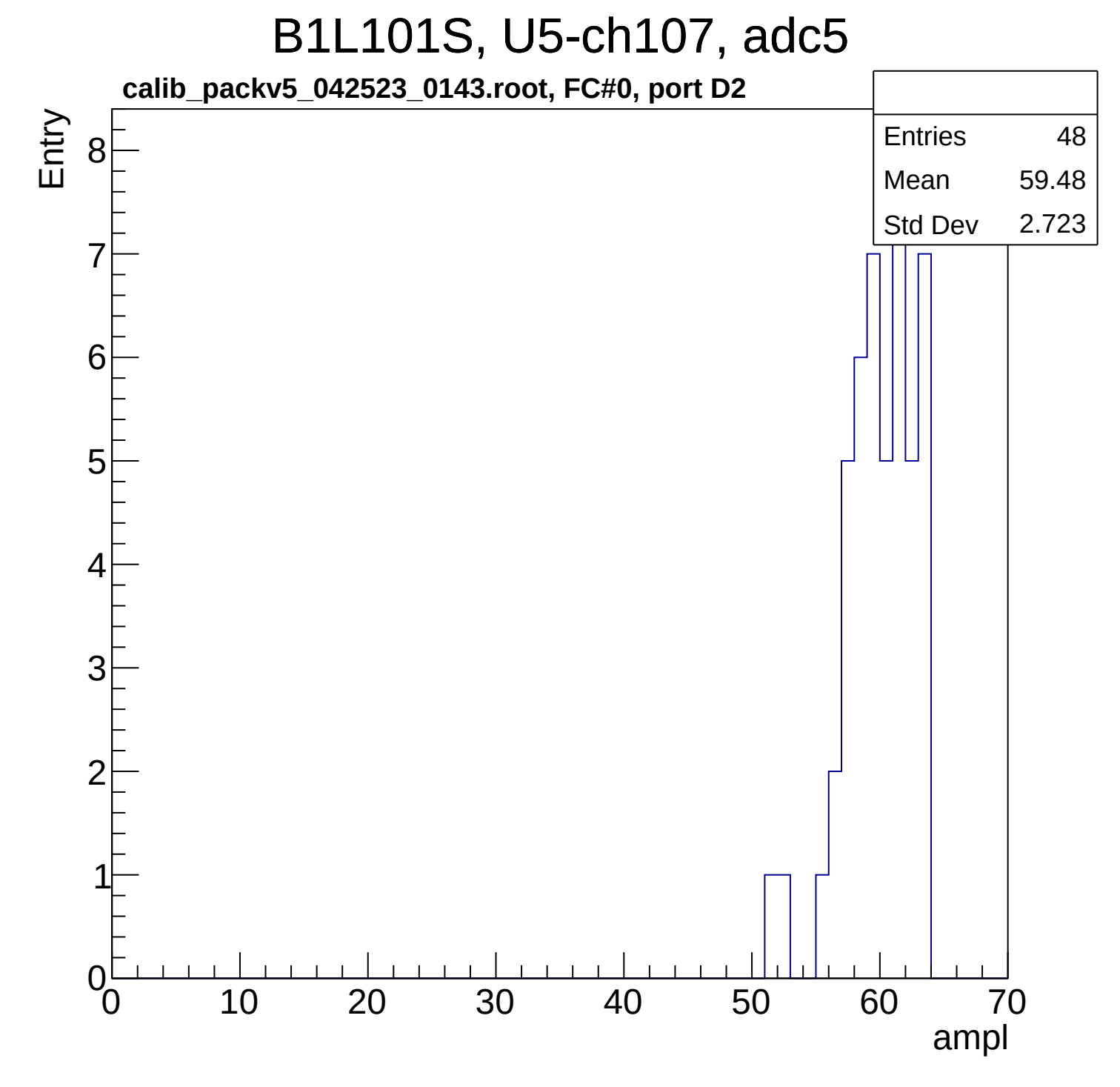
B1L101S, U5-ch107, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 59.48
Std Dev 2.723
Entry
ampl
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4
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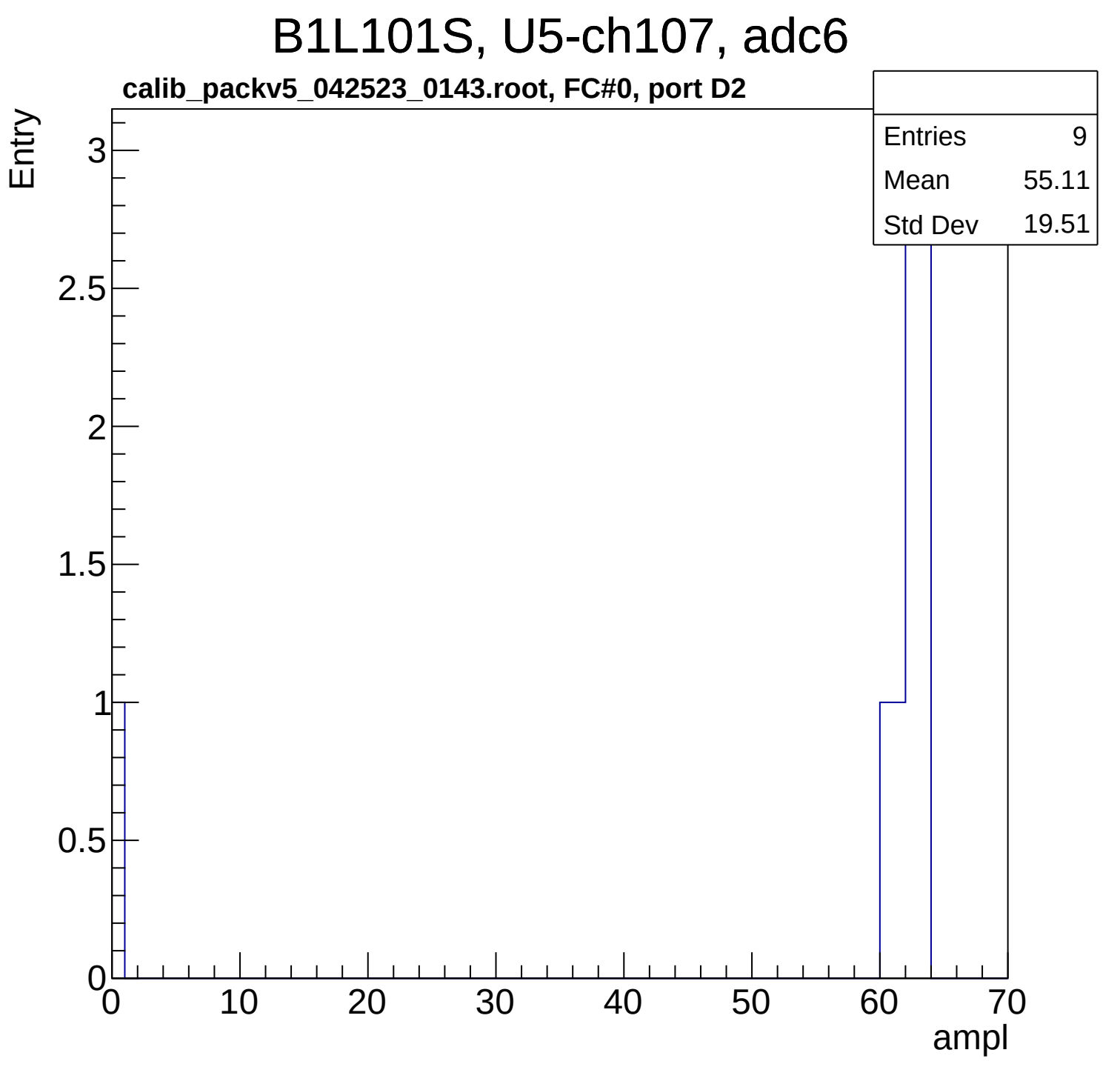
B1L101S, U5-ch107, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 55.11
Std Dev 19.51
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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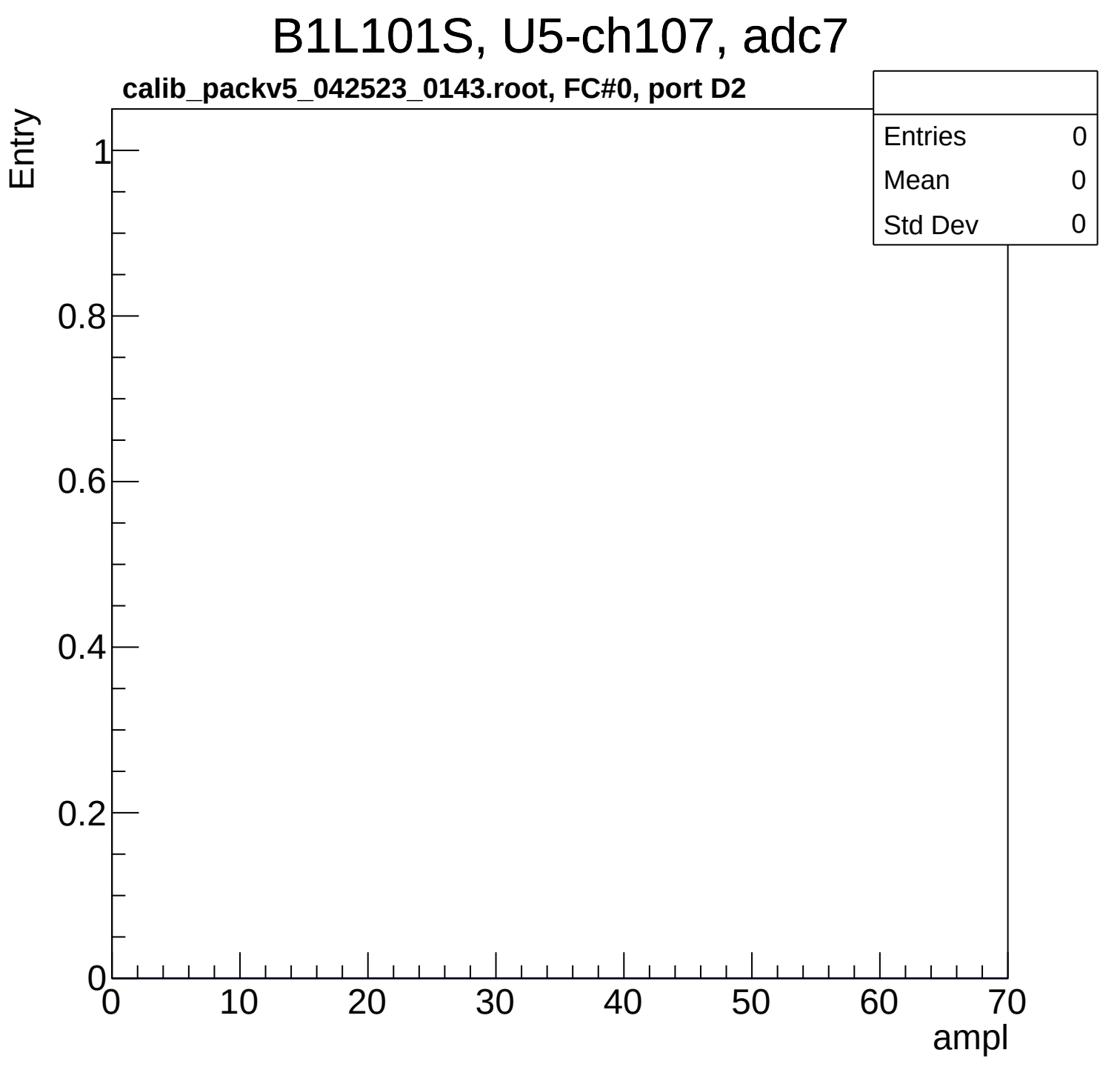
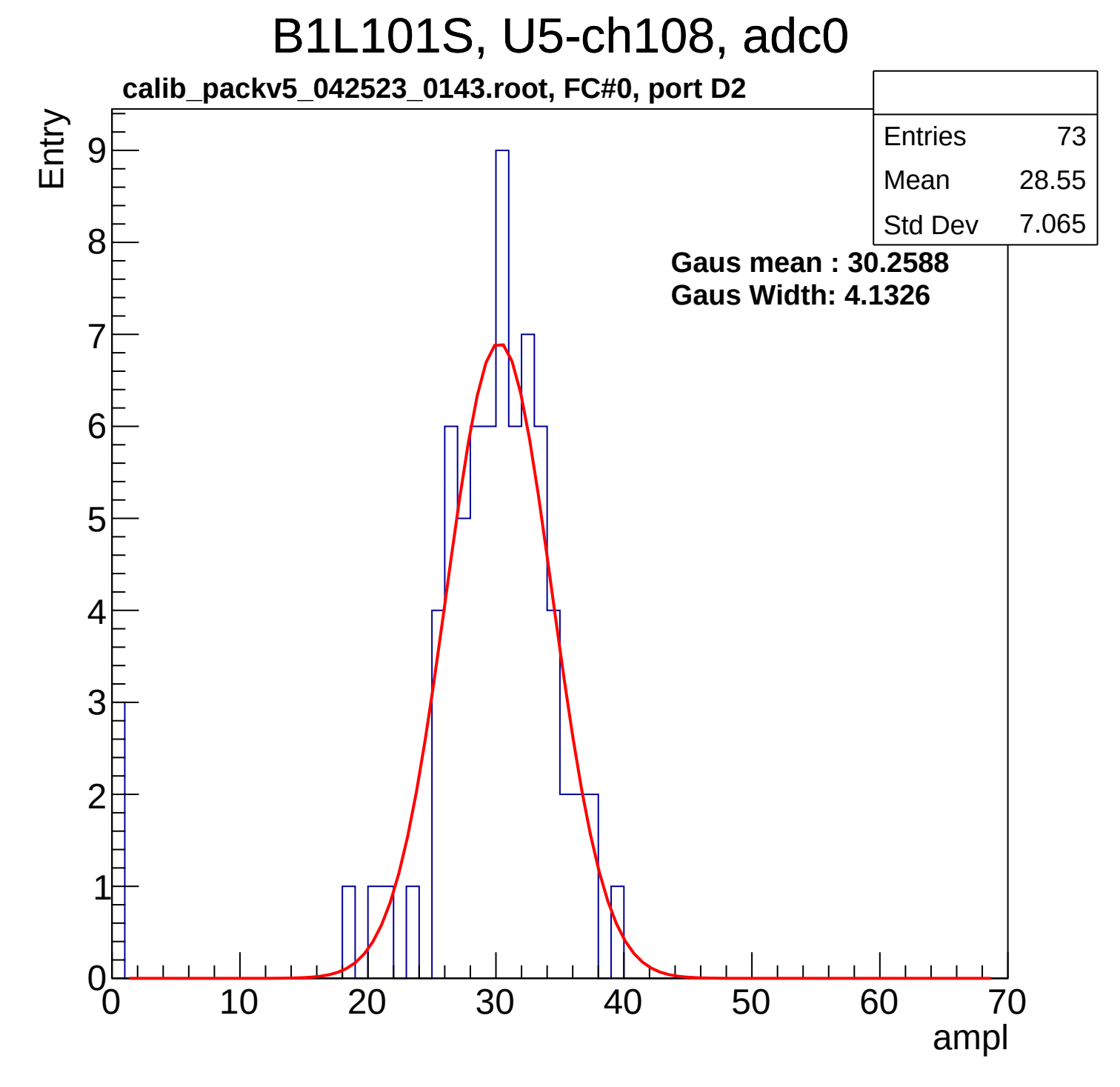
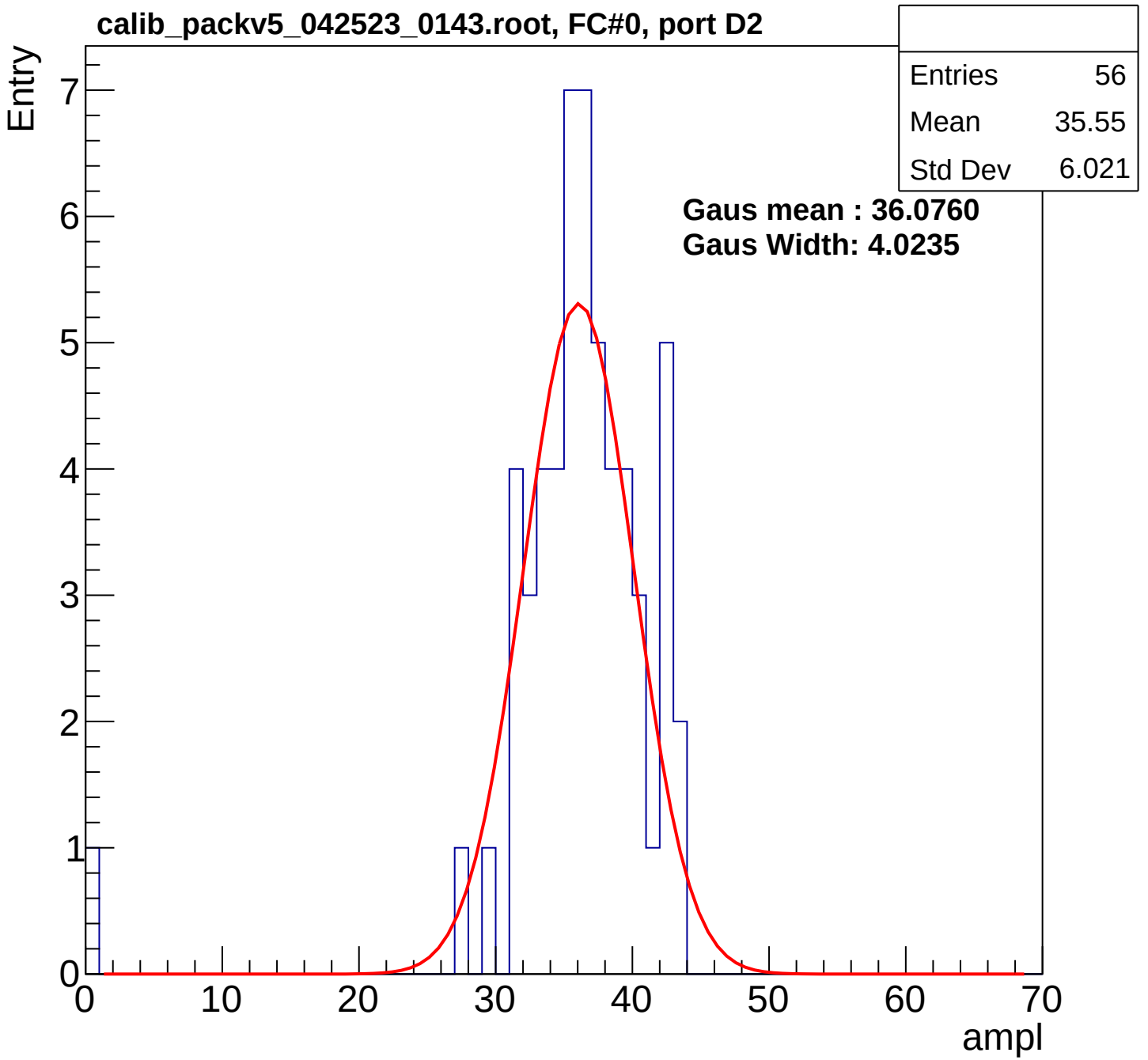
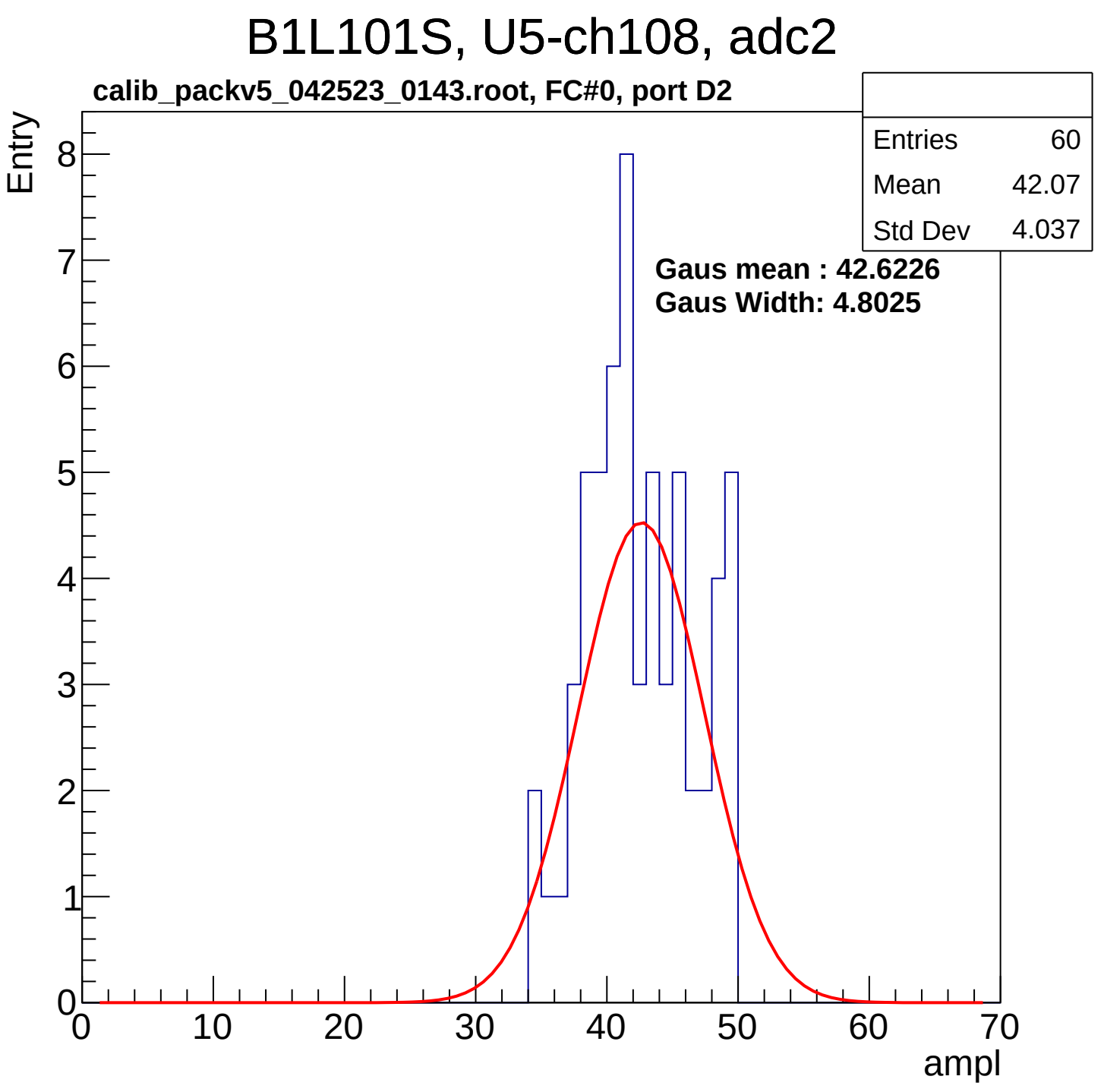
40
50
60
70


B1L101S, U5-ch107, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch108, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 28.55
Std Dev 7.065
Gaus mean : 30.2588
Gaus Width: 4.1326
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch108, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 35.55
Std Dev 6.021
Gaus mean : 36.0760
Gaus Width: 4.0235
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch108, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 42.07
Std Dev 4.037
Gaus mean : 42.6226
Gaus Width: 4.8025
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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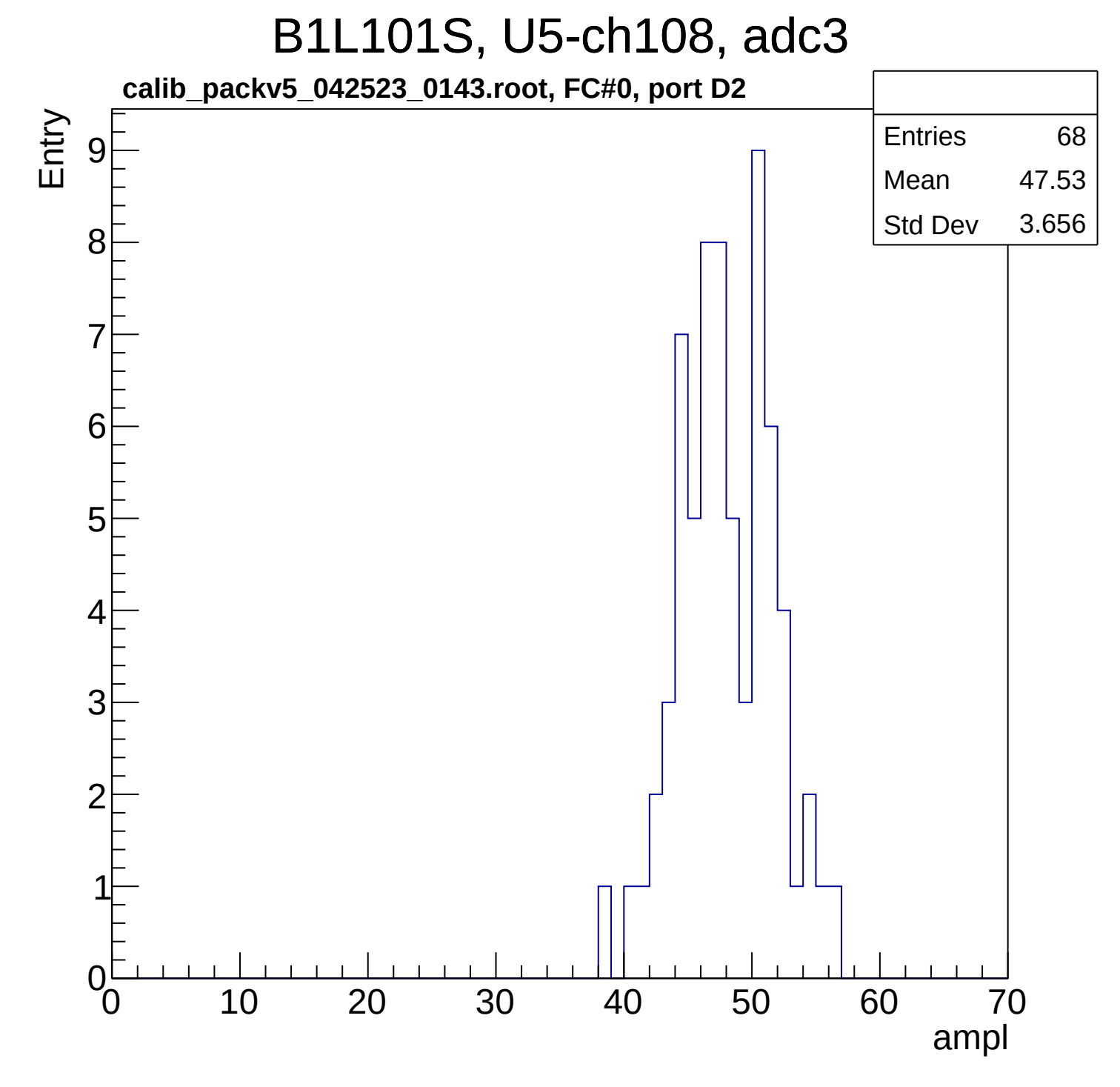
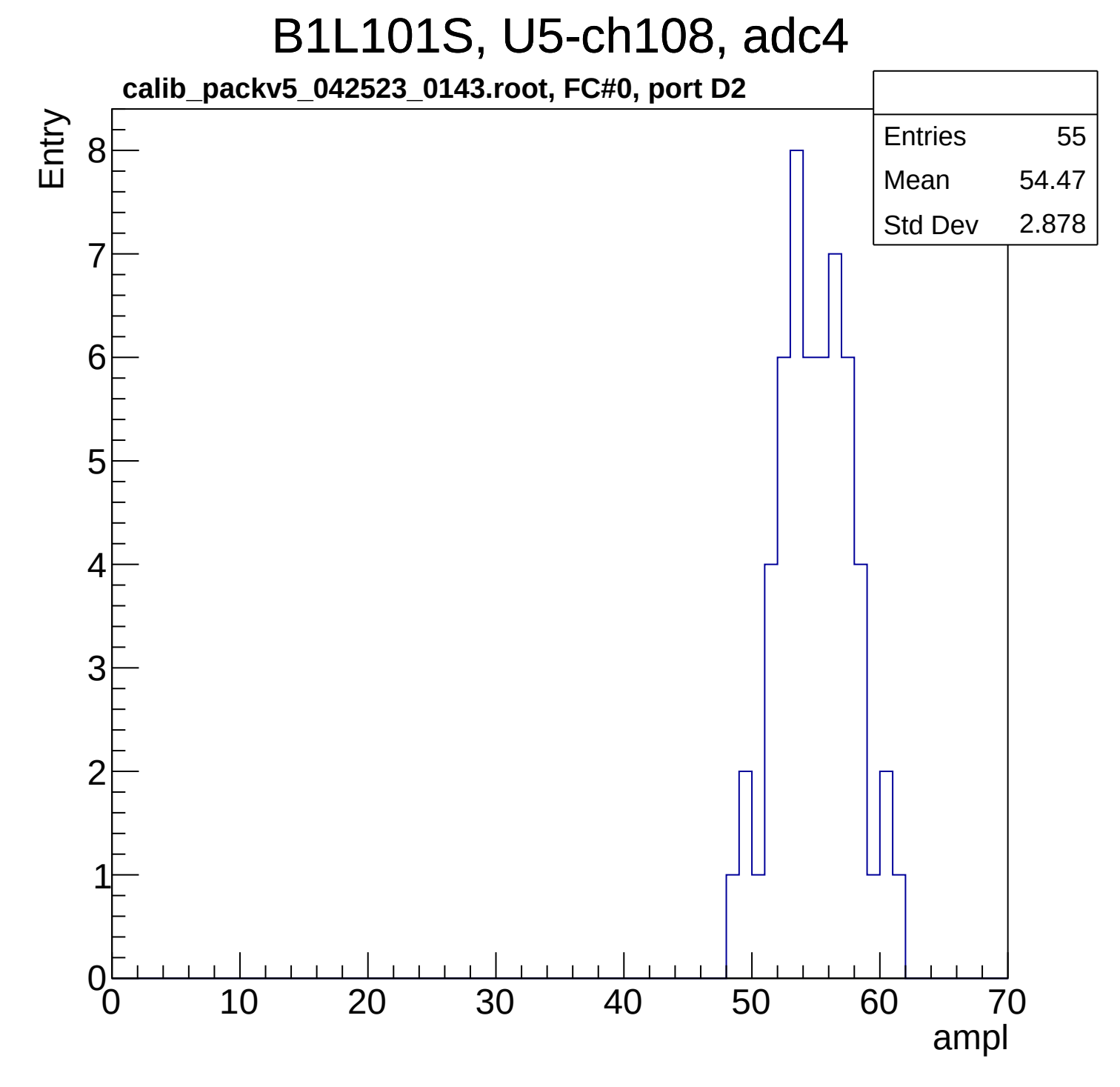

B1L101S, U5-ch108, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 47.53
Std Dev 3.656
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch108, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 54.47
Std Dev 2.878
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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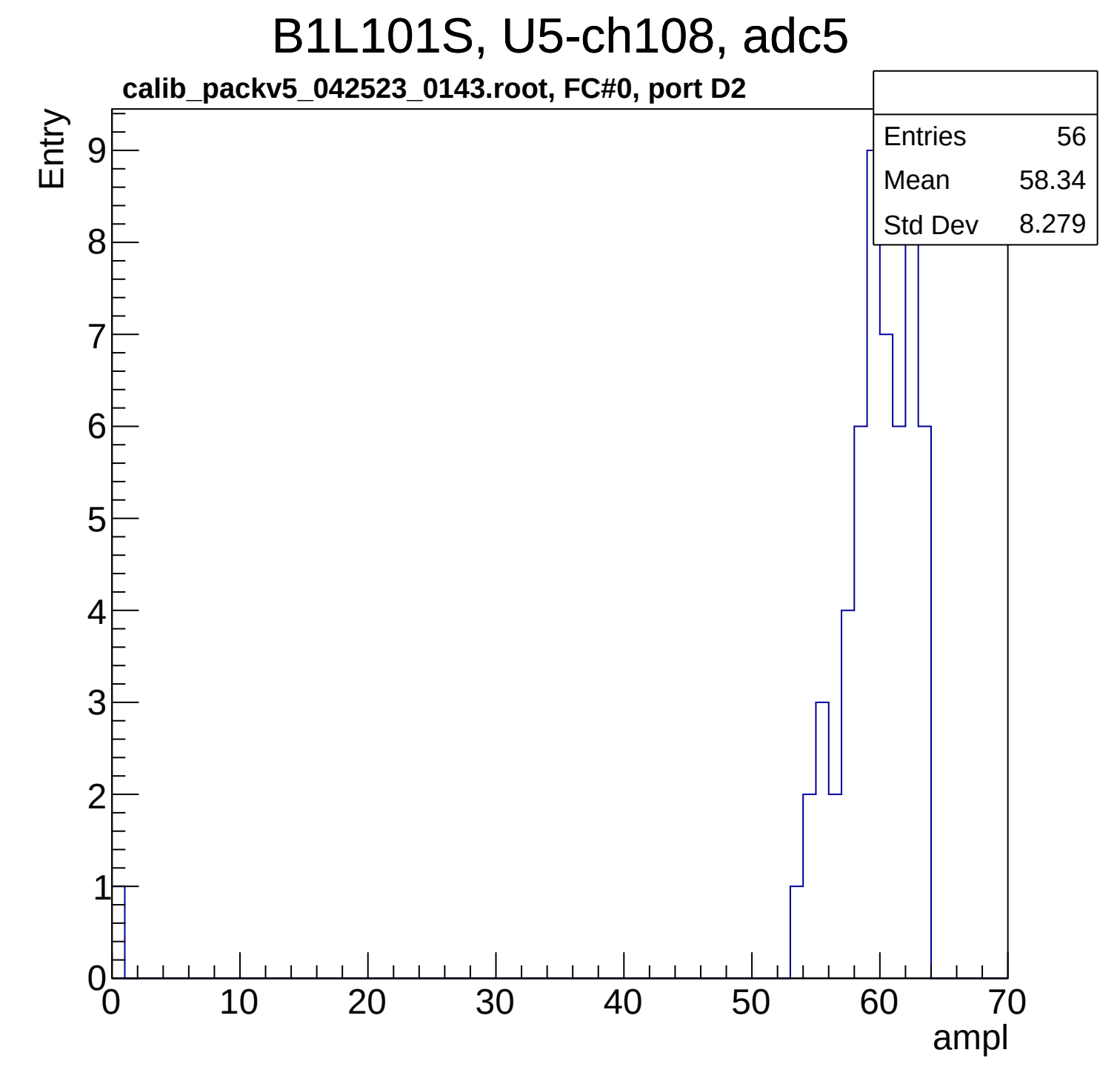
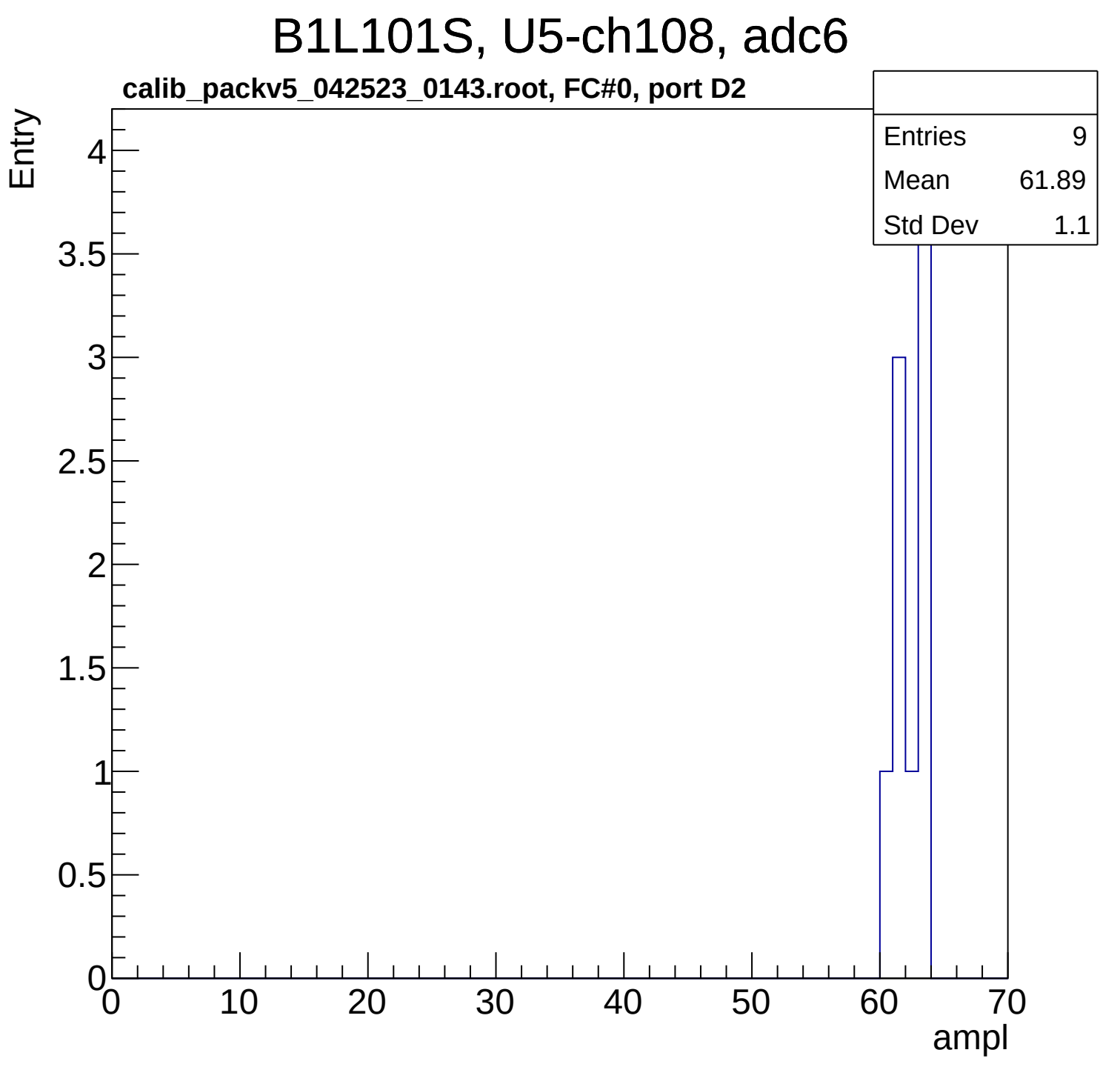
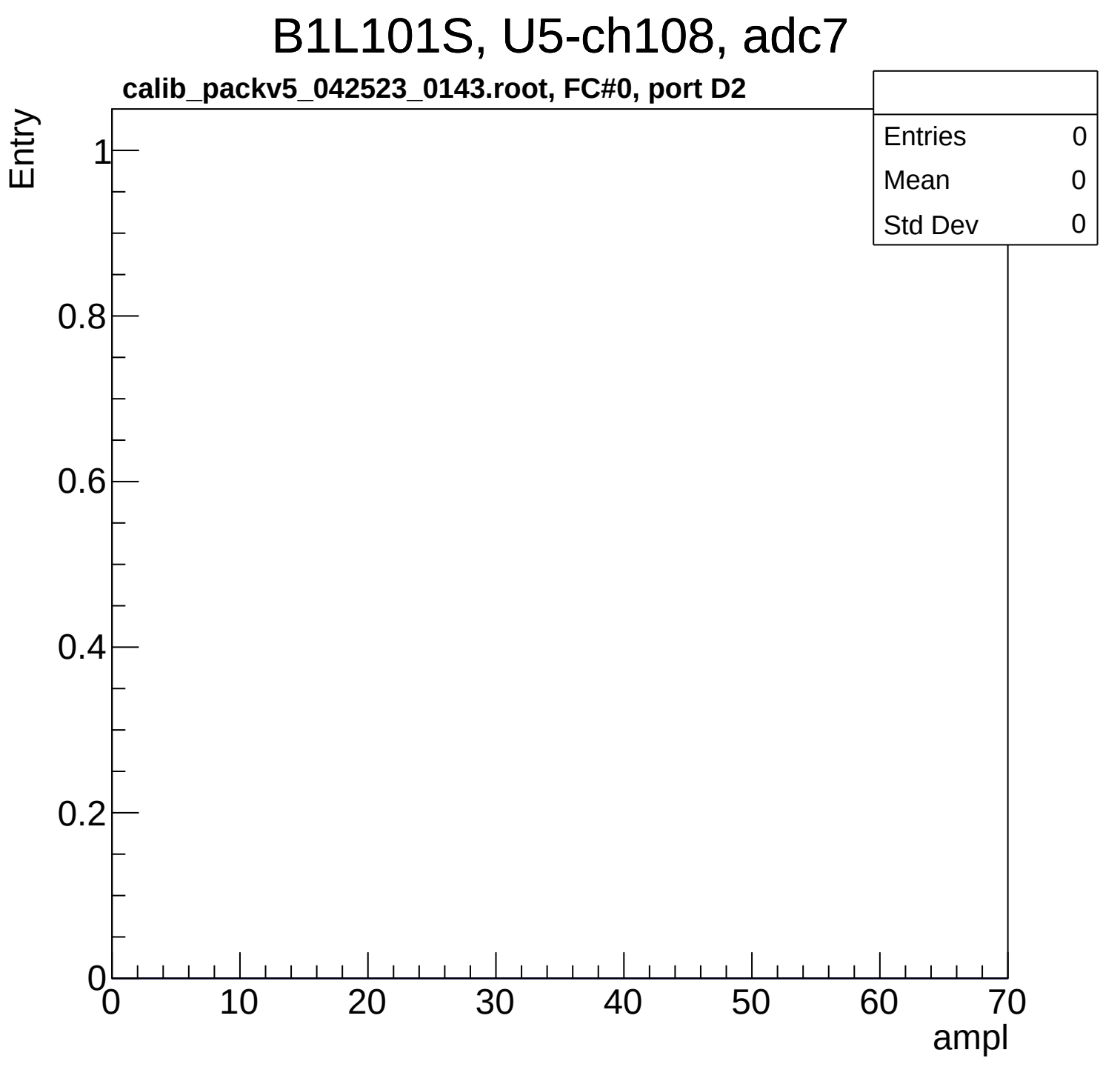
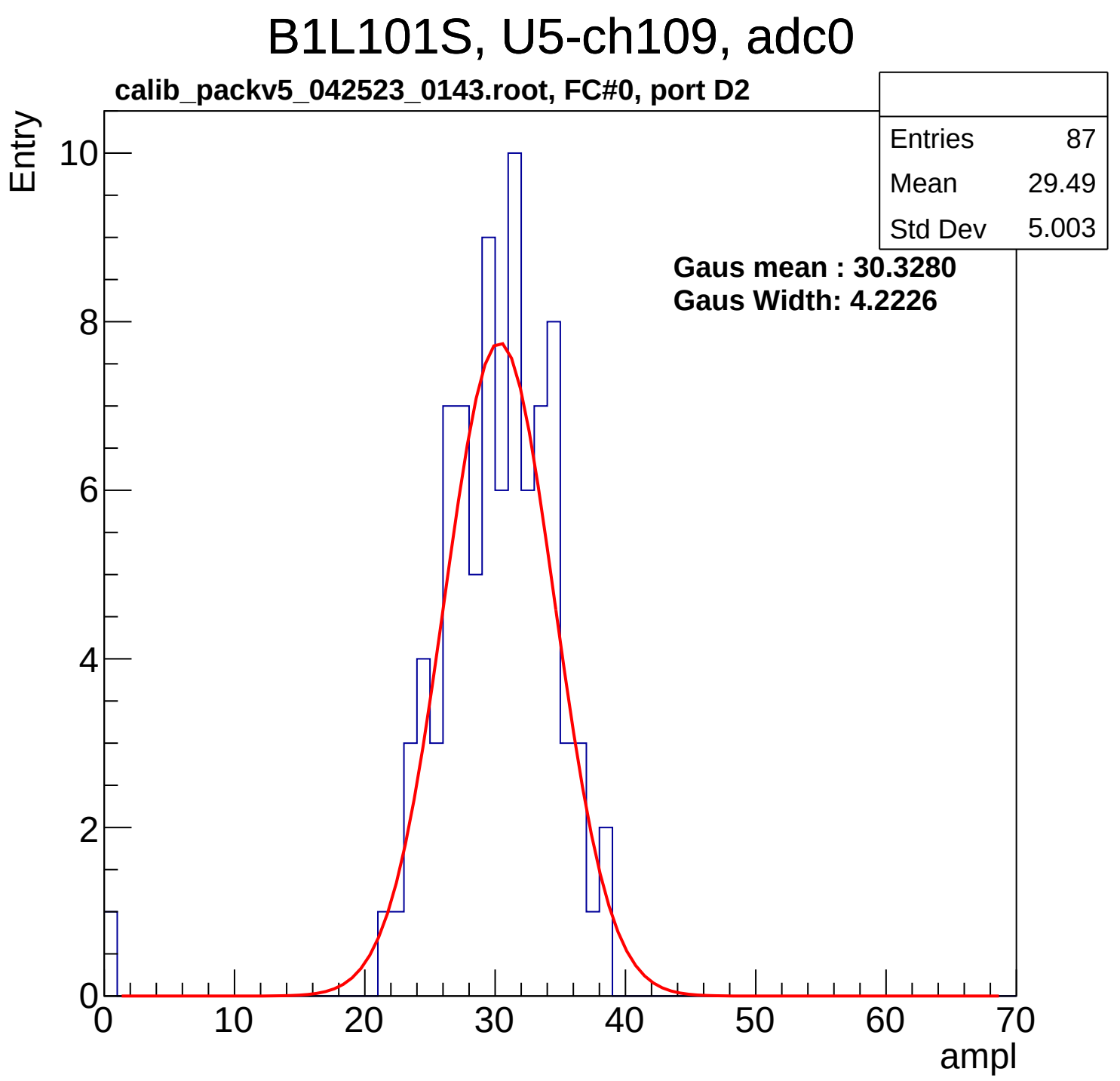
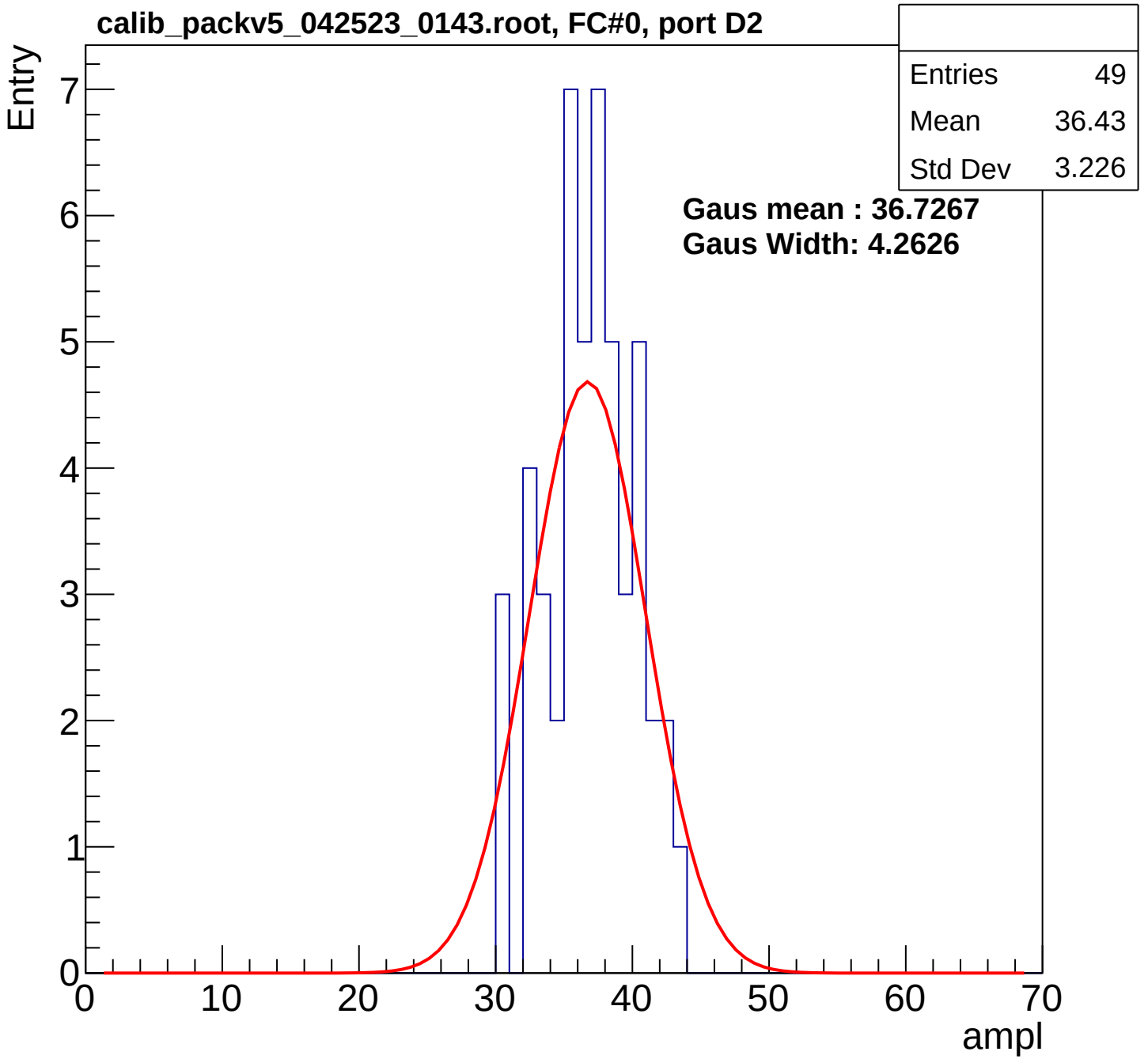
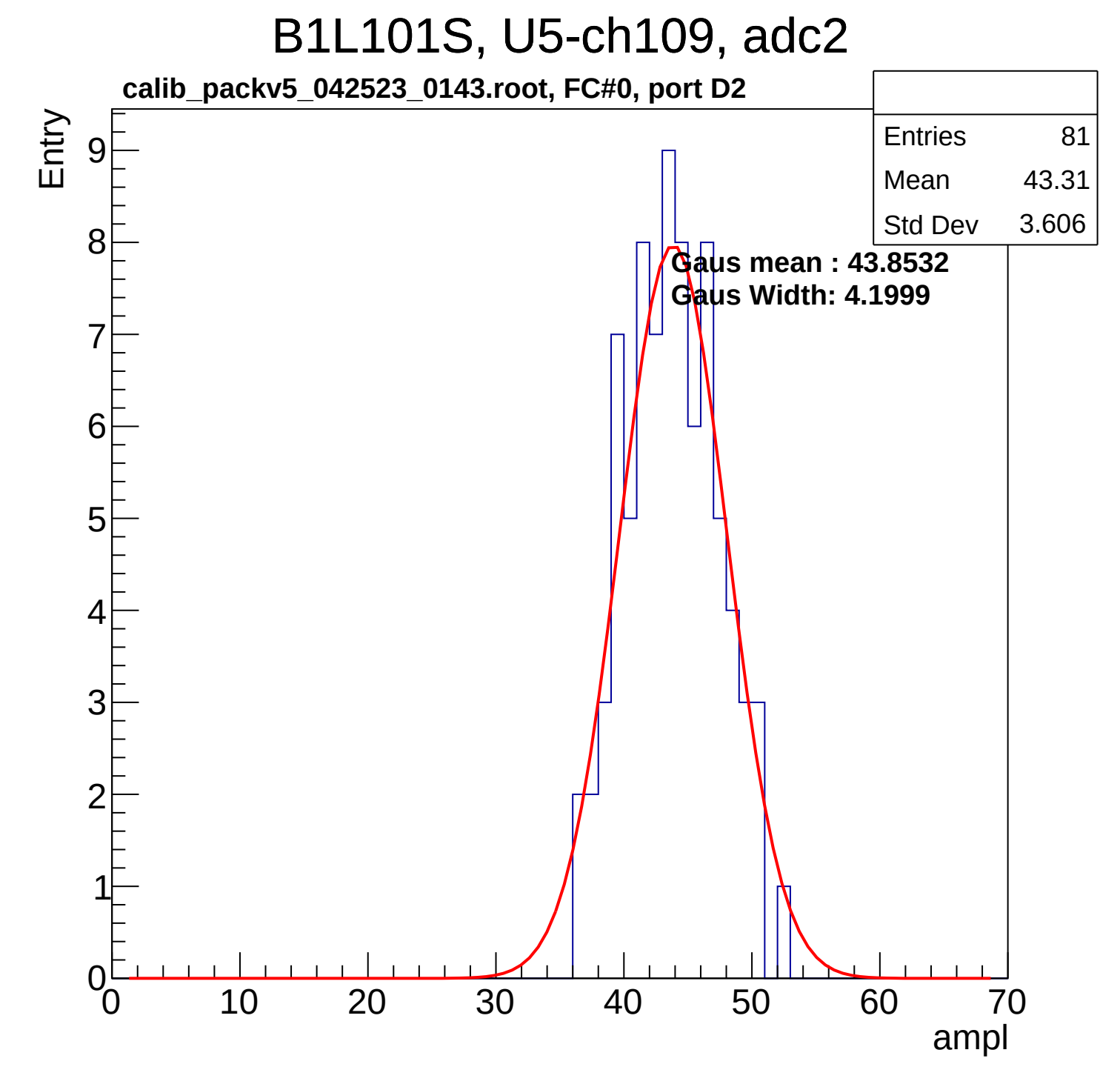

B1L101S, U5-ch108, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 58.34
Std Dev 8.279
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch108, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 61.89
Std Dev 1.1
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L101S, U5-ch108, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch109, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 87
Mean 29.49
Std Dev 5.003
Gaus mean : 30.3280
Gaus Width: 4.2226
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch109, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 36.43
Std Dev 3.226
Gaus mean : 36.7267
Gaus Width: 4.2626
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch109, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 81
Mean 43.31
Std Dev 3.606
Gaus mean : 43.8532
Gaus Width: 4.1999
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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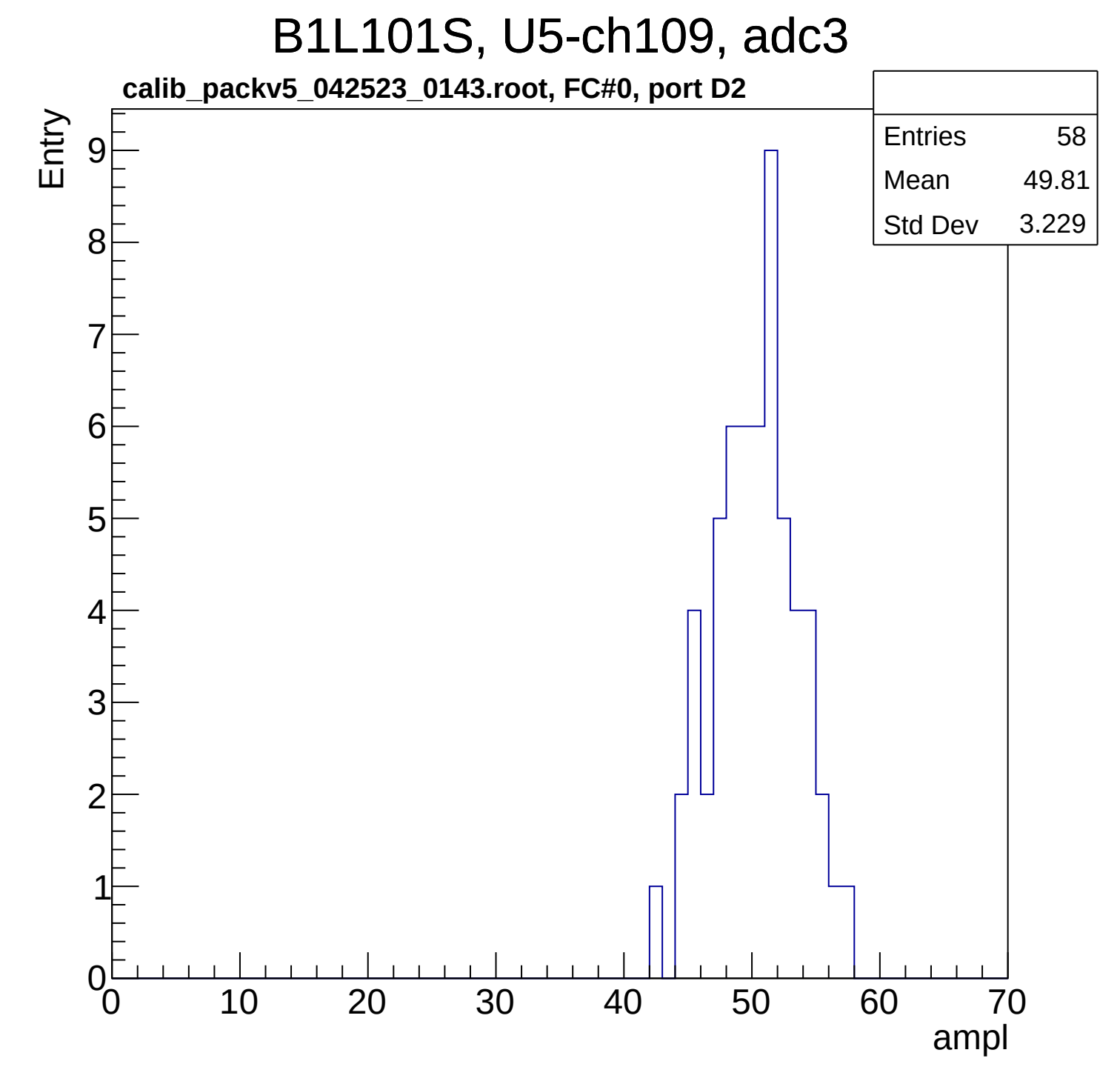
B1L101S, U5-ch109, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 49.81
Std Dev 3.229
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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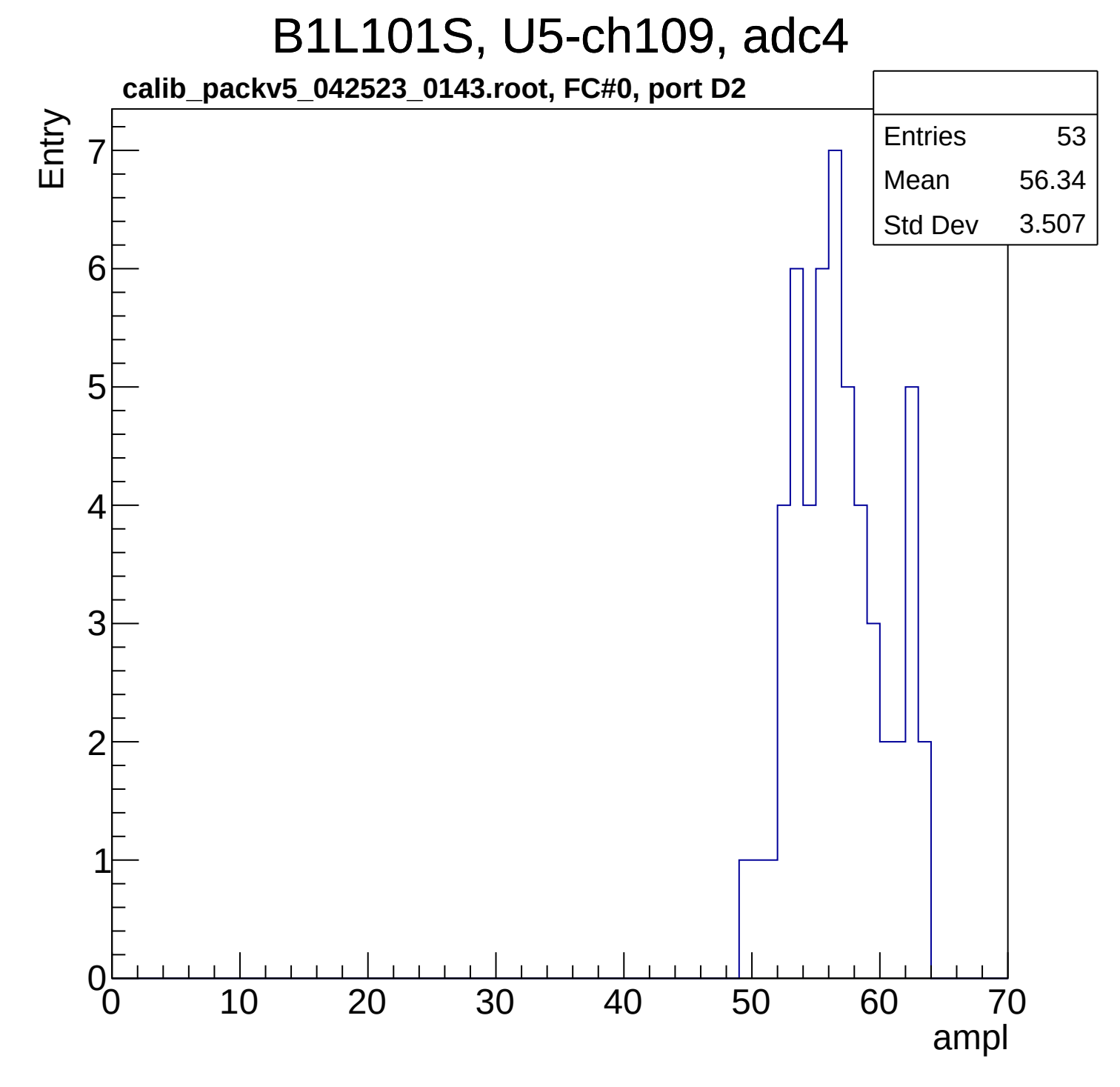
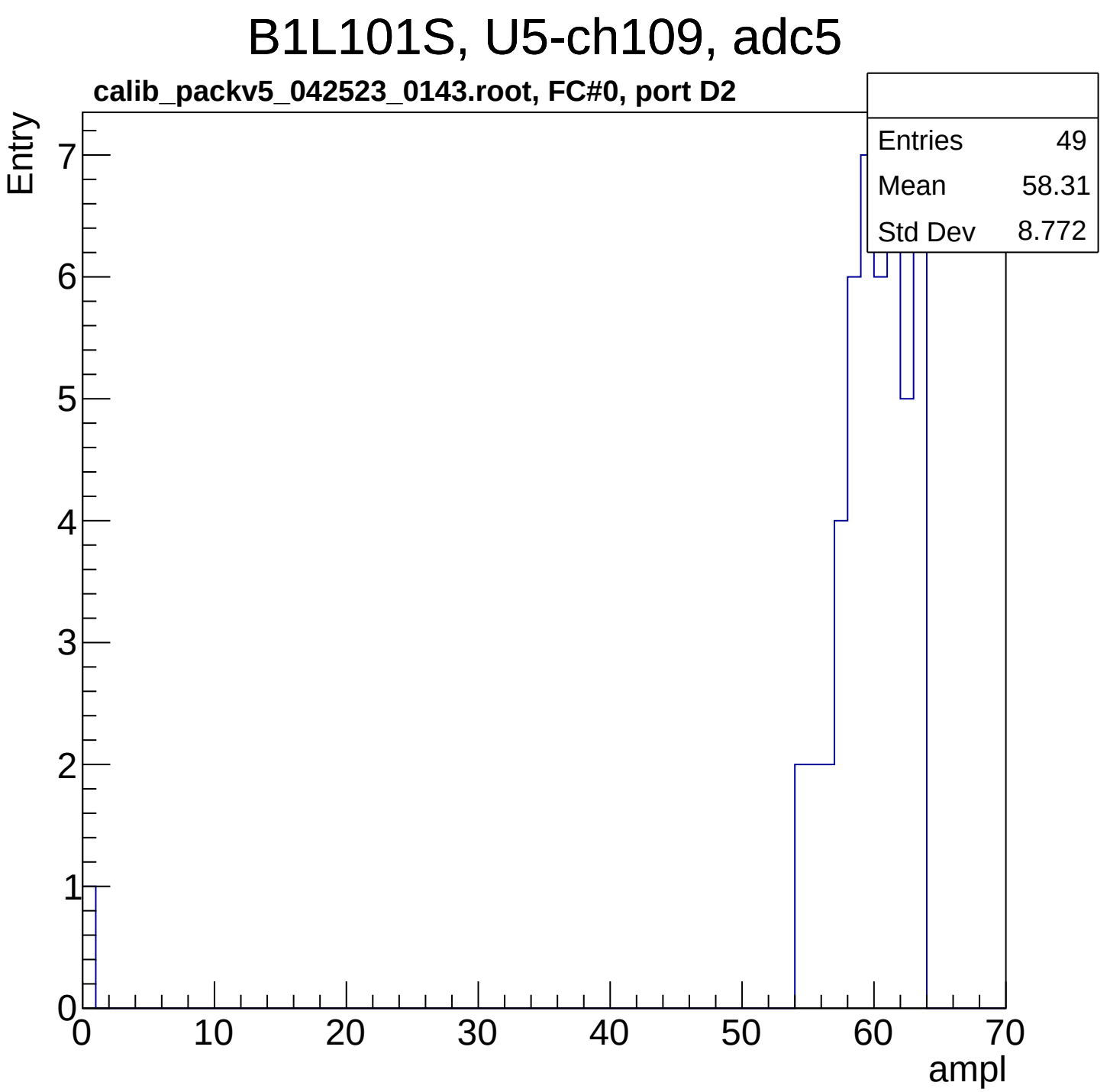
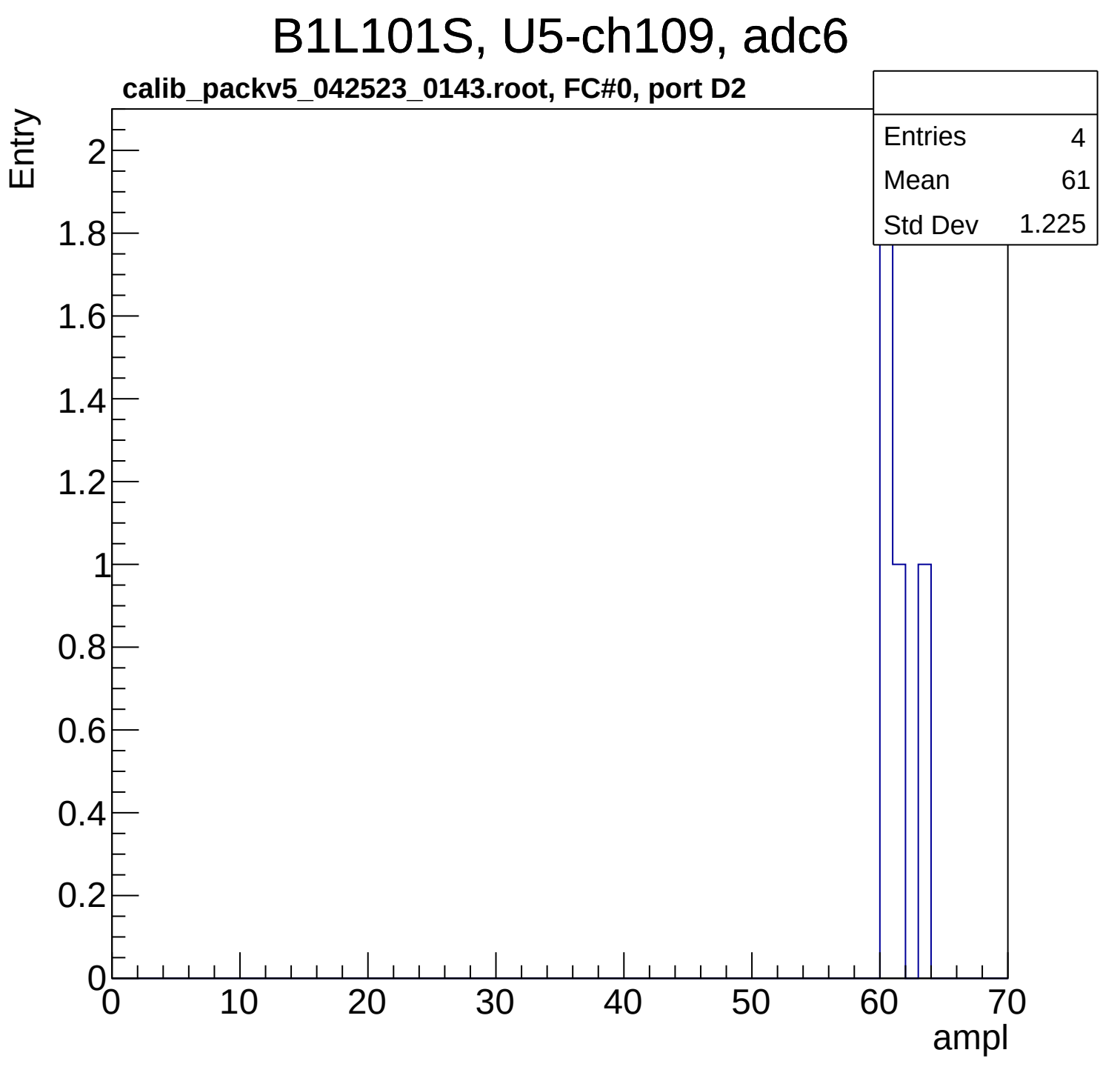
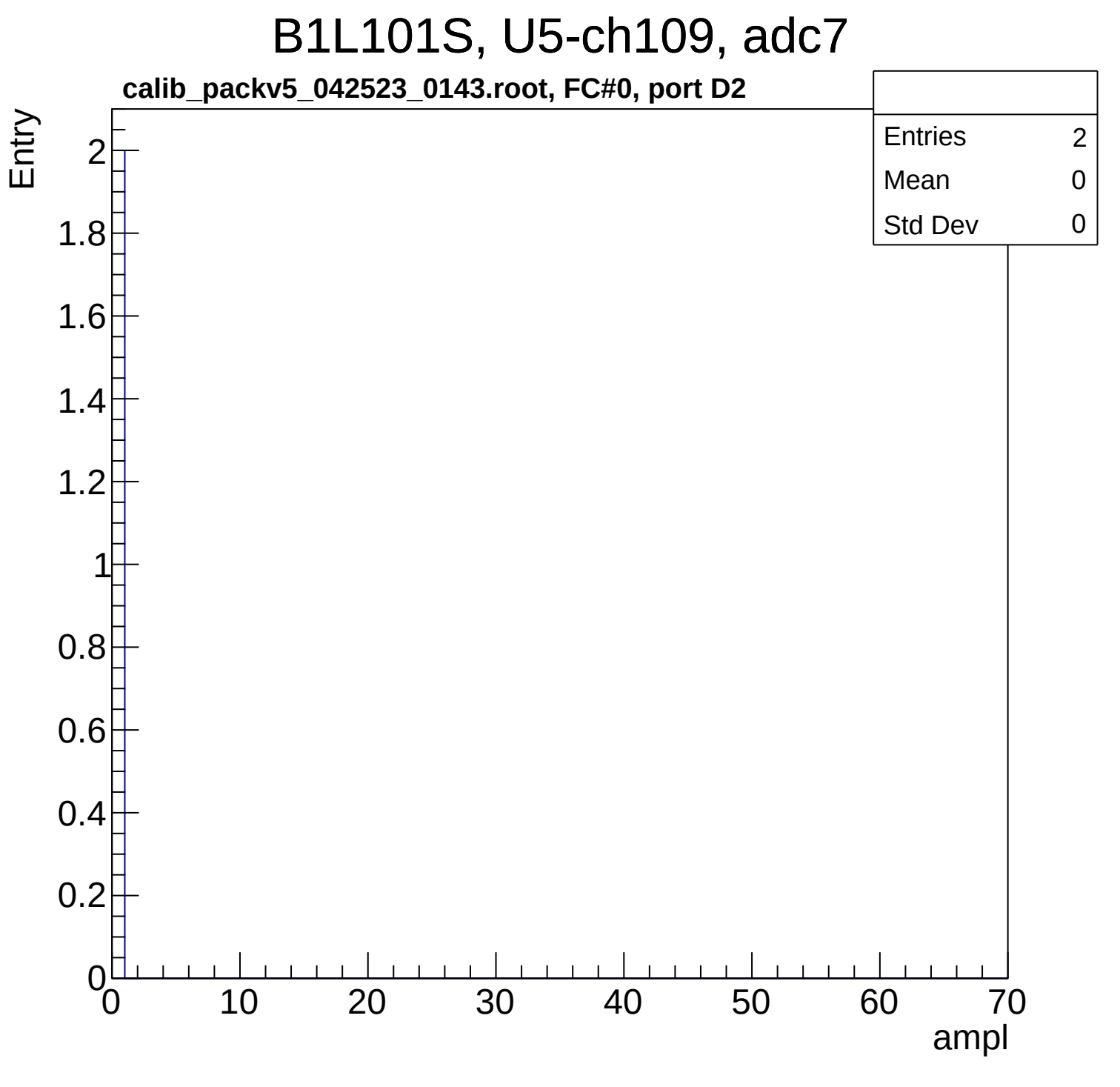
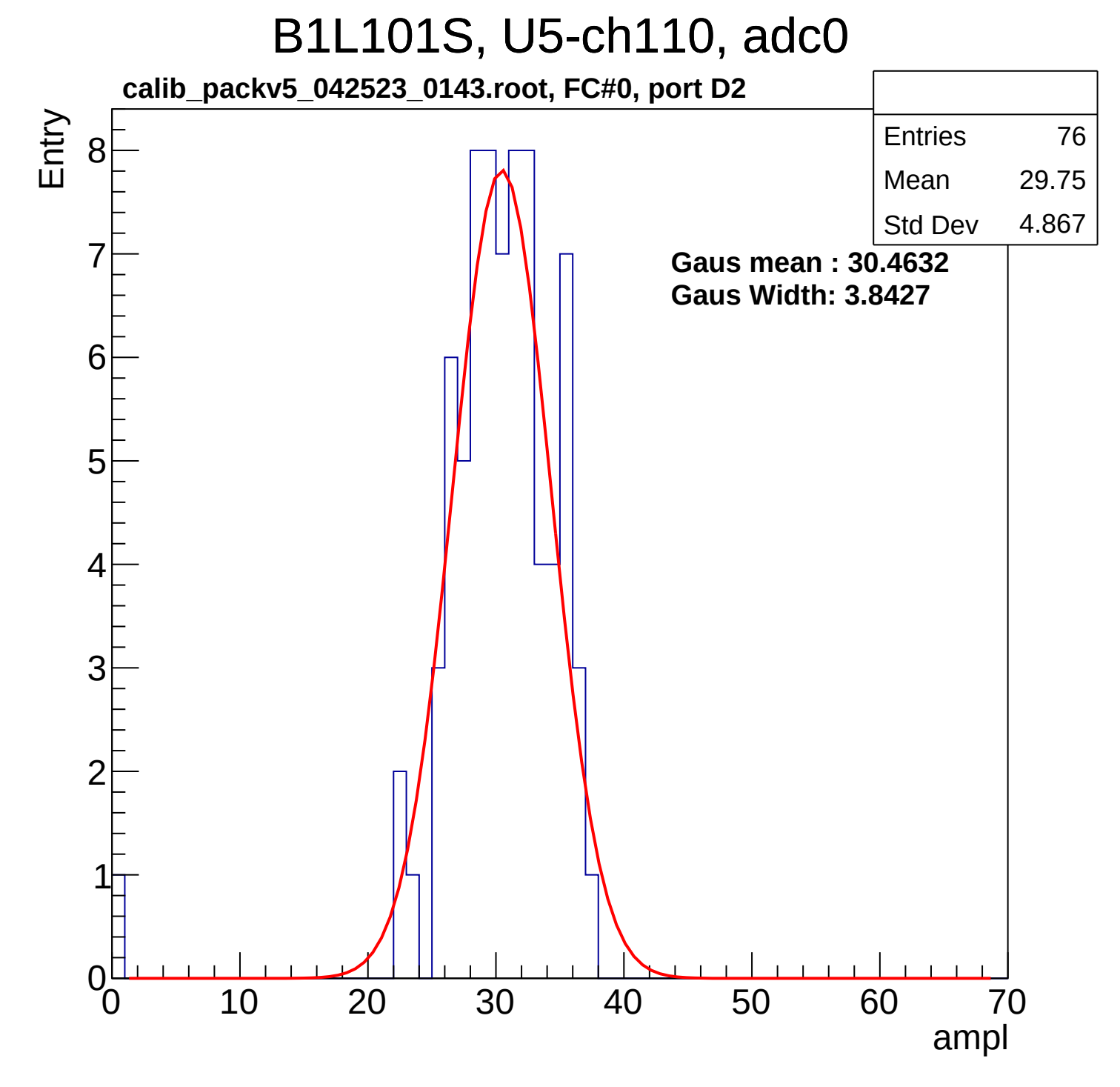
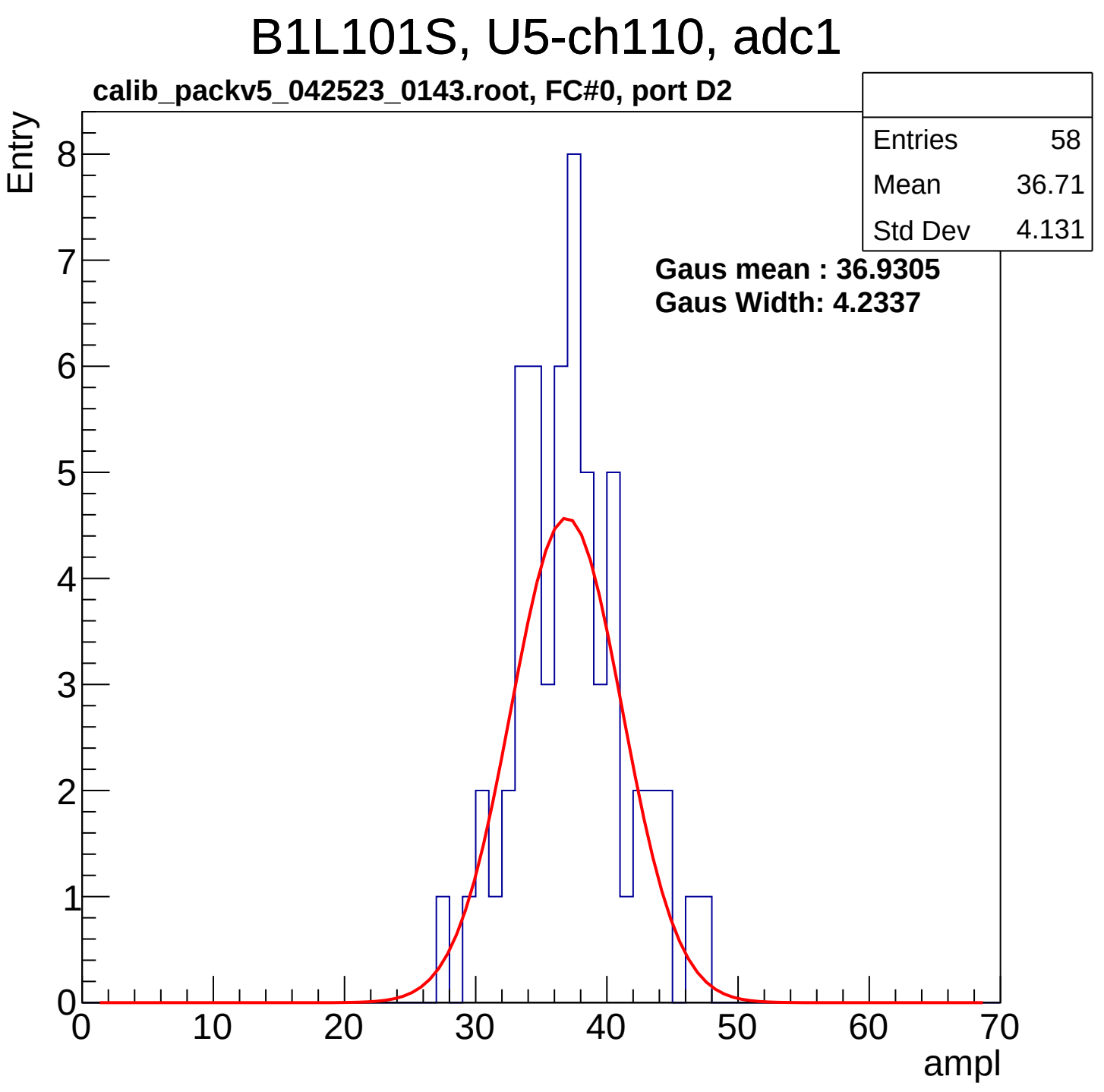

B1L101S, U5-ch109, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 56.34
Std Dev 3.507
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

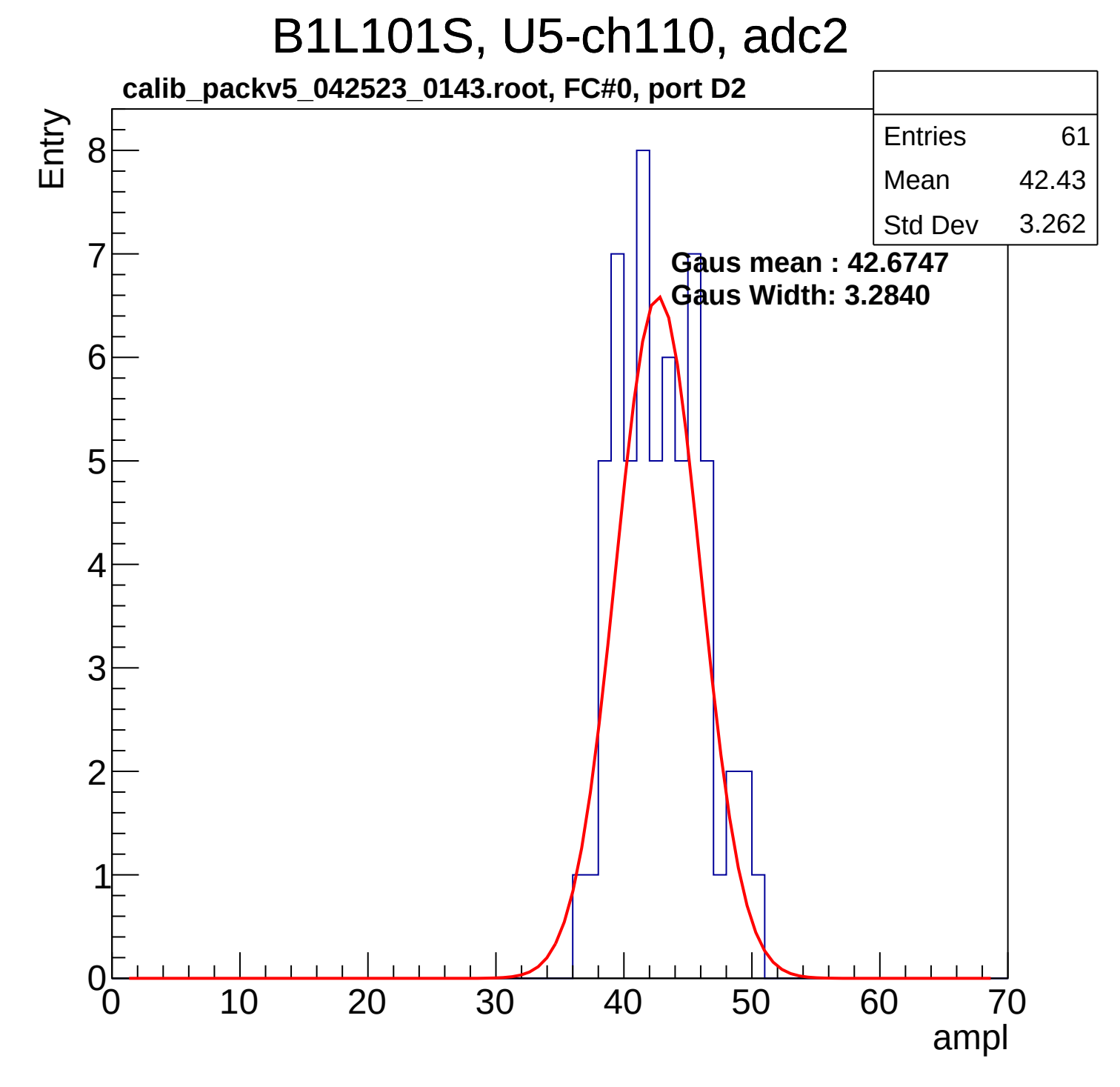

B1L101S, U5-ch109, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 58.31
Std Dev 8.772
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch109, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 61
Std Dev 1.225
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U5-ch109, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch110, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 29.75
Std Dev 4.867
Gaus mean : 30.4632
Gaus Width: 3.8427
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch110, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 36.71
Std Dev 4.131
Gaus mean : 36.9305
Gaus Width: 4.2337
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch110, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 42.43
Std Dev 3.262
Gaus mean : 42.6747
Gaus Width: 3.2840
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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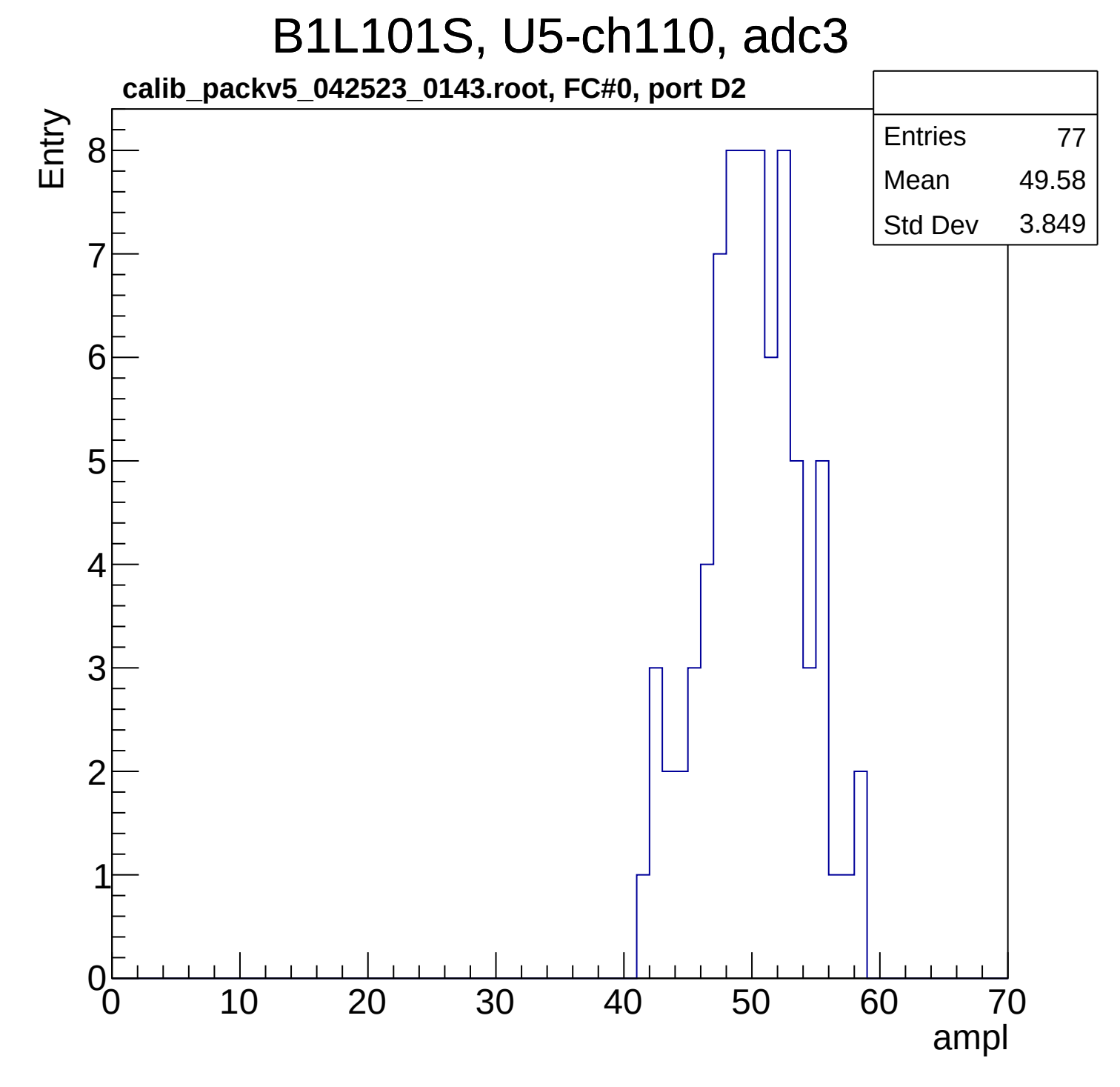
40
50
60
70


B1L101S, U5-ch110, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 49.58
Std Dev 3.849
Entry
ampl
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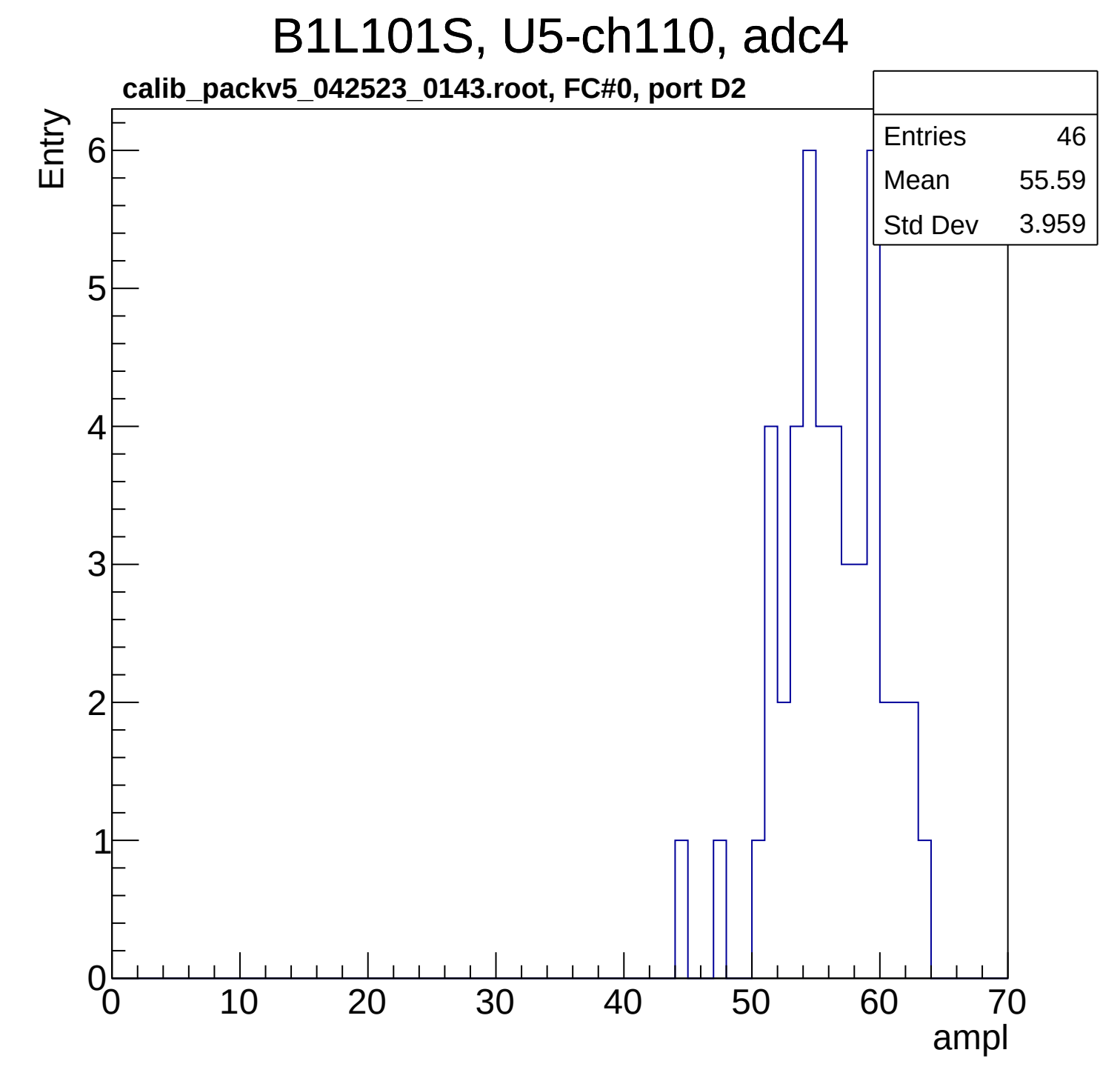
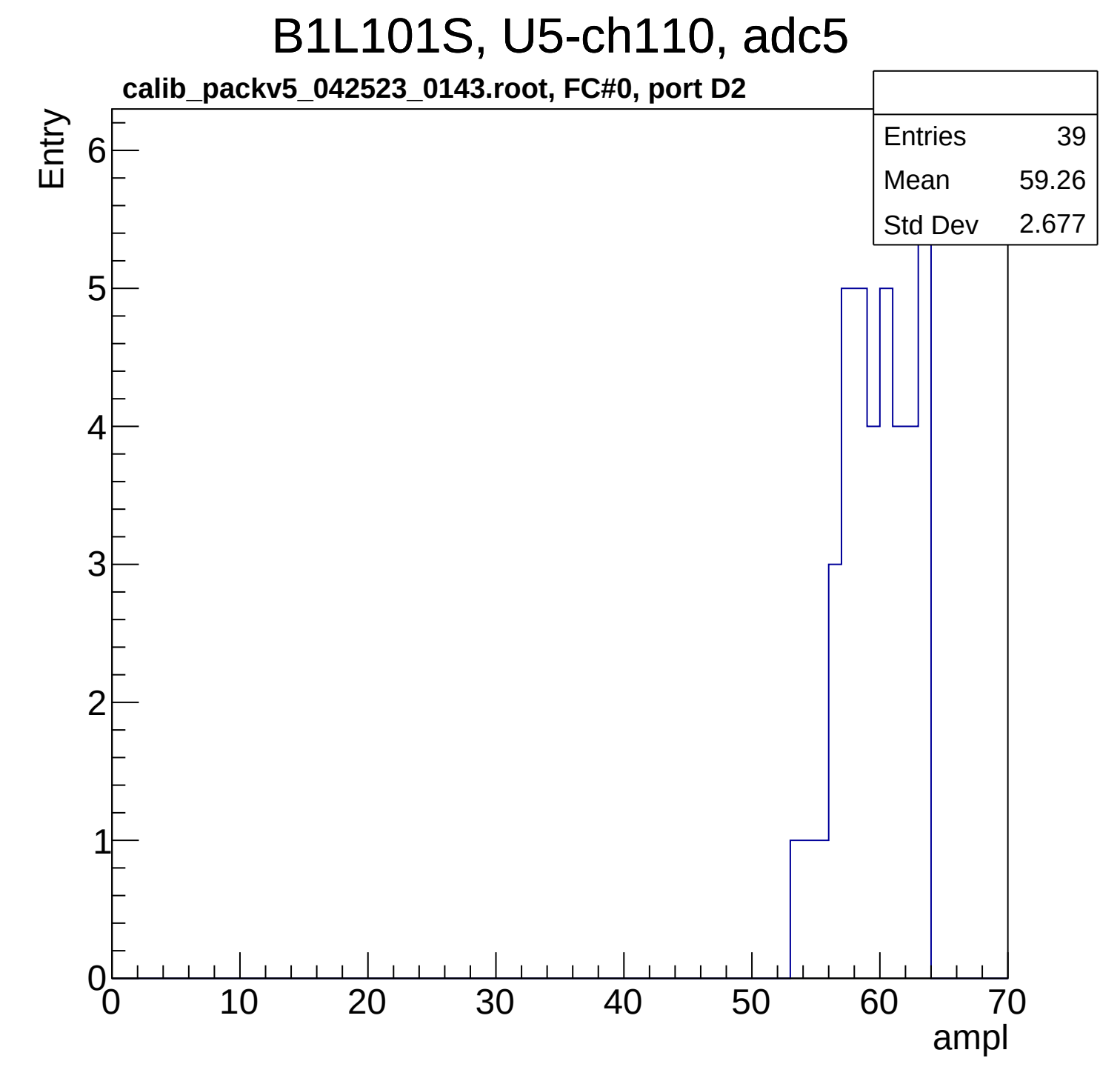
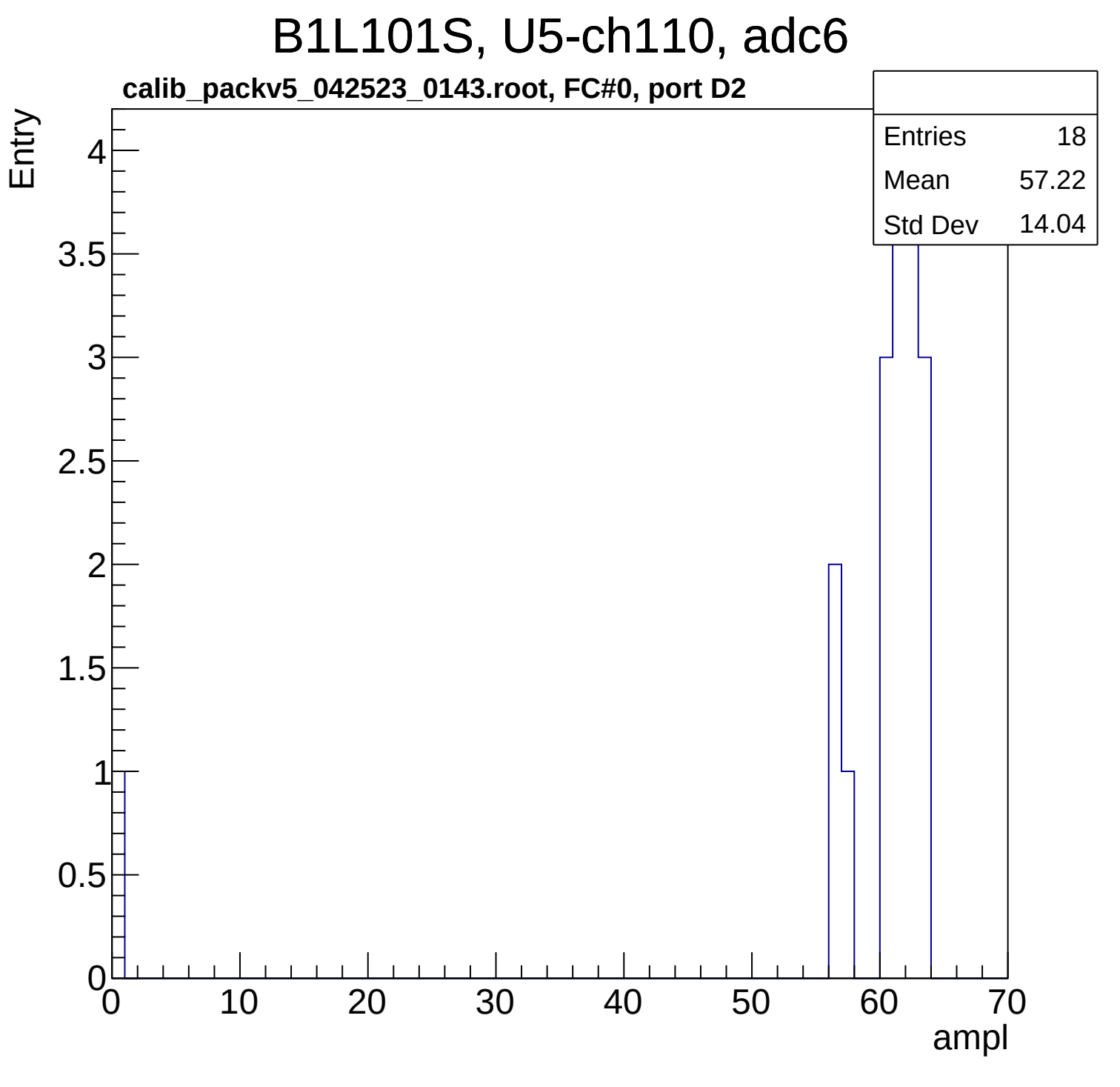
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch110, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 55.59
Std Dev 3.959
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L101S, U5-ch110, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 39
Mean 59.26
Std Dev 2.677
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L101S, U5-ch110, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 18
Mean 57.22
Std Dev 14.04
Entry
ampl
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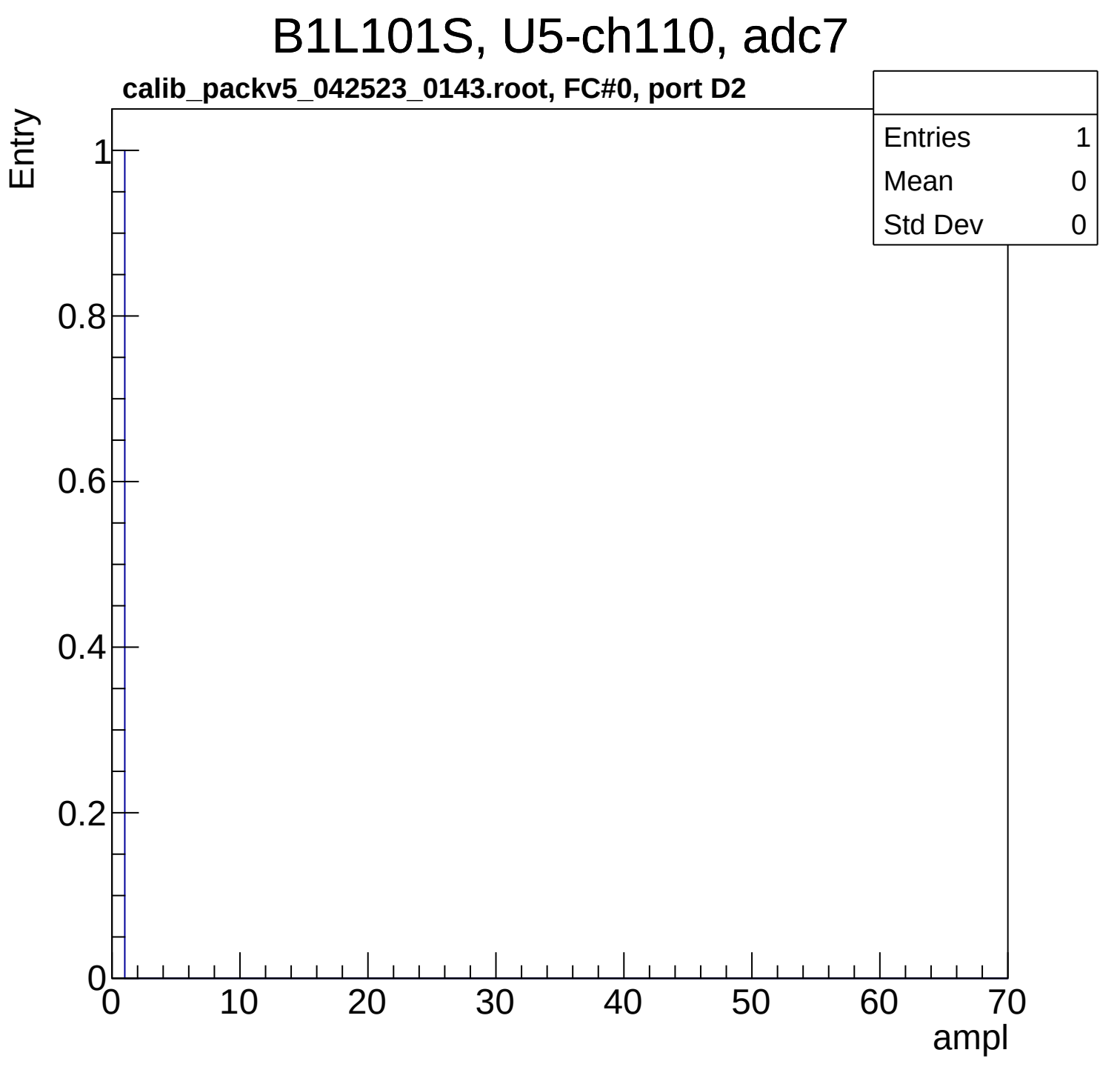
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L101S, U5-ch110, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
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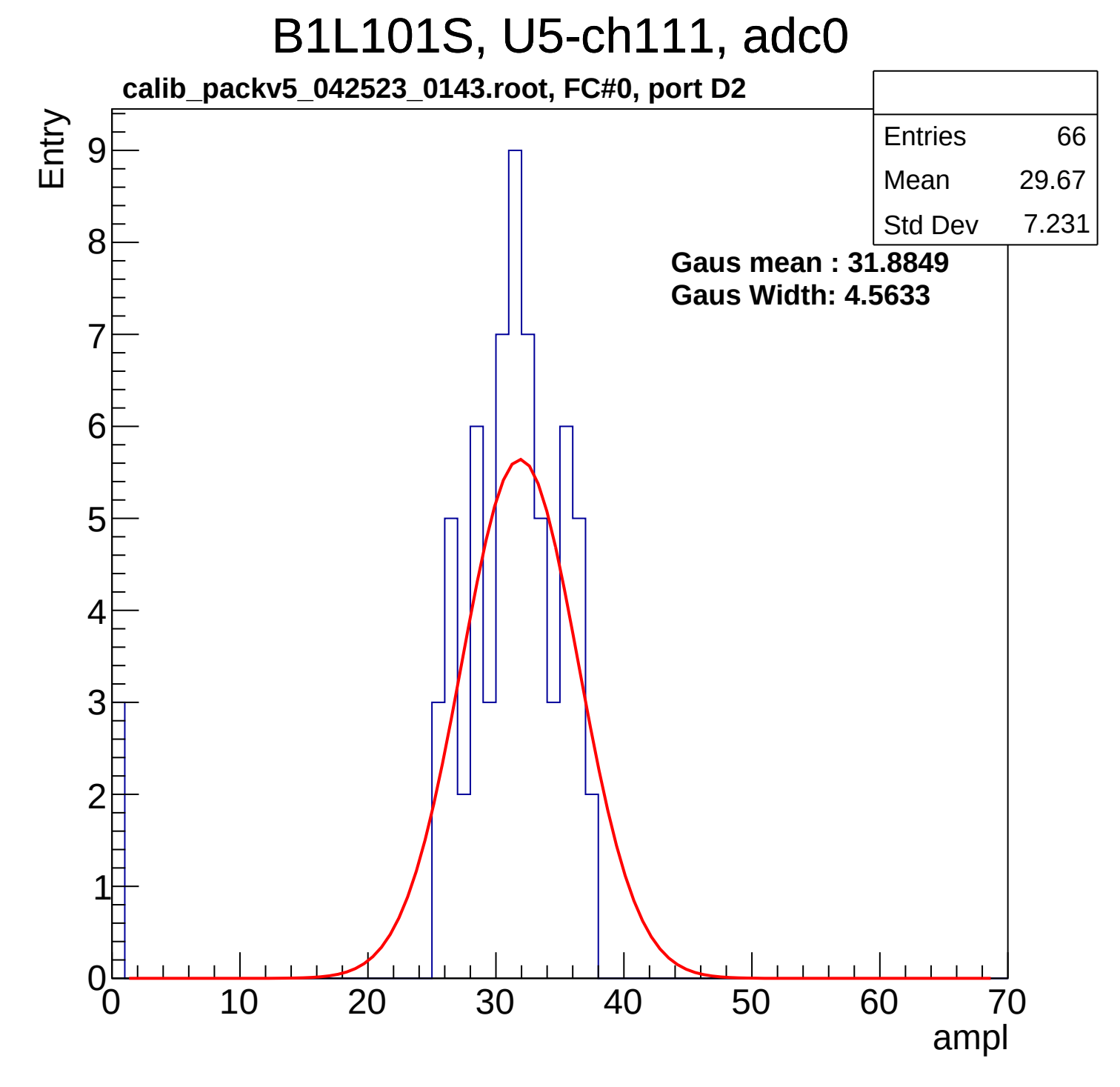
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch111, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 29.67
Std Dev 7.231
Gaus mean : 31.8849
Gaus Width: 4.5633
Entry
ampl
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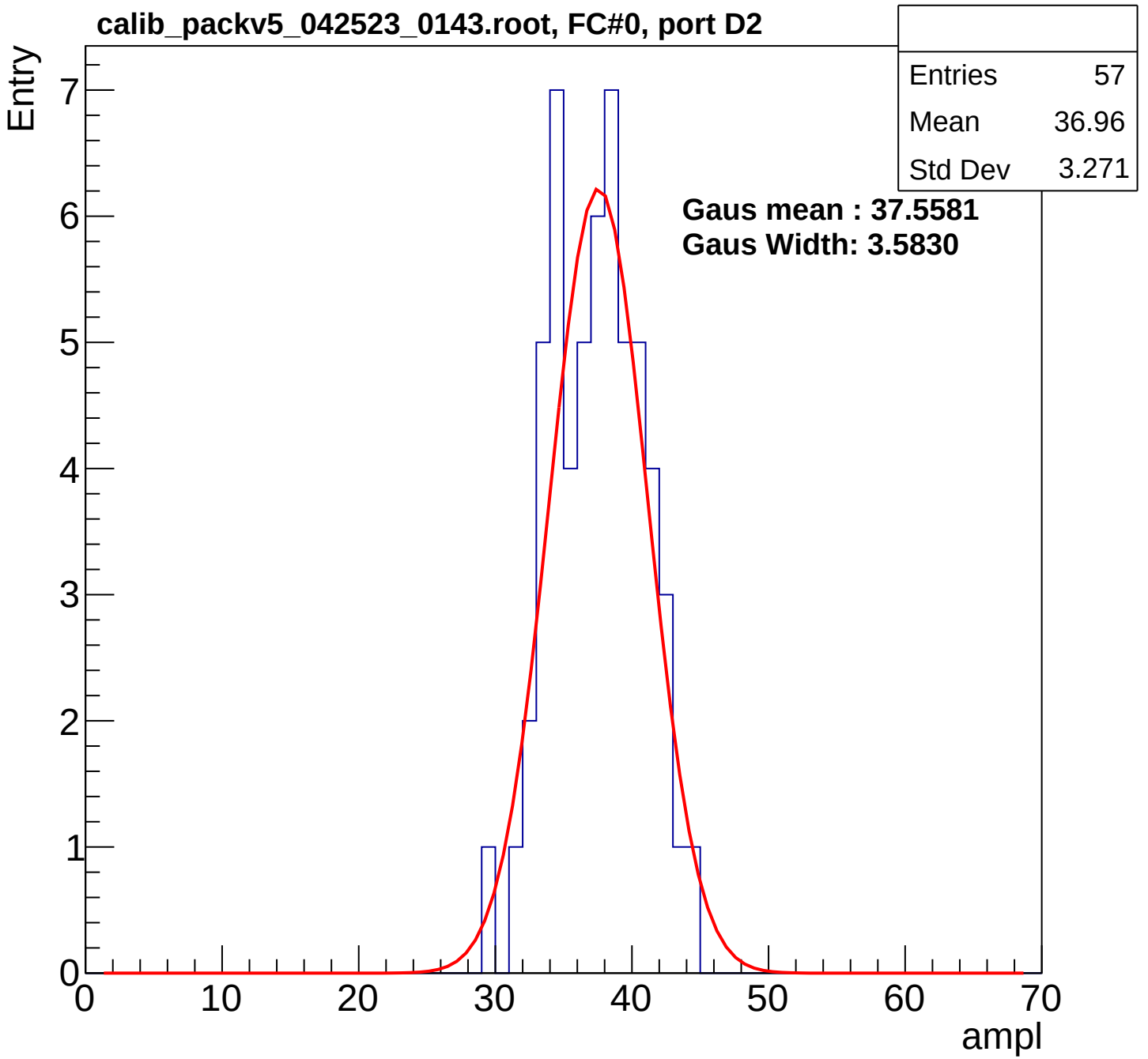
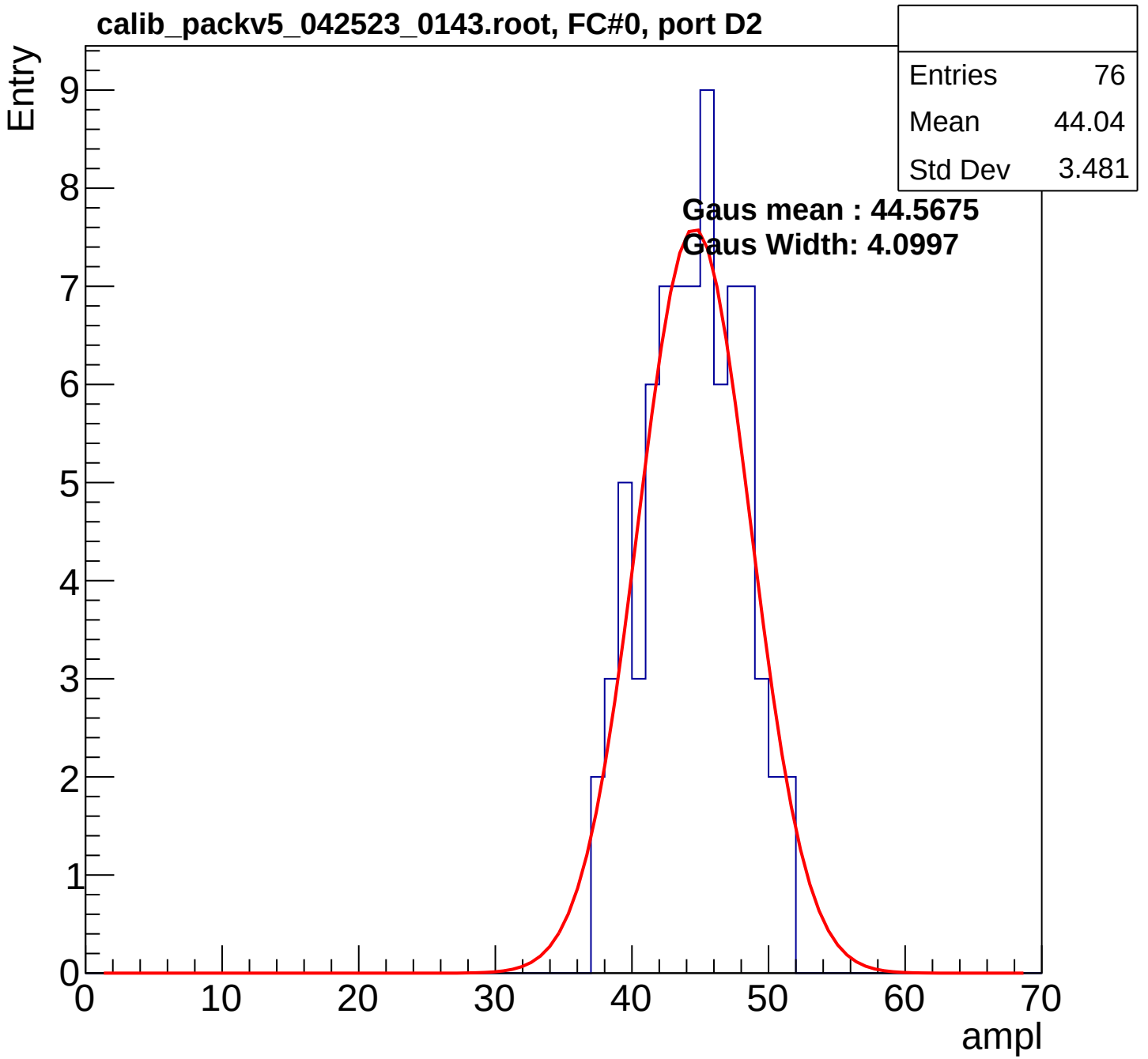
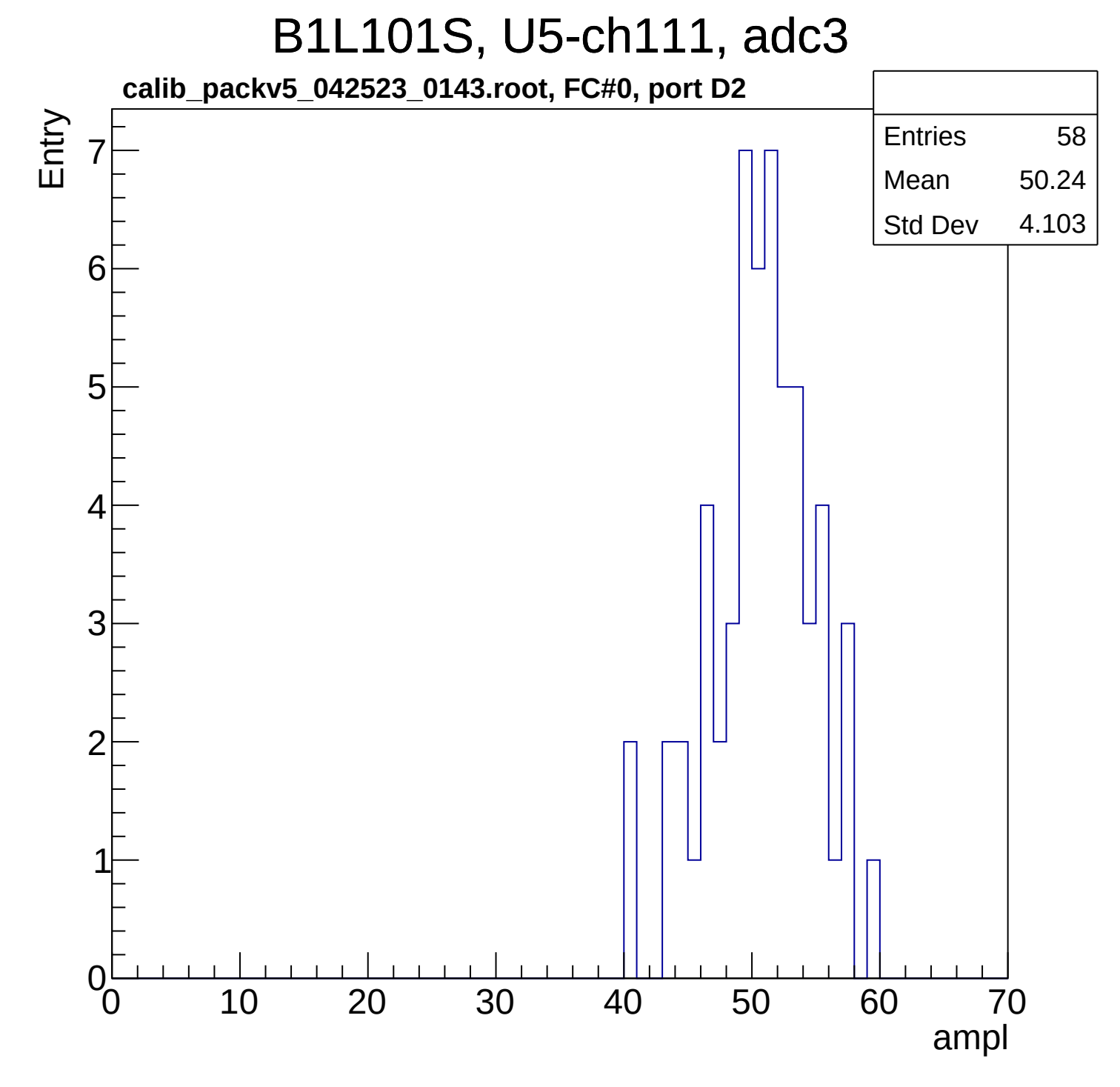
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch111, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 36.96
Std Dev 3.271
Gaus mean : 37.5581
Gaus Width: 3.5830
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch111, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 44.04
Std Dev 3.481
Gaus mean : 44.5675
Gaus Width: 4.0997
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch111, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 50.24
Std Dev 4.103
Entry
ampl
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2
3
4
5
6
7
0
10
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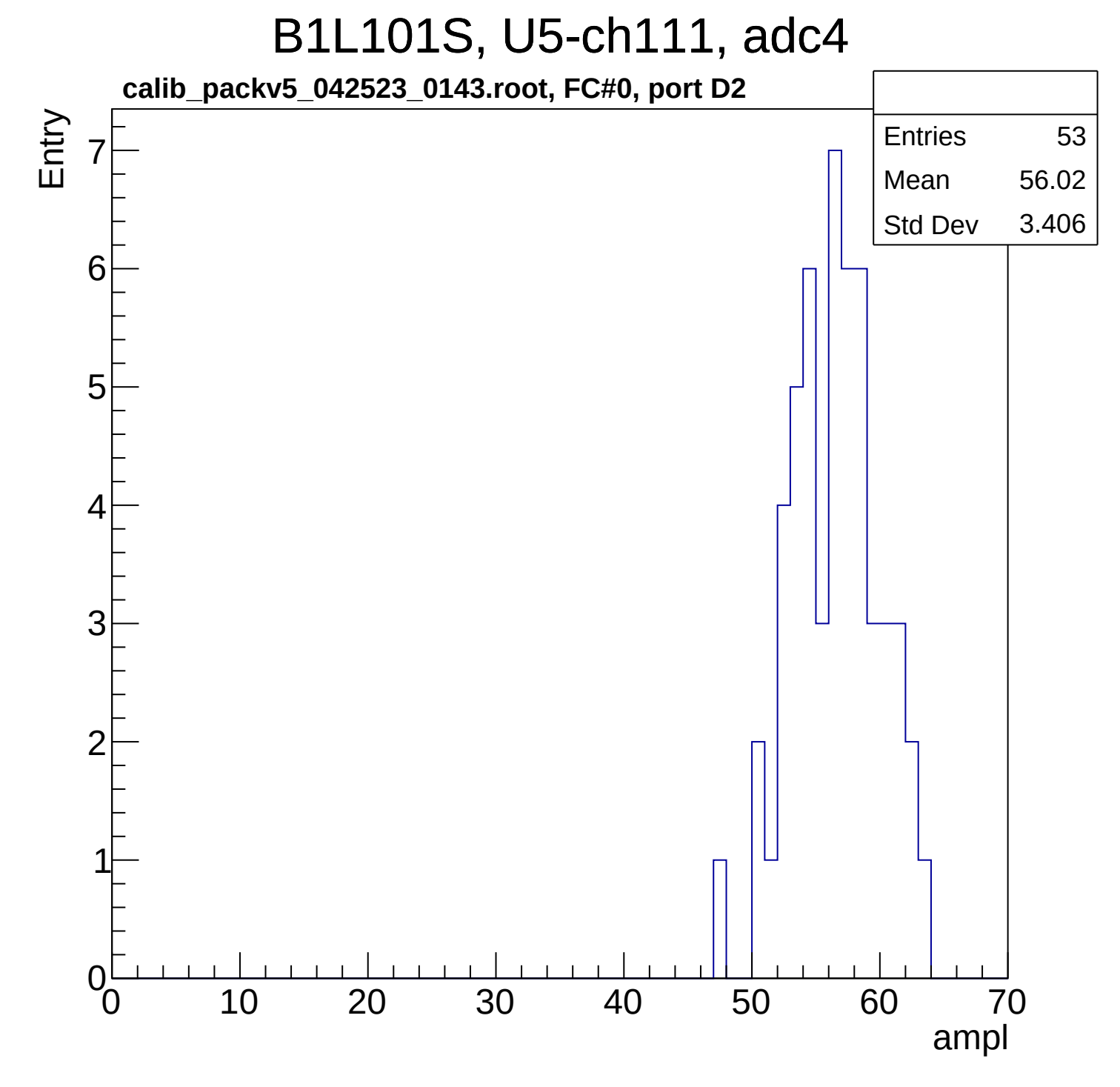
40
50
60
70


B1L101S, U5-ch111, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 56.02
Std Dev 3.406
Entry
ampl
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2
3
4
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0
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40
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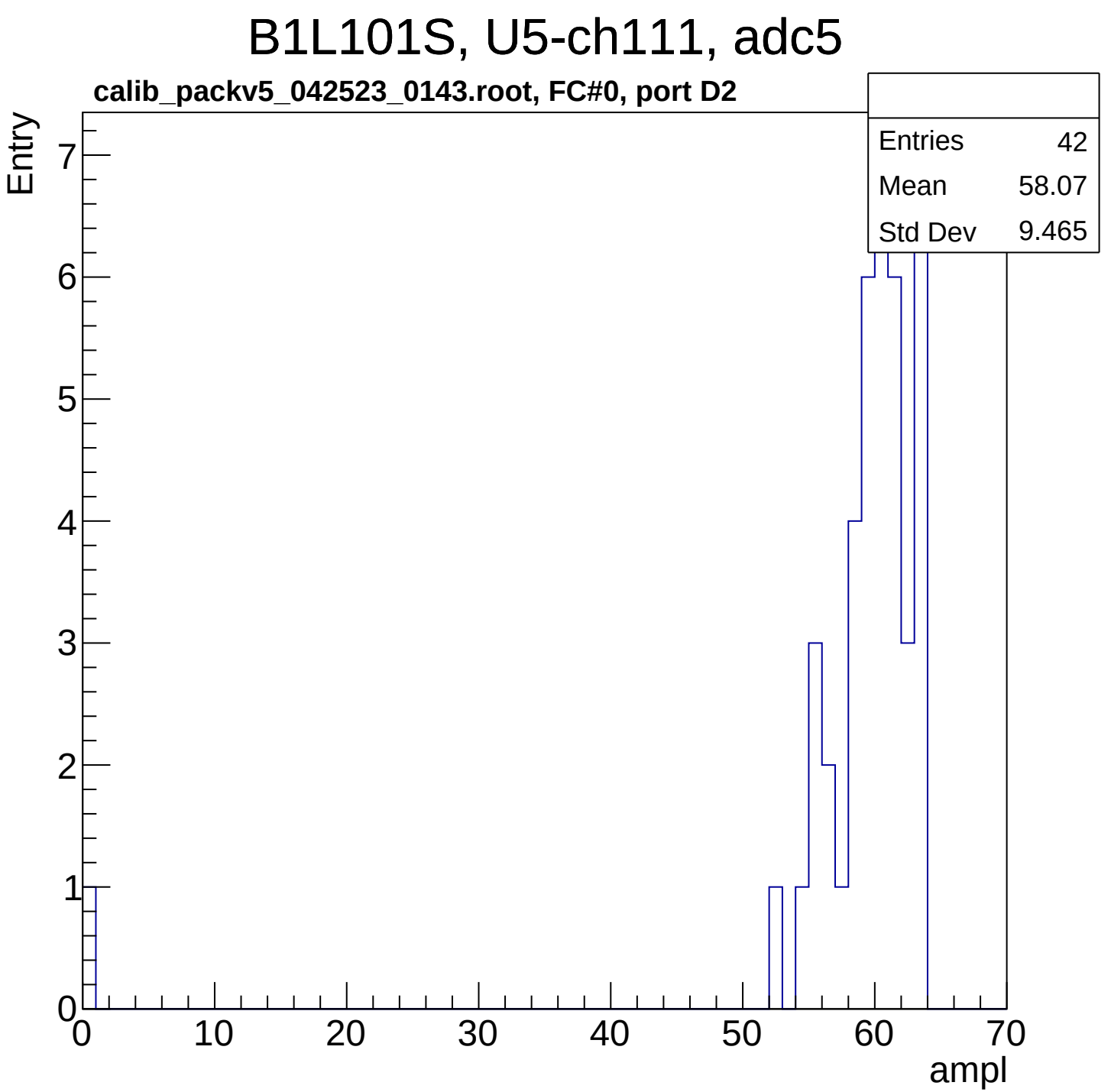
60
70


B1L101S, U5-ch111, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 58.07
Std Dev 9.465
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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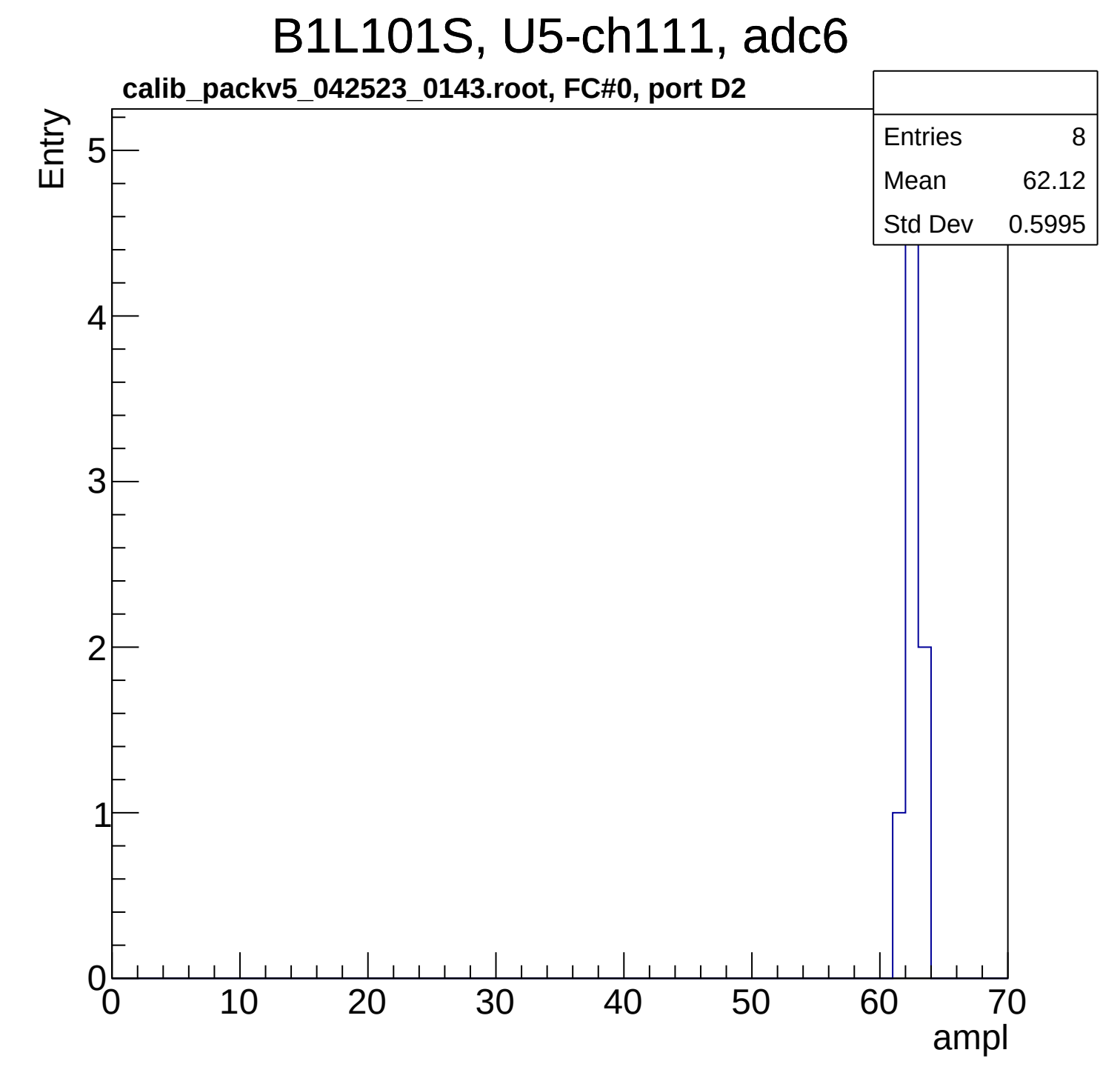
B1L101S, U5-ch111, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 62.12
Std Dev 0.5995
Entry
ampl
0
1
2
3
4
5
0
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20
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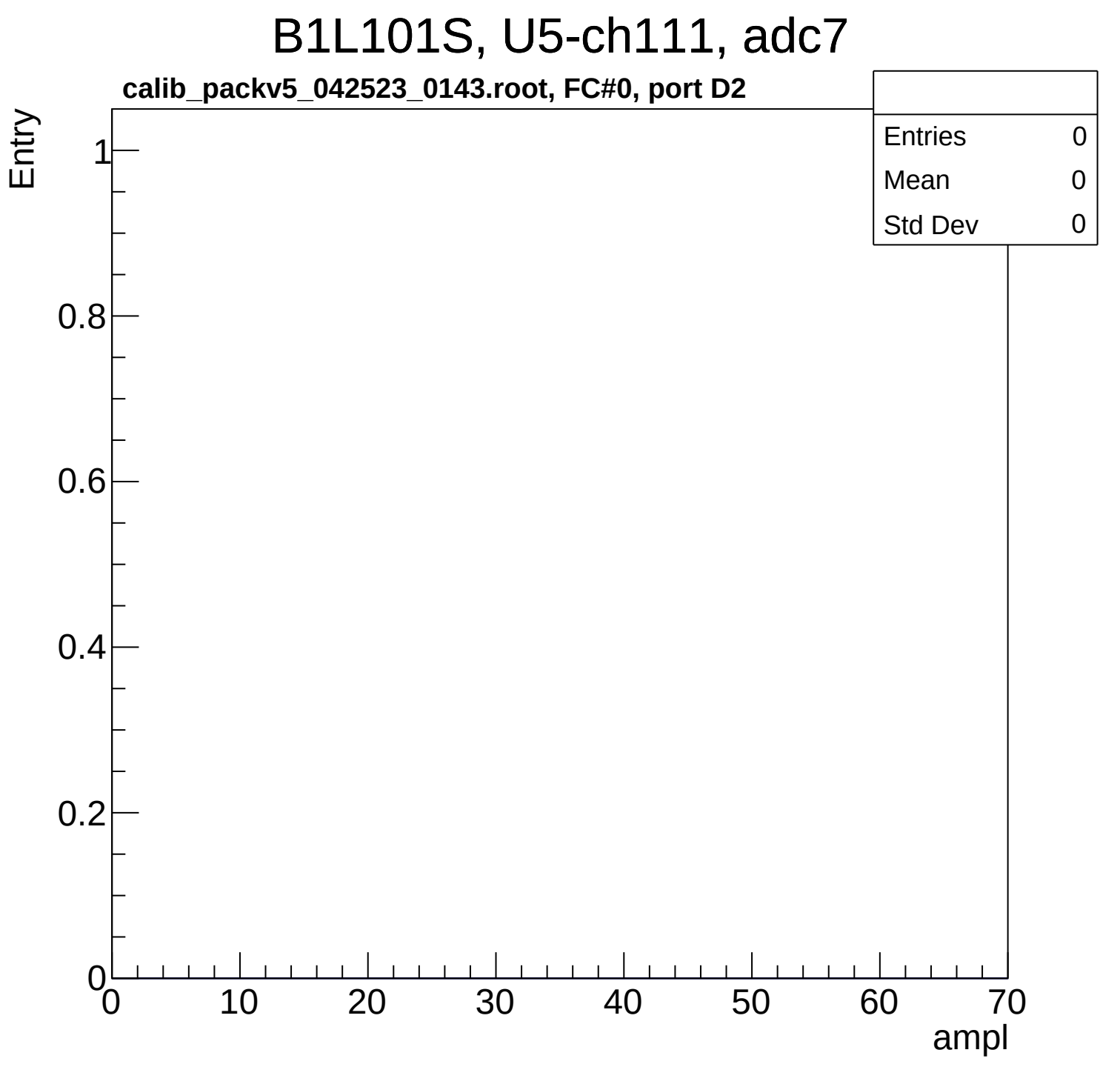
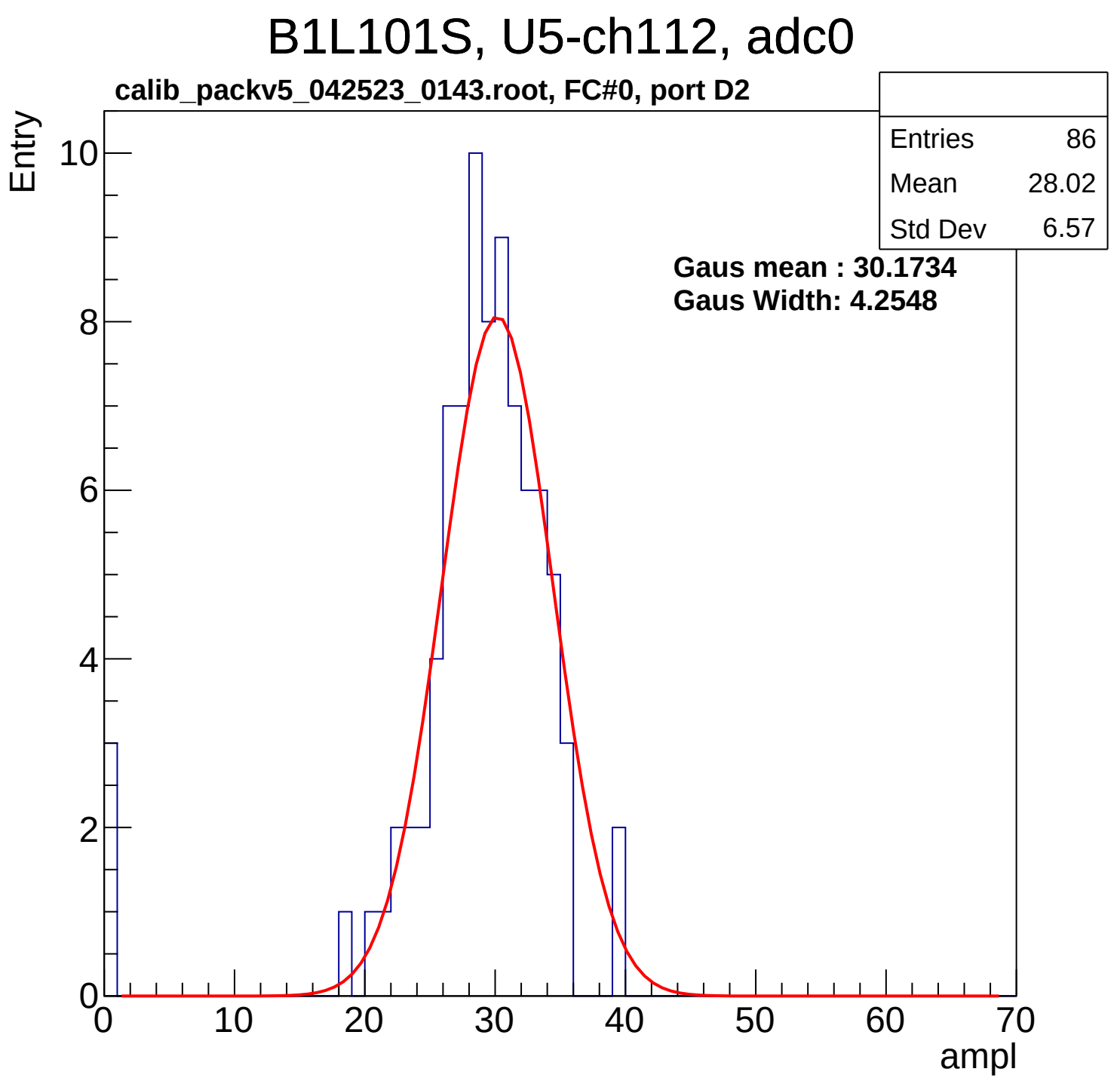
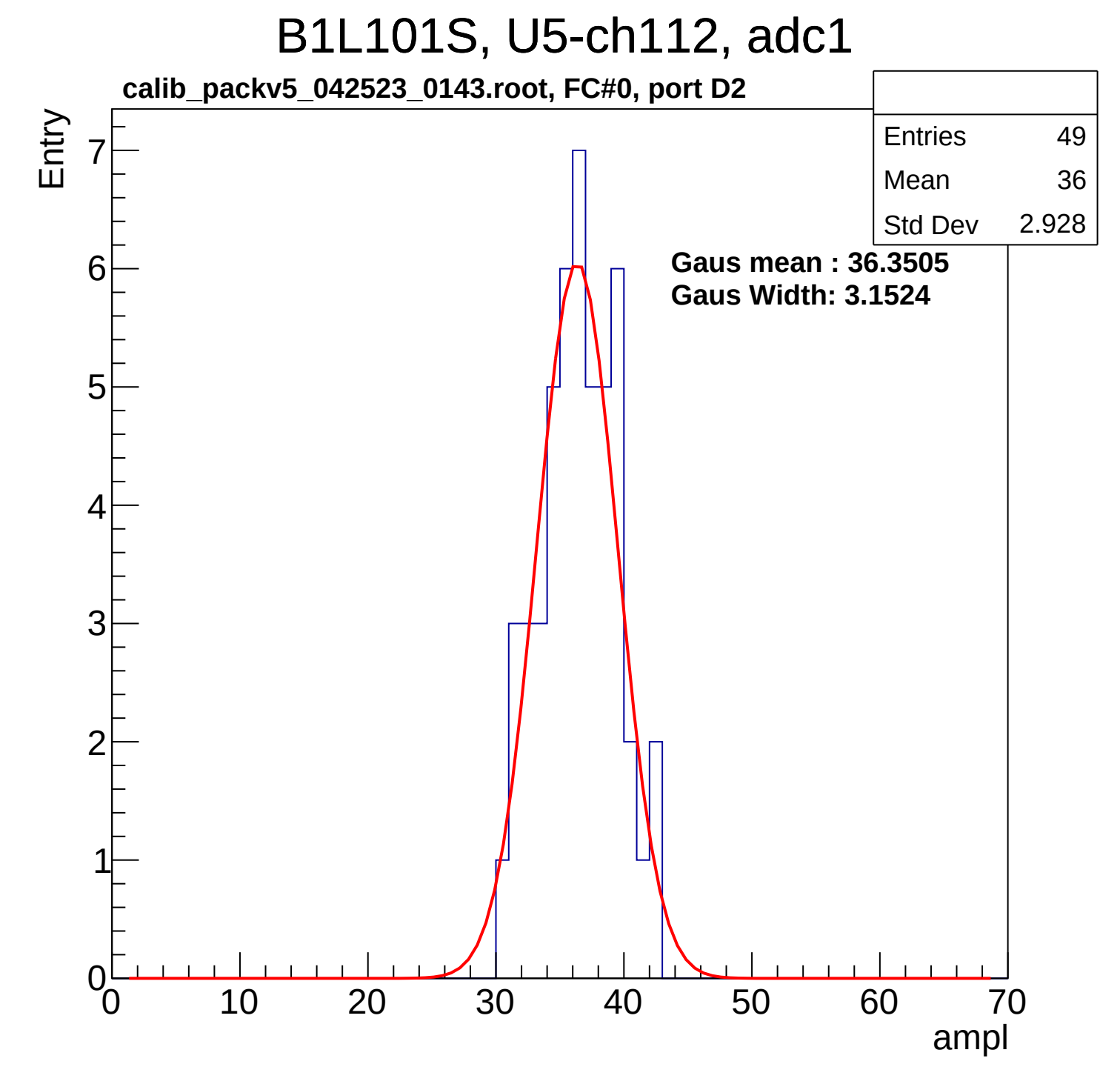
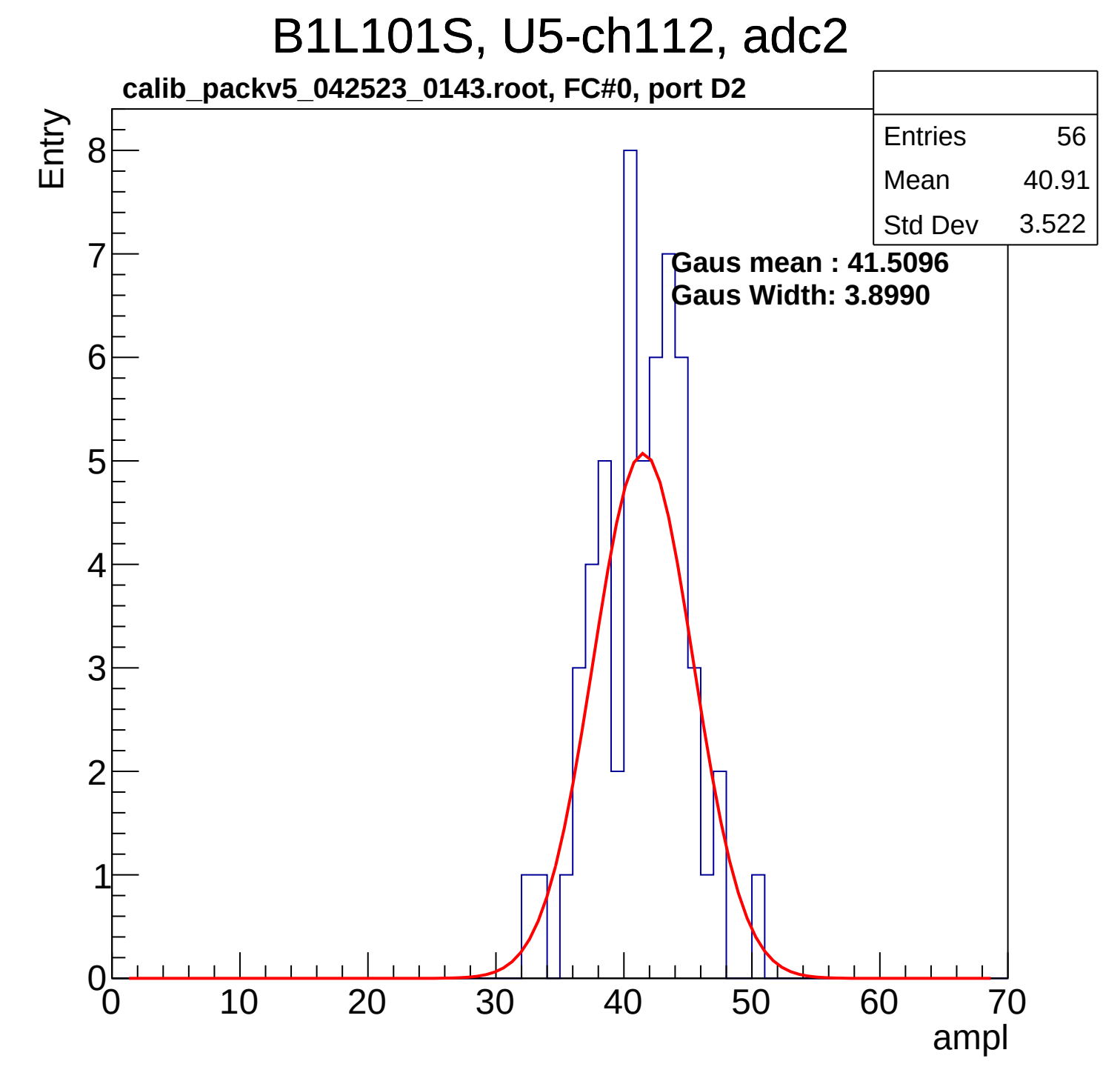
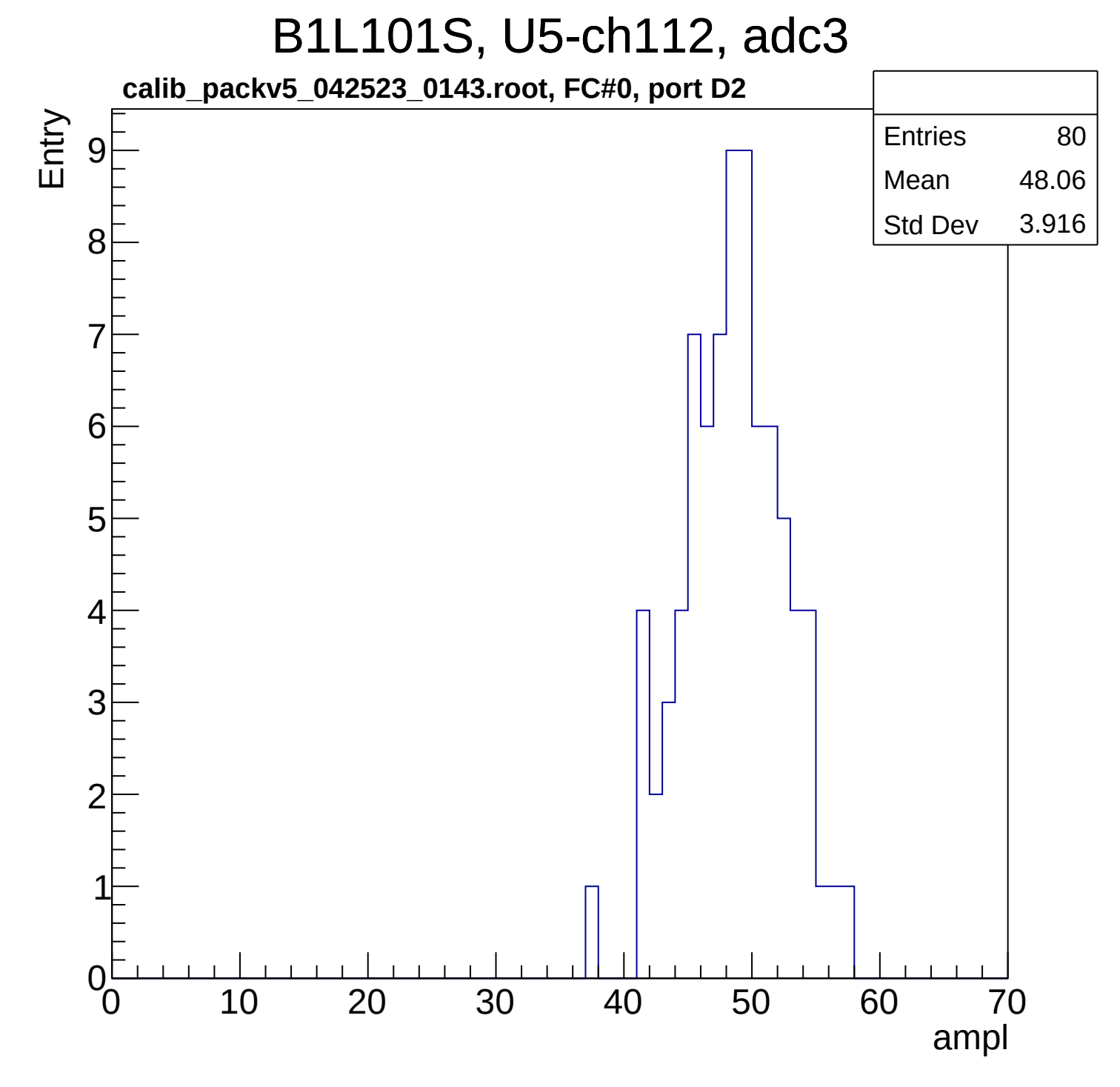
40
50
60
70

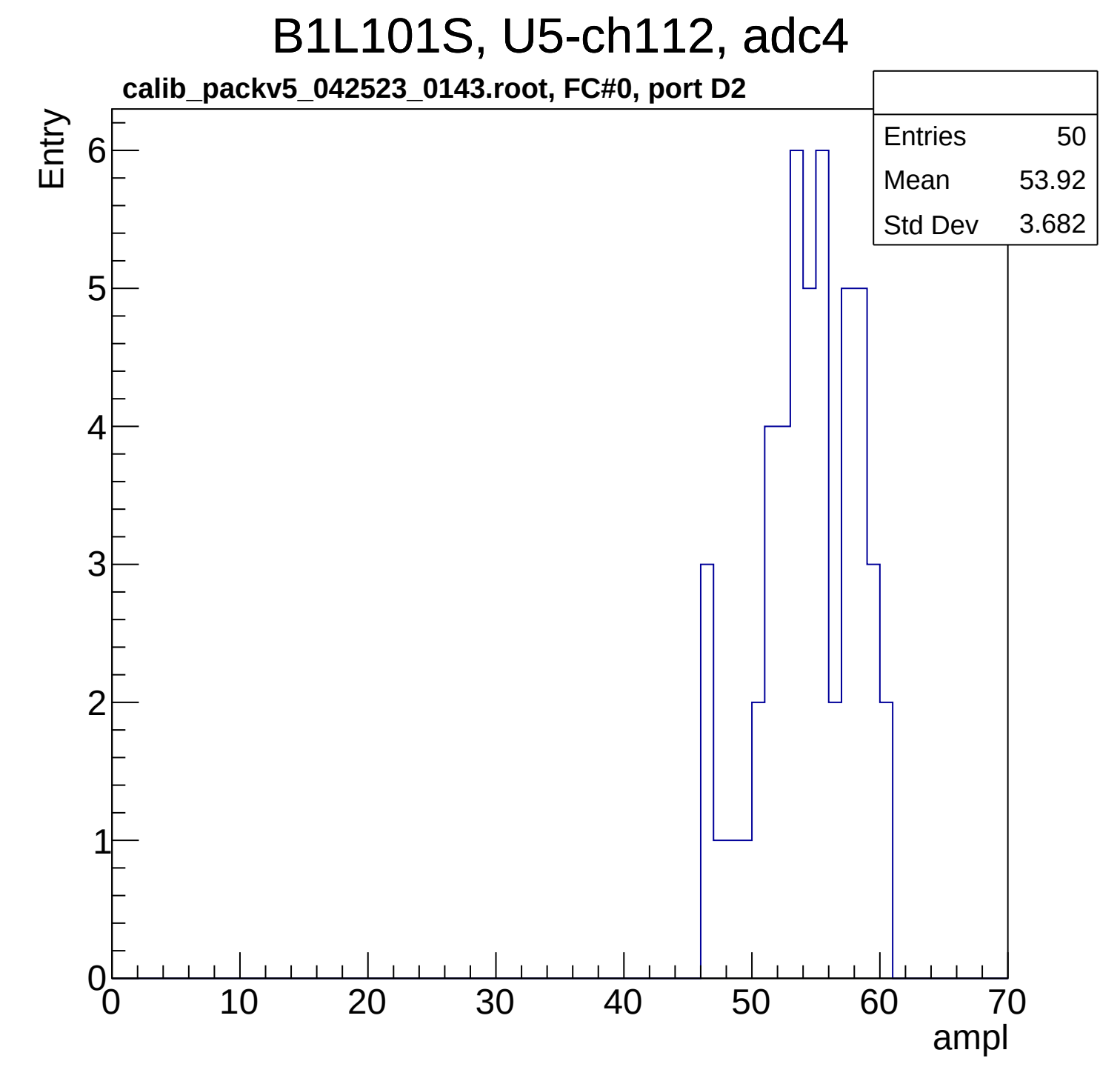

B1L101S, U5-ch111, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

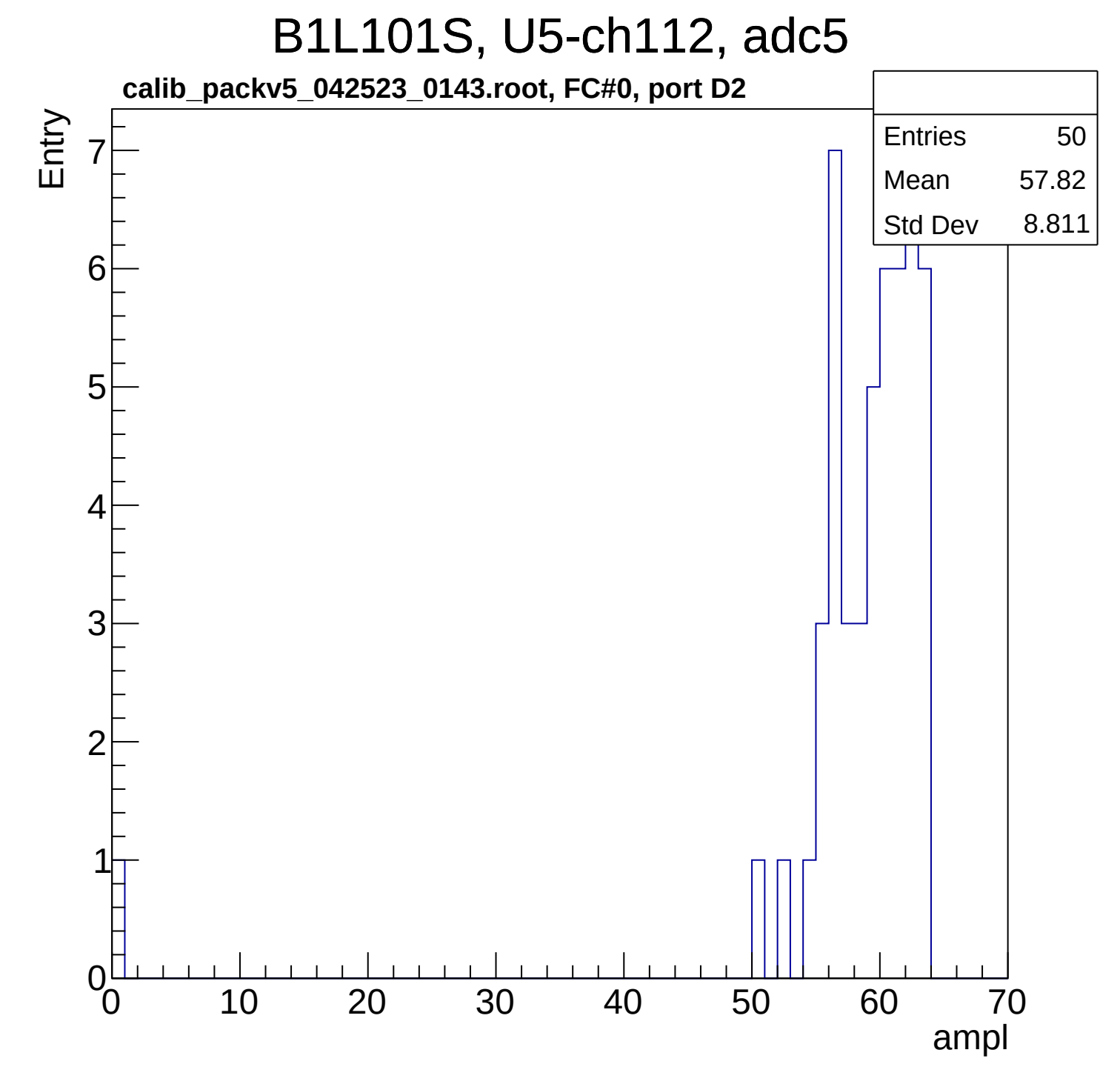

B1L101S, U5-ch112, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 86
Mean 28.02
Std Dev 6.57
Gaus mean : 30.1734
Gaus Width: 4.2548
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch112, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 36
Std Dev 2.928
Gaus mean : 36.3505
Gaus Width: 3.1524
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch112, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 40.91
Std Dev 3.522
Gaus mean : 41.5096
Gaus Width: 3.8990
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch112, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 80
Mean 48.06
Std Dev 3.916
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch112, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 53.92
Std Dev 3.682
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L101S, U5-ch112, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 57.82
Std Dev 8.811
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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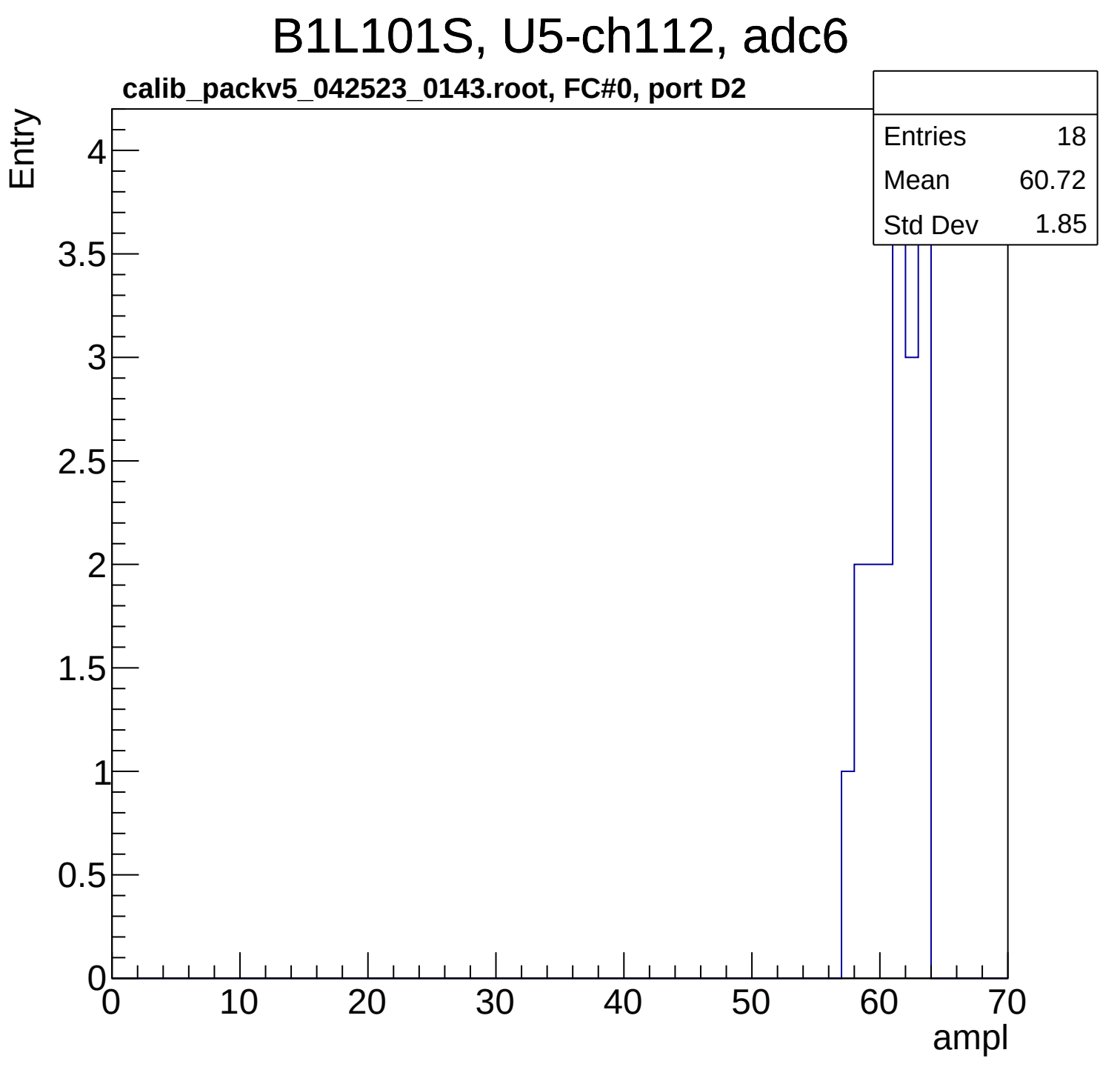
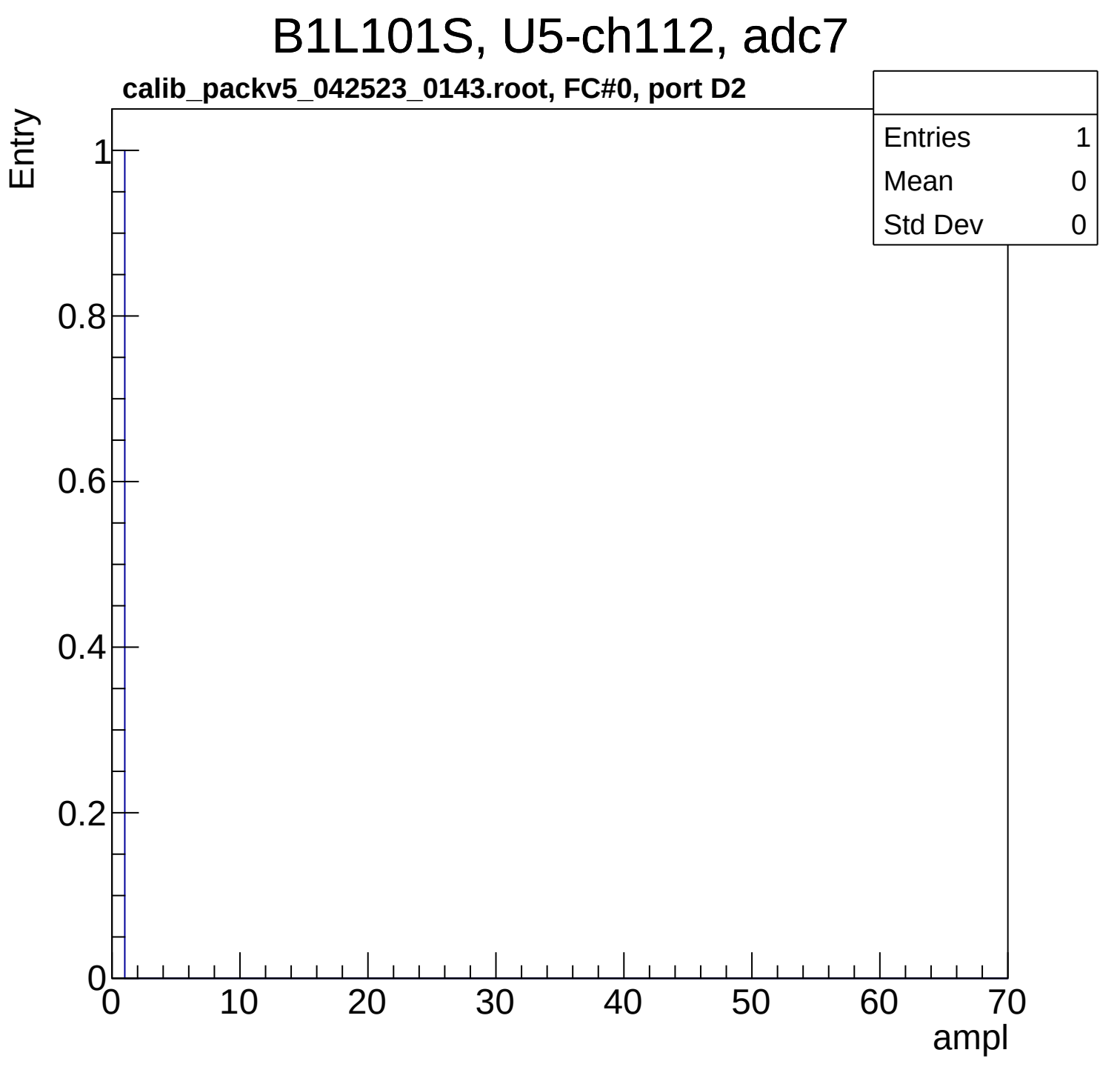
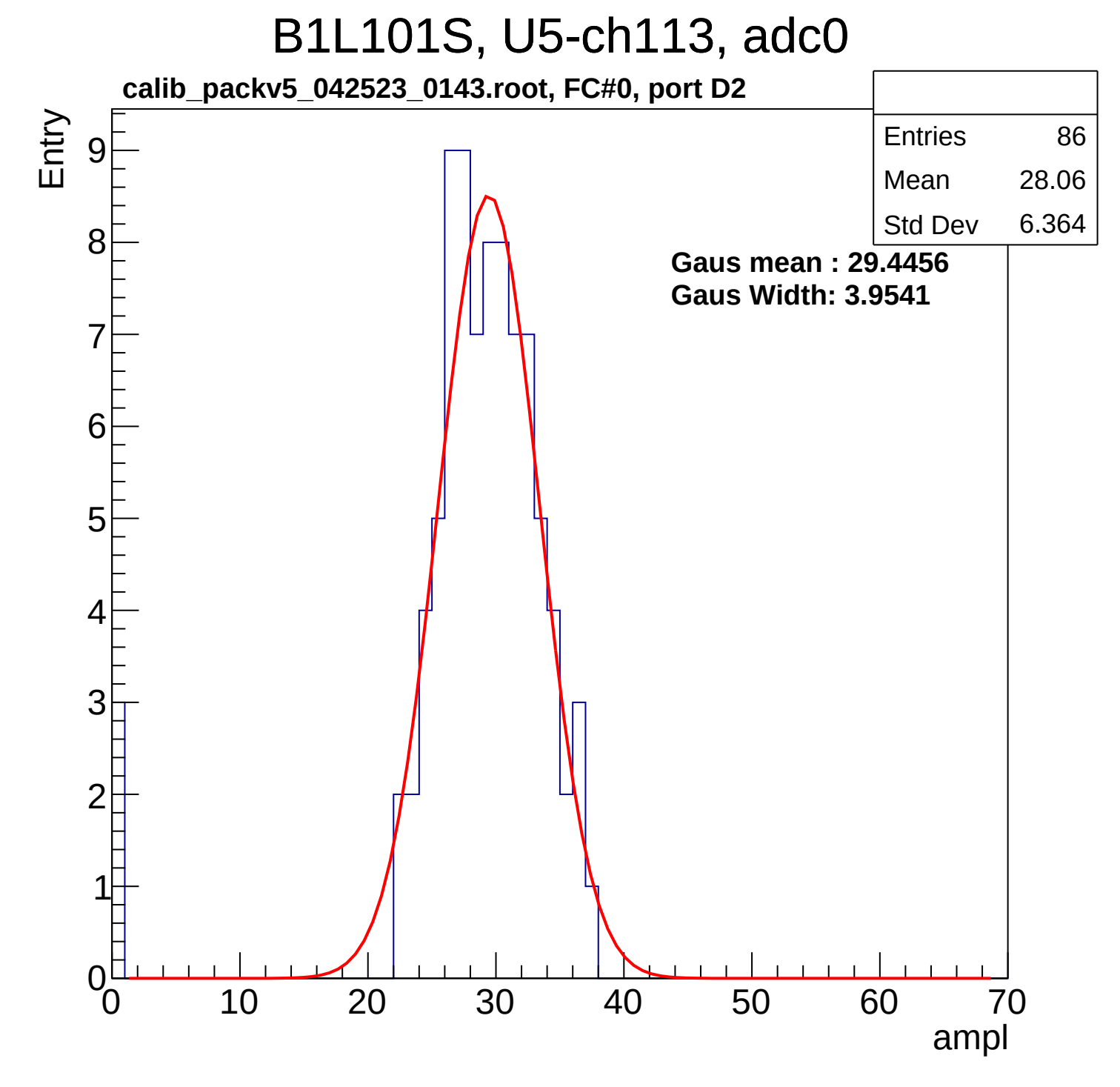
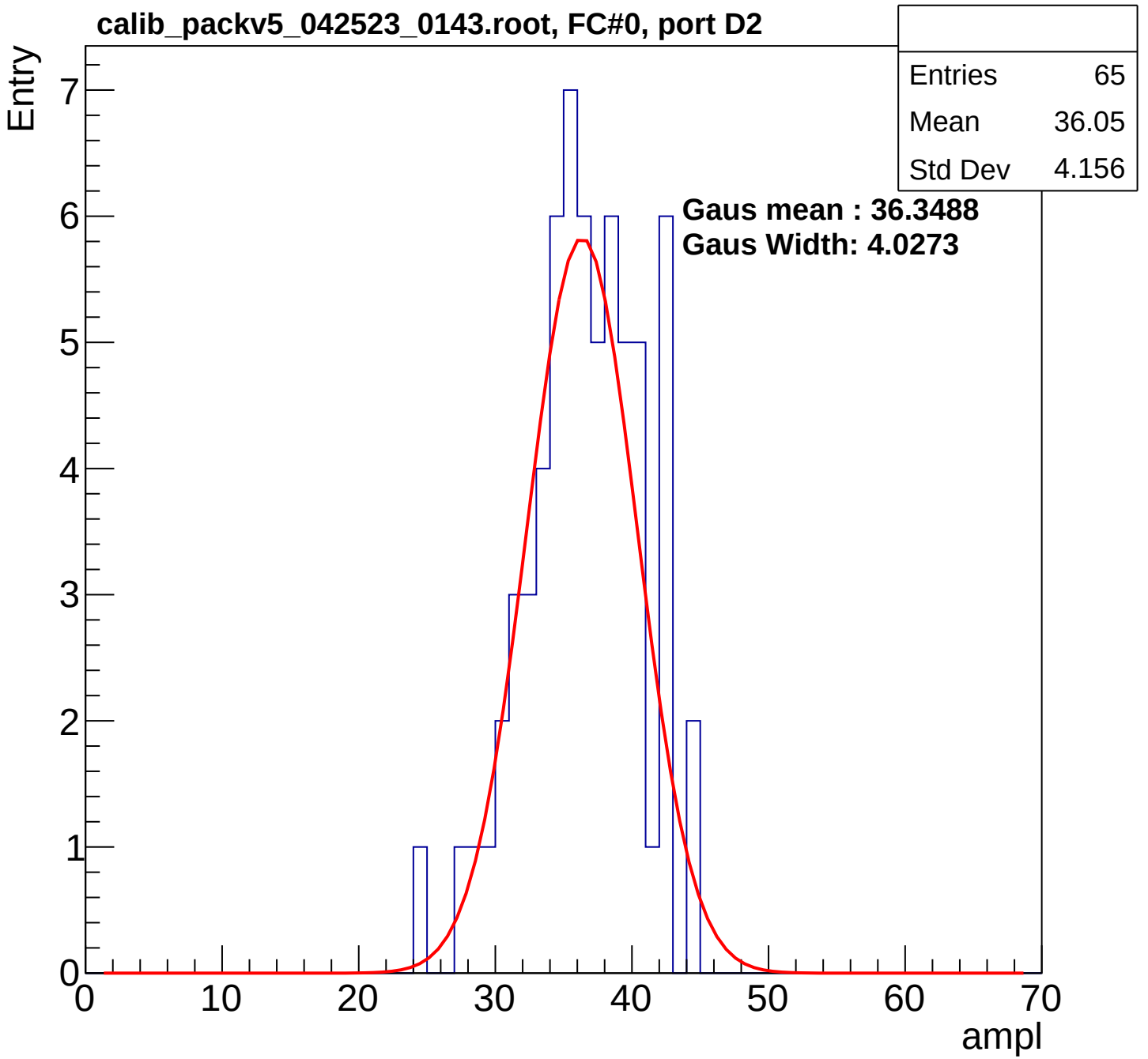

B1L101S, U5-ch112, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 18
Mean 60.72
Std Dev 1.85
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L101S, U5-ch112, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch113, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 86
Mean 28.06
Std Dev 6.364
Gaus mean : 29.4456
Gaus Width: 3.9541
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch113, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 36.05
Std Dev 4.156
Gaus mean : 36.3488
Gaus Width: 4.0273
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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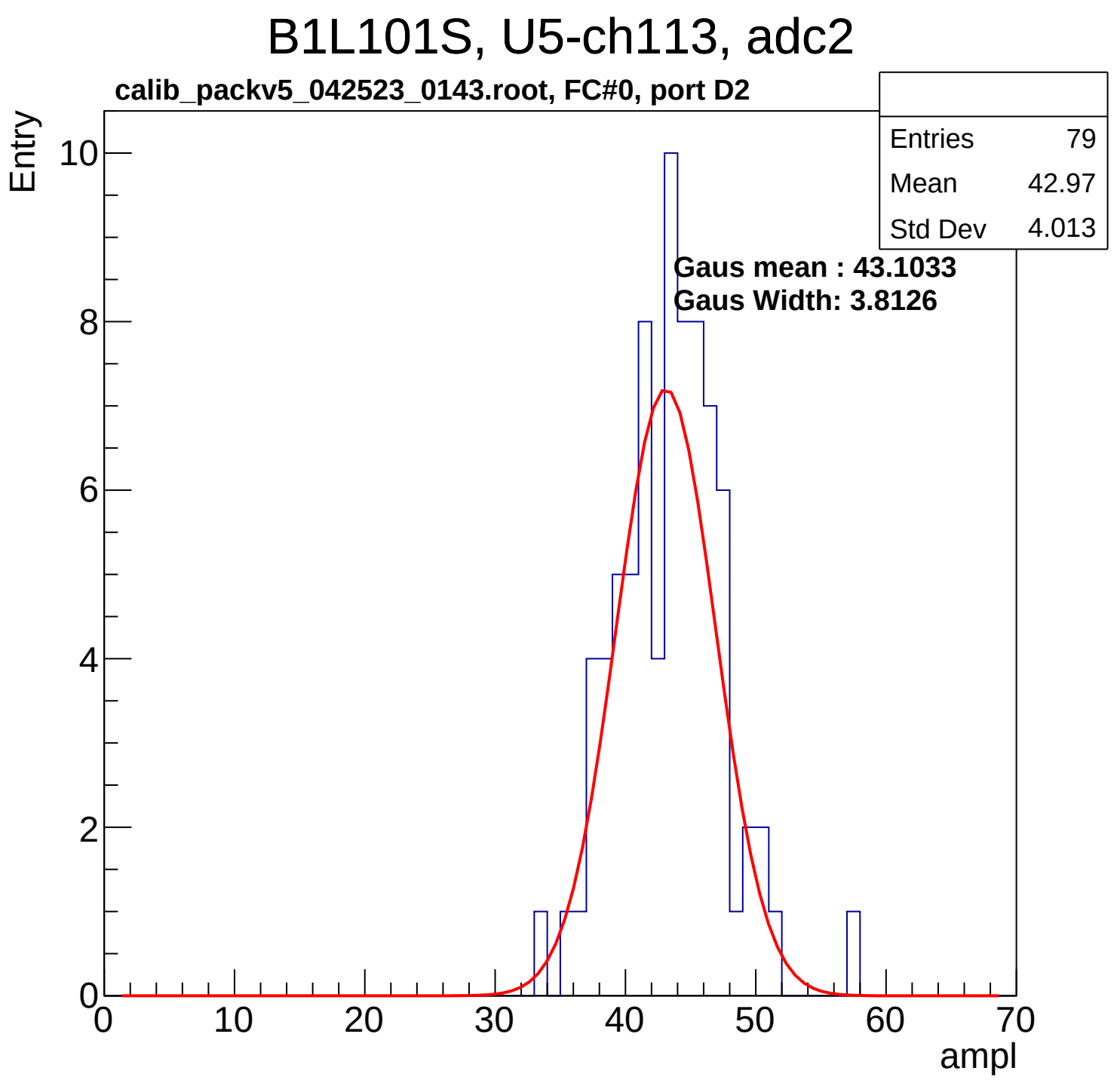
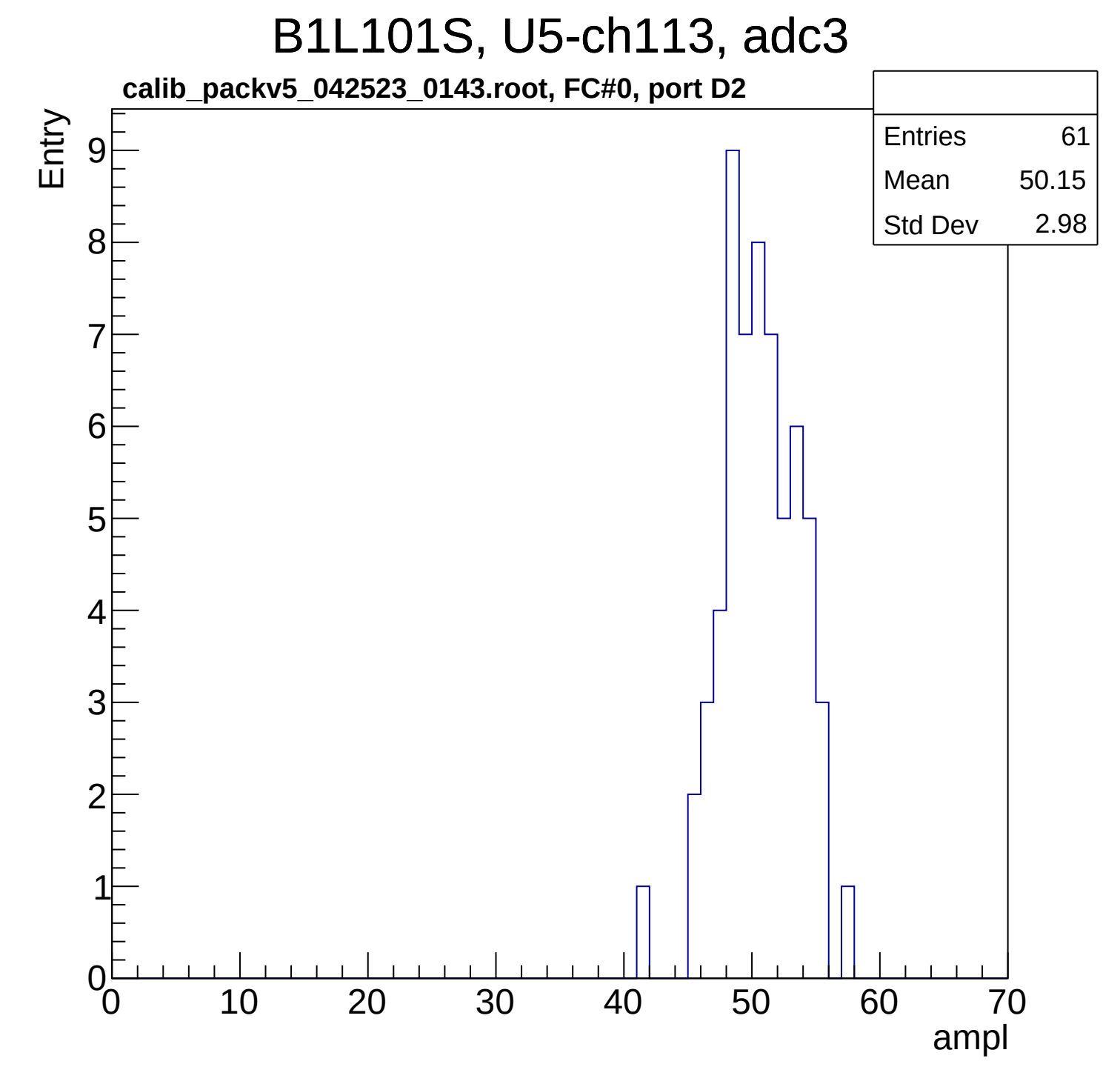

B1L101S, U5-ch113, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 42.97
Std Dev 4.013
Gaus mean : 43.1033
Gaus Width: 3.8126
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch113, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 50.15
Std Dev 2.98
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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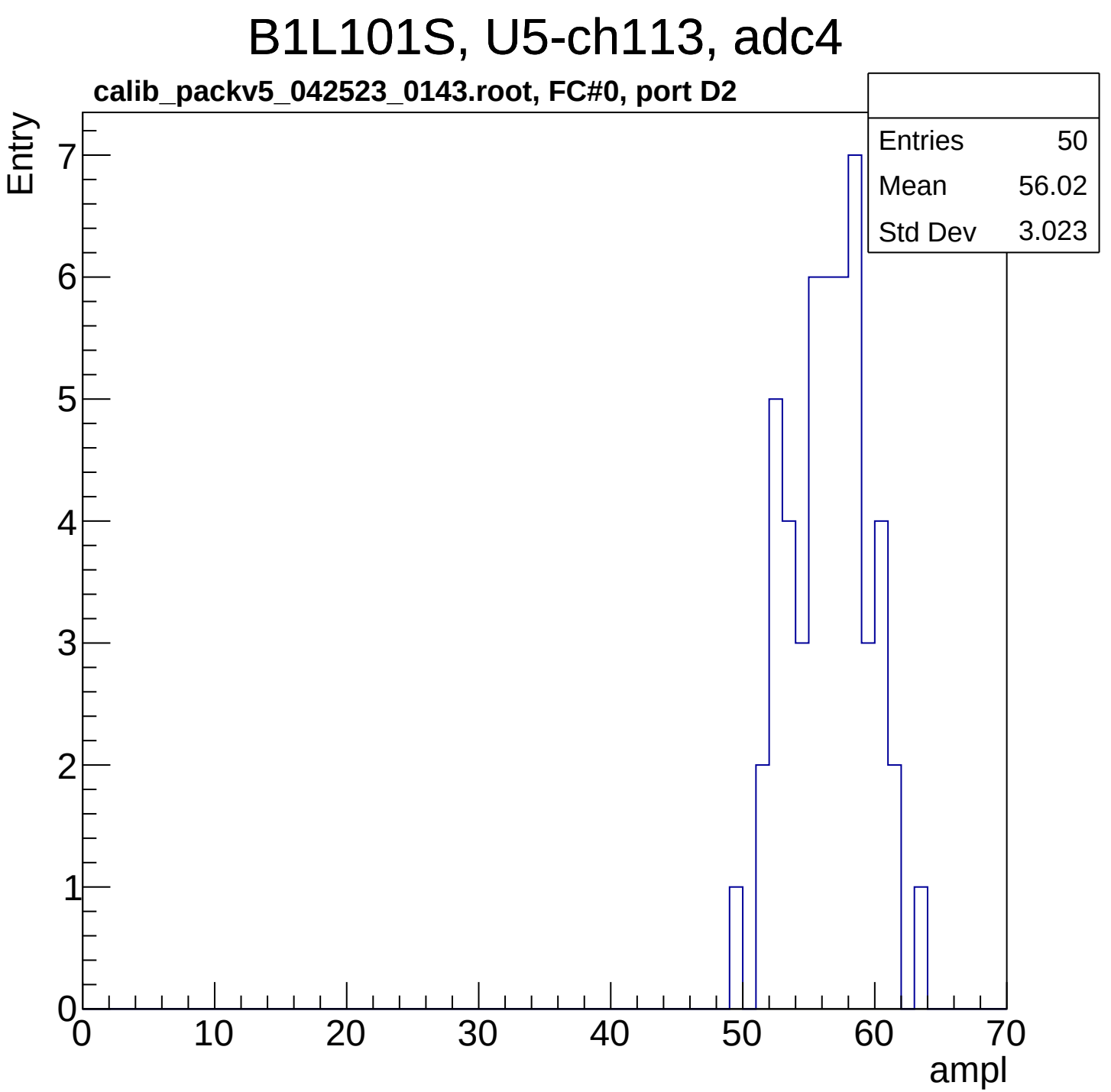
B1L101S, U5-ch113, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 56.02
Std Dev 3.023
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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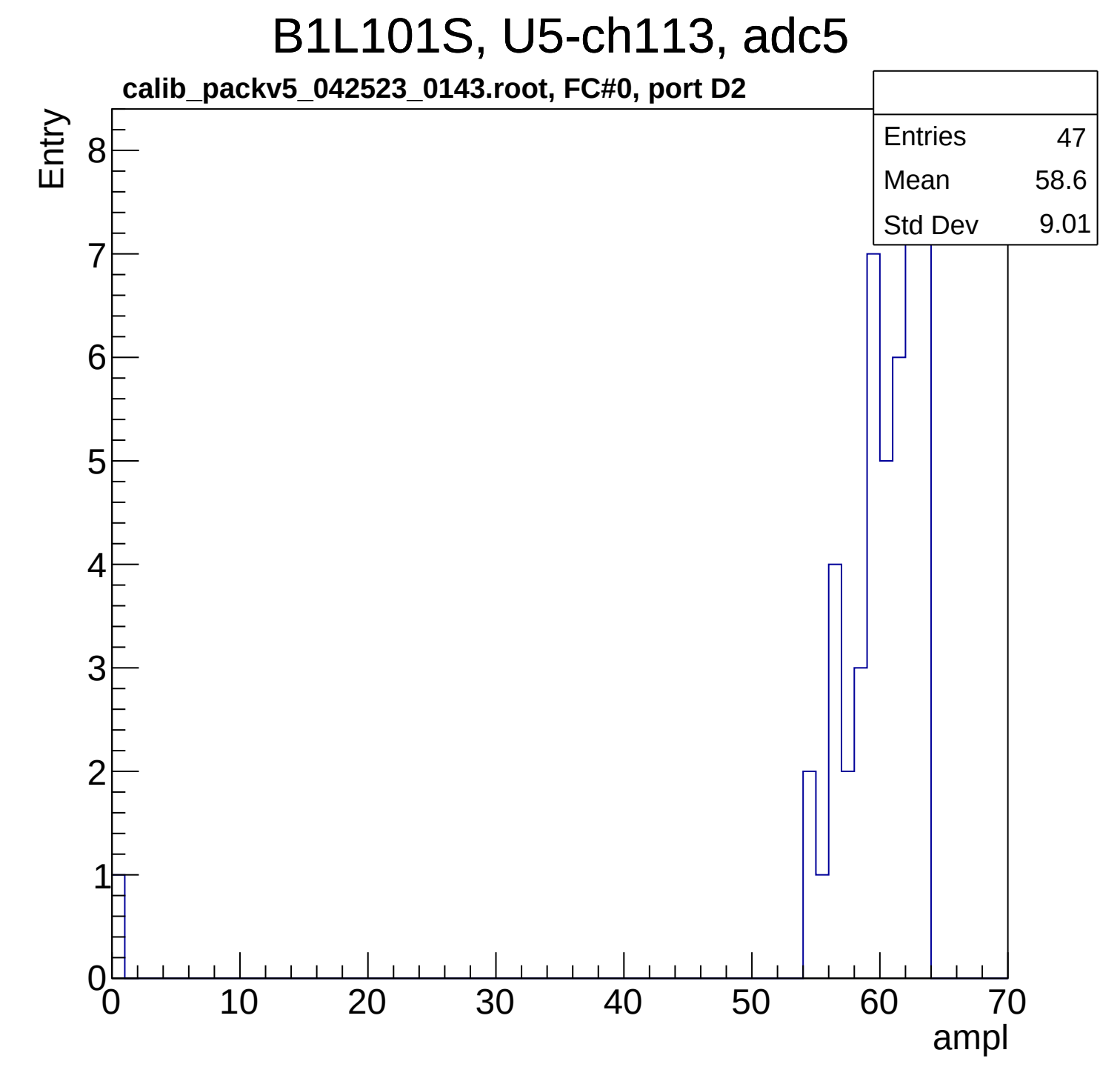
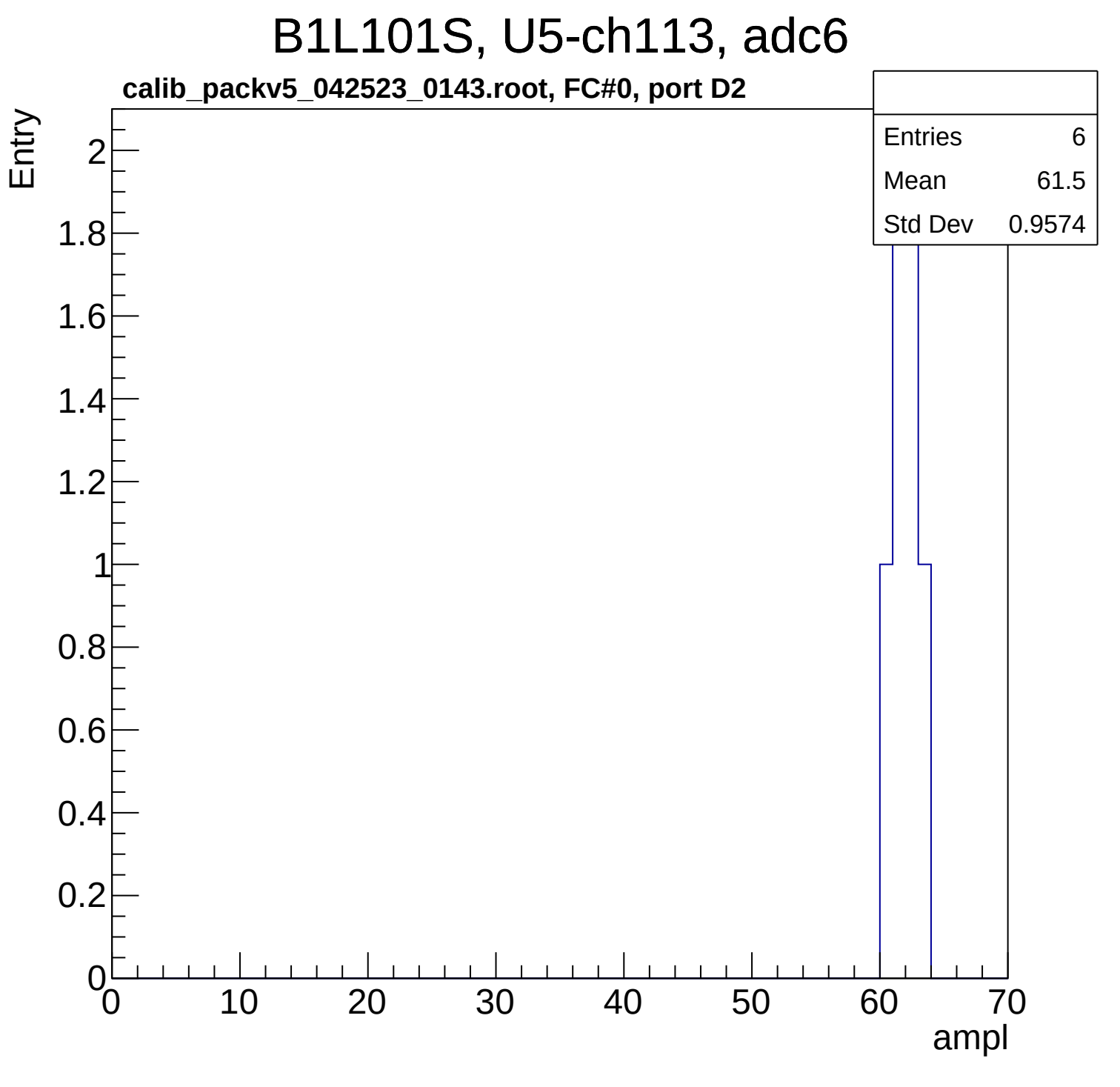
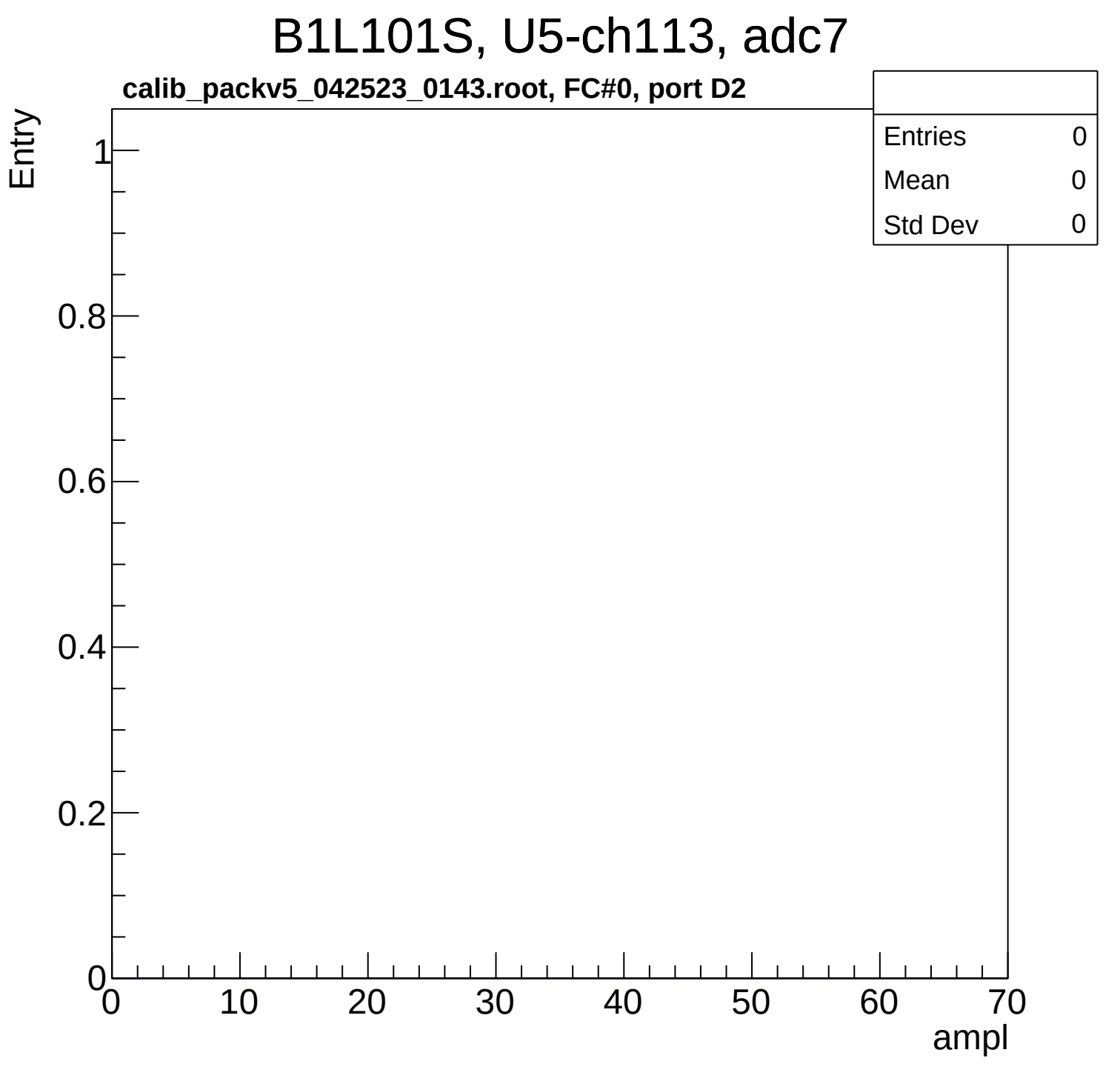
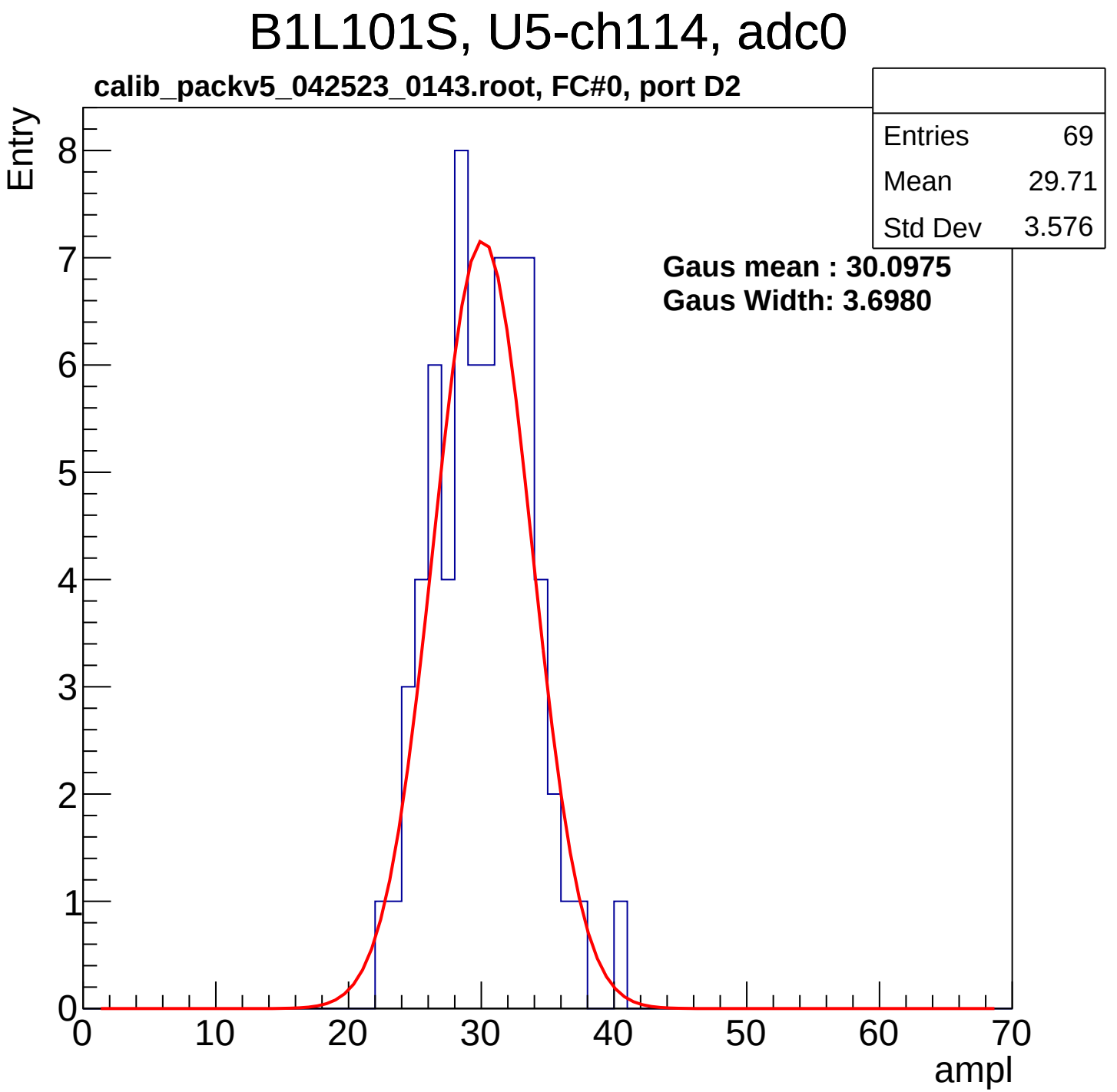

B1L101S, U5-ch113, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 58.6
Std Dev 9.01
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch113, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 61.5
Std Dev 0.9574
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L101S, U5-ch113, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch114, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 29.71
Std Dev 3.576
Gaus mean : 30.0975
Gaus Width: 3.6980
Entry
ampl
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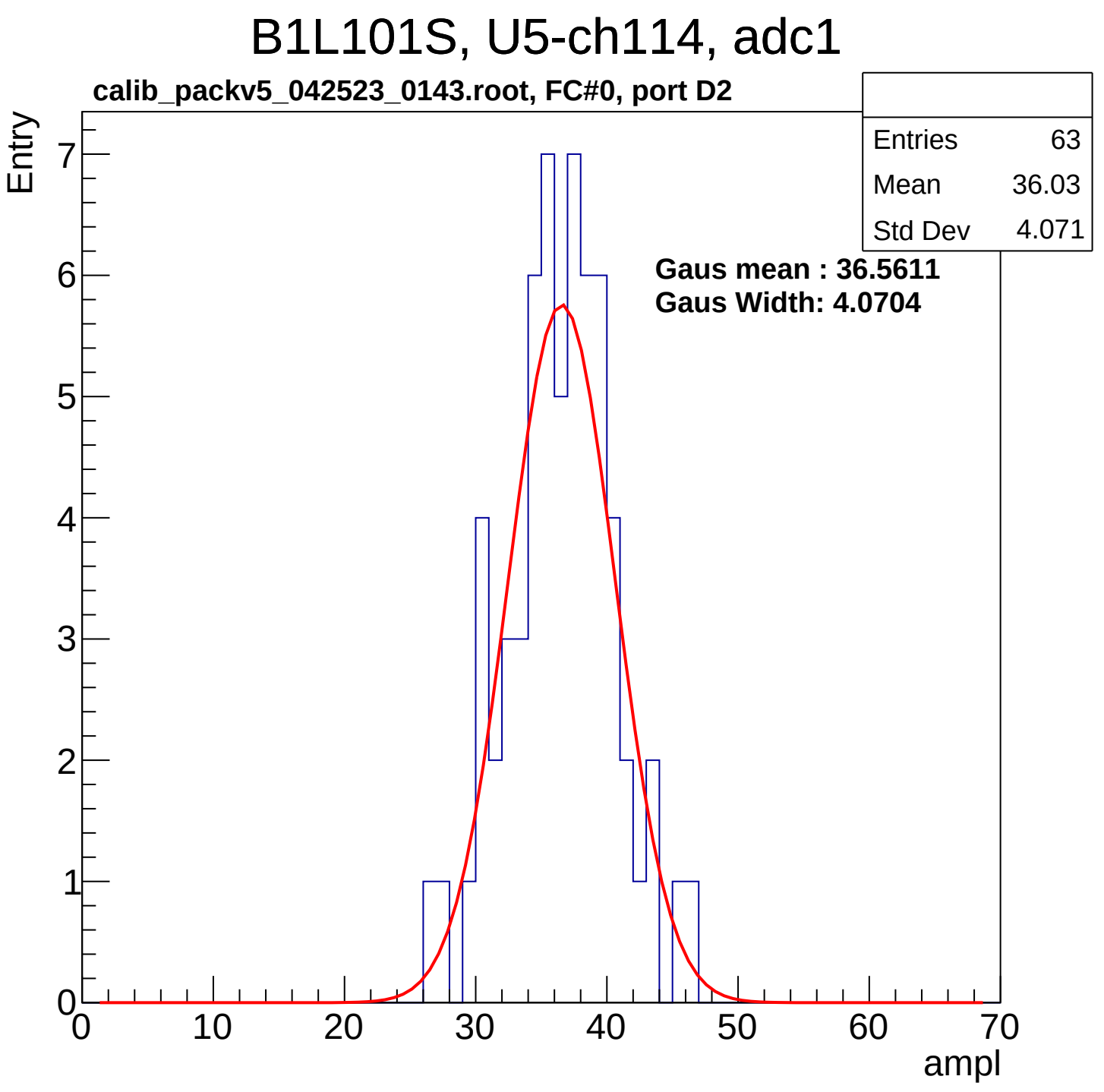
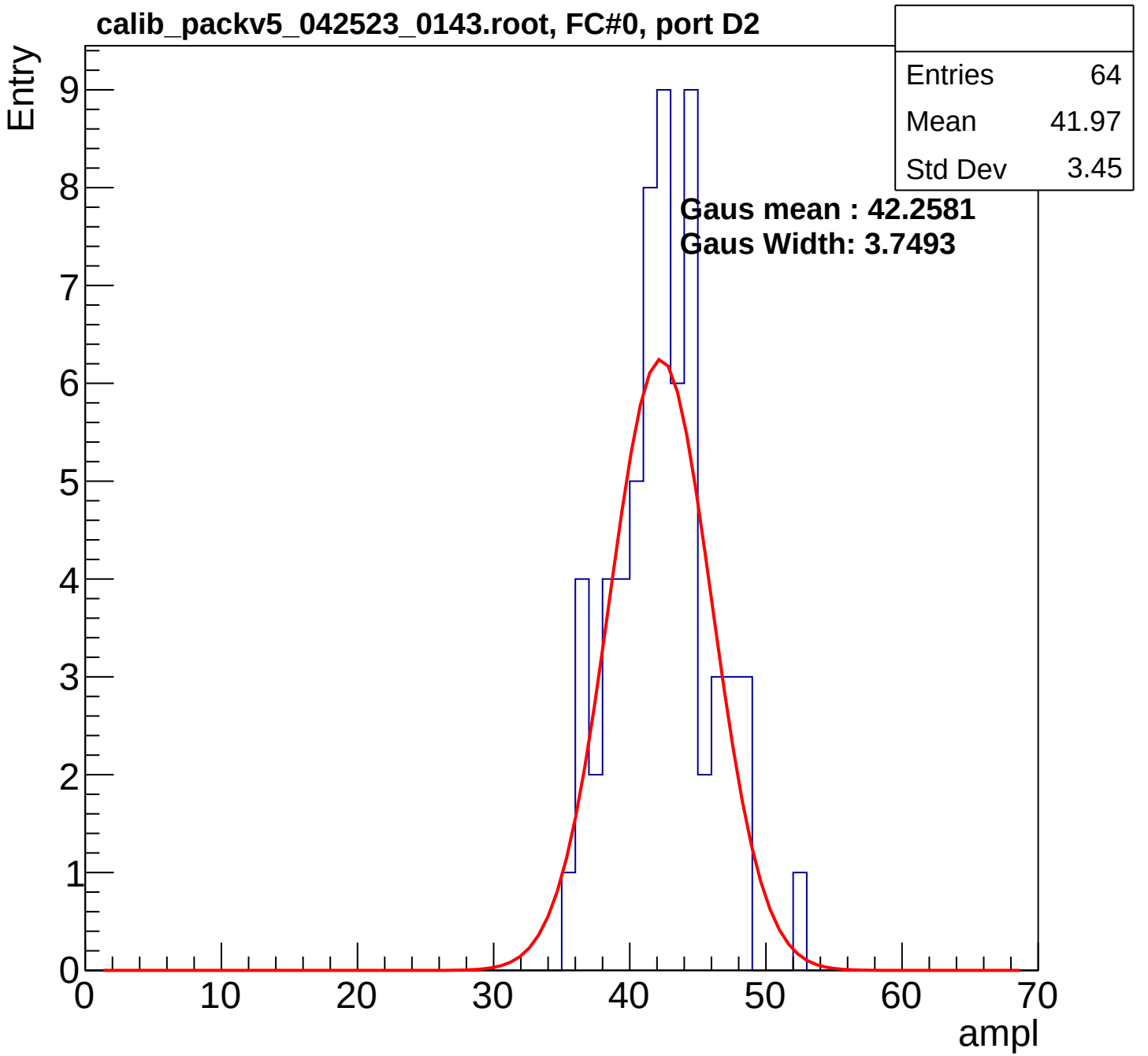
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch114, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 36.03
Std Dev 4.071
Gaus mean : 36.5611
Gaus Width: 4.0704
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch114, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 41.97
Std Dev 3.45
Gaus mean : 42.2581
Gaus Width: 3.7493
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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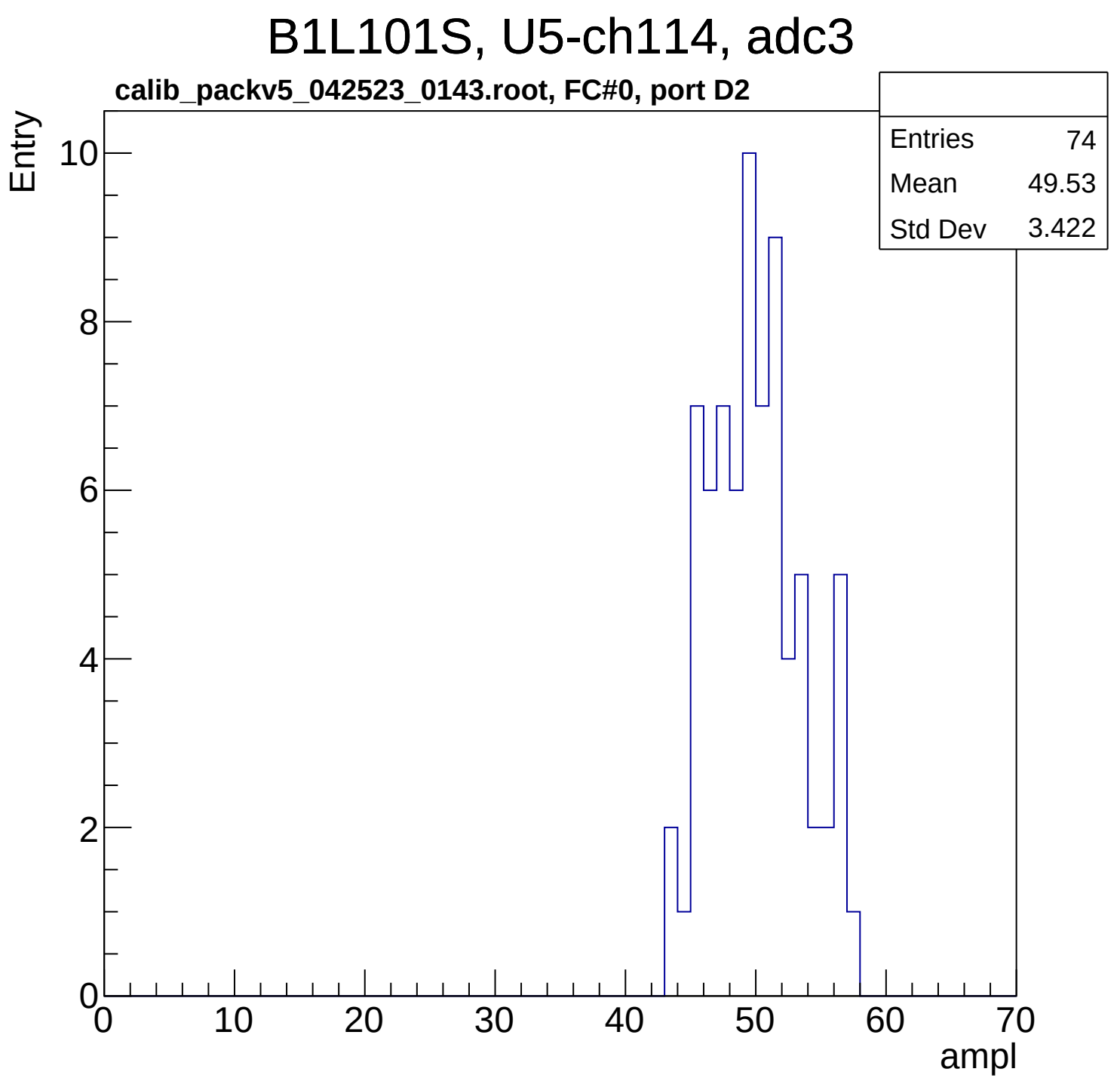
B1L101S, U5-ch114, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 49.53
Std Dev 3.422
Entry
ampl
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2
4
6
8
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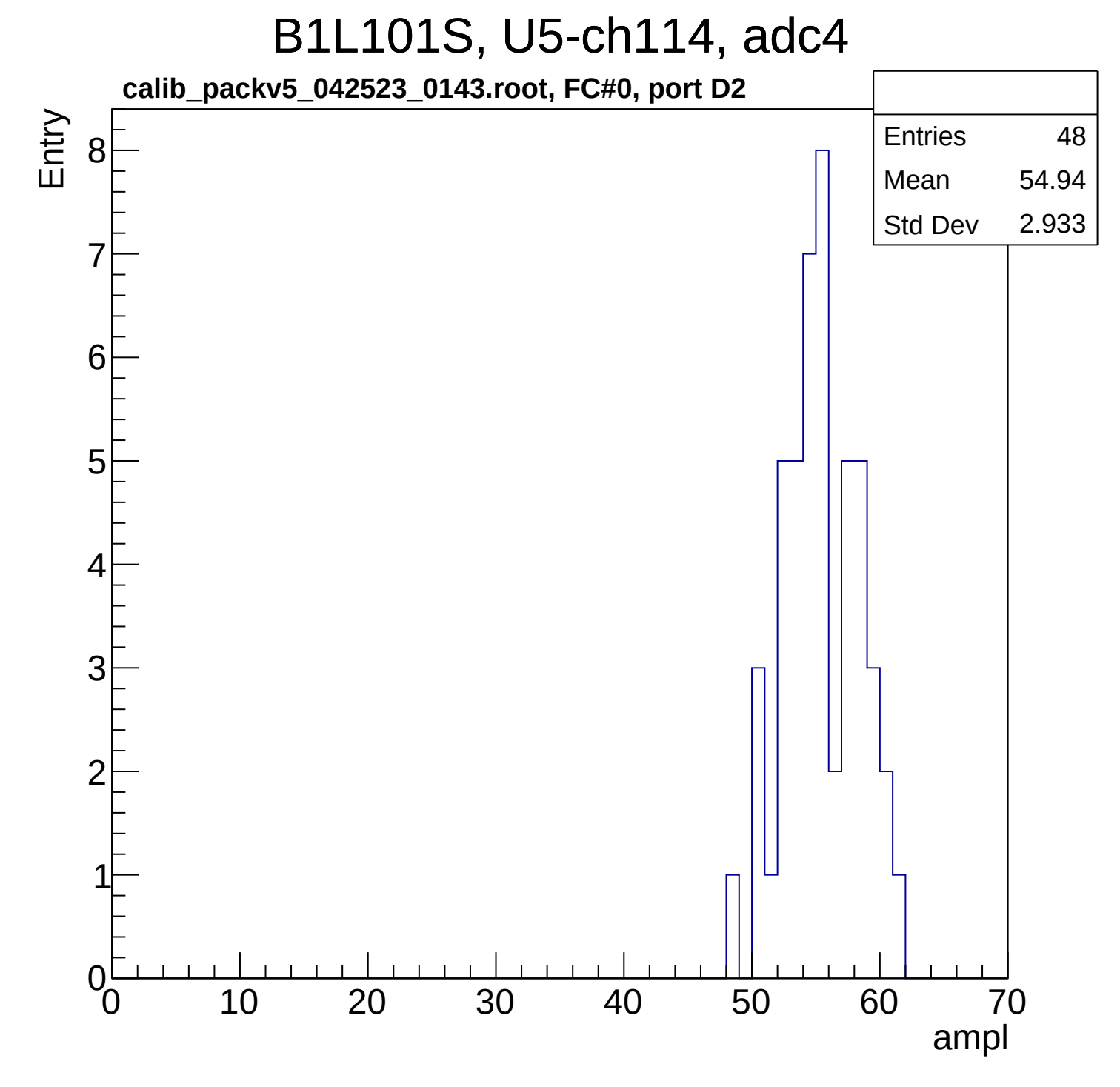
0
10
20
30
40
50
60
70


B1L101S, U5-ch114, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 54.94
Std Dev 2.933
Entry
ampl
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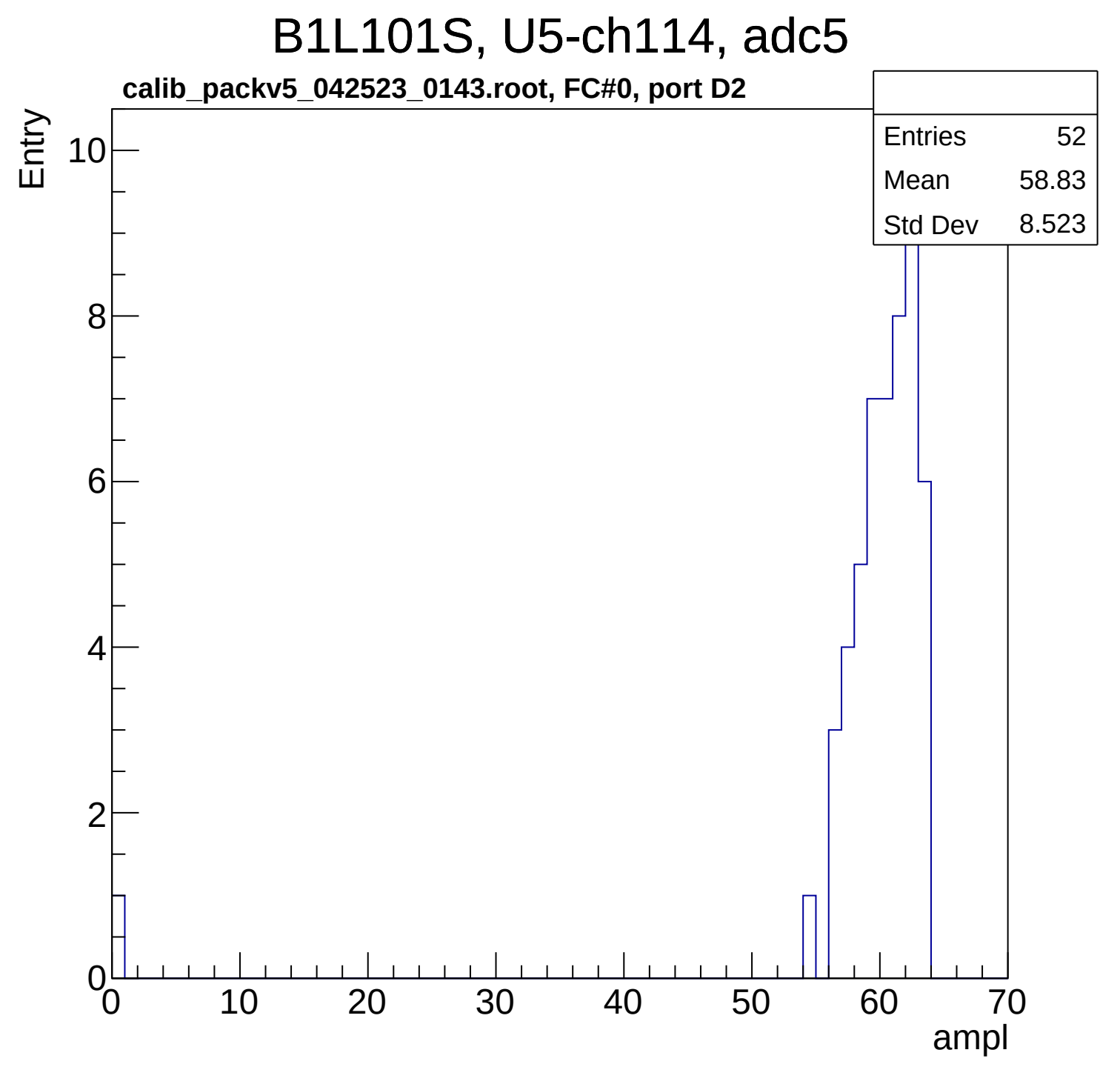
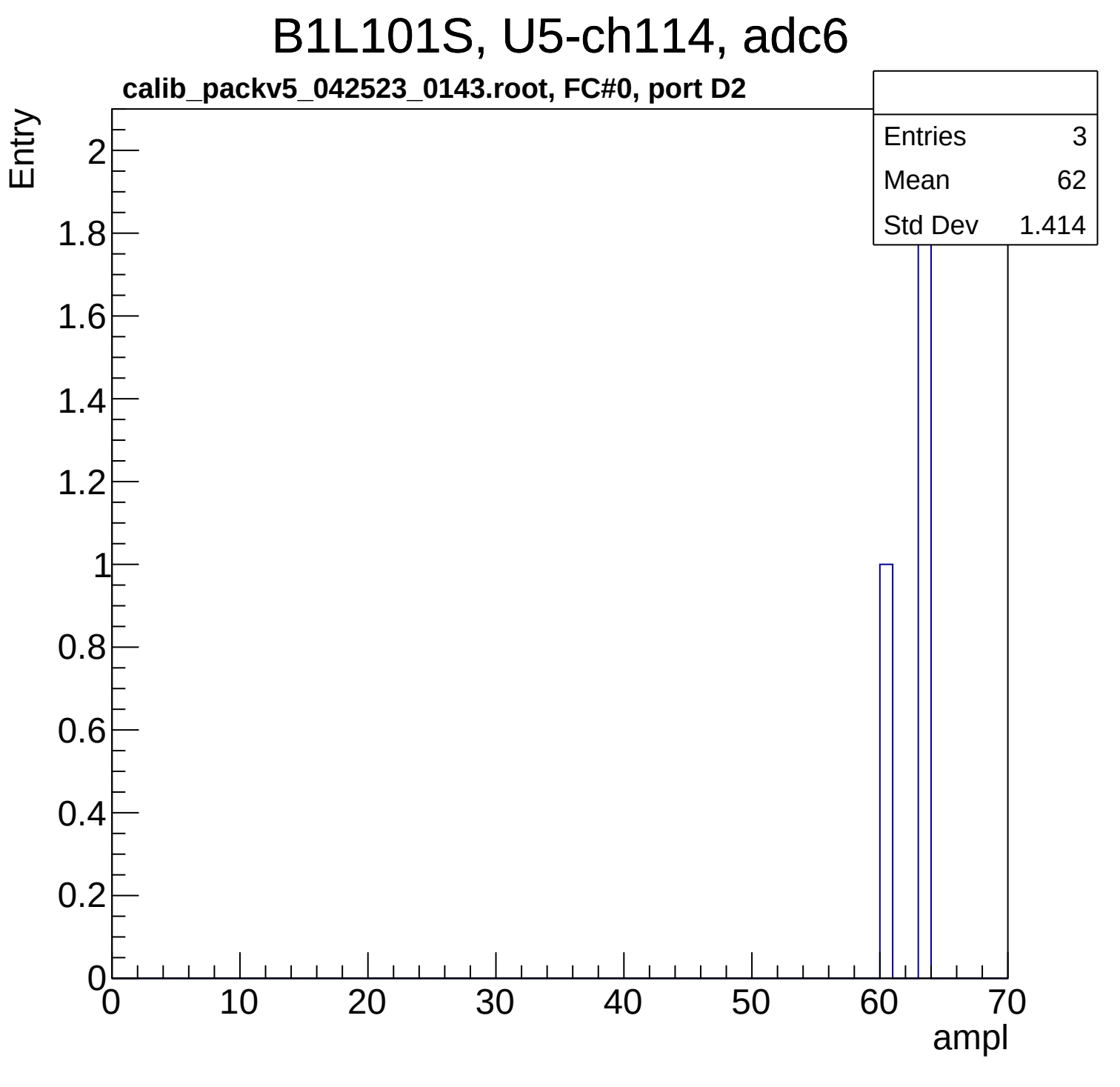
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch114, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 58.83
Std Dev 8.523
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch114, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 62
Std Dev 1.414
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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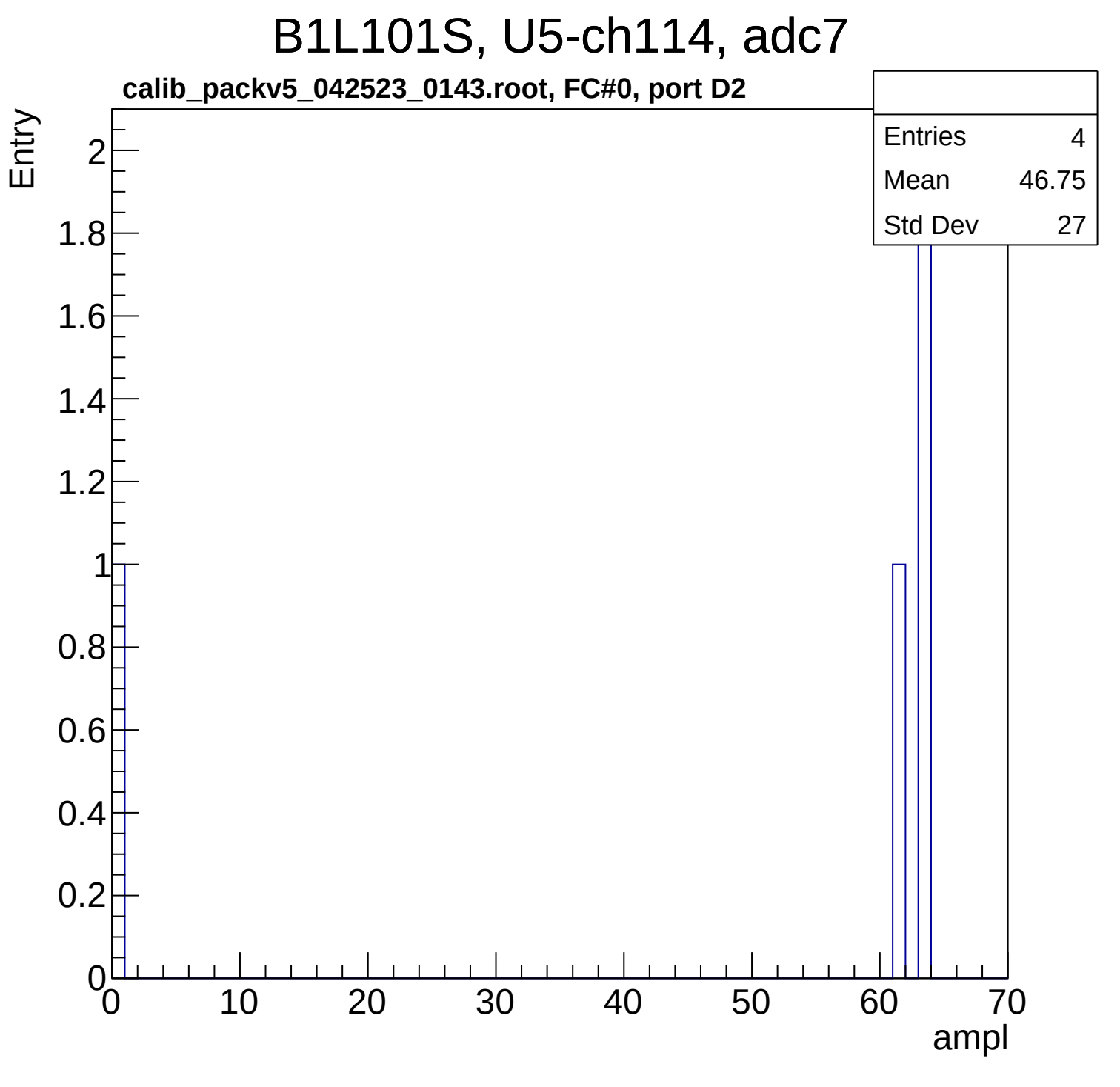
20
30
40
50
60
70


B1L101S, U5-ch114, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 46.75
Std Dev 27
Entry
ampl
0
0.2
0.4
0.6
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1.2
1.4
1.6
1.8
2
0
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30
40
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60
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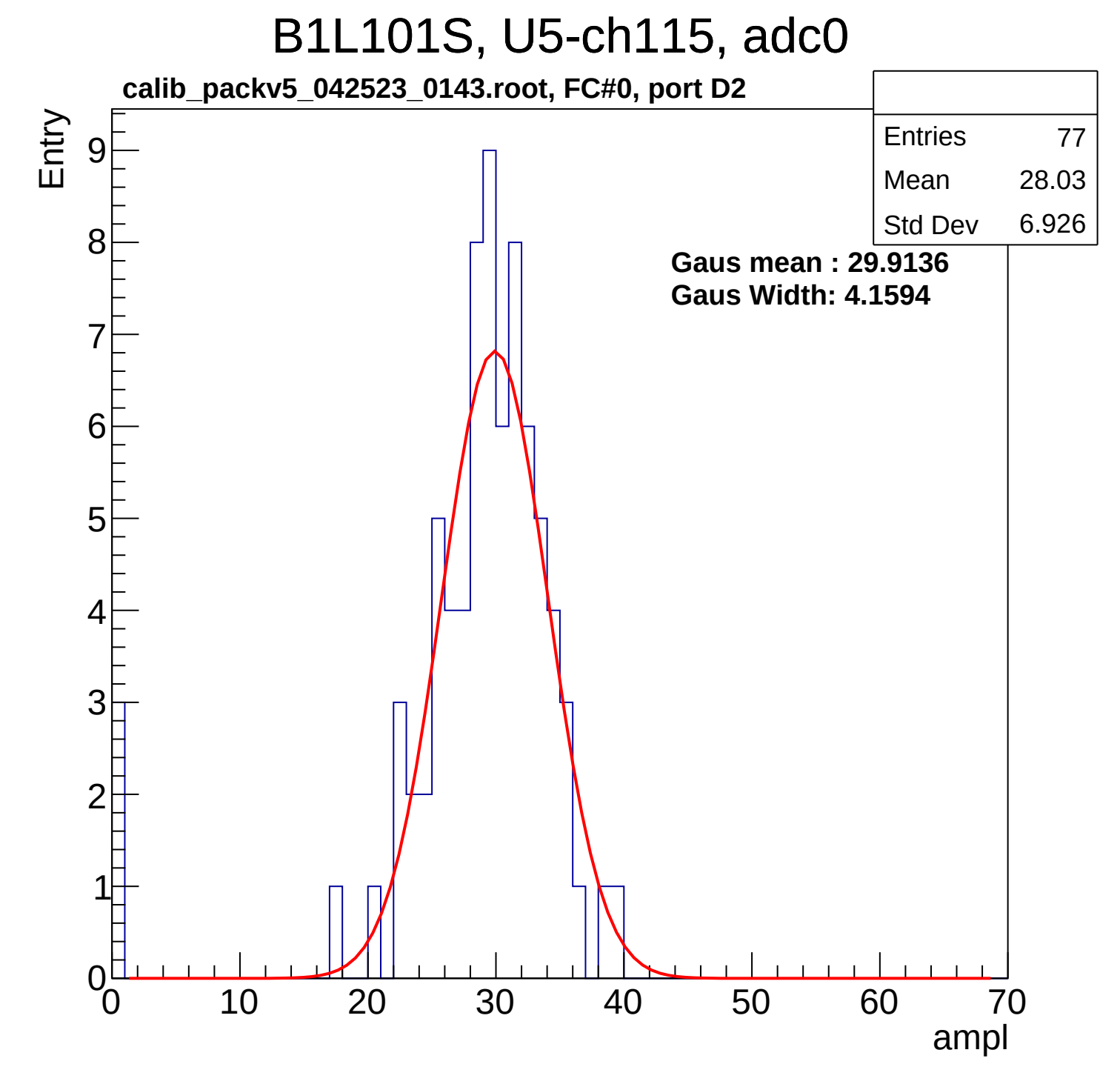
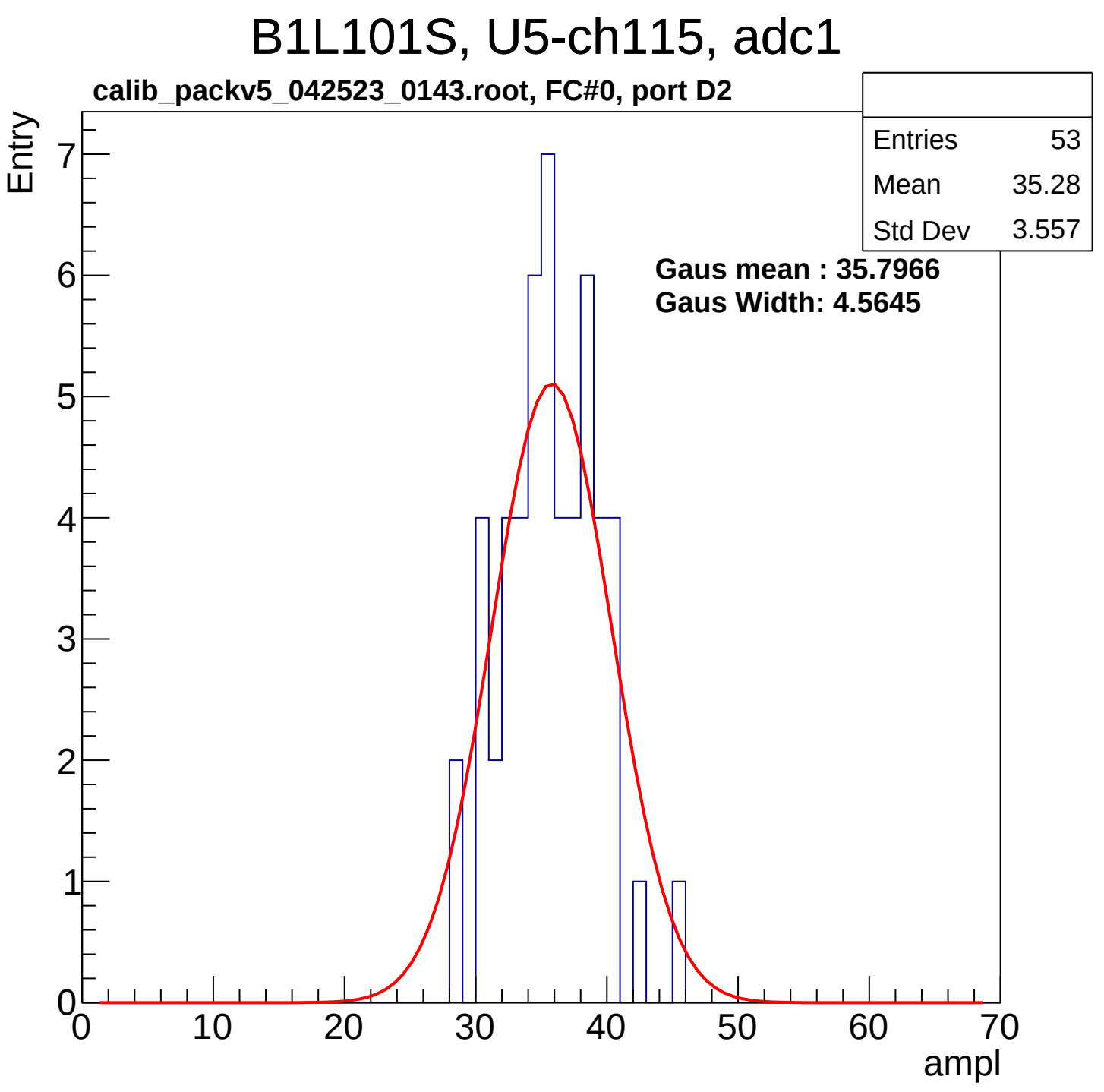
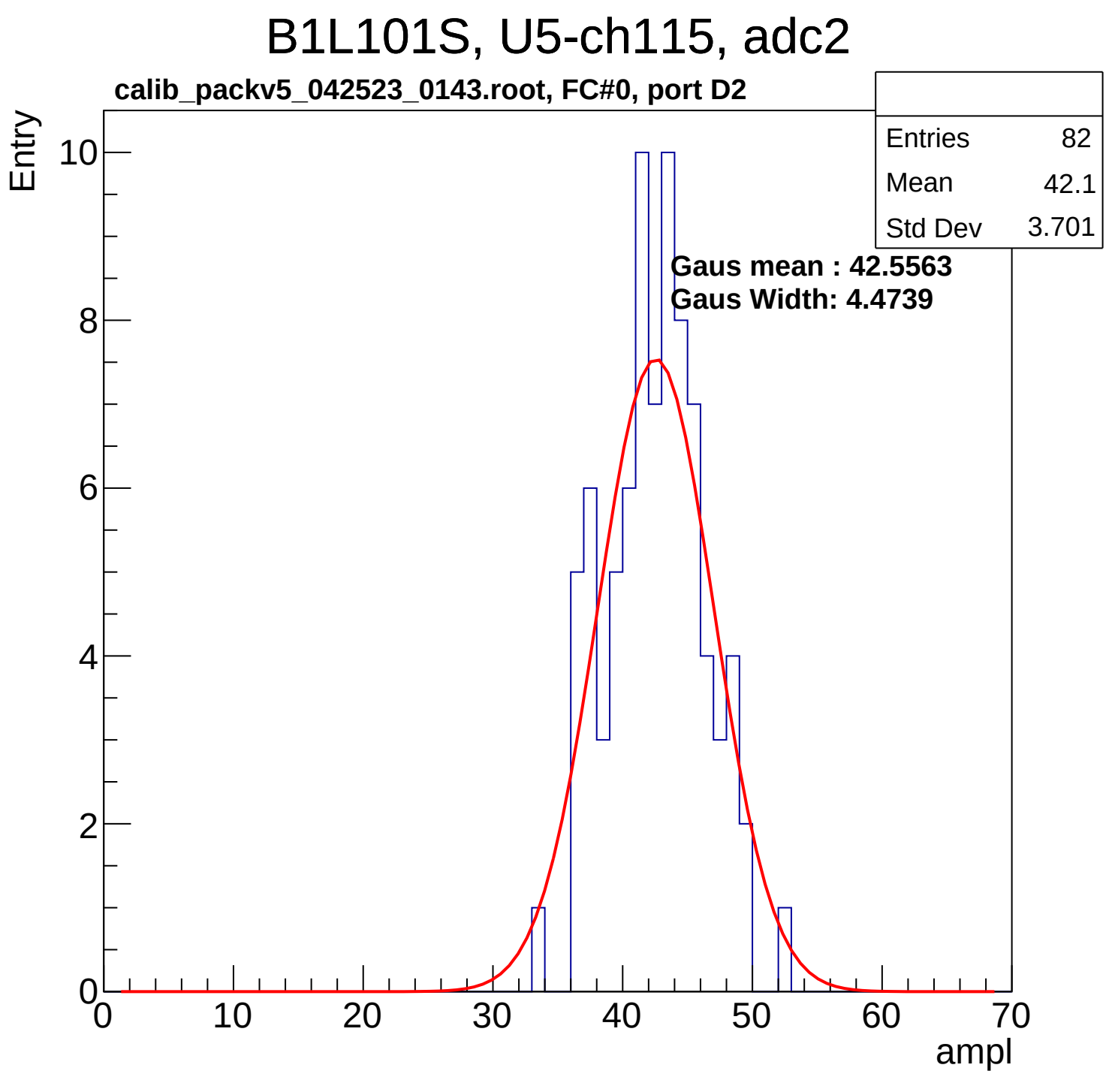
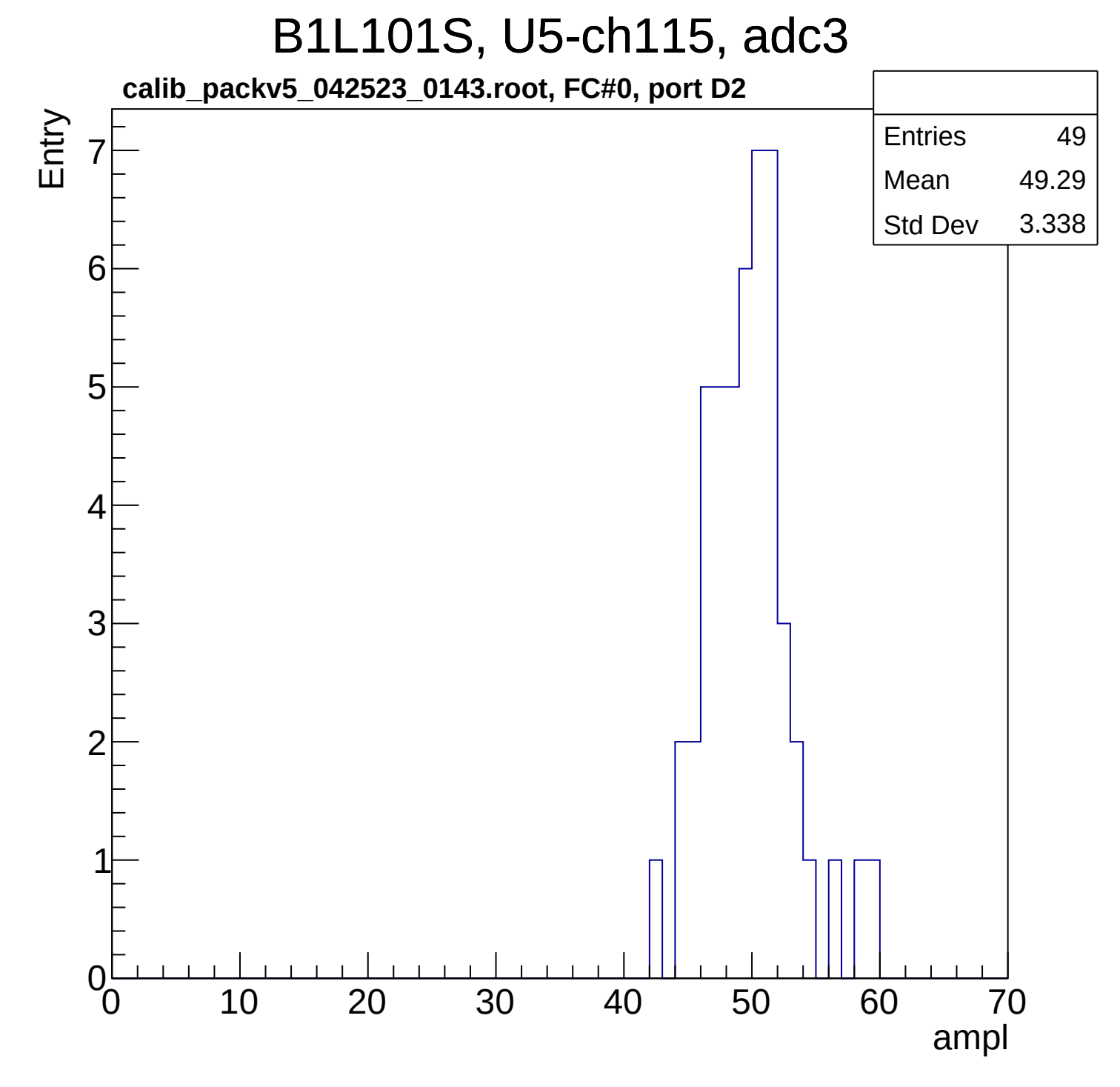

B1L101S, U5-ch115, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 28.03
Std Dev 6.926
Gaus mean : 29.9136
Gaus Width: 4.1594
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch115, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 35.28
Std Dev 3.557
Gaus mean : 35.7966
Gaus Width: 4.5645
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch115, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 82
Mean 42.1
Std Dev 3.701
Gaus mean : 42.5563
Gaus Width: 4.4739
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch115, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 49.29
Std Dev 3.338
Entry
ampl
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4
5
6
7
0
10
20
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40
50
60
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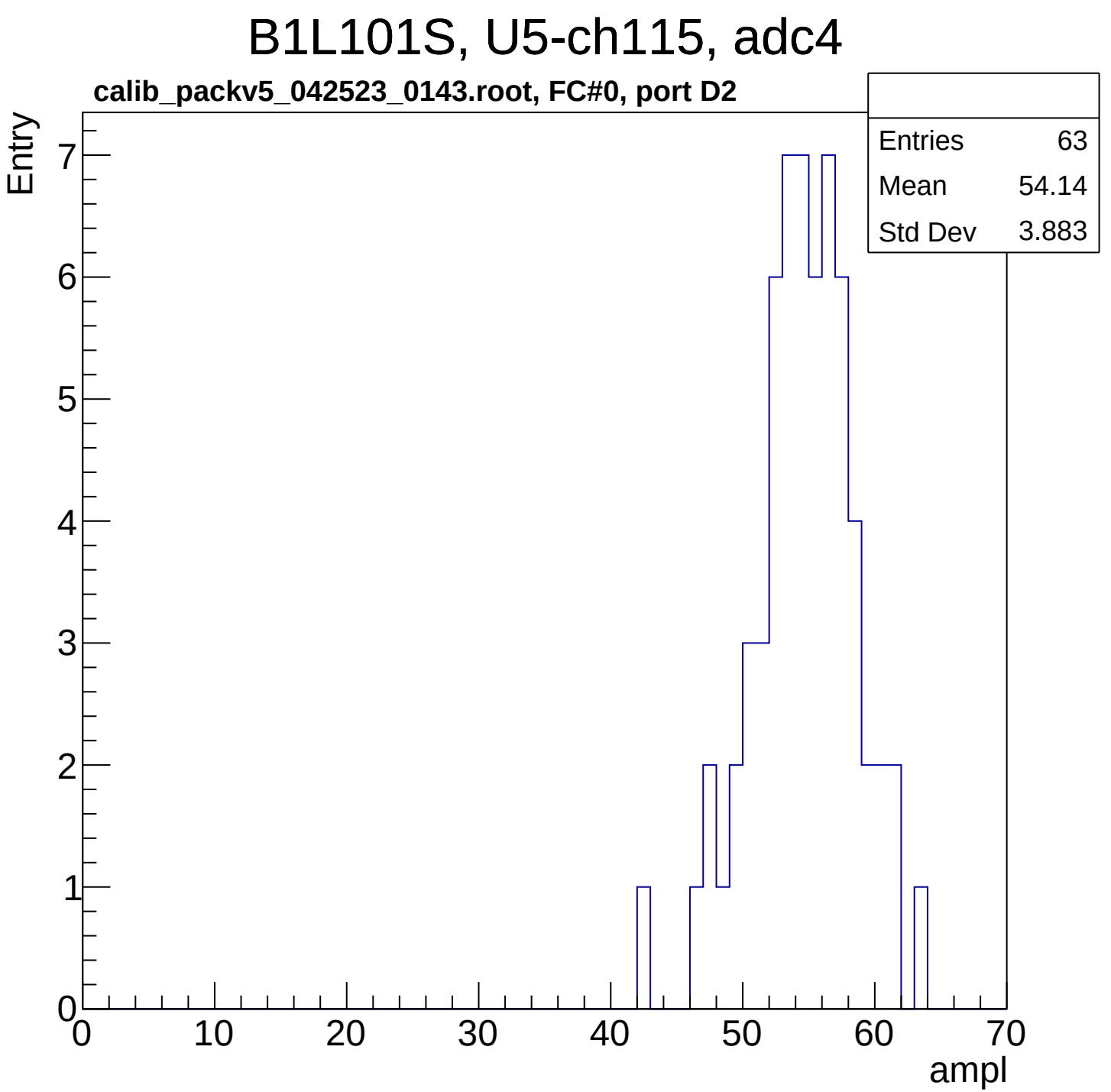
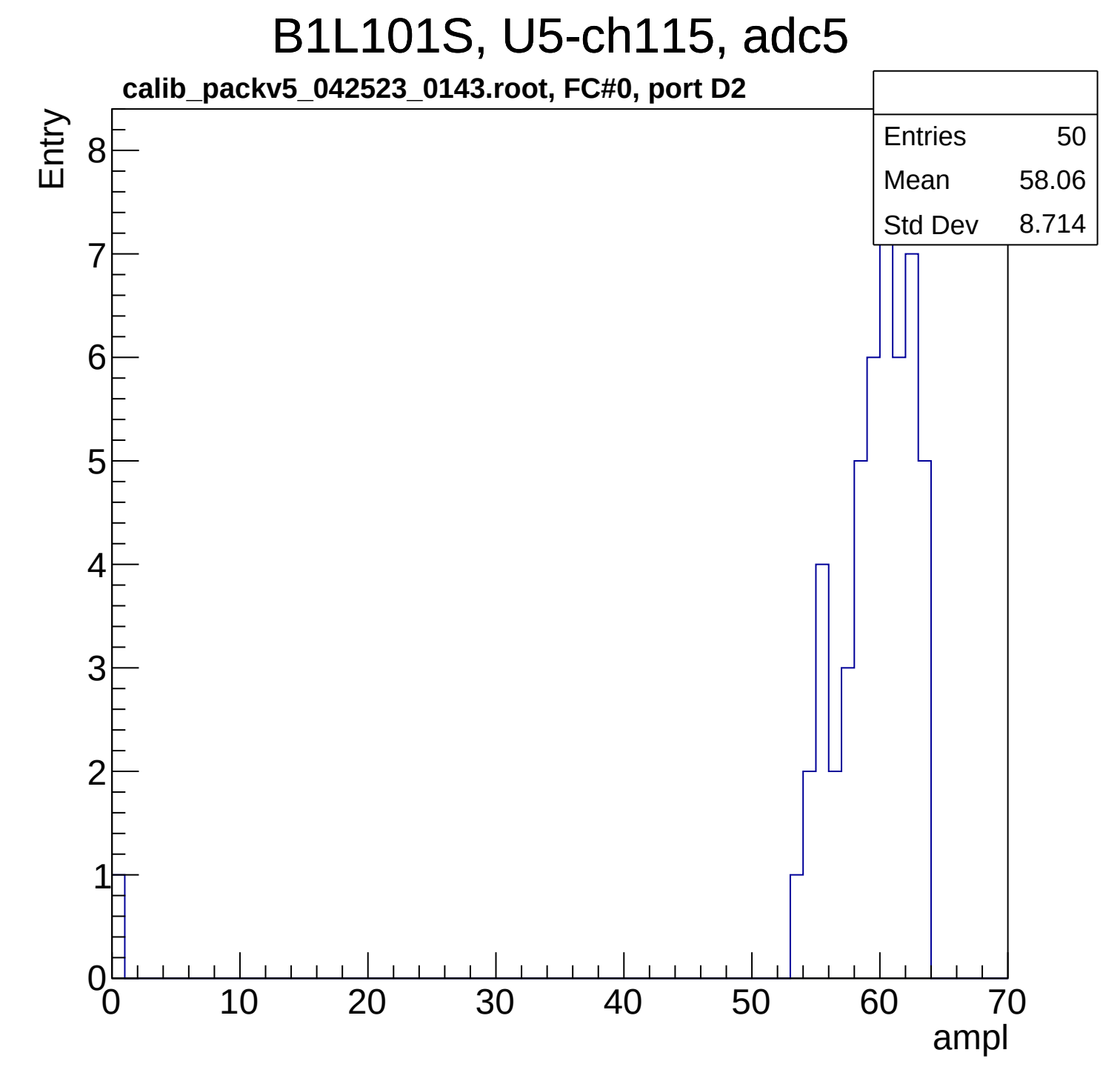

B1L101S, U5-ch115, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 54.14
Std Dev 3.883
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch115, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 58.06
Std Dev 8.714
Entry
ampl
0
1
2
3
4
5
6
7
8
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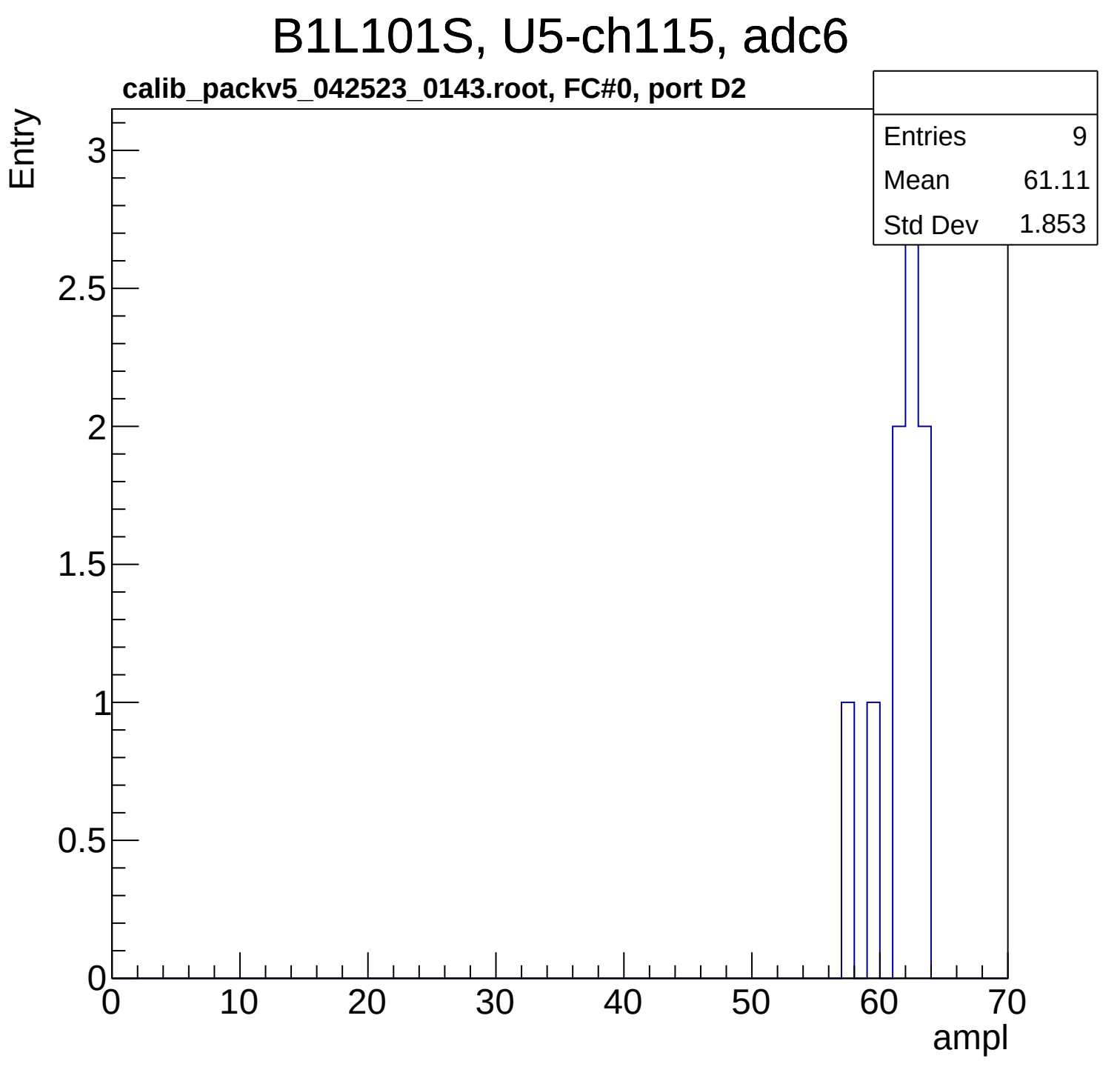
B1L101S, U5-ch115, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 61.11
Std Dev 1.853
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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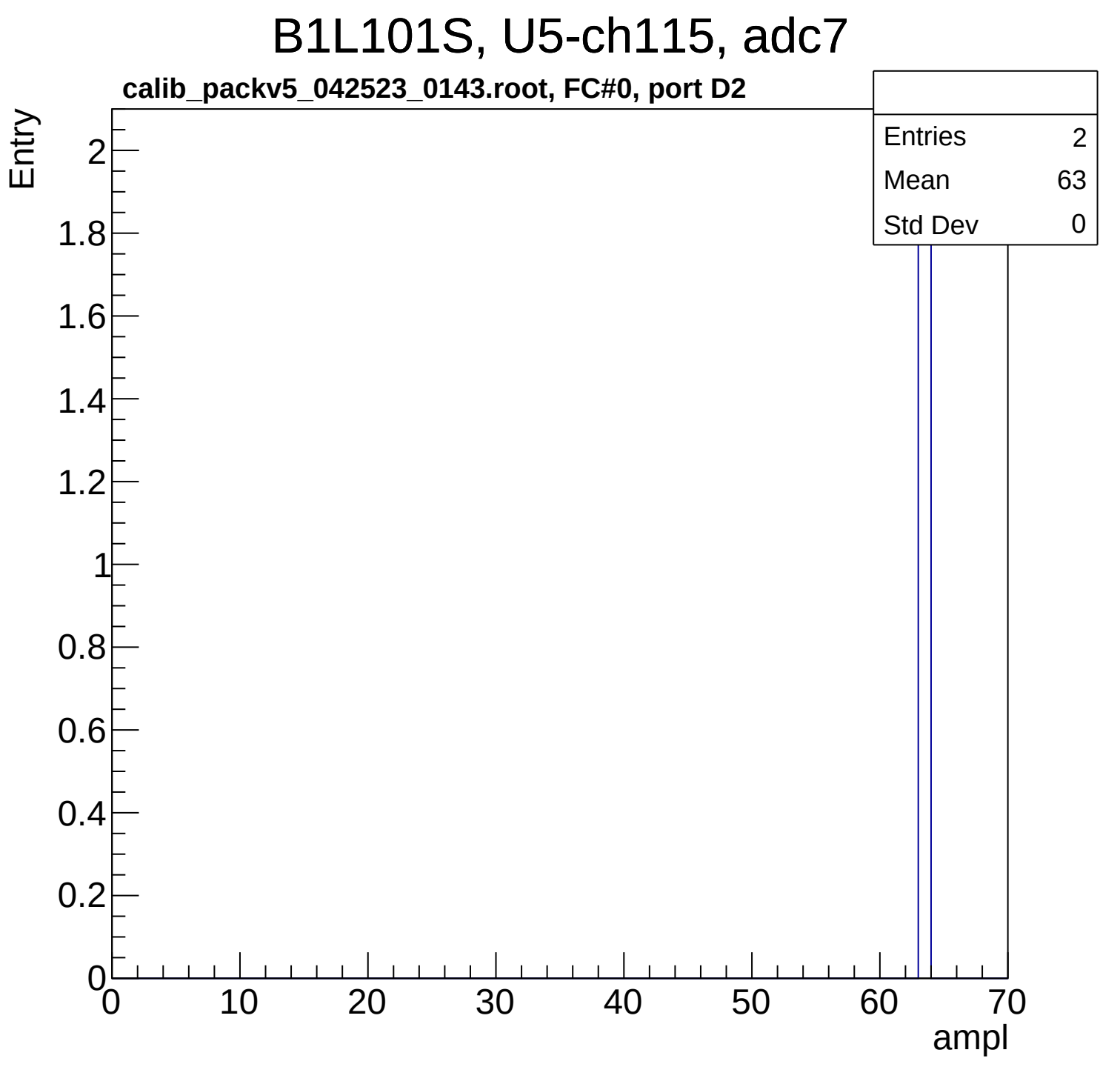
B1L101S, U5-ch115, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
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40
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60
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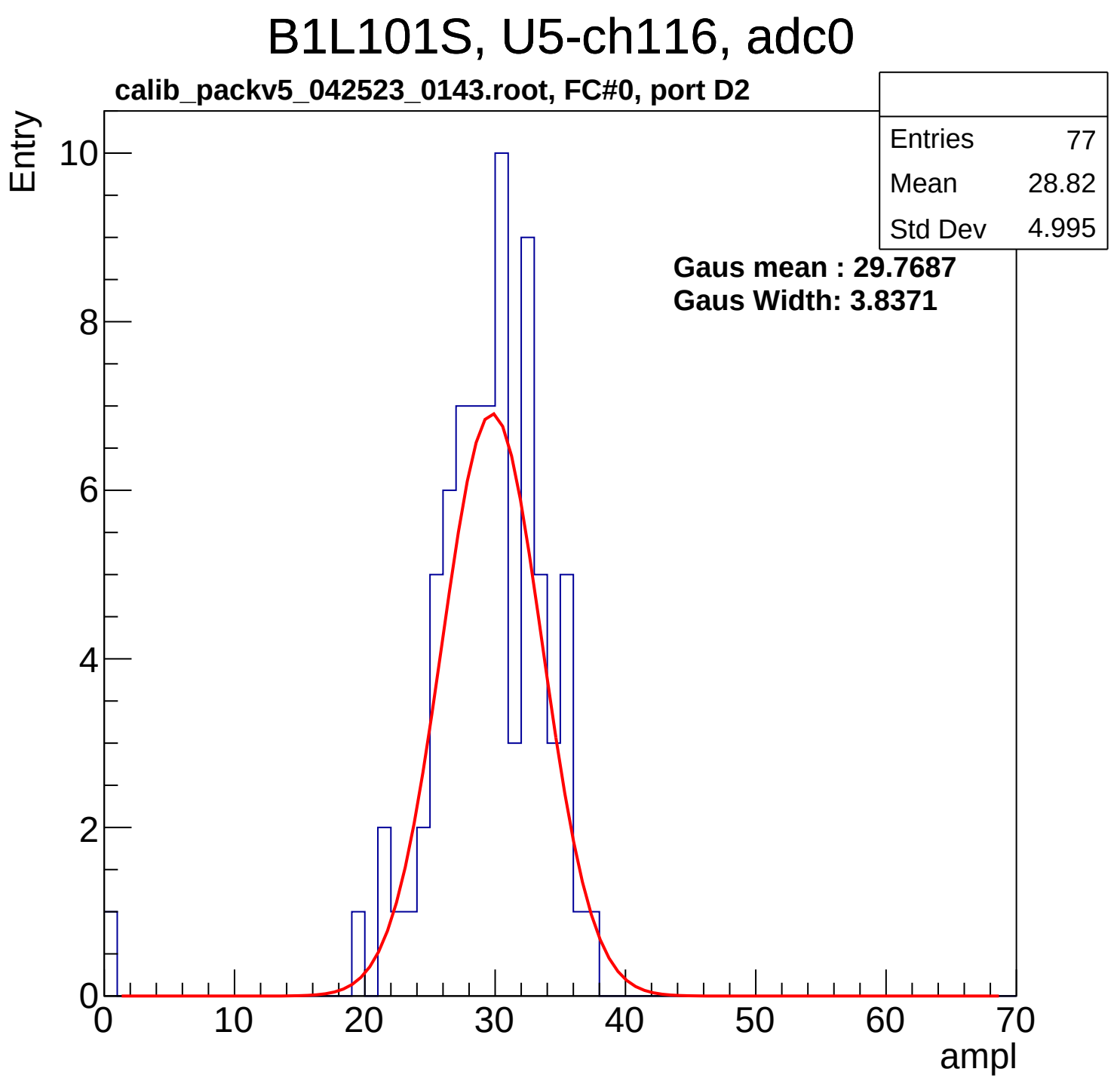
B1L101S, U5-ch116, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 28.82
Std Dev 4.995
Gaus mean : 29.7687
Gaus Width: 3.8371
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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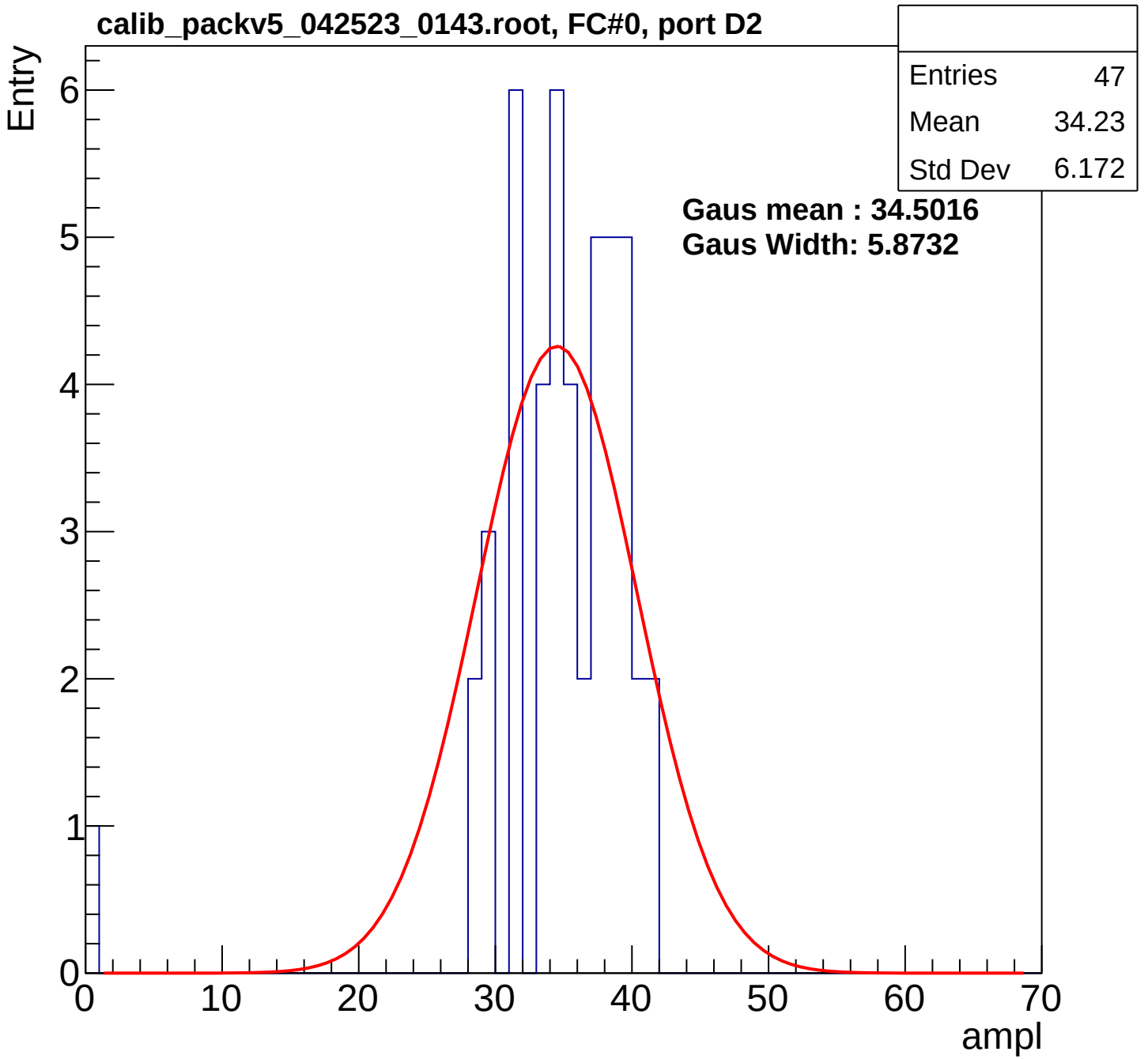
B1L101S, U5-ch116, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 34.23
Std Dev 6.172
Gaus mean : 34.5016
Gaus Width: 5.8732
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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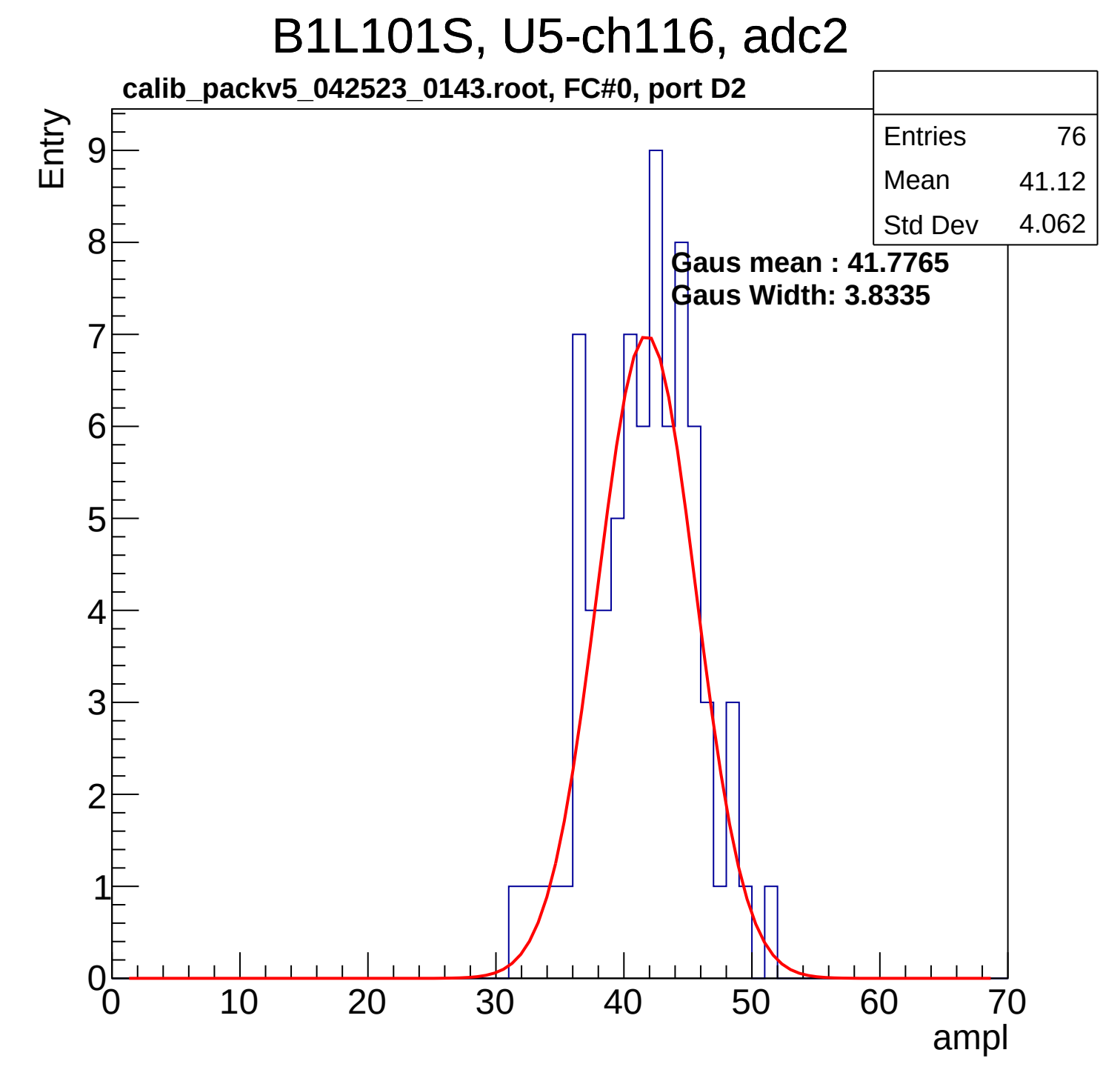
B1L101S, U5-ch116, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 41.12
Std Dev 4.062
Gaus mean : 41.7765
Gaus Width: 3.8335
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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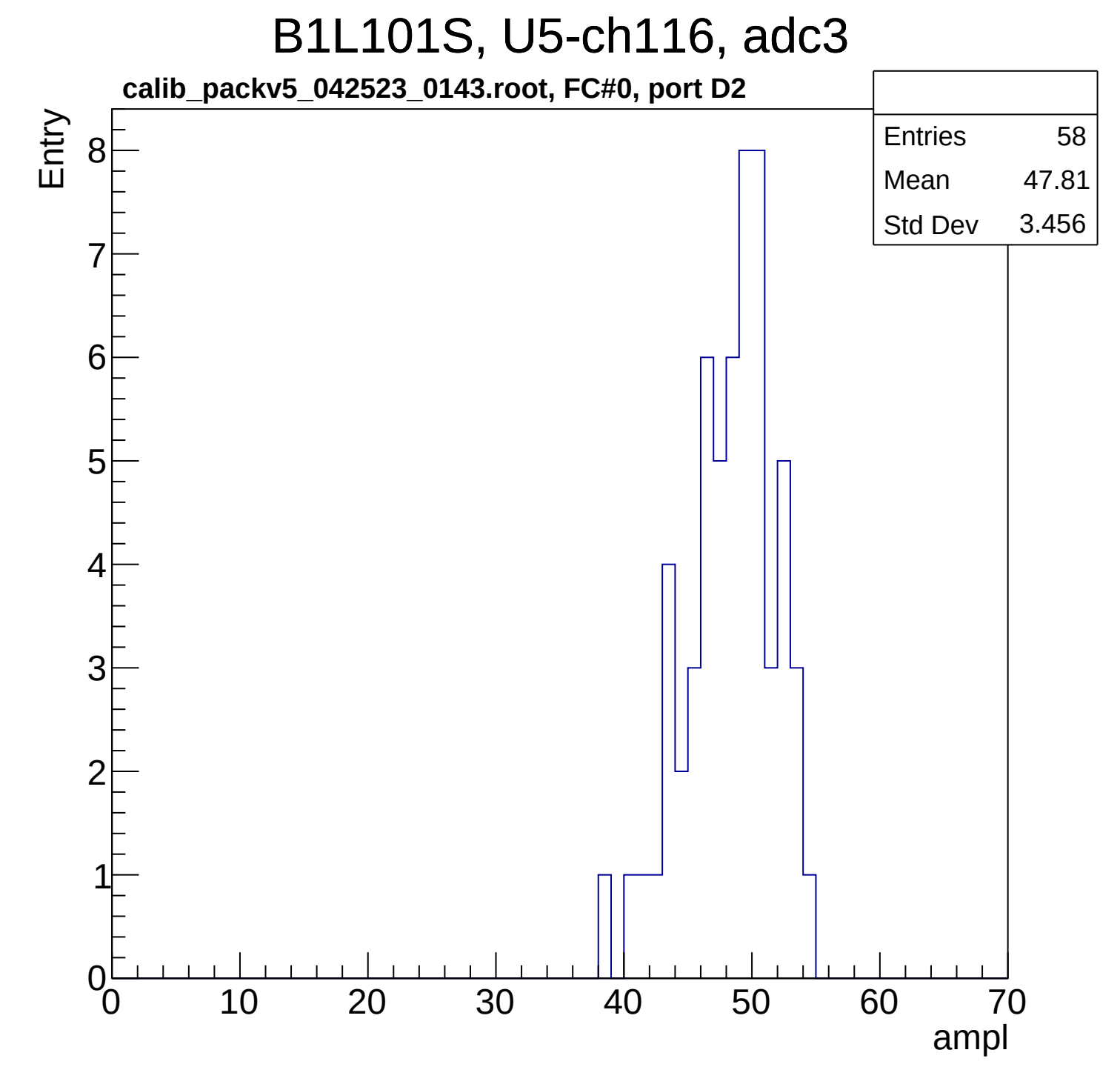
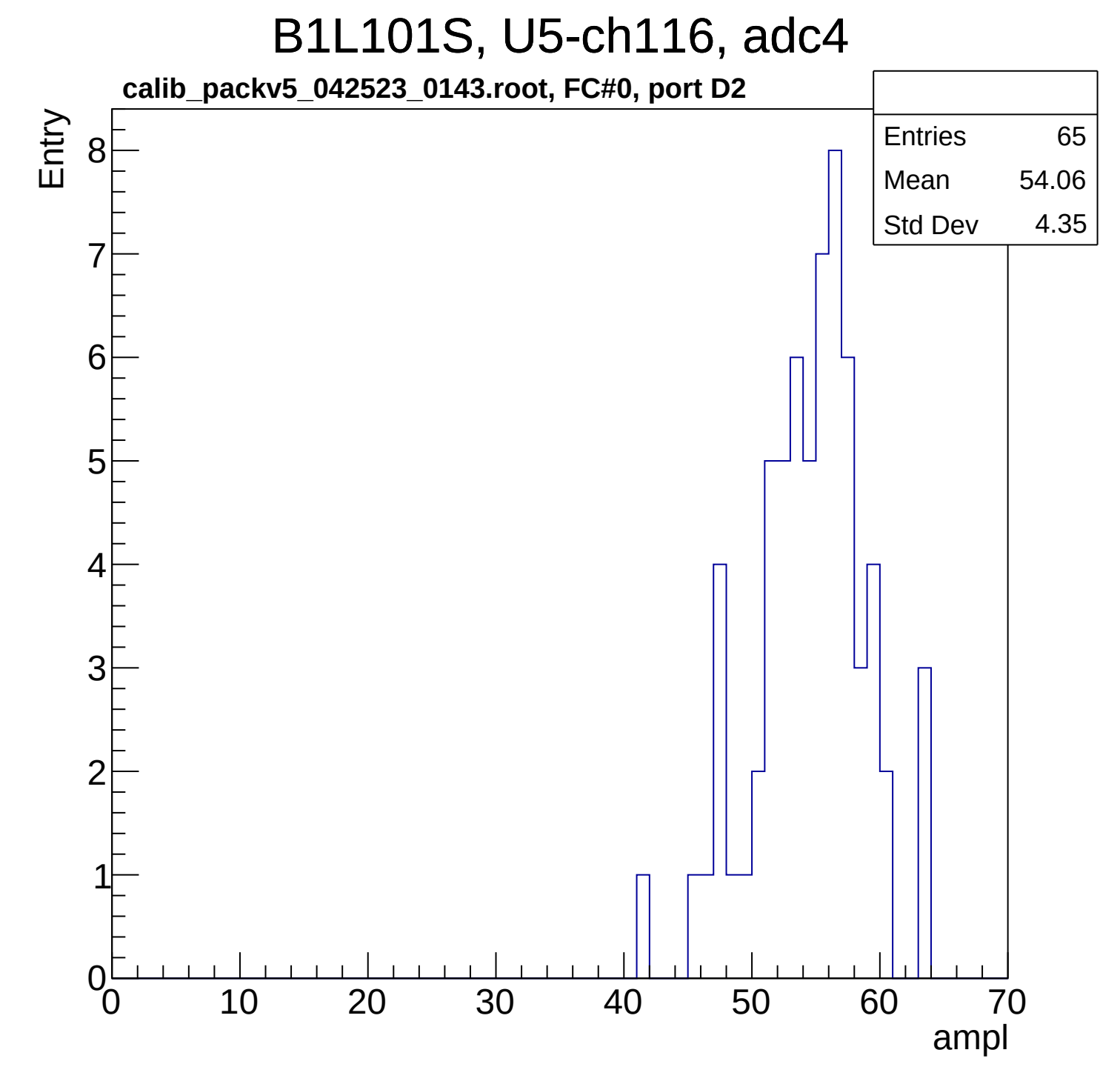
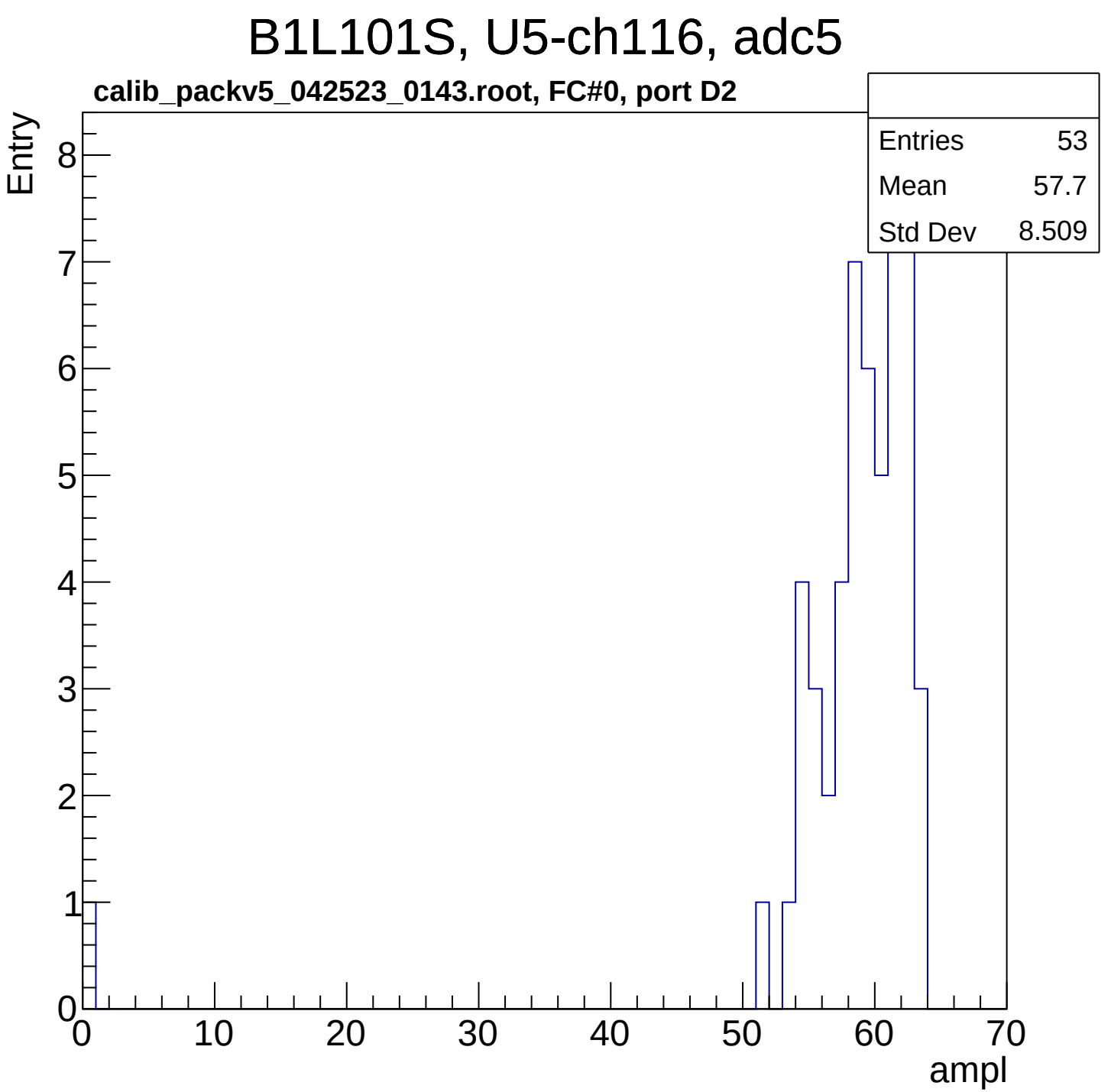
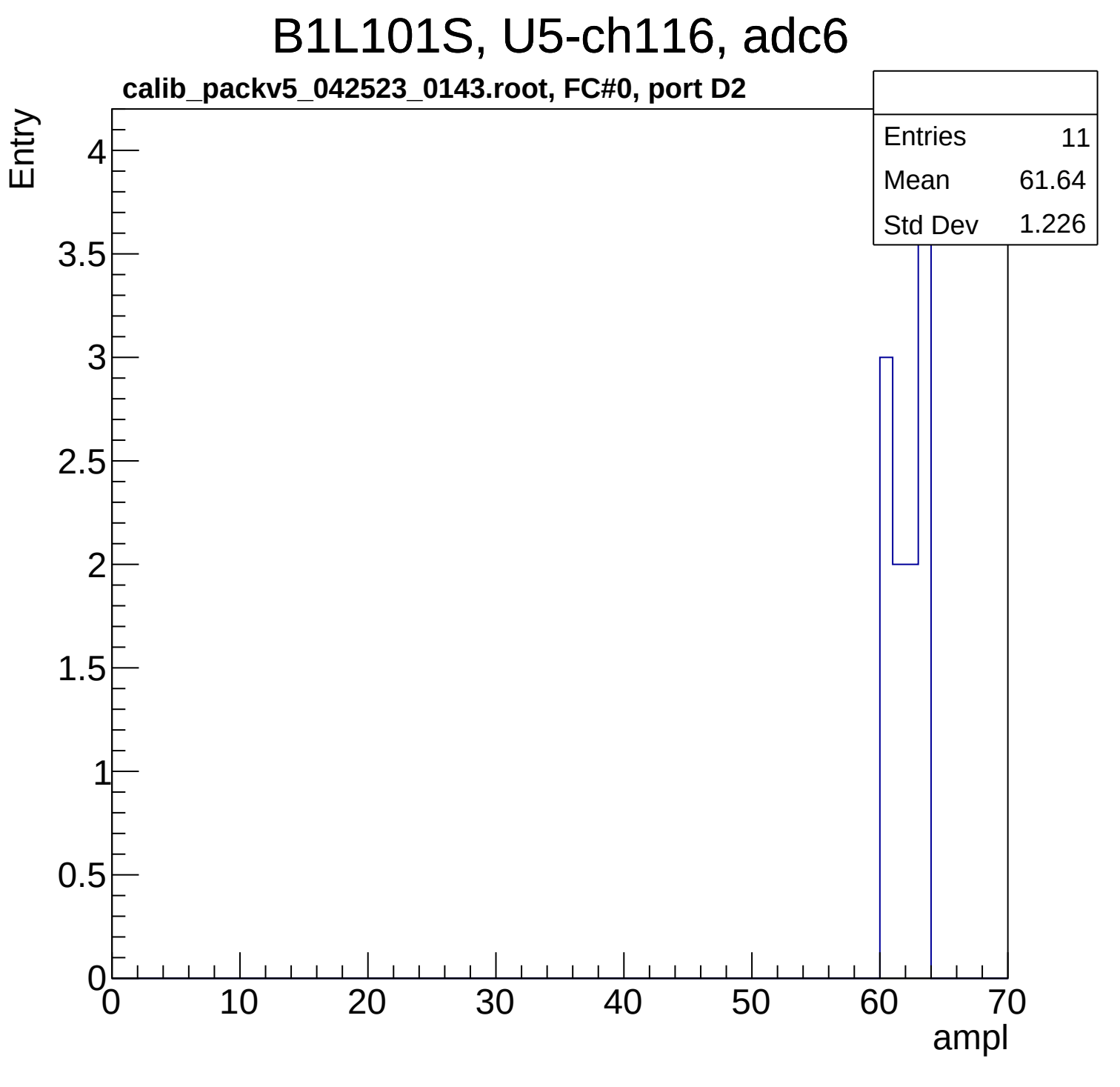
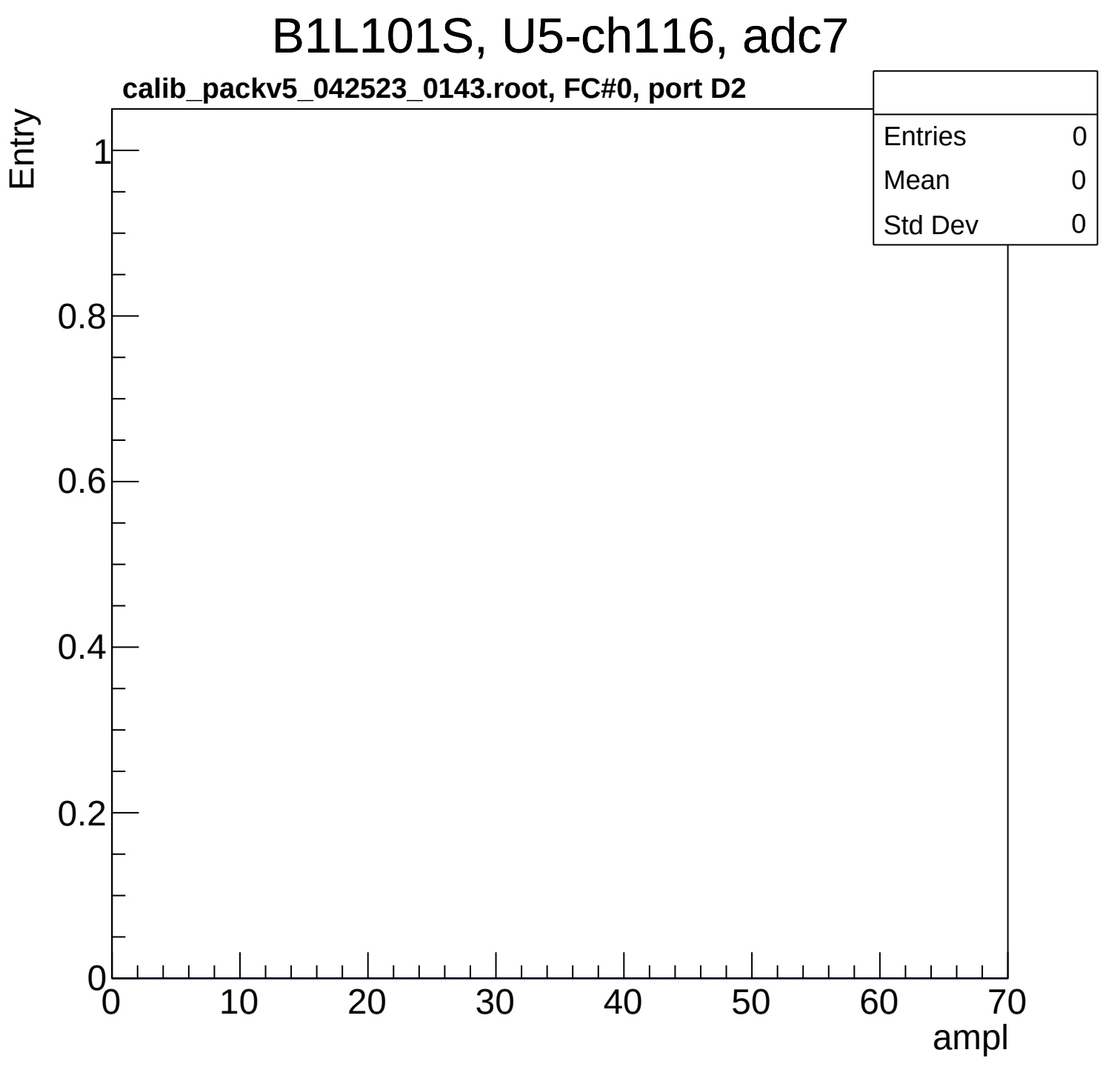
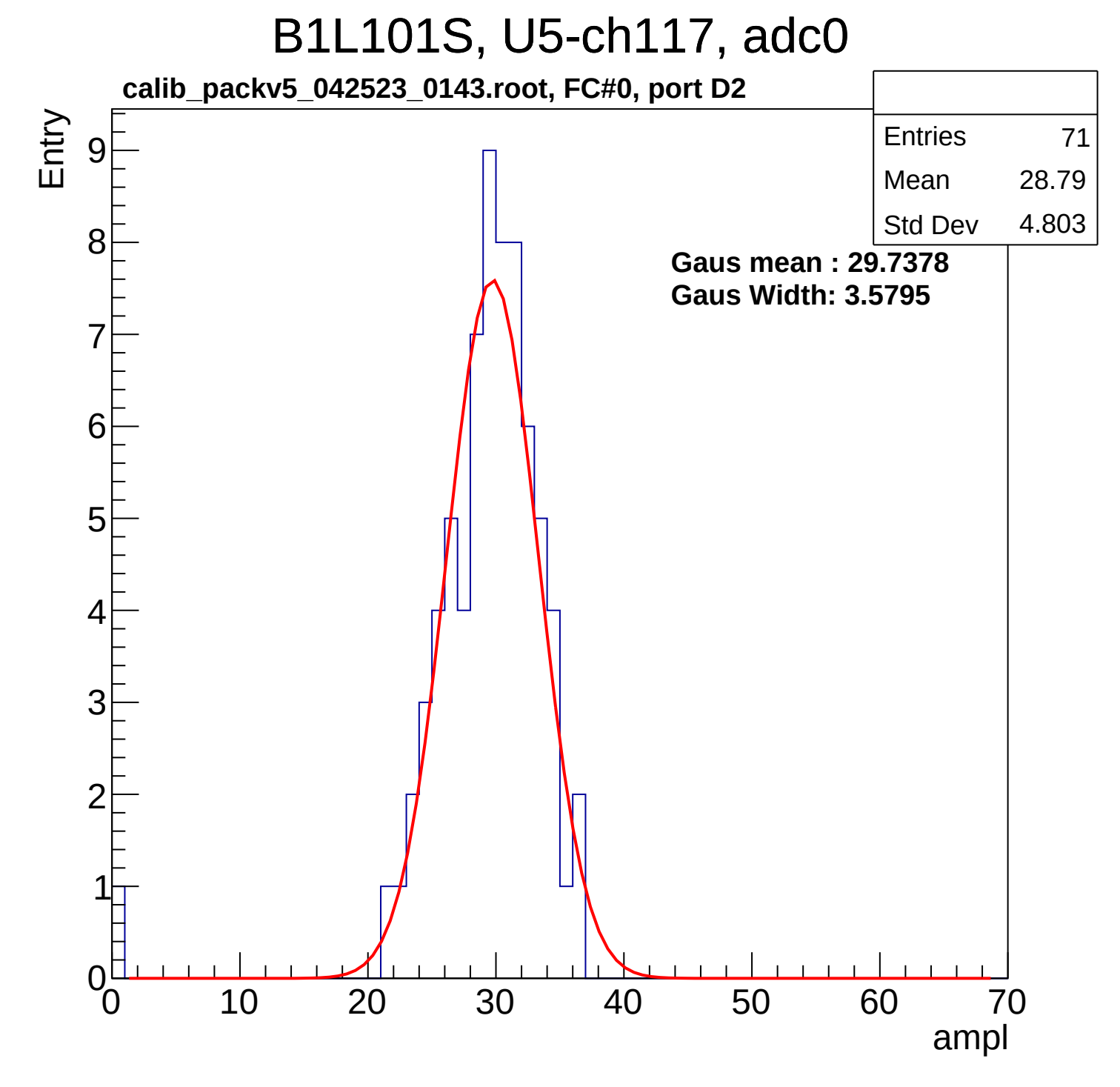

B1L101S, U5-ch116, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 47.81
Std Dev 3.456
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

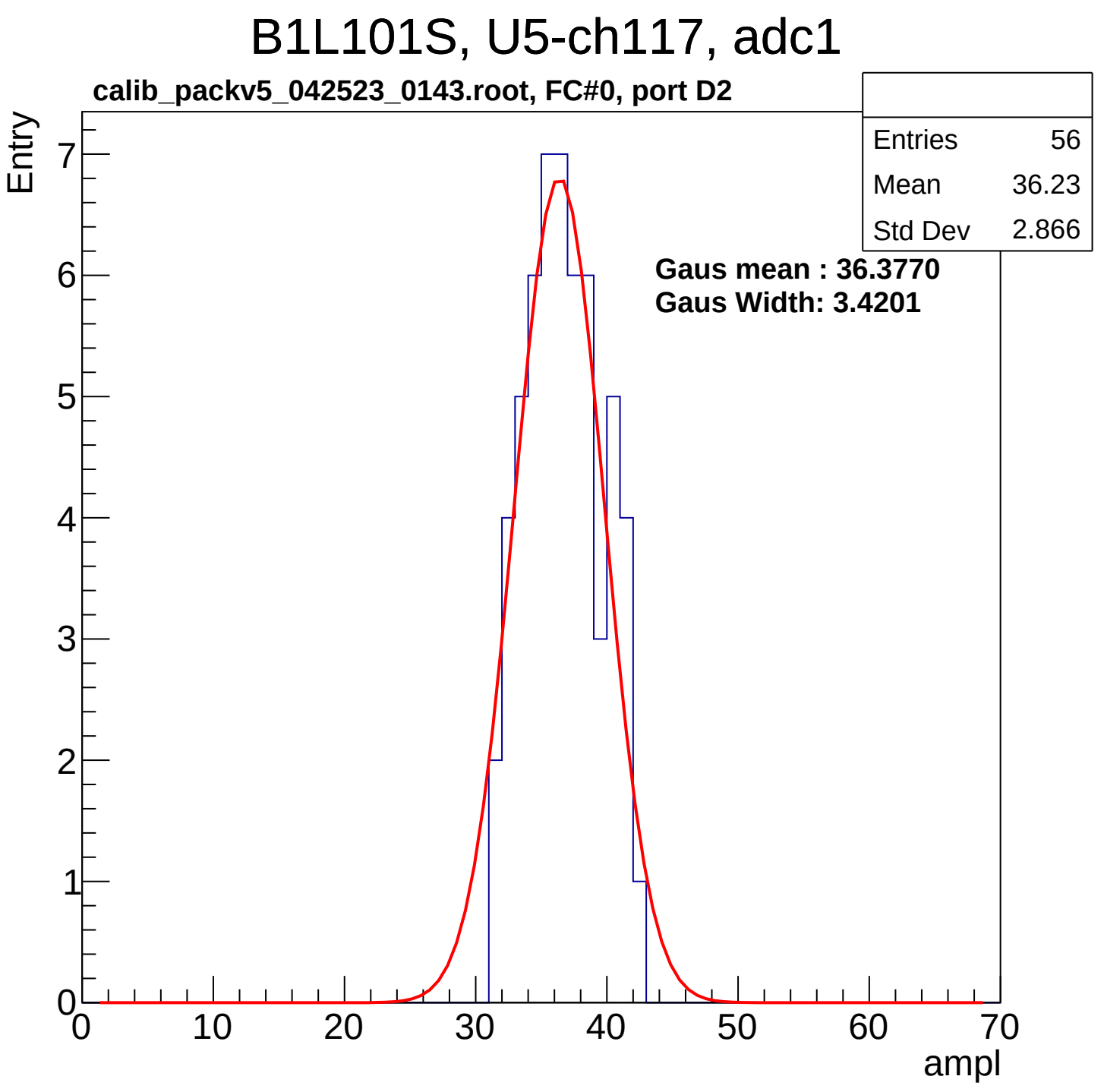

B1L101S, U5-ch116, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 54.06
Std Dev 4.35
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch116, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 57.7
Std Dev 8.509
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch116, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 11
Mean 61.64
Std Dev 1.226
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L101S, U5-ch116, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch117, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 28.79
Std Dev 4.803
Gaus mean : 29.7378
Gaus Width: 3.5795
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch117, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 36.23
Std Dev 2.866
Gaus mean : 36.3770
Gaus Width: 3.4201
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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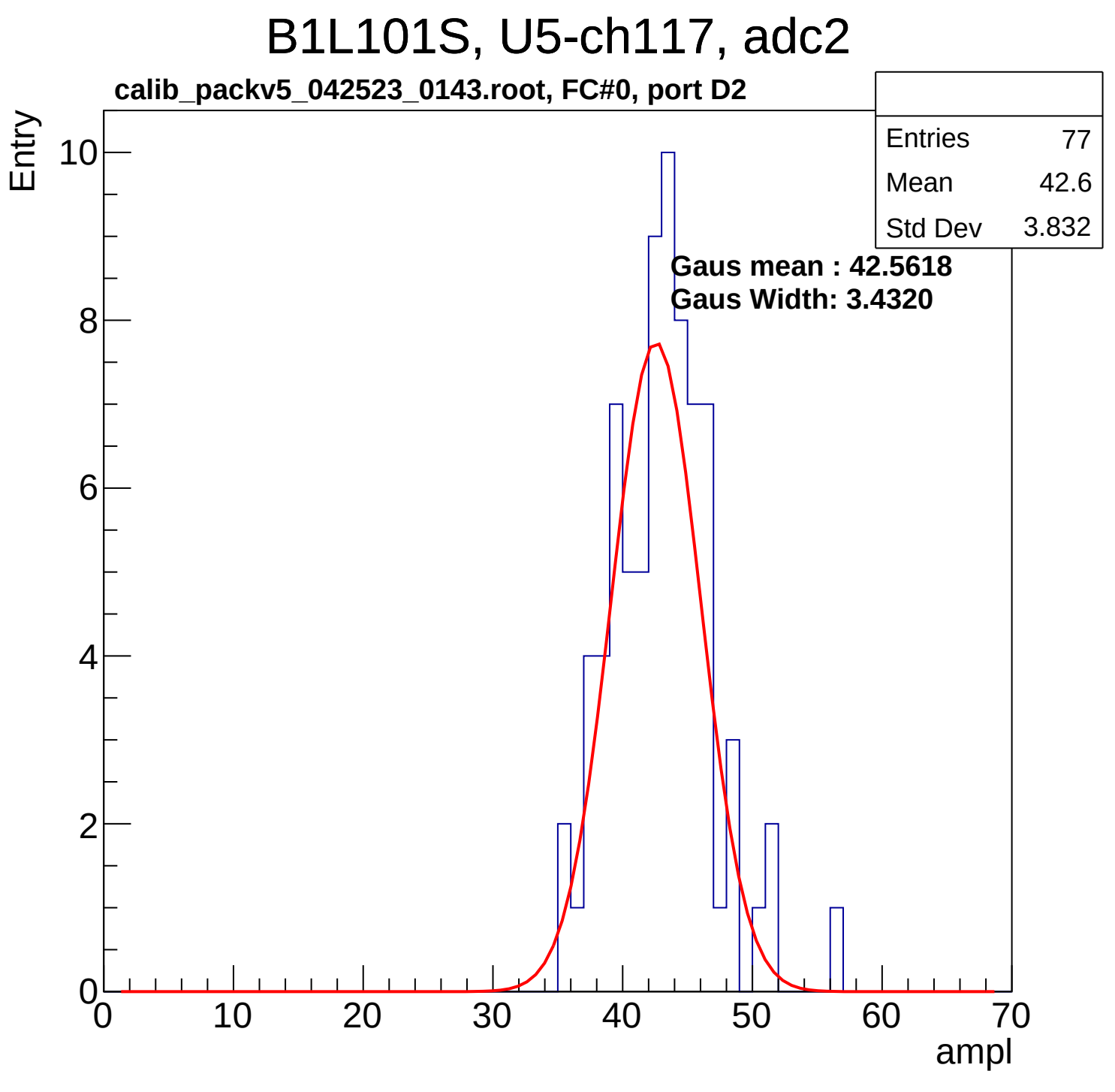
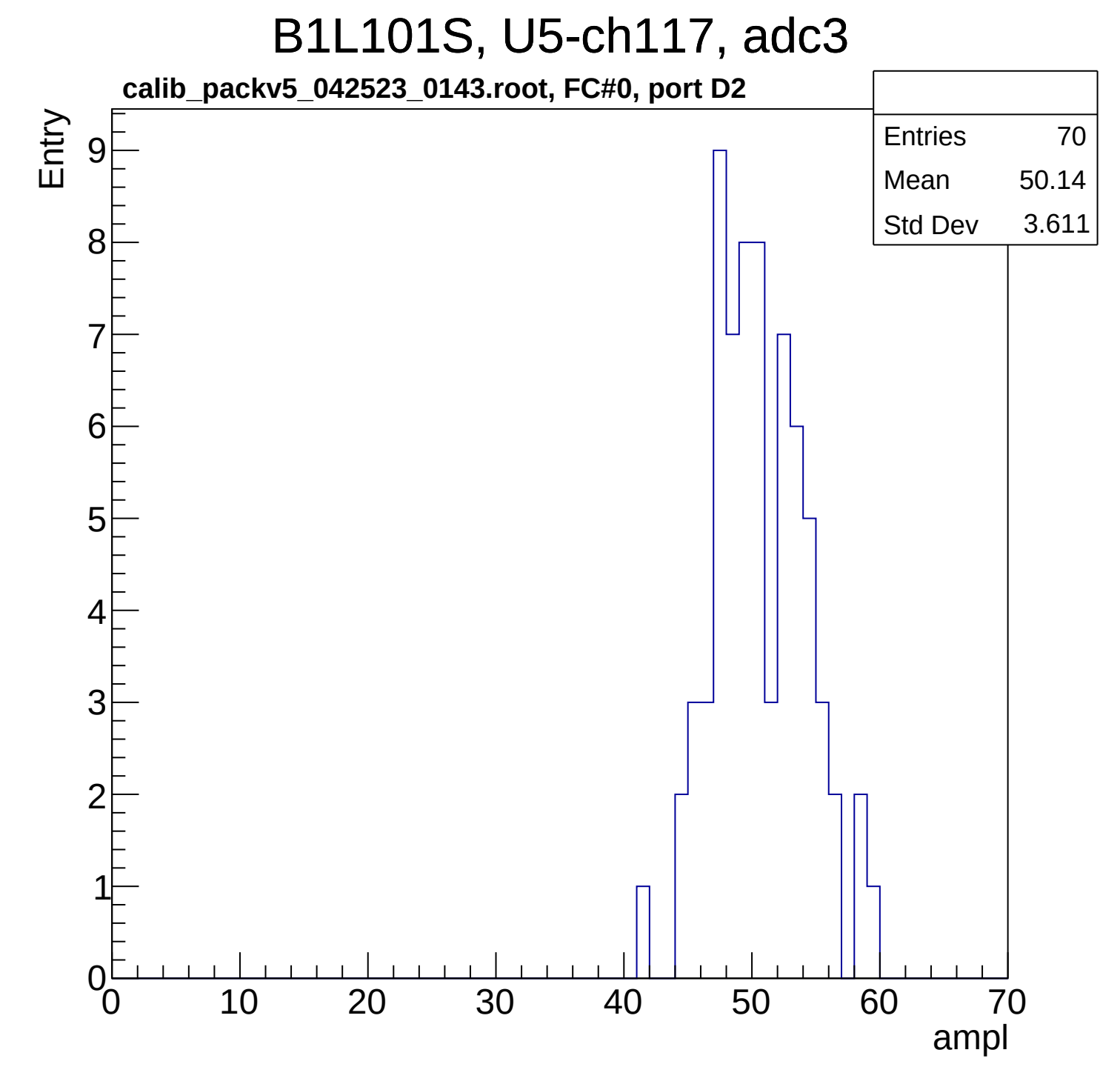

B1L101S, U5-ch117, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 42.6
Std Dev 3.832
Gaus mean : 42.5618
Gaus Width: 3.4320
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L101S, U5-ch117, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 50.14
Std Dev 3.611
Entry
ampl
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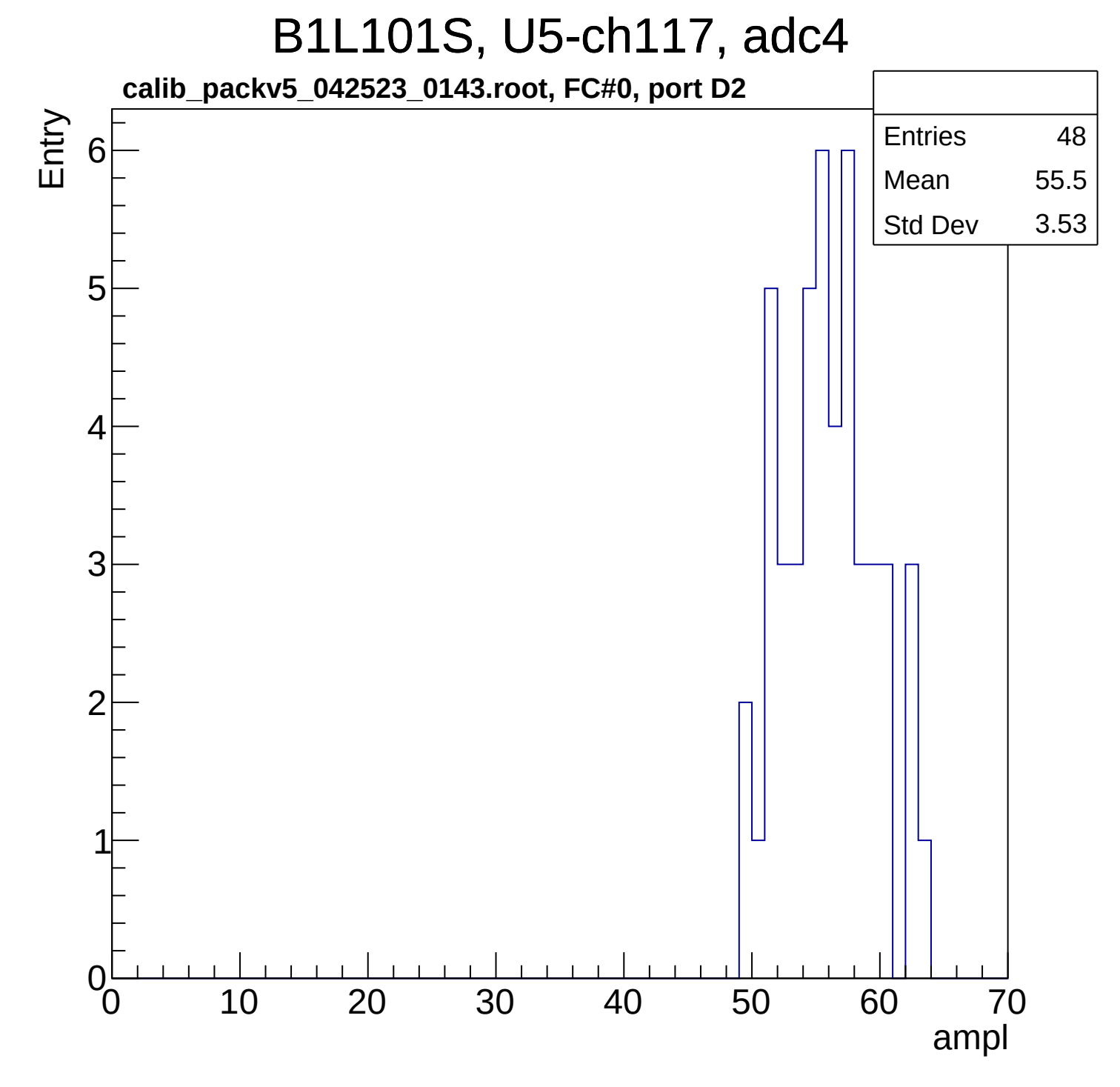
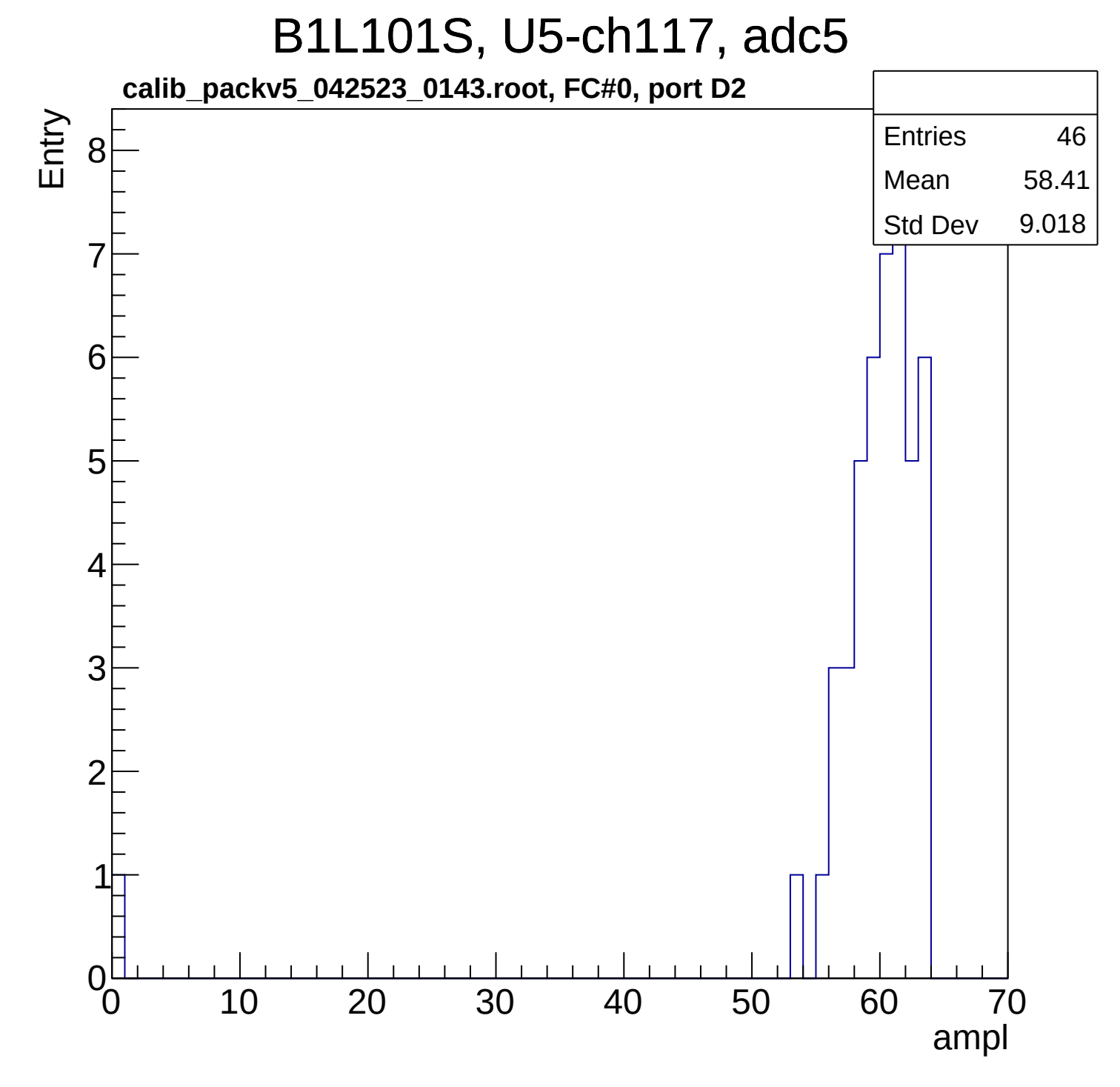
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch117, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 55.5
Std Dev 3.53
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch117, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 58.41
Std Dev 9.018
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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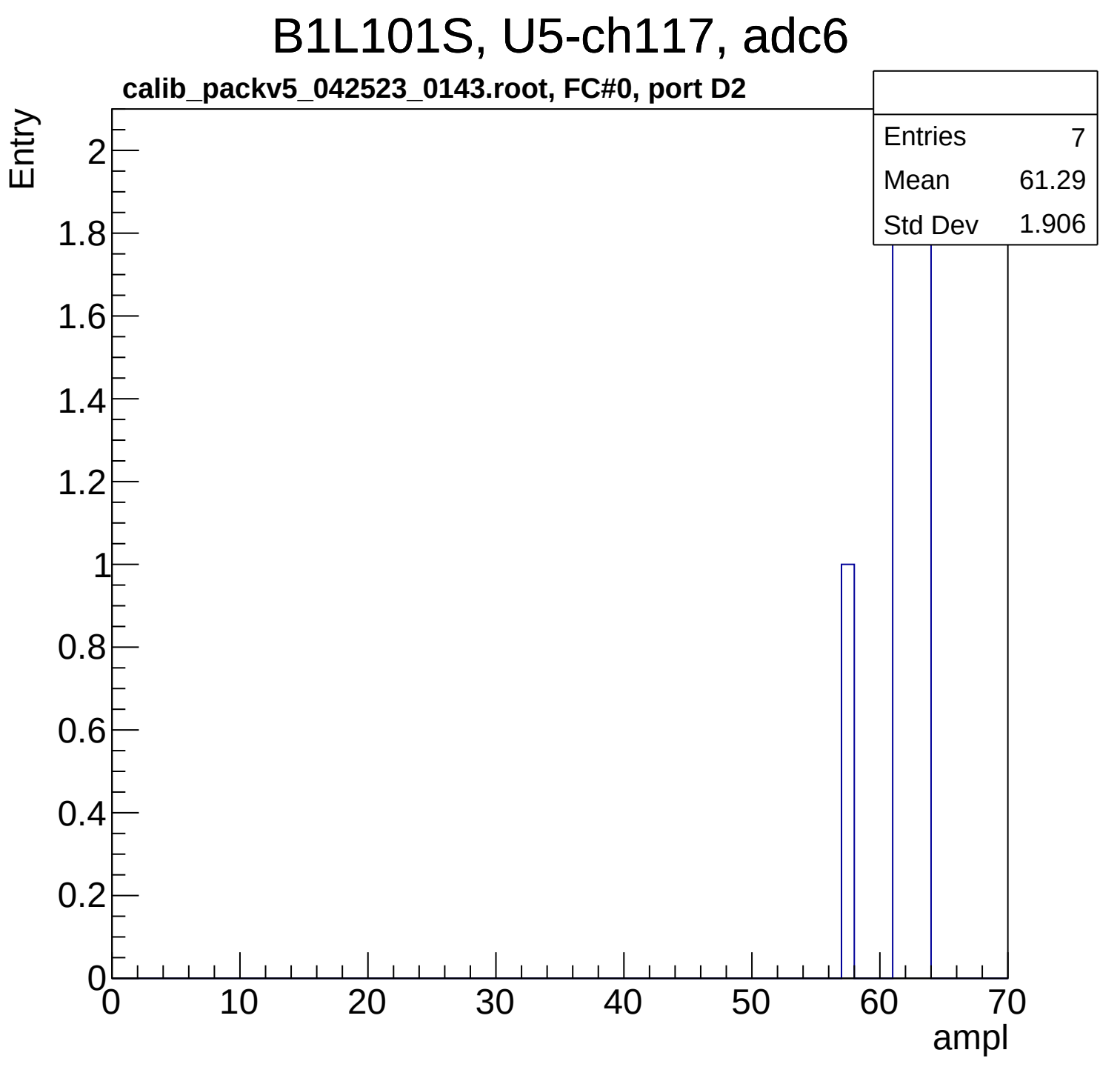
60
70


B1L101S, U5-ch117, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 61.29
Std Dev 1.906
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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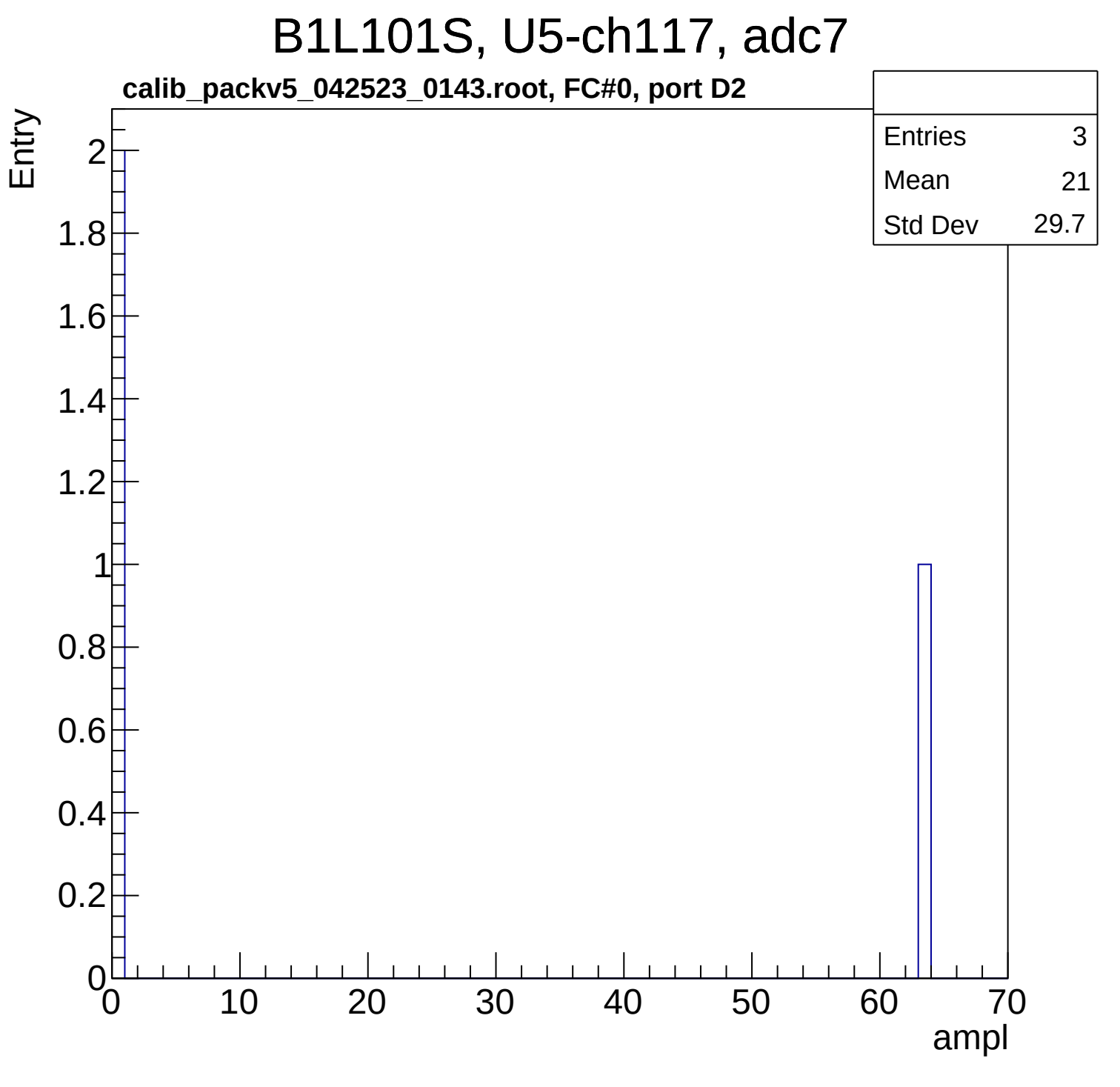
20
30
40
50
60
70


B1L101S, U5-ch117, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 21
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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20
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40
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60
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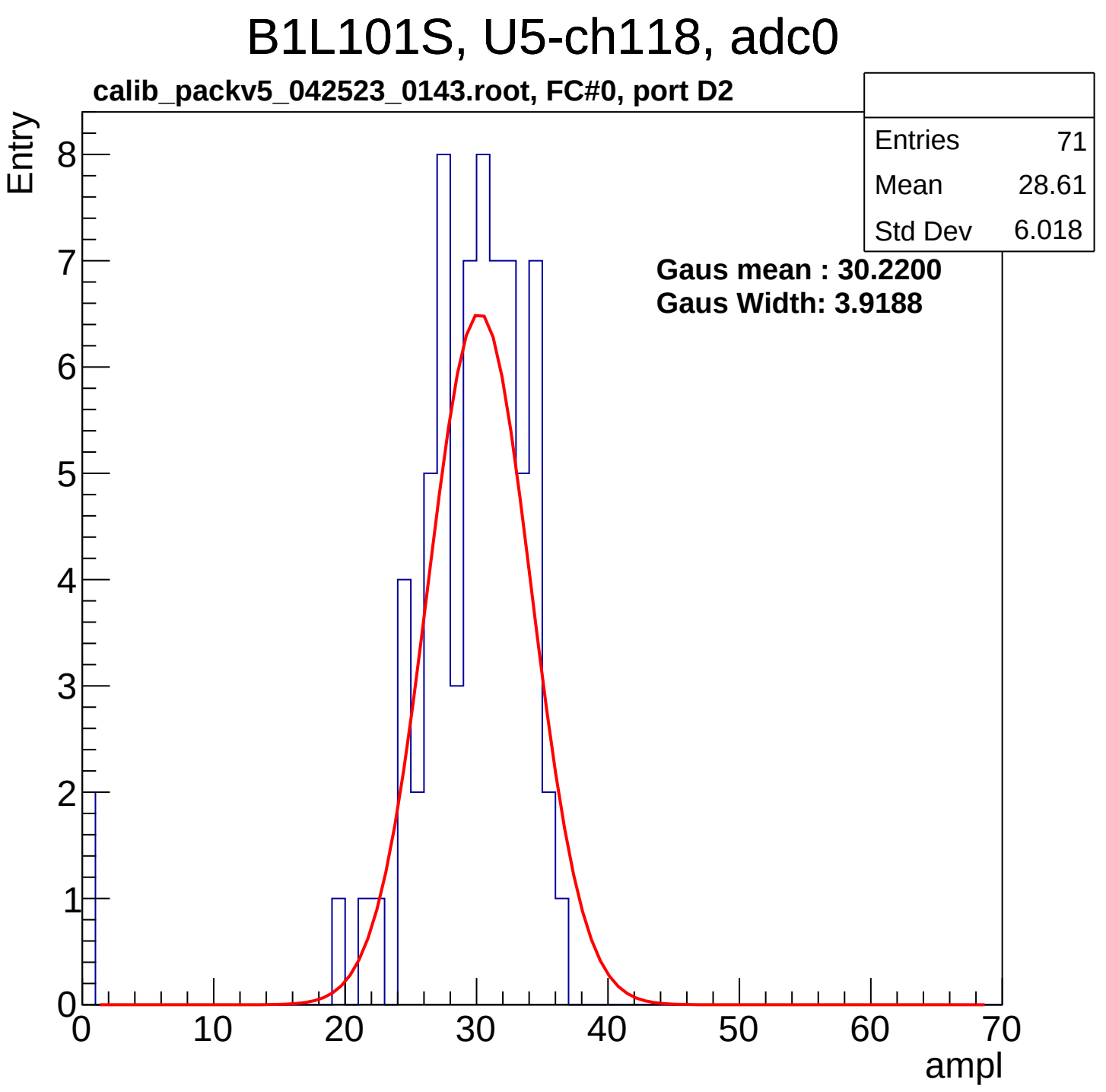
B1L101S, U5-ch118, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 28.61
Std Dev 6.018
Gaus mean : 30.2200
Gaus Width: 3.9188
Entry
ampl
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1
2
3
4
5
6
7
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0
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60
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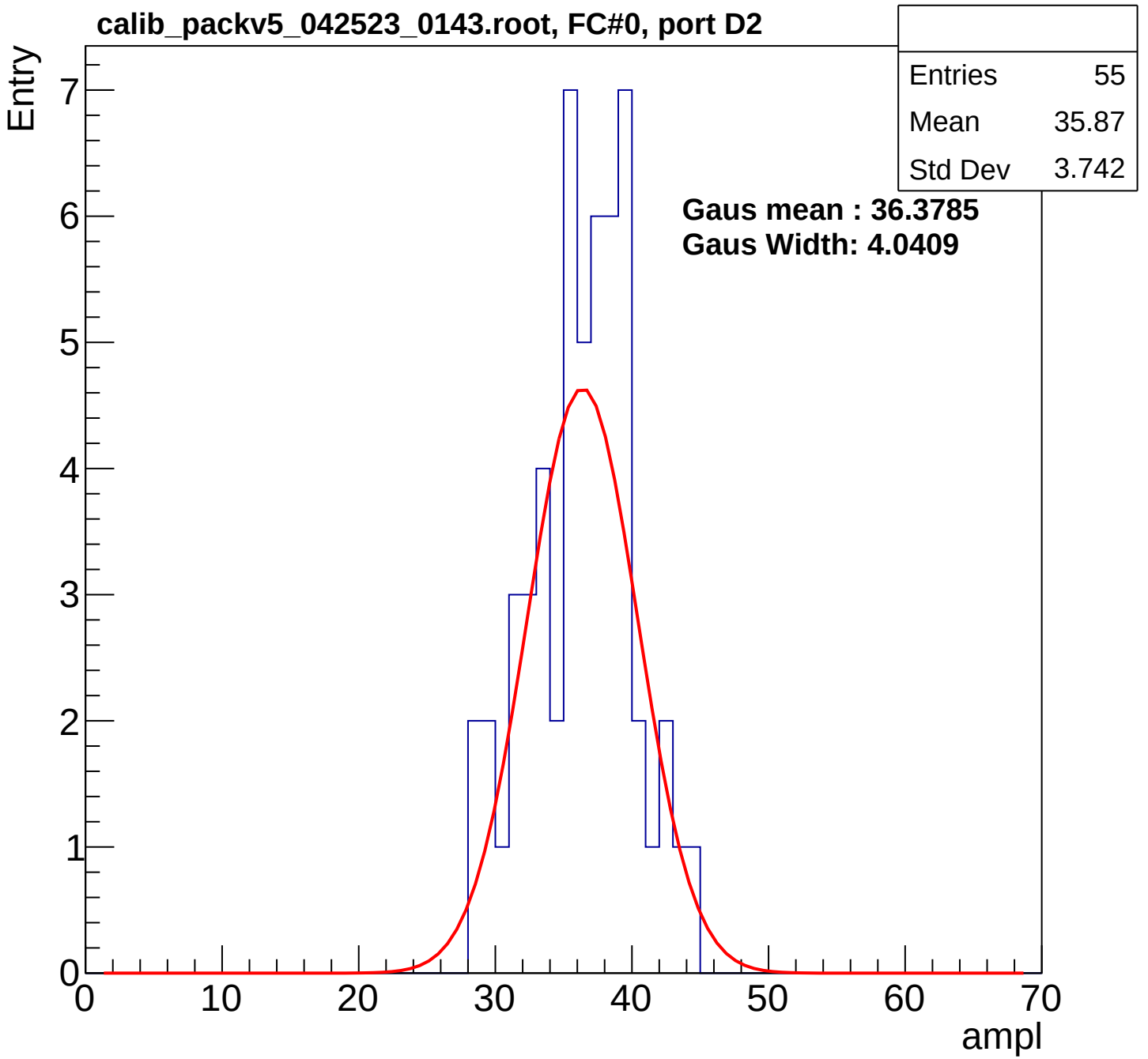
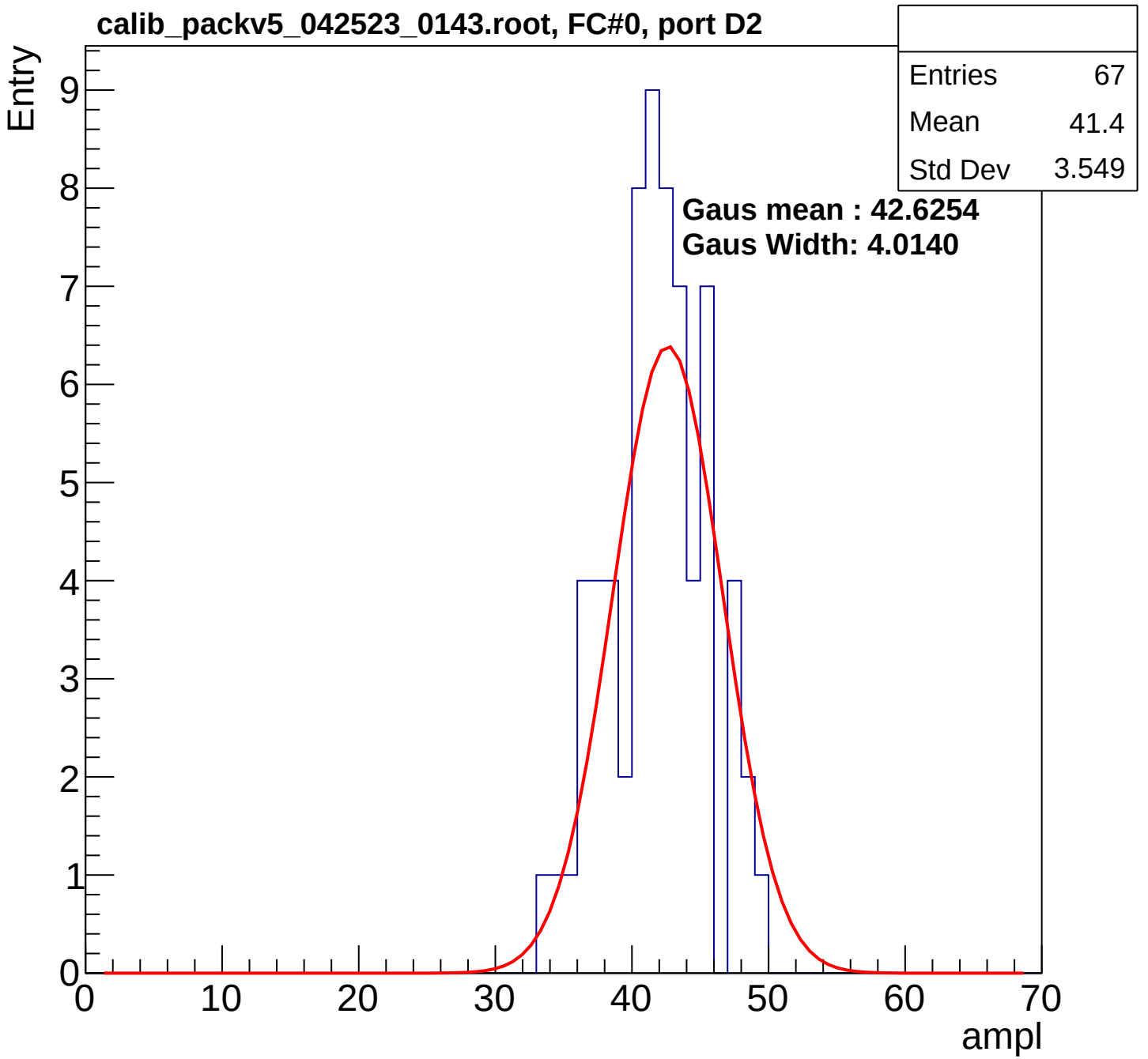

B1L101S, U5-ch118, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 35.87
Std Dev 3.742
Gaus mean : 36.3785
Gaus Width: 4.0409
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch118, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 41.4
Std Dev 3.549
Gaus mean : 42.6254
Gaus Width: 4.0140
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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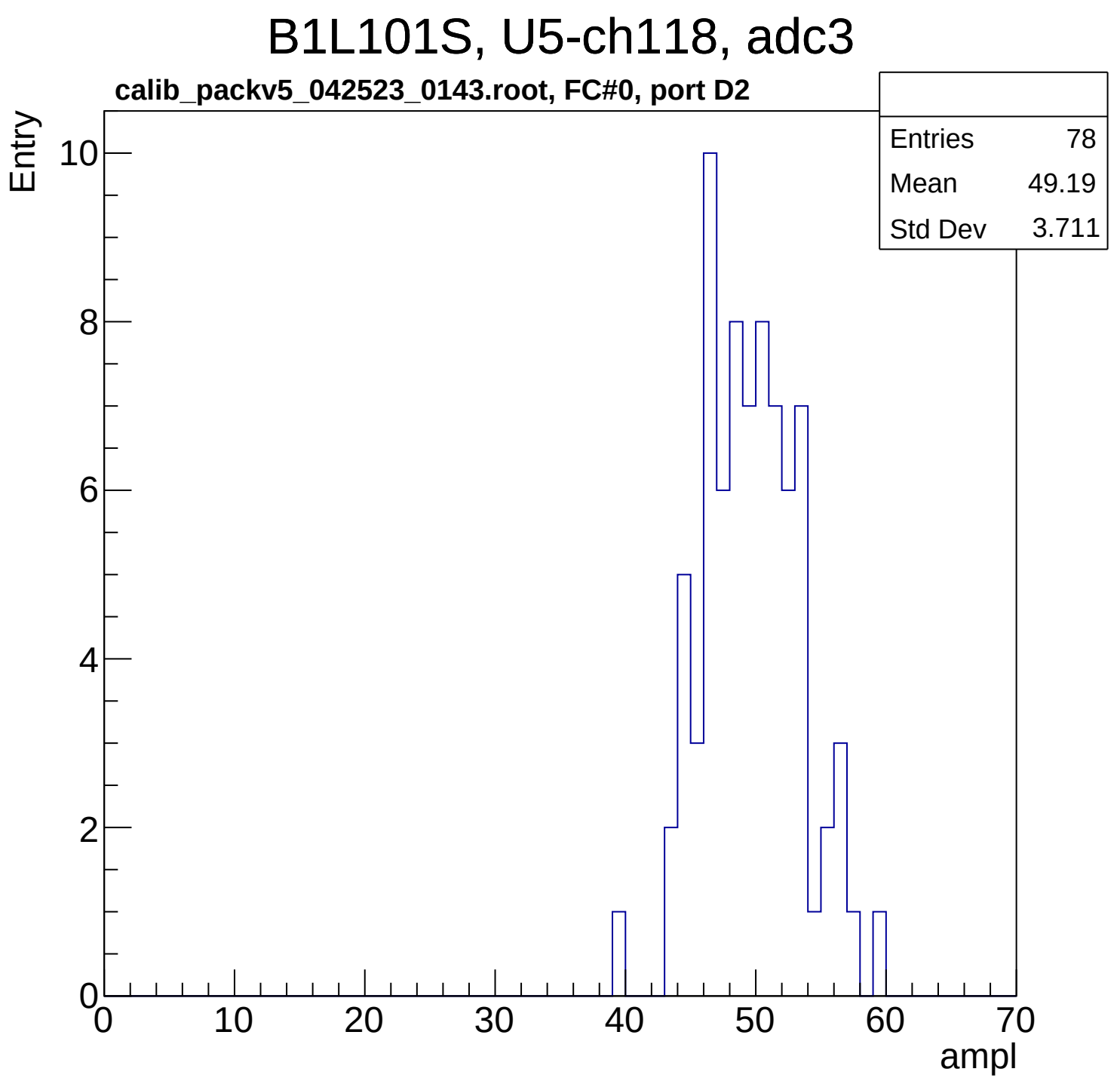
B1L101S, U5-ch118, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 49.19
Std Dev 3.711
Entry
0
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4
6
8
10
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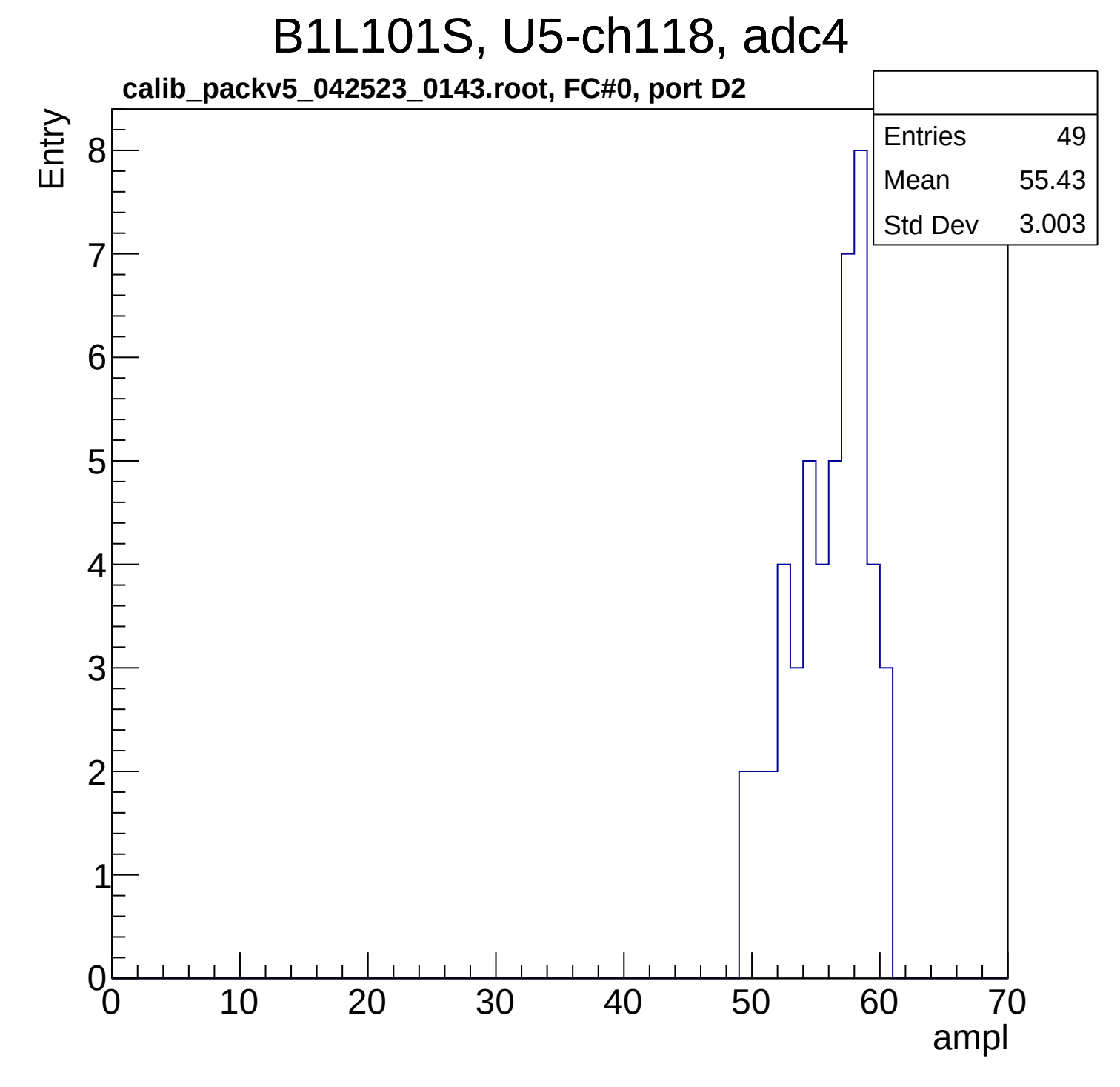
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch118, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 55.43
Std Dev 3.003
Entry
ampl
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5
6
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0
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20
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40
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60
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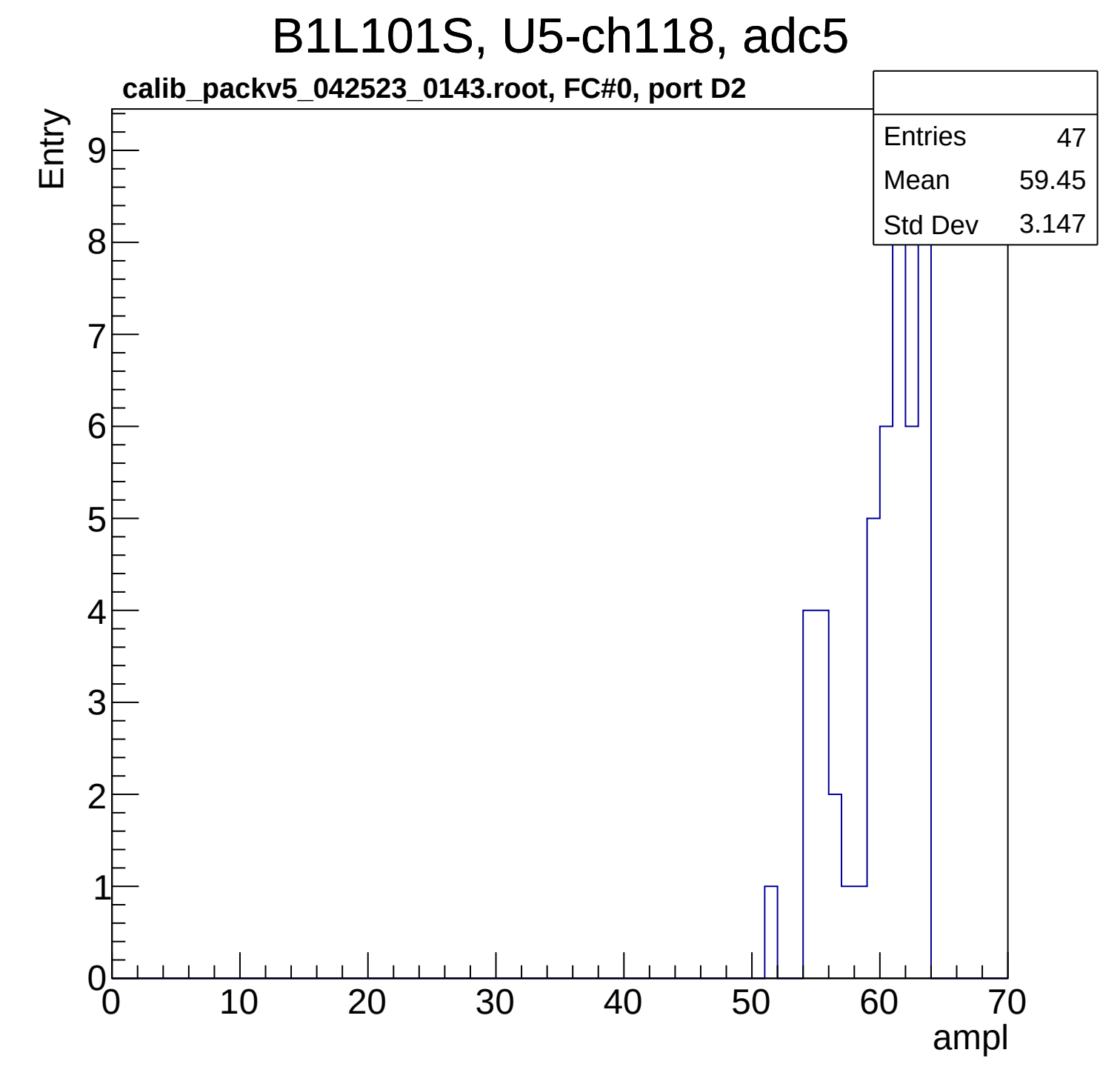
B1L101S, U5-ch118, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 59.45
Std Dev 3.147
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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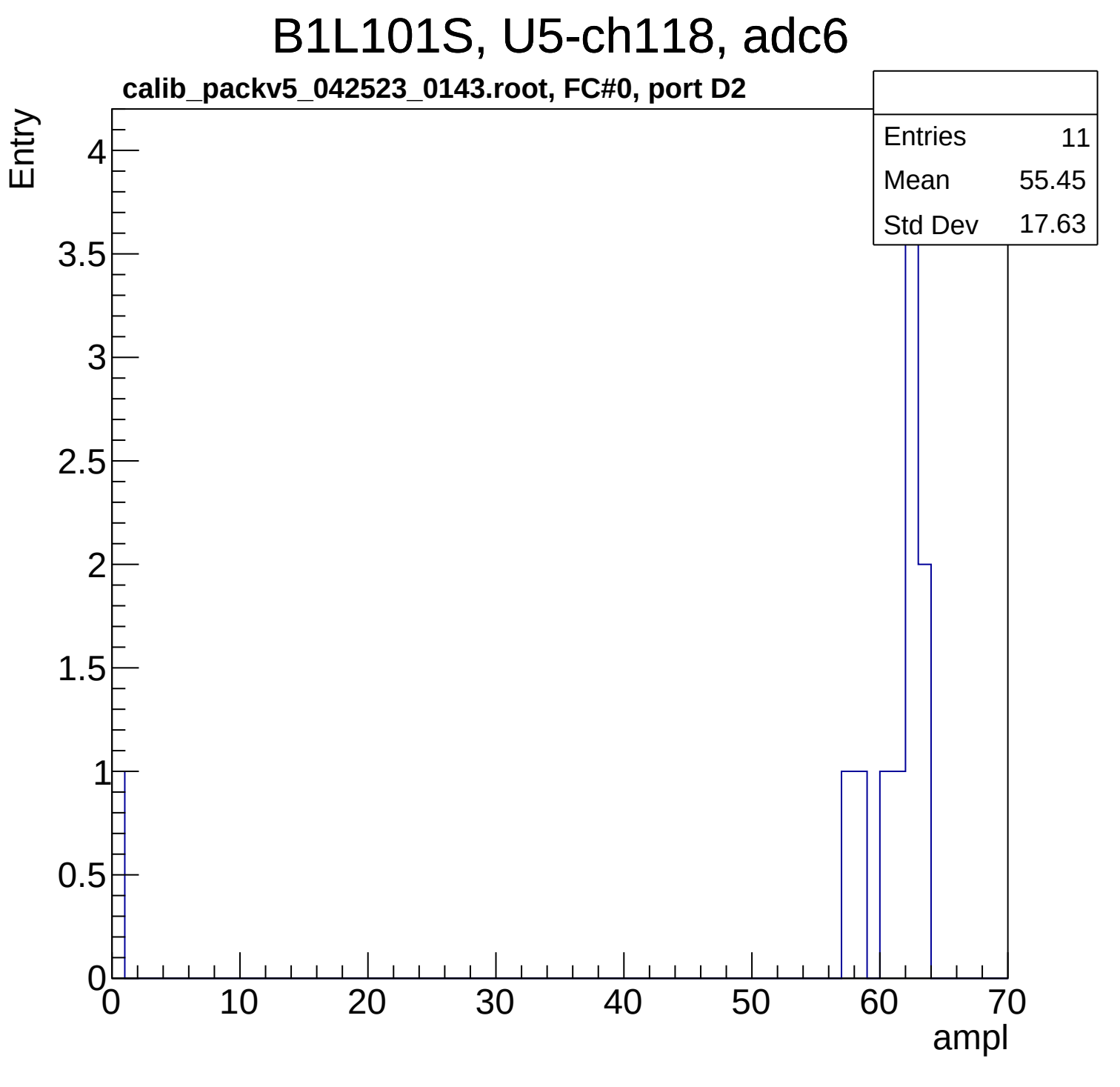
40
50
60
70


B1L101S, U5-ch118, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 11
Mean 55.45
Std Dev 17.63
Entry
ampl
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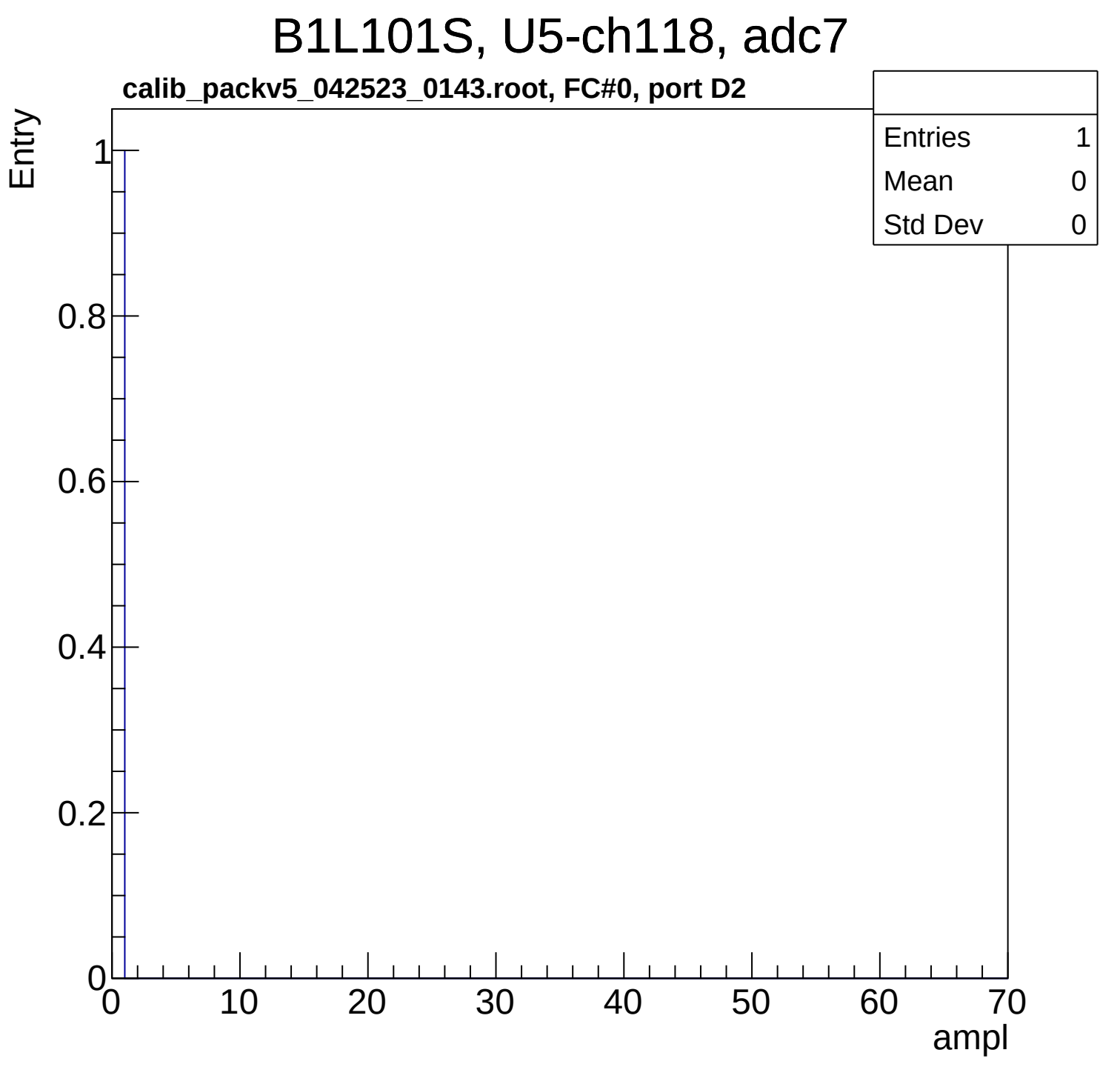
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L101S, U5-ch118, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
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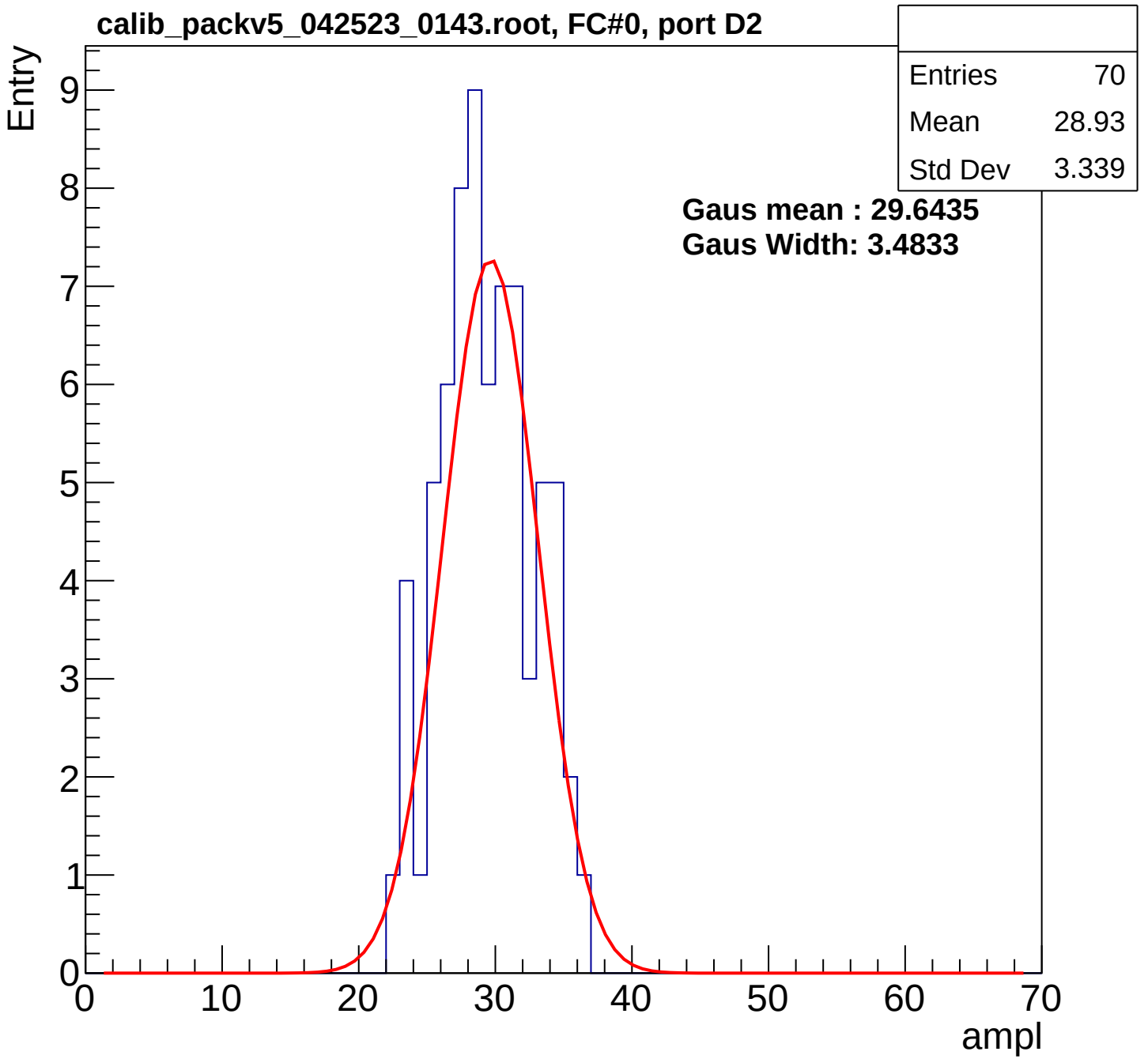
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch119, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 28.93
Std Dev 3.339
Gaus mean : 29.6435
Gaus Width: 3.4833
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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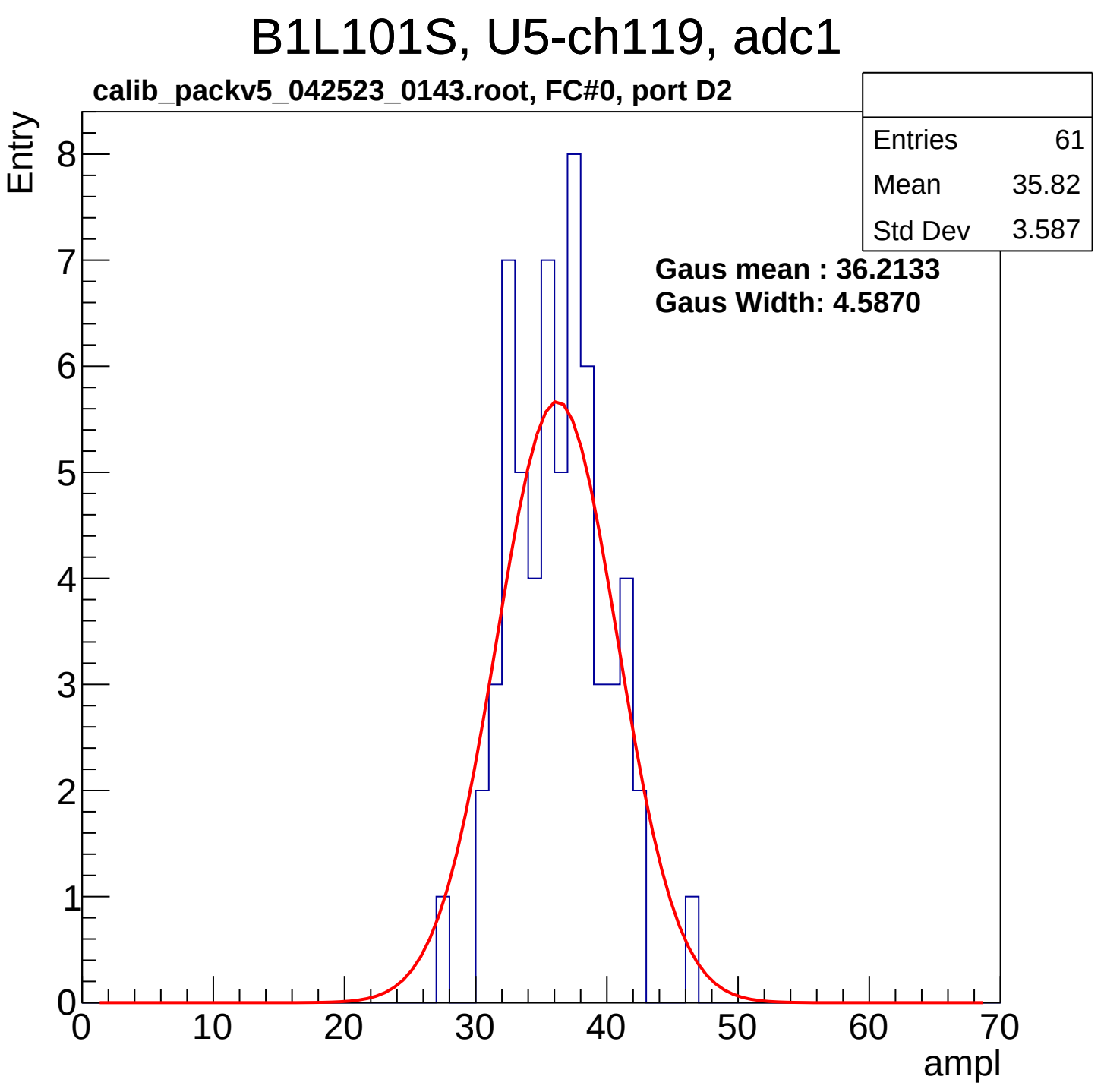
B1L101S, U5-ch119, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 35.82
Std Dev 3.587
Gaus mean : 36.2133
Gaus Width: 4.5870
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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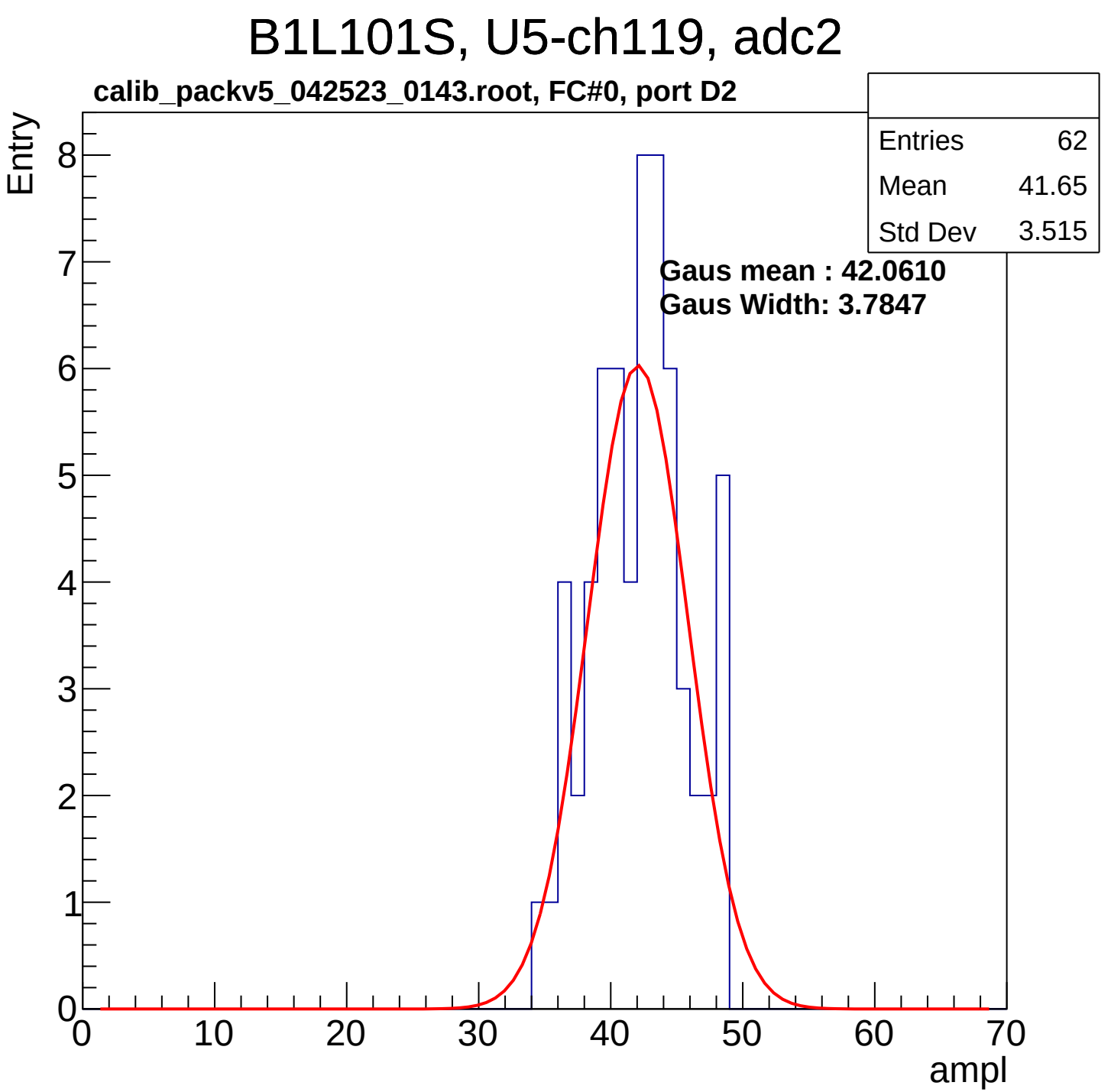
40
50
60
70


B1L101S, U5-ch119, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 41.65
Std Dev 3.515
Gaus mean : 42.0610
Gaus Width: 3.7847
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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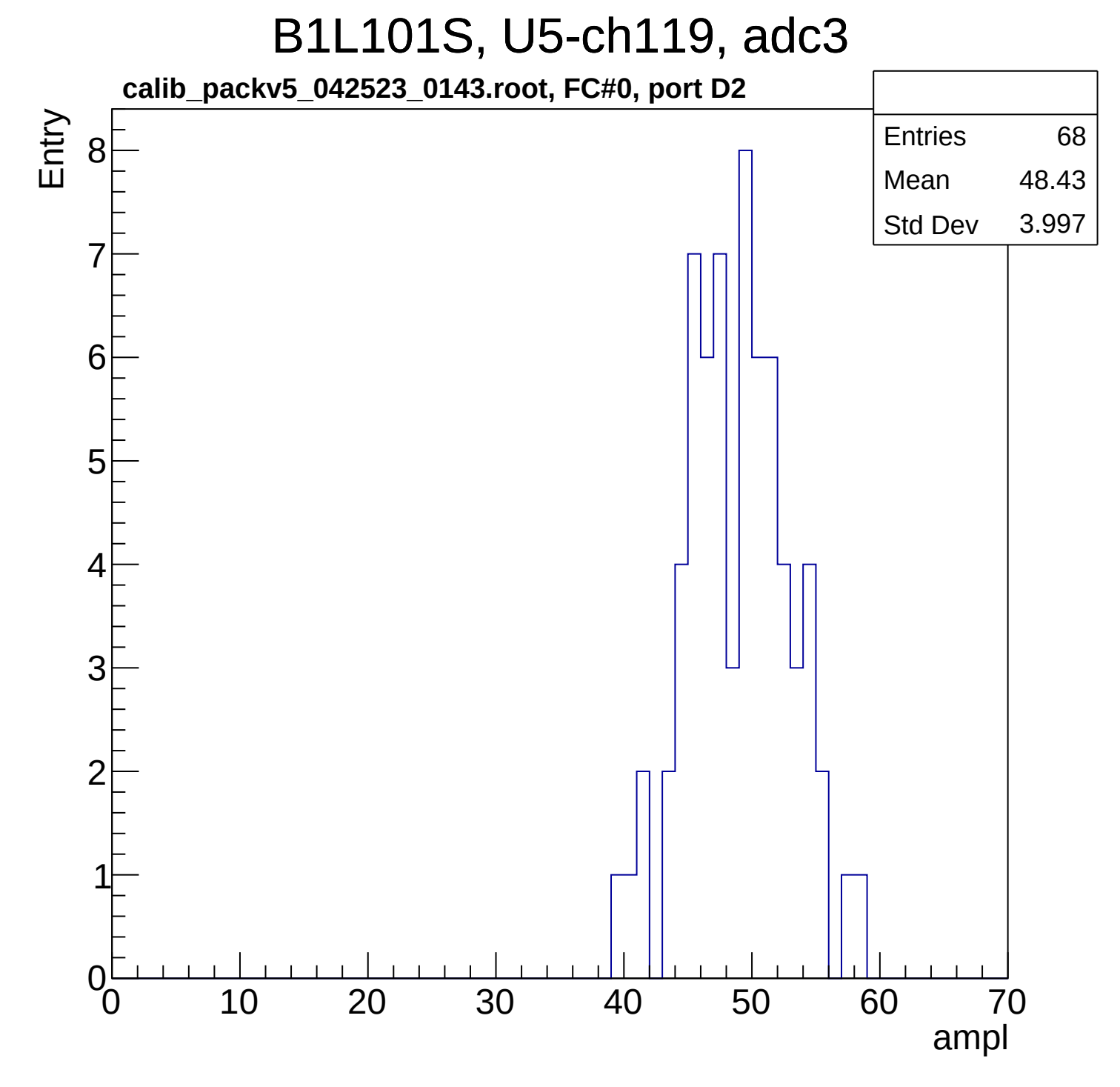
40
50
60
70


B1L101S, U5-ch119, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 48.43
Std Dev 3.997
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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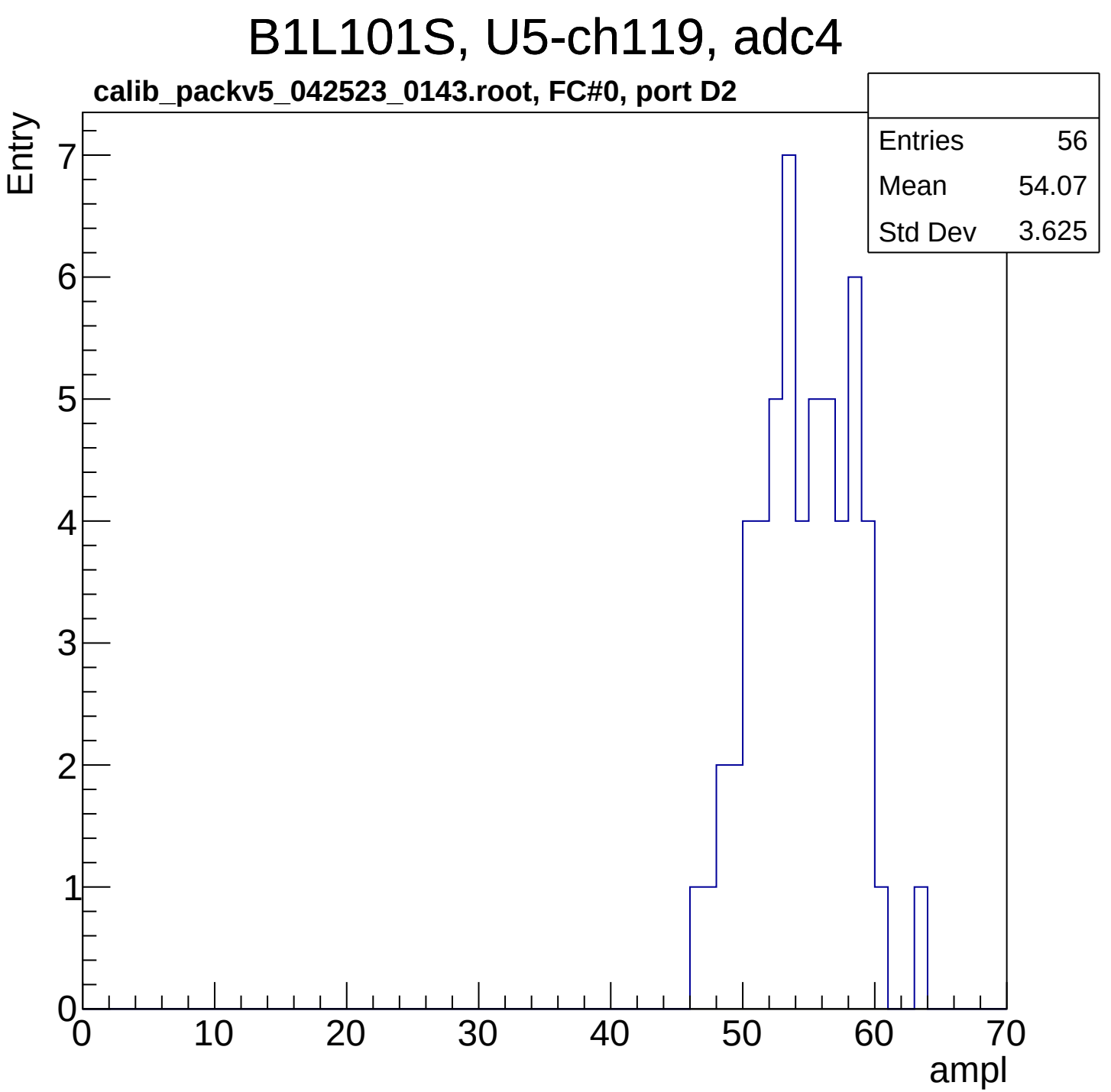
B1L101S, U5-ch119, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 54.07
Std Dev 3.625
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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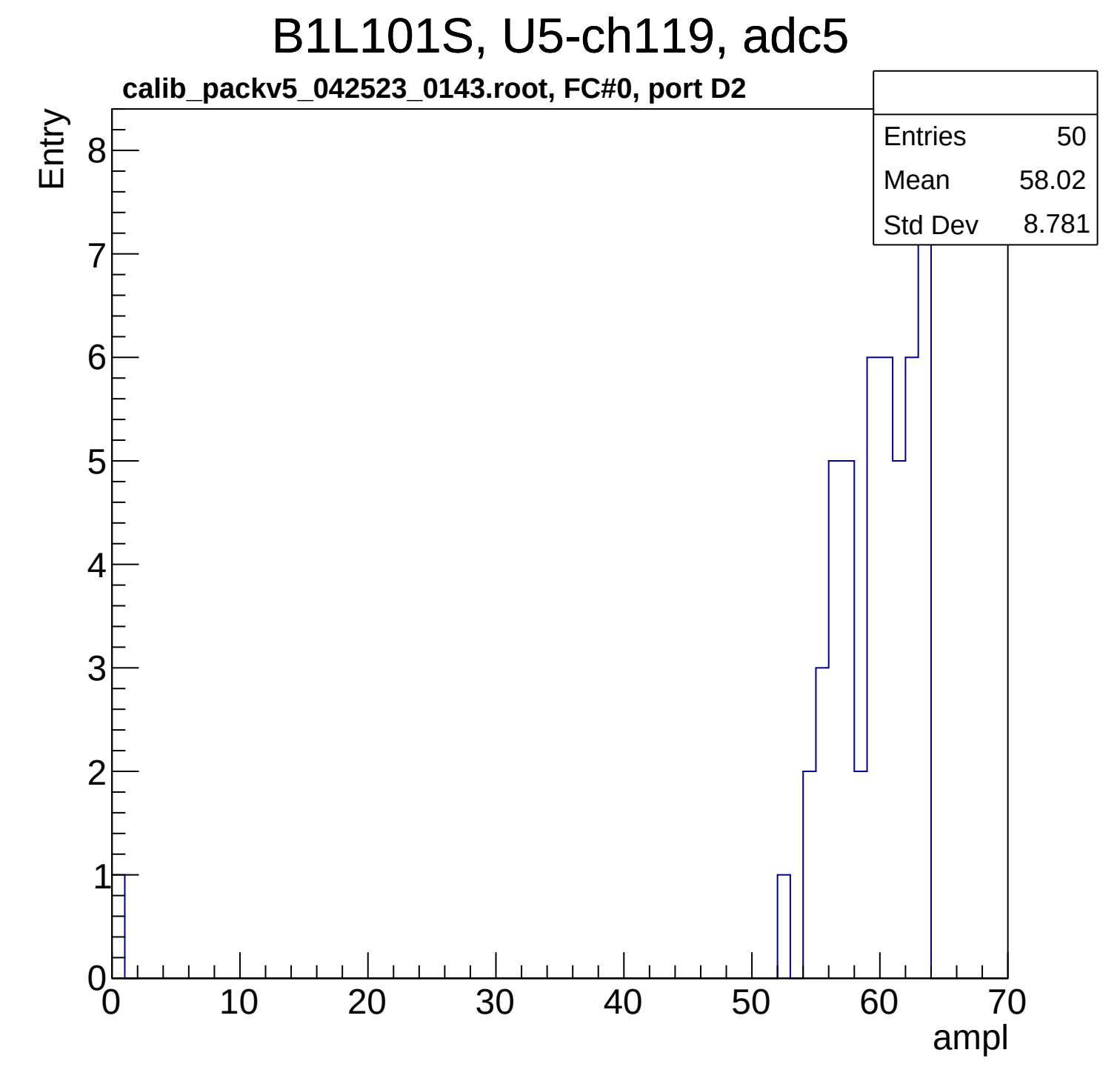
B1L101S, U5-ch119, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 58.02
Std Dev 8.781
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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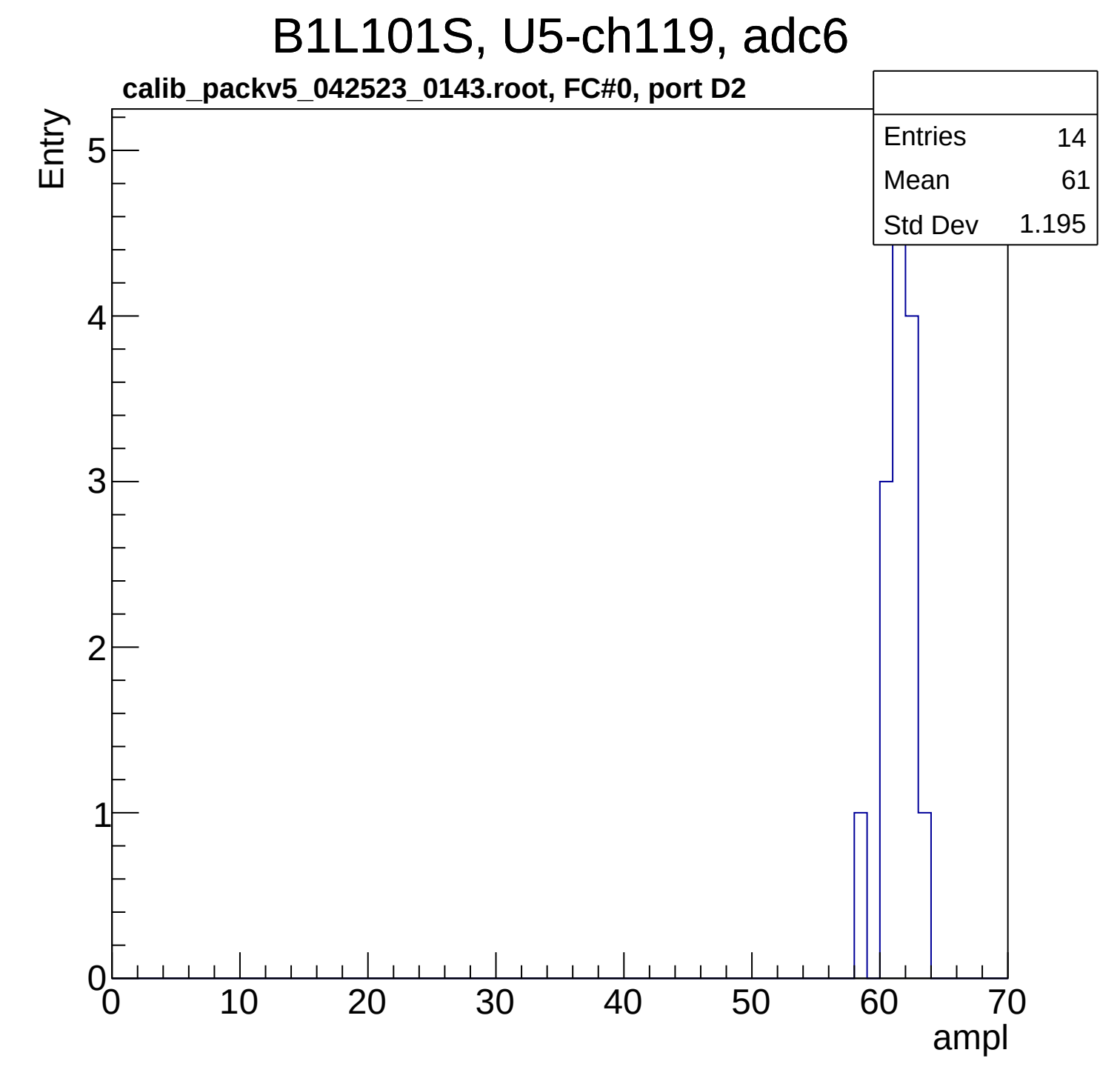
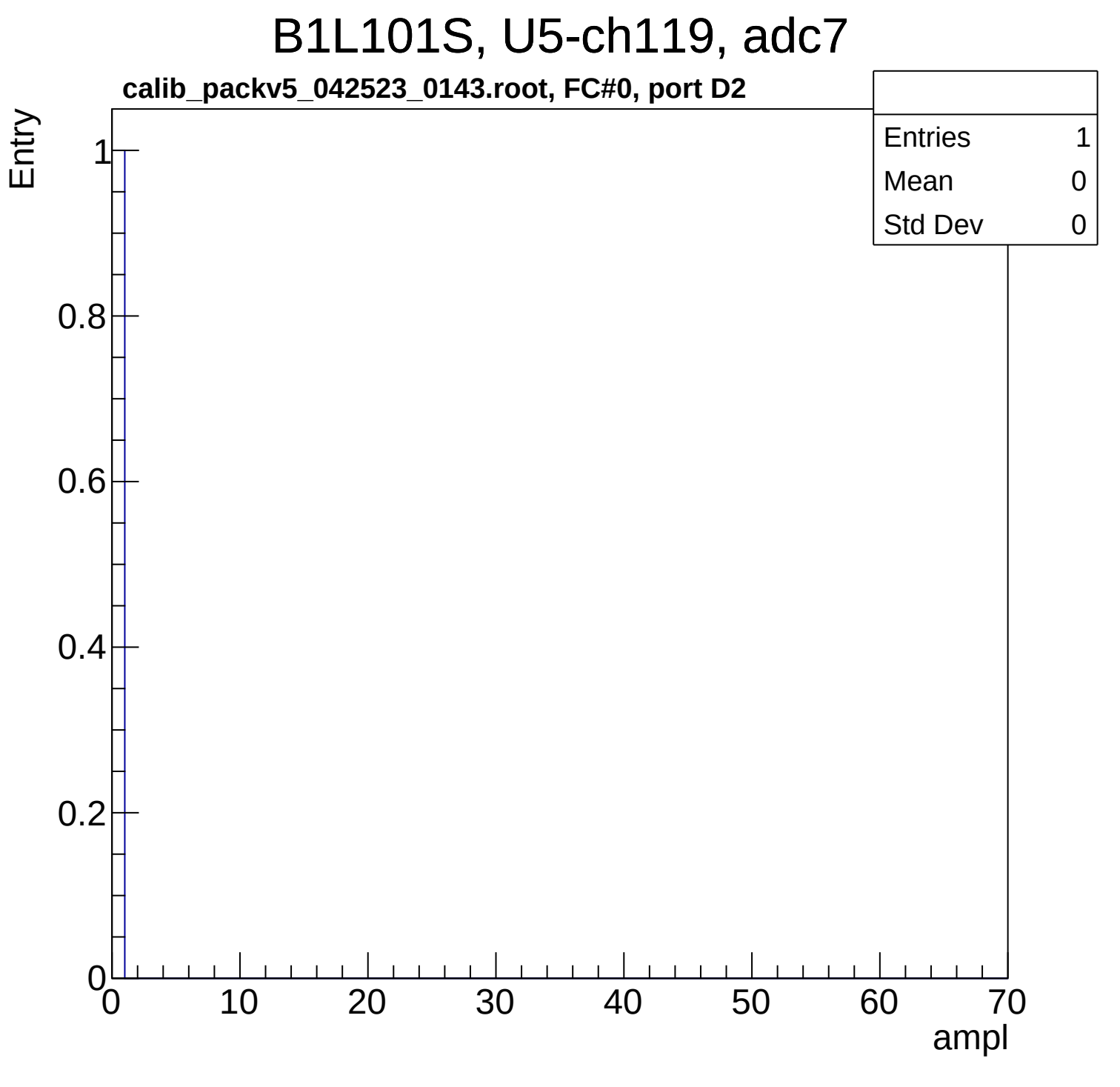
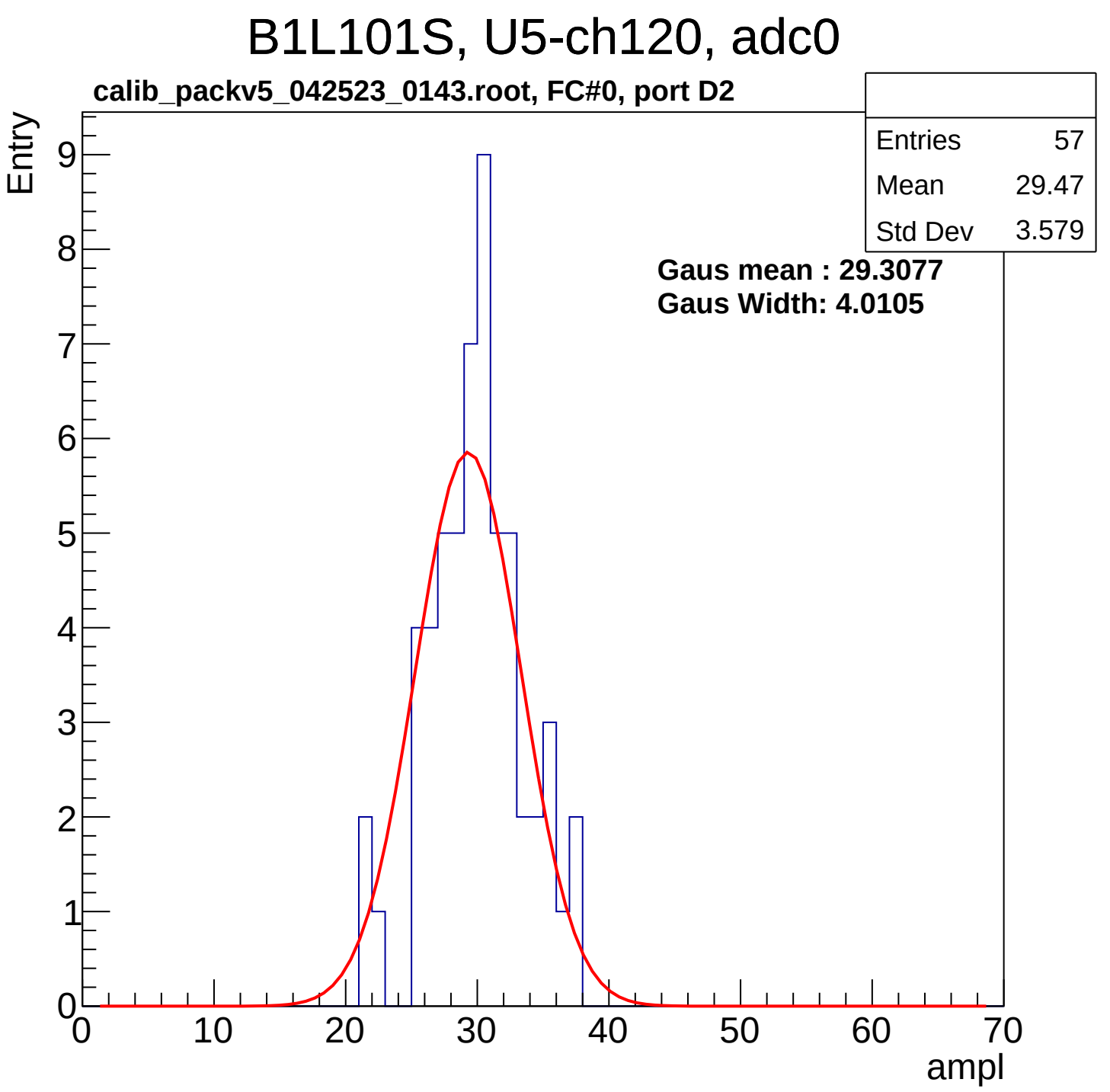
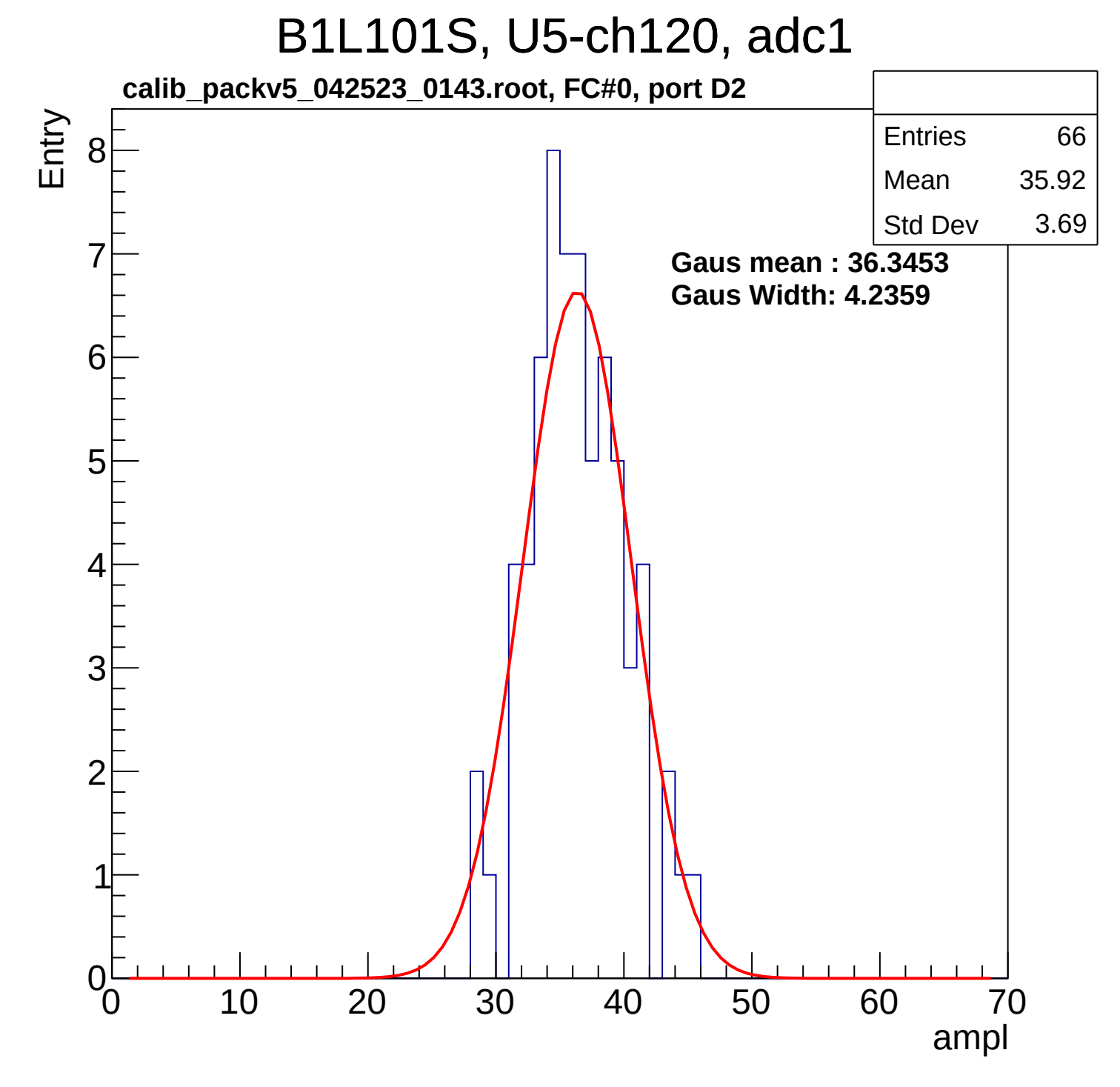

B1L101S, U5-ch119, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 14
Mean 61
Std Dev 1.195
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch119, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch120, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 29.47
Std Dev 3.579
Gaus mean : 29.3077
Gaus Width: 4.0105
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch120, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 35.92
Std Dev 3.69
Gaus mean : 36.3453
Gaus Width: 4.2359
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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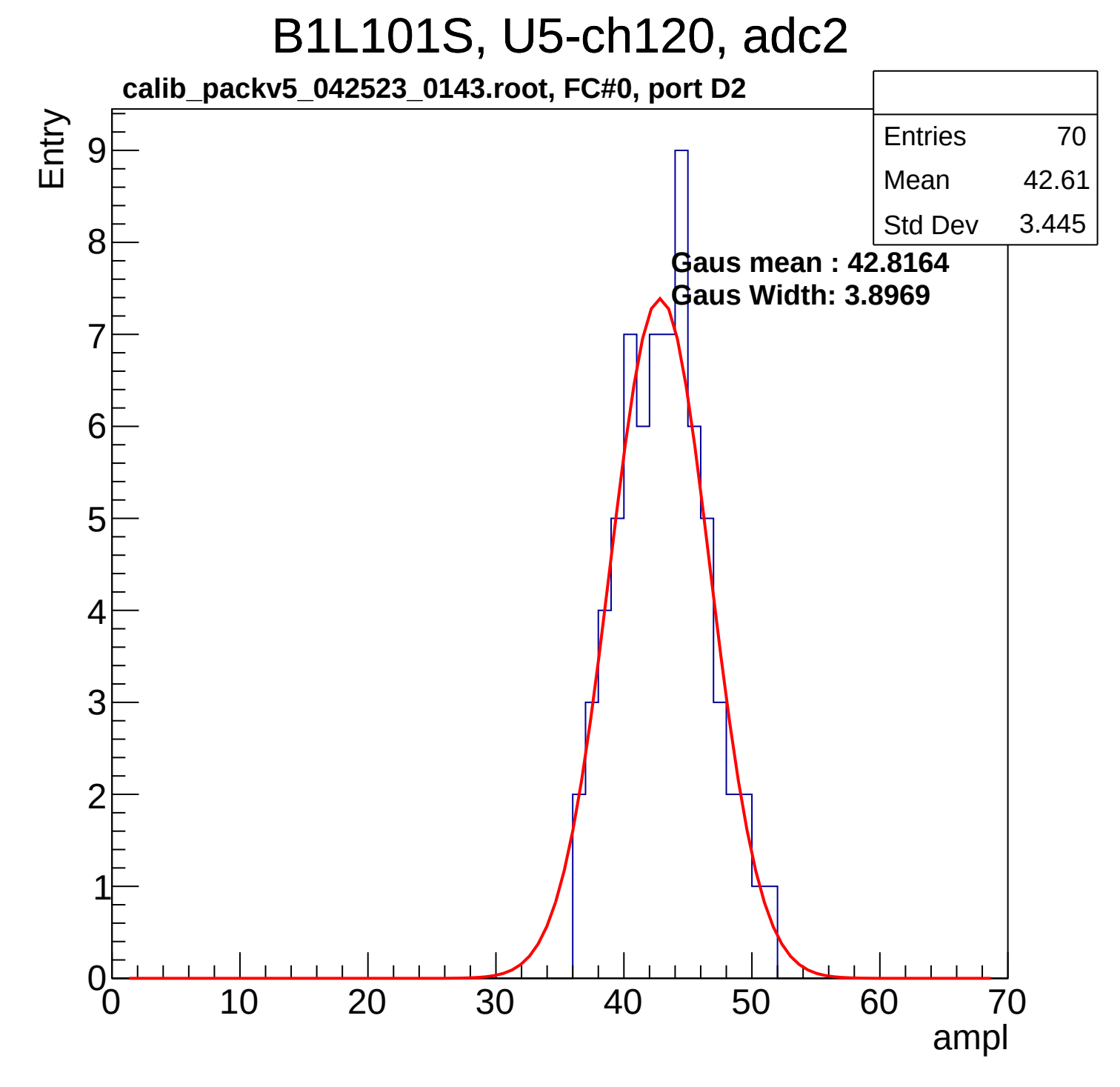
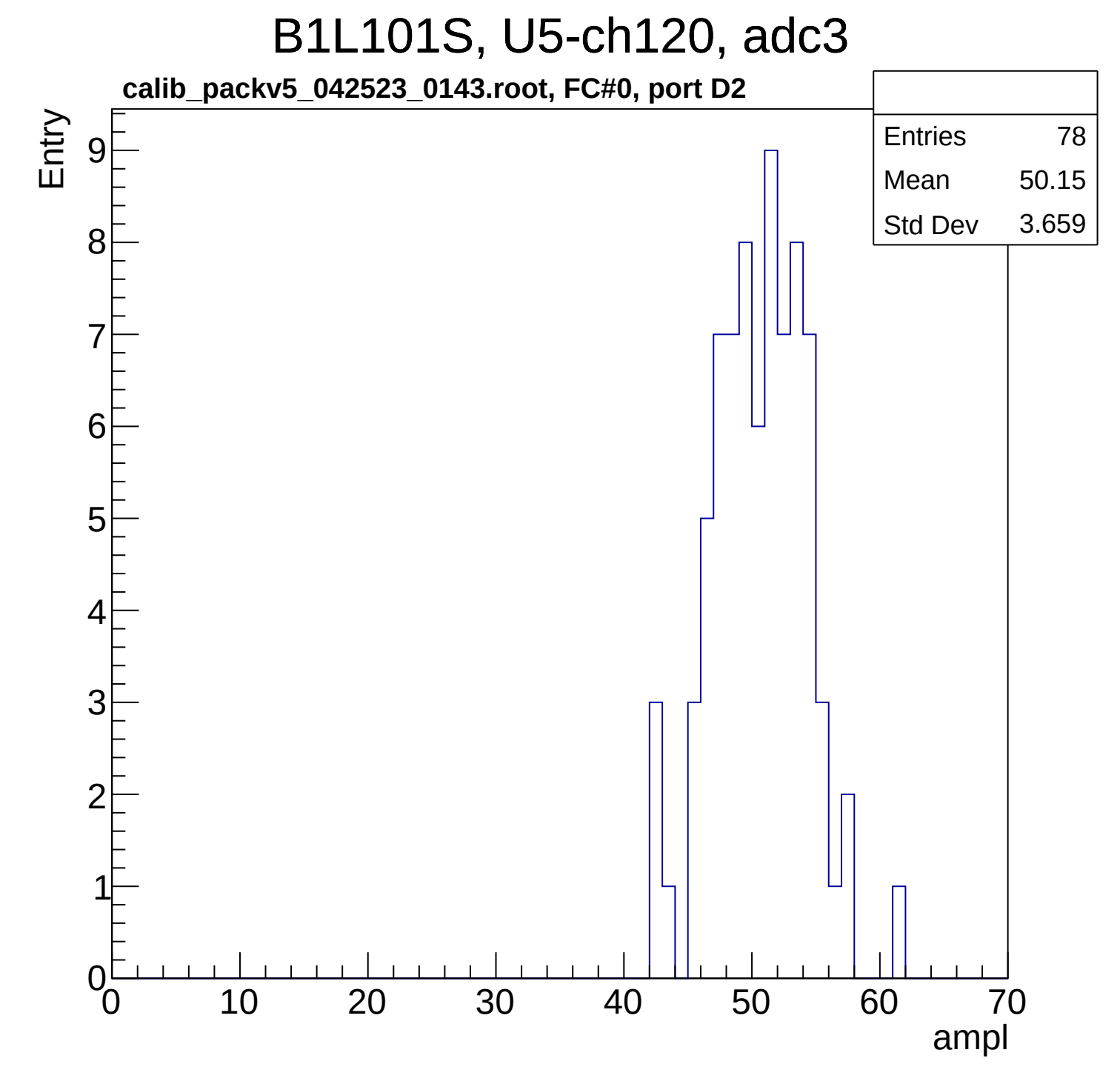
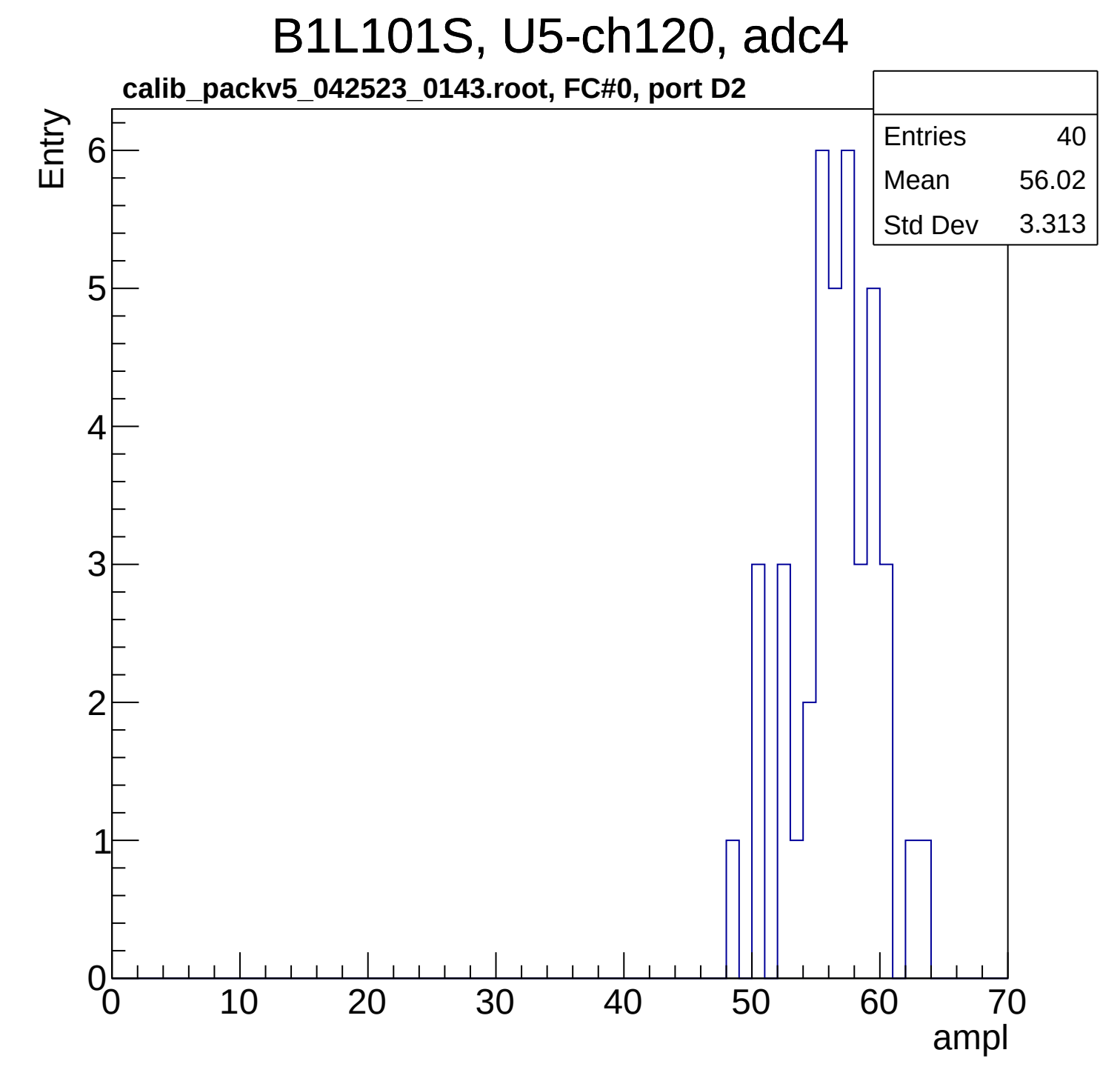
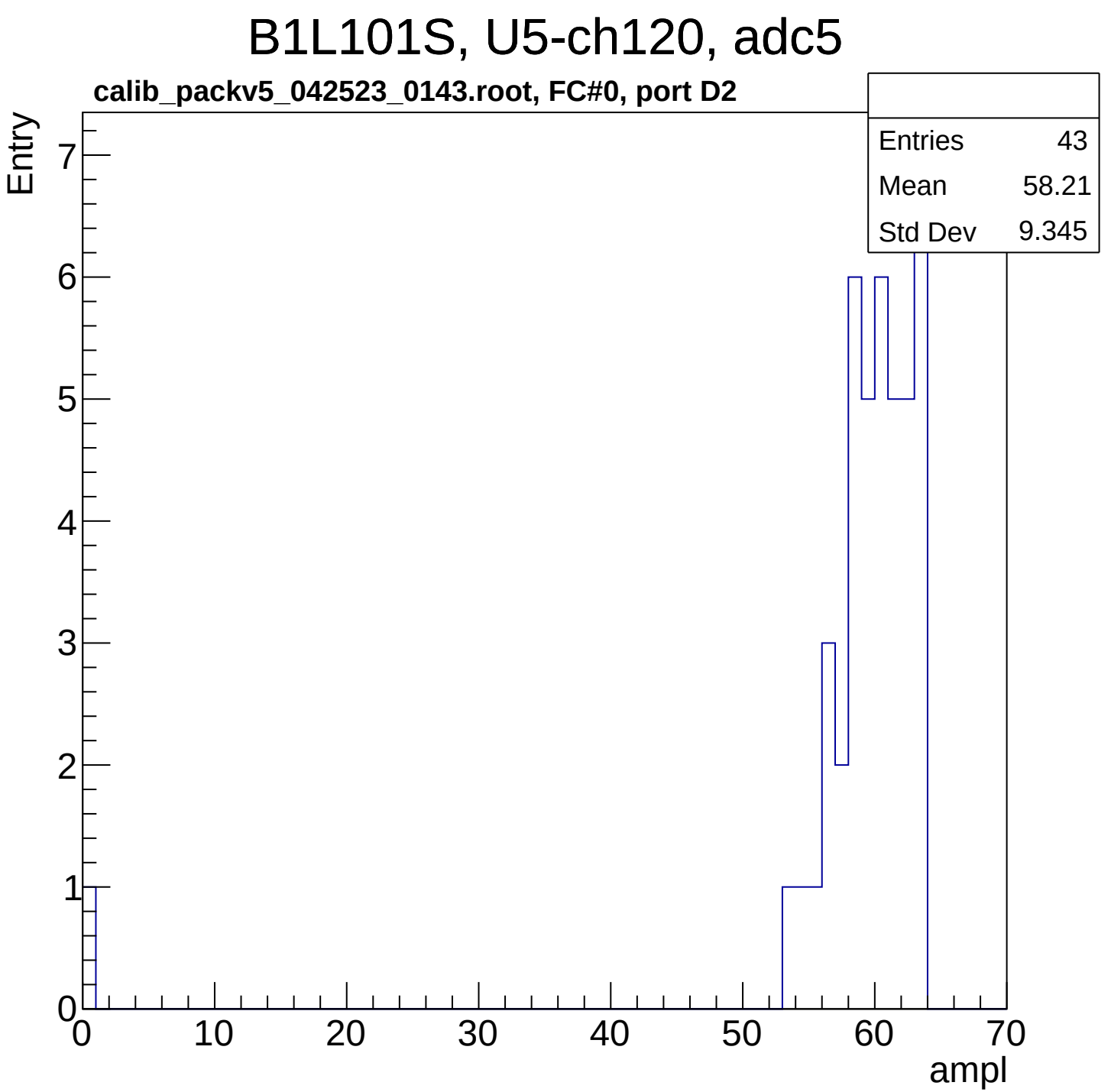
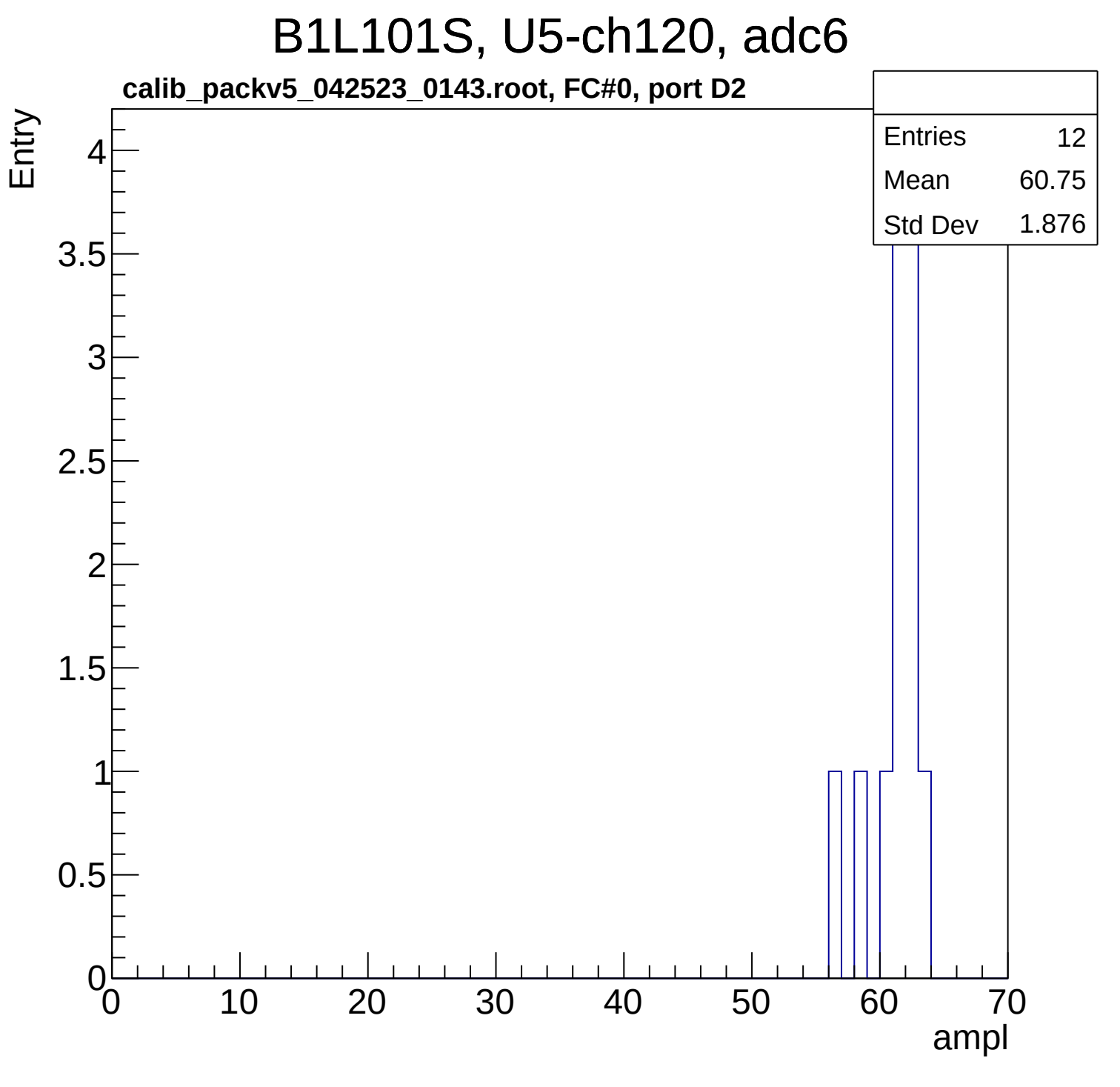

B1L101S, U5-ch120, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 42.61
Std Dev 3.445
Gaus mean : 42.8164
Gaus Width: 3.8969
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch120, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 50.15
Std Dev 3.659
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch120, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 40
Mean 56.02
Std Dev 3.313
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L101S, U5-ch120, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 43
Mean 58.21
Std Dev 9.345
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch120, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 12
Mean 60.75
Std Dev 1.876
Entry
ampl
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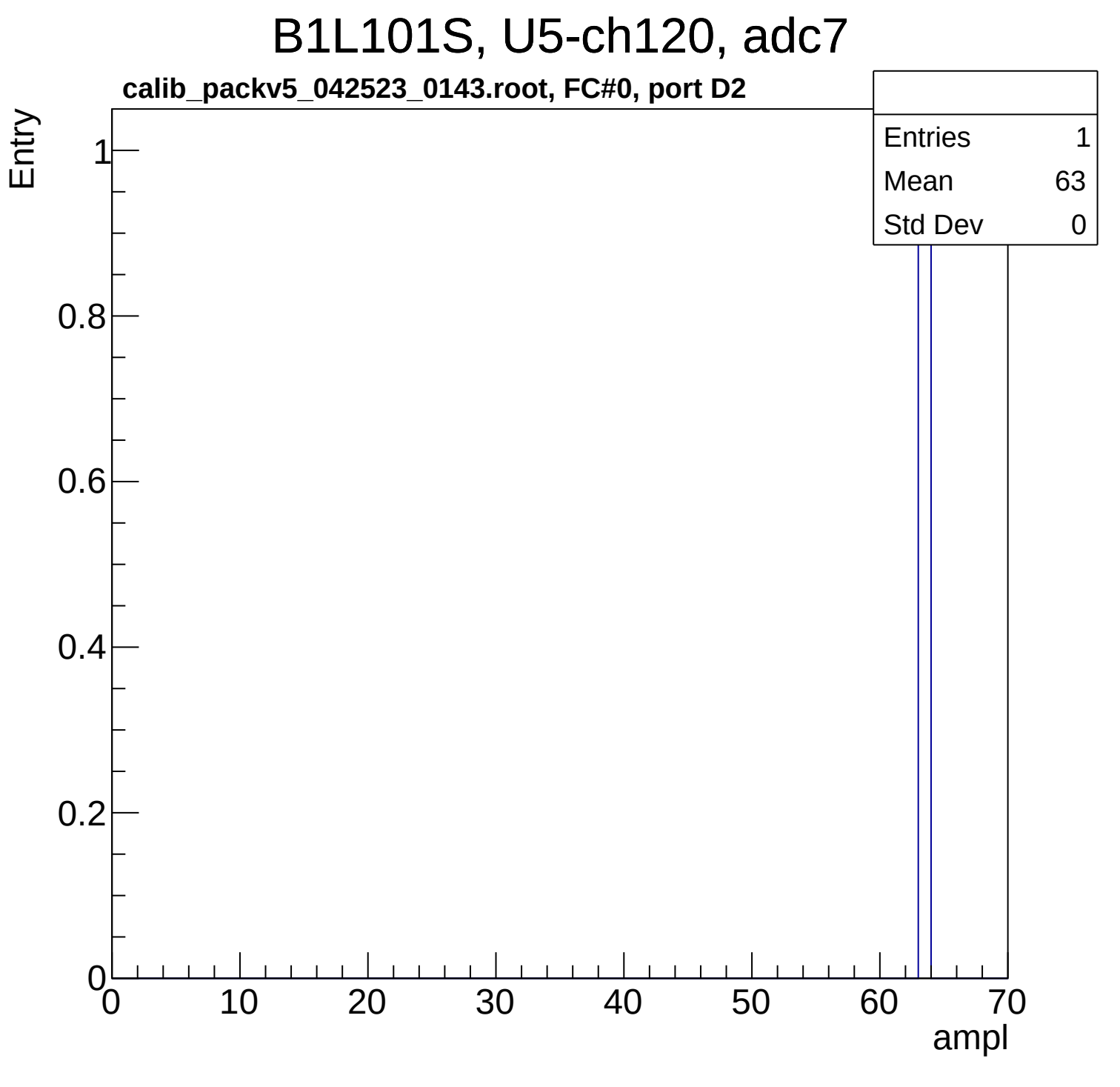
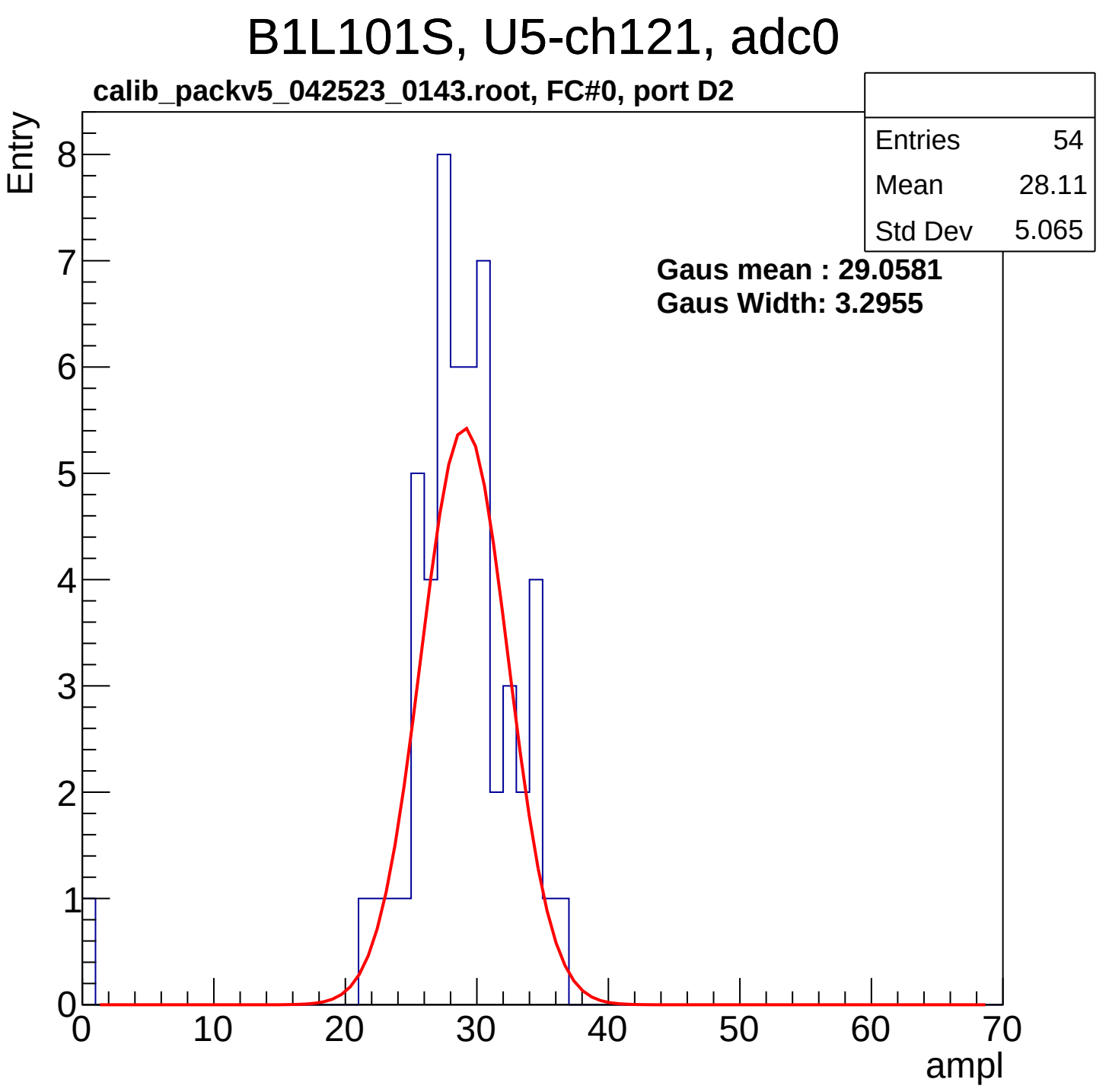
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L101S, U5-ch120, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch121, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 28.11
Std Dev 5.065
Gaus mean : 29.0581
Gaus Width: 3.2955
Entry
ampl
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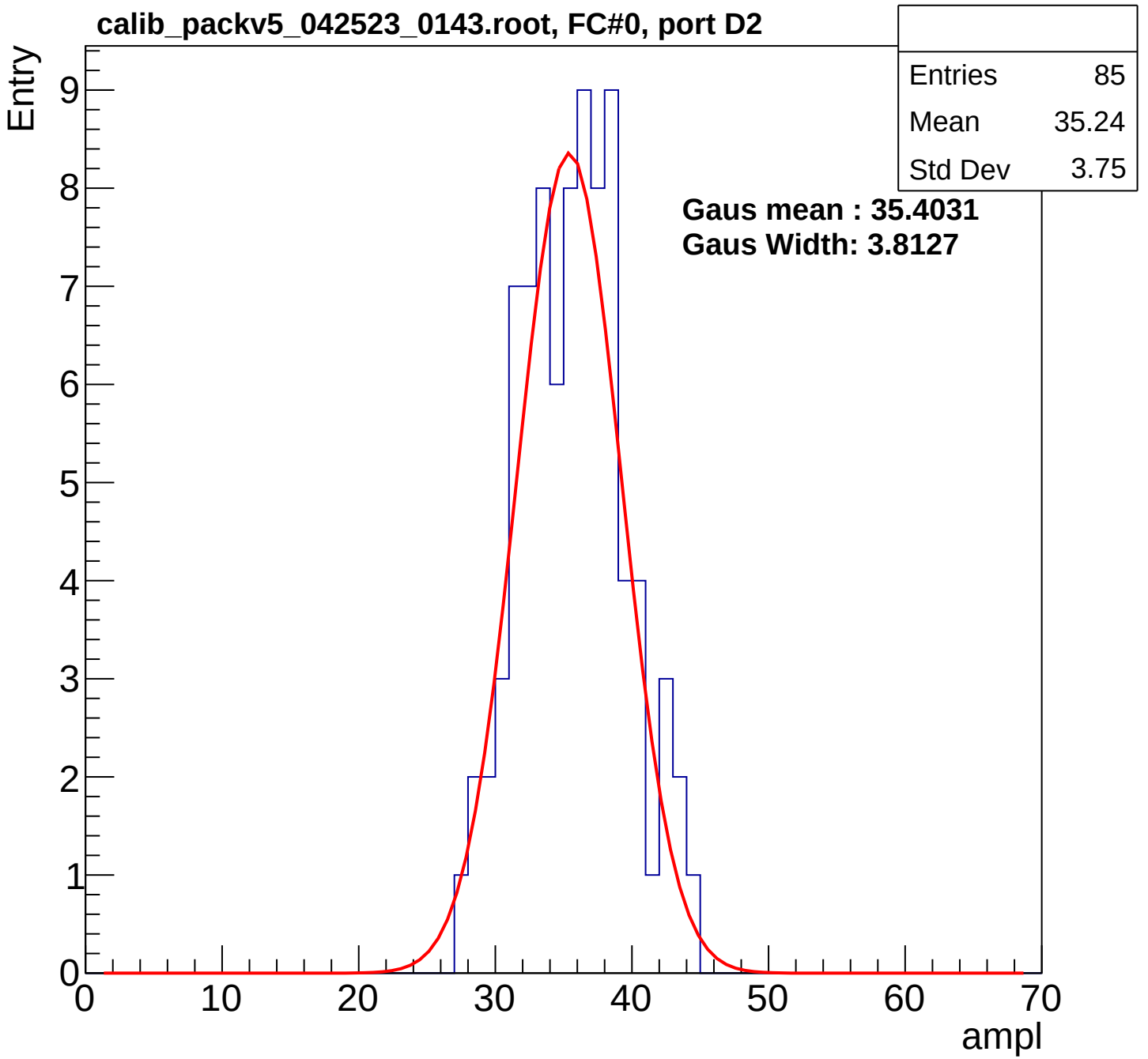
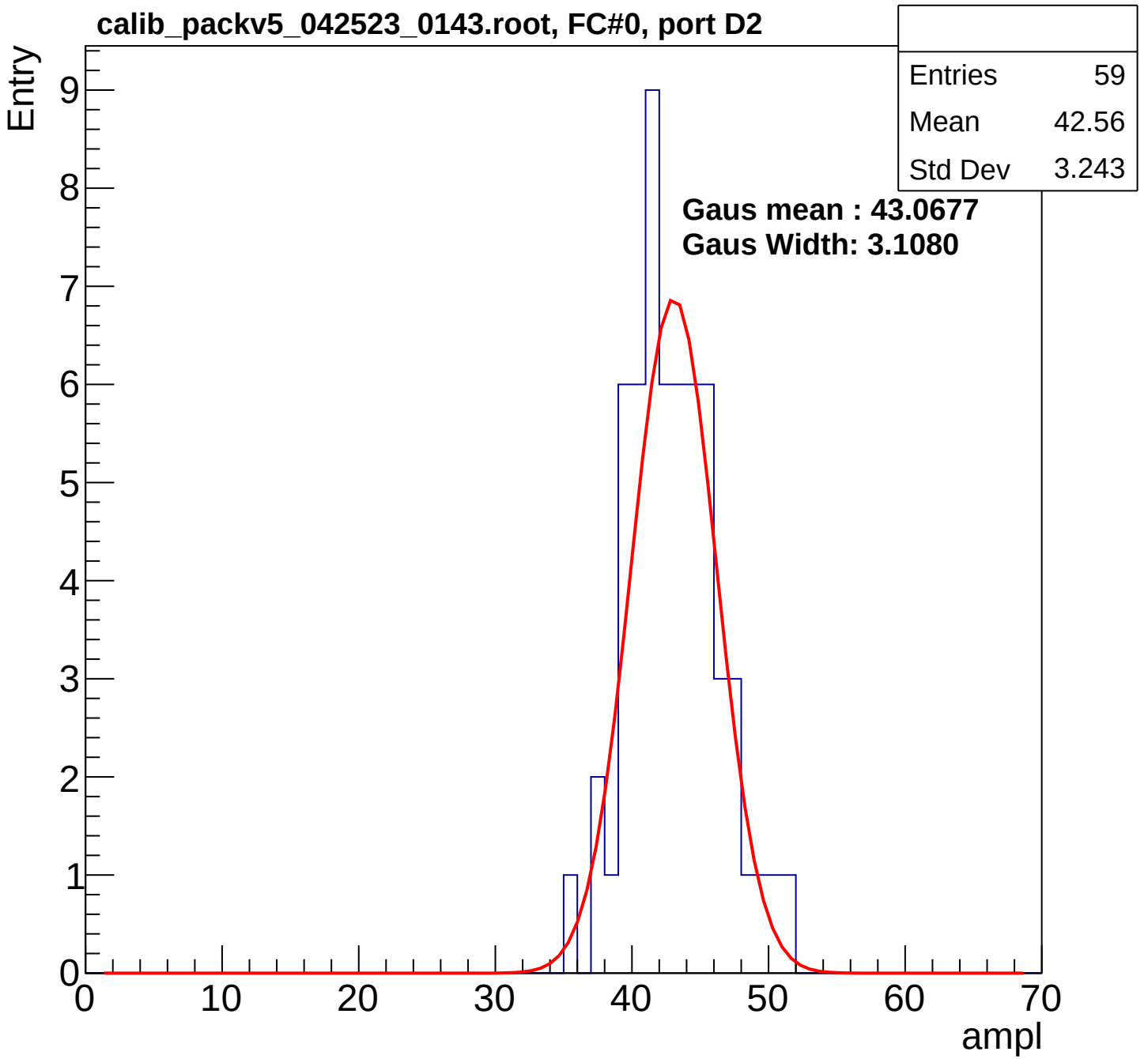
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch121, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 85
Mean 35.24
Std Dev 3.75
Gaus mean : 35.4031
Gaus Width: 3.8127
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch121, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 42.56
Std Dev 3.243
Gaus mean : 43.0677
Gaus Width: 3.1080
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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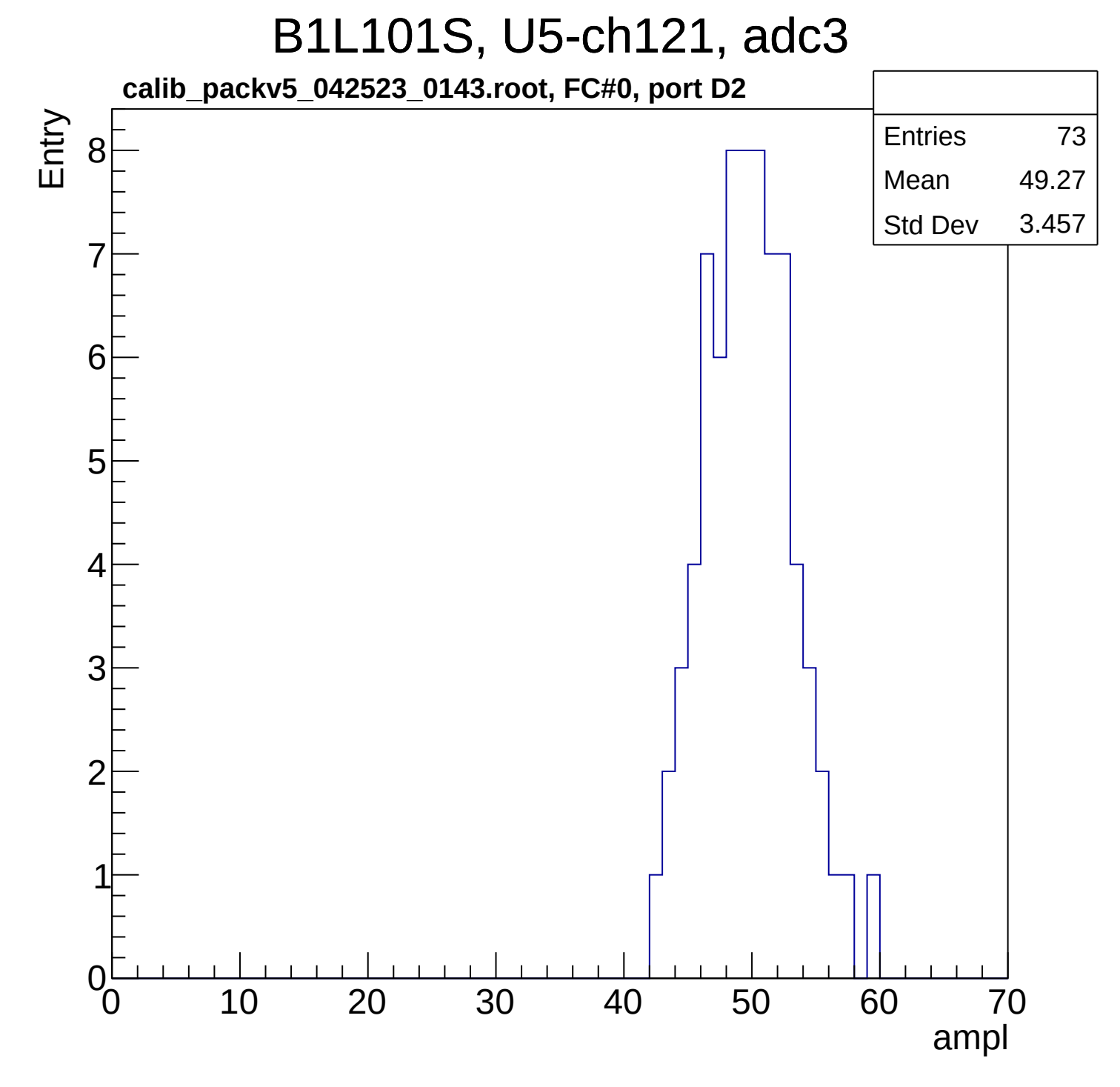
B1L101S, U5-ch121, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 49.27
Std Dev 3.457
Entry
ampl
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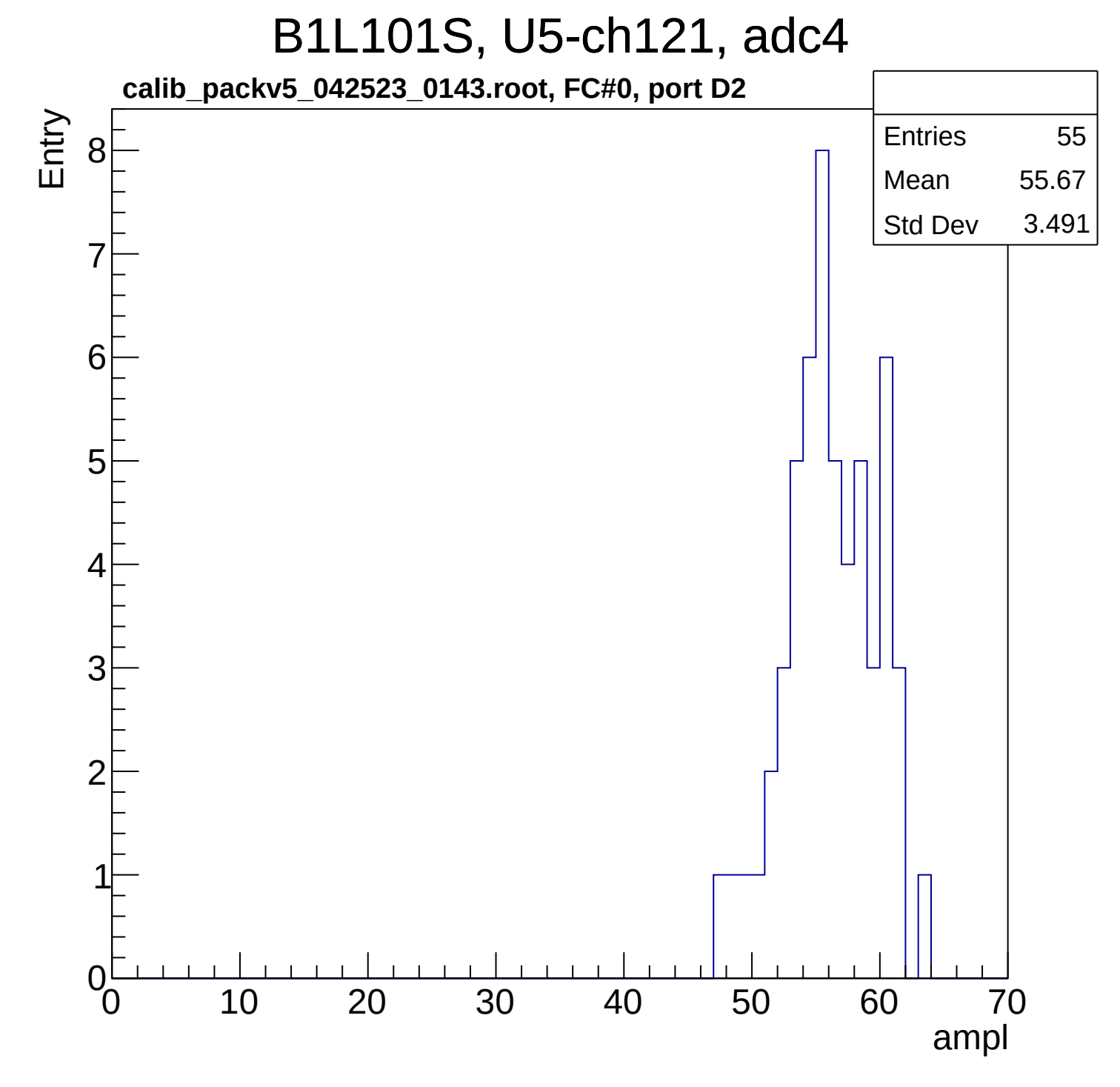
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch121, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 55.67
Std Dev 3.491
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
50
60
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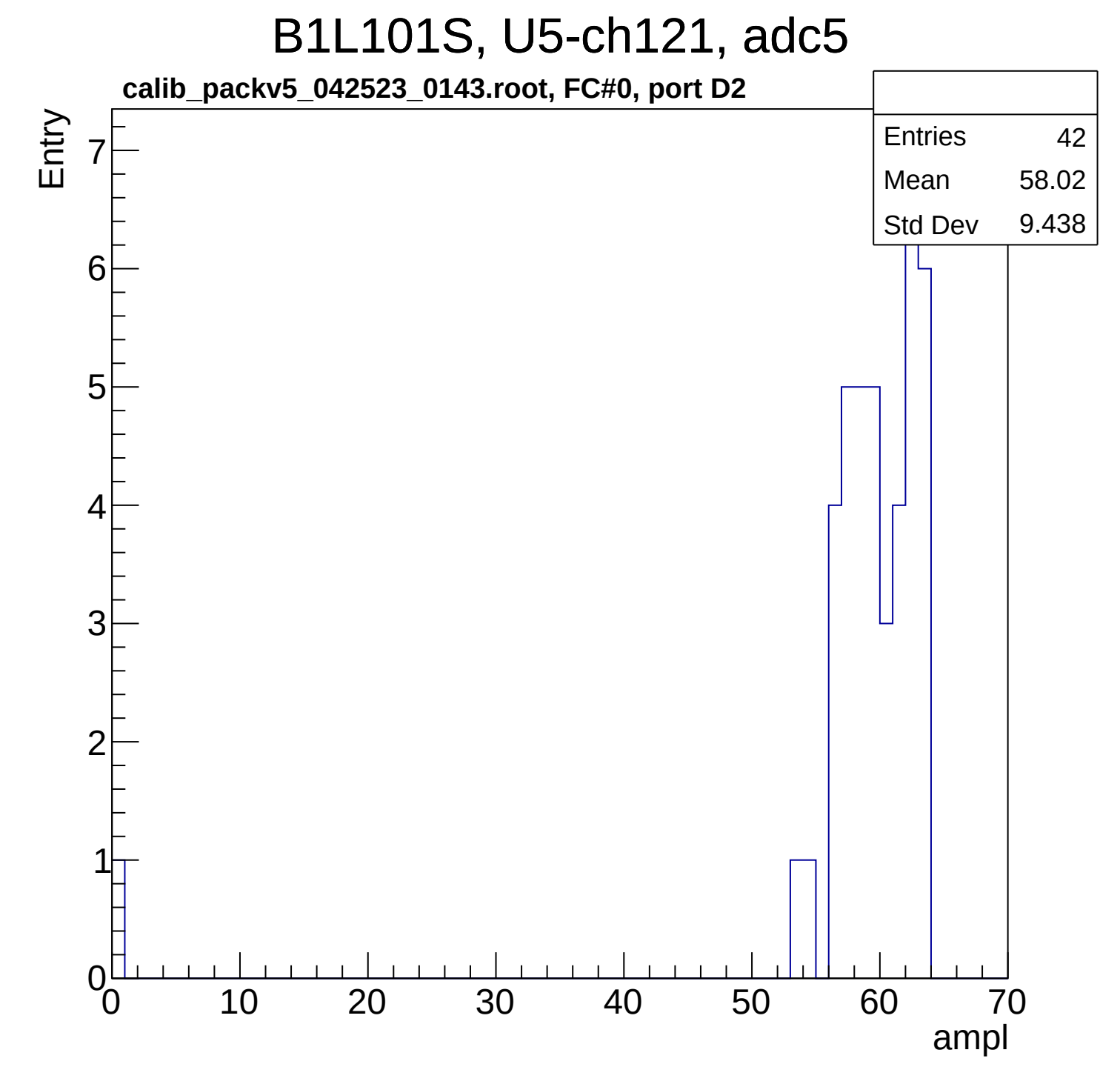
B1L101S, U5-ch121, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 58.02
Std Dev 9.438
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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60
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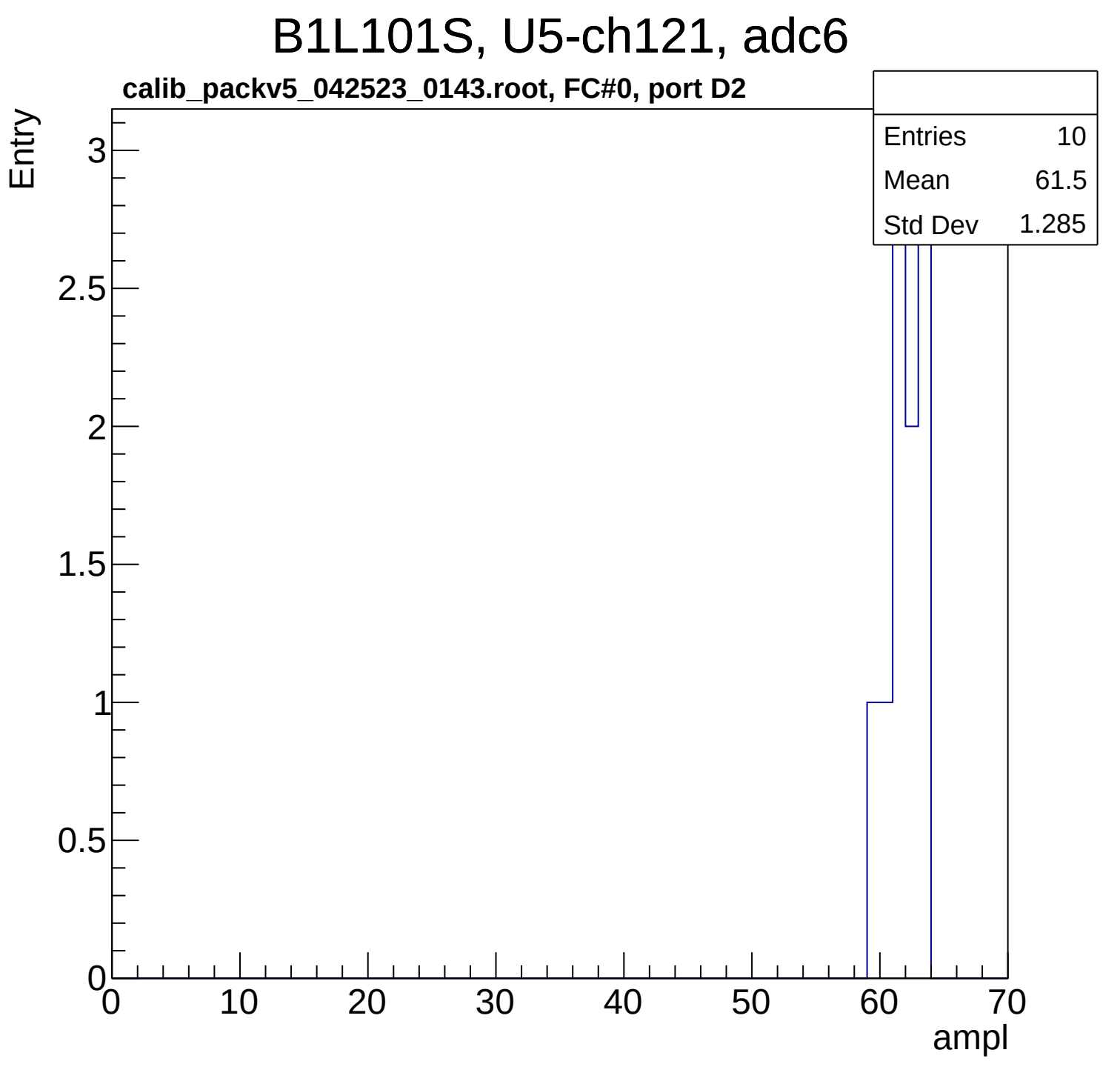
B1L101S, U5-ch121, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 61.5
Std Dev 1.285
Entry
ampl
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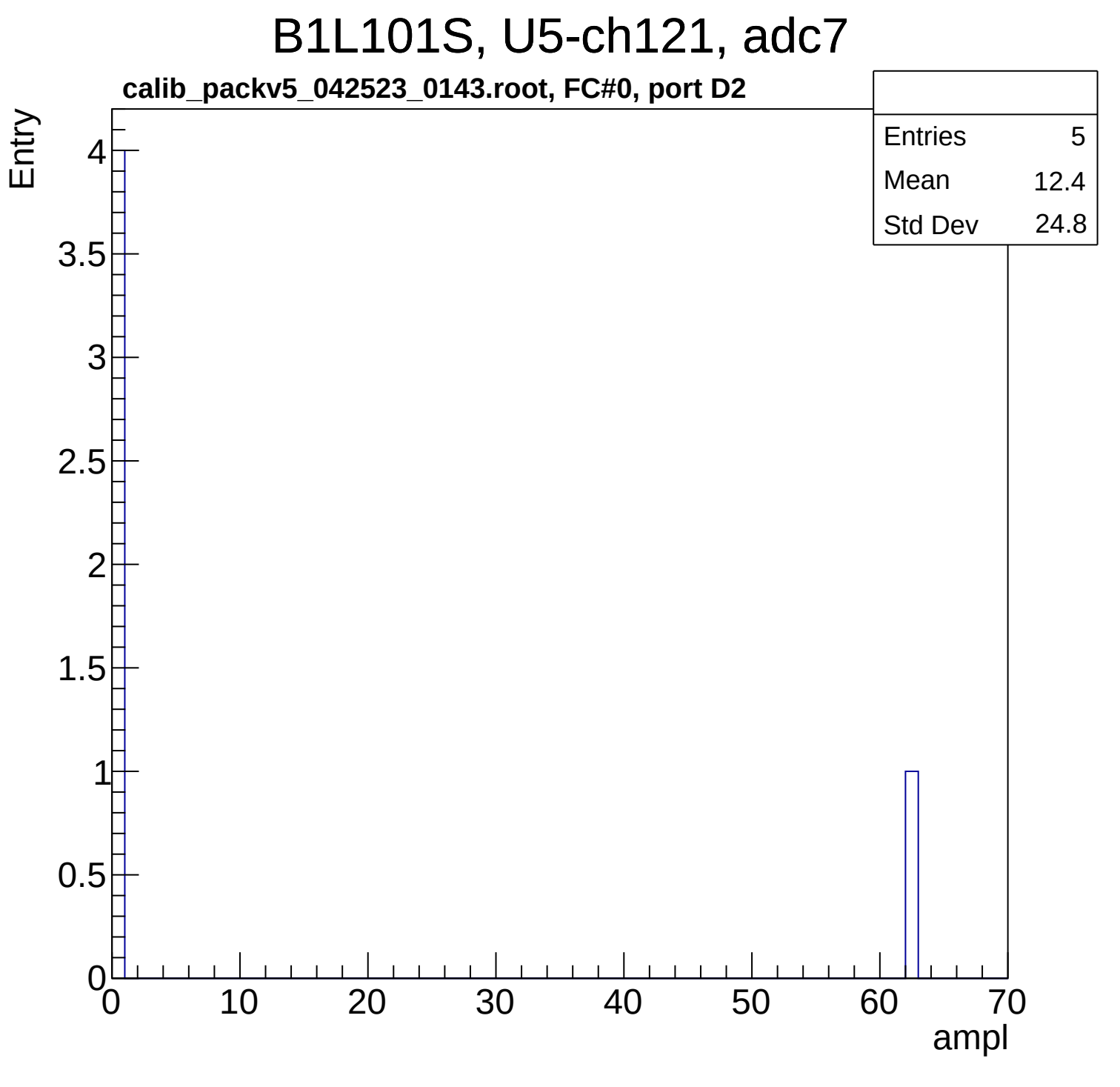
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U5-ch121, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 12.4
Std Dev 24.8
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
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60
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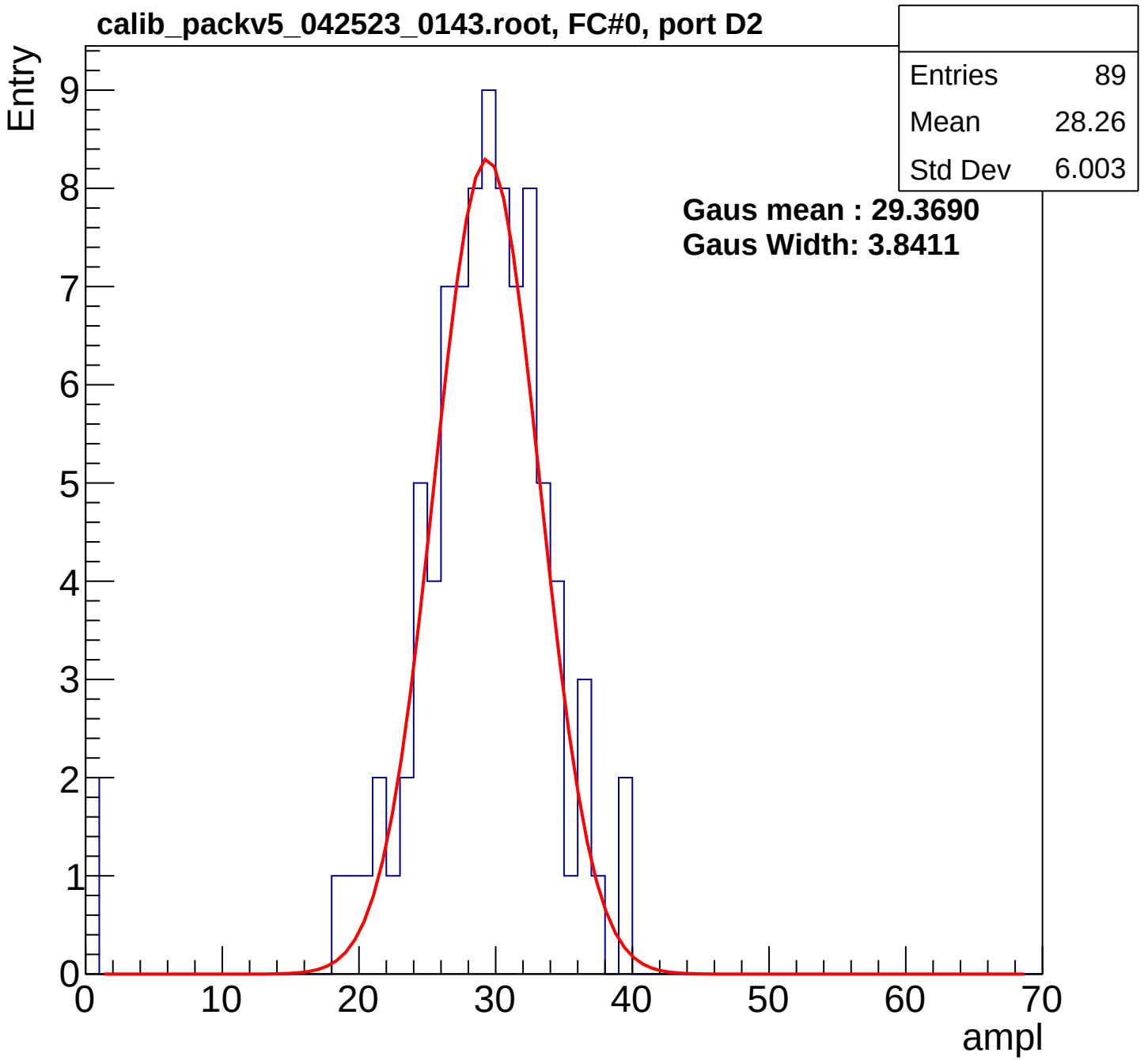
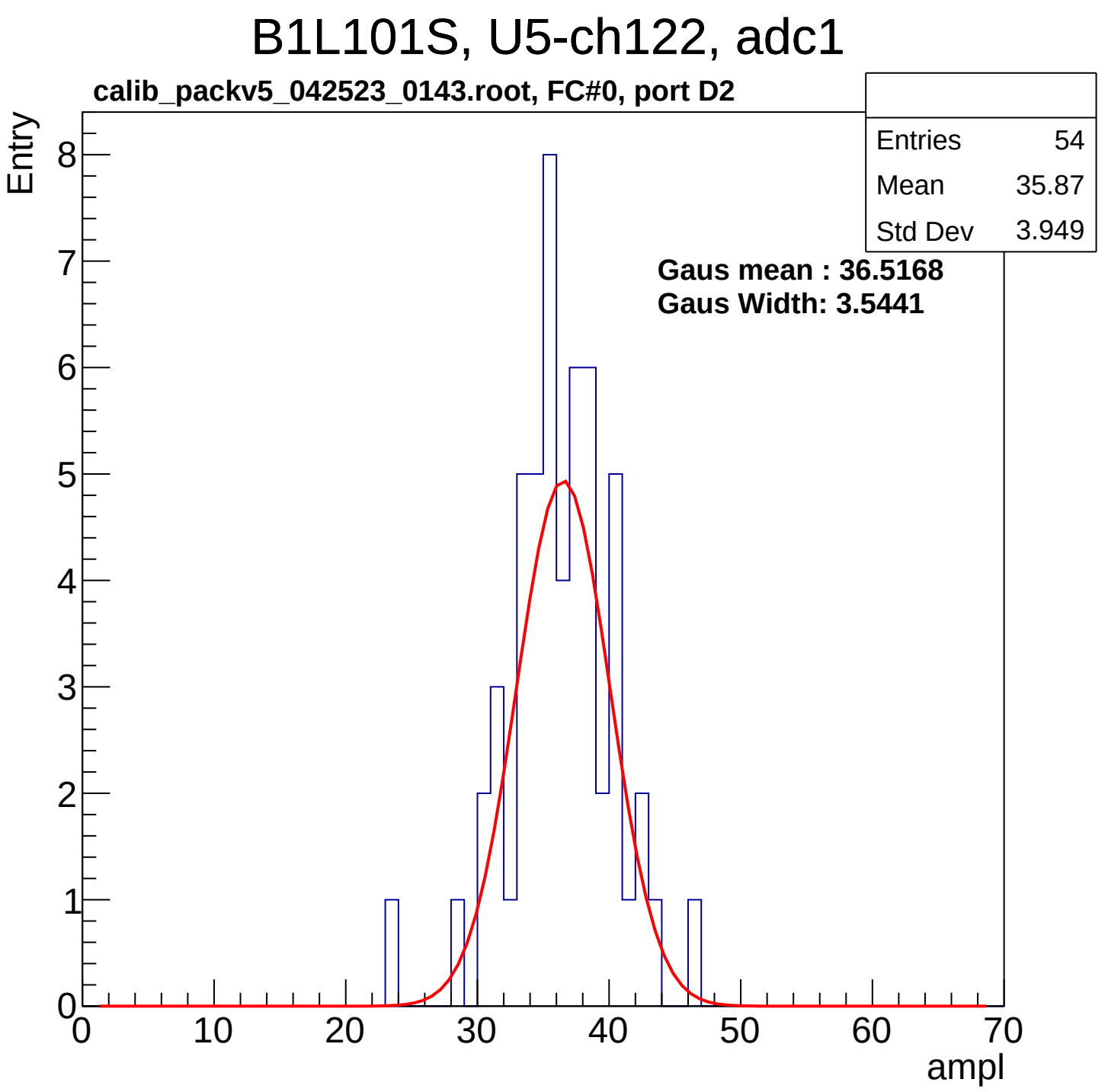
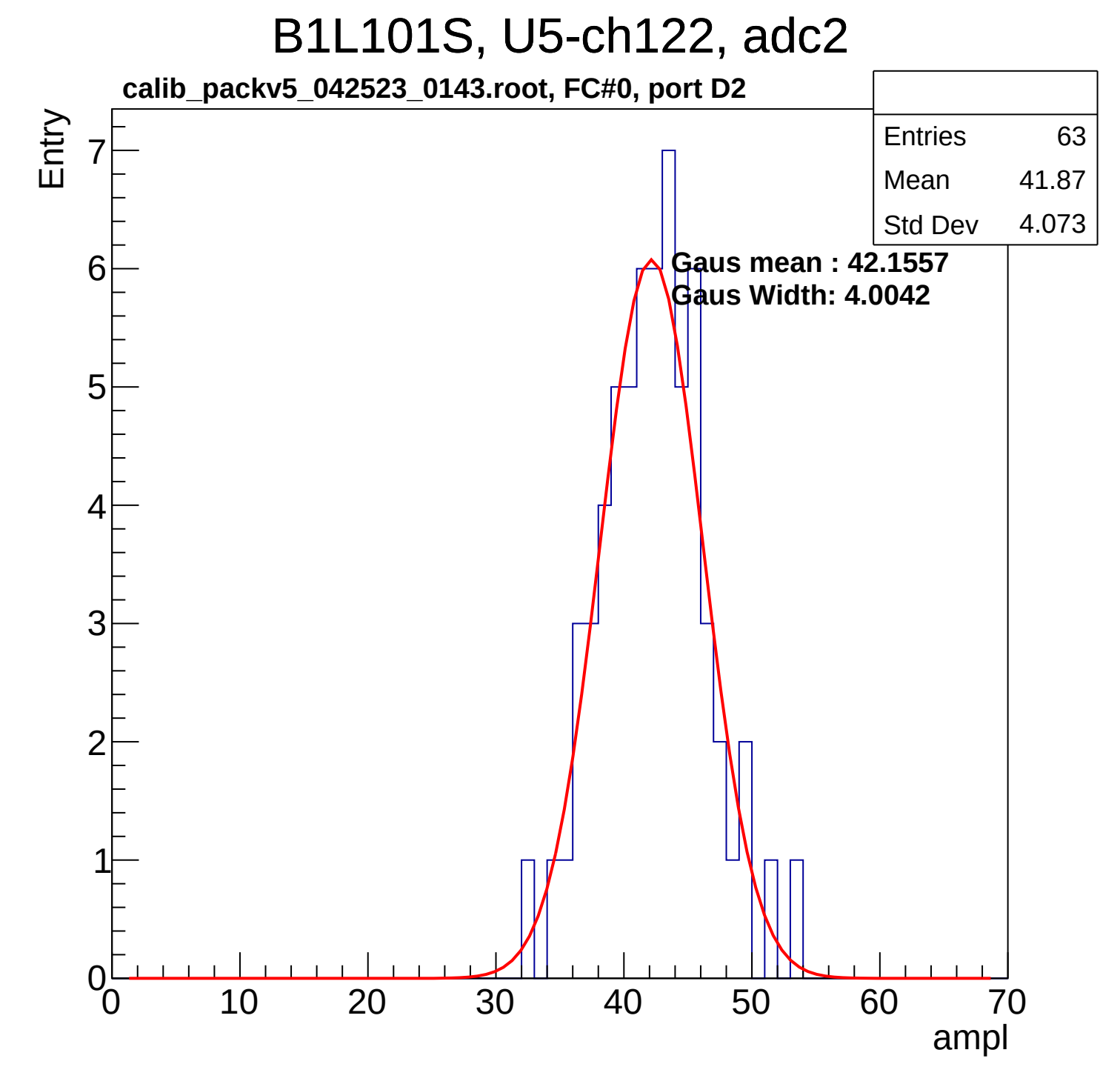

B1L101S, U5-ch122, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 89
Mean 28.26
Std Dev 6.003
Gaus mean : 29.3690
Gaus Width: 3.8411
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch122, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 35.87
Std Dev 3.949
Gaus mean : 36.5168
Gaus Width: 3.5441
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch122, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 41.87
Std Dev 4.073
Gaus mean : 42.1557
Gaus Width: 4.0042
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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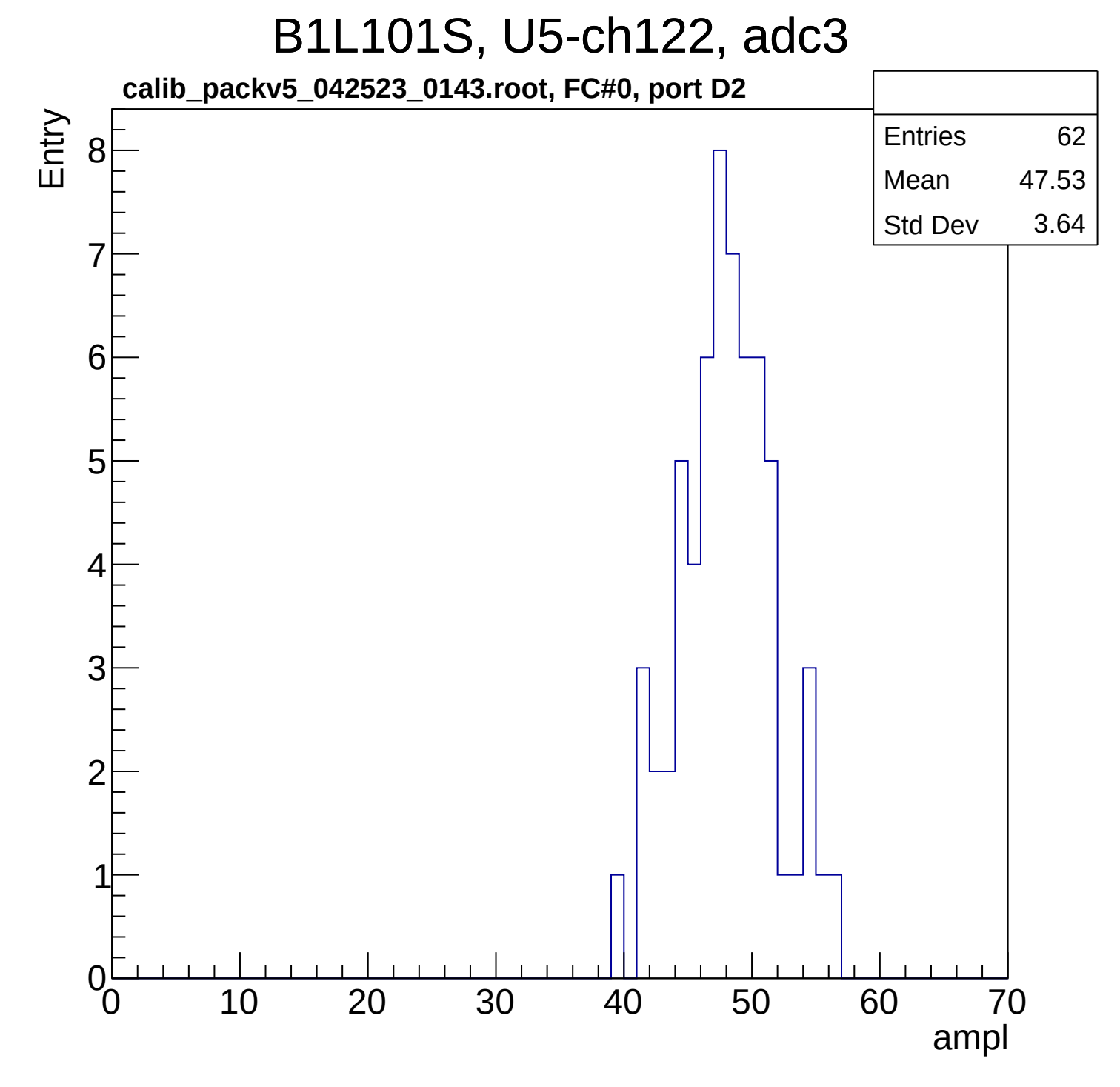
B1L101S, U5-ch122, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 47.53
Std Dev 3.64
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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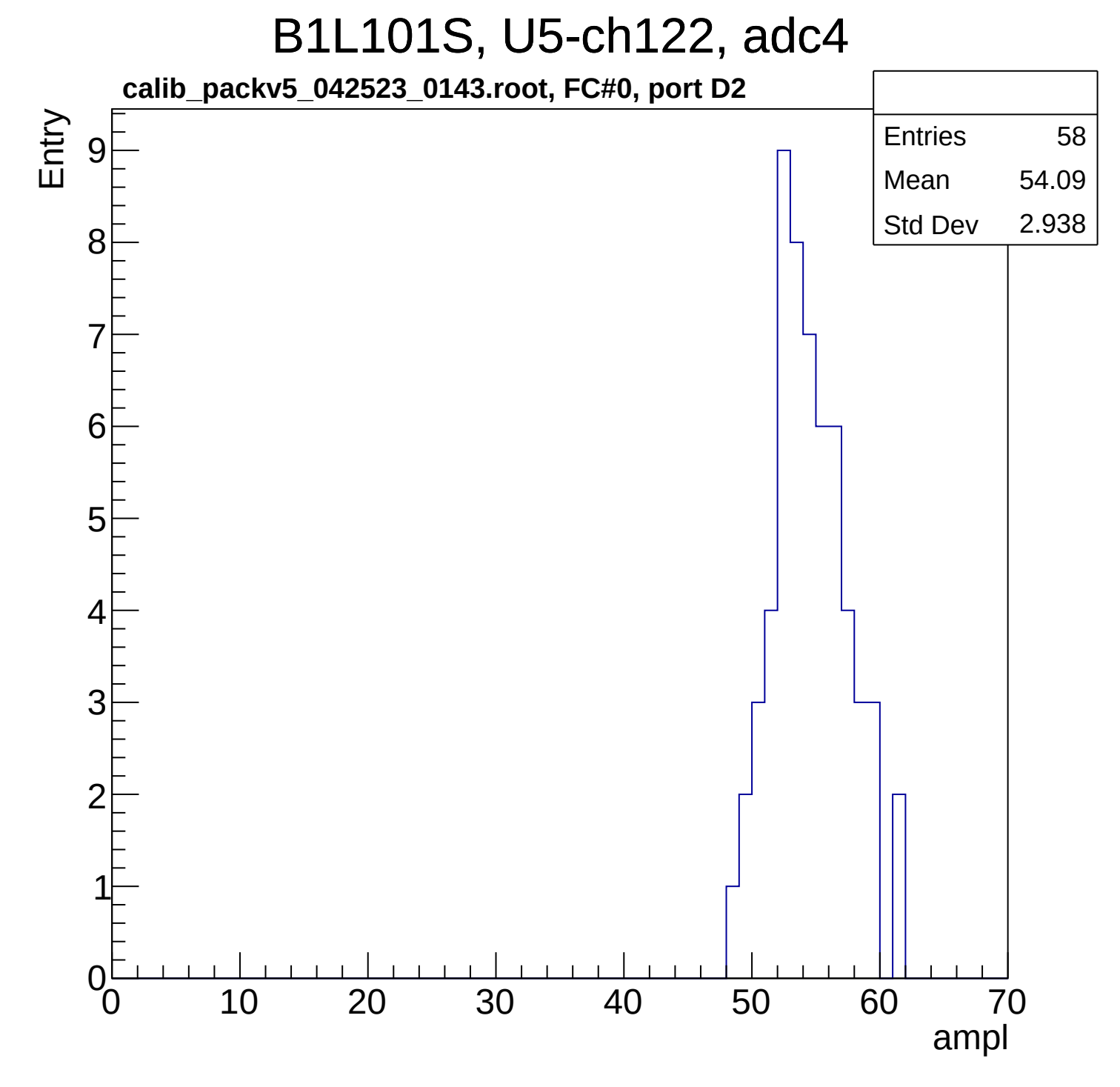
B1L101S, U5-ch122, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 54.09
Std Dev 2.938
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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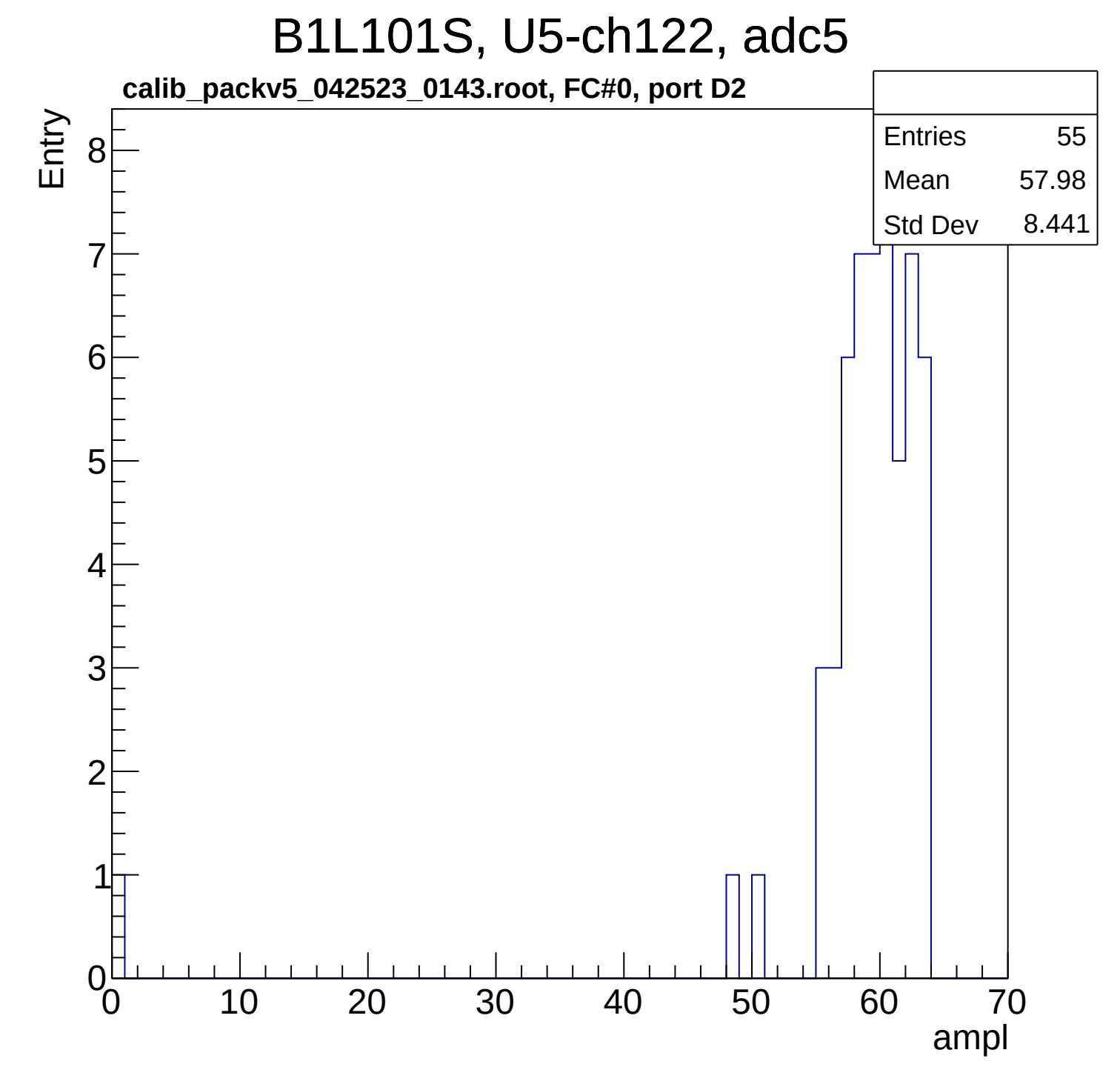
B1L101S, U5-ch122, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 57.98
Std Dev 8.441
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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40
50
60
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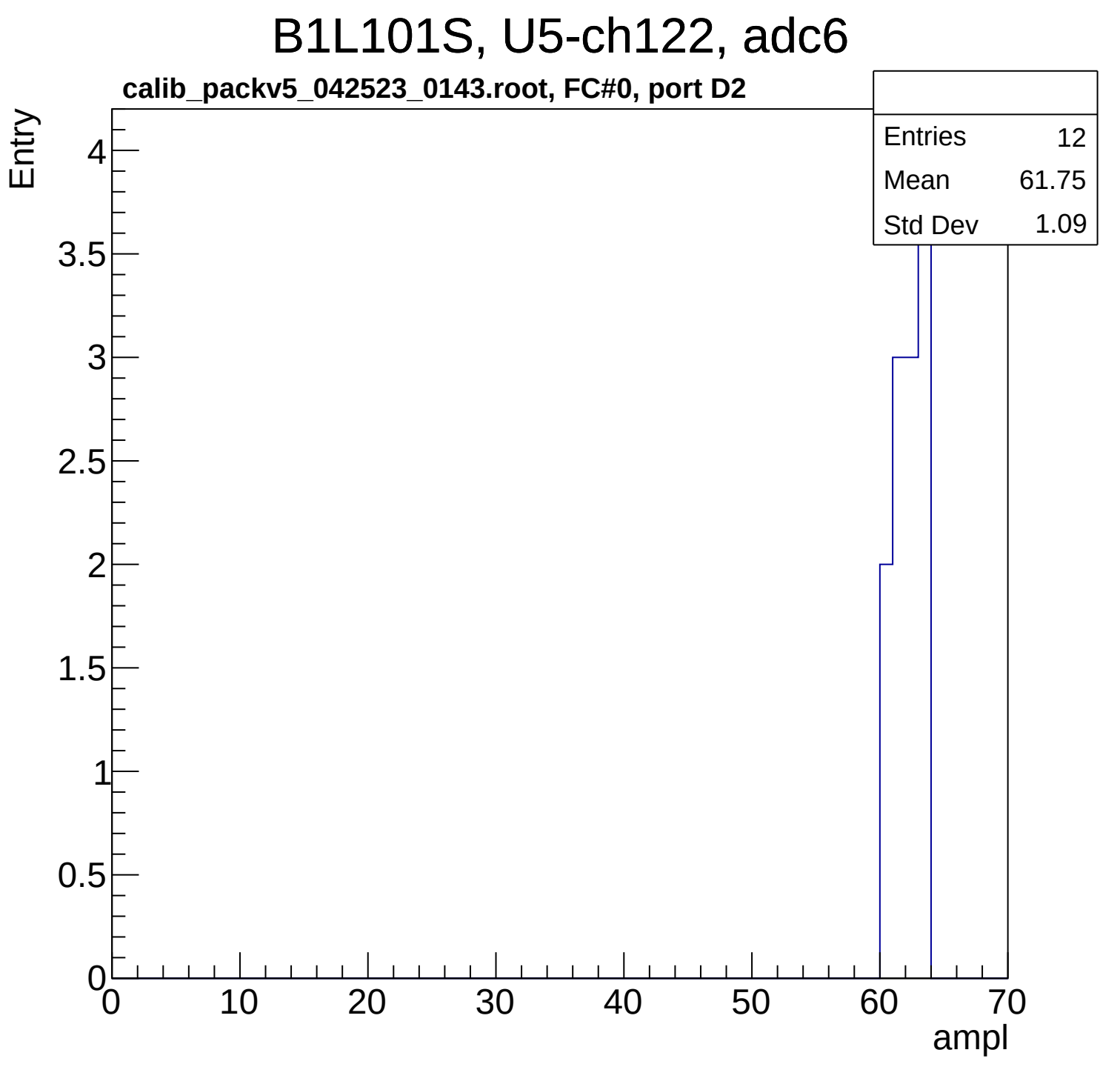
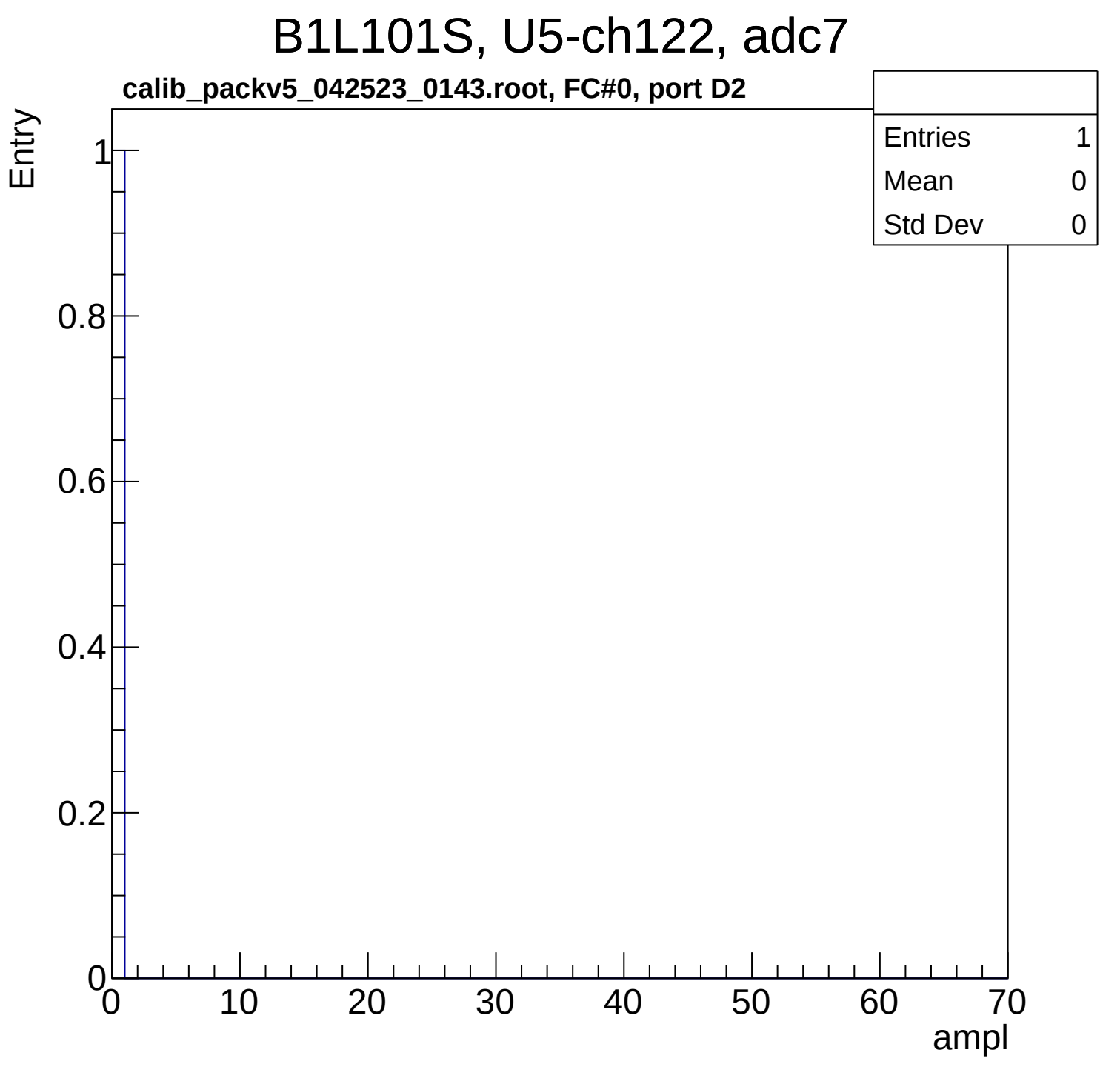

B1L101S, U5-ch122, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 12
Mean 61.75
Std Dev 1.09
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L101S, U5-ch122, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
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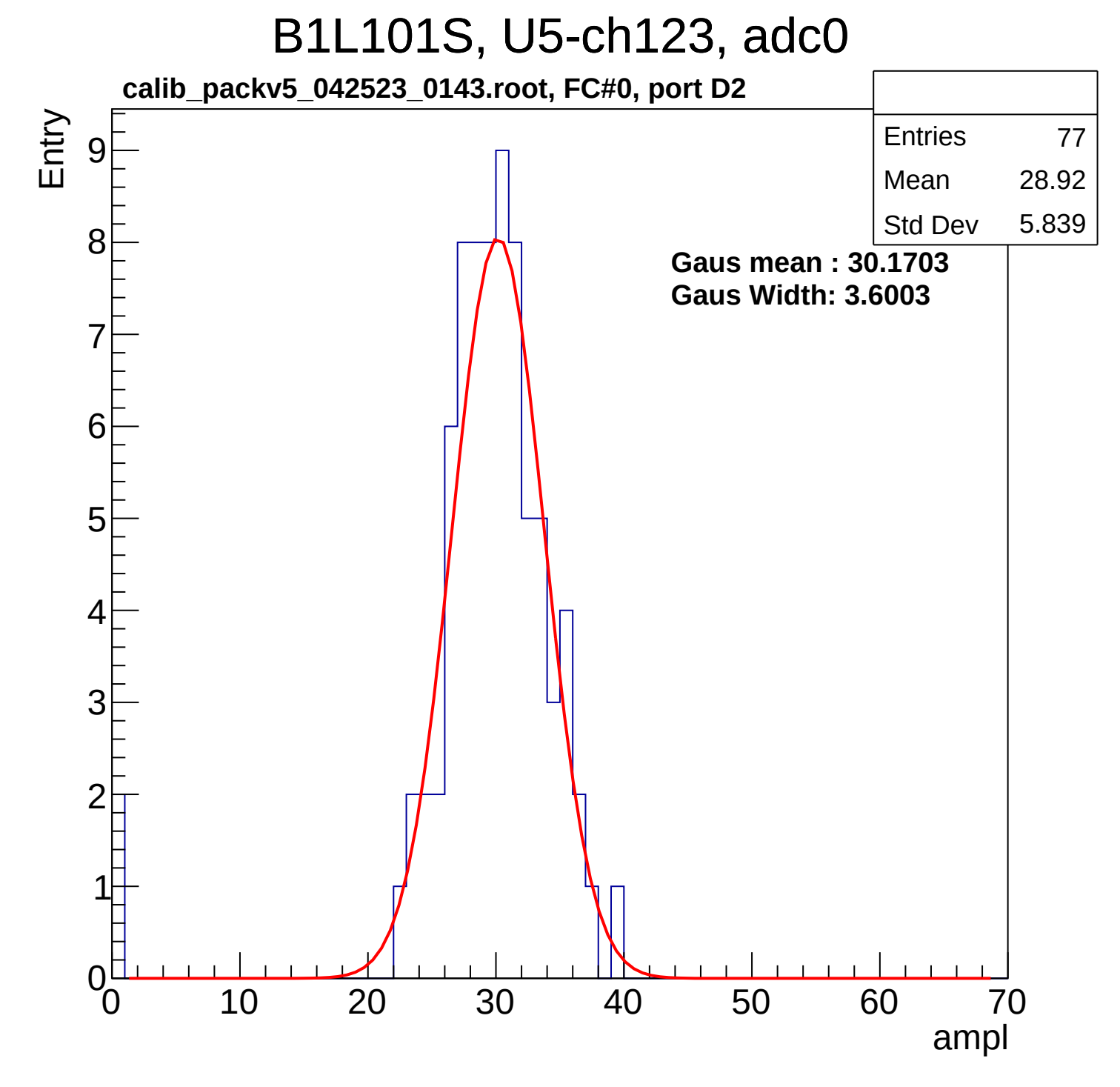
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch123, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 28.92
Std Dev 5.839
Gaus mean : 30.1703
Gaus Width: 3.6003
Entry
ampl
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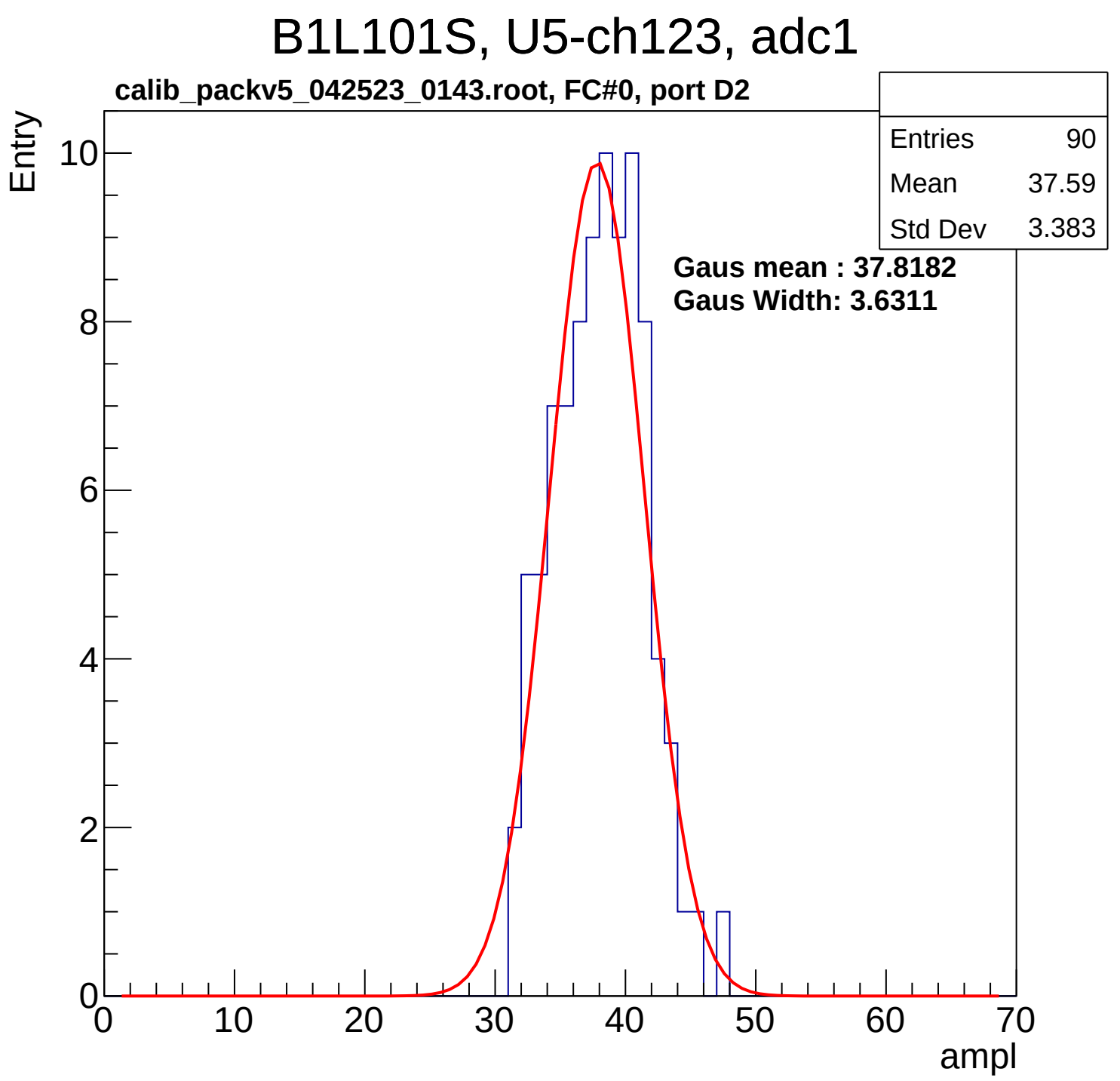
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch123, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 90
Mean 37.59
Std Dev 3.383
Gaus mean : 37.8182
Gaus Width: 3.6311
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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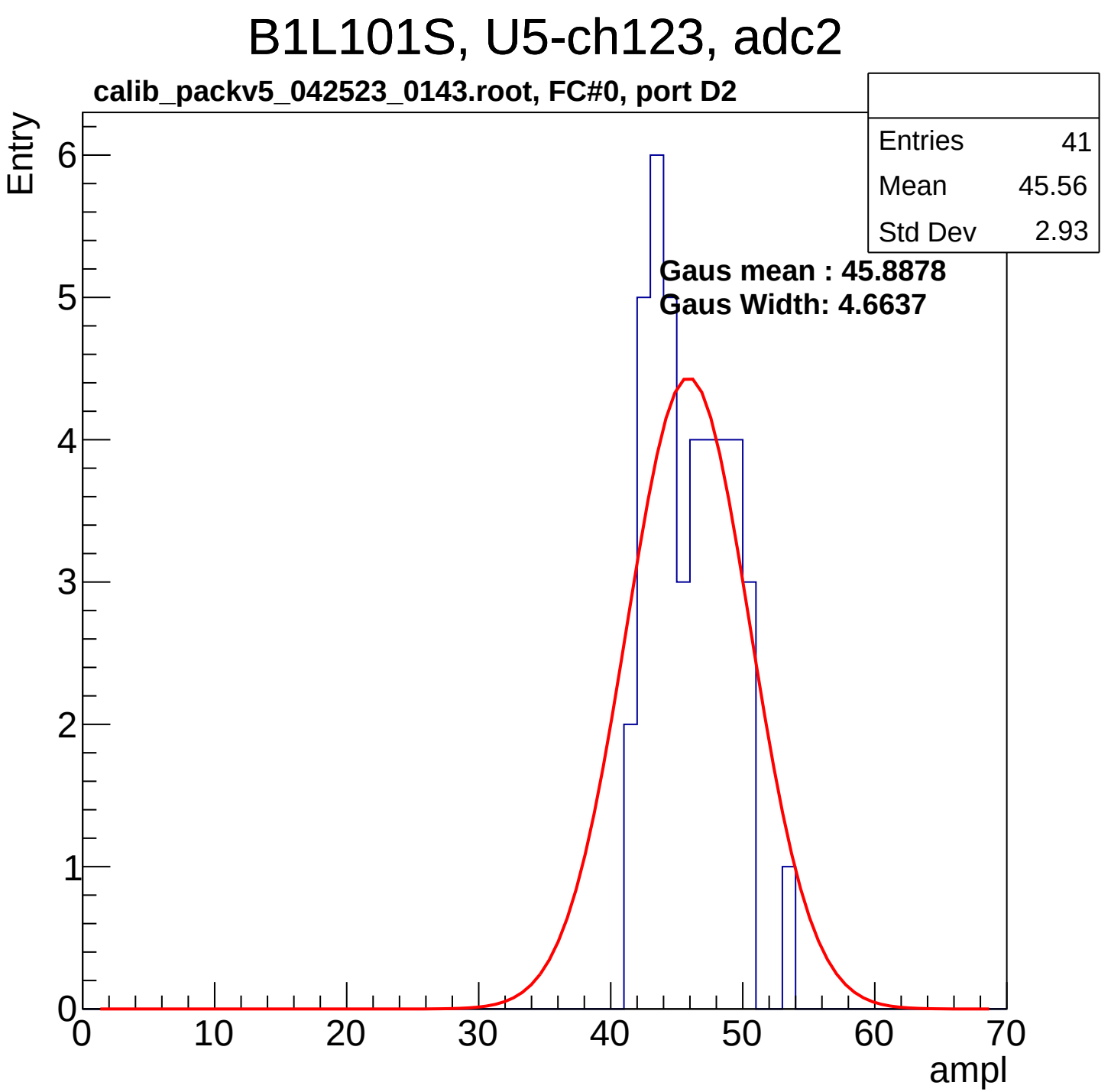
B1L101S, U5-ch123, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 41
Mean 45.56
Std Dev 2.93
Gaus mean : 45.8878
Gaus Width: 4.6637
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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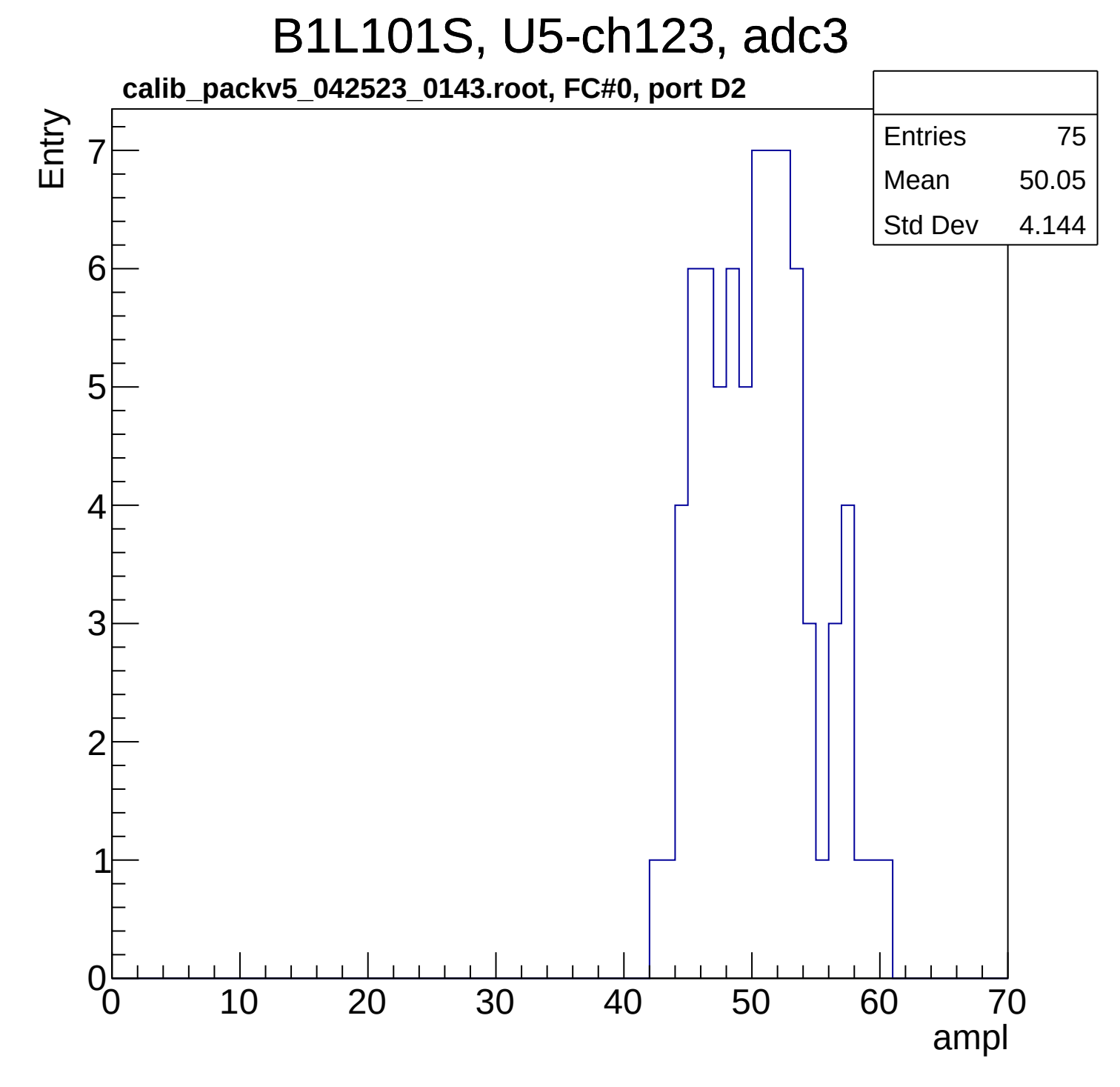
B1L101S, U5-ch123, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 50.05
Std Dev 4.144
Entry
ampl
0
1
2
3
4
5
6
7
0
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40
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60
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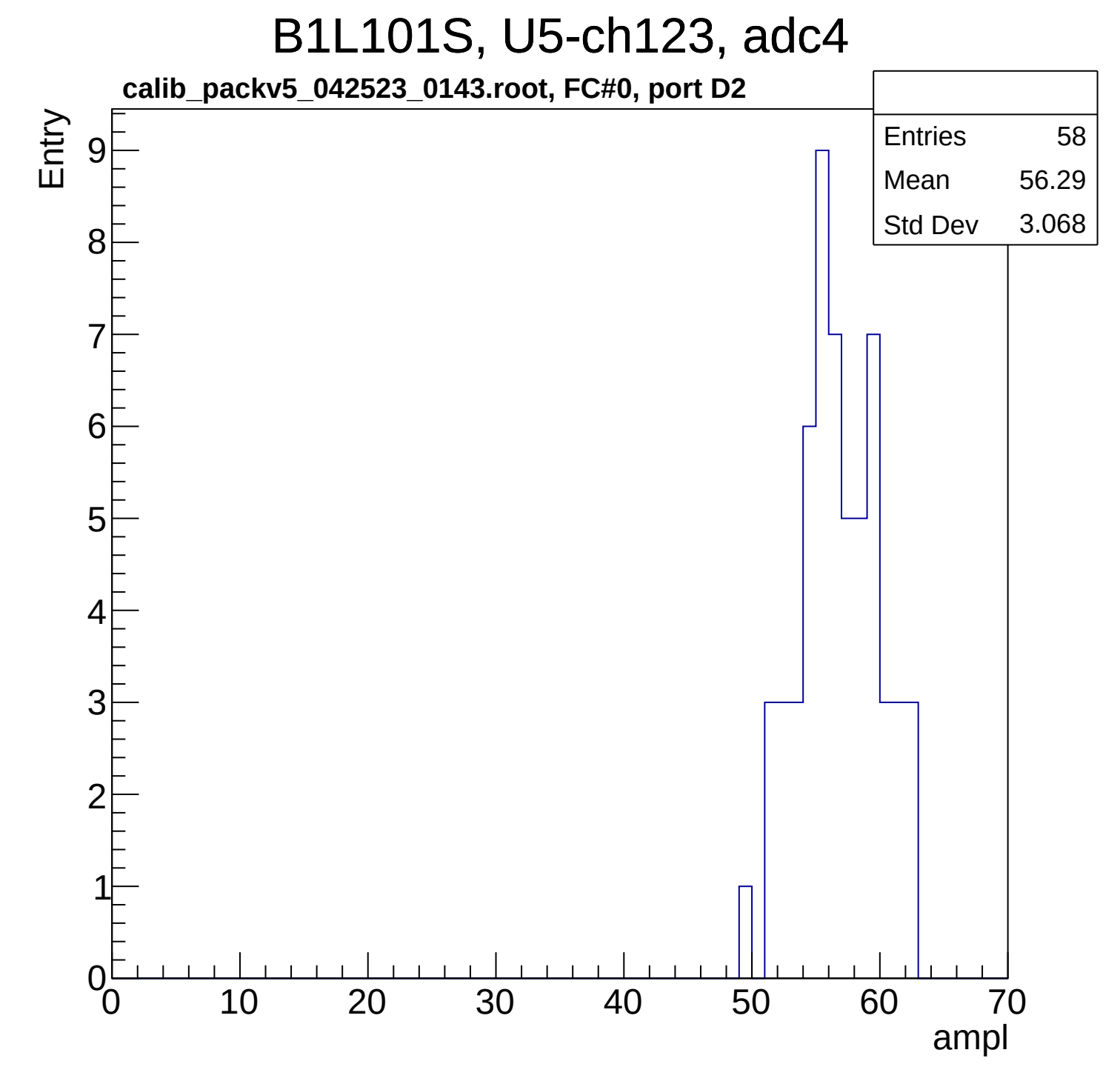
B1L101S, U5-ch123, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 56.29
Std Dev 3.068
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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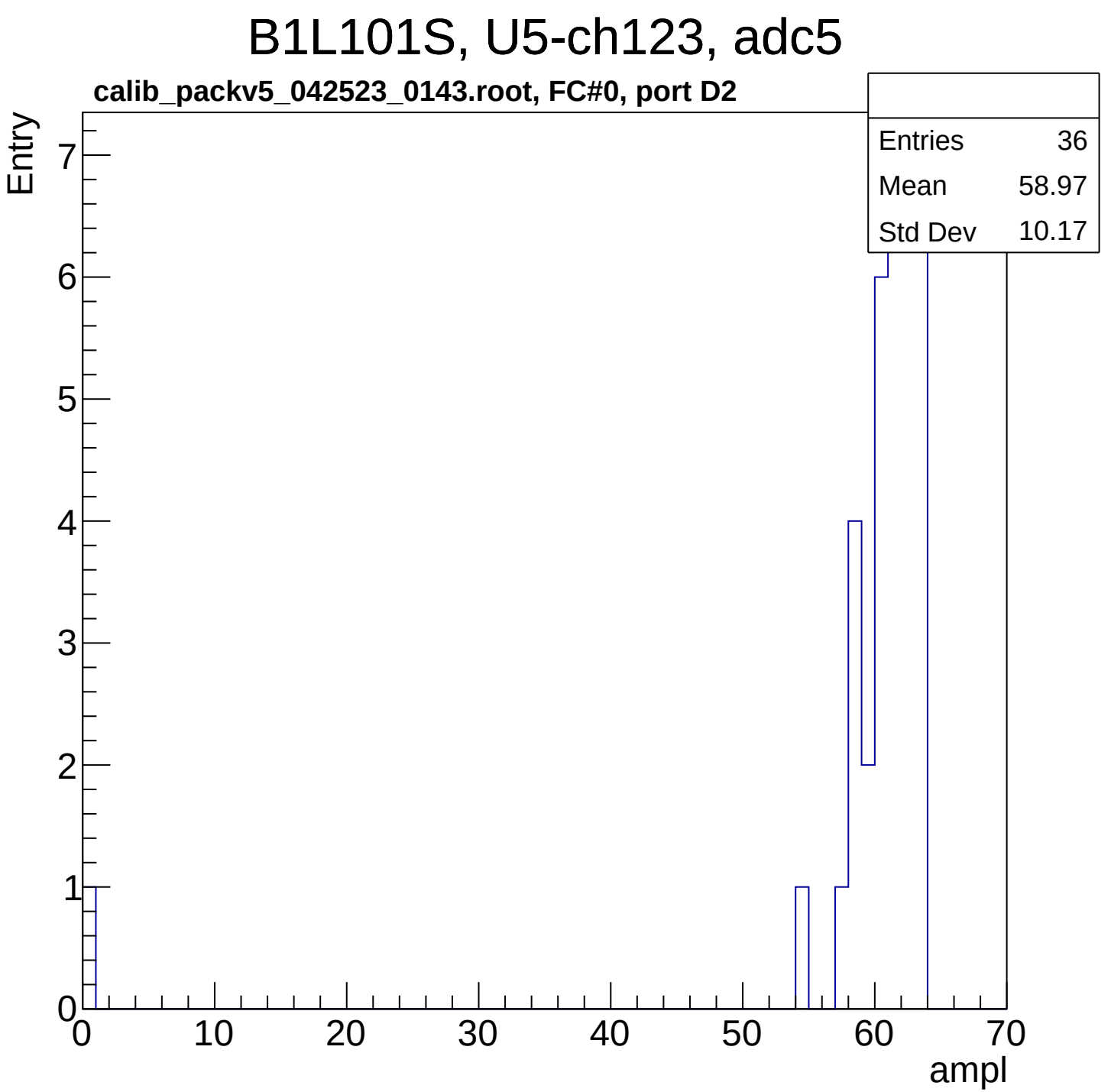
B1L101S, U5-ch123, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 36
Mean 58.97
Std Dev 10.17
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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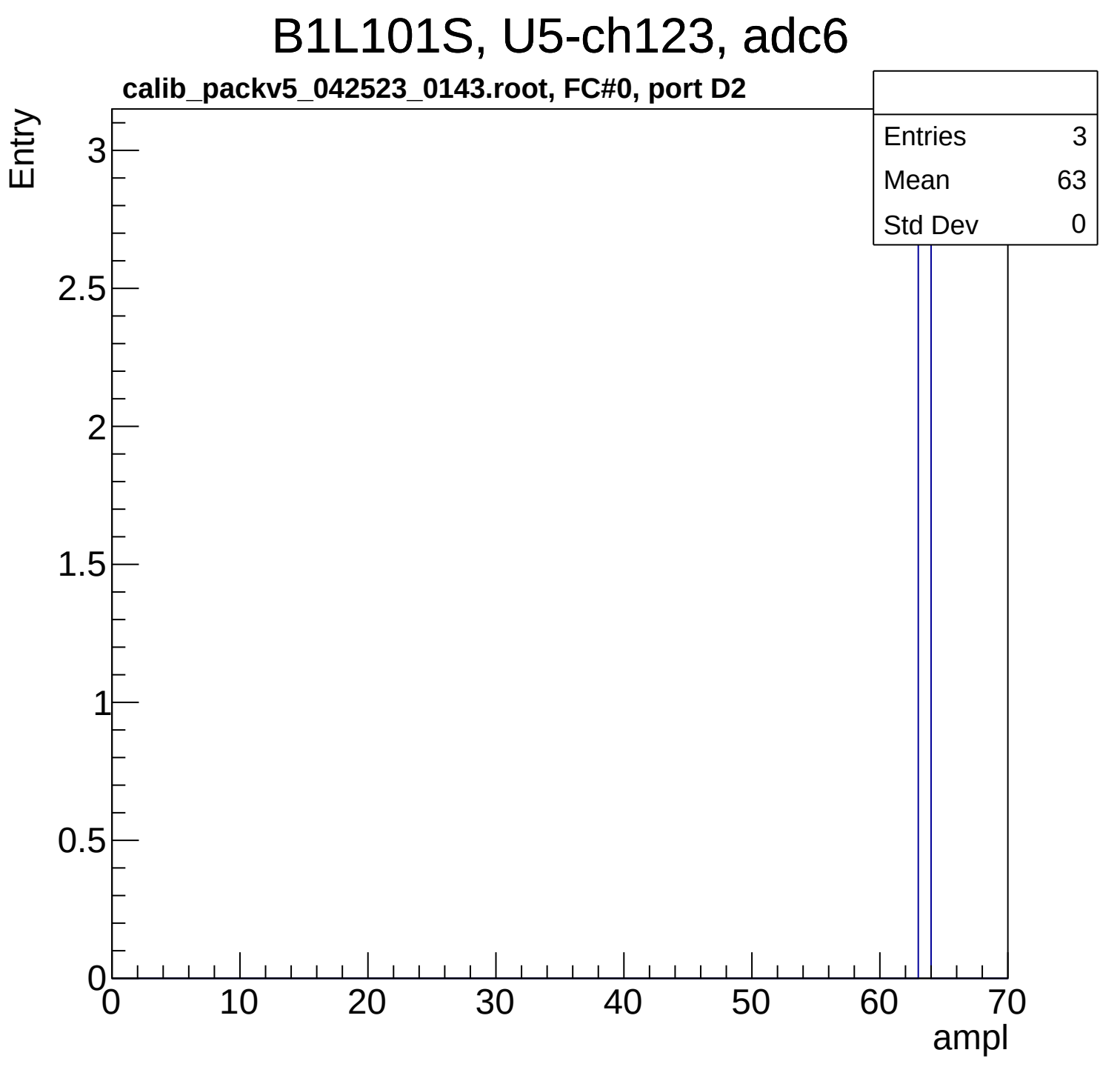
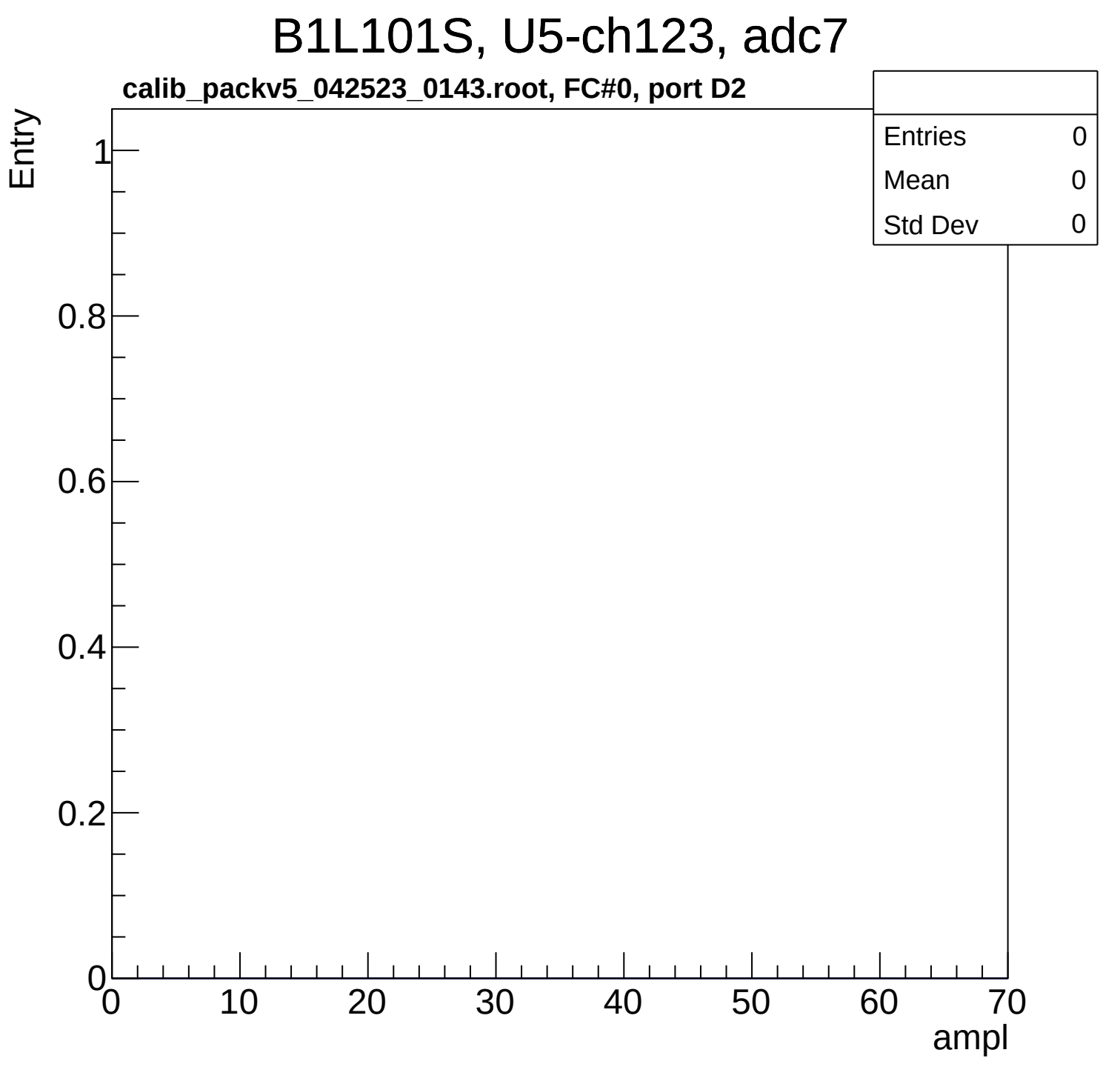
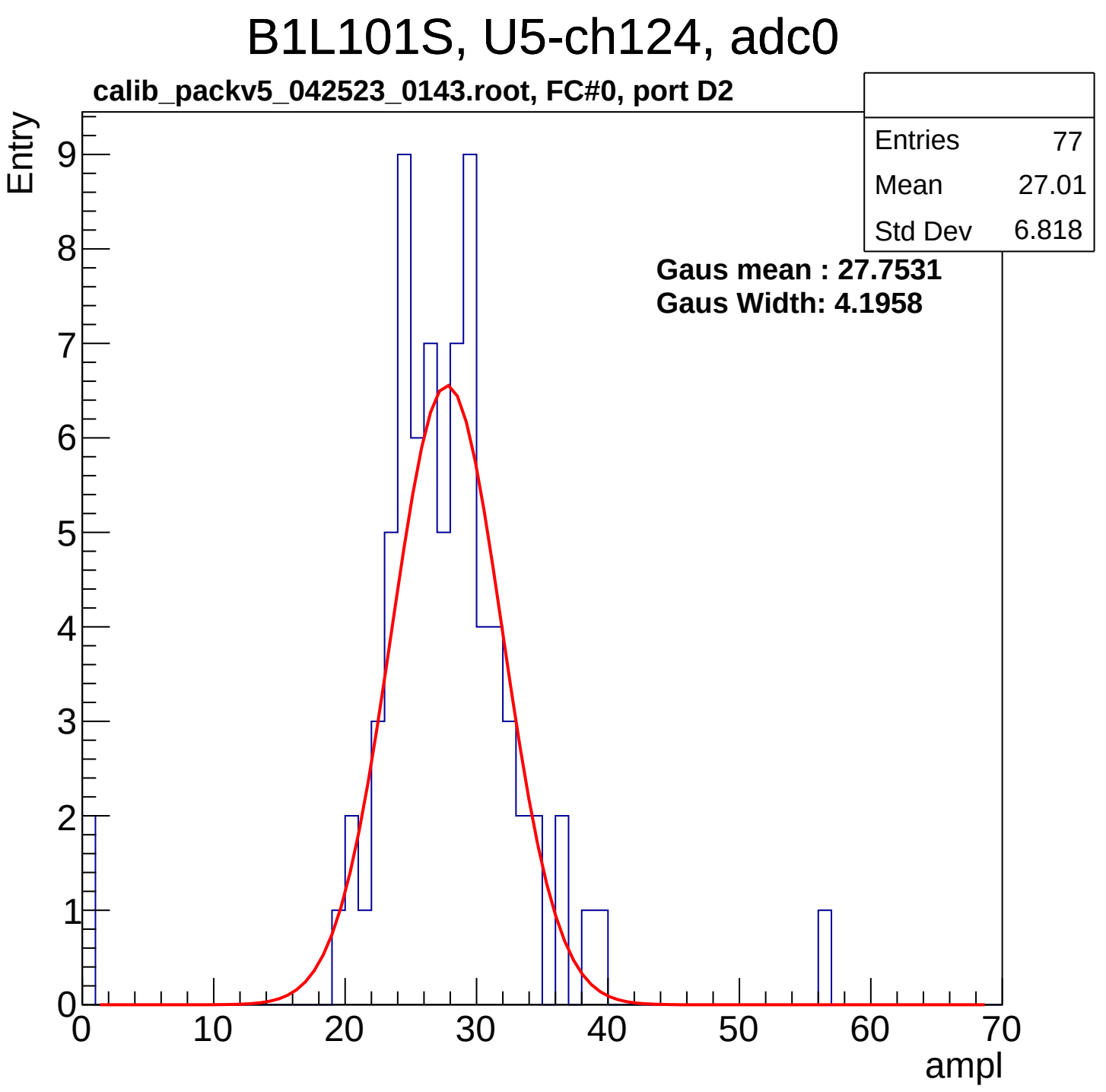
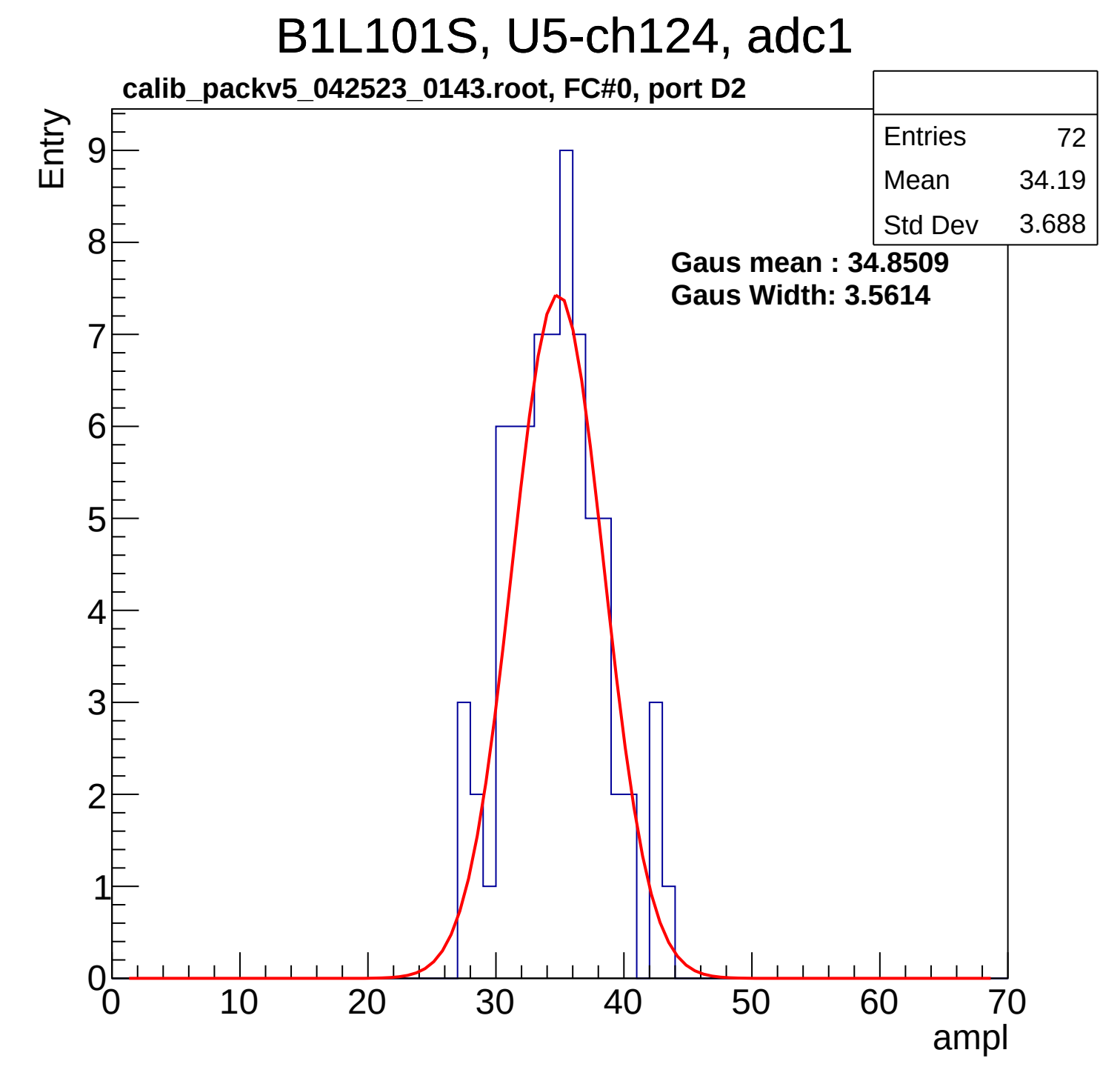

B1L101S, U5-ch123, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 63
Std Dev 0
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U5-ch123, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch124, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 27.01
Std Dev 6.818
Gaus mean : 27.7531
Gaus Width: 4.1958
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch124, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 34.19
Std Dev 3.688
Gaus mean : 34.8509
Gaus Width: 3.5614
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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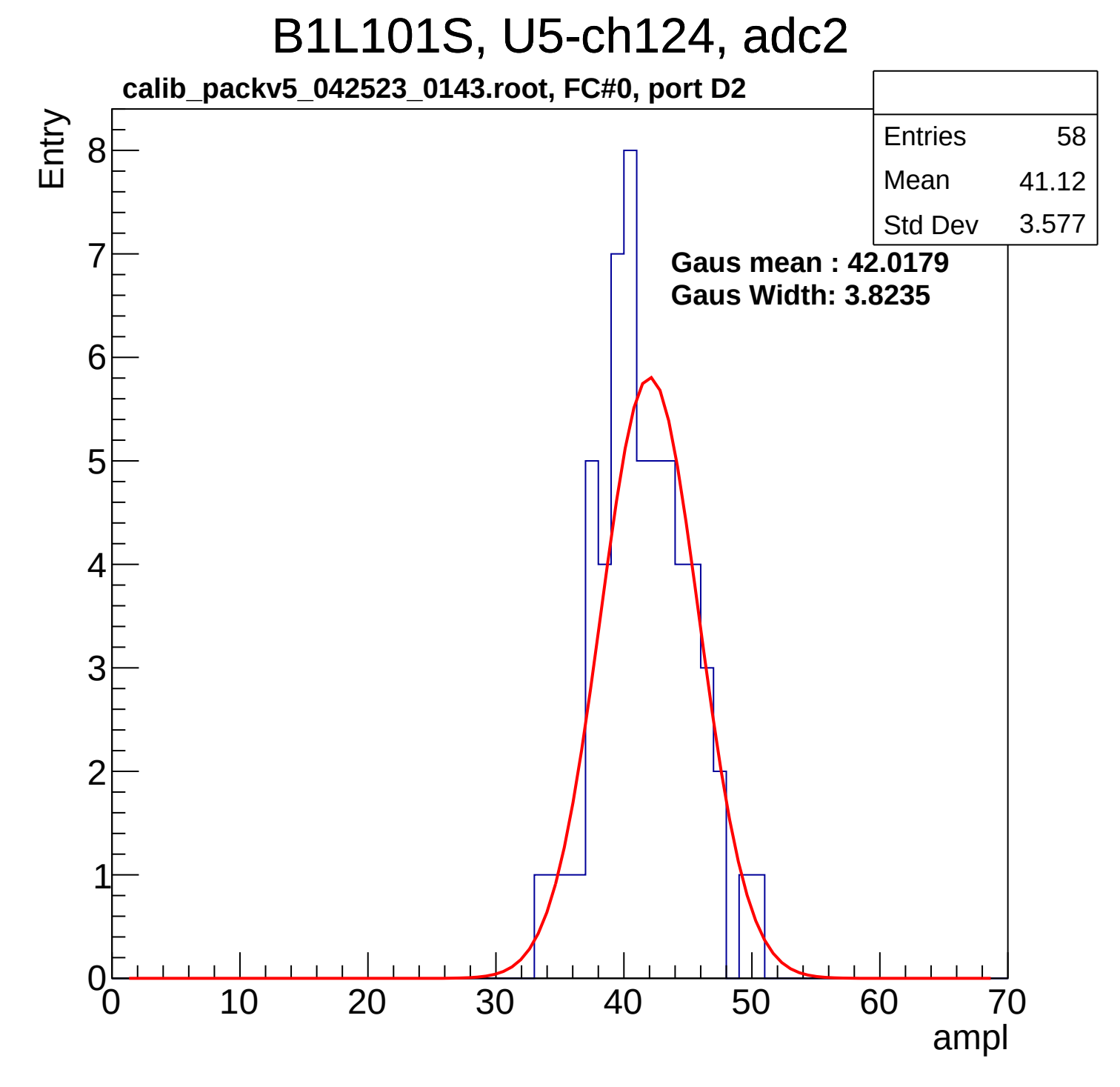
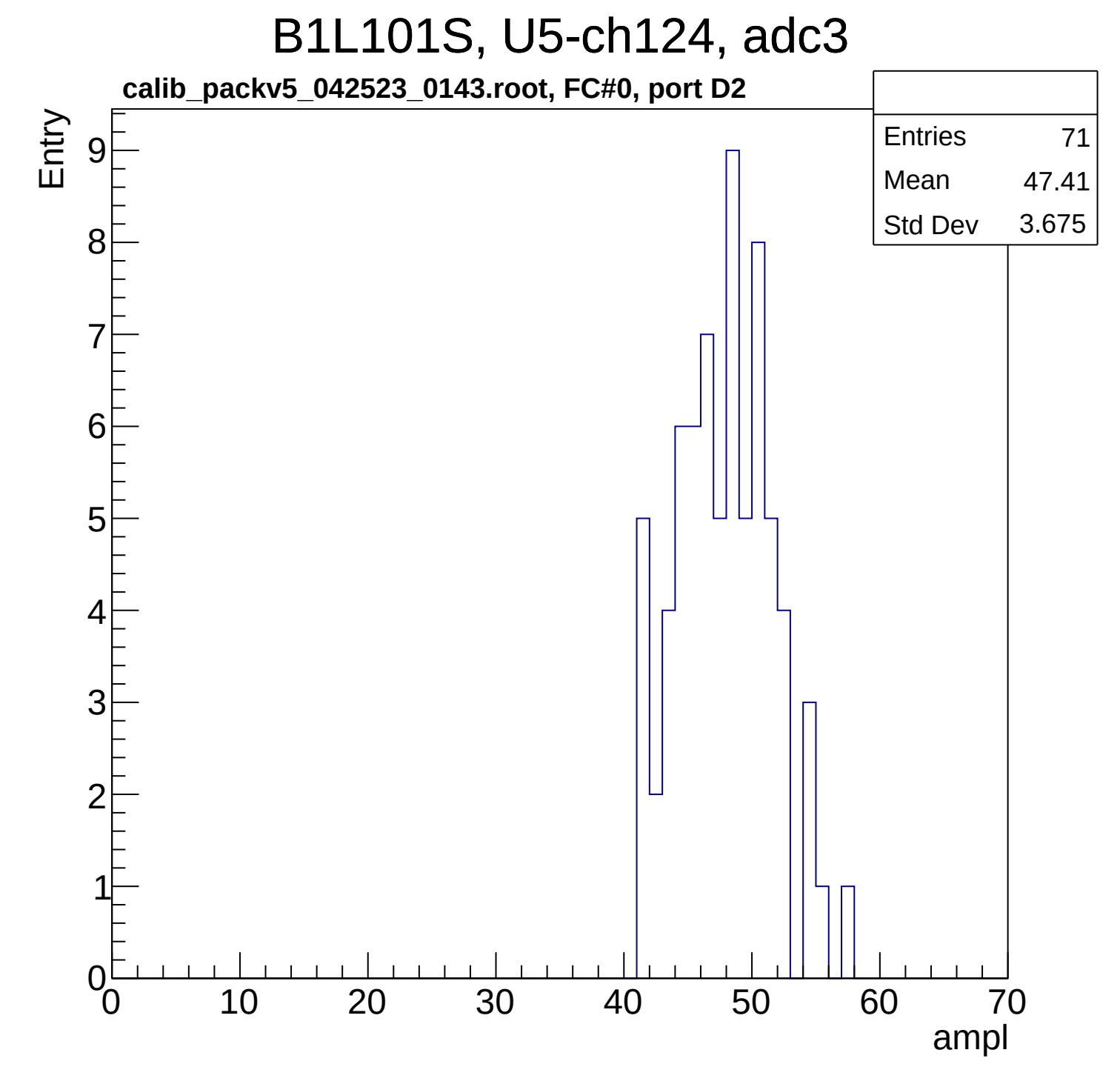
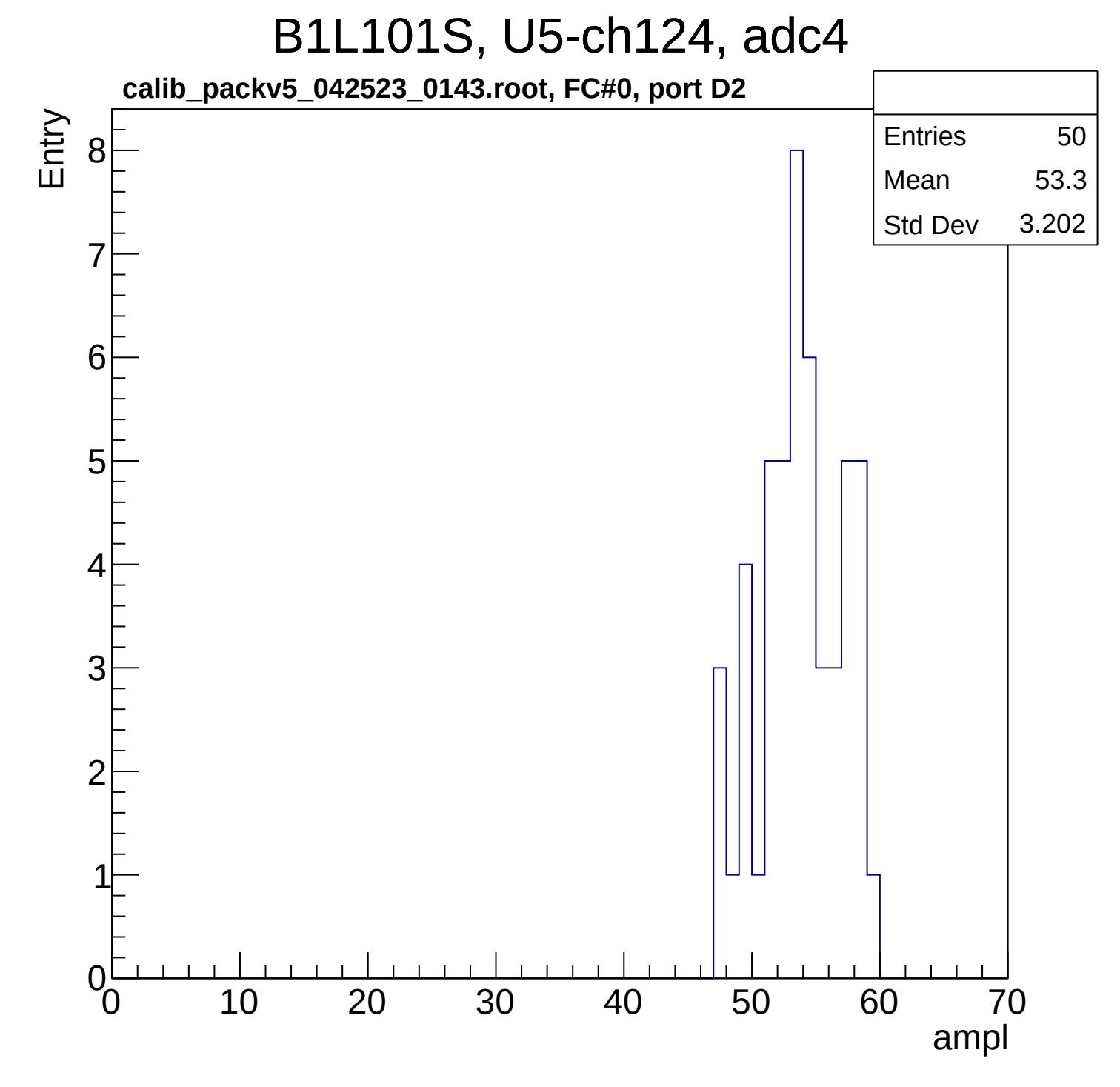

B1L101S, U5-ch124, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 41.12
Std Dev 3.577
Gaus mean : 42.0179
Gaus Width: 3.8235
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch124, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 47.41
Std Dev 3.675
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch124, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 53.3
Std Dev 3.202
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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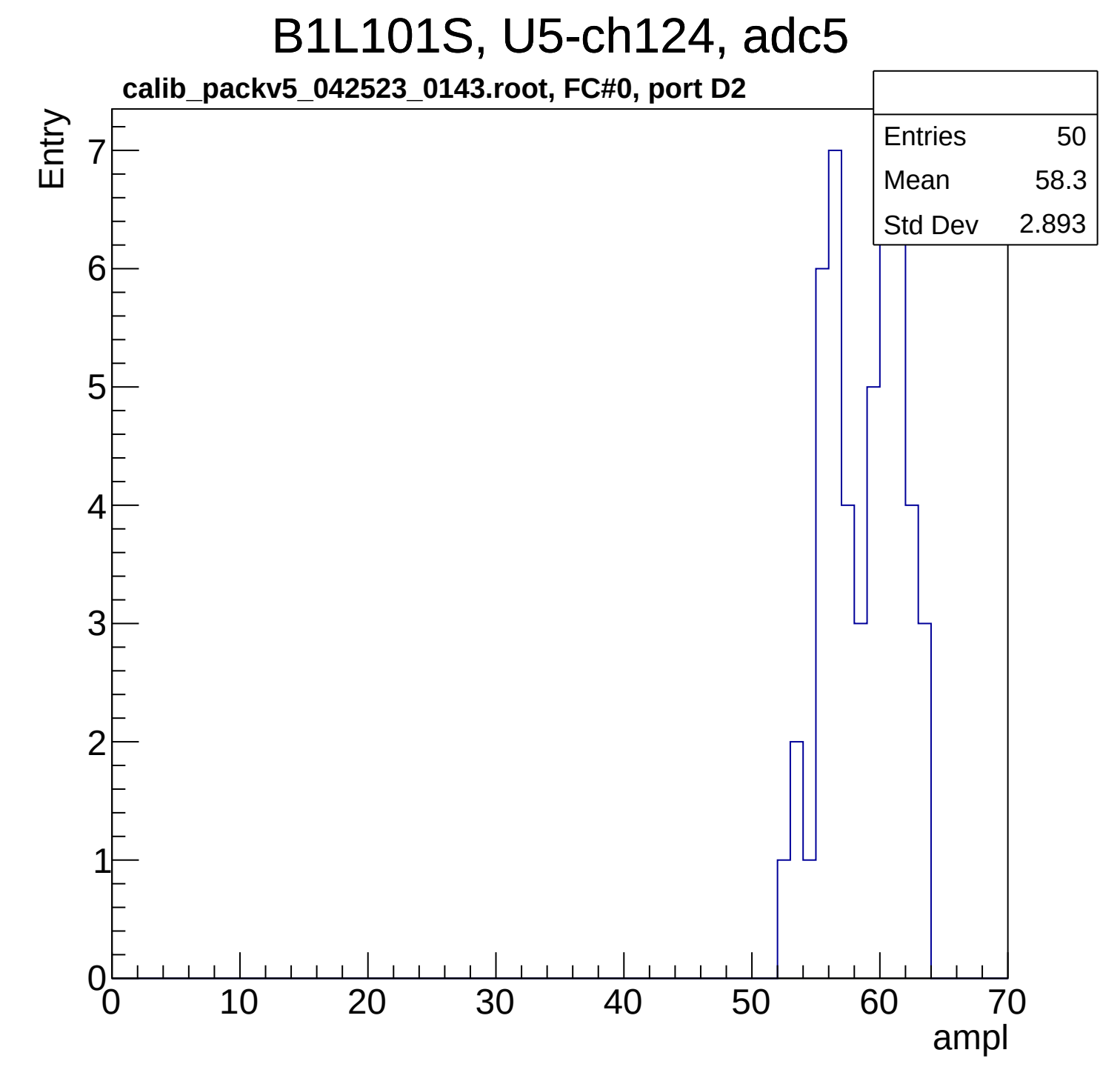
40
50
60
70


B1L101S, U5-ch124, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 58.3
Std Dev 2.893
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
30
40
50
60
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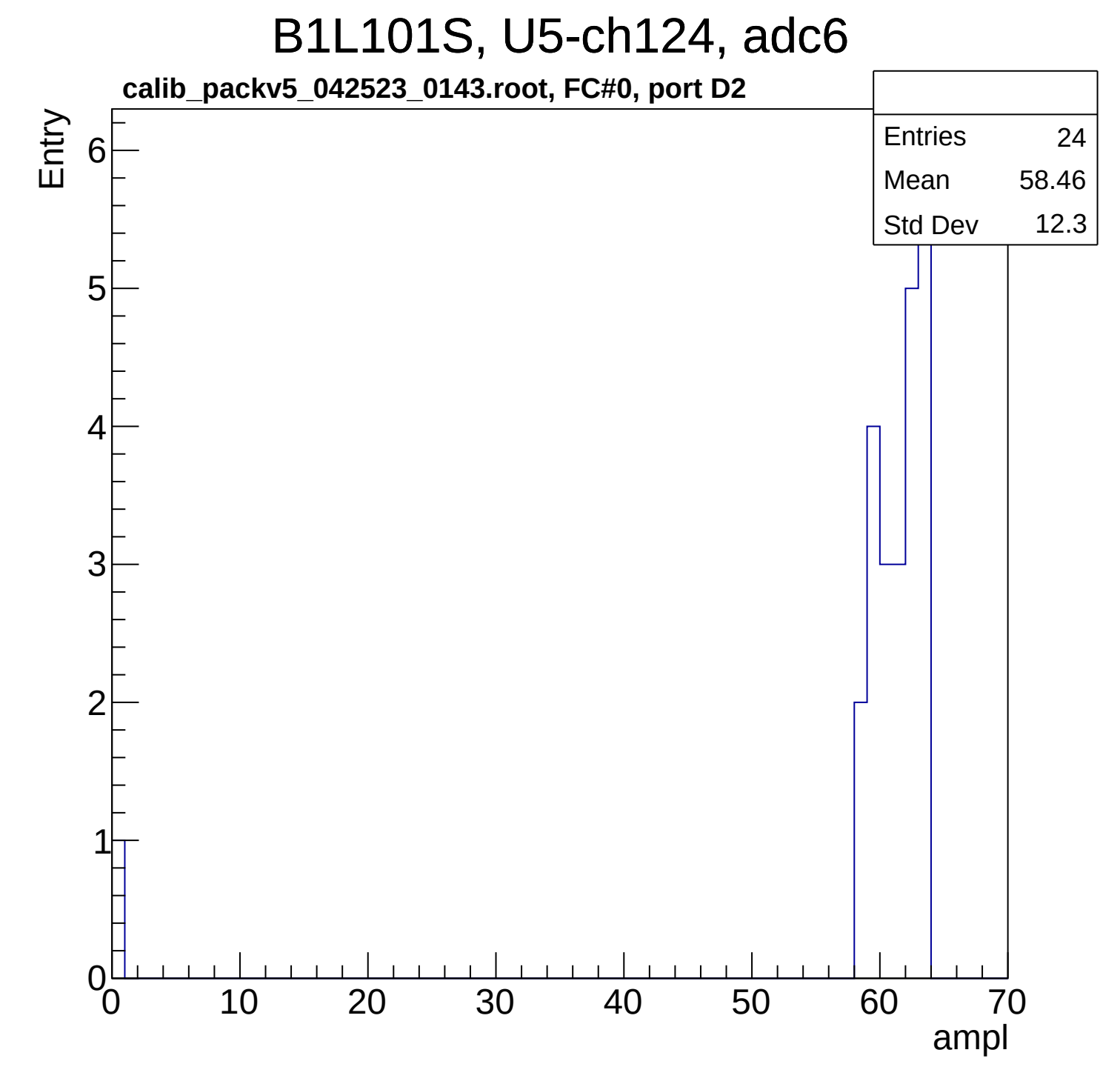
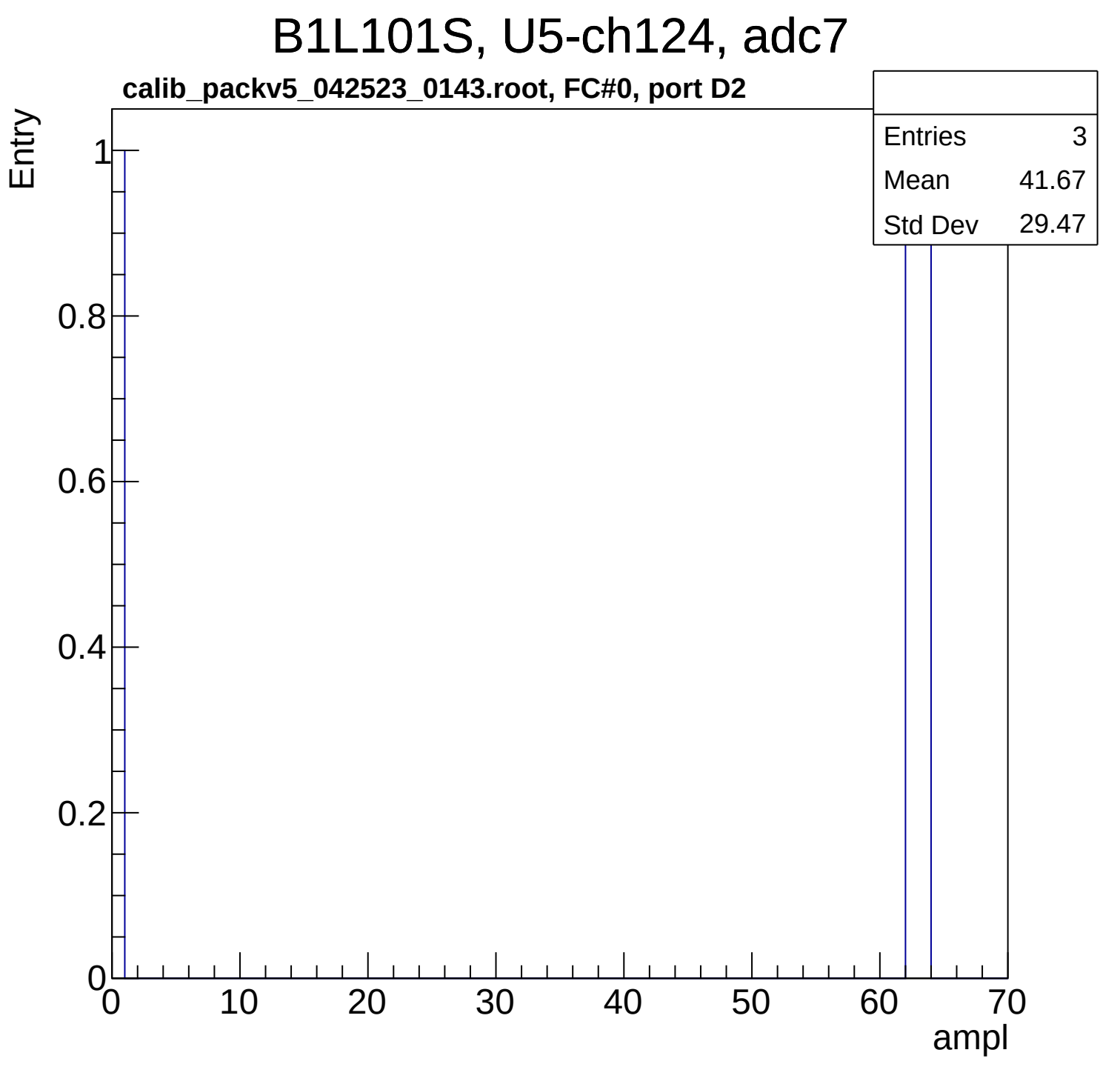

B1L101S, U5-ch124, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 24
Mean 58.46
Std Dev 12.3
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L101S, U5-ch124, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 41.67
Std Dev 29.47
Entry
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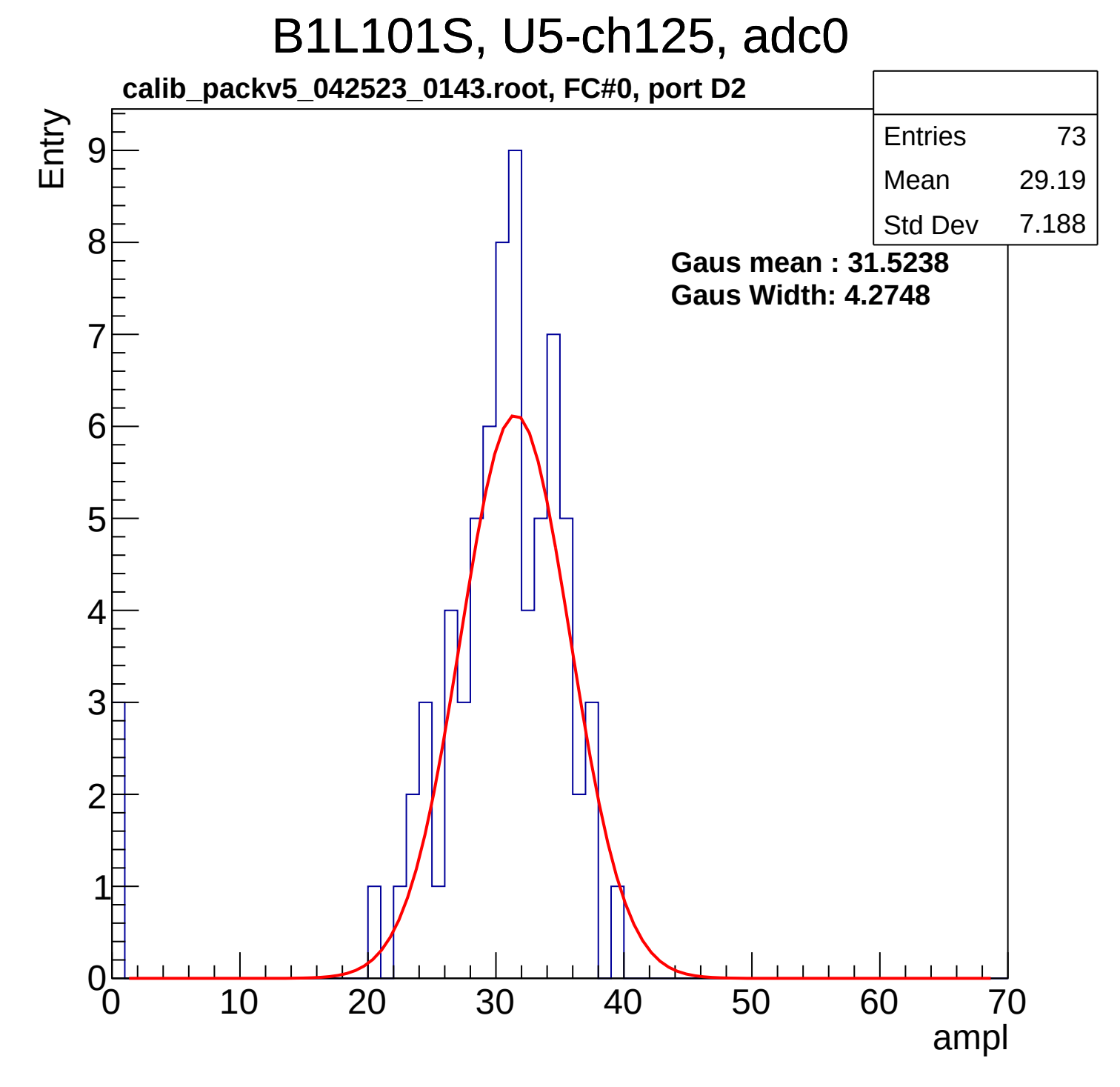
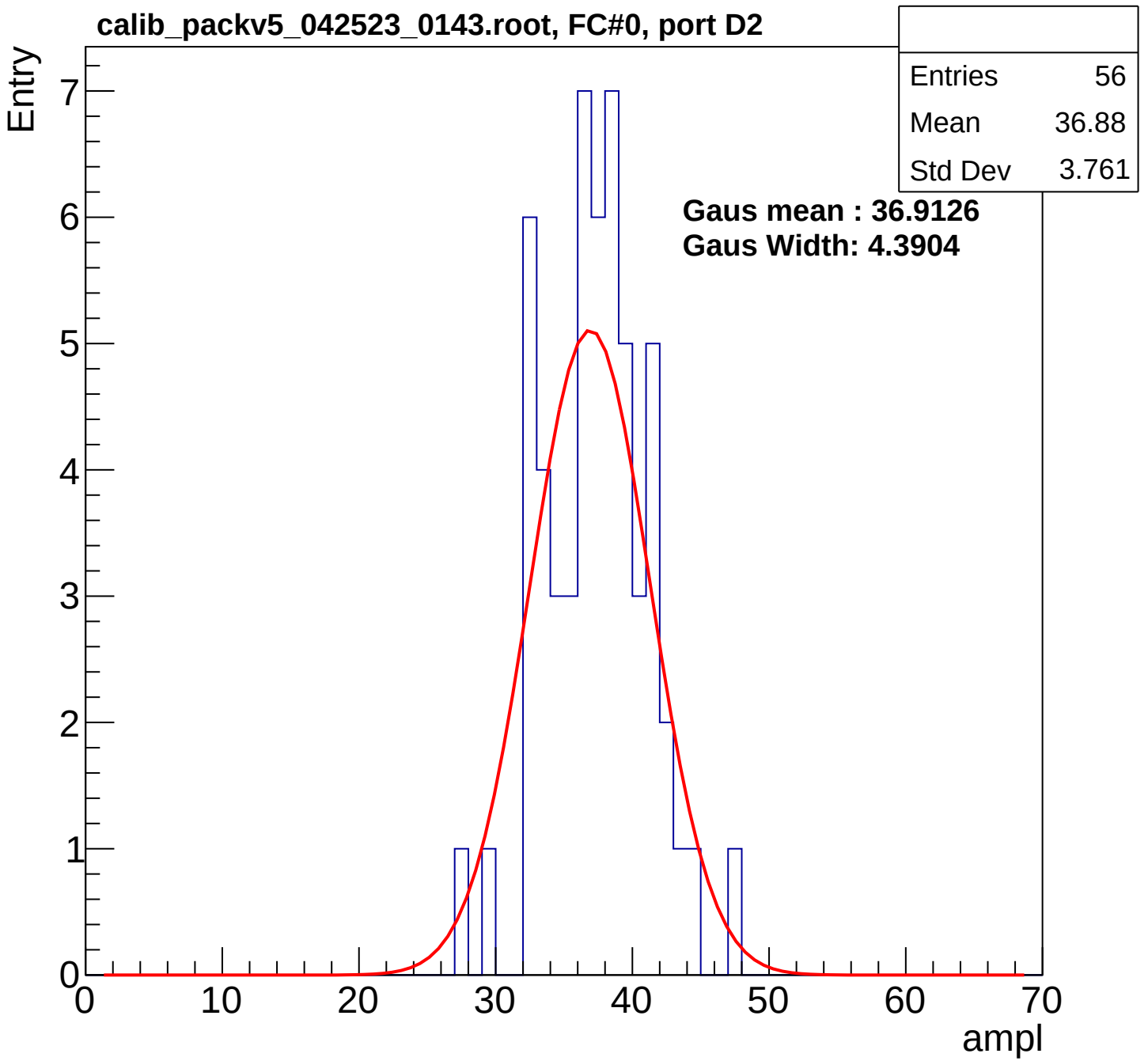
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch125, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 29.19
Std Dev 7.188
Gaus mean : 31.5238
Gaus Width: 4.2748
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch125, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 36.88
Std Dev 3.761
Gaus mean : 36.9126
Gaus Width: 4.3904
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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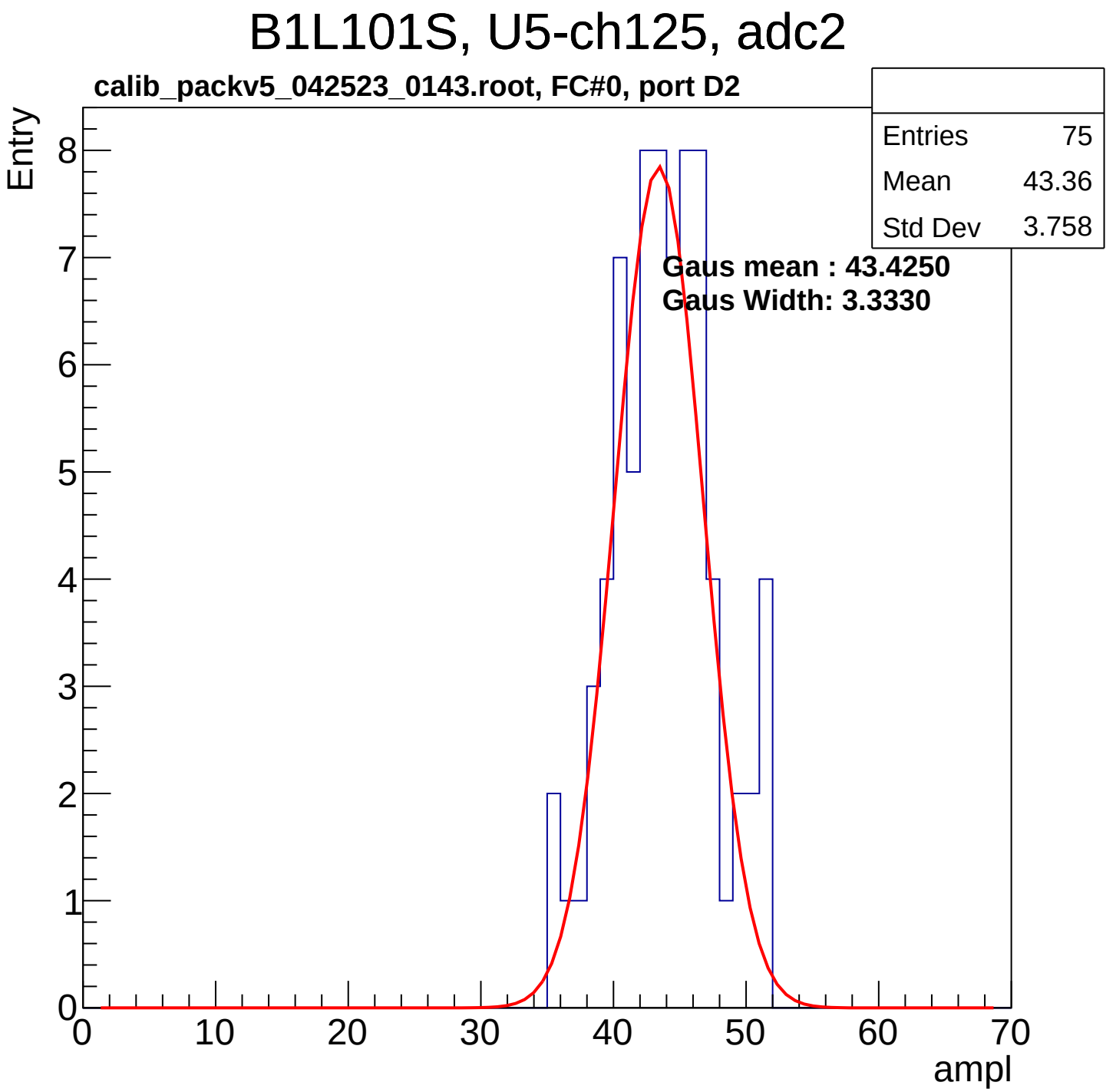
B1L101S, U5-ch125, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 43.36
Std Dev 3.758
Gaus mean : 43.4250
Gaus Width: 3.3330
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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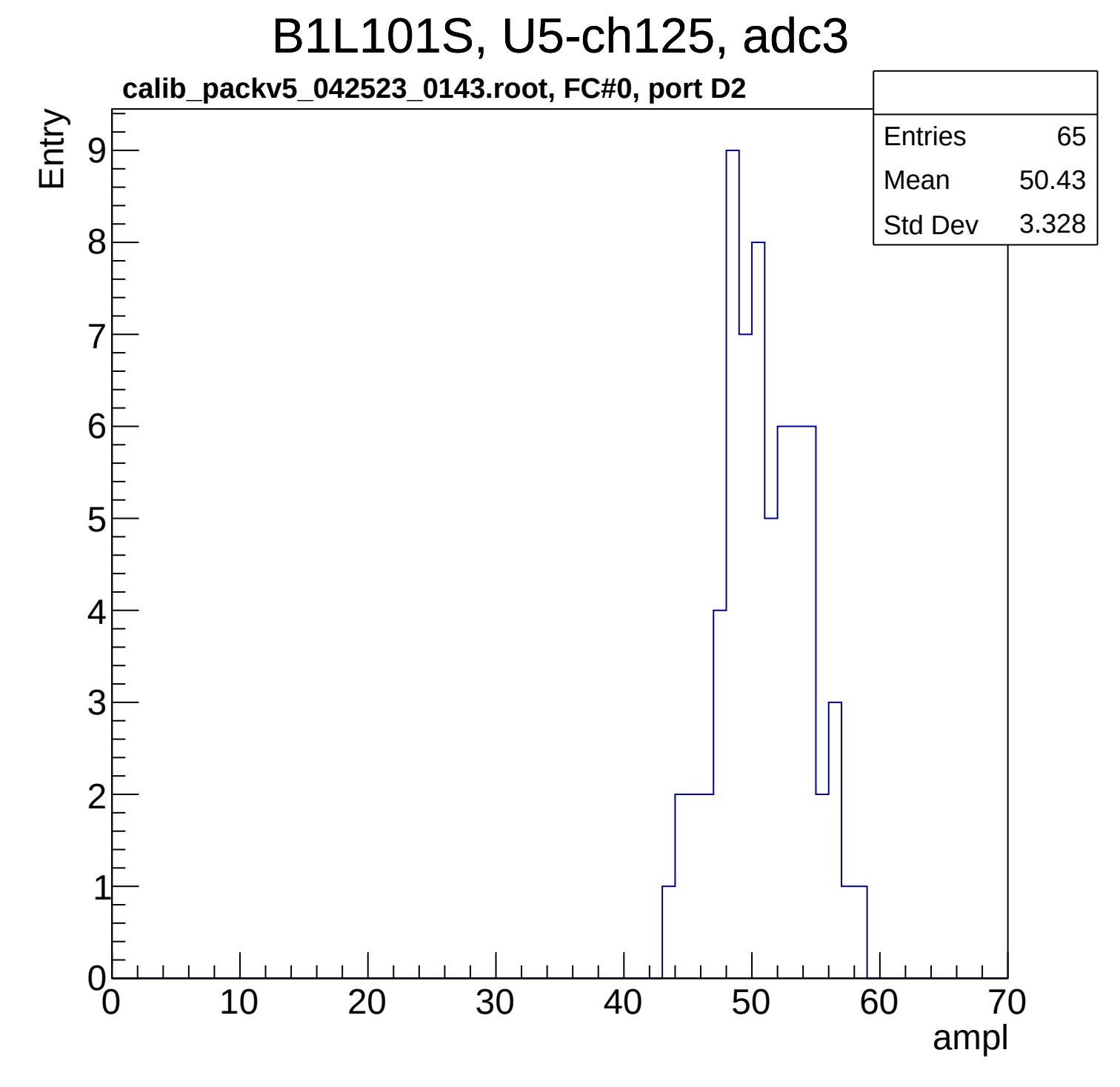
B1L101S, U5-ch125, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 50.43
Std Dev 3.328
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
50
60
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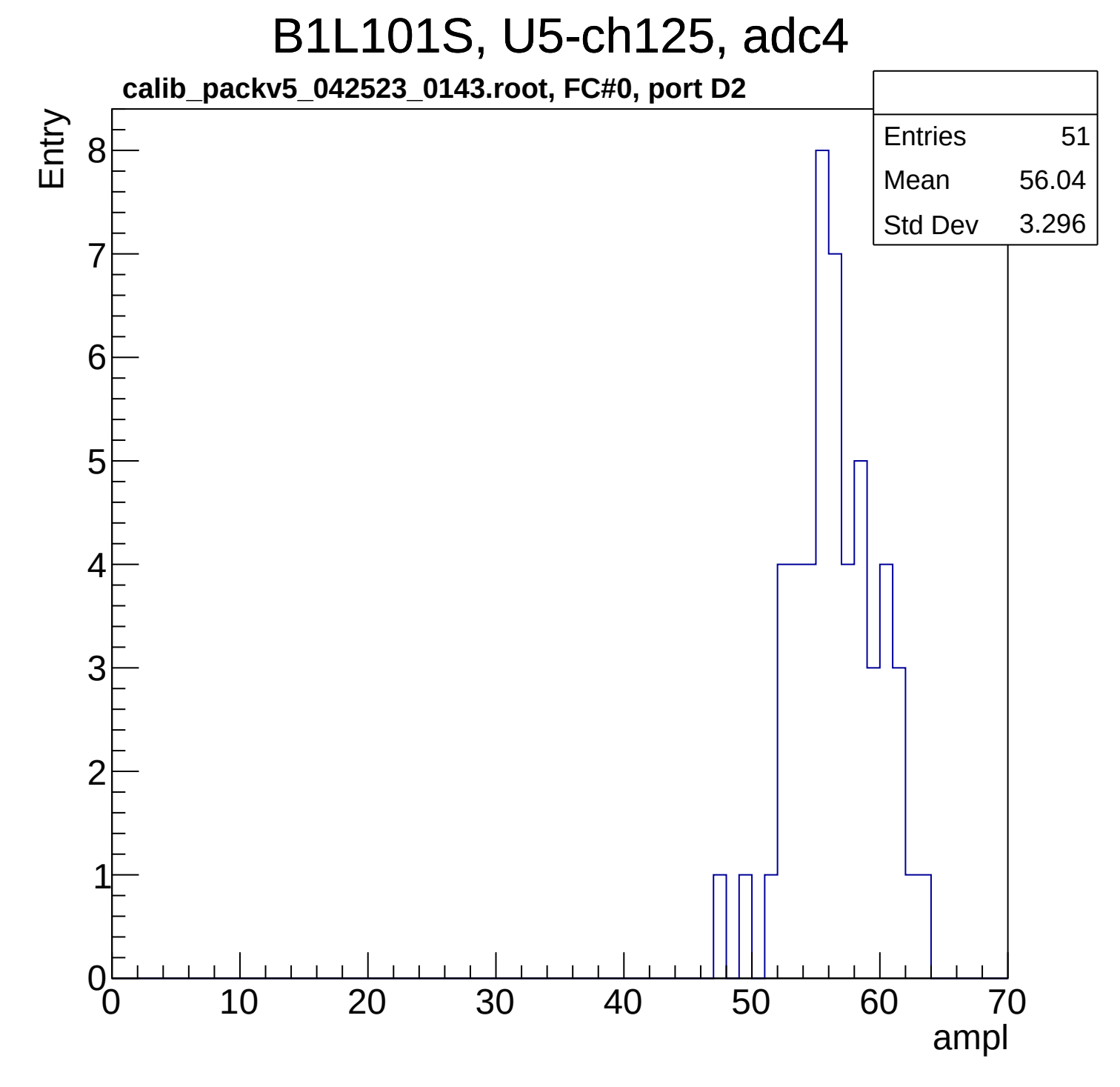
B1L101S, U5-ch125, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 56.04
Std Dev 3.296
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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40
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60
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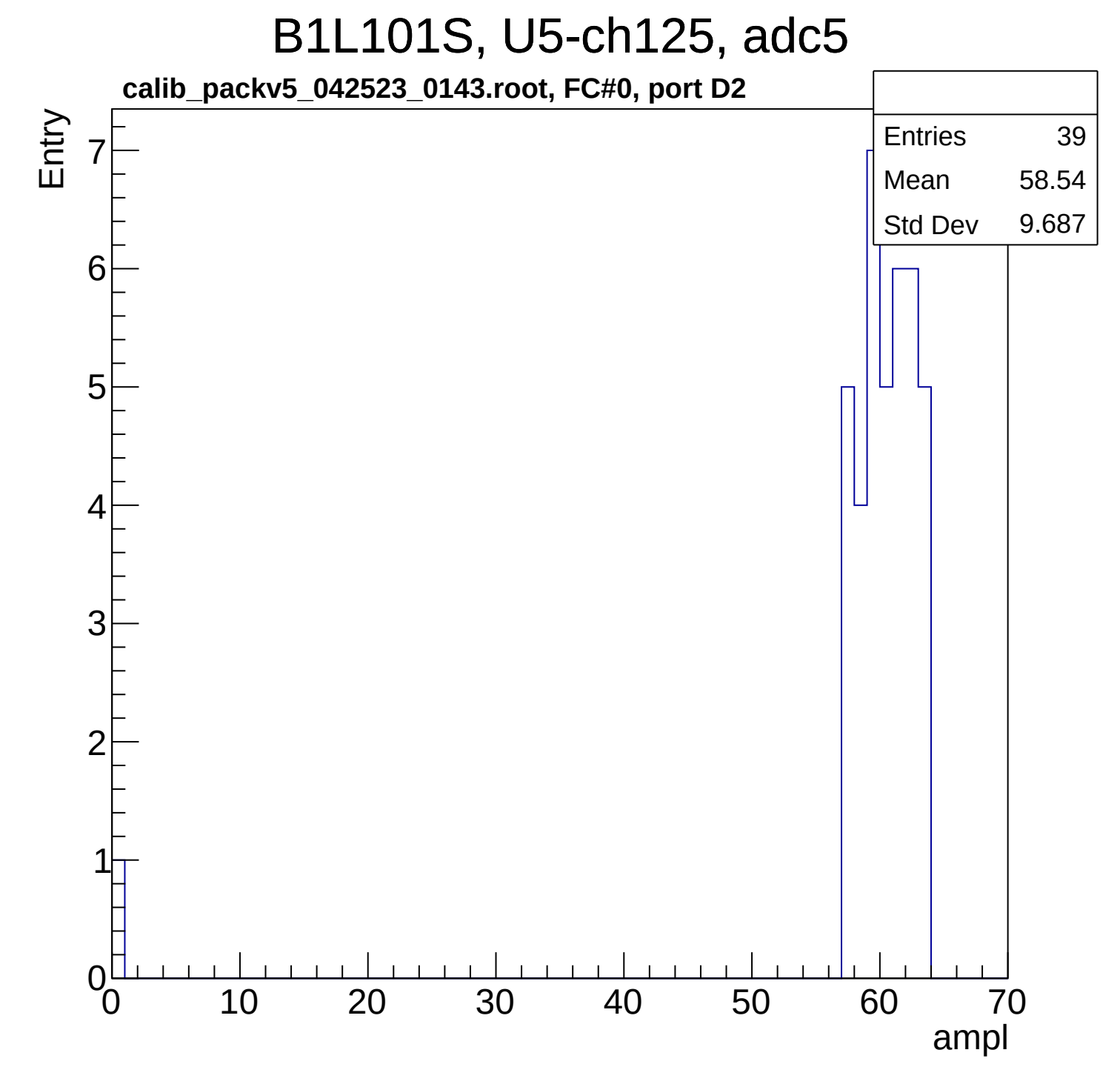
B1L101S, U5-ch125, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 39
Mean 58.54
Std Dev 9.687
Entry
ampl
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1
2
3
4
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6
7
0
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20
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60
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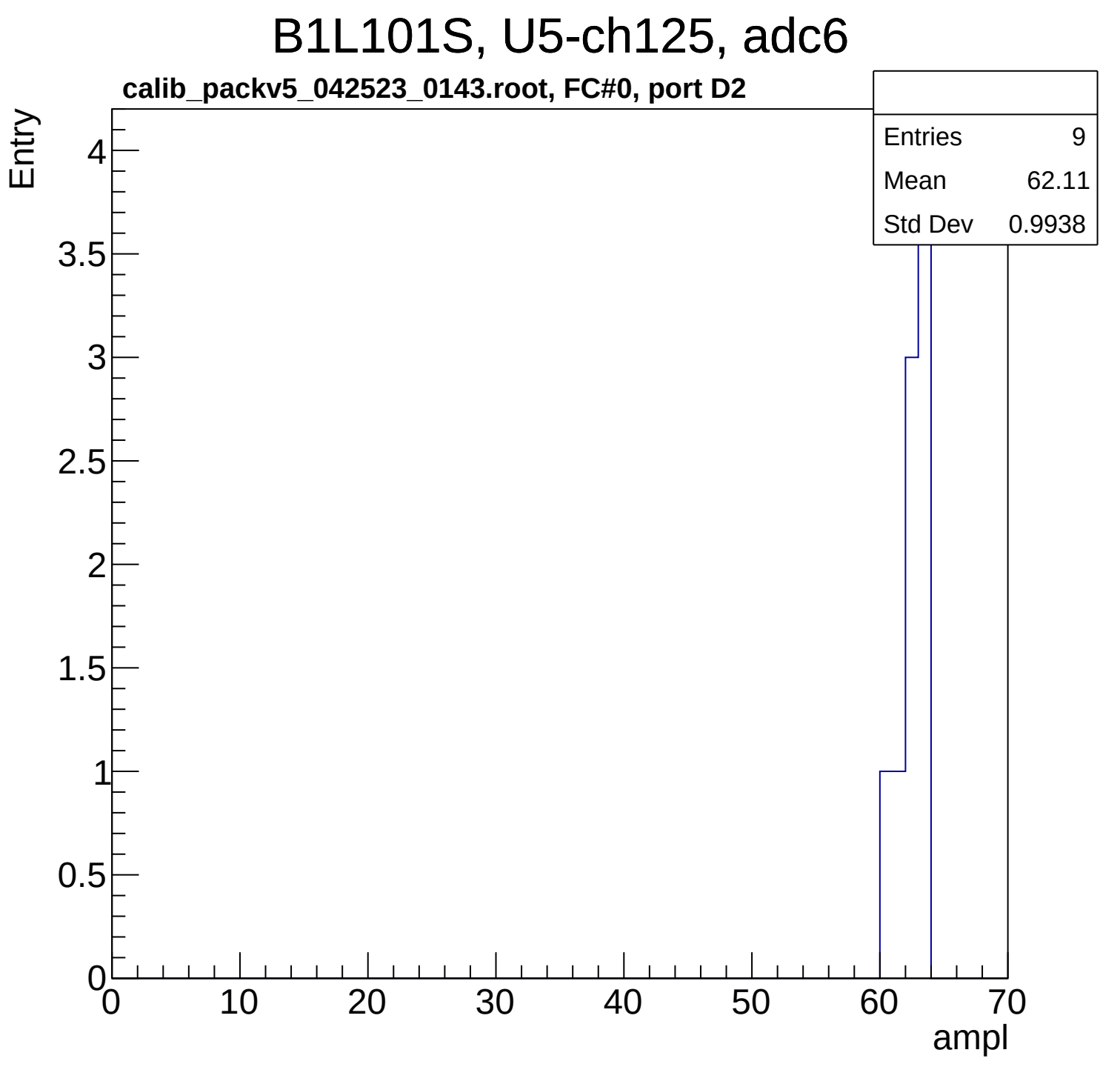
B1L101S, U5-ch125, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 62.11
Std Dev 0.9938
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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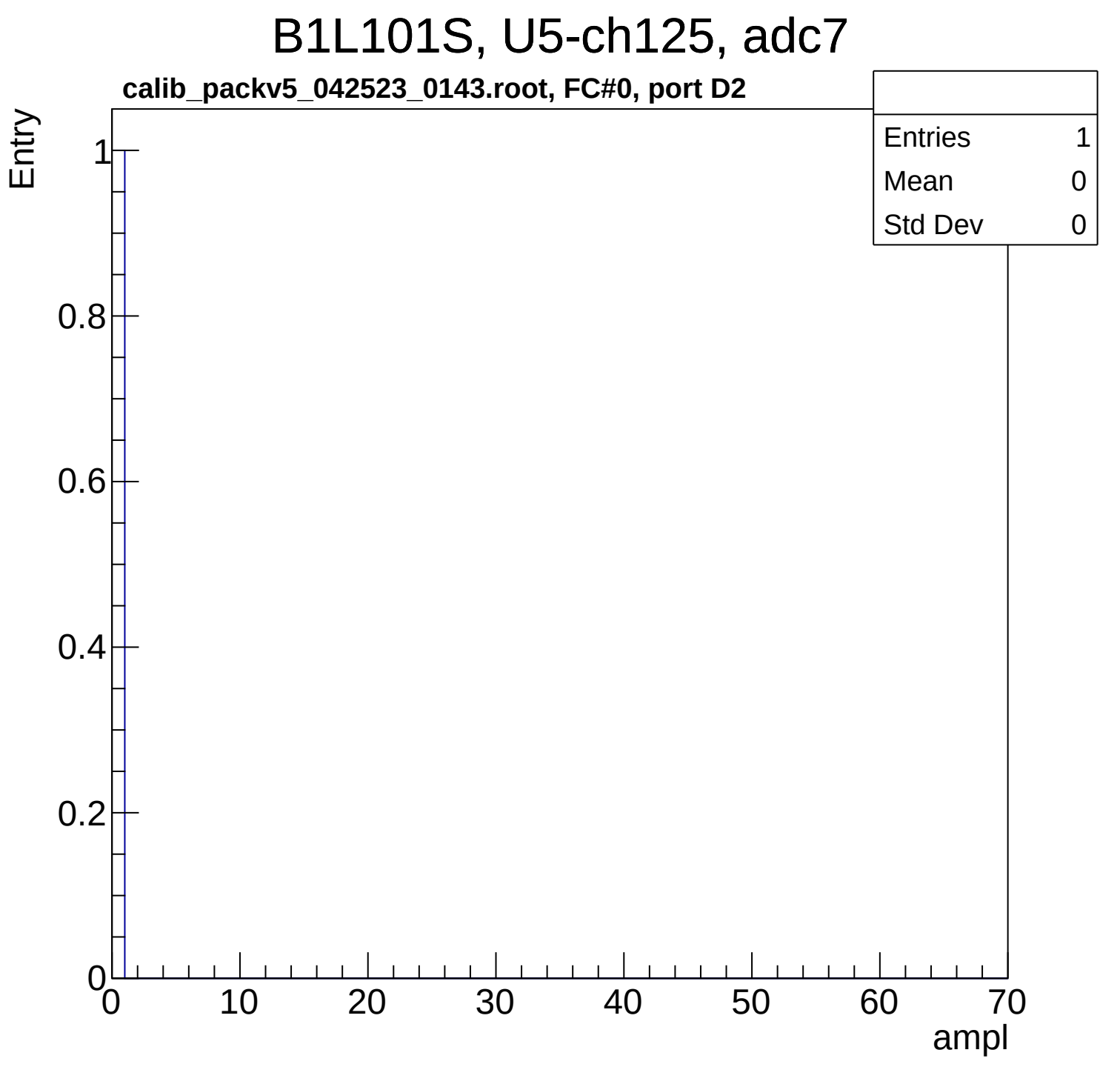
40
50
60
70


B1L101S, U5-ch125, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
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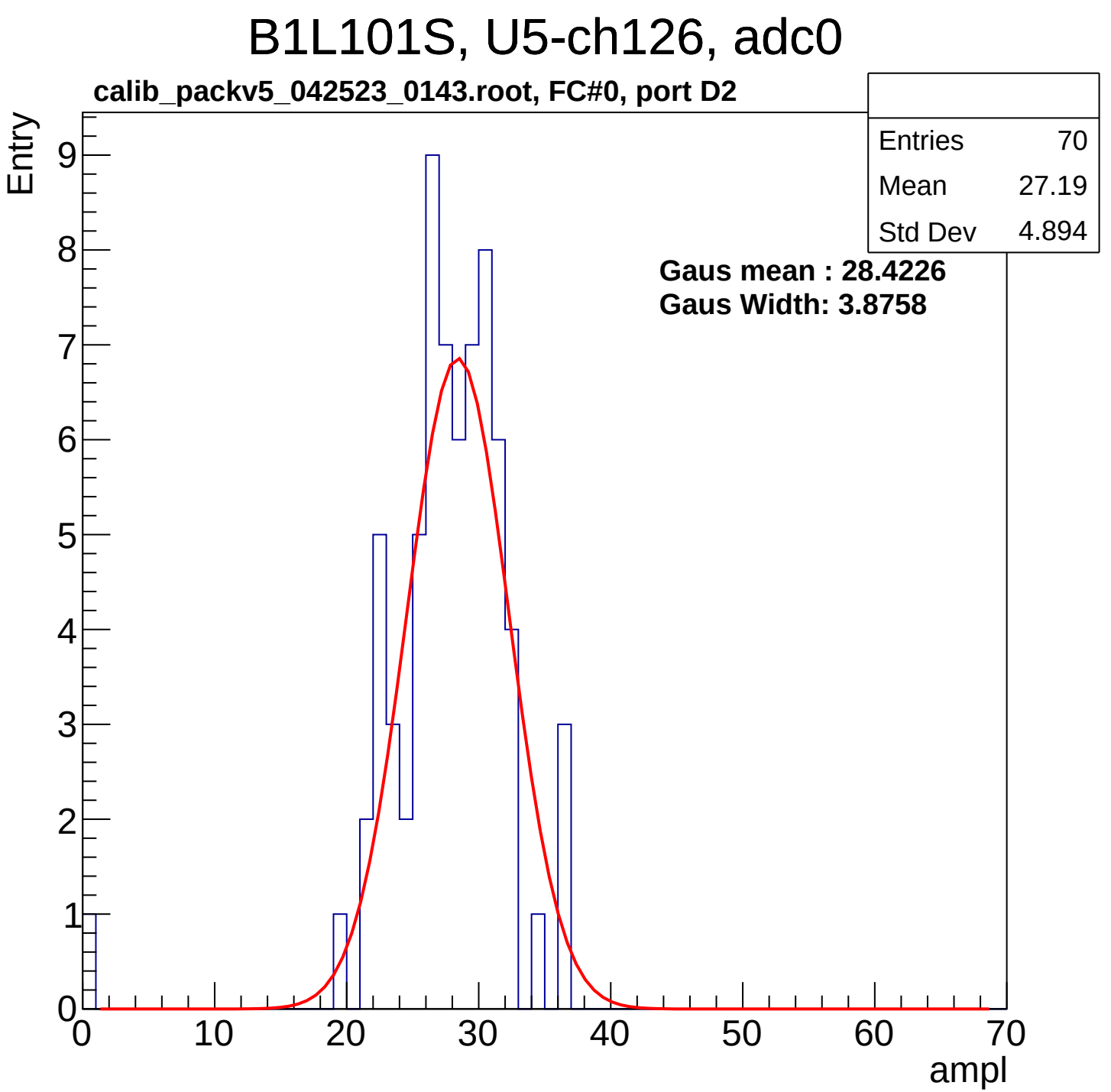
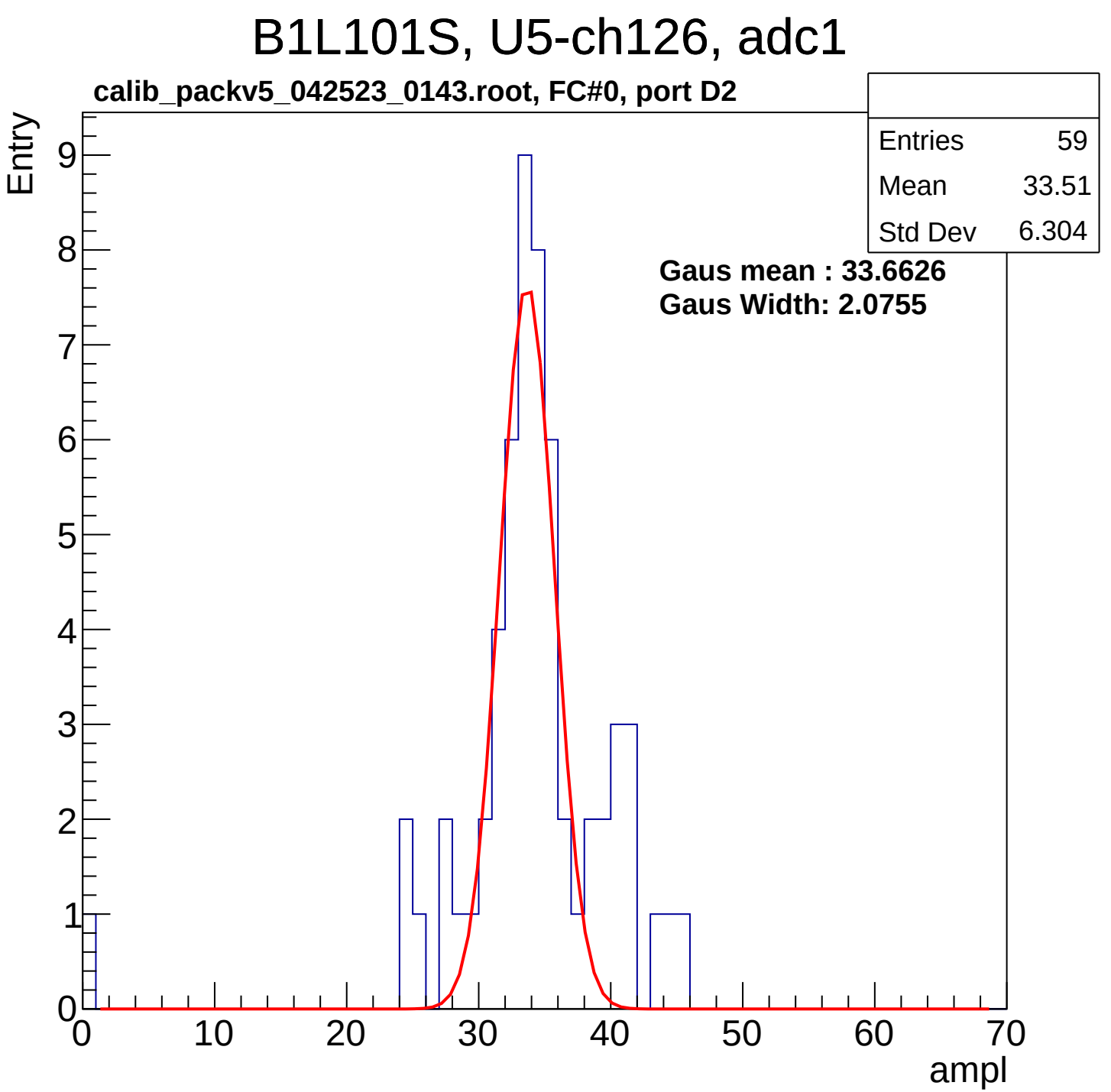
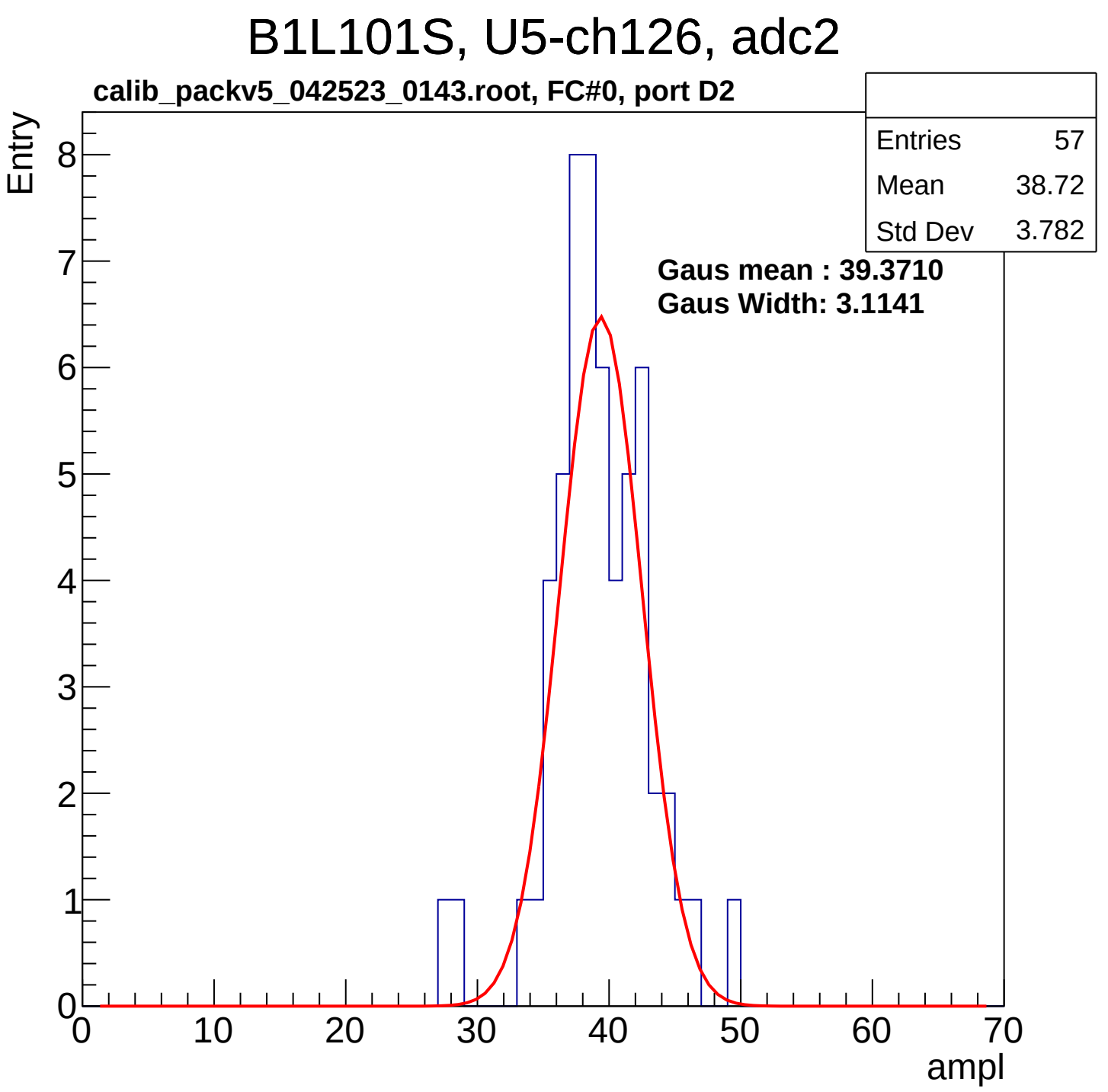
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch126, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 27.19
Std Dev 4.894
Gaus mean : 28.4226
Gaus Width: 3.8758
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch126, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 33.51
Std Dev 6.304
Gaus mean : 33.6626
Gaus Width: 2.0755
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U5-ch126, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 38.72
Std Dev 3.782
Gaus mean : 39.3710
Gaus Width: 3.1141
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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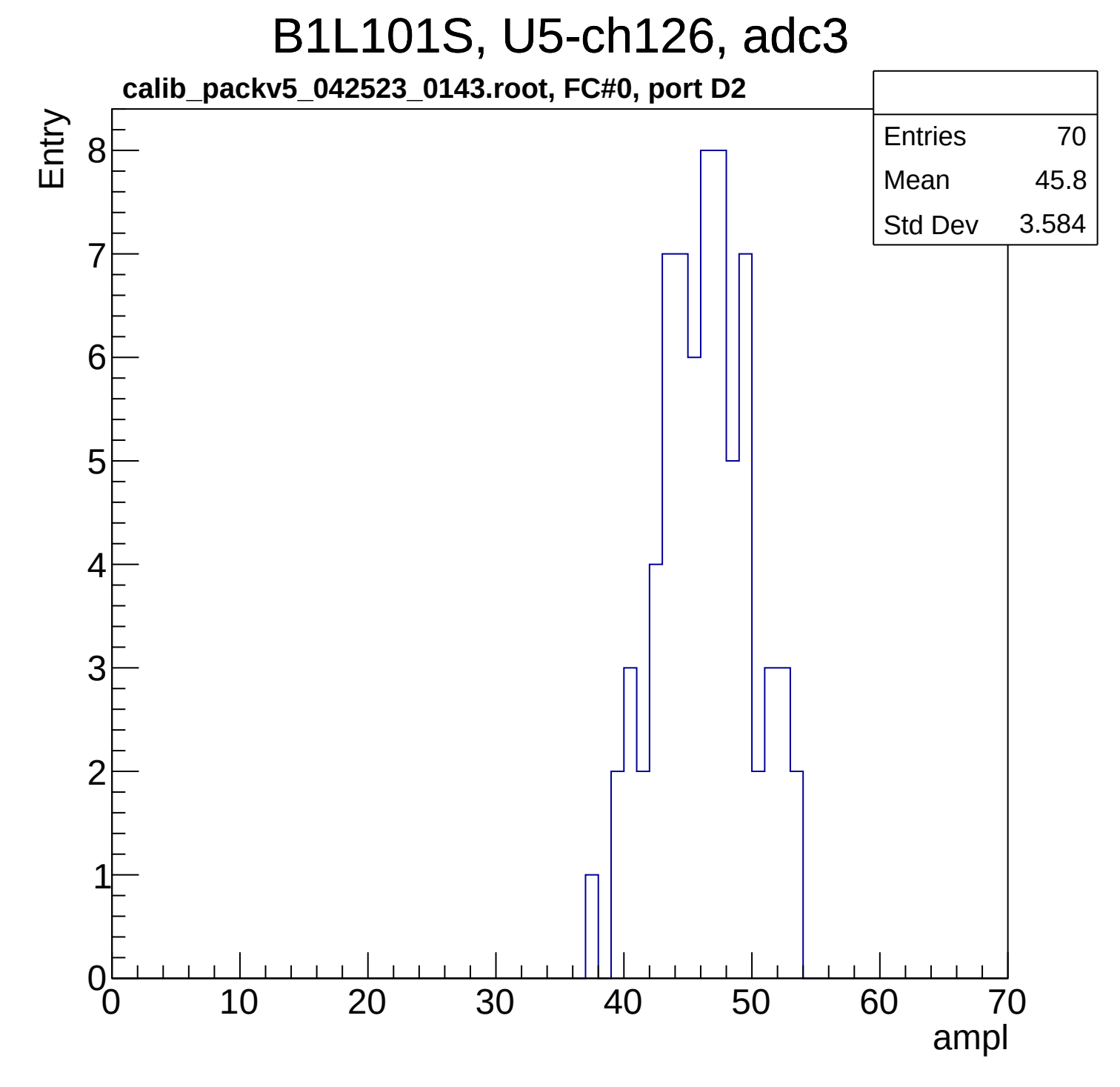
B1L101S, U5-ch126, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 45.8
Std Dev 3.584
Entry
ampl
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1
2
3
4
5
6
7
8
0
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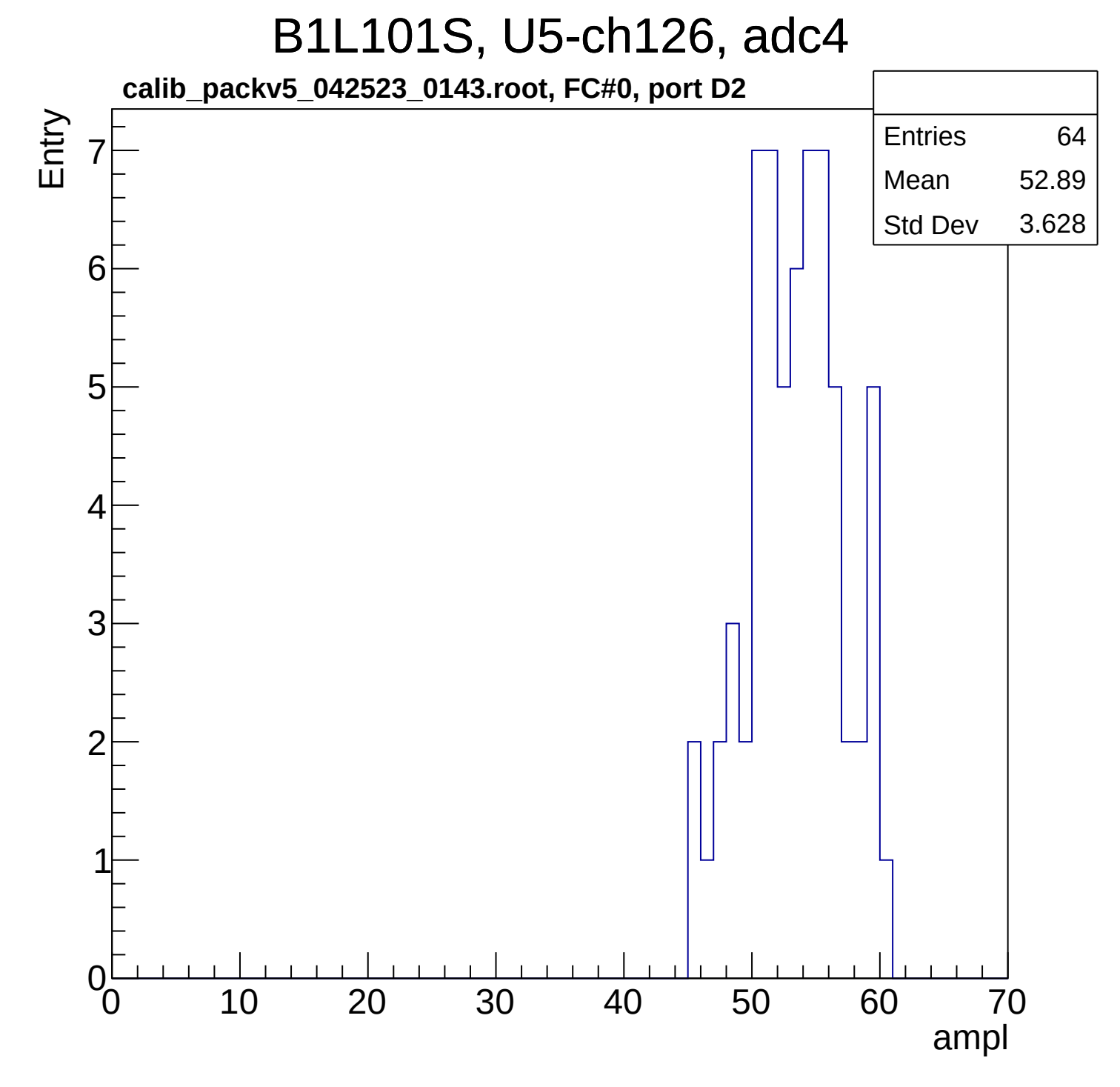
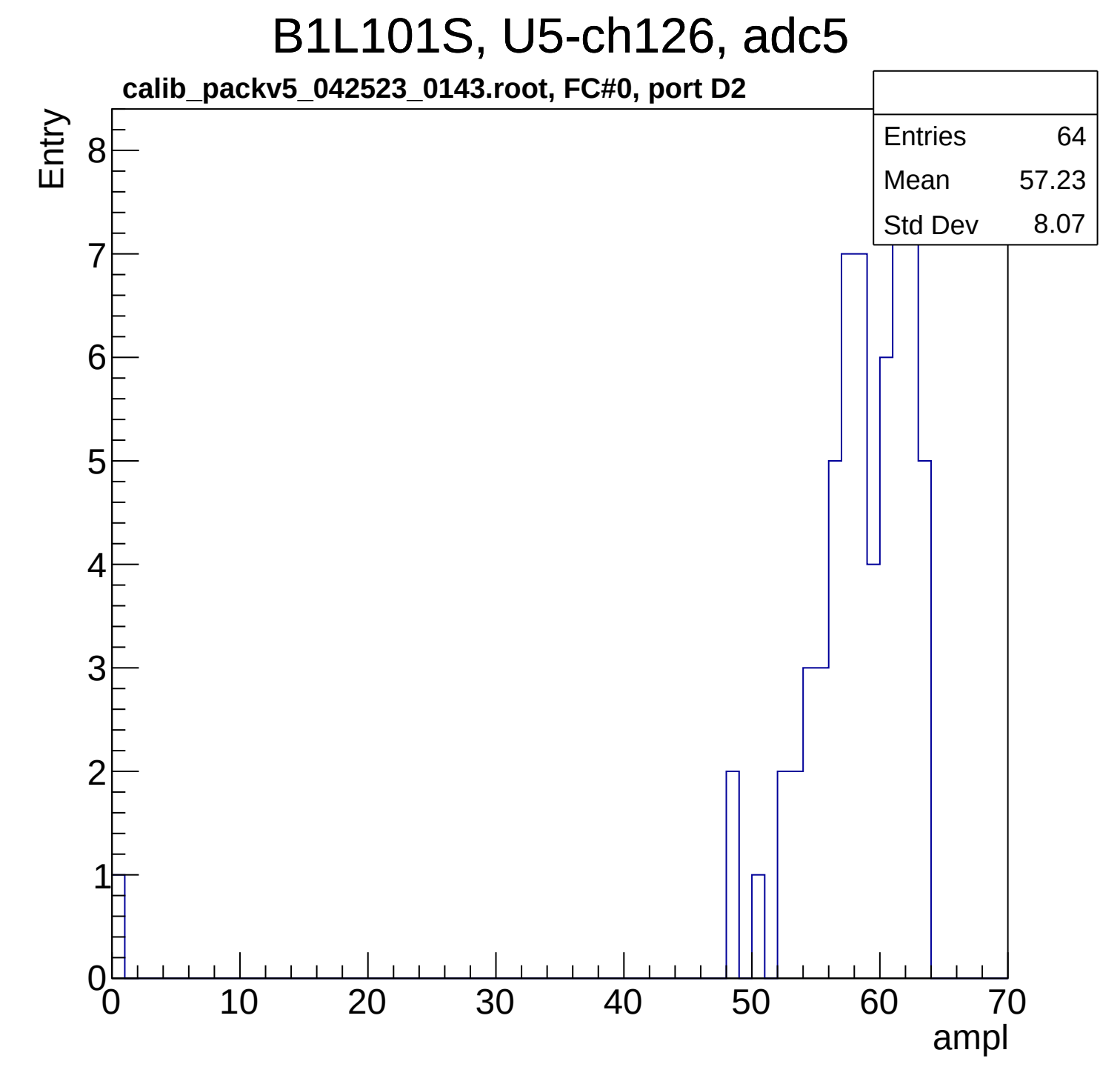
60
70


B1L101S, U5-ch126, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 52.89
Std Dev 3.628
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U5-ch126, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 57.23
Std Dev 8.07
Entry
ampl
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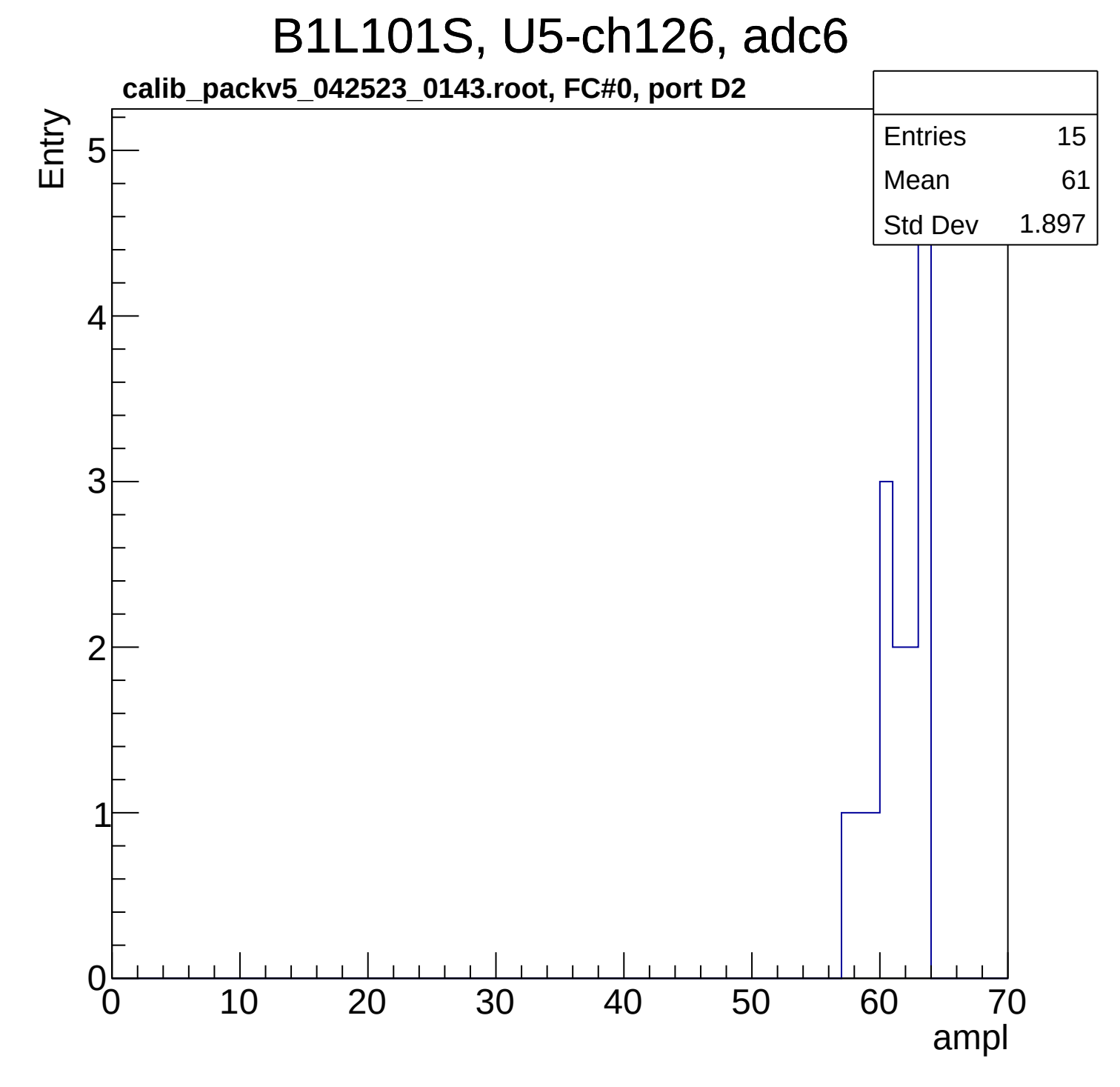
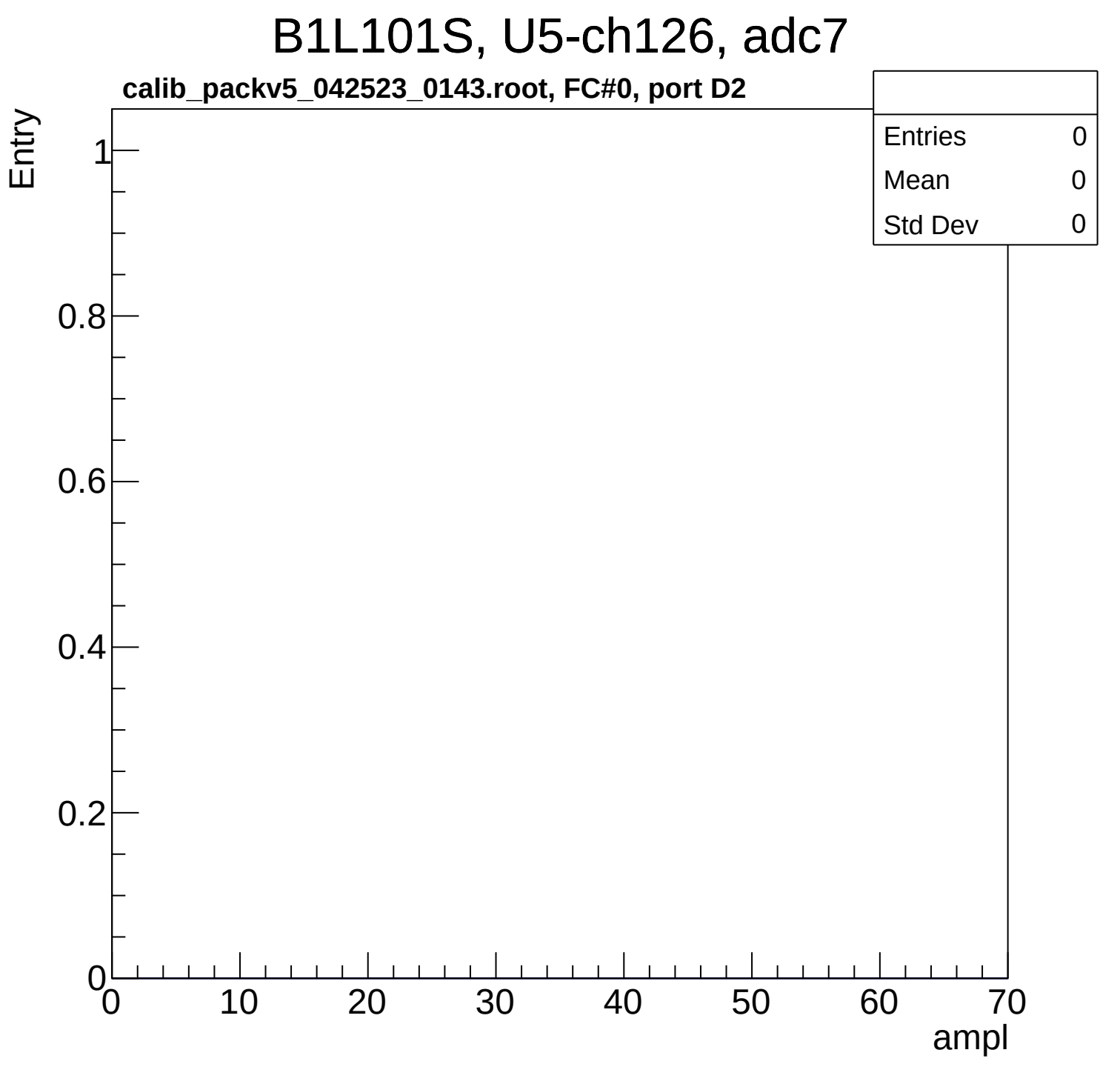
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch126, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 15
Mean 61
Std Dev 1.897
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L101S, U5-ch126, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
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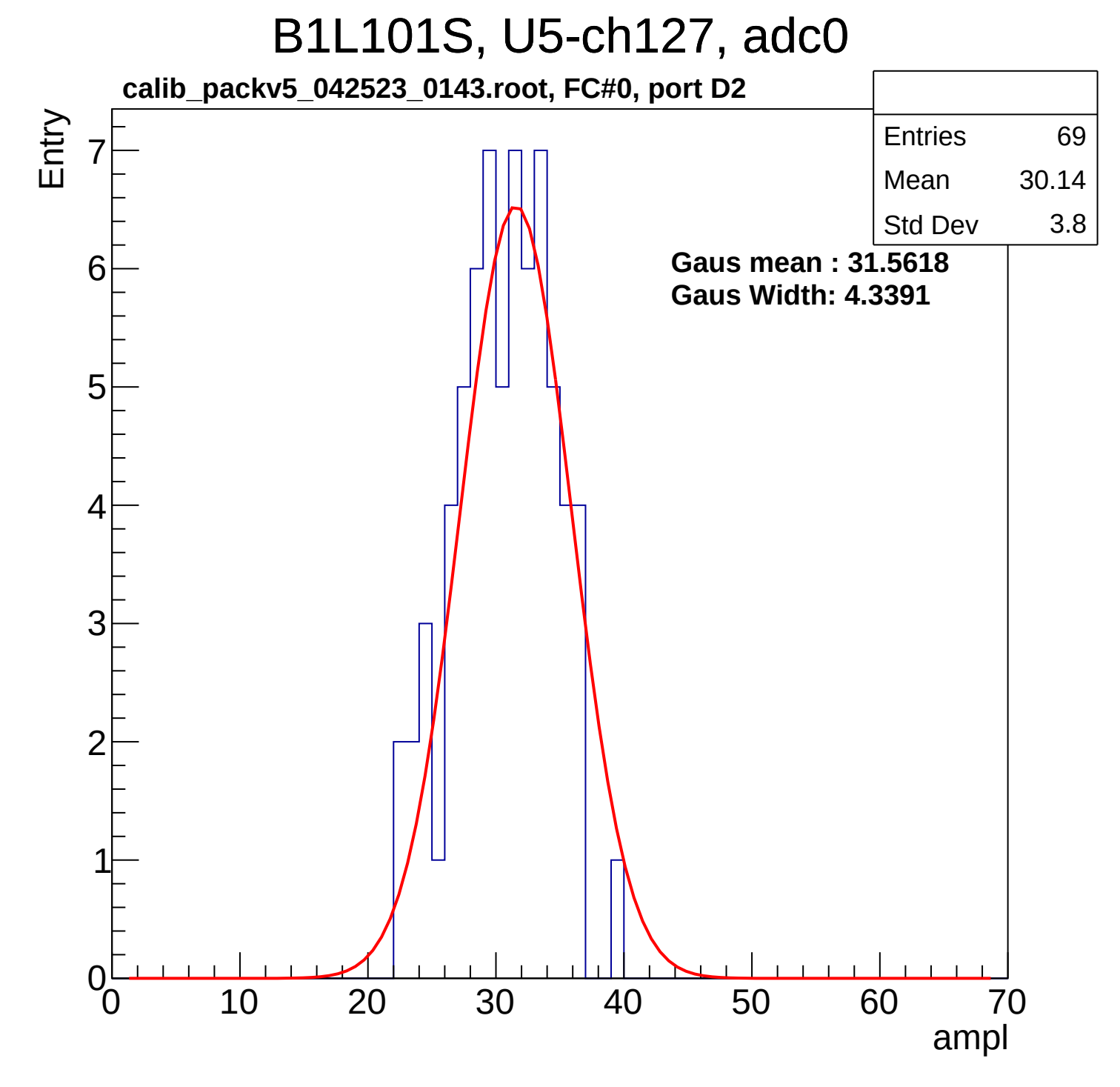
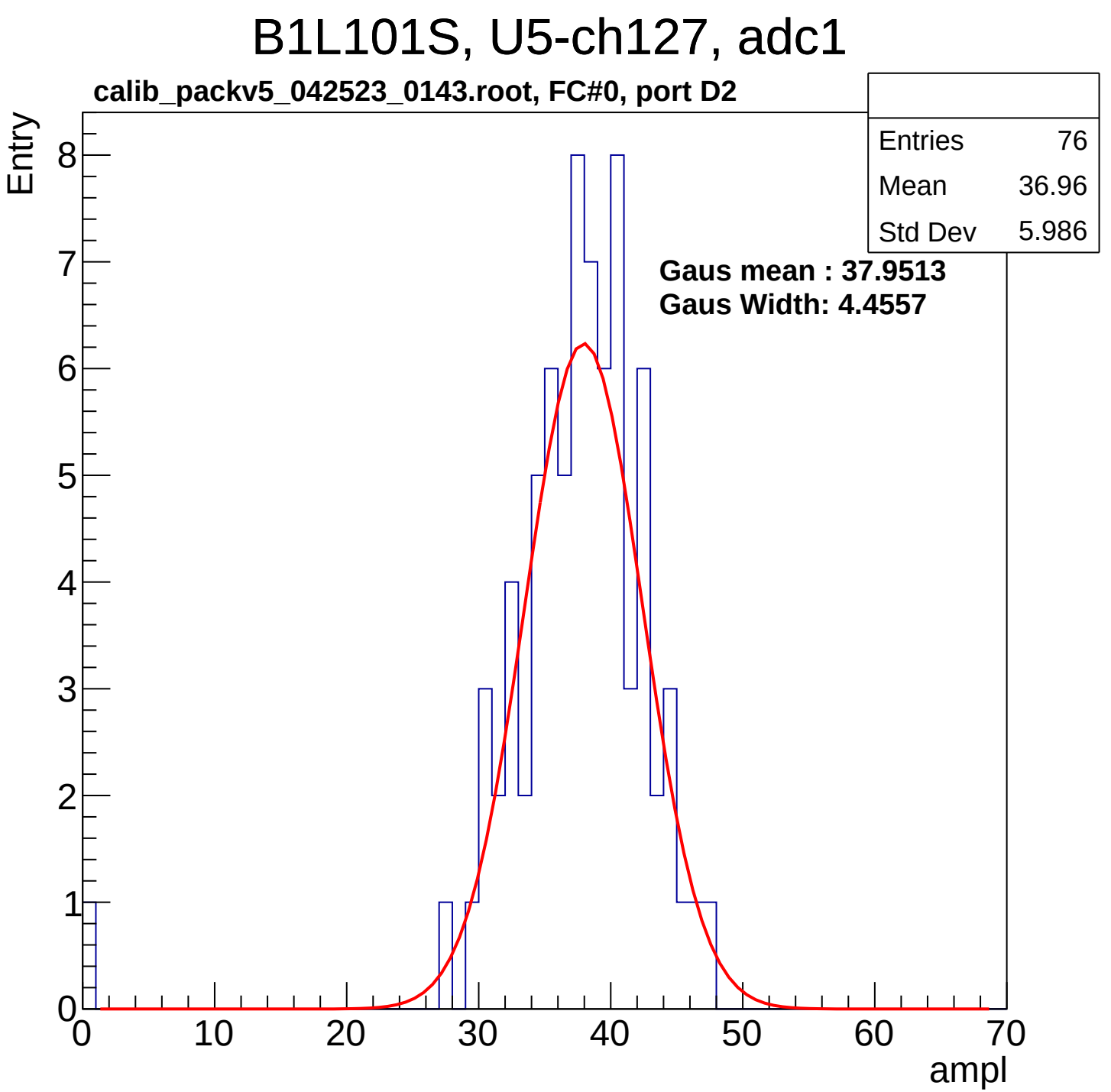
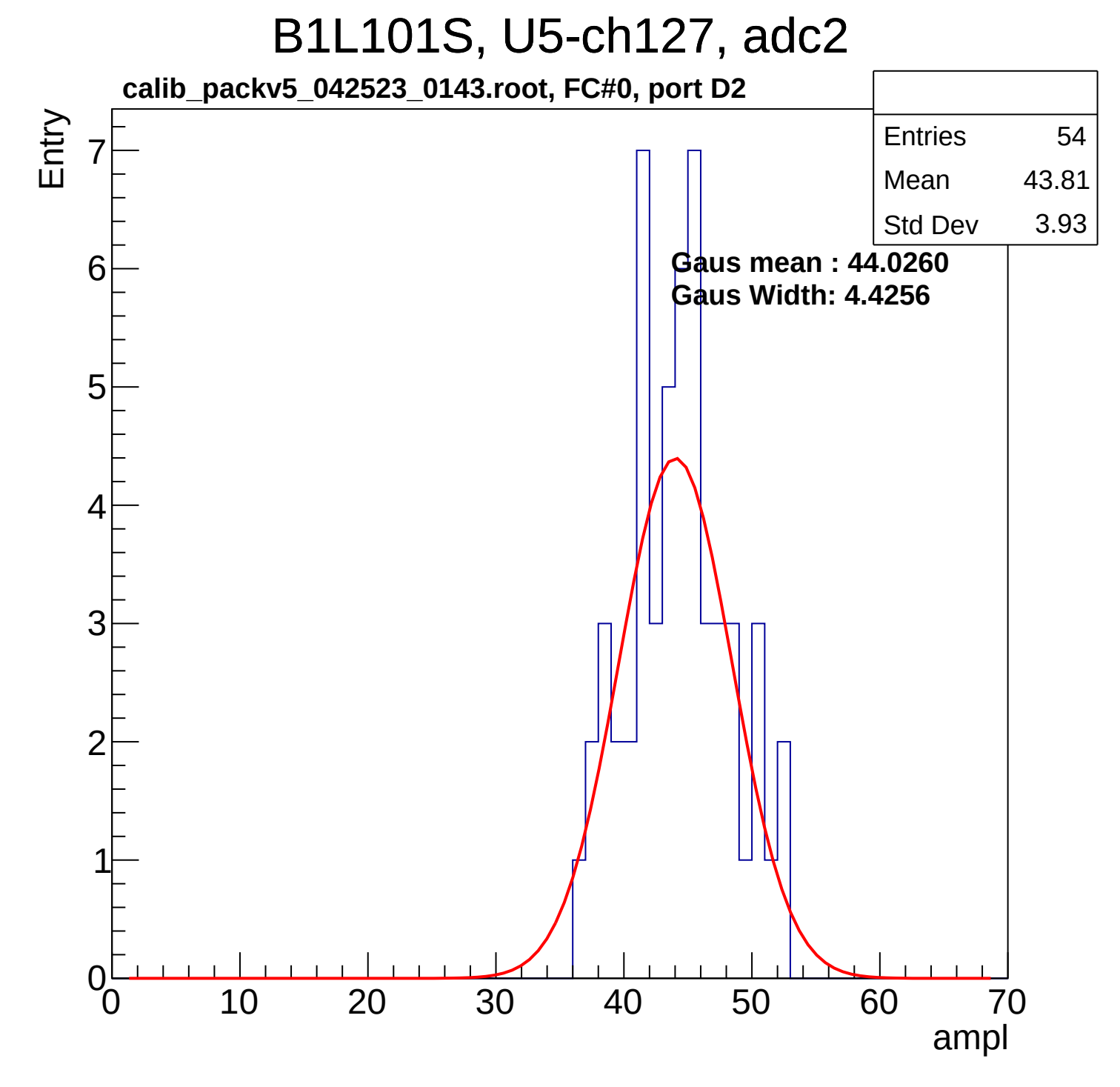
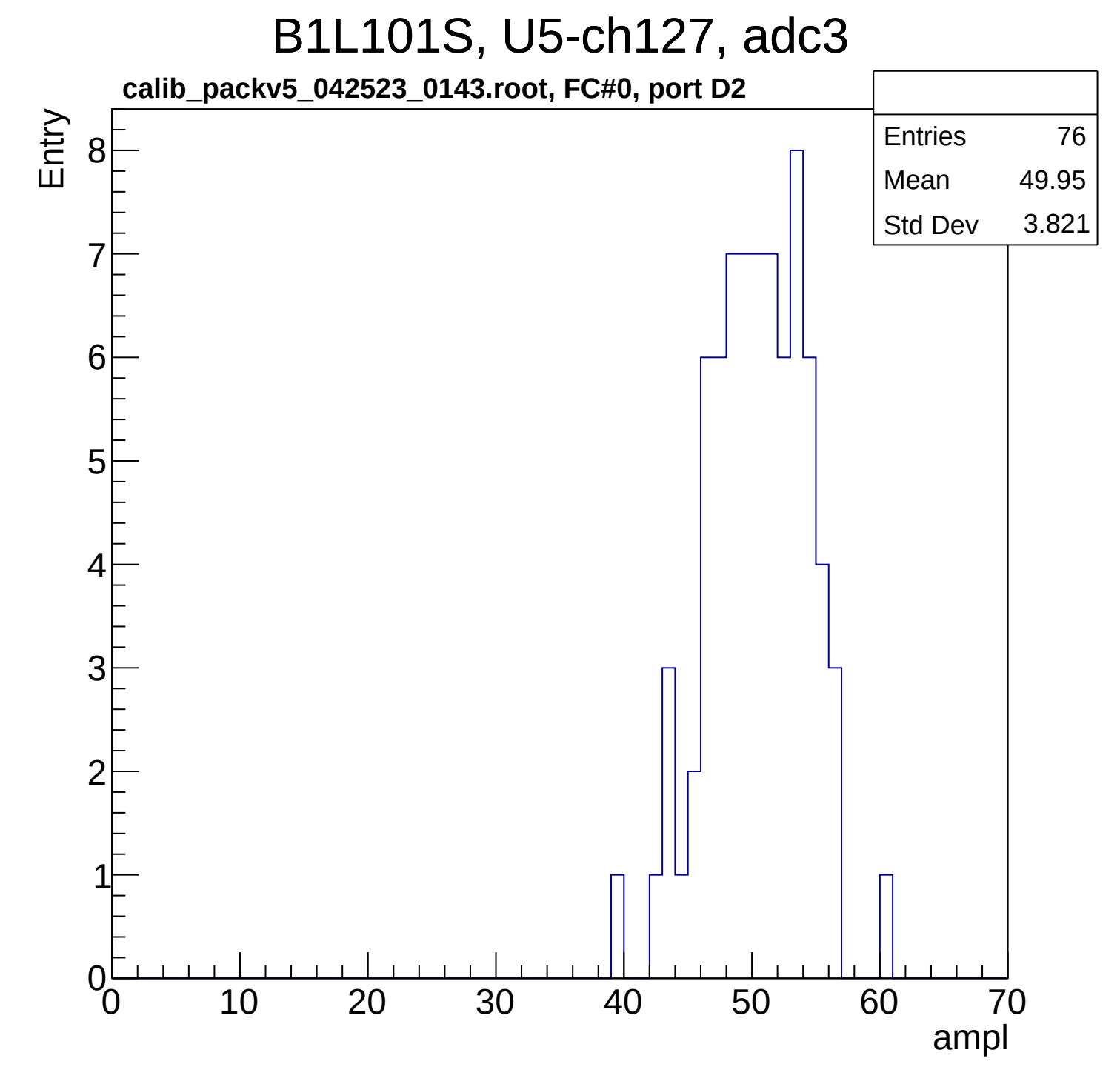
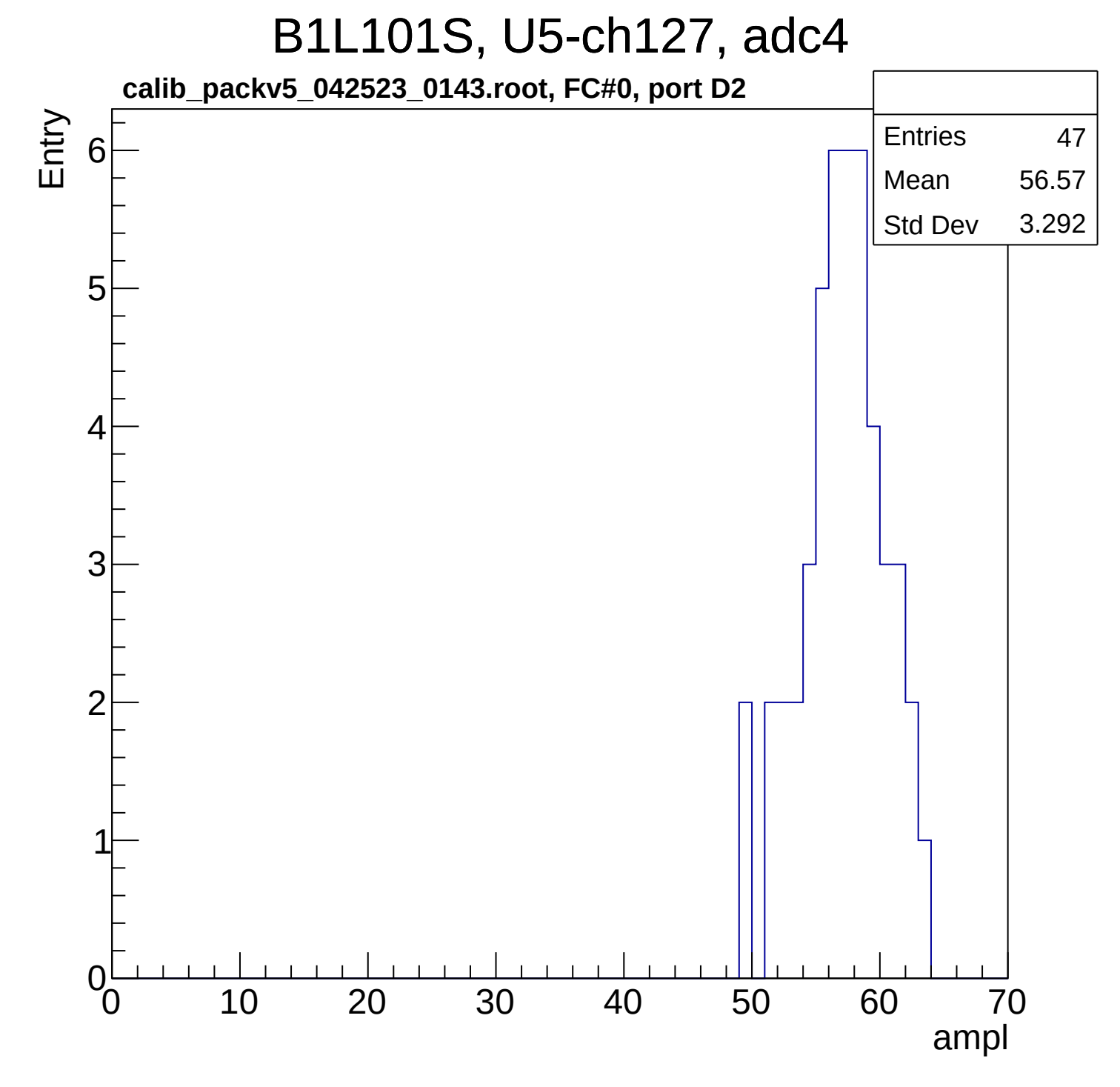
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

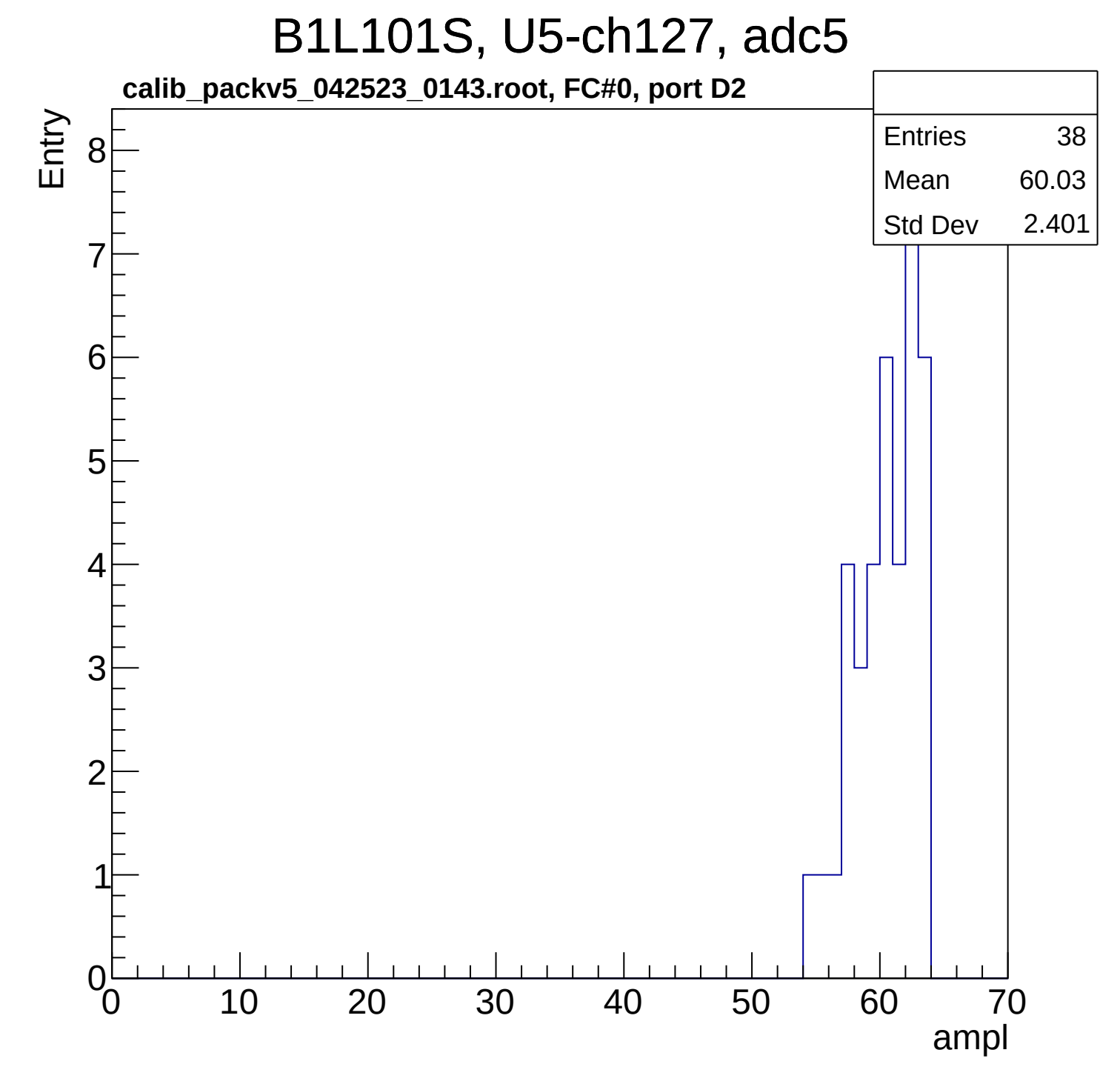

B1L101S, U5-ch127, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 30.14
Std Dev 3.8
Gaus mean : 31.5618
Gaus Width: 4.3391
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

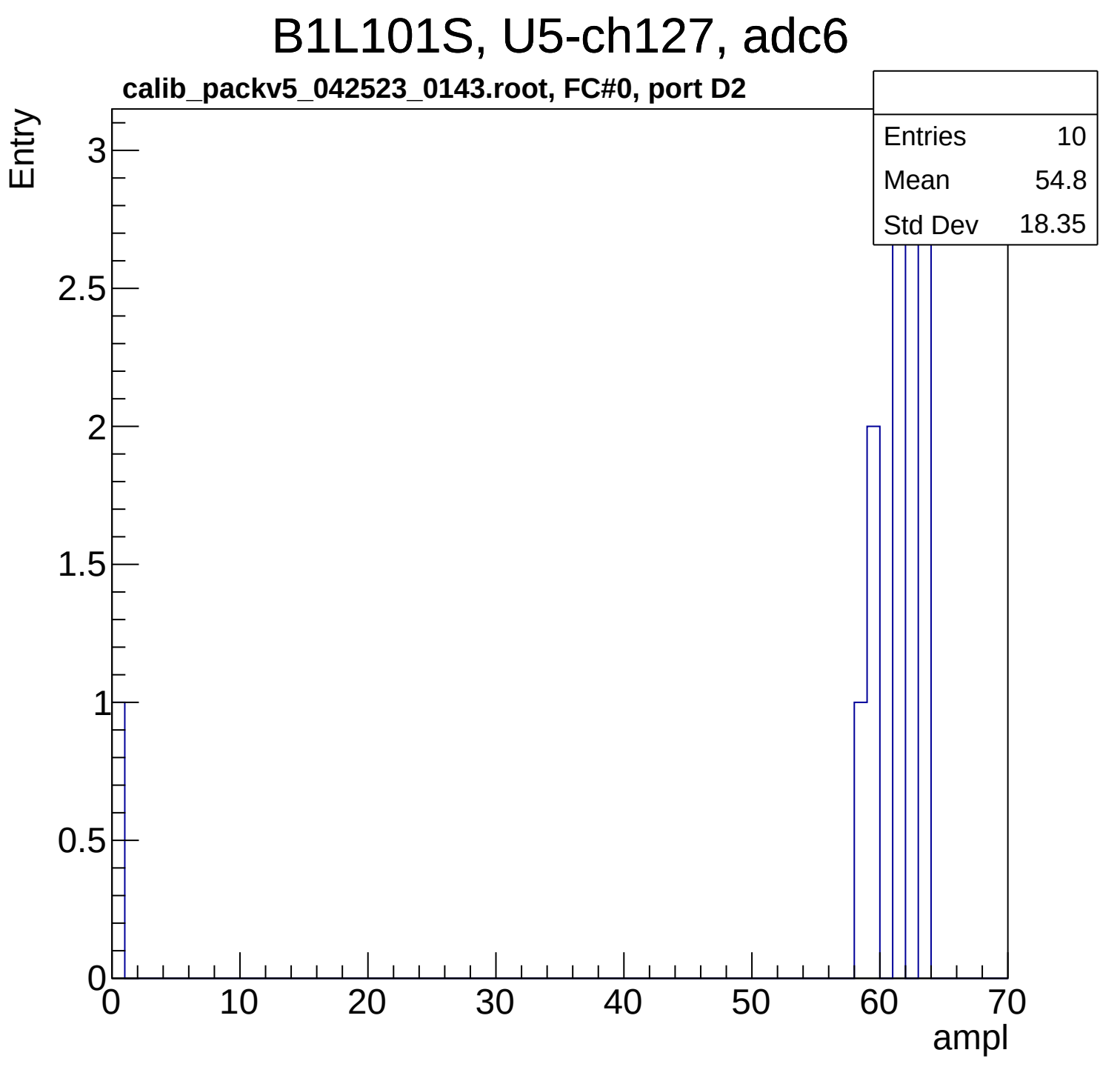

B1L101S, U5-ch127, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 36.96
Std Dev 5.986
Gaus mean : 37.9513
Gaus Width: 4.4557
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

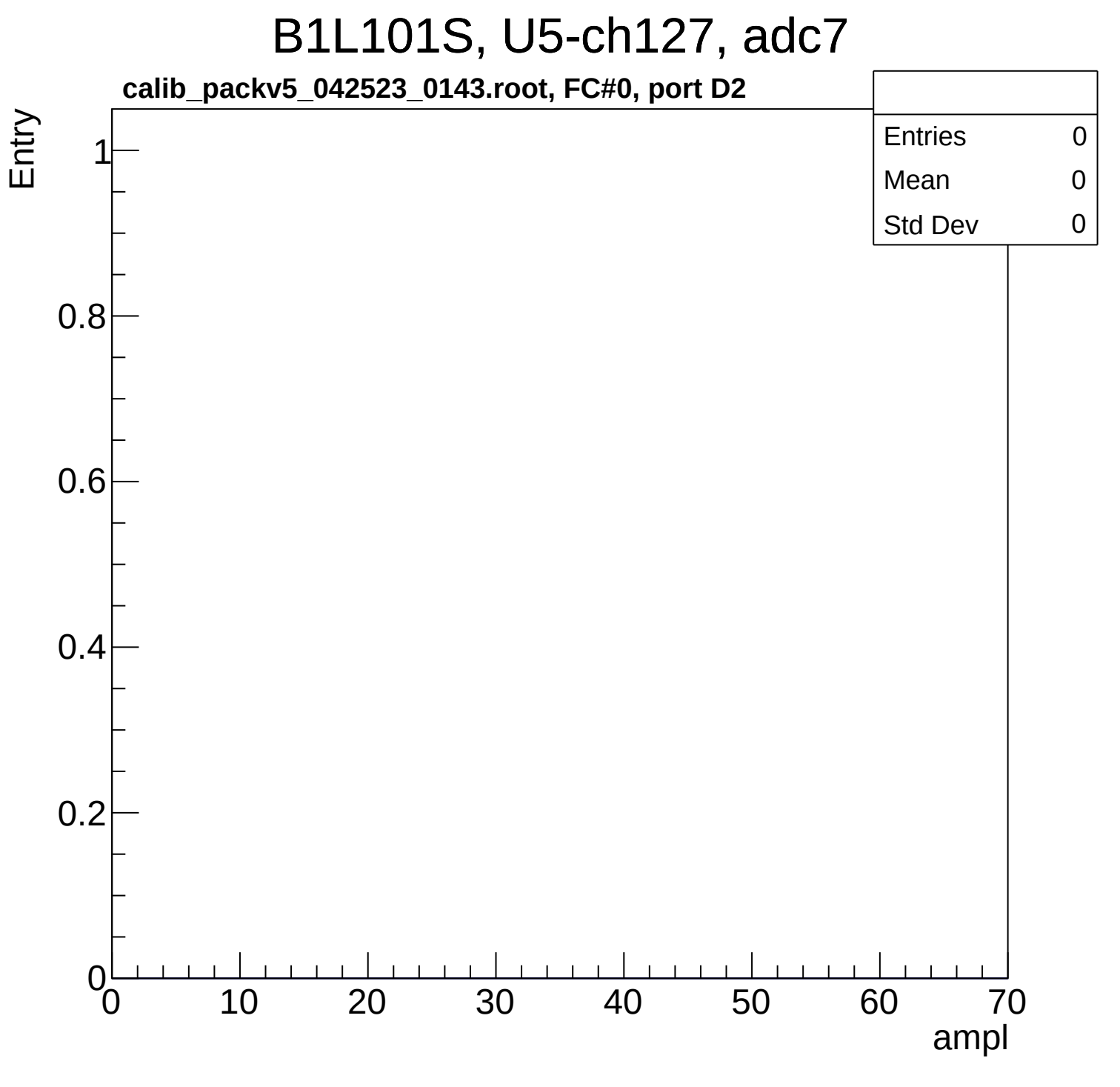

B1L101S, U5-ch127, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 43.81
Std Dev 3.93
Gaus mean : 44.0260
Gaus Width: 4.4256
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

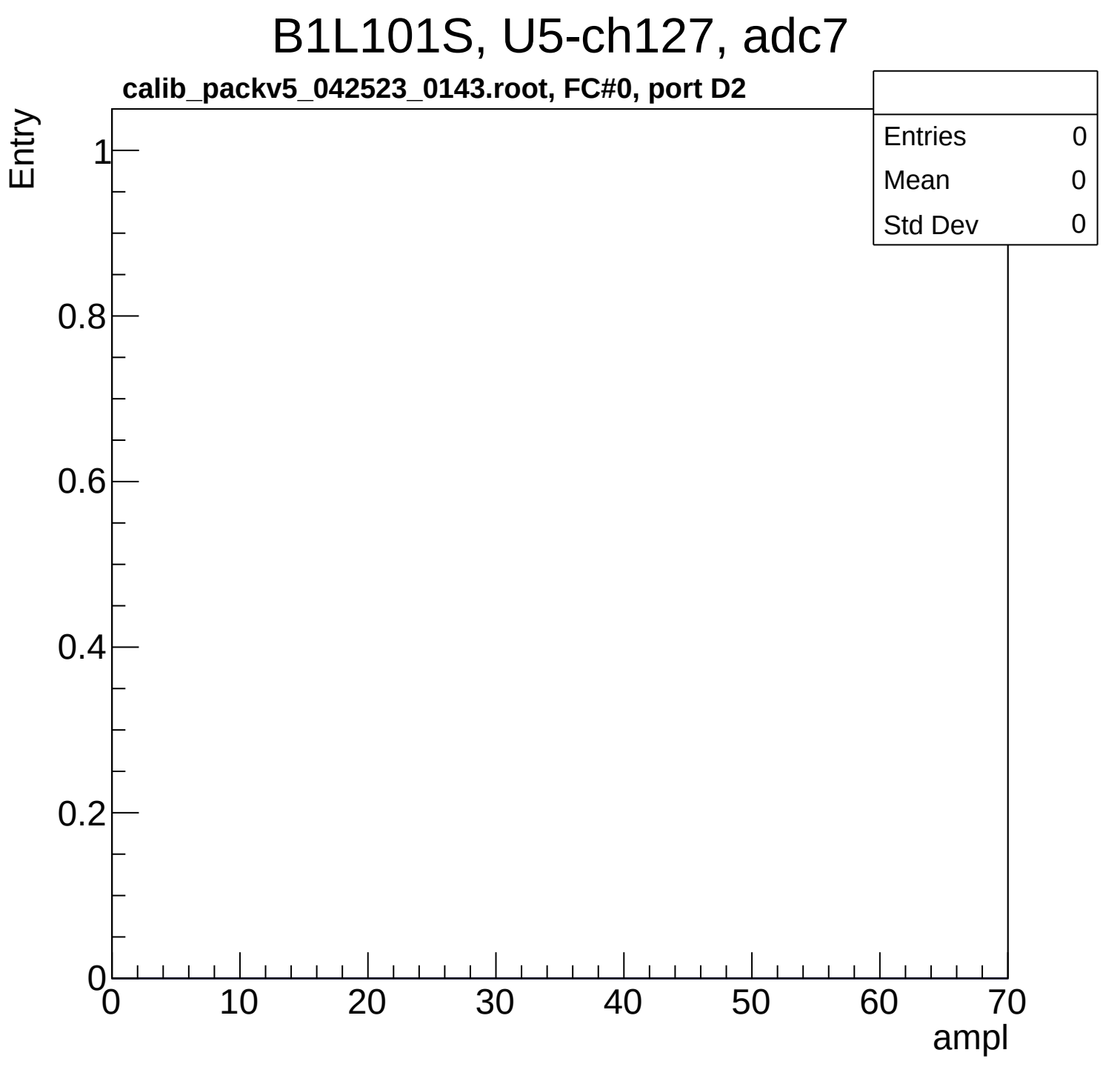

B1L101S, U5-ch127, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 49.95
Std Dev 3.821
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch127, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 56.57
Std Dev 3.292
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L101S, U5-ch127, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 38
Mean 60.03
Std Dev 2.401
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L101S, U5-ch127, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 54.8
Std Dev 18.35
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L101S, U5-ch127, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L101S, U5-ch127, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl