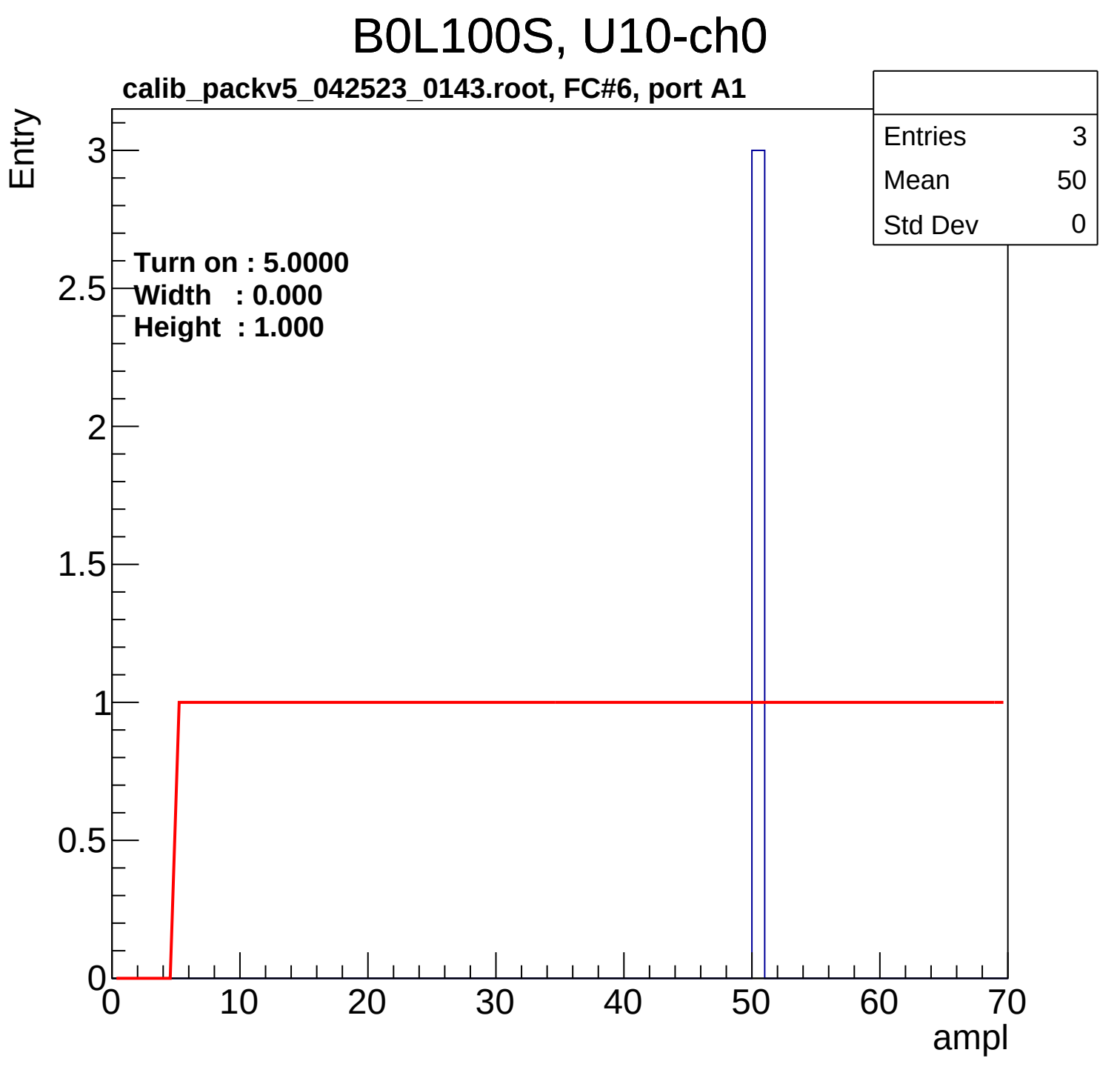
B0L100S, U10-ch0
calib_packv5_042523_0143.root, FC#6, port A1
Entries 3
Mean 50
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
50
60
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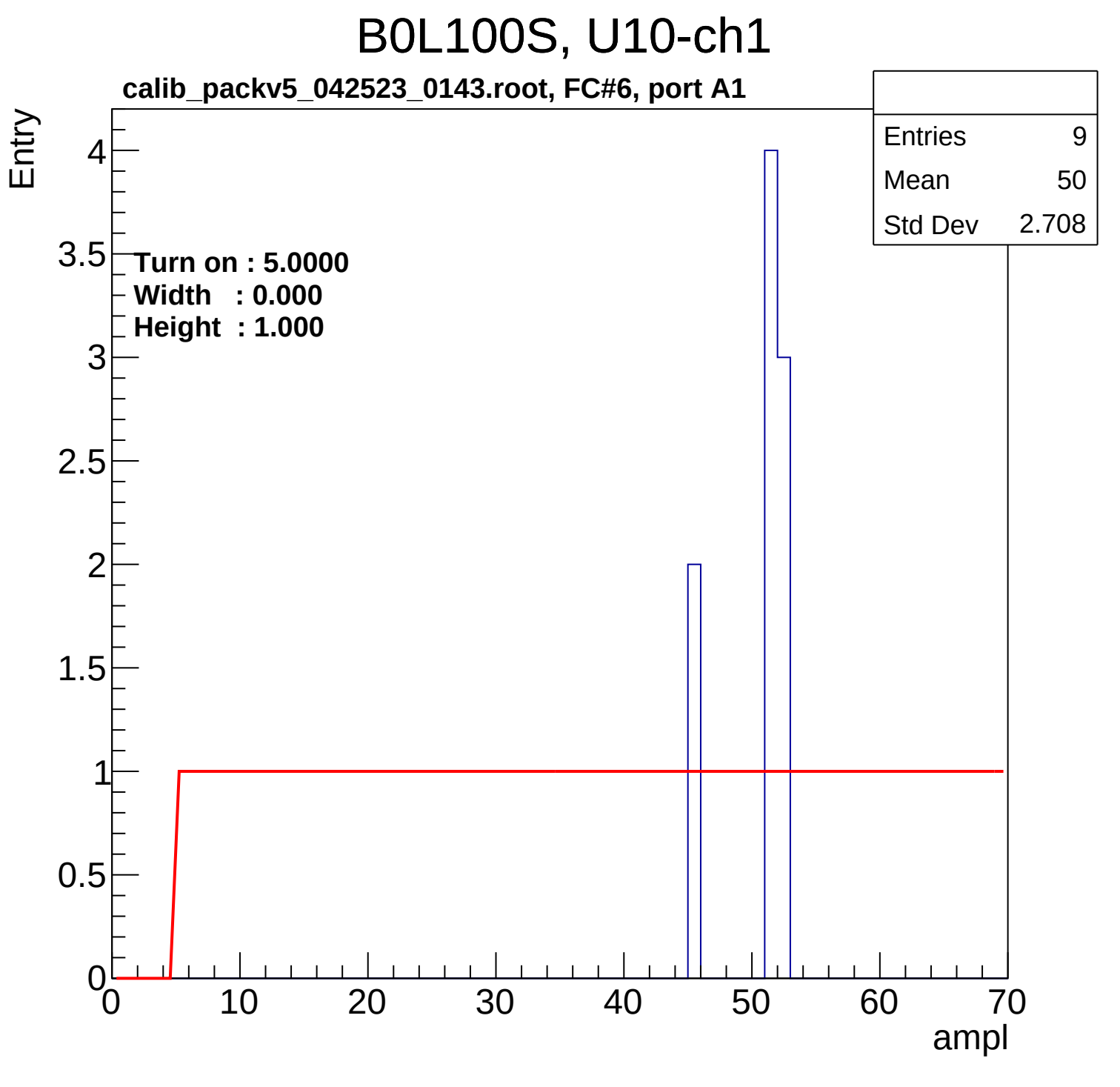
B0L100S, U10-ch1
calib_packv5_042523_0143.root, FC#6, port A1
Entries 9
Mean 50
Std Dev 2.708
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
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20
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40
50
60
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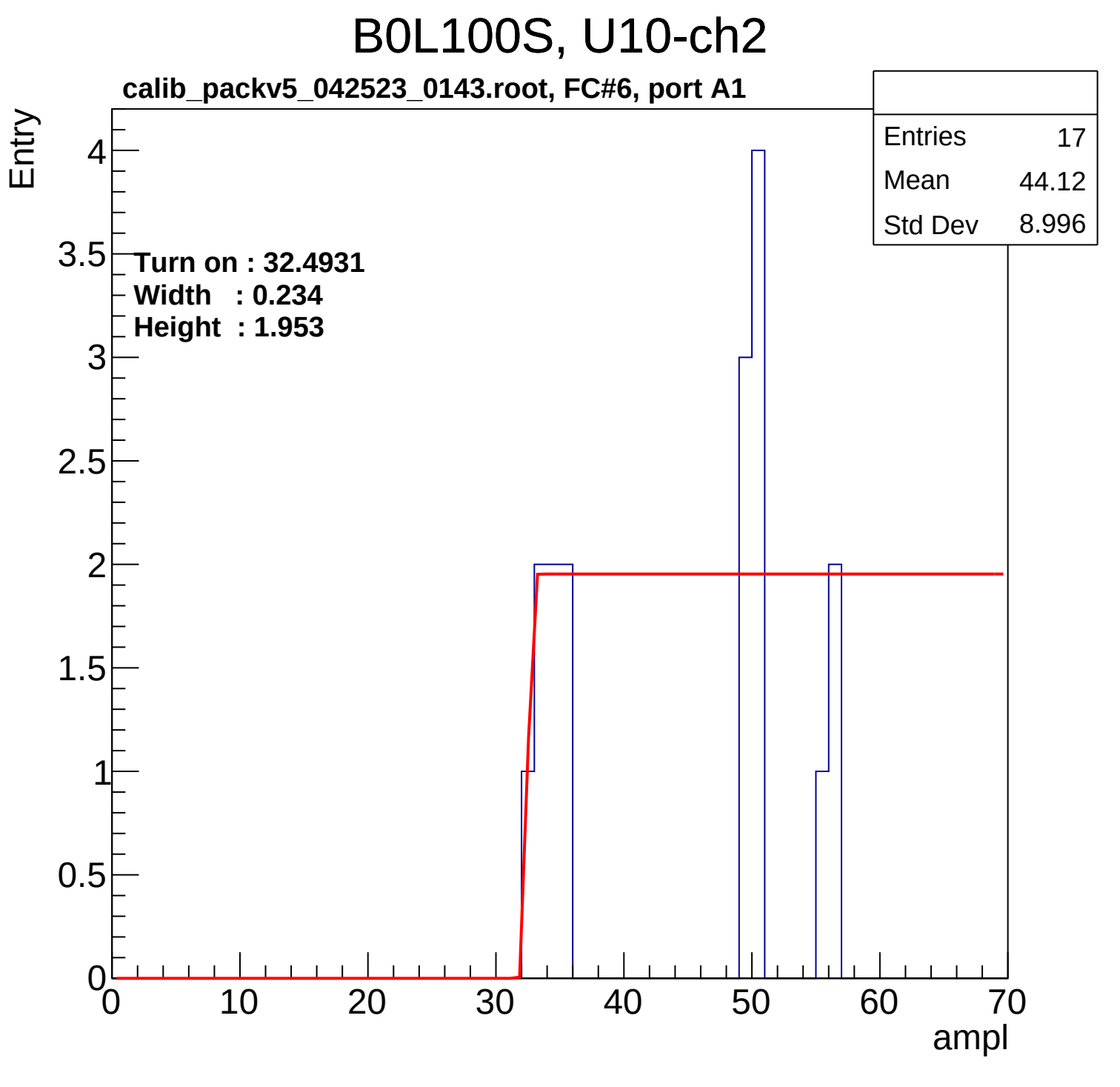
B0L100S, U10-ch2
calib_packv5_042523_0143.root, FC#6, port A1
Entries 17
Mean 44.12
Std Dev 8.996
Turn on : 32.4931
Width : 0.234
Height : 1.953
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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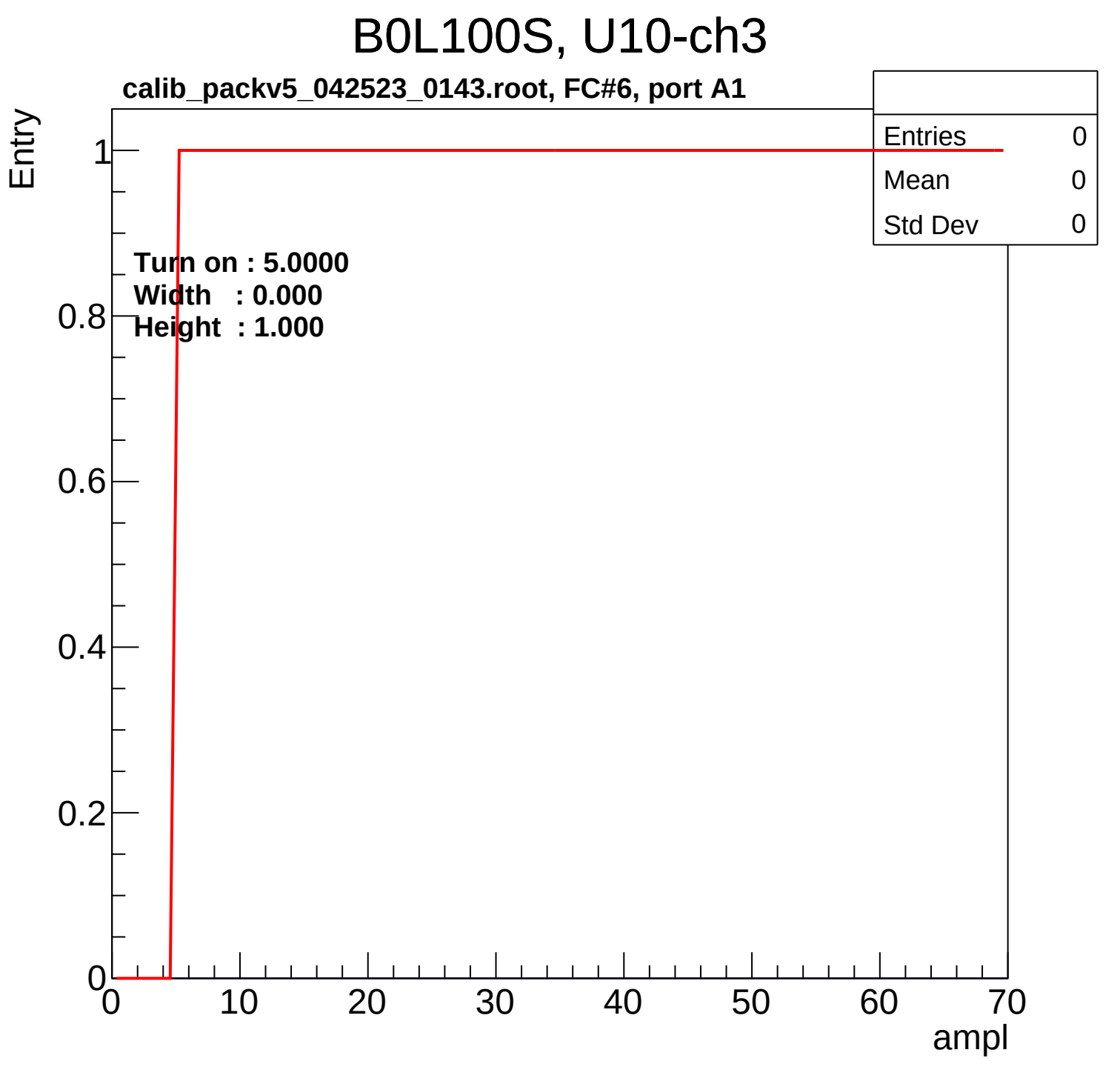
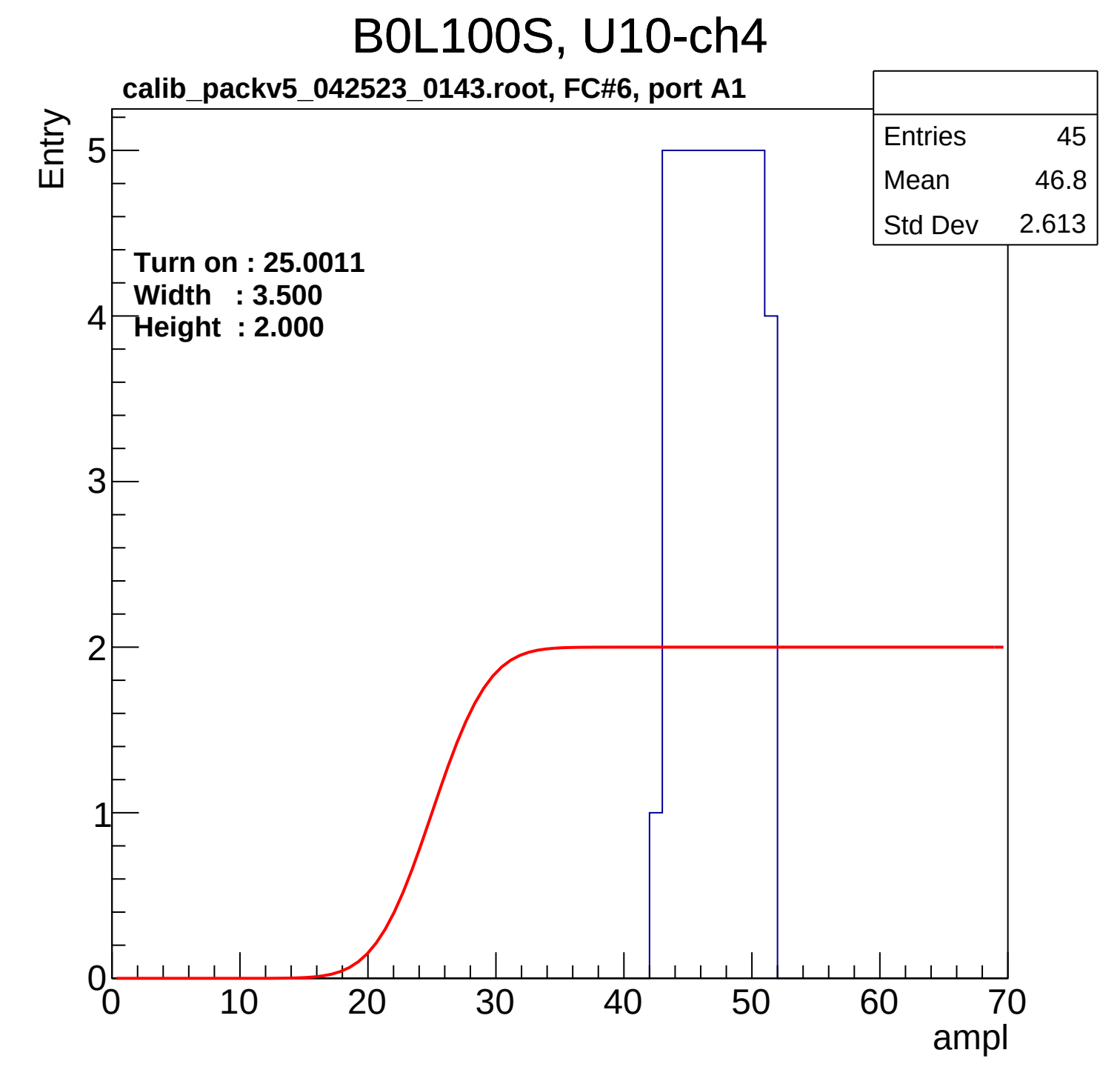
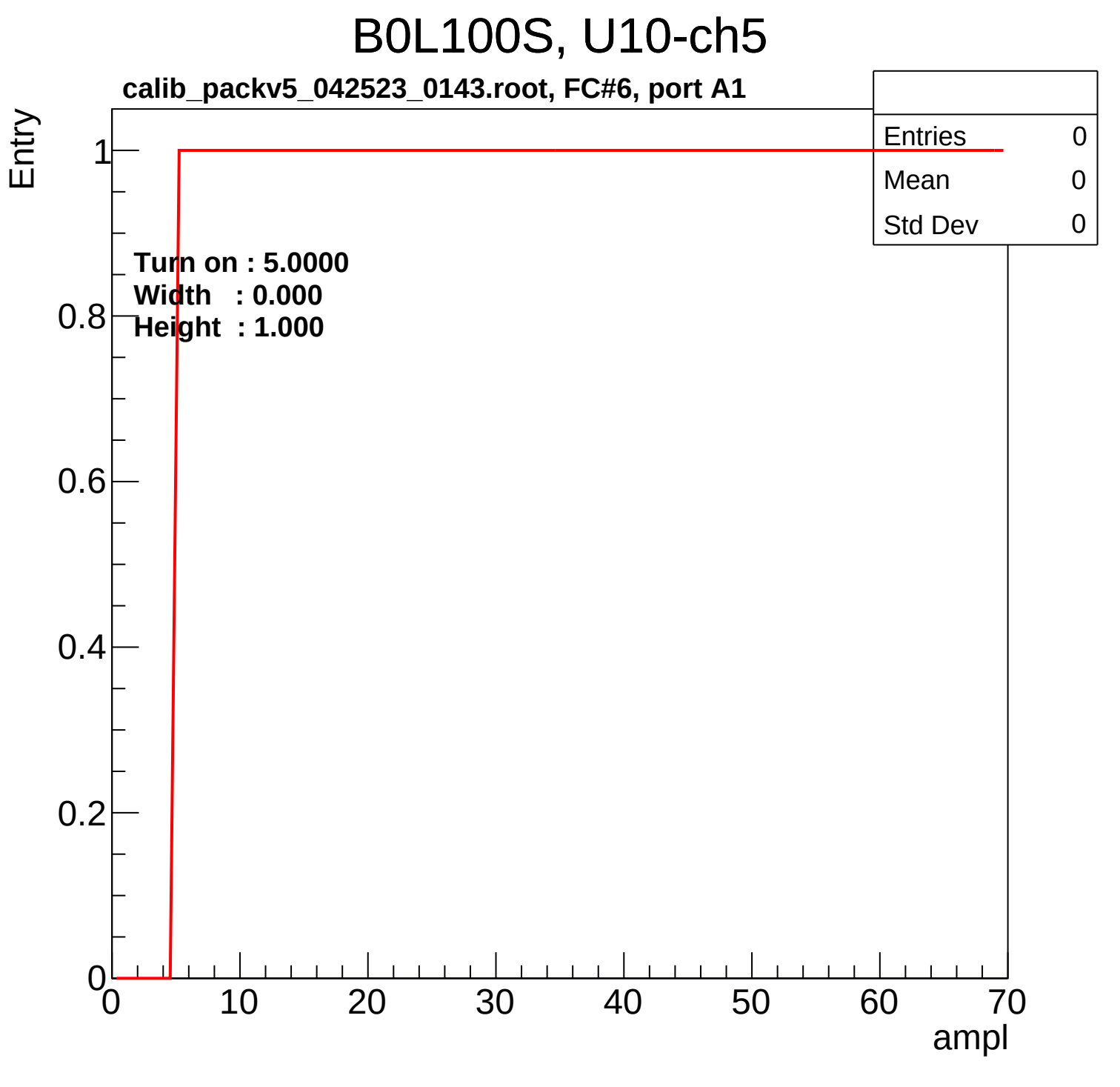
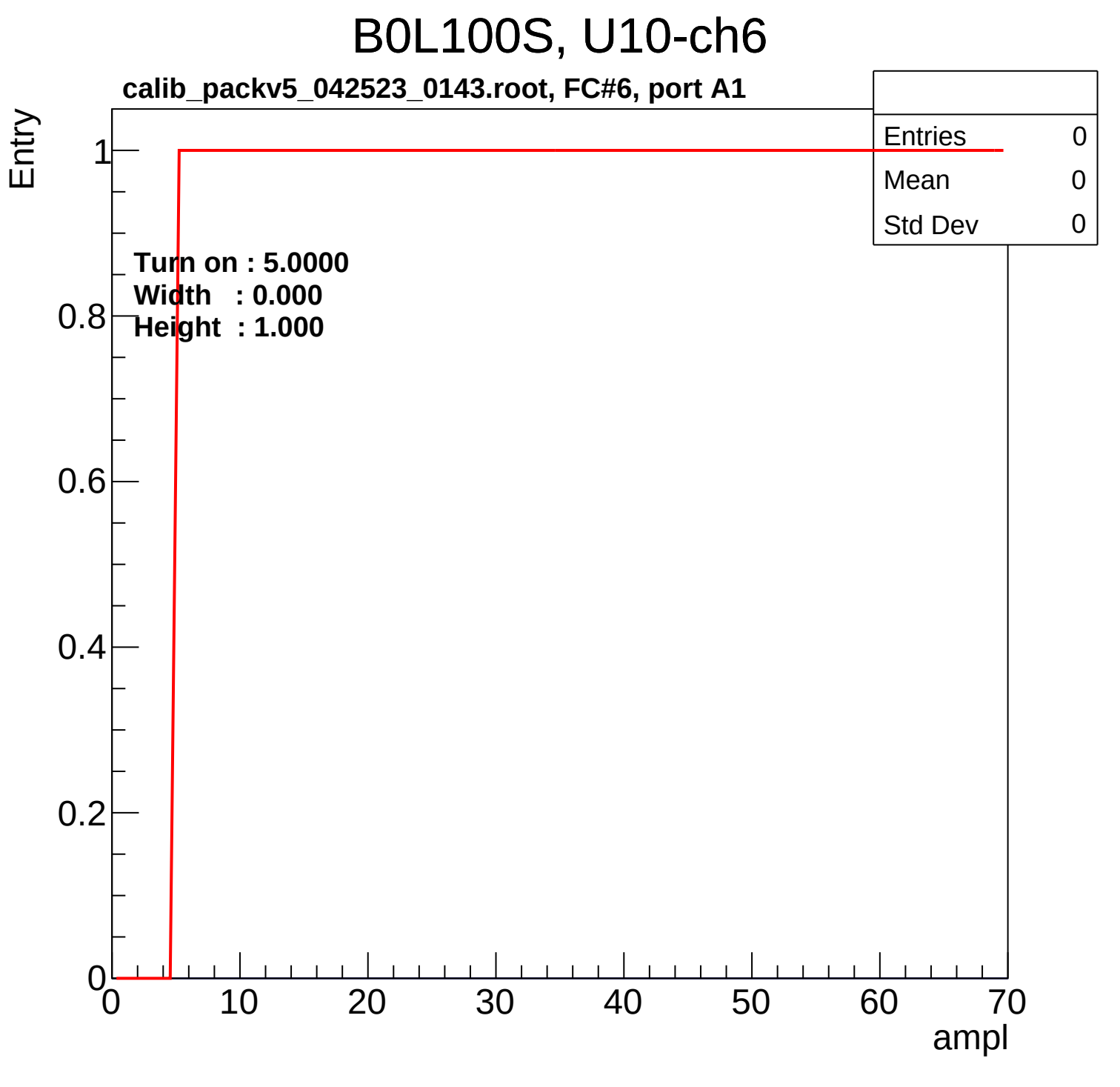
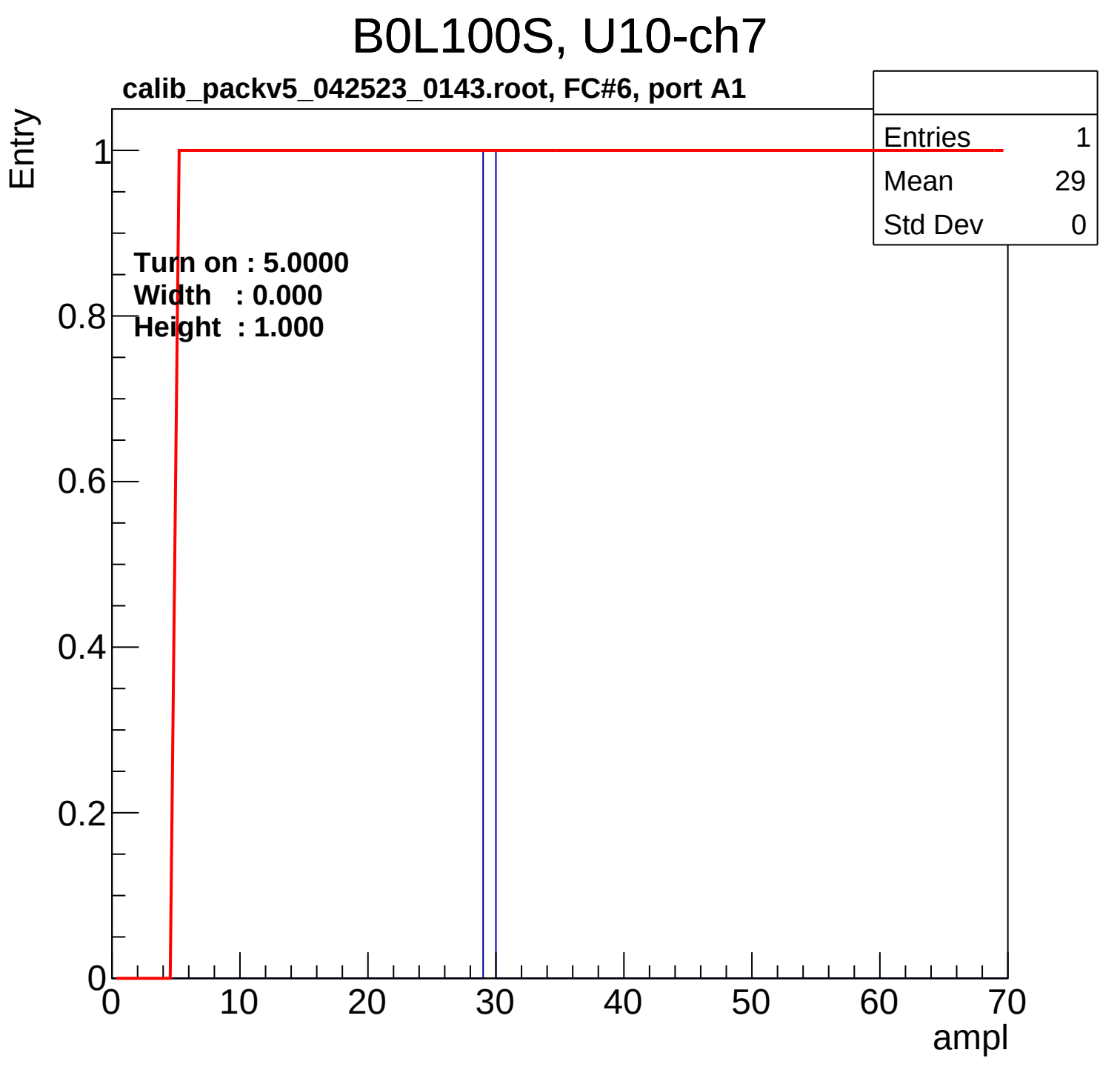
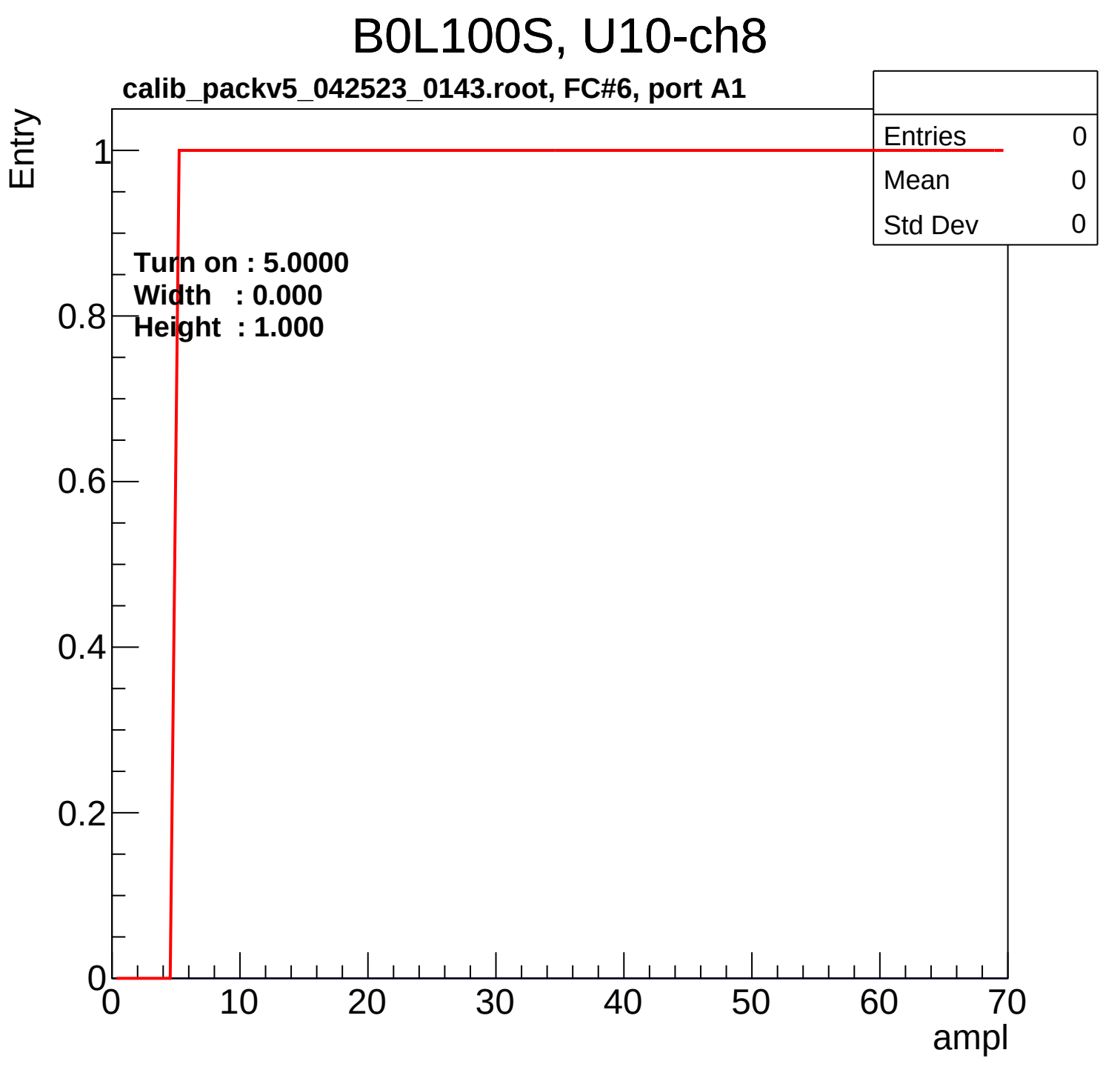

B0L100S, U10-ch3
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

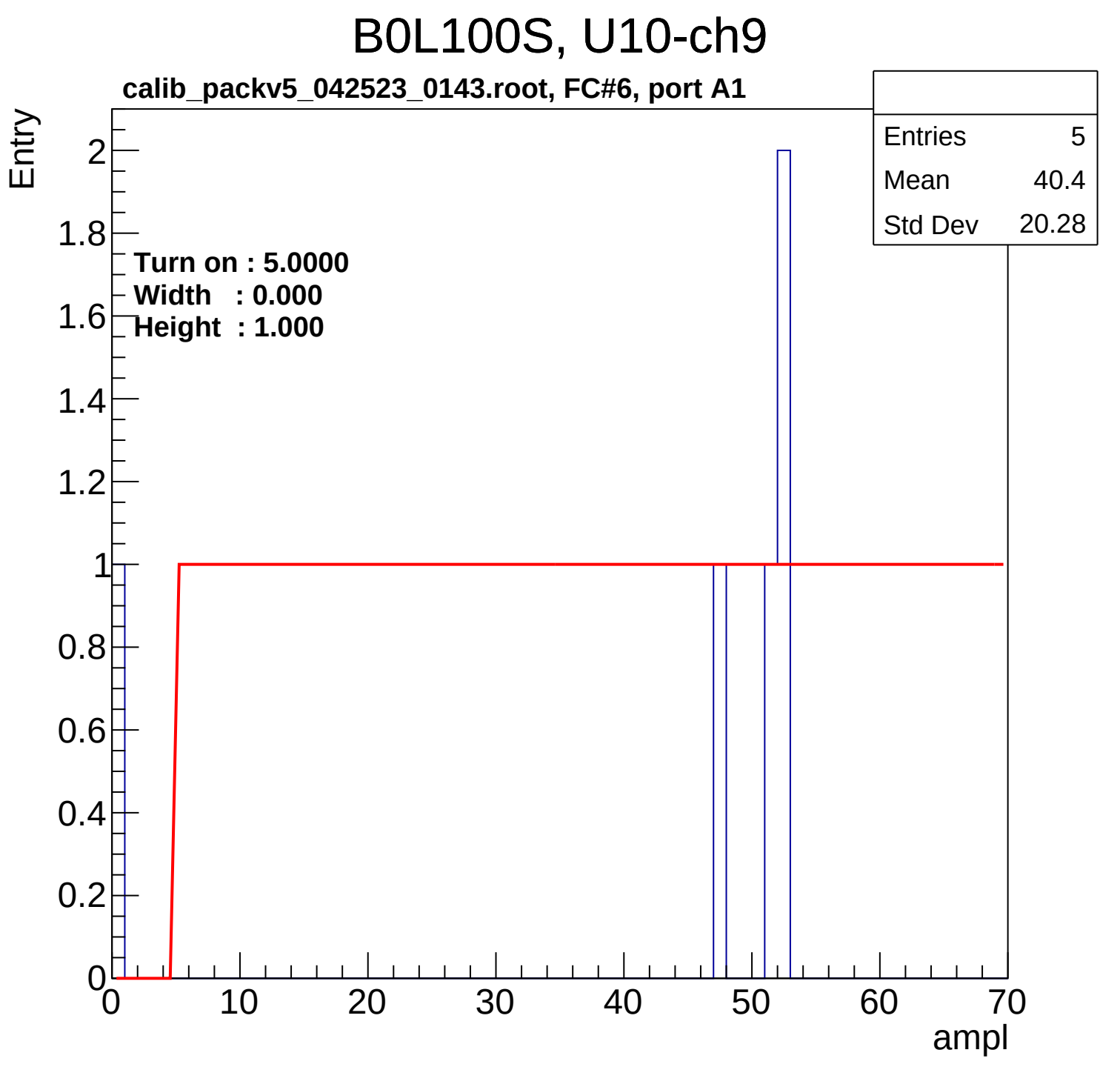

B0L100S, U10-ch4
calib_packv5_042523_0143.root, FC#6, port A1
Entries 45
Mean 46.8
Std Dev 2.613
Turn on : 25.0011
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U10-ch5
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U10-ch6
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U10-ch7
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 29
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U10-ch8
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U10-ch9
calib_packv5_042523_0143.root, FC#6, port A1
Entries 5
Mean 40.4
Std Dev 20.28
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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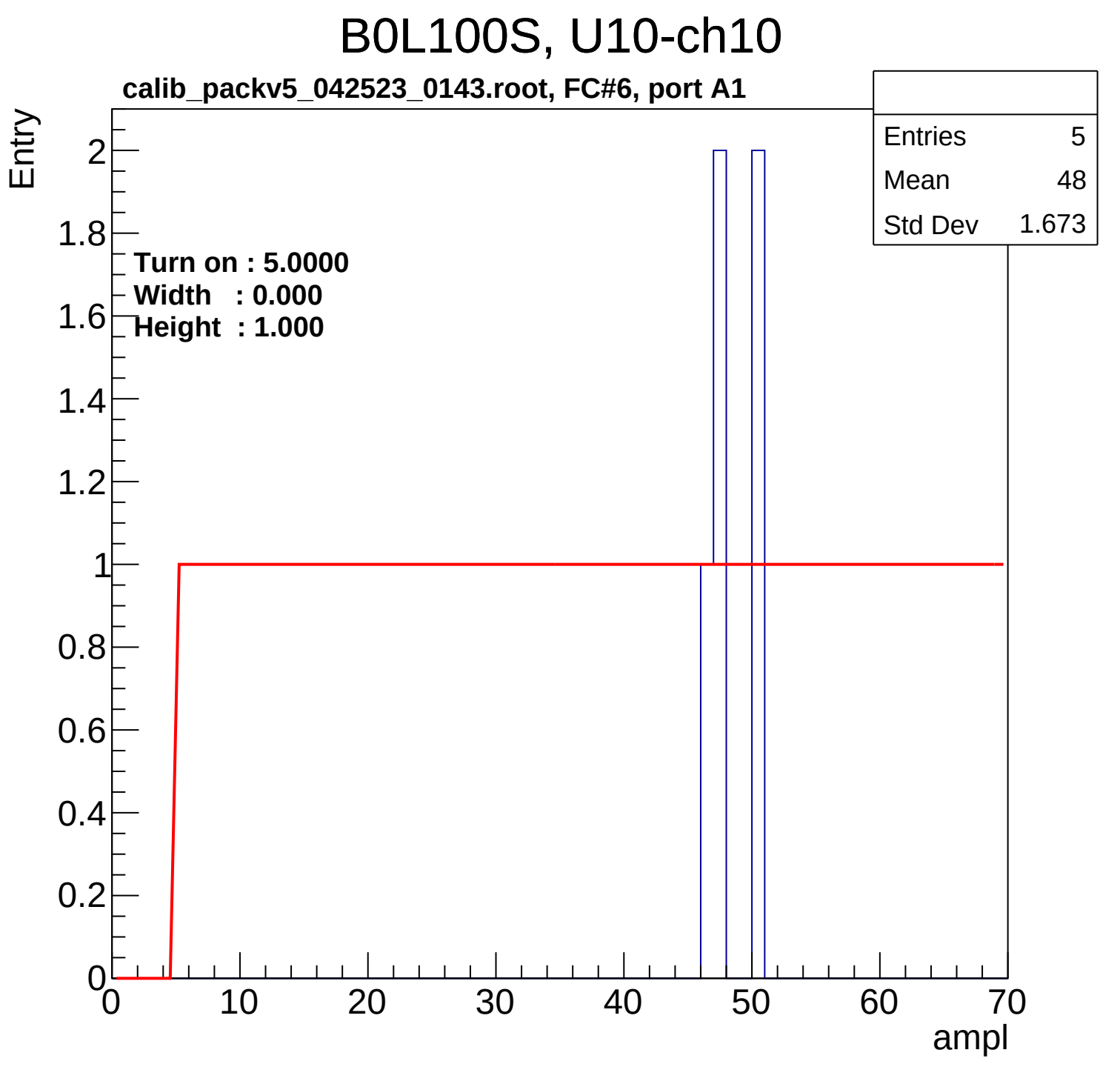
B0L100S, U10-ch10
calib_packv5_042523_0143.root, FC#6, port A1
Entries 5
Mean 48
Std Dev 1.673
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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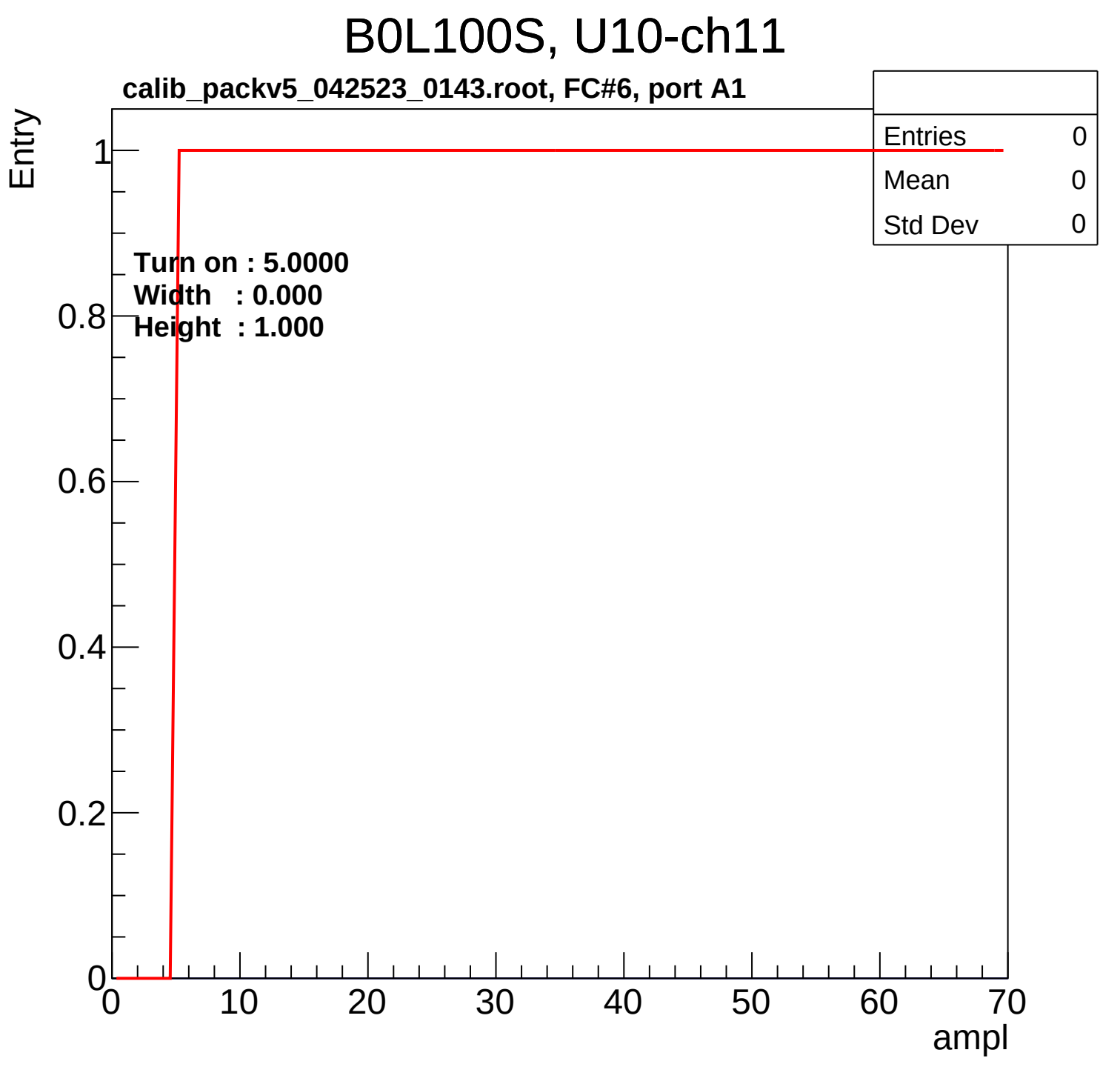
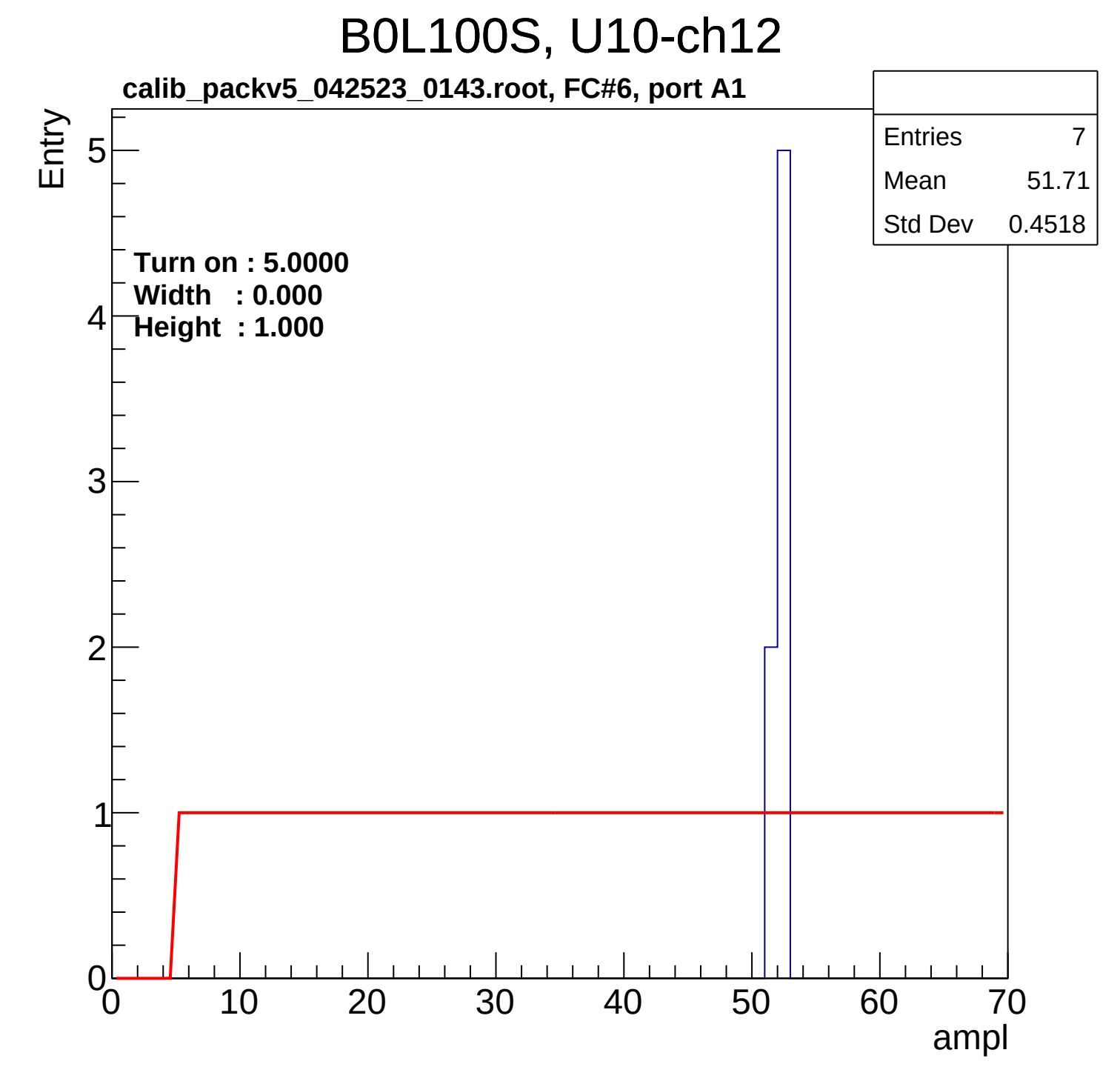
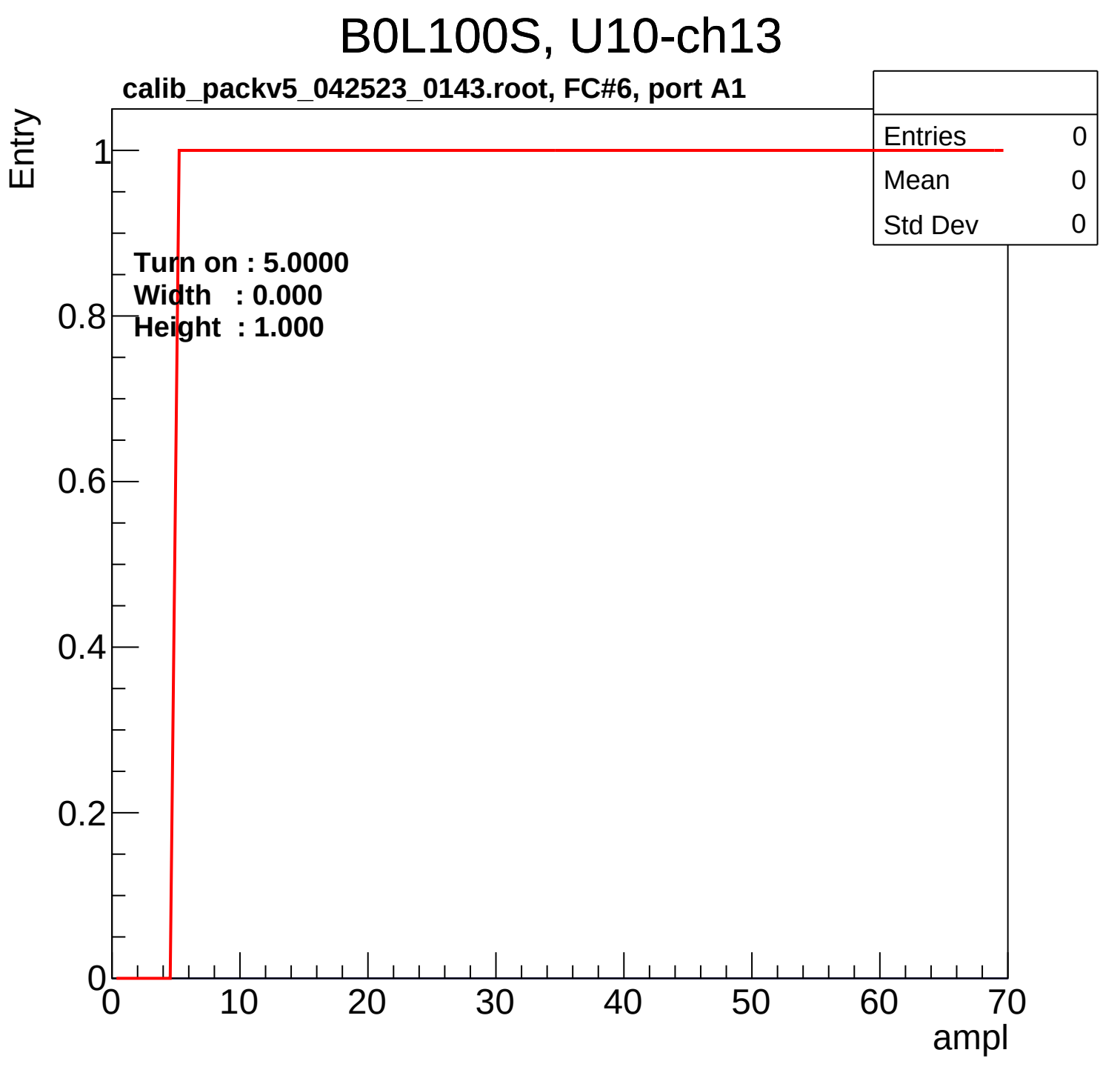
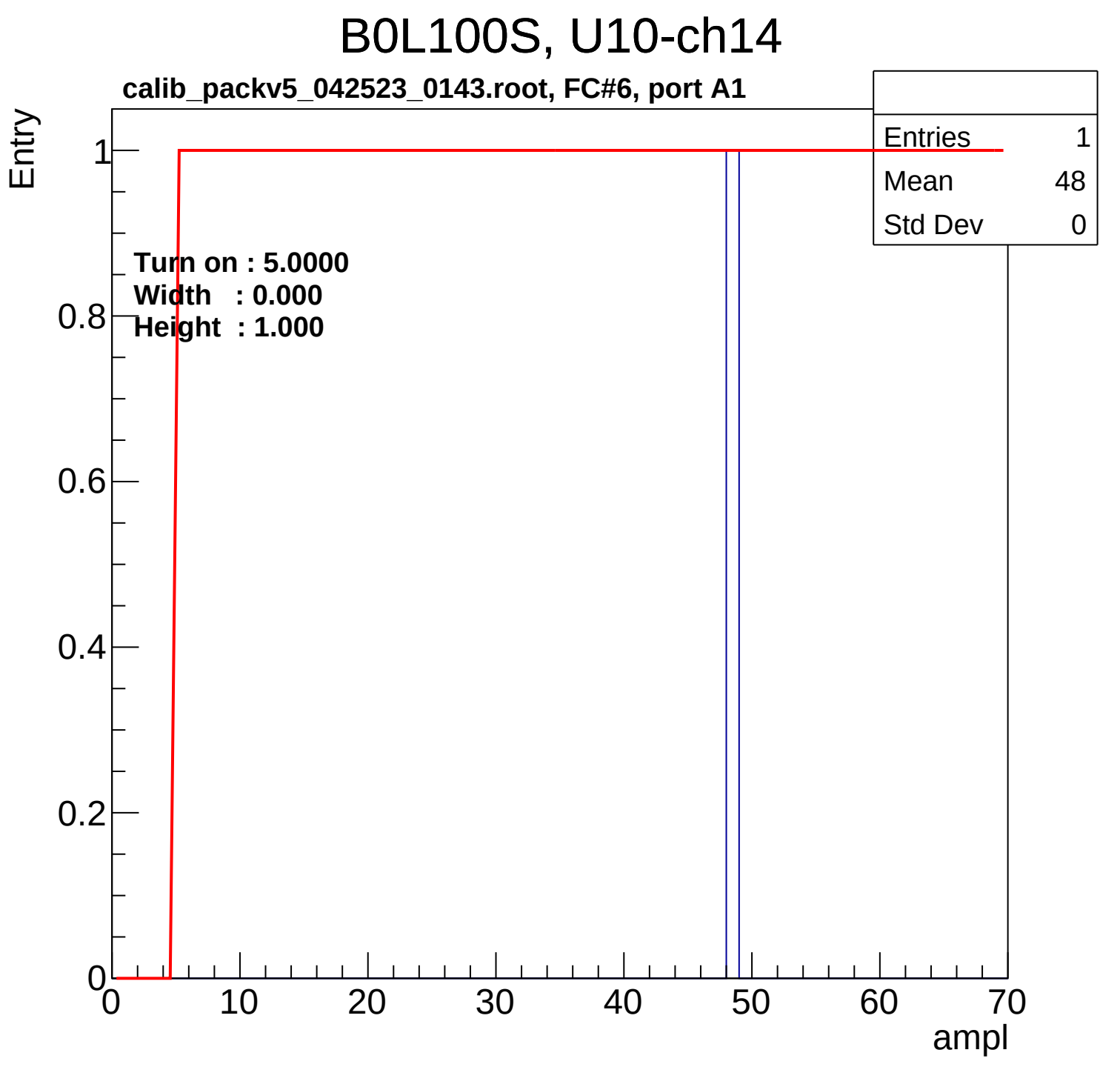

B0L100S, U10-ch11
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U10-ch12
calib_packv5_042523_0143.root, FC#6, port A1
Entries 7
Mean 51.71
Std Dev 0.4518
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U10-ch13
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U10-ch14
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 48
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
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40
50
60
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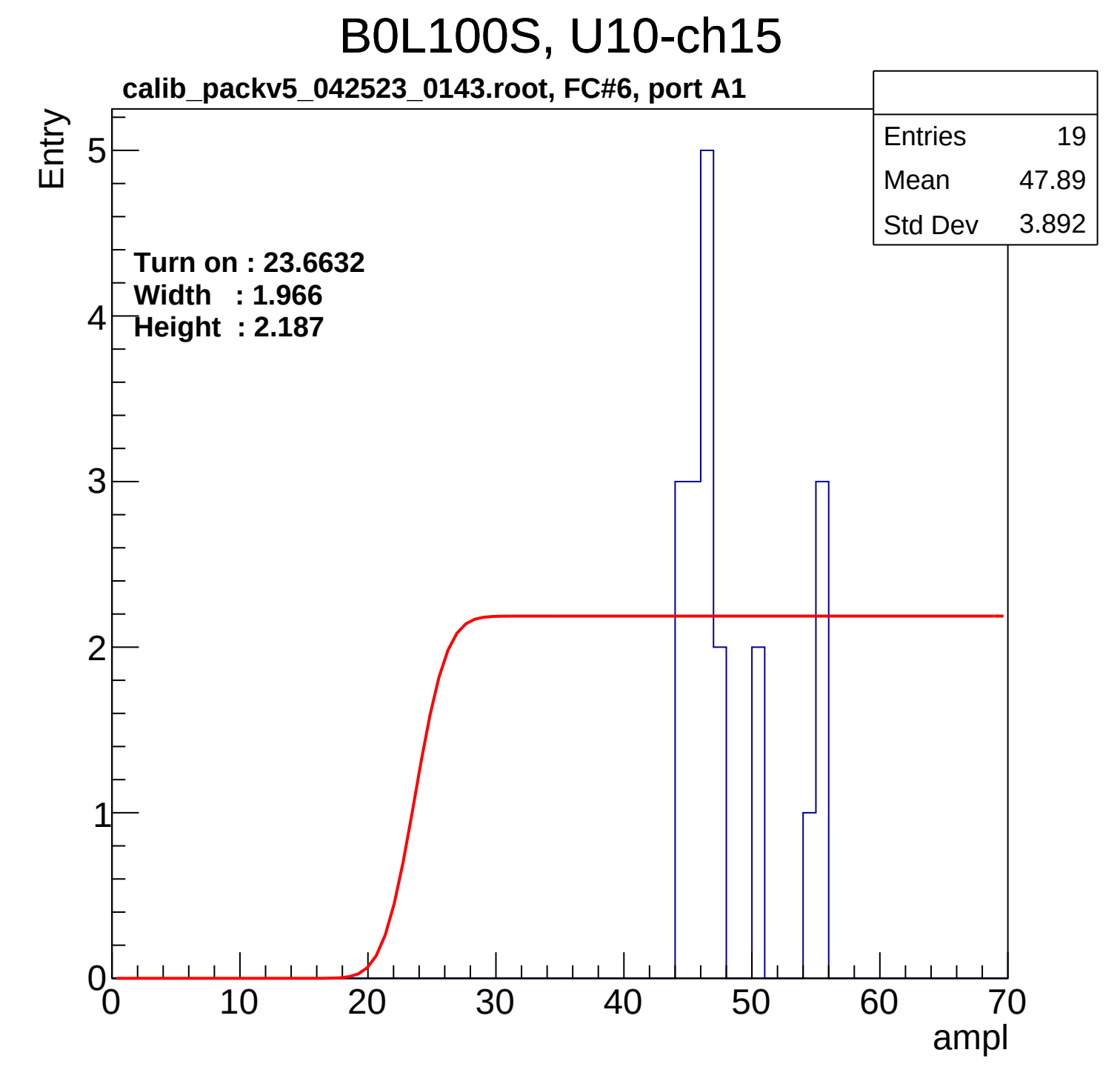
B0L100S, U10-ch15
calib_packv5_042523_0143.root, FC#6, port A1
Entries 19
Mean 47.89
Std Dev 3.892
Turn on : 23.6632
Width : 1.966
Height : 2.187
Entry
ampl
0
1
2
3
4
5
0
10
20
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40
50
60
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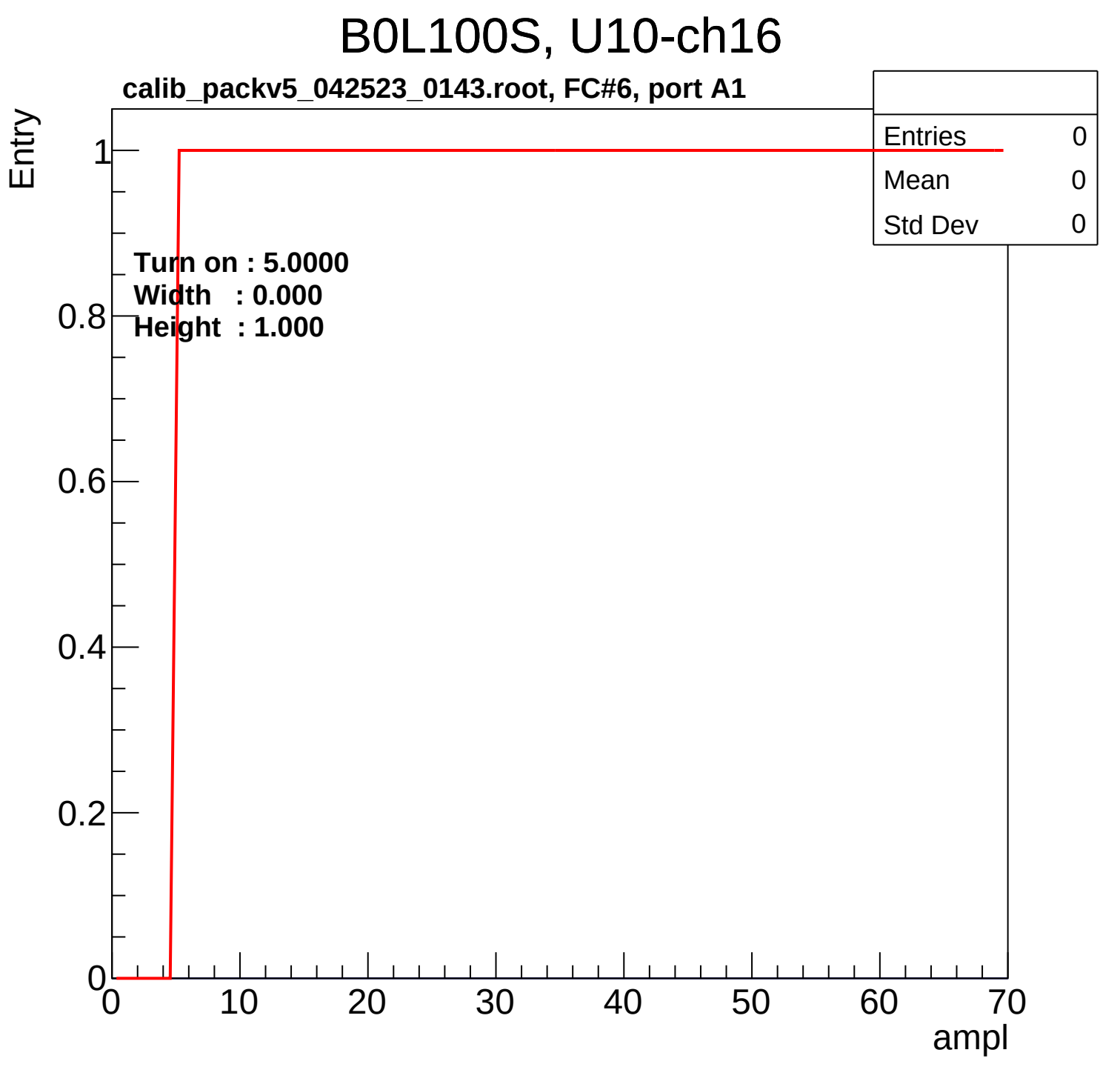
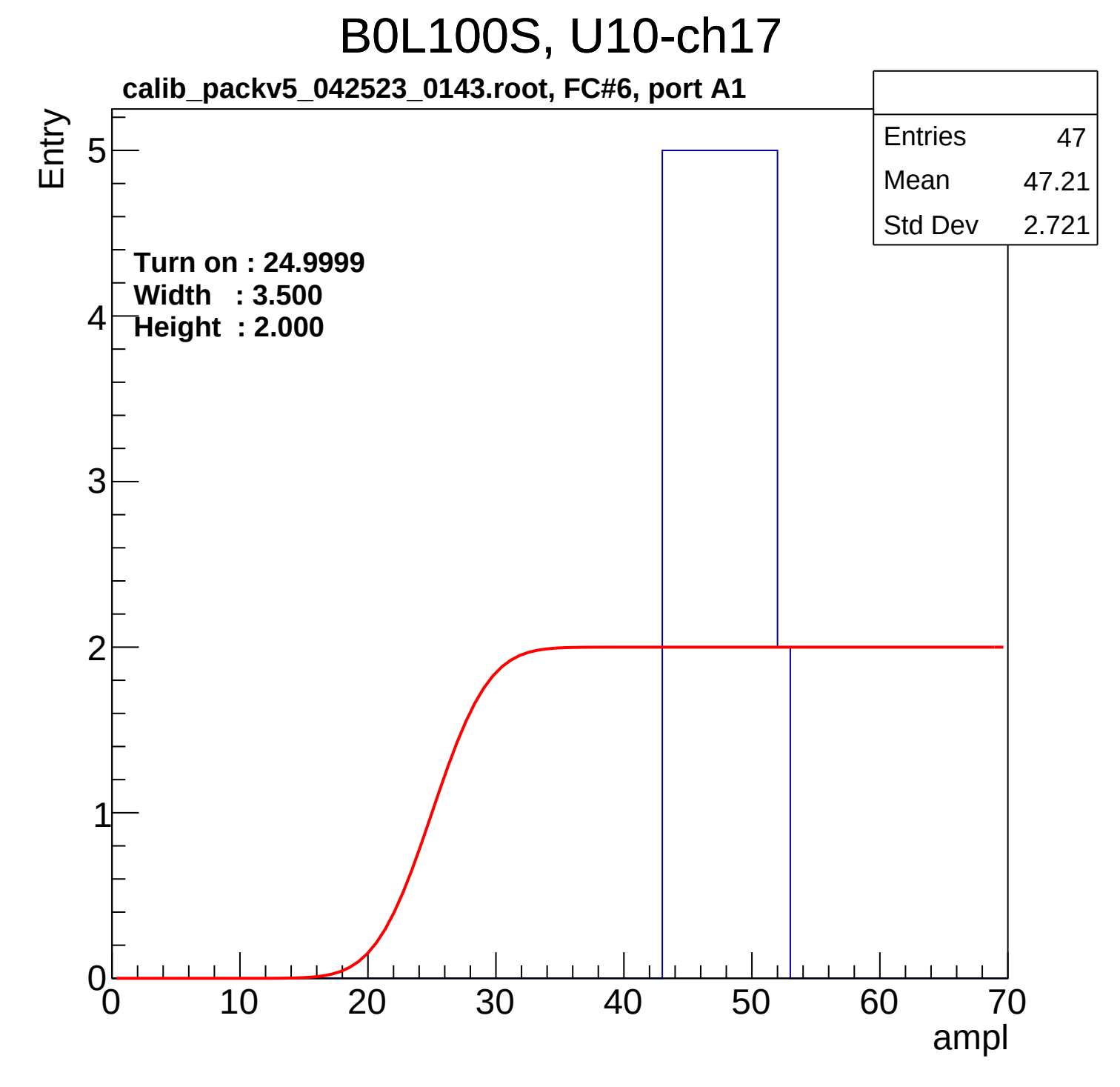

B0L100S, U10-ch16
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U10-ch17
calib_packv5_042523_0143.root, FC#6, port A1
Entries 47
Mean 47.21
Std Dev 2.721
Turn on : 24.9999
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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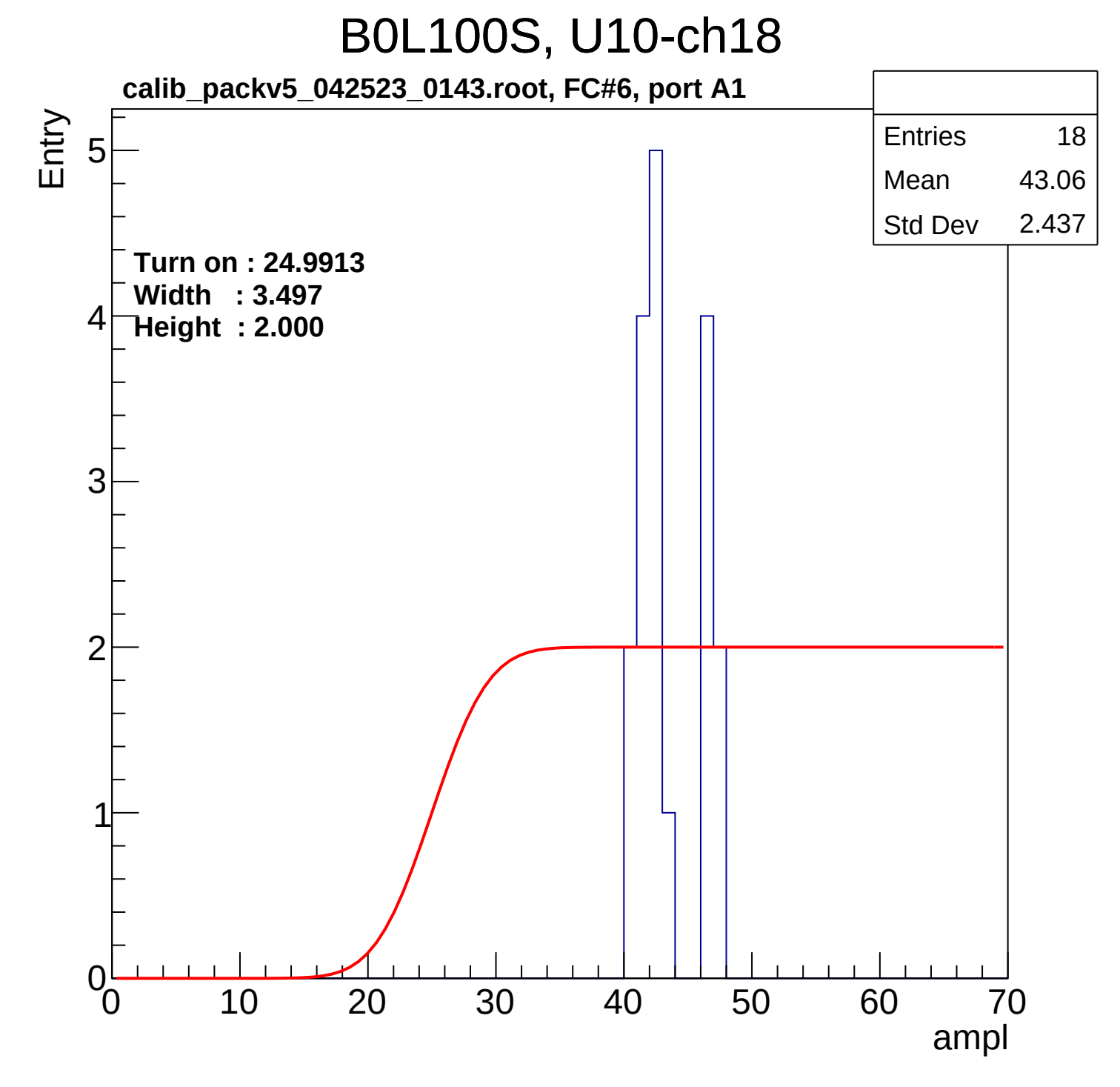
B0L100S, U10-ch18
calib_packv5_042523_0143.root, FC#6, port A1
Entries 18
Mean 43.06
Std Dev 2.437
Turn on : 24.9913
Width : 3.497
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
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20
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60
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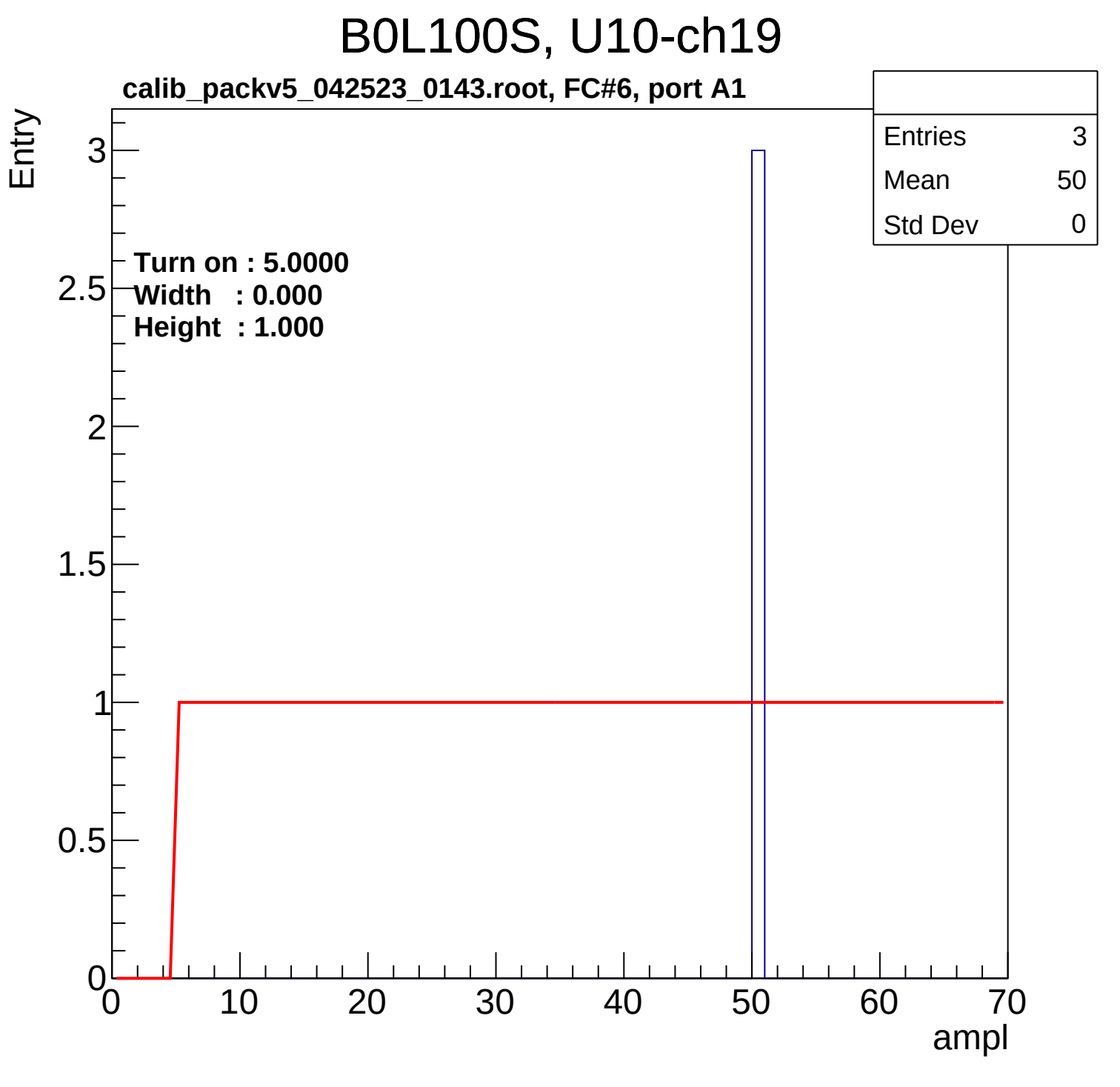
B0L100S, U10-ch19
calib_packv5_042523_0143.root, FC#6, port A1
Entries 3
Mean 50
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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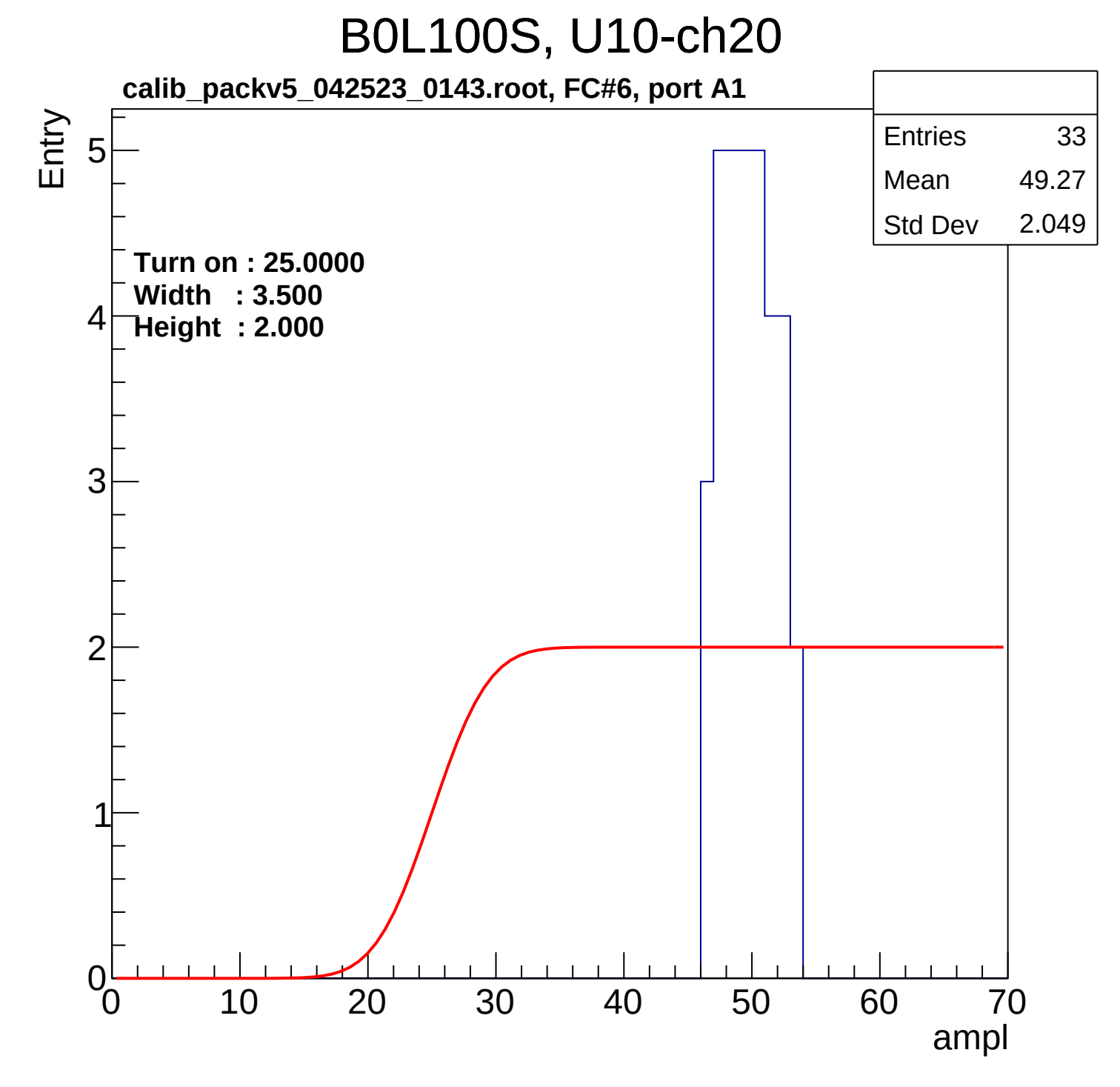
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B0L100S, U10-ch20
calib_packv5_042523_0143.root, FC#6, port A1
Entries 33
Mean 49.27
Std Dev 2.049
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
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20
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40
50
60
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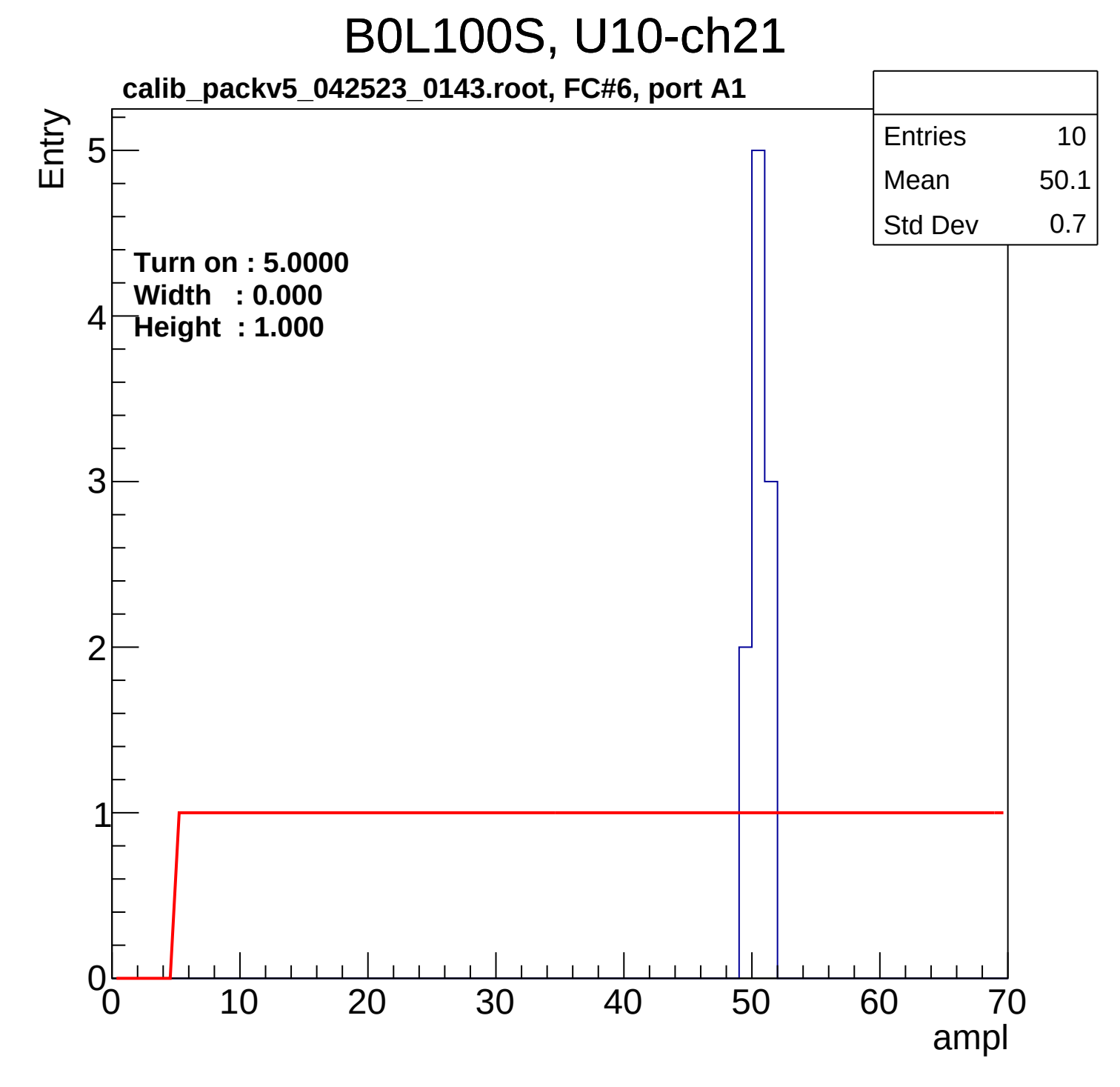
B0L100S, U10-ch21
calib_packv5_042523_0143.root, FC#6, port A1
Entries 10
Mean 50.1
Std Dev 0.7
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
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20
30
40
50
60
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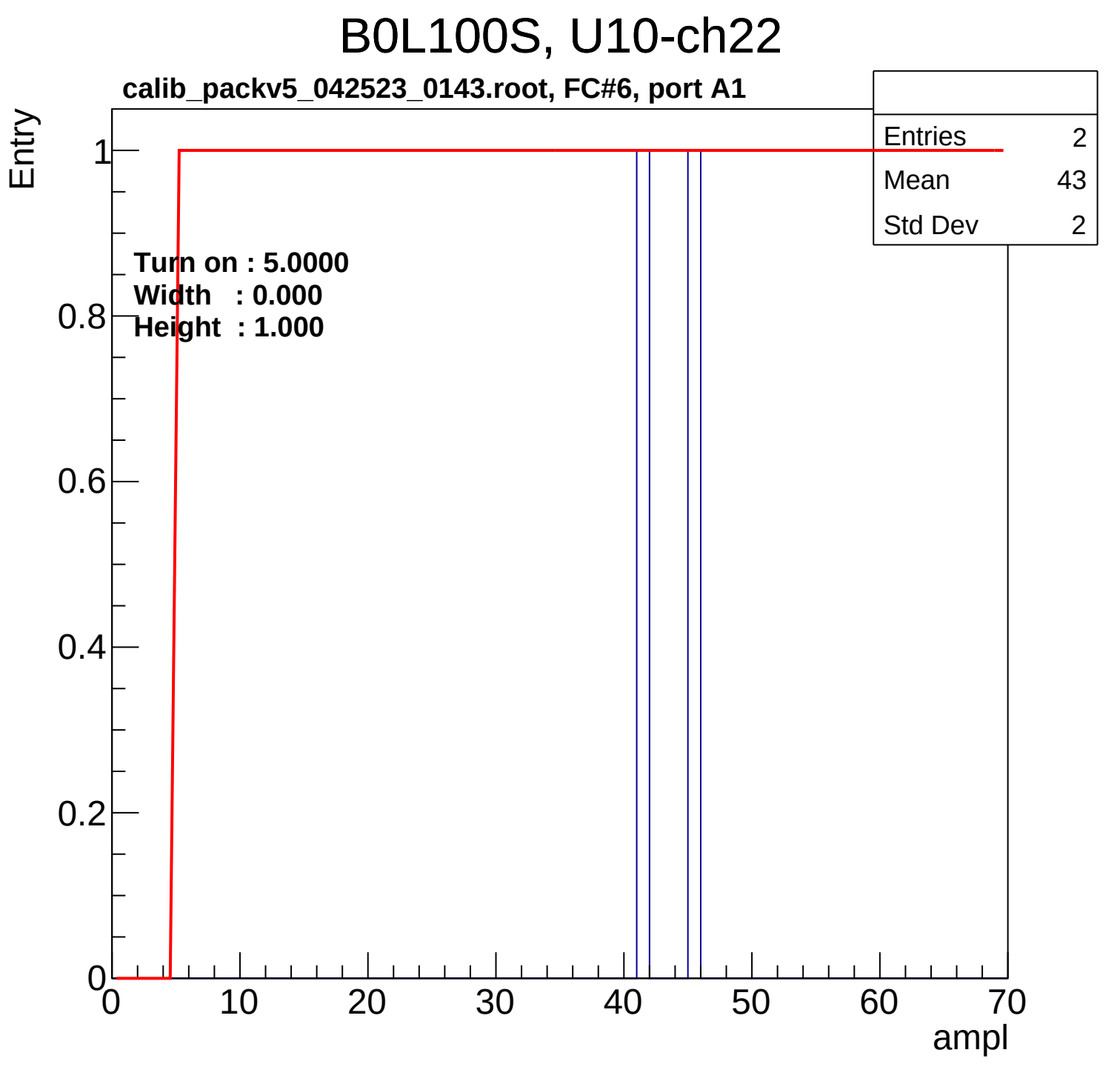
B0L100S, U10-ch22
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 43
Std Dev 2
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
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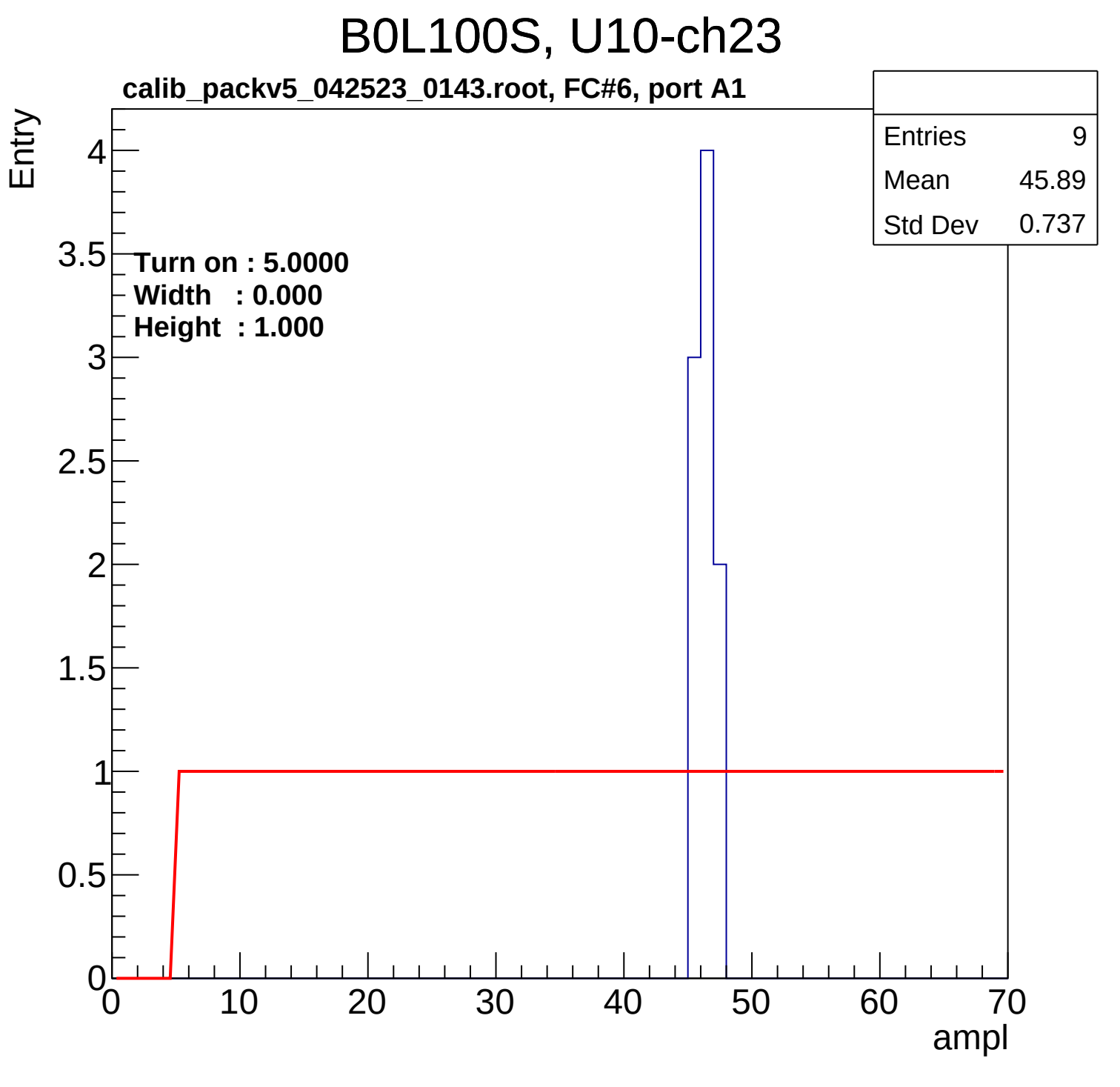
20
30
40
50
60
70


B0L100S, U10-ch23
calib_packv5_042523_0143.root, FC#6, port A1
Entries 9
Mean 45.89
Std Dev 0.737
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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1.5
2
2.5
3
3.5
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0
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60
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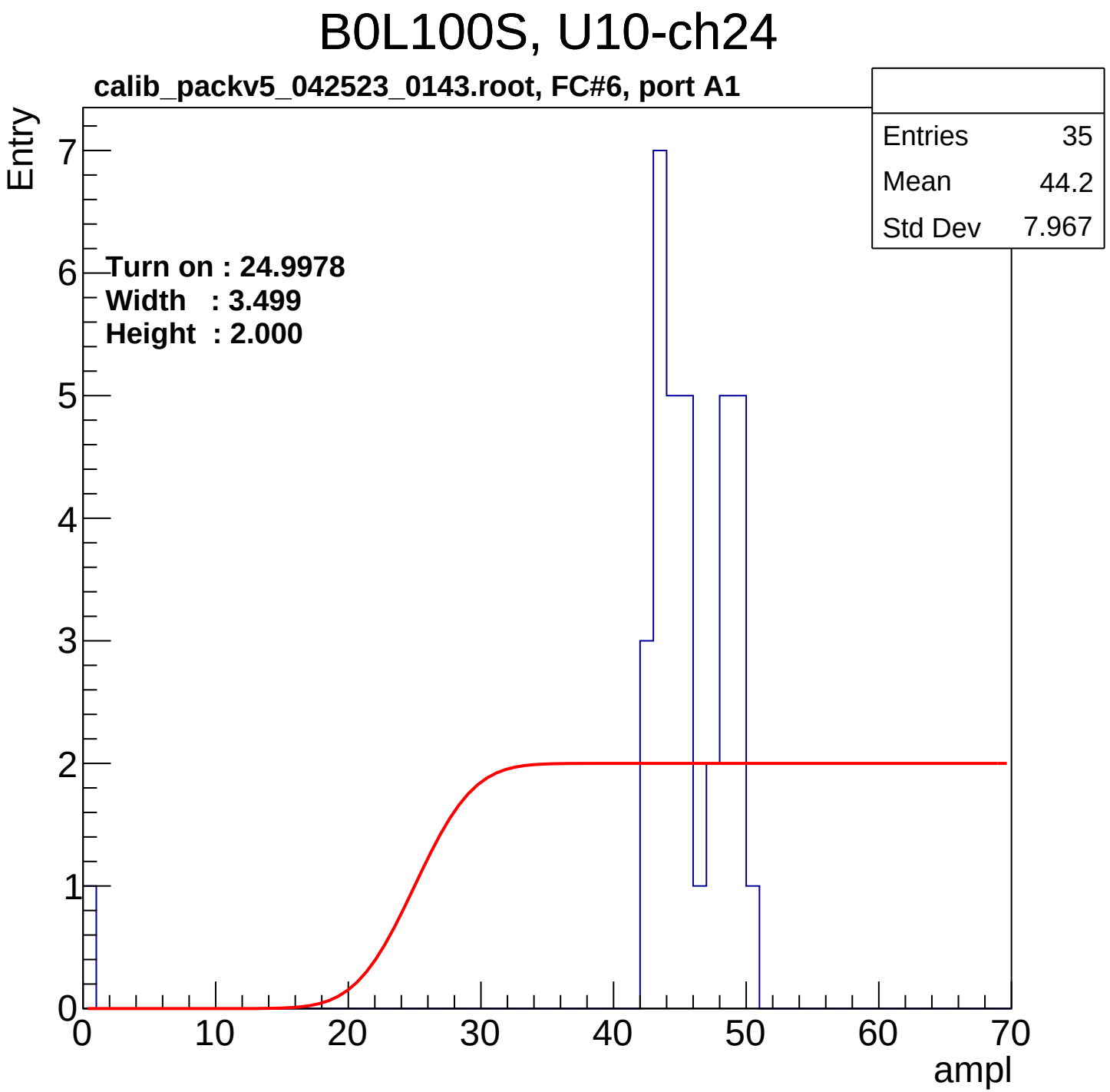
B0L100S, U10-ch24
calib_packv5_042523_0143.root, FC#6, port A1
Entries 35
Mean 44.2
Std Dev 7.967
Turn on : 24.9978
Width : 3.499
Height : 2.000
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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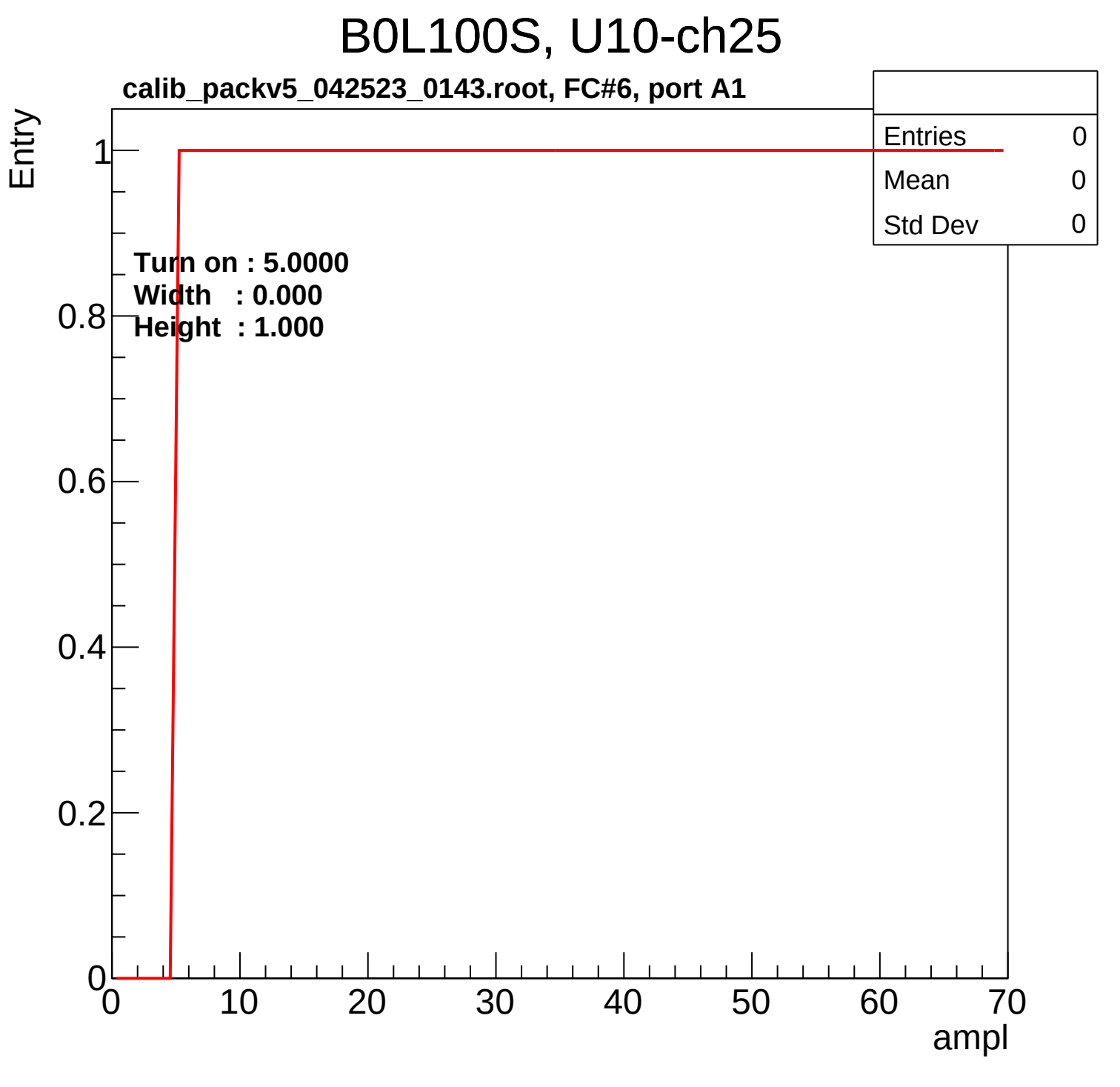
40
50
60
70


B0L100S, U10-ch25
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
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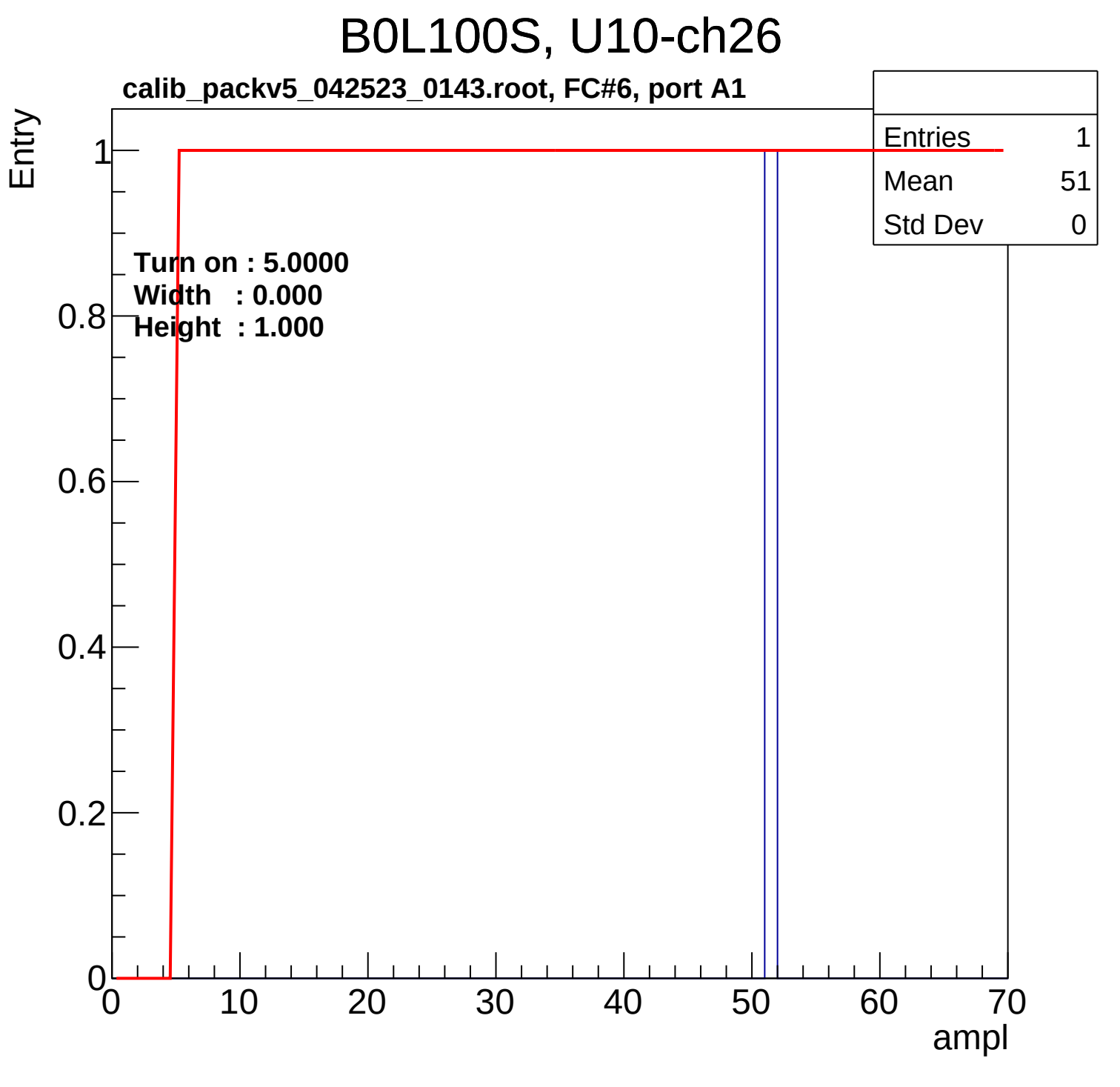
B0L100S, U10-ch26
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 51
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
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20
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40
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60
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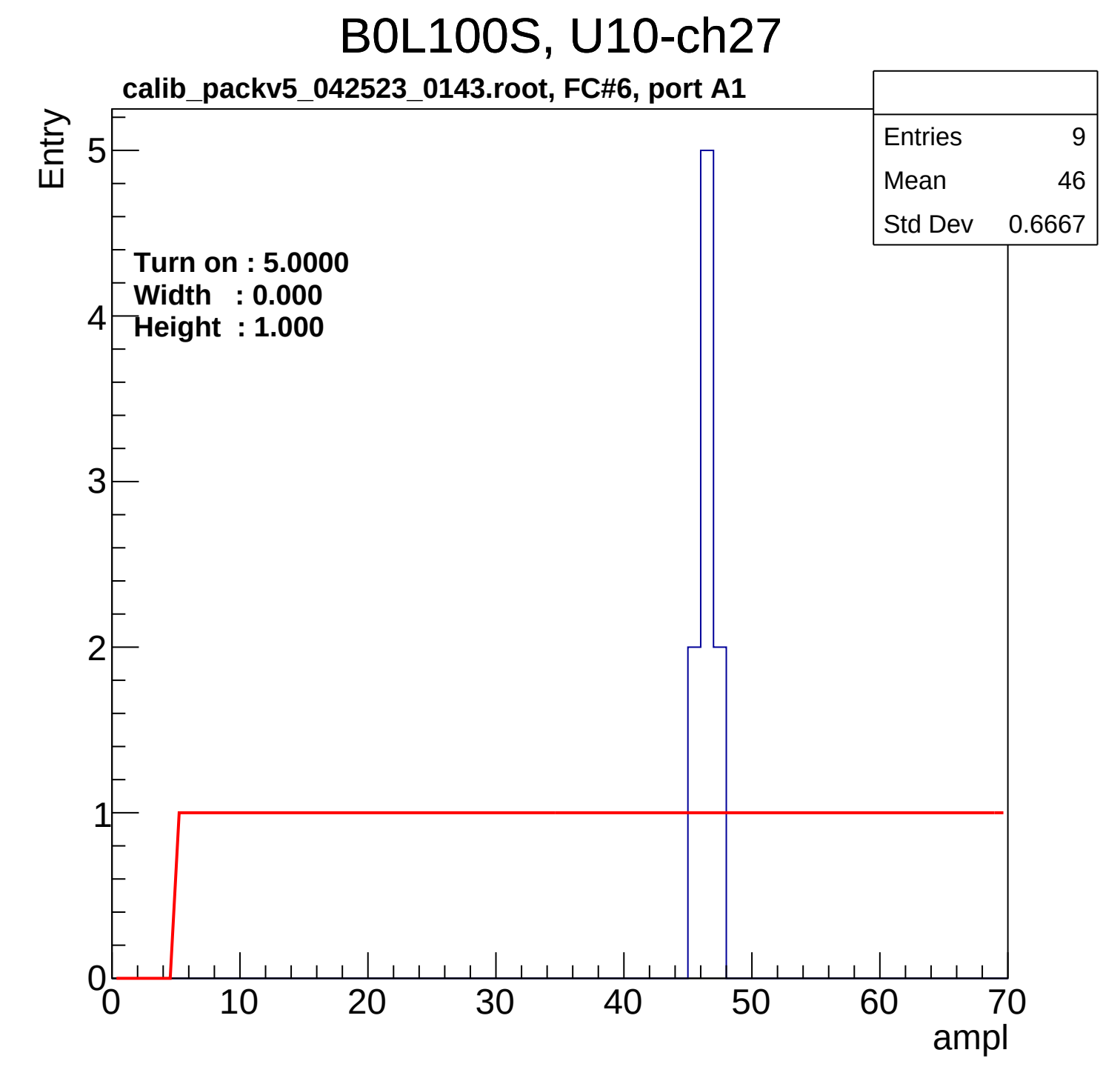
B0L100S, U10-ch27
calib_packv5_042523_0143.root, FC#6, port A1
Entries 9
Mean 46
Std Dev 0.6667
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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1
2
3
4
5
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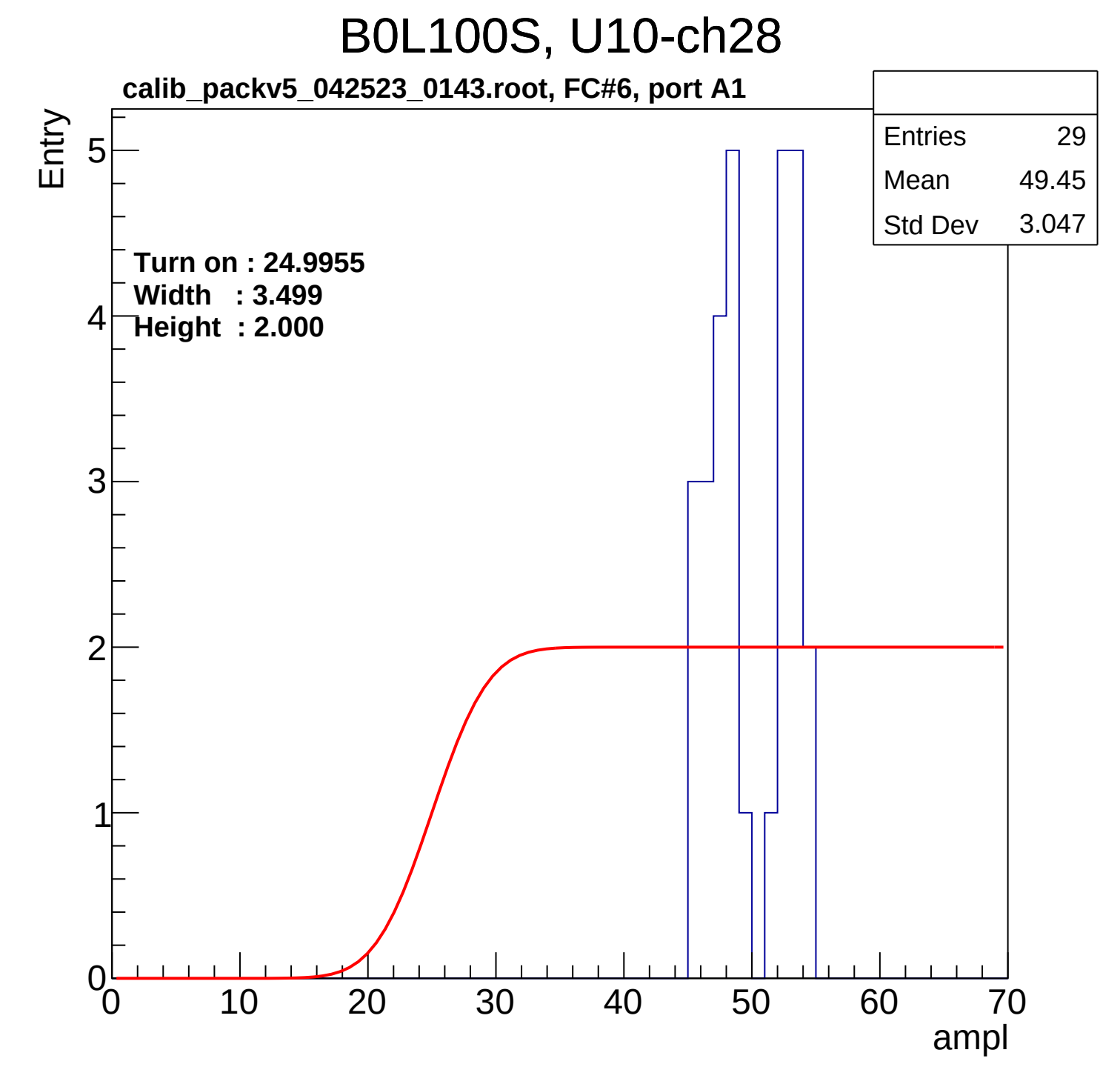
B0L100S, U10-ch28
calib_packv5_042523_0143.root, FC#6, port A1
Entries 29
Mean 49.45
Std Dev 3.047
Turn on : 24.9955
Width : 3.499
Height : 2.000
Entry
ampl
0
1
2
3
4
5
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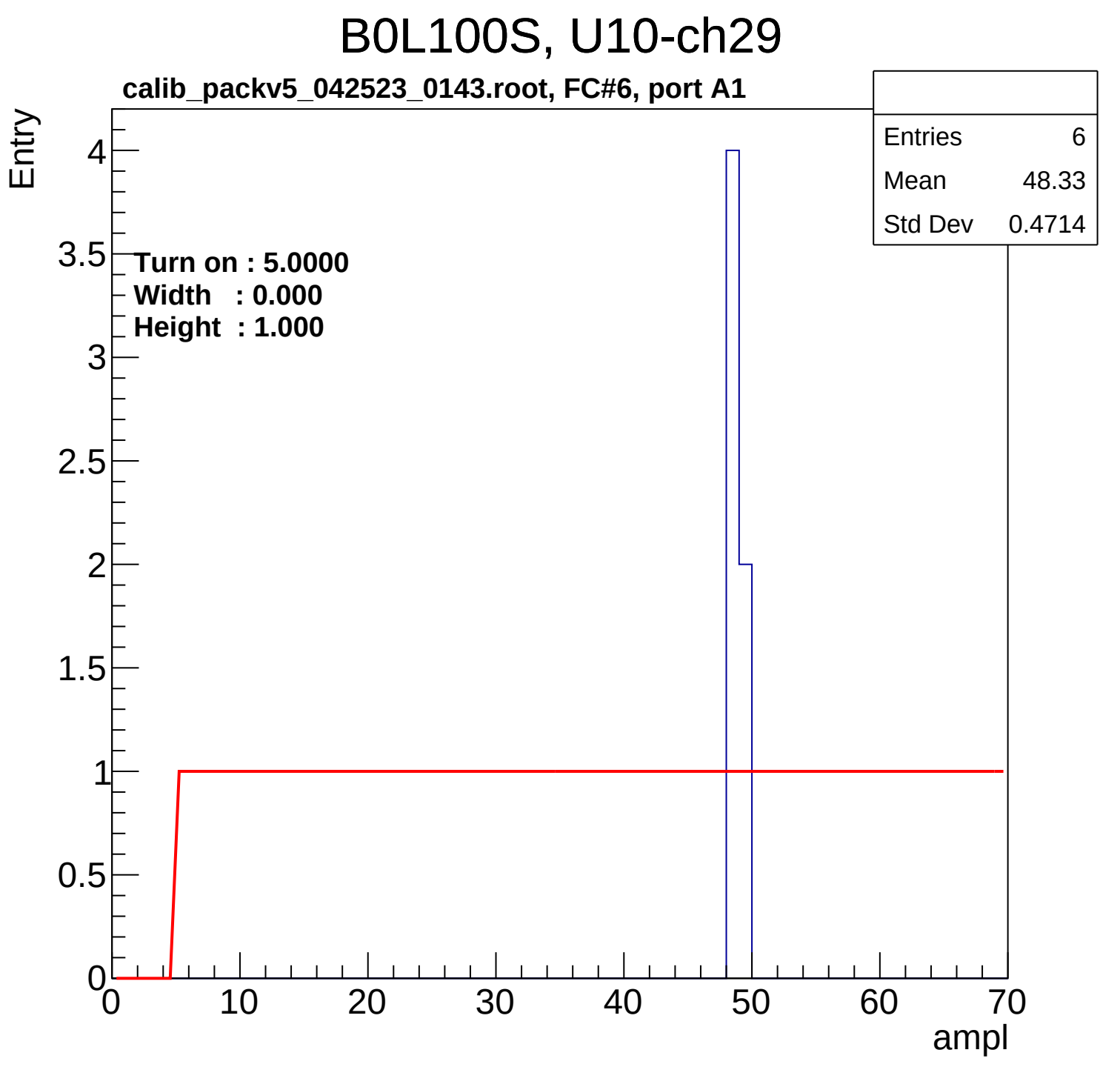
B0L100S, U10-ch29
calib_packv5_042523_0143.root, FC#6, port A1
Entries 6
Mean 48.33
Std Dev 0.4714
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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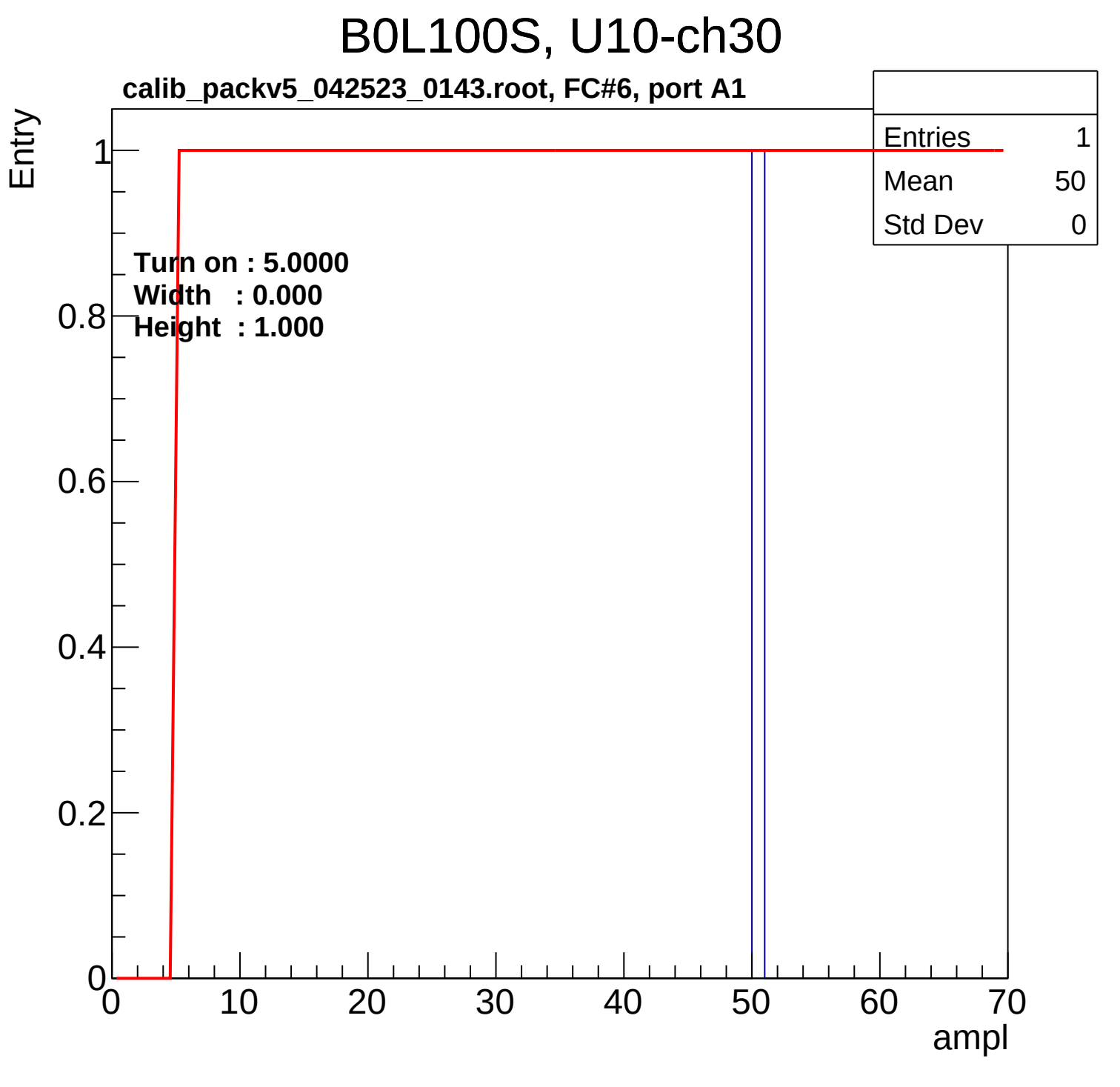
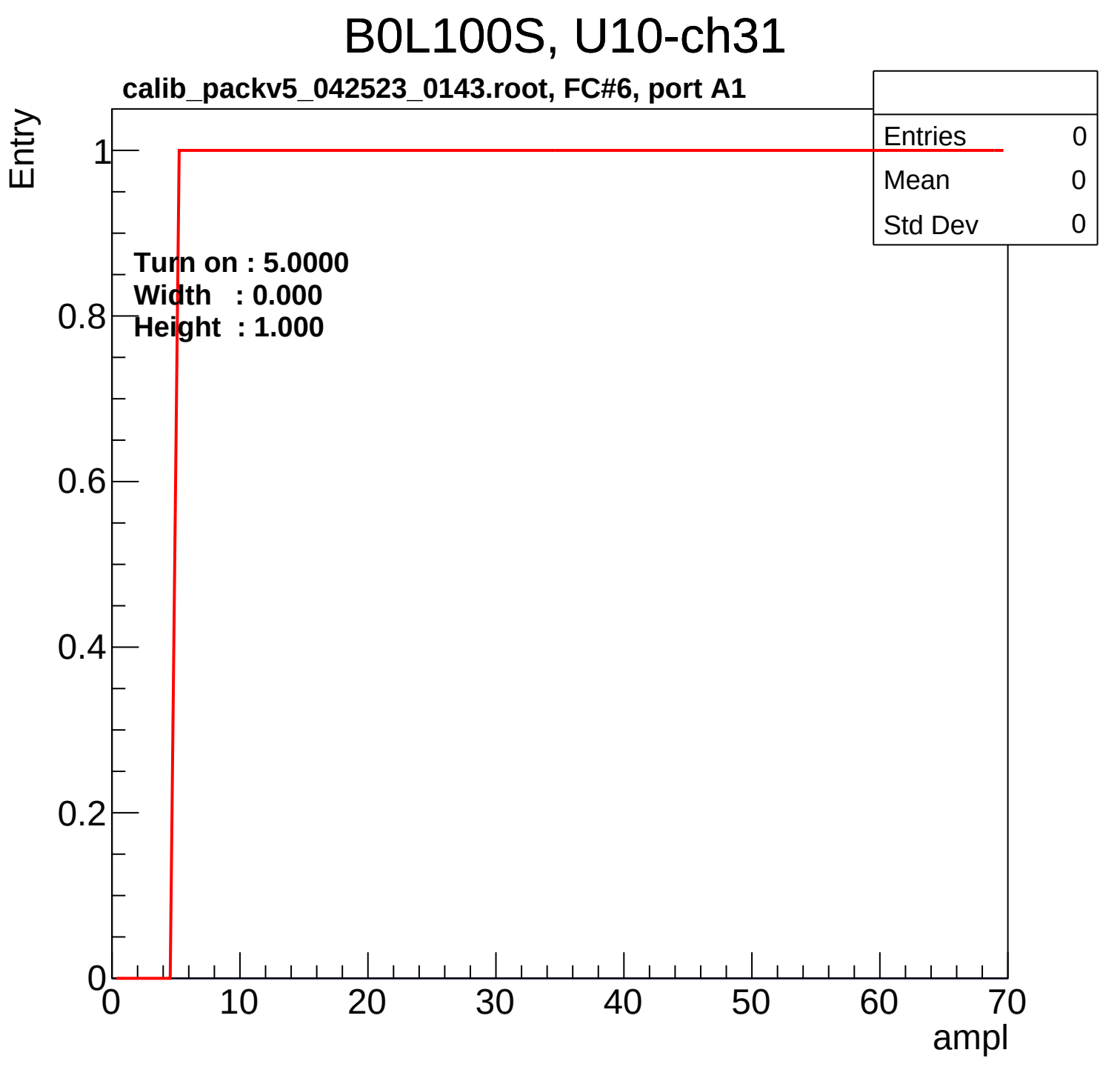
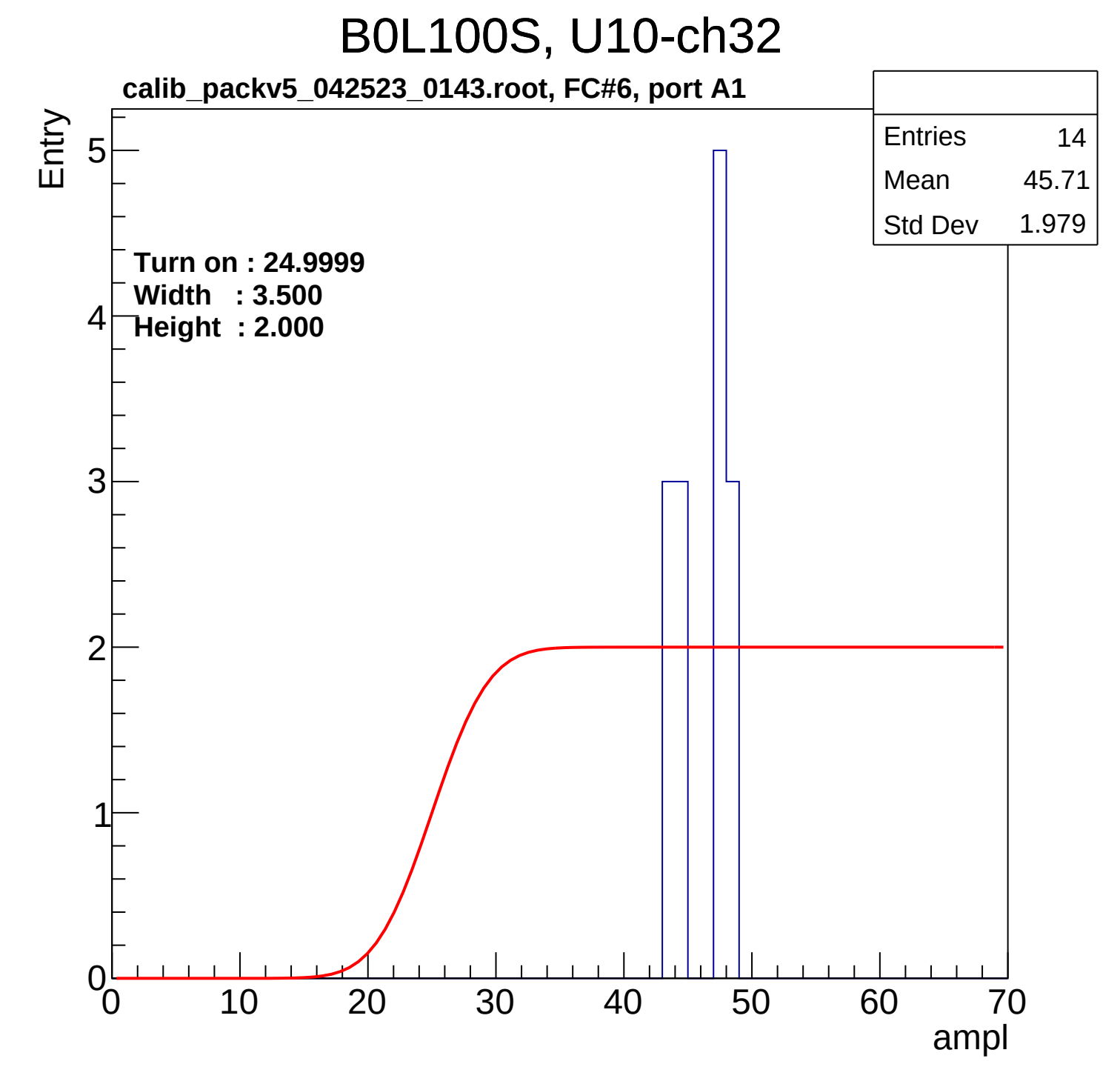
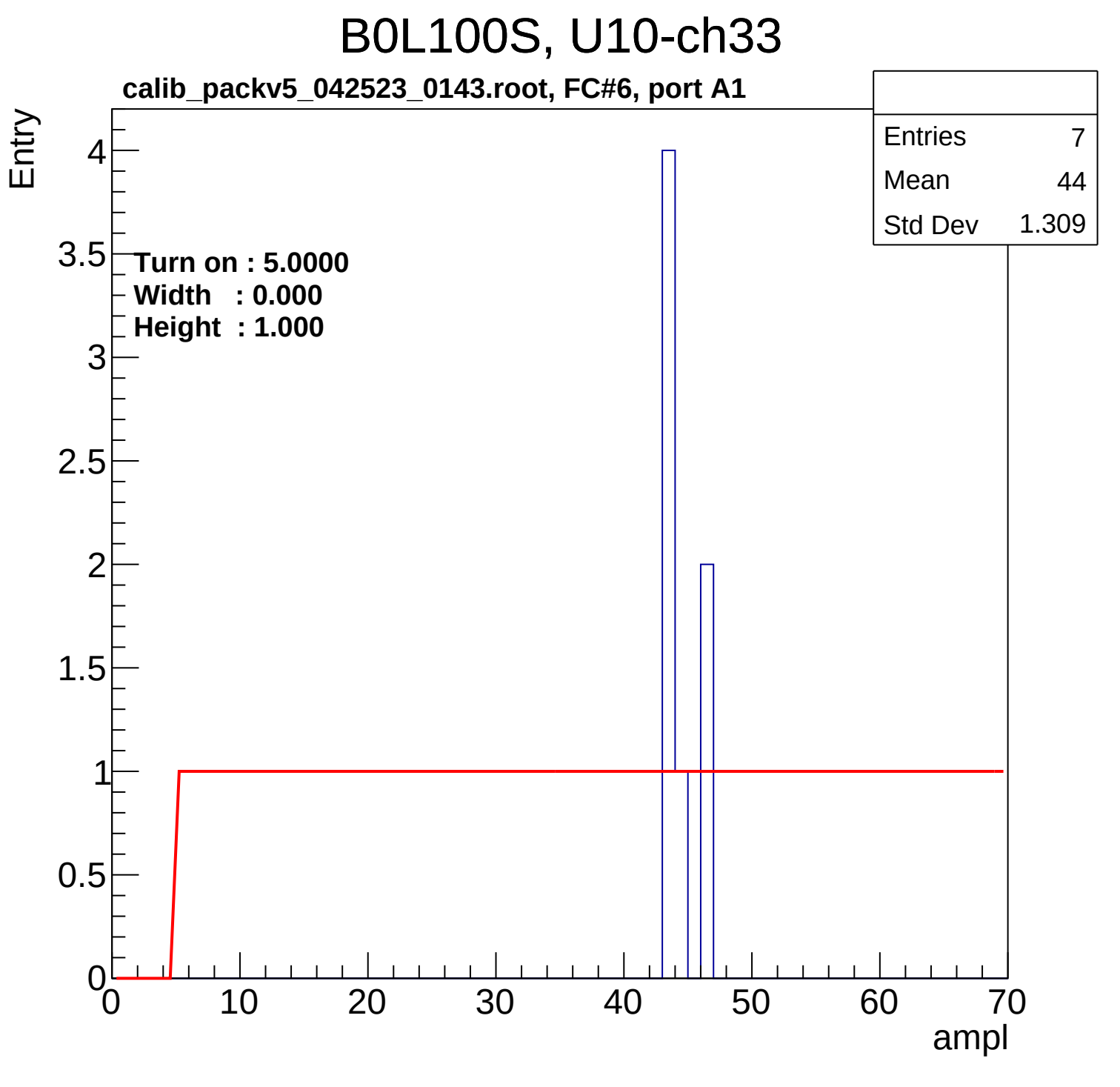
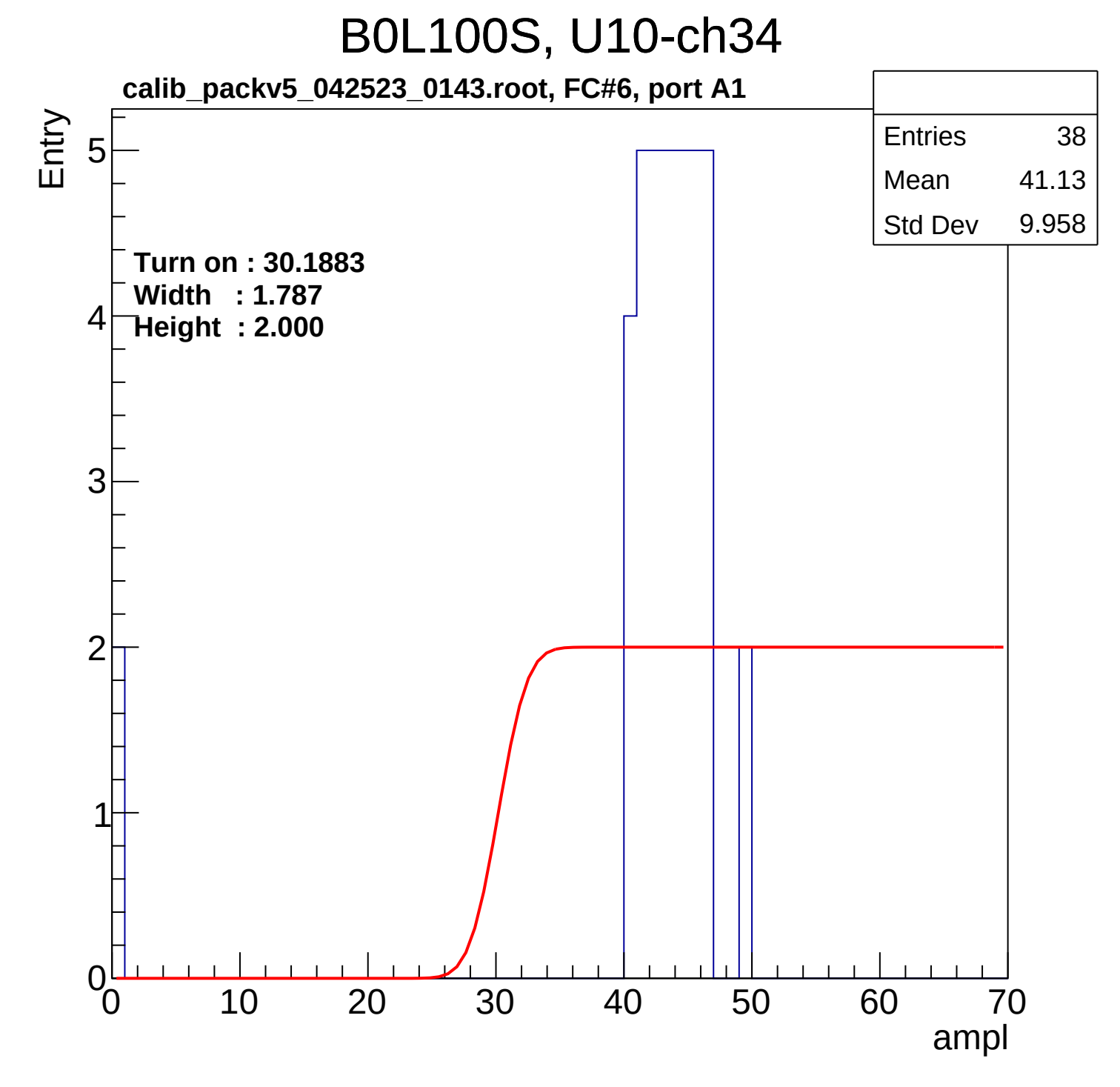
40
50
60
70

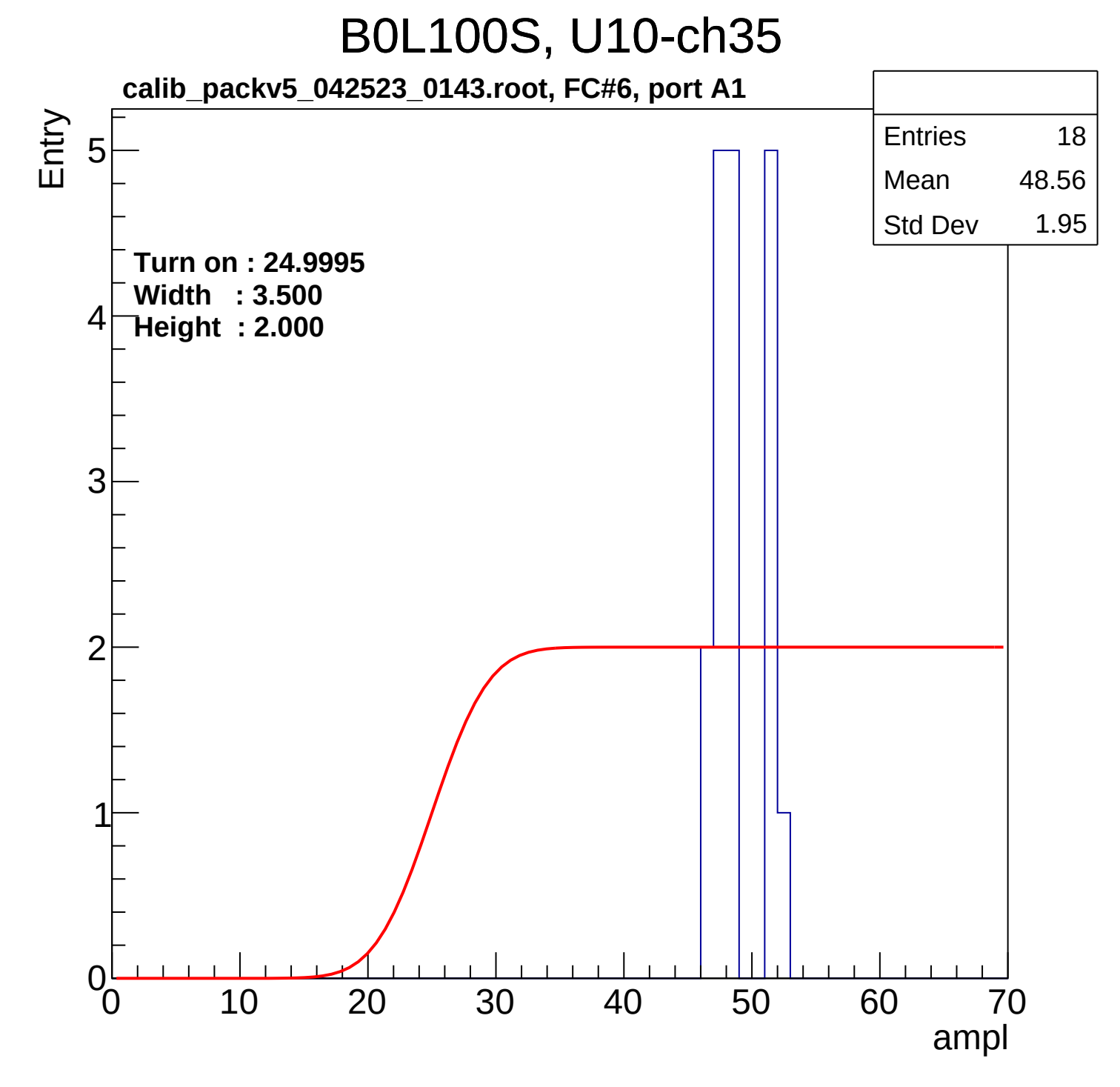

B0L100S, U10-ch30
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 50
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

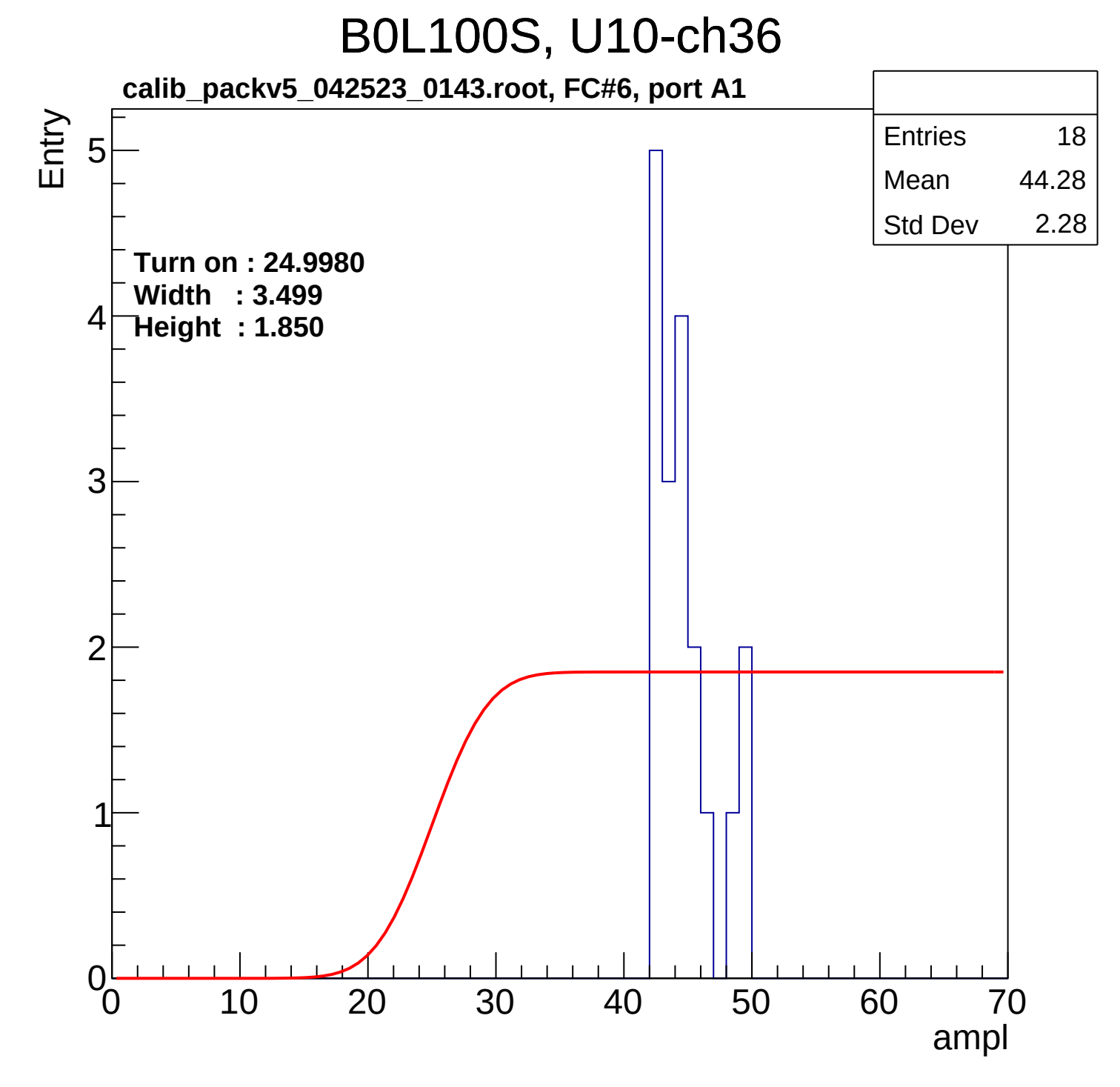

B0L100S, U10-ch31
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

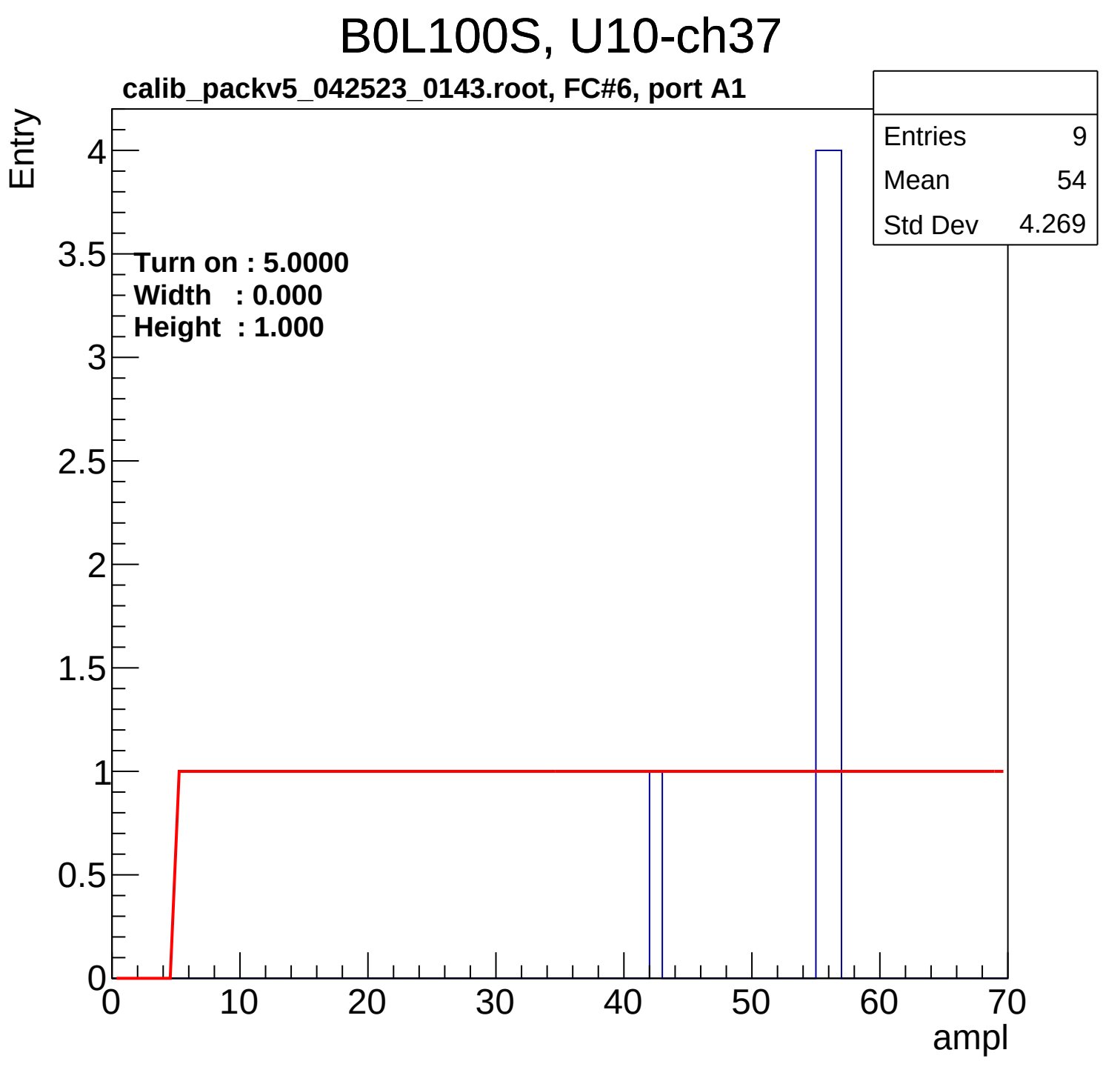

B0L100S, U10-ch32
calib_packv5_042523_0143.root, FC#6, port A1
Entries 14
Mean 45.71
Std Dev 1.979
Turn on : 24.9999
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

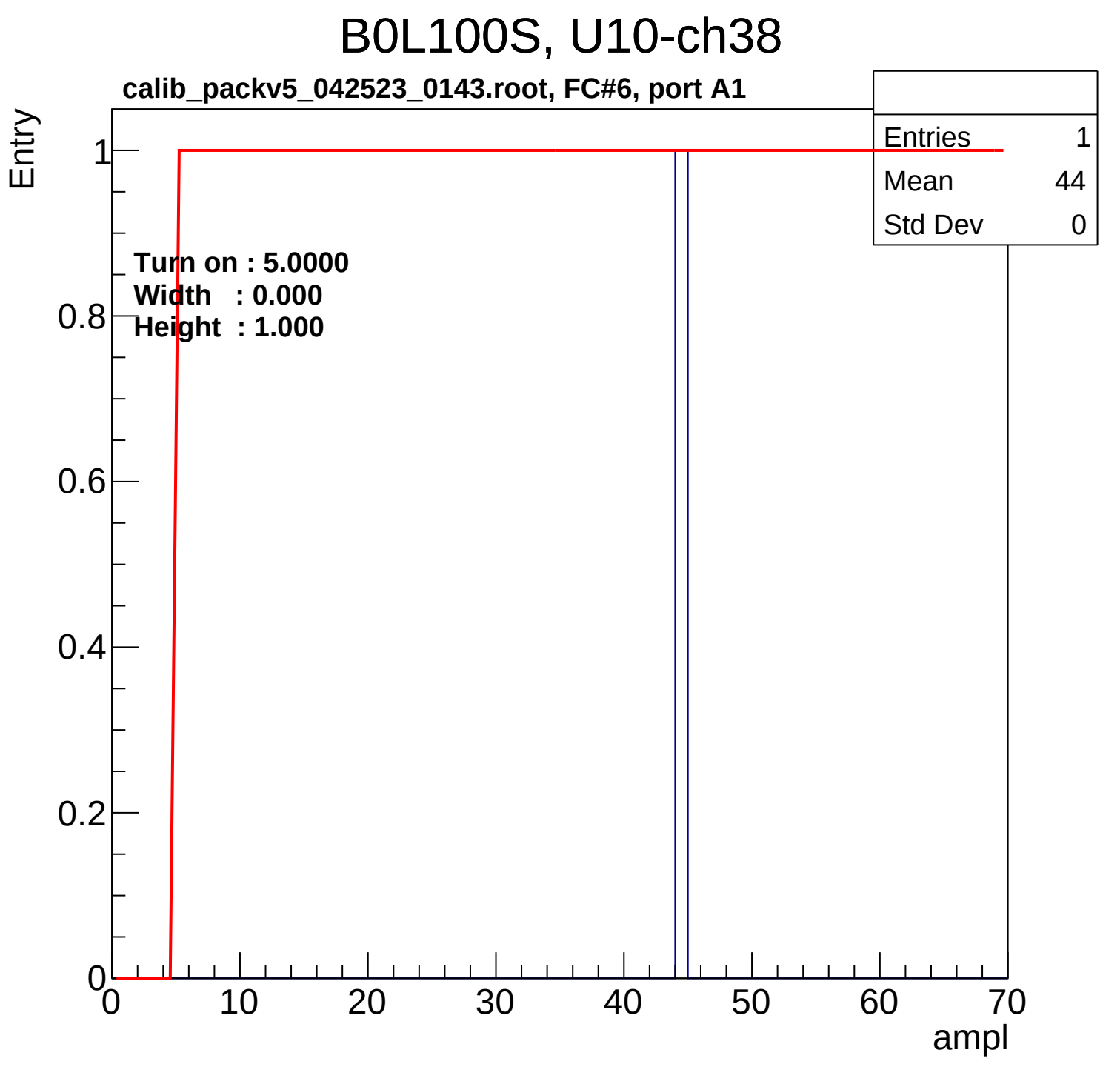

B0L100S, U10-ch33
calib_packv5_042523_0143.root, FC#6, port A1
Entries 7
Mean 44
Std Dev 1.309
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

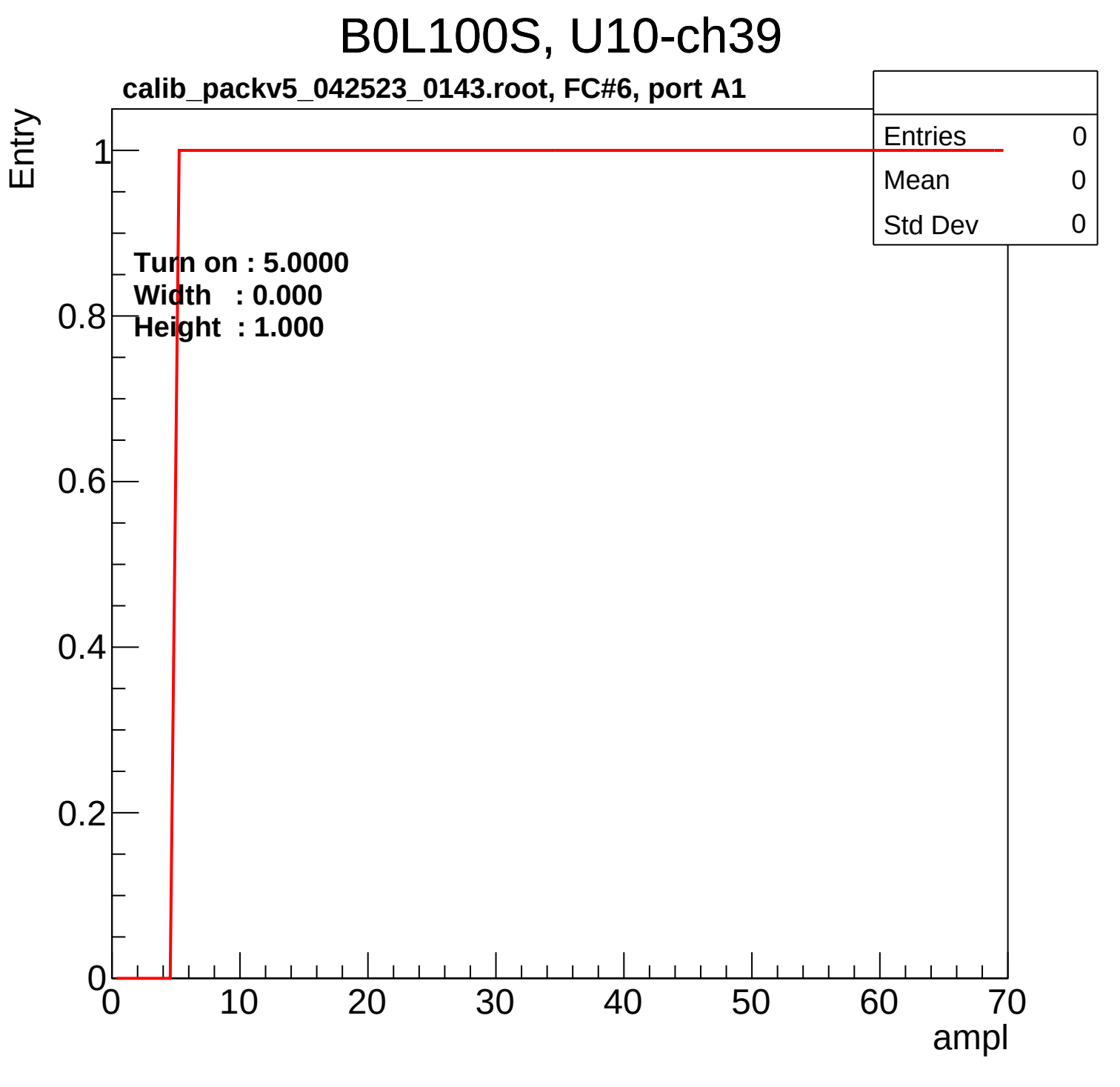

B0L100S, U10-ch34
calib_packv5_042523_0143.root, FC#6, port A1
Entries 38
Mean 41.13
Std Dev 9.958
Turn on : 30.1883
Width : 1.787
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

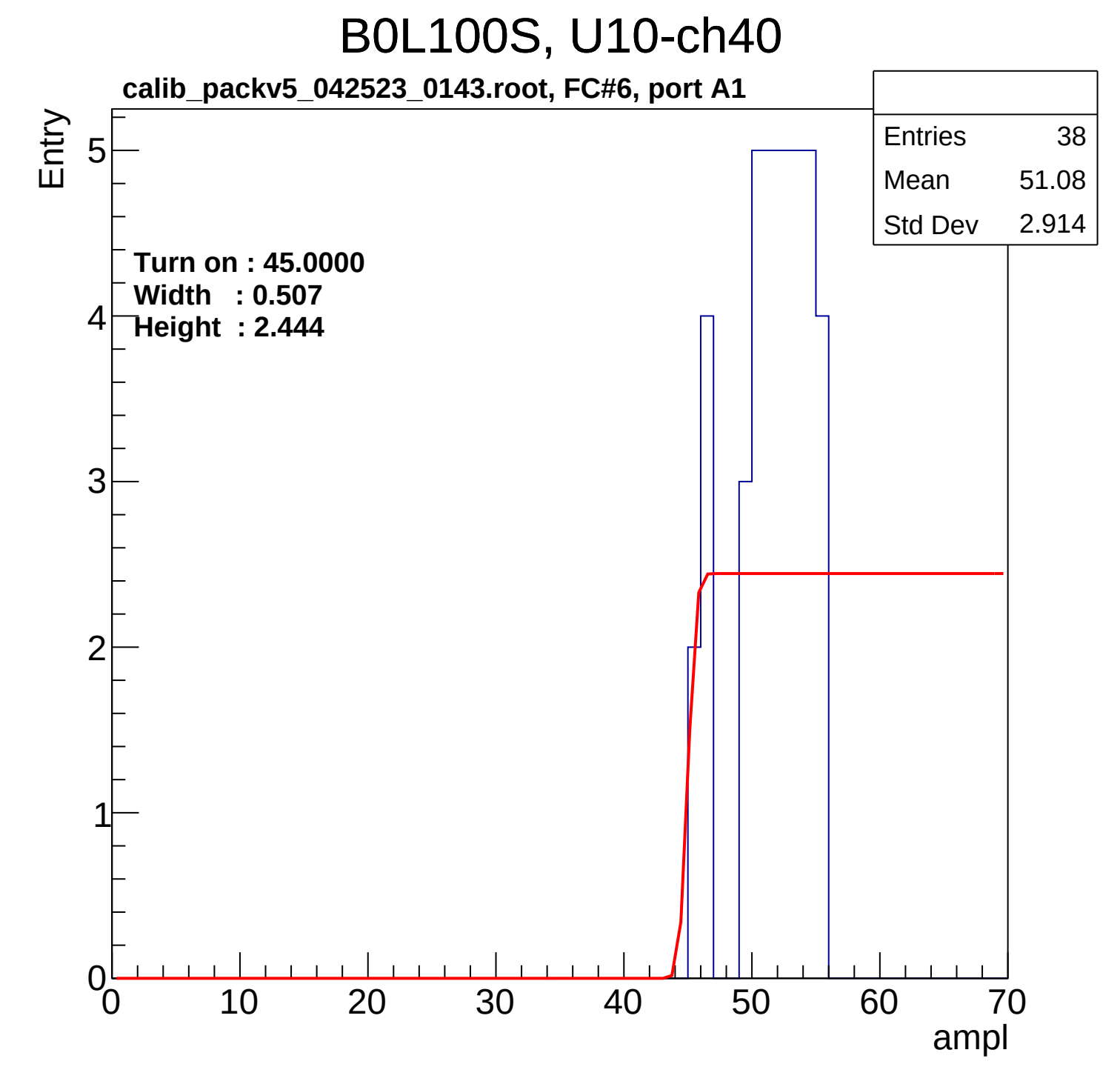

B0L100S, U10-ch35
calib_packv5_042523_0143.root, FC#6, port A1
Entries 18
Mean 48.56
Std Dev 1.95
Turn on : 24.9995
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

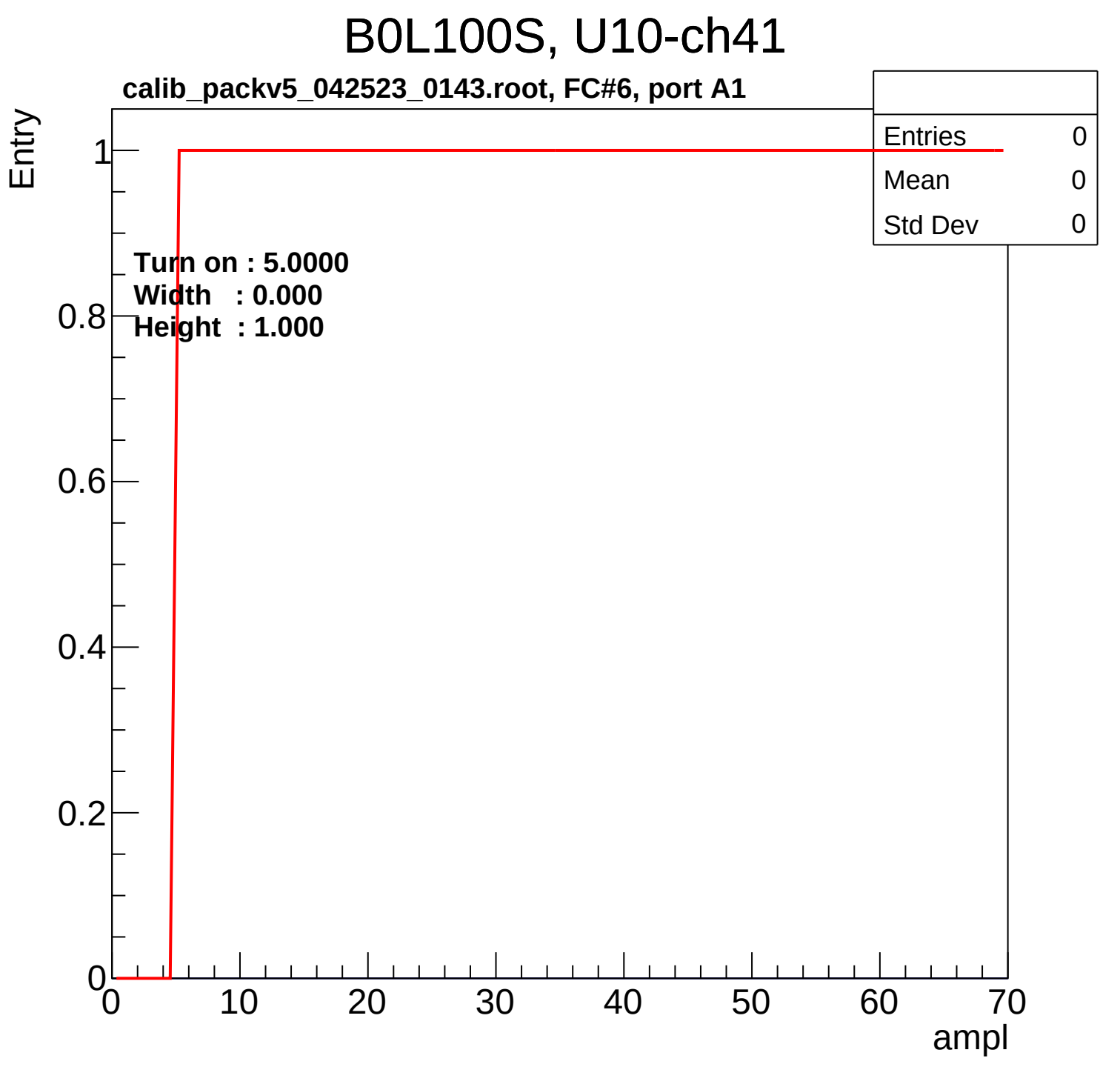

B0L100S, U10-ch36
calib_packv5_042523_0143.root, FC#6, port A1
Entries 18
Mean 44.28
Std Dev 2.28
Turn on : 24.9980
Width : 3.499
Height : 1.850
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

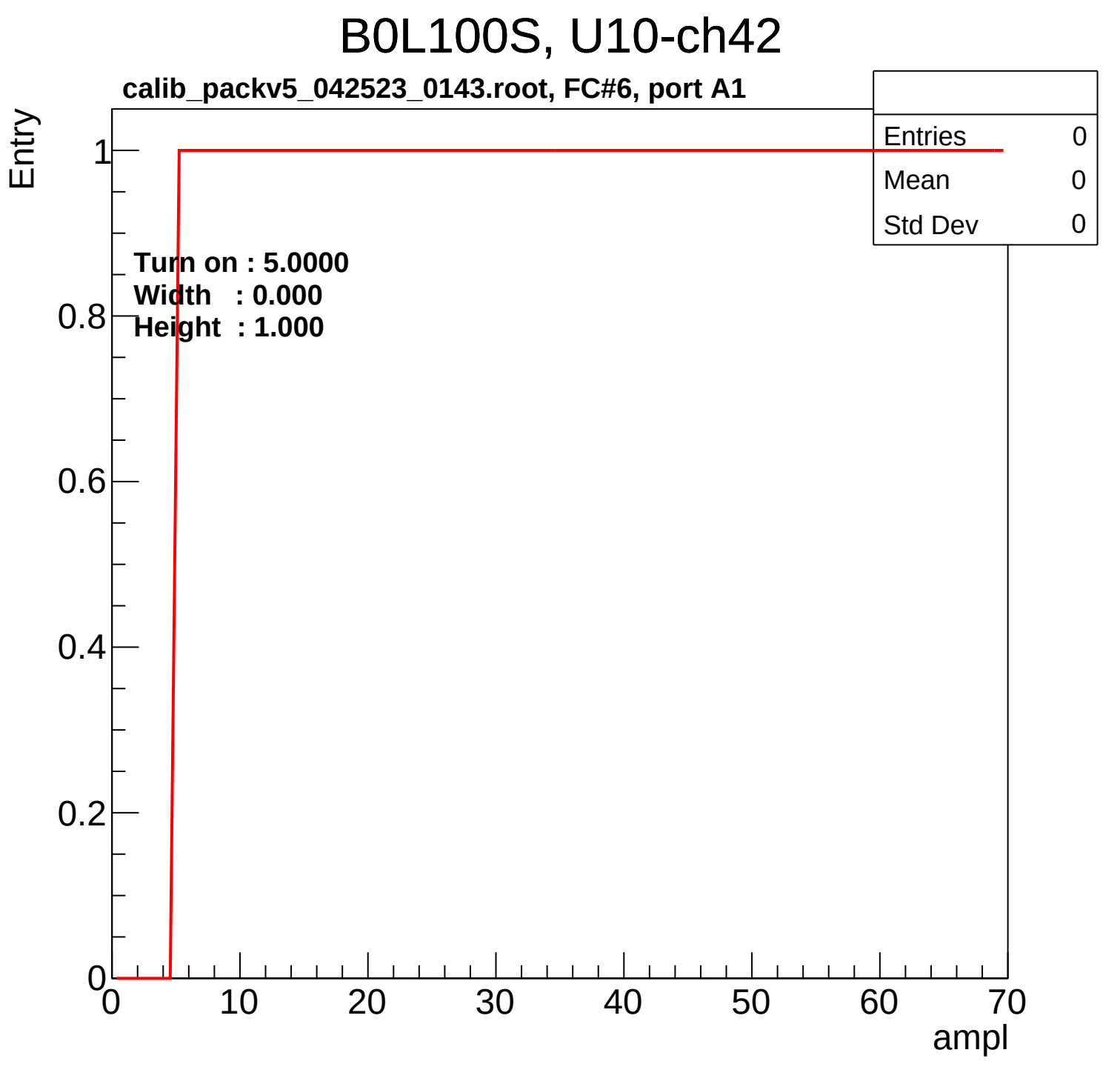

B0L100S, U10-ch37
calib_packv5_042523_0143.root, FC#6, port A1
Entries 9
Mean 54
Std Dev 4.269
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

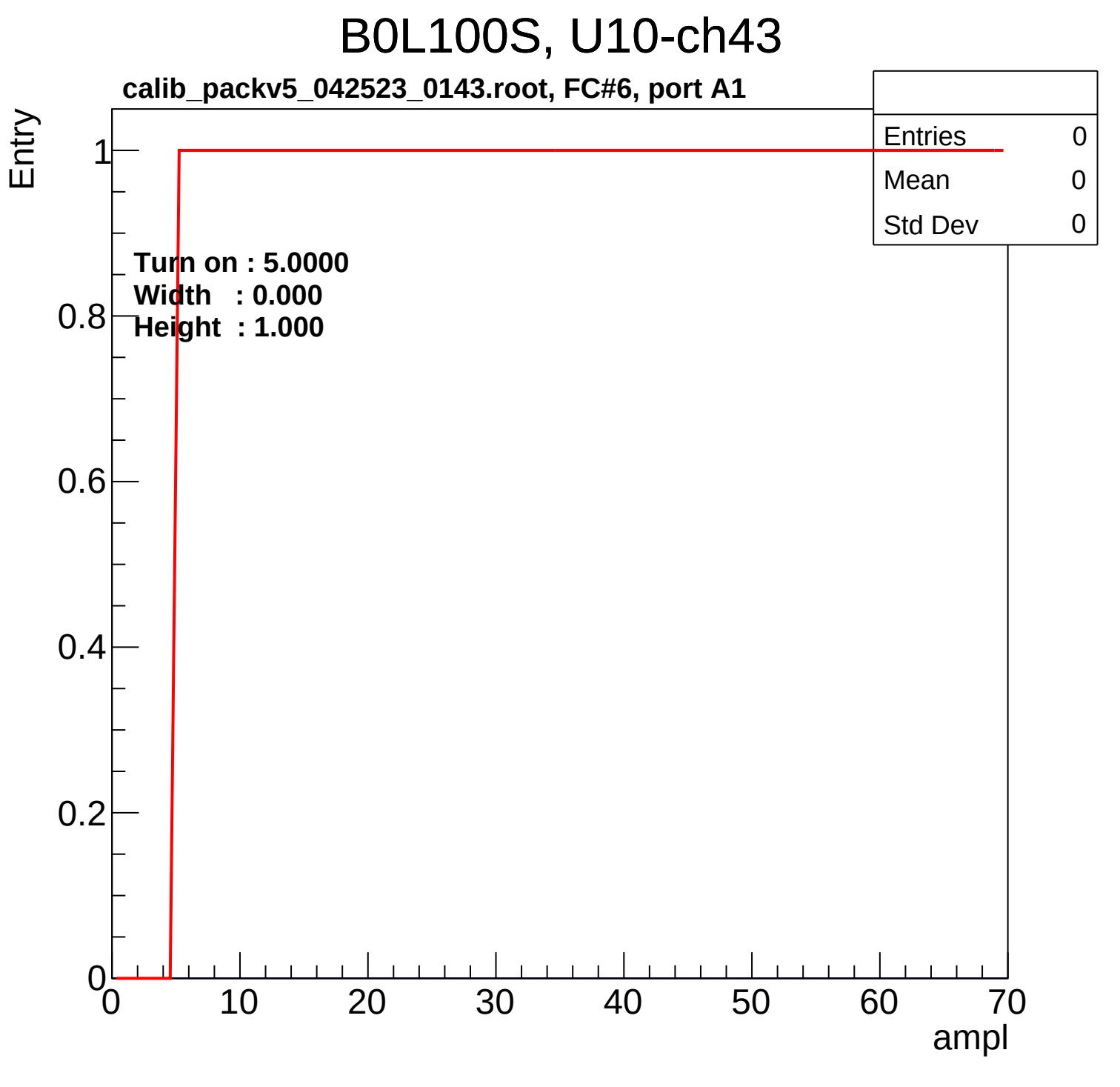

B0L100S, U10-ch38
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 44
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

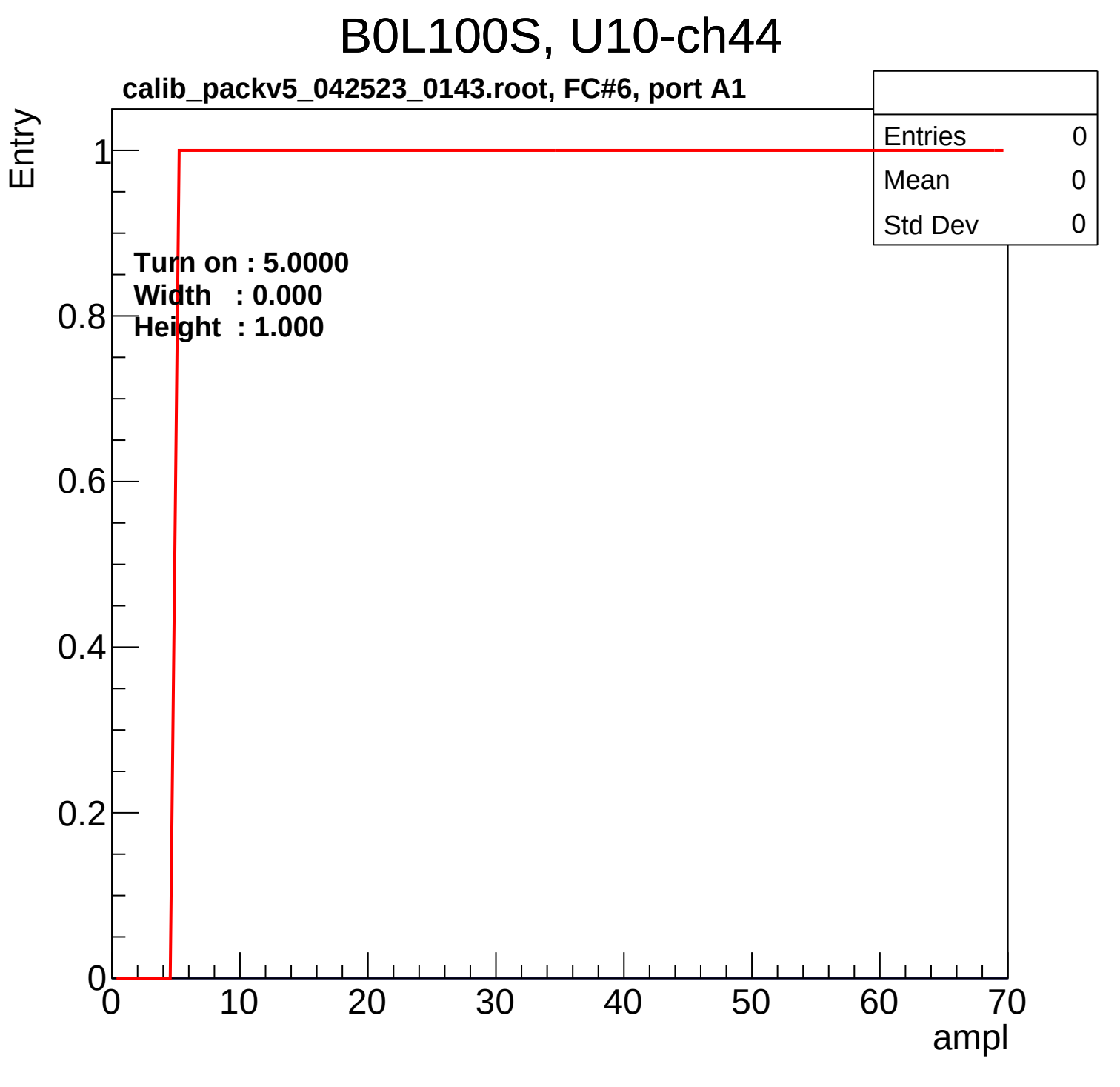

B0L100S, U10-ch39
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

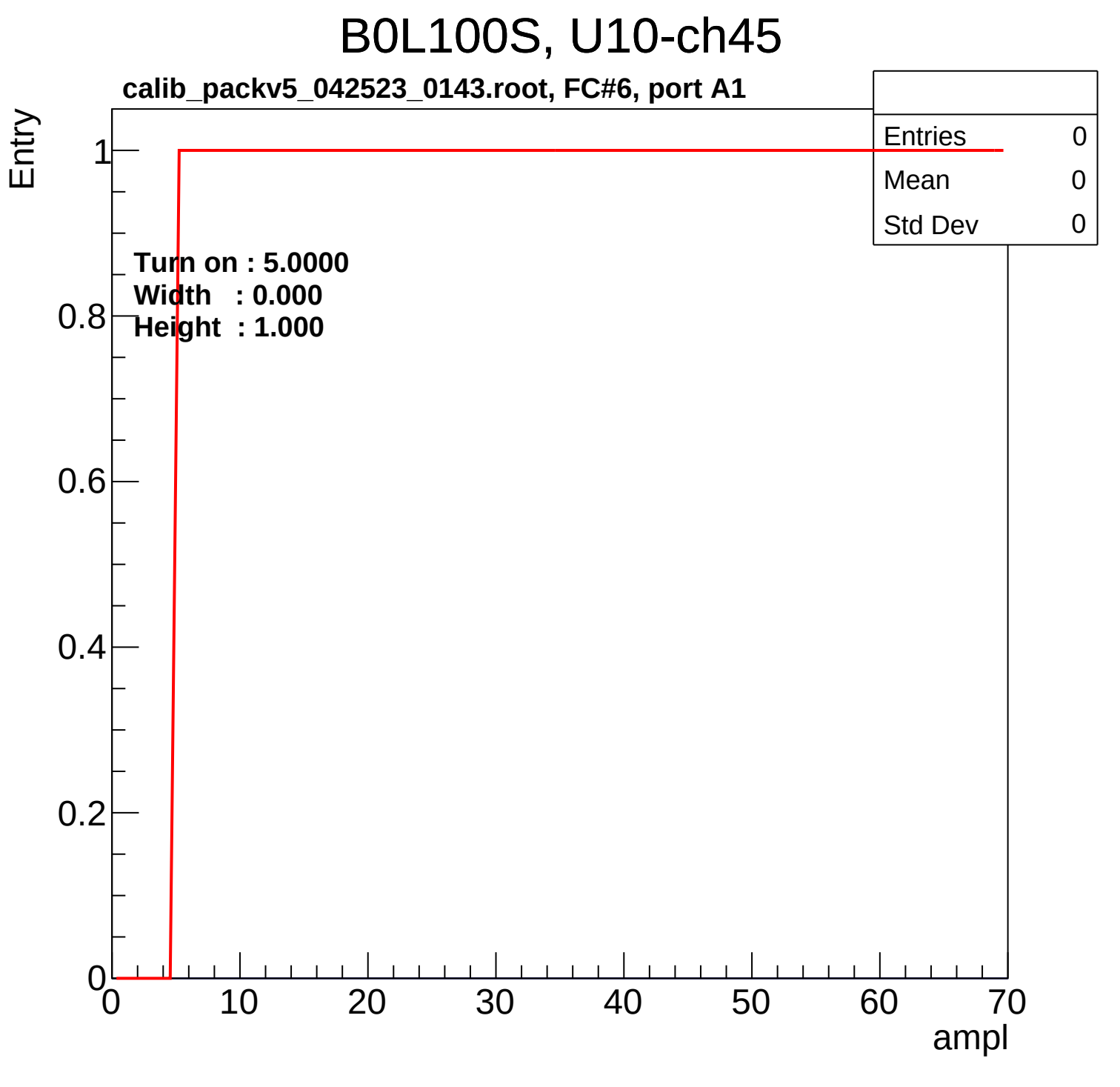

B0L100S, U10-ch40
calib_packv5_042523_0143.root, FC#6, port A1
Entries 38
Mean 51.08
Std Dev 2.914
Turn on : 45.0000
Width : 0.507
Height : 2.444
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

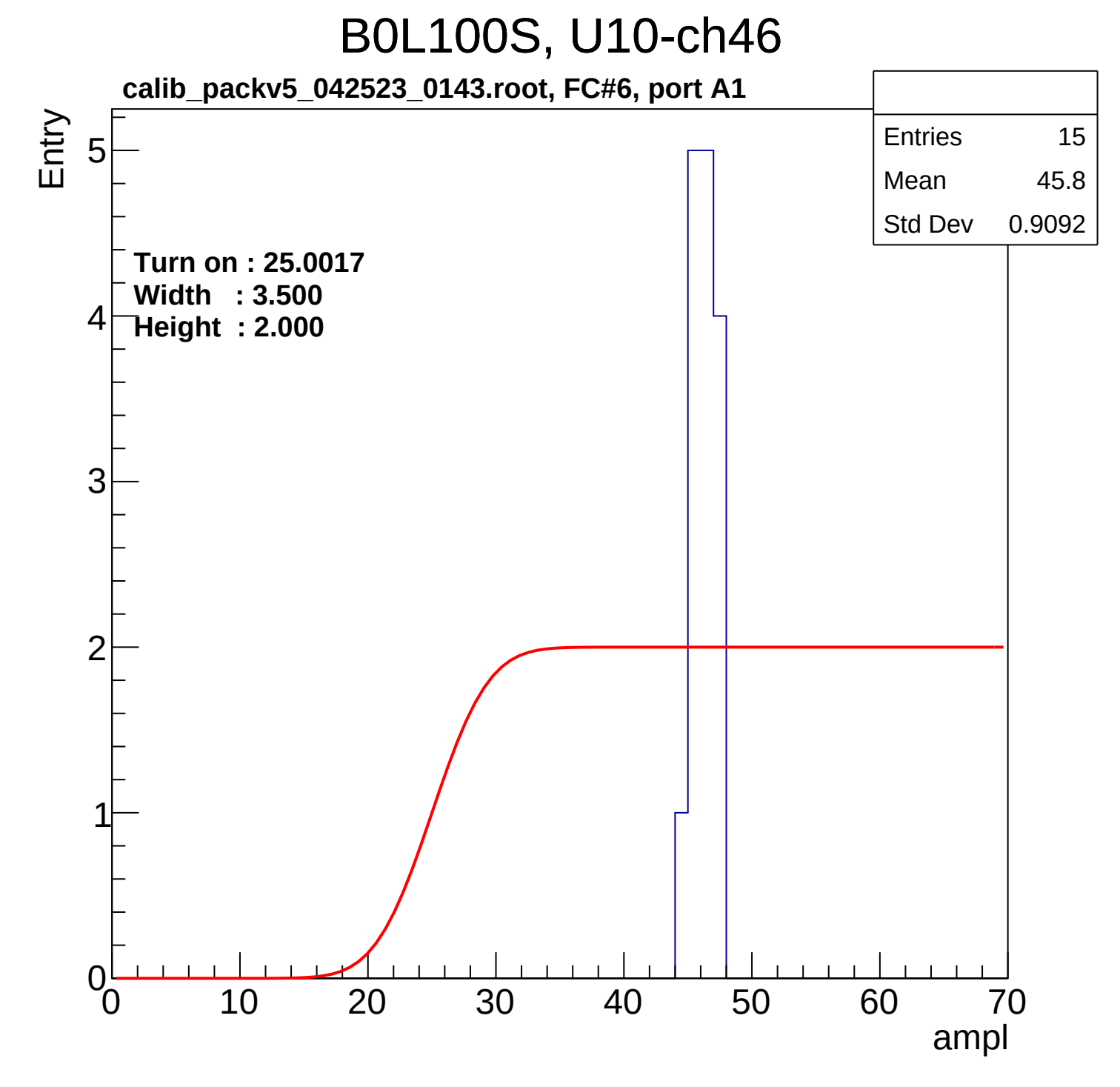

B0L100S, U10-ch41
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

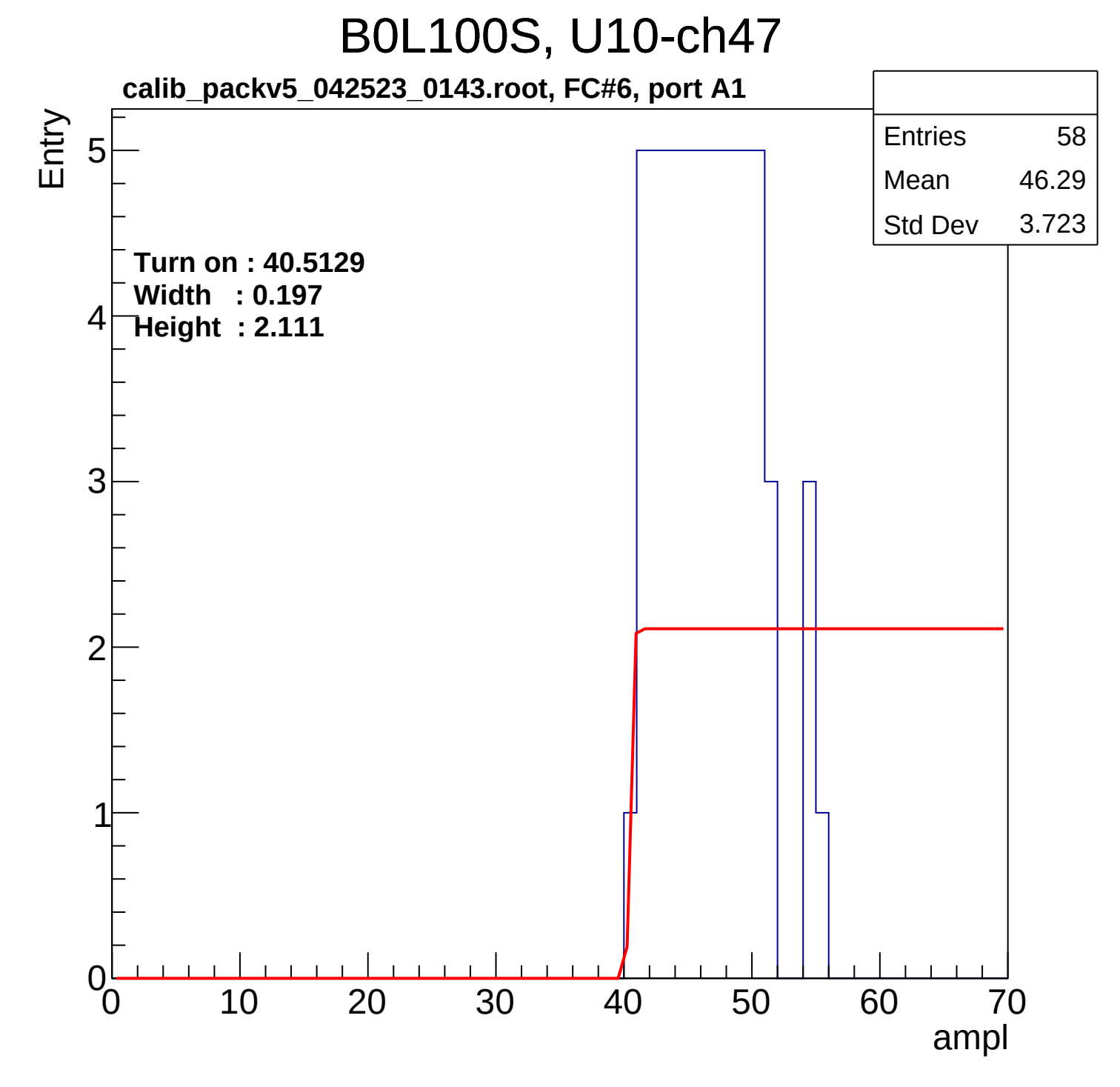

B0L100S, U10-ch42
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

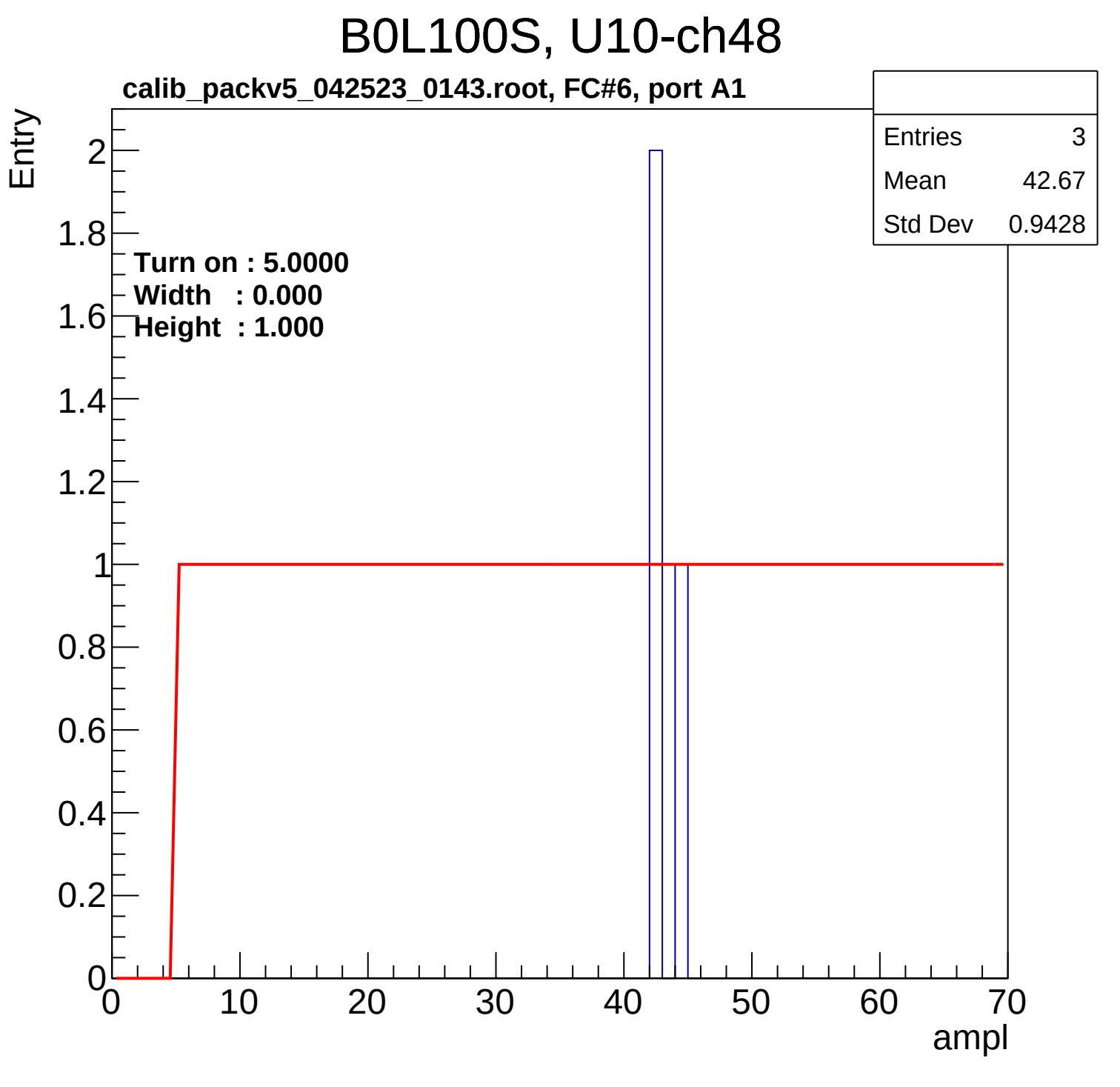

B0L100S, U10-ch43
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

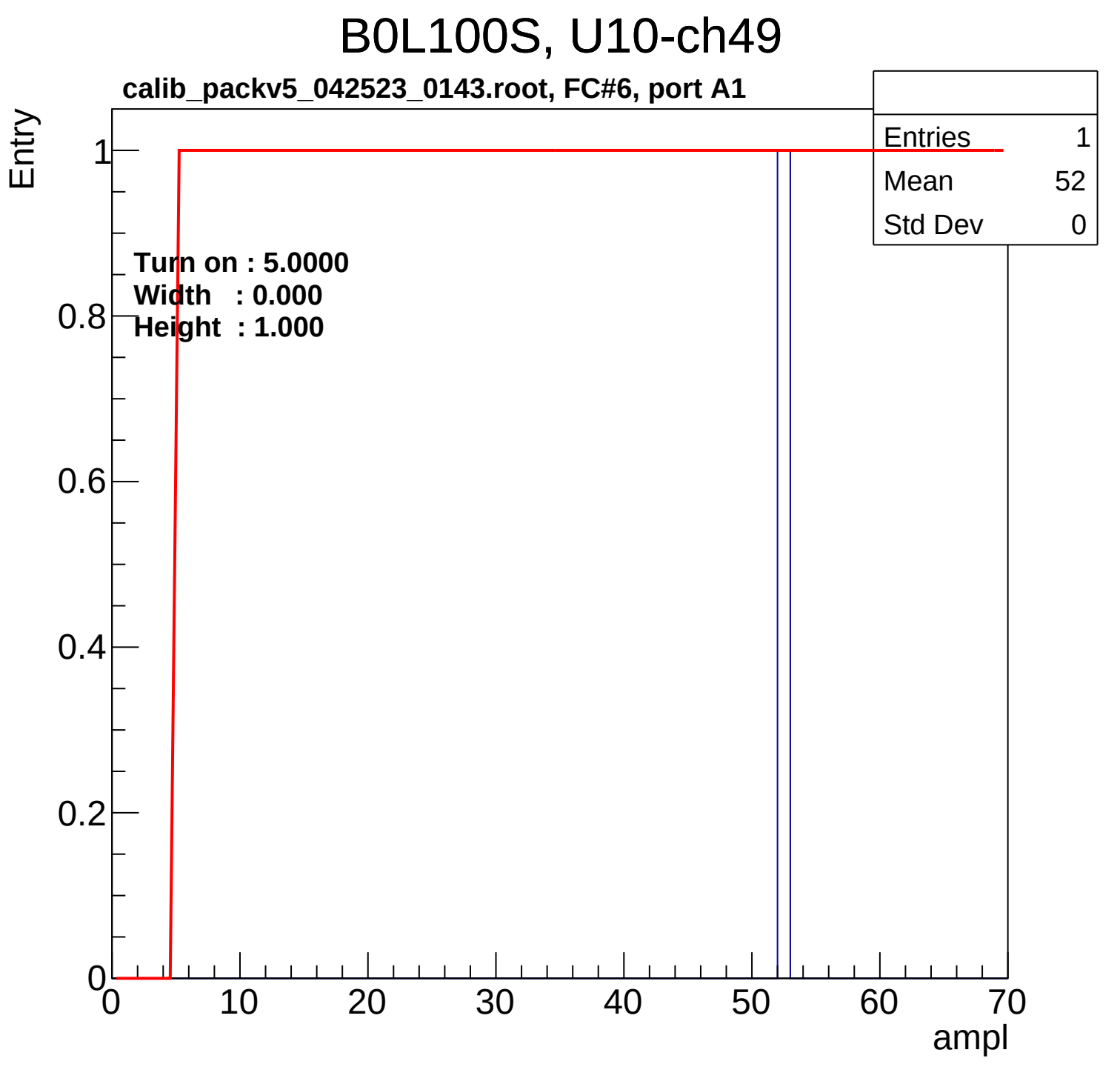

B0L100S, U10-ch44
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

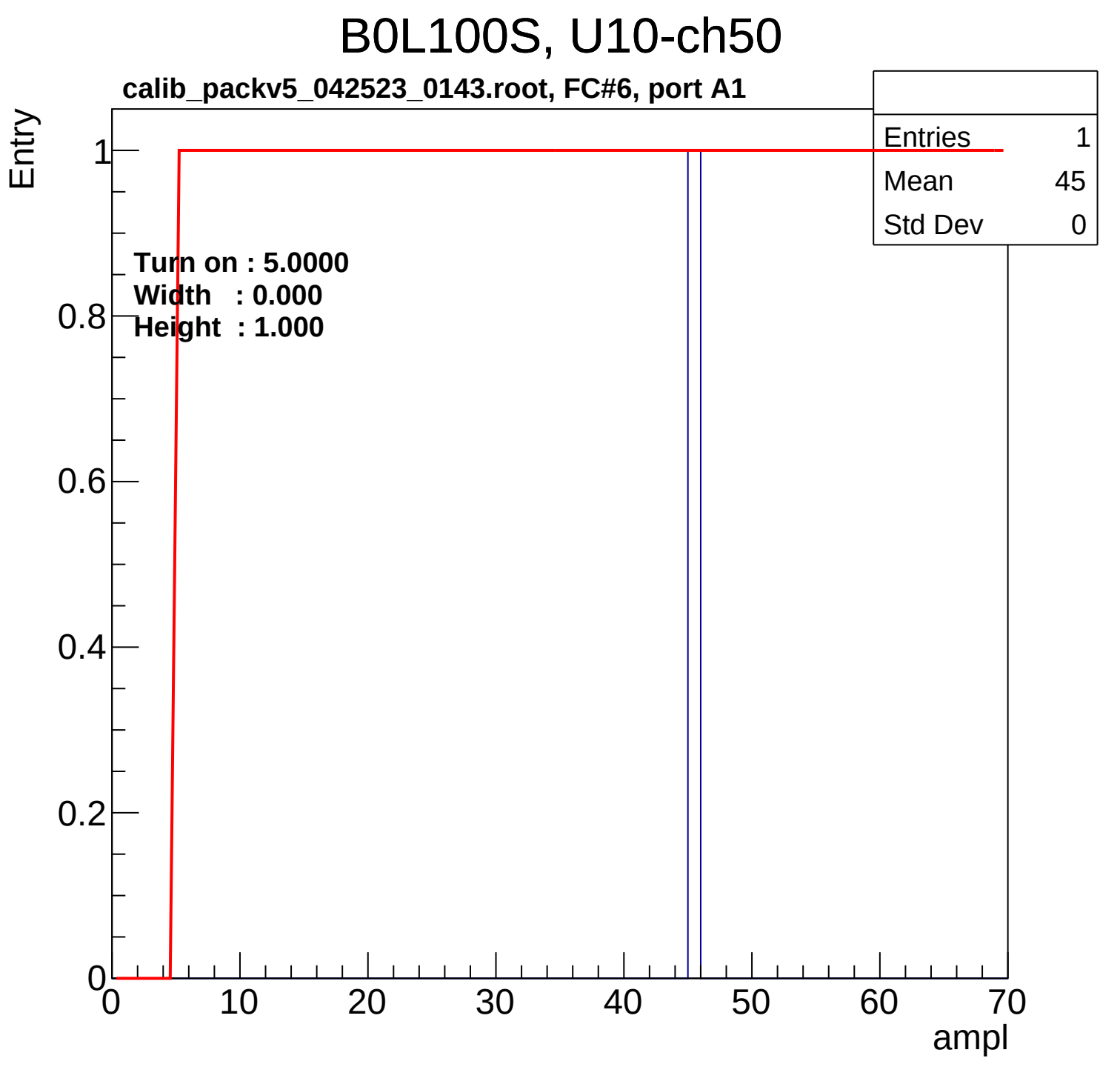

B0L100S, U10-ch45
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

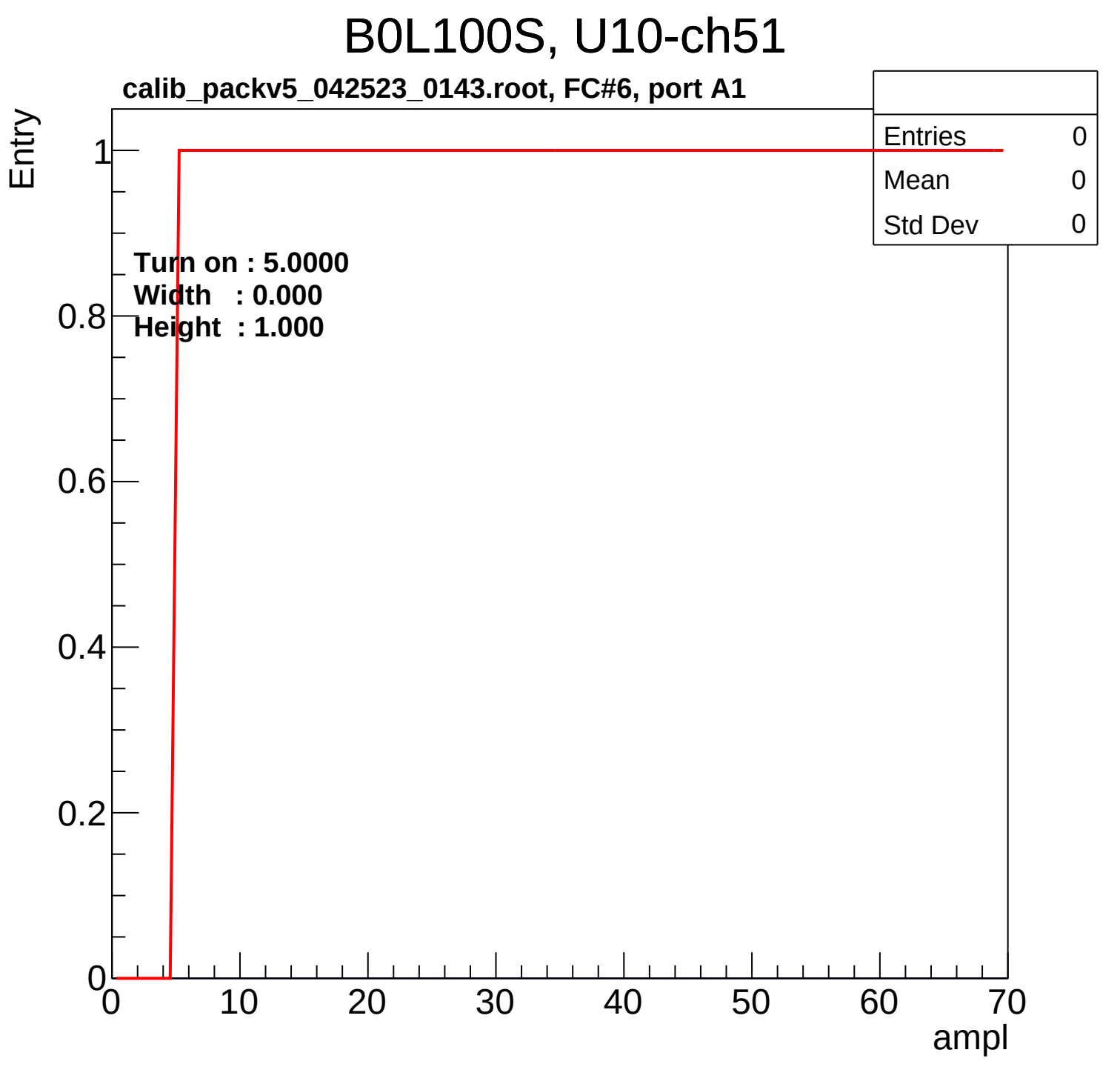

B0L100S, U10-ch46
calib_packv5_042523_0143.root, FC#6, port A1
Entries 15
Mean 45.8
Std Dev 0.9092
Turn on : 25.0017
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

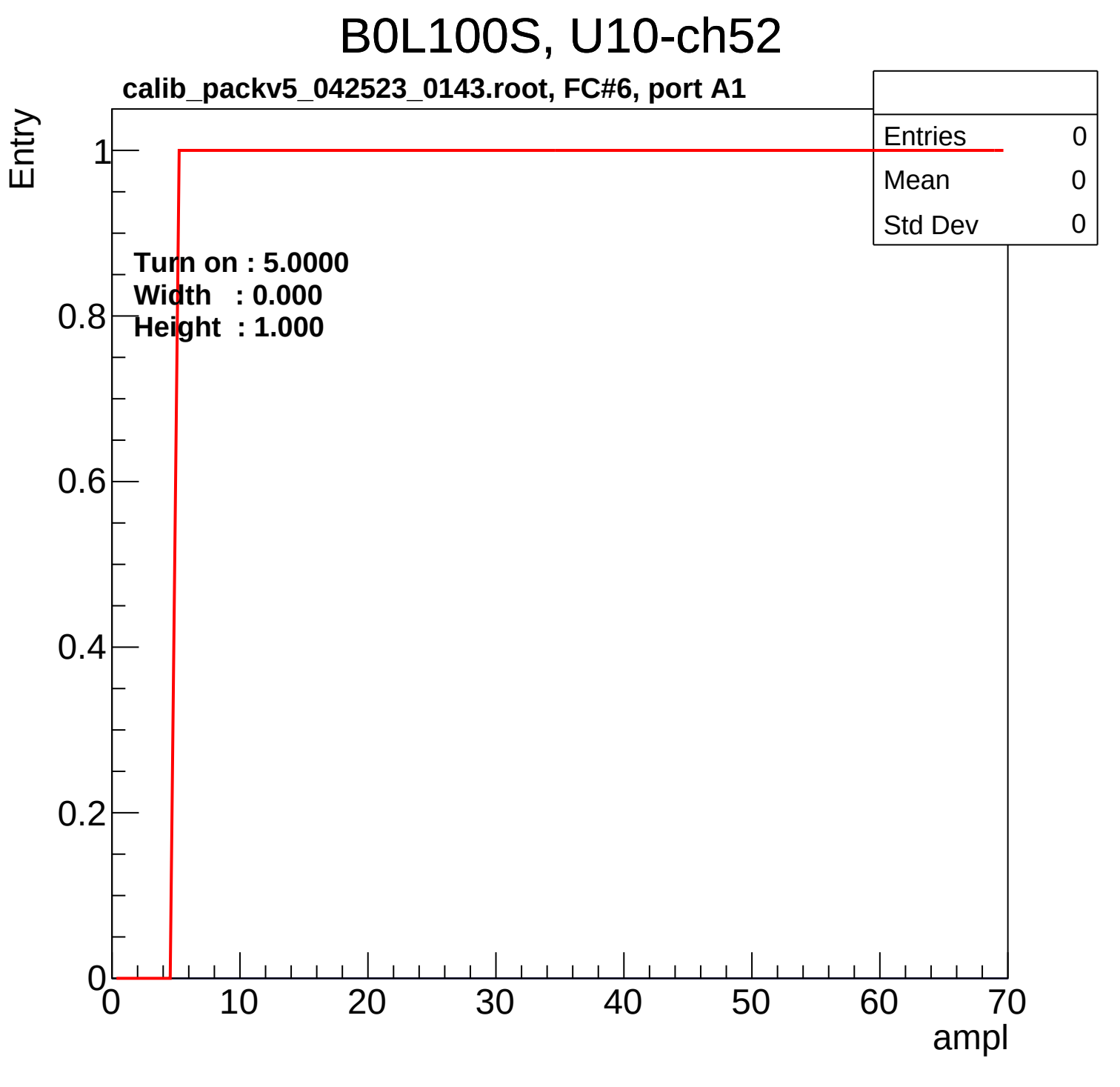

B0L100S, U10-ch47
calib_packv5_042523_0143.root, FC#6, port A1
Entries 58
Mean 46.29
Std Dev 3.723
Turn on : 40.5129
Width : 0.197
Height : 2.111
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

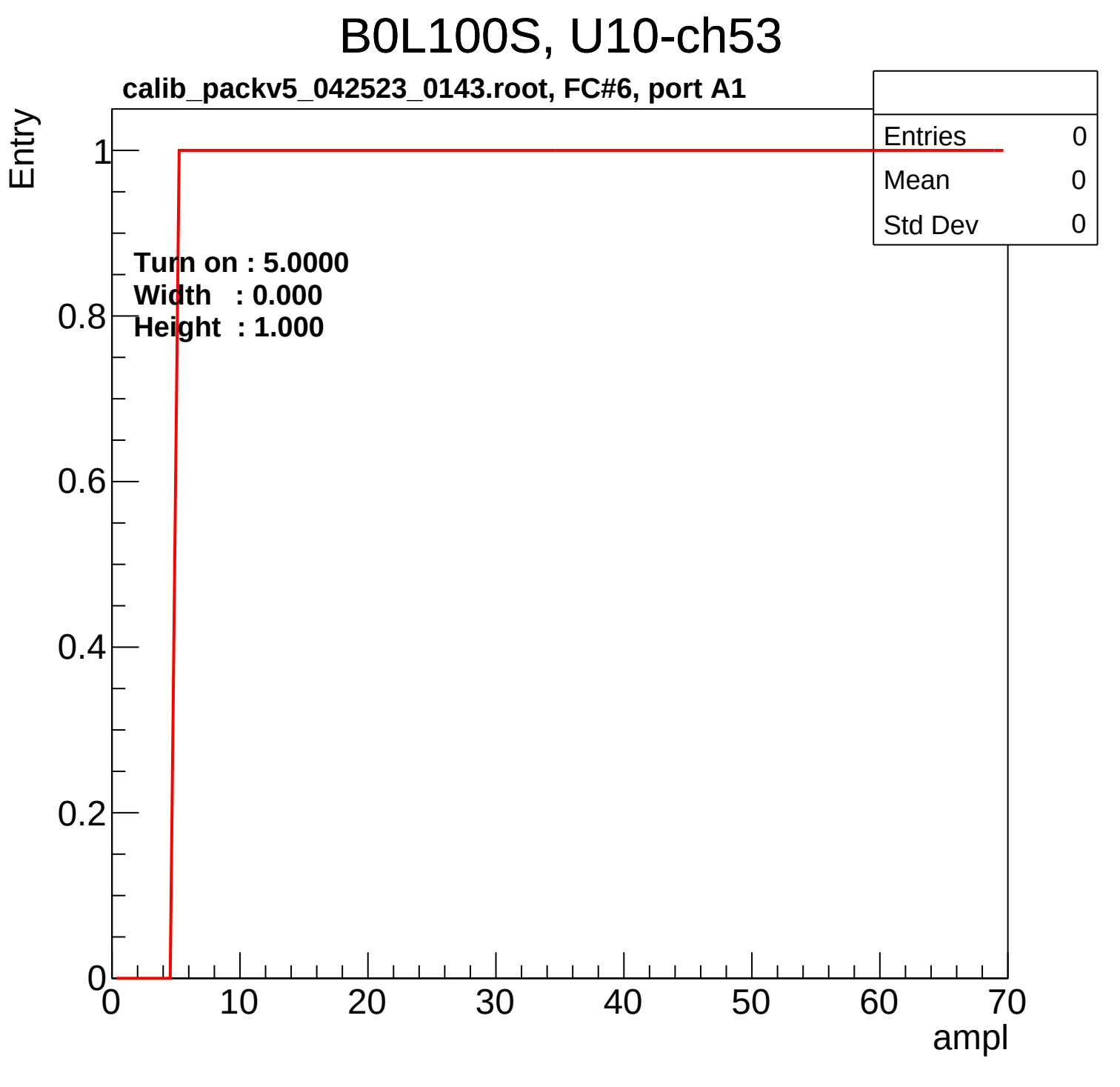

B0L100S, U10-ch48
calib_packv5_042523_0143.root, FC#6, port A1
Entries 3
Mean 42.67
Std Dev 0.9428
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

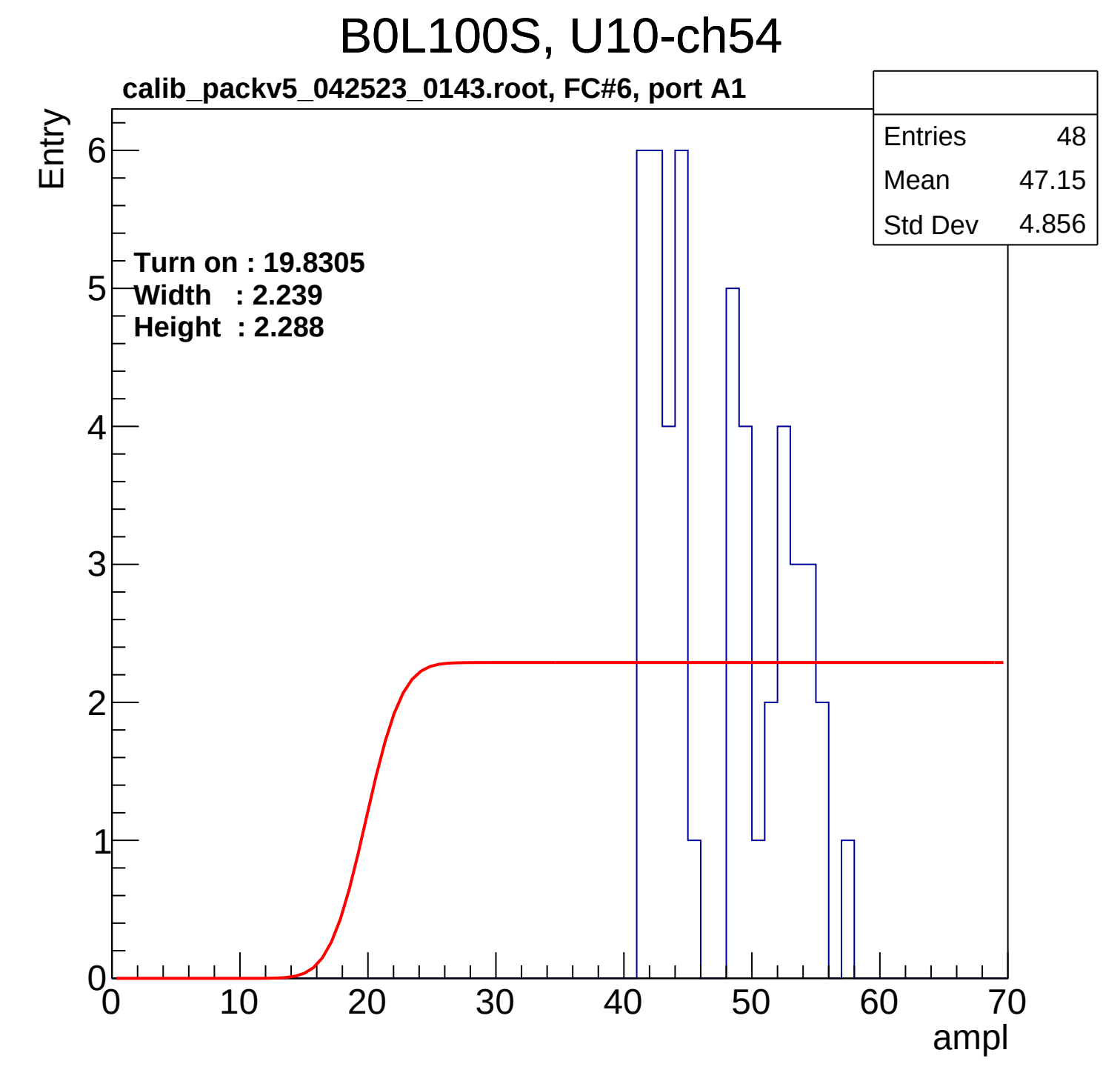

B0L100S, U10-ch49
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 52
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

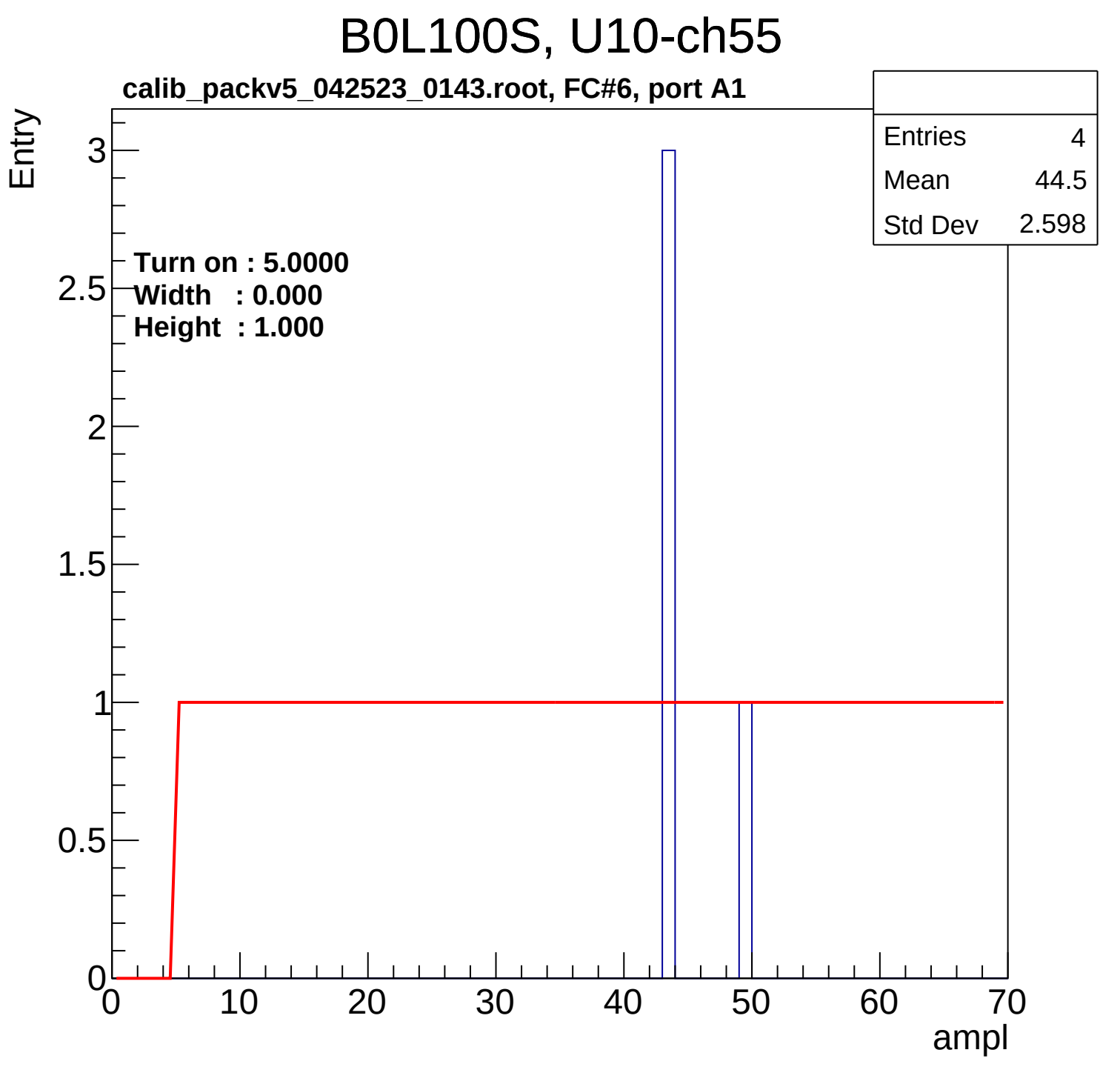

B0L100S, U10-ch50
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 45
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

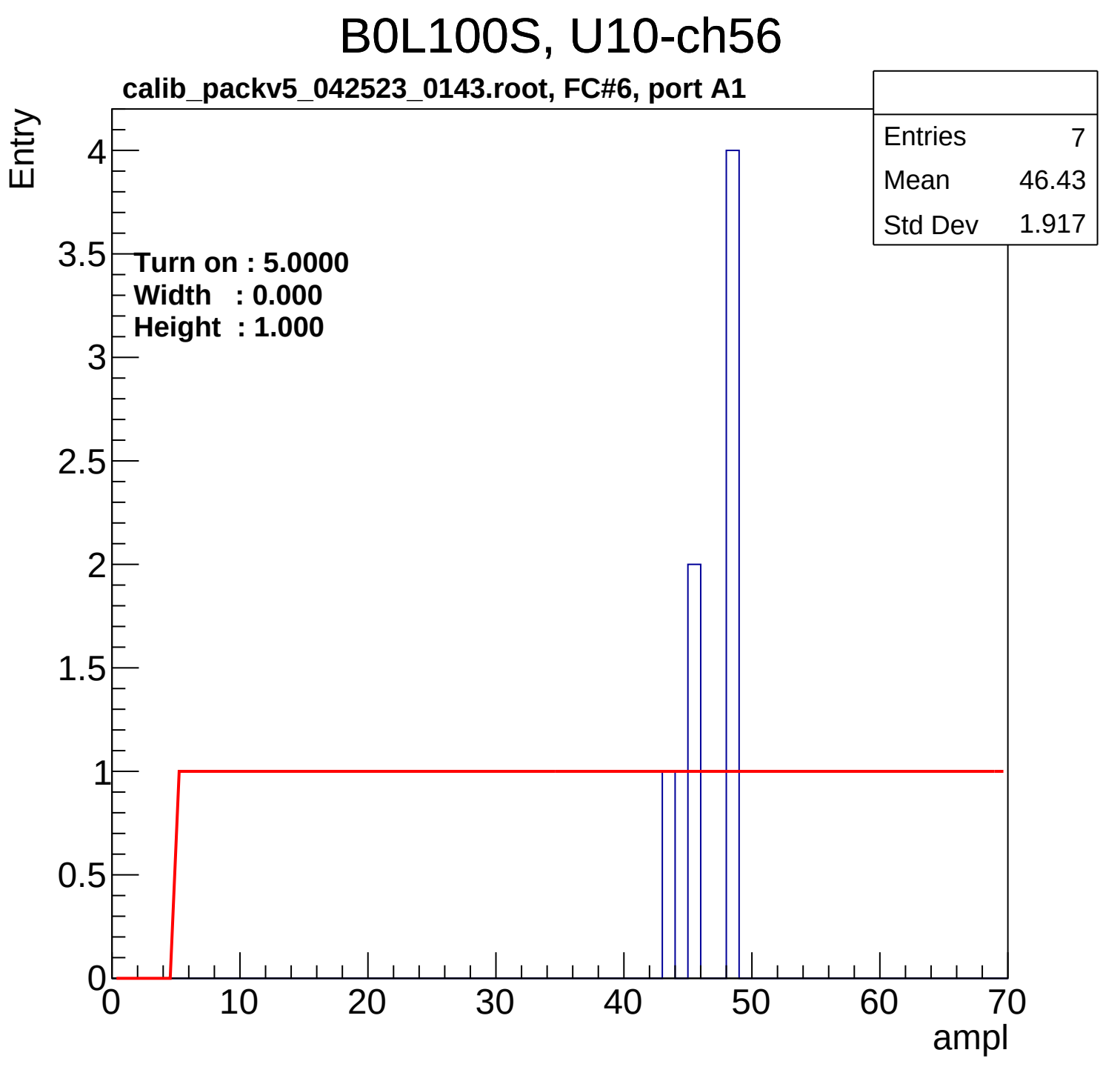

B0L100S, U10-ch51
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U10-ch52
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U10-ch53
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U10-ch54
calib_packv5_042523_0143.root, FC#6, port A1
Entries 48
Mean 47.15
Std Dev 4.856
Turn on : 19.8305
Width : 2.239
Height : 2.288
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B0L100S, U10-ch55
calib_packv5_042523_0143.root, FC#6, port A1
Entries 4
Mean 44.5
Std Dev 2.598
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B0L100S, U10-ch56
calib_packv5_042523_0143.root, FC#6, port A1
Entries 7
Mean 46.43
Std Dev 1.917
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
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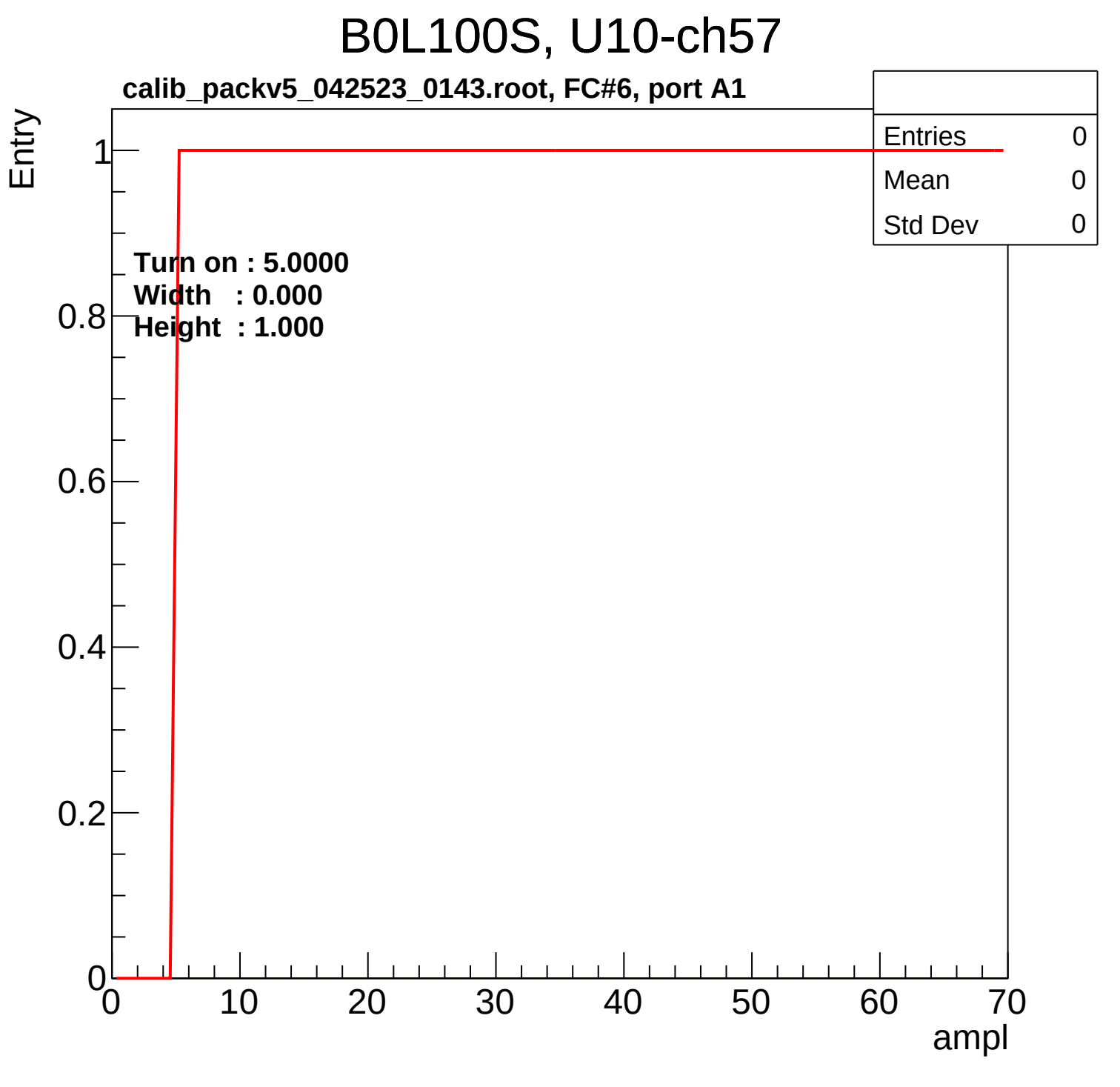
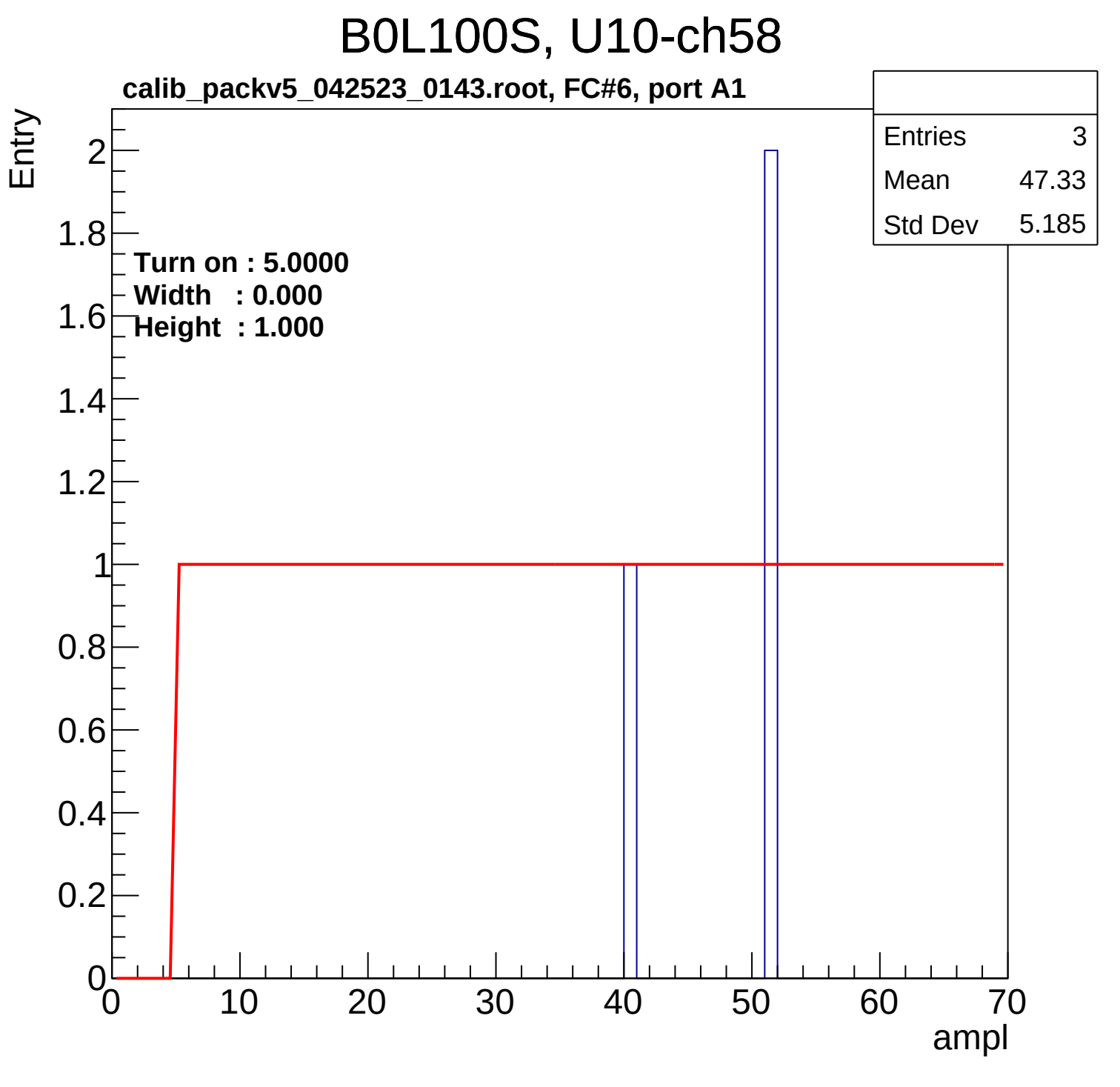
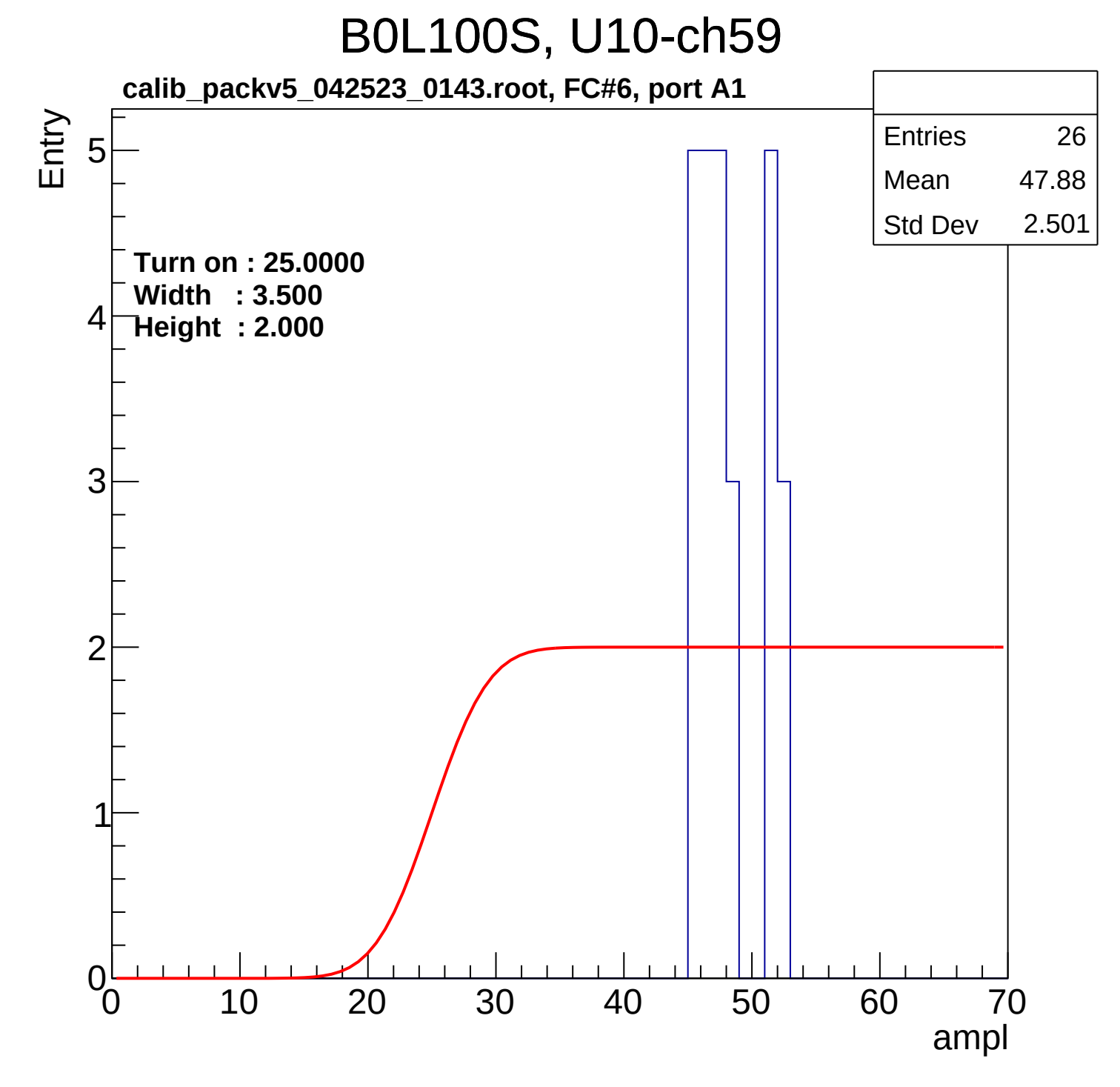
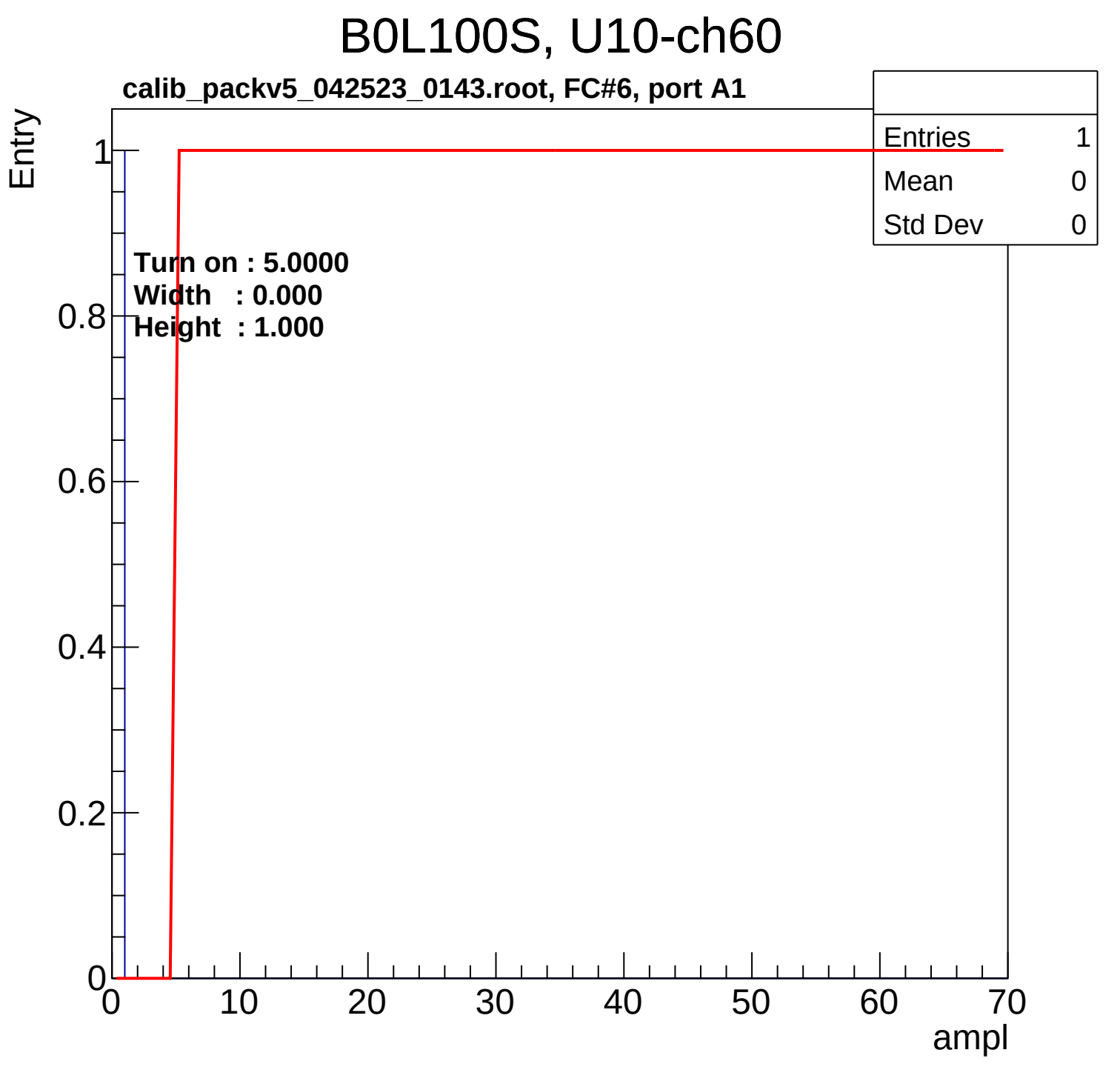
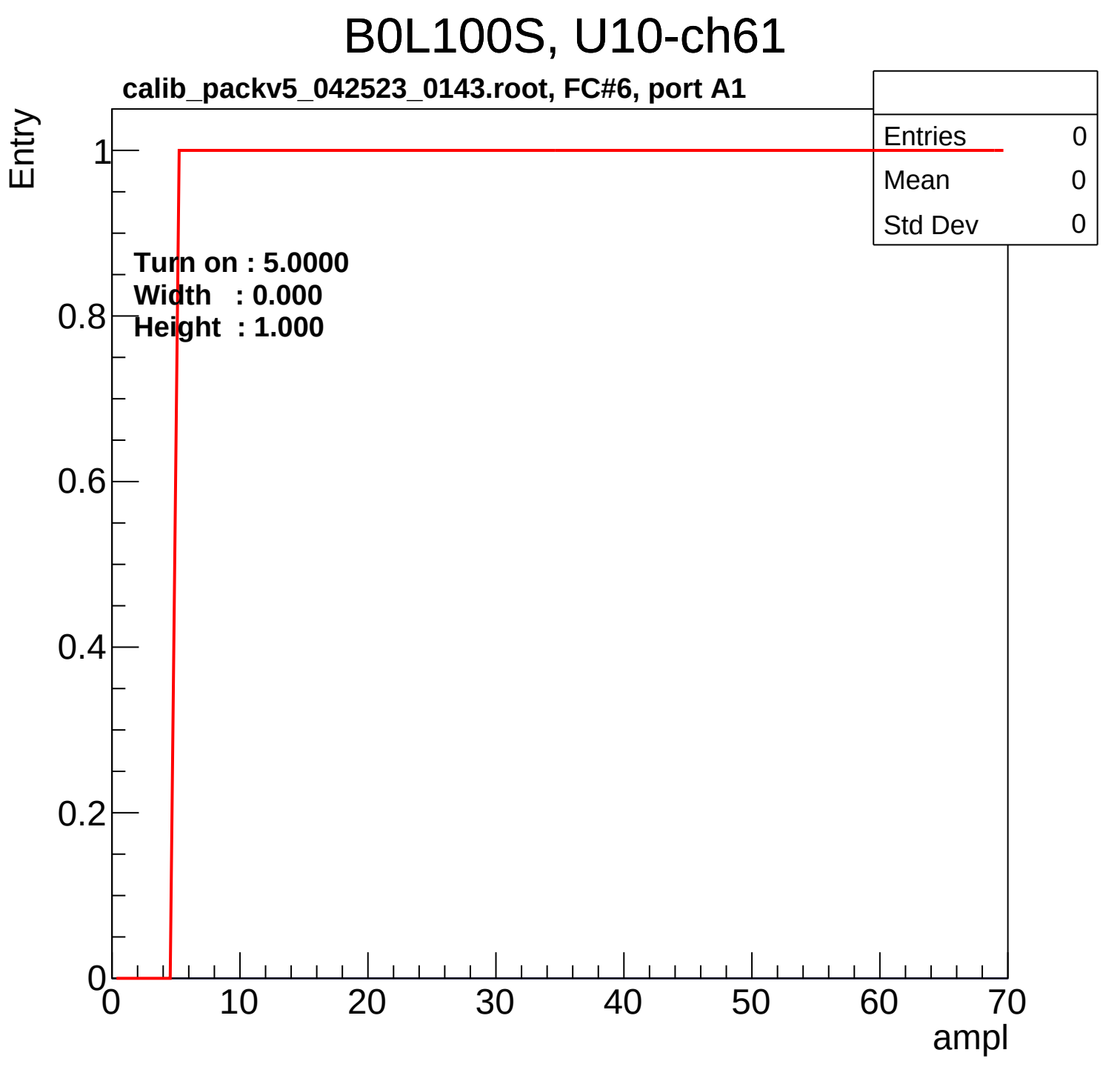
20
30
40
50
60
70

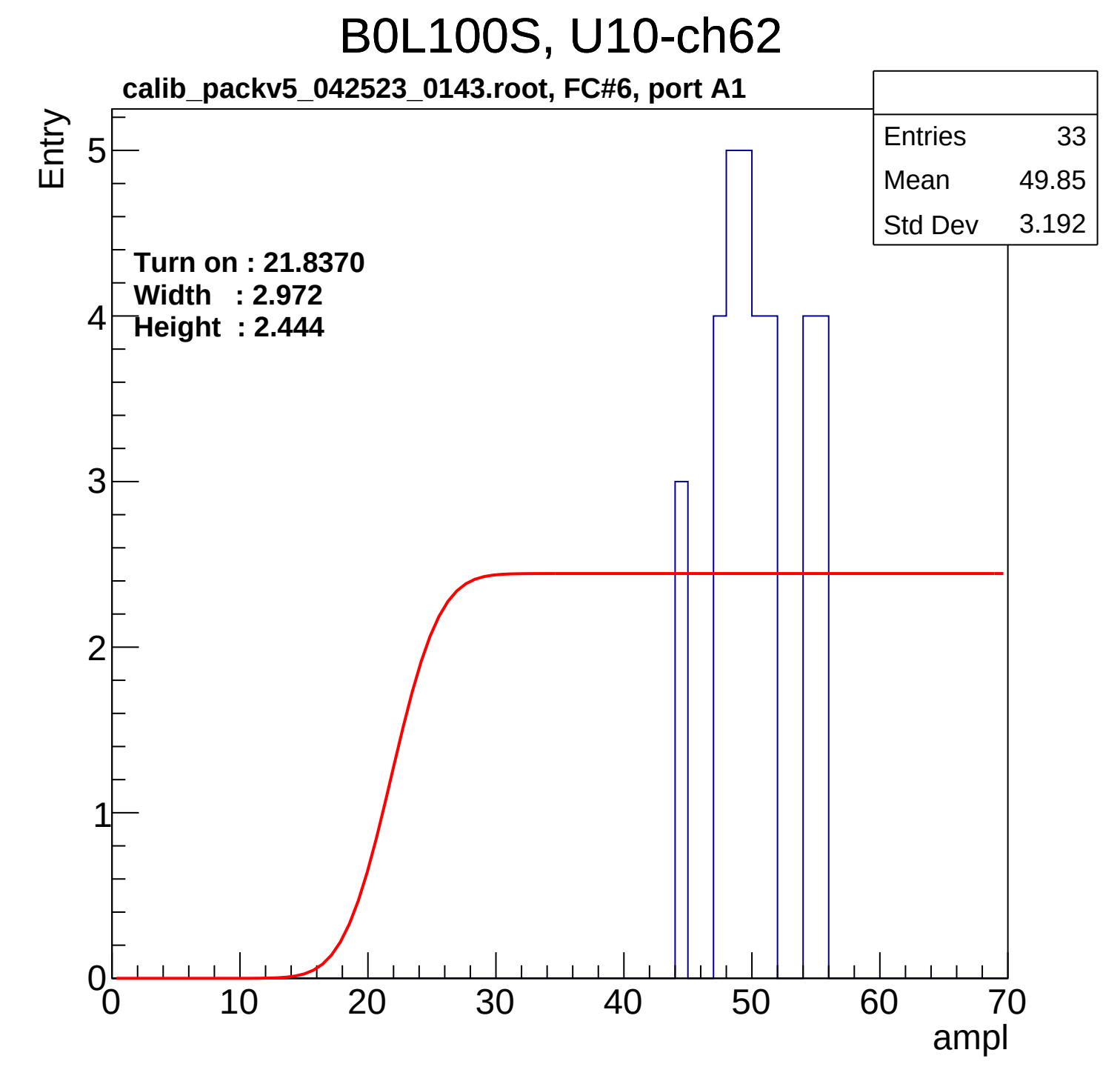

B0L100S, U10-ch57
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

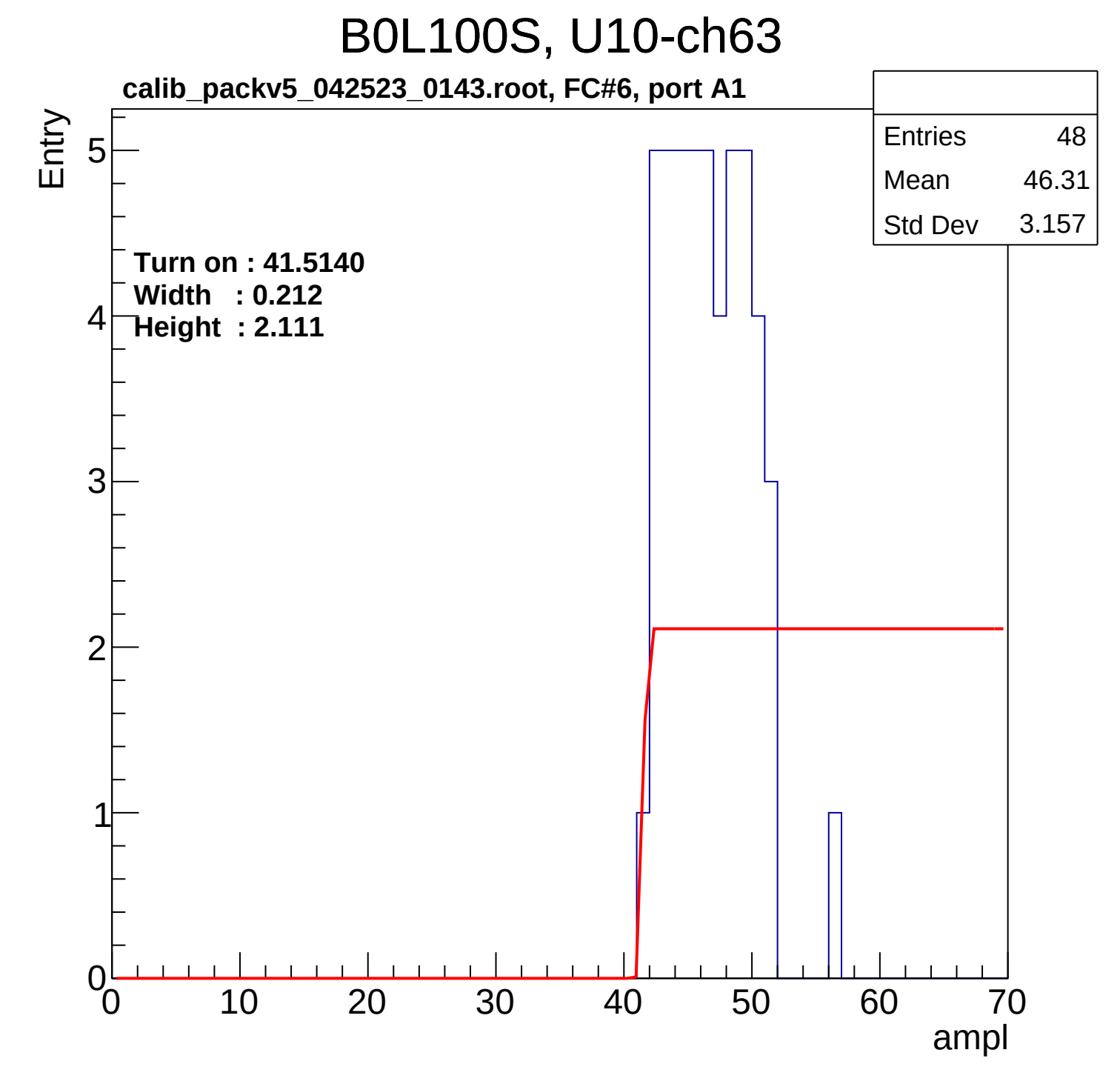

B0L100S, U10-ch58
calib_packv5_042523_0143.root, FC#6, port A1
Entries 3
Mean 47.33
Std Dev 5.185
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

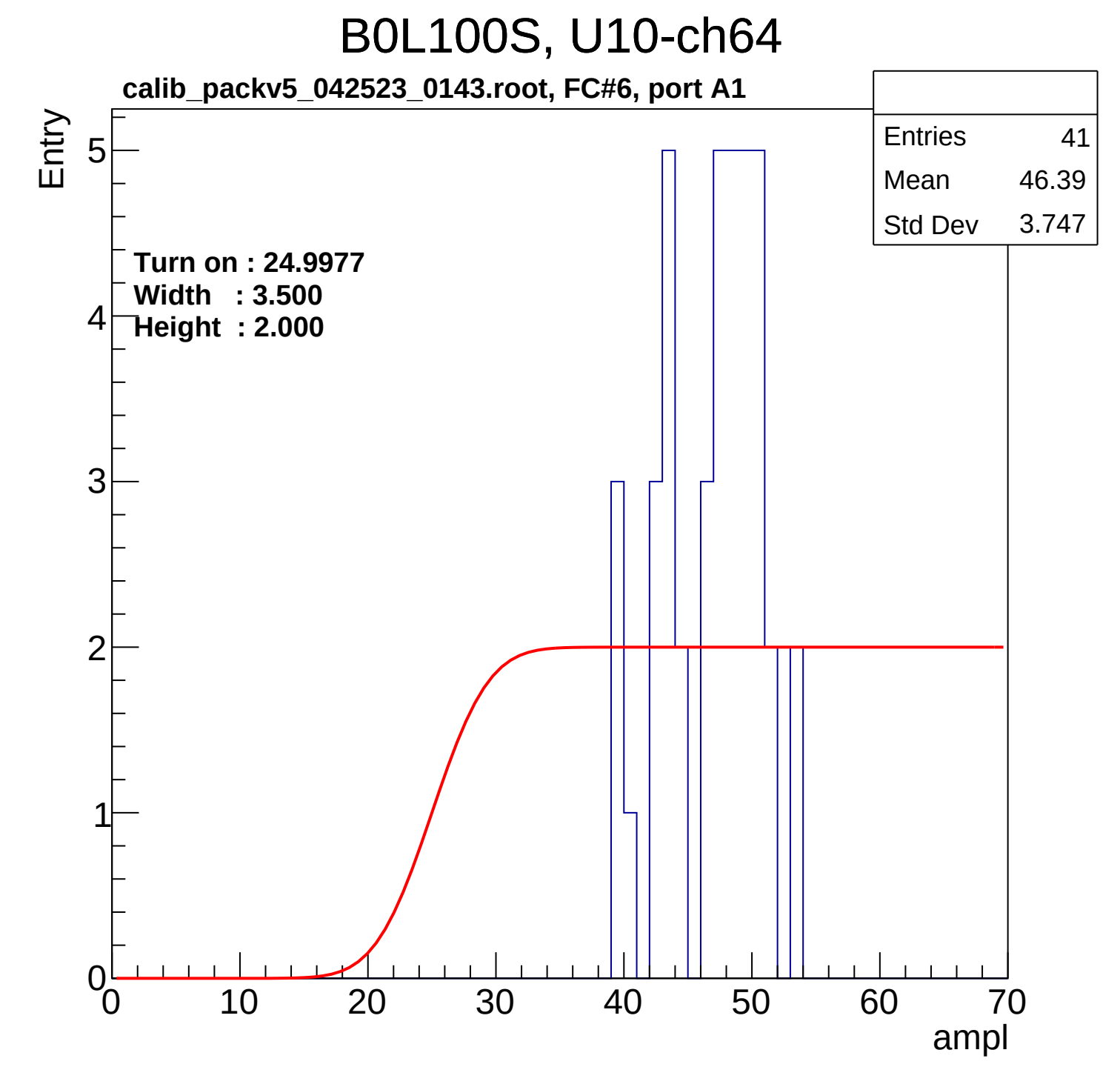

B0L100S, U10-ch59
calib_packv5_042523_0143.root, FC#6, port A1
Entries 26
Mean 47.88
Std Dev 2.501
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

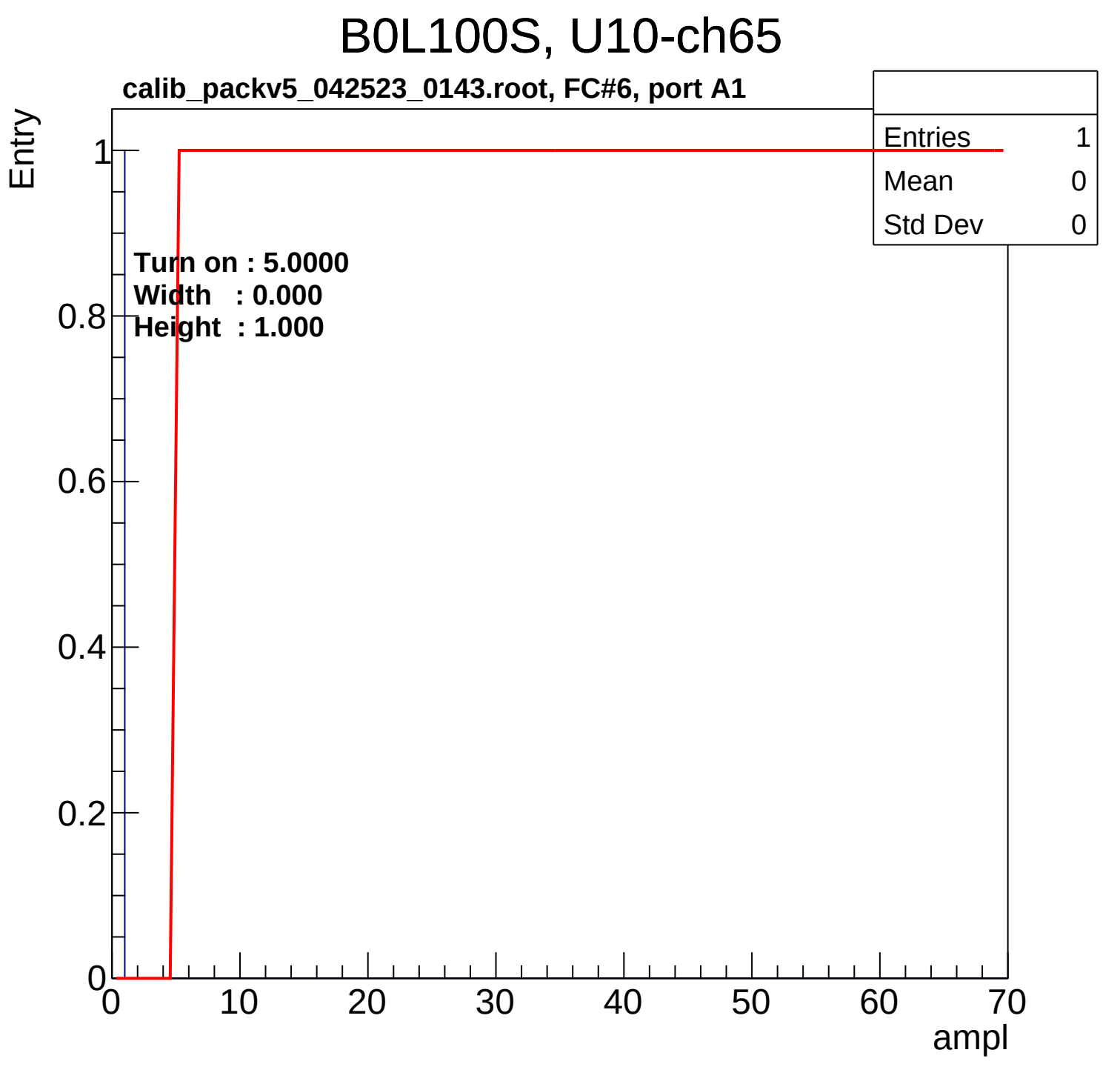

B0L100S, U10-ch60
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

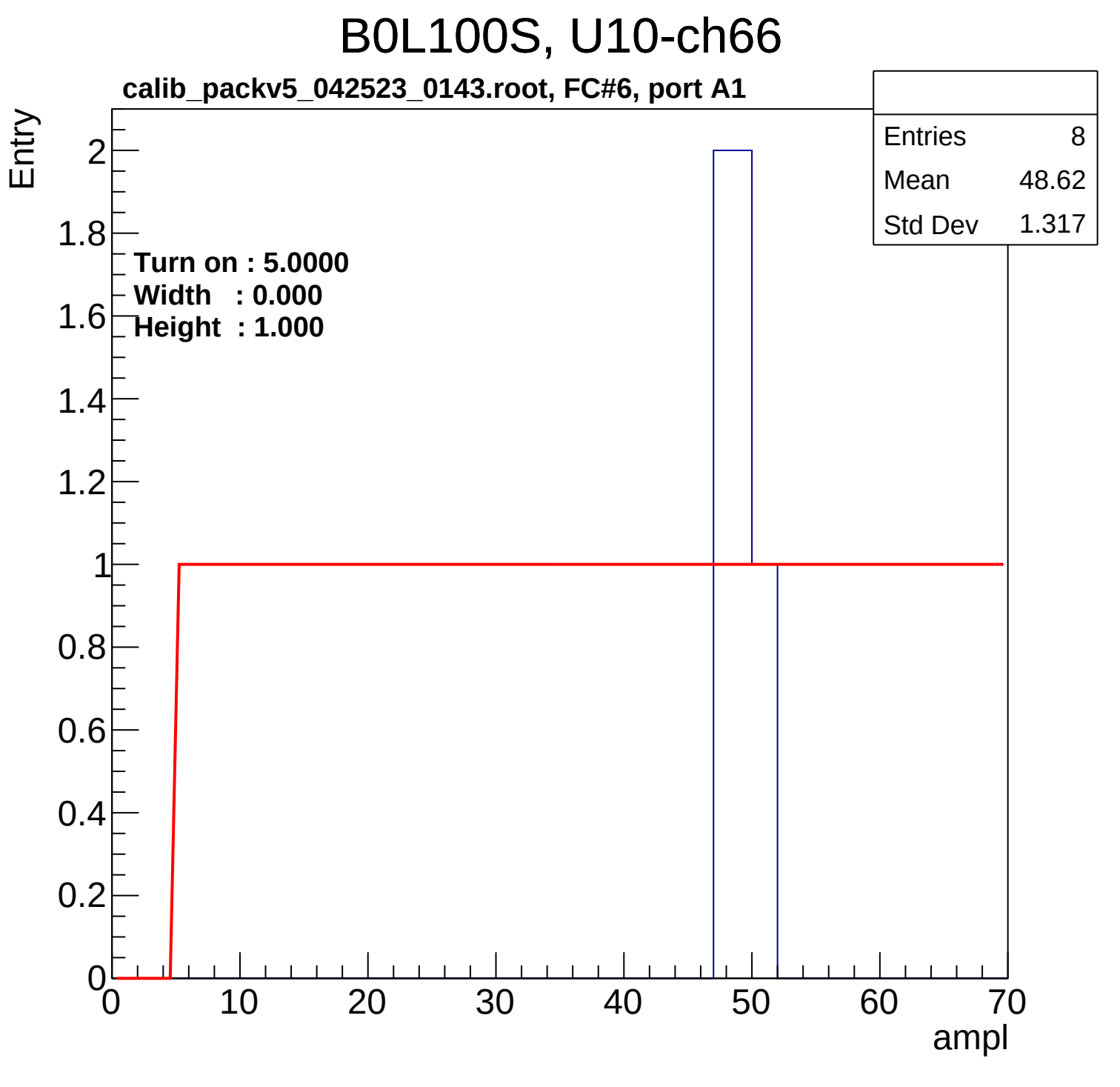

B0L100S, U10-ch61
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

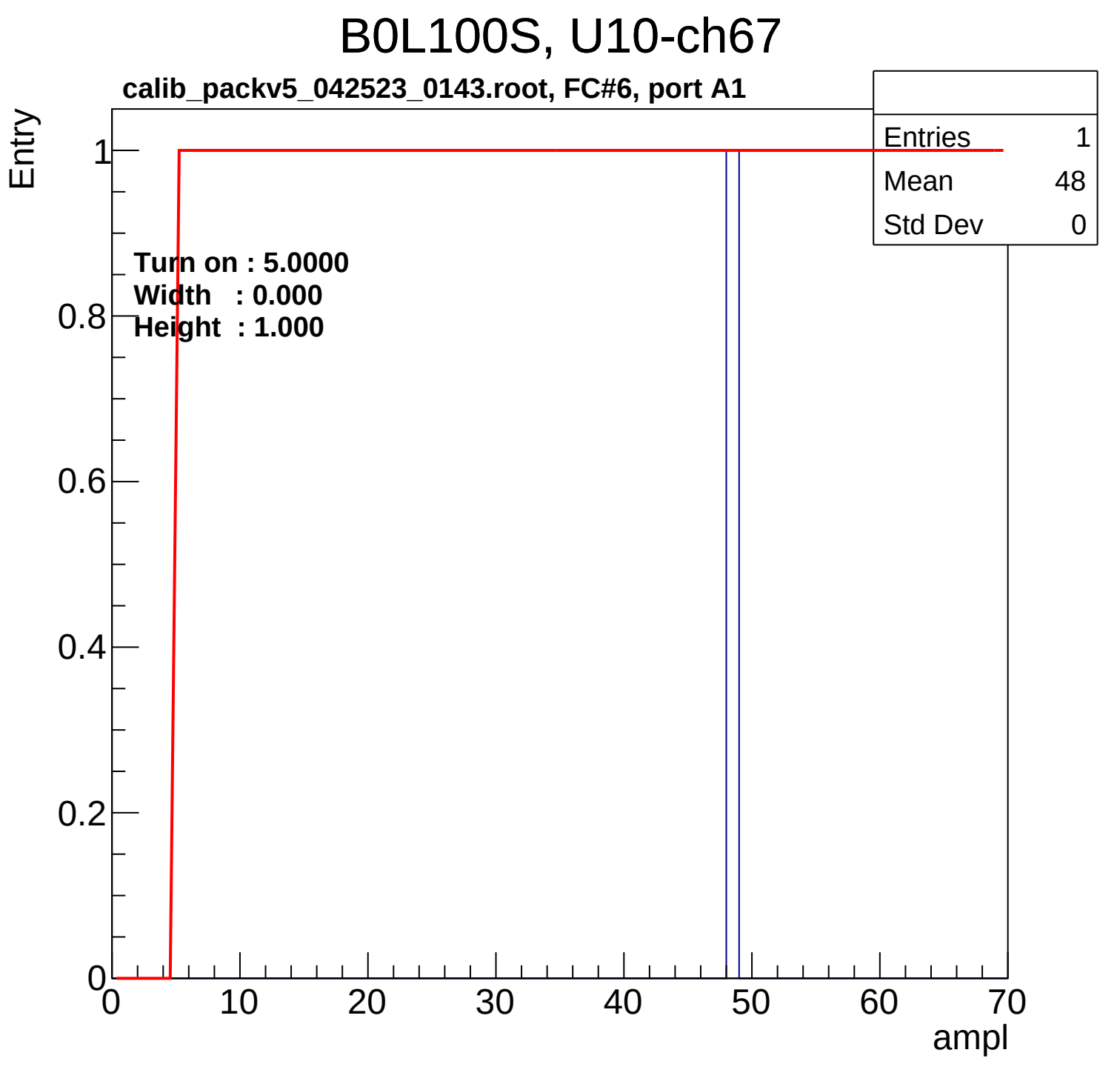

B0L100S, U10-ch62
calib_packv5_042523_0143.root, FC#6, port A1
Entries 33
Mean 49.85
Std Dev 3.192
Turn on : 21.8370
Width : 2.972
Height : 2.444
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

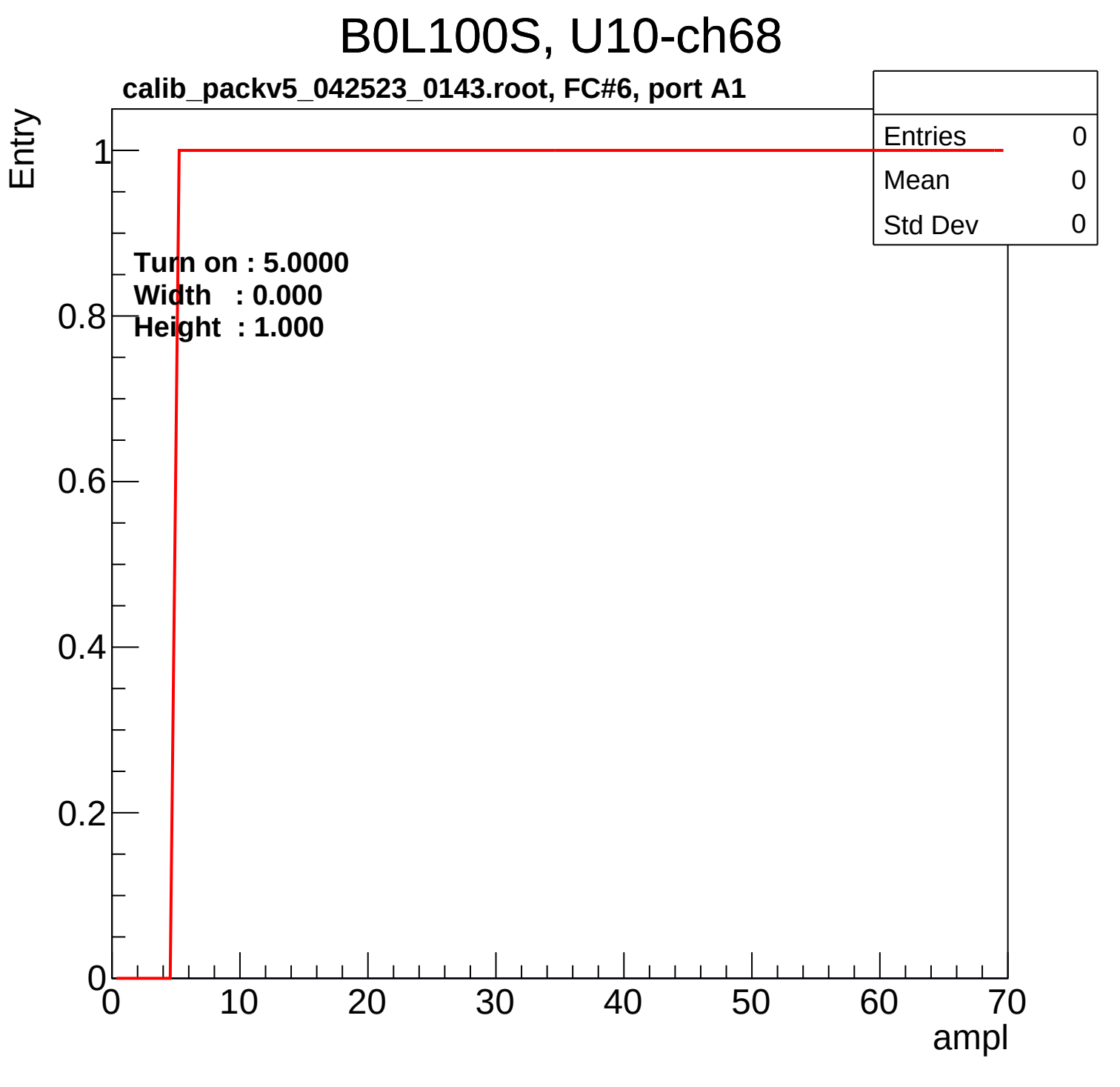

B0L100S, U10-ch63
calib_packv5_042523_0143.root, FC#6, port A1
Entries 48
Mean 46.31
Std Dev 3.157
Turn on : 41.5140
Width : 0.212
Height : 2.111
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

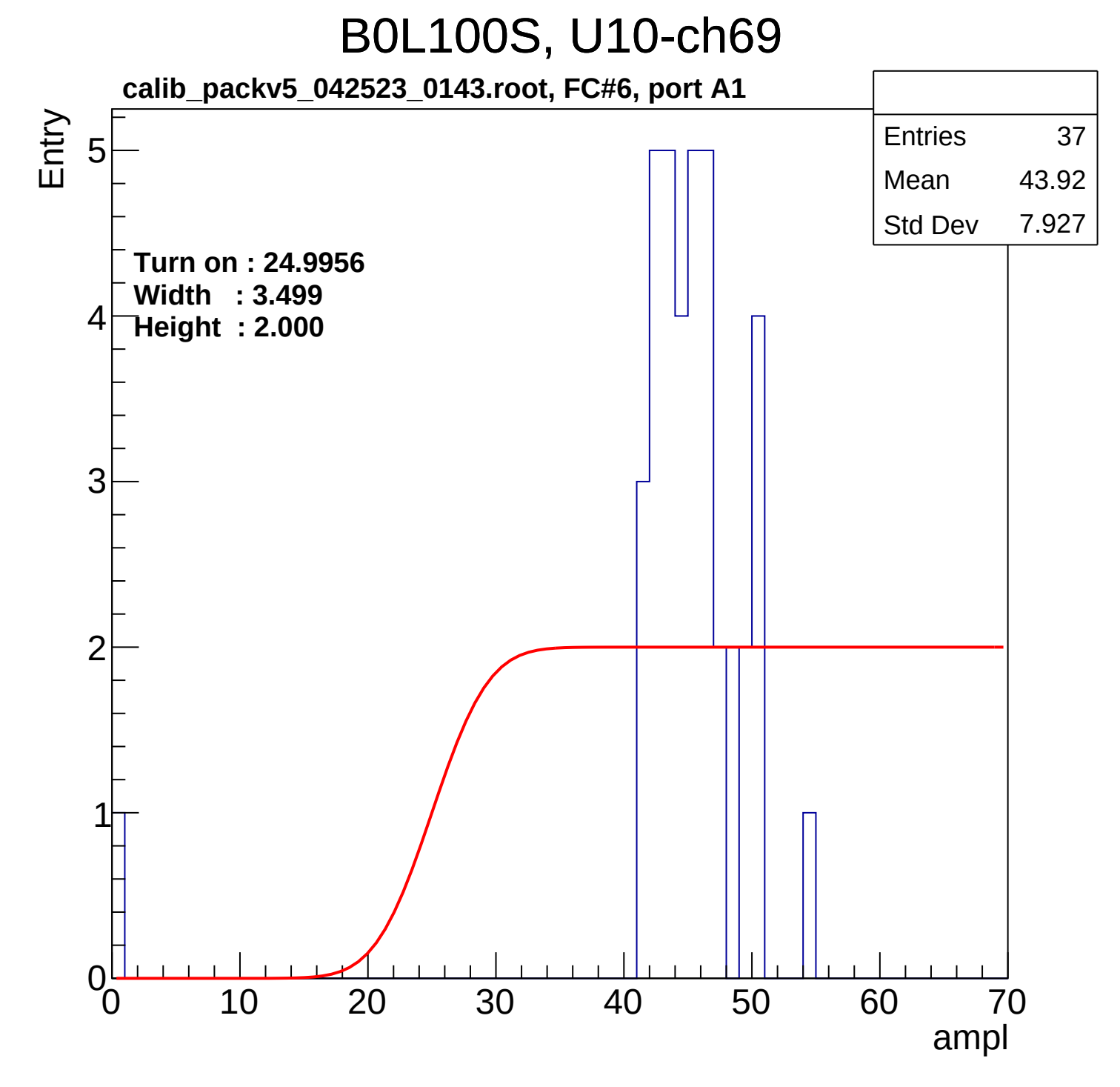

B0L100S, U10-ch64
calib_packv5_042523_0143.root, FC#6, port A1
Entries 41
Mean 46.39
Std Dev 3.747
Turn on : 24.9977
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

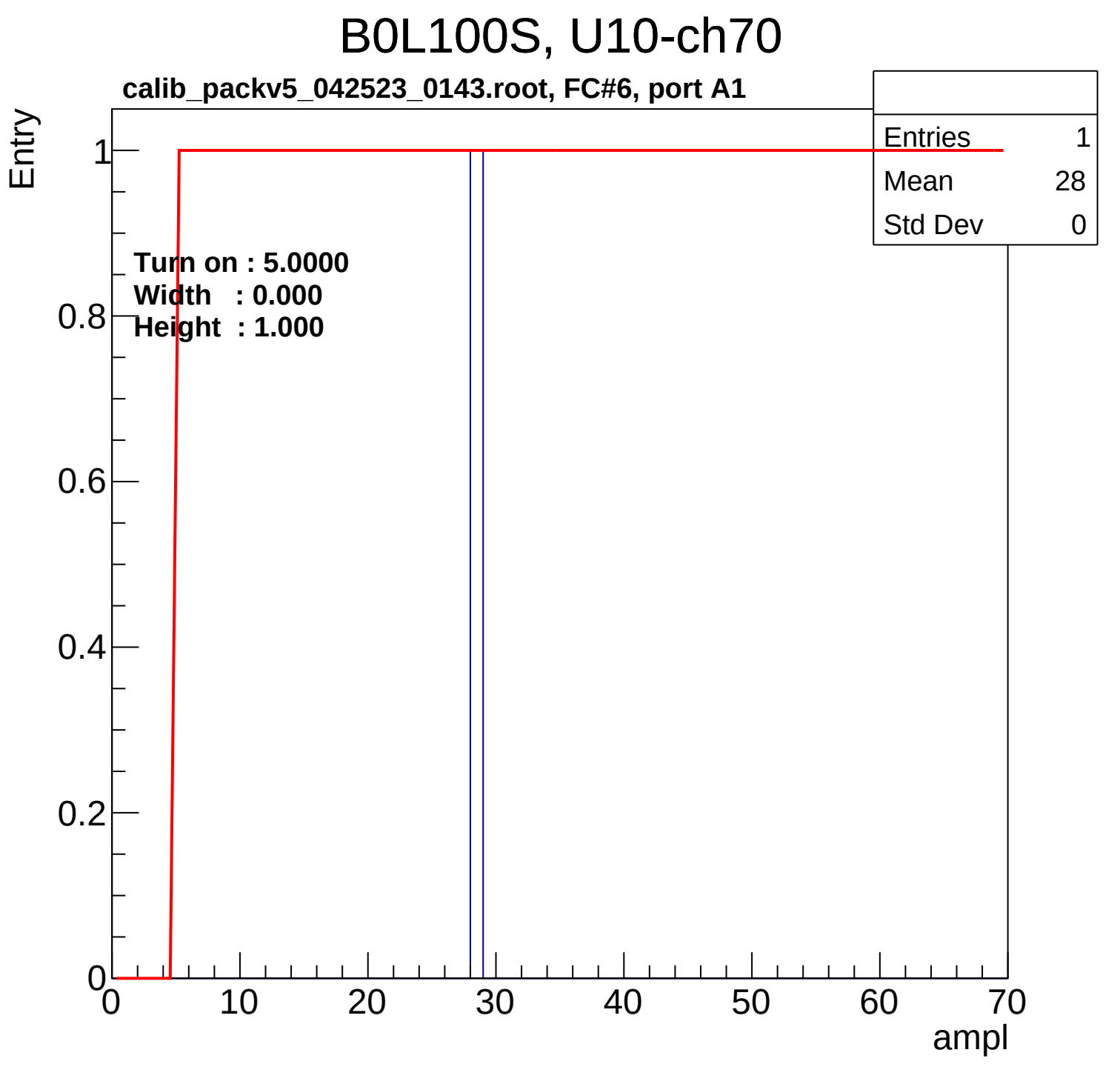

B0L100S, U10-ch65
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

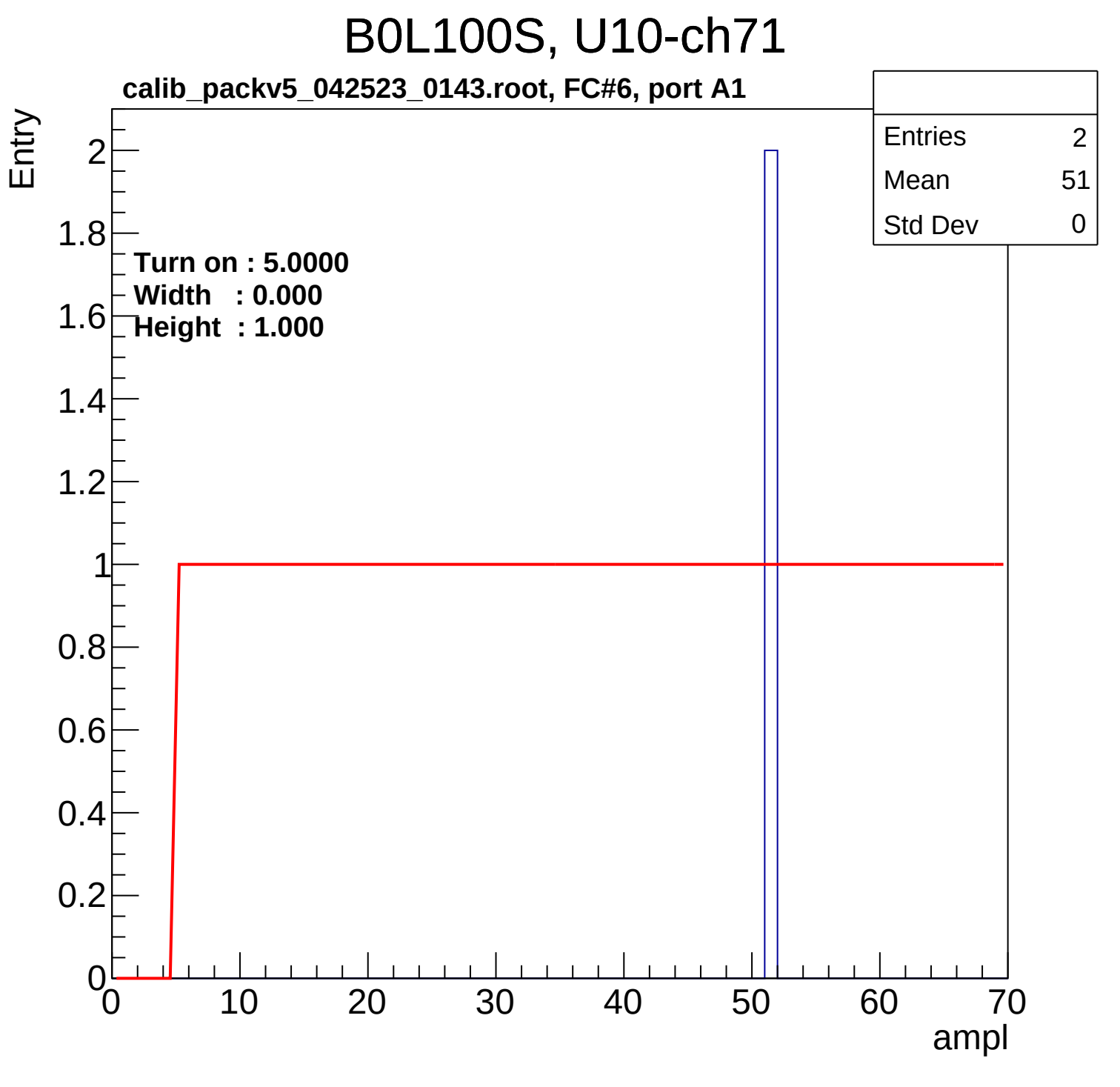

B0L100S, U10-ch66
calib_packv5_042523_0143.root, FC#6, port A1
Entries 8
Mean 48.62
Std Dev 1.317
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

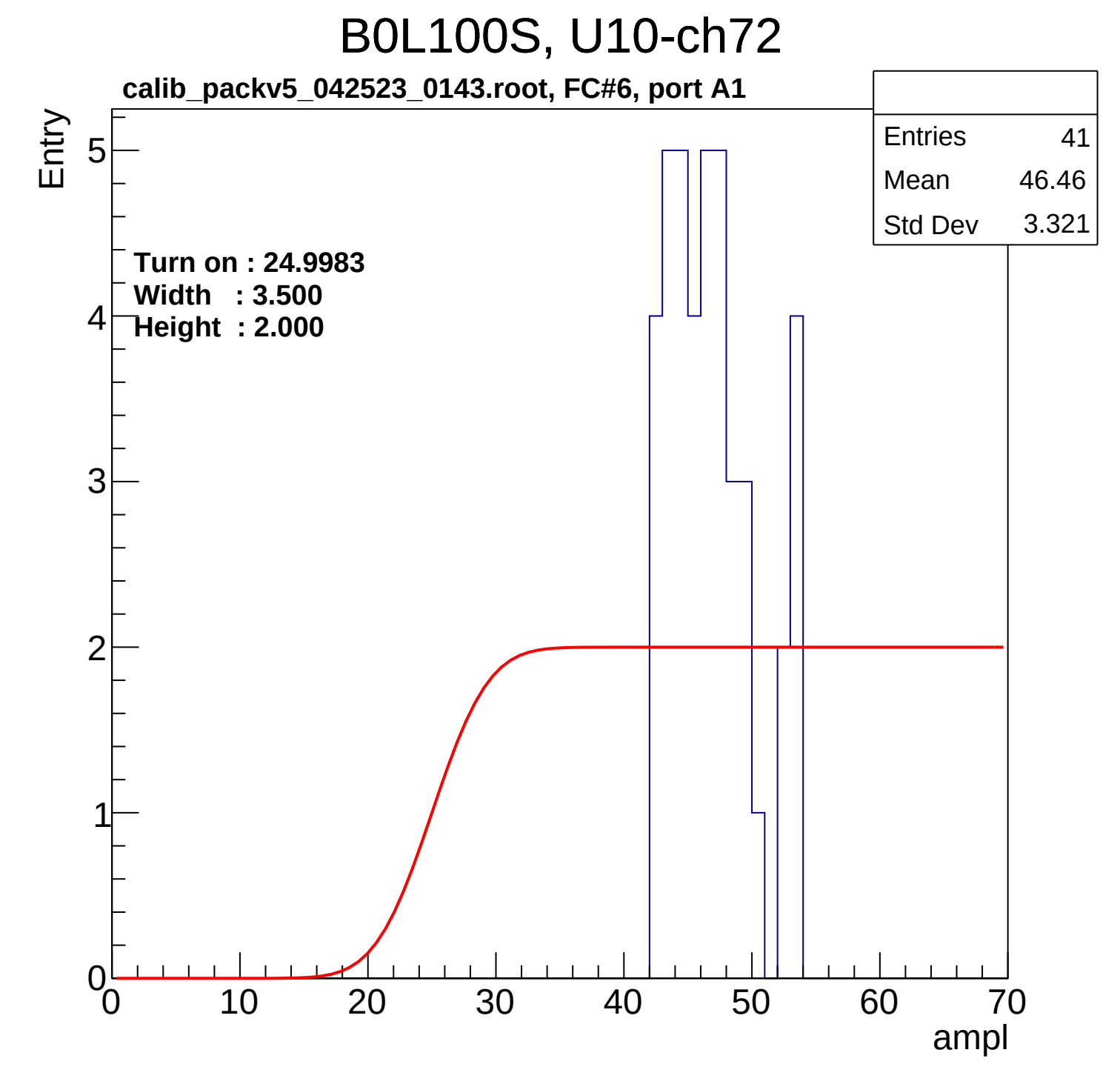

B0L100S, U10-ch67
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 48
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

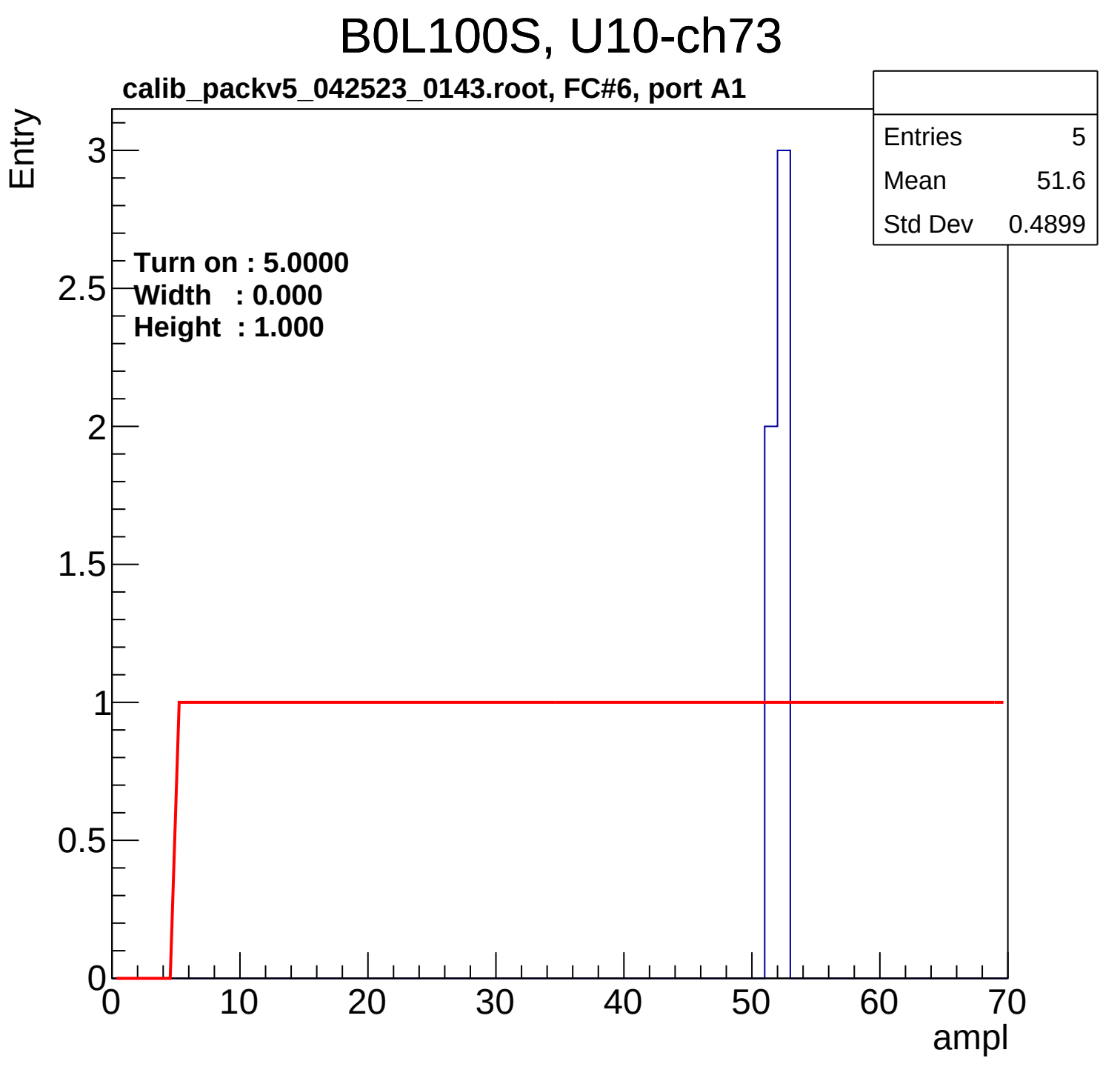

B0L100S, U10-ch68
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

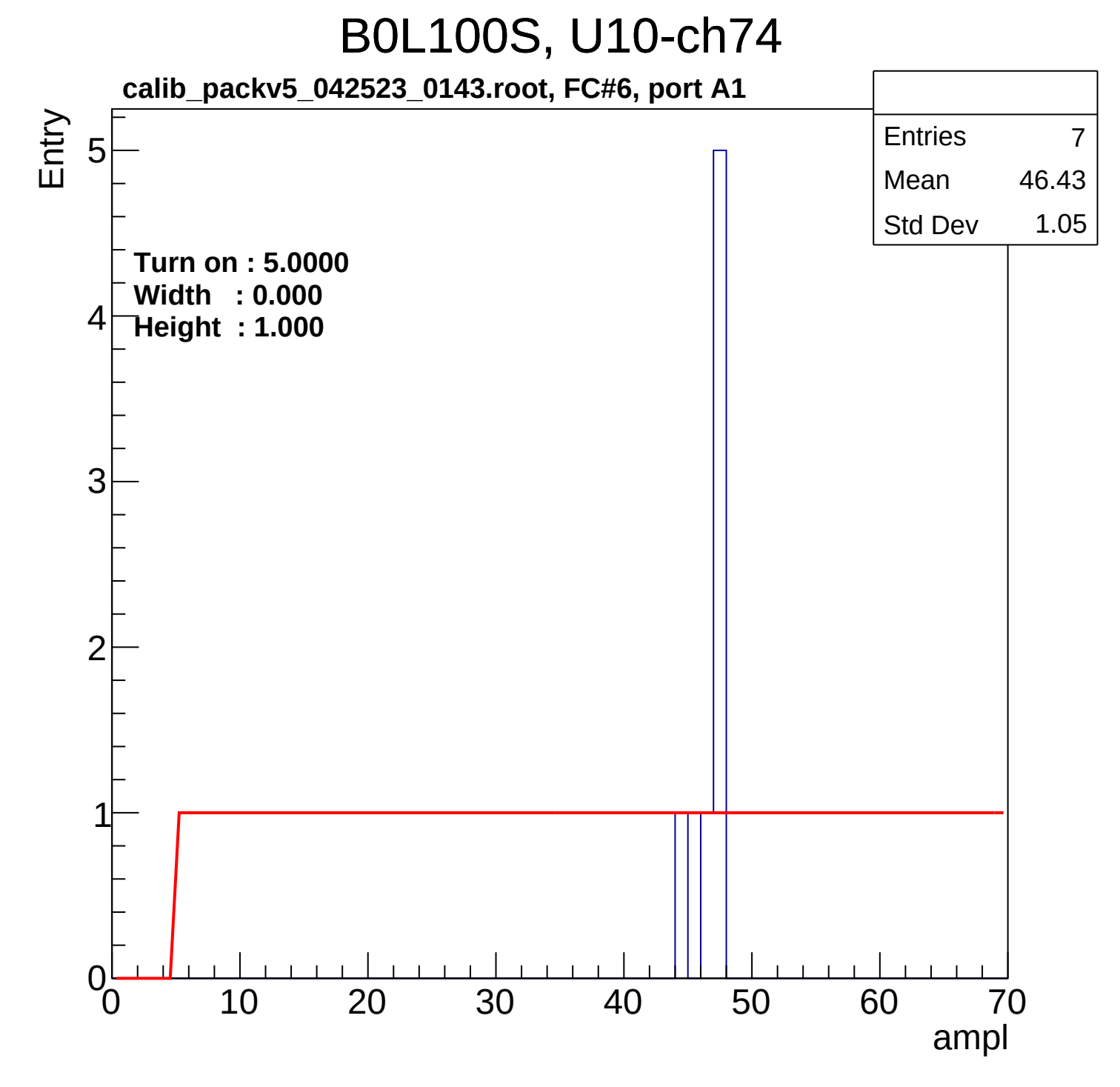

B0L100S, U10-ch69
calib_packv5_042523_0143.root, FC#6, port A1
Entries 37
Mean 43.92
Std Dev 7.927
Turn on : 24.9956
Width : 3.499
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

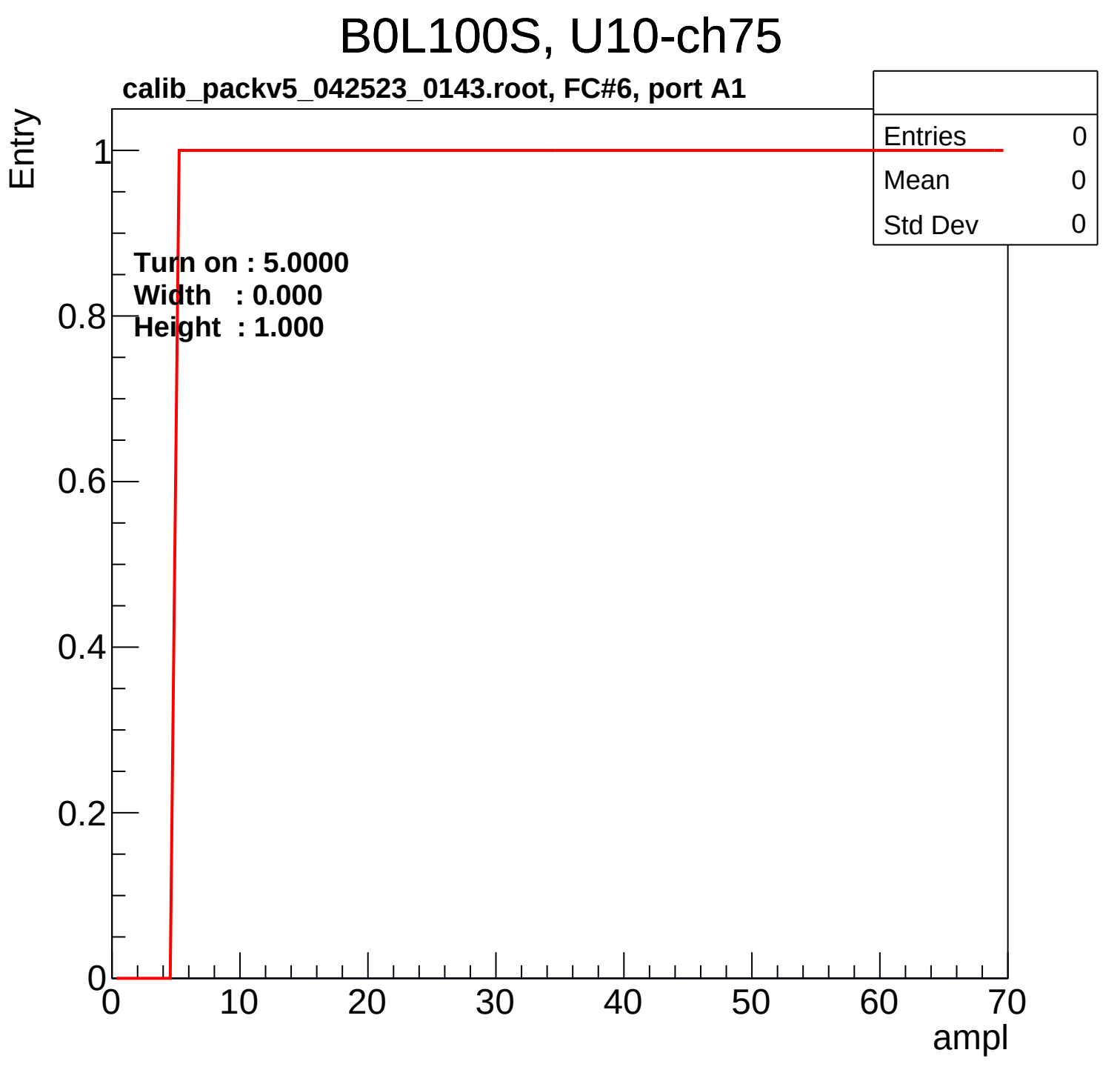

B0L100S, U10-ch70
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 28
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

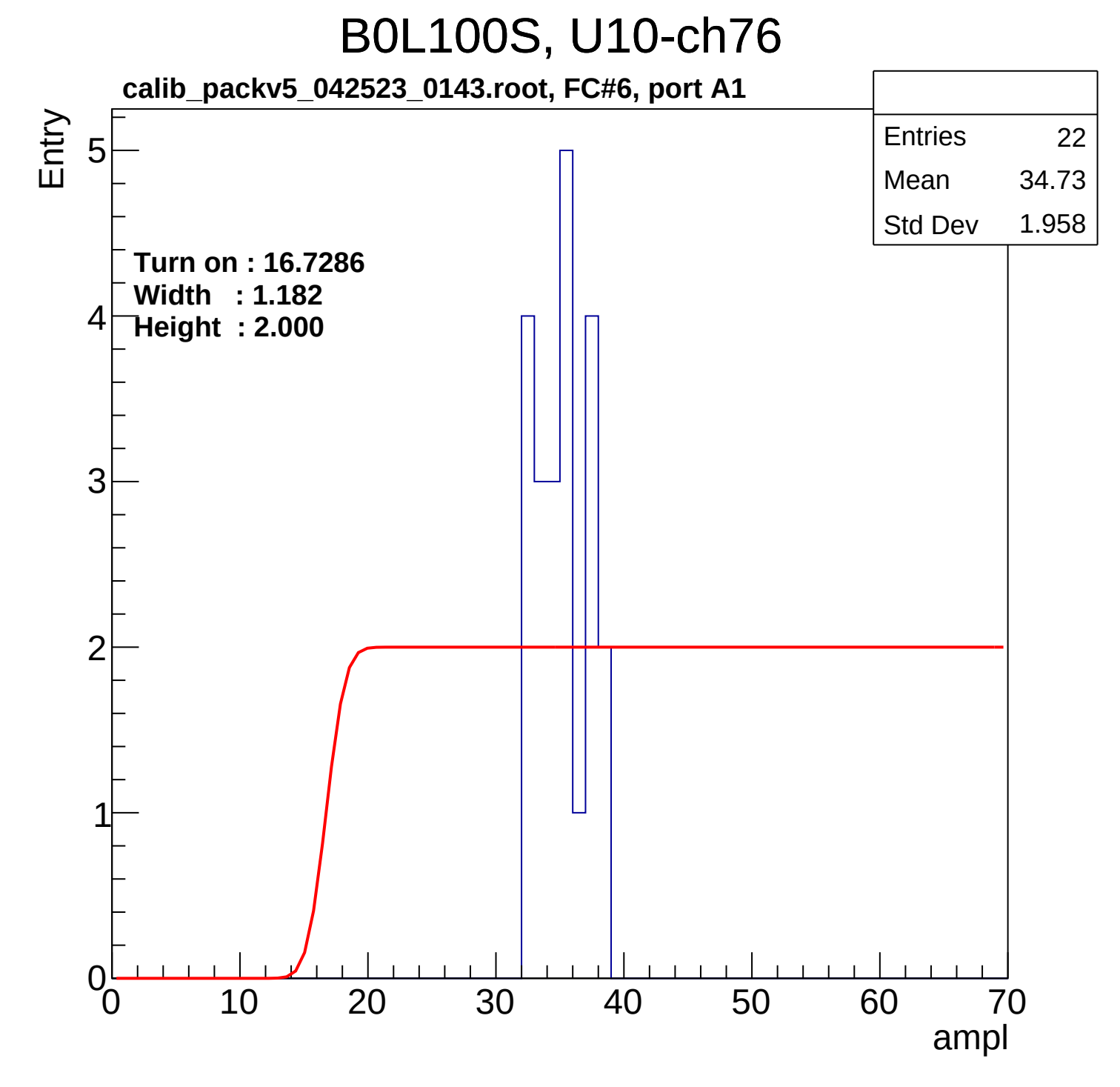

B0L100S, U10-ch71
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 51
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

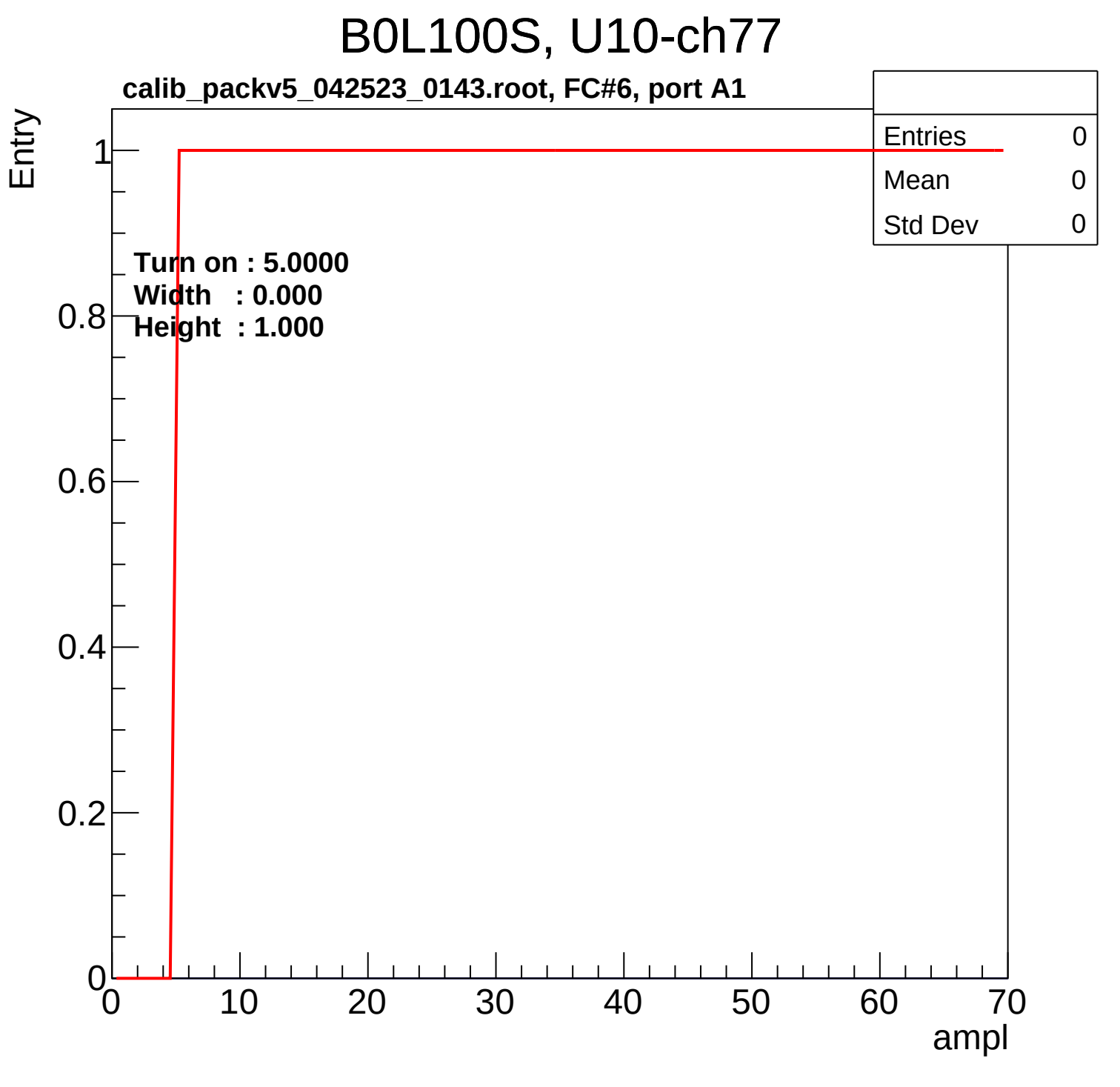

B0L100S, U10-ch72
calib_packv5_042523_0143.root, FC#6, port A1
Entries 41
Mean 46.46
Std Dev 3.321
Turn on : 24.9983
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

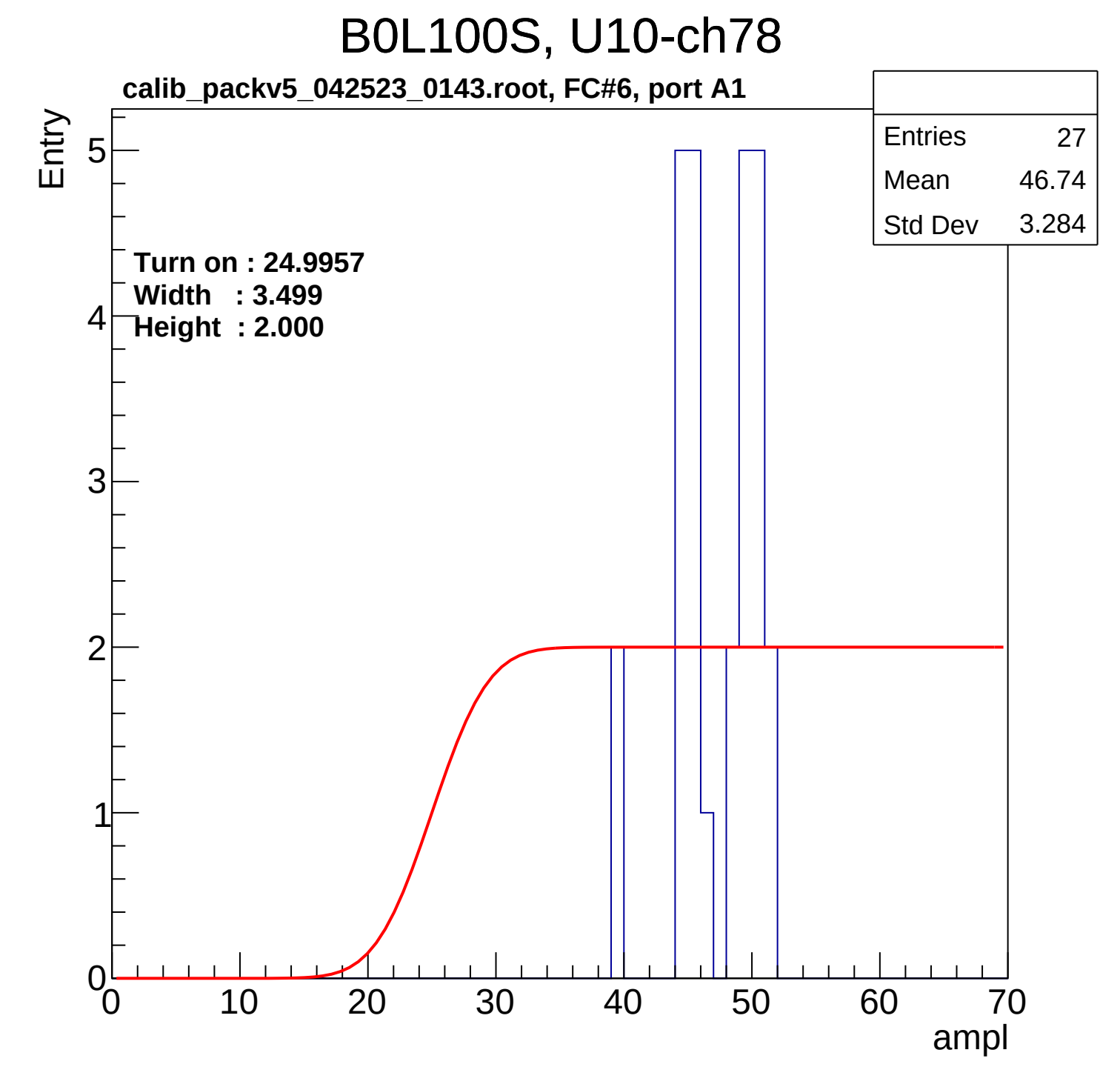

B0L100S, U10-ch73
calib_packv5_042523_0143.root, FC#6, port A1
Entries 5
Mean 51.6
Std Dev 0.4899
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

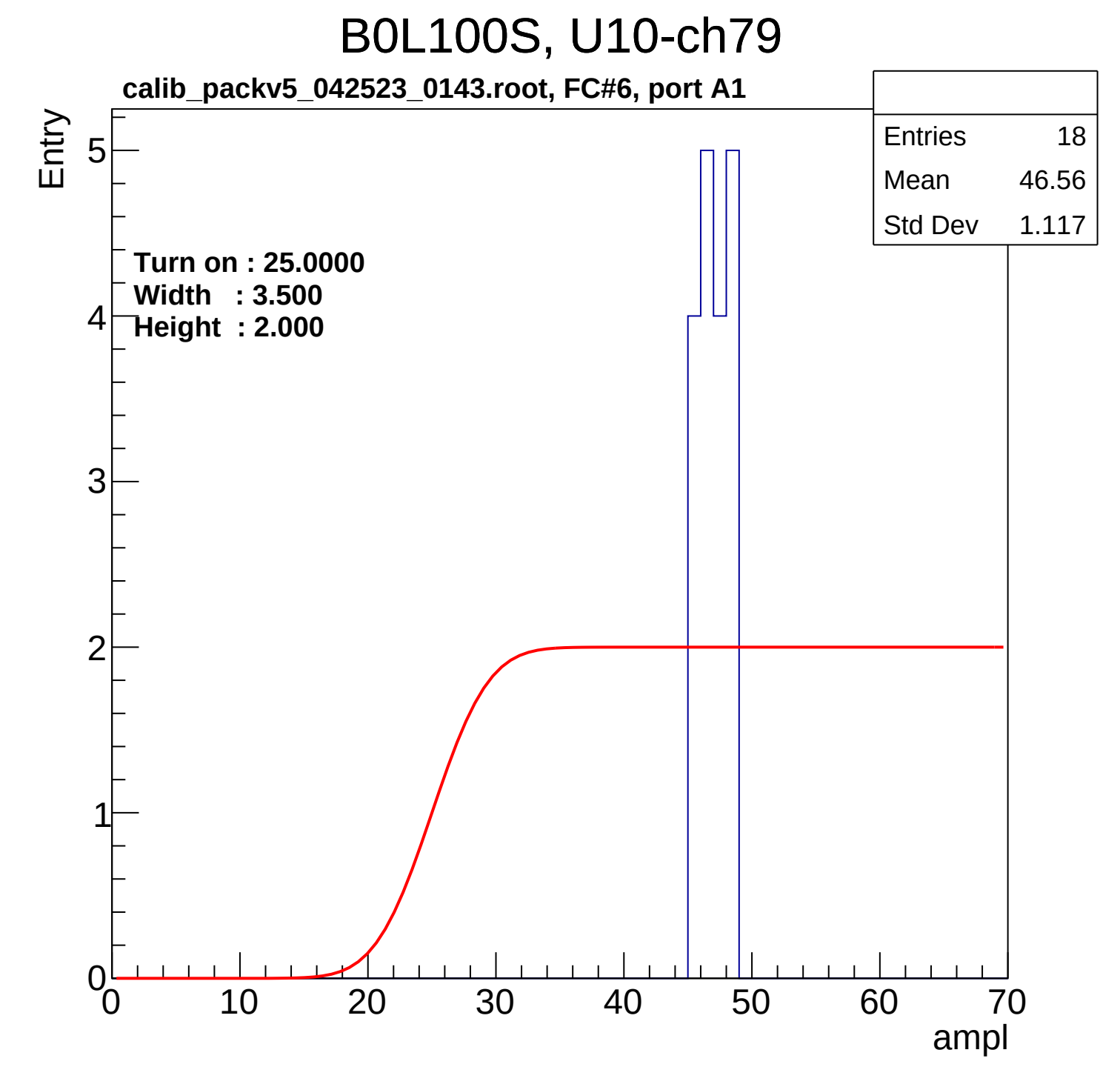

B0L100S, U10-ch74
calib_packv5_042523_0143.root, FC#6, port A1
Entries 7
Mean 46.43
Std Dev 1.05
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

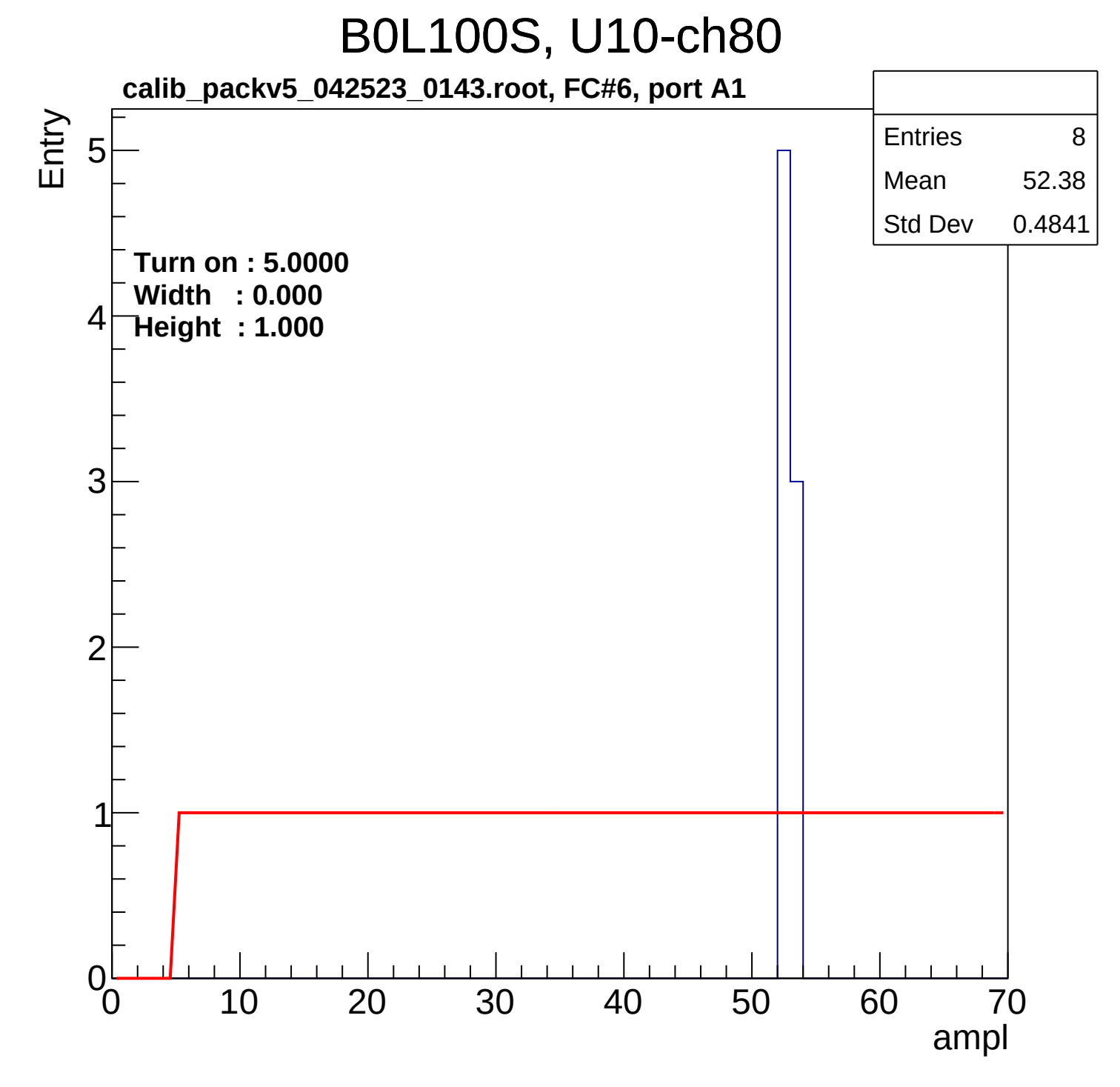

B0L100S, U10-ch75
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U10-ch76
calib_packv5_042523_0143.root, FC#6, port A1
Entries 22
Mean 34.73
Std Dev 1.958
Turn on : 16.7286
Width : 1.182
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U10-ch77
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U10-ch78
calib_packv5_042523_0143.root, FC#6, port A1
Entries 27
Mean 46.74
Std Dev 3.284
Turn on : 24.9957
Width : 3.499
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U10-ch79
calib_packv5_042523_0143.root, FC#6, port A1
Entries 18
Mean 46.56
Std Dev 1.117
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U10-ch80
calib_packv5_042523_0143.root, FC#6, port A1
Entries 8
Mean 52.38
Std Dev 0.4841
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
10
20
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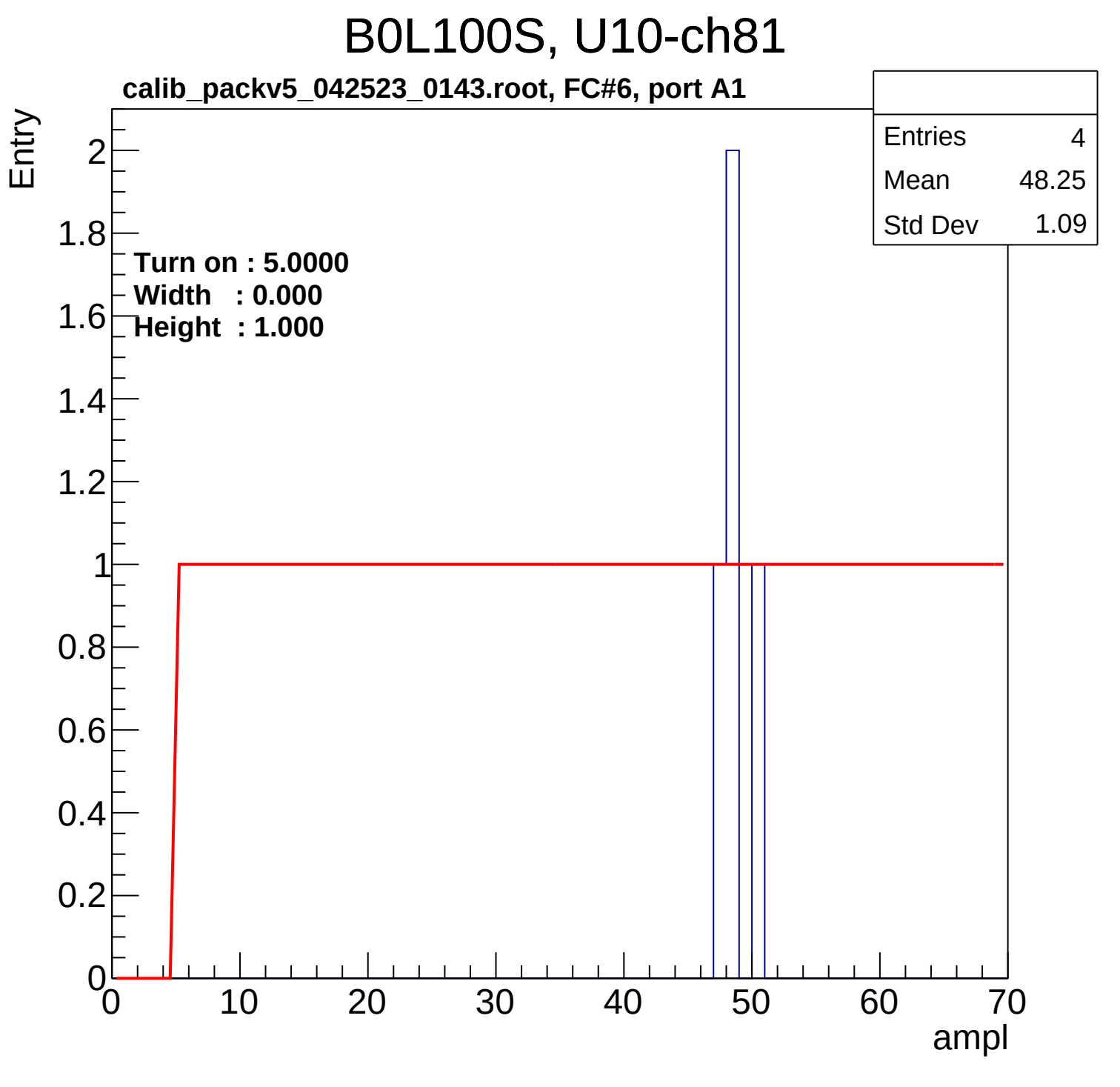
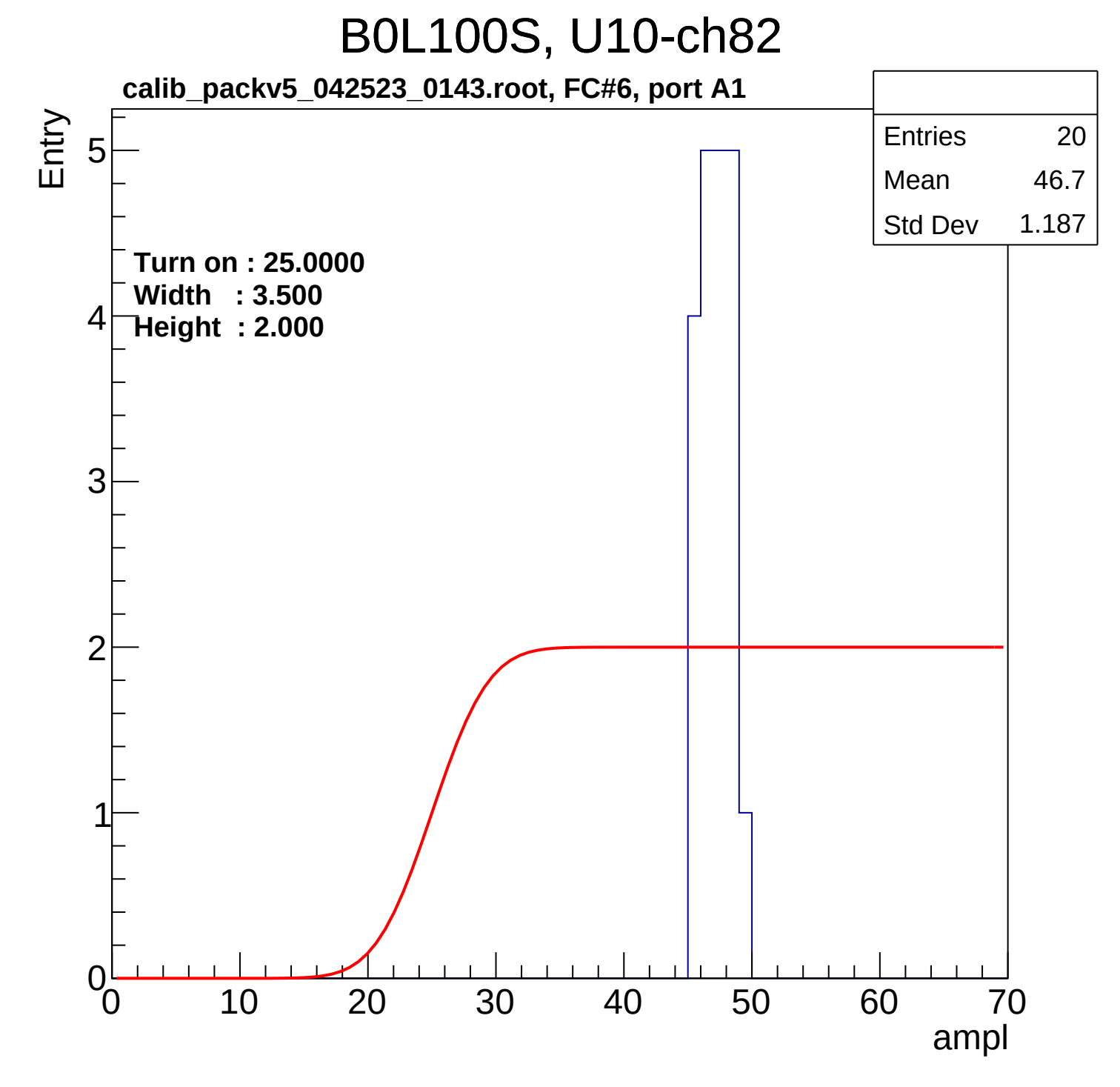
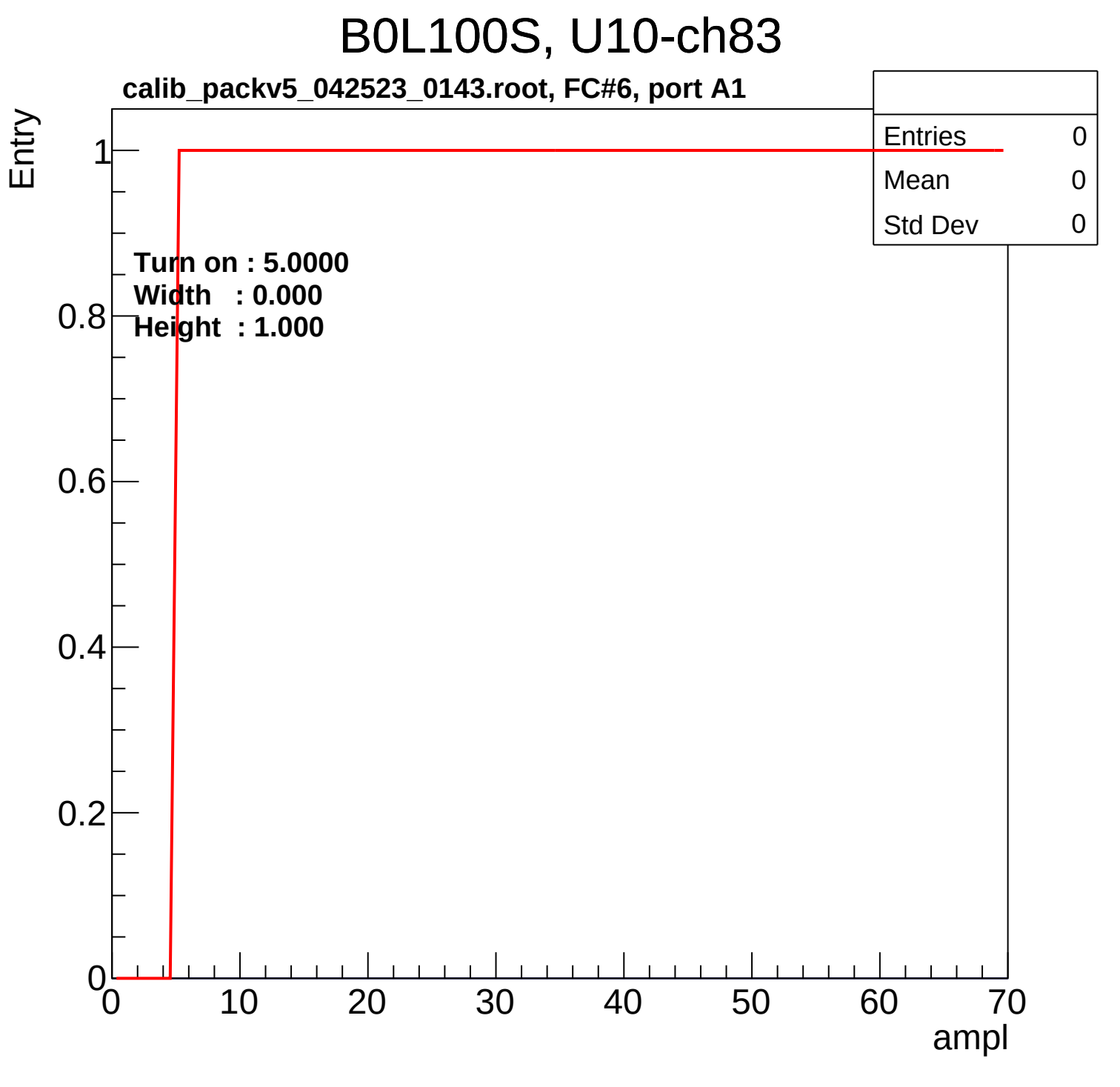
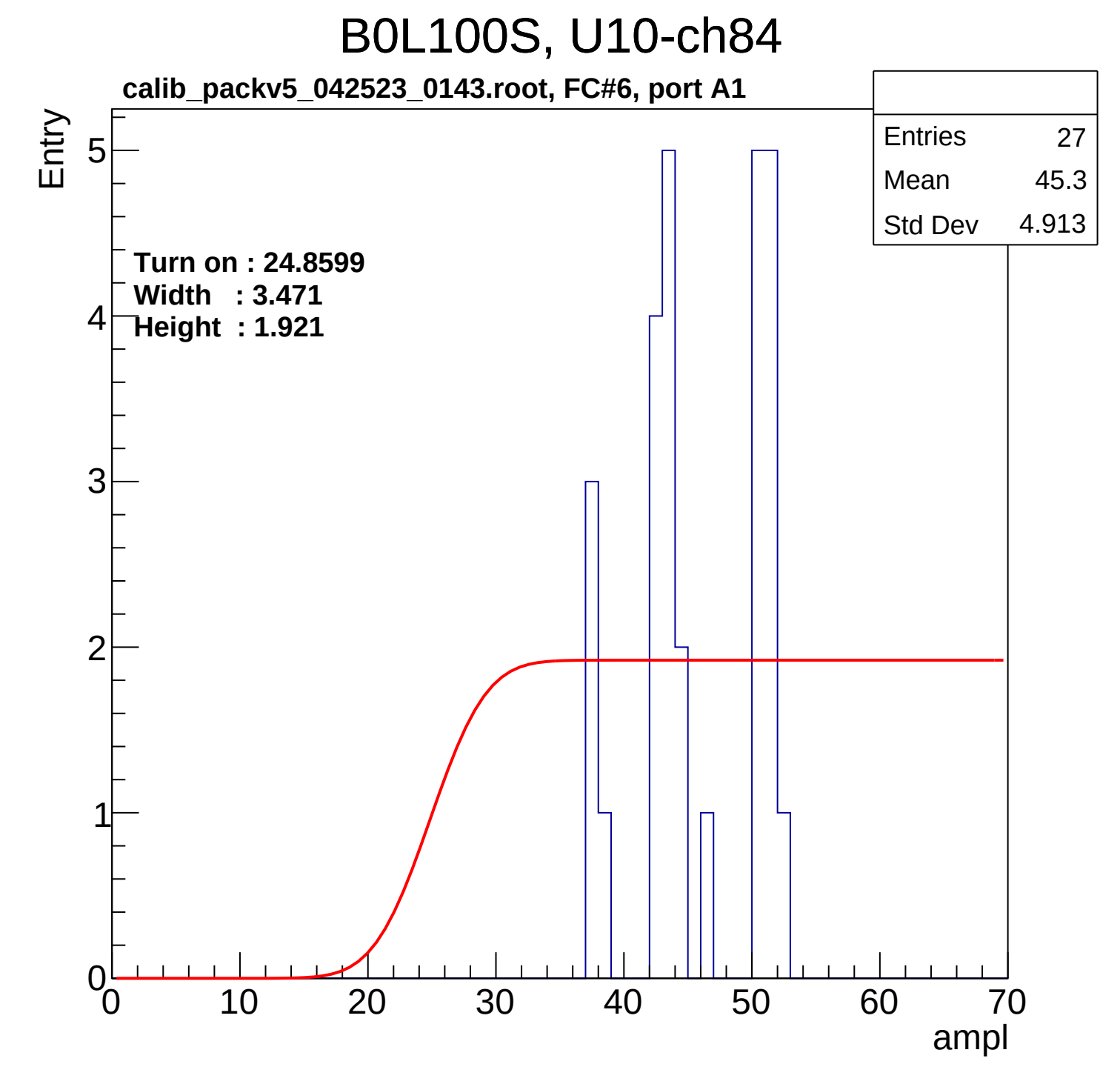
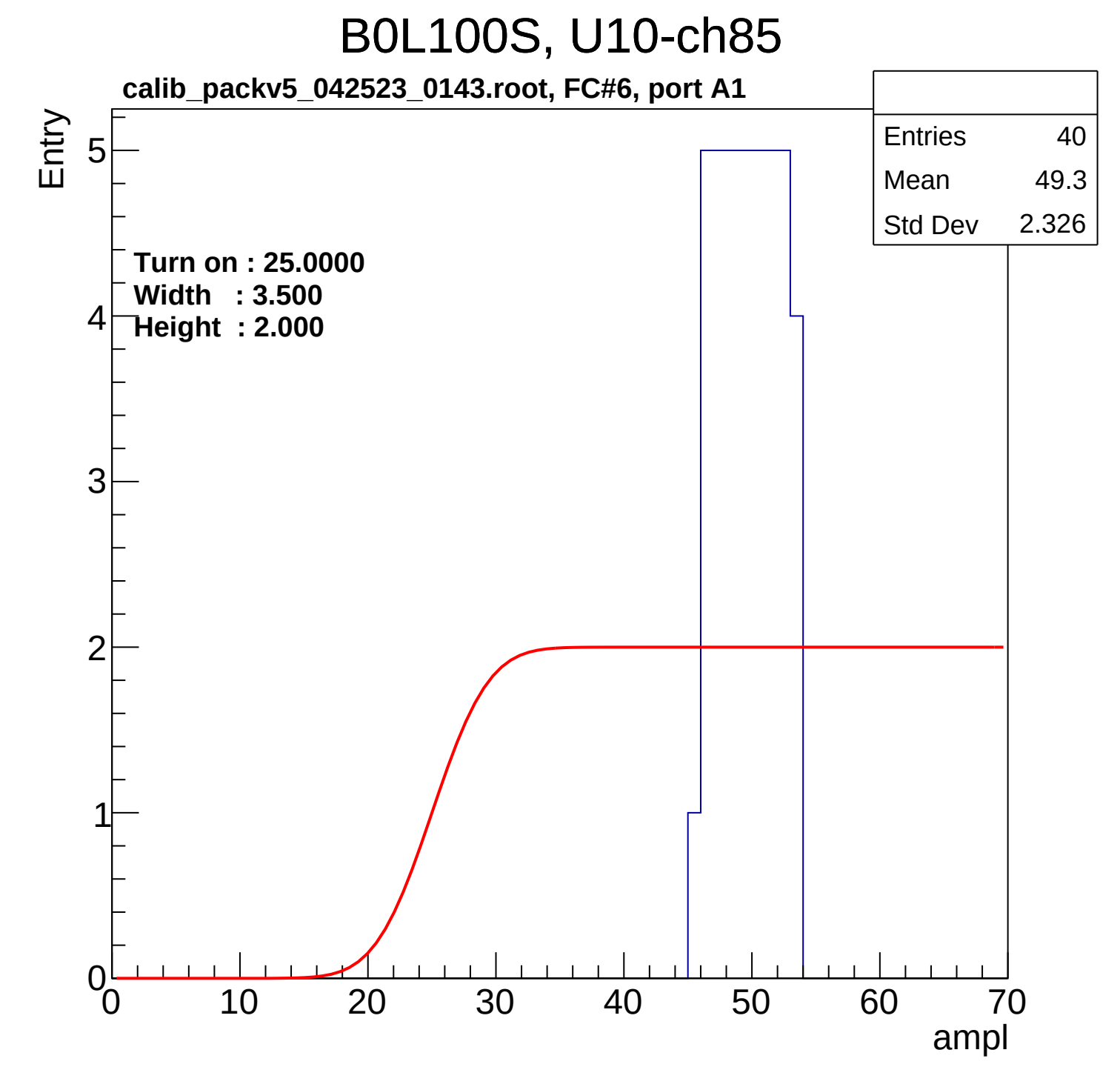
40
50
60
70

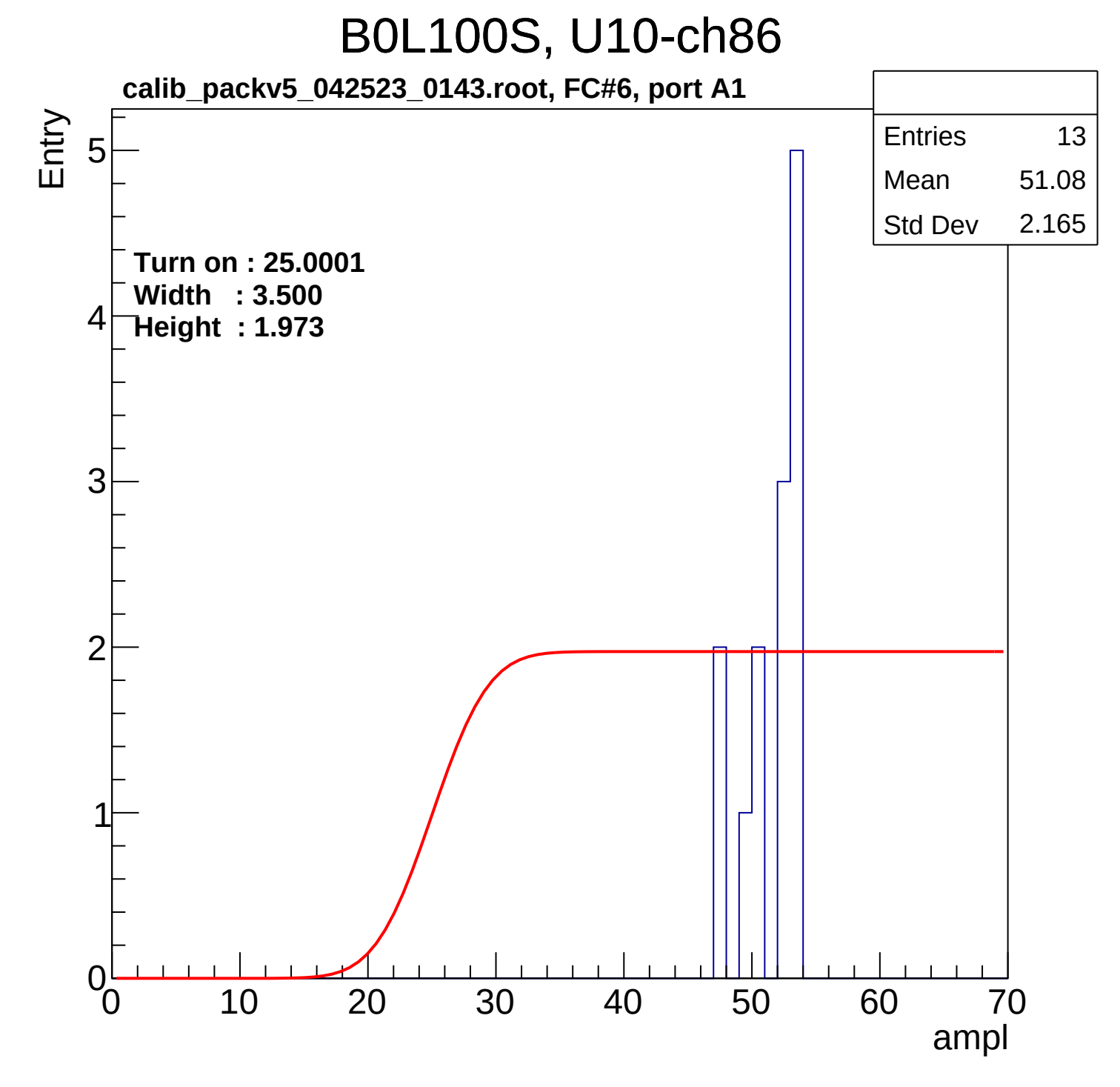

B0L100S, U10-ch81
calib_packv5_042523_0143.root, FC#6, port A1
Entries 4
Mean 48.25
Std Dev 1.09
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

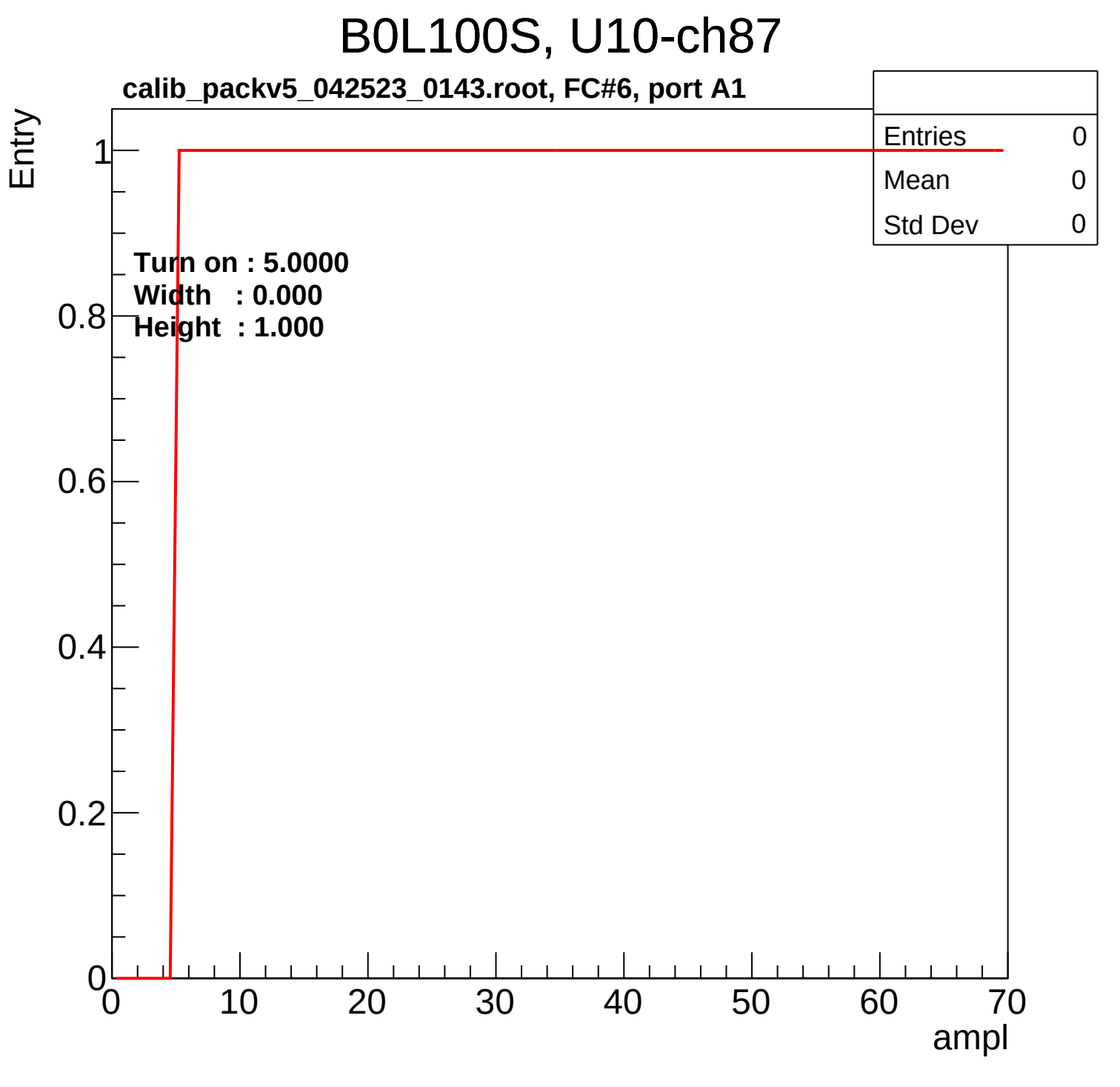

B0L100S, U10-ch82
calib_packv5_042523_0143.root, FC#6, port A1
Entries 20
Mean 46.7
Std Dev 1.187
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

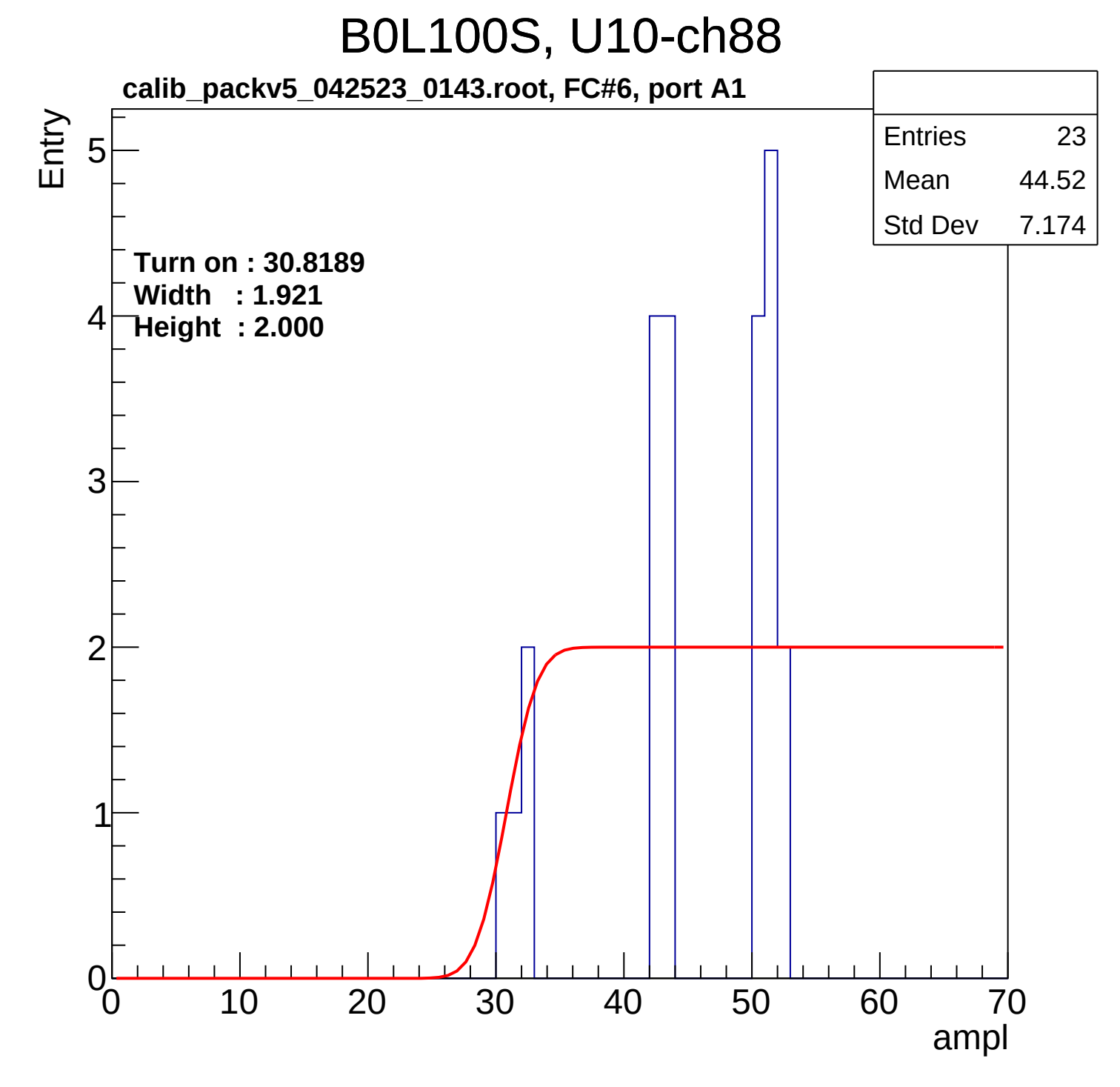

B0L100S, U10-ch83
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U10-ch84
calib_packv5_042523_0143.root, FC#6, port A1
Entries 27
Mean 45.3
Std Dev 4.913
Turn on : 24.8599
Width : 3.471
Height : 1.921
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U10-ch85
calib_packv5_042523_0143.root, FC#6, port A1
Entries 40
Mean 49.3
Std Dev 2.326
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U10-ch86
calib_packv5_042523_0143.root, FC#6, port A1
Entries 13
Mean 51.08
Std Dev 2.165
Turn on : 25.0001
Width : 3.500
Height : 1.973
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U10-ch87
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U10-ch88
calib_packv5_042523_0143.root, FC#6, port A1
Entries 23
Mean 44.52
Std Dev 7.174
Turn on : 30.8189
Width : 1.921
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
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40
50
60
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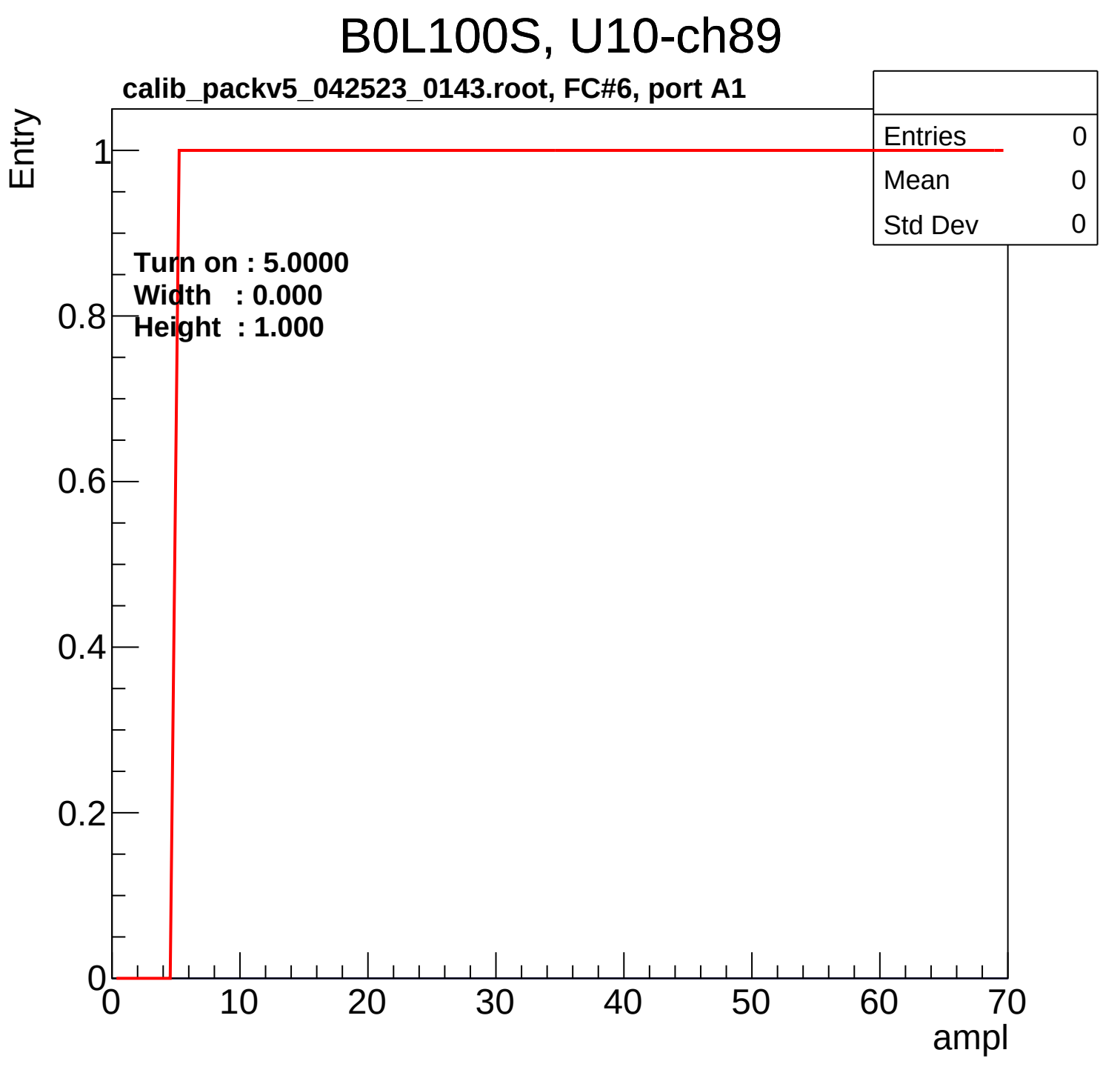
B0L100S, U10-ch89
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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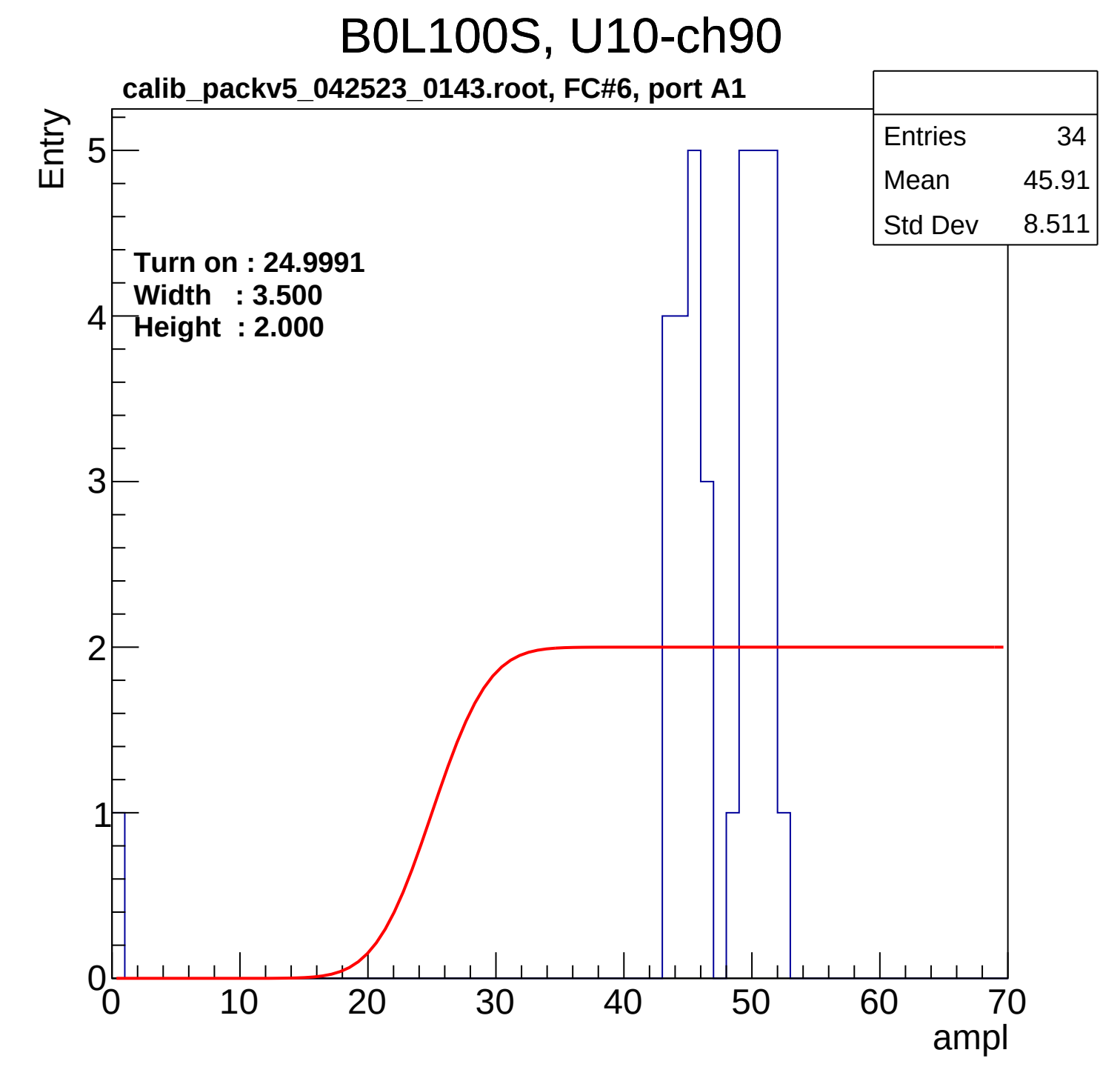
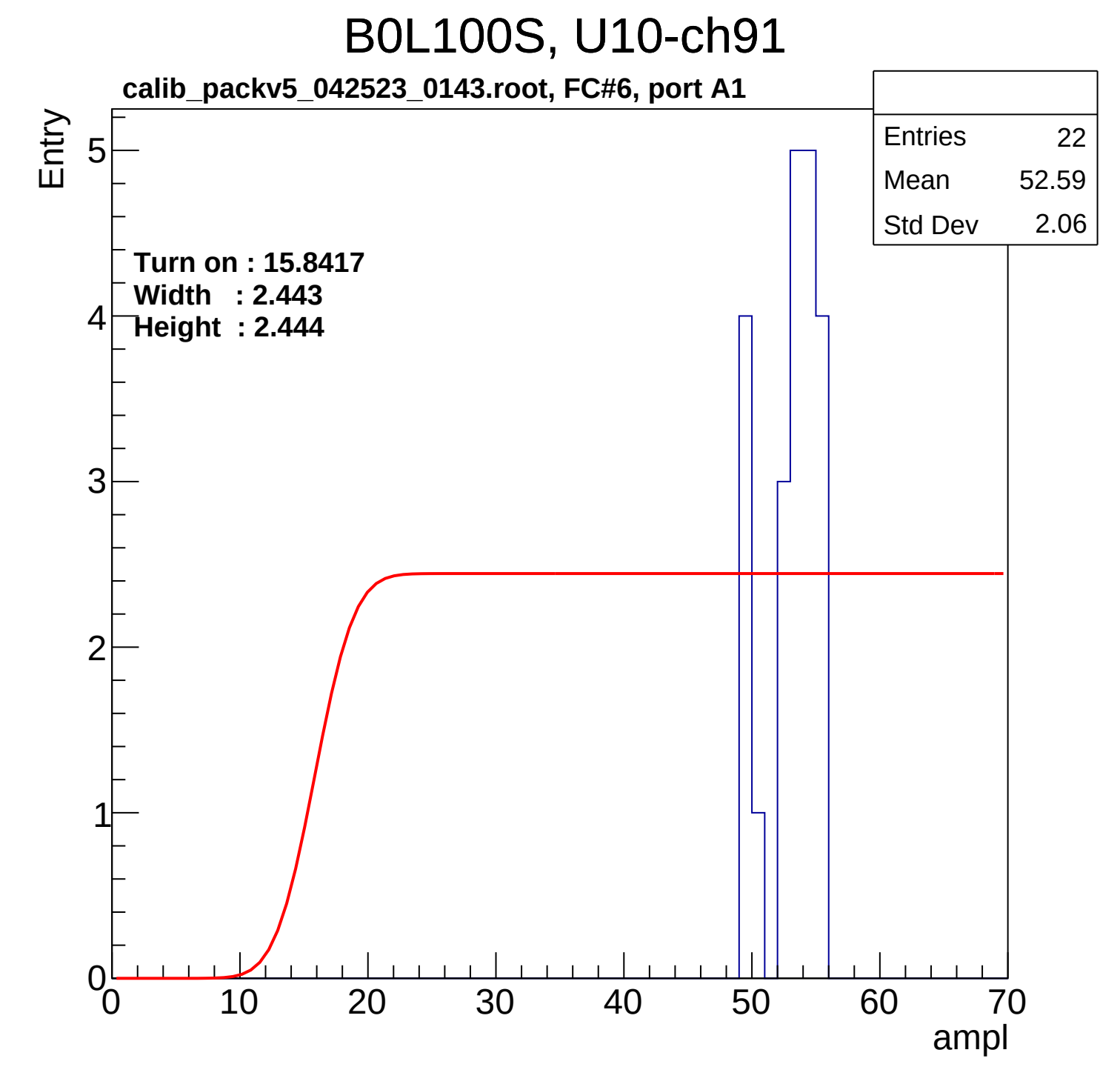
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U10-ch90
calib_packv5_042523_0143.root, FC#6, port A1
Entries 34
Mean 45.91
Std Dev 8.511
Turn on : 24.9991
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U10-ch91
calib_packv5_042523_0143.root, FC#6, port A1
Entries 22
Mean 52.59
Std Dev 2.06
Turn on : 15.8417
Width : 2.443
Height : 2.444
Entry
ampl
0
1
2
3
4
5
0
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20
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40
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60
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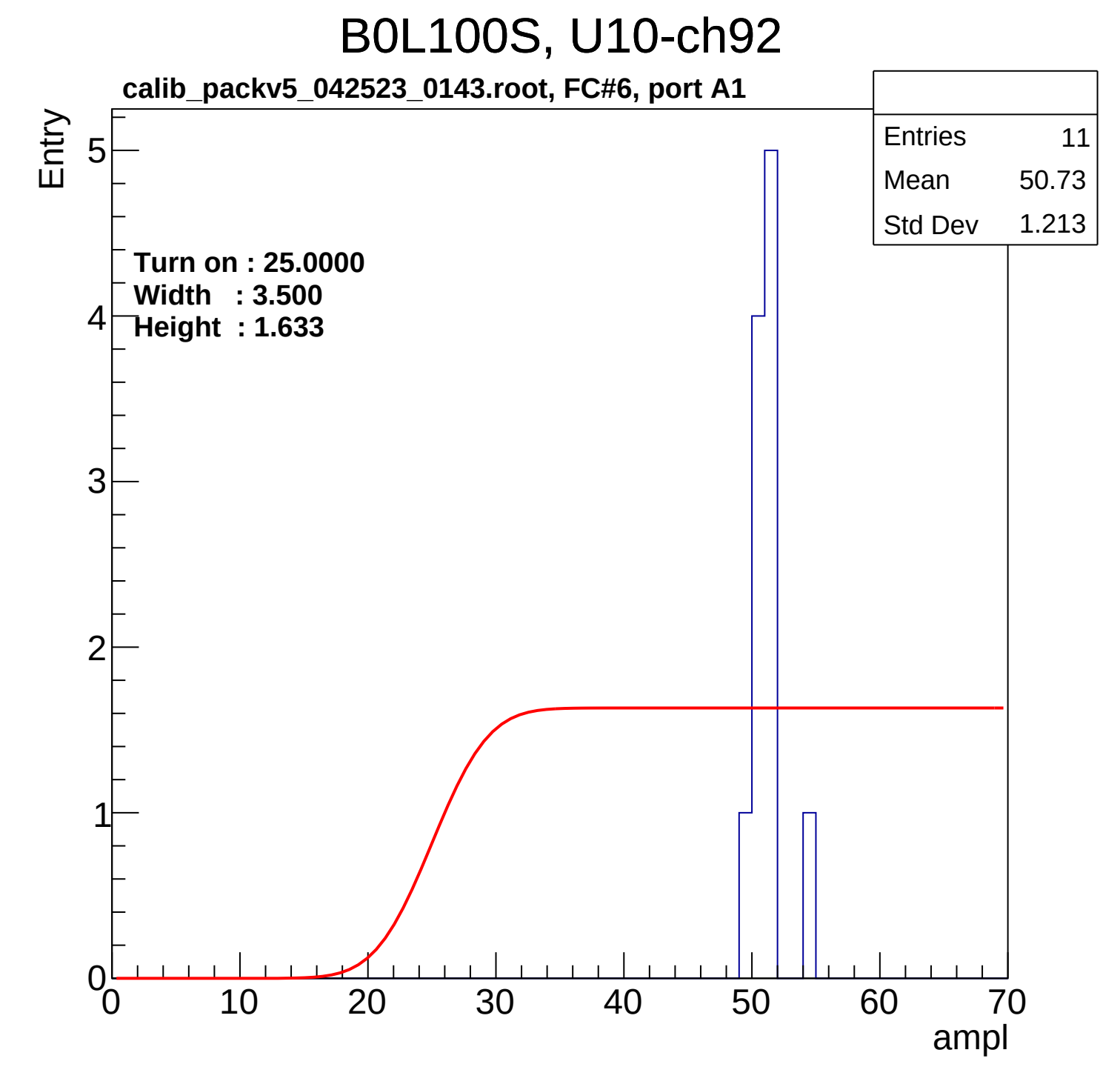
B0L100S, U10-ch92
calib_packv5_042523_0143.root, FC#6, port A1
Entries 11
Mean 50.73
Std Dev 1.213
Turn on : 25.0000
Width : 3.500
Height : 1.633
Entry
ampl
0
1
2
3
4
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0
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40
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60
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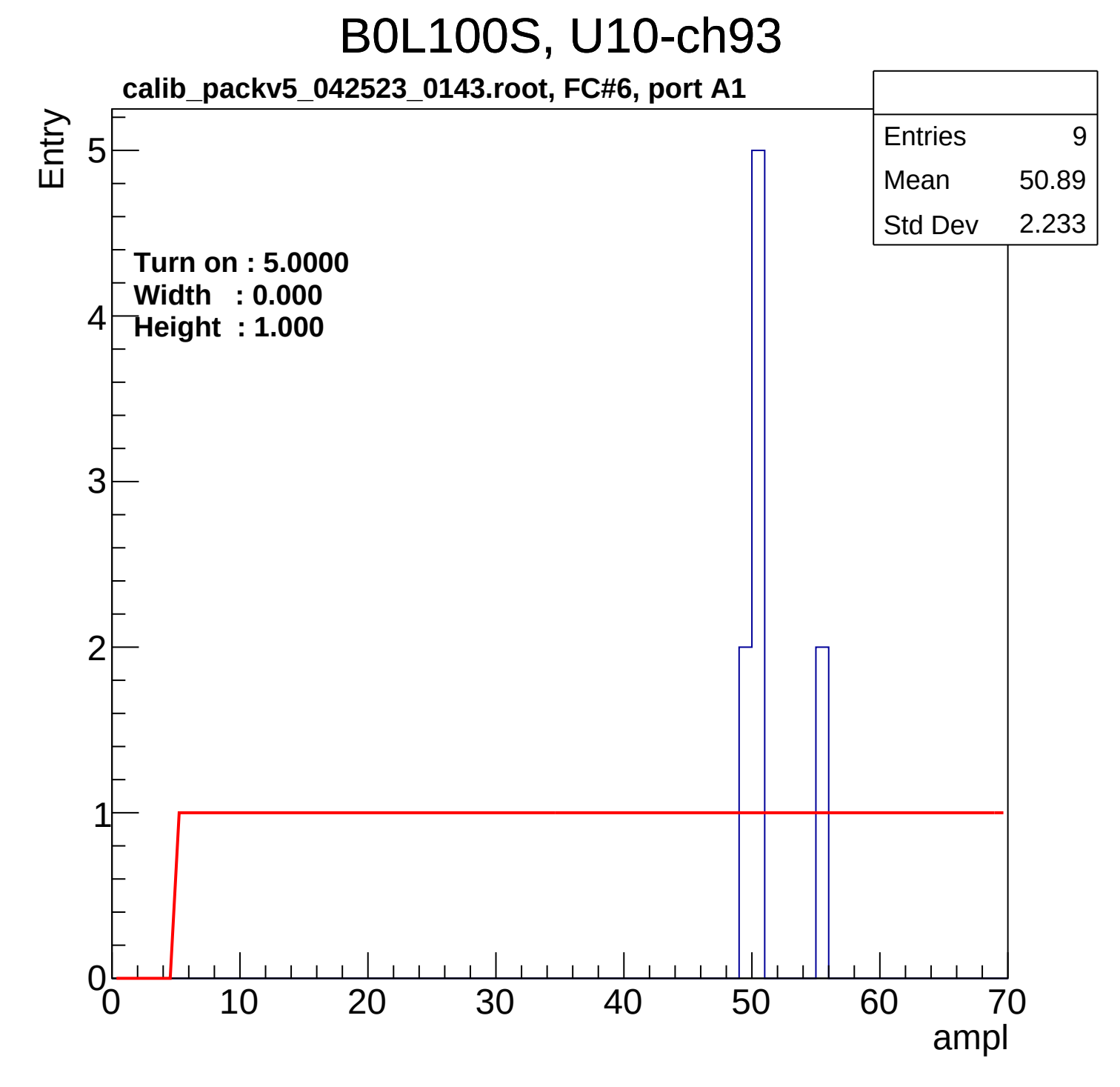
B0L100S, U10-ch93
calib_packv5_042523_0143.root, FC#6, port A1
Entries 9
Mean 50.89
Std Dev 2.233
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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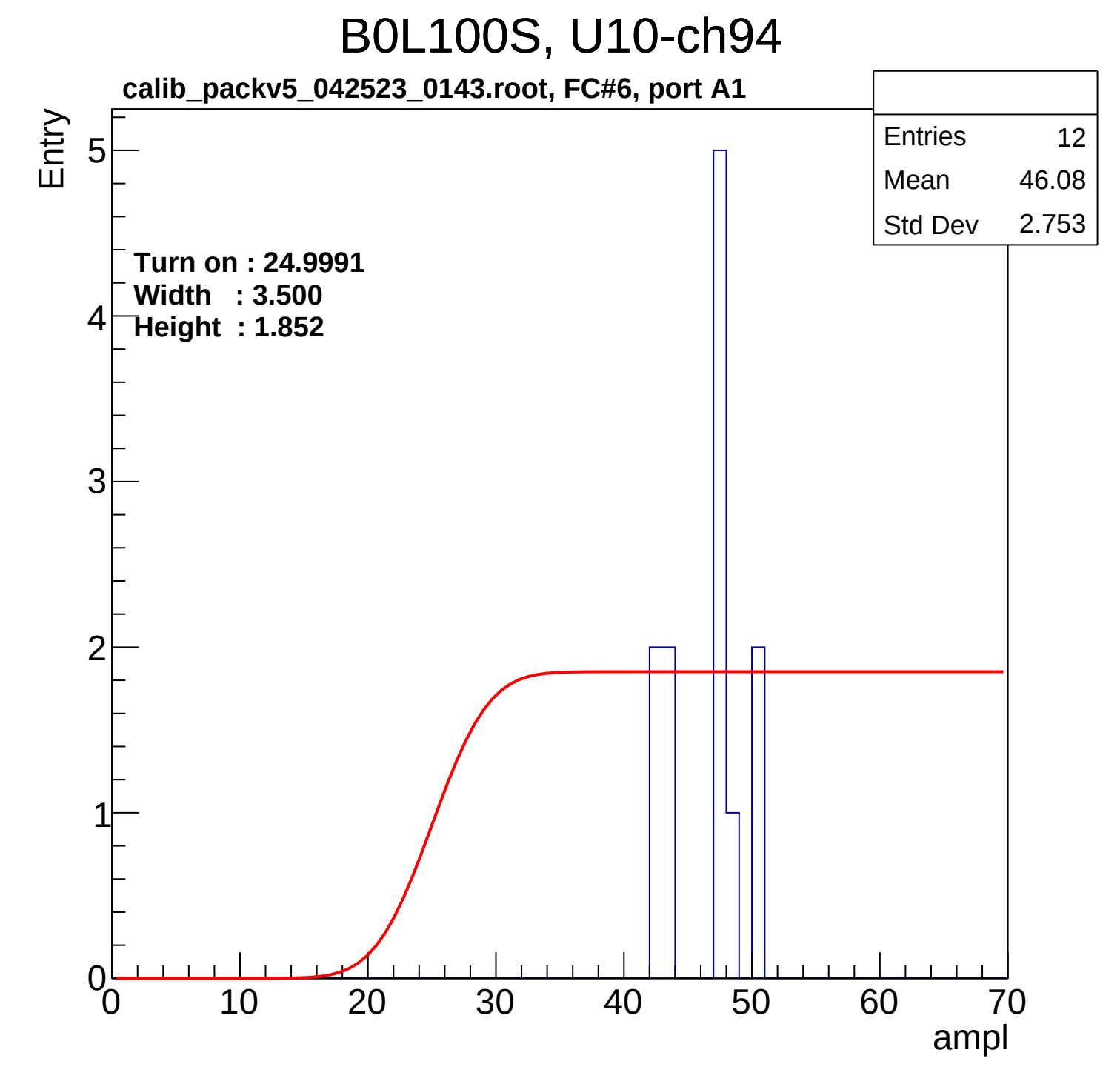
B0L100S, U10-ch94
calib_packv5_042523_0143.root, FC#6, port A1
Entries 12
Mean 46.08
Std Dev 2.753
Turn on : 24.9991
Width : 3.500
Height : 1.852
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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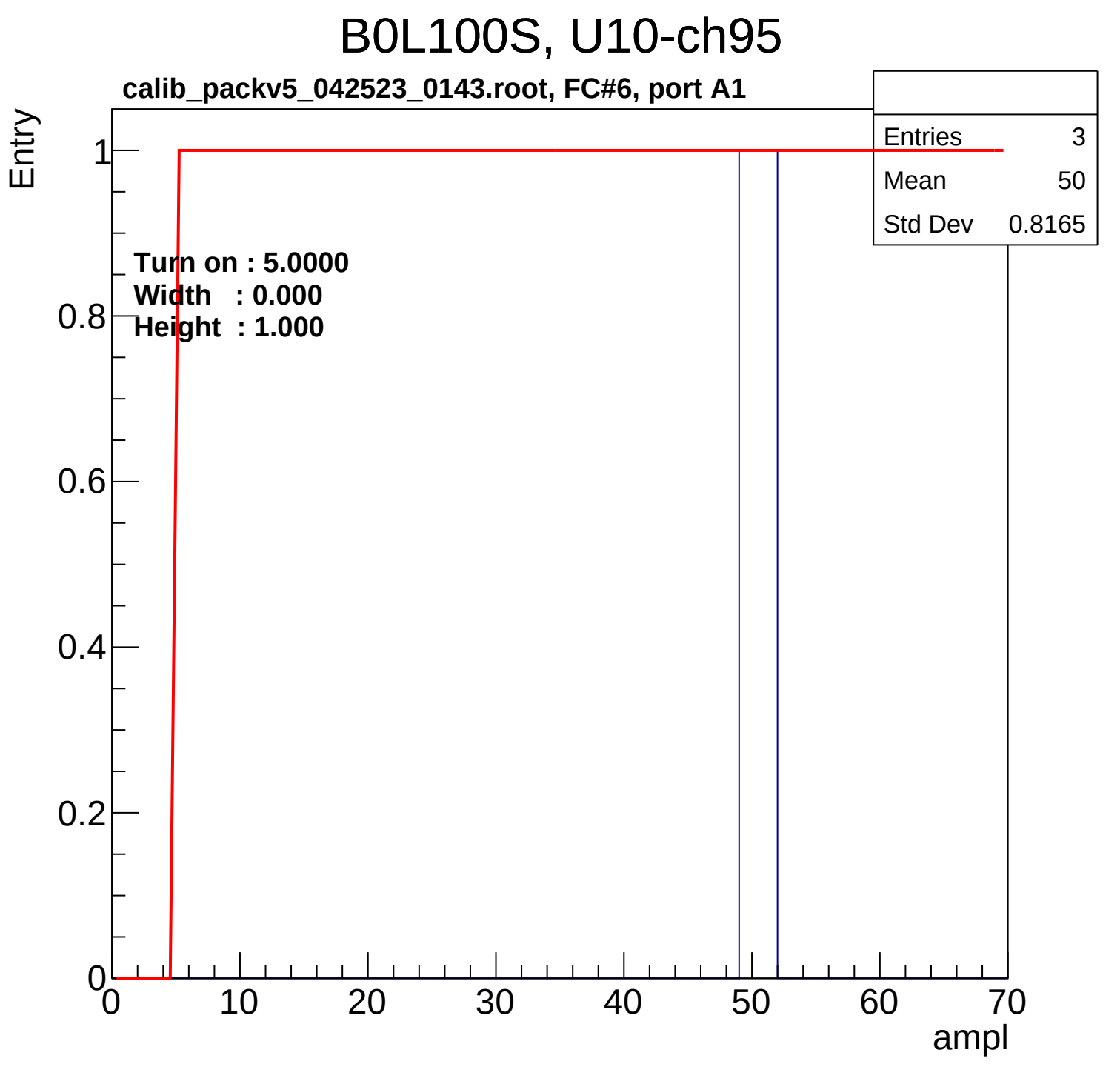
B0L100S, U10-ch95
calib_packv5_042523_0143.root, FC#6, port A1
Entries 3
Mean 50
Std Dev 0.8165
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
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40
50
60
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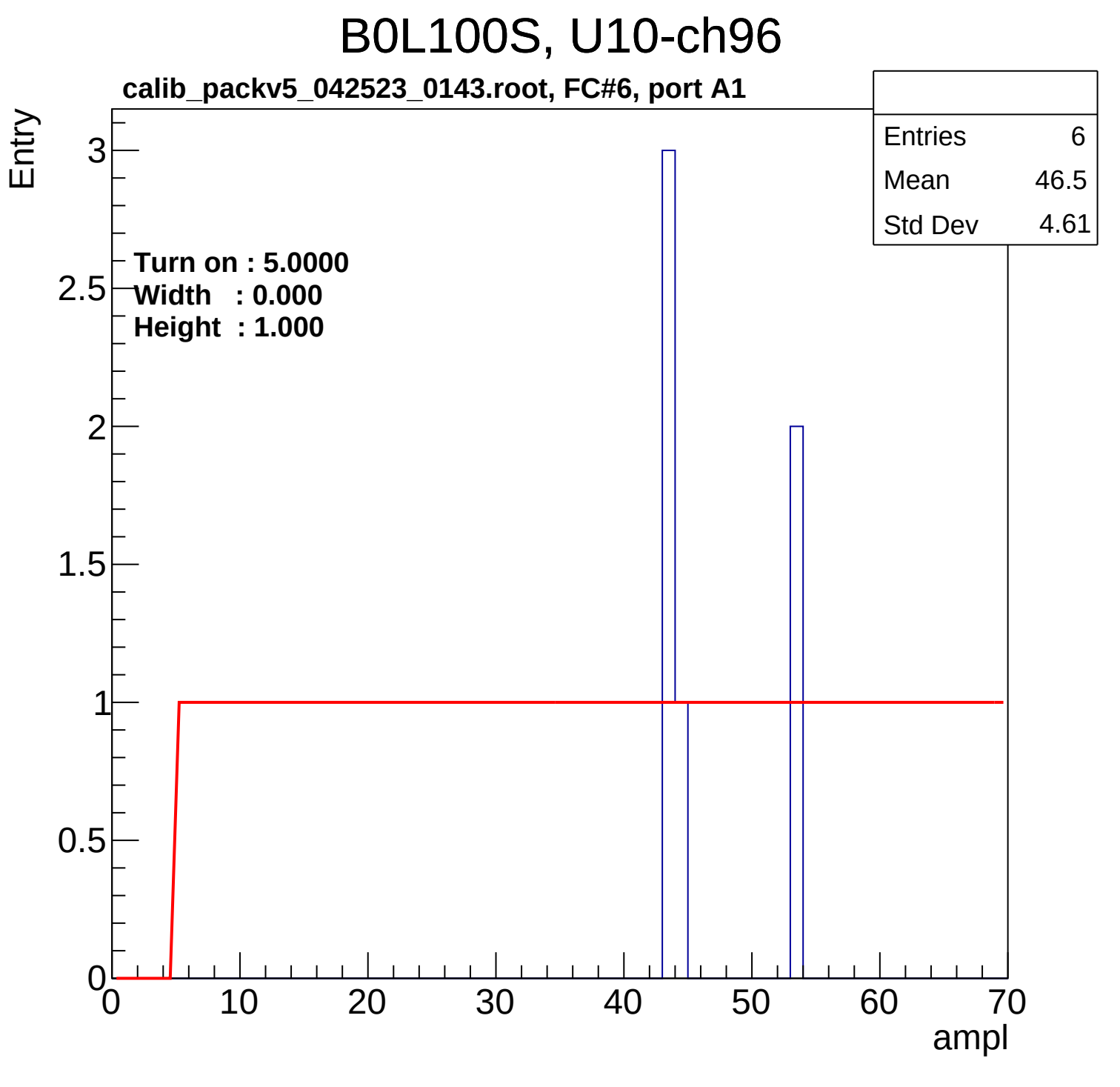
B0L100S, U10-ch96
calib_packv5_042523_0143.root, FC#6, port A1
Entries 6
Mean 46.5
Std Dev 4.61
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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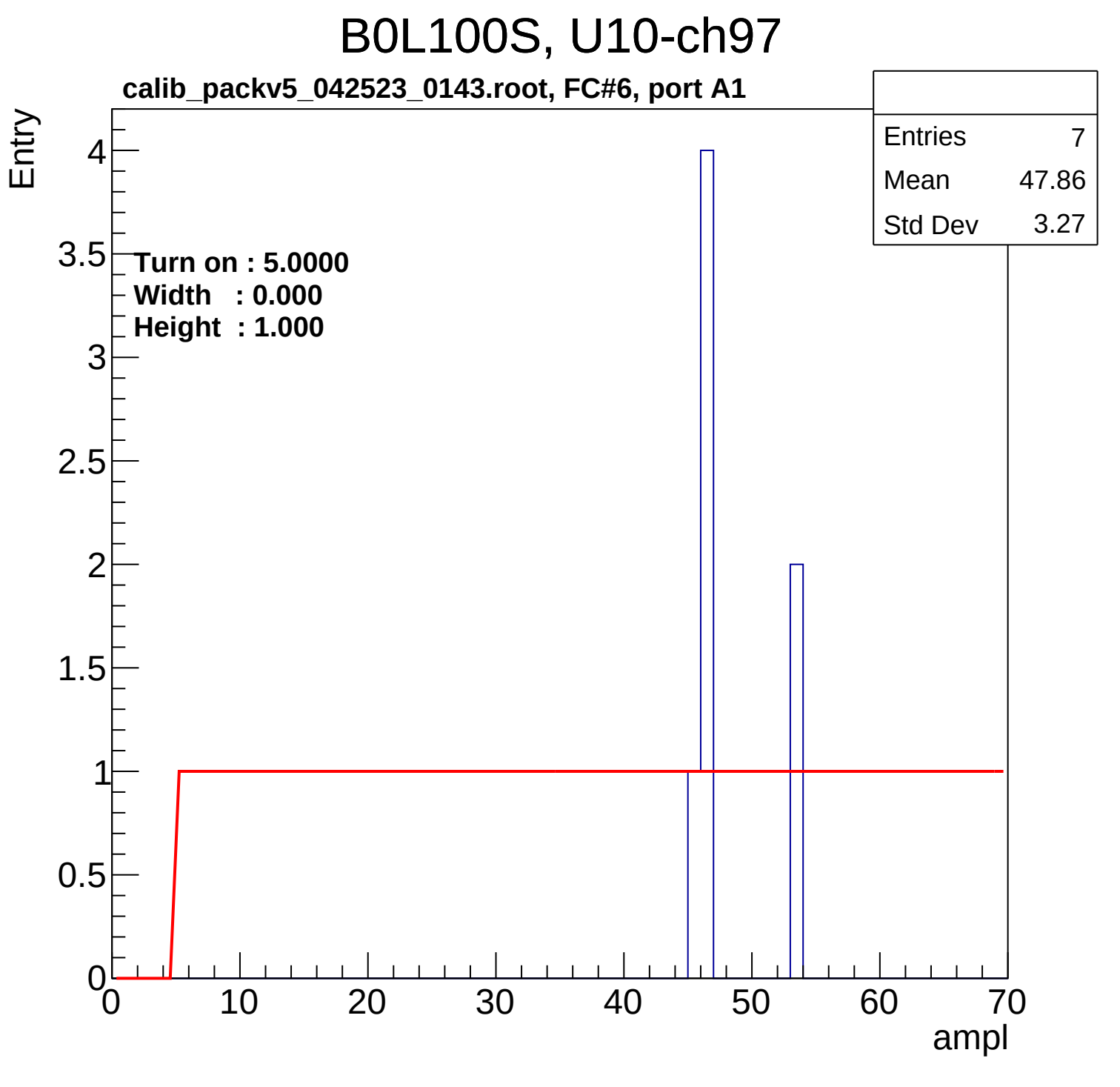
B0L100S, U10-ch97
calib_packv5_042523_0143.root, FC#6, port A1
Entries 7
Mean 47.86
Std Dev 3.27
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
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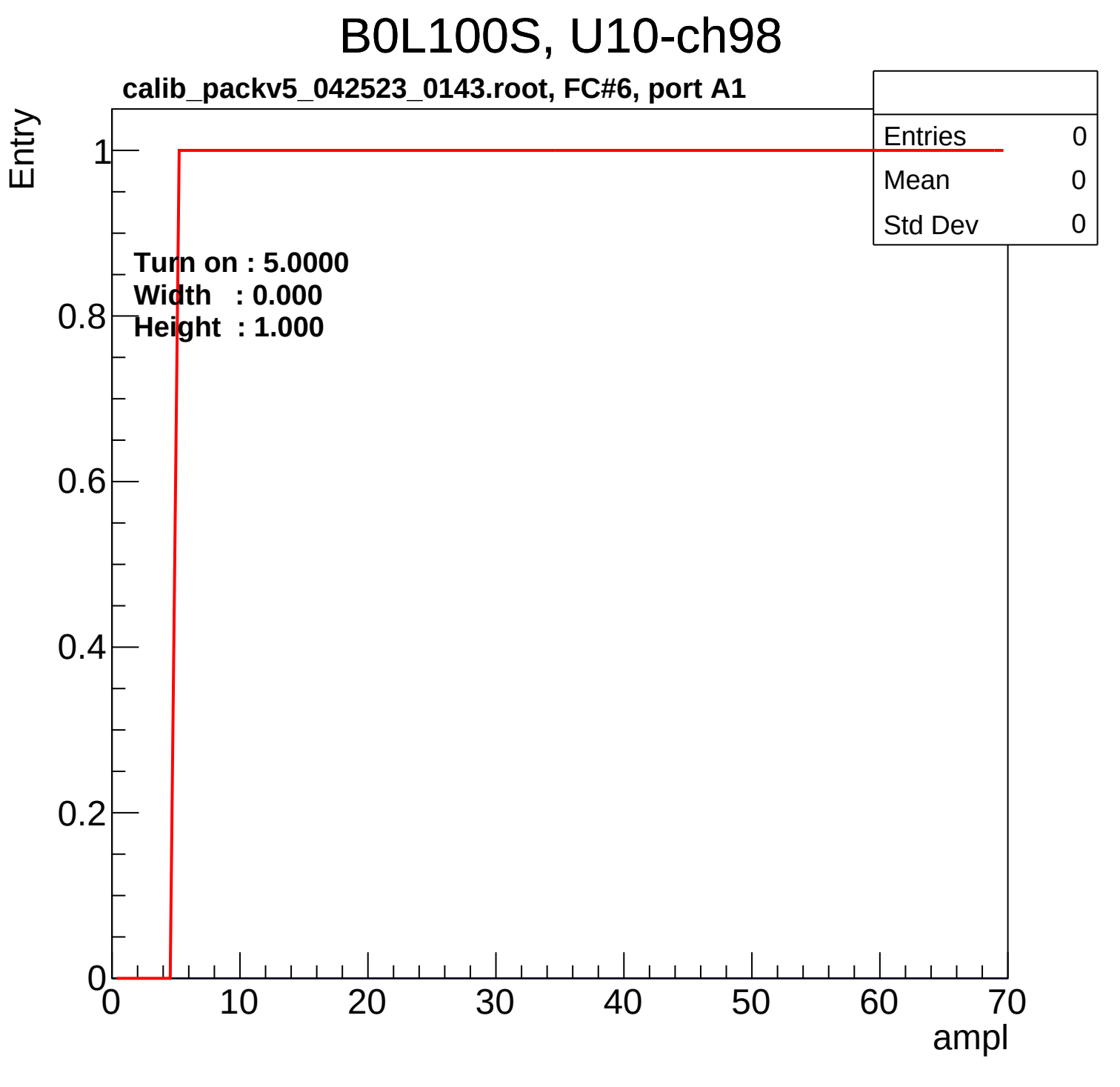
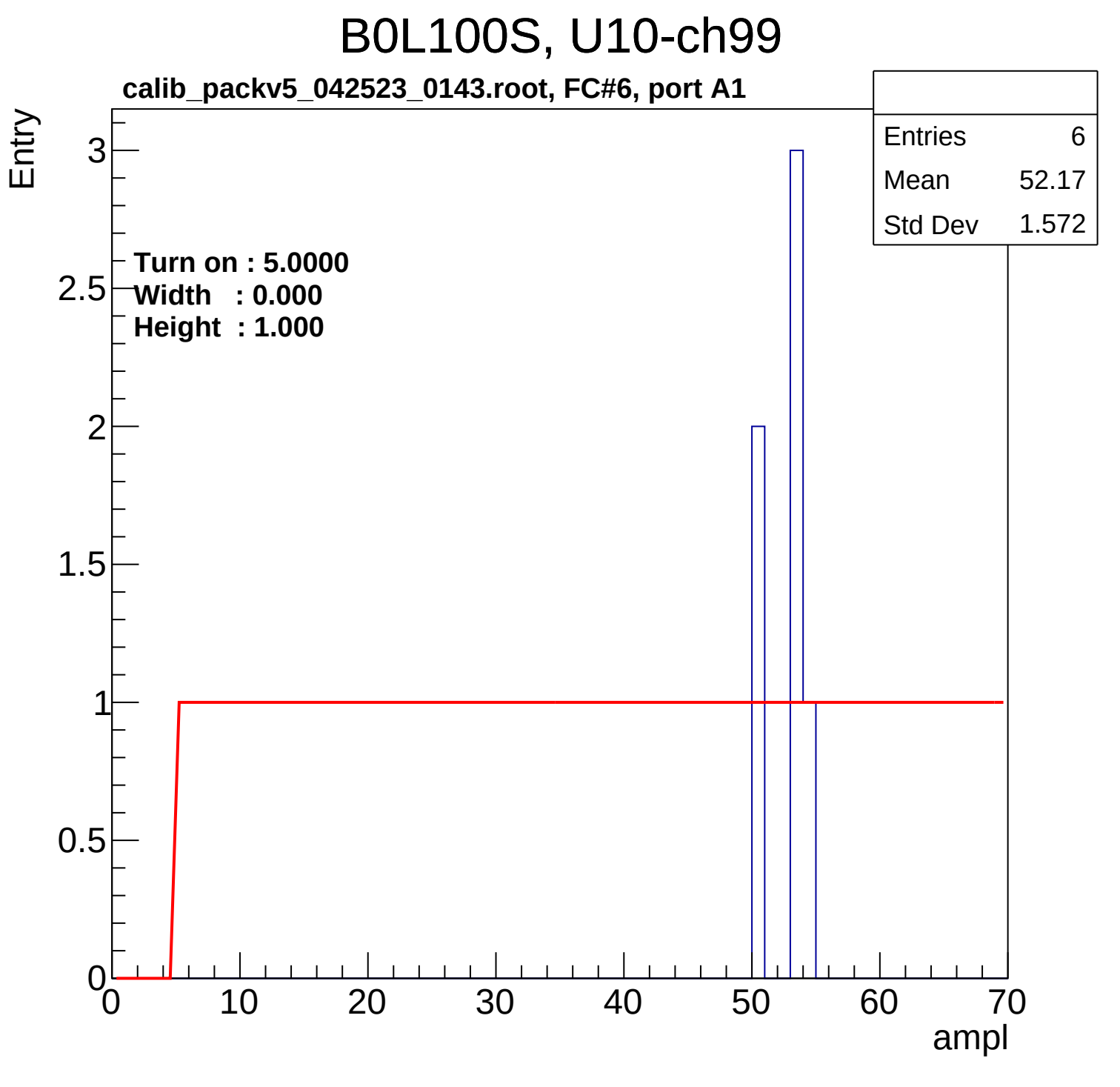
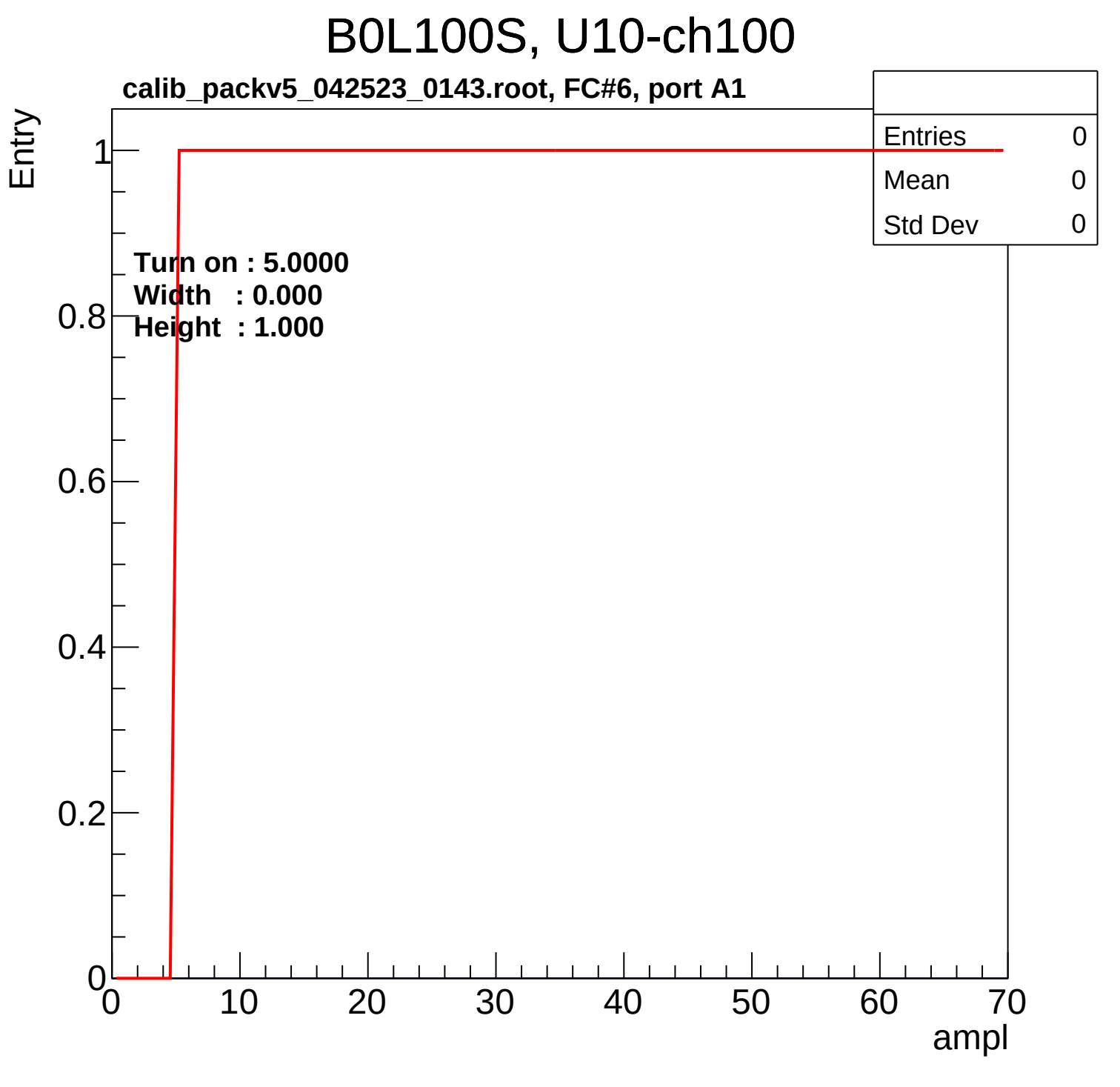
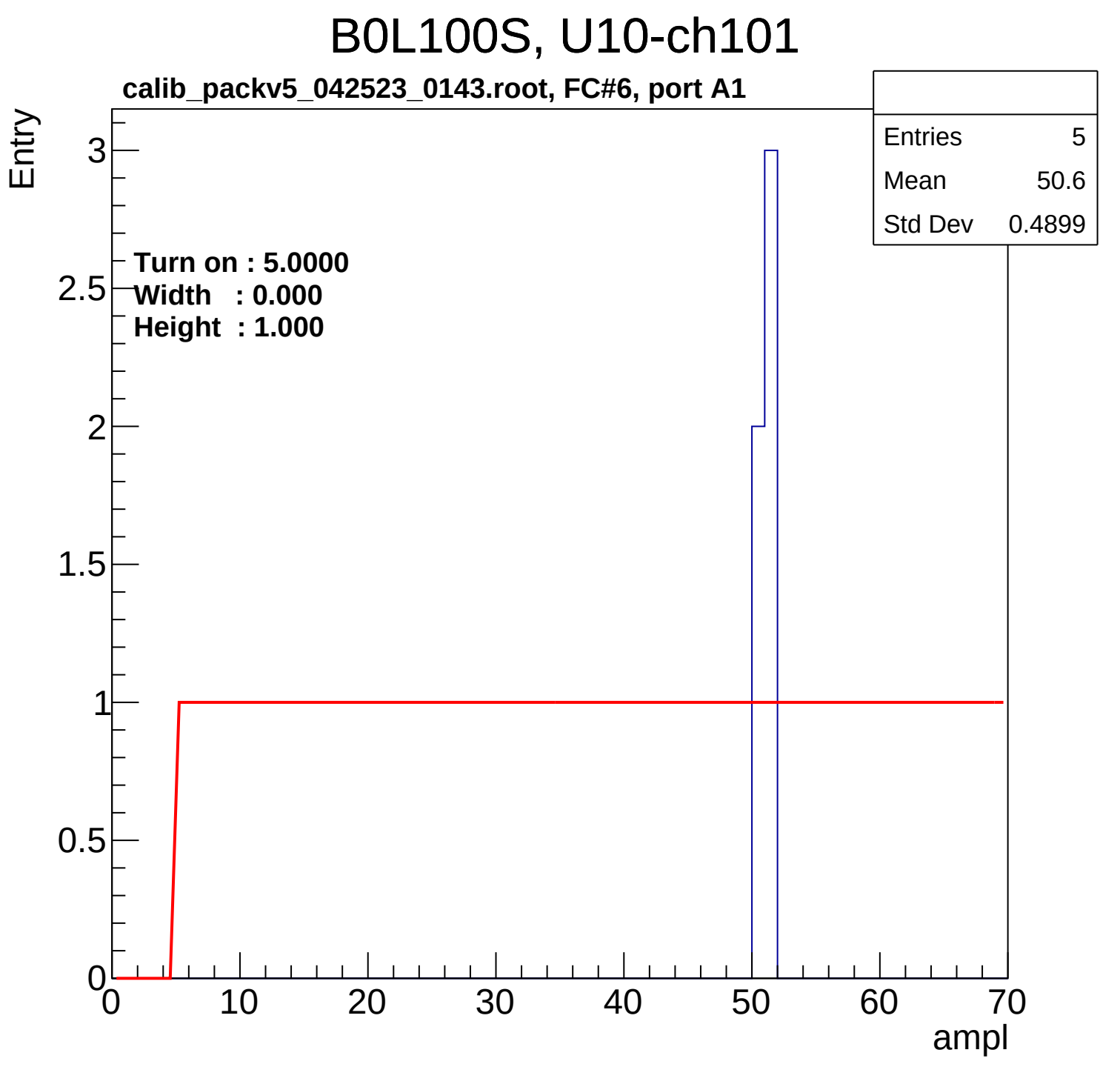
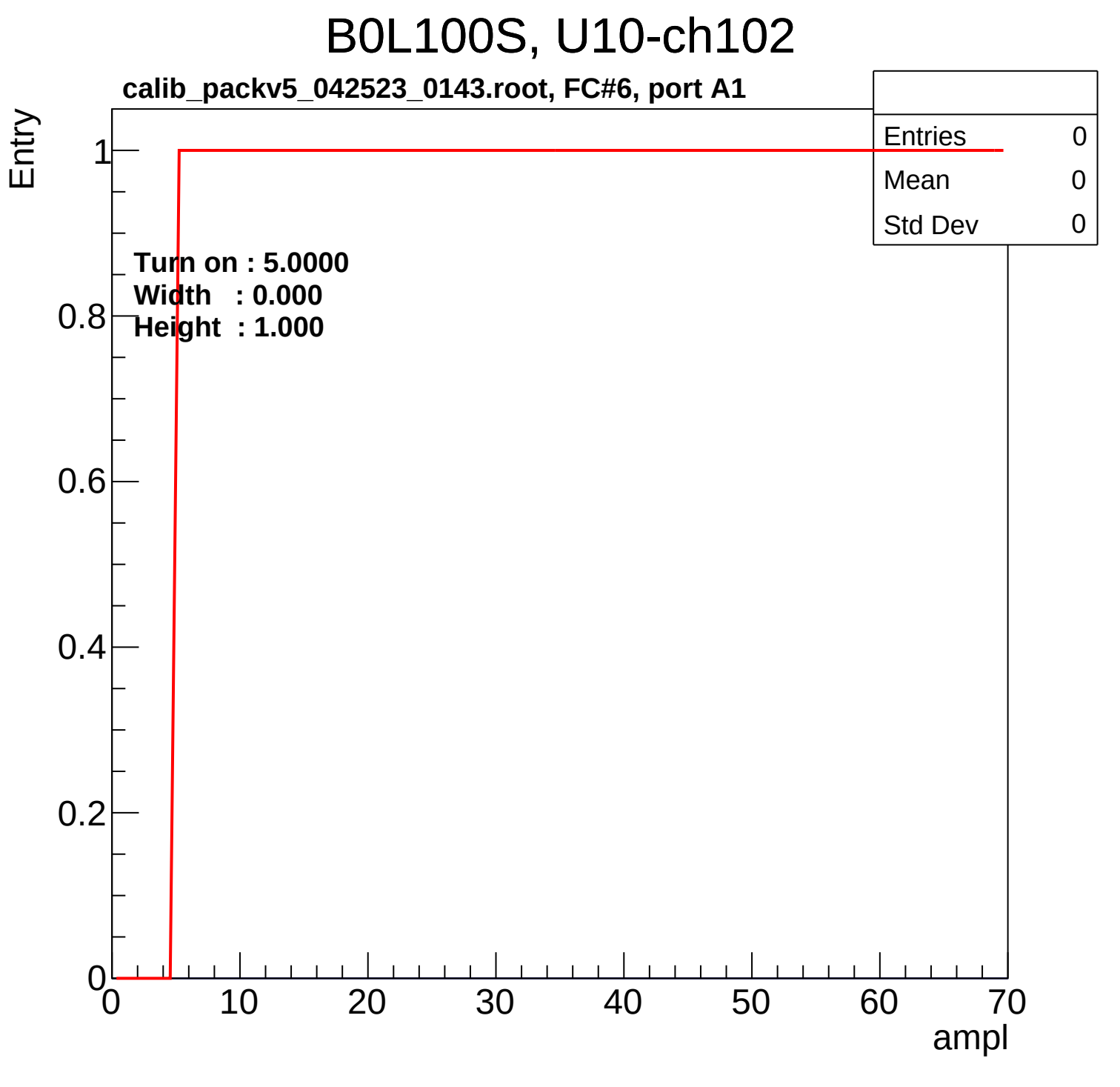
20
30
40
50
60
70

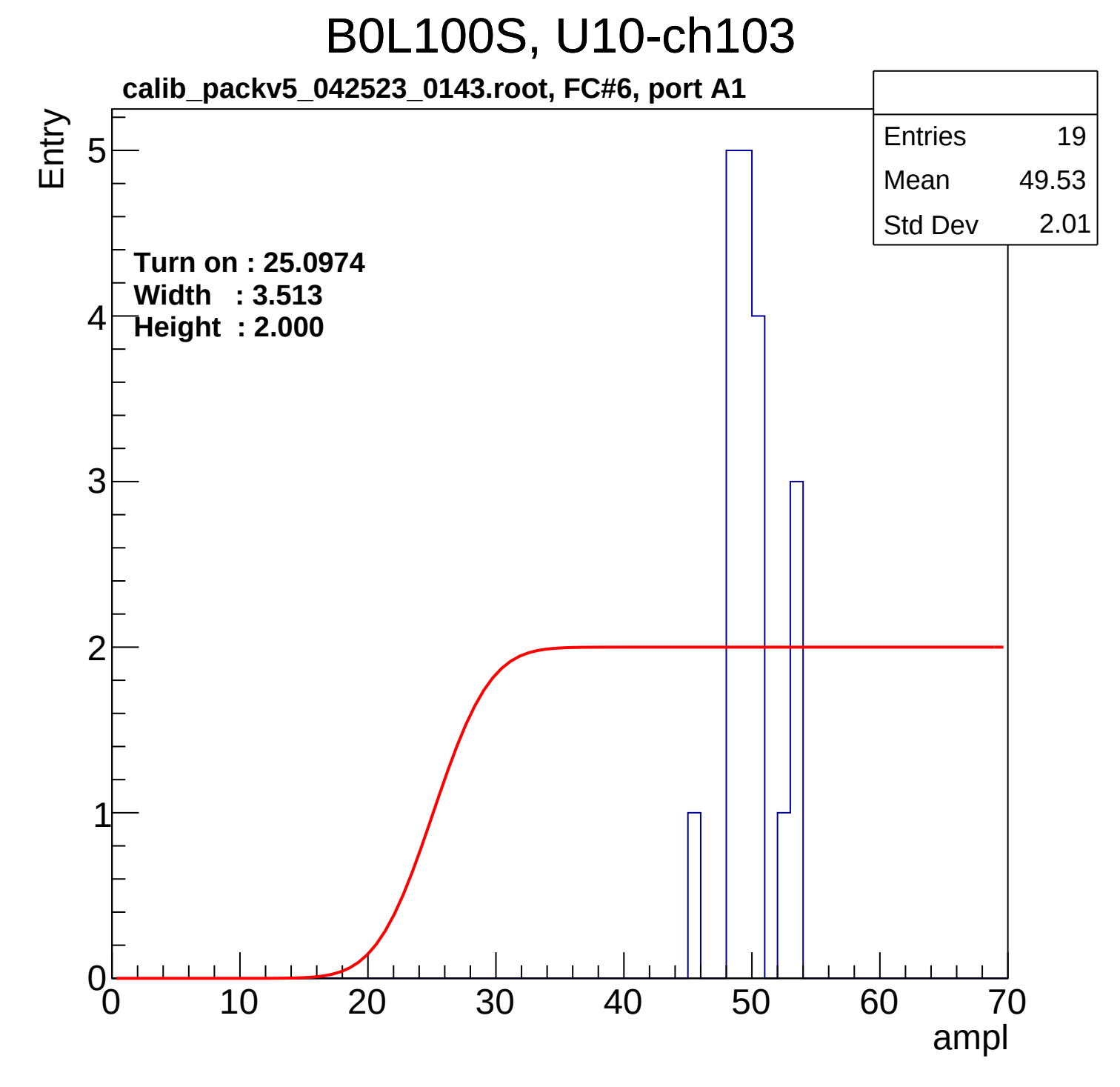

B0L100S, U10-ch98
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U10-ch99
calib_packv5_042523_0143.root, FC#6, port A1
Entries 6
Mean 52.17
Std Dev 1.572
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B0L100S, U10-ch100
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U10-ch101
calib_packv5_042523_0143.root, FC#6, port A1
Entries 5
Mean 50.6
Std Dev 0.4899
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B0L100S, U10-ch102
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U10-ch103
calib_packv5_042523_0143.root, FC#6, port A1
Entries 19
Mean 49.53
Std Dev 2.01
Turn on : 25.0974
Width : 3.513
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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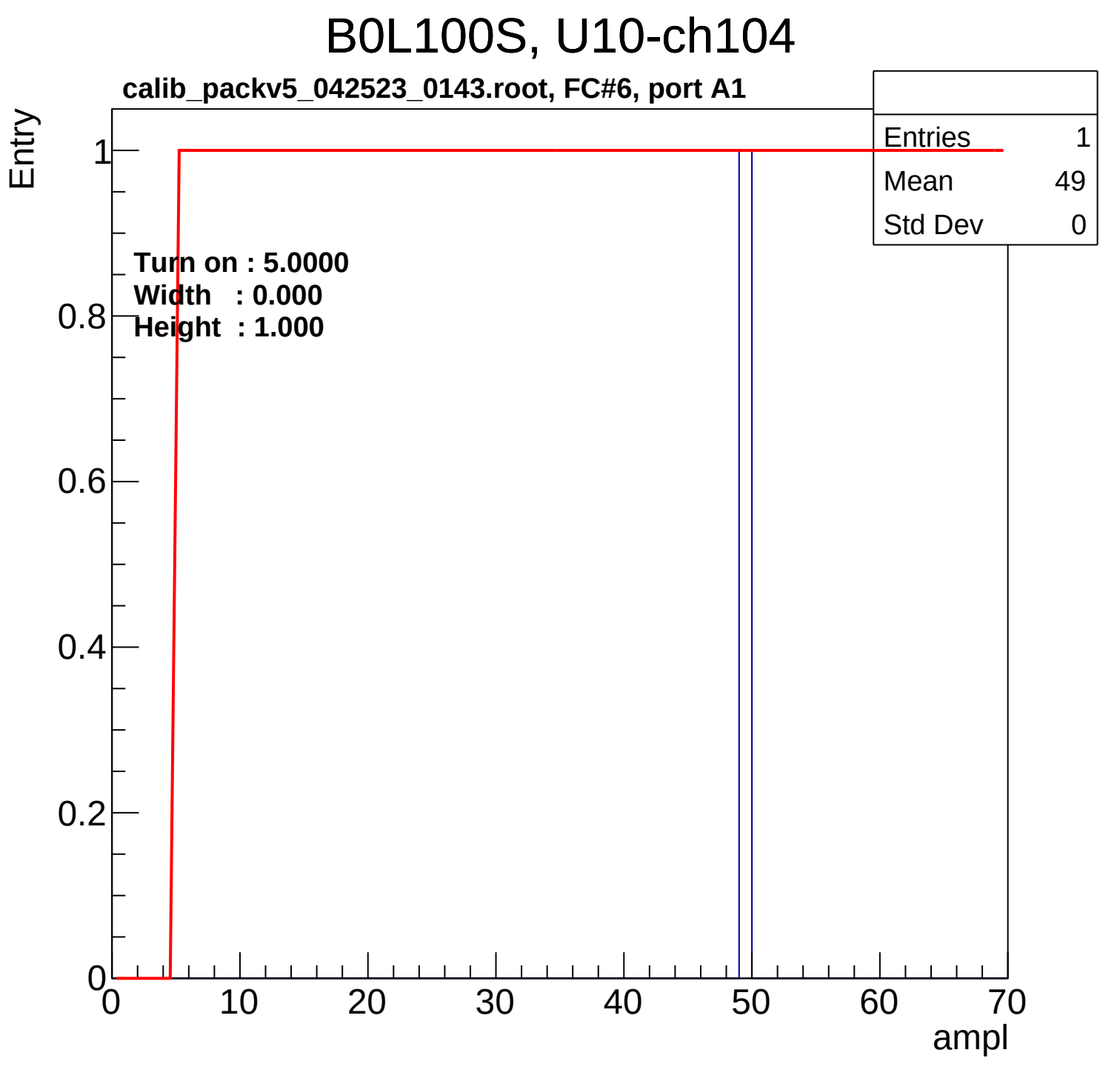
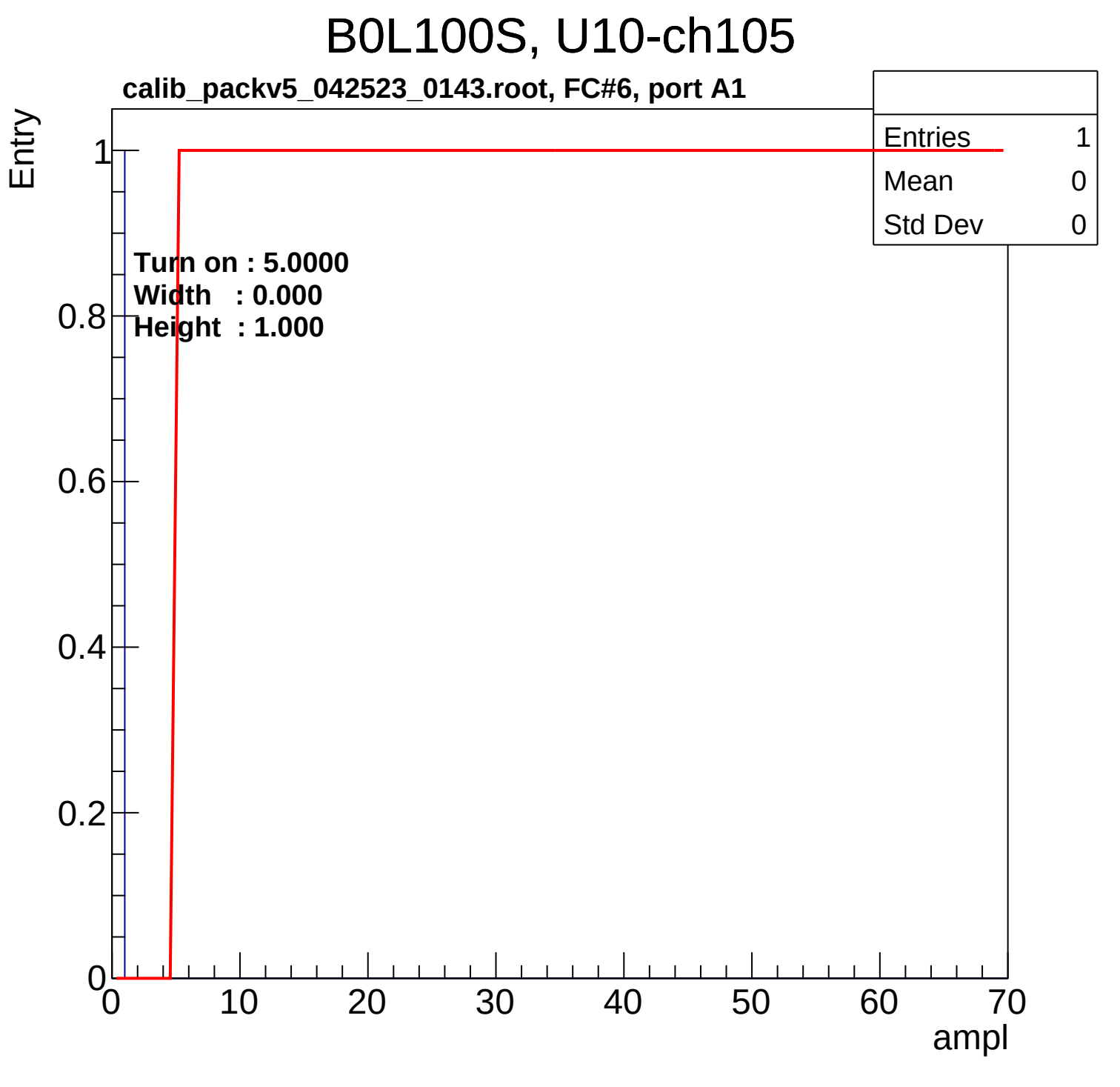
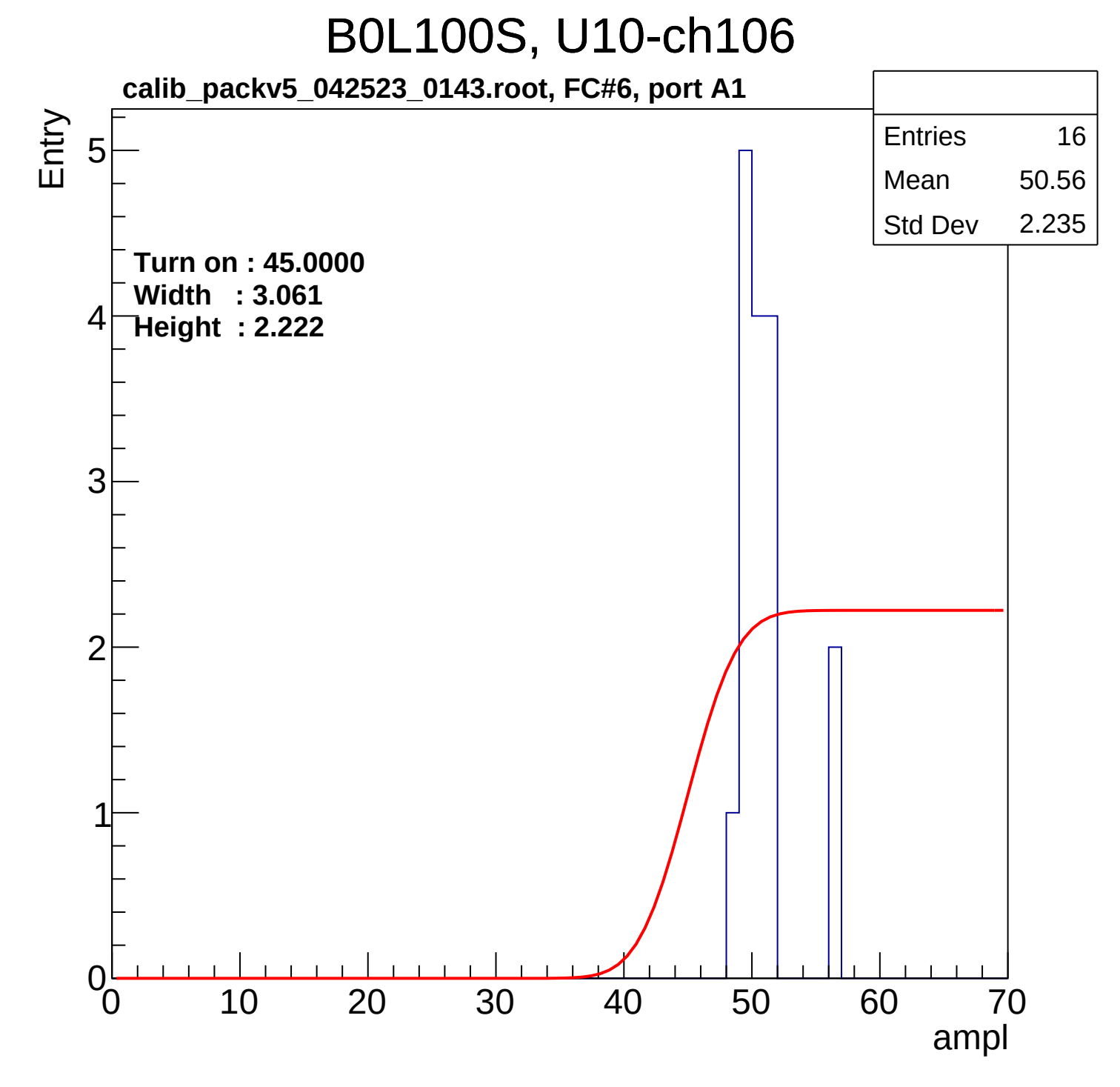

B0L100S, U10-ch104
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 49
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U10-ch105
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U10-ch106
calib_packv5_042523_0143.root, FC#6, port A1
Entries 16
Mean 50.56
Std Dev 2.235
Turn on : 45.0000
Width : 3.061
Height : 2.222
Entry
ampl
0
1
2
3
4
5
0
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20
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40
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60
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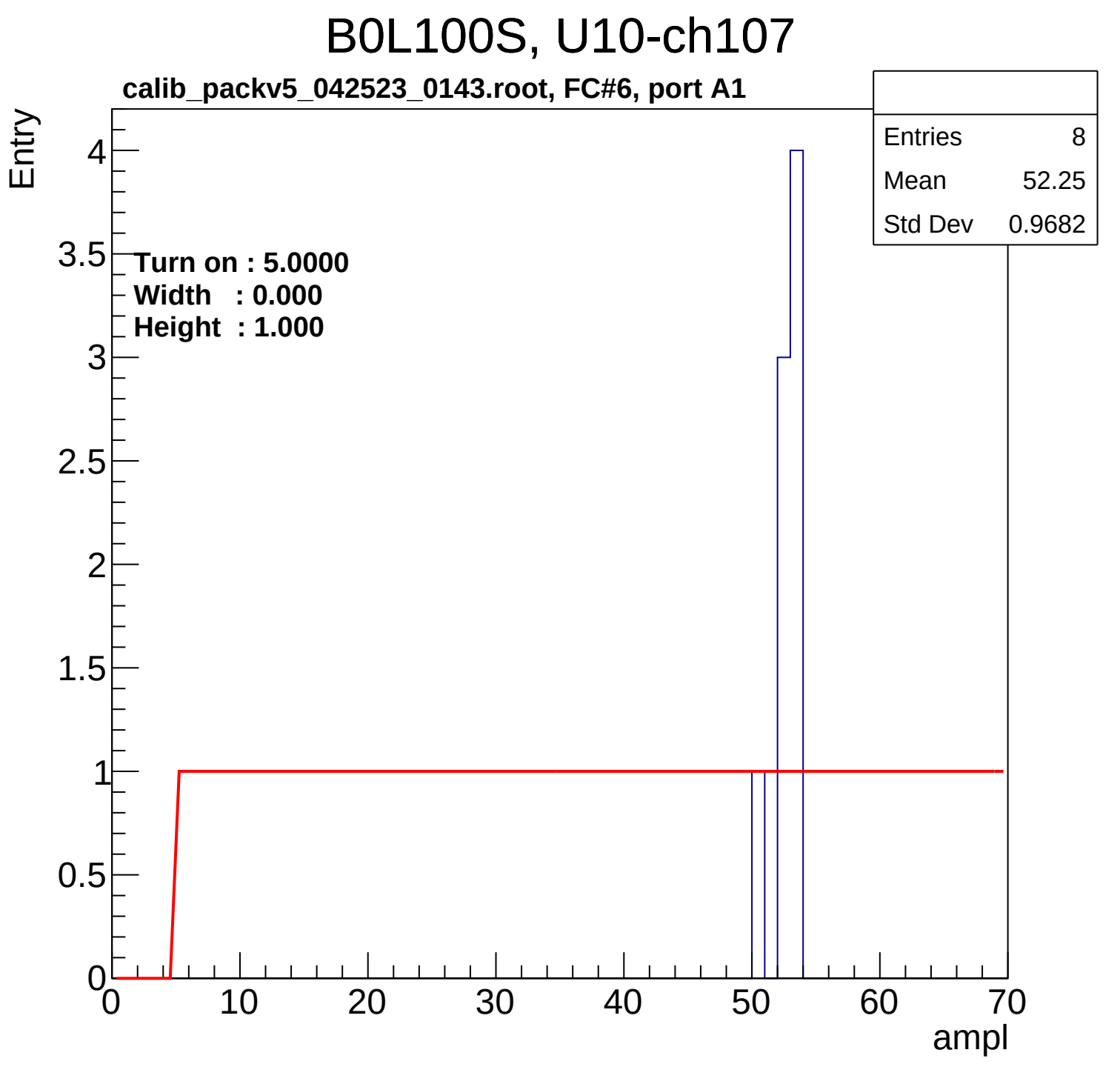
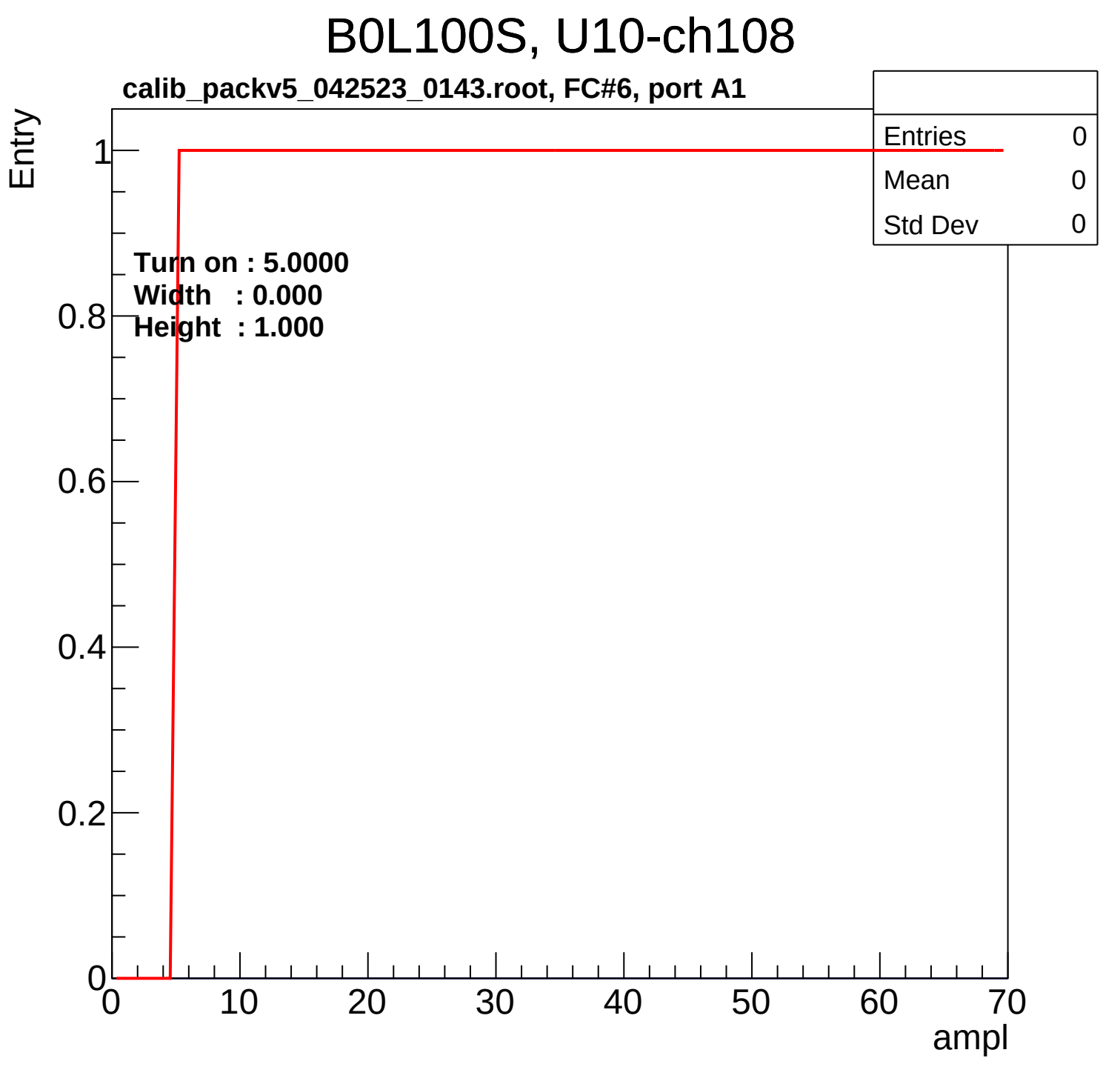
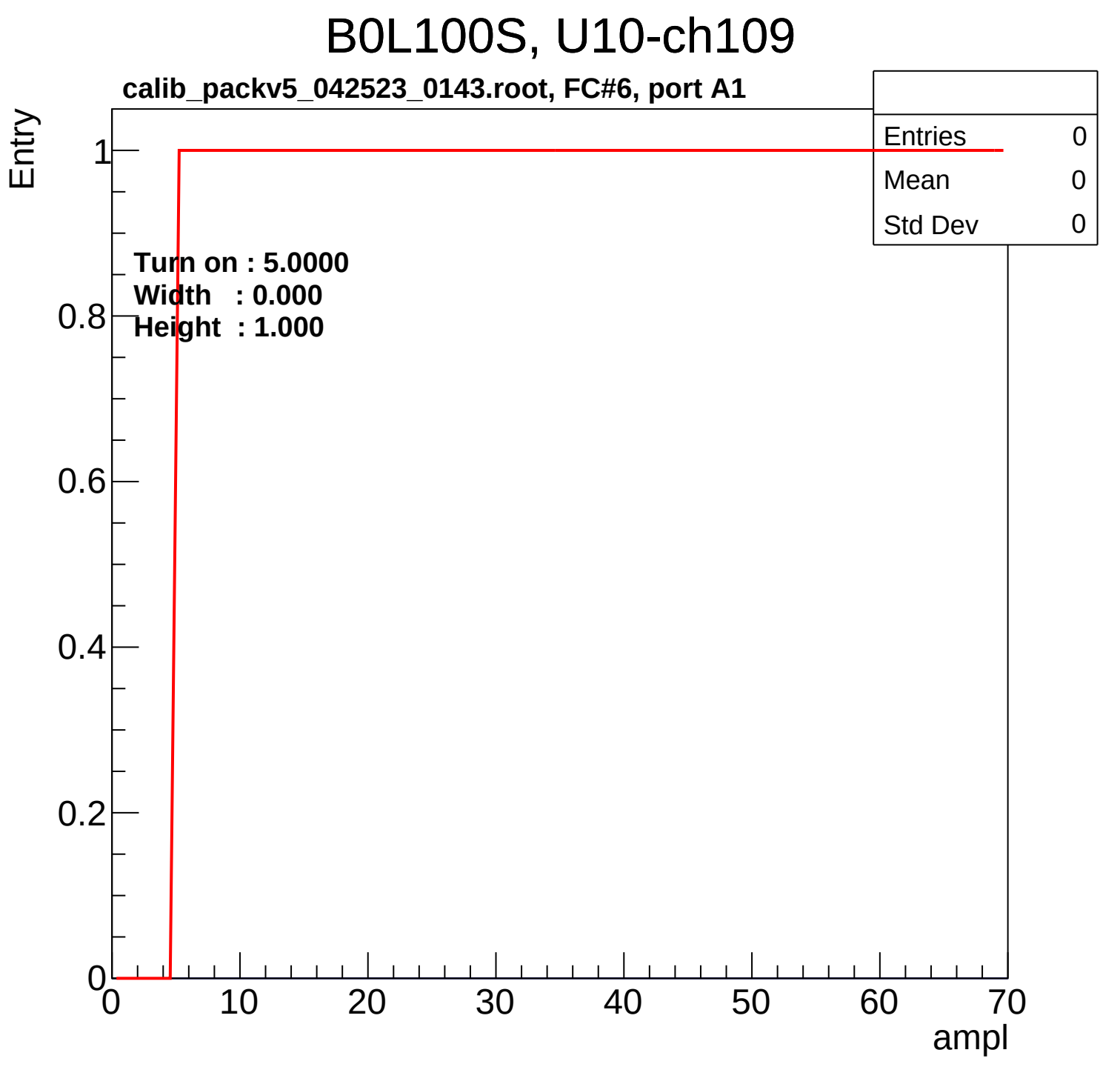

B0L100S, U10-ch107
calib_packv5_042523_0143.root, FC#6, port A1
Entries 8
Mean 52.25
Std Dev 0.9682
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B0L100S, U10-ch108
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U10-ch109
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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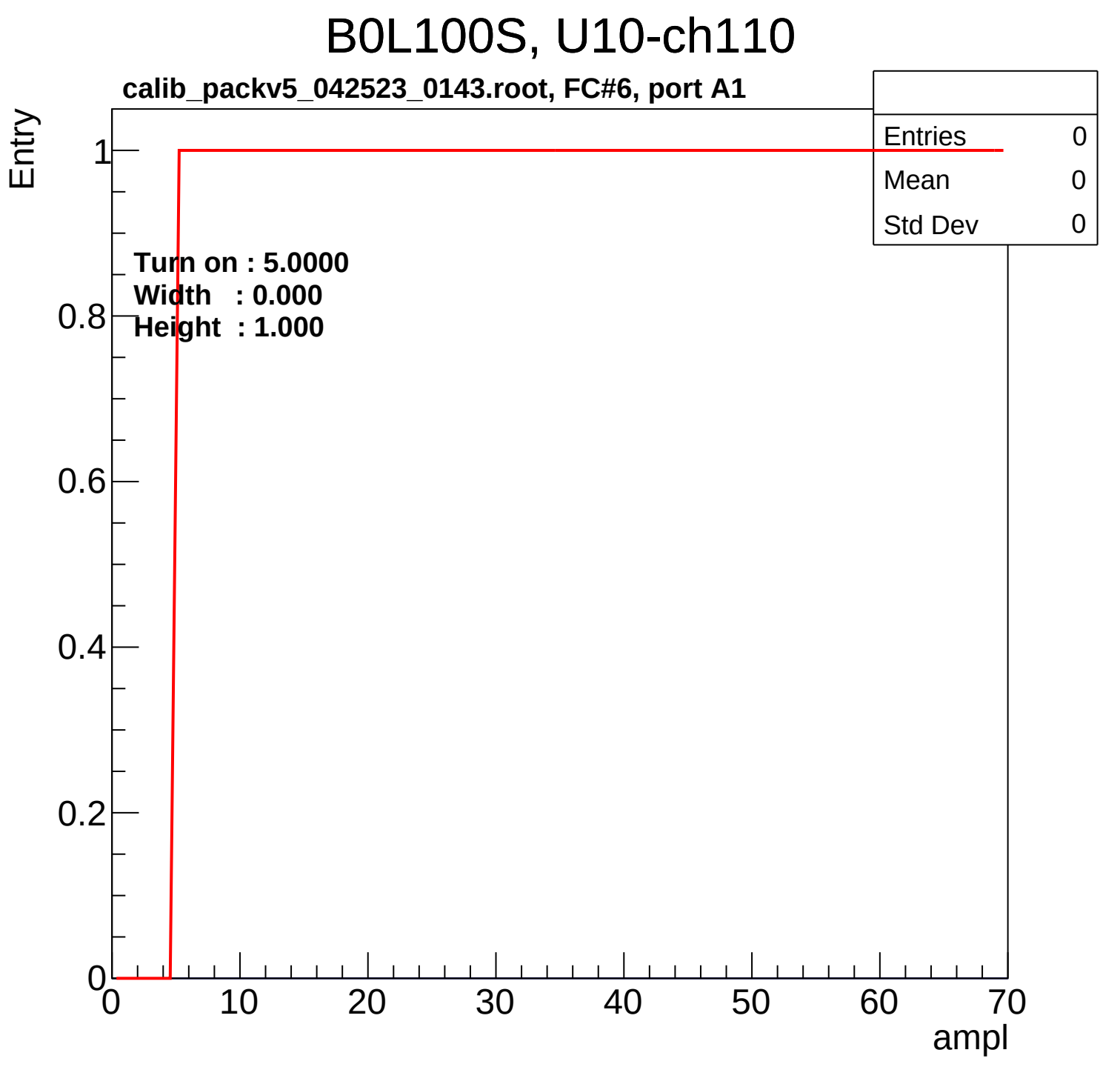
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U10-ch110
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.8
0.6
0.4
0.2
0
0
10
20
30
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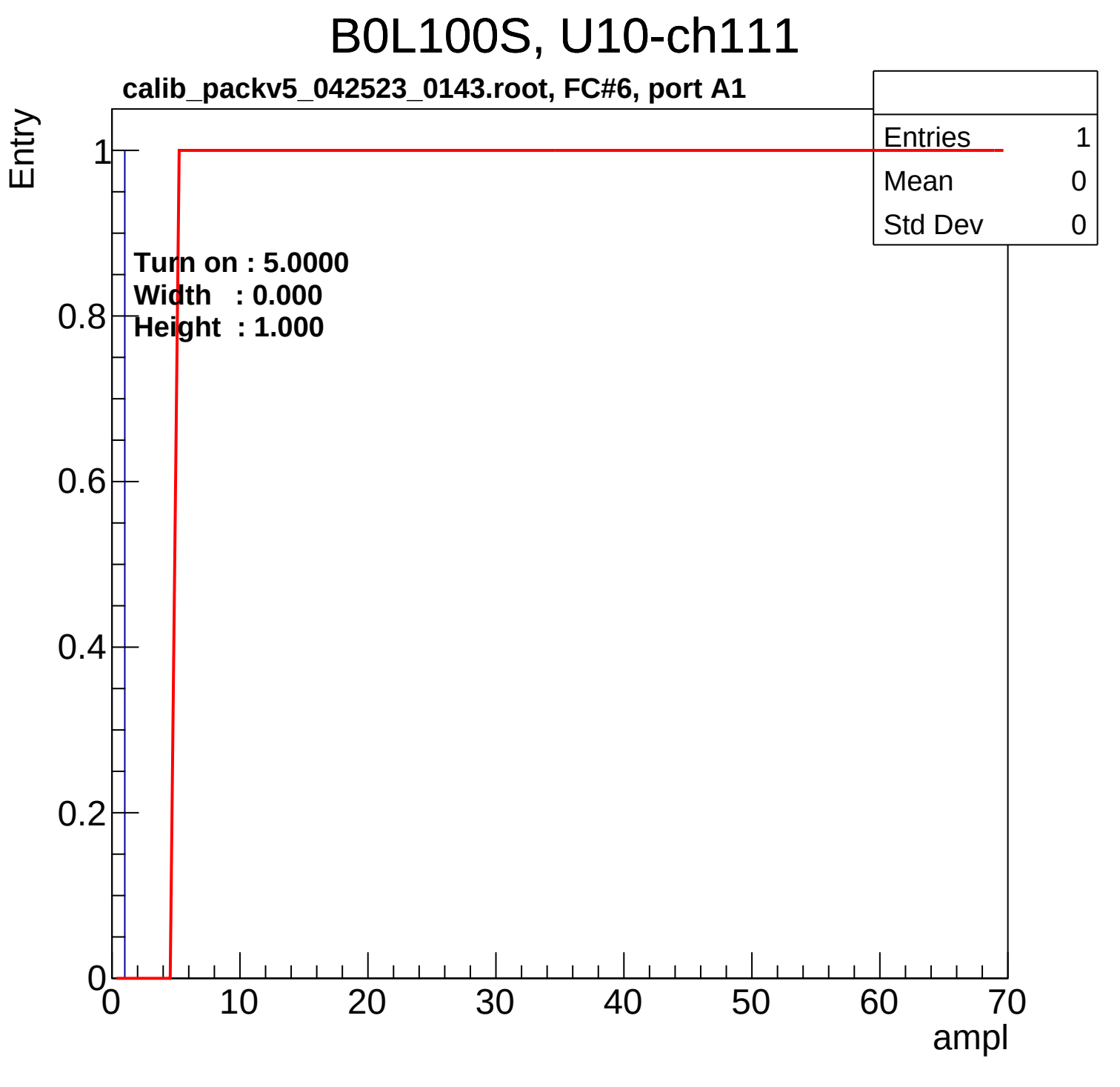
50
60
70
ampl


B0L100S, U10-ch111
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
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20
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40
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60
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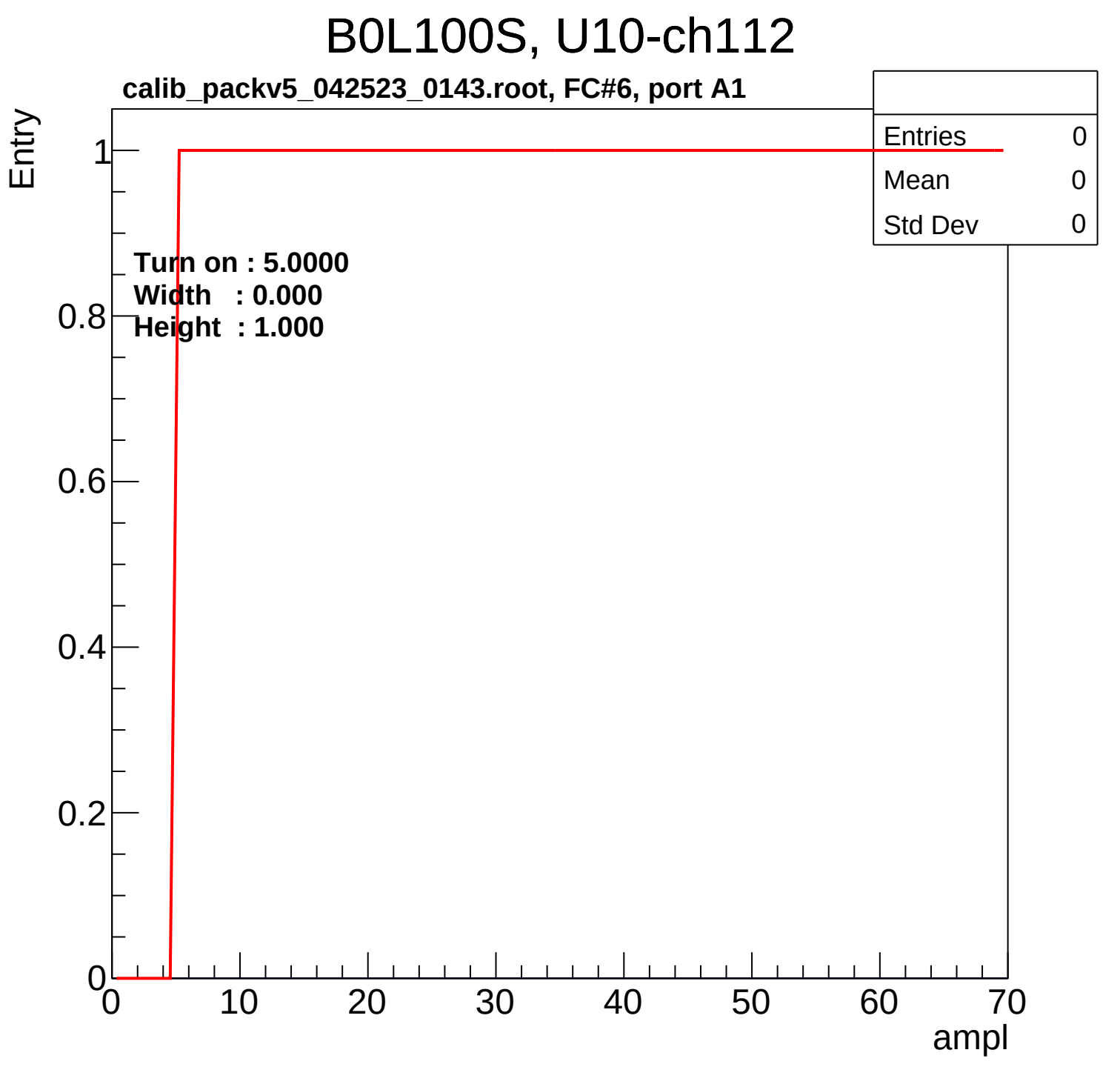
B0L100S, U10-ch112
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
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40
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60
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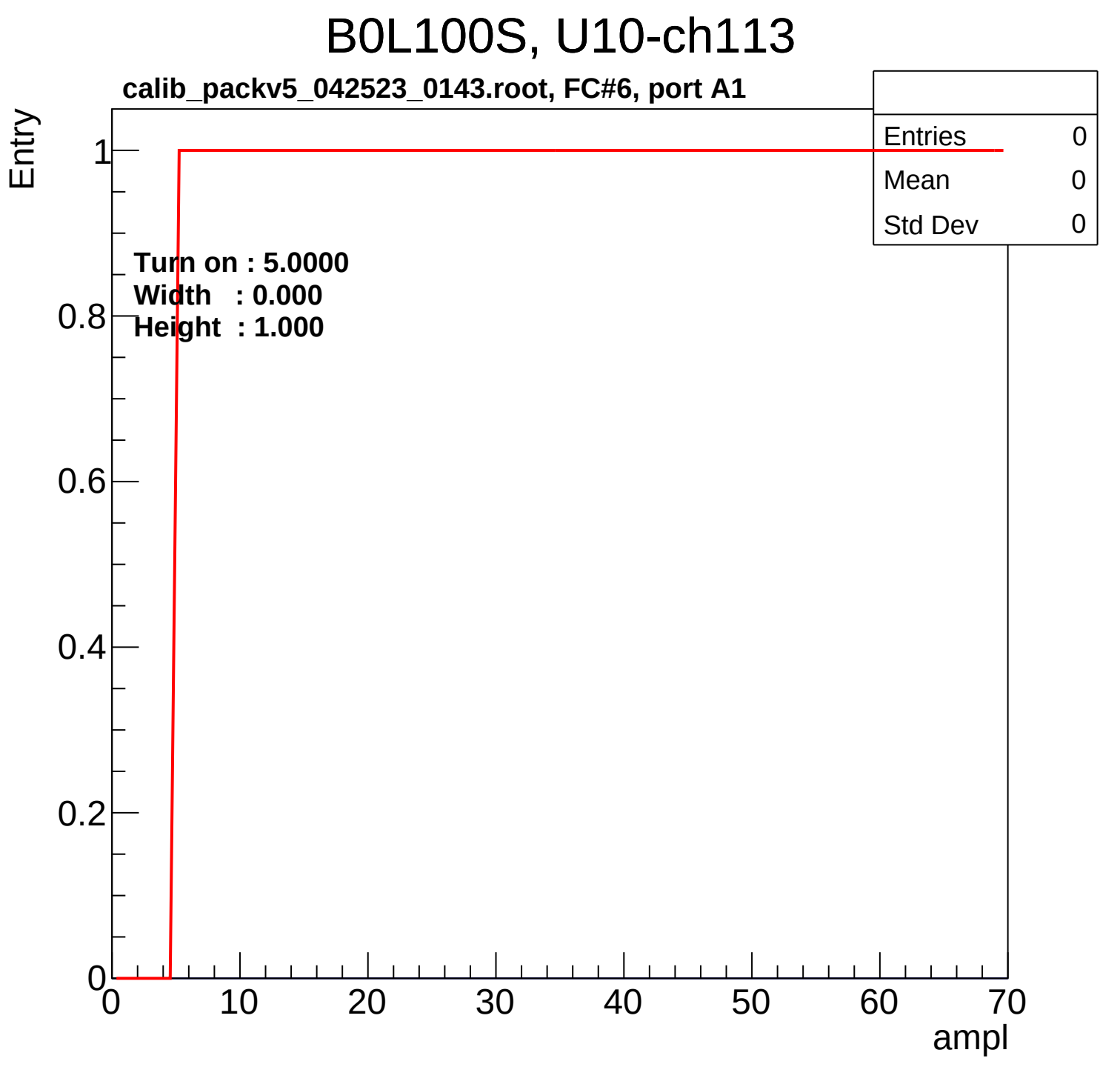
B0L100S, U10-ch113
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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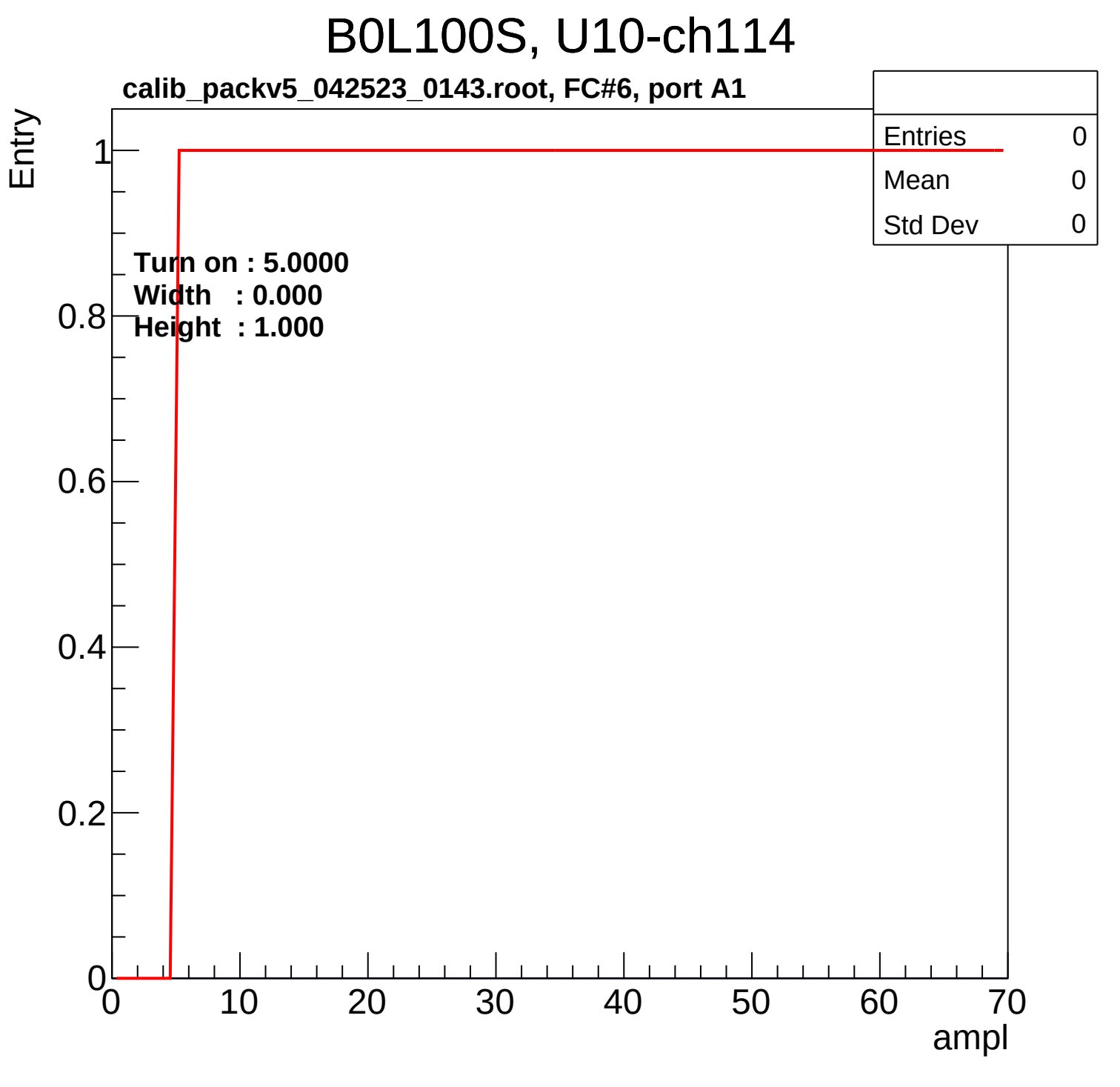
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U10-ch114
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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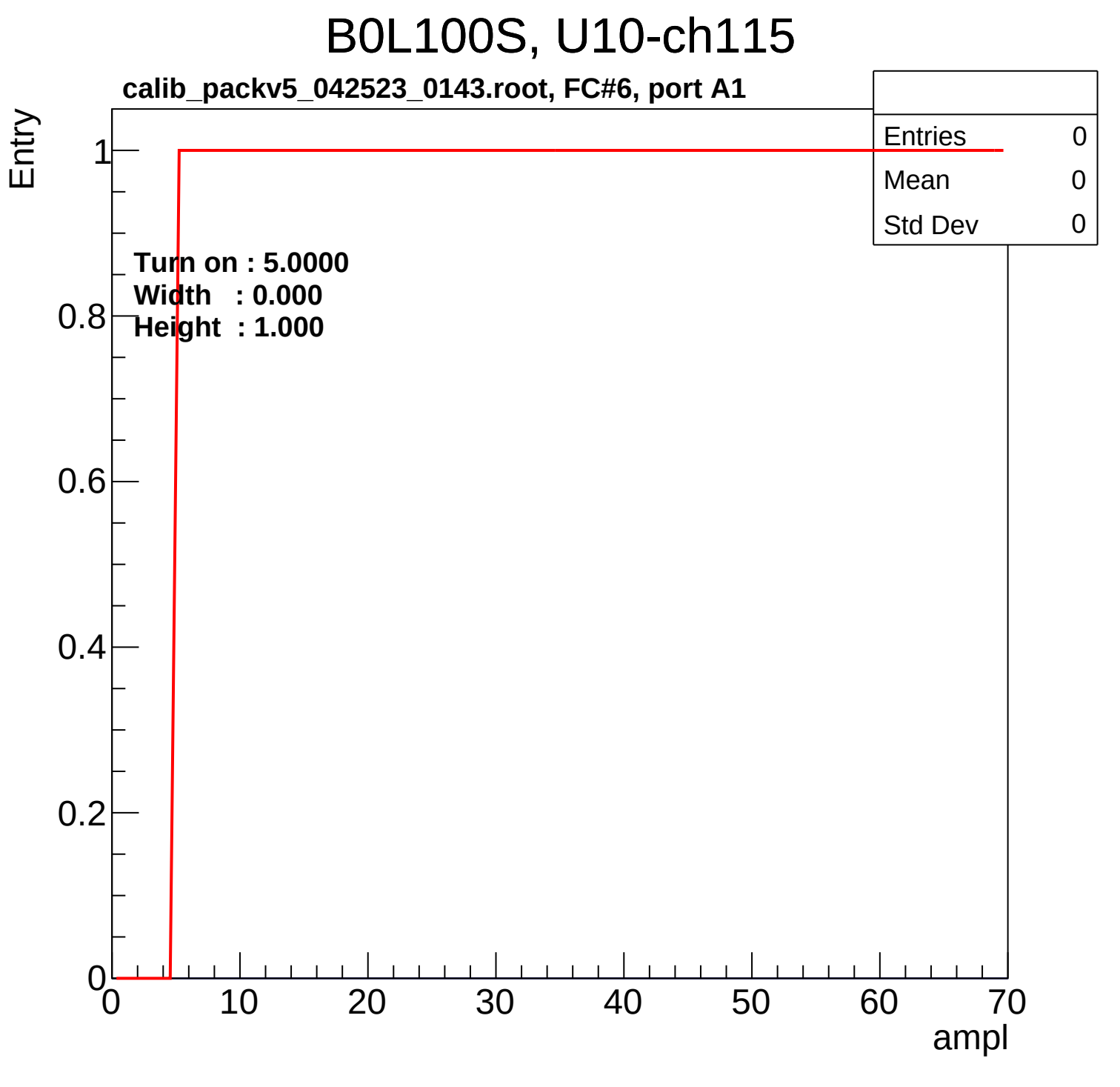
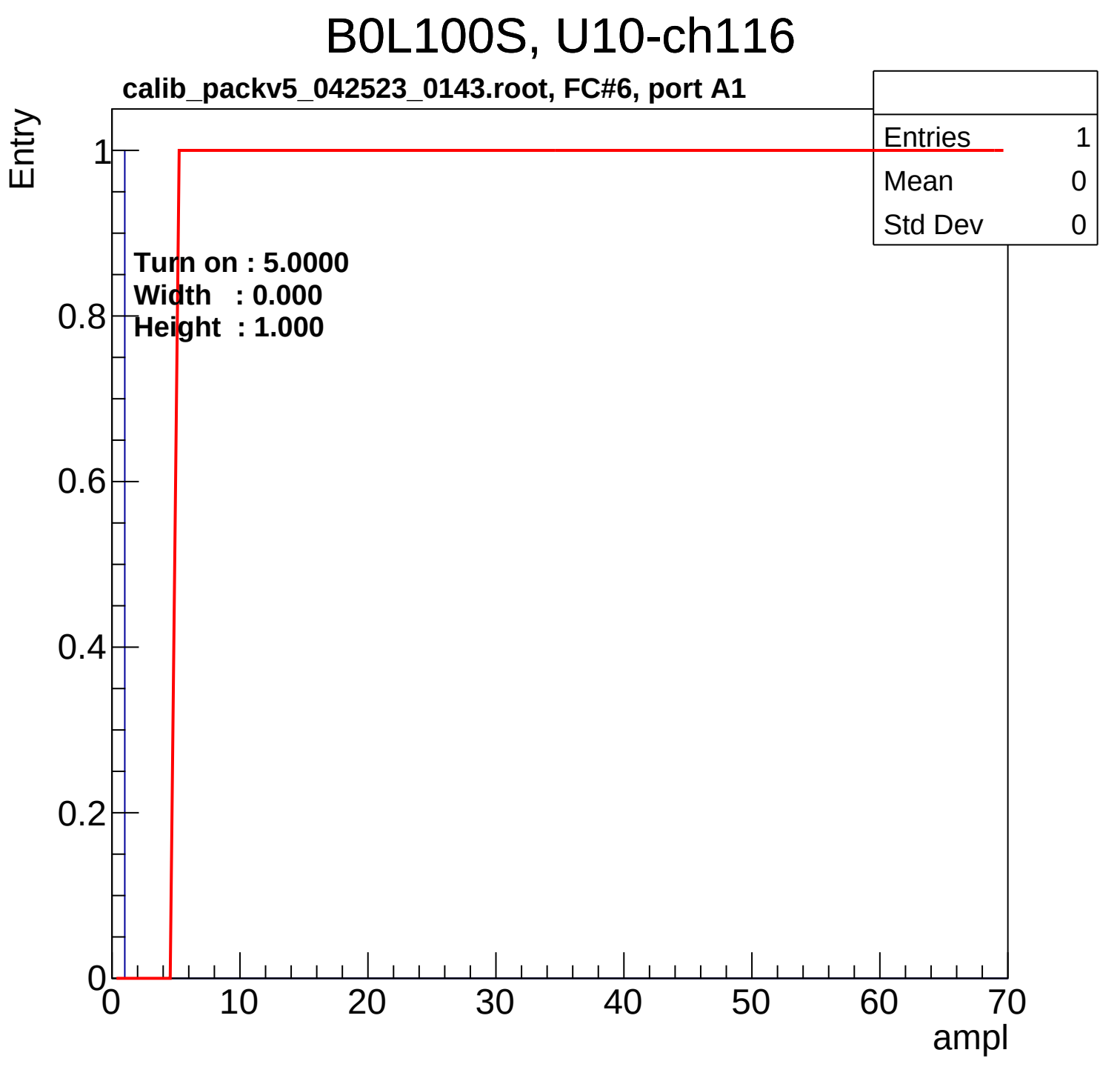
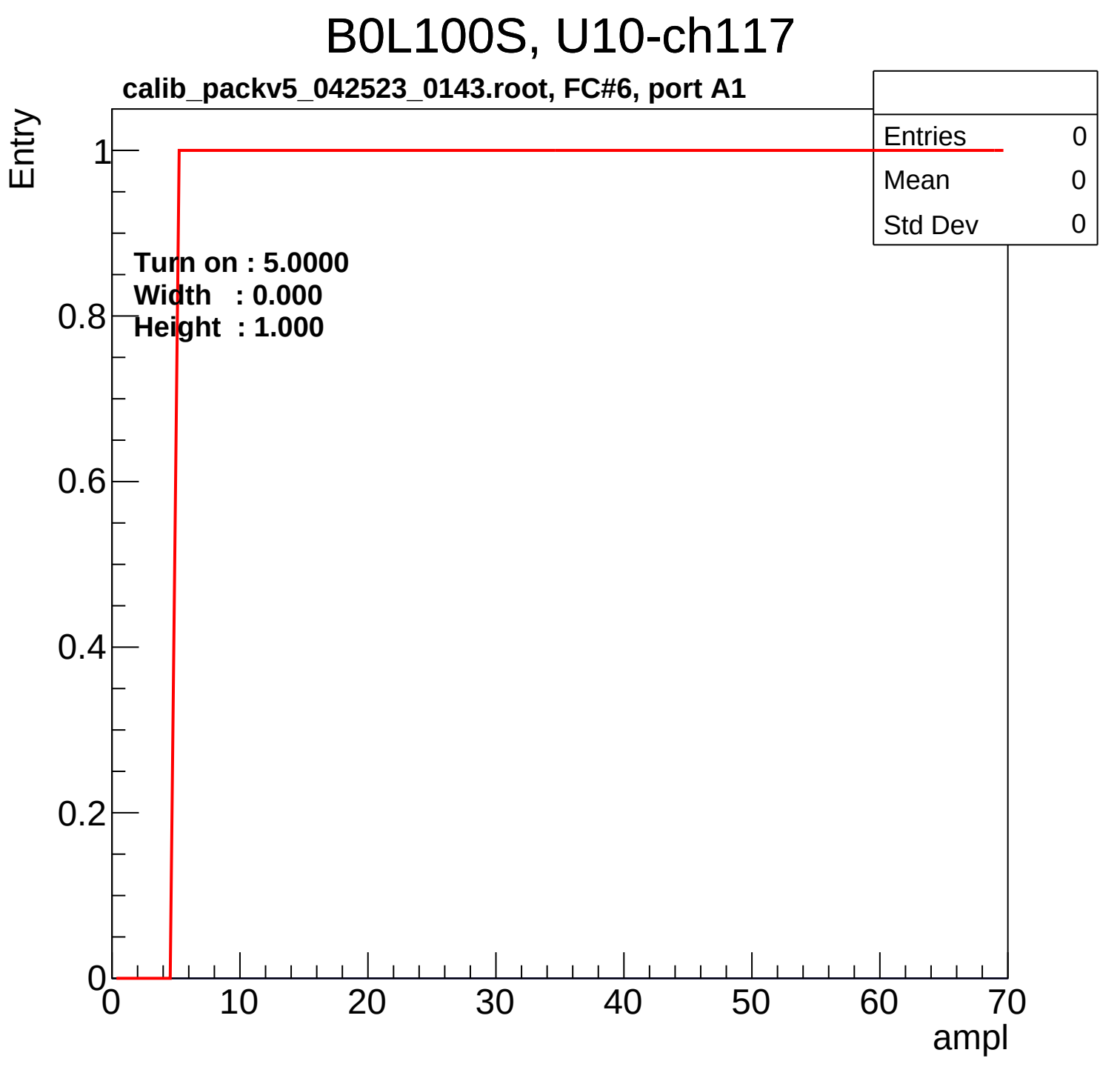
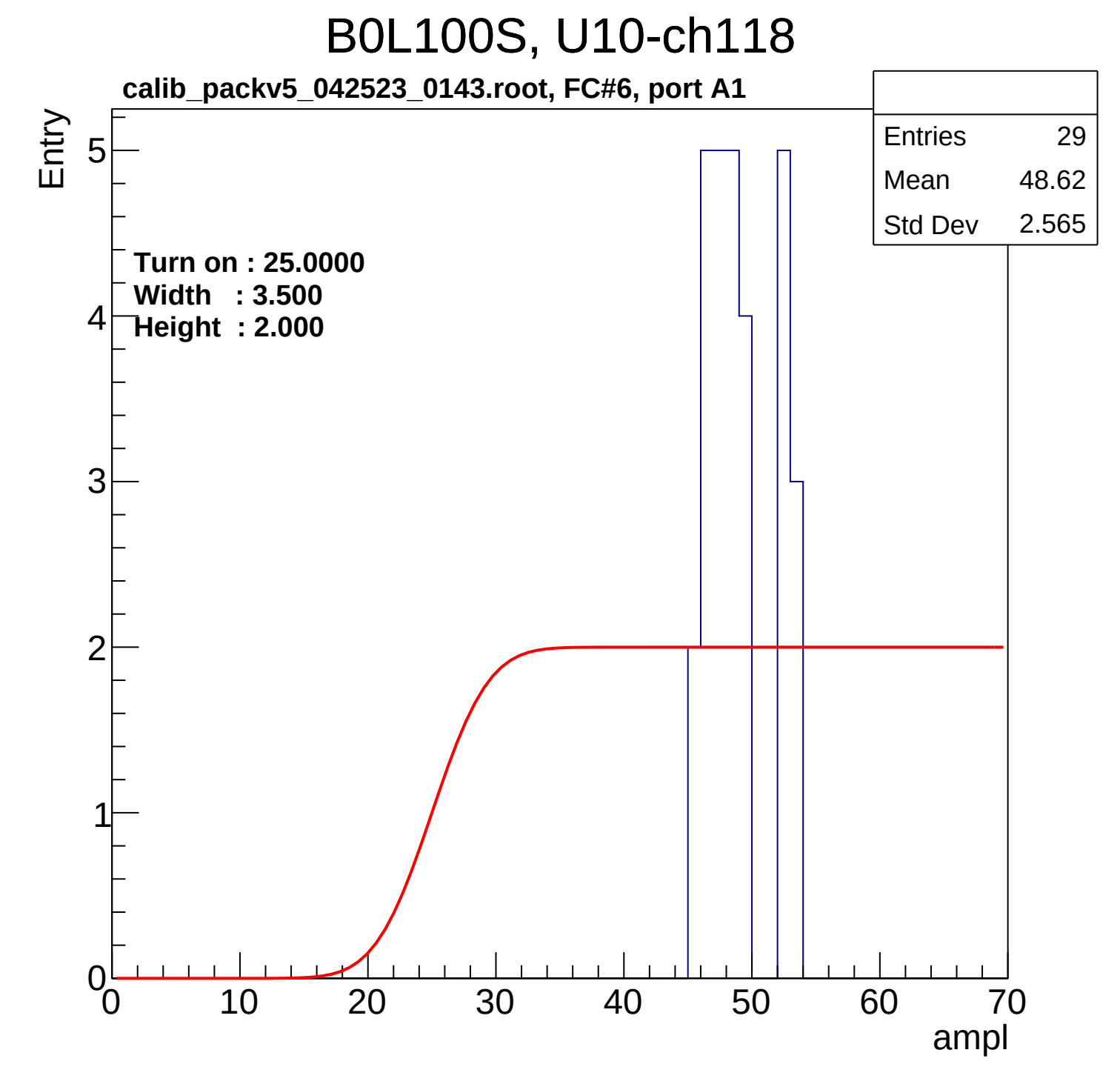
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U10-ch115
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U10-ch116
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U10-ch117
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U10-ch118
calib_packv5_042523_0143.root, FC#6, port A1
Entries 29
Mean 48.62
Std Dev 2.565
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
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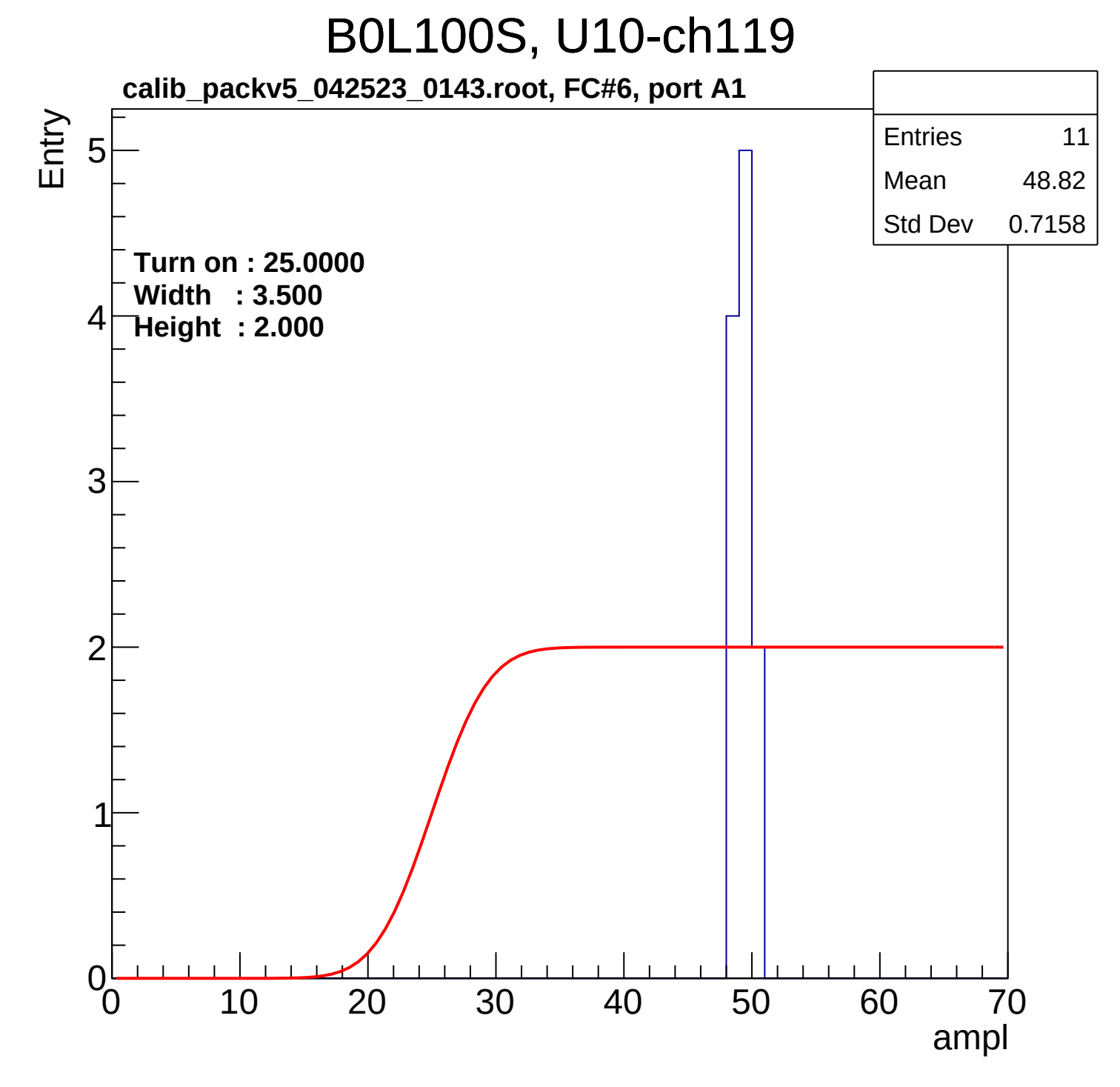
B0L100S, U10-ch119
calib_packv5_042523_0143.root, FC#6, port A1
Entries 11
Mean 48.82
Std Dev 0.7158
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
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1
2
3
4
5
0
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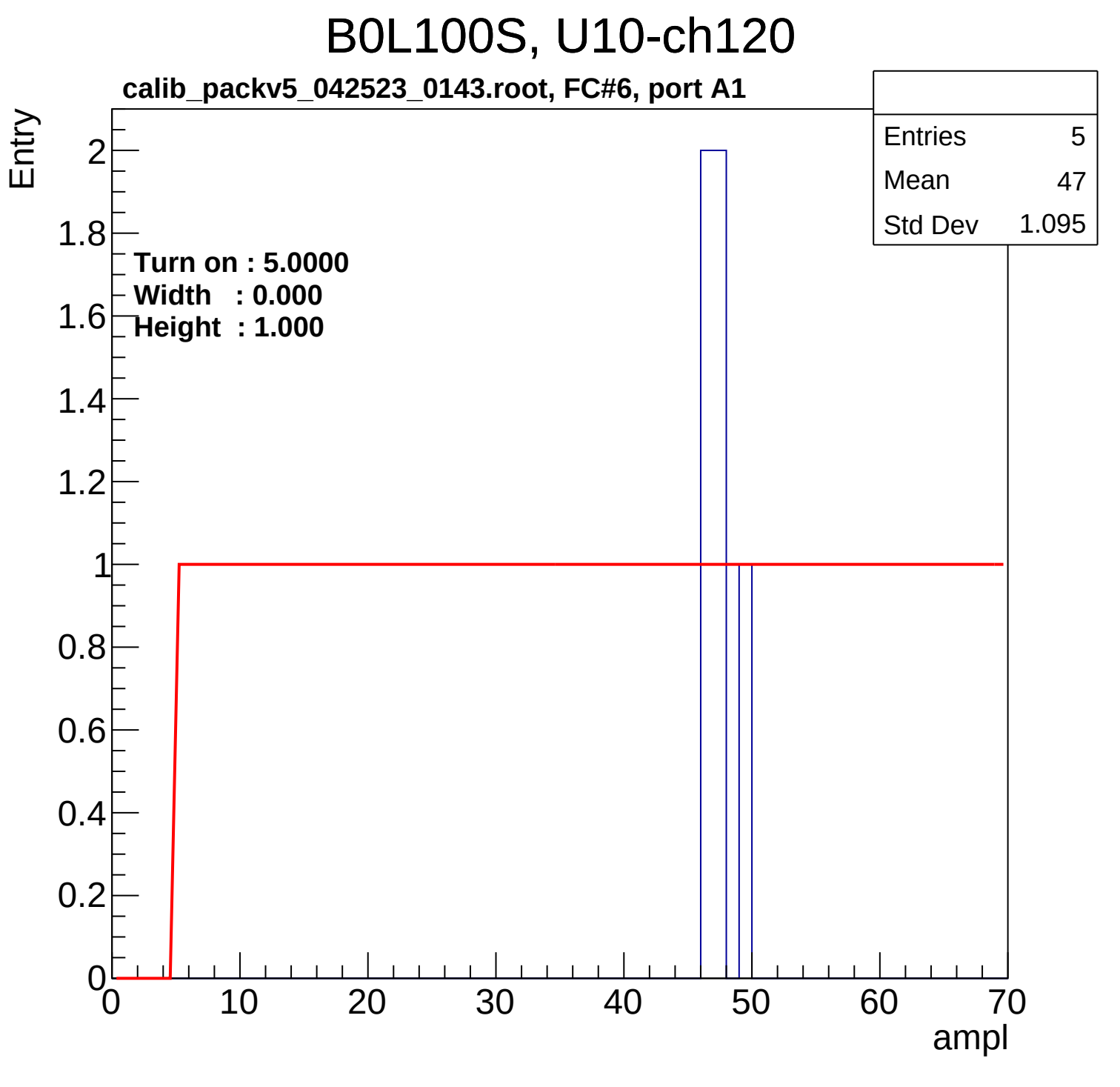
B0L100S, U10-ch120
calib_packv5_042523_0143.root, FC#6, port A1
Entries 5
Mean 47
Std Dev 1.095
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
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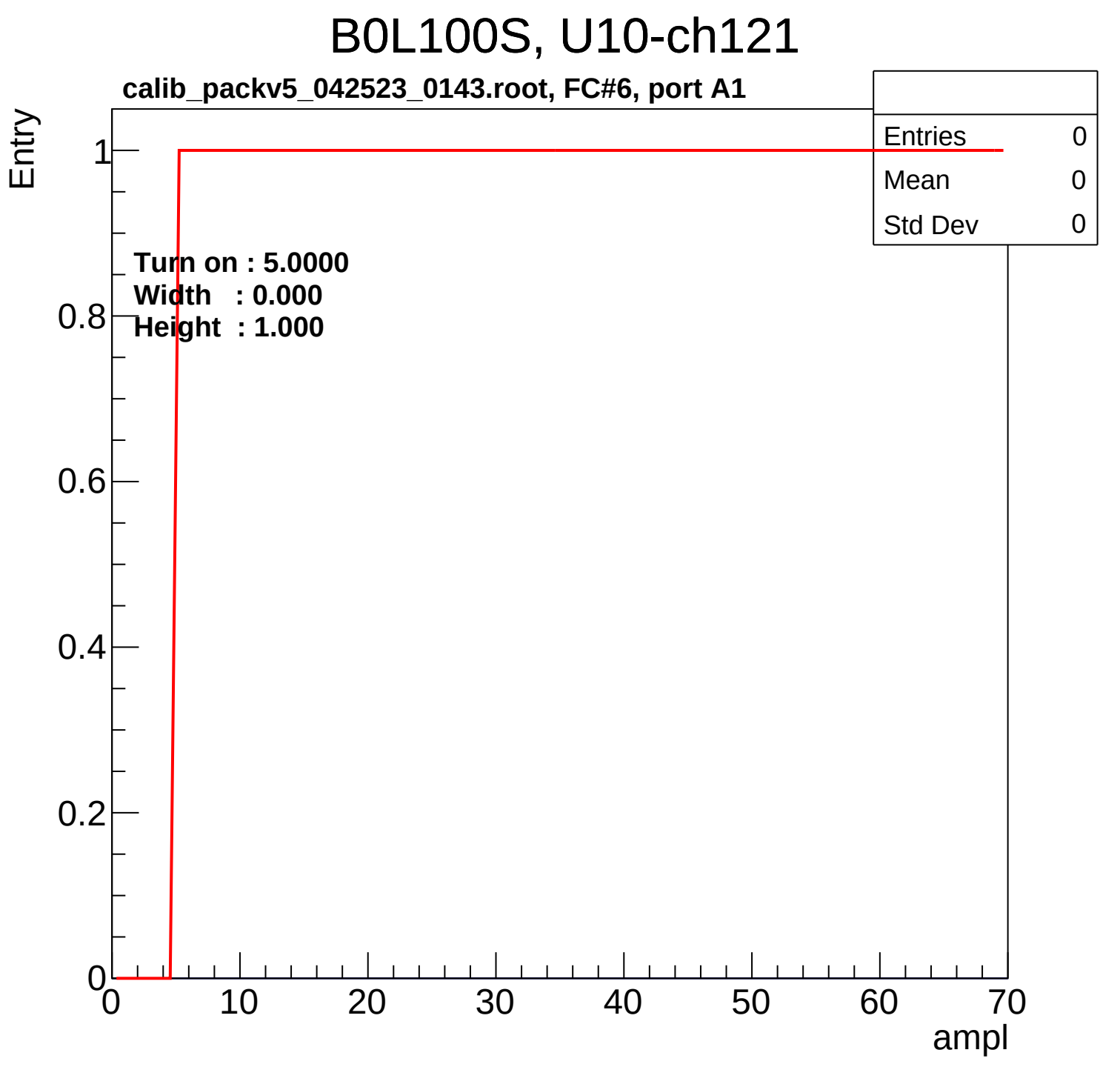
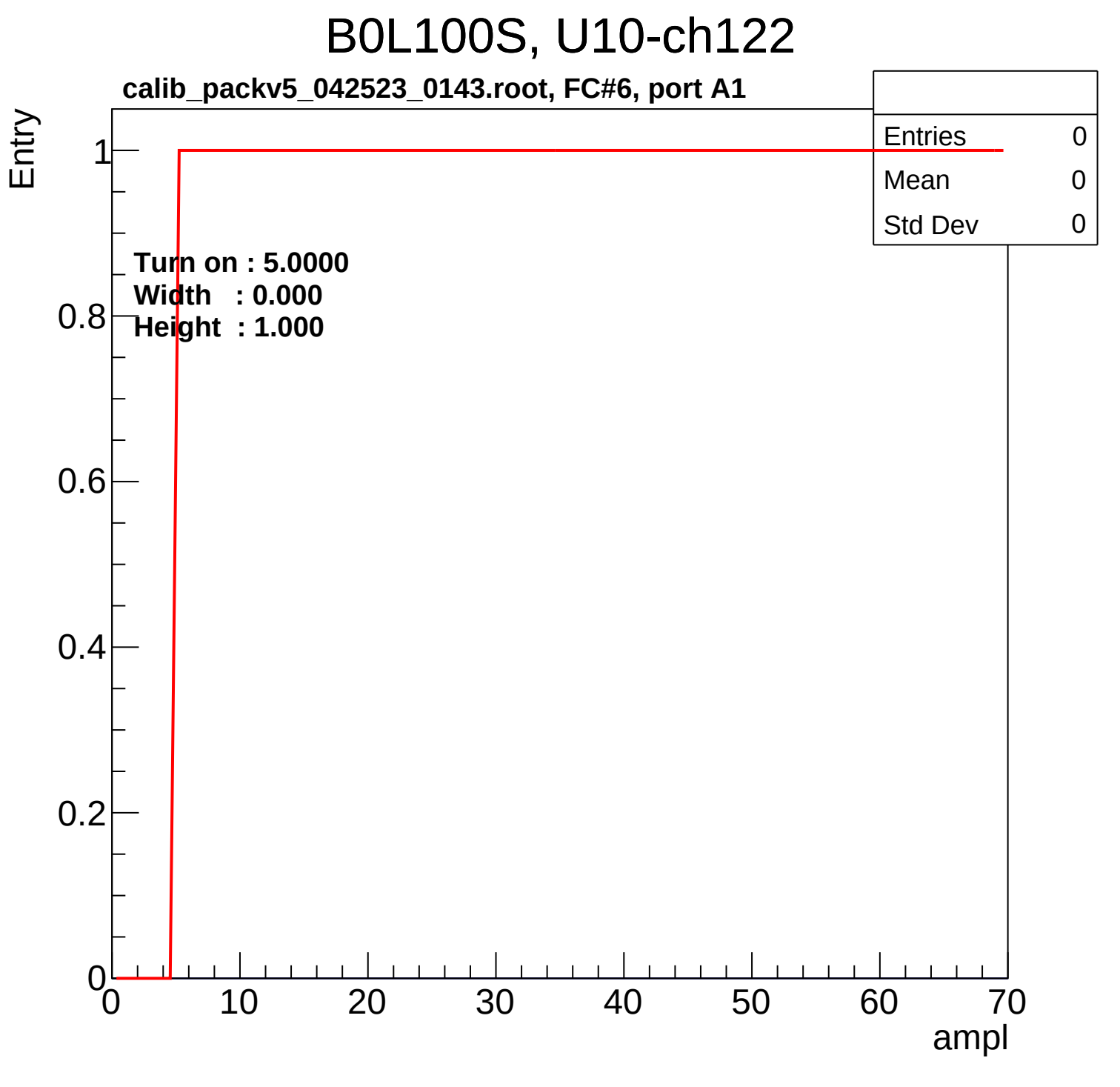
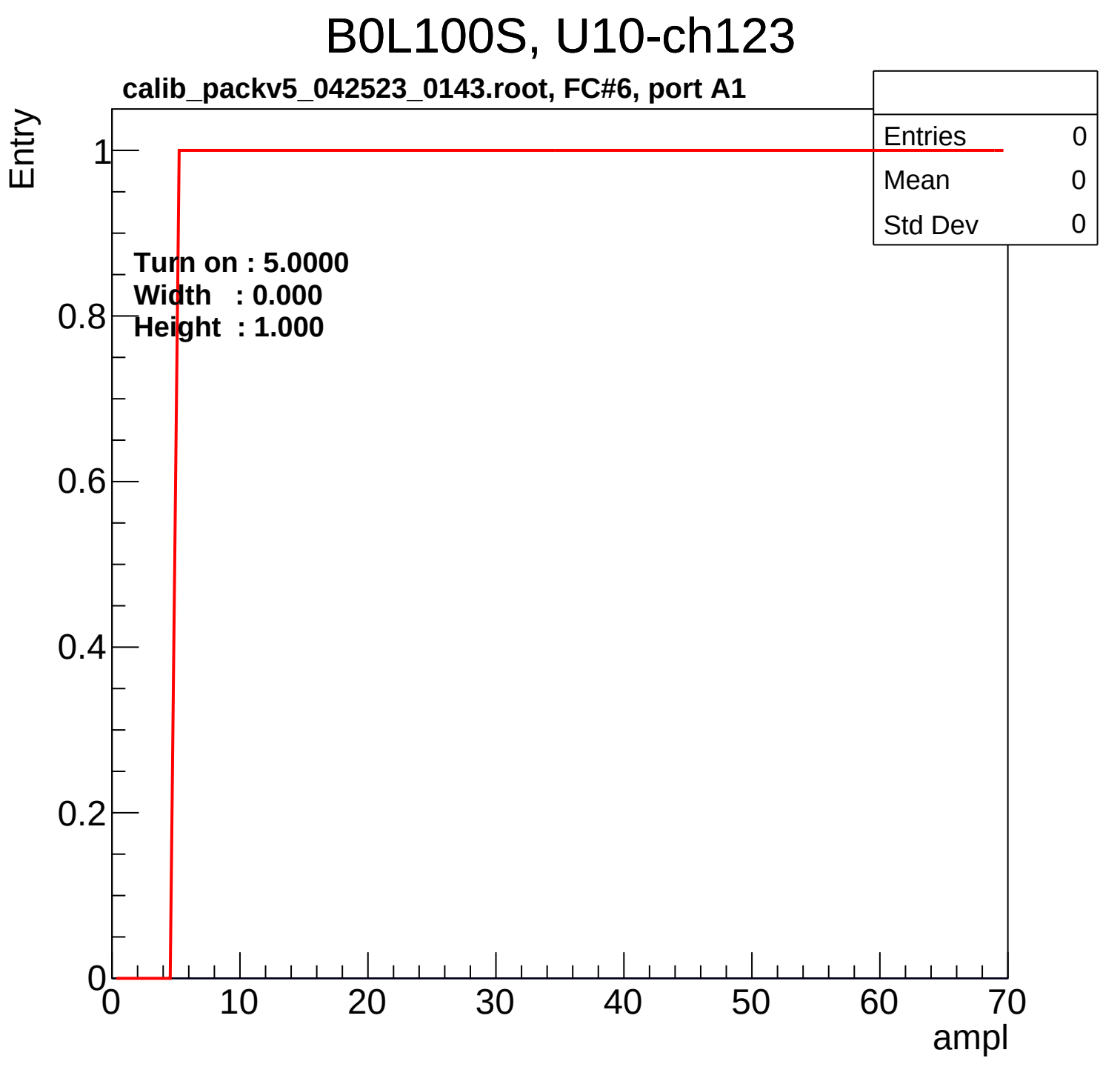
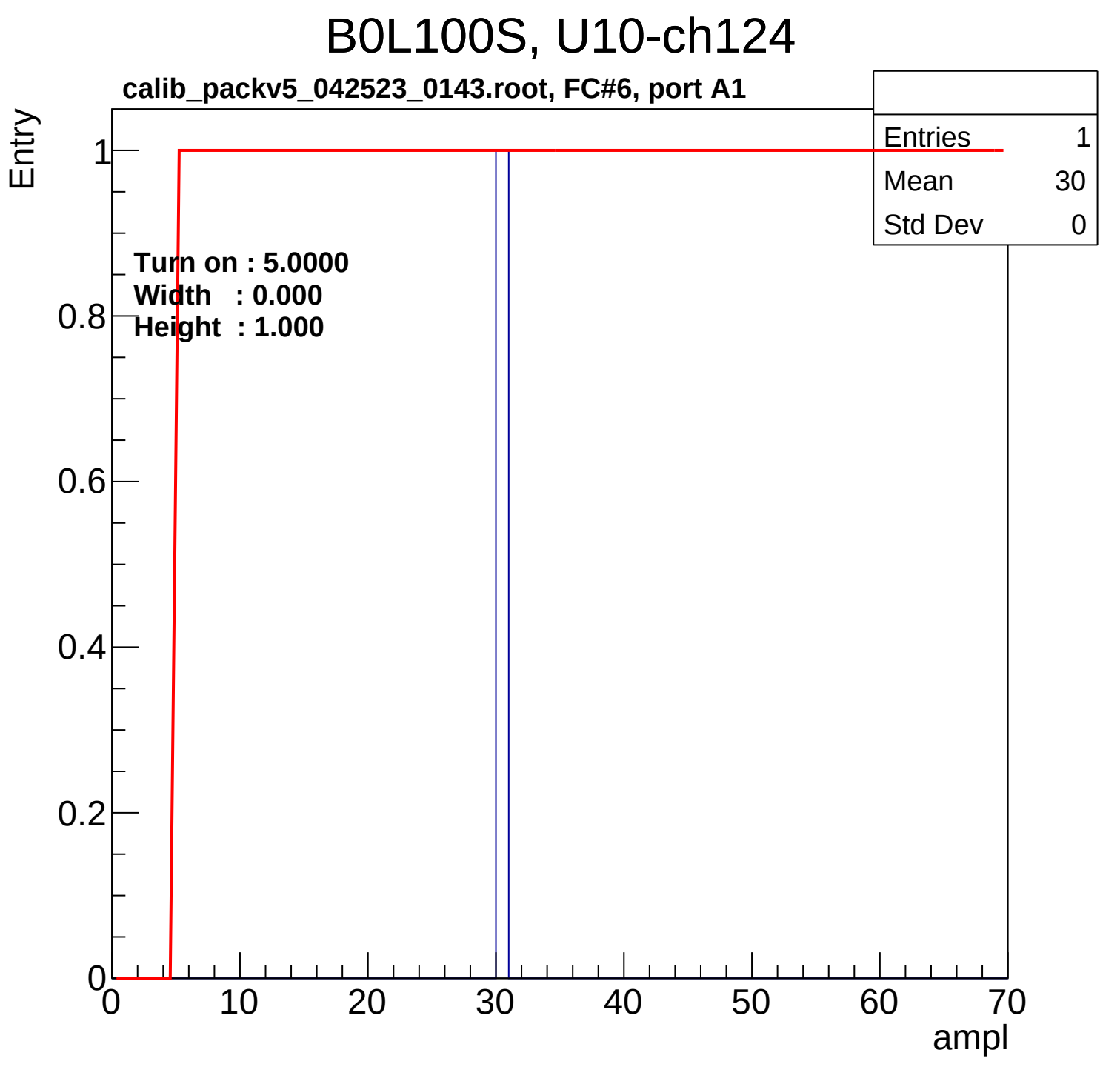
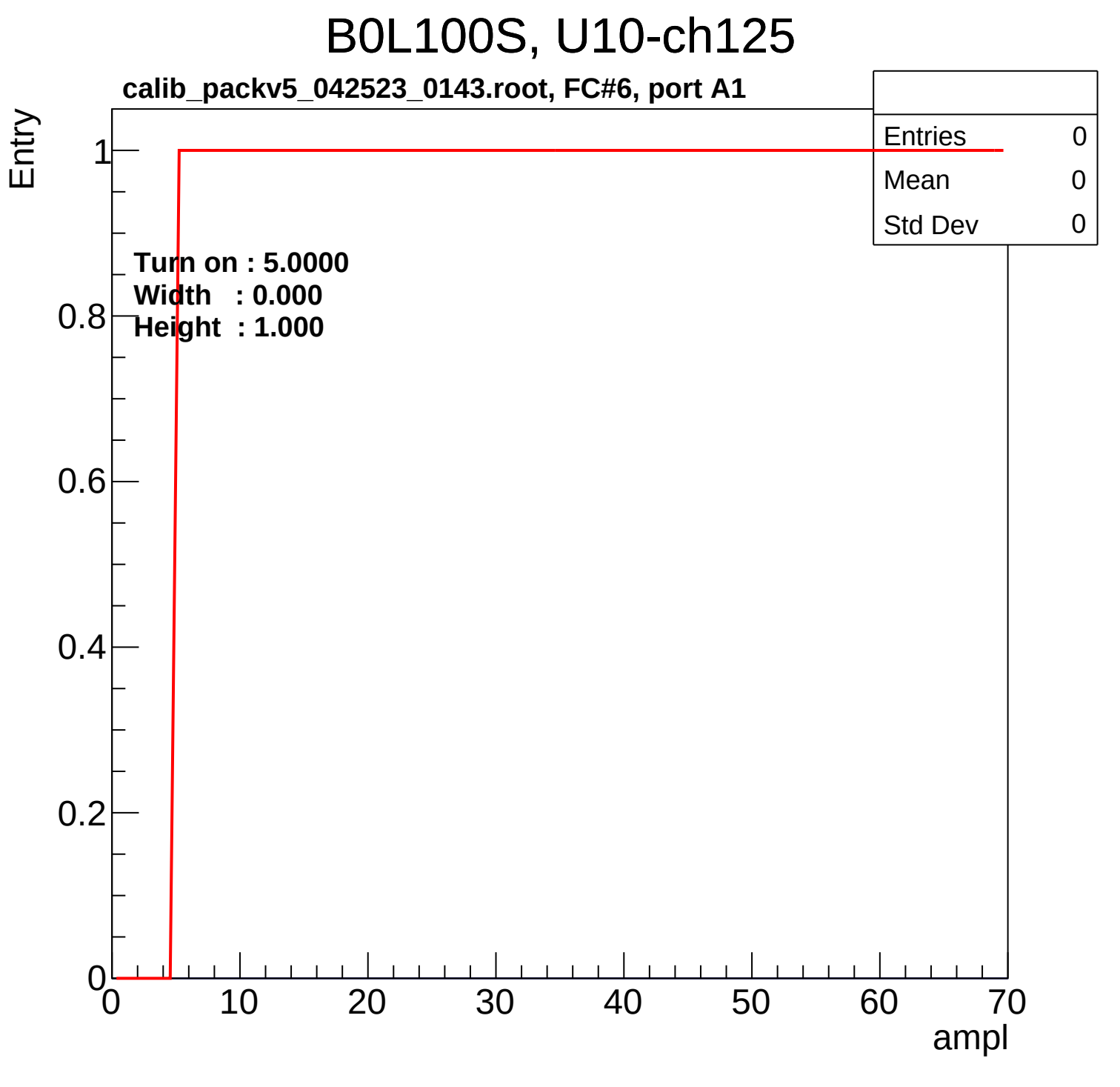
60
70

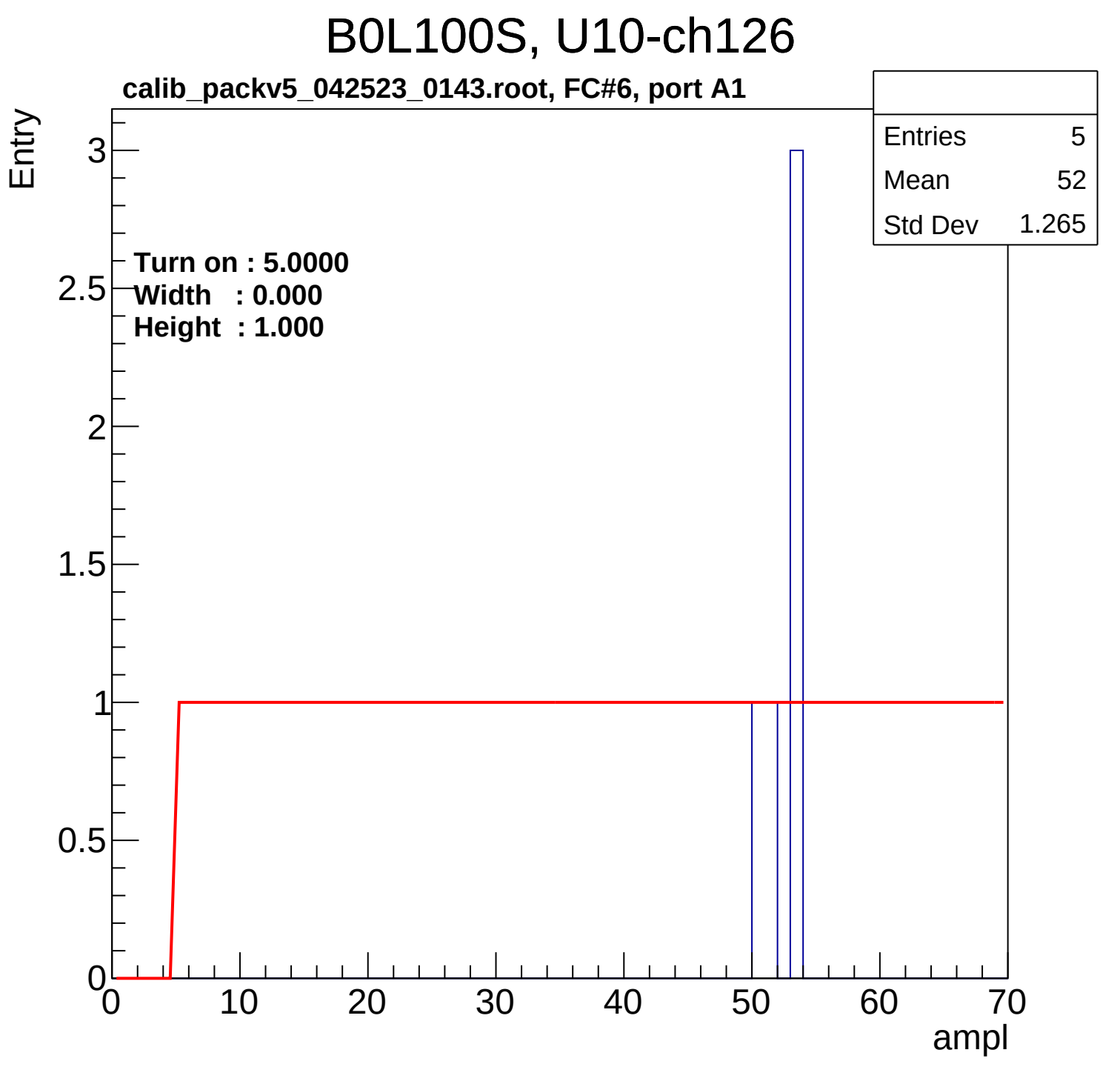

B0L100S, U10-ch121
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

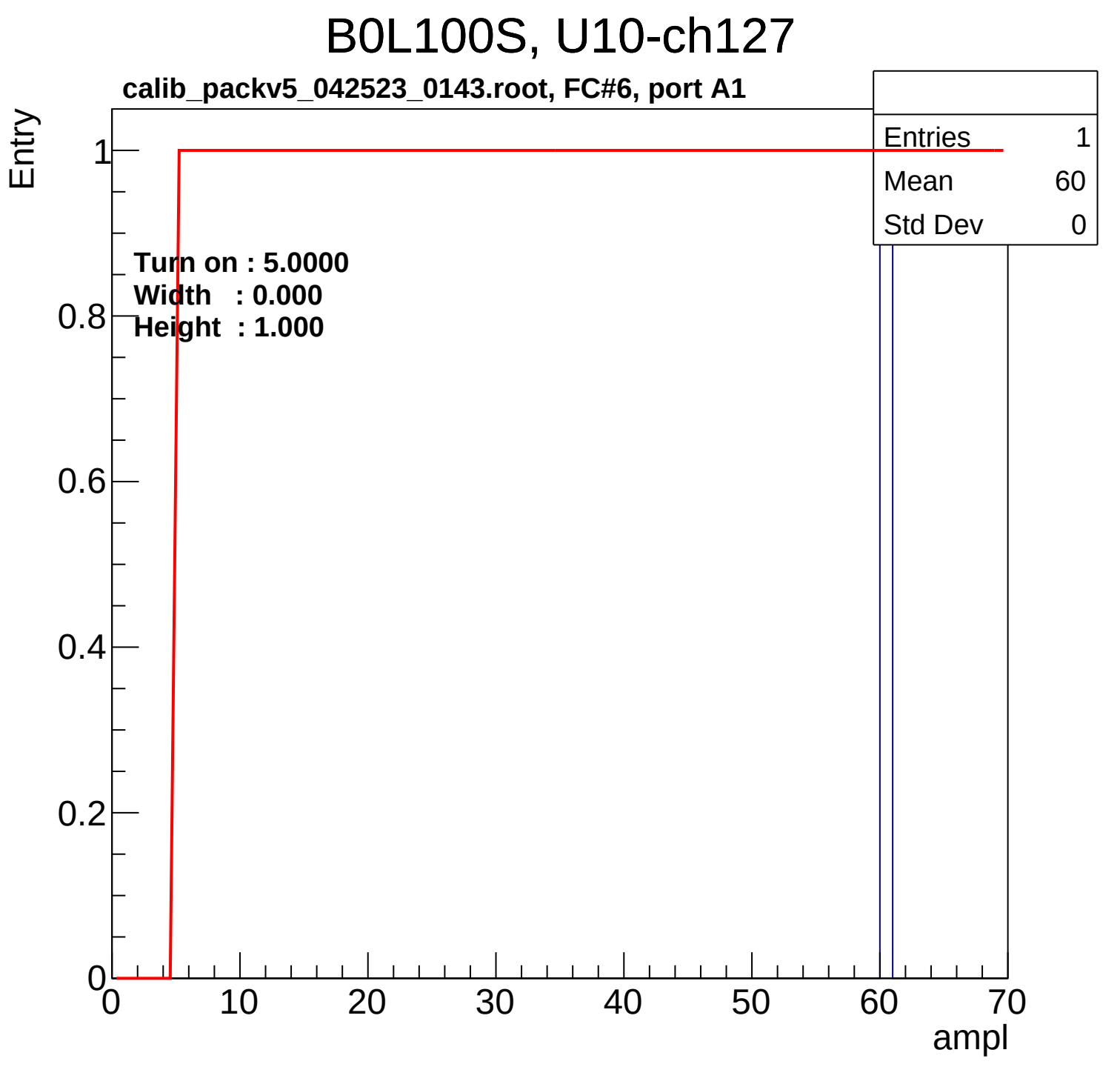

B0L100S, U10-ch122
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

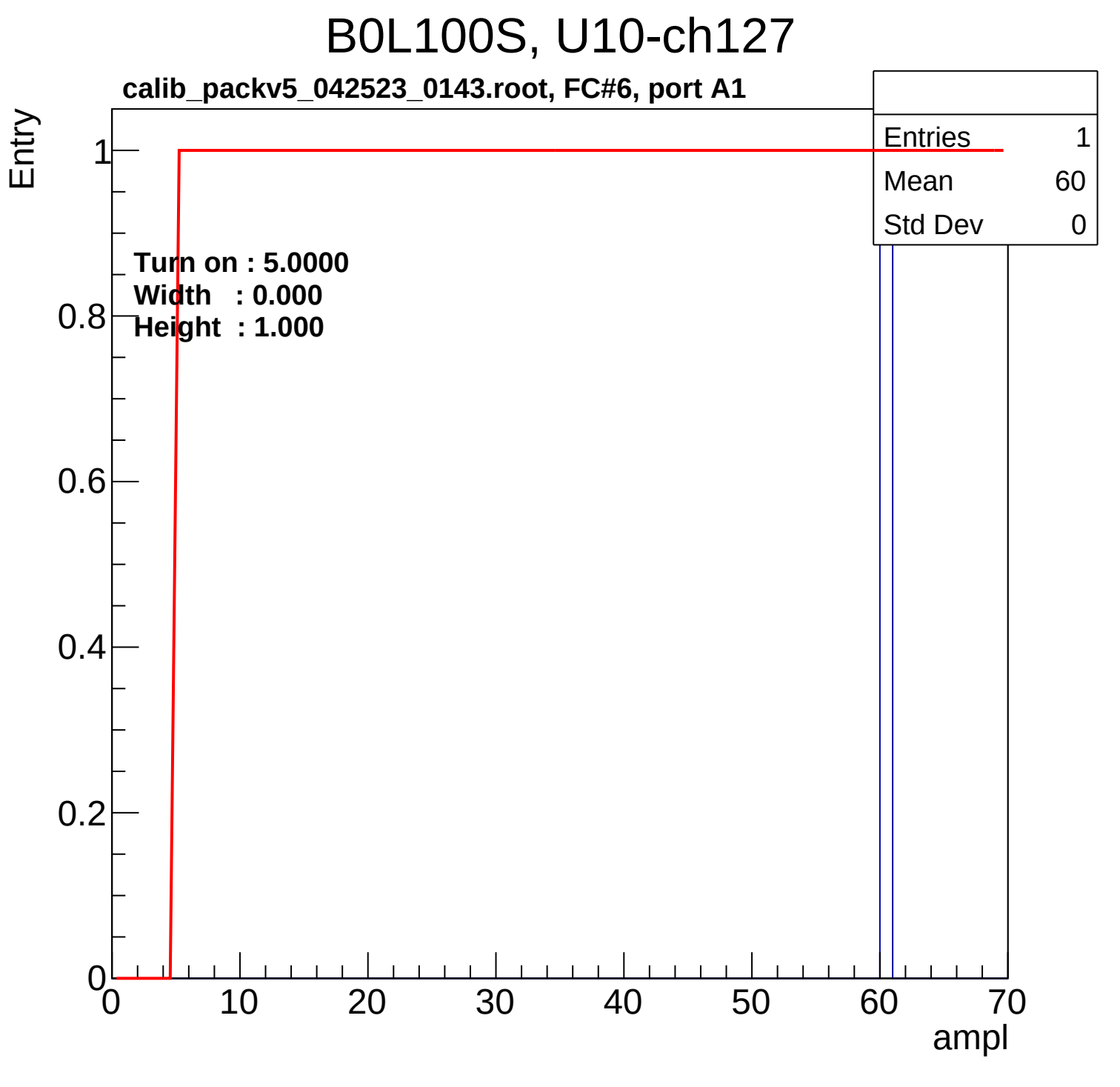

B0L100S, U10-ch123
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U10-ch124
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 30
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U10-ch125
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U10-ch126
calib_packv5_042523_0143.root, FC#6, port A1
Entries 5
Mean 52
Std Dev 1.265
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B0L100S, U10-ch127
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 60
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U10-ch127
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 60
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70