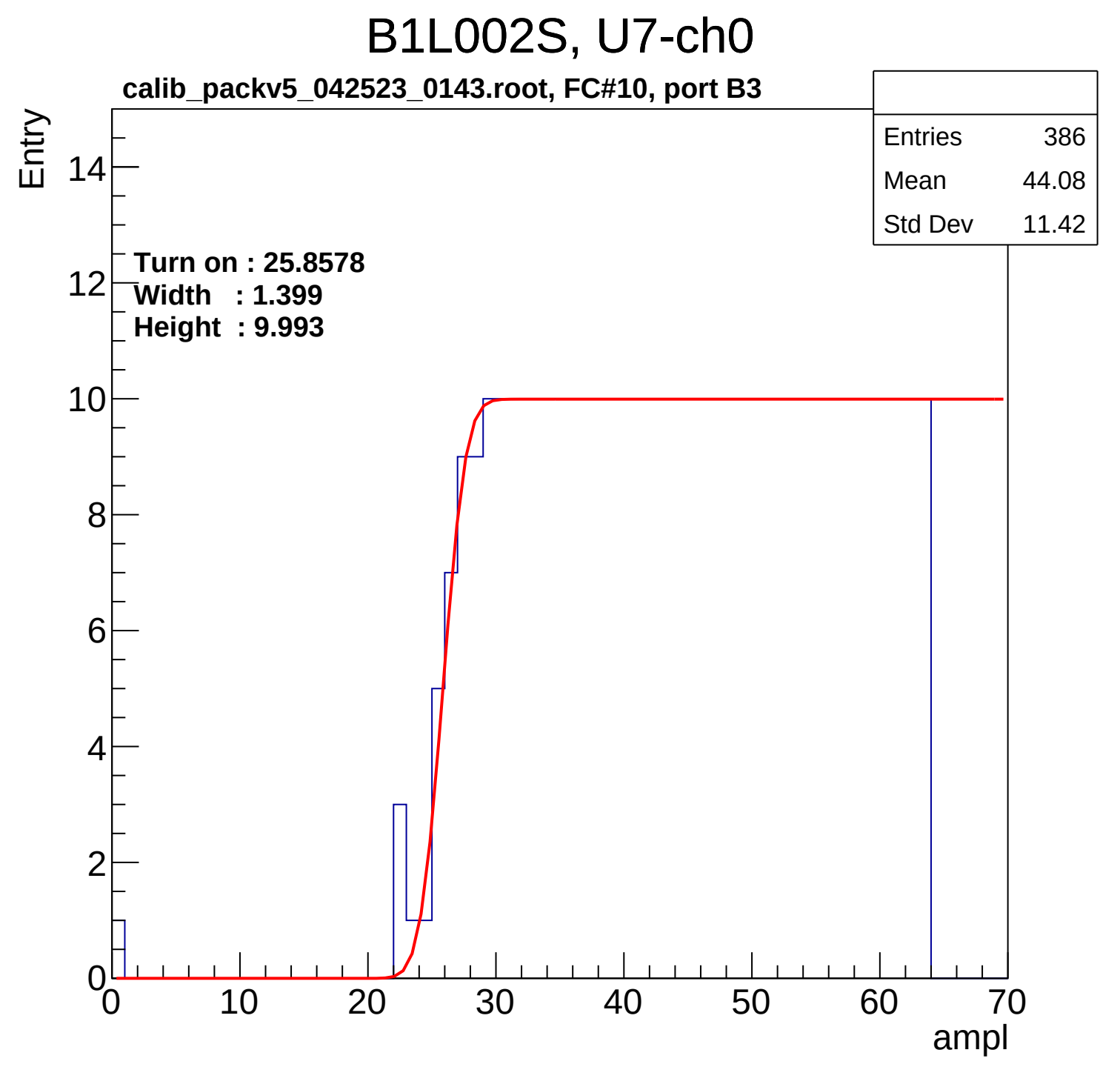
B1L002S, U7-ch0
calib_packv5_042523_0143.root, FC#10, port B3
Entries 386
Mean 44.08
Std Dev 11.42
Turn on : 25.8578
Width : 1.399
Height : 9.993
Entry
ampl
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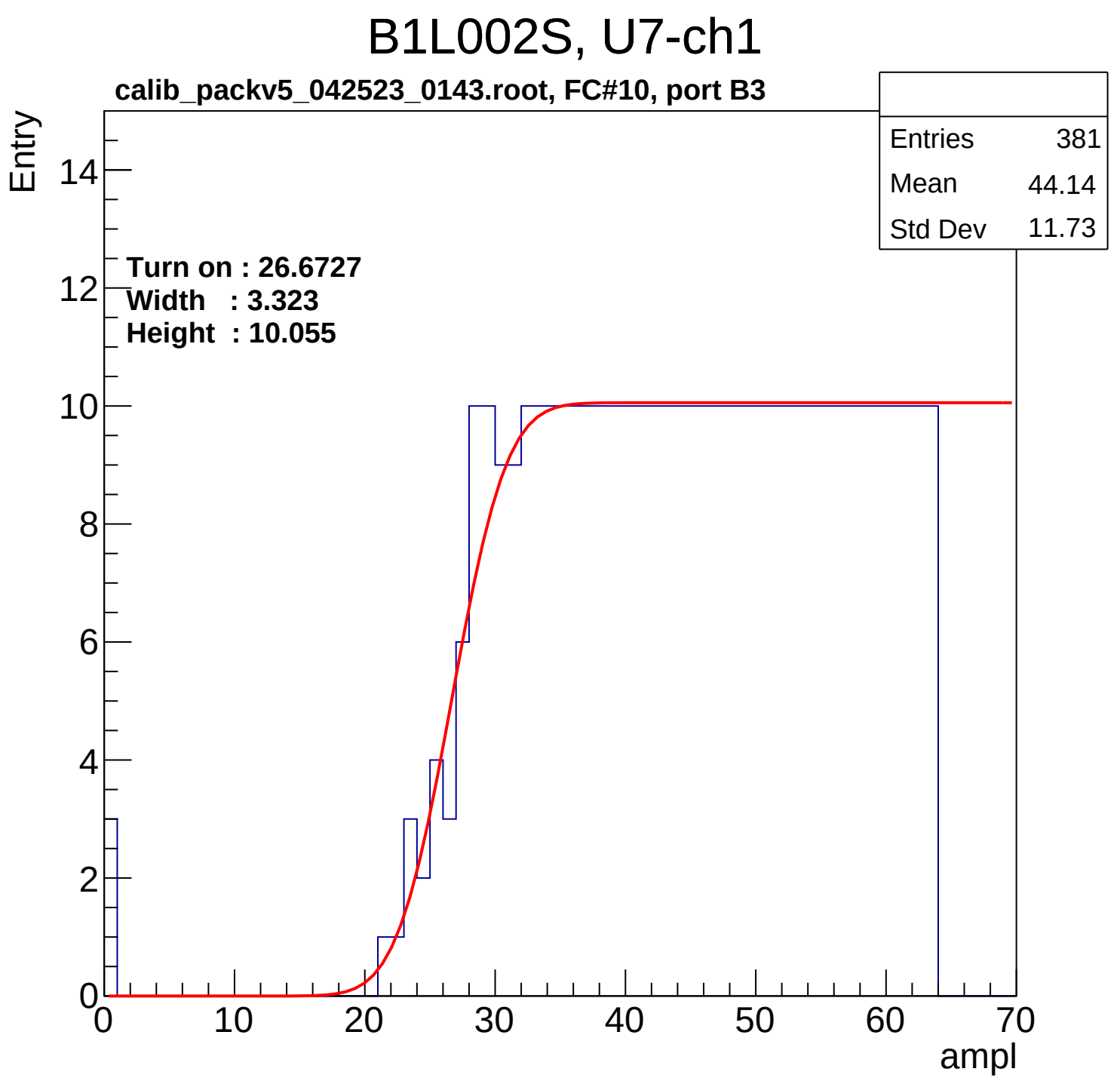
B1L002S, U7-ch1
calib_packv5_042523_0143.root, FC#10, port B3
Entries 381
Mean 44.14
Std Dev 11.73
Turn on : 26.6727
Width : 3.323
Height : 10.055
Entry
ampl
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2
4
6
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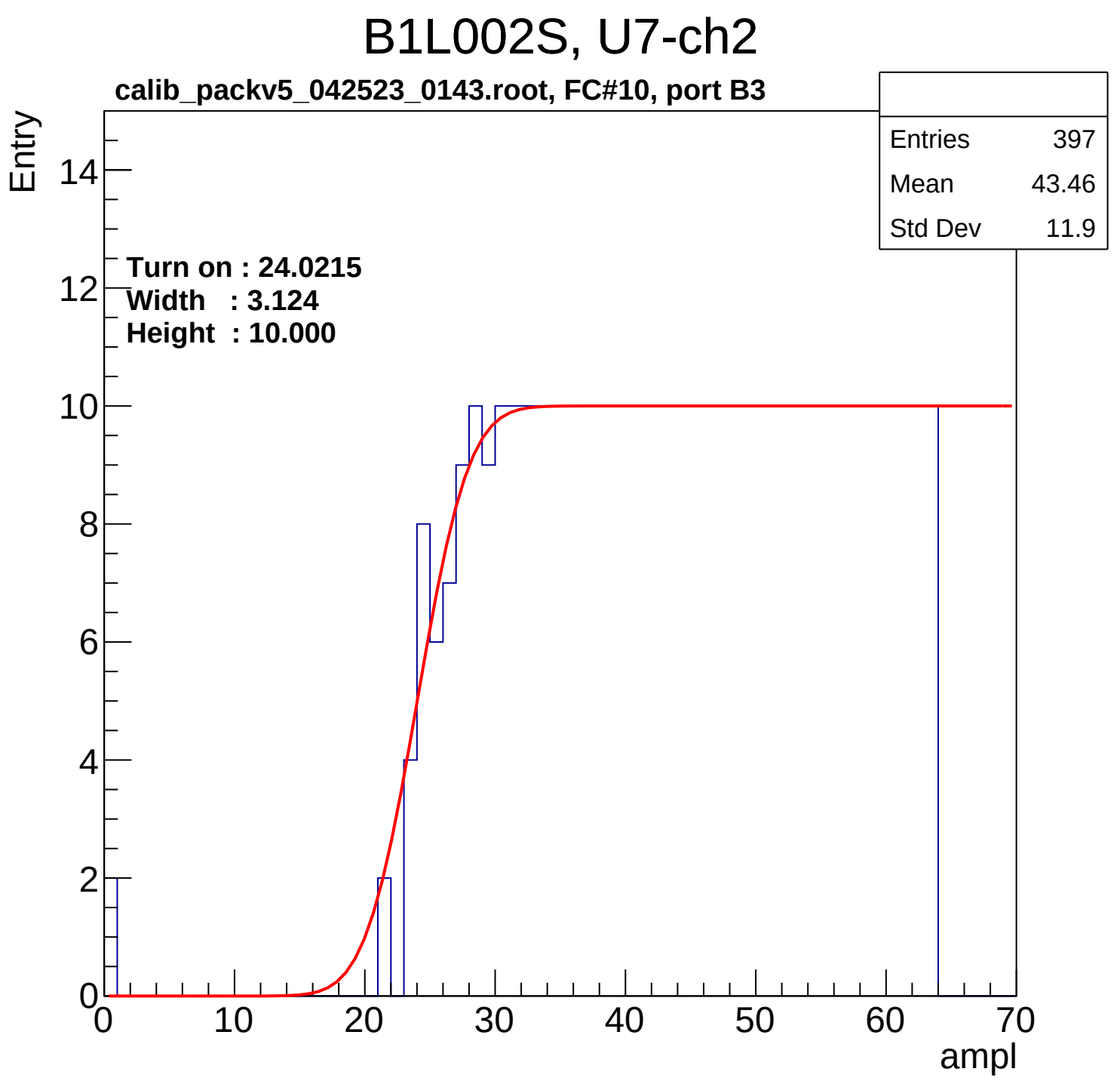
B1L002S, U7-ch2
calib_packv5_042523_0143.root, FC#10, port B3
Entries 397
Mean 43.46
Std Dev 11.9
Turn on : 24.0215
Width : 3.124
Height : 10.000
Entry
ampl
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2
4
6
8
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0
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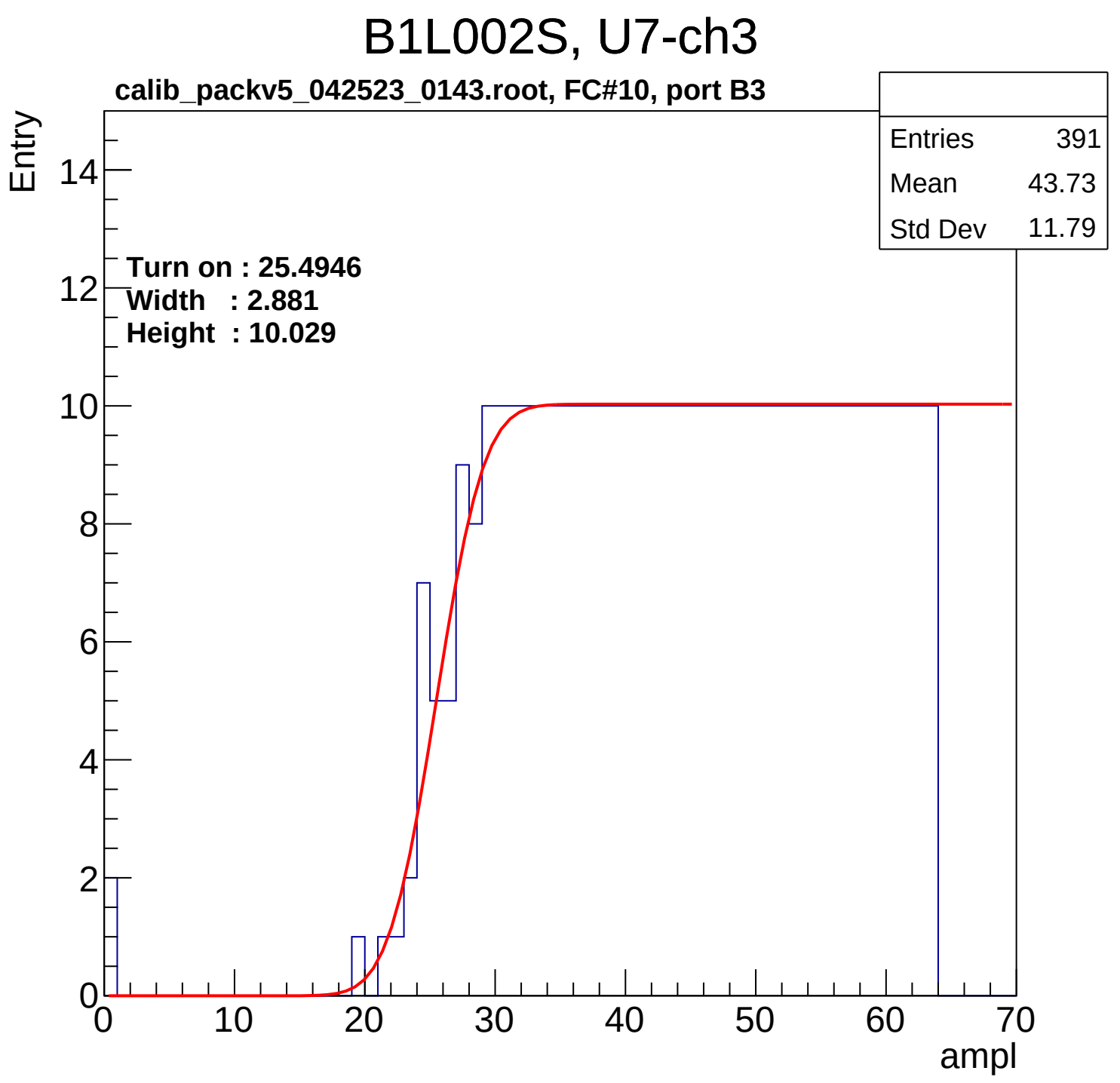
B1L002S, U7-ch3
calib_packv5_042523_0143.root, FC#10, port B3
Entries 391
Mean 43.73
Std Dev 11.79
Turn on : 25.4946
Width : 2.881
Height : 10.029
Entry
ampl
0
2
4
6
8
10
12
14
0
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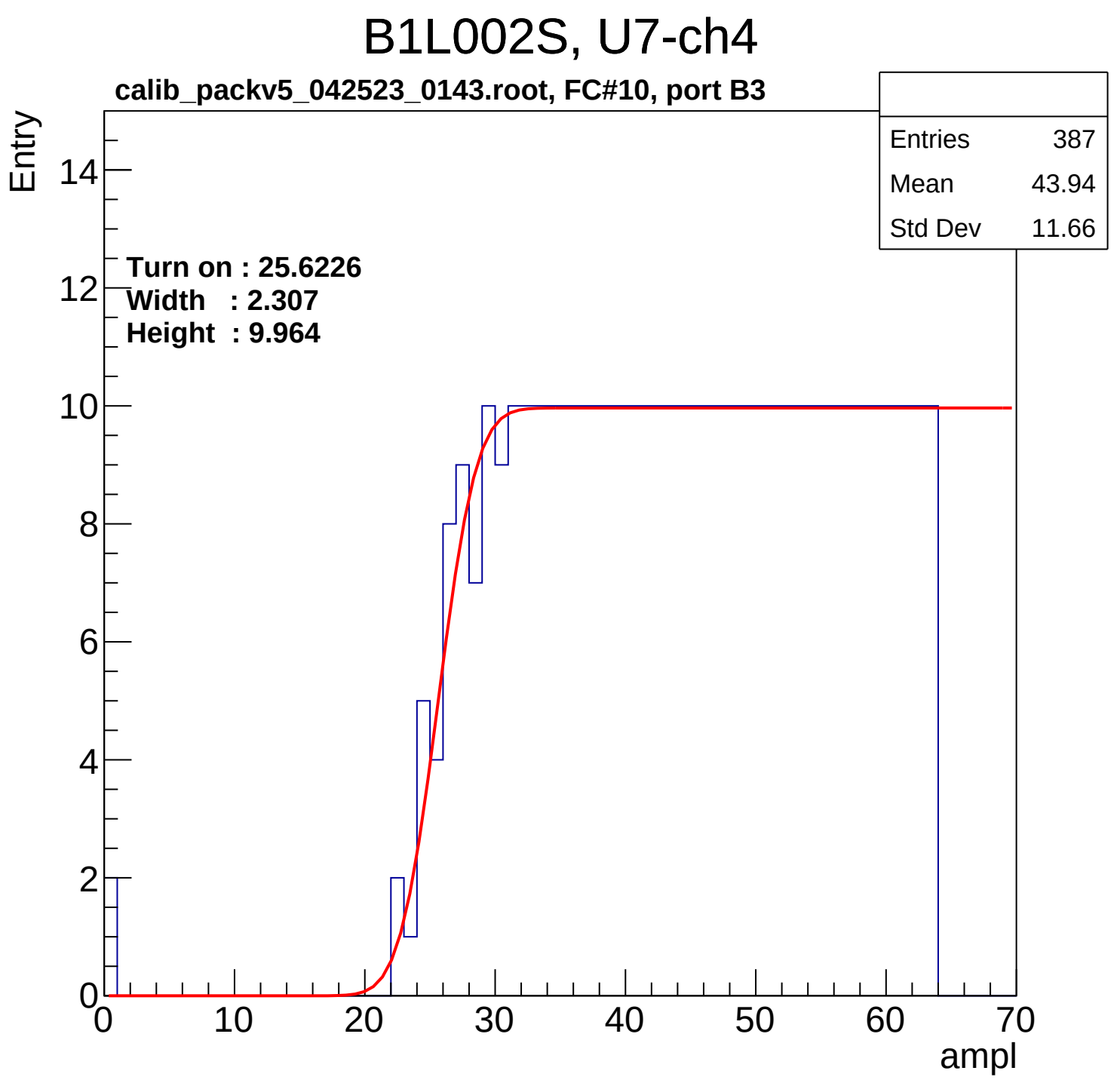
B1L002S, U7-ch4
calib_packv5_042523_0143.root, FC#10, port B3
Entries 387
Mean 43.94
Std Dev 11.66
Turn on : 25.6226
Width : 2.307
Height : 9.964
Entry
ampl
0
2
4
6
8
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0
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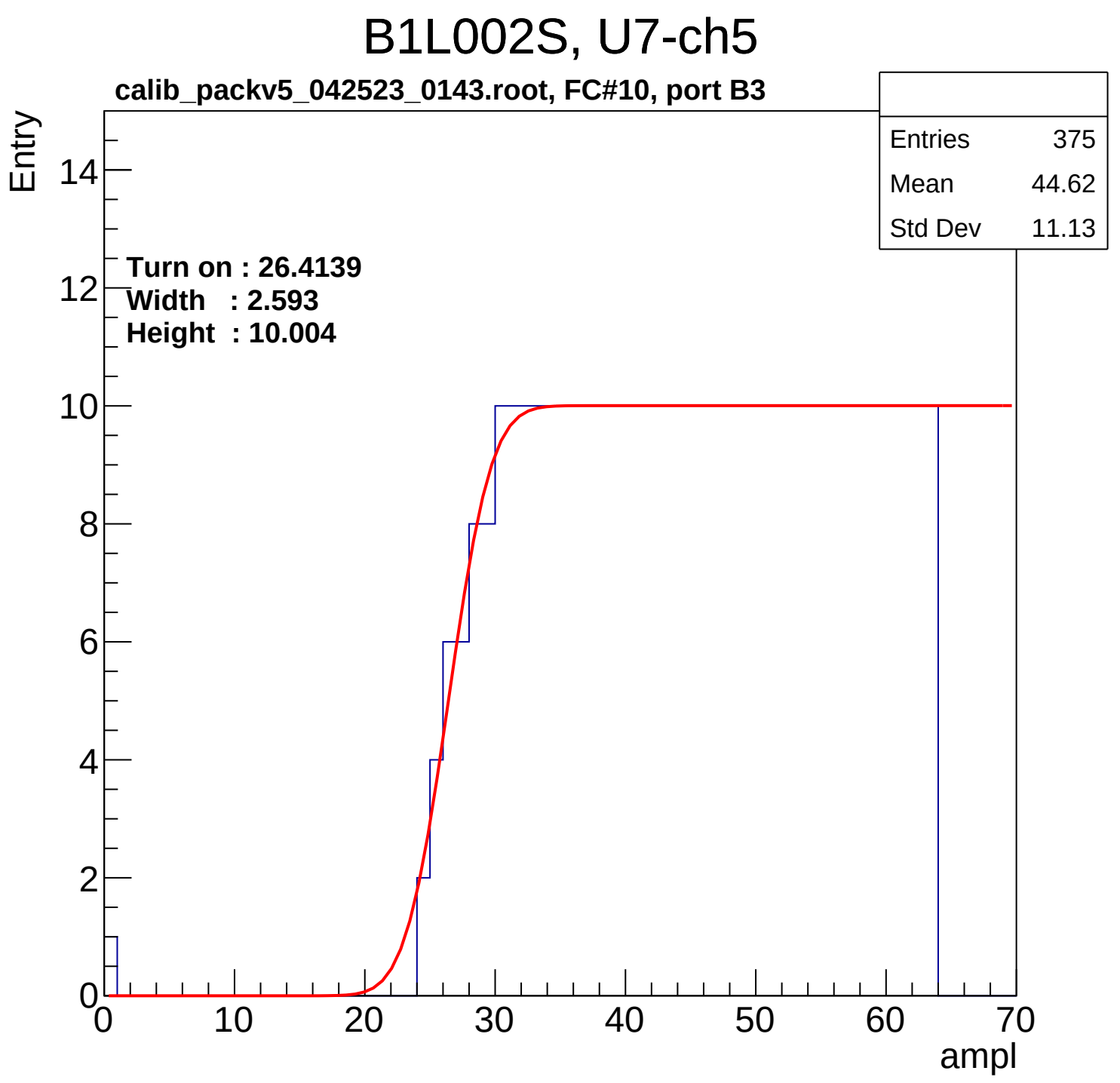
B1L002S, U7-ch5
calib_packv5_042523_0143.root, FC#10, port B3
Entries 375
Mean 44.62
Std Dev 11.13
Turn on : 26.4139
Width : 2.593
Height : 10.004
Entry
ampl
0
2
4
6
8
10
12
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0
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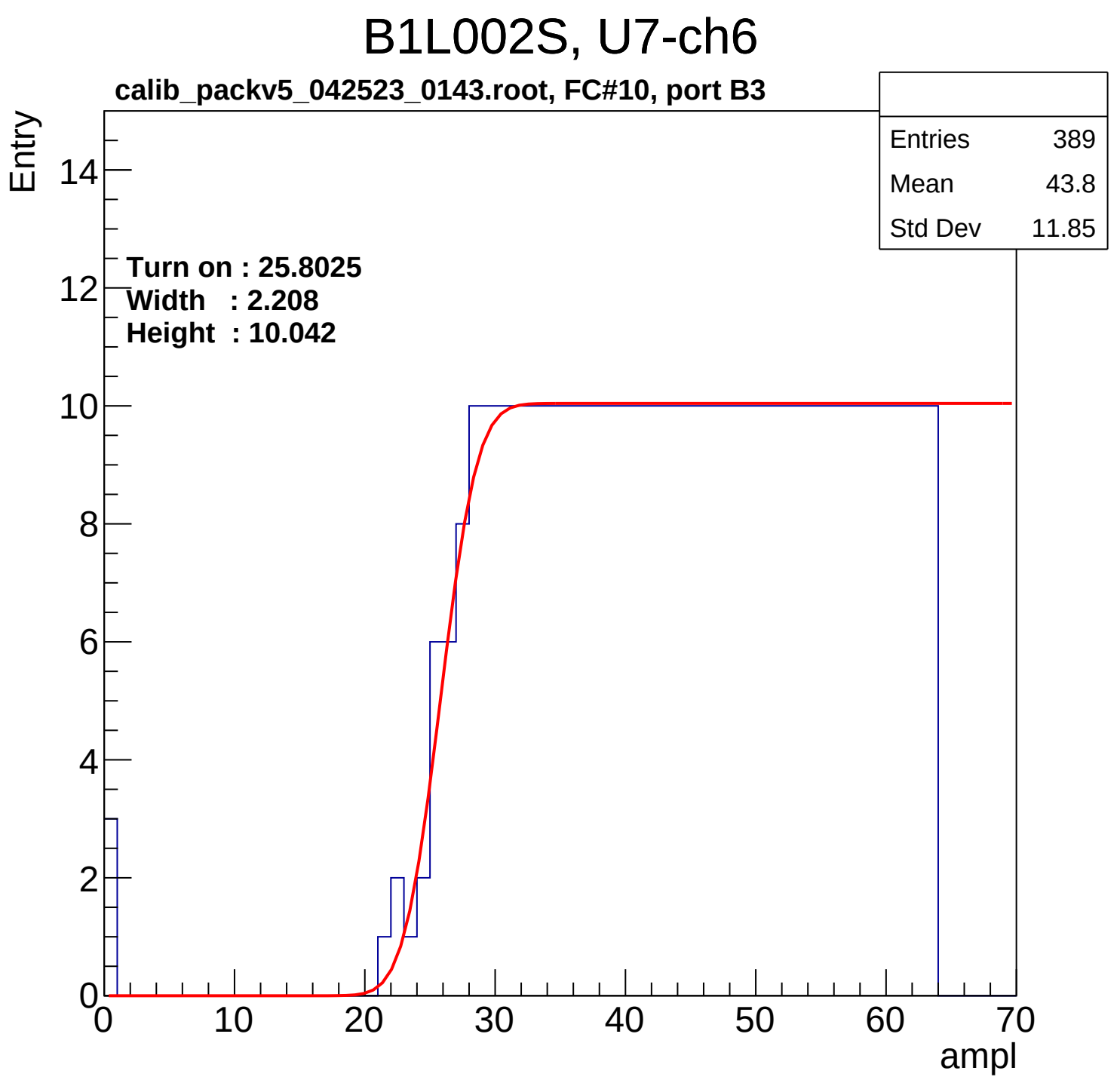
B1L002S, U7-ch6
calib_packv5_042523_0143.root, FC#10, port B3
Entries 389
Mean 43.8
Std Dev 11.85
Turn on : 25.8025
Width : 2.208
Height : 10.042
Entry
ampl
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2
4
6
8
10
12
14
0
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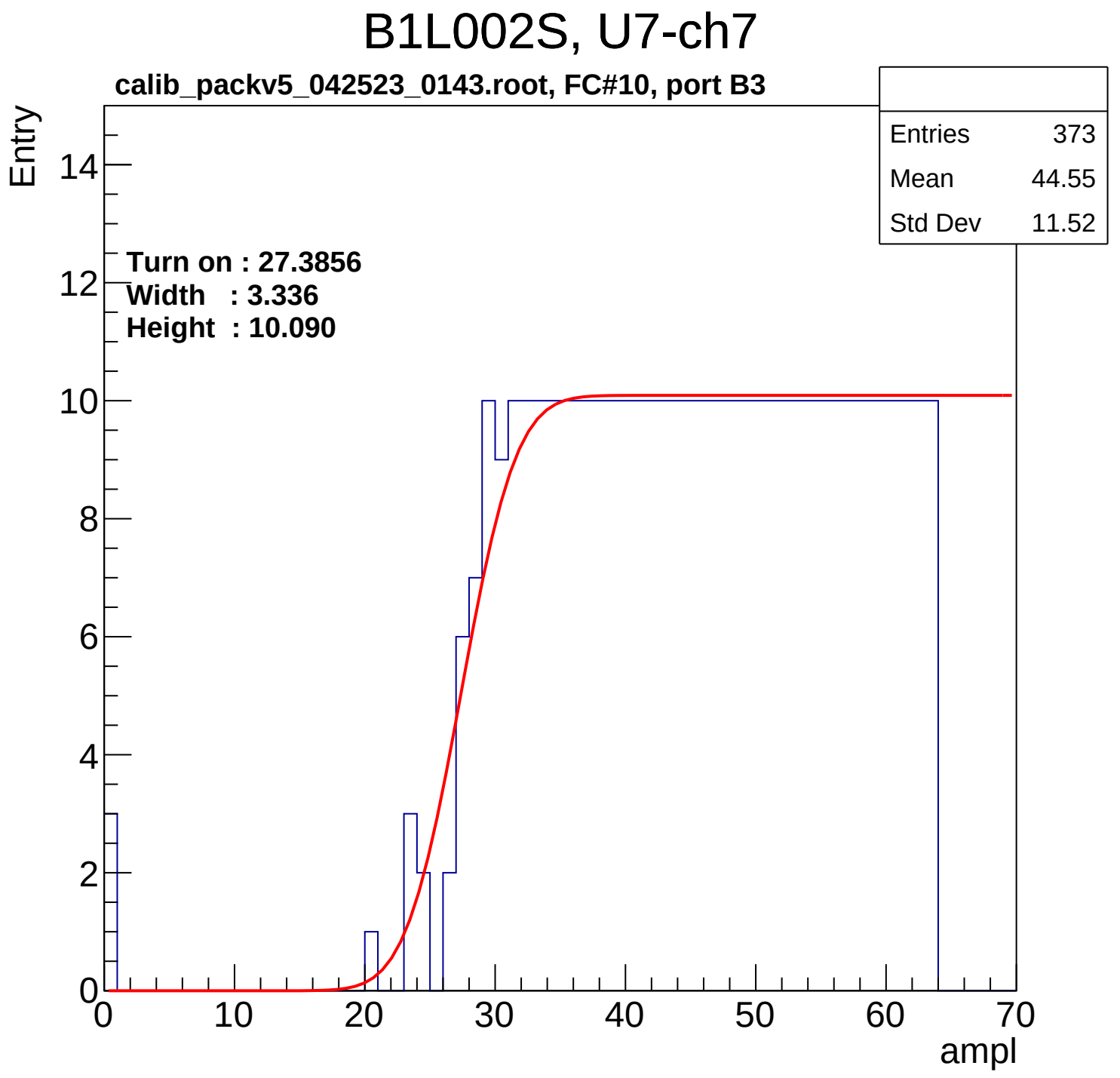
B1L002S, U7-ch7
calib_packv5_042523_0143.root, FC#10, port B3
Entries 373
Mean 44.55
Std Dev 11.52
Turn on : 27.3856
Width : 3.336
Height : 10.090
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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60
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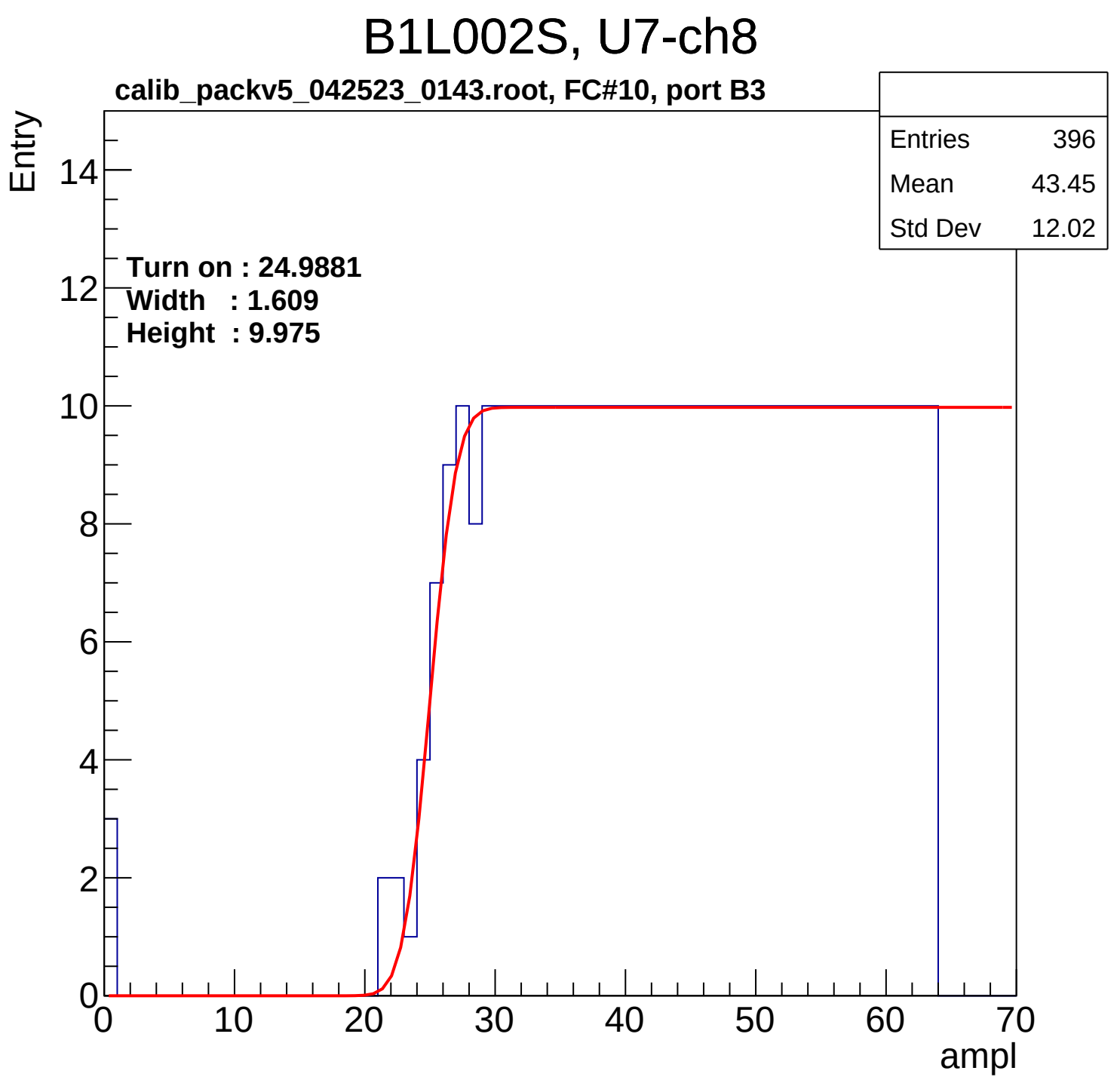
B1L002S, U7-ch8
calib_packv5_042523_0143.root, FC#10, port B3
Entries 396
Mean 43.45
Std Dev 12.02
Turn on : 24.9881
Width : 1.609
Height : 9.975
Entry
ampl
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6
8
10
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0
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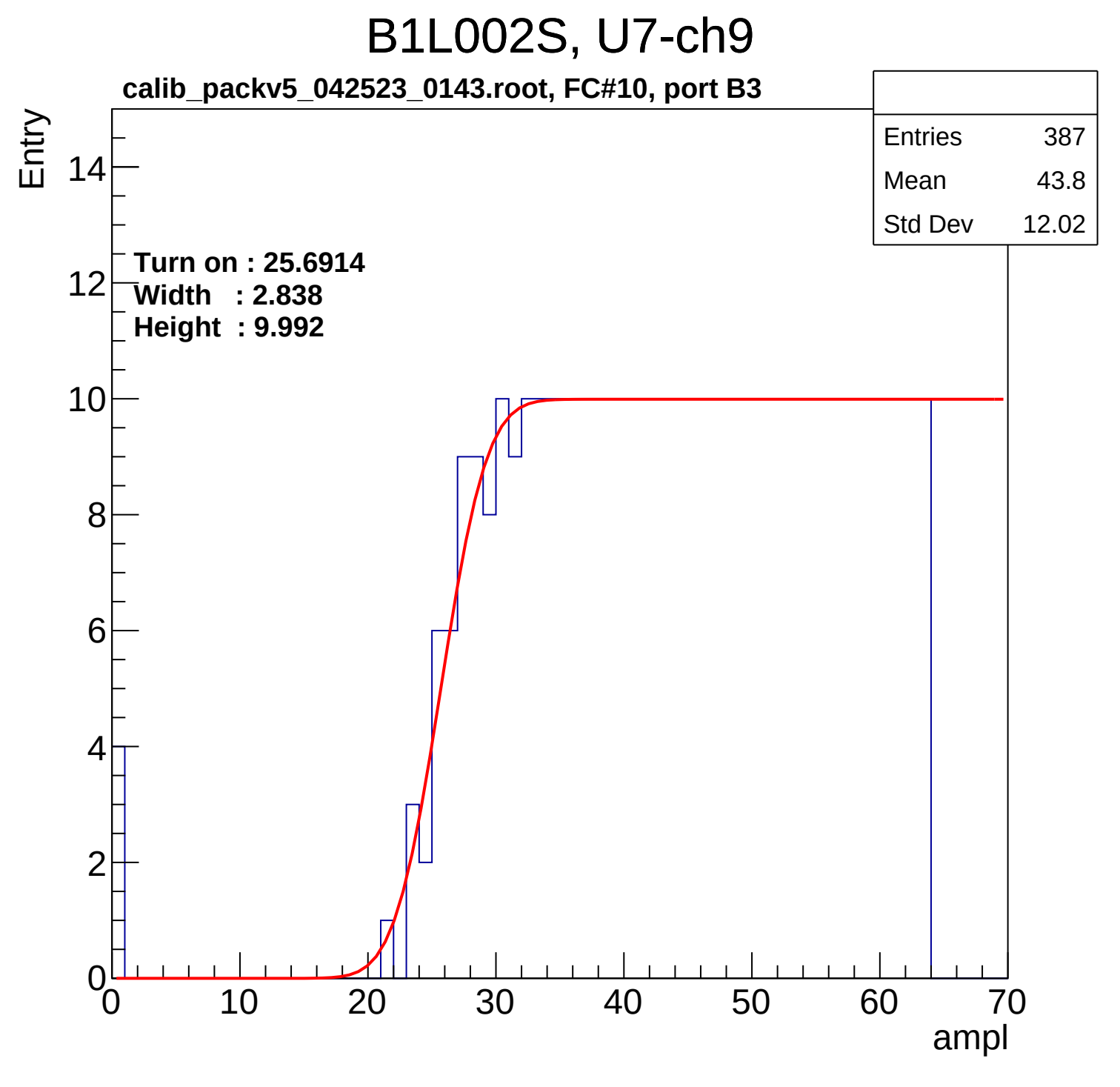
B1L002S, U7-ch9
calib_packv5_042523_0143.root, FC#10, port B3
Entries 387
Mean 43.8
Std Dev 12.02
Turn on : 25.6914
Width : 2.838
Height : 9.992
Entry
ampl
0
2
4
6
8
10
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0
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60
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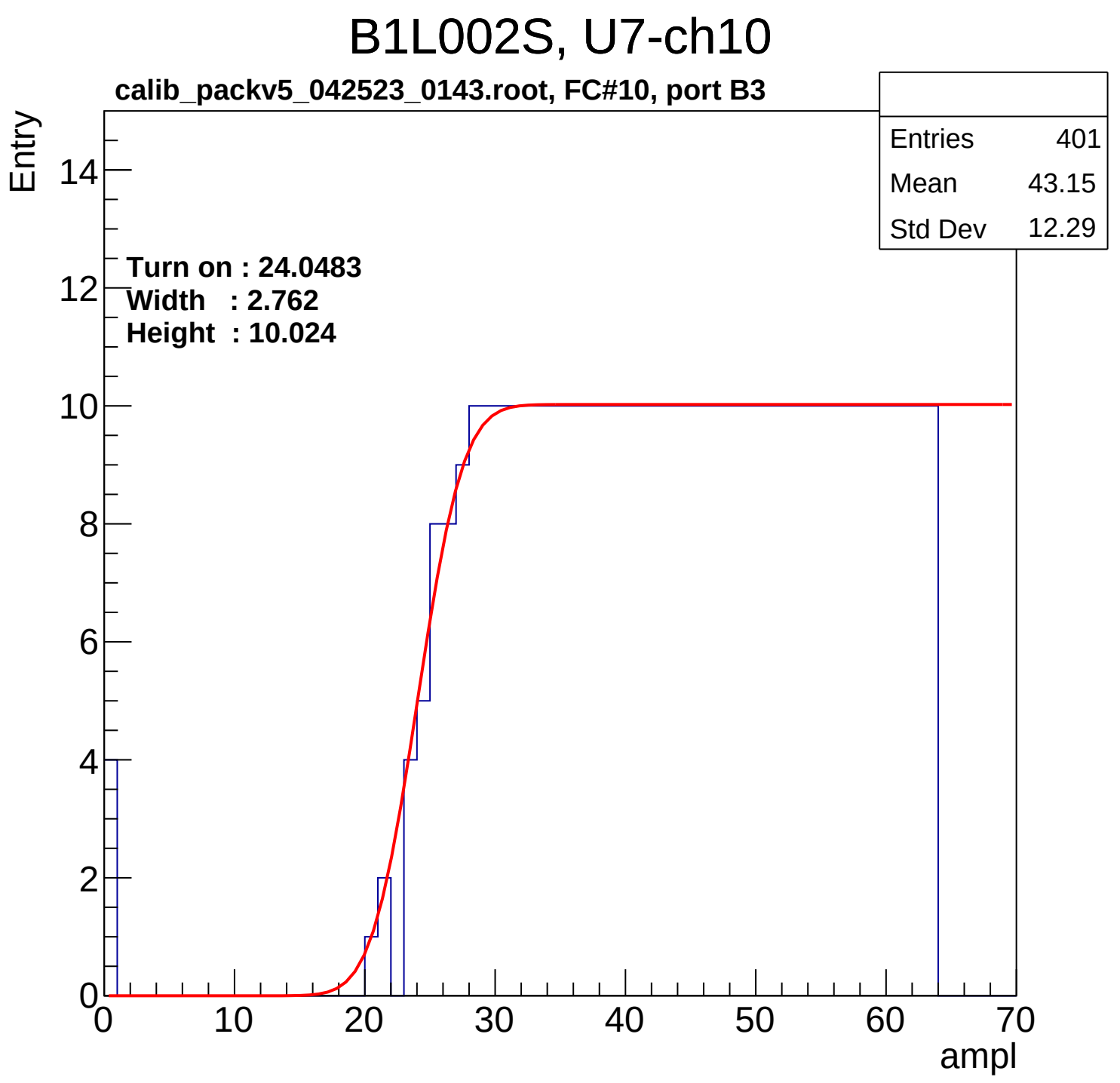
B1L002S, U7-ch10
calib_packv5_042523_0143.root, FC#10, port B3
Entries 401
Mean 43.15
Std Dev 12.29
Turn on : 24.0483
Width : 2.762
Height : 10.024
Entry
ampl
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6
8
10
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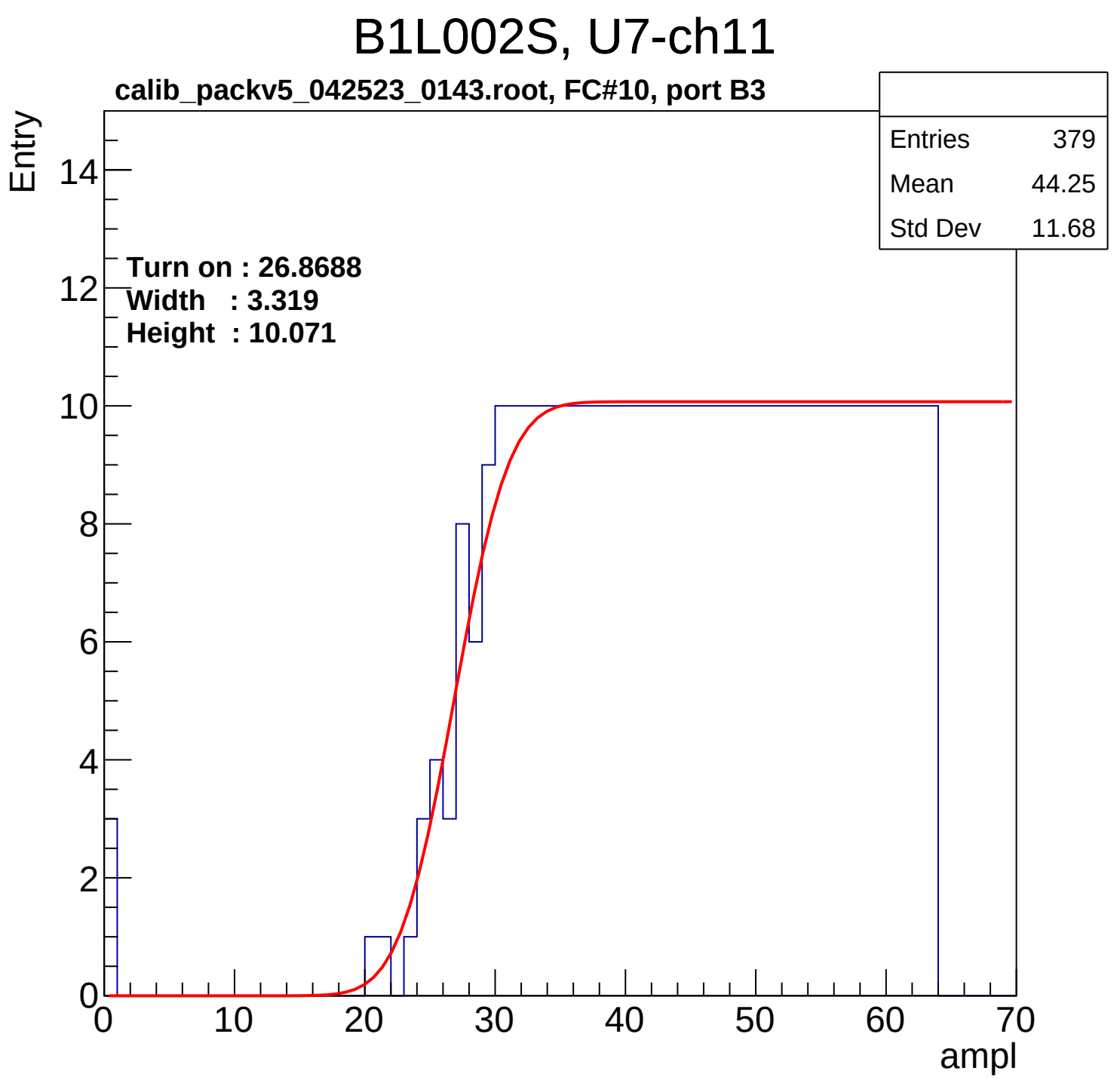
B1L002S, U7-ch11
calib_packv5_042523_0143.root, FC#10, port B3
Entries 379
Mean 44.25
Std Dev 11.68
Turn on : 26.8688
Width : 3.319
Height : 10.071
Entry
ampl
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6
8
10
12
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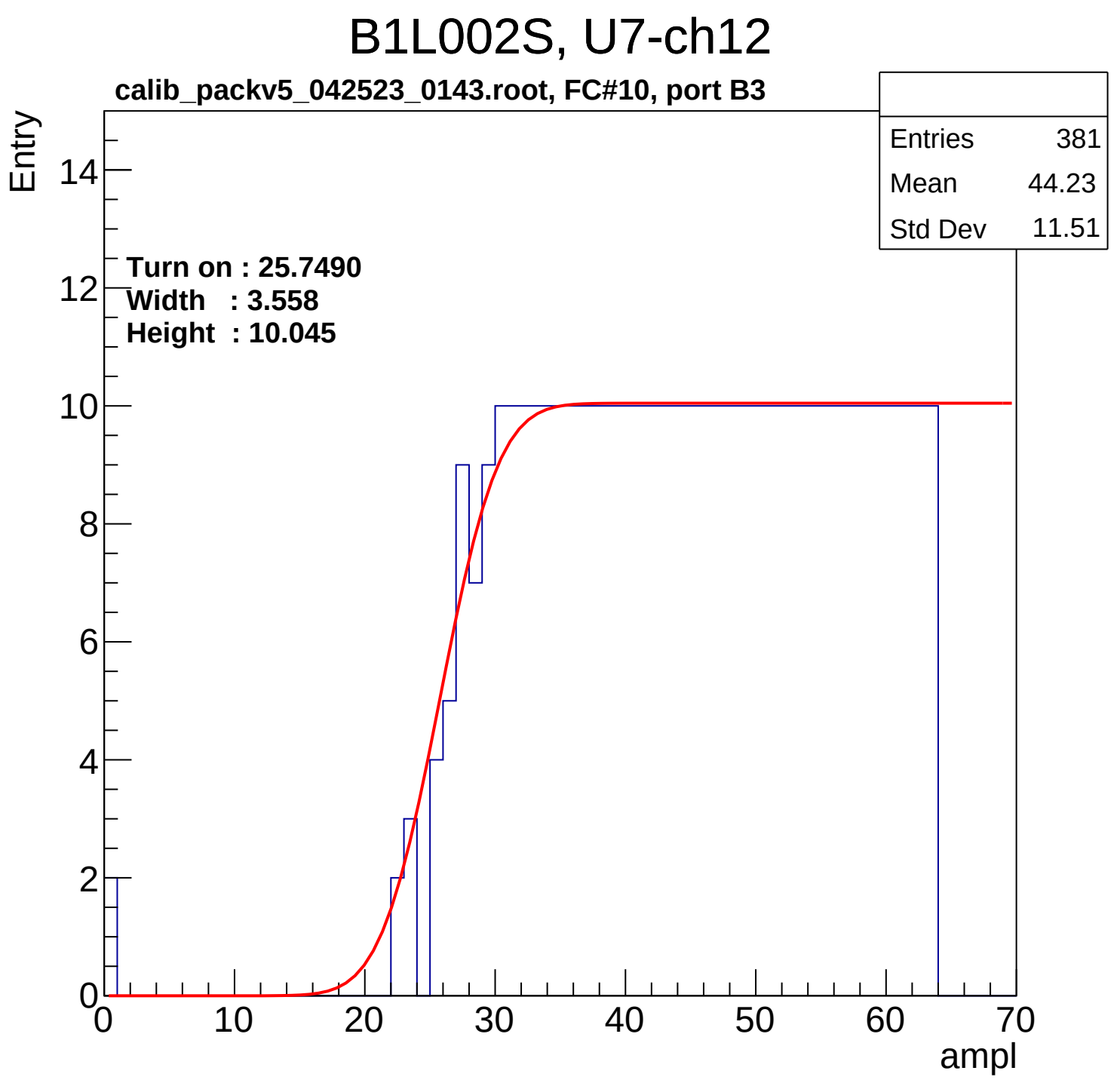
B1L002S, U7-ch12
calib_packv5_042523_0143.root, FC#10, port B3
Entries 381
Mean 44.23
Std Dev 11.51
Turn on : 25.7490
Width : 3.558
Height : 10.045
Entry
ampl
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2
4
6
8
10
12
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0
10
20
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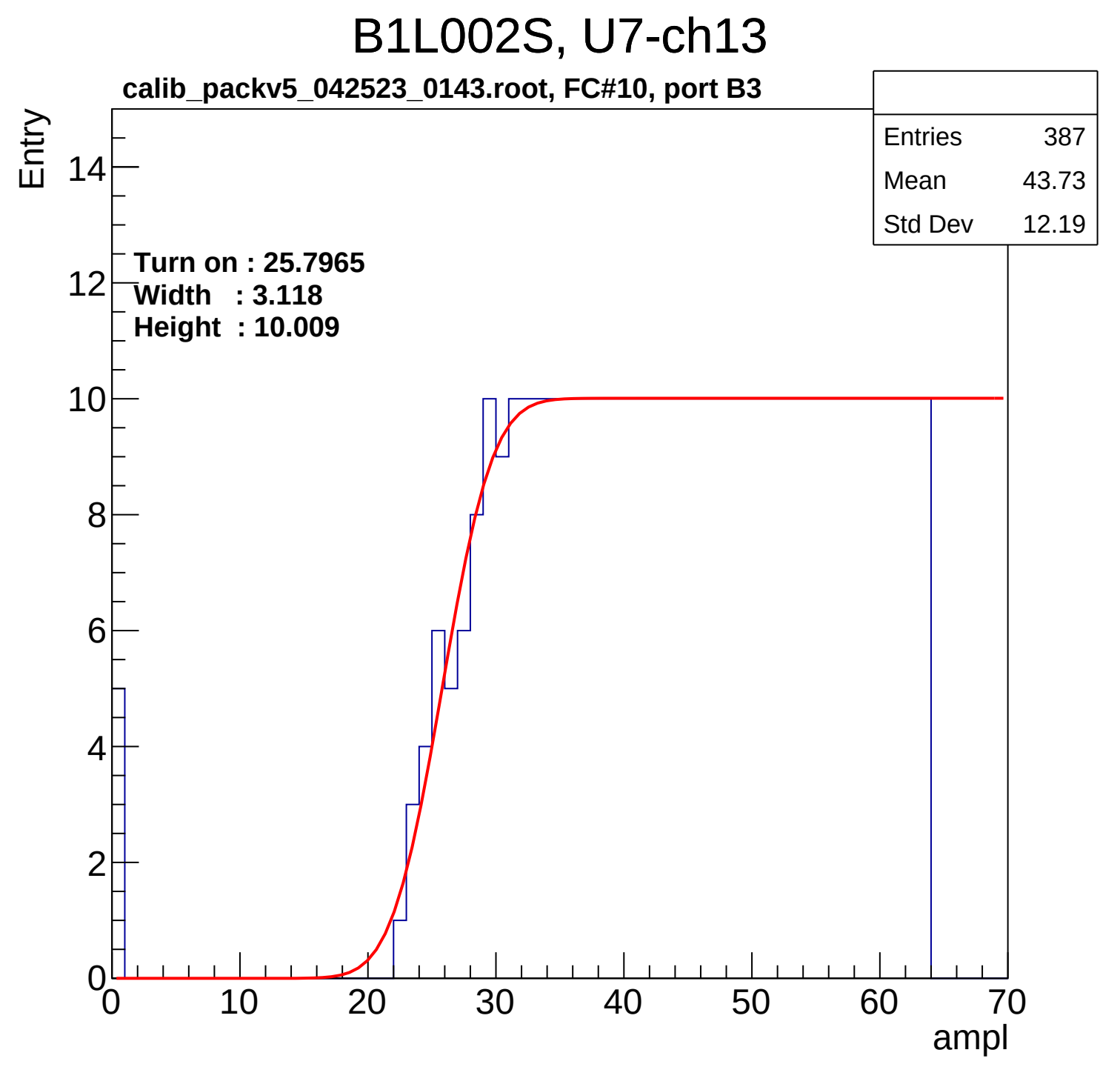
B1L002S, U7-ch13
calib_packv5_042523_0143.root, FC#10, port B3
Entries 387
Mean 43.73
Std Dev 12.19
Turn on : 25.7965
Width : 3.118
Height : 10.009
Entry
ampl
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4
6
8
10
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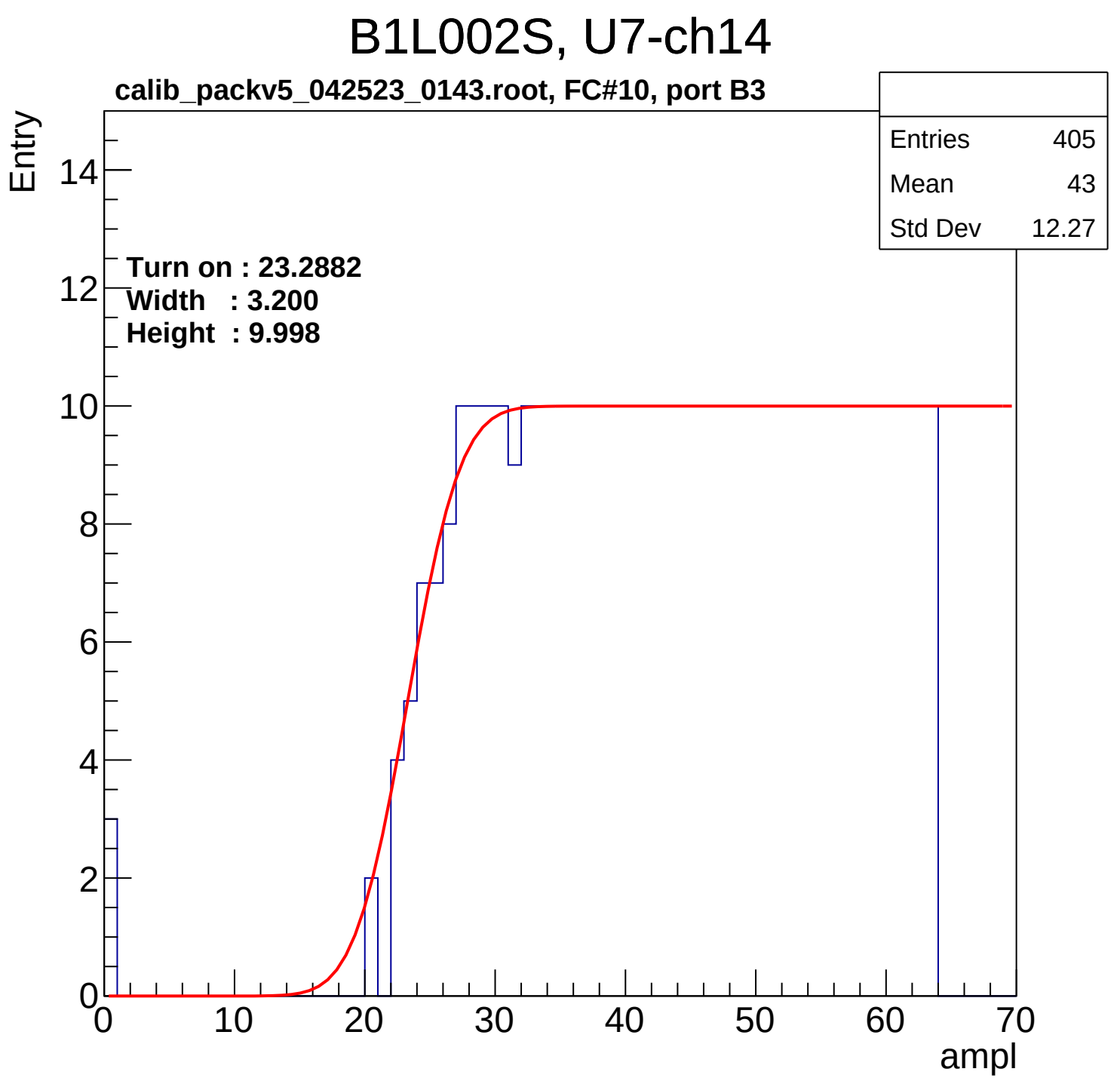
B1L002S, U7-ch14
calib_packv5_042523_0143.root, FC#10, port B3
Entries 405
Mean 43
Std Dev 12.27
Turn on : 23.2882
Width : 3.200
Height : 9.998
Entry
ampl
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4
6
8
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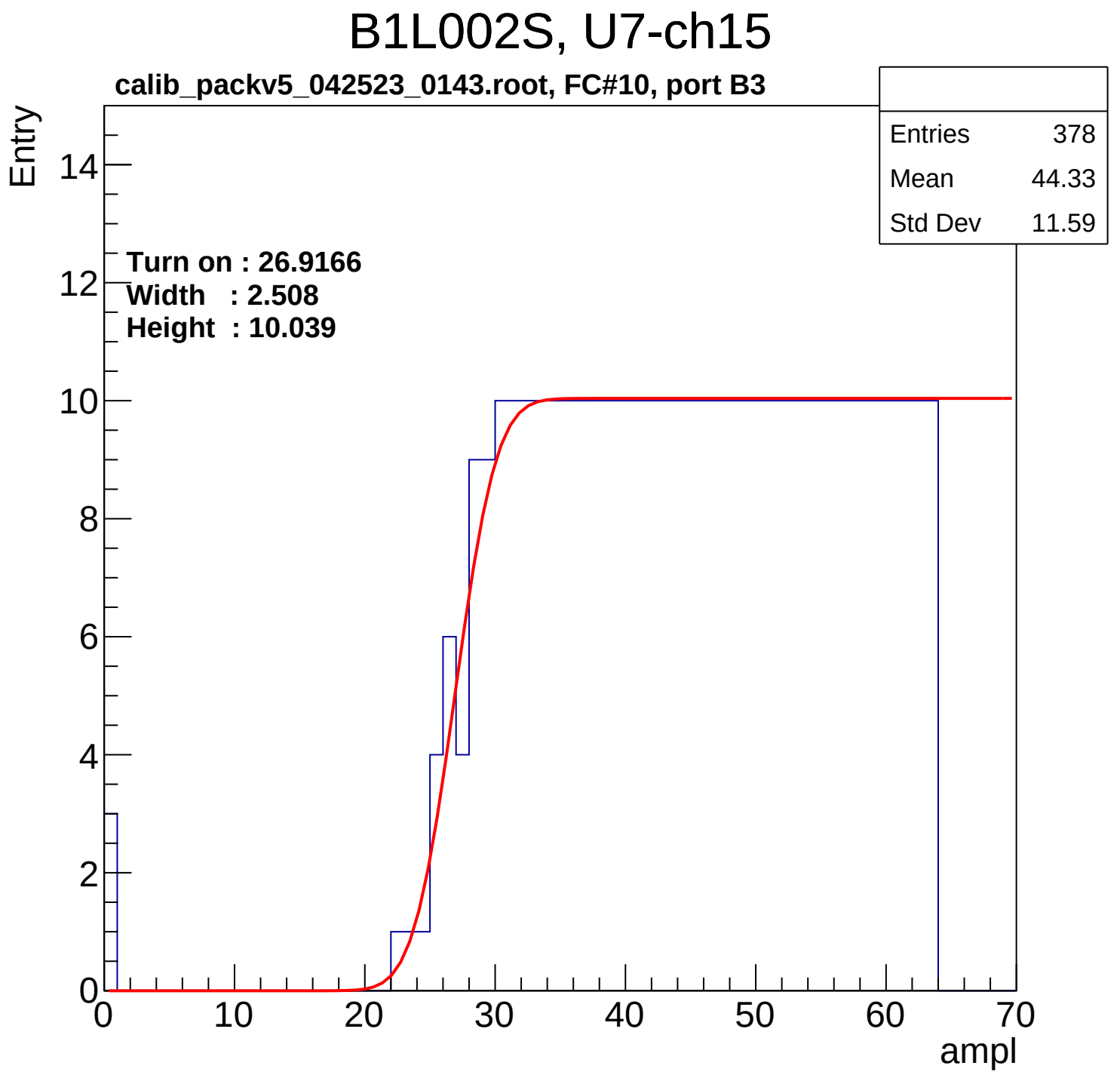
B1L002S, U7-ch15
calib_packv5_042523_0143.root, FC#10, port B3
Entries 378
Mean 44.33
Std Dev 11.59
Turn on : 26.9166
Width : 2.508
Height : 10.039
Entry
ampl
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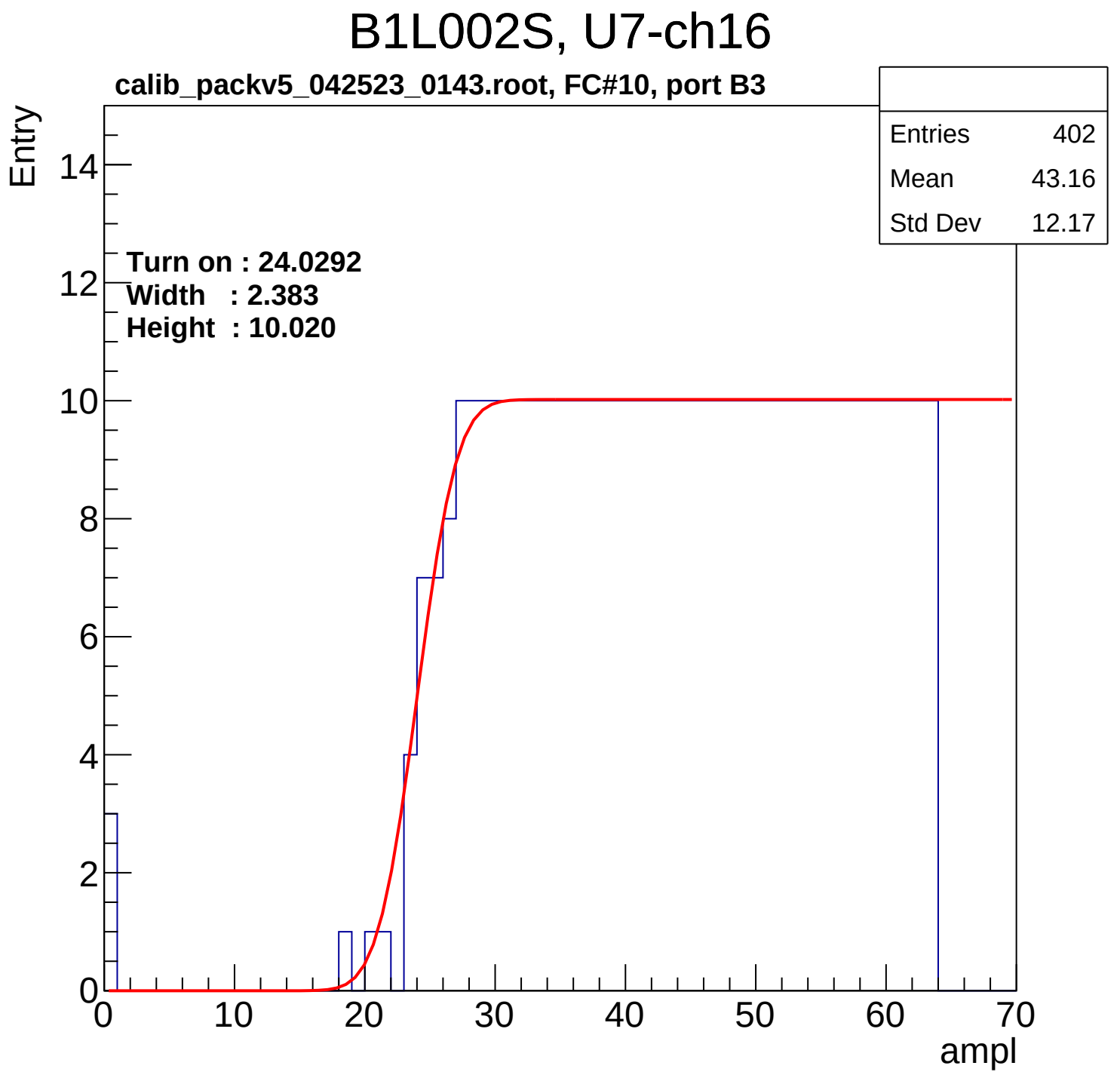
B1L002S, U7-ch16
calib_packv5_042523_0143.root, FC#10, port B3
Entries 402
Mean 43.16
Std Dev 12.17
Turn on : 24.0292
Width : 2.383
Height : 10.020
Entry
ampl
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2
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6
8
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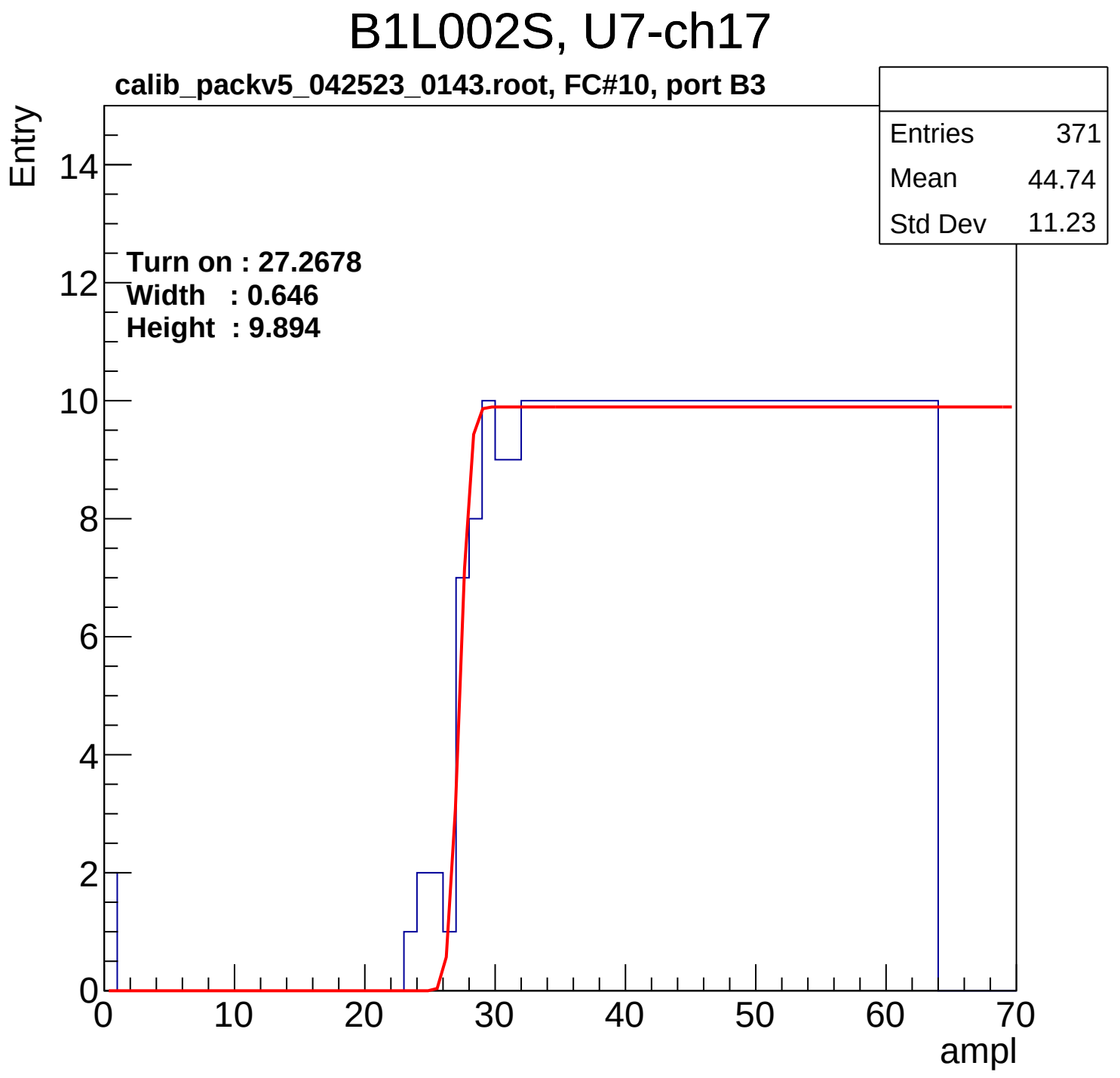
B1L002S, U7-ch17
calib_packv5_042523_0143.root, FC#10, port B3
Entries 371
Mean 44.74
Std Dev 11.23
Turn on : 27.2678
Width : 0.646
Height : 9.894
Entry
ampl
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2
4
6
8
10
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0
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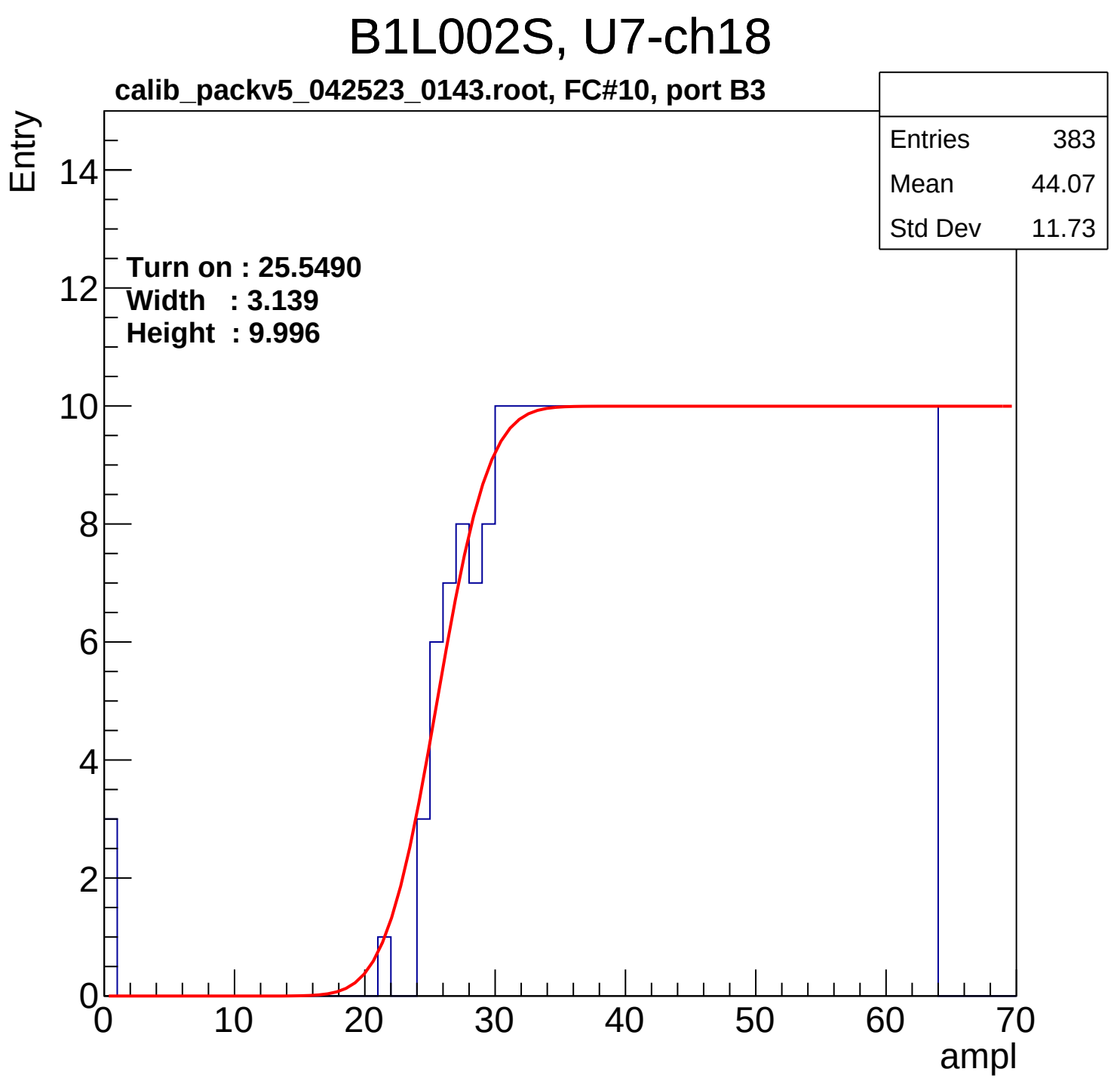
B1L002S, U7-ch18
calib_packv5_042523_0143.root, FC#10, port B3
Entries 383
Mean 44.07
Std Dev 11.73
Turn on : 25.5490
Width : 3.139
Height : 9.996
Entry
ampl
0
2
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6
8
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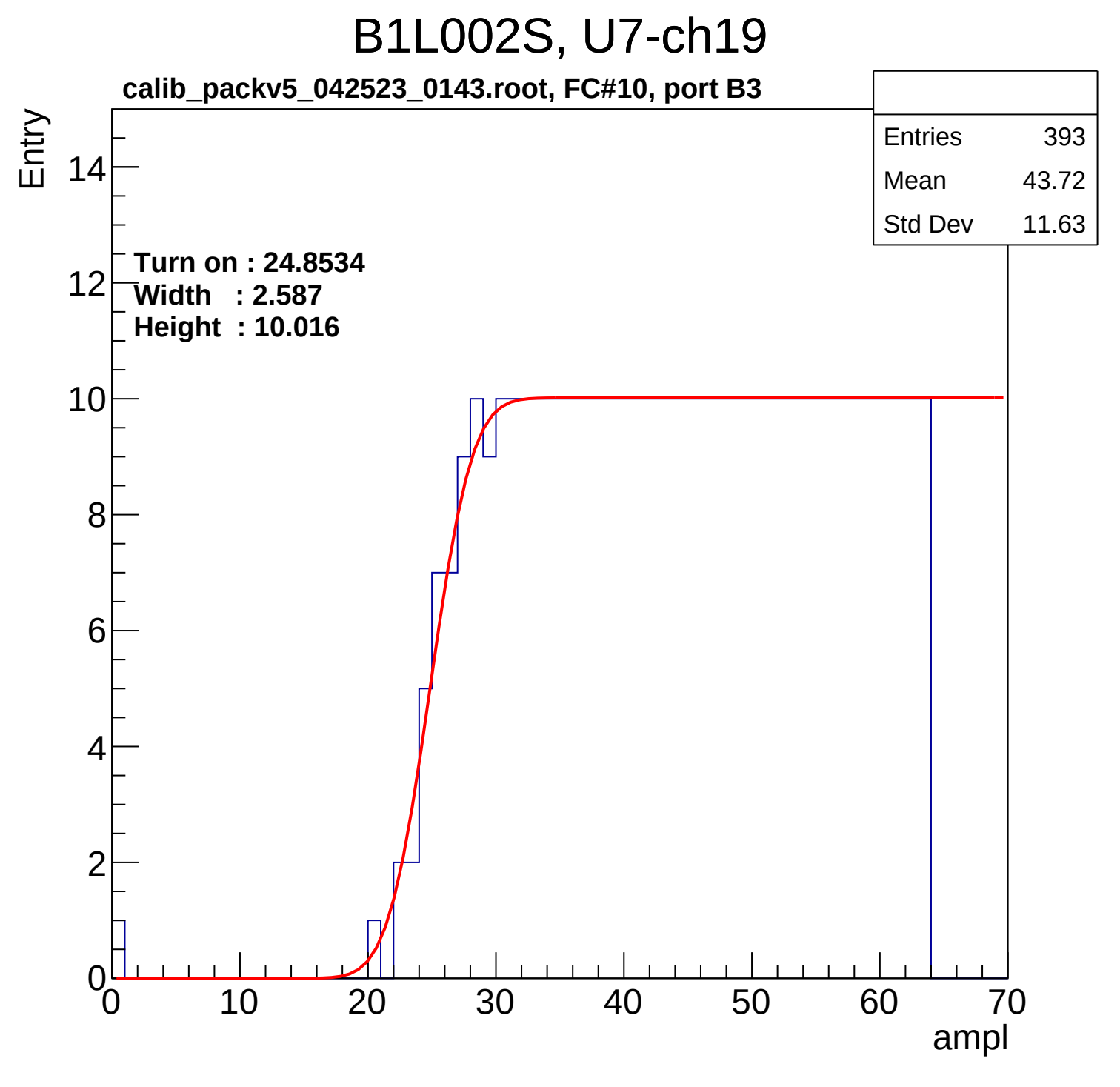
B1L002S, U7-ch19
calib_packv5_042523_0143.root, FC#10, port B3
Entries 393
Mean 43.72
Std Dev 11.63
Turn on : 24.8534
Width : 2.587
Height : 10.016
Entry
ampl
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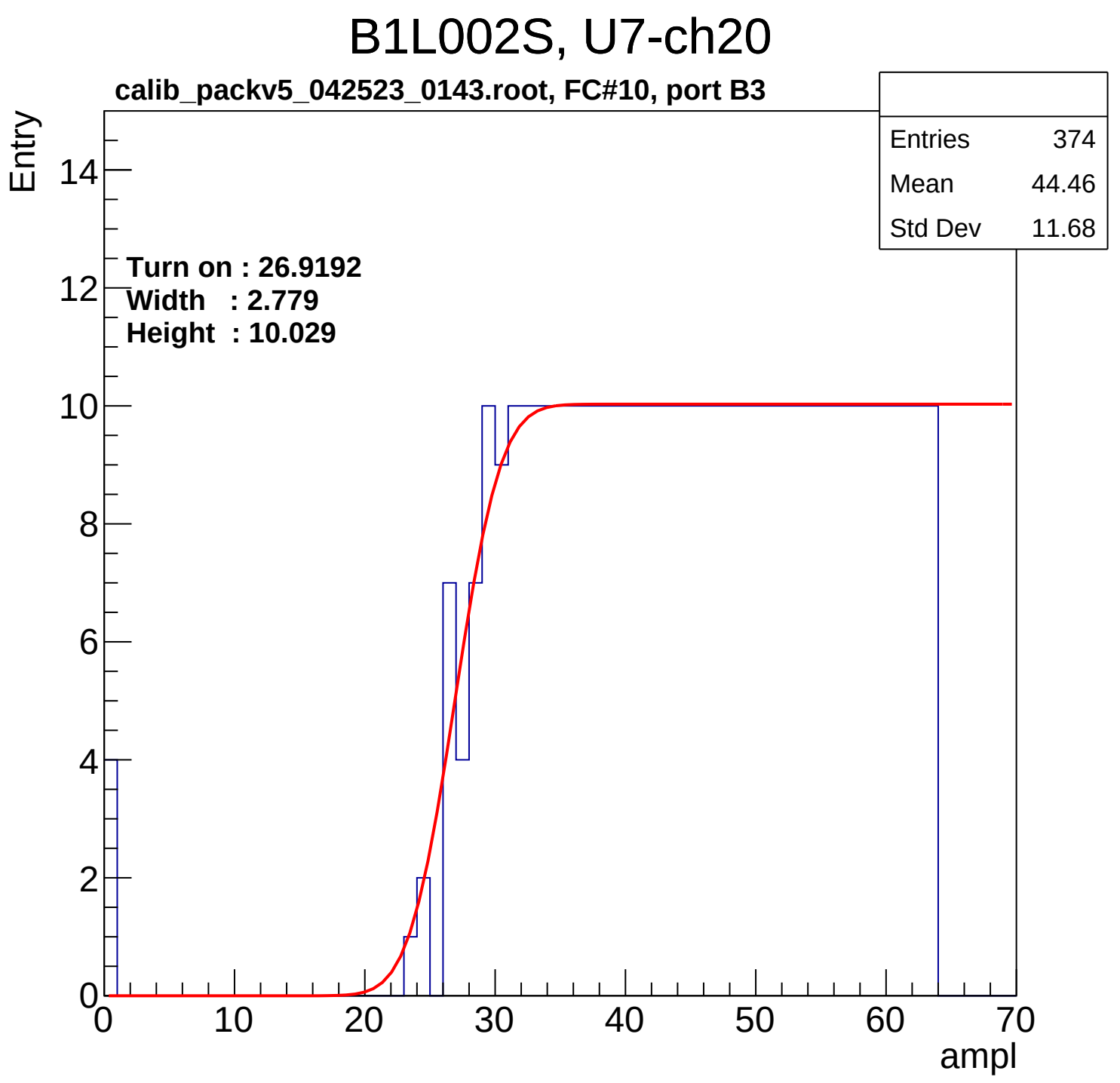
B1L002S, U7-ch20
calib_packv5_042523_0143.root, FC#10, port B3
Entries 374
Mean 44.46
Std Dev 11.68
Turn on : 26.9192
Width : 2.779
Height : 10.029
Entry
ampl
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8
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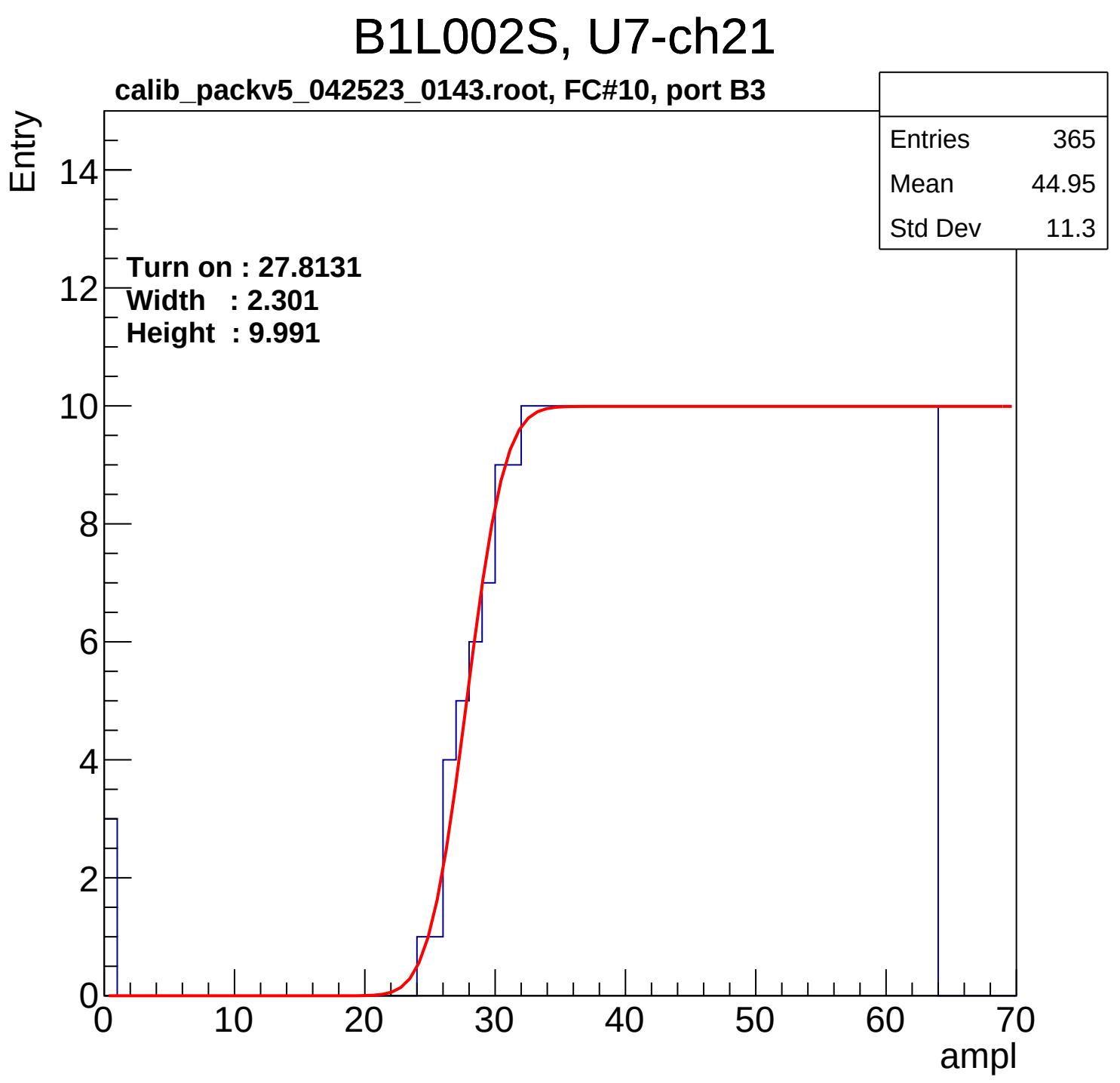
B1L002S, U7-ch21
calib_packv5_042523_0143.root, FC#10, port B3
Entries 365
Mean 44.95
Std Dev 11.3
Turn on : 27.8131
Width : 2.301
Height : 9.991
Entry
ampl
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6
8
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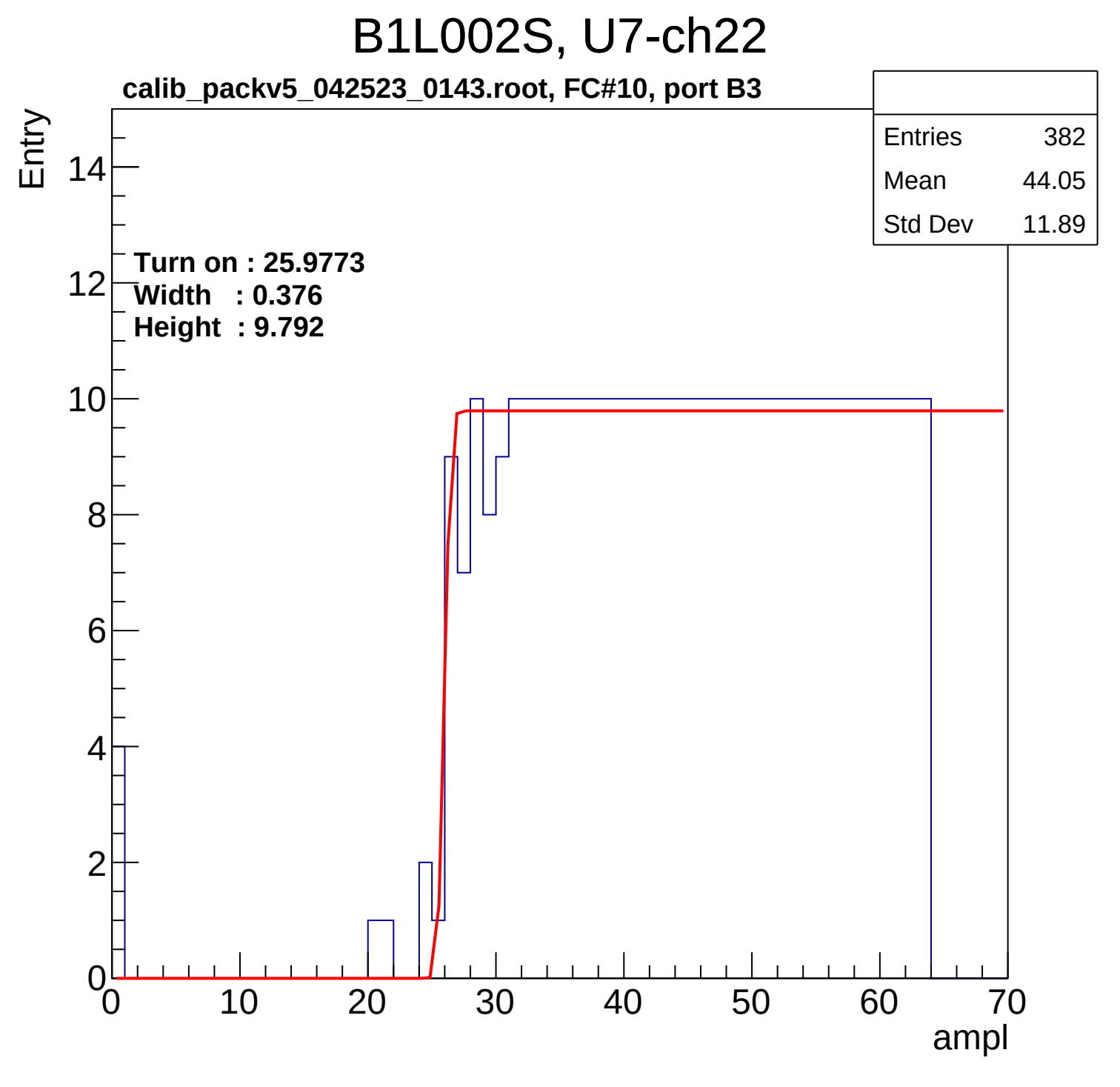
B1L002S, U7-ch22
calib_packv5_042523_0143.root, FC#10, port B3
Entries 382
Mean 44.05
Std Dev 11.89
Turn on : 25.9773
Width : 0.376
Height : 9.792
Entry
ampl
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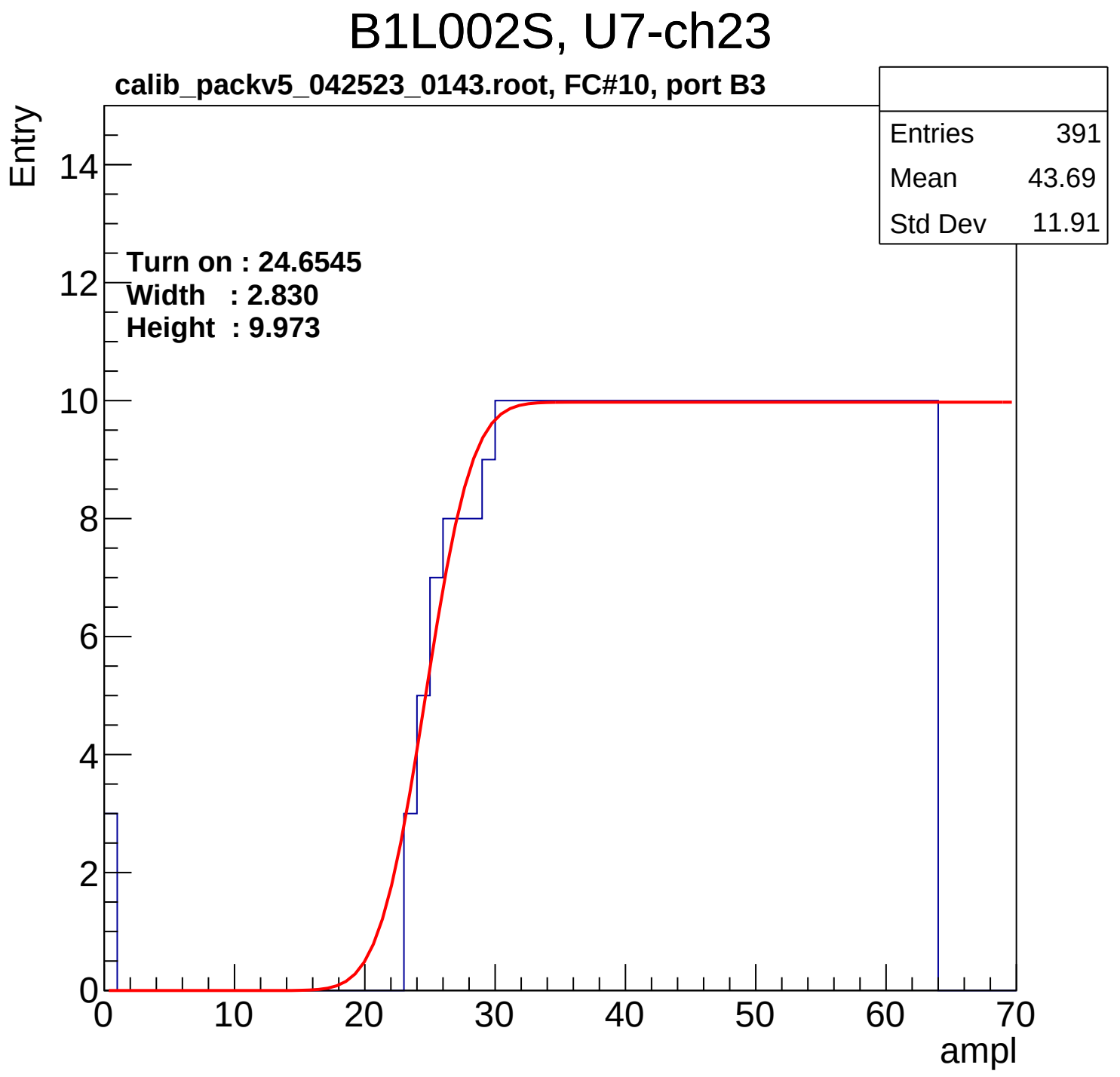
B1L002S, U7-ch23
calib_packv5_042523_0143.root, FC#10, port B3
Entries 391
Mean 43.69
Std Dev 11.91
Turn on : 24.6545
Width : 2.830
Height : 9.973
Entry
ampl
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4
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8
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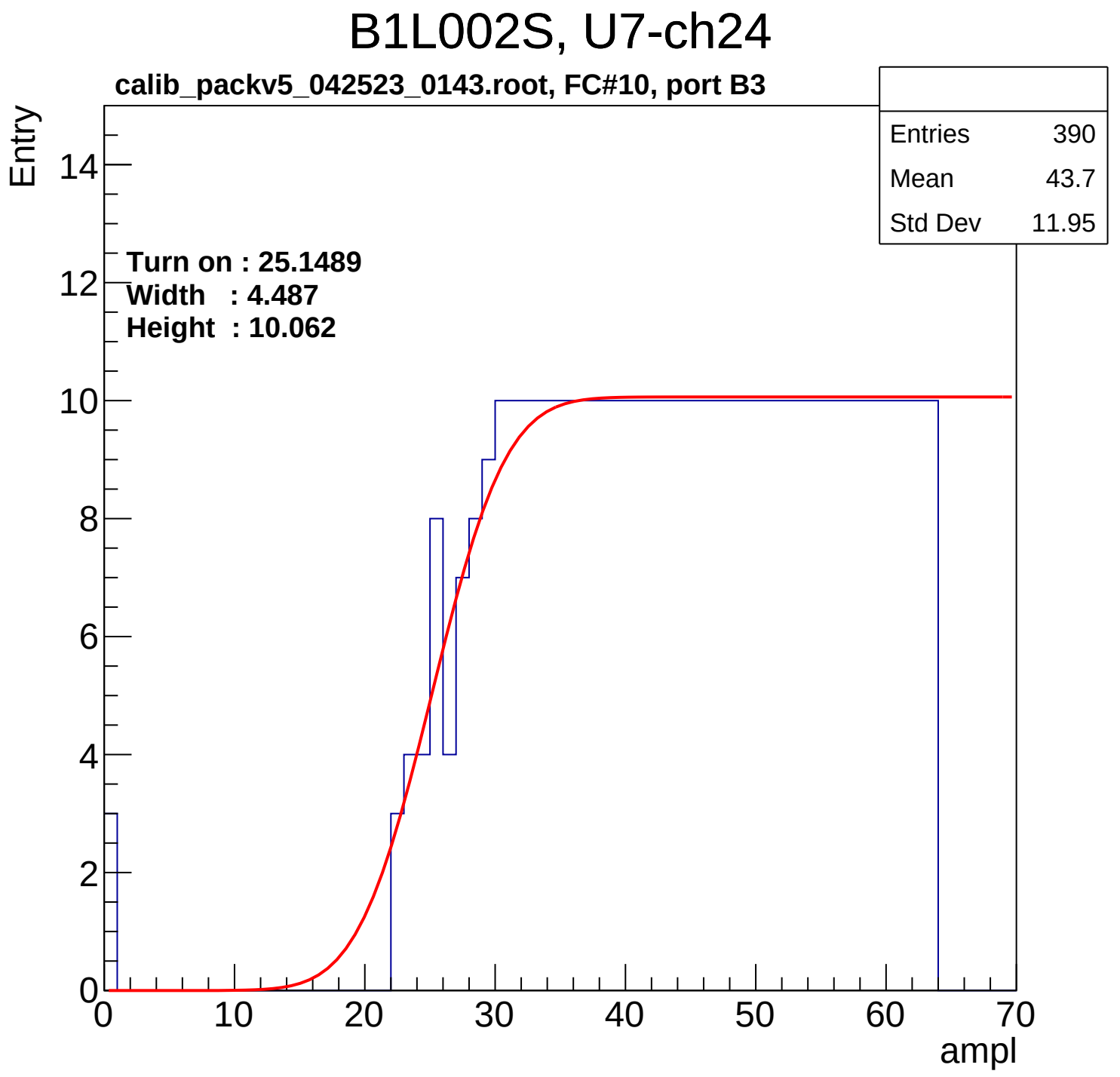
B1L002S, U7-ch24
calib_packv5_042523_0143.root, FC#10, port B3
Entries 390
Mean 43.7
Std Dev 11.95
Turn on : 25.1489
Width : 4.487
Height : 10.062
Entry
ampl
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6
8
10
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0
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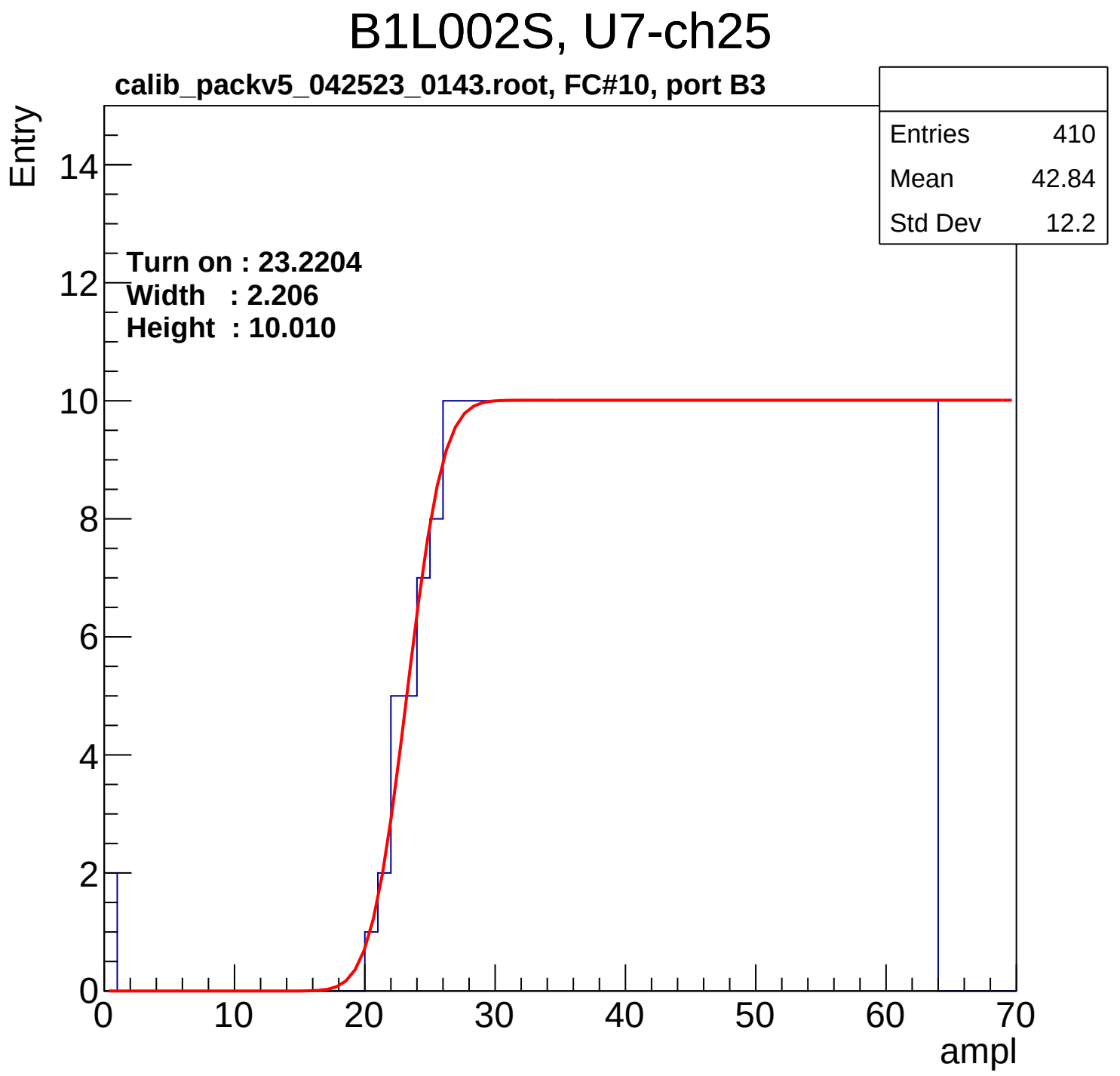
B1L002S, U7-ch25
calib_packv5_042523_0143.root, FC#10, port B3
Entries 410
Mean 42.84
Std Dev 12.2
Turn on : 23.2204
Width : 2.206
Height : 10.010
Entry
ampl
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2
4
6
8
10
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0
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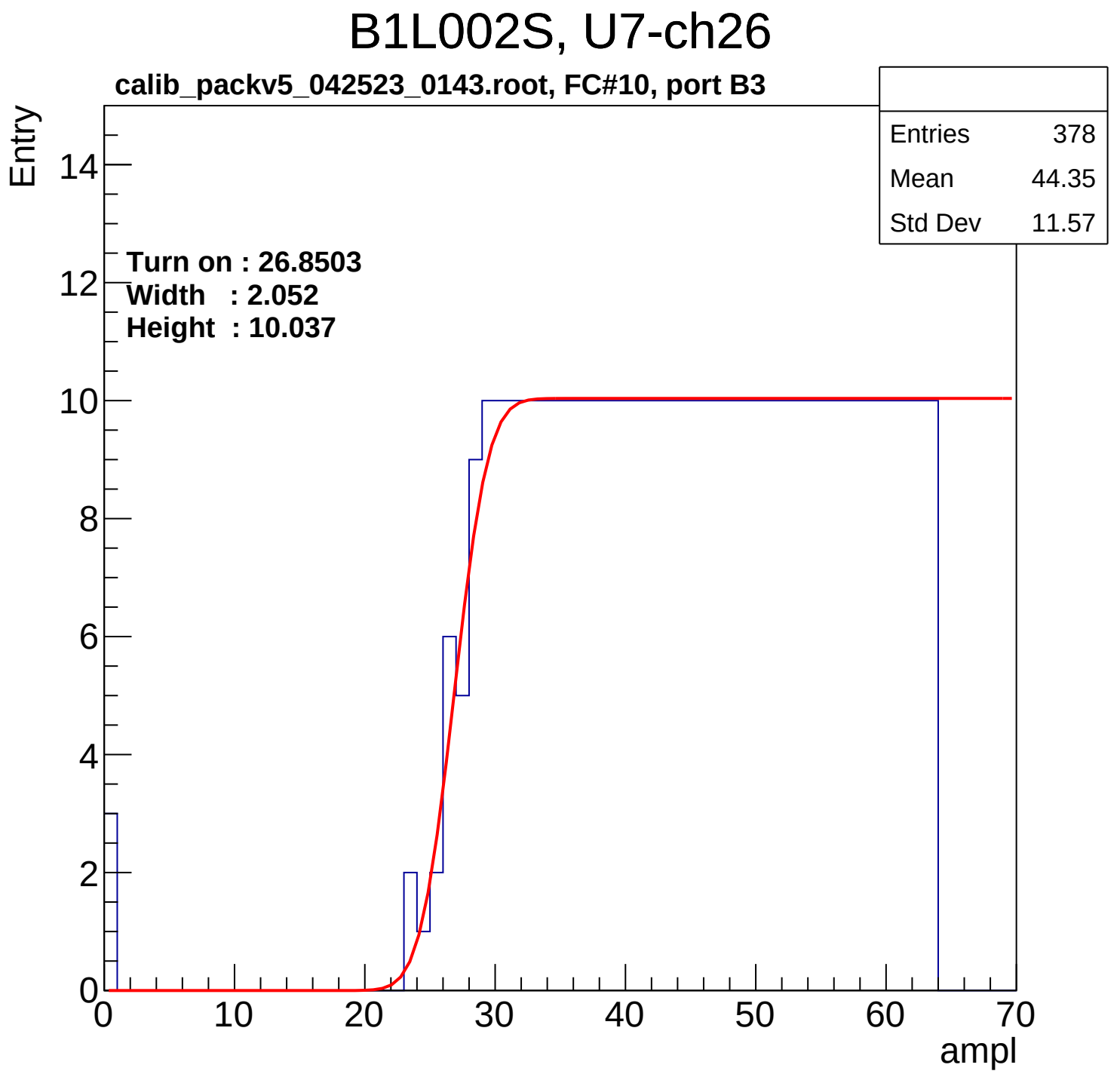
B1L002S, U7-ch26
calib_packv5_042523_0143.root, FC#10, port B3
Entries 378
Mean 44.35
Std Dev 11.57
Turn on : 26.8503
Width : 2.052
Height : 10.037
Entry
ampl
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2
4
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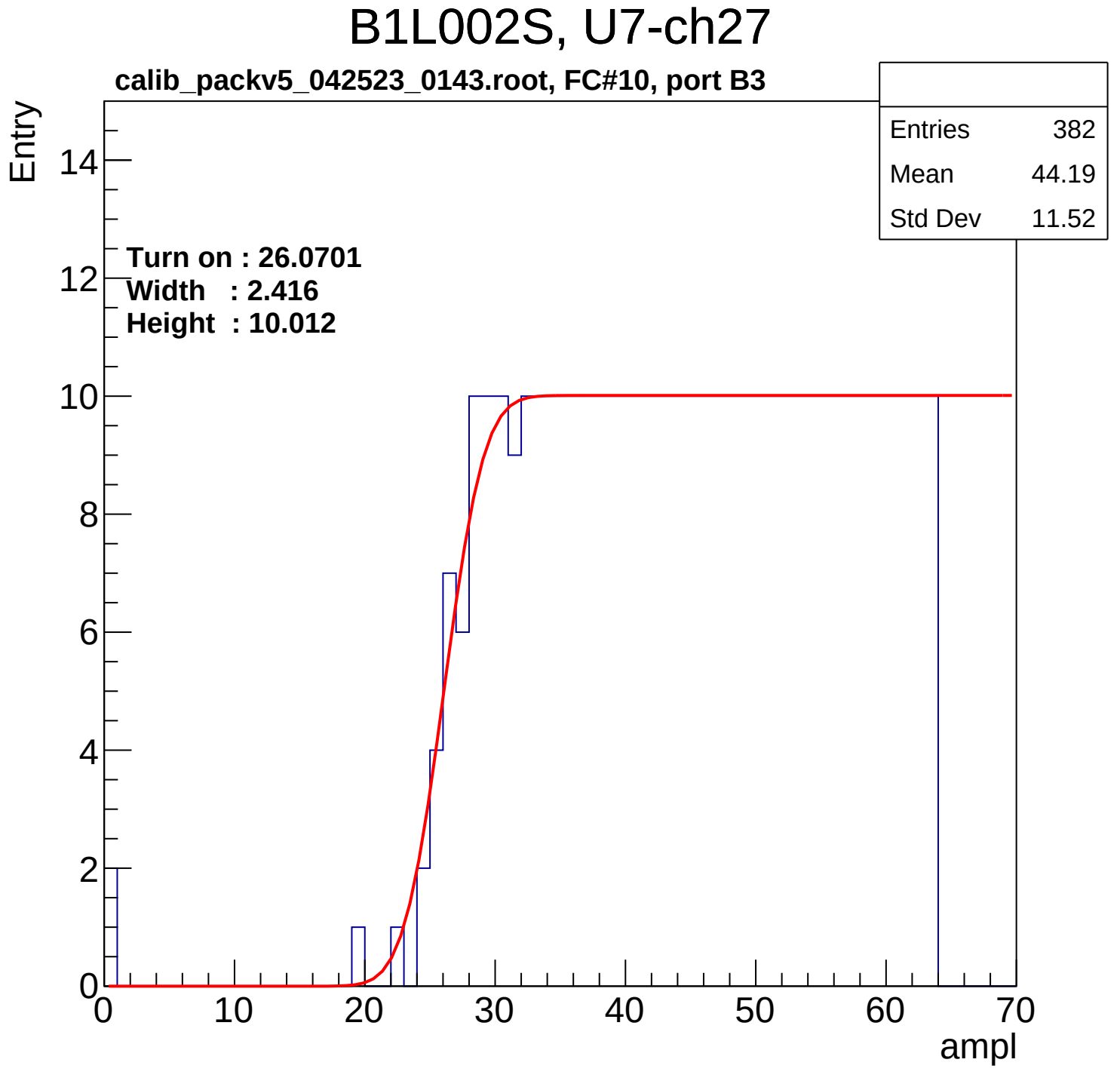
B1L002S, U7-ch27
calib_packv5_042523_0143.root, FC#10, port B3
Entries 382
Mean 44.19
Std Dev 11.52
Turn on : 26.0701
Width : 2.416
Height : 10.012
Entry
ampl
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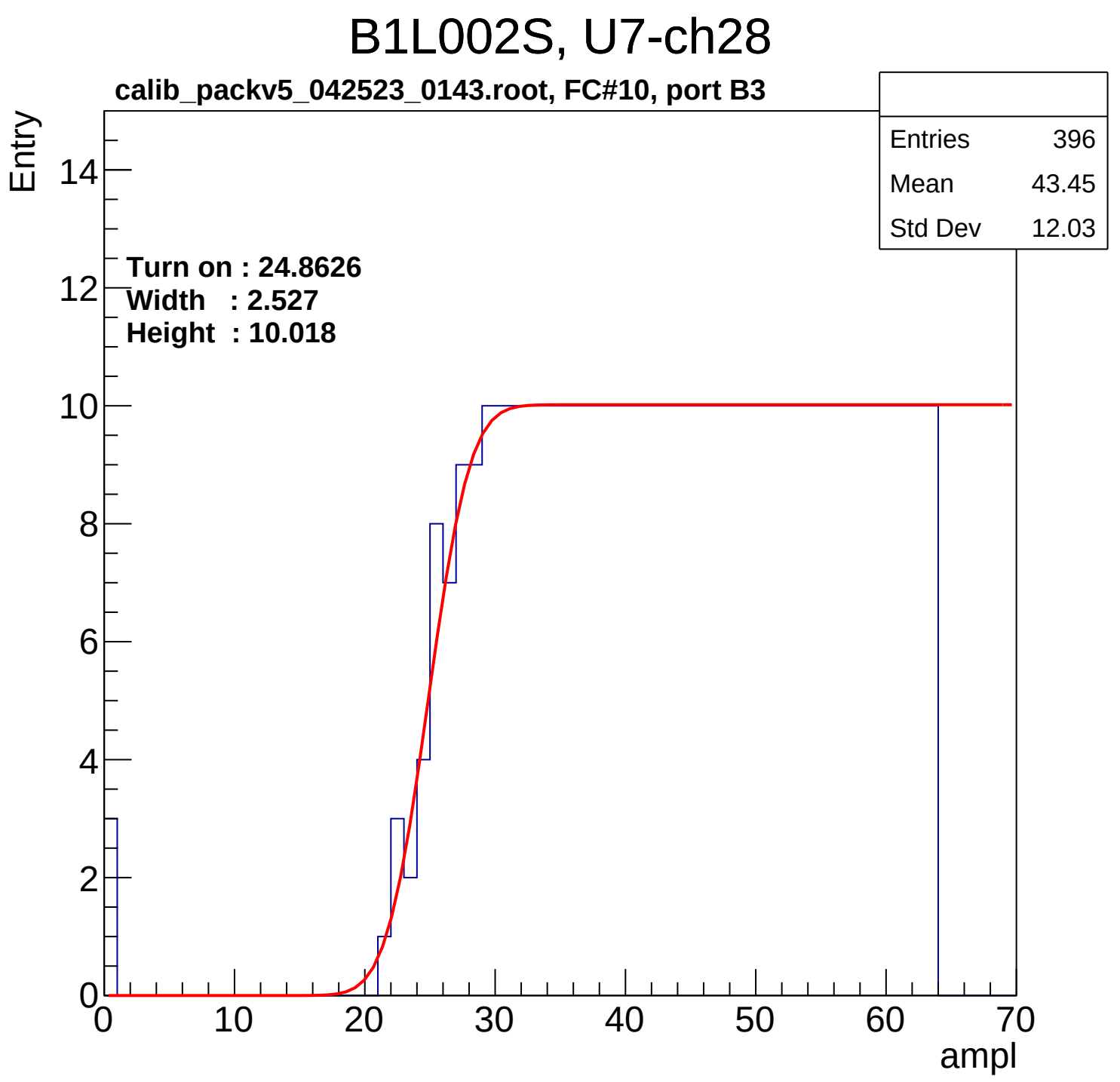
B1L002S, U7-ch28
calib_packv5_042523_0143.root, FC#10, port B3
Entries 396
Mean 43.45
Std Dev 12.03
Turn on : 24.8626
Width : 2.527
Height : 10.018
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
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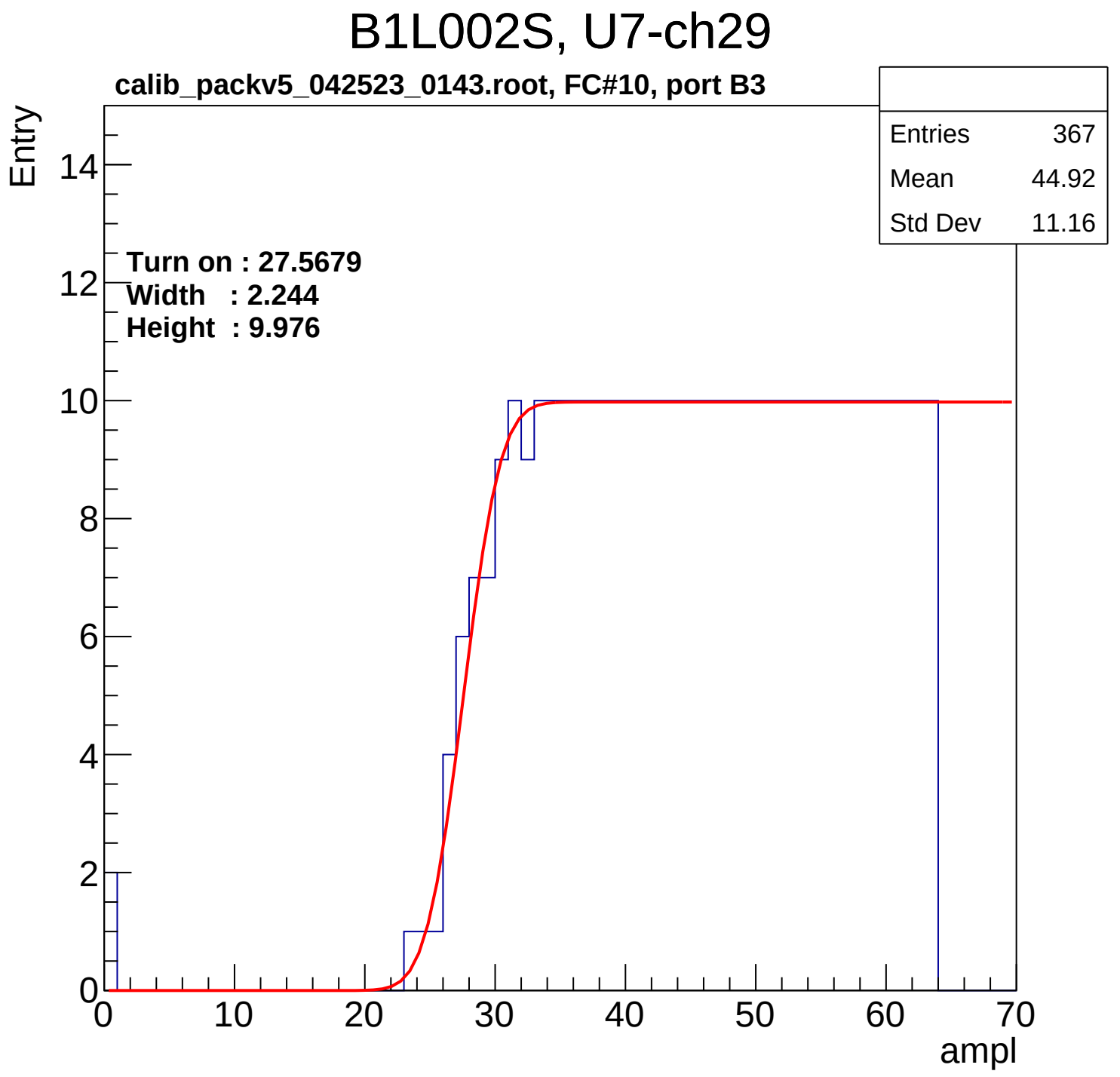
B1L002S, U7-ch29
calib_packv5_042523_0143.root, FC#10, port B3
Entries 367
Mean 44.92
Std Dev 11.16
Turn on : 27.5679
Width : 2.244
Height : 9.976
Entry
ampl
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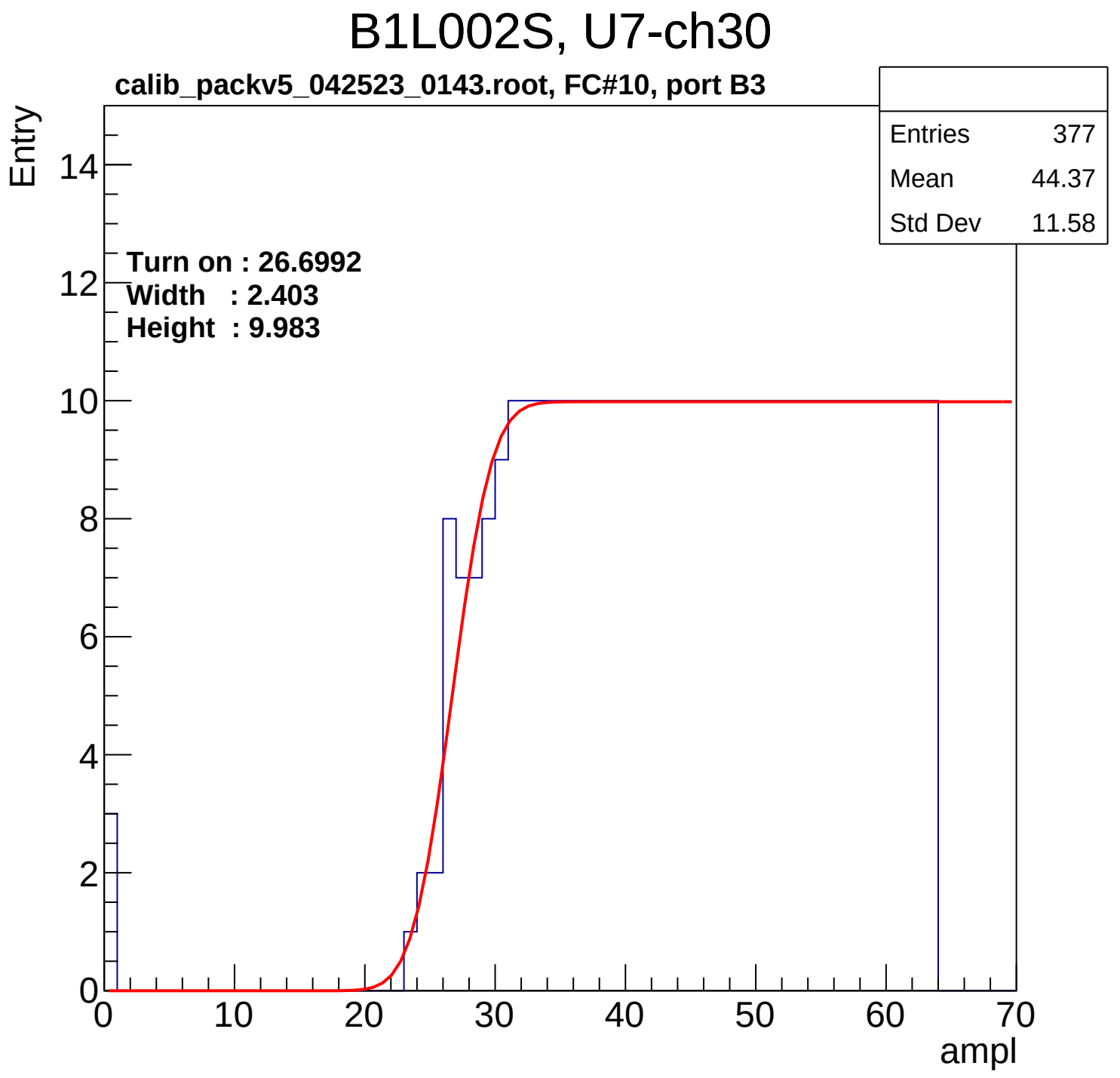
B1L002S, U7-ch30
calib_packv5_042523_0143.root, FC#10, port B3
Entries 377
Mean 44.37
Std Dev 11.58
Turn on : 26.6992
Width : 2.403
Height : 9.983
Entry
ampl
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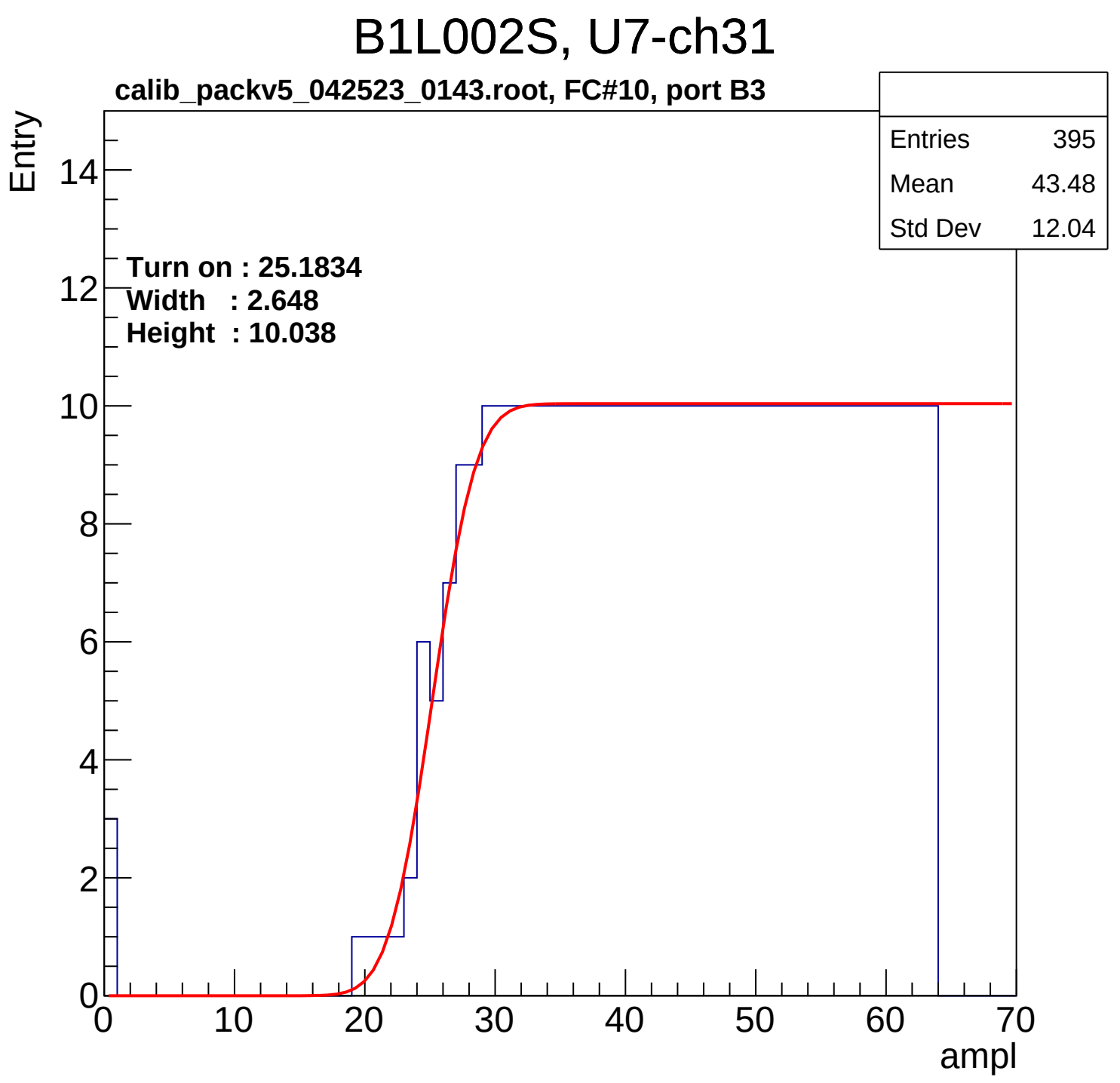
B1L002S, U7-ch31
calib_packv5_042523_0143.root, FC#10, port B3
Entries 395
Mean 43.48
Std Dev 12.04
Turn on : 25.1834
Width : 2.648
Height : 10.038
Entry
ampl
0
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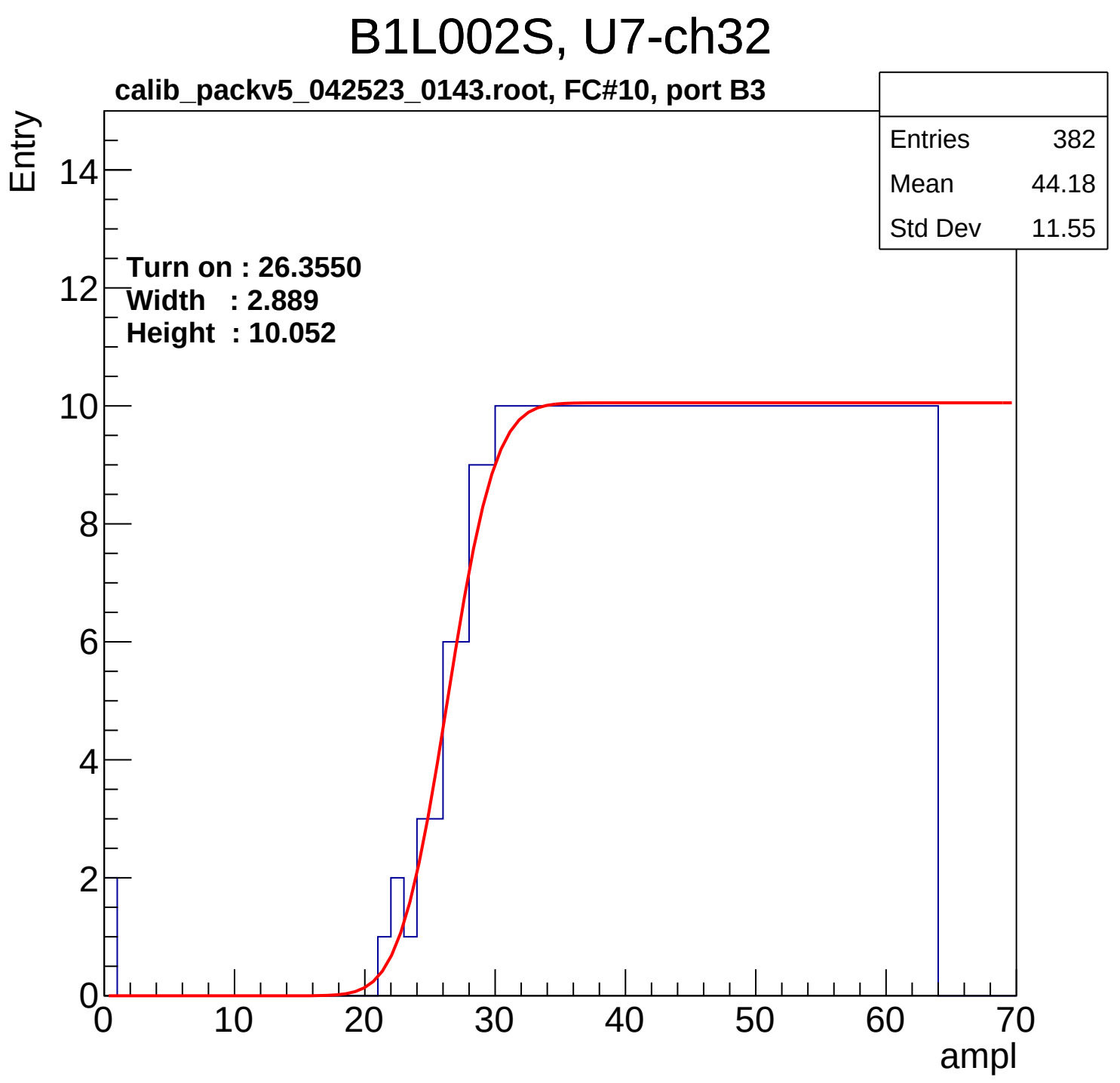
B1L002S, U7-ch32
calib_packv5_042523_0143.root, FC#10, port B3
Entries 382
Mean 44.18
Std Dev 11.55
Turn on : 26.3550
Width : 2.889
Height : 10.052
Entry
ampl
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2
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6
8
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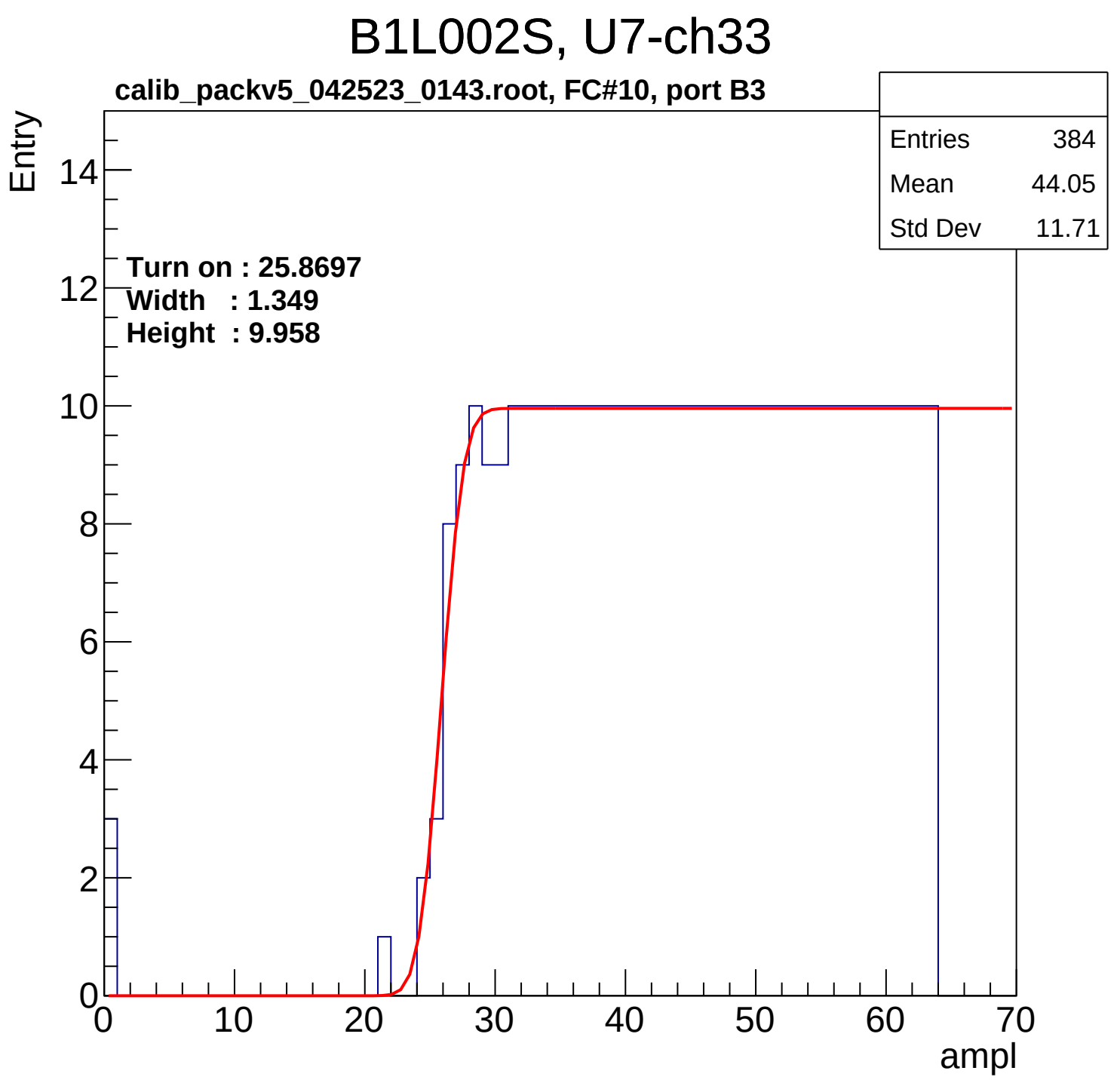
B1L002S, U7-ch33
calib_packv5_042523_0143.root, FC#10, port B3
Entries 384
Mean 44.05
Std Dev 11.71
Turn on : 25.8697
Width : 1.349
Height : 9.958
Entry
ampl
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2
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6
8
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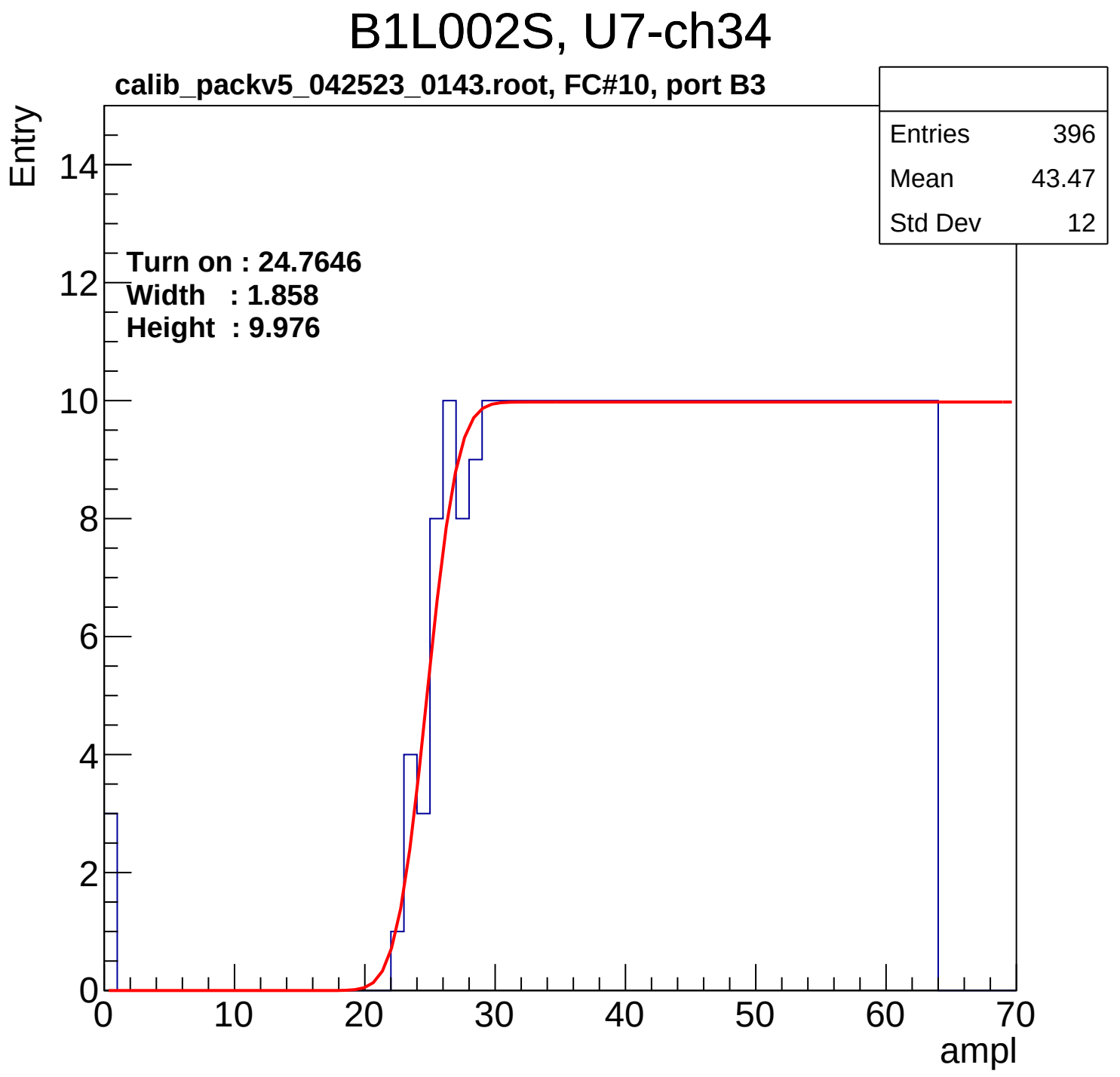
B1L002S, U7-ch34
calib_packv5_042523_0143.root, FC#10, port B3
Entries 396
Mean 43.47
Std Dev 12
Turn on : 24.7646
Width : 1.858
Height : 9.976
Entry
ampl
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2
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6
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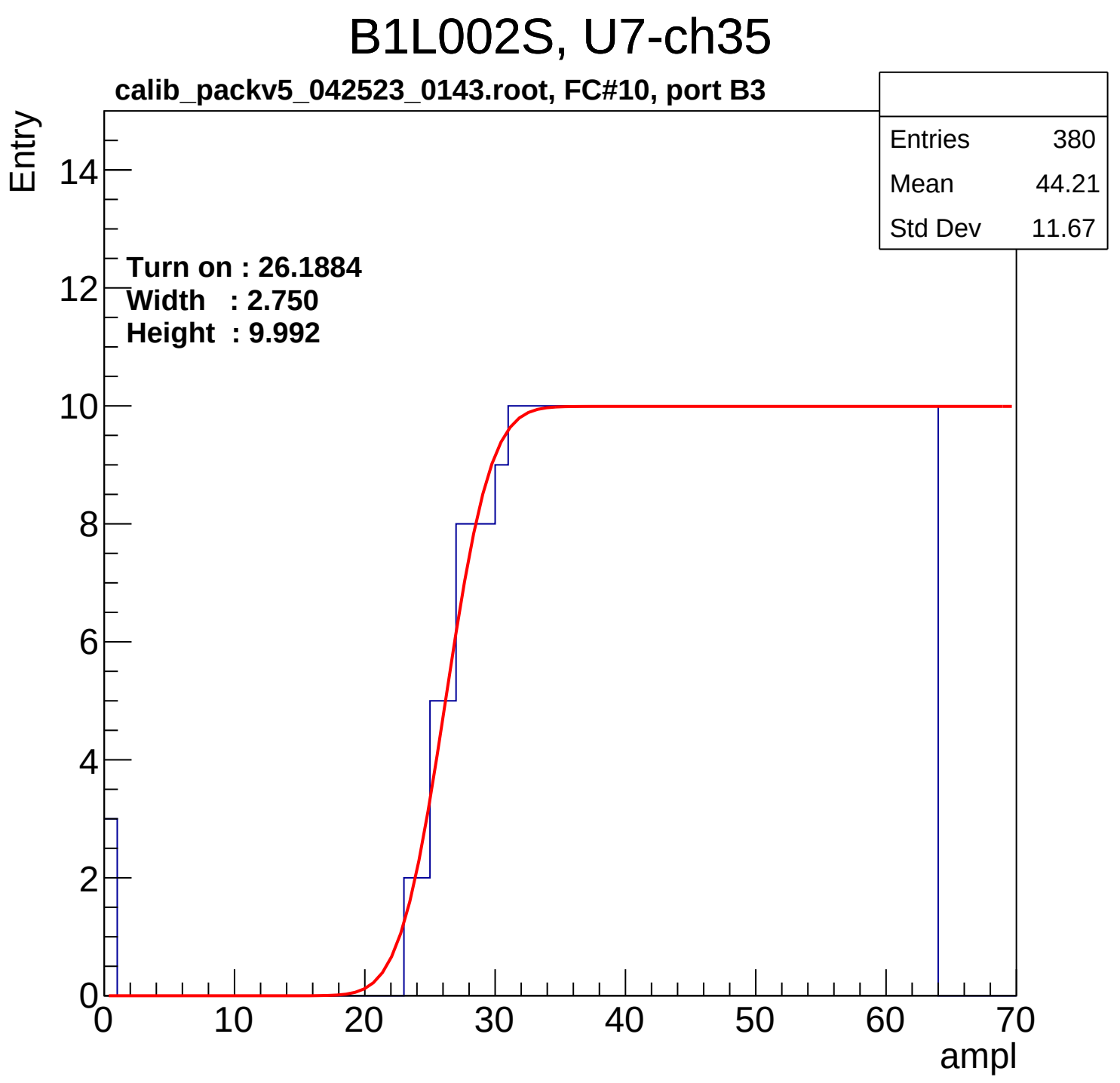
B1L002S, U7-ch35
calib_packv5_042523_0143.root, FC#10, port B3
Entries 380
Mean 44.21
Std Dev 11.67
Turn on : 26.1884
Width : 2.750
Height : 9.992
Entry
ampl
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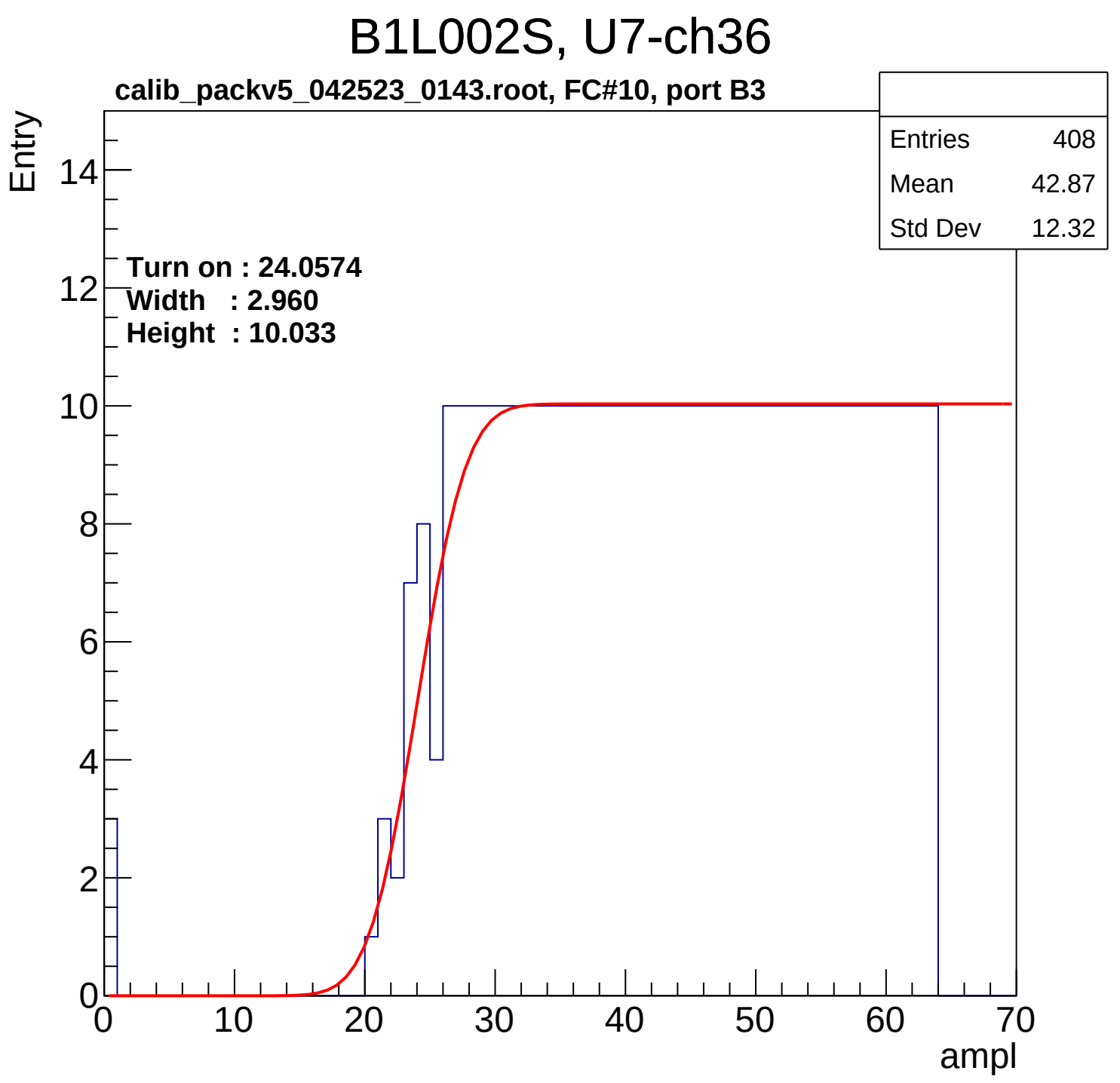
B1L002S, U7-ch36
calib_packv5_042523_0143.root, FC#10, port B3
Entries 408
Mean 42.87
Std Dev 12.32
Turn on : 24.0574
Width : 2.960
Height : 10.033
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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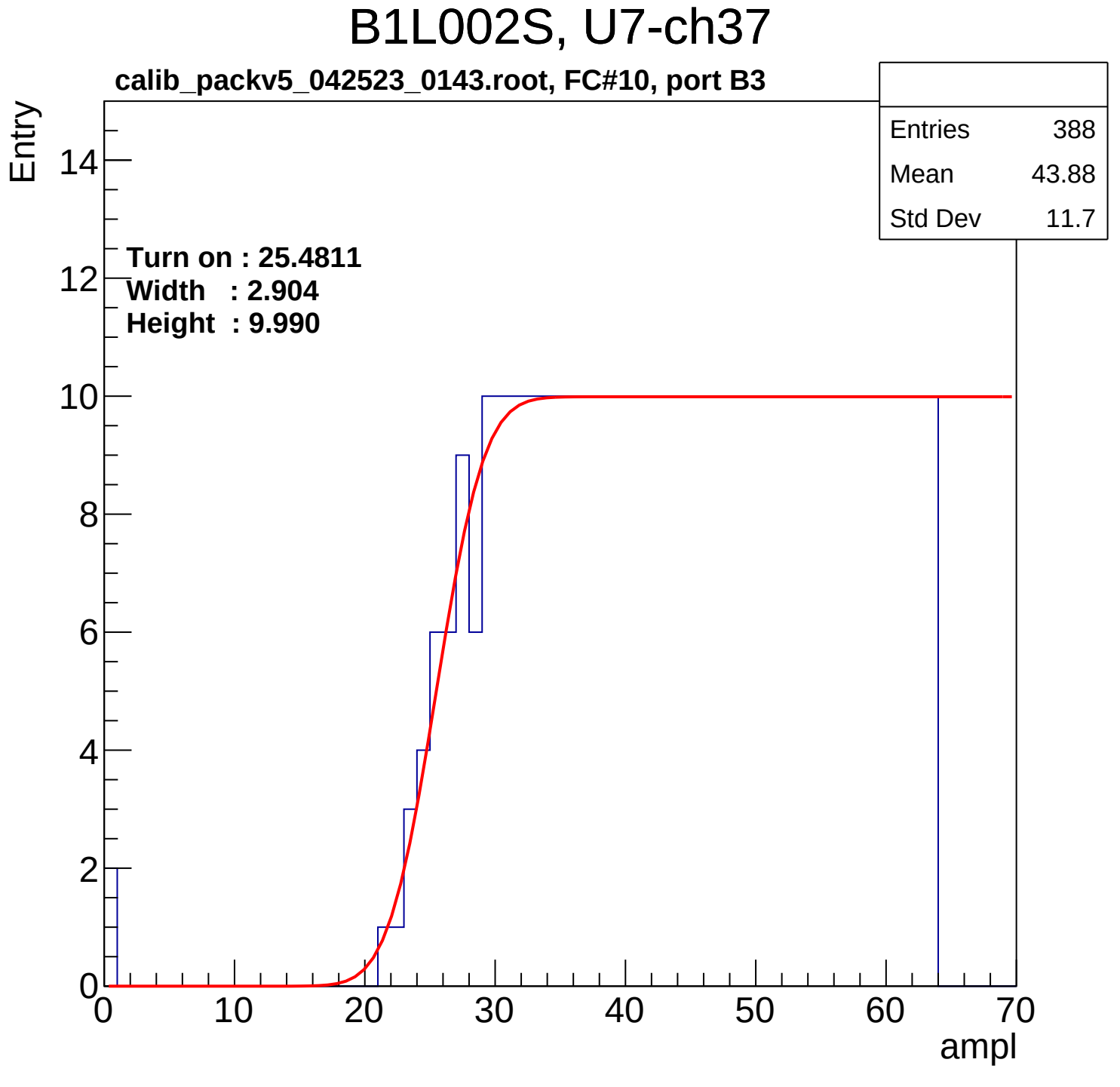
B1L002S, U7-ch37
calib_packv5_042523_0143.root, FC#10, port B3
Entries 388
Mean 43.88
Std Dev 11.7
Turn on : 25.4811
Width : 2.904
Height : 9.990
Entry
ampl
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2
4
6
8
10
12
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0
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60
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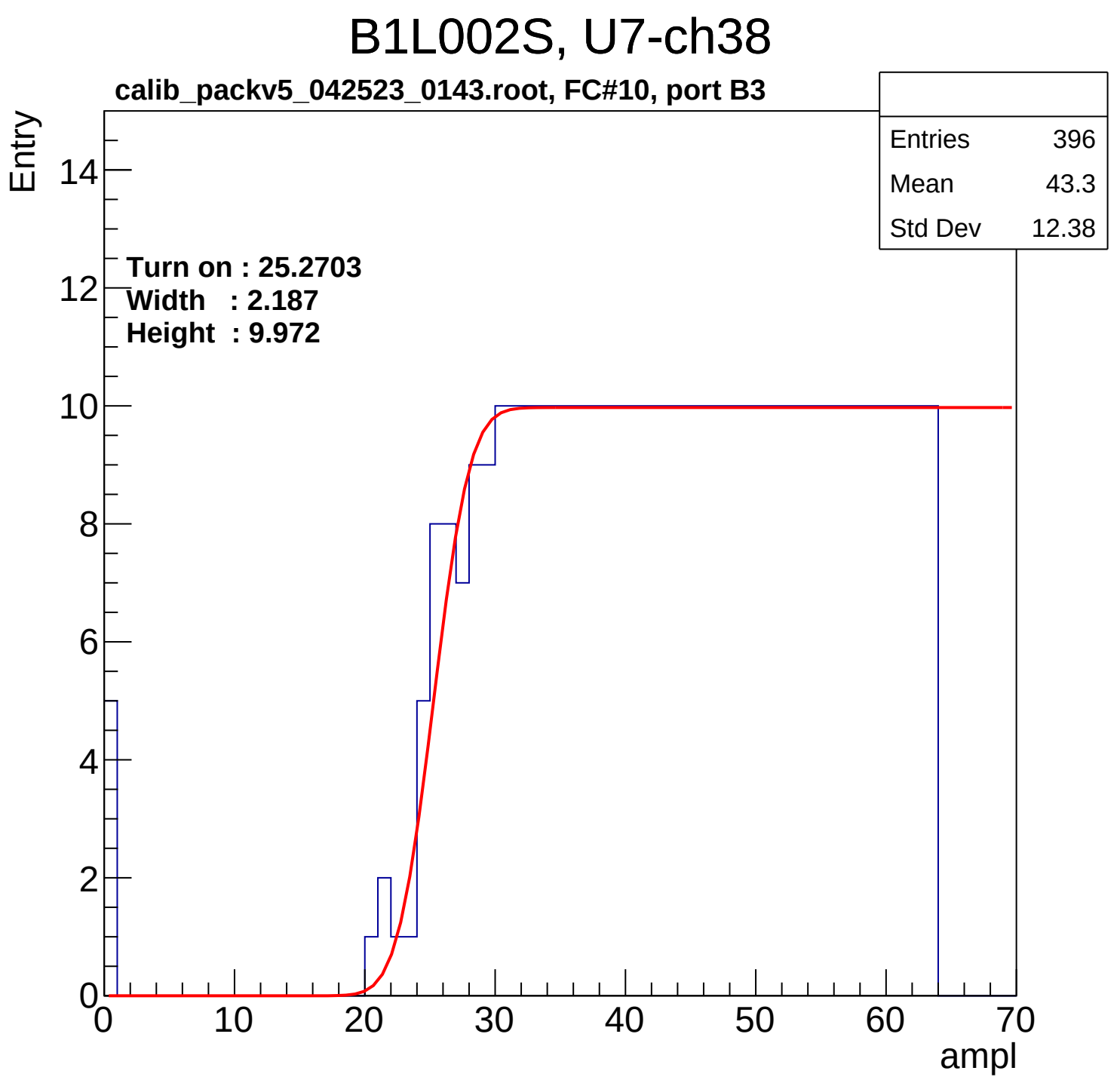
B1L002S, U7-ch38
calib_packv5_042523_0143.root, FC#10, port B3
Entries 396
Mean 43.3
Std Dev 12.38
Turn on : 25.2703
Width : 2.187
Height : 9.972
Entry
ampl
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2
4
6
8
10
12
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0
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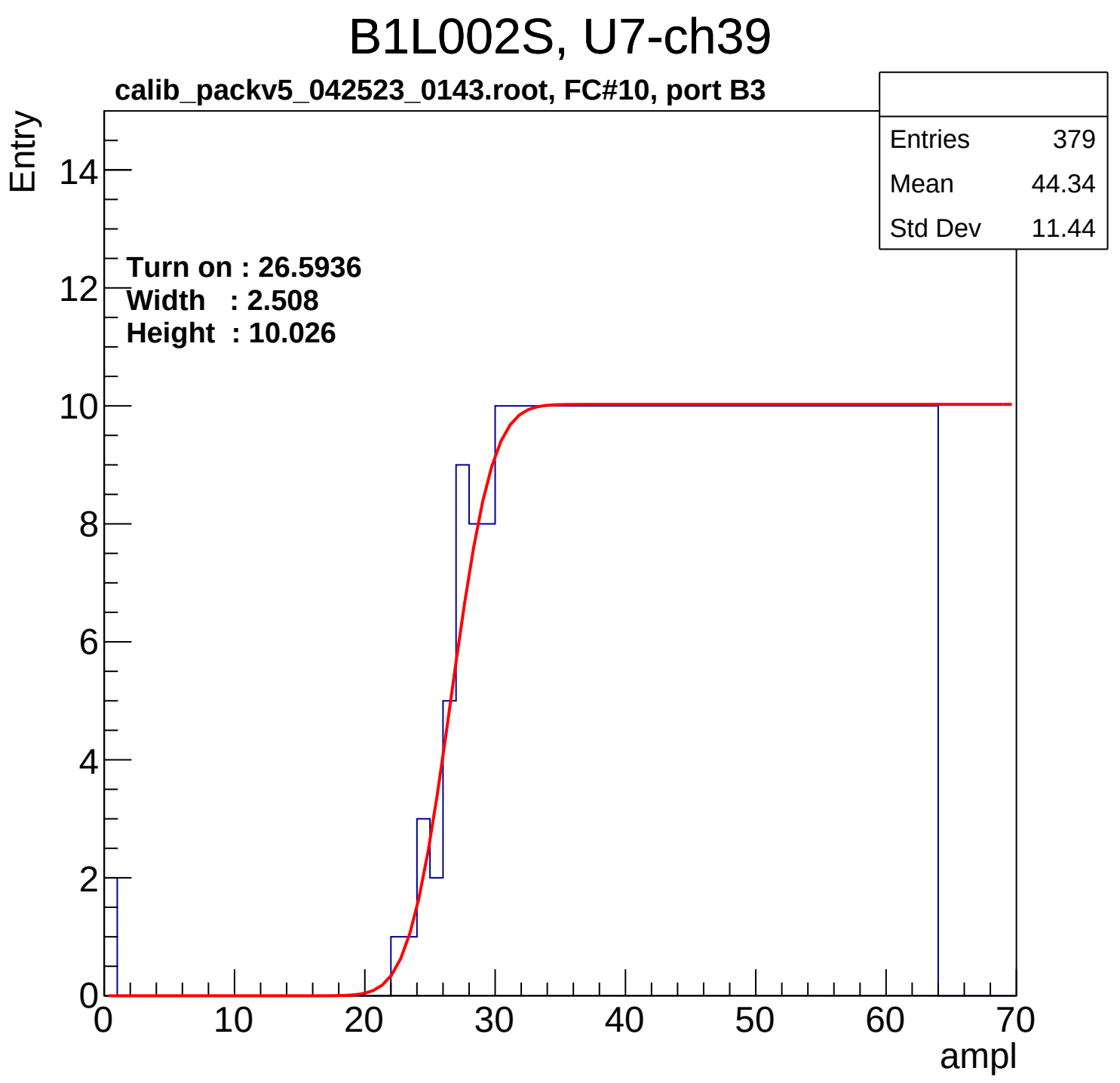
B1L002S, U7-ch39
calib_packv5_042523_0143.root, FC#10, port B3
Entries 379
Mean 44.34
Std Dev 11.44
Turn on : 26.5936
Width : 2.508
Height : 10.026
Entry
ampl
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6
8
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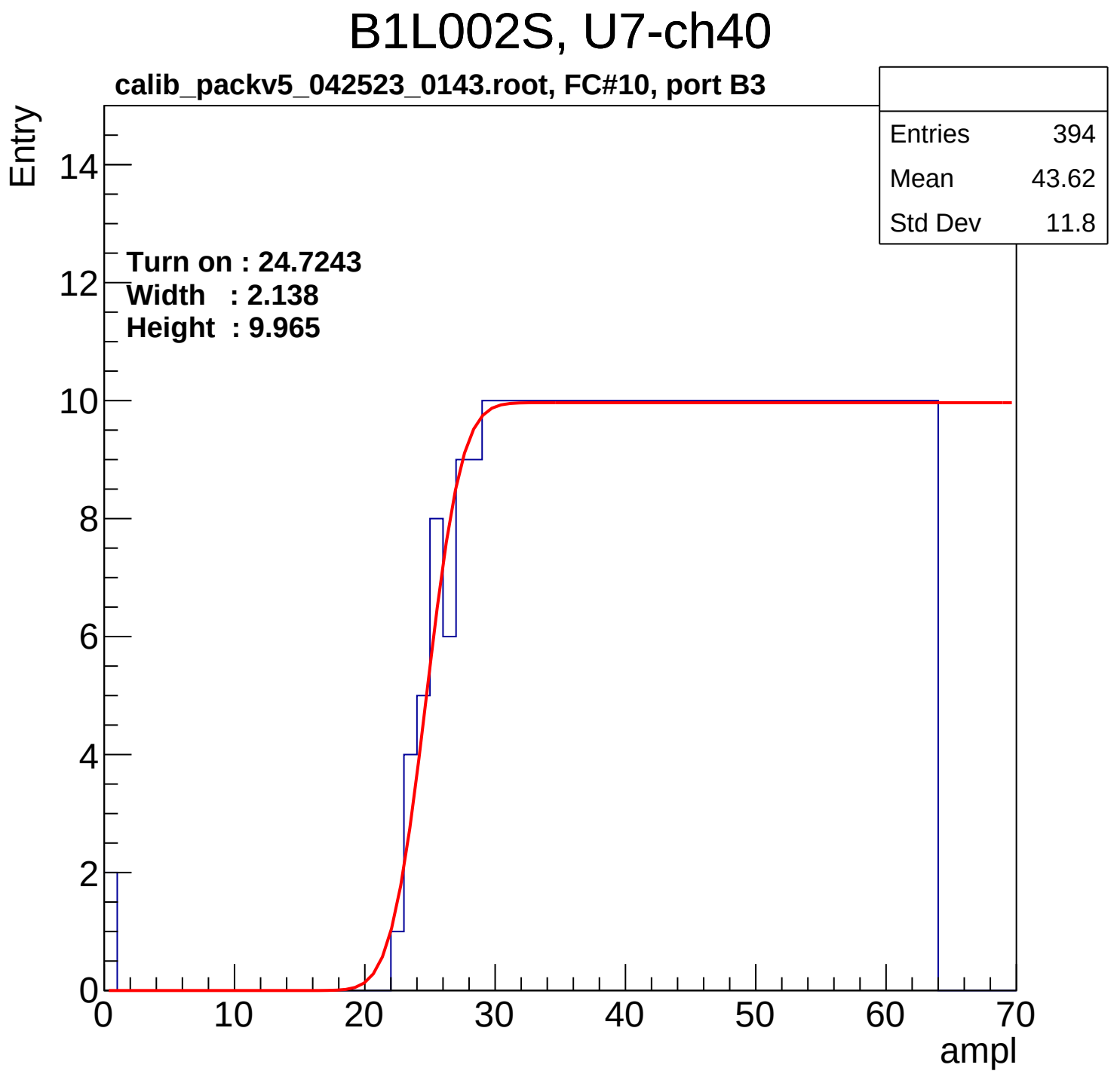
B1L002S, U7-ch40
calib_packv5_042523_0143.root, FC#10, port B3
Entries 394
Mean 43.62
Std Dev 11.8
Turn on : 24.7243
Width : 2.138
Height : 9.965
Entry
ampl
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6
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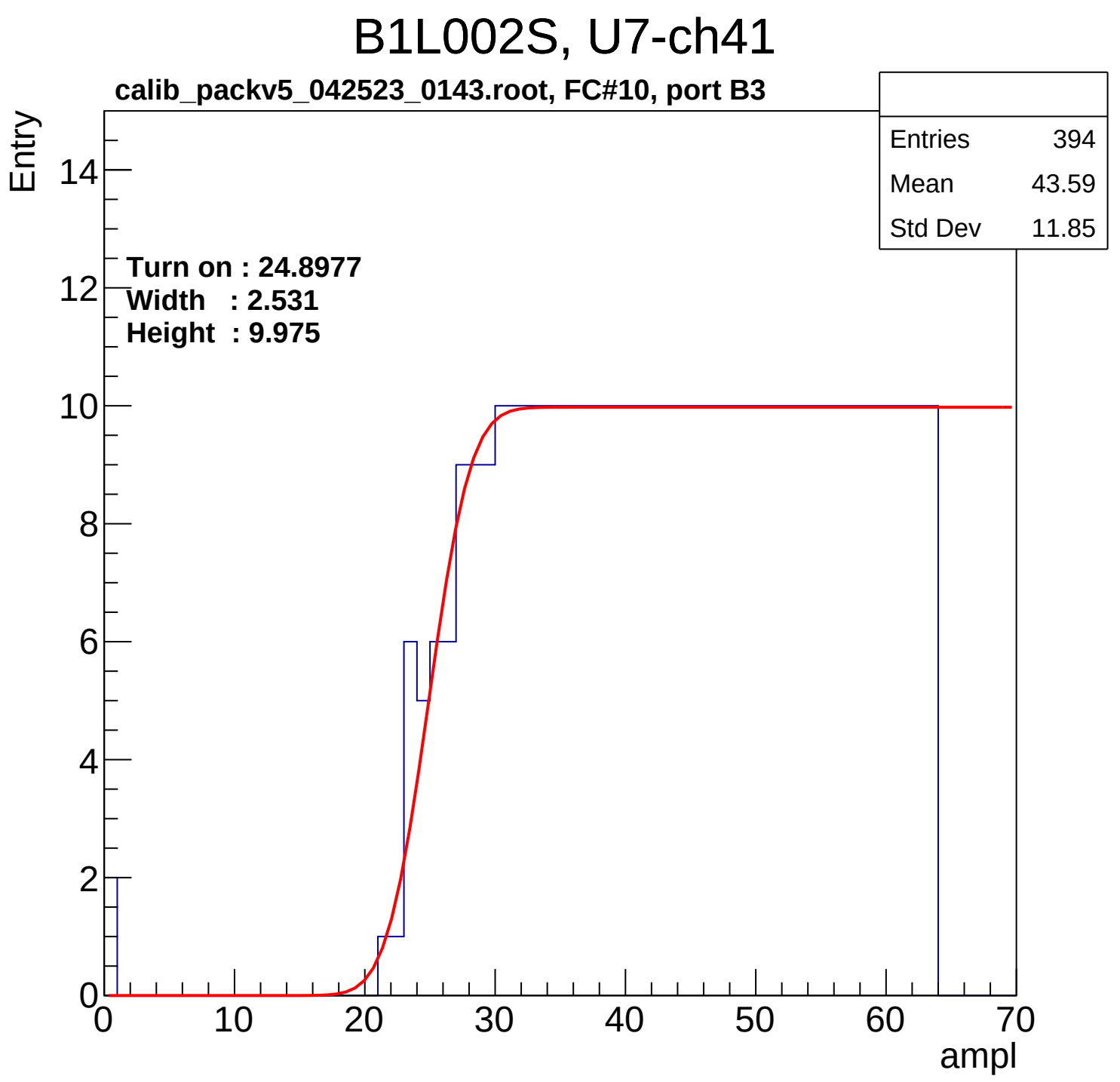
B1L002S, U7-ch41
calib_packv5_042523_0143.root, FC#10, port B3
Entries 394
Mean 43.59
Std Dev 11.85
Turn on : 24.8977
Width : 2.531
Height : 9.975
Entry
ampl
0
2
4
6
8
10
12
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0
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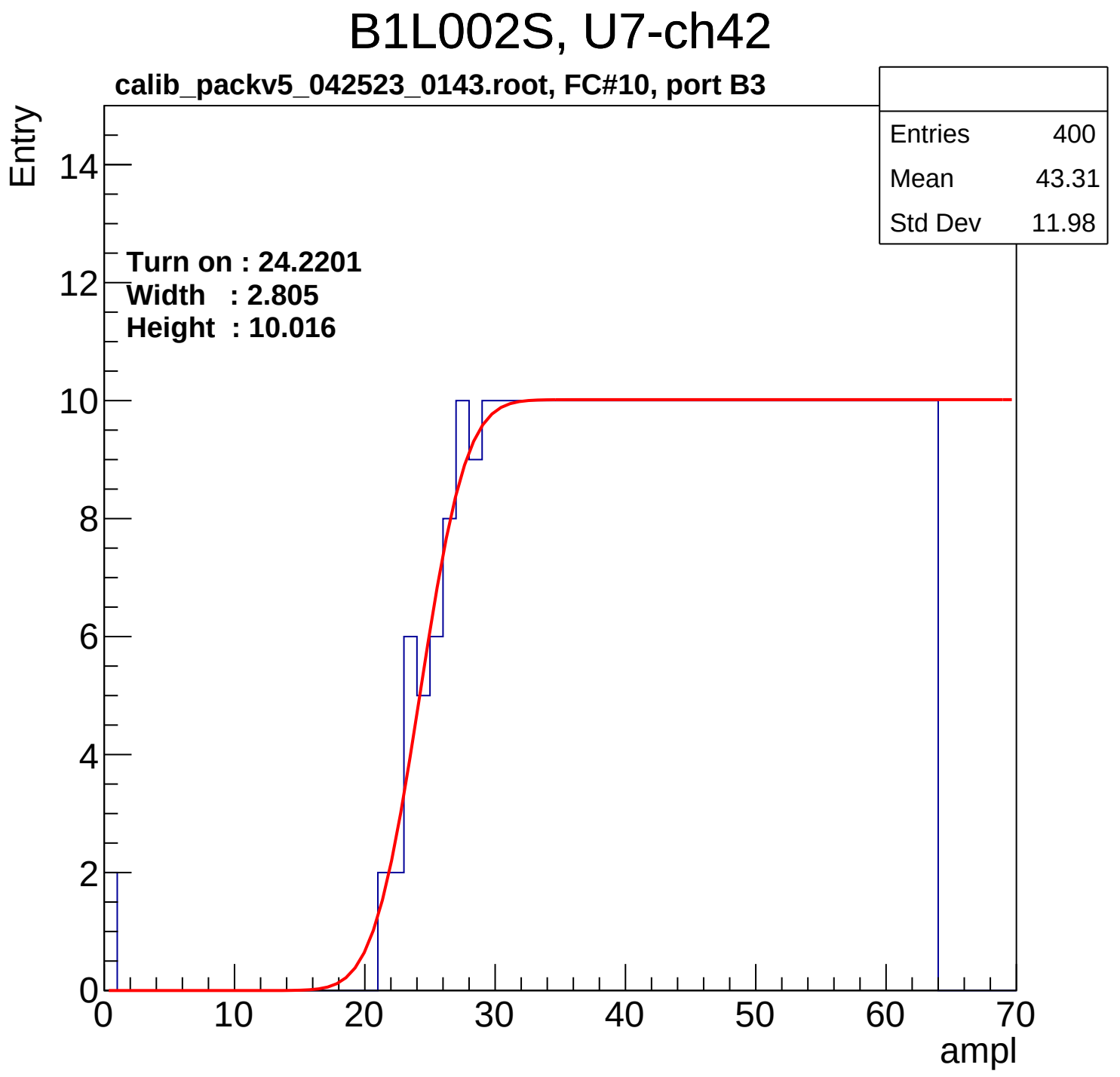
B1L002S, U7-ch42
calib_packv5_042523_0143.root, FC#10, port B3
Entries 400
Mean 43.31
Std Dev 11.98
Turn on : 24.2201
Width : 2.805
Height : 10.016
Entry
ampl
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6
8
10
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0
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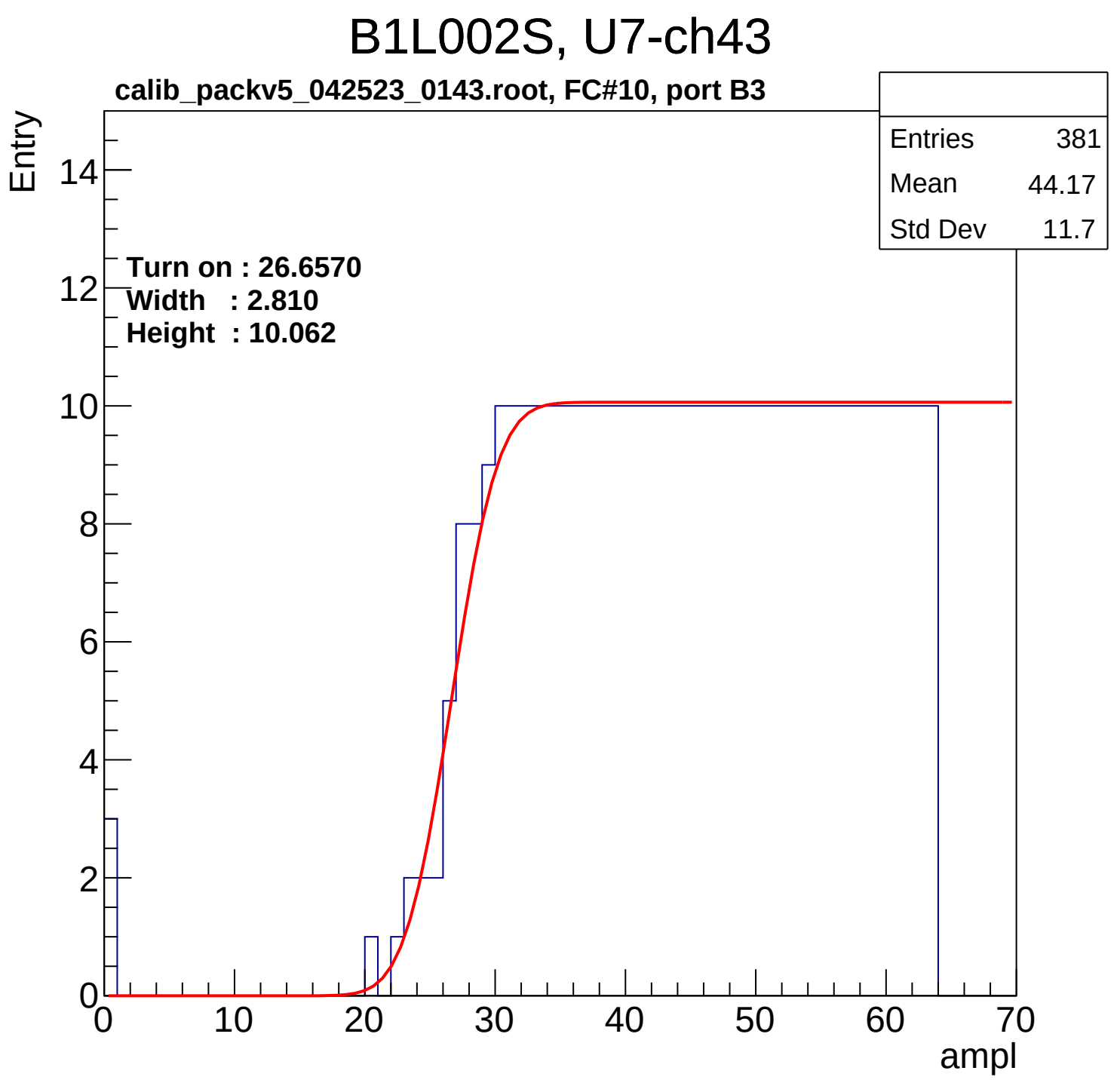
B1L002S, U7-ch43
calib_packv5_042523_0143.root, FC#10, port B3
Entries 381
Mean 44.17
Std Dev 11.7
Turn on : 26.6570
Width : 2.810
Height : 10.062
Entry
ampl
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6
8
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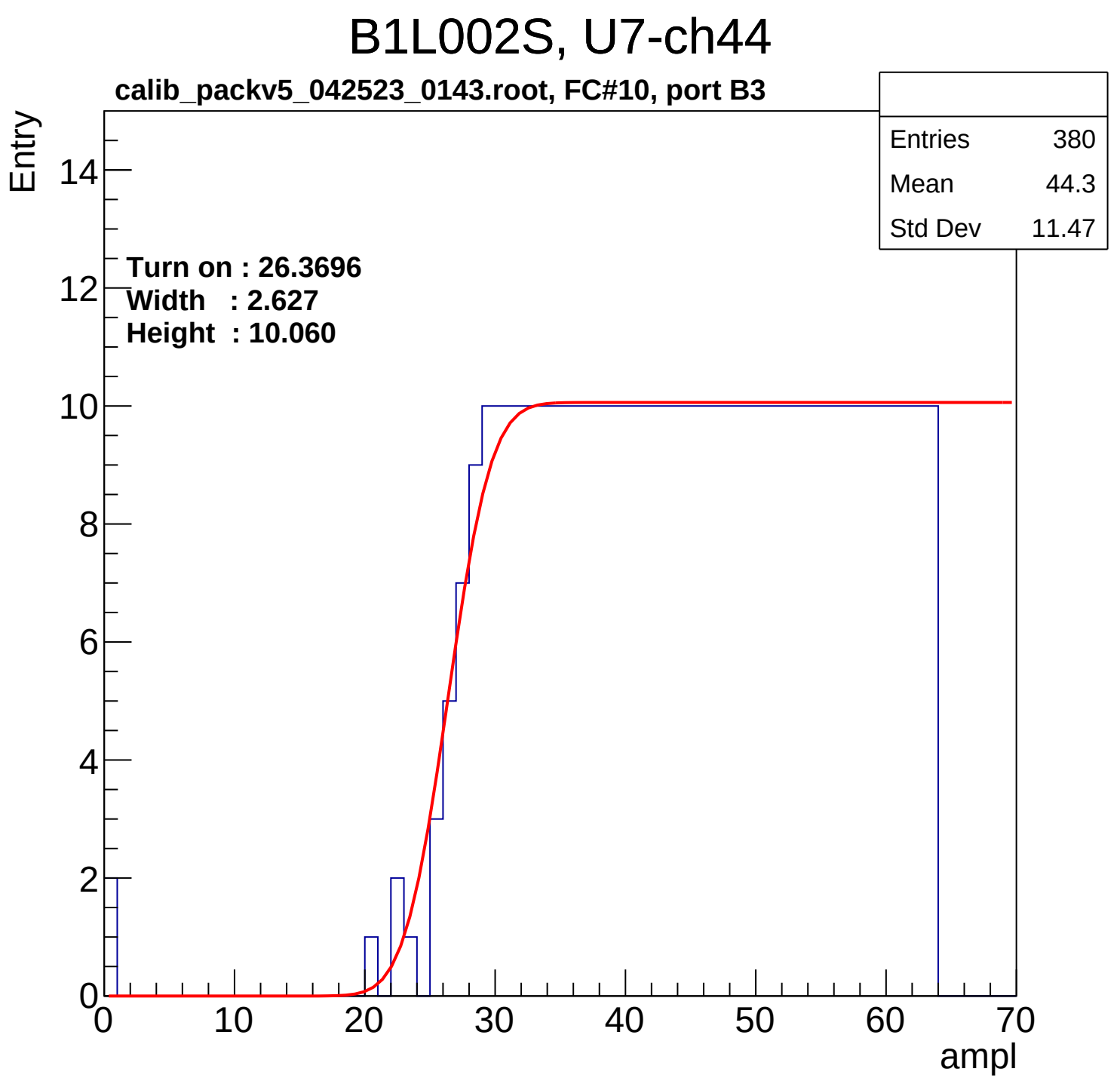
B1L002S, U7-ch44
calib_packv5_042523_0143.root, FC#10, port B3
Entries 380
Mean 44.3
Std Dev 11.47
Turn on : 26.3696
Width : 2.627
Height : 10.060
Entry
ampl
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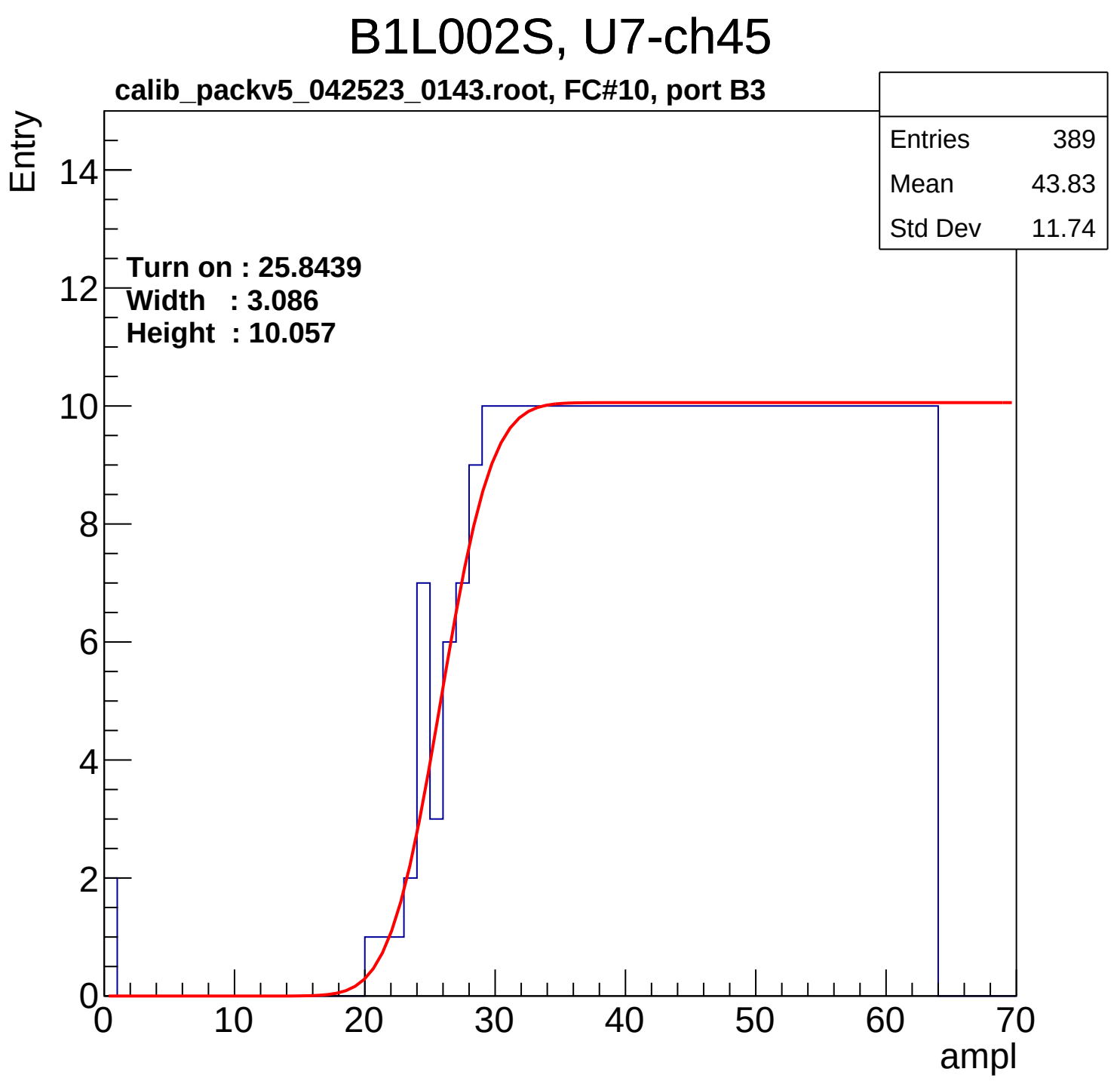
B1L002S, U7-ch45
calib_packv5_042523_0143.root, FC#10, port B3
Entries 389
Mean 43.83
Std Dev 11.74
Turn on : 25.8439
Width : 3.086
Height : 10.057
Entry
ampl
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6
8
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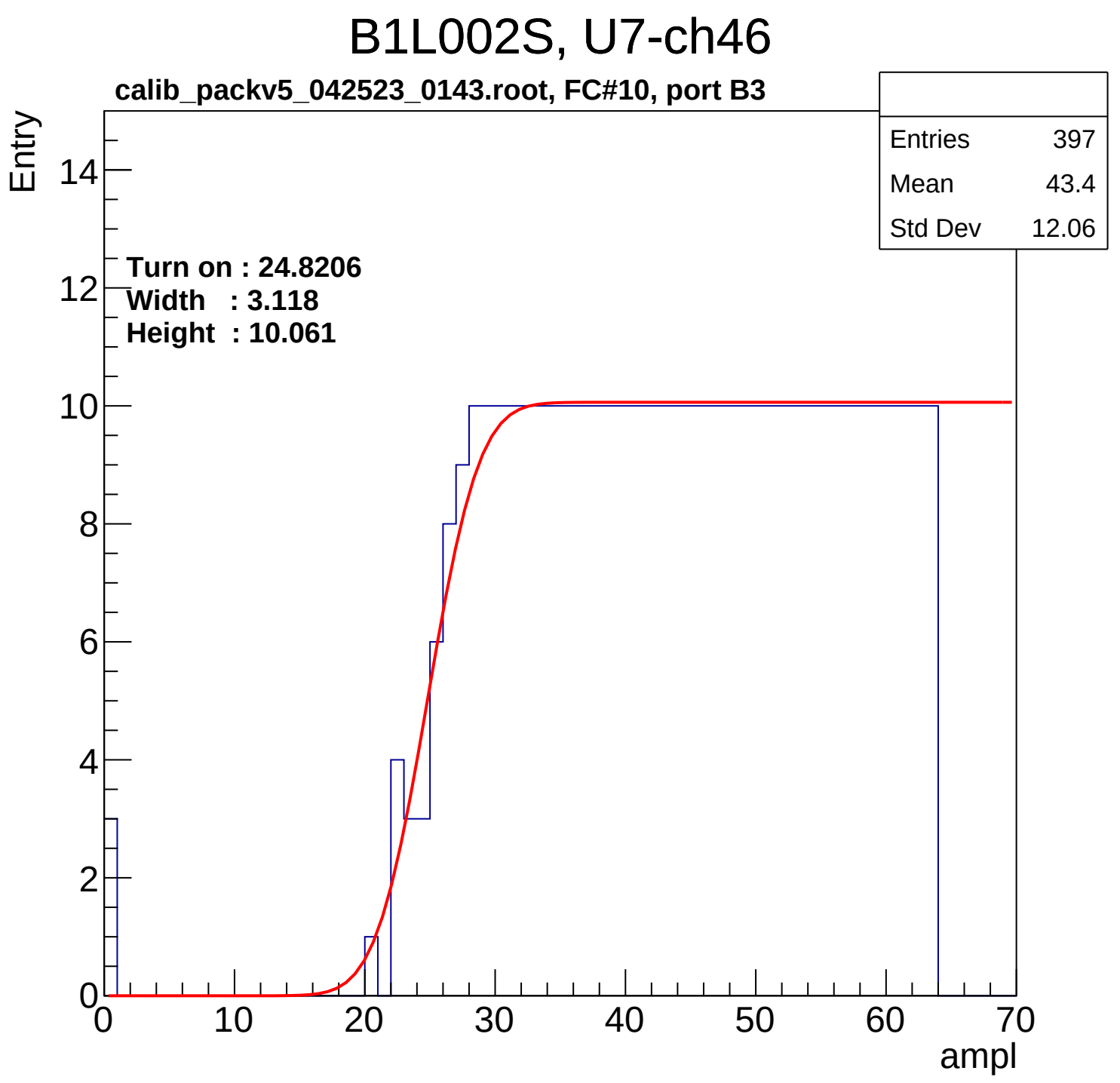
B1L002S, U7-ch46
calib_packv5_042523_0143.root, FC#10, port B3
Entries 397
Mean 43.4
Std Dev 12.06
Turn on : 24.8206
Width : 3.118
Height : 10.061
Entry
ampl
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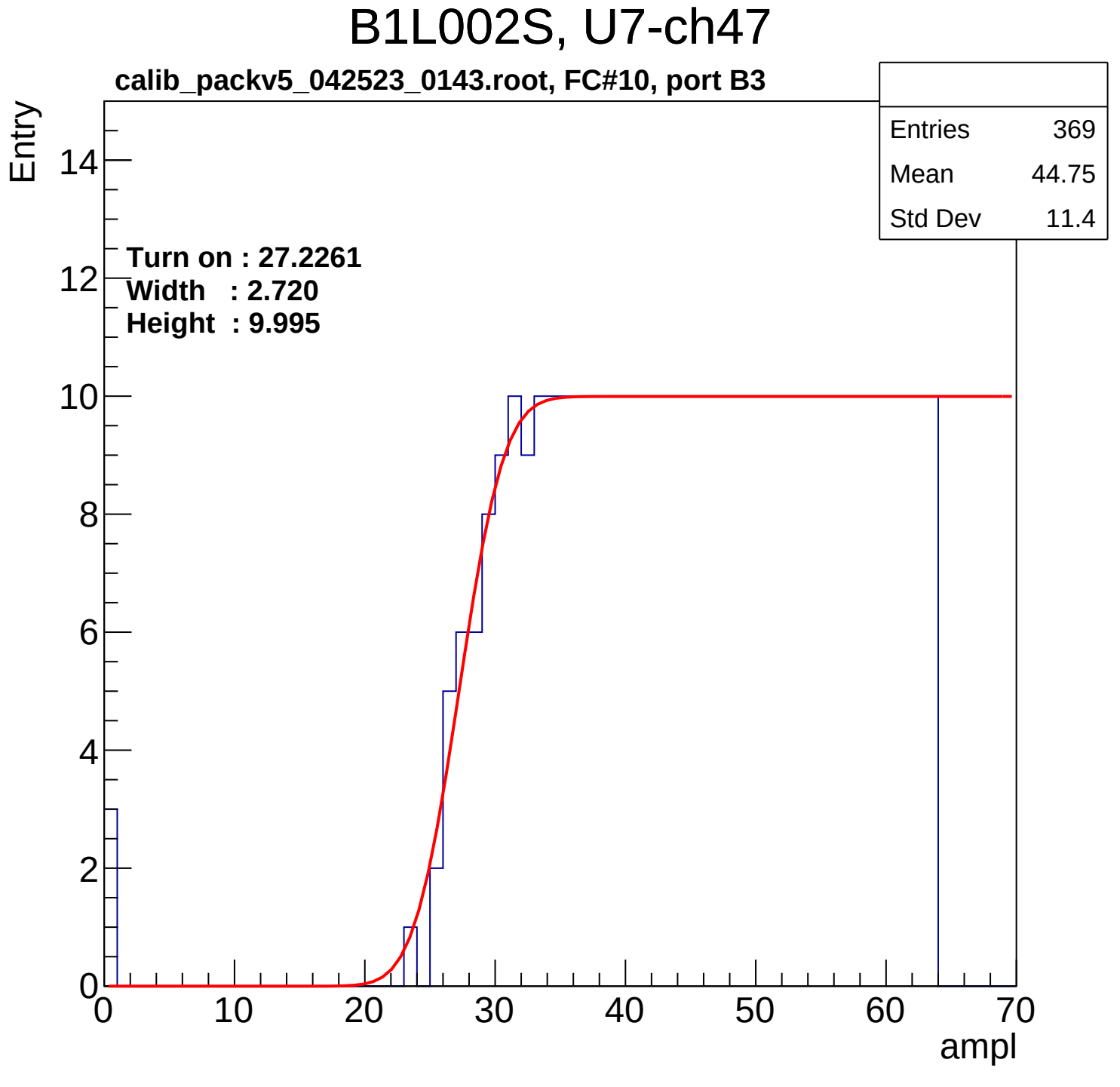
B1L002S, U7-ch47
calib_packv5_042523_0143.root, FC#10, port B3
Entries 369
Mean 44.75
Std Dev 11.4
Turn on : 27.2261
Width : 2.720
Height : 9.995
Entry
ampl
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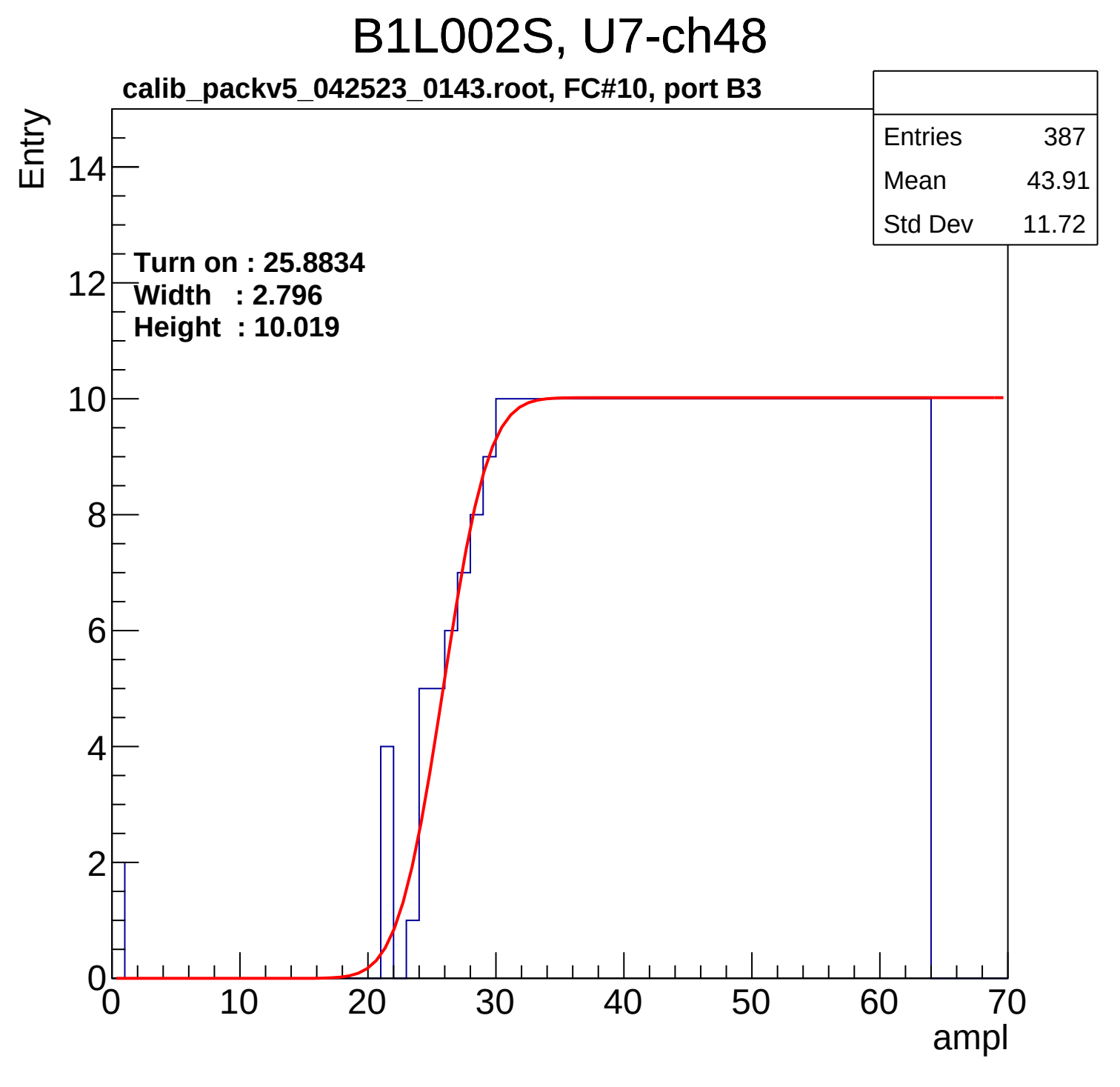
B1L002S, U7-ch48
calib_packv5_042523_0143.root, FC#10, port B3
Entries 387
Mean 43.91
Std Dev 11.72
Turn on : 25.8834
Width : 2.796
Height : 10.019
Entry
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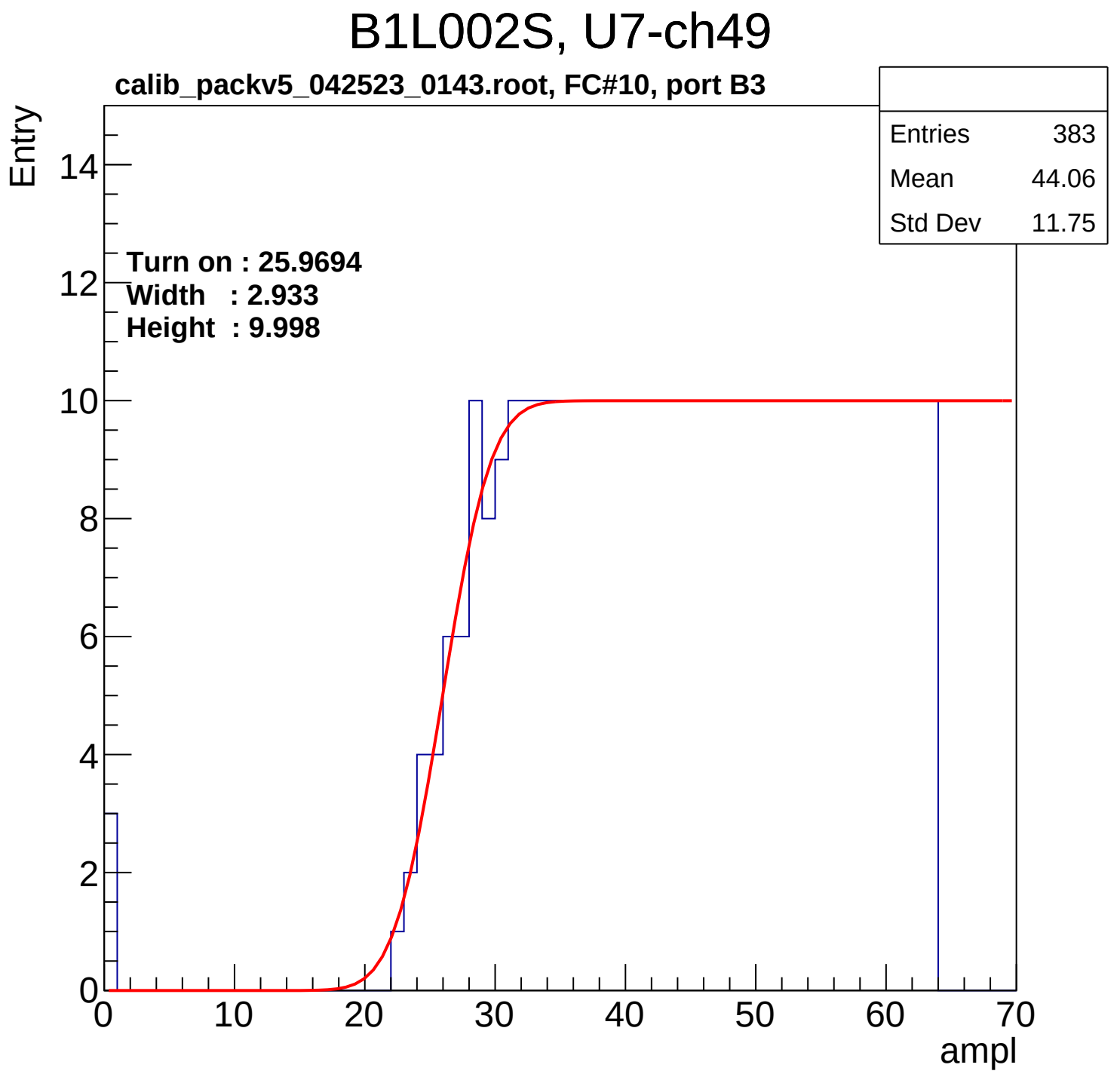
B1L002S, U7-ch49
calib_packv5_042523_0143.root, FC#10, port B3
Entries 383
Mean 44.06
Std Dev 11.75
Turn on : 25.9694
Width : 2.933
Height : 9.998
Entry
ampl
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8
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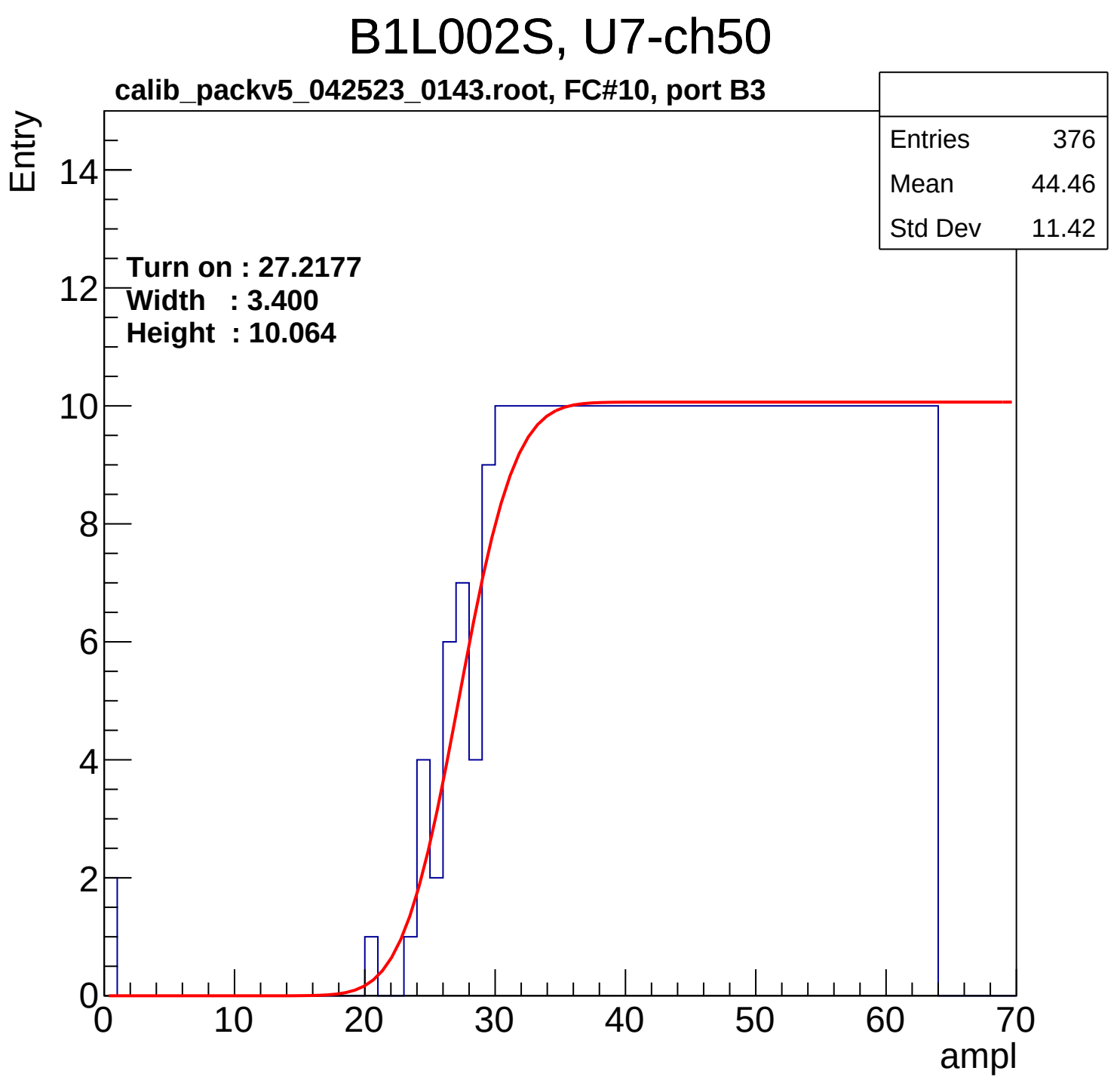
B1L002S, U7-ch50
calib_packv5_042523_0143.root, FC#10, port B3
Entries 376
Mean 44.46
Std Dev 11.42
Turn on : 27.2177
Width : 3.400
Height : 10.064
Entry
ampl
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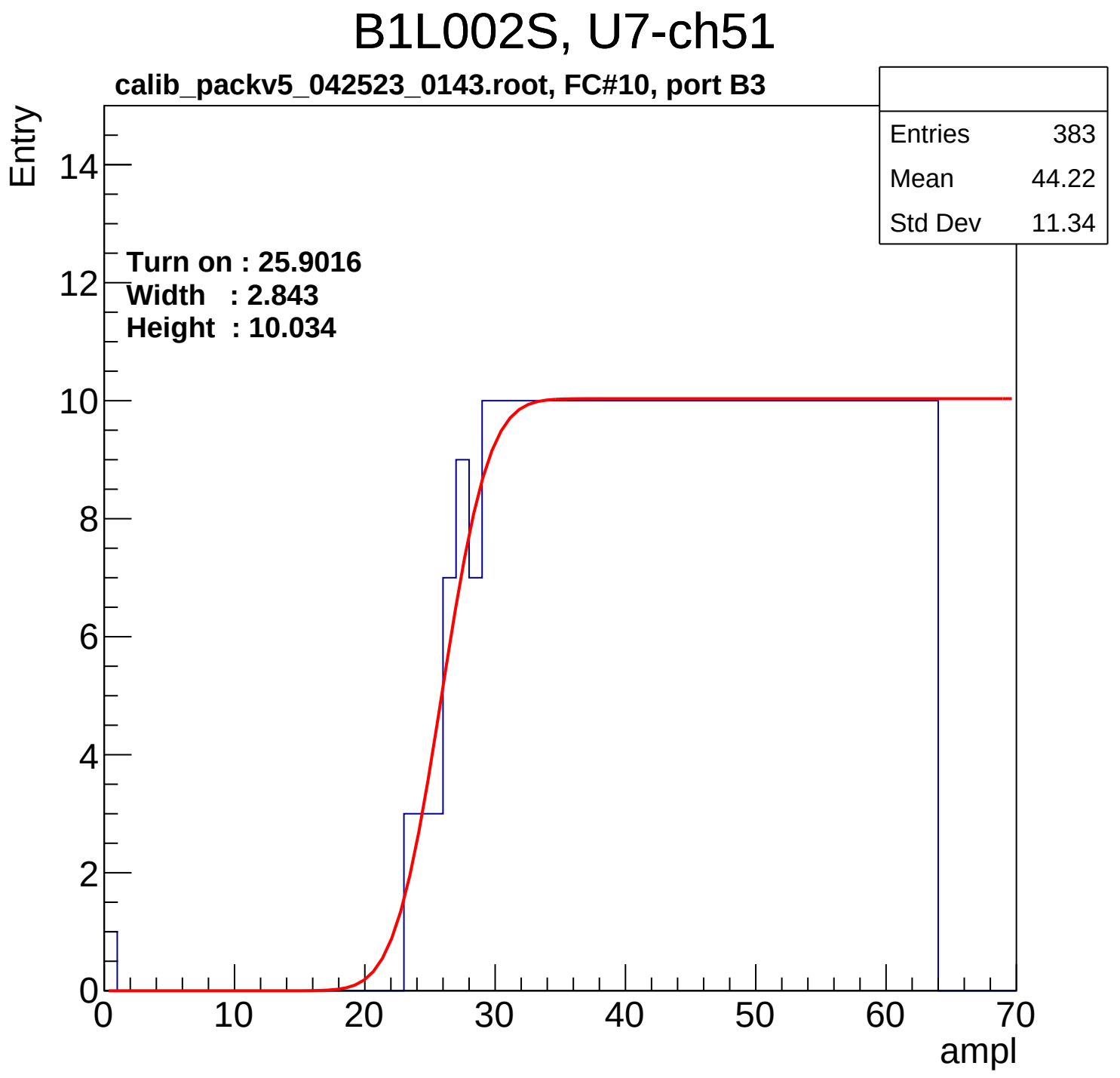
B1L002S, U7-ch51
calib_packv5_042523_0143.root, FC#10, port B3
Entries 383
Mean 44.22
Std Dev 11.34
Turn on : 25.9016
Width : 2.843
Height : 10.034
Entry
ampl
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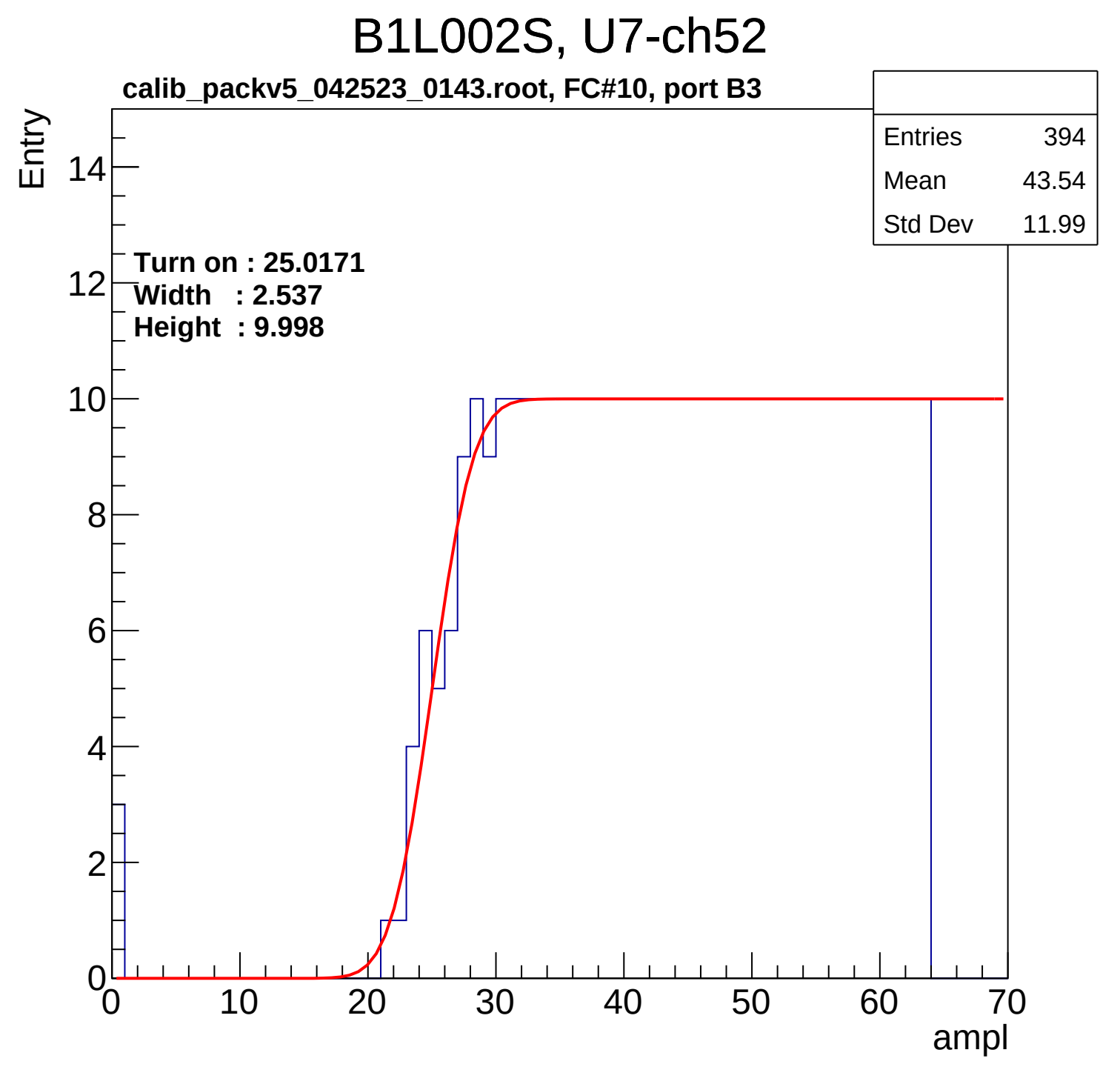
B1L002S, U7-ch52
calib_packv5_042523_0143.root, FC#10, port B3
Entries 394
Mean 43.54
Std Dev 11.99
Turn on : 25.0171
Width : 2.537
Height : 9.998
Entry
ampl
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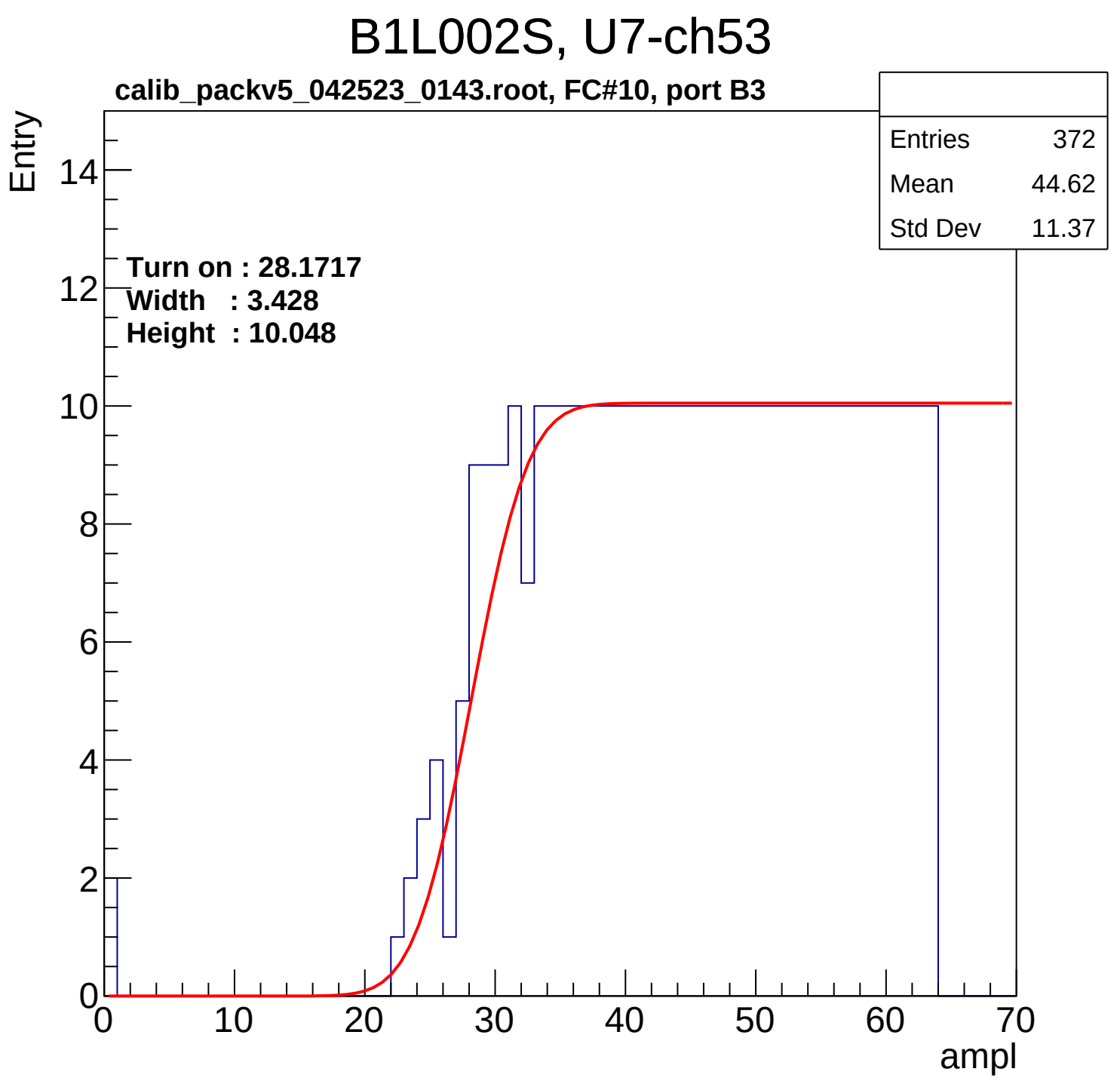
B1L002S, U7-ch53
calib_packv5_042523_0143.root, FC#10, port B3
Entries 372
Mean 44.62
Std Dev 11.37
Turn on : 28.1717
Width : 3.428
Height : 10.048
Entry
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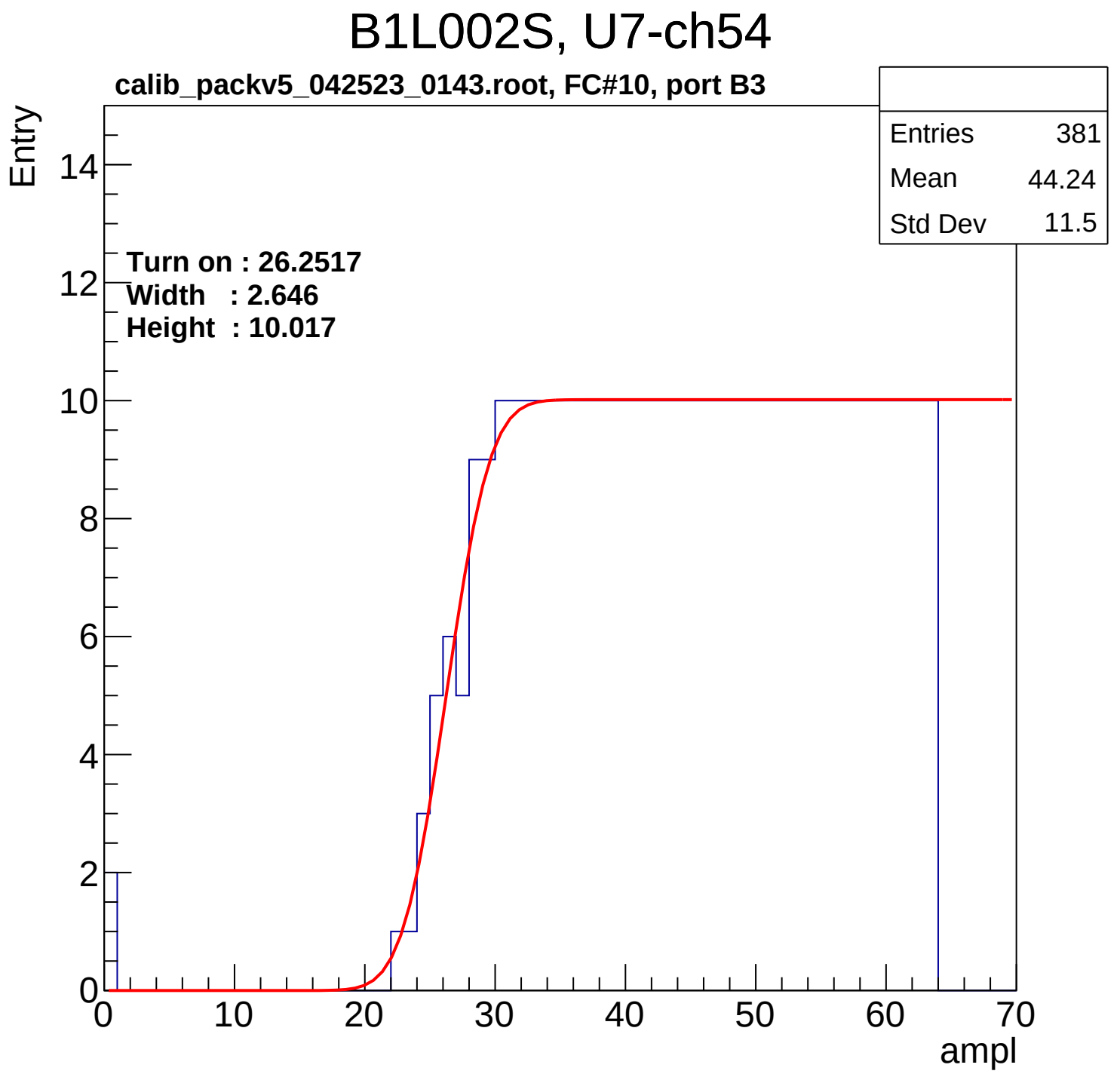
B1L002S, U7-ch54
calib_packv5_042523_0143.root, FC#10, port B3
Entries 381
Mean 44.24
Std Dev 11.5
Turn on : 26.2517
Width : 2.646
Height : 10.017
Entry
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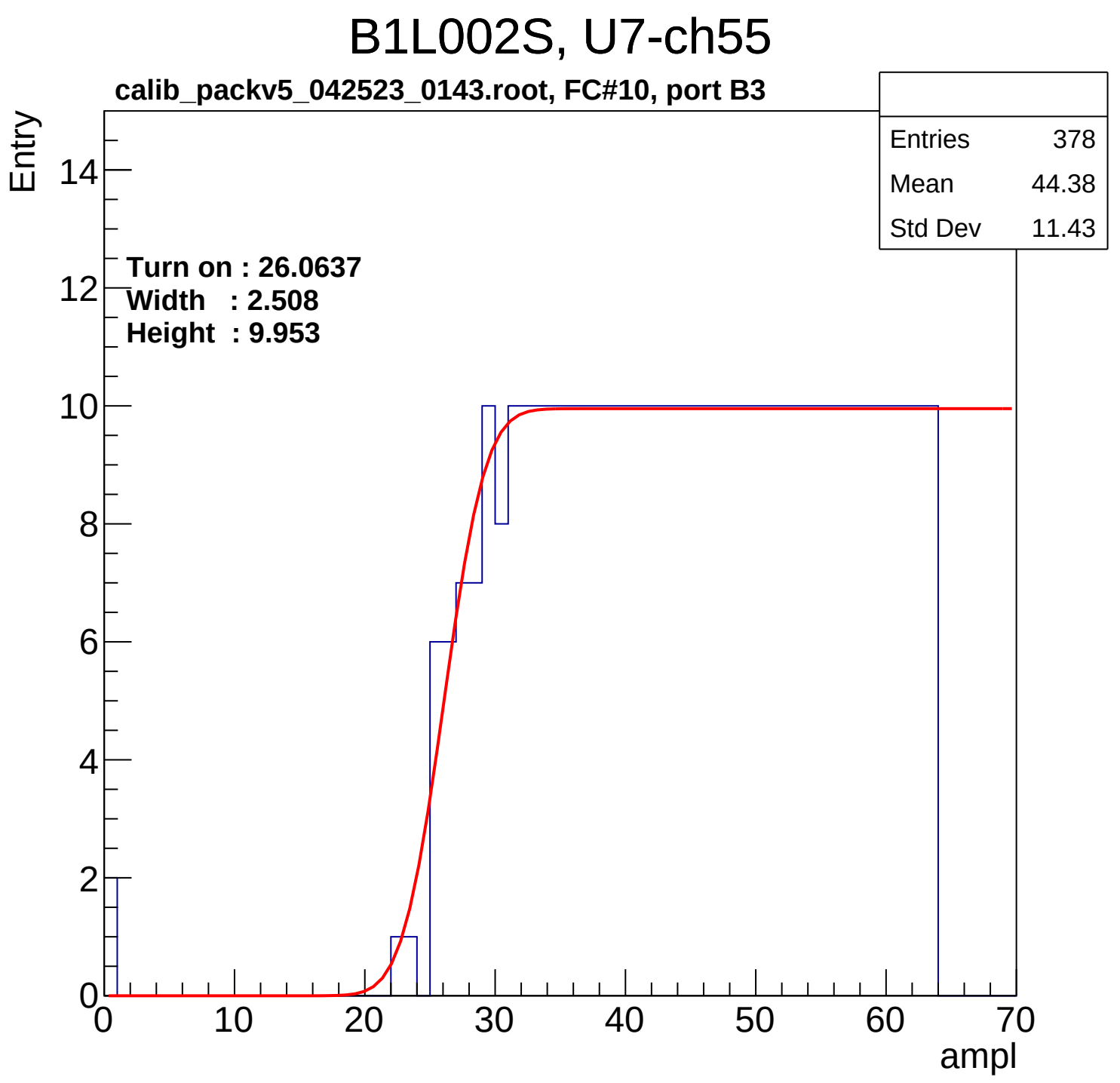
B1L002S, U7-ch55
calib_packv5_042523_0143.root, FC#10, port B3
Entries 378
Mean 44.38
Std Dev 11.43
Turn on : 26.0637
Width : 2.508
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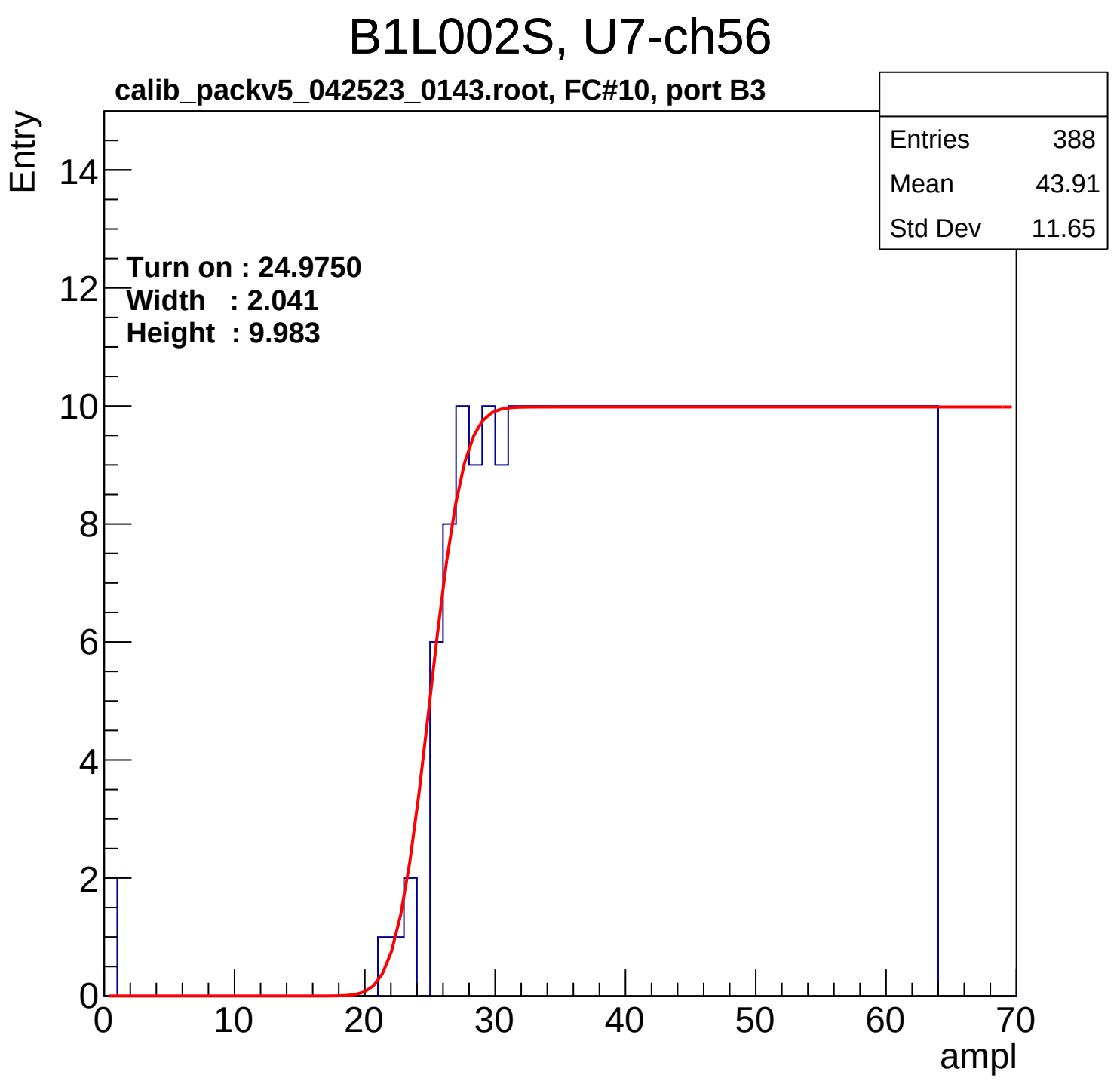
B1L002S, U7-ch56
calib_packv5_042523_0143.root, FC#10, port B3
Entries 388
Mean 43.91
Std Dev 11.65
Turn on : 24.9750
Width : 2.041
Height : 9.983
Entry
ampl
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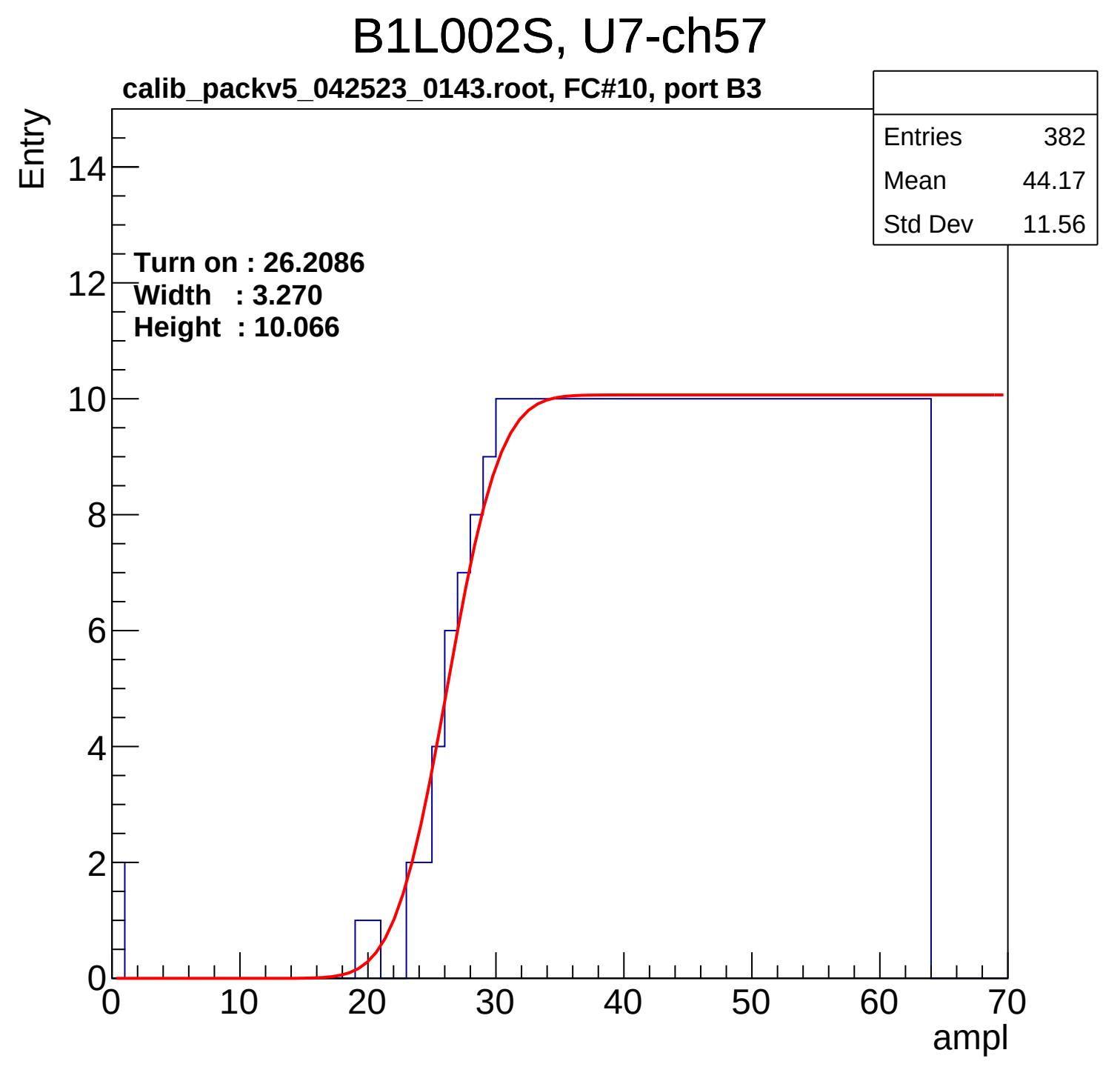
B1L002S, U7-ch57
calib_packv5_042523_0143.root, FC#10, port B3
Entries 382
Mean 44.17
Std Dev 11.56
Turn on : 26.2086
Width : 3.270
Height : 10.066
Entry
ampl
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4
6
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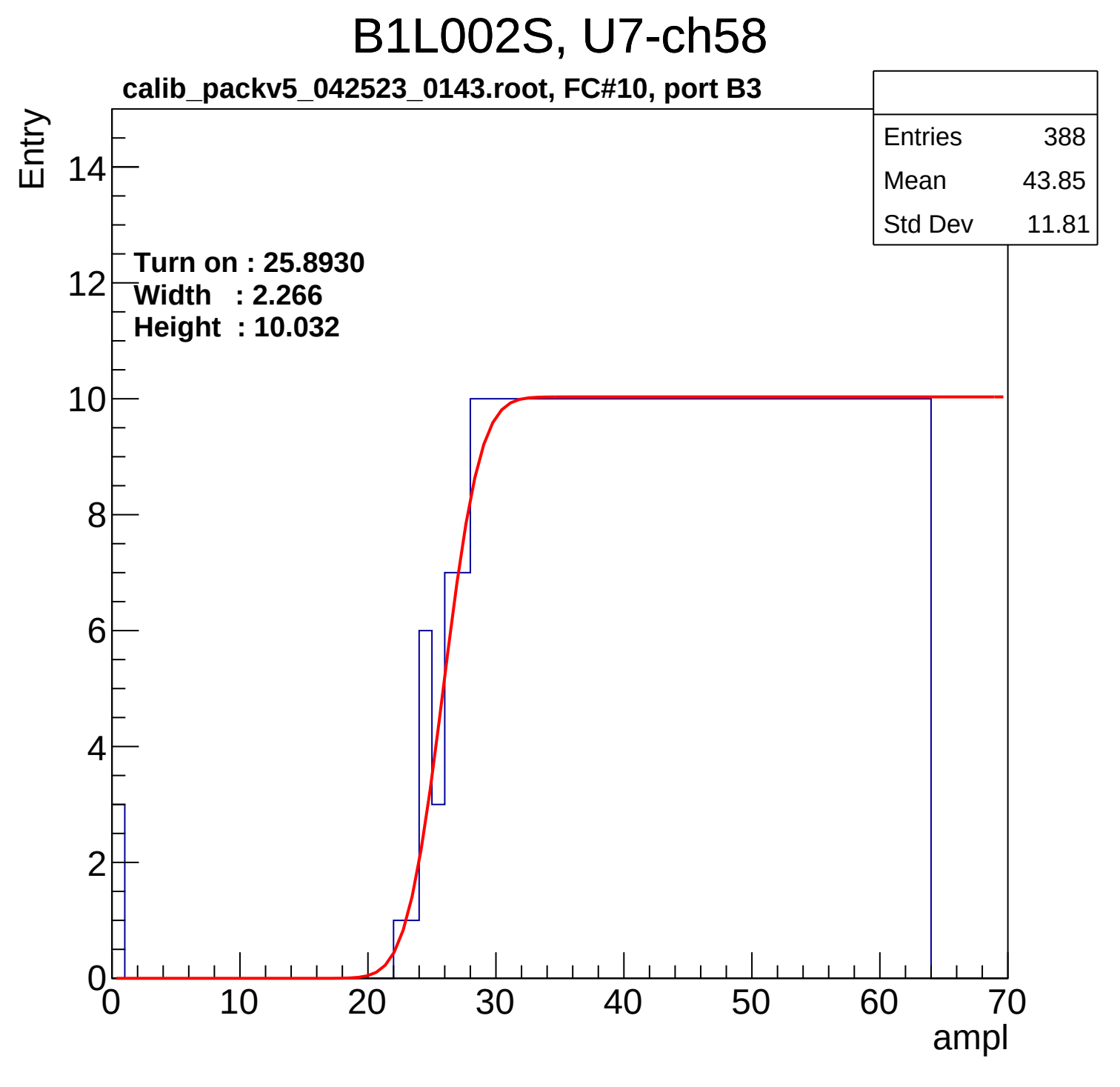
B1L002S, U7-ch58
calib_packv5_042523_0143.root, FC#10, port B3
Entries 388
Mean 43.85
Std Dev 11.81
Turn on : 25.8930
Width : 2.266
Height : 10.032
Entry
ampl
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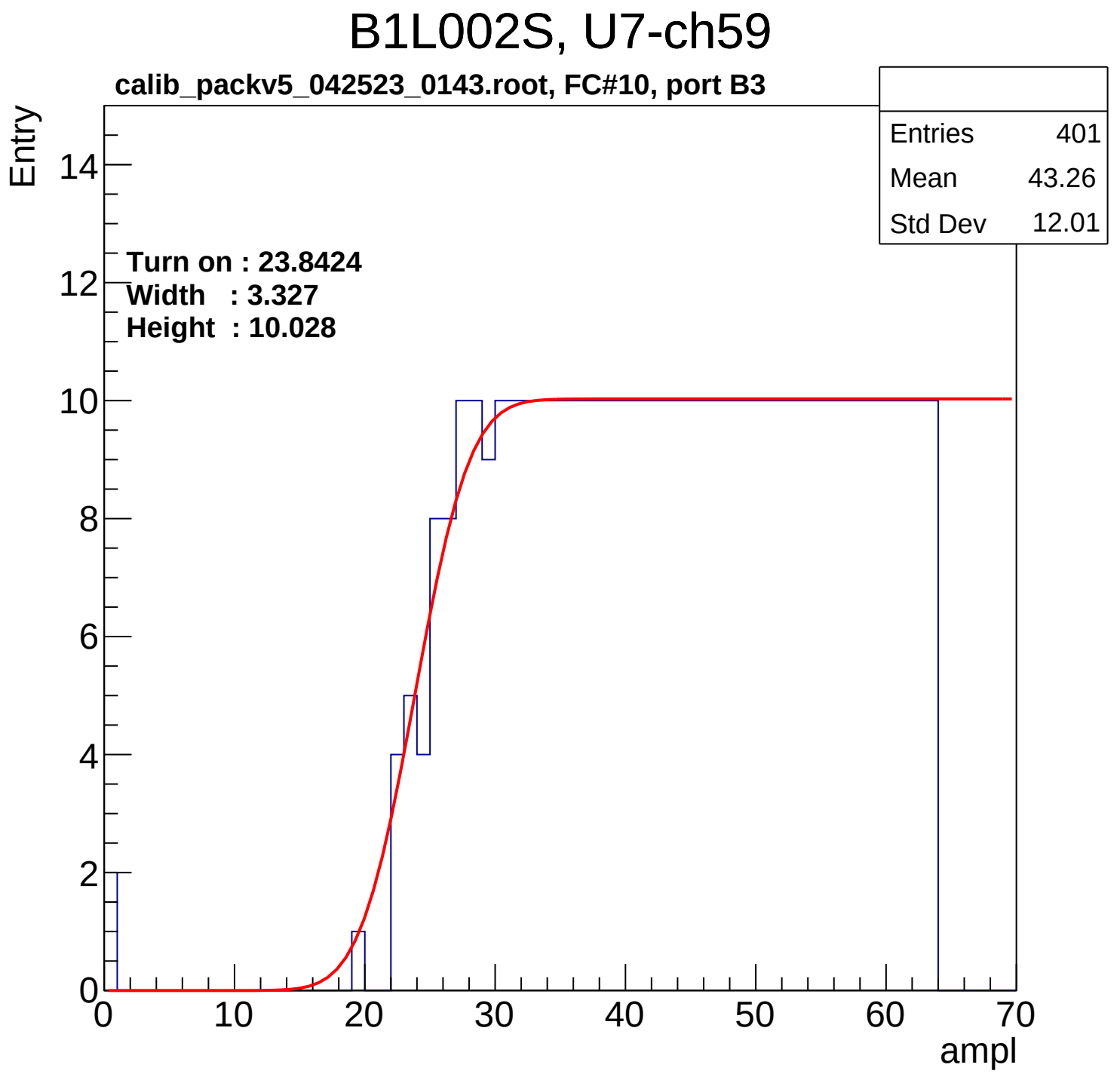
B1L002S, U7-ch59
calib_packv5_042523_0143.root, FC#10, port B3
Entries 401
Mean 43.26
Std Dev 12.01
Turn on : 23.8424
Width : 3.327
Height : 10.028
Entry
ampl
0
2
4
6
8
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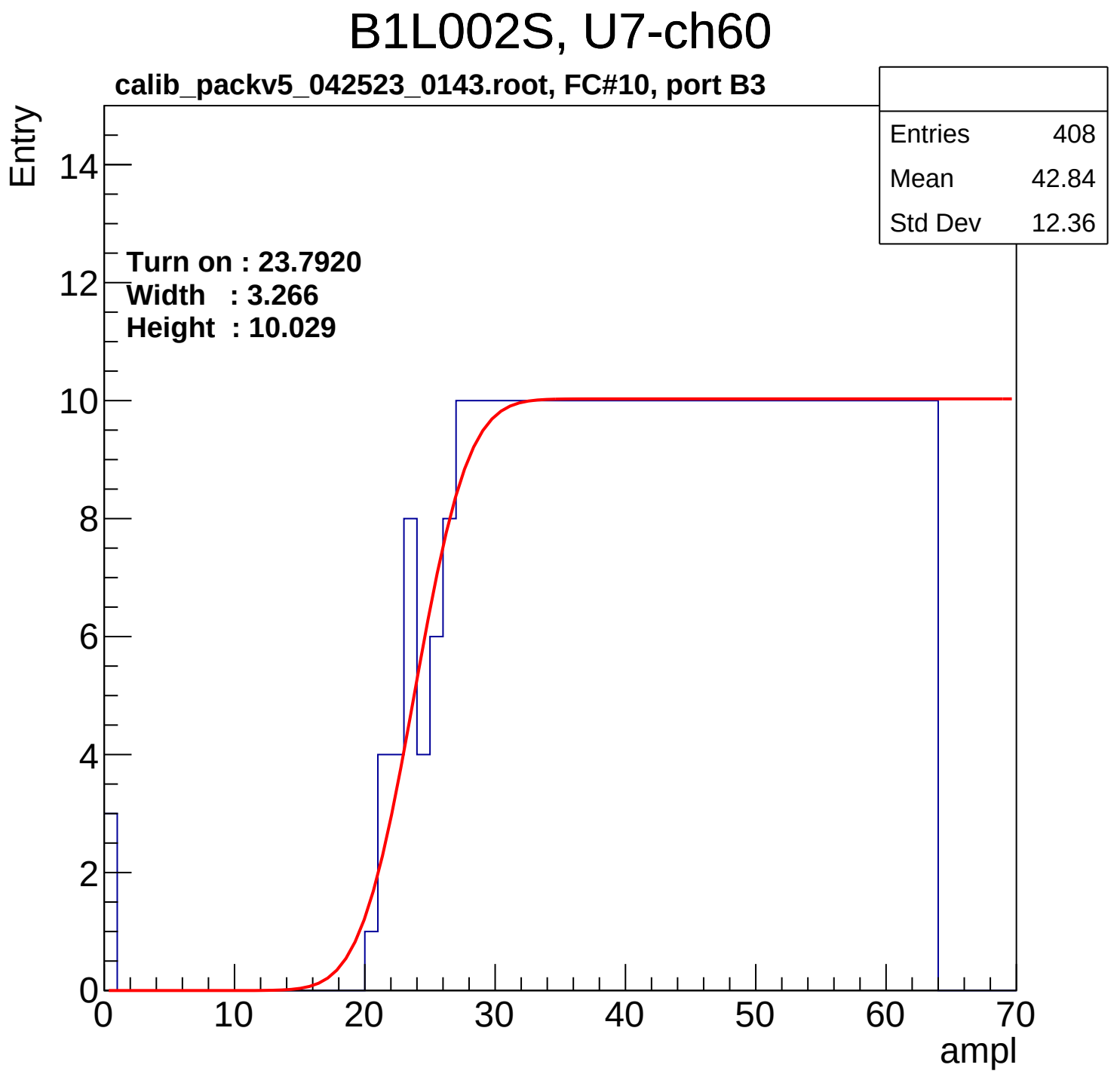
B1L002S, U7-ch60
calib_packv5_042523_0143.root, FC#10, port B3
Entries 408
Mean 42.84
Std Dev 12.36
Turn on : 23.7920
Width : 3.266
Height : 10.029
Entry
ampl
0
2
4
6
8
10
12
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0
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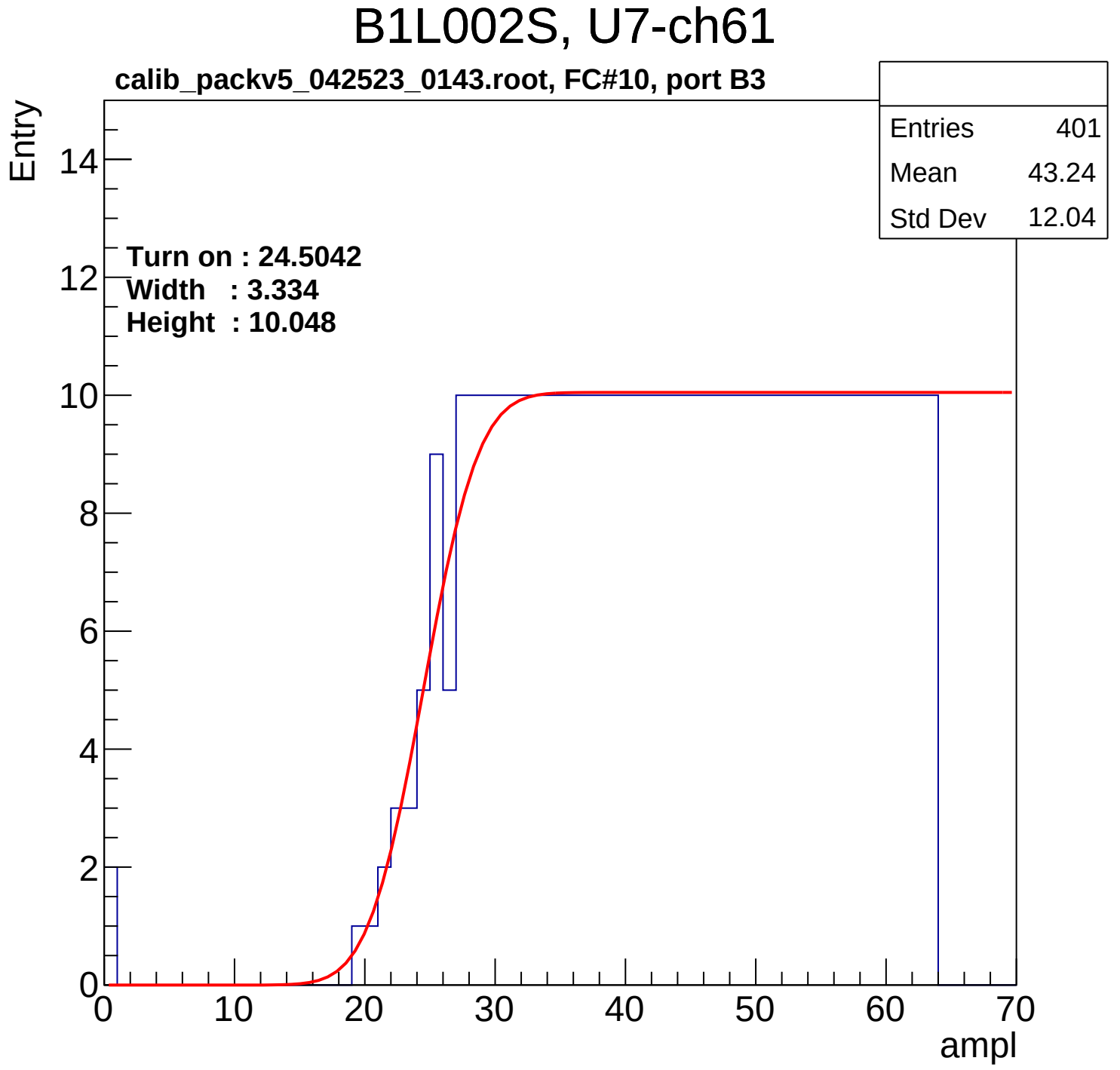
B1L002S, U7-ch61
calib_packv5_042523_0143.root, FC#10, port B3
Entries 401
Mean 43.24
Std Dev 12.04
Turn on : 24.5042
Width : 3.334
Height : 10.048
Entry
ampl
0
2
4
6
8
10
12
14
0
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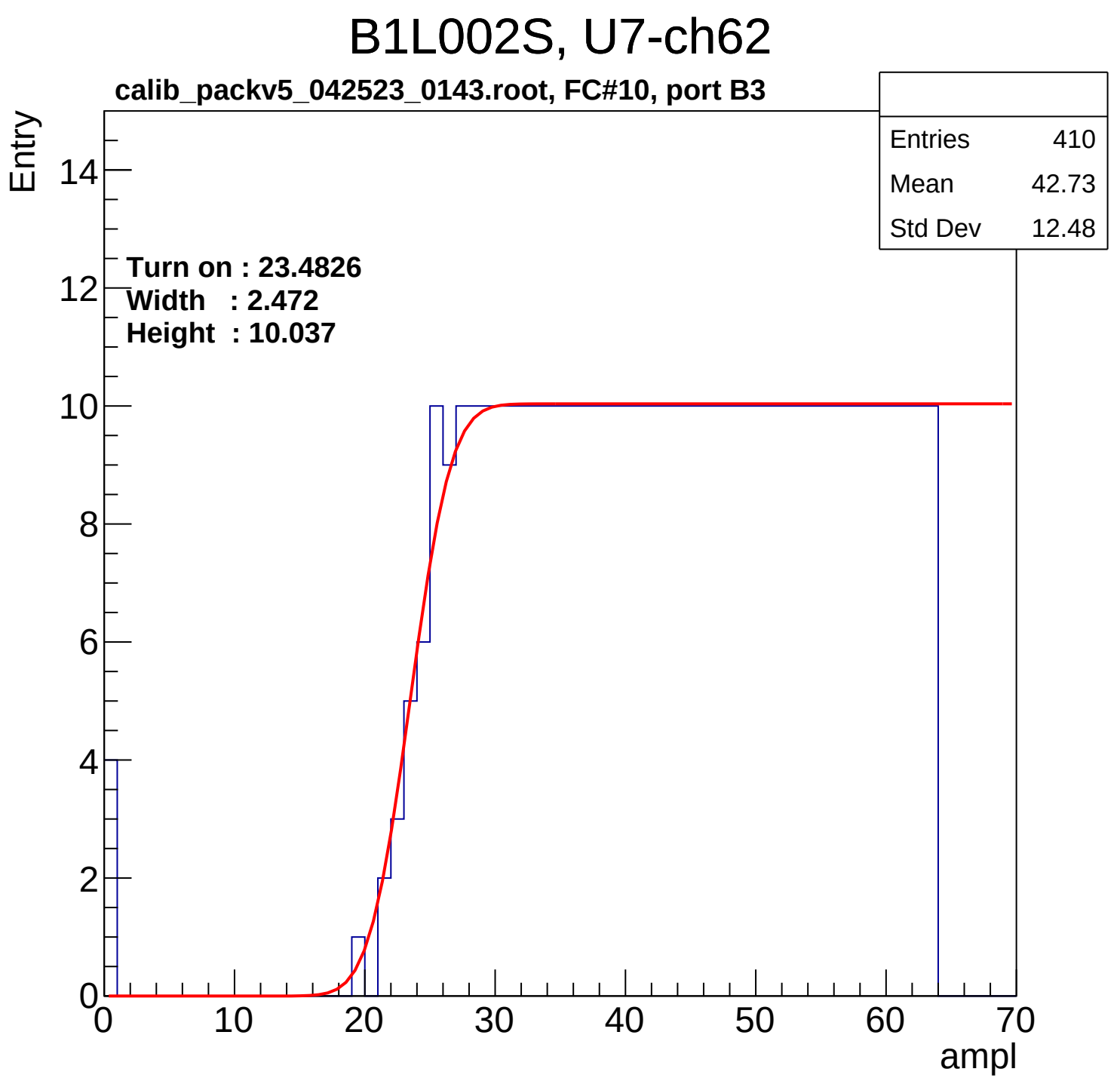
B1L002S, U7-ch62
calib_packv5_042523_0143.root, FC#10, port B3
Entries 410
Mean 42.73
Std Dev 12.48
Turn on : 23.4826
Width : 2.472
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
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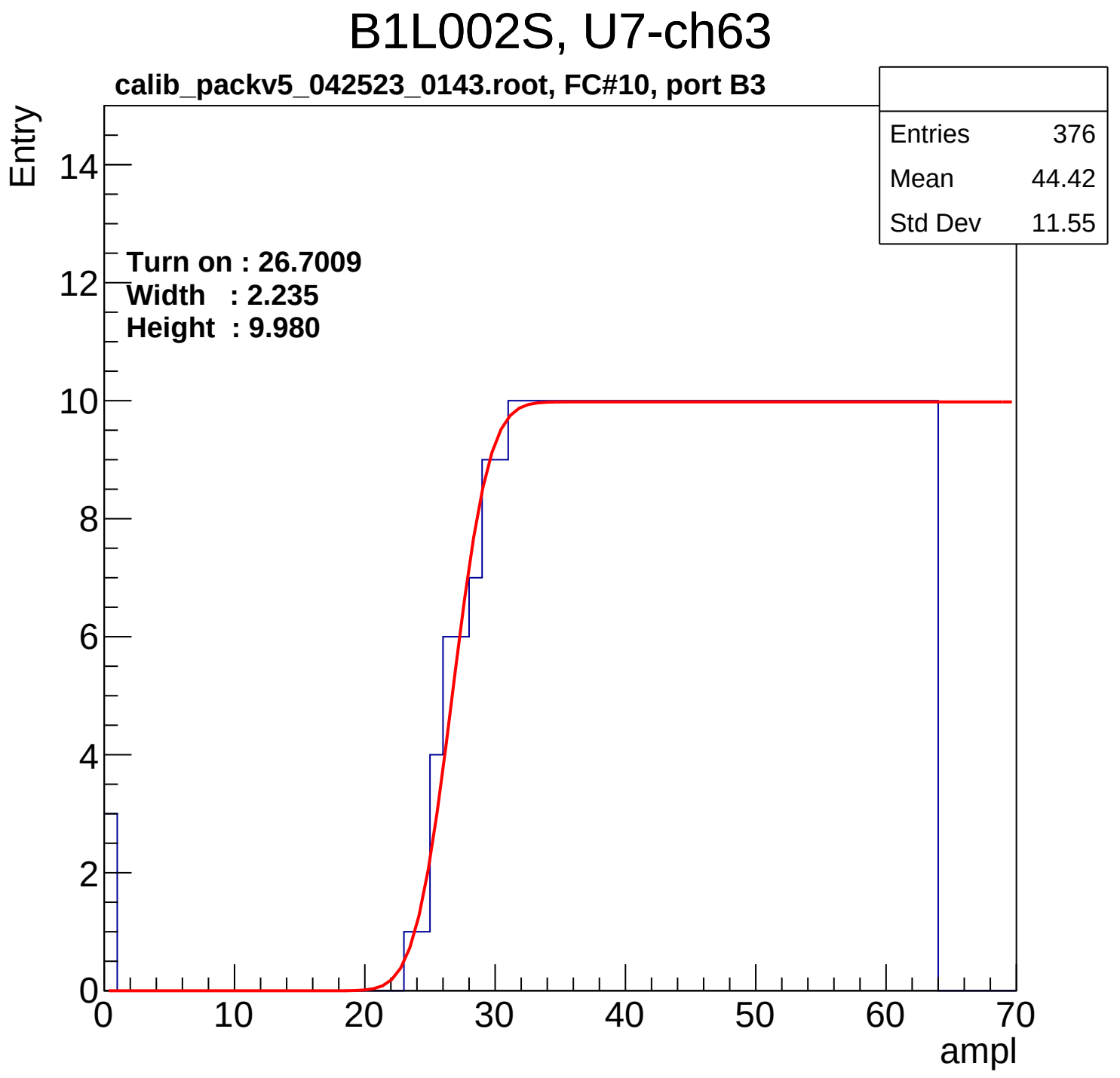
B1L002S, U7-ch63
calib_packv5_042523_0143.root, FC#10, port B3
Entries 376
Mean 44.42
Std Dev 11.55
Turn on : 26.7009
Width : 2.235
Height : 9.980
Entry
ampl
0
2
4
6
8
10
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0
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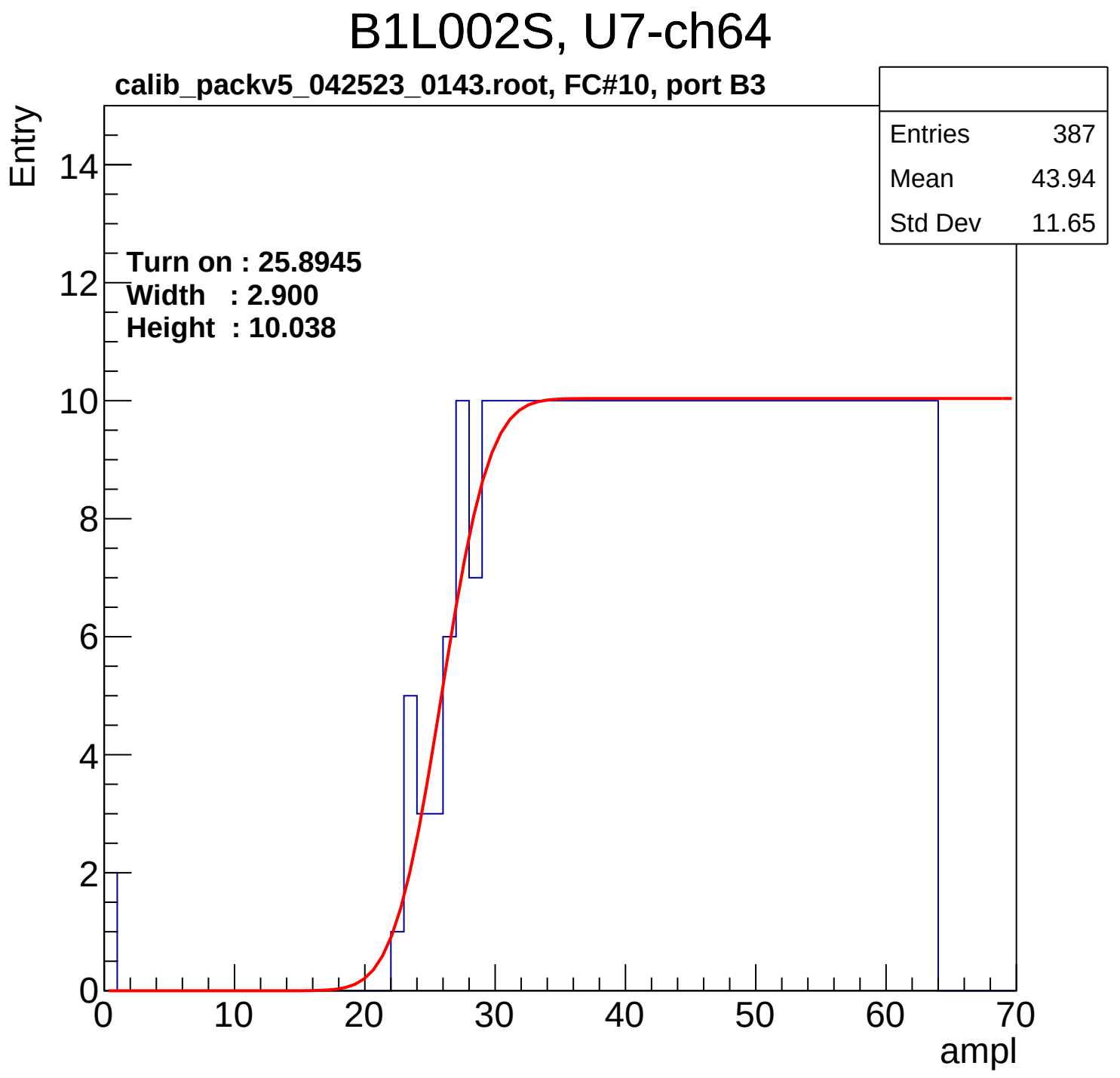
B1L002S, U7-ch64
calib_packv5_042523_0143.root, FC#10, port B3
Entries 387
Mean 43.94
Std Dev 11.65
Turn on : 25.8945
Width : 2.900
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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60
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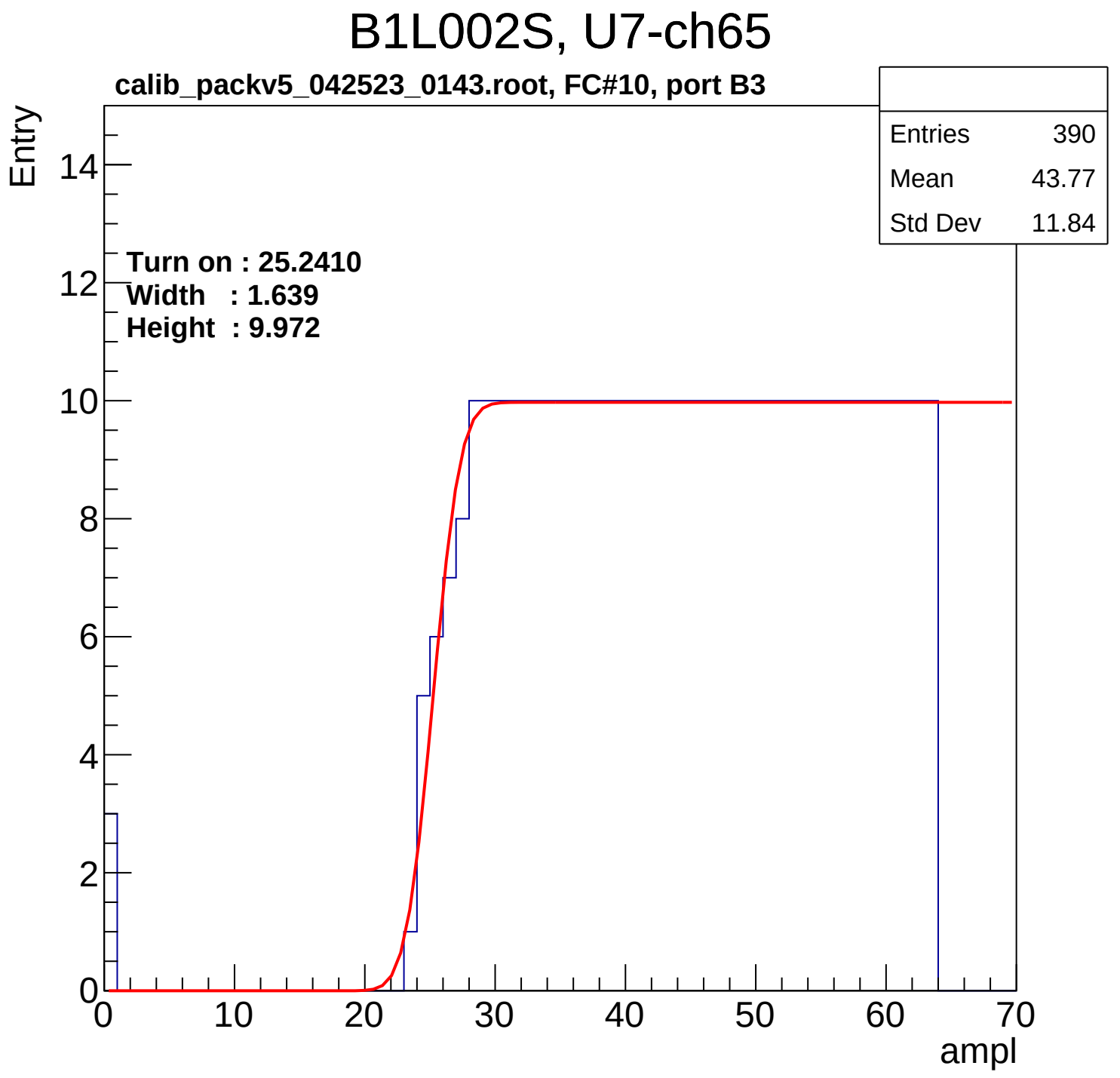
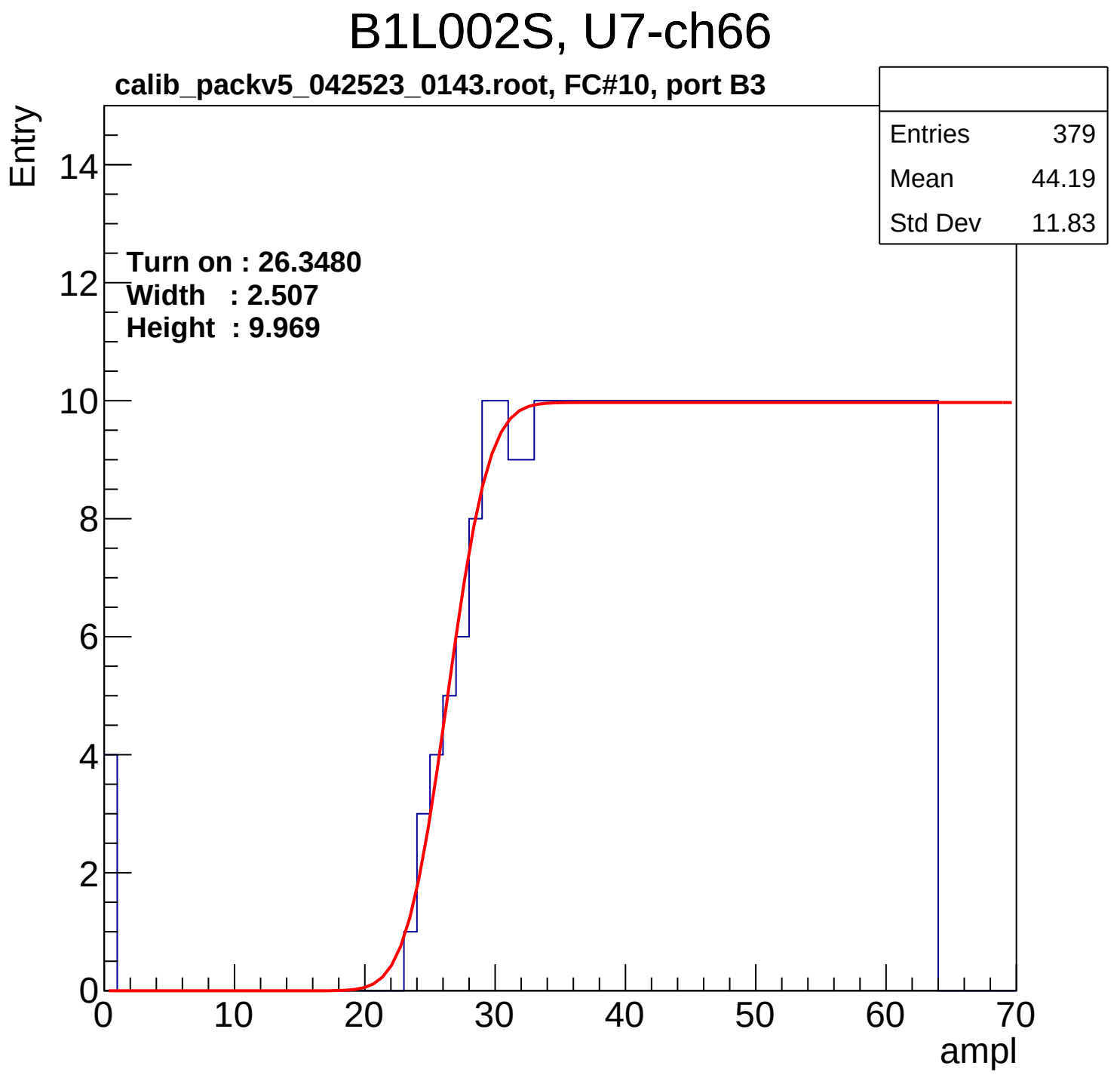

B1L002S, U7-ch65
calib_packv5_042523_0143.root, FC#10, port B3
Entries 390
Mean 43.77
Std Dev 11.84
Turn on : 25.2410
Width : 1.639
Height : 9.972
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L002S, U7-ch66
calib_packv5_042523_0143.root, FC#10, port B3
Entries 379
Mean 44.19
Std Dev 11.83
Turn on : 26.3480
Width : 2.507
Height : 9.969
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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60
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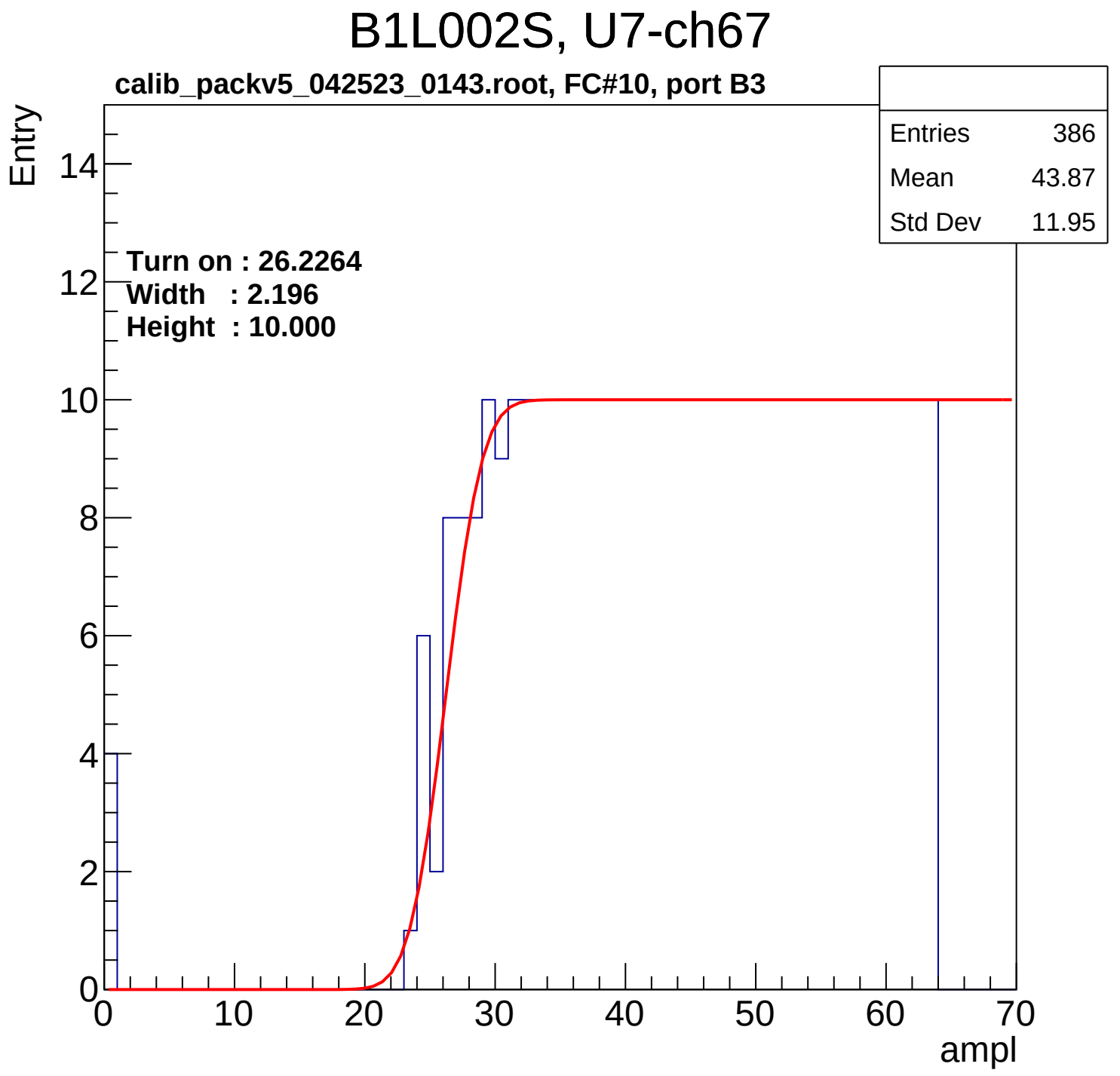
B1L002S, U7-ch67
calib_packv5_042523_0143.root, FC#10, port B3
Entries 386
Mean 43.87
Std Dev 11.95
Turn on : 26.2264
Width : 2.196
Height : 10.000
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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60
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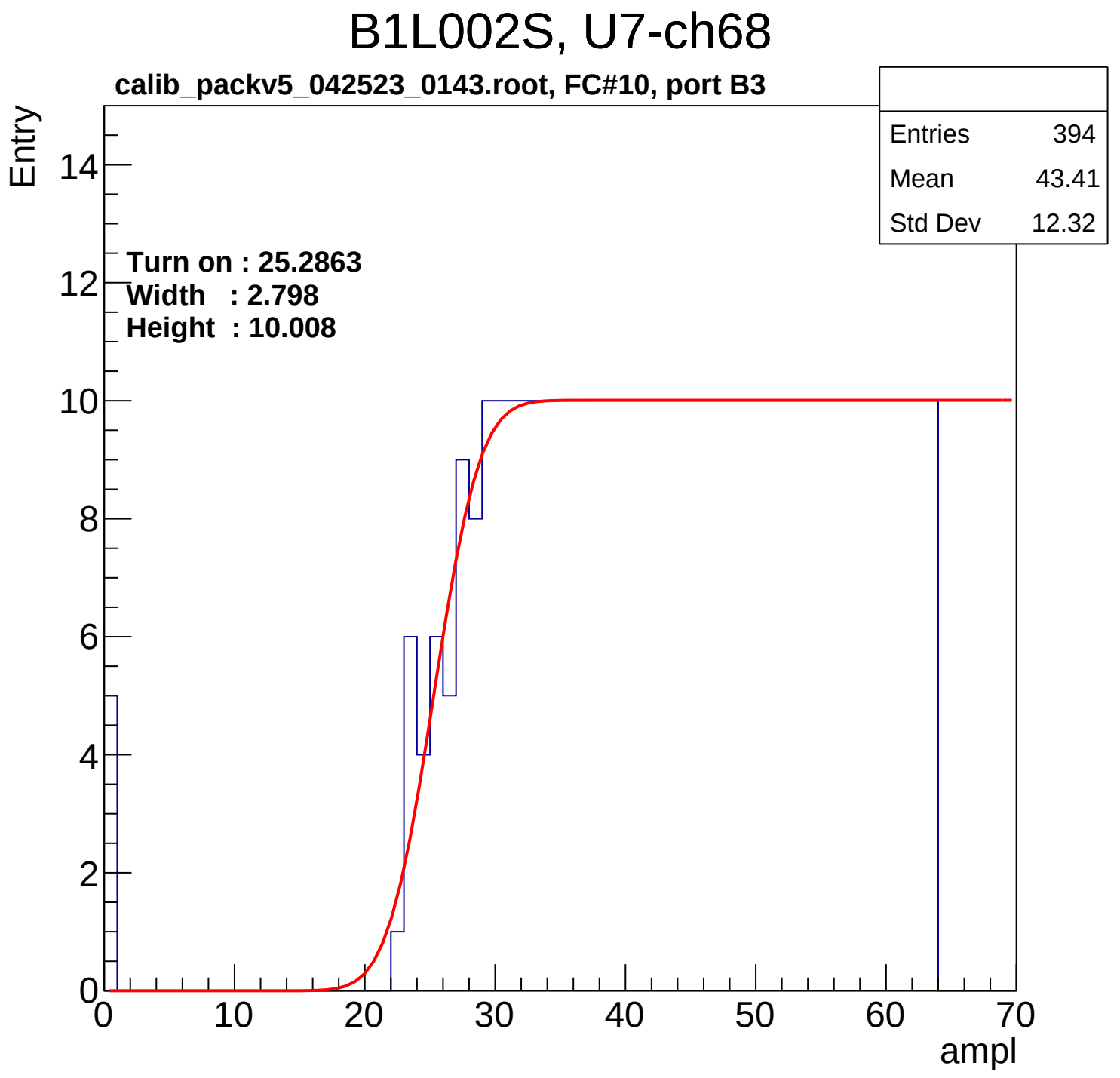
B1L002S, U7-ch68
calib_packv5_042523_0143.root, FC#10, port B3
Entries 394
Mean 43.41
Std Dev 12.32
Turn on : 25.2863
Width : 2.798
Height : 10.008
Entry
ampl
0
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6
8
10
12
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0
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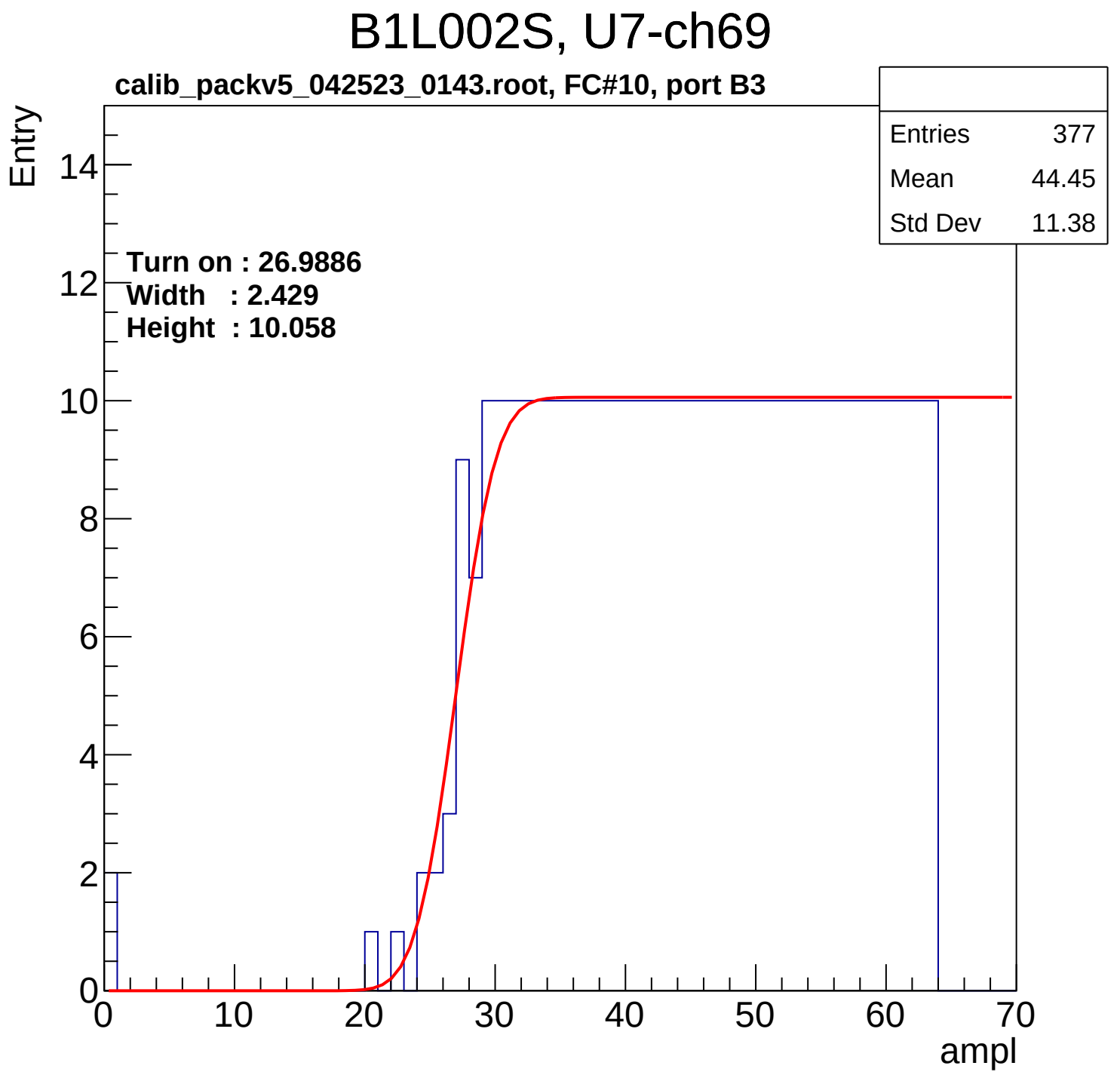
B1L002S, U7-ch69
calib_packv5_042523_0143.root, FC#10, port B3
Entries 377
Mean 44.45
Std Dev 11.38
Turn on : 26.9886
Width : 2.429
Height : 10.058
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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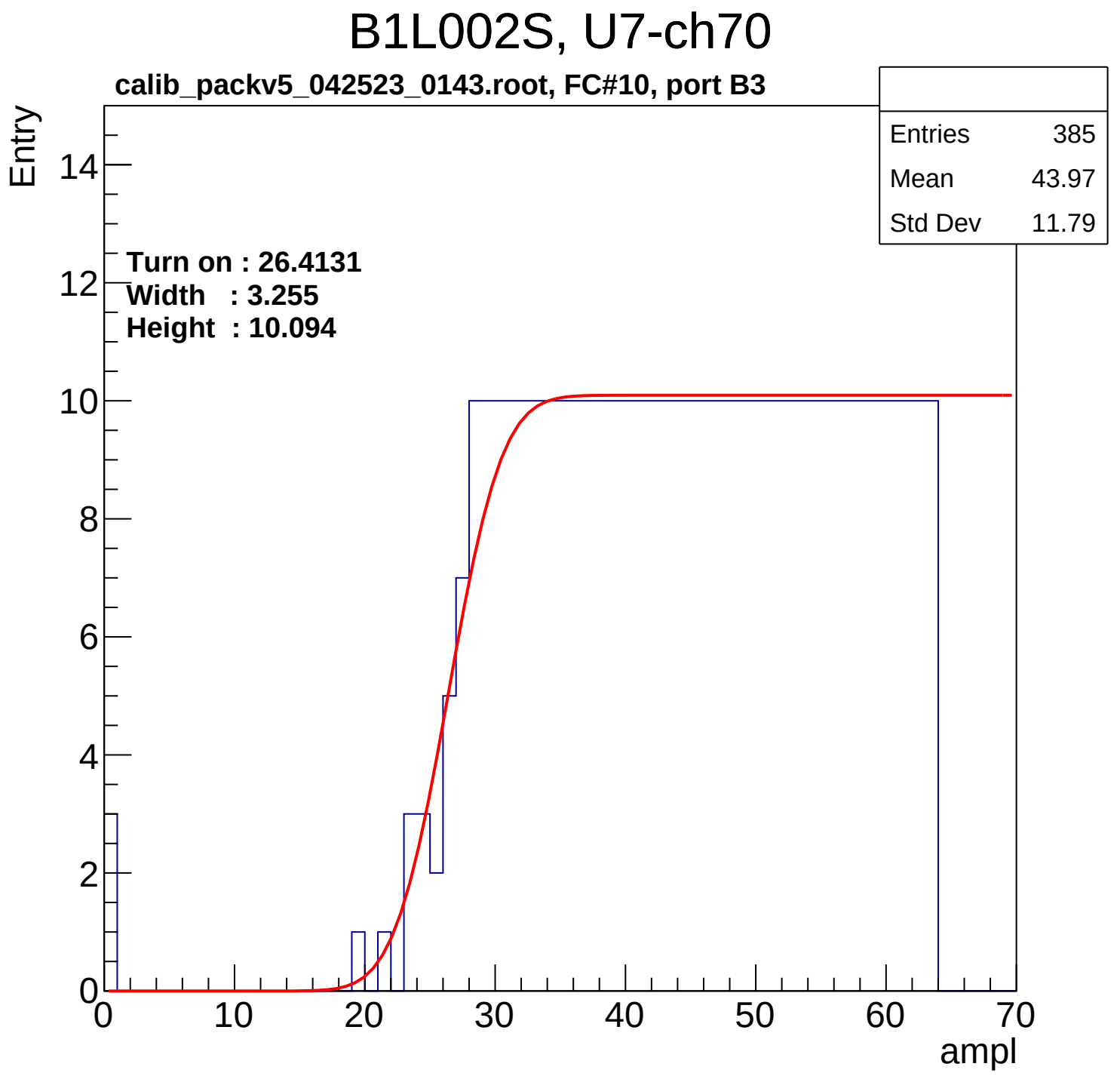
B1L002S, U7-ch70
calib_packv5_042523_0143.root, FC#10, port B3
Entries 385
Mean 43.97
Std Dev 11.79
Turn on : 26.4131
Width : 3.255
Height : 10.094
Entry
ampl
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2
4
6
8
10
12
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0
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20
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40
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60
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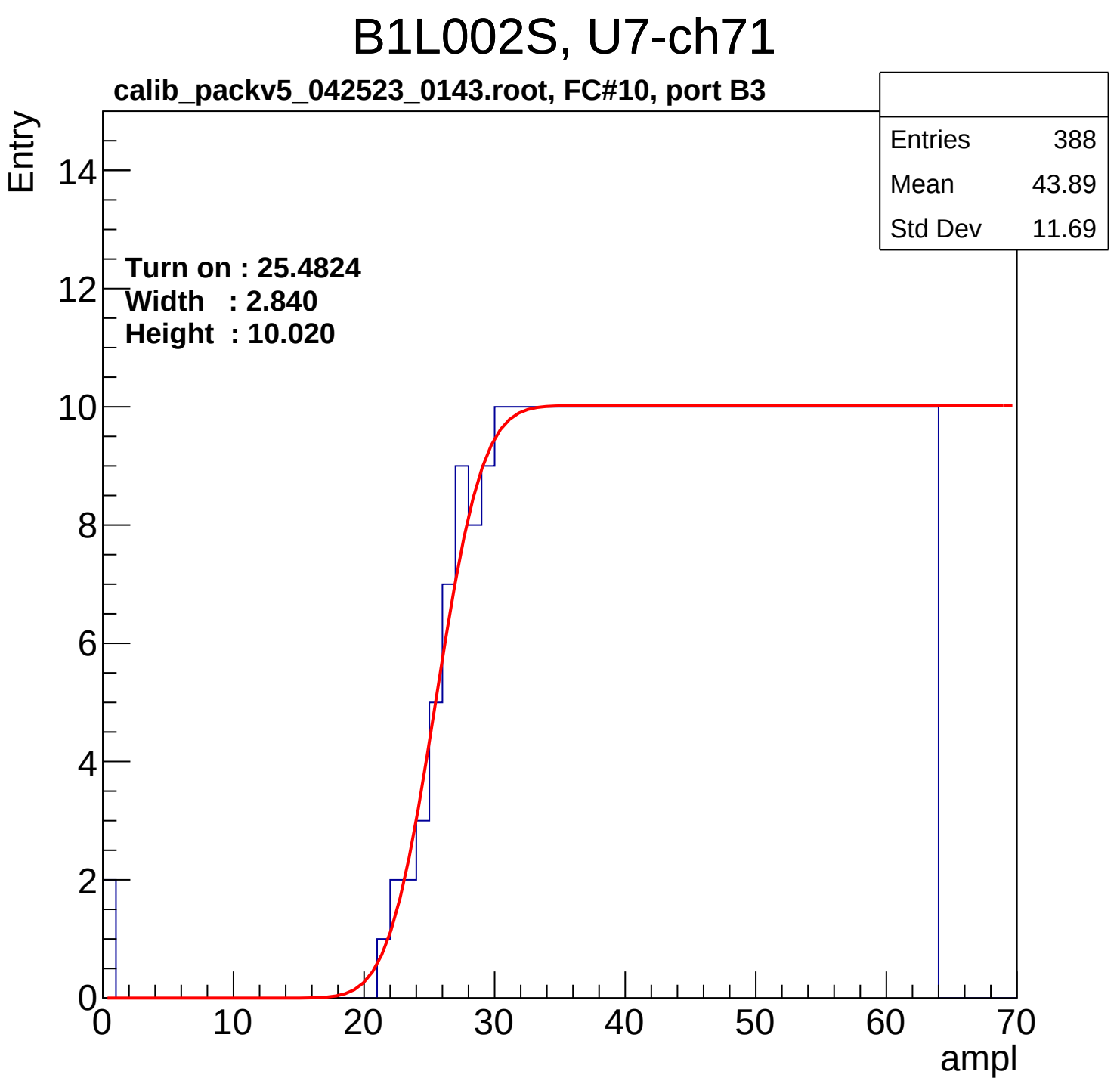
B1L002S, U7-ch71
calib_packv5_042523_0143.root, FC#10, port B3
Entries 388
Mean 43.89
Std Dev 11.69
Turn on : 25.4824
Width : 2.840
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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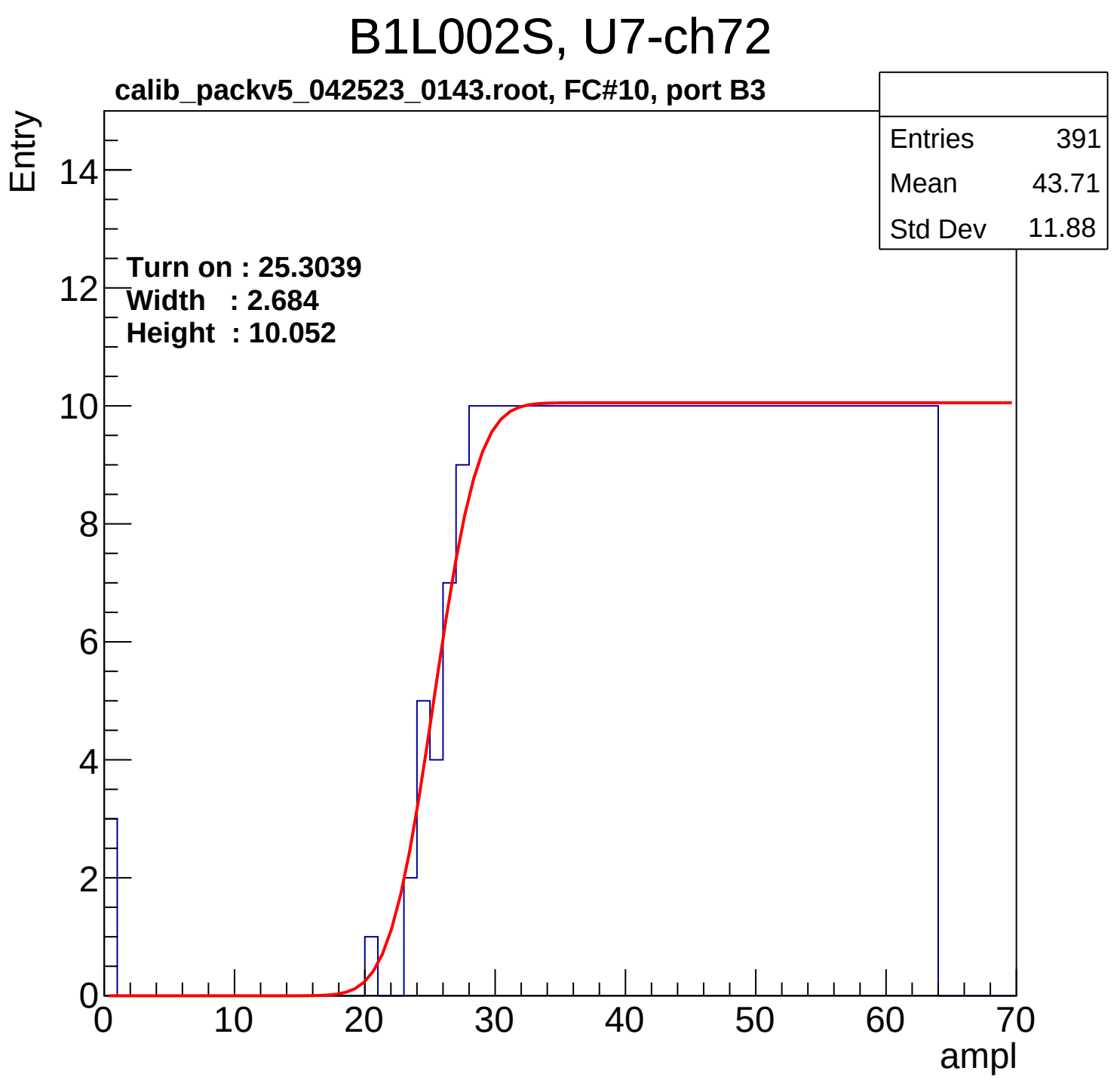
B1L002S, U7-ch72
calib_packv5_042523_0143.root, FC#10, port B3
Entries 391
Mean 43.71
Std Dev 11.88
Turn on : 25.3039
Width : 2.684
Height : 10.052
Entry
ampl
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2
4
6
8
10
12
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0
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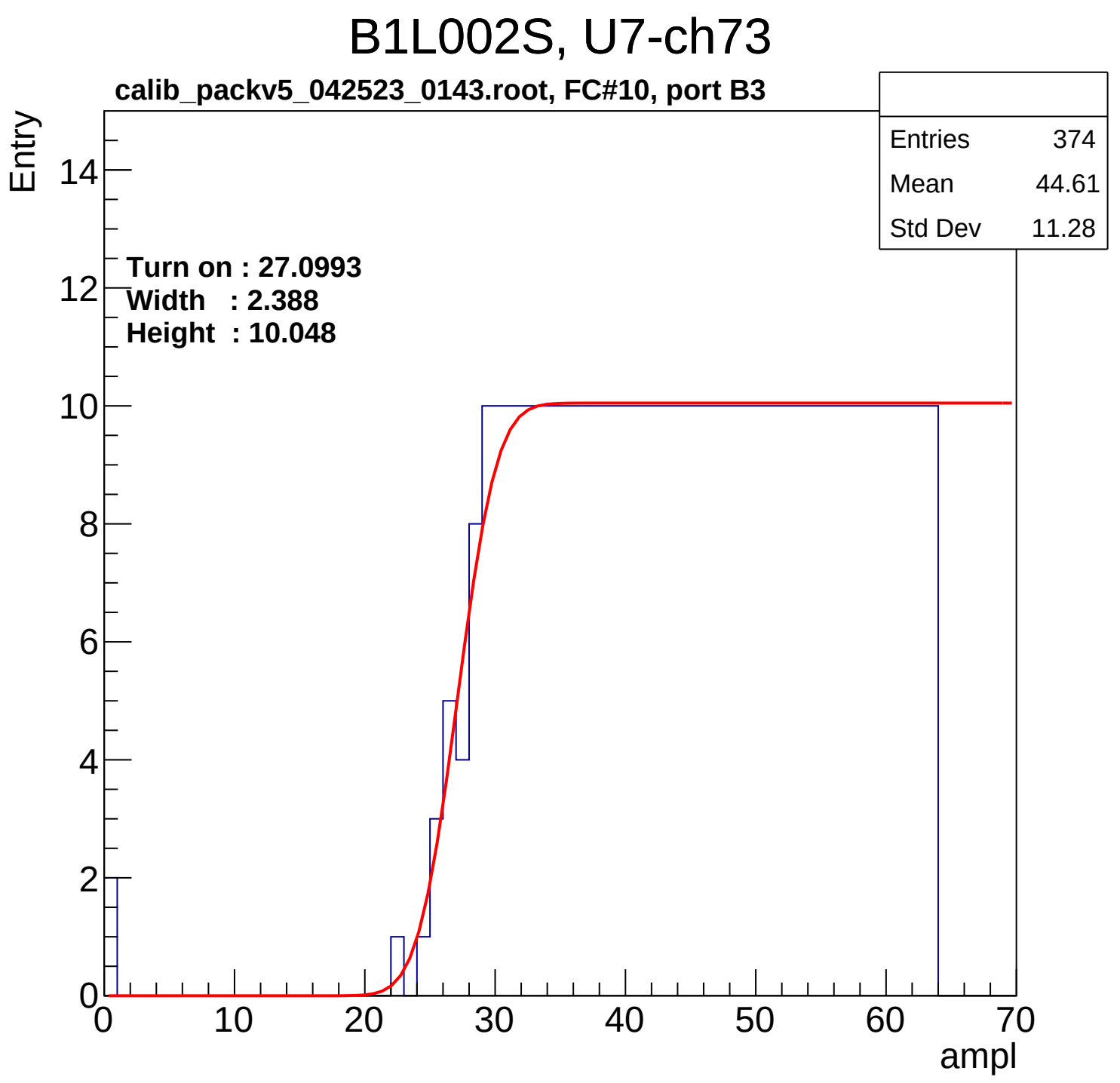
B1L002S, U7-ch73
calib_packv5_042523_0143.root, FC#10, port B3
Entries 374
Mean 44.61
Std Dev 11.28
Turn on : 27.0993
Width : 2.388
Height : 10.048
Entry
ampl
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4
6
8
10
12
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0
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60
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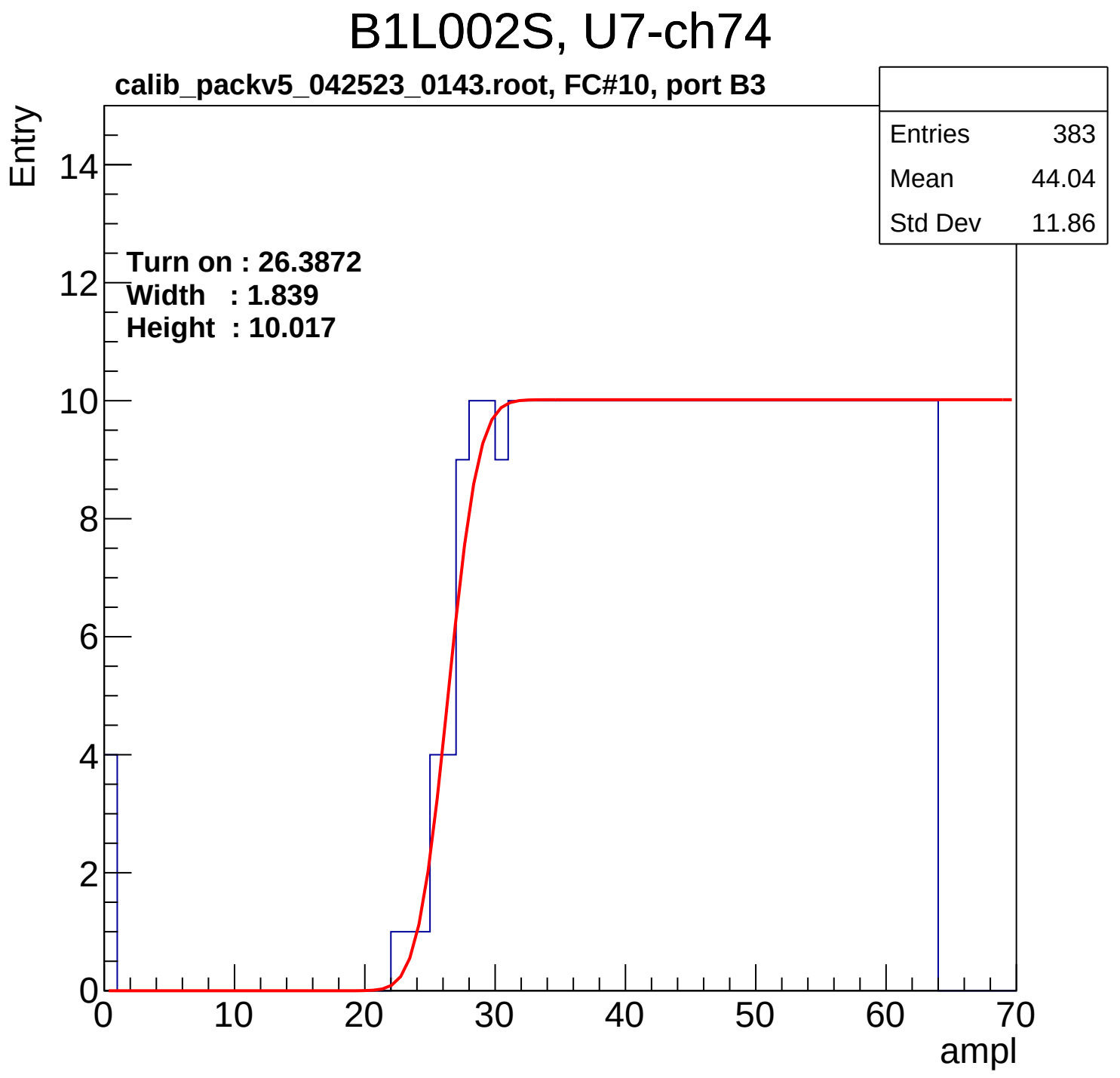
B1L002S, U7-ch74
calib_packv5_042523_0143.root, FC#10, port B3
Entries 383
Mean 44.04
Std Dev 11.86
Turn on : 26.3872
Width : 1.839
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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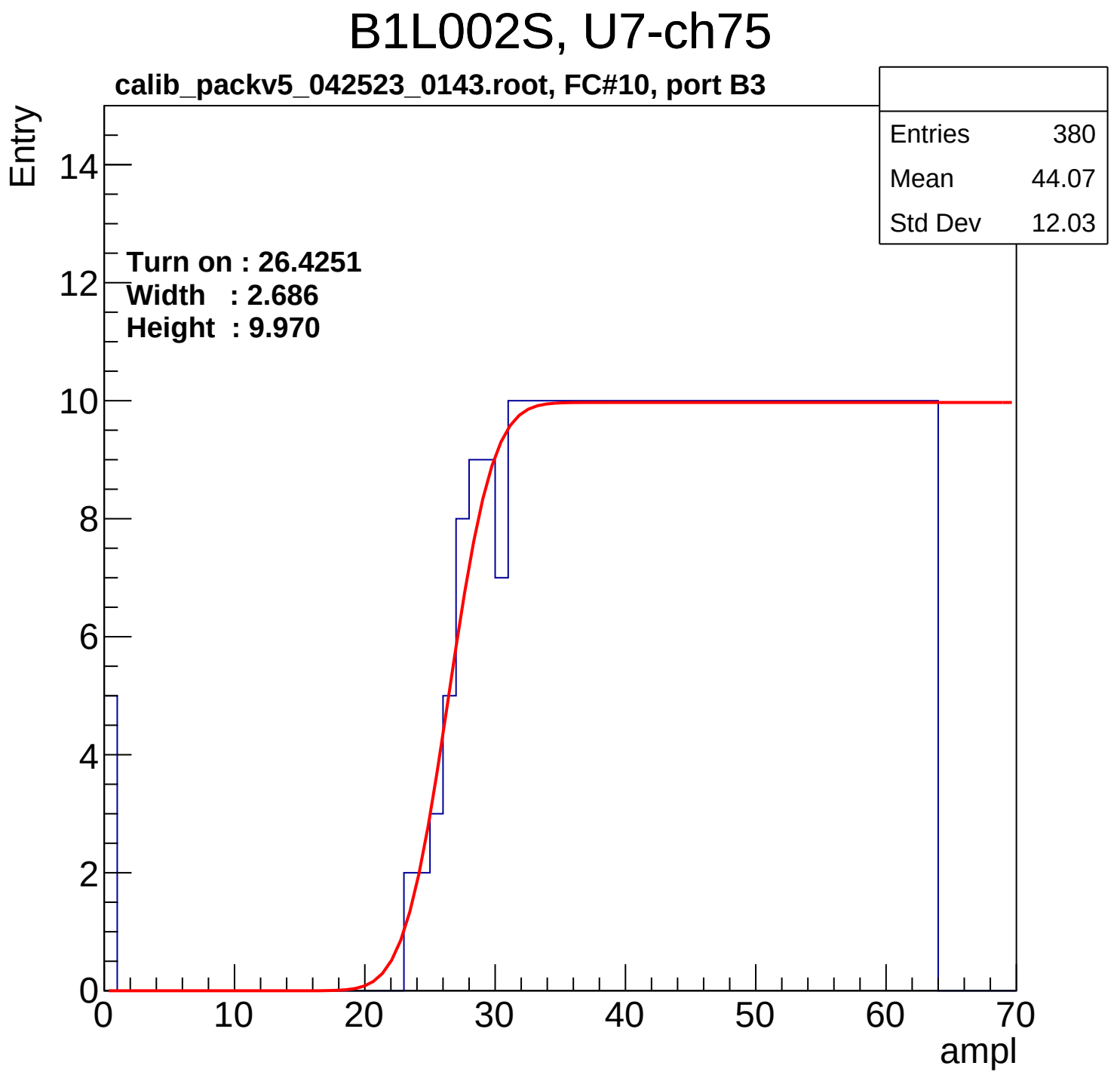
B1L002S, U7-ch75
calib_packv5_042523_0143.root, FC#10, port B3
Entries 380
Mean 44.07
Std Dev 12.03
Turn on : 26.4251
Width : 2.686
Height : 9.970
Entry
ampl
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8
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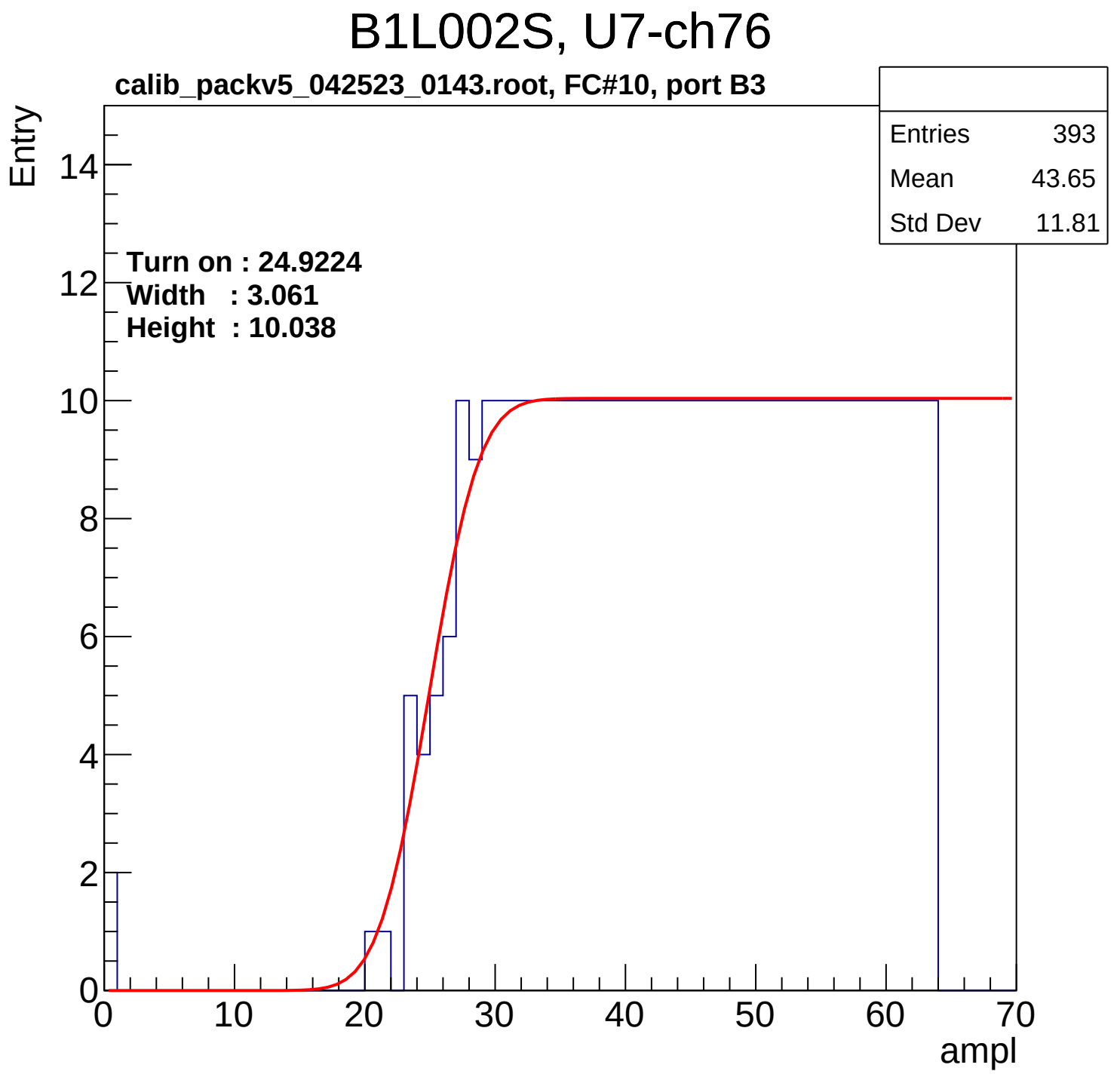
B1L002S, U7-ch76
calib_packv5_042523_0143.root, FC#10, port B3
Entries 393
Mean 43.65
Std Dev 11.81
Turn on : 24.9224
Width : 3.061
Height : 10.038
Entry
ampl
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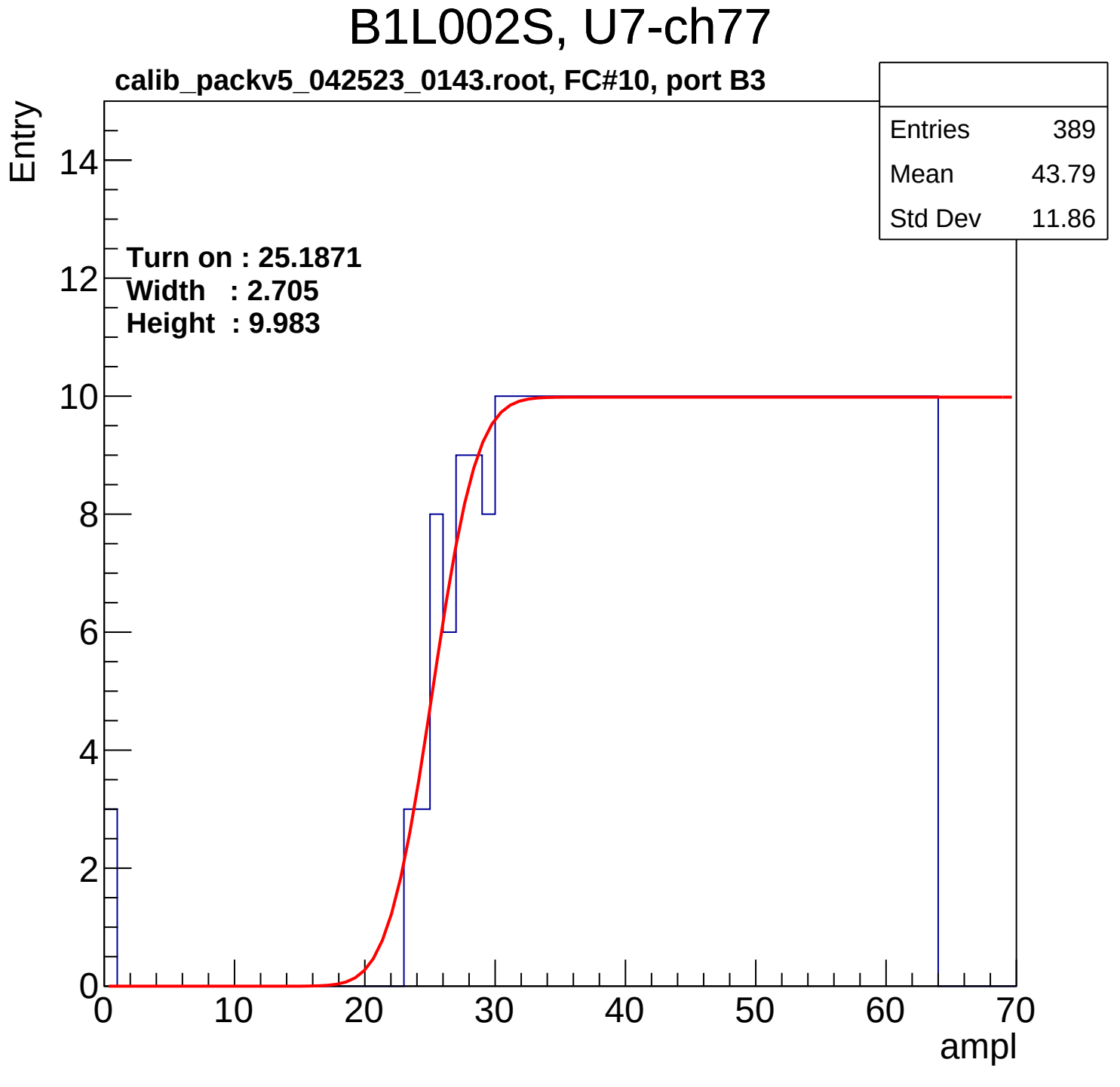
B1L002S, U7-ch77
calib_packv5_042523_0143.root, FC#10, port B3
Entries 389
Mean 43.79
Std Dev 11.86
Turn on : 25.1871
Width : 2.705
Height : 9.983
Entry
ampl
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0
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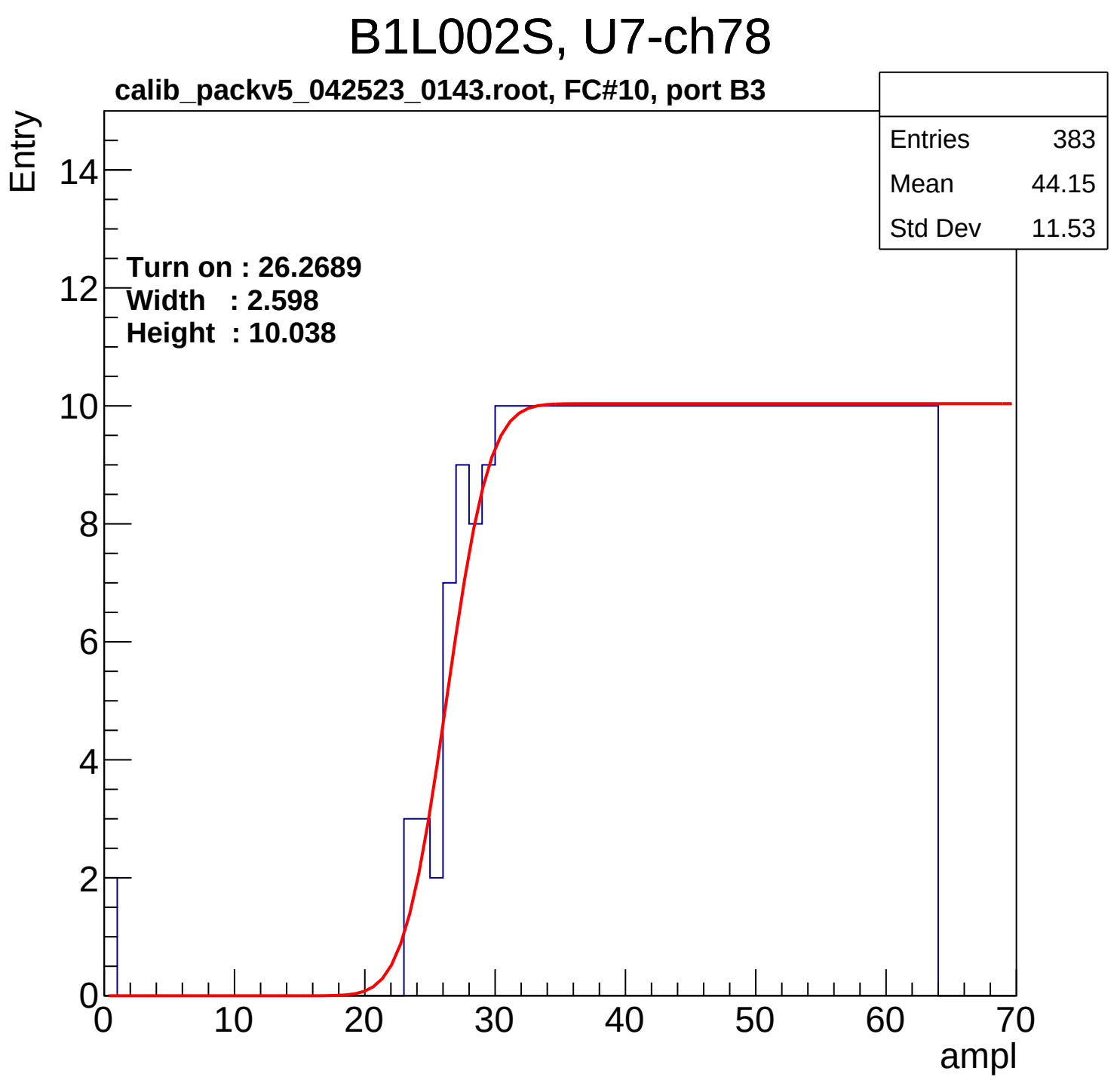
B1L002S, U7-ch78
calib_packv5_042523_0143.root, FC#10, port B3
Entries 383
Mean 44.15
Std Dev 11.53
Turn on : 26.2689
Width : 2.598
Height : 10.038
Entry
ampl
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2
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6
8
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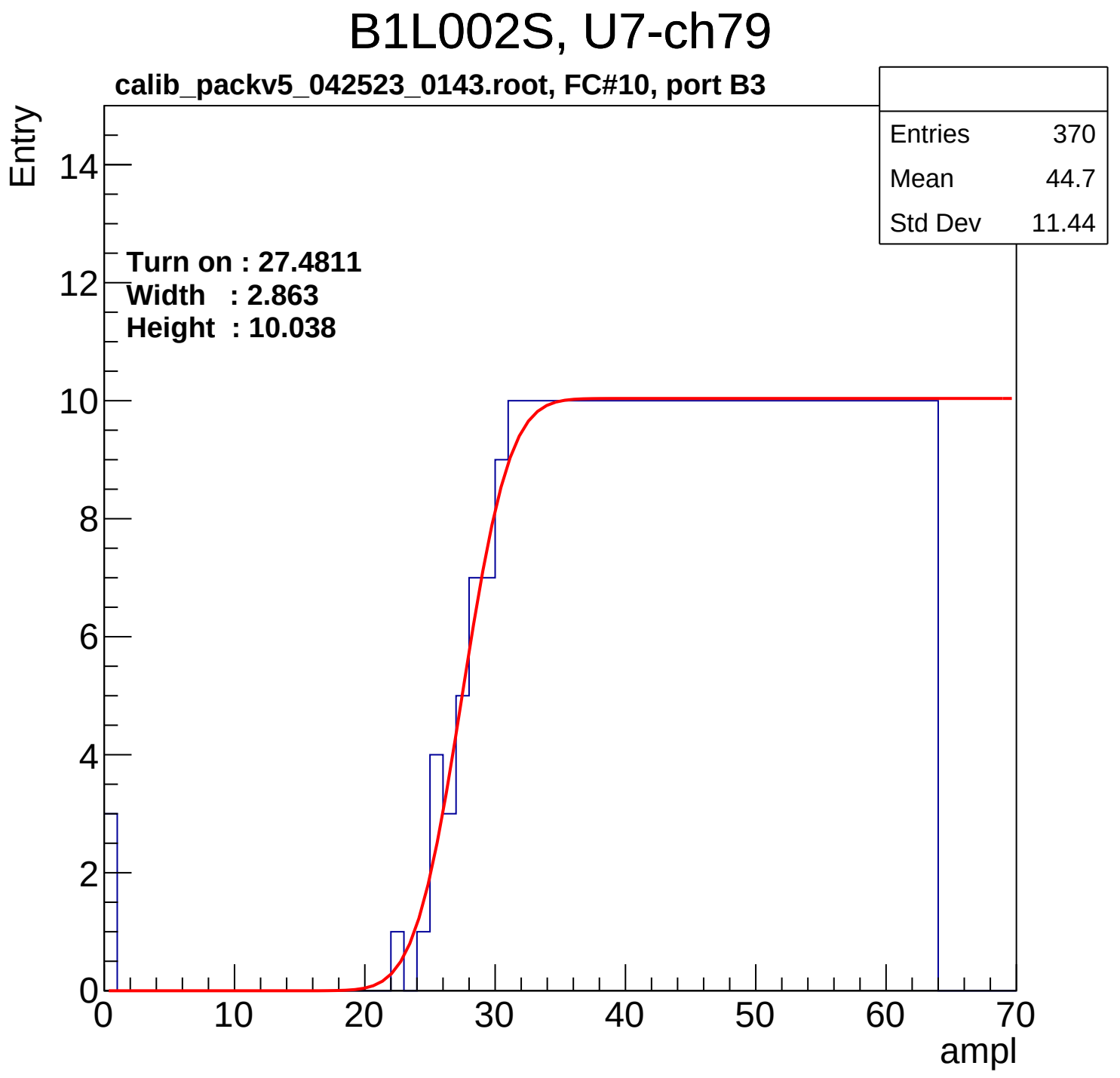
B1L002S, U7-ch79
calib_packv5_042523_0143.root, FC#10, port B3
Entries 370
Mean 44.7
Std Dev 11.44
Turn on : 27.4811
Width : 2.863
Height : 10.038
Entry
ampl
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4
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8
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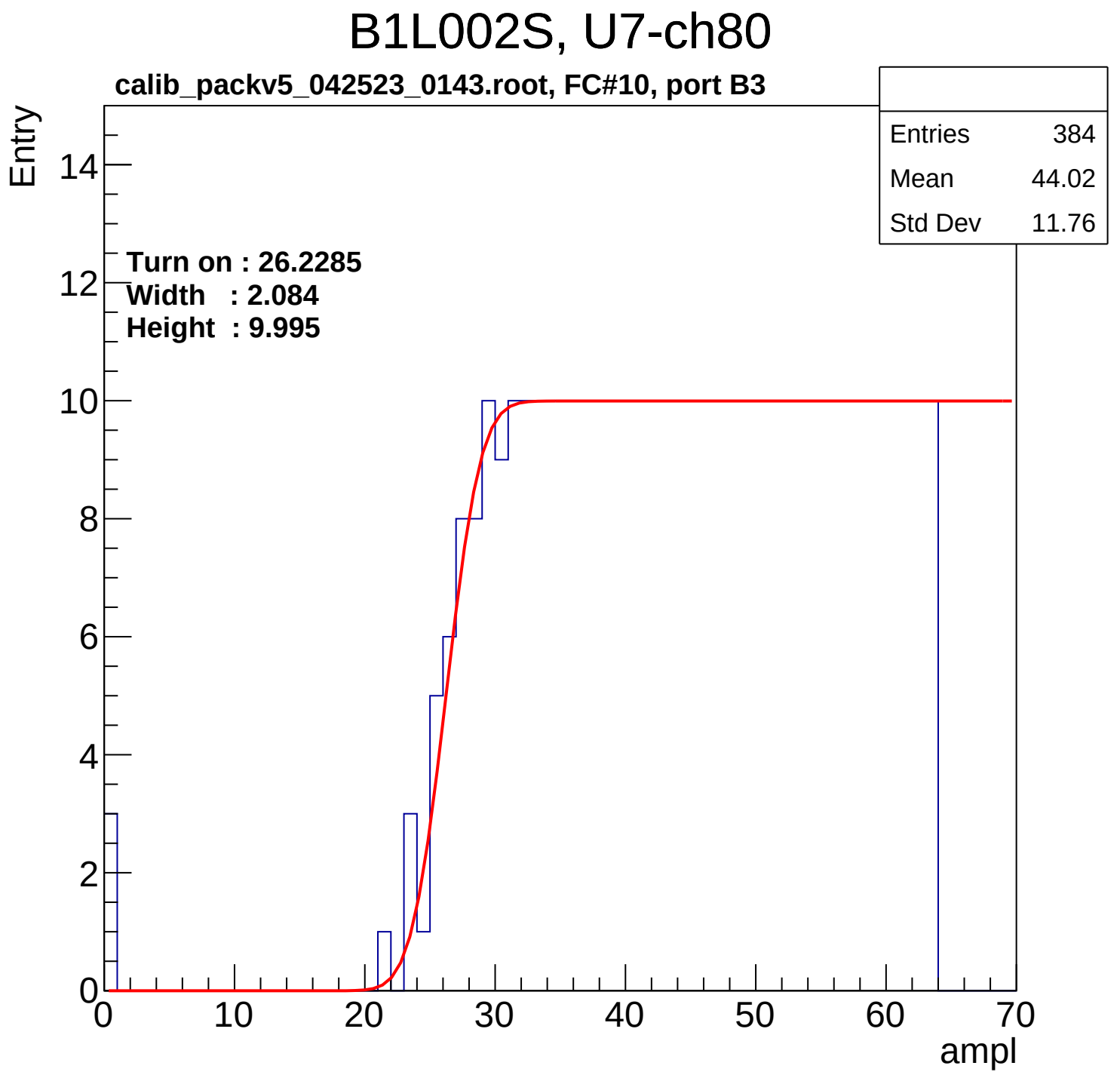
B1L002S, U7-ch80
calib_packv5_042523_0143.root, FC#10, port B3
Entries 384
Mean 44.02
Std Dev 11.76
Turn on : 26.2285
Width : 2.084
Height : 9.995
Entry
ampl
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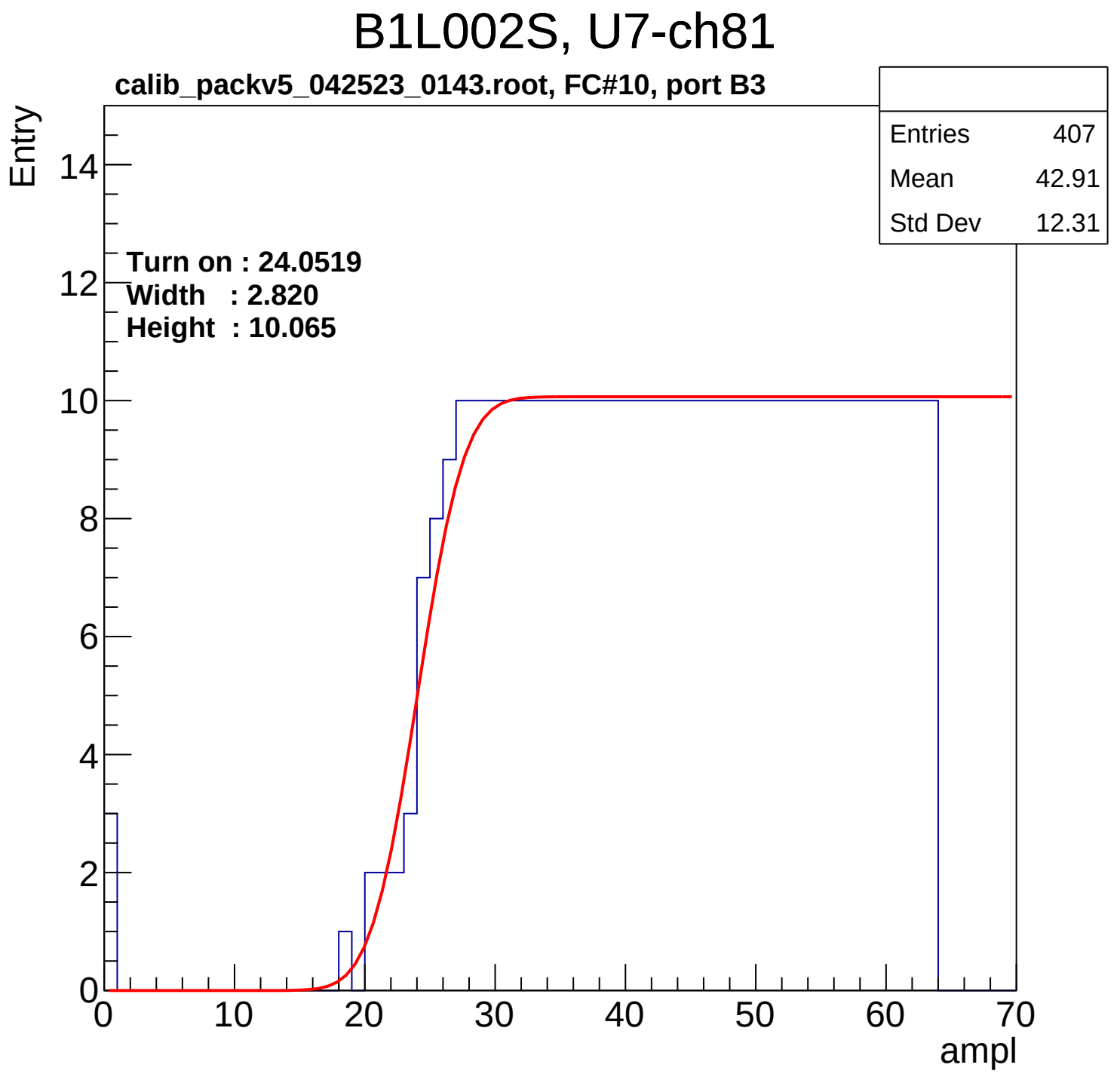
B1L002S, U7-ch81
calib_packv5_042523_0143.root, FC#10, port B3
Entries 407
Mean 42.91
Std Dev 12.31
Turn on : 24.0519
Width : 2.820
Height : 10.065
Entry
ampl
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8
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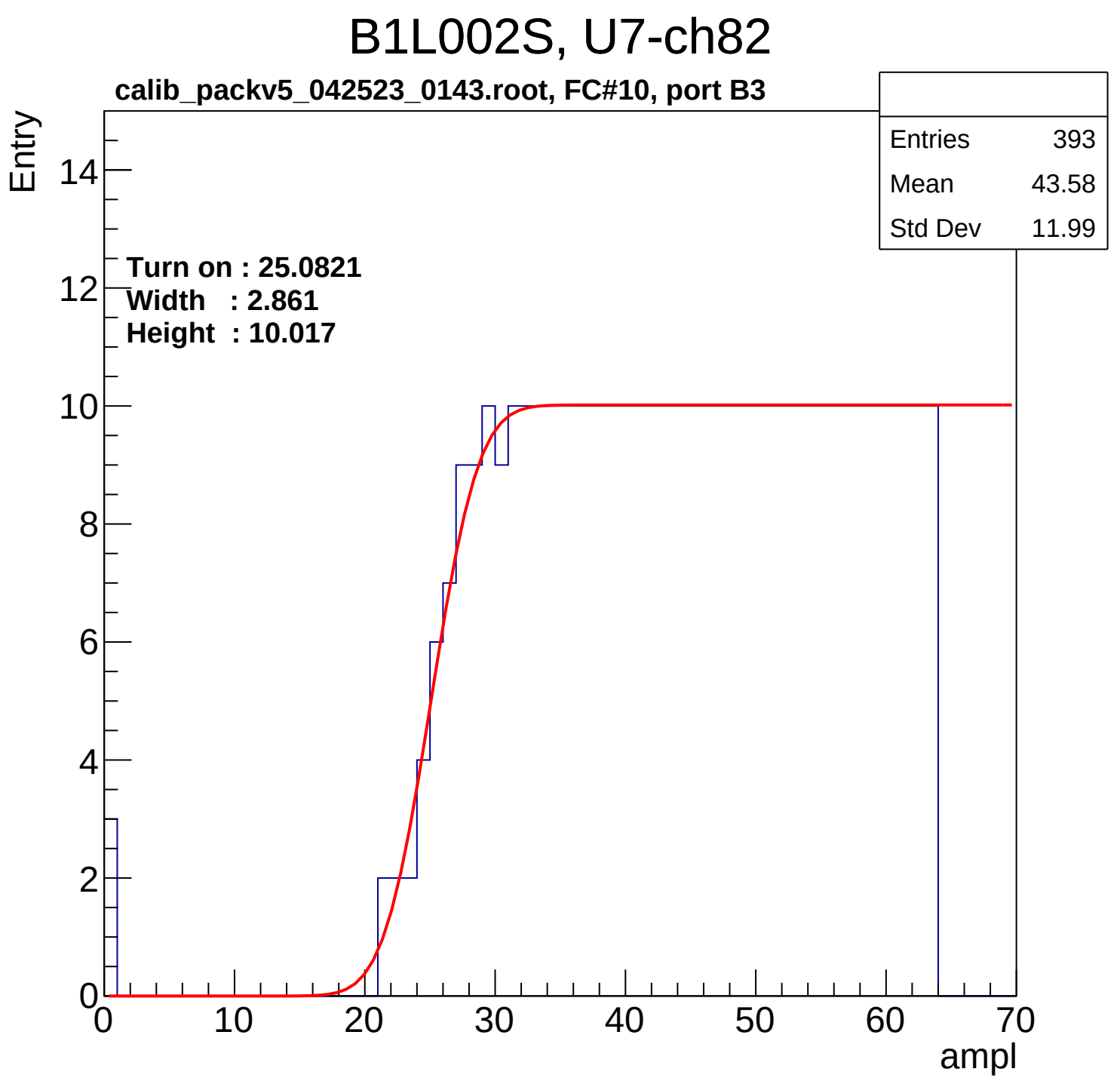
B1L002S, U7-ch82
calib_packv5_042523_0143.root, FC#10, port B3
Entries 393
Mean 43.58
Std Dev 11.99
Turn on : 25.0821
Width : 2.861
Height : 10.017
Entry
ampl
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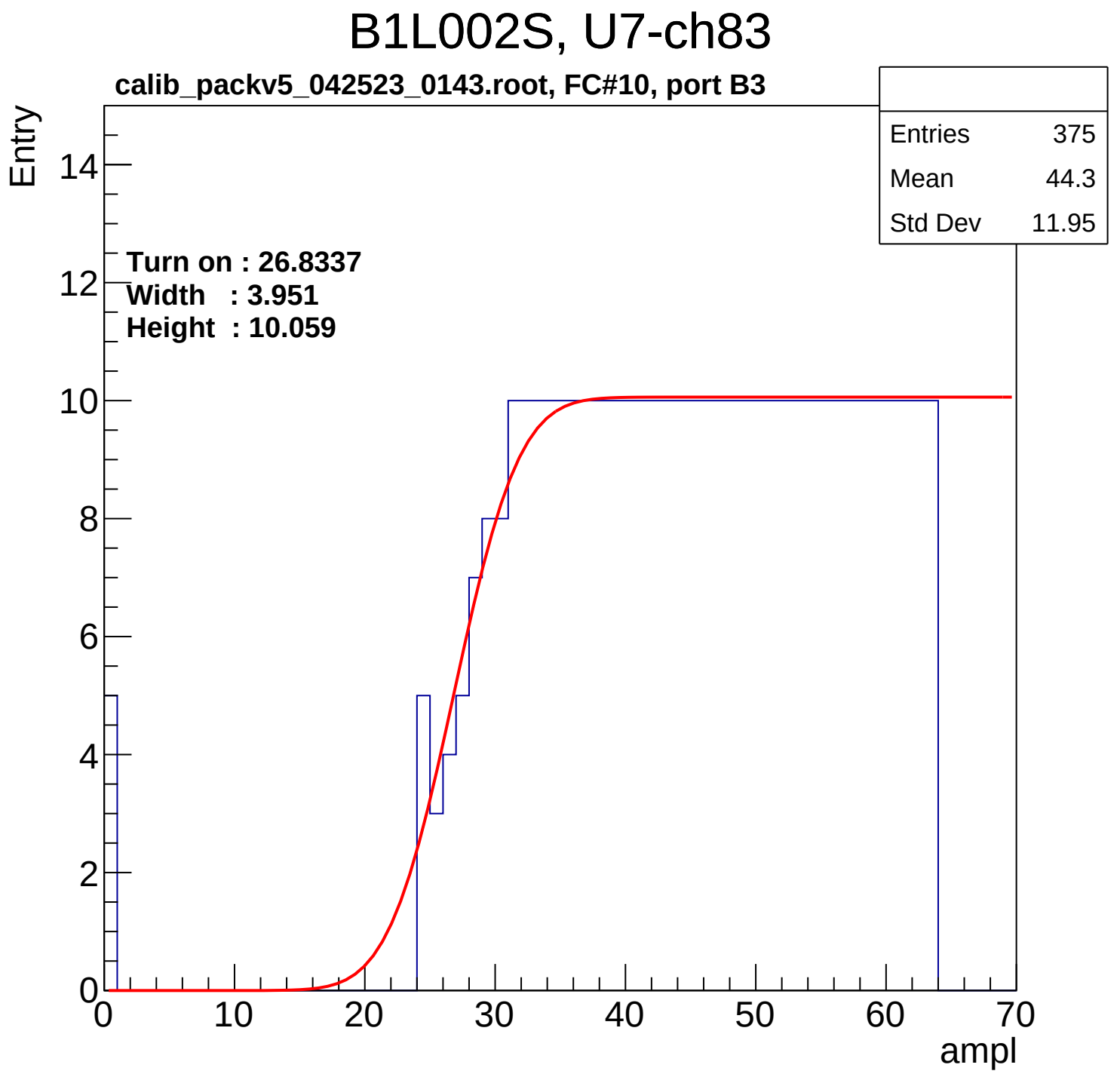
B1L002S, U7-ch83
calib_packv5_042523_0143.root, FC#10, port B3
Entries 375
Mean 44.3
Std Dev 11.95
Turn on : 26.8337
Width : 3.951
Height : 10.059
Entry
ampl
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2
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6
8
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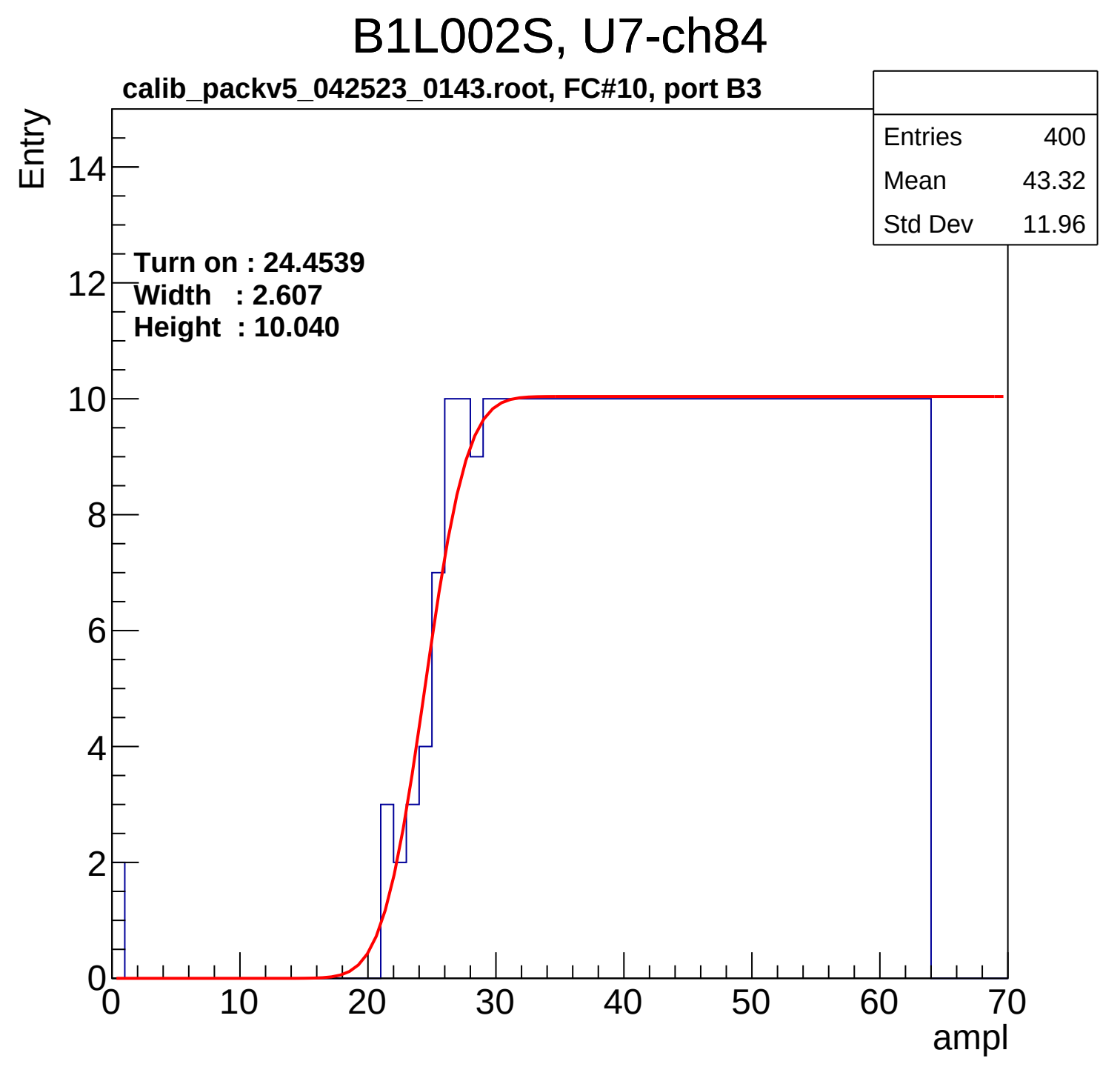
B1L002S, U7-ch84
calib_packv5_042523_0143.root, FC#10, port B3
Entries 400
Mean 43.32
Std Dev 11.96
Turn on : 24.4539
Width : 2.607
Height : 10.040
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ampl
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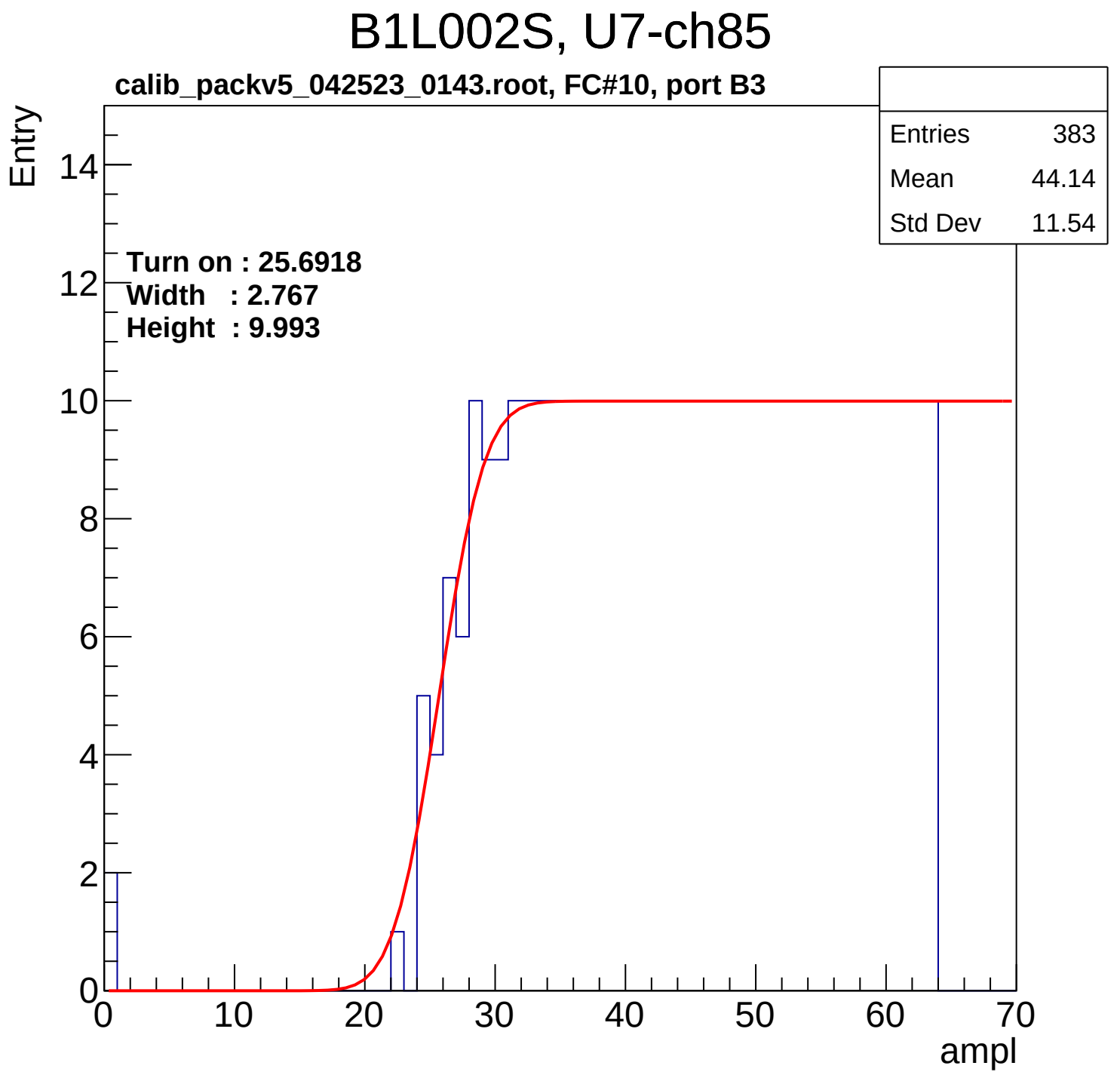
B1L002S, U7-ch85
calib_packv5_042523_0143.root, FC#10, port B3
Entries 383
Mean 44.14
Std Dev 11.54
Turn on : 25.6918
Width : 2.767
Height : 9.993
Entry
ampl
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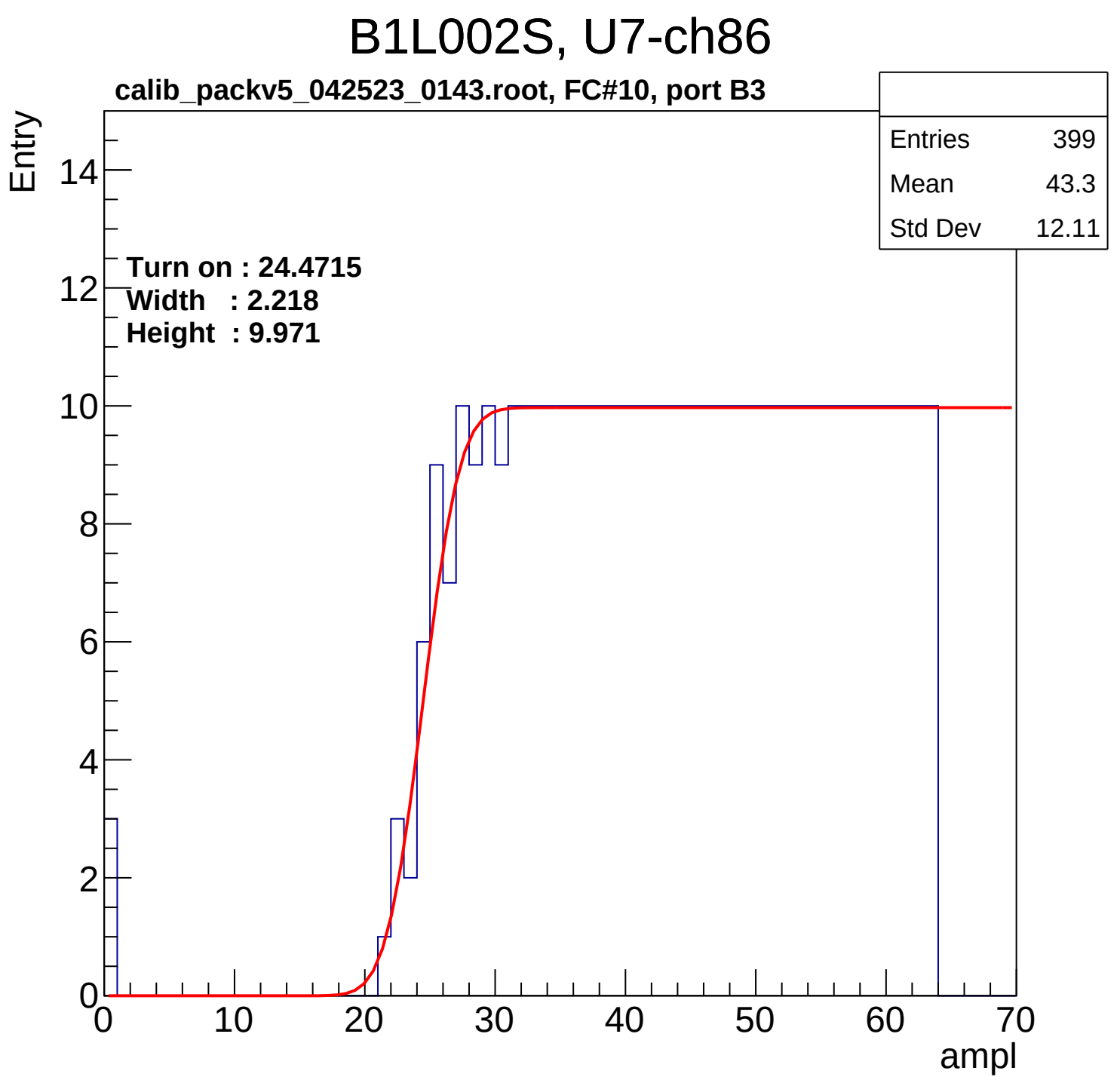
B1L002S, U7-ch86
calib_packv5_042523_0143.root, FC#10, port B3
Entries 399
Mean 43.3
Std Dev 12.11
Turn on : 24.4715
Width : 2.218
Height : 9.971
Entry
ampl
0
2
4
6
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12
14
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10
20
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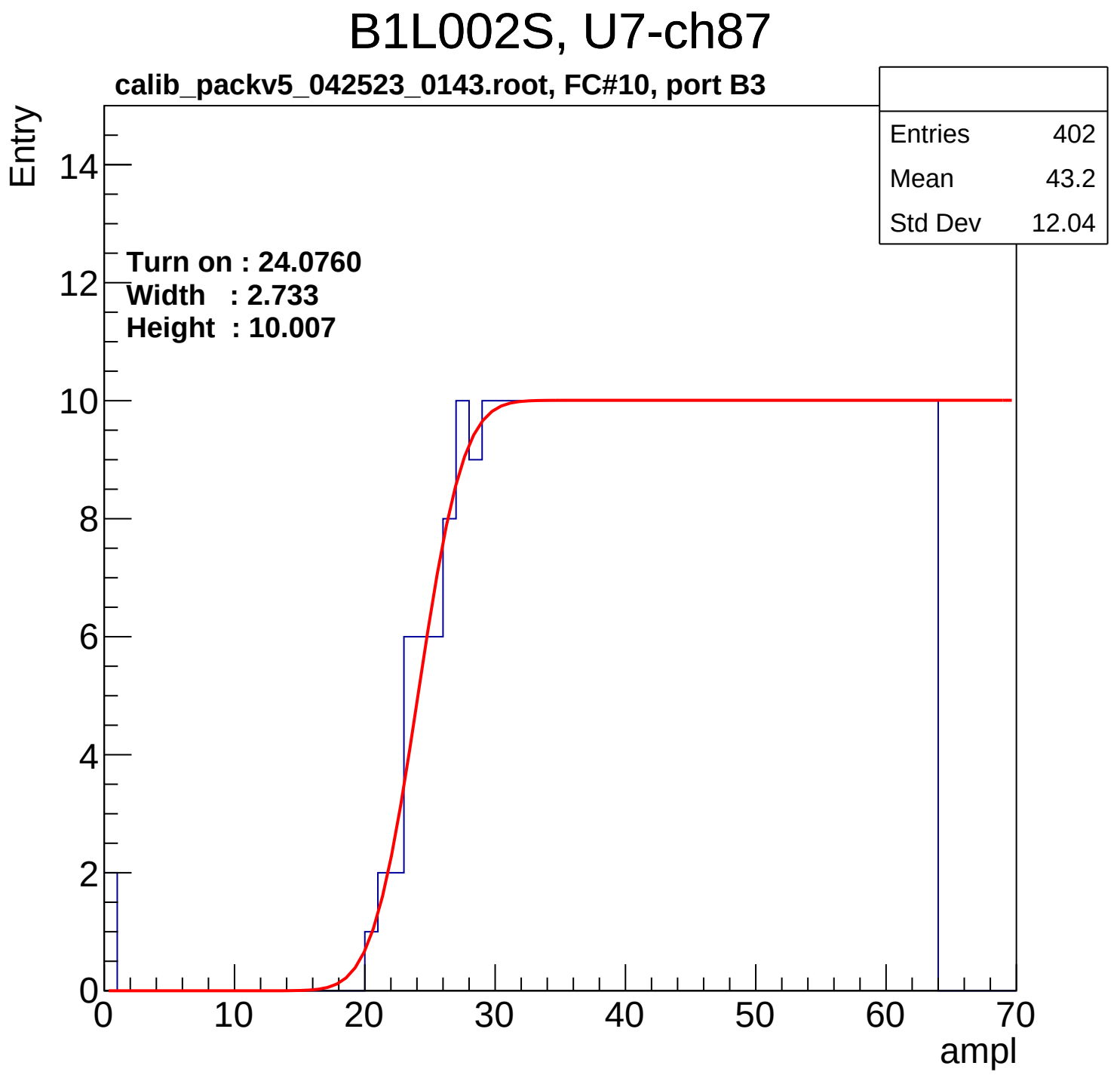
B1L002S, U7-ch87
calib_packv5_042523_0143.root, FC#10, port B3
Entries 402
Mean 43.2
Std Dev 12.04
Turn on : 24.0760
Width : 2.733
Height : 10.007
Entry
ampl
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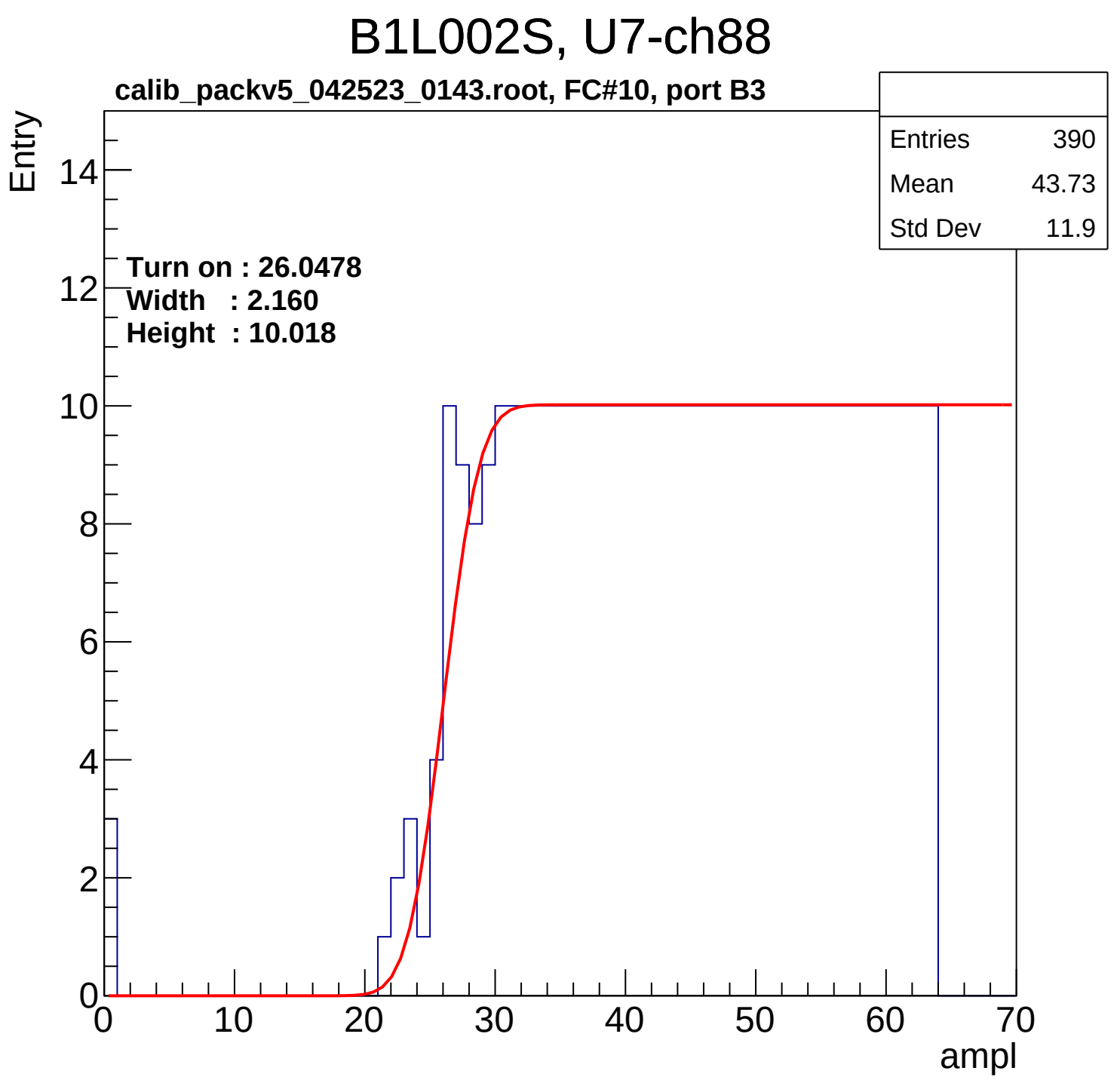
B1L002S, U7-ch88
calib_packv5_042523_0143.root, FC#10, port B3
Entries 390
Mean 43.73
Std Dev 11.9
Turn on : 26.0478
Width : 2.160
Height : 10.018
Entry
ampl
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2
4
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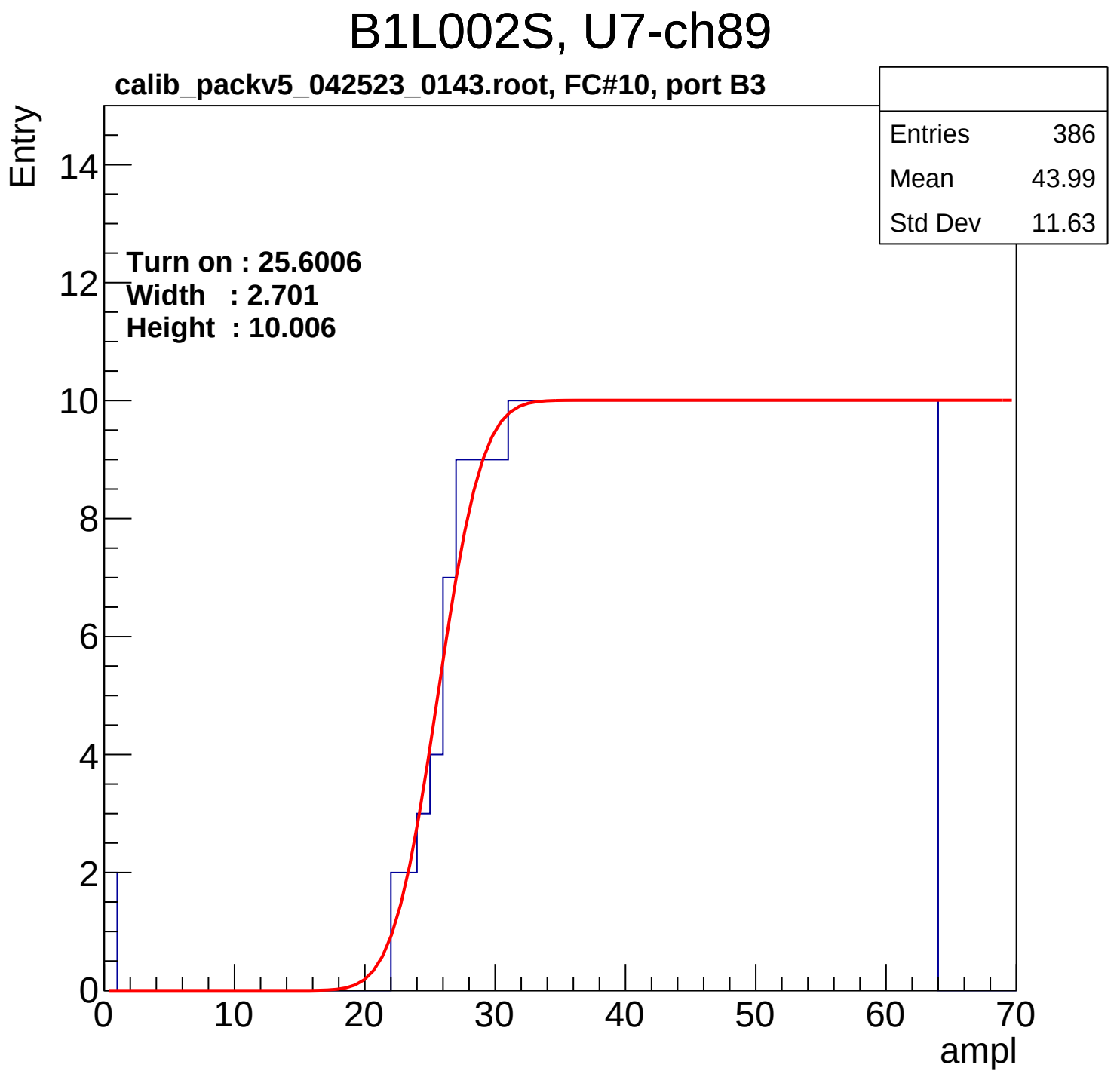
B1L002S, U7-ch89
calib_packv5_042523_0143.root, FC#10, port B3
Entries 386
Mean 43.99
Std Dev 11.63
Turn on : 25.6006
Width : 2.701
Height : 10.006
Entry
ampl
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2
4
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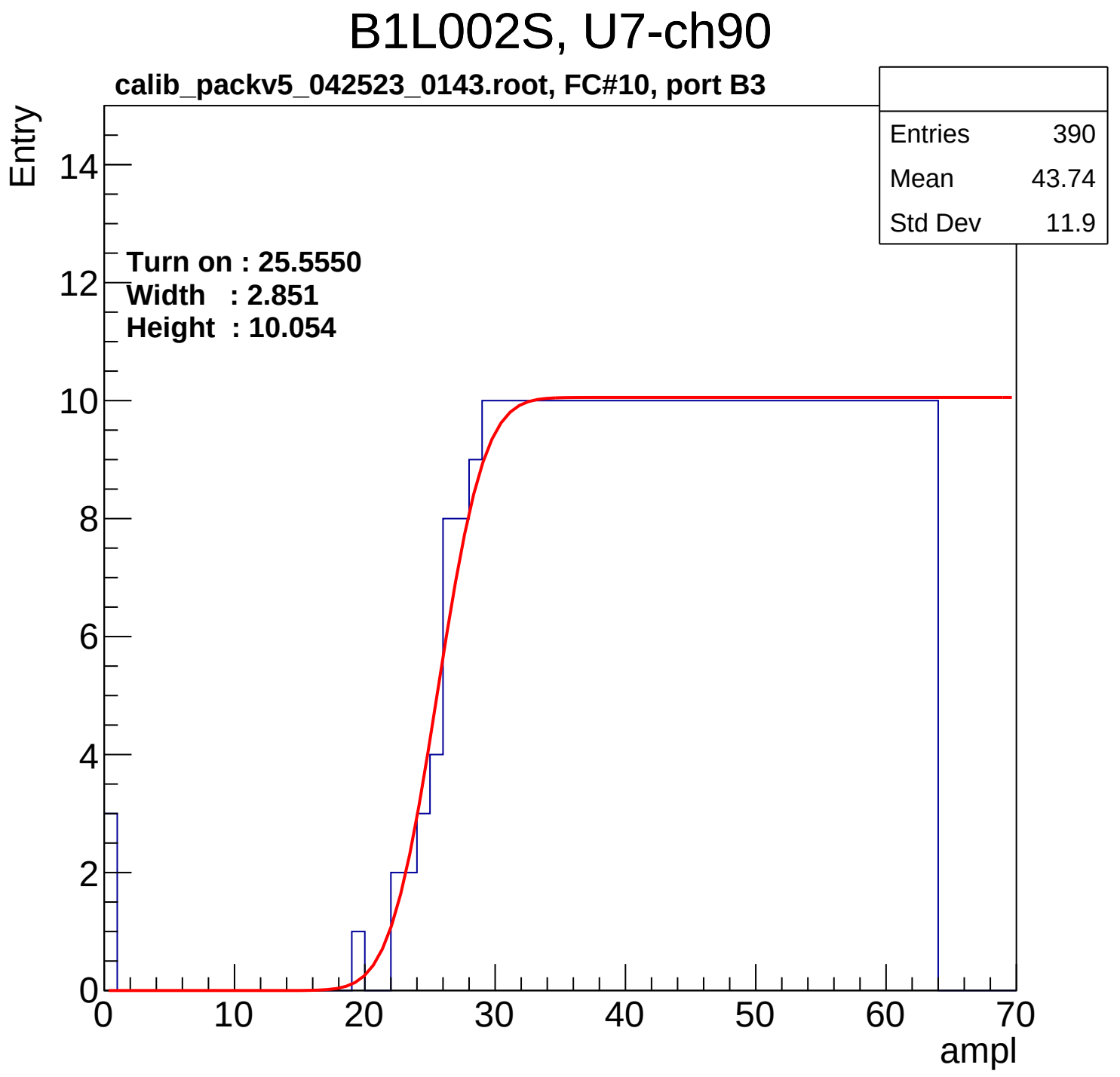
B1L002S, U7-ch90
calib_packv5_042523_0143.root, FC#10, port B3
Entries 390
Mean 43.74
Std Dev 11.9
Turn on : 25.5550
Width : 2.851
Height : 10.054
Entry
ampl
0
2
4
6
8
10
12
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0
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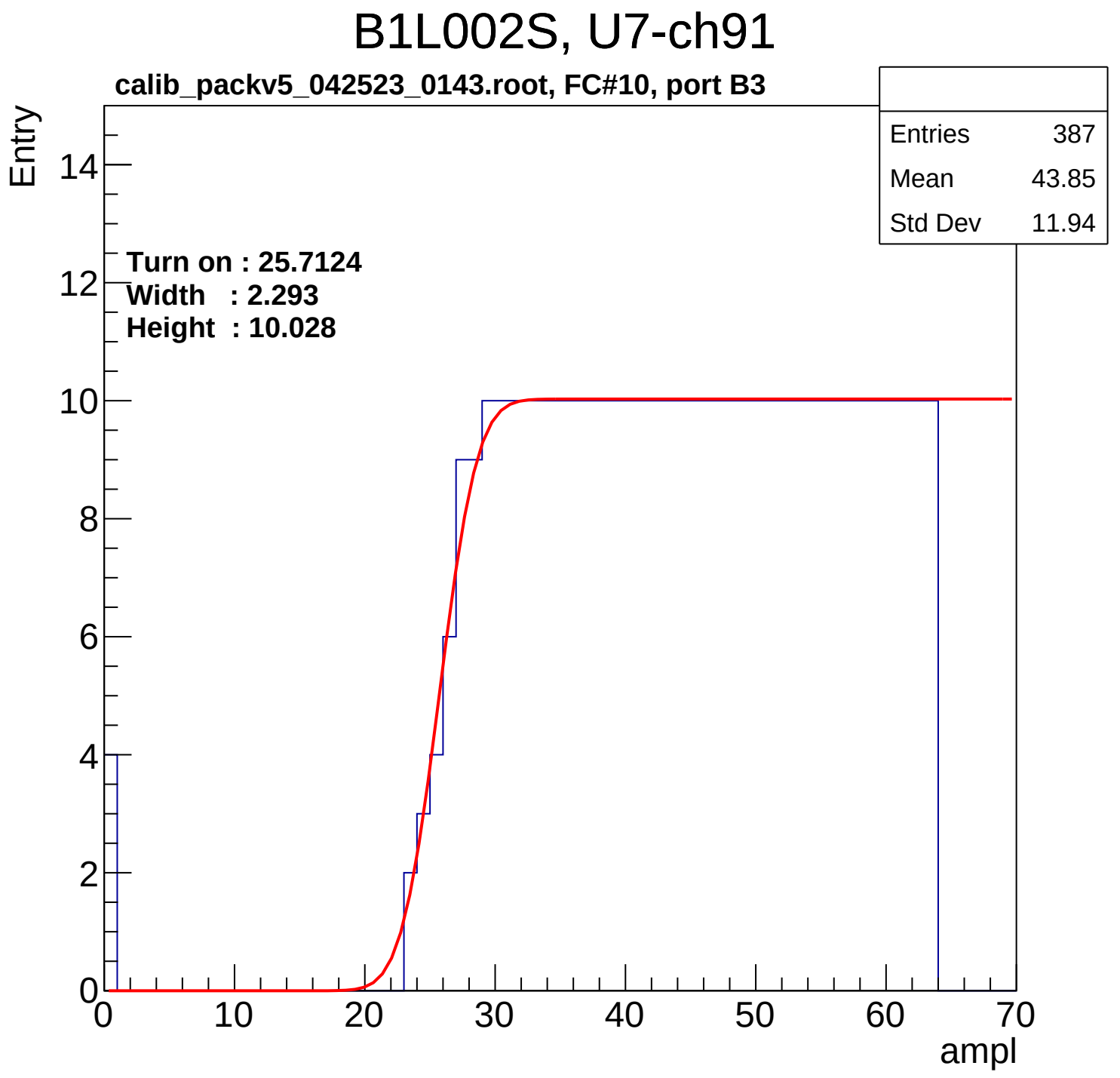
B1L002S, U7-ch91
calib_packv5_042523_0143.root, FC#10, port B3
Entries 387
Mean 43.85
Std Dev 11.94
Turn on : 25.7124
Width : 2.293
Height : 10.028
Entry
ampl
0
2
4
6
8
10
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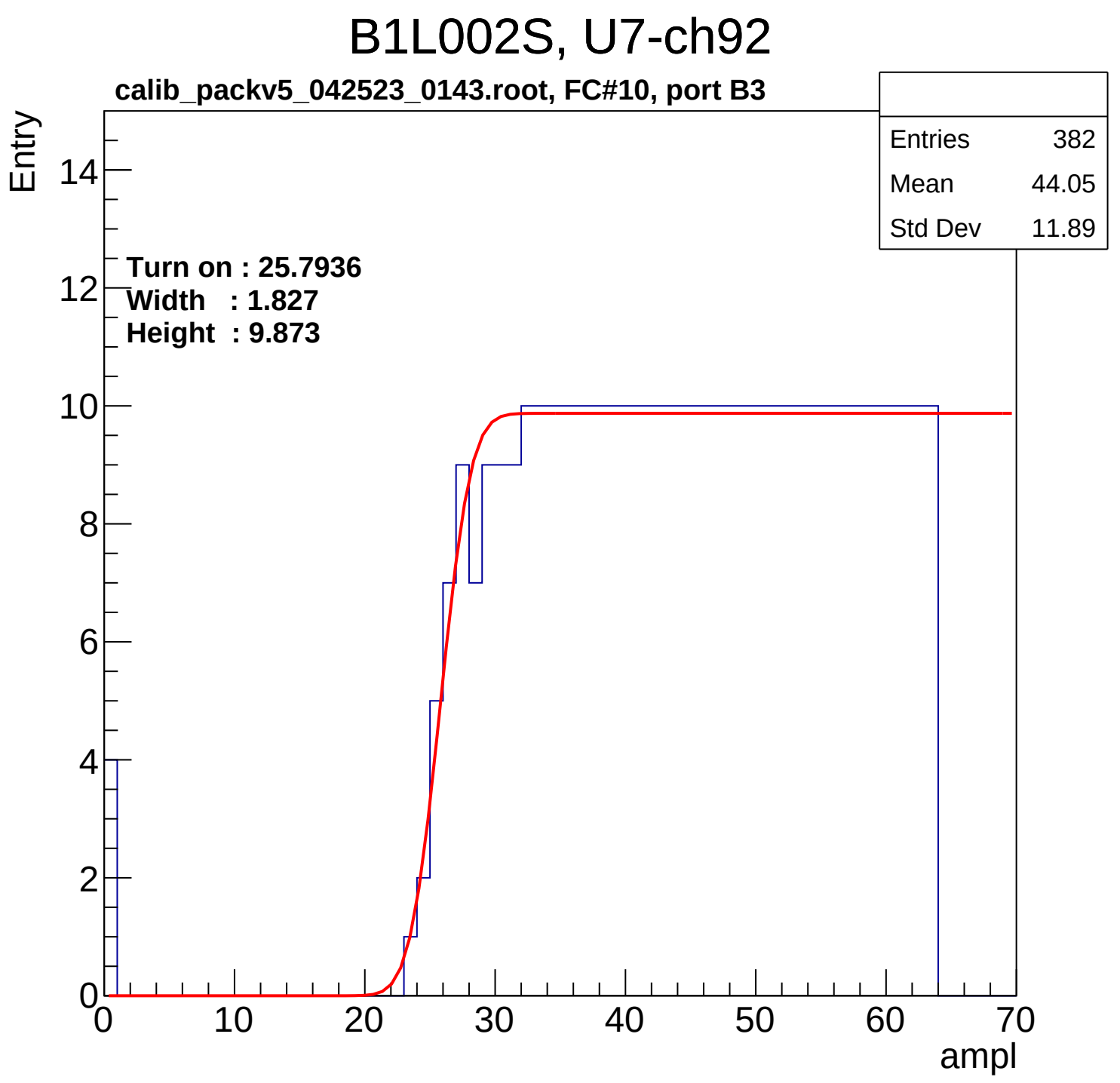
B1L002S, U7-ch92
calib_packv5_042523_0143.root, FC#10, port B3
Entries 382
Mean 44.05
Std Dev 11.89
Turn on : 25.7936
Width : 1.827
Height : 9.873
Entry
ampl
0
2
4
6
8
10
12
14
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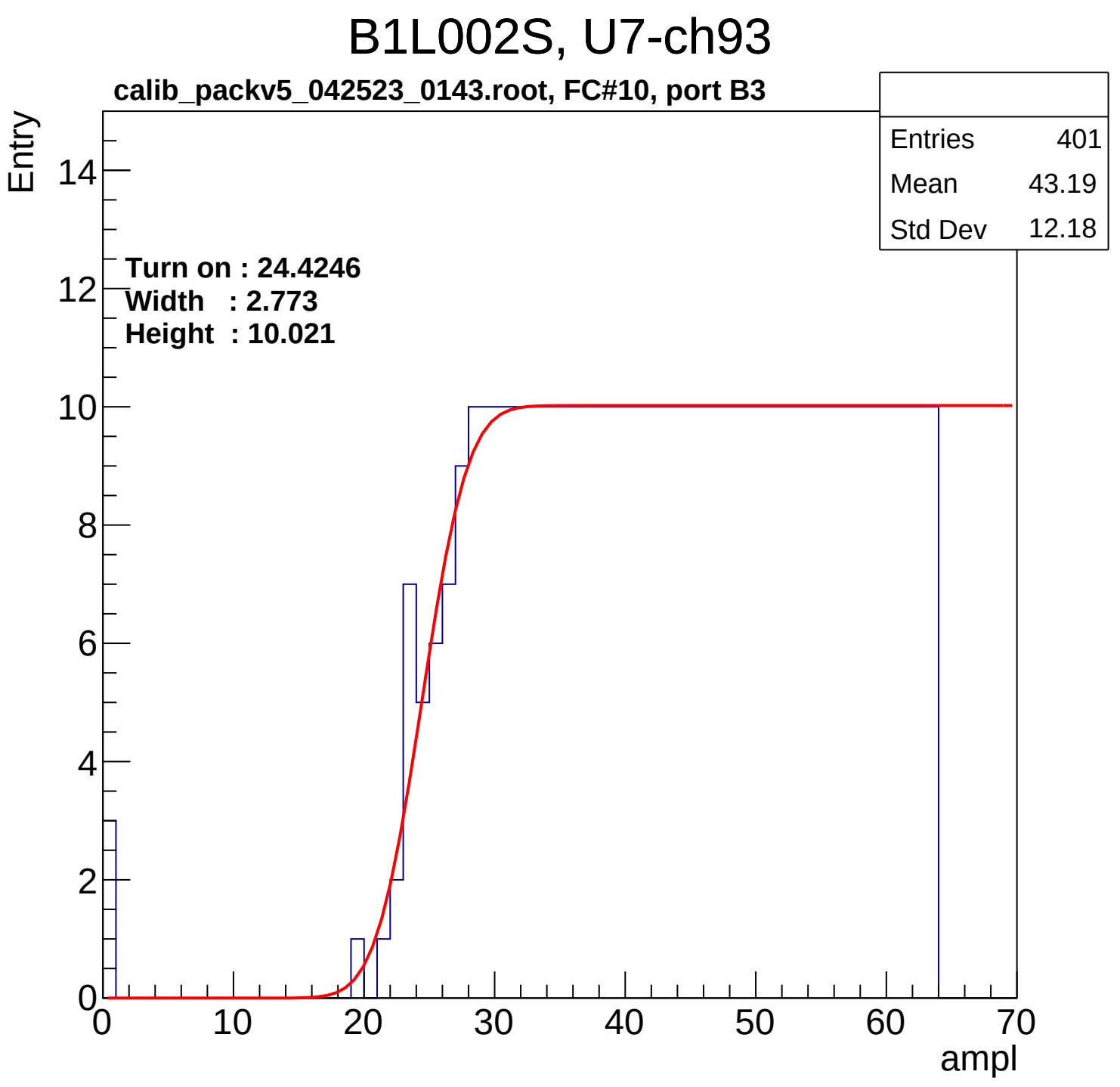
B1L002S, U7-ch93
calib_packv5_042523_0143.root, FC#10, port B3
Entries 401
Mean 43.19
Std Dev 12.18
Turn on : 24.4246
Width : 2.773
Height : 10.021
Entry
ampl
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2
4
6
8
10
12
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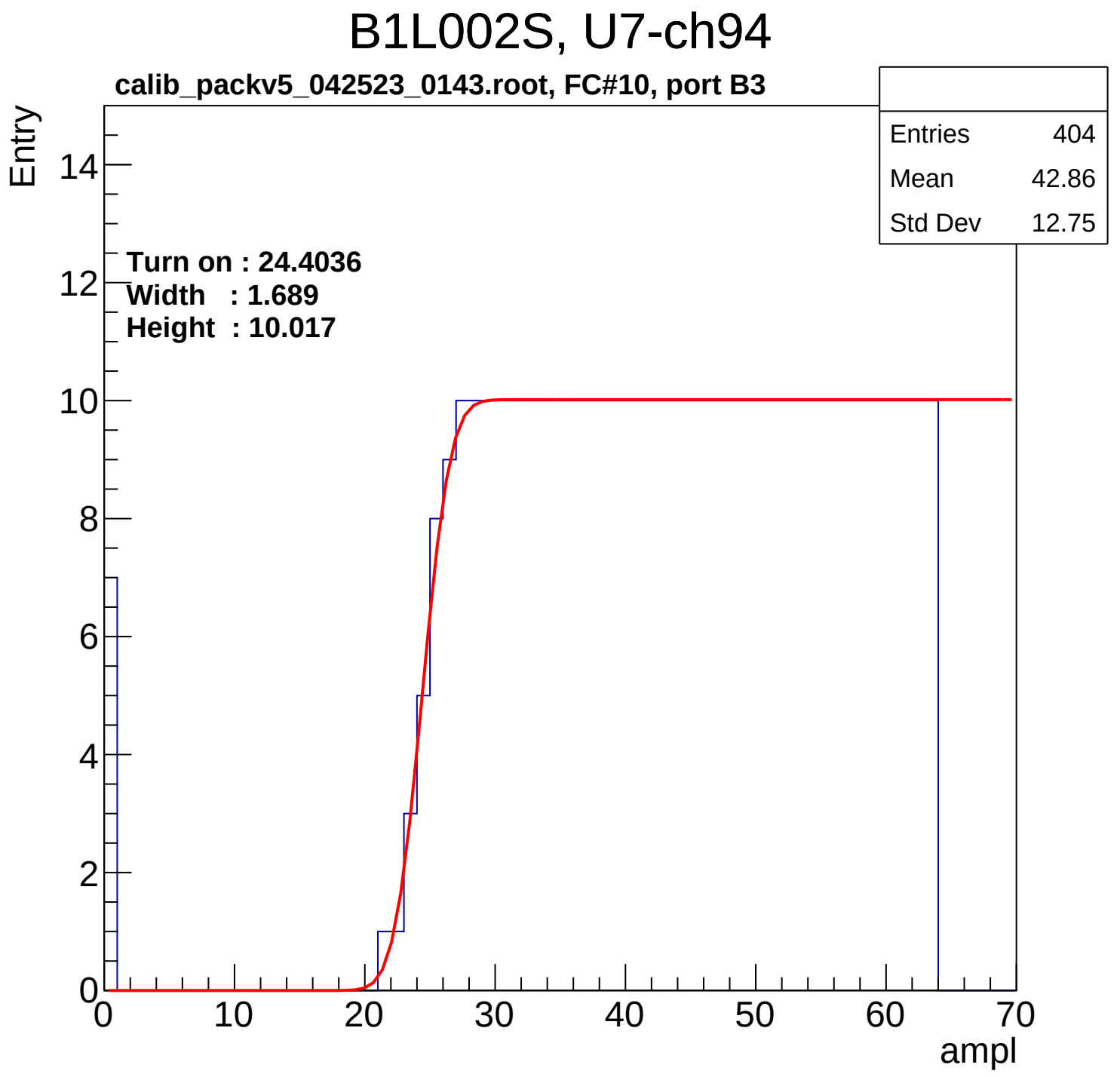
B1L002S, U7-ch94
calib_packv5_042523_0143.root, FC#10, port B3
Entries 404
Mean 42.86
Std Dev 12.75
Turn on : 24.4036
Width : 1.689
Height : 10.017
Entry
ampl
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2
4
6
8
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12
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60
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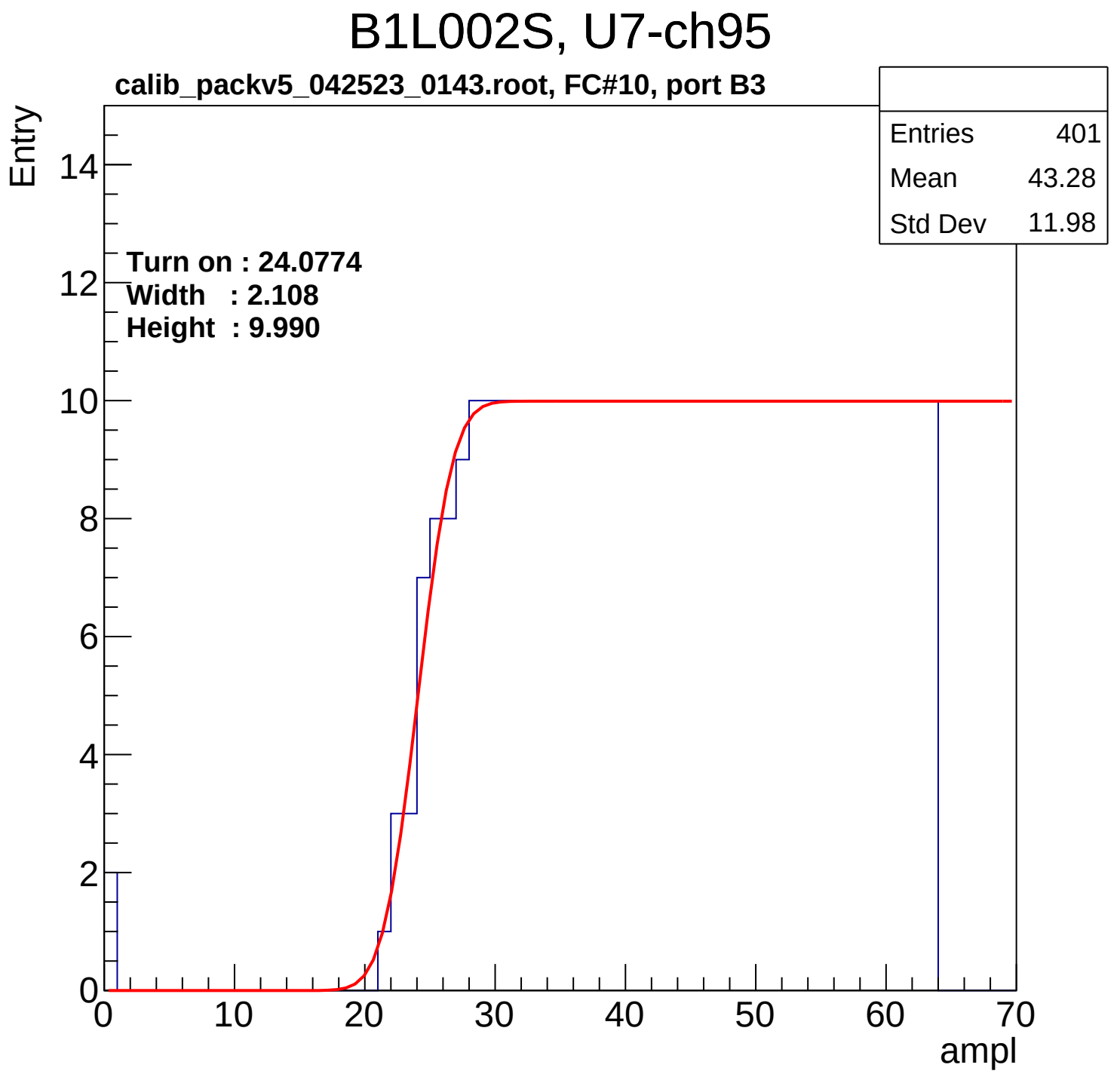
B1L002S, U7-ch95
calib_packv5_042523_0143.root, FC#10, port B3
Entries 401
Mean 43.28
Std Dev 11.98
Turn on : 24.0774
Width : 2.108
Height : 9.990
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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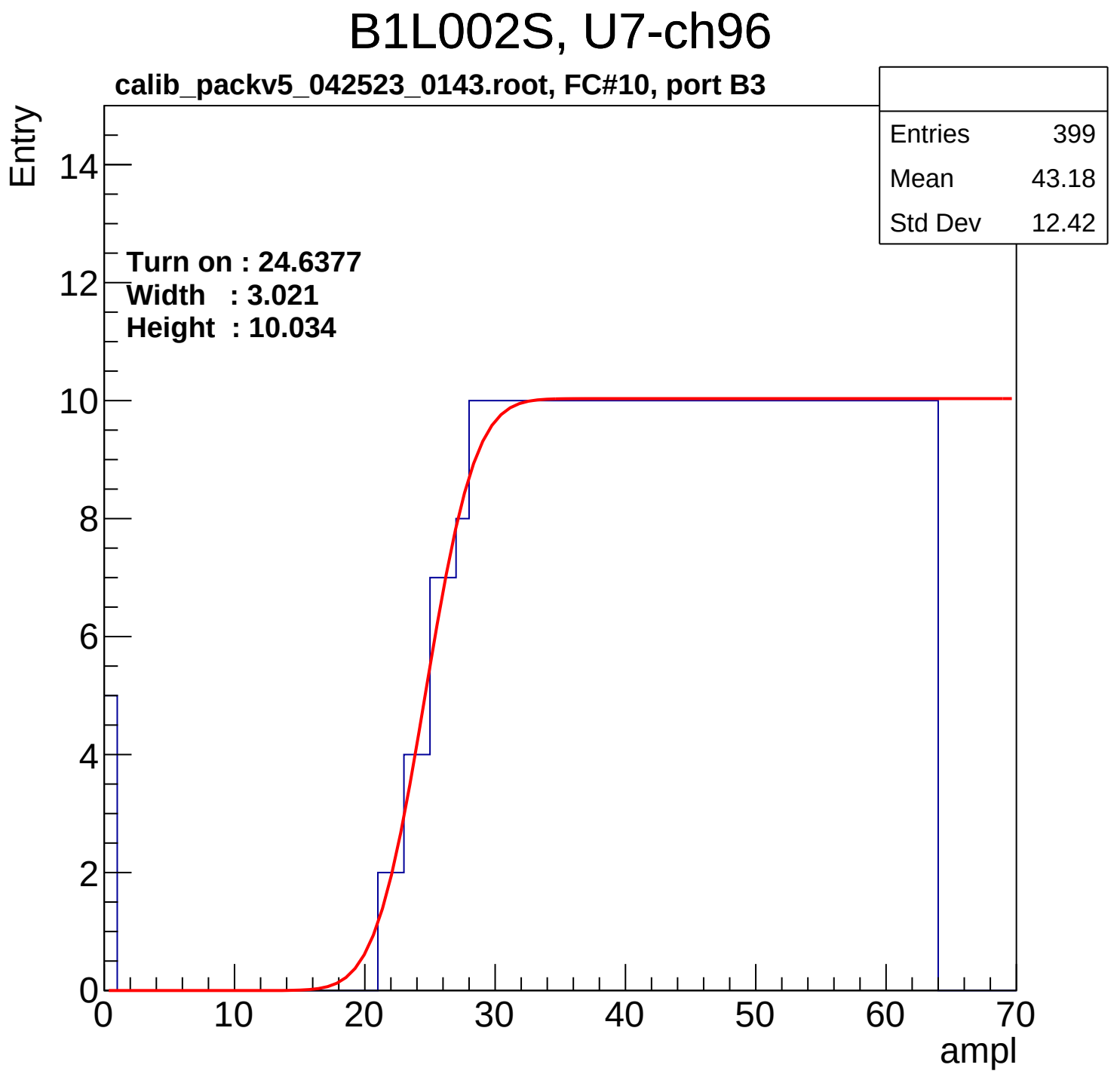
B1L002S, U7-ch96
calib_packv5_042523_0143.root, FC#10, port B3
Entries 399
Mean 43.18
Std Dev 12.42
Turn on : 24.6377
Width : 3.021
Height : 10.034
Entry
ampl
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4
6
8
10
12
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60
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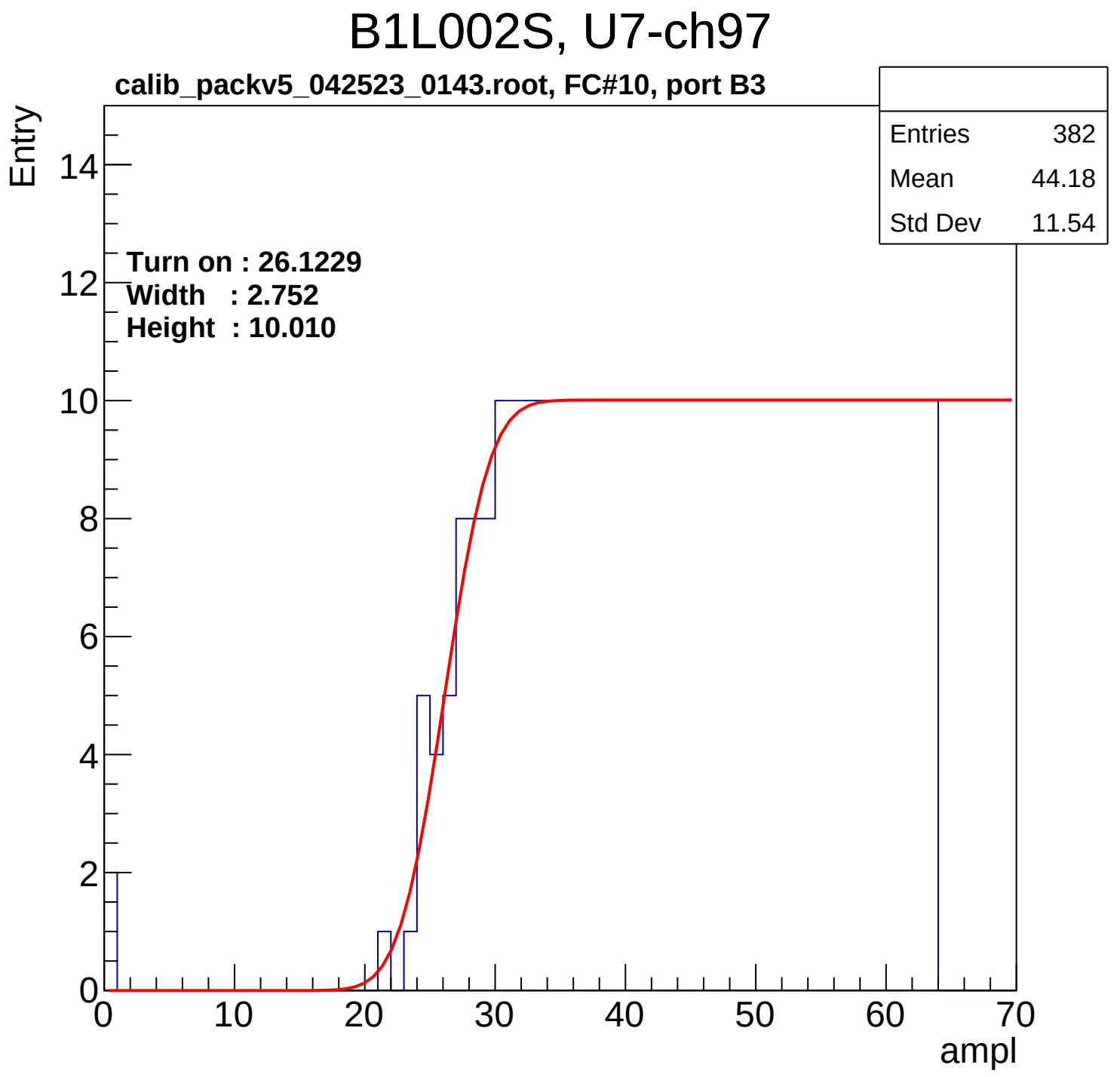
B1L002S, U7-ch97
calib_packv5_042523_0143.root, FC#10, port B3
Entries 382
Mean 44.18
Std Dev 11.54
Turn on : 26.1229
Width : 2.752
Height : 10.010
Entry
ampl
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4
6
8
10
12
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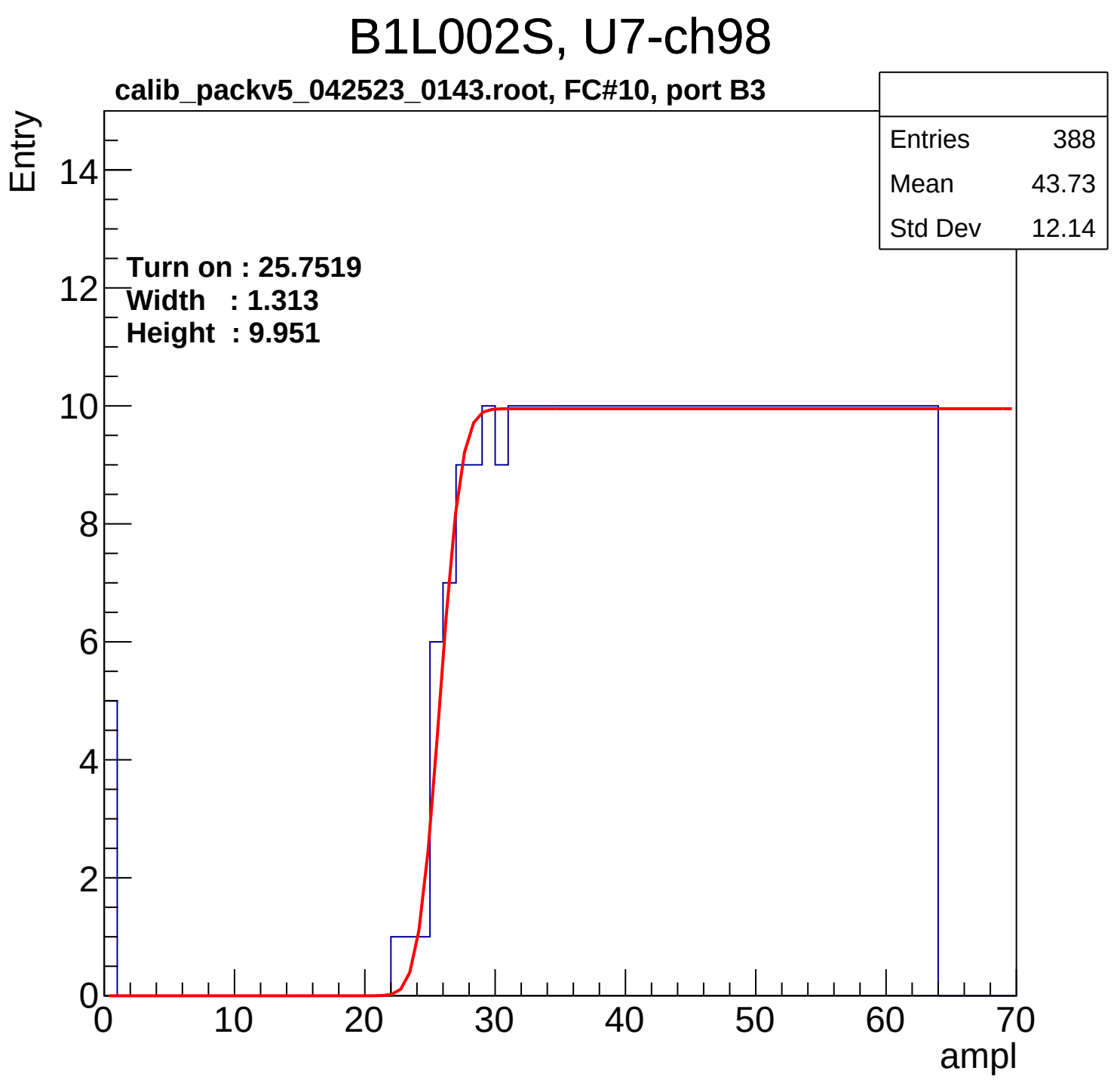
B1L002S, U7-ch98
calib_packv5_042523_0143.root, FC#10, port B3
Entries 388
Mean 43.73
Std Dev 12.14
Turn on : 25.7519
Width : 1.313
Height : 9.951
Entry
ampl
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6
8
10
12
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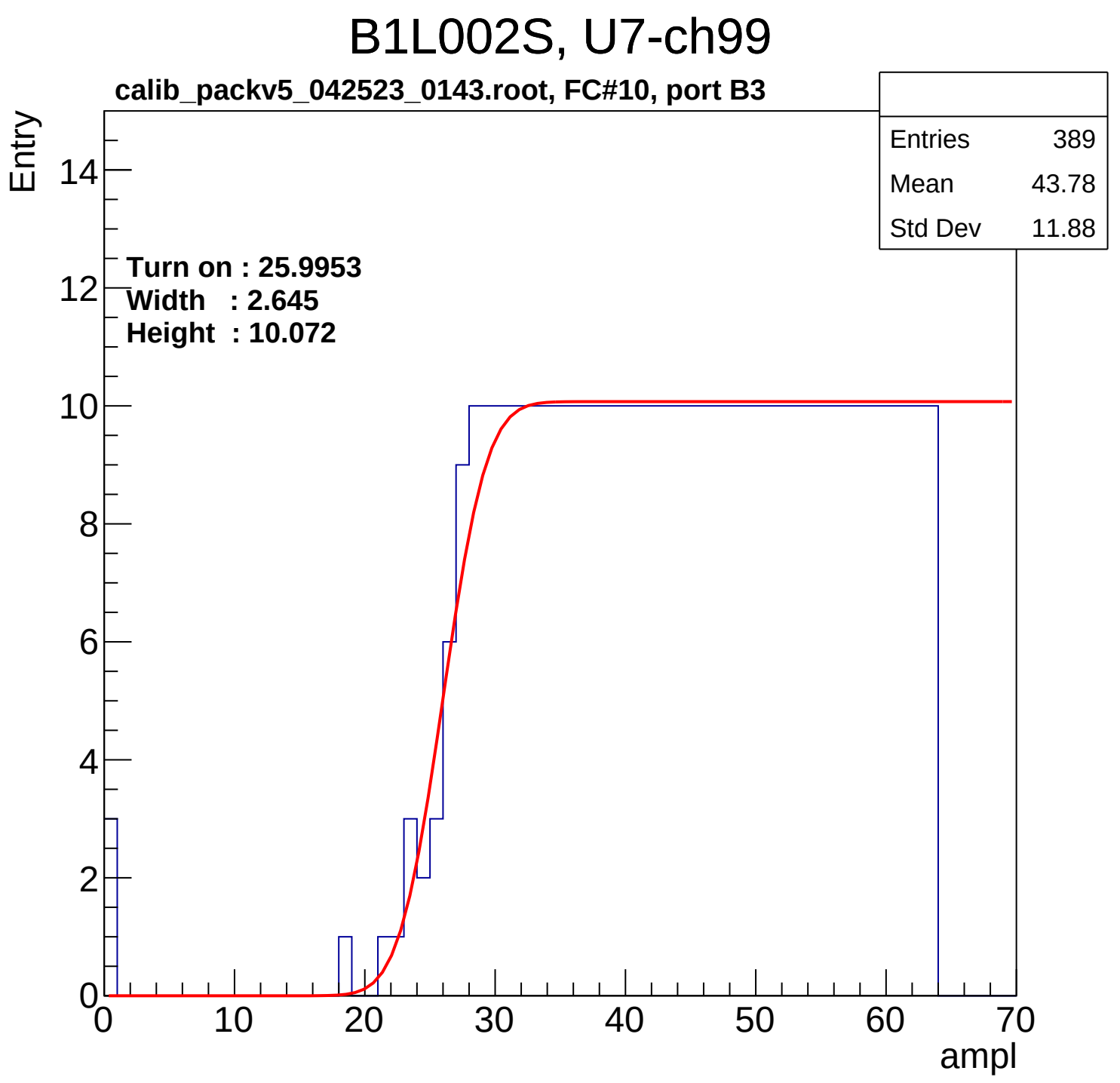
B1L002S, U7-ch99
calib_packv5_042523_0143.root, FC#10, port B3
Entries 389
Mean 43.78
Std Dev 11.88
Turn on : 25.9953
Width : 2.645
Height : 10.072
Entry
ampl
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6
8
10
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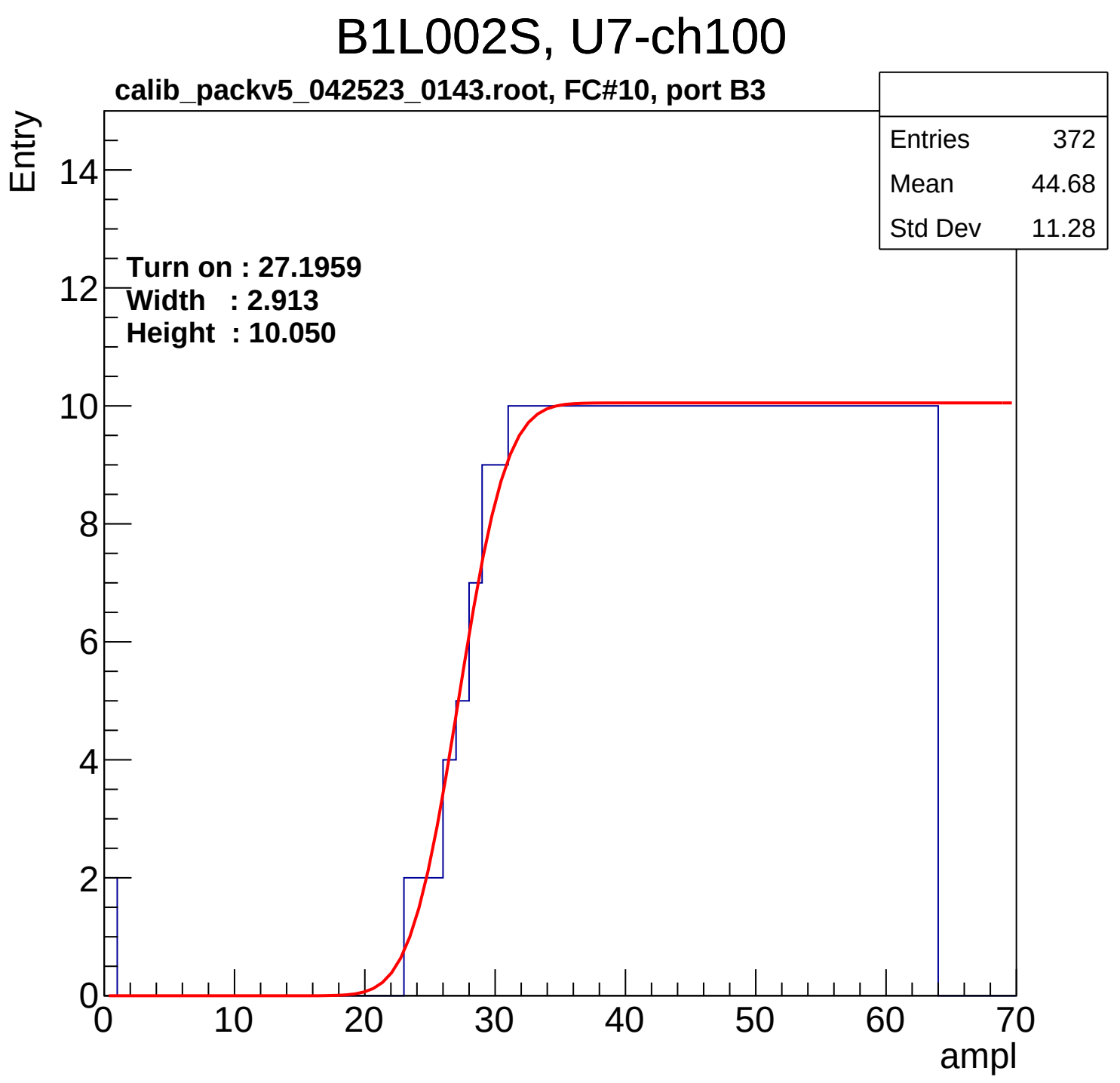
B1L002S, U7-ch100
calib_packv5_042523_0143.root, FC#10, port B3
Entries 372
Mean 44.68
Std Dev 11.28
Turn on : 27.1959
Width : 2.913
Height : 10.050
Entry
ampl
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6
8
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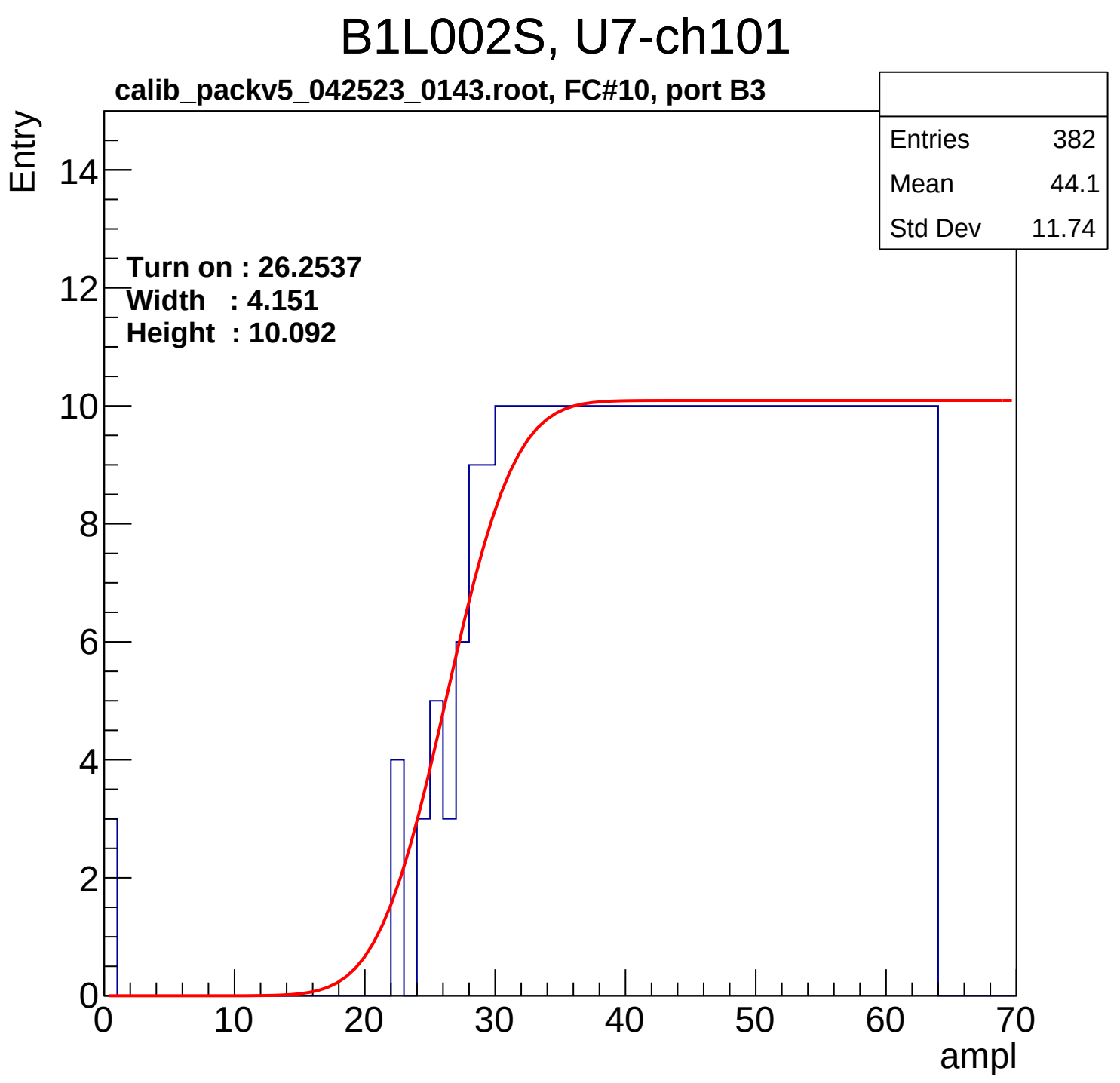
B1L002S, U7-ch101
calib_packv5_042523_0143.root, FC#10, port B3
Entries 382
Mean 44.1
Std Dev 11.74
Turn on : 26.2537
Width : 4.151
Height : 10.092
Entry
ampl
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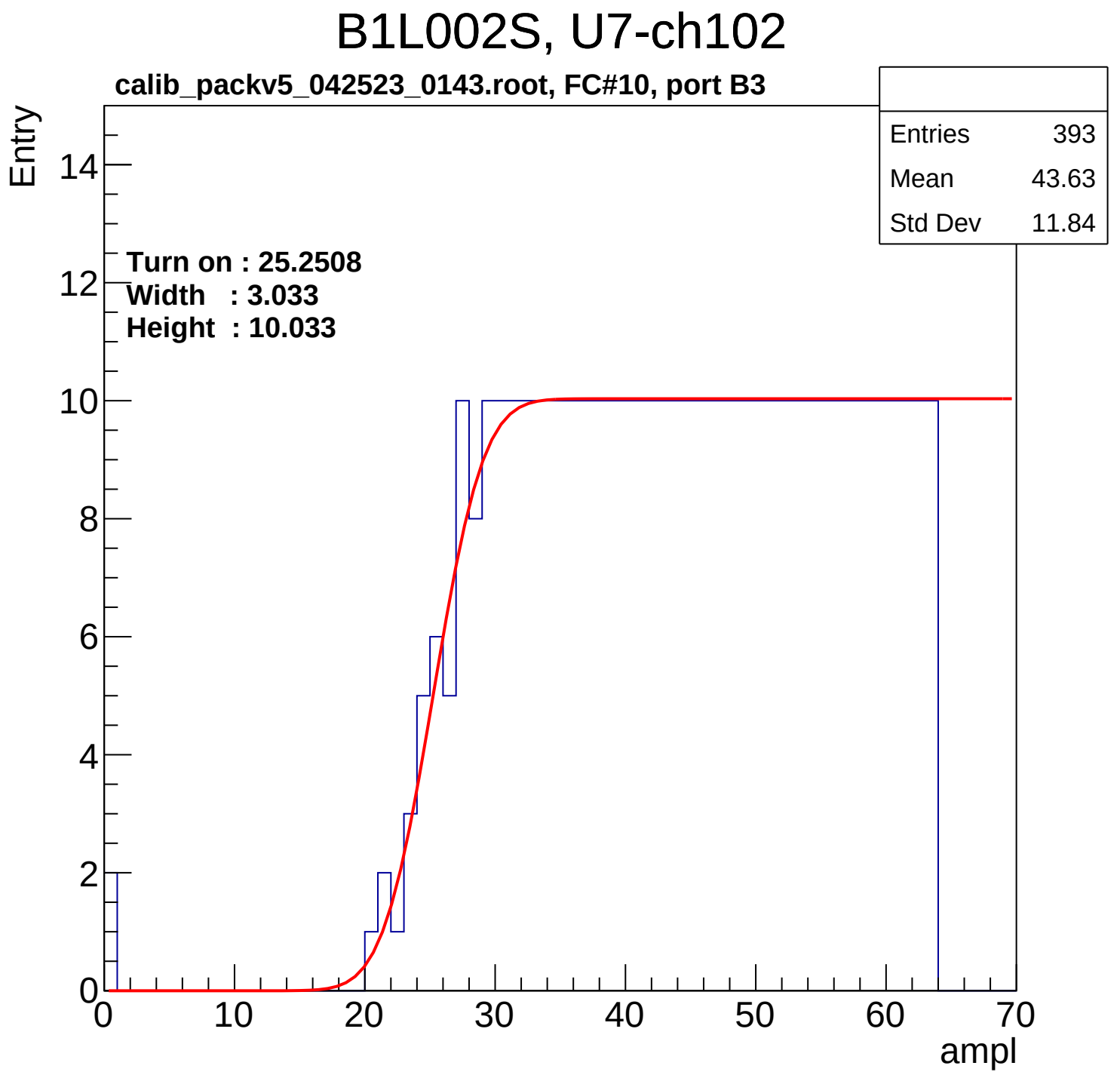
B1L002S, U7-ch102
calib_packv5_042523_0143.root, FC#10, port B3
Entries 393
Mean 43.63
Std Dev 11.84
Turn on : 25.2508
Width : 3.033
Height : 10.033
Entry
ampl
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6
8
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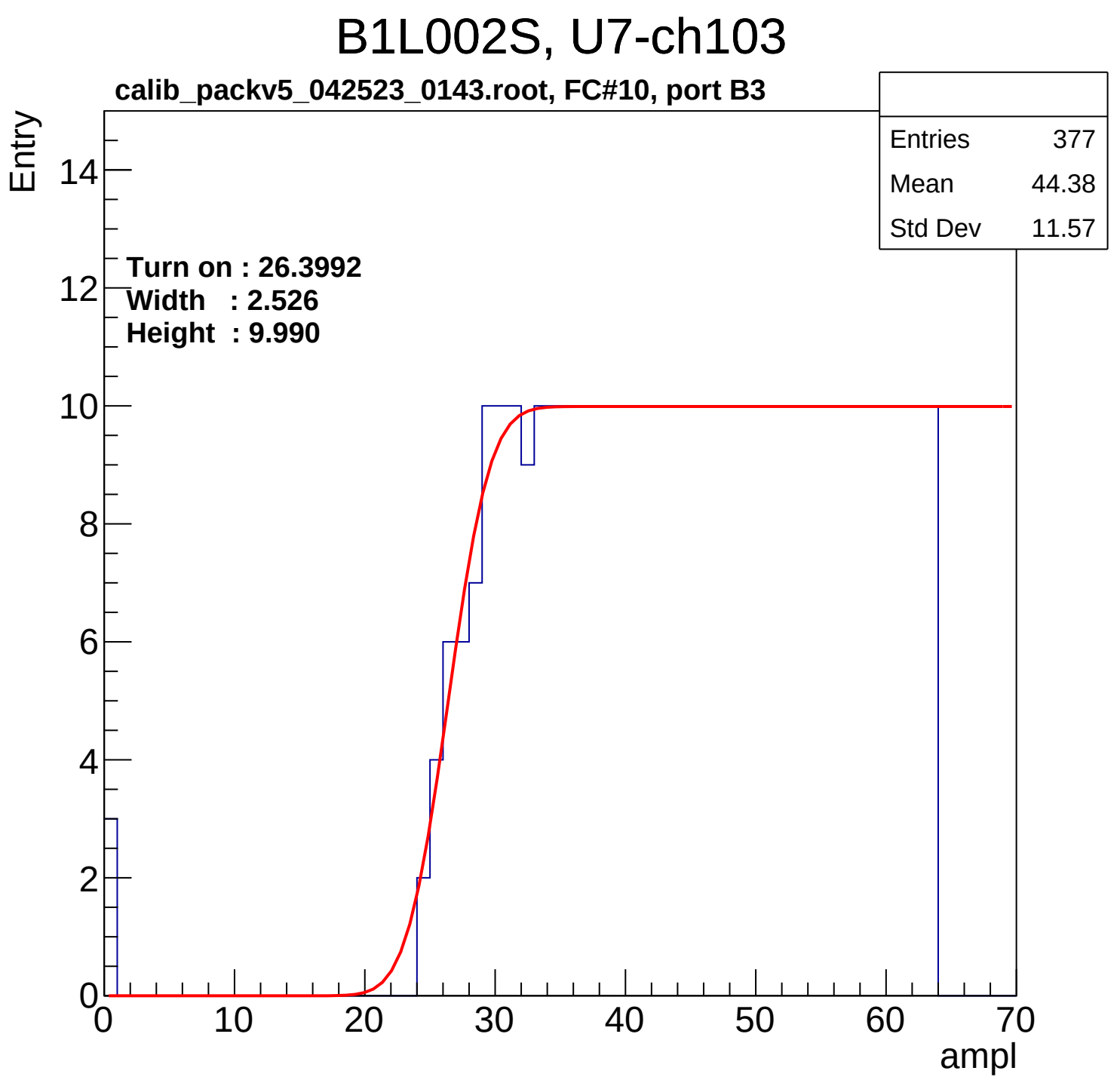
B1L002S, U7-ch103
calib_packv5_042523_0143.root, FC#10, port B3
Entries 377
Mean 44.38
Std Dev 11.57
Turn on : 26.3992
Width : 2.526
Height : 9.990
Entry
ampl
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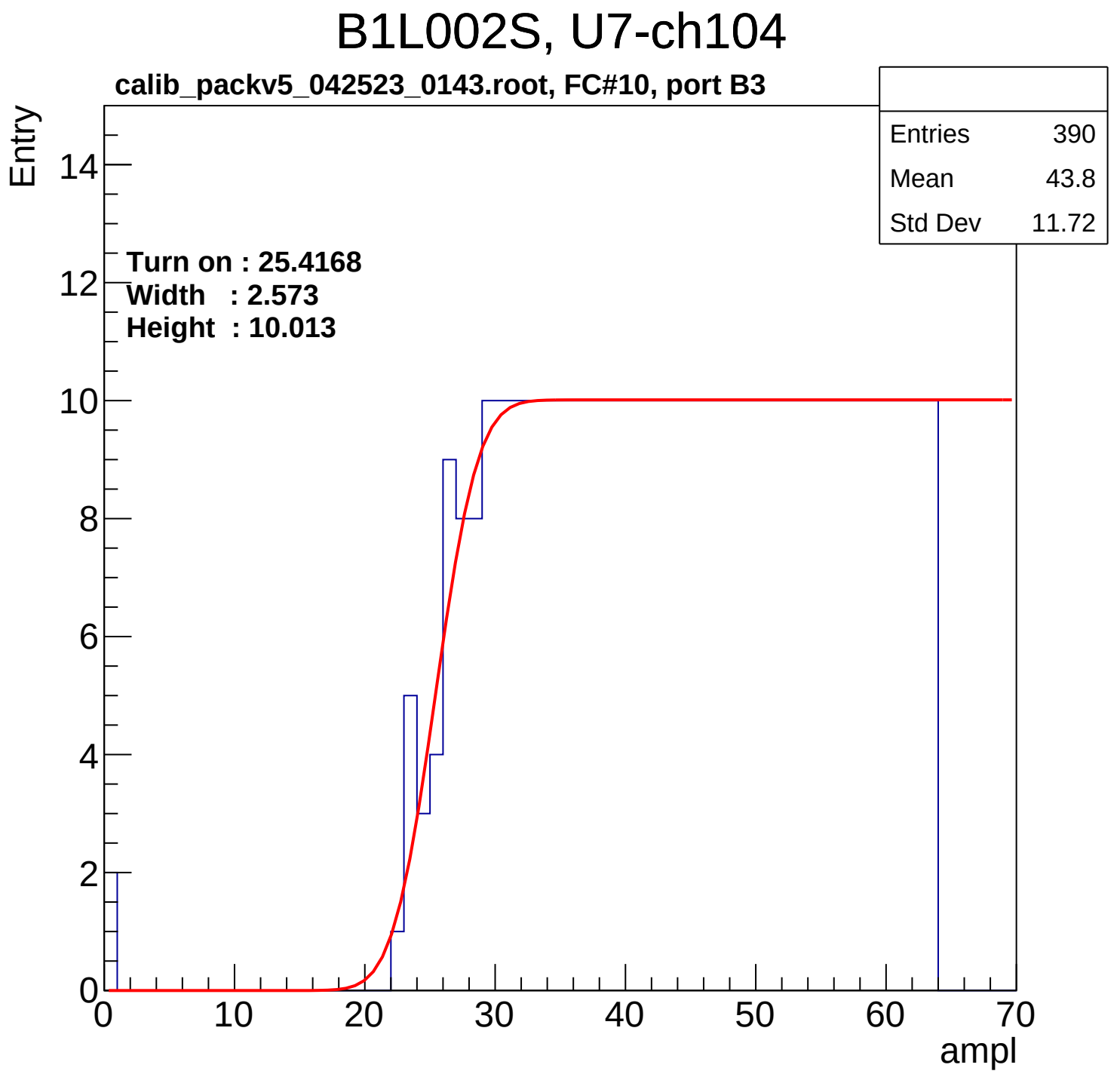
B1L002S, U7-ch104
calib_packv5_042523_0143.root, FC#10, port B3
Entries 390
Mean 43.8
Std Dev 11.72
Turn on : 25.4168
Width : 2.573
Height : 10.013
Entry
ampl
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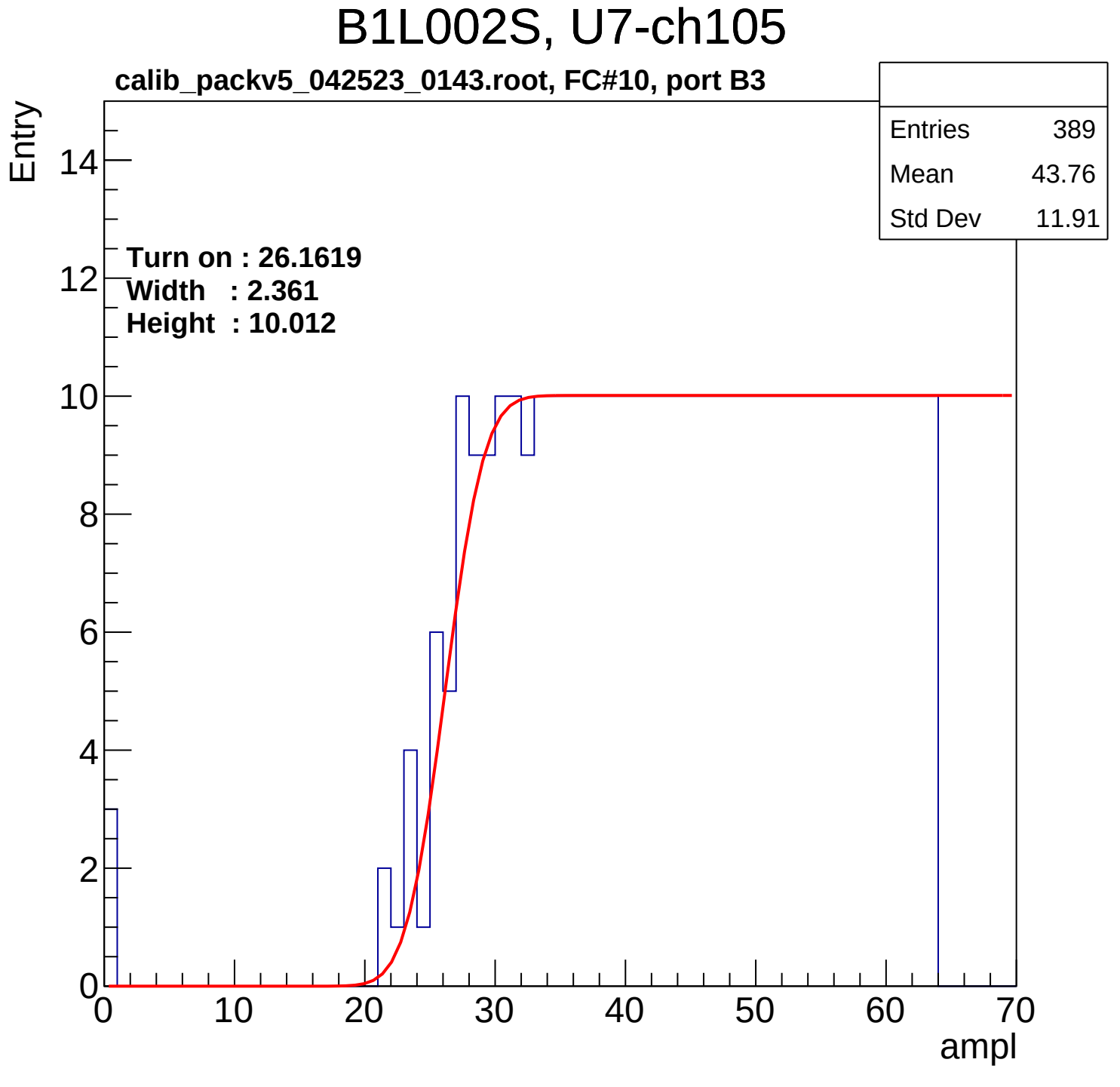
B1L002S, U7-ch105
calib_packv5_042523_0143.root, FC#10, port B3
Entries 389
Mean 43.76
Std Dev 11.91
Turn on : 26.1619
Width : 2.361
Height : 10.012
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ampl
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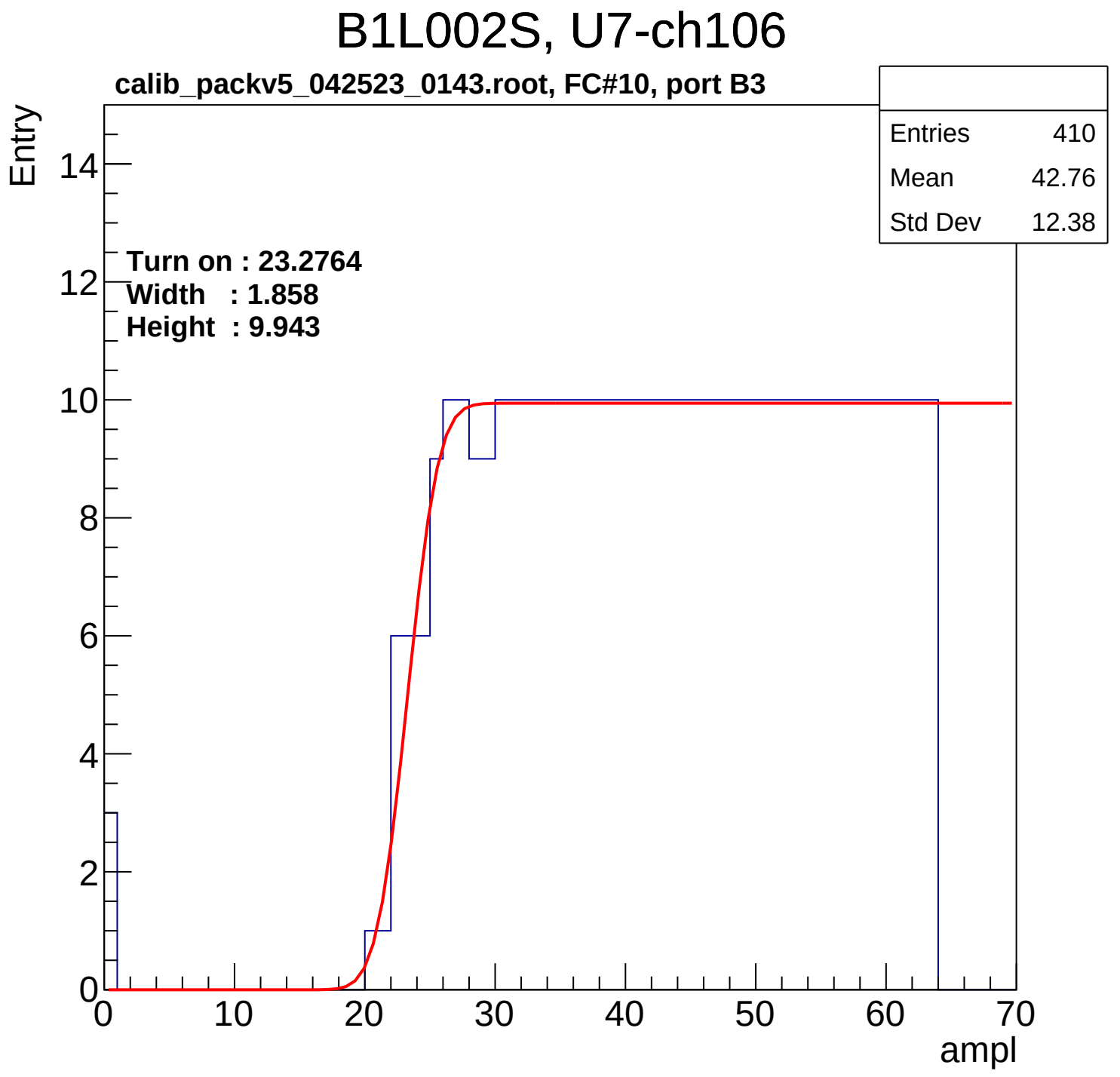
B1L002S, U7-ch106
calib_packv5_042523_0143.root, FC#10, port B3
Entries 410
Mean 42.76
Std Dev 12.38
Turn on : 23.2764
Width : 1.858
Height : 9.943
Entry
ampl
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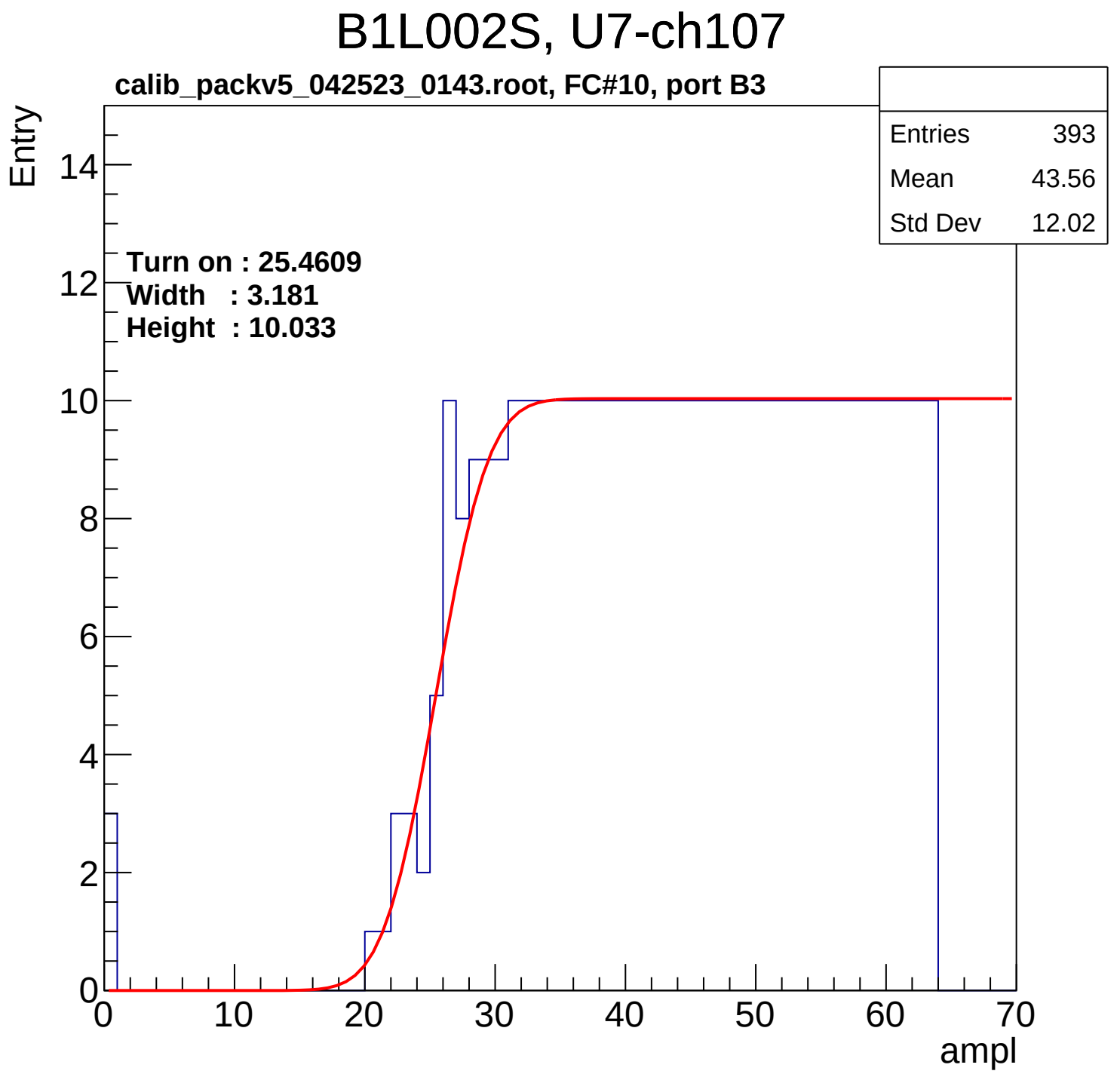
B1L002S, U7-ch107
calib_packv5_042523_0143.root, FC#10, port B3
Entries 393
Mean 43.56
Std Dev 12.02
Turn on : 25.4609
Width : 3.181
Height : 10.033
Entry
ampl
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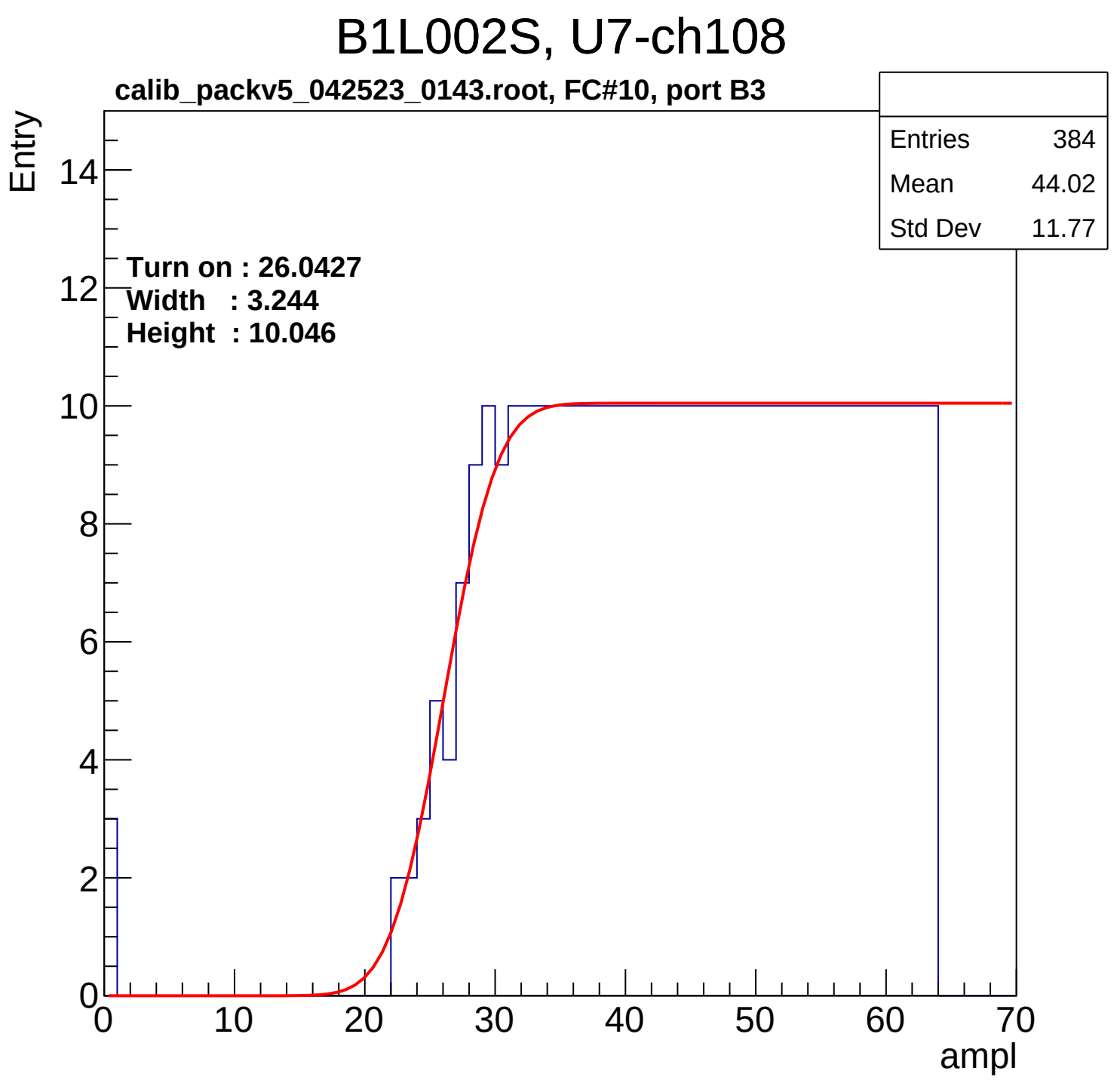
B1L002S, U7-ch108
calib_packv5_042523_0143.root, FC#10, port B3
Entries 384
Mean 44.02
Std Dev 11.77
Turn on : 26.0427
Width : 3.244
Height : 10.046
Entry
ampl
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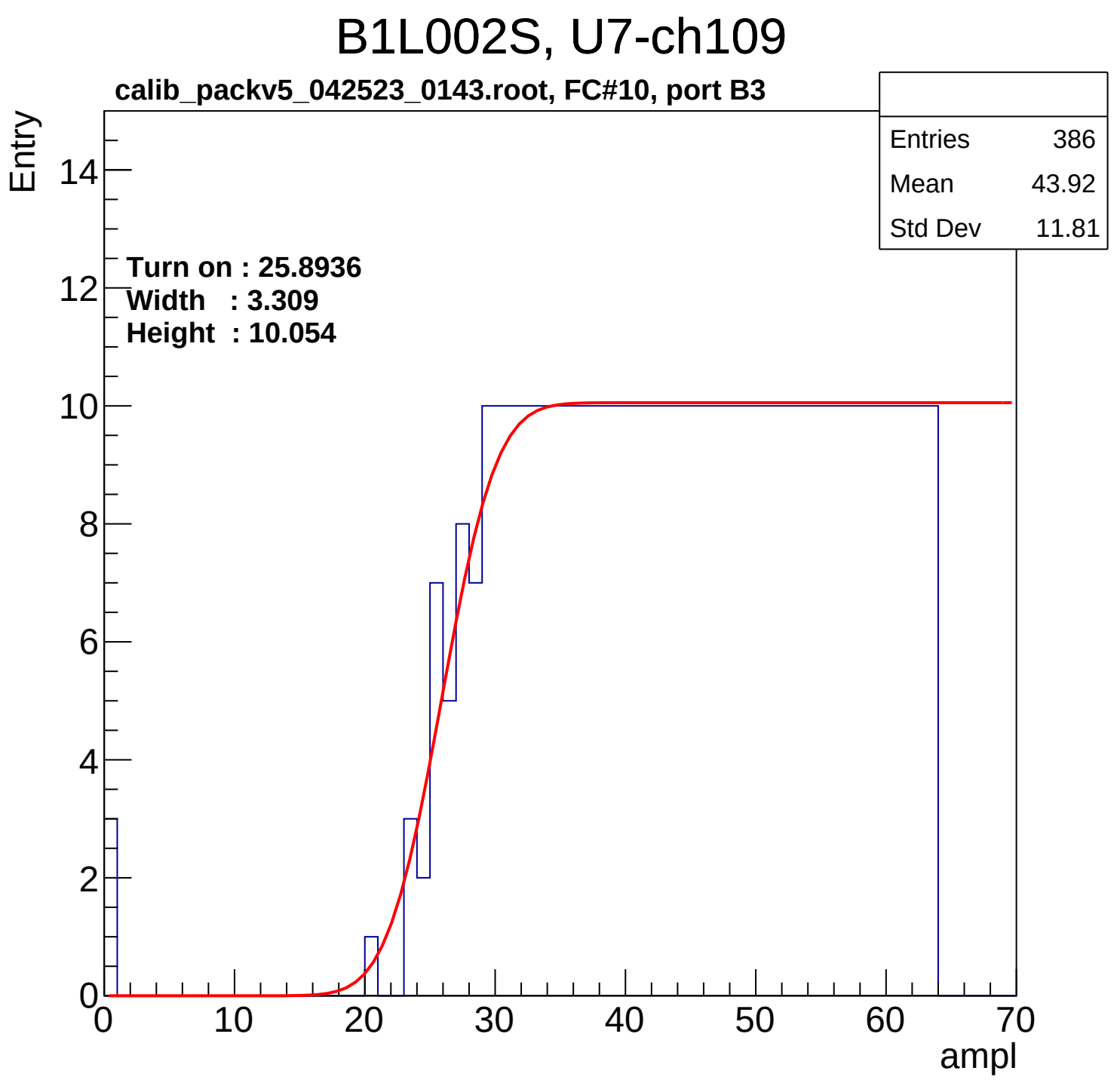
B1L002S, U7-ch109
calib_packv5_042523_0143.root, FC#10, port B3
Entries 386
Mean 43.92
Std Dev 11.81
Turn on : 25.8936
Width : 3.309
Height : 10.054
Entry
ampl
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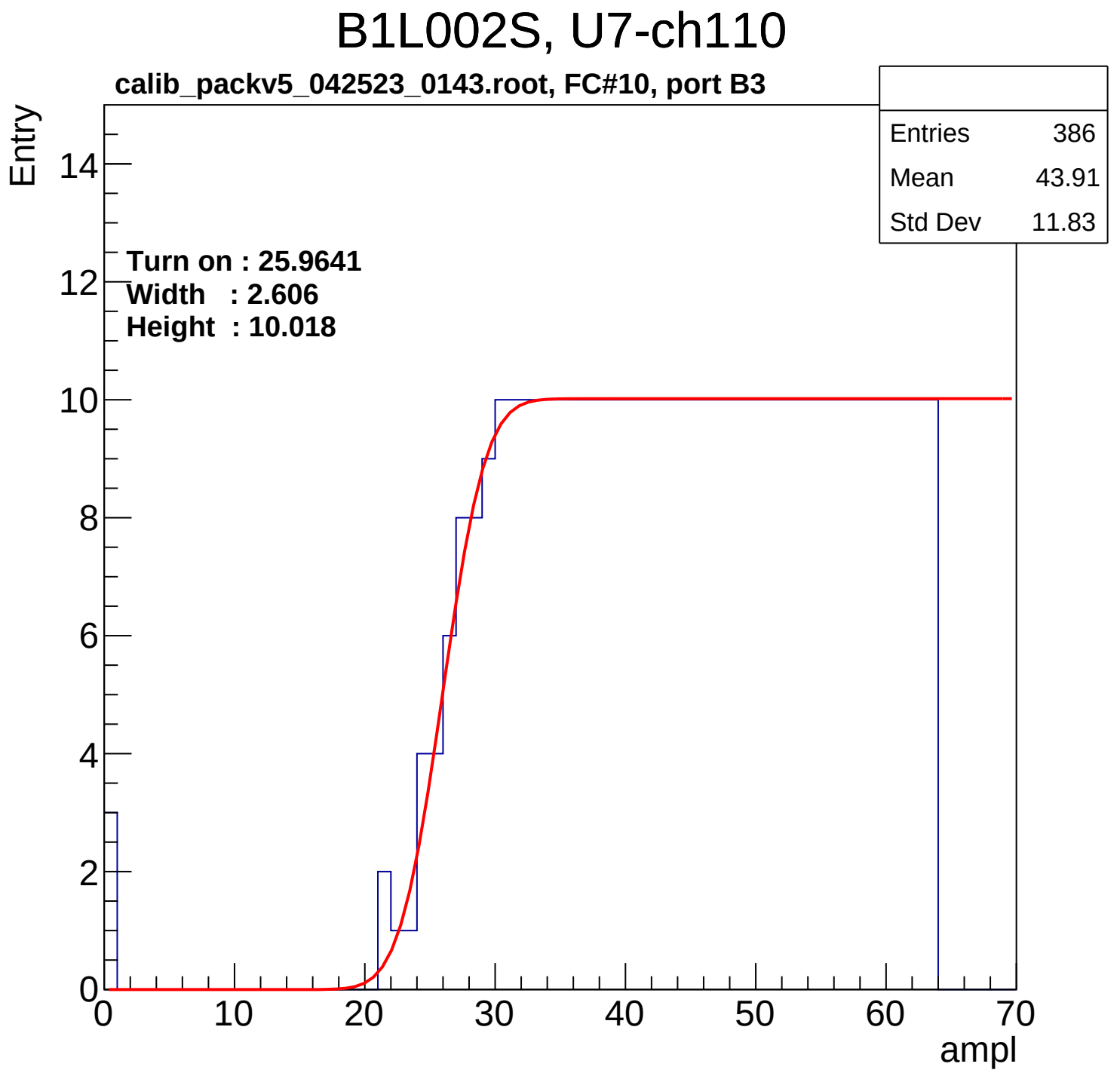
B1L002S, U7-ch110
calib_packv5_042523_0143.root, FC#10, port B3
Entries 386
Mean 43.91
Std Dev 11.83
Turn on : 25.9641
Width : 2.606
Height : 10.018
Entry
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8
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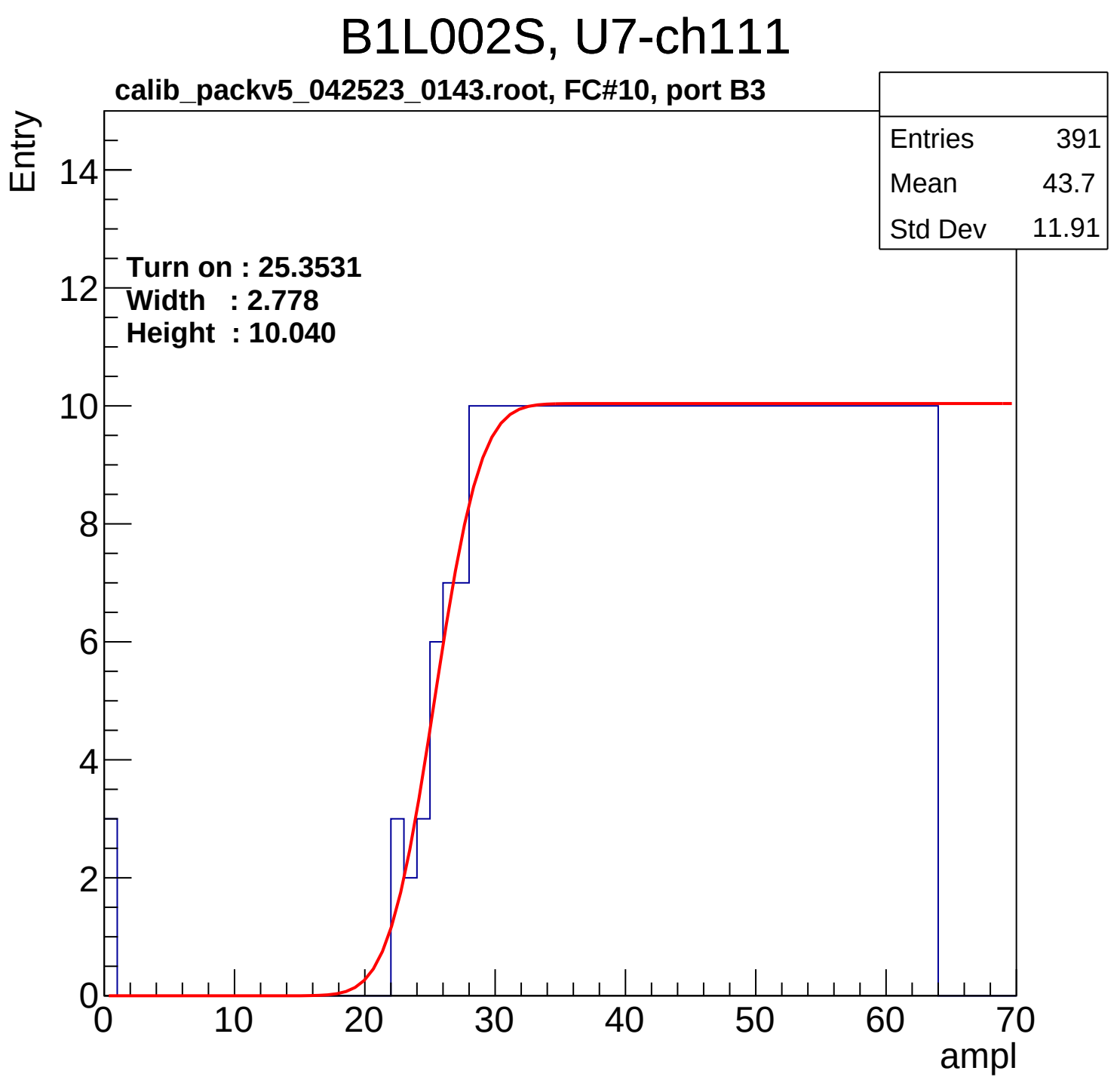
B1L002S, U7-ch111
calib_packv5_042523_0143.root, FC#10, port B3
Entries 391
Mean 43.7
Std Dev 11.91
Turn on : 25.3531
Width : 2.778
Height : 10.040
Entry
ampl
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6
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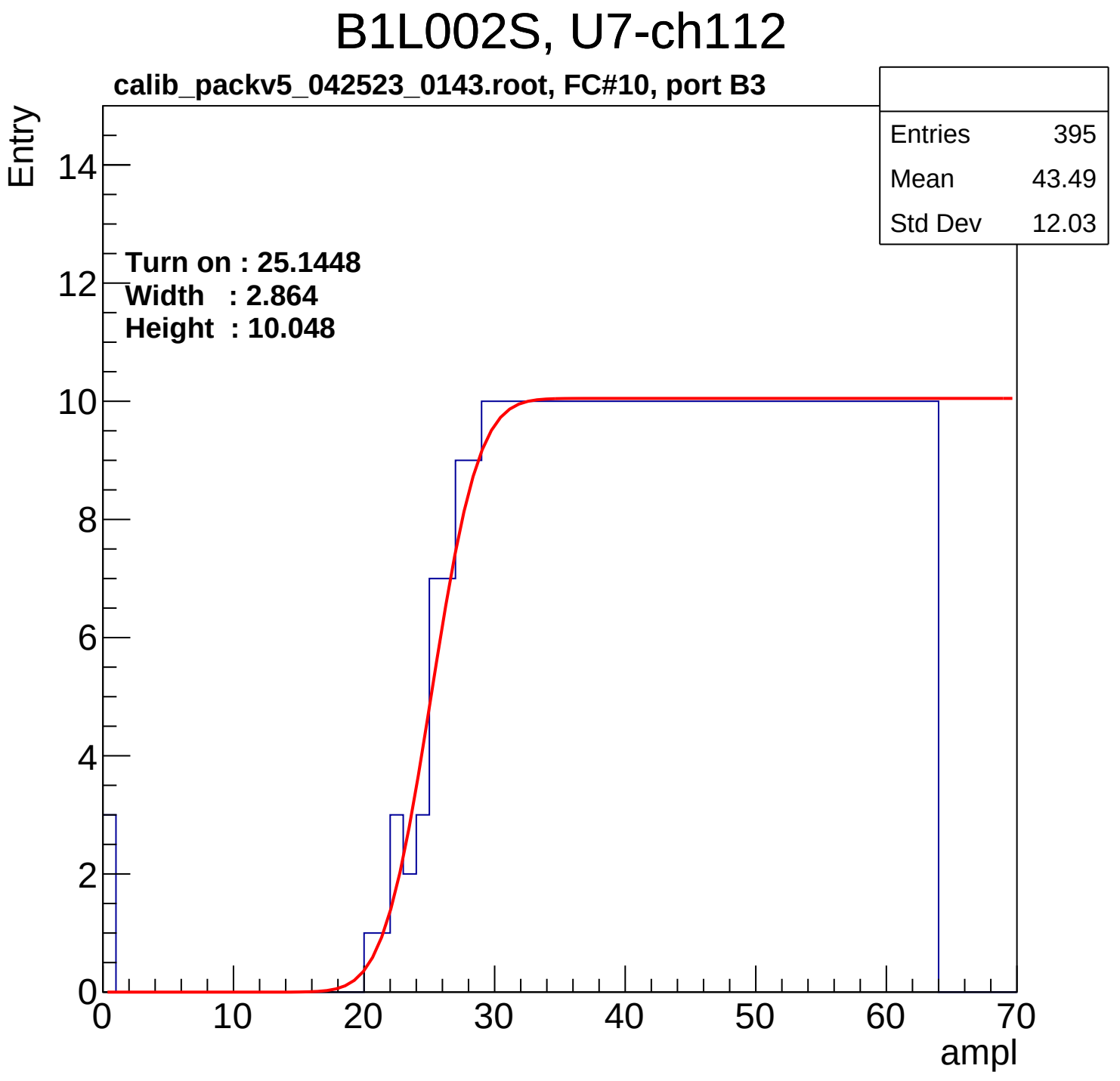
B1L002S, U7-ch112
calib_packv5_042523_0143.root, FC#10, port B3
Entries 395
Mean 43.49
Std Dev 12.03
Turn on : 25.1448
Width : 2.864
Height : 10.048
Entry
ampl
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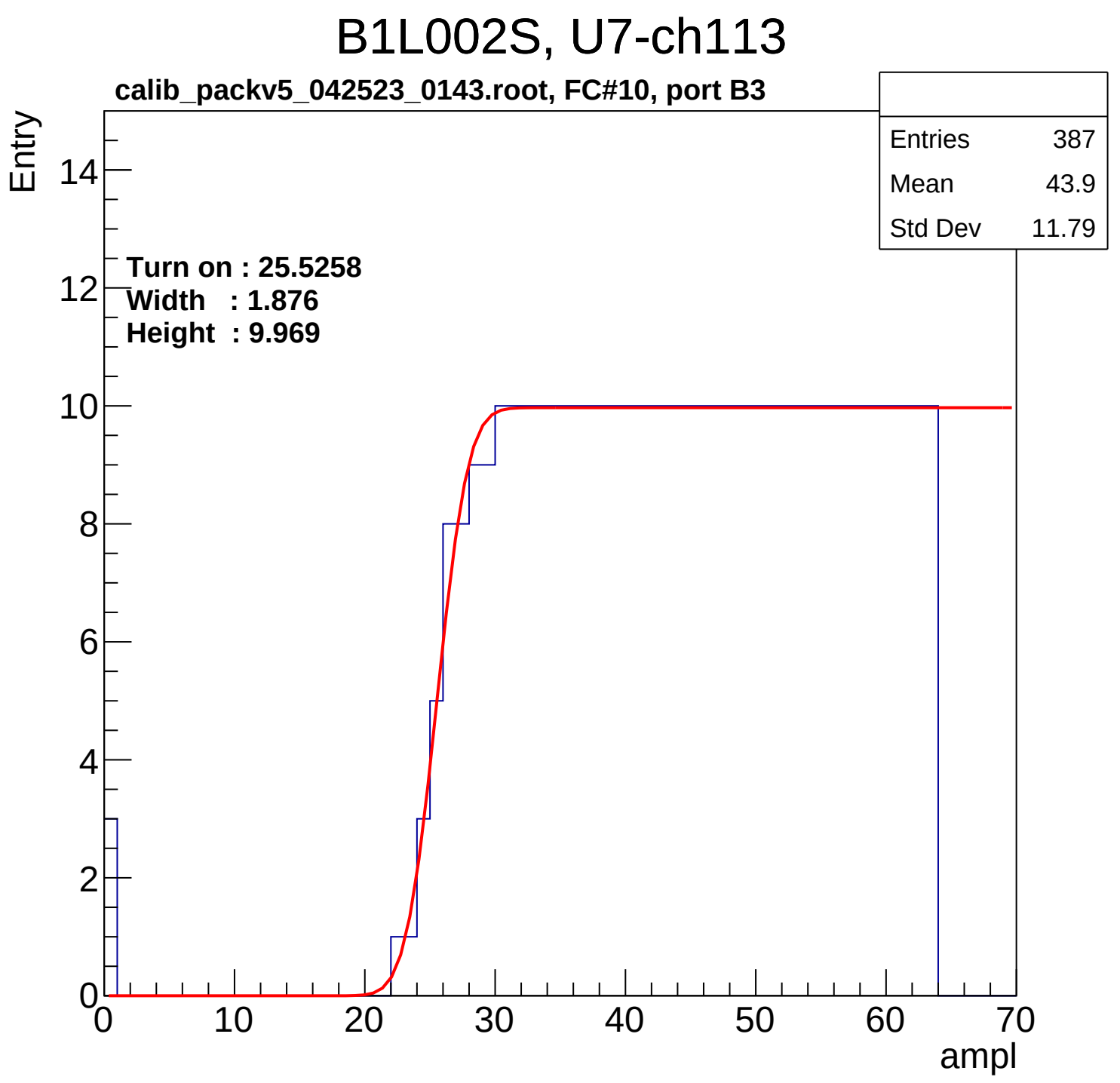
B1L002S, U7-ch113
calib_packv5_042523_0143.root, FC#10, port B3
Entries 387
Mean 43.9
Std Dev 11.79
Turn on : 25.5258
Width : 1.876
Height : 9.969
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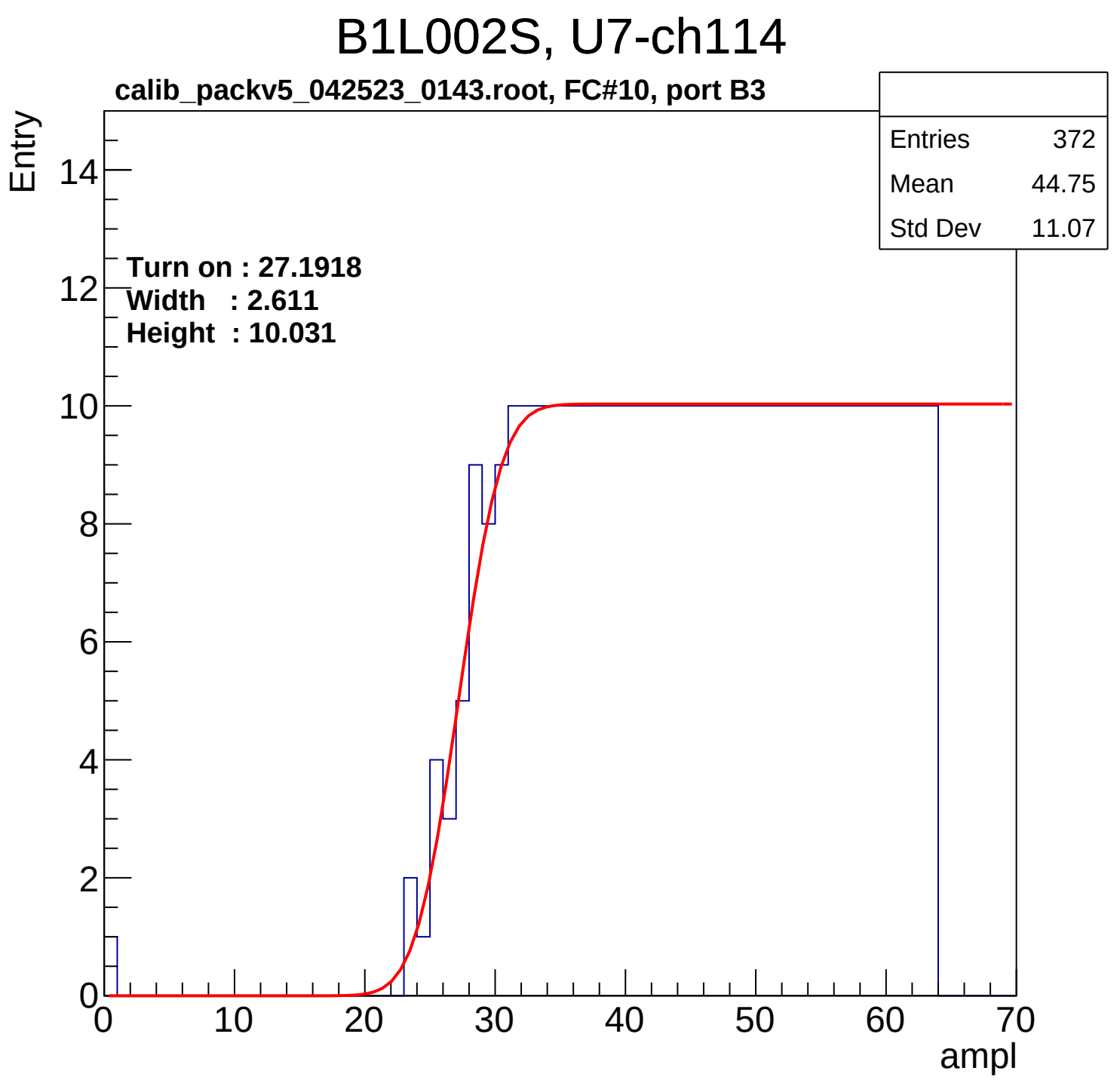
B1L002S, U7-ch114
calib_packv5_042523_0143.root, FC#10, port B3
Entries 372
Mean 44.75
Std Dev 11.07
Turn on : 27.1918
Width : 2.611
Height : 10.031
Entry
ampl
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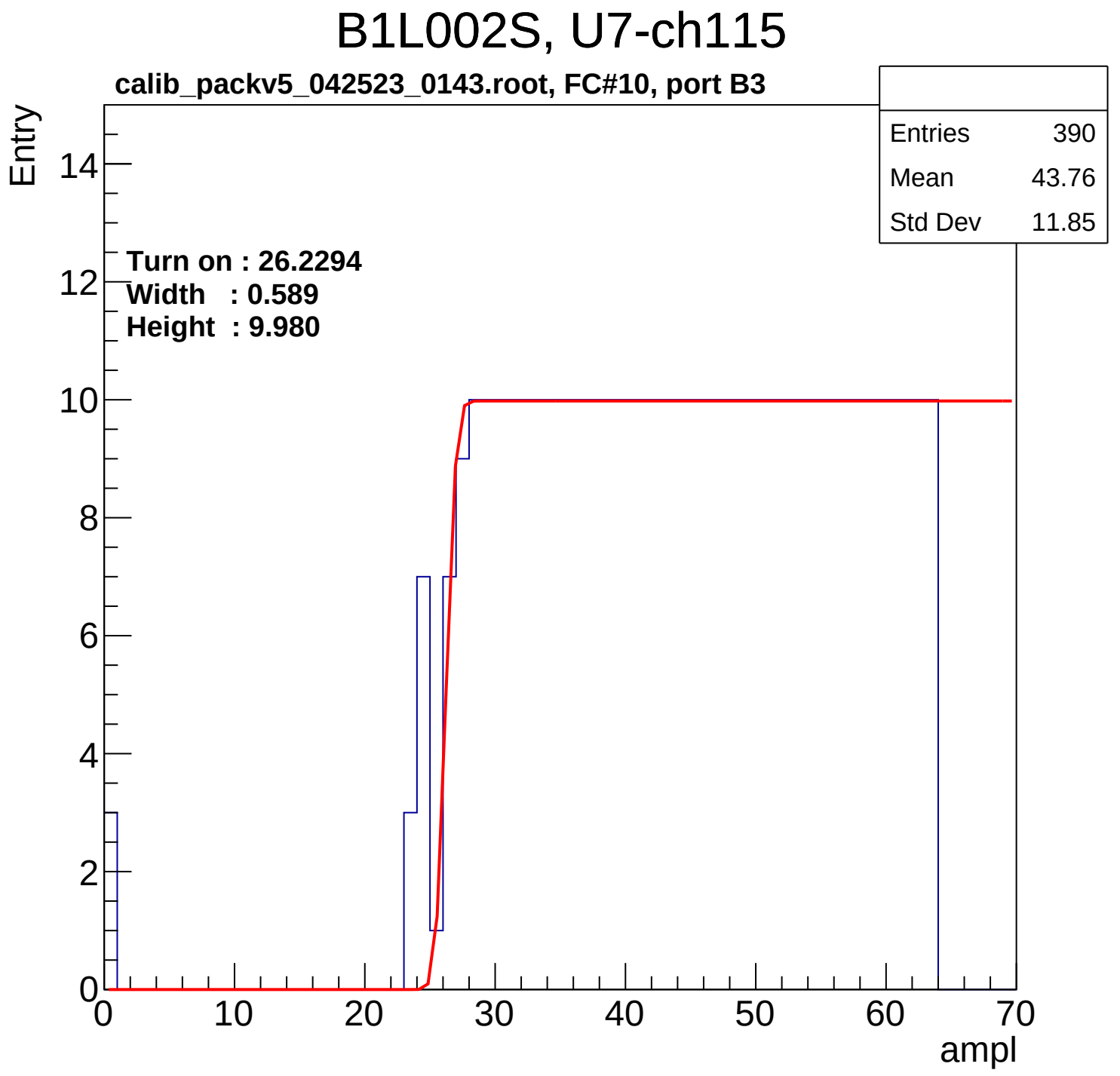
B1L002S, U7-ch115
calib_packv5_042523_0143.root, FC#10, port B3
Entries 390
Mean 43.76
Std Dev 11.85
Turn on : 26.2294
Width : 0.589
Height : 9.980
Entry
ampl
0
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4
6
8
10
12
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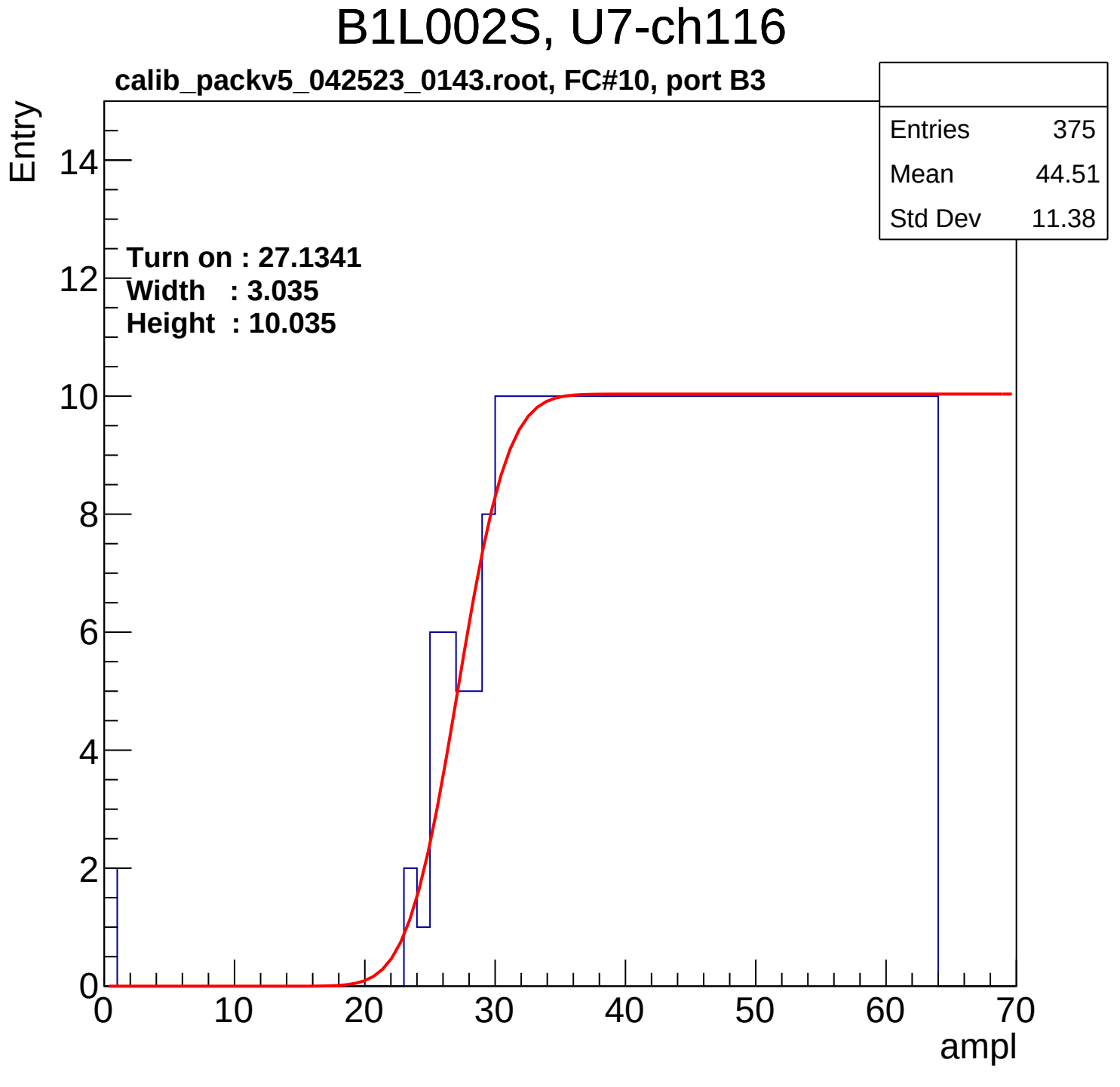
B1L002S, U7-ch116
calib_packv5_042523_0143.root, FC#10, port B3
Entries 375
Mean 44.51
Std Dev 11.38
Turn on : 27.1341
Width : 3.035
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
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0
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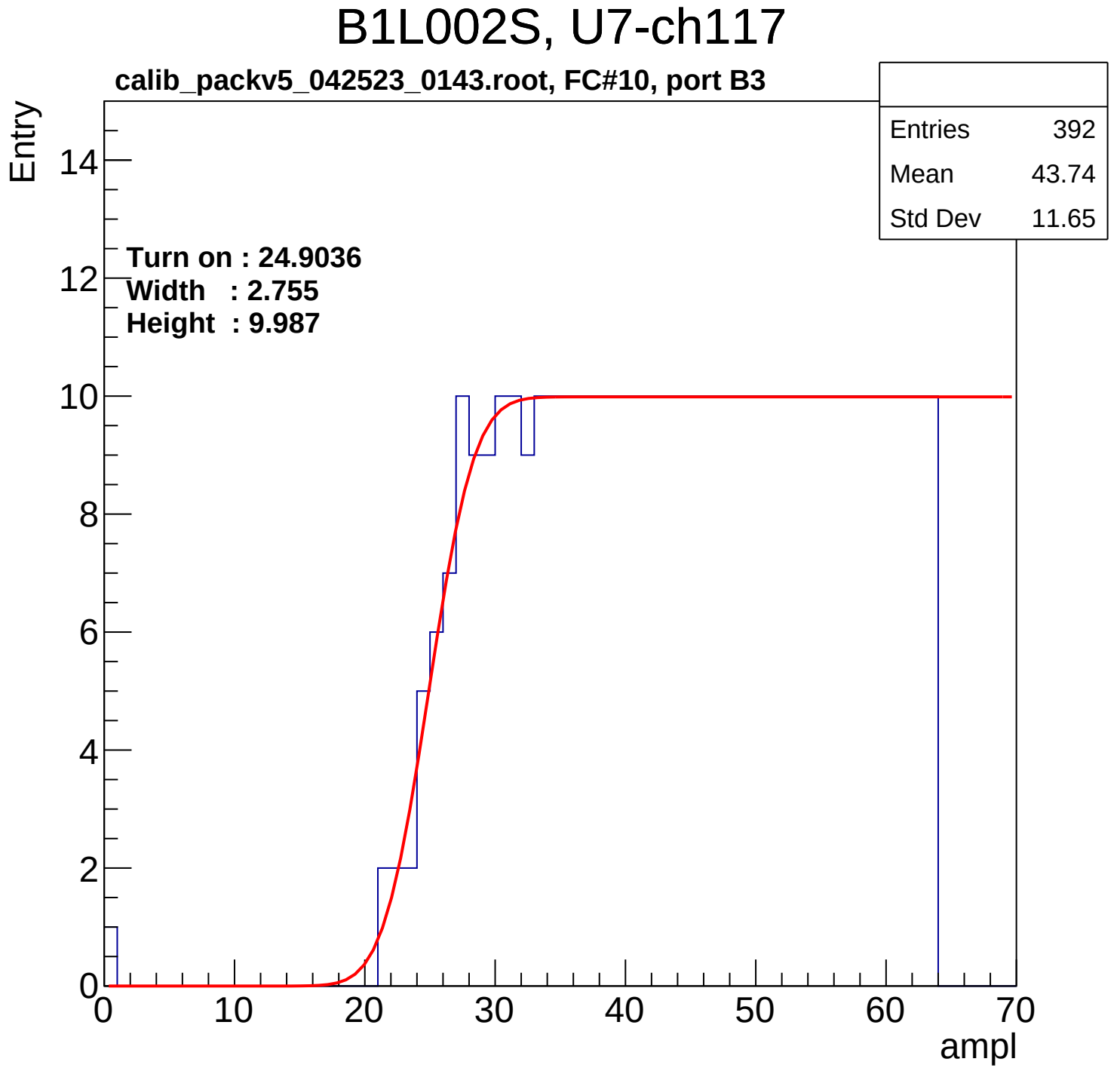
B1L002S, U7-ch117
calib_packv5_042523_0143.root, FC#10, port B3
Entries 392
Mean 43.74
Std Dev 11.65
Turn on : 24.9036
Width : 2.755
Height : 9.987
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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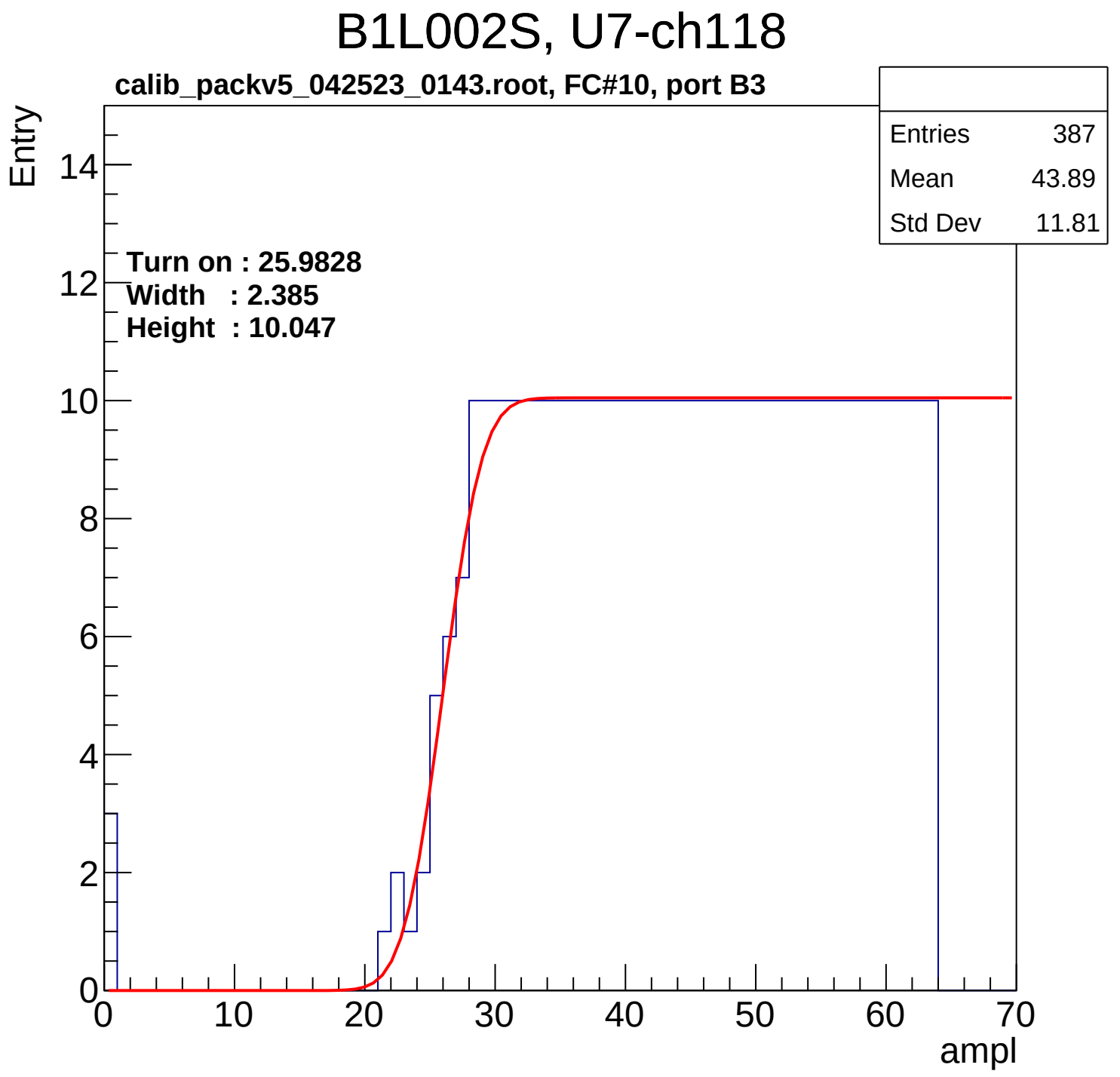
B1L002S, U7-ch118
calib_packv5_042523_0143.root, FC#10, port B3
Entries 387
Mean 43.89
Std Dev 11.81
Turn on : 25.9828
Width : 2.385
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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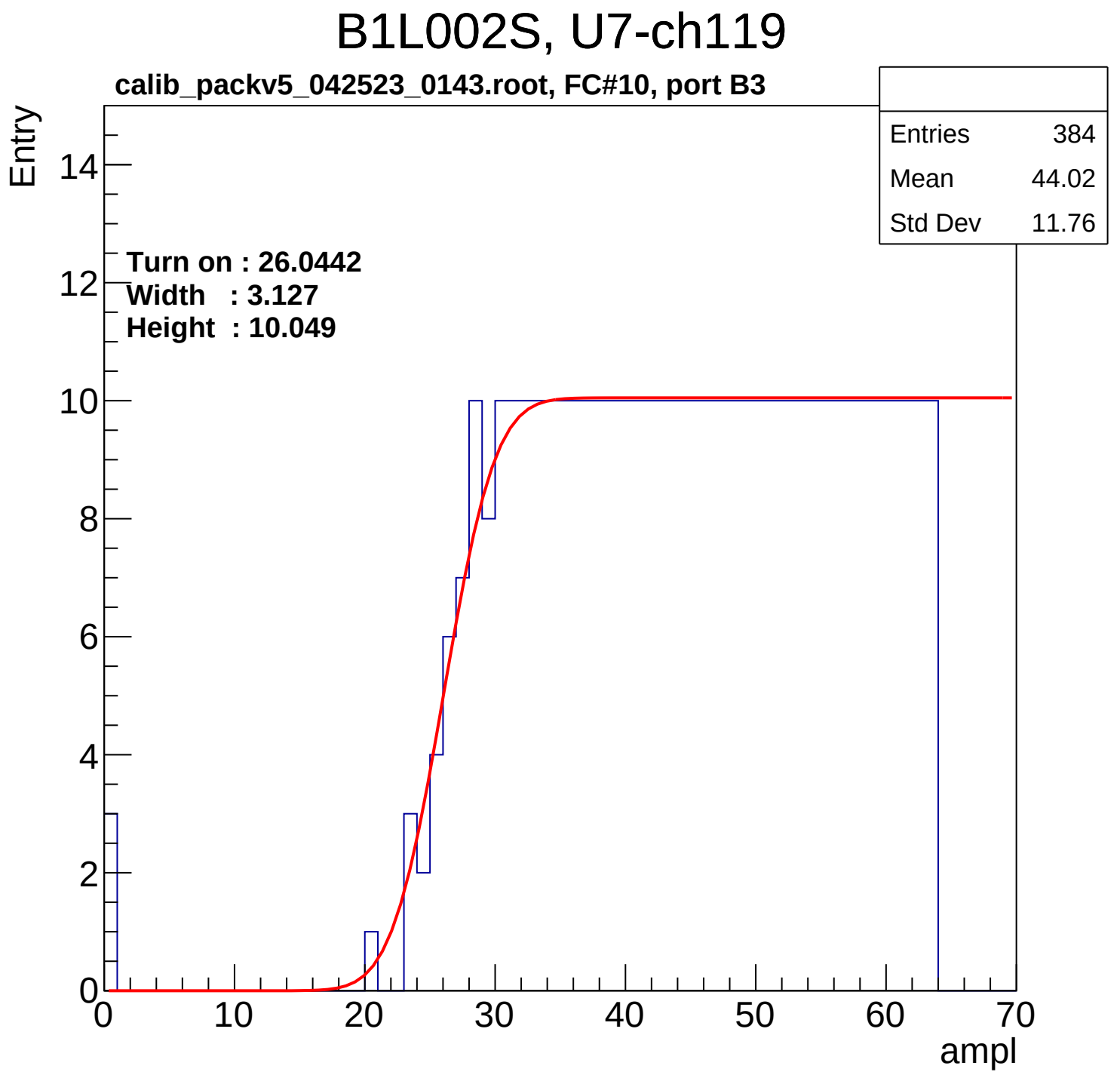
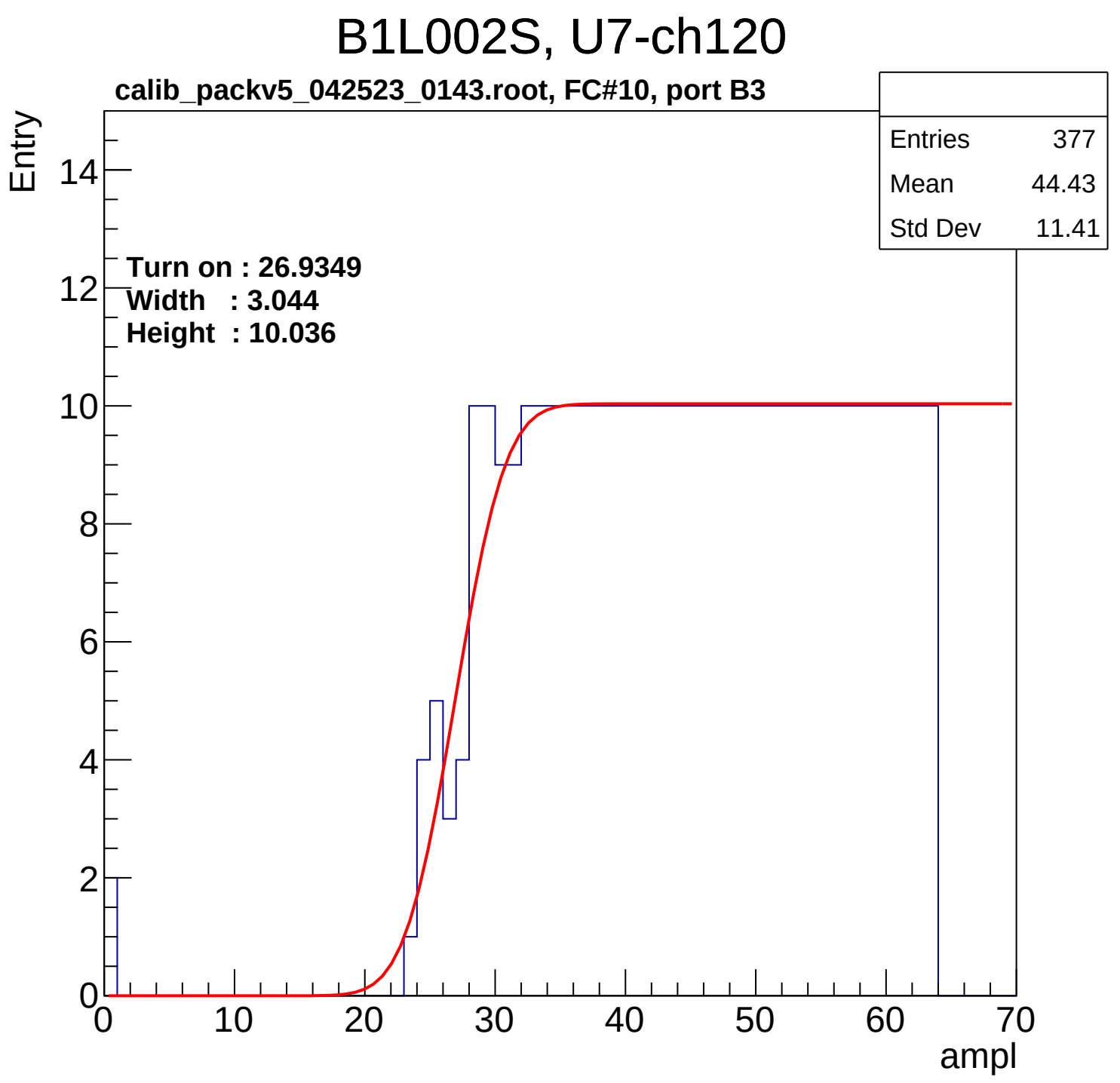

B1L002S, U7-ch119
calib_packv5_042523_0143.root, FC#10, port B3
Entries 384
Mean 44.02
Std Dev 11.76
Turn on : 26.0442
Width : 3.127
Height : 10.049
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L002S, U7-ch120
calib_packv5_042523_0143.root, FC#10, port B3
Entries 377
Mean 44.43
Std Dev 11.41
Turn on : 26.9349
Width : 3.044
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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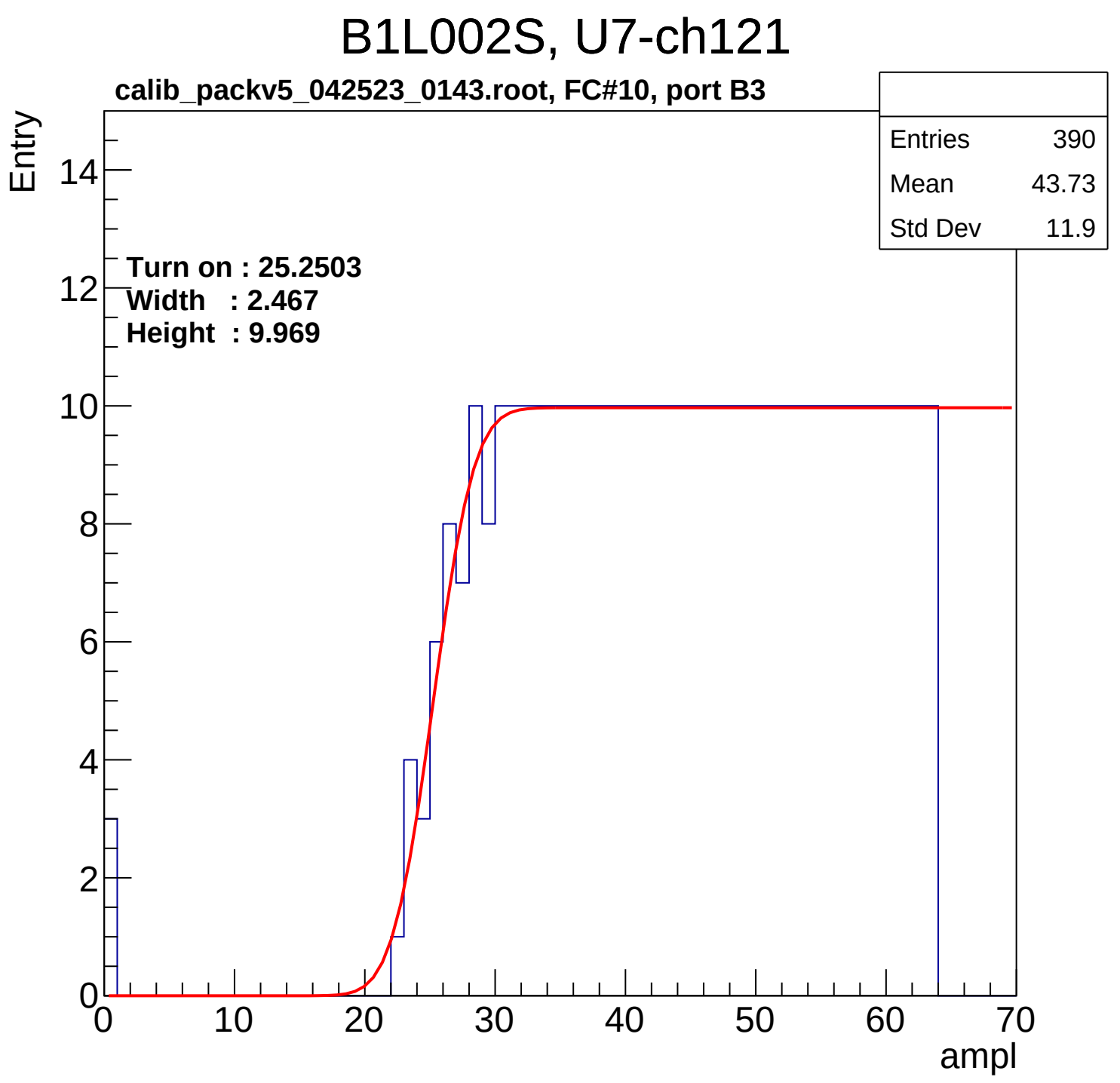
B1L002S, U7-ch121
calib_packv5_042523_0143.root, FC#10, port B3
Entries 390
Mean 43.73
Std Dev 11.9
Turn on : 25.2503
Width : 2.467
Height : 9.969
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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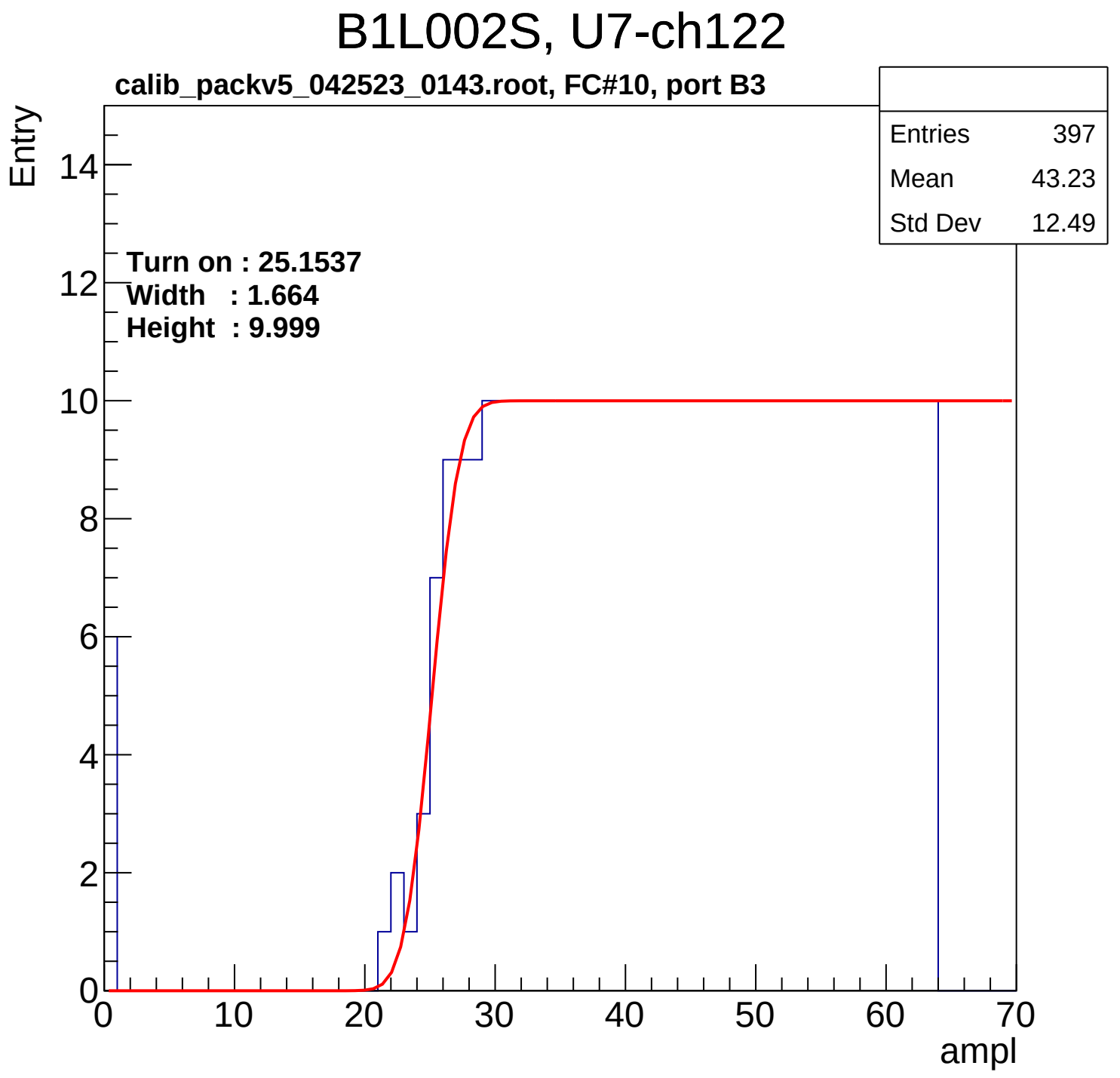
B1L002S, U7-ch122
calib_packv5_042523_0143.root, FC#10, port B3
Entries 397
Mean 43.23
Std Dev 12.49
Turn on : 25.1537
Width : 1.664
Height : 9.999
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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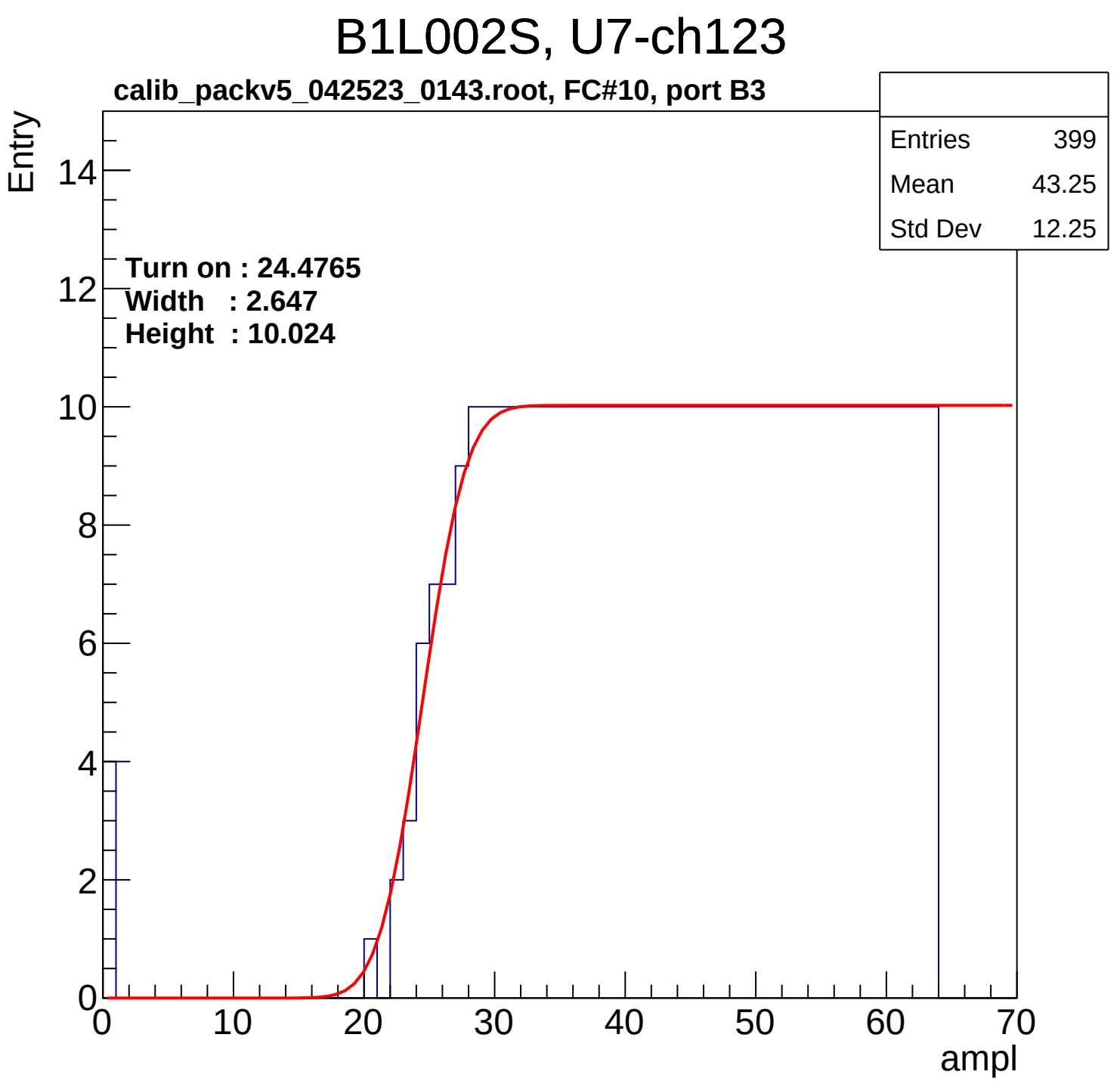
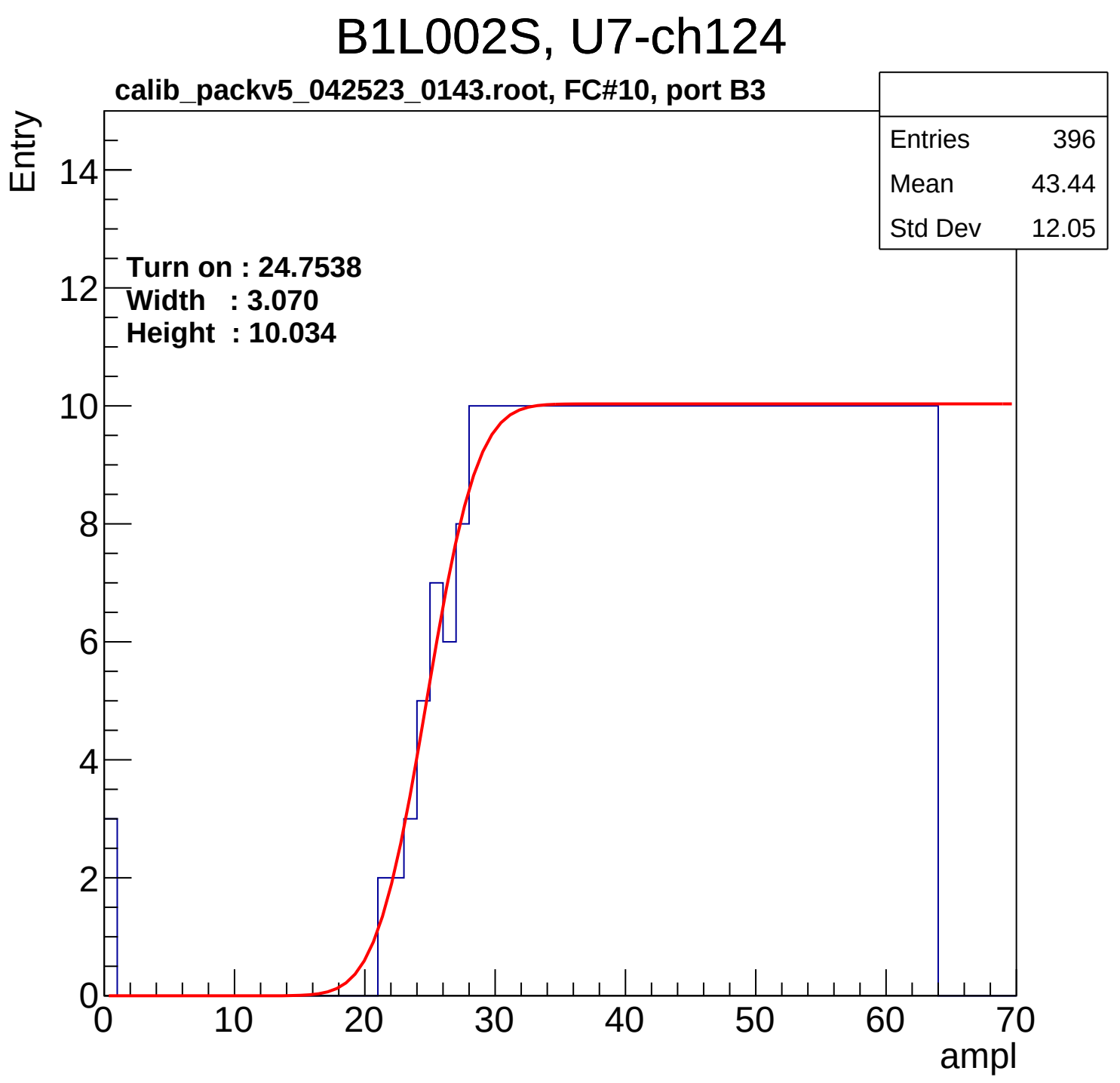

B1L002S, U7-ch123
calib_packv5_042523_0143.root, FC#10, port B3
Entries 399
Mean 43.25
Std Dev 12.25
Turn on : 24.4765
Width : 2.647
Height : 10.024
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L002S, U7-ch124
calib_packv5_042523_0143.root, FC#10, port B3
Entries 396
Mean 43.44
Std Dev 12.05
Turn on : 24.7538
Width : 3.070
Height : 10.034
Entry
ampl
0
2
4
6
8
10
12
14
0
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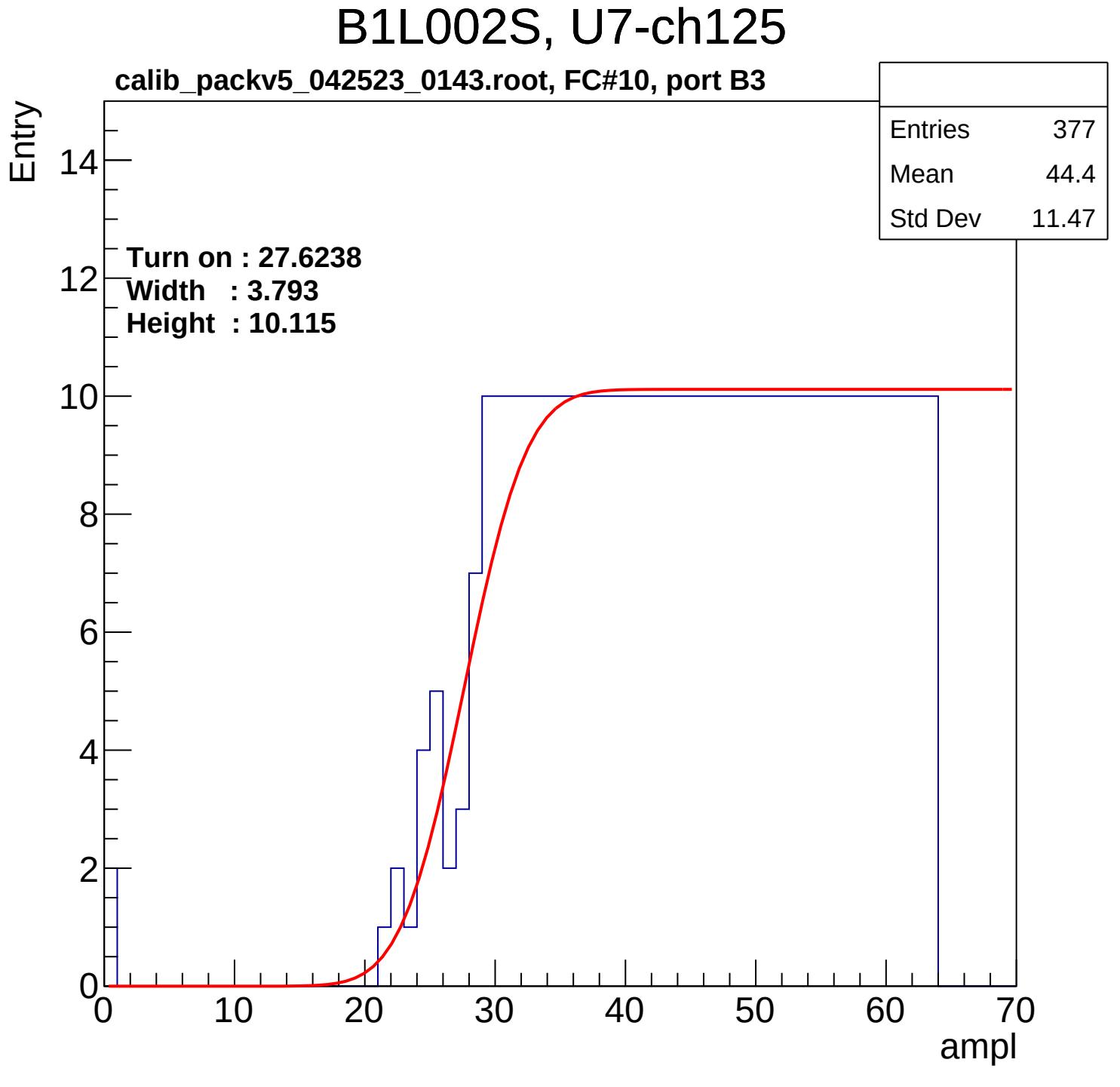
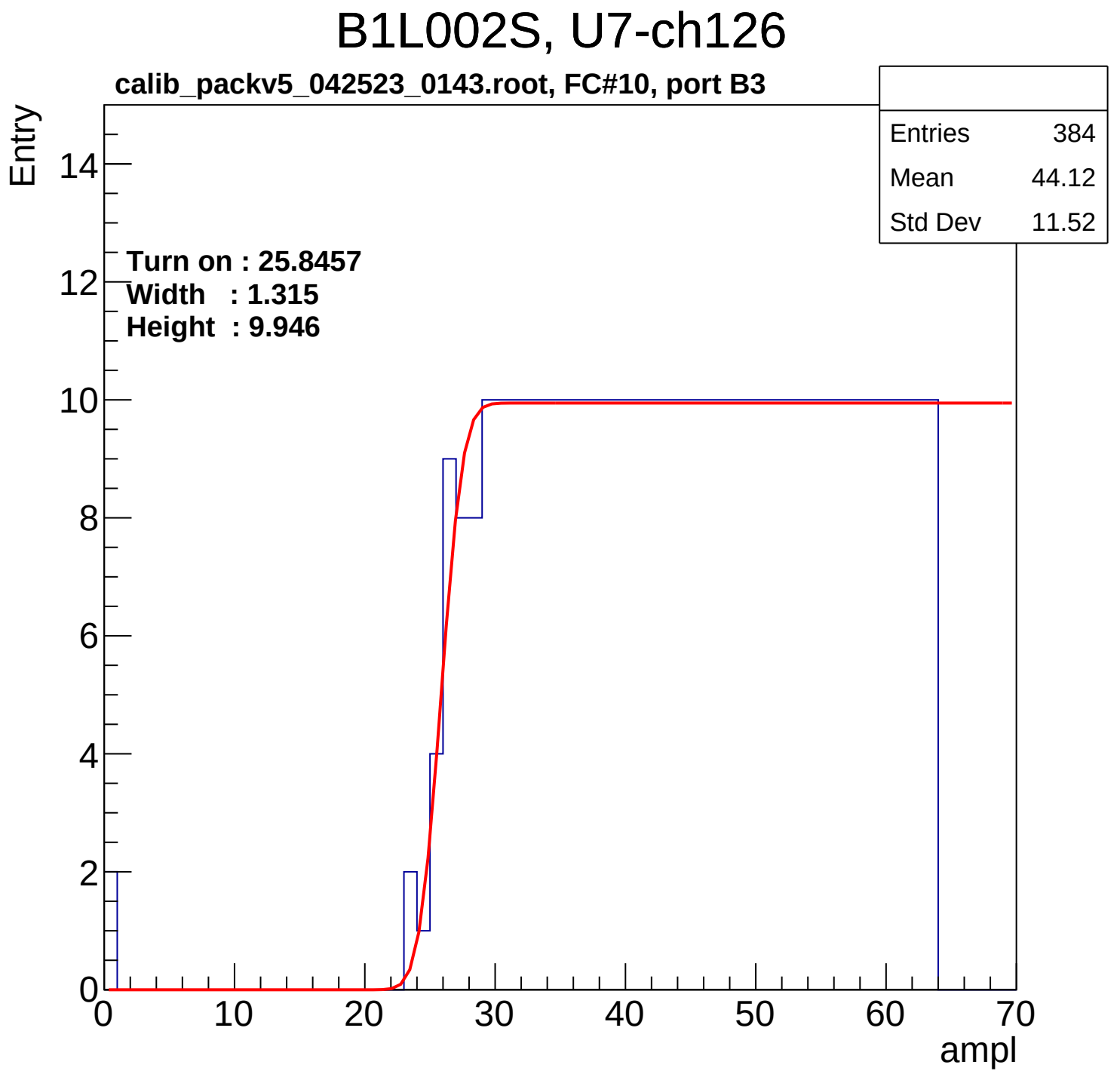
20
30
40
50
60
70


B1L002S, U7-ch125
calib_packv5_042523_0143.root, FC#10, port B3
Entries 377
Mean 44.4
Std Dev 11.47
Turn on : 27.6238
Width : 3.793
Height : 10.115
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L002S, U7-ch126
calib_packv5_042523_0143.root, FC#10, port B3
Entries 384
Mean 44.12
Std Dev 11.52
Turn on : 25.8457
Width : 1.315
Height : 9.946
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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60
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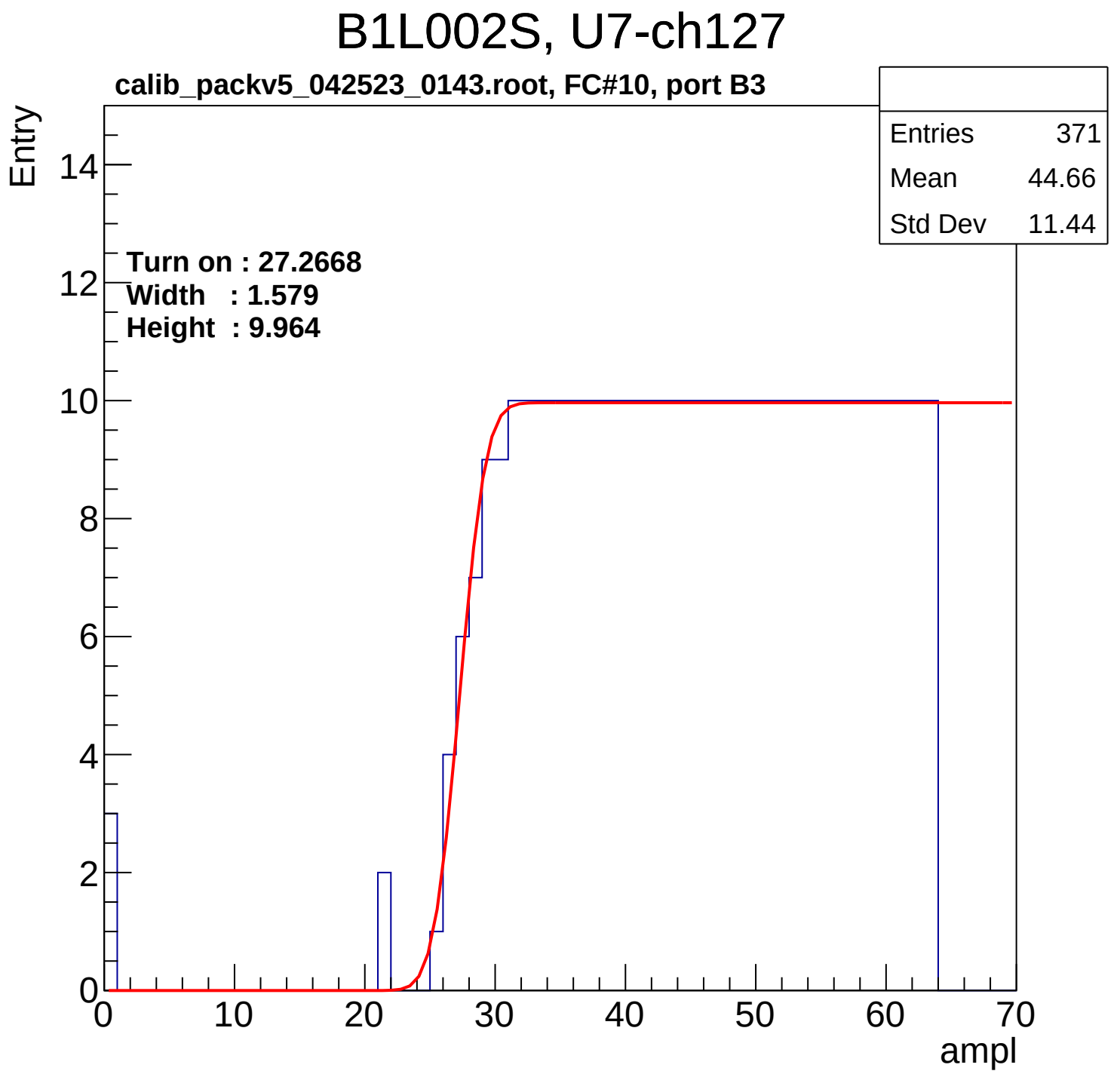
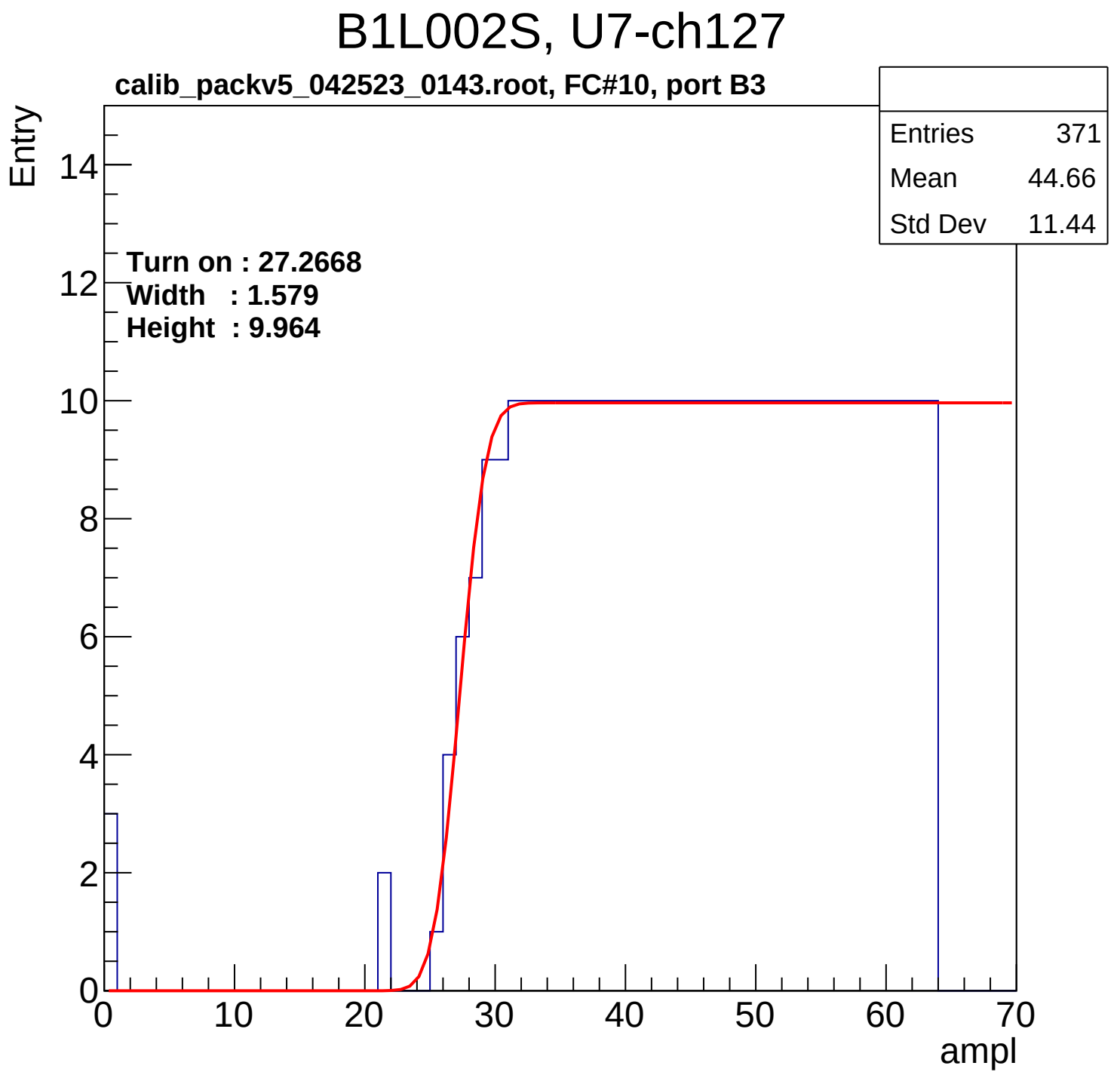

B1L002S, U7-ch127
calib_packv5_042523_0143.root, FC#10, port B3
Entries 371
Mean 44.66
Std Dev 11.44
Turn on : 27.2668
Width : 1.579
Height : 9.964
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L002S, U7-ch127
calib_packv5_042523_0143.root, FC#10, port B3
Entries 371
Mean 44.66
Std Dev 11.44
Turn on : 27.2668
Width : 1.579
Height : 9.964
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70