

B0L100S, U12-ch0, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch0, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch0, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

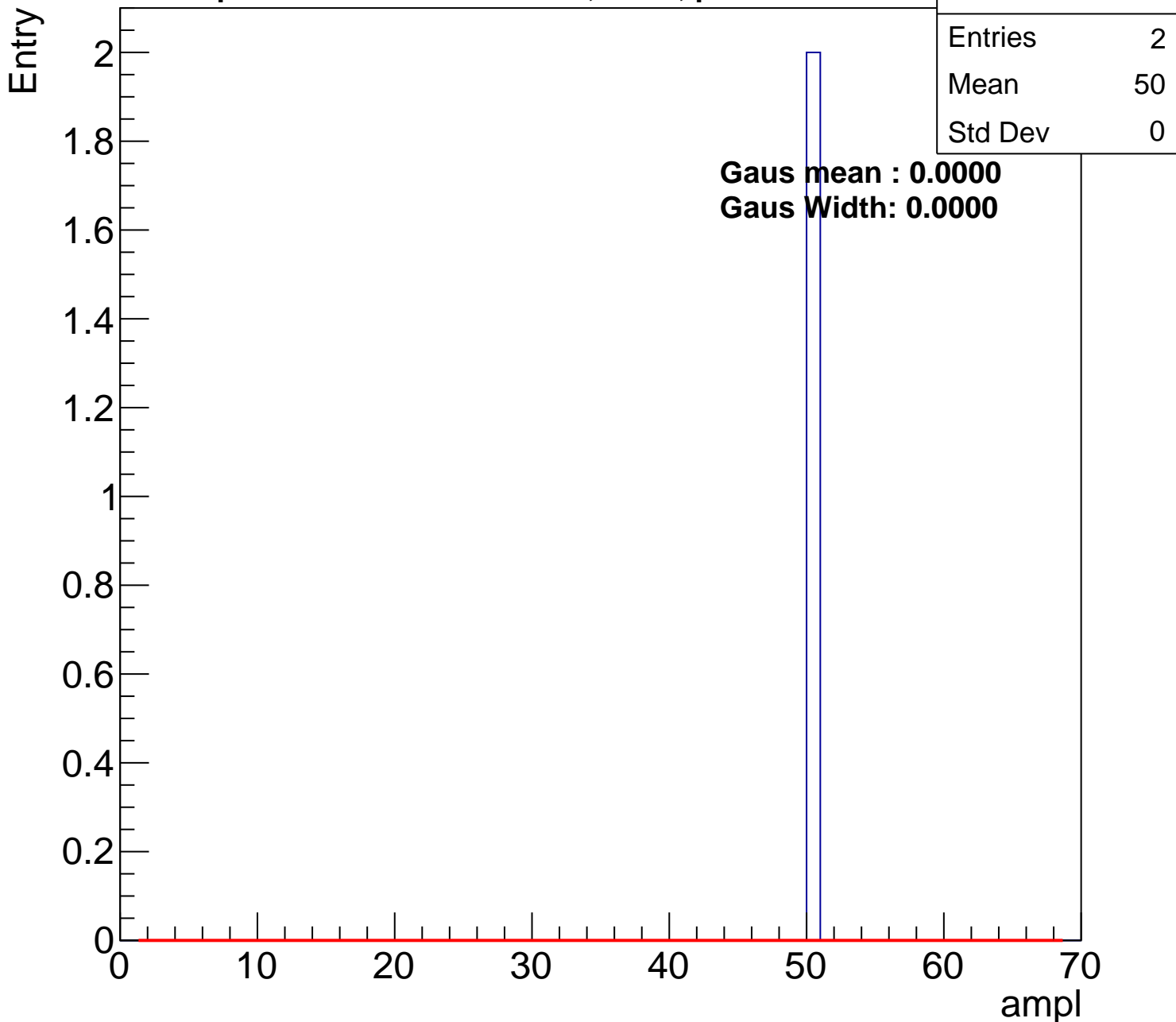
Entries	2
Mean	50
Std Dev	0

Gaus mean : 0.0000

Gaus Width: 0.0000

0 10 20 30 40 50 60 70

ampl



B0L100S, U12-ch0, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	2
Mean	50
Std Dev	0

0 10 20 30 40 50 60 70

ampl

ampl

B0L100S, U12-ch0, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch0, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch0, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch0, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch1, adc0

calib_packv5_042523_0143.root, FC#6, port A1

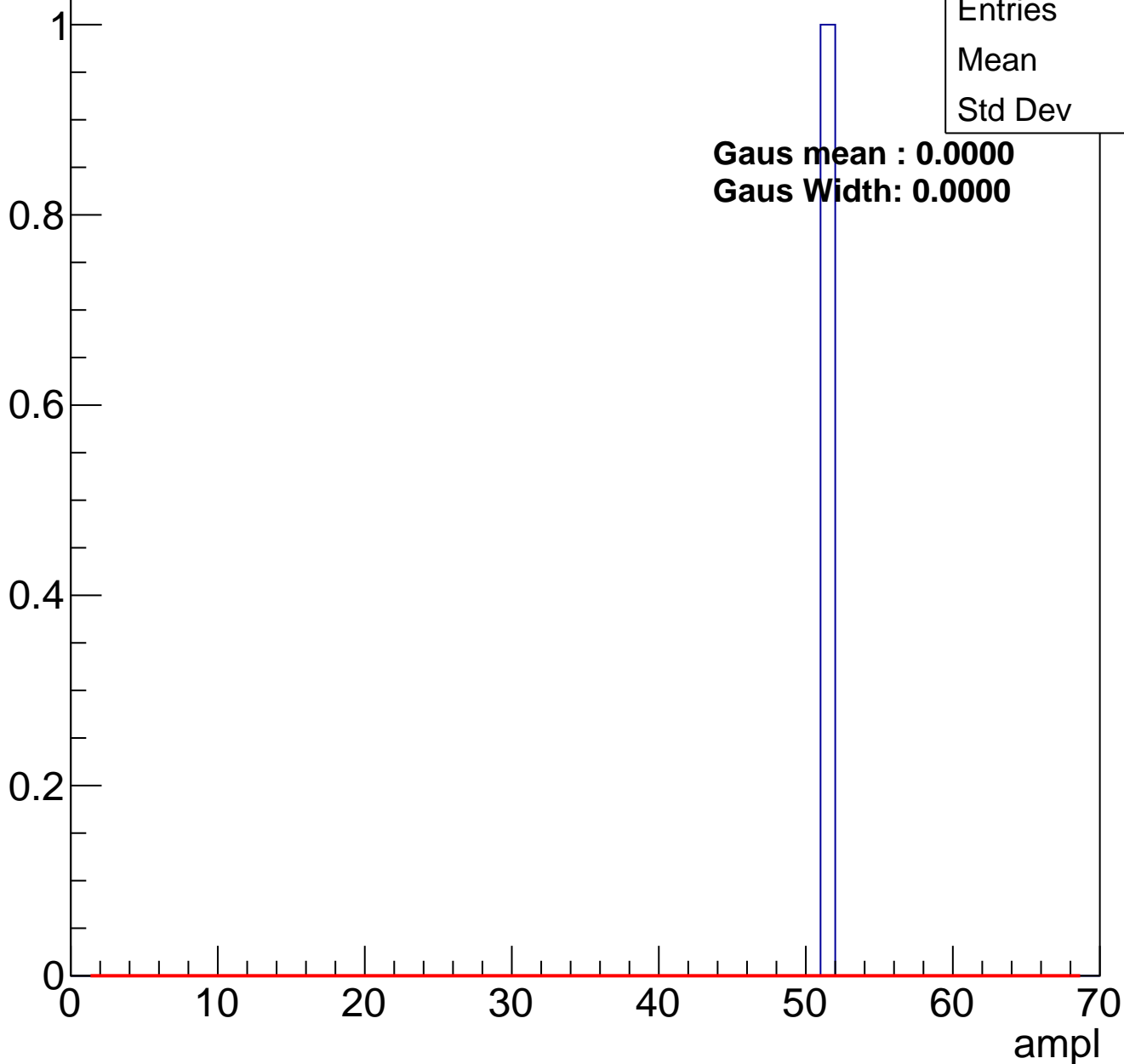
Entry



B0L100S, U12-ch1, adc1

calib_packv5_042523_0143.root, FC#6, port A1

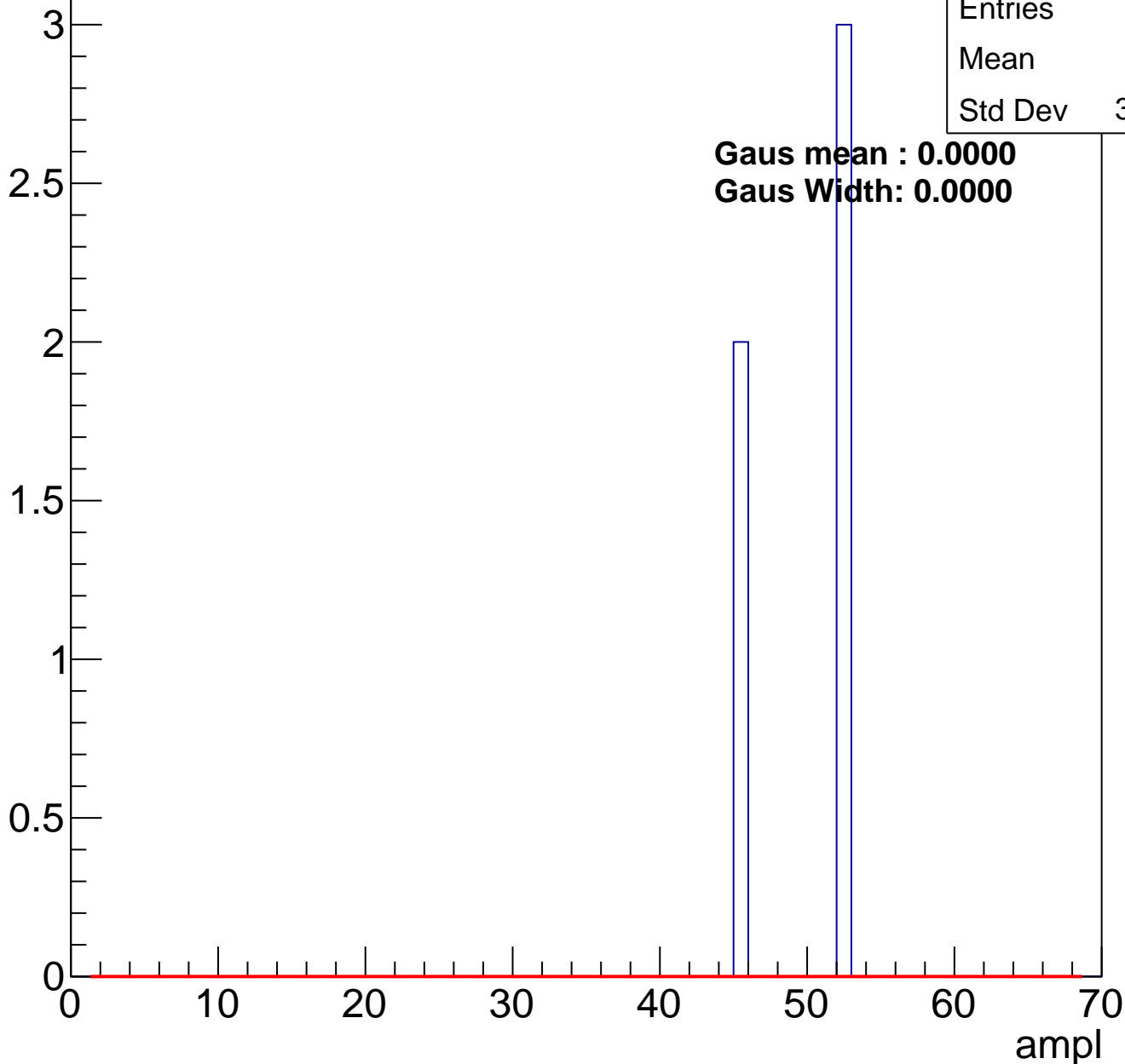
Entry



B0L100S, U12-ch1, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	5
Mean	49.2
Std Dev	3.429

B0L100S, U12-ch1, adc3

calib_packv5_042523_0143.root, FC#6, port A1

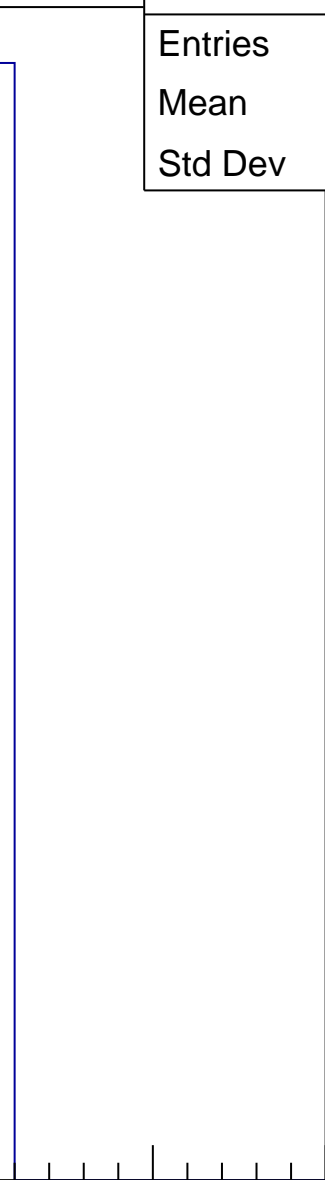
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	2
Mean	51
Std Dev	0

0 10 20 30 40 50 60 70

ampl



B0L100S, U12-ch1, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch1, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch1, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch1, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry

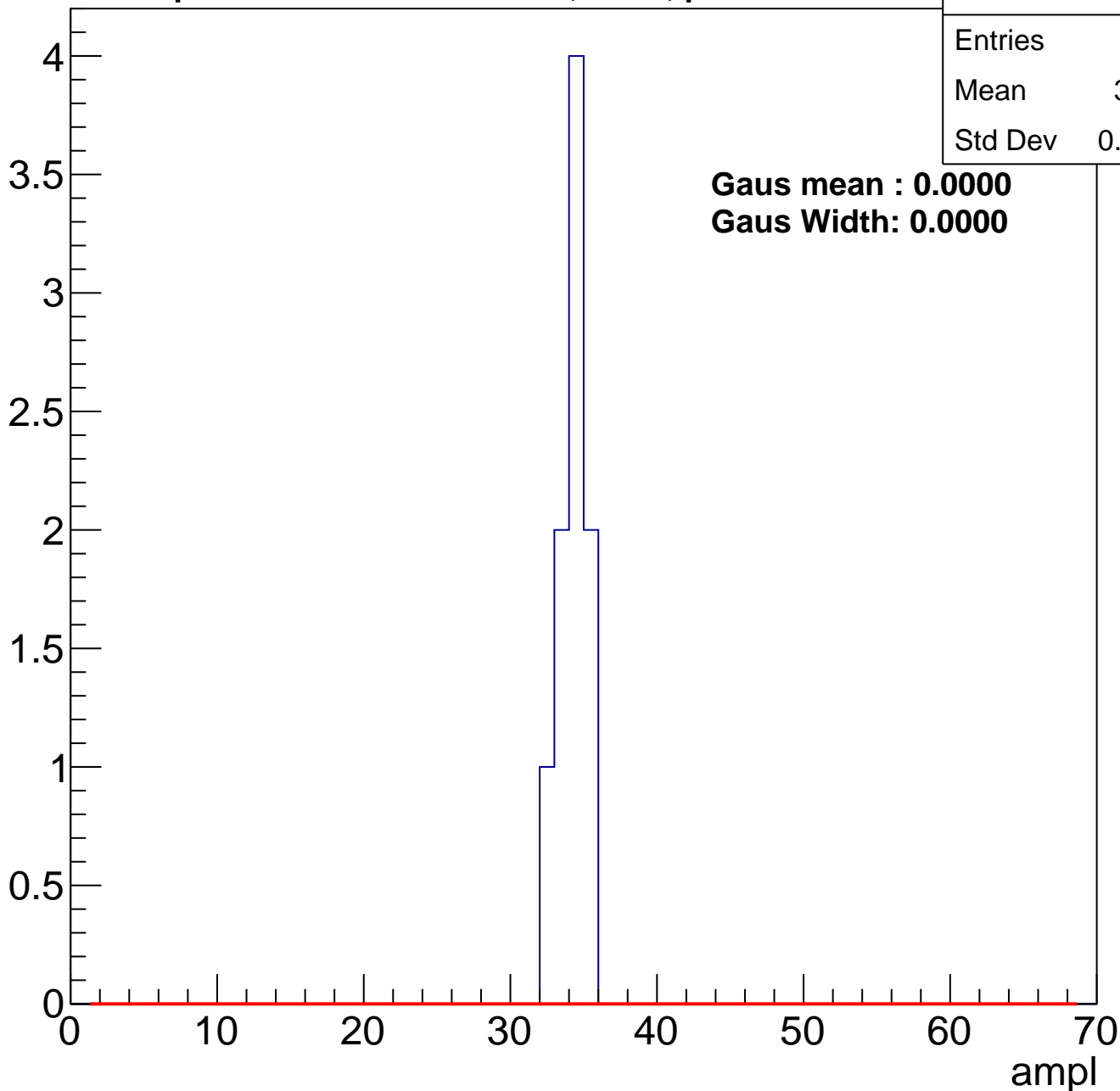


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch2, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	9
Mean	33.78
Std Dev	0.9162

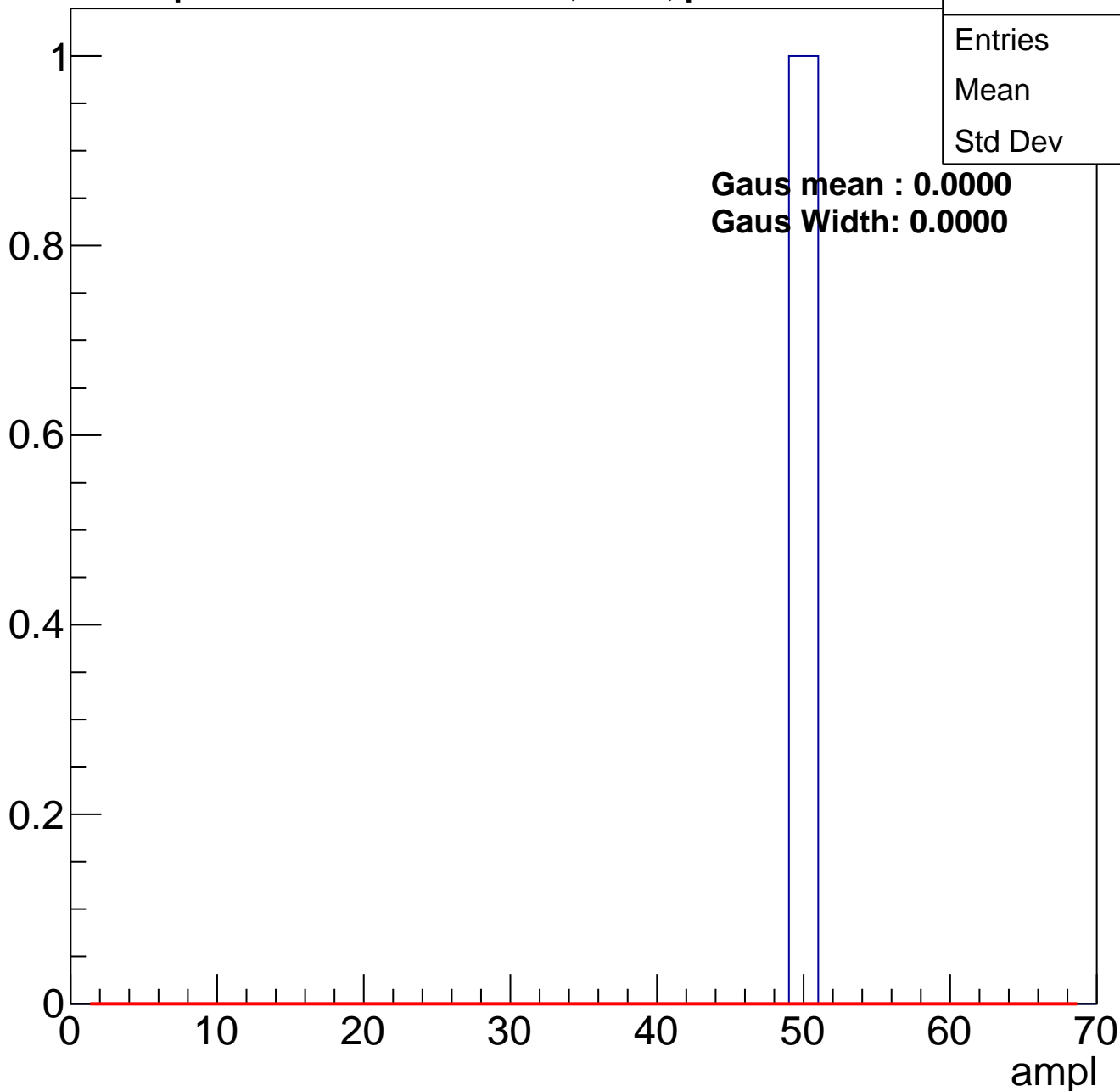
Gaus mean : 0.0000

Gaus Width: 0.0000

B0L100S, U12-ch2, adc1

calib_packv5_042523_0143.root, FC#6, port A1

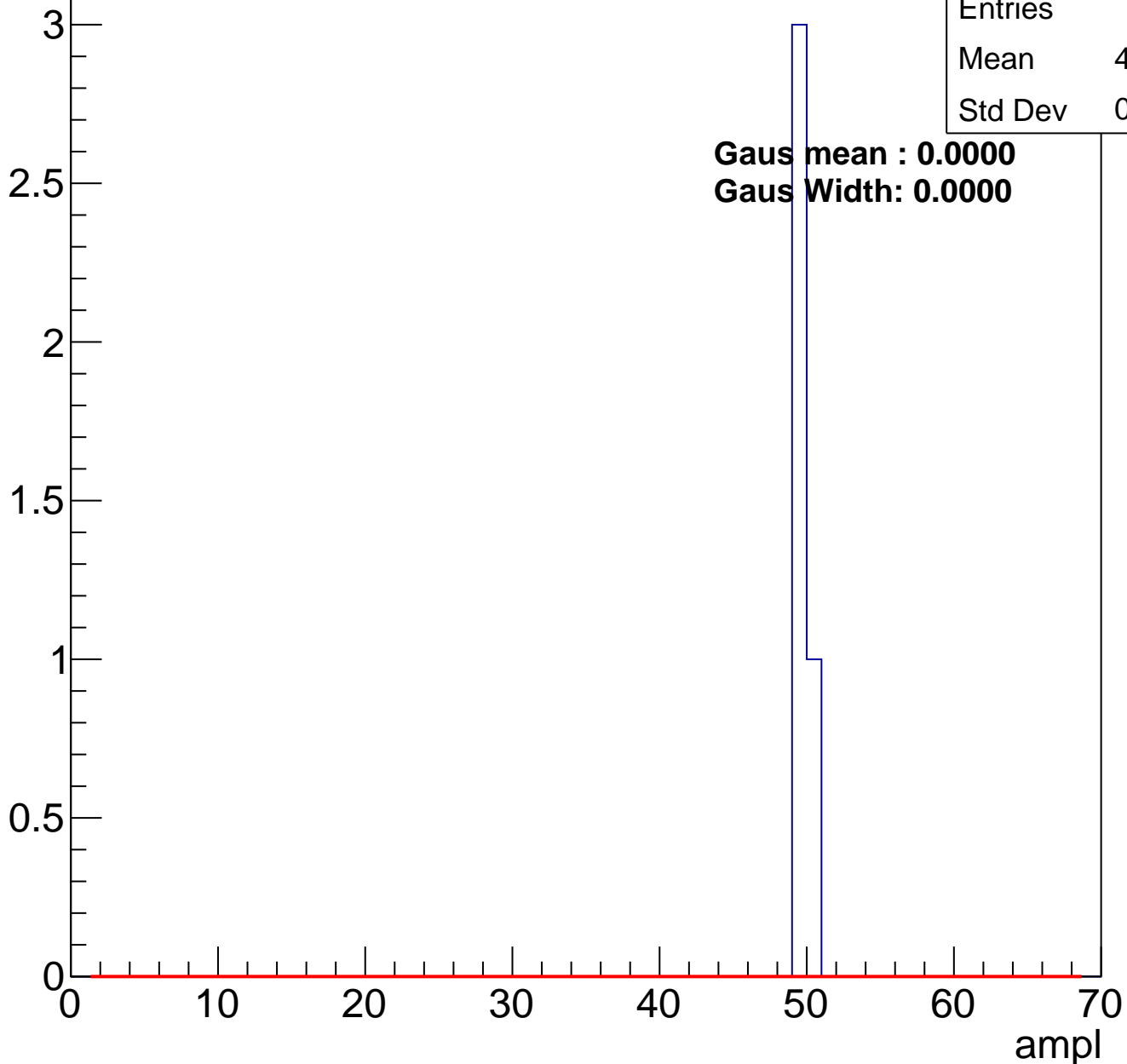
Entry



B0L100S, U12-ch2, adc2

calib_packv5_042523_0143.root, FC#6, port A1

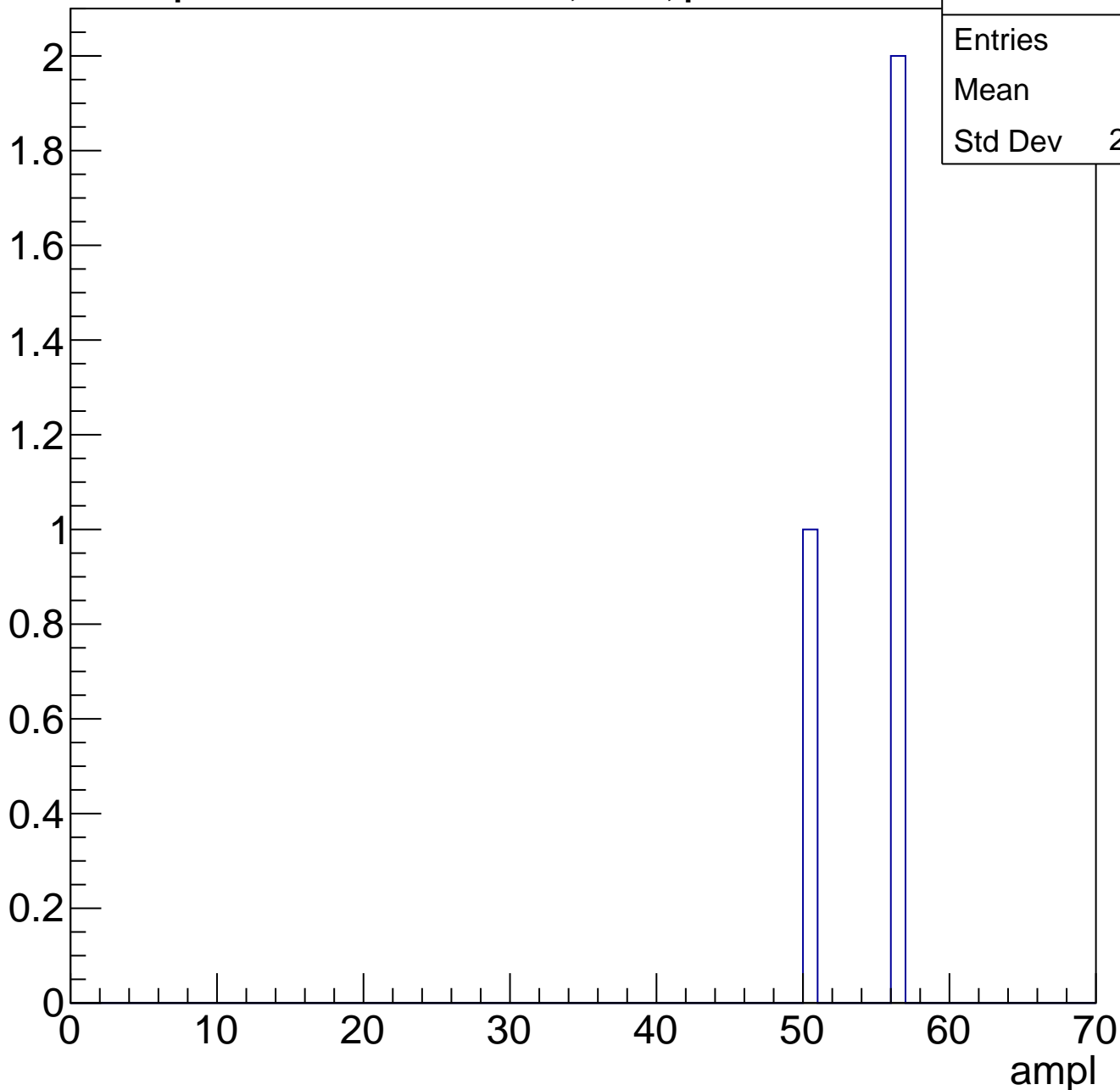
Entry



B0L100S, U12-ch2, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	3
Mean	54
Std Dev	2.828

B0L100S, U12-ch2, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch2, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch2, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch2, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch3, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch3, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch3, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch3, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch3, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch3, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch3, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch3, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch4, adc0

calib_packv5_042523_0143.root, FC#6, port A1

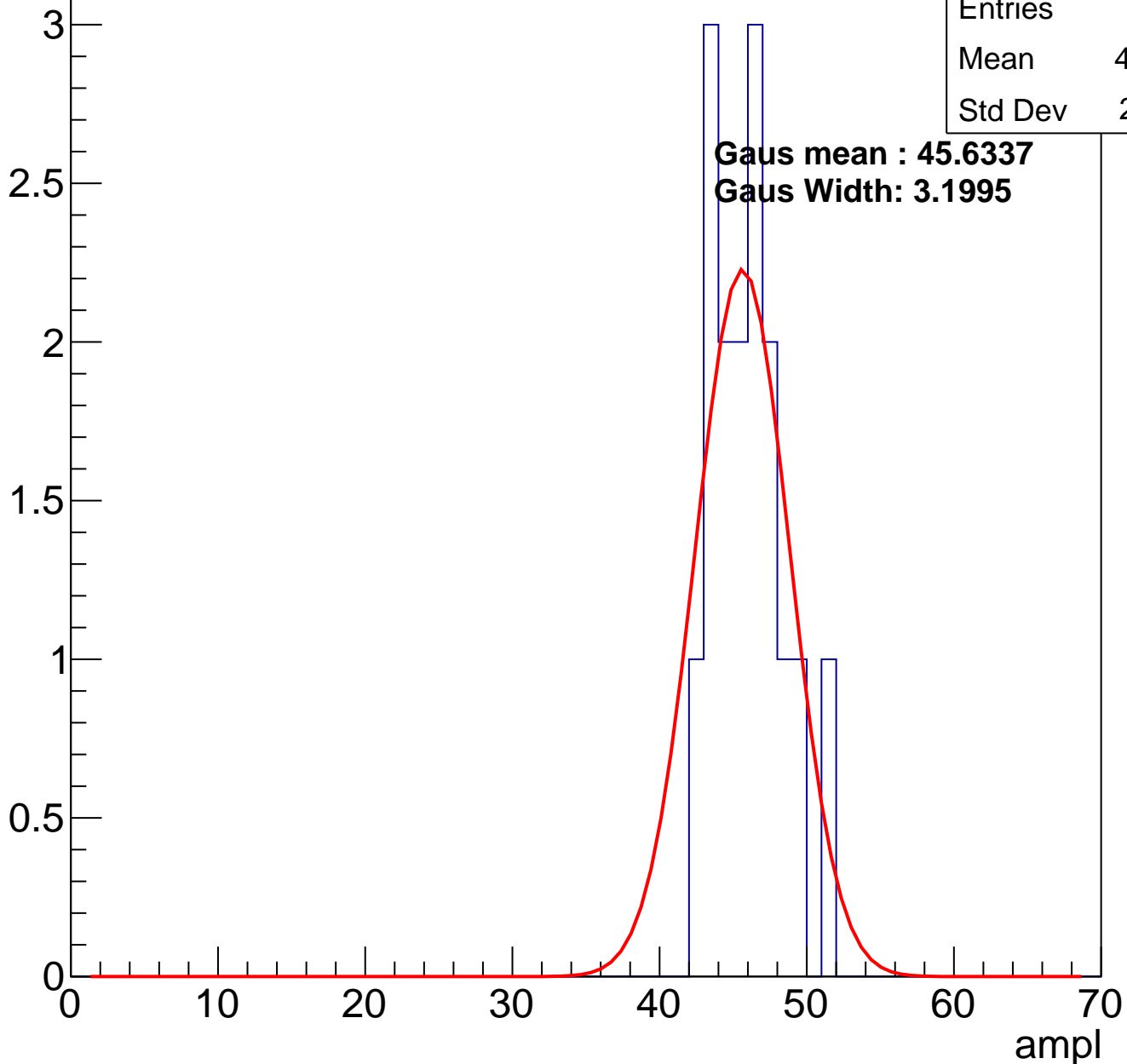
Entry



B0L100S, U12-ch4, adc1

calib_packv5_042523_0143.root, FC#6, port A1

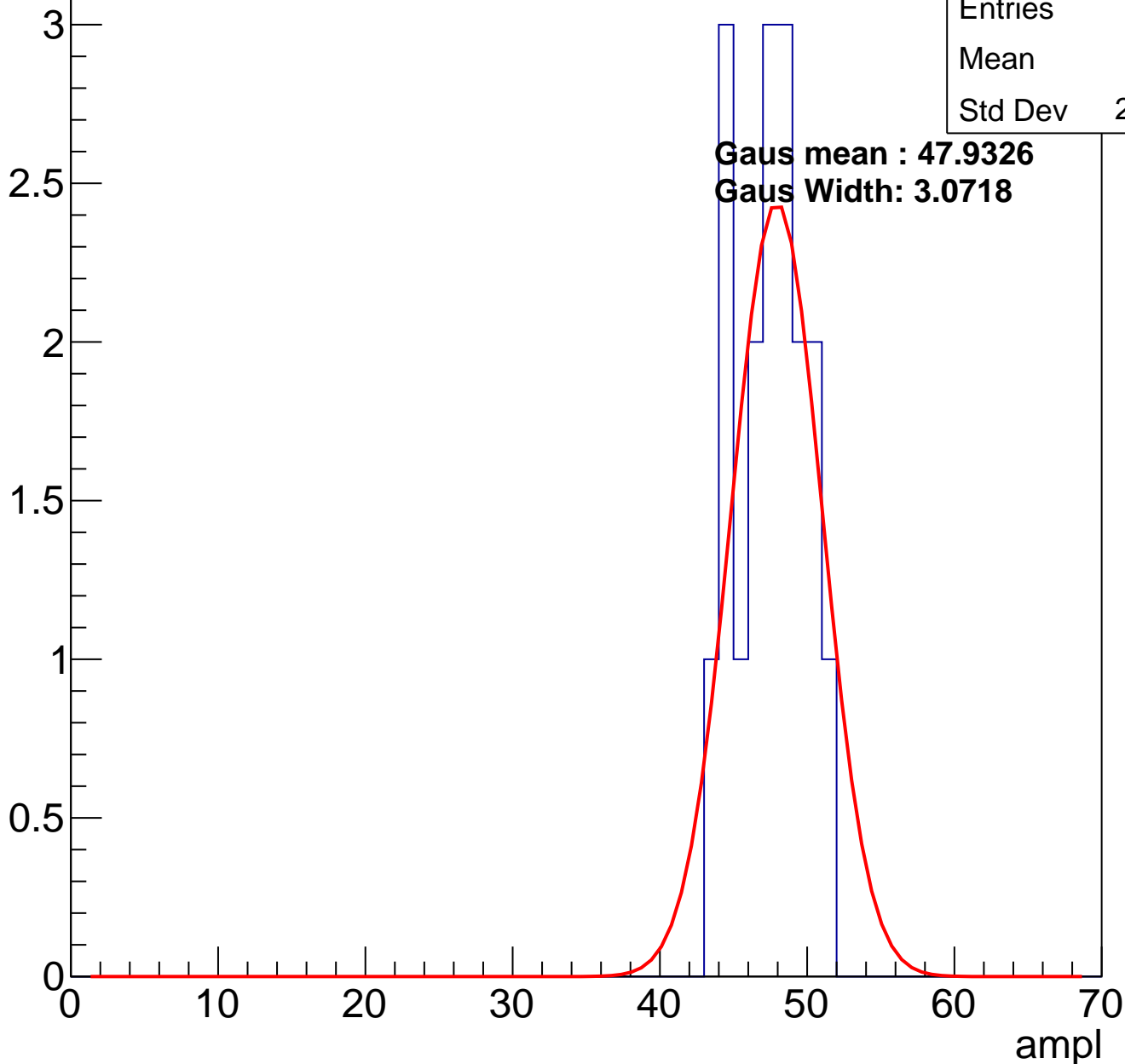
Entry



B0L100S, U12-ch4, adc2

calib_packv5_042523_0143.root, FC#6, port A1

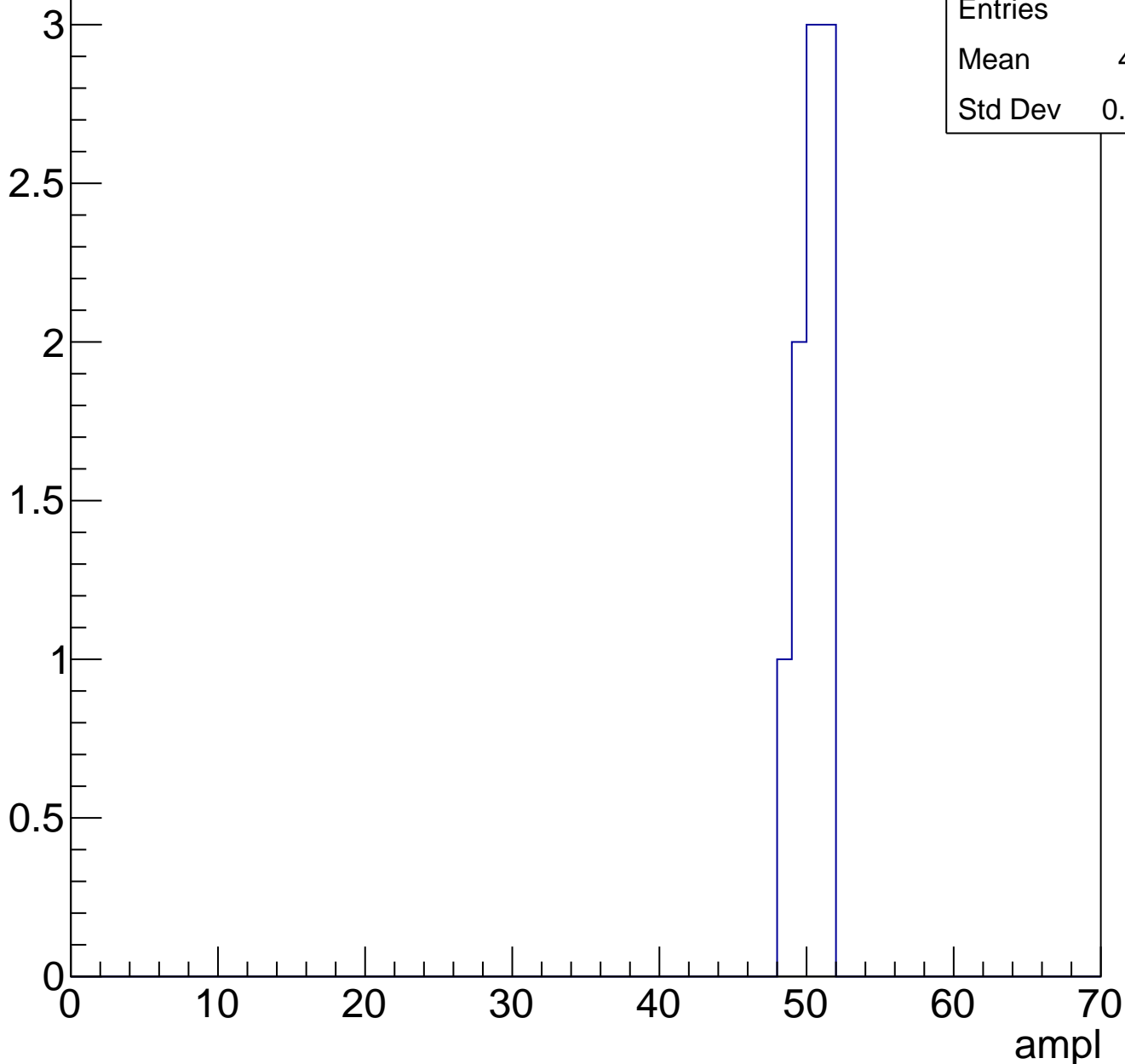
Entry



B0L100S, U12-ch4, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch4, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch4, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch4, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch4, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch5, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch5, adc1

calib_packv5_042523_0143.root, FC#6, port A1

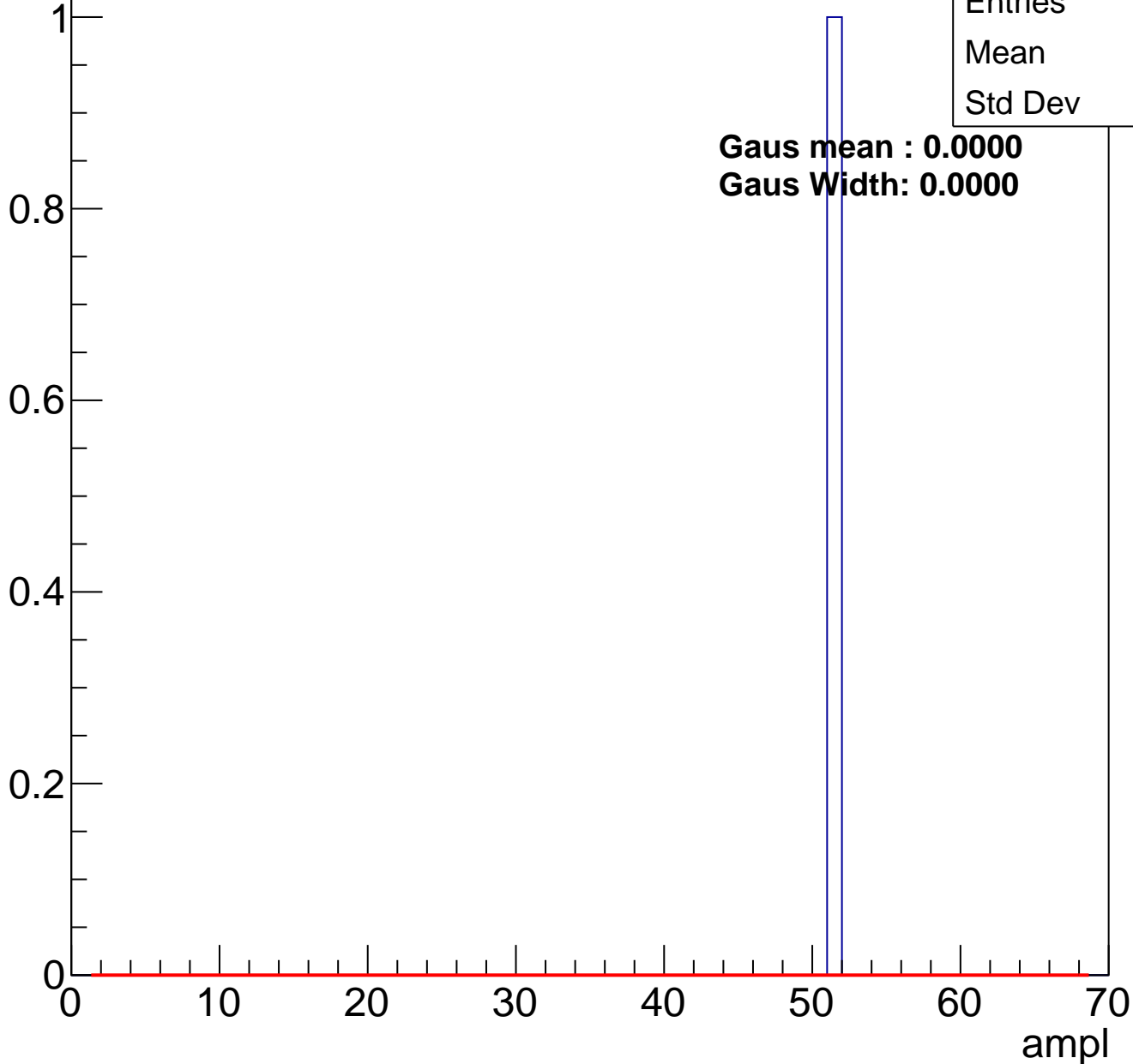
Entry



B0L100S, U12-ch5, adc2

calib_packv5_042523_0143.root, FC#6, port A1

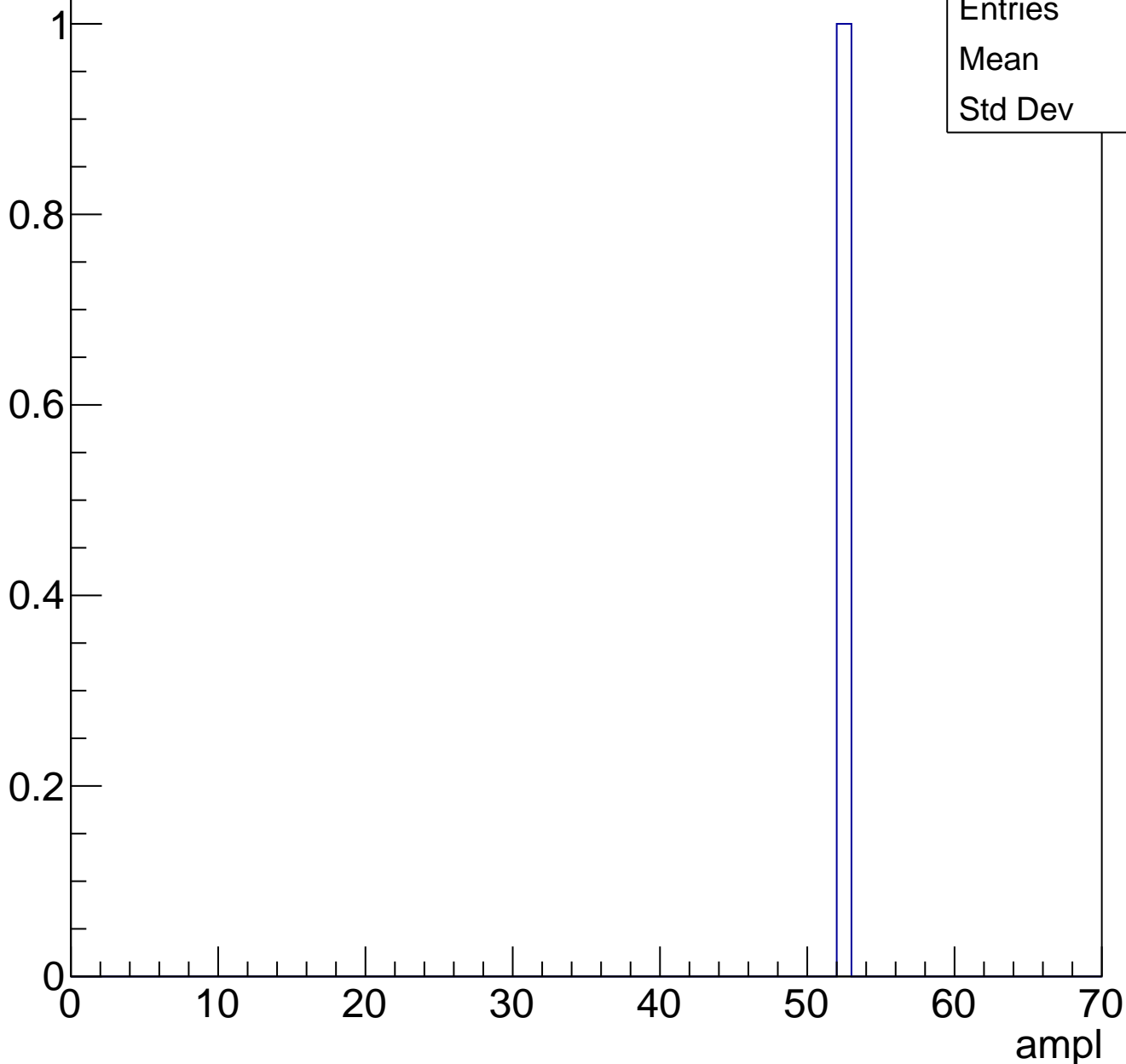
Entry



B0L100S, U12-ch5, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch5, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch5, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch5, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch5, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch6, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch6, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch6, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch6, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch6, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch6, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch6, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch6, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch7, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch7, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch7, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch7, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch7, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch7, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch7, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch7, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch8, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch8, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch8, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch8, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch8, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch8, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch8, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch8, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch9, adc0

calib_packv5_042523_0143.root, FC#6, port A1

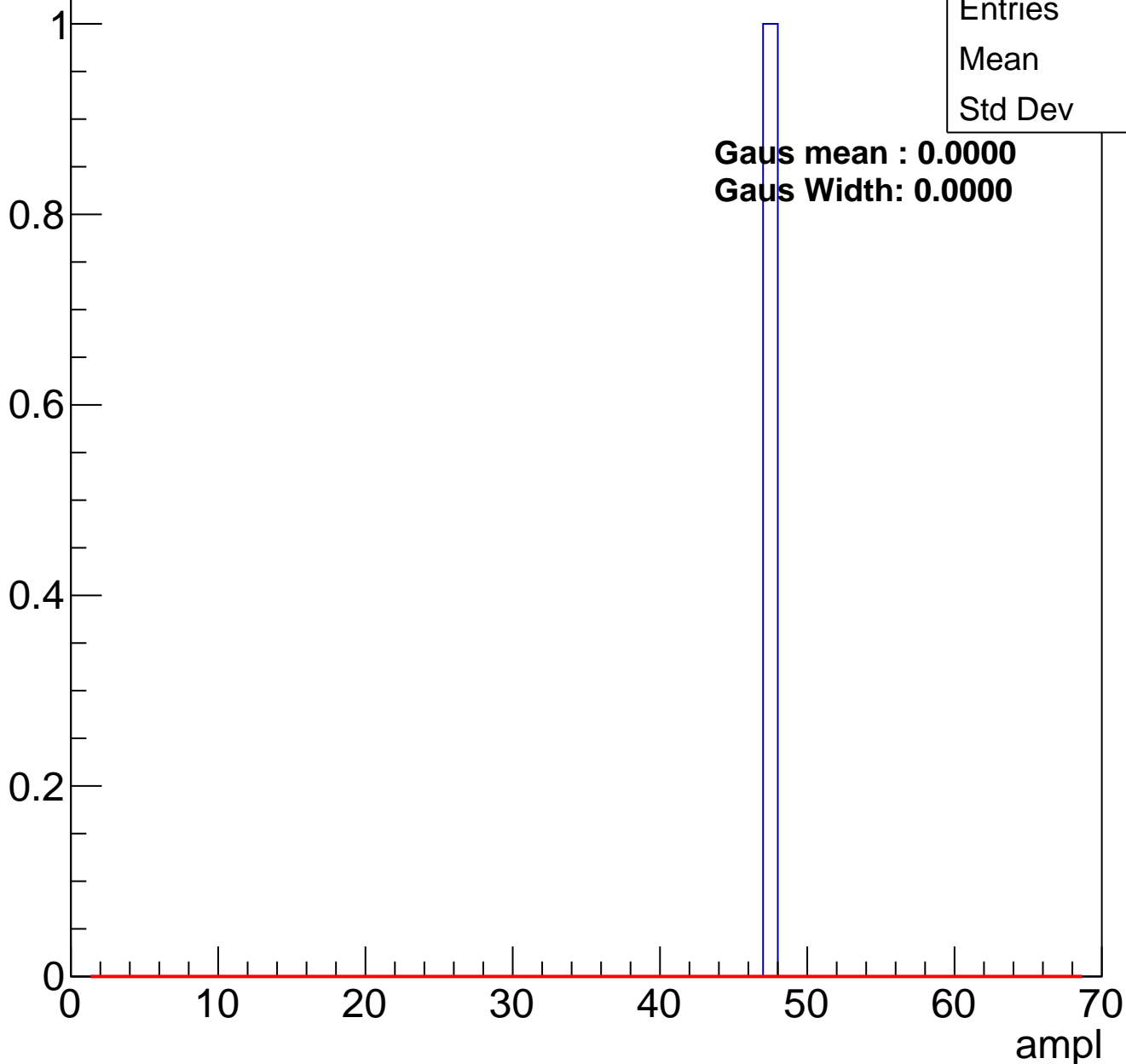
Entry



B0L100S, U12-ch9, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch9, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

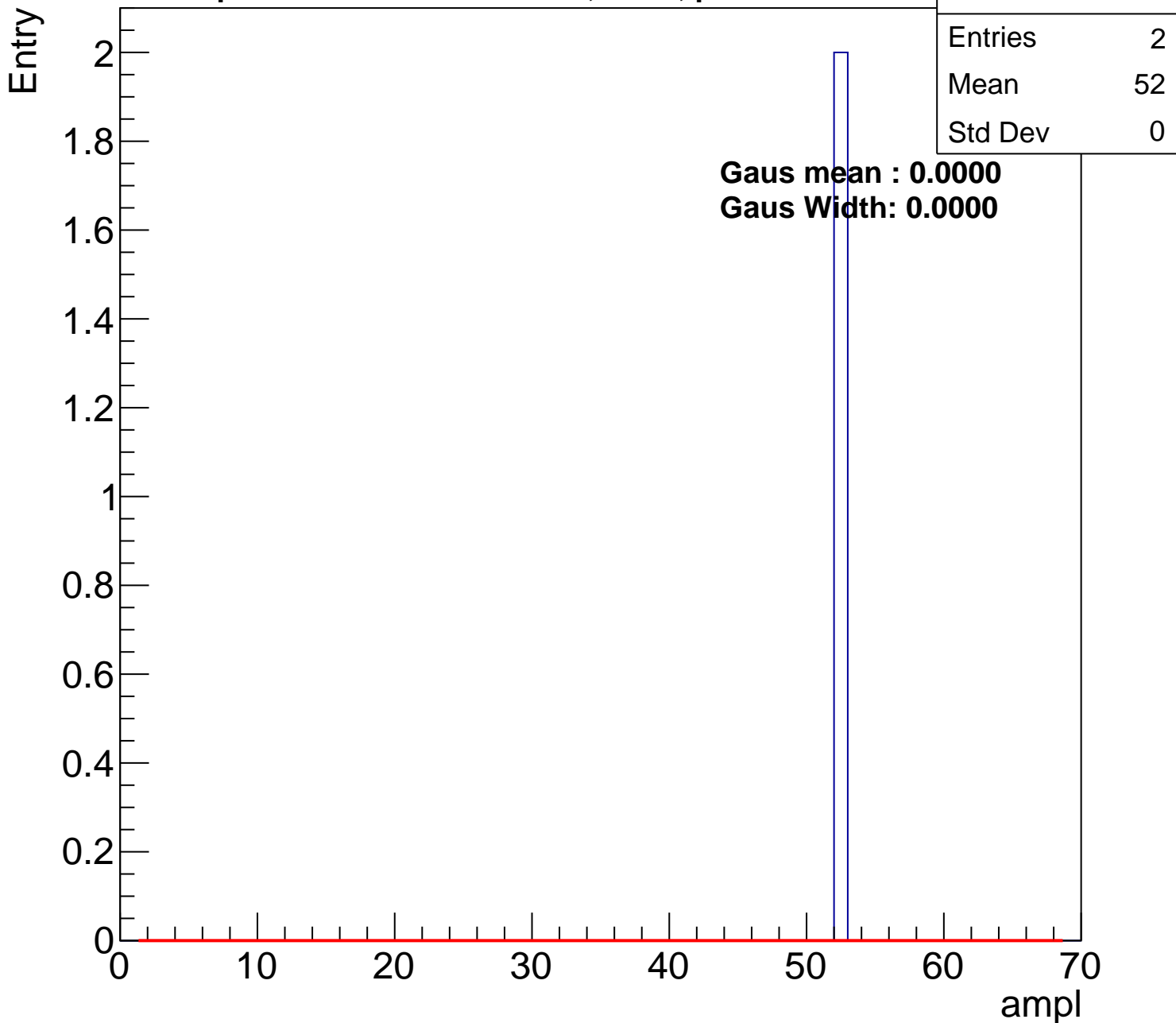
Entries	2
Mean	52
Std Dev	0

Gaus mean : 0.0000

Gaus Width: 0.0000

0 10 20 30 40 50 60 70

ampl



B0L100S, U12-ch9, adc3

calib_packv5_042523_0143.root, FC#6, port A1

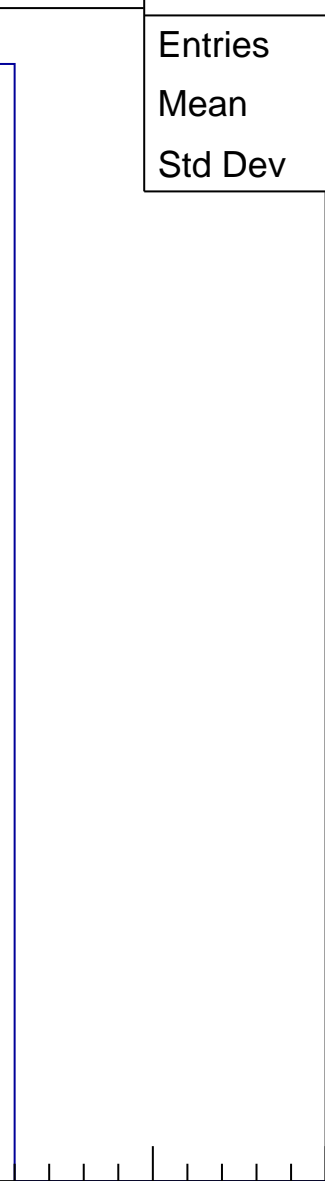
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	2
Mean	51
Std Dev	0

0 10 20 30 40 50 60 70

ampl



B0L100S, U12-ch9, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry

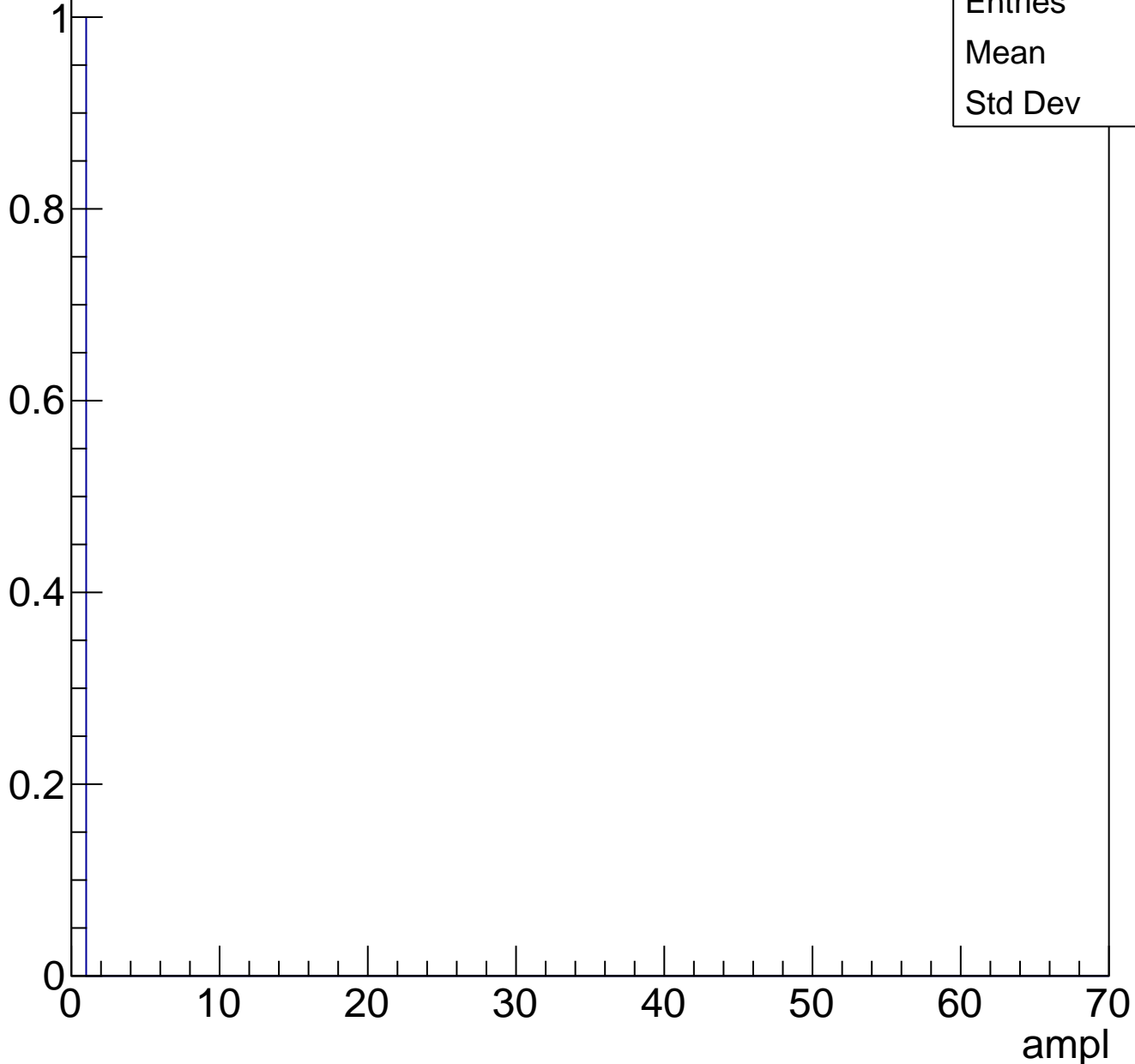


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch9, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	1
Mean	0
Std Dev	0

B0L100S, U12-ch9, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch9, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch10, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch10, adc1

calib_packv5_042523_0143.root, FC#6, port A1

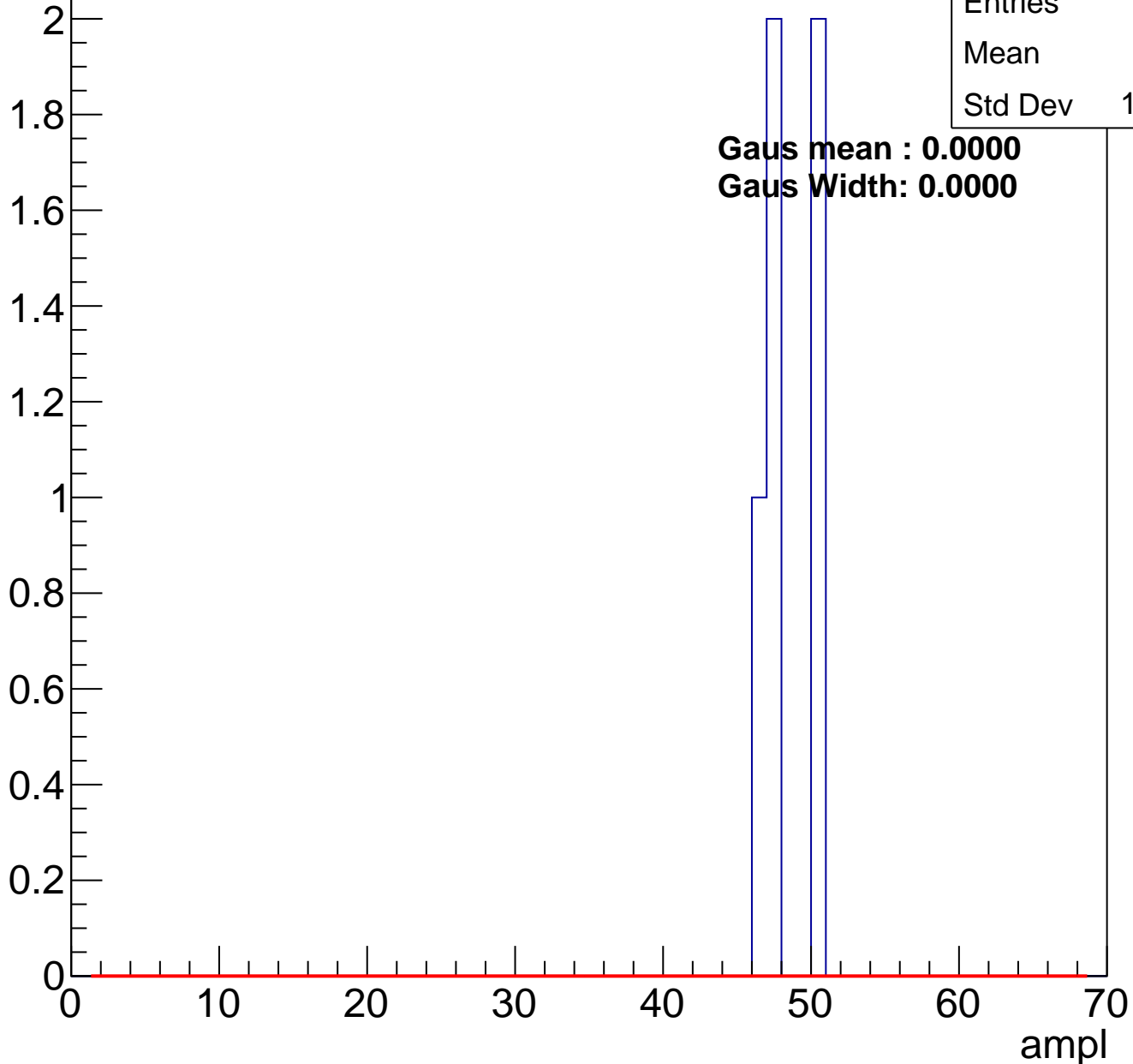
Entry



B0L100S, U12-ch10, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	5
Mean	48
Std Dev	1.673

Gaus mean : 0.0000

Gaus Width: 0.0000

B0L100S, U12-ch10, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch10, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch10, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch10, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch10, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch11, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch11, adc1

calib_packv5_042523_0143.root, FC#6, port A1

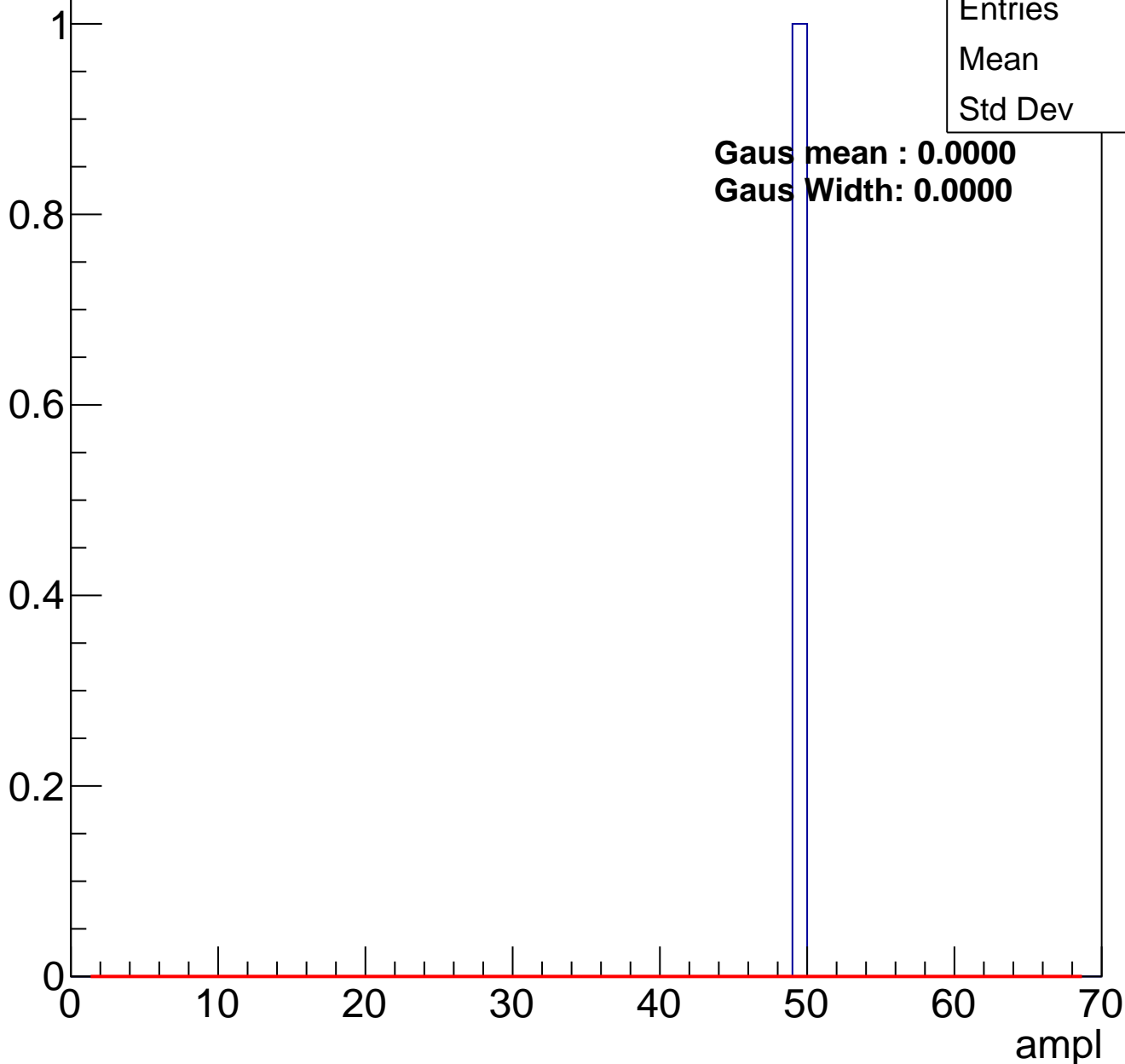
Entry



B0L100S, U12-ch11, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	1
Mean	49
Std Dev	0

B0L100S, U12-ch11, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch11, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch11, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch11, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch11, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch12, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch12, adc1

calib_packv5_042523_0143.root, FC#6, port A1

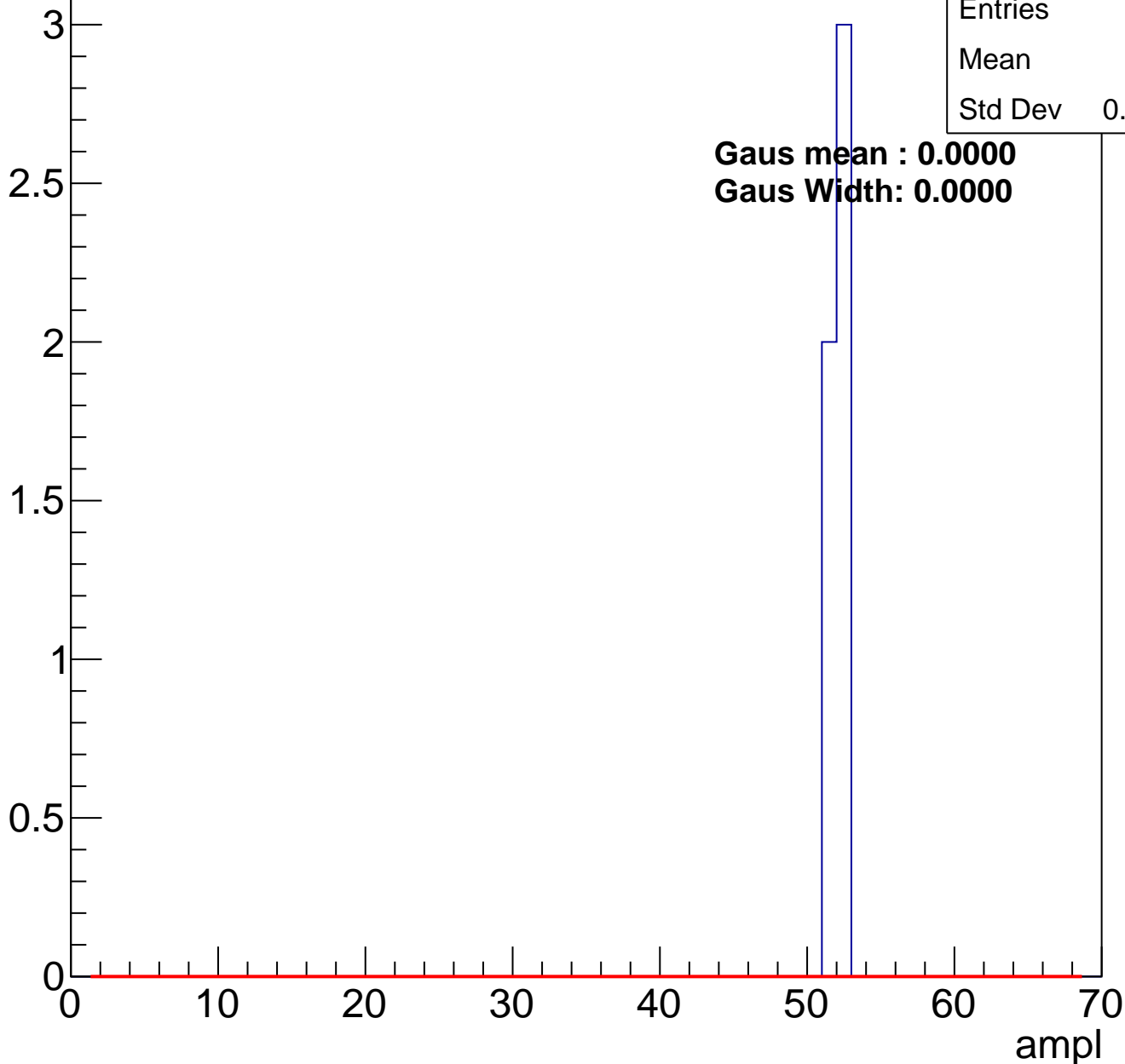
Entry



B0L100S, U12-ch12, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

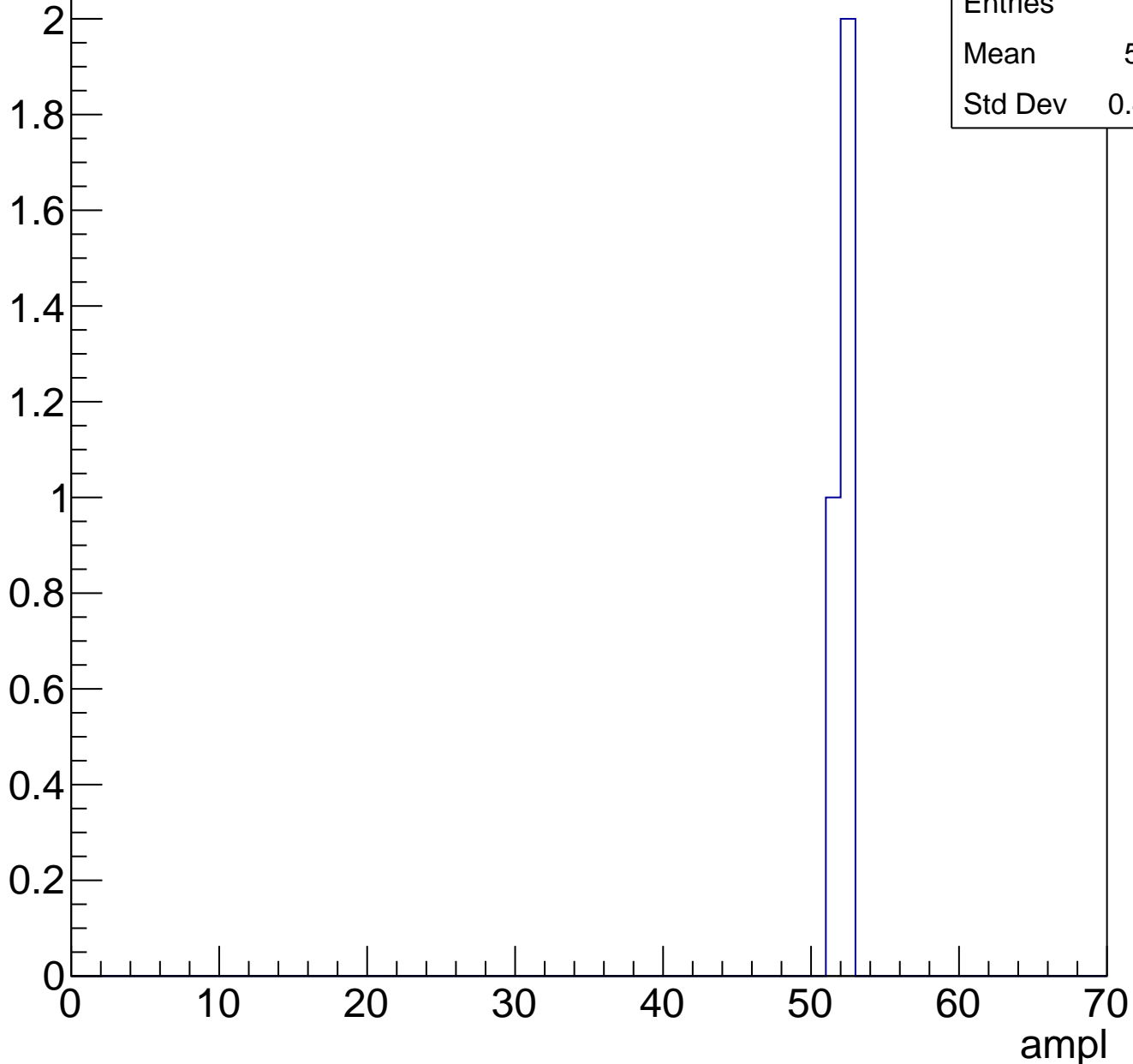


Entries	5
Mean	51.6
Std Dev	0.4899

B0L100S, U12-ch12, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch12, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch12, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch12, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch12, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch13, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch13, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch13, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch13, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch13, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch13, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch13, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch13, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch14, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch14, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	4
Mean	47.5
Std Dev	0.5

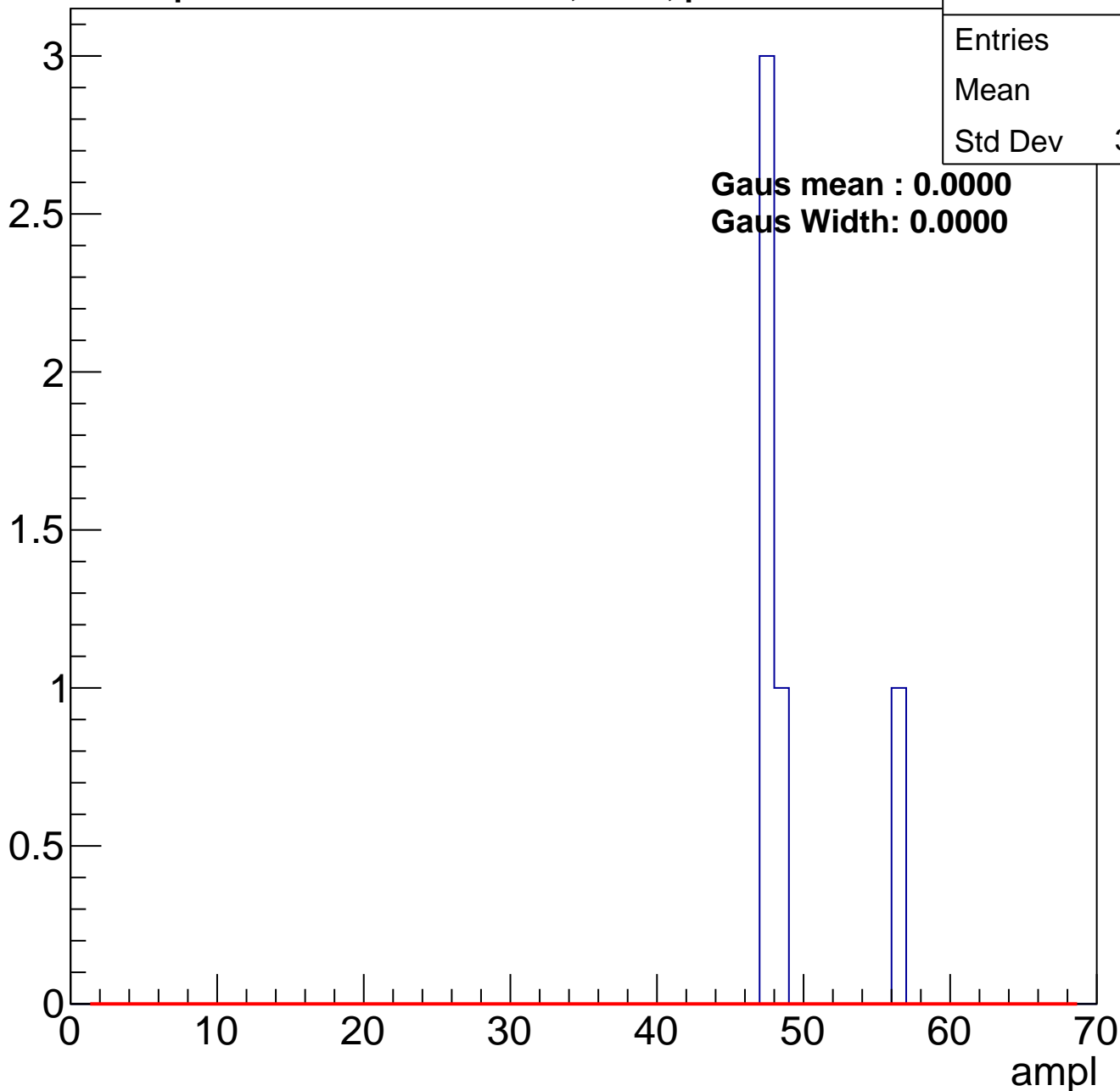
Gaus mean : 0.0000
Gaus Width: 0.0000

ampl

B0L100S, U12-ch14, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	5
Mean	49
Std Dev	3.521

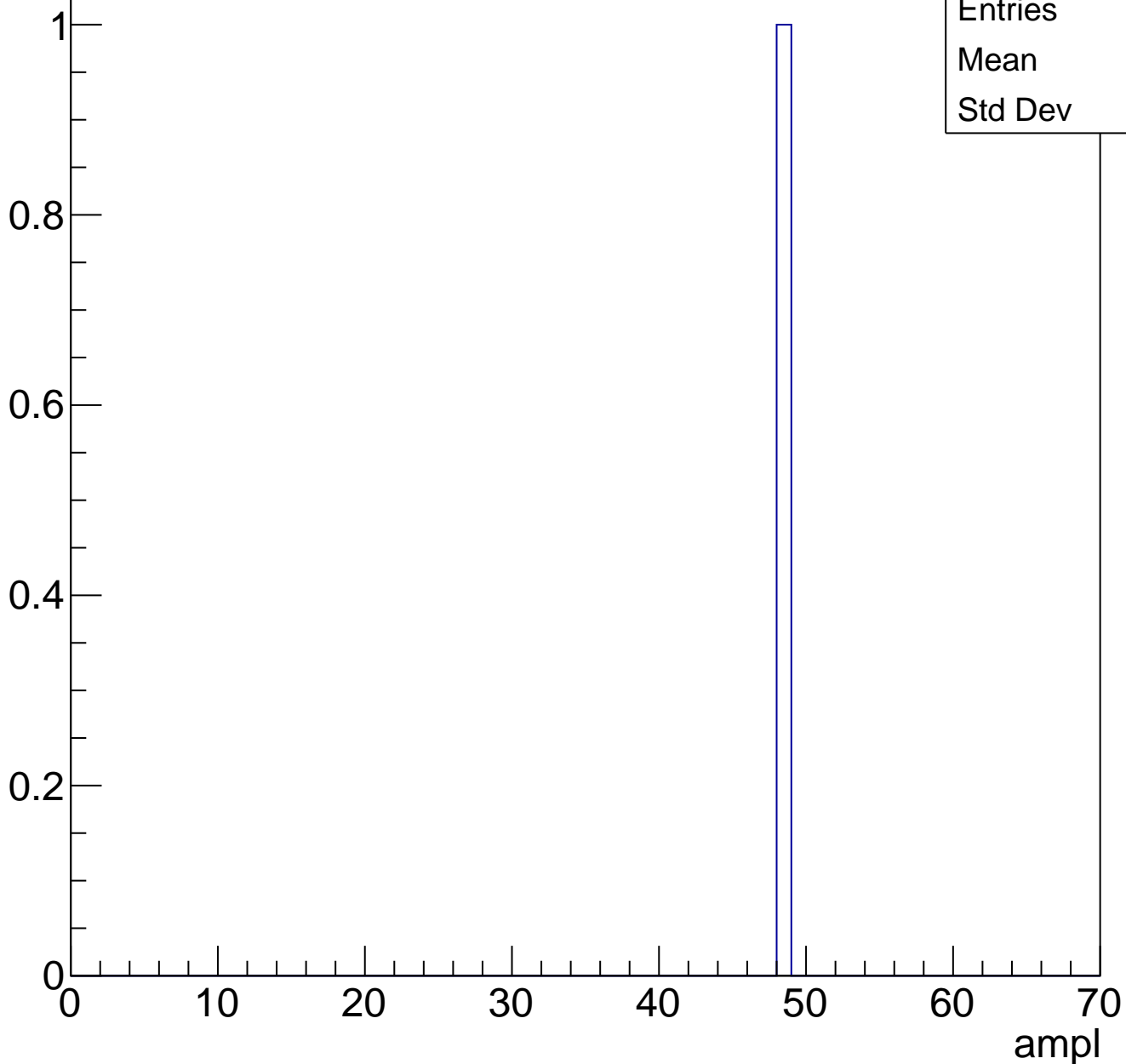
Gaus mean : 0.0000

Gaus Width: 0.0000

B0L100S, U12-ch14, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch14, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch14, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch14, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch14, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch15, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch15, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	6
Mean	46
Std Dev	1.915

Gaus mean : 0.0000

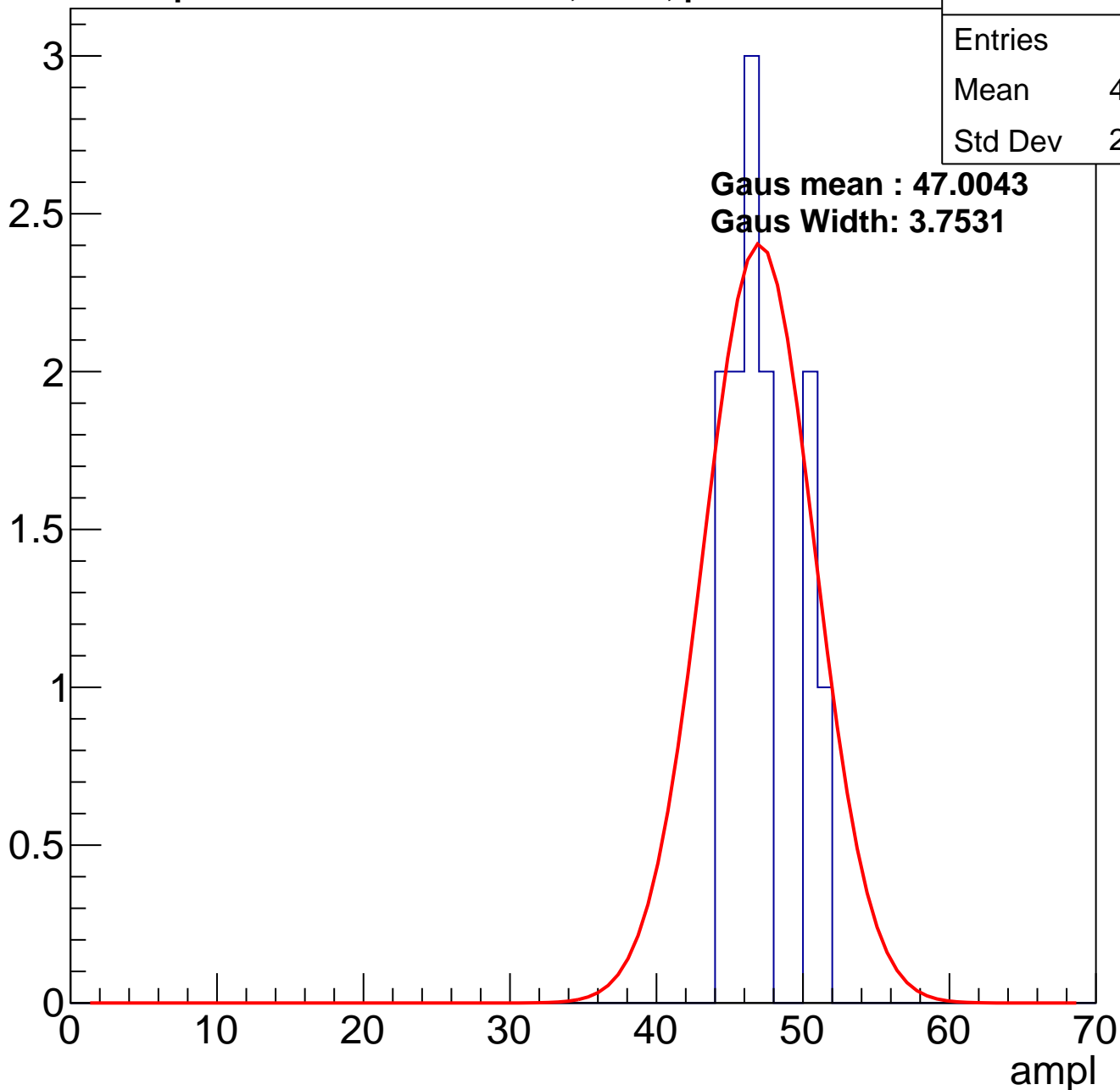
Gaus Width: 0.0000

0 10 20 30 40 50 60 70
ampl

B0L100S, U12-ch15, adc2

calib_packv5_042523_0143.root, FC#6, port A1

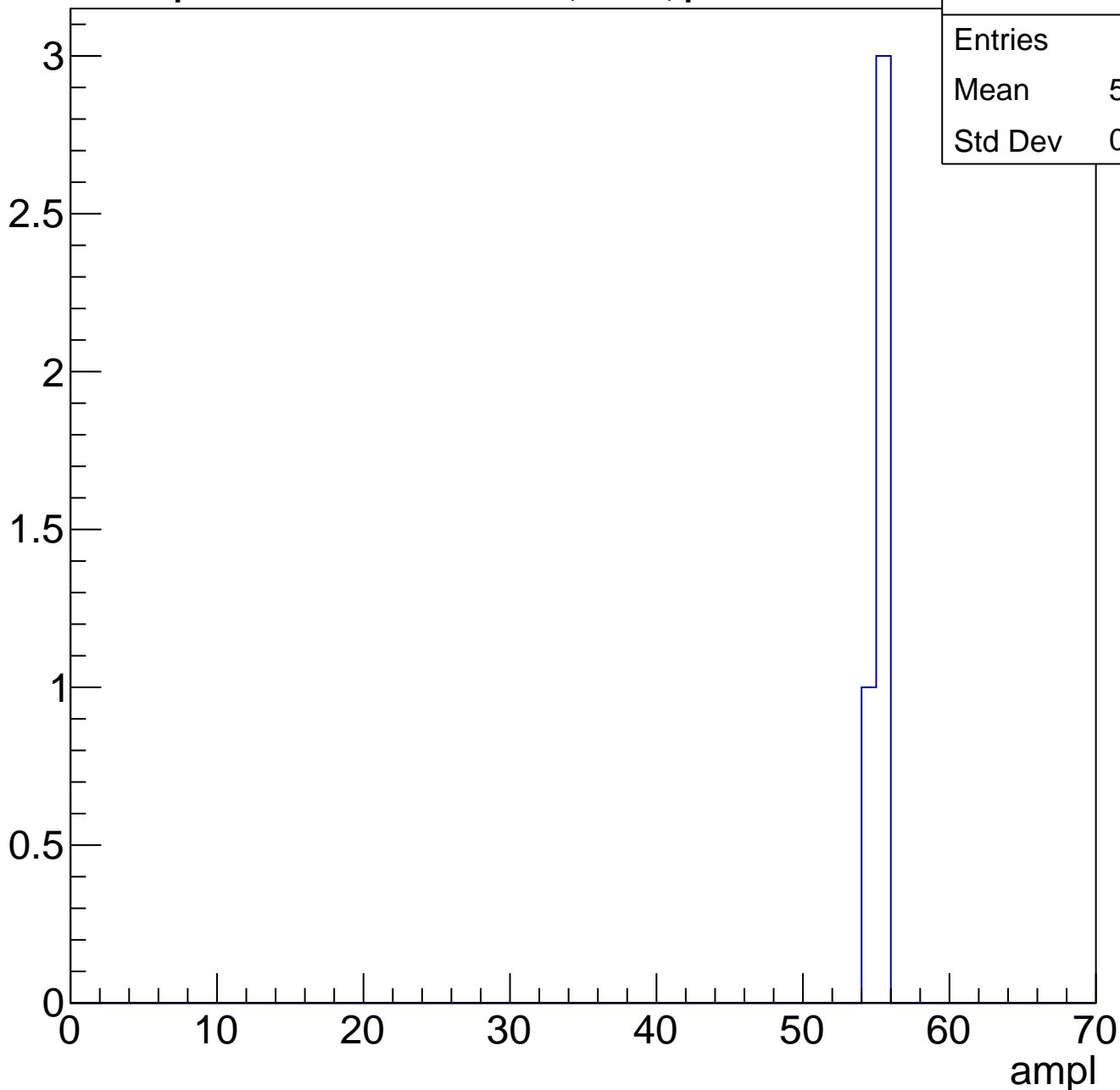
Entry



B0L100S, U12-ch15, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch15, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch15, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch15, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch15, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch16, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch16, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch16, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch16, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch16, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch16, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch16, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch16, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch17, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry

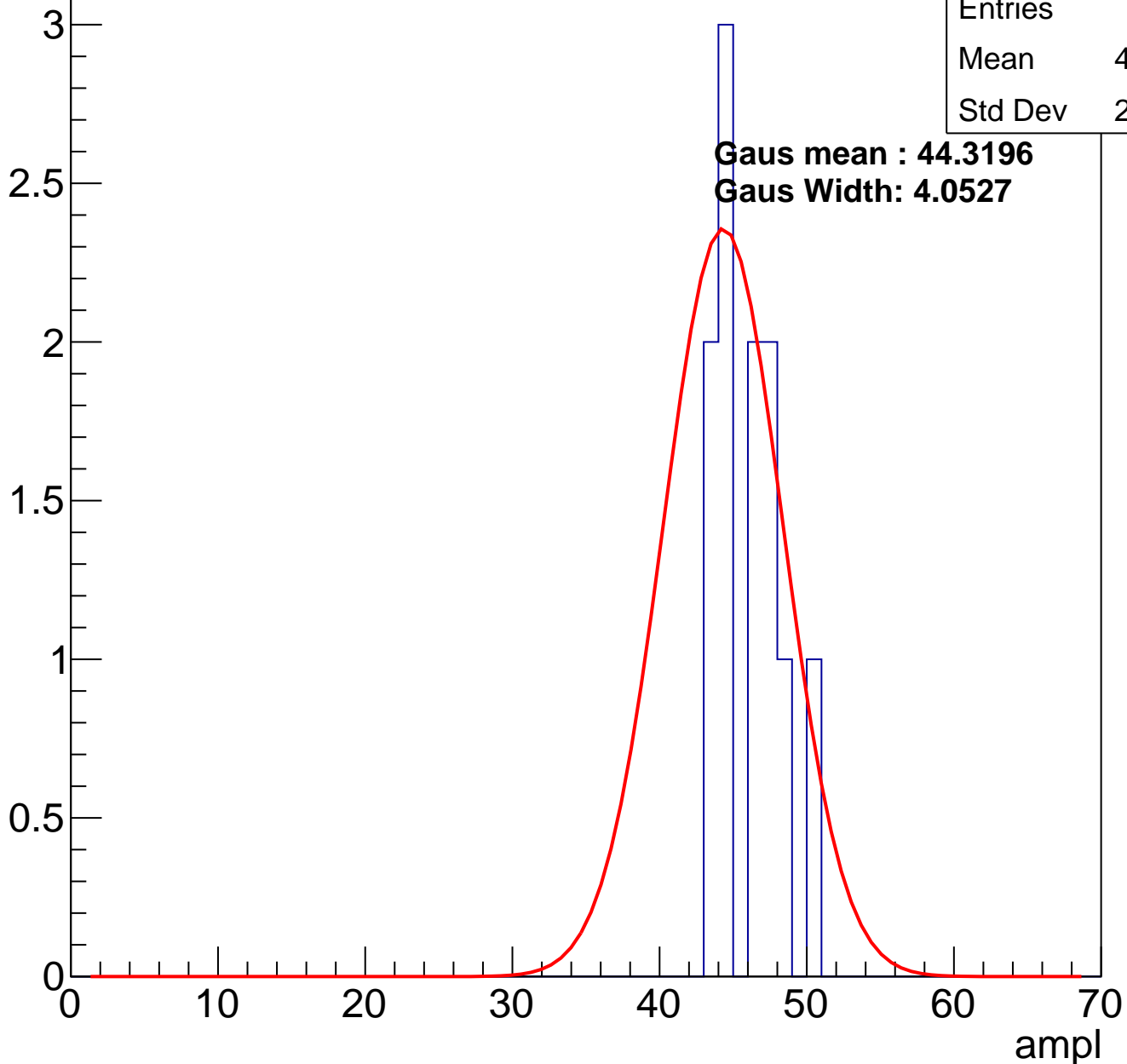


Entries	1
Mean	0
Std Dev	0

B0L100S, U12-ch17, adc1

calib_packv5_042523_0143.root, FC#6, port A1

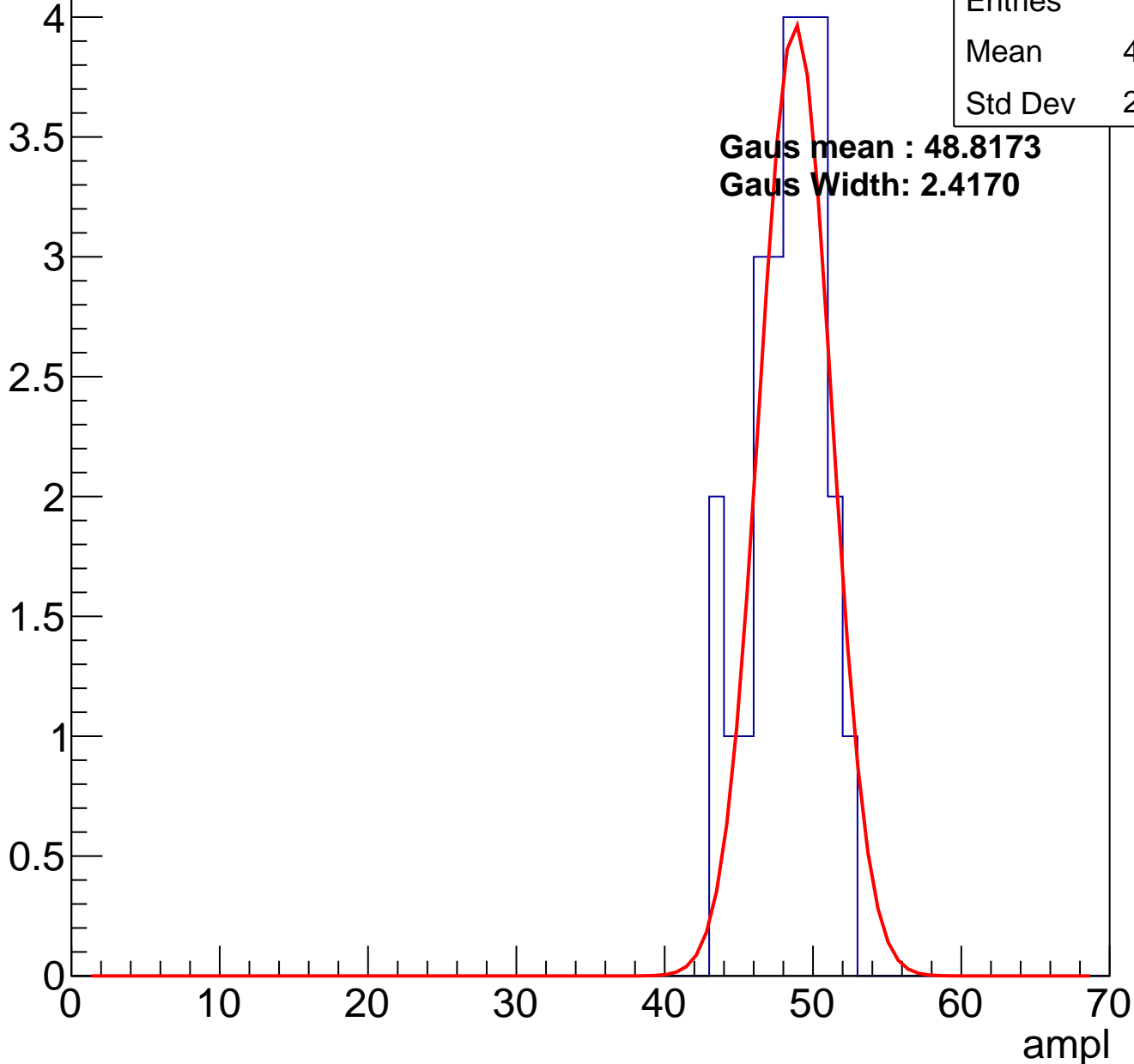
Entry



B0L100S, U12-ch17, adc2

calib_packv5_042523_0143.root, FC#6, port A1

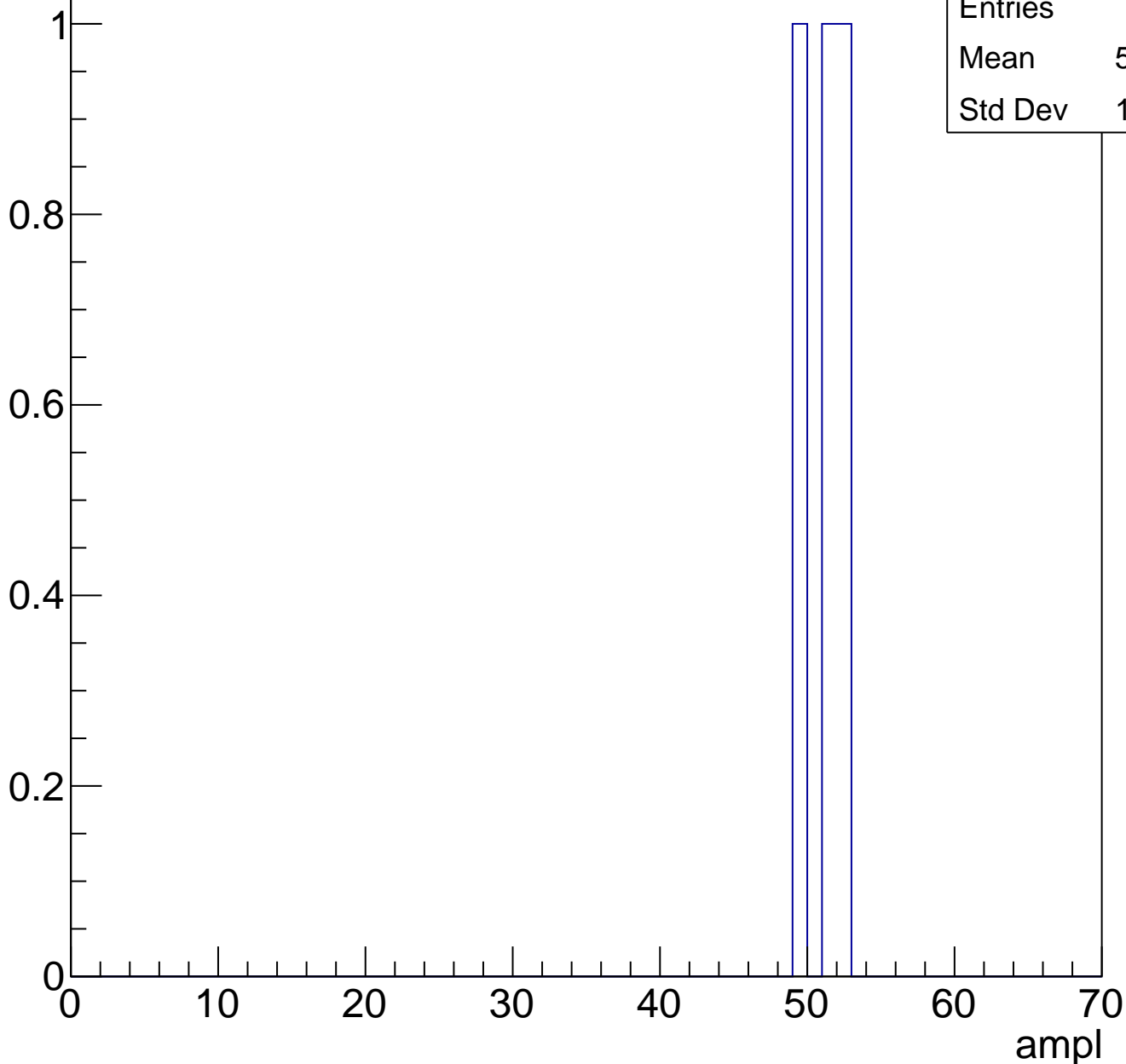
Entry



B0L100S, U12-ch17, adc3

calib_packv5_042523_0143.root, FC#6, port A1

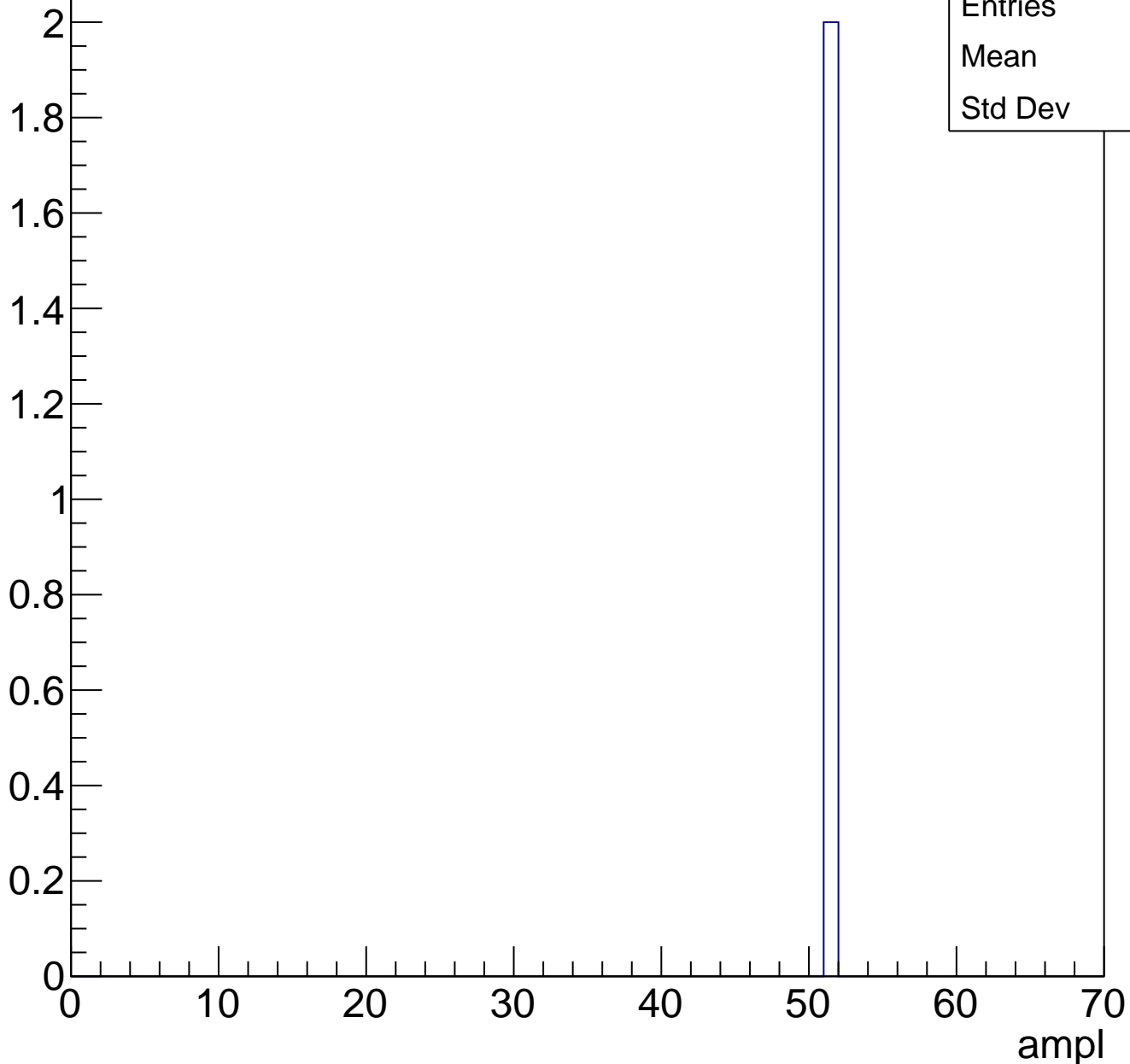
Entry



B0L100S, U12-ch17, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch17, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch17, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch17, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry

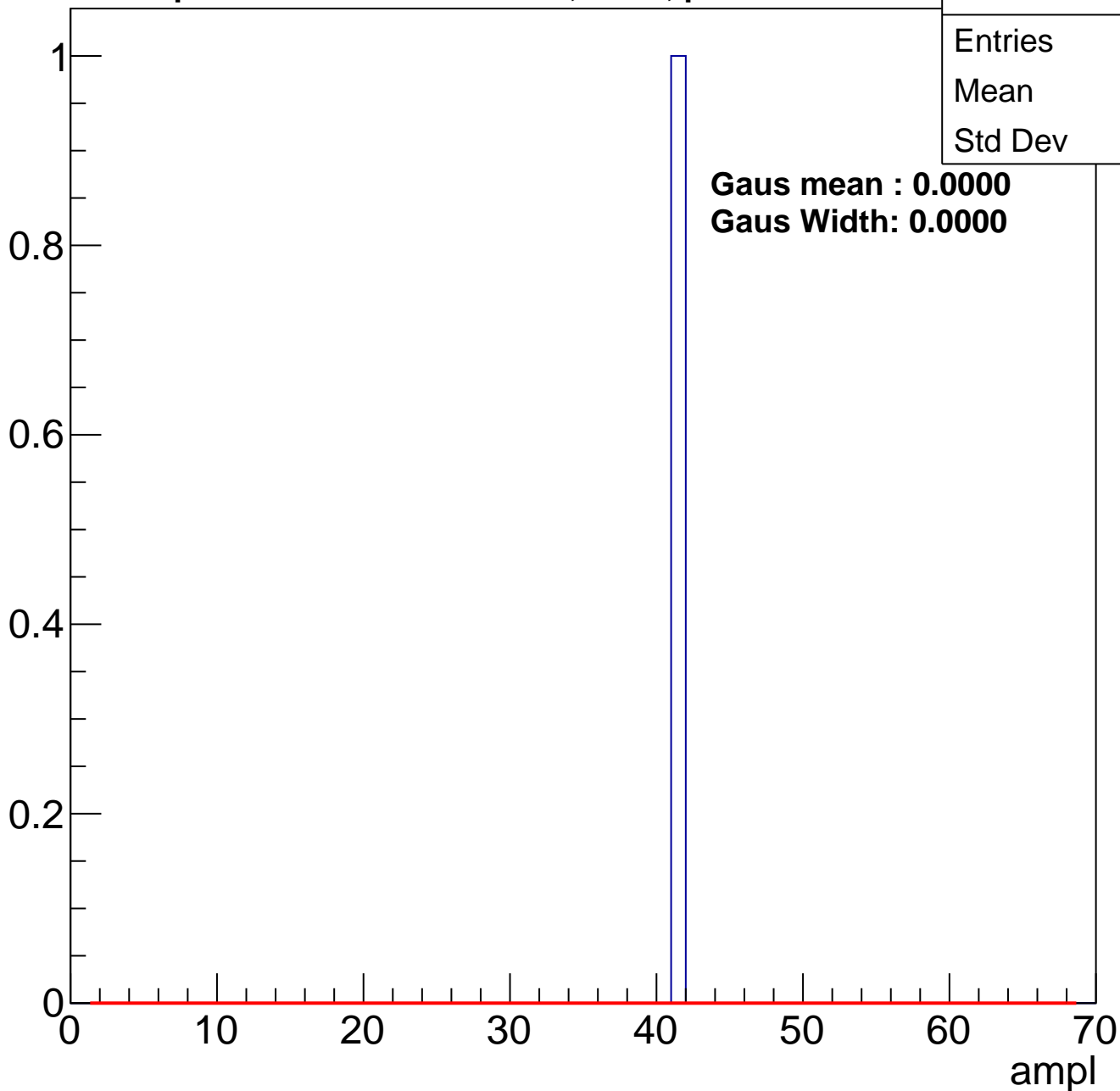


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch18, adc0

calib_packv5_042523_0143.root, FC#6, port A1

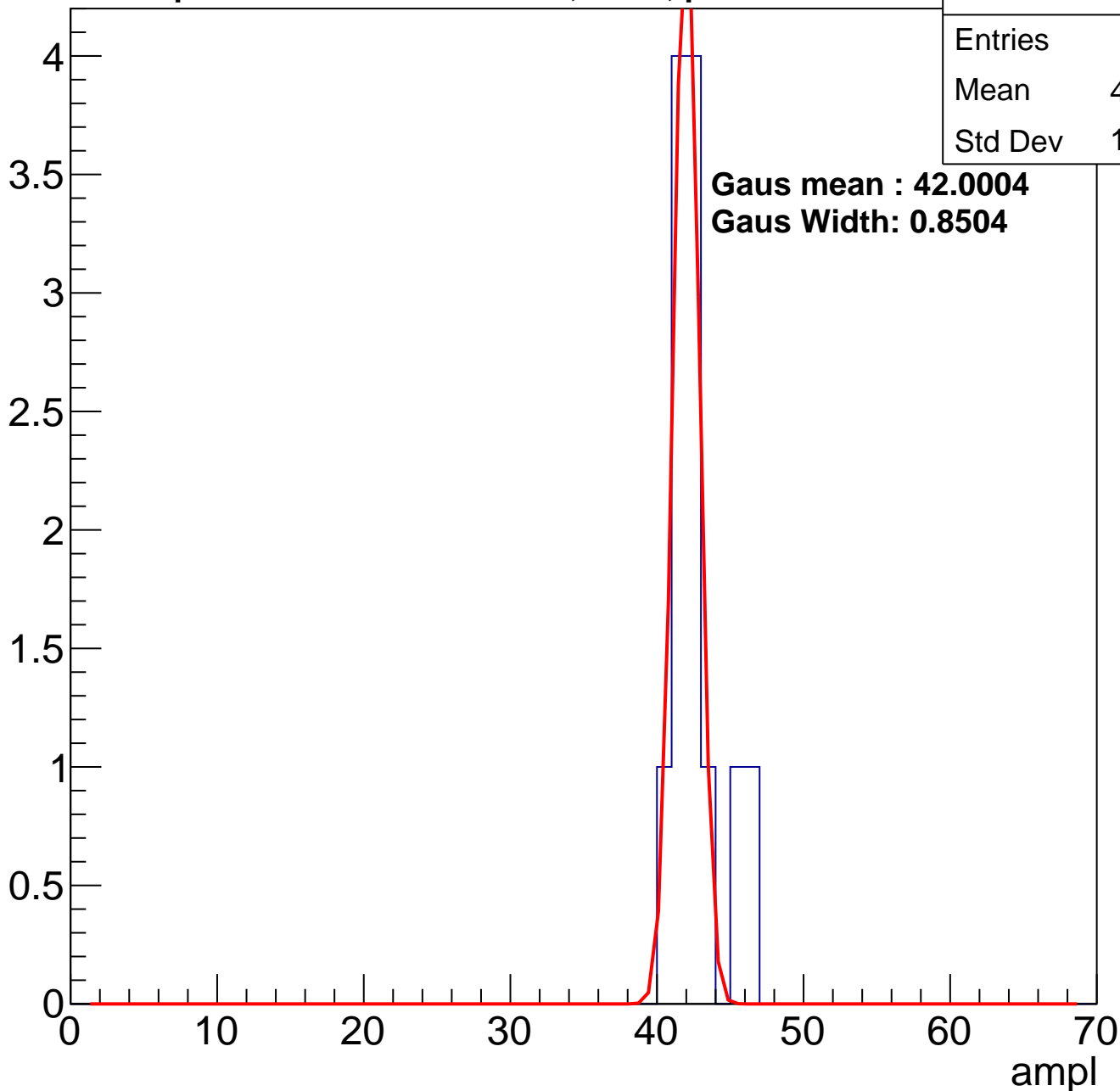
Entry



B0L100S, U12-ch18, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch18, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

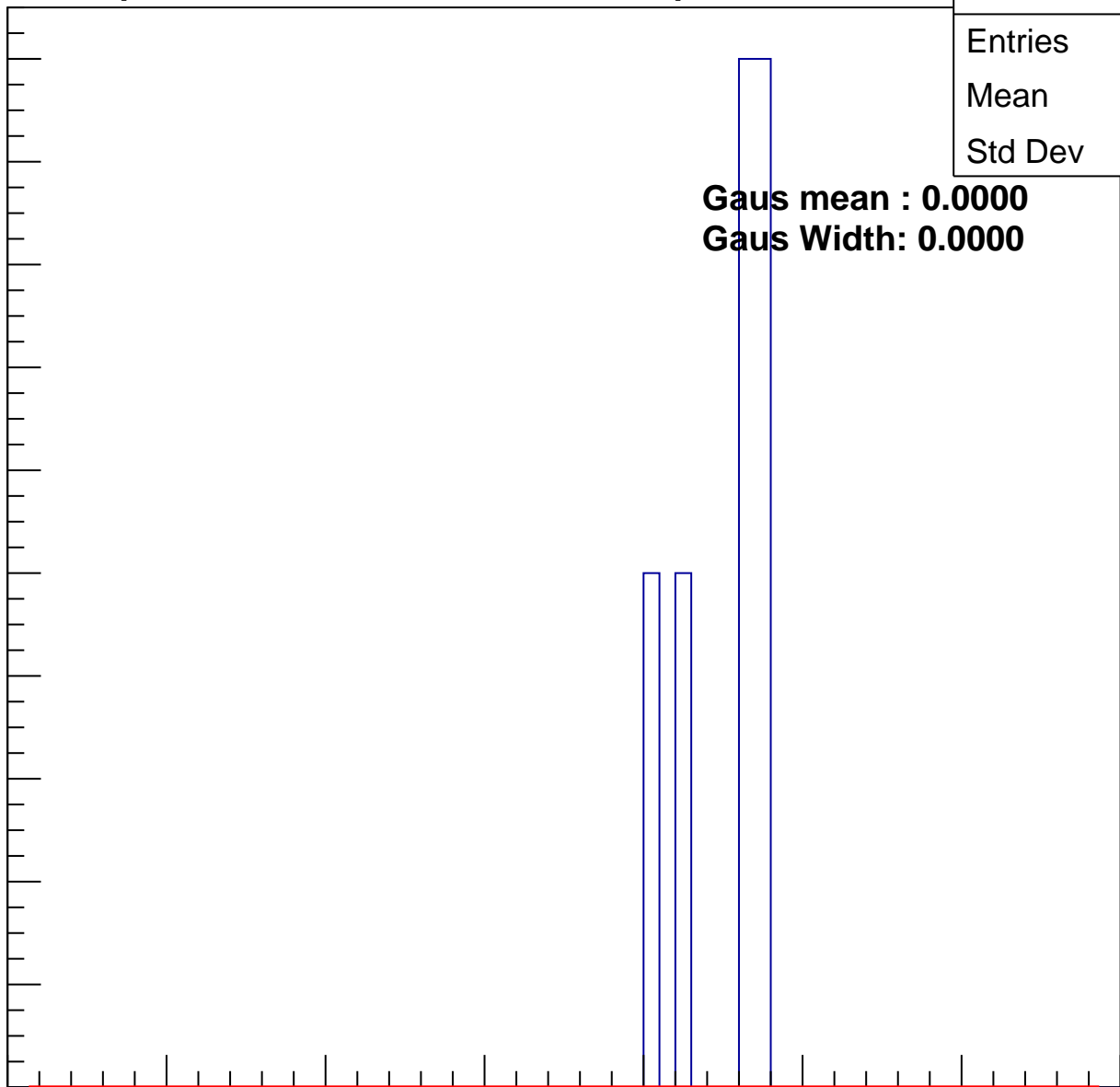
Entries	6
Mean	44.67
Std Dev	2.687

Gaus mean : 0.0000

Gaus Width: 0.0000

0 10 20 30 40 50 60 70

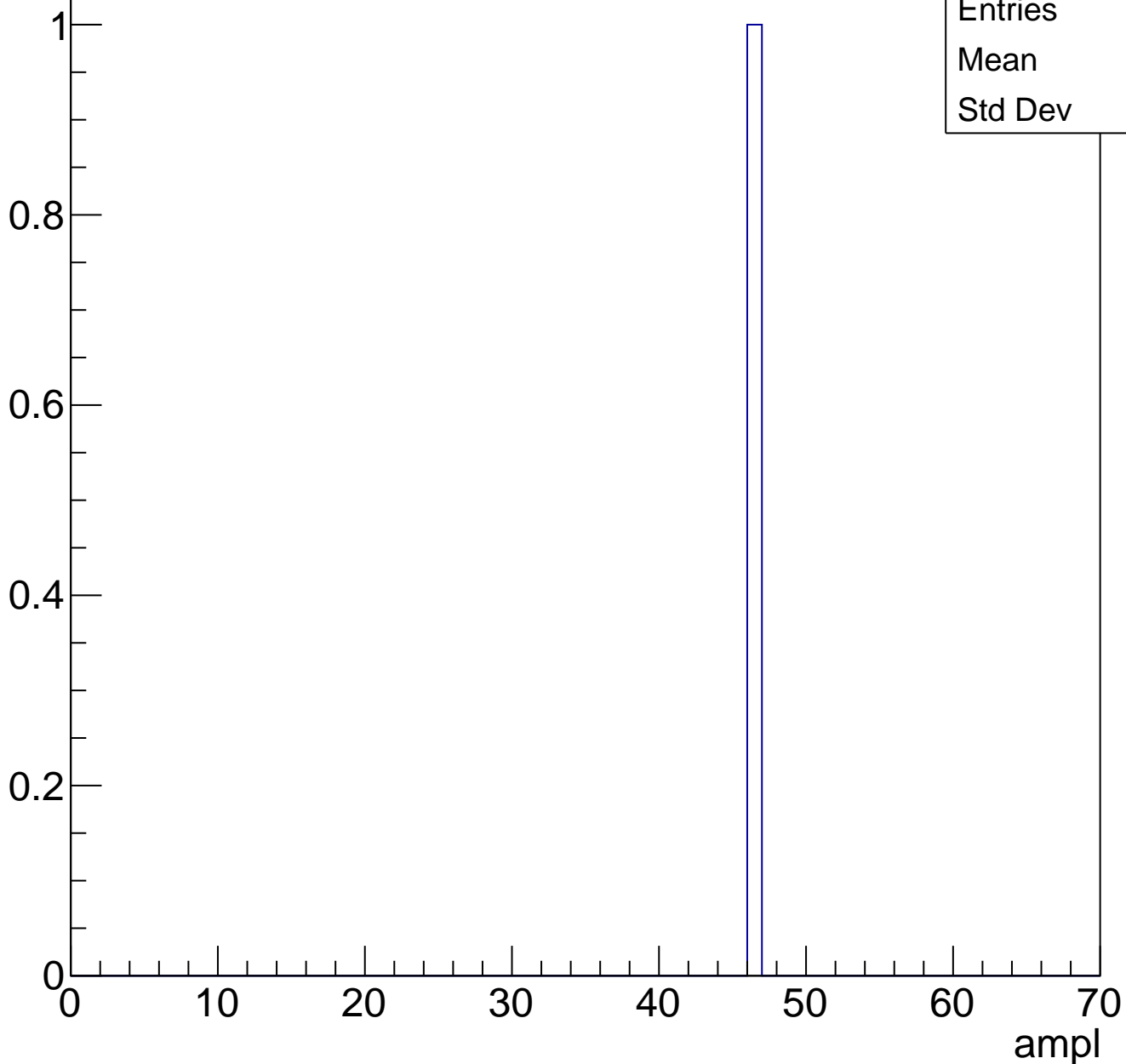
ampl



B0L100S, U12-ch18, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch18, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch18, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch18, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch18, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch19, adc0

calib_packv5_042523_0143.root, FC#6, port A1

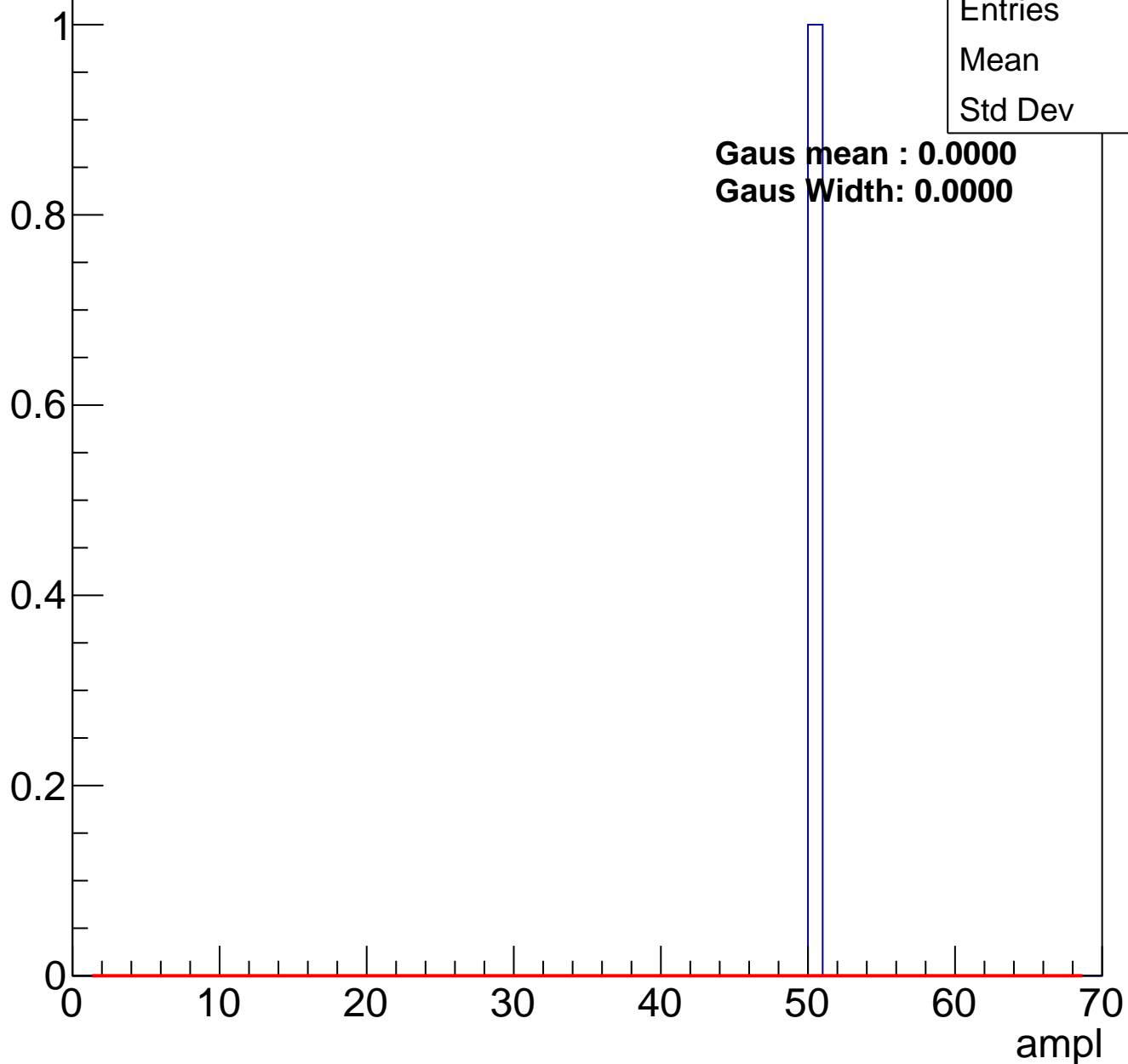
Entry



B0L100S, U12-ch19, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch19, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

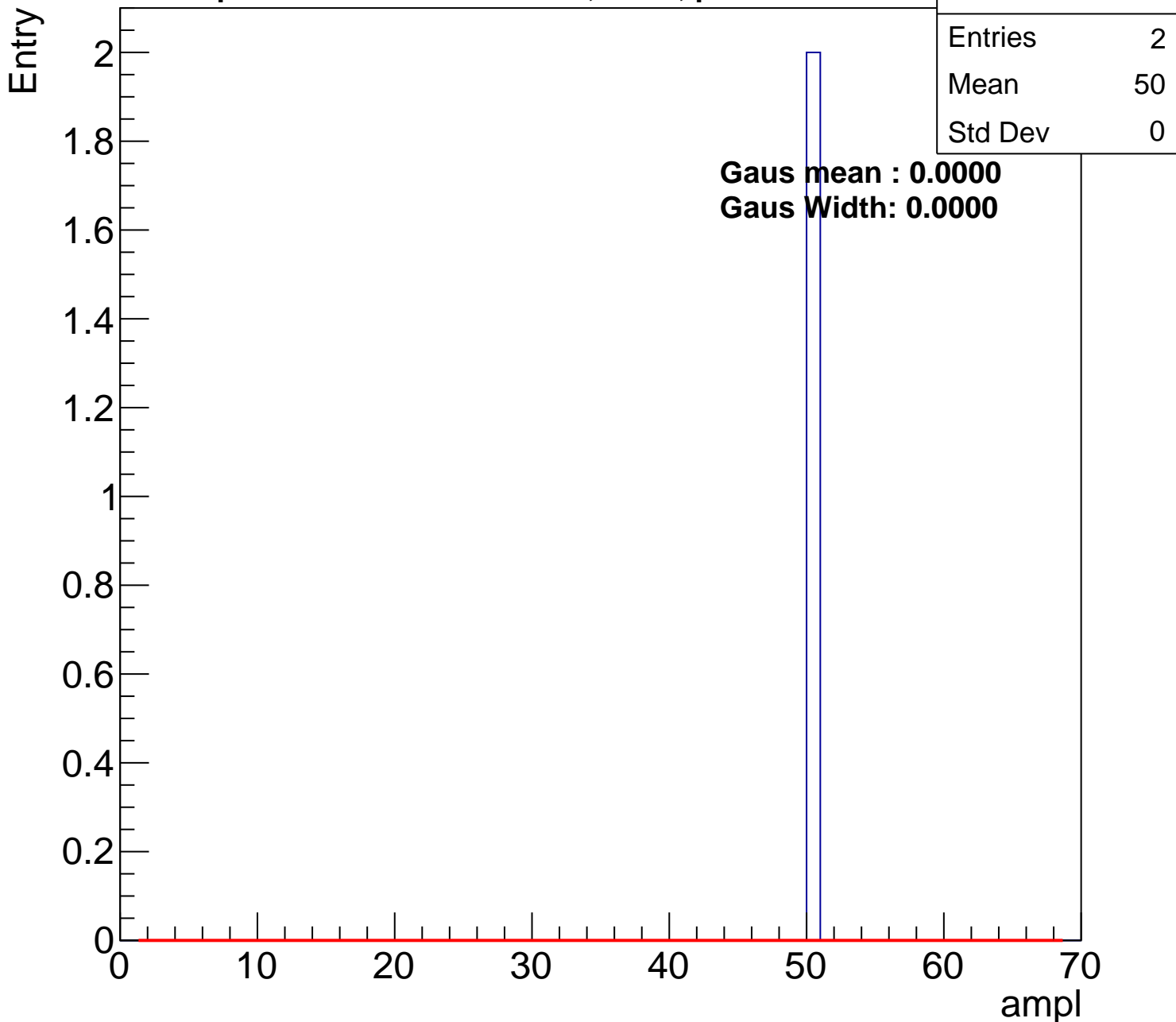
Entries	2
Mean	50
Std Dev	0

Gaus mean : 0.0000

Gaus Width: 0.0000

0 10 20 30 40 50 60 70

ampl



B0L100S, U12-ch19, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch19, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch19, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch19, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch19, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch20, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch20, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	7
Mean	49
Std Dev	2

Gaus mean : 0.0000

Gaus Width: 0.0000

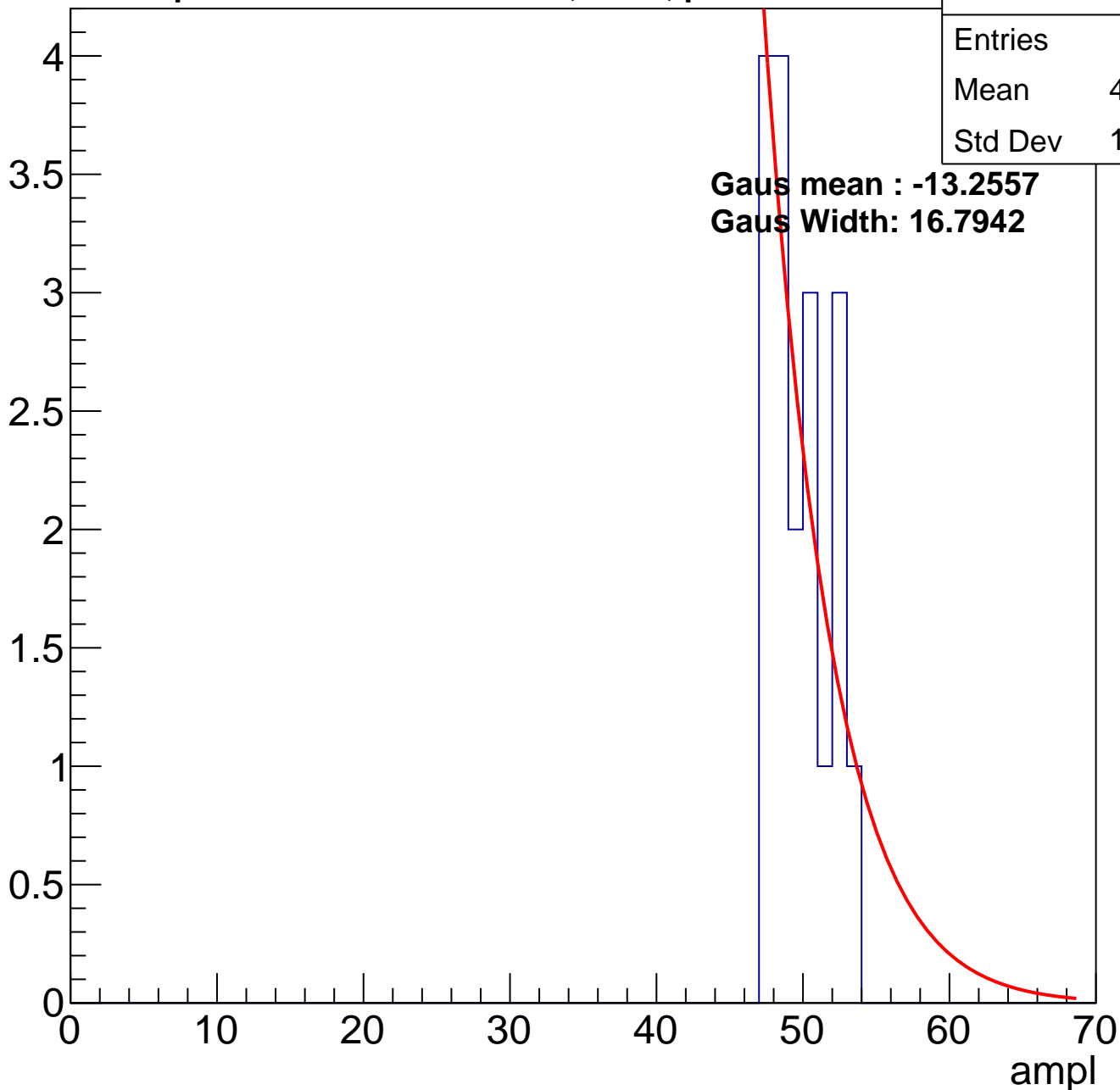
ampl

0 10 20 30 40 50 60 70

B0L100S, U12-ch20, adc2

calib_packv5_042523_0143.root, FC#6, port A1

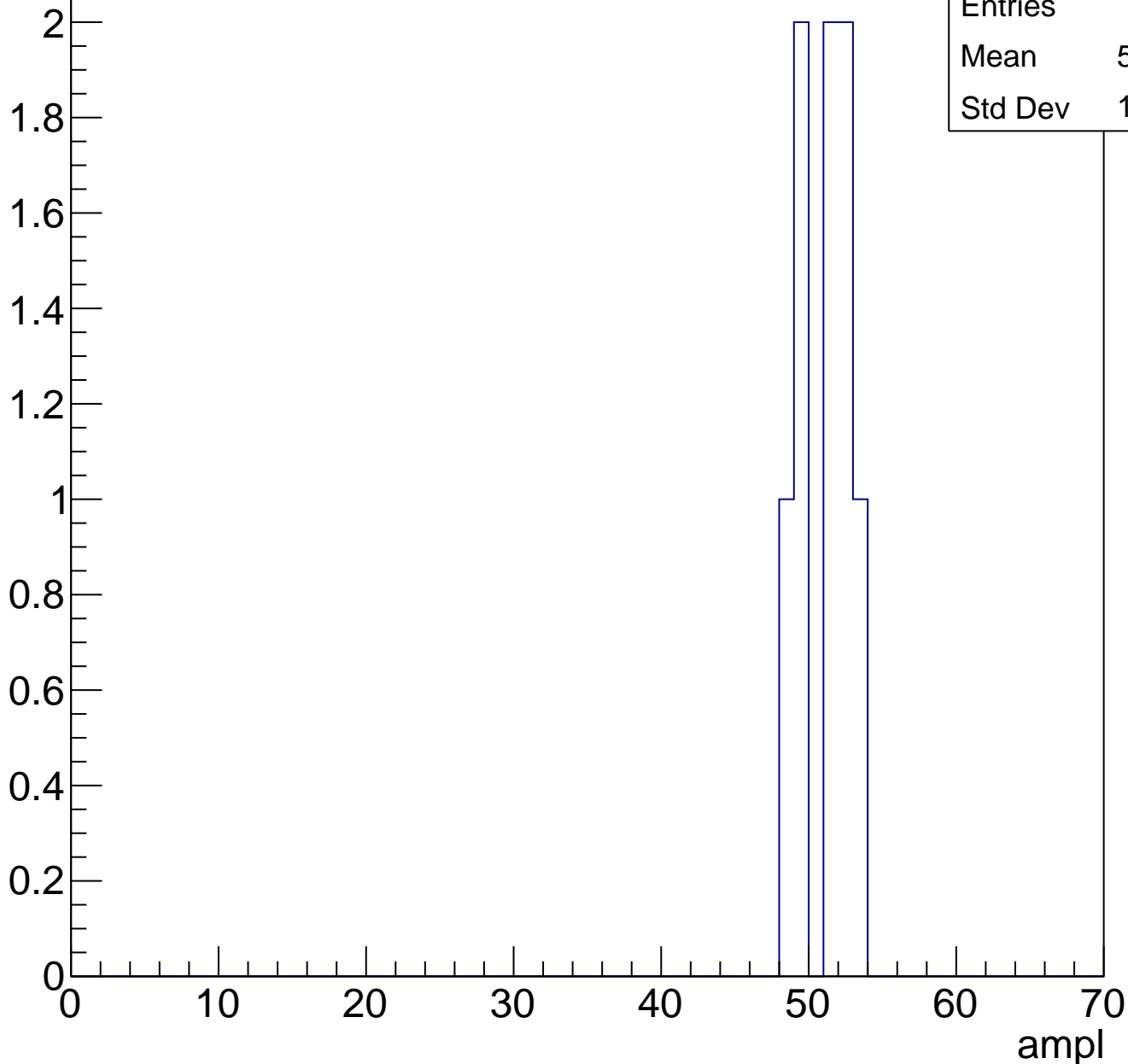
Entry



B0L100S, U12-ch20, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch20, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch20, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch20, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch20, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch21, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry

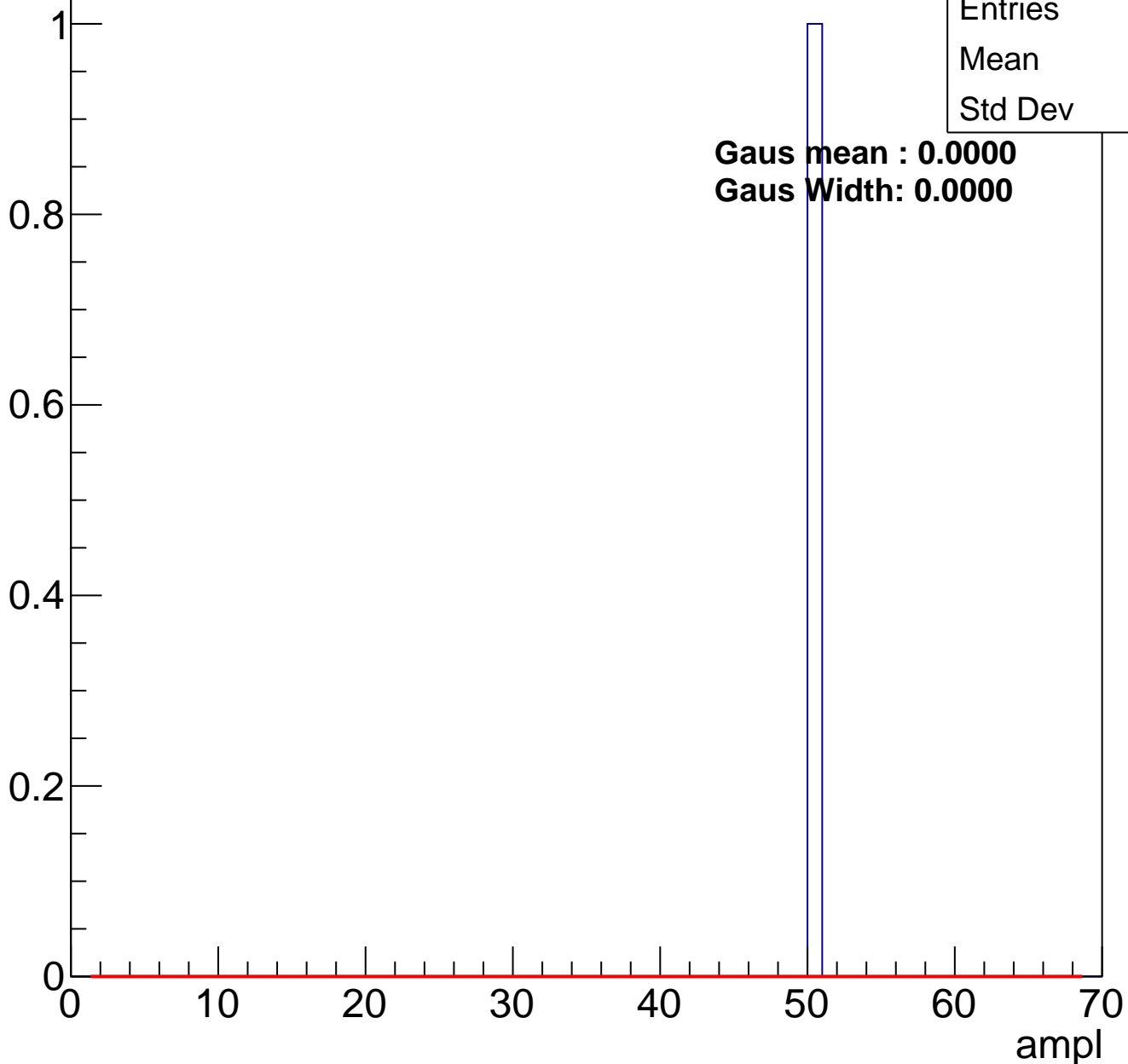


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch21, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	1
Mean	50
Std Dev	0

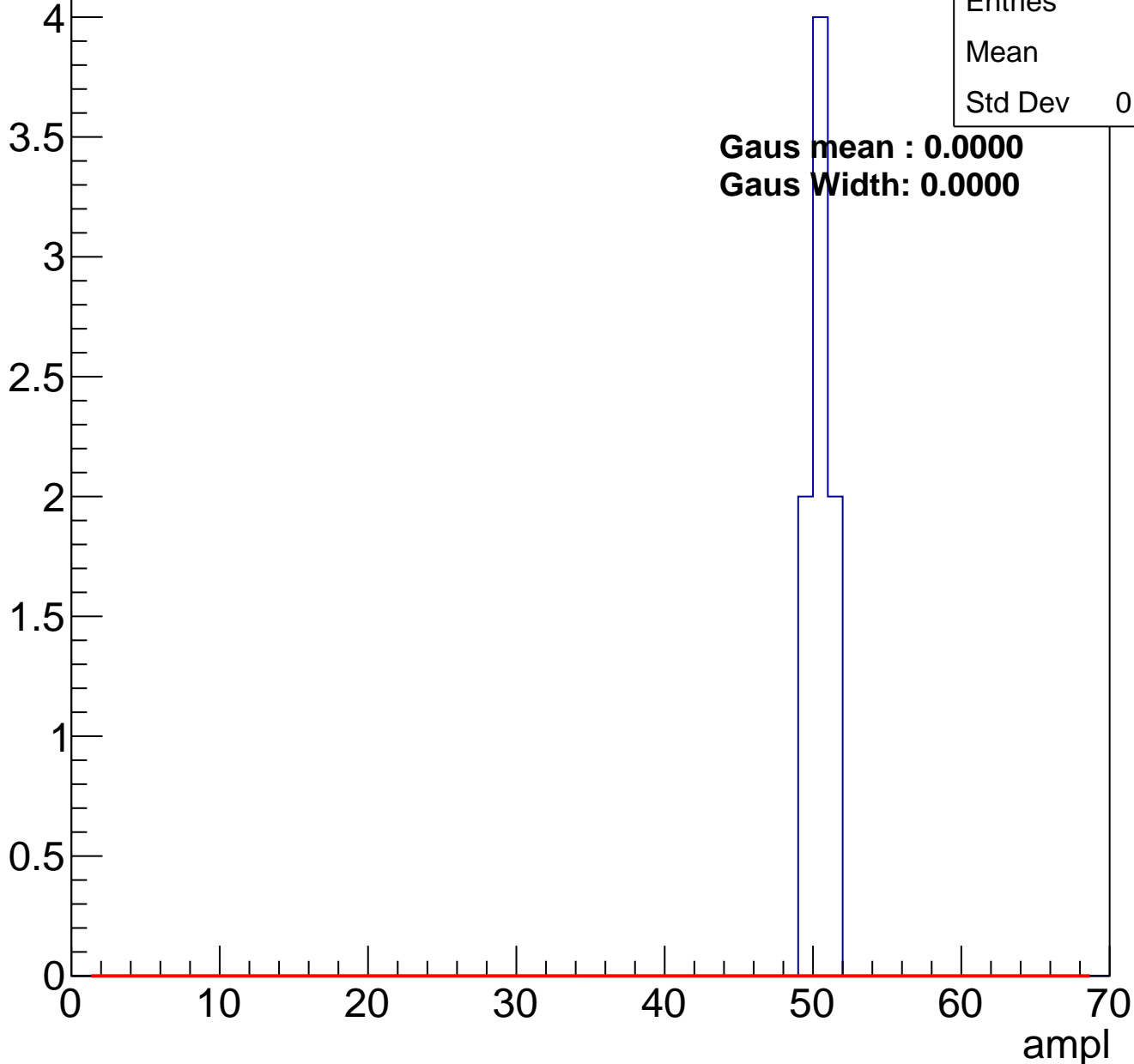
Gaus mean : 0.0000

Gaus Width: 0.0000

B0L100S, U12-ch21, adc2

calib_packv5_042523_0143.root, FC#6, port A1

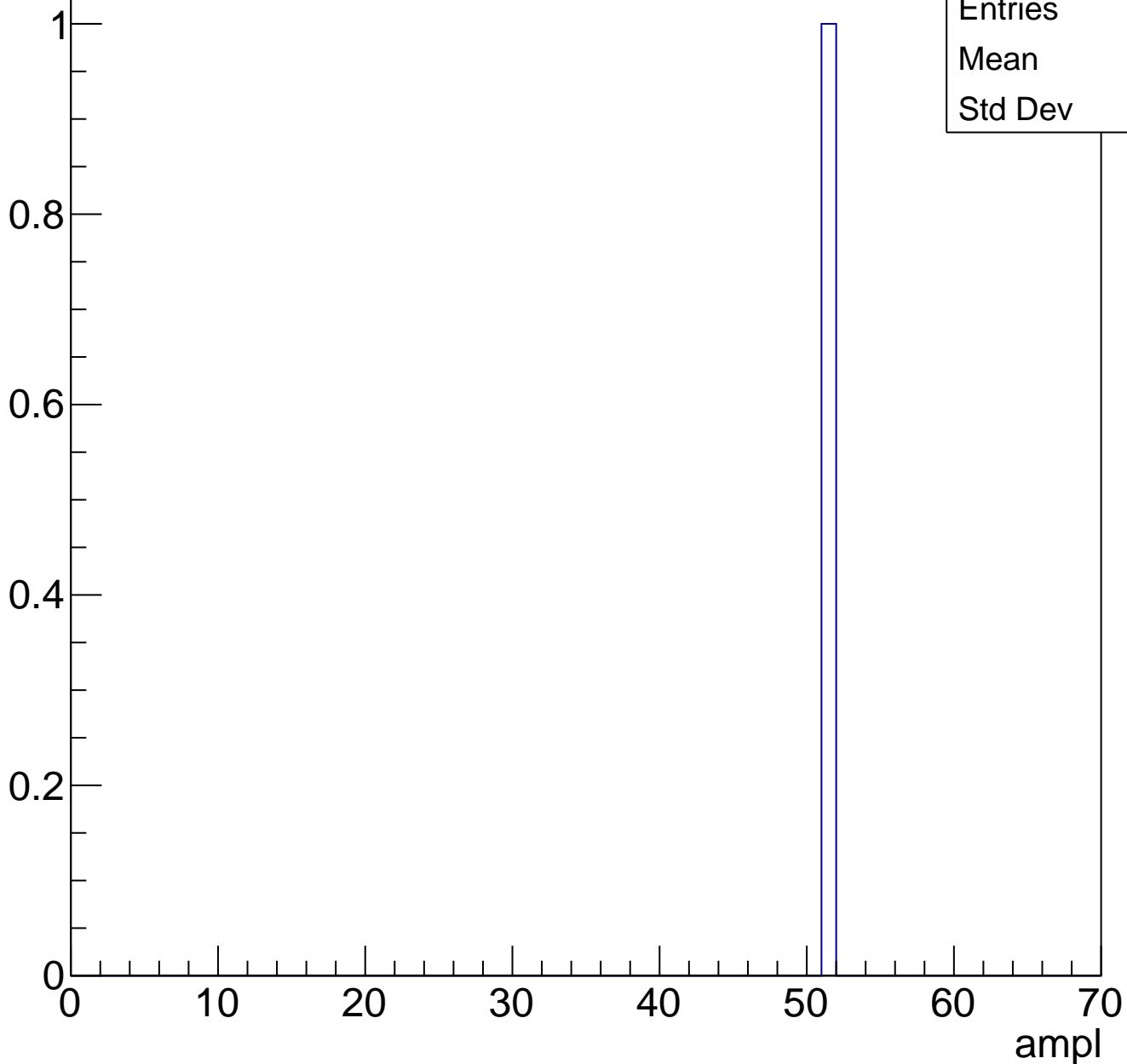
Entry



B0L100S, U12-ch21, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch21, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch21, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch21, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch21, adc7

calib_packv5_042523_0143.root, FC#6, port A1

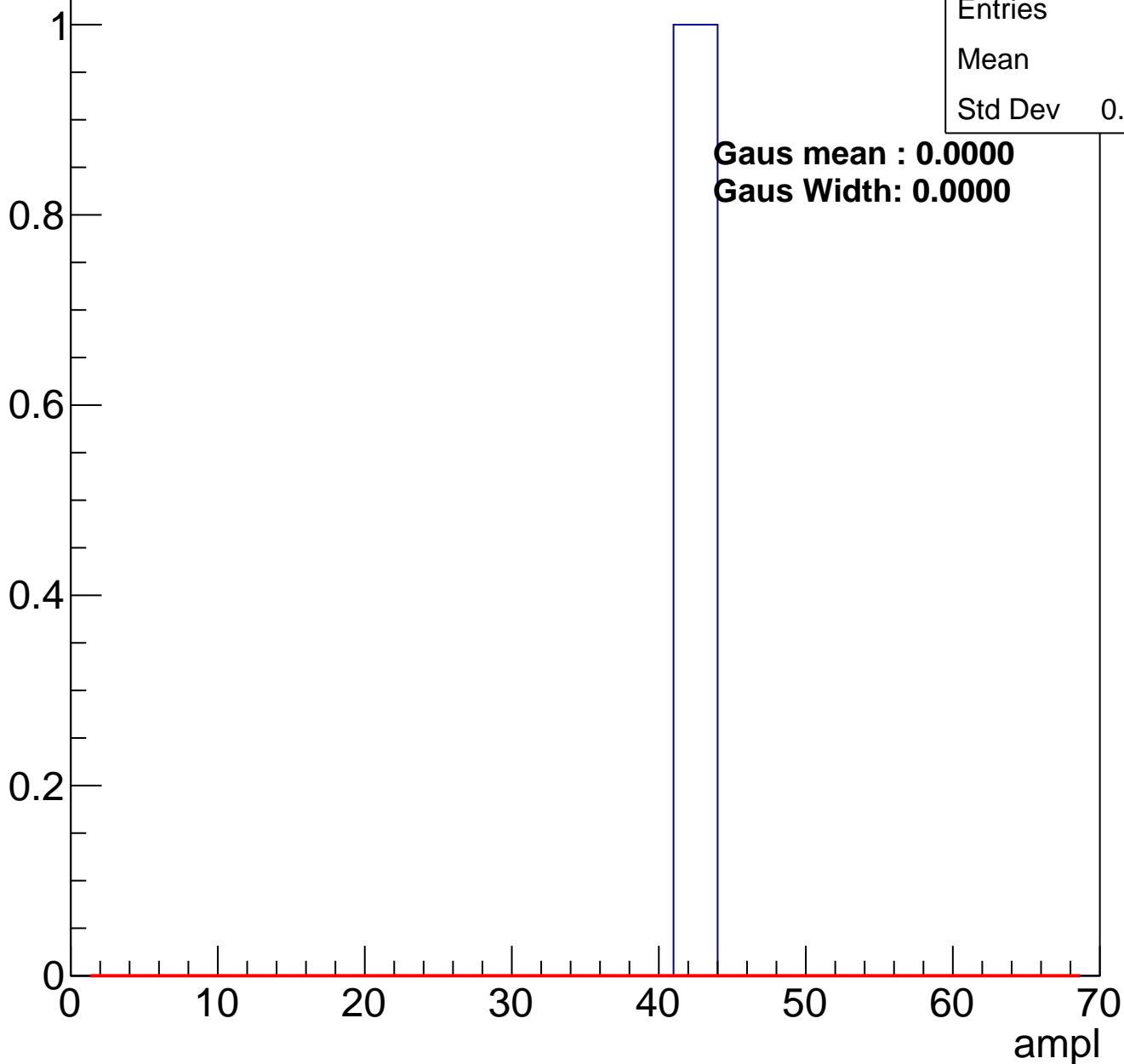
Entry



B0L100S, U12-ch22, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch22, adc1

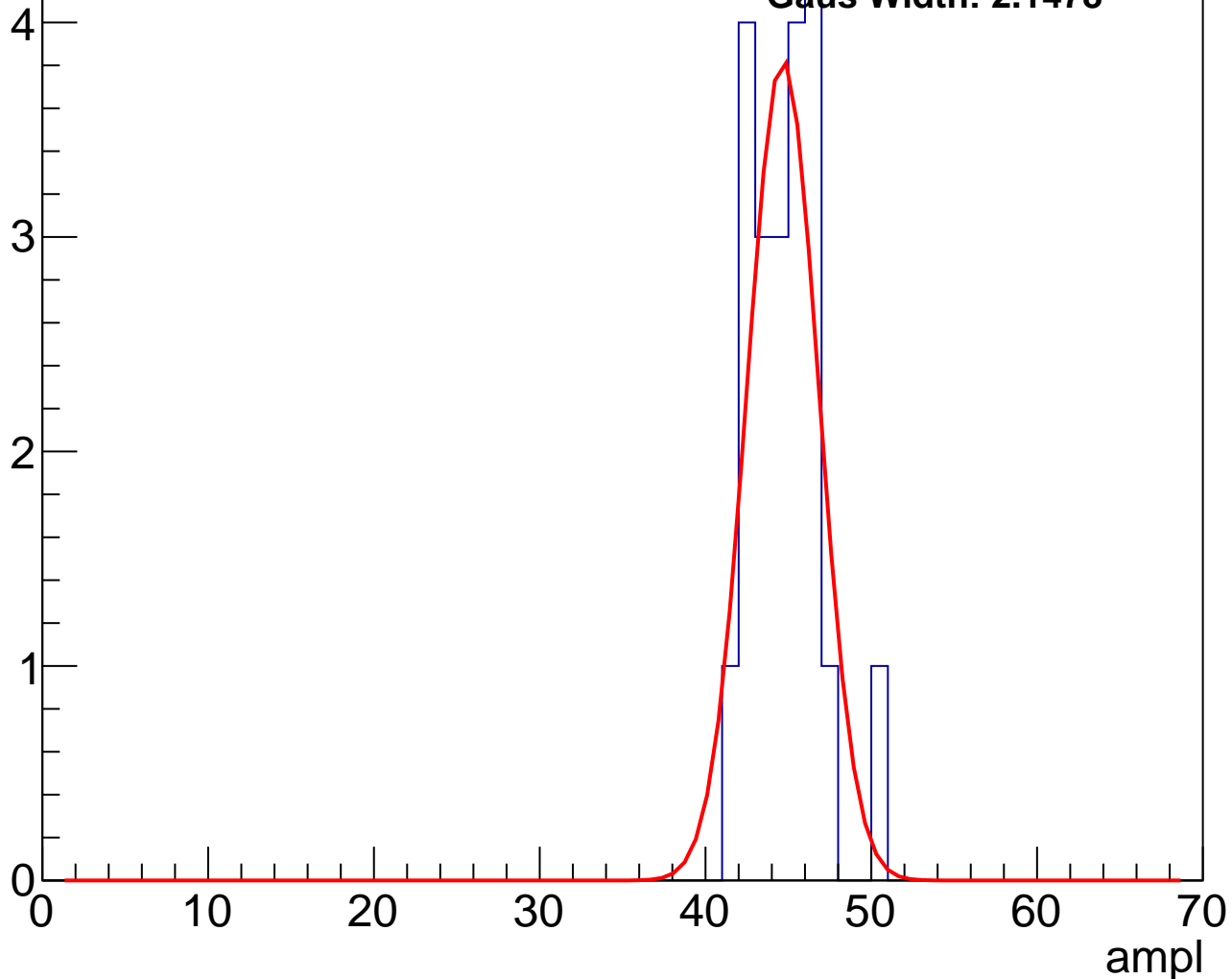
calib_packv5_042523_0143.root, FC#6, port A1

Entry

Entries	22
Mean	44.41
Std Dev	2.06

Gaus mean : 44.6677

Gaus Width: 2.1478



B0L100S, U12-ch22, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

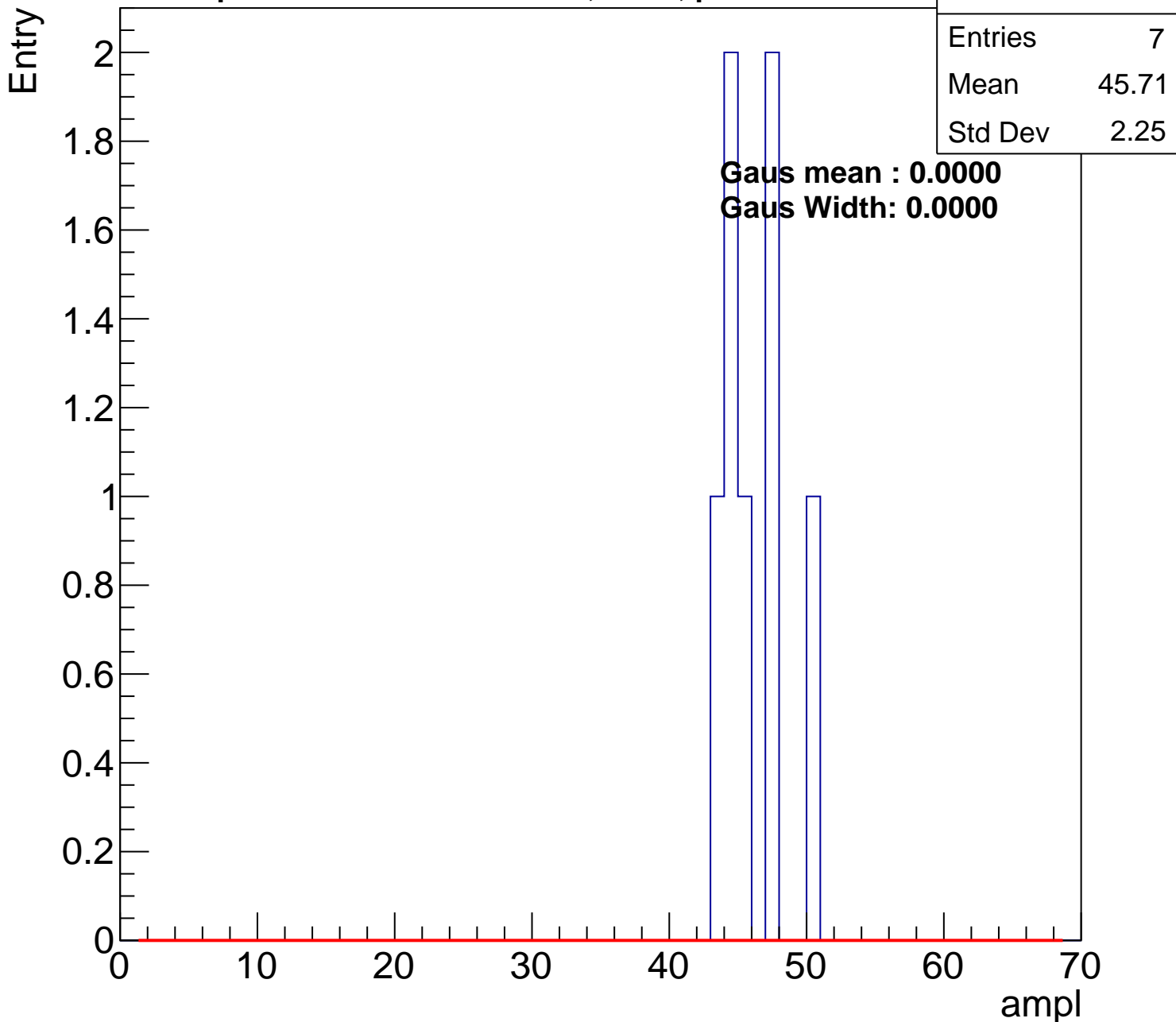
Entries	7
Mean	45.71
Std Dev	2.25

Gaus mean : 0.0000

Gaus Width: 0.0000

0 10 20 30 40 50 60 70

ampl



B0L100S, U12-ch22, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch22, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch22, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch22, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch22, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch23, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch23, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

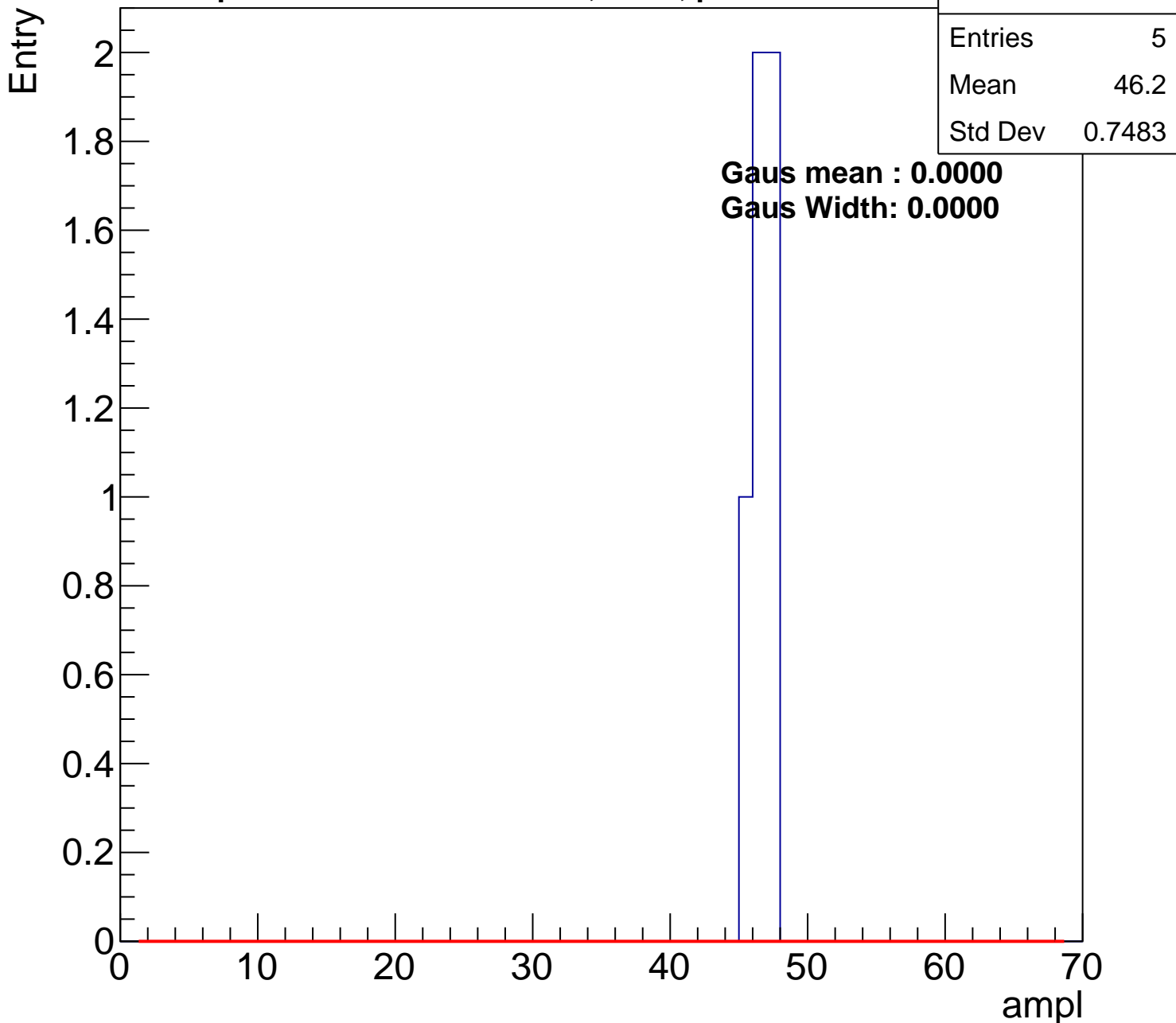
Entries	5
Mean	46.2
Std Dev	0.7483

Gaus mean : 0.0000

Gaus Width: 0.0000

0 10 20 30 40 50 60 70

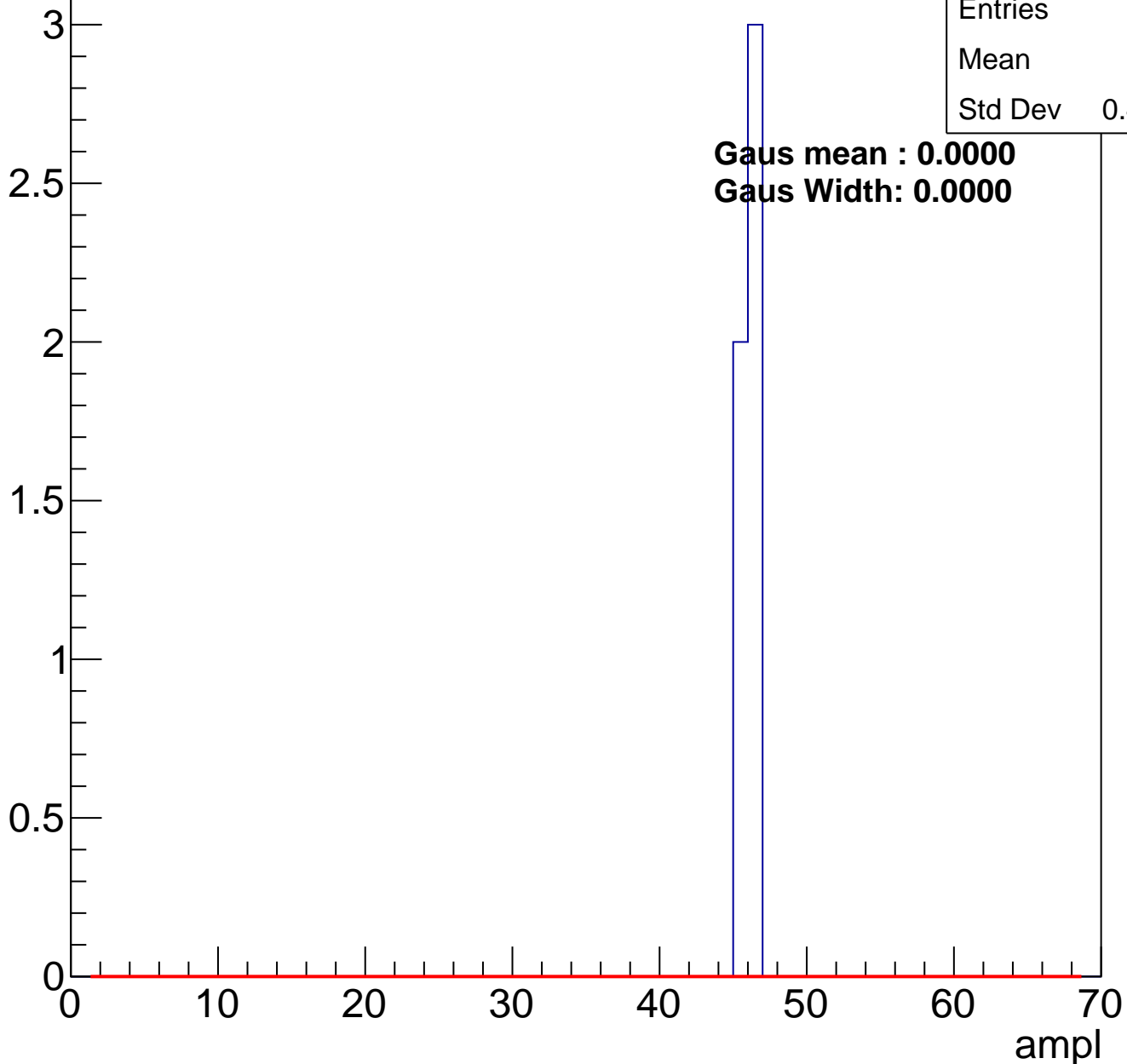
ampl



B0L100S, U12-ch23, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch23, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch23, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch23, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch23, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch23, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry

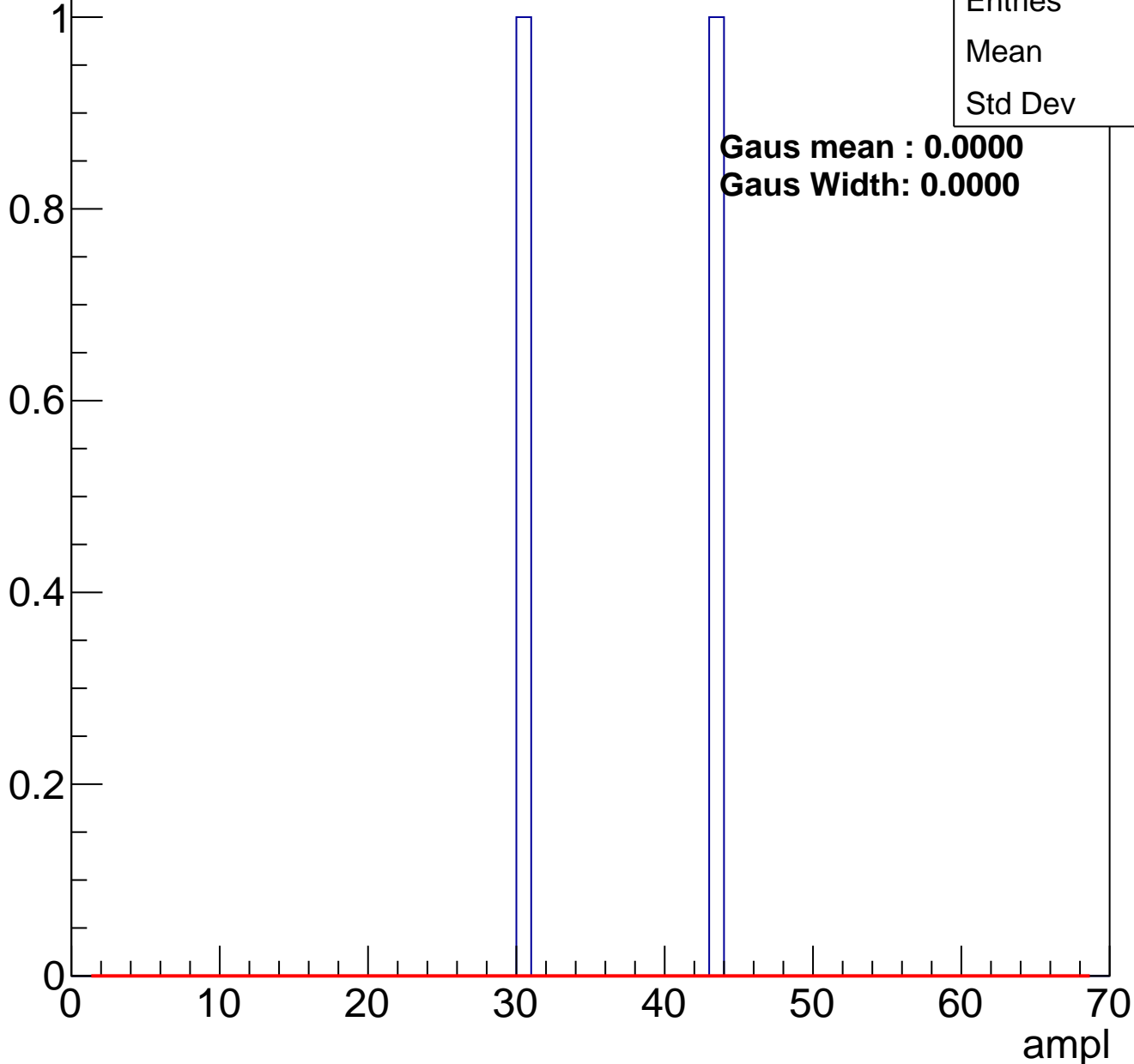


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch24, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry

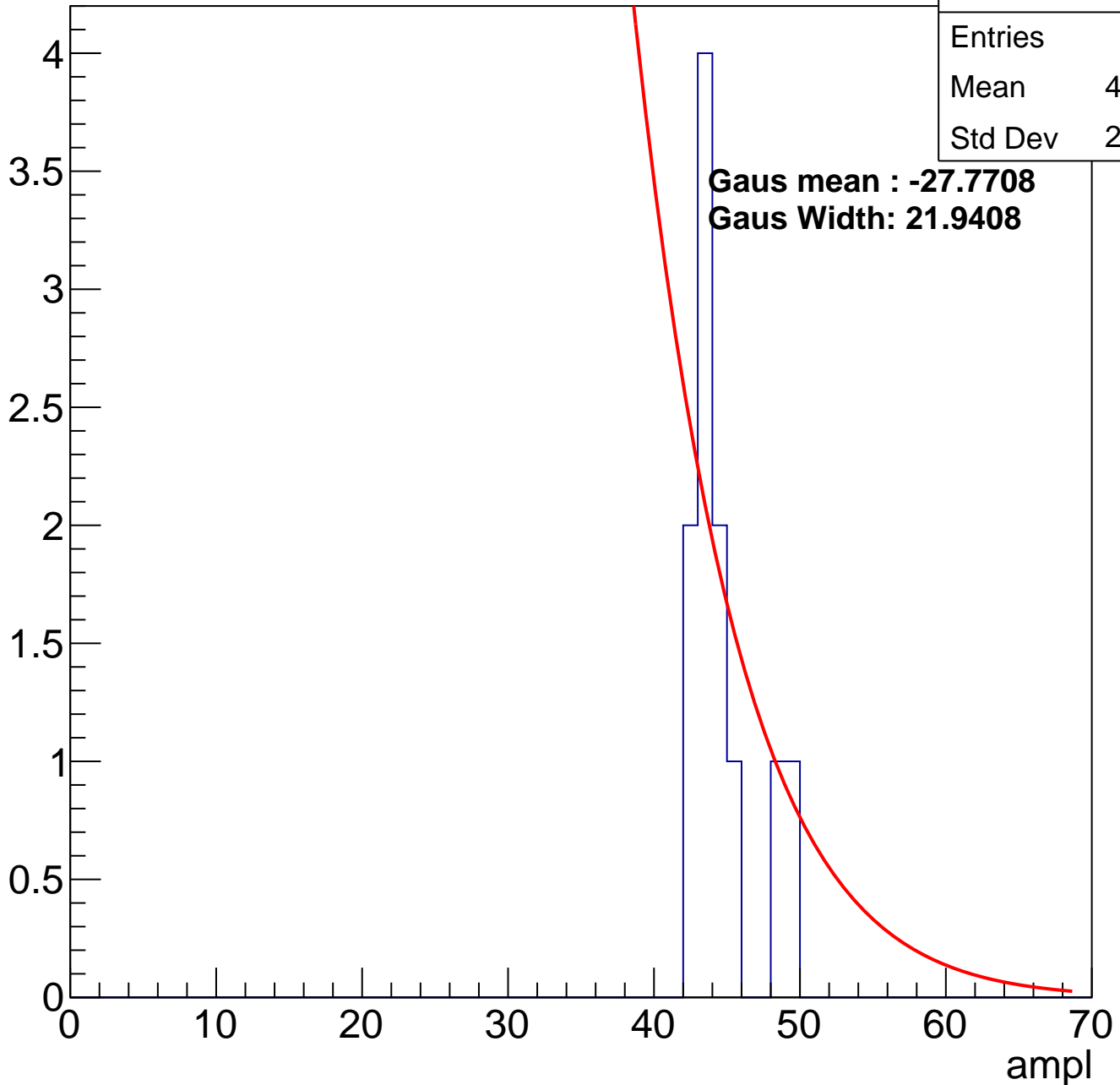


Entries	2
Mean	36.5
Std Dev	6.5

B0L100S, U12-ch24, adc1

calib_packv5_042523_0143.root, FC#6, port A1

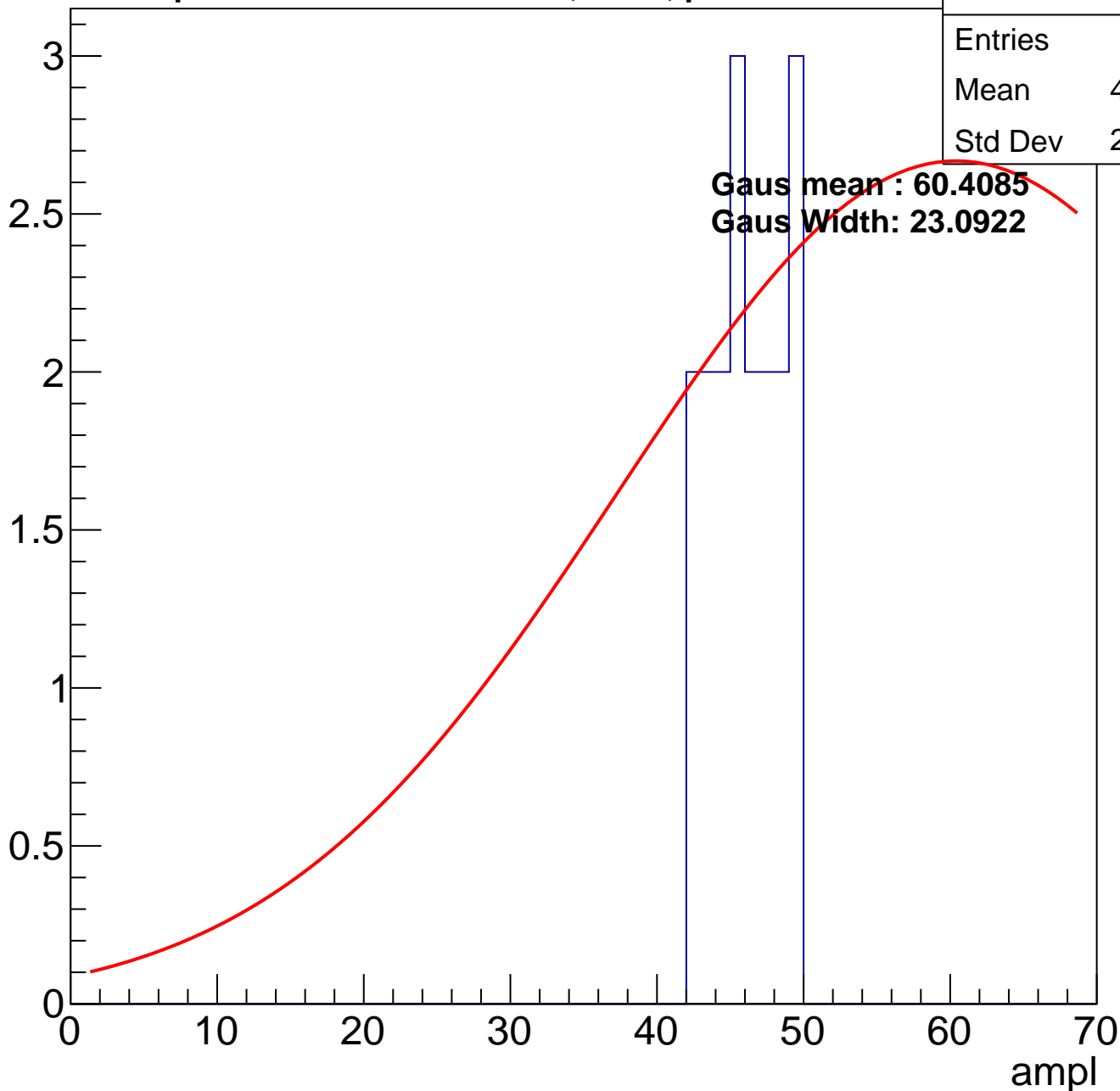
Entry



B0L100S, U12-ch24, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch24, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	5
Mean	48
Std Dev	1.673

ampl

0 10 20 30 40 50 60 70



B0L100S, U12-ch24, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch24, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch24, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch24, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch25, adc0

calib_packv5_042523_0143.root, FC#6, port A1

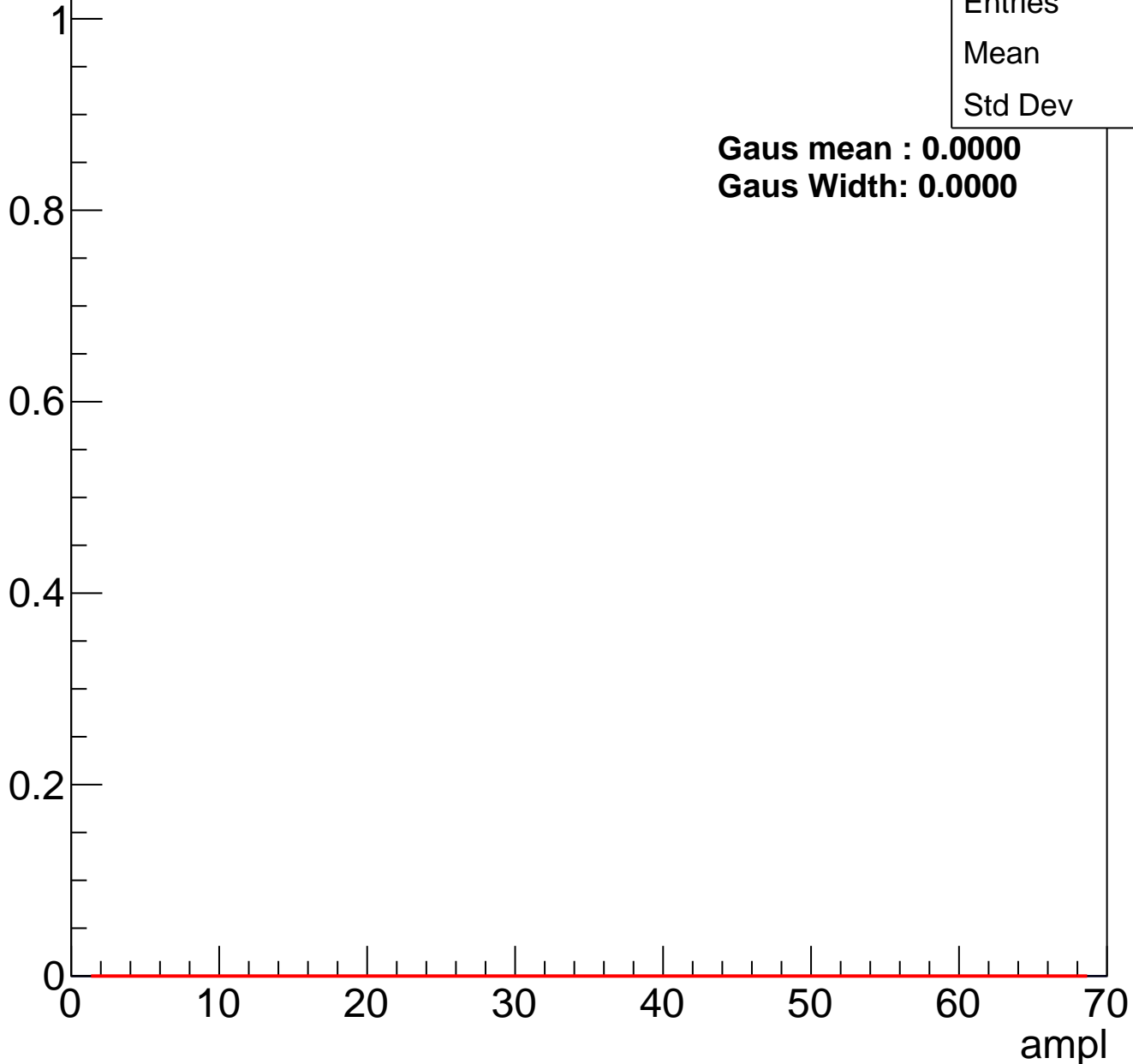
Entry



B0L100S, U12-ch25, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch25, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch25, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch25, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch25, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch25, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch25, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch26, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch26, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch26, adc2

calib_packv5_042523_0143.root, FC#6, port A1

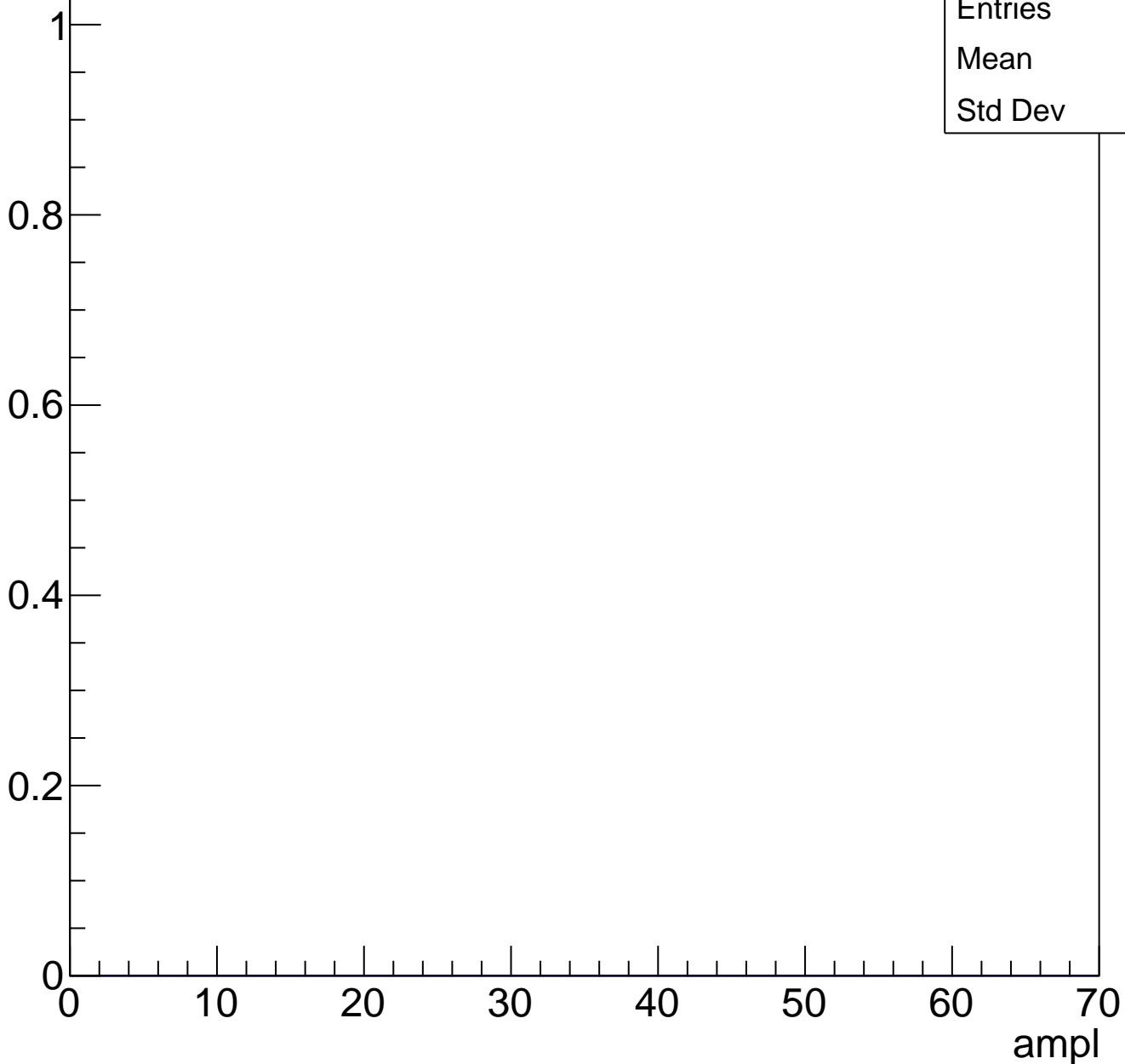
Entry



B0L100S, U12-ch26, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch26, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

0

Mean

0

Std Dev

0

B0L100S, U12-ch26, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch26, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch26, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch27, adc0

calib_packv5_042523_0143.root, FC#6, port A1

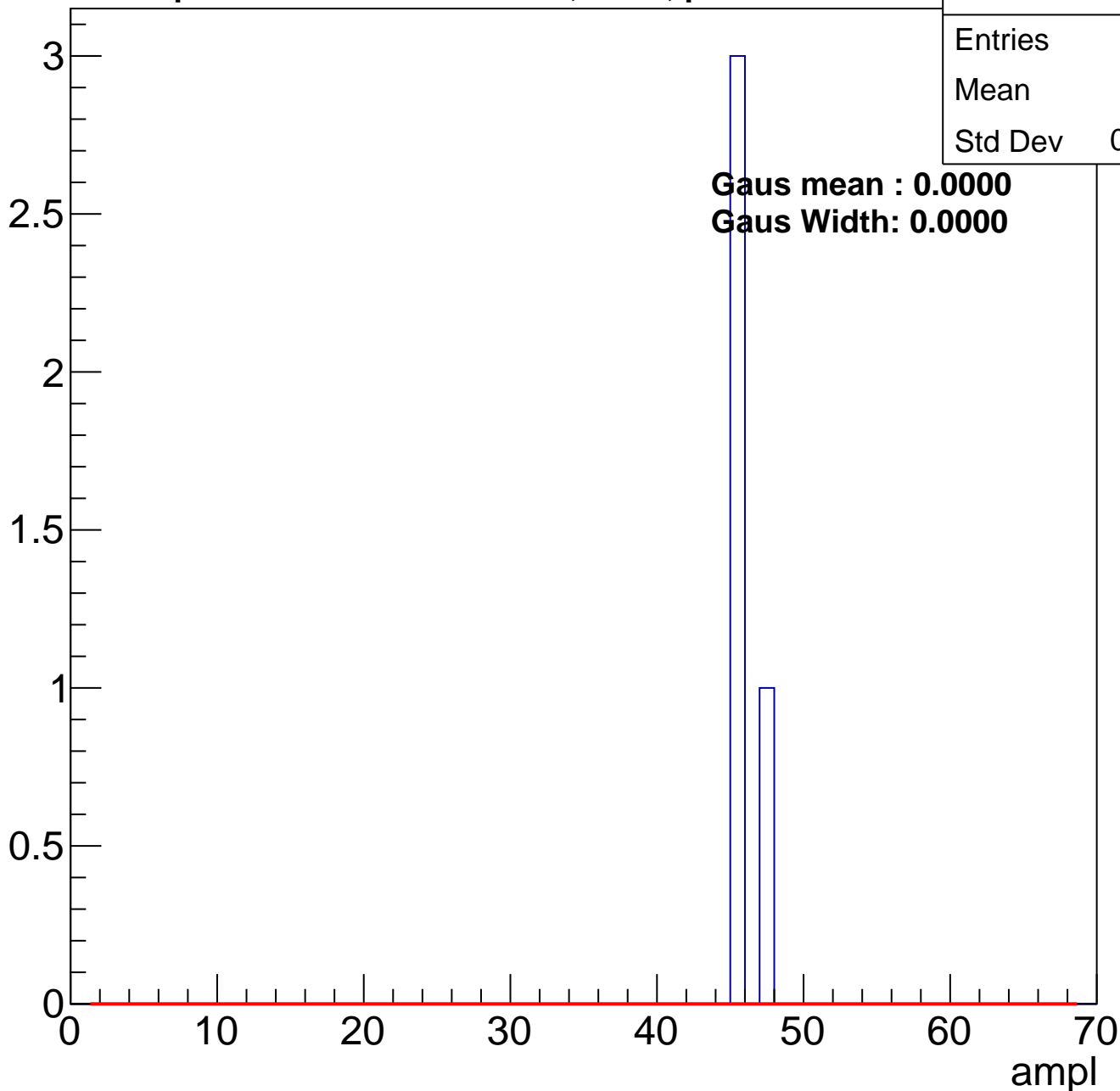
Entry



B0L100S, U12-ch27, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry

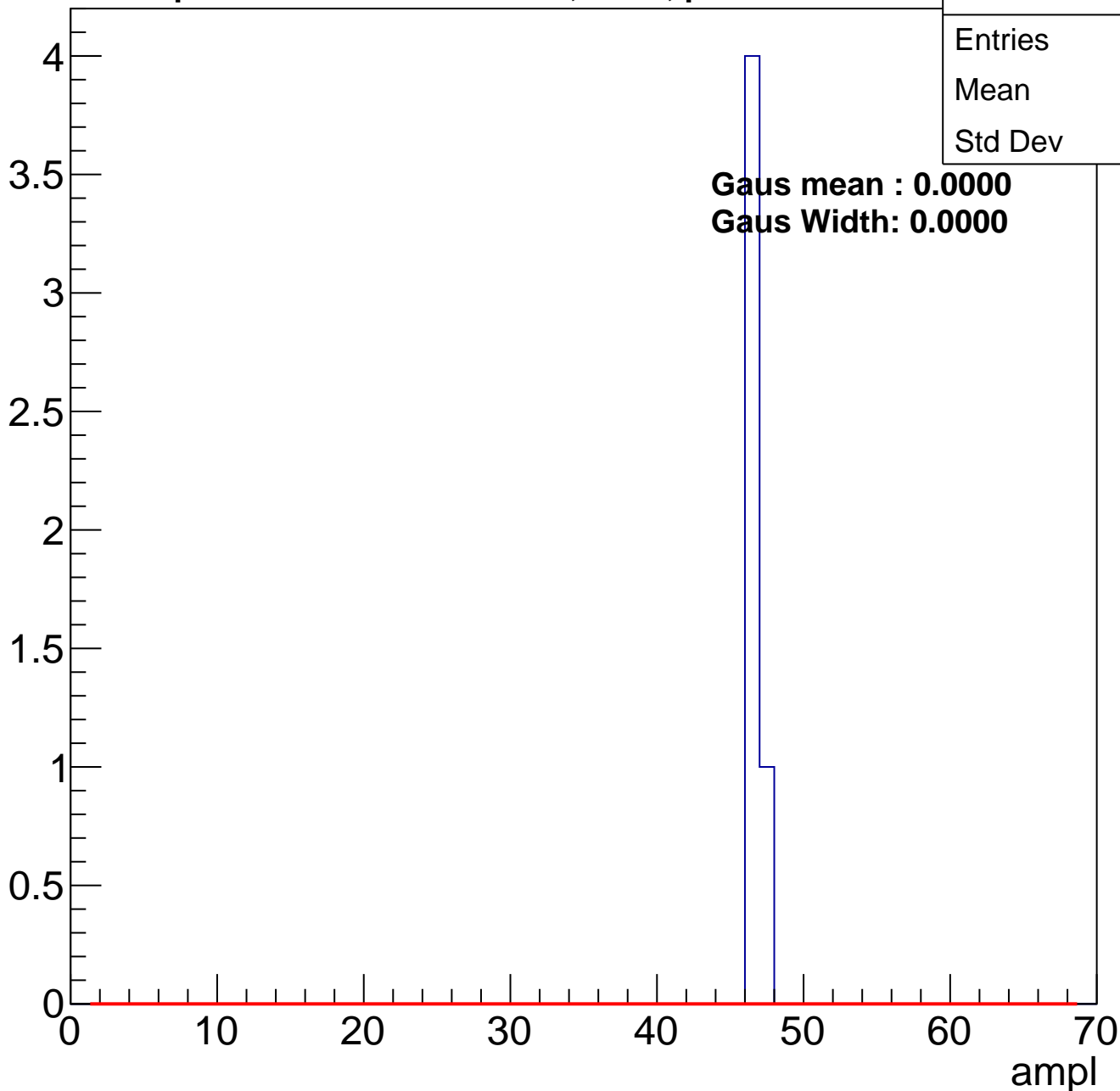


Entries	4
Mean	45.5
Std Dev	0.866

B0L100S, U12-ch27, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

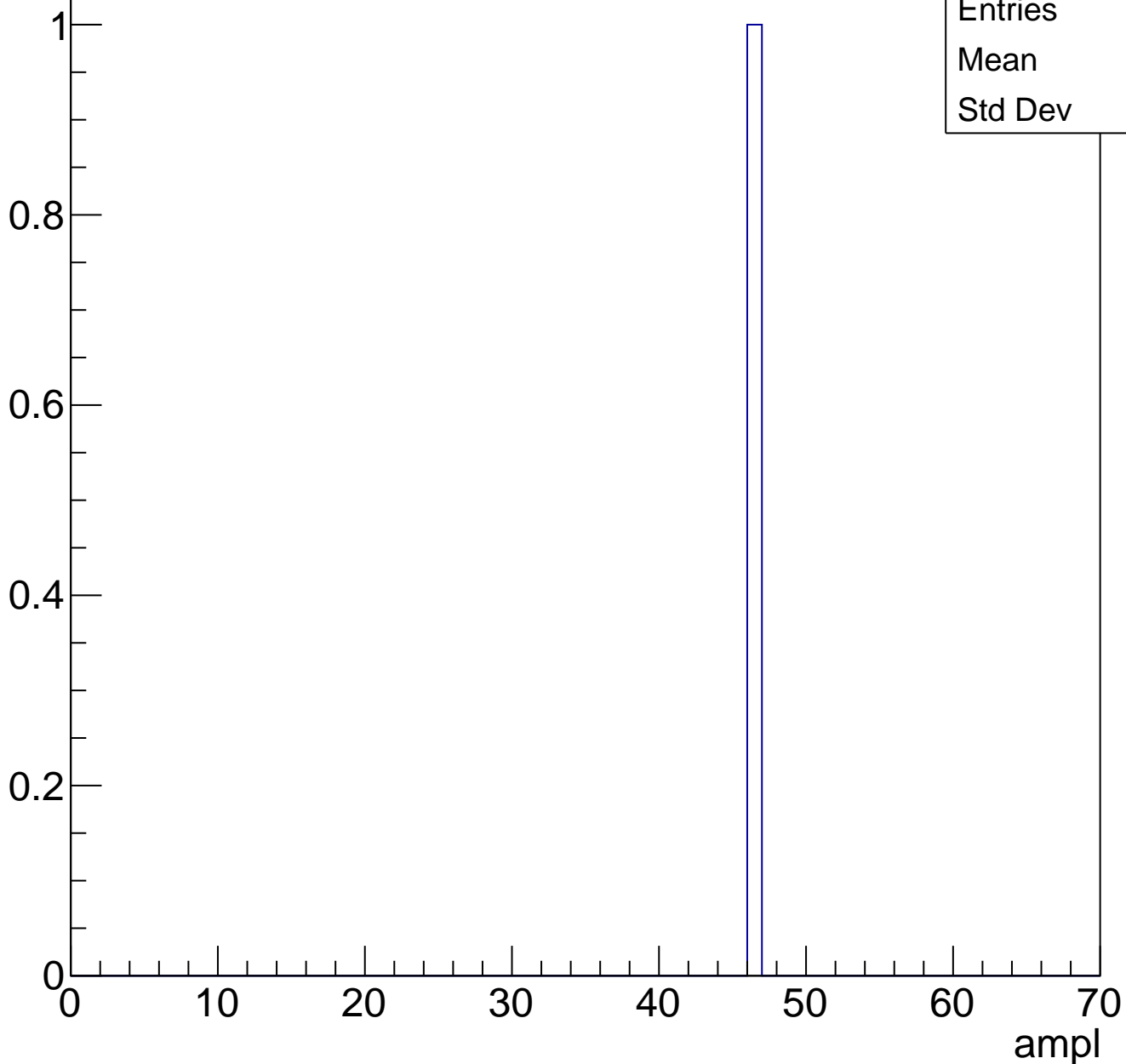


Entries	5
Mean	46.2
Std Dev	0.4

B0L100S, U12-ch27, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch27, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch27, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch27, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch27, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch28, adc0

calib_packv5_042523_0143.root, FC#6, port A1

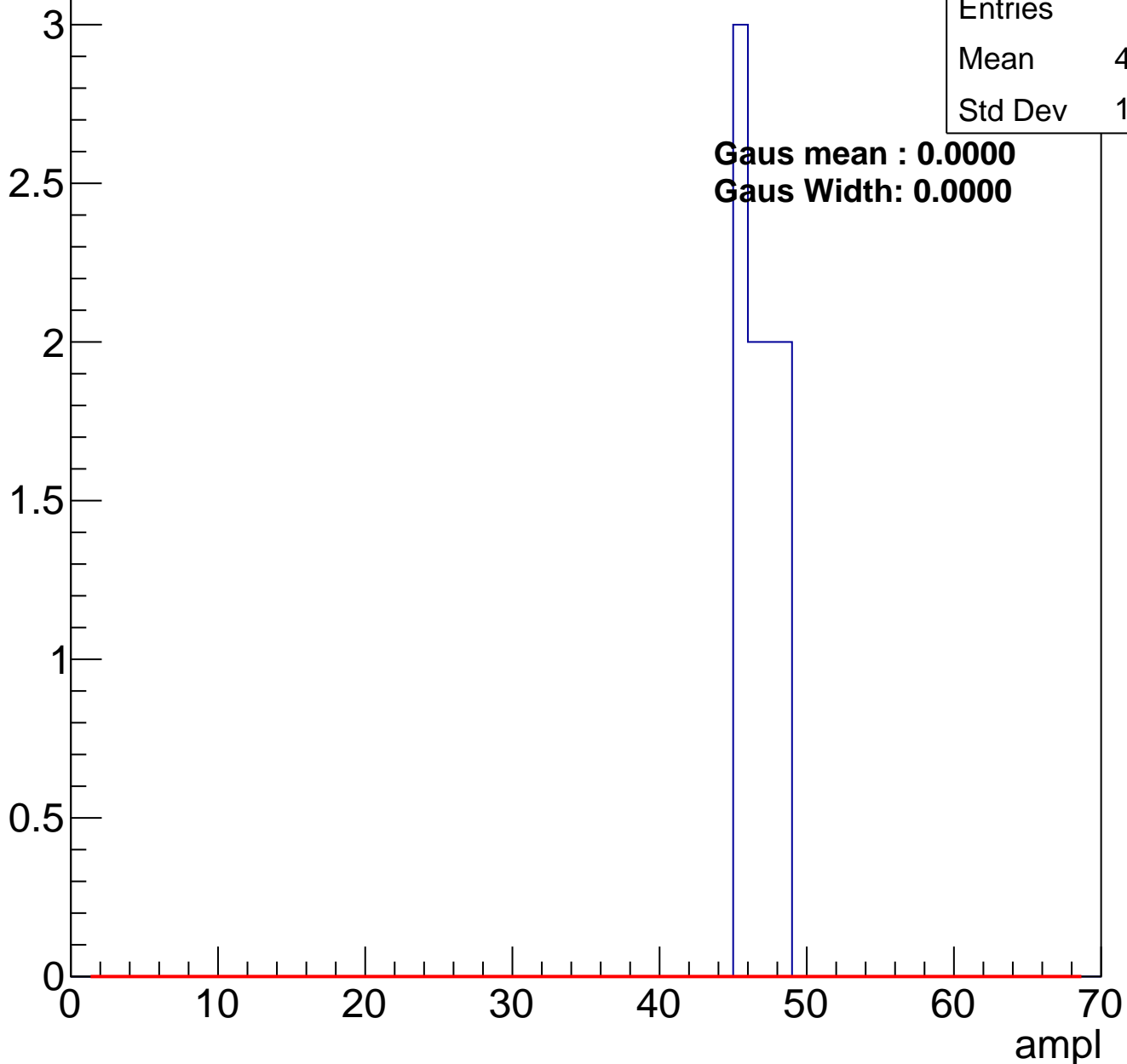
Entry



B0L100S, U12-ch28, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry

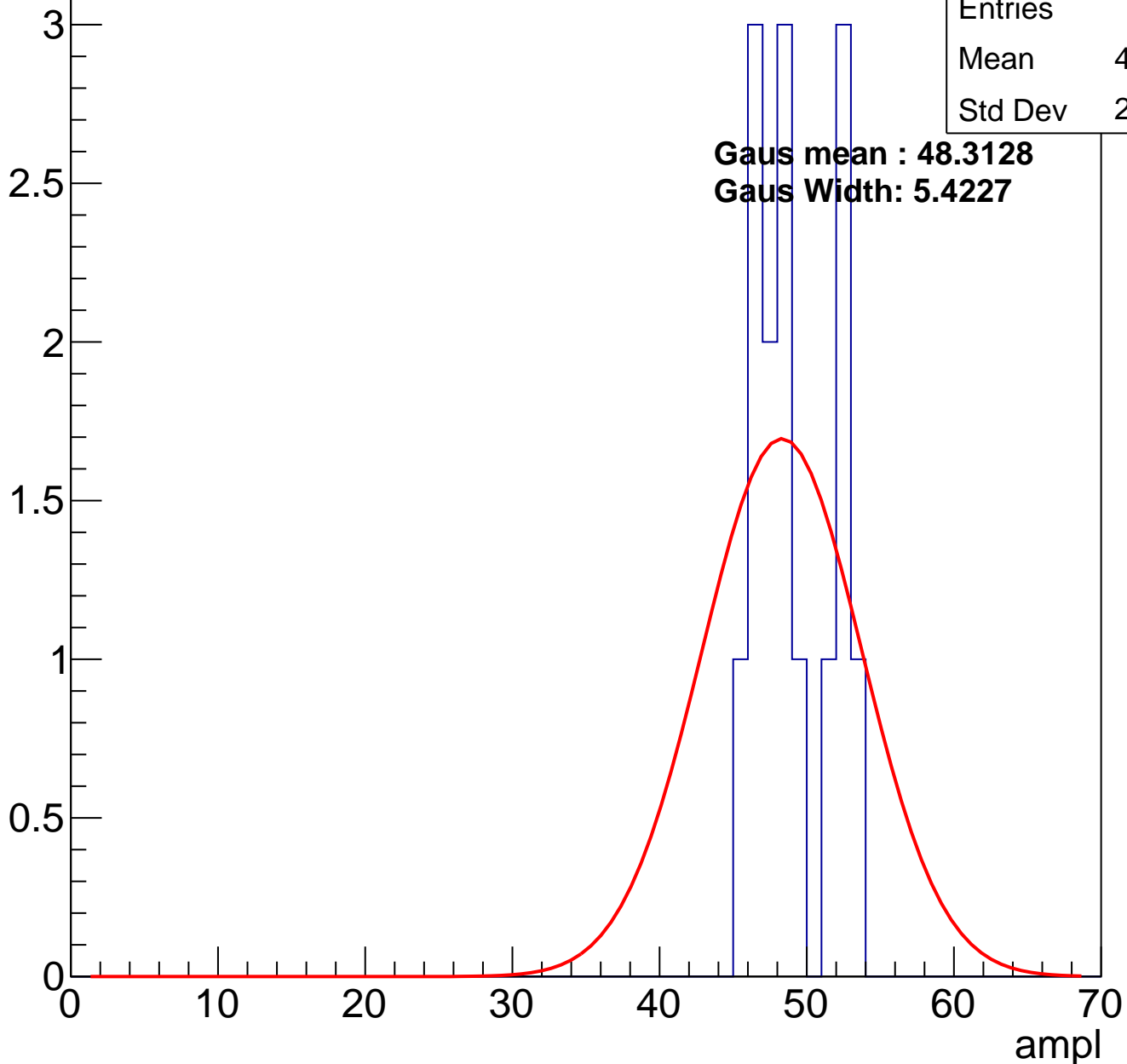


Entries	9
Mean	46.33
Std Dev	1.155

B0L100S, U12-ch28, adc2

calib_packv5_042523_0143.root, FC#6, port A1

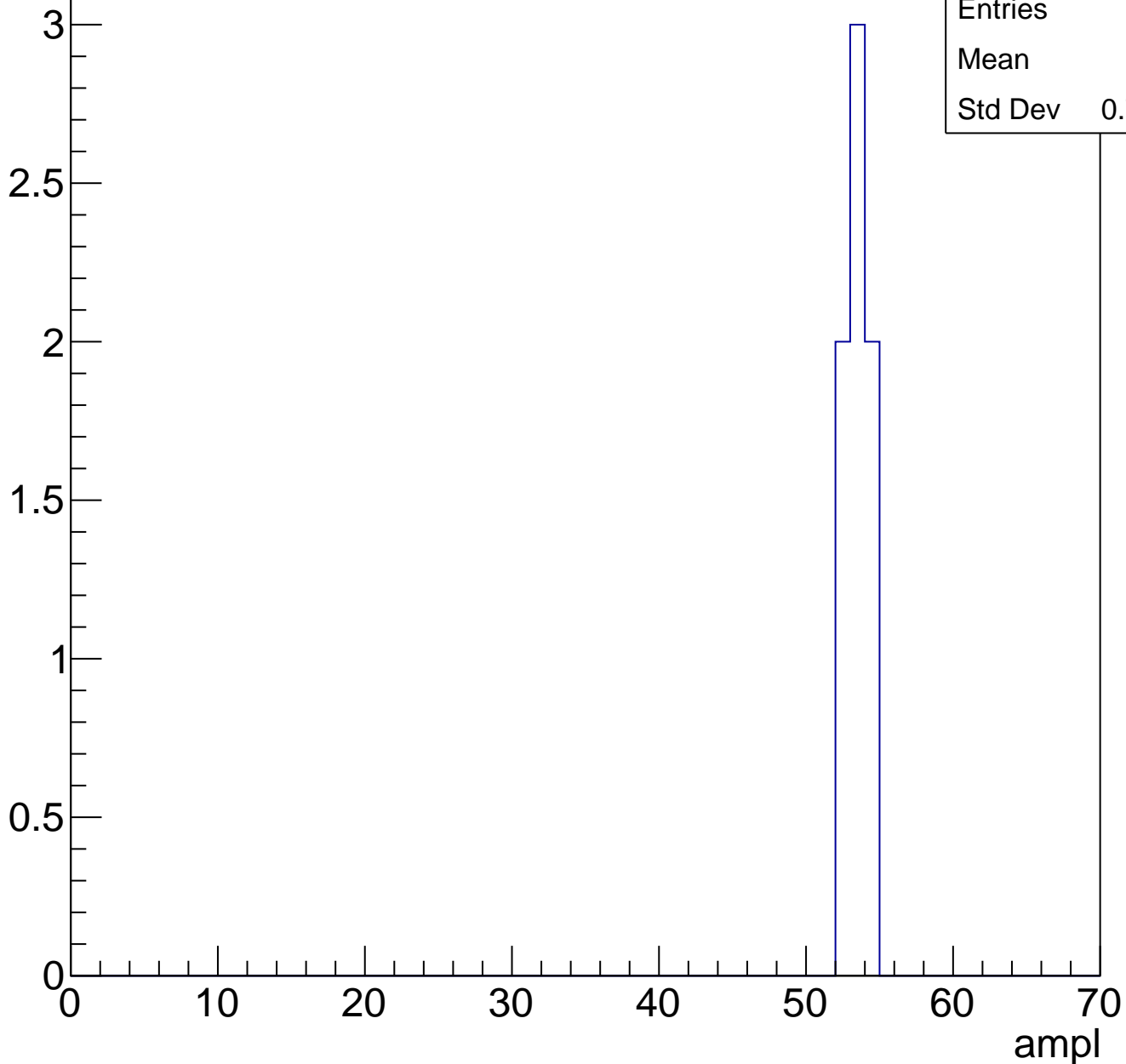
Entry



B0L100S, U12-ch28, adc3

calib_packv5_042523_0143.root, FC#6, port A1

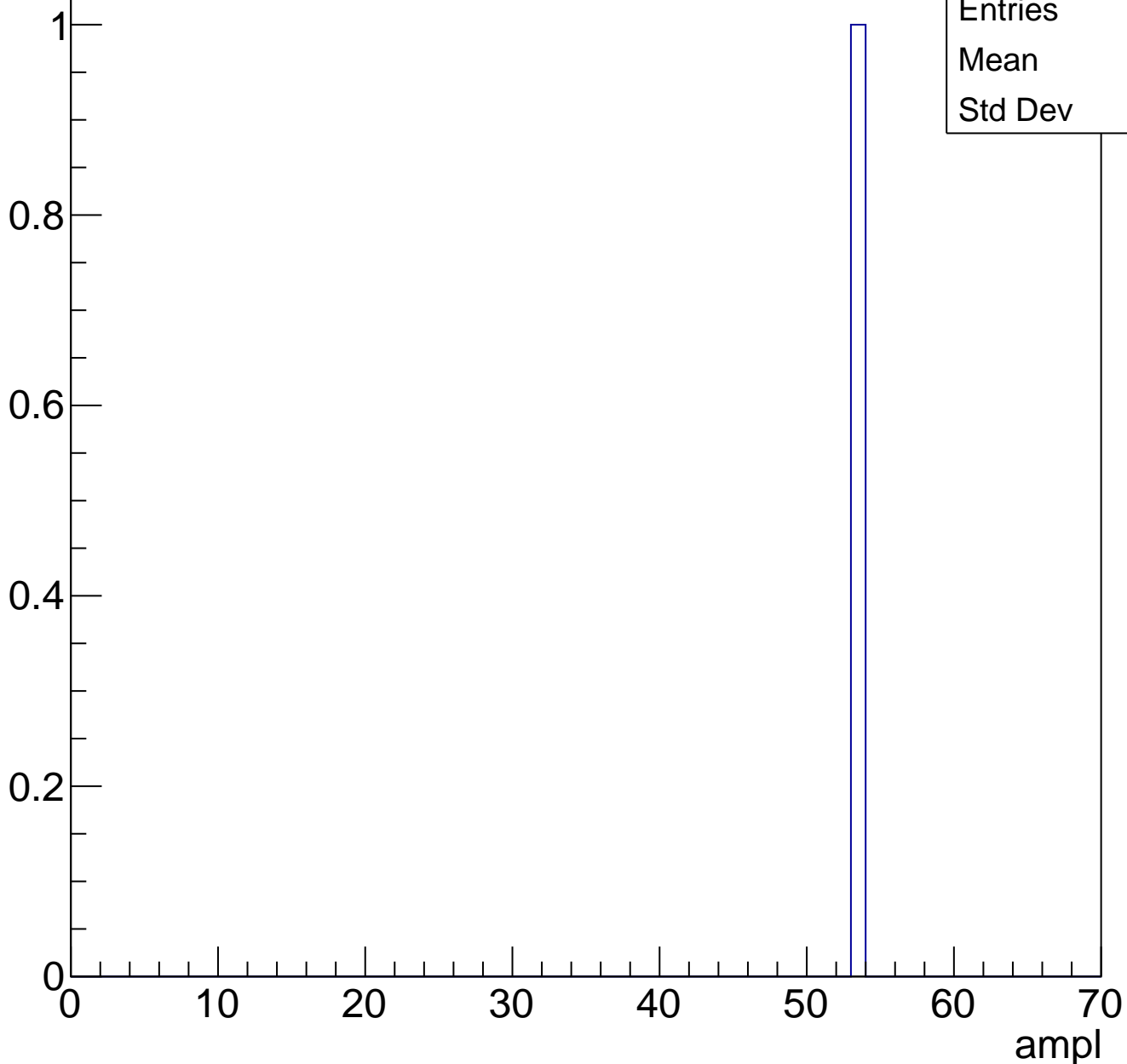
Entry



B0L100S, U12-ch28, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch28, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch28, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch28, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch29, adc0

calib_packv5_042523_0143.root, FC#6, port A1

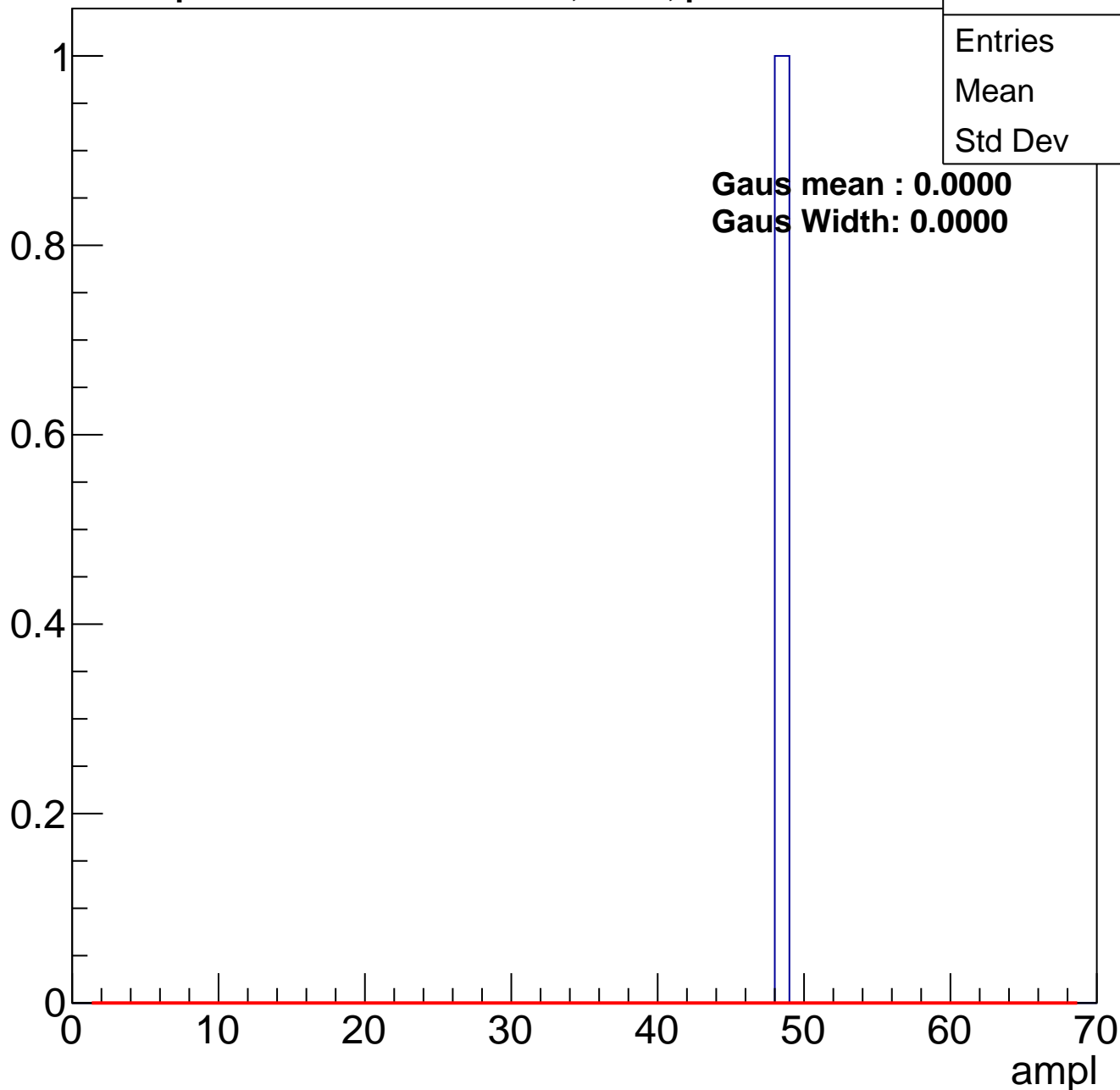
Entry



B0L100S, U12-ch29, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry

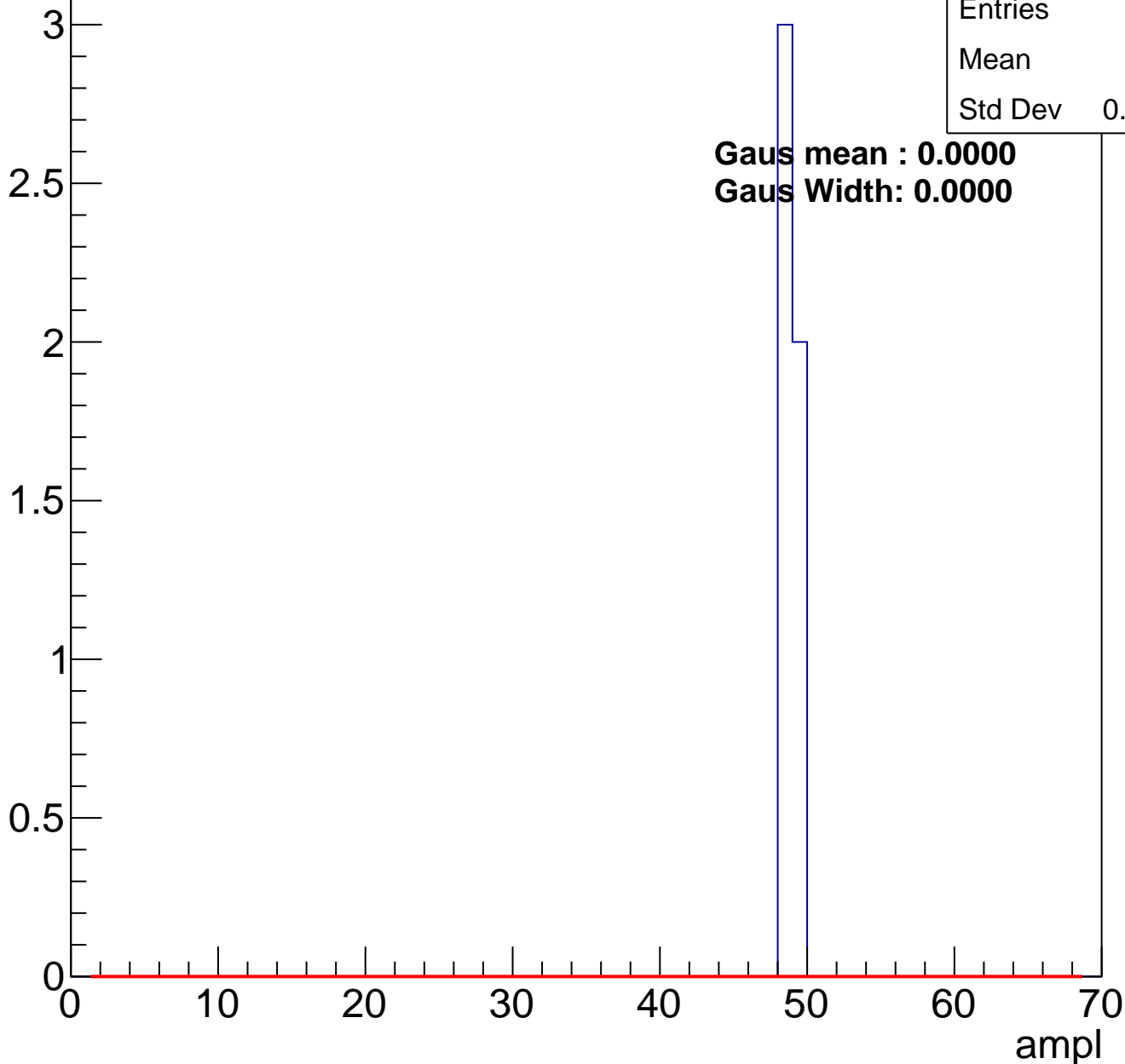


Entries	1
Mean	48
Std Dev	0

B0L100S, U12-ch29, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch29, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch29, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch29, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch29, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch29, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch30, adc0

calib_packv5_042523_0143.root, FC#6, port A1

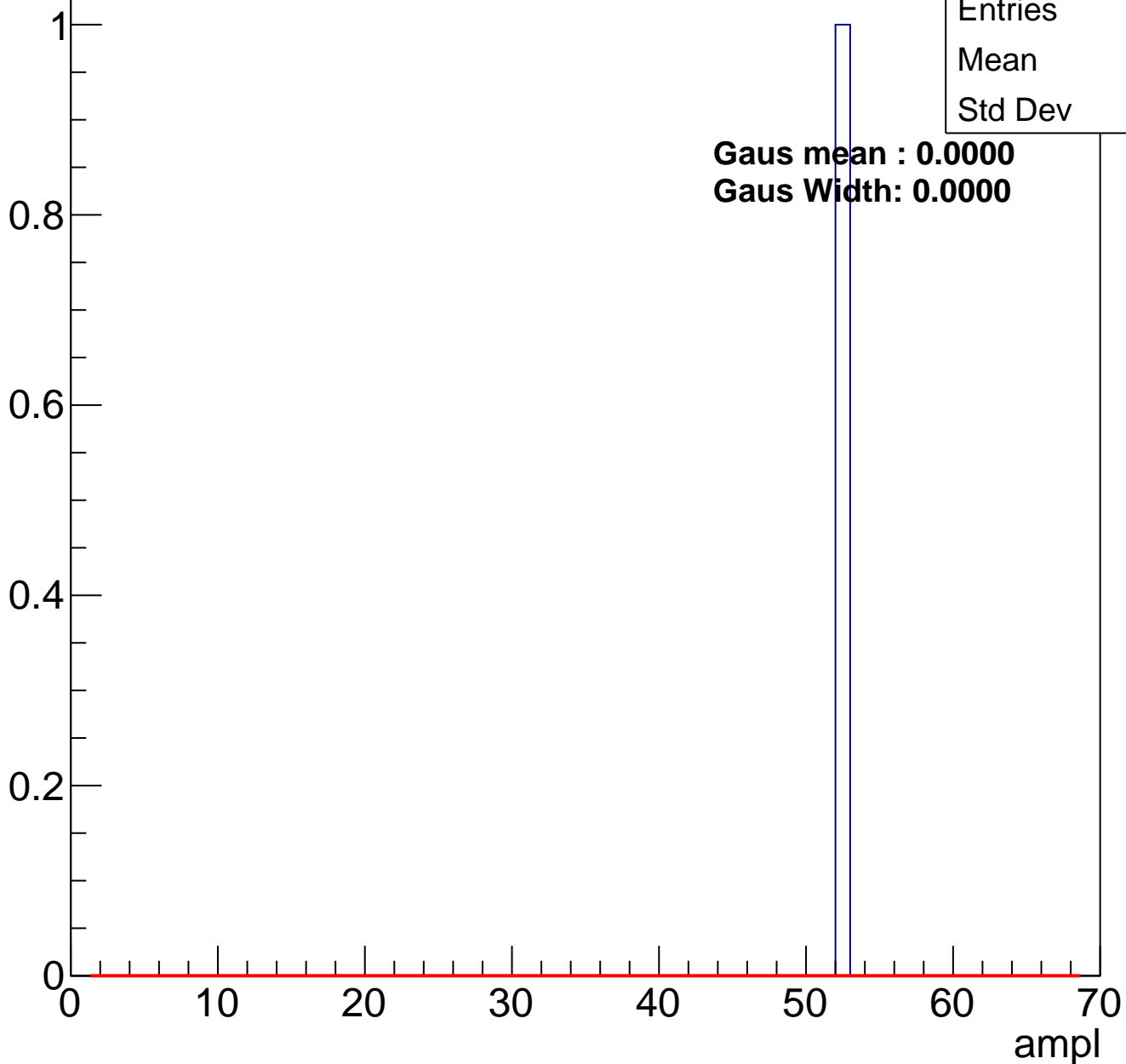
Entry



B0L100S, U12-ch30, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch30, adc2

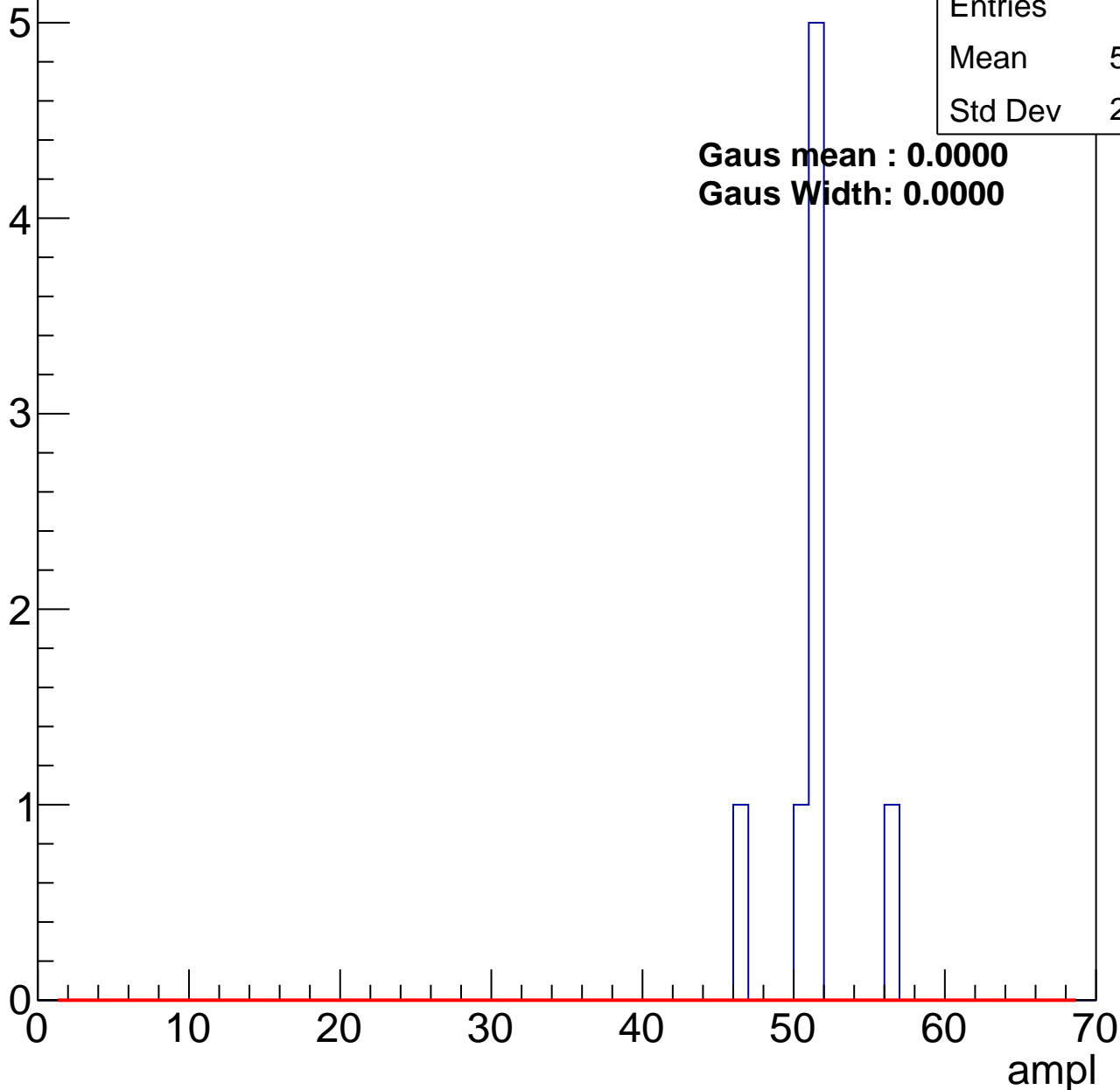
calib_packv5_042523_0143.root, FC#6, port A1

Entry

Entries	8
Mean	50.88
Std Dev	2.522

Gaus mean : 0.0000

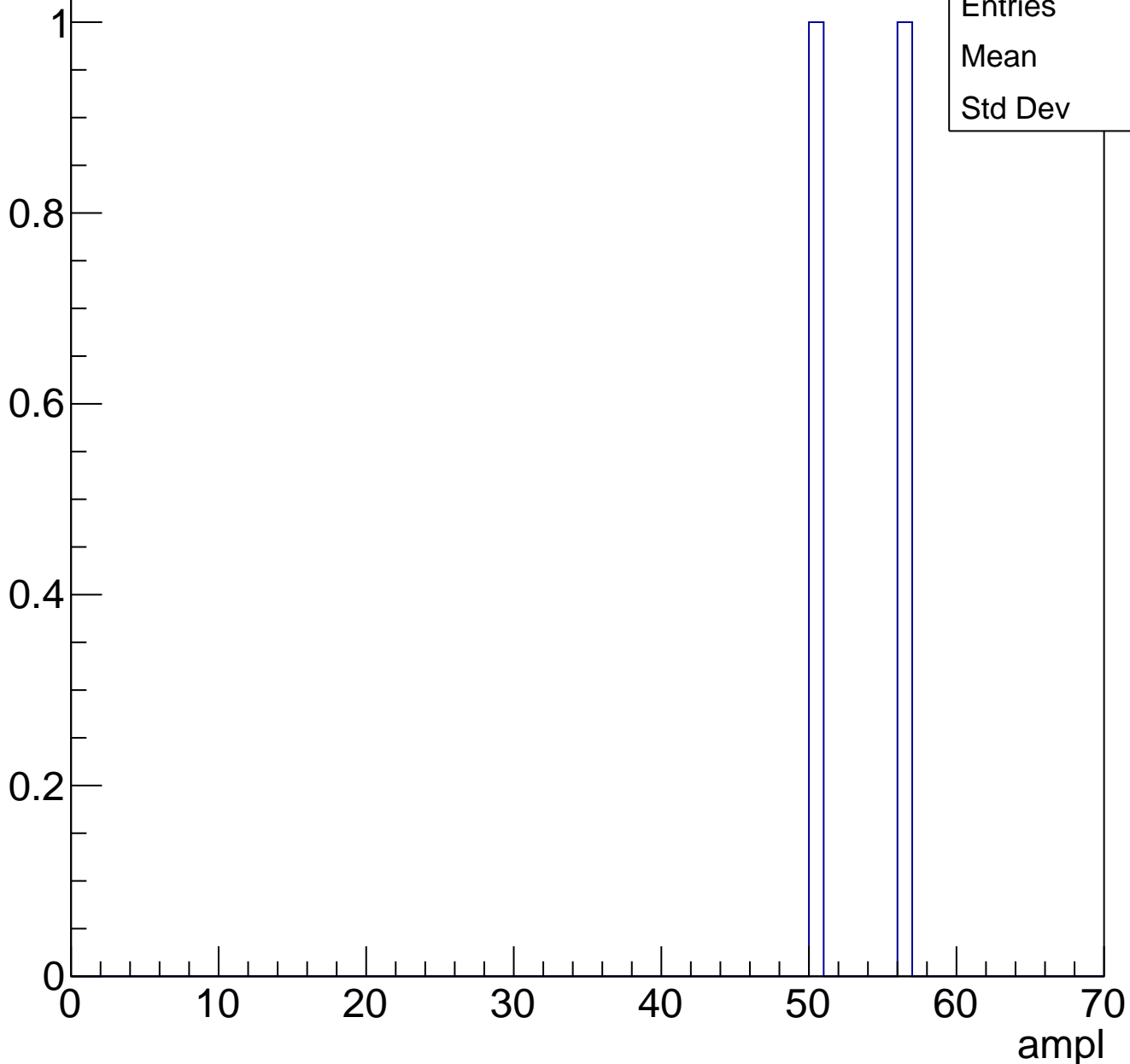
Gaus Width: 0.0000



B0L100S, U12-ch30, adc3

calib_packv5_042523_0143.root, FC#6, port A1

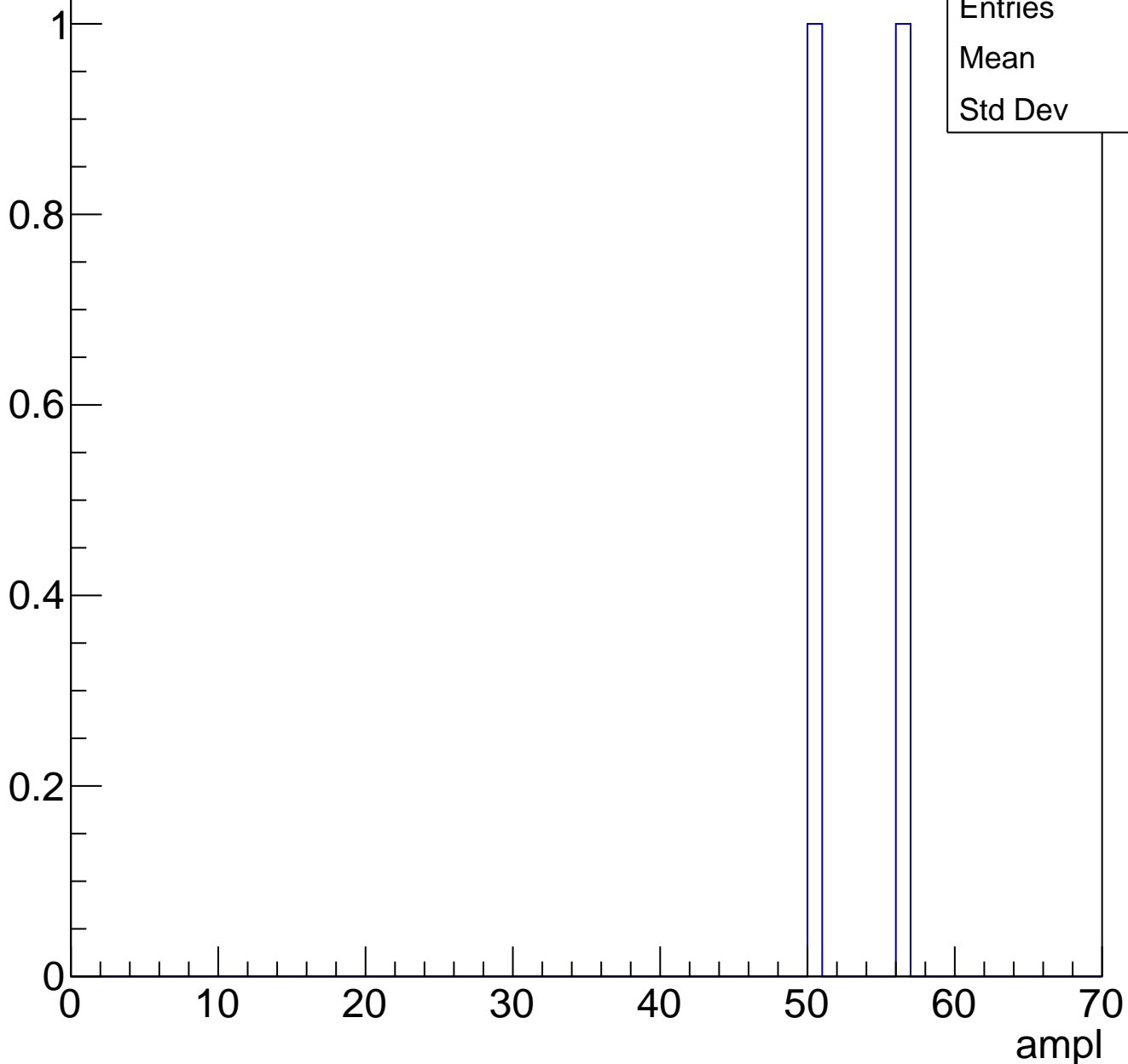
Entry



B0L100S, U12-ch30, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch30, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch30, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch30, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch31, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch31, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch31, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch31, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch31, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch31, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch31, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch31, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch32, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry

1
0.8
0.6
0.4
0.2
0

Entries	1
Mean	43
Std Dev	0

Gaus mean : 0.0000

Gaus Width: 0.0000

ampl

B0L100S, U12-ch32, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	4
Mean	44.5
Std Dev	1.5

Gaus mean : 0.0000

Gaus Width: 0.0000

ampl

0 10 20 30 40 50 60 70

B0L100S, U12-ch32, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

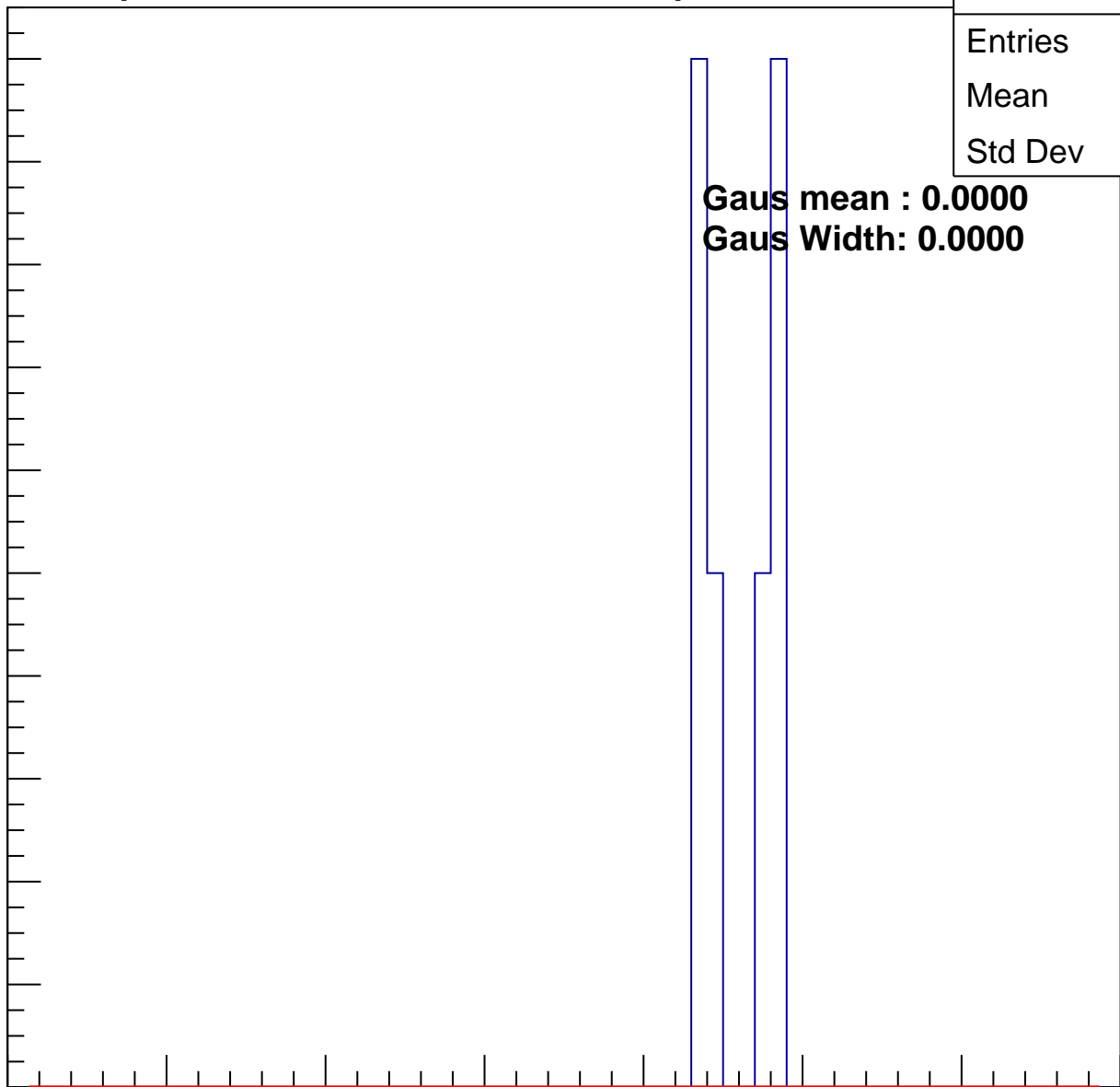
Entries	6
Mean	45.5
Std Dev	2.217

Gaus mean : 0.0000

Gaus Width: 0.0000

0 10 20 30 40 50 60 70

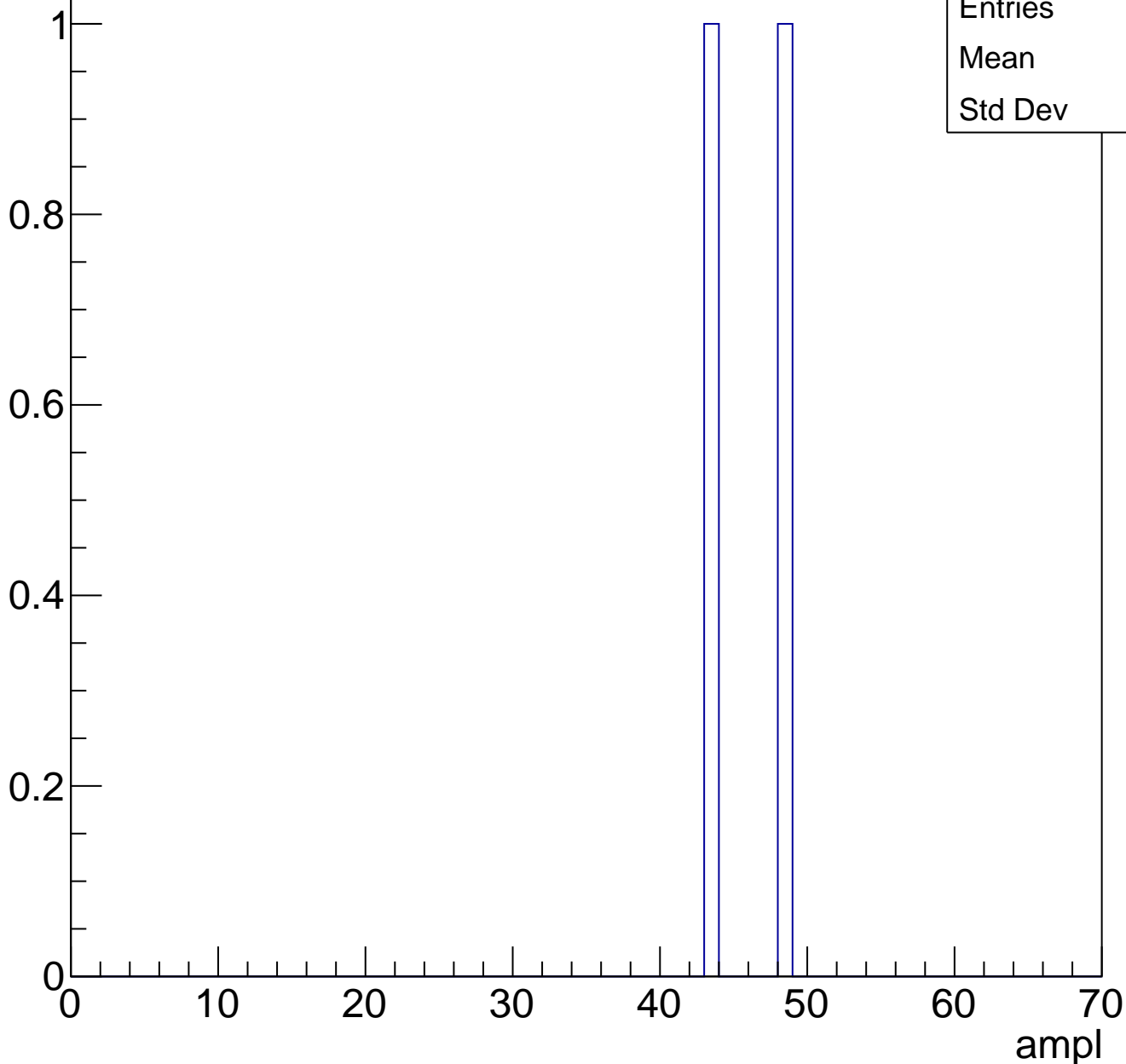
ampl



B0L100S, U12-ch32, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch32, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch32, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch32, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch32, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch33, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry

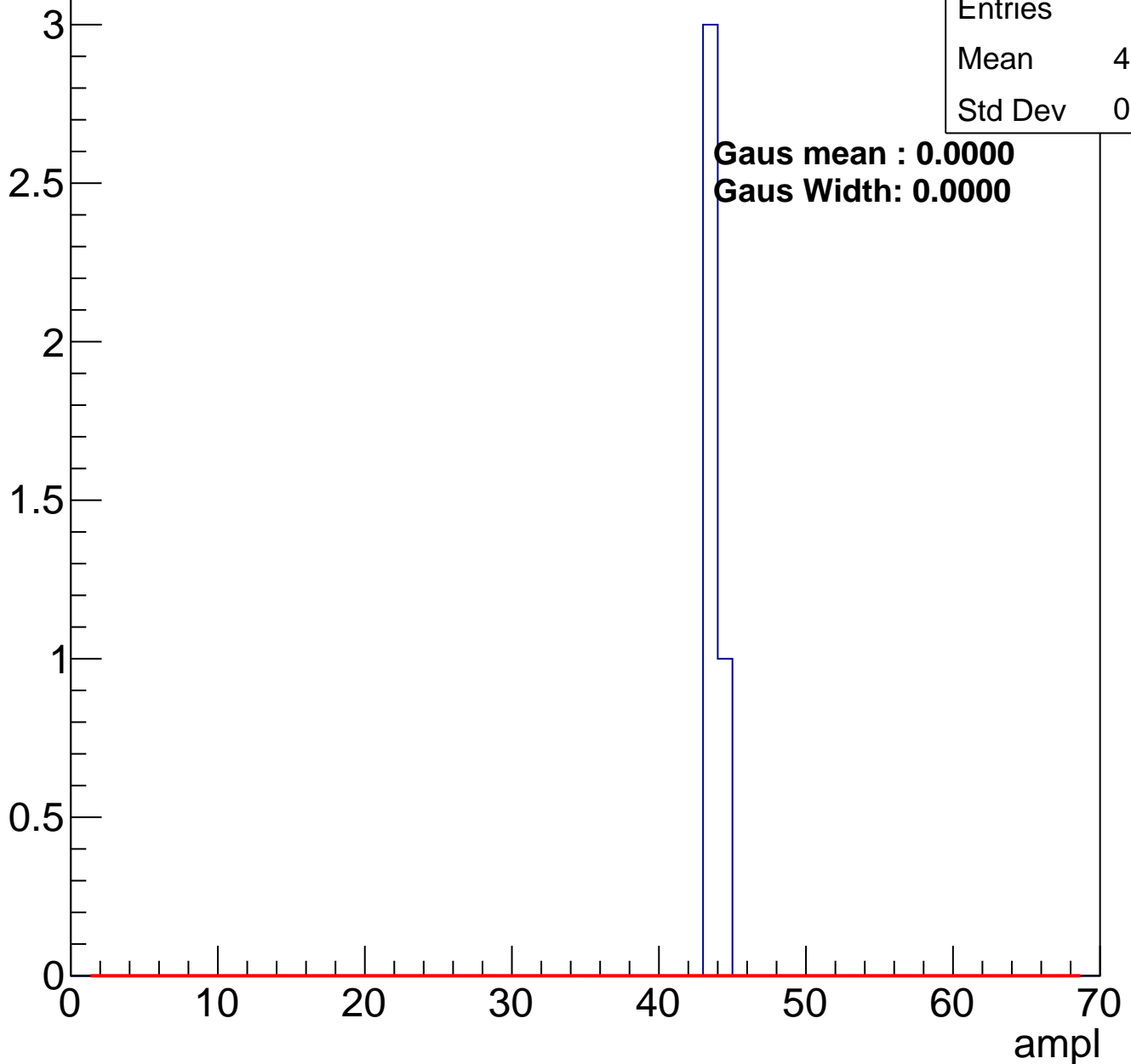


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch33, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	4
Mean	43.25
Std Dev	0.433

B0L100S, U12-ch33, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	4
Mean	44.5
Std Dev	1.5

Gaus mean : 0.0000

Gaus Width: 0.0000

0 10 20 30 40 50 60 70

ampl

B0L100S, U12-ch33, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch33, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch33, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch33, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch33, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch34, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

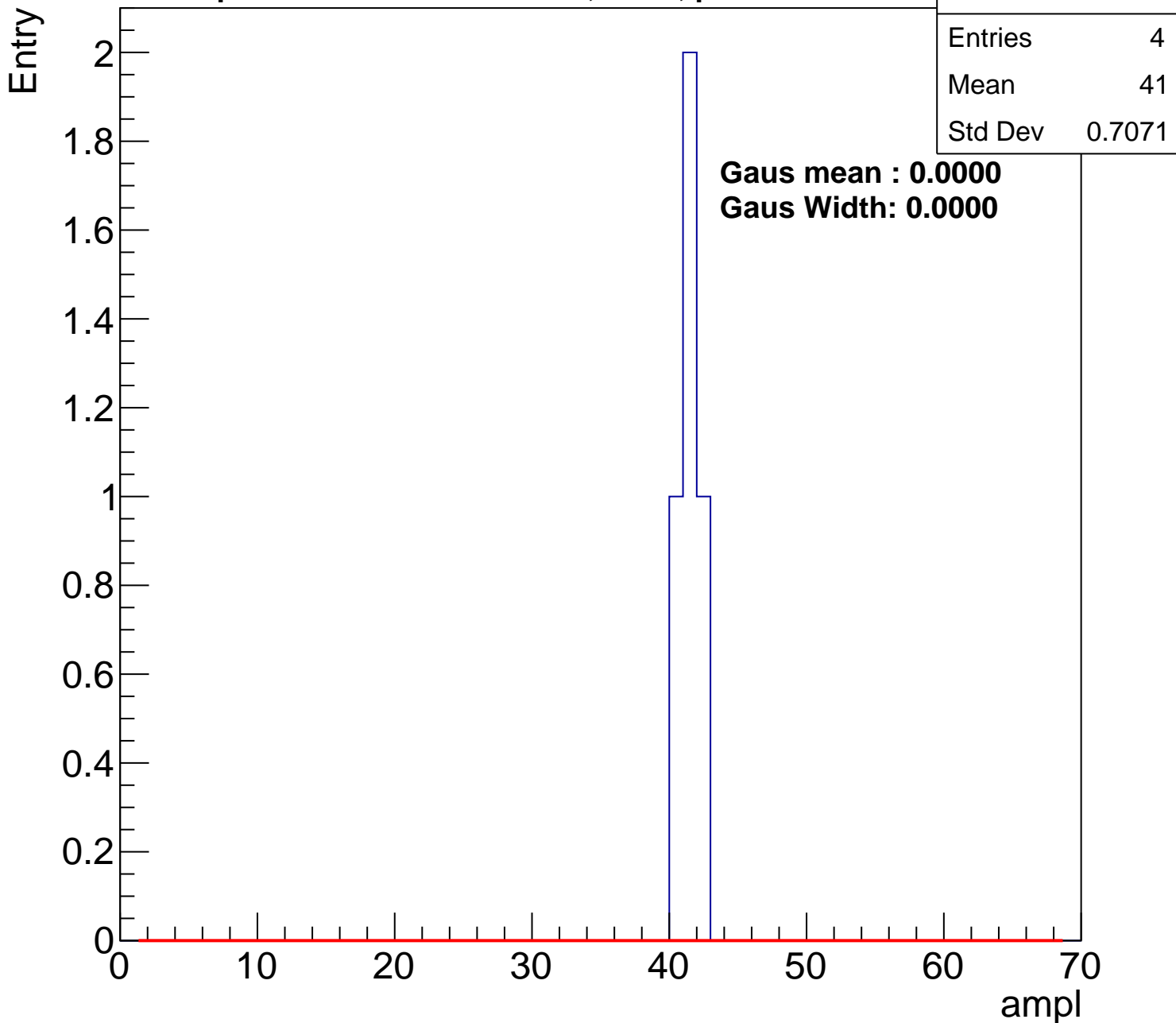
Entries	4
Mean	41
Std Dev	0.7071

Gaus mean : 0.0000

Gaus Width: 0.0000

0 10 20 30 40 50 60 70

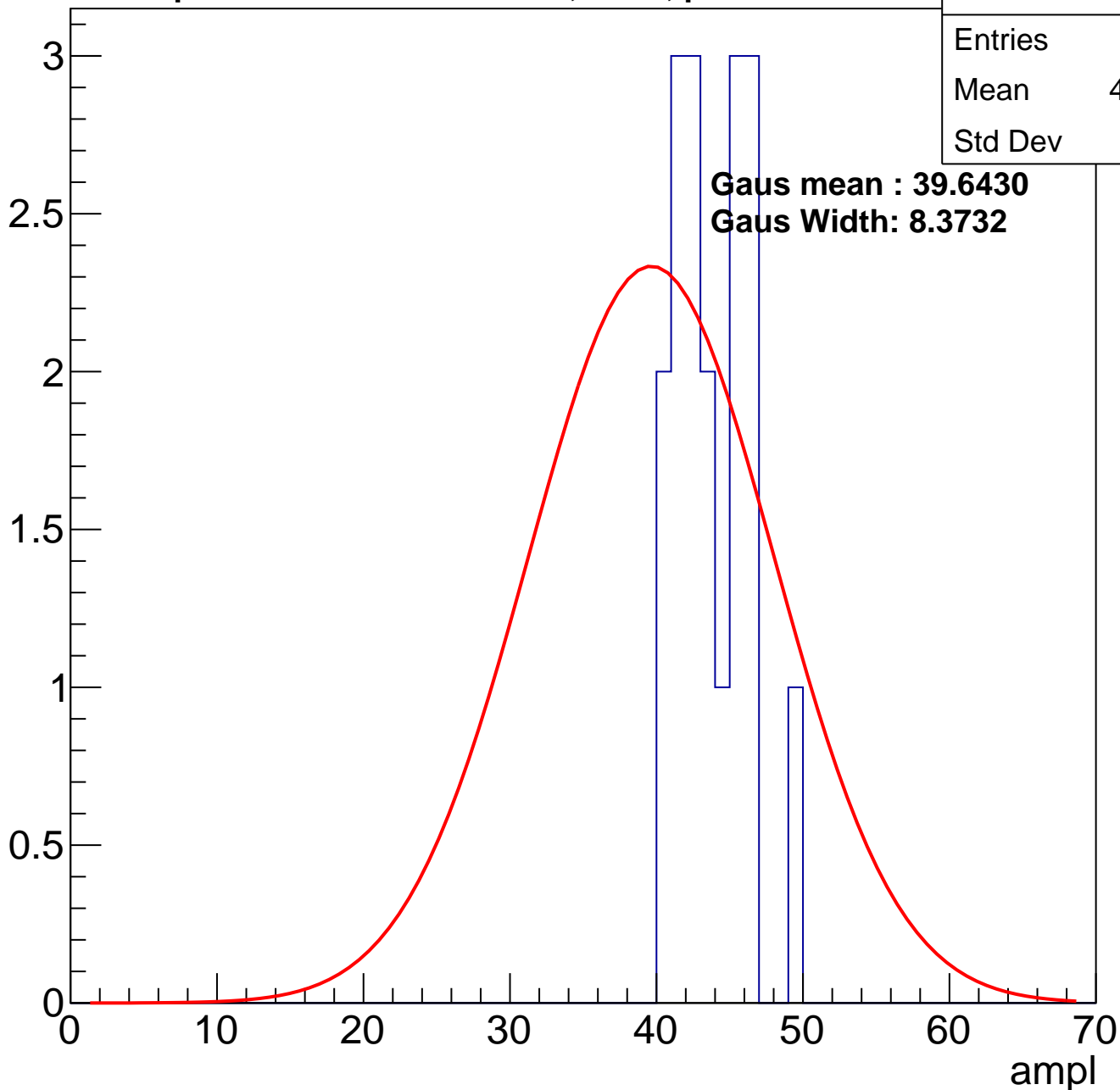
ampl



B0L100S, U12-ch34, adc1

calib_packv5_042523_0143.root, FC#6, port A1

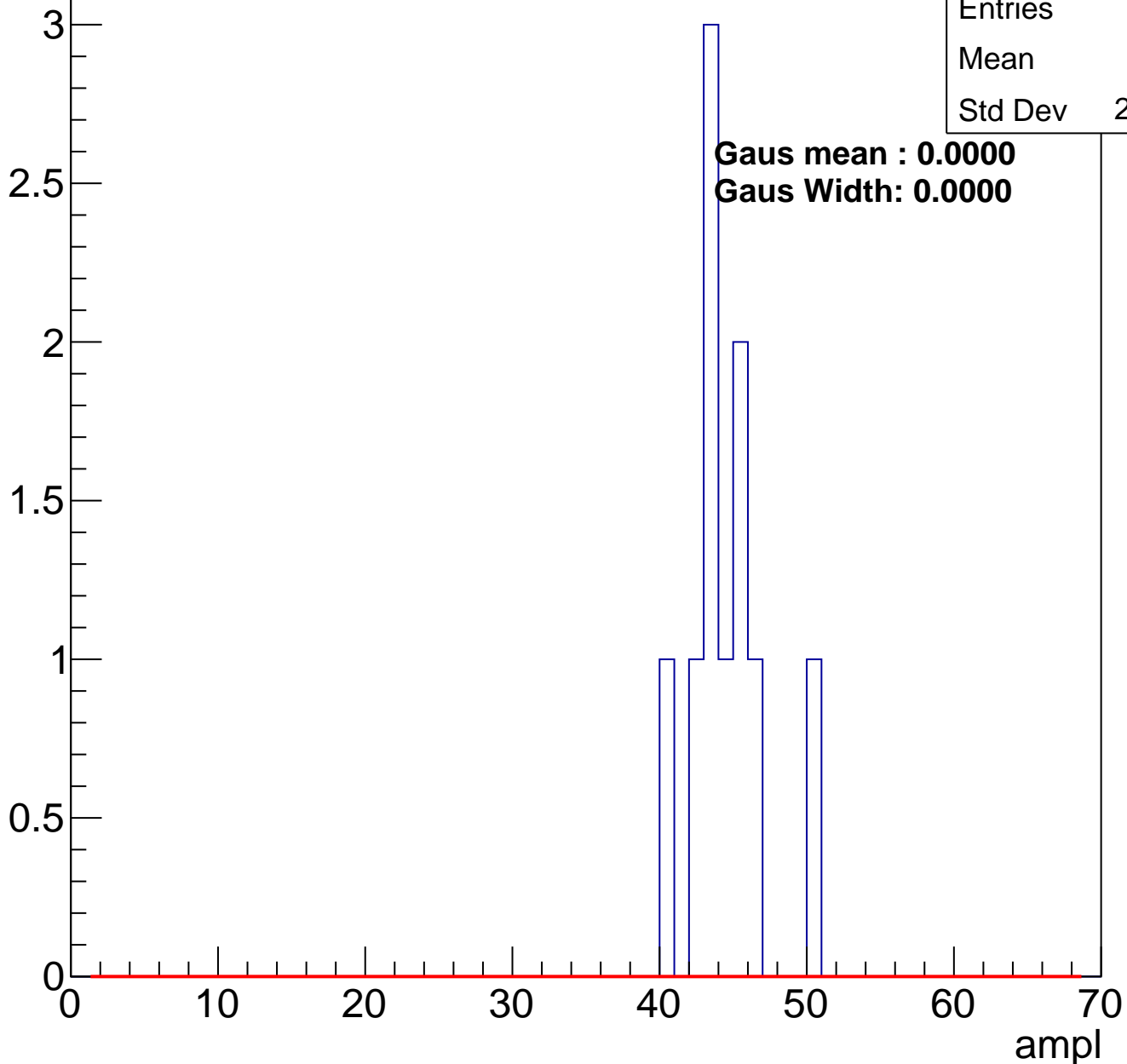
Entry



B0L100S, U12-ch34, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch34, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch34, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch34, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch34, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch34, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch35, adc0

calib_packv5_042523_0143.root, FC#6, port A1

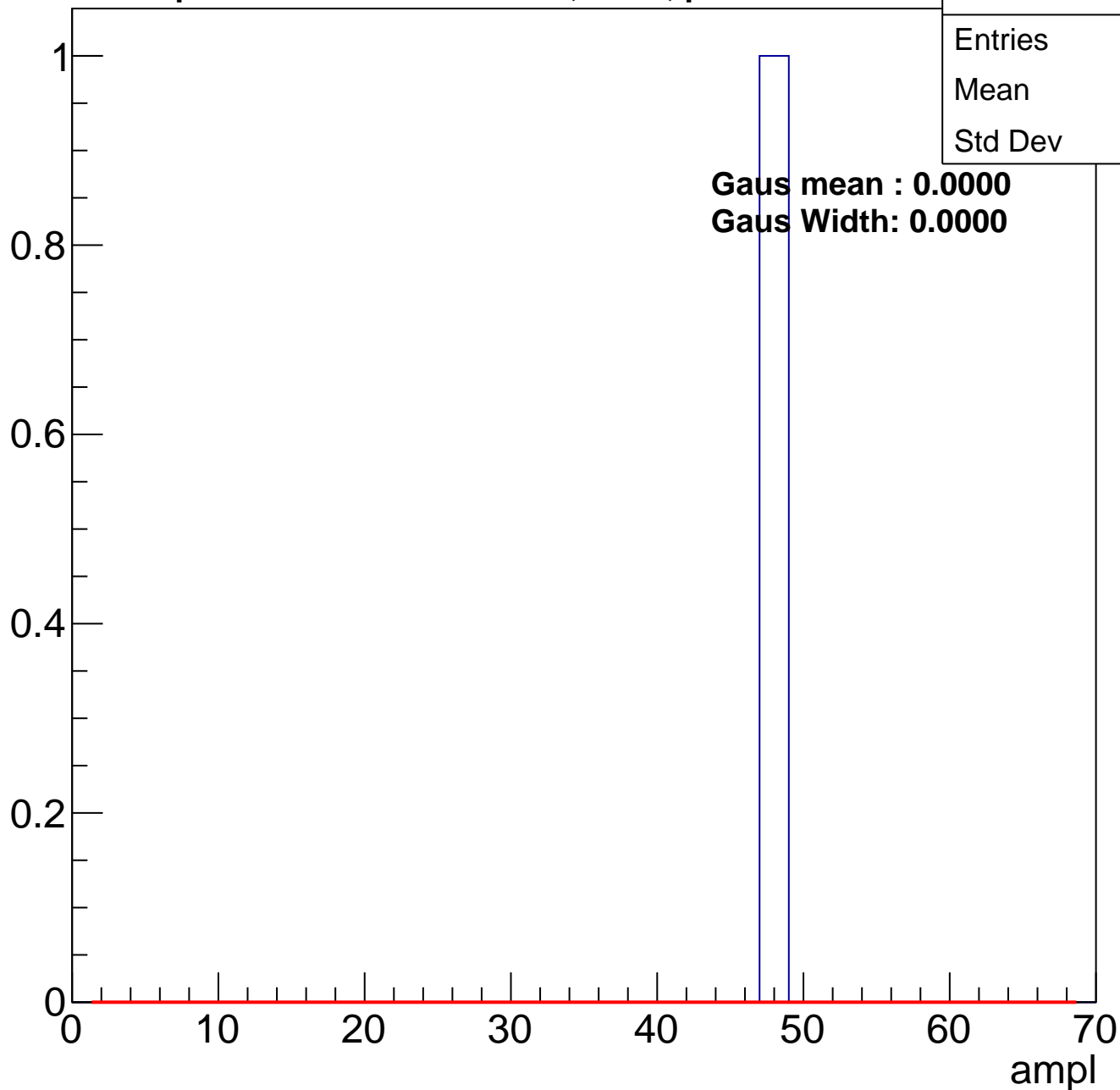
Entry



B0L100S, U12-ch35, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch35, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

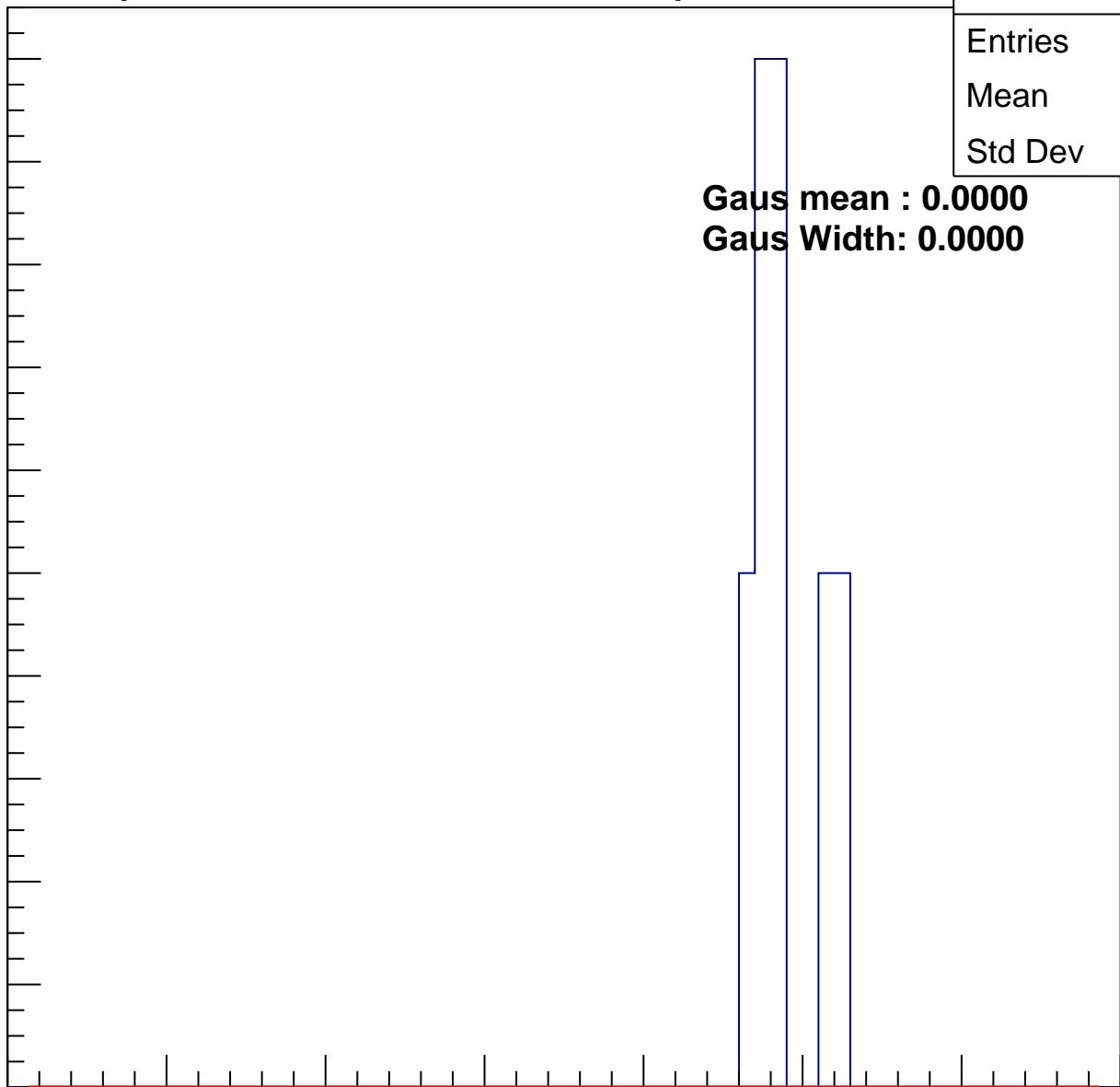
Entries	7
Mean	48.43
Std Dev	2.06

Gaus mean : 0.0000

Gaus Width: 0.0000

0 10 20 30 40 50 60 70

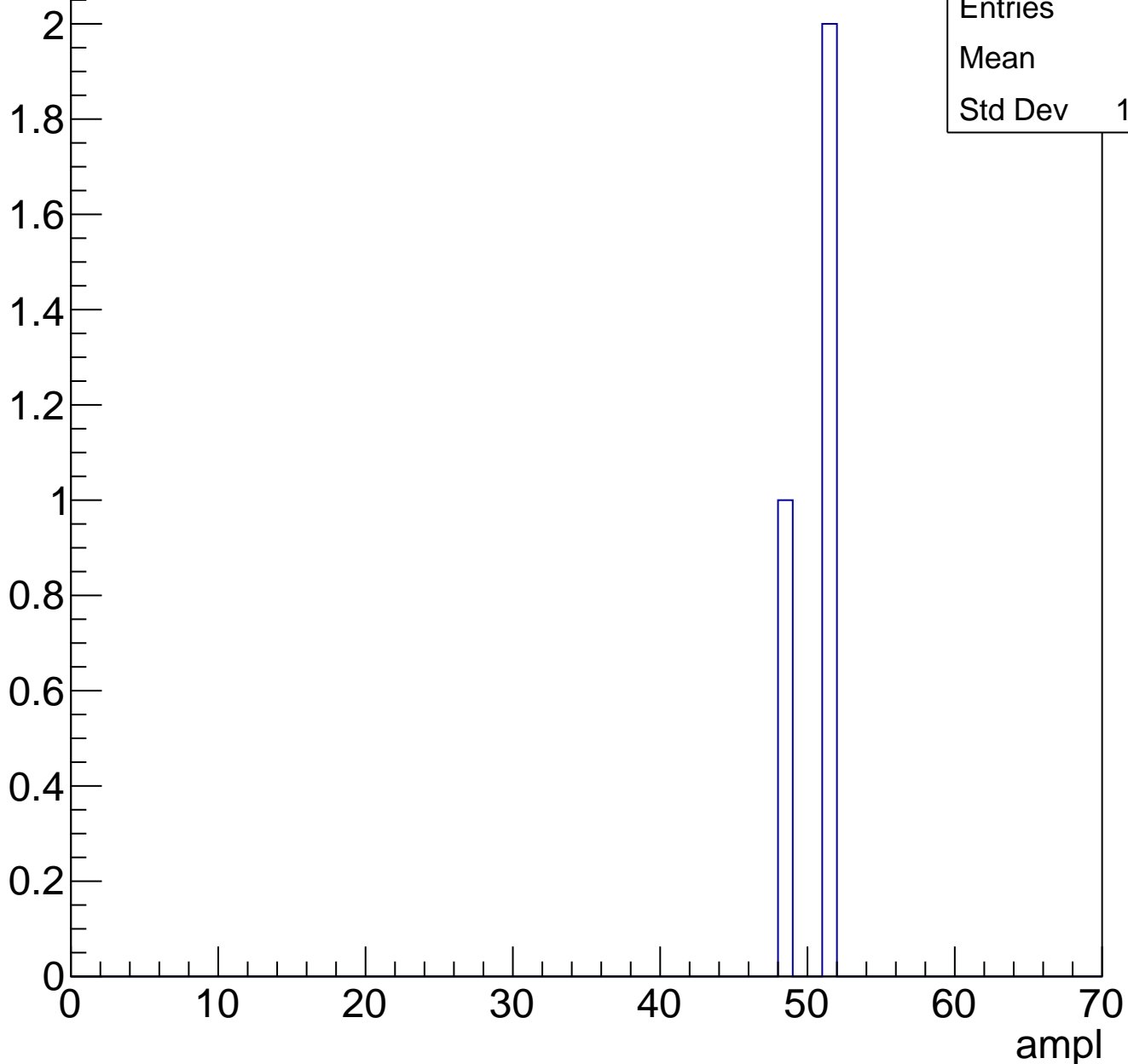
ampl



B0L100S, U12-ch35, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	3
Mean	50
Std Dev	1.414

B0L100S, U12-ch35, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch35, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch35, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch35, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch36, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry

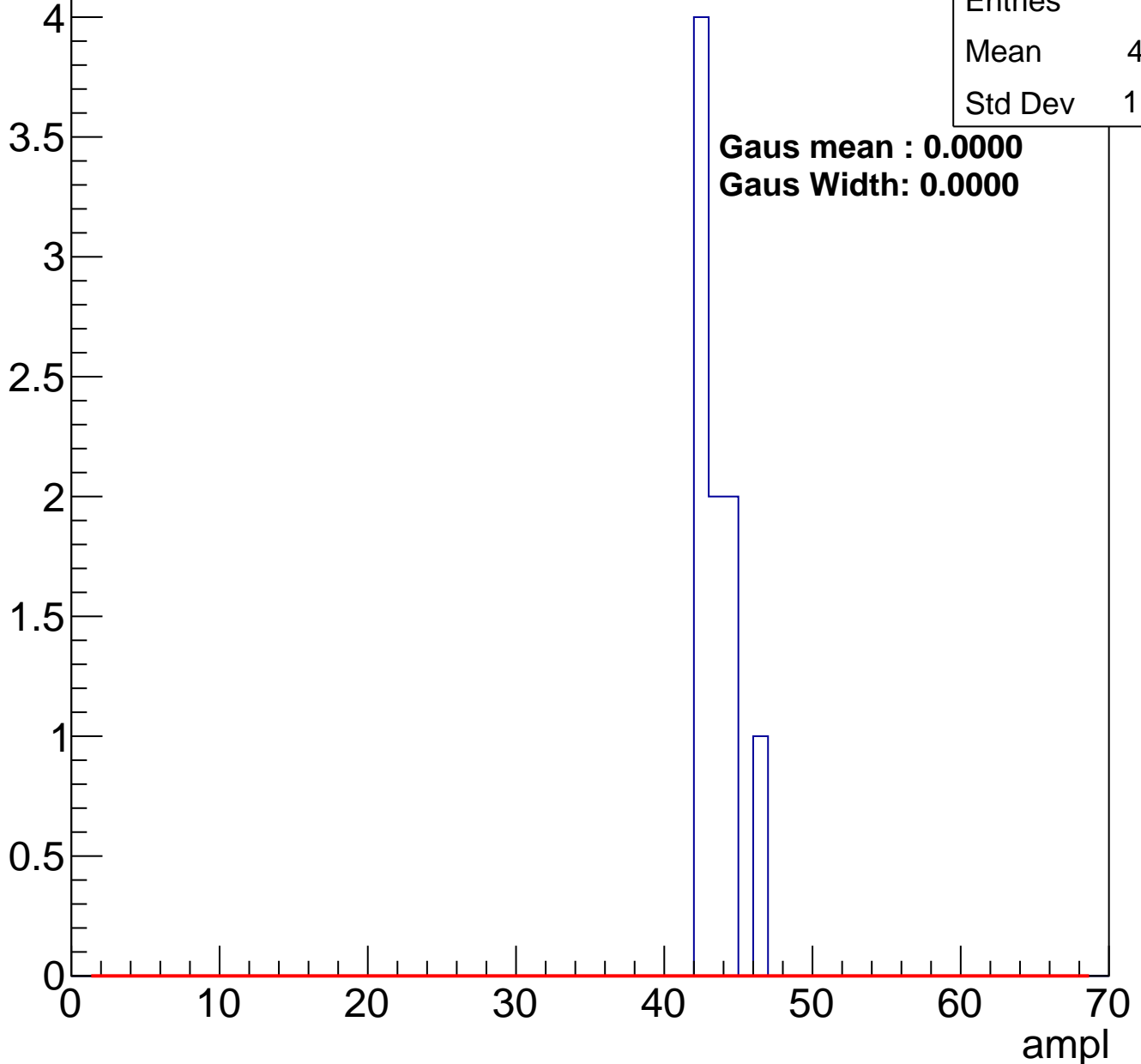


Entries	1
Mean	0
Std Dev	0

B0L100S, U12-ch36, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	9
Mean	43.11
Std Dev	1.286

B0L100S, U12-ch36, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

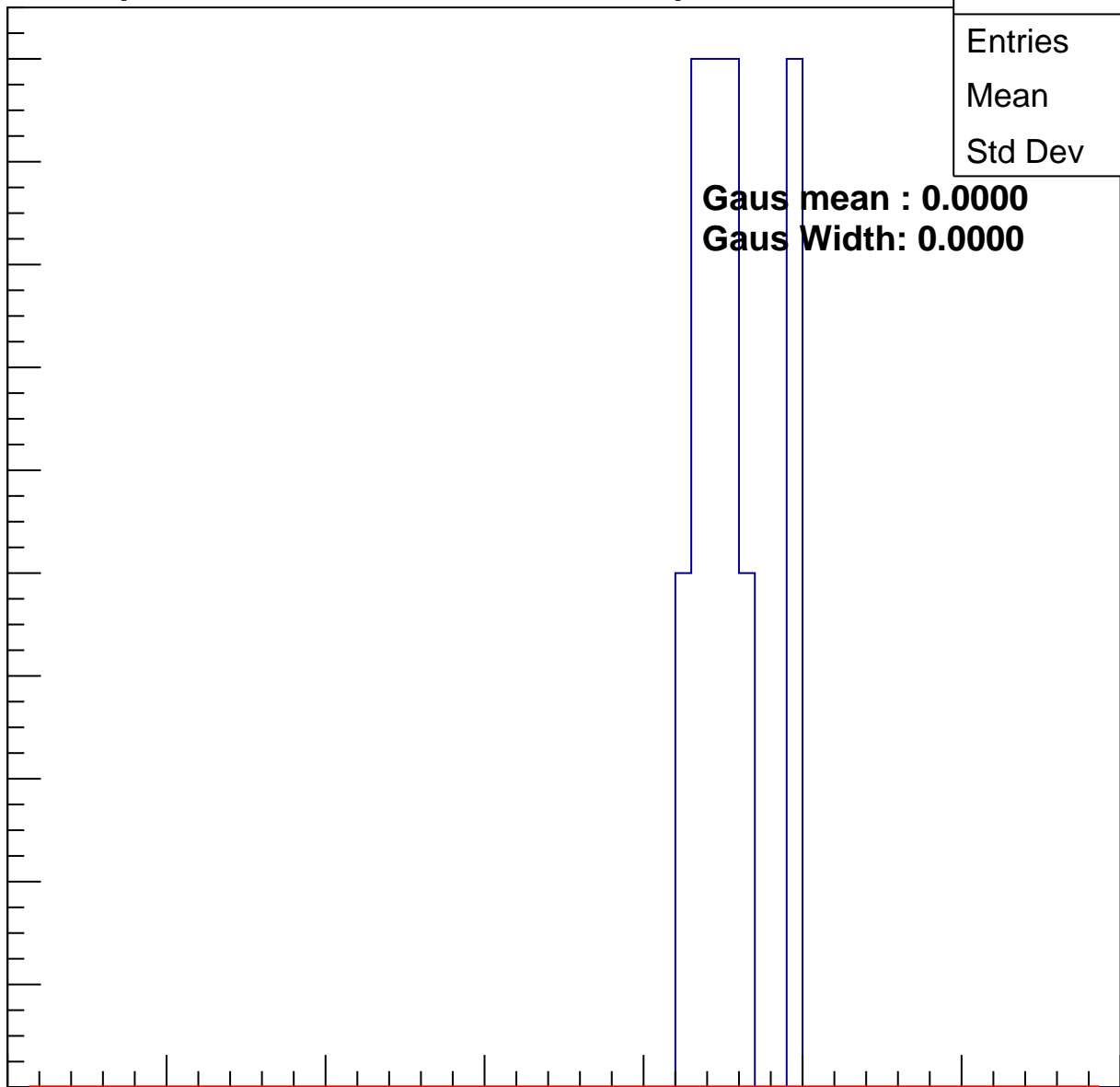
Entries	10
Mean	45
Std Dev	2.28

Gaus mean : 0.0000

Gaus Width: 0.0000

0 10 20 30 40 50 60 70

ampl



B0L100S, U12-ch36, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	2
Mean	45
Std Dev	0

0 10 20 30 40 50 60 70

ampl



B0L100S, U12-ch36, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch36, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch36, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch36, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry

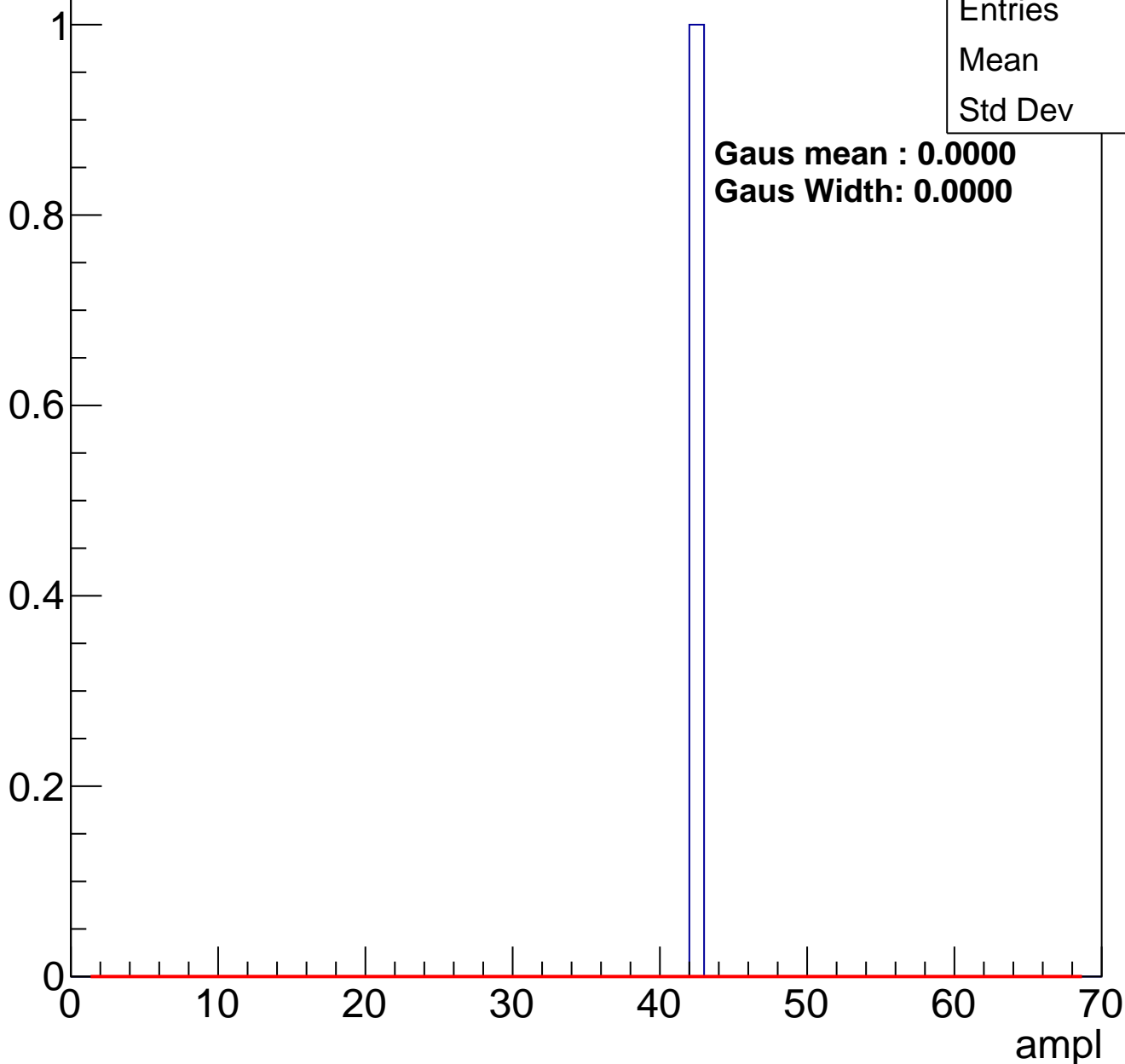


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch37, adc0

calib_packv5_042523_0143.root, FC#6, port A1

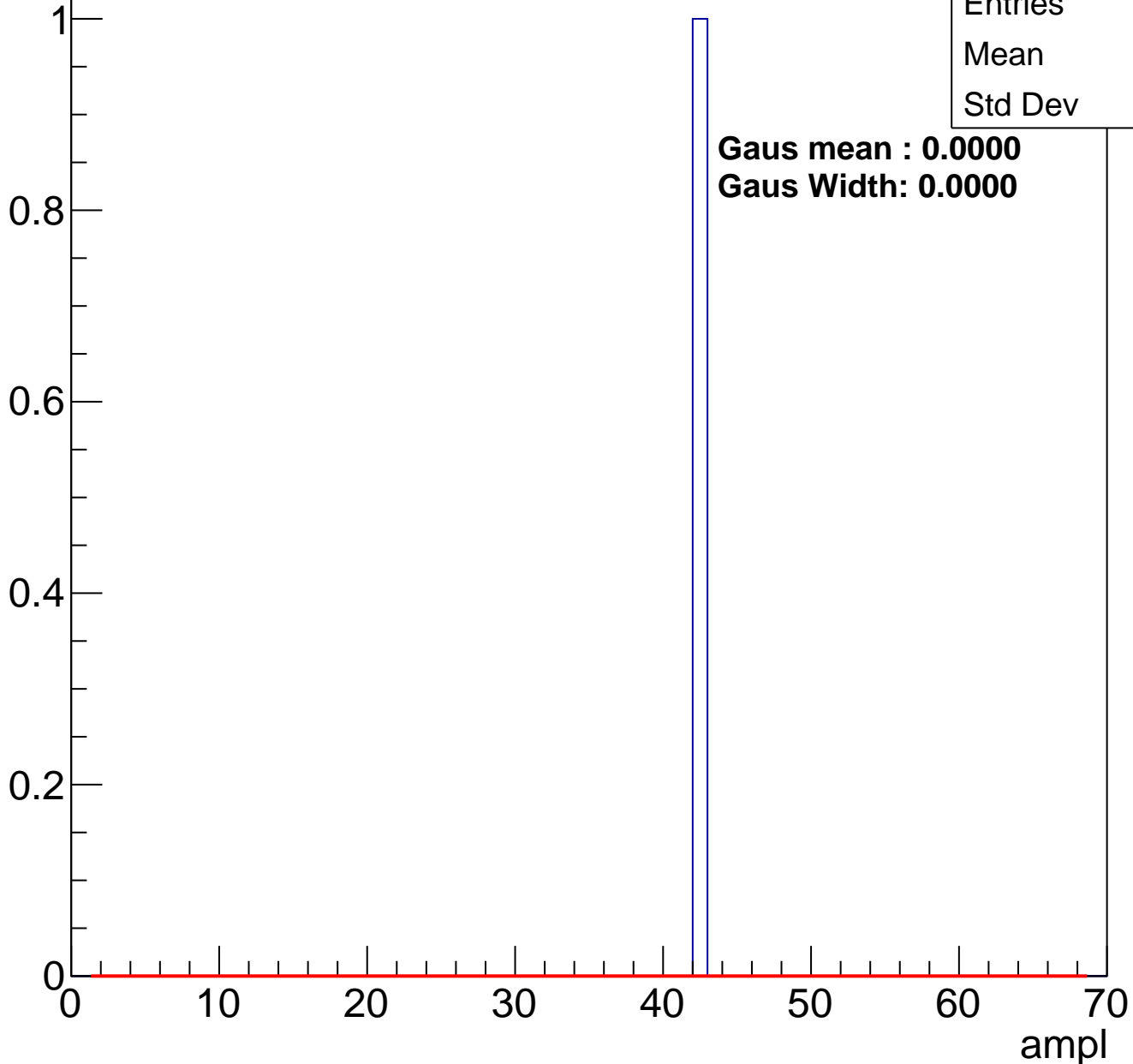
Entry



B0L100S, U12-ch37, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry

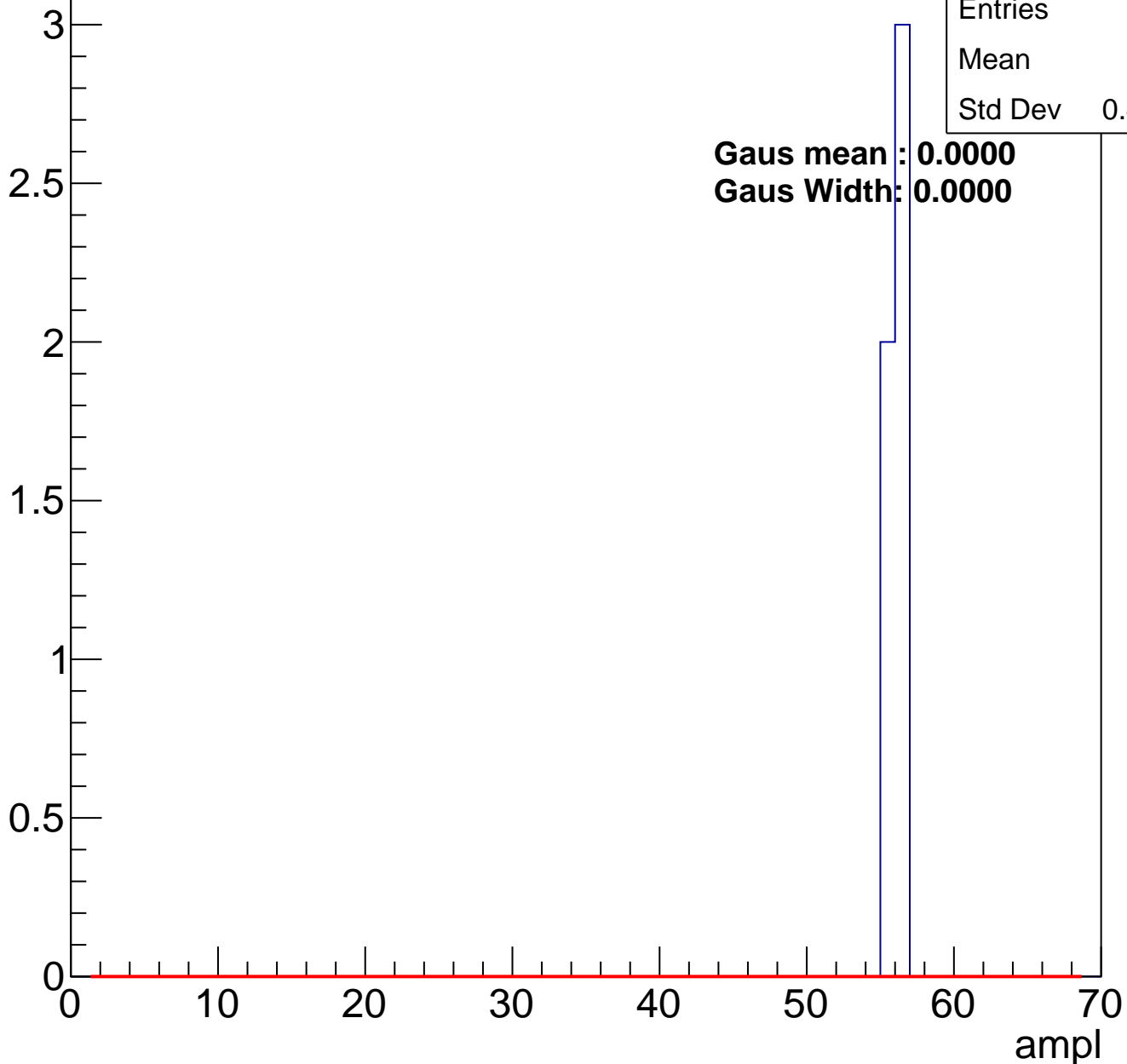


Entries	1
Mean	42
Std Dev	0

B0L100S, U12-ch37, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	5
Mean	55.6
Std Dev	0.4899

B0L100S, U12-ch37, adc3

calib_packv5_042523_0143.root, FC#6, port A1

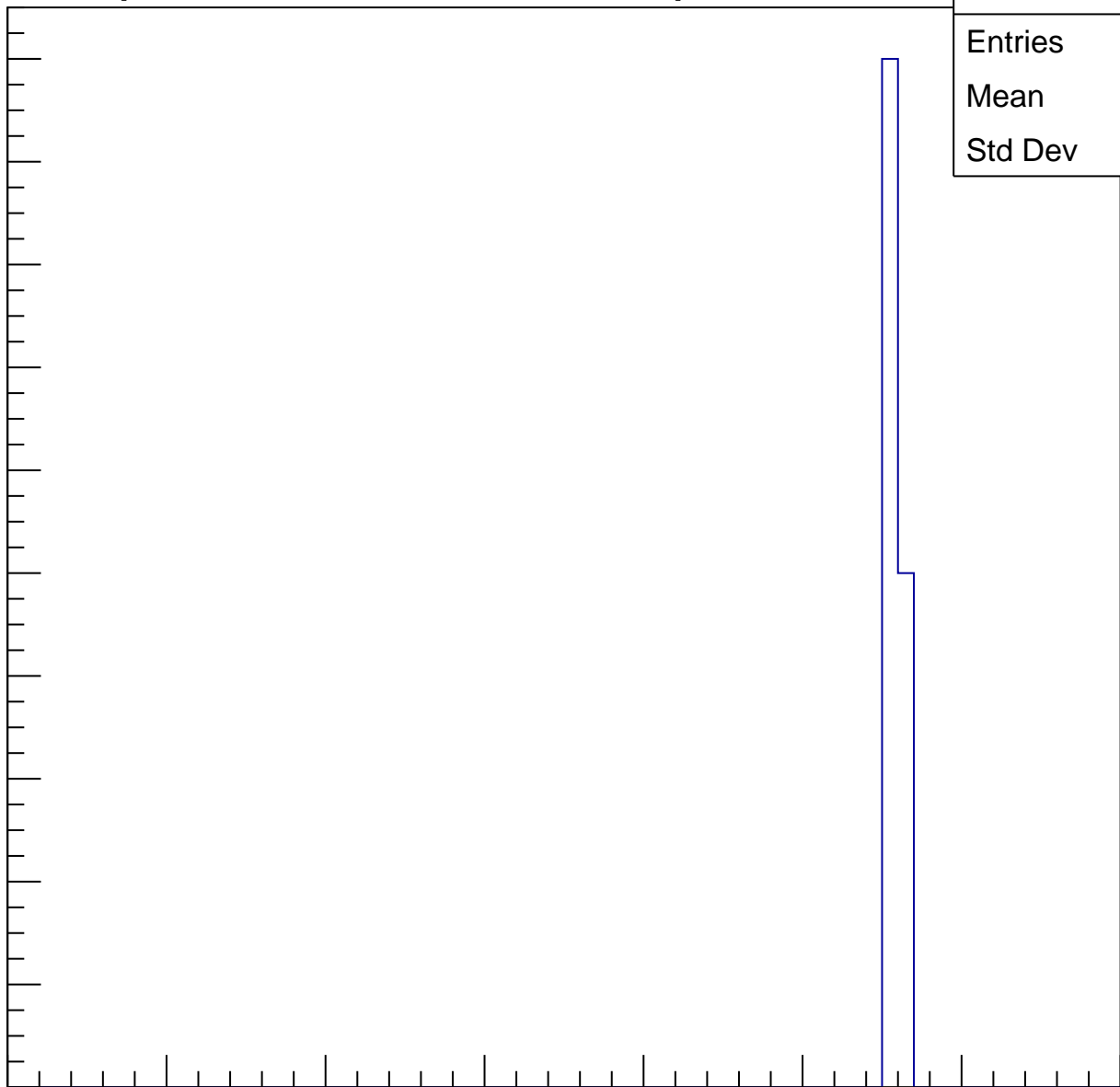
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	3
Mean	55.33
Std Dev	0.4714

0 10 20 30 40 50 60 70

ampl



B0L100S, U12-ch37, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch37, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch37, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch37, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch38, adc0

calib_packv5_042523_0143.root, FC#6, port A1

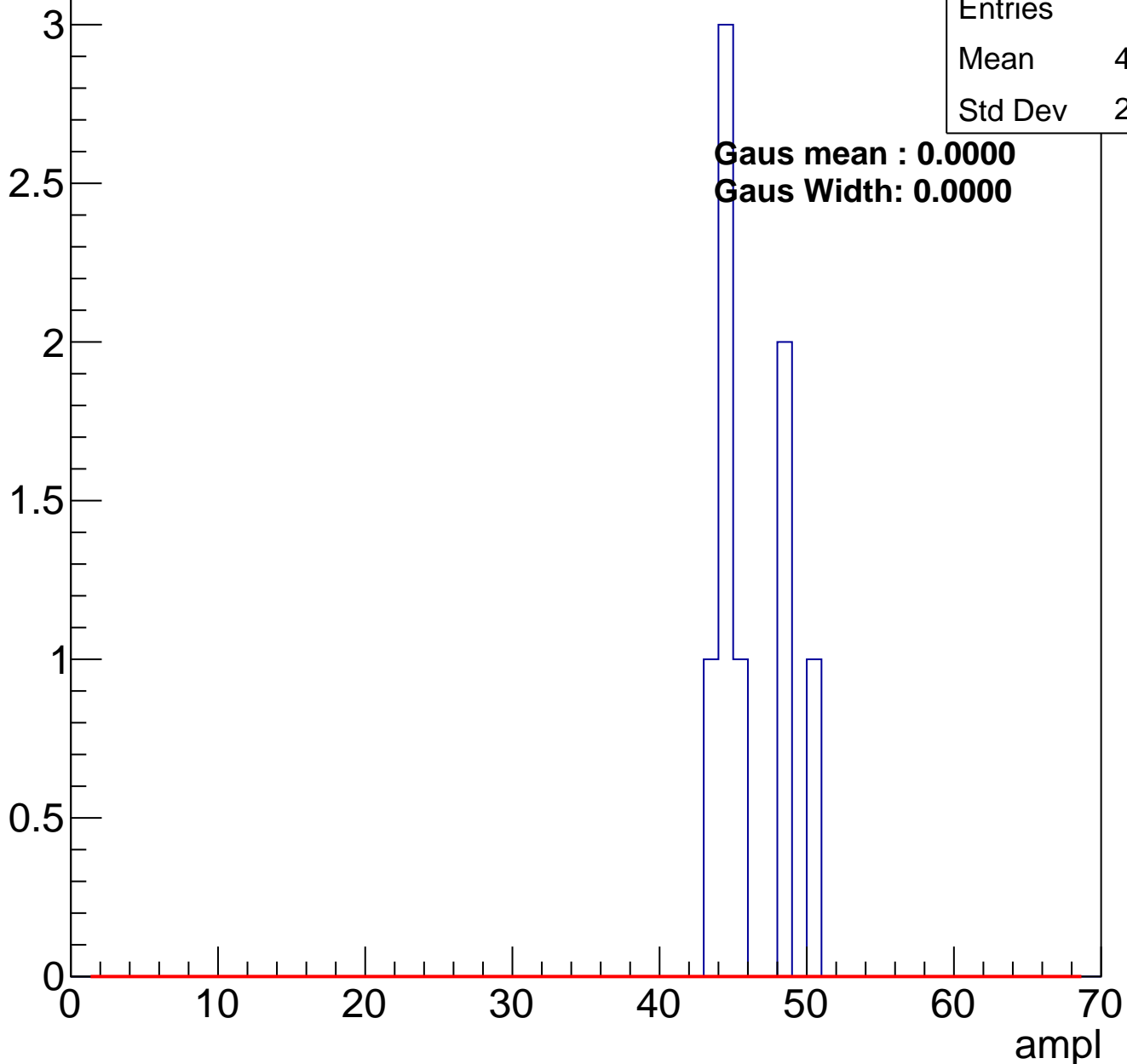
Entry



B0L100S, U12-ch38, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry

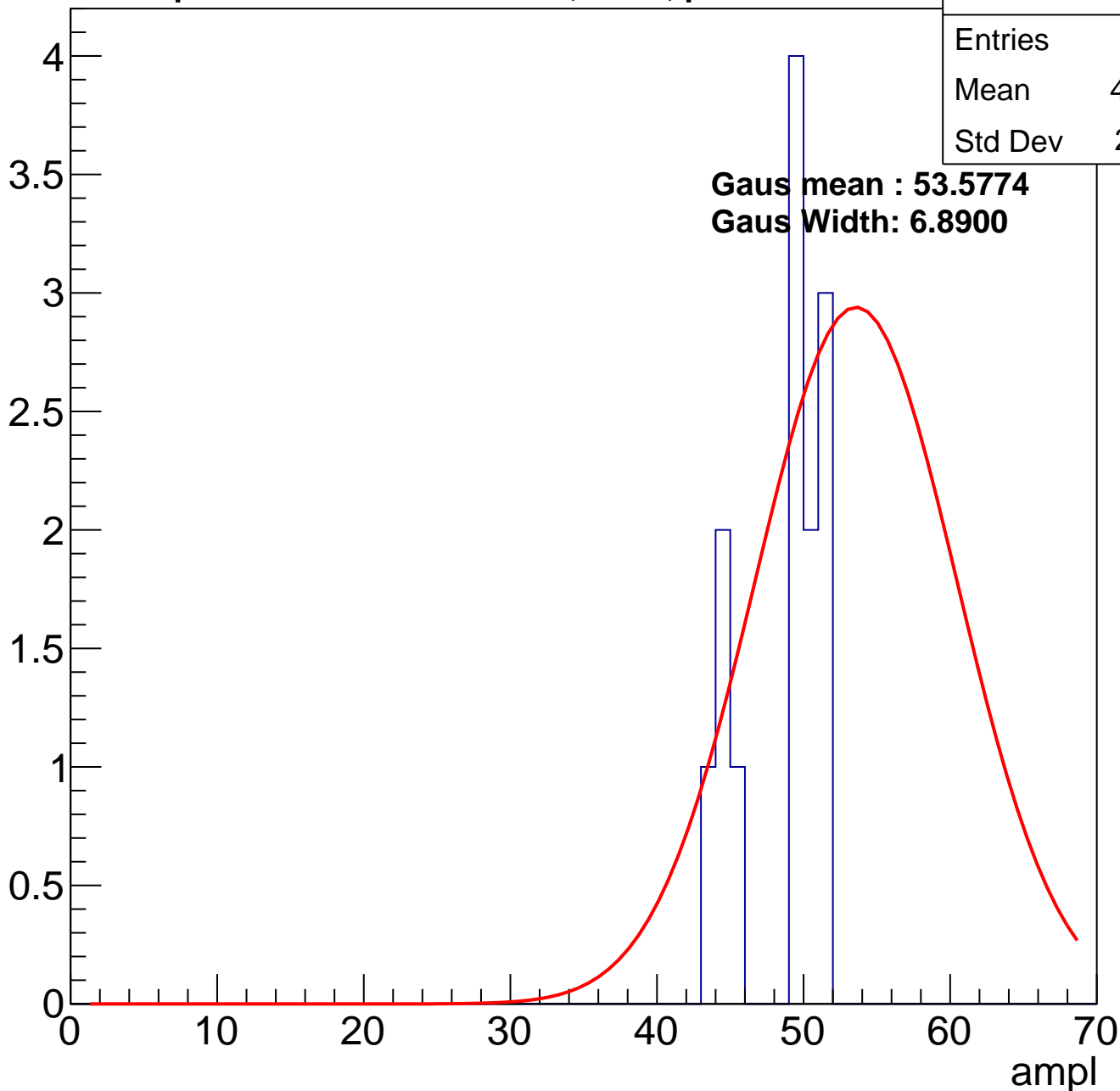


Entries	8
Mean	45.75
Std Dev	2.385

B0L100S, U12-ch38, adc2

calib_packv5_042523_0143.root, FC#6, port A1

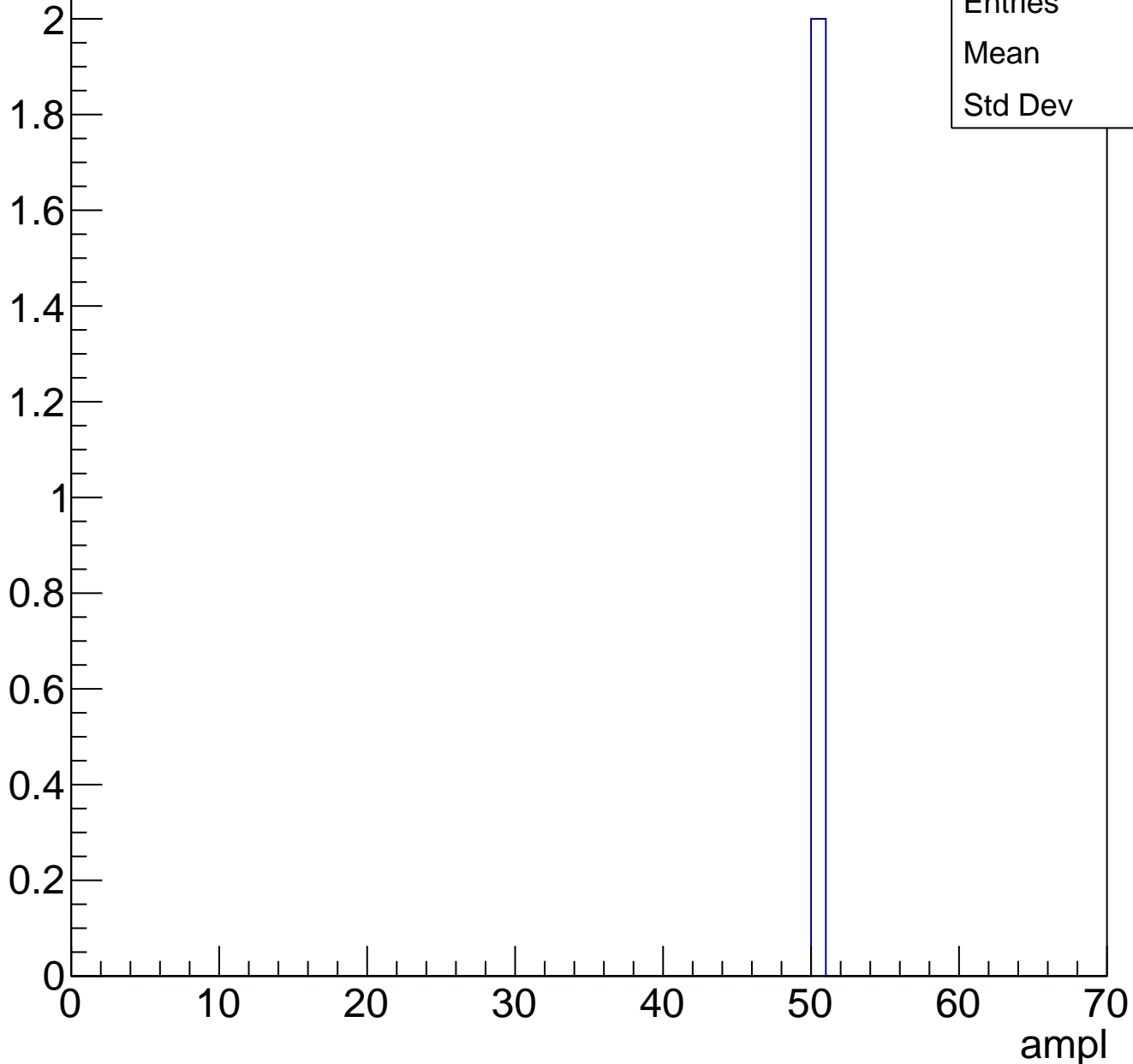
Entry



B0L100S, U12-ch38, adc3

calib_packv5_042523_0143.root, FC#6, port A1

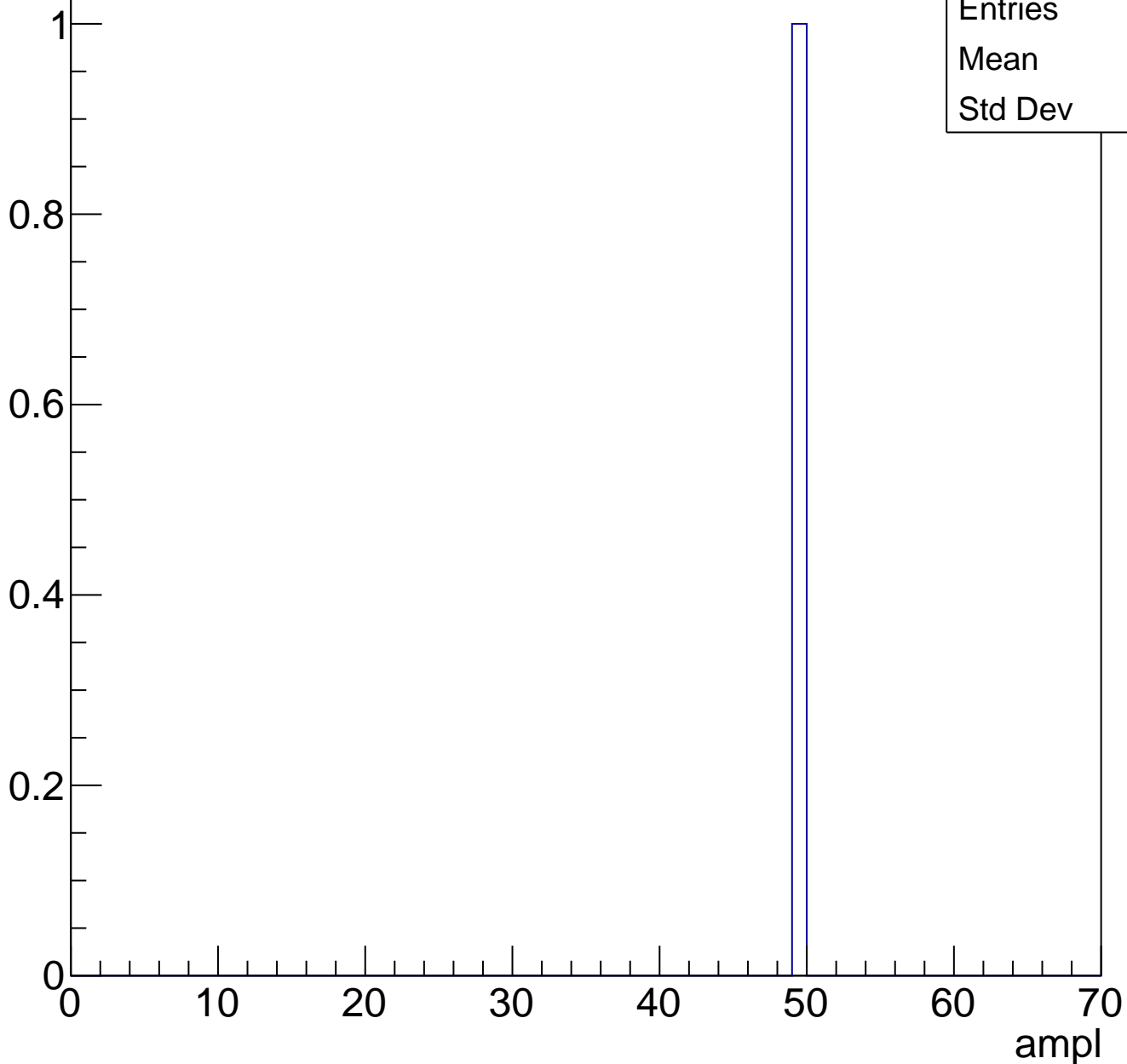
Entry



B0L100S, U12-ch38, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch38, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch38, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch38, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch39, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch39, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch39, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch39, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch39, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch39, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch39, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch39, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch40, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch40, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

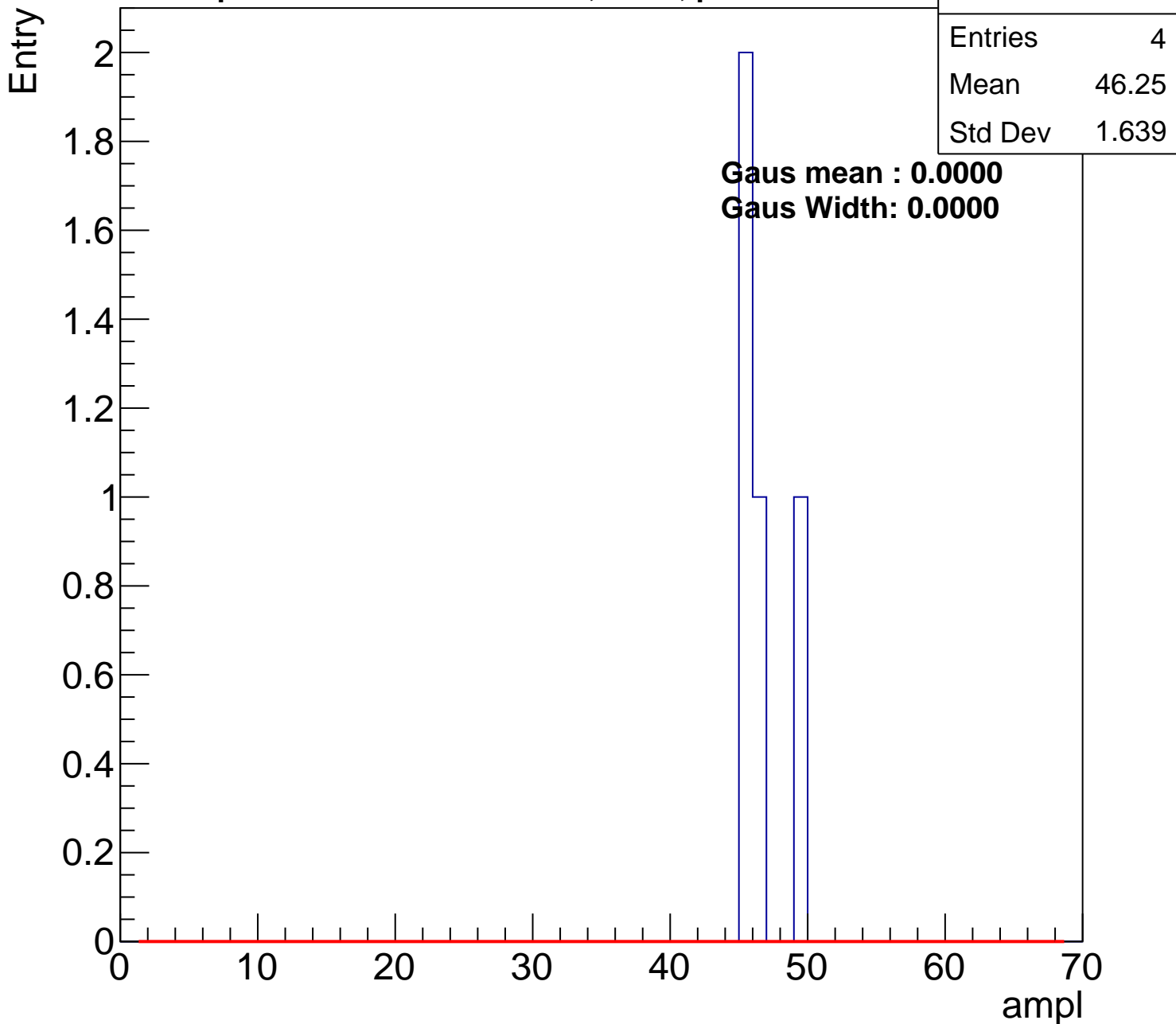
Entries	4
Mean	46.25
Std Dev	1.639

Gaus mean : 0.0000

Gaus Width: 0.0000

0 10 20 30 40 50 60 70

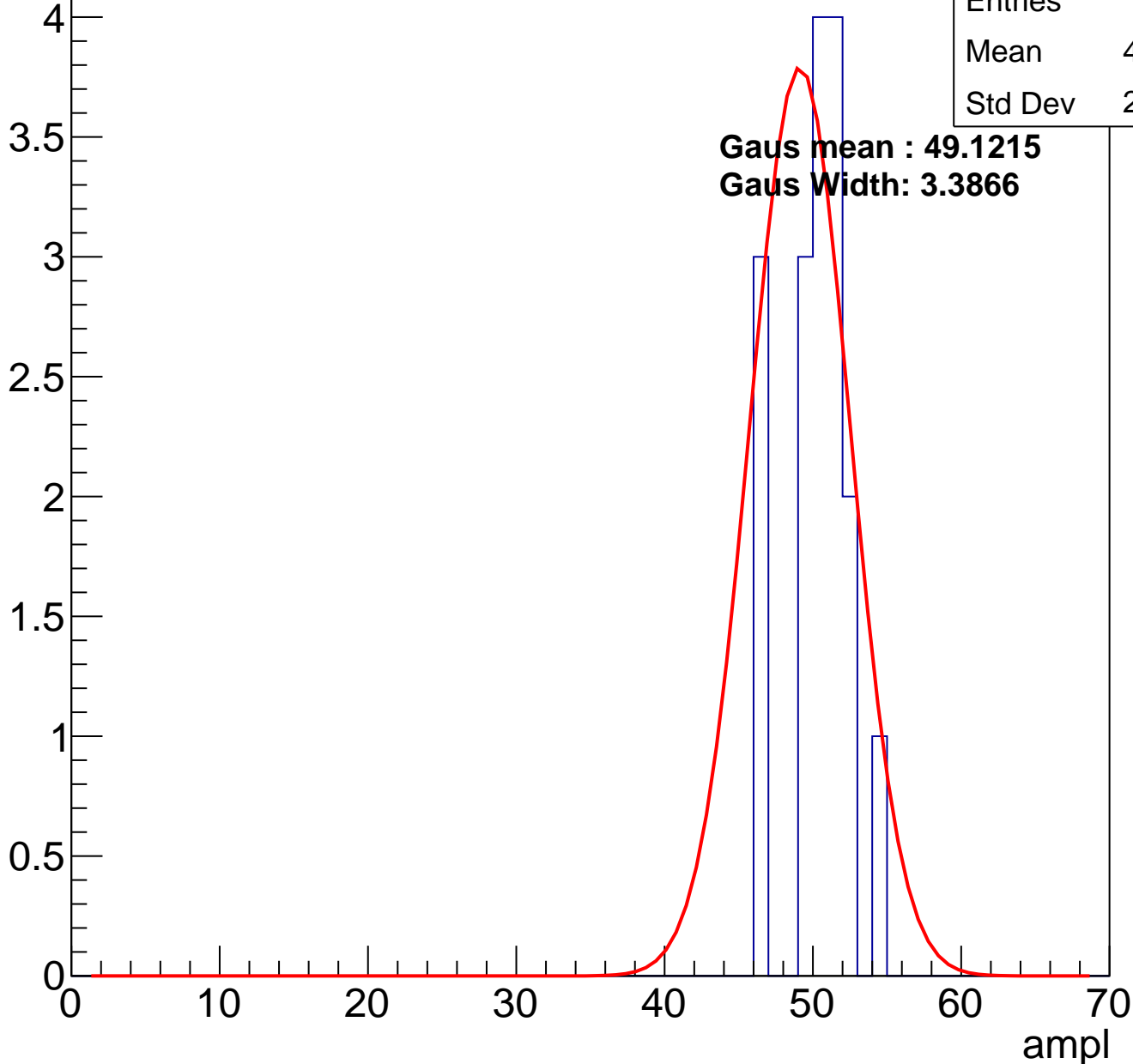
ampl



B0L100S, U12-ch40, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

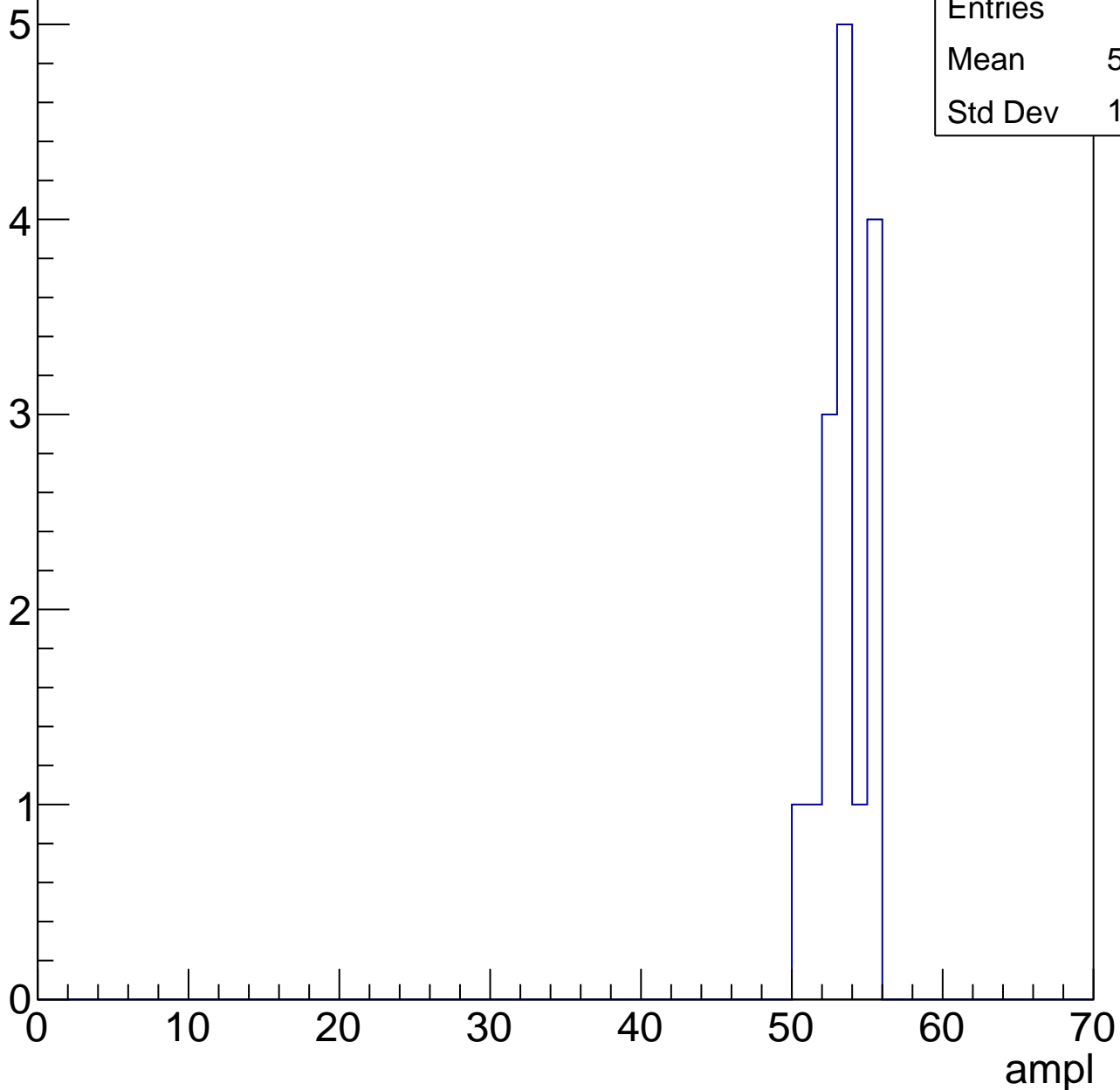


B0L100S, U12-ch40, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry

Entries	15
Mean	53.07
Std Dev	1.482



B0L100S, U12-ch40, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry

3
2.5
2
1.5
1
0.5
0

Entries	3
Mean	54
Std Dev	0

ampl

0 10 20 30 40 50 60 70

B0L100S, U12-ch40, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch40, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch40, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch41, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch41, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch41, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch41, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch41, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch41, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch41, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch41, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch42, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch42, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch42, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch42, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch42, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch42, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch42, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch42, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch43, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch43, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch43, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch43, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch43, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch43, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch43, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch43, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch44, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Gaus mean : 0.0000

Gaus Width: 0.0000

Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch44, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch44, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch44, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch44, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch44, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch44, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch44, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch45, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch45, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch45, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch45, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch45, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch45, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch45, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch45, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch46, adc0

calib_packv5_042523_0143.root, FC#6, port A1

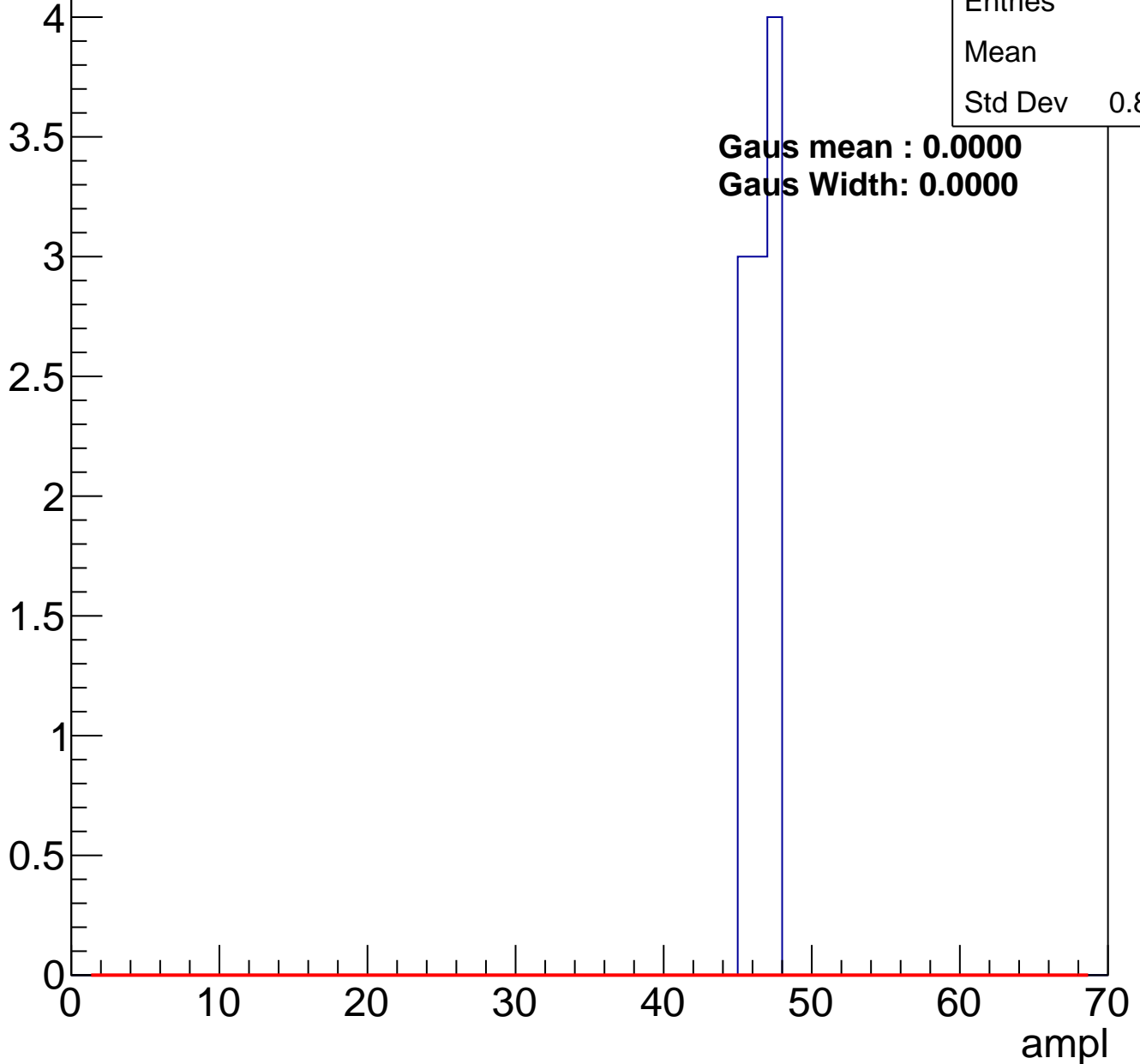
Entry



B0L100S, U12-ch46, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch46, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

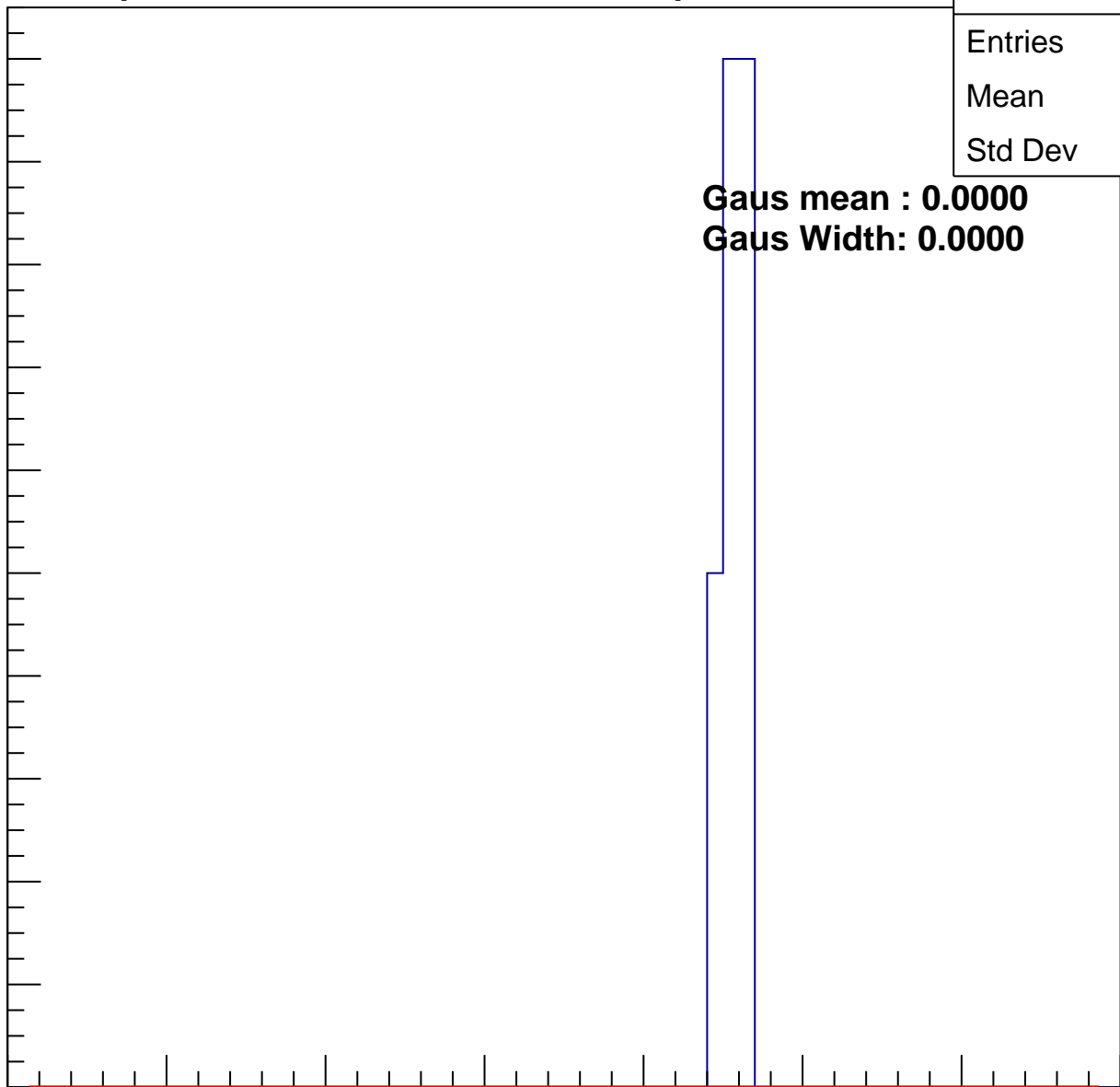
Entries	5
Mean	45.2
Std Dev	0.7483

Gaus mean : 0.0000

Gaus Width: 0.0000

0 10 20 30 40 50 60 70

ampl



B0L100S, U12-ch46, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch46, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch46, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch46, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch46, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry

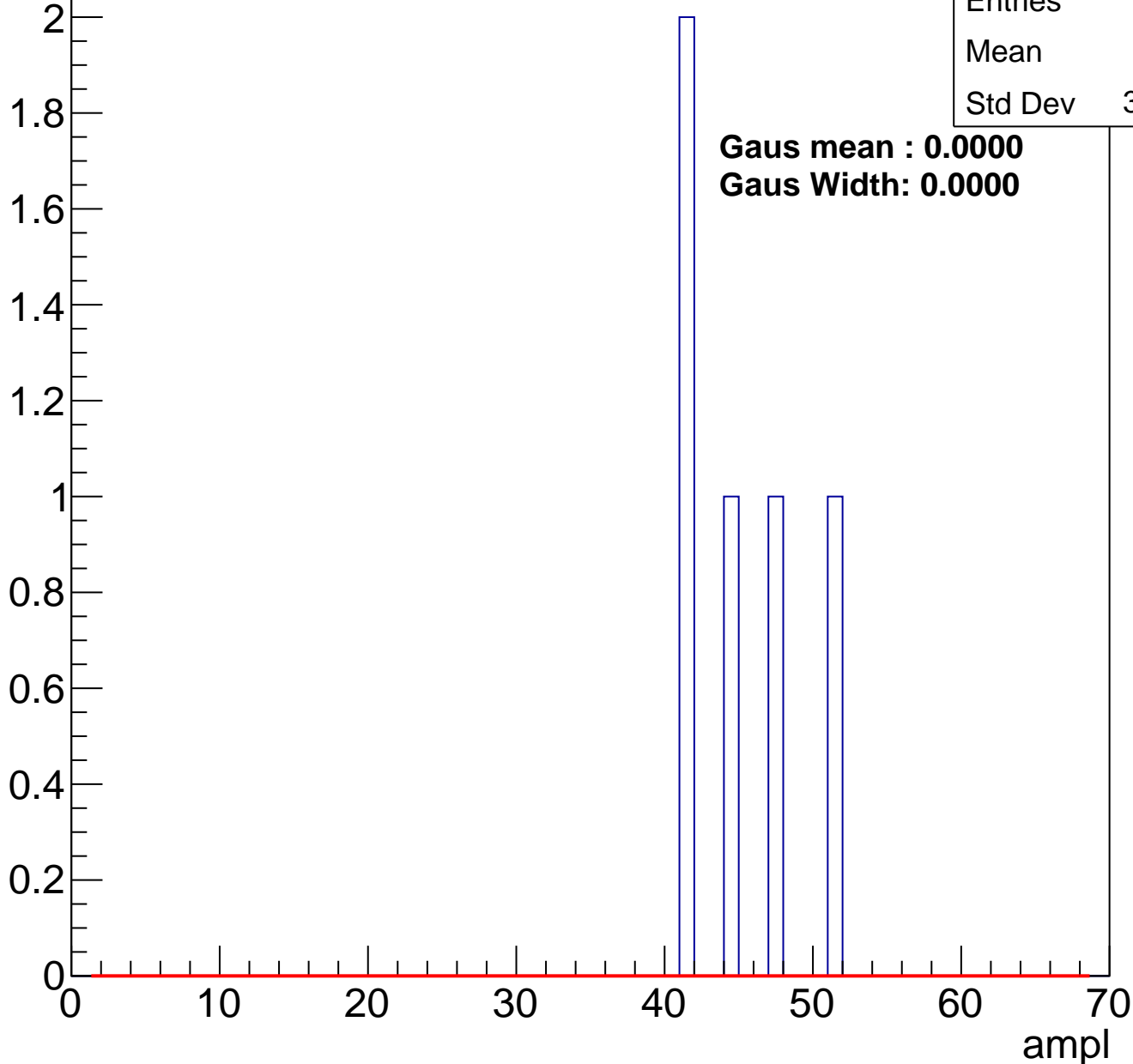


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch47, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	5
Mean	44.8
Std Dev	3.816

B0L100S, U12-ch47, adc1

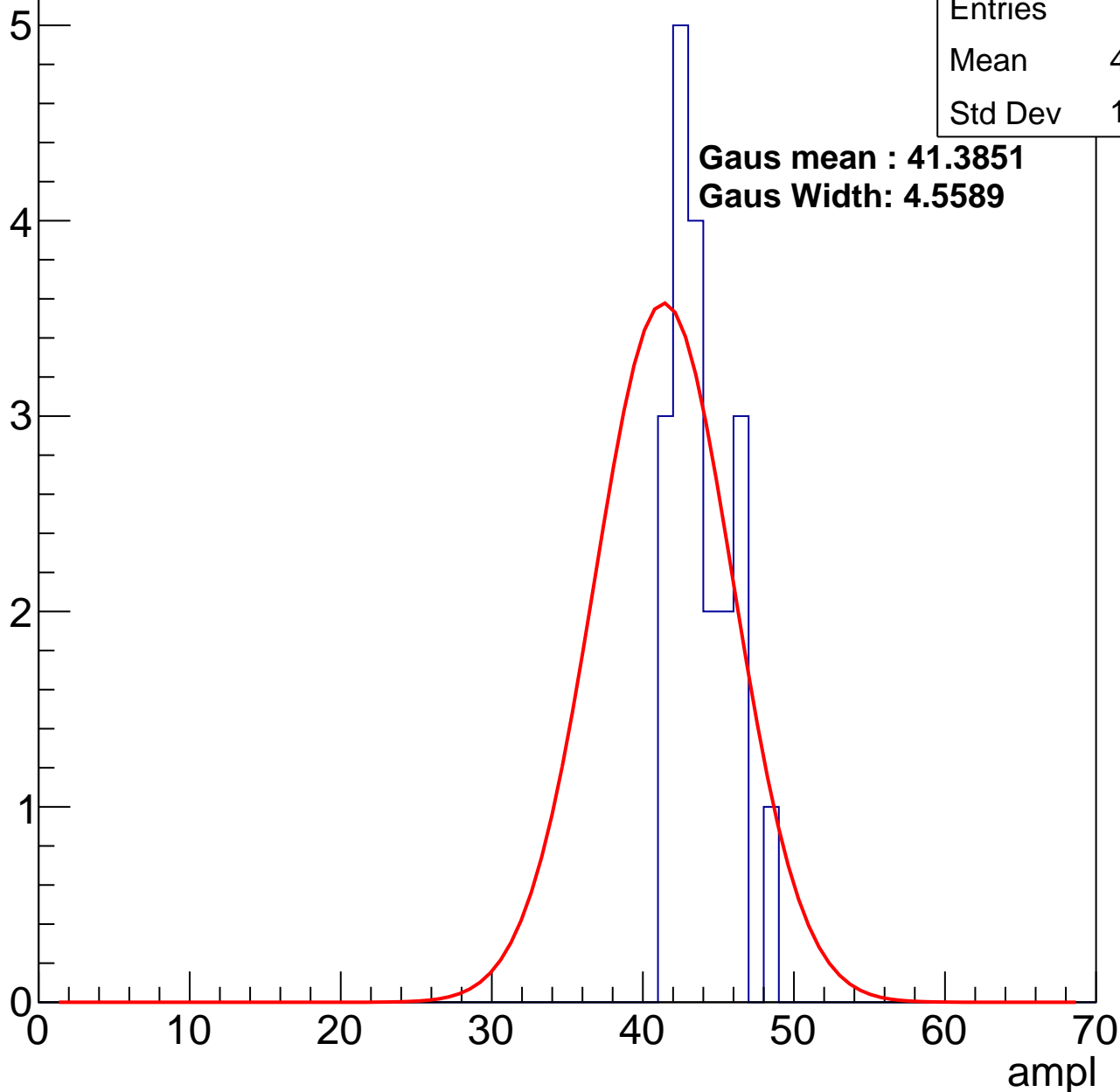
calib_packv5_042523_0143.root, FC#6, port A1

Entry

Entries	20
Mean	43.45
Std Dev	1.936

Gaus mean : 41.3851

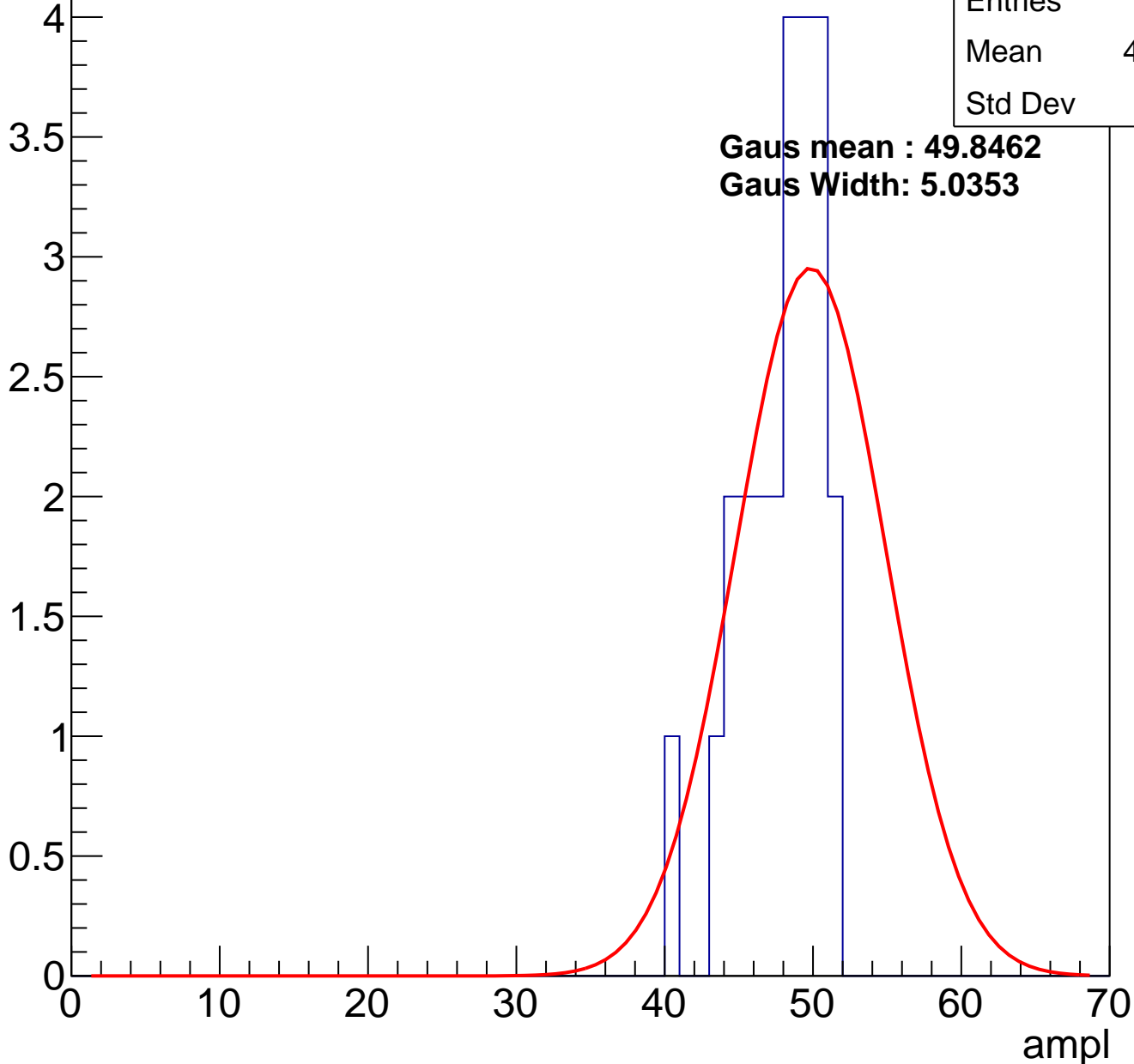
Gaus Width: 4.5589



B0L100S, U12-ch47, adc2

calib_packv5_042523_0143.root, FC#6, port A1

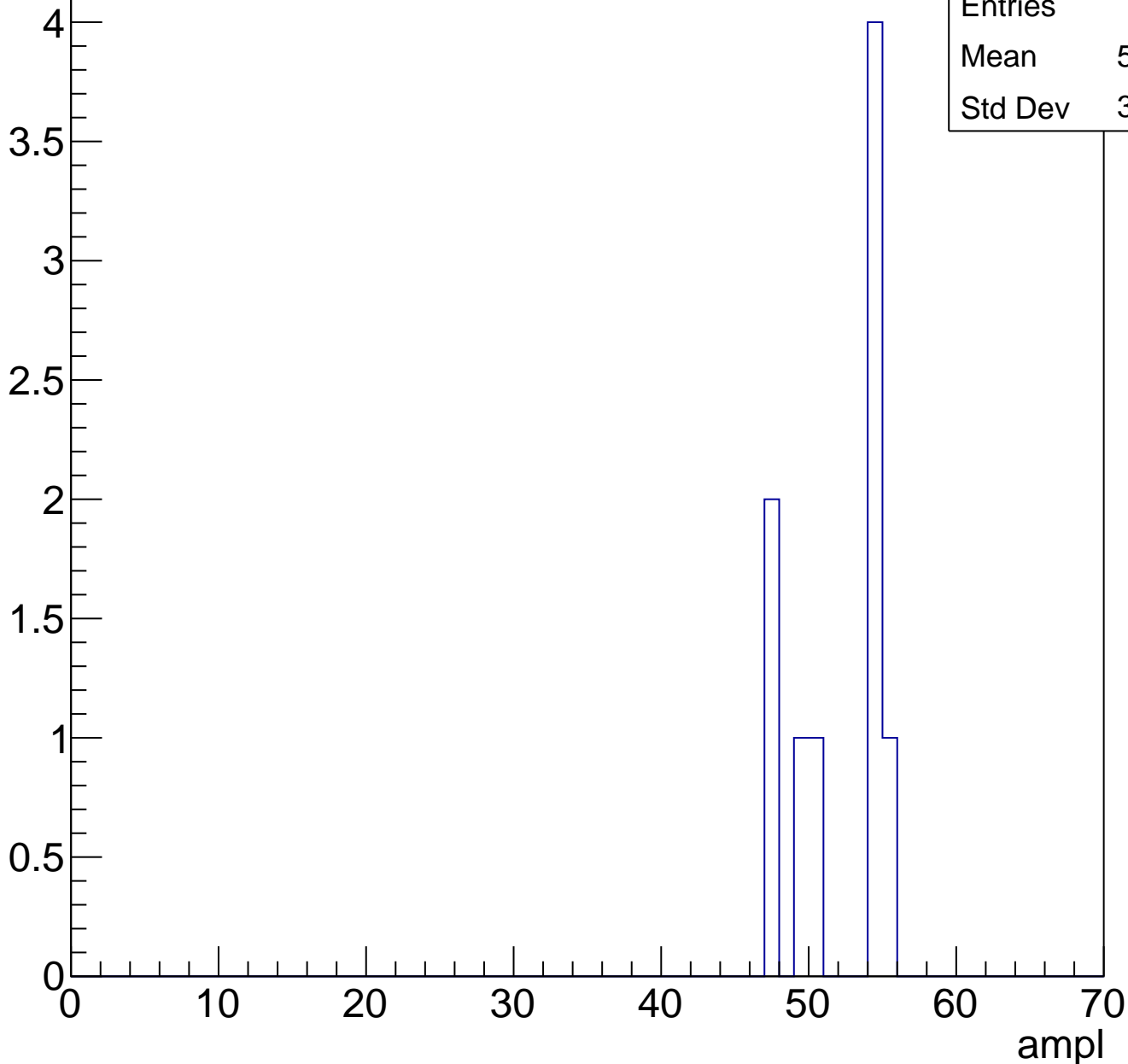
Entry



B0L100S, U12-ch47, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch47, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch47, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch47, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch47, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch48, adc0

calib_packv5_042523_0143.root, FC#6, port A1

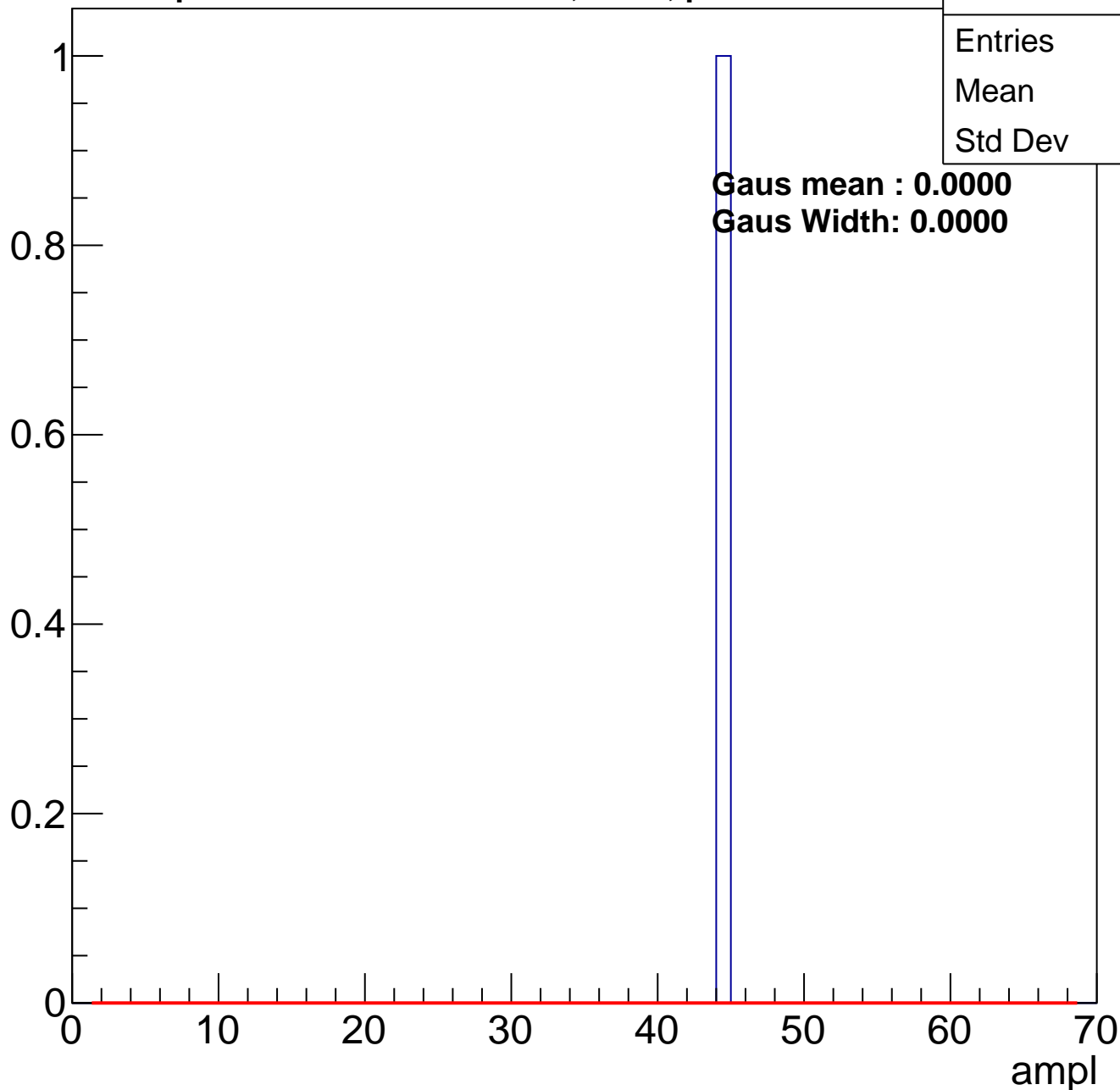
Entry



B0L100S, U12-ch48, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	1
Mean	44
Std Dev	0

B0L100S, U12-ch48, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch48, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch48, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch48, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch48, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch48, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch49, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch49, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch49, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch49, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch49, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch49, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch49, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch49, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch50, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch50, adc1

calib_packv5_042523_0143.root, FC#6, port A1

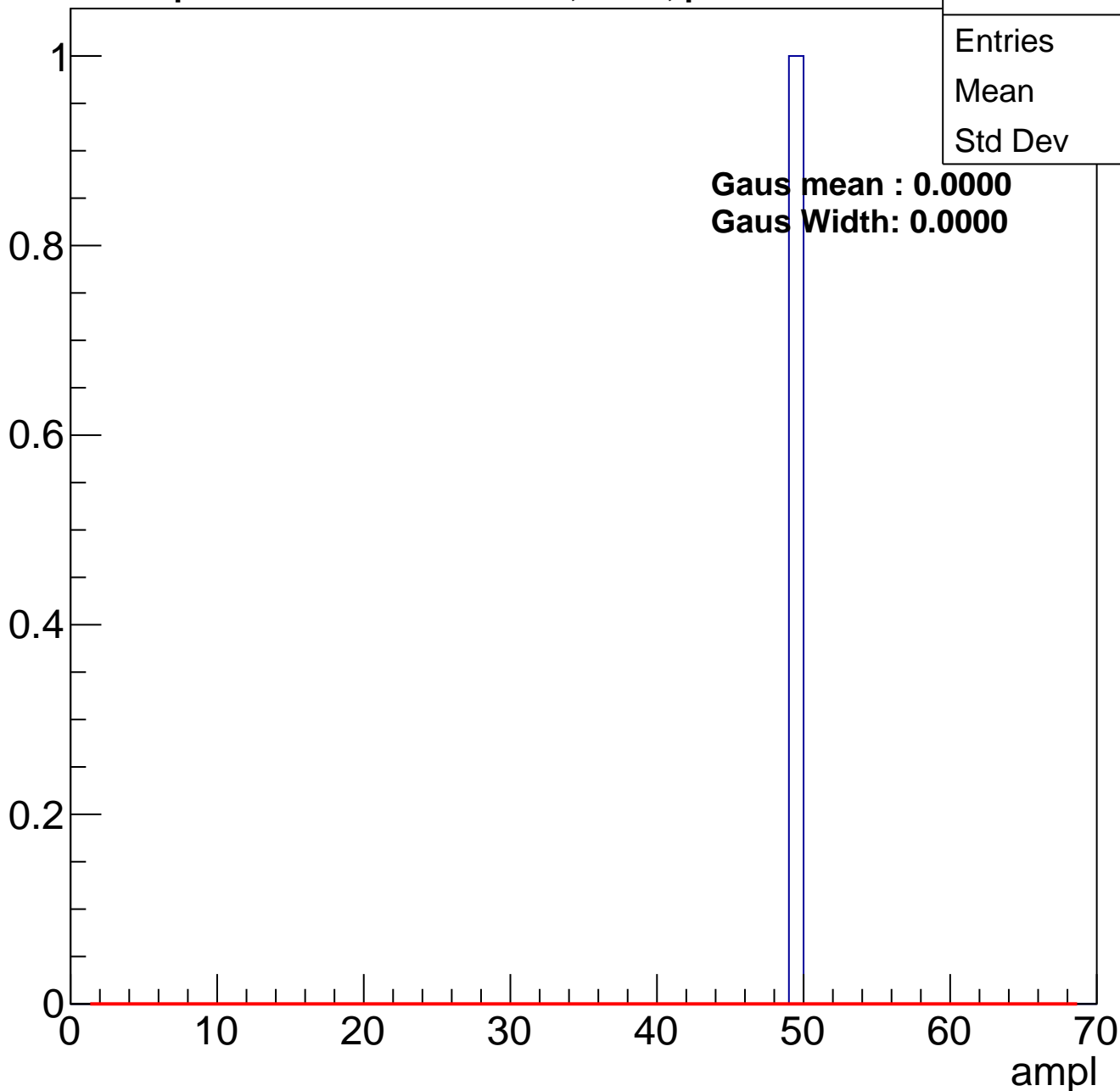
Entry



B0L100S, U12-ch50, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	1
Mean	49
Std Dev	0

B0L100S, U12-ch50, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch50, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch50, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch50, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch50, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch51, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch51, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry

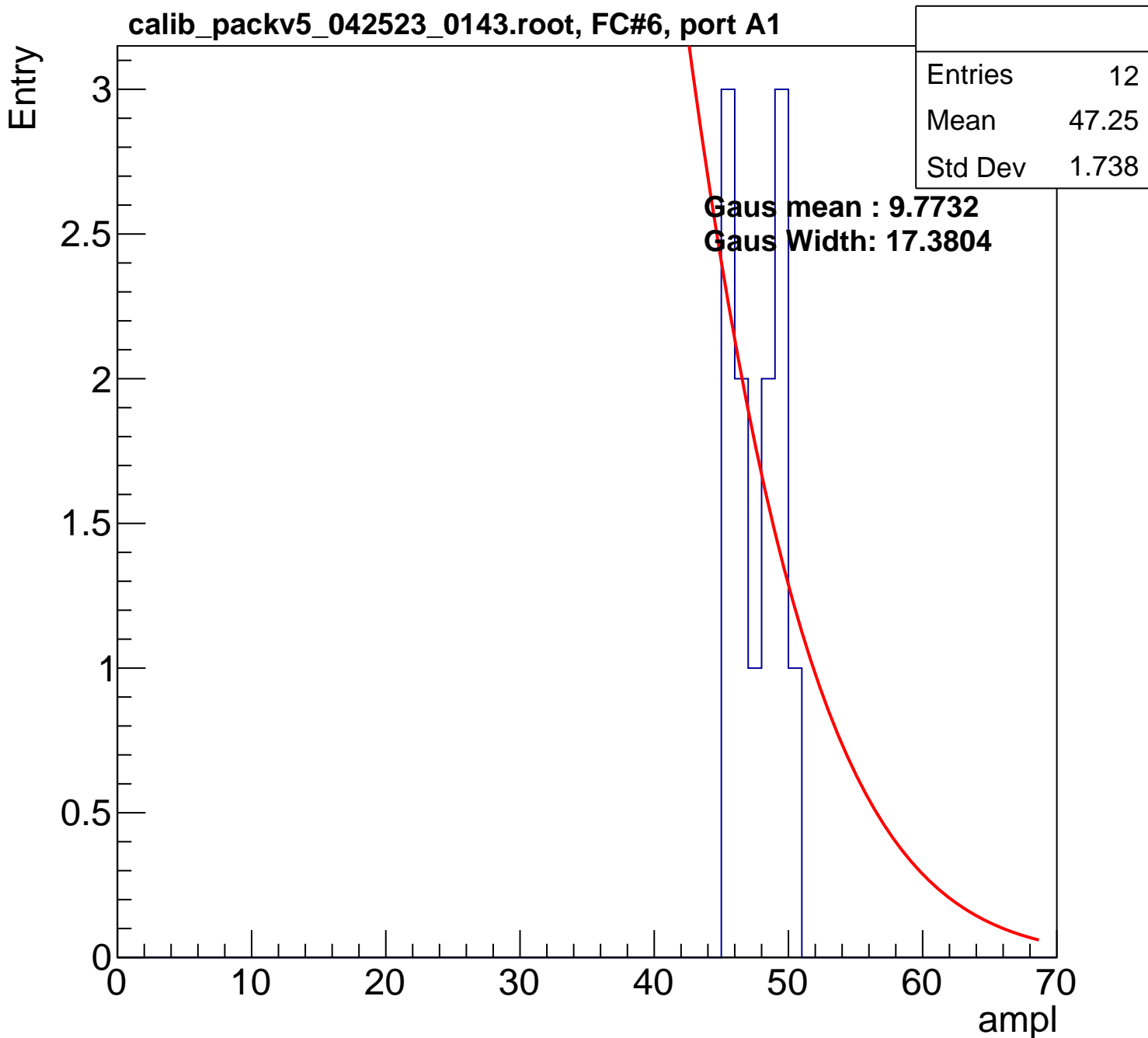
3
2.5
2
1.5
1
0.5
0

Entries	12
Mean	47.25
Std Dev	1.738

Gaus mean : 9.7732
Gaus Width: 17.3804

ampl

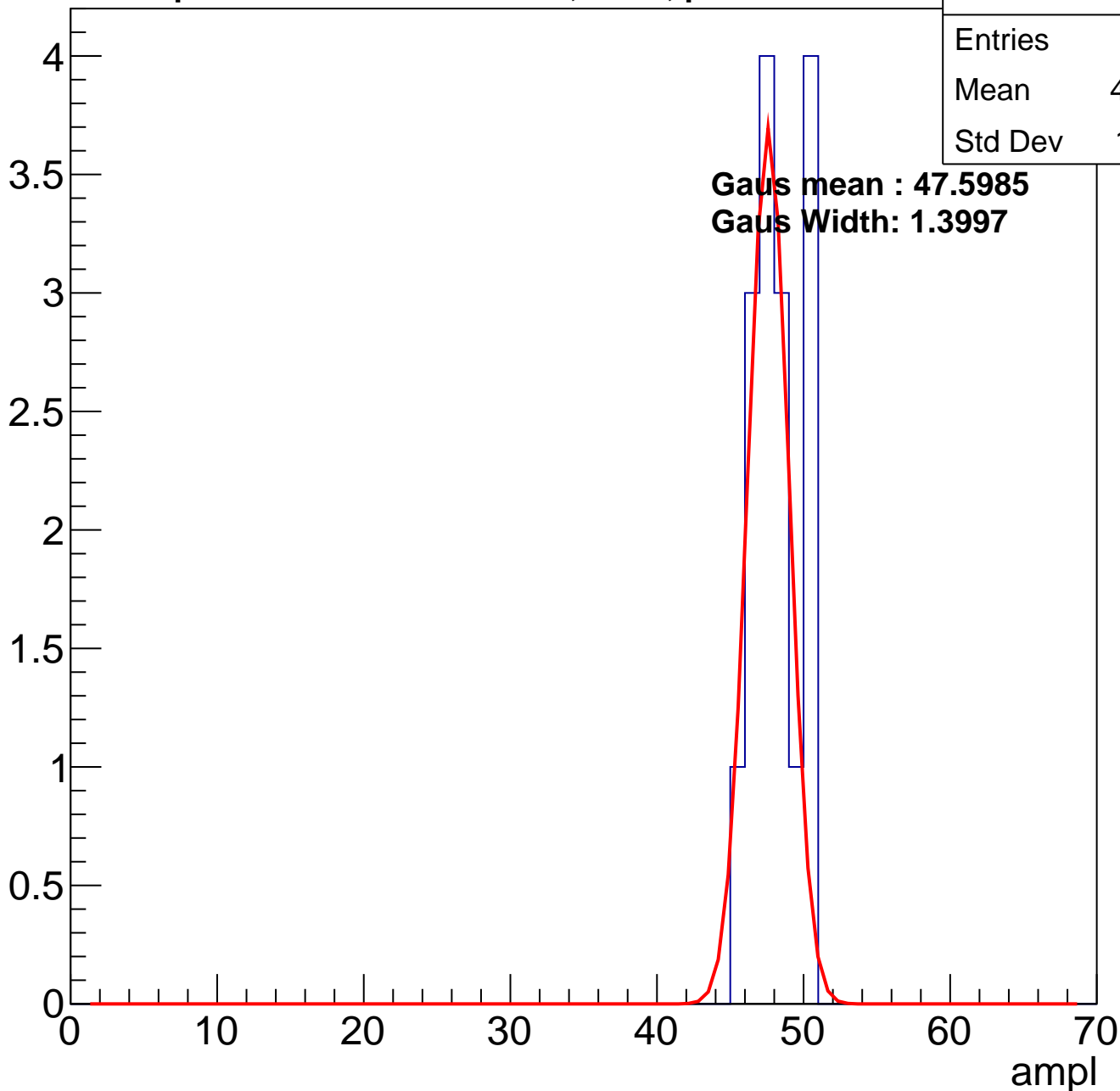
0 10 20 30 40 50 60 70



B0L100S, U12-ch51, adc2

calib_packv5_042523_0143.root, FC#6, port A1

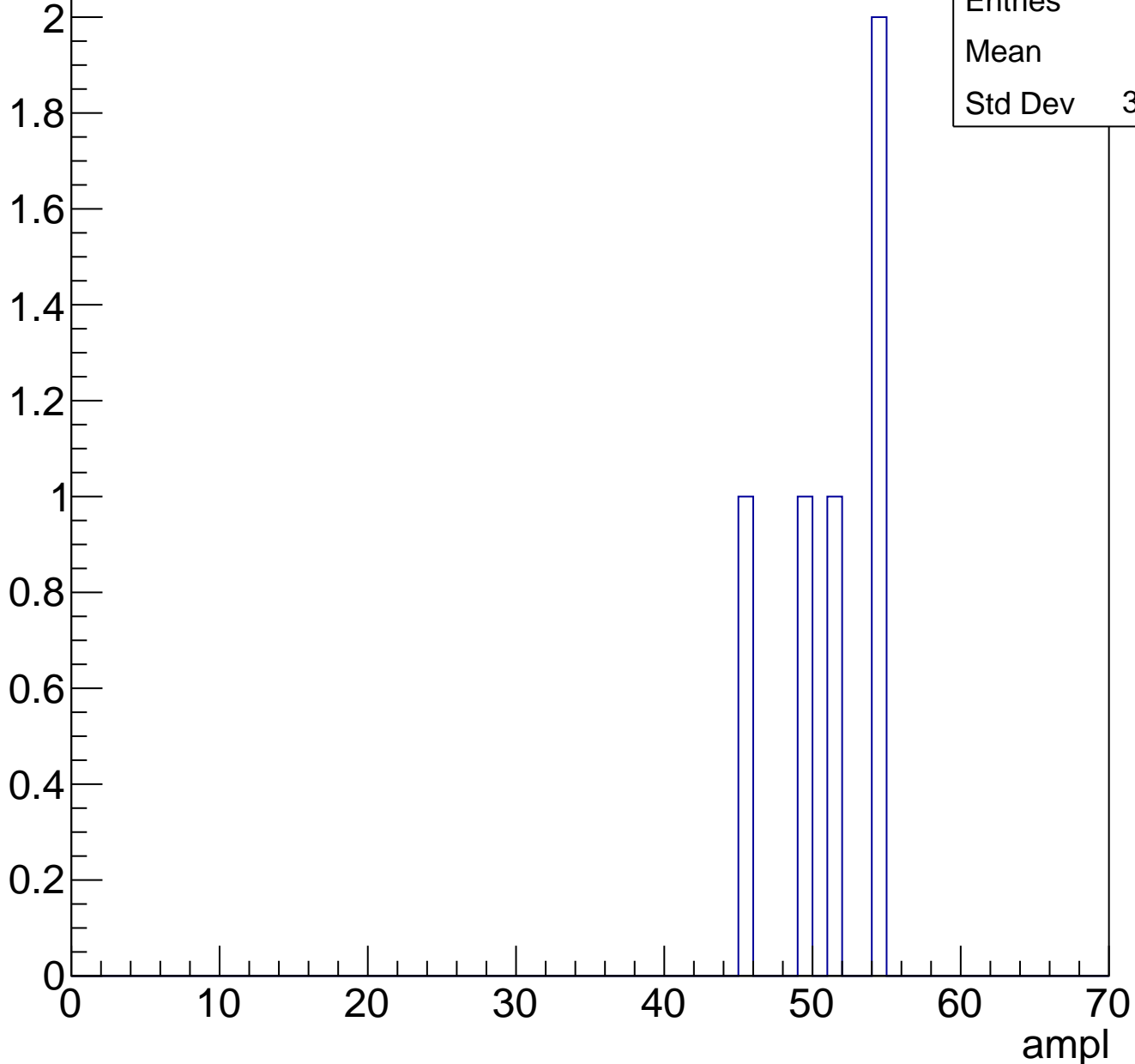
Entry



B0L100S, U12-ch51, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch51, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch51, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch51, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch51, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch52, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch52, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch52, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch52, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch52, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch52, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch52, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch52, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch53, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch53, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch53, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch53, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch53, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch53, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch53, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch53, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch54, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch54, adc1

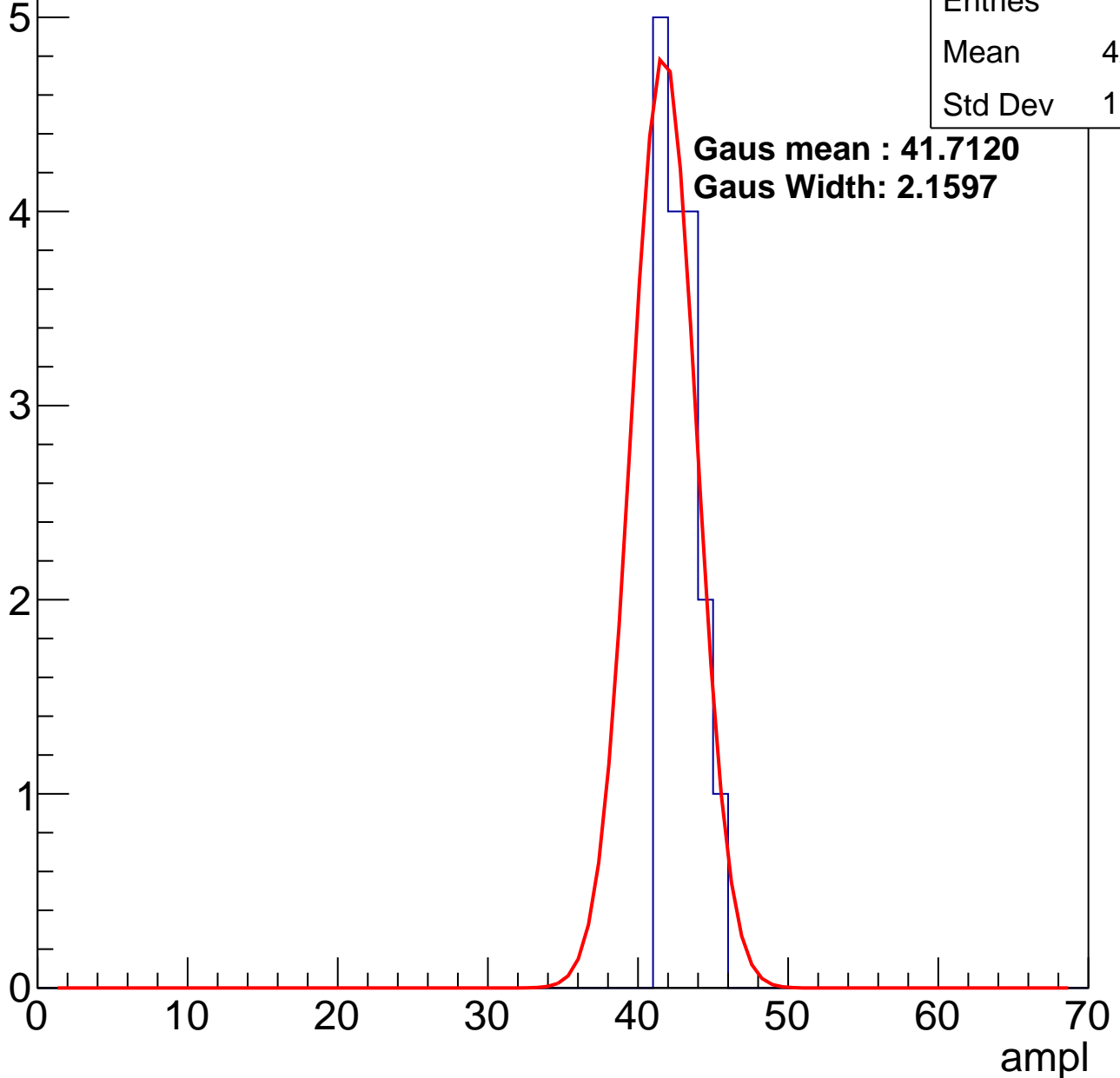
calib_packv5_042523_0143.root, FC#6, port A1

Entry

Entries	16
Mean	42.38
Std Dev	1.218

Gaus mean : 41.7120

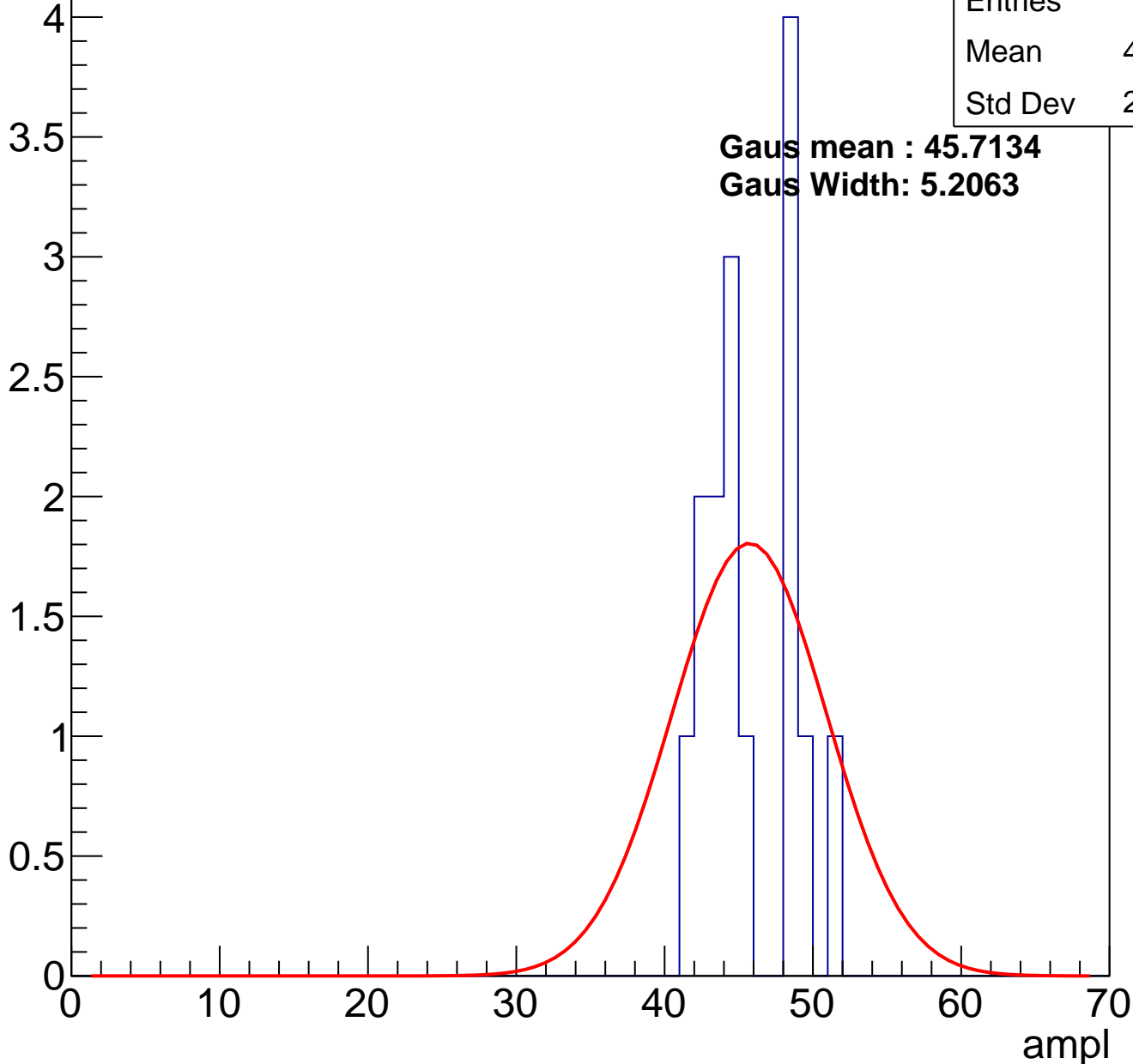
Gaus Width: 2.1597



B0L100S, U12-ch54, adc2

calib_packv5_042523_0143.root, FC#6, port A1

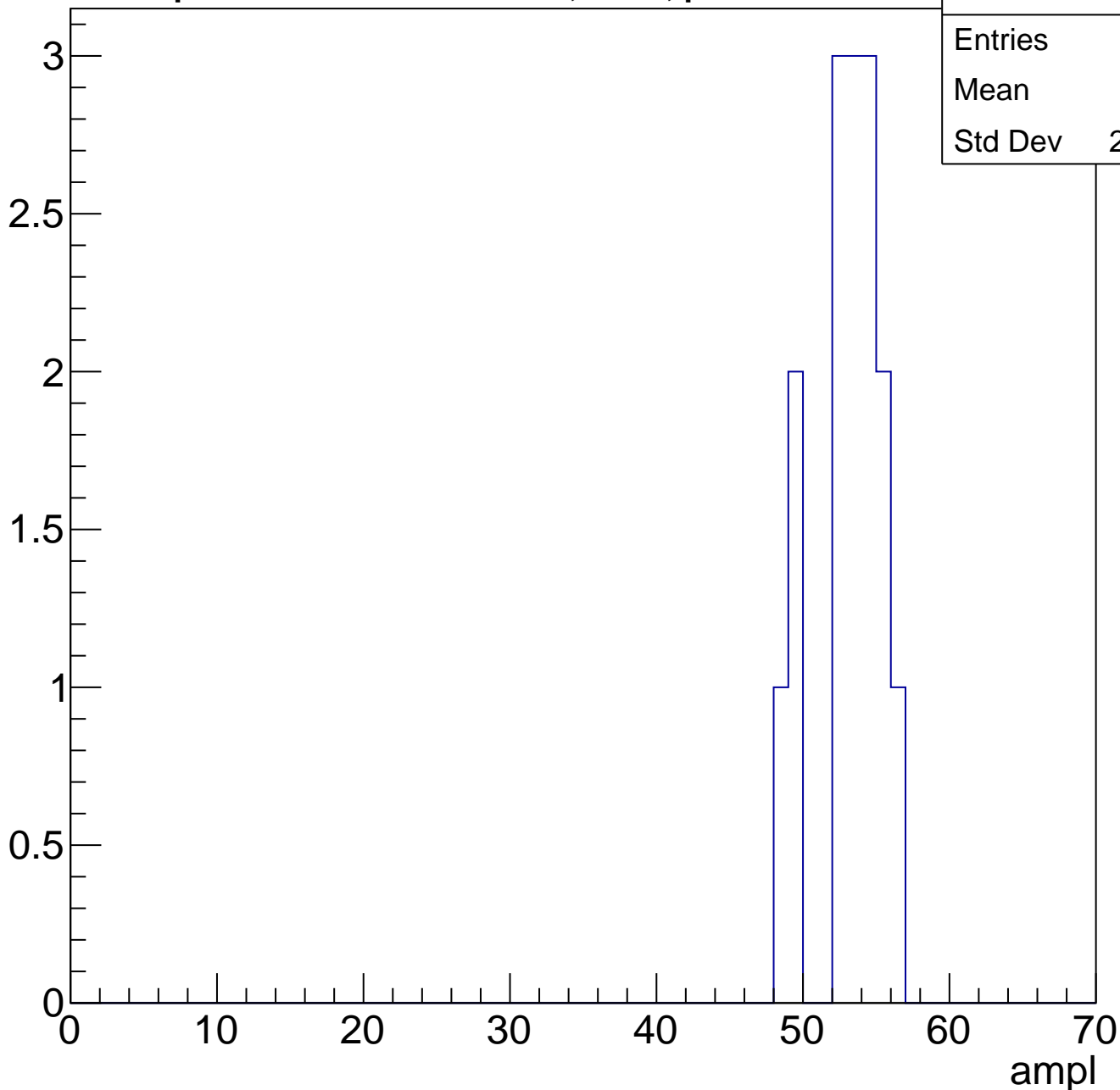
Entry



B0L100S, U12-ch54, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry

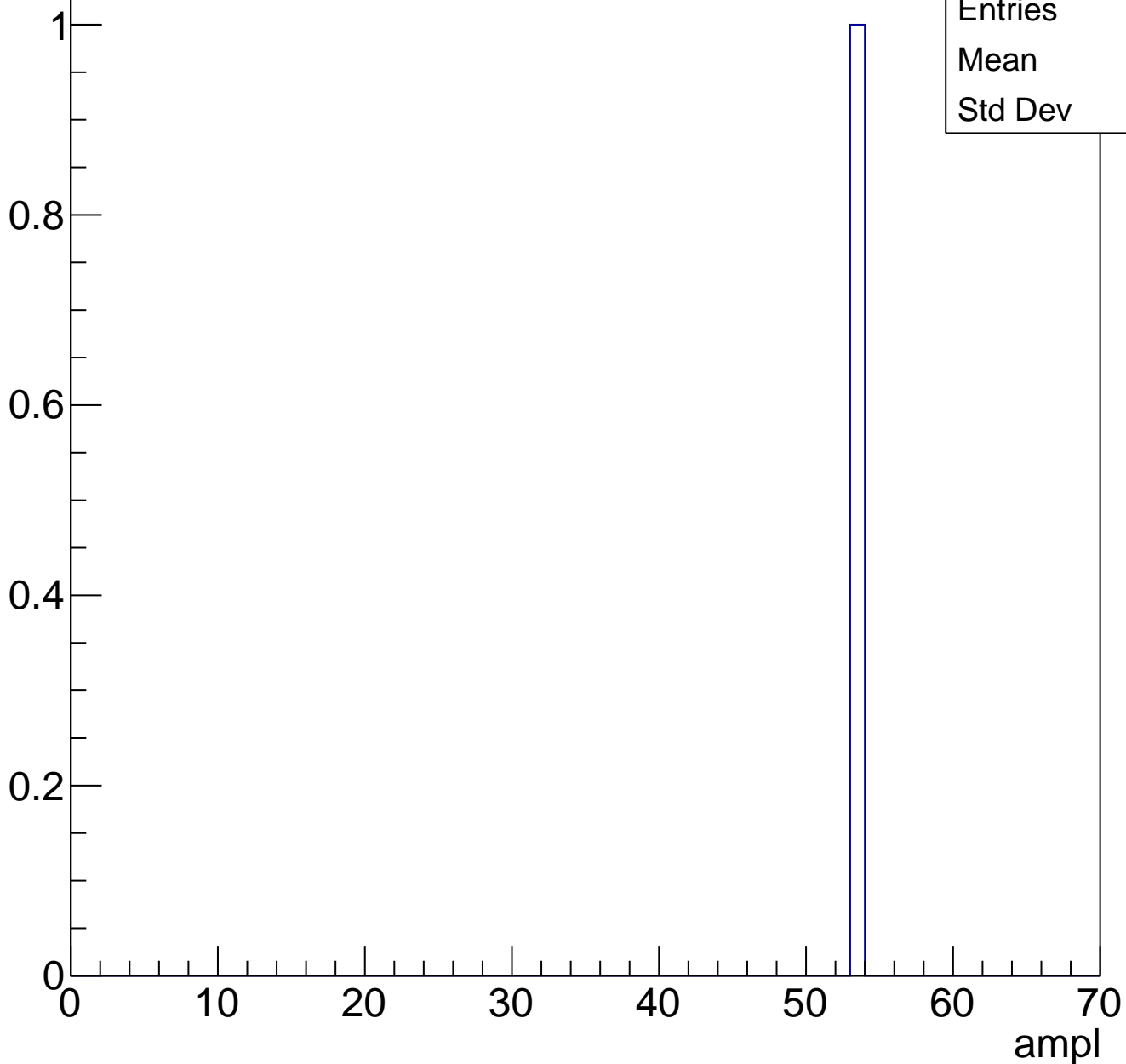


Entries	15
Mean	52.6
Std Dev	2.274

B0L100S, U12-ch54, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch54, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch54, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch54, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry

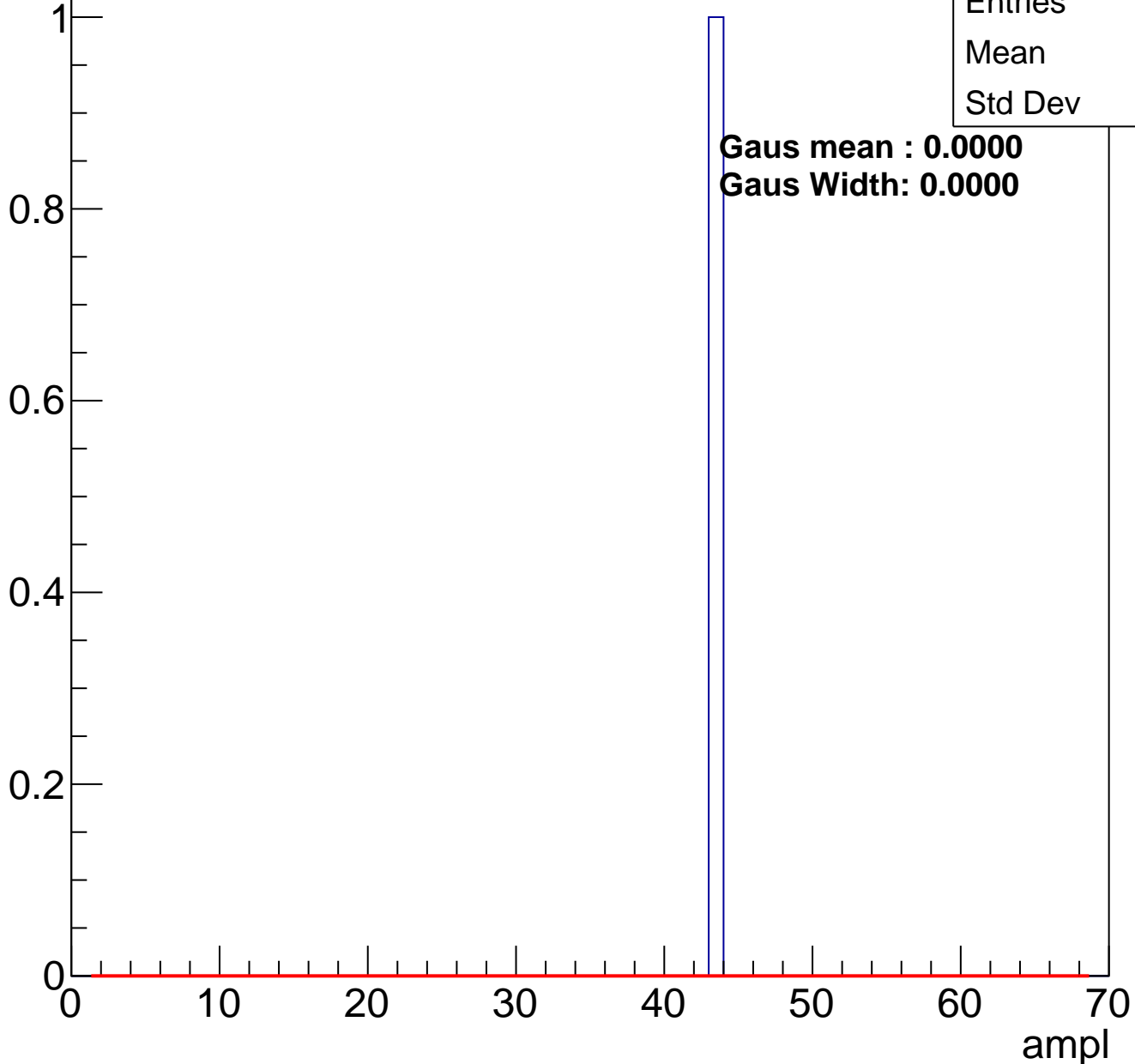


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch55, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	1
Mean	43
Std Dev	0

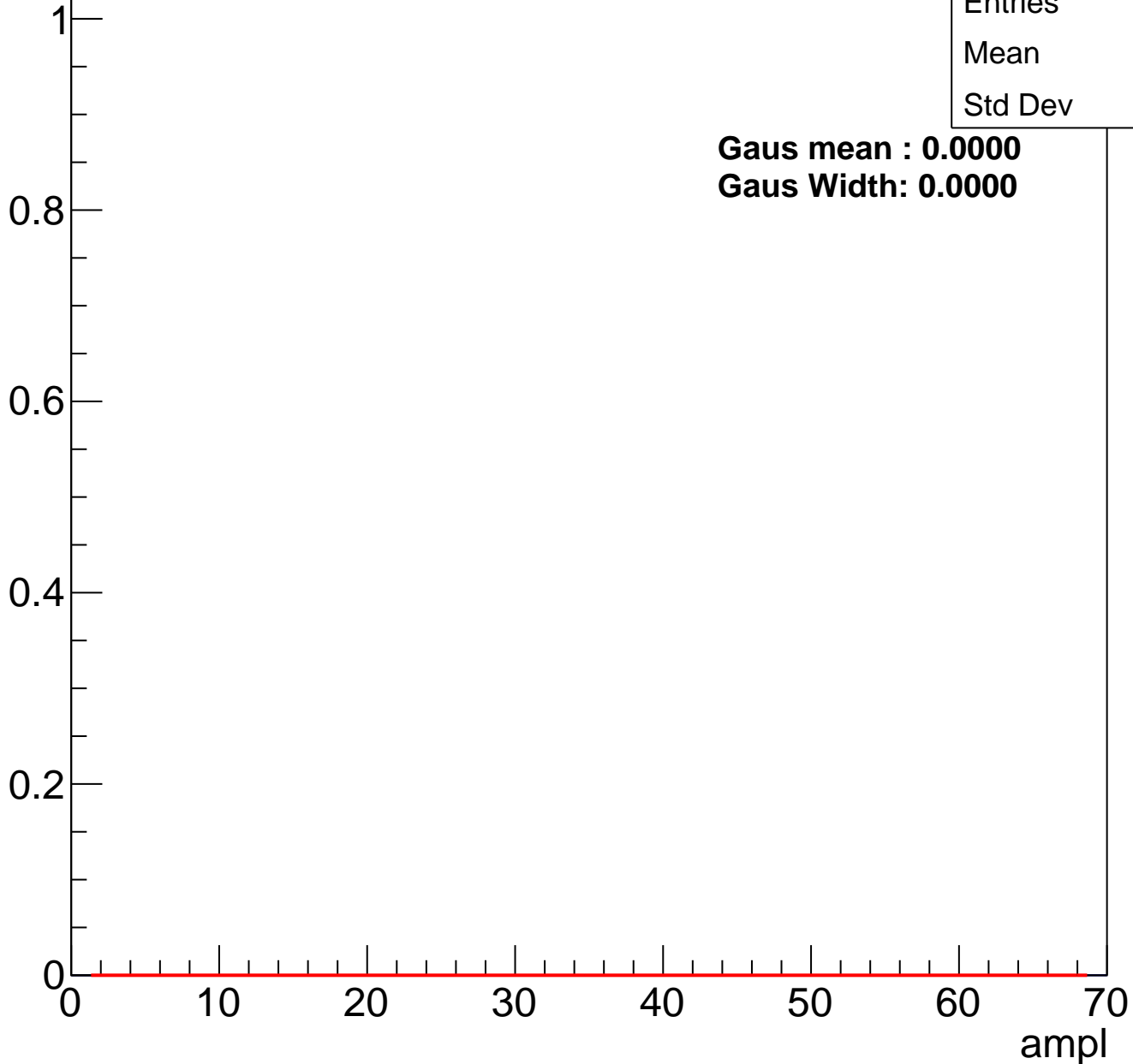
Gaus mean : 0.0000

Gaus Width: 0.0000

B0L100S, U12-ch55, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch55, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

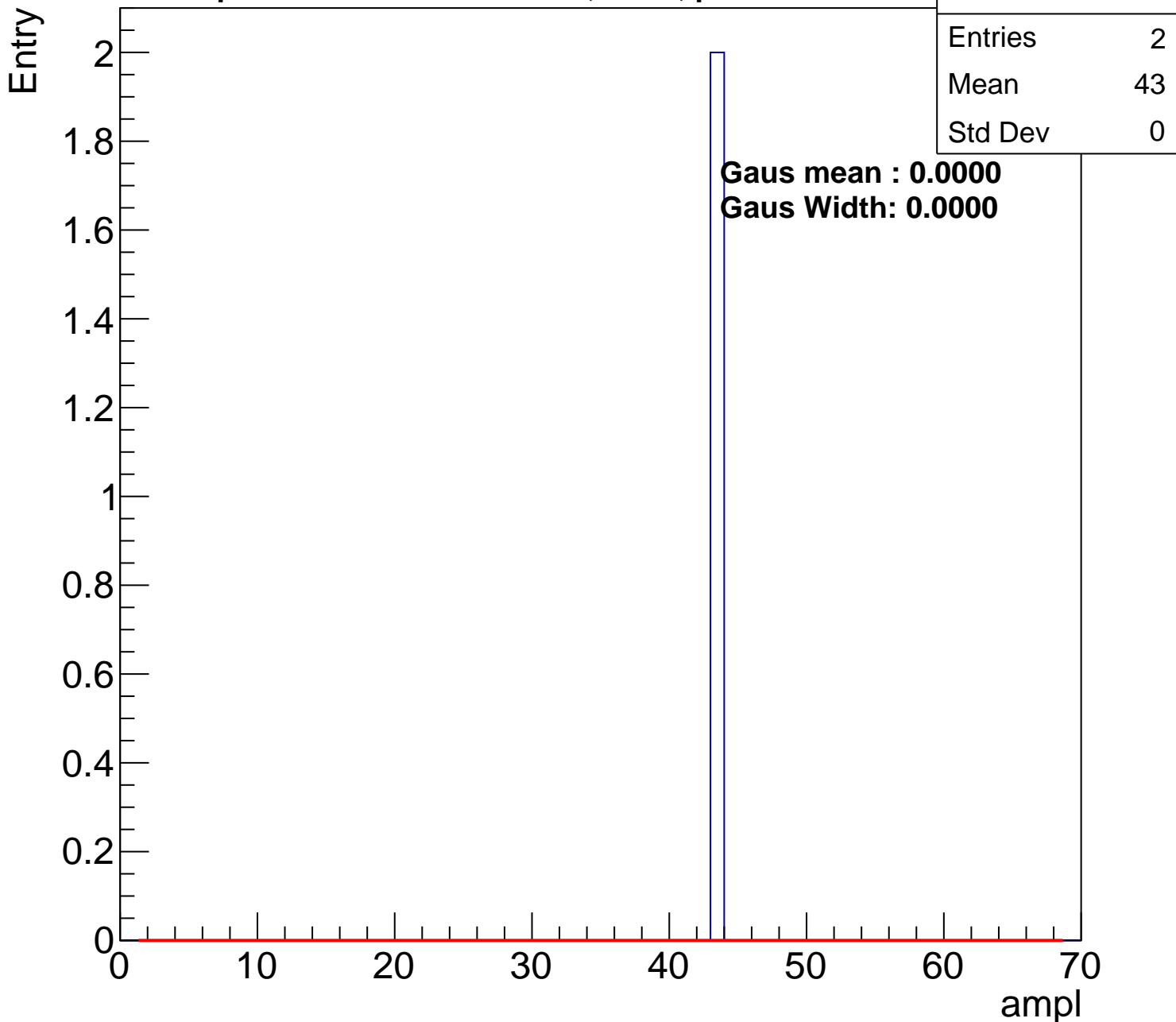
Entries	2
Mean	43
Std Dev	0

Gaus mean : 0.0000

Gaus Width: 0.0000

0 10 20 30 40 50 60 70

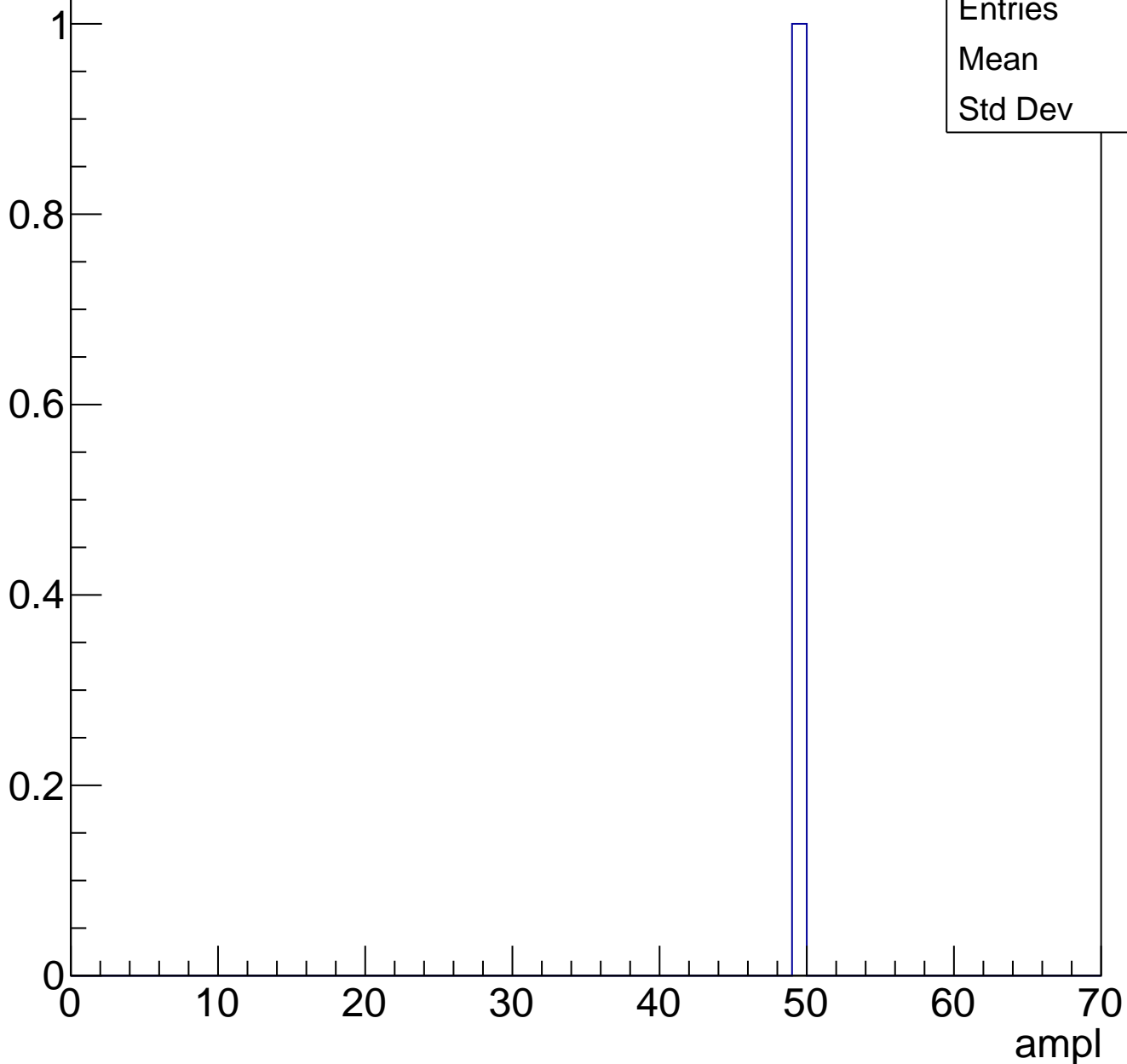
ampl



B0L100S, U12-ch55, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch55, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch55, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch55, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch55, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch56, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch56, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

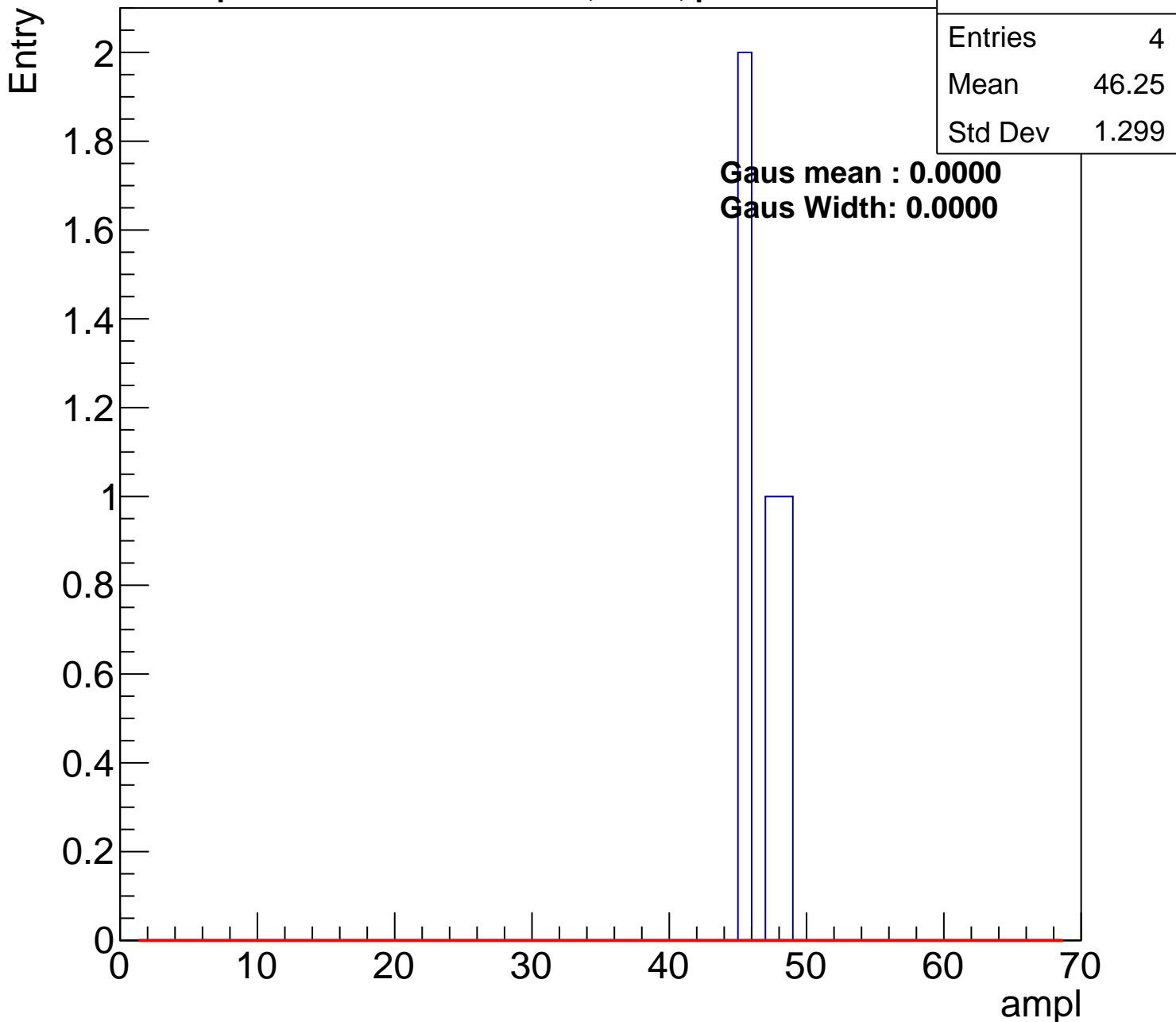
Entries	4
Mean	46.25
Std Dev	1.299

Gaus mean : 0.0000

Gaus Width: 0.0000

0 10 20 30 40 50 60 70

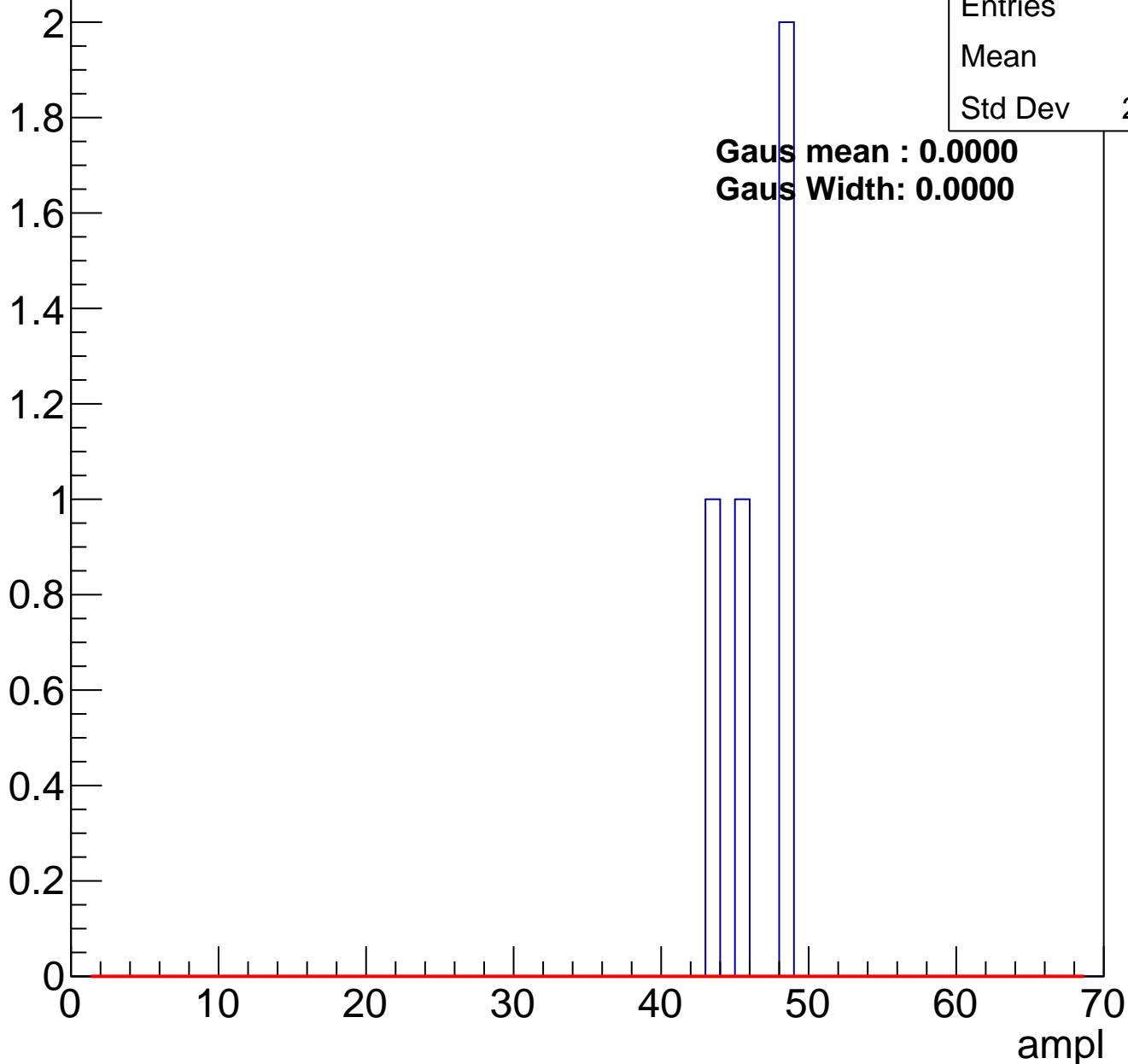
ampl



B0L100S, U12-ch56, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

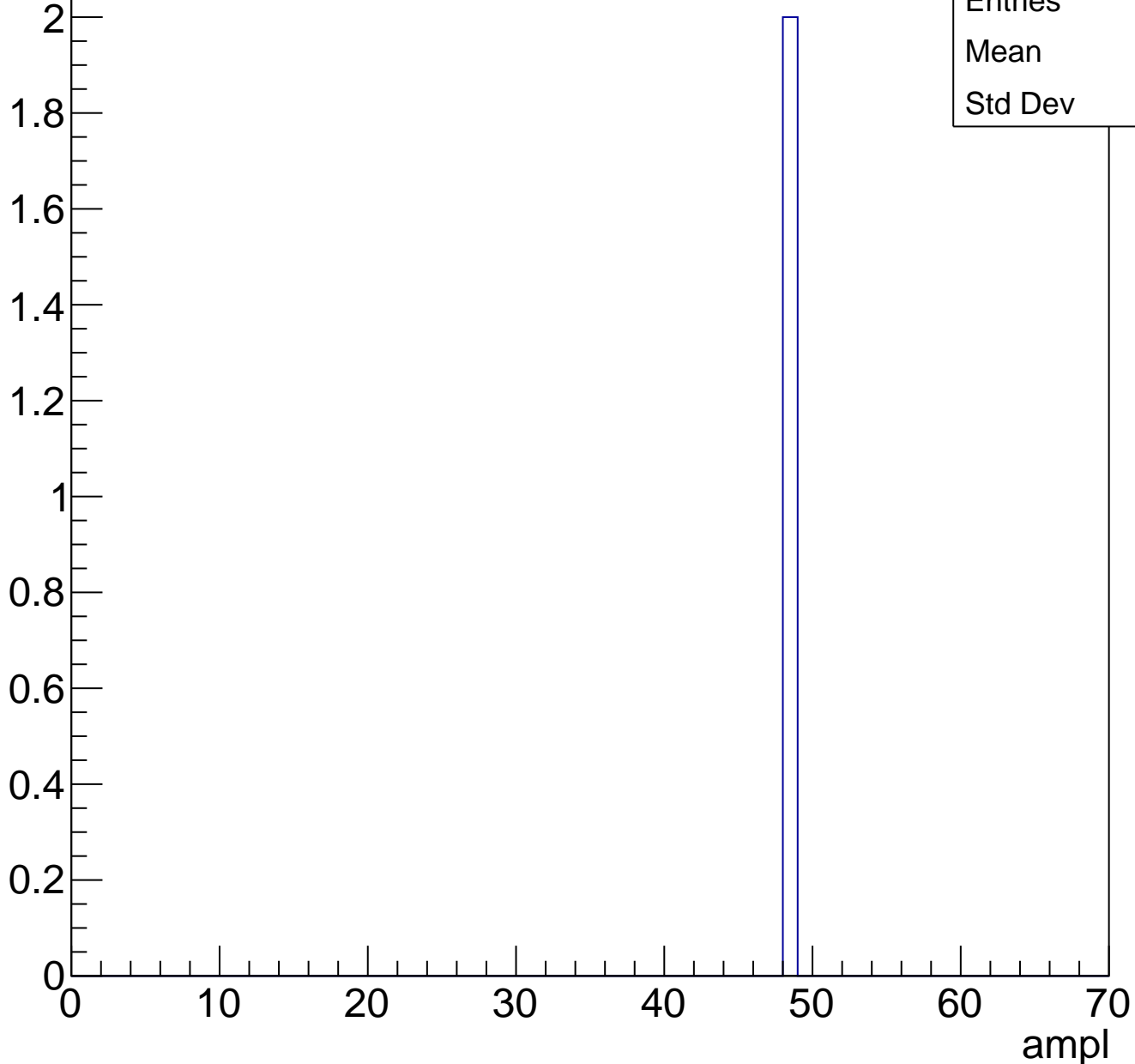


Entries	4
Mean	46
Std Dev	2.121

B0L100S, U12-ch56, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	2
Mean	48
Std Dev	0

B0L100S, U12-ch56, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch56, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch56, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch56, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch57, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch57, adc1

calib_packv5_042523_0143.root, FC#6, port A1

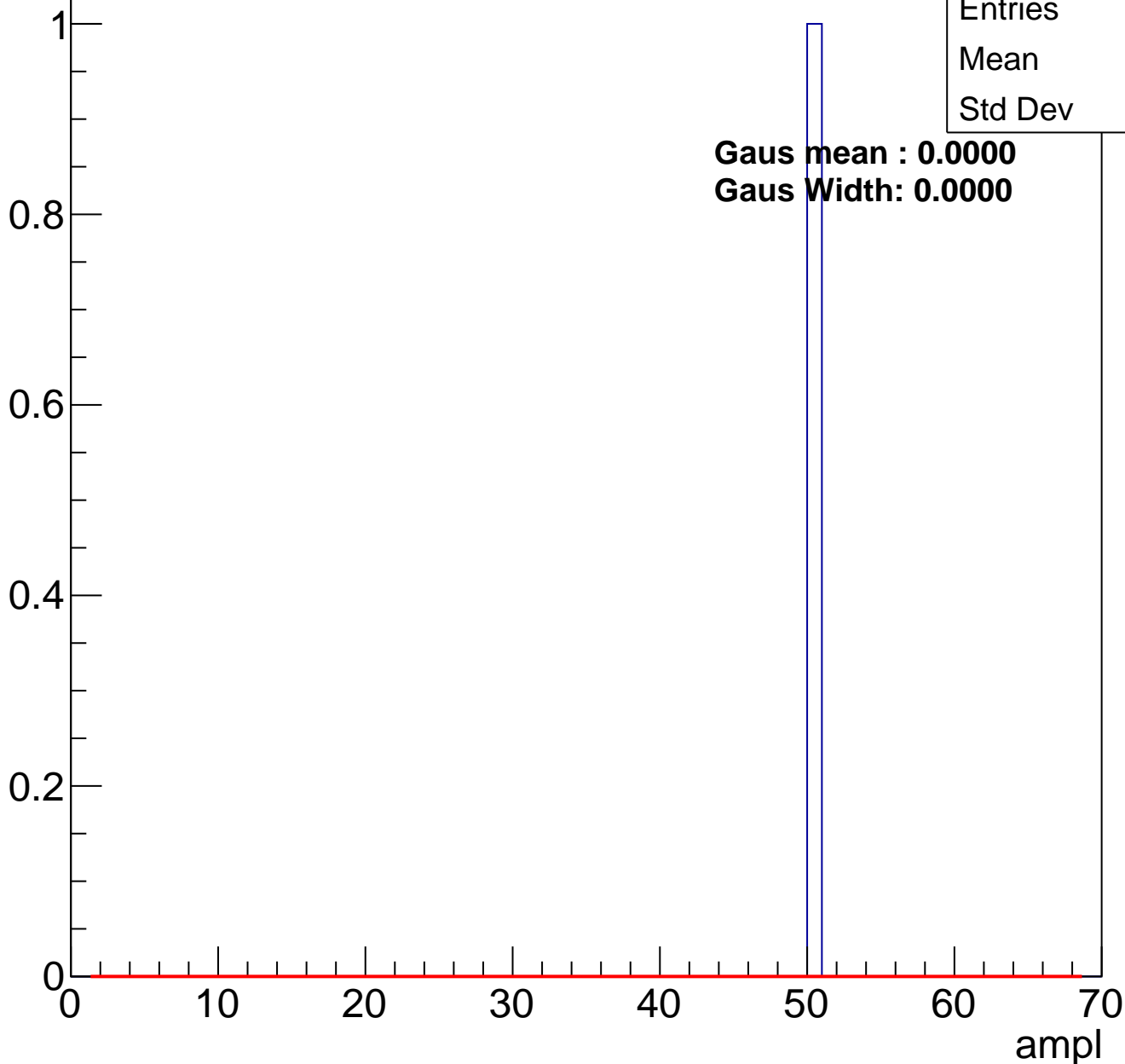
Entry



B0L100S, U12-ch57, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

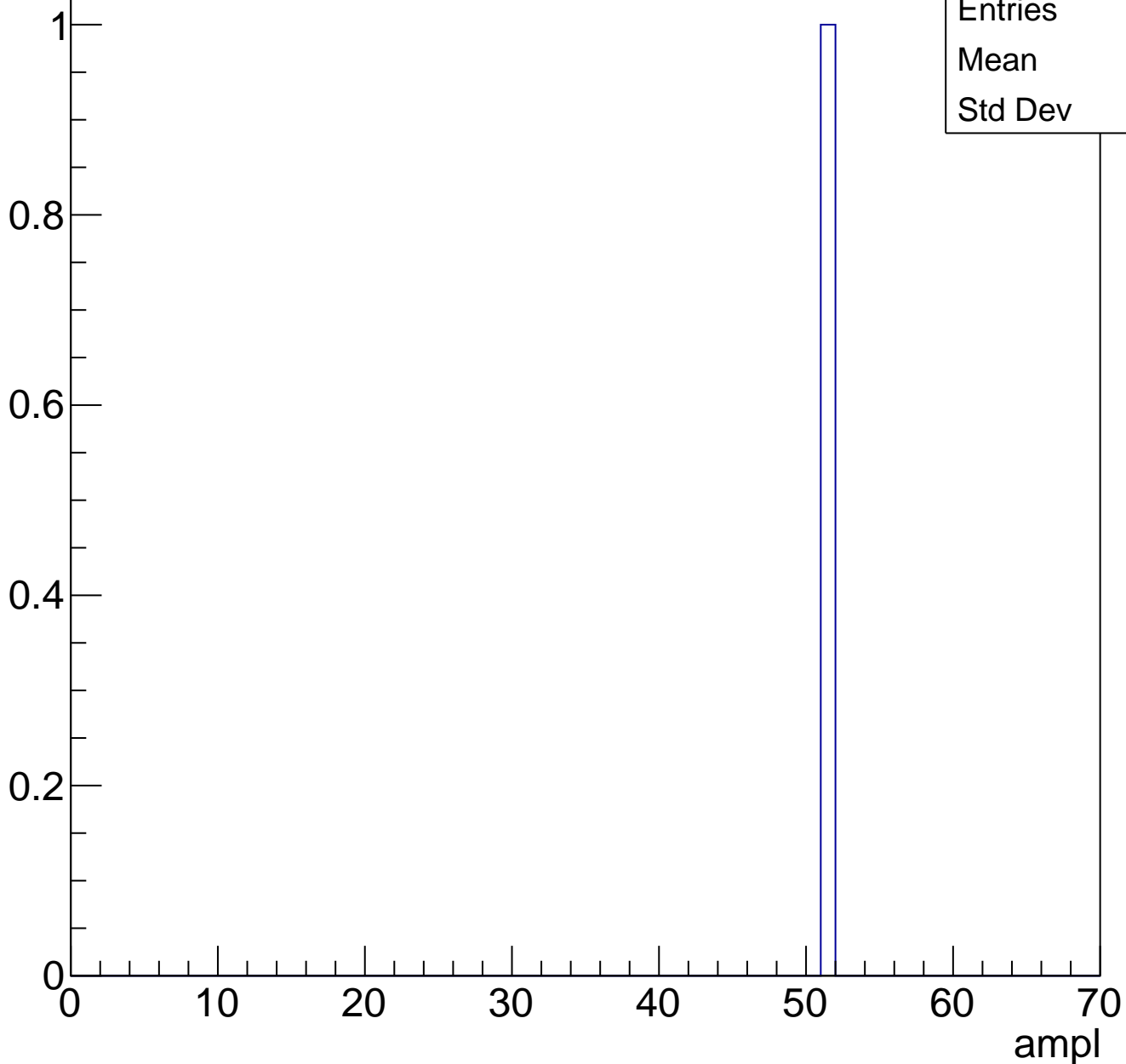


Entries	1
Mean	50
Std Dev	0

B0L100S, U12-ch57, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch57, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch57, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch57, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch57, adc7

calib_packv5_042523_0143.root, FC#6, port A1

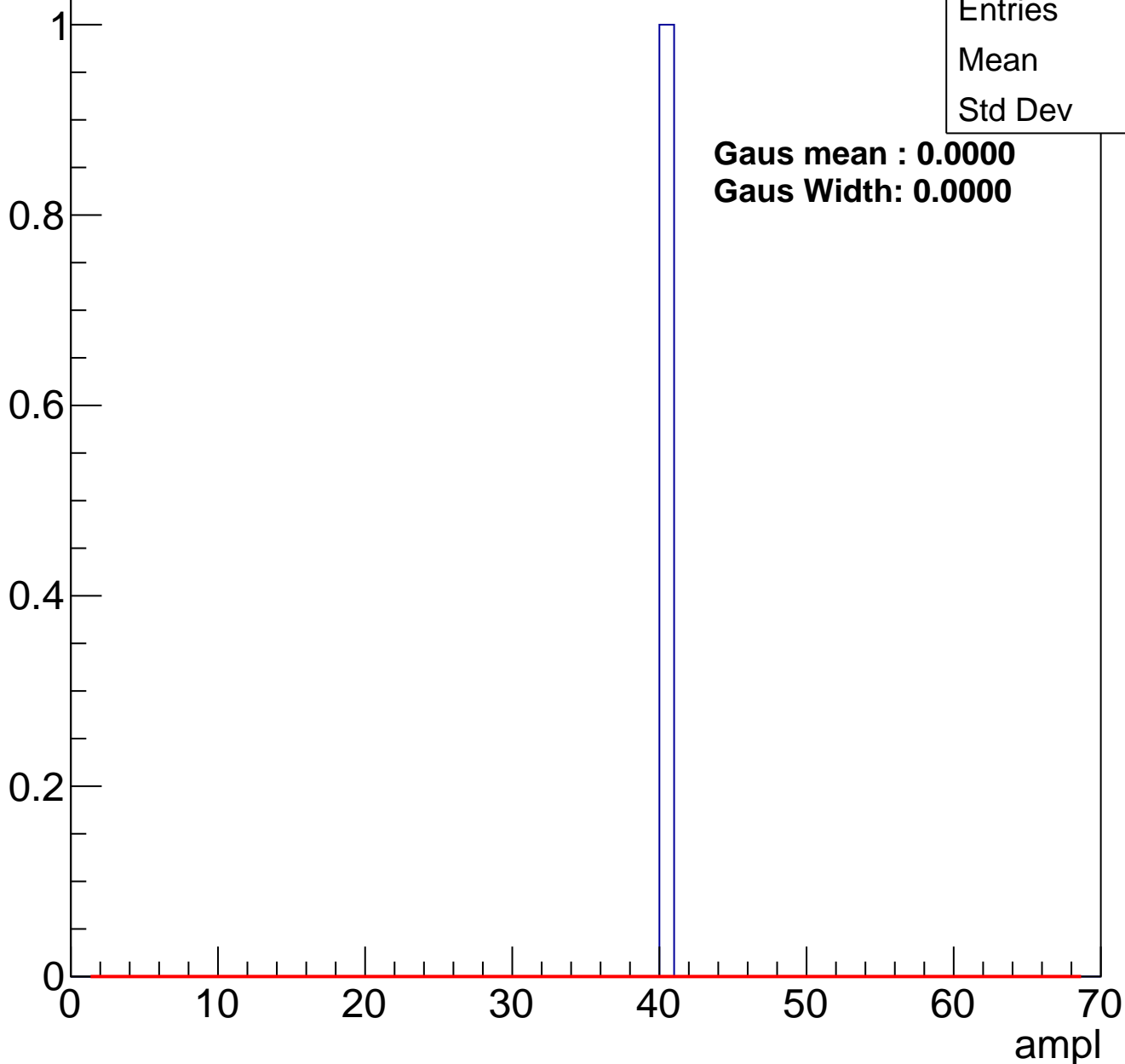
Entry



B0L100S, U12-ch58, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch58, adc1

calib_packv5_042523_0143.root, FC#6, port A1

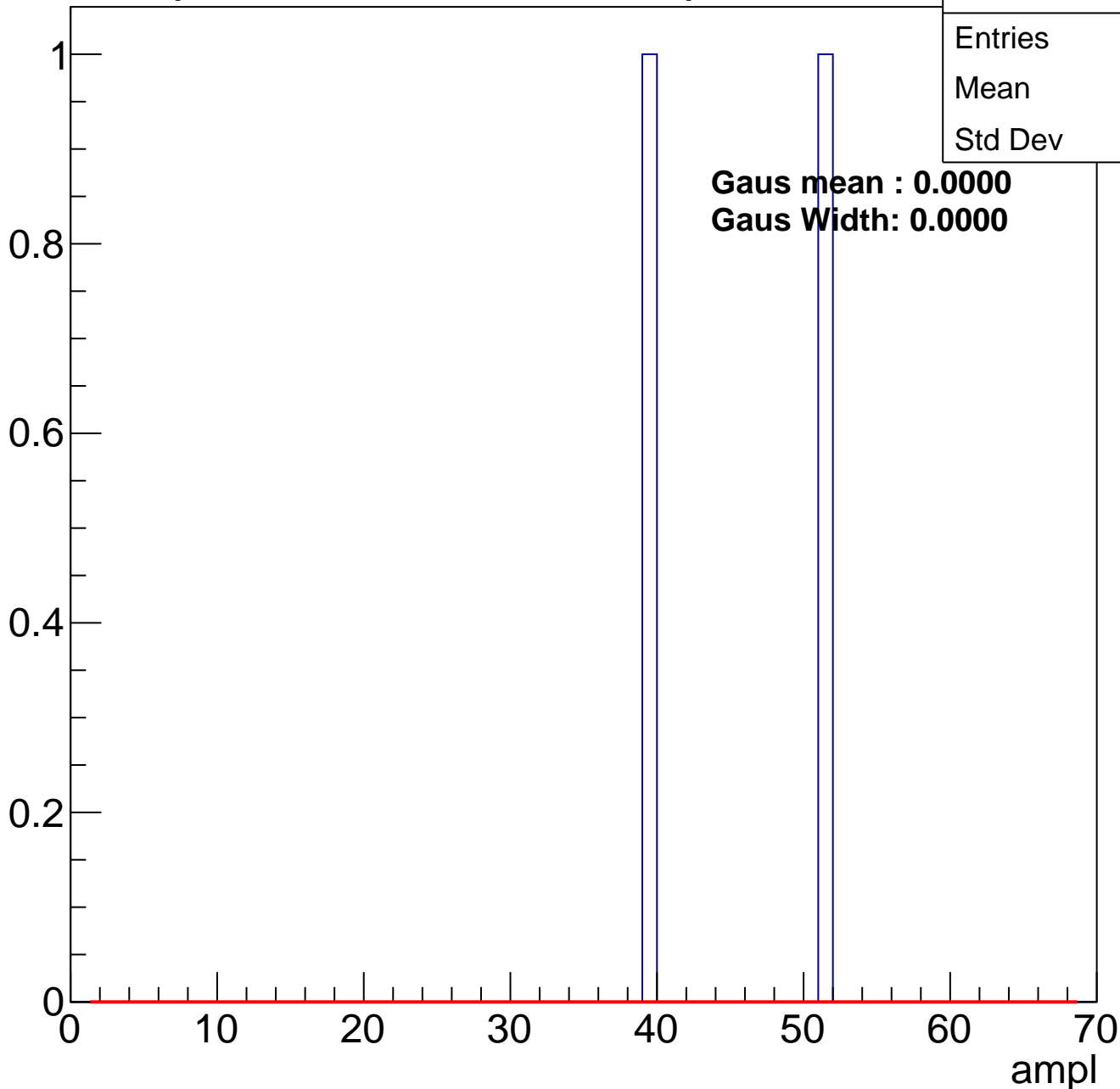
Entry



B0L100S, U12-ch58, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

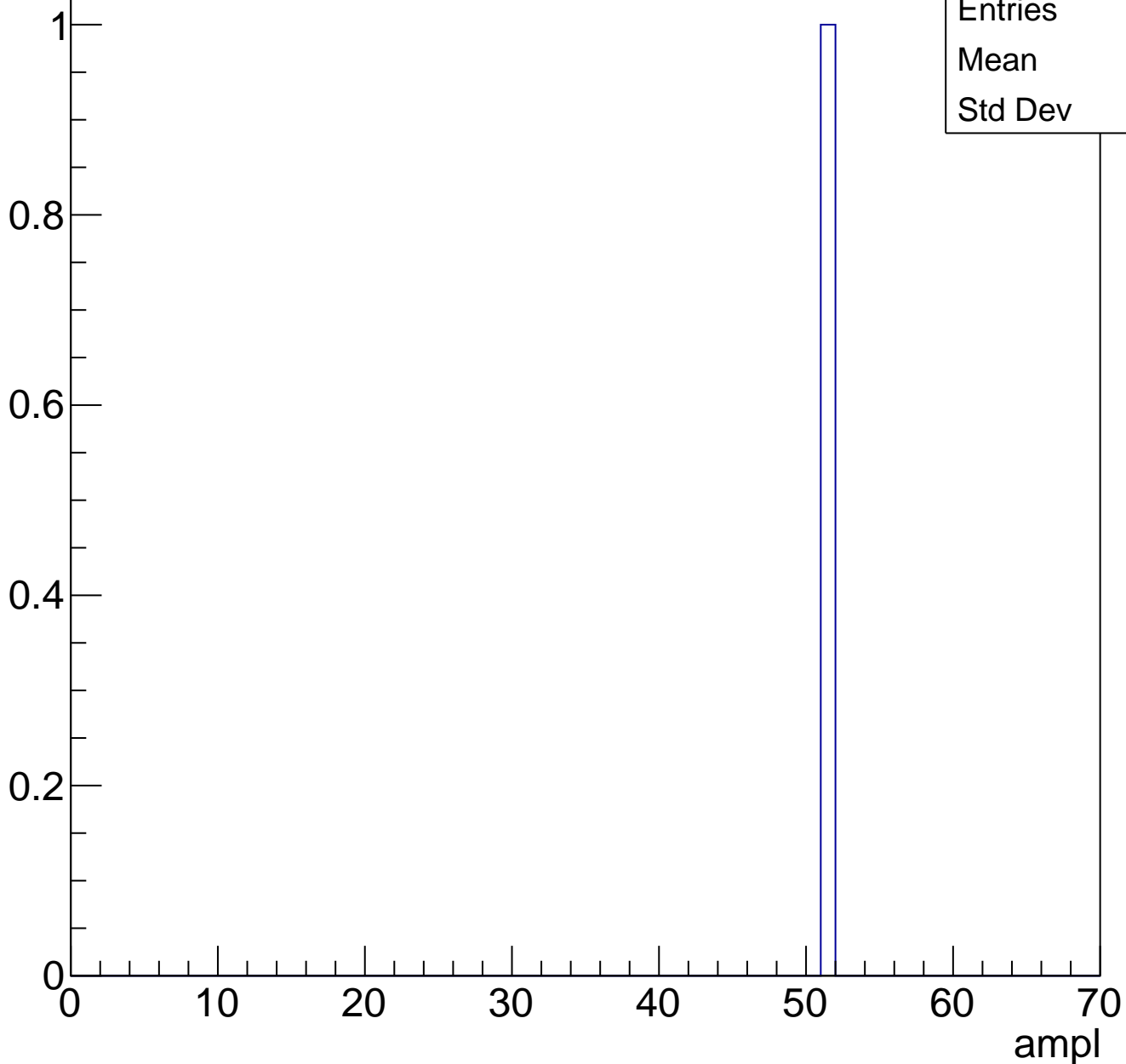


Entries	2
Mean	45
Std Dev	6

B0L100S, U12-ch58, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch58, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch58, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch58, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch58, adc7

calib_packv5_042523_0143.root, FC#6, port A1

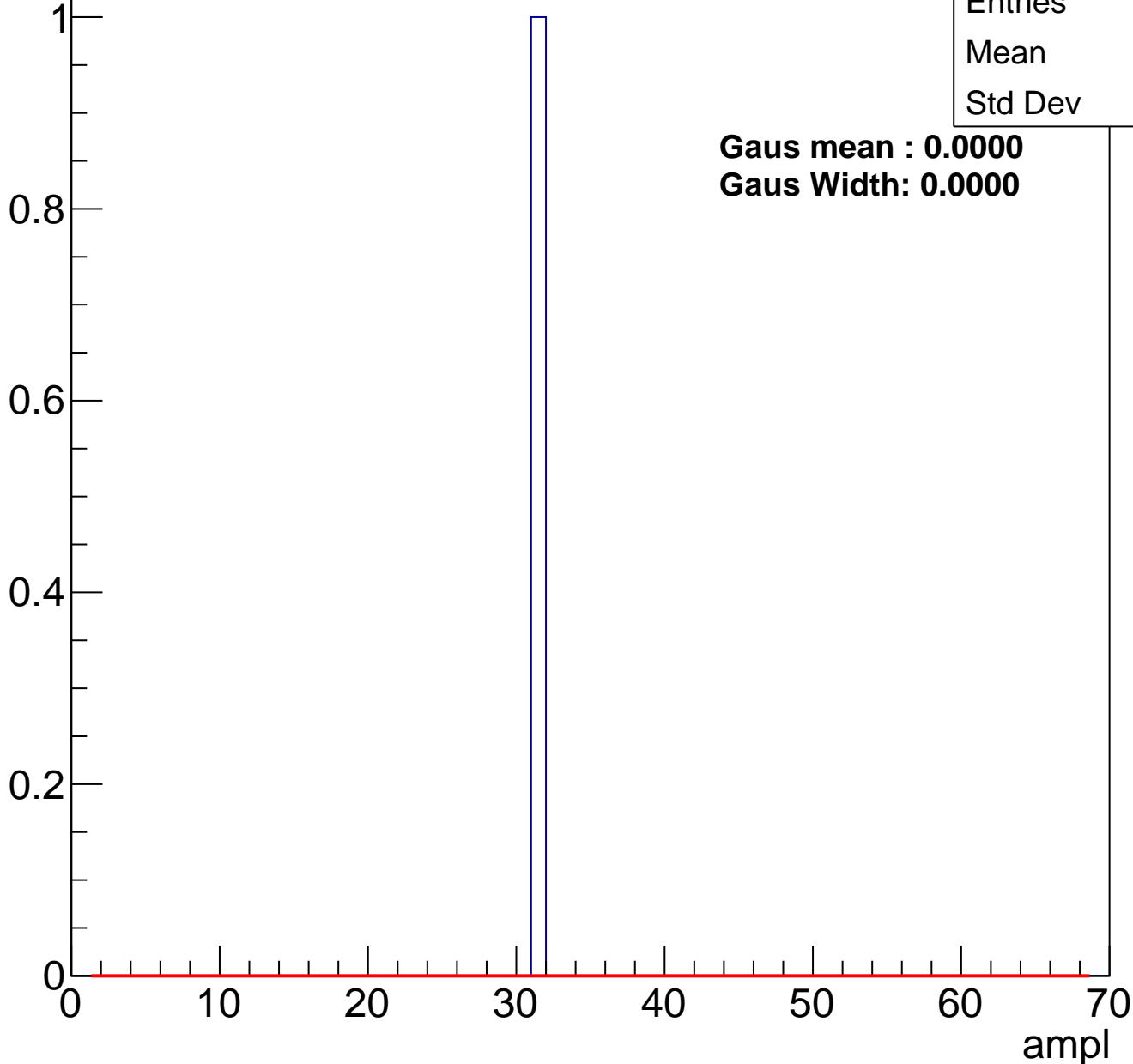
Entry



B0L100S, U12-ch59, adc0

calib_packv5_042523_0143.root, FC#6, port A1

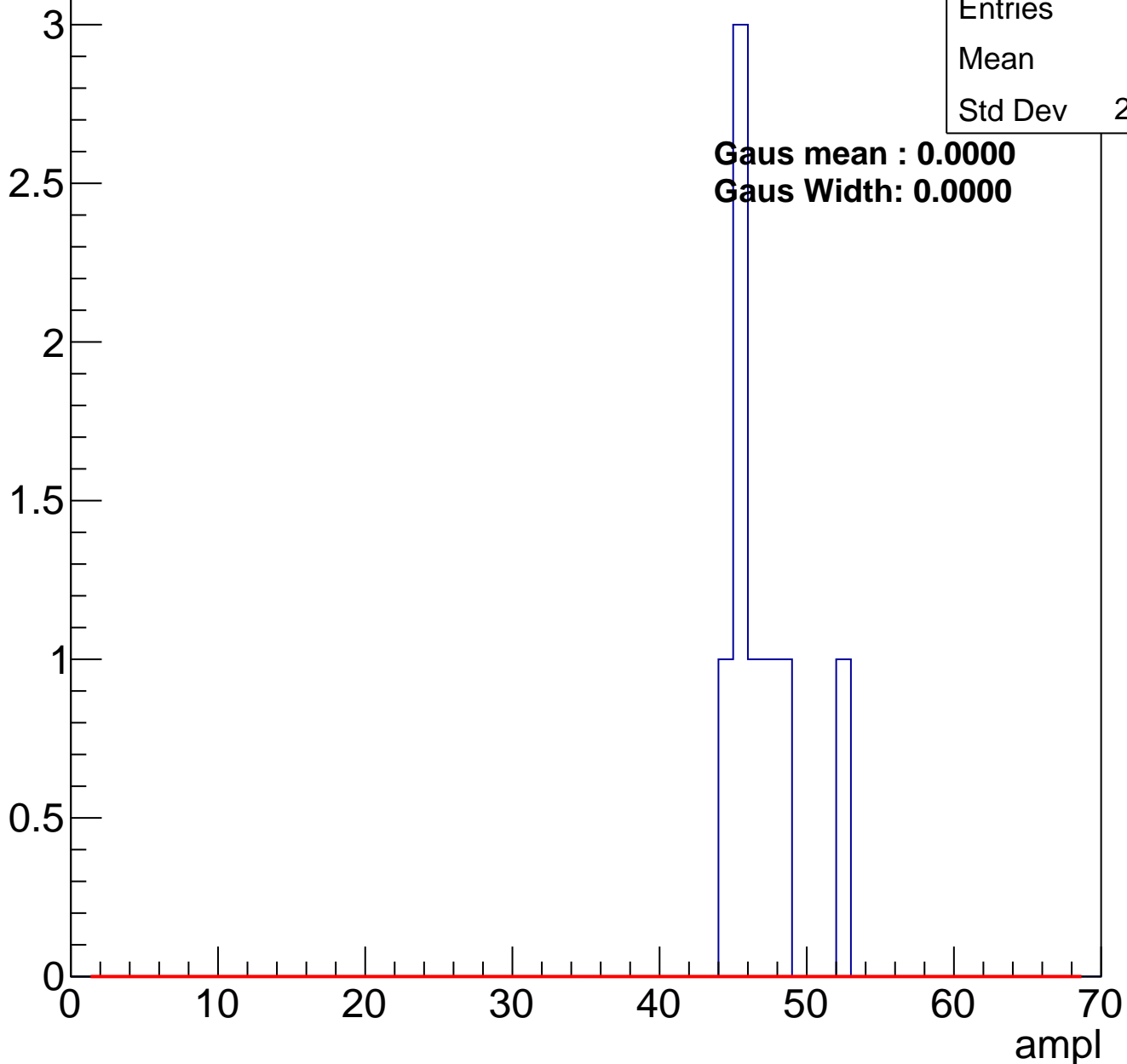
Entry



B0L100S, U12-ch59, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry

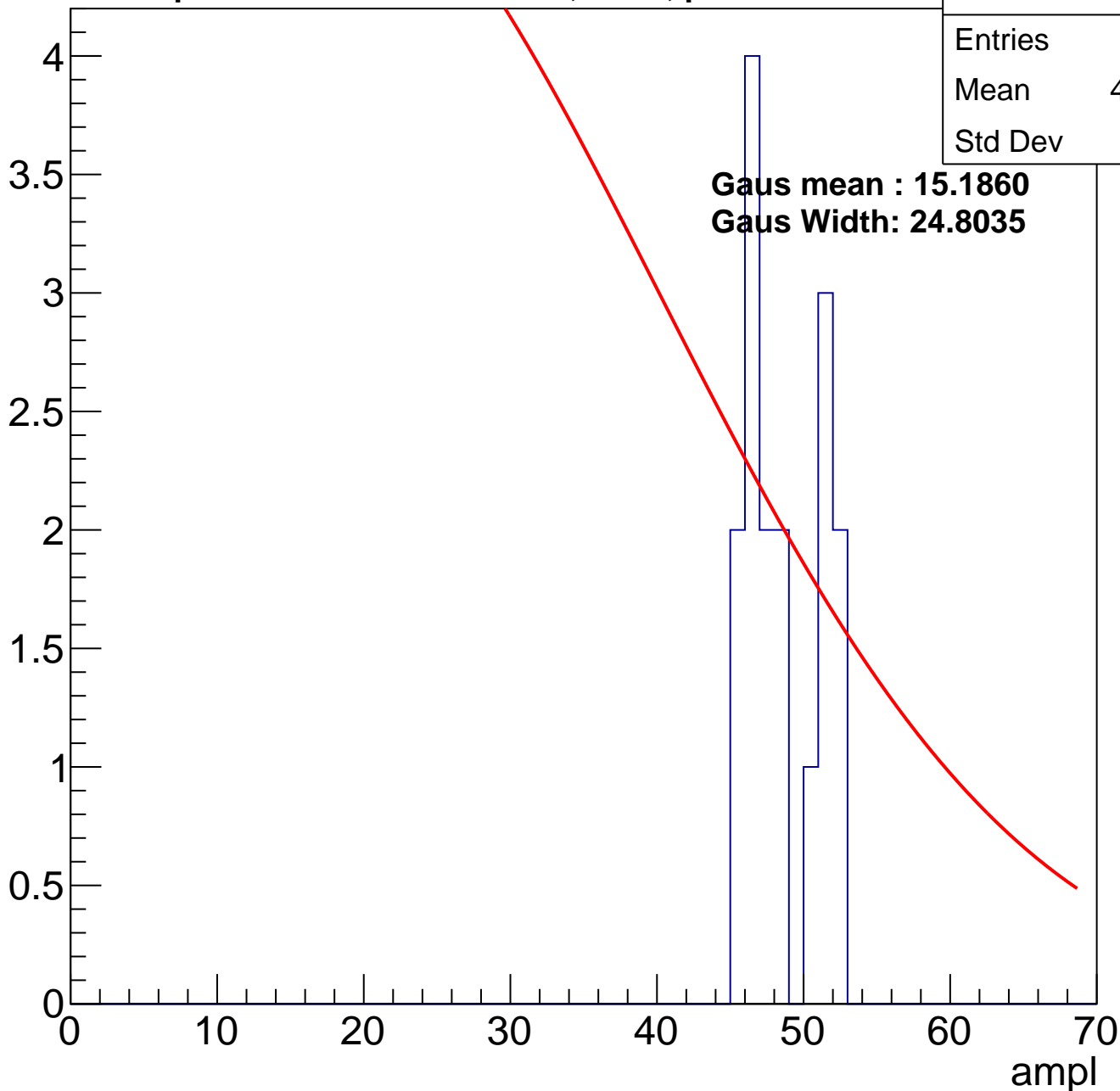


Entries	8
Mean	46.5
Std Dev	2.398

B0L100S, U12-ch59, adc2

calib_packv5_042523_0143.root, FC#6, port A1

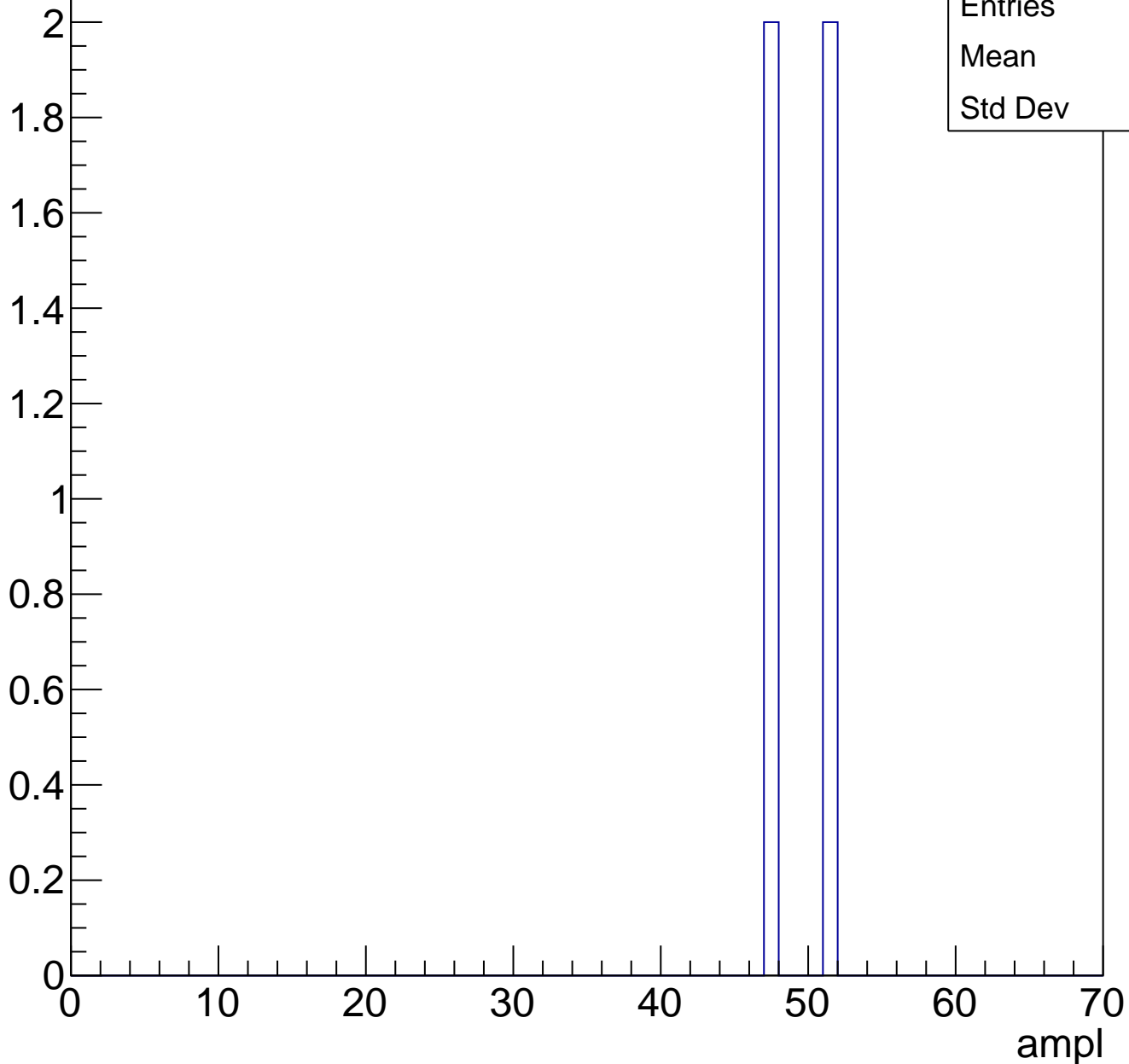
Entry



B0L100S, U12-ch59, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch59, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch59, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch59, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch59, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch60, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch60, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch60, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch60, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch60, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch60, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch60, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch60, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch61, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	1
Mean	0
Std Dev	0

B0L100S, U12-ch61, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Gaus mean : 0.0000

Gaus Width: 0.0000

Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch61, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch61, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch61, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch61, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch61, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch61, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch62, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry

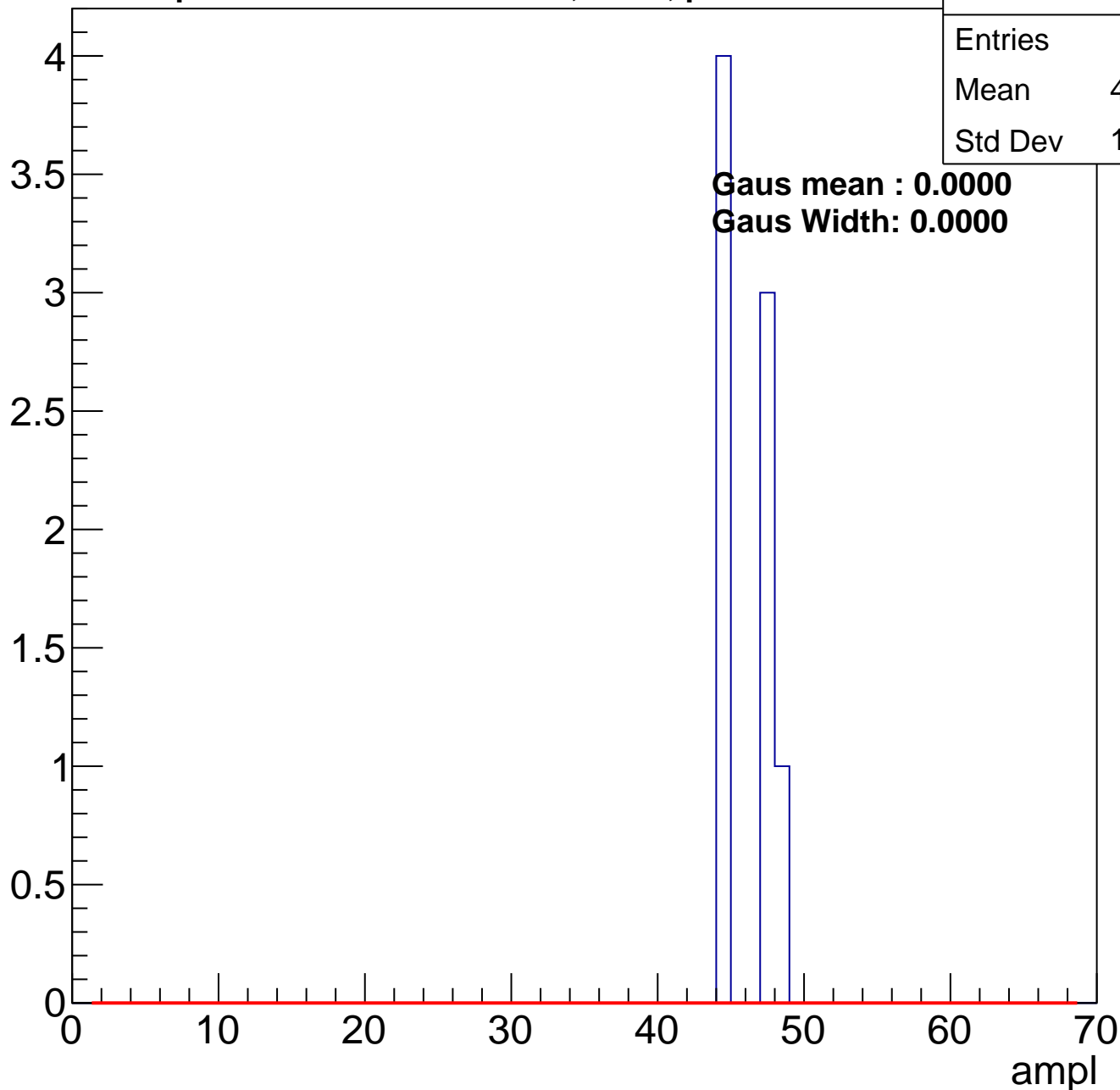


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch62, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	8
Mean	45.62
Std Dev	1.654

B0L100S, U12-ch62, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

Entries	15
Mean	49.07
Std Dev	1.062

Gaus mean : 49.5509

Gaus Width: 1.1736

4

3

2

1

0

ampl

0

10

20

30

40

50

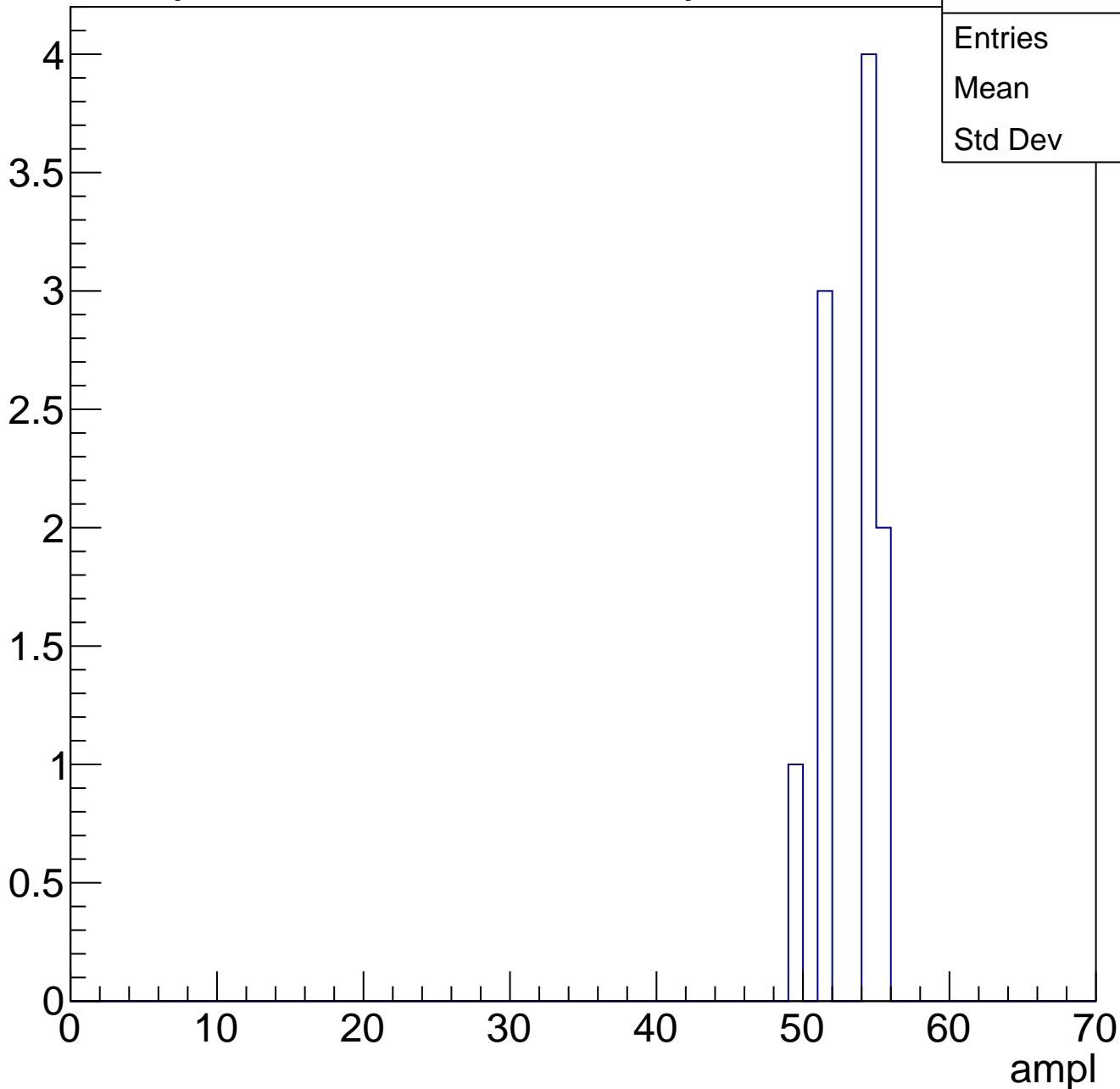
60

70

B0L100S, U12-ch62, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch62, adc4

calib_packv5_042523_0143.root, FC#6, port A1

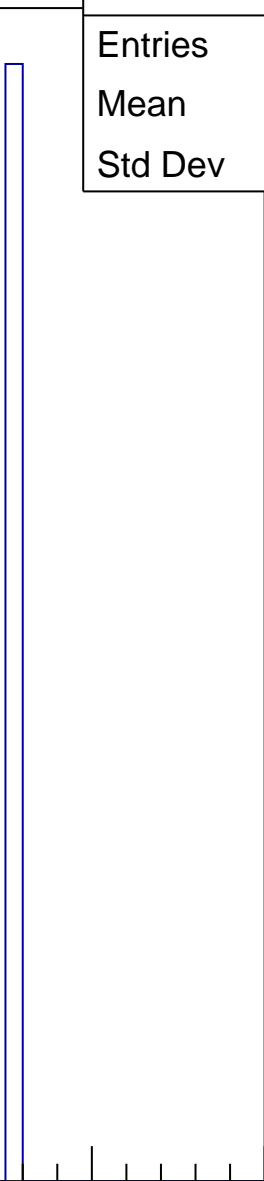
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	2
Mean	55
Std Dev	0

0 10 20 30 40 50 60 70

ampl



B0L100S, U12-ch62, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch62, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch62, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry

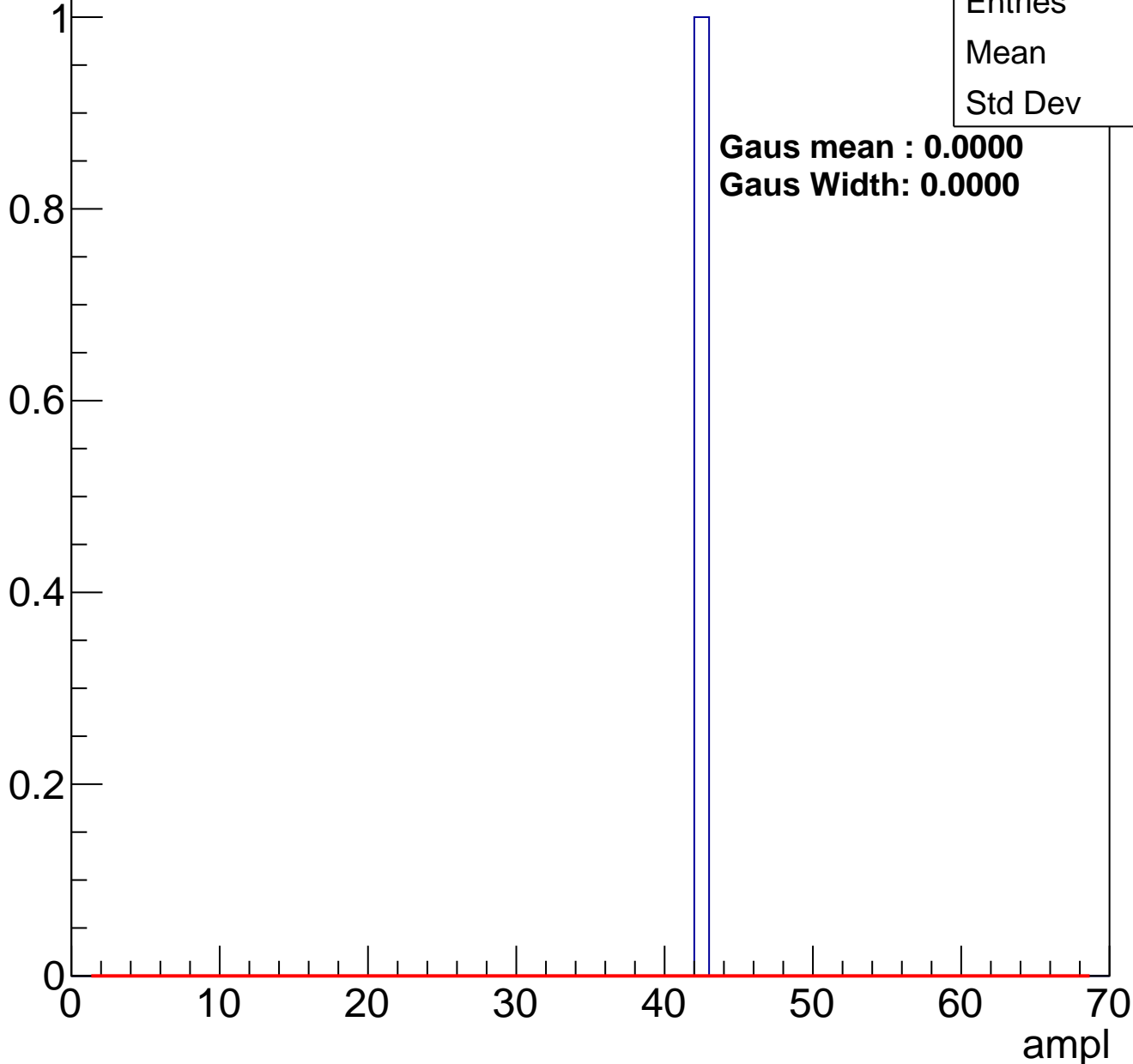


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch63, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry

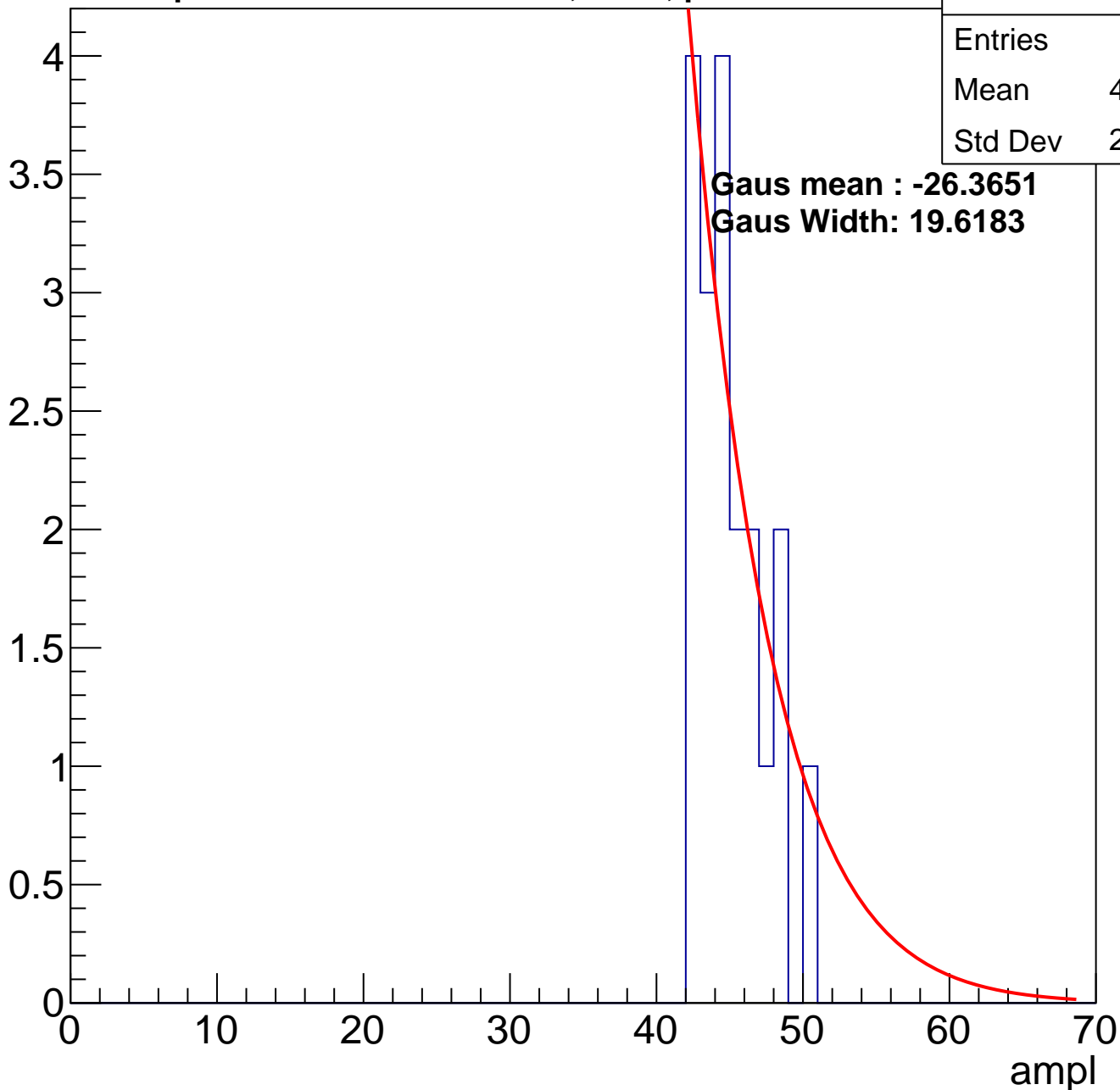


Entries	1
Mean	42
Std Dev	0

B0L100S, U12-ch63, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch63, adc2

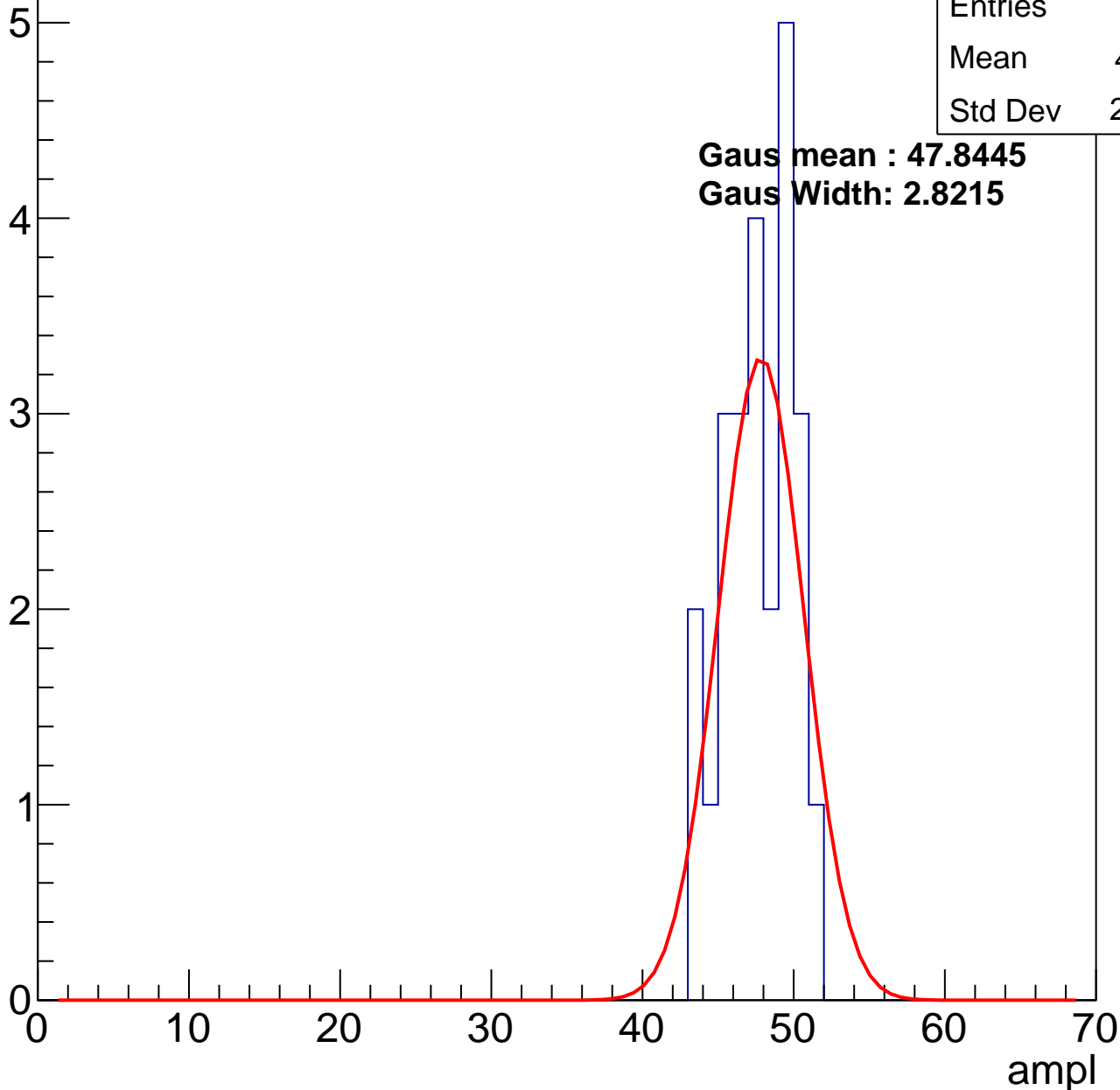
calib_packv5_042523_0143.root, FC#6, port A1

Entry

Entries	24
Mean	47.21
Std Dev	2.236

Gaus mean : 47.8445

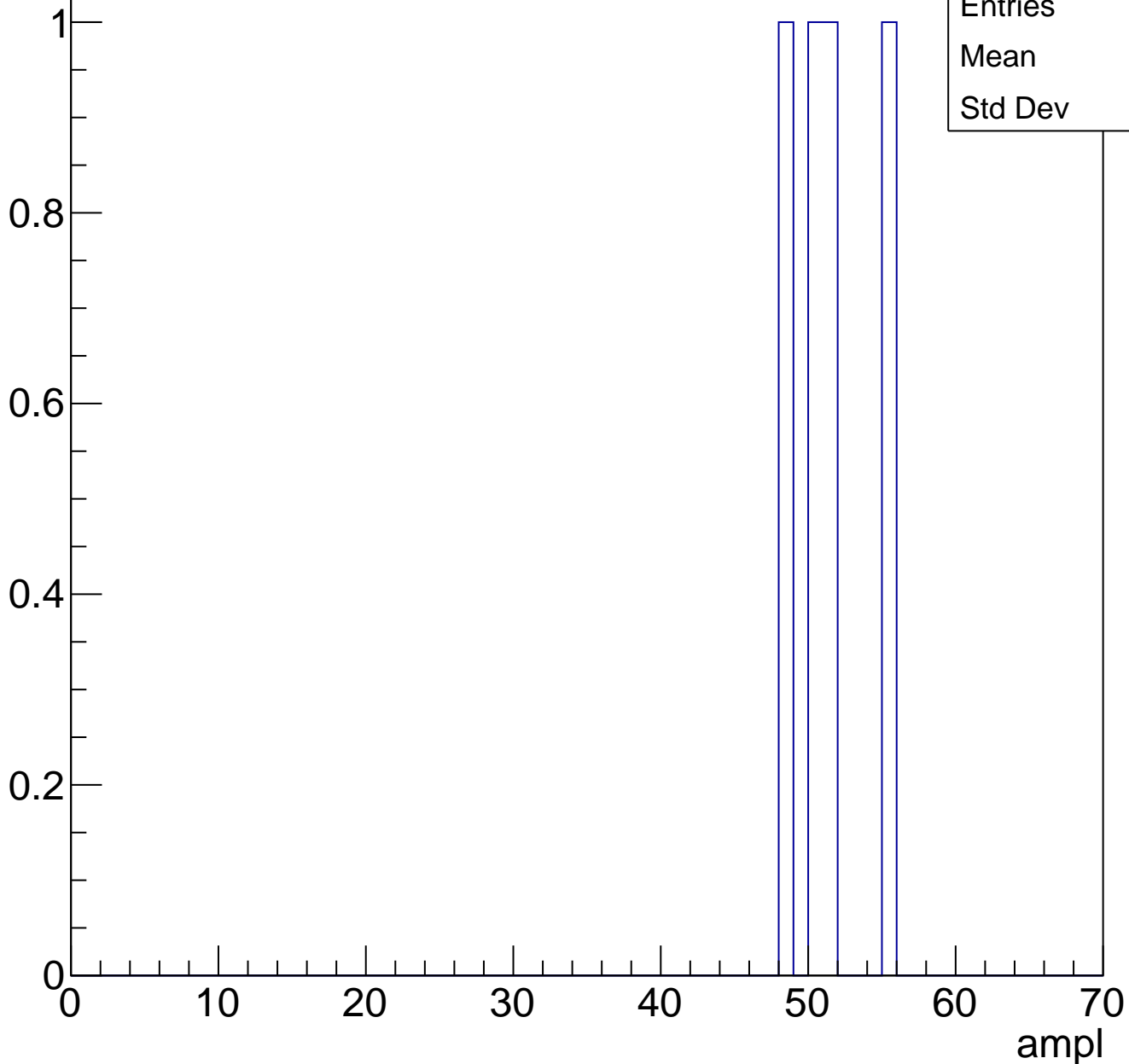
Gaus Width: 2.8215



B0L100S, U12-ch63, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch63, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch63, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch63, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch63, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch64, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry

1
0.8
0.6
0.4
0.2
0

Entries	1
Mean	44
Std Dev	0

Gaus mean : 0.0000

Gaus Width: 0.0000

ampl

0 10 20 30 40 50 60 70

B0L100S, U12-ch64, adc1

calib_packv5_042523_0143.root, FC#6, port A1

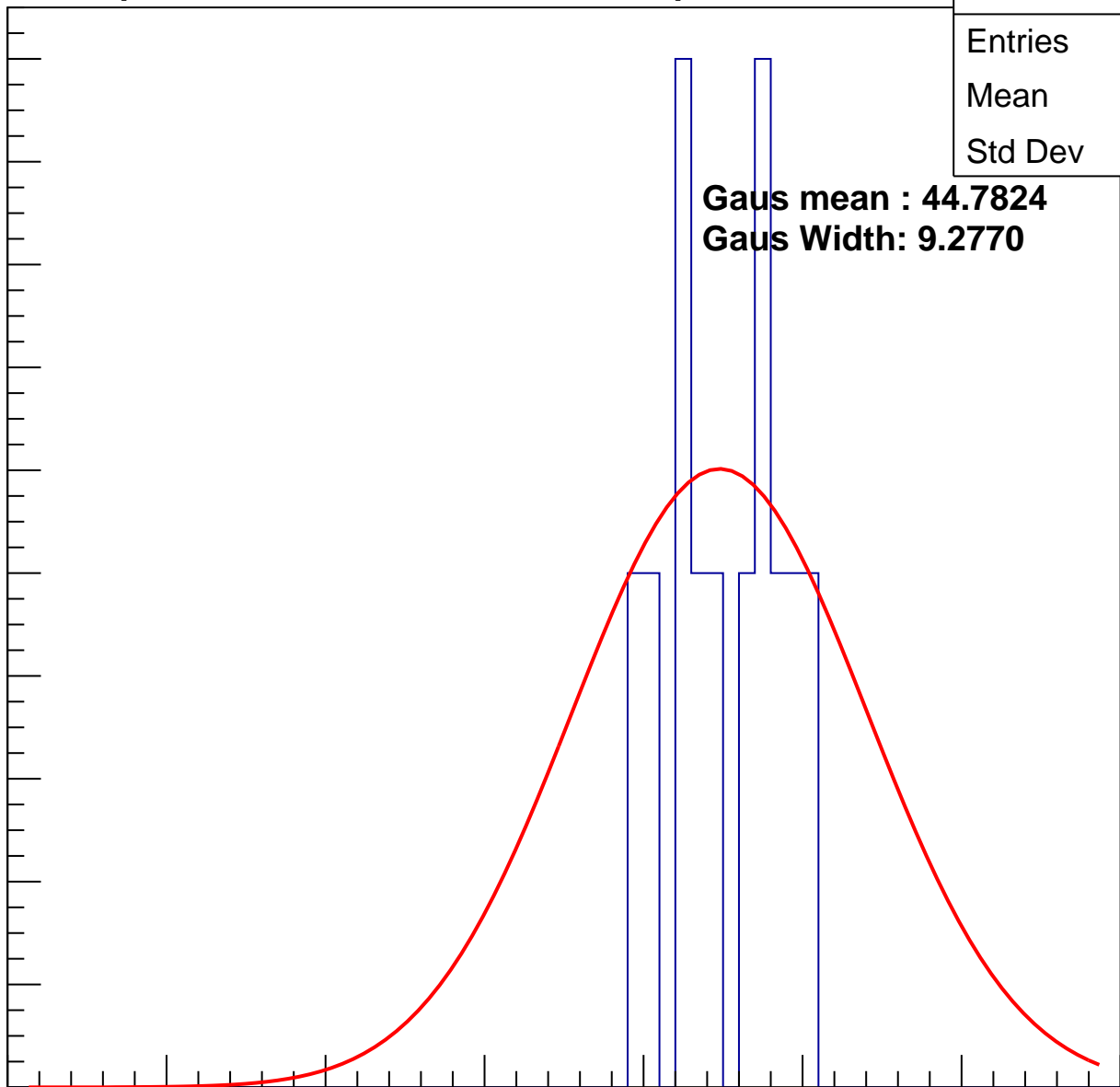
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	12
Mean	44.75
Std Dev	3.443

Gaus mean : 44.7824
Gaus Width: 9.2770

0 10 20 30 40 50 60 70
ampl



B0L100S, U12-ch64, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

4
3.5
3
2.5
2
1.5
1
0.5
0

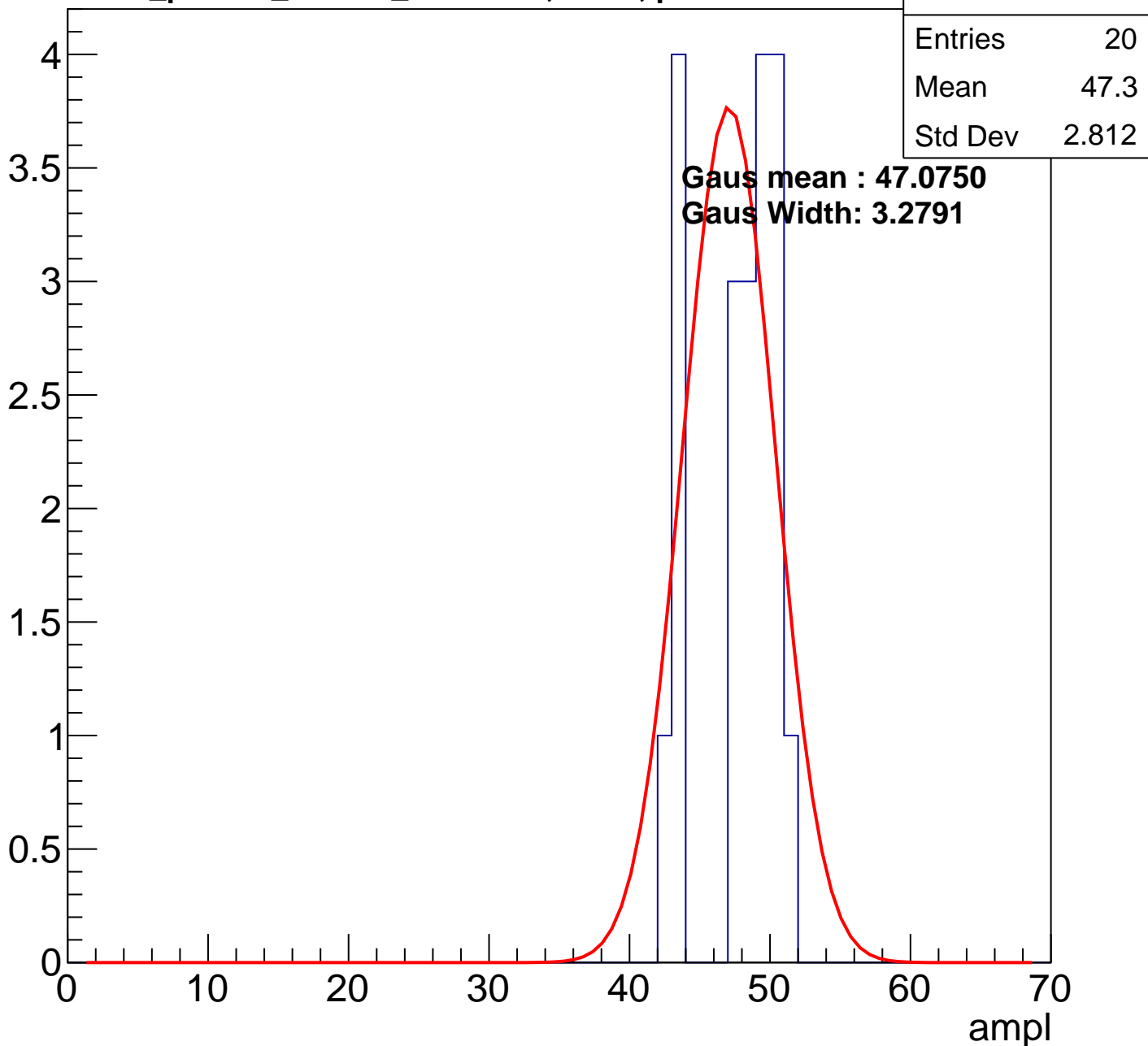
Entries	20
Mean	47.3
Std Dev	2.812

Gaus mean : 47.0750

Gaus Width: 3.2791

0 10 20 30 40 50 60 70

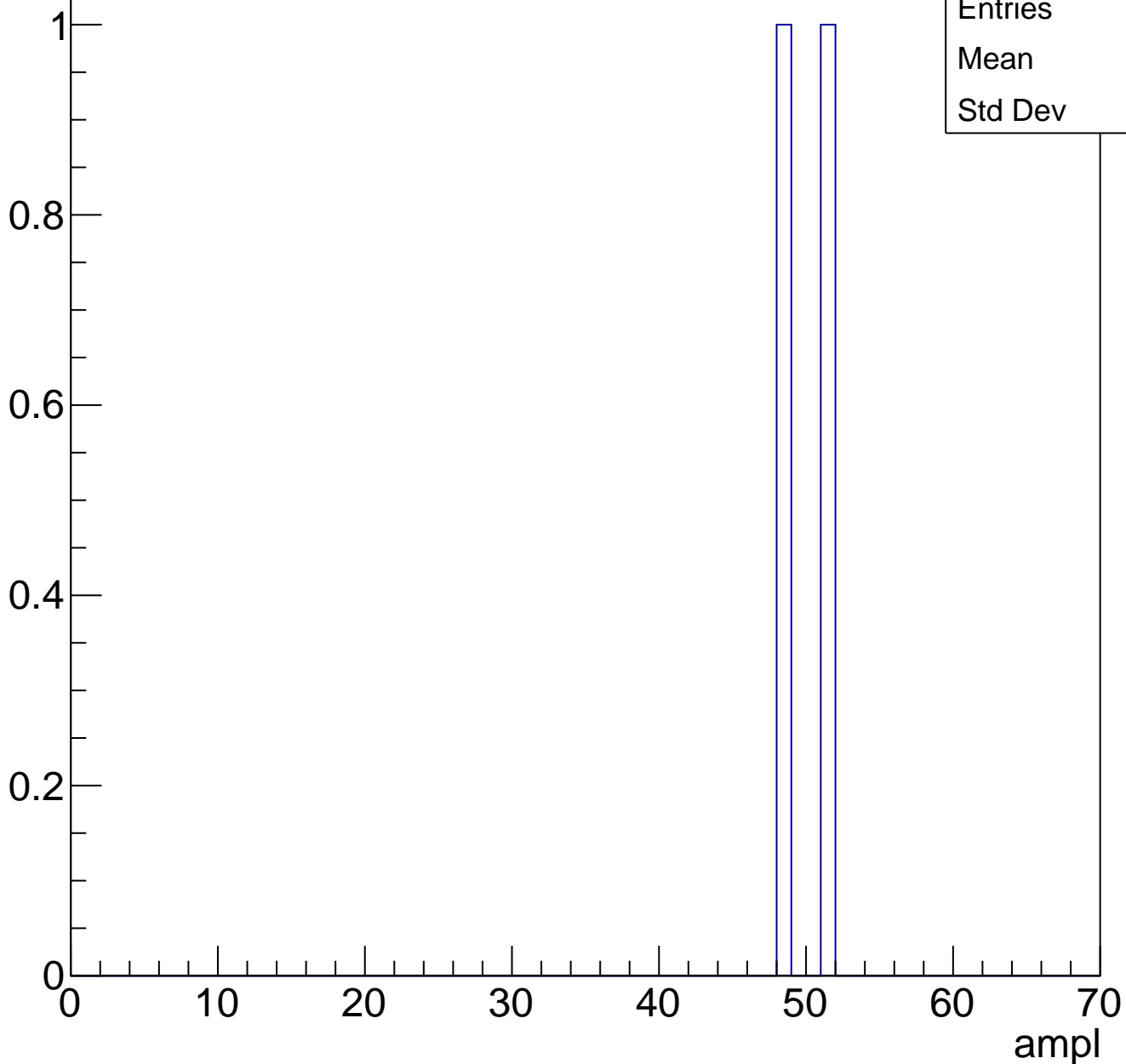
ampl



B0L100S, U12-ch64, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch64, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch64, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch64, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch64, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch65, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	1
Mean	0
Std Dev	0

Gaus mean : 0.0000

Gaus Width: 0.0000

B0L100S, U12-ch65, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch65, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch65, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch65, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch65, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch65, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch65, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch66, adc0

calib_packv5_042523_0143.root, FC#6, port A1

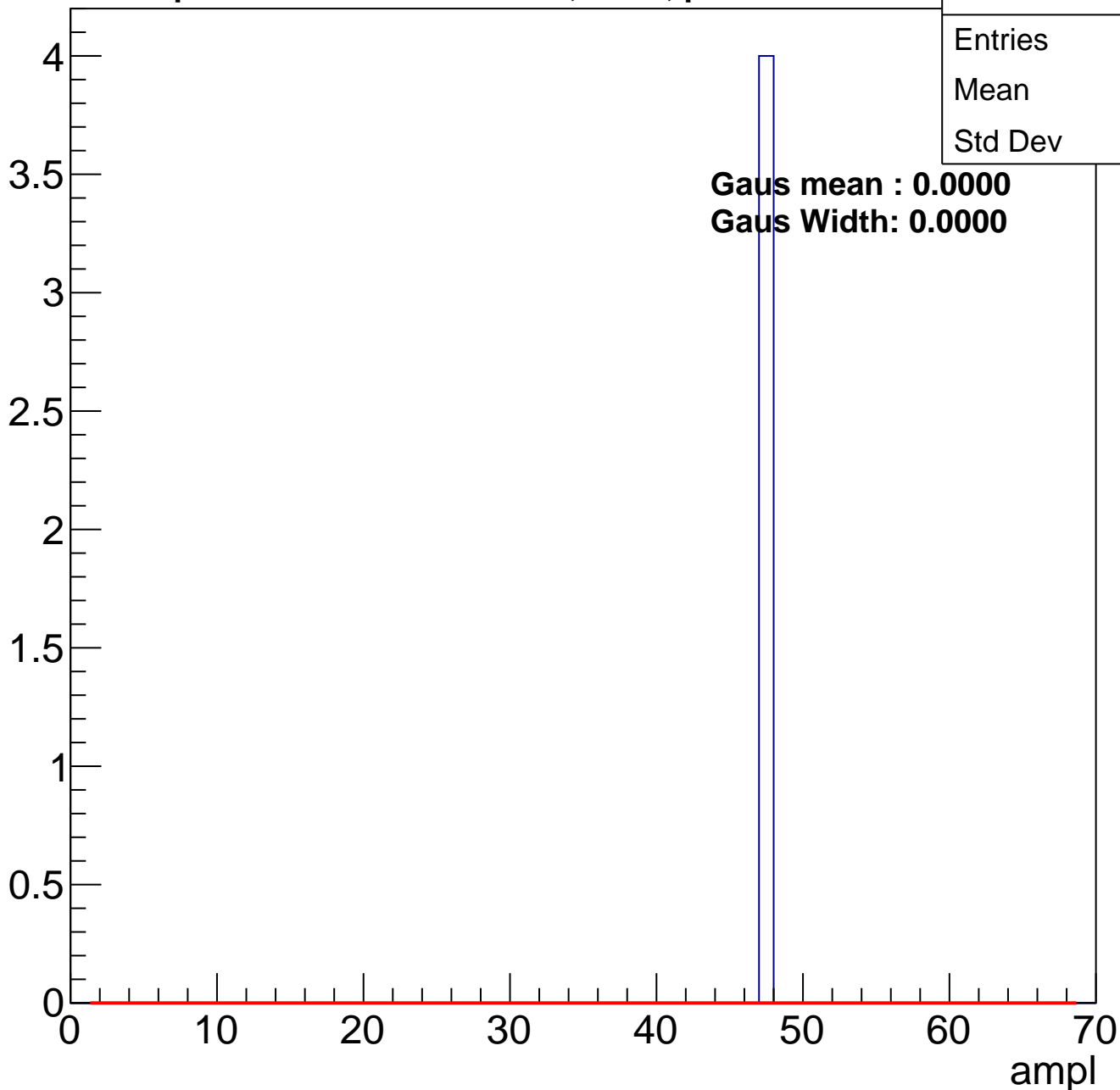
Entry



B0L100S, U12-ch66, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry

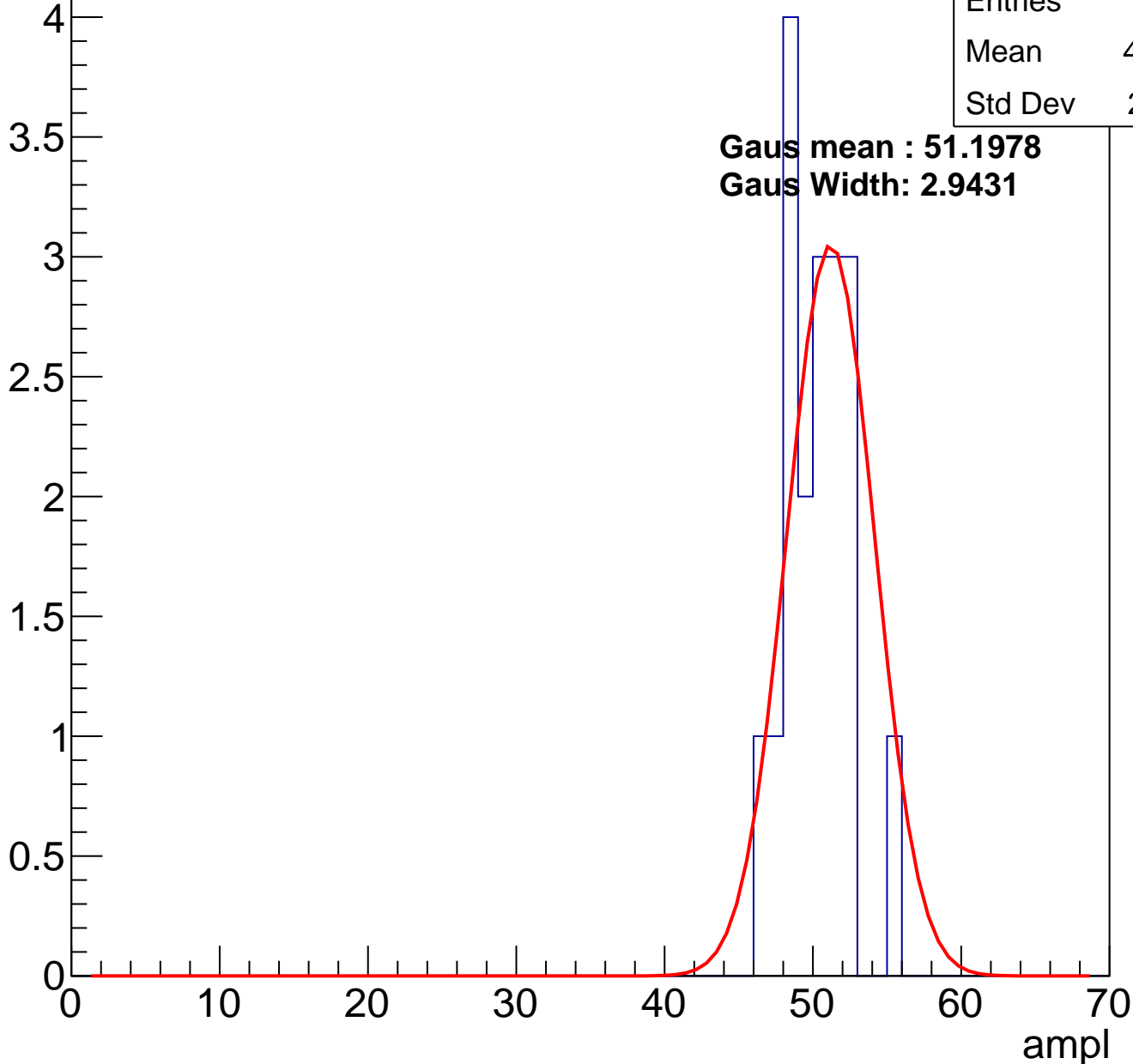


Entries	4
Mean	47
Std Dev	0

B0L100S, U12-ch66, adc2

calib_packv5_042523_0143.root, FC#6, port A1

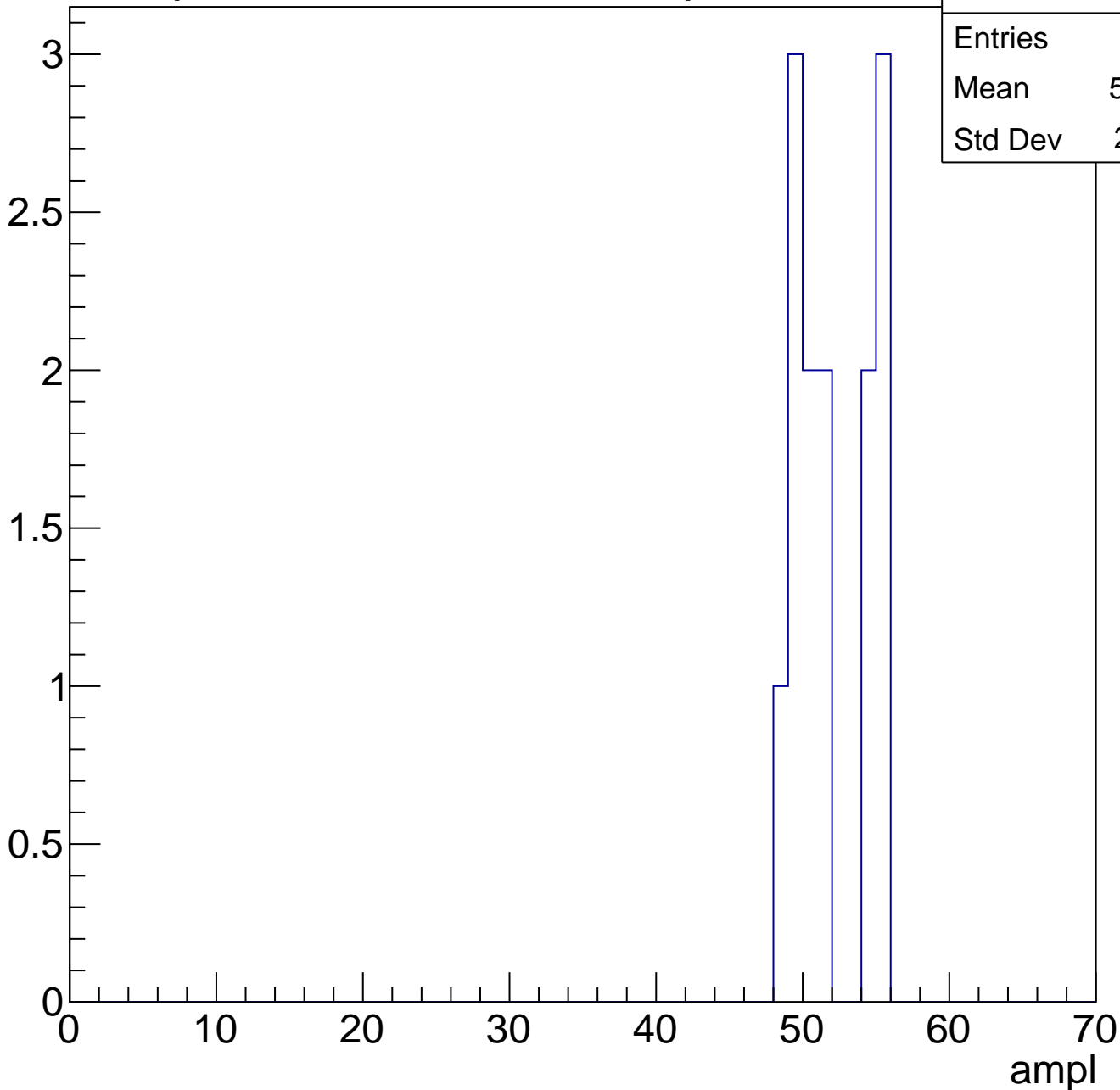
Entry



B0L100S, U12-ch66, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch66, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

1

Mean

55

Std Dev

0

B0L100S, U12-ch66, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch66, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch66, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch67, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch67, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch67, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch67, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch67, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch67, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch67, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch67, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry

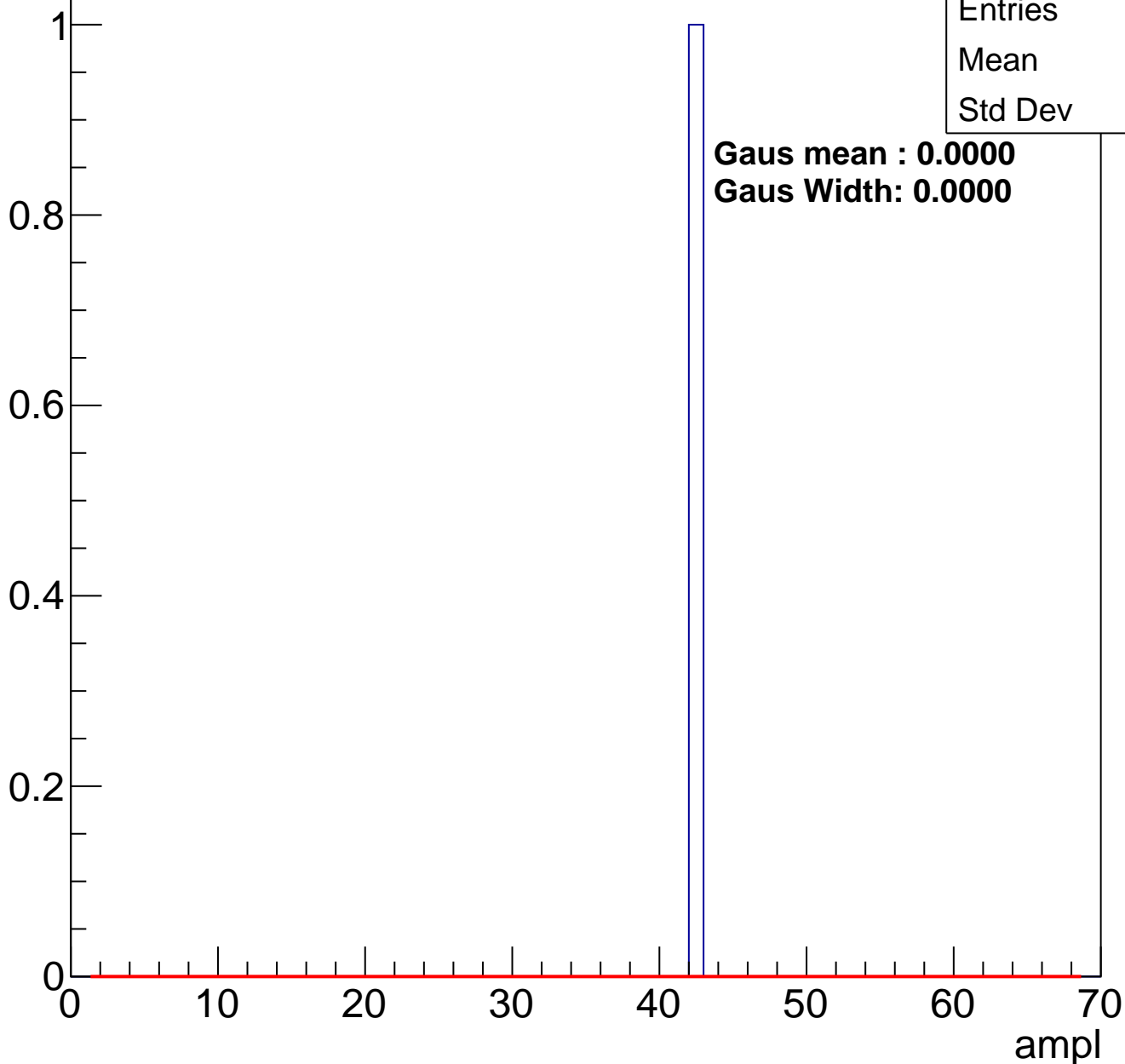


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch68, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch68, adc1

calib_packv5_042523_0143.root, FC#6, port A1

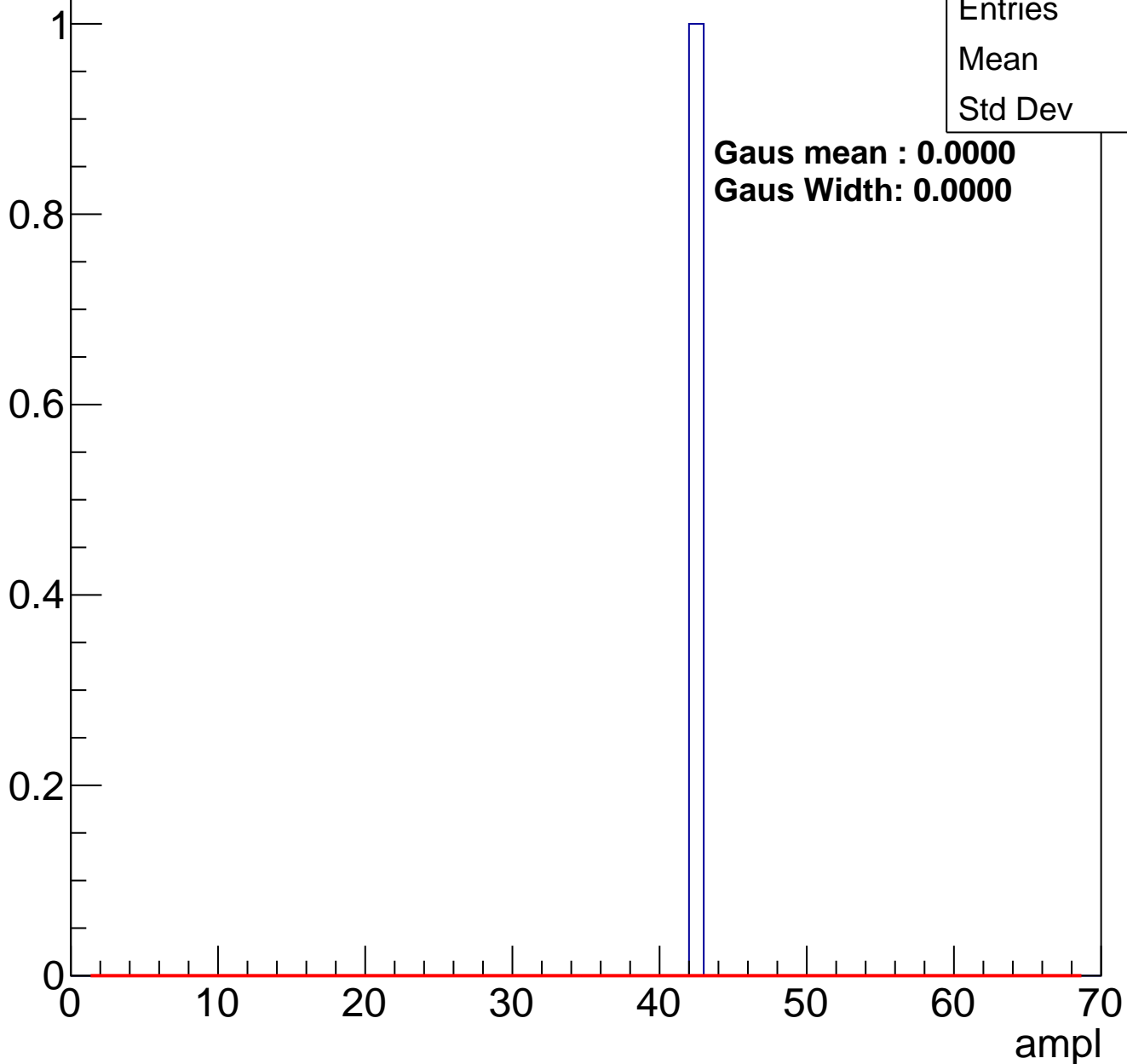
Entry



B0L100S, U12-ch68, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	1
Mean	42
Std Dev	0

B0L100S, U12-ch68, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch68, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch68, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch68, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch68, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry

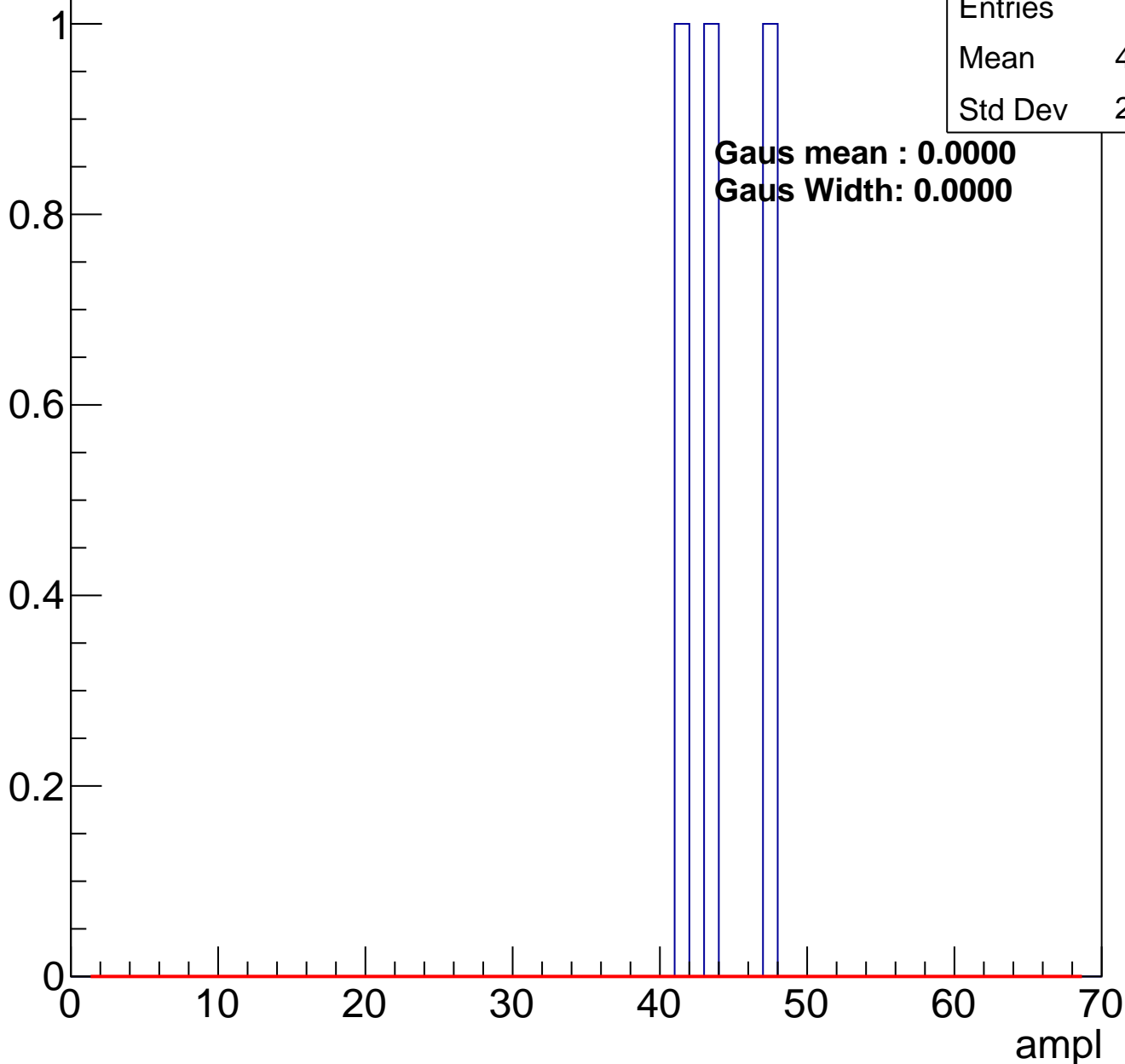


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch69, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry

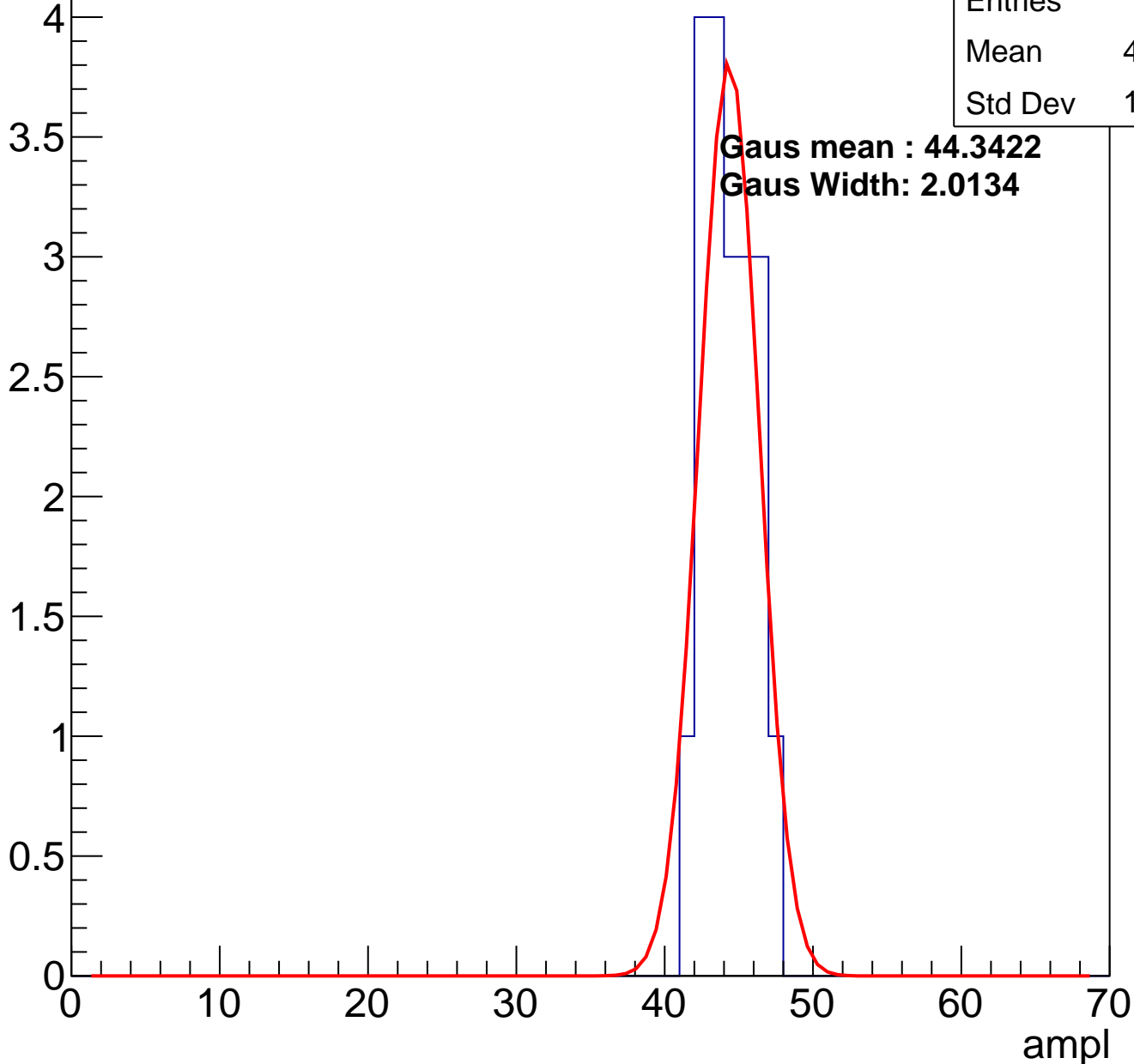


Entries	3
Mean	43.67
Std Dev	2.494

B0L100S, U12-ch69, adc1

calib_packv5_042523_0143.root, FC#6, port A1

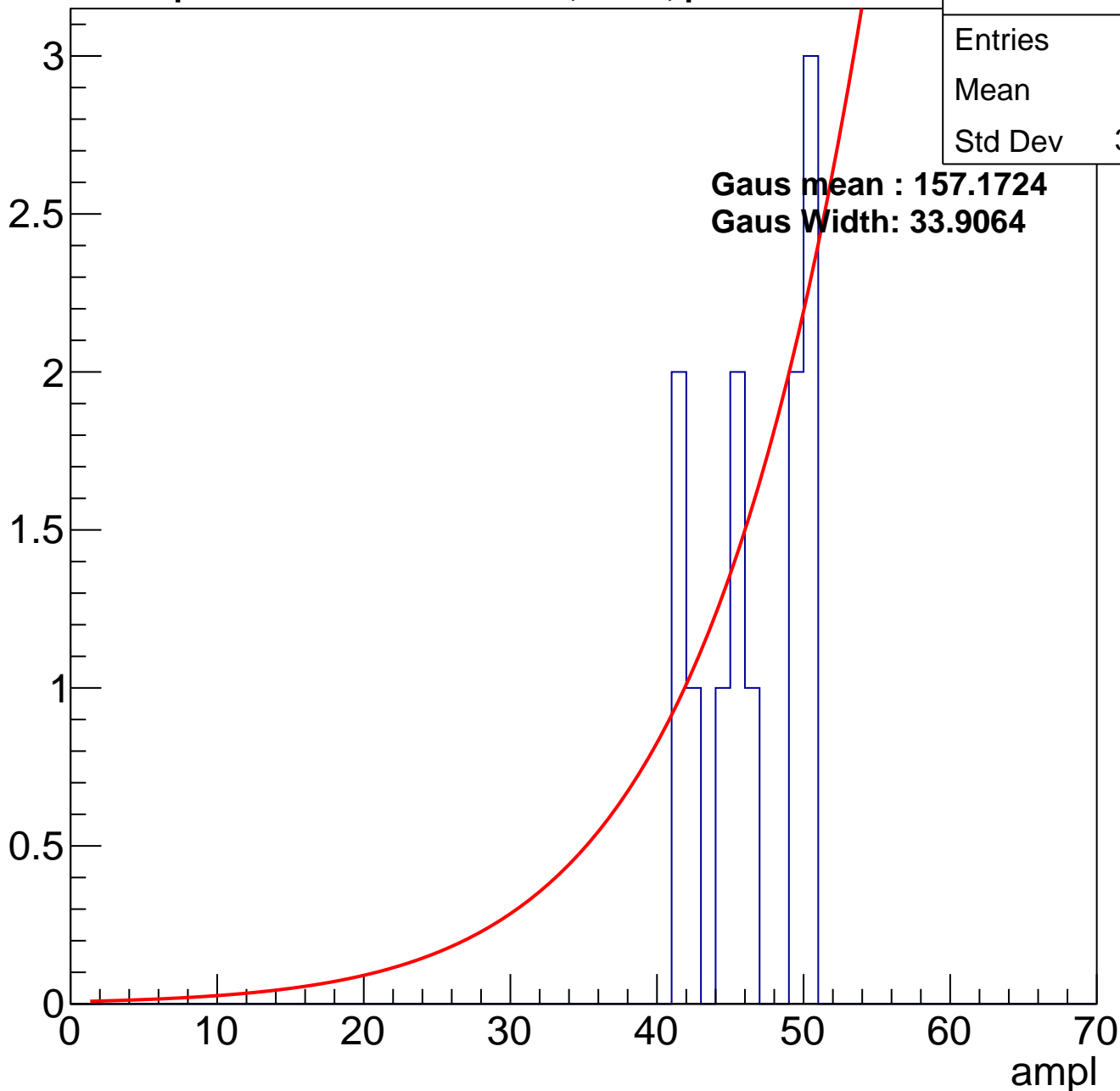
Entry



B0L100S, U12-ch69, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



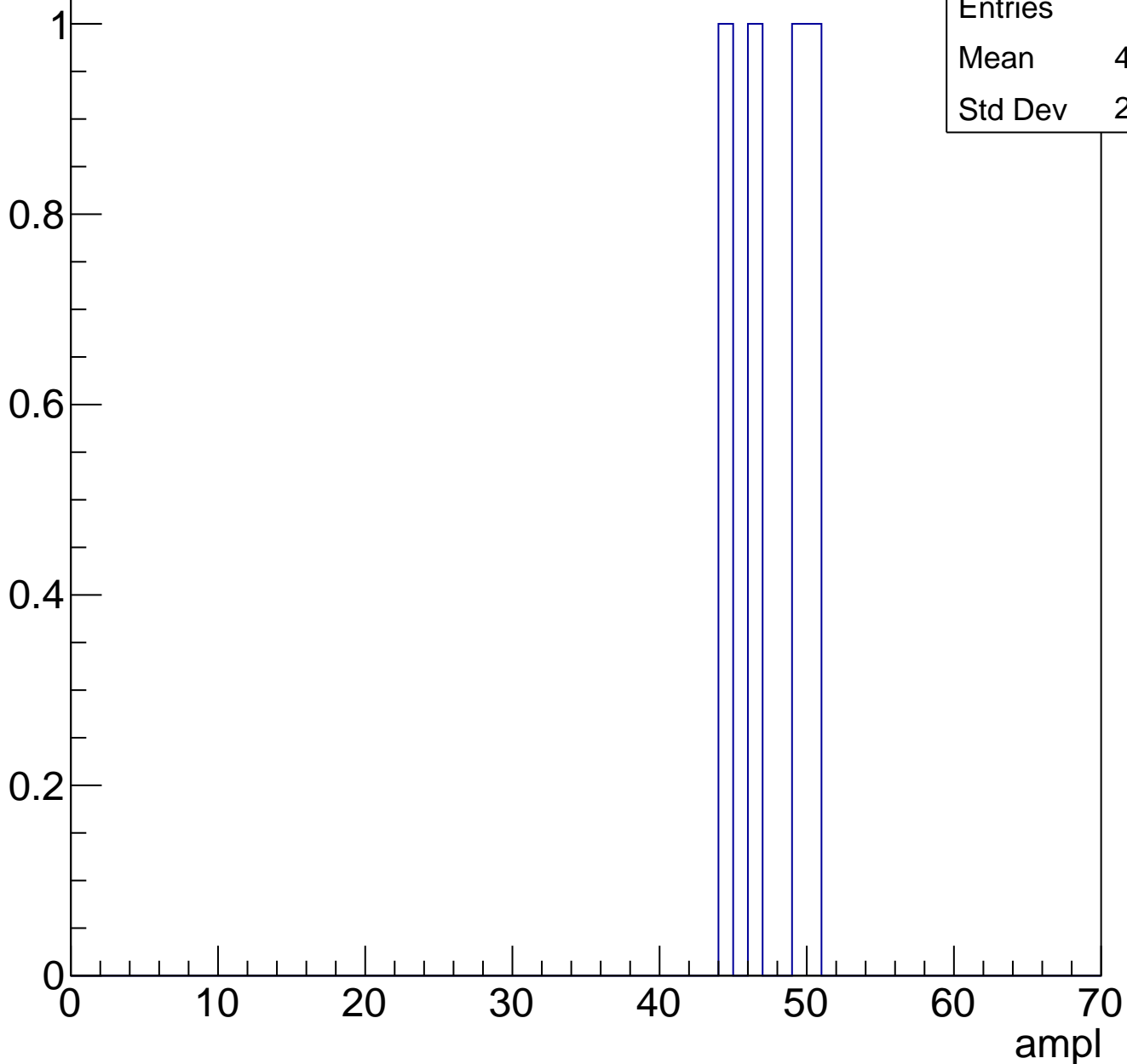
Entries	12
Mean	46
Std Dev	3.391

Gaus mean : 157.1724
Gaus Width: 33.9064

B0L100S, U12-ch69, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch69, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch69, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch69, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch69, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch70, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch70, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch70, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch70, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch70, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch70, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch70, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch70, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch71, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry

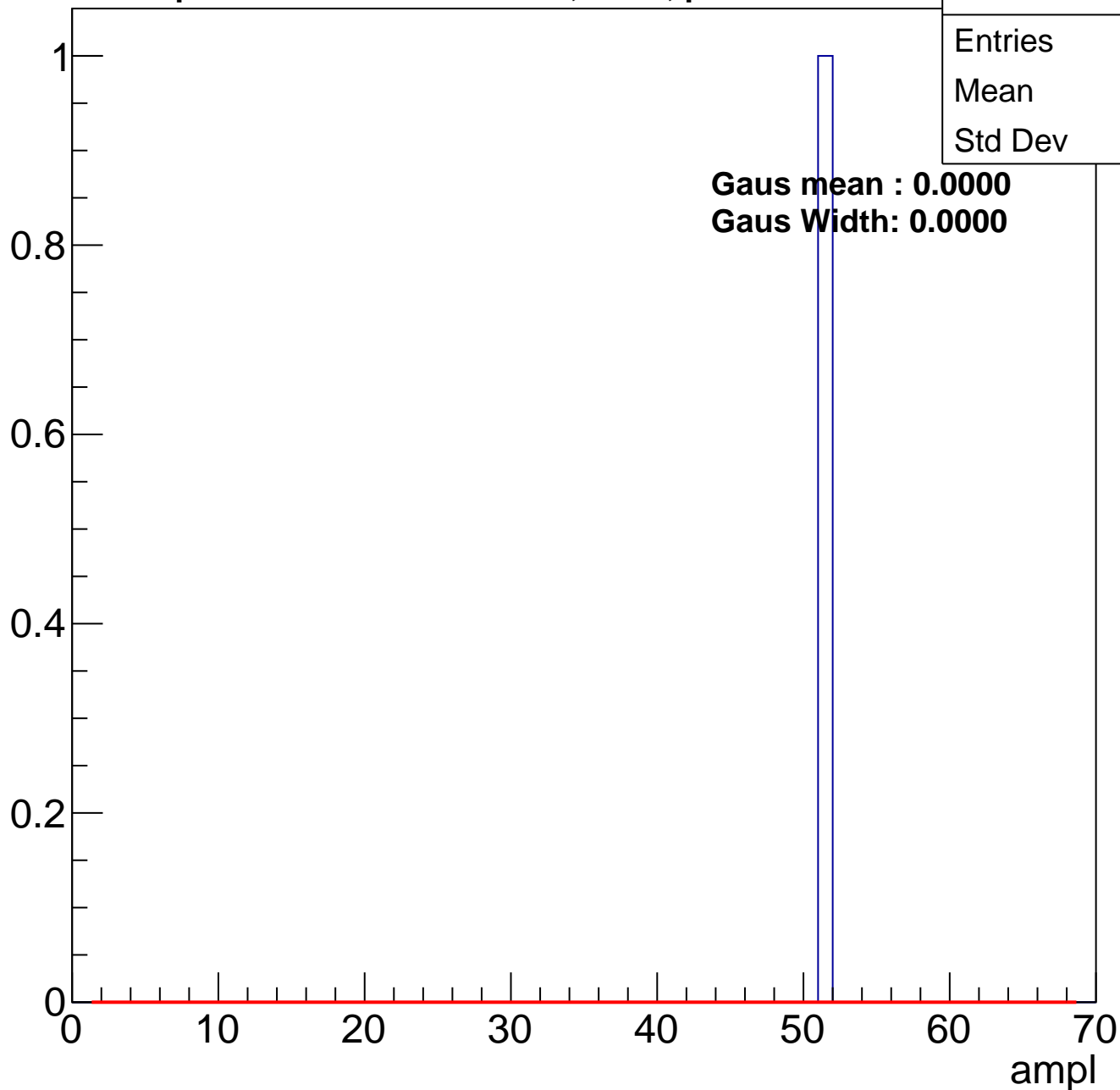


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch71, adc1

calib_packv5_042523_0143.root, FC#6, port A1

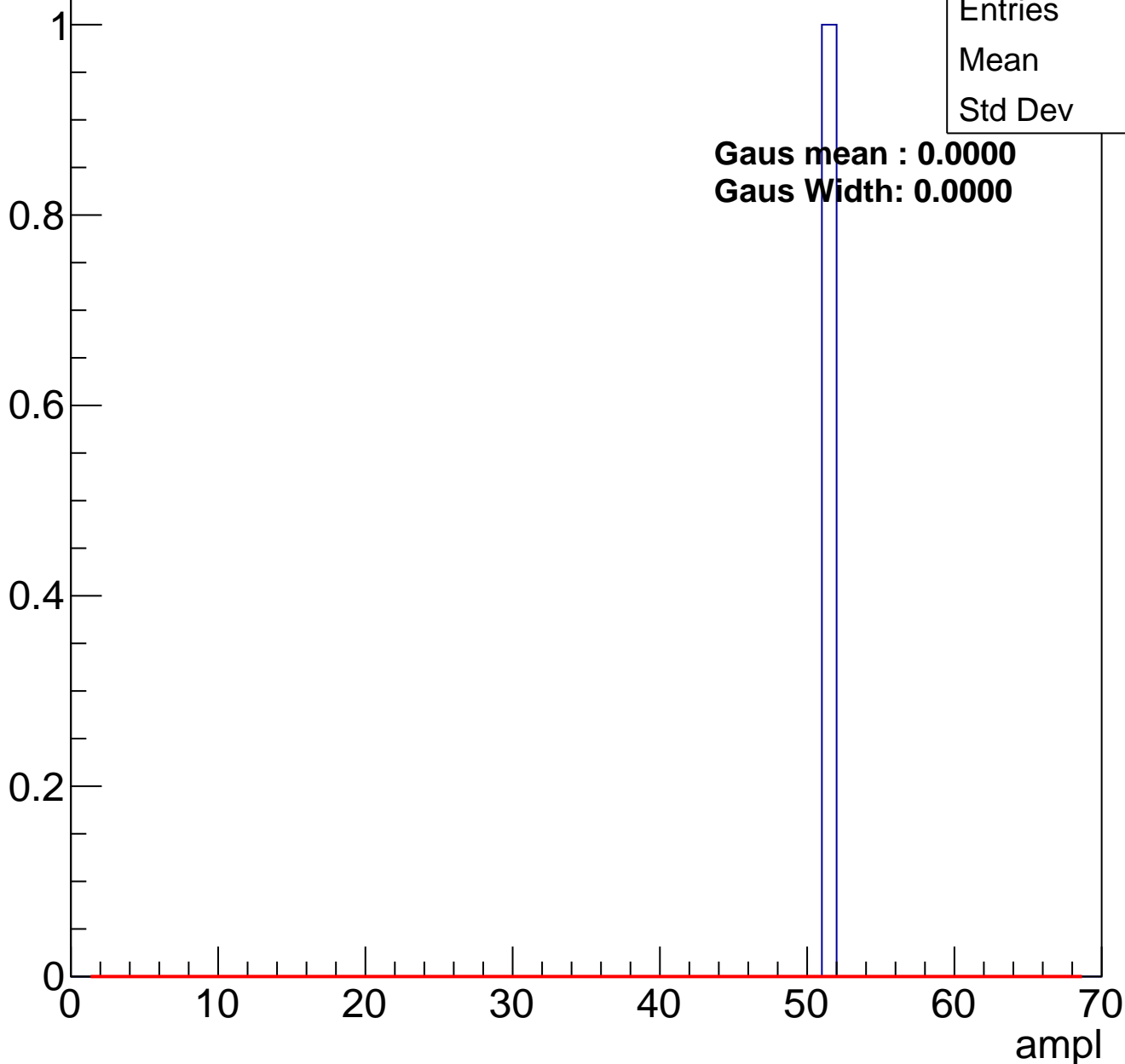
Entry



B0L100S, U12-ch71, adc2

calib_packv5_042523_0143.root, FC#6, port A1

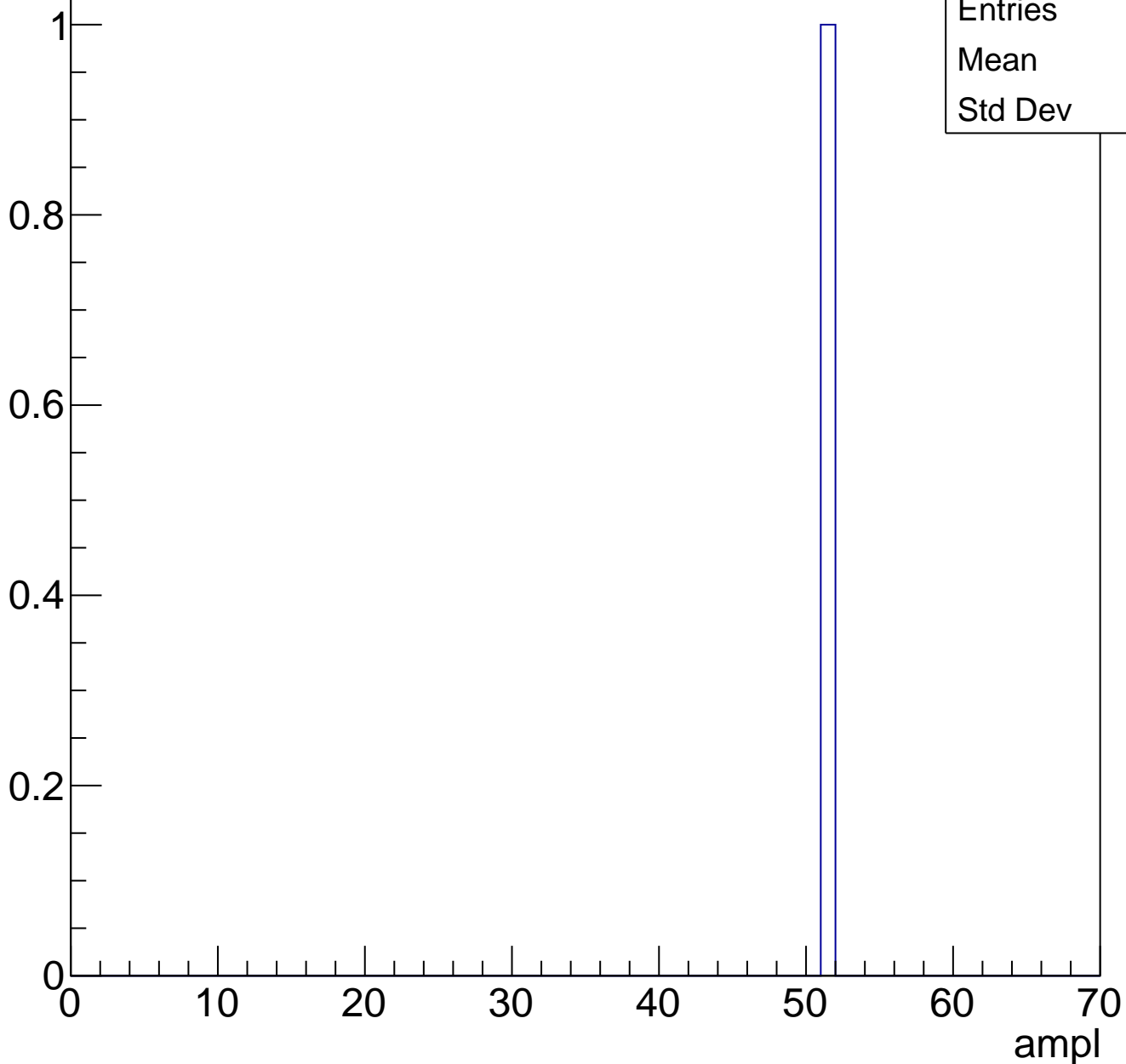
Entry



B0L100S, U12-ch71, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch71, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch71, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch71, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch71, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch72, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry

1
0.8
0.6
0.4
0.2
0

Entries	2
Mean	43.5
Std Dev	1.5

Gaus mean : 0.0000

Gaus Width: 0.0000

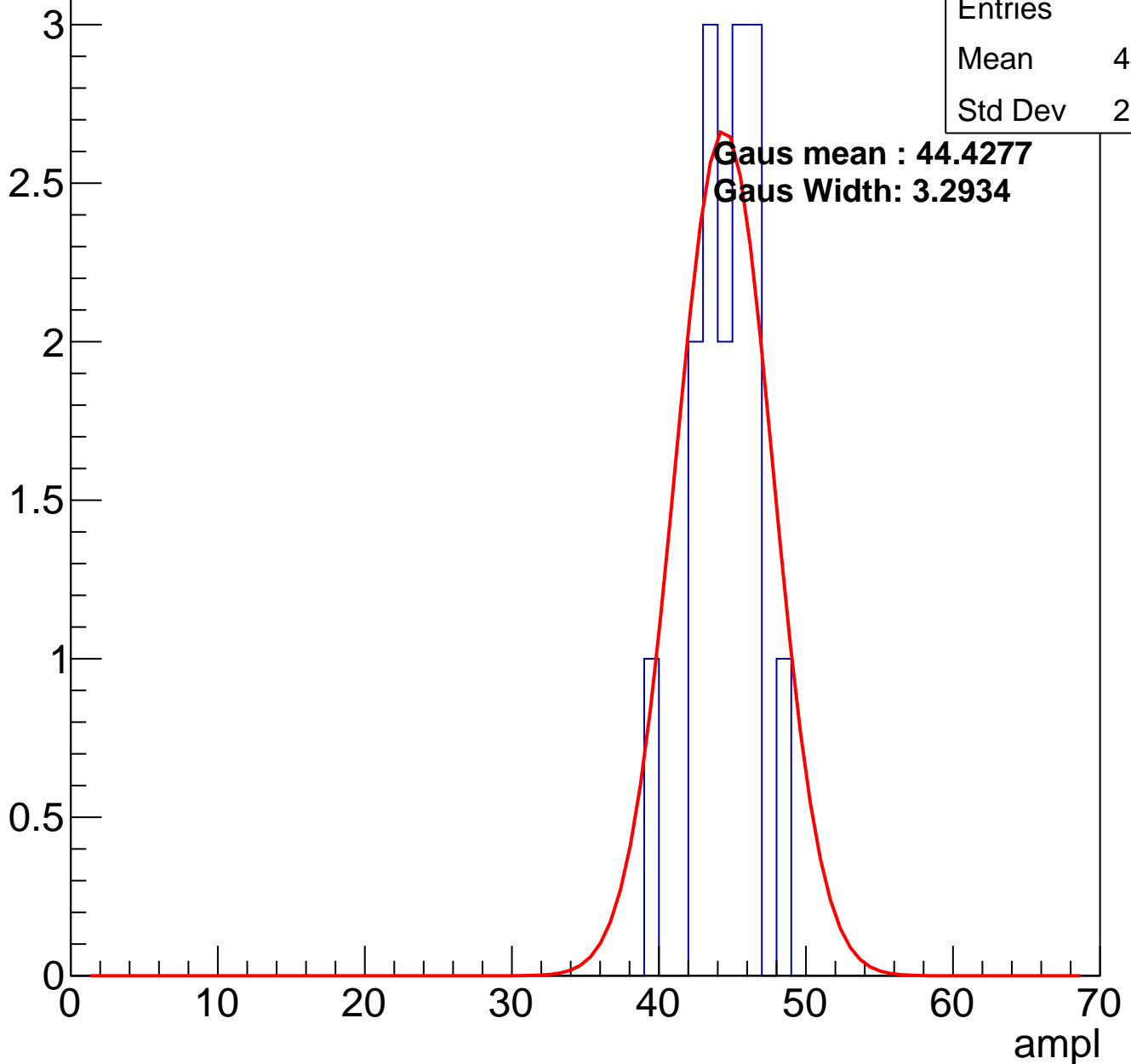
ampl

0 10 20 30 40 50 60 70

B0L100S, U12-ch72, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch72, adc2

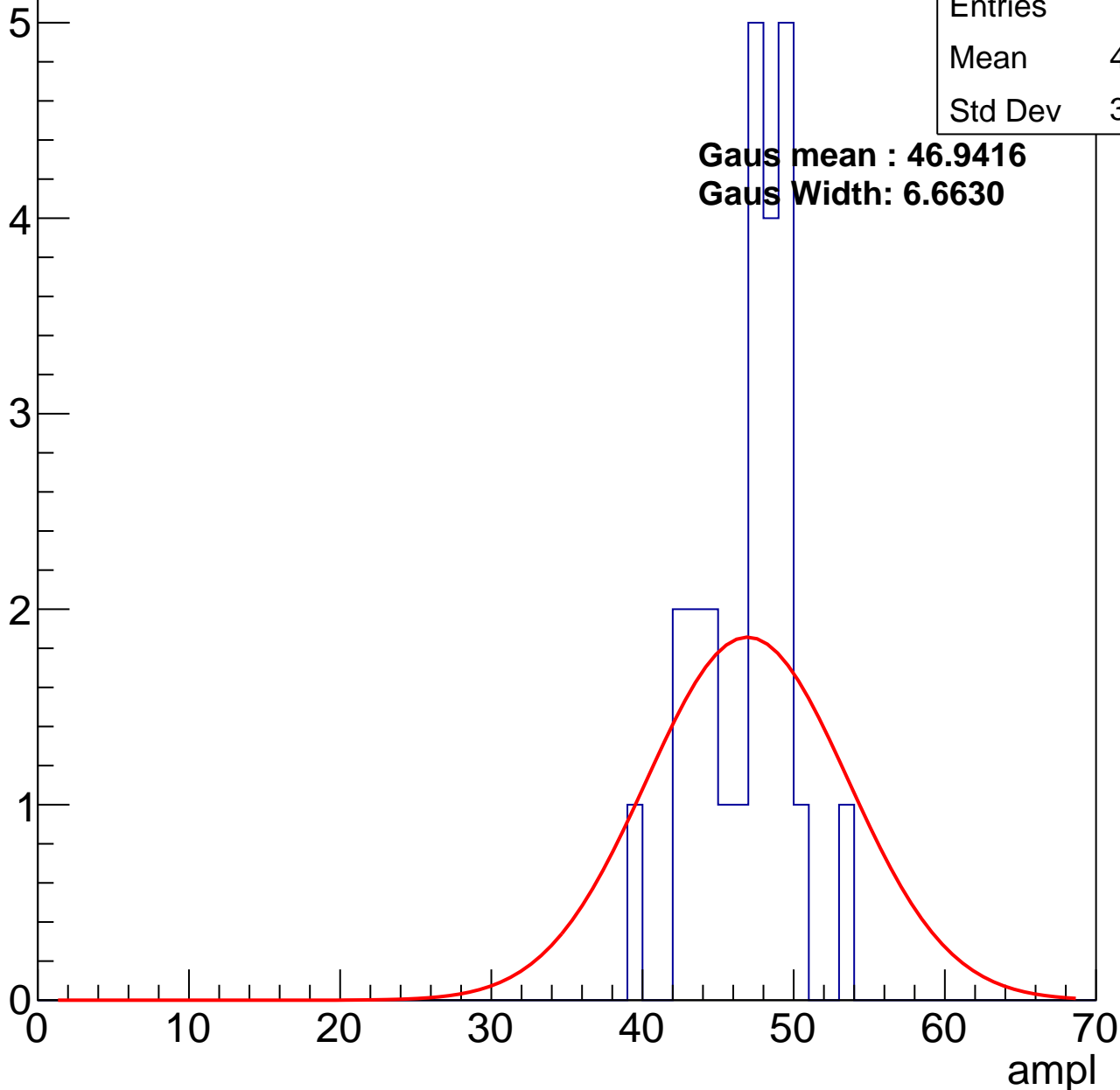
calib_packv5_042523_0143.root, FC#6, port A1

Entry

Entries	25
Mean	46.52
Std Dev	3.048

Gaus mean : 46.9416

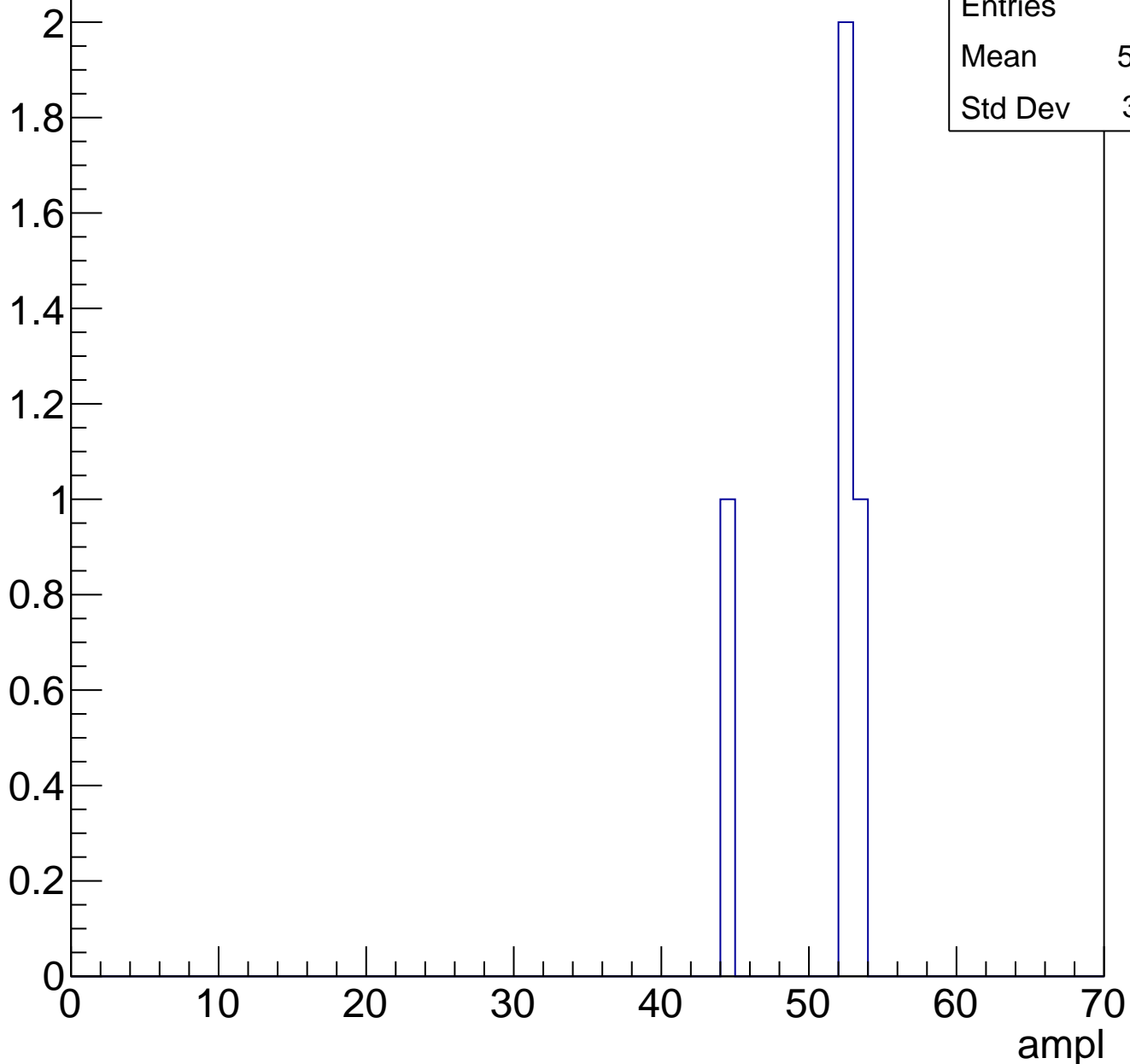
Gaus Width: 6.6630



B0L100S, U12-ch72, adc3

calib_packv5_042523_0143.root, FC#6, port A1

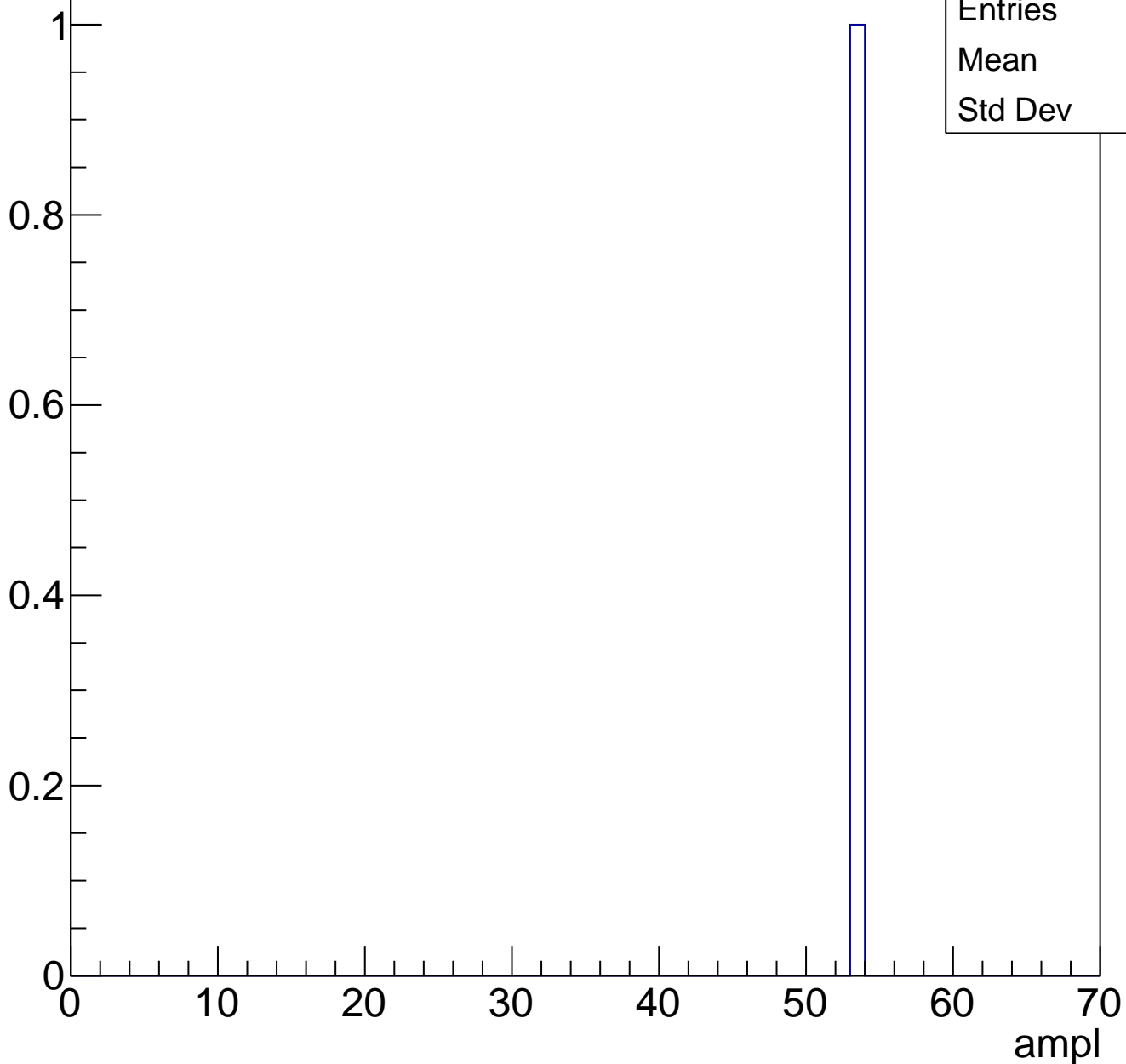
Entry



B0L100S, U12-ch72, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch72, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch72, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch72, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch73, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch73, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch73, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

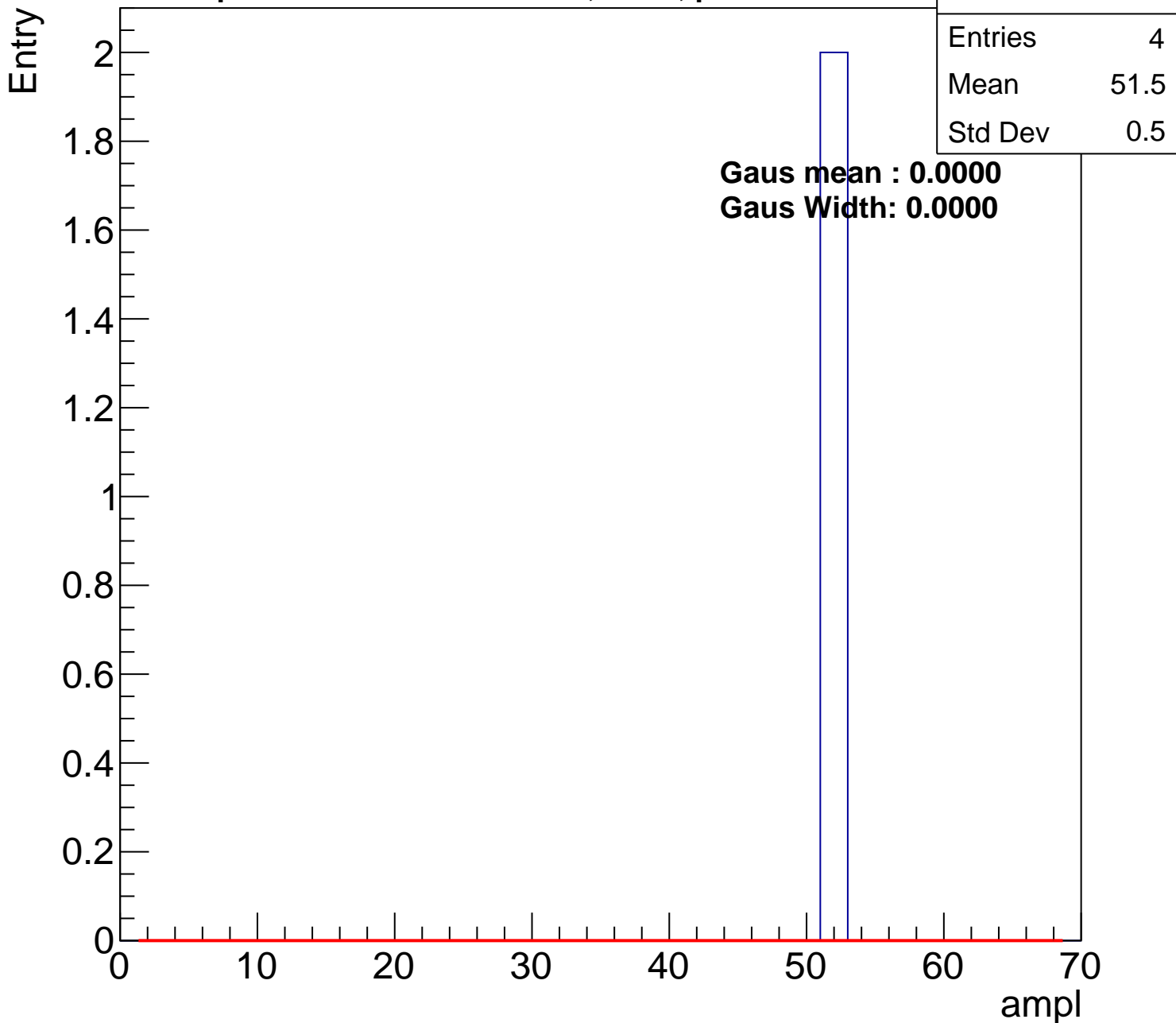
Entries	4
Mean	51.5
Std Dev	0.5

Gaus mean : 0.0000

Gaus Width: 0.0000

0 10 20 30 40 50 60 70

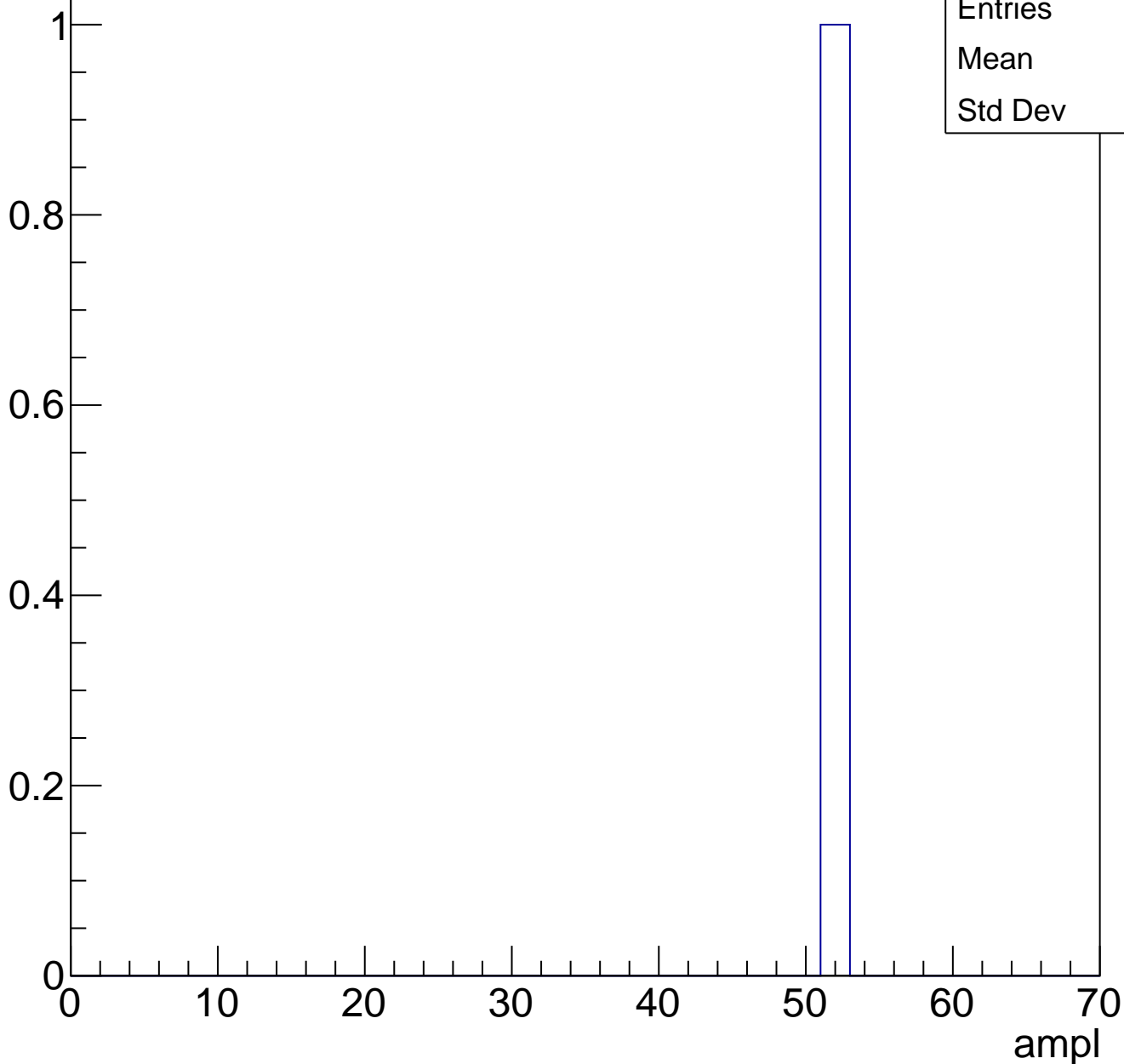
ampl



B0L100S, U12-ch73, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch73, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch73, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch73, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch73, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch74, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch74, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry

1
0.8
0.6
0.4
0.2
0

Entries	1
Mean	44
Std Dev	0

Gaus mean : 0.0000

Gaus Width: 0.0000

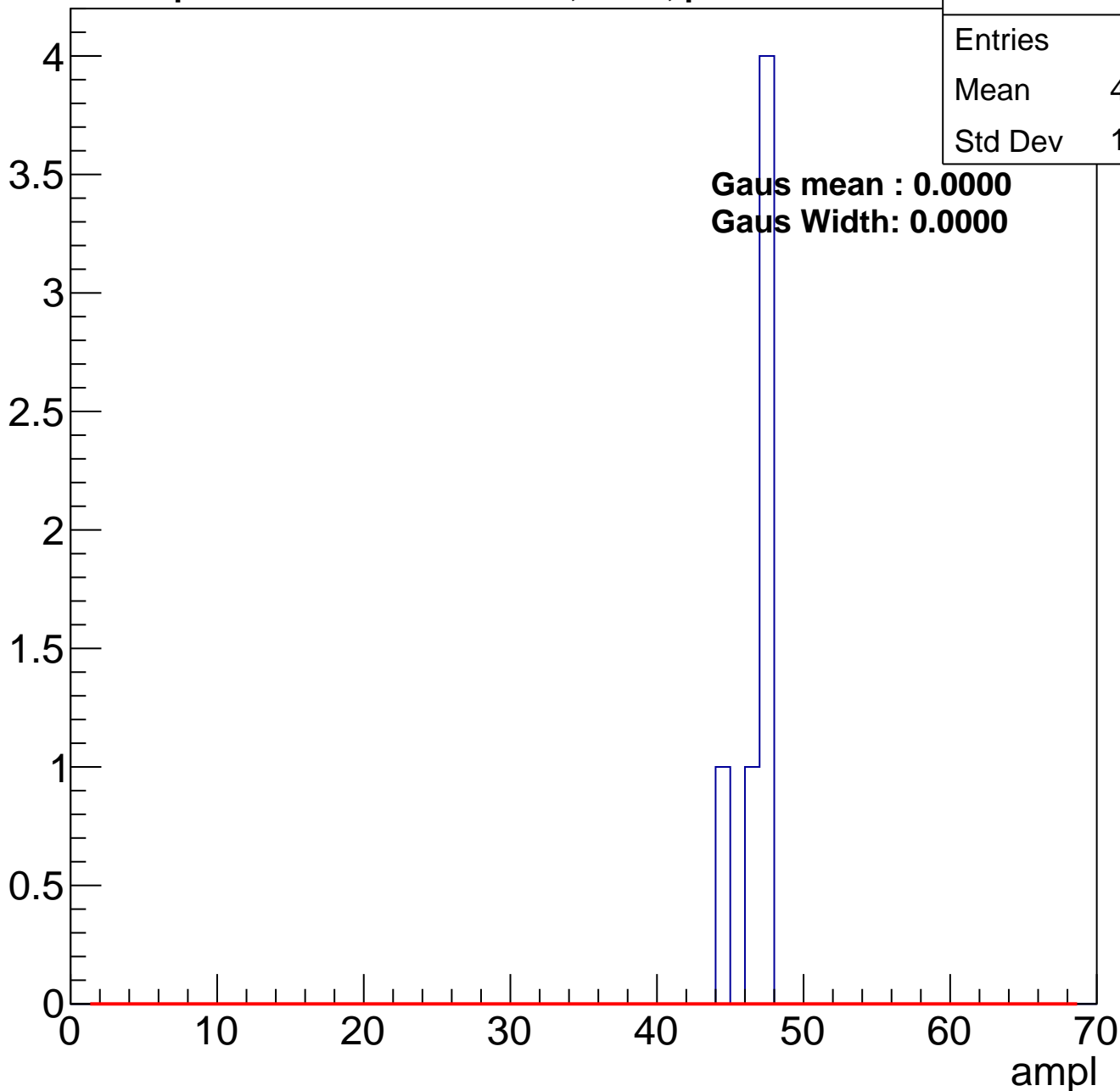
ampl

0 10 20 30 40 50 60 70

B0L100S, U12-ch74, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

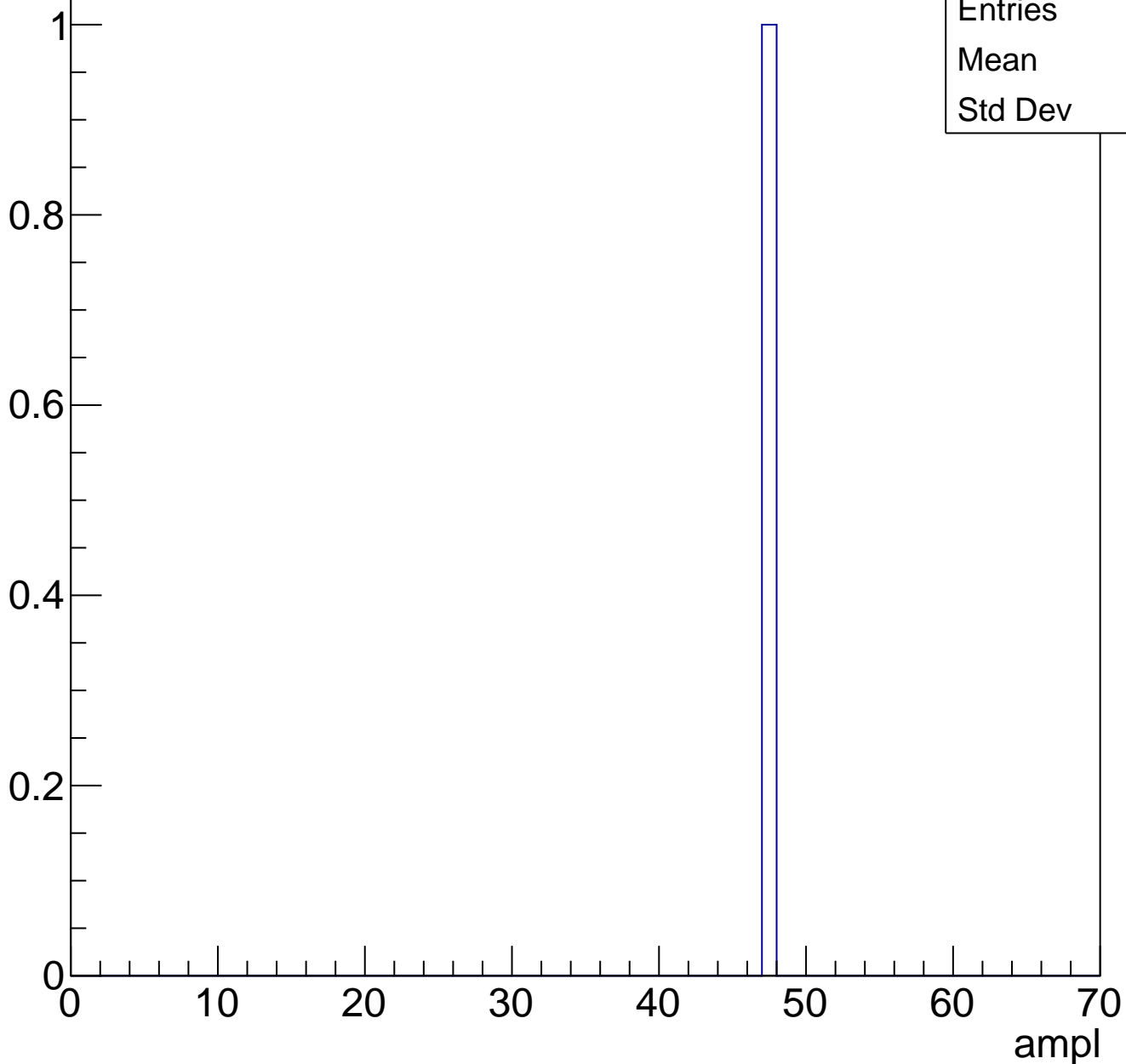


Entries	6
Mean	46.33
Std Dev	1.106

B0L100S, U12-ch74, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch74, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch74, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch74, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch74, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch75, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch75, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch75, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch75, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch75, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch75, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch75, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch75, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch76, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry

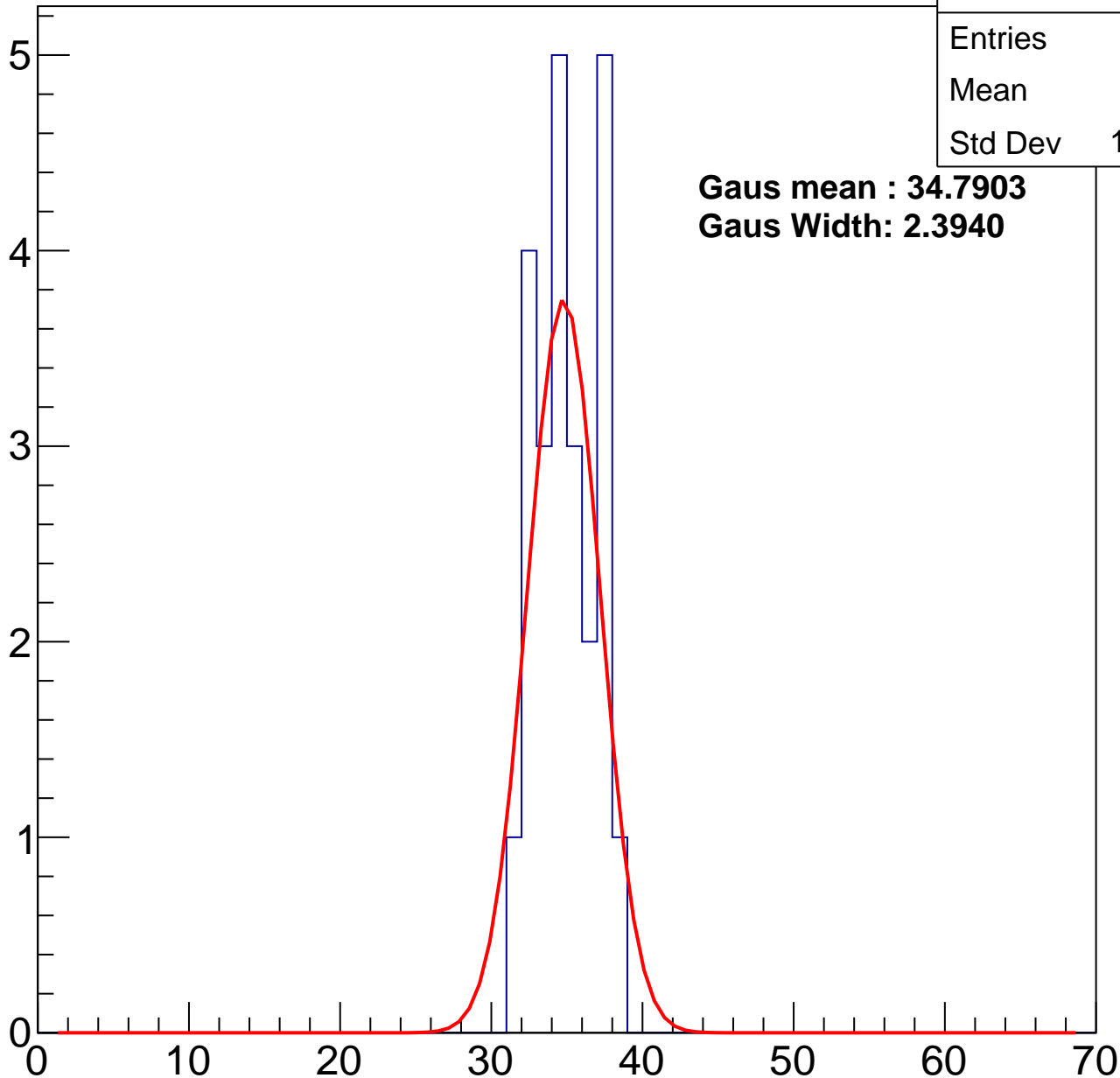
Entries	24
Mean	34.5
Std Dev	1.979

Gaus mean : 34.7903

Gaus Width: 2.3940

5
4
3
2
1
0

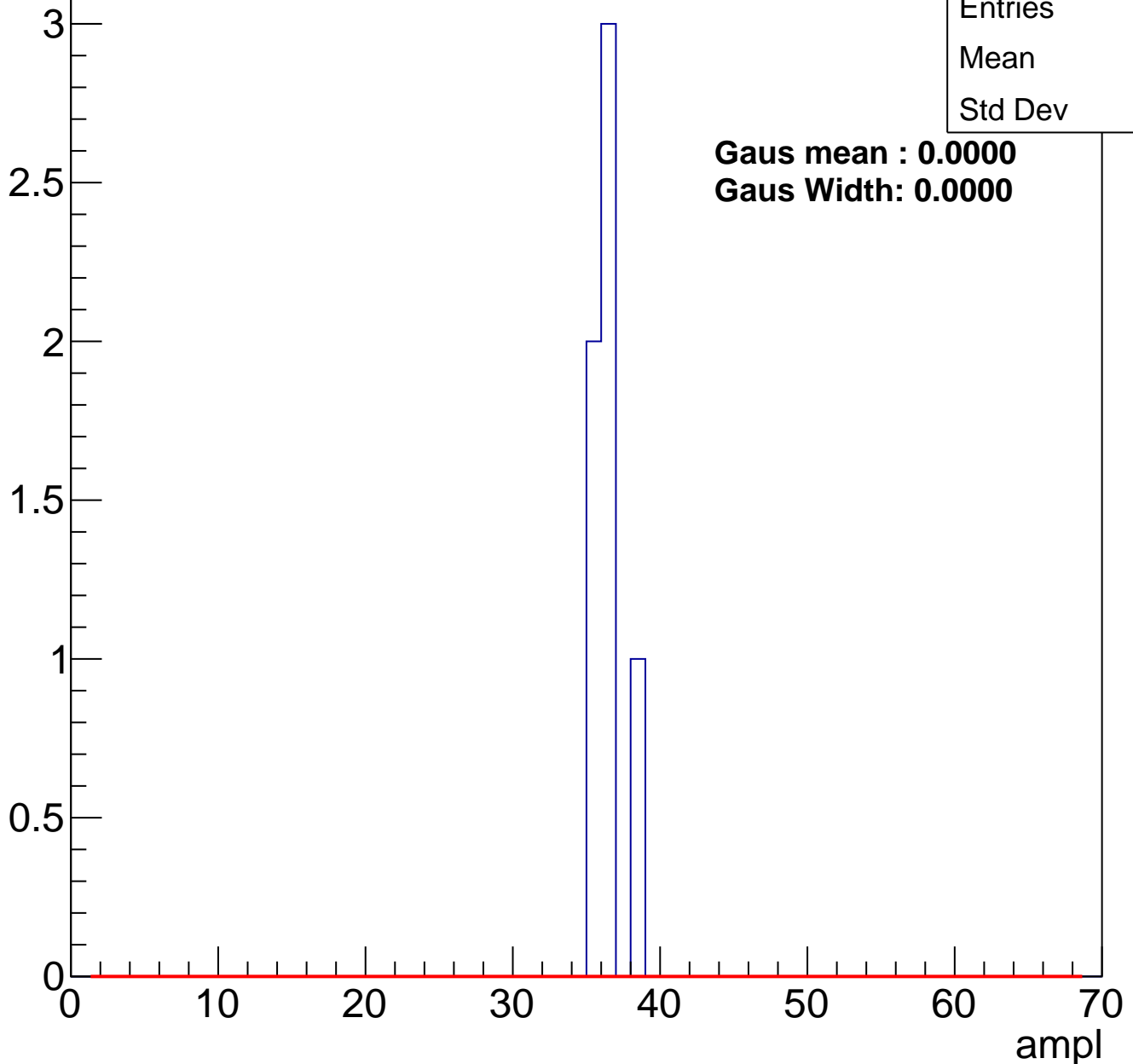
ampl



B0L100S, U12-ch76, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry

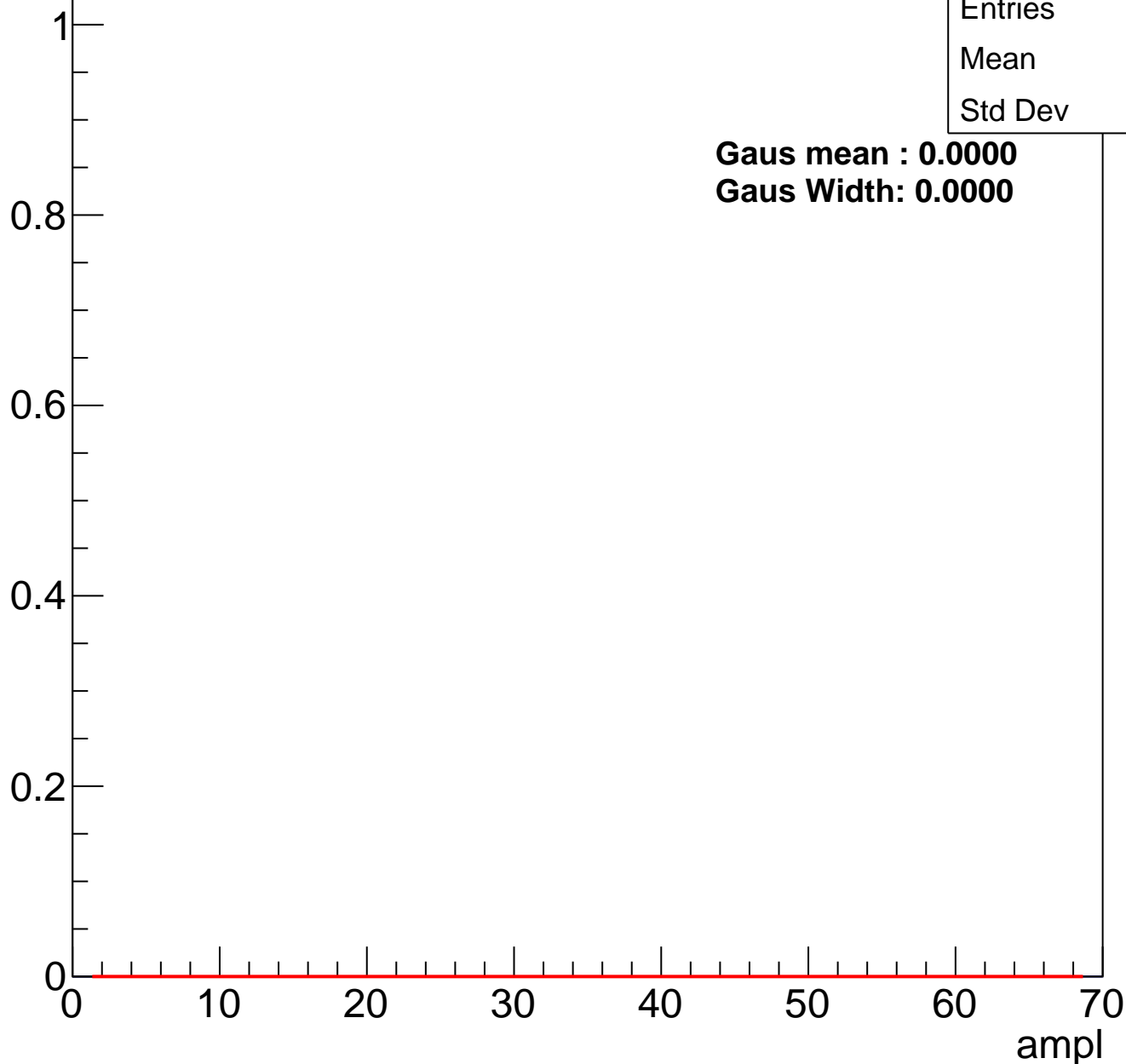


Entries	6
Mean	36
Std Dev	1

B0L100S, U12-ch76, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch76, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch76, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch76, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch76, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch76, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch77, adc0

calib_packv5_042523_0143.root, FC#6, port A1

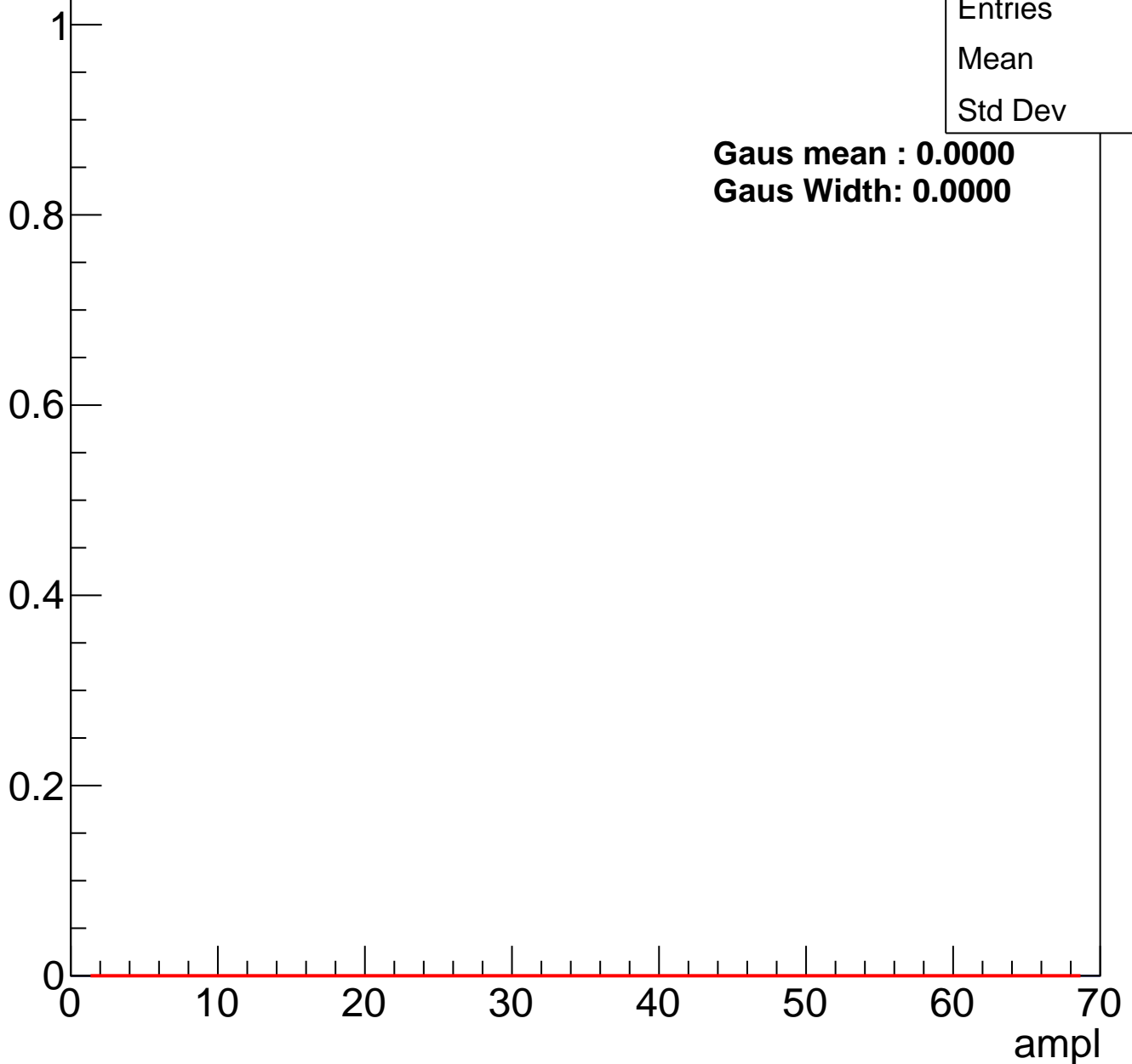
Entry



B0L100S, U12-ch77, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch77, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch77, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch77, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch77, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch77, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch77, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry

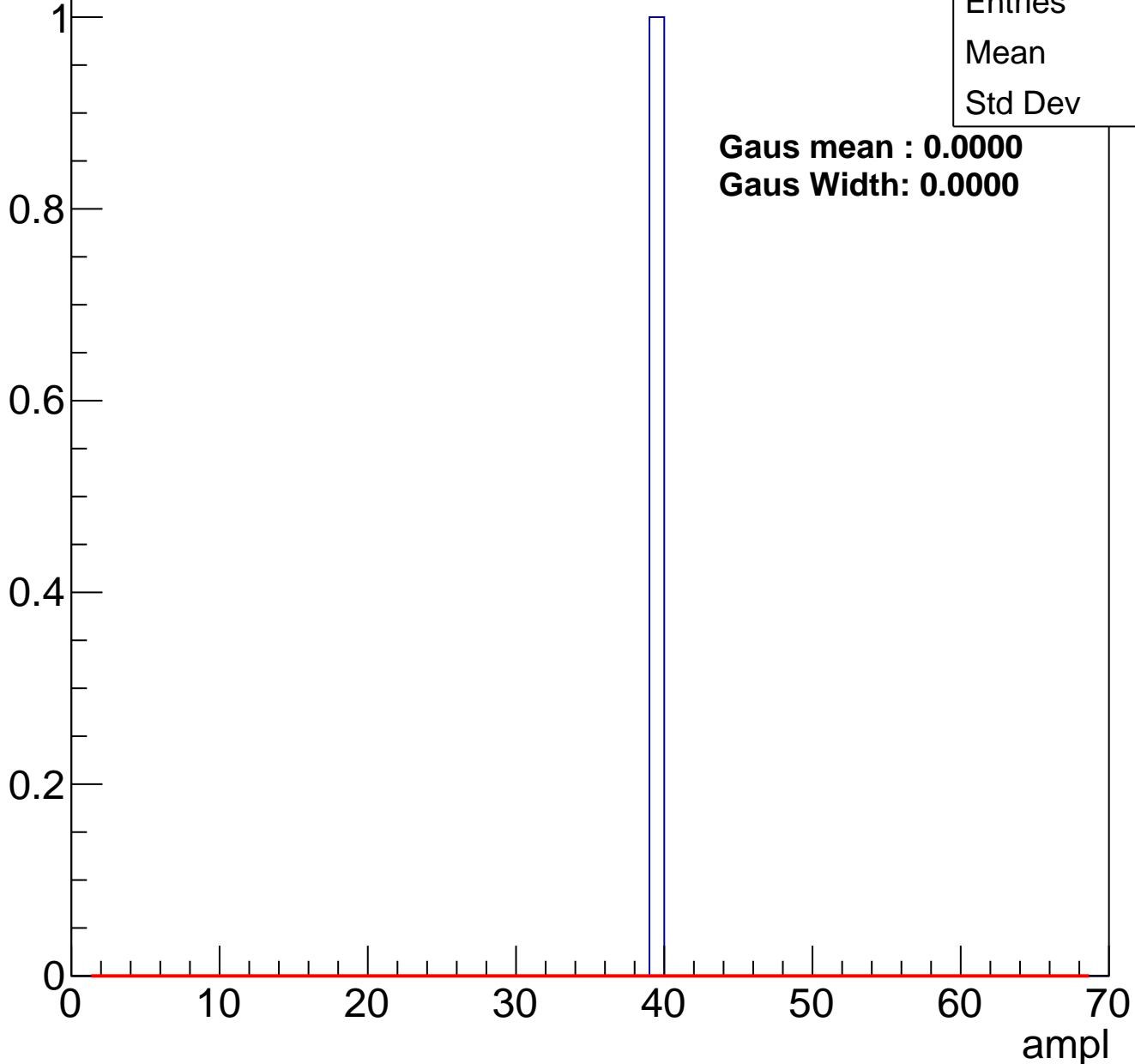


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch78, adc0

calib_packv5_042523_0143.root, FC#6, port A1

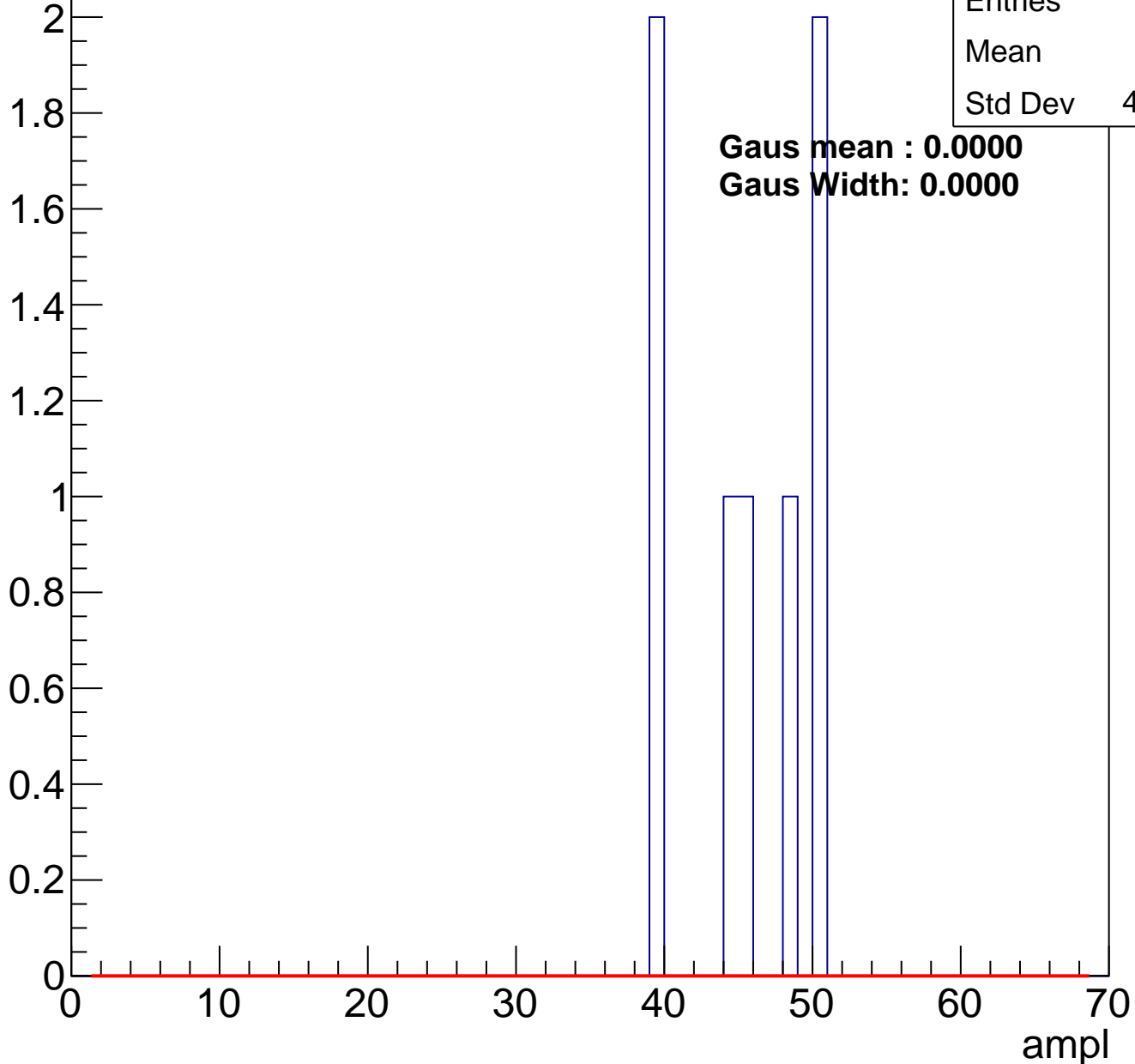
Entry



B0L100S, U12-ch78, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	7
Mean	45
Std Dev	4.342

Gaus mean : 0.0000

Gaus Width: 0.0000

B0L100S, U12-ch78, adc2

calib_packv5_042523_0143.root, FC#6, port A1

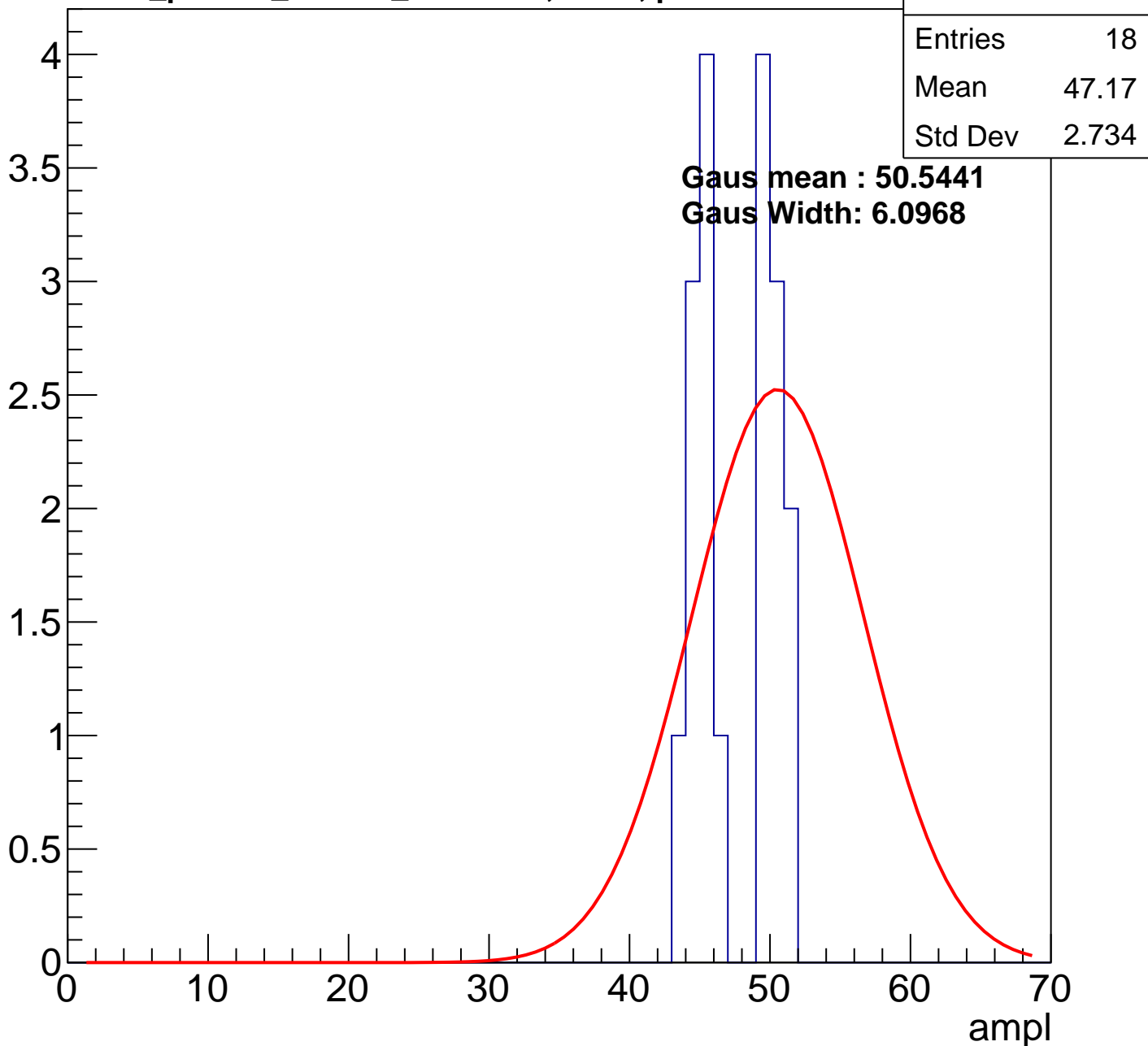
Entry

4
3.5
3
2.5
2
1.5
1
0.5
0

Entries	18
Mean	47.17
Std Dev	2.734

Gaus mean : 50.5441
Gaus Width: 6.0968

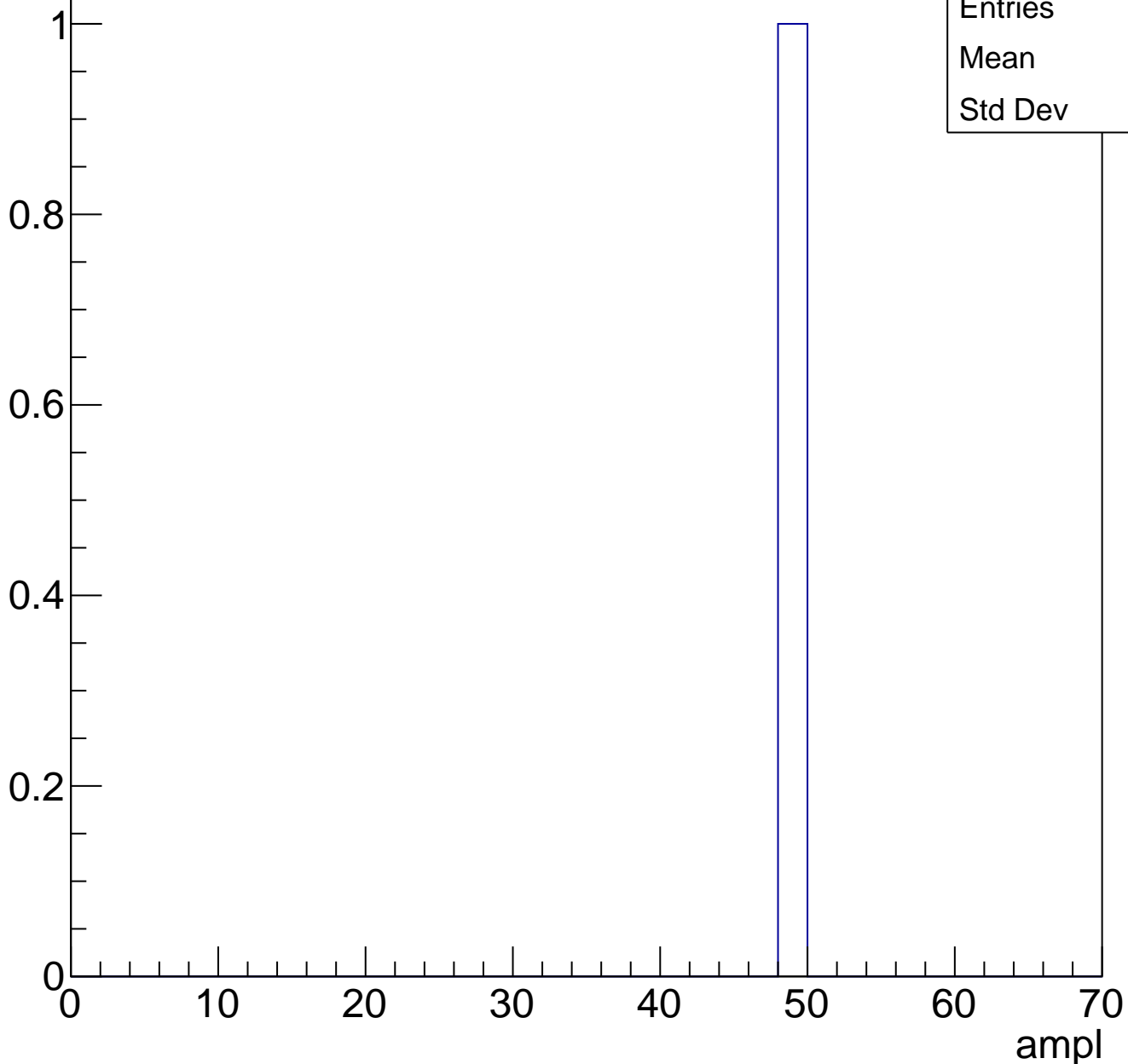
0 10 20 30 40 50 60 70
ampl



B0L100S, U12-ch78, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch78, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch78, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch78, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch78, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch79, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch79, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	7
Mean	46.43
Std Dev	1.178

Gaus mean : 0.0000

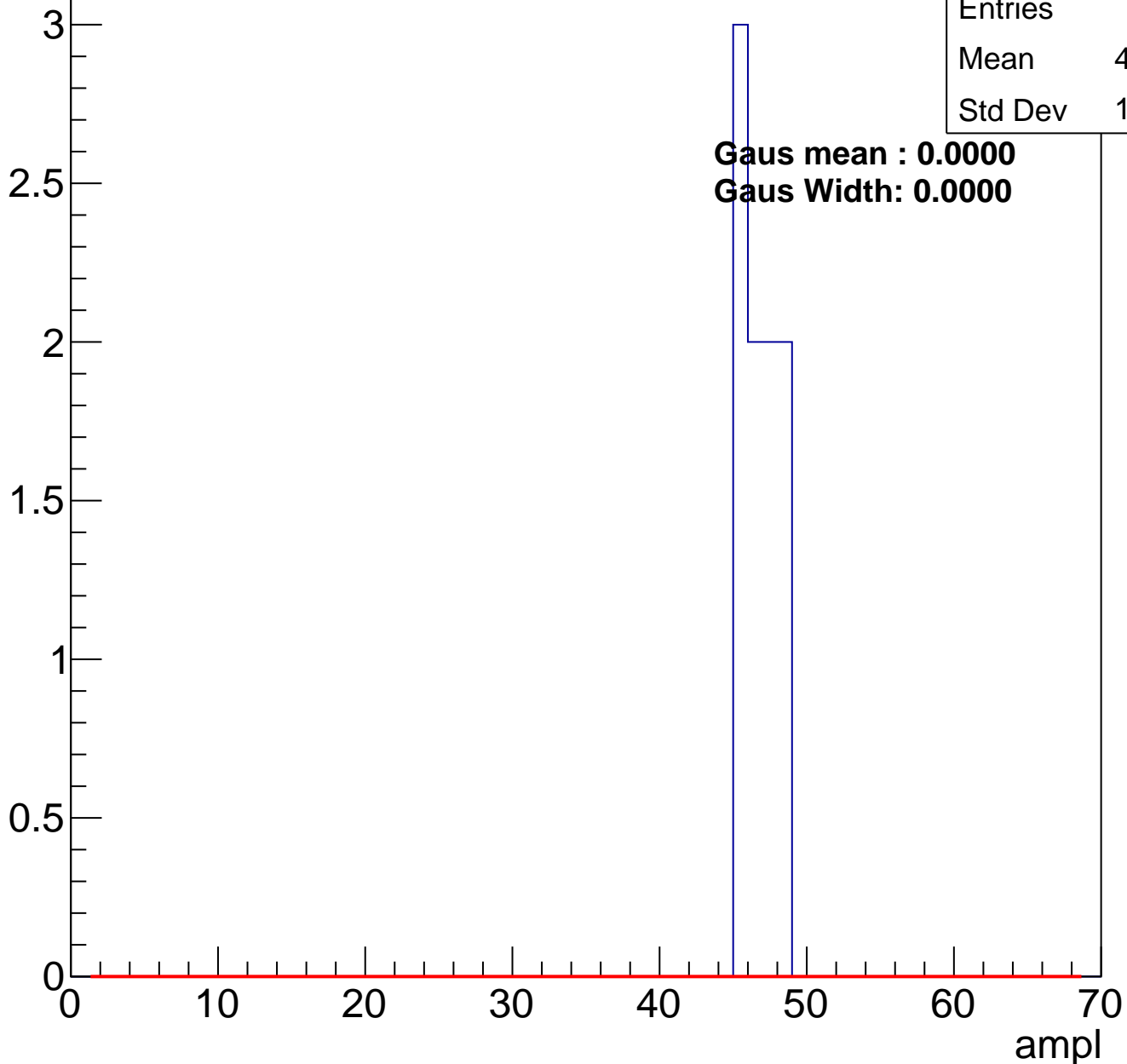
Gaus Width: 0.0000

0 10 20 30 40 50 60 70
ampl

B0L100S, U12-ch79, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

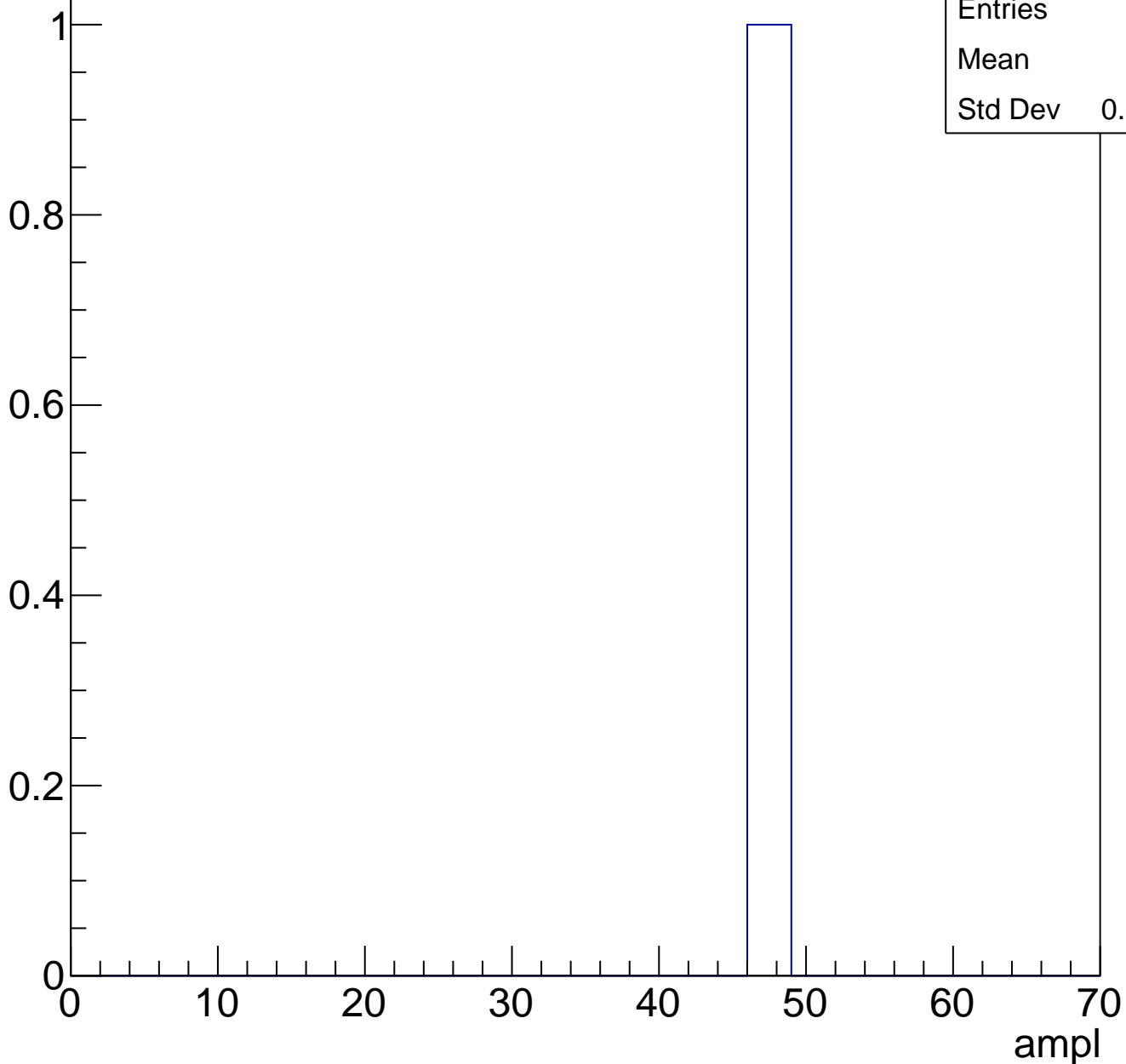


Entries	9
Mean	46.33
Std Dev	1.155

B0L100S, U12-ch79, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch79, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch79, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch79, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch79, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch80, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	1
Mean	0
Std Dev	0

B0L100S, U12-ch80, adc1

calib_packv5_042523_0143.root, FC#6, port A1

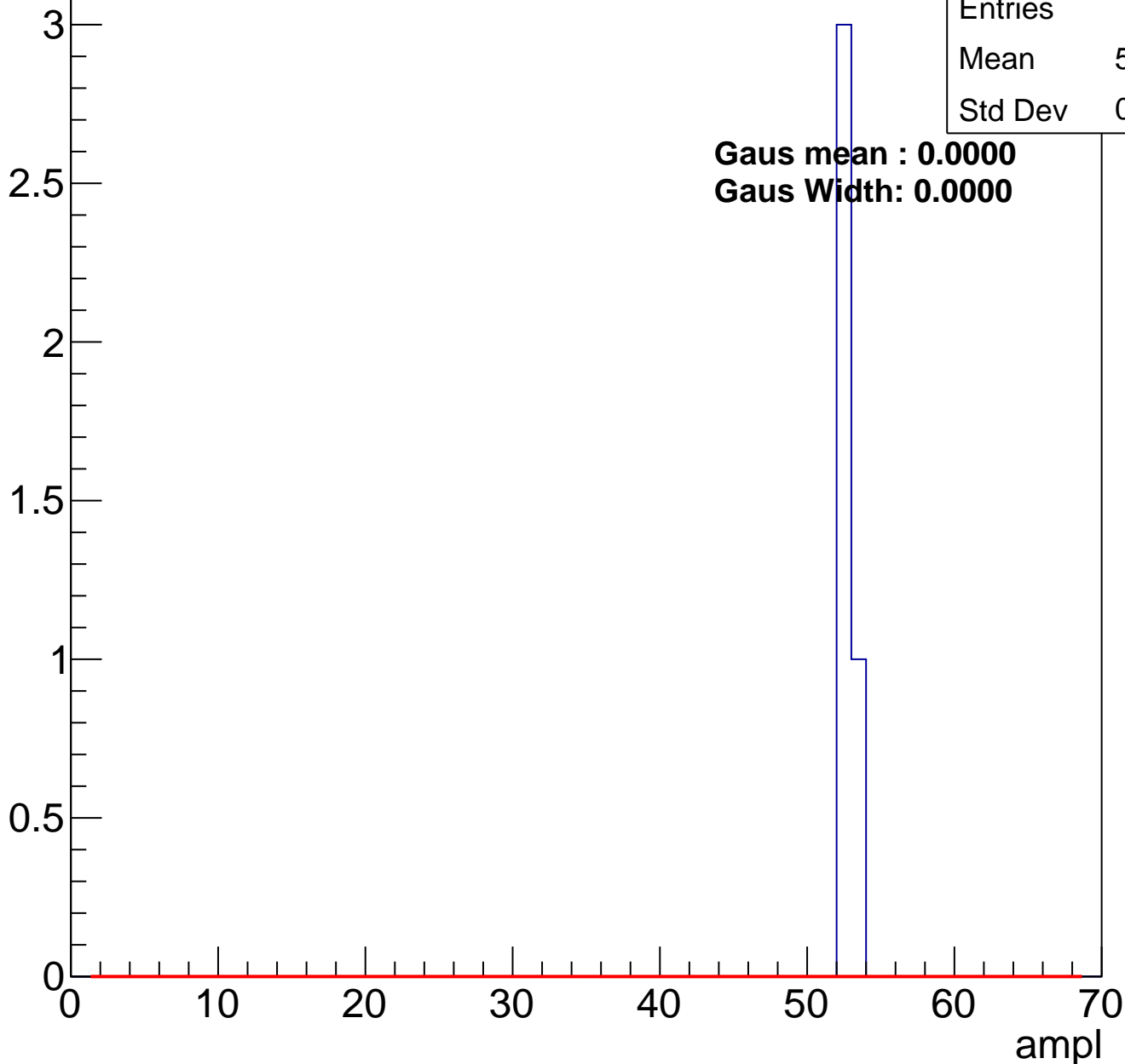
Entry



B0L100S, U12-ch80, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	4
Mean	52.25
Std Dev	0.433

B0L100S, U12-ch80, adc3

calib_packv5_042523_0143.root, FC#6, port A1

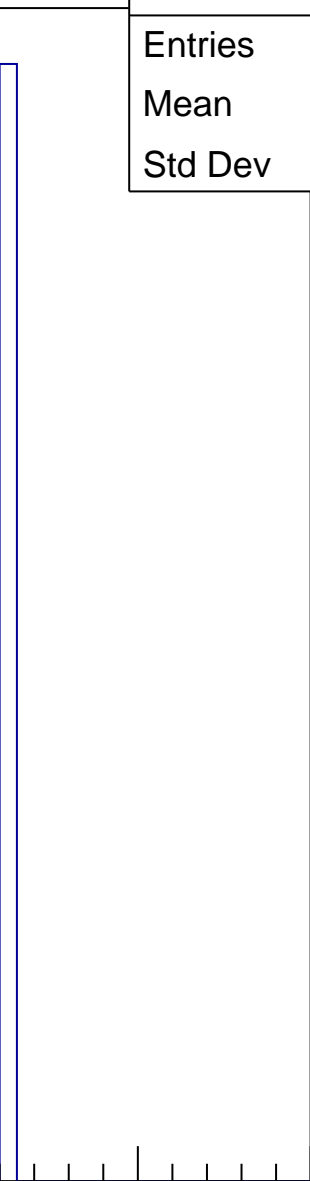
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	2
Mean	52
Std Dev	0

0 10 20 30 40 50 60 70

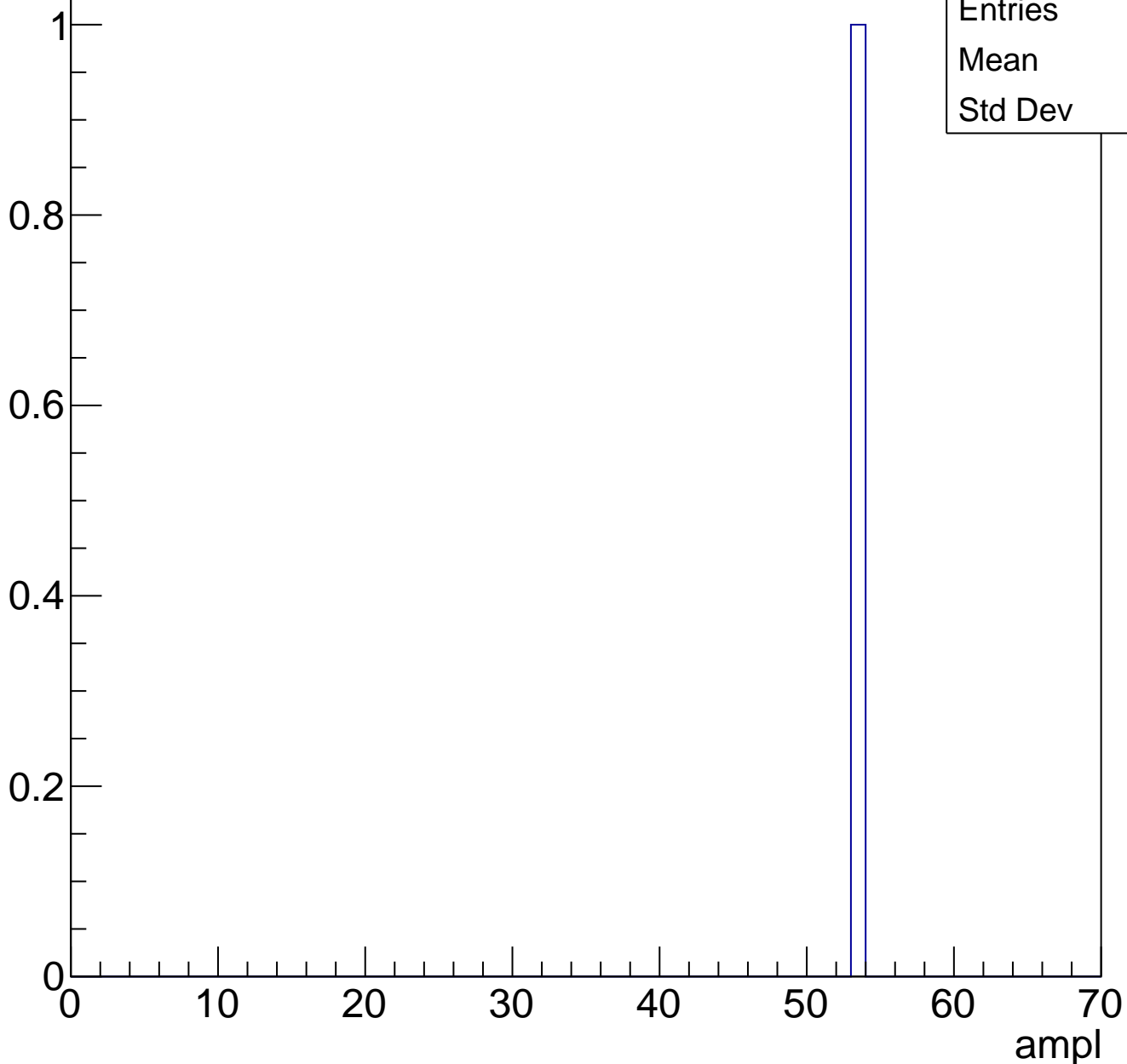
ampl



B0L100S, U12-ch80, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch80, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch80, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch80, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch81, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch81, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch81, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

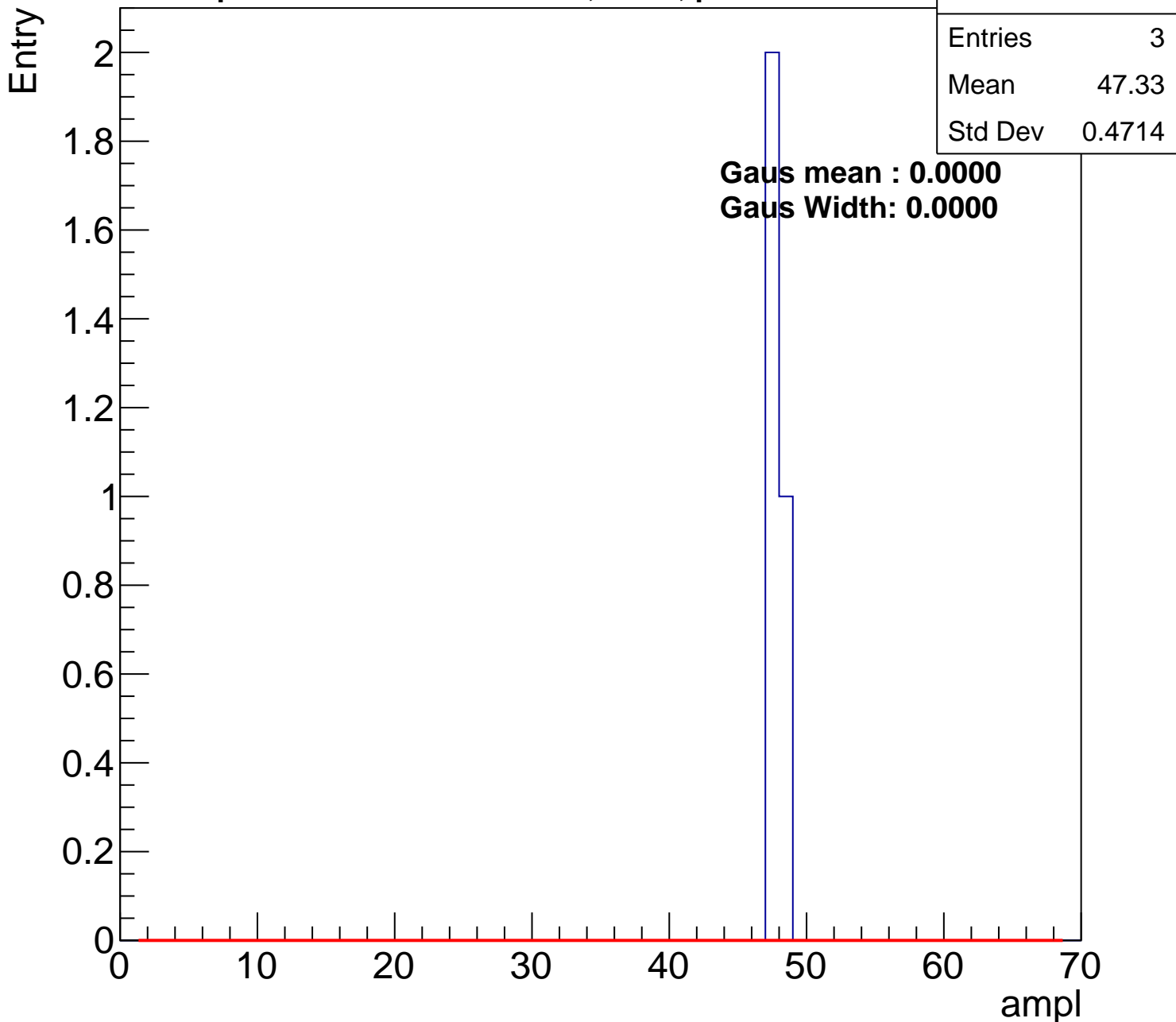
Entries	3
Mean	47.33
Std Dev	0.4714

Gaus mean : 0.0000

Gaus Width: 0.0000

0 10 20 30 40 50 60 70

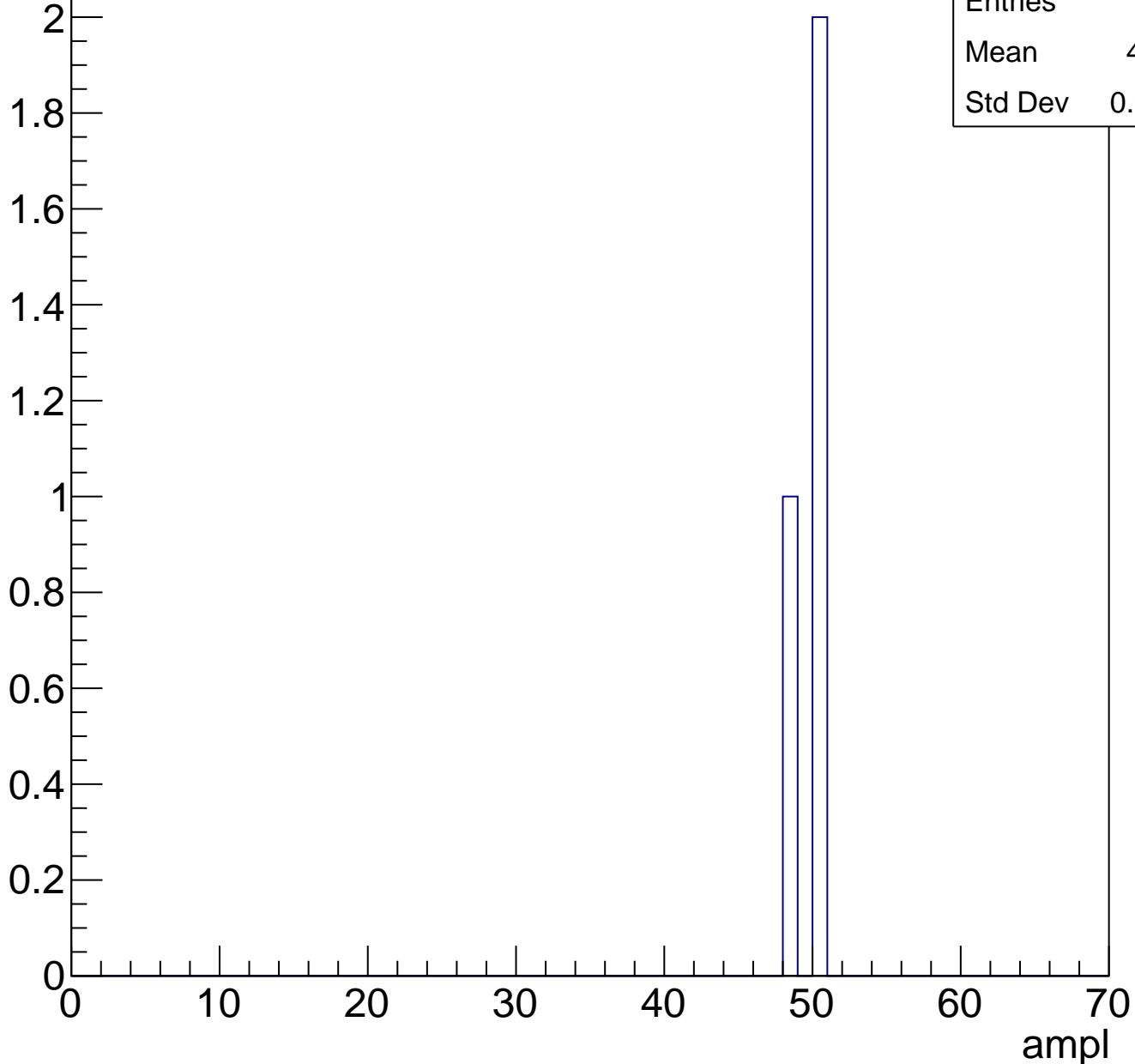
ampl



B0L100S, U12-ch81, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch81, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch81, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch81, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch81, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry

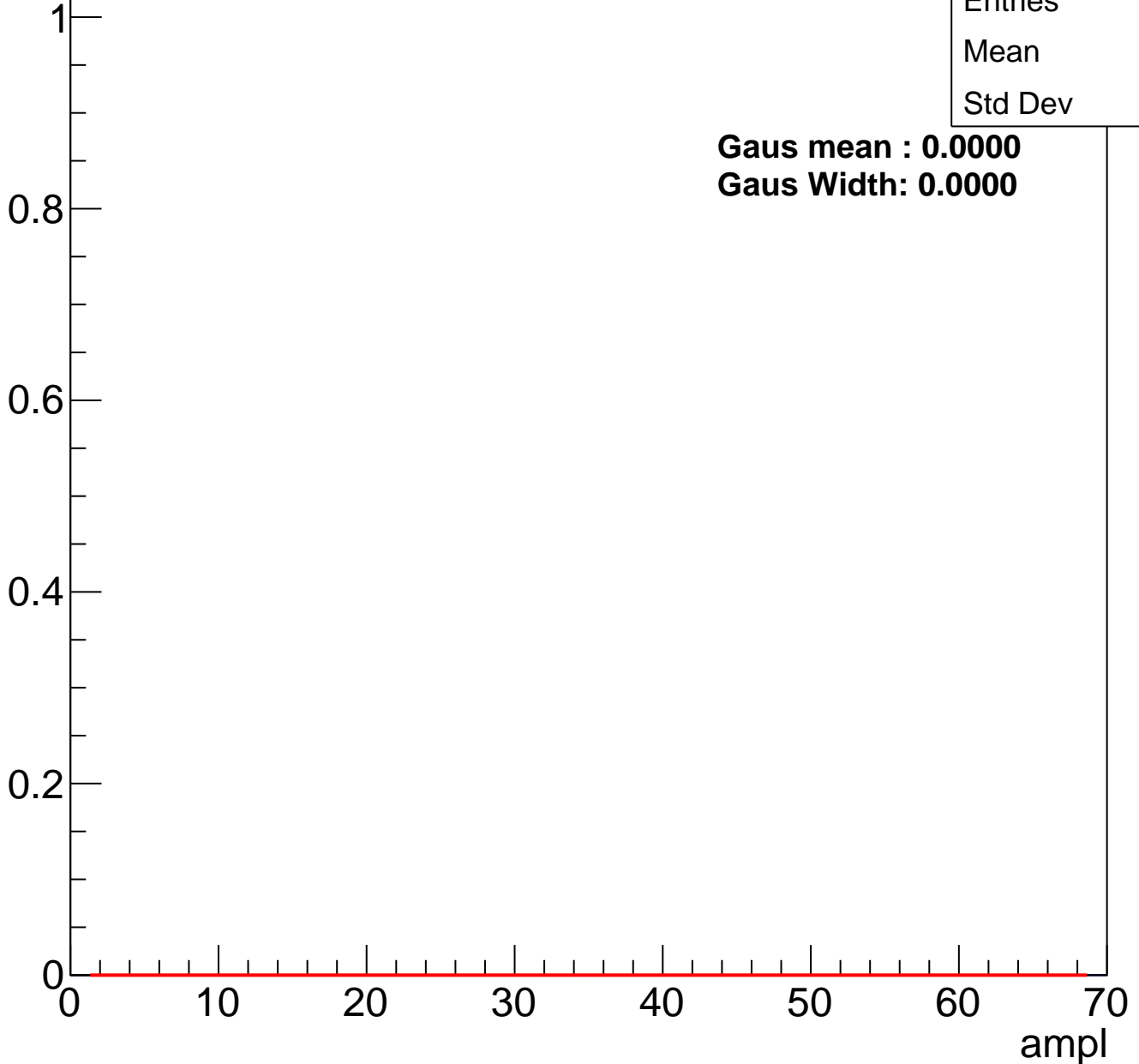


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch82, adc0

calib_packv5_042523_0143.root, FC#6, port A1

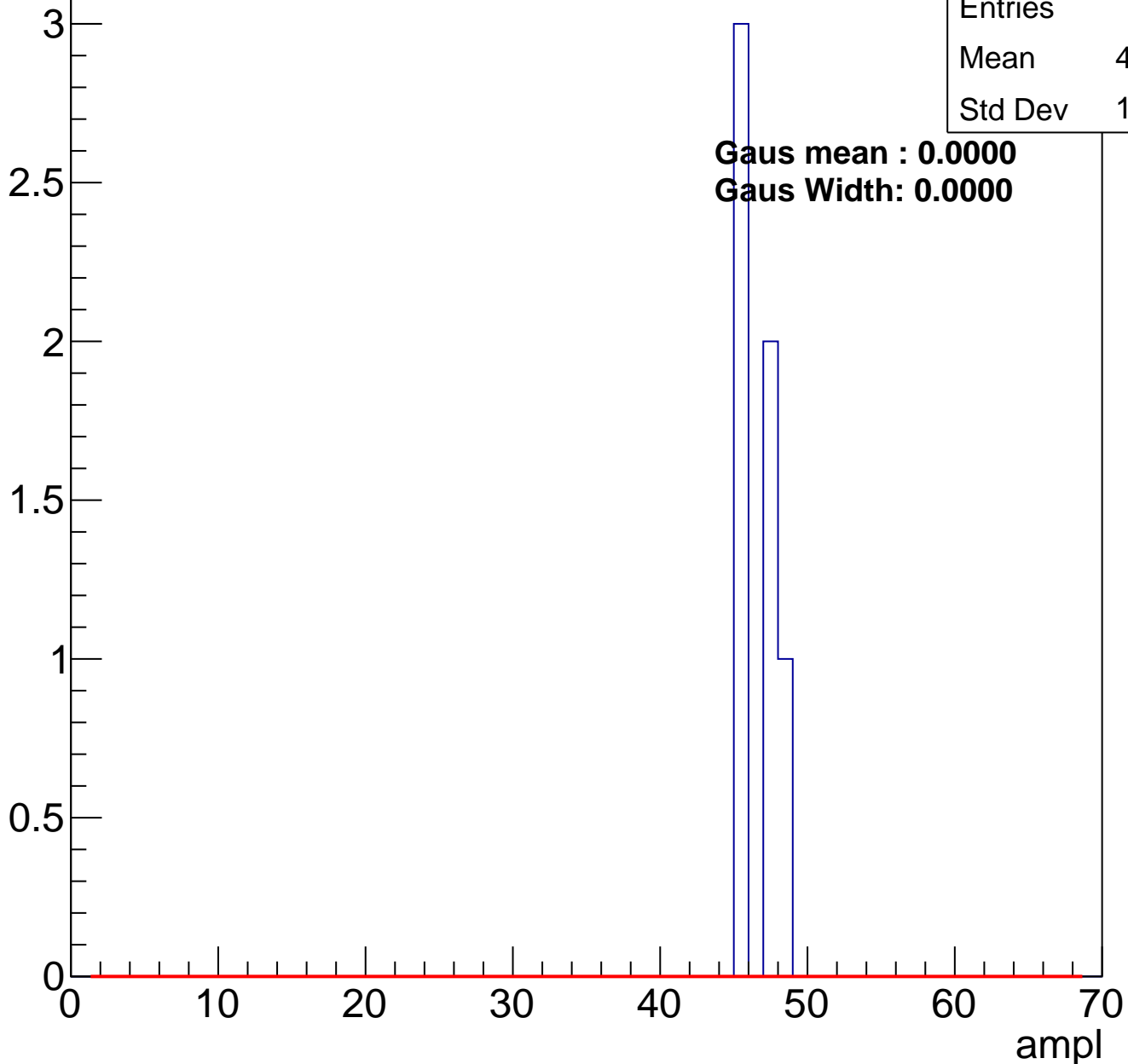
Entry



B0L100S, U12-ch82, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	6
Mean	46.17
Std Dev	1.213

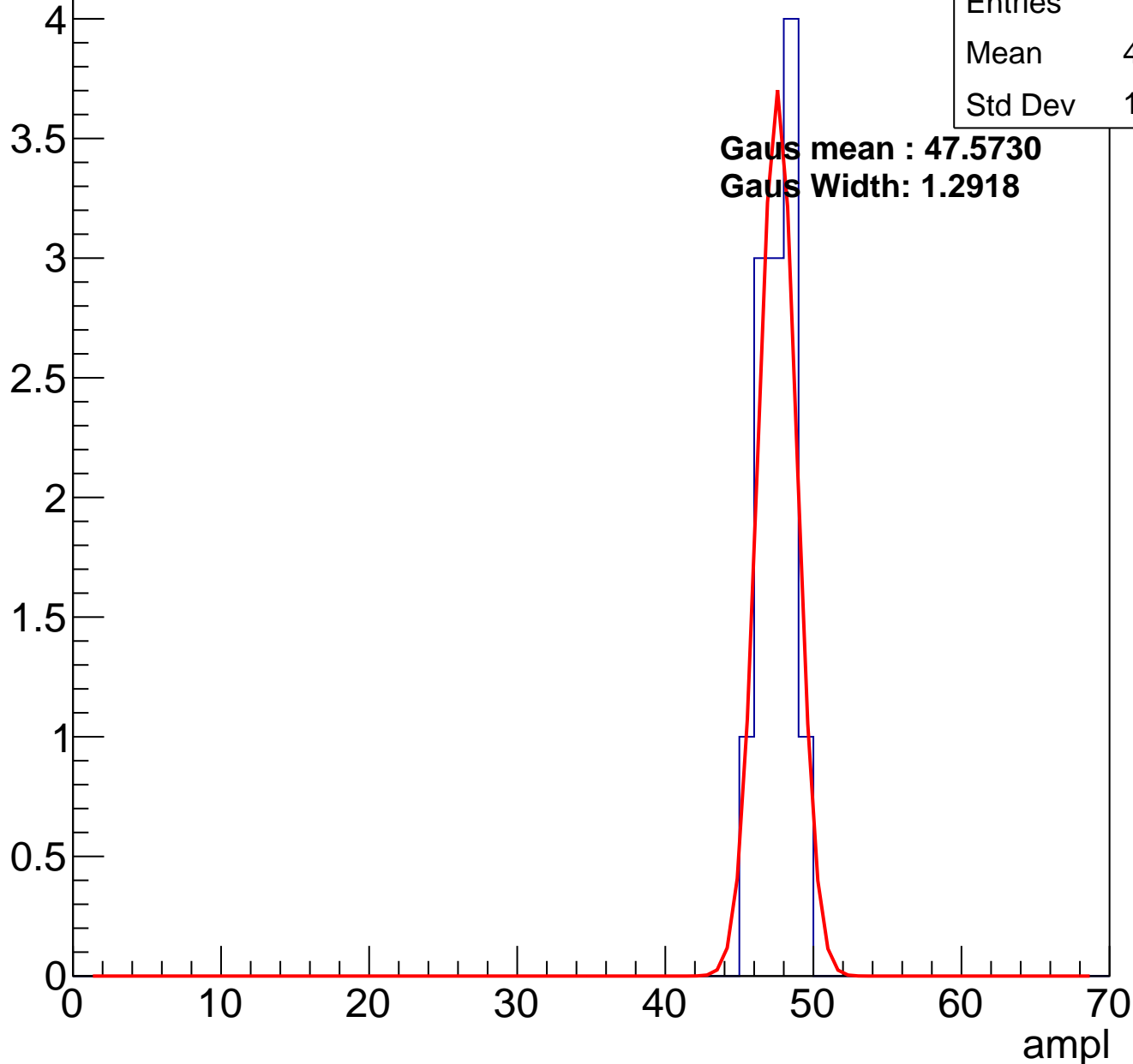
Gaus mean : 0.0000

Gaus Width: 0.0000

B0L100S, U12-ch82, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch82, adc3

calib_packv5_042523_0143.root, FC#6, port A1

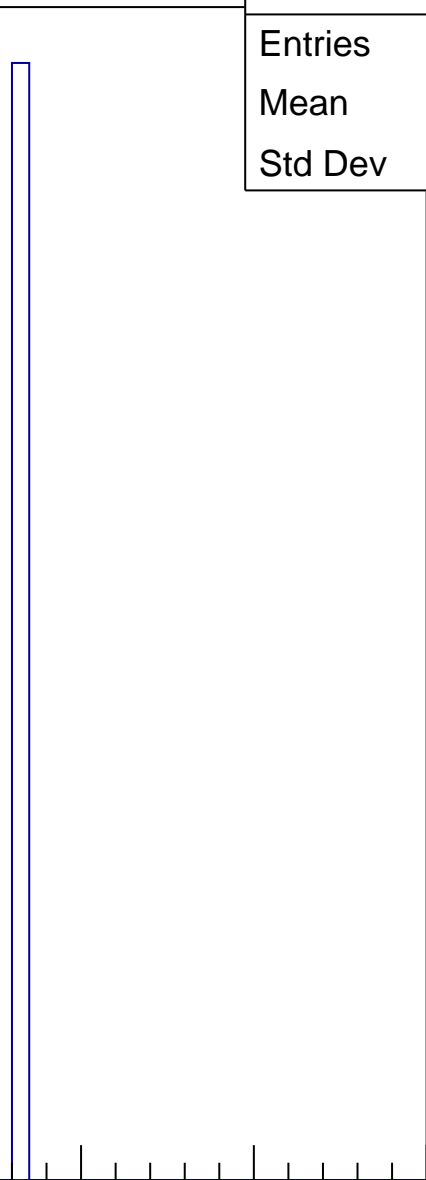
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	2
Mean	46
Std Dev	0

0 10 20 30 40 50 60 70

ampl



B0L100S, U12-ch82, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch82, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch82, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch82, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch83, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch83, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch83, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch83, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry

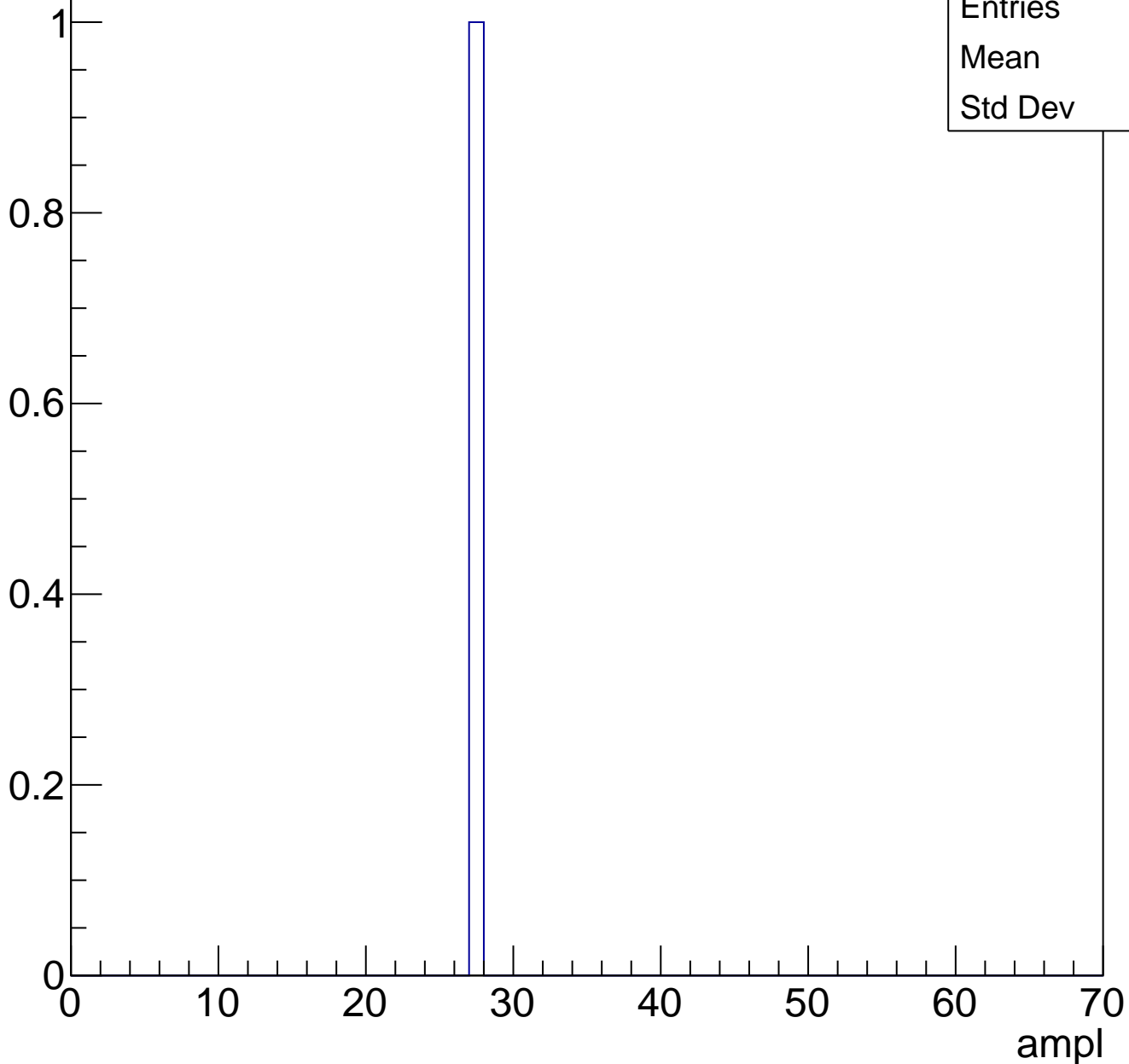


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch83, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch83, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch83, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch83, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch84, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

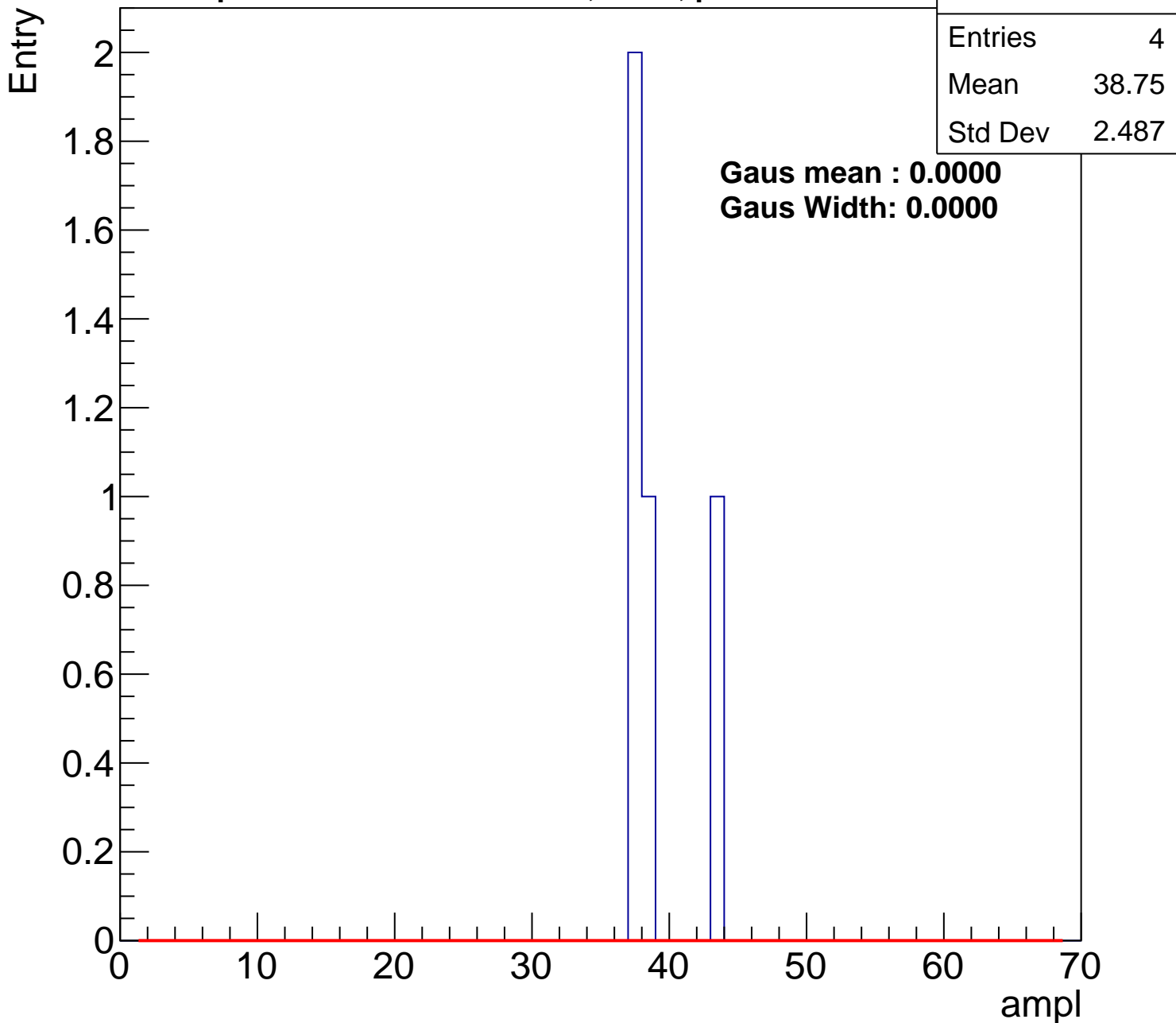
Entries	4
Mean	38.75
Std Dev	2.487

Gaus mean : 0.0000

Gaus Width: 0.0000

0 10 20 30 40 50 60 70

ampl



B0L100S, U12-ch84, adc1

calib_packv5_042523_0143.root, FC#6, port A1

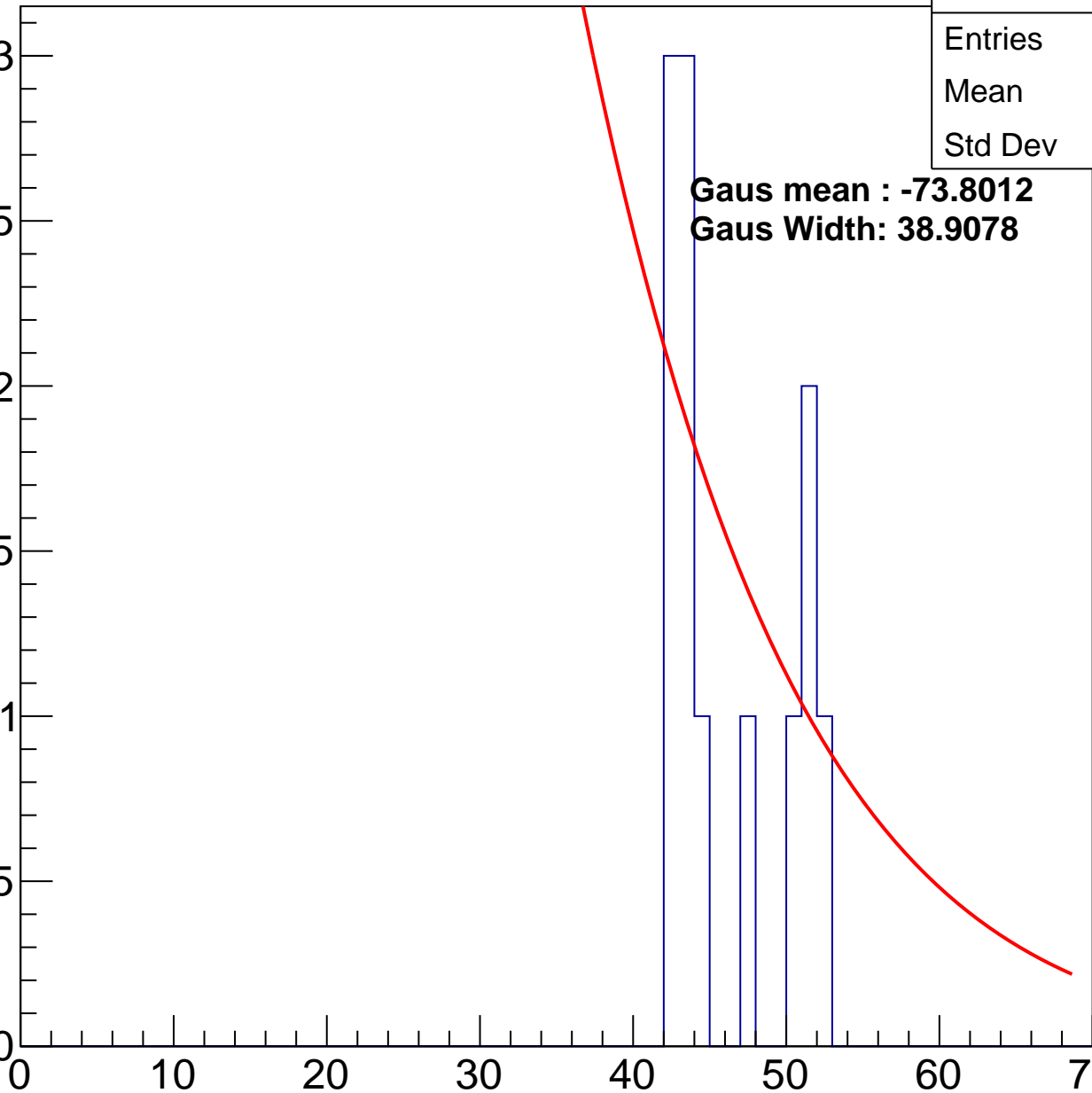
Entry

3
2.5
2
1.5
1
0.5
0

Entries	12
Mean	45.83
Std Dev	3.891

Gaus mean : -73.8012
Gaus Width: 38.9078

ampl



B0L100S, U12-ch84, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

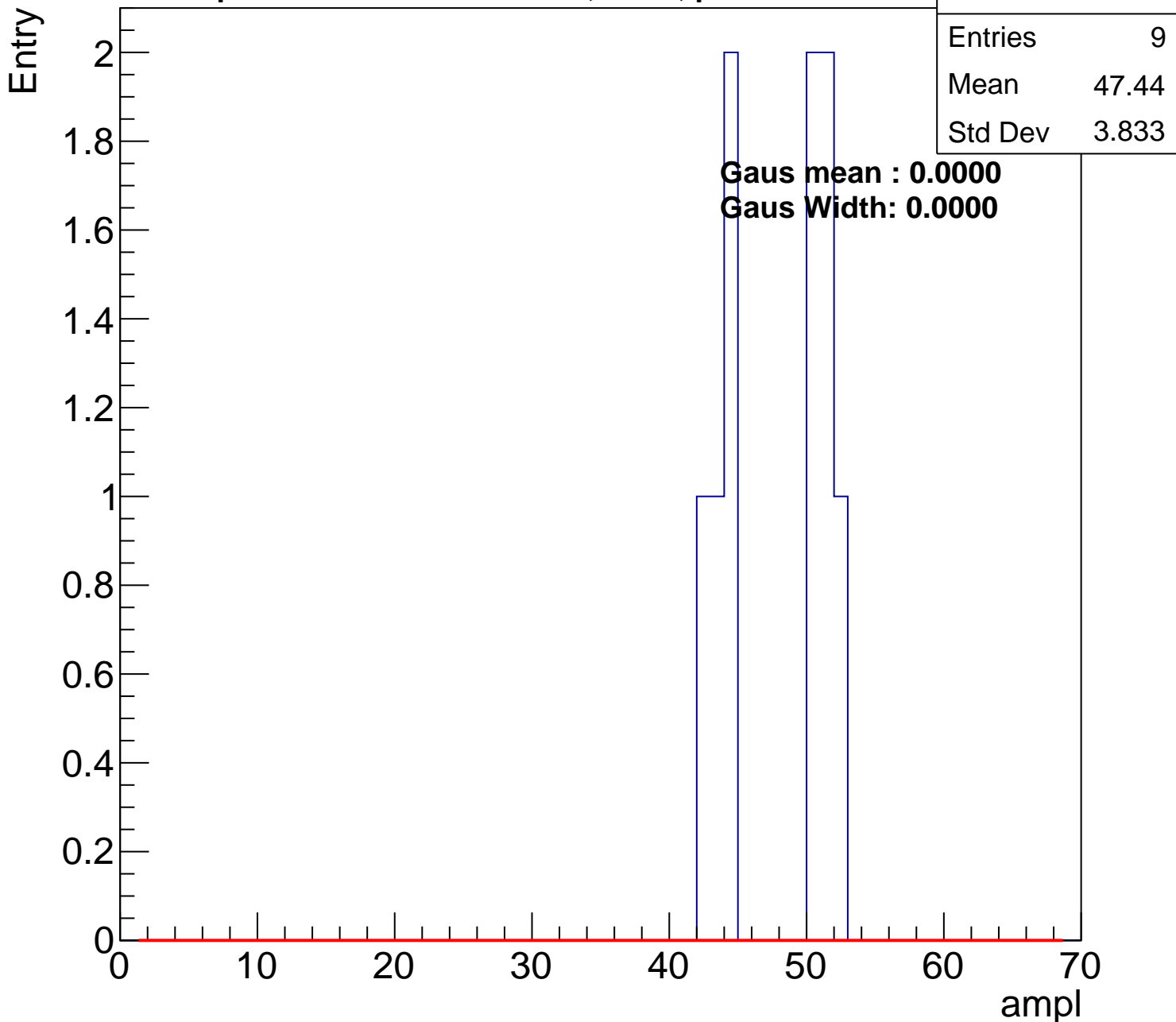
Entries	9
Mean	47.44
Std Dev	3.833

Gaus mean : 0.0000

Gaus Width: 0.0000

0 10 20 30 40 50 60 70

ampl



B0L100S, U12-ch84, adc3

calib_packv5_042523_0143.root, FC#6, port A1

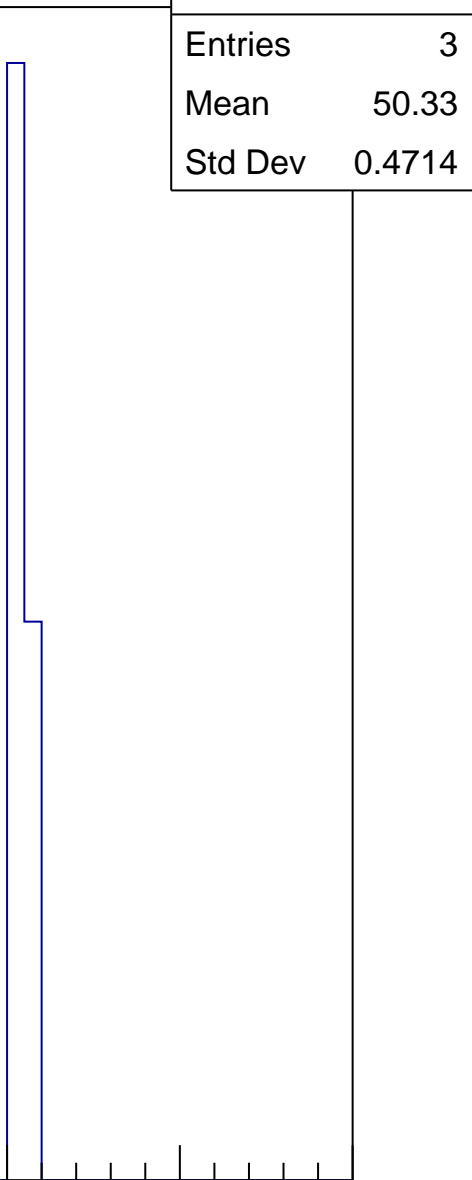
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	3
Mean	50.33
Std Dev	0.4714

0 10 20 30 40 50 60 70

ampl



B0L100S, U12-ch84, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch84, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch84, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch84, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch85, adc0

calib_packv5_042523_0143.root, FC#6, port A1

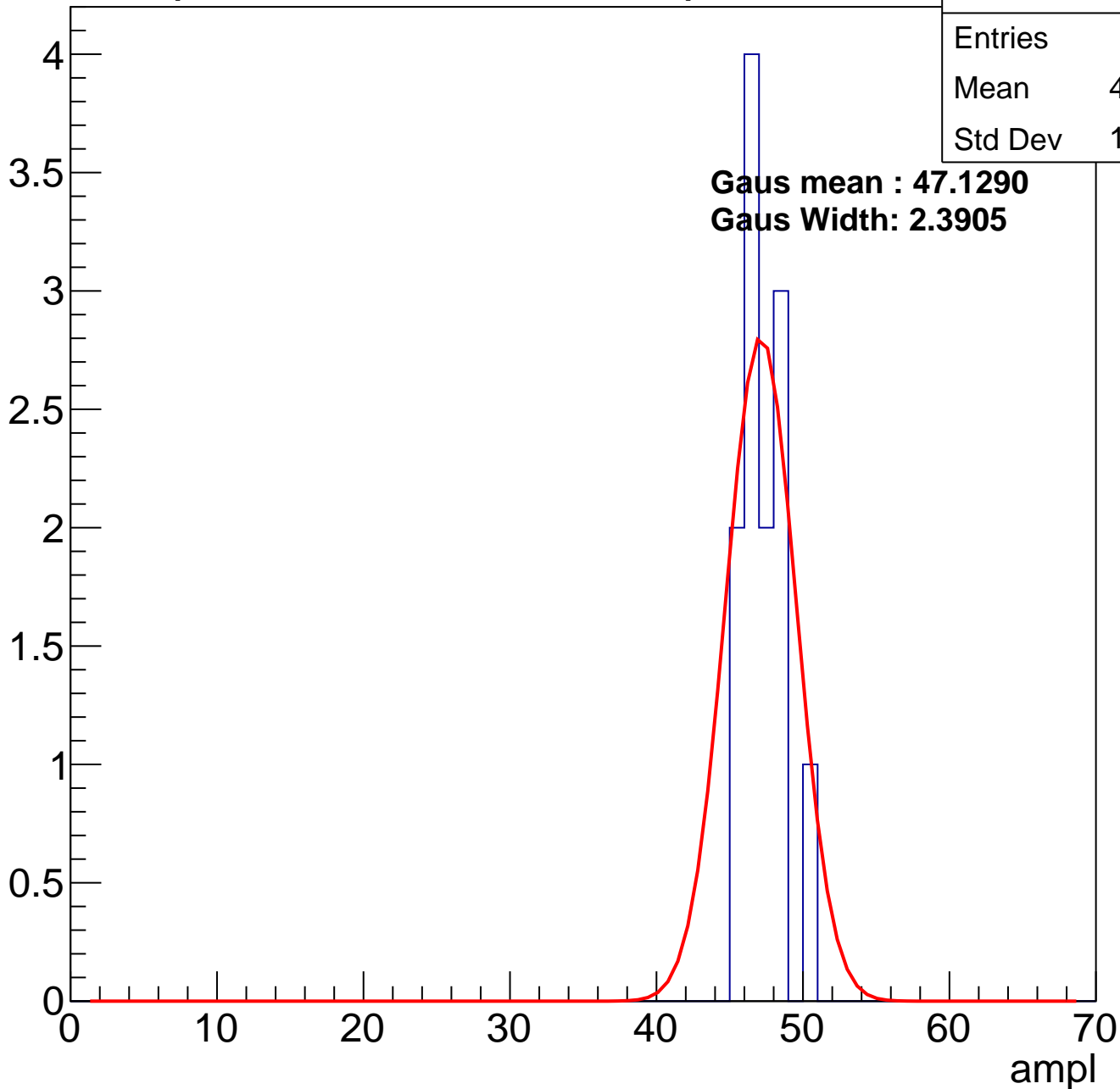
Entry



B0L100S, U12-ch85, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch85, adc2

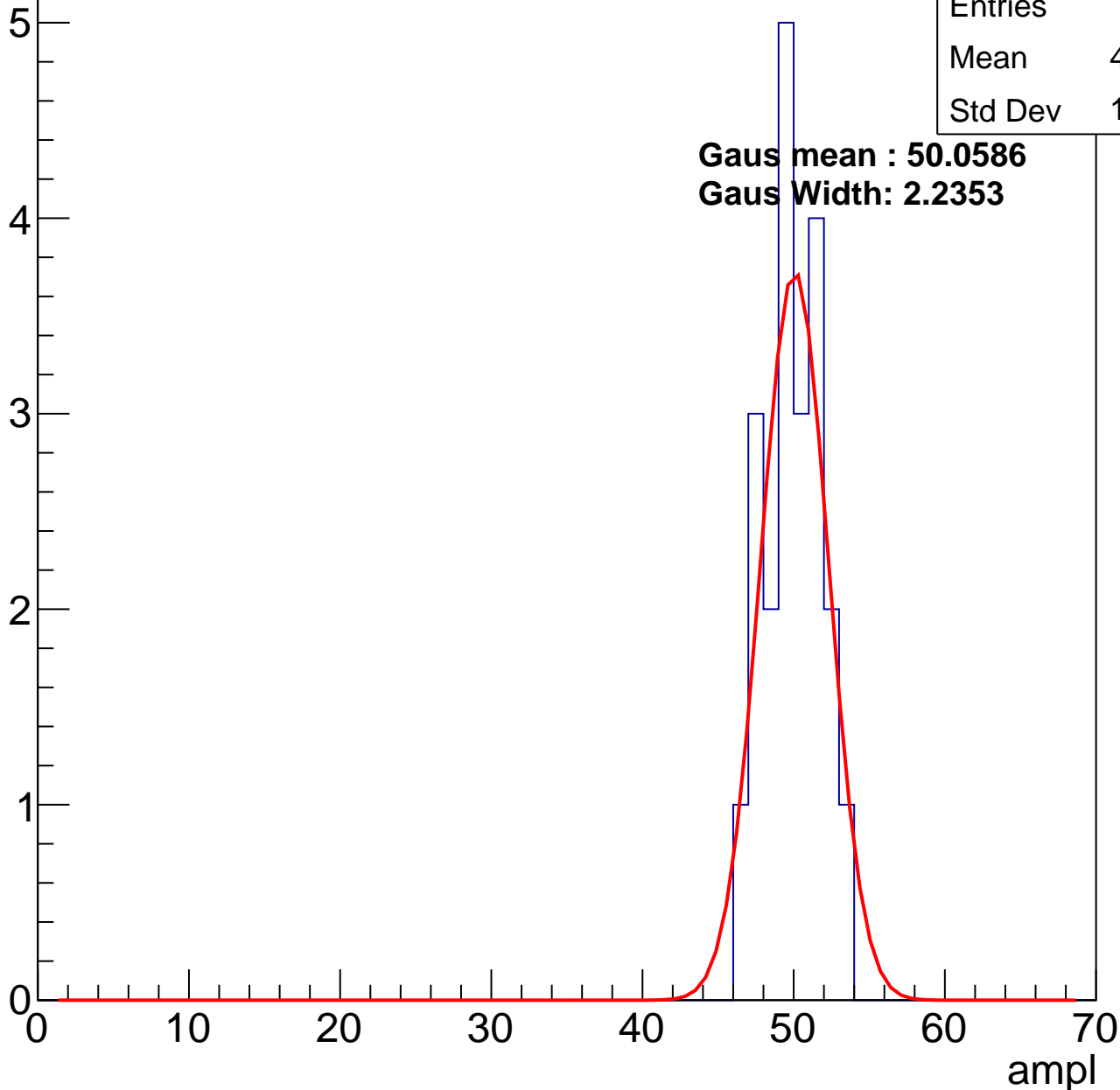
calib_packv5_042523_0143.root, FC#6, port A1

Entry

Entries	21
Mean	49.48
Std Dev	1.842

Gaus mean : 50.0586

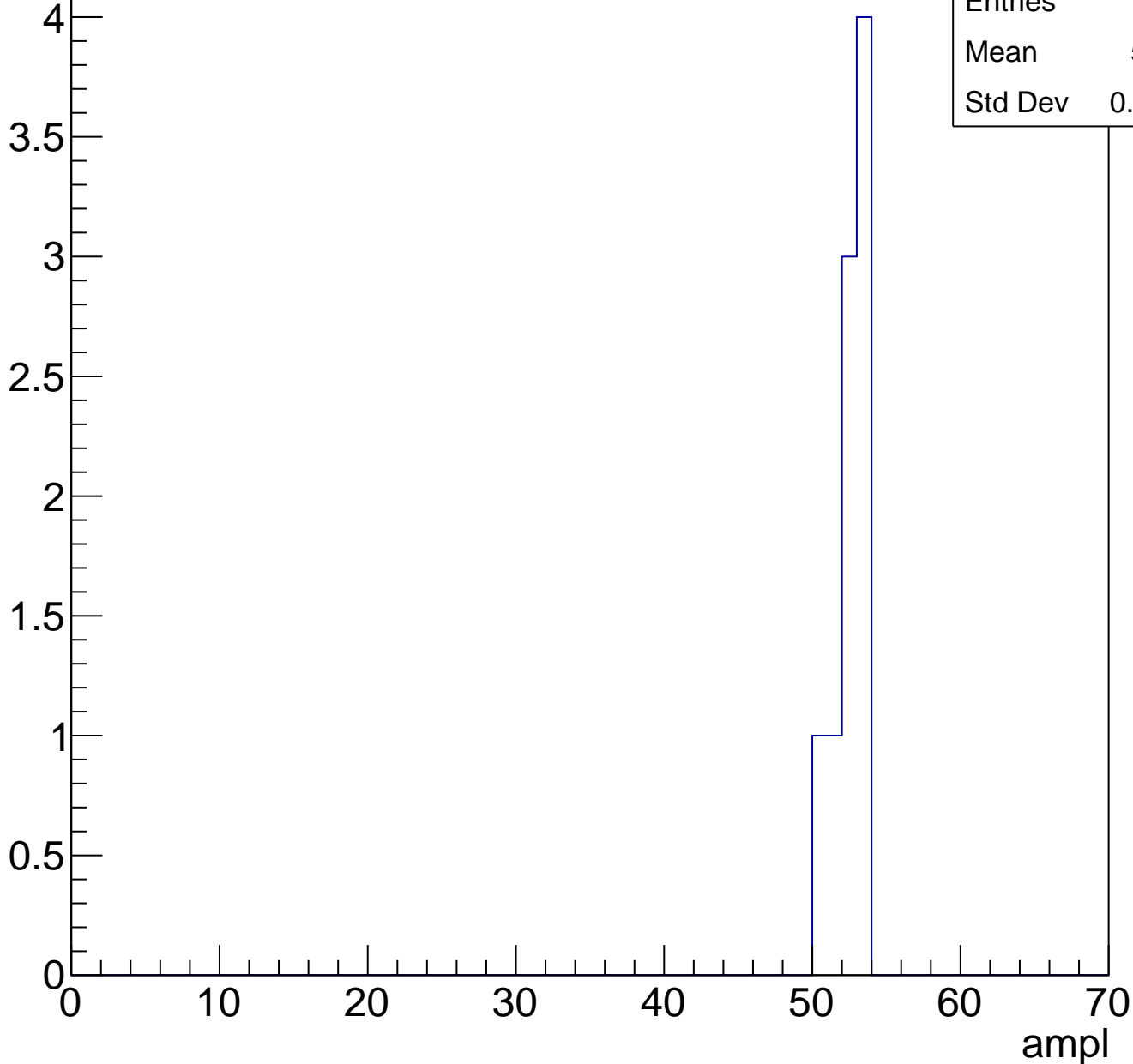
Gaus Width: 2.2353



B0L100S, U12-ch85, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch85, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch85, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch85, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch85, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch86, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch86, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch86, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

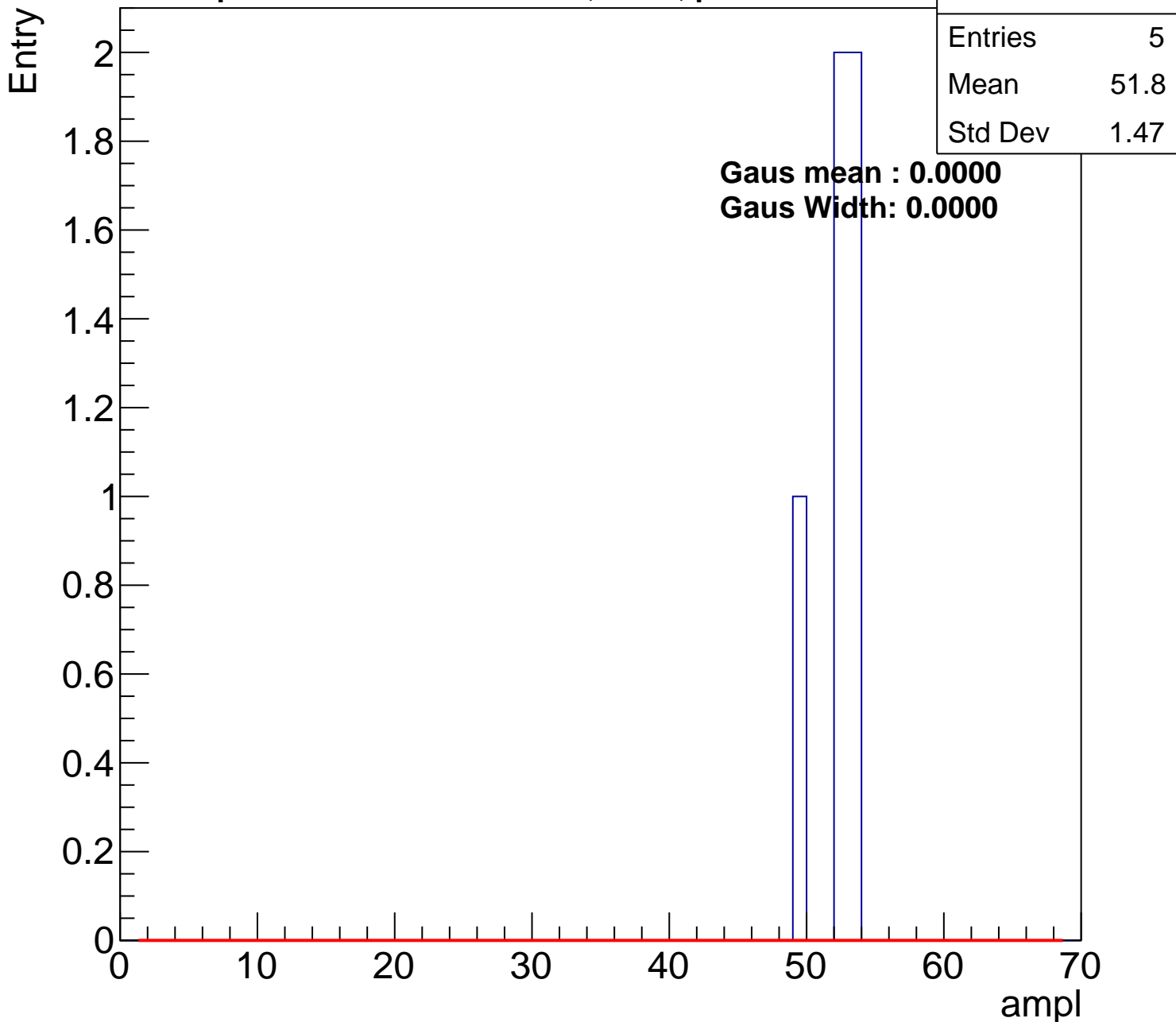
Entries	5
Mean	51.8
Std Dev	1.47

Gaus mean : 0.0000

Gaus Width: 0.0000

0 10 20 30 40 50 60 70

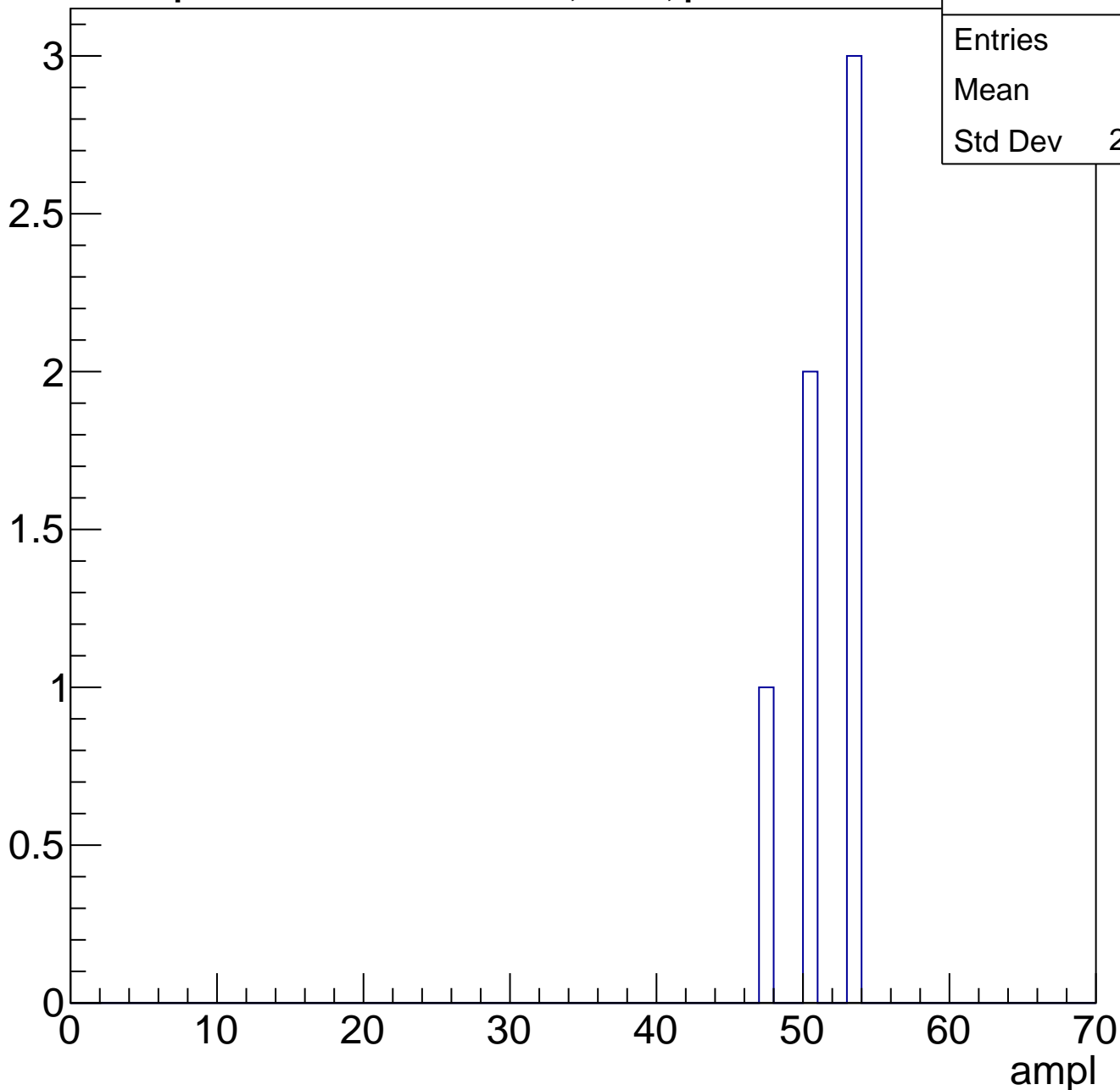
ampl



B0L100S, U12-ch86, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch86, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch86, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch86, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch86, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch87, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch87, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch87, adc2

calib_packv5_042523_0143.root, FC#6, port A1

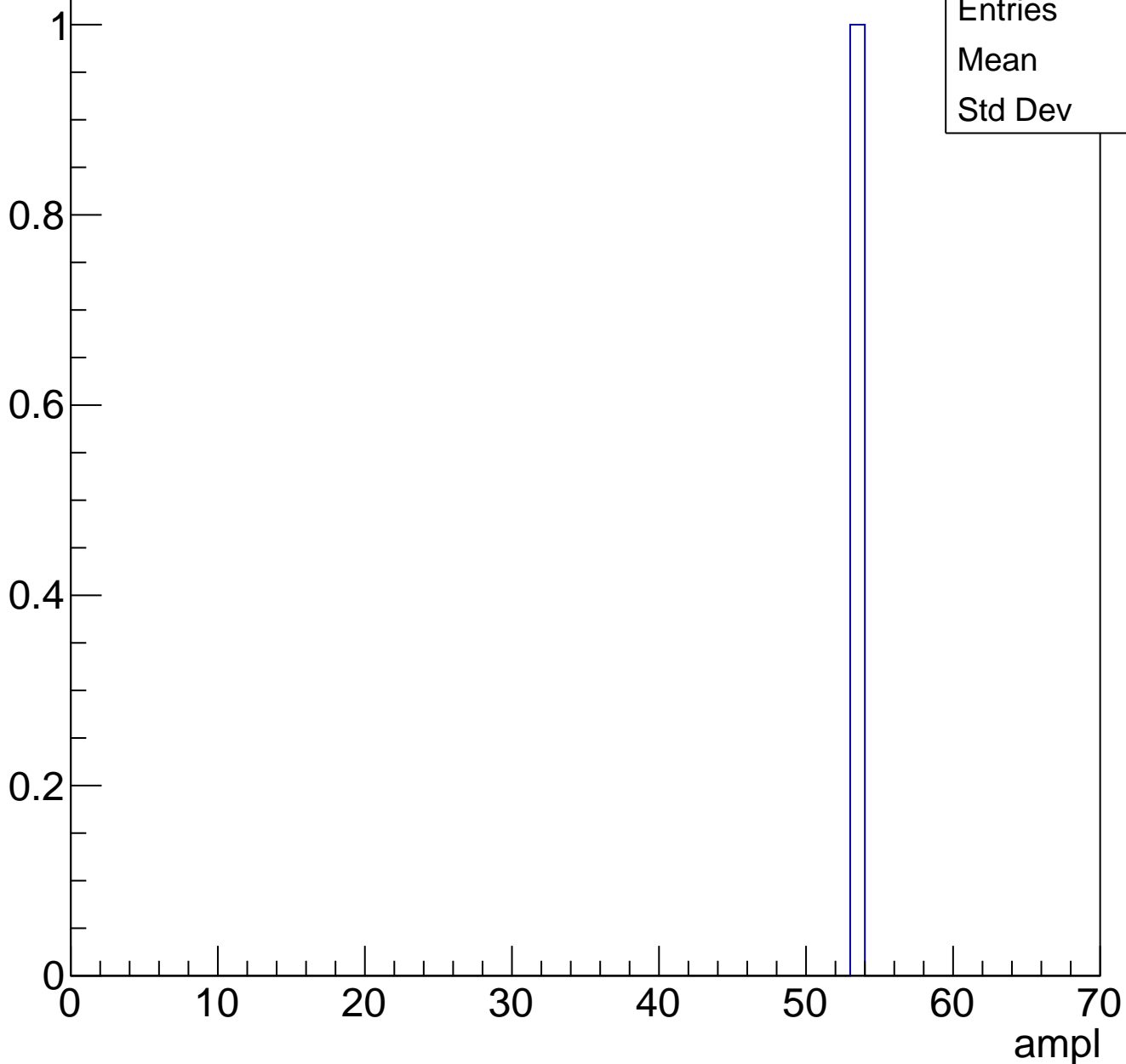
Entry



B0L100S, U12-ch87, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch87, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch87, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch87, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch87, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch88, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

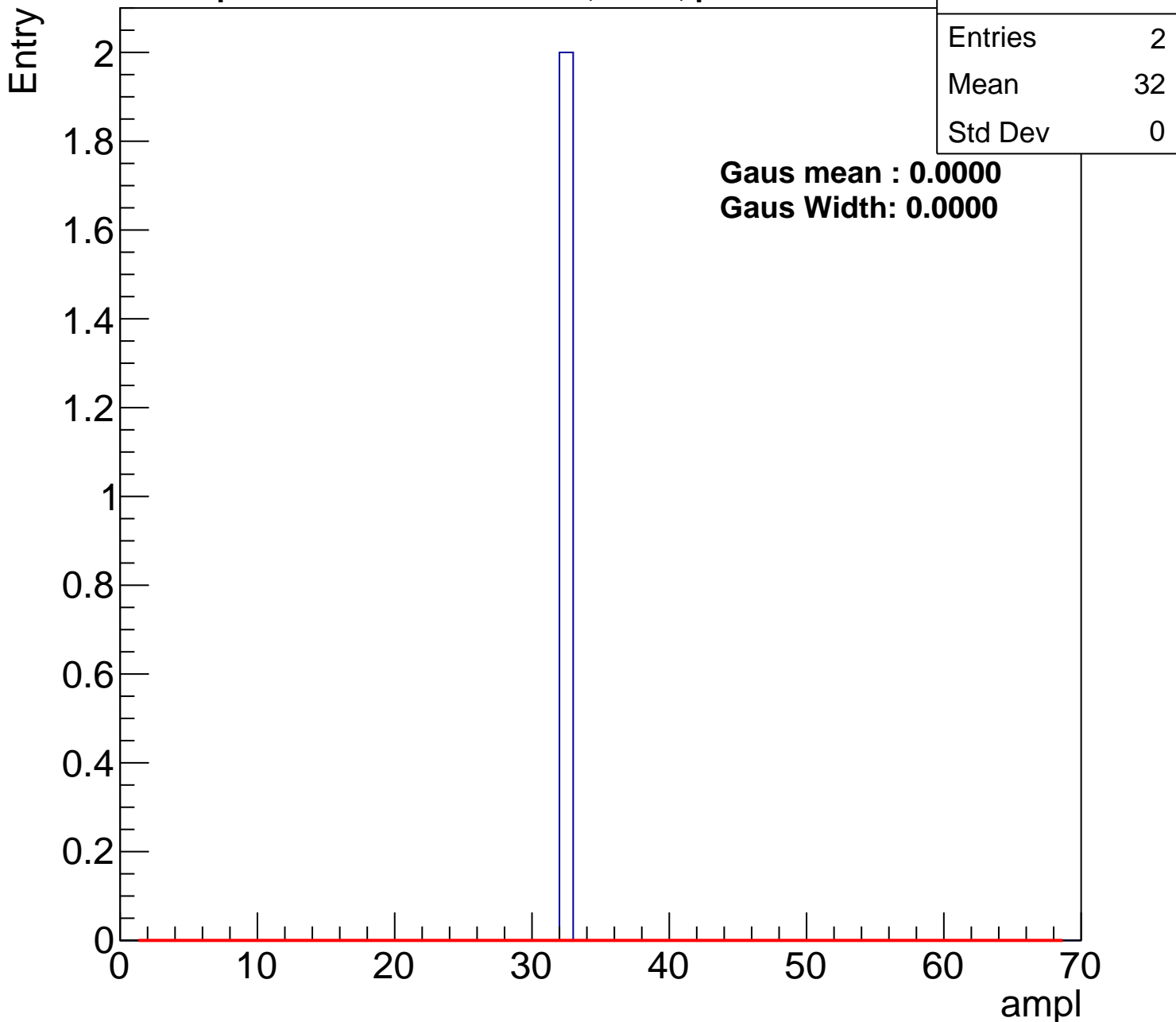
Entries	2
Mean	32
Std Dev	0

Gaus mean : 0.0000

Gaus Width: 0.0000

0 10 20 30 40 50 60 70

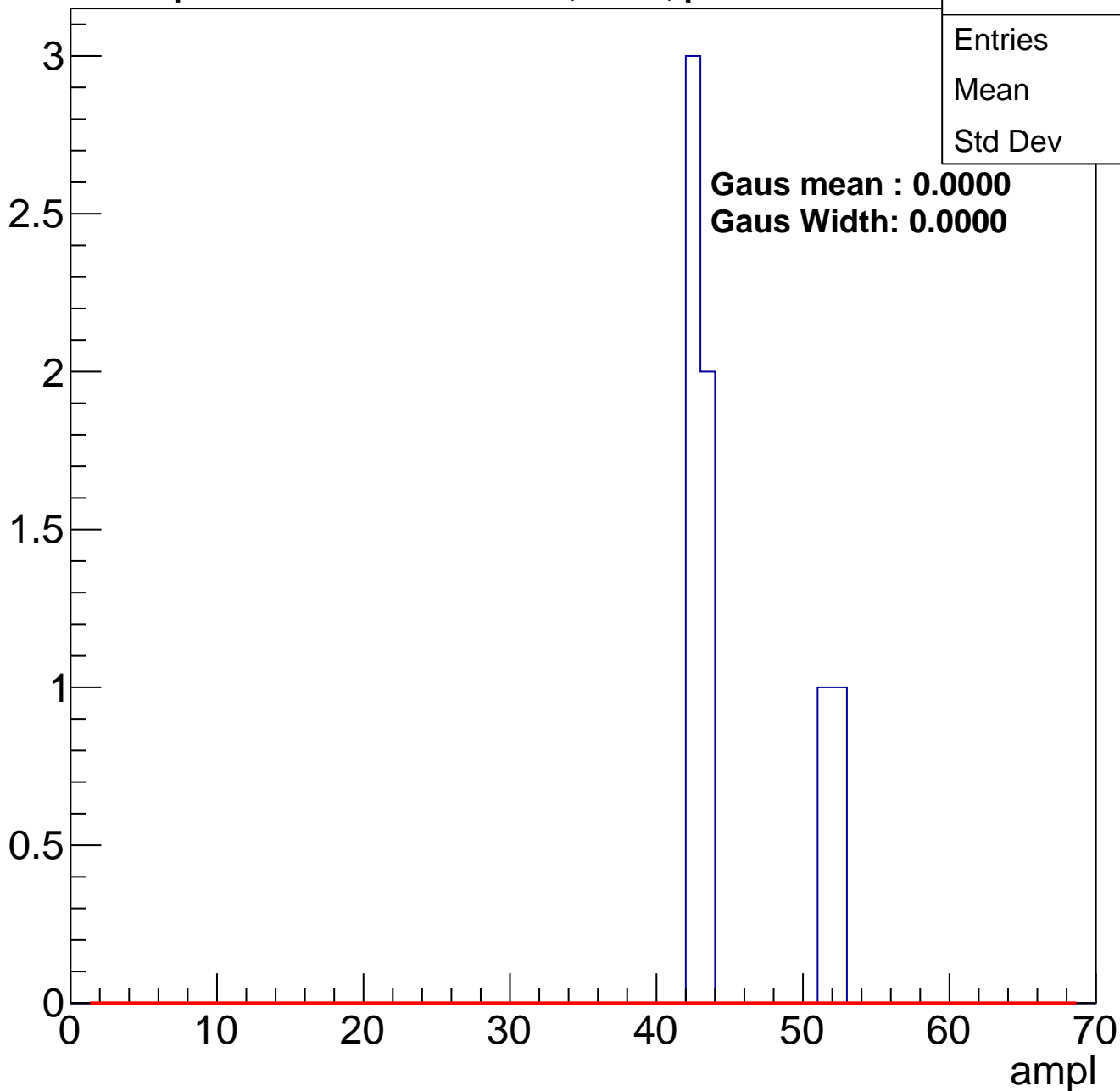
ampl



B0L100S, U12-ch88, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry

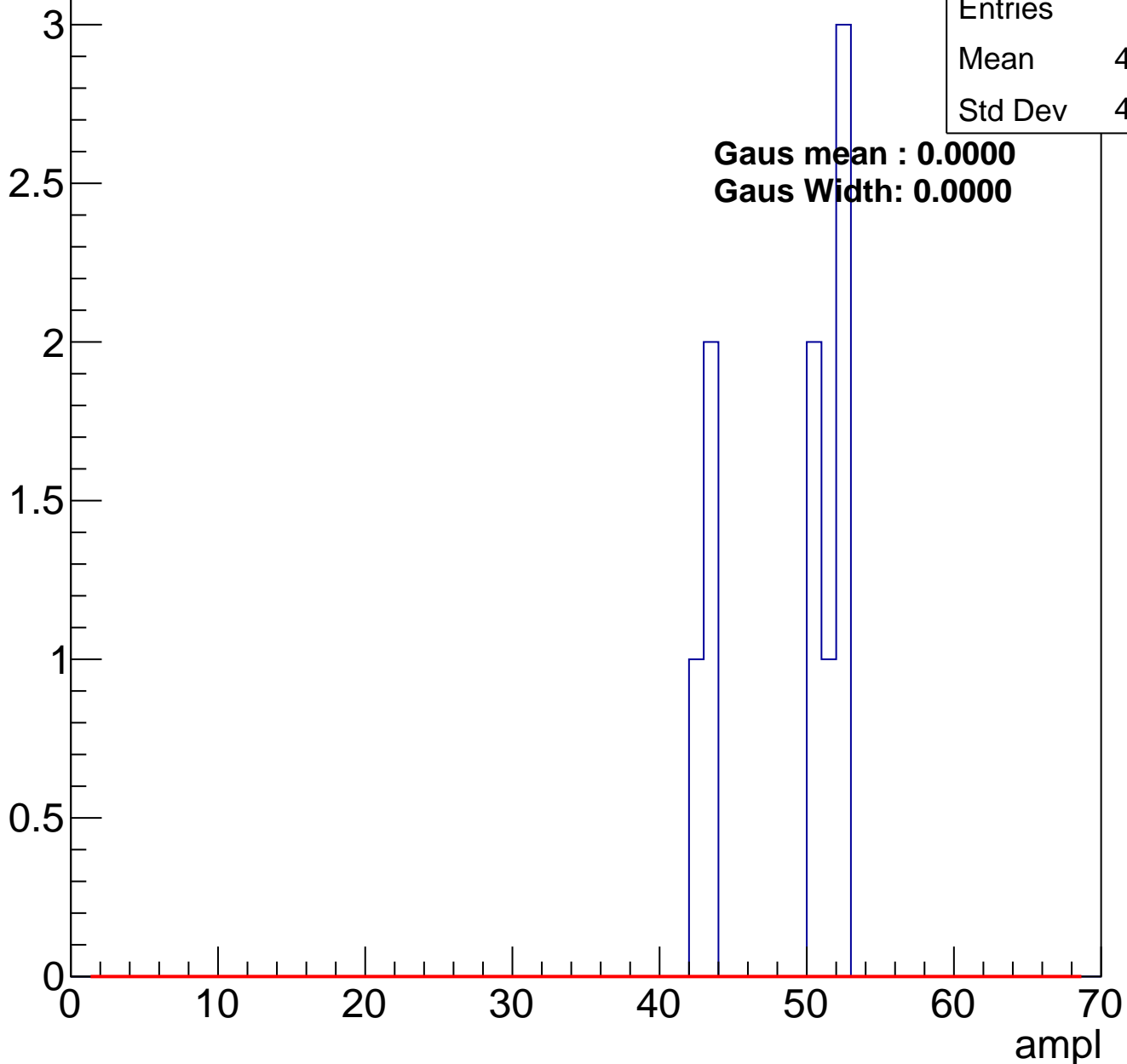


Entries	7
Mean	45
Std Dev	4.14

B0L100S, U12-ch88, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

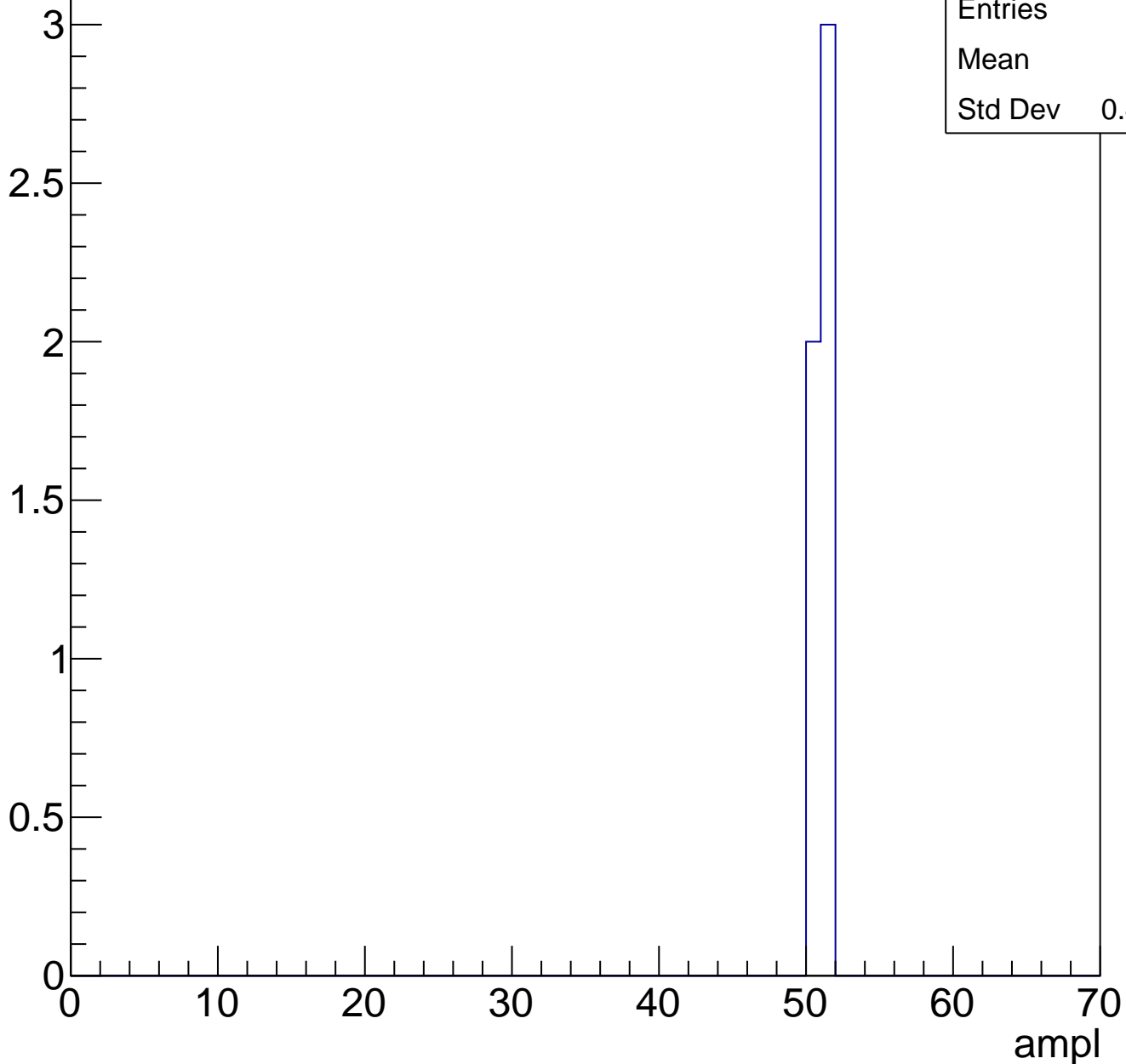


Entries	9
Mean	48.33
Std Dev	4.082

B0L100S, U12-ch88, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch88, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	2
Mean	31
Std Dev	0

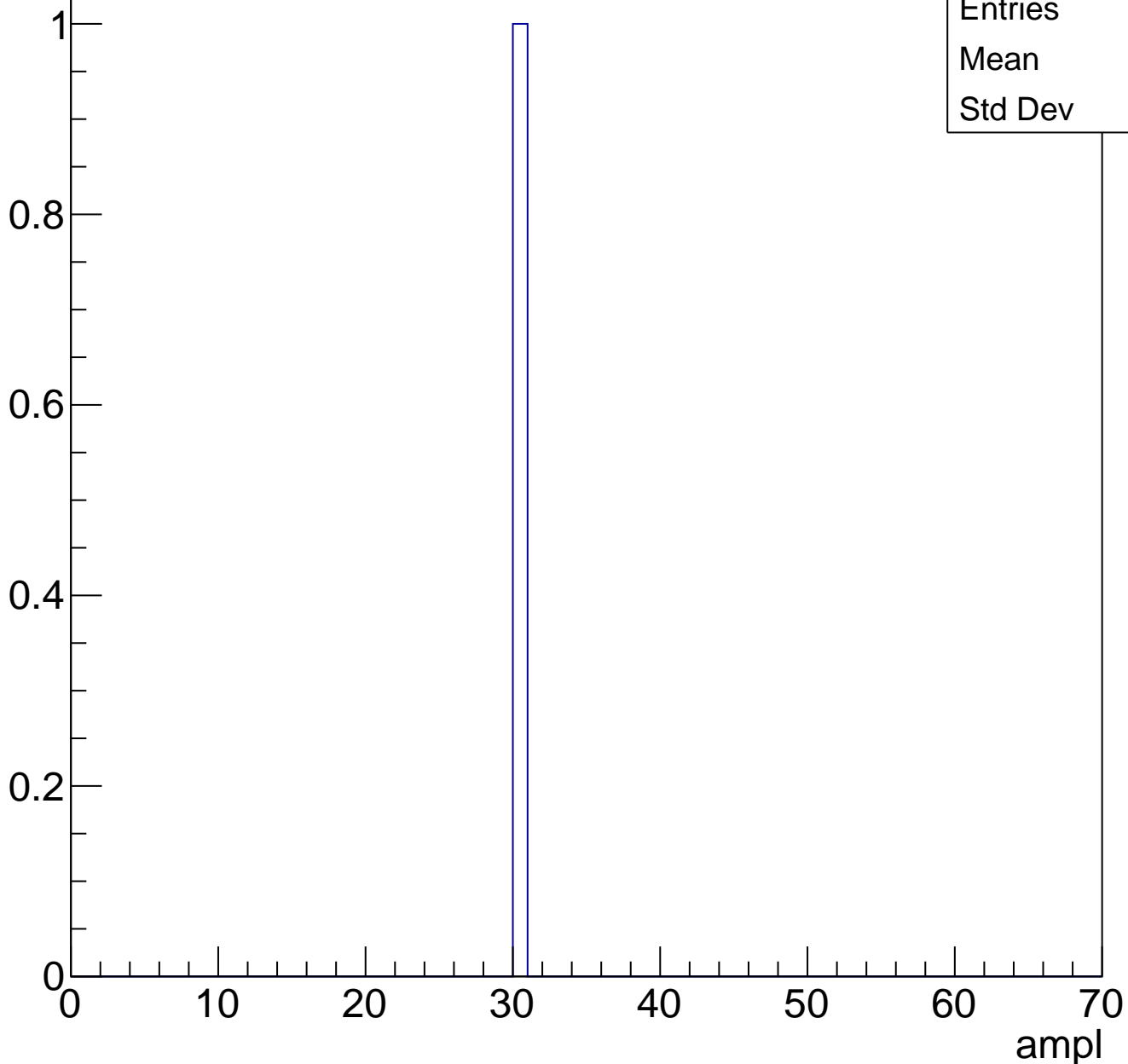
ampl

0 10 20 30 40 50 60 70

B0L100S, U12-ch88, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	1
Mean	30
Std Dev	0

B0L100S, U12-ch88, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch88, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch89, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry

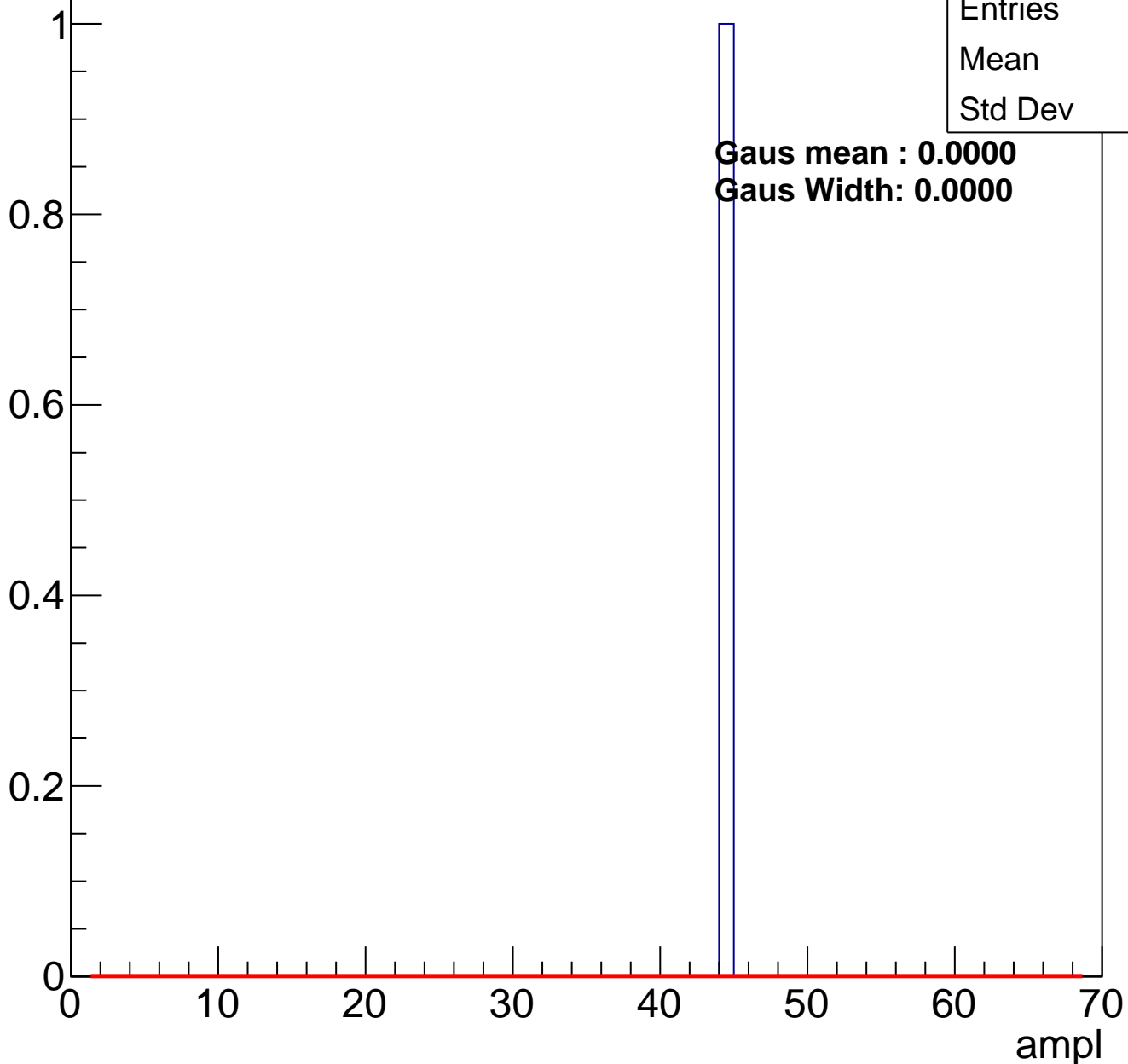


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch89, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	1
Mean	44
Std Dev	0

Gaus mean : 0.0000

Gaus Width: 0.0000

B0L100S, U12-ch89, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch89, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch89, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry

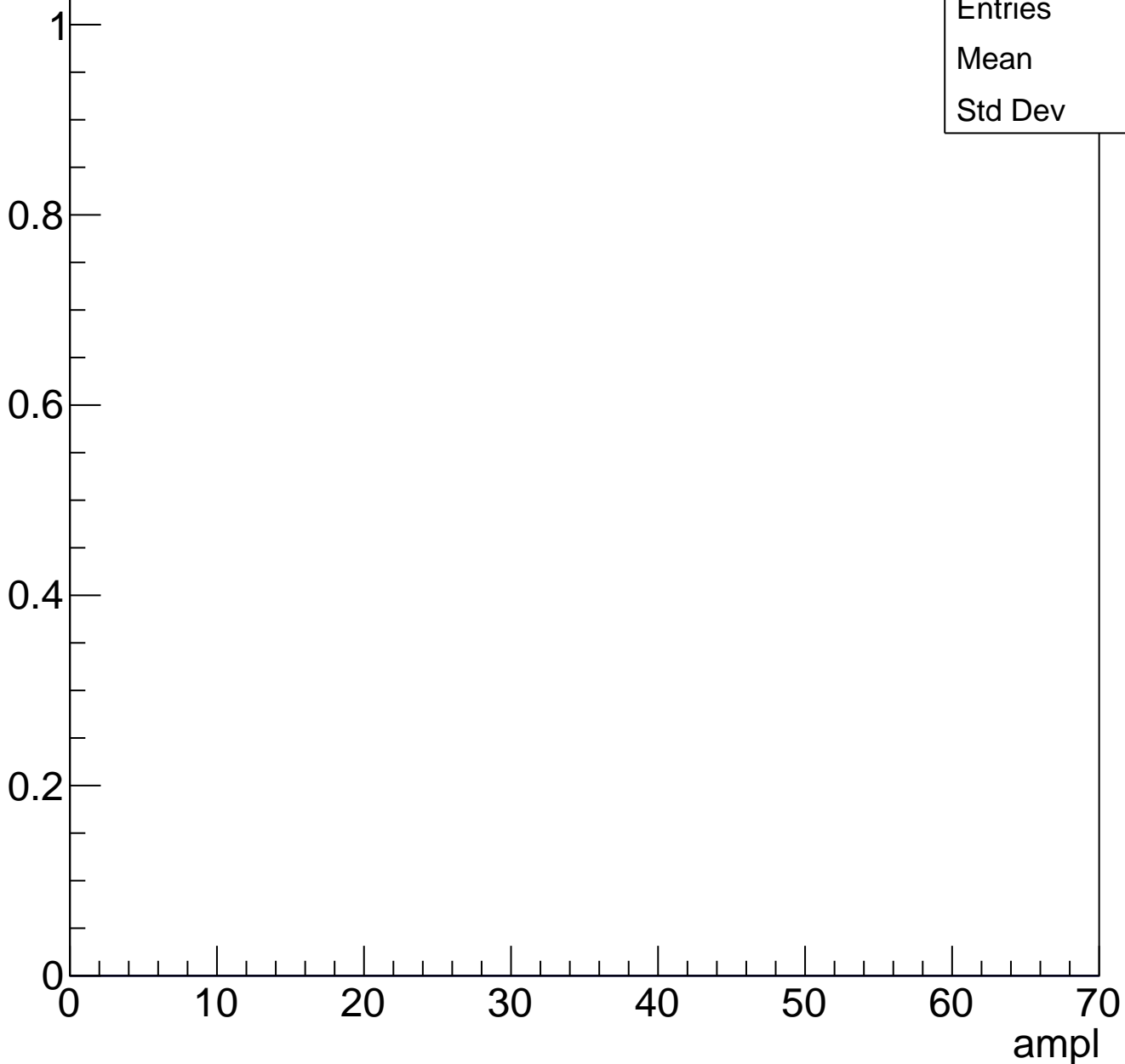


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch89, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch89, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch89, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry

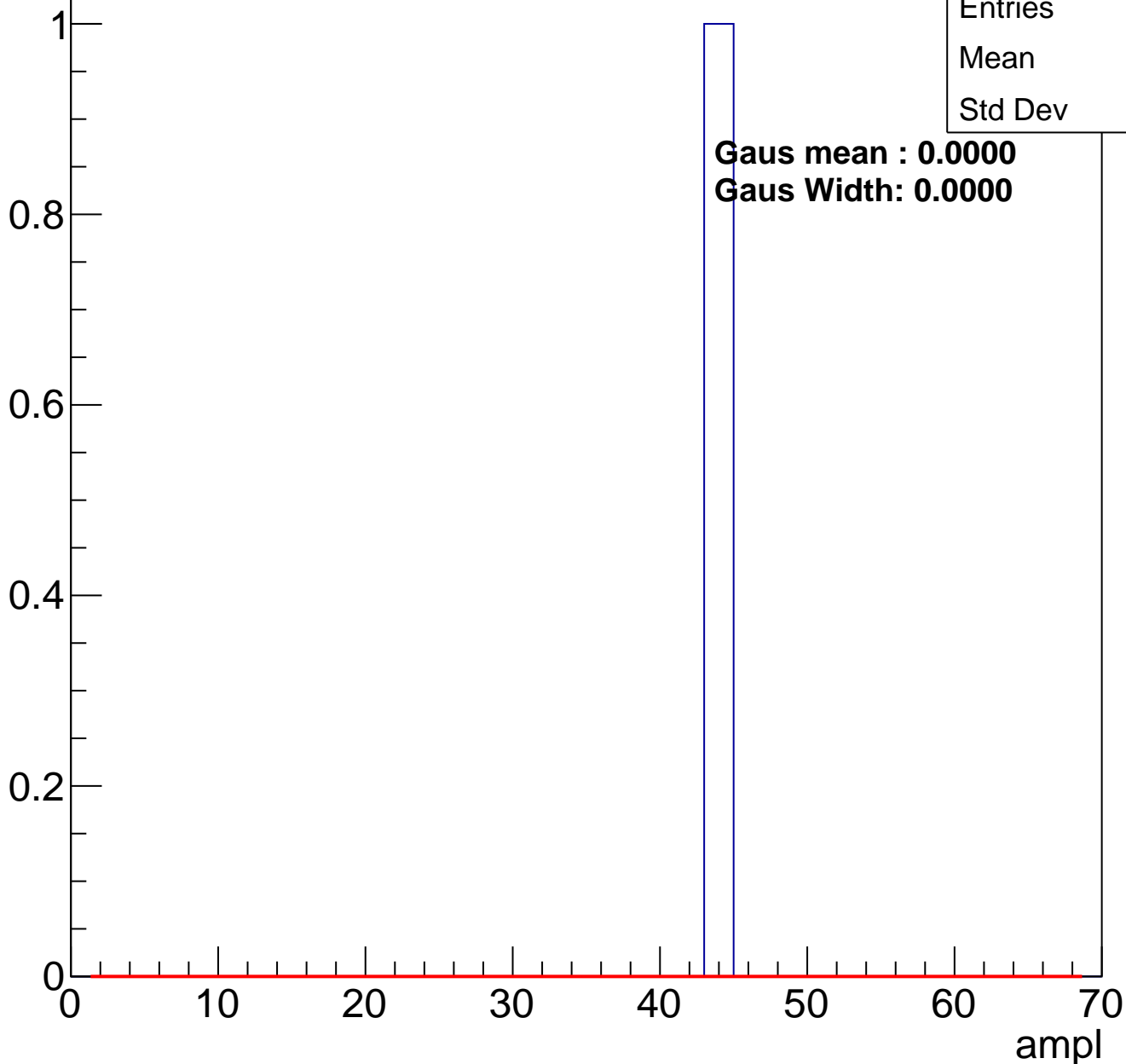


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch90, adc0

calib_packv5_042523_0143.root, FC#6, port A1

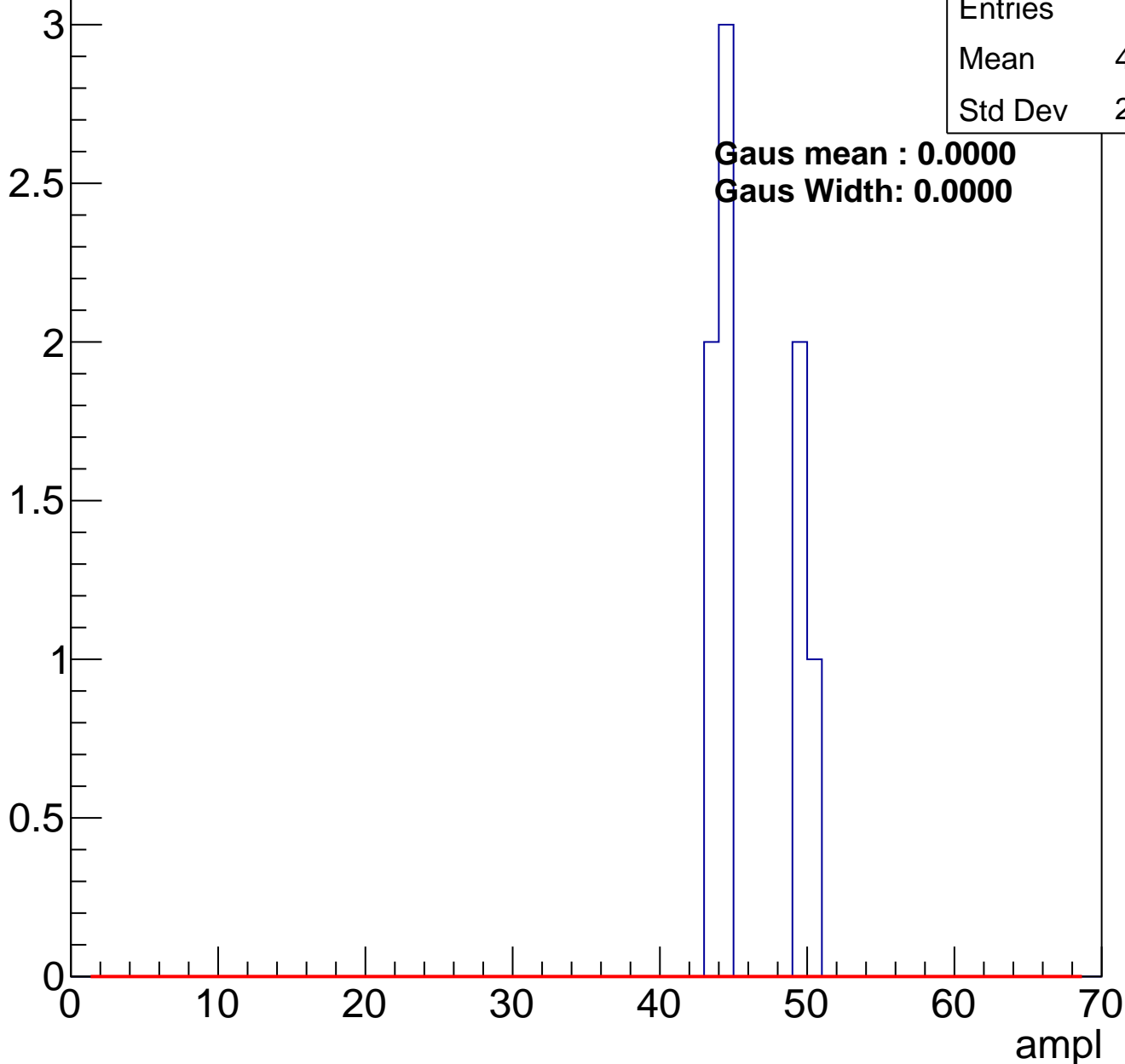
Entry



B0L100S, U12-ch90, adc1

calib_packv5_042523_0143.root, FC#6, port A1

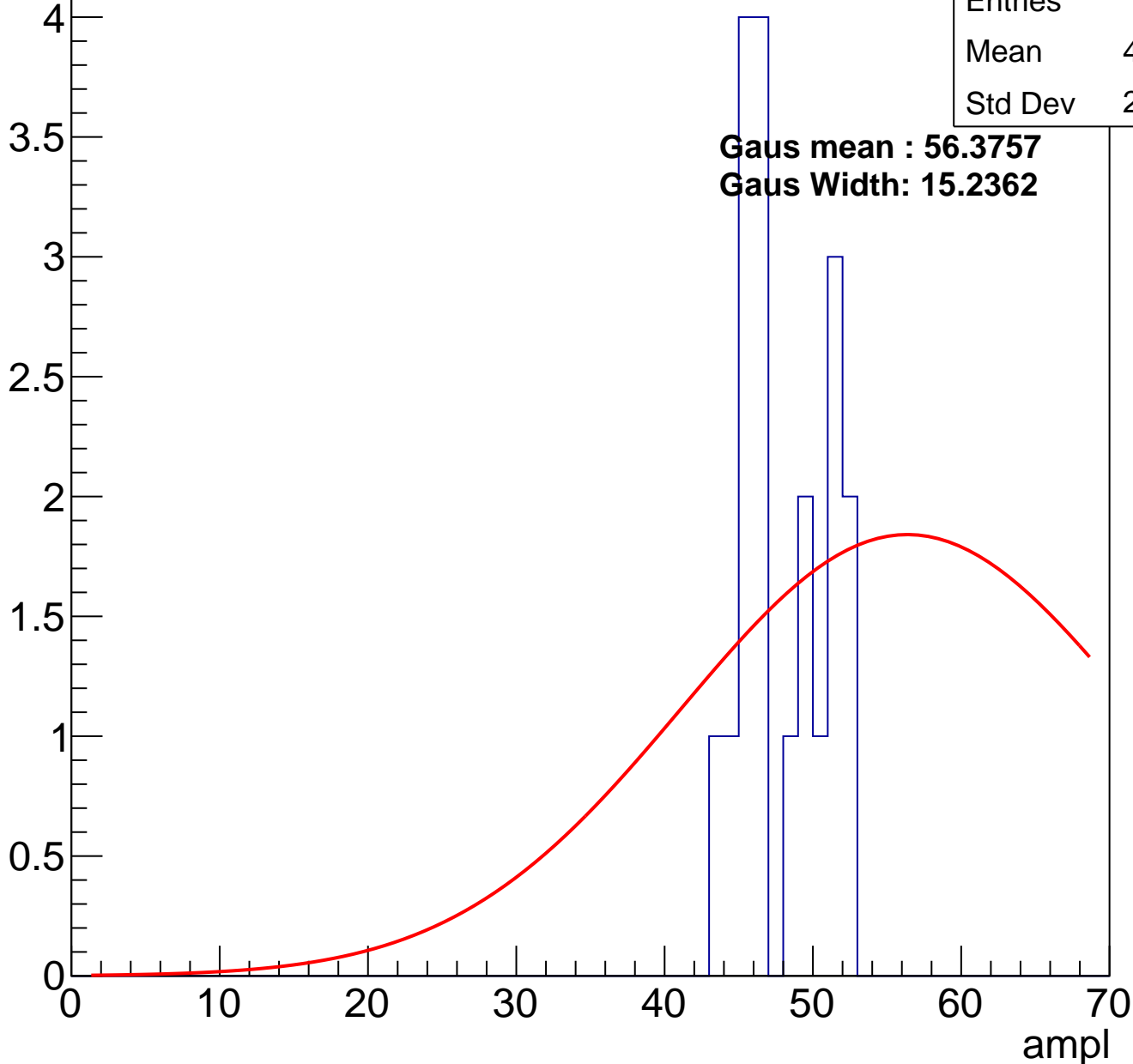
Entry



B0L100S, U12-ch90, adc2

calib_packv5_042523_0143.root, FC#6, port A1

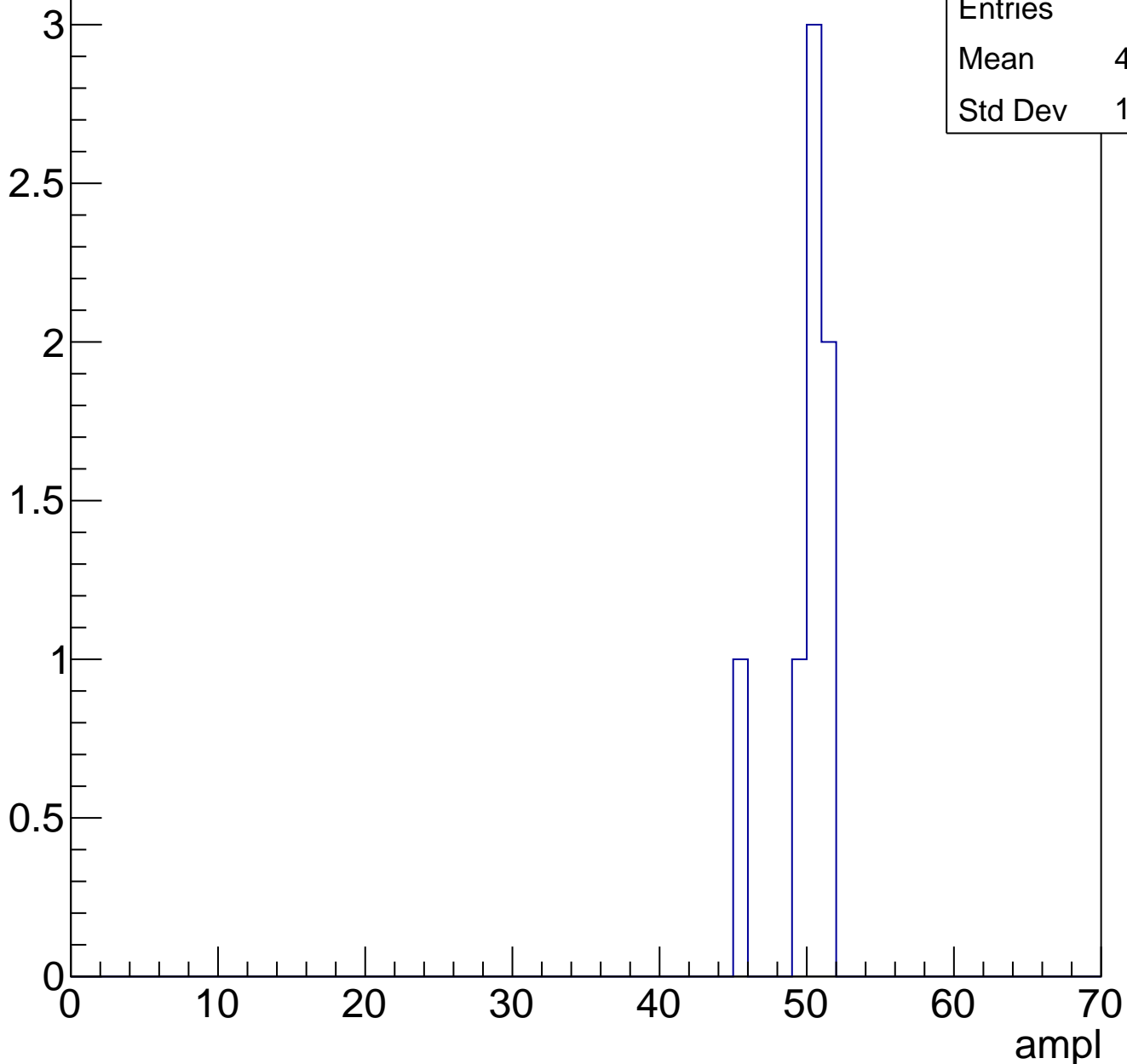
Entry



B0L100S, U12-ch90, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch90, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch90, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch90, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch90, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry

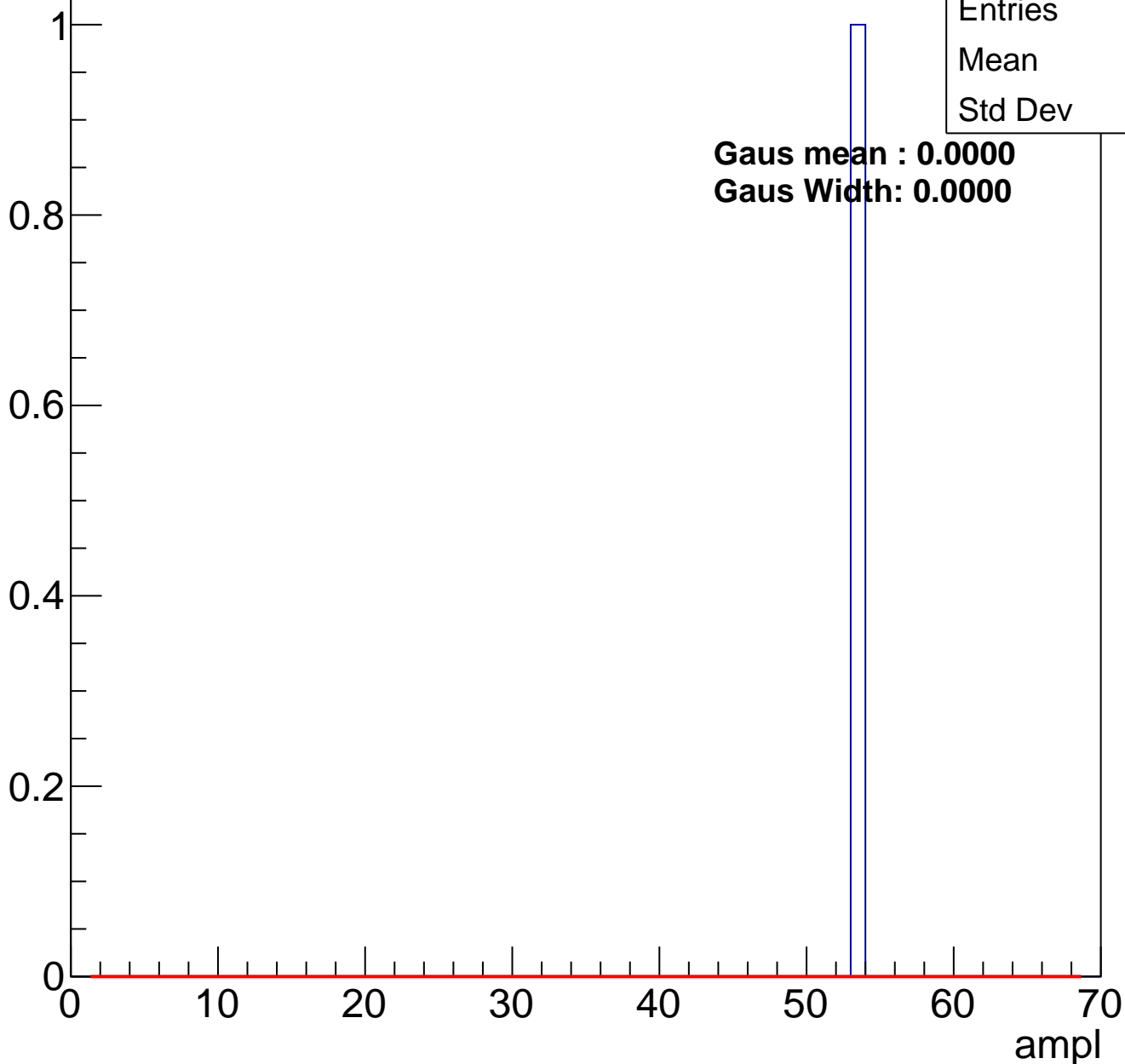


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch91, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch91, adc1

calib_packv5_042523_0143.root, FC#6, port A1

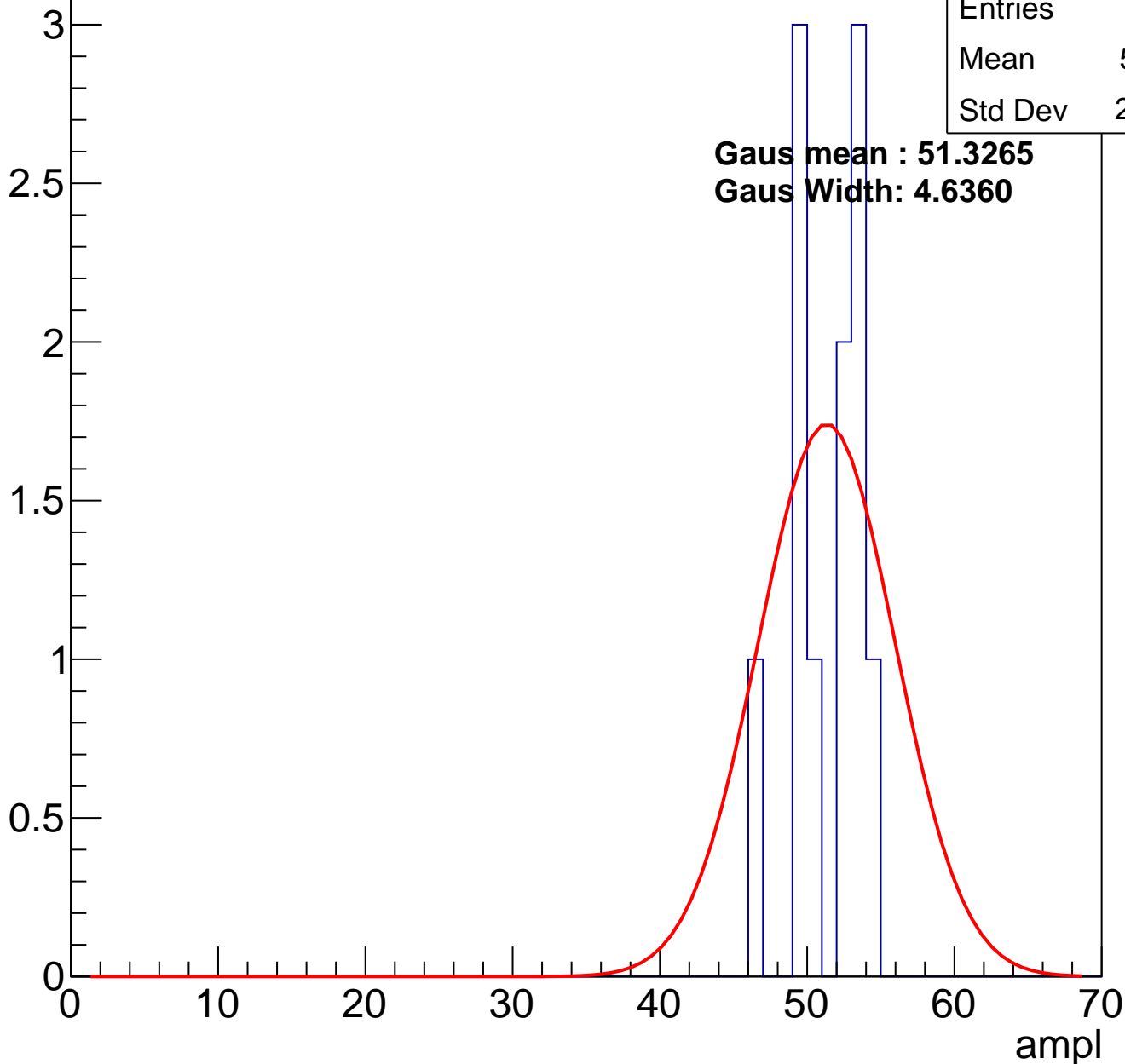
Entry



B0L100S, U12-ch91, adc2

calib_packv5_042523_0143.root, FC#6, port A1

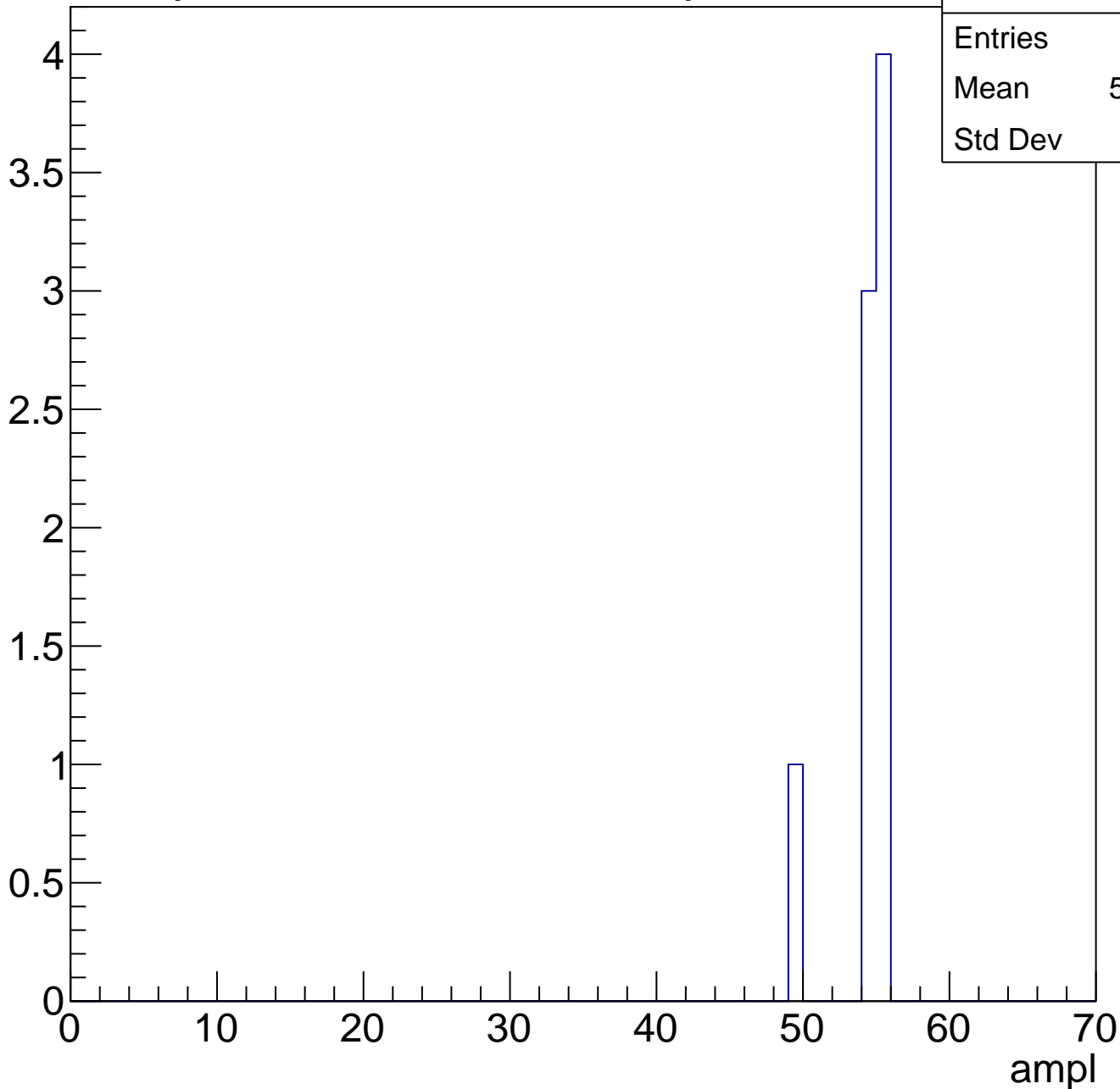
Entry



B0L100S, U12-ch91, adc3

calib_packv5_042523_0143.root, FC#6, port A1

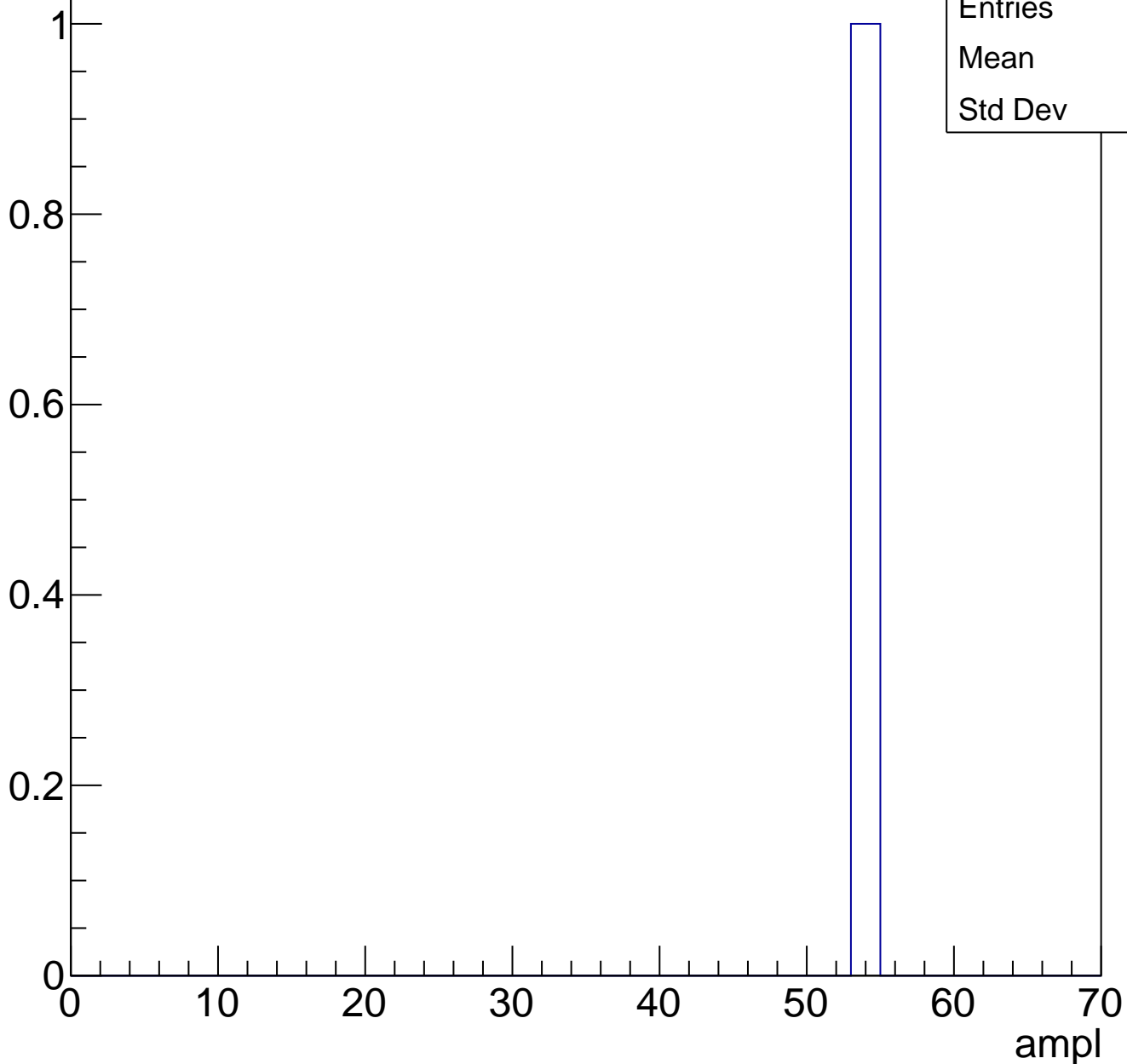
Entry



B0L100S, U12-ch91, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch91, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch91, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch91, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch92, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry

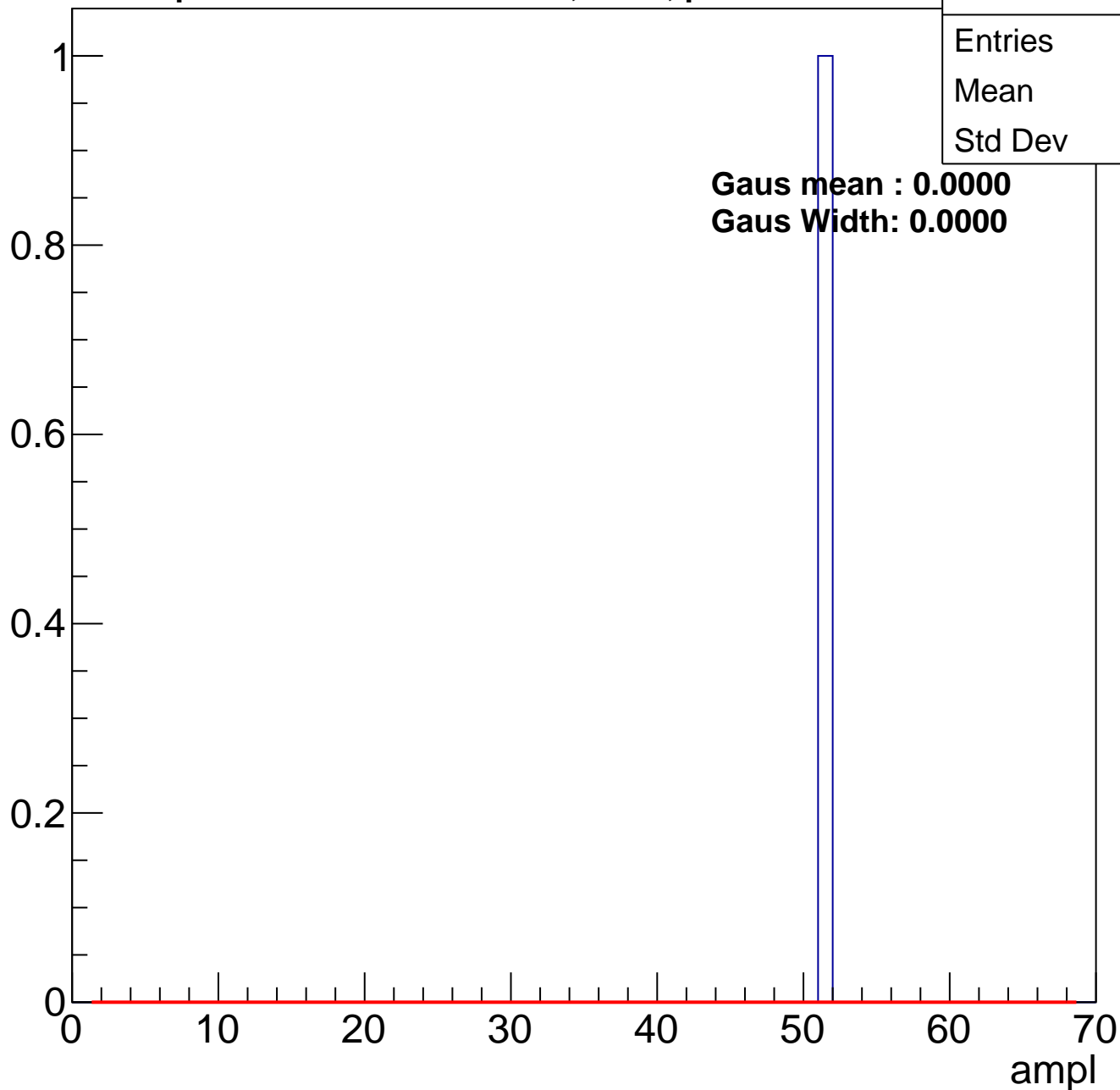


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch92, adc1

calib_packv5_042523_0143.root, FC#6, port A1

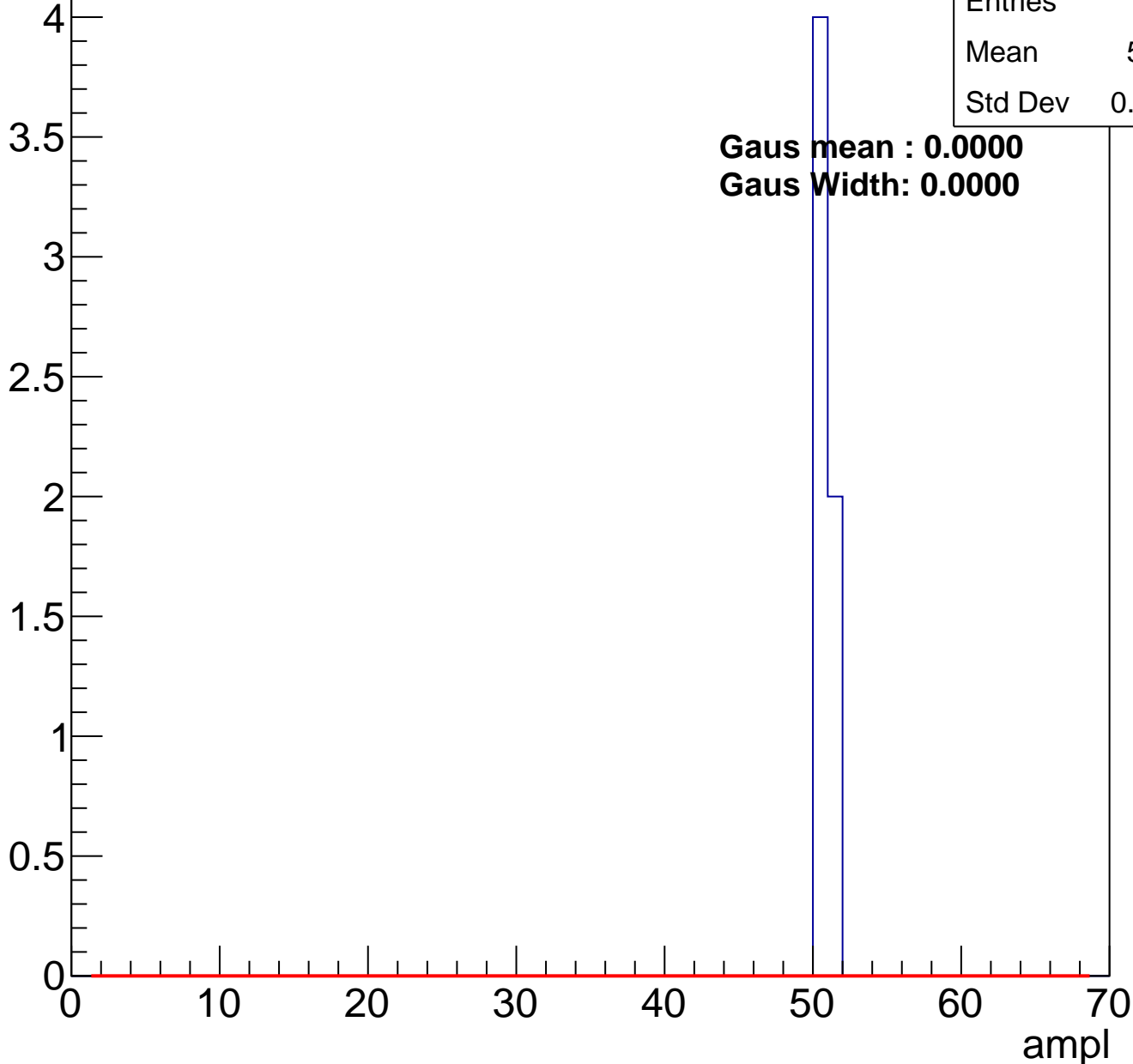
Entry



B0L100S, U12-ch92, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	6
Mean	50.33
Std Dev	0.4714

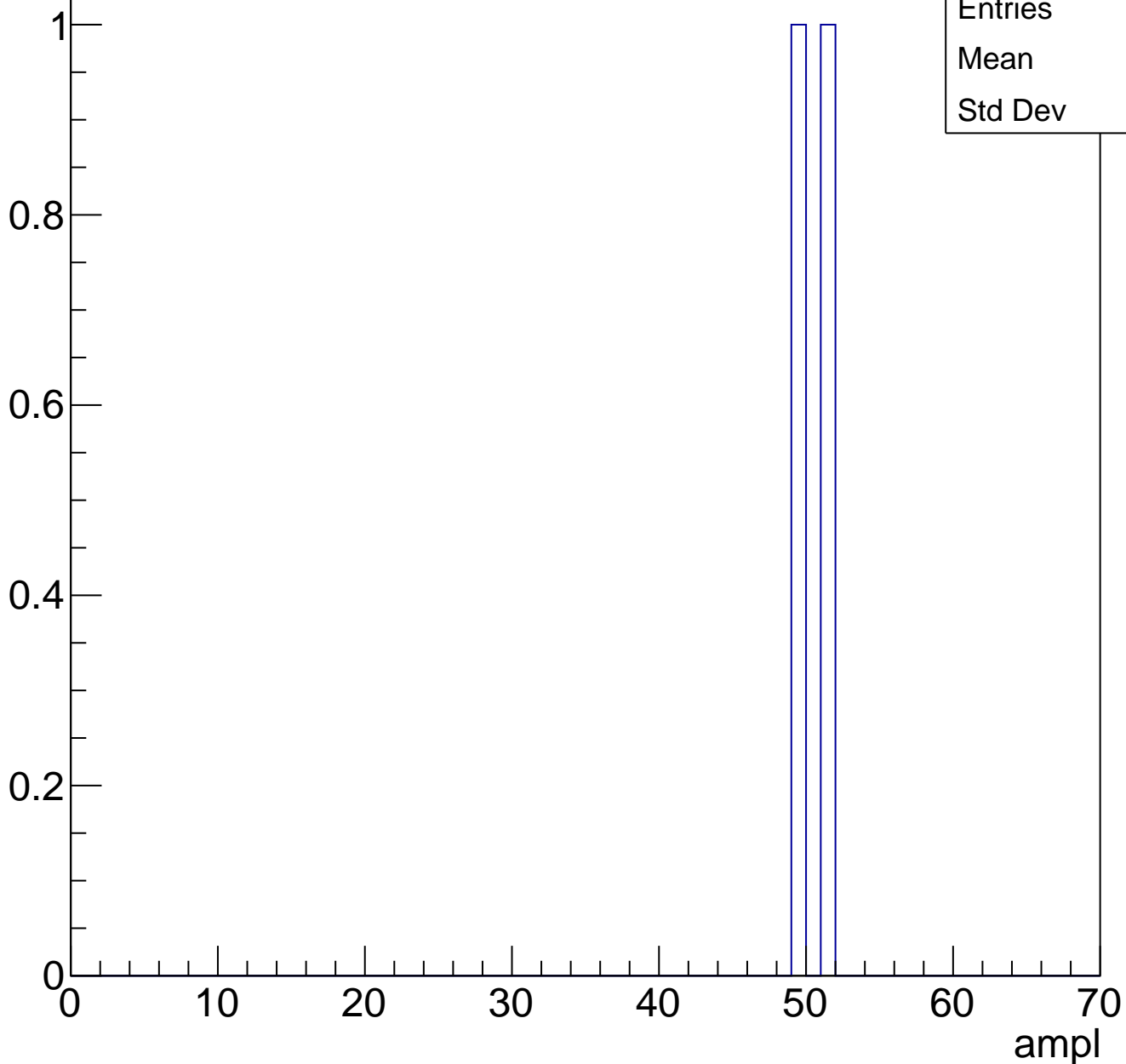
Gaus mean : 0.0000

Gaus Width: 0.0000

B0L100S, U12-ch92, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch92, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch92, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch92, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch92, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch93, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch93, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	2
Mean	50
Std Dev	0

Gaus mean : 0.0000

Gaus Width: 0.0000

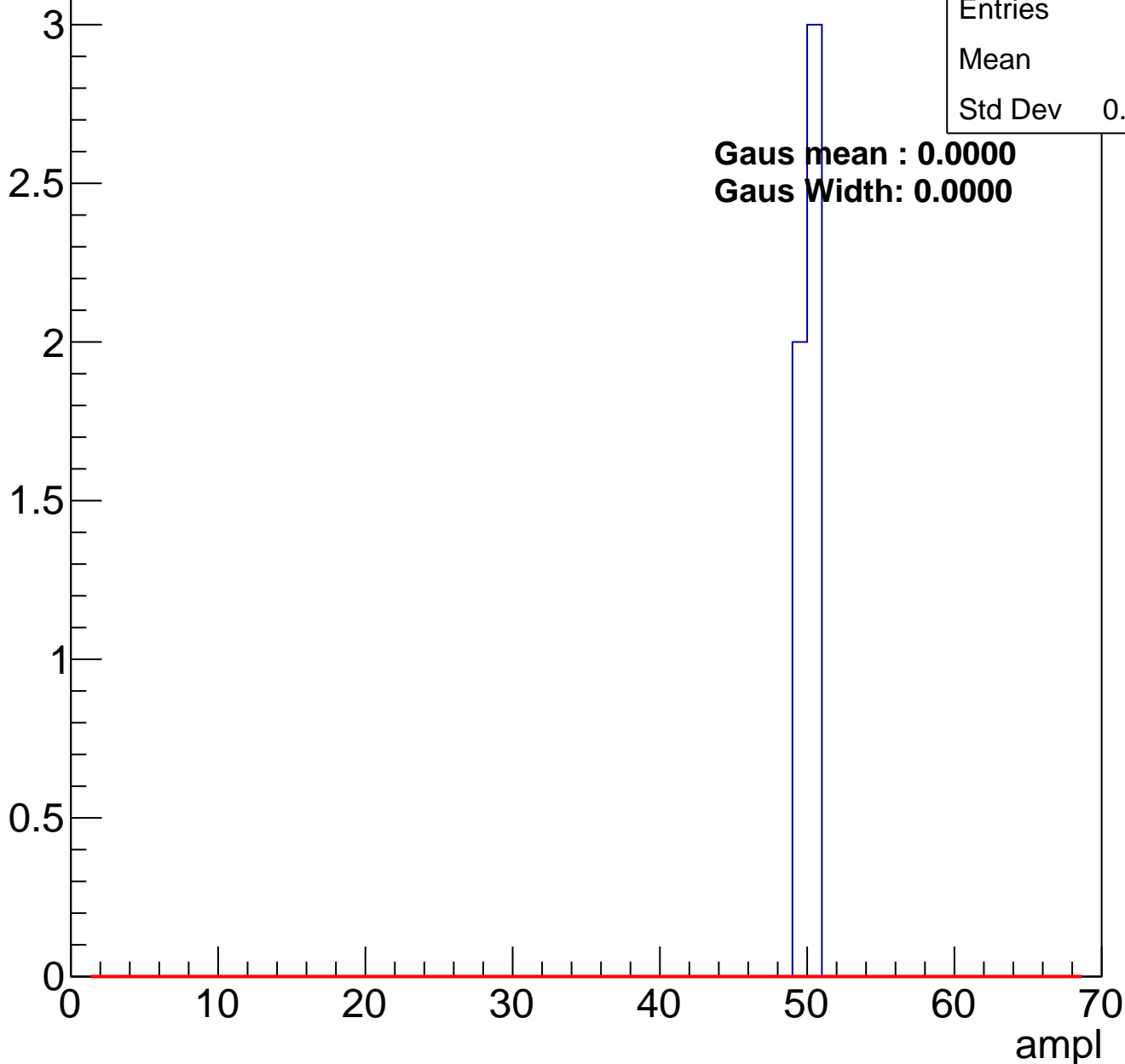
ampl

0 10 20 30 40 50 60 70

B0L100S, U12-ch93, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

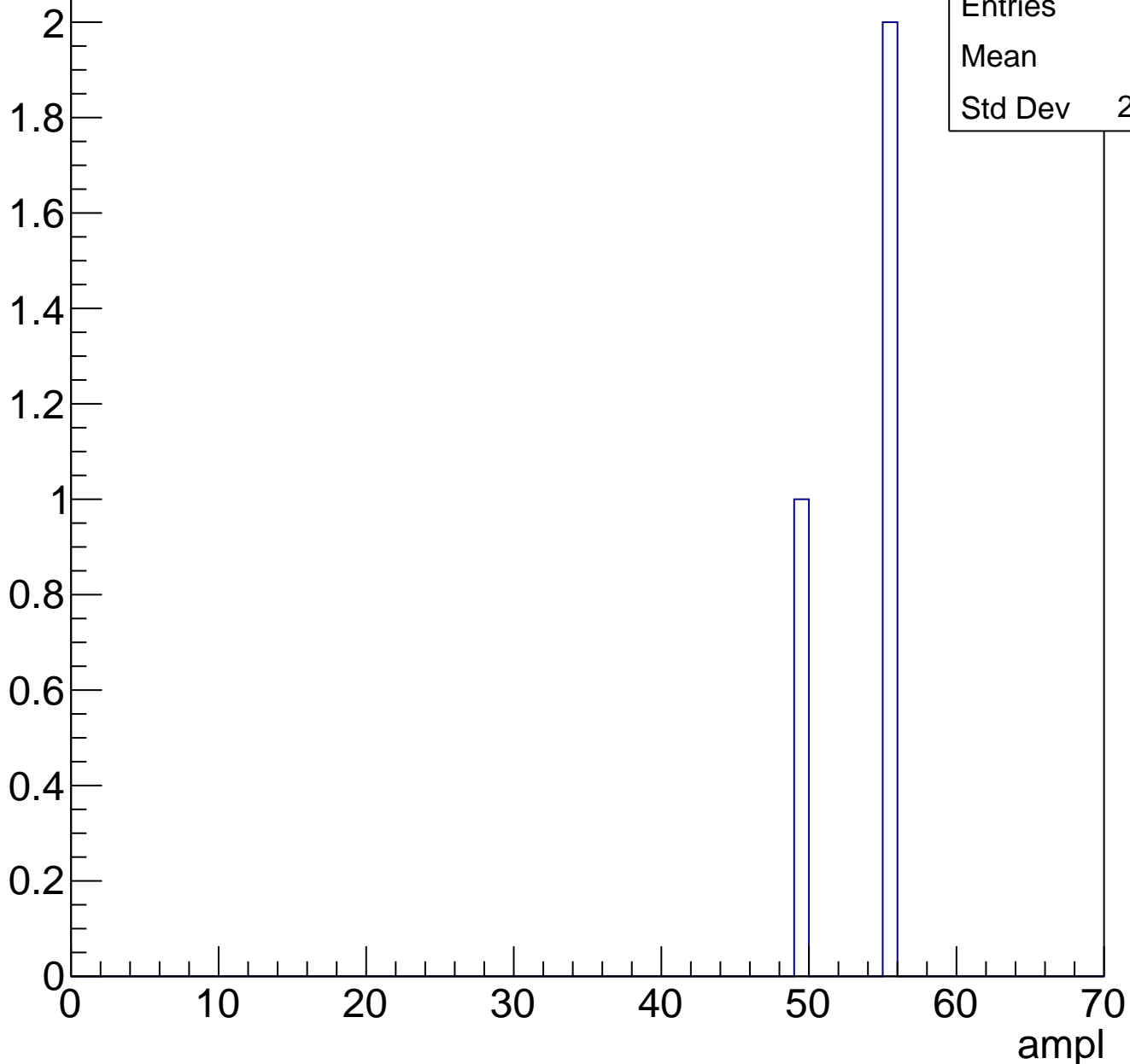


Entries	5
Mean	49.6
Std Dev	0.4899

B0L100S, U12-ch93, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	3
Mean	53
Std Dev	2.828

B0L100S, U12-ch93, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch93, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch93, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch93, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry

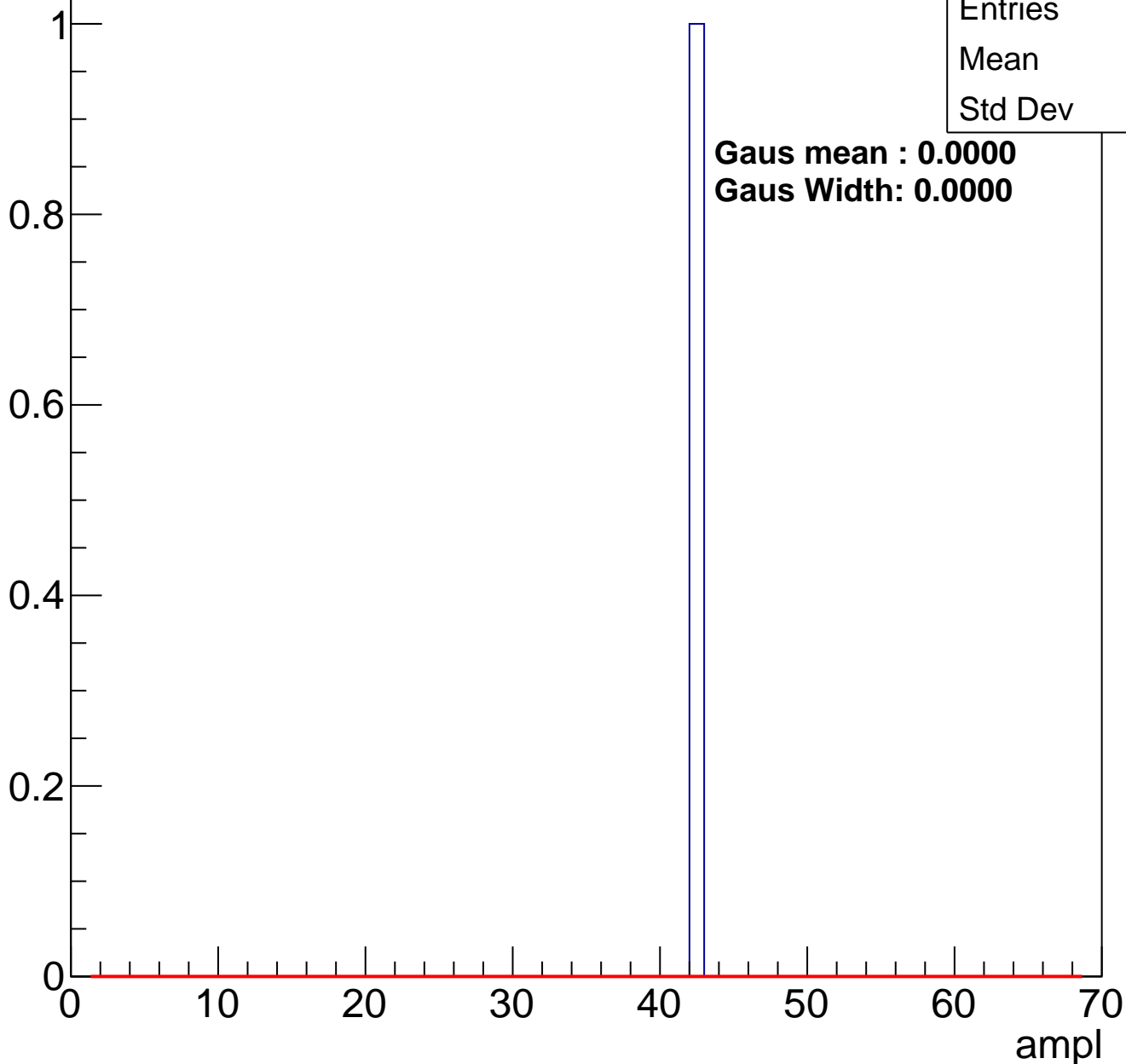


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch94, adc0

calib_packv5_042523_0143.root, FC#6, port A1

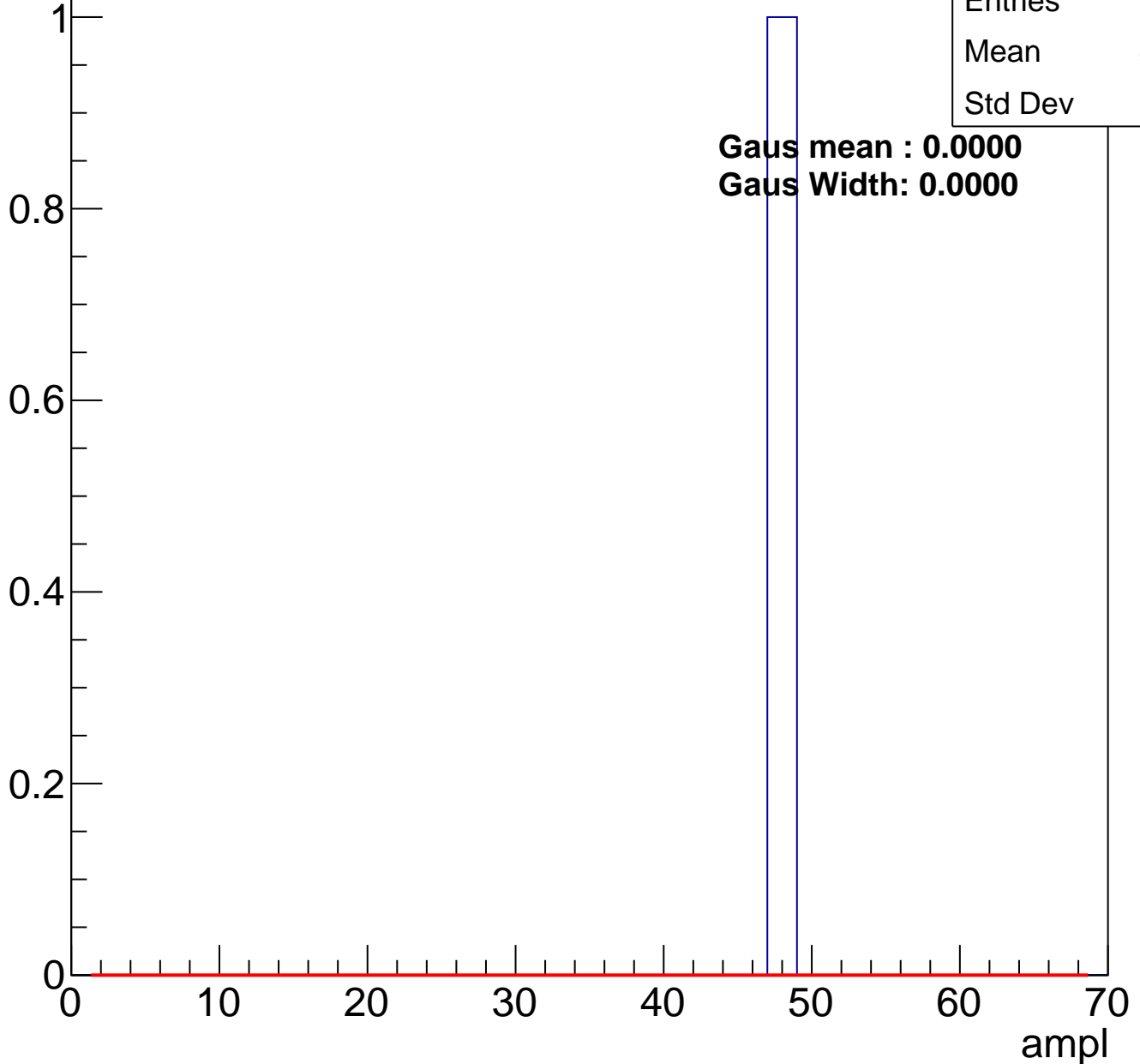
Entry



B0L100S, U12-ch94, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry

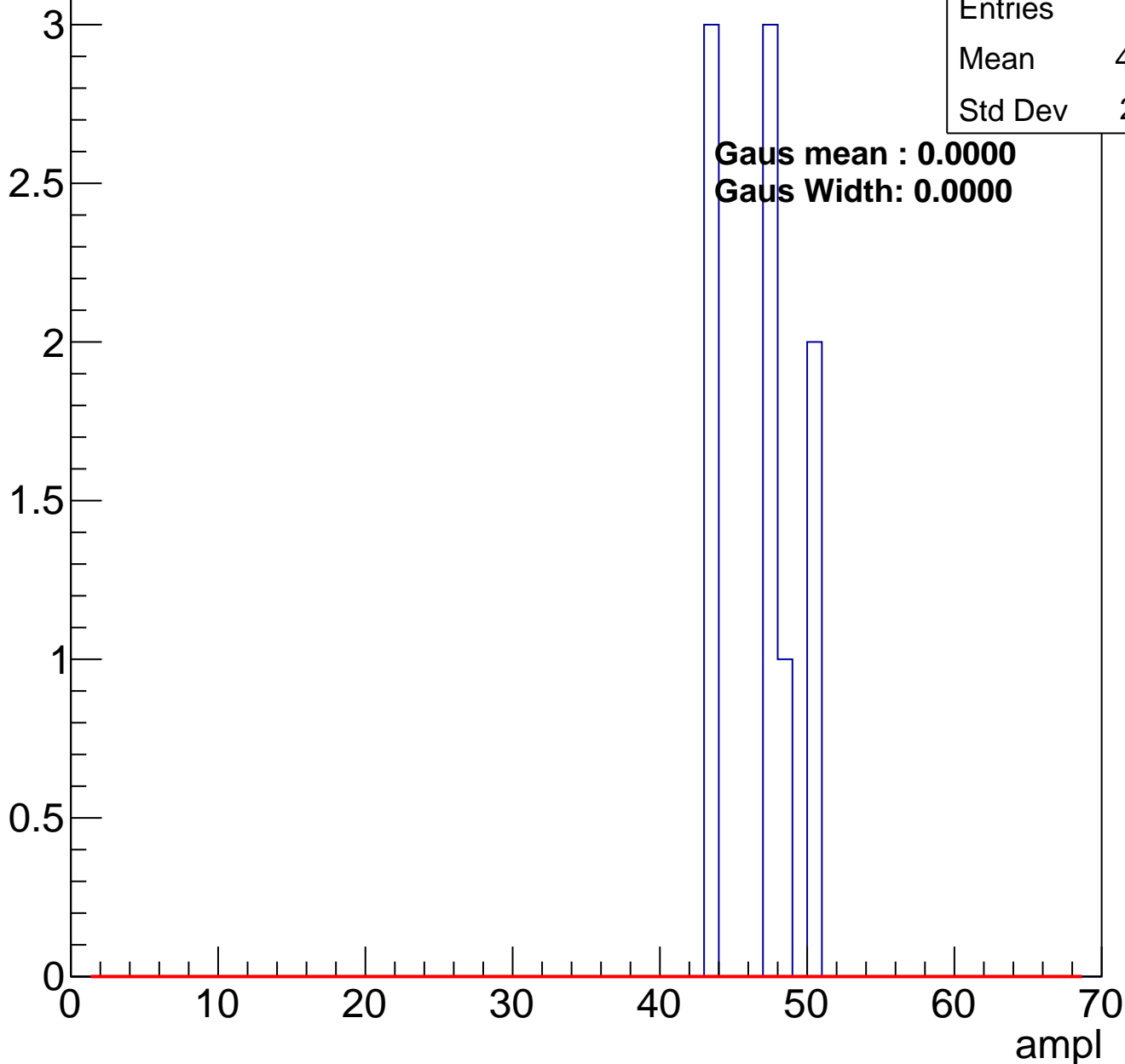


Entries	2
Mean	47.5
Std Dev	0.5

B0L100S, U12-ch94, adc2

calib_packv5_042523_0143.root, FC#6, port A1

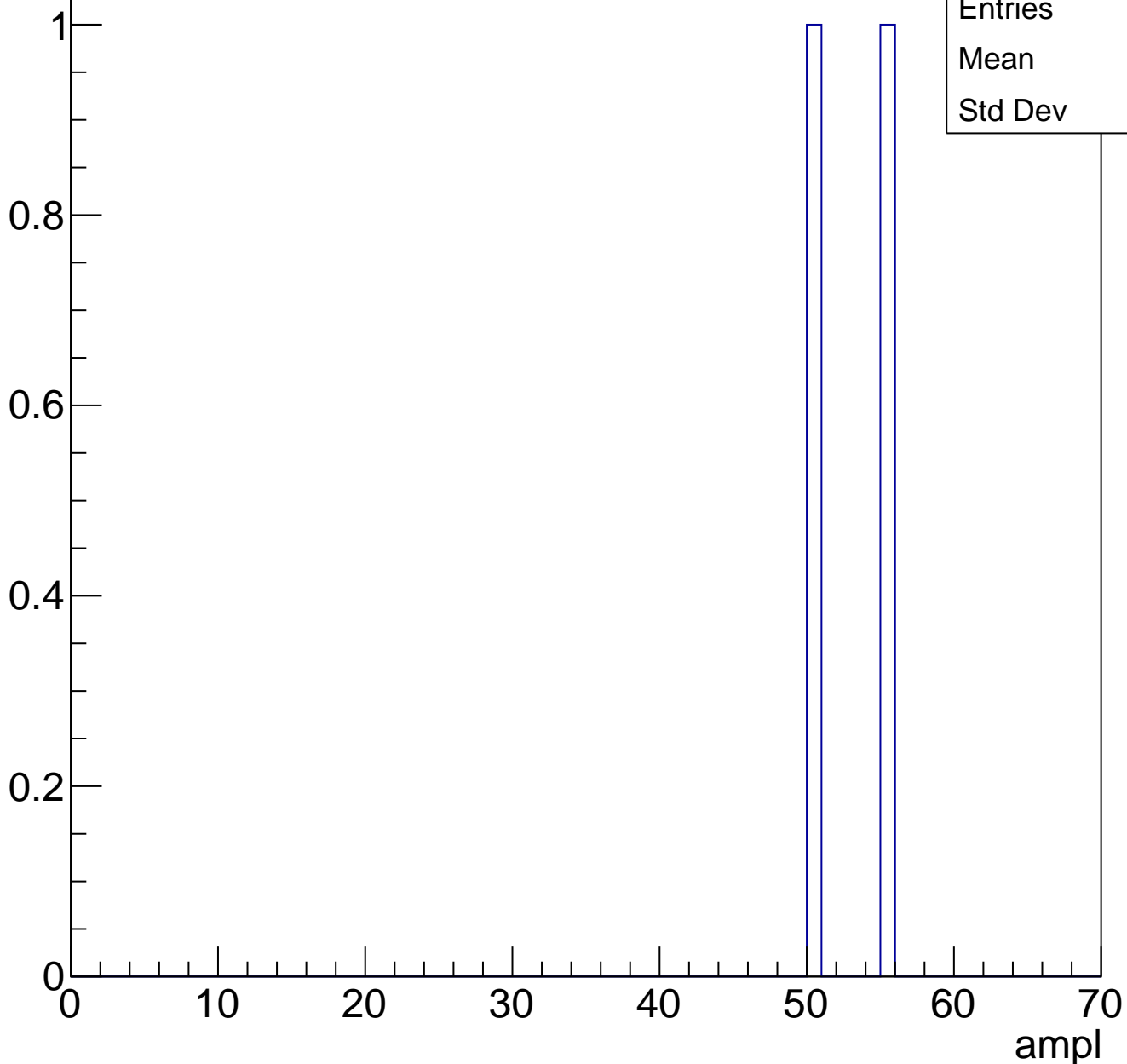
Entry



B0L100S, U12-ch94, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch94, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch94, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch94, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch94, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch95, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry

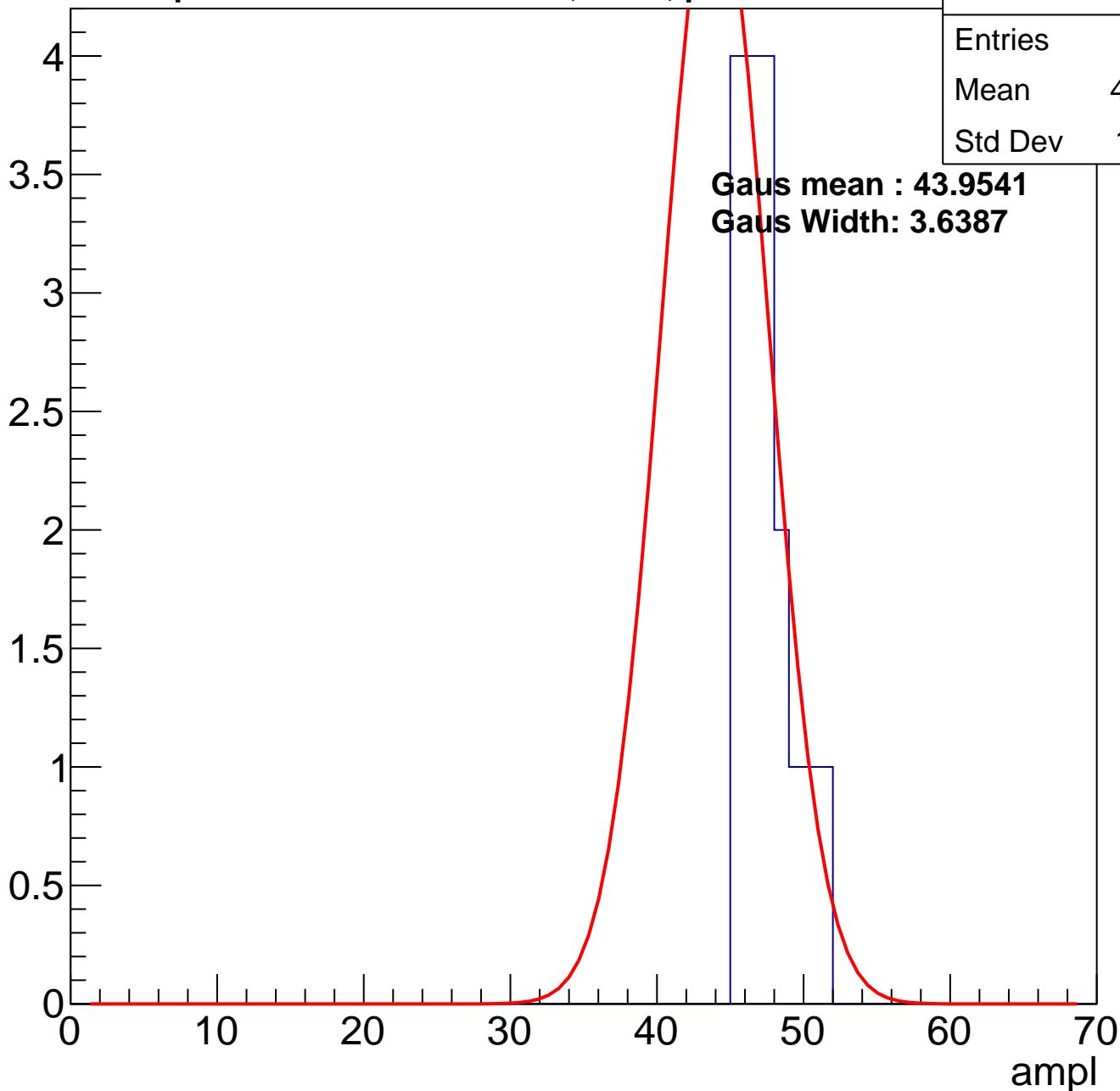


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch95, adc1

calib_packv5_042523_0143.root, FC#6, port A1

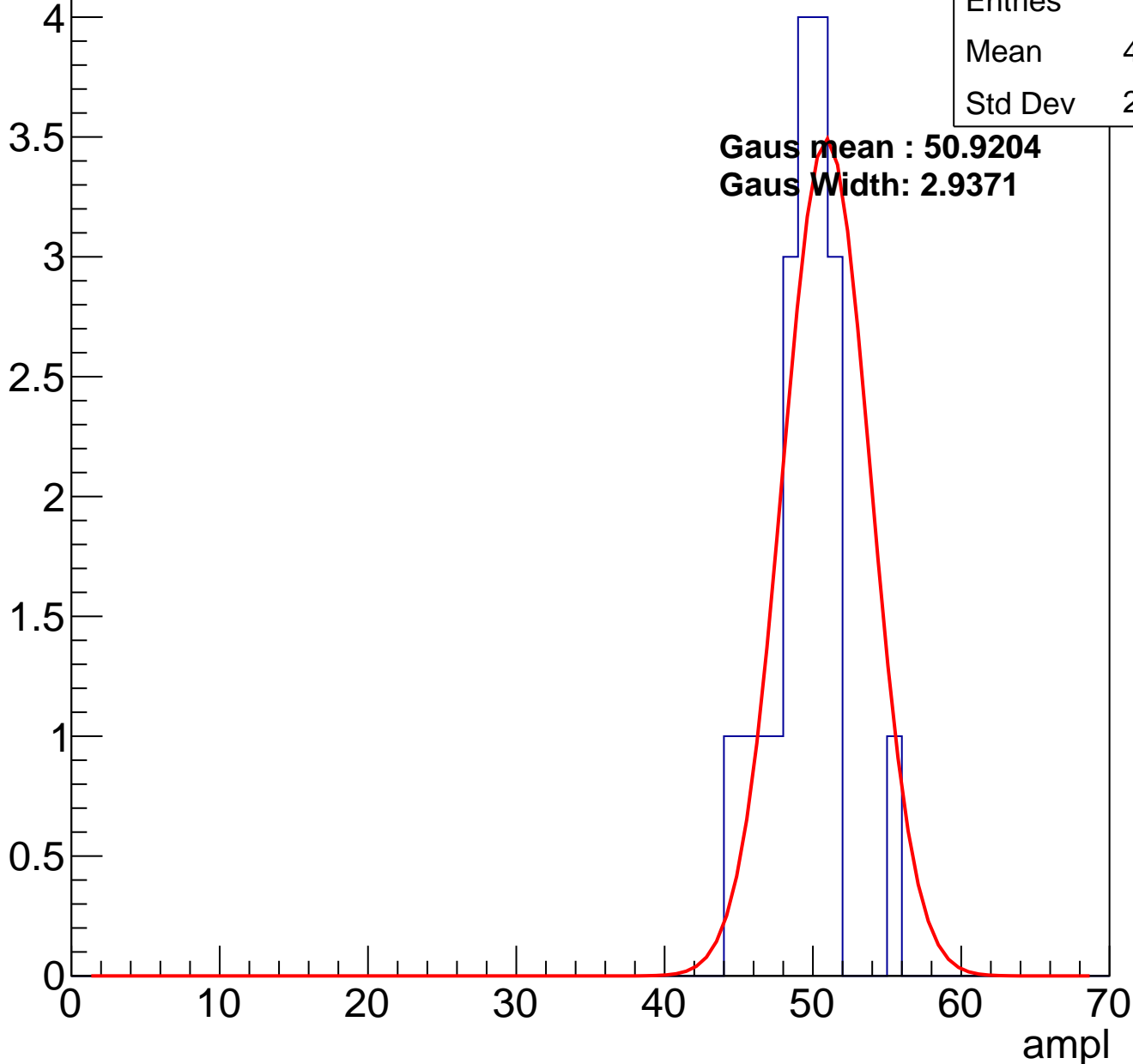
Entry



B0L100S, U12-ch95, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch95, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch95, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch95, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch95, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch95, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch96, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry

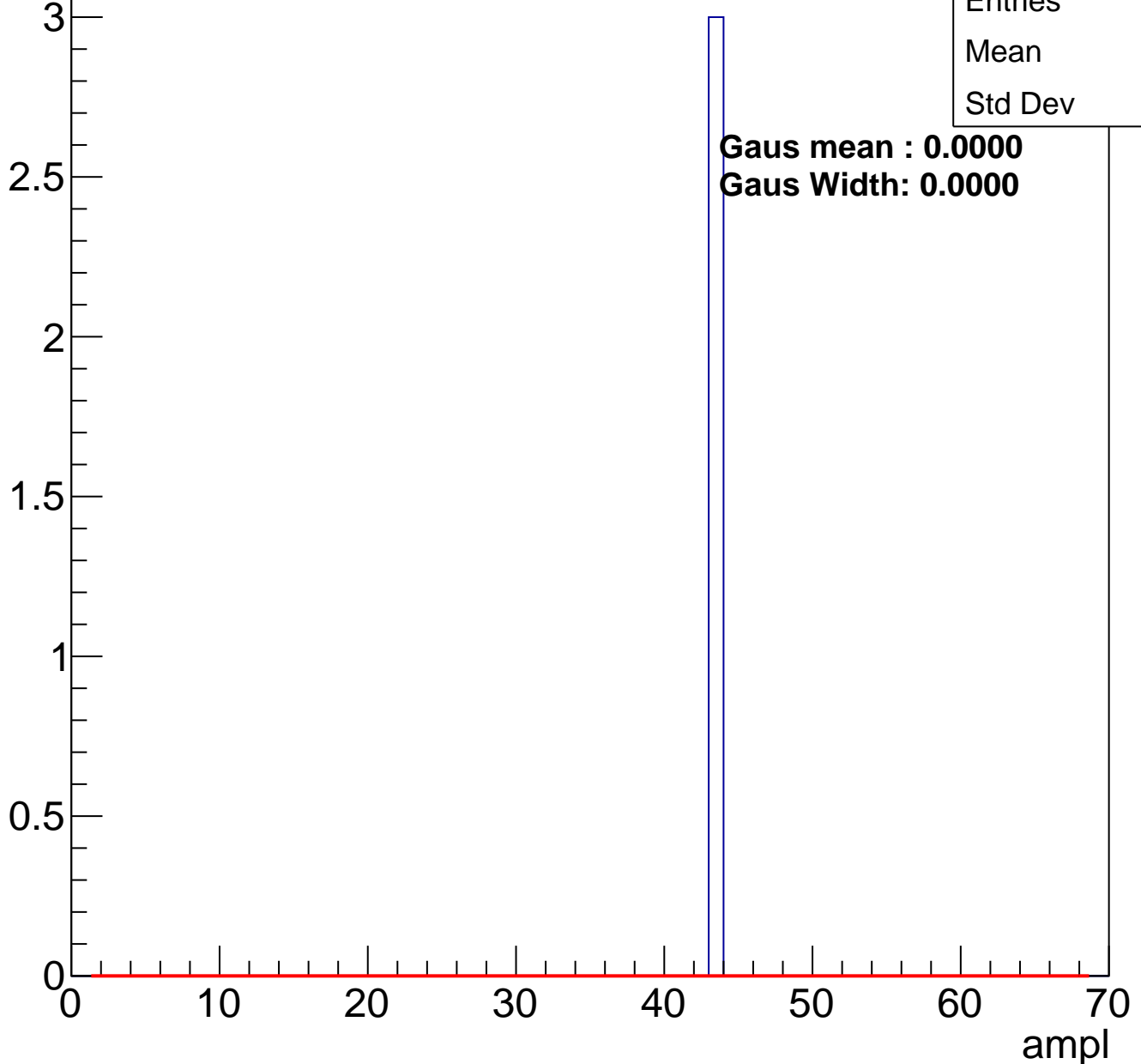


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch96, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	3
Mean	43
Std Dev	0

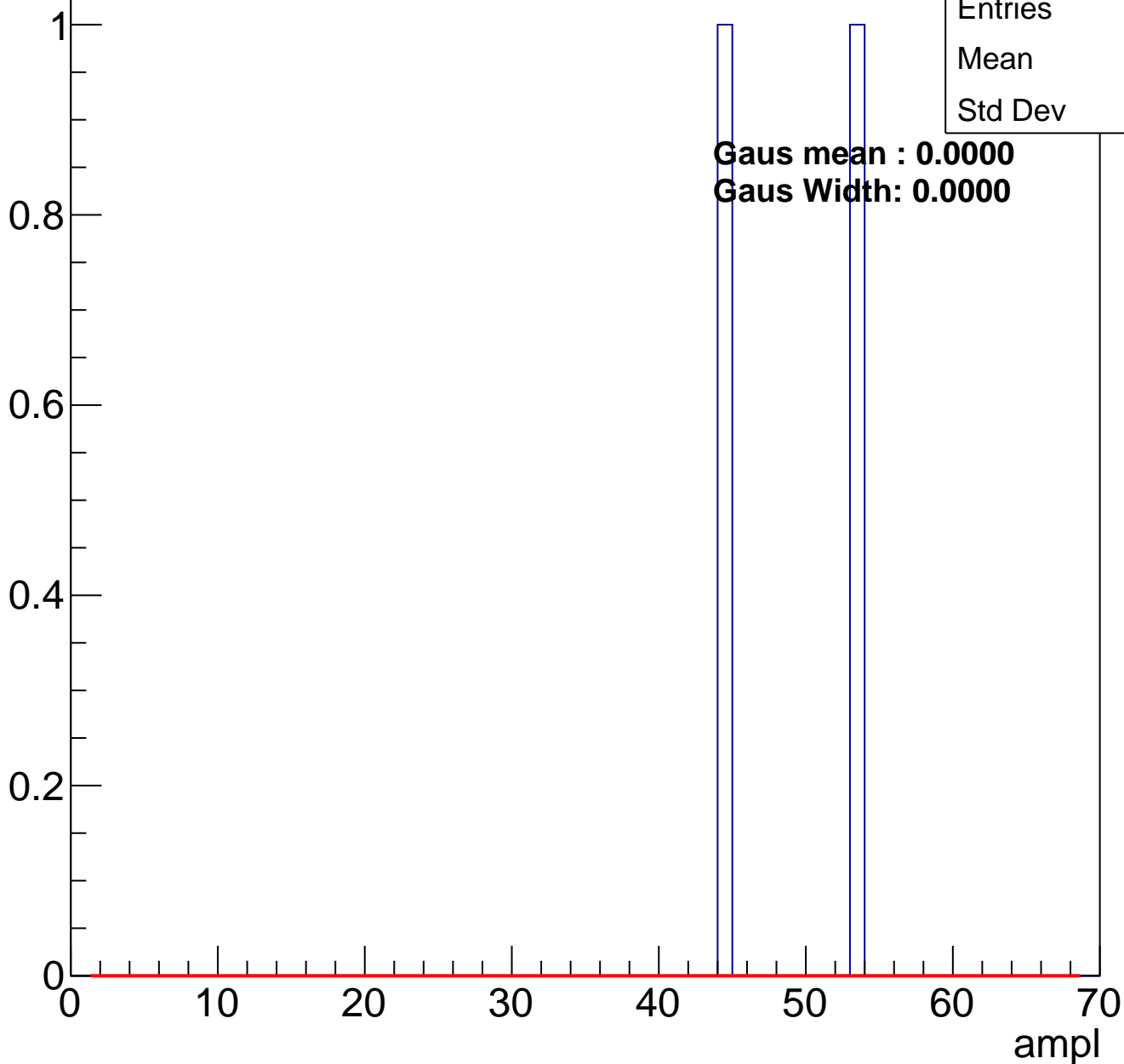
Gaus mean : 0.0000

Gaus Width: 0.0000

B0L100S, U12-ch96, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch96, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	2
Mean	53
Std Dev	0

0 10 20 30 40 50 60 70

ampl



B0L100S, U12-ch96, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch96, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch96, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch96, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch97, adc0

calib_packv5_042523_0143.root, FC#6, port A1

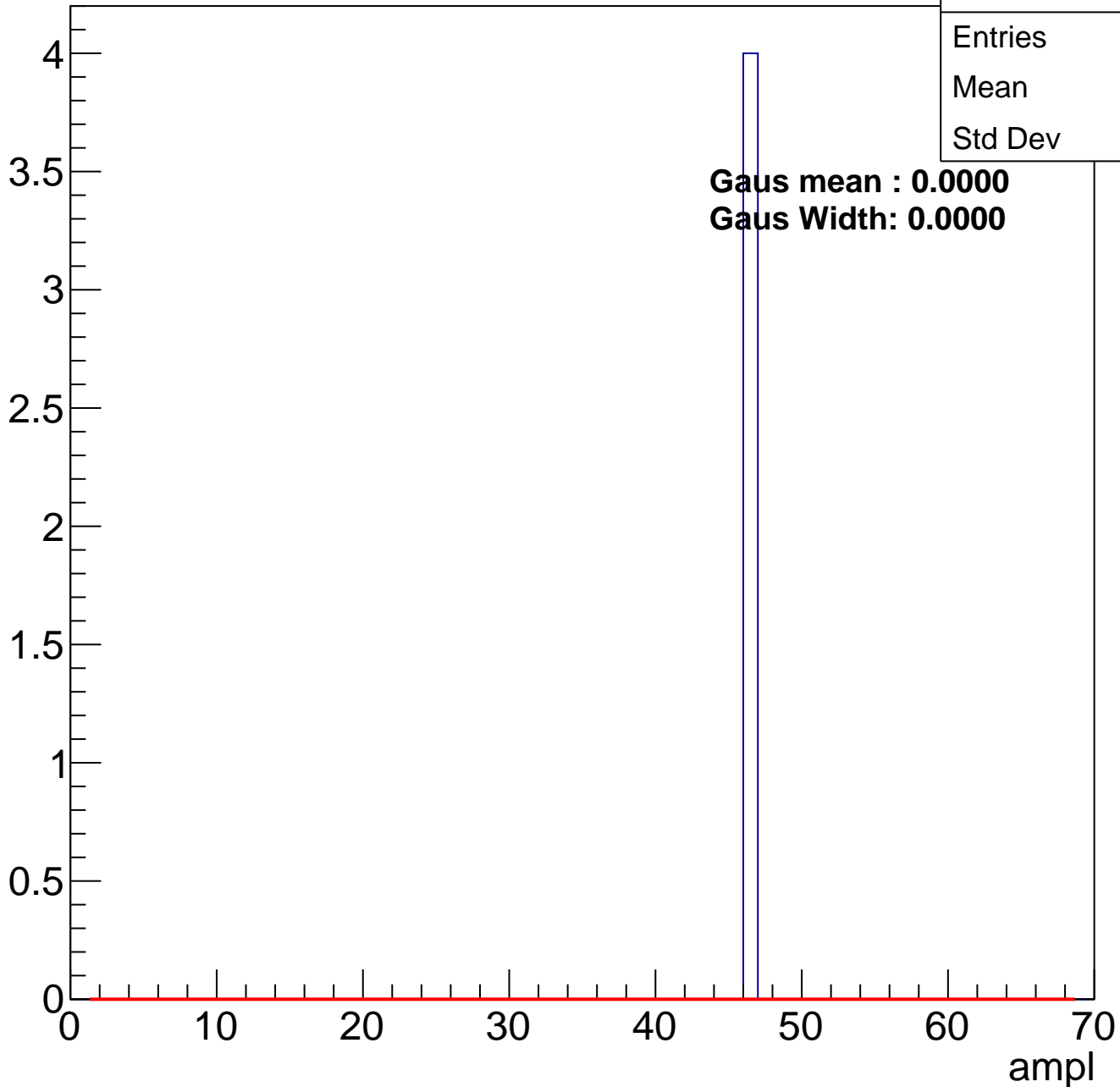
Entry



B0L100S, U12-ch97, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	4
Mean	46
Std Dev	0

Gaus mean : 0.0000

Gaus Width: 0.0000

B0L100S, U12-ch97, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

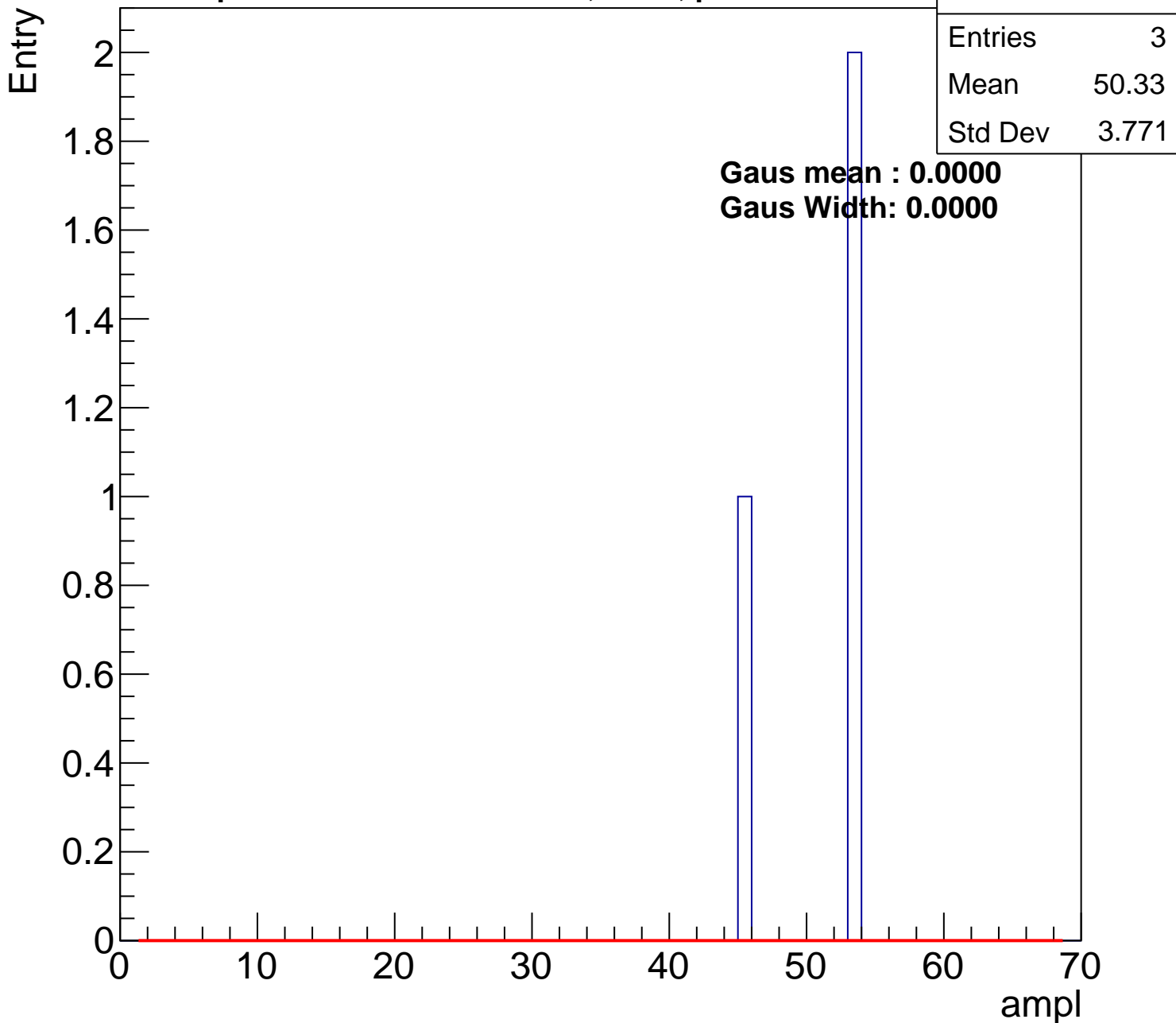
Entries	3
Mean	50.33
Std Dev	3.771

Gaus mean : 0.0000

Gaus Width: 0.0000

0 10 20 30 40 50 60 70

ampl



B0L100S, U12-ch97, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch97, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch97, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch97, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch97, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch98, adc0

calib_packv5_042523_0143.root, FC#6, port A1

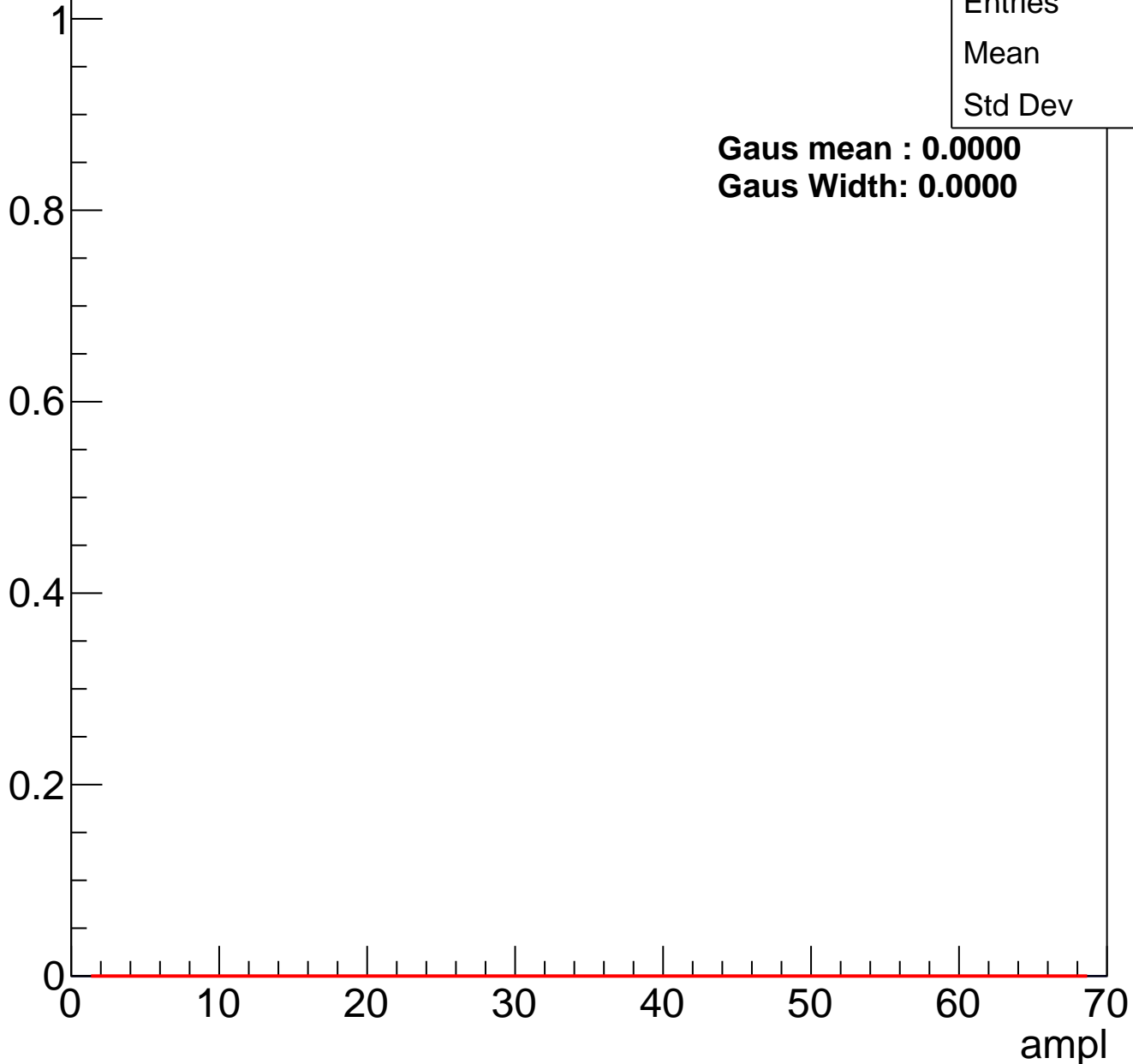
Entry



B0L100S, U12-ch98, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch98, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch98, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch98, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch98, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch98, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch98, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch99, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch99, adc1

calib_packv5_042523_0143.root, FC#6, port A1

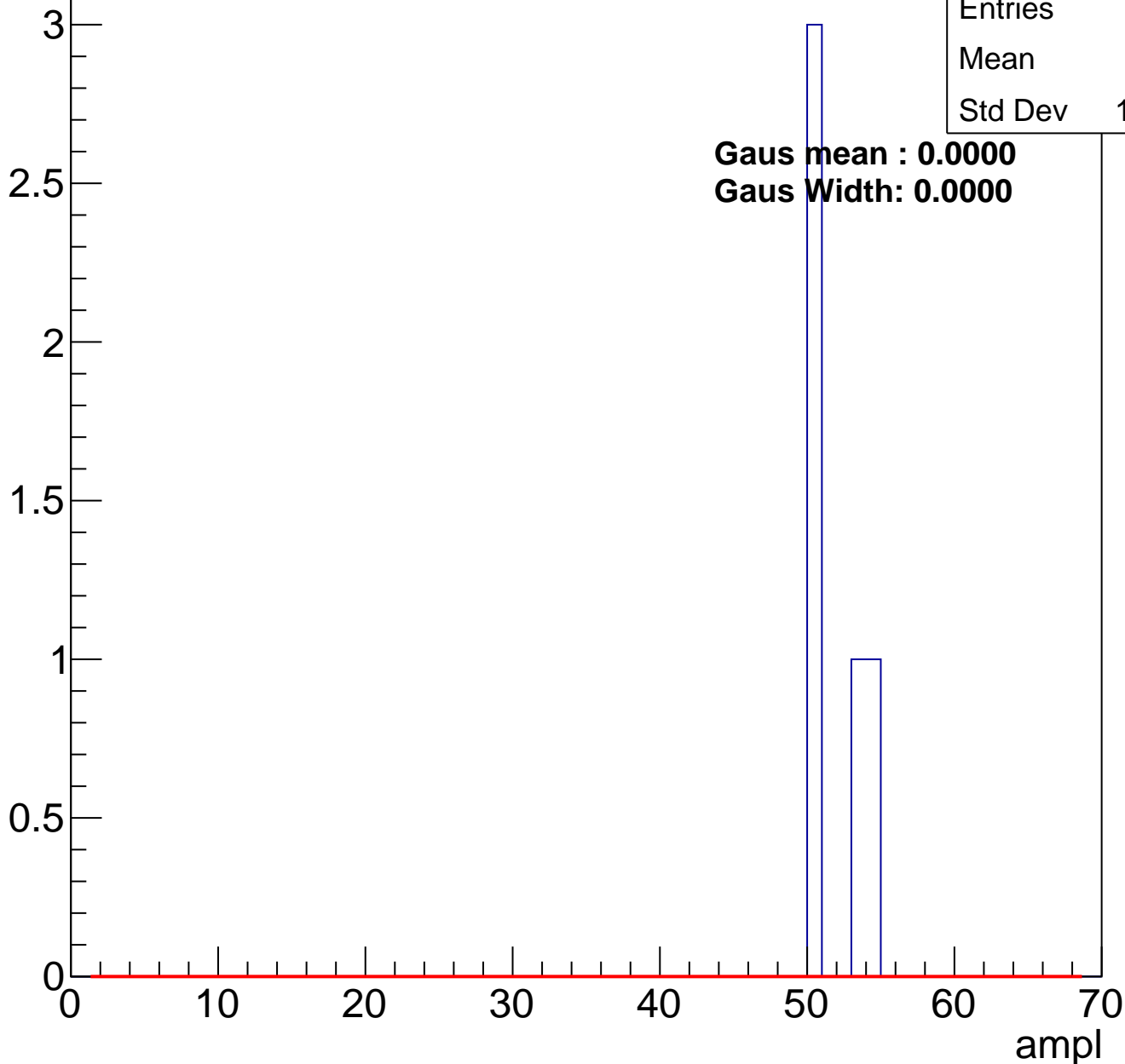
Entry



B0L100S, U12-ch99, adc2

calib_packv5_042523_0143.root, FC#6, port A1

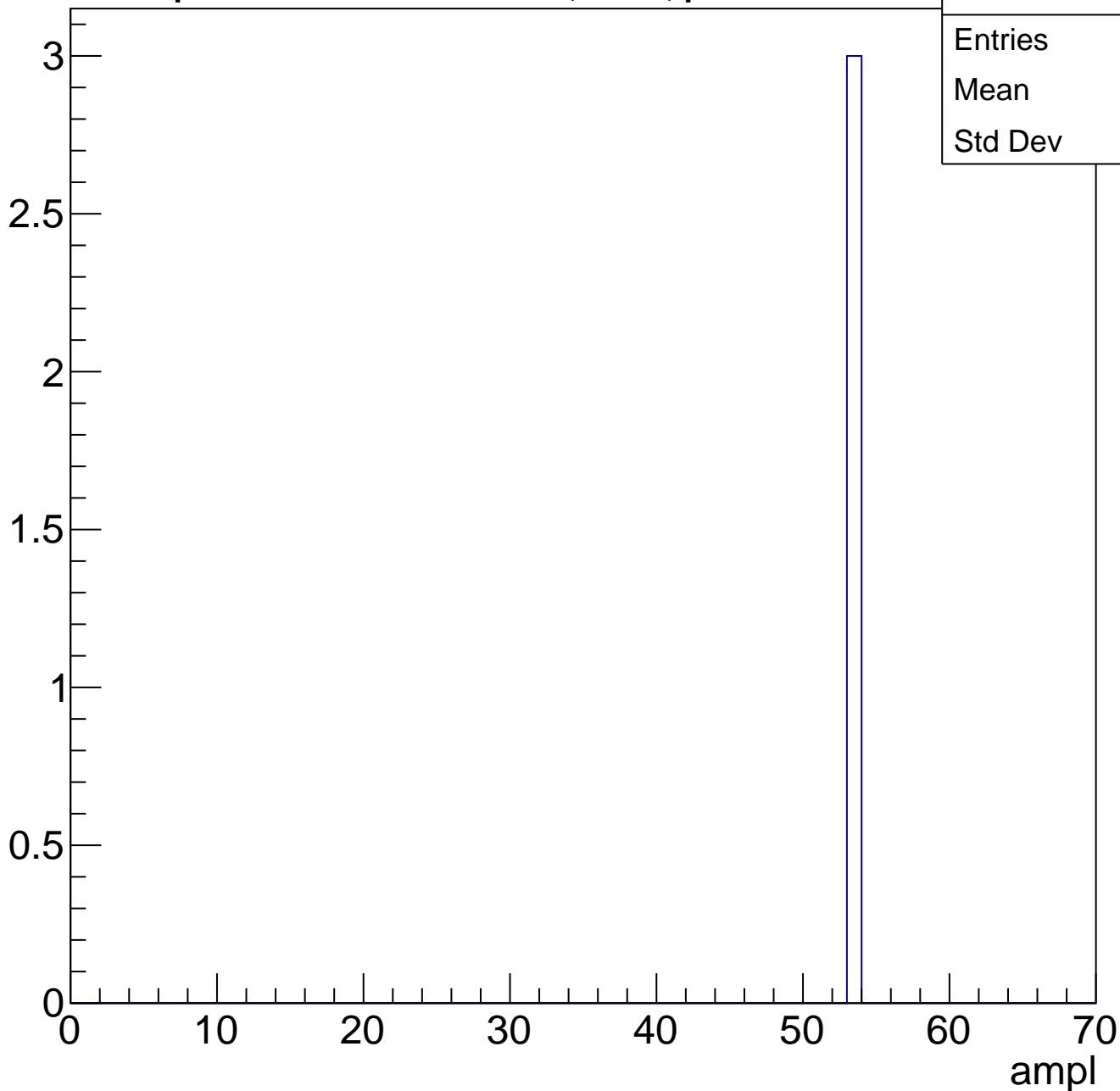
Entry



B0L100S, U12-ch99, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch99, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch99, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch99, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch99, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch100, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch100, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch100, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch100, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch100, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch100, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch100, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch100, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch101, adc0

calib_packv5_042523_0143.root, FC#6, port A1

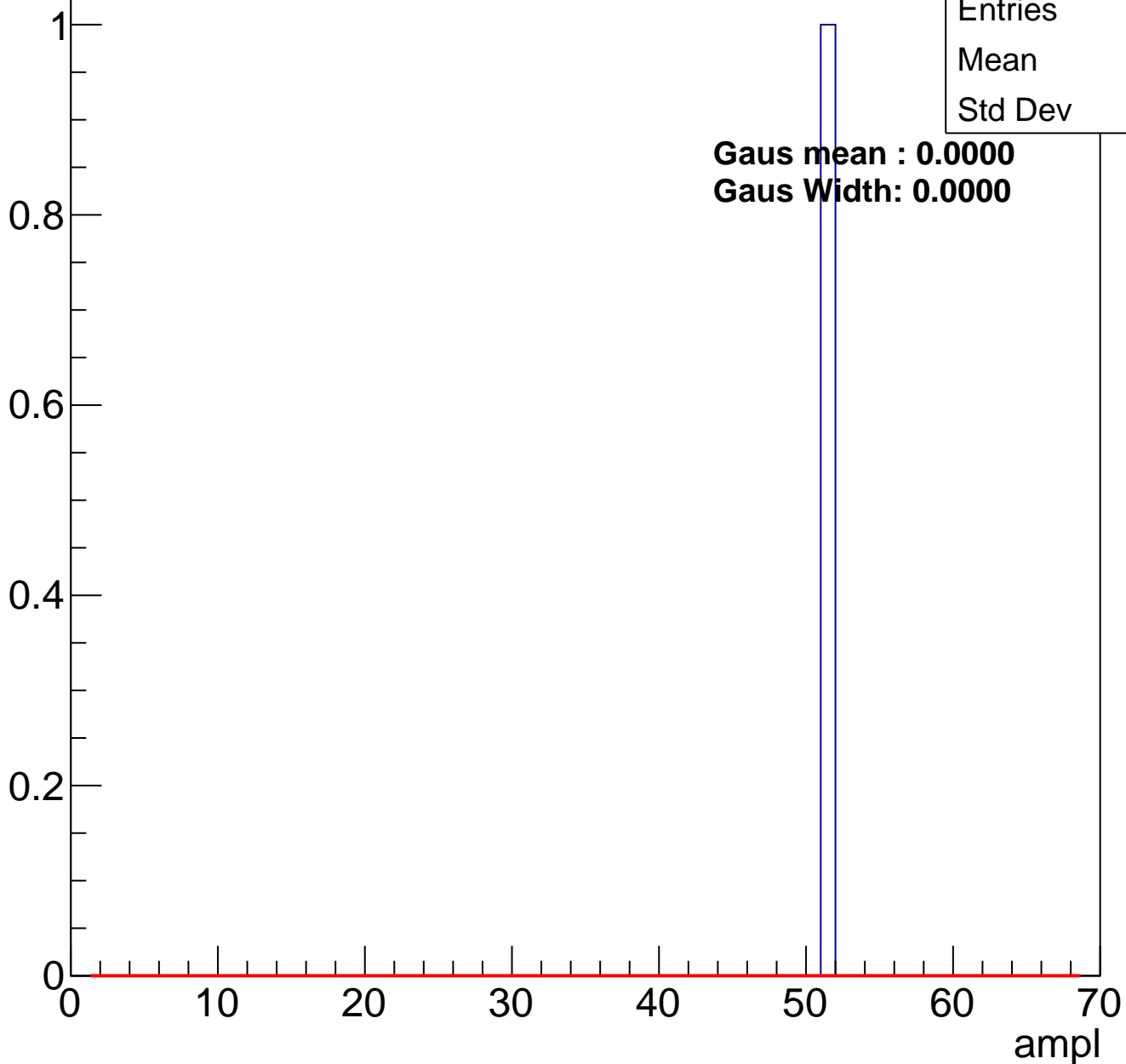
Entry



B0L100S, U12-ch101, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch101, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

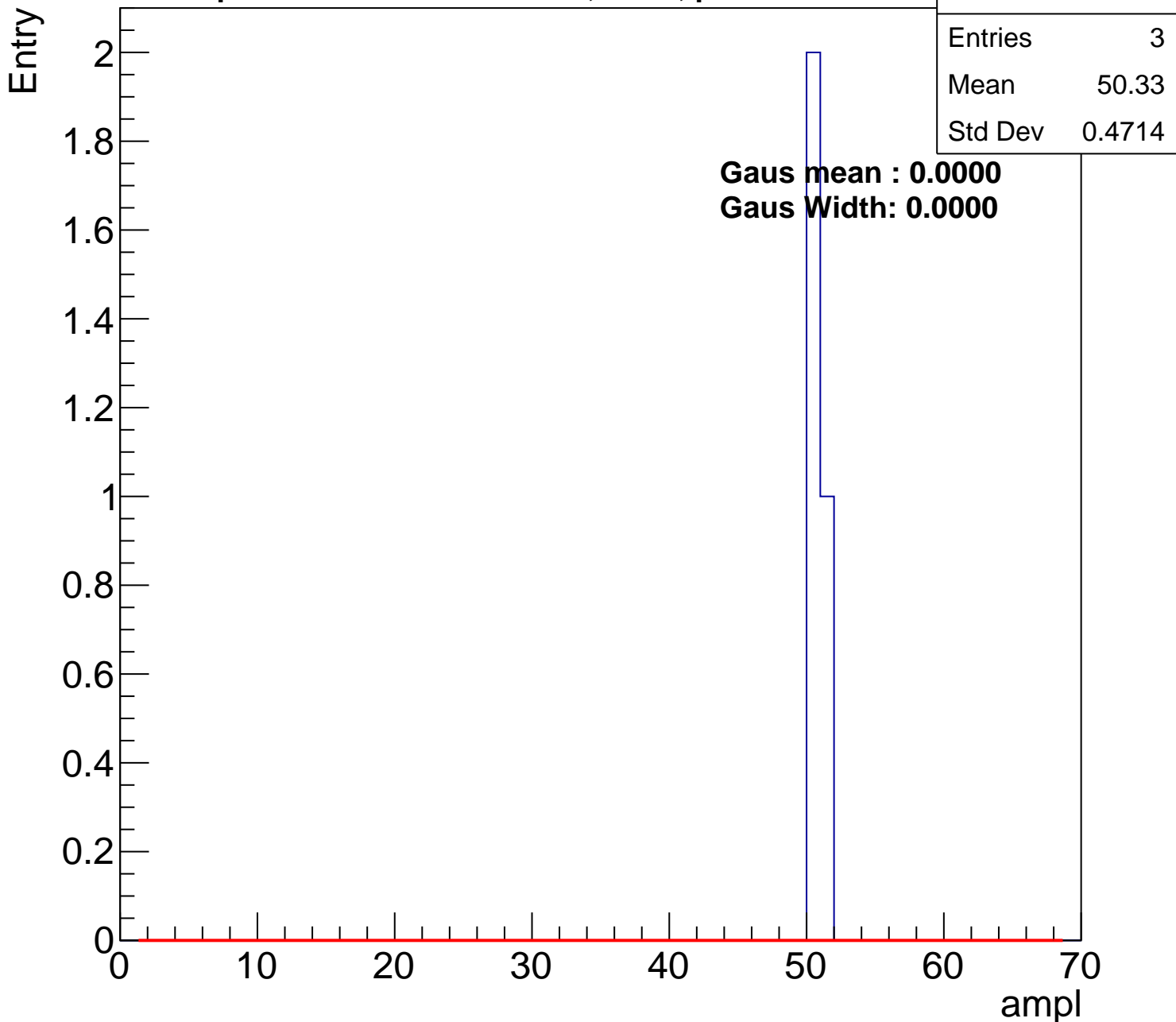
Entries	3
Mean	50.33
Std Dev	0.4714

Gaus mean : 0.0000

Gaus Width: 0.0000

0 10 20 30 40 50 60 70

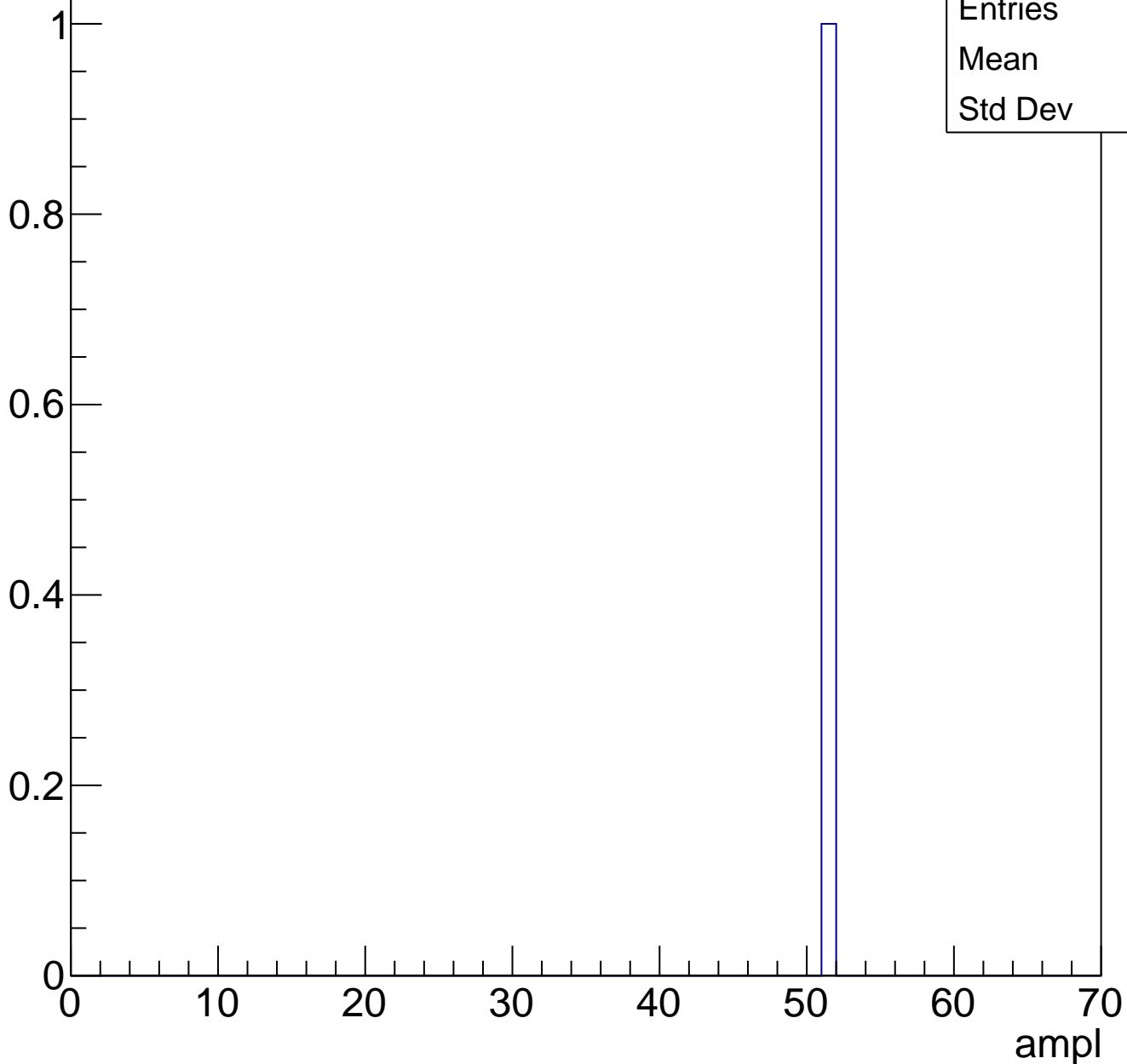
ampl



B0L100S, U12-ch101, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch101, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch101, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch101, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch101, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch102, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch102, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch102, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch102, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch102, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch102, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch102, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch102, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch103, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch103, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

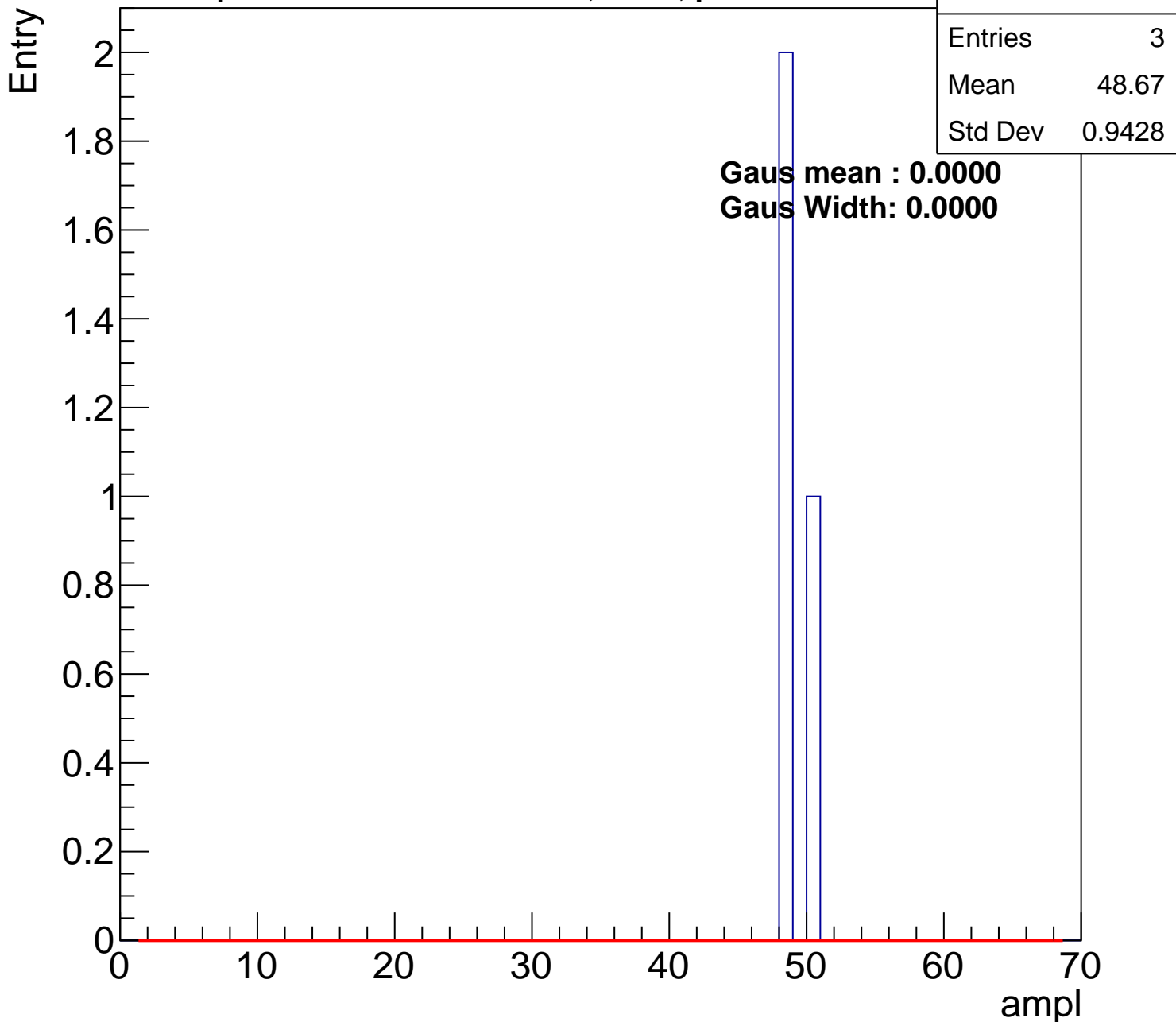
Entries	3
Mean	48.67
Std Dev	0.9428

Gaus mean : 0.0000

Gaus Width: 0.0000

0 10 20 30 40 50 60 70

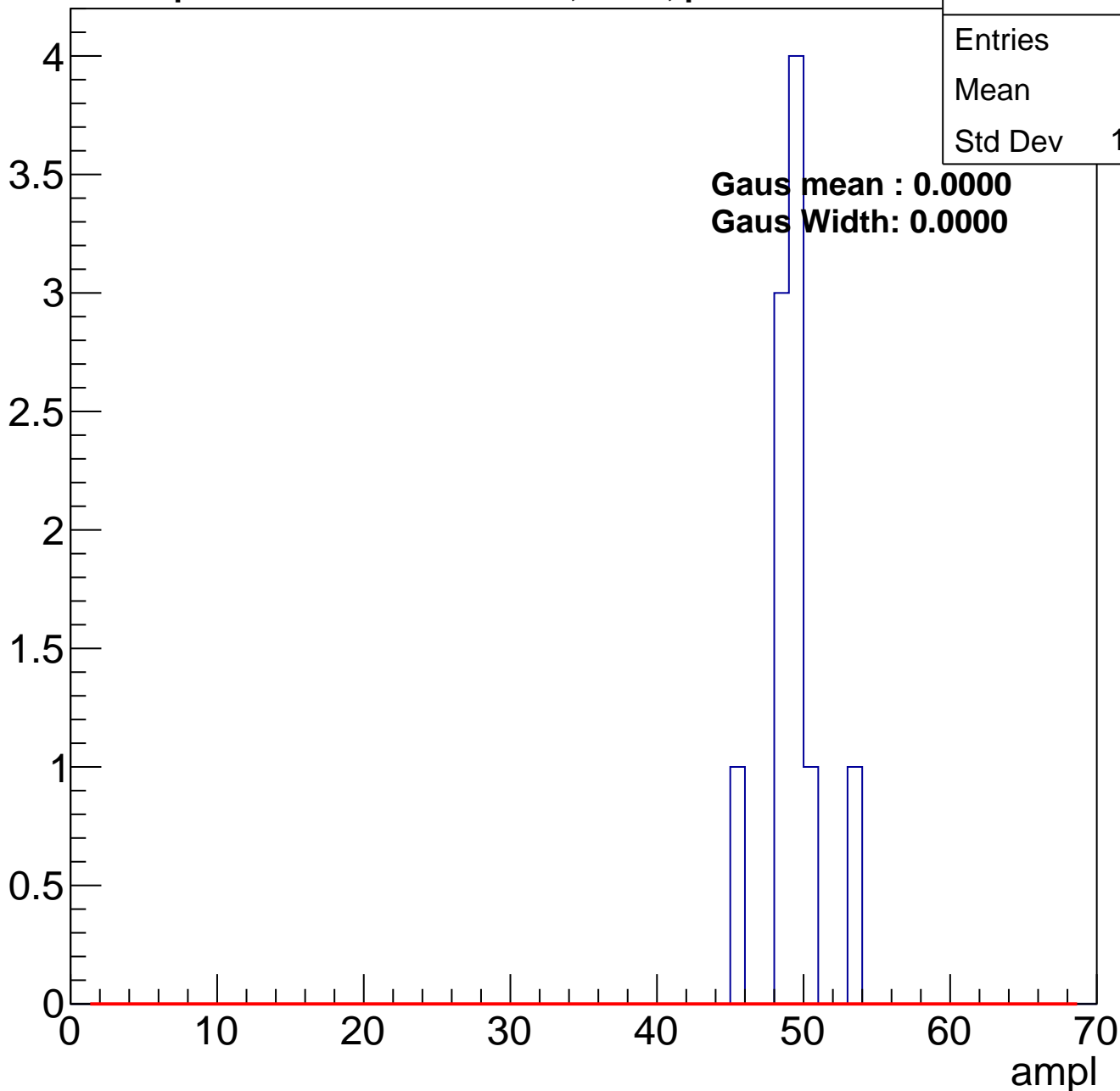
ampl



B0L100S, U12-ch103, adc2

calib_packv5_042523_0143.root, FC#6, port A1

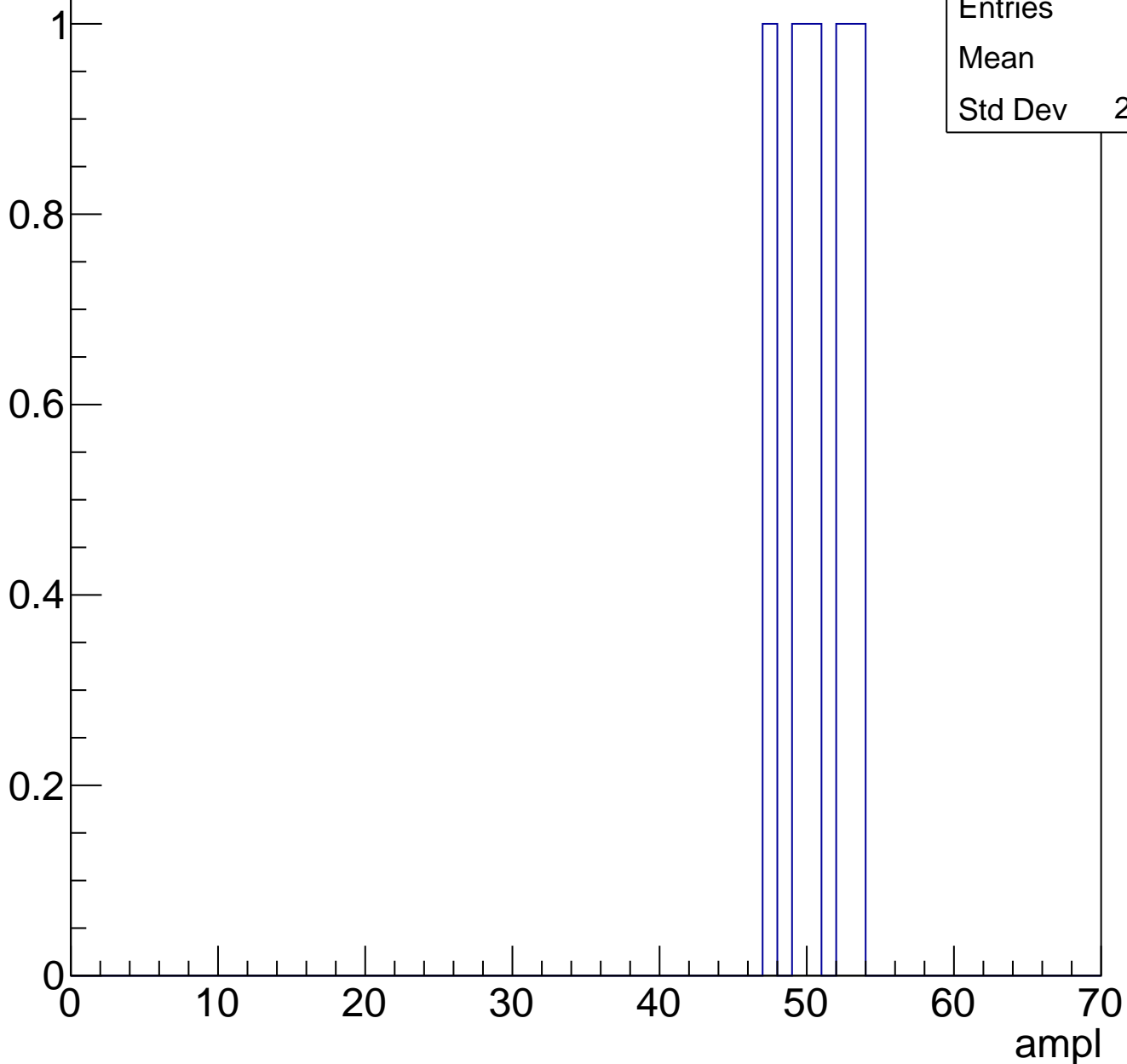
Entry



B0L100S, U12-ch103, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch103, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch103, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch103, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch103, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch104, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch104, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch104, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

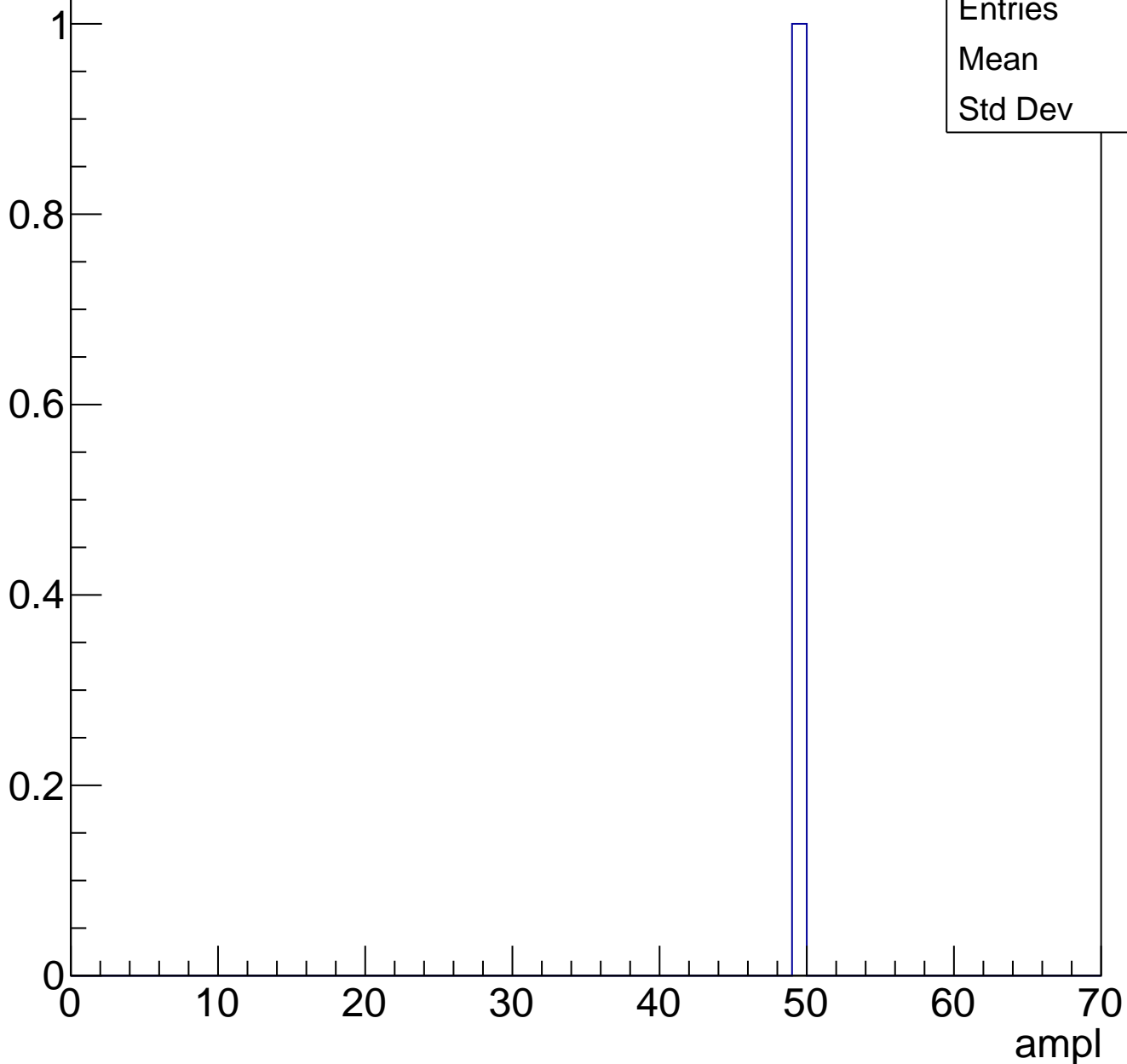


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch104, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch104, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch104, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch104, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch104, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch105, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch105, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch105, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch105, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch105, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch105, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch105, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch105, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch106, adc0

calib_packv5_042523_0143.root, FC#6, port A1

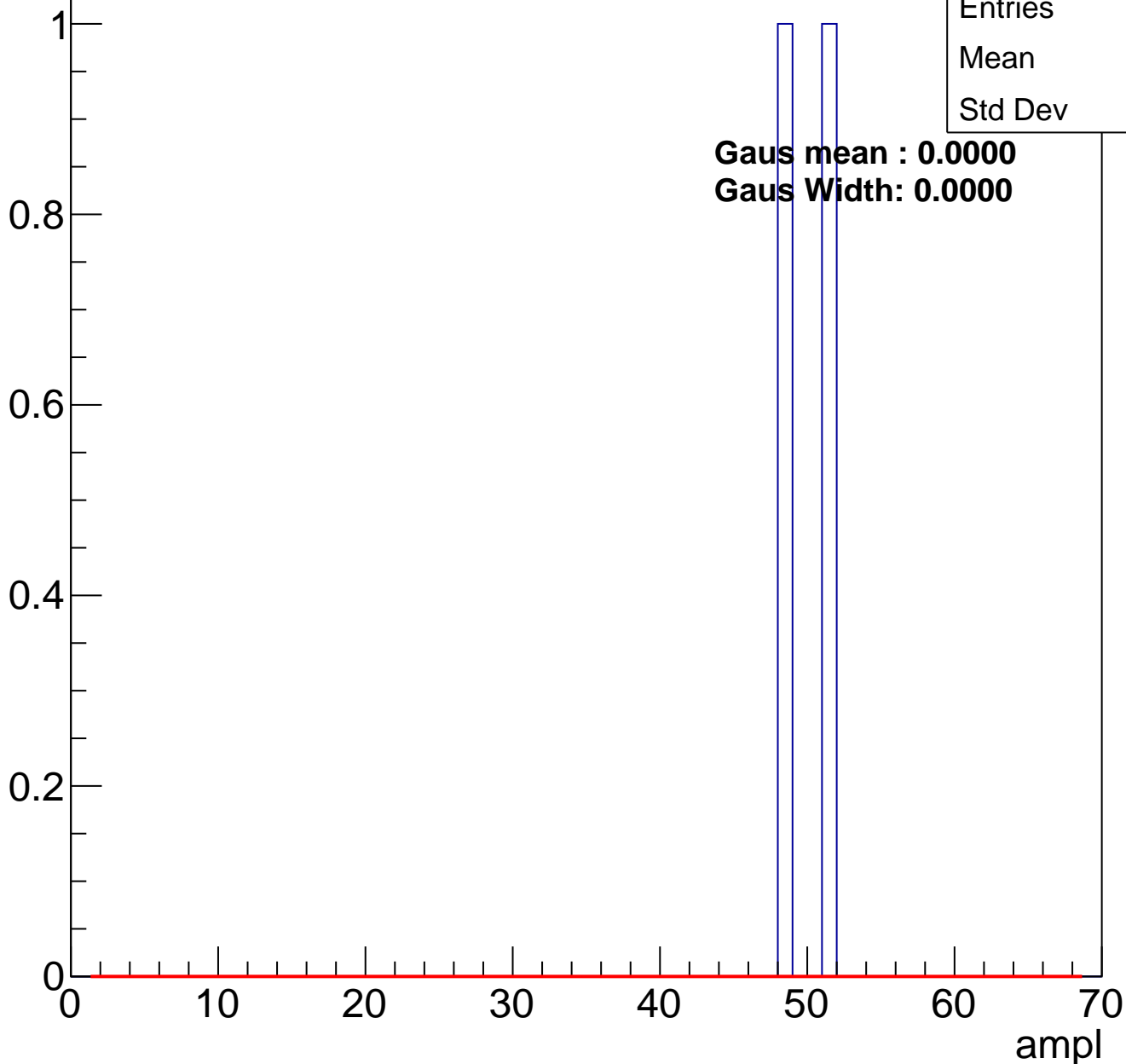
Entry



B0L100S, U12-ch106, adc1

calib_packv5_042523_0143.root, FC#6, port A1

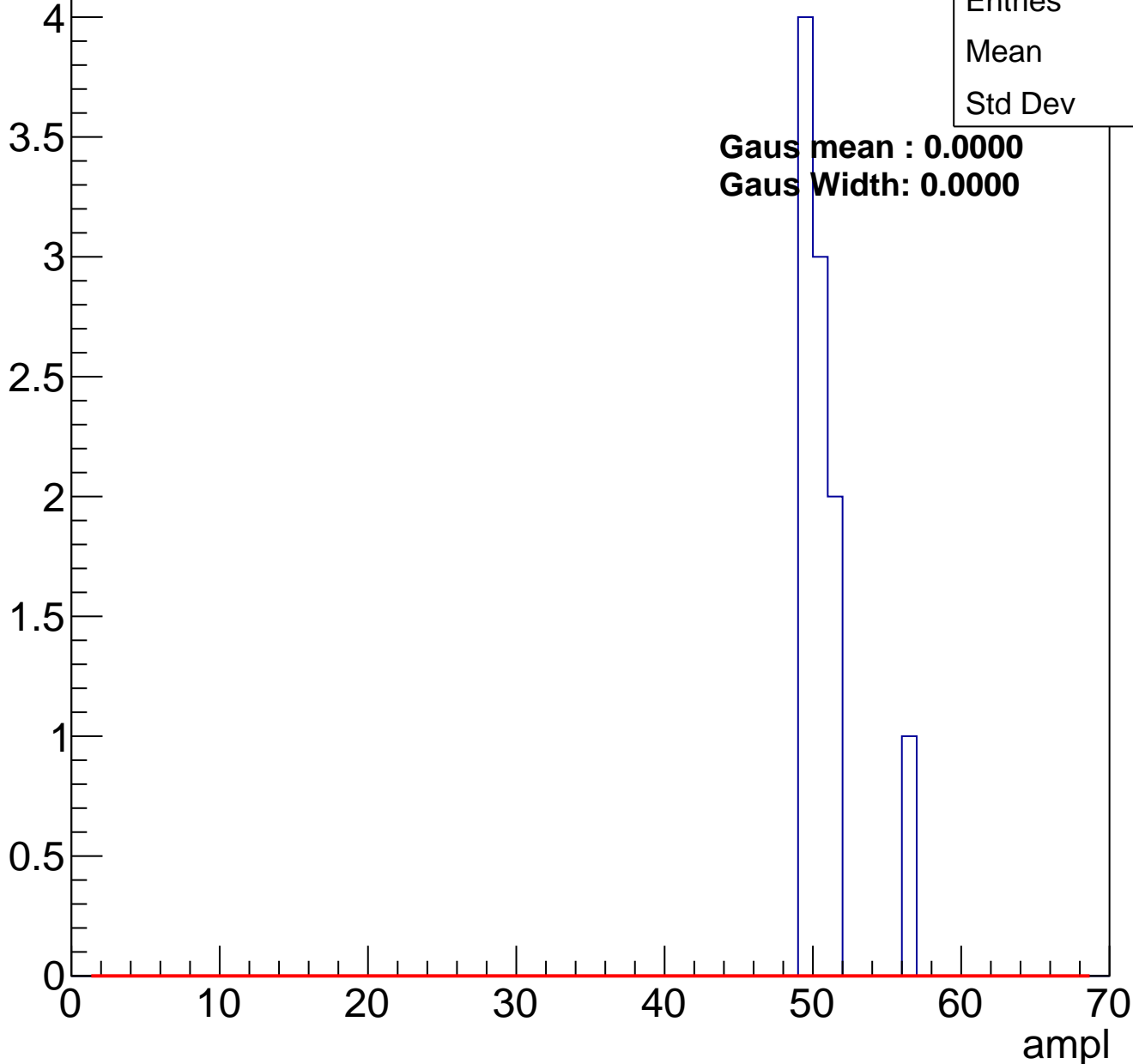
Entry



B0L100S, U12-ch106, adc2

calib_packv5_042523_0143.root, FC#6, port A1

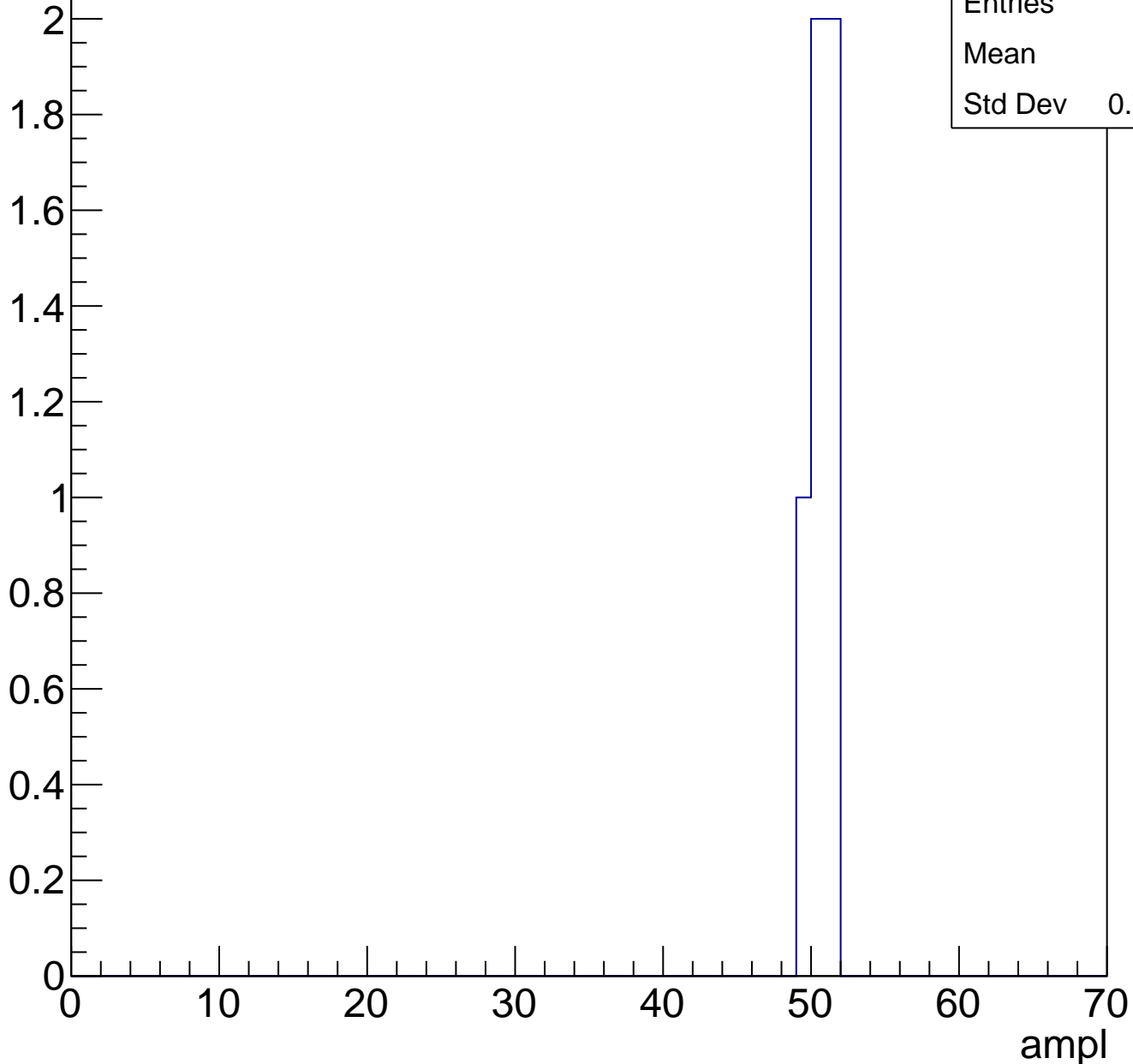
Entry



B0L100S, U12-ch106, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch106, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch106, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch106, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch106, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch107, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch107, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch107, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

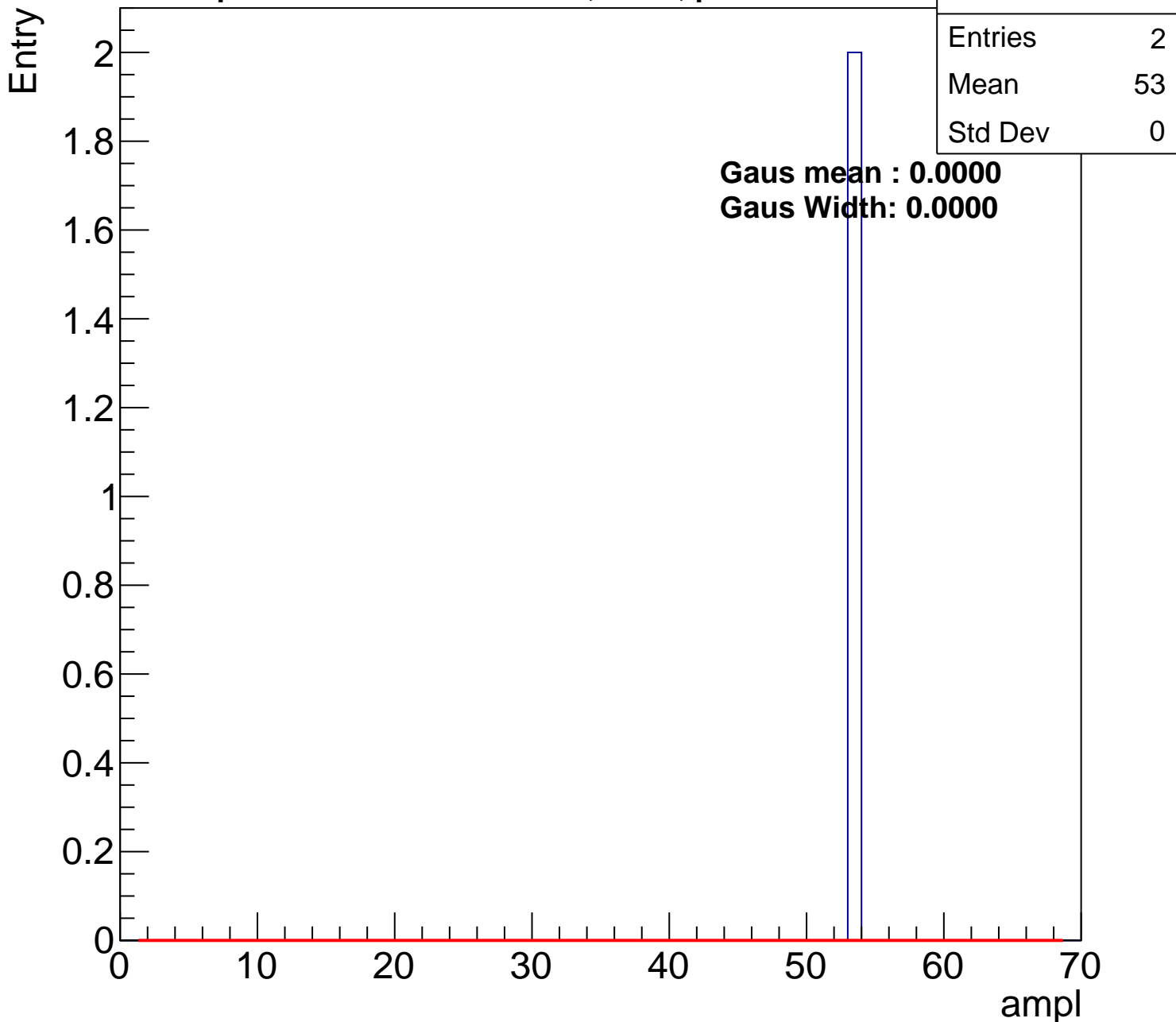
Entries	2
Mean	53
Std Dev	0

Gaus mean : 0.0000

Gaus Width: 0.0000

0 10 20 30 40 50 60 70

ampl



B0L100S, U12-ch107, adc3

calib_packv5_042523_0143.root, FC#6, port A1

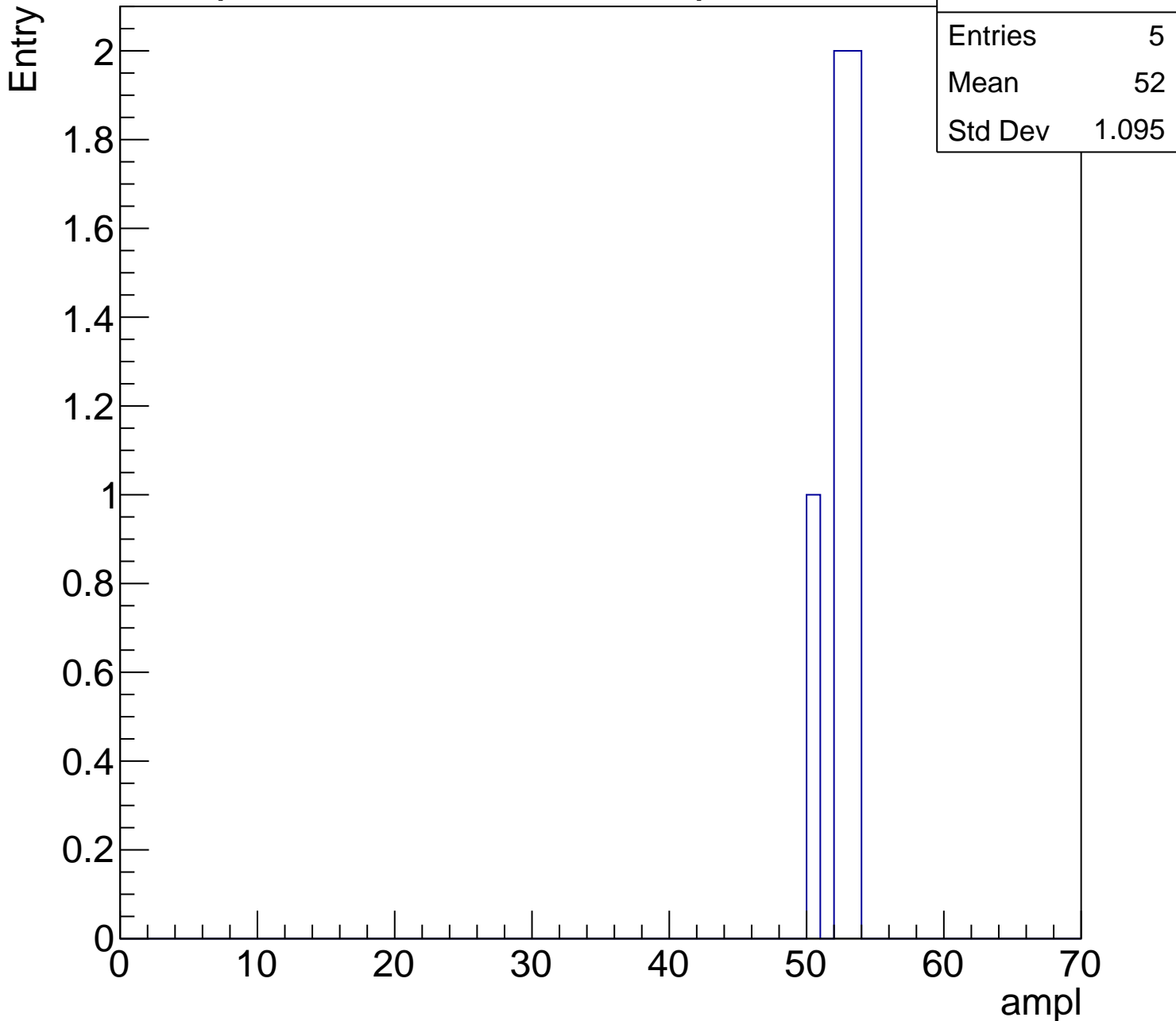
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	5
Mean	52
Std Dev	1.095

0 10 20 30 40 50 60 70

ampl



B0L100S, U12-ch107, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch107, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch107, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch107, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry

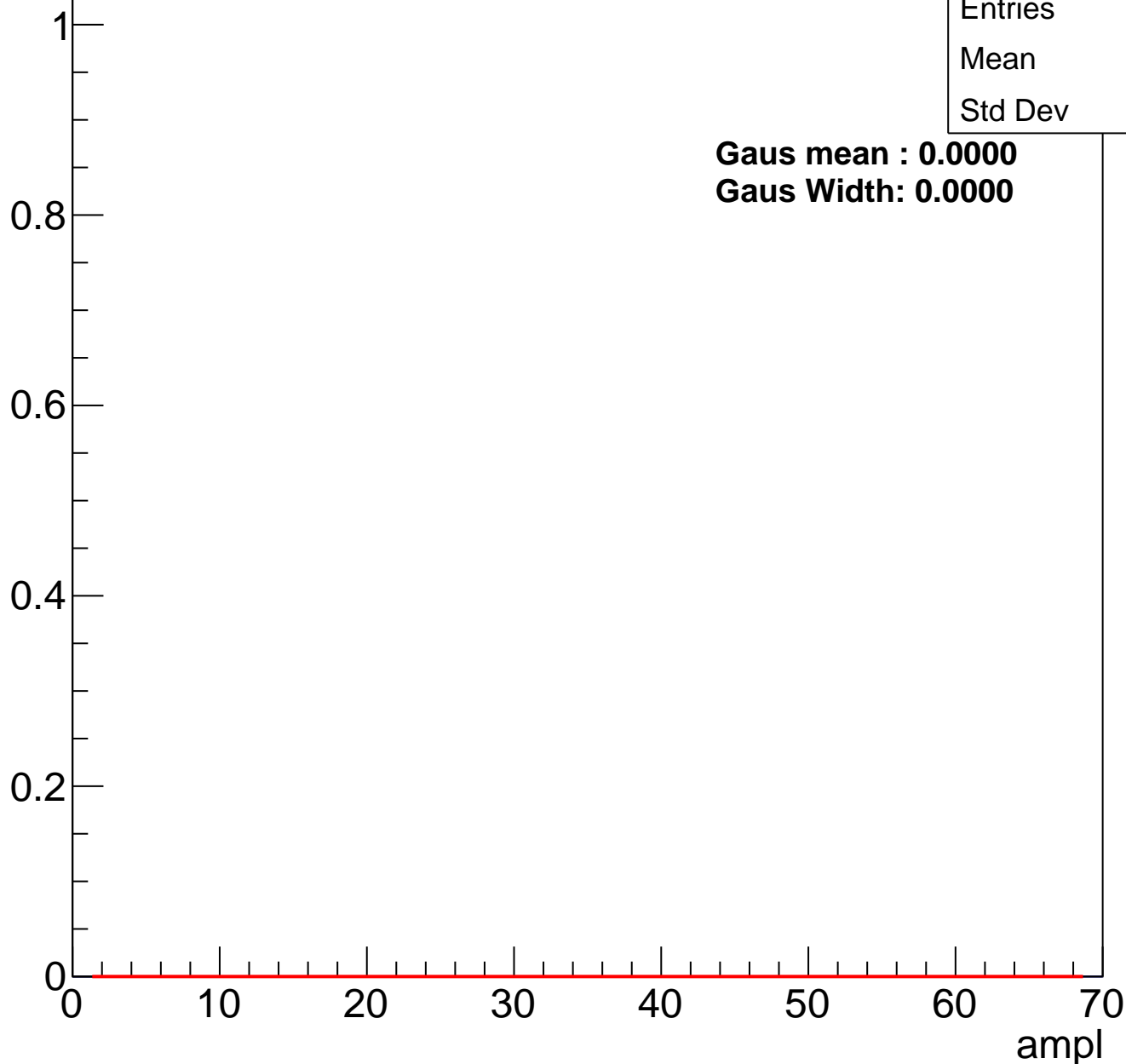


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch108, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch108, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch108, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch108, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch108, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch108, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch108, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch108, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry

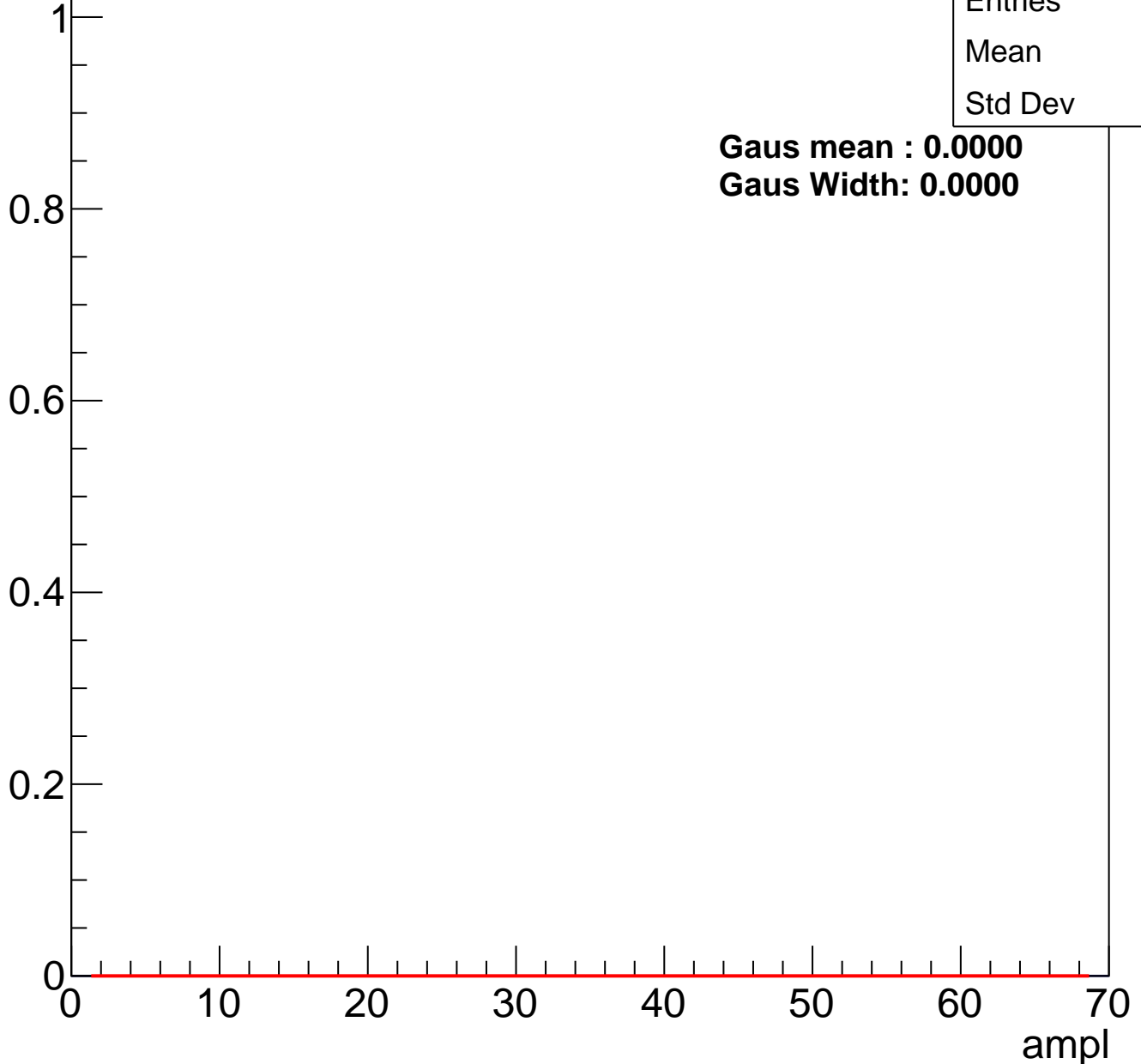


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch109, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch109, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch109, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch109, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch109, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch109, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch109, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch109, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch110, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch110, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch110, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch110, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch110, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch110, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch110, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch110, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry

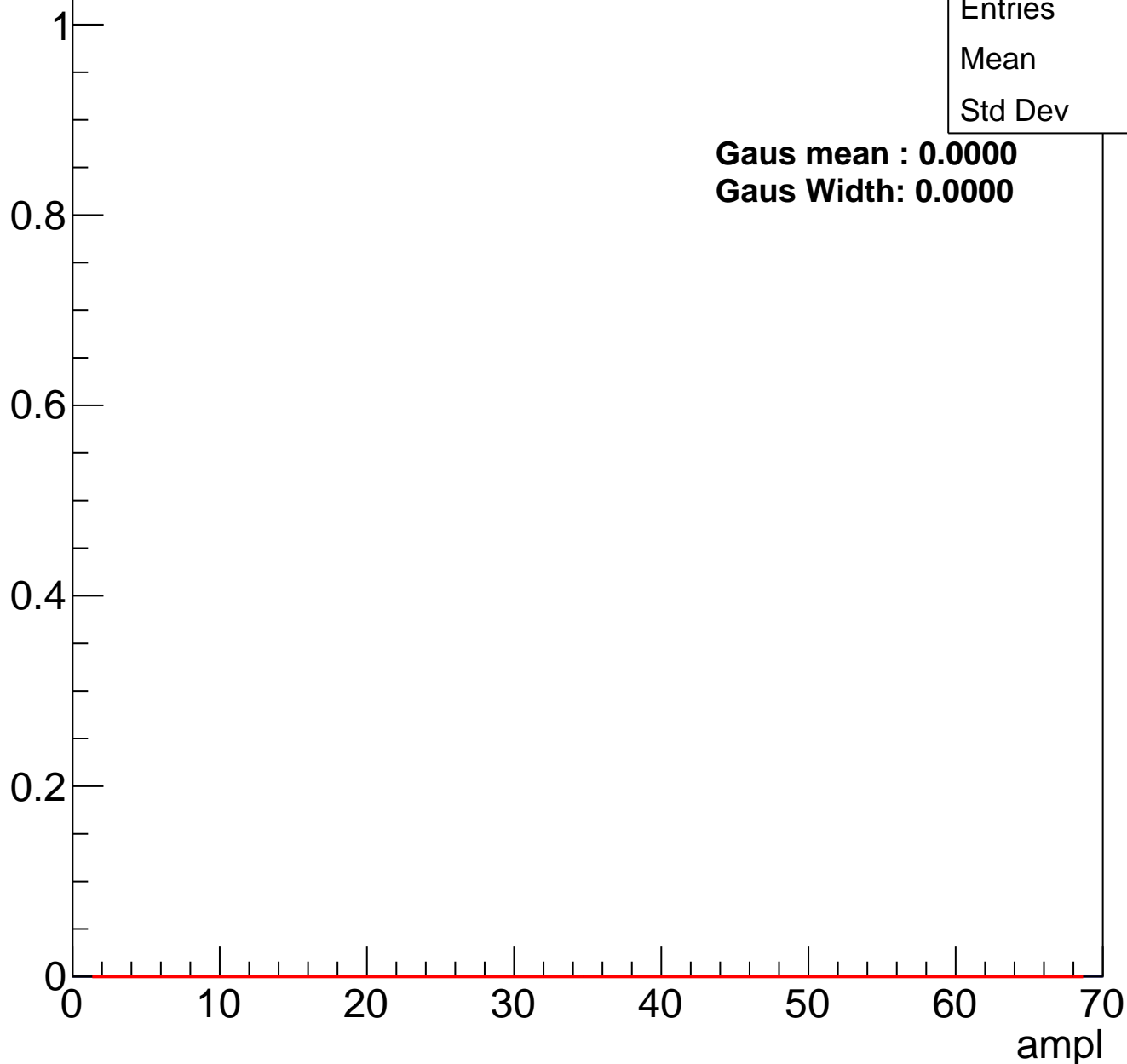


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch111, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch111, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch111, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch111, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch111, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch111, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch111, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch111, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch112, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch112, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch112, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch112, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch112, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch112, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch112, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch112, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch113, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch113, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch113, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch113, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch113, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch113, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch113, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch113, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch114, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch114, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch114, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch114, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch114, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch114, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch114, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch114, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch115, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch115, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch115, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch115, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch115, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch115, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch115, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch115, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch116, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch116, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch116, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch116, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry

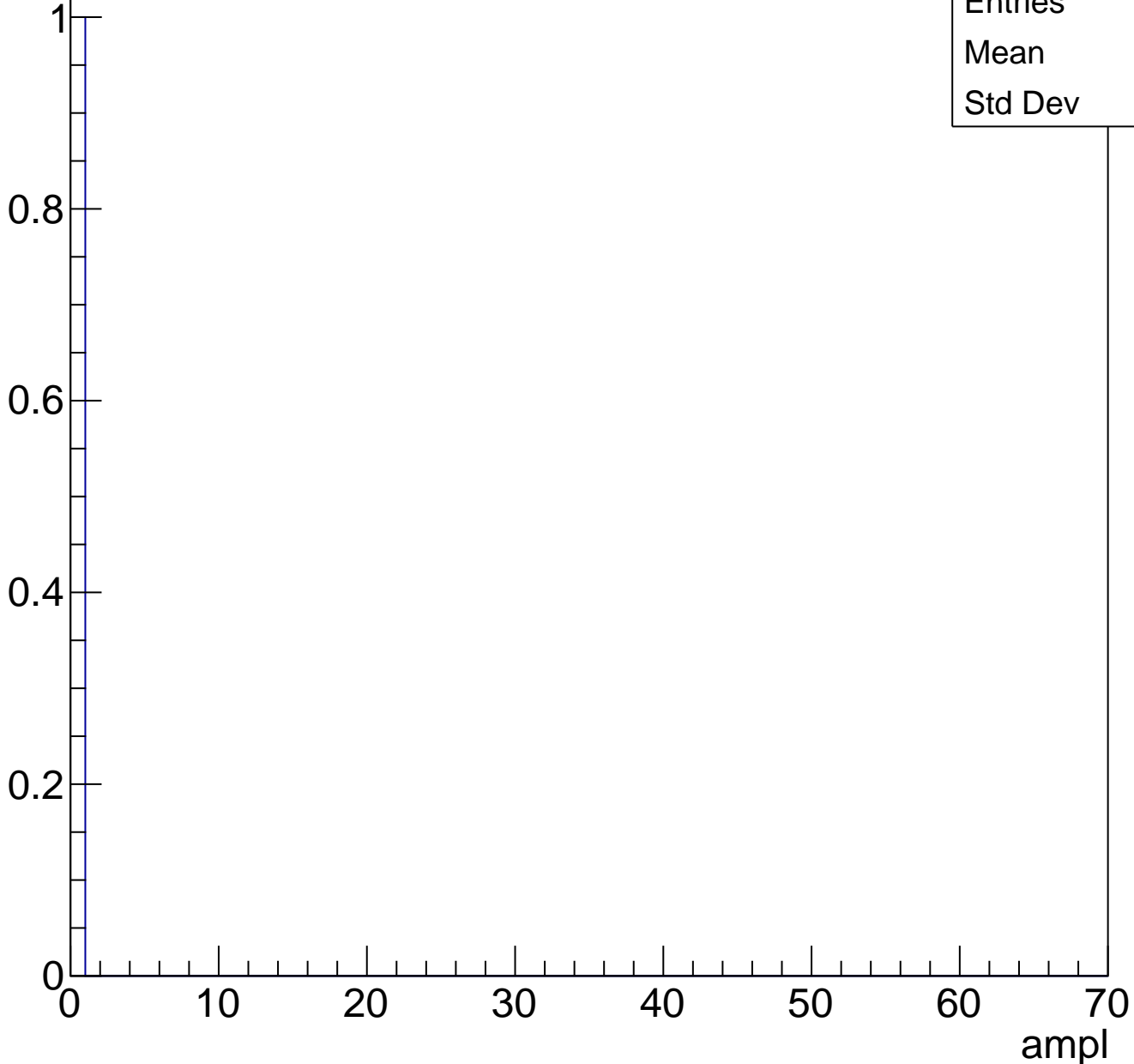


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch116, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch116, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch116, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch116, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch117, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch117, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch117, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch117, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch117, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch117, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch117, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch117, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch118, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Gaus mean : 0.0000

Gaus Width: 0.0000

Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch118, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	7
Mean	47
Std Dev	1.414

Gaus mean : 0.0000

Gaus Width: 0.0000

ampl

0 10 20 30 40 50 60 70

B0L100S, U12-ch118, adc2

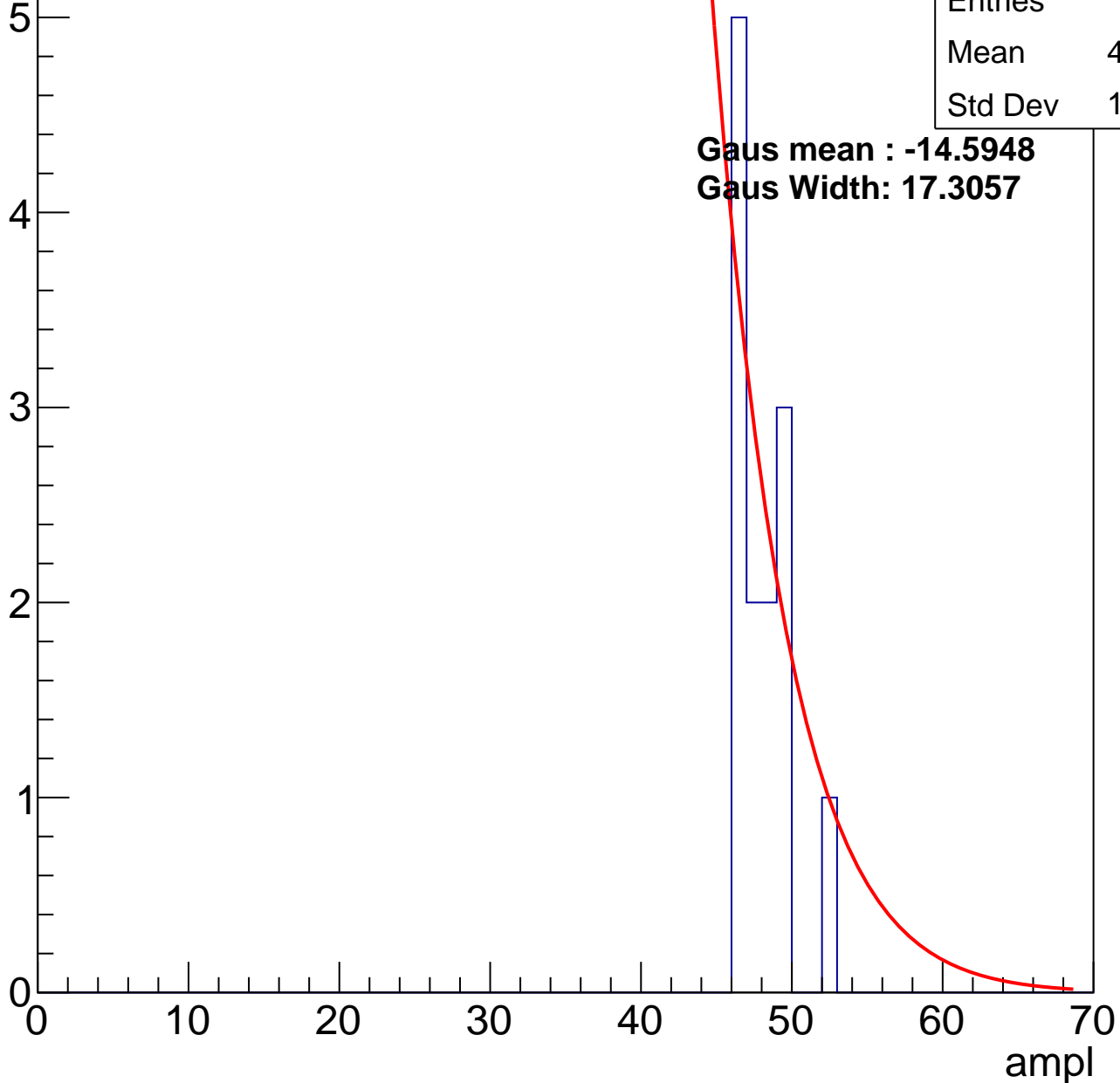
calib_packv5_042523_0143.root, FC#6, port A1

Entry

Entries	13
Mean	47.62
Std Dev	1.734

Gaus mean : -14.5948

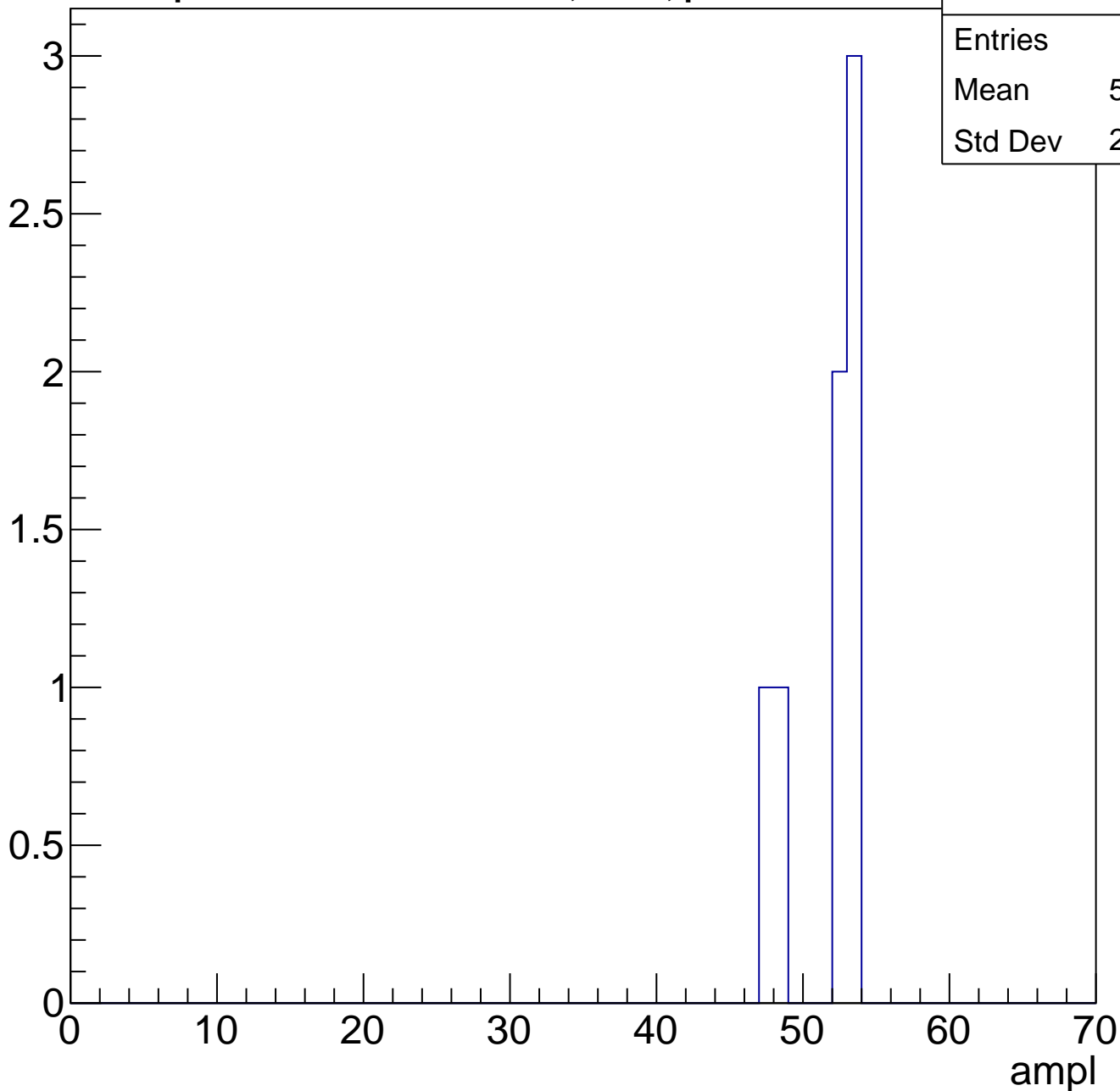
Gaus Width: 17.3057



B0L100S, U12-ch118, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch118, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry

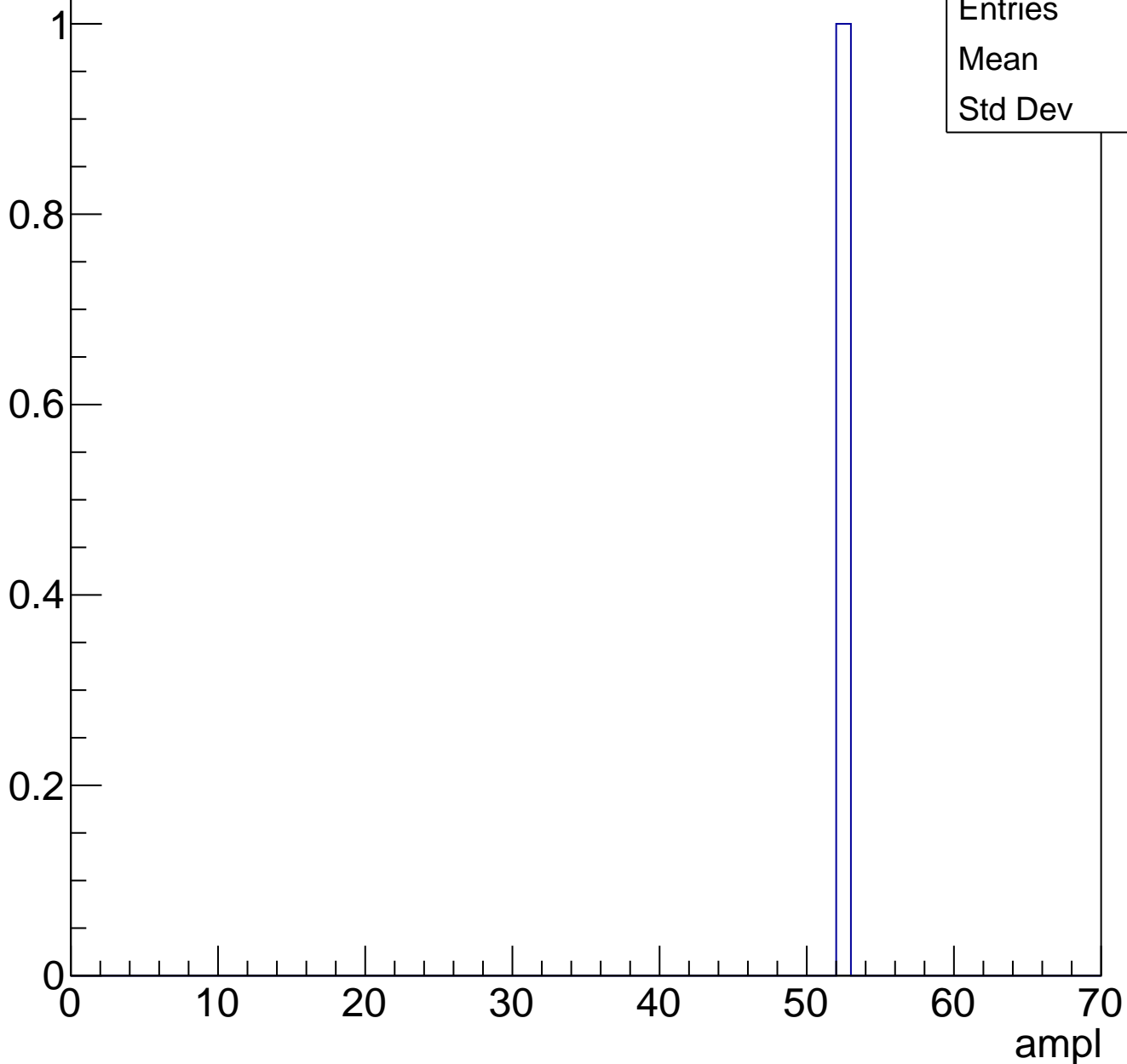


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch118, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch118, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch118, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch119, adc0

calib_packv5_042523_0143.root, FC#6, port A1

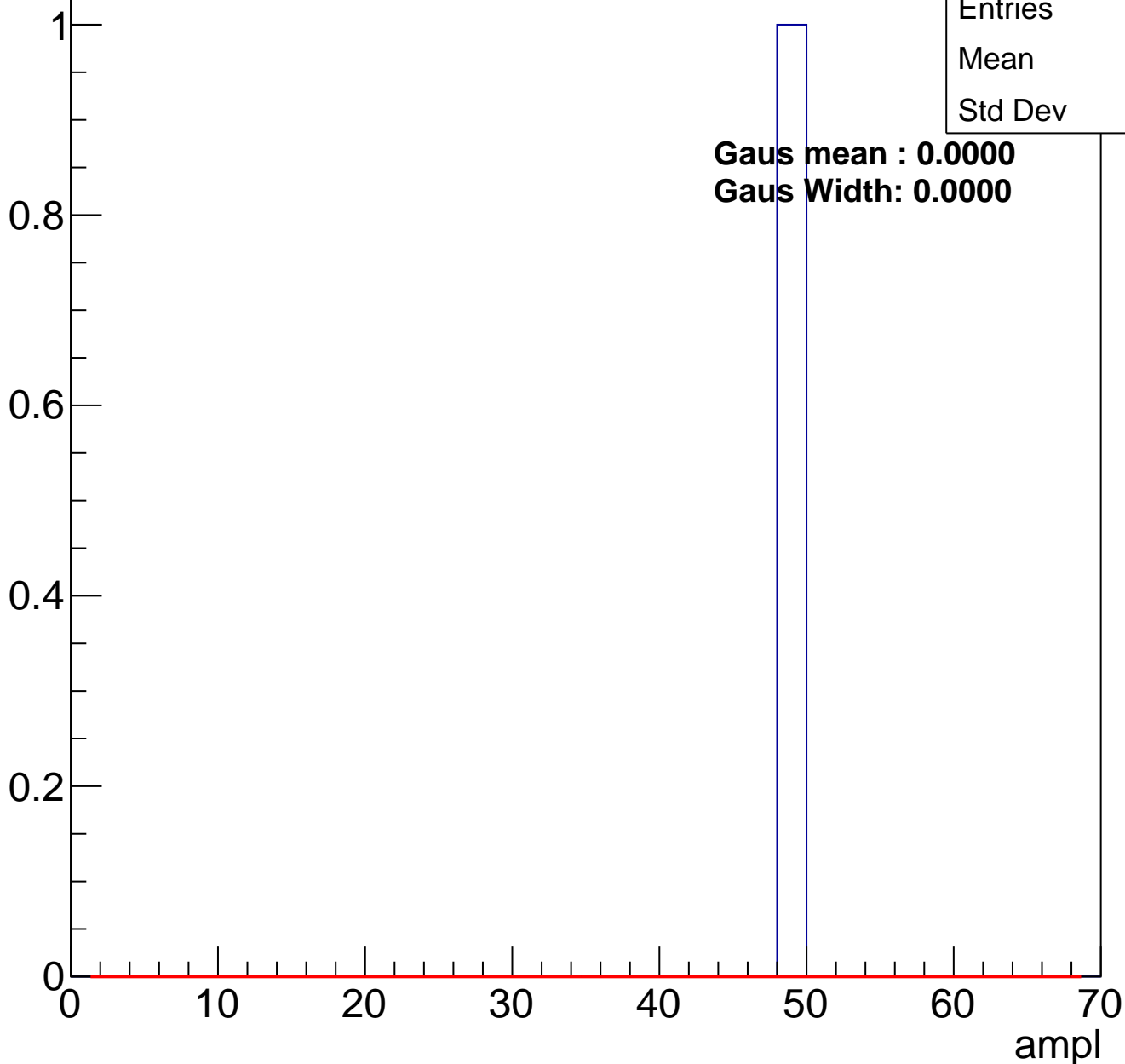
Entry



B0L100S, U12-ch119, adc1

calib_packv5_042523_0143.root, FC#6, port A1

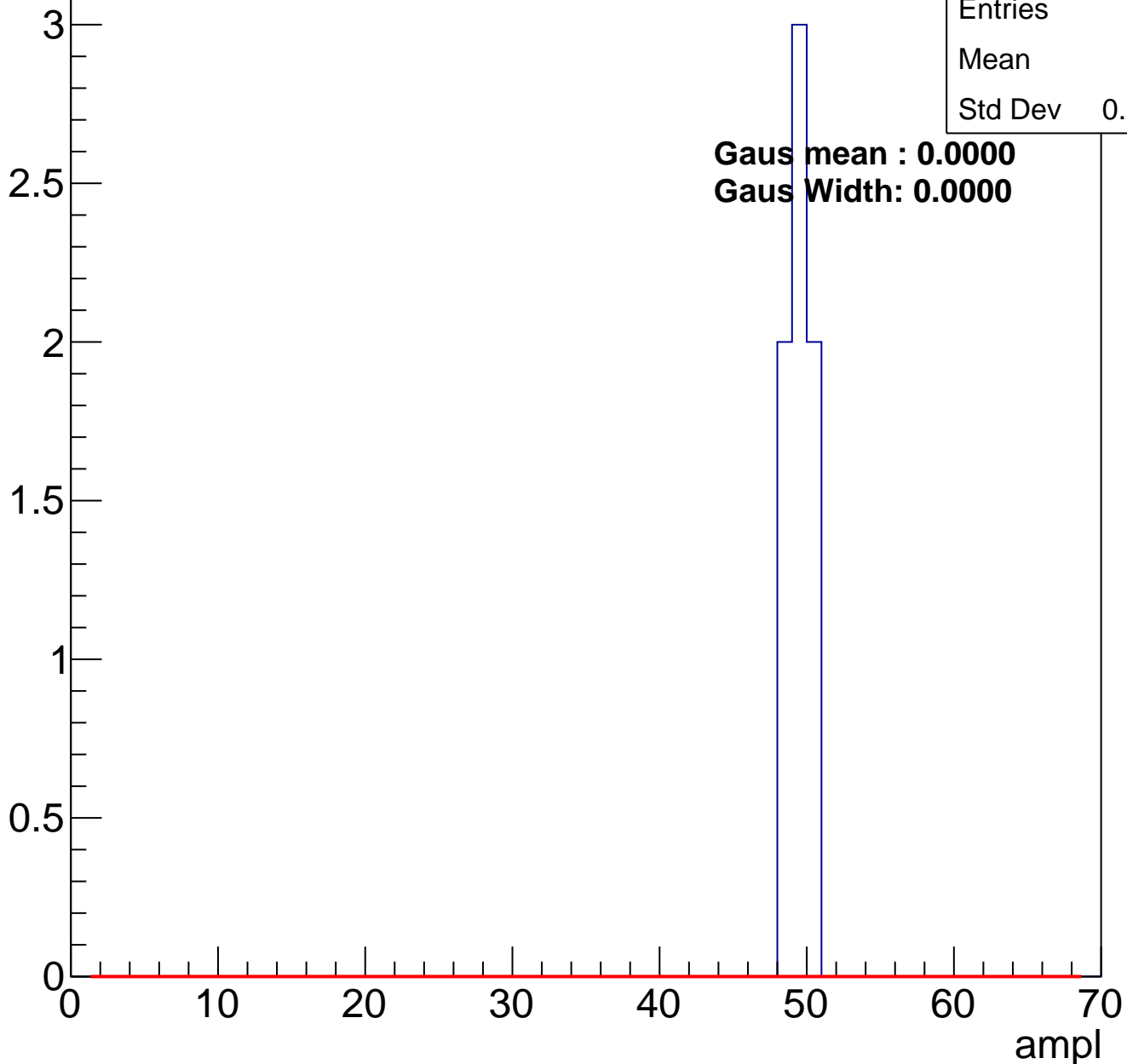
Entry



B0L100S, U12-ch119, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

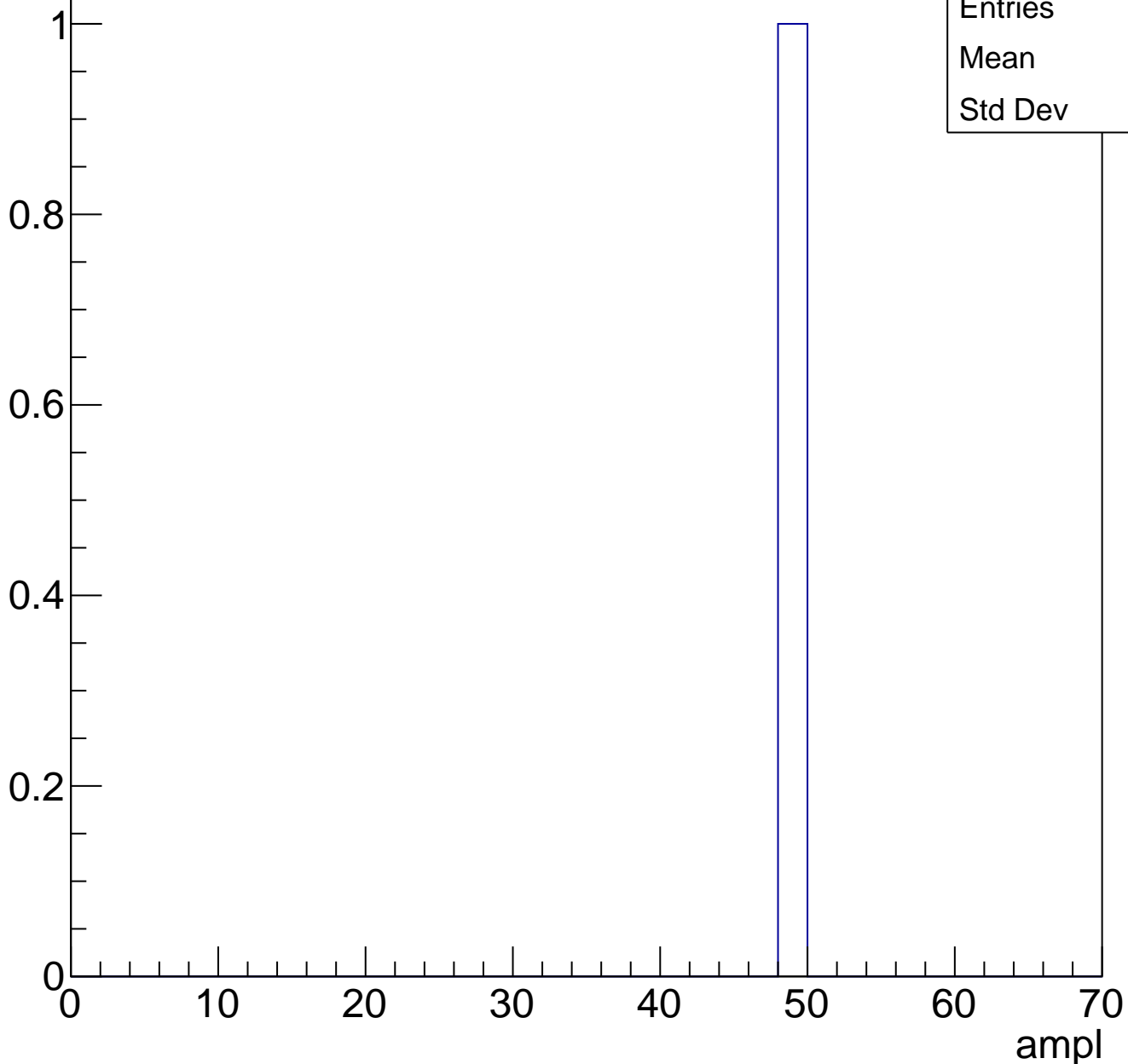


Entries	7
Mean	49
Std Dev	0.7559

B0L100S, U12-ch119, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	2
Mean	48.5
Std Dev	0.5

B0L100S, U12-ch119, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch119, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch119, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch119, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch120, adc0

calib_packv5_042523_0143.root, FC#6, port A1

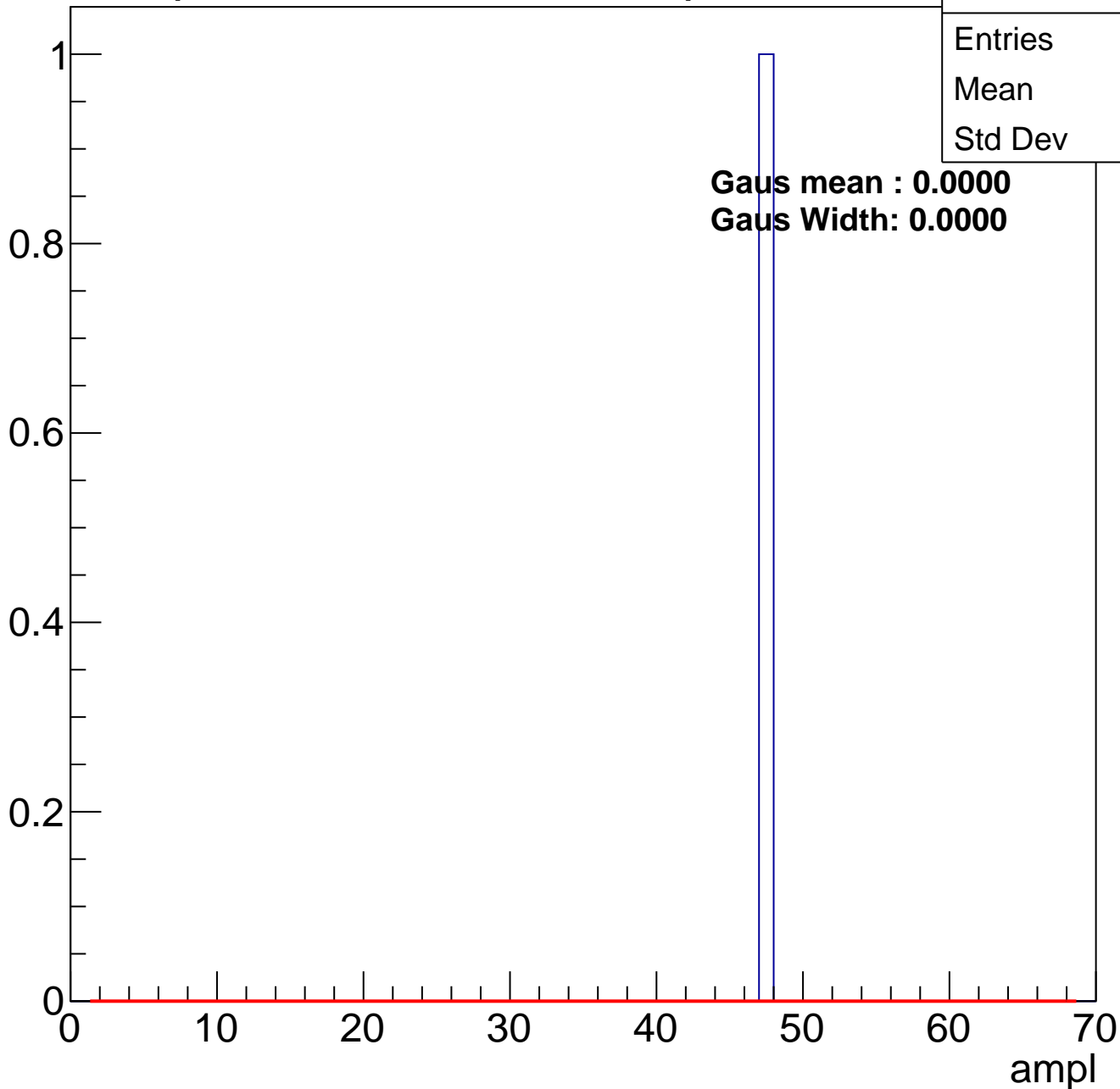
Entry



B0L100S, U12-ch120, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch120, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

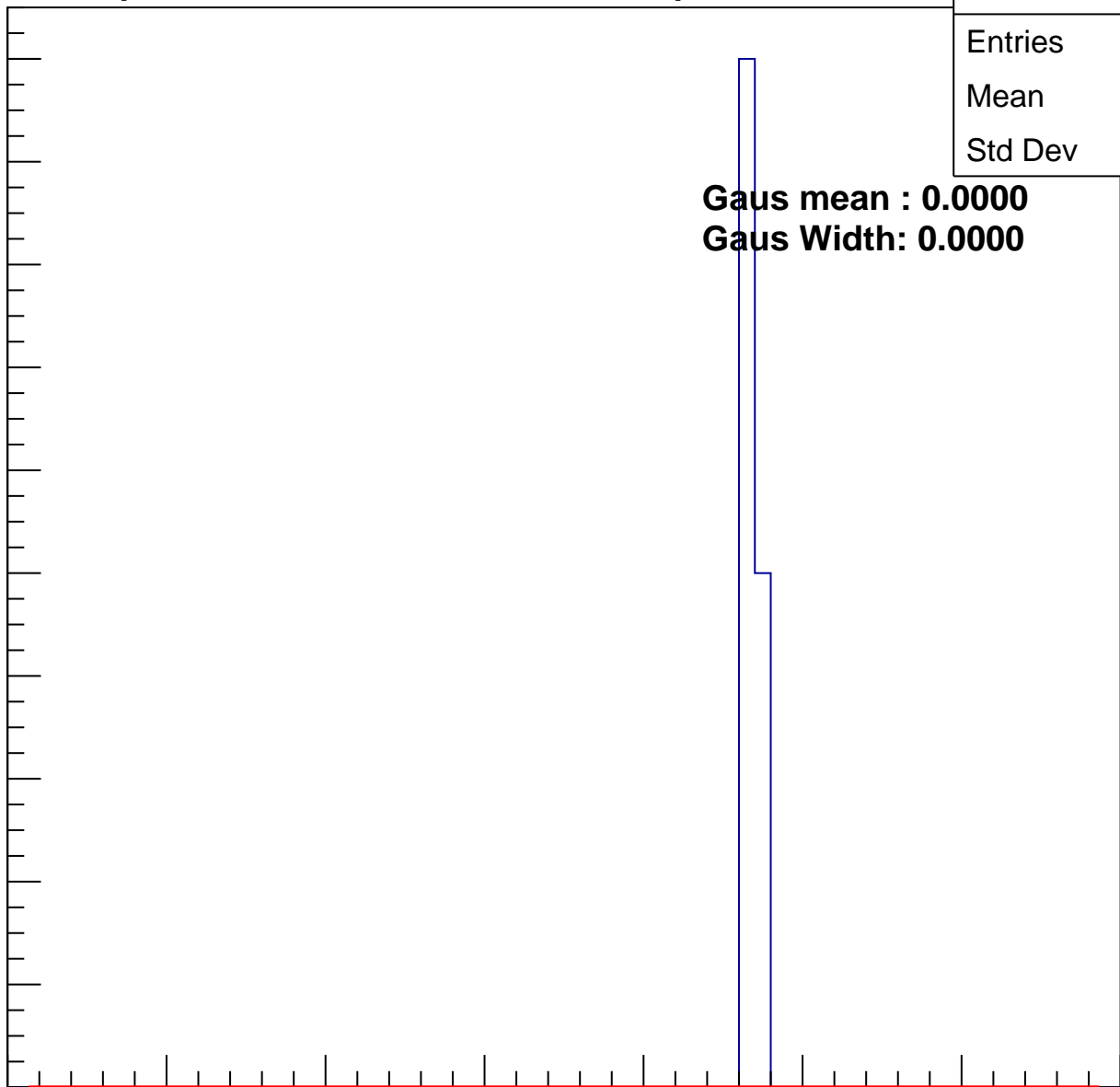
Entries	3
Mean	46.33
Std Dev	0.4714

Gaus mean : 0.0000

Gaus Width: 0.0000

0 10 20 30 40 50 60 70

ampl



B0L100S, U12-ch120, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch120, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch120, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch120, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch120, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	1
Mean	0
Std Dev	0

B0L100S, U12-ch121, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch121, adc1

calib_packv5_042523_0143.root, FC#6, port A1

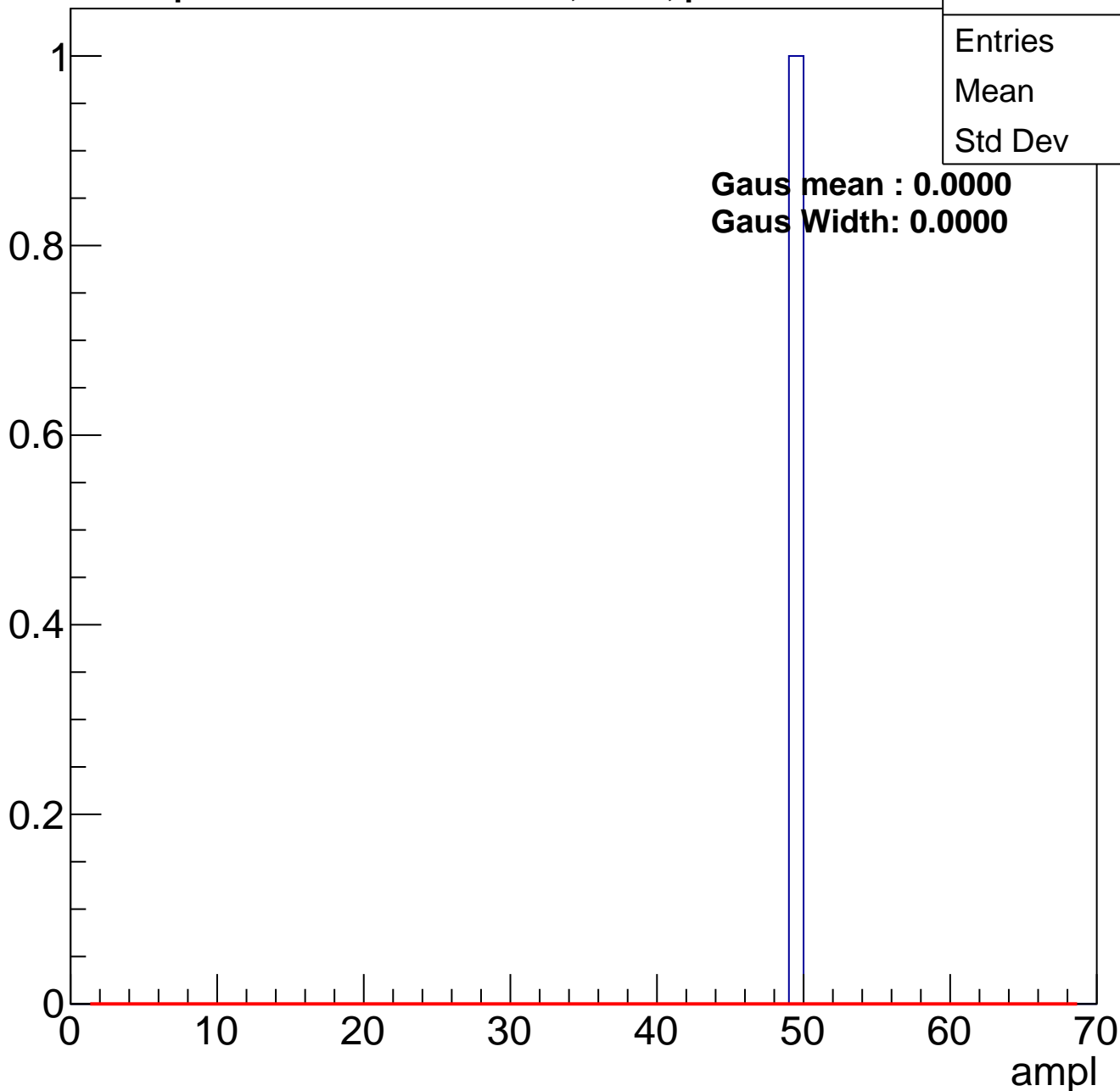
Entry



B0L100S, U12-ch121, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch121, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch121, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch121, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch121, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch121, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch122, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch122, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch122, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch122, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch122, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch122, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch122, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch122, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch123, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch123, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch123, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch123, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch123, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch123, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch123, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry

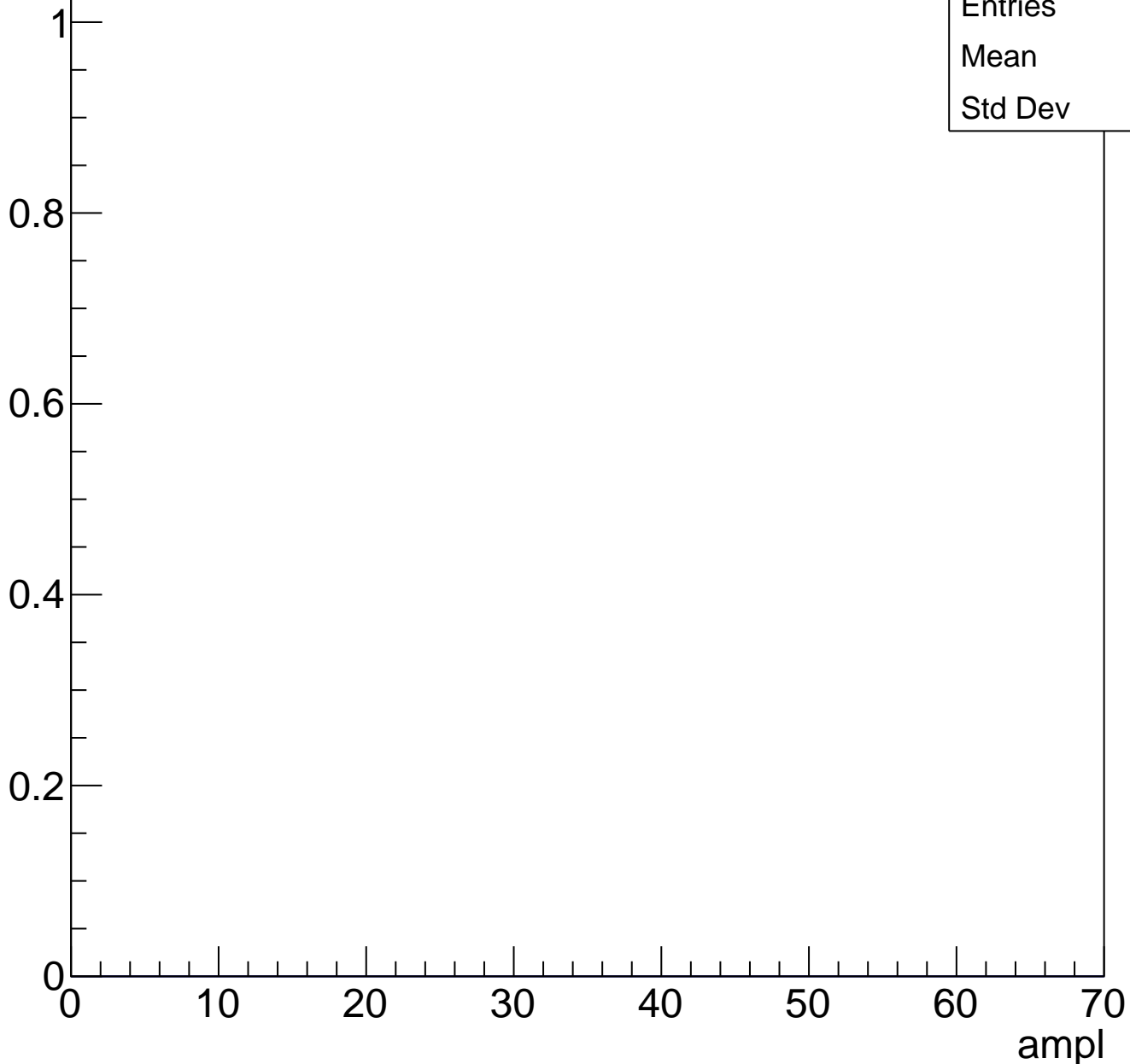


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch123, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch124, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch124, adc1

calib_packv5_042523_0143.root, FC#6, port A1

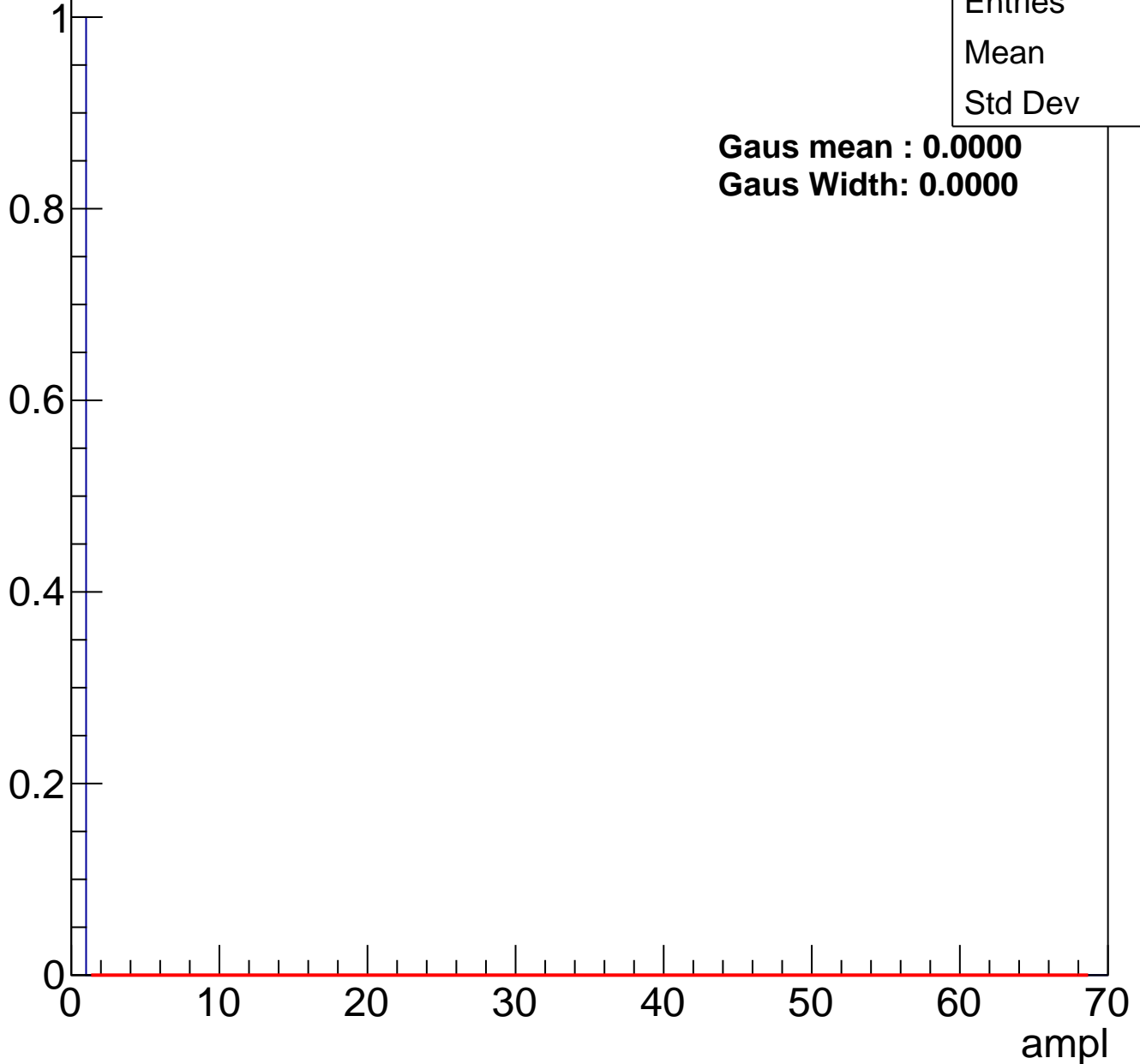
Entry



B0L100S, U12-ch124, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	1
Mean	0
Std Dev	0

B0L100S, U12-ch124, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch124, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch124, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry

1
0.8
0.6
0.4
0.2
0

Entries	1
Mean	30
Std Dev	0

ampl



B0L100S, U12-ch124, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch124, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch125, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Gaus mean : 0.0000

Gaus Width: 0.0000

Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch125, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch125, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch125, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch125, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch125, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch125, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch125, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch126, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch126, adc1

calib_packv5_042523_0143.root, FC#6, port A1

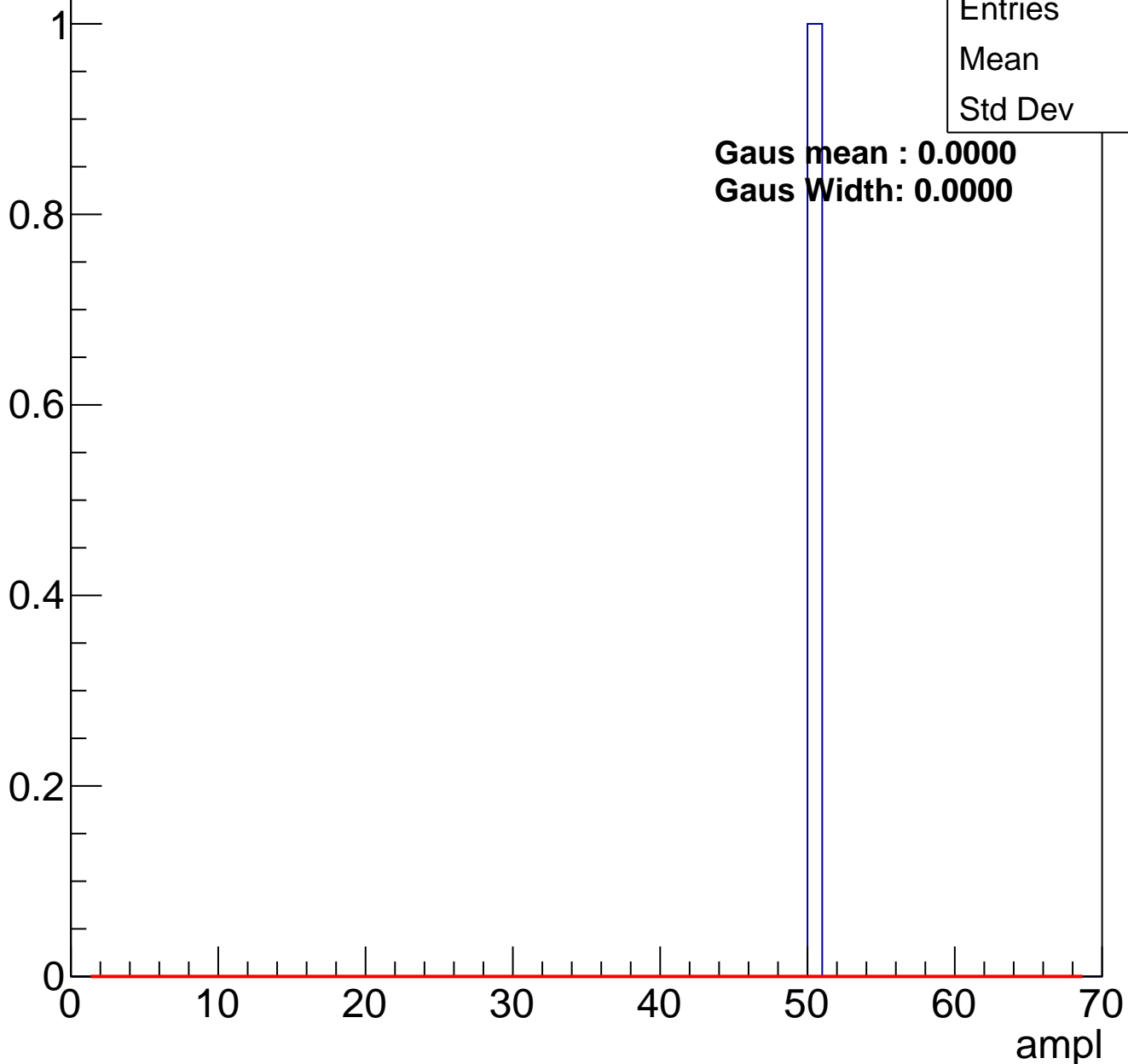
Entry



B0L100S, U12-ch126, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	1
Mean	50
Std Dev	0

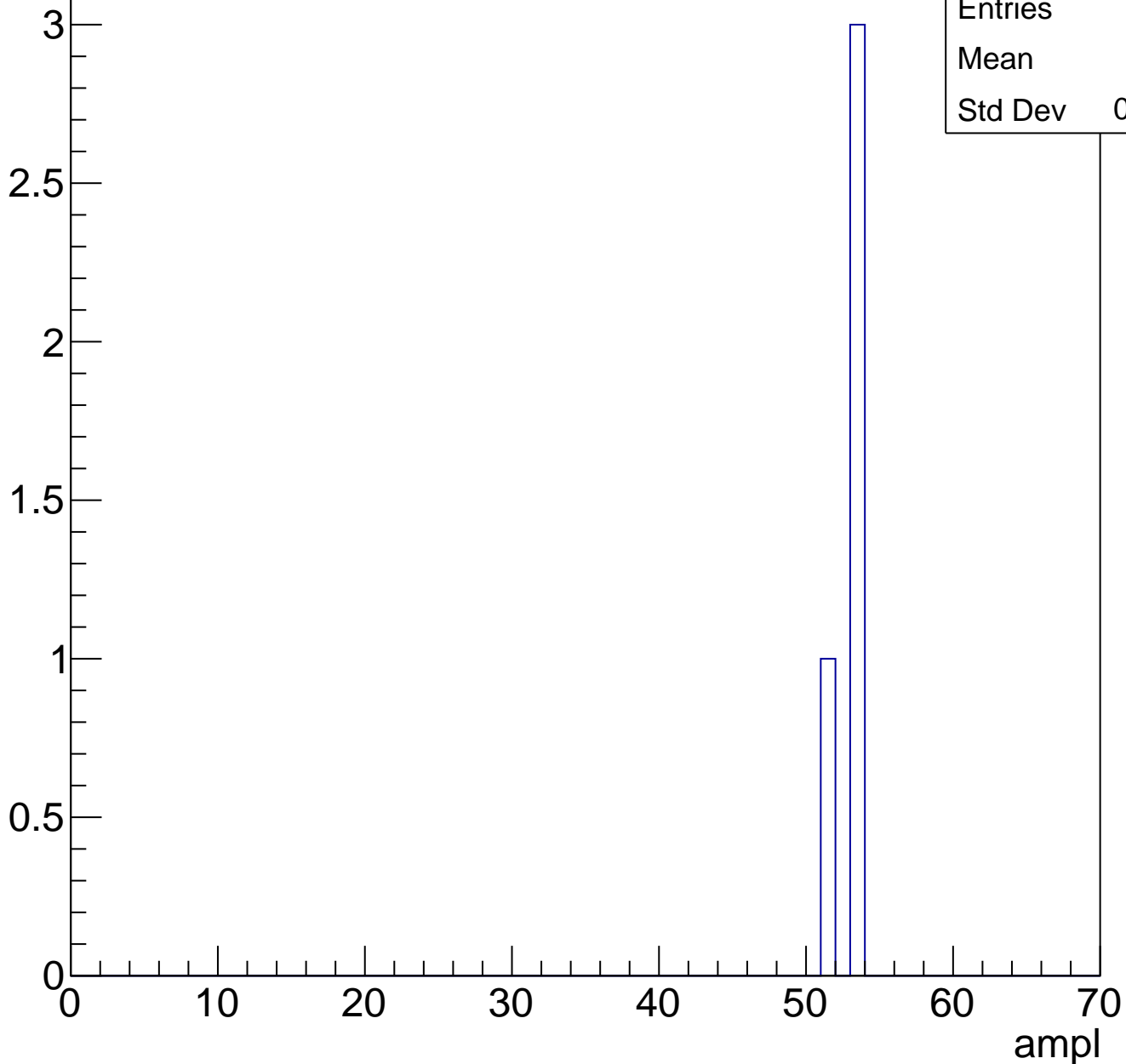
Gaus mean : 0.0000

Gaus Width: 0.0000

B0L100S, U12-ch126, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch126, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch126, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch126, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch126, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry

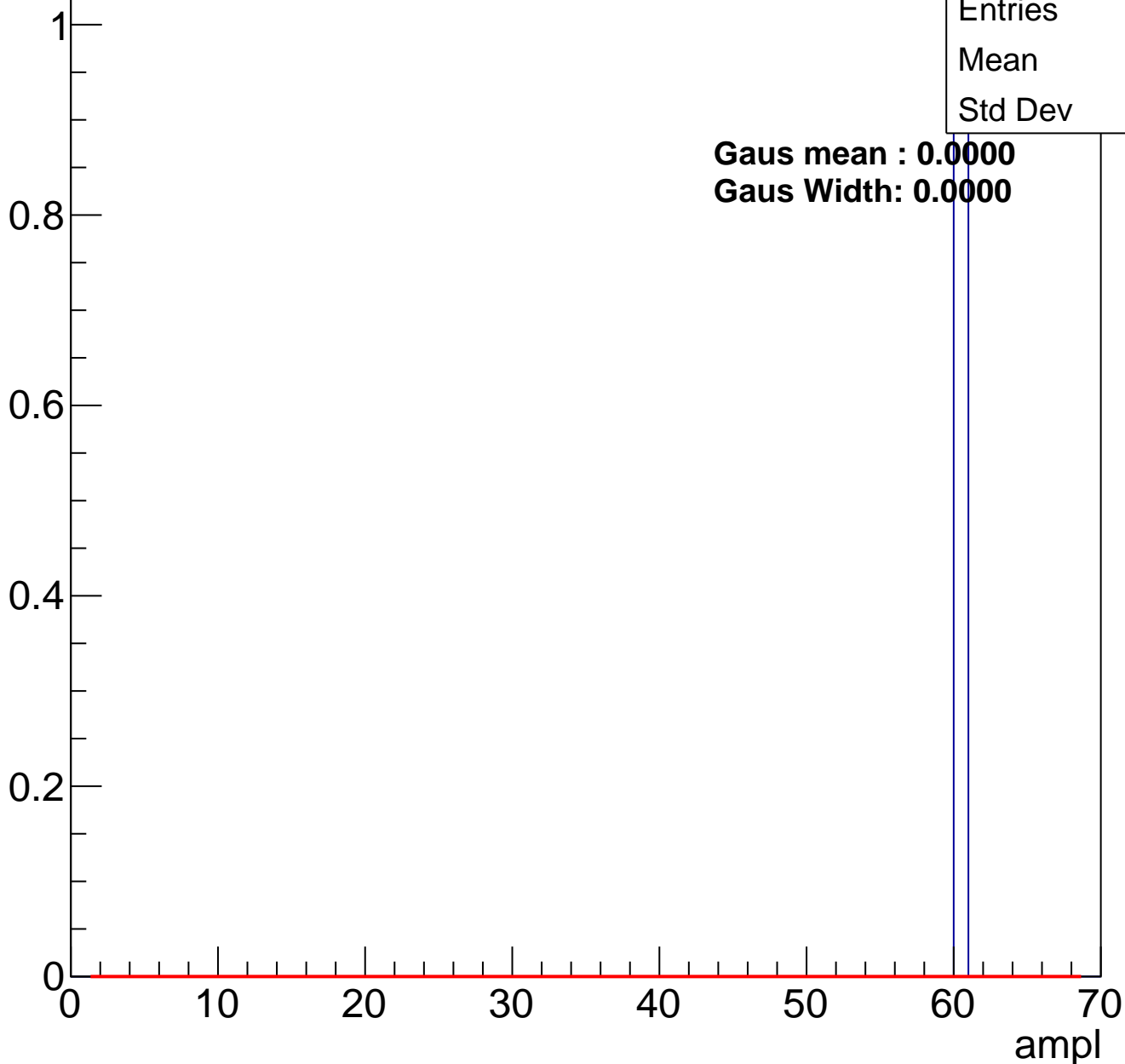


Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch127, adc0

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch127, adc1

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch127, adc2

calib_packv5_042523_0143.root, FC#6, port A1

Entry



B0L100S, U12-ch127, adc3

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch127, adc4

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch127, adc5

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch127, adc6

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	0
Mean	0
Std Dev	0

B0L100S, U12-ch127, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry



Entries	1
Mean	0
Std Dev	0

B0L100S, U12-ch127, adc7

calib_packv5_042523_0143.root, FC#6, port A1

Entry

