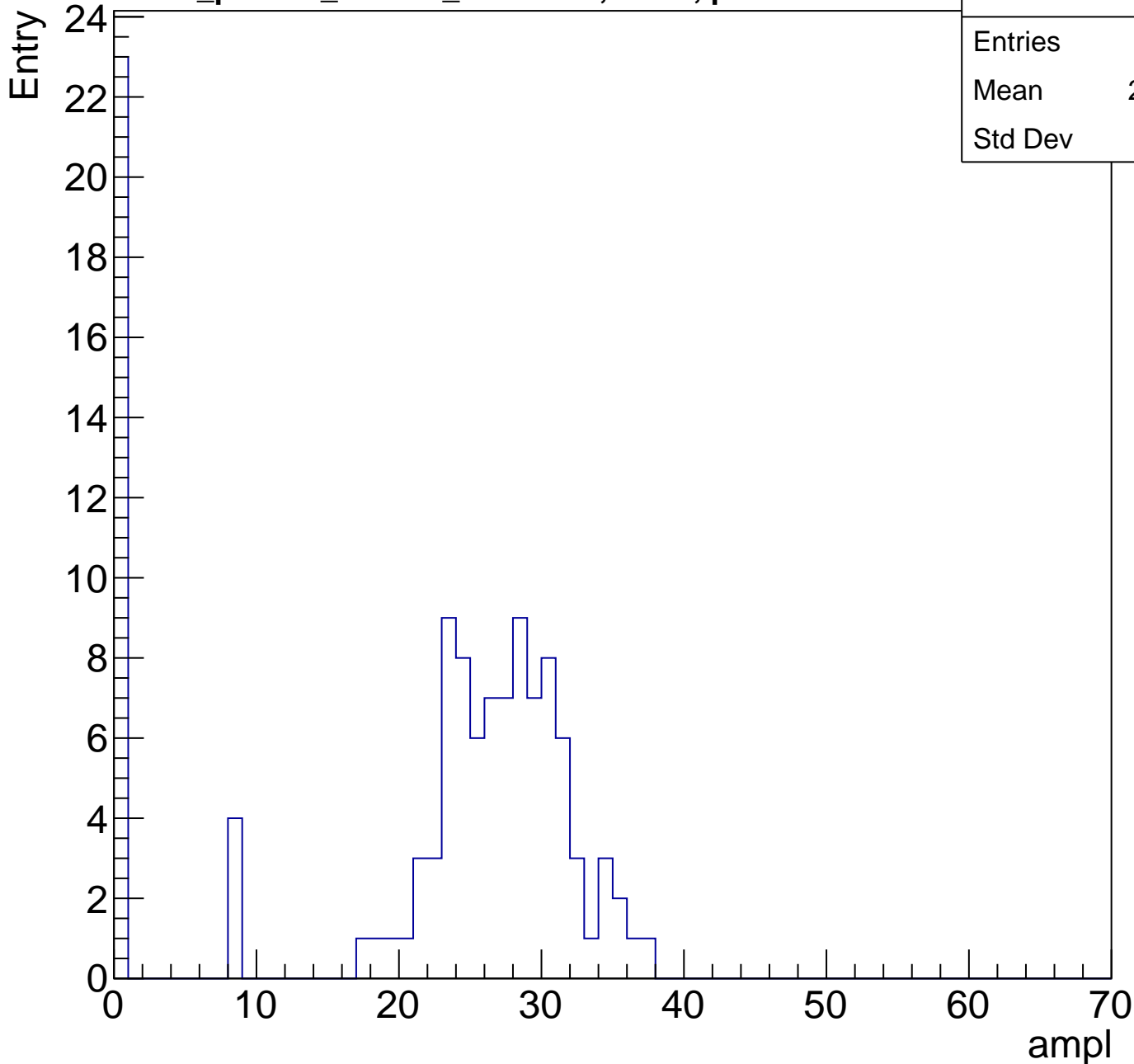


B1L103S, U11-ch0, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	115
Mean	20.96
Std Dev	11.61

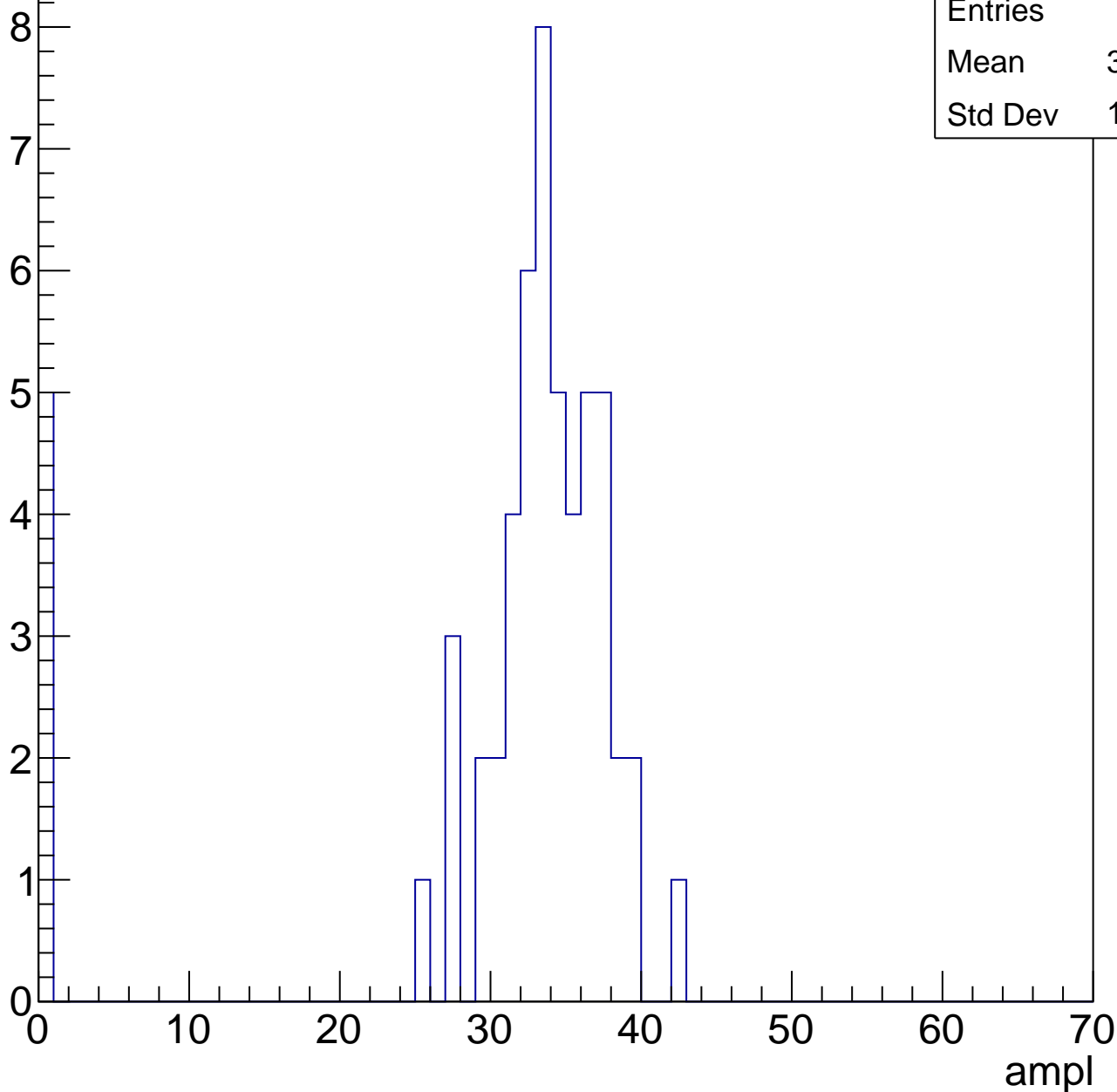


B1L103S, U11-ch0, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	30.45
Std Dev	10.16



B1L103S, U11-ch0, adc2

calib_packv5_041523_1651.root, FC#0, port C2

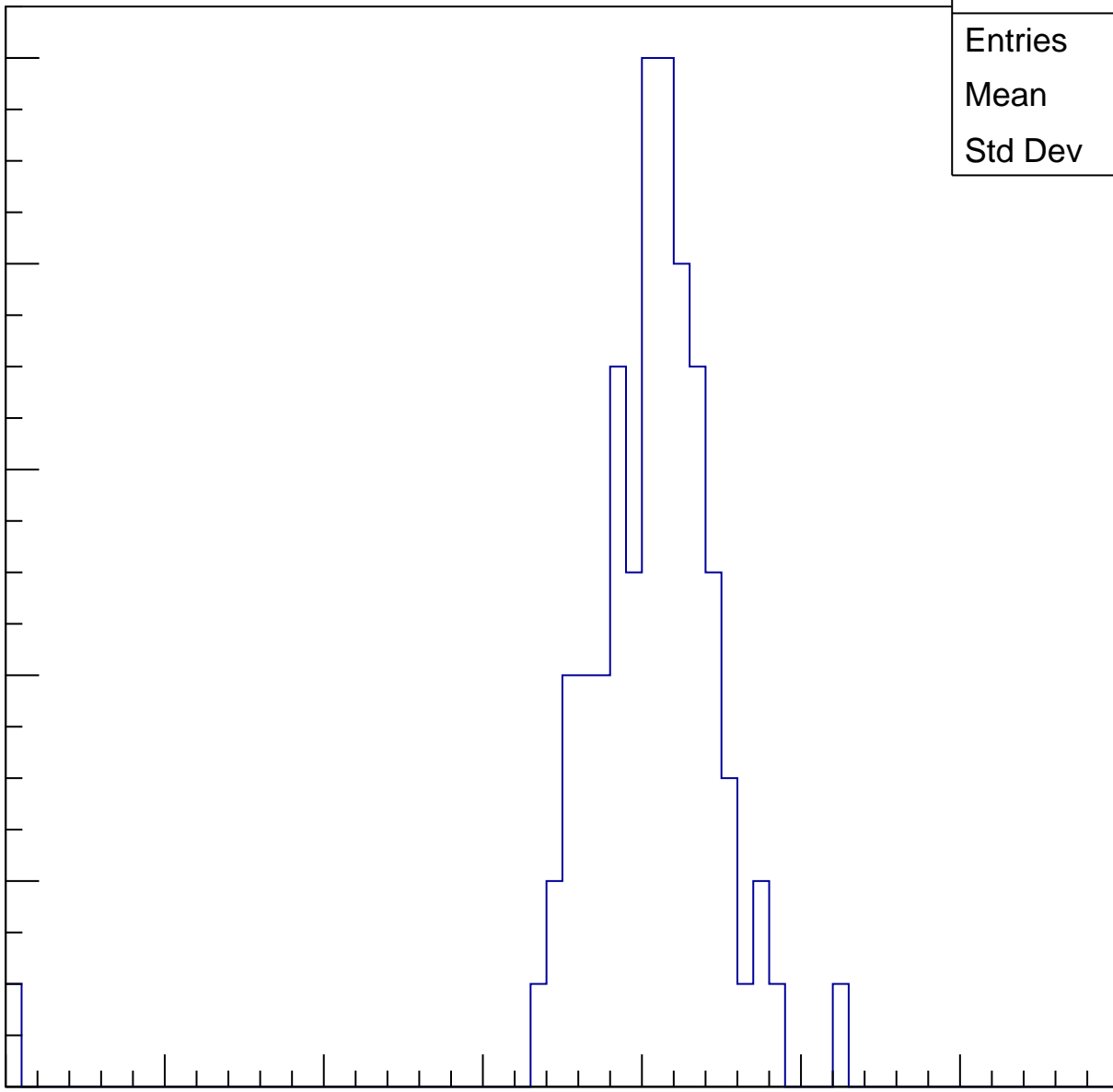
Entries	76
Mean	39.95
Std Dev	5.799

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

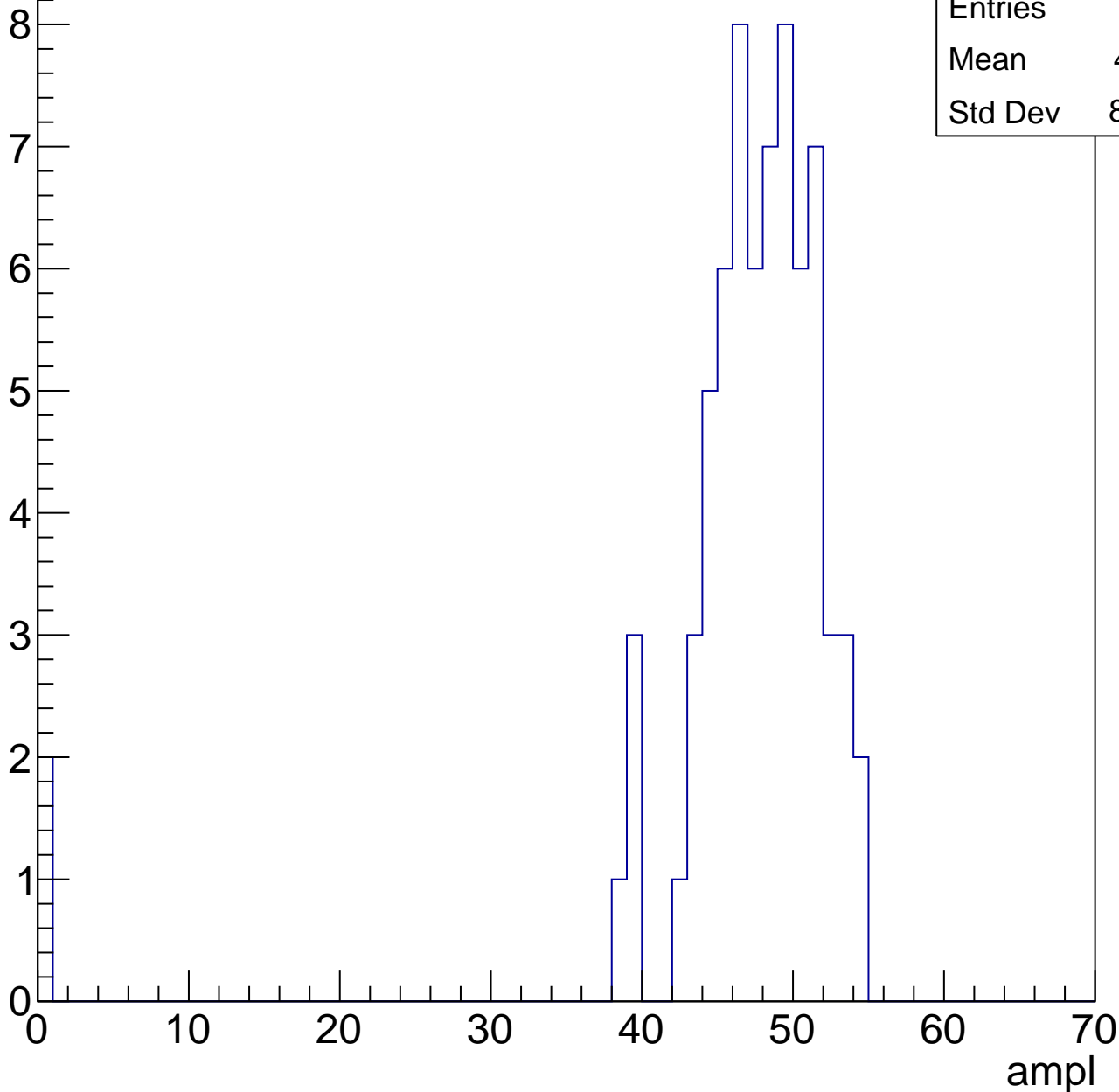


B1L103S, U11-ch0, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	46.11
Std Dev	8.616

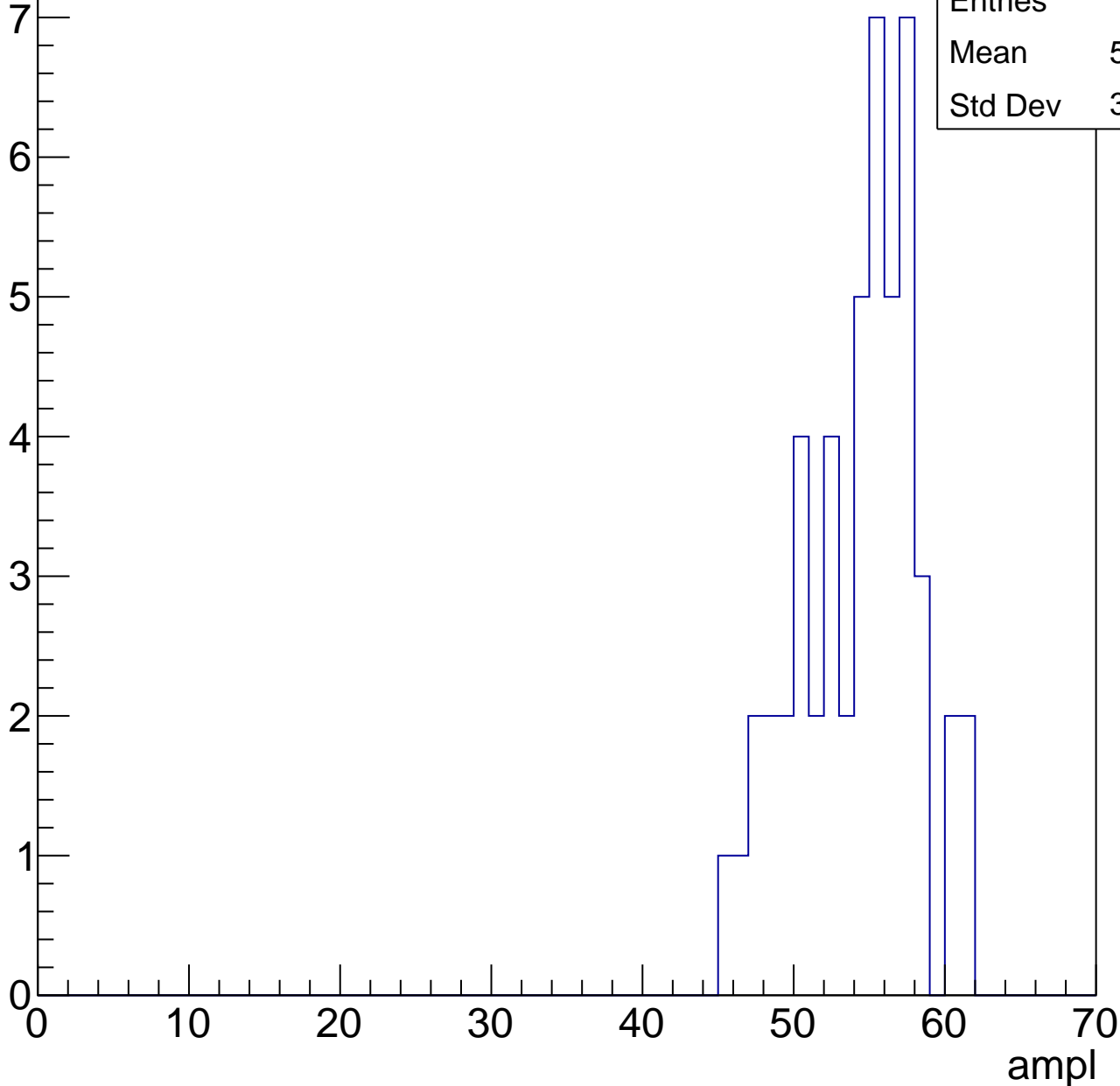


B1L103S, U11-ch0, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

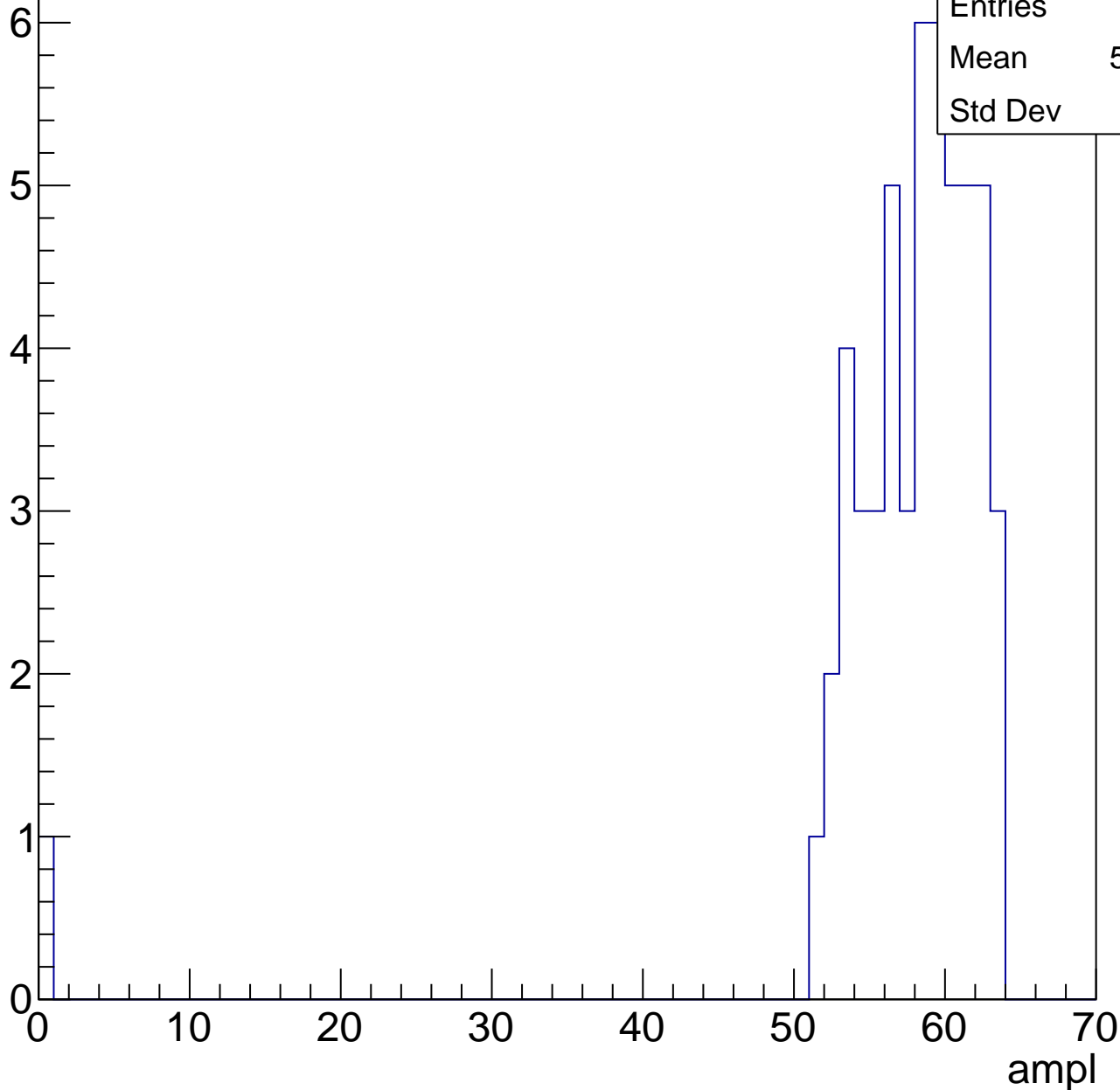
Entries	51
Mean	53.82
Std Dev	3.889



B1L103S, U11-ch0, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

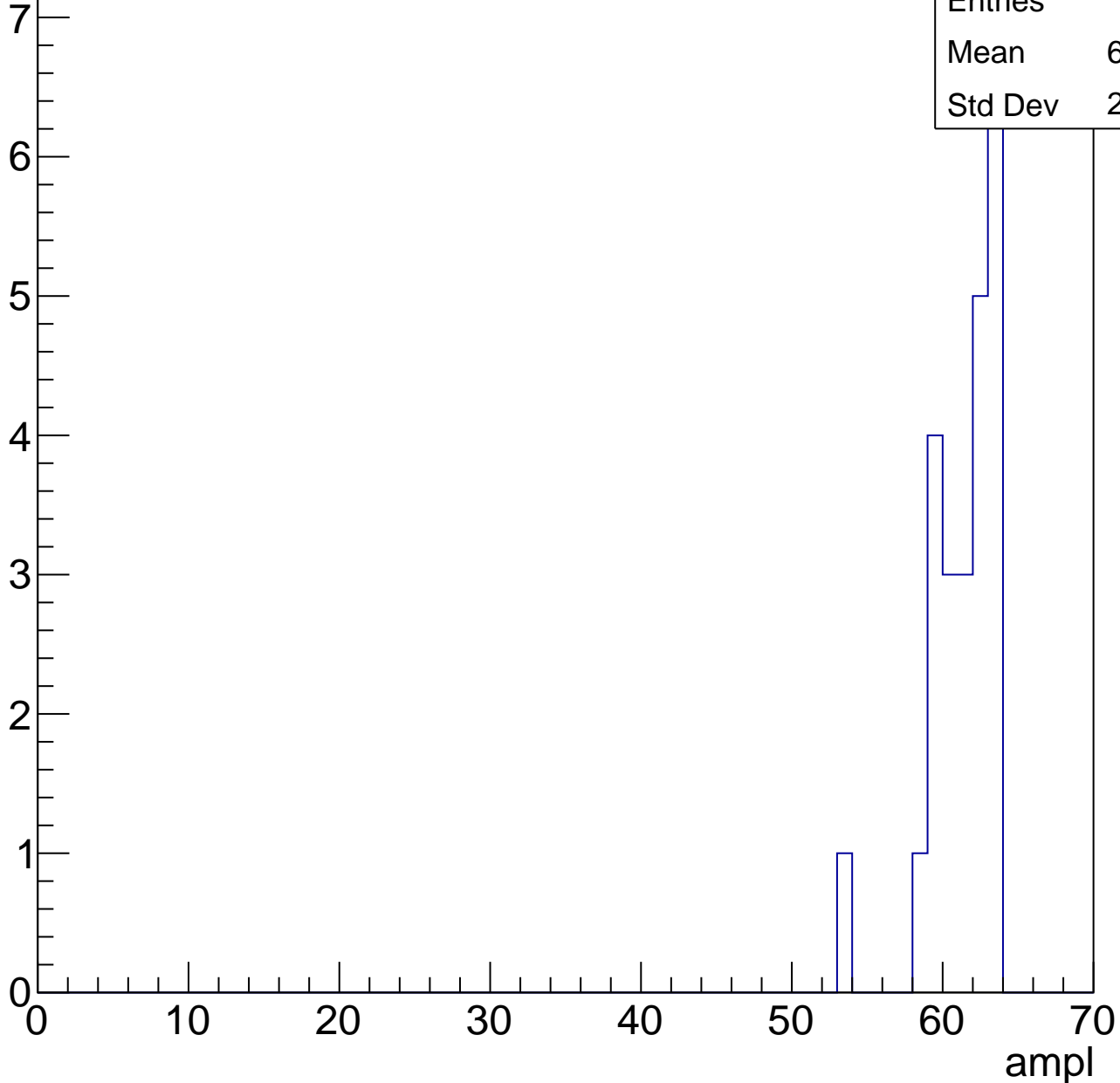


B1L103S, U11-ch0, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	24
Mean	60.88
Std Dev	2.279



B1L103S, U11-ch0, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

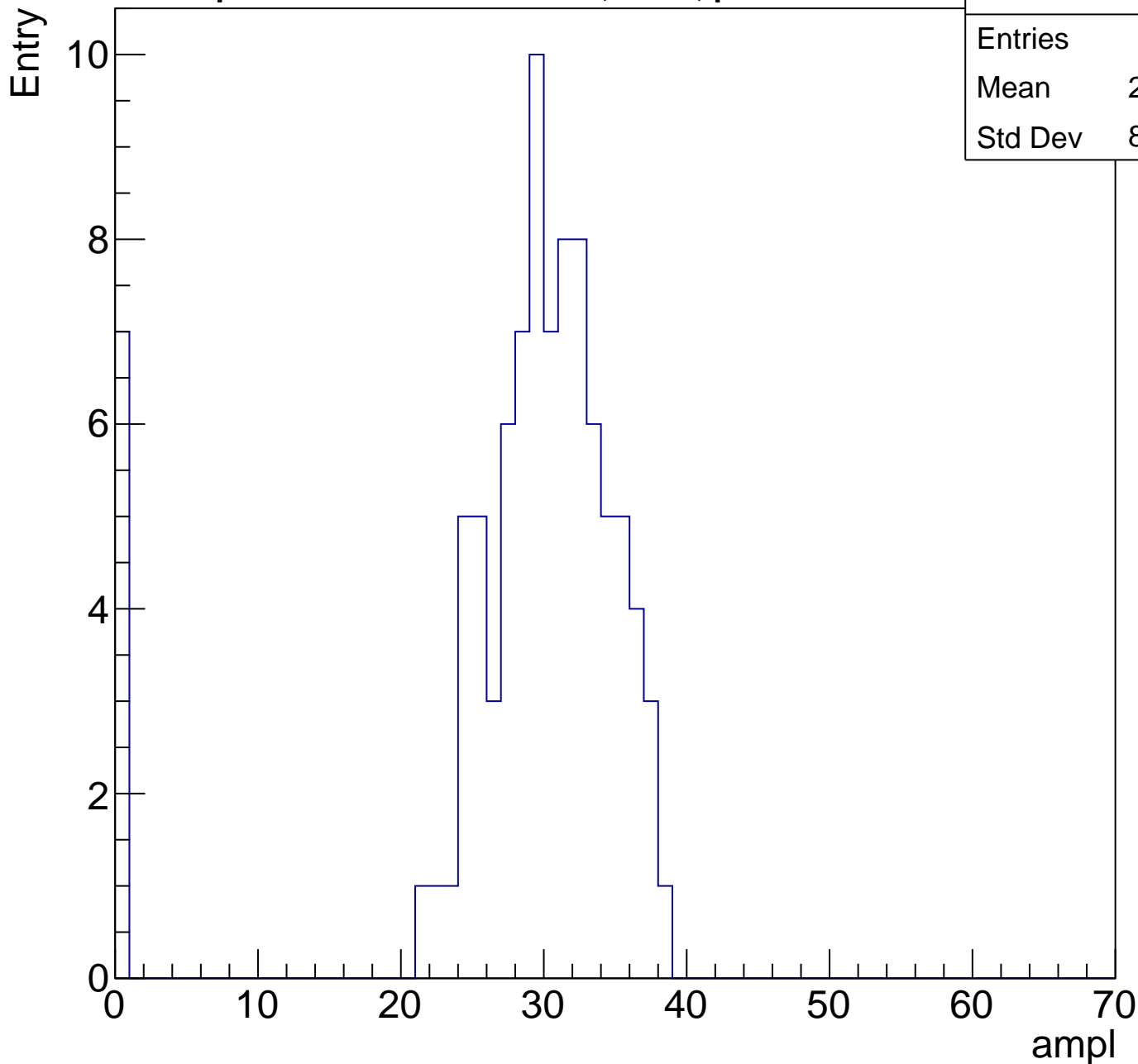
Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U11-ch1, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	93
Mean	27.82
Std Dev	8.768

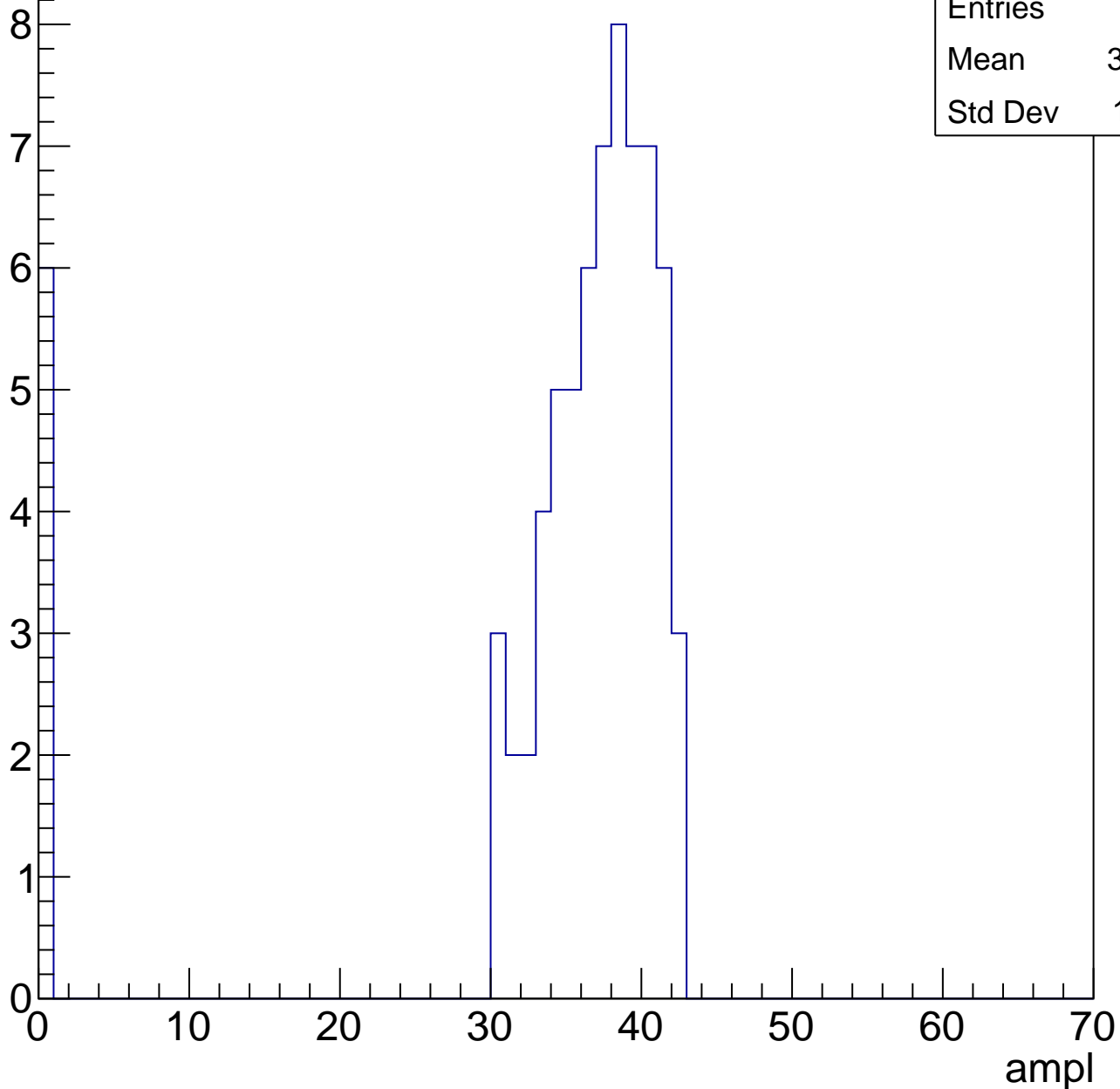


B1L103S, U11-ch1, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	33.76
Std Dev	10.71

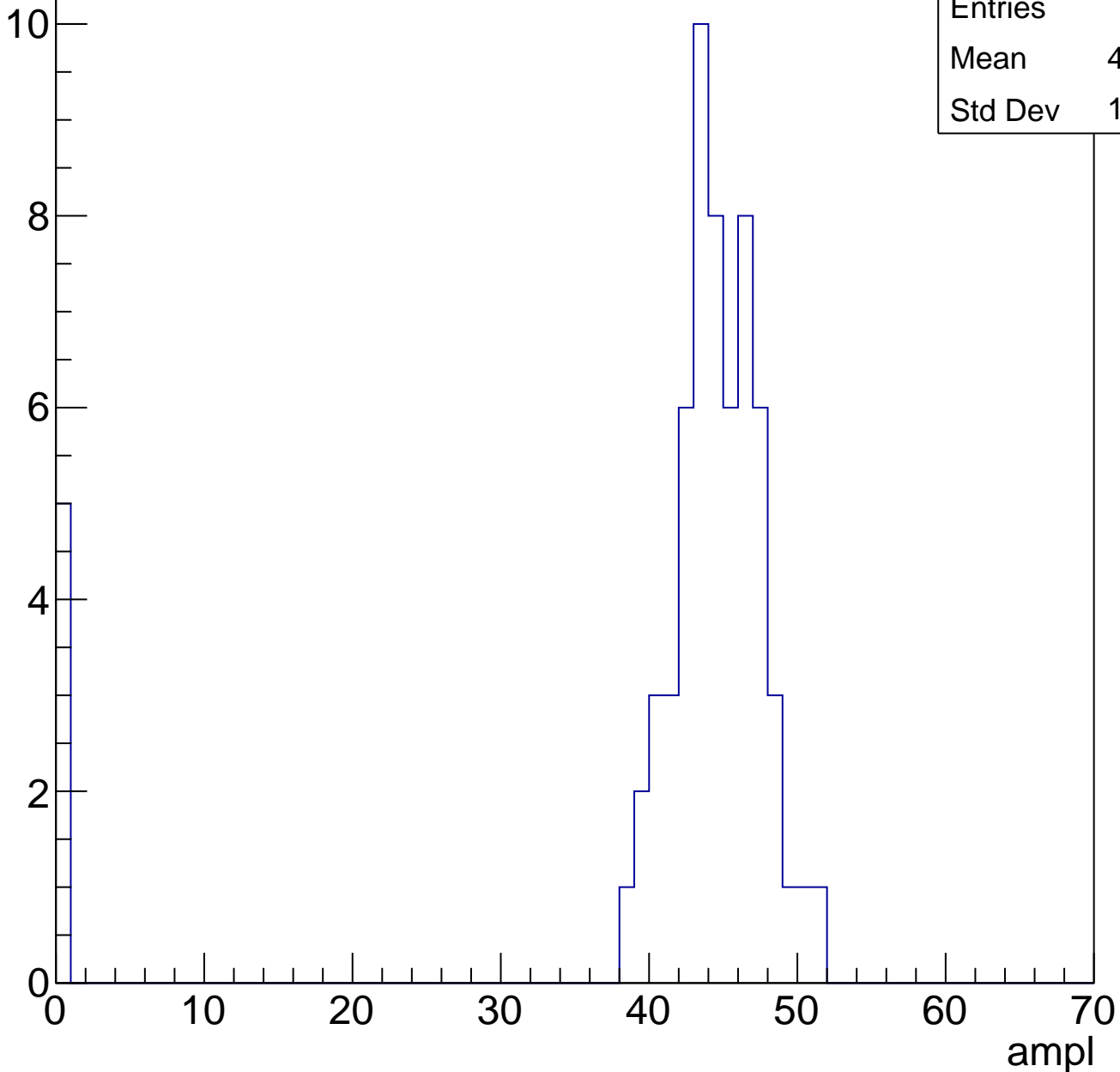


B1L103S, U11-ch1, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	64
Mean	40.73
Std Dev	12.15

Entry

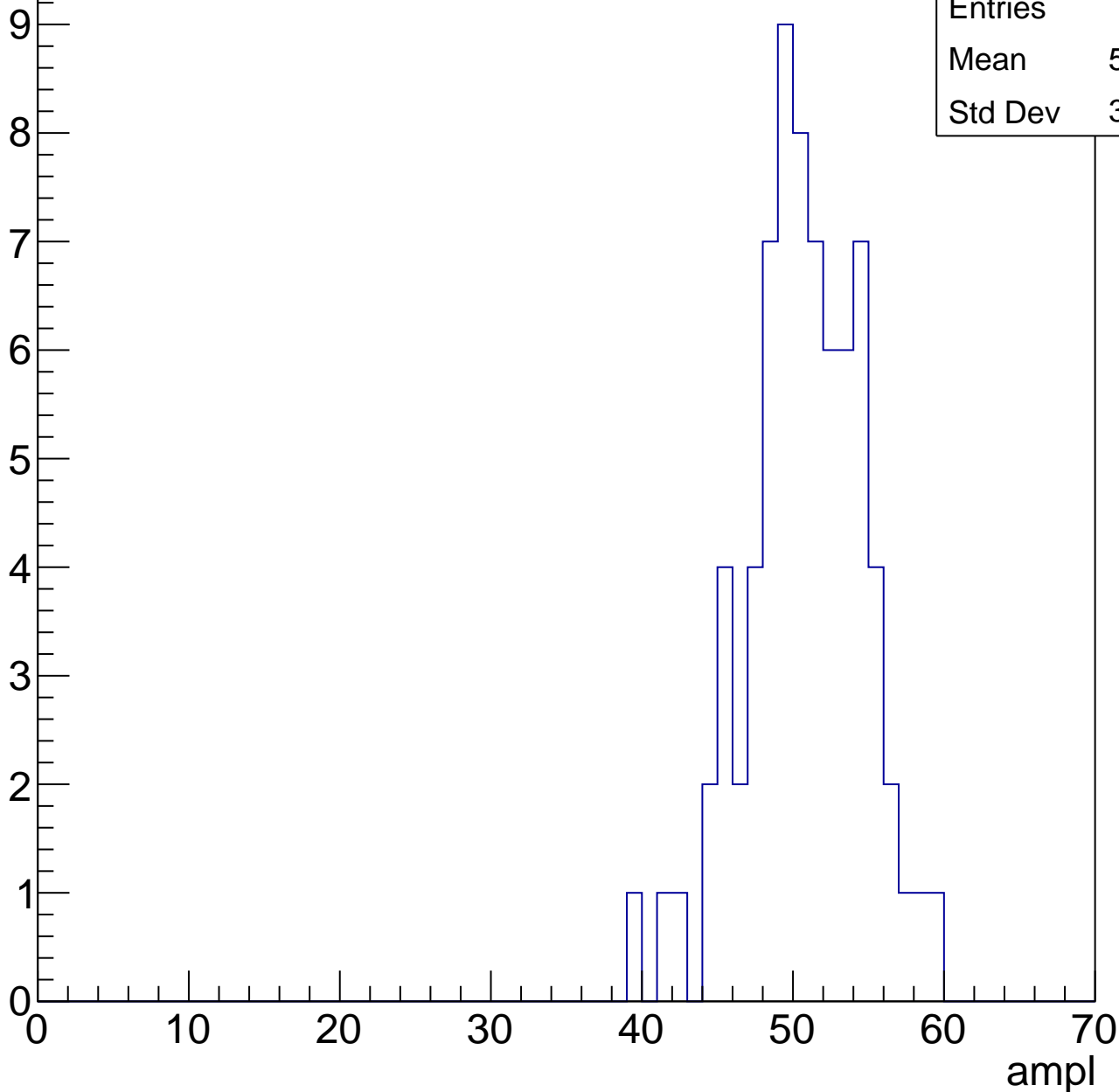


B1L103S, U11-ch1, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	50.24
Std Dev	3.858

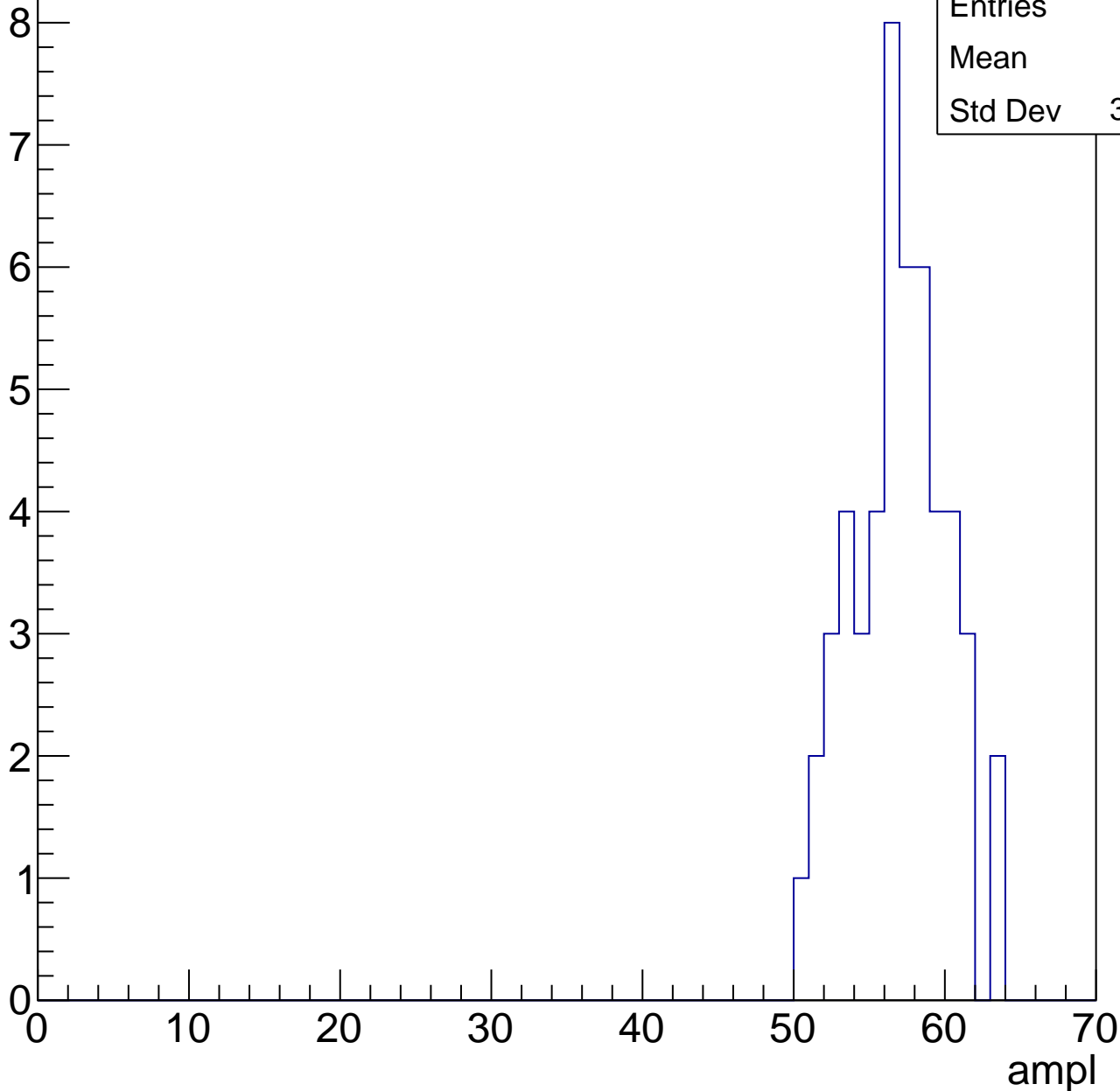


B1L103S, U11-ch1, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	56.5
Std Dev	3.087

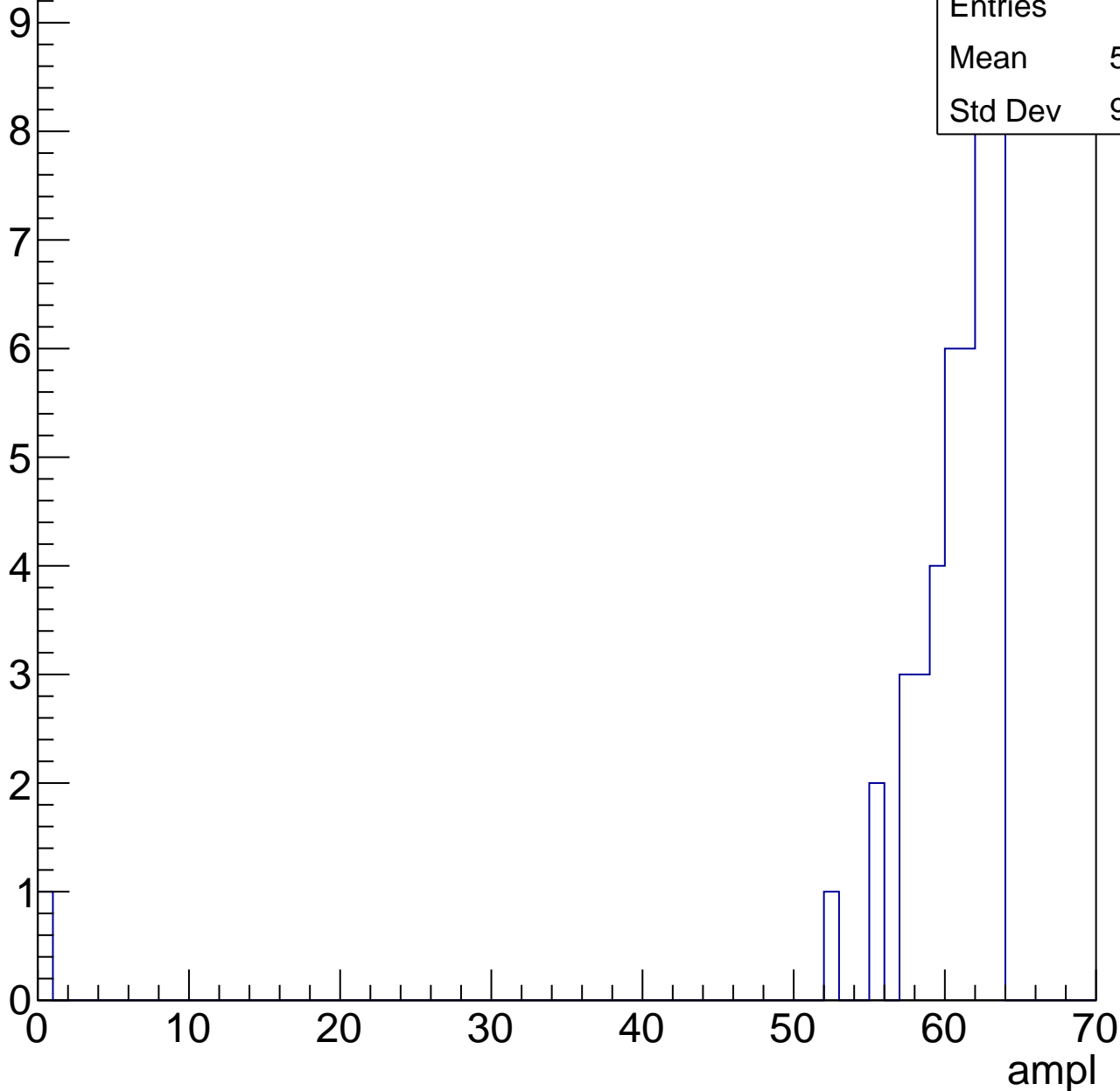


B1L103S, U11-ch1, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	43
Mean	58.86
Std Dev	9.419



B1L103S, U11-ch1, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

1
0.8
0.6
0.4
0.2
0

Entries	3
Mean	60.67
Std Dev	1.247

ampl

B1L103S, U11-ch1, adc7

calib_packv5_041523_1651.root, FC#0, port C2

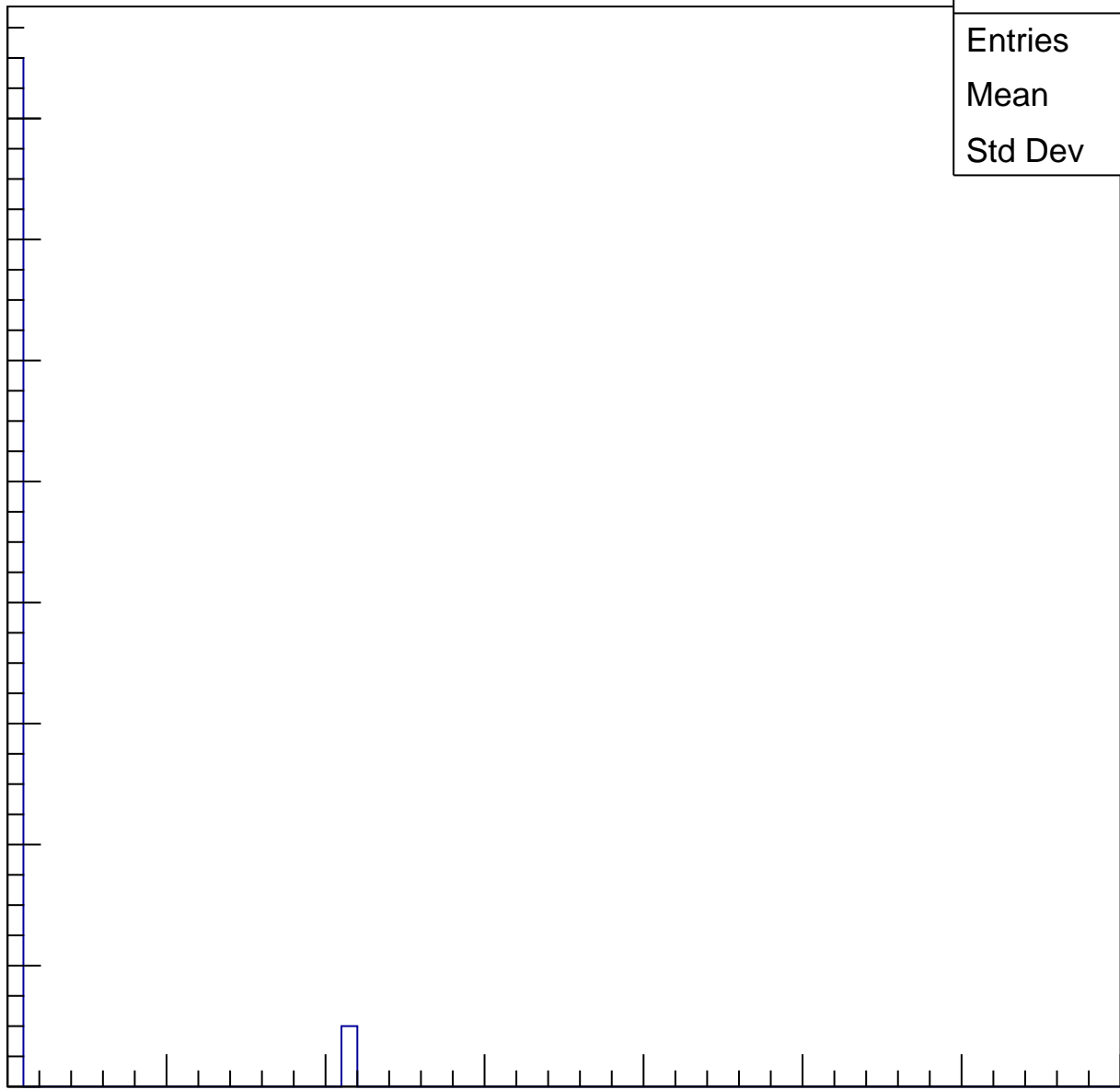
Entries	18
Mean	1.167
Std Dev	4.81

Entry

16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

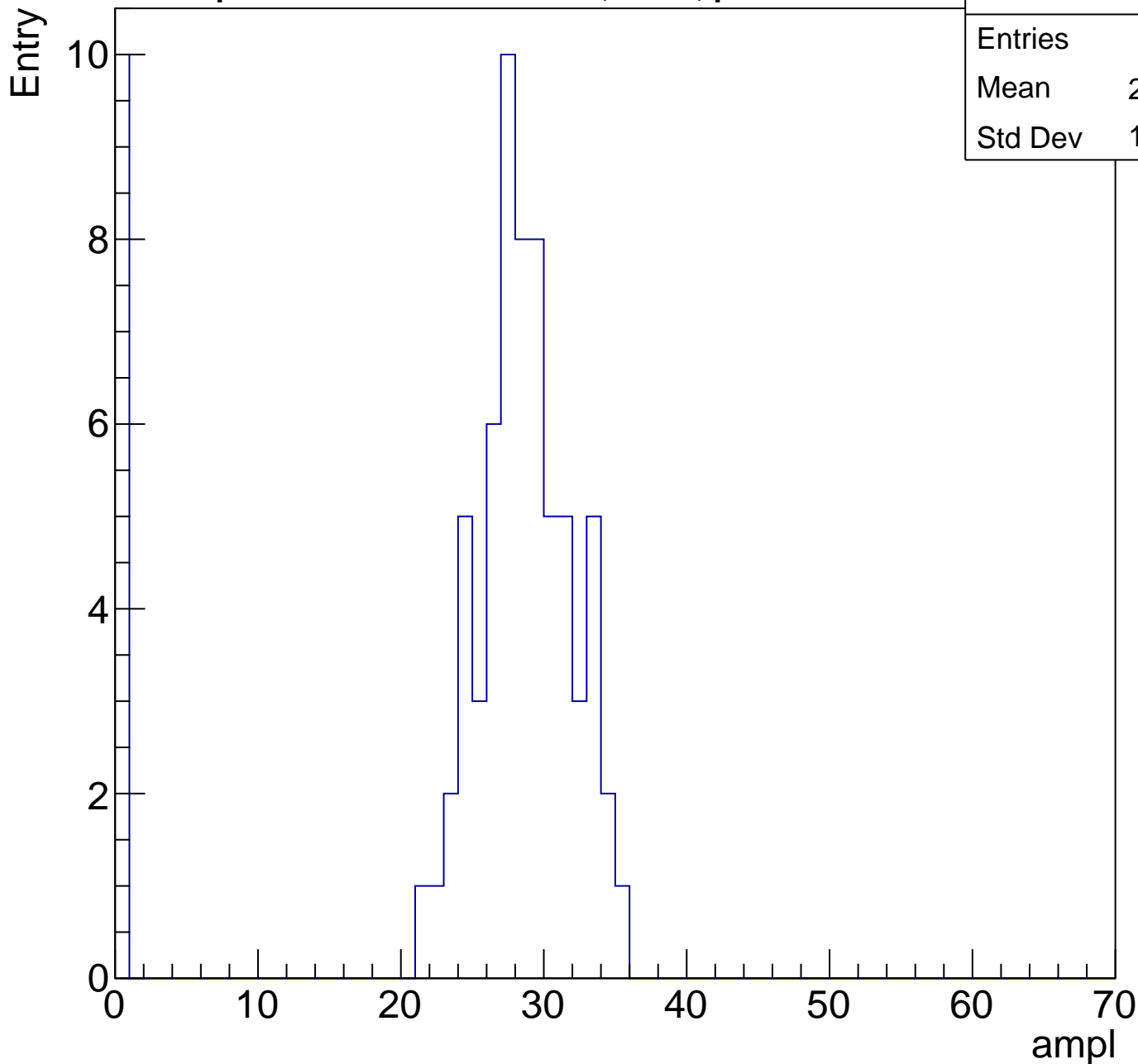
ampl



B1L103S, U11-ch2, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	24.47
Std Dev	10.03



B1L103S, U11-ch2, adc1

calib_packv5_041523_1651.root, FC#0, port C2

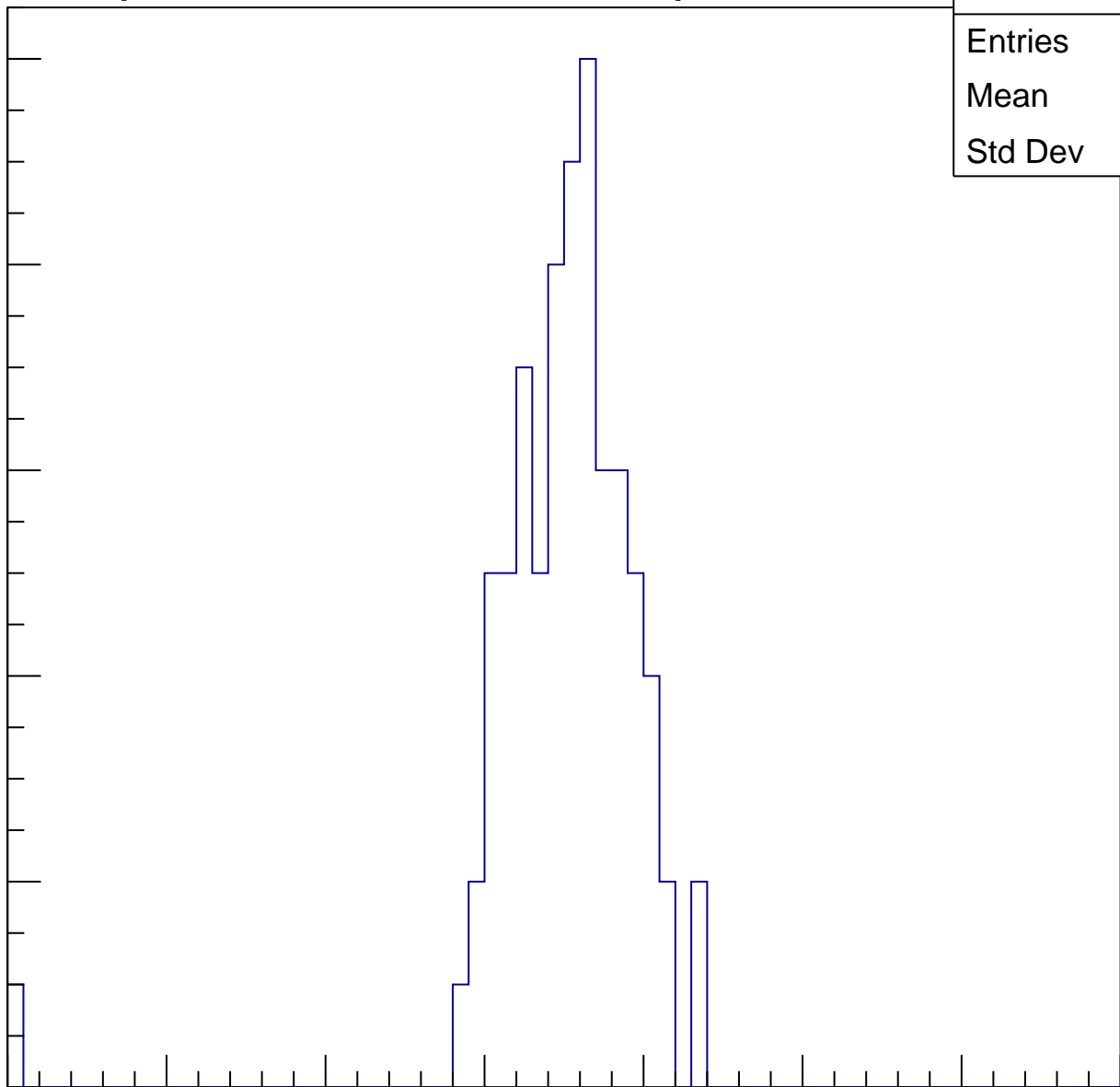
Entries	78
Mean	34.62
Std Dev	5.187

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

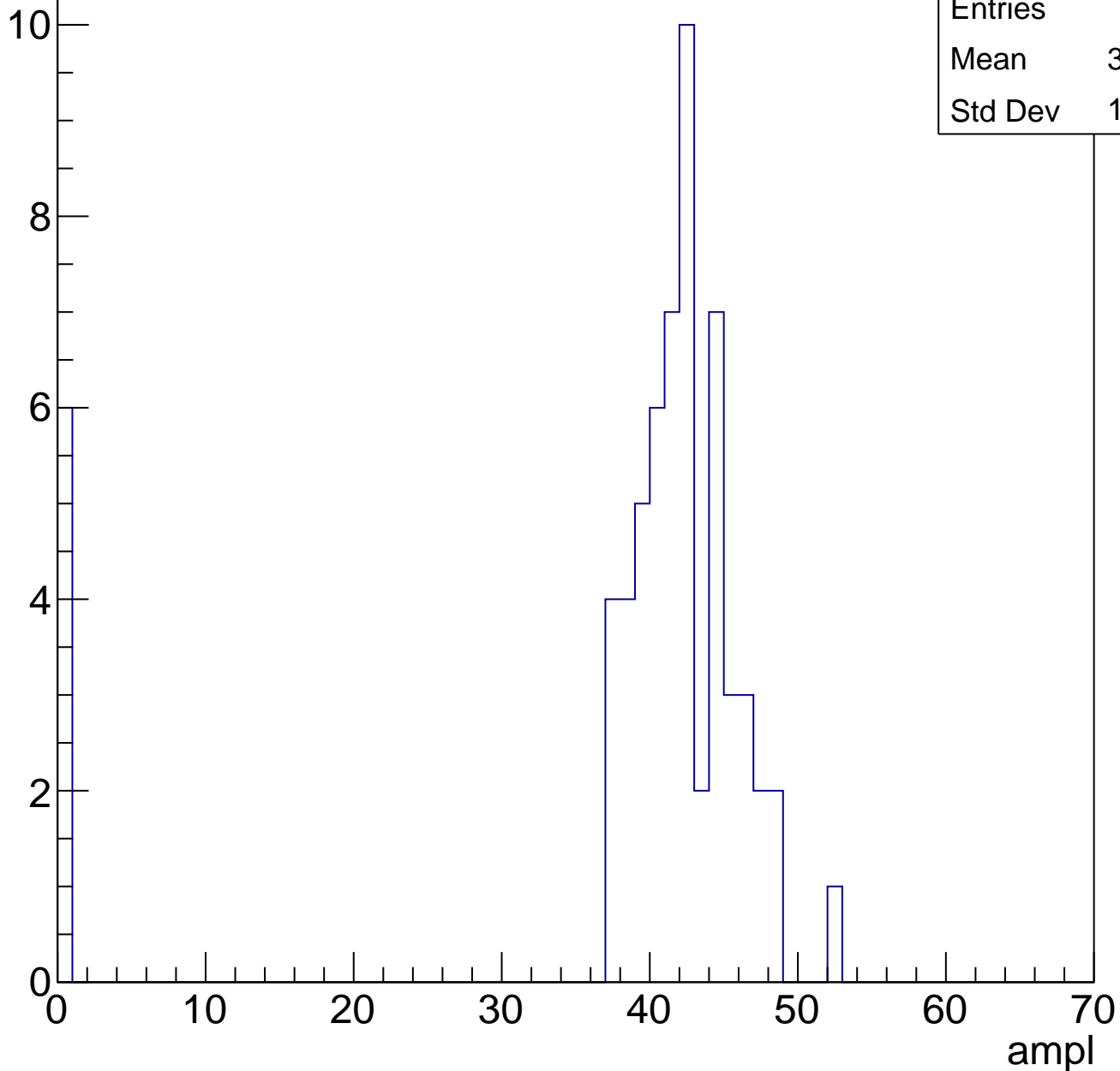


B1L103S, U11-ch2, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	62
Mean	37.92
Std Dev	12.78

Entry

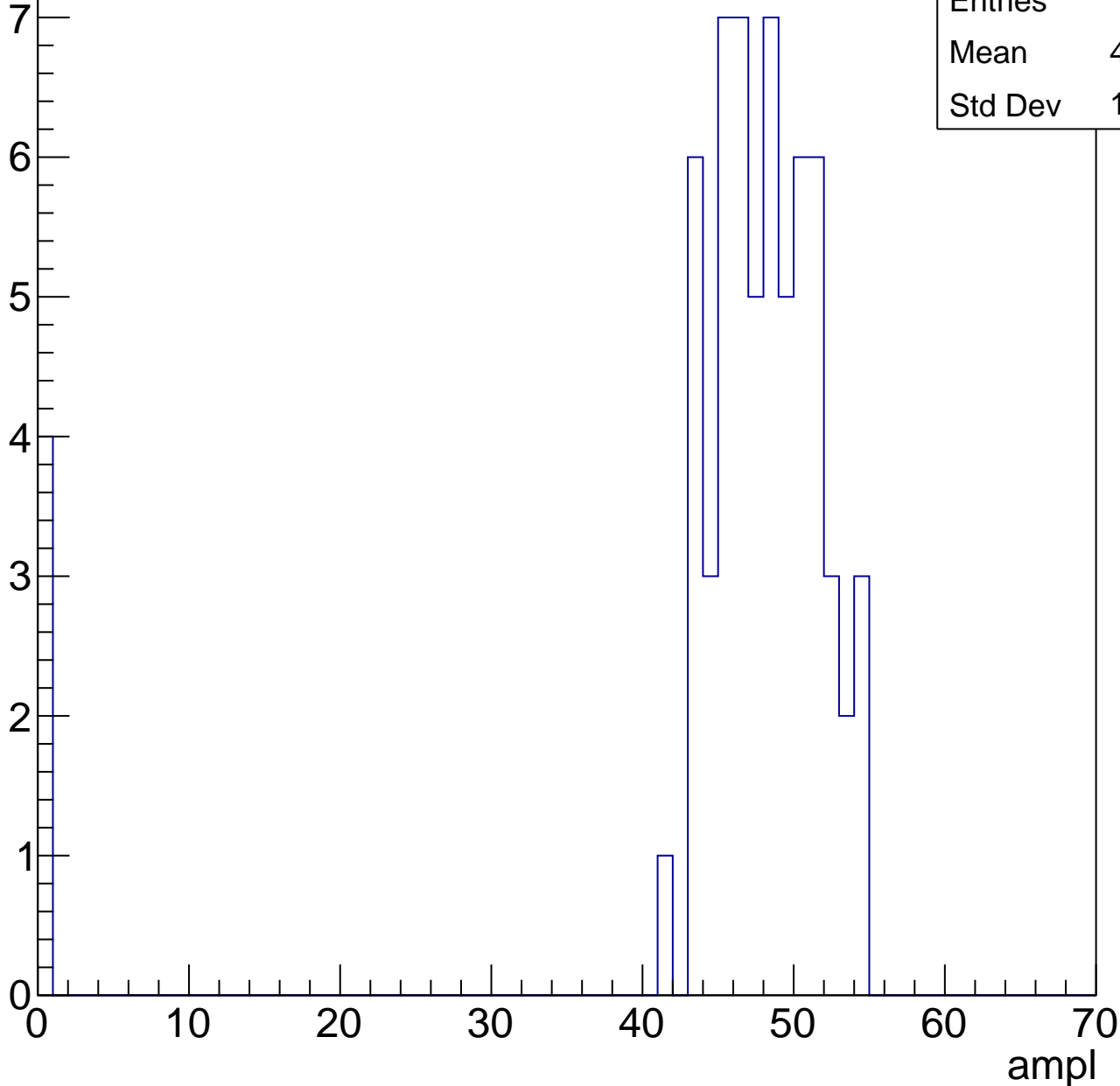


B1L103S, U11-ch2, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	44.83
Std Dev	11.89

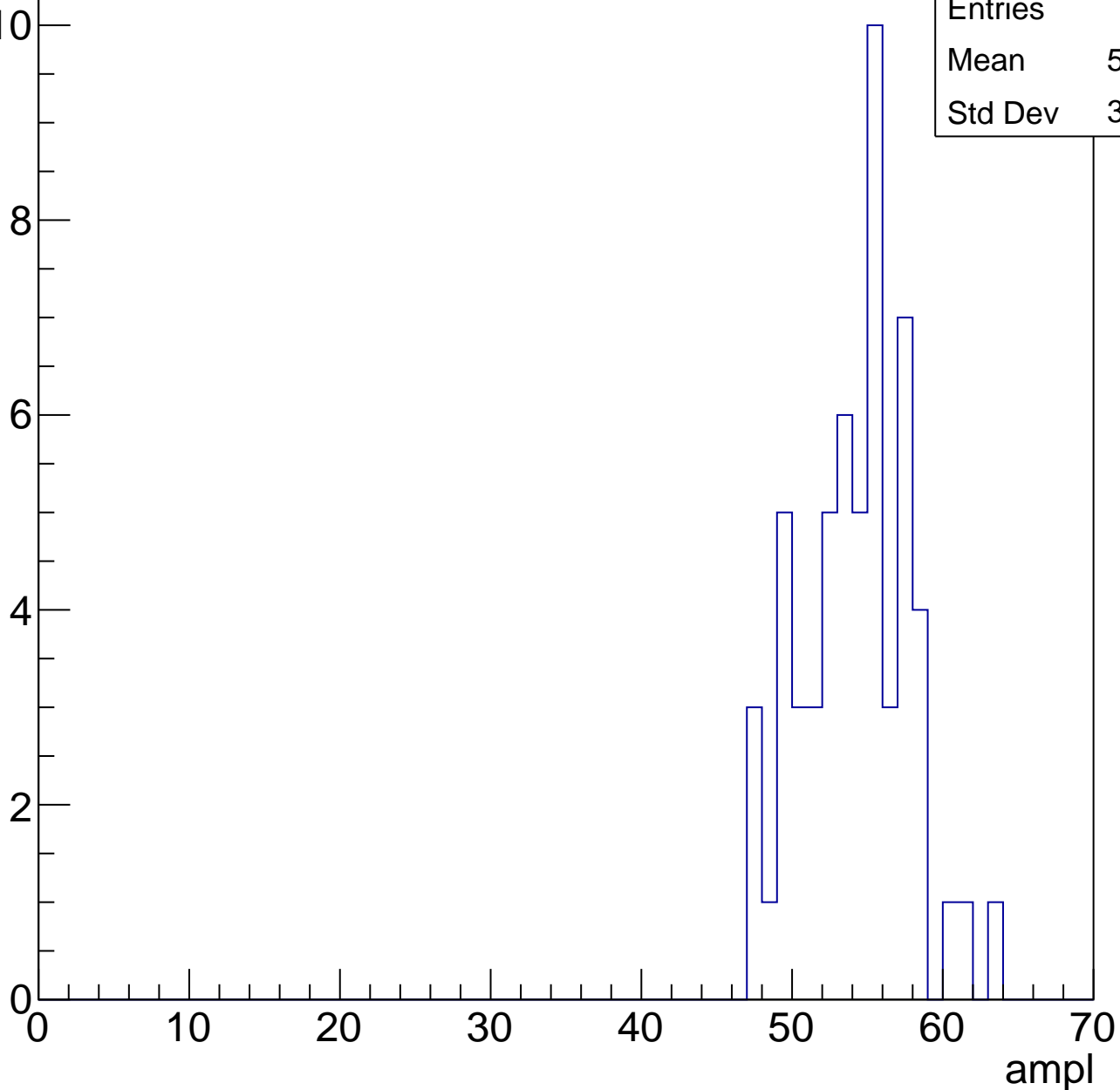


B1L103S, U11-ch2, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	53.76
Std Dev	3.525

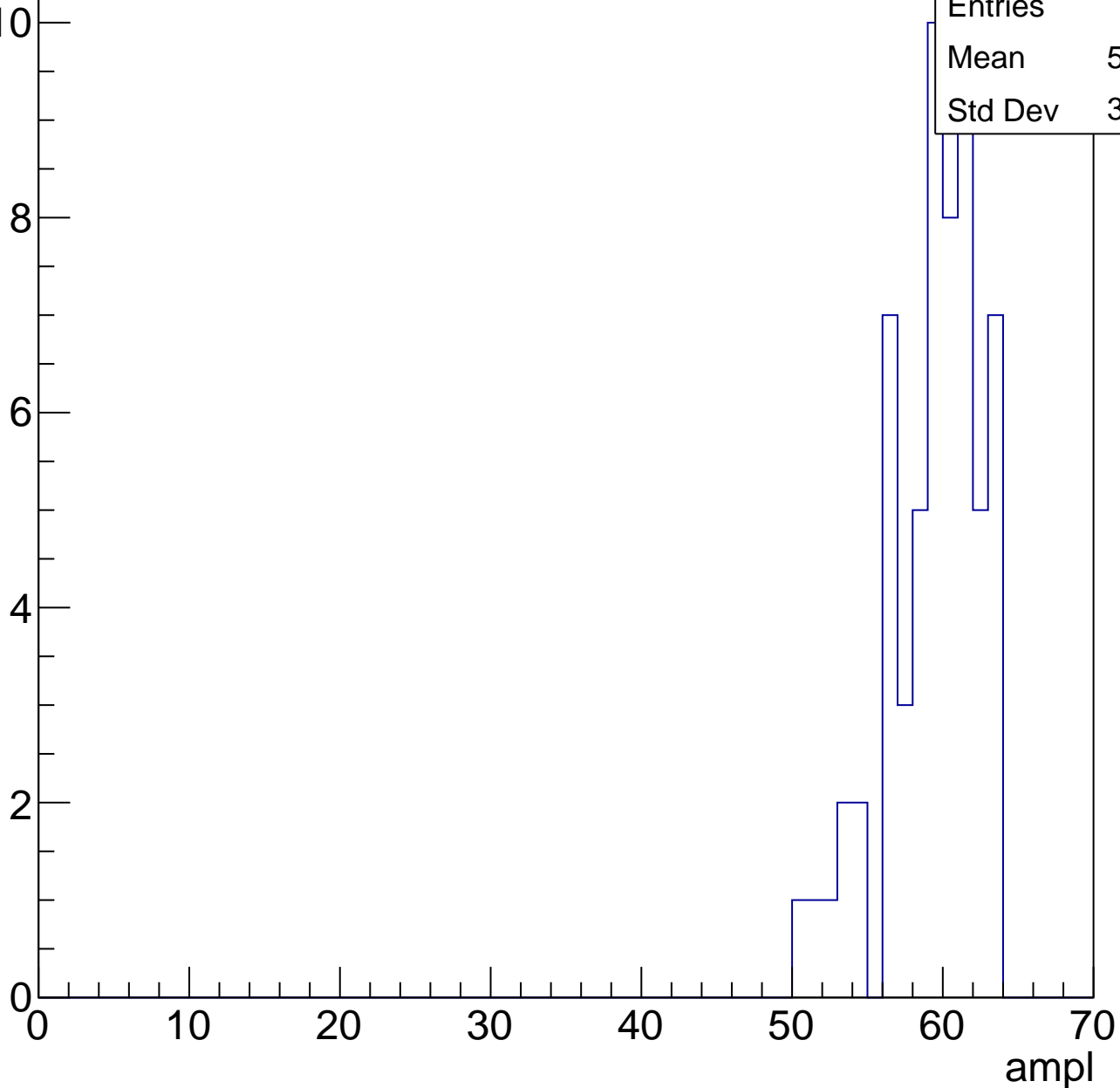


B1L103S, U11-ch2, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	58.85
Std Dev	3.125

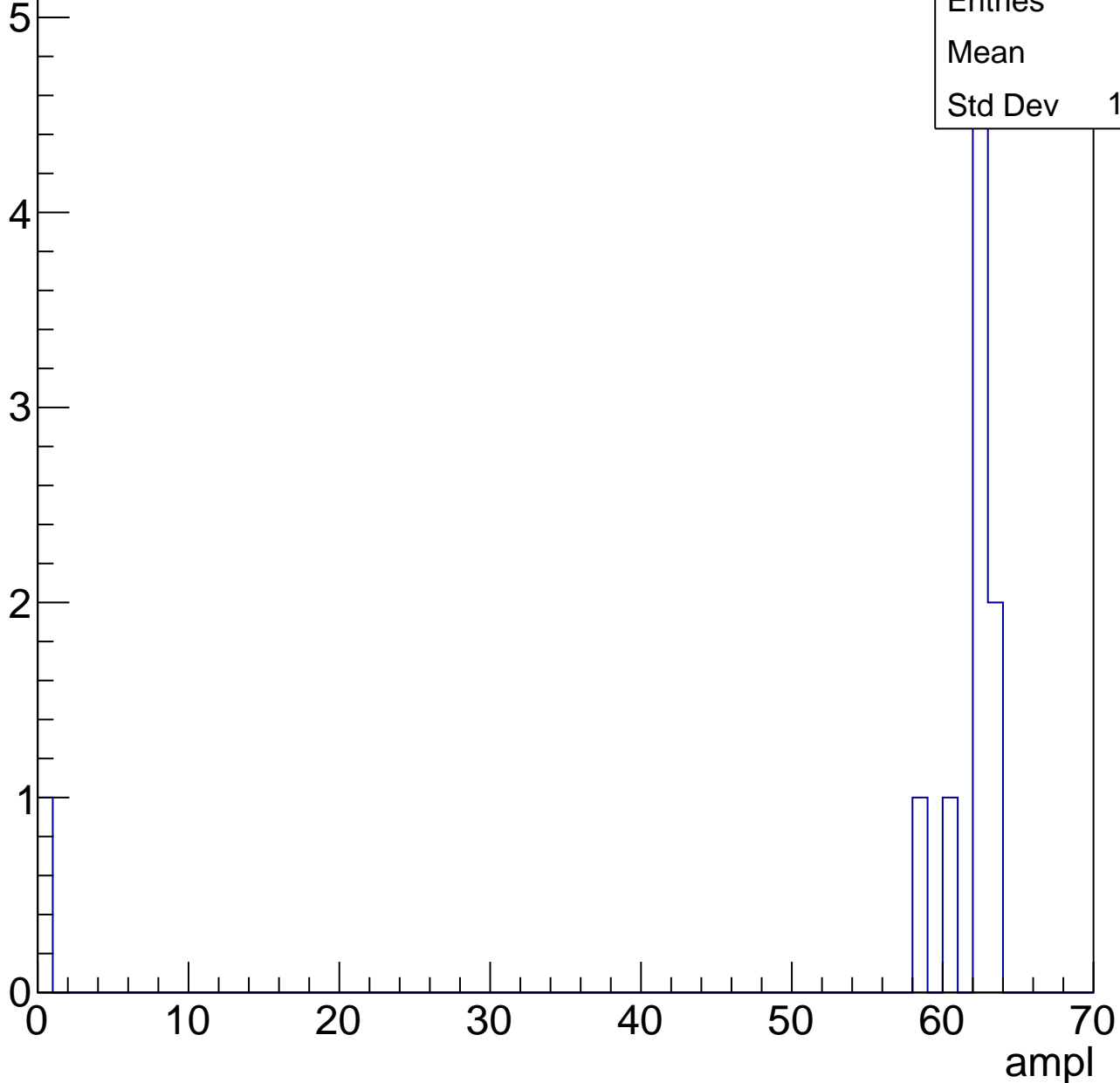


B1L103S, U11-ch2, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	10
Mean	55.4
Std Dev	18.52



B1L103S, U11-ch2, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.105
Std Dev	4.689

Entry

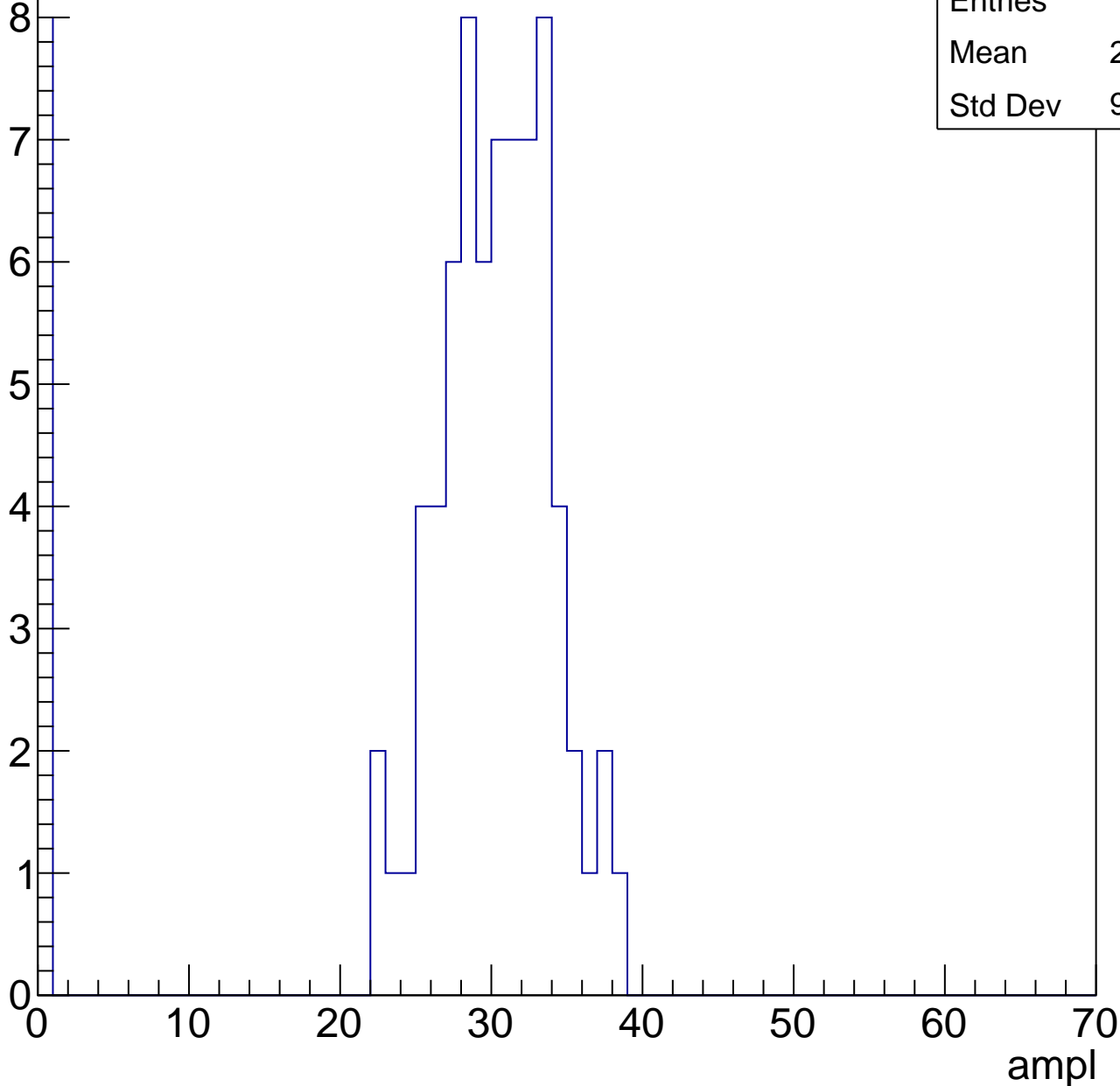


B1L103S, U11-ch3, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	79
Mean	26.89
Std Dev	9.627

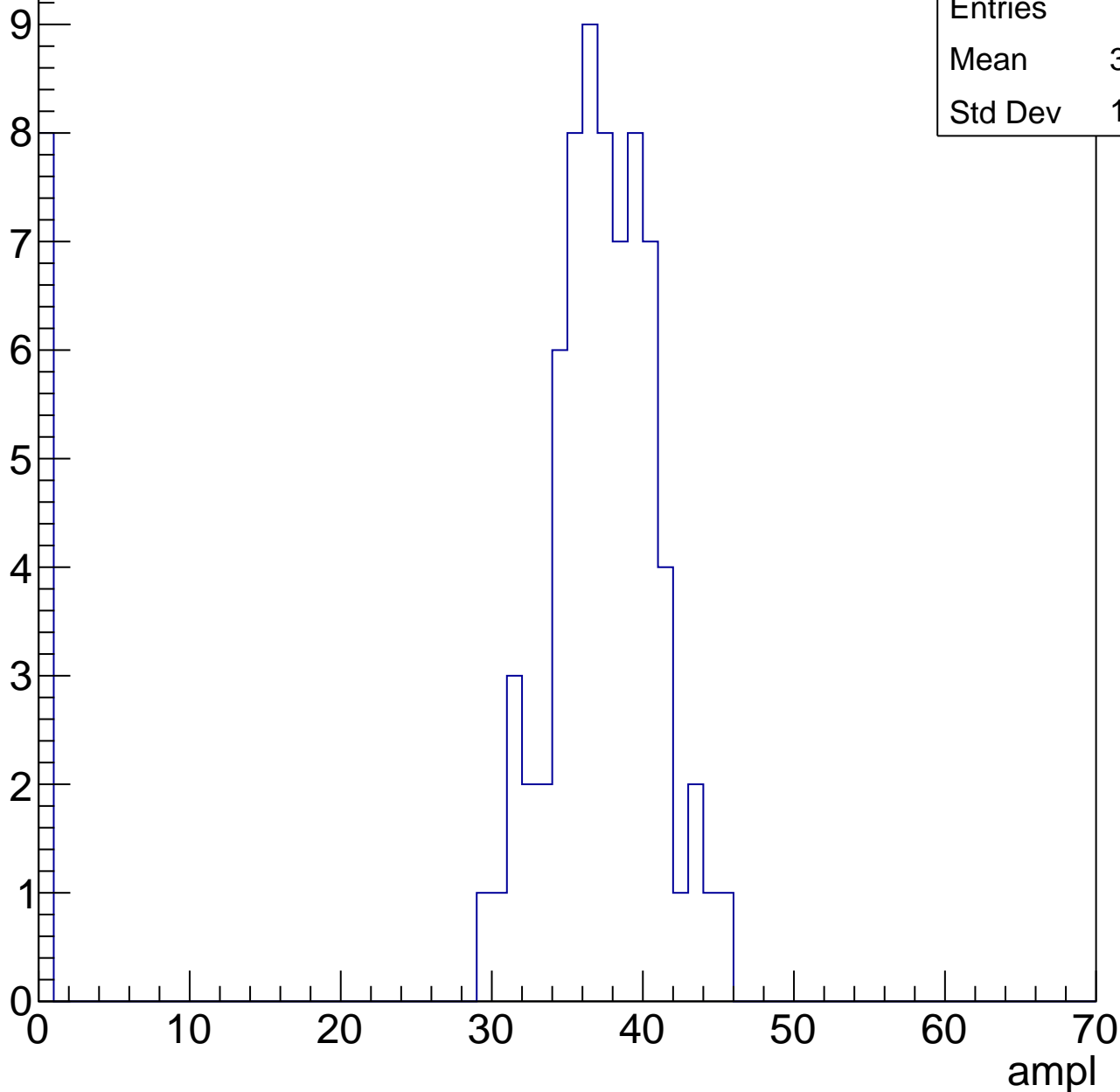


B1L103S, U11-ch3, adc1

calib_packv5_041523_1651.root, FC#0, port C2

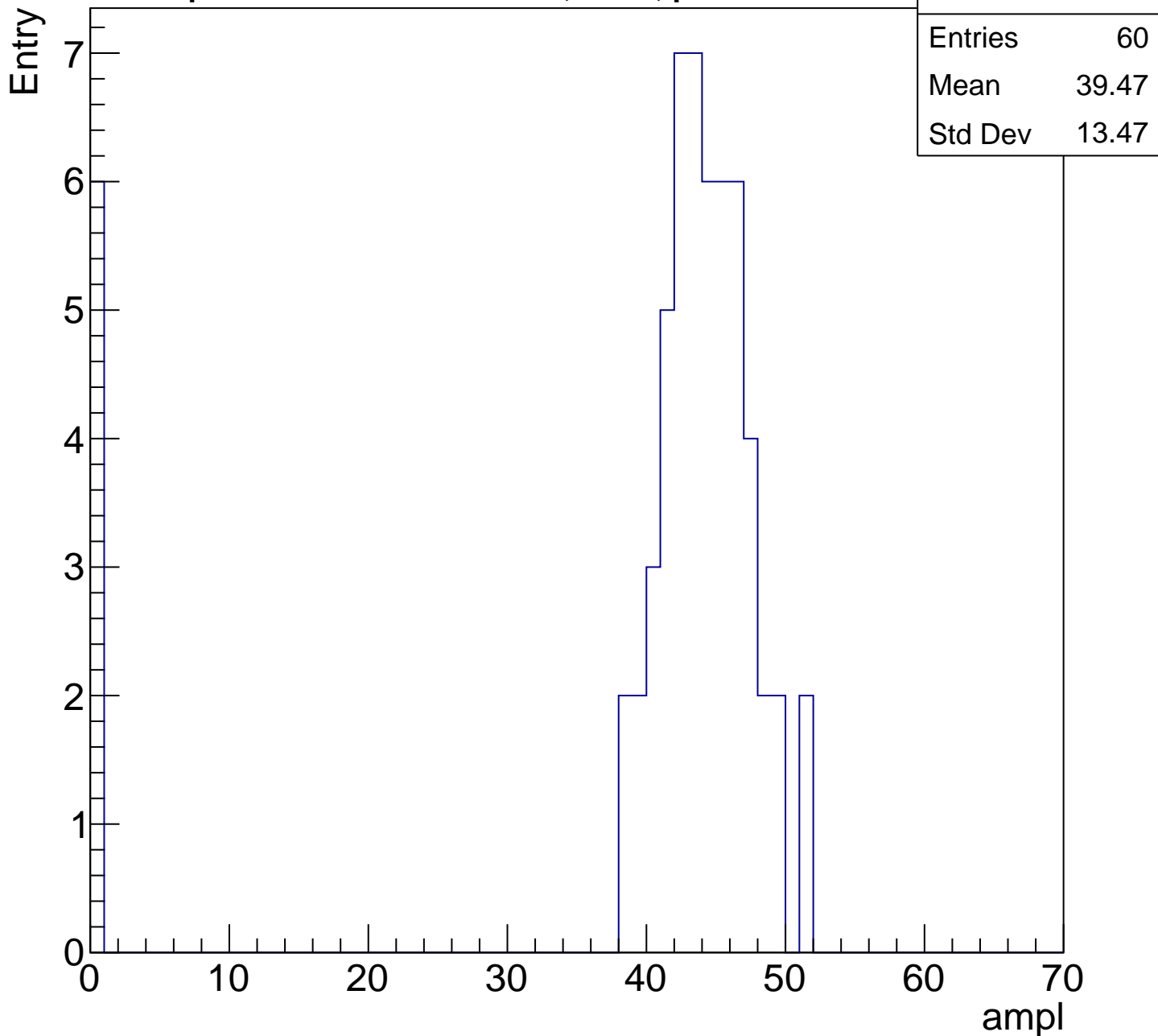
Entry

Entries	79
Mean	33.23
Std Dev	11.58



B1L103S, U11-ch3, adc2

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U11-ch3, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	76
Mean	49.76
Std Dev	3.943

Entry

10

8

6

4

2

0

0

10

20

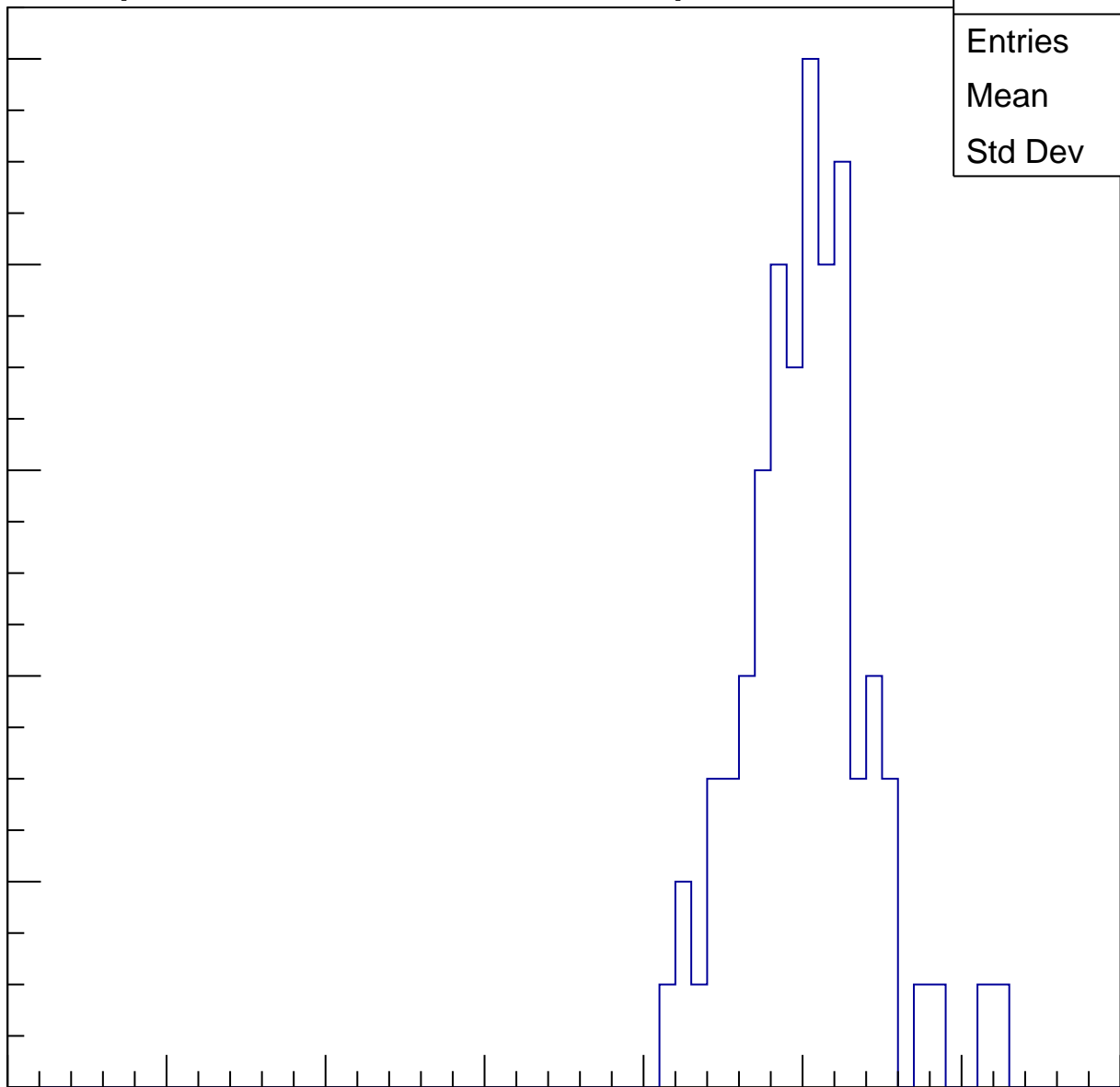
30

40

50

60

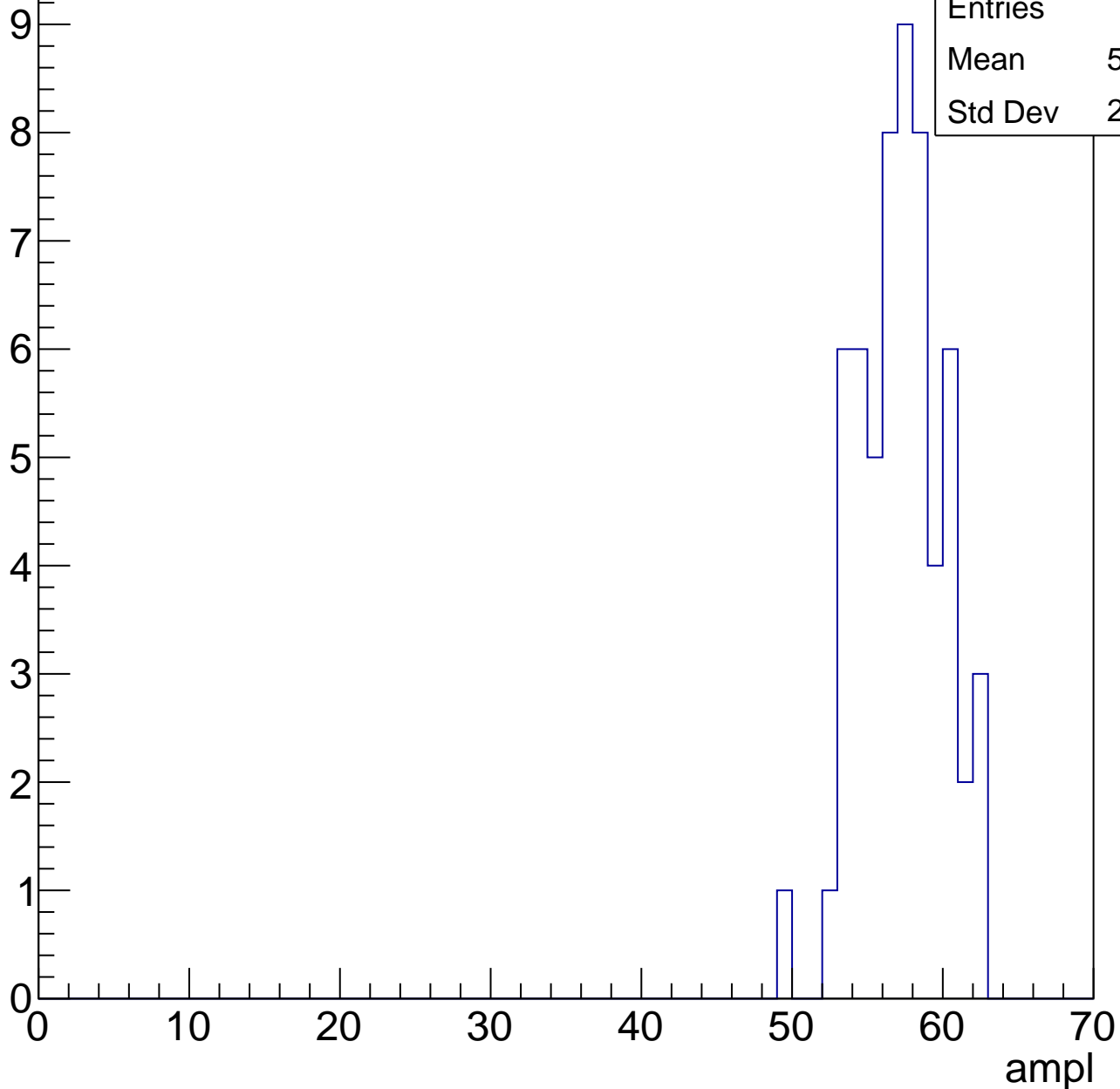
ampl



B1L103S, U11-ch3, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

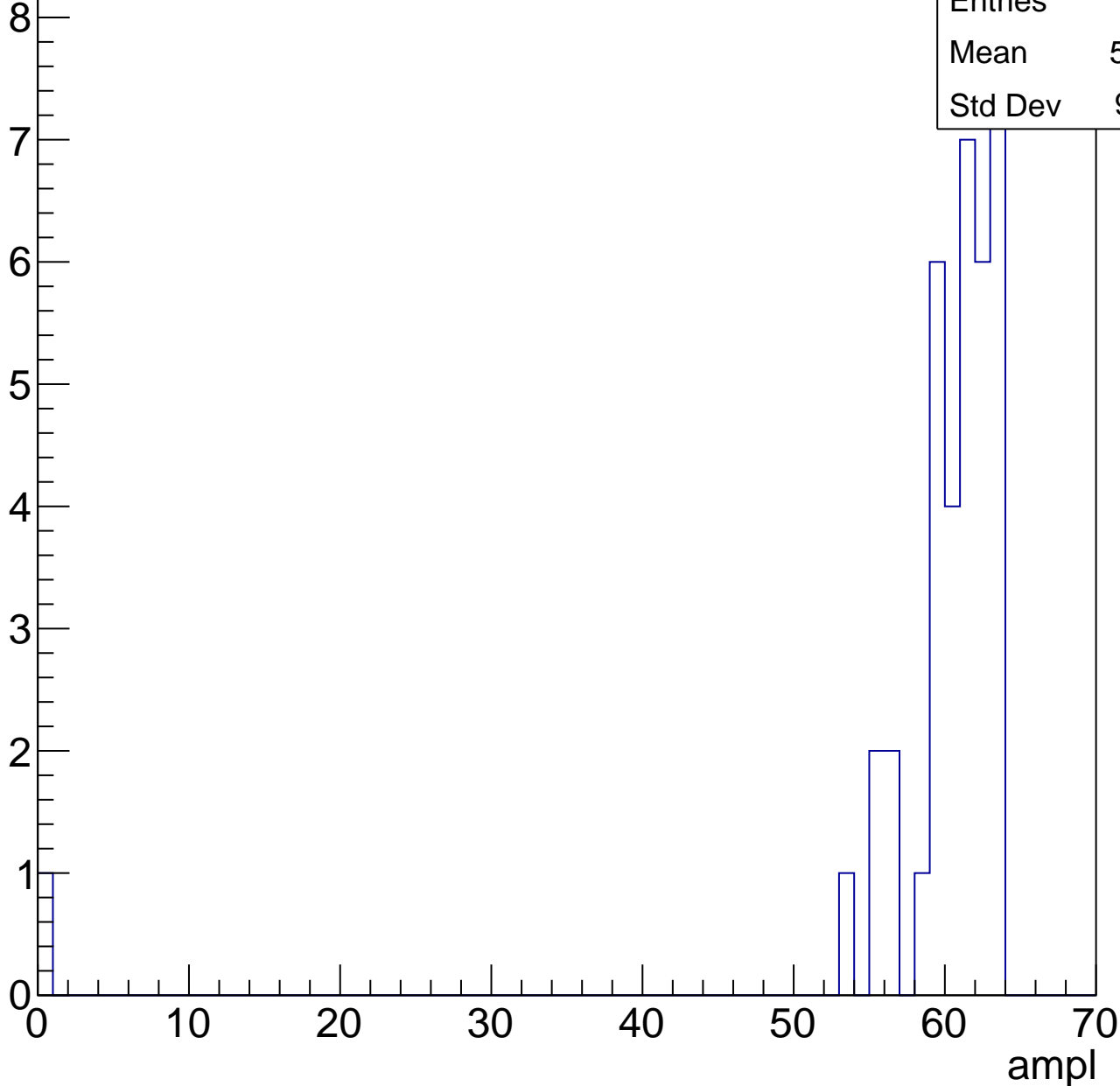


B1L103S, U11-ch3, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	38
Mean	58.68
Std Dev	9.971



B1L103S, U11-ch3, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	2
Mean	63
Std Dev	0

0 10 20 30 40 50 60 70

ampl

B1L103S, U11-ch3, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch4, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	24.33
Std Dev	10.5

Entry

12

10

8

6

4

2

0

0

10

20

30

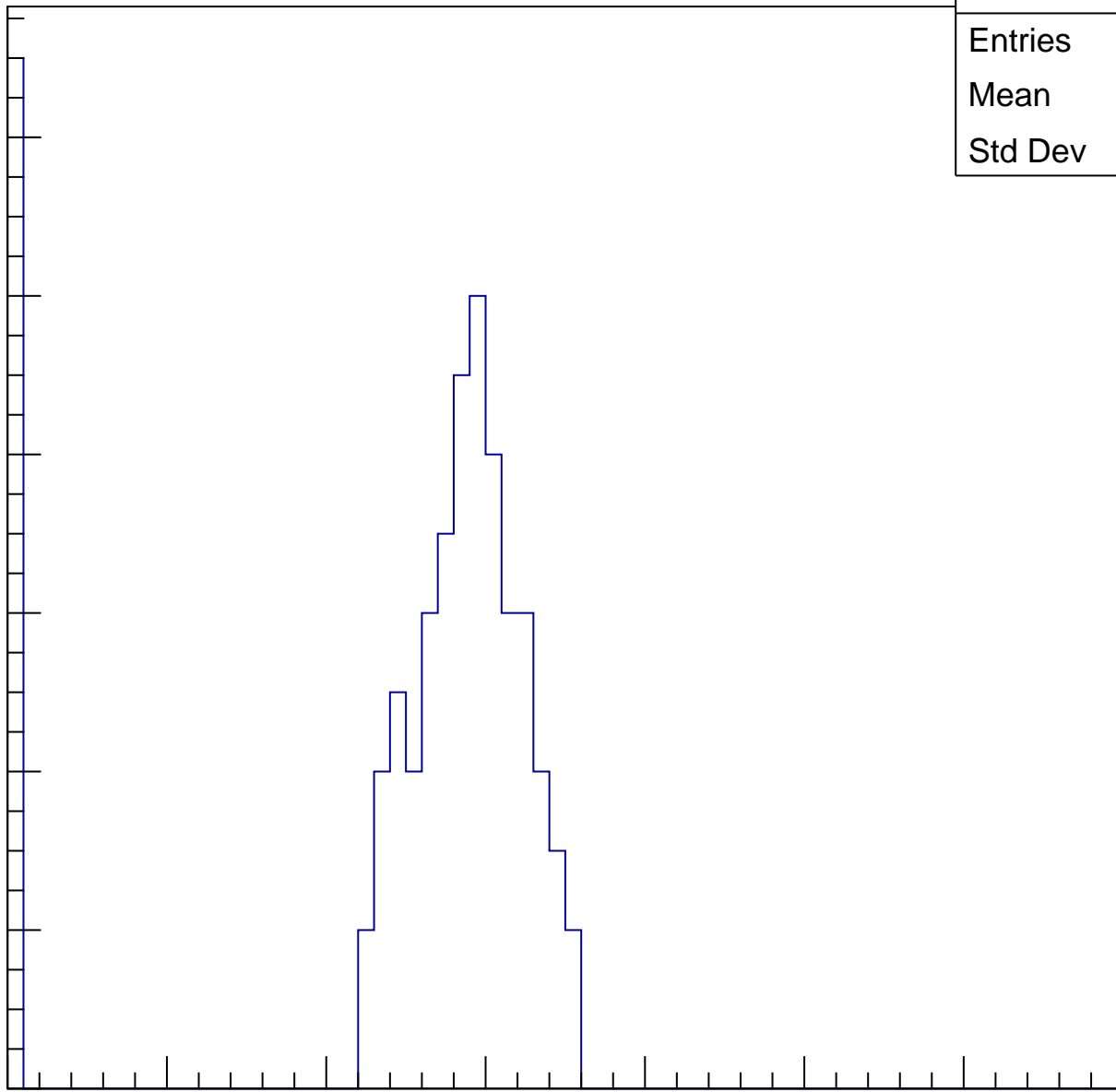
40

50

60

70

ampl

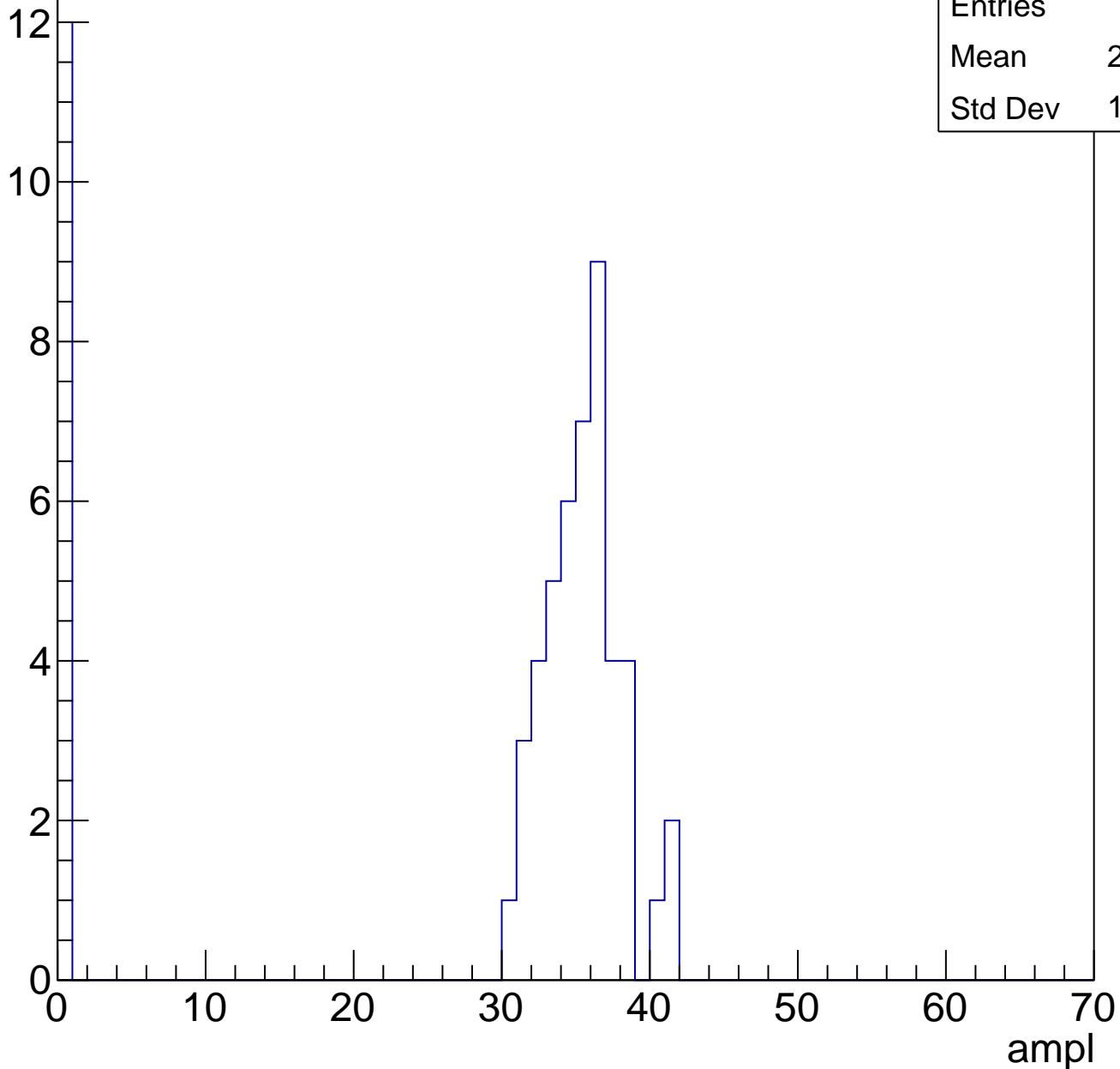


B1L103S, U11-ch4, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	58
Mean	27.78
Std Dev	14.36

Entry

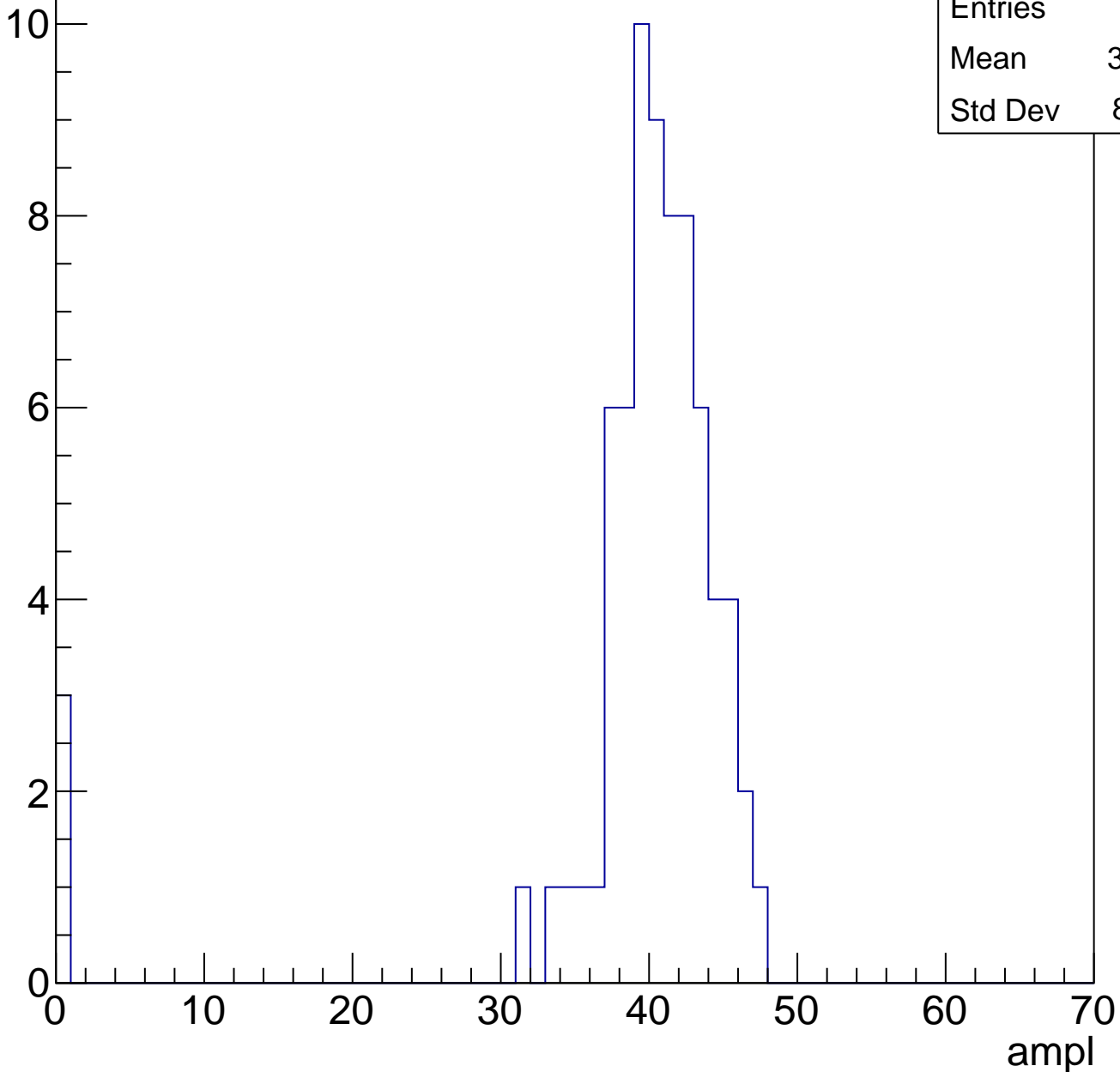


B1L103S, U11-ch4, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	72
Mean	38.69
Std Dev	8.621

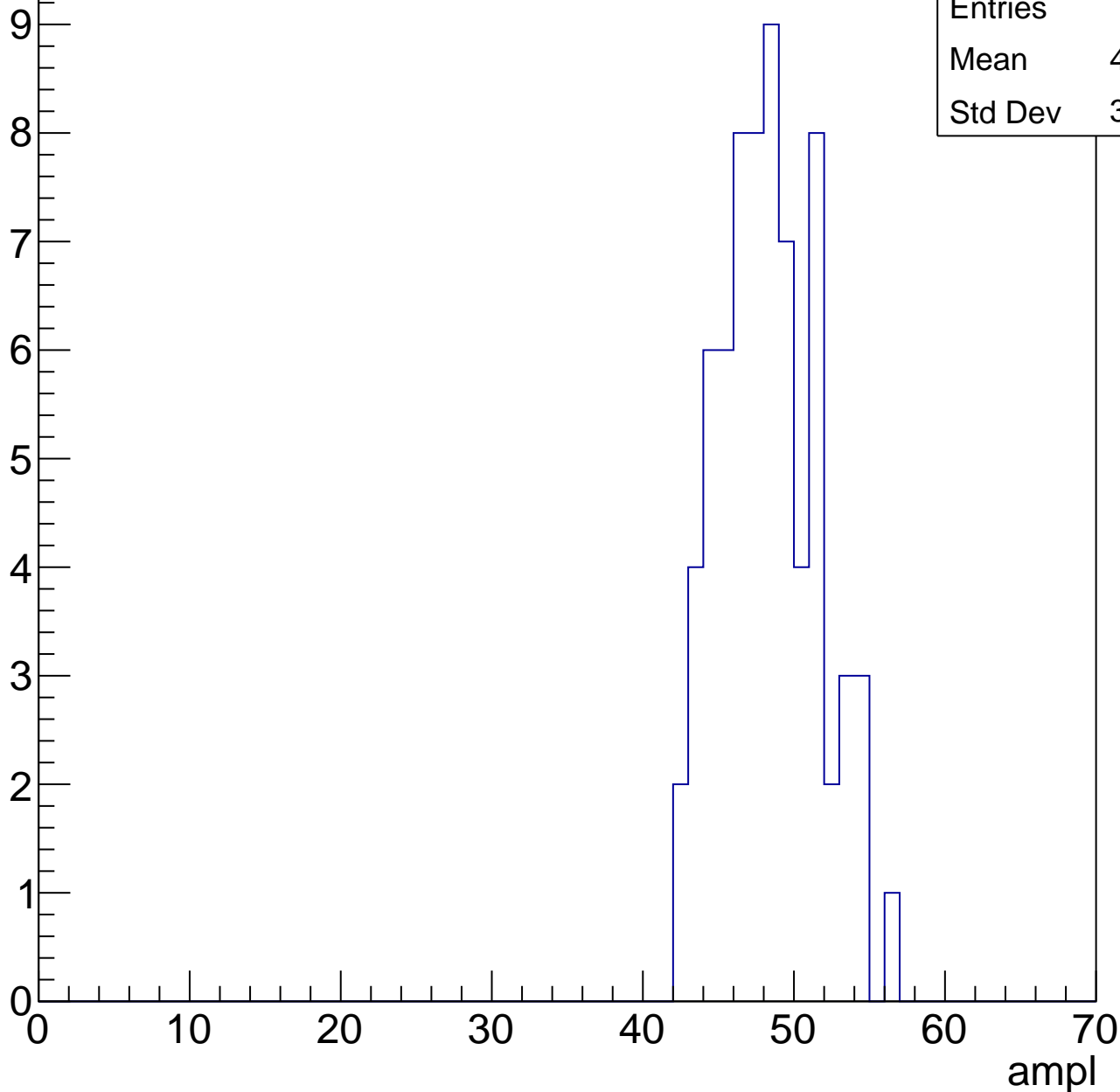
Entry



B1L103S, U11-ch4, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry



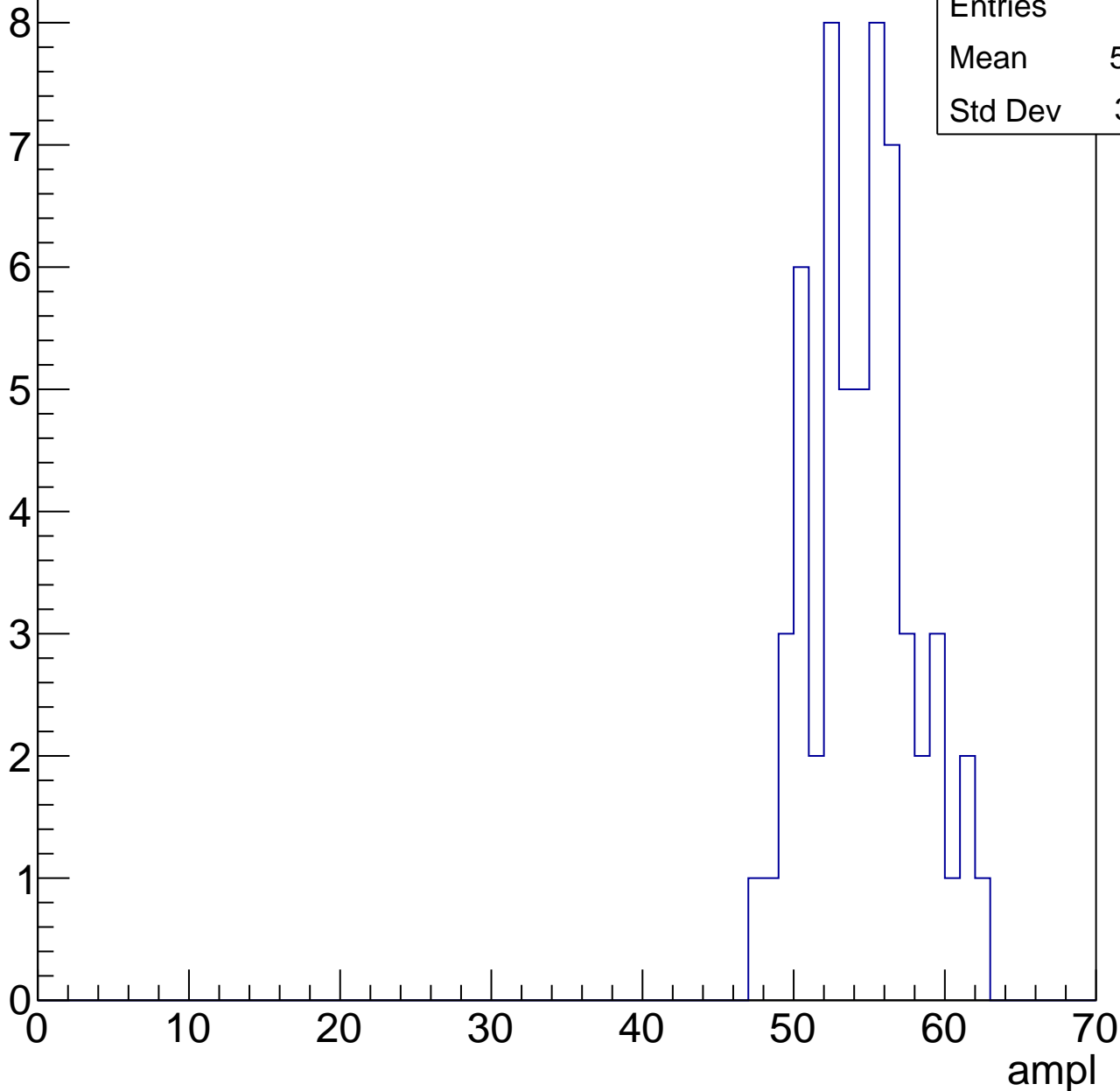
Entries	71
Mean	47.86
Std Dev	3.217

B1L103S, U11-ch4, adc4

calib_packv5_041523_1651.root, FC#0, port C2

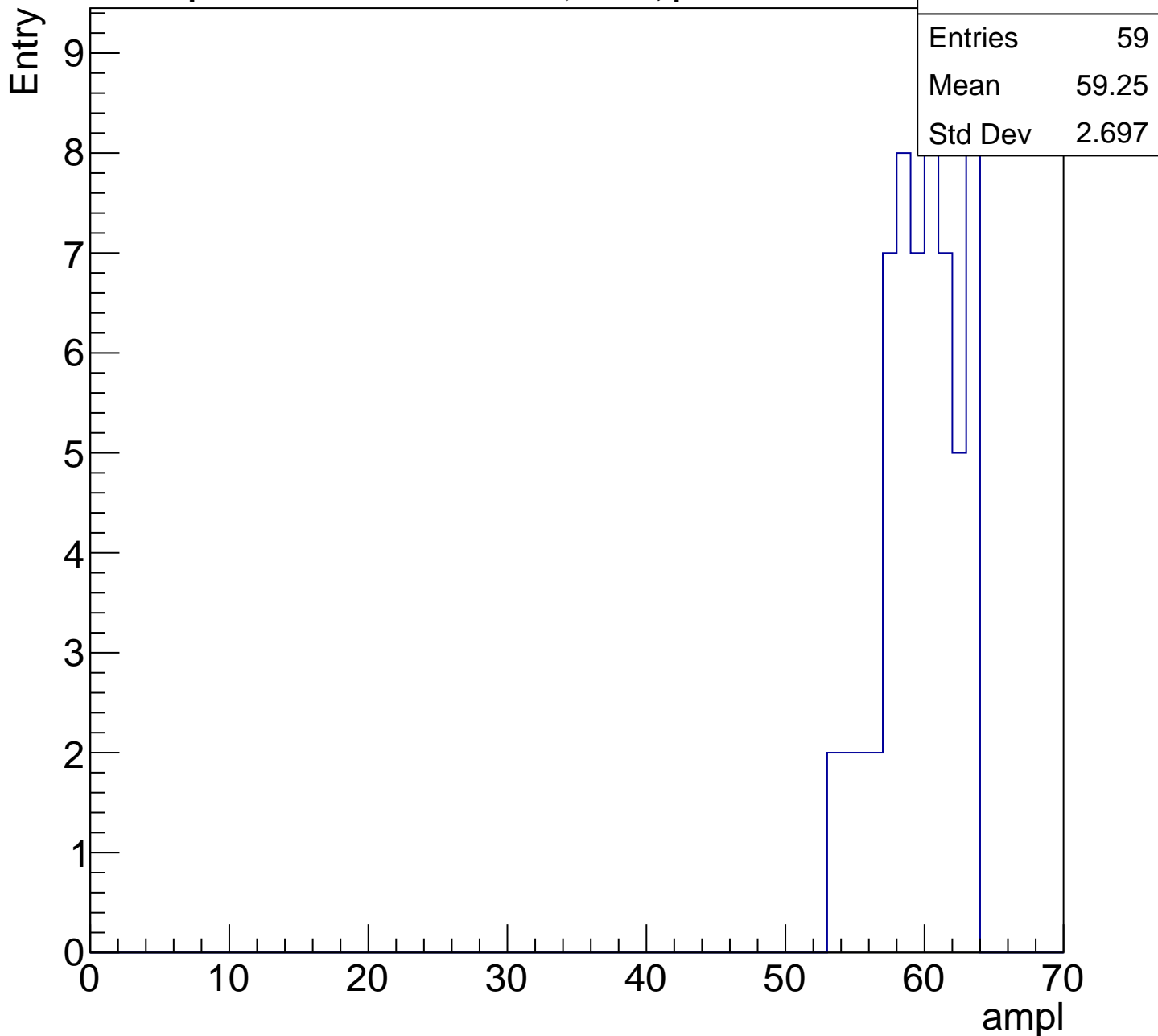
Entry

Entries	58
Mean	54.05
Std Dev	3.421



B1L103S, U11-ch4, adc5

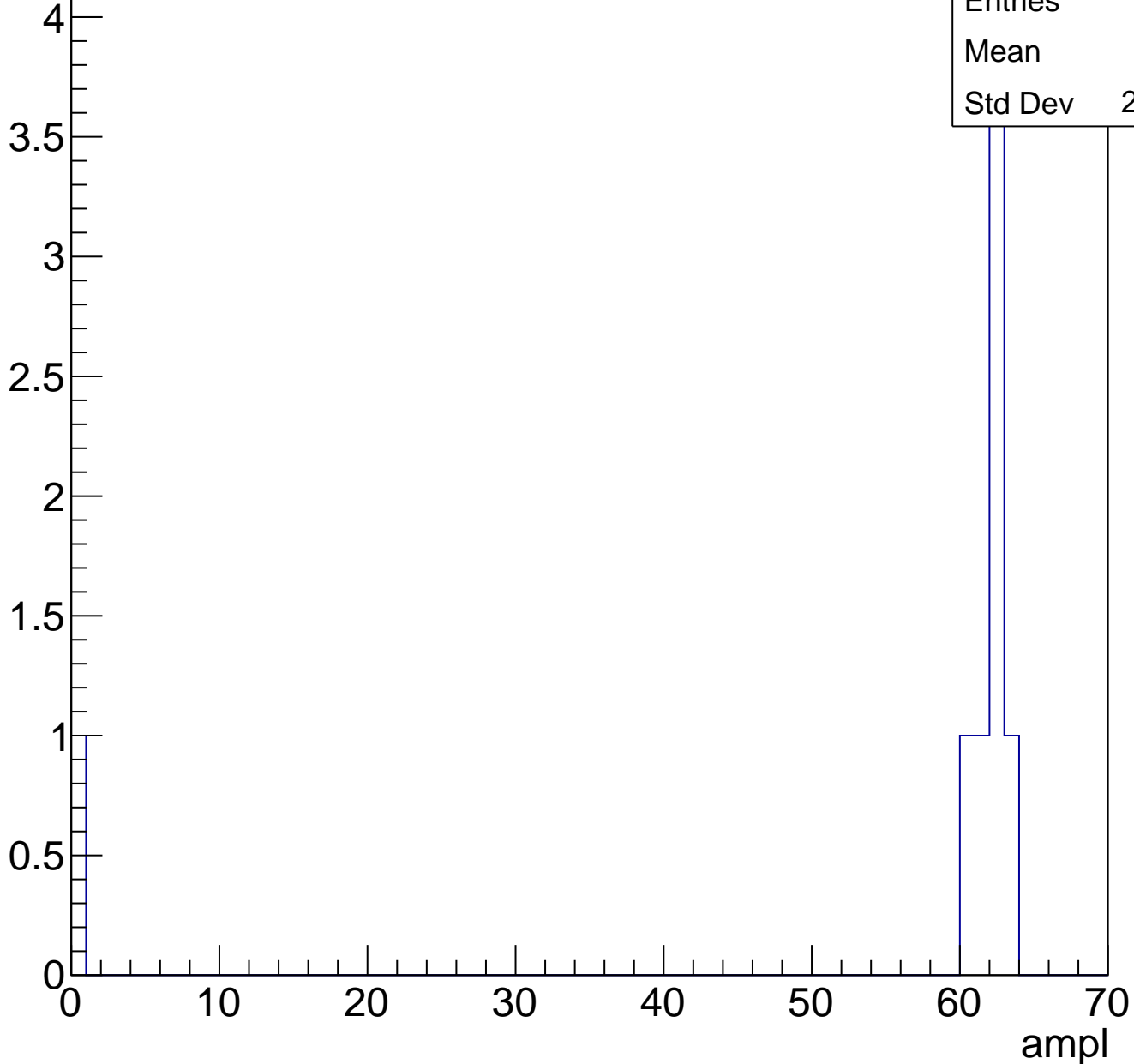
calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U11-ch4, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch4, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	19
Mean	0
Std Dev	0

B1L103S, U11-ch5, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	88
Mean	30.64
Std Dev	7.455

Entry

10

8

6

4

2

0

0

10

20

30

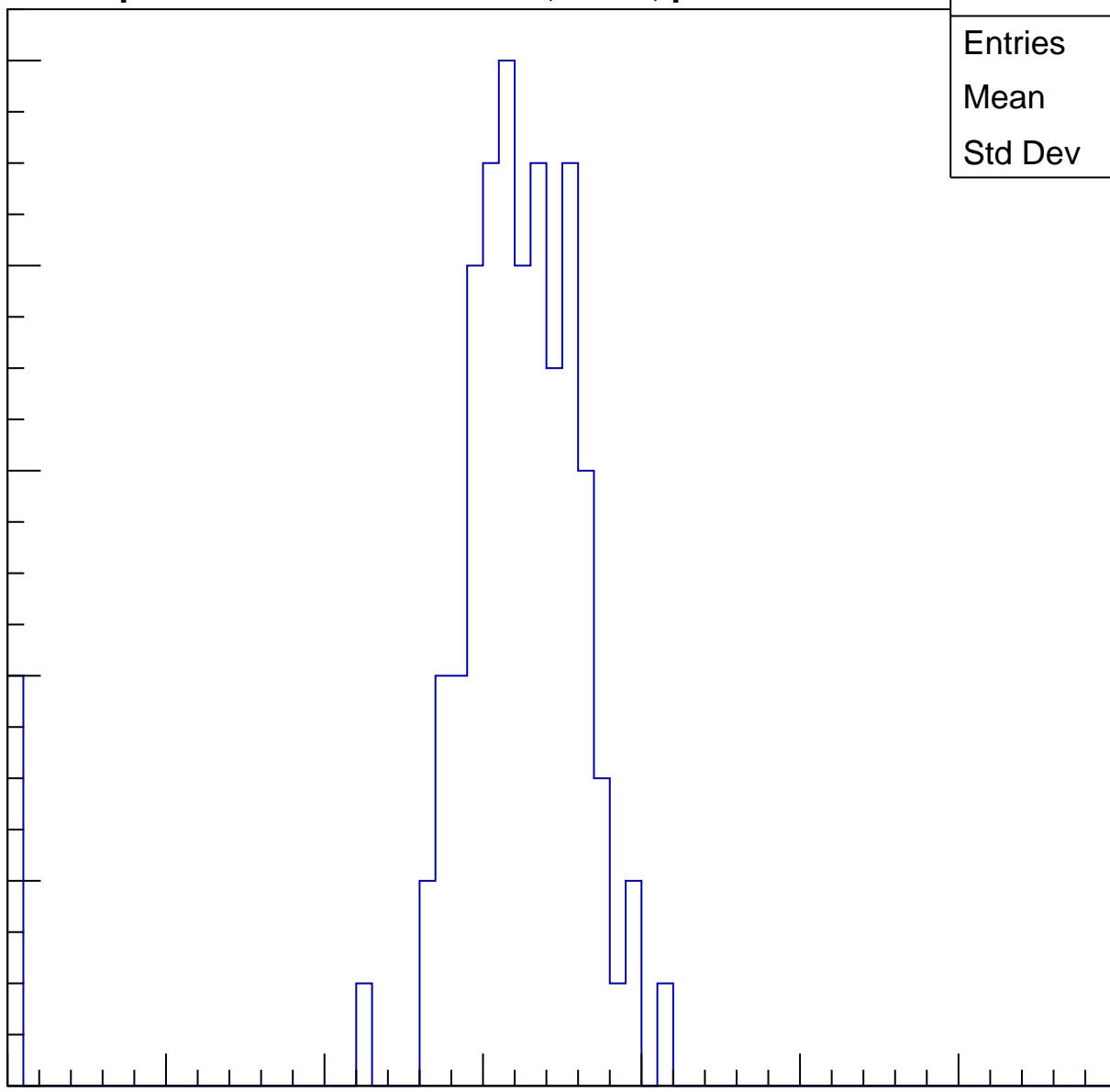
40

50

60

70

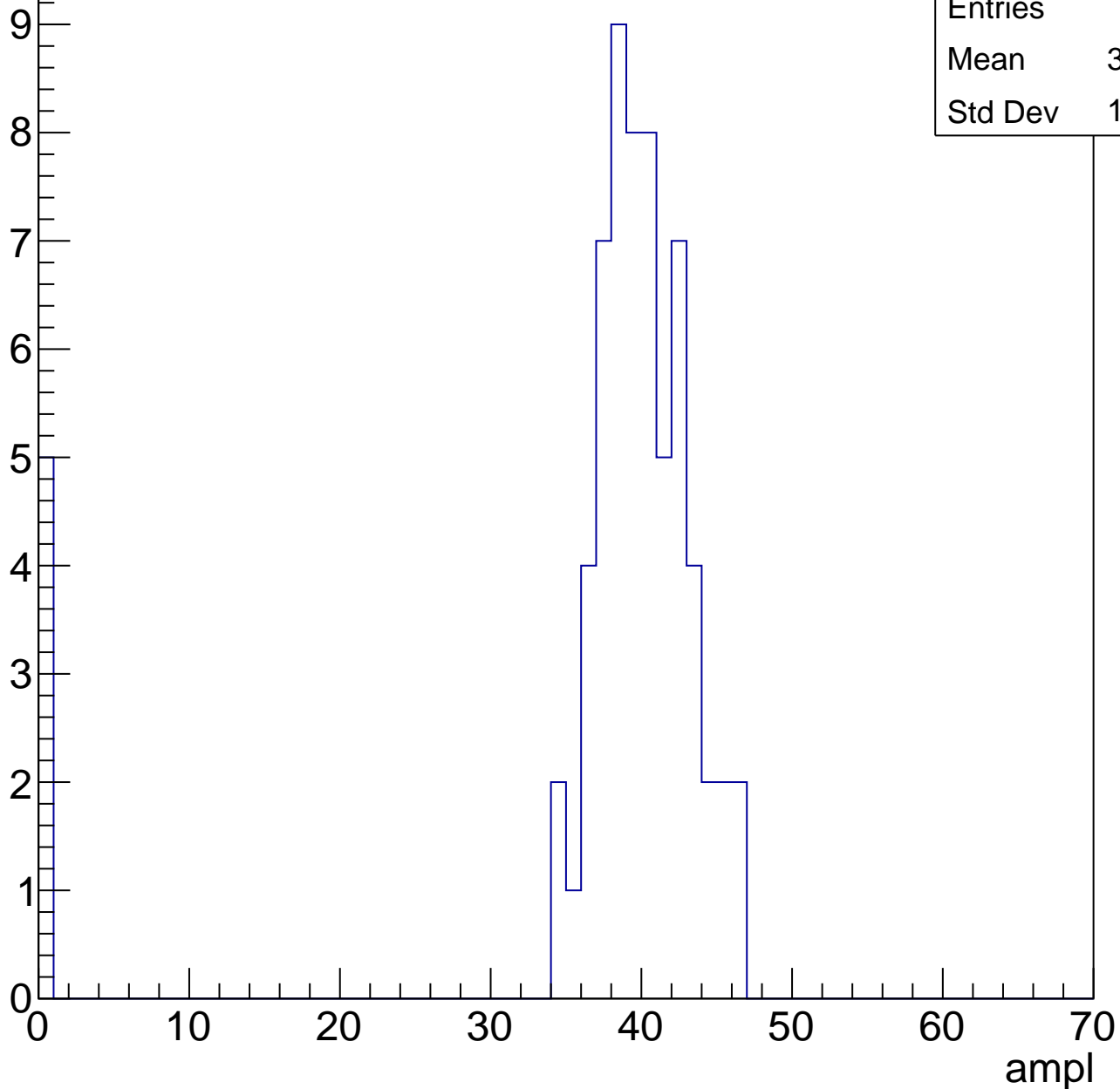
ampl



B1L103S, U11-ch5, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch5, adc2

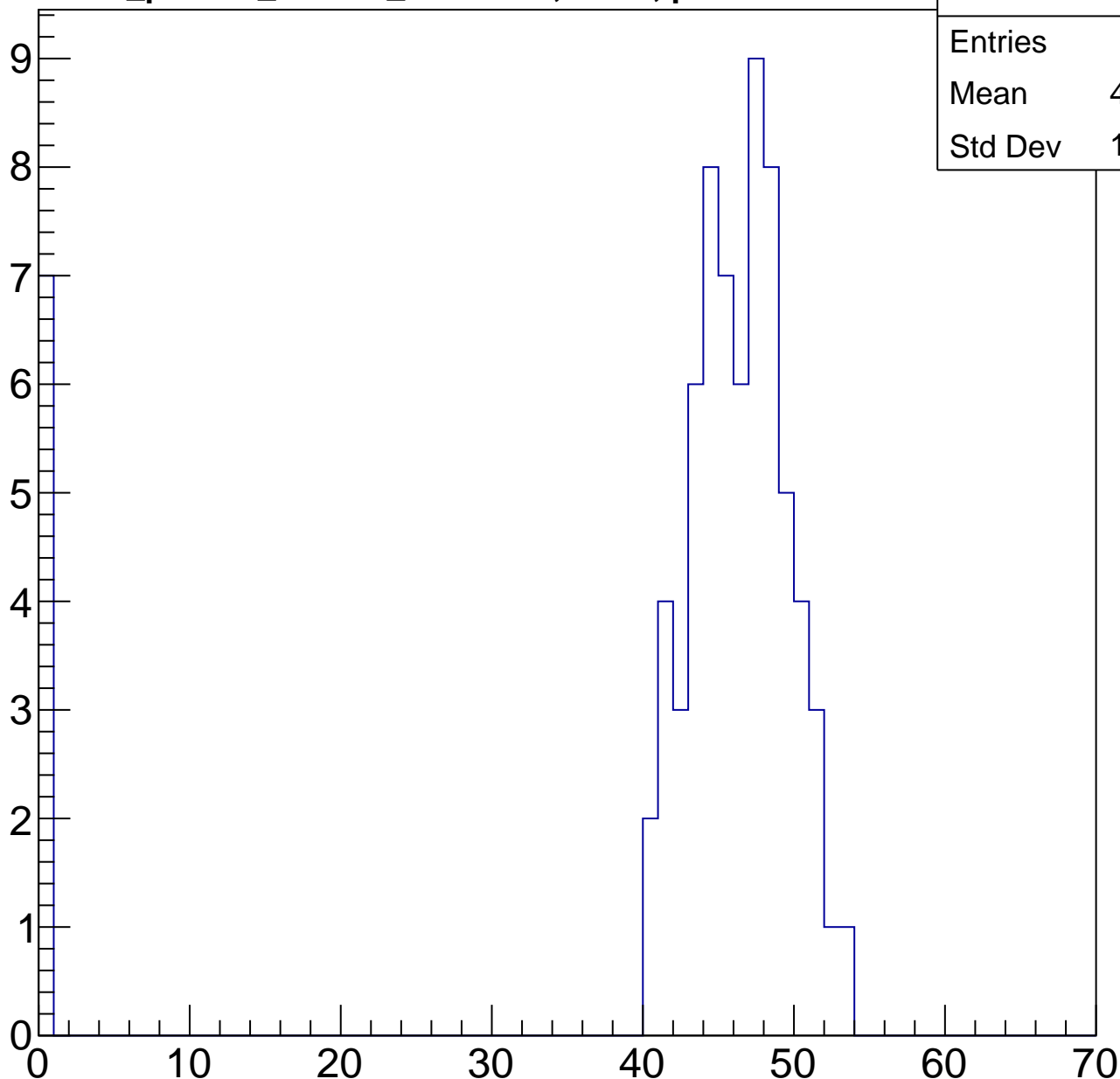
calib_packv5_041523_1651.root, FC#0, port C2

Entry

9
8
7
6
5
4
3
2
1
0

Entries	74
Mean	41.64
Std Dev	13.77

ampl

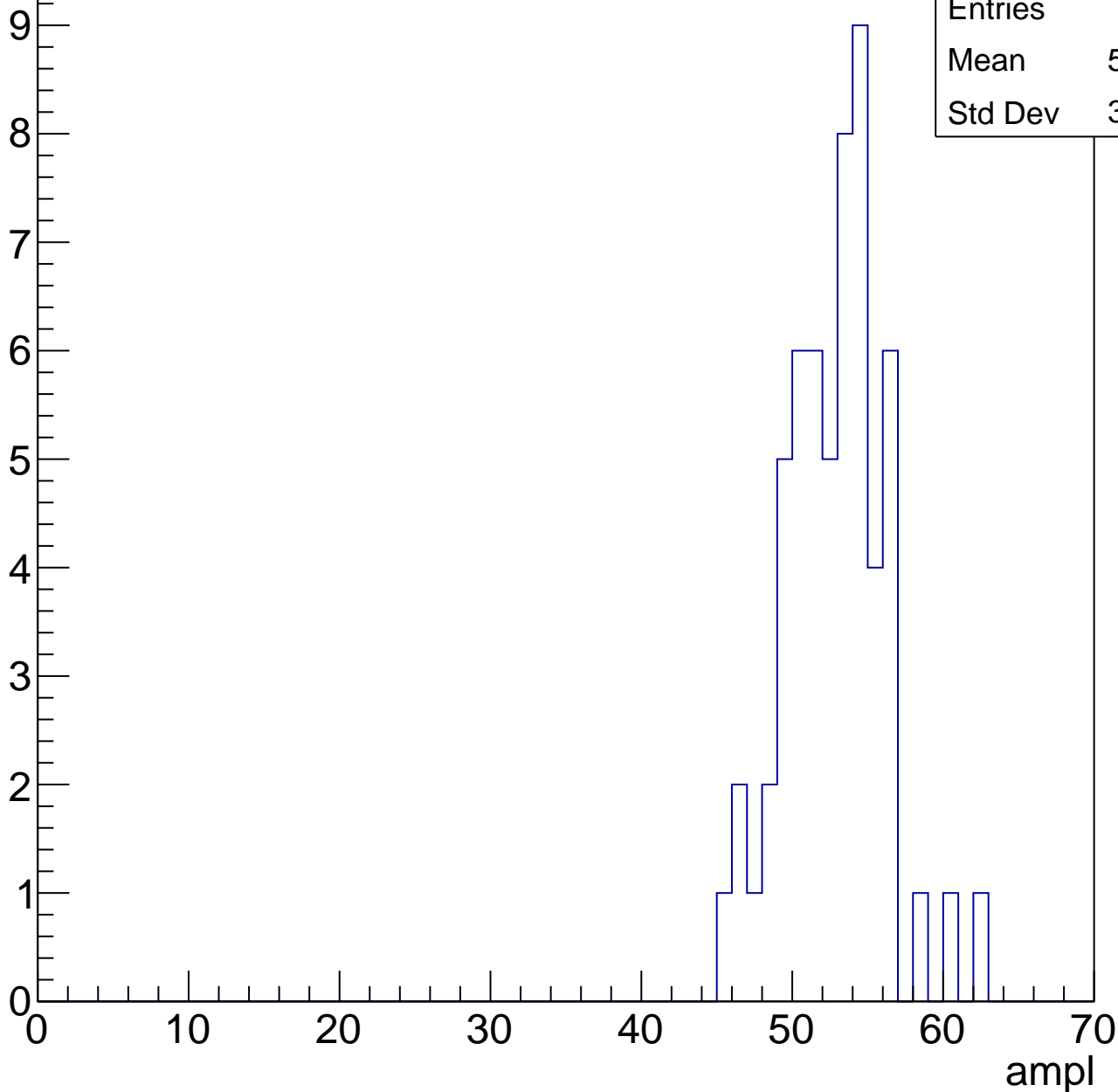


B1L103S, U11-ch5, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	52.36
Std Dev	3.273



B1L103S, U11-ch5, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	50
Mean	57.24
Std Dev	2.811

Entry

10

8

6

4

2

0

0

10

20

30

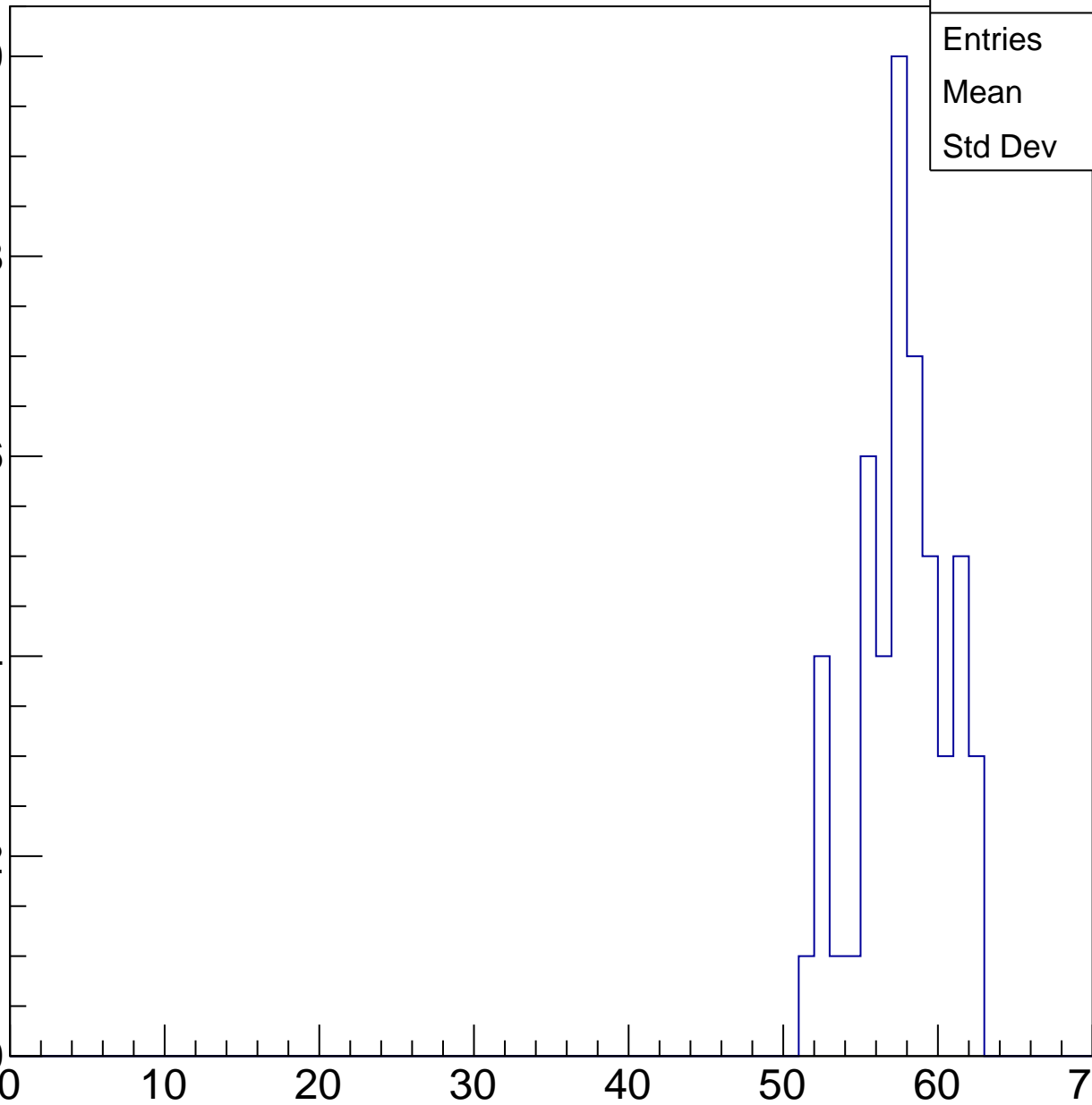
40

50

60

70

ampl

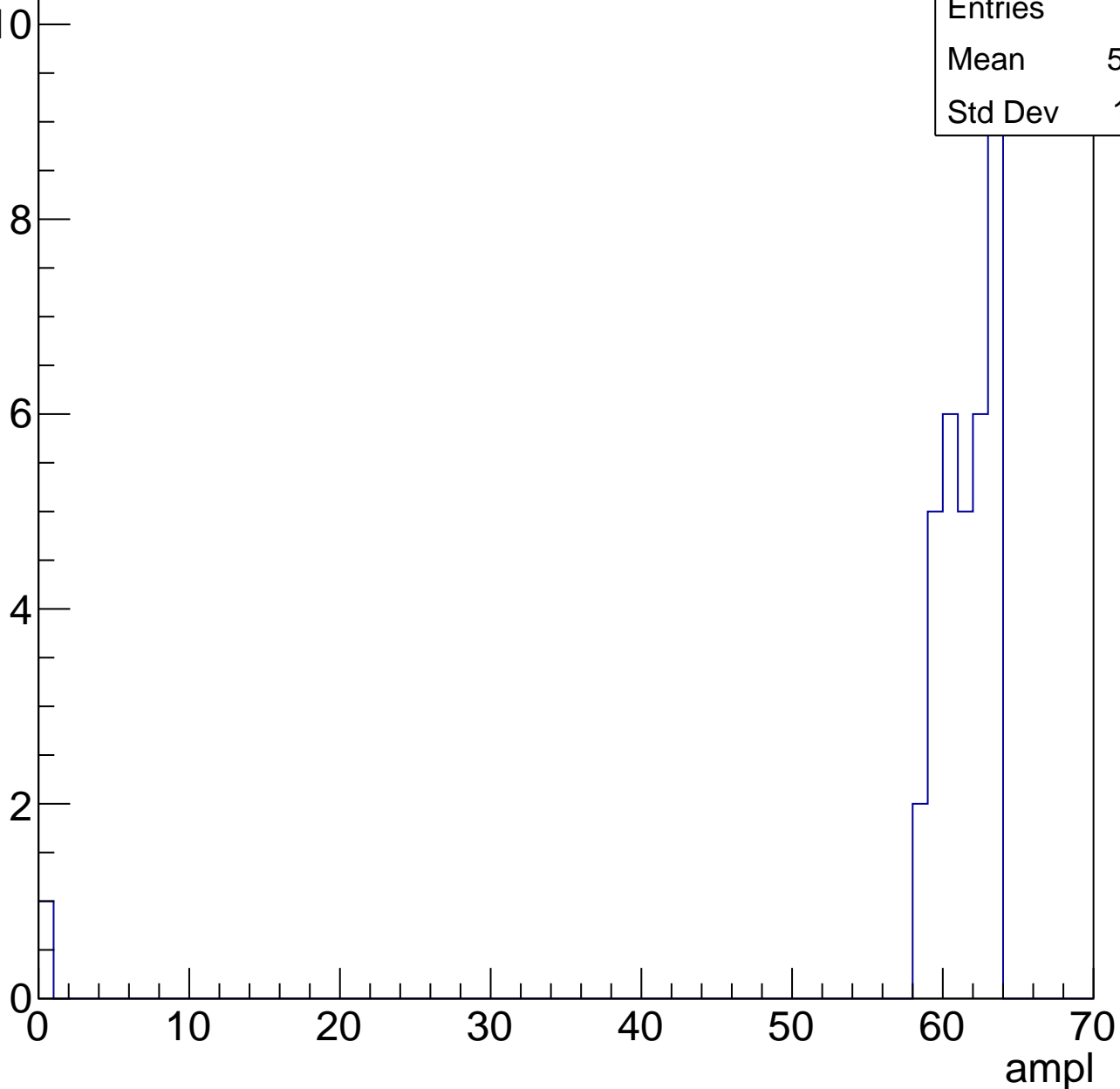


B1L103S, U11-ch5, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	35
Mean	59.37
Std Dev	10.31



B1L103S, U11-ch5, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L103S, U11-ch5, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	18
Mean	0
Std Dev	0

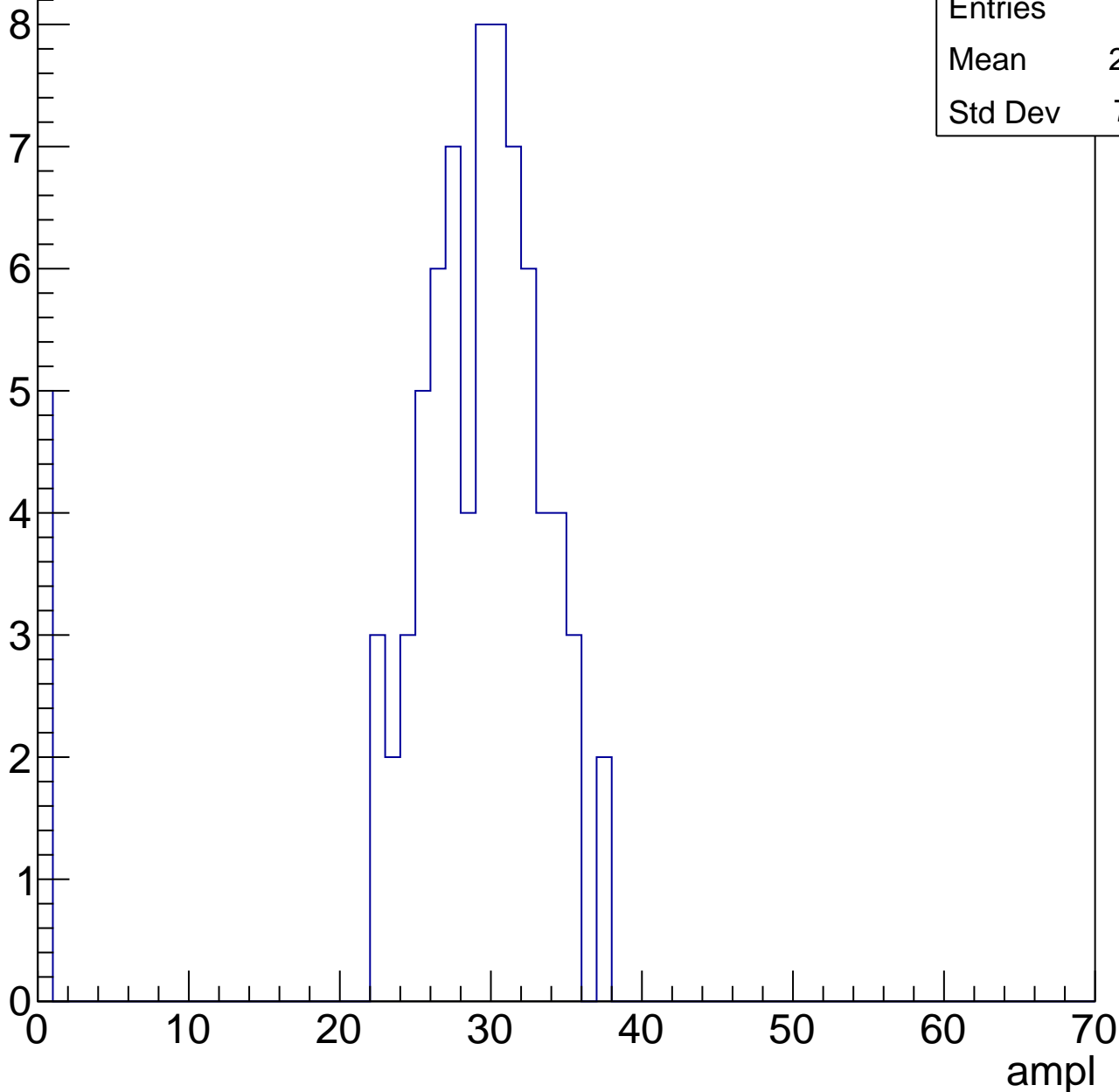
ampl

B1L103S, U11-ch6, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	27.19
Std Dev	7.981



B1L103S, U11-ch6, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	33.95
Std Dev	10.17

Entry

10

8

6

4

2

0

0

10

20

30

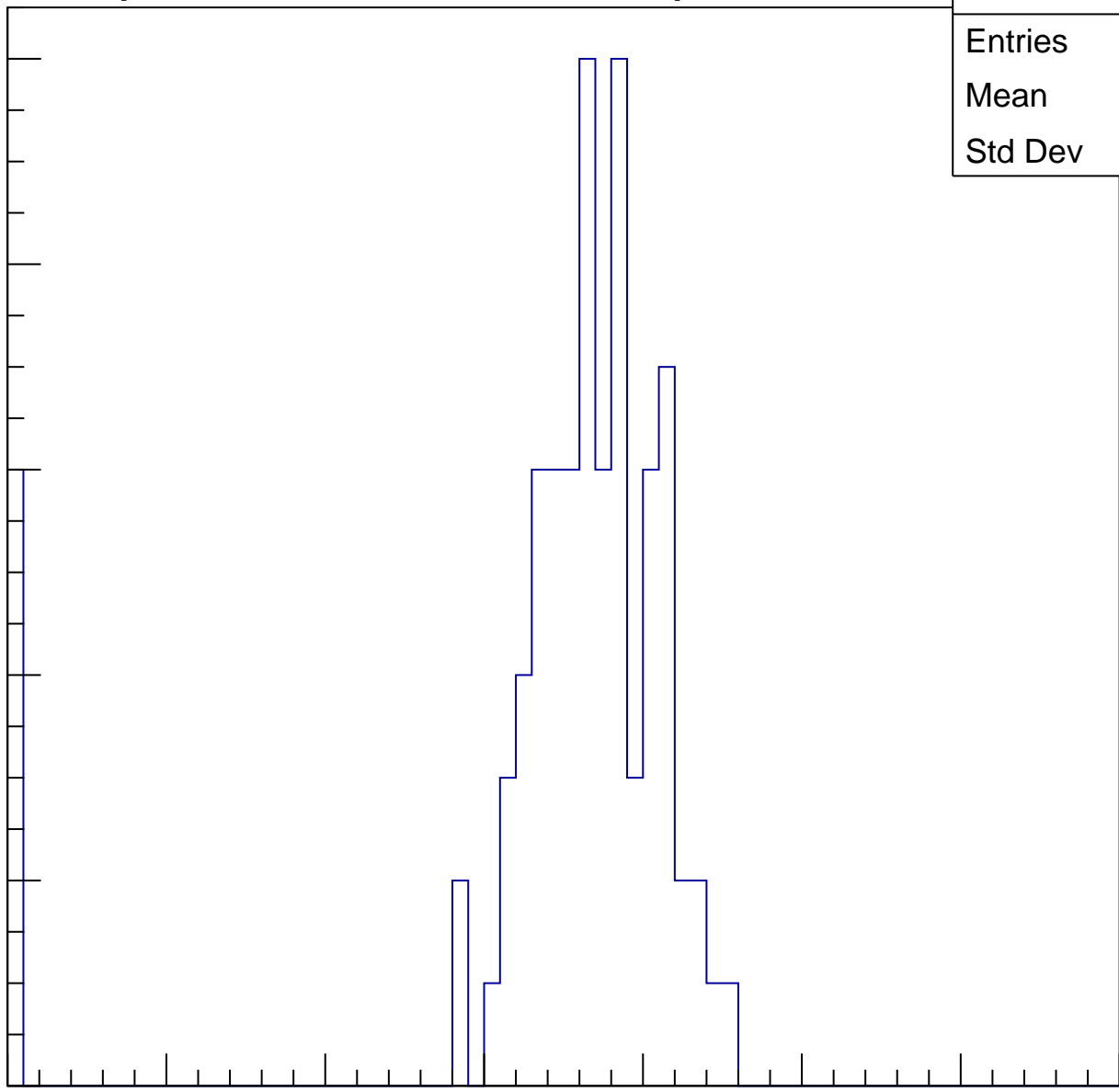
40

50

60

70

ampl

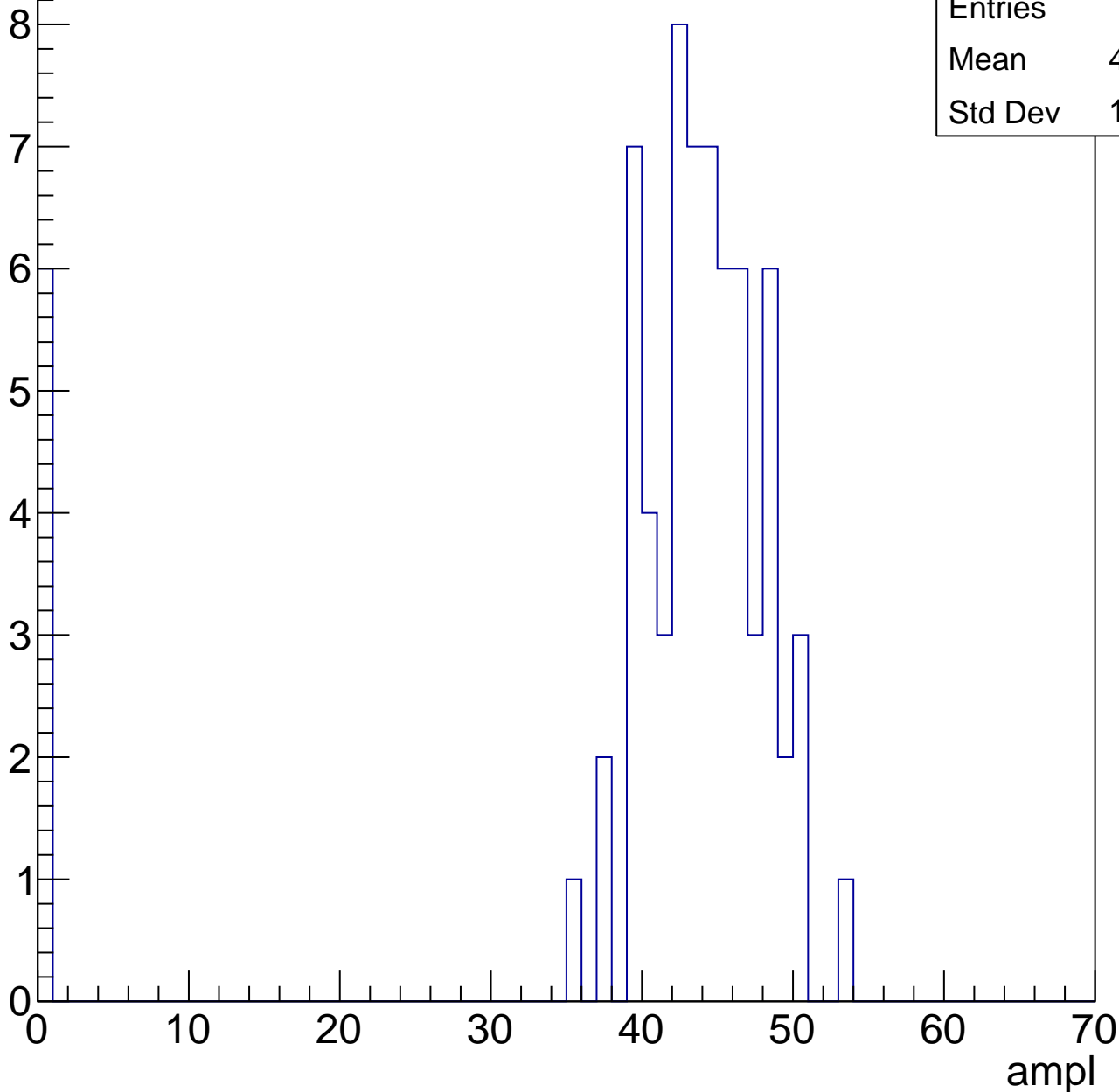


B1L103S, U11-ch6, adc2

calib_packv5_041523_1651.root, FC#0, port C2

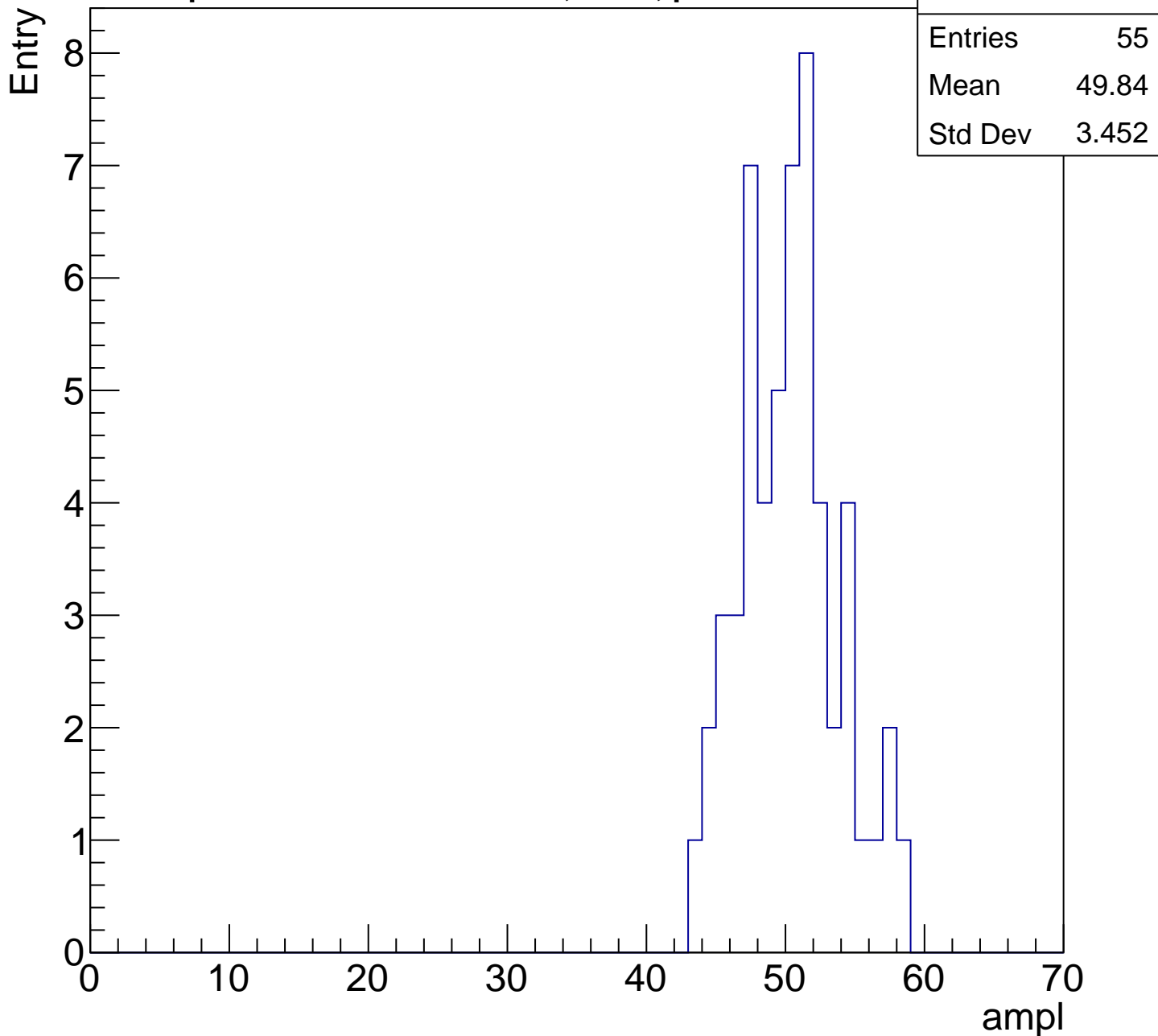
Entry

Entries	72
Mean	40.08
Std Dev	12.58



B1L103S, U11-ch6, adc3

calib_packv5_041523_1651.root, FC#0, port C2

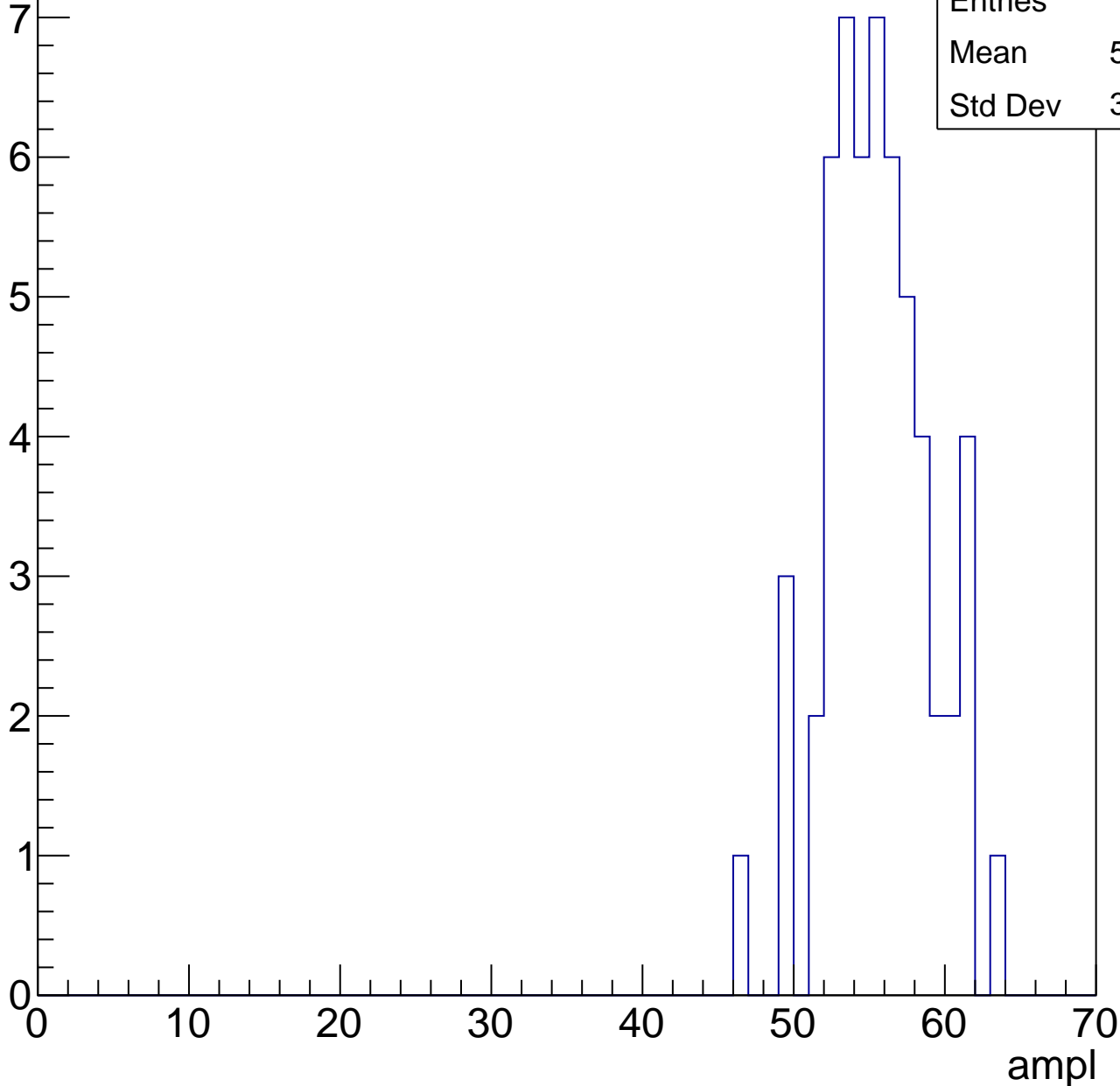


B1L103S, U11-ch6, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	55.09
Std Dev	3.434



B1L103S, U11-ch6, adc5

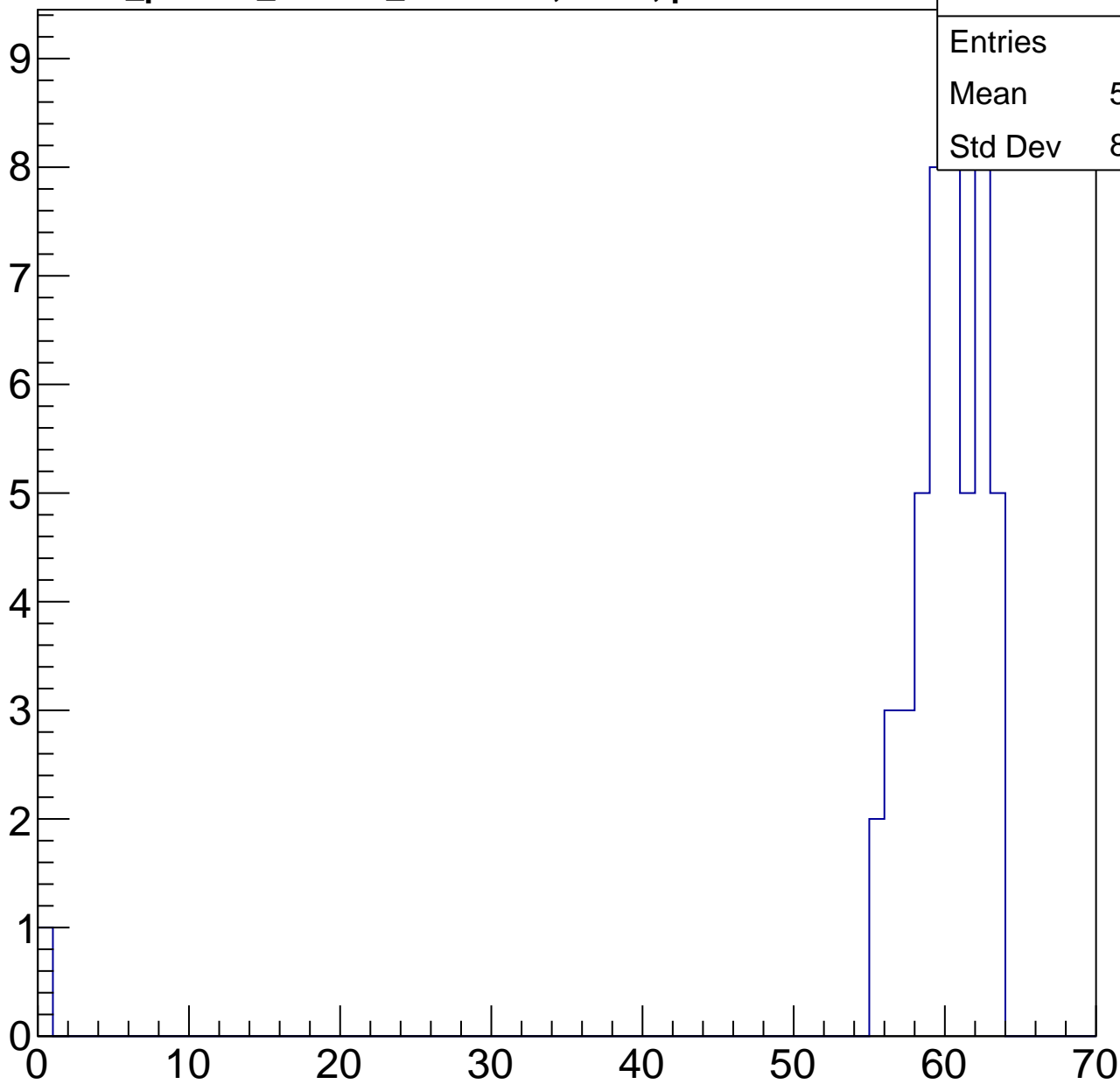
calib_packv5_041523_1651.root, FC#0, port C2

Entry

9
8
7
6
5
4
3
2
1
0

Entries	49
Mean	58.55
Std Dev	8.732

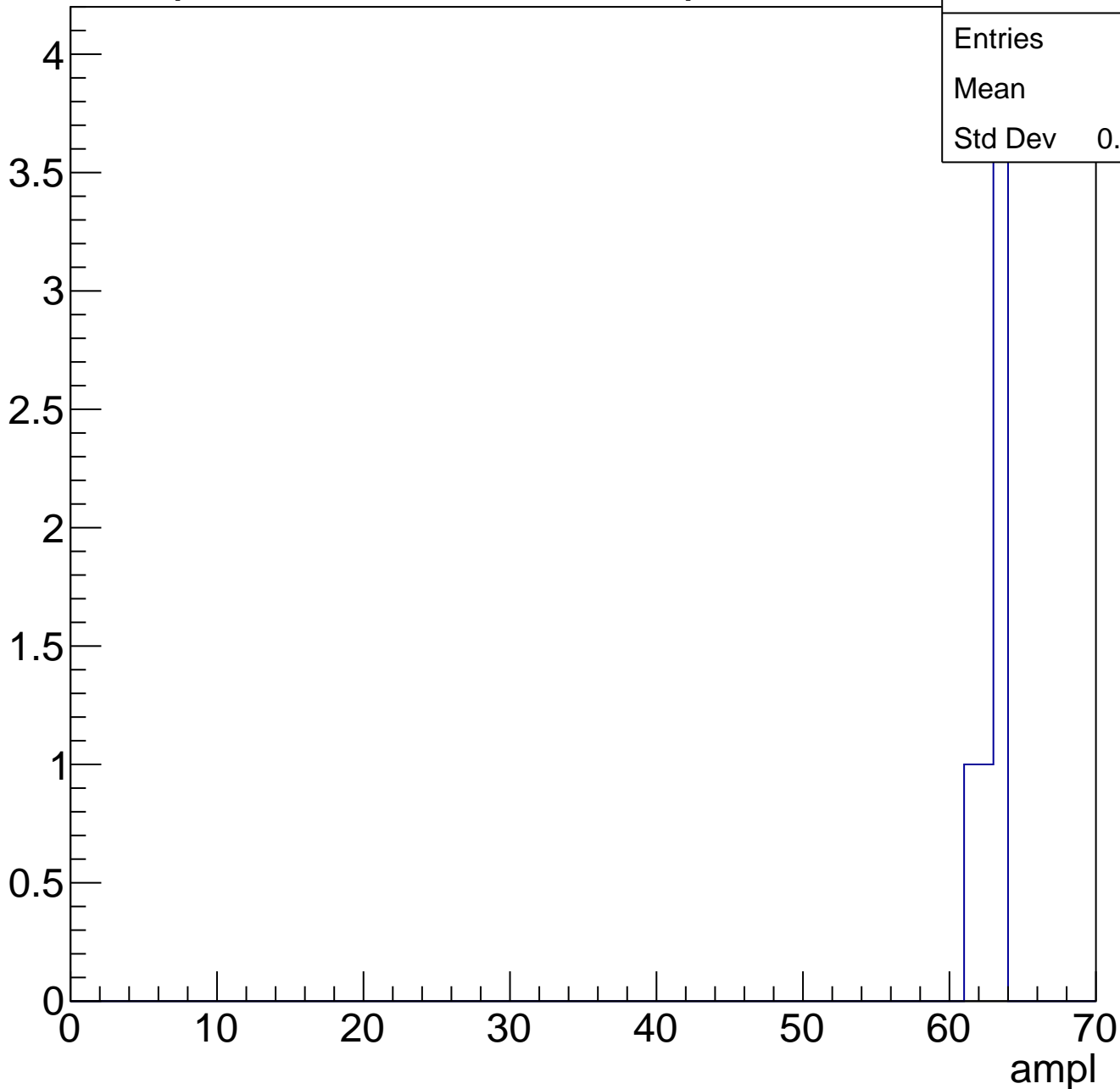
ampl



B1L103S, U11-ch6, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch6, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch7, adc0

calib_packv5_041523_1651.root, FC#0, port C2

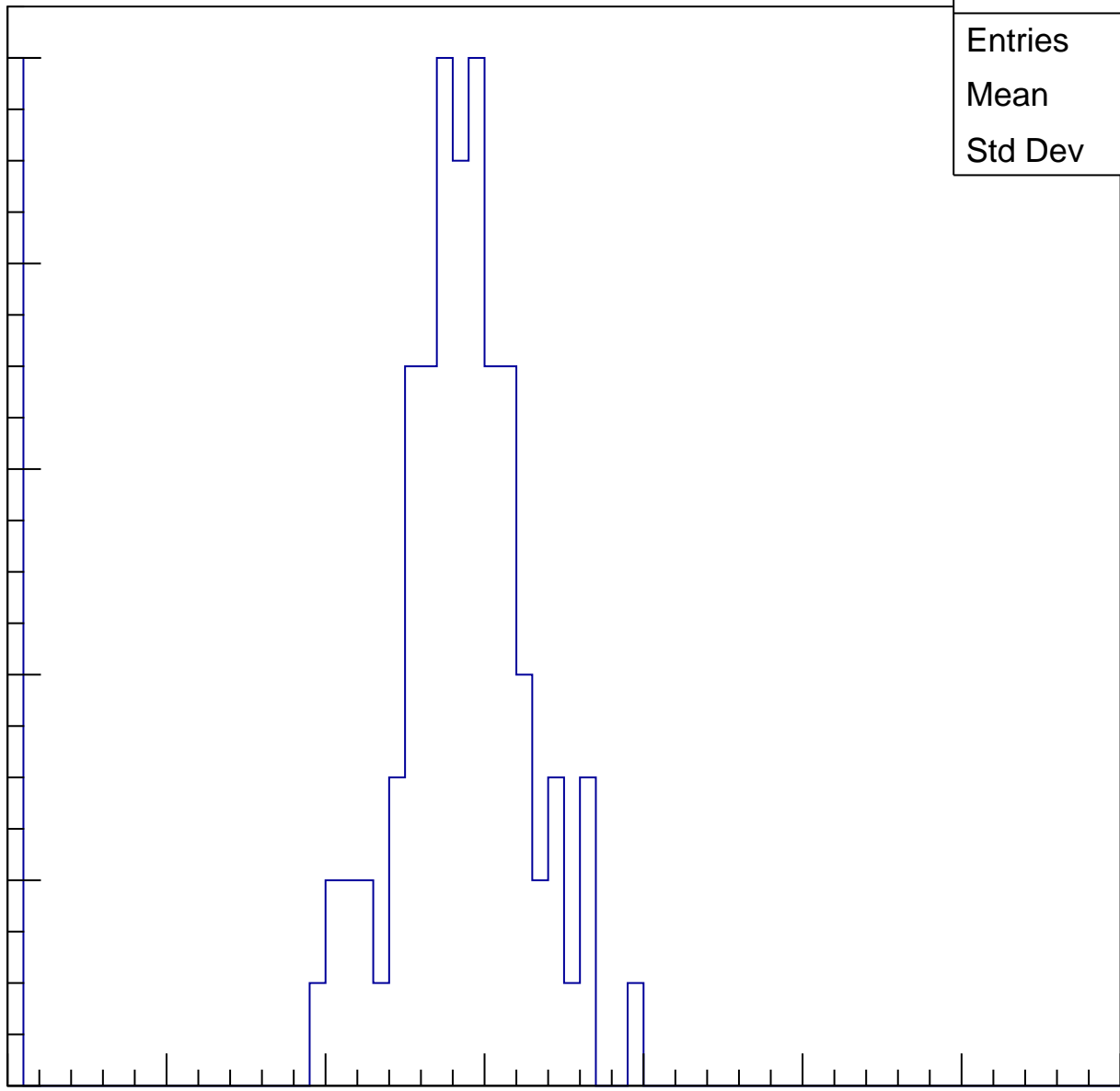
Entries	92
Mean	25.15
Std Dev	9.517

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

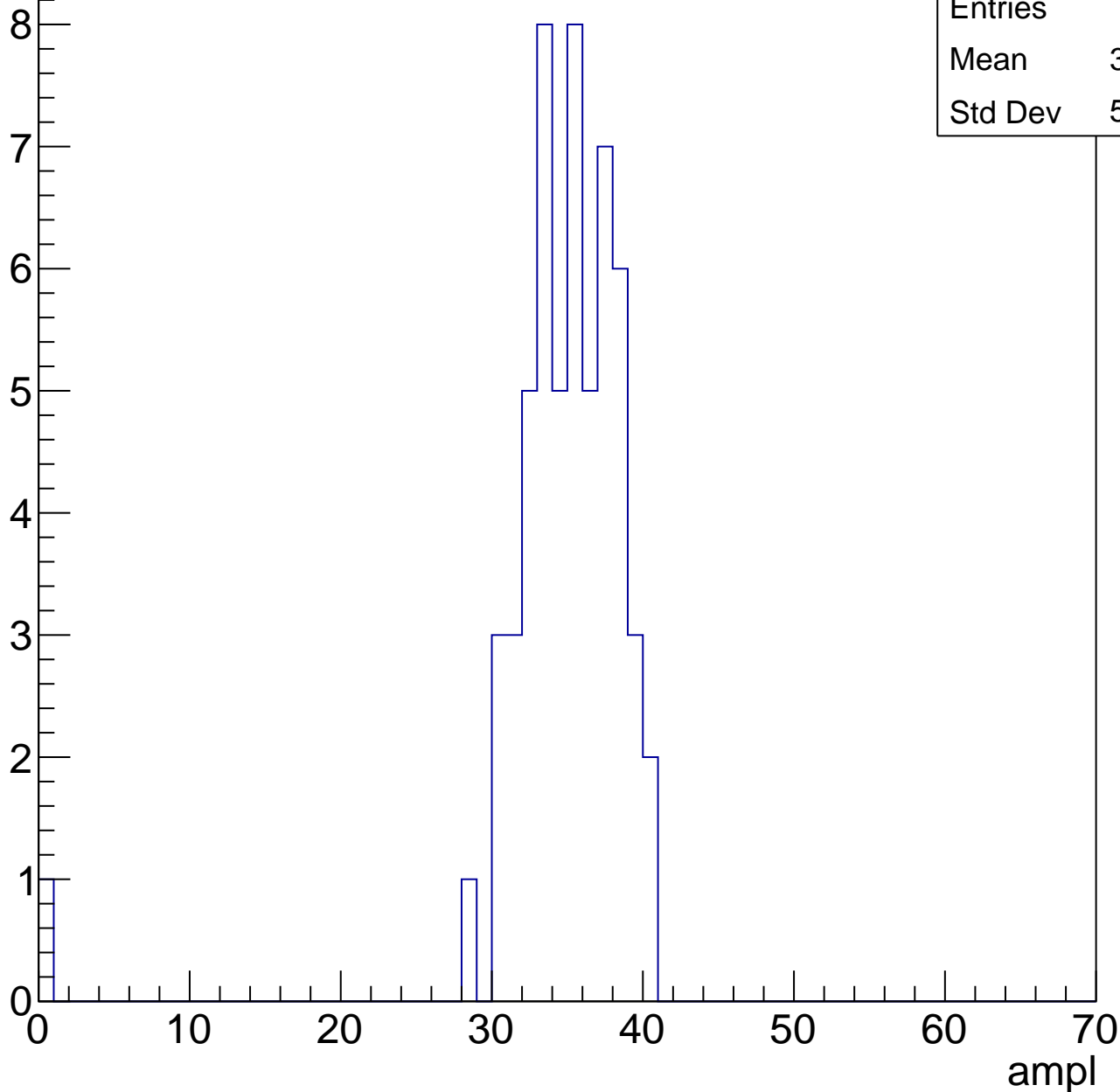


B1L103S, U11-ch7, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	34.19
Std Dev	5.342

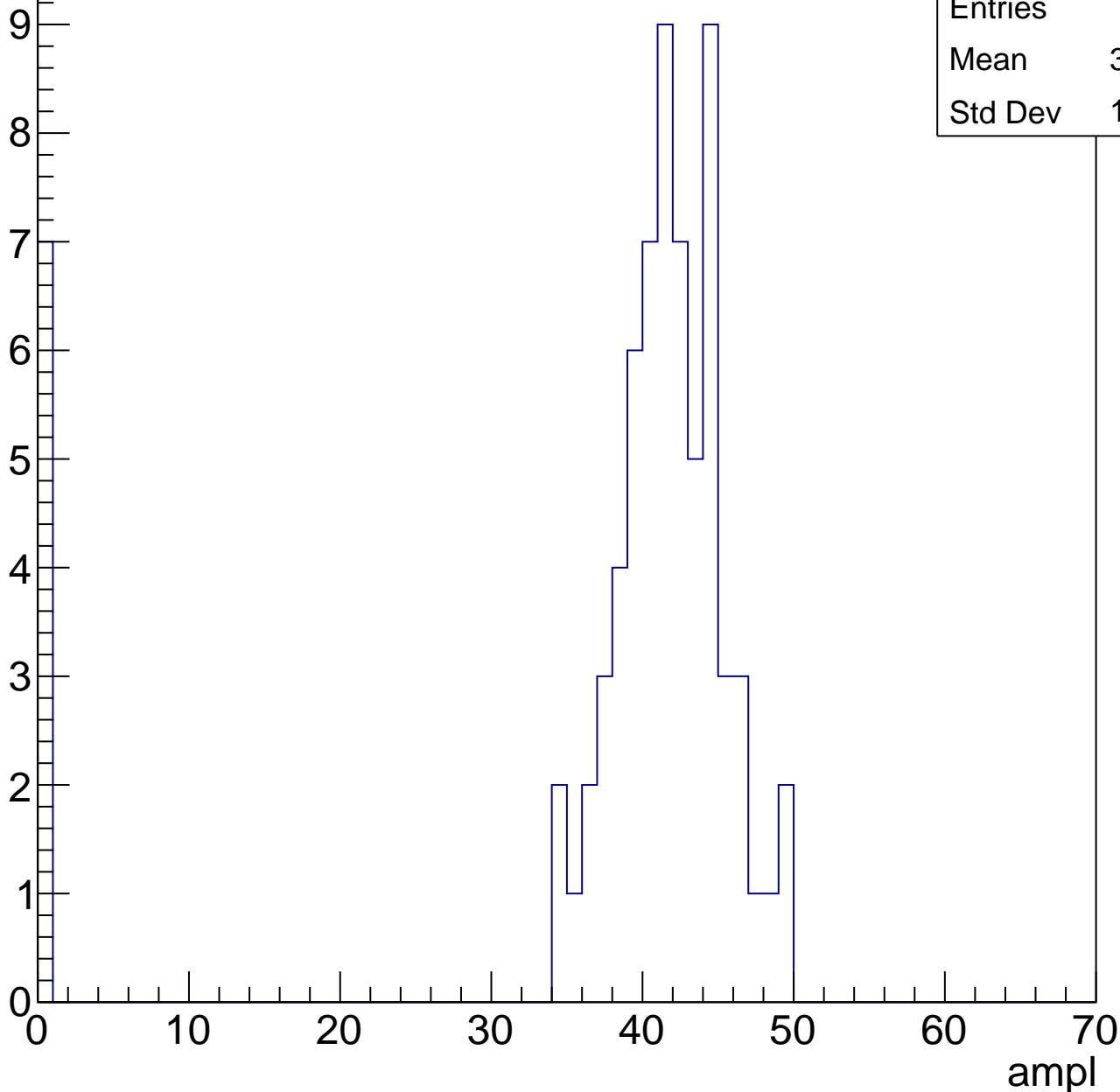


B1L103S, U11-ch7, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	37.39
Std Dev	12.68

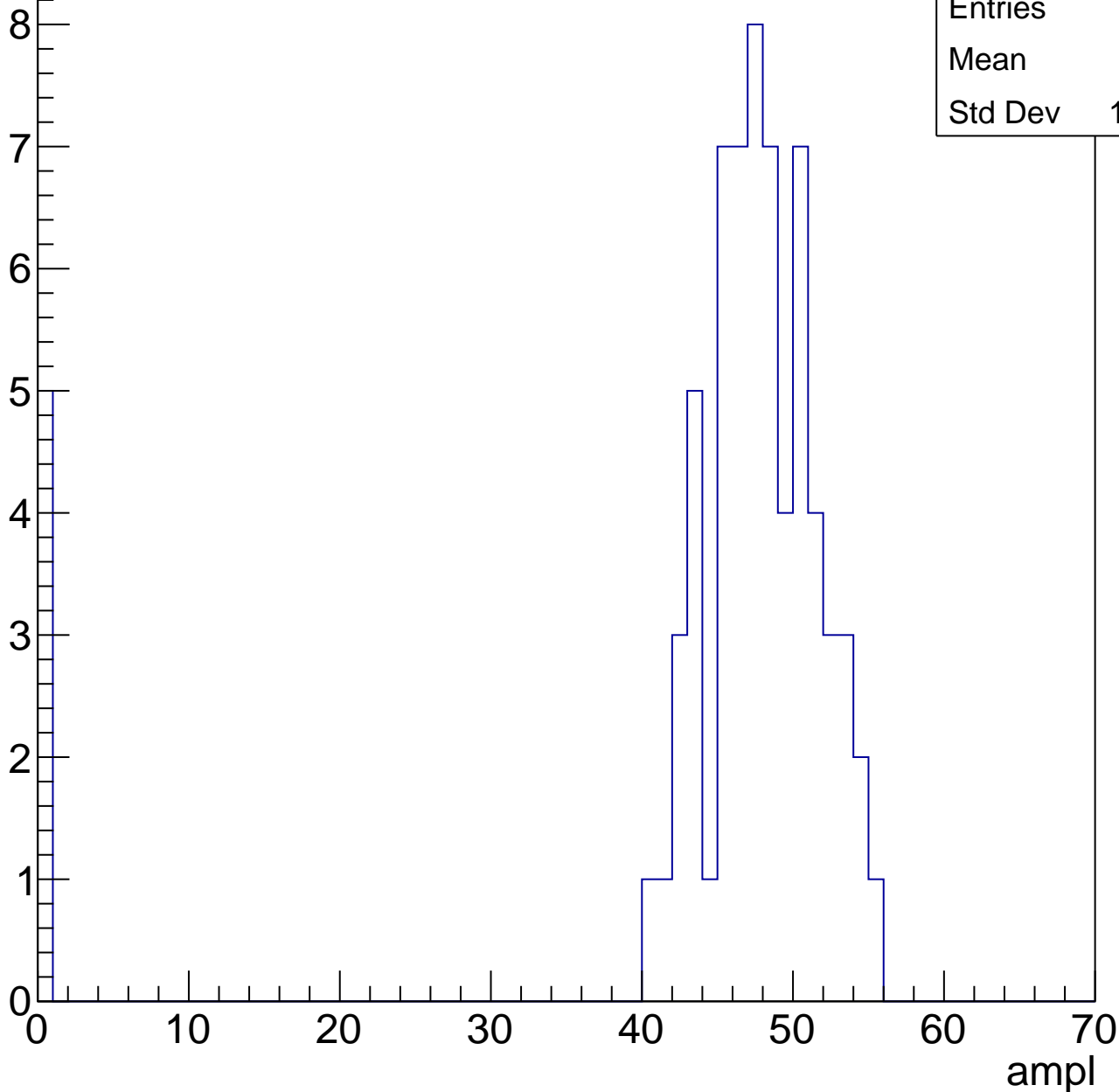


B1L103S, U11-ch7, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	44.1
Std Dev	12.77

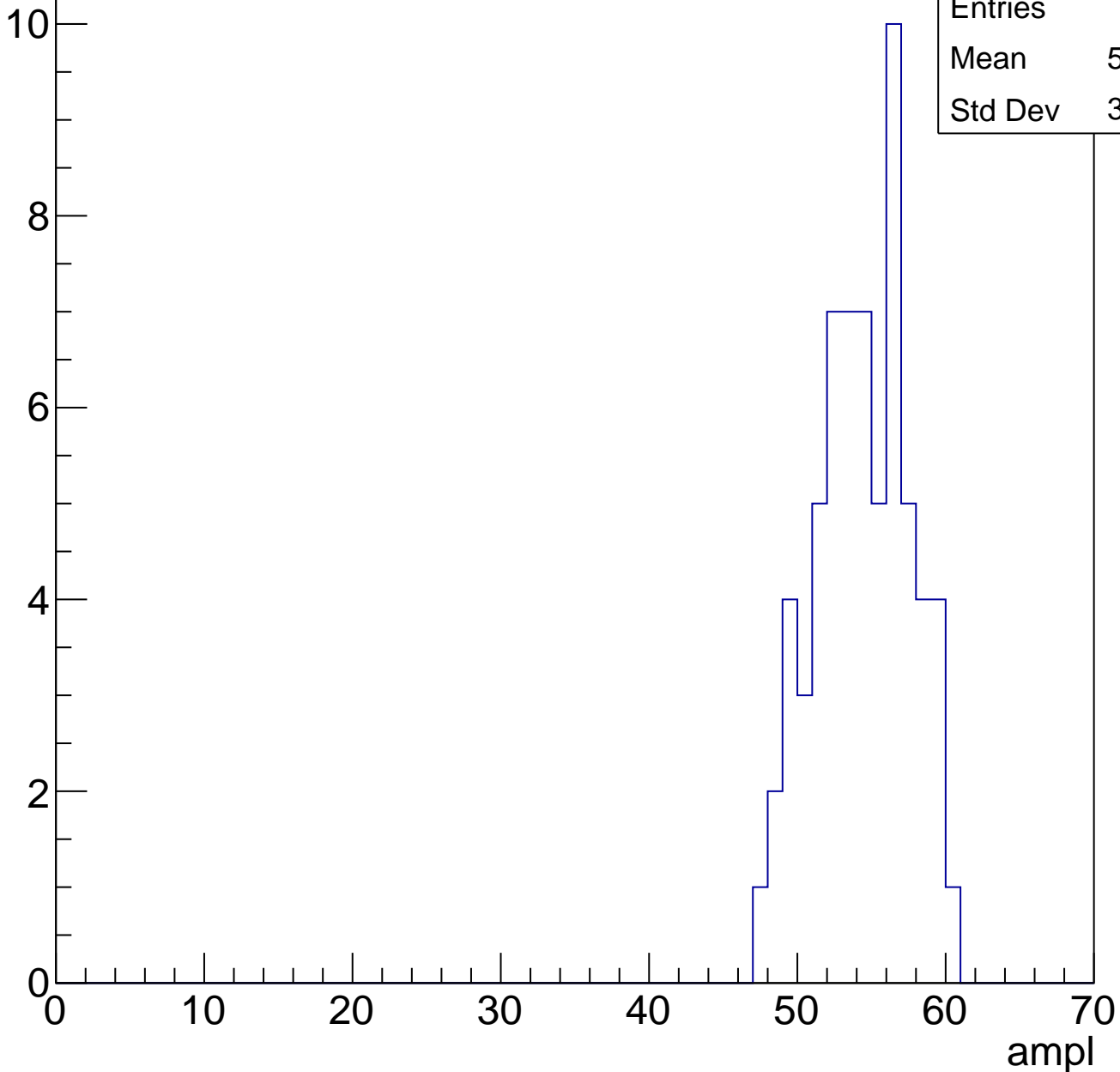


B1L103S, U11-ch7, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	65
Mean	53.92
Std Dev	3.134

Entry

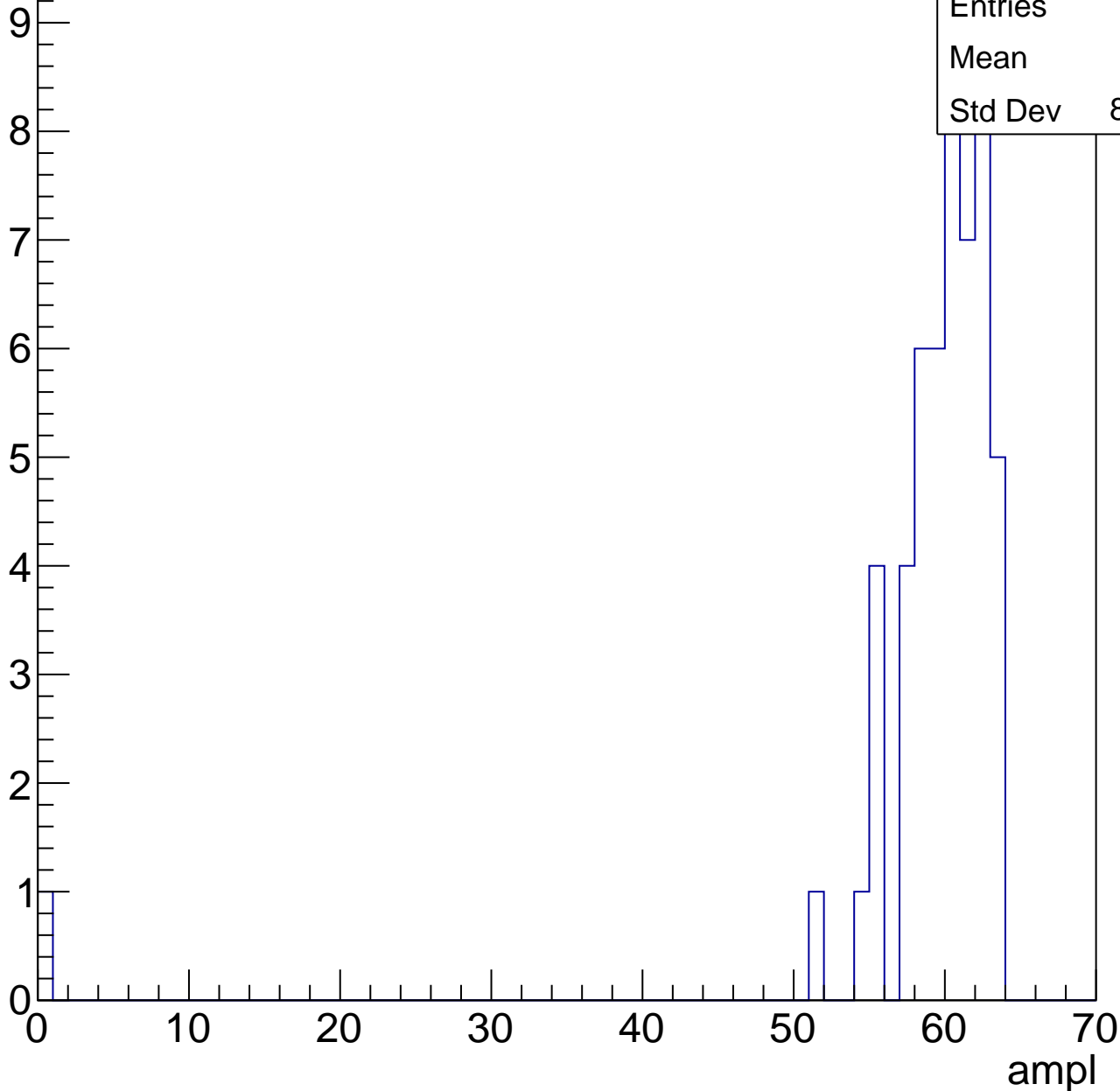


B1L103S, U11-ch7, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	58.4
Std Dev	8.506

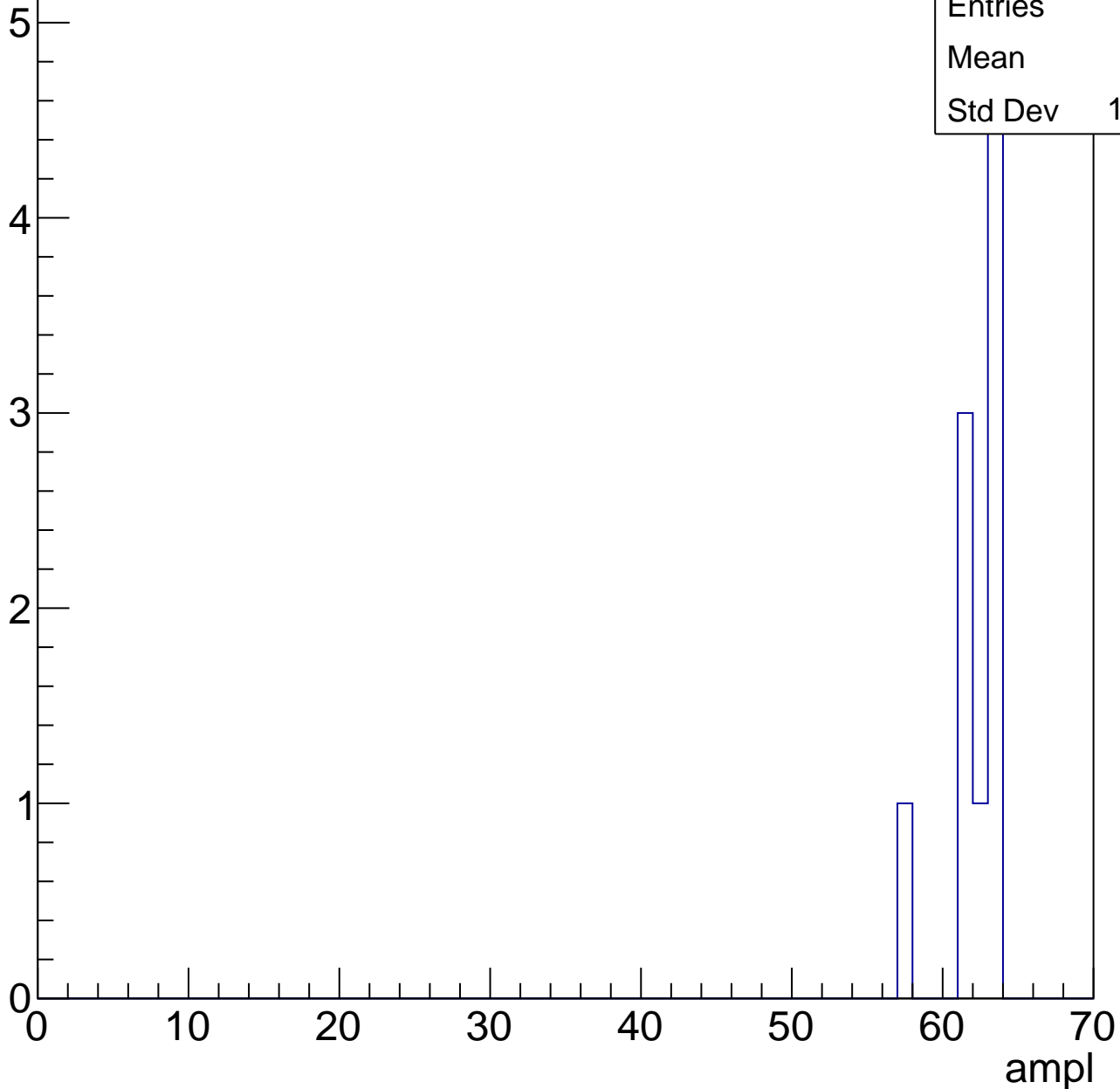


B1L103S, U11-ch7, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	10
Mean	61.7
Std Dev	1.792



B1L103S, U11-ch7, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

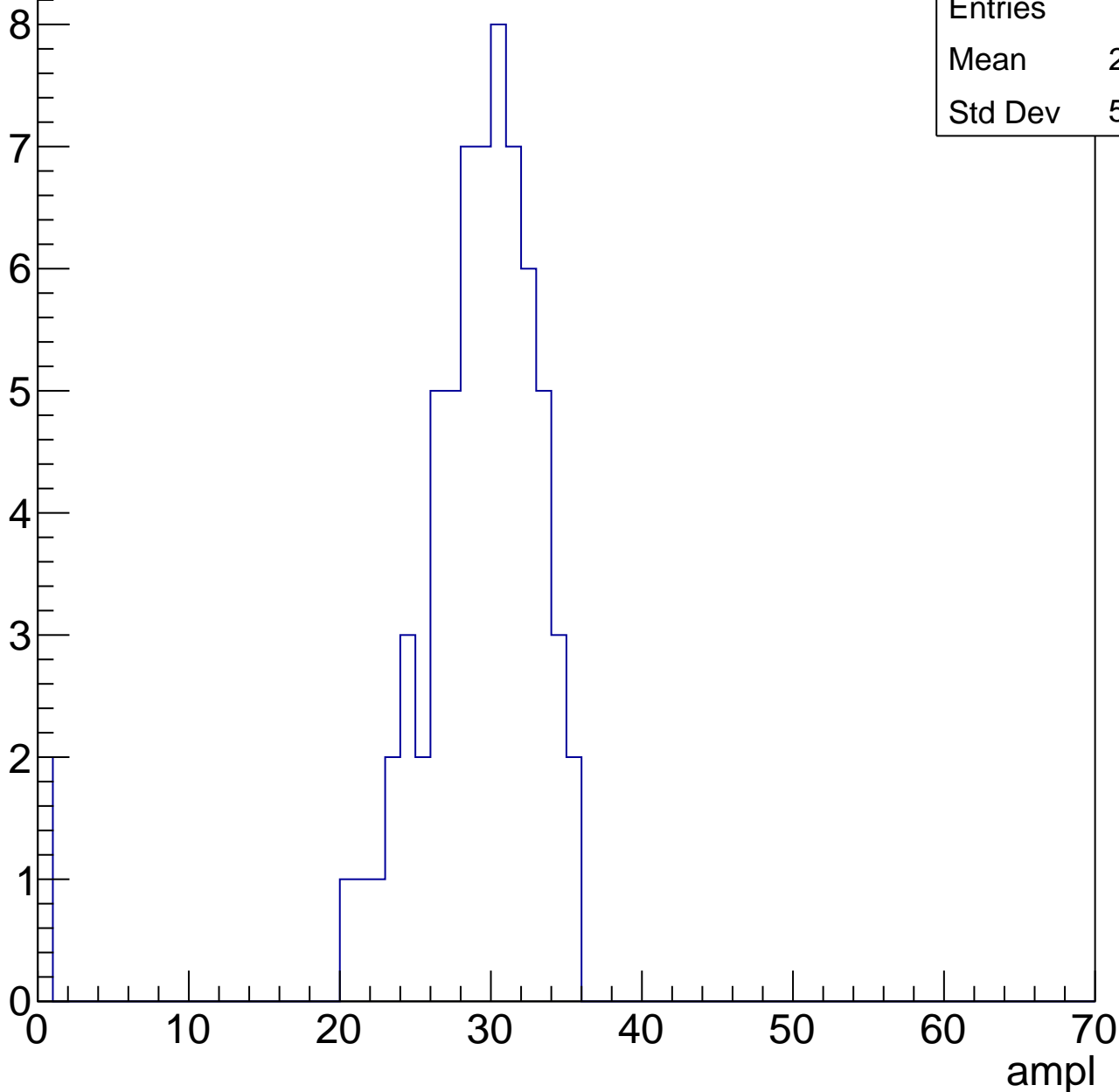
ampl

B1L103S, U11-ch8, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	28.07
Std Dev	5.968

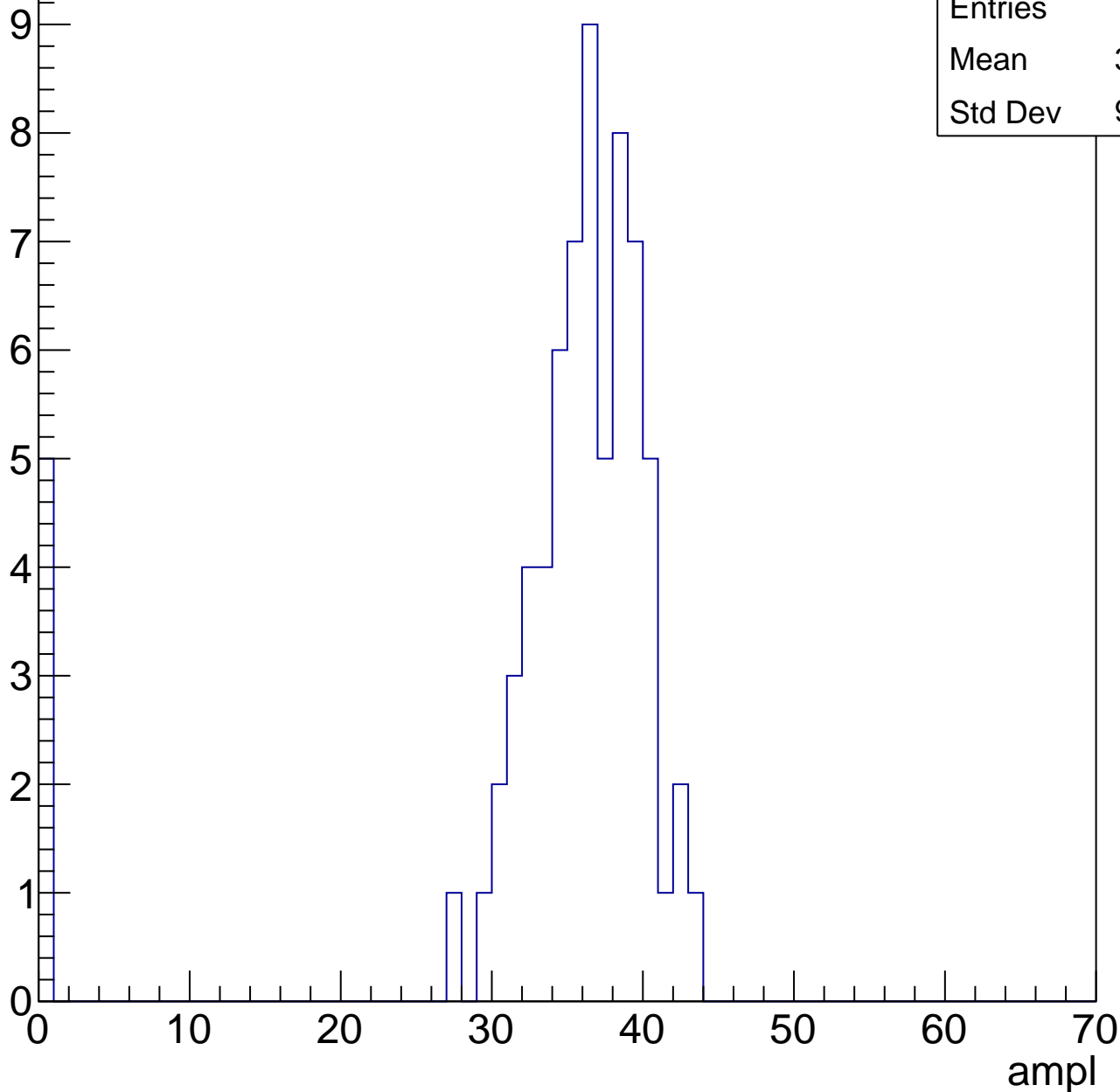


B1L103S, U11-ch8, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	33.41
Std Dev	9.741

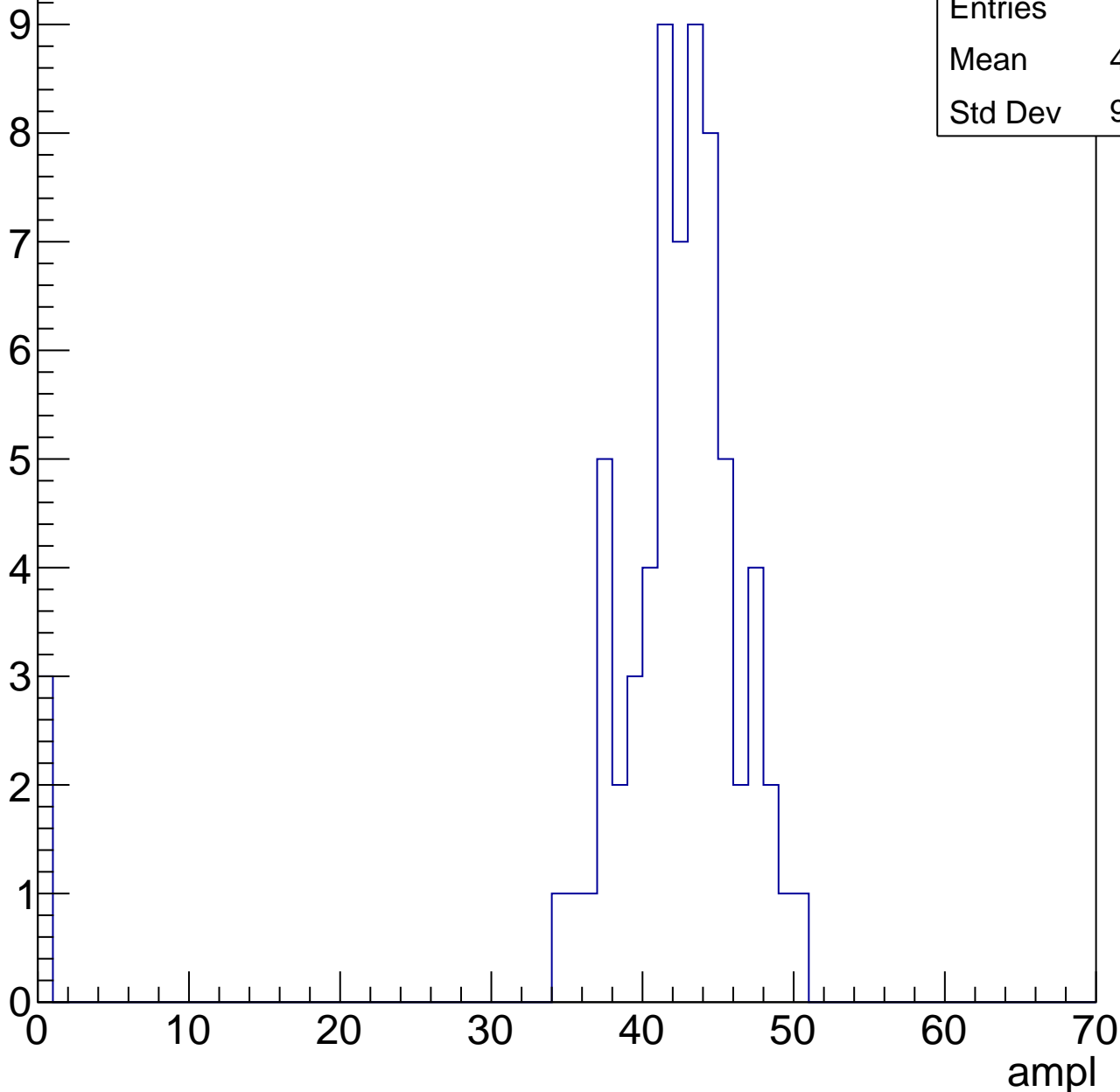


B1L103S, U11-ch8, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	40.37
Std Dev	9.292

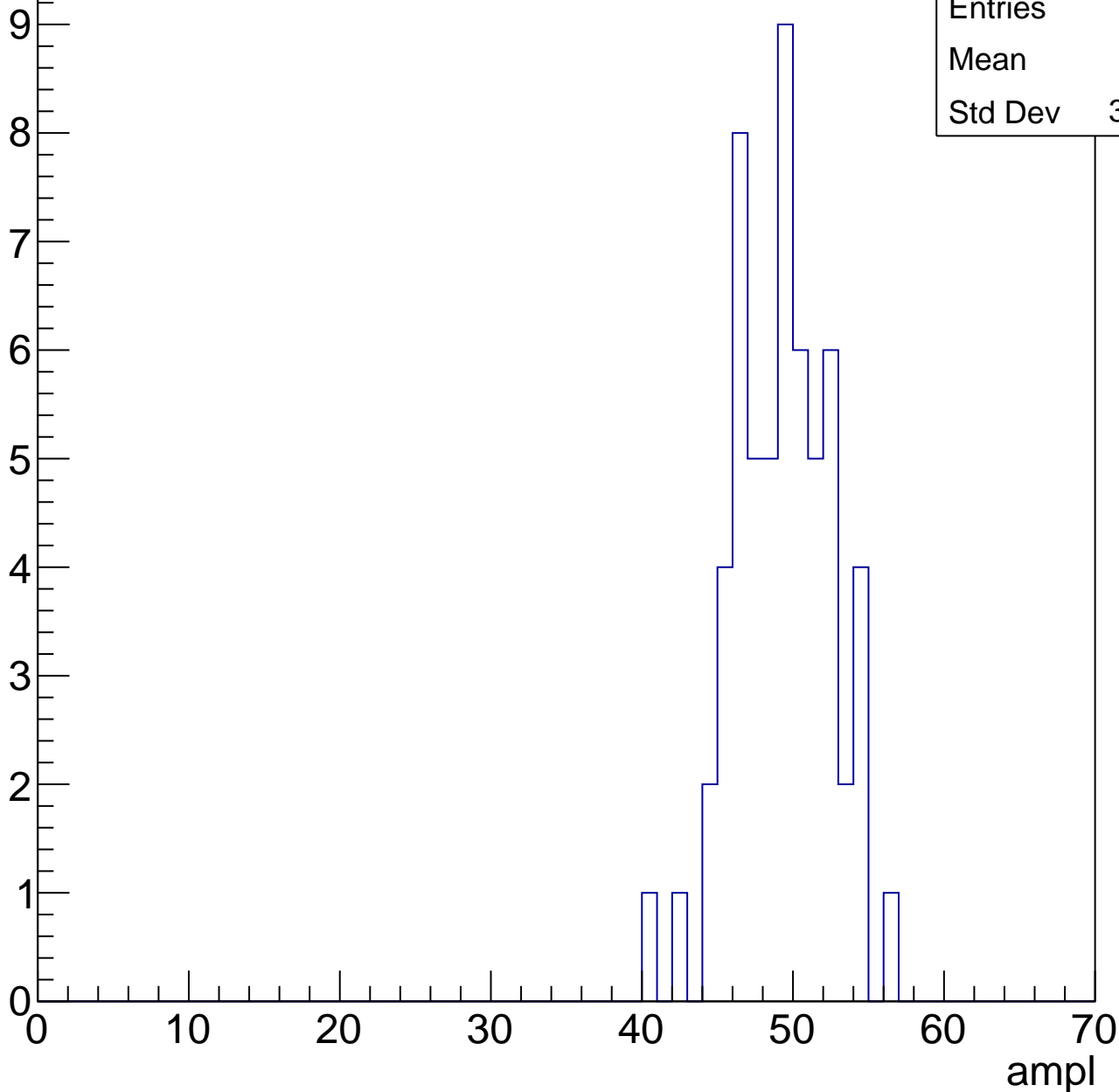


B1L103S, U11-ch8, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	48.8
Std Dev	3.188

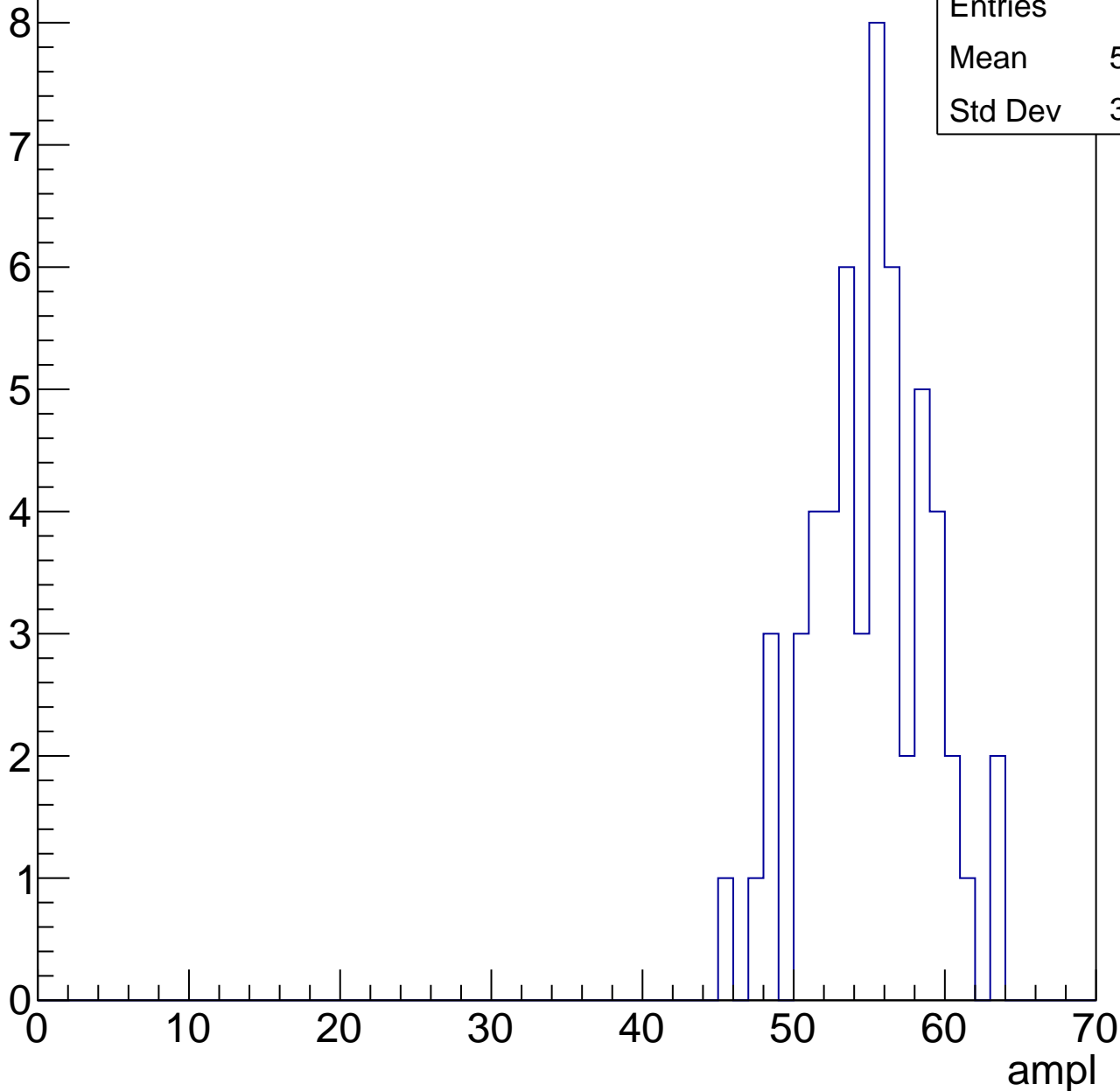


B1L103S, U11-ch8, adc4

calib_packv5_041523_1651.root, FC#0, port C2

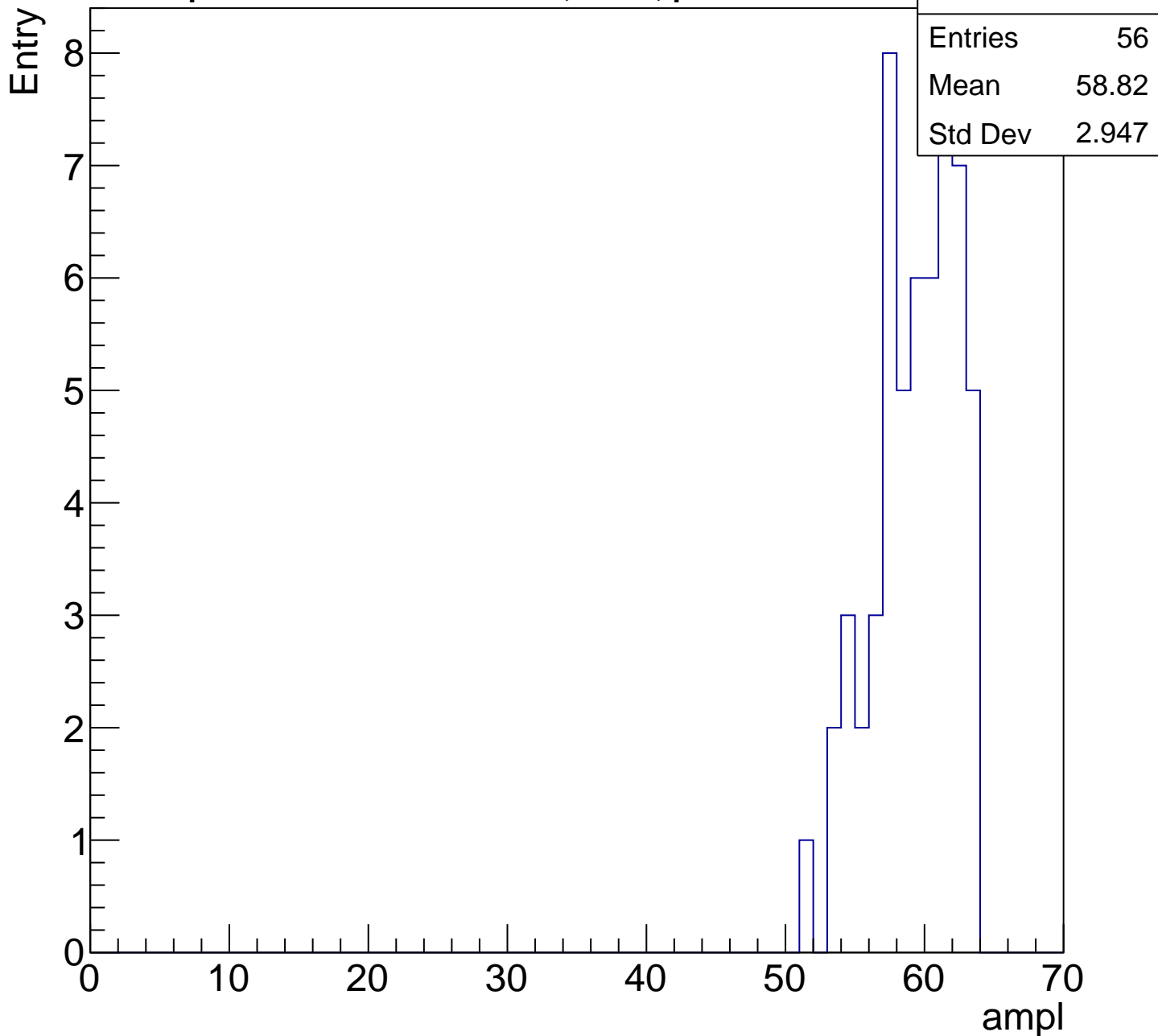
Entry

Entries	55
Mean	54.56
Std Dev	3.907



B1L103S, U11-ch8, adc5

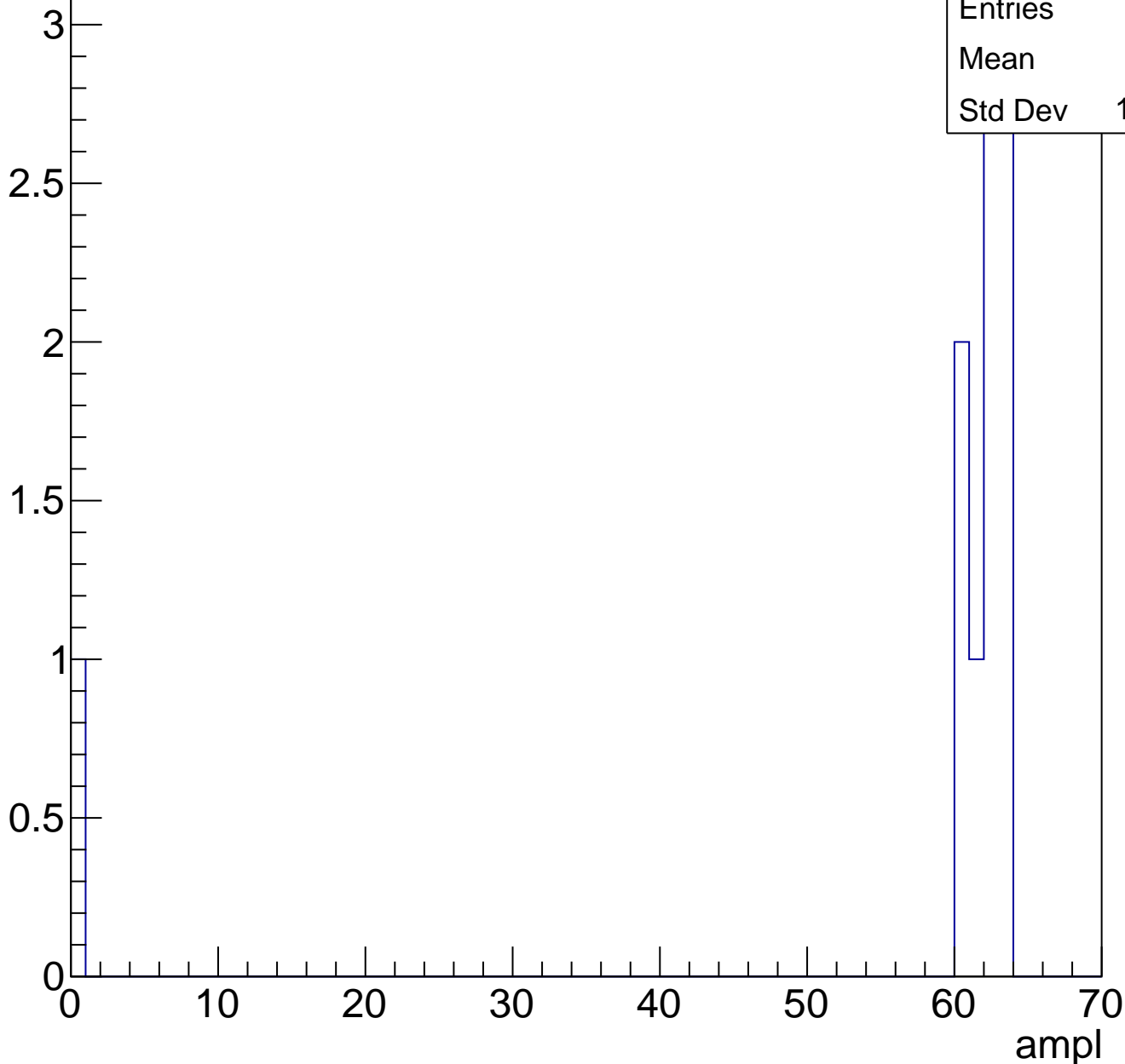
calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U11-ch8, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch8, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	18
Mean	0
Std Dev	0

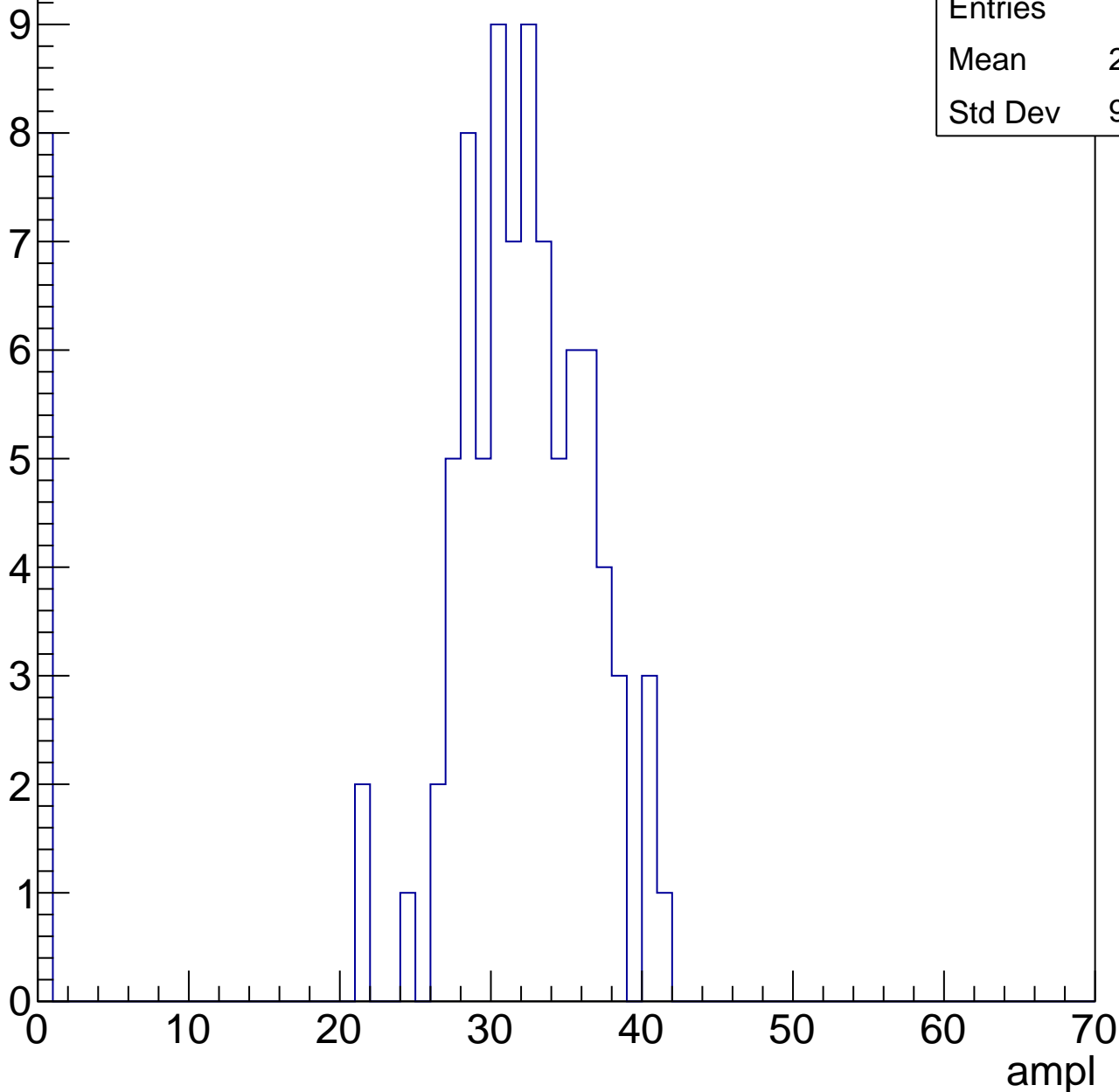
ampl

B1L103S, U11-ch9, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	91
Mean	29.09
Std Dev	9.832

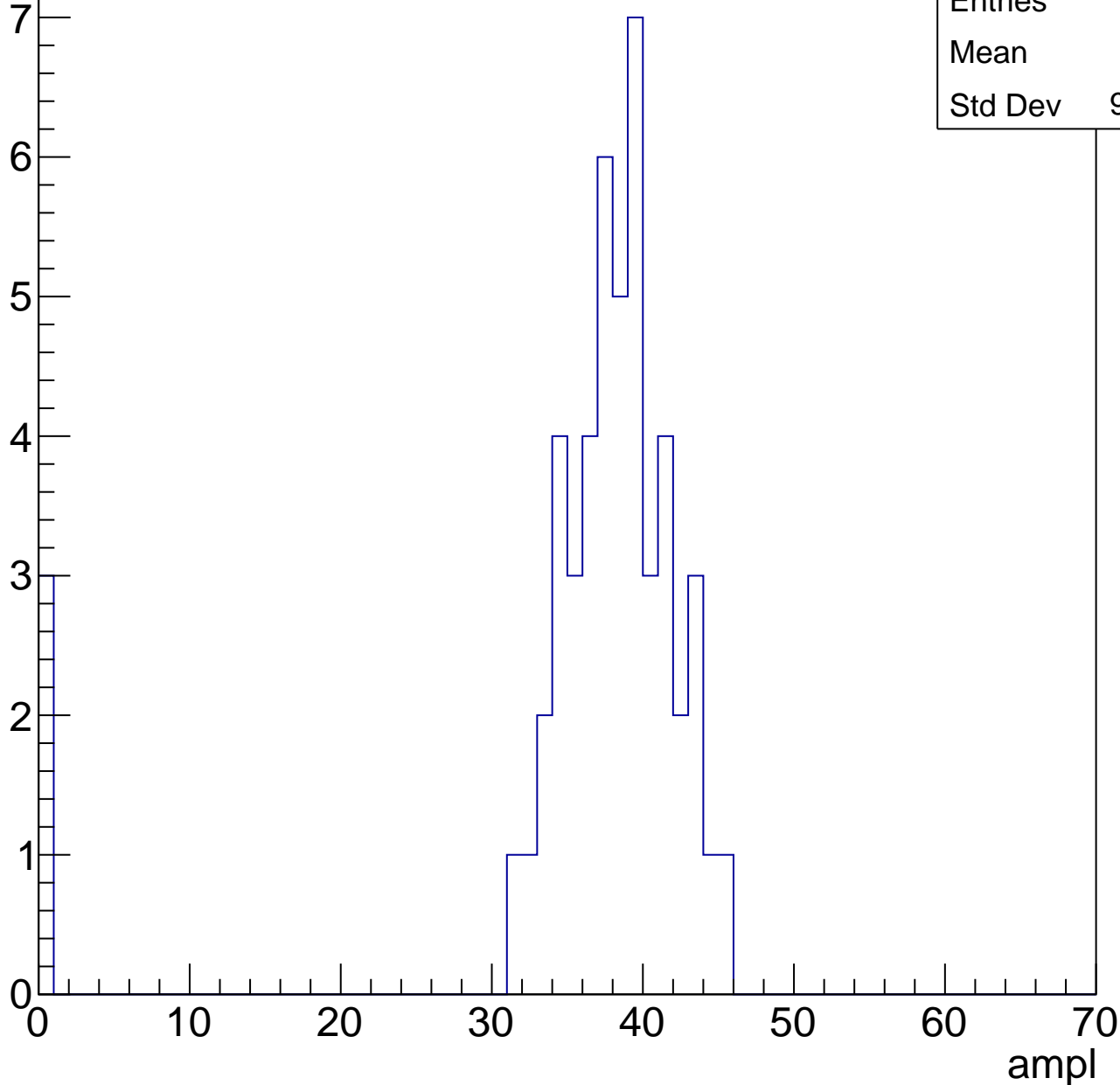


B1L103S, U11-ch9, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	35.7
Std Dev	9.552

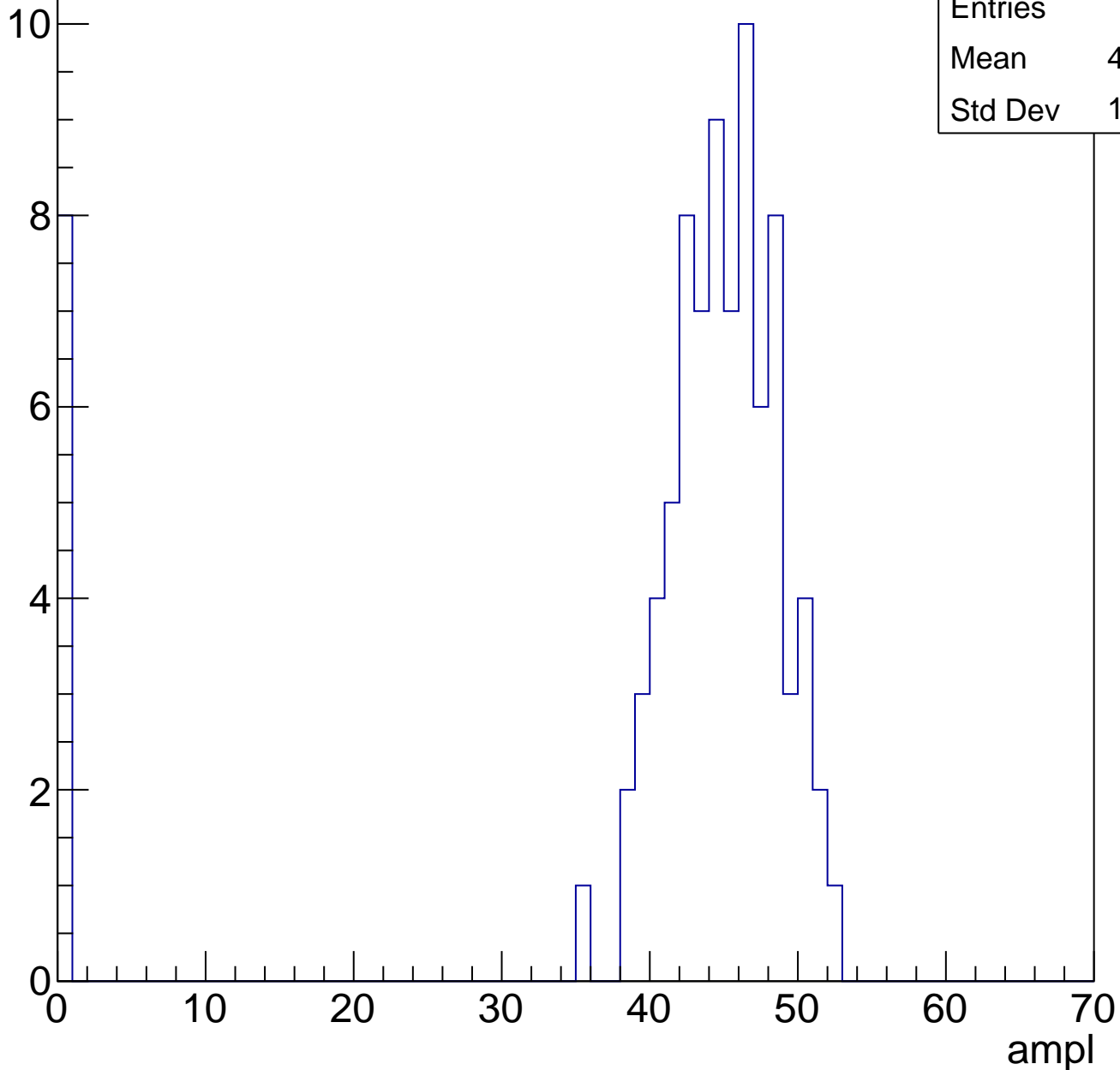


B1L103S, U11-ch9, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	88
Mean	40.55
Std Dev	13.24

Entry

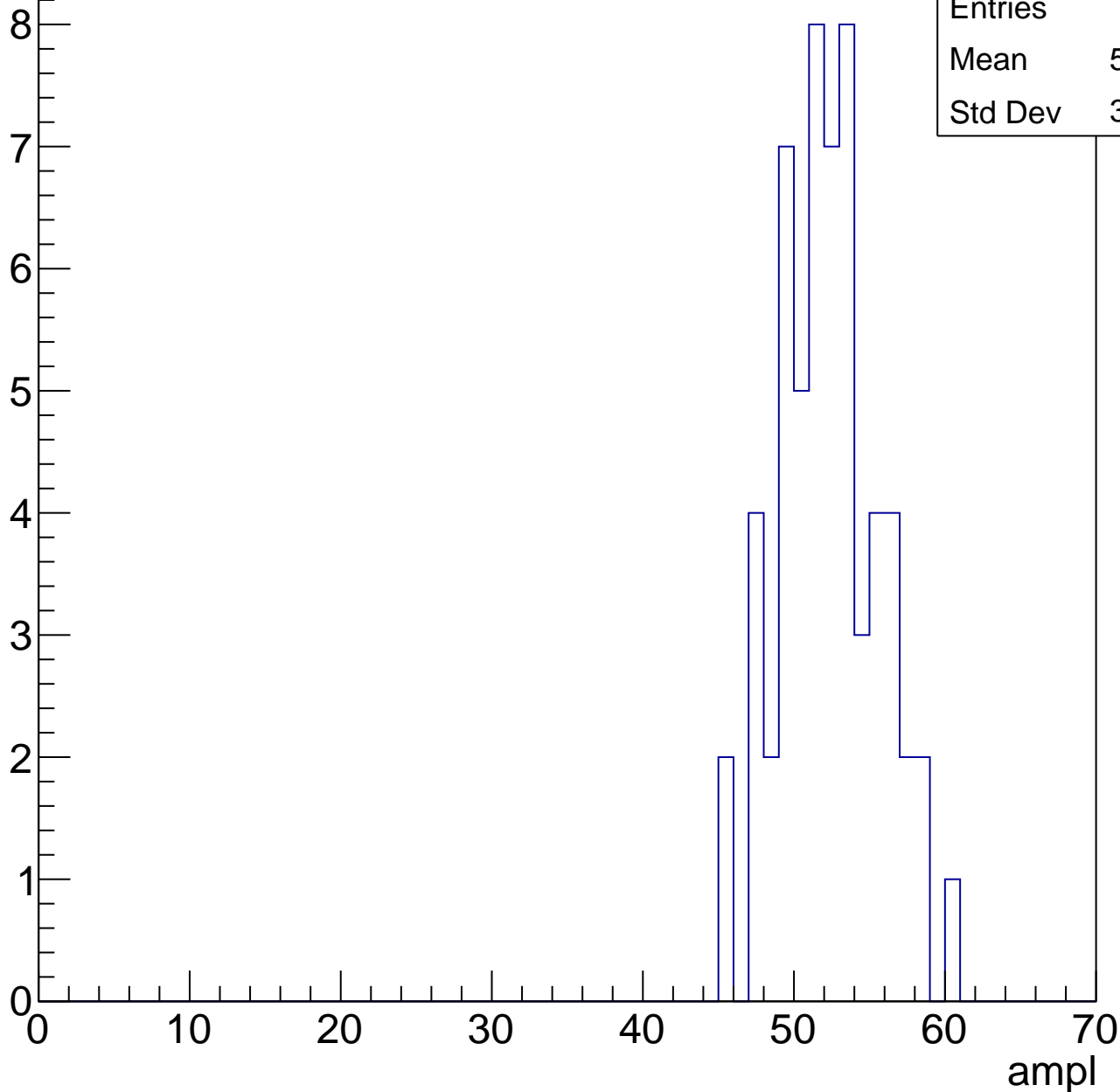


B1L103S, U11-ch9, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	51.85
Std Dev	3.256



B1L103S, U11-ch9, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	61
Mean	57.44
Std Dev	2.956

Entry

10

8

6

4

2

0

0

10

20

30

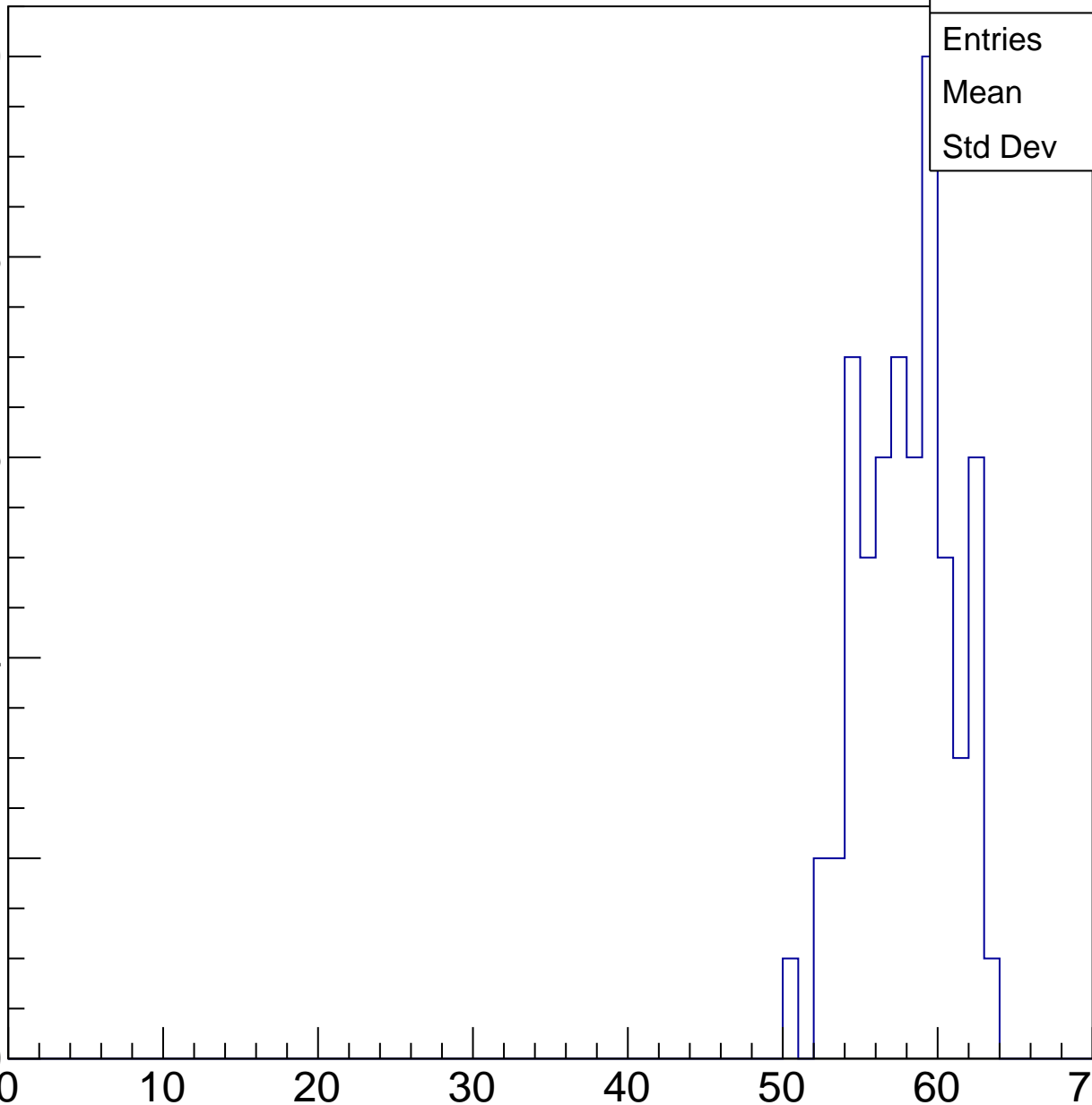
40

50

60

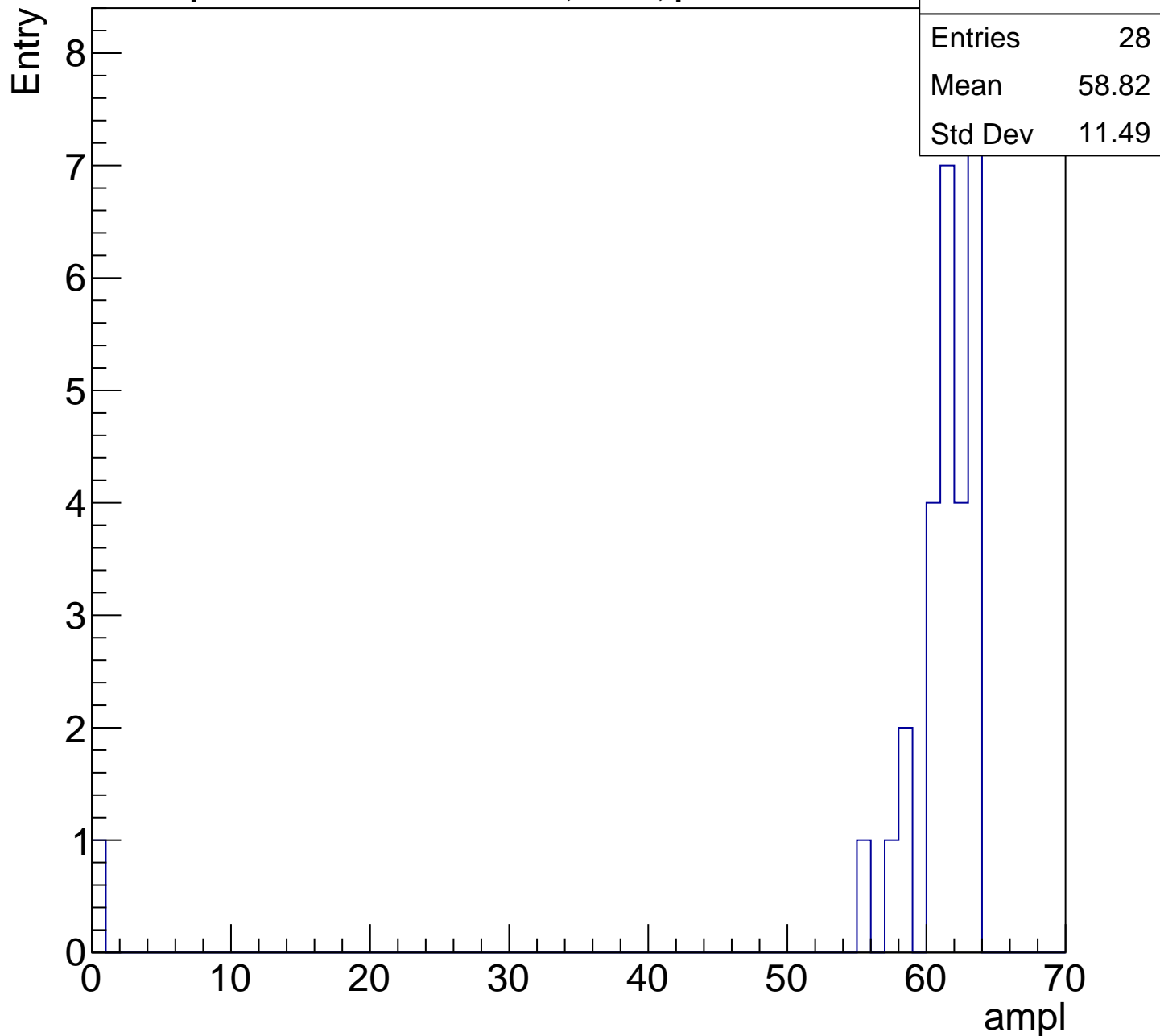
70

ampl



B1L103S, U11-ch9, adc5

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U11-ch9, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch9, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	18
Mean	0
Std Dev	0

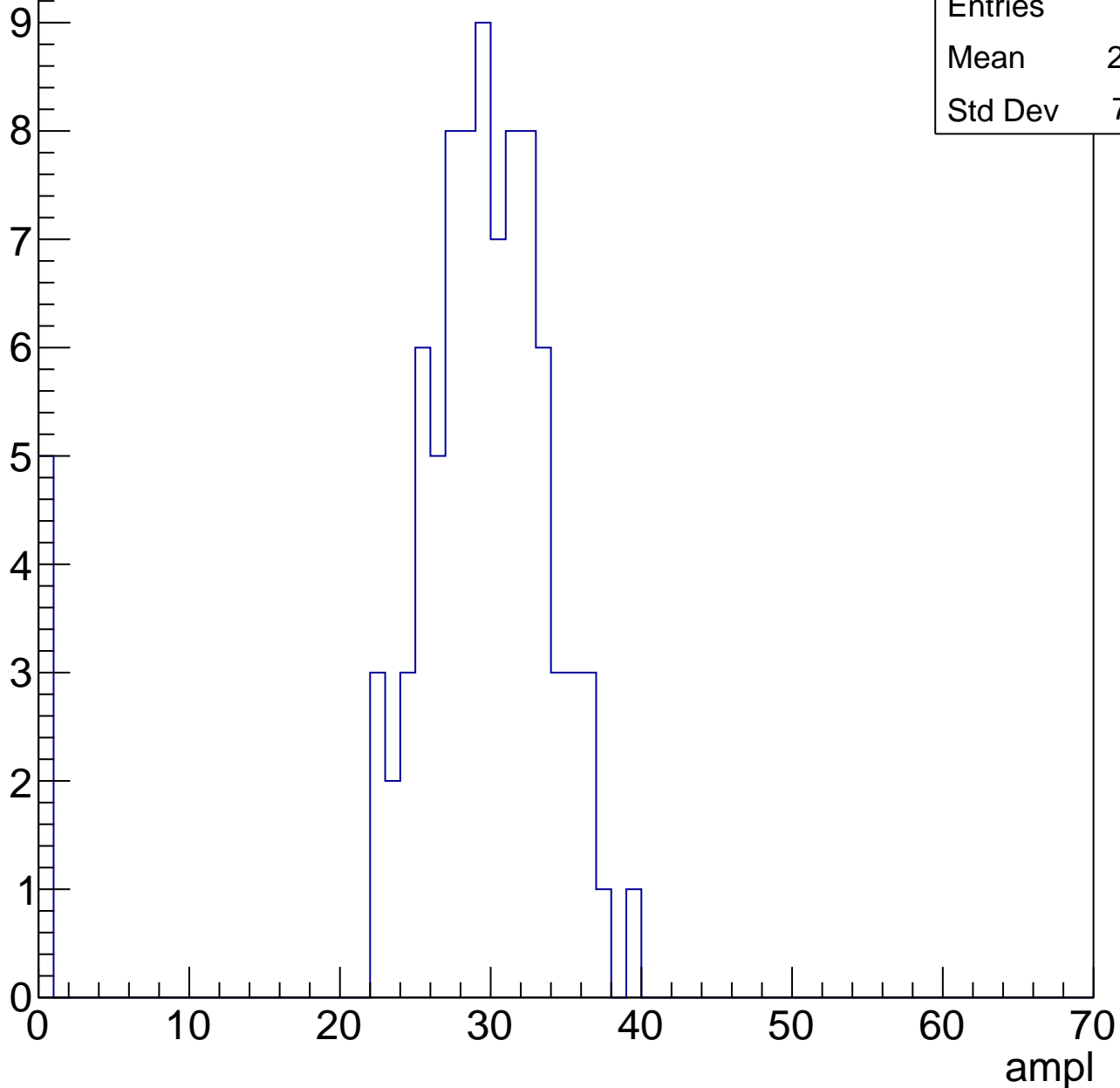
ampl

B1L103S, U11-ch10, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	89
Mean	27.73
Std Dev	7.671

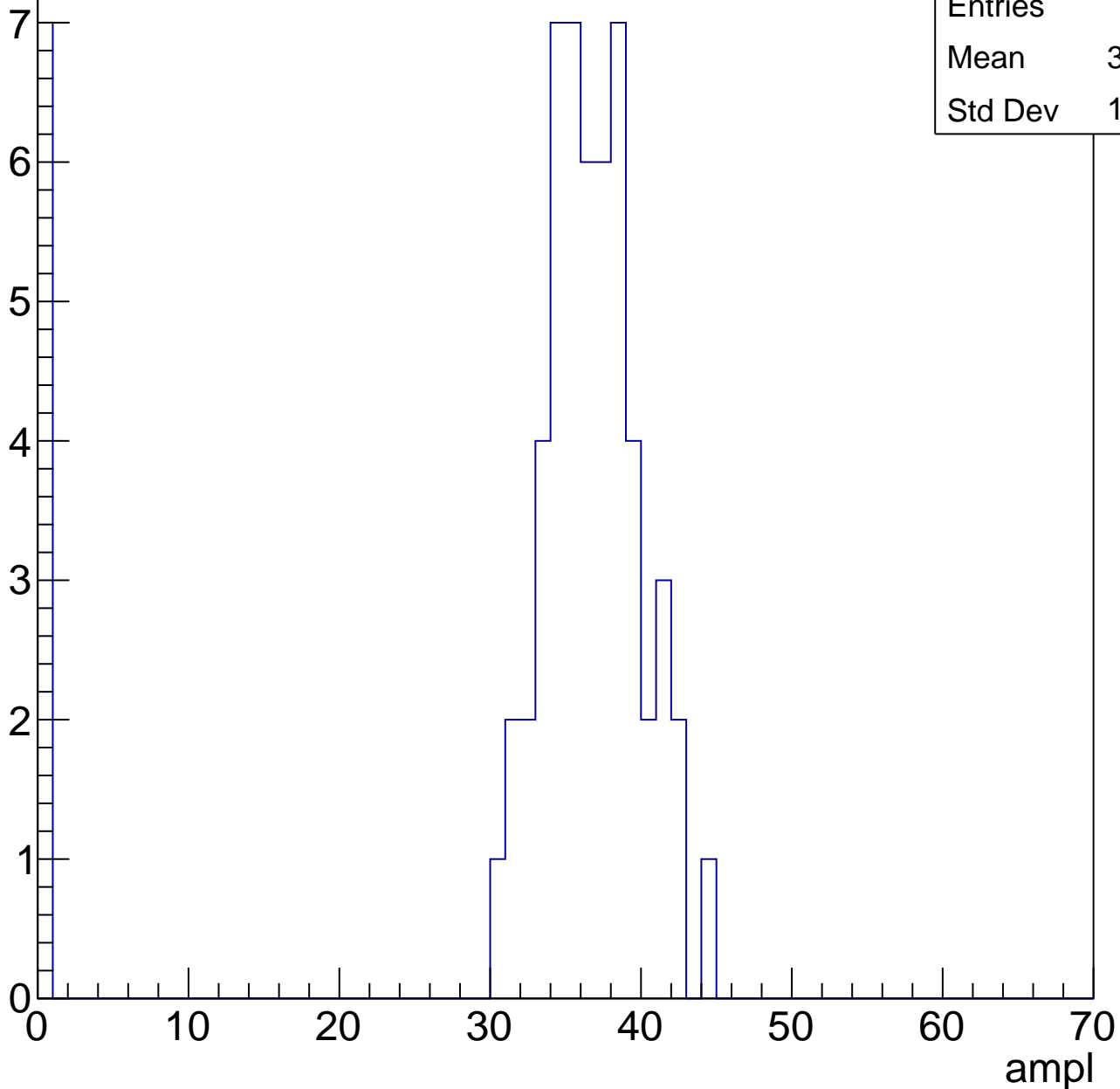


B1L103S, U11-ch10, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	32.16
Std Dev	11.93

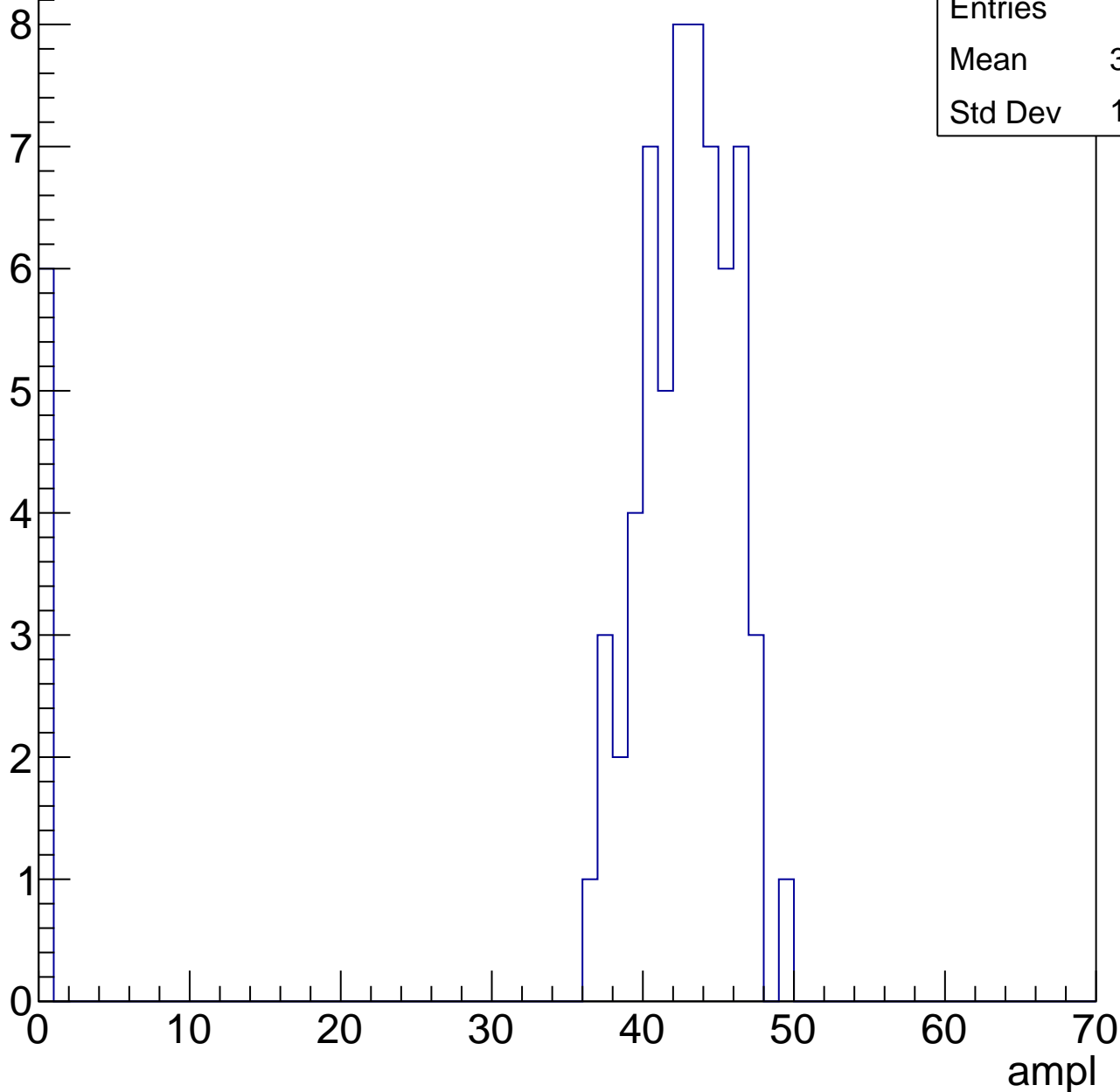


B1L103S, U11-ch10, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	38.74
Std Dev	12.37

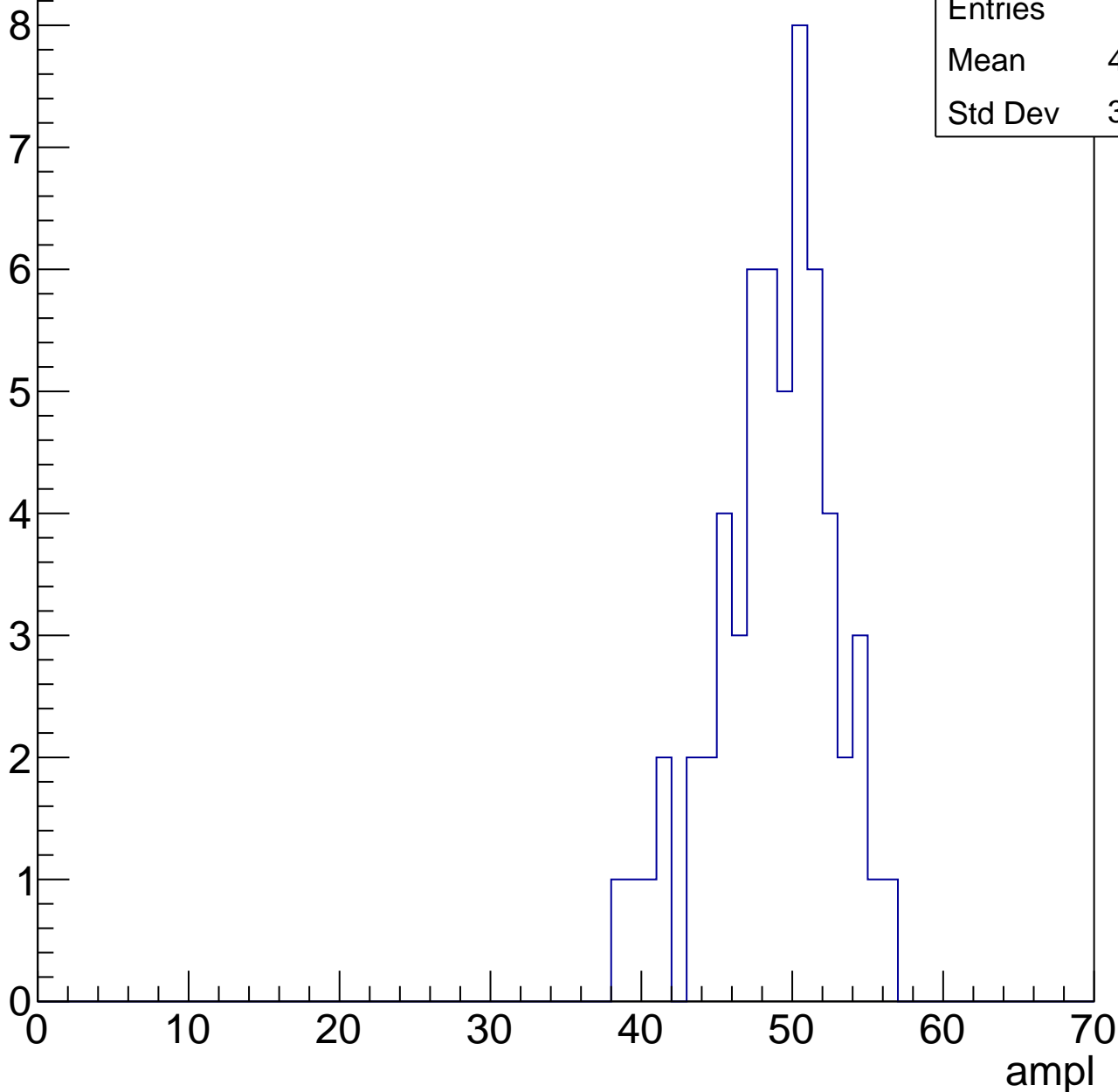


B1L103S, U11-ch10, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

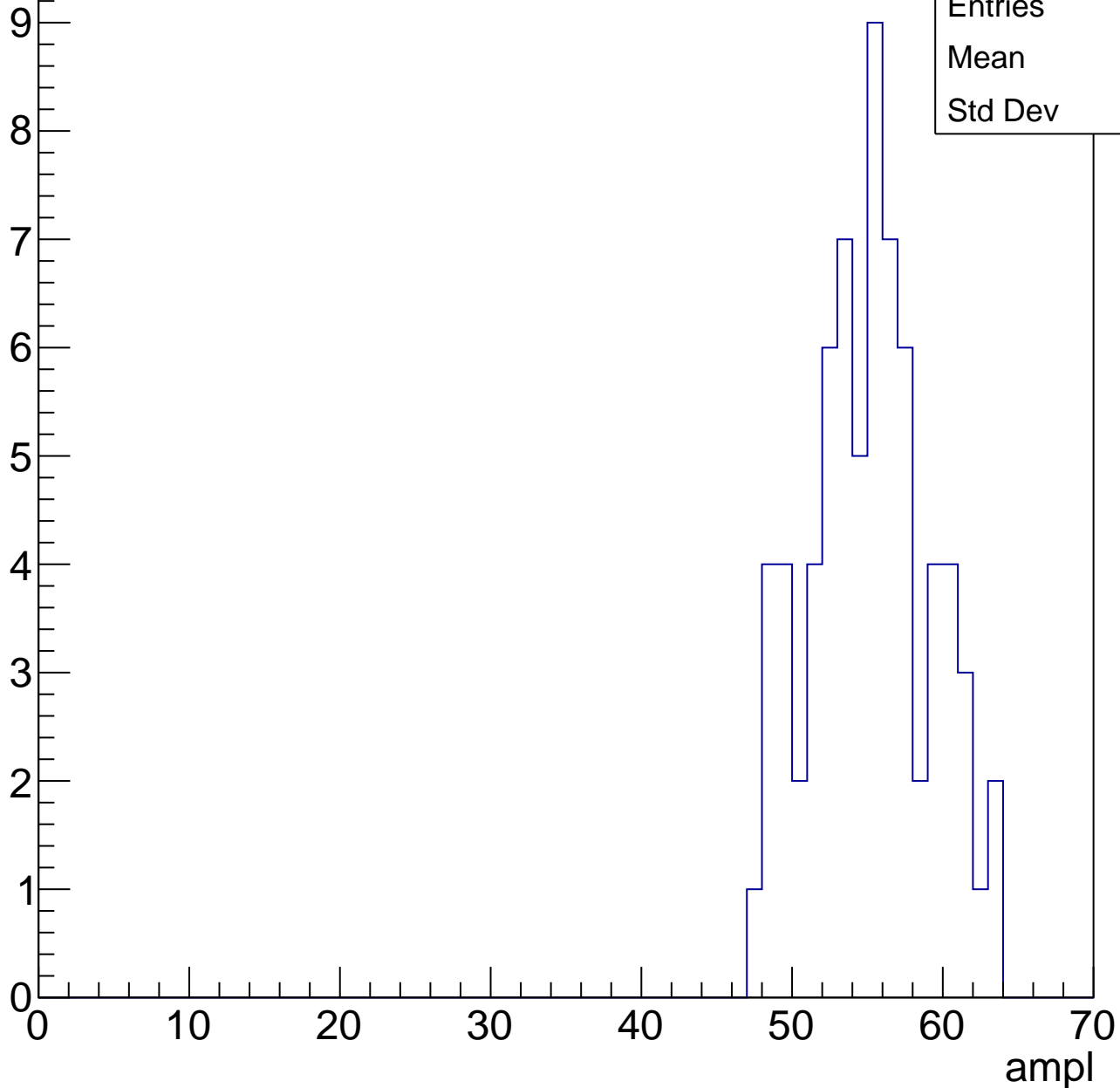
Entries	58
Mean	48.26
Std Dev	3.942



B1L103S, U11-ch10, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



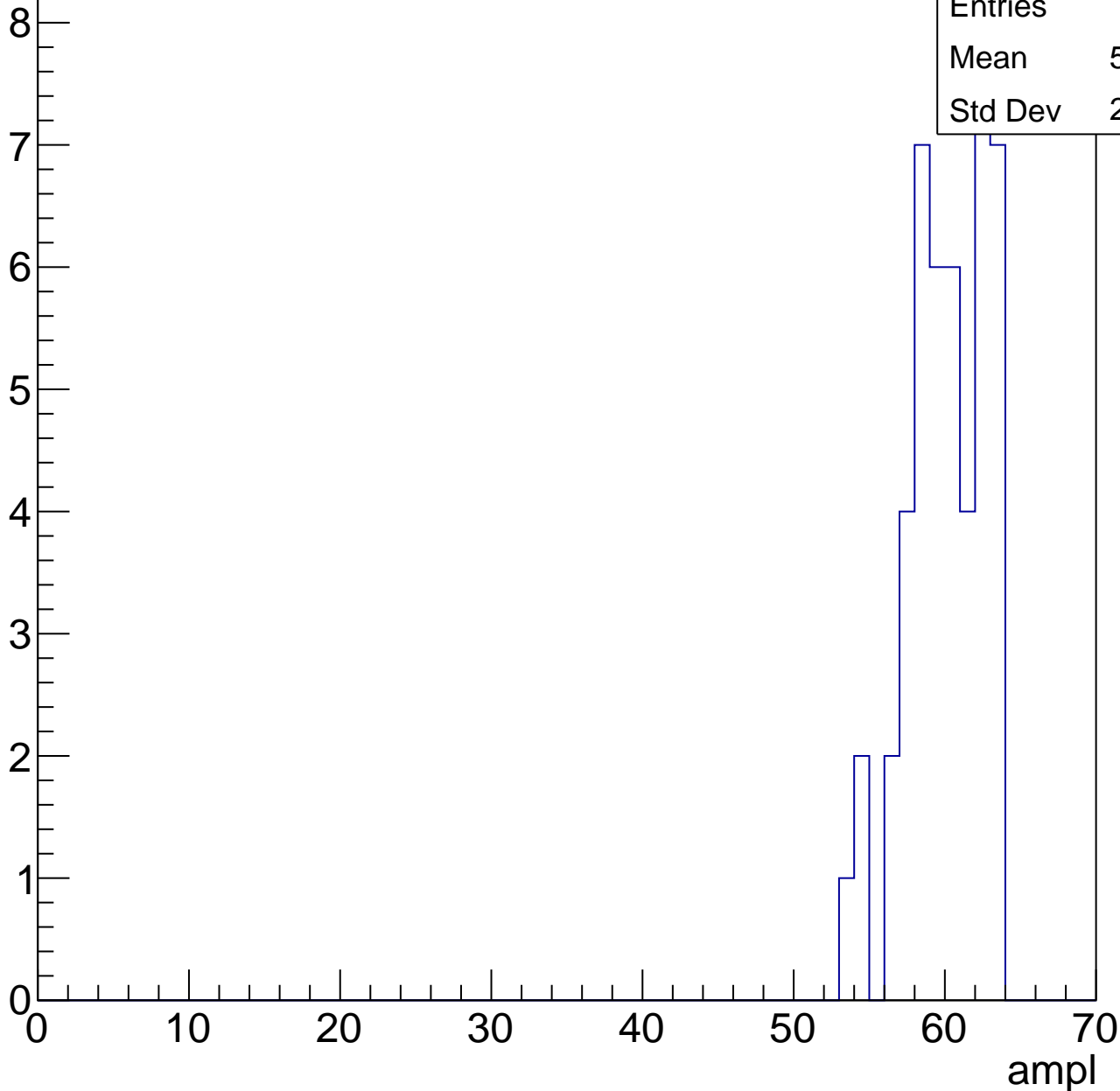
Entries	71
Mean	54.7
Std Dev	3.93

B1L103S, U11-ch10, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

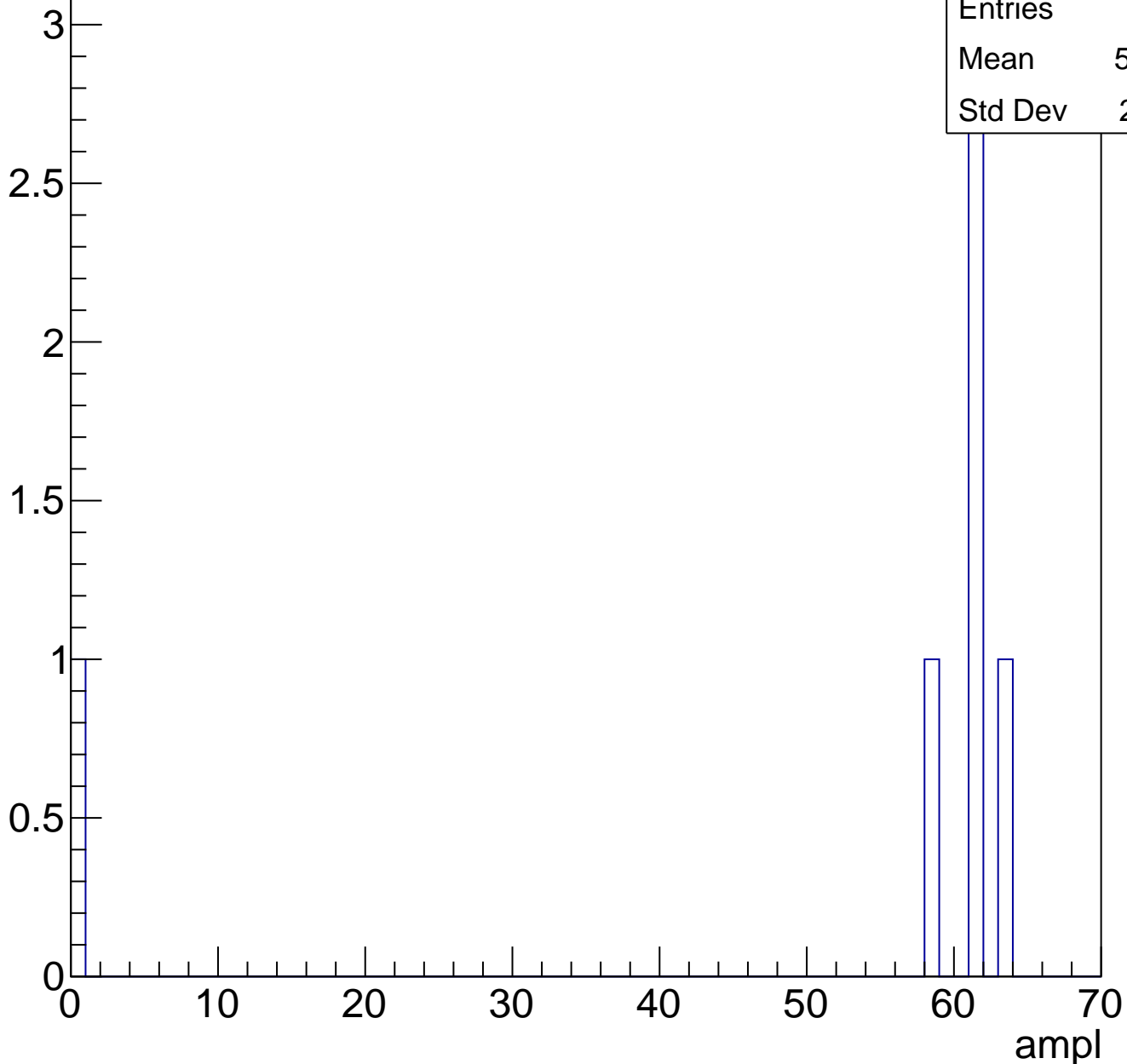
Entries	47
Mean	59.62
Std Dev	2.589



B1L103S, U11-ch10, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

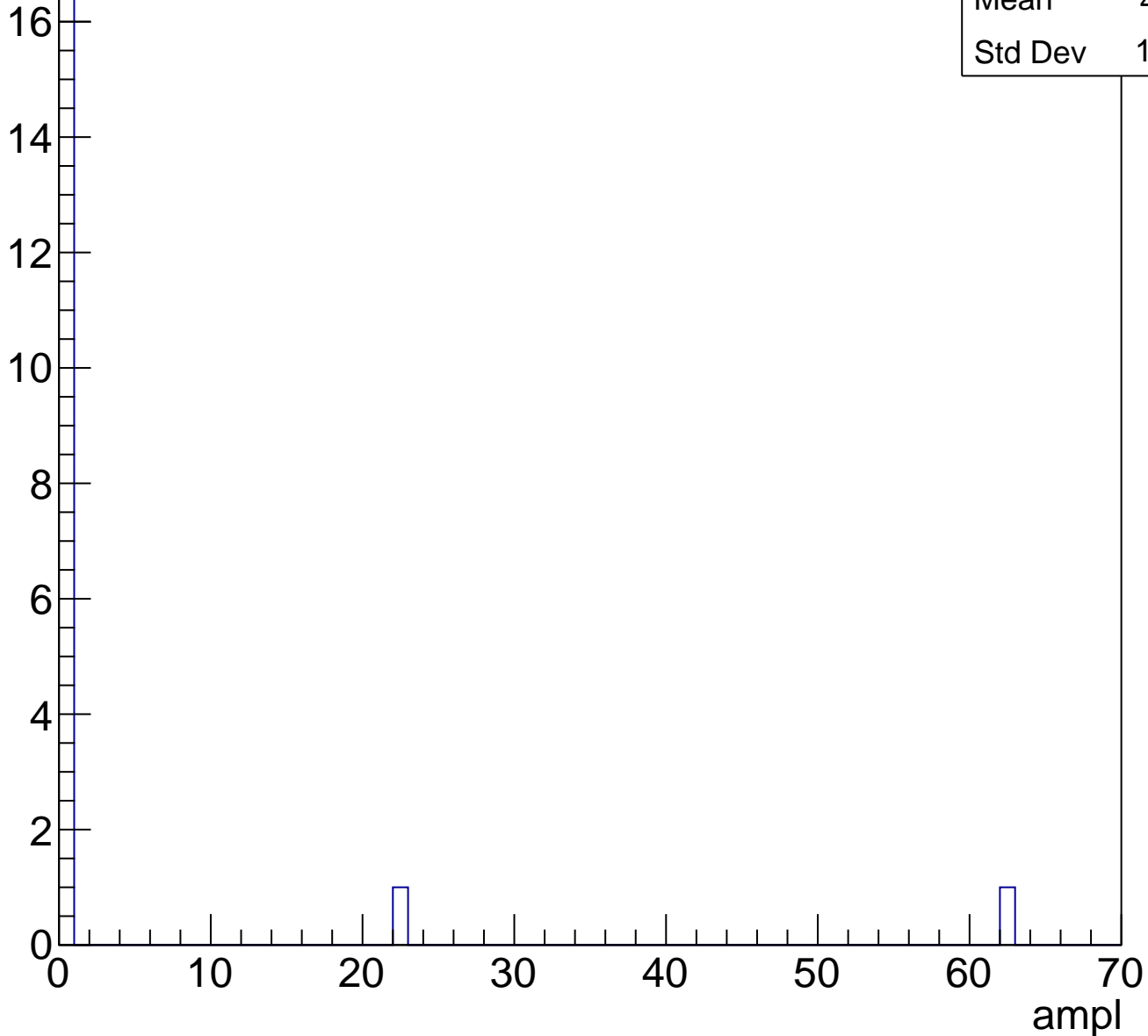


B1L103S, U11-ch10, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	4.421
Std Dev	14.43

Entry

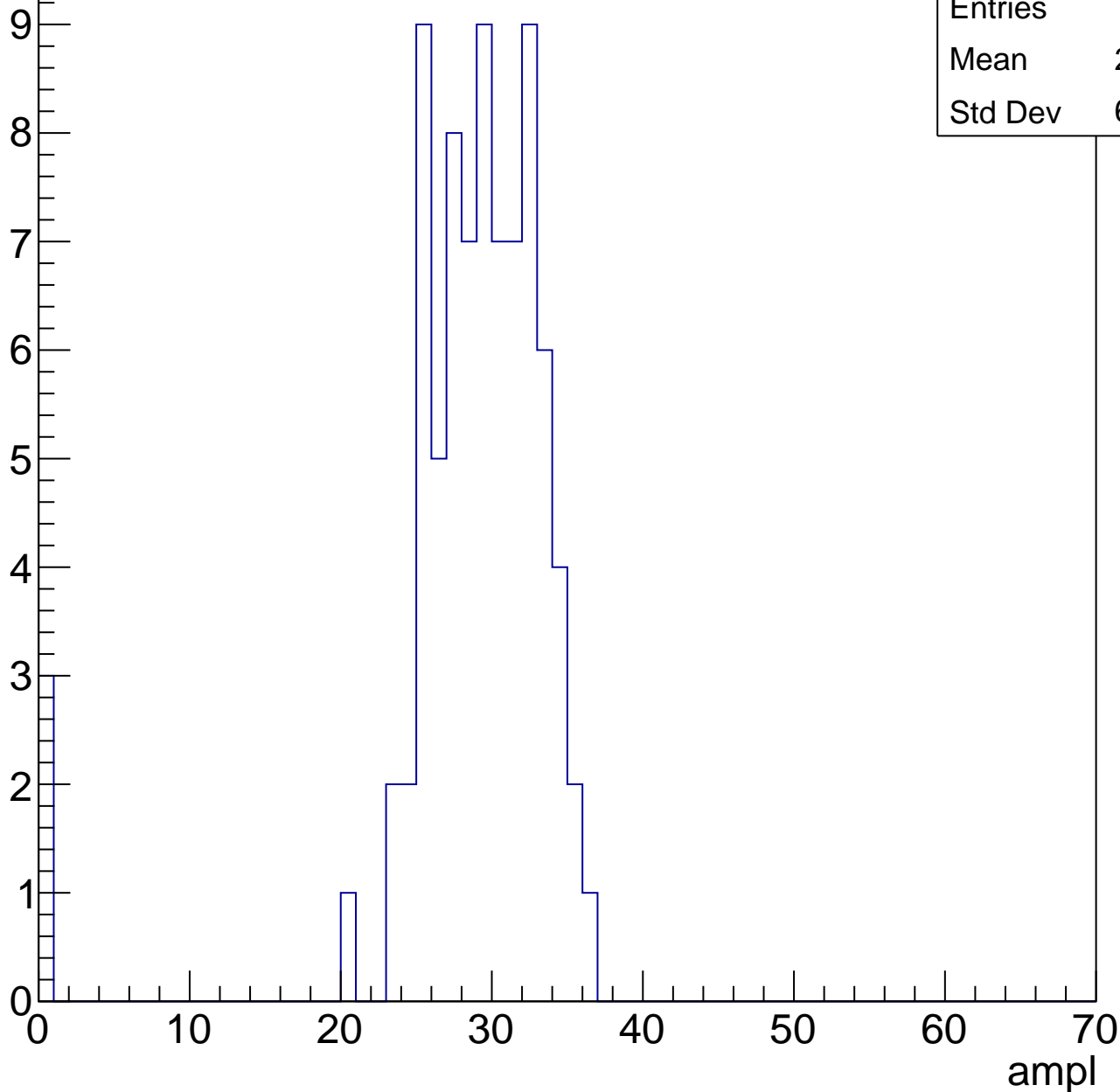


B1L103S, U11-ch11, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	82
Mean	28.01
Std Dev	6.351

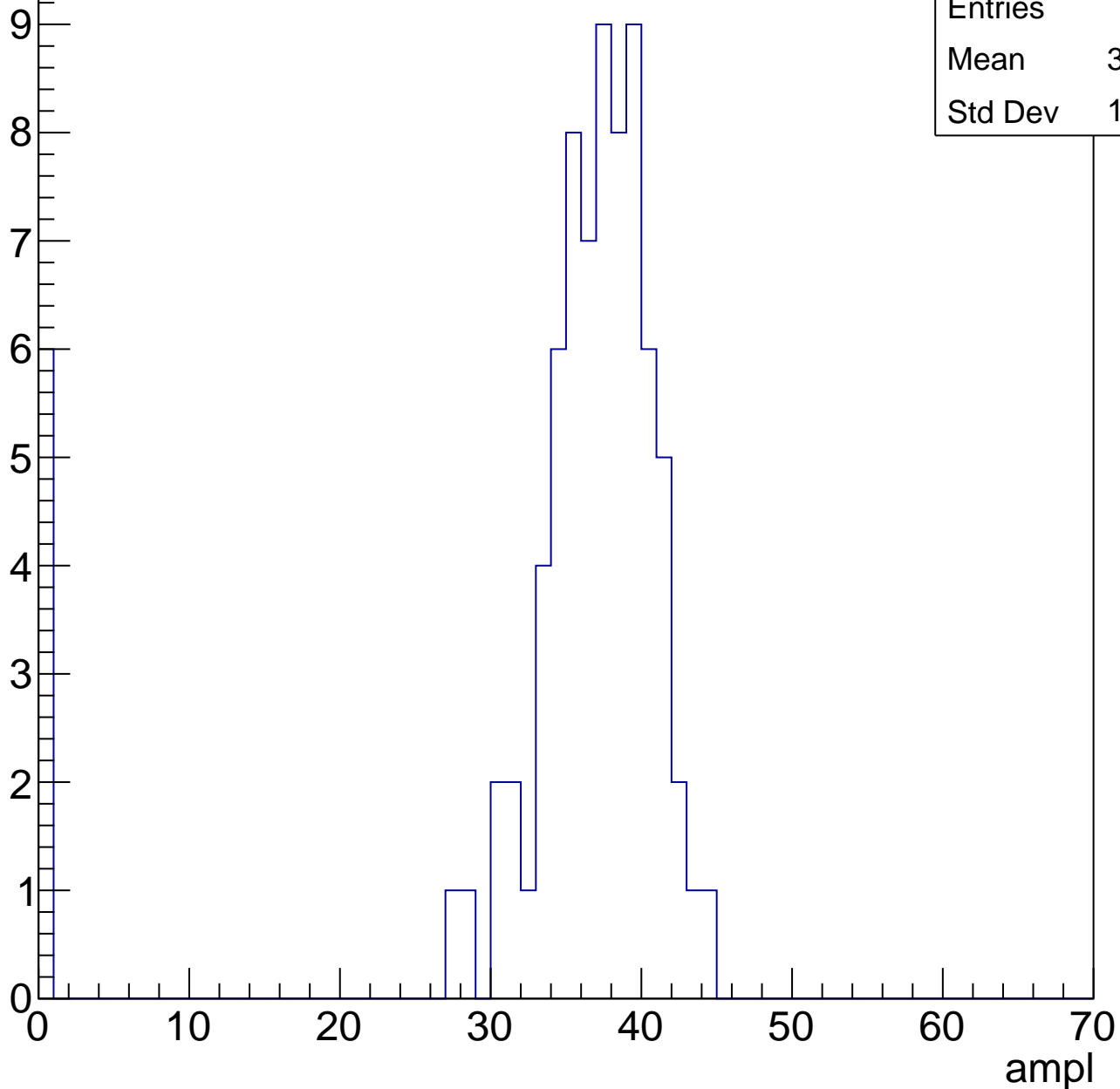


B1L103S, U11-ch11, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	79
Mean	33.94
Std Dev	10.26

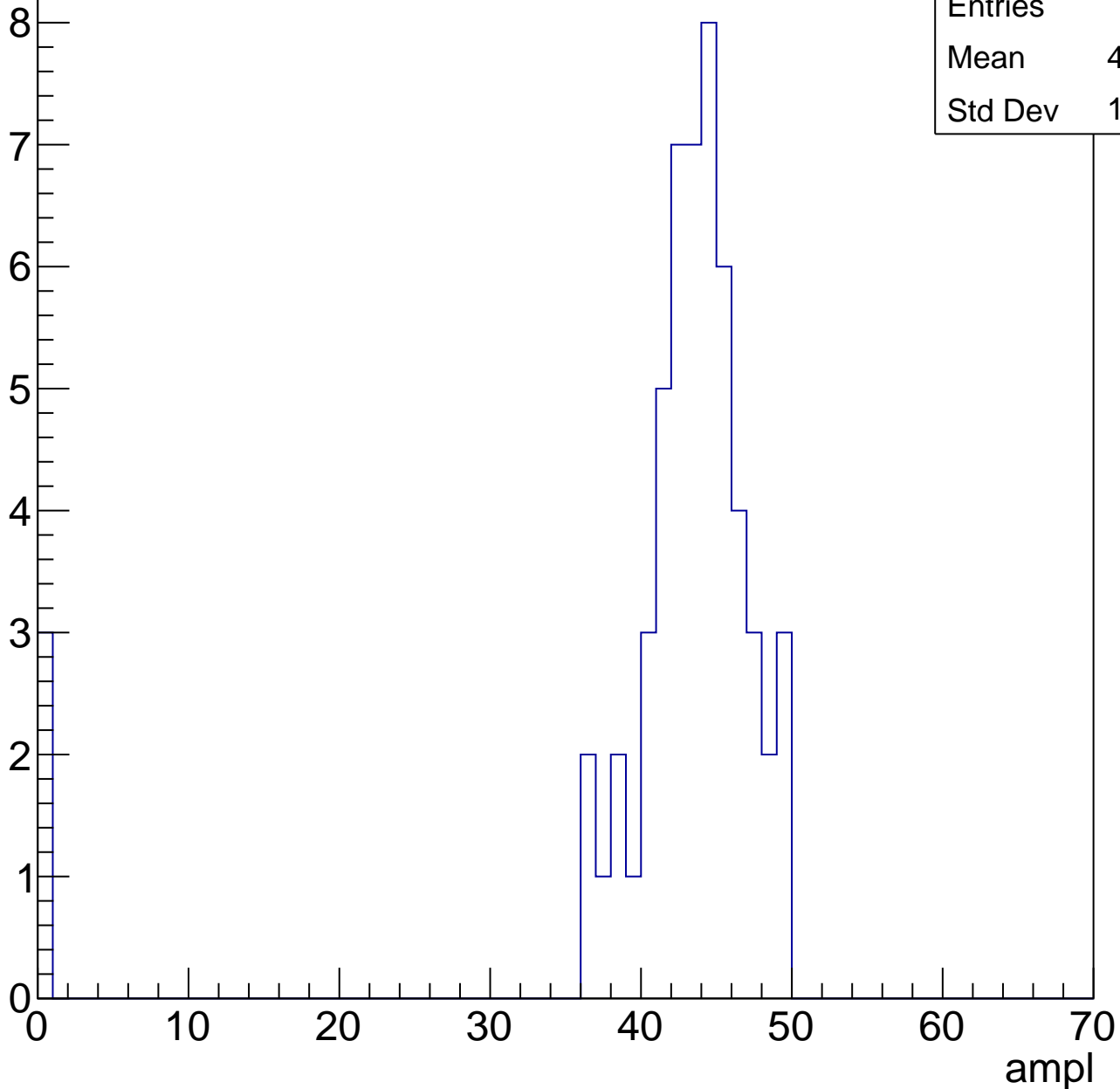


B1L103S, U11-ch11, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	40.95
Std Dev	10.12



B1L103S, U11-ch11, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	66
Mean	49
Std Dev	3.521

Entry

10

8

6

4

2

0

0

10

20

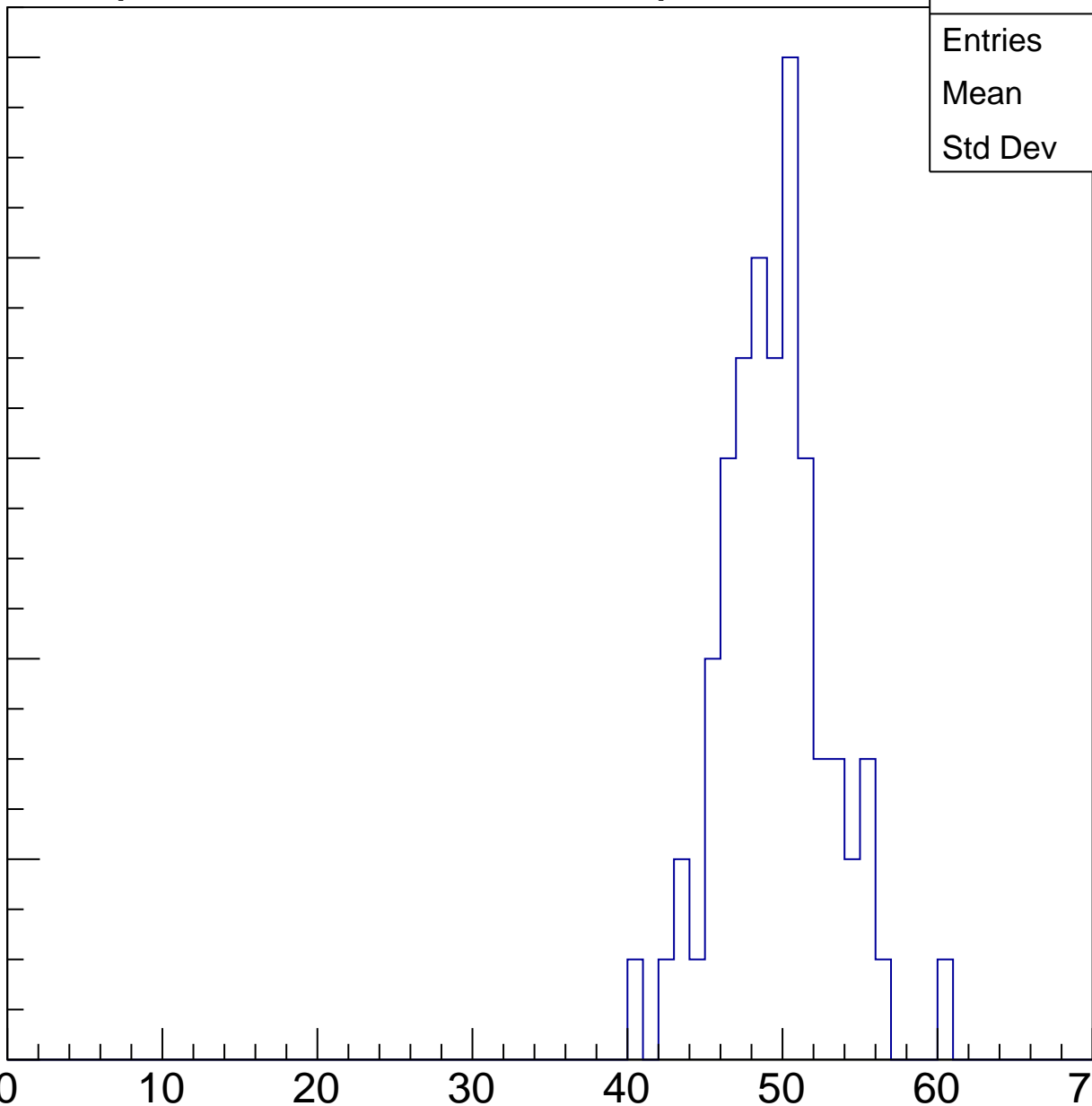
30

40

50

60

ampl

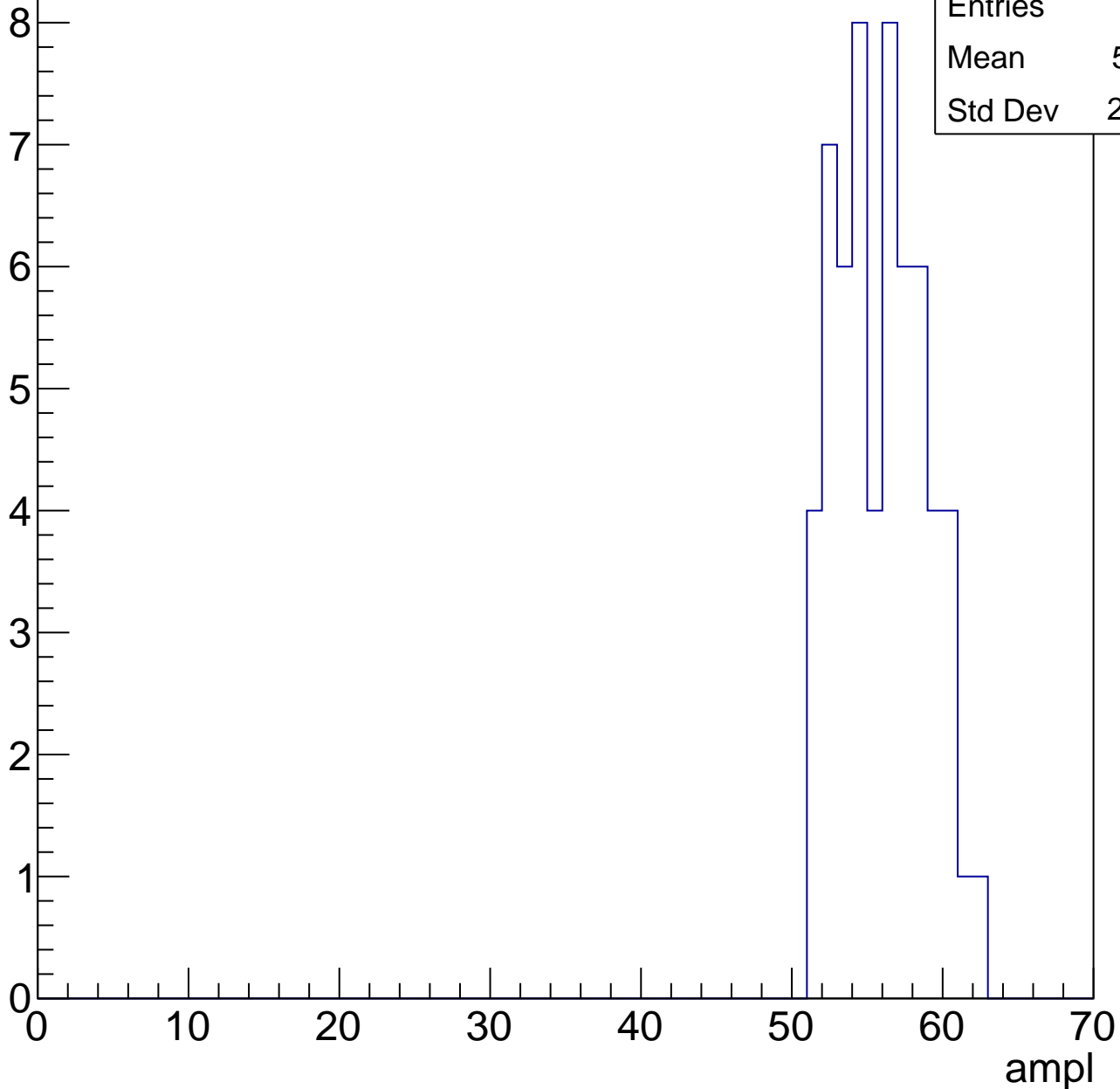


B1L103S, U11-ch11, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	55.51
Std Dev	2.849

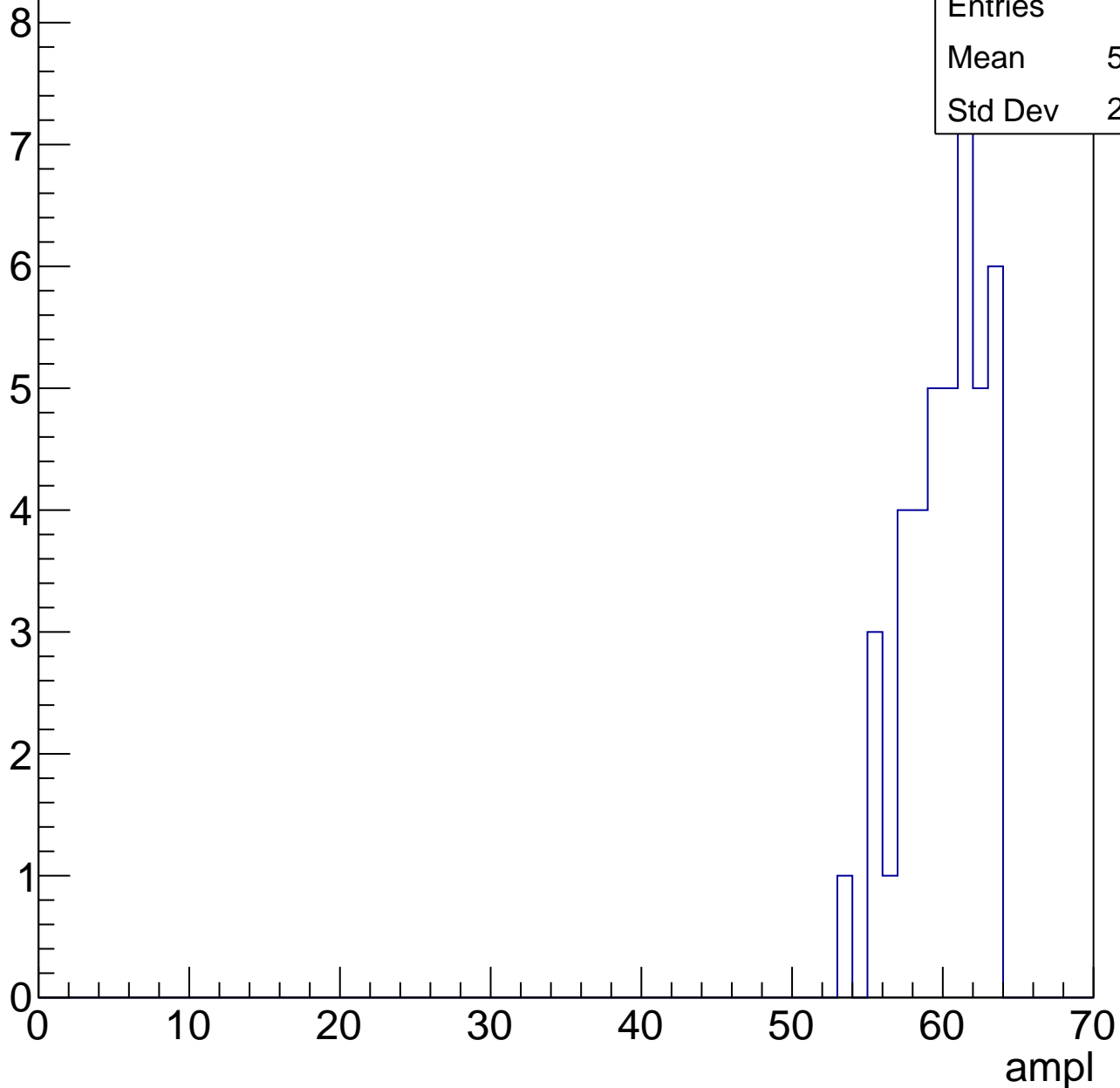


B1L103S, U11-ch11, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

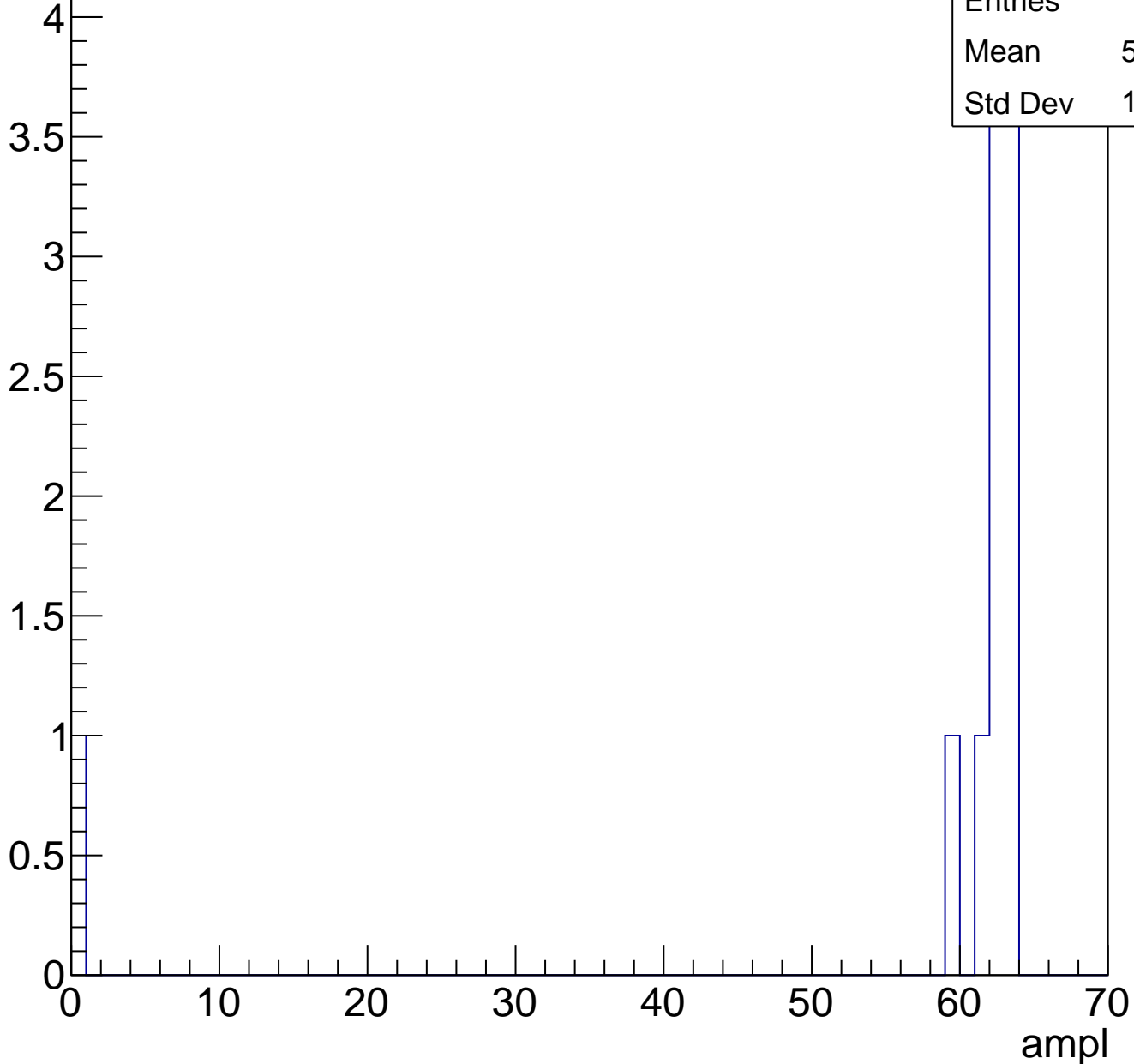
Entries	42
Mean	59.64
Std Dev	2.553



B1L103S, U11-ch11, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

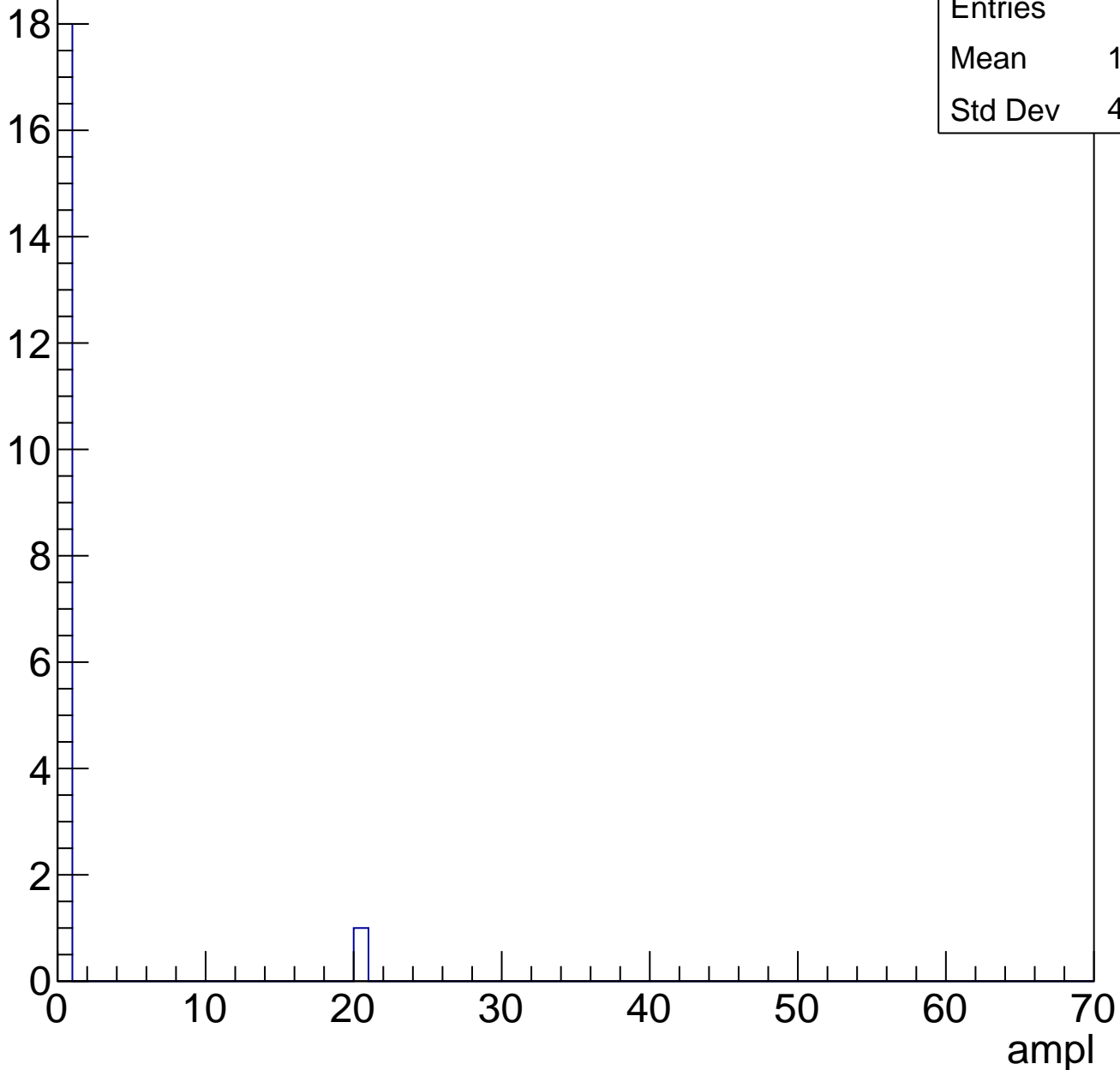


B1L103S, U11-ch11, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.053
Std Dev	4.466

Entry

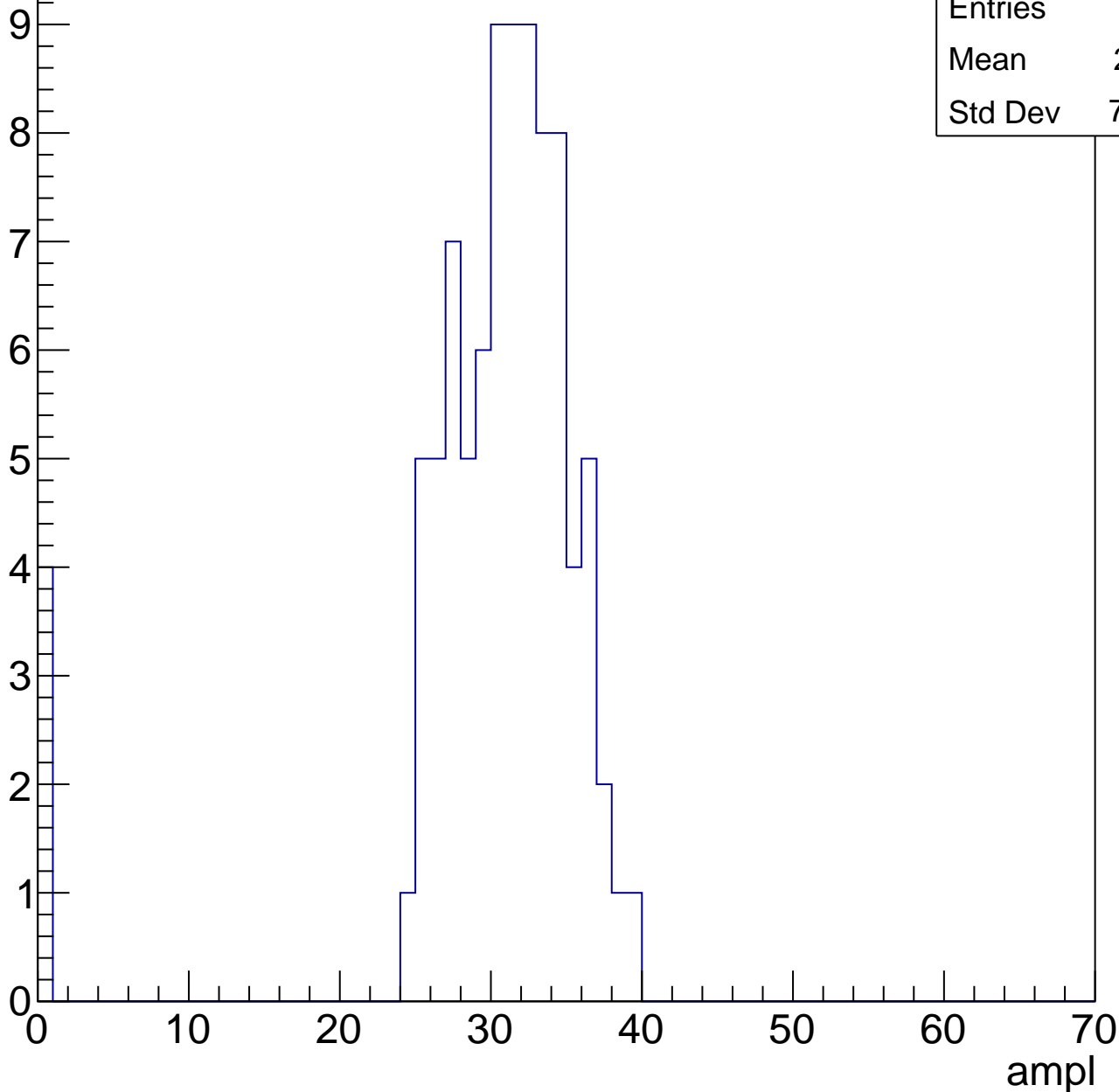


B1L103S, U11-ch12, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	89
Mean	29.51
Std Dev	7.249

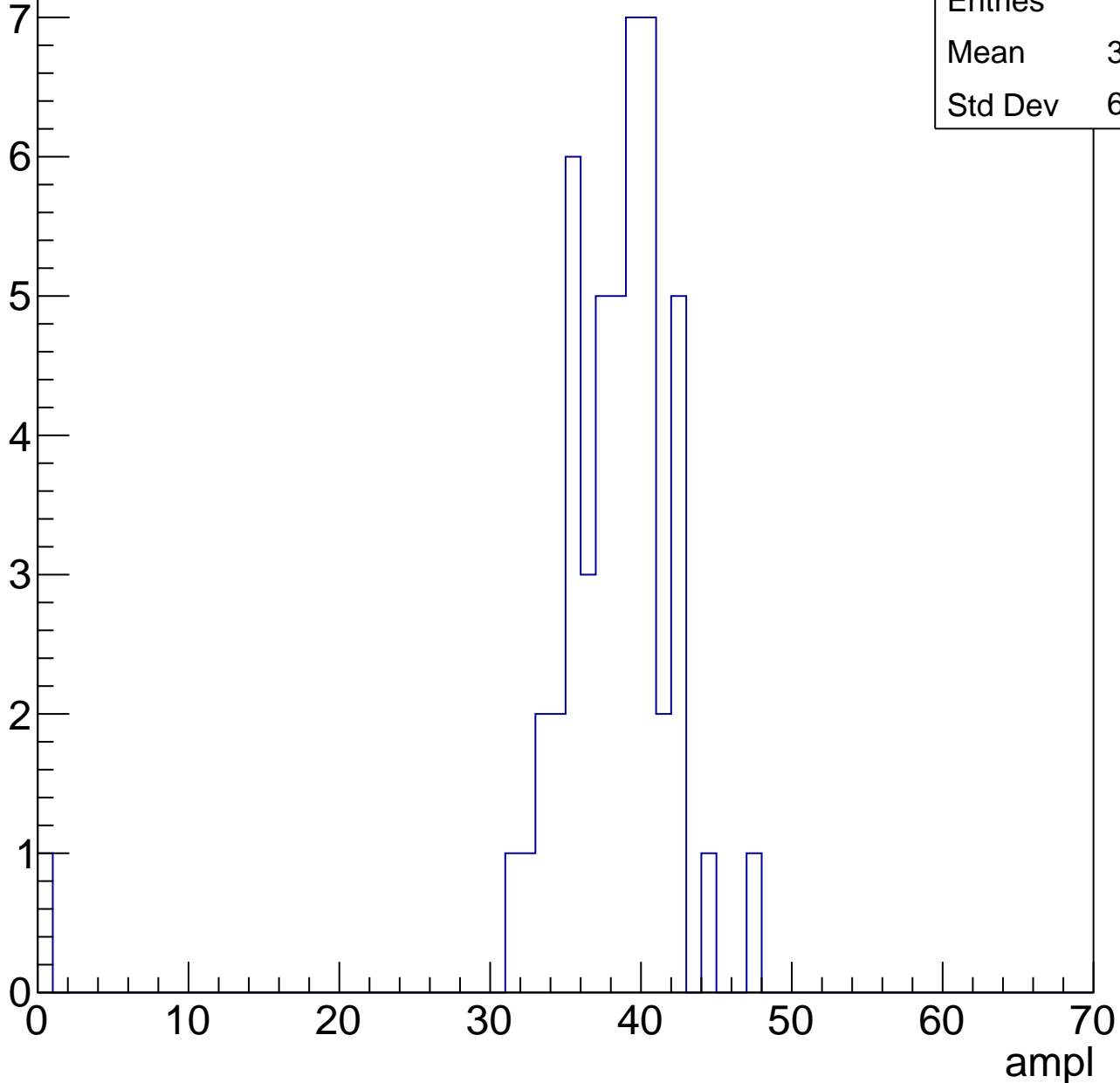


B1L103S, U11-ch12, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

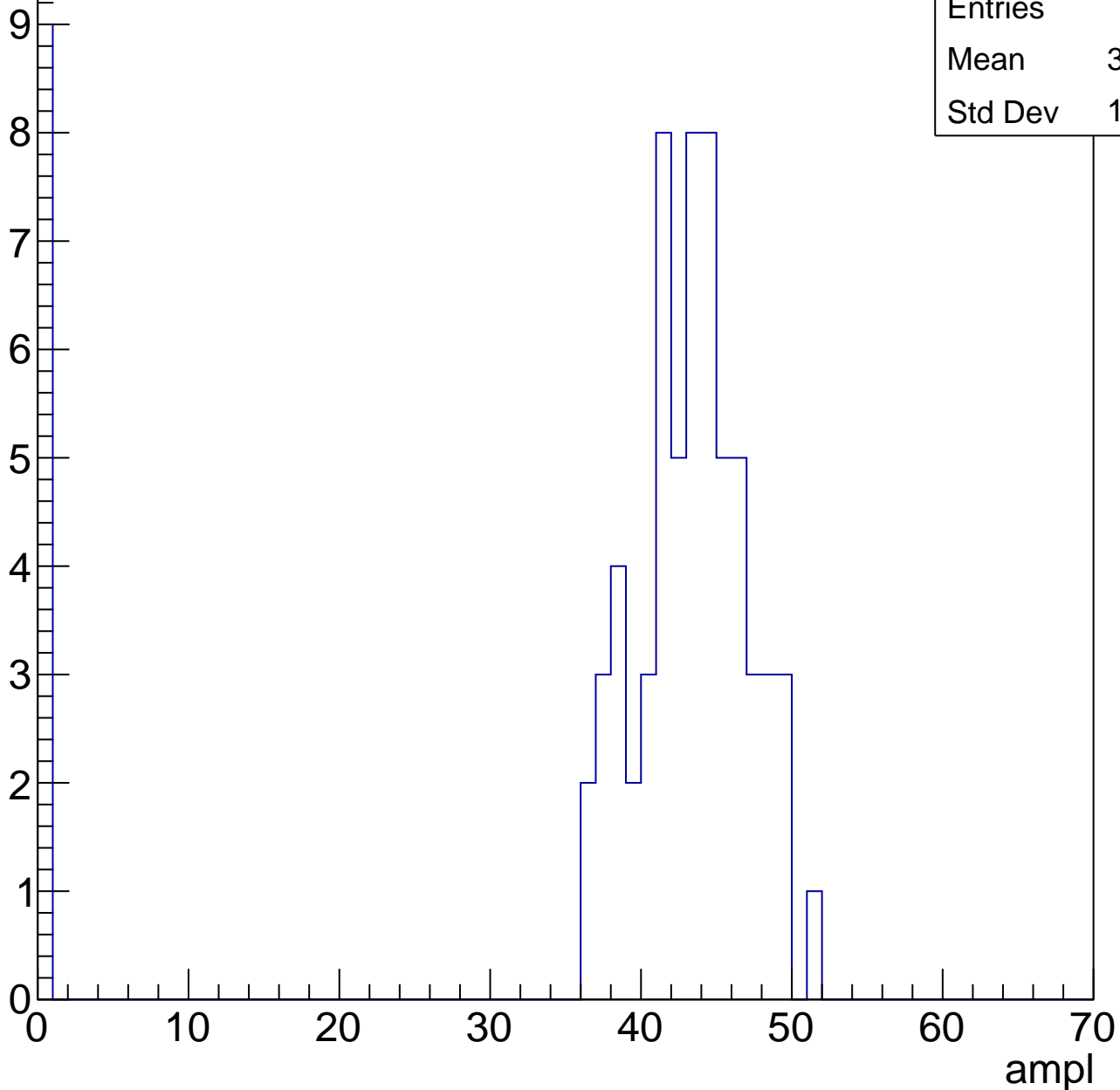
Entries	49
Mean	37.27
Std Dev	6.236



B1L103S, U11-ch12, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

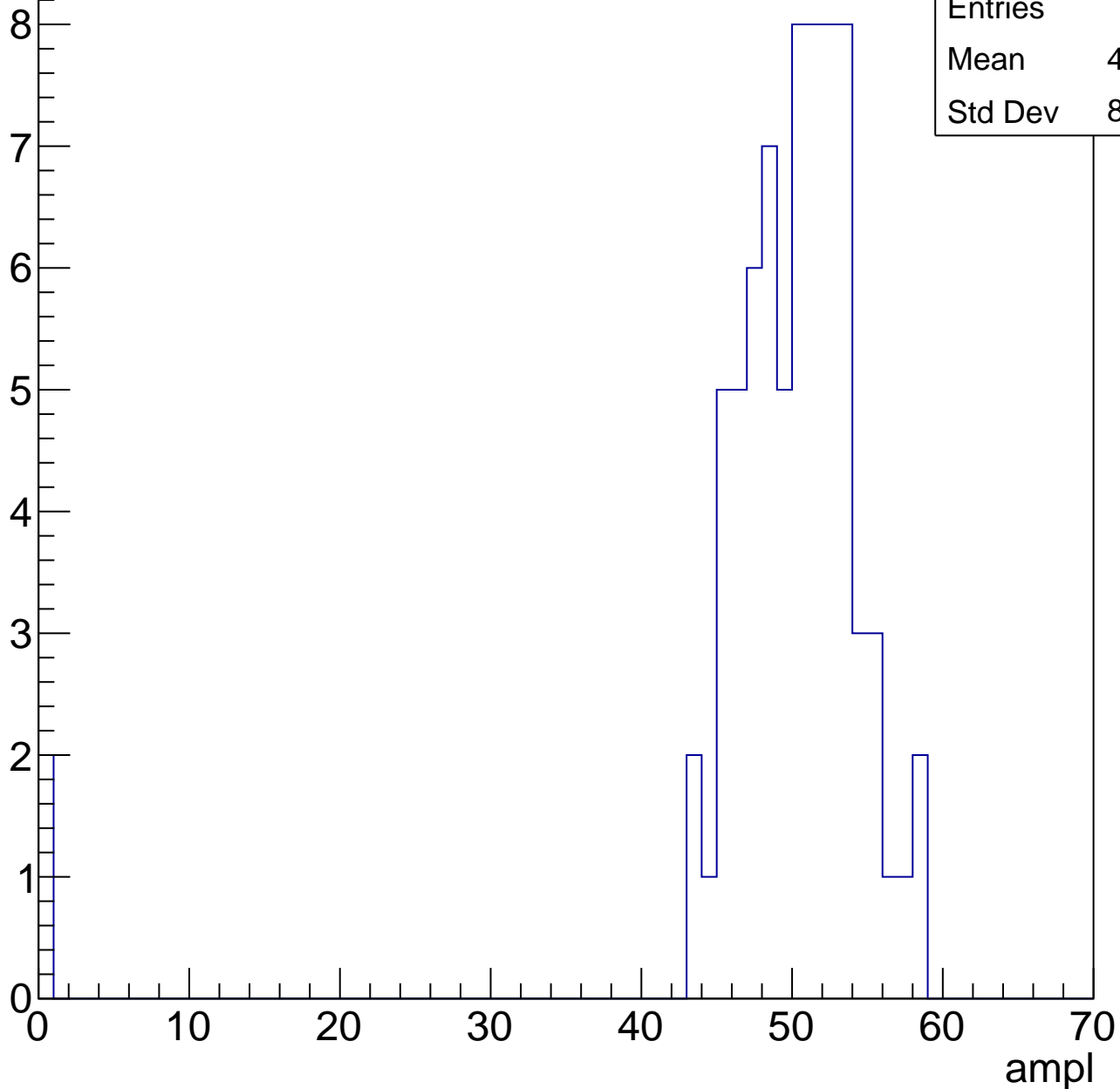


B1L103S, U11-ch12, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

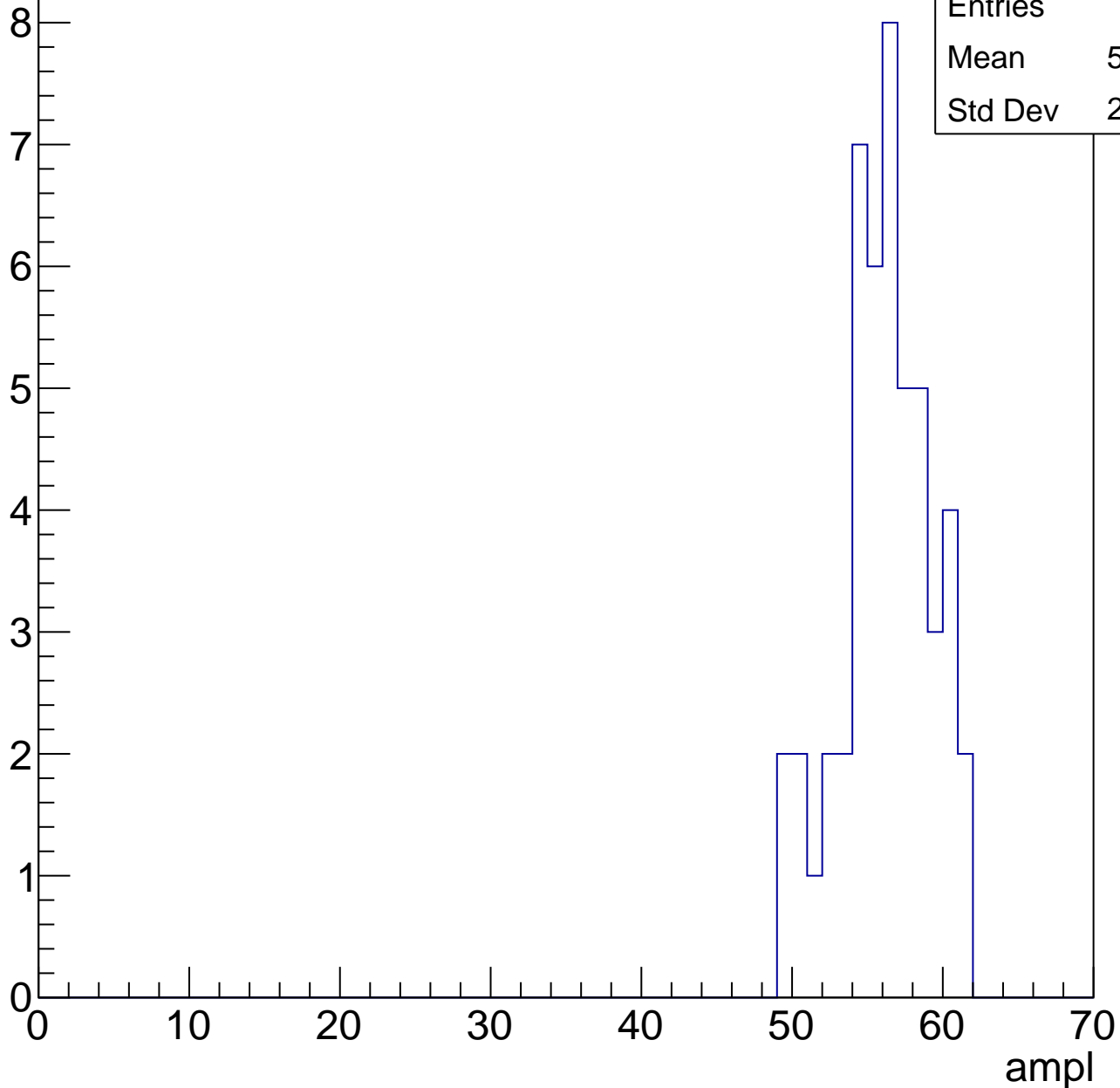
Entries	75
Mean	48.69
Std Dev	8.753



B1L103S, U11-ch12, adc4

calib_packv5_041523_1651.root, FC#0, port C2

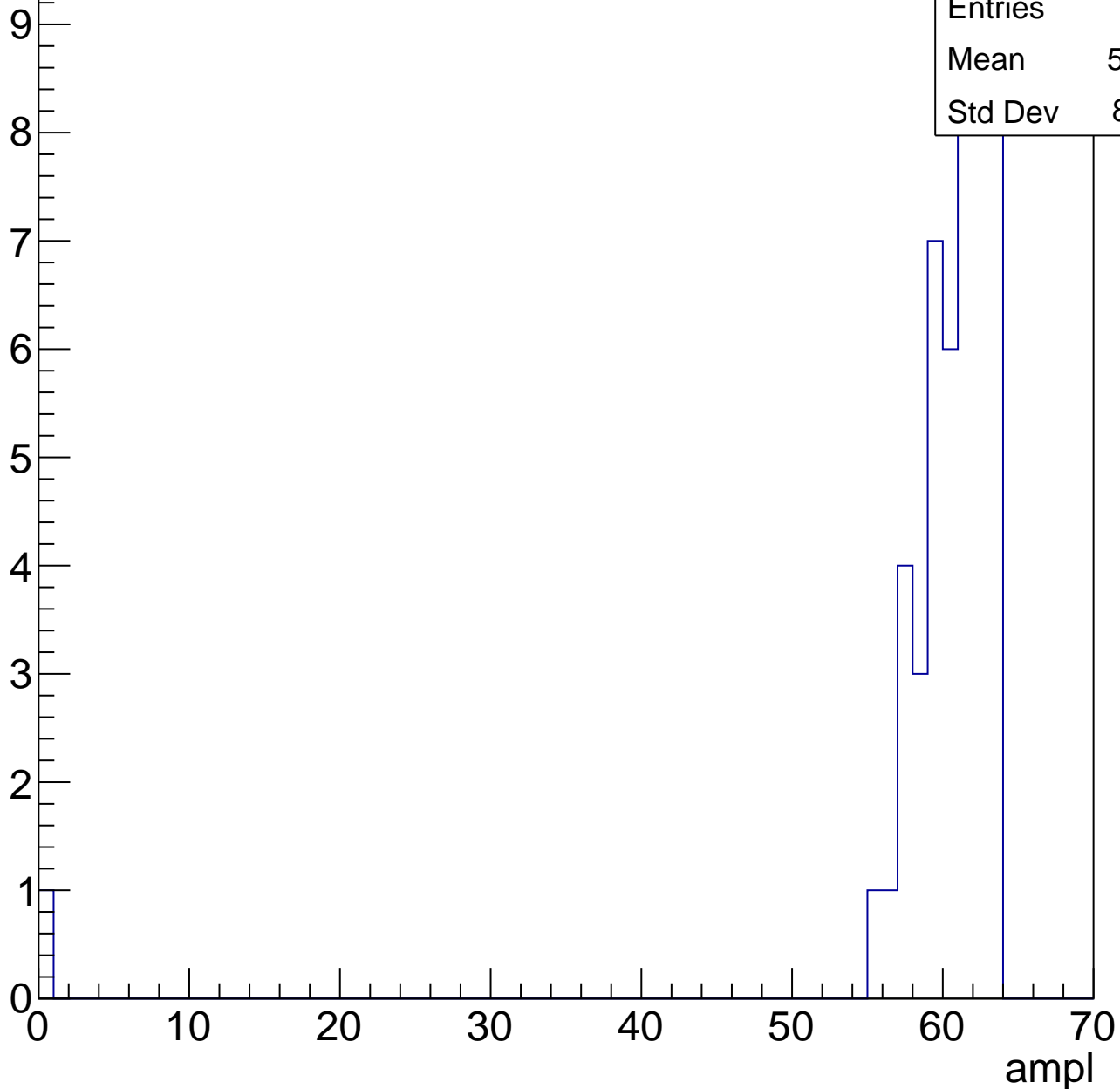
Entry



B1L103S, U11-ch12, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch12, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch12, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	18
Mean	0
Std Dev	0

B1L103S, U11-ch13, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	24.8
Std Dev	11.33

Entry

12

10

8

6

4

2

0

0

10

20

30

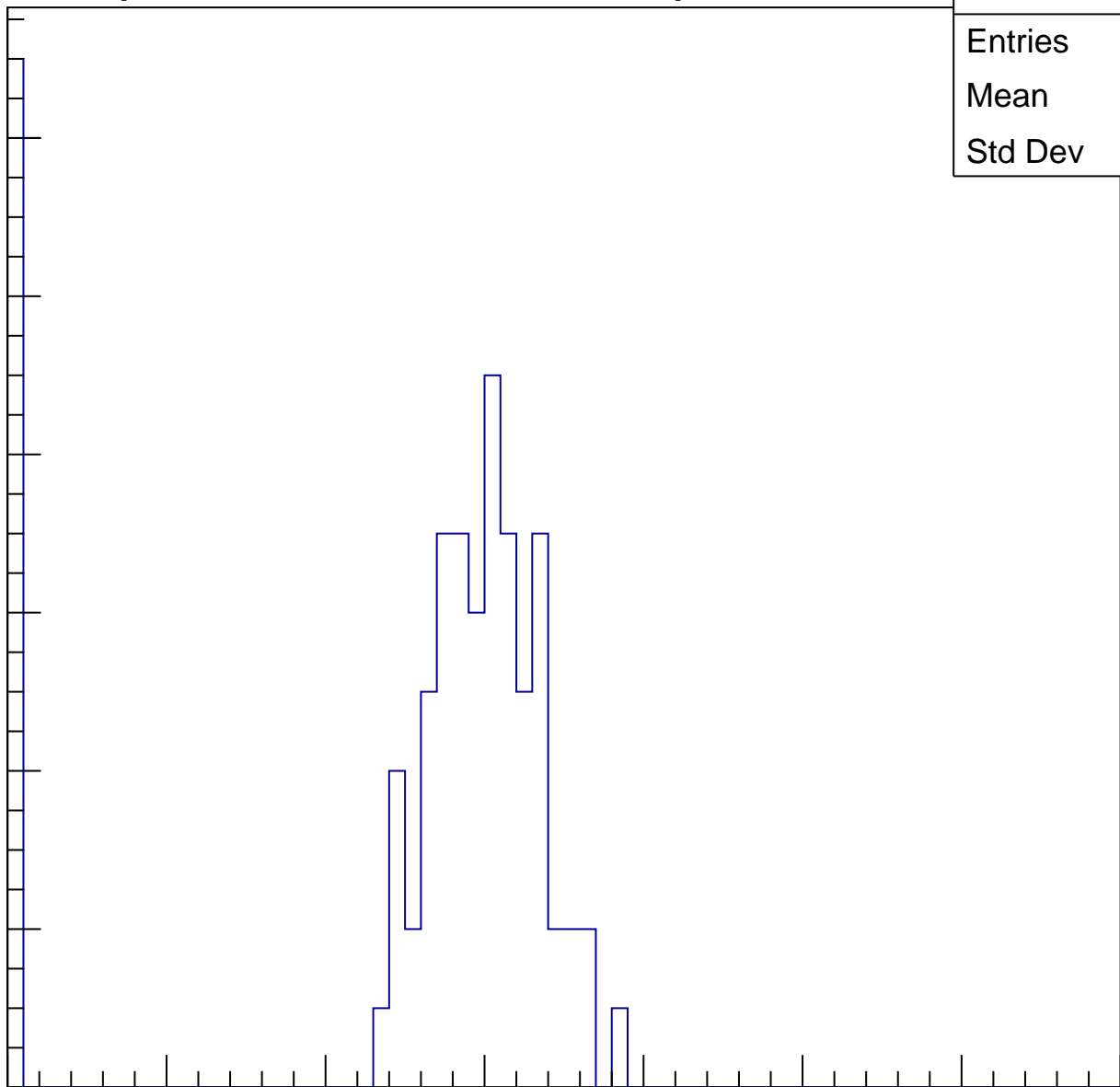
40

50

60

70

ampl

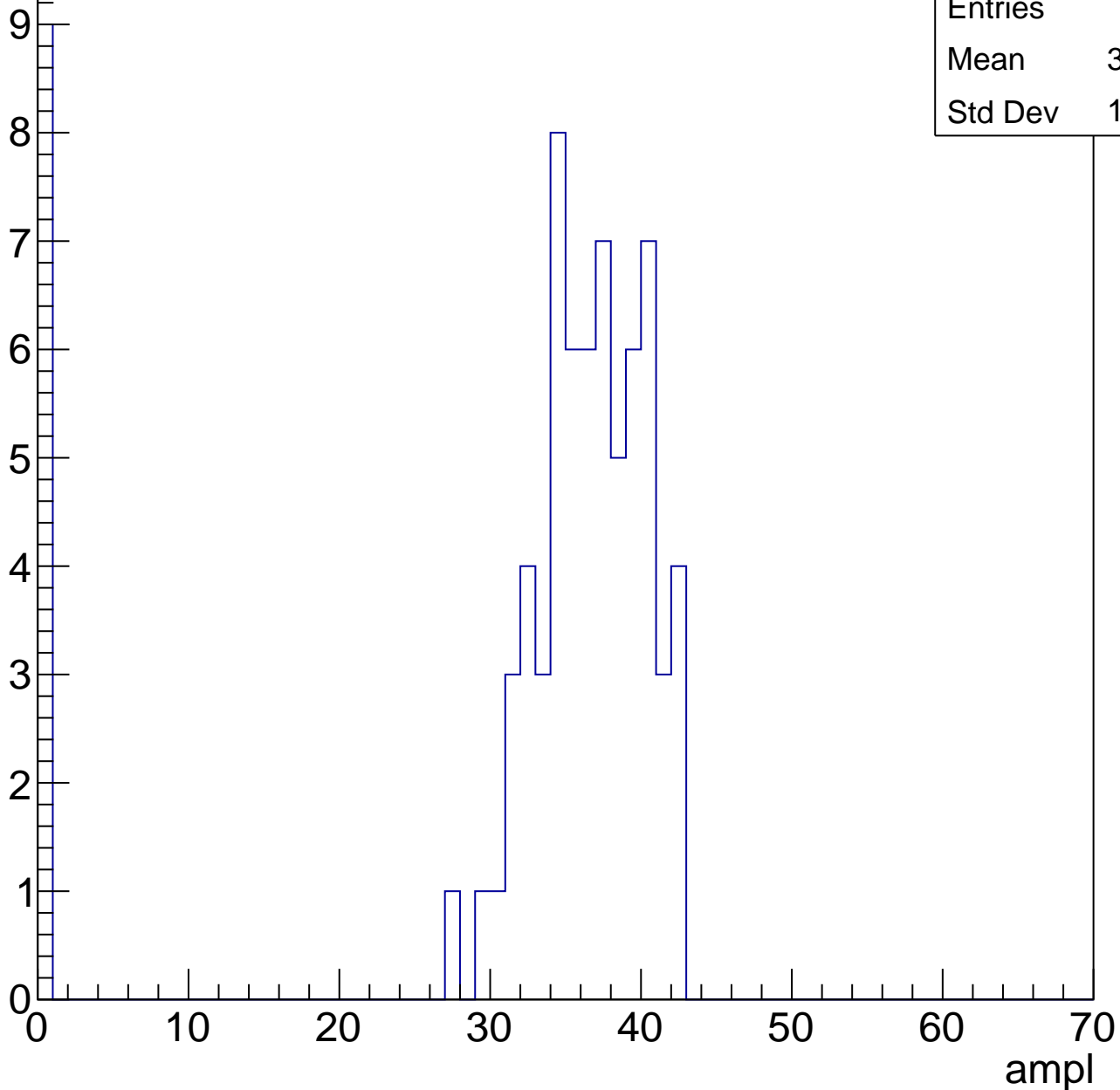


B1L103S, U11-ch13, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	31.86
Std Dev	12.29

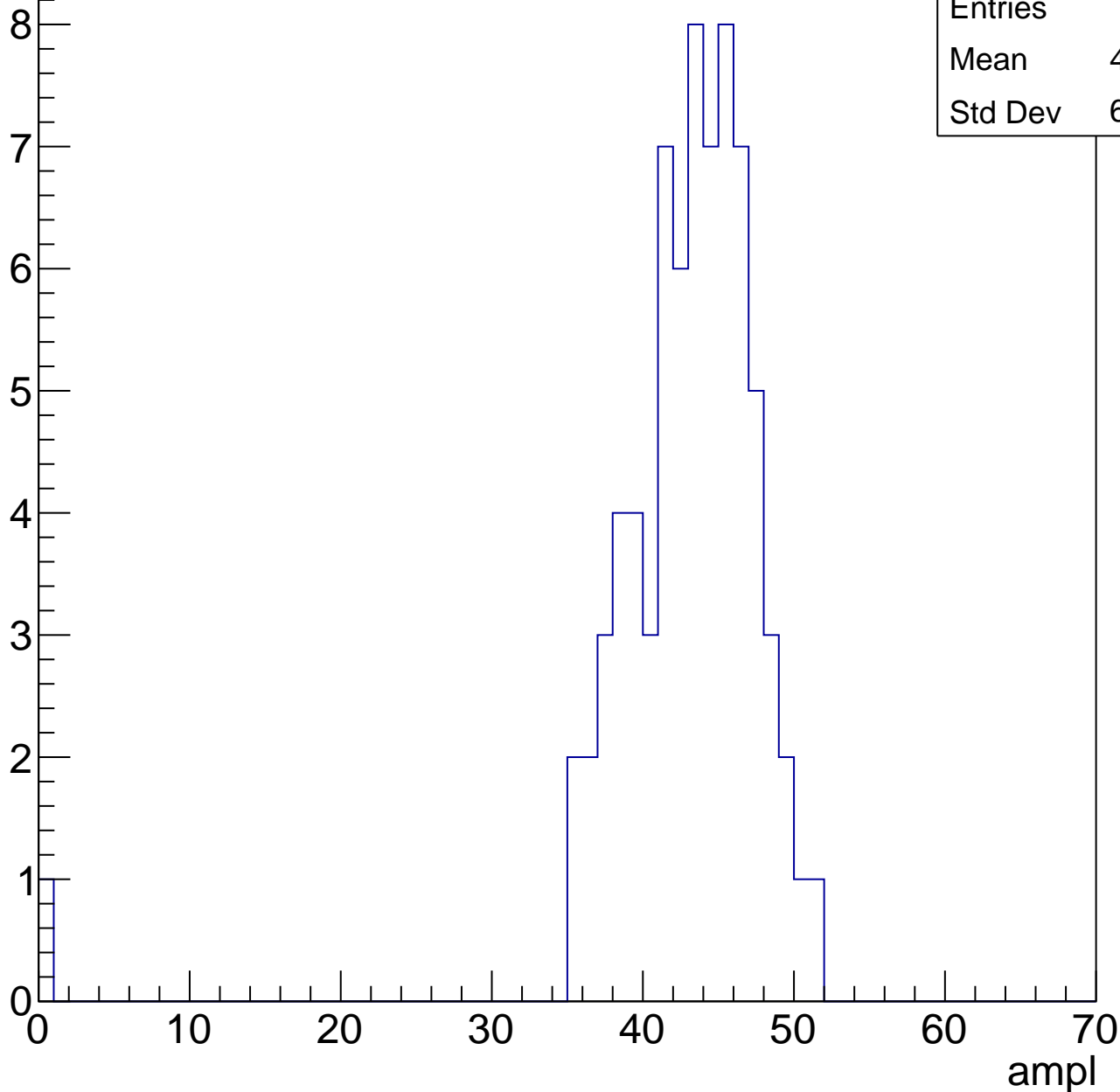


B1L103S, U11-ch13, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	42.32
Std Dev	6.169

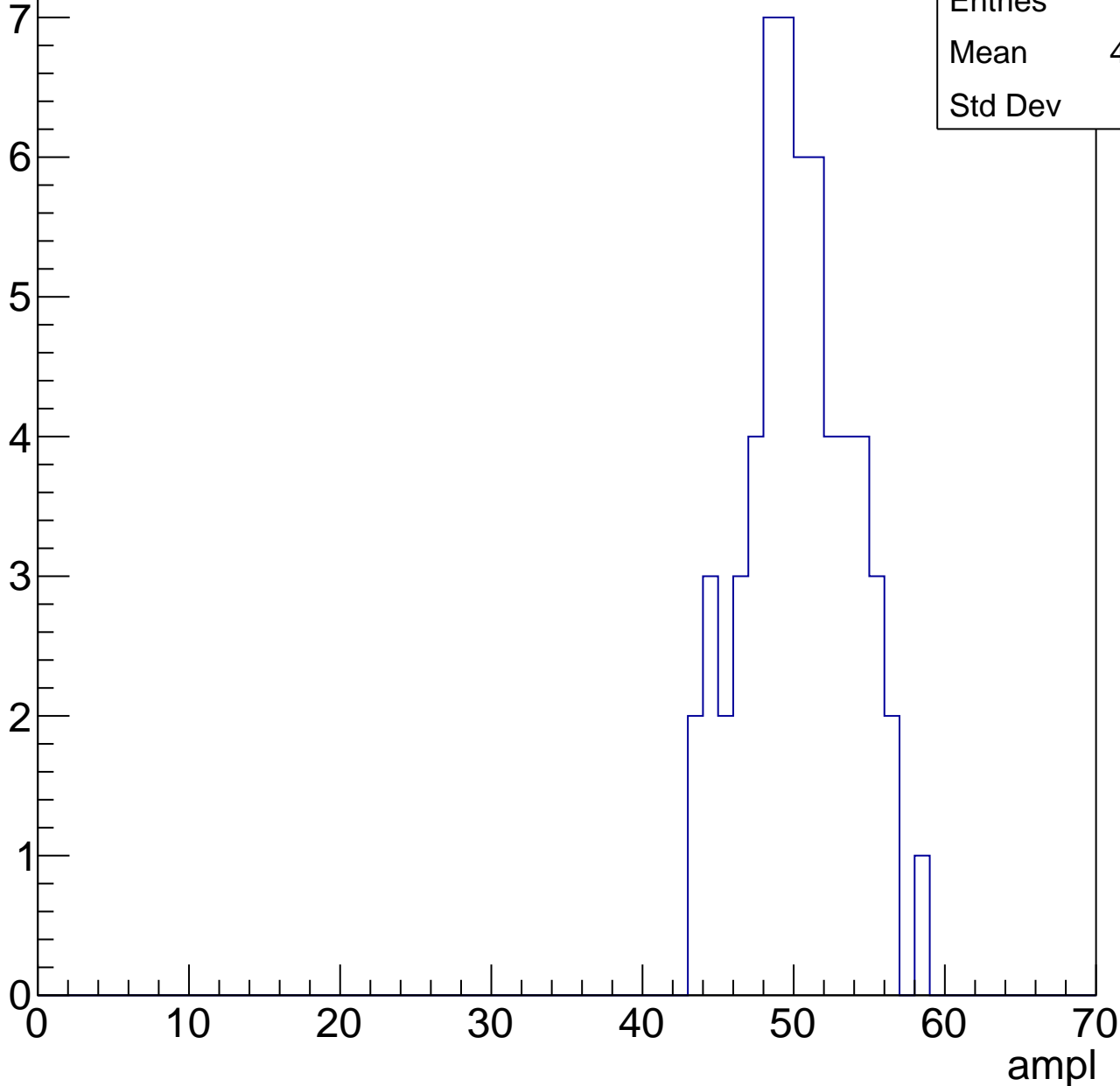


B1L103S, U11-ch13, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	49.83
Std Dev	3.49

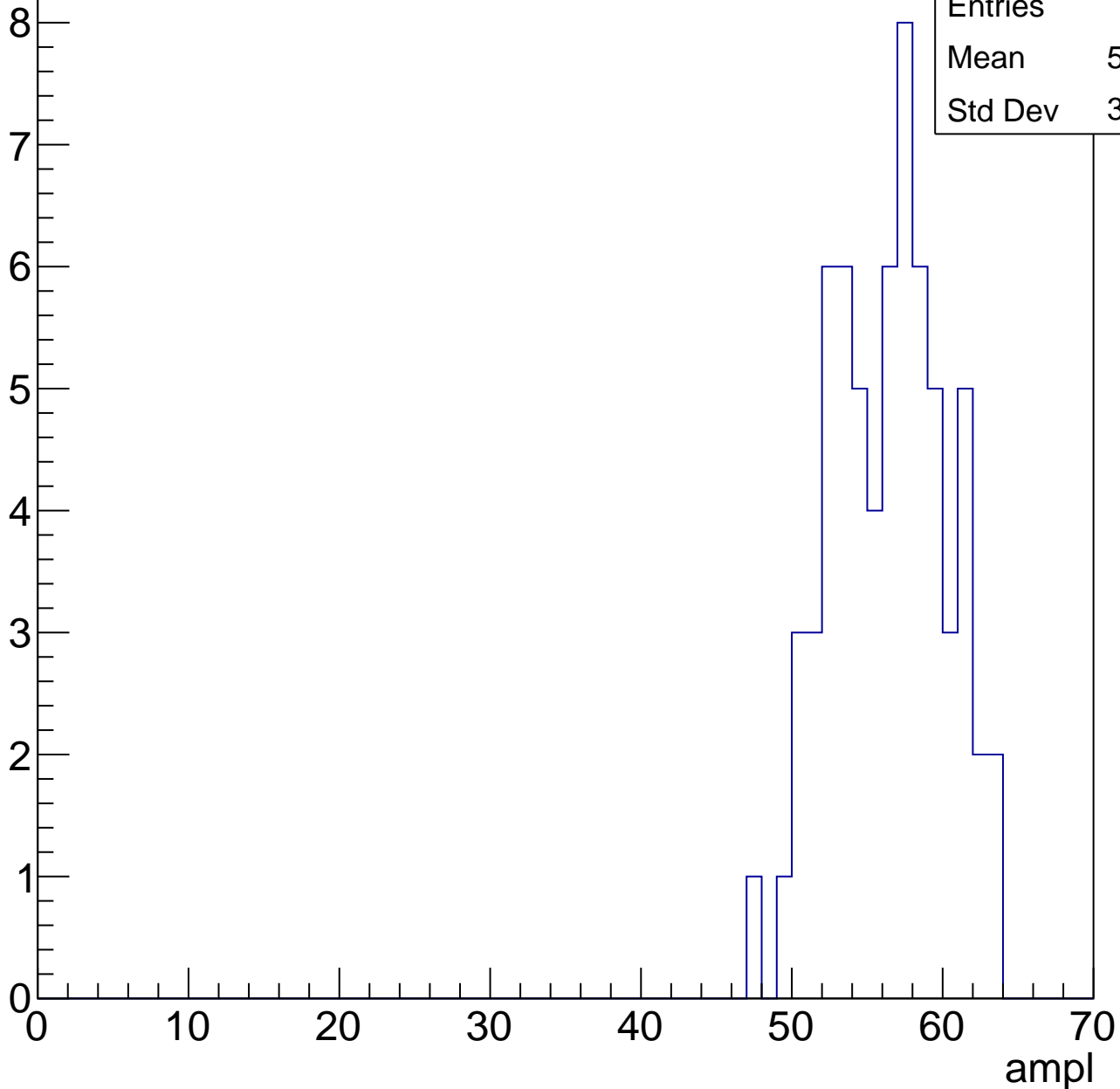


B1L103S, U11-ch13, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	55.89
Std Dev	3.706

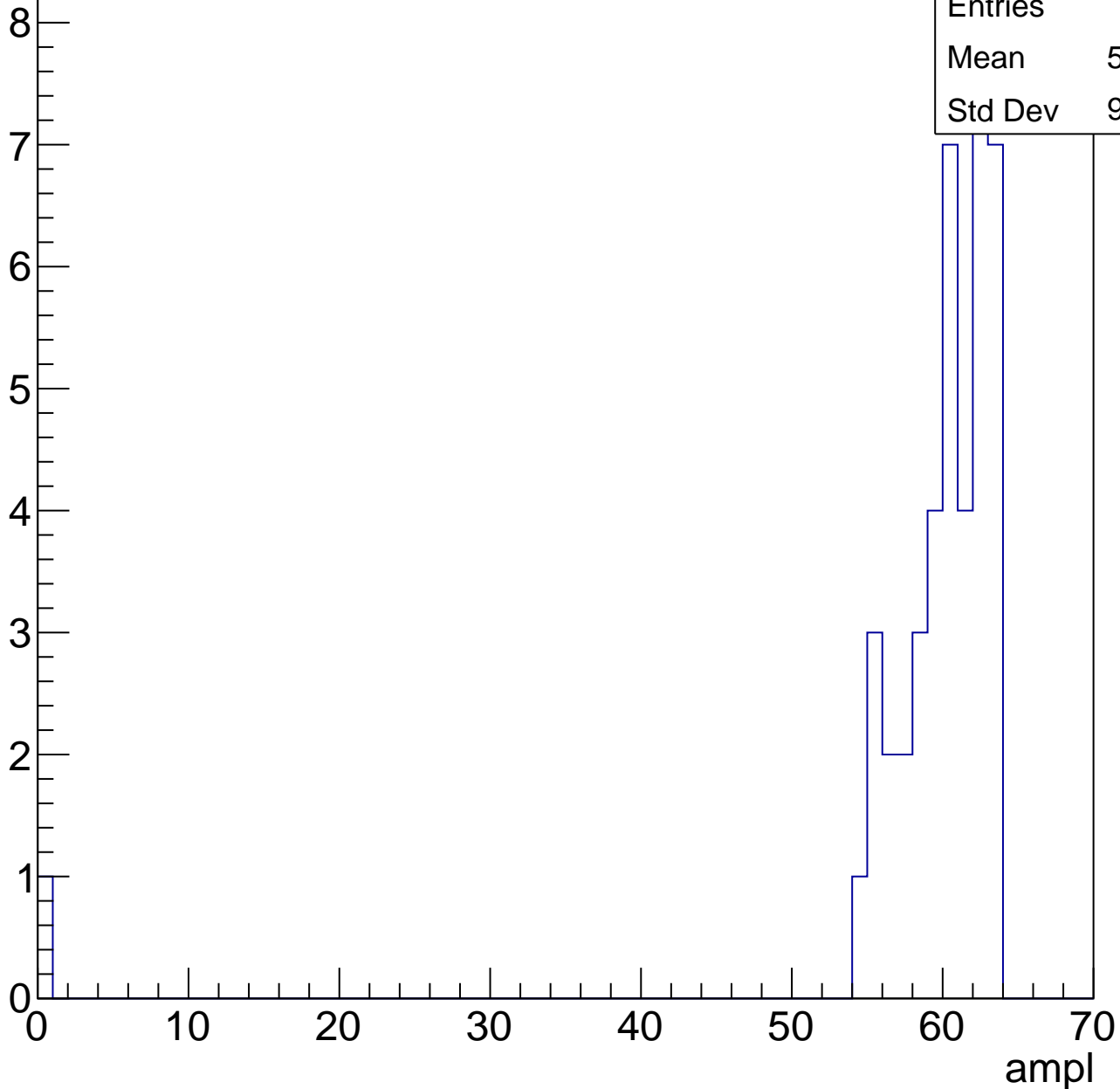


B1L103S, U11-ch13, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

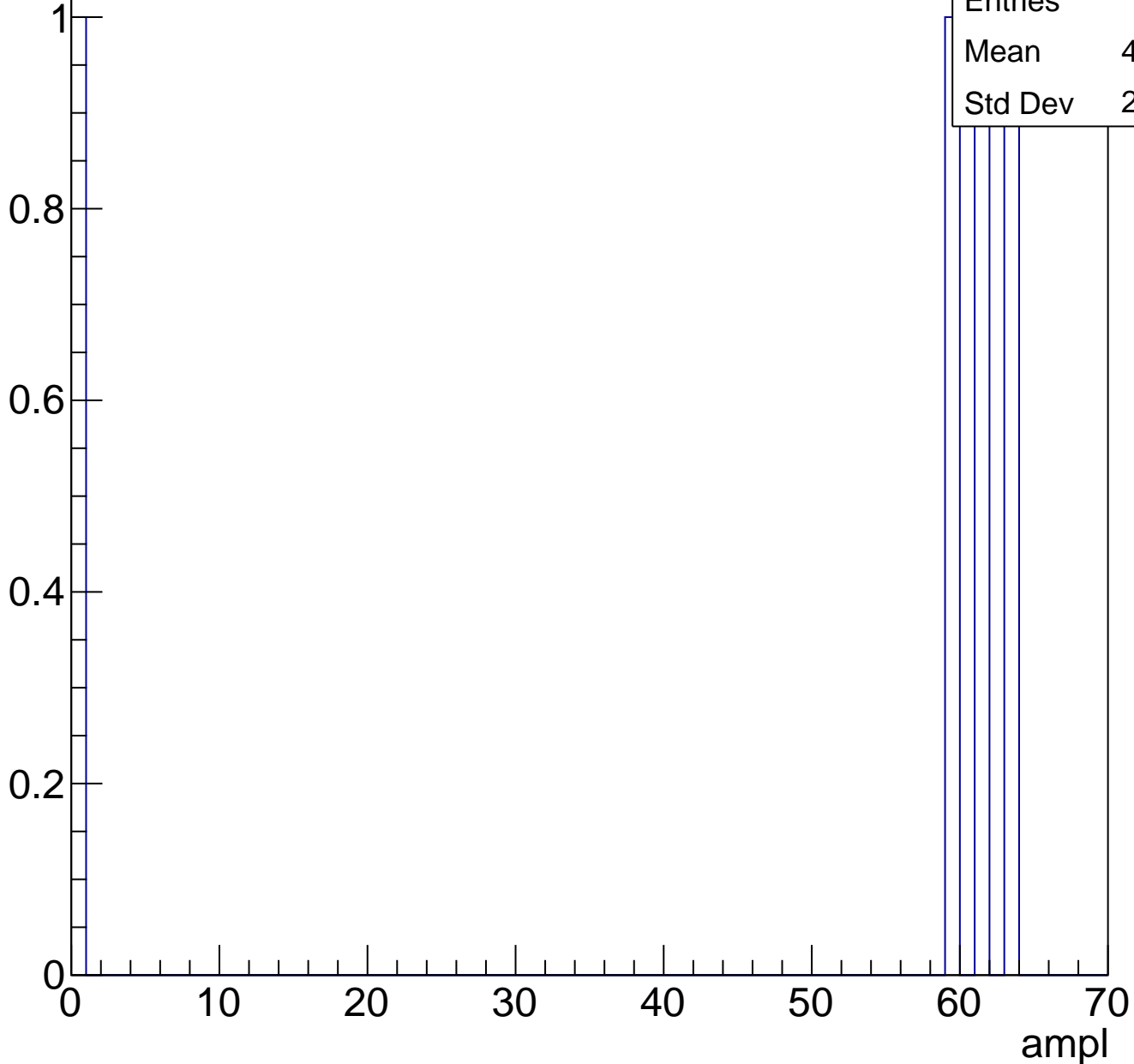
Entries	42
Mean	58.48
Std Dev	9.485



B1L103S, U11-ch13, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

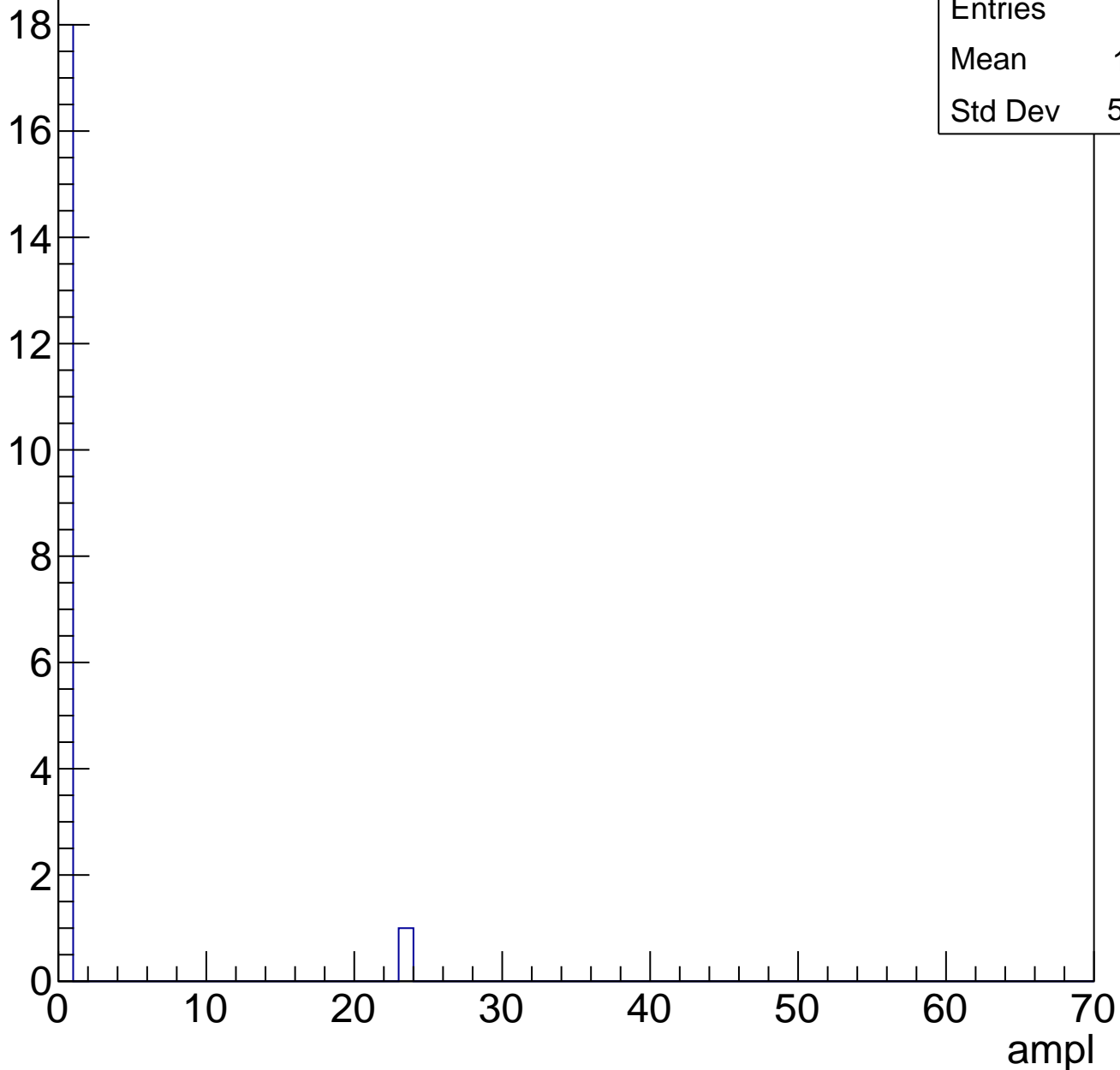


B1L103S, U11-ch13, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.211
Std Dev	5.136

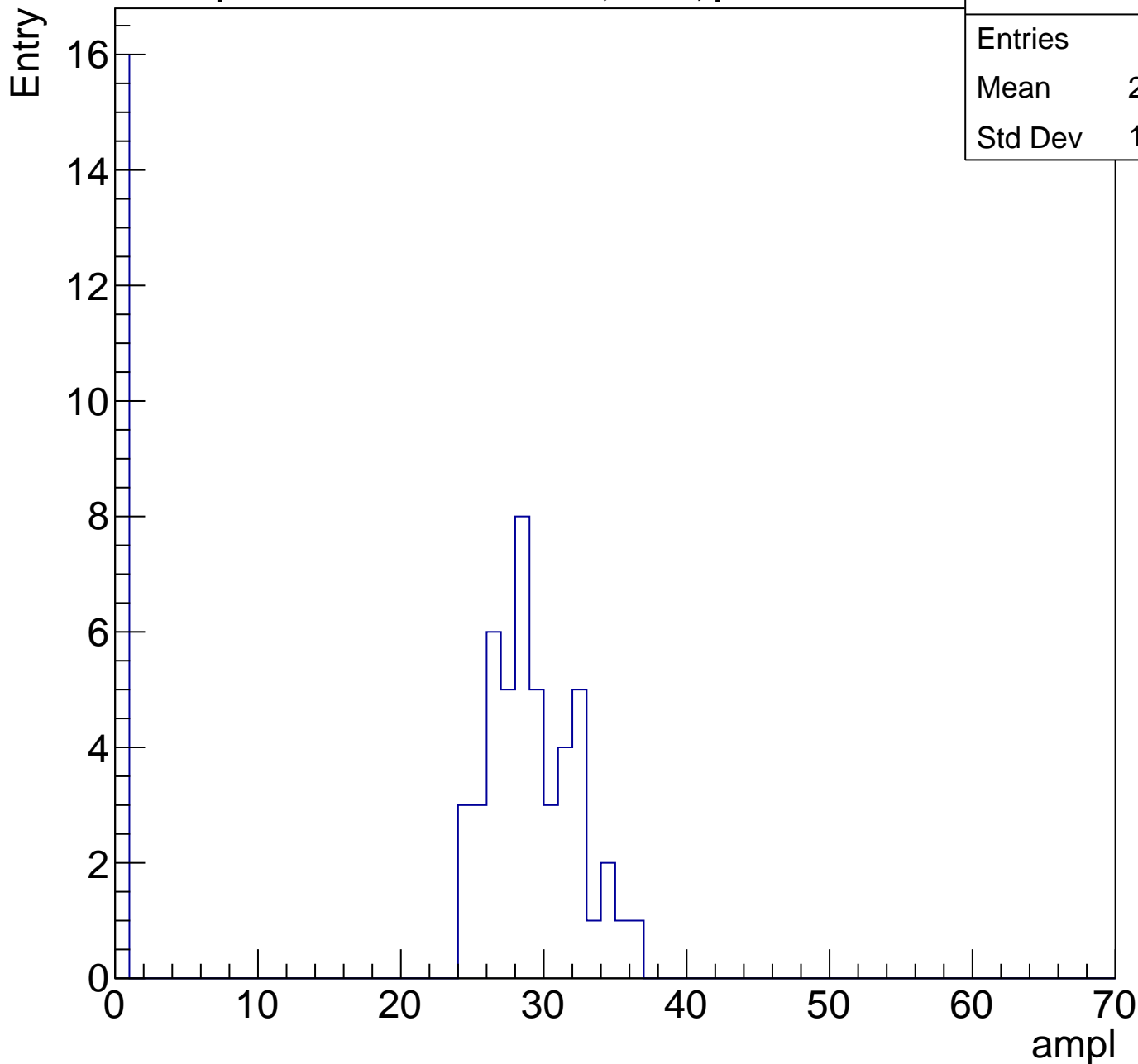
Entry



B1L103S, U11-ch14, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	63
Mean	21.48
Std Dev	12.79



B1L103S, U11-ch14, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	90
Mean	29.87
Std Dev	12.73

Entry

12

10

8

6

4

2

0

0

10

20

30

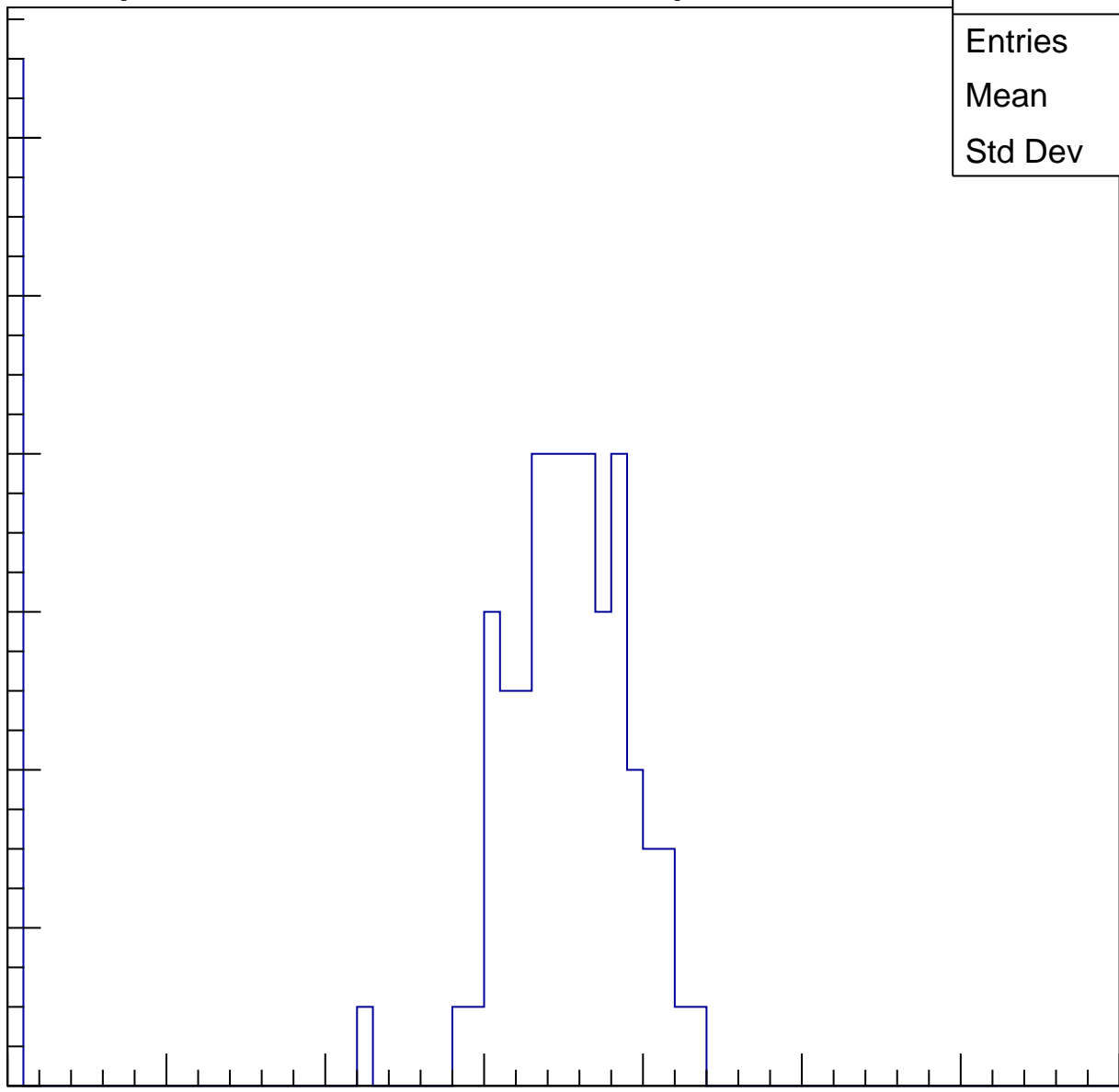
40

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70

ampl

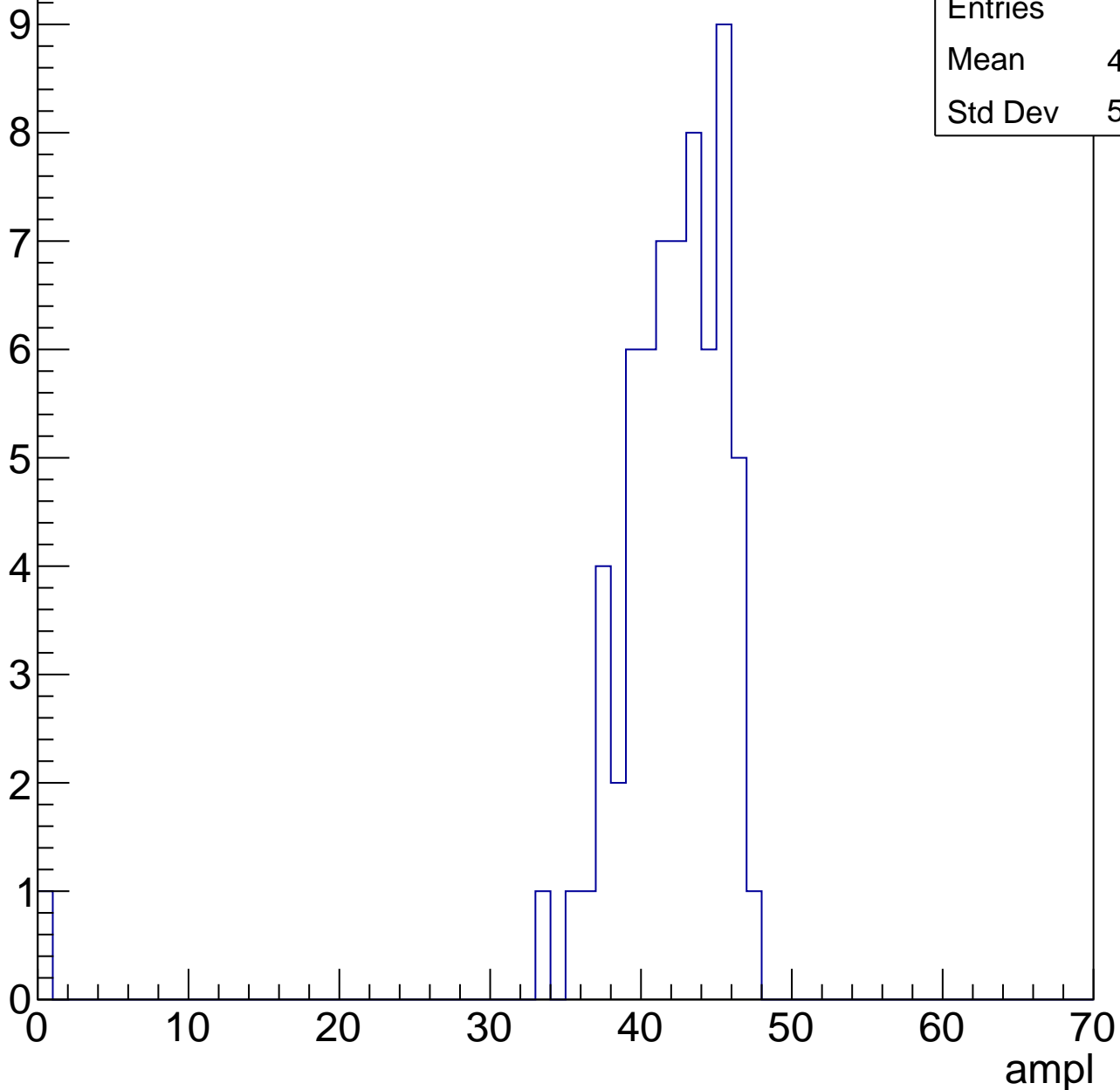


B1L103S, U11-ch14, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	41.12
Std Dev	5.968

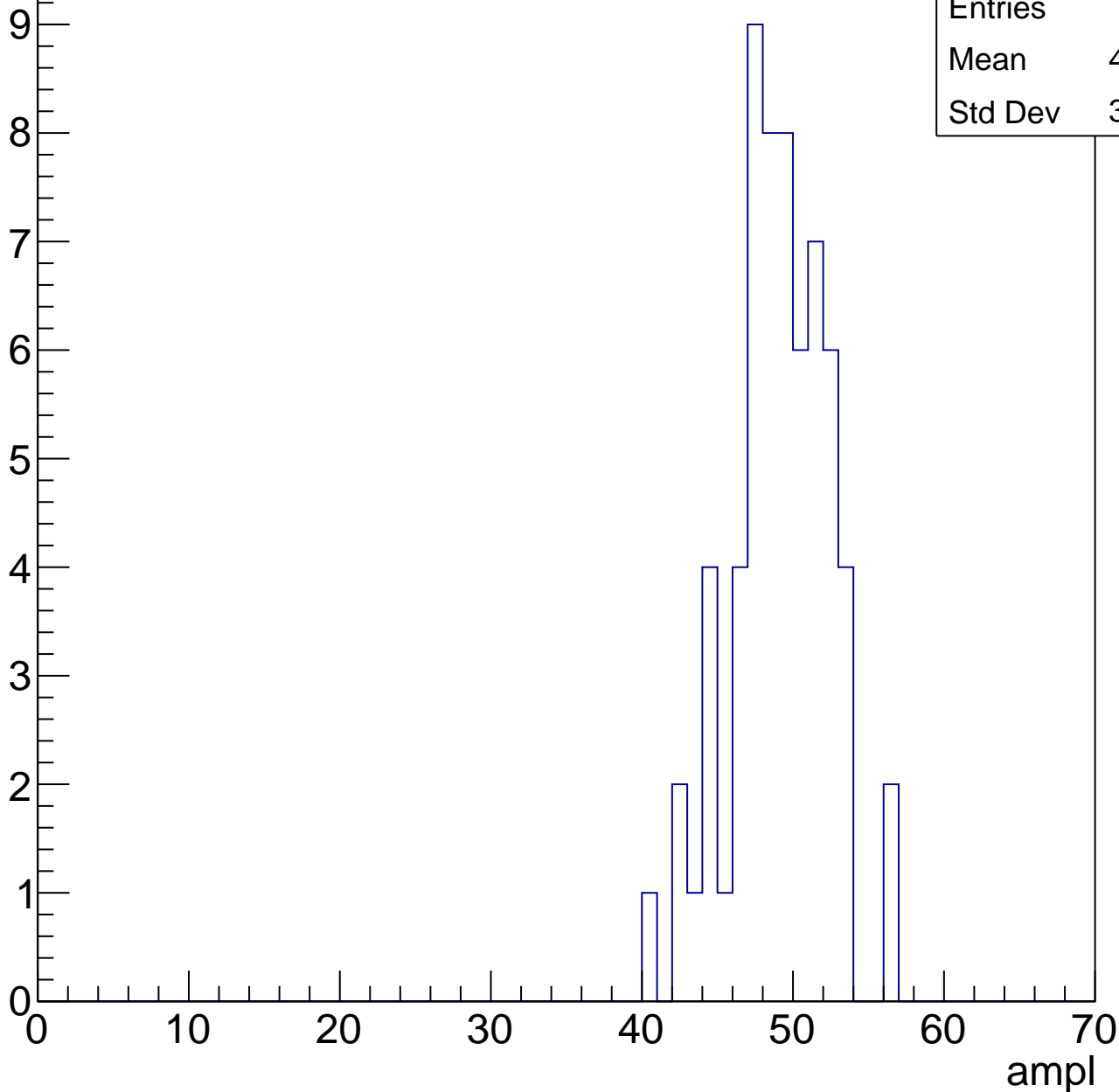


B1L103S, U11-ch14, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	48.63
Std Dev	3.219

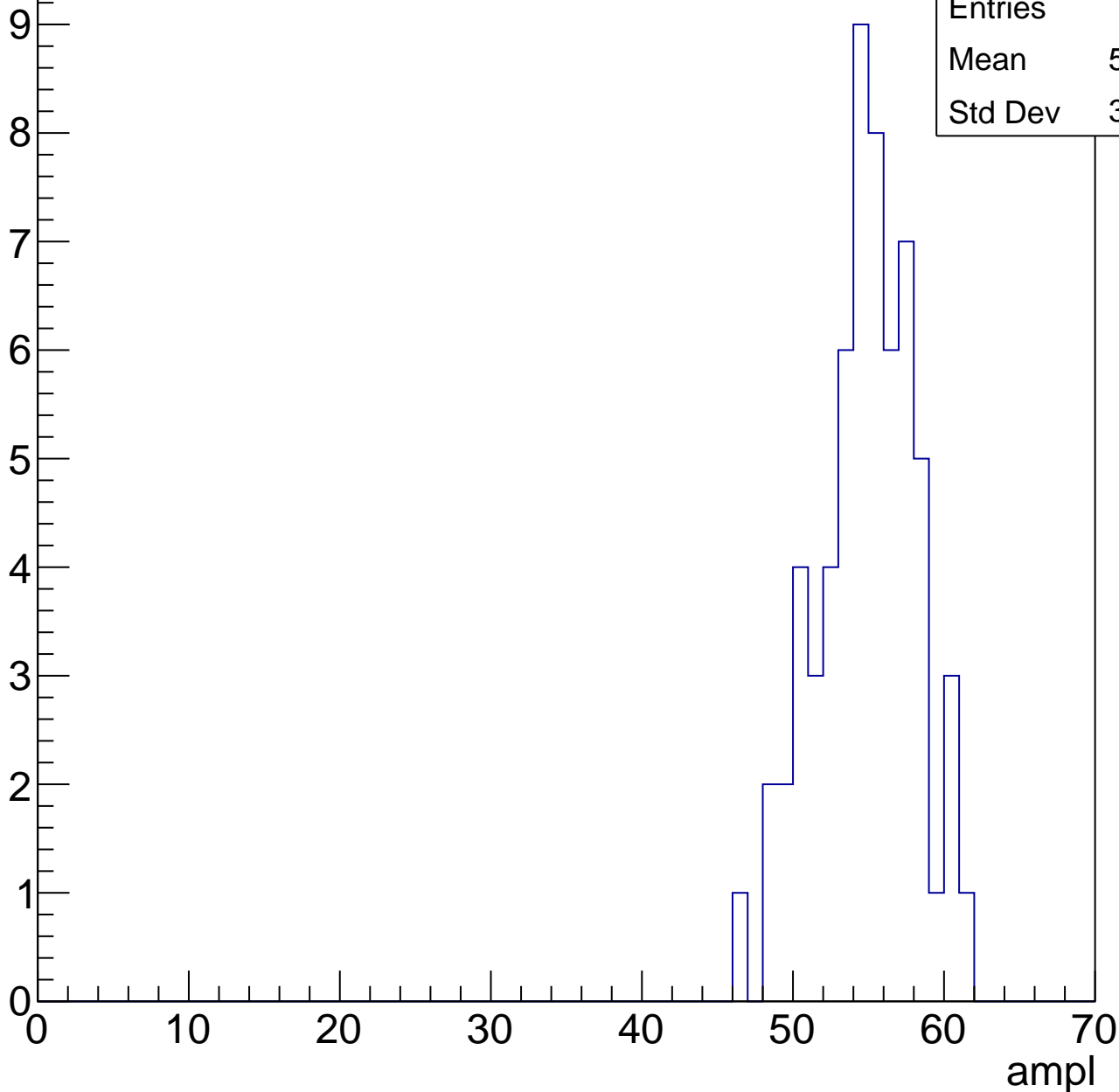


B1L103S, U11-ch14, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

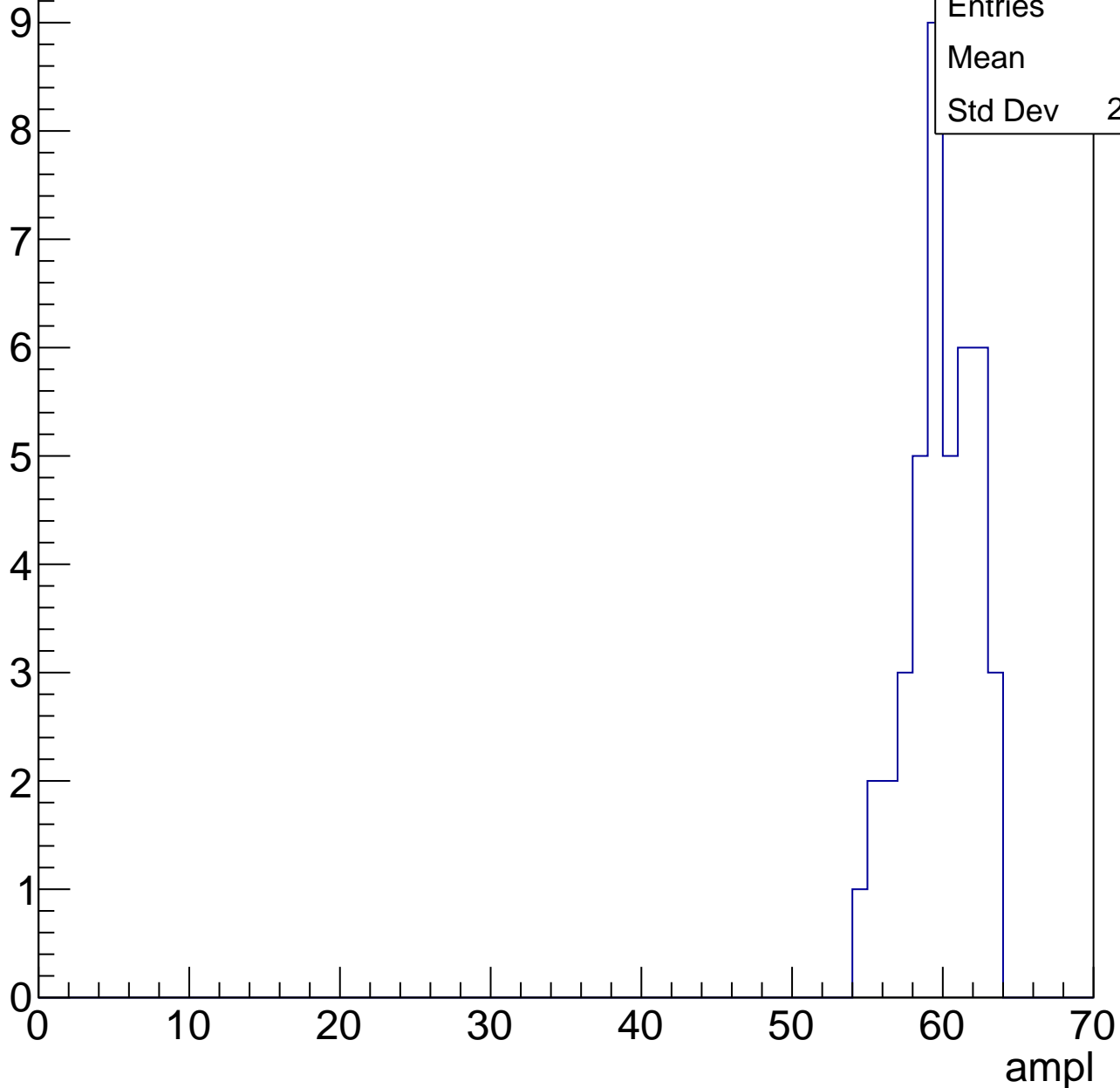
Entries	62
Mean	54.35
Std Dev	3.233



B1L103S, U11-ch14, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

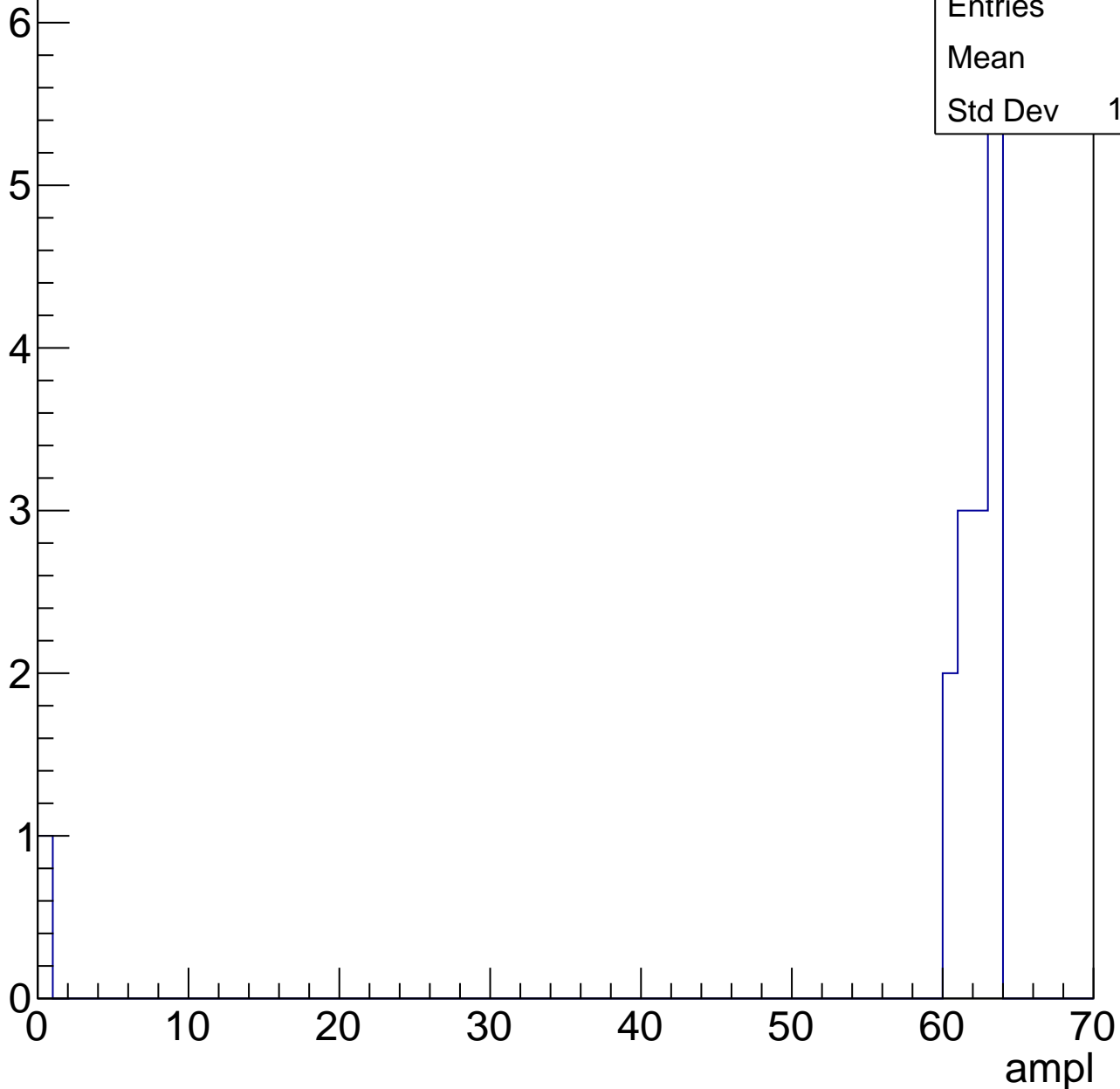


B1L103S, U11-ch14, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	15
Mean	57.8
Std Dev	15.48

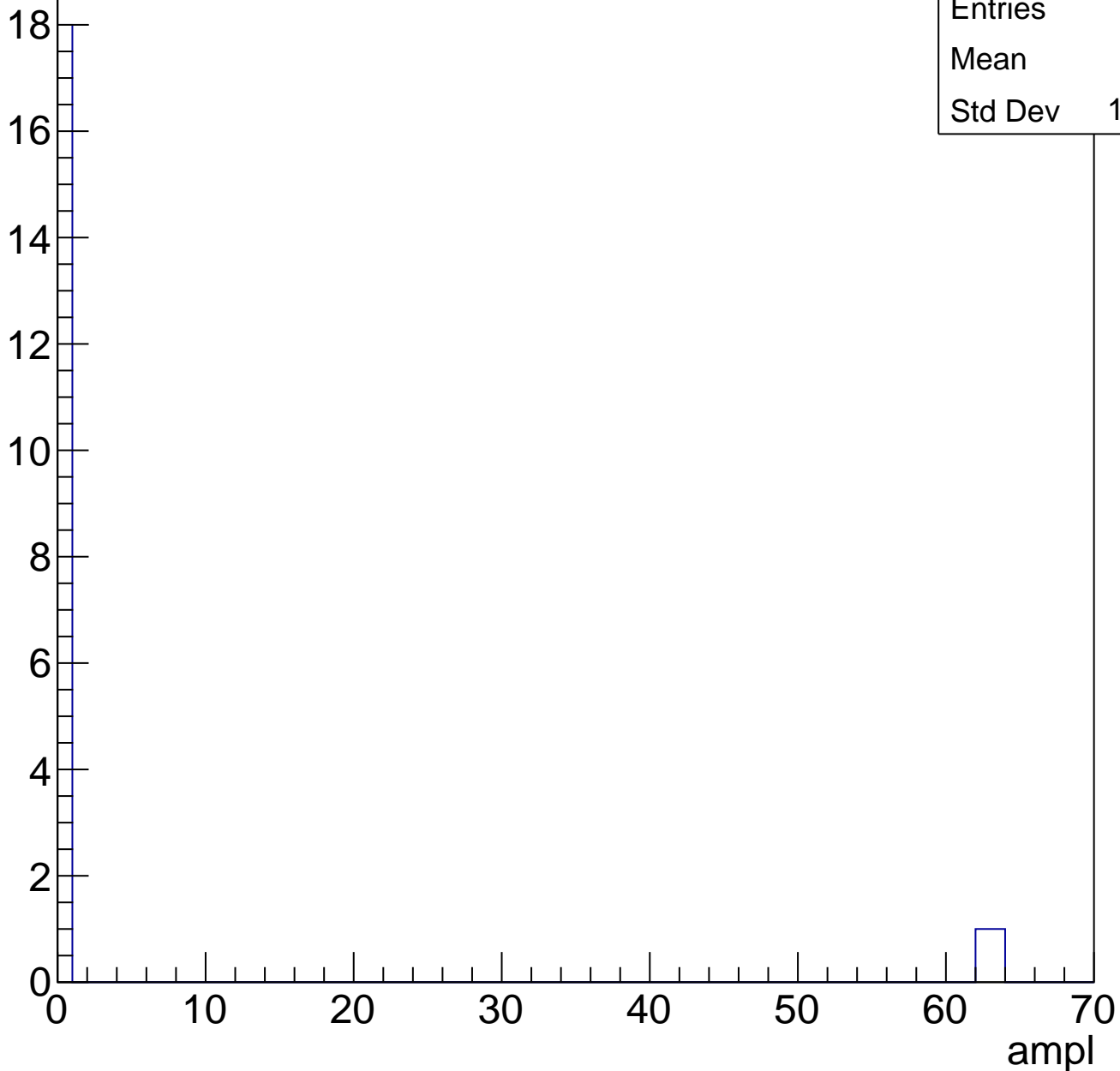


B1L103S, U11-ch14, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	6.25
Std Dev	18.75

Entry

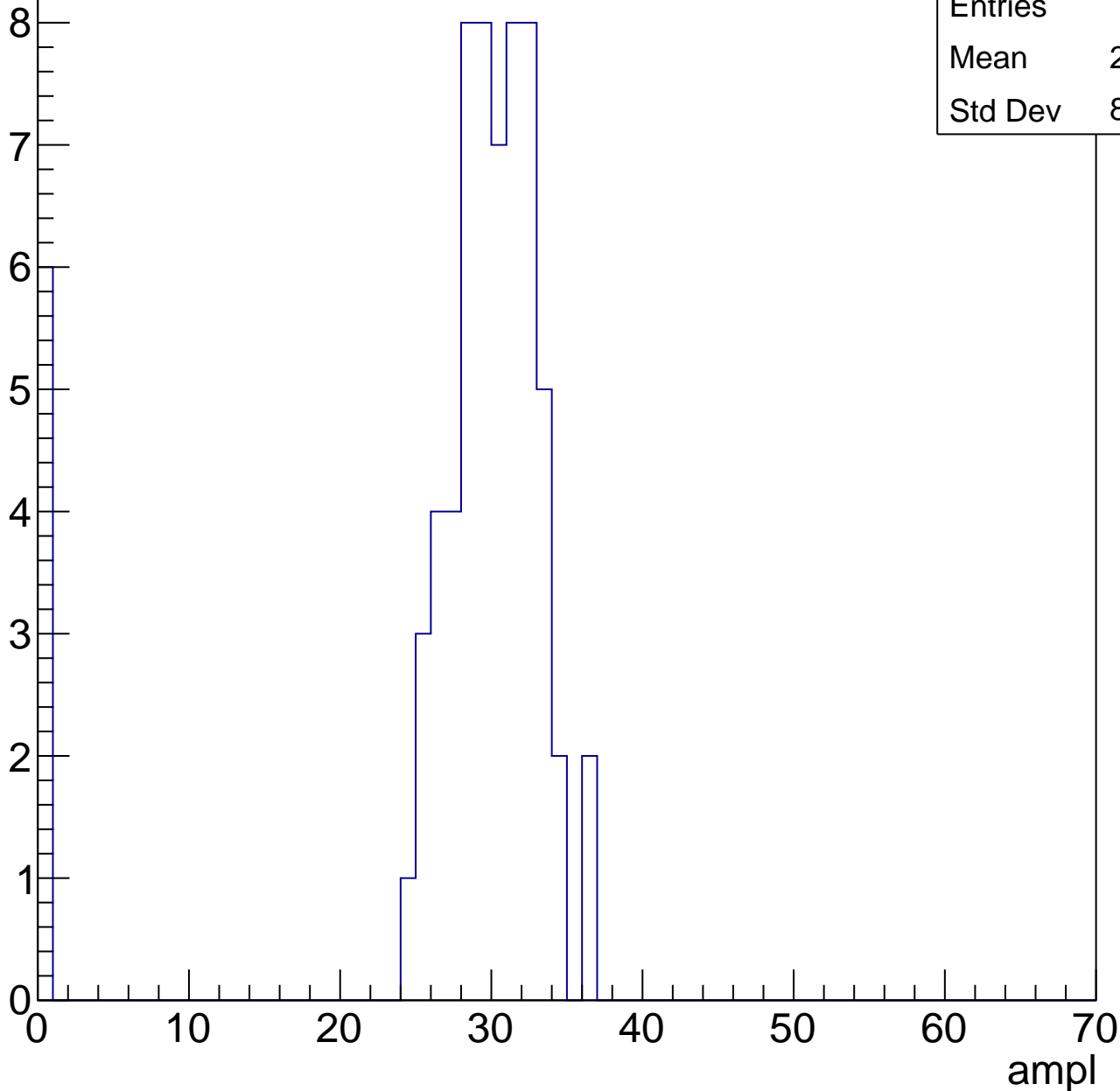


B1L103S, U11-ch15, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	27.06
Std Dev	8.936



B1L103S, U11-ch15, adc1

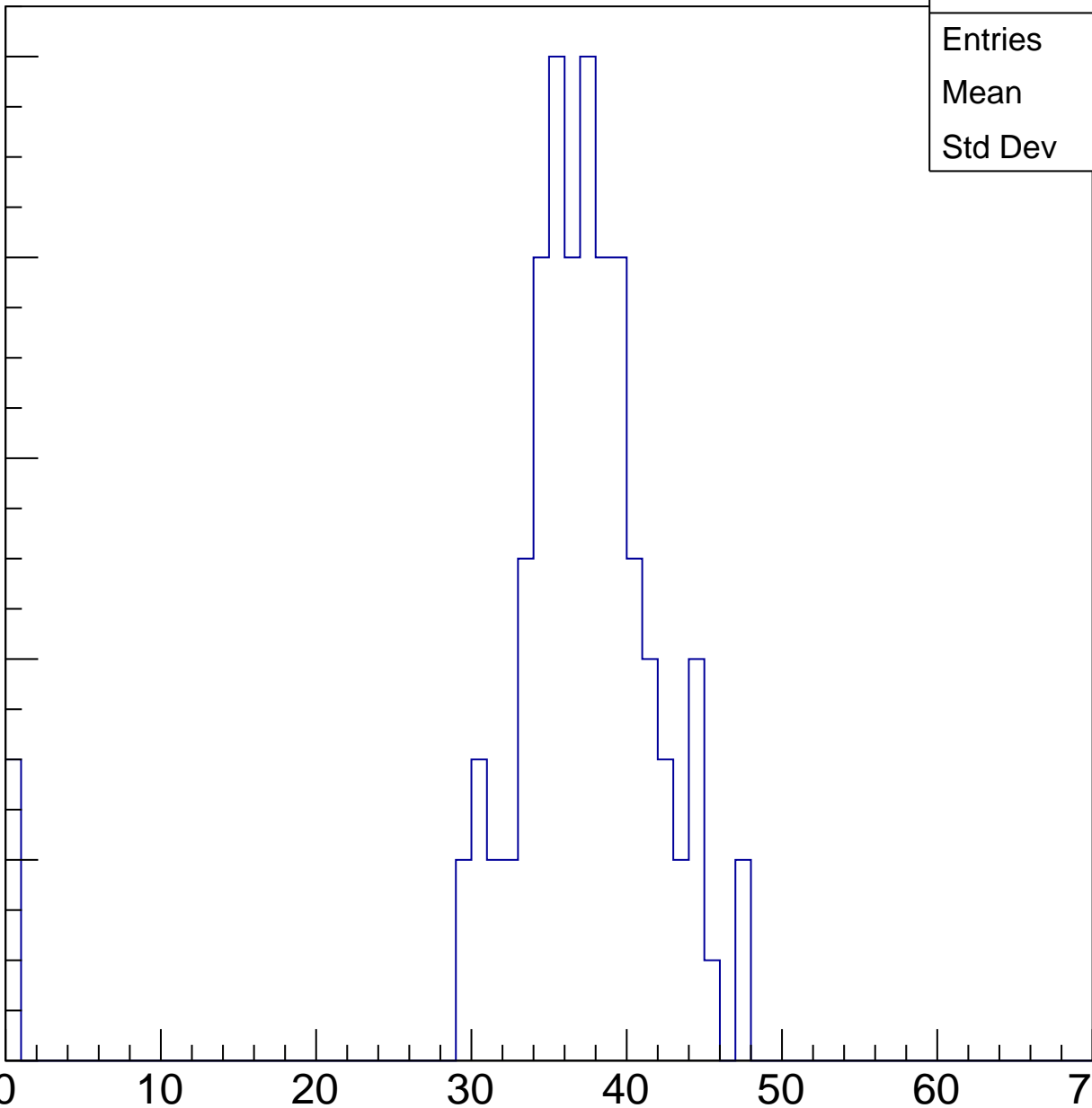
calib_packv5_041523_1651.root, FC#0, port C2

Entries	90
Mean	35.84
Std Dev	7.703

Entry

10
8
6
4
2
0

ampl

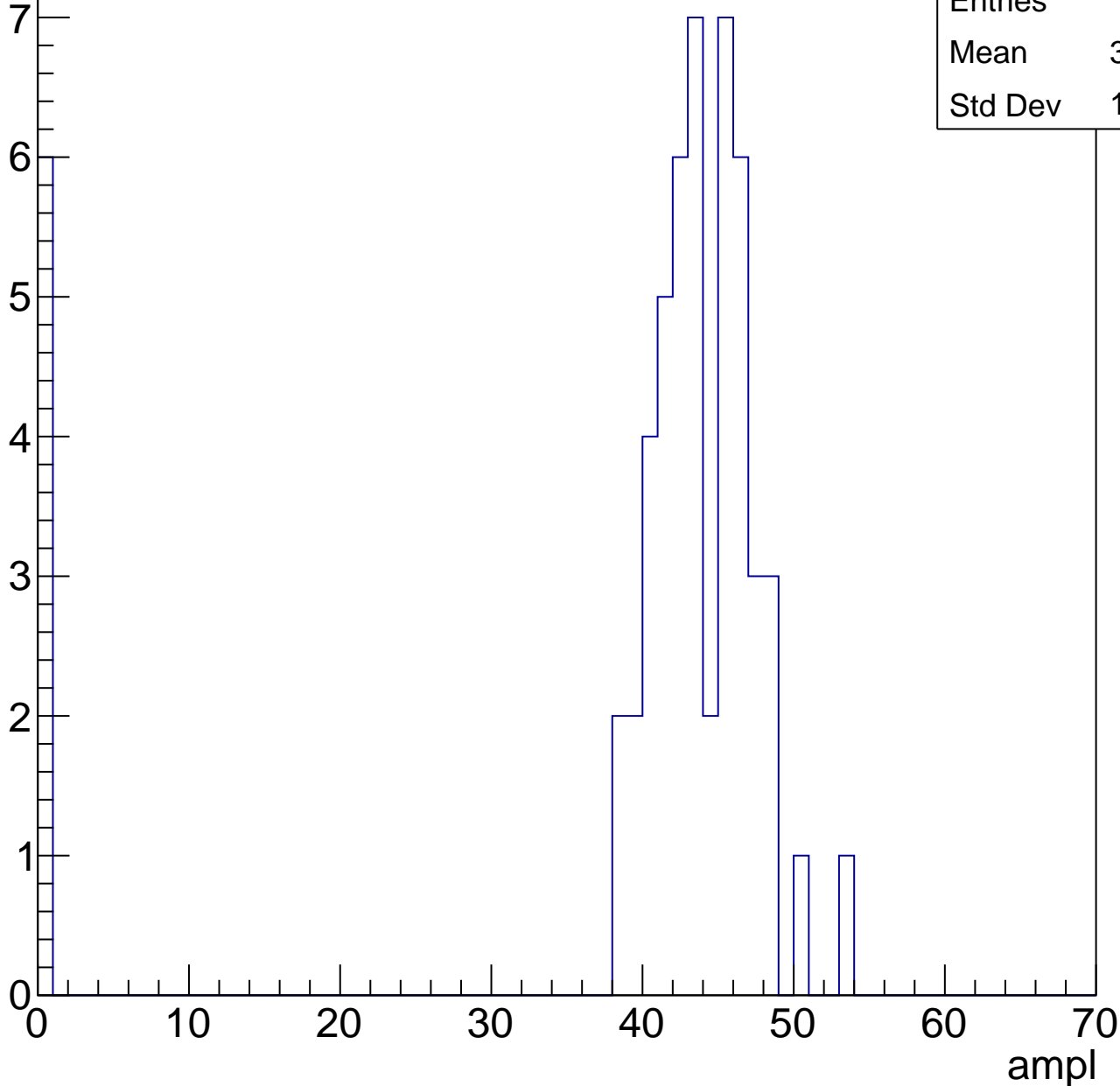


B1L103S, U11-ch15, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	38.89
Std Dev	13.93



B1L103S, U11-ch15, adc3

calib_packv5_041523_1651.root, FC#0, port C2

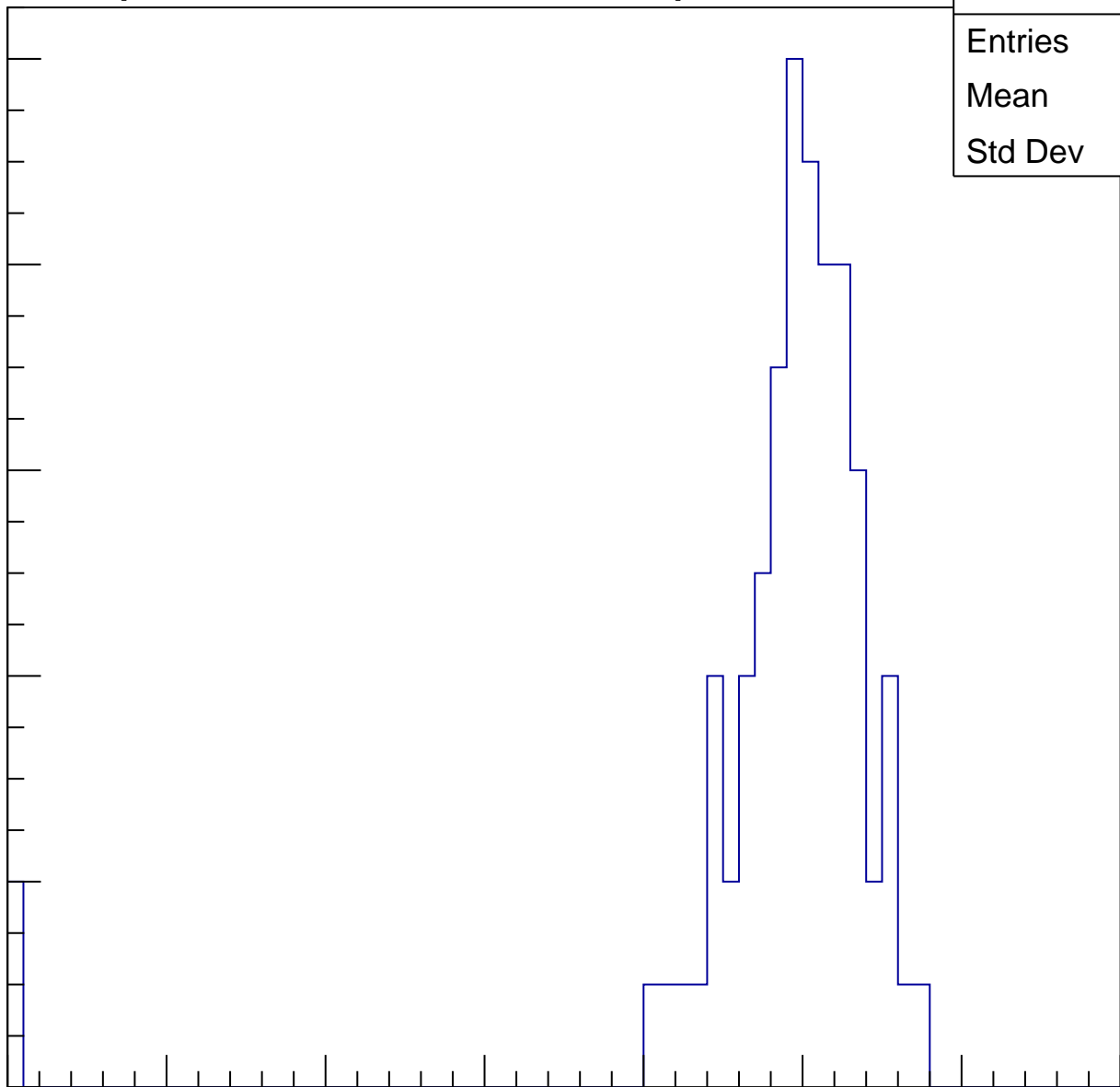
Entries	77
Mean	48.18
Std Dev	8.597

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

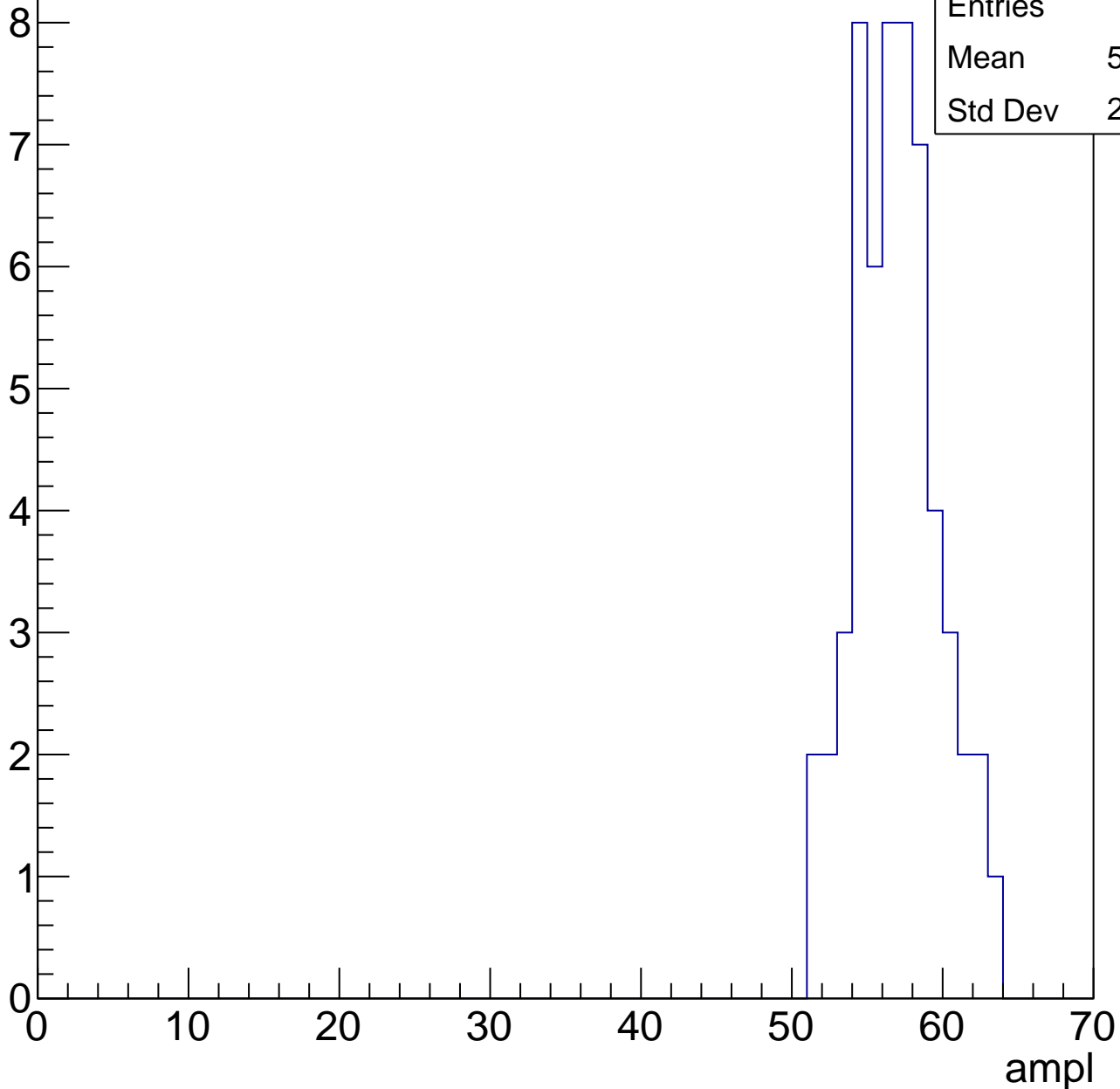


B1L103S, U11-ch15, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	56.46
Std Dev	2.758

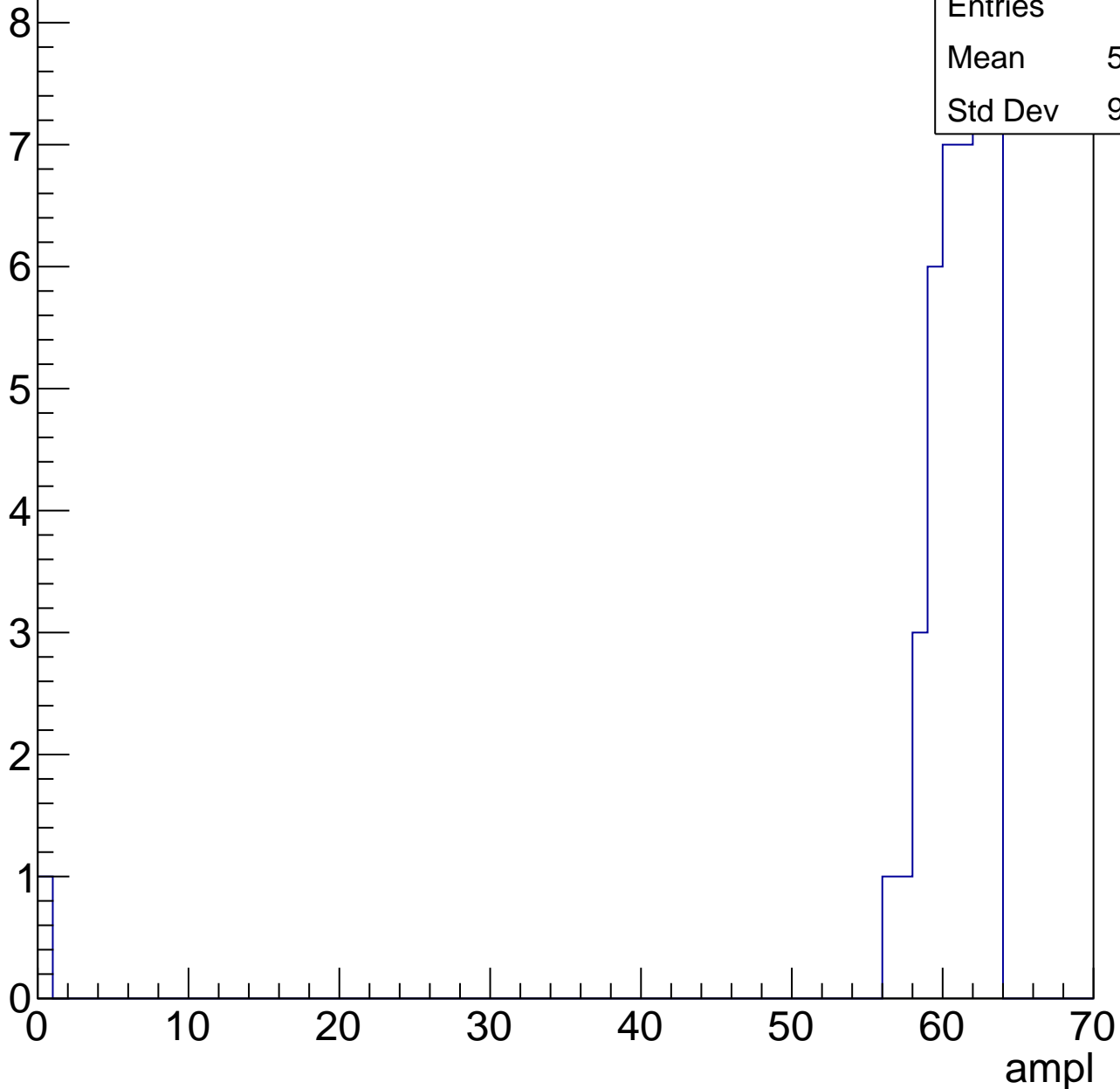


B1L103S, U11-ch15, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	42
Mean	59.24
Std Dev	9.423



B1L103S, U11-ch15, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch15, adc7

calib_packv5_041523_1651.root, FC#0, port C2

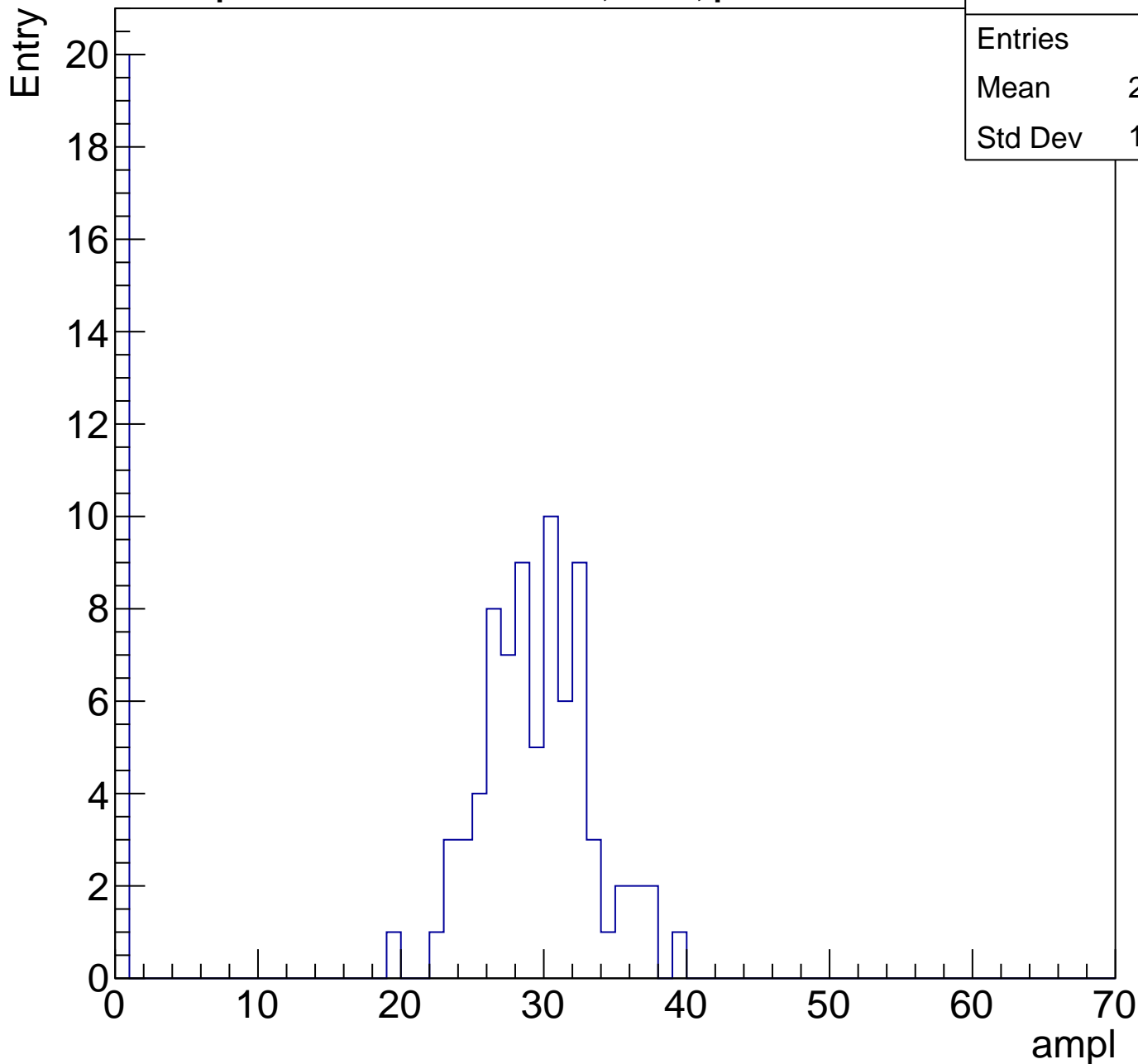
Entry



B1L103S, U11-ch16, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	97
Mean	23.07
Std Dev	12.23

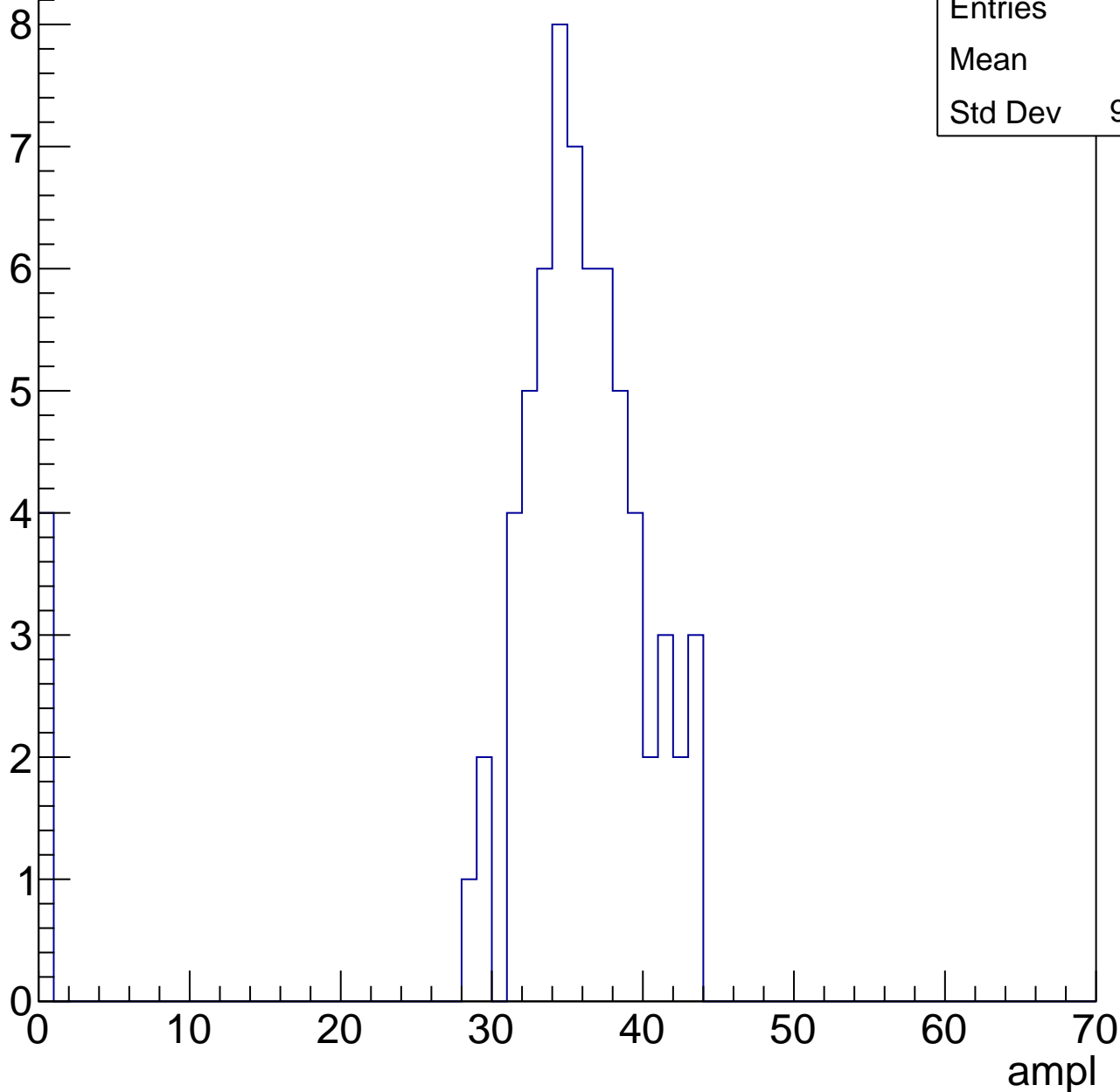


B1L103S, U11-ch16, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	33.6
Std Dev	9.088

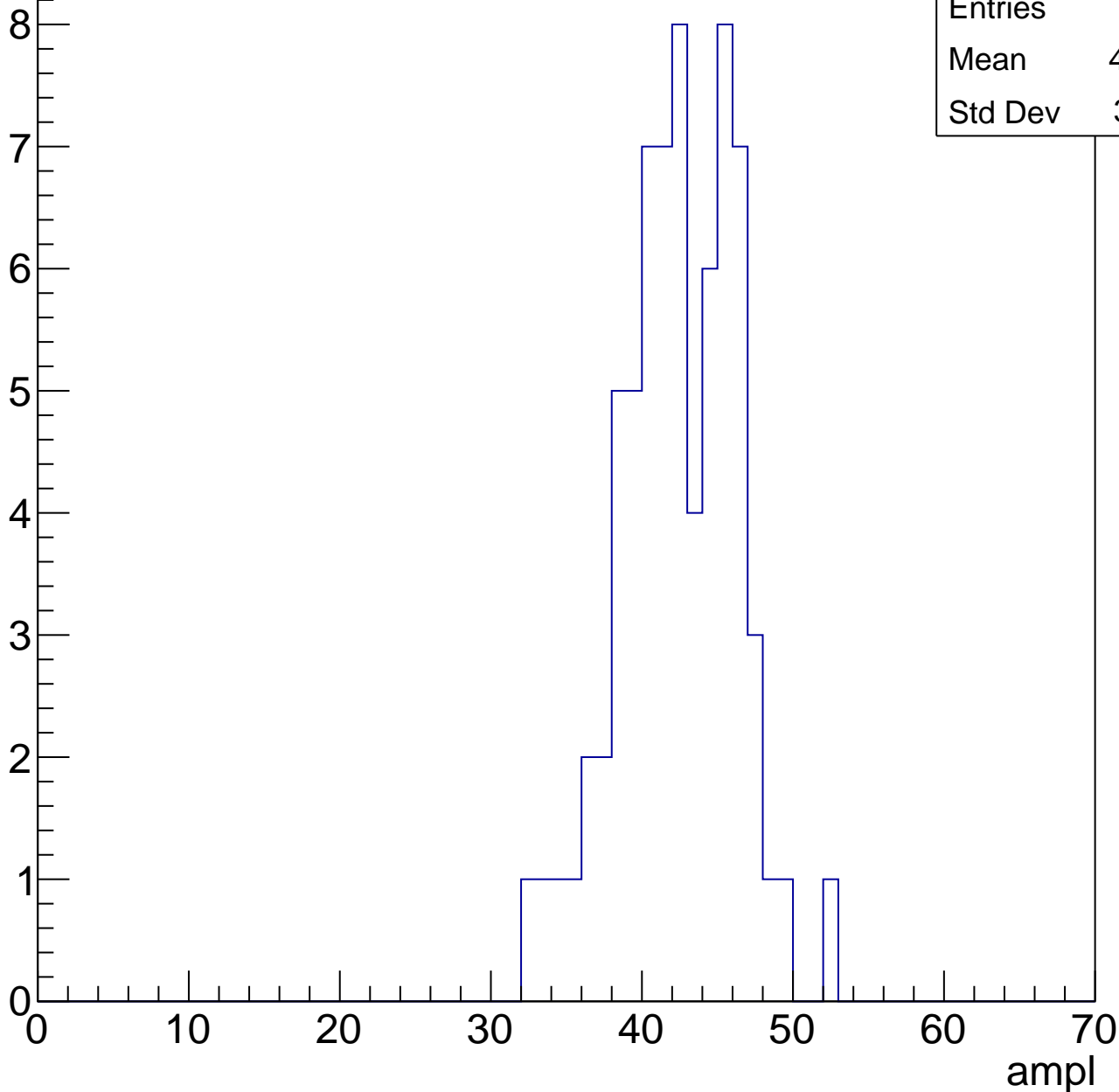


B1L103S, U11-ch16, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	41.92
Std Dev	3.841

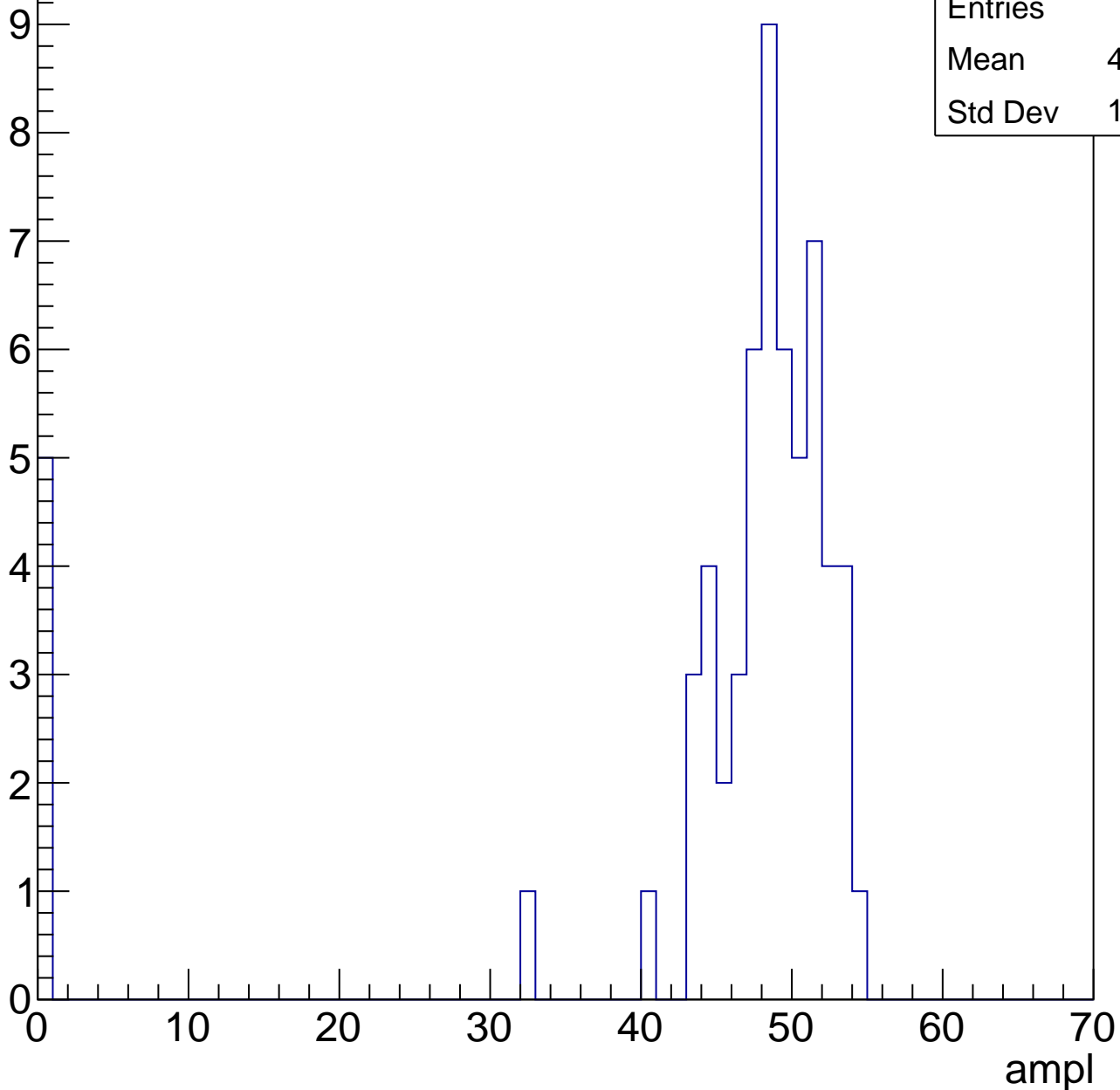


B1L103S, U11-ch16, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	44.16
Std Dev	13.67



B1L103S, U11-ch16, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	68
Mean	53.12
Std Dev	9.817

Entry

10

8

6

4

2

0

0

10

20

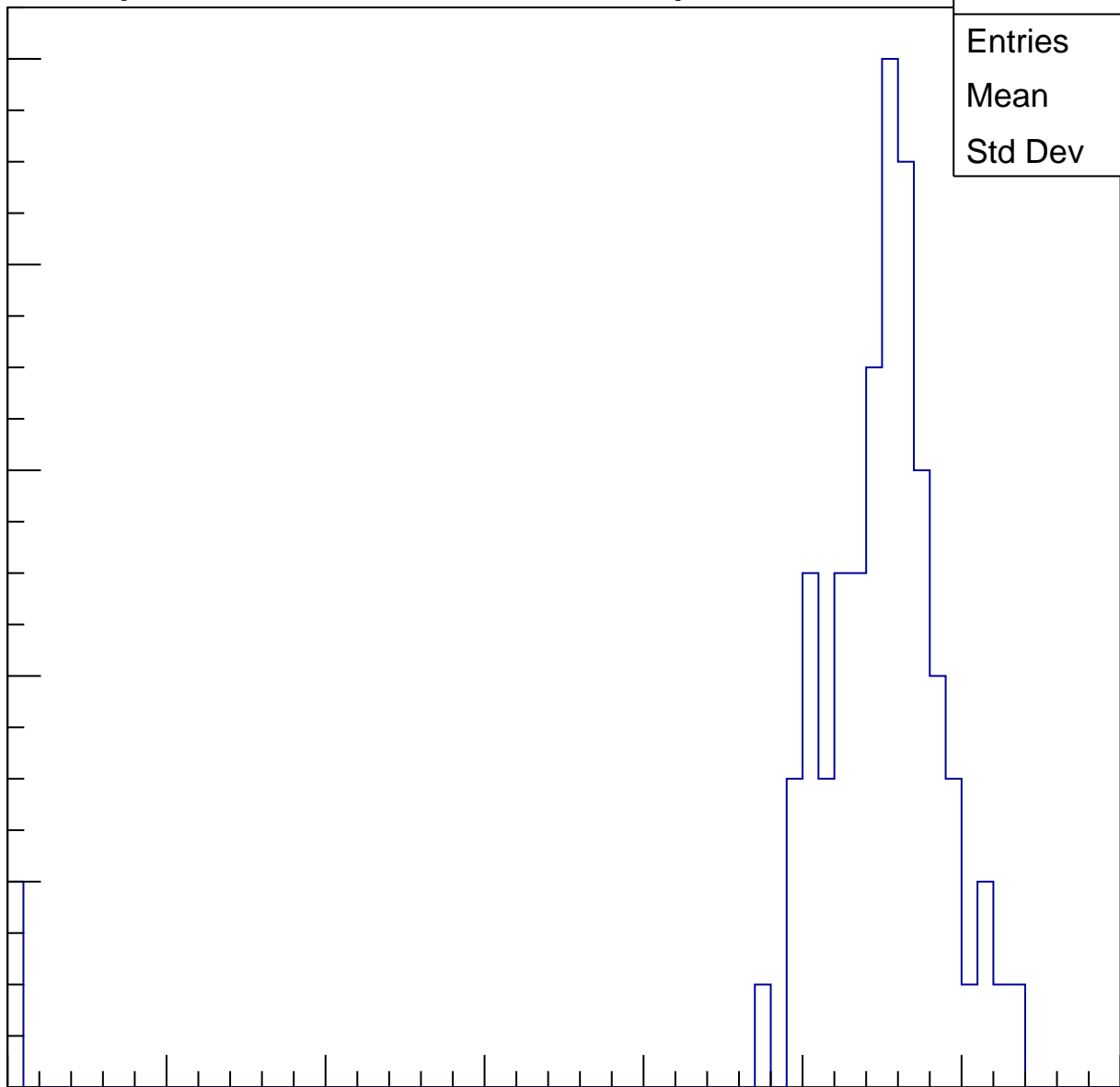
30

40

50

60

ampl

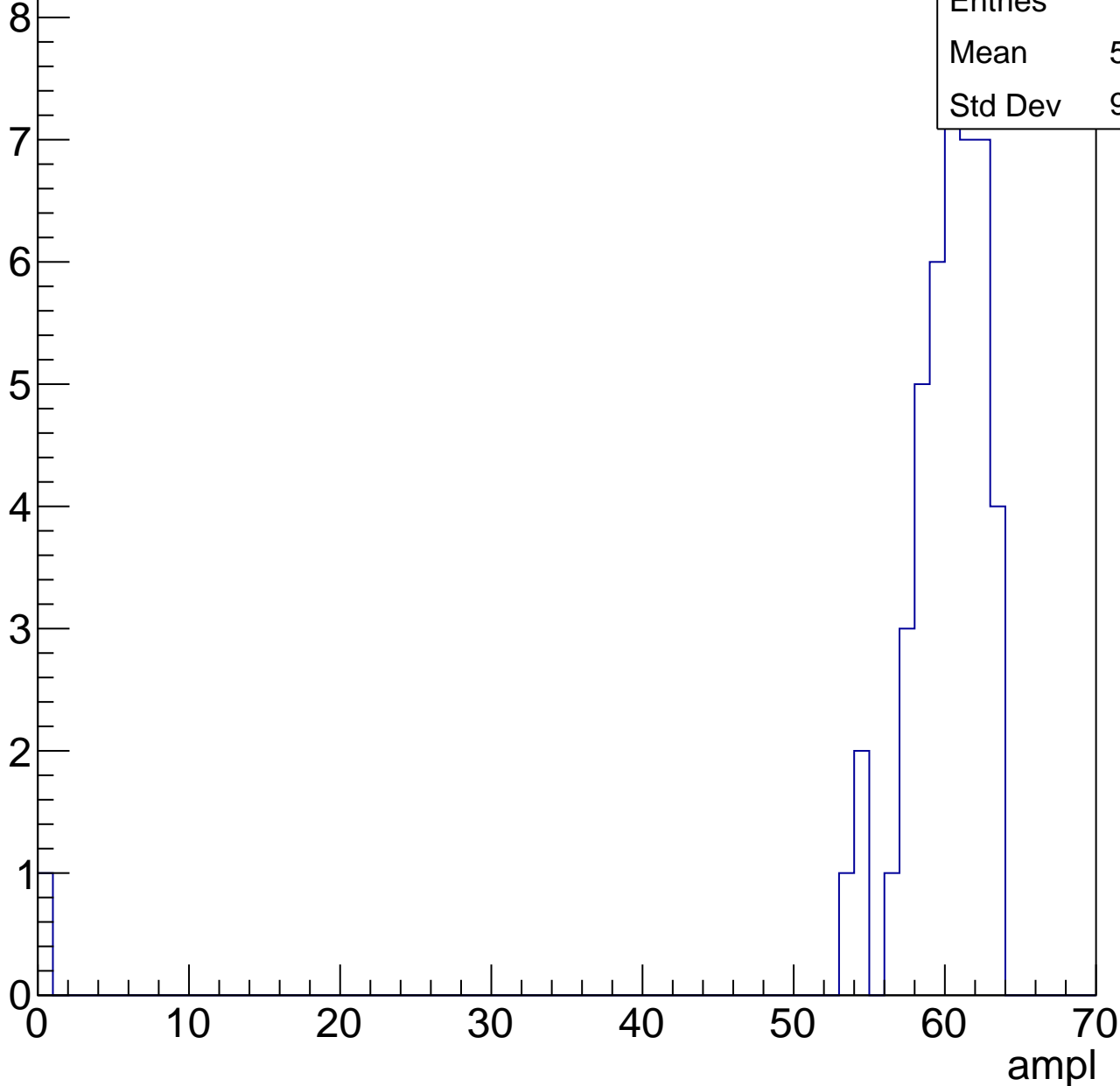


B1L103S, U11-ch16, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

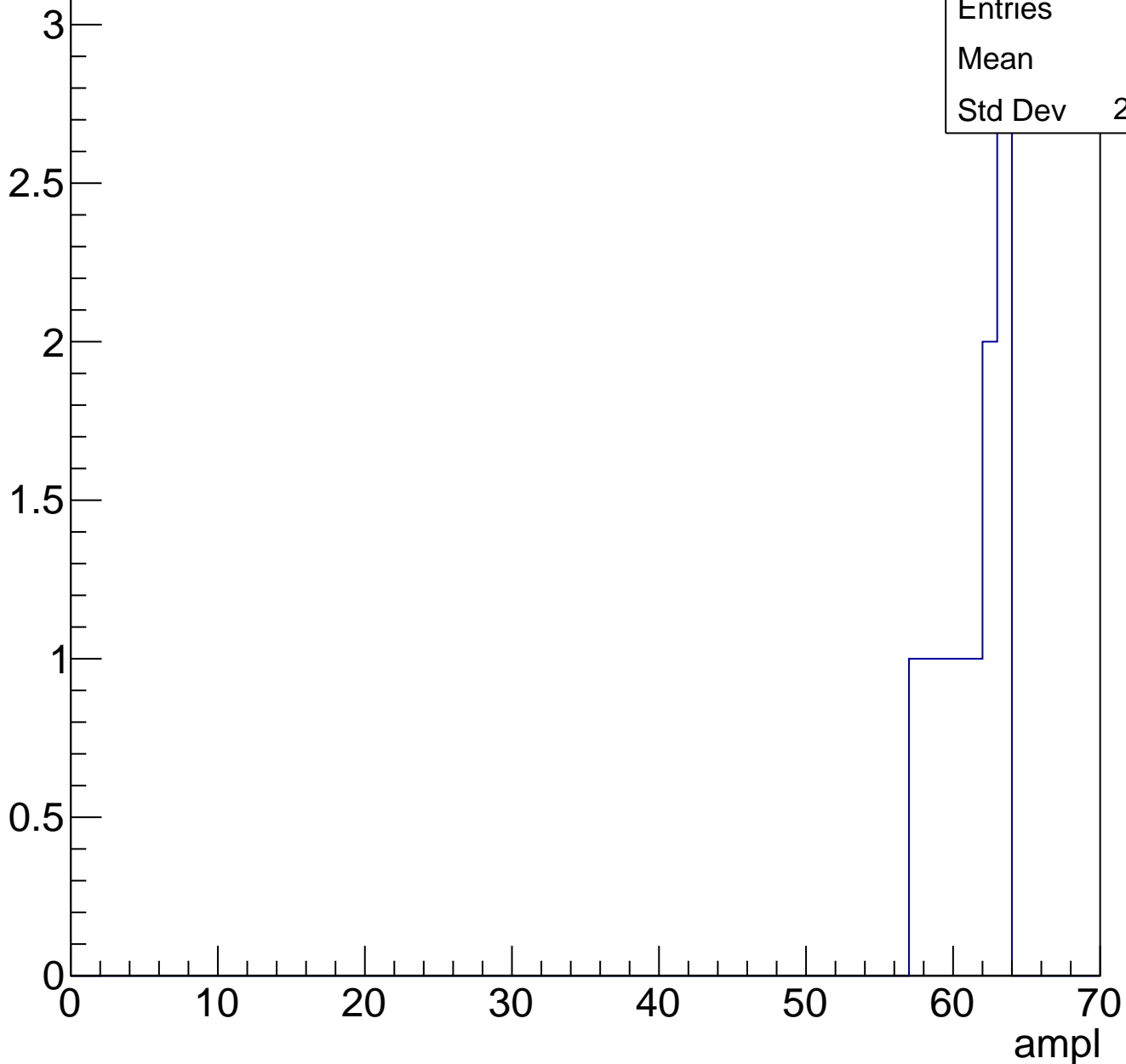
Entries	45
Mean	58.33
Std Dev	9.112



B1L103S, U11-ch16, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

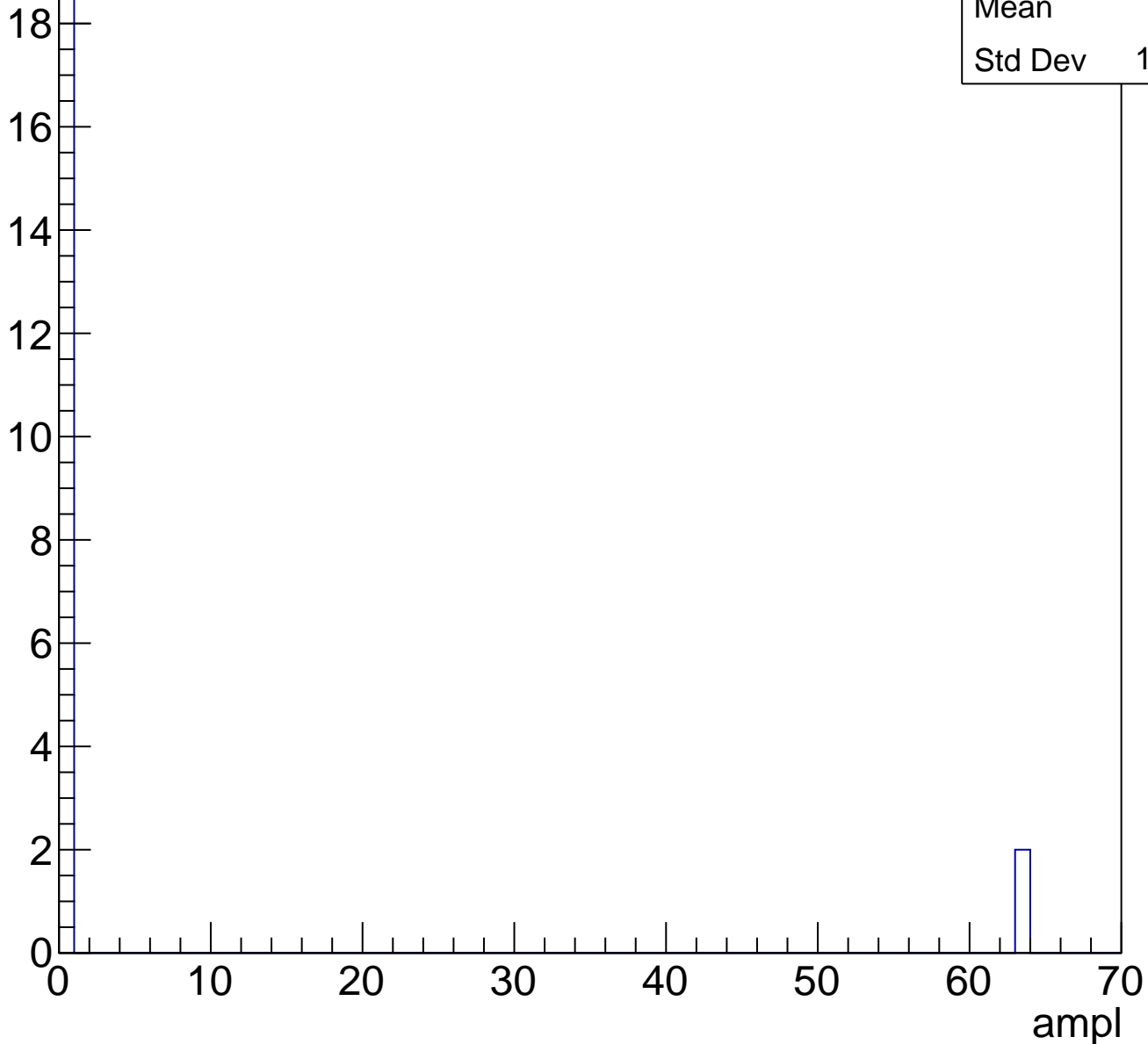


B1L103S, U11-ch16, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	6
Std Dev	18.49

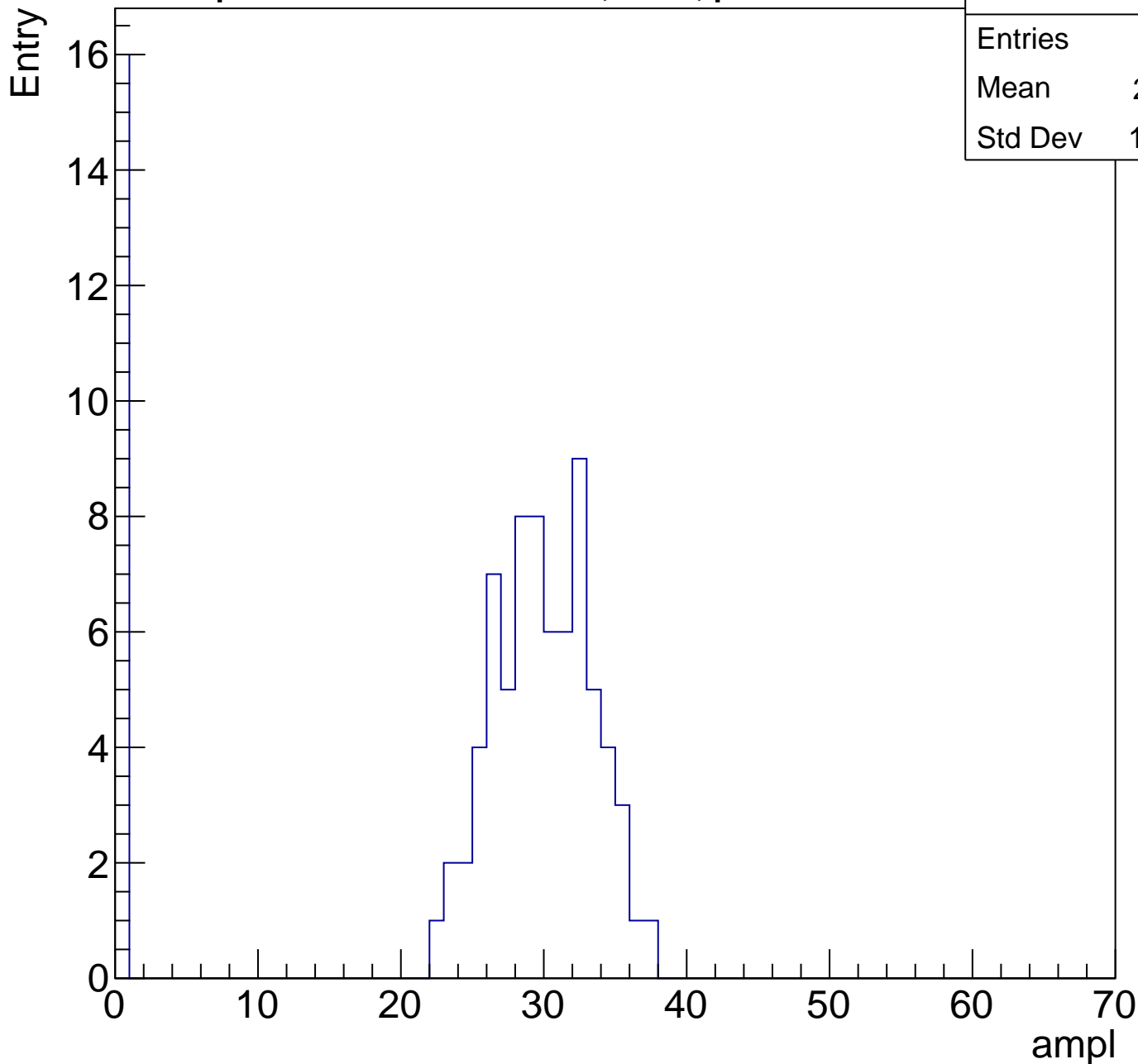
Entry



B1L103S, U11-ch17, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	88
Mean	24.11
Std Dev	11.77



B1L103S, U11-ch17, adc1

calib_packv5_041523_1651.root, FC#0, port C2

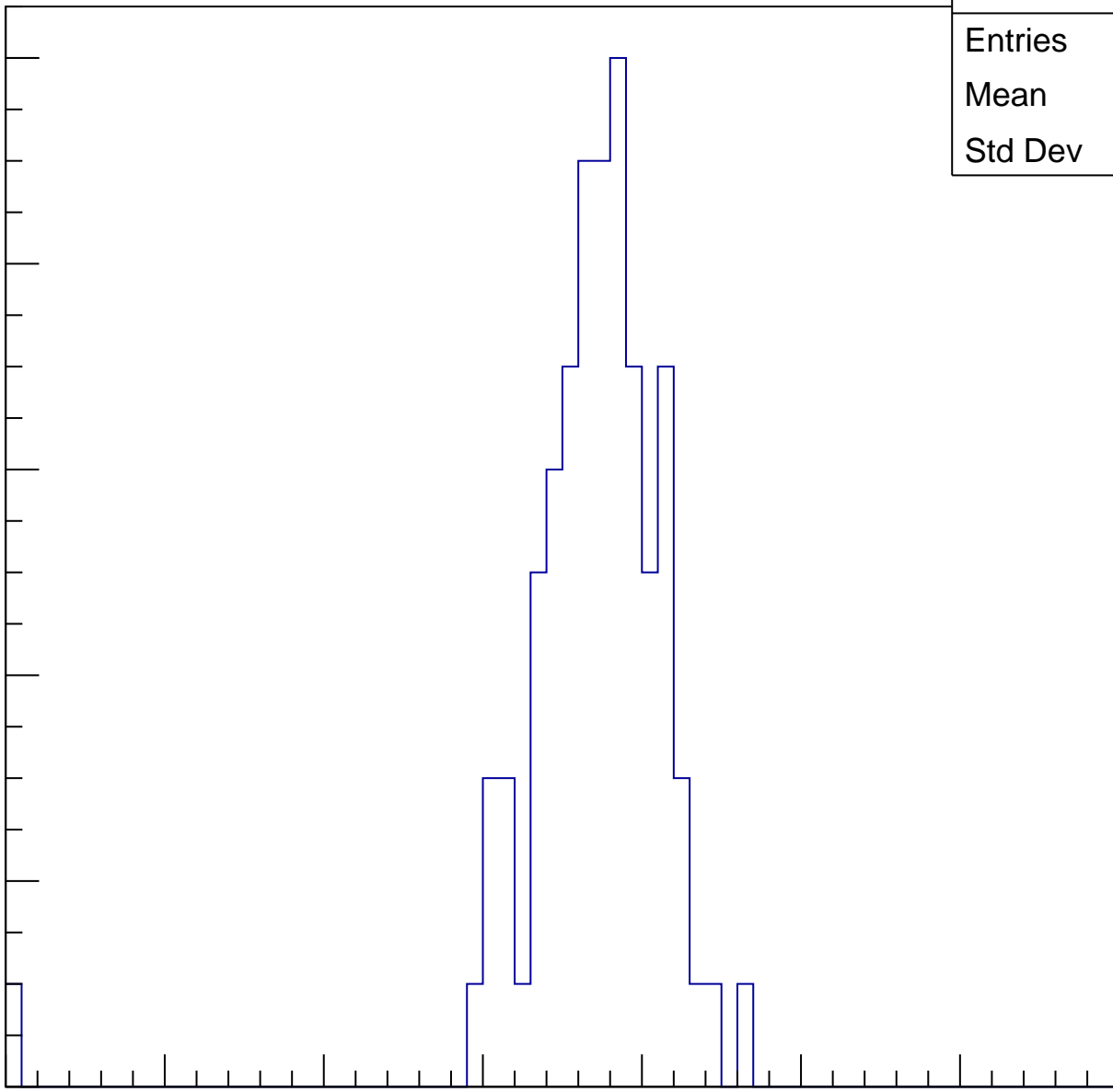
Entries	80
Mean	36.42
Std Dev	5.354

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

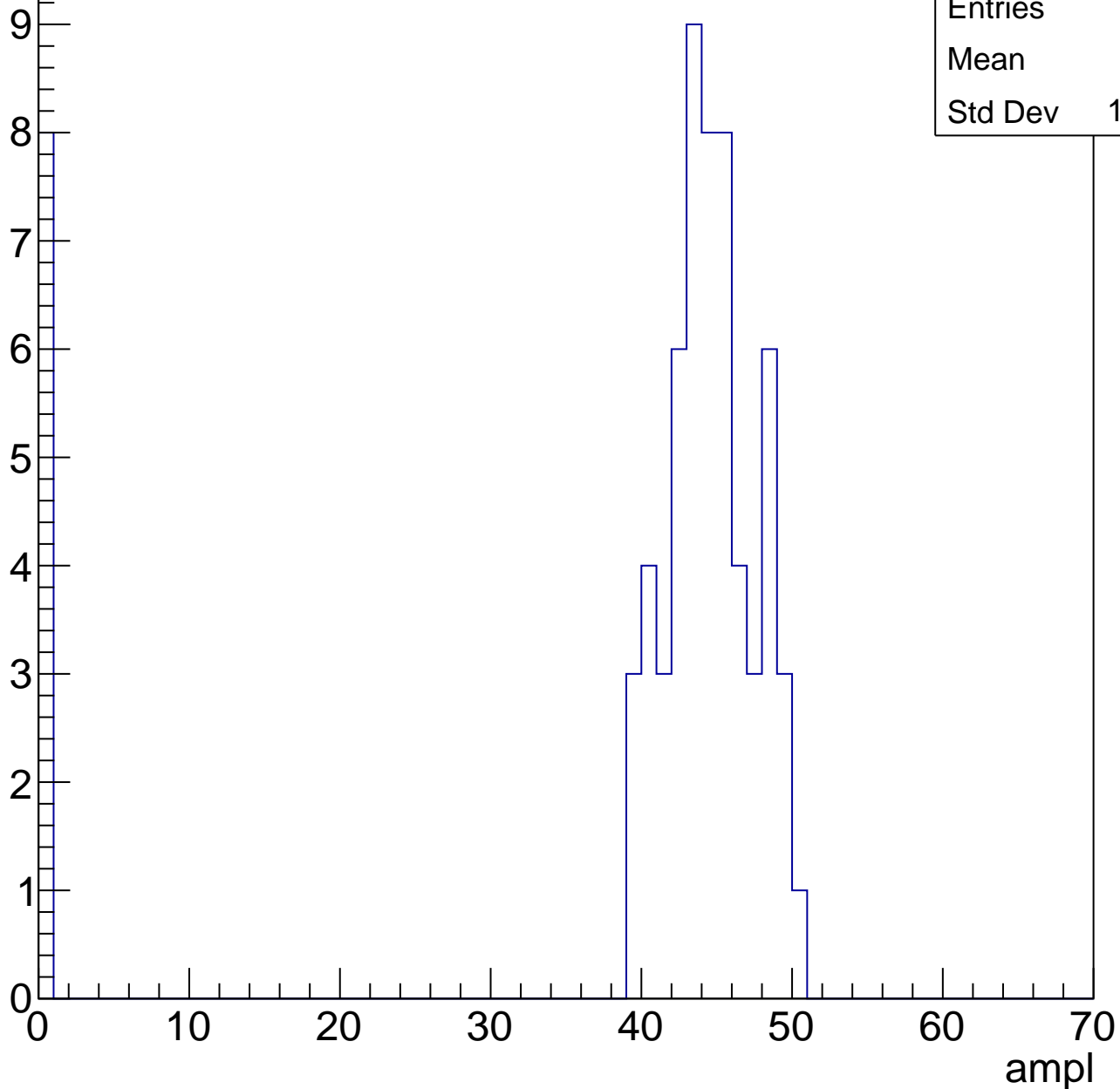
ampl



B1L103S, U11-ch17, adc2

calib_packv5_041523_1651.root, FC#0, port C2

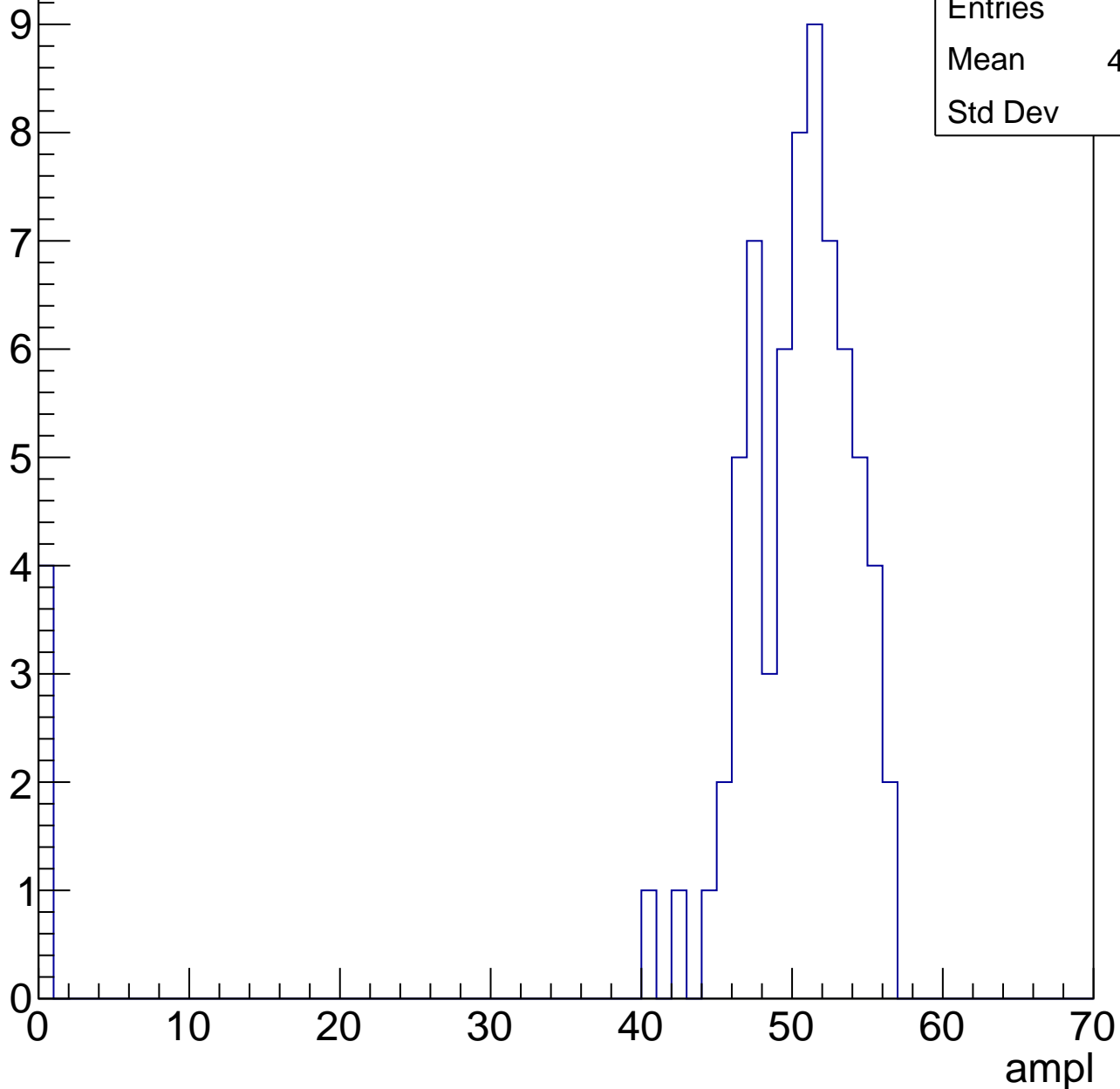
Entry



B1L103S, U11-ch17, adc3

calib_packv5_041523_1651.root, FC#0, port C2

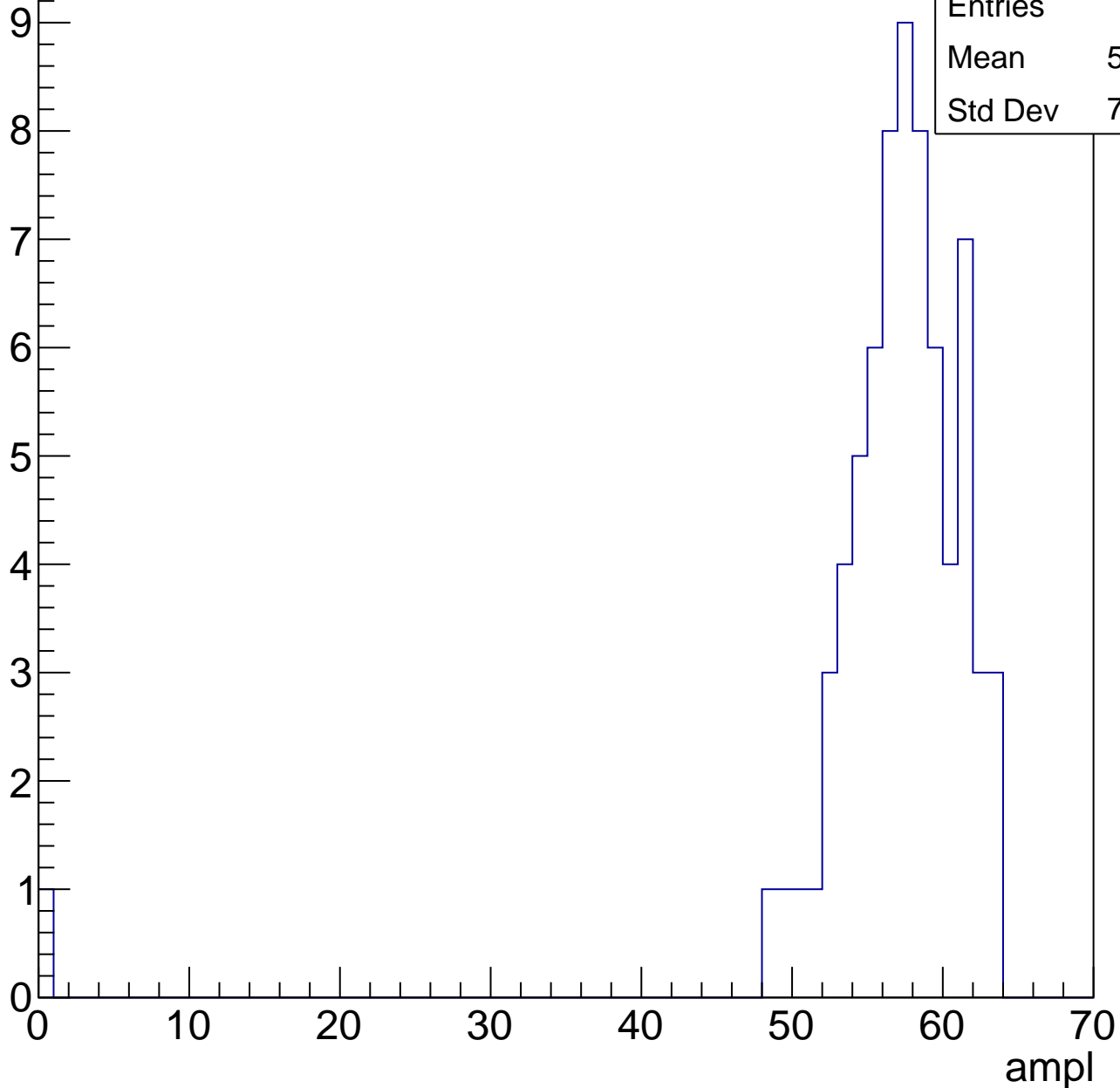
Entry



B1L103S, U11-ch17, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

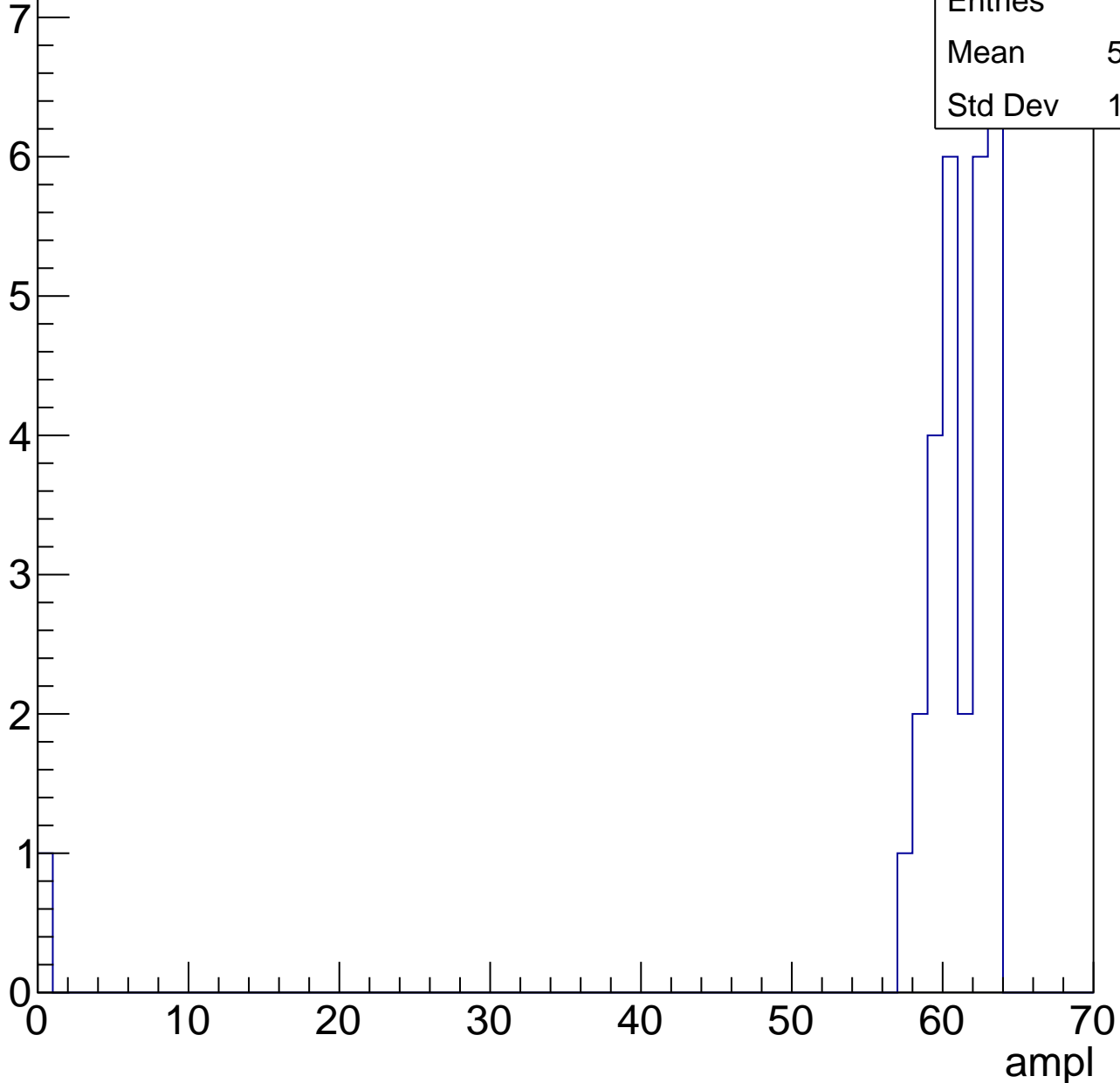


B1L103S, U11-ch17, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	29
Mean	58.76
Std Dev	11.24



B1L103S, U11-ch17, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

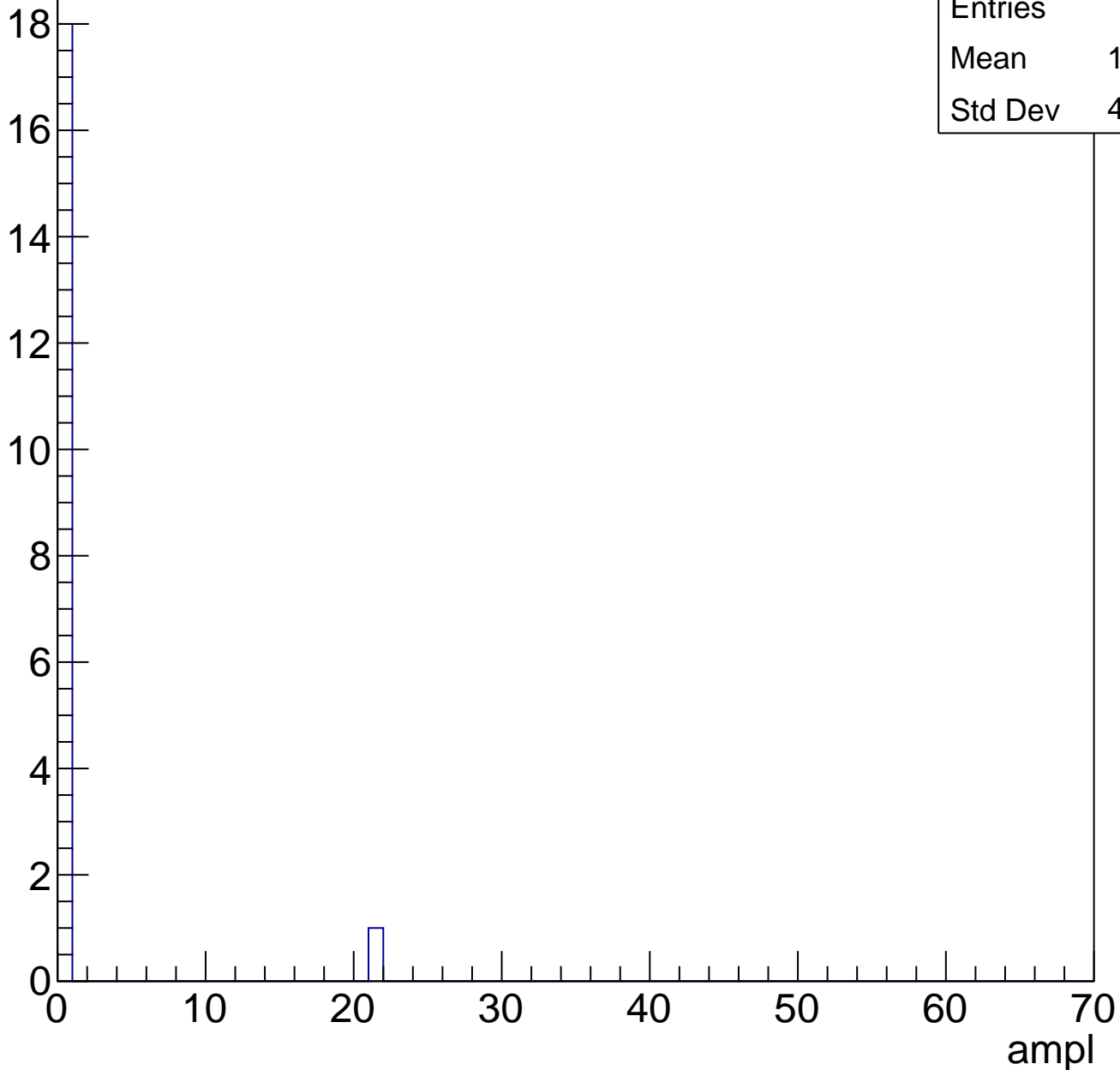


B1L103S, U11-ch17, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.105
Std Dev	4.689

Entry

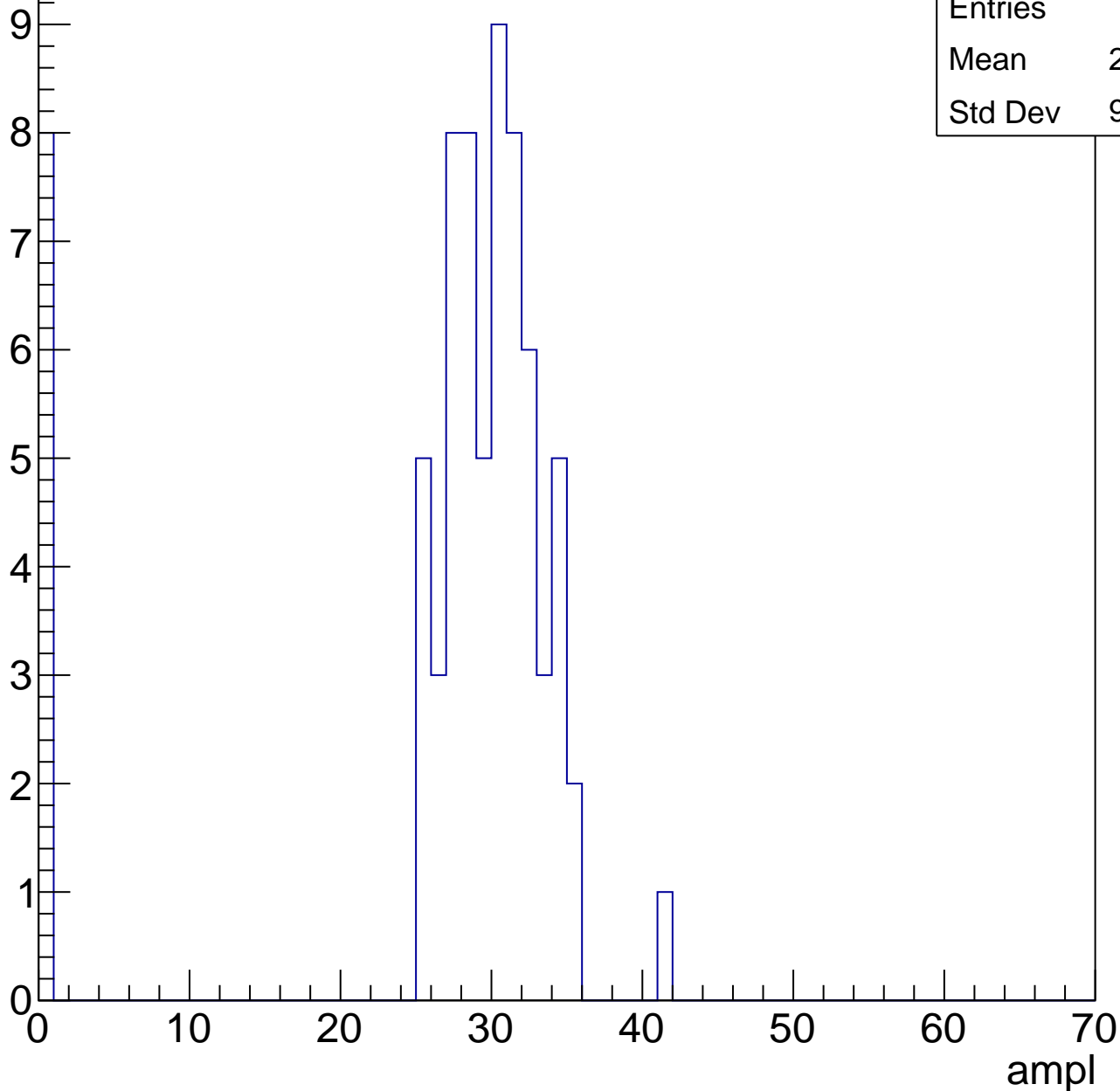


B1L103S, U11-ch18, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	26.45
Std Dev	9.856

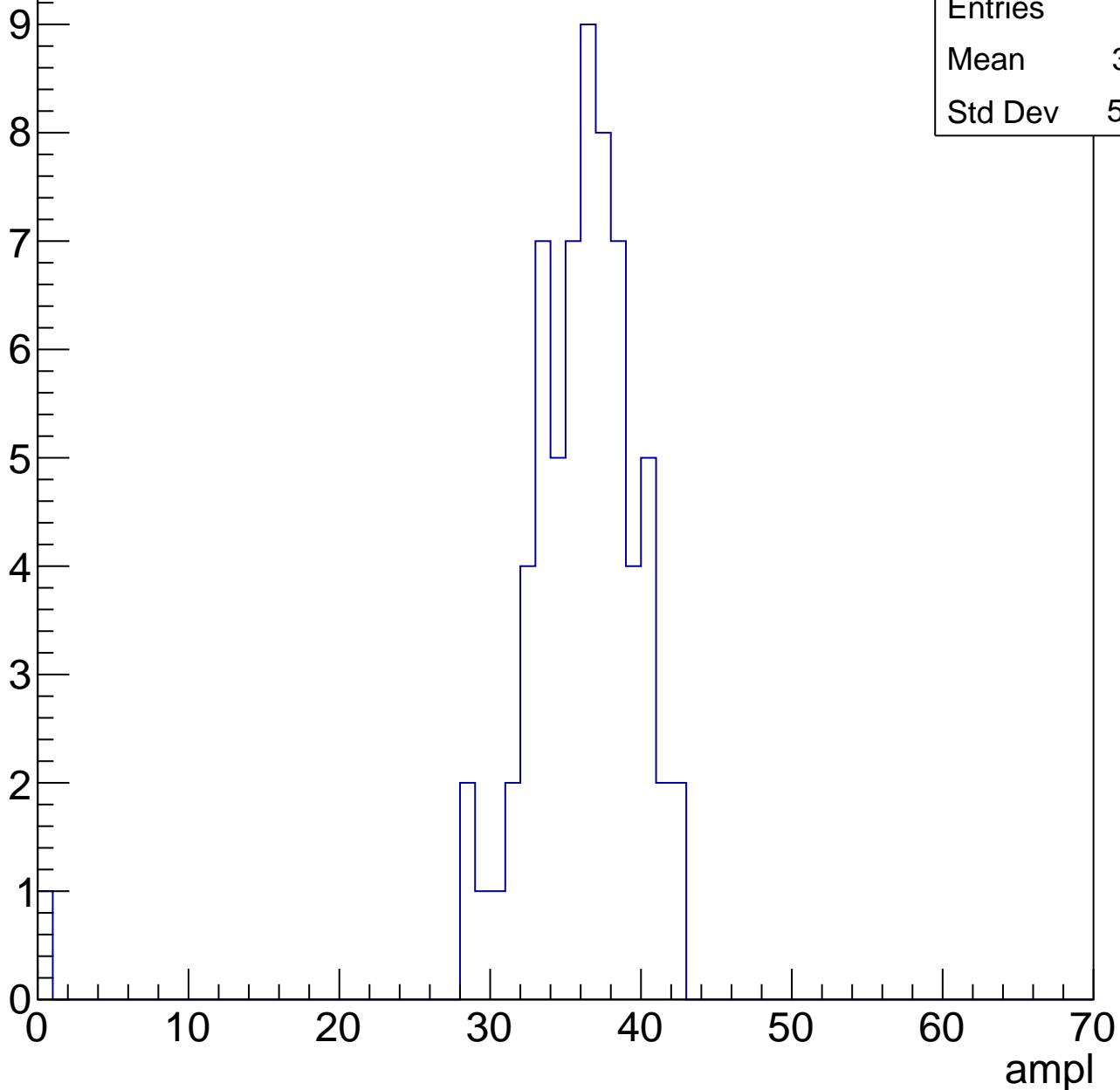


B1L103S, U11-ch18, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	35.21
Std Dev	5.388



B1L103S, U11-ch18, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

8

6

4

2

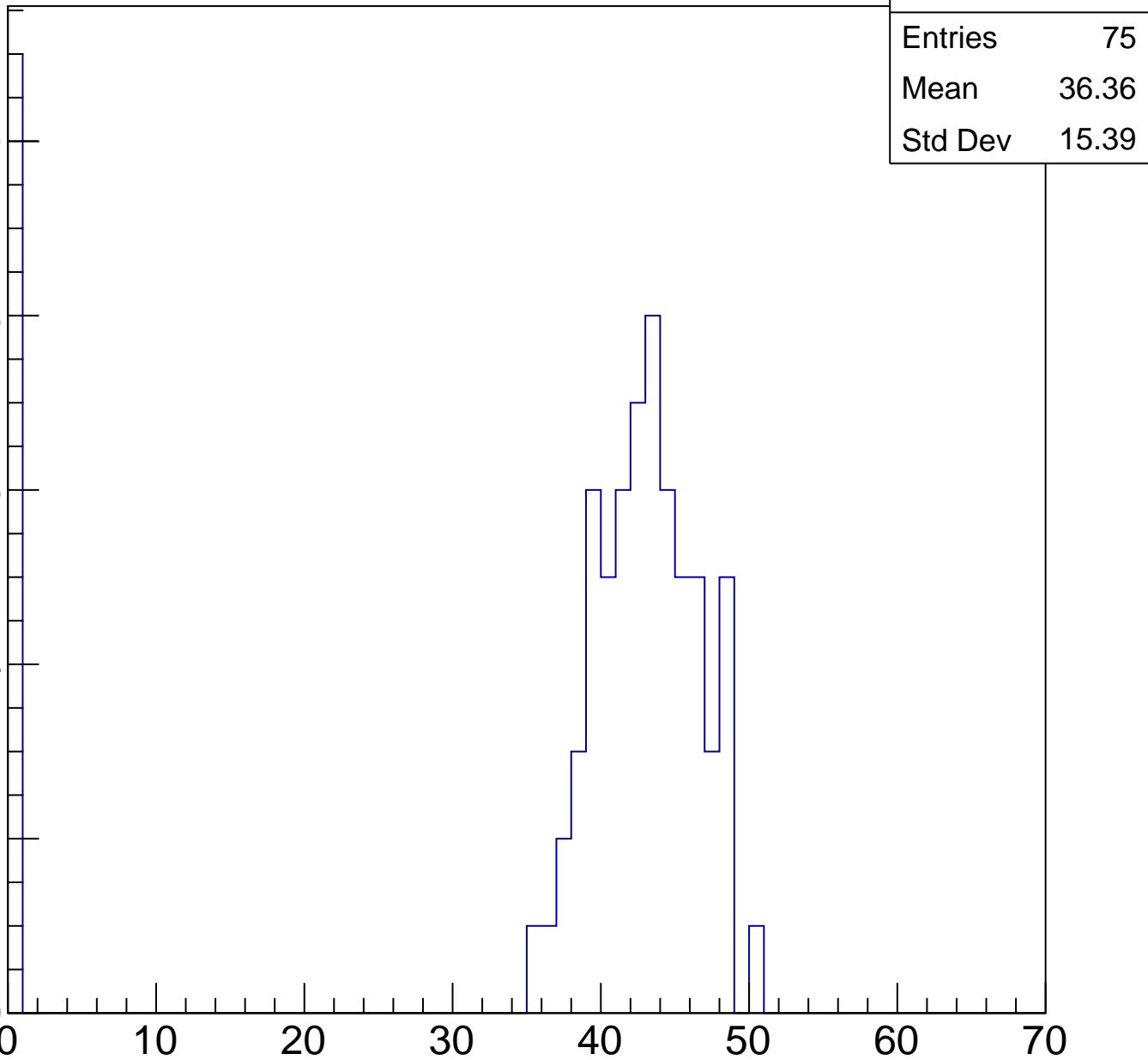
0

Entries 75

Mean 36.36

Std Dev 15.39

ampl

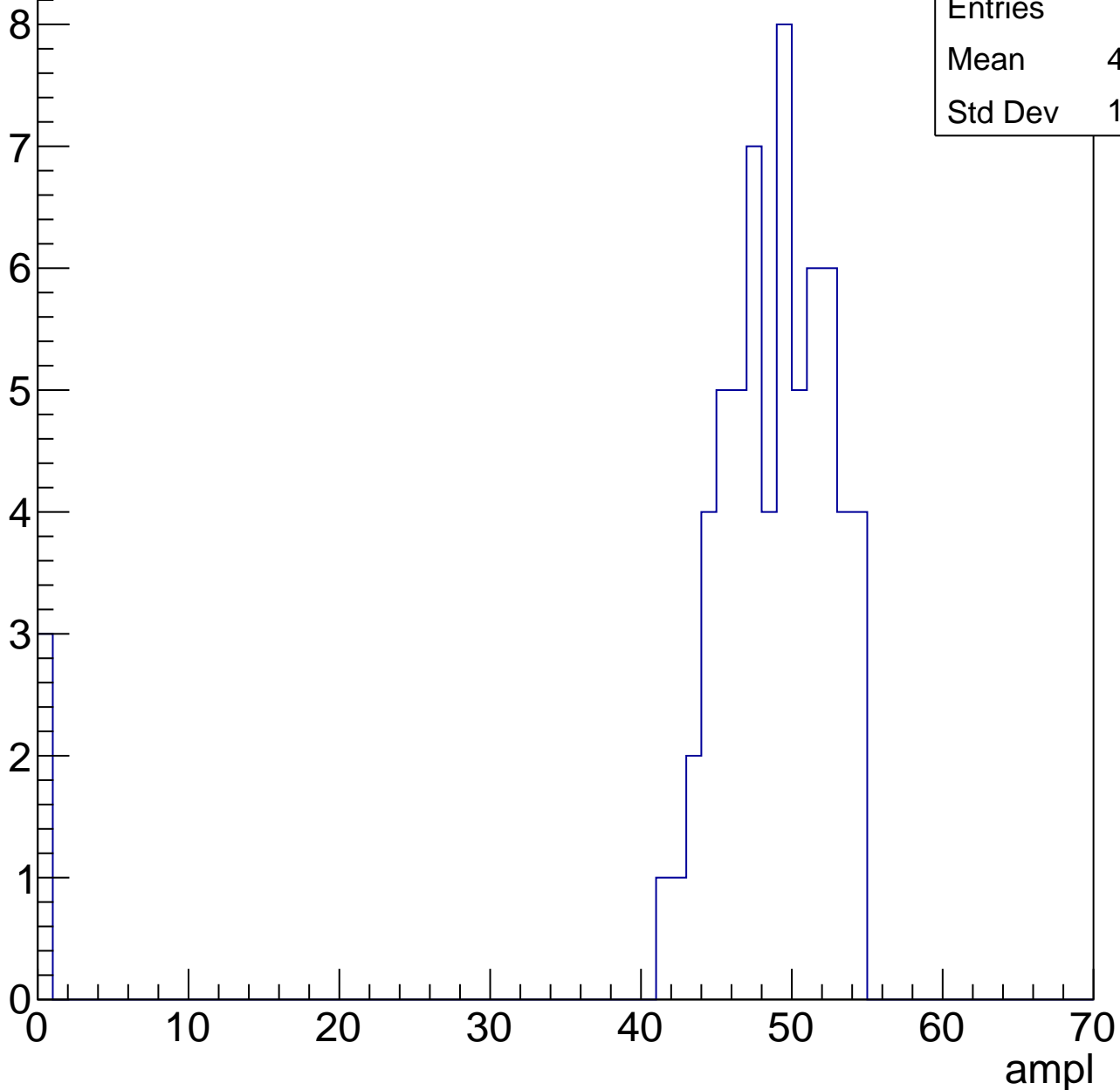


B1L103S, U11-ch18, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

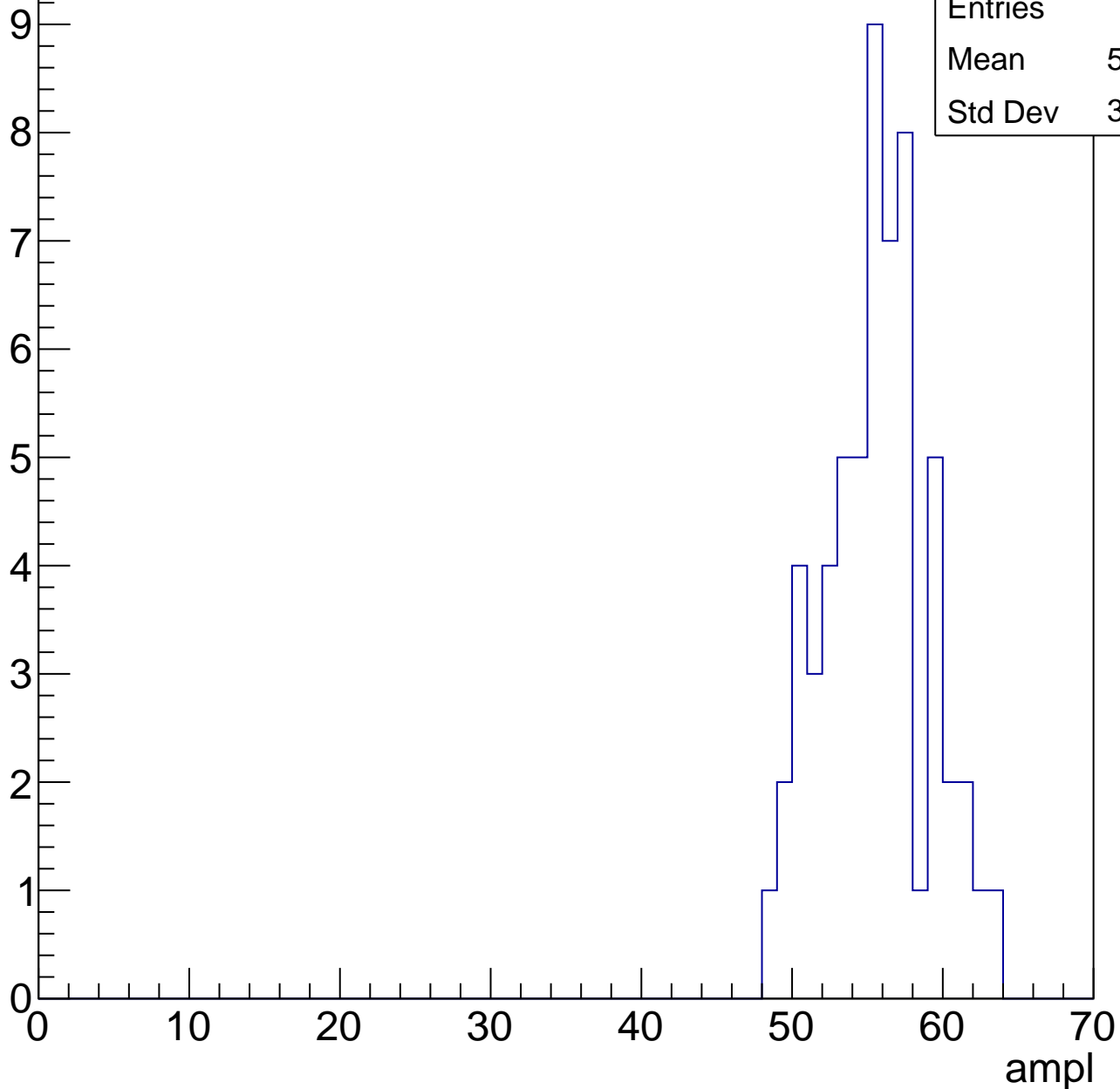
Entries	65
Mean	46.29
Std Dev	10.68



B1L103S, U11-ch18, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

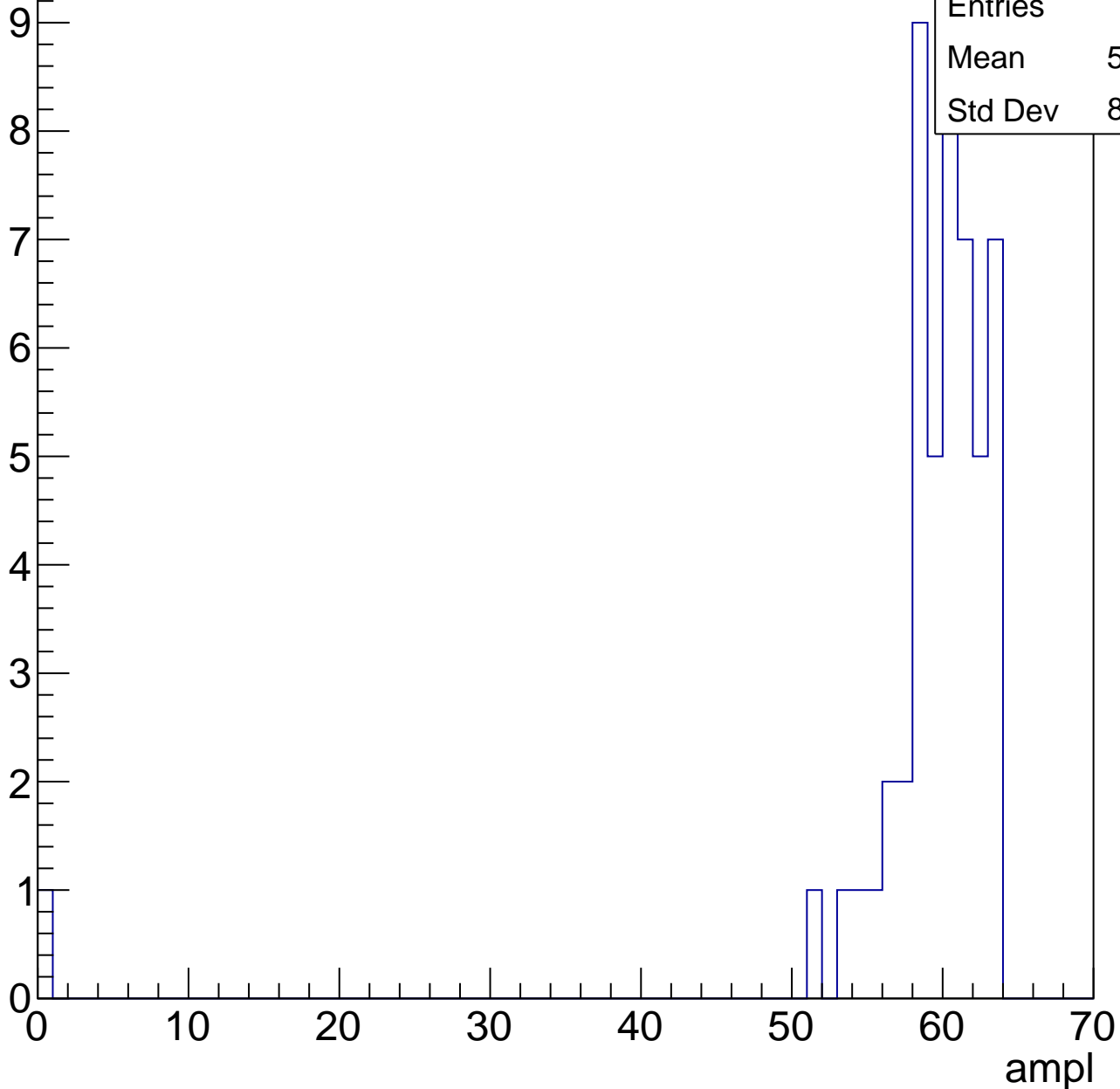


B1L103S, U11-ch18, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

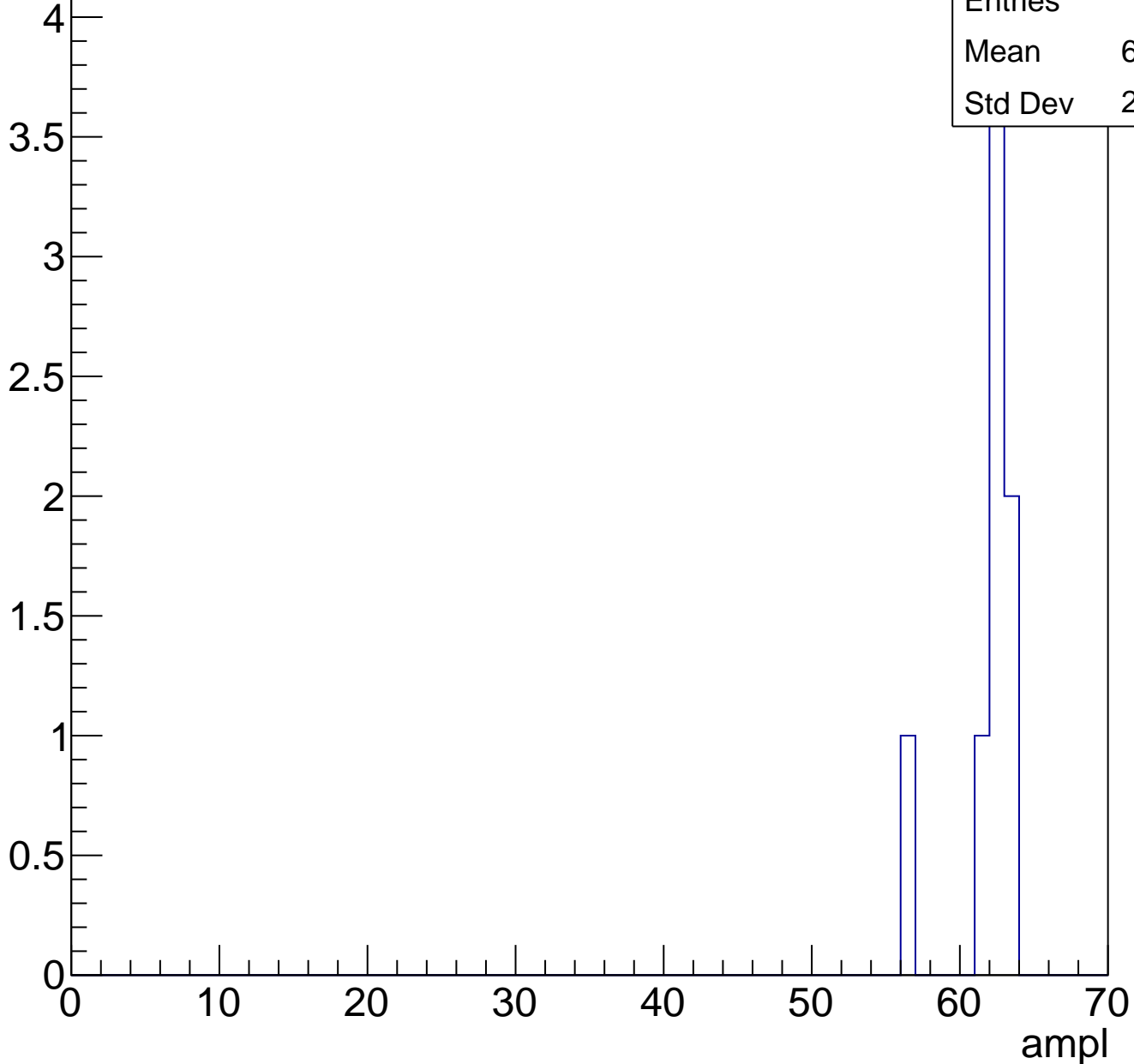
Entries	50
Mean	58.28
Std Dev	8.745



B1L103S, U11-ch18, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

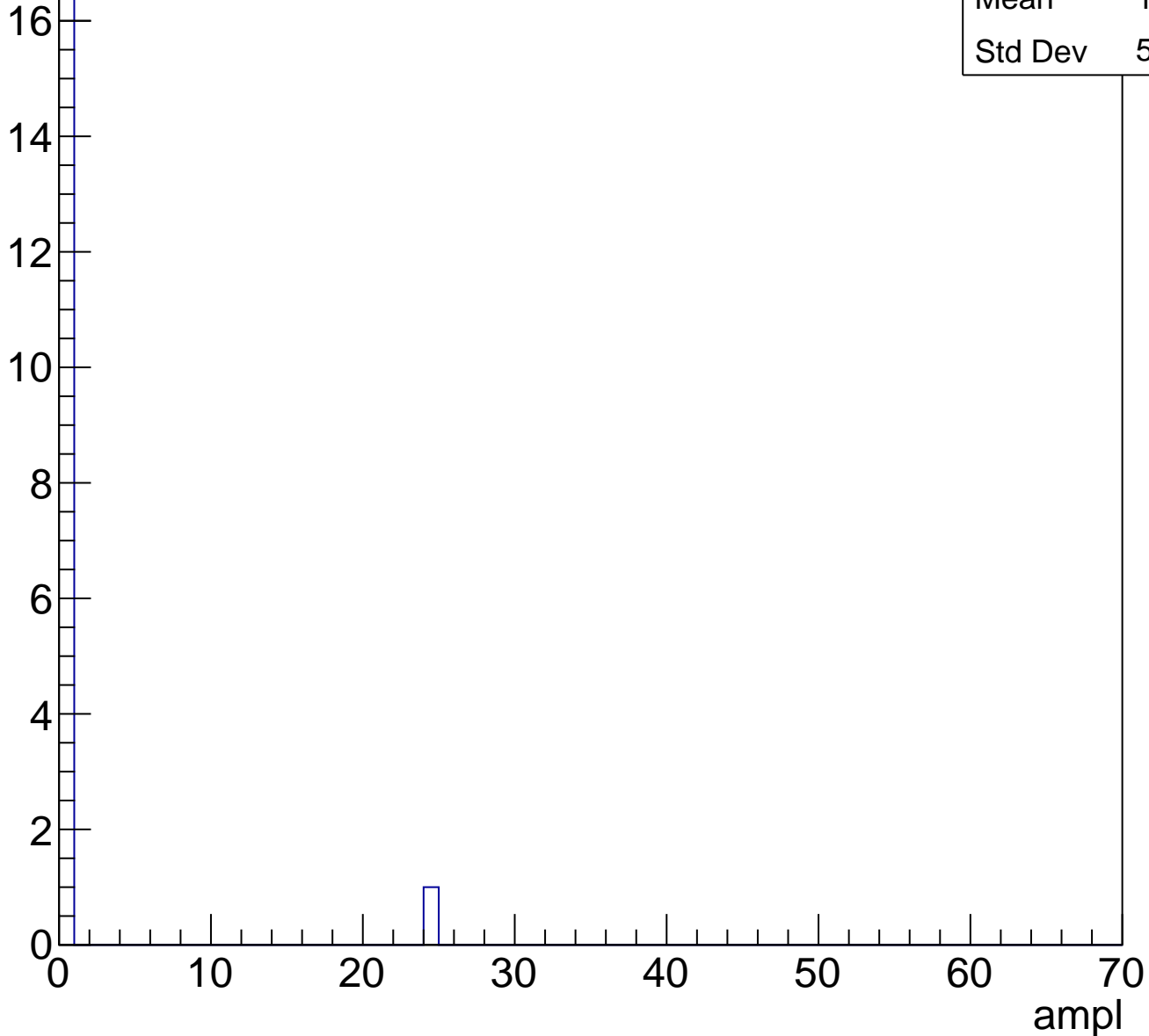


B1L103S, U11-ch18, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	18
Mean	1.333
Std Dev	5.497

Entry



B1L103S, U11-ch19, adc0

calib_packv5_041523_1651.root, FC#0, port C2

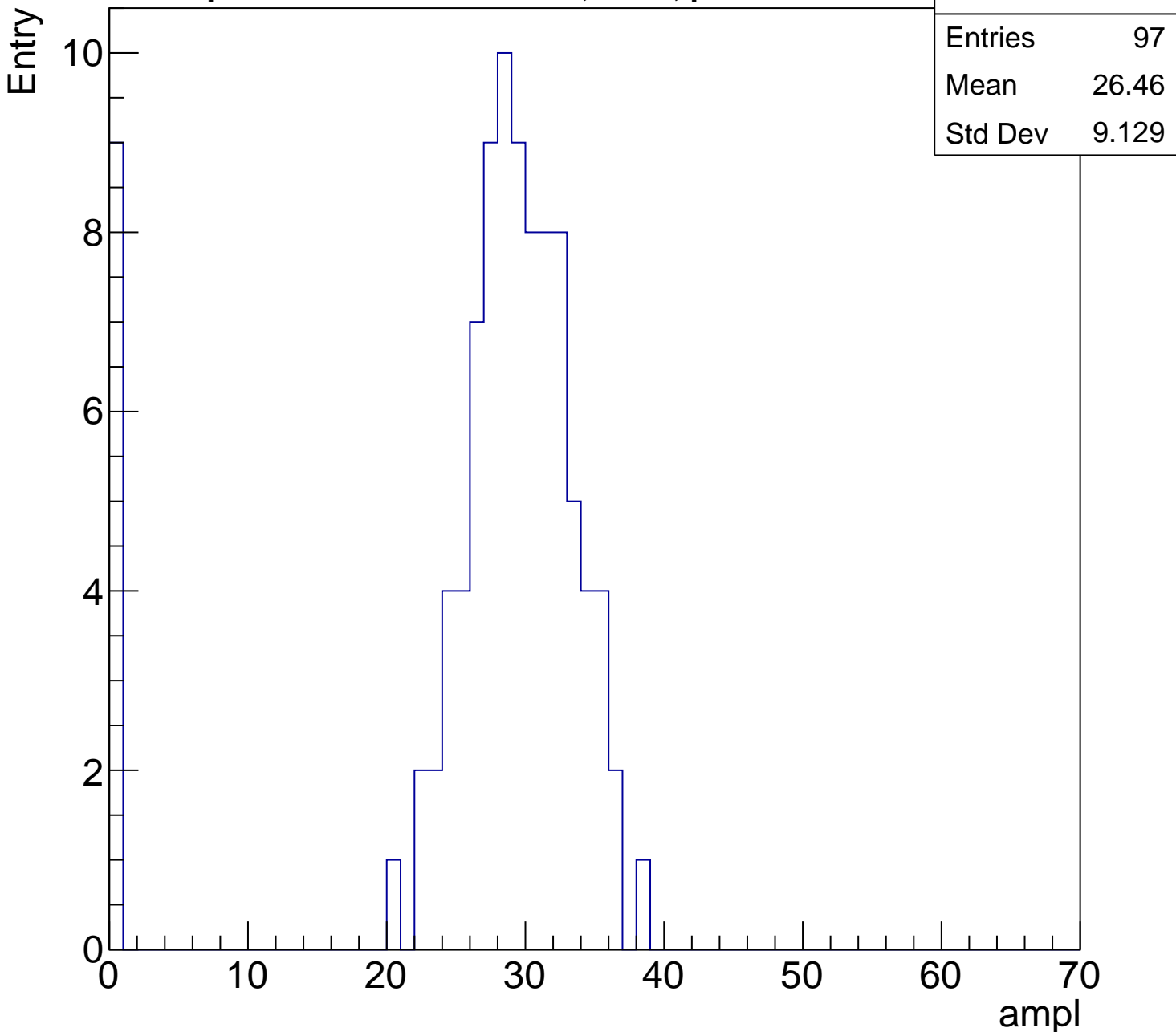
Entries	97
Mean	26.46
Std Dev	9.129

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

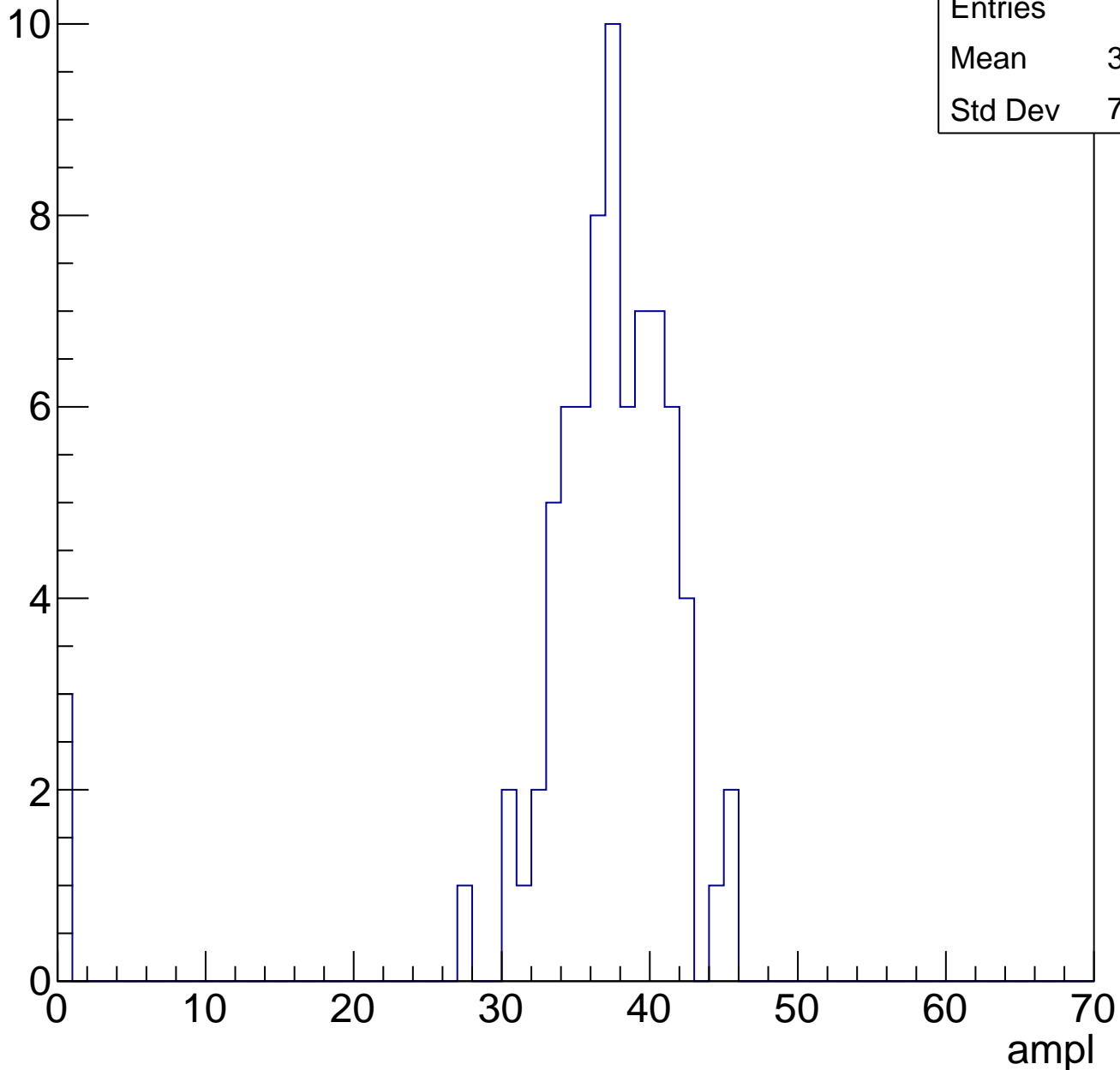


B1L103S, U11-ch19, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	77
Mean	35.69
Std Dev	7.973

Entry

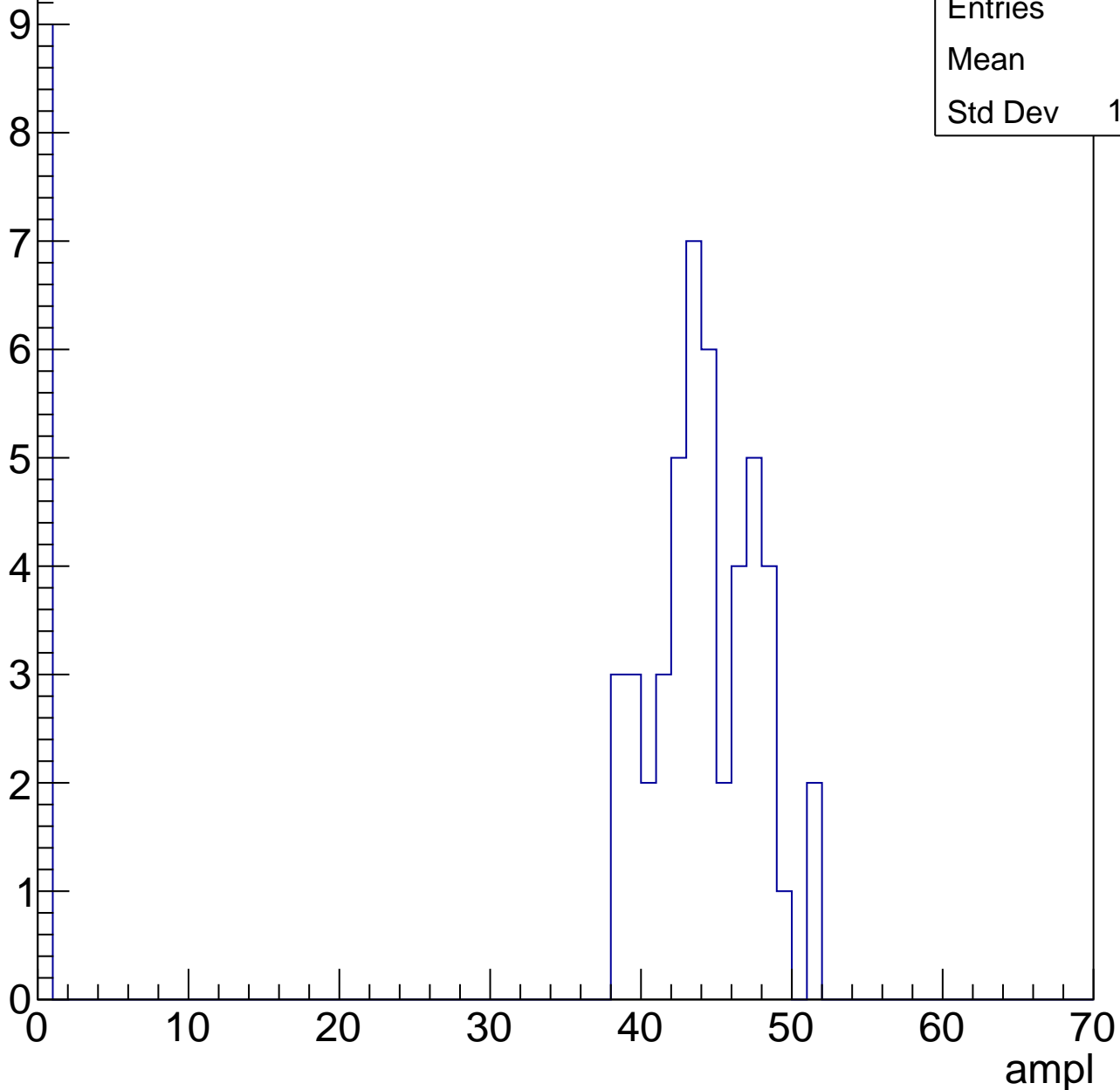


B1L103S, U11-ch19, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

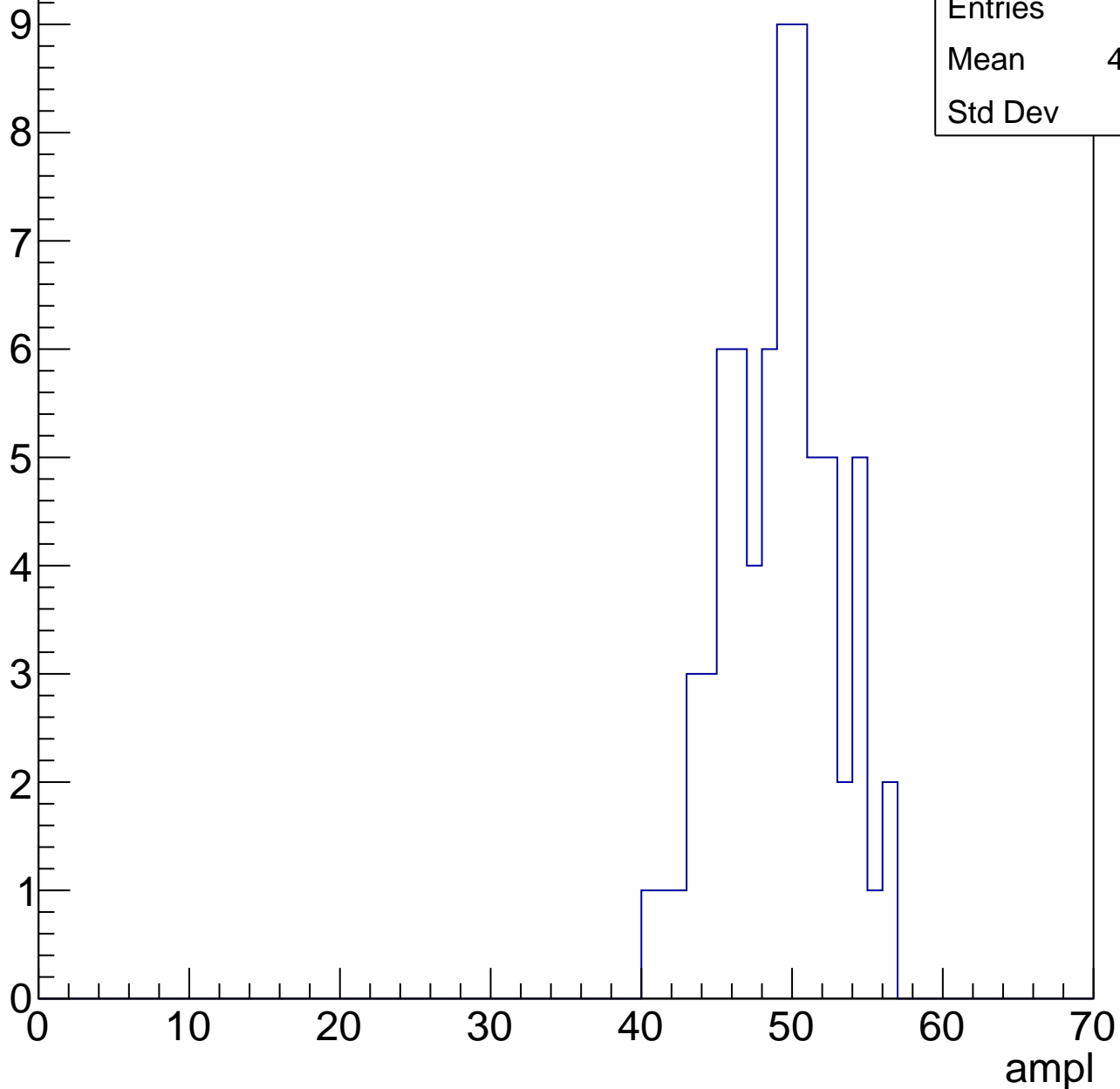
Entries	56
Mean	36.8
Std Dev	16.39



B1L103S, U11-ch19, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

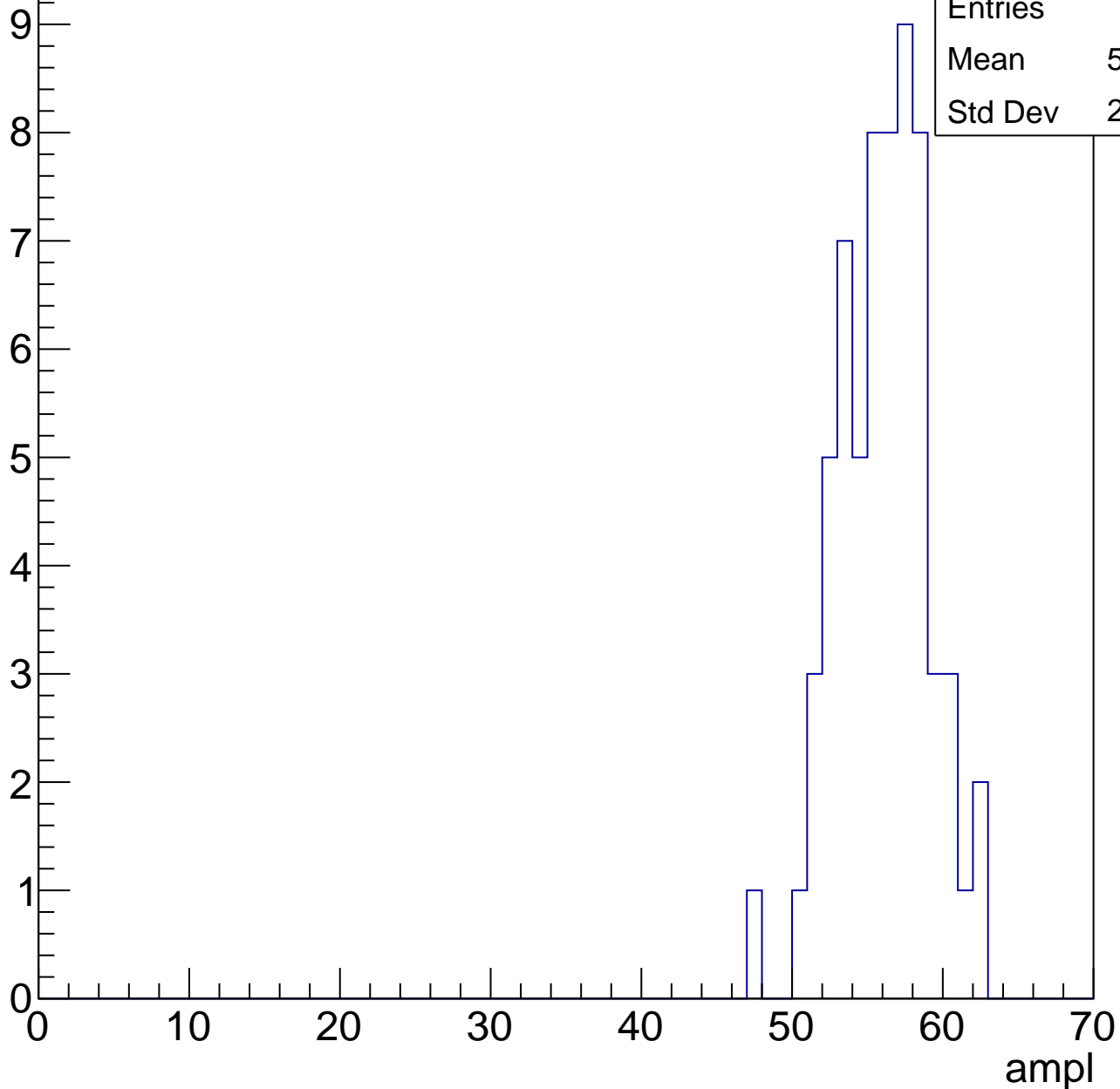


Entries	69
Mean	48.62
Std Dev	3.62

B1L103S, U11-ch19, adc4

calib_packv5_041523_1651.root, FC#0, port C2

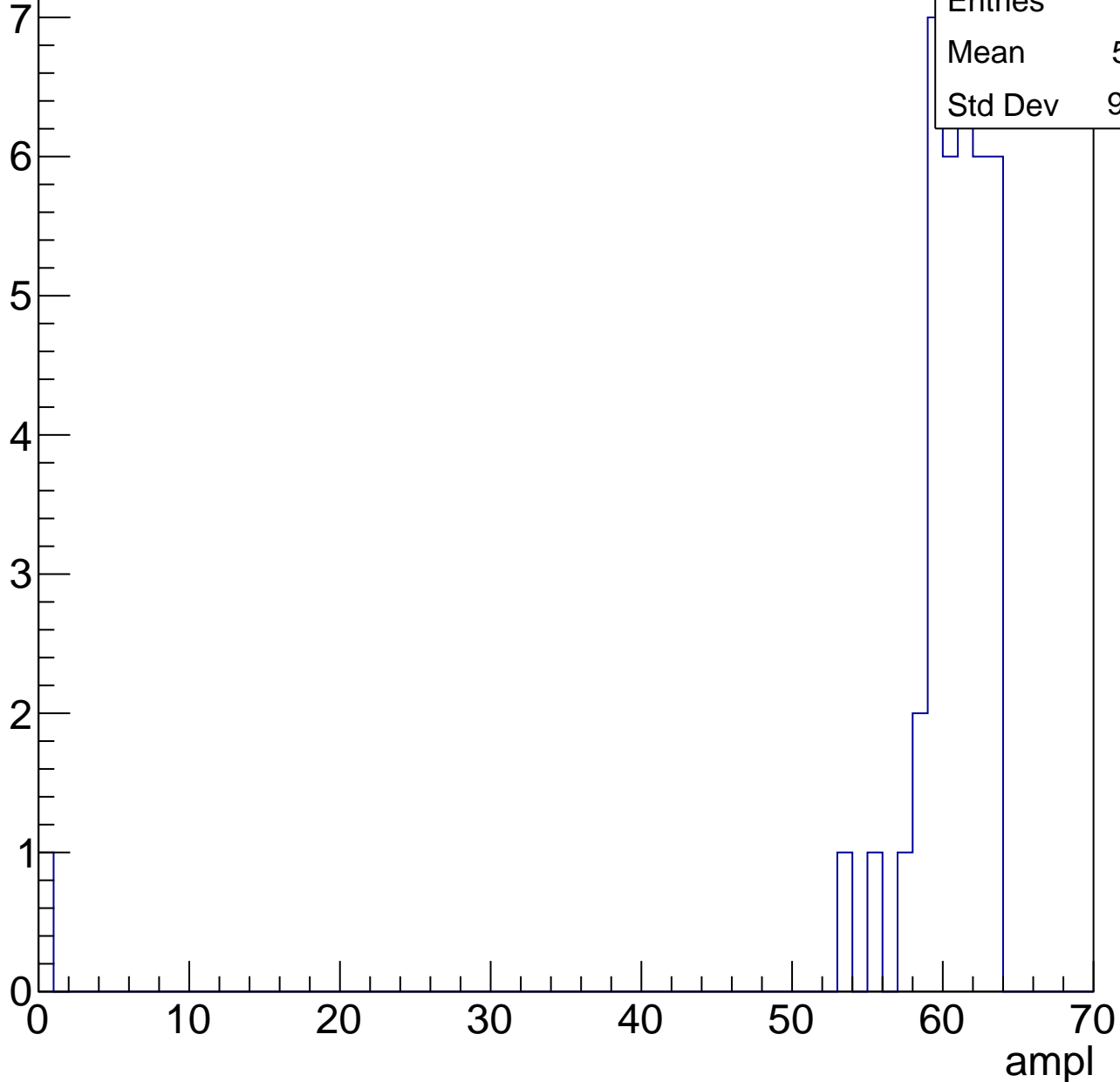
Entry



B1L103S, U11-ch19, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch19, adc6

calib_packv5_041523_1651.root, FC#0, port C2

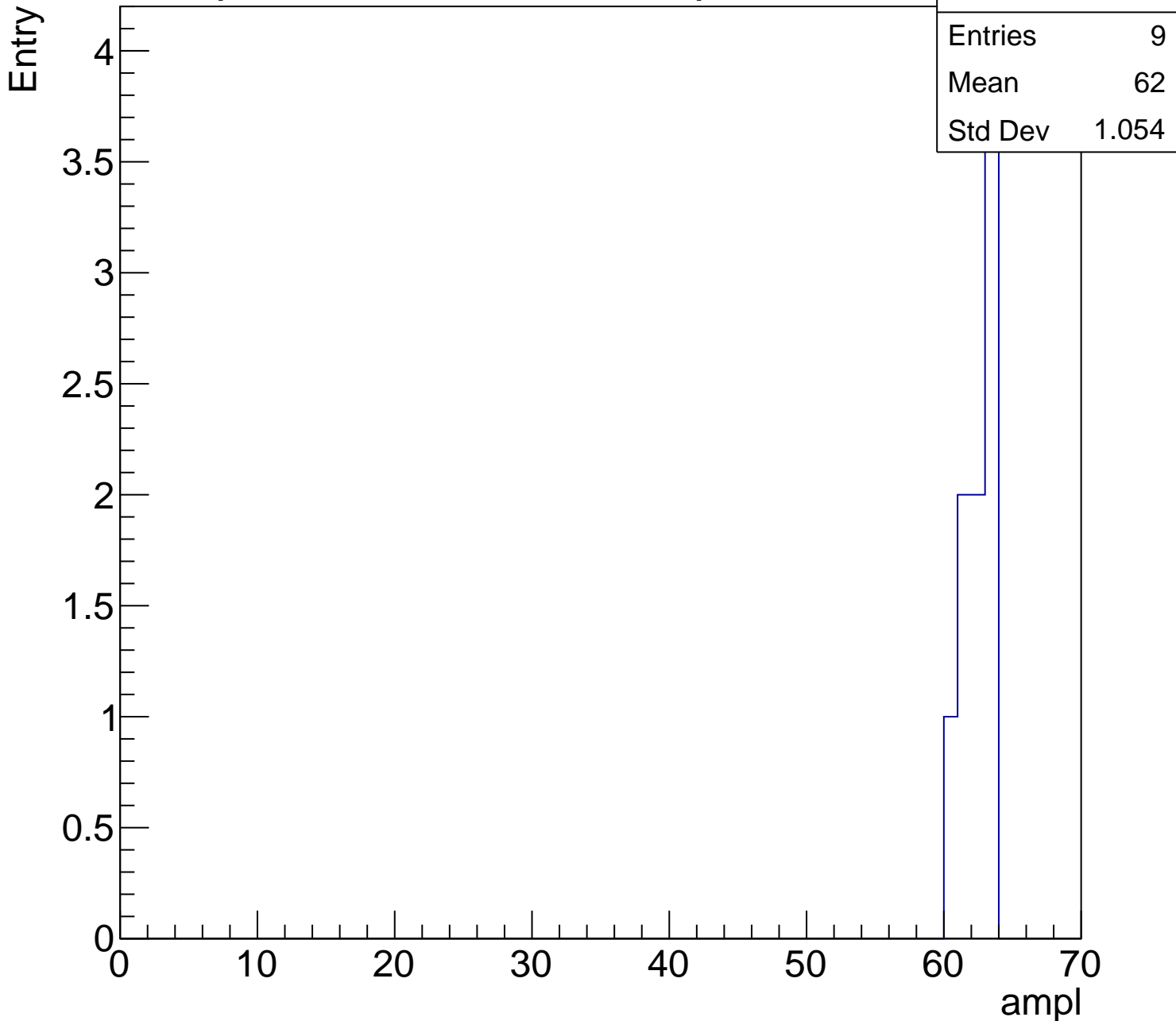
Entry

4
3.5
3
2.5
2
1.5
1
0.5
0

Entries	9
Mean	62
Std Dev	1.054

ampl

0 10 20 30 40 50 60 70



B1L103S, U11-ch19, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

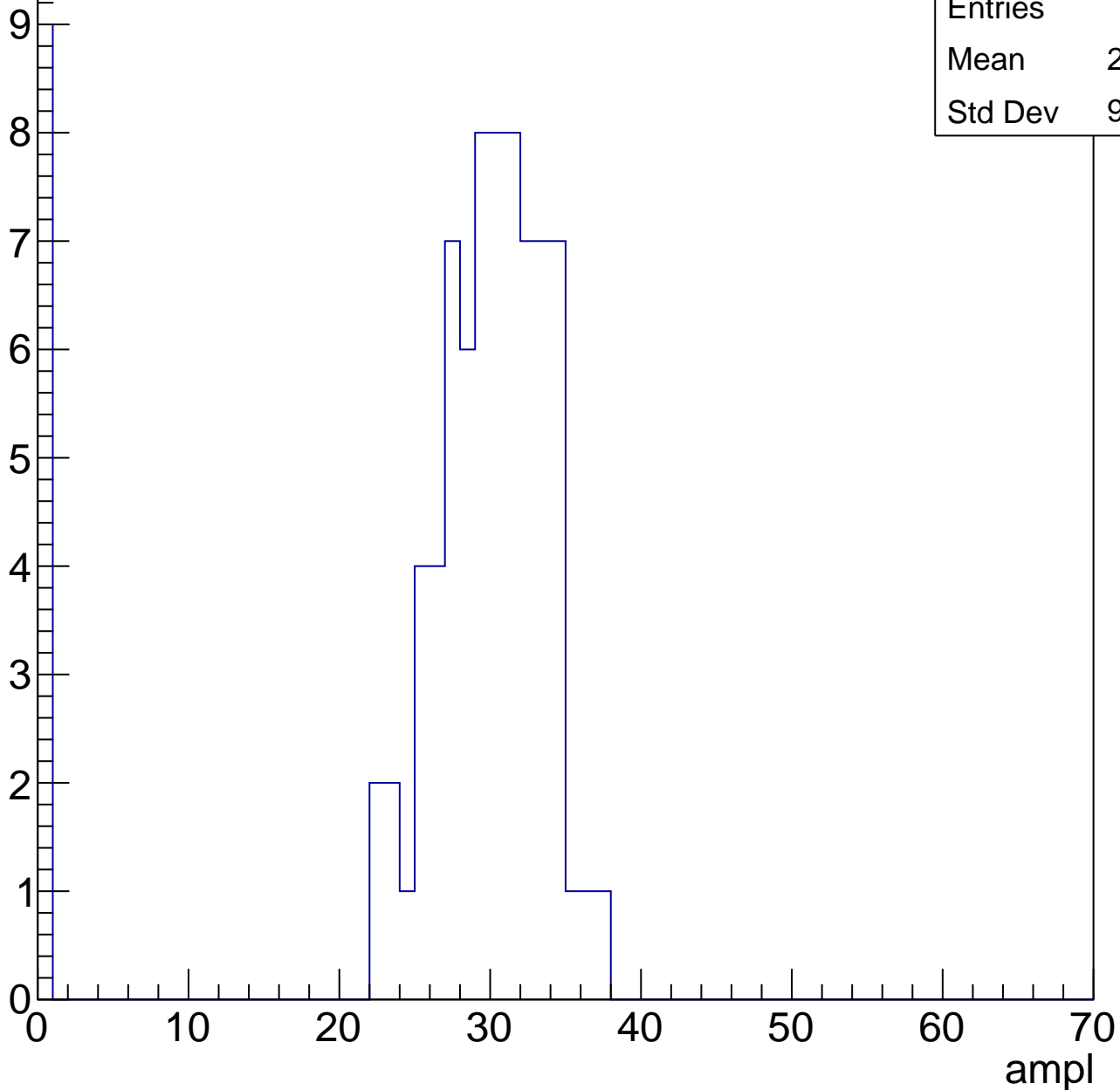


B1L103S, U11-ch20, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	83
Mean	26.46
Std Dev	9.756

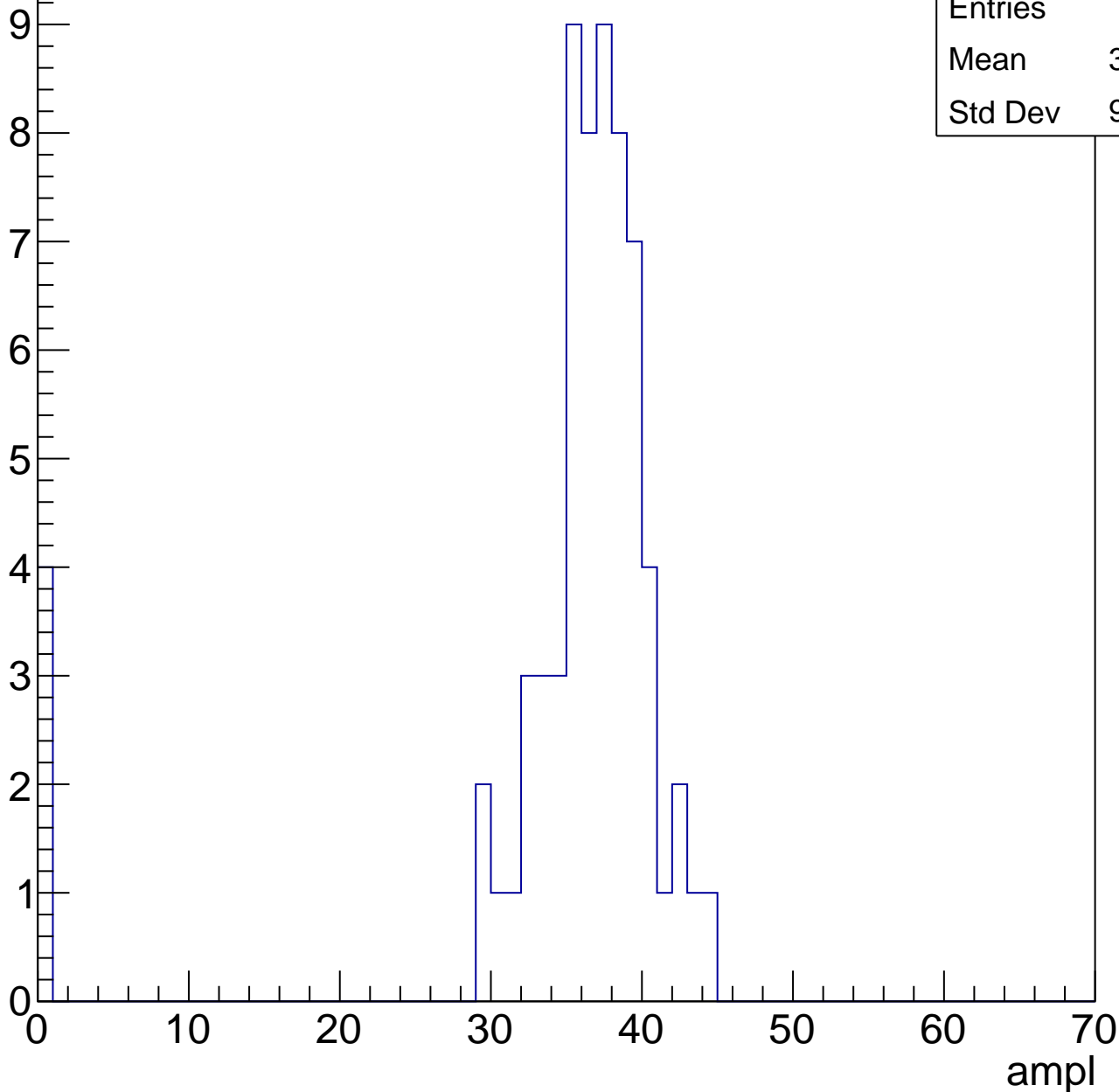


B1L103S, U11-ch20, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	34.34
Std Dev	9.169

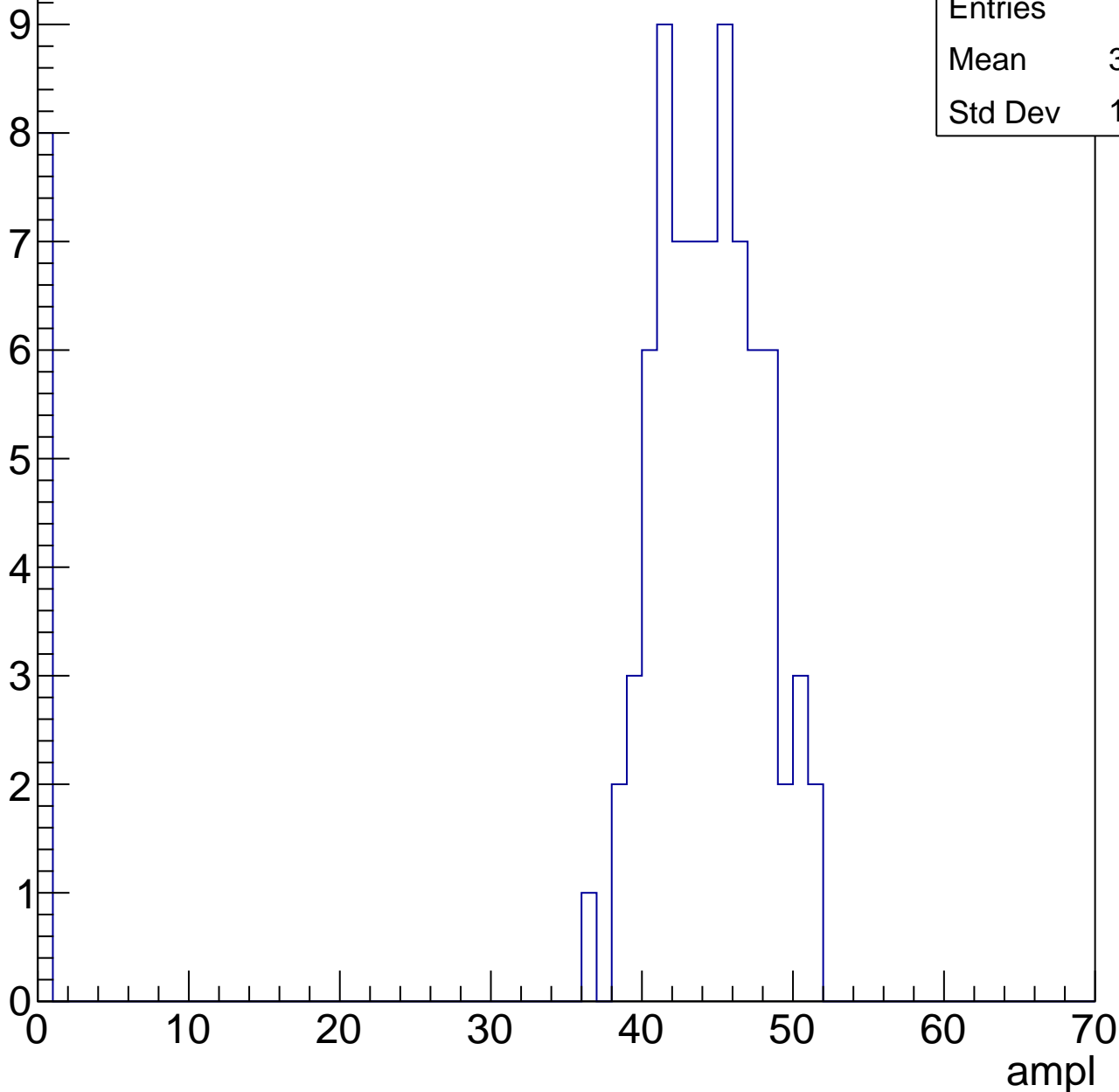


B1L103S, U11-ch20, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	85
Mean	39.86
Std Dev	13.24

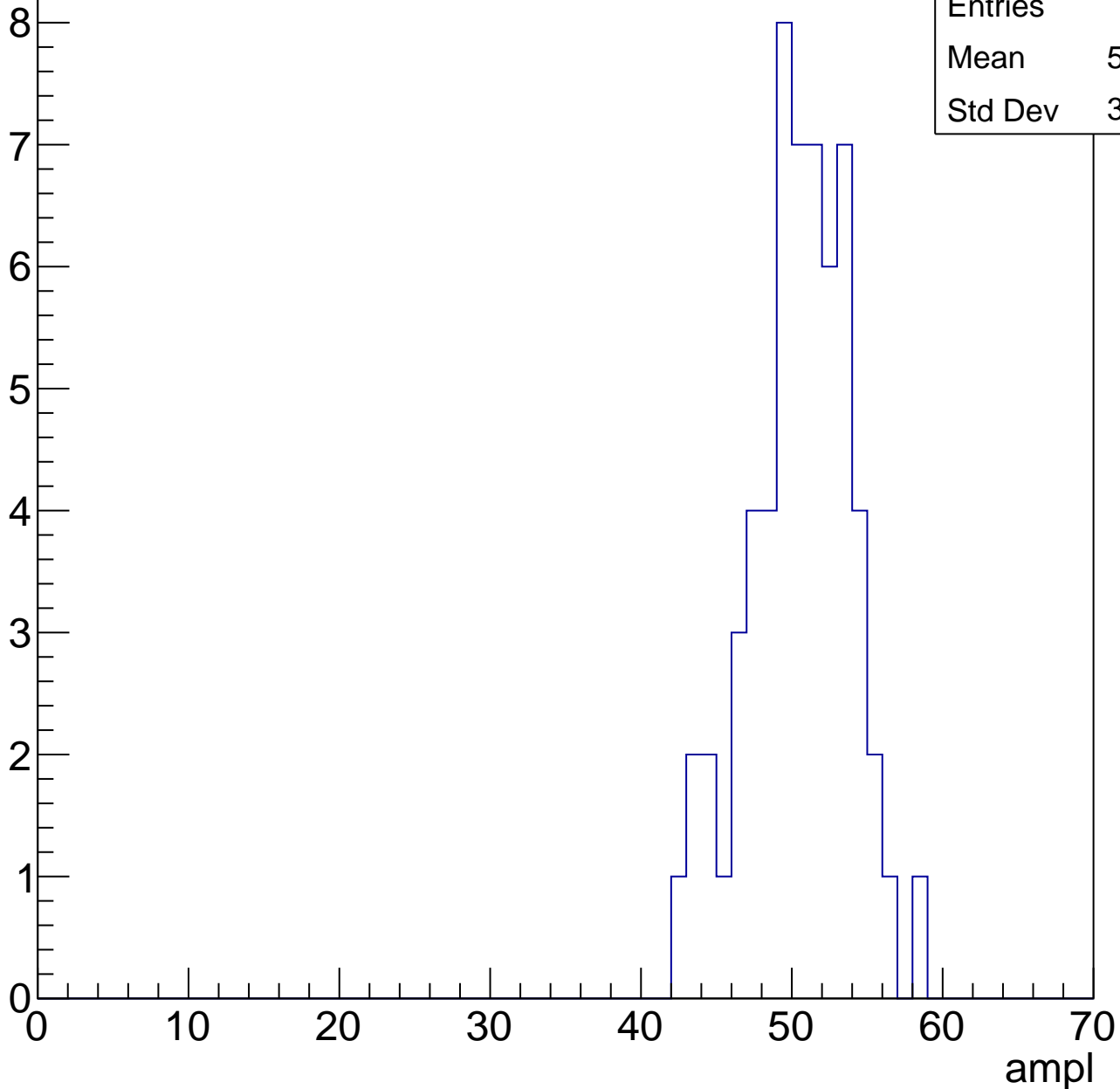


B1L103S, U11-ch20, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

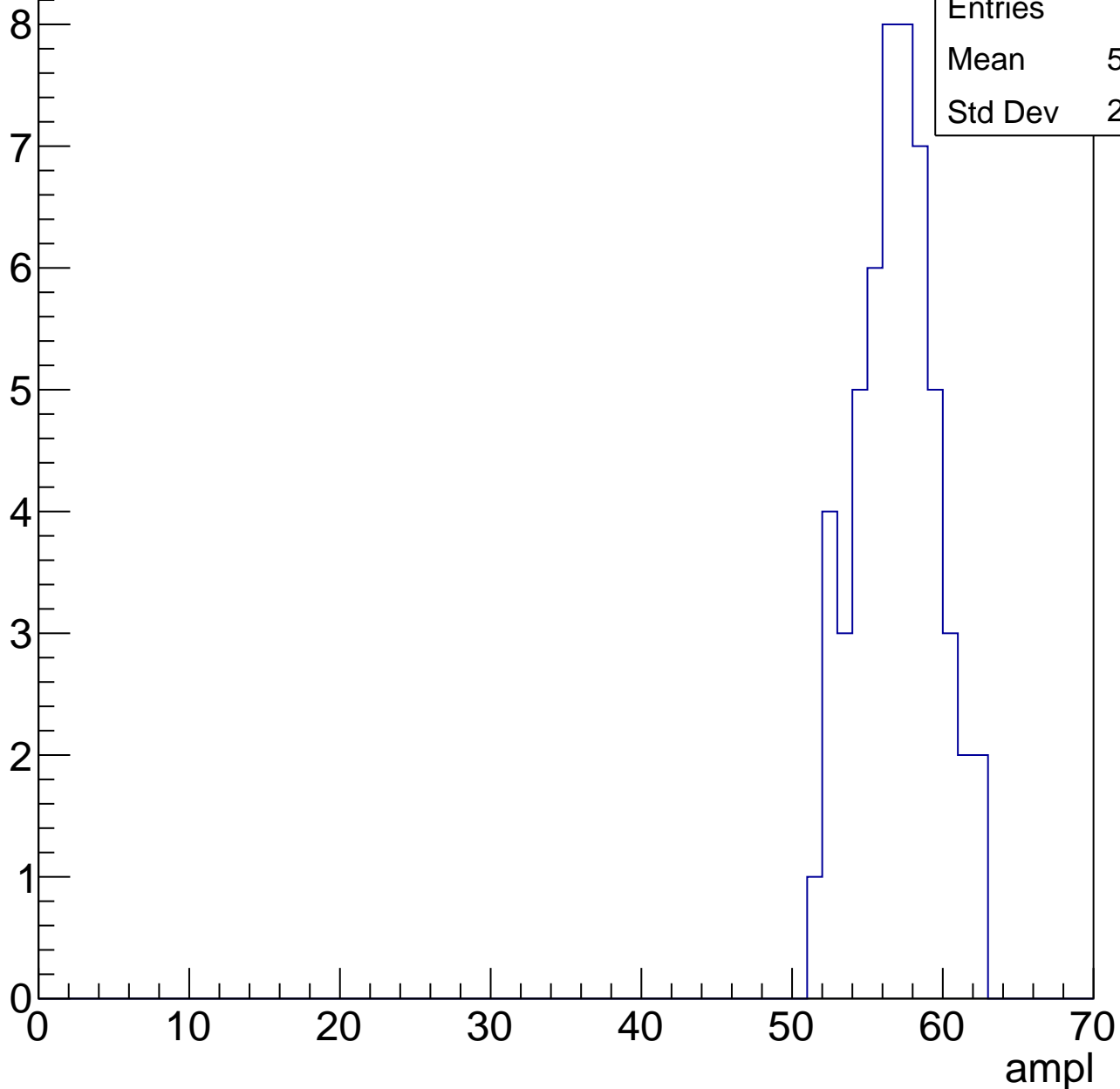
Entries	60
Mean	50.02
Std Dev	3.354



B1L103S, U11-ch20, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



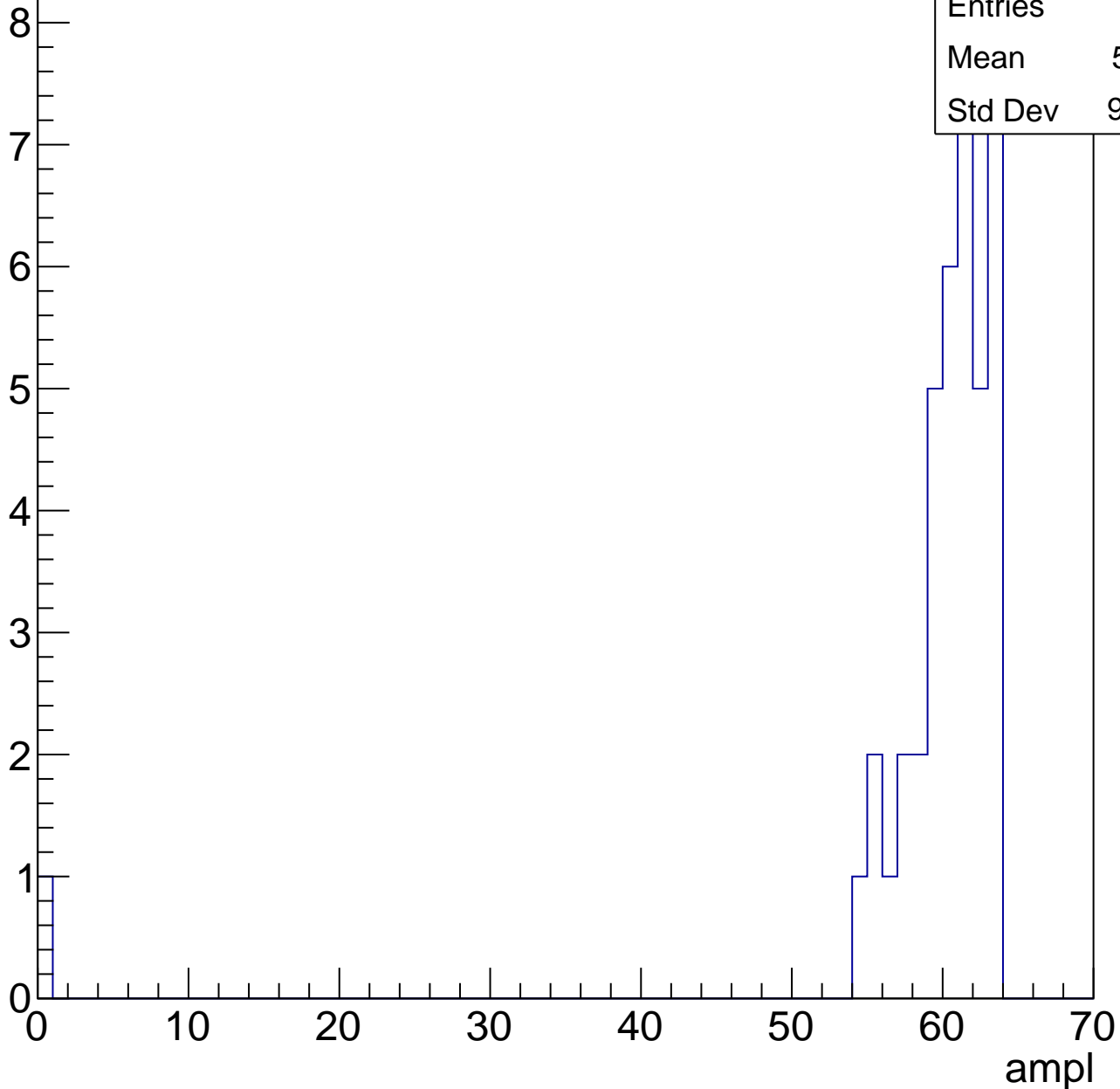
Entries	54
Mean	56.46
Std Dev	2.658

B1L103S, U11-ch20, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

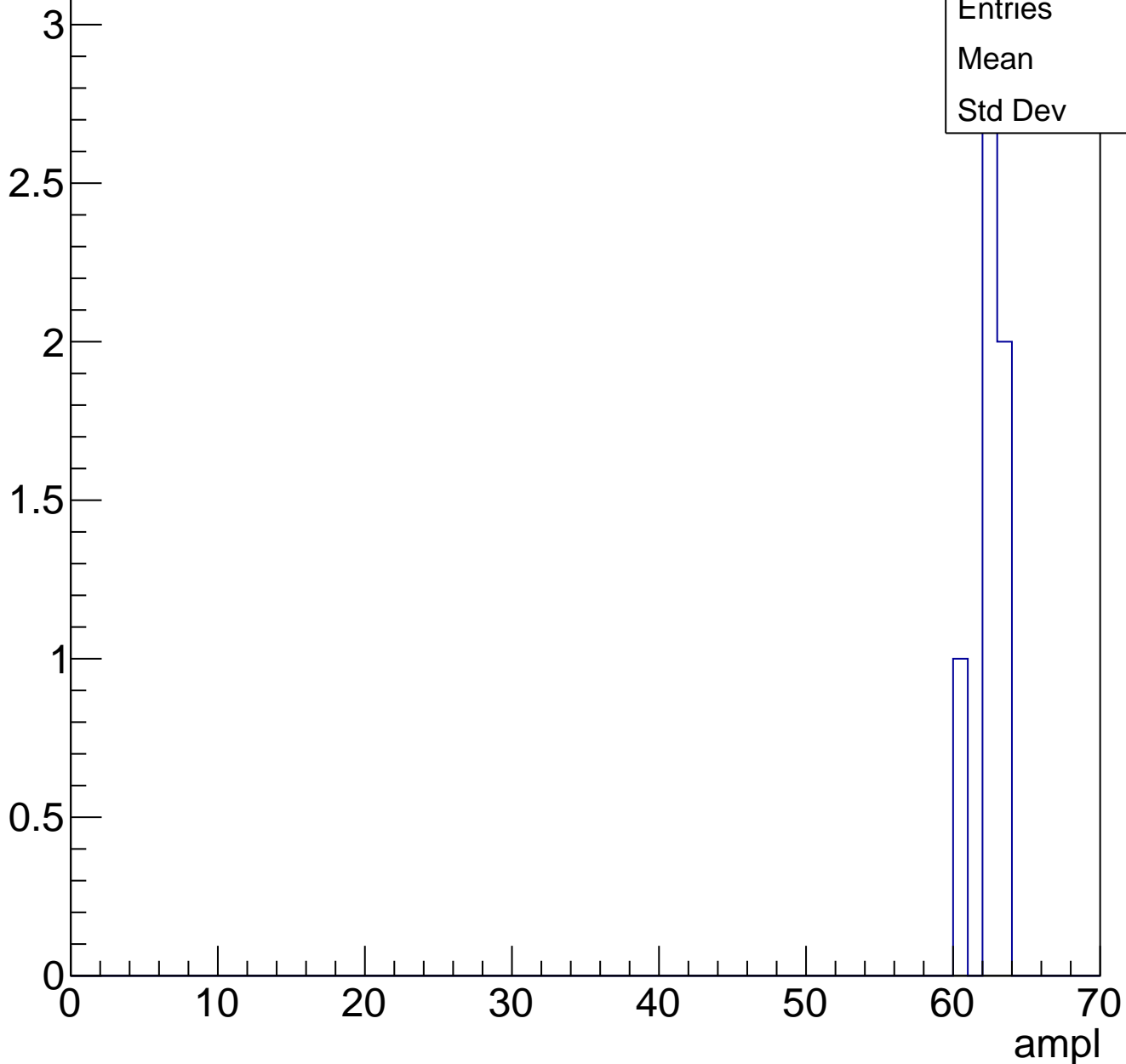
Entries	41
Mean	58.71
Std Dev	9.582



B1L103S, U11-ch20, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch20, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U11-ch21, adc0

calib_packv5_041523_1651.root, FC#0, port C2

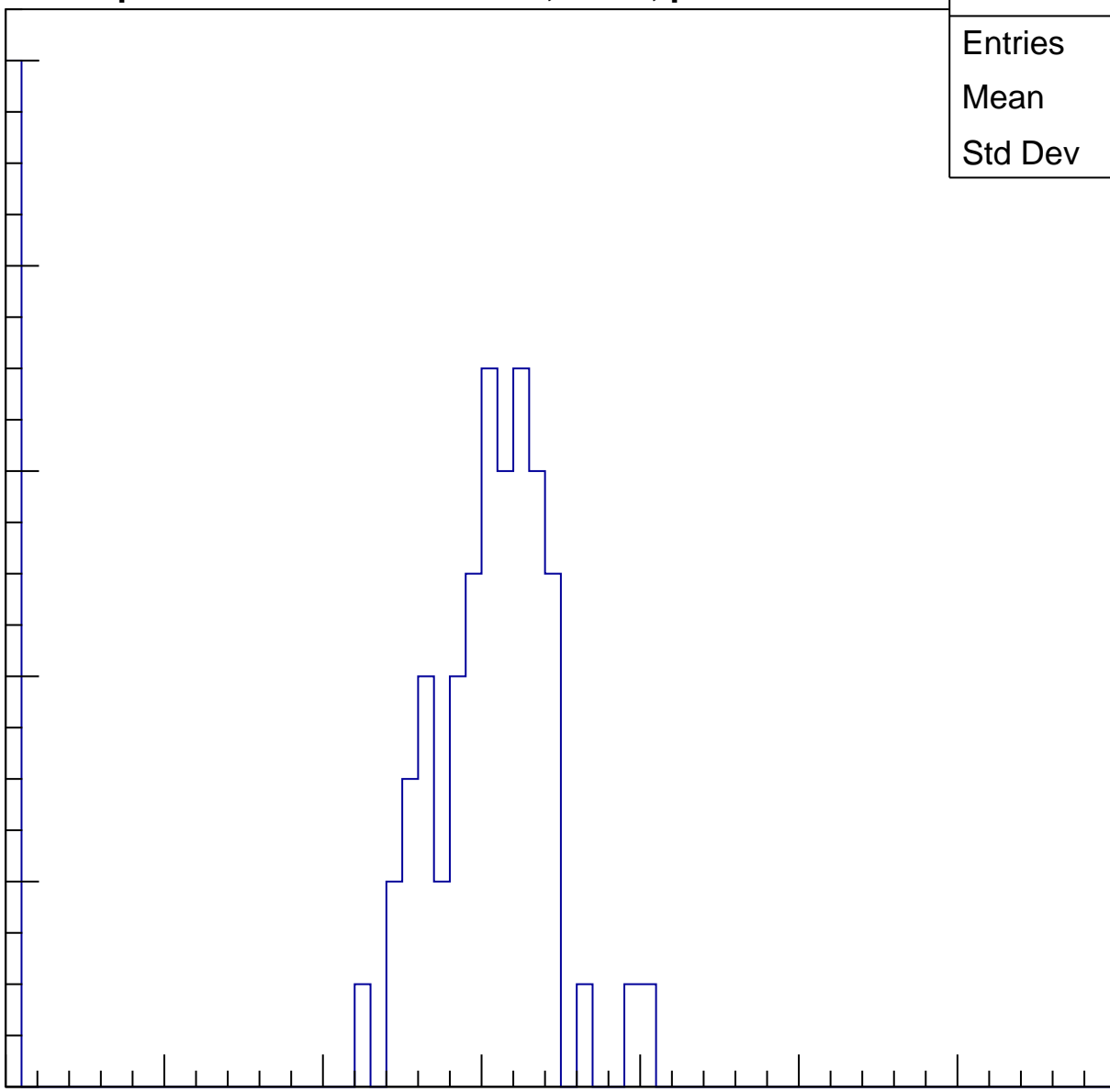
Entries	65
Mean	25.58
Std Dev	11.39

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

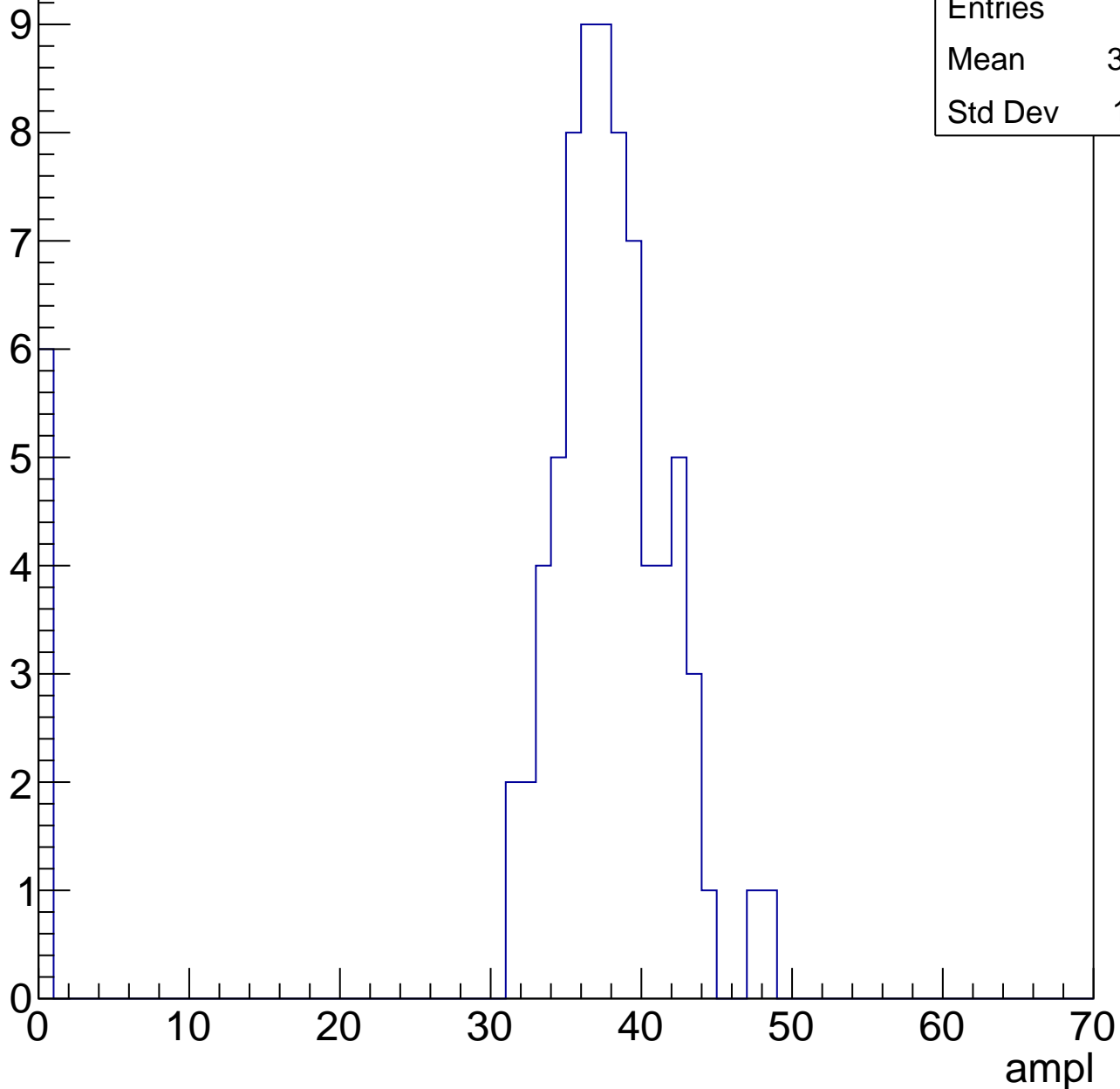


B1L103S, U11-ch21, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	79
Mean	34.73
Std Dev	10.51

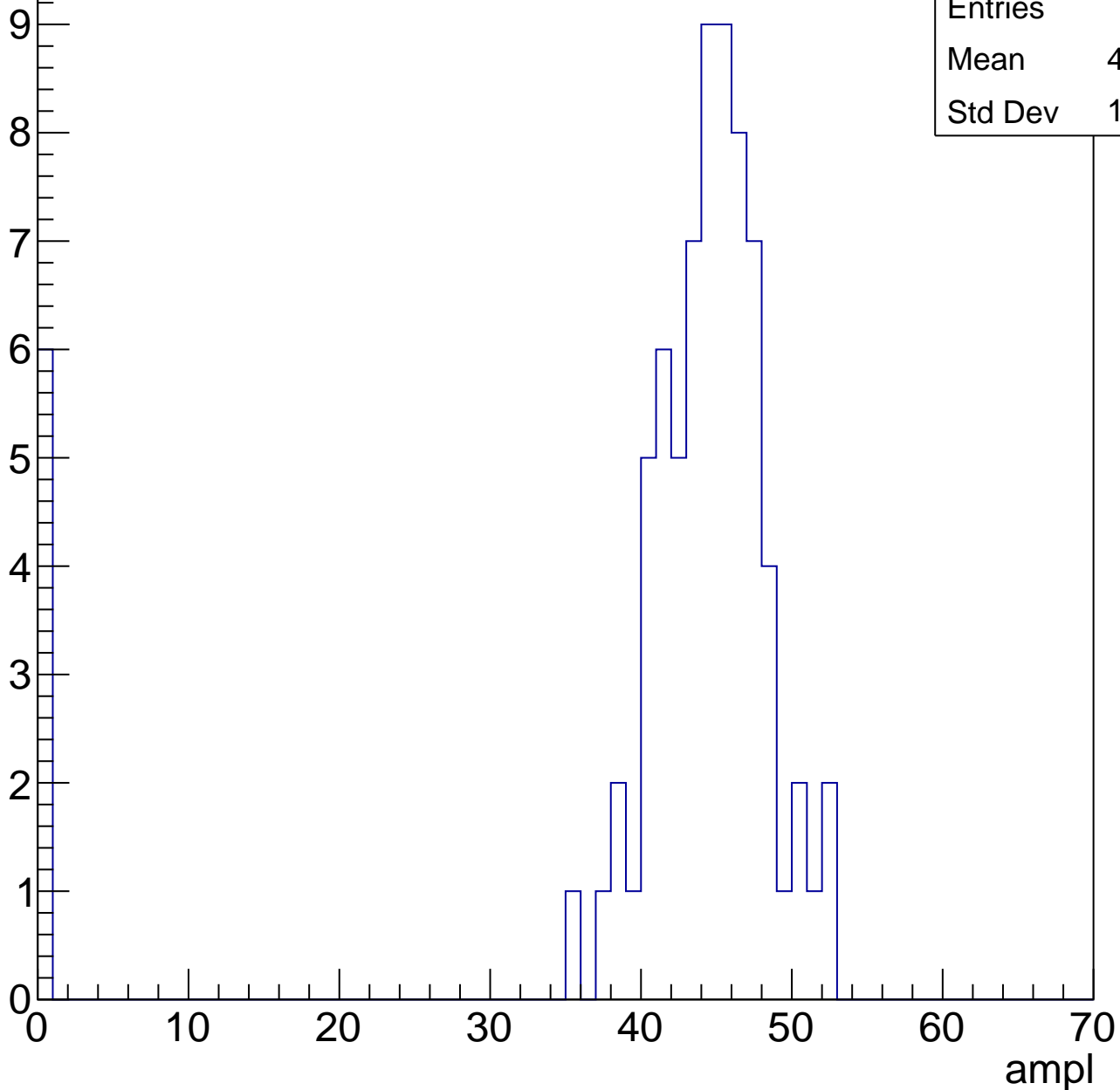


B1L103S, U11-ch21, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

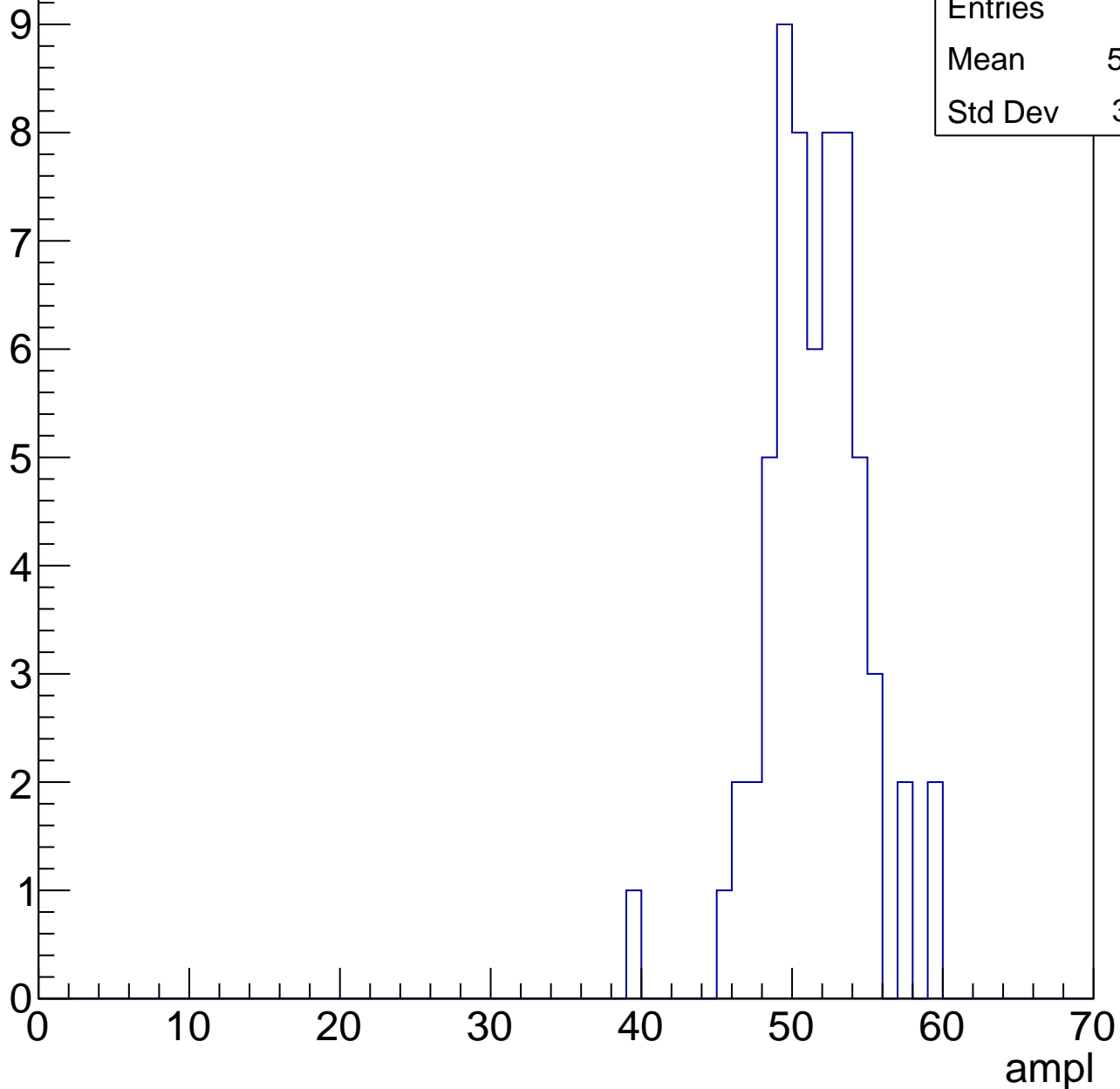
Entries	77
Mean	40.75
Std Dev	12.29



B1L103S, U11-ch21, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

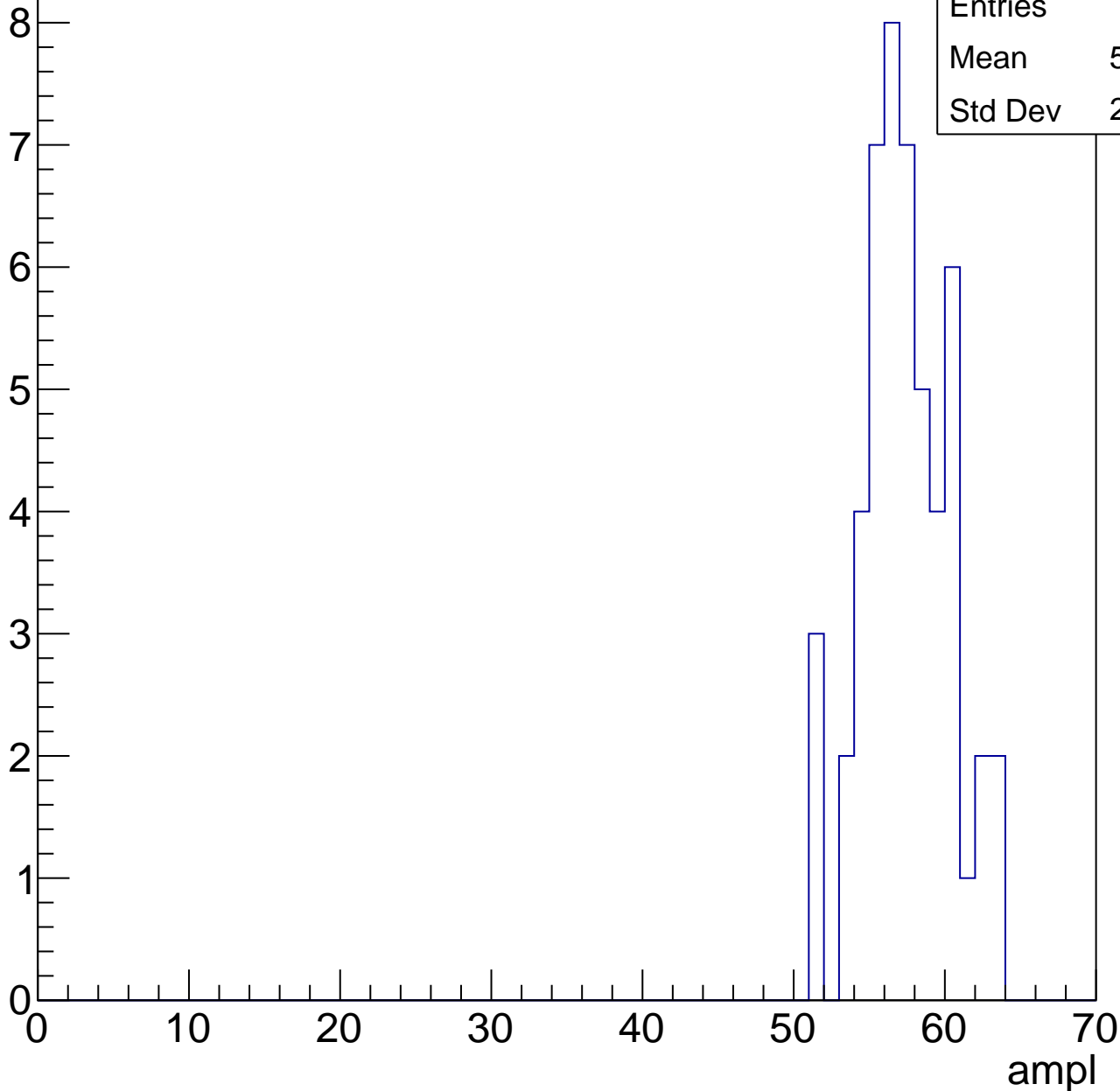


B1L103S, U11-ch21, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	56.94
Std Dev	2.886

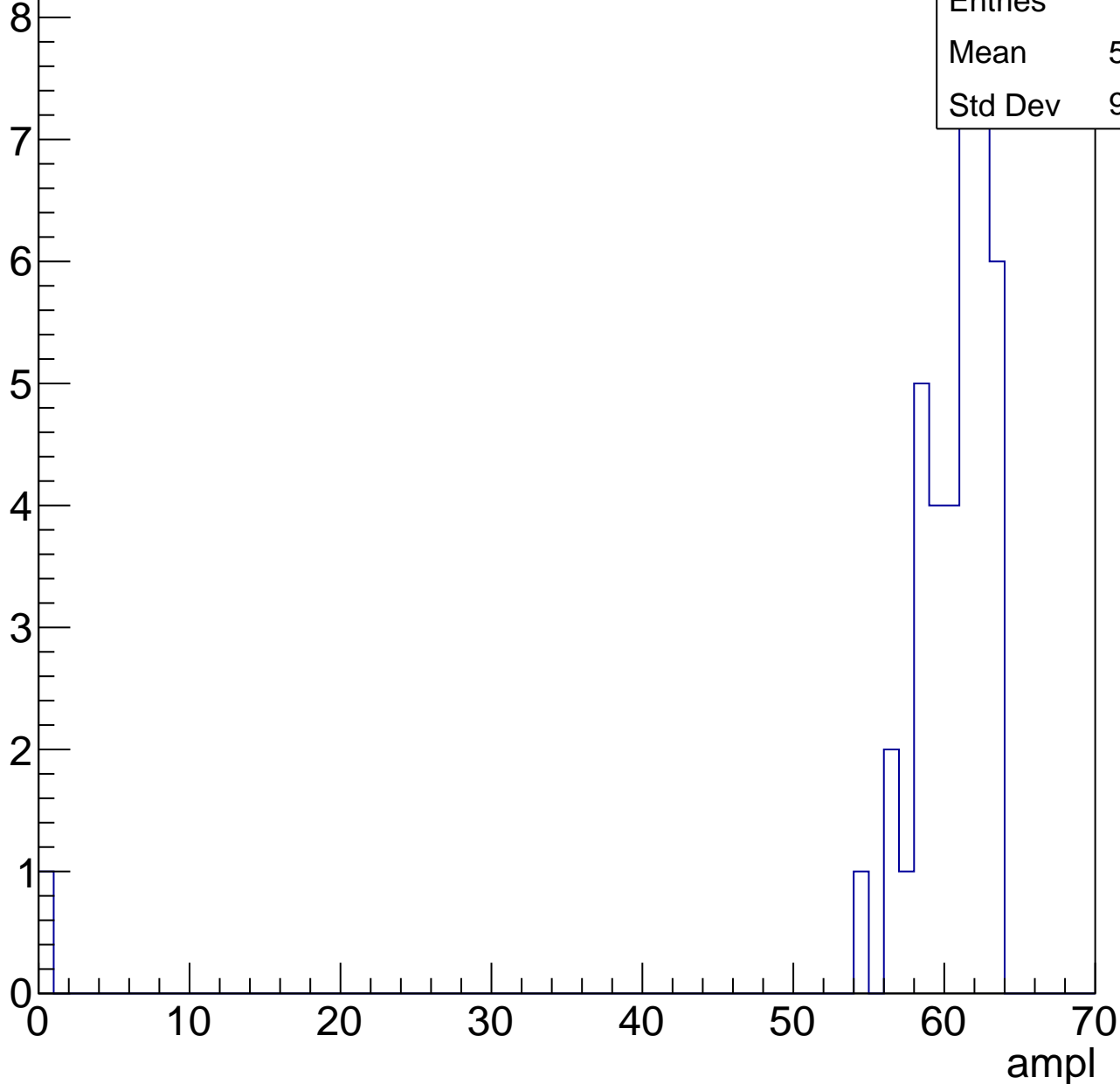


B1L103S, U11-ch21, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	58.77
Std Dev	9.663



B1L103S, U11-ch21, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch21, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

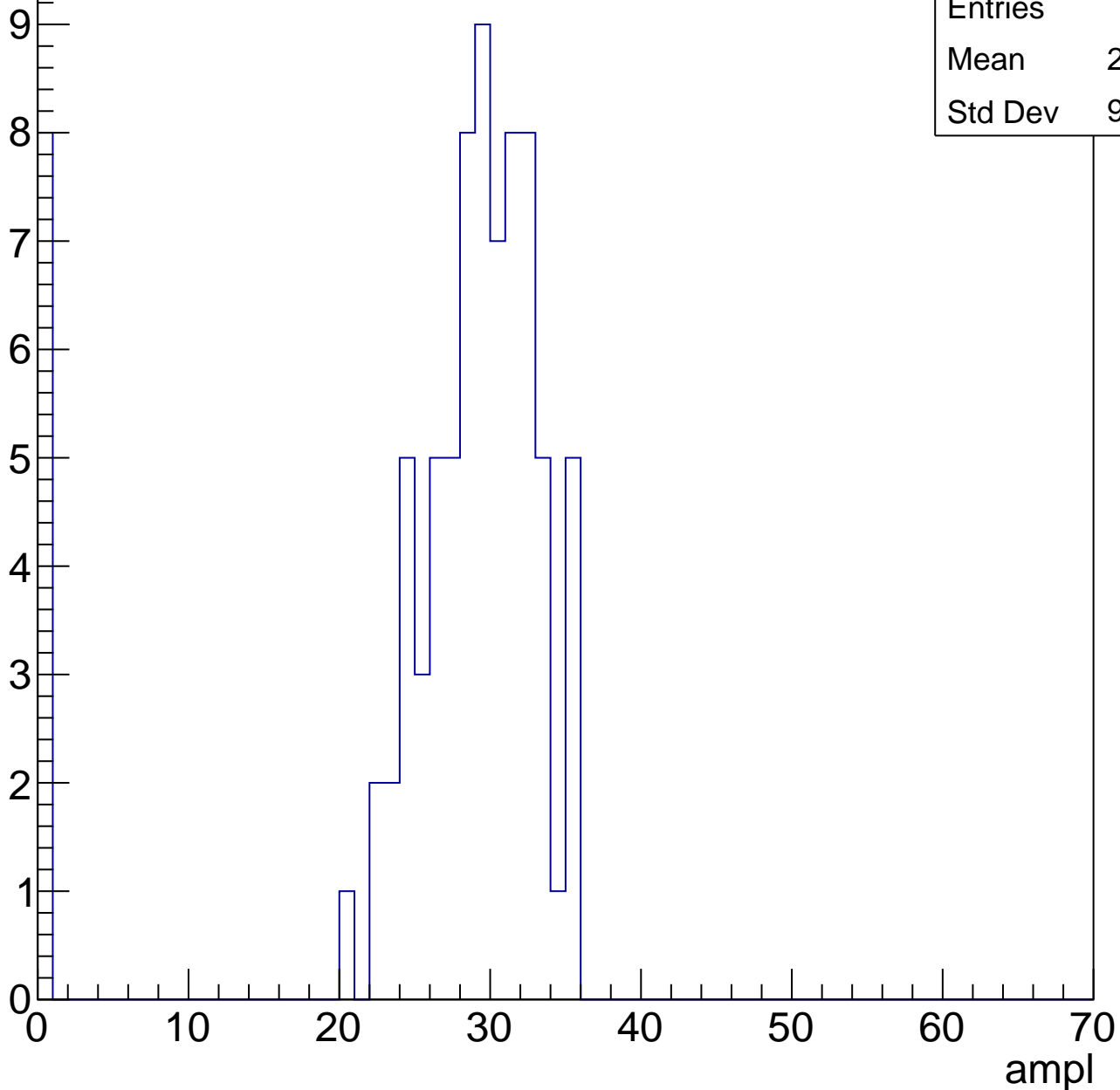


B1L103S, U11-ch22, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	82
Mean	26.13
Std Dev	9.205

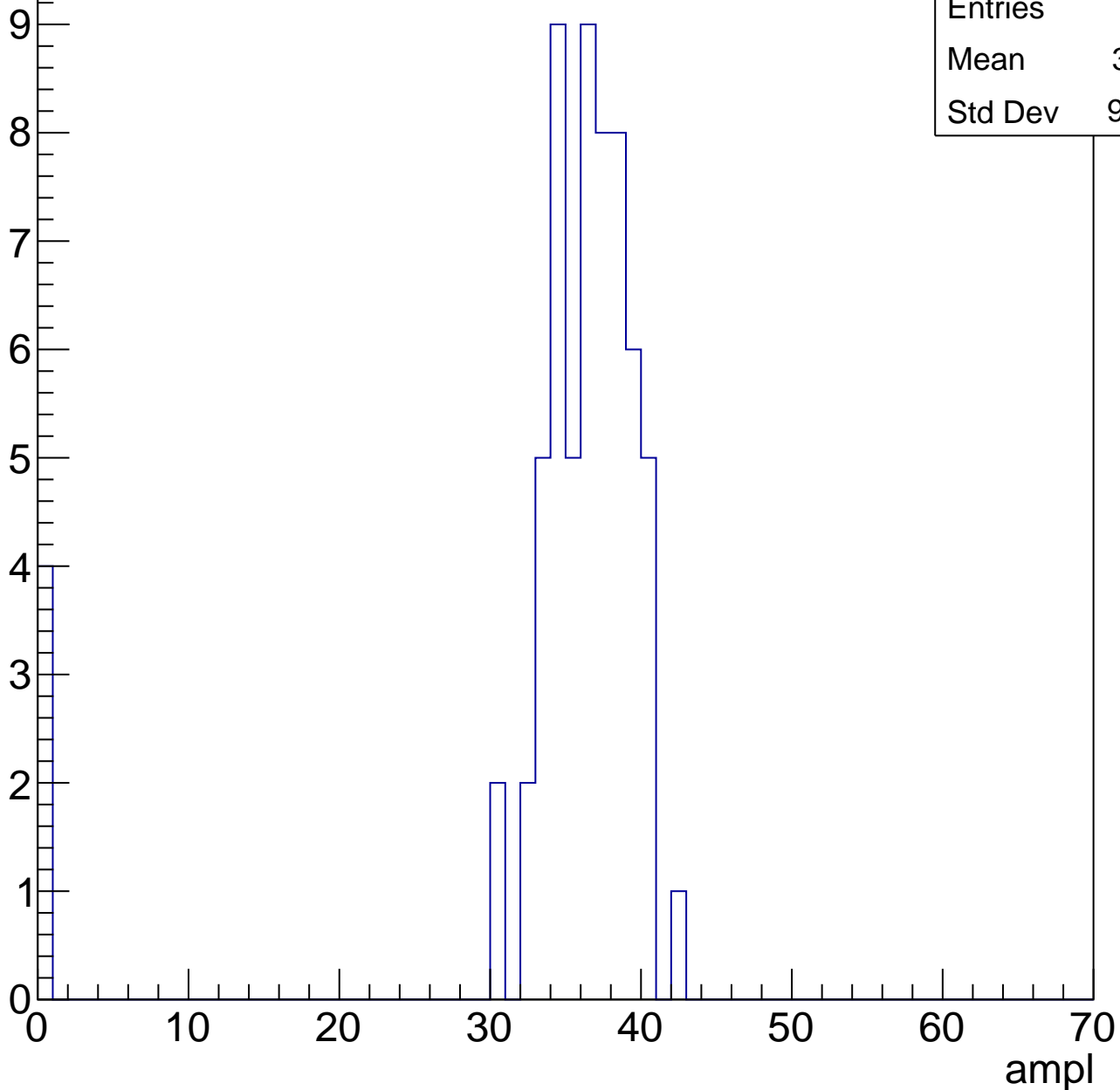


B1L103S, U11-ch22, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

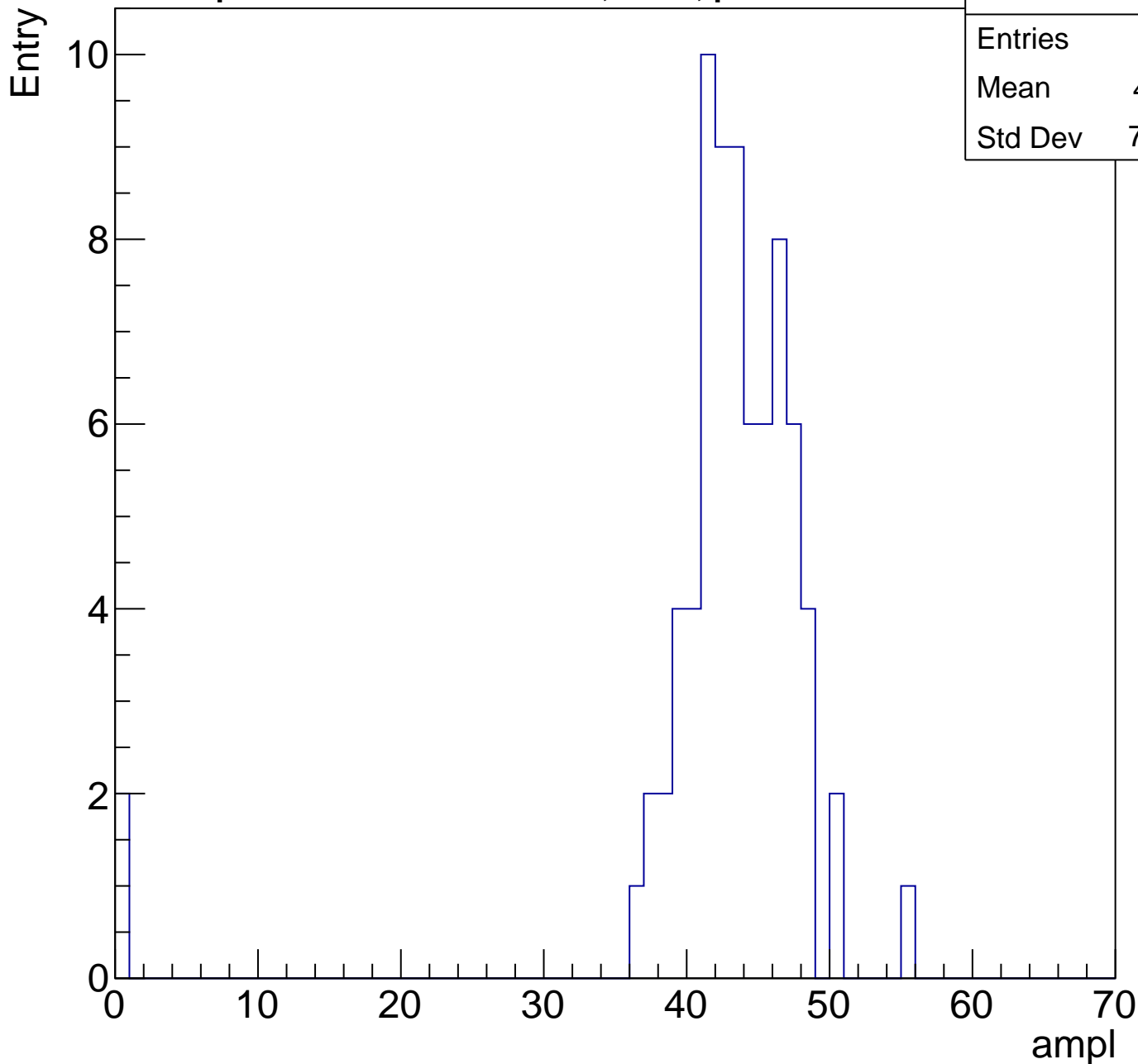
Entries	64
Mean	33.91
Std Dev	9.103



B1L103S, U11-ch22, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	76
Mean	42.21
Std Dev	7.704

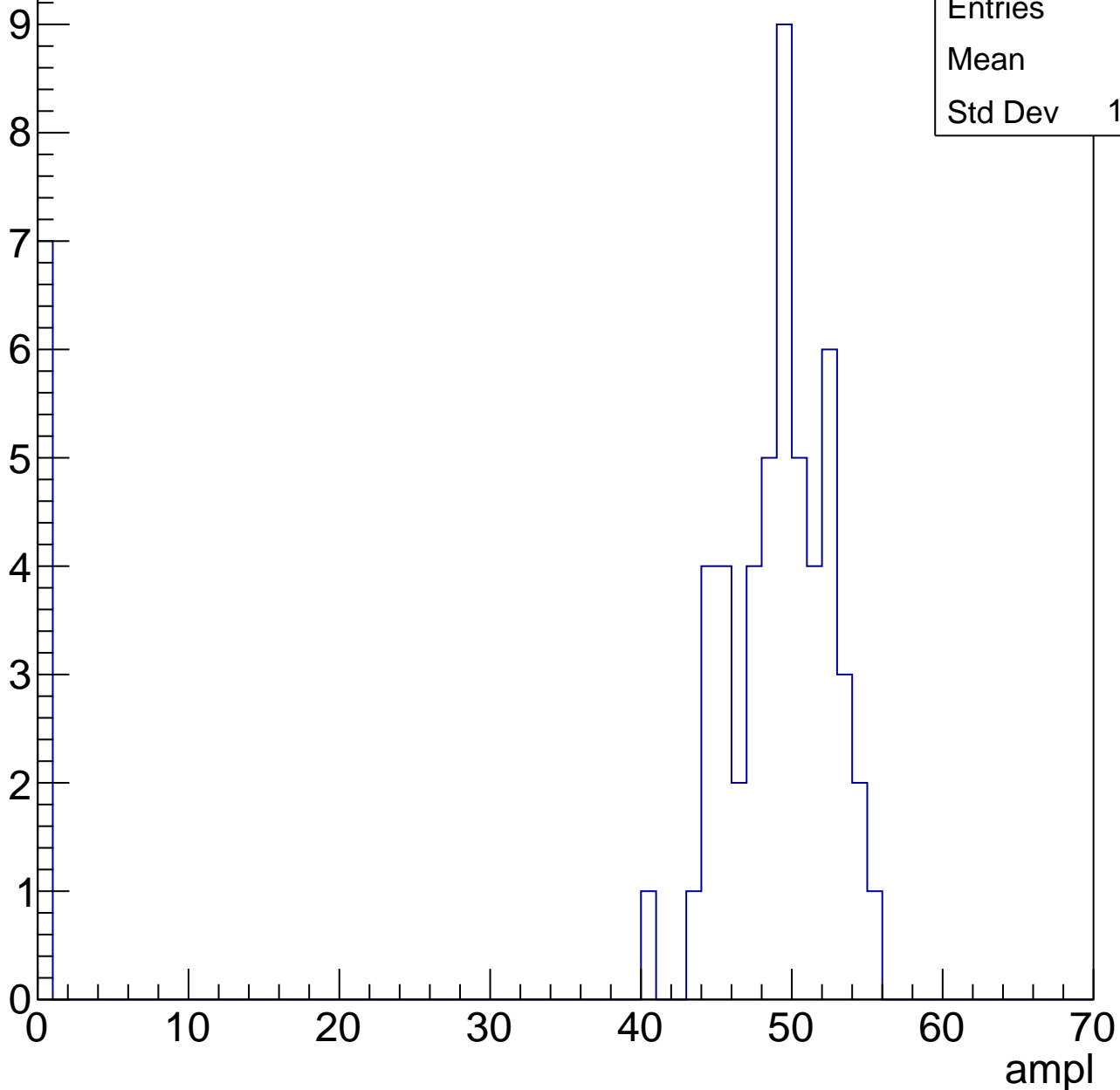


B1L103S, U11-ch22, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	42.9
Std Dev	16.18

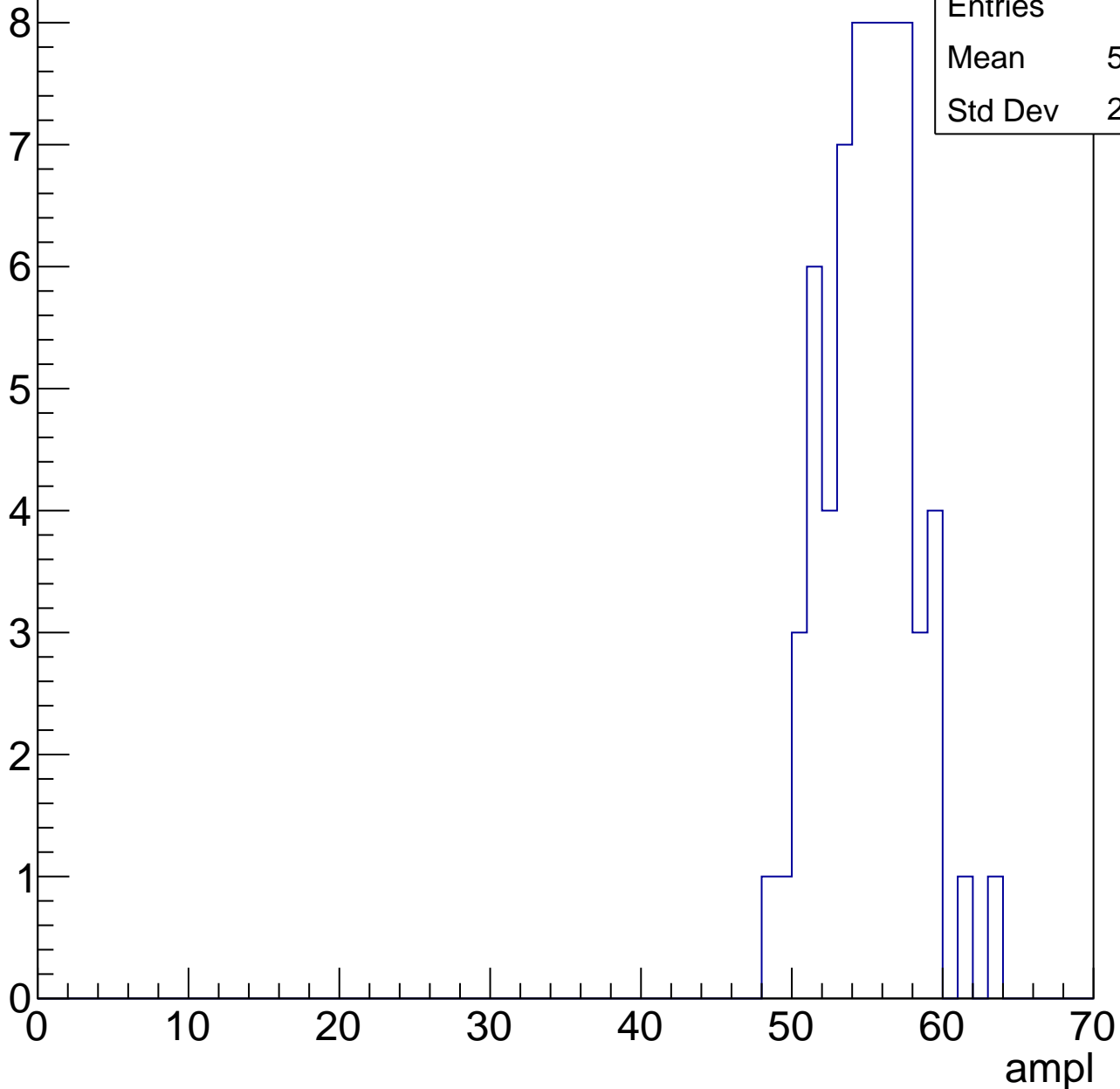


B1L103S, U11-ch22, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	54.63
Std Dev	2.956



B1L103S, U11-ch22, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

Entries 54

Mean 59.2

Std Dev 8.352

8

6

4

2

0

0

10

20

30

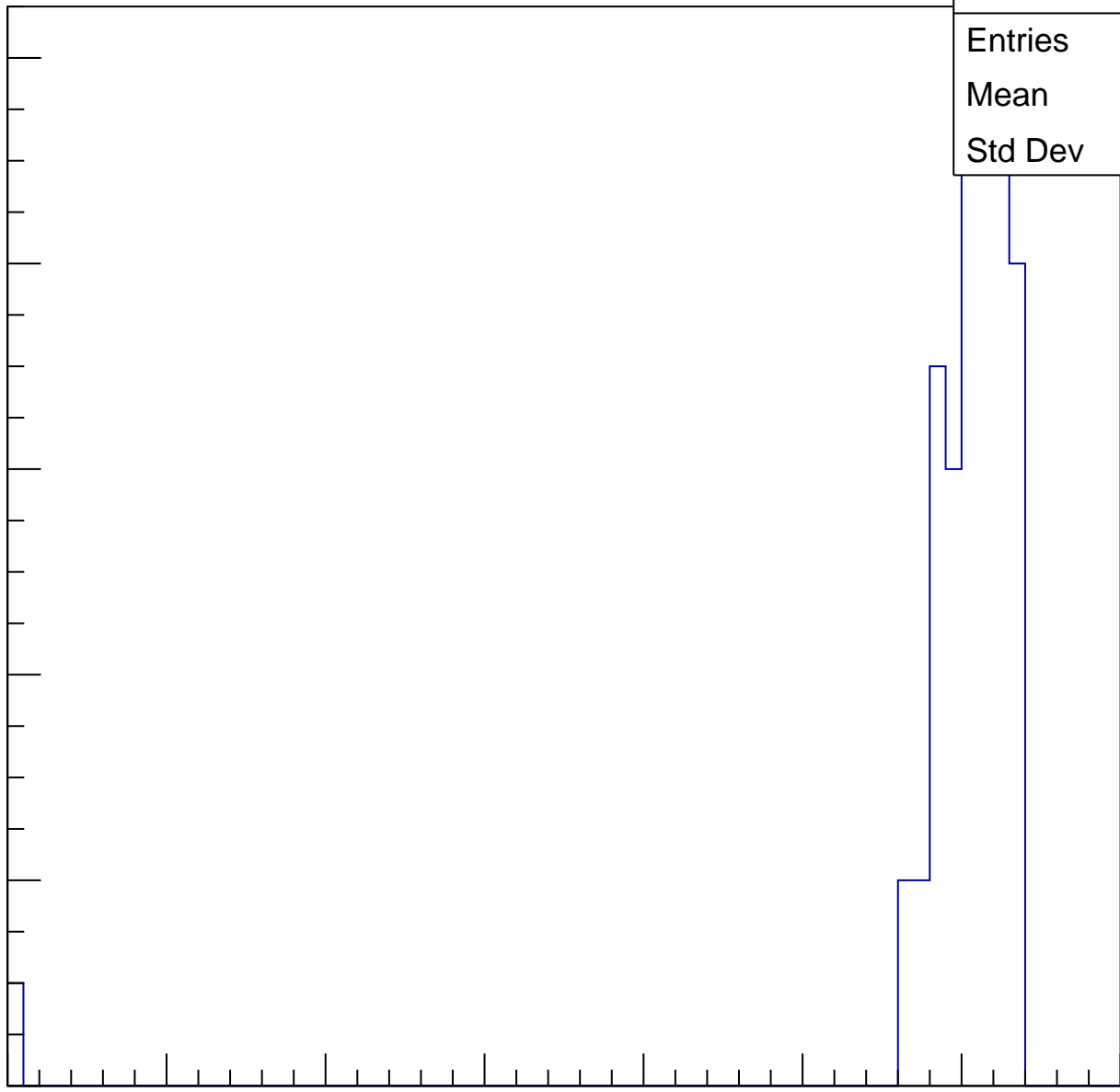
40

50

60

70

ampl



B1L103S, U11-ch22, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch22, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

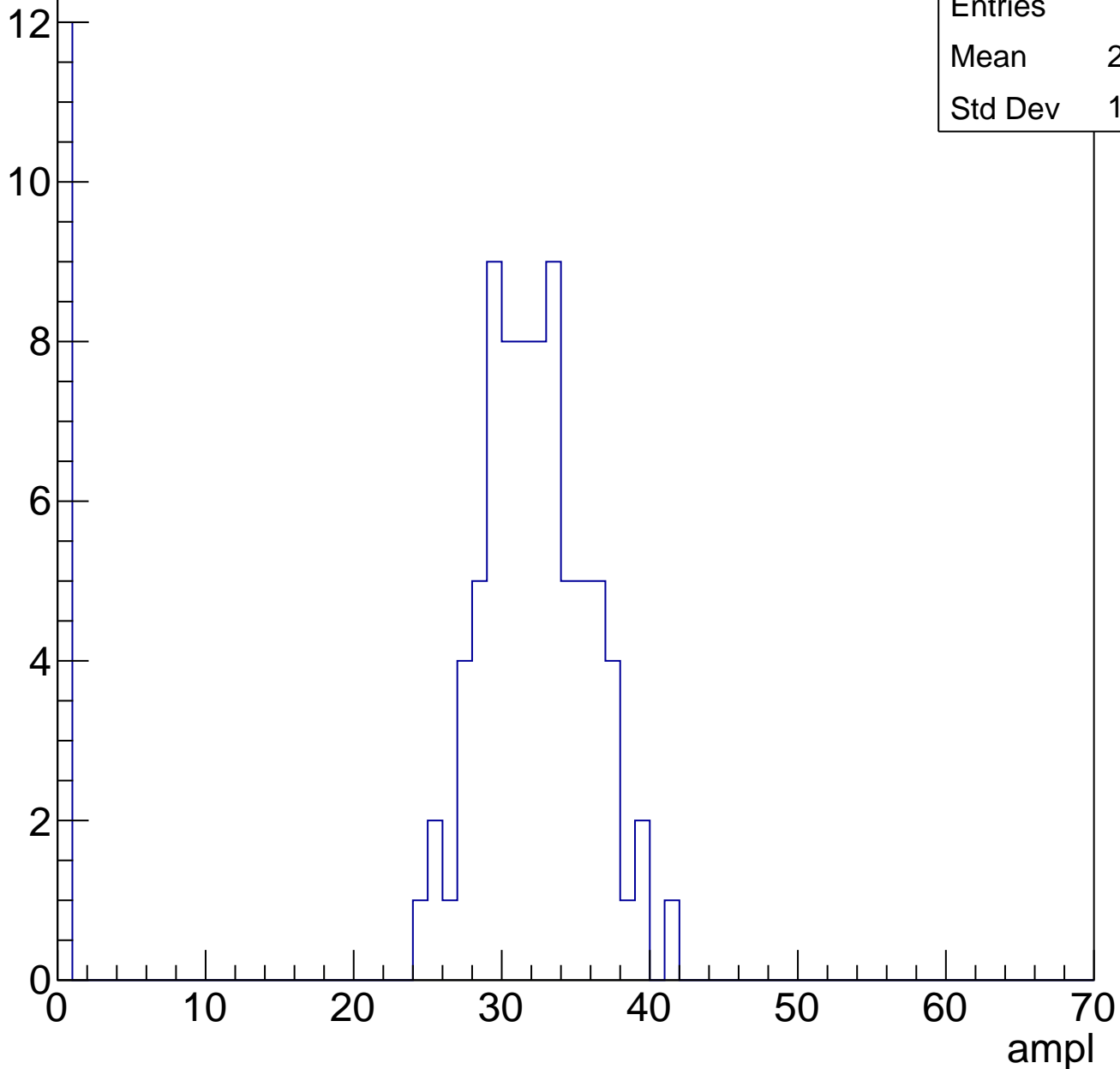
ampl

B1L103S, U11-ch23, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	90
Mean	27.56
Std Dev	11.29

Entry

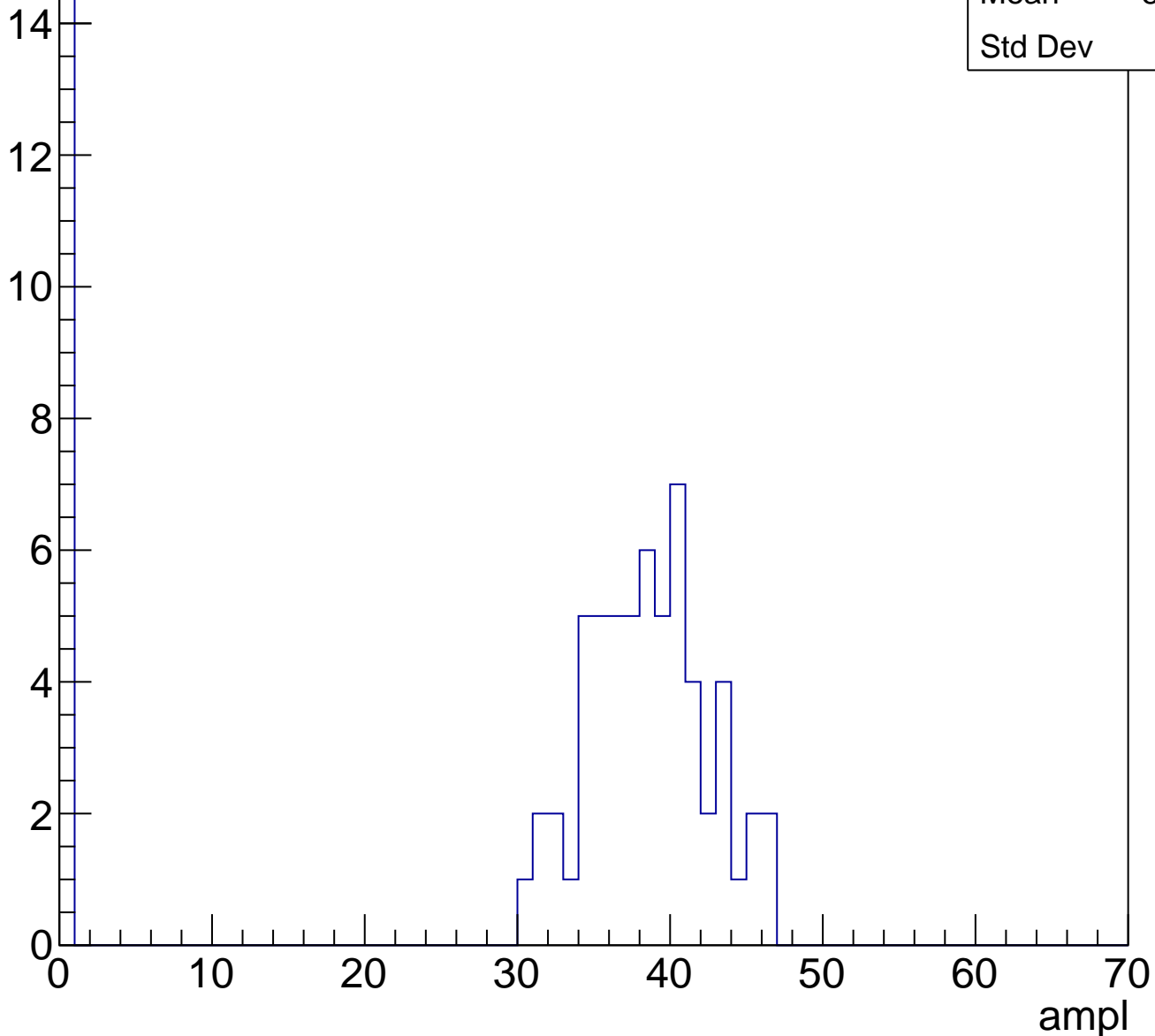


B1L103S, U11-ch23, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	74
Mean	30.38
Std Dev	15.7

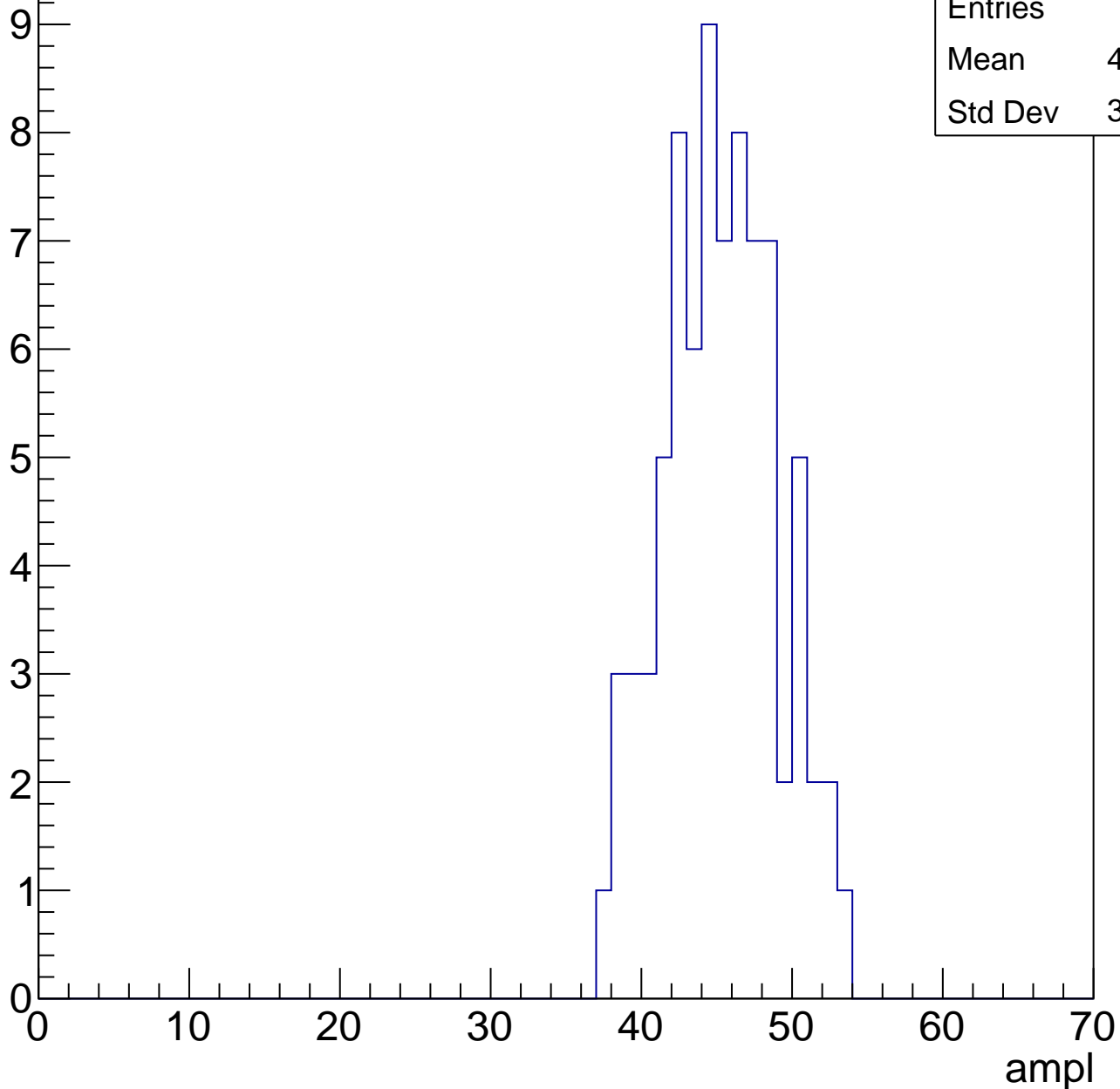
Entry



B1L103S, U11-ch23, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

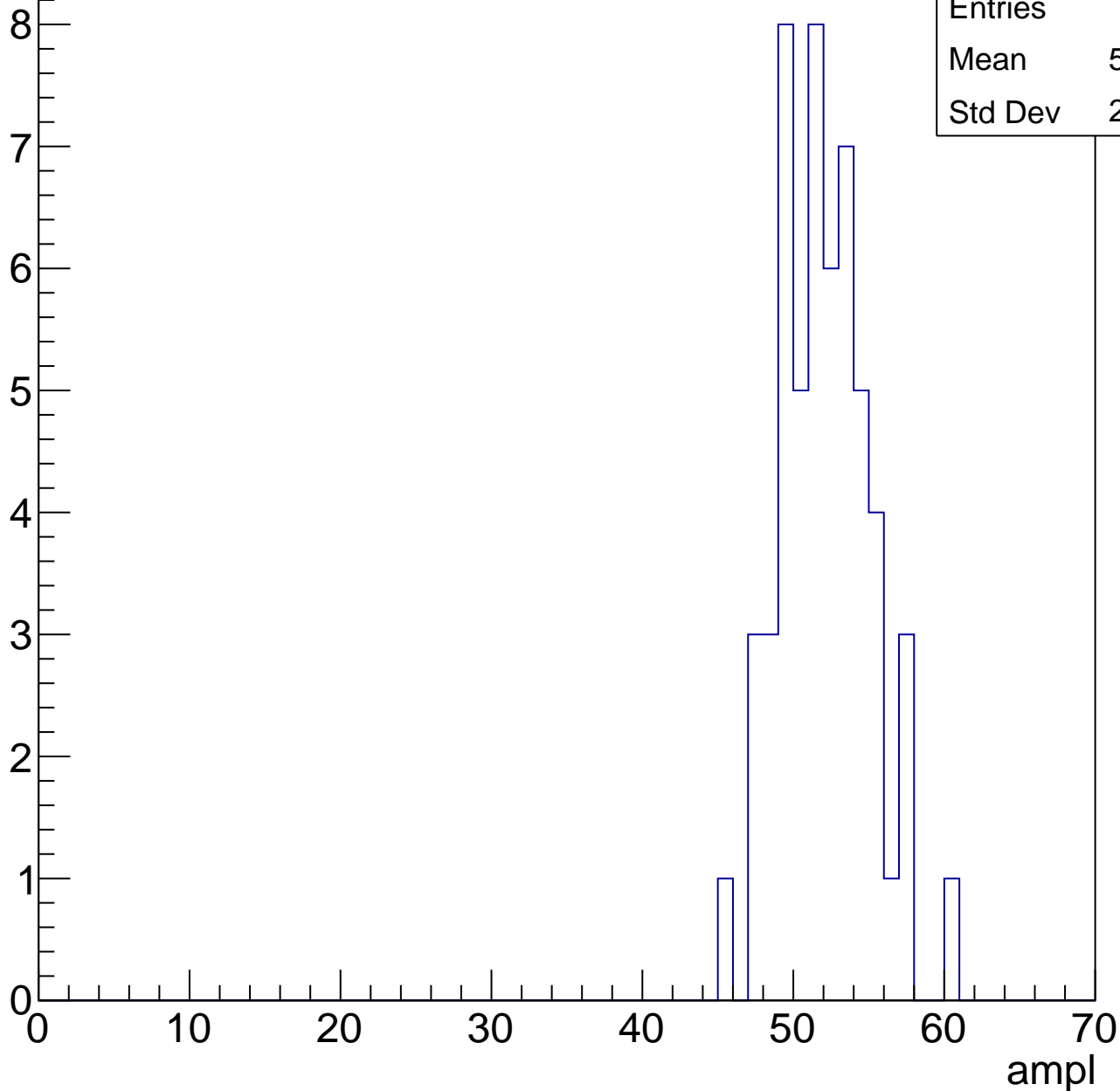


B1L103S, U11-ch23, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	51.64
Std Dev	2.963

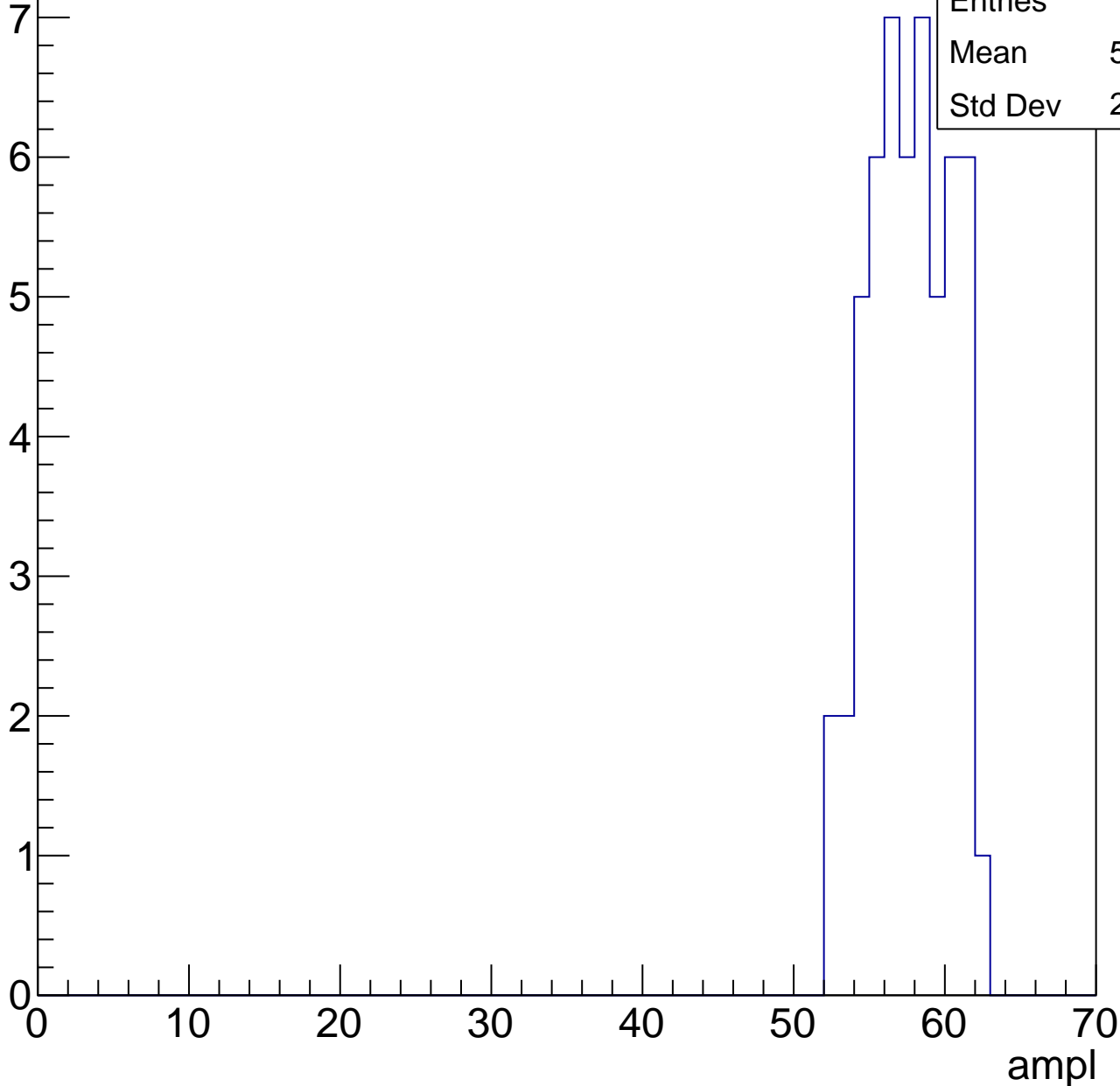


B1L103S, U11-ch23, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	57.23
Std Dev	2.596

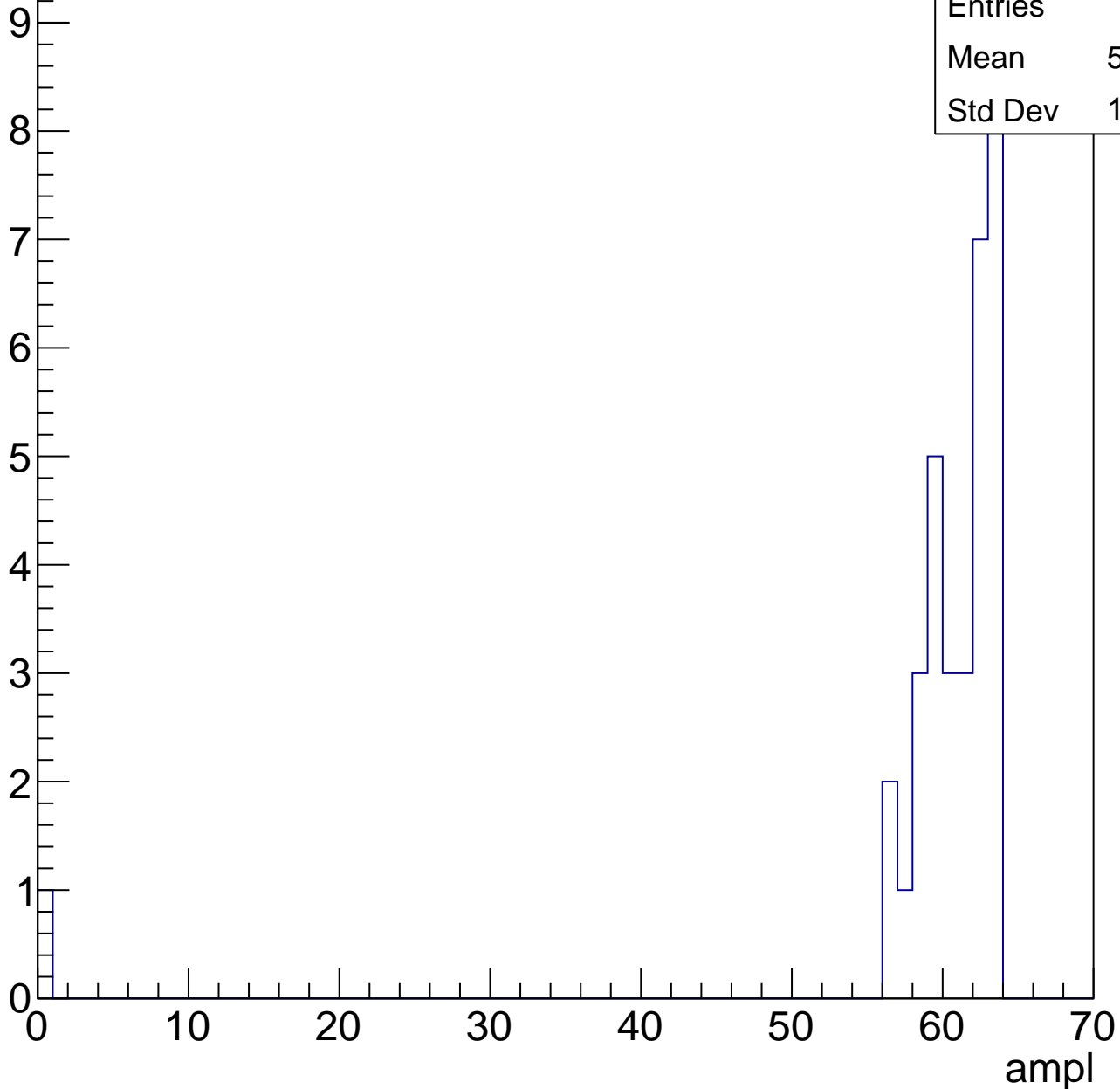


B1L103S, U11-ch23, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	34
Mean	58.88
Std Dev	10.47



B1L103S, U11-ch23, adc6

calib_packv5_041523_1651.root, FC#0, port C2

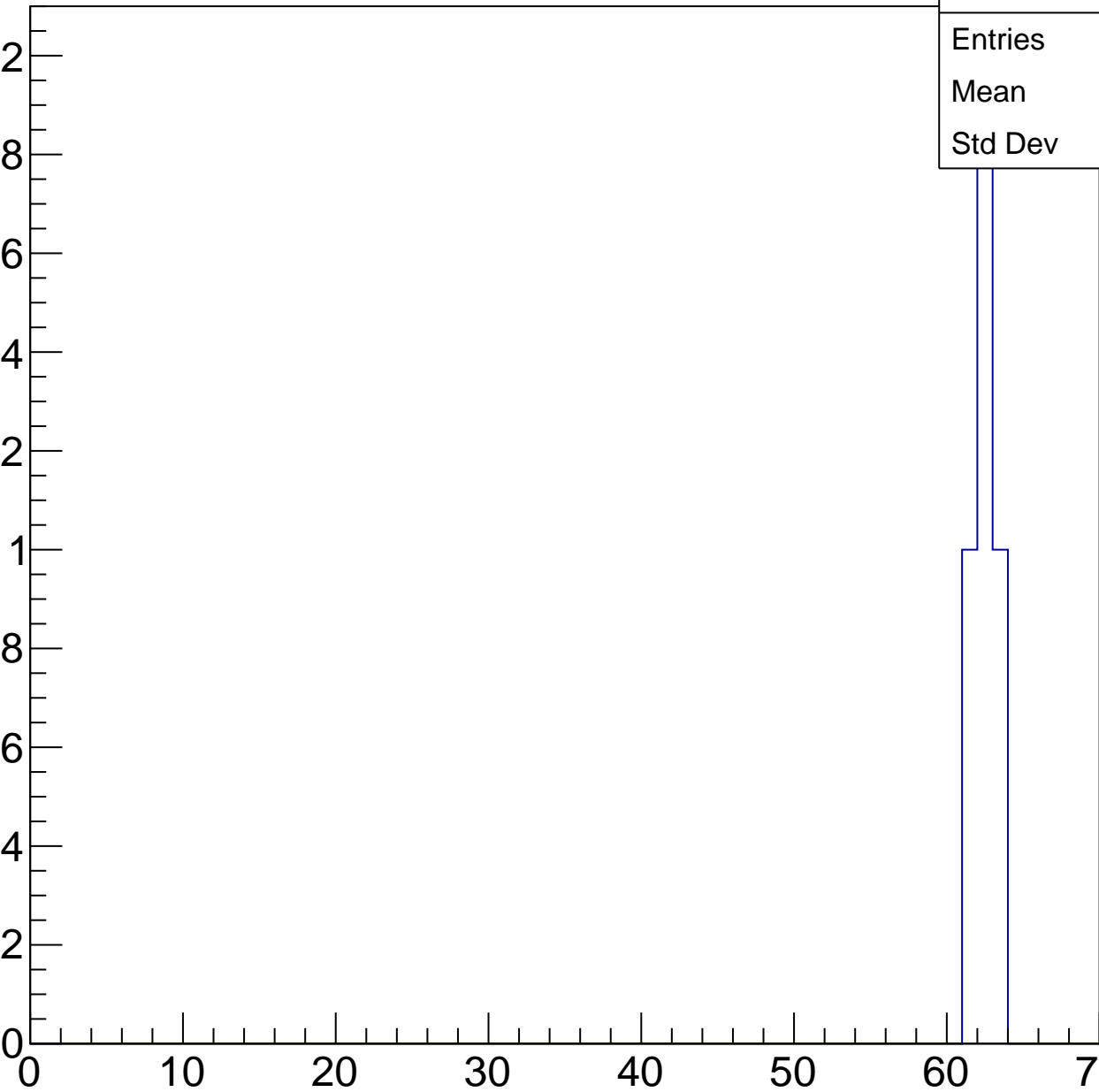
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	4
Mean	62
Std Dev	0.7071

0 10 20 30 40 50 60 70

ampl

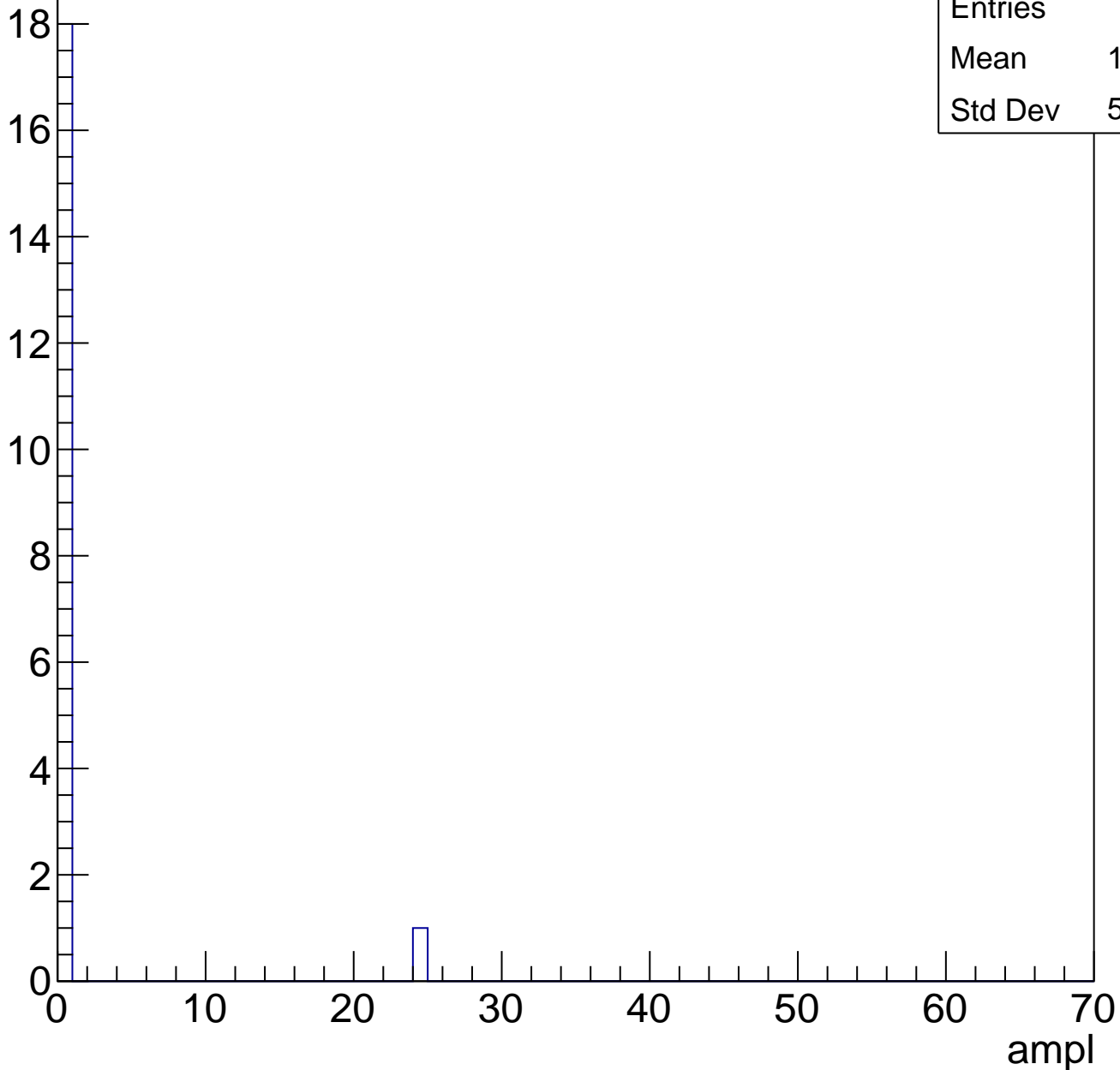


B1L103S, U11-ch23, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.263
Std Dev	5.359

Entry

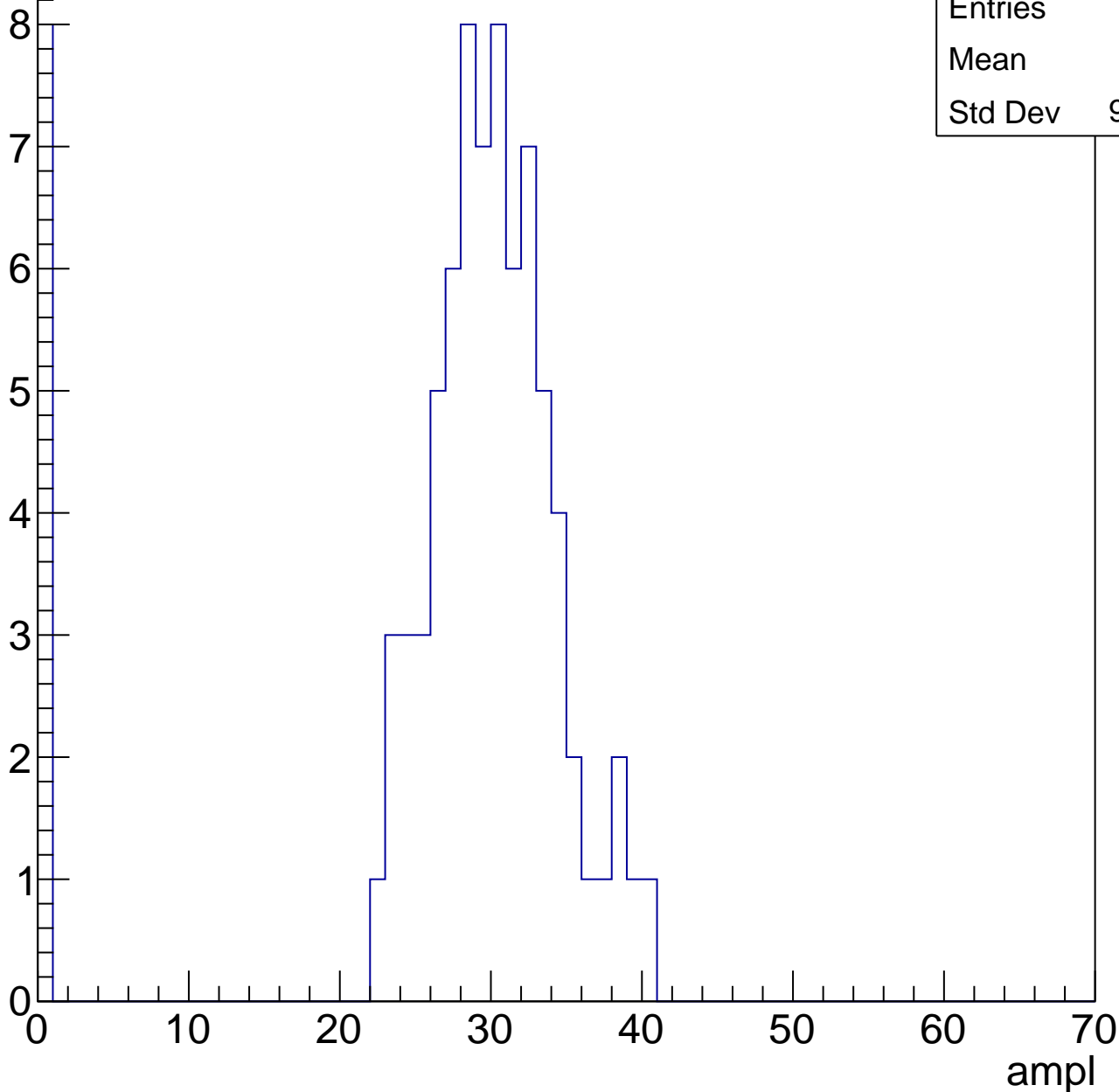


B1L103S, U11-ch24, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	82
Mean	26.9
Std Dev	9.606

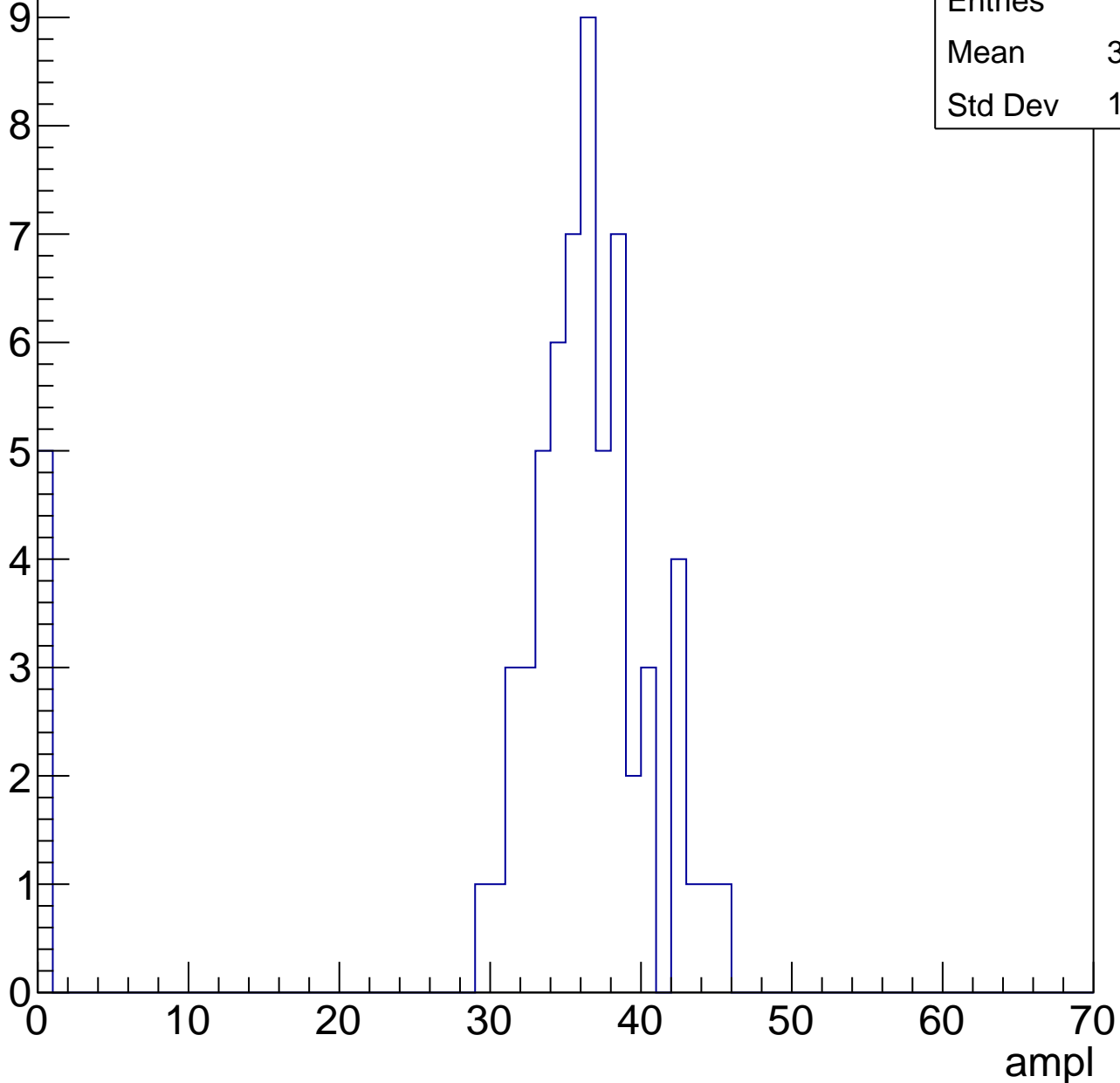


B1L103S, U11-ch24, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	33.36
Std Dev	10.27

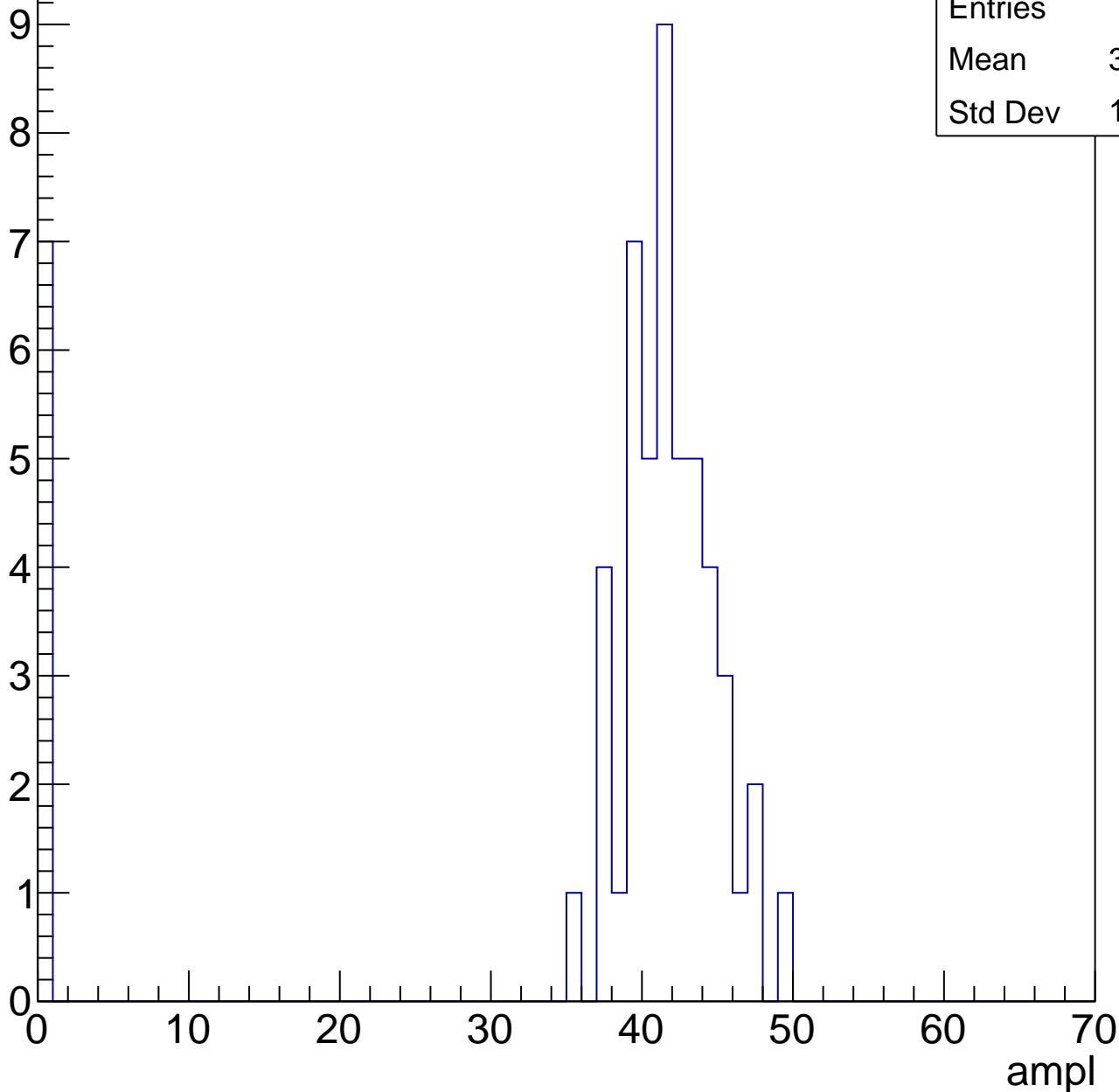


B1L103S, U11-ch24, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	36.15
Std Dev	14.07



B1L103S, U11-ch24, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	85
Mean	48.27
Std Dev	3.376

Entry

10

8

6

4

2

0

0

10

20

30

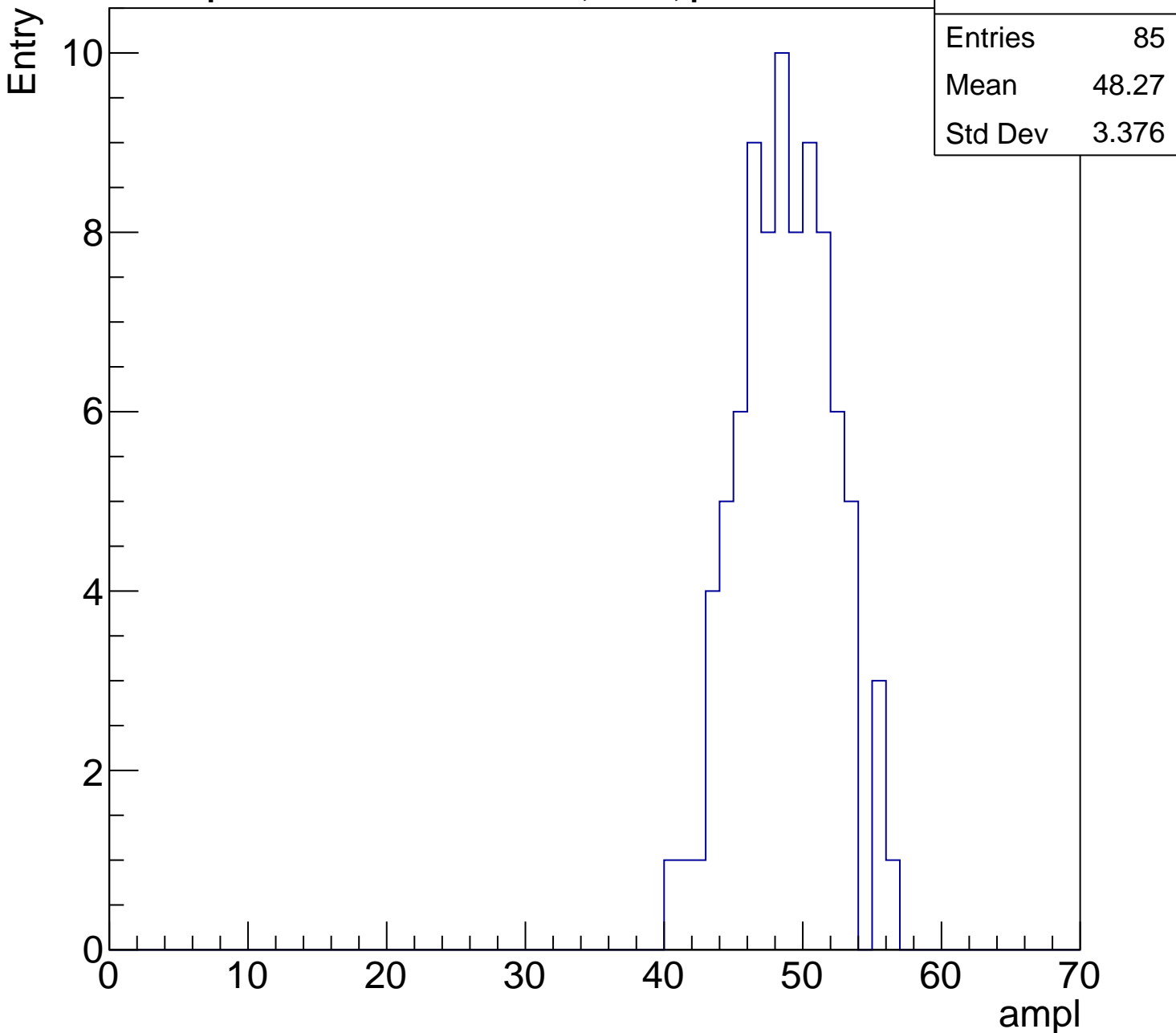
40

50

60

70

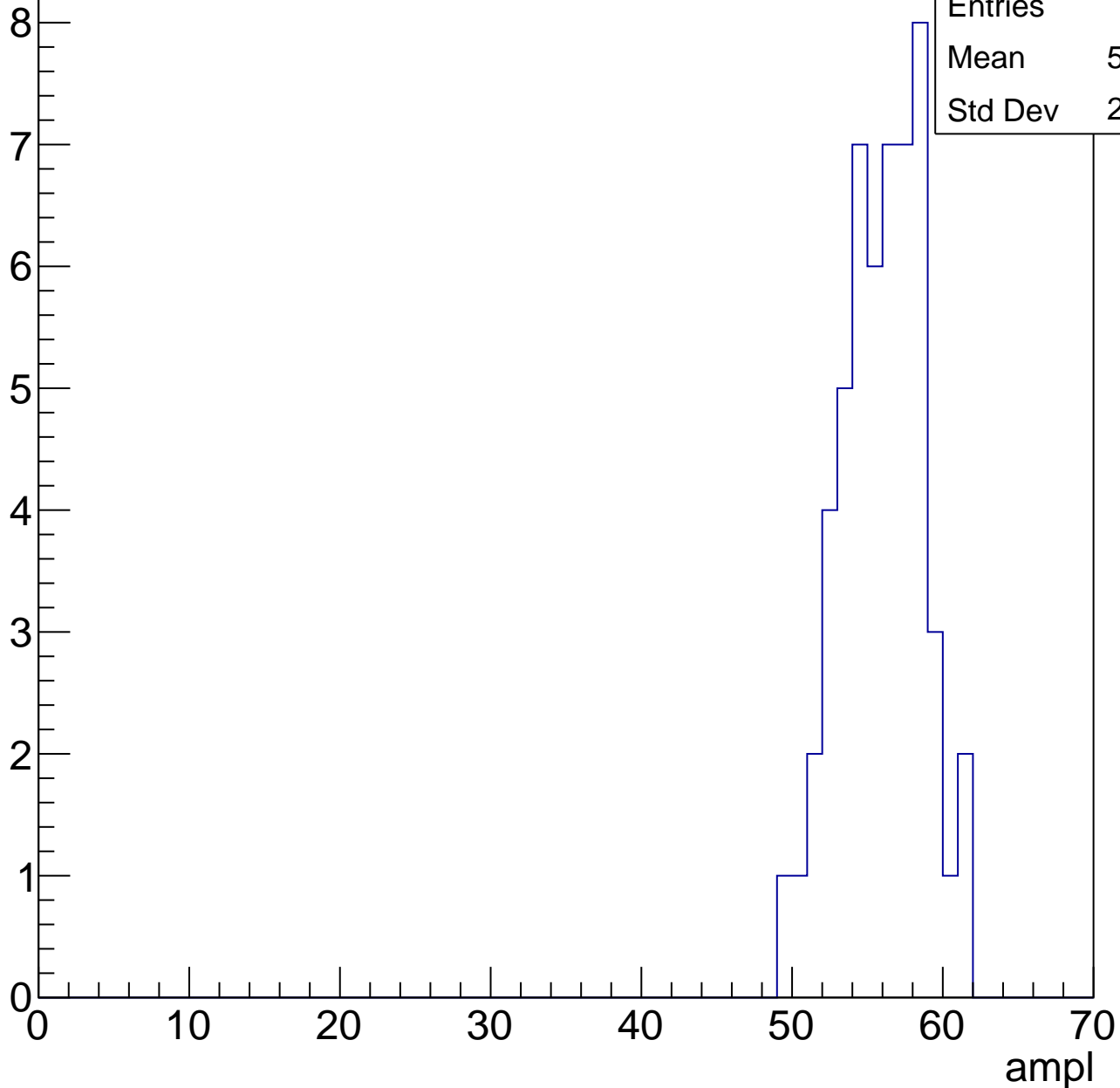
ampl



B1L103S, U11-ch24, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



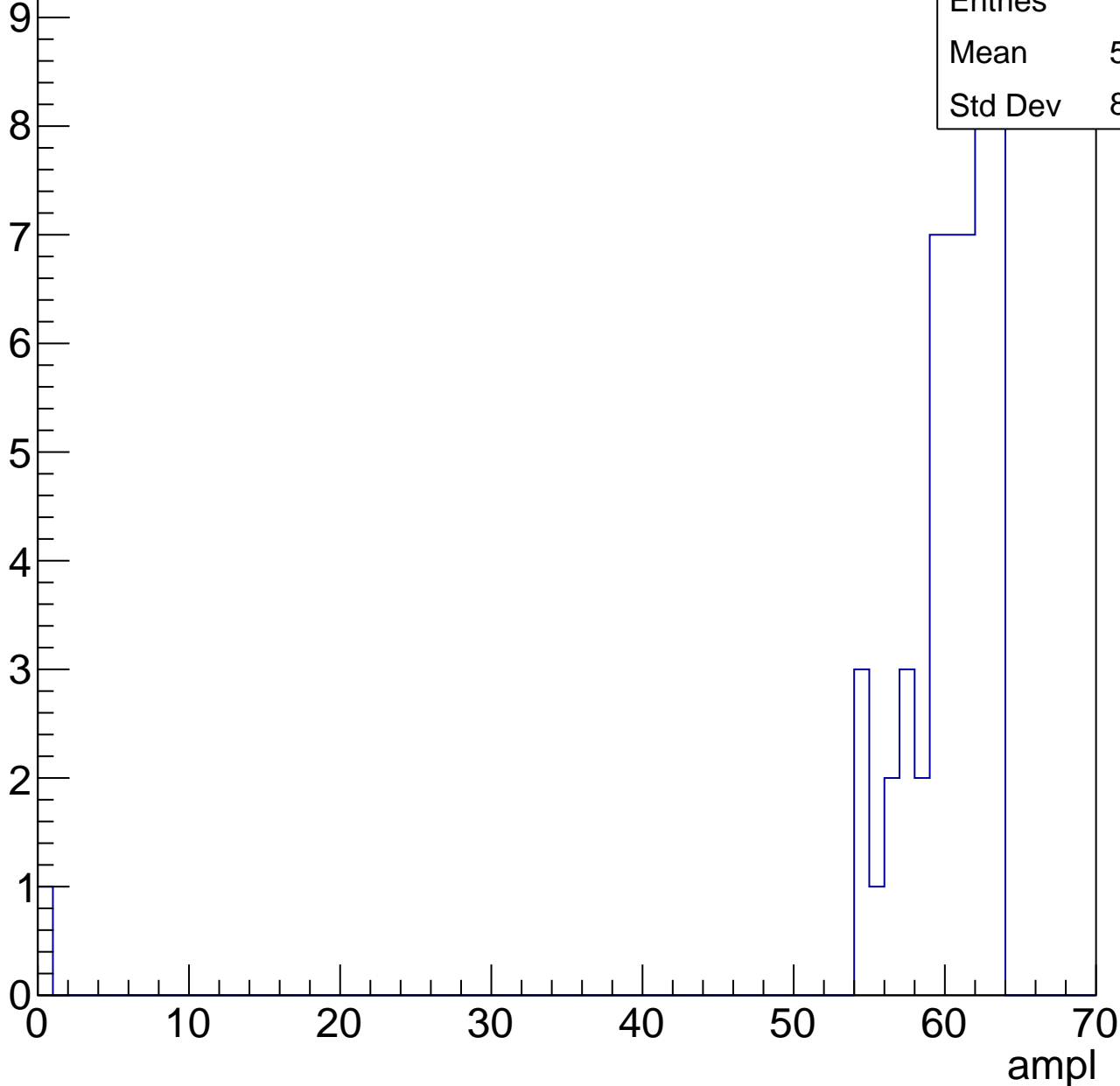
Entries	54
Mean	55.48
Std Dev	2.706

B1L103S, U11-ch24, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

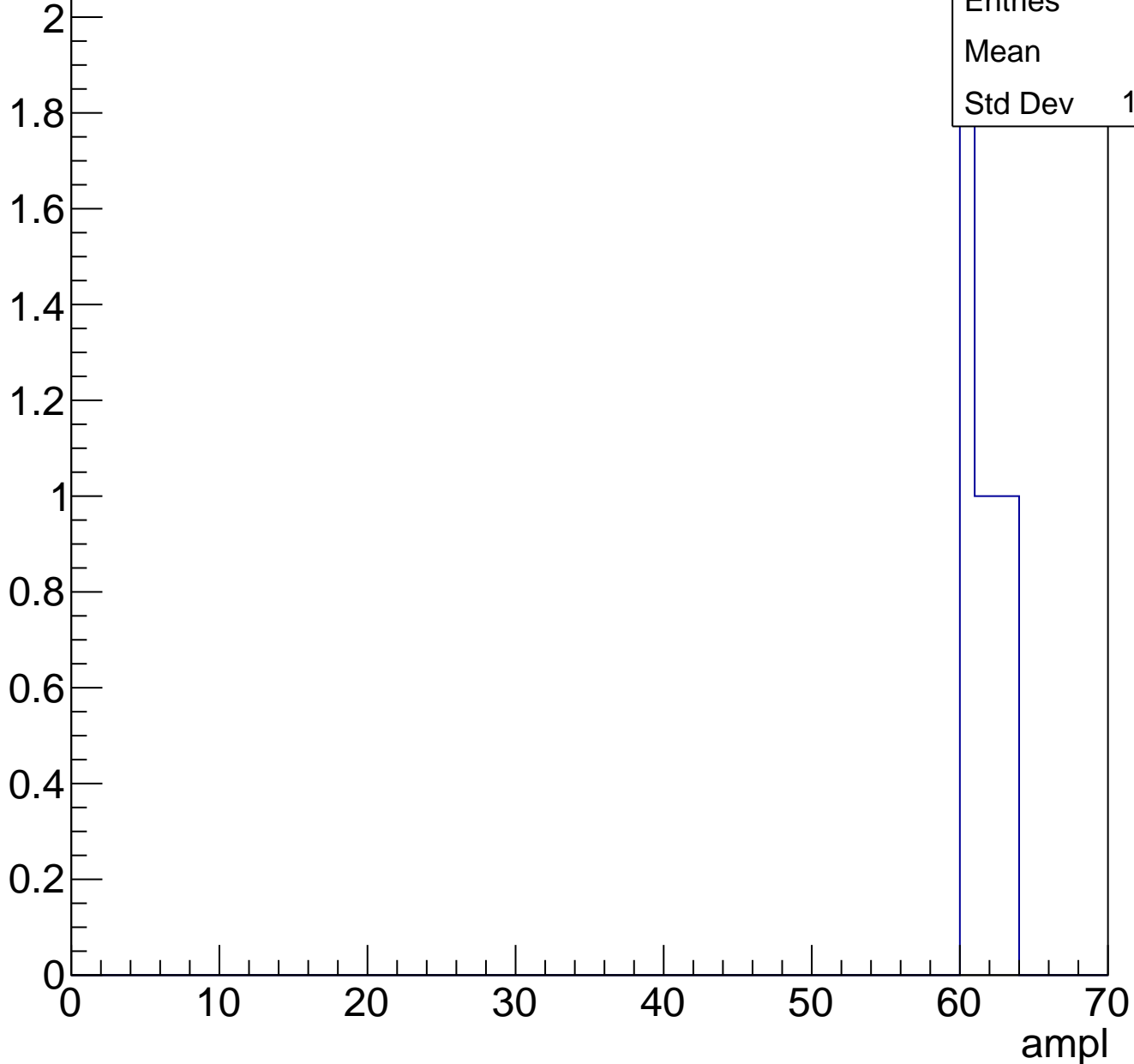
Entries	51
Mean	58.84
Std Dev	8.703



B1L103S, U11-ch24, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

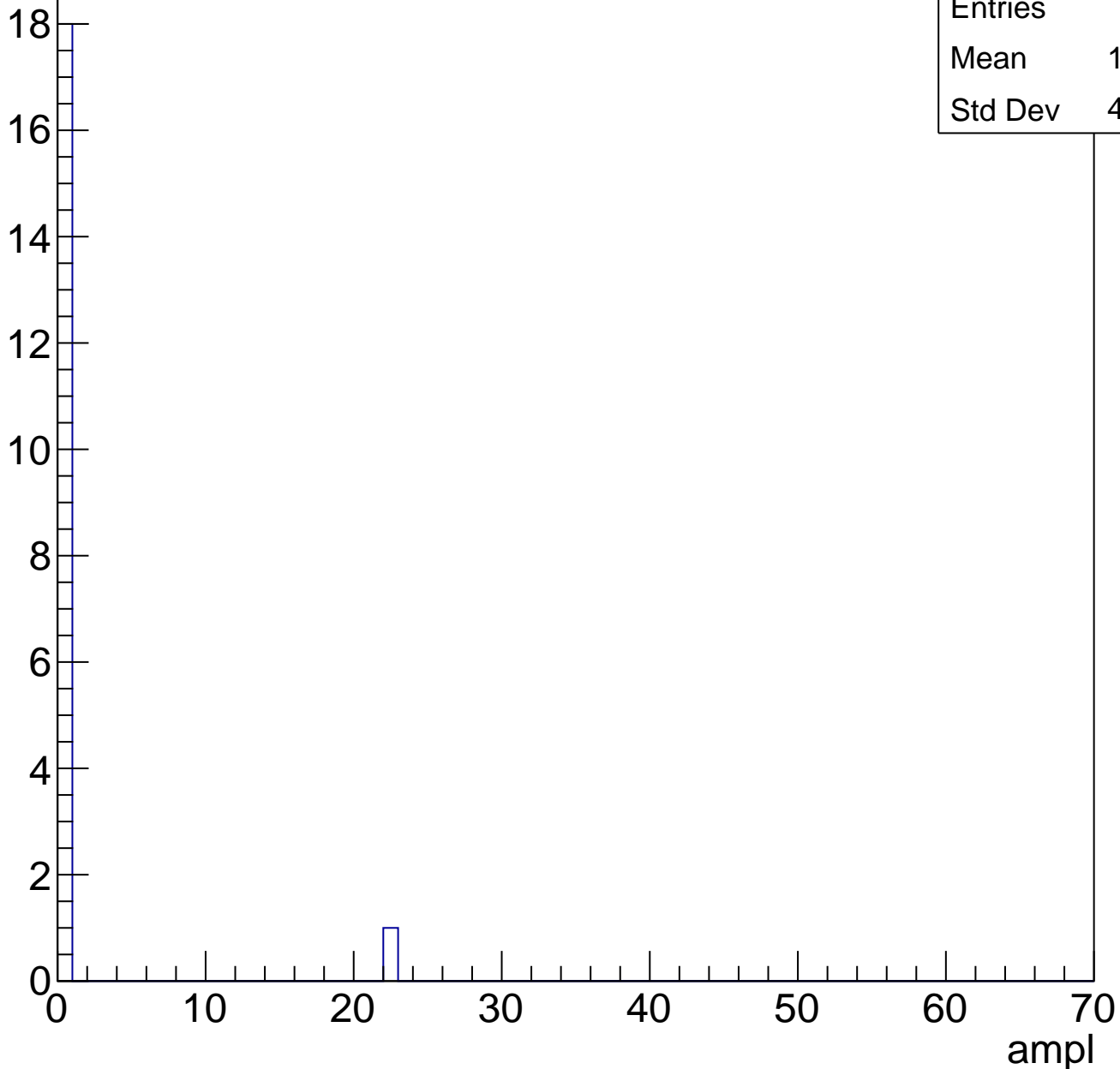


B1L103S, U11-ch24, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.158
Std Dev	4.913

Entry

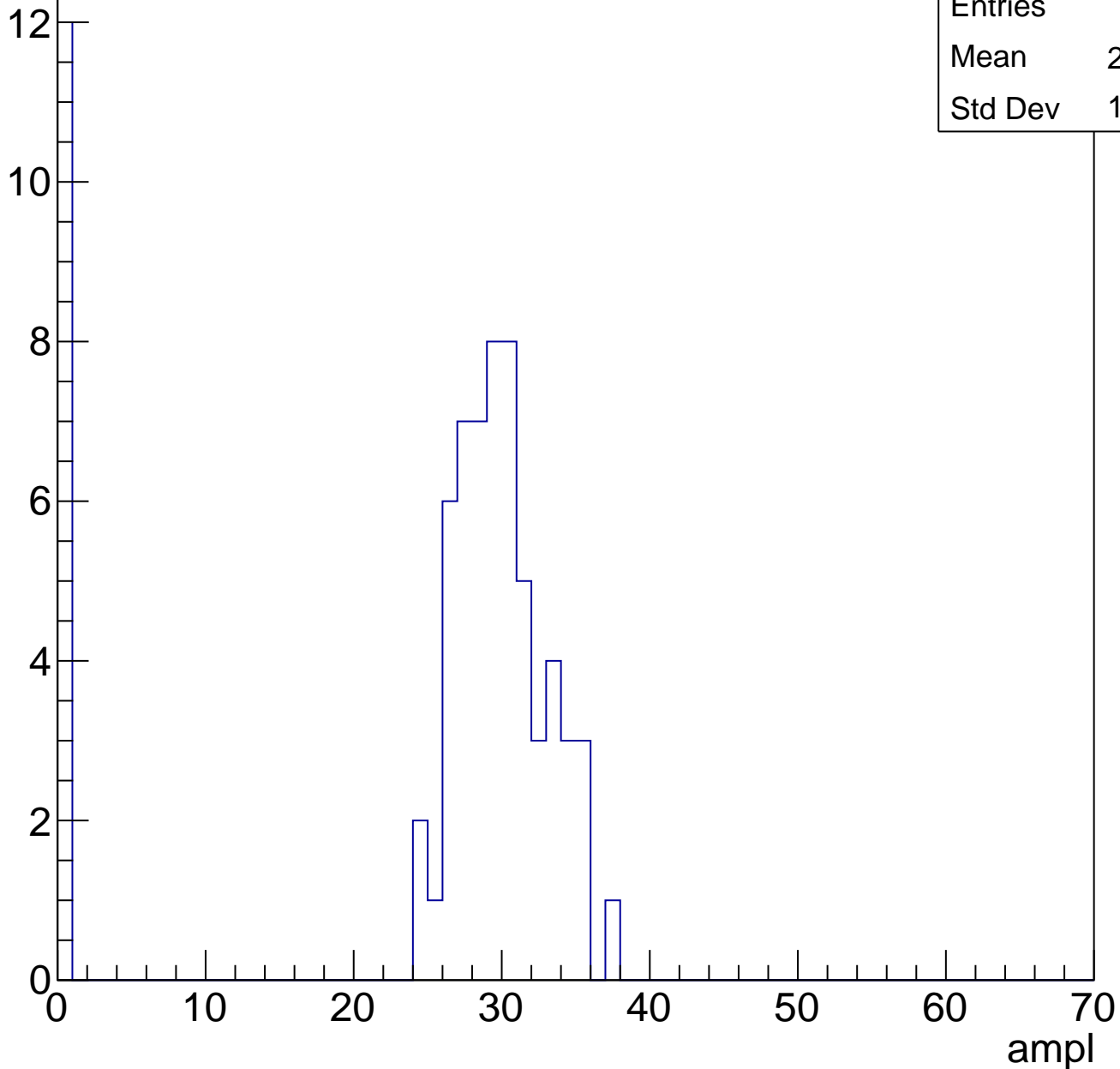


B1L103S, U11-ch25, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	70
Mean	24.47
Std Dev	11.45

Entry



B1L103S, U11-ch25, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	100
Mean	32.33
Std Dev	11.98

Entry

10

8

6

4

2

0

0

10

20

30

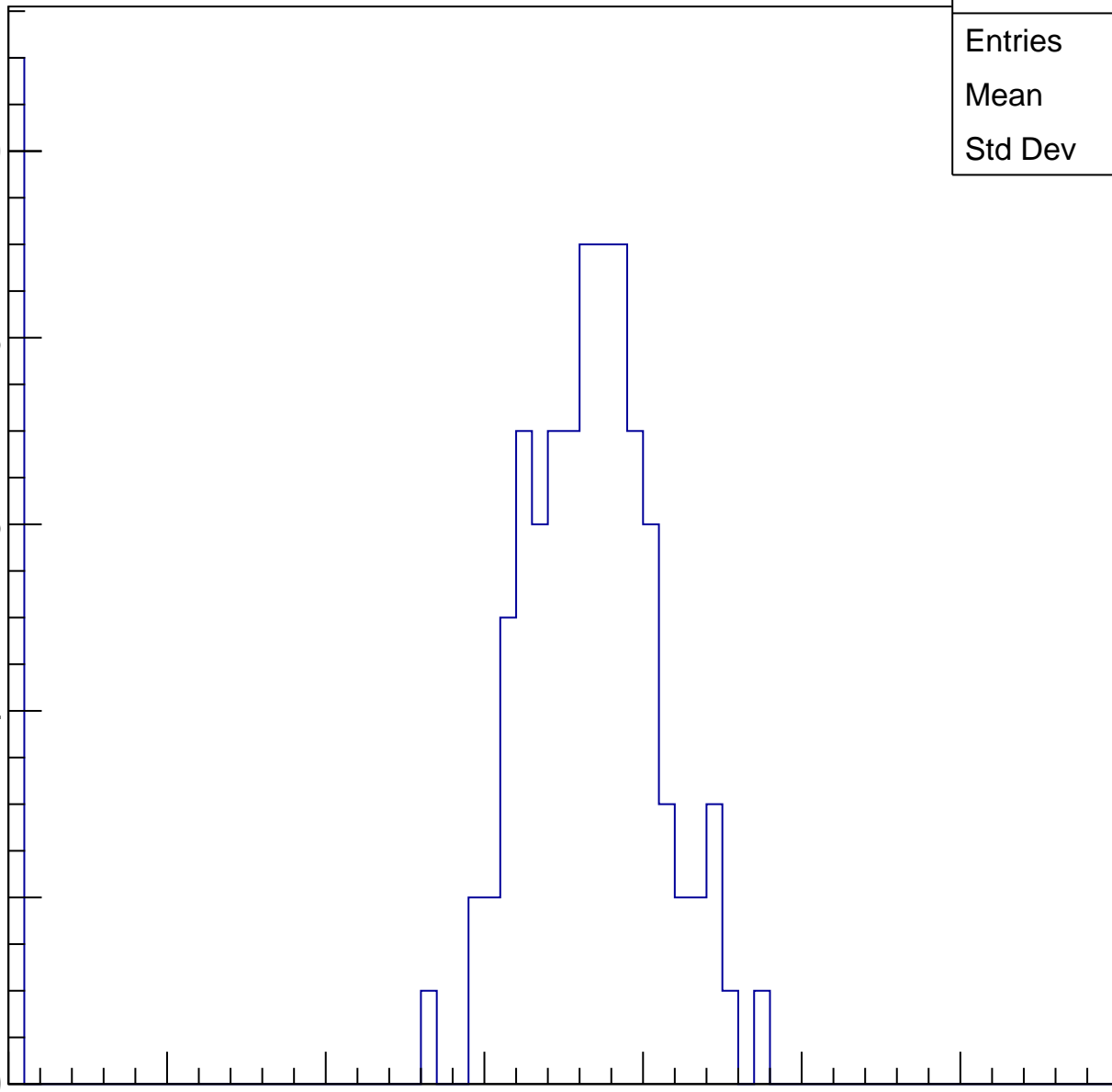
40

50

60

70

ampl

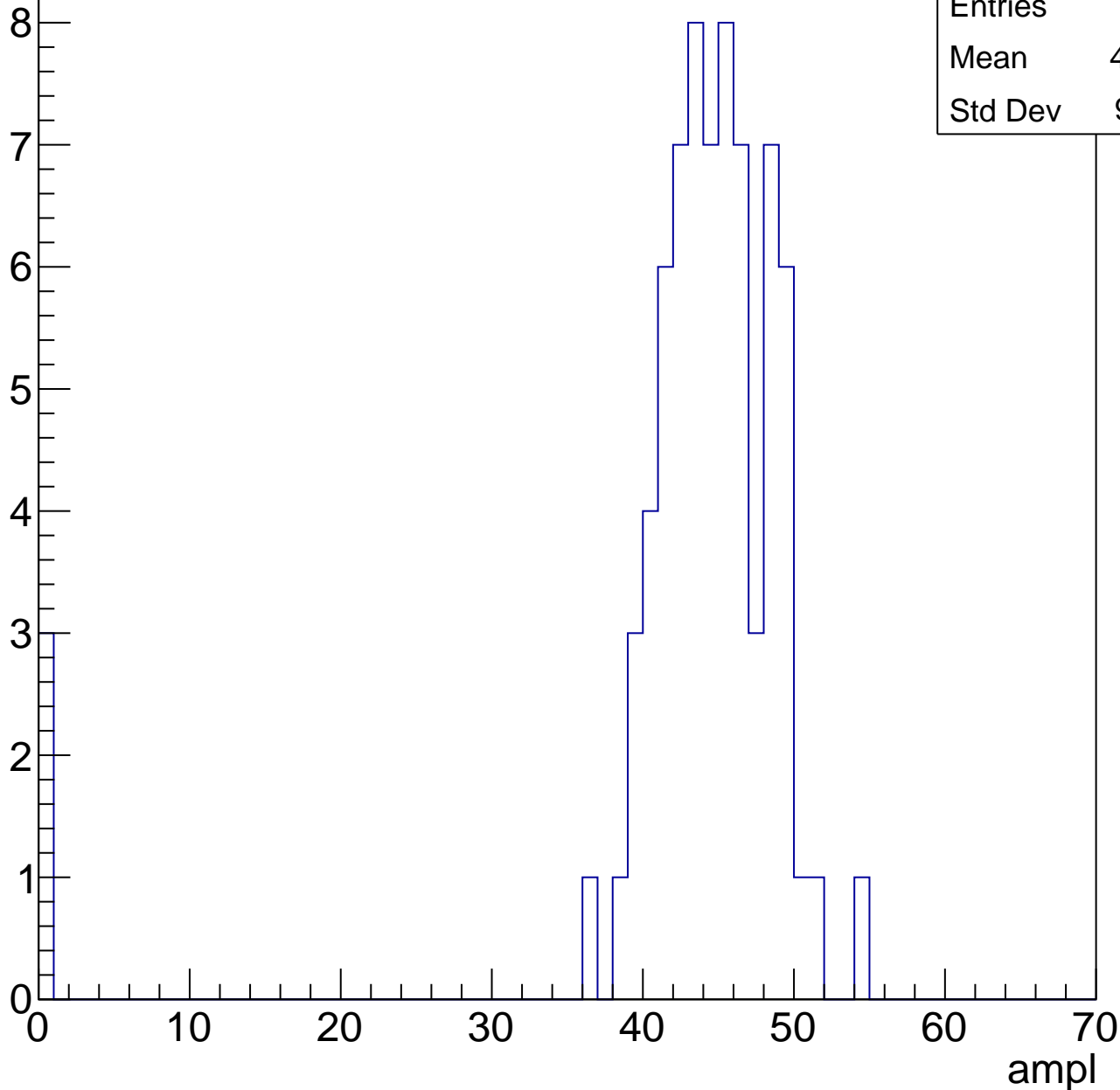


B1L103S, U11-ch25, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	42.58
Std Dev	9.371

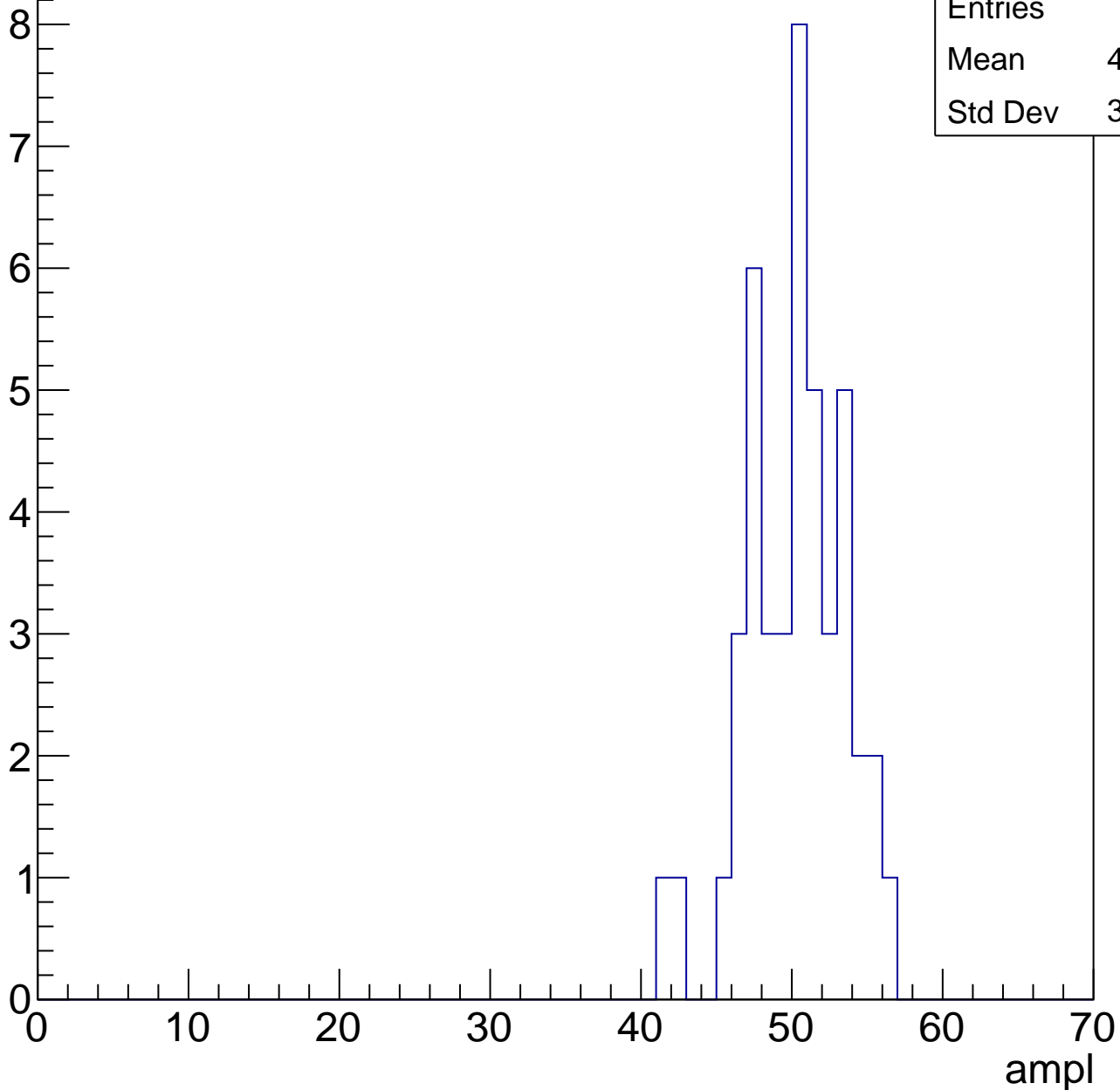


B1L103S, U11-ch25, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

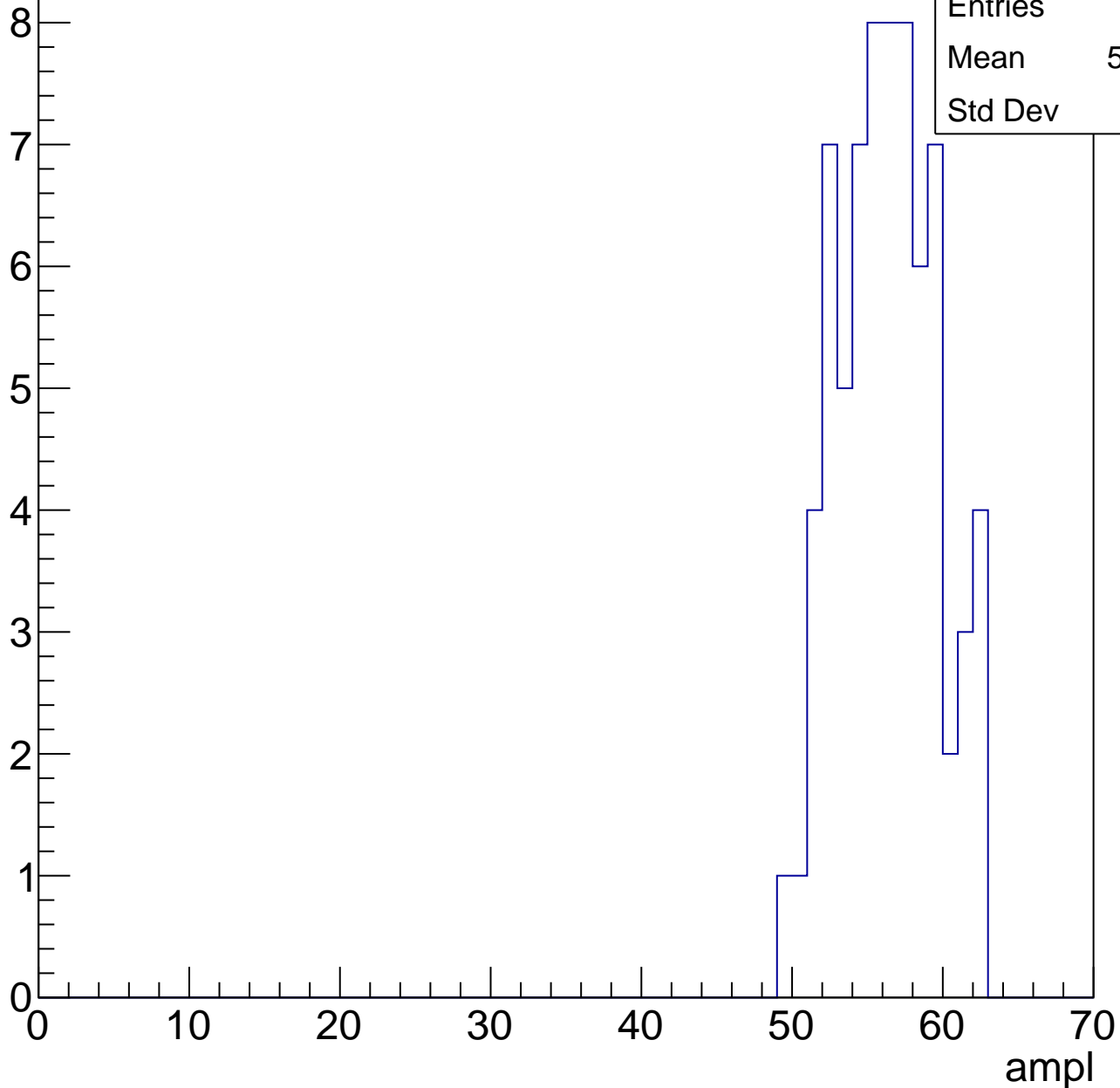
Entries	44
Mean	49.75
Std Dev	3.248



B1L103S, U11-ch25, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



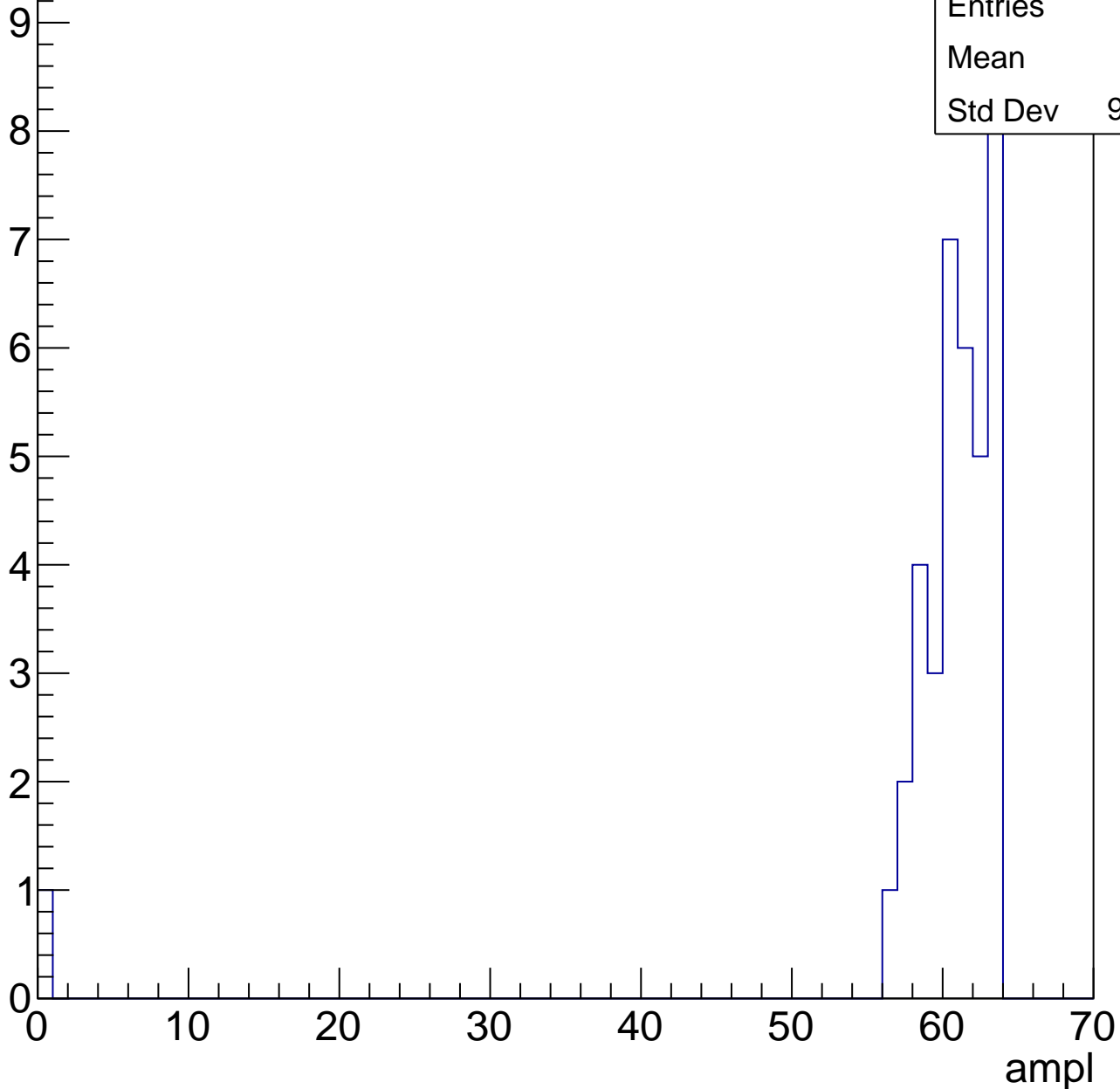
Entries	71
Mean	55.86
Std Dev	3.19

B1L103S, U11-ch25, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	38
Mean	59
Std Dev	9.897



B1L103S, U11-ch25, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

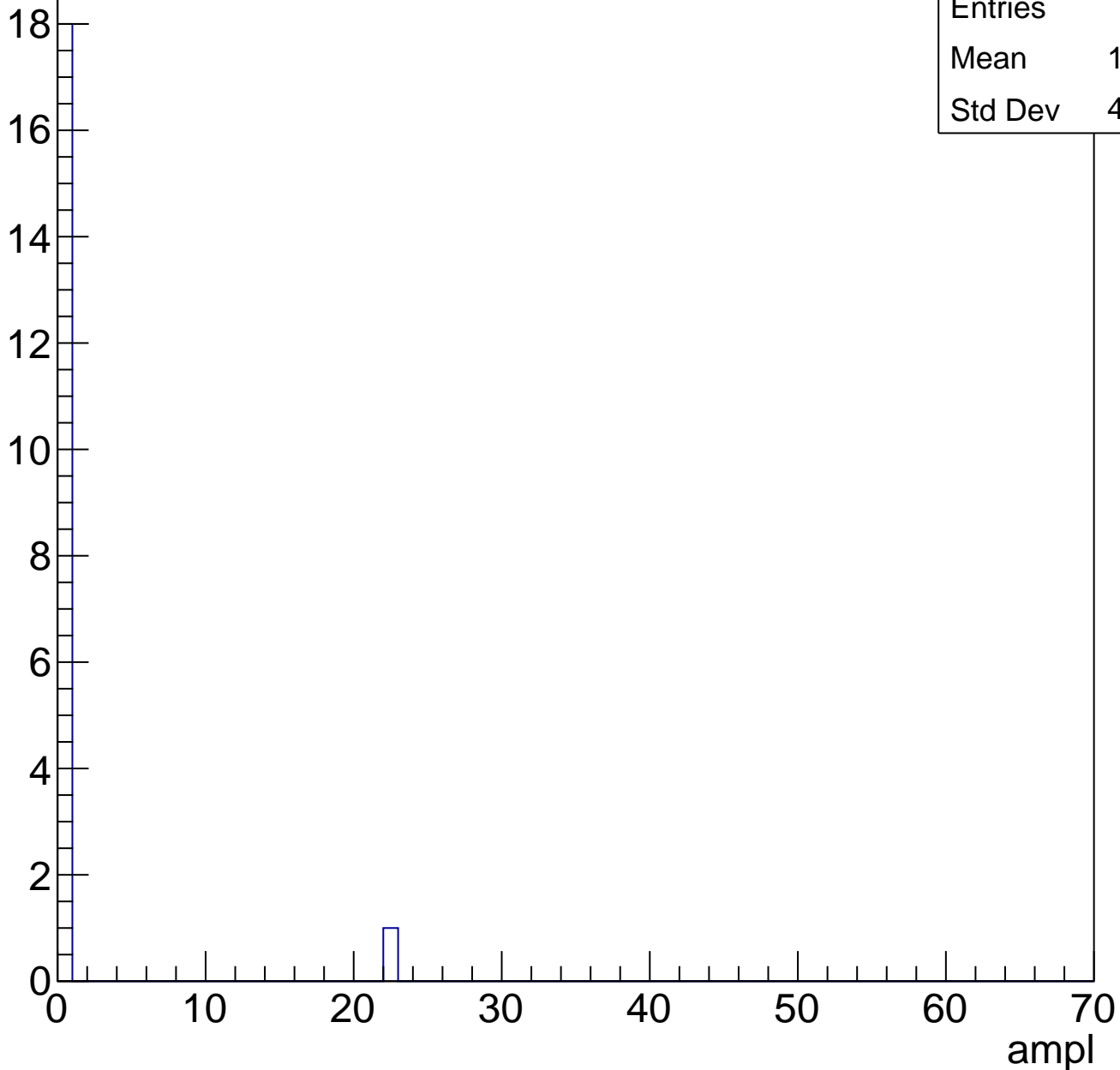


B1L103S, U11-ch25, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.158
Std Dev	4.913

Entry

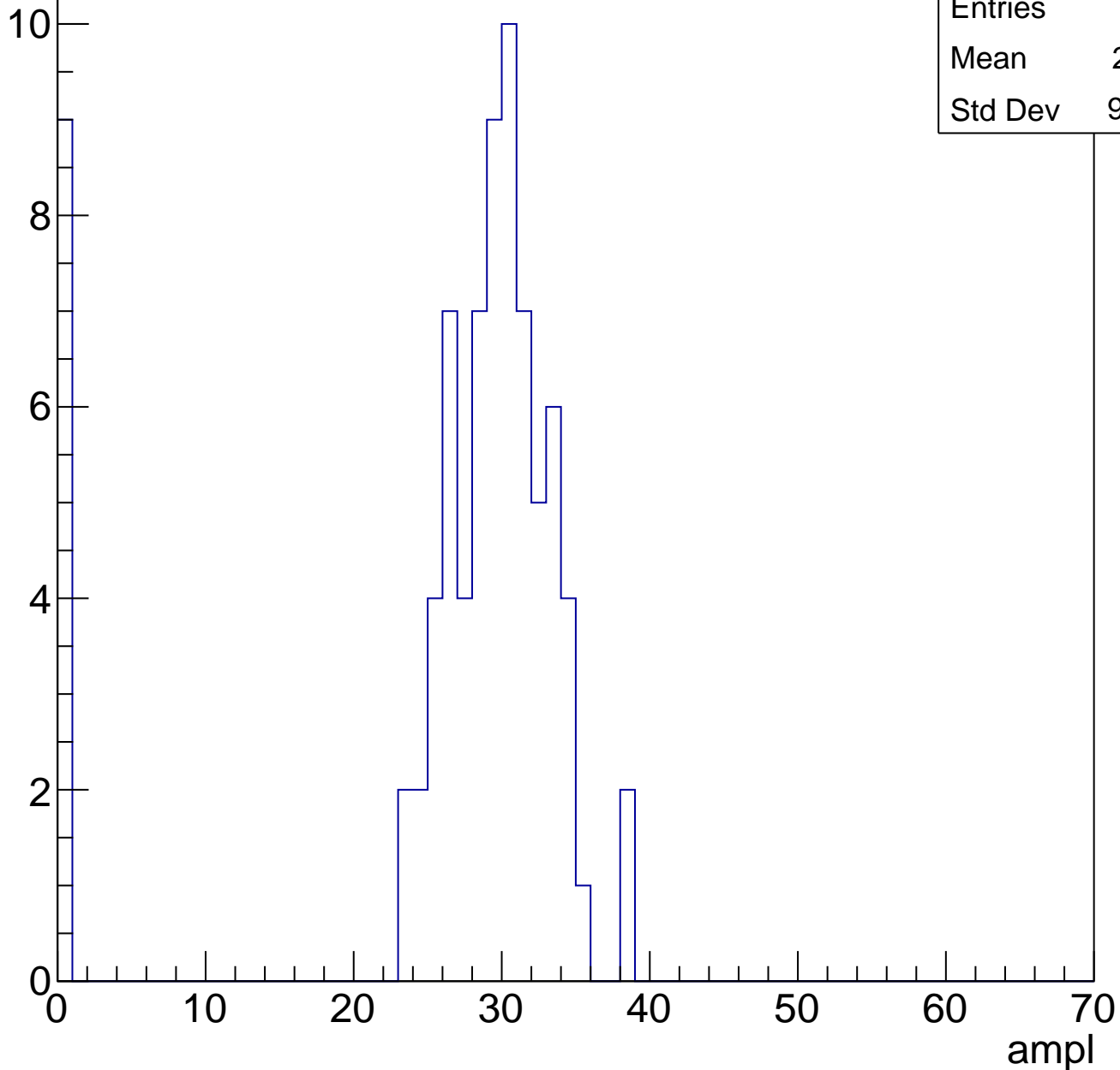


B1L103S, U11-ch26, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	79
Mean	26.11
Std Dev	9.847

Entry

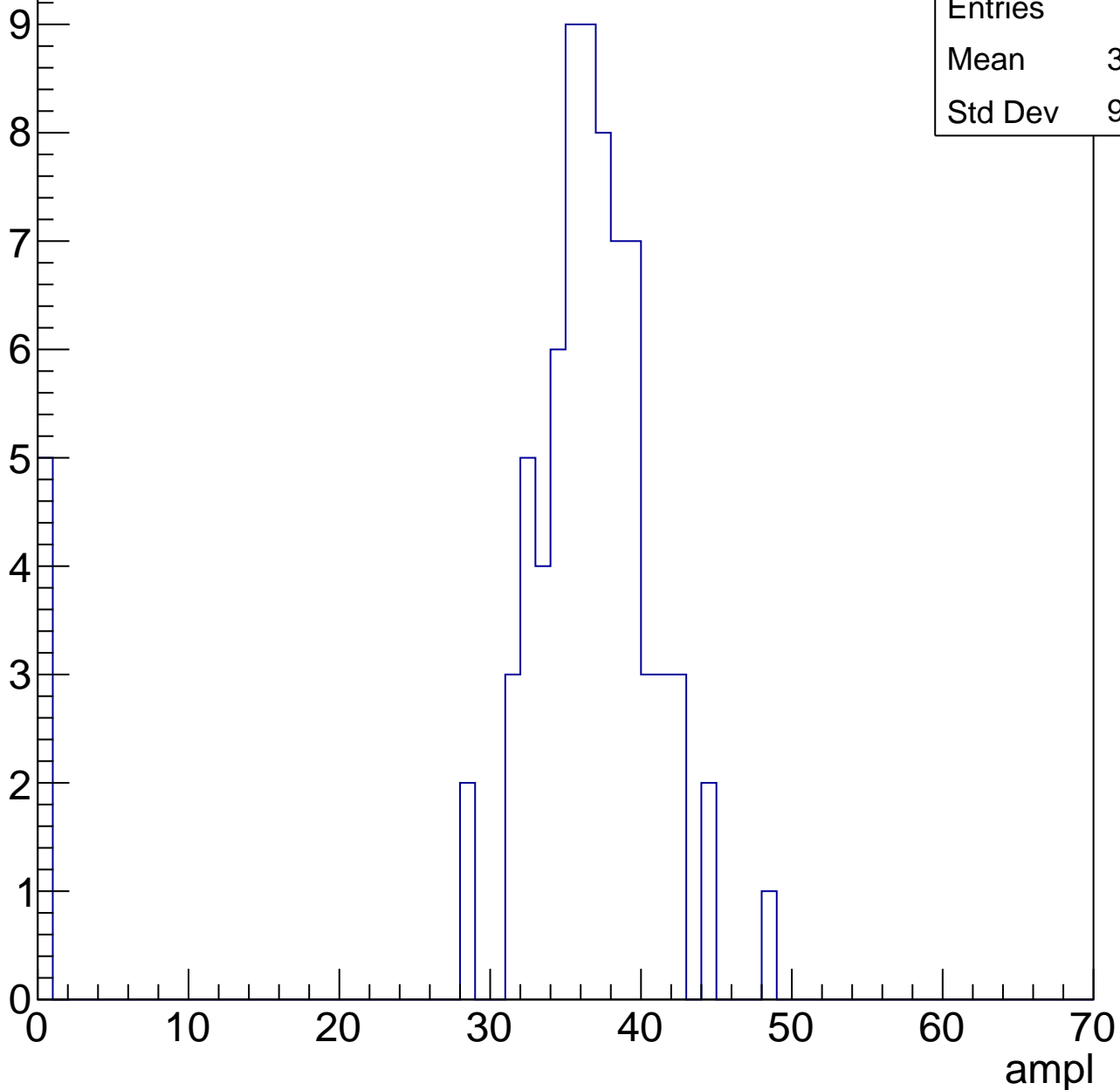


B1L103S, U11-ch26, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

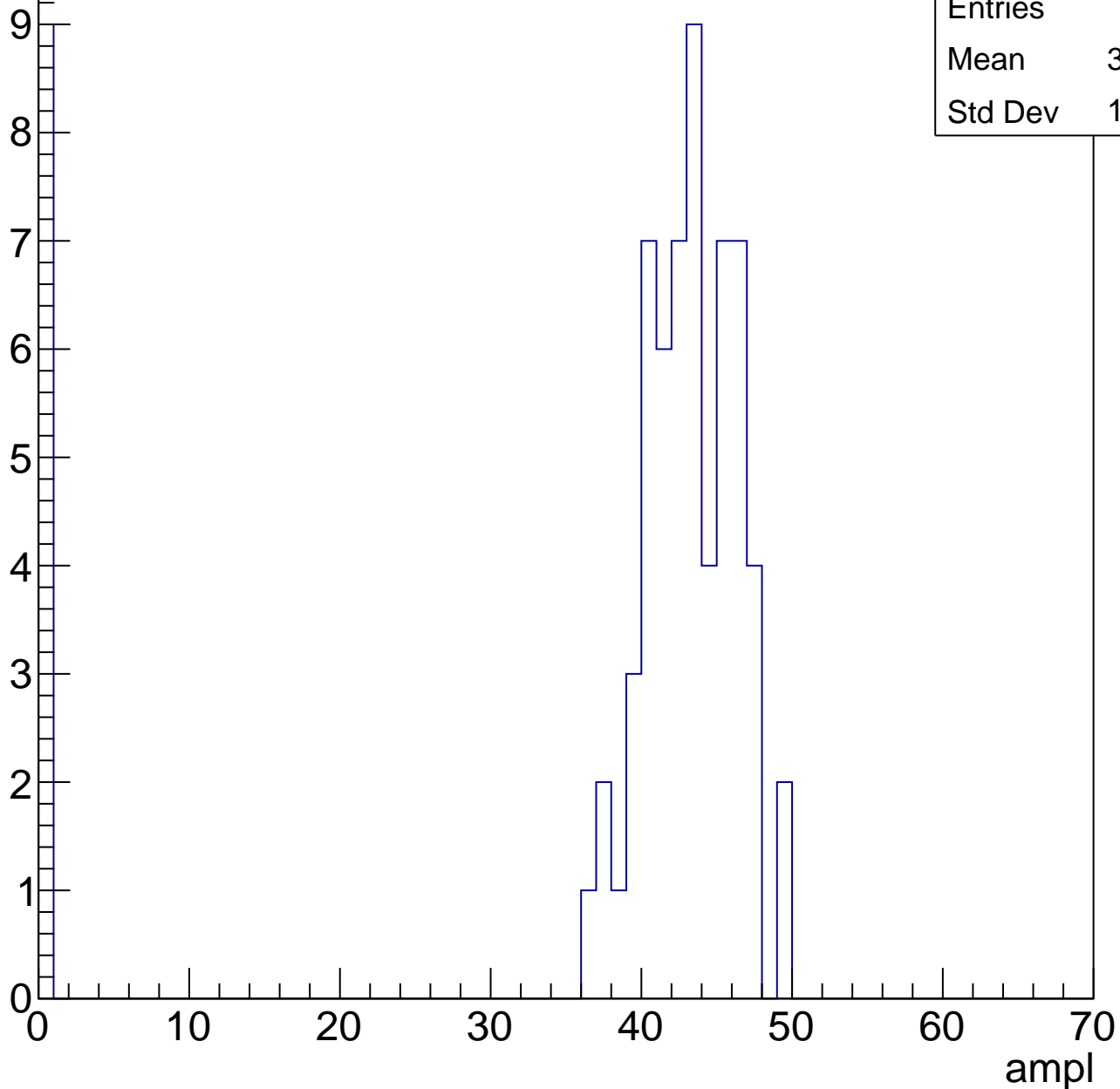
Entries	77
Mean	34.08
Std Dev	9.636



B1L103S, U11-ch26, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

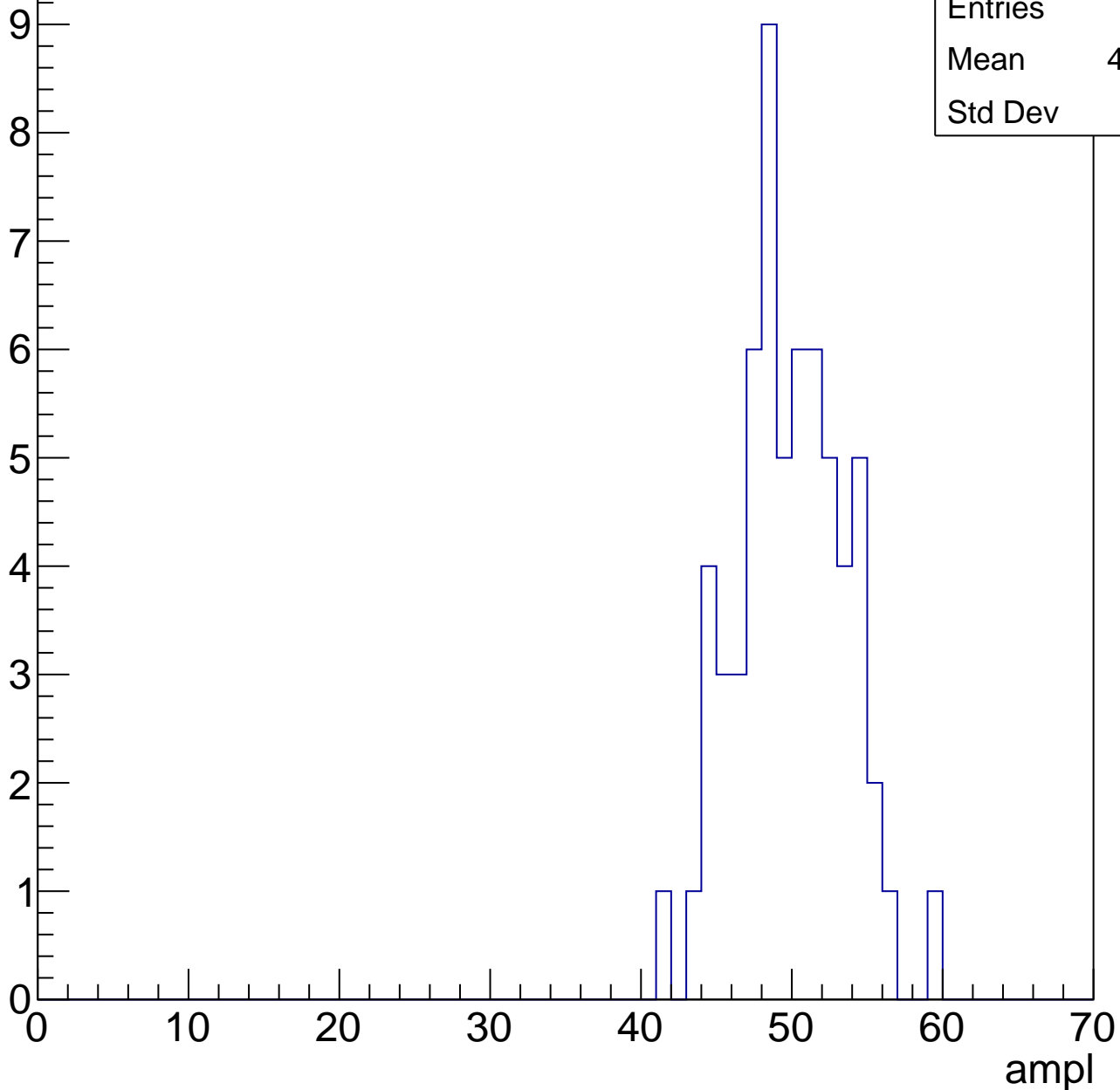


B1L103S, U11-ch26, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	49.44
Std Dev	3.55

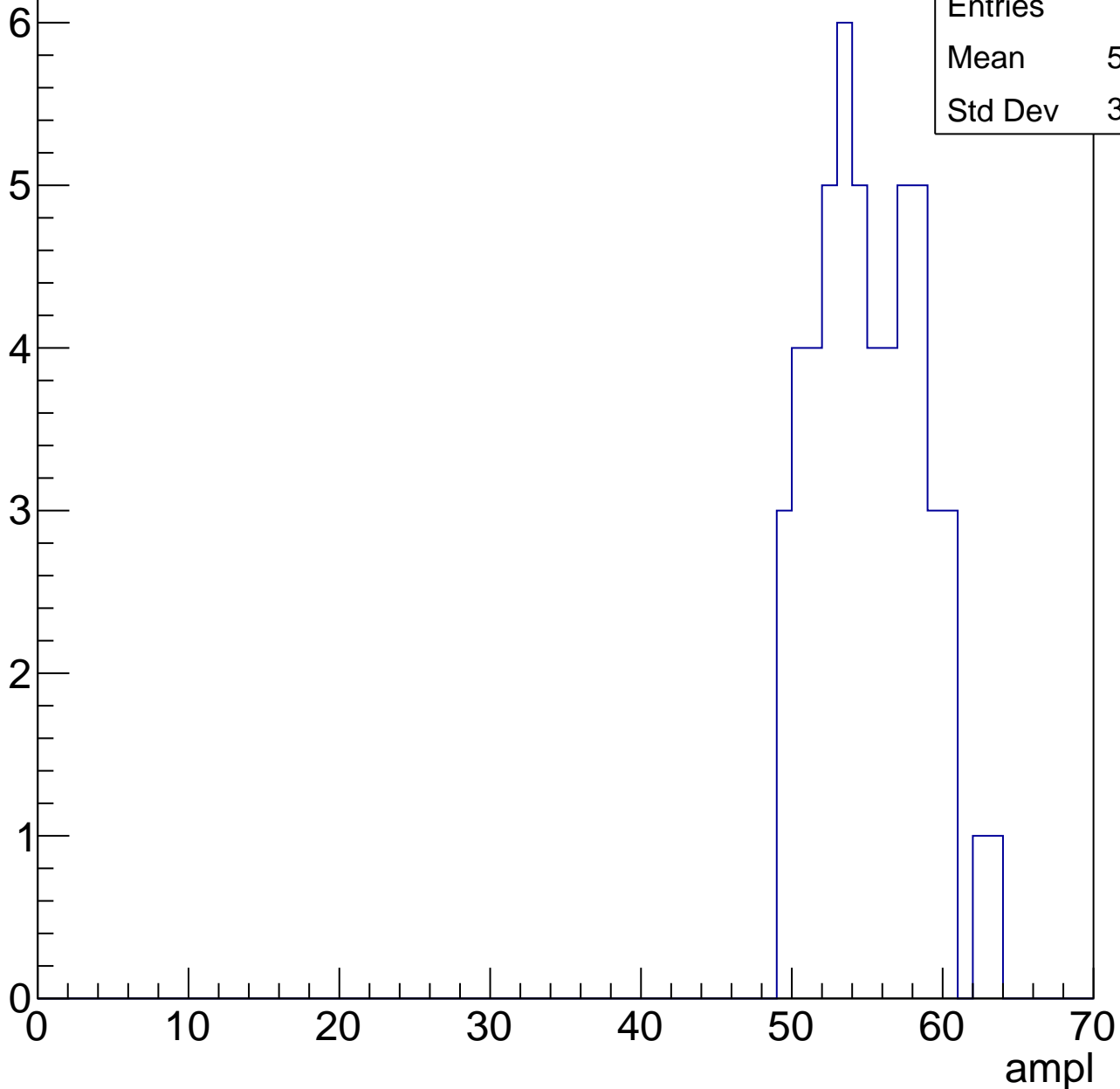


B1L103S, U11-ch26, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

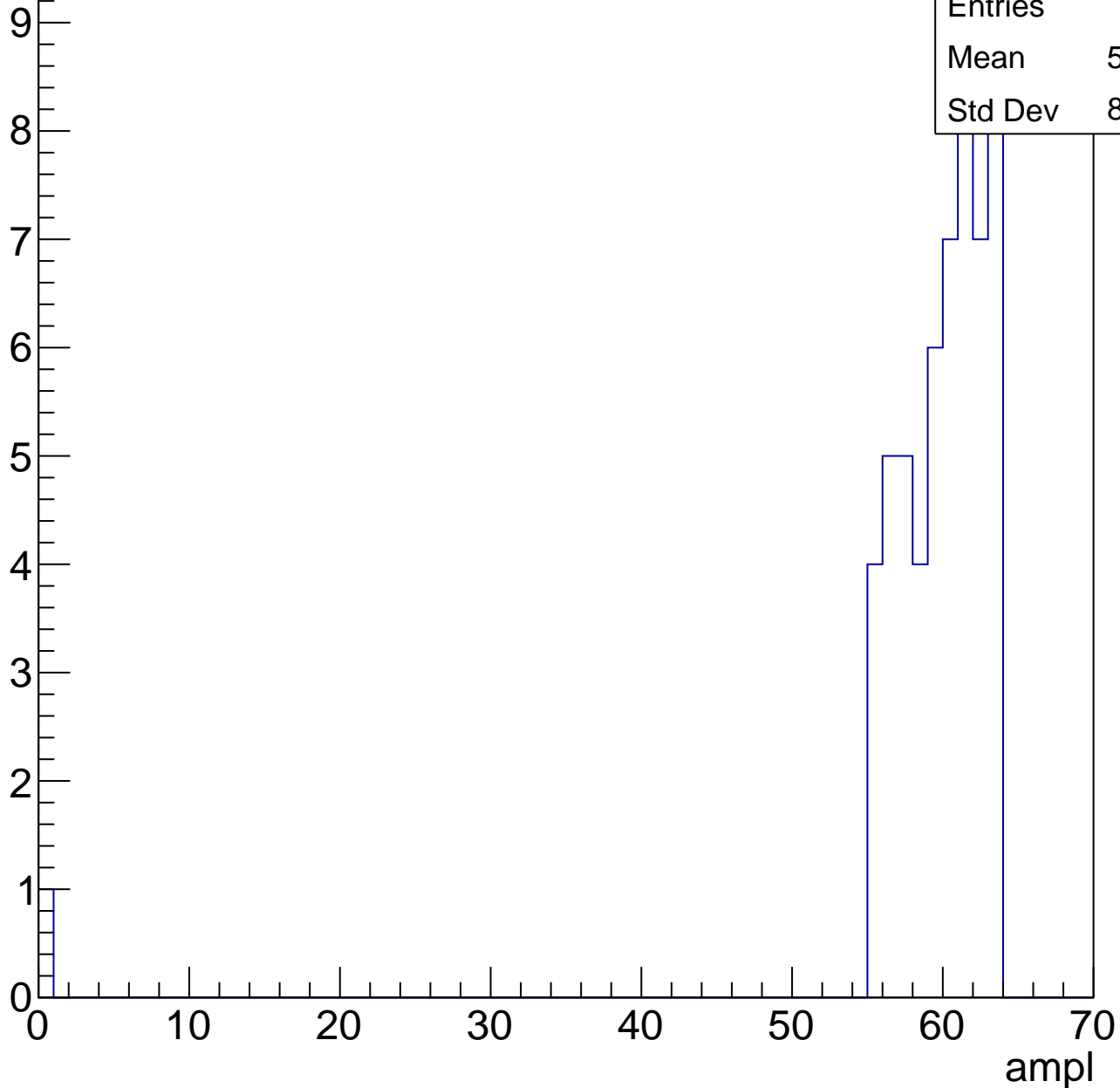
Entries	53
Mean	54.72
Std Dev	3.493



B1L103S, U11-ch26, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

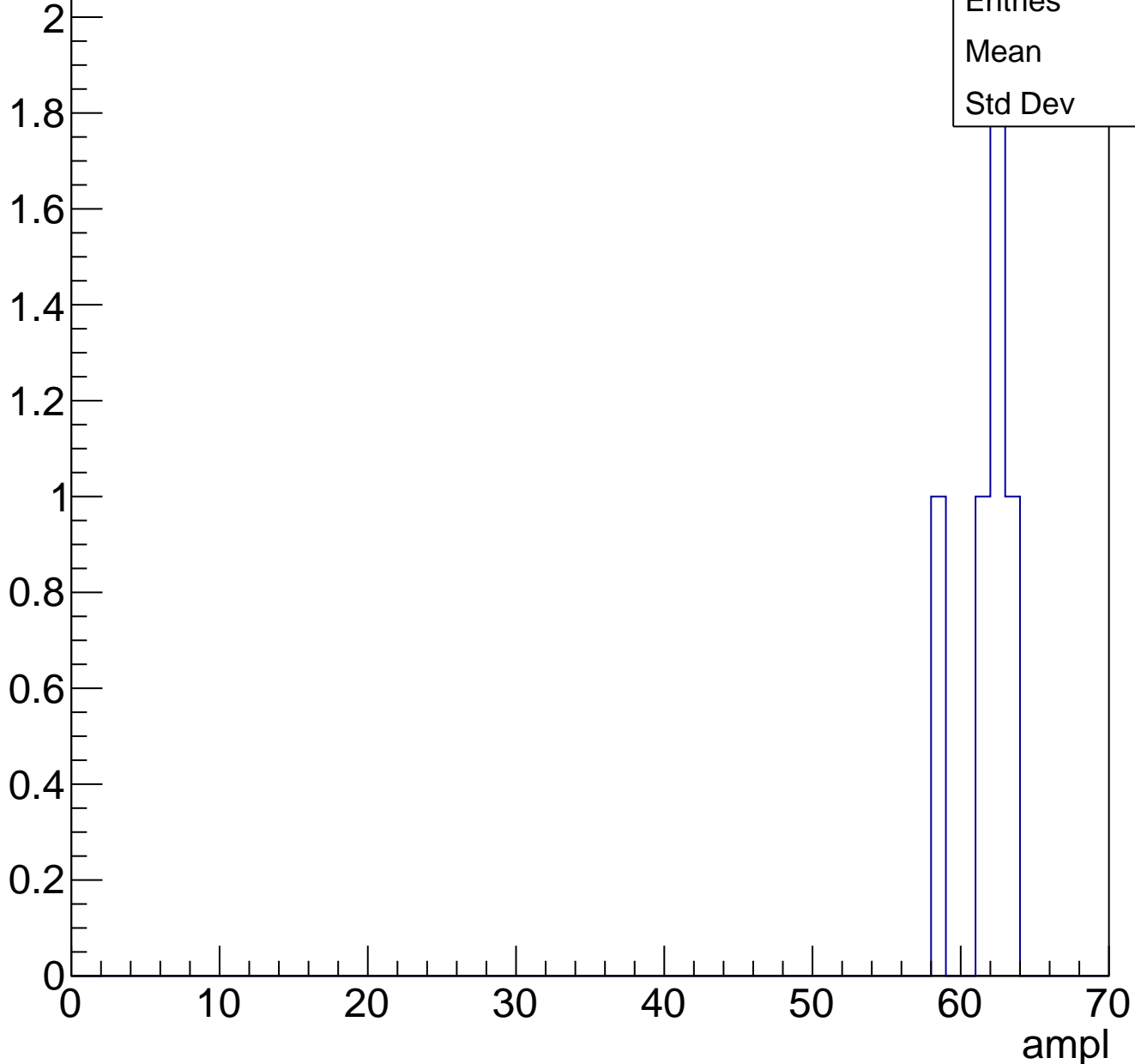


Entries	56
Mean	58.54
Std Dev	8.276

B1L103S, U11-ch26, adc6

calib_packv5_041523_1651.root, FC#0, port C2

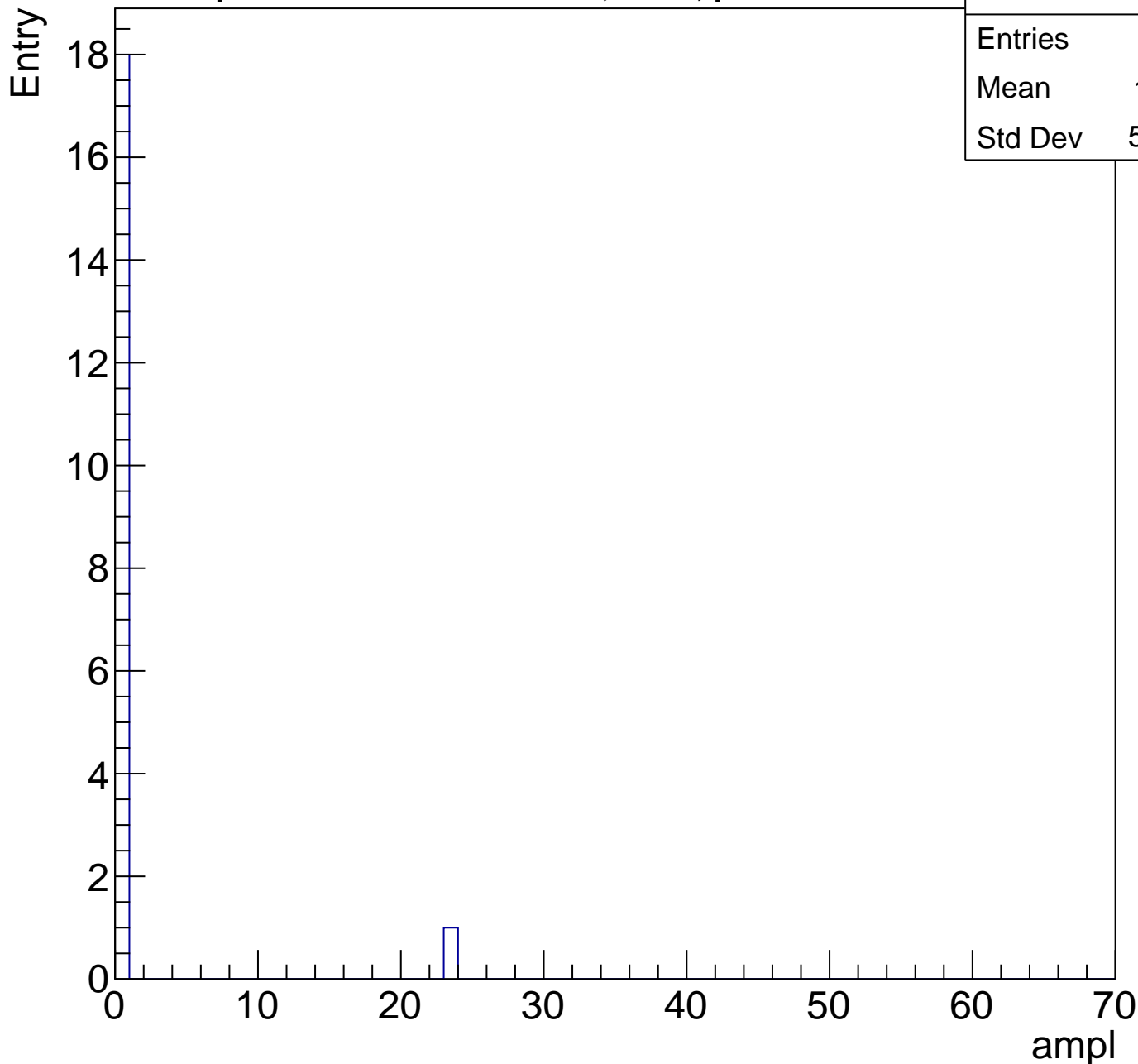
Entry



B1L103S, U11-ch26, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.211
Std Dev	5.136

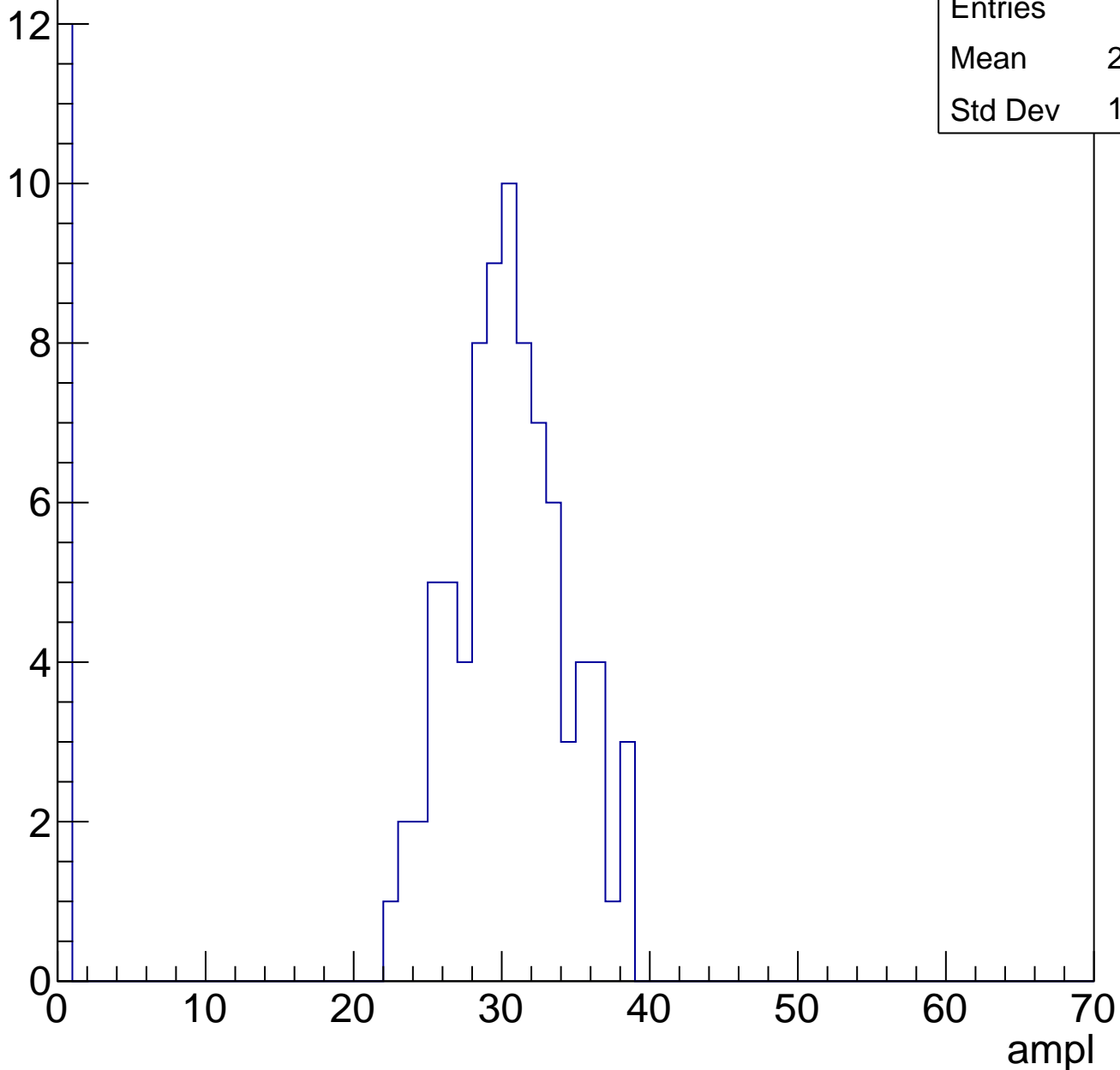


B1L103S, U11-ch27, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	94
Mean	26.29
Std Dev	10.64

Entry

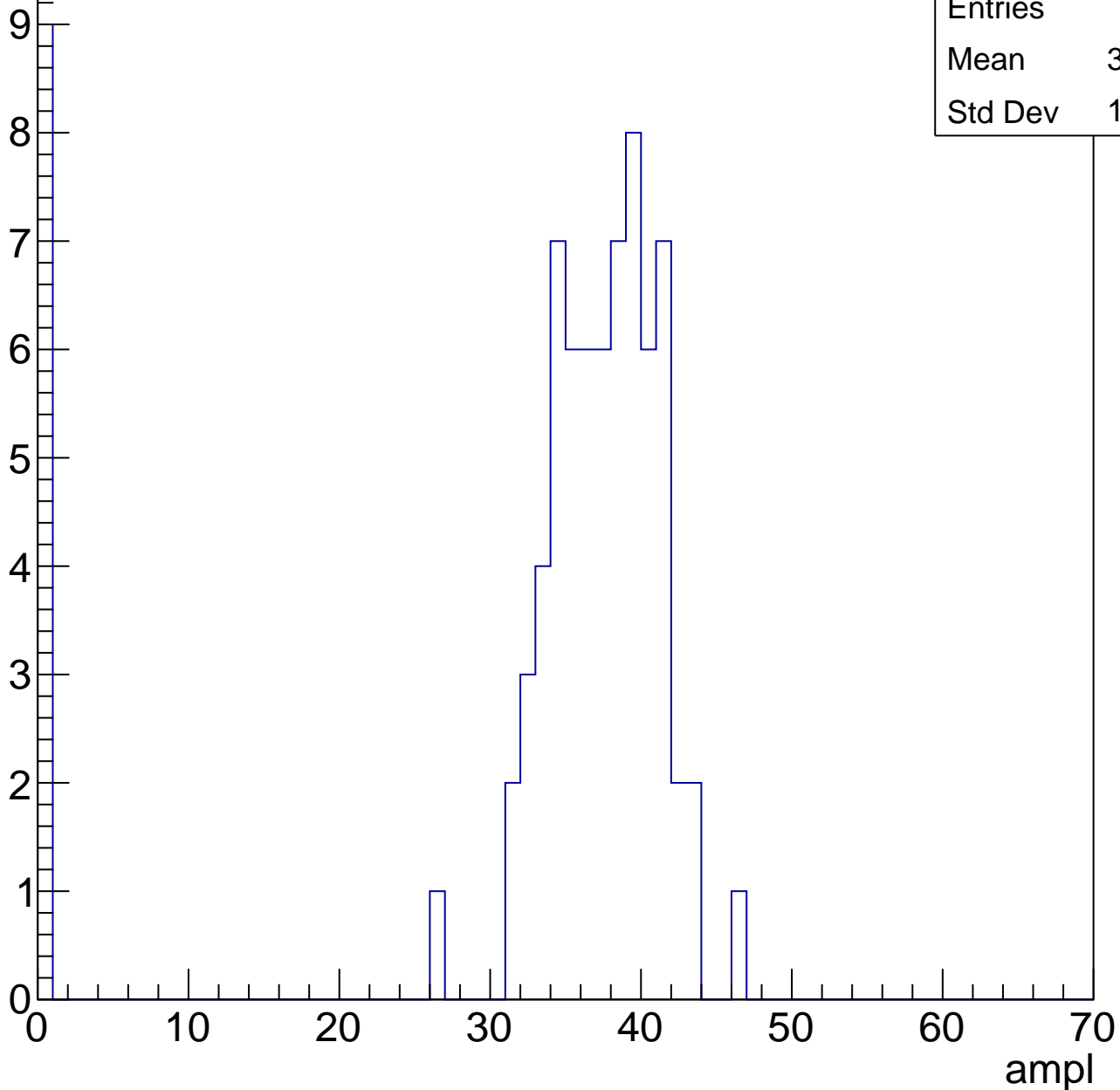


B1L103S, U11-ch27, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	32.77
Std Dev	12.37

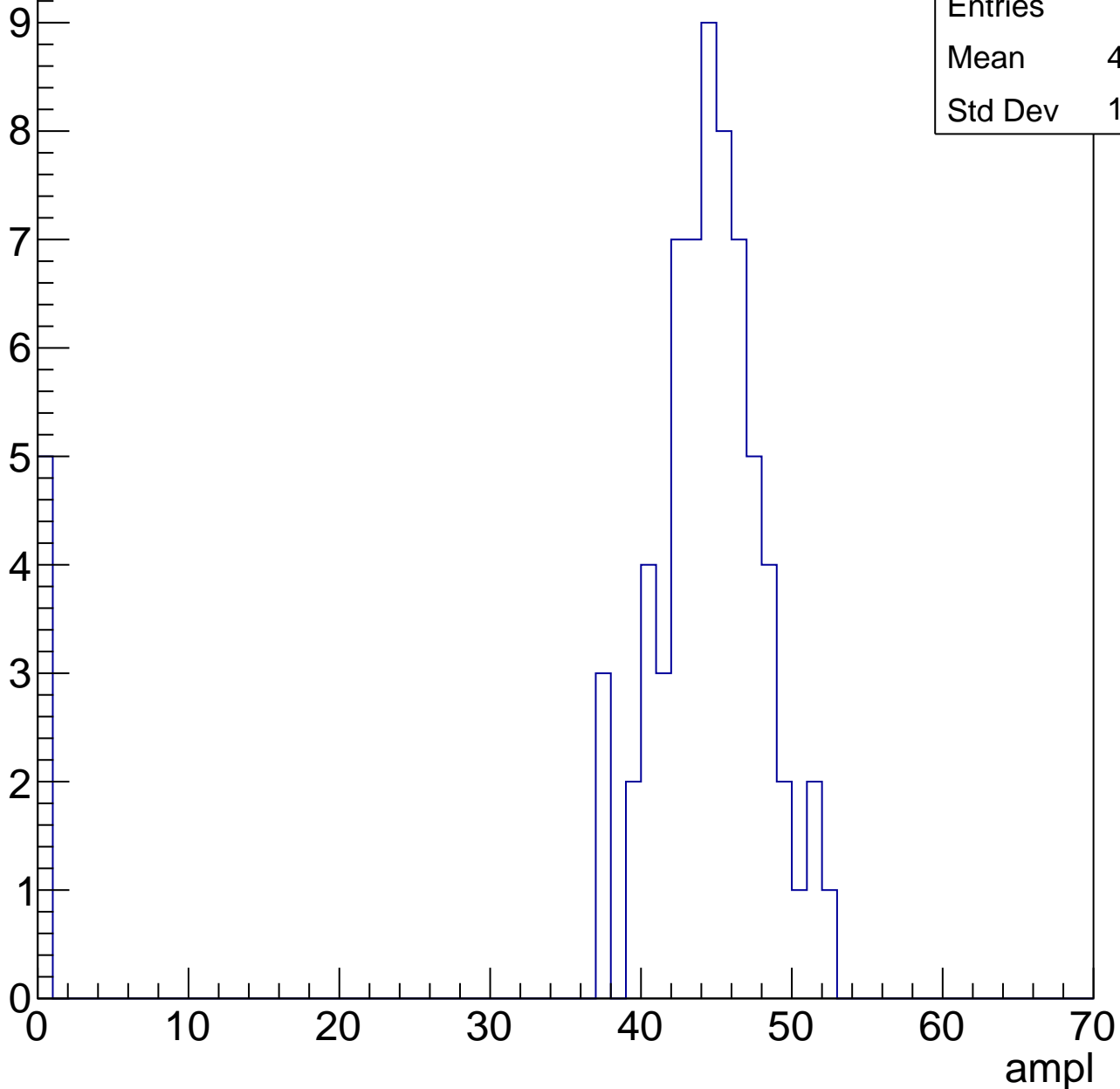


B1L103S, U11-ch27, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	41.06
Std Dev	11.83

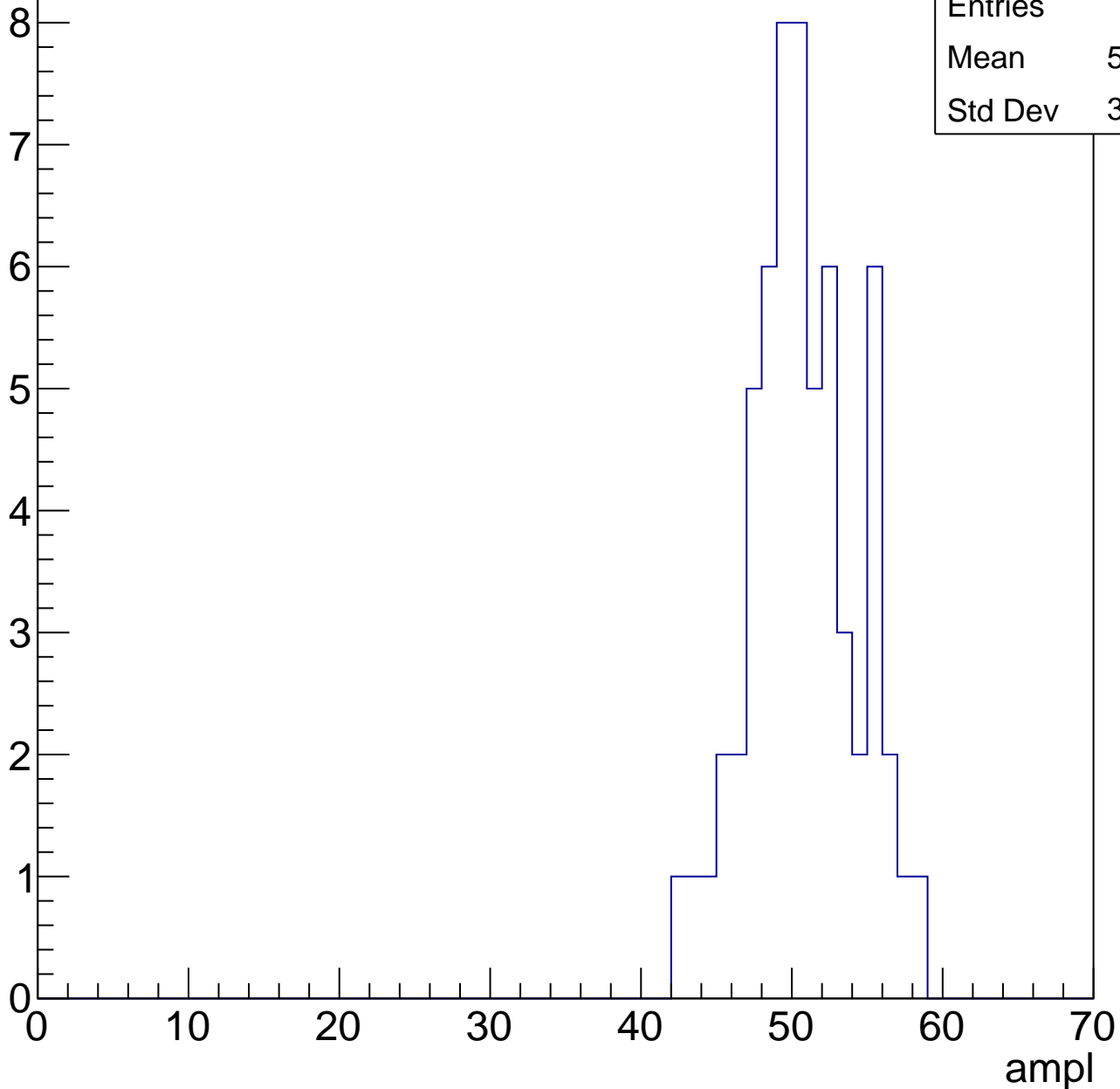


B1L103S, U11-ch27, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	50.28
Std Dev	3.479

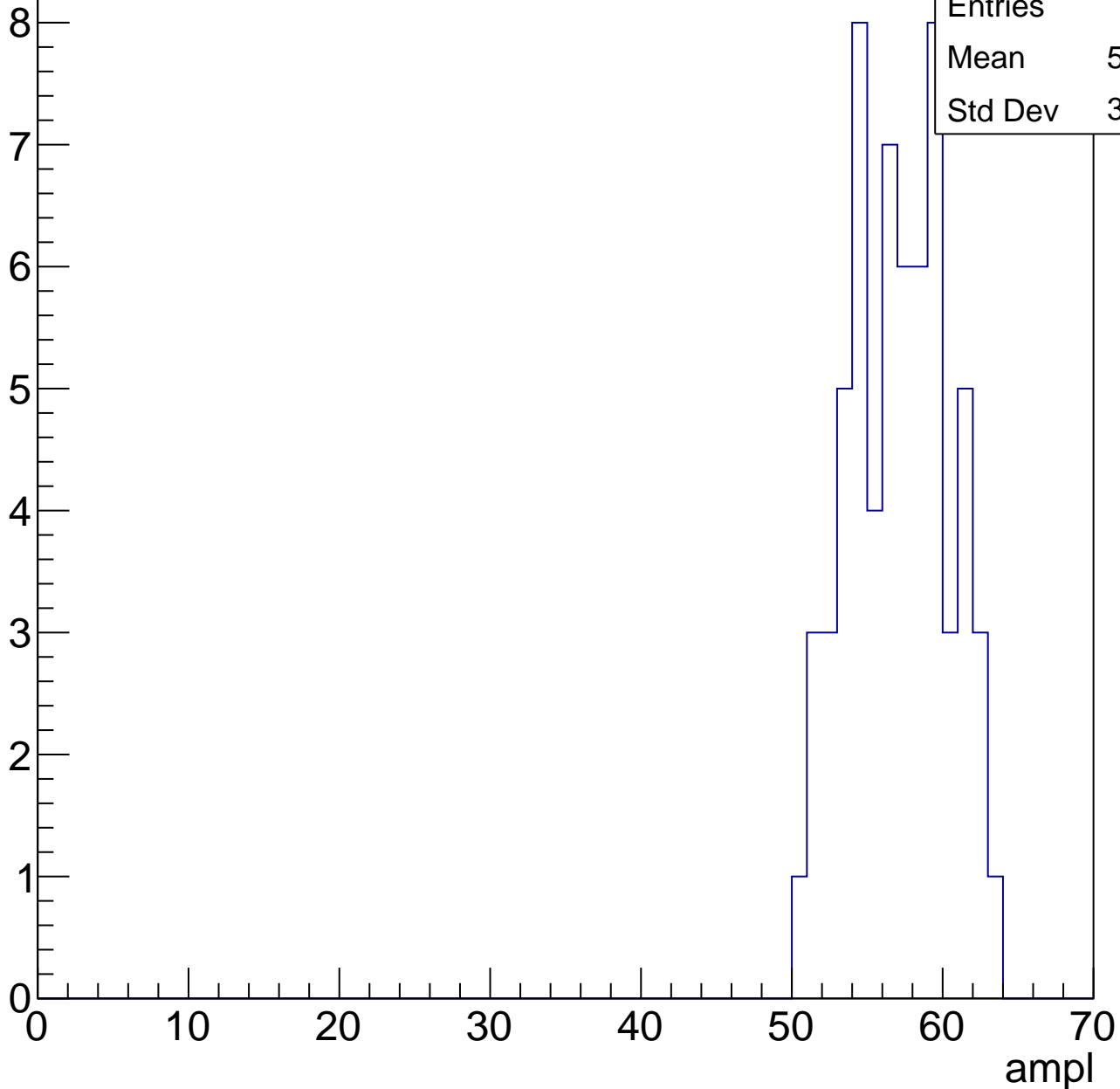


B1L103S, U11-ch27, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	56.57
Std Dev	3.216

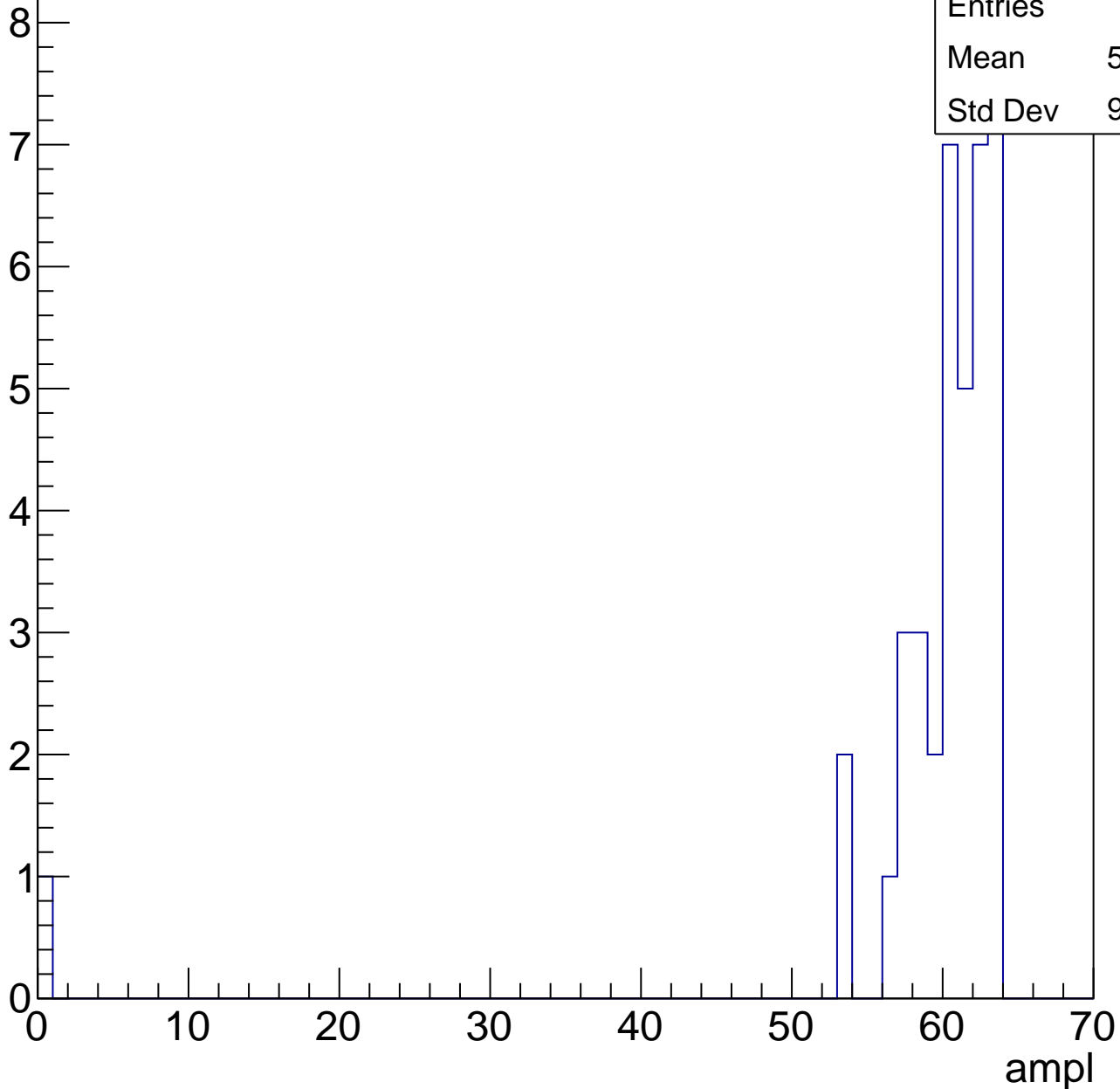


B1L103S, U11-ch27, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	58.67
Std Dev	9.859



B1L103S, U11-ch27, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch27, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

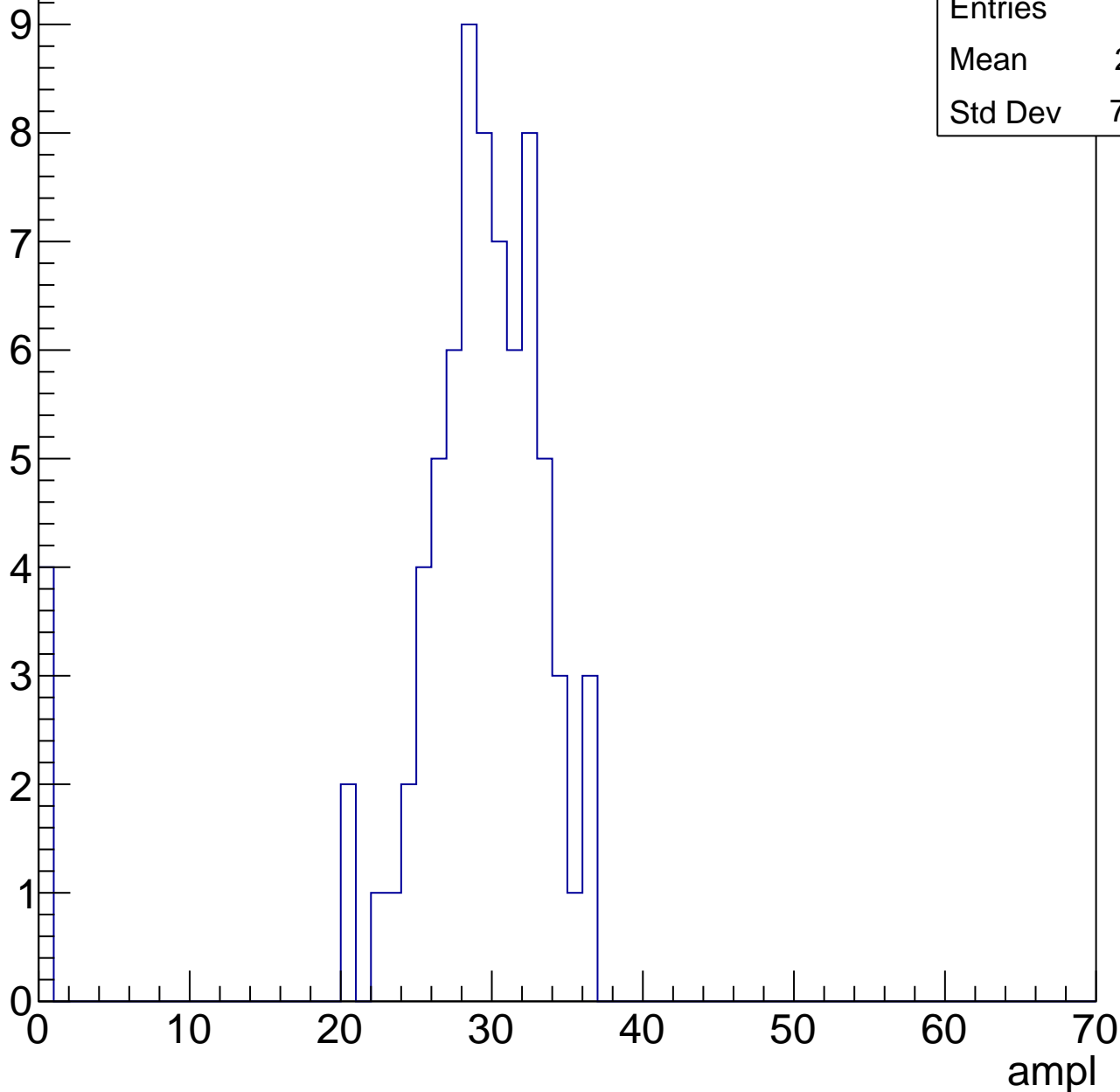
ampl

B1L103S, U11-ch28, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	27.61
Std Dev	7.393

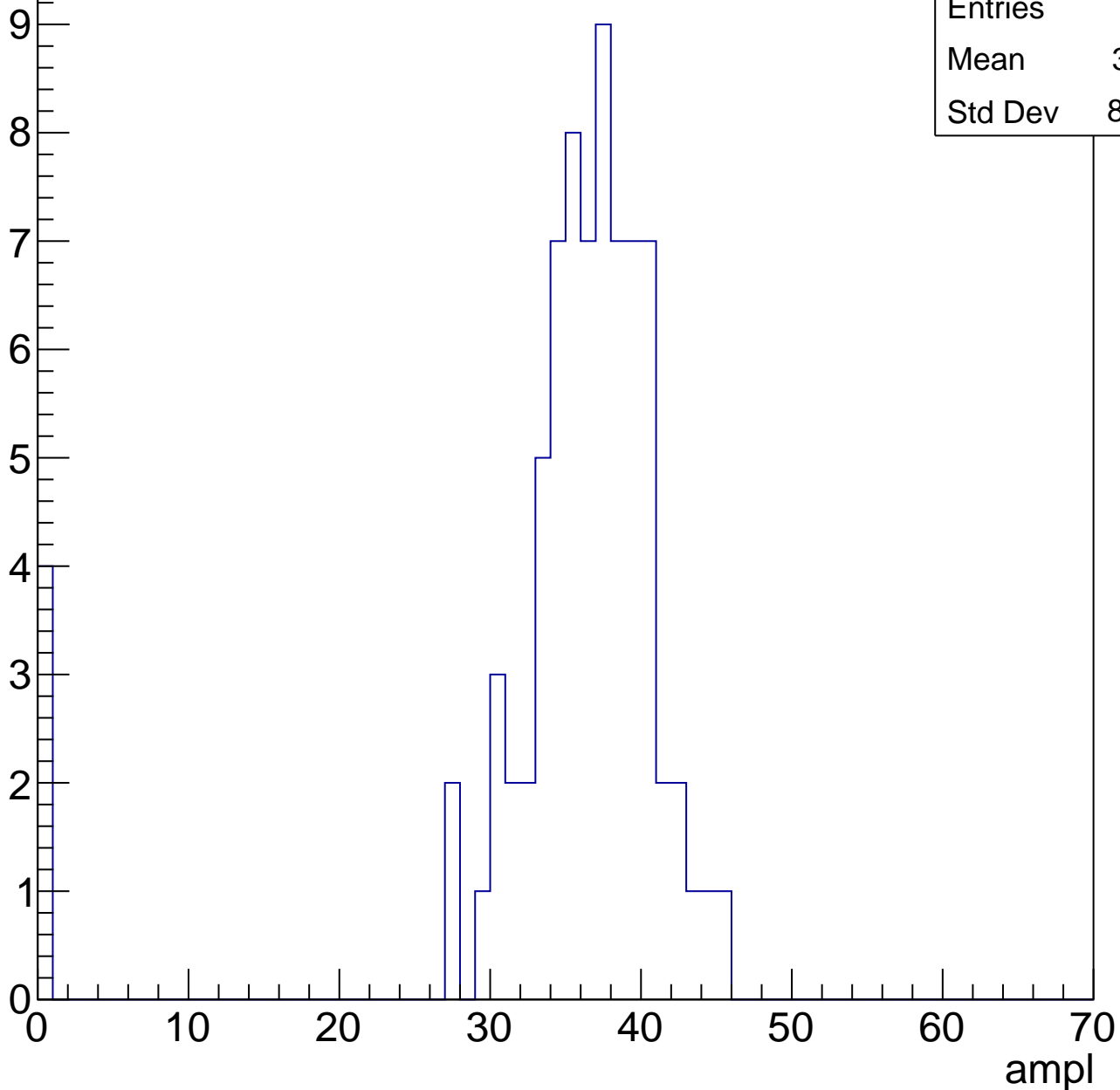


B1L103S, U11-ch28, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	34.41
Std Dev	8.768

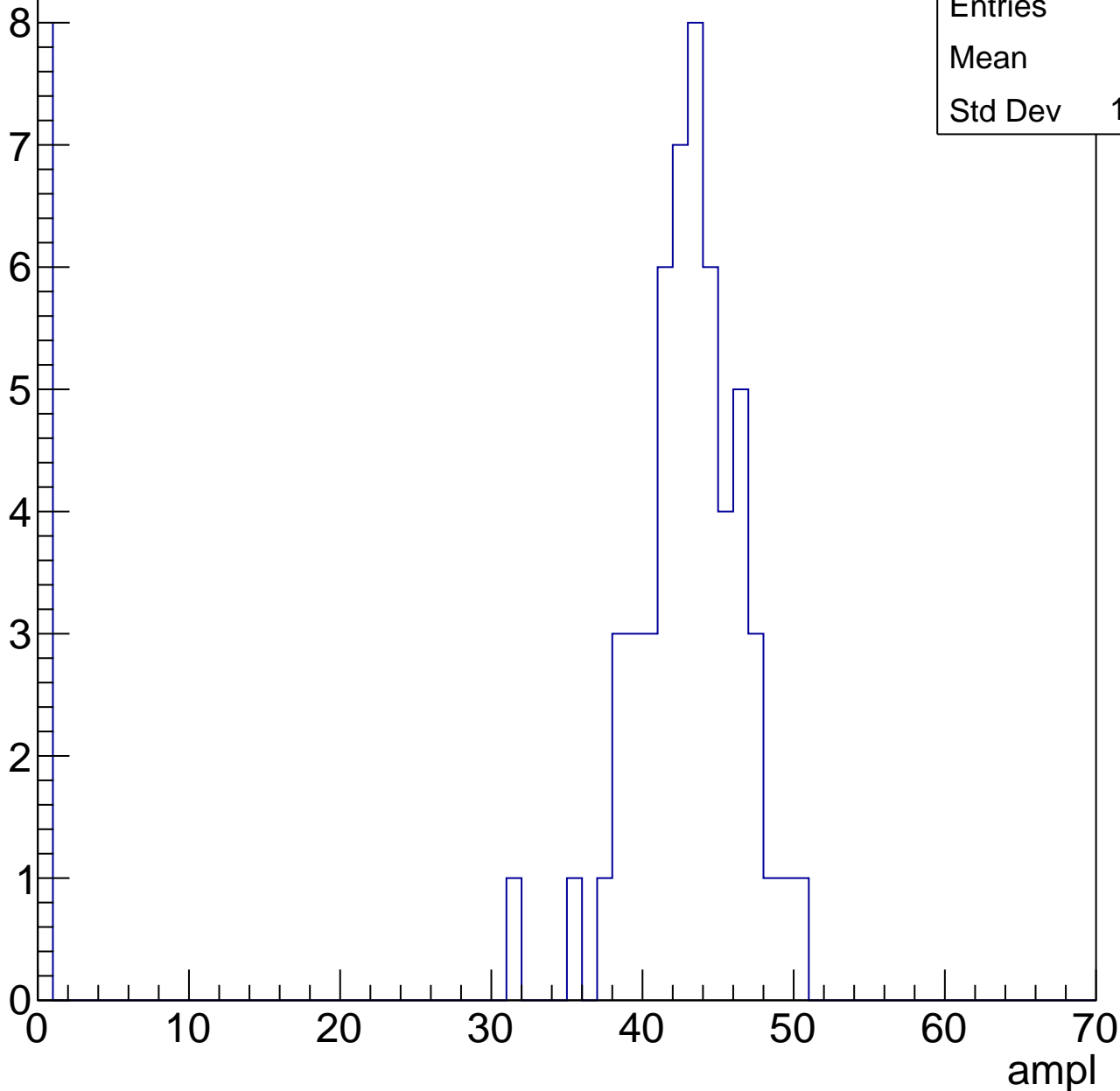


B1L103S, U11-ch28, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	37.1
Std Dev	14.64

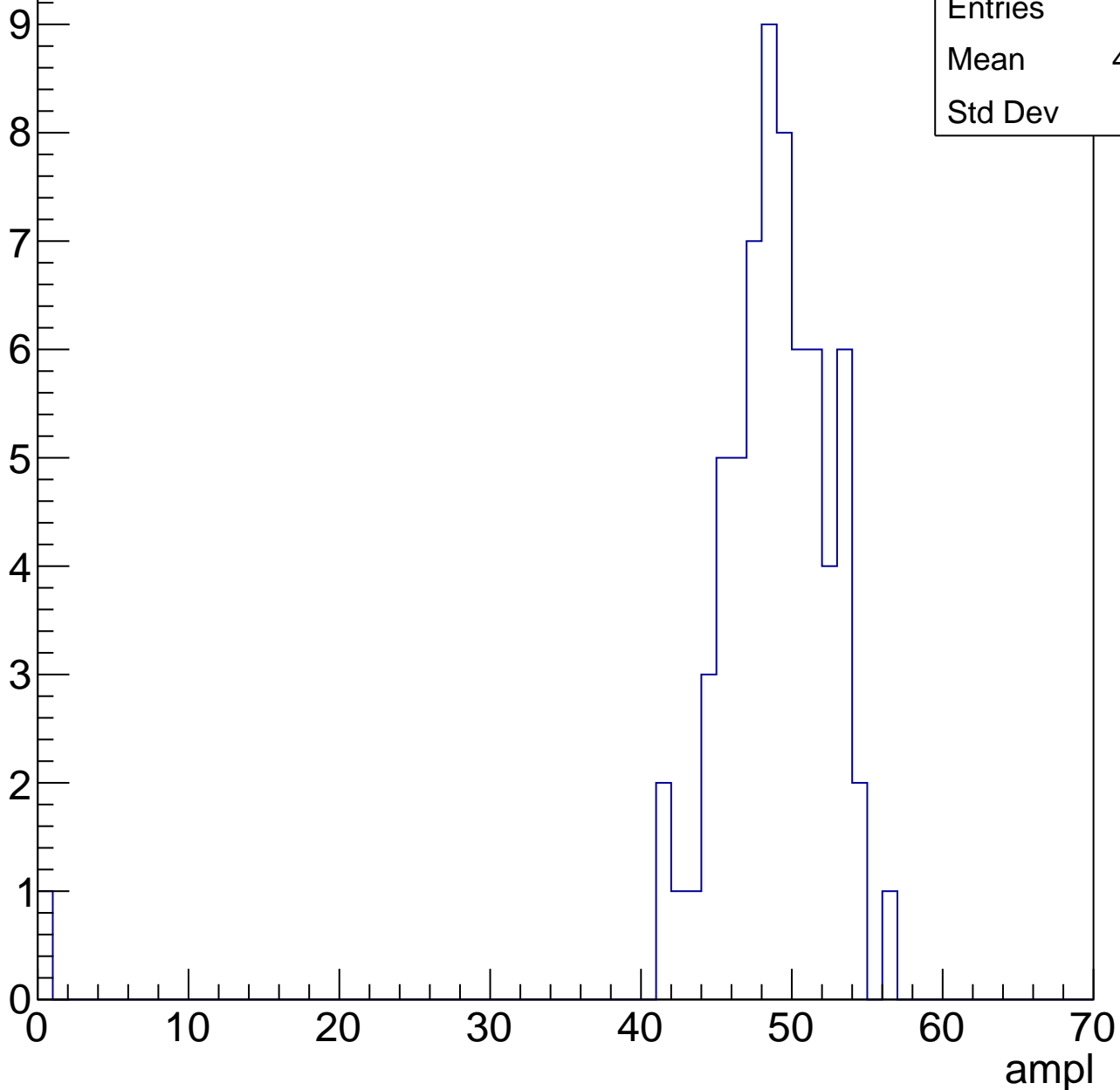


B1L103S, U11-ch28, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

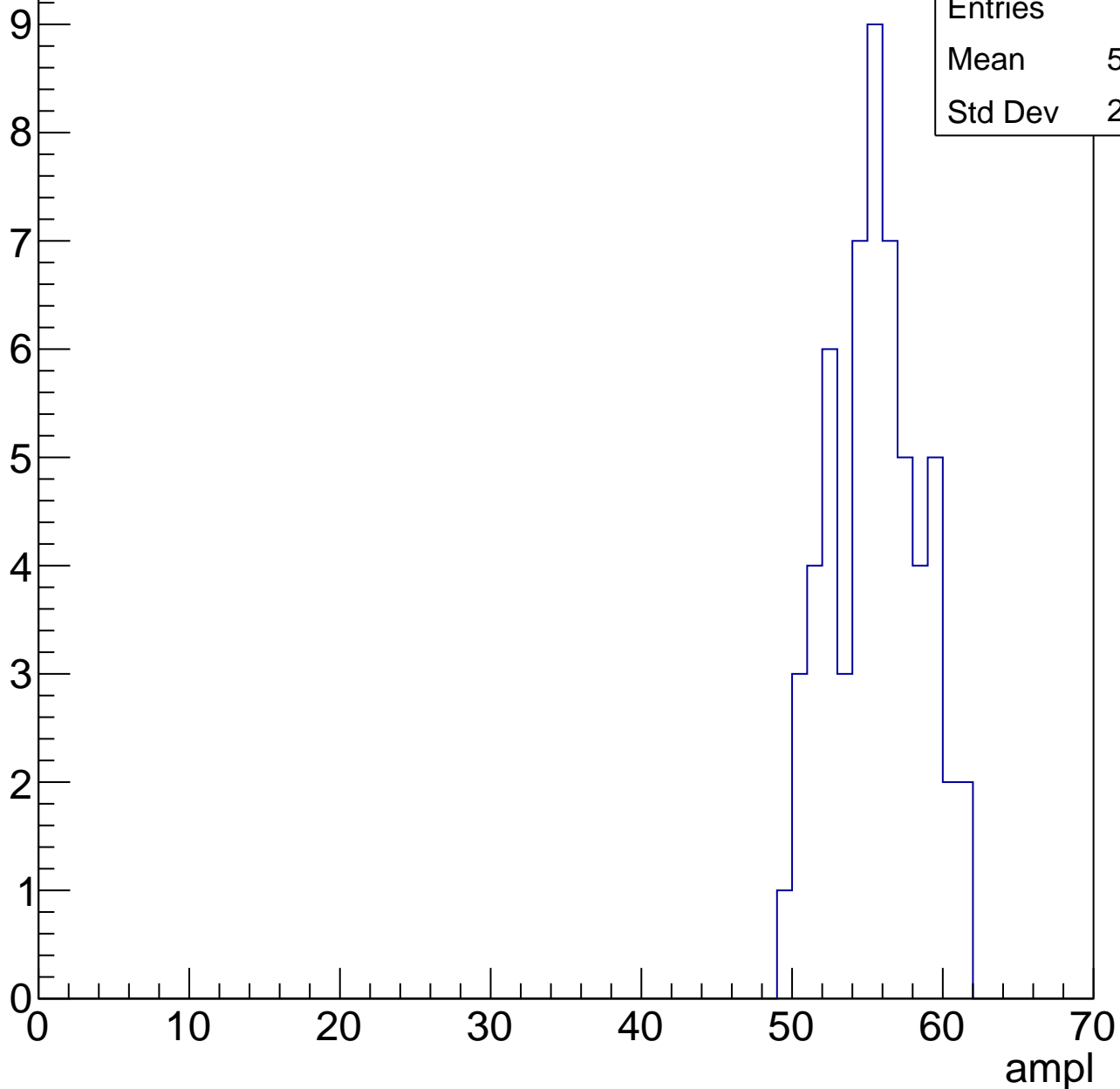
Entries	67
Mean	47.81
Std Dev	6.71



B1L103S, U11-ch28, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



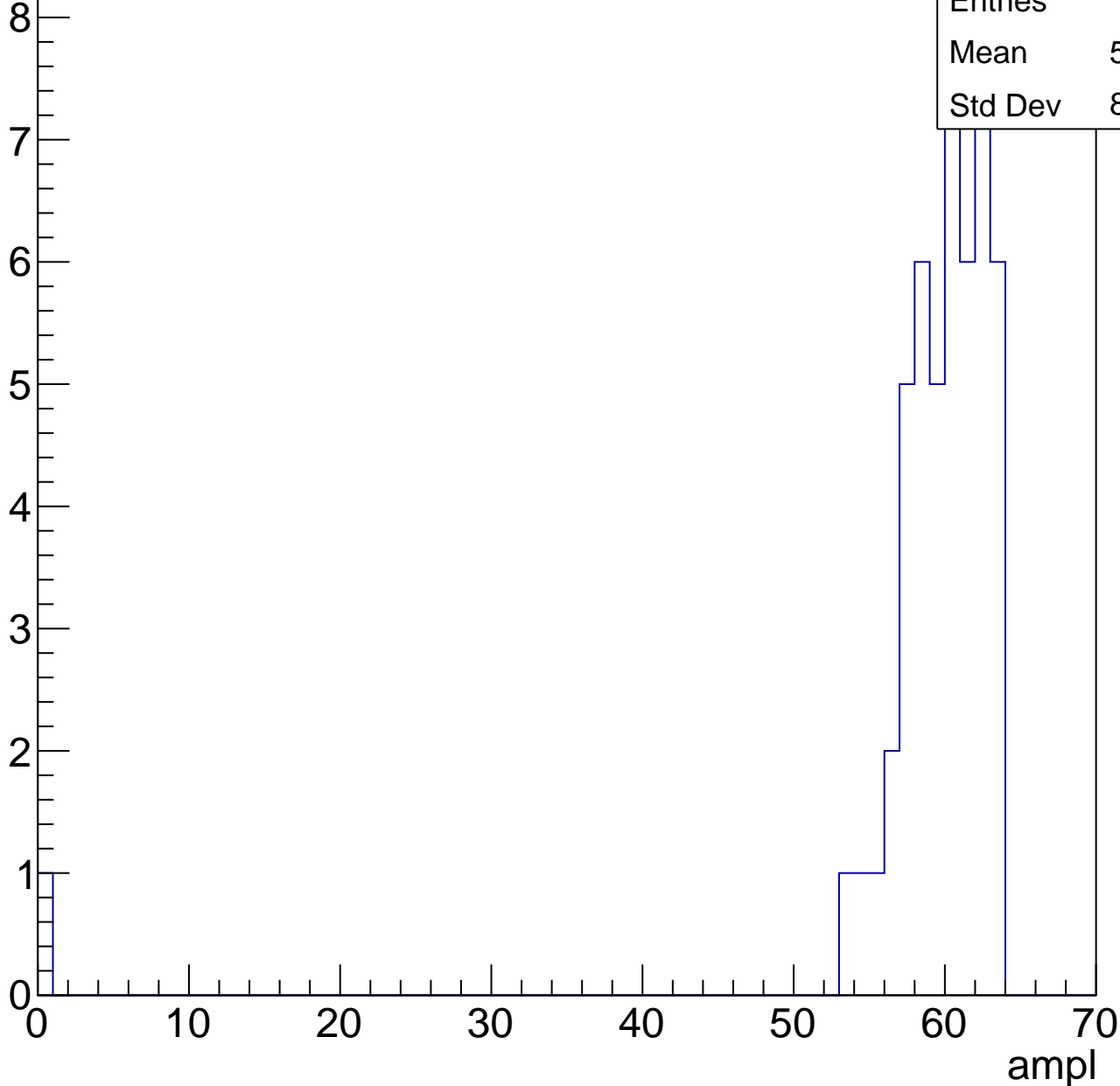
Entries	58
Mean	55.05
Std Dev	2.974

B1L103S, U11-ch28, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	58.44
Std Dev	8.702



B1L103S, U11-ch28, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch28, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

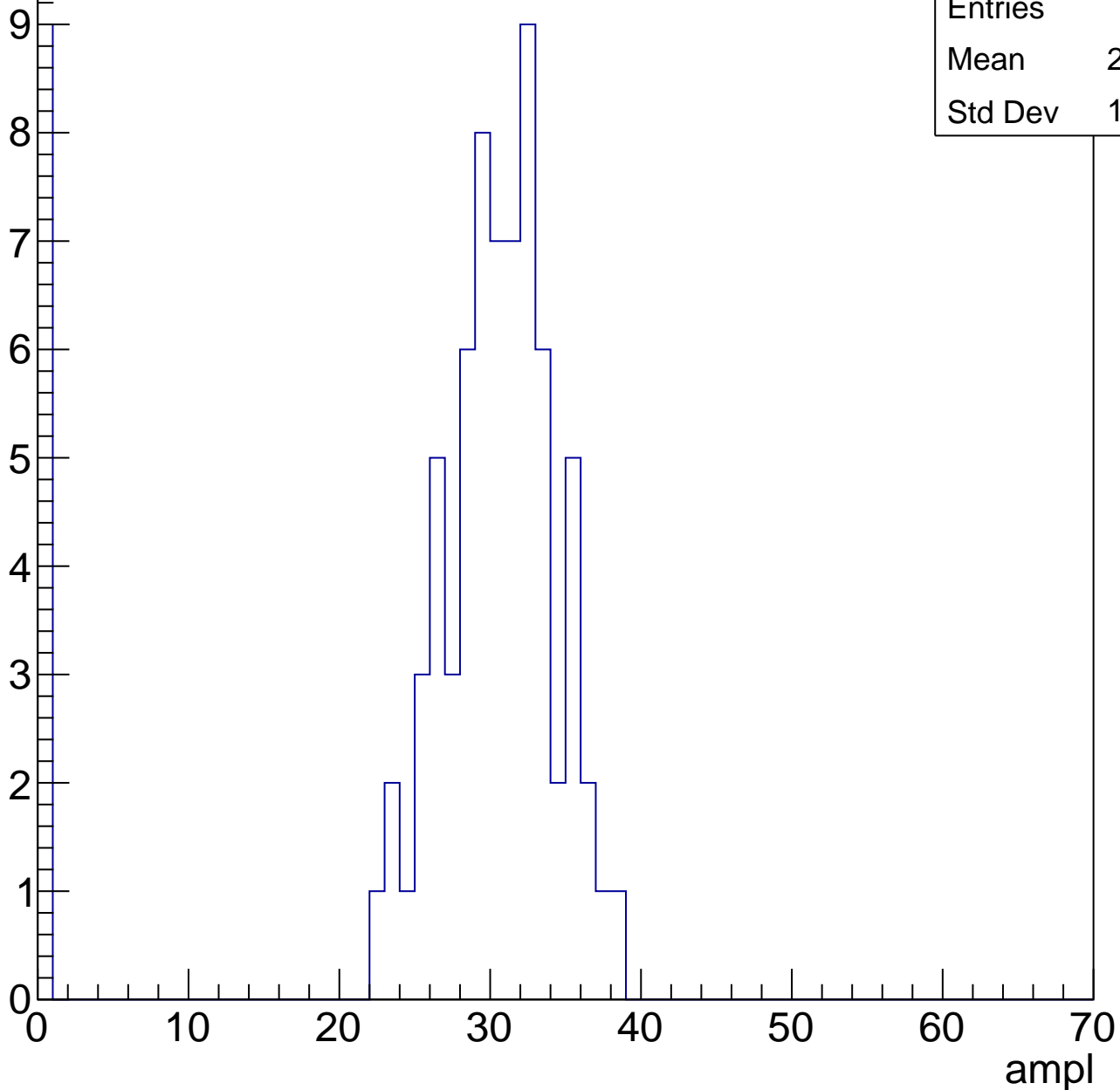


B1L103S, U11-ch29, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	26.68
Std Dev	10.18

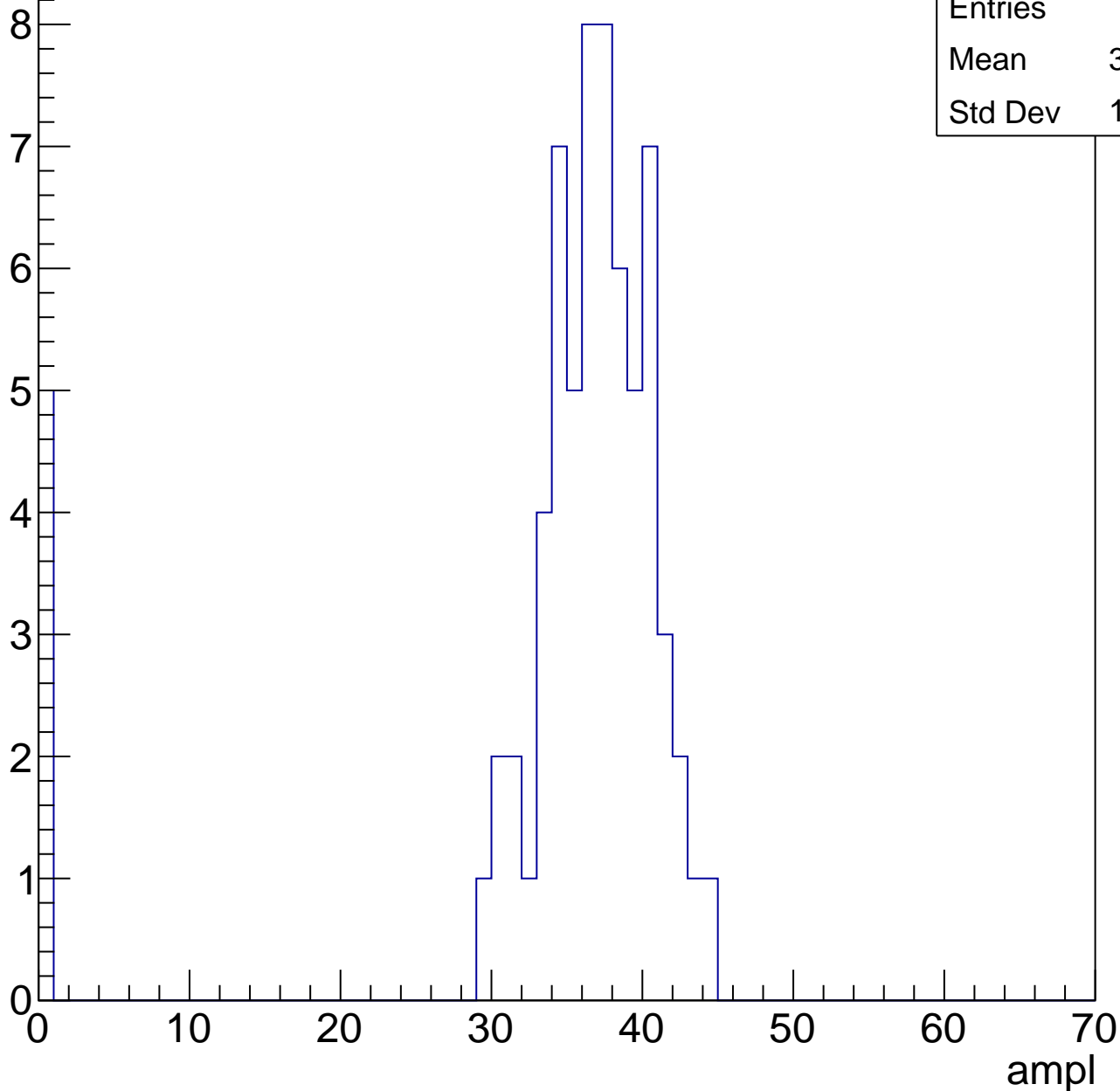


B1L103S, U11-ch29, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	33.96
Std Dev	10.07

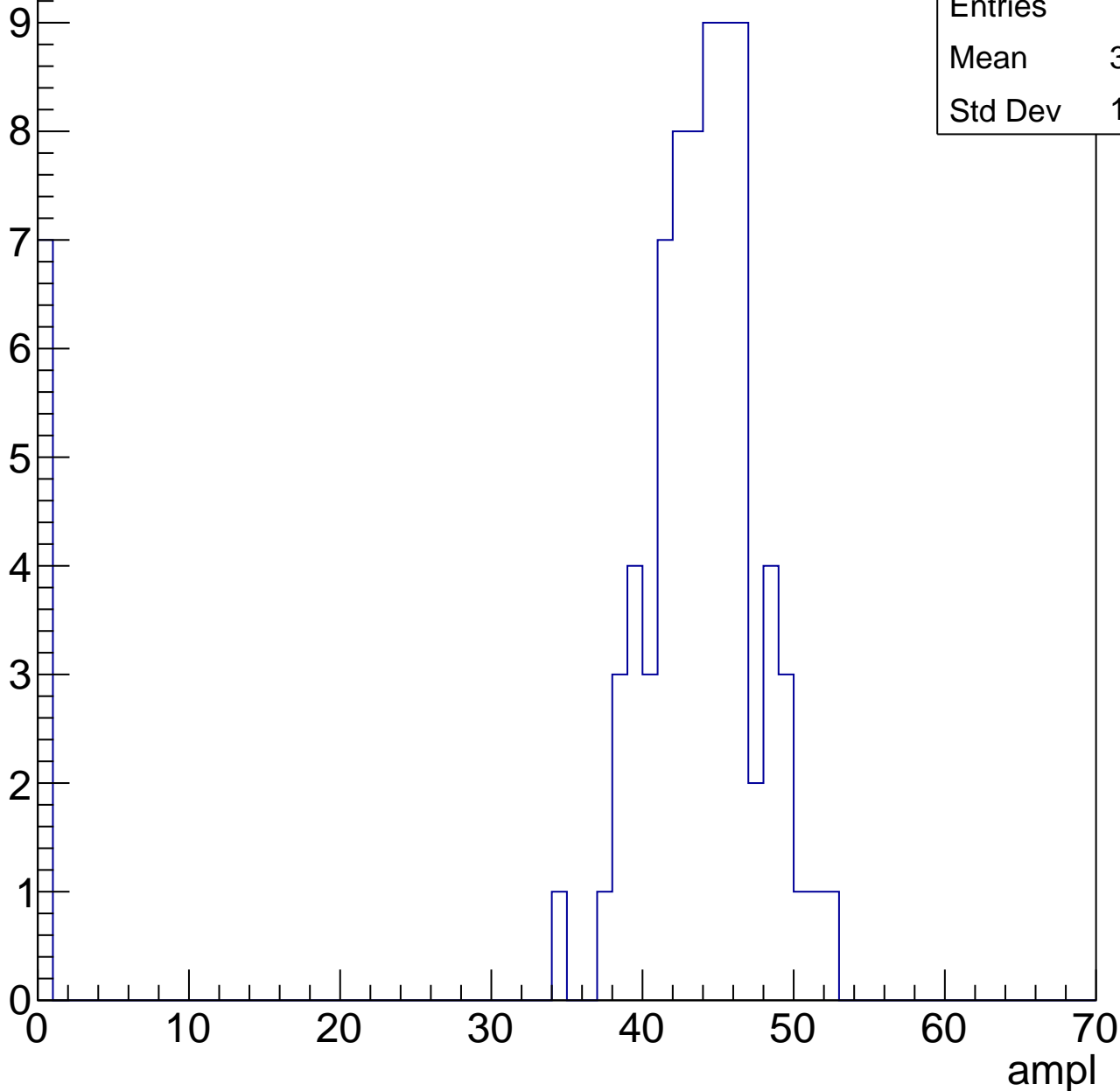


B1L103S, U11-ch29, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	81
Mean	39.86
Std Dev	12.68

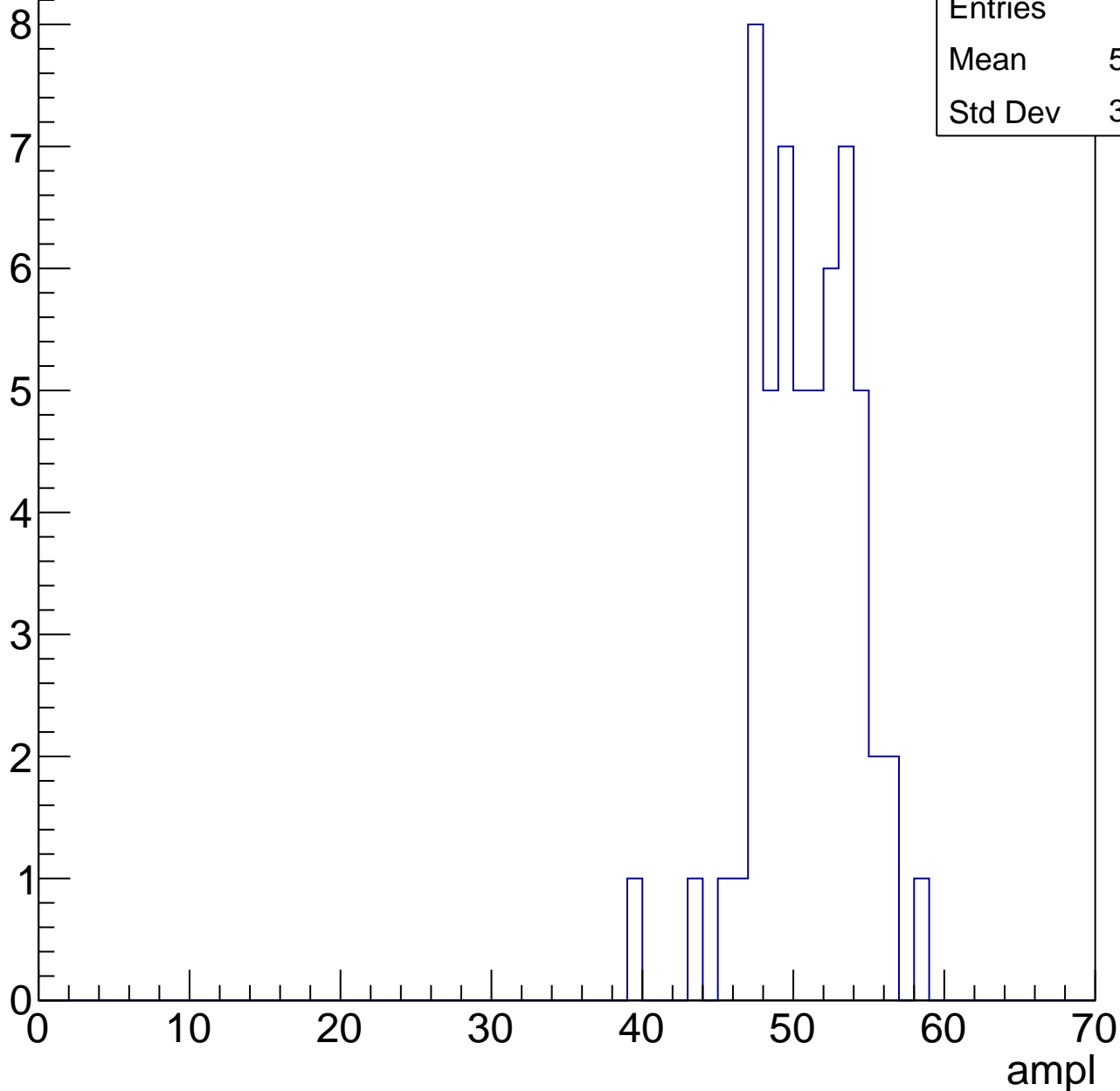


B1L103S, U11-ch29, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	50.35
Std Dev	3.405

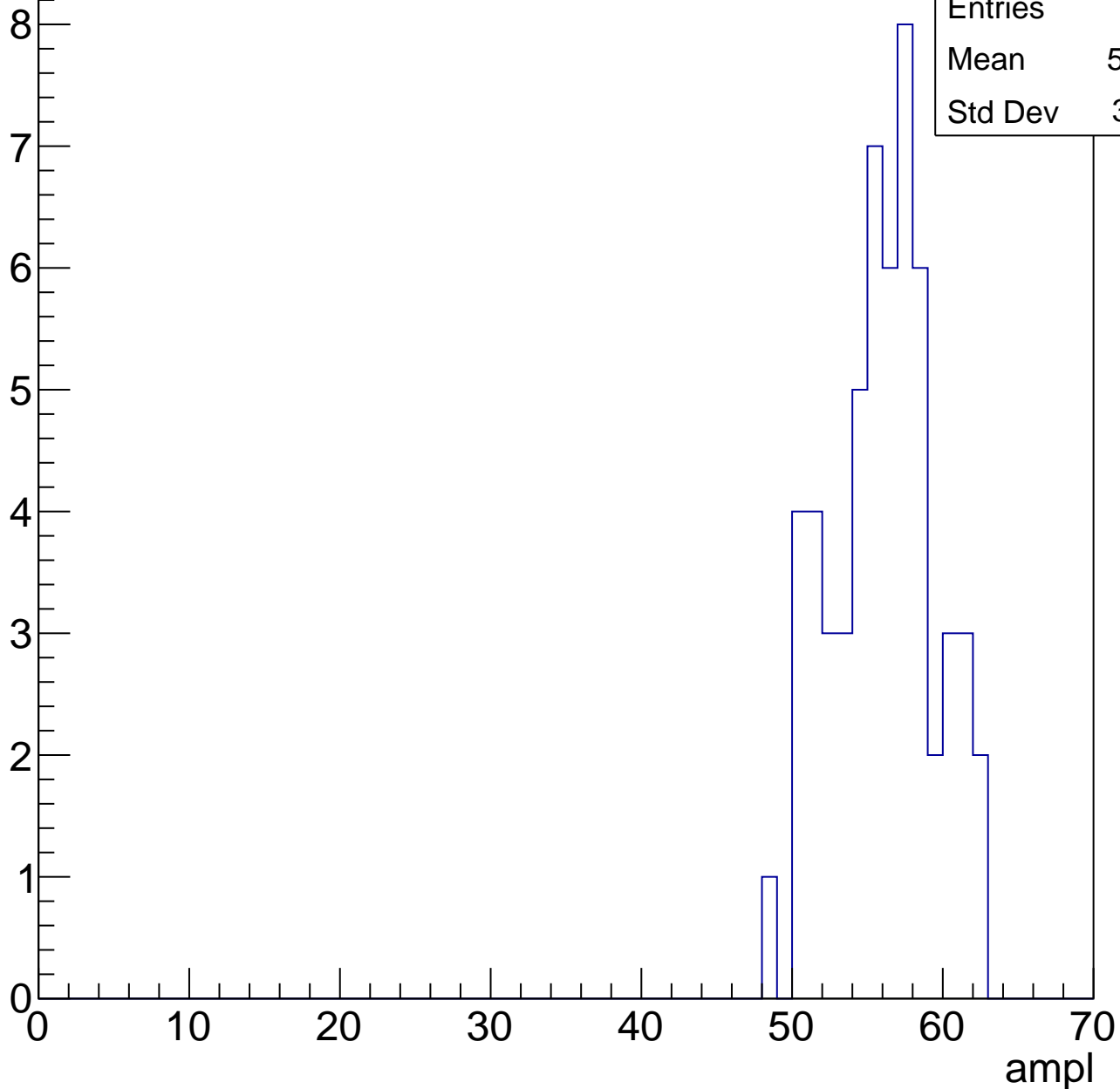


B1L103S, U11-ch29, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	55.56
Std Dev	3.361

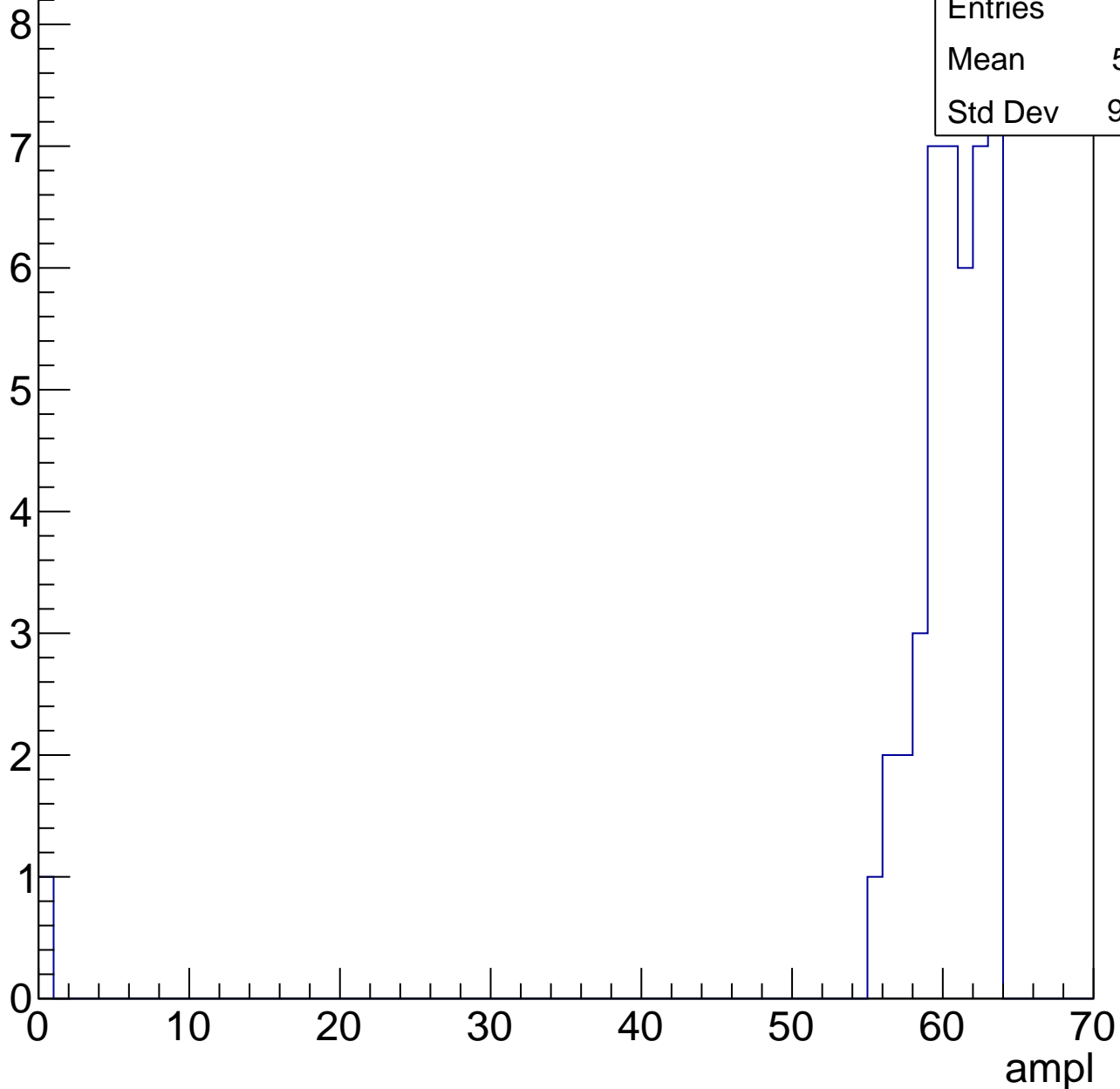


B1L103S, U11-ch29, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

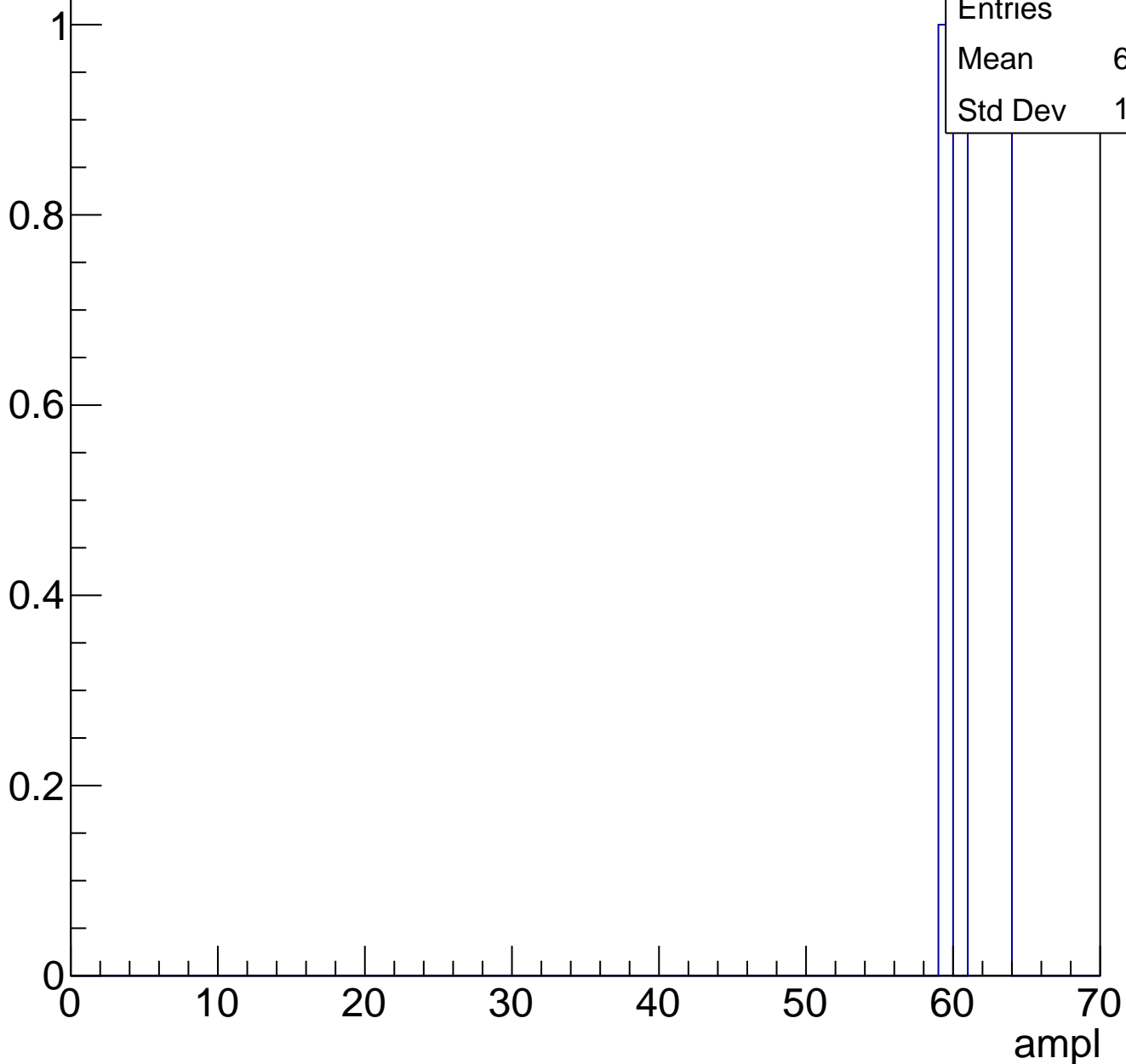
Entries	44
Mean	58.91
Std Dev	9.229



B1L103S, U11-ch29, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch29, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry



B1L103S, U11-ch30, adc0

calib_packv5_041523_1651.root, FC#0, port C2

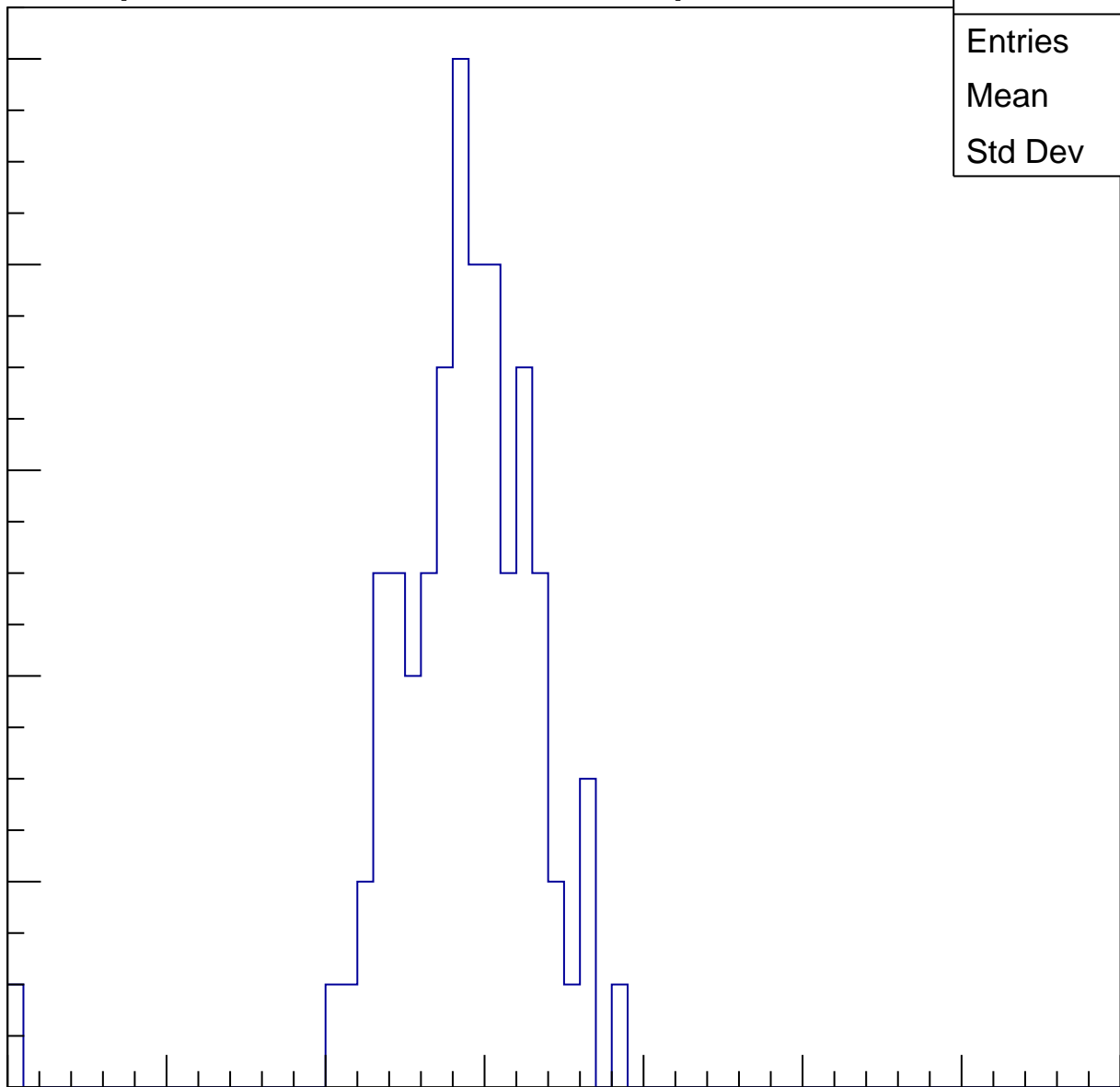
Entries	81
Mean	28.2
Std Dev	4.93

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

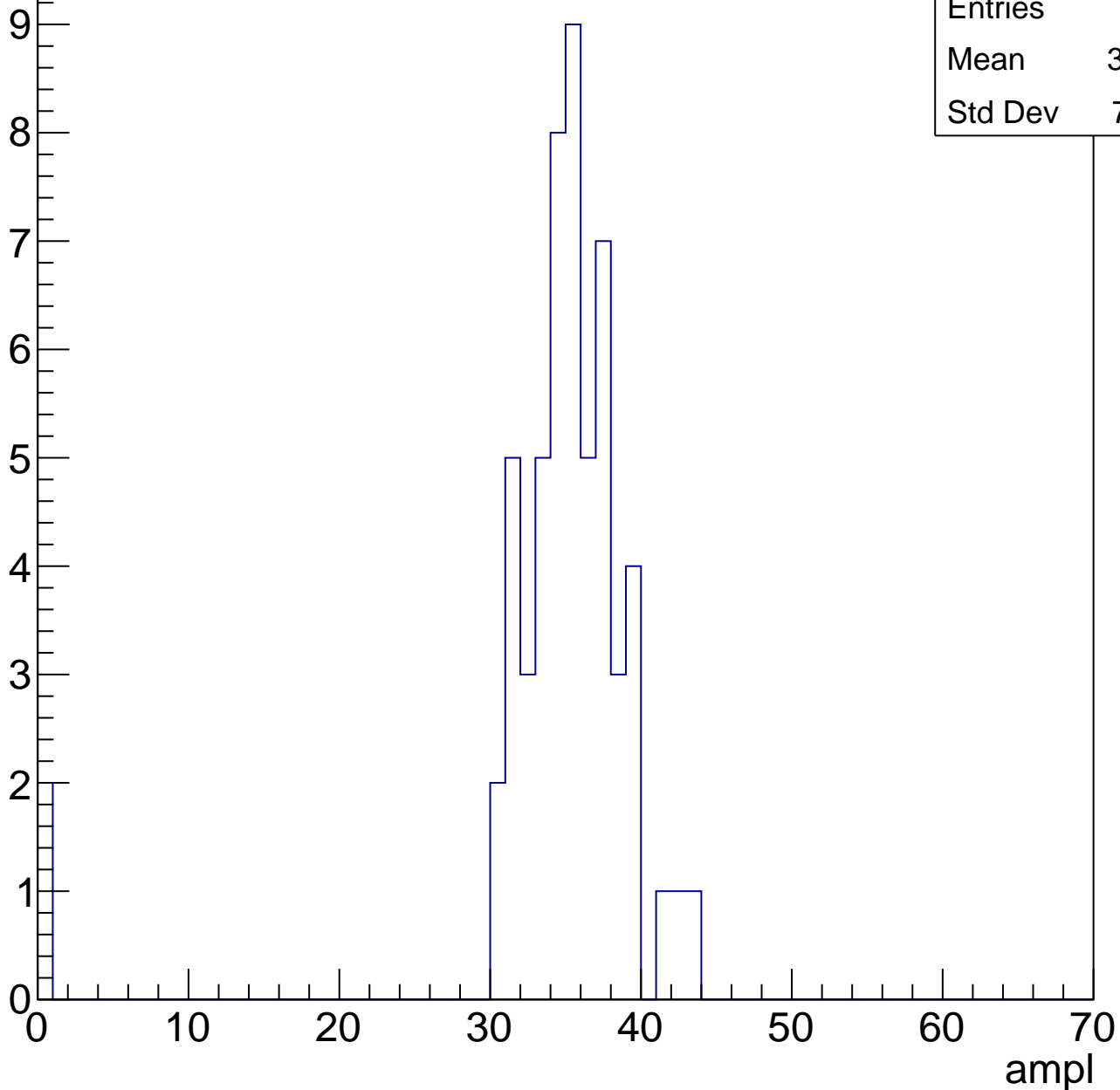


B1L103S, U11-ch30, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

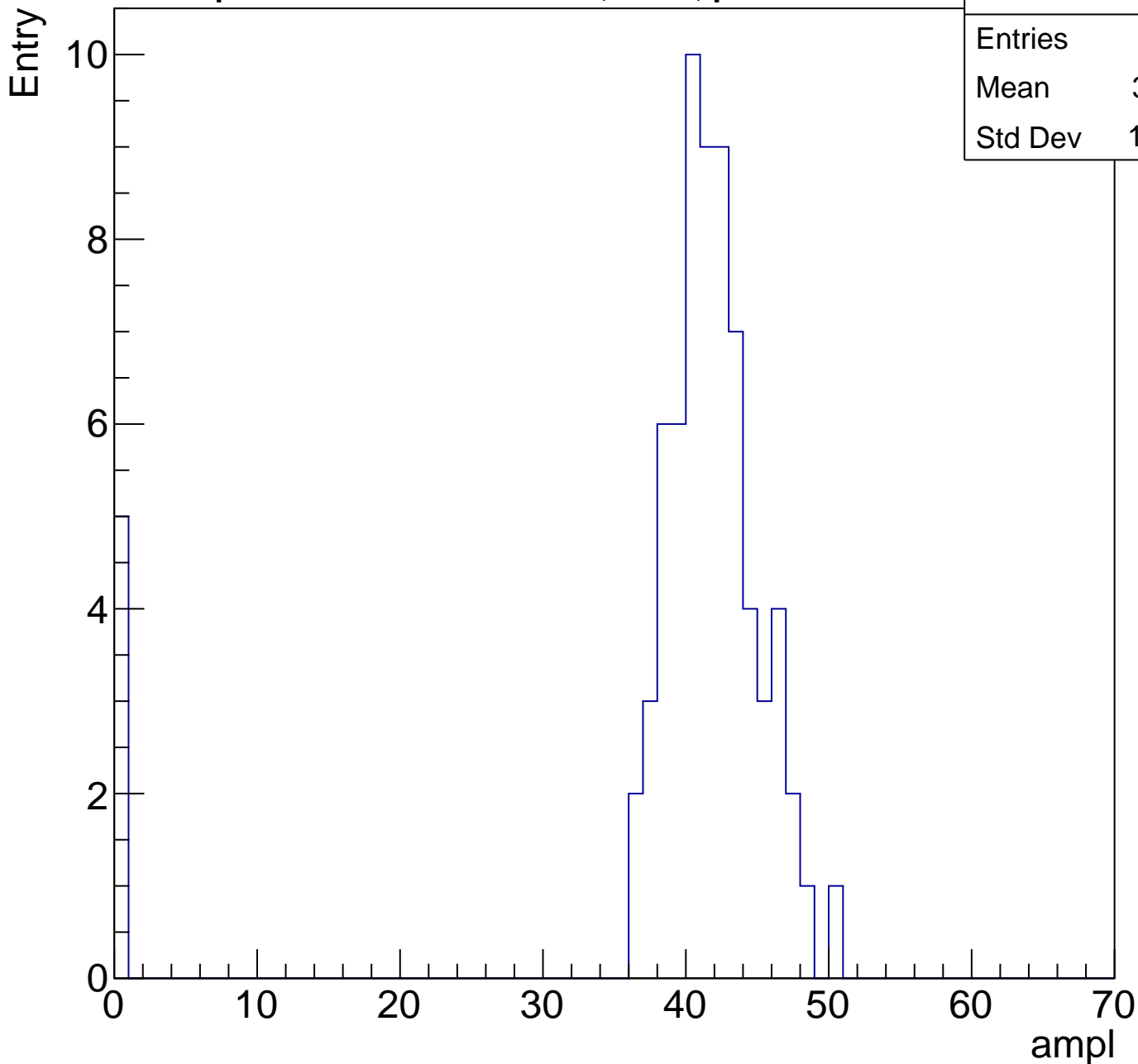
Entries	56
Mean	33.89
Std Dev	7.121



B1L103S, U11-ch30, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	72
Mean	38.61
Std Dev	10.93



B1L103S, U11-ch30, adc3

calib_packv5_041523_1651.root, FC#0, port C2

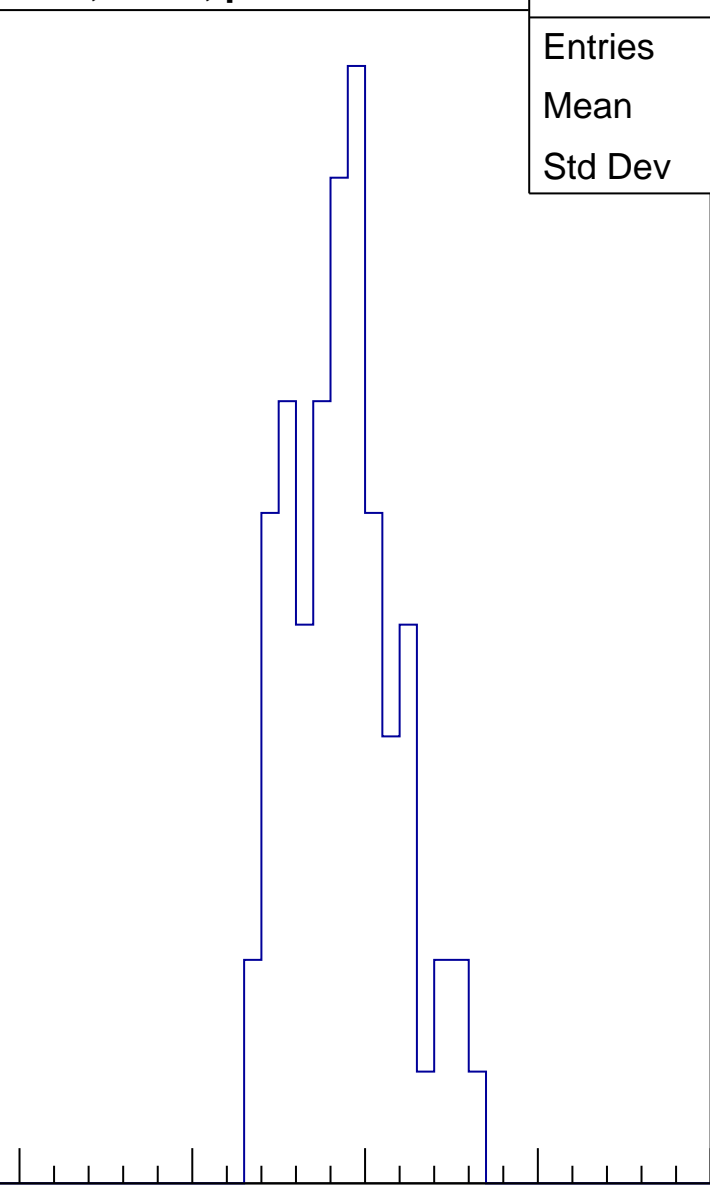
Entries	67
Mean	48.31
Std Dev	3.087

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

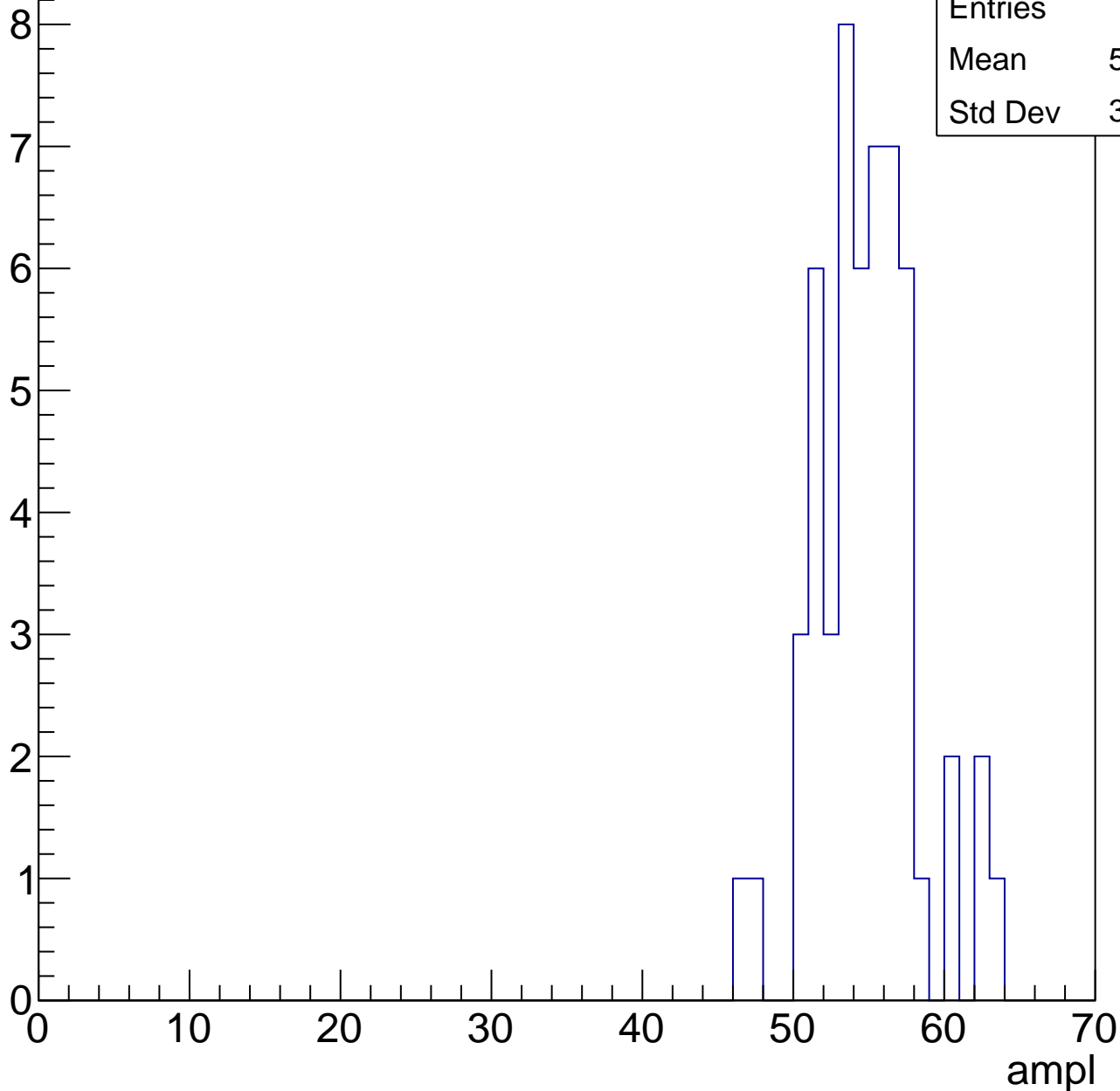


B1L103S, U11-ch30, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	54.39
Std Dev	3.369

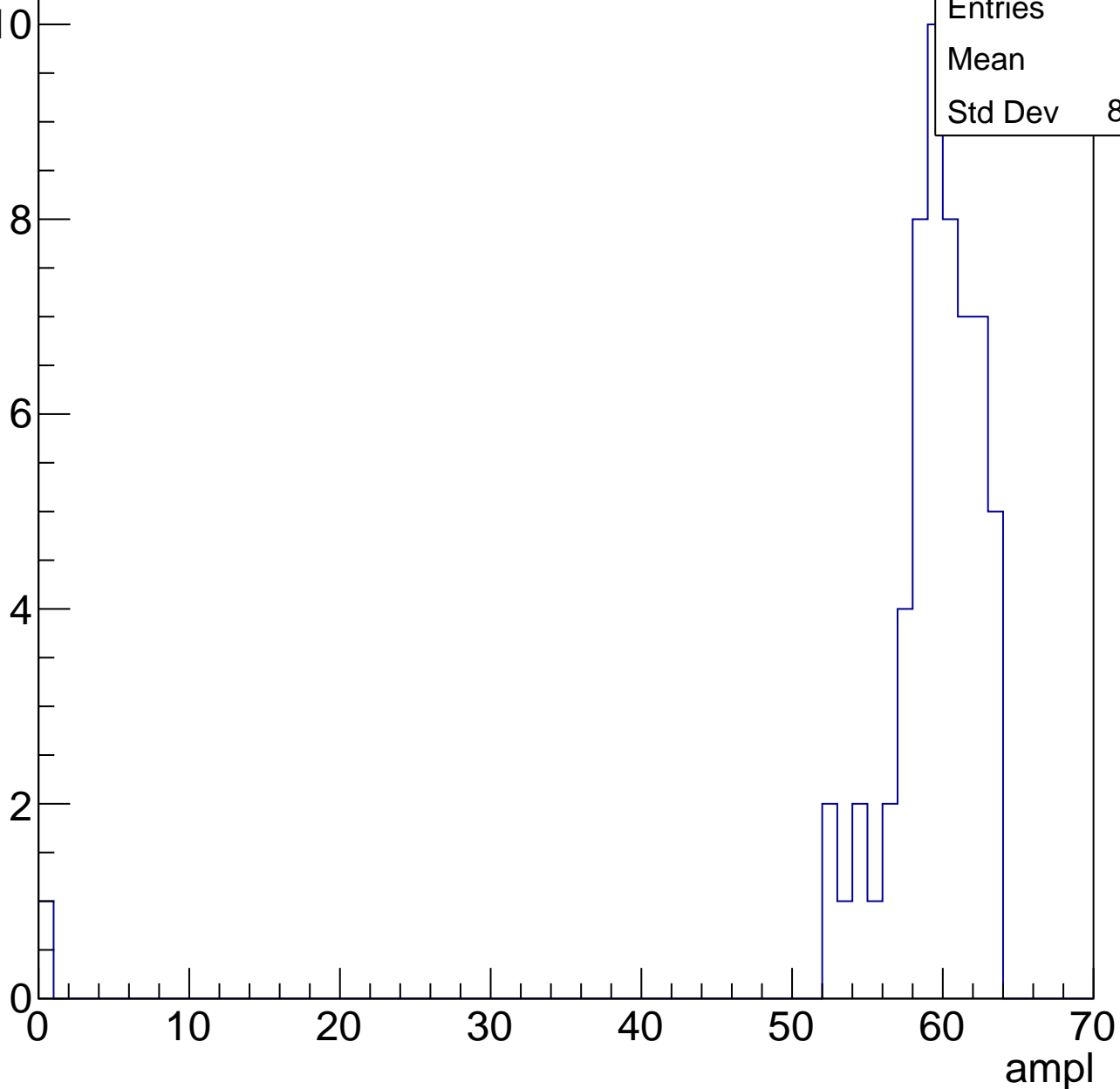


B1L103S, U11-ch30, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

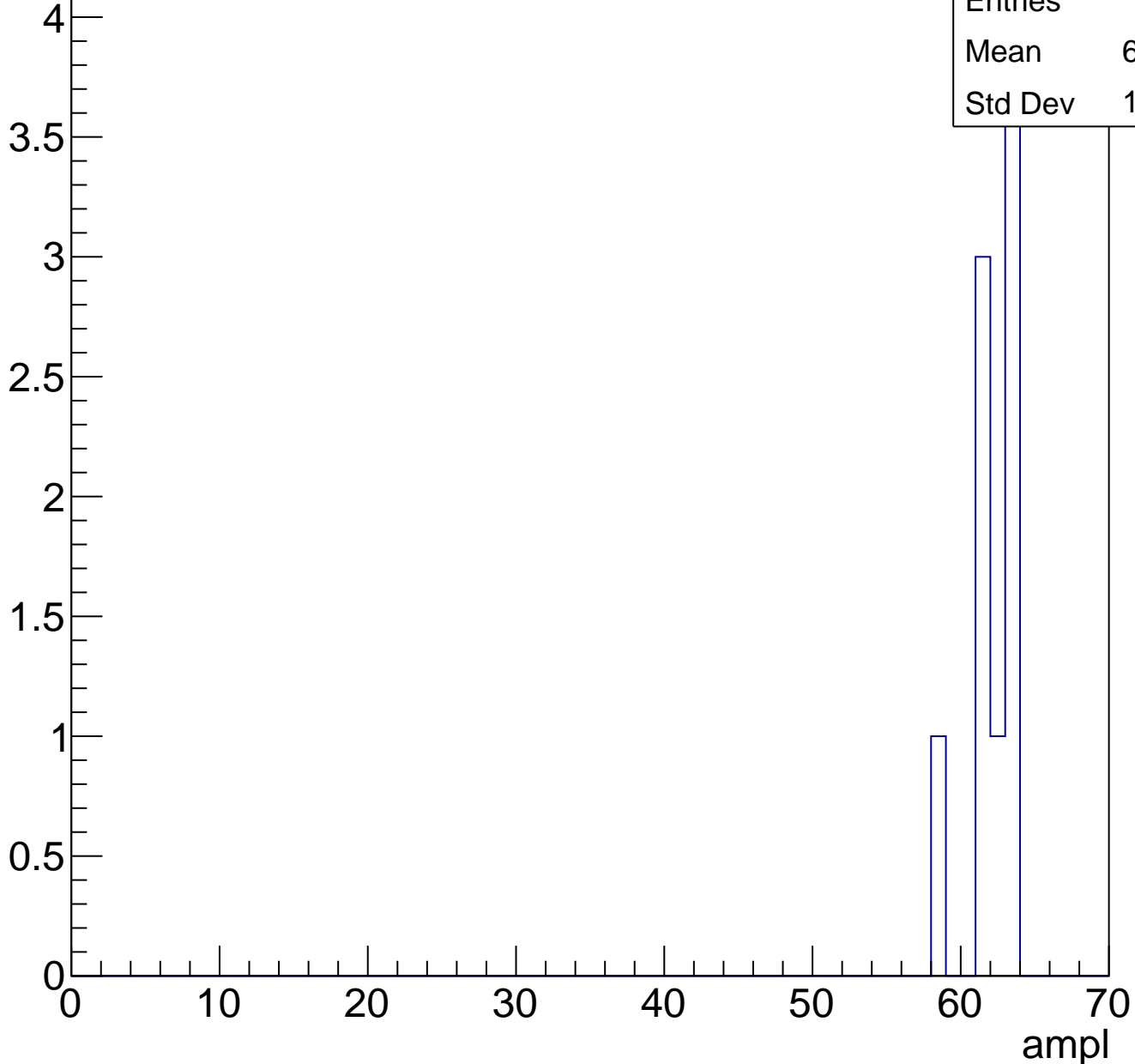
Entries	58
Mean	58.1
Std Dev	8.153



B1L103S, U11-ch30, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch30, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

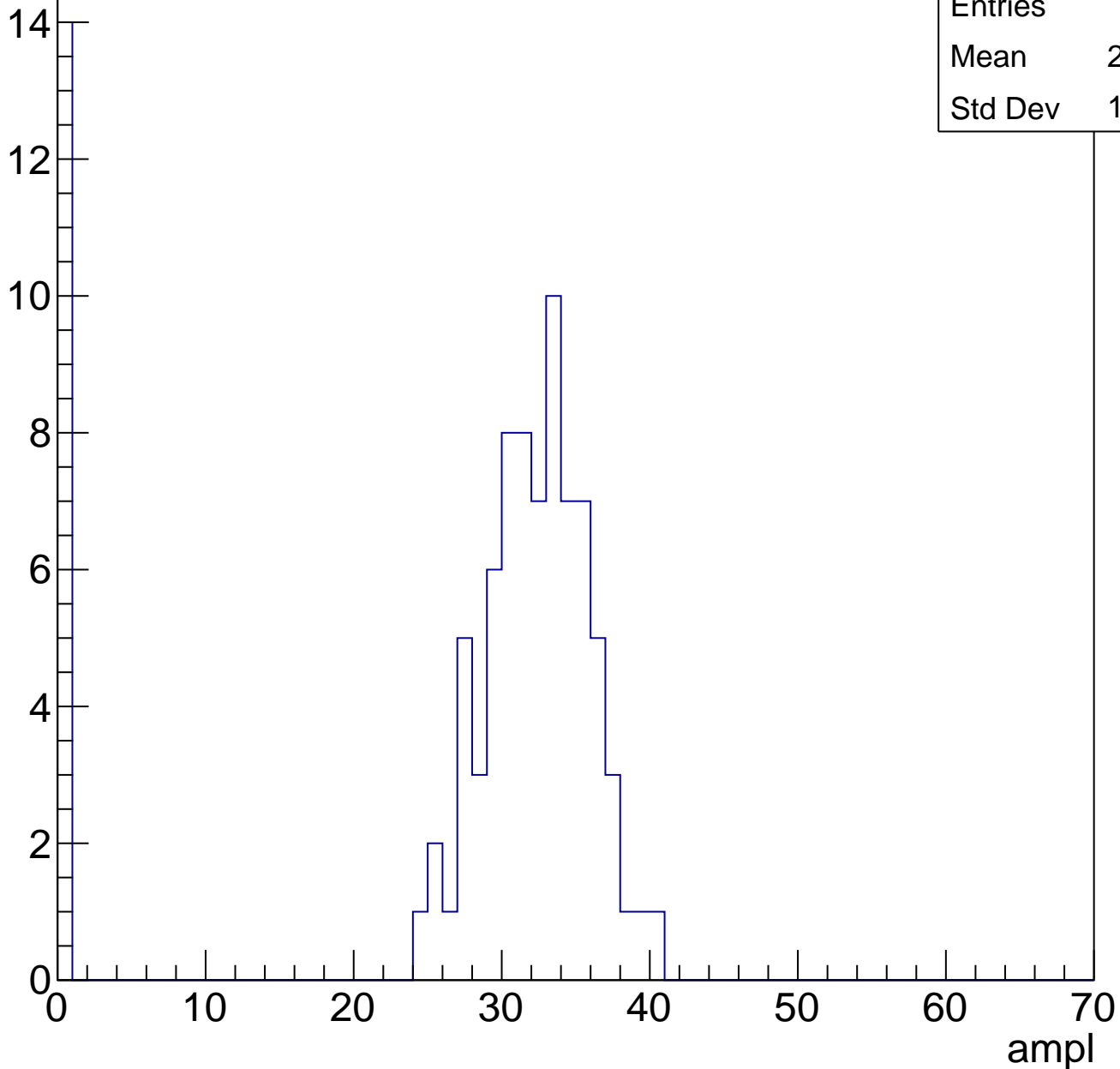


B1L103S, U11-ch31, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	90
Mean	26.96
Std Dev	11.98

Entry

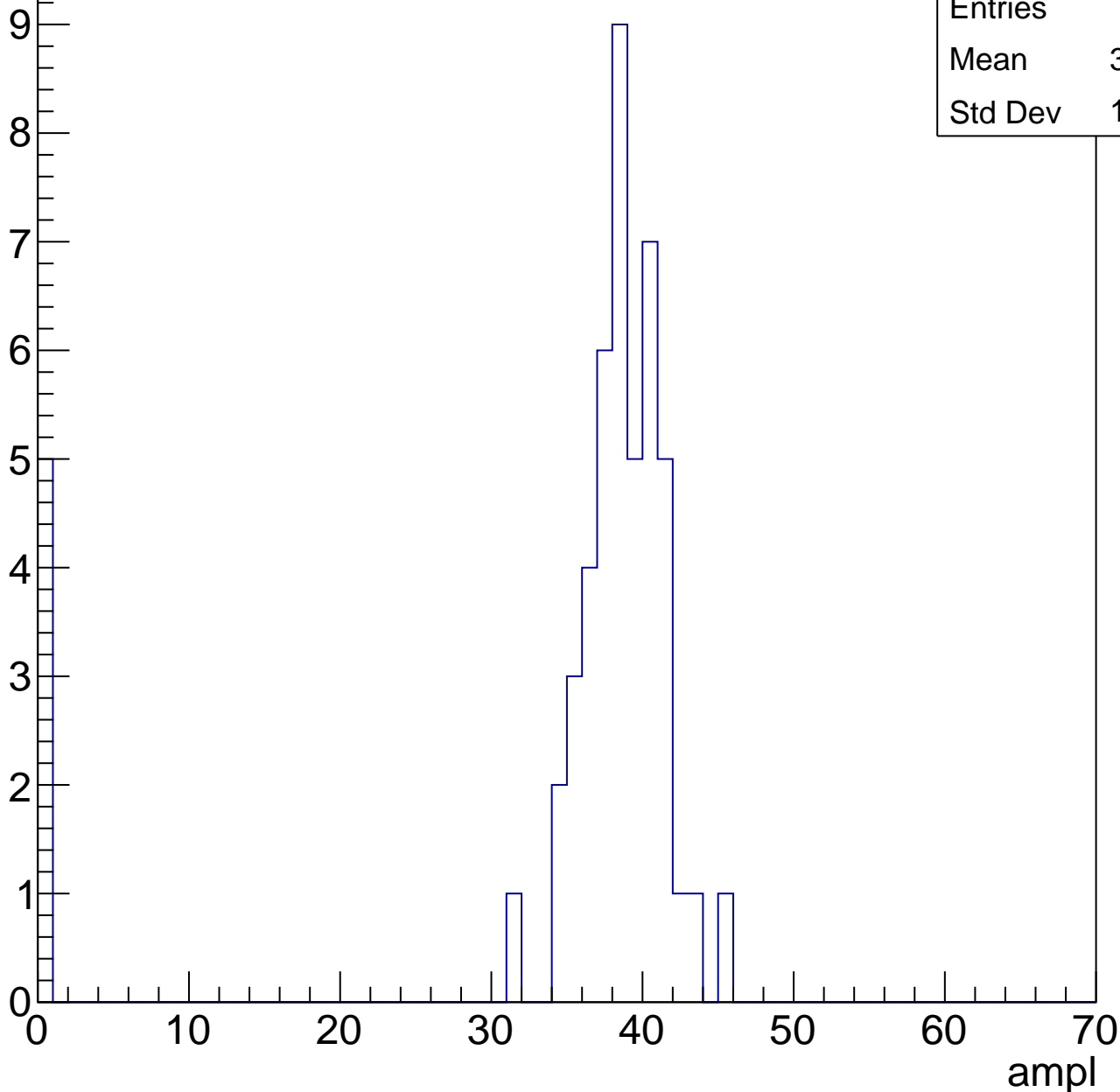


B1L103S, U11-ch31, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	34.44
Std Dev	11.73

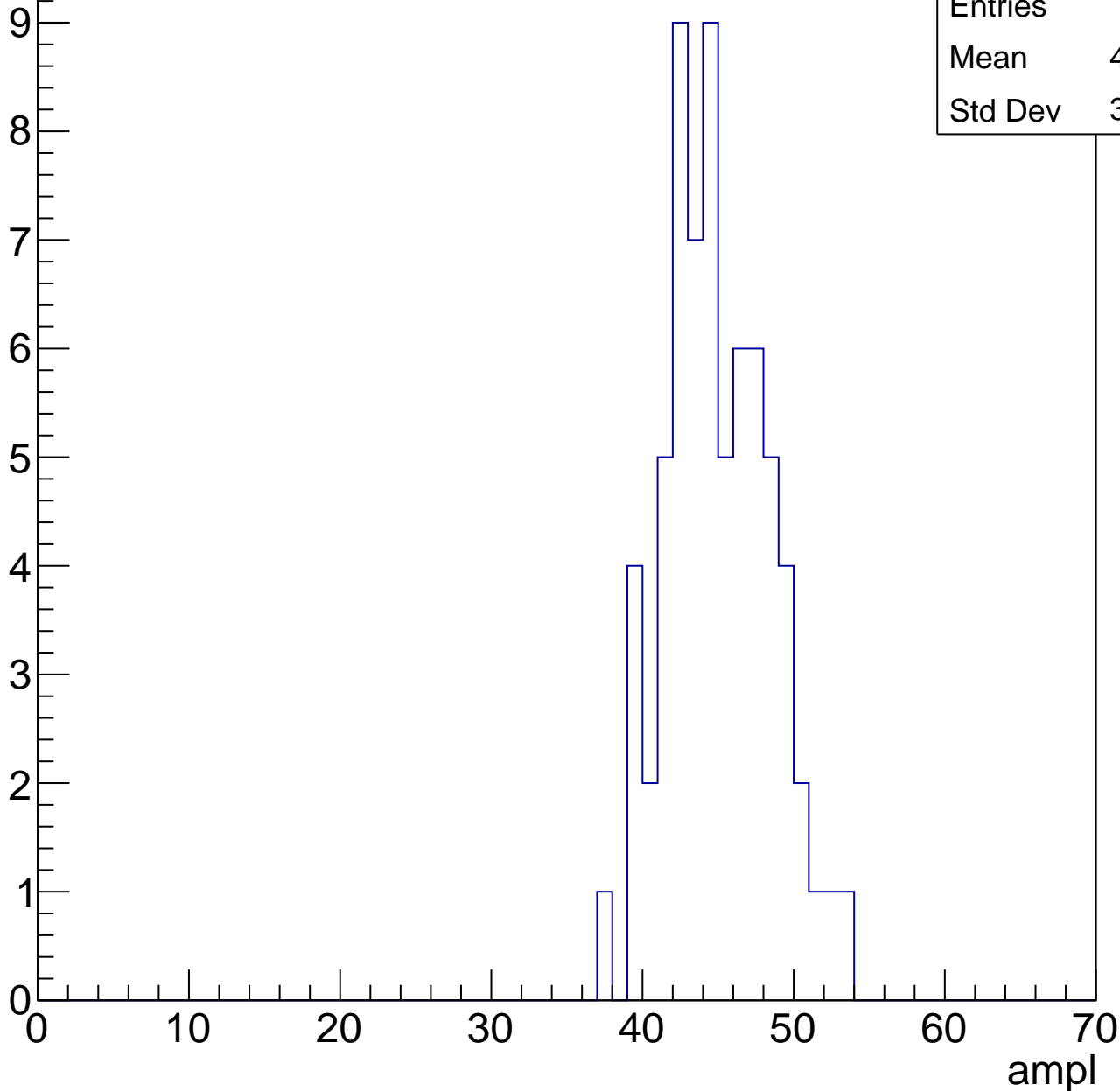


B1L103S, U11-ch31, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	44.53
Std Dev	3.385

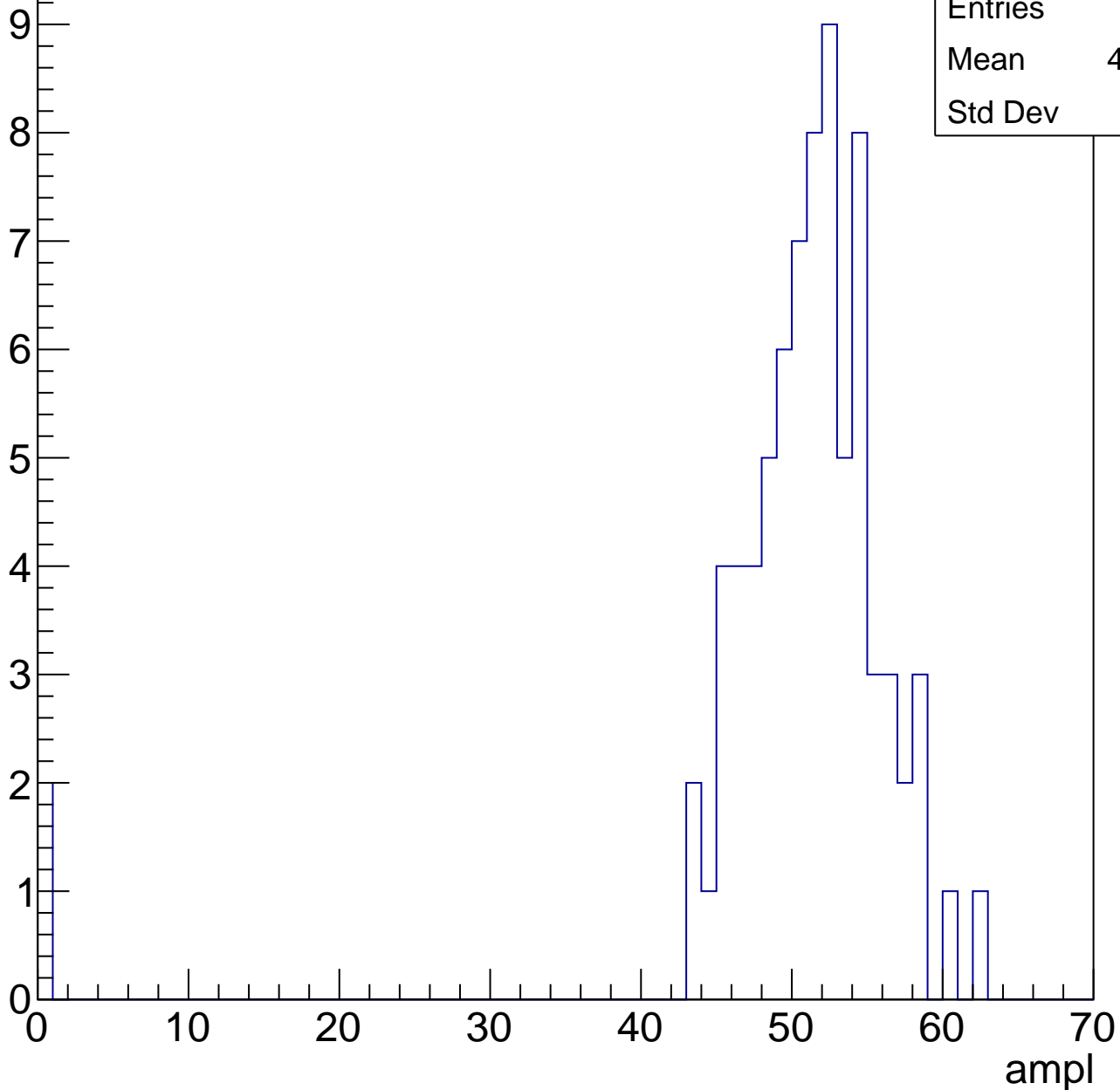


B1L103S, U11-ch31, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	49.77
Std Dev	8.98

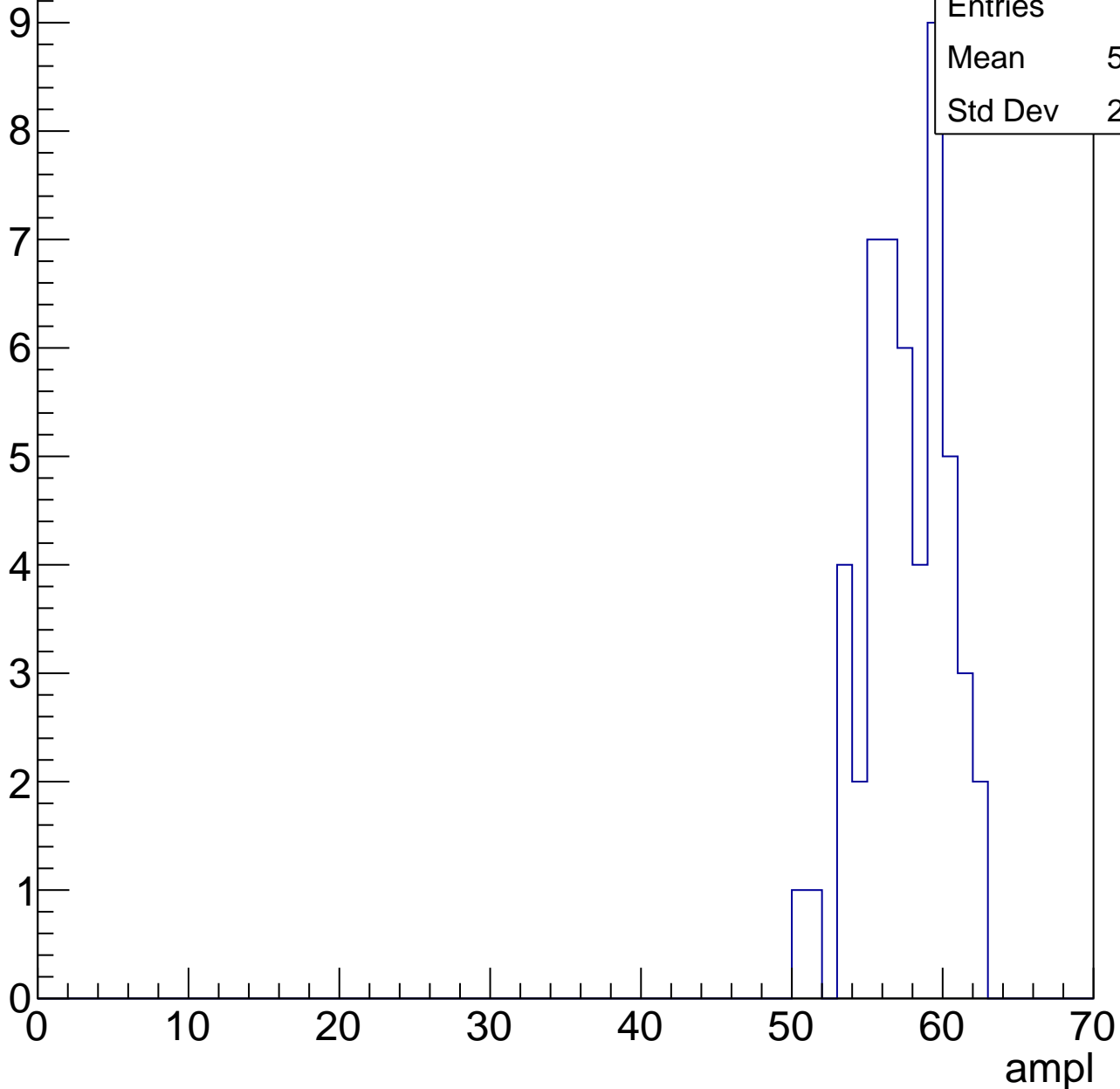


B1L103S, U11-ch31, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	57.06
Std Dev	2.747

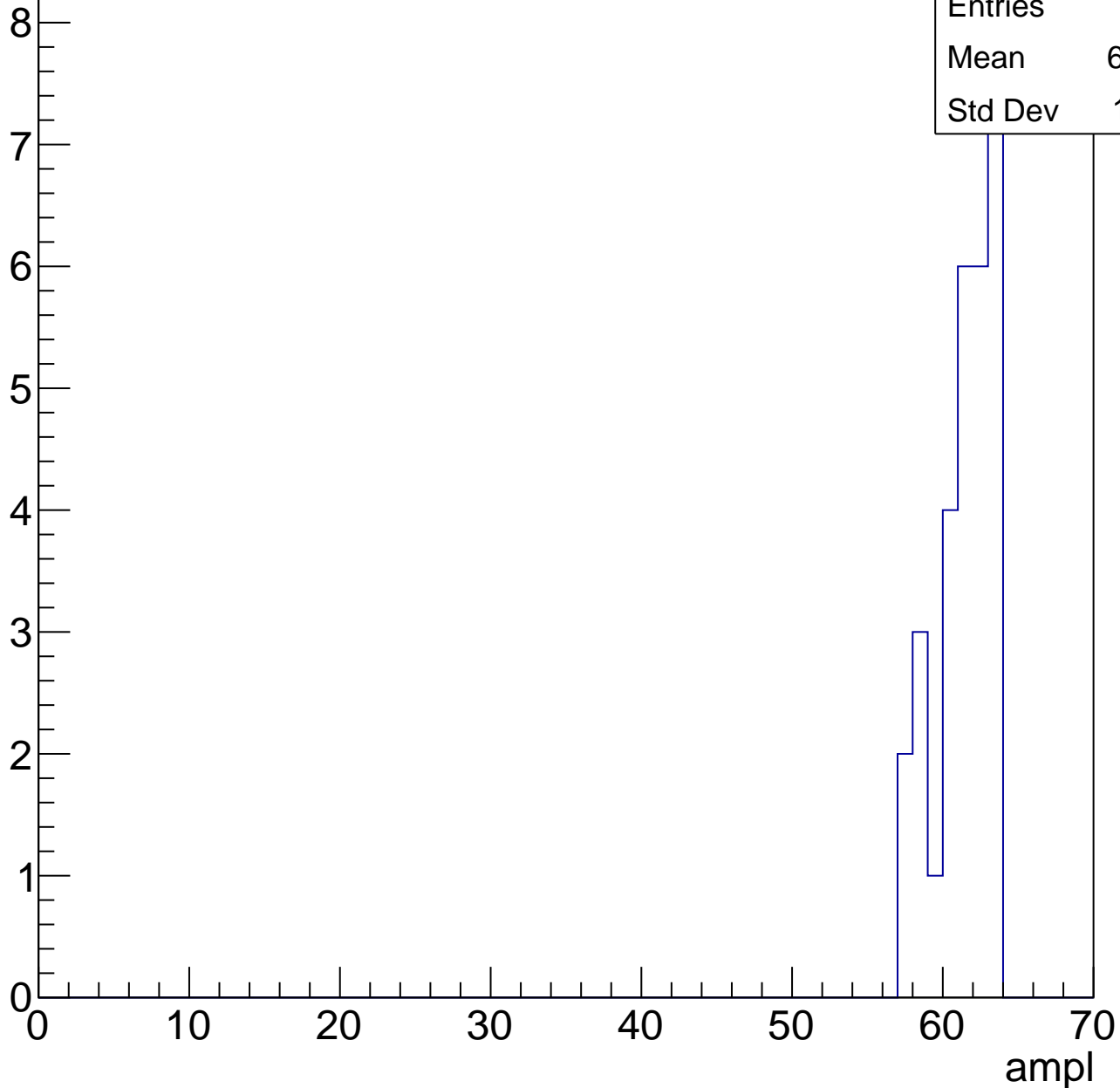


B1L103S, U11-ch31, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	30
Mean	60.97
Std Dev	1.871



B1L103S, U11-ch31, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch31, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

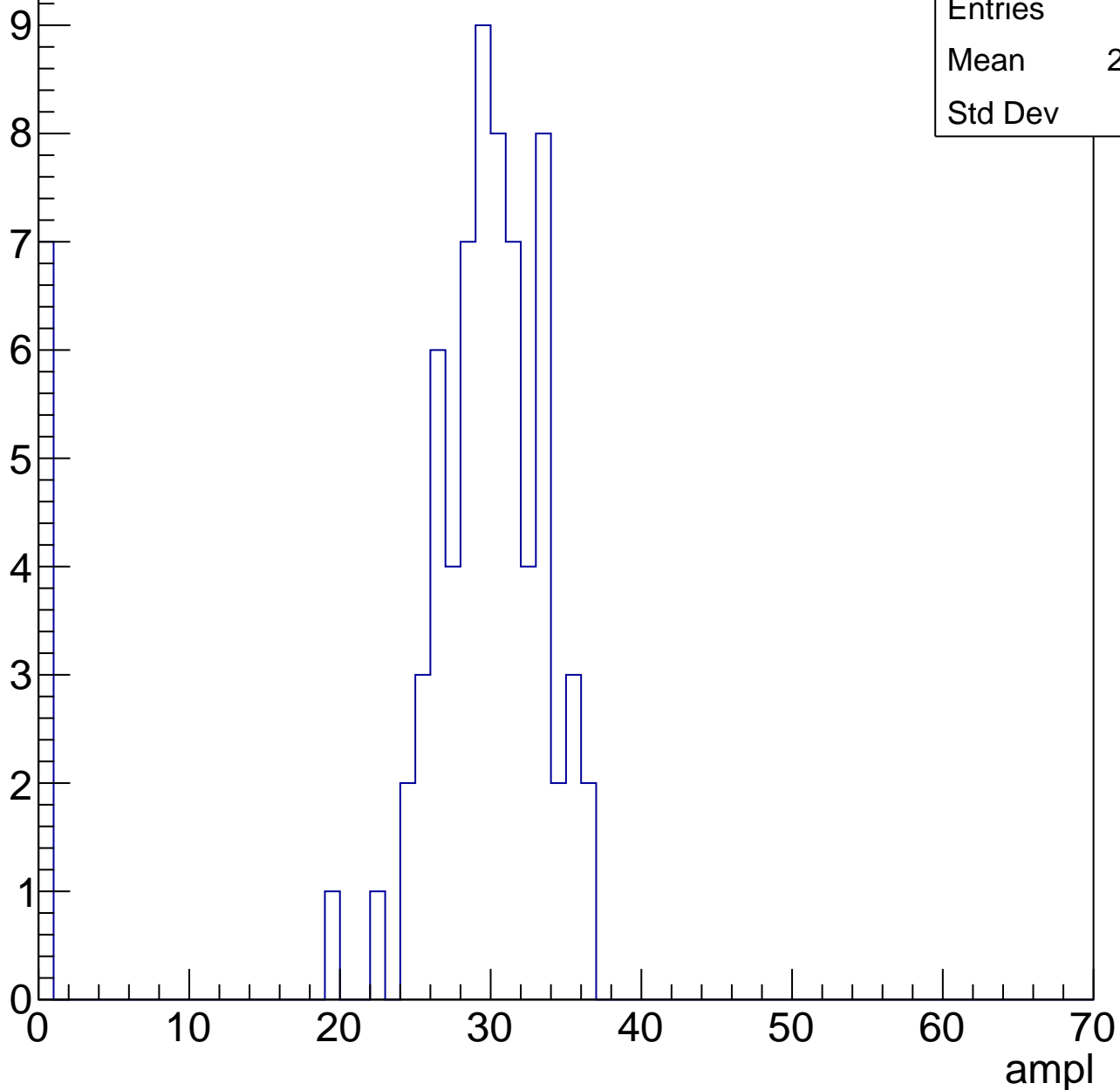


B1L103S, U11-ch32, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	26.74
Std Dev	9.22

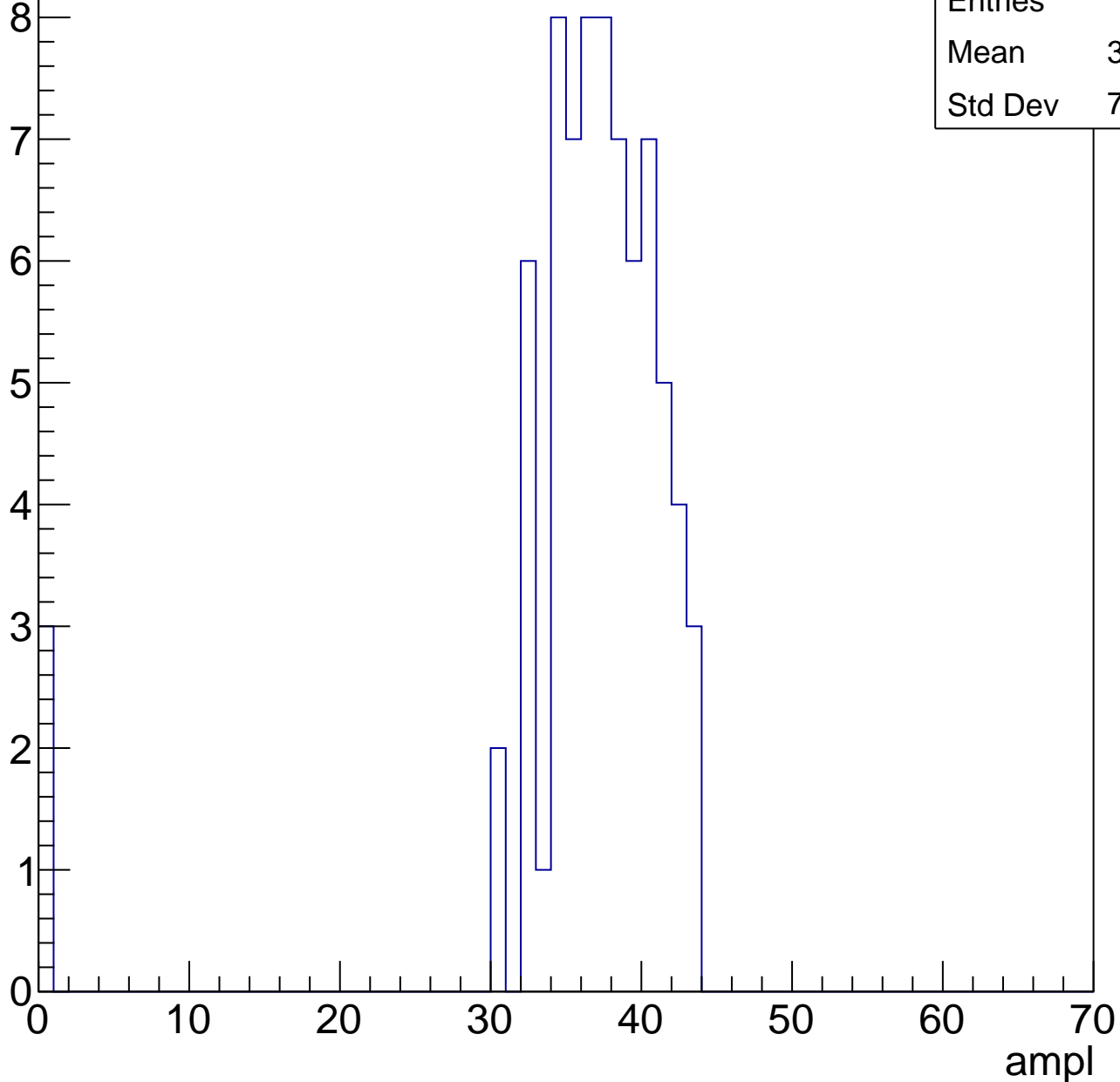


B1L103S, U11-ch32, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	35.57
Std Dev	7.923

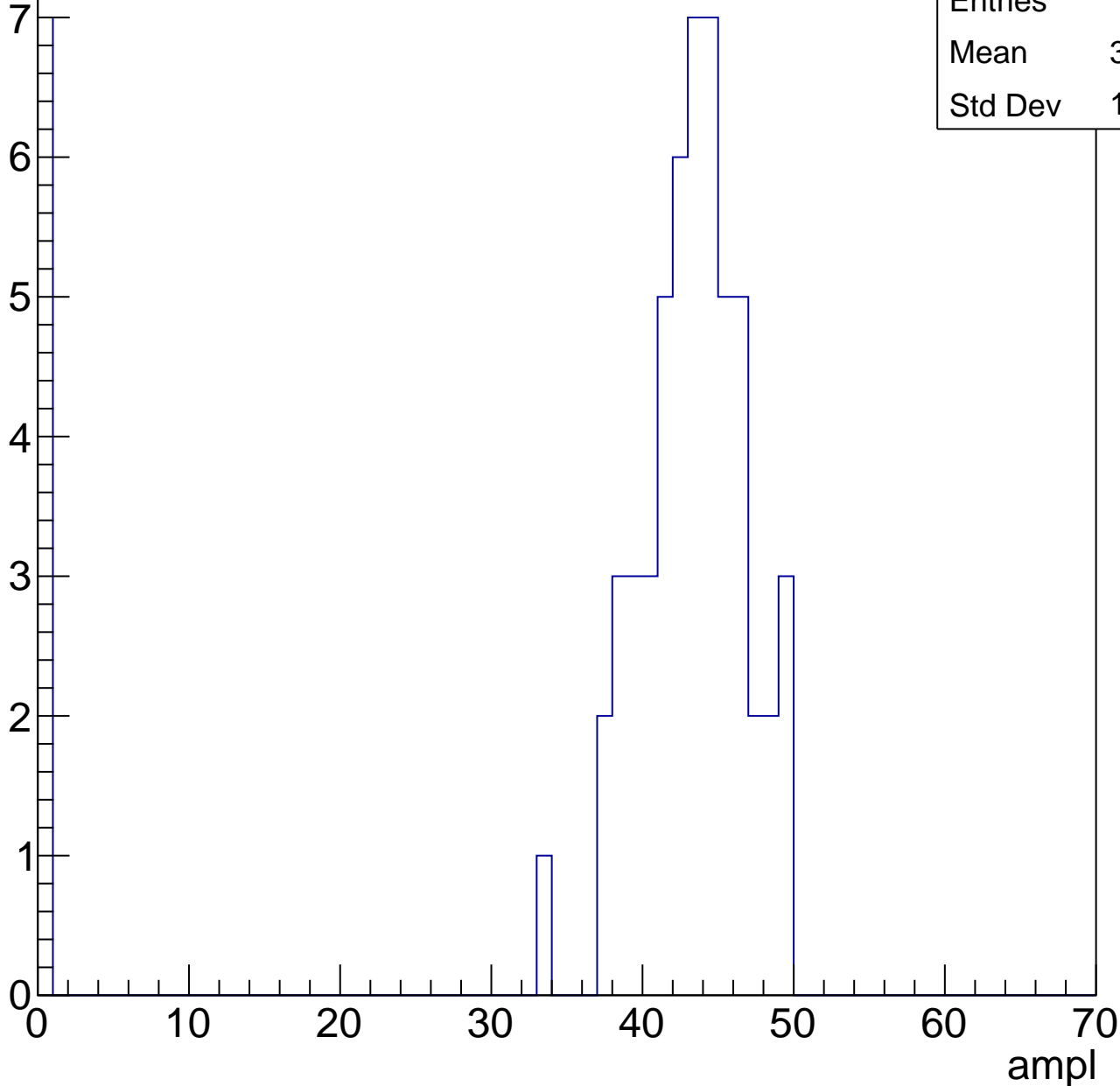


B1L103S, U11-ch32, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	37.97
Std Dev	14.03

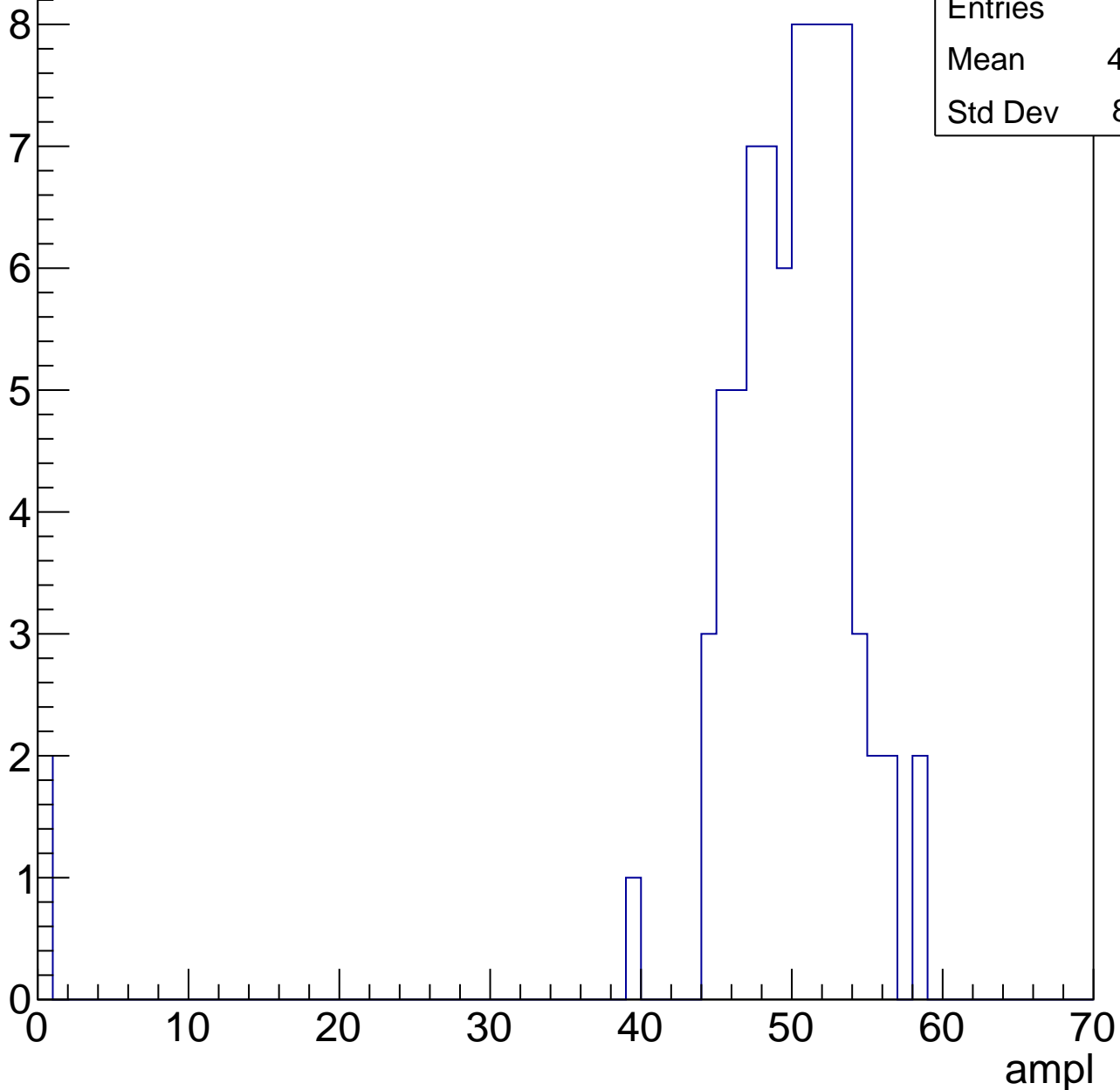


B1L103S, U11-ch32, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	48.48
Std Dev	8.651

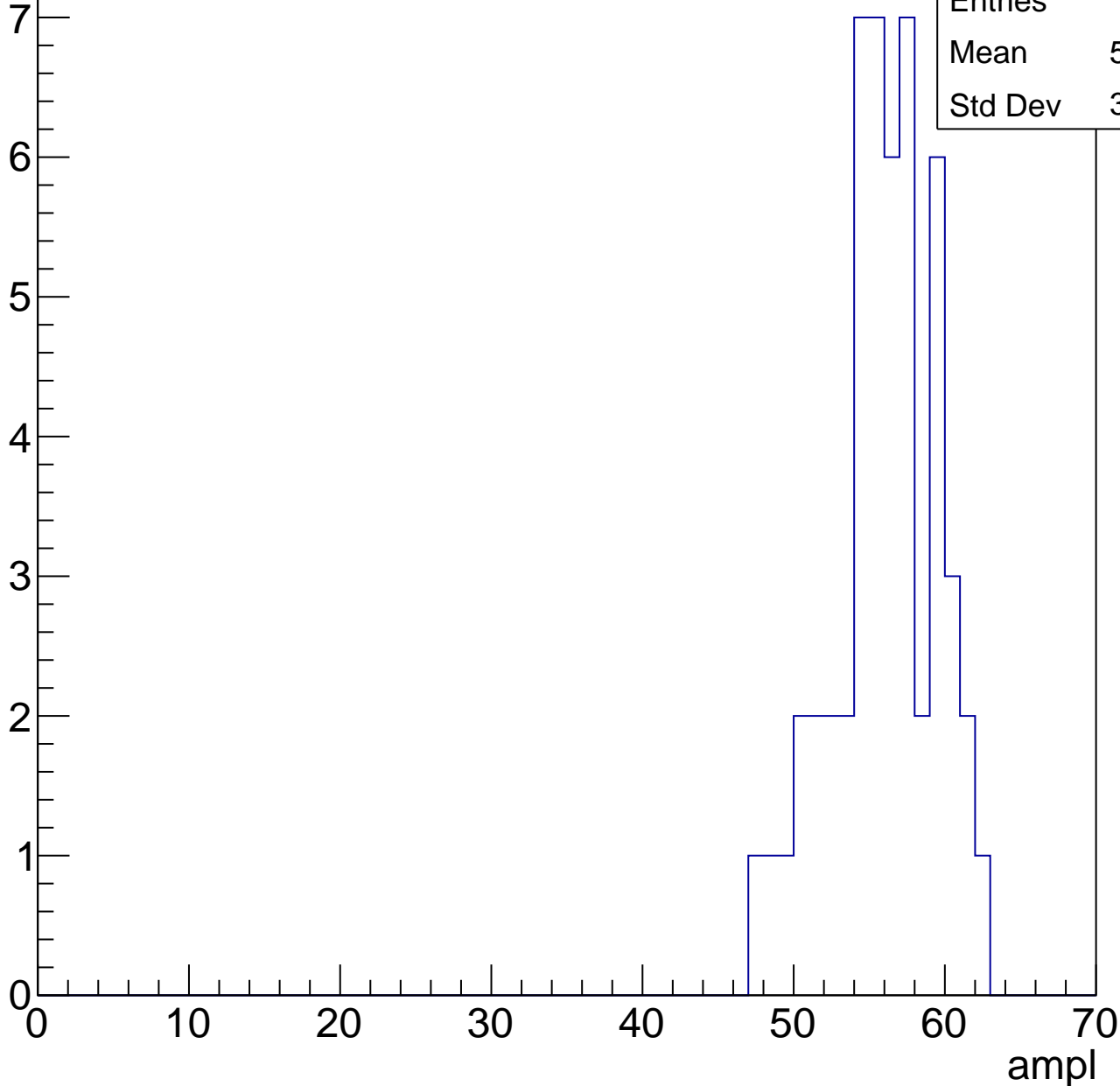


B1L103S, U11-ch32, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

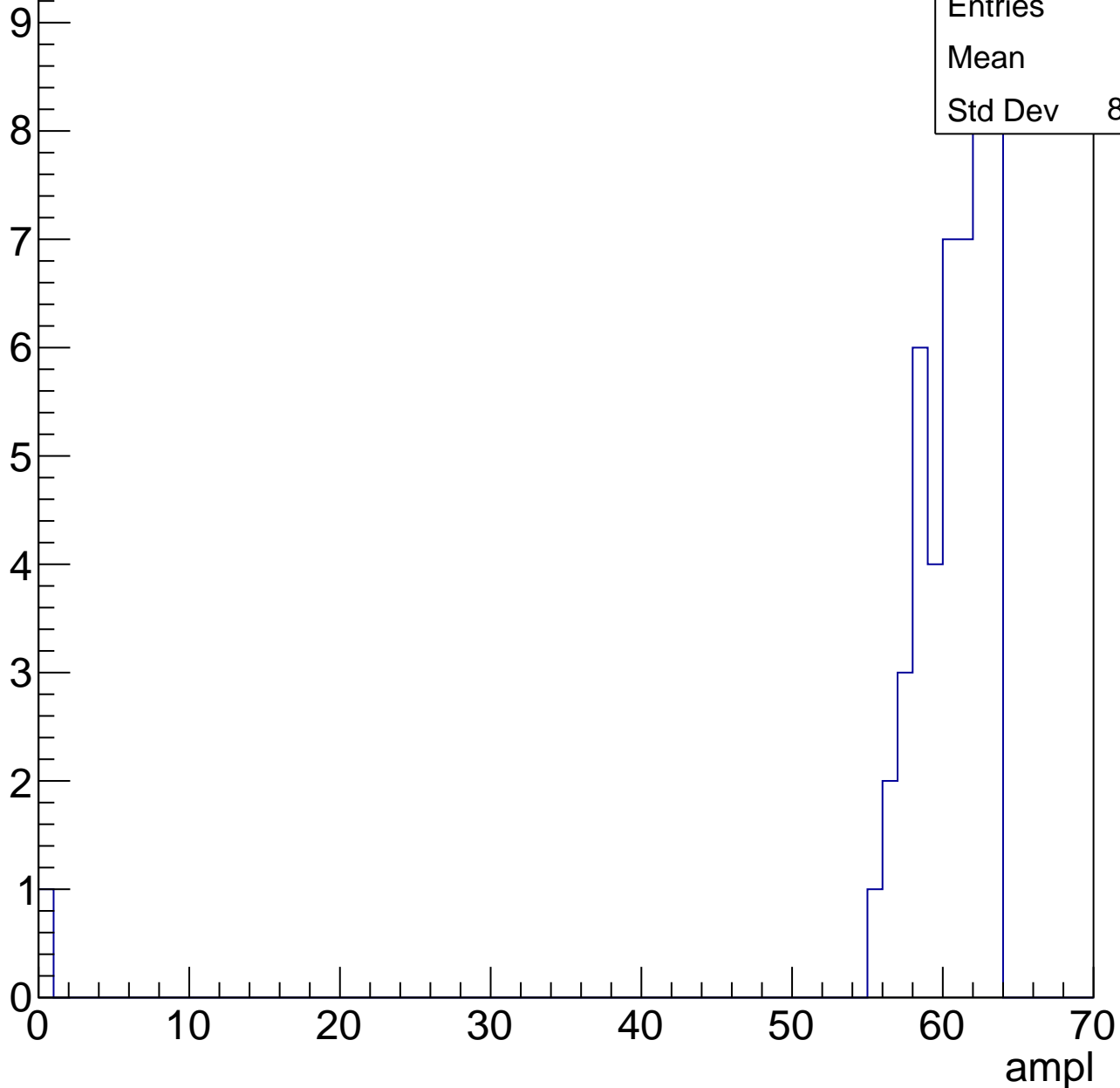
Entries	52
Mean	55.54
Std Dev	3.377



B1L103S, U11-ch32, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch32, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch32, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch33, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	68
Mean	24.54
Std Dev	11.13

Entry

10

8

6

4

2

0

ampl

0

10

20

30

40

50

60

70

B1L103S, U11-ch33, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	93
Mean	32
Std Dev	12.28

Entry

10

8

6

4

2

0

0

10

20

30

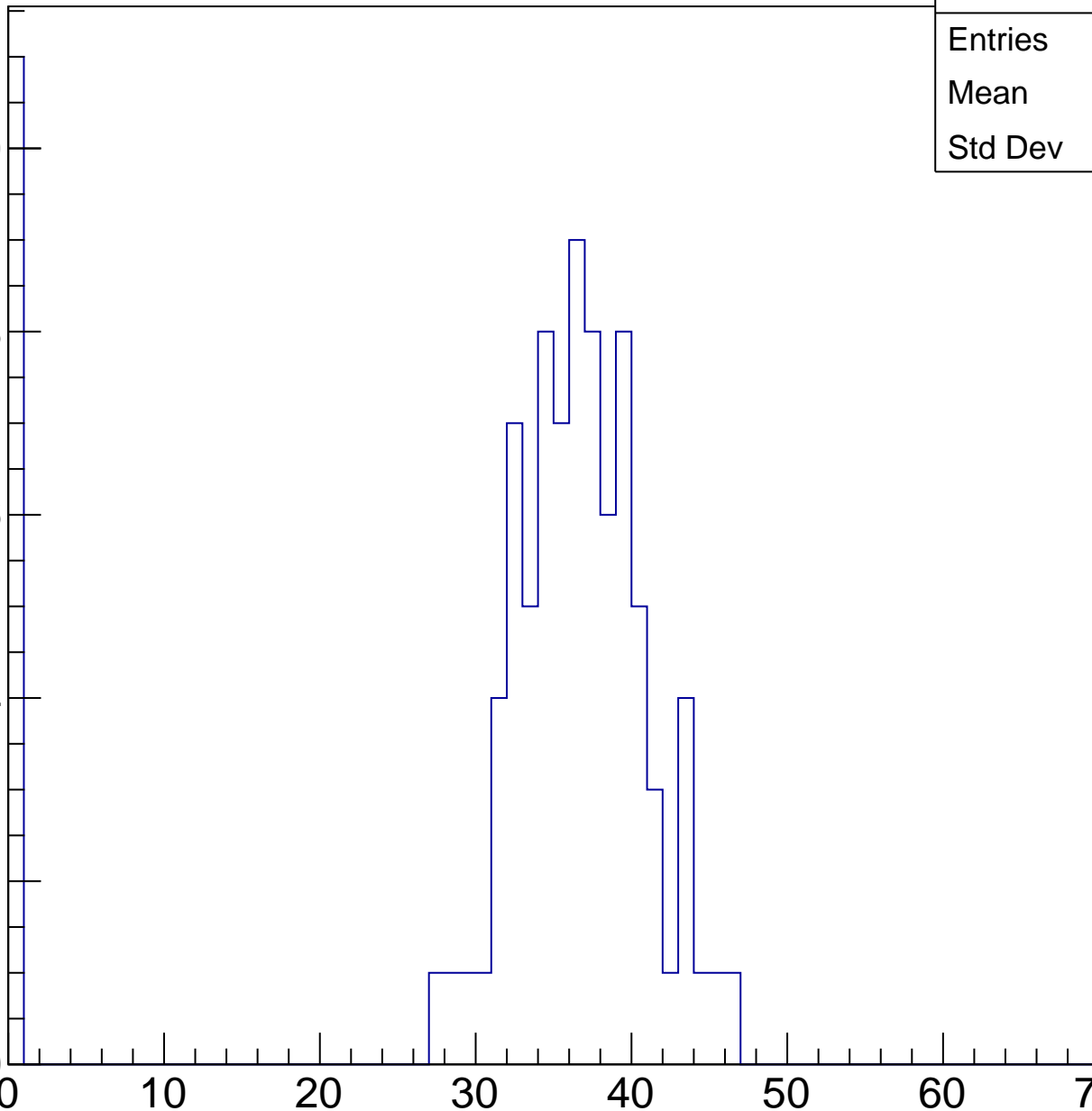
40

50

60

70

ampl

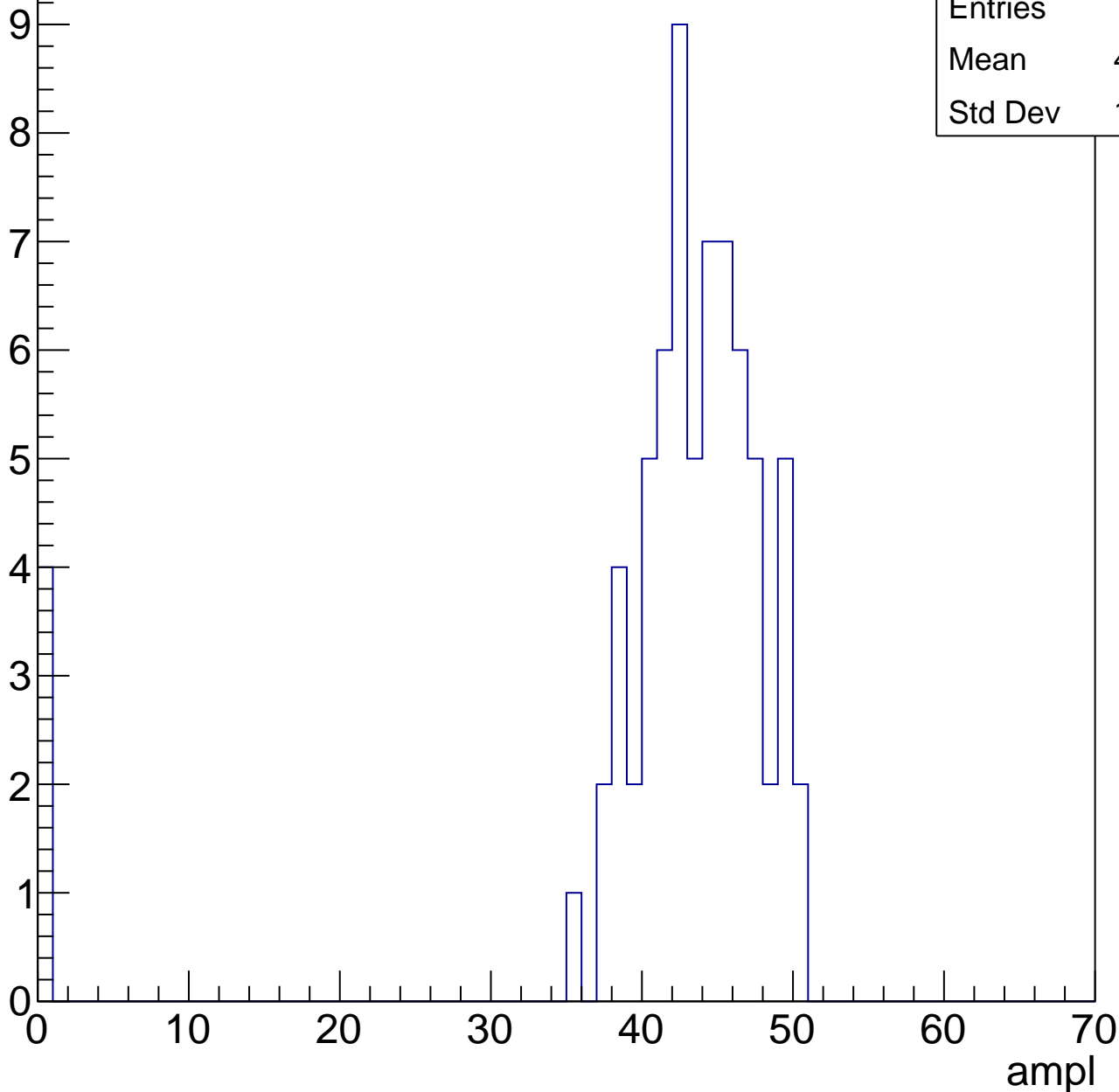


B1L103S, U11-ch33, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	41.01
Std Dev	10.51

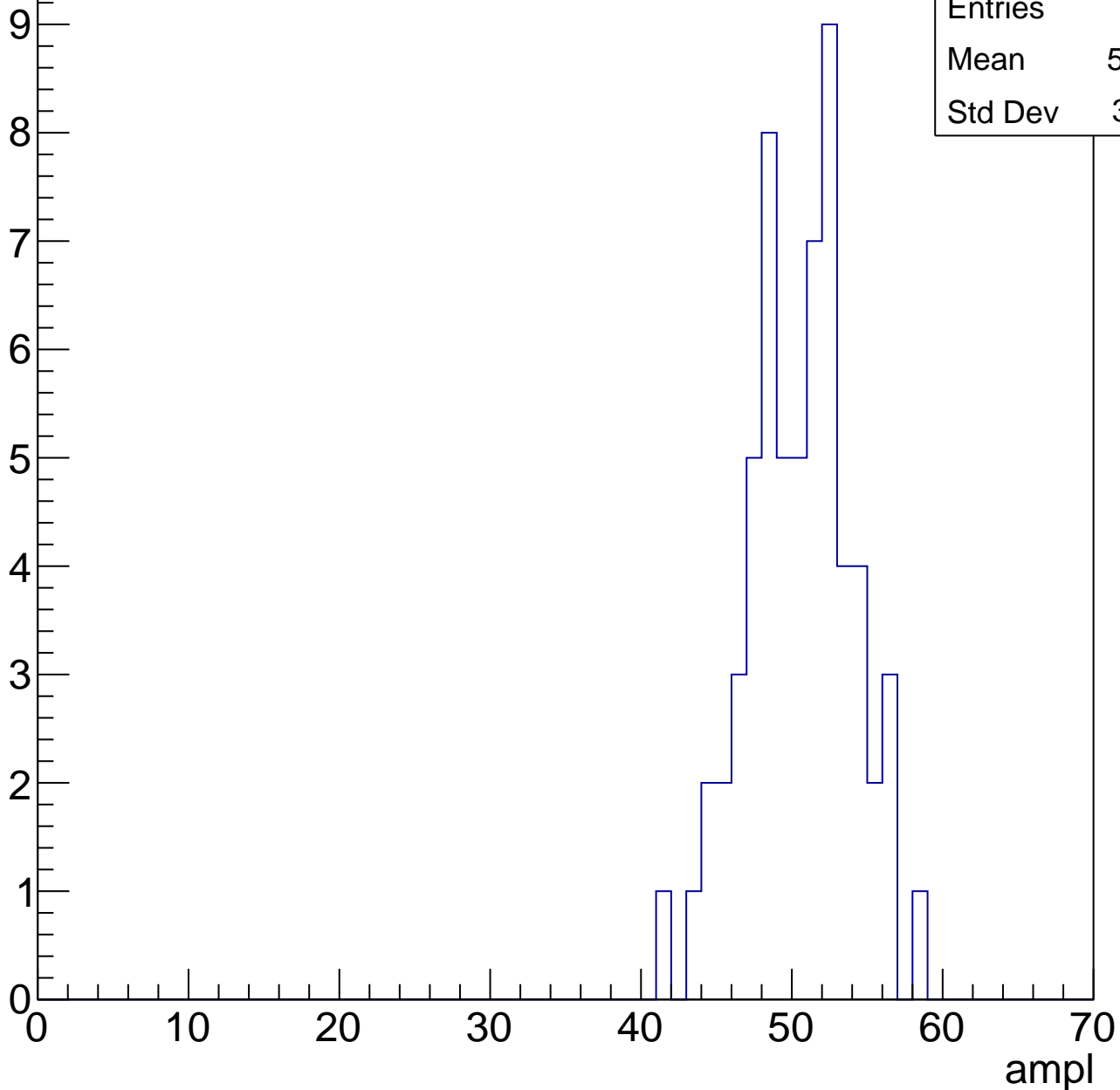


B1L103S, U11-ch33, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	50.05
Std Dev	3.471

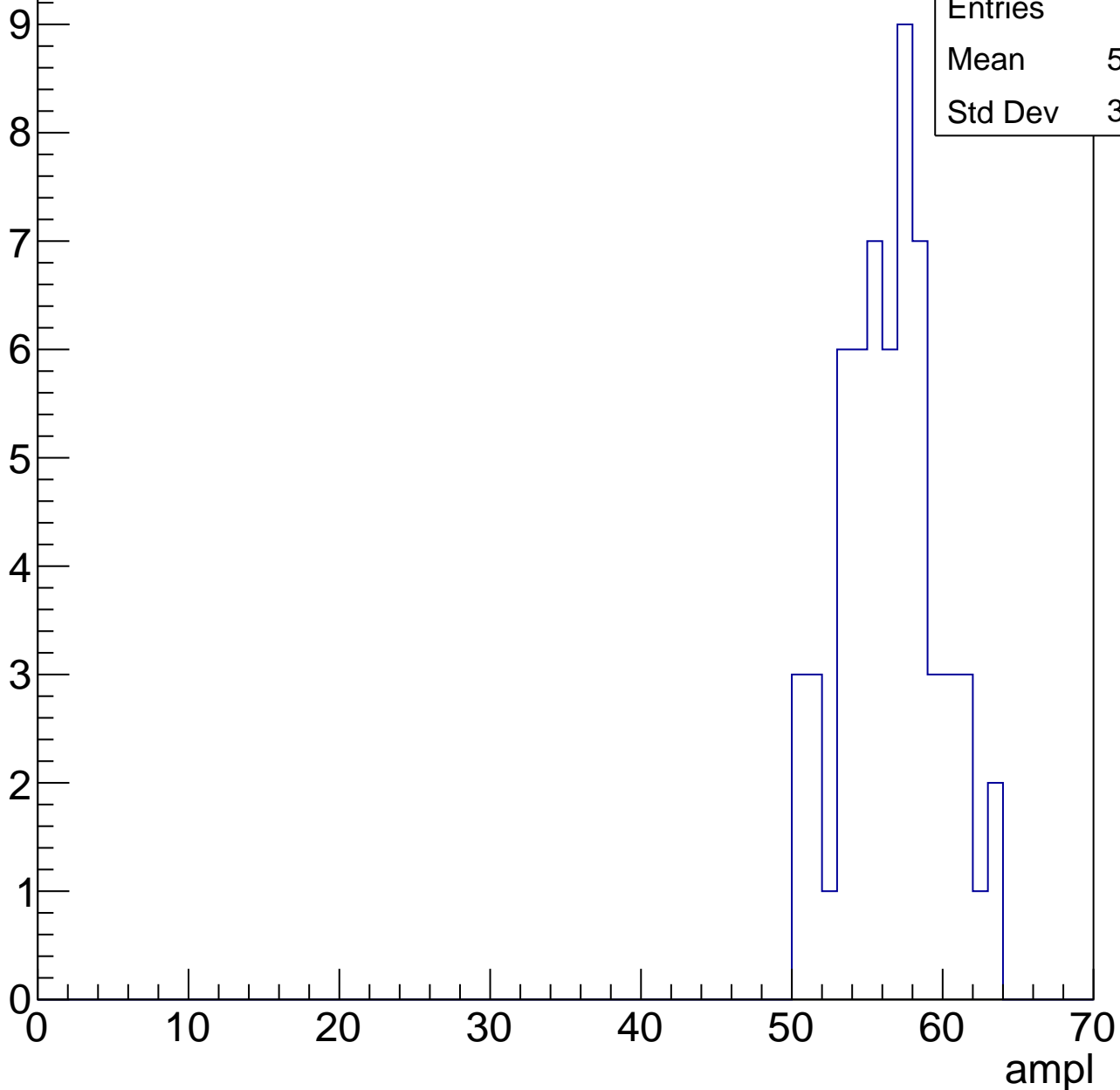


B1L103S, U11-ch33, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

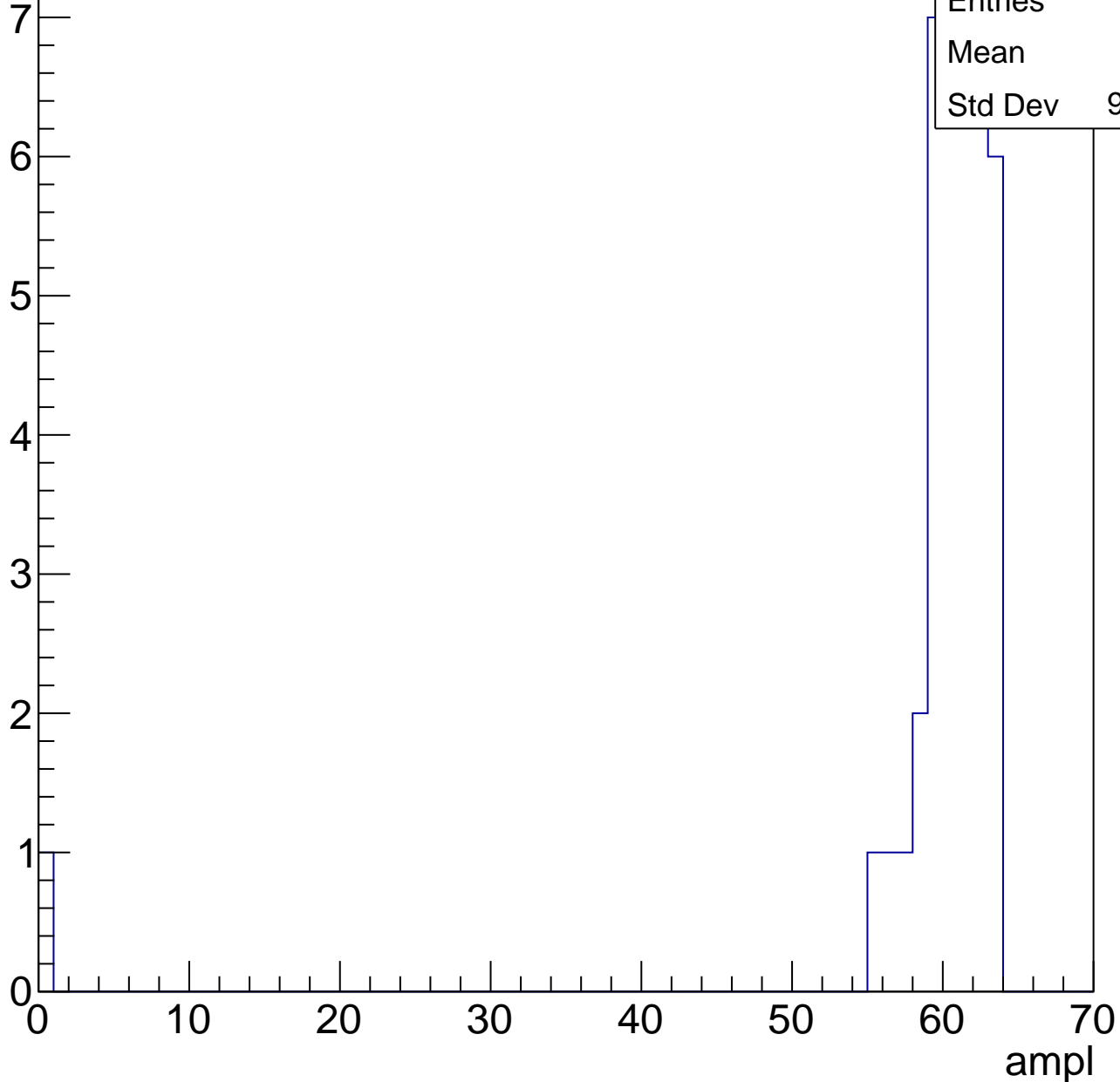
Entries	60
Mean	56.08
Std Dev	3.174



B1L103S, U11-ch33, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch33, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	4
Mean	62.5
Std Dev	0.5

0 10 20 30 40 50 60 70

ampl

B1L103S, U11-ch33, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	19
Mean	0
Std Dev	0

B1L103S, U11-ch34, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	98
Mean	25.71
Std Dev	9.881

Entry

10

8

6

4

2

0

0

10

20

30

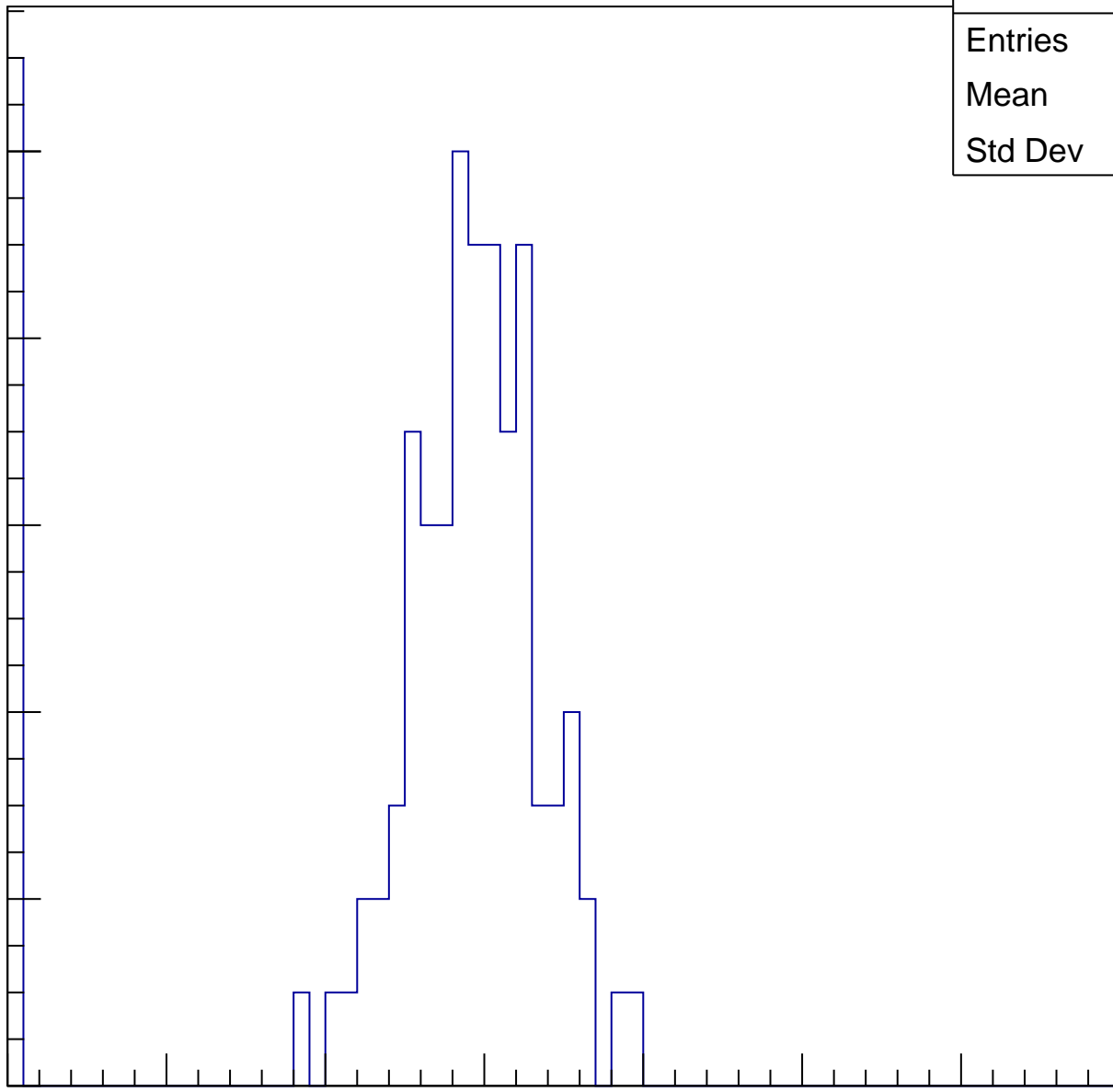
40

50

60

70

ampl



B1L103S, U11-ch34, adc1

calib_packv5_041523_1651.root, FC#0, port C2

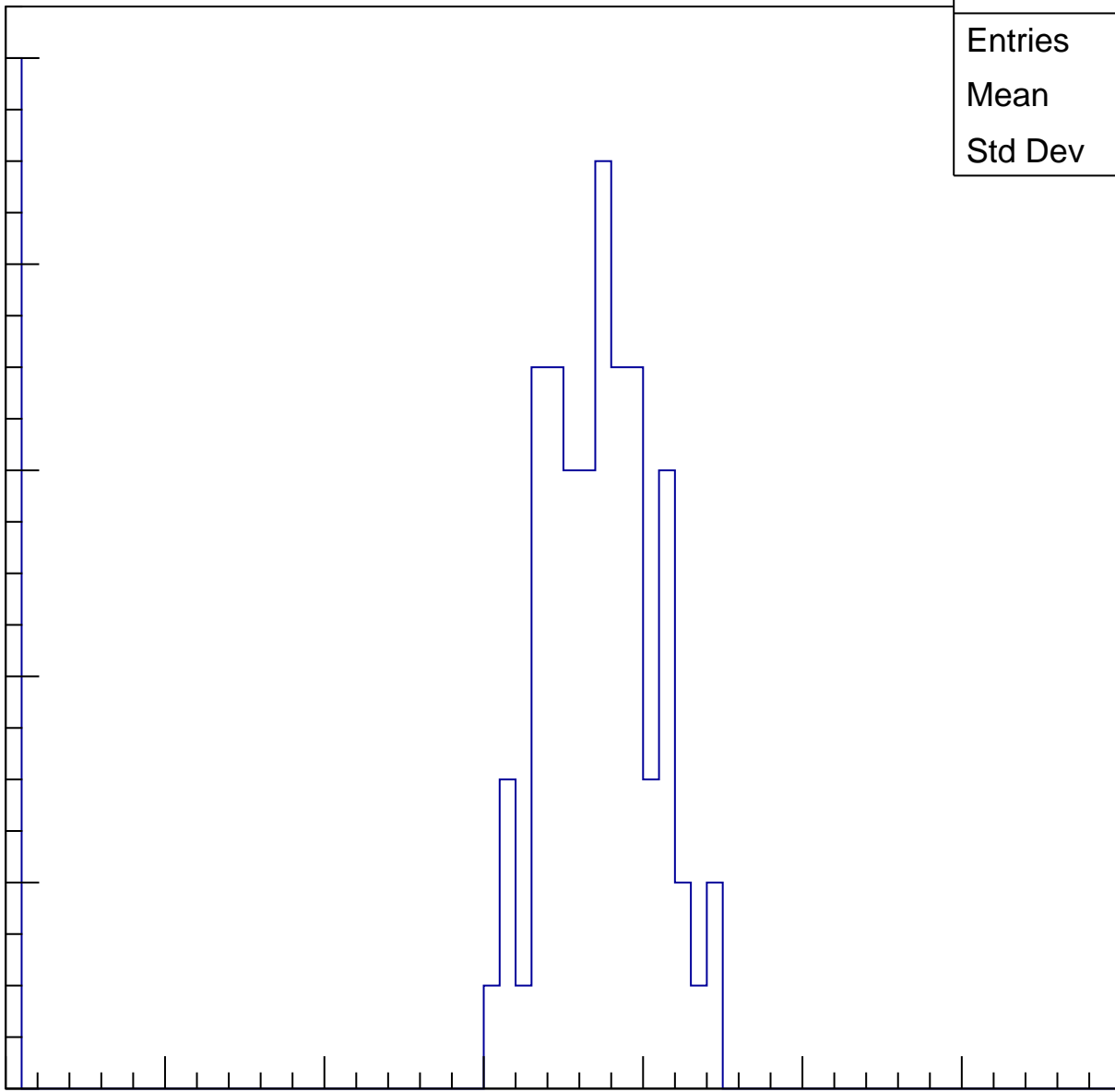
Entries	78
Mean	32.09
Std Dev	12.68

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

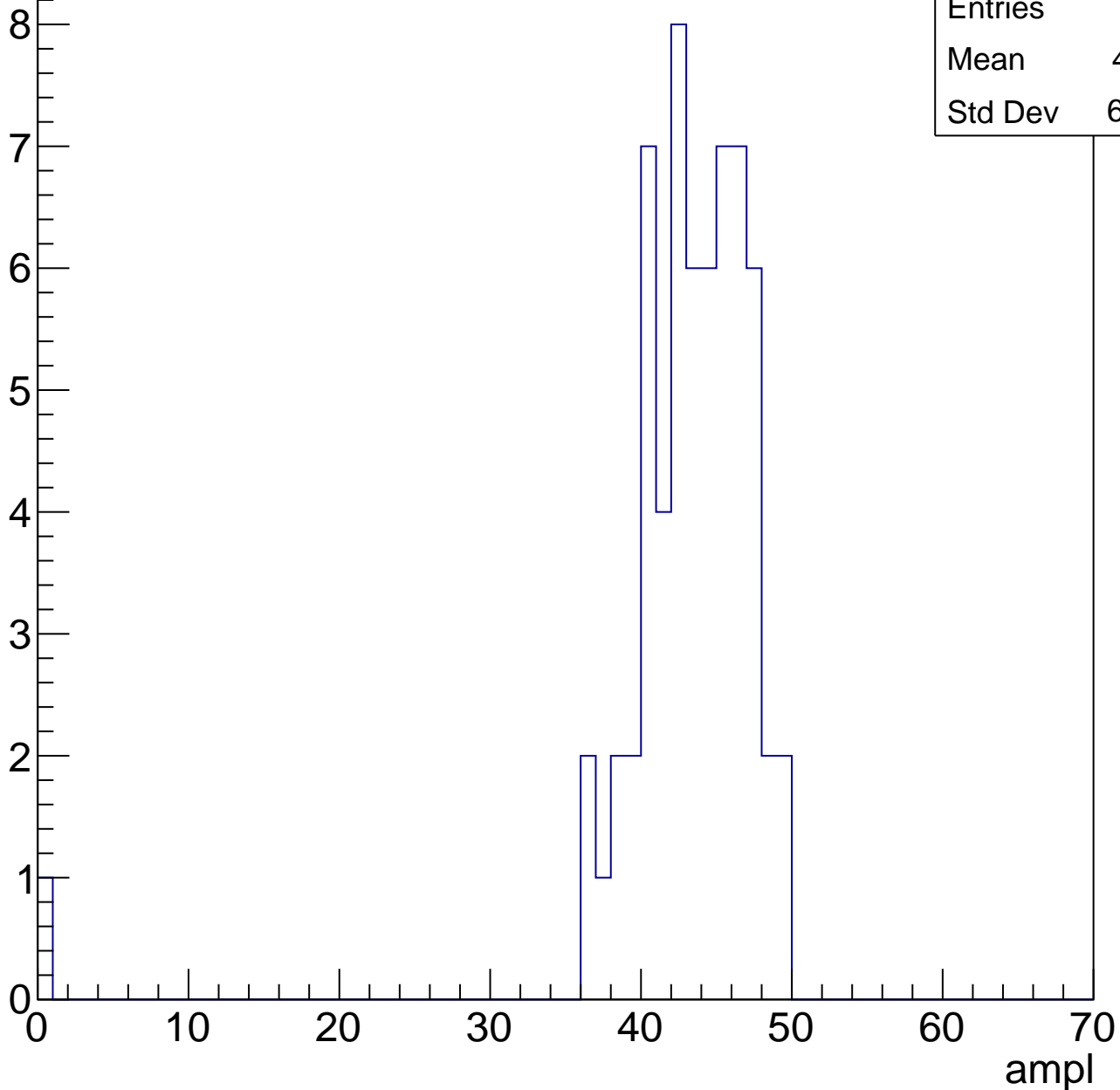


B1L103S, U11-ch34, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

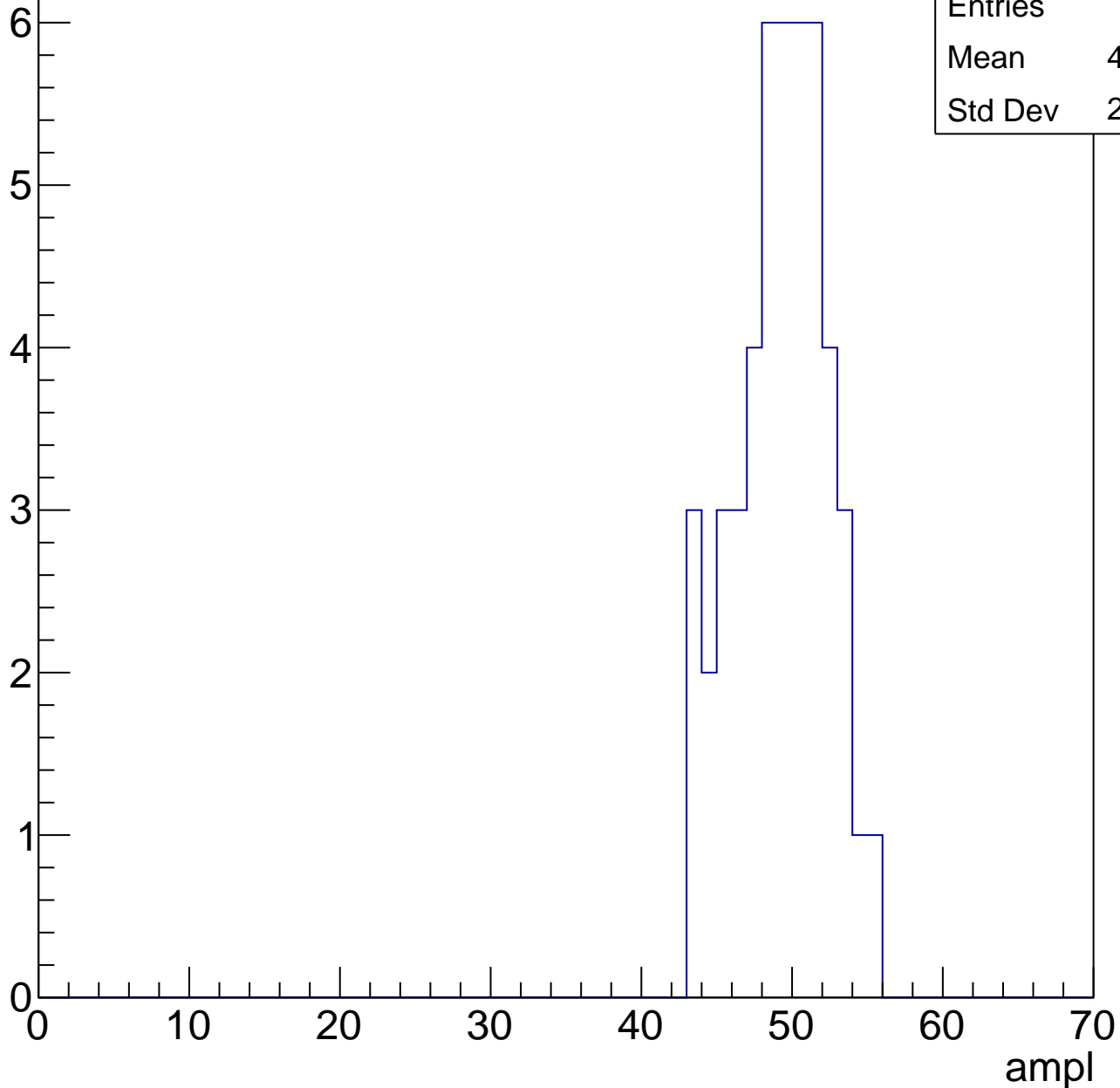
Entries	63
Mean	42.51
Std Dev	6.238



B1L103S, U11-ch34, adc3

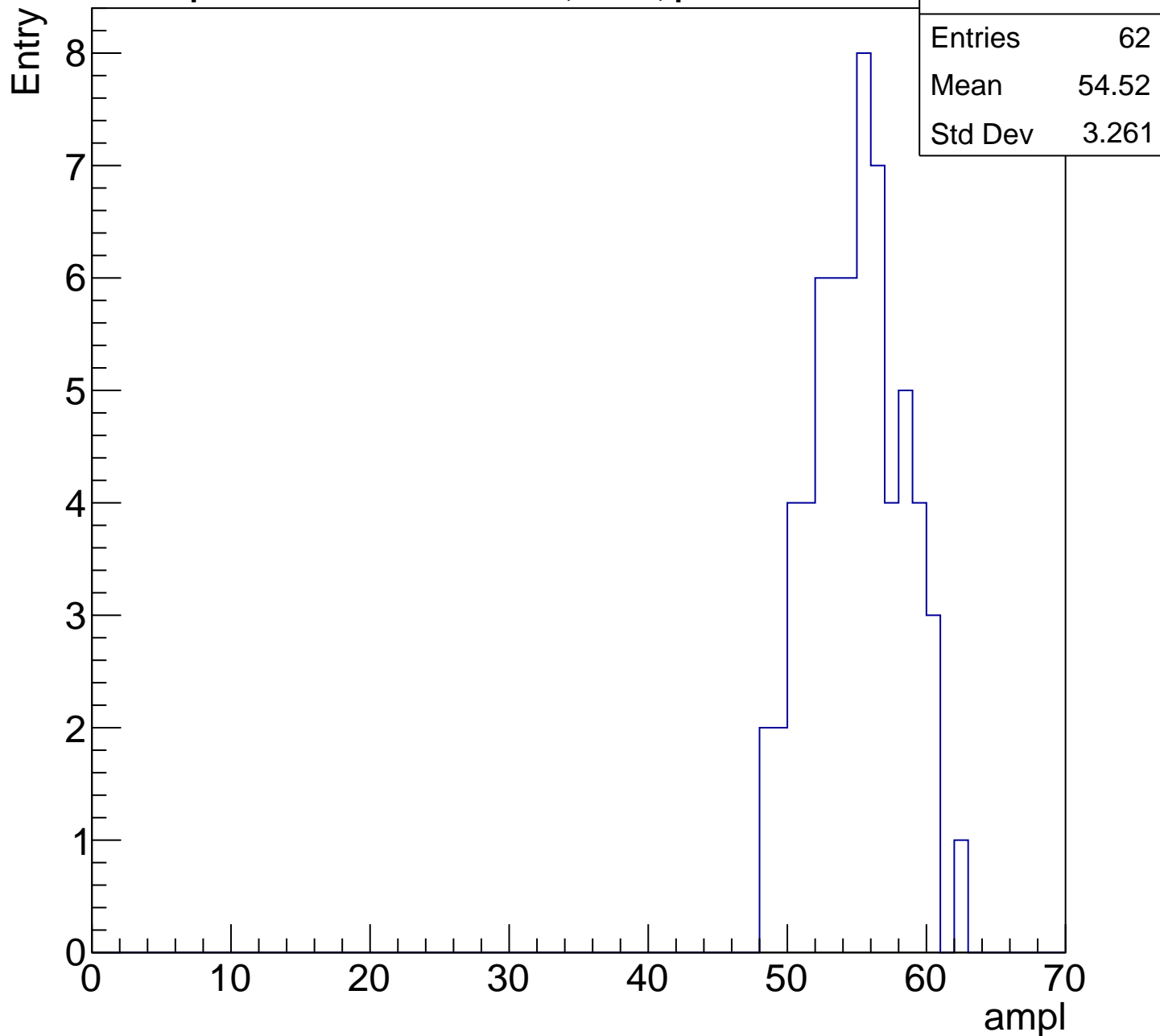
calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch34, adc4

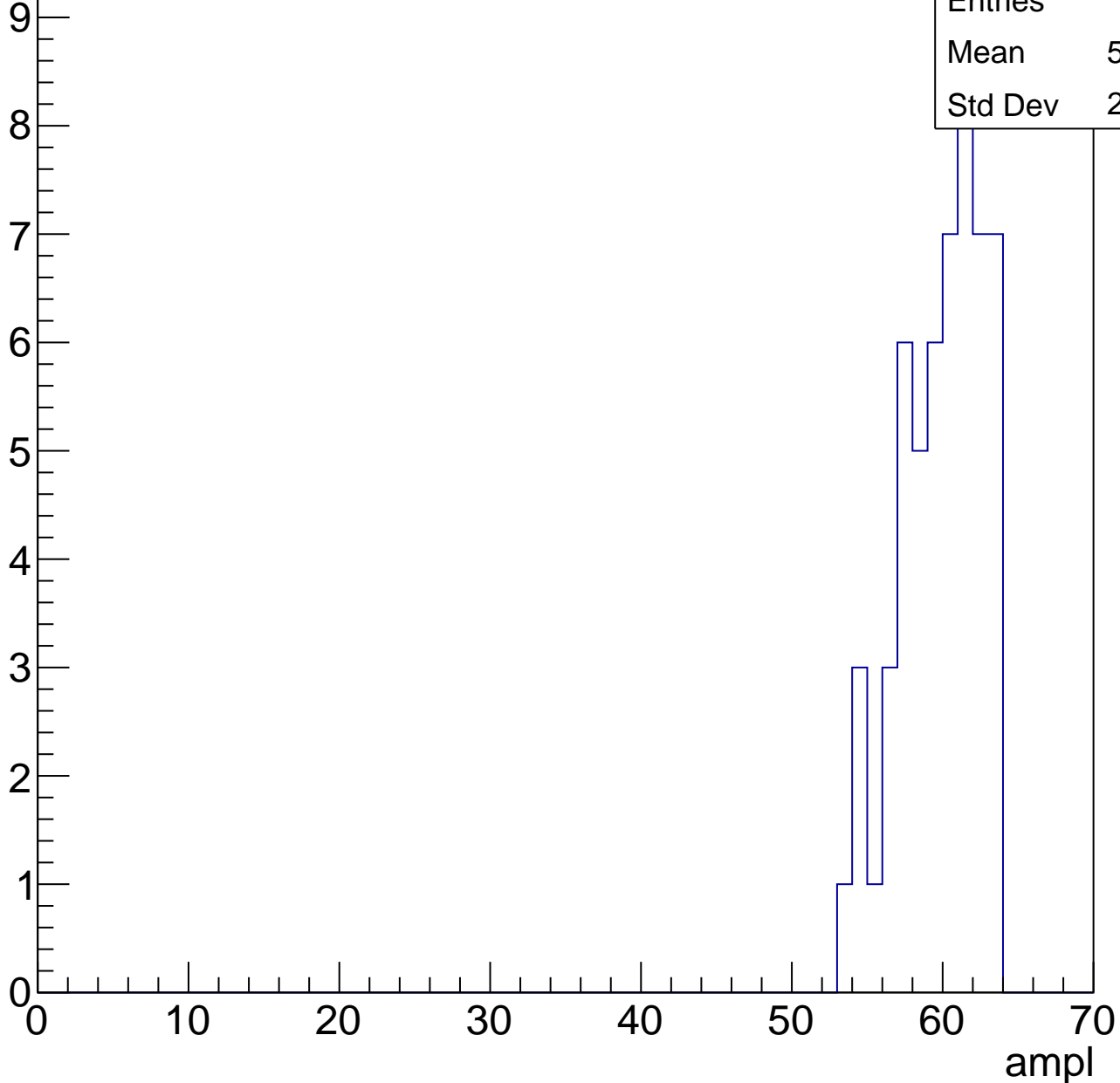
calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U11-ch34, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch34, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch34, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	19
Mean	0
Std Dev	0

B1L103S, U11-ch35, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	79
Mean	28.33
Std Dev	7.287

Entry

10
8
6
4
2
0

0

10

20

30

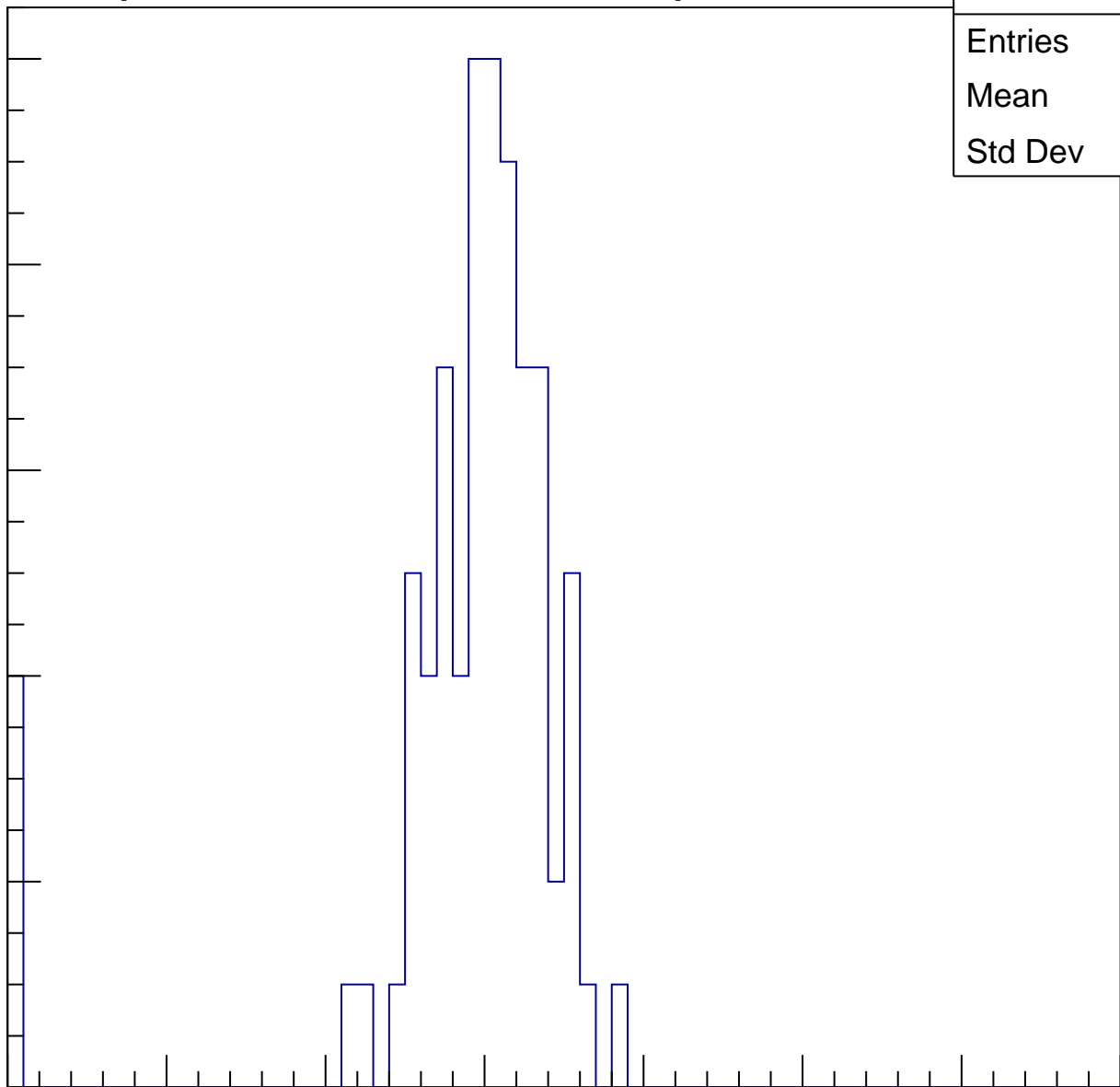
40

50

60

70

ampl

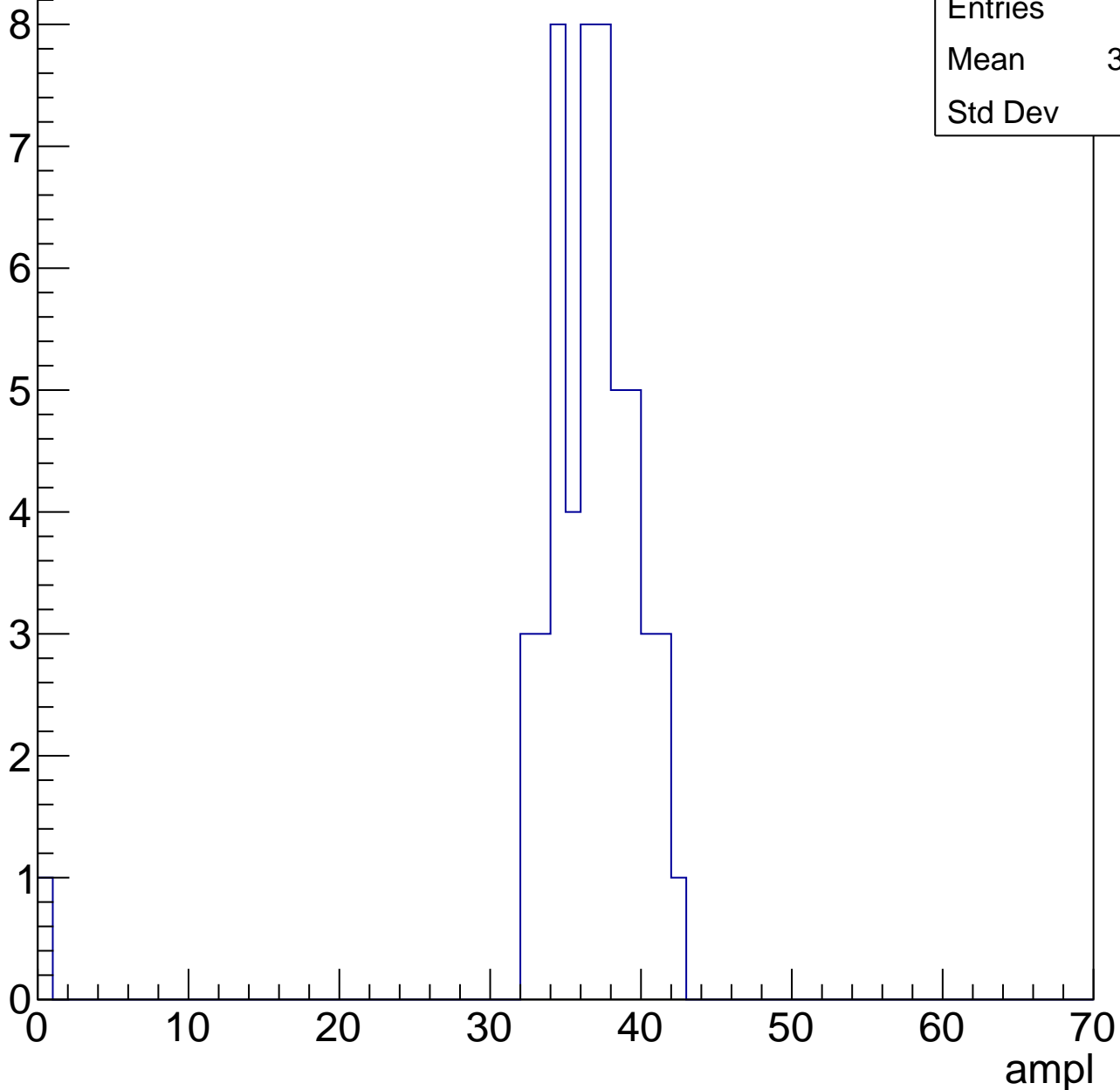


B1L103S, U11-ch35, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	35.79
Std Dev	5.61

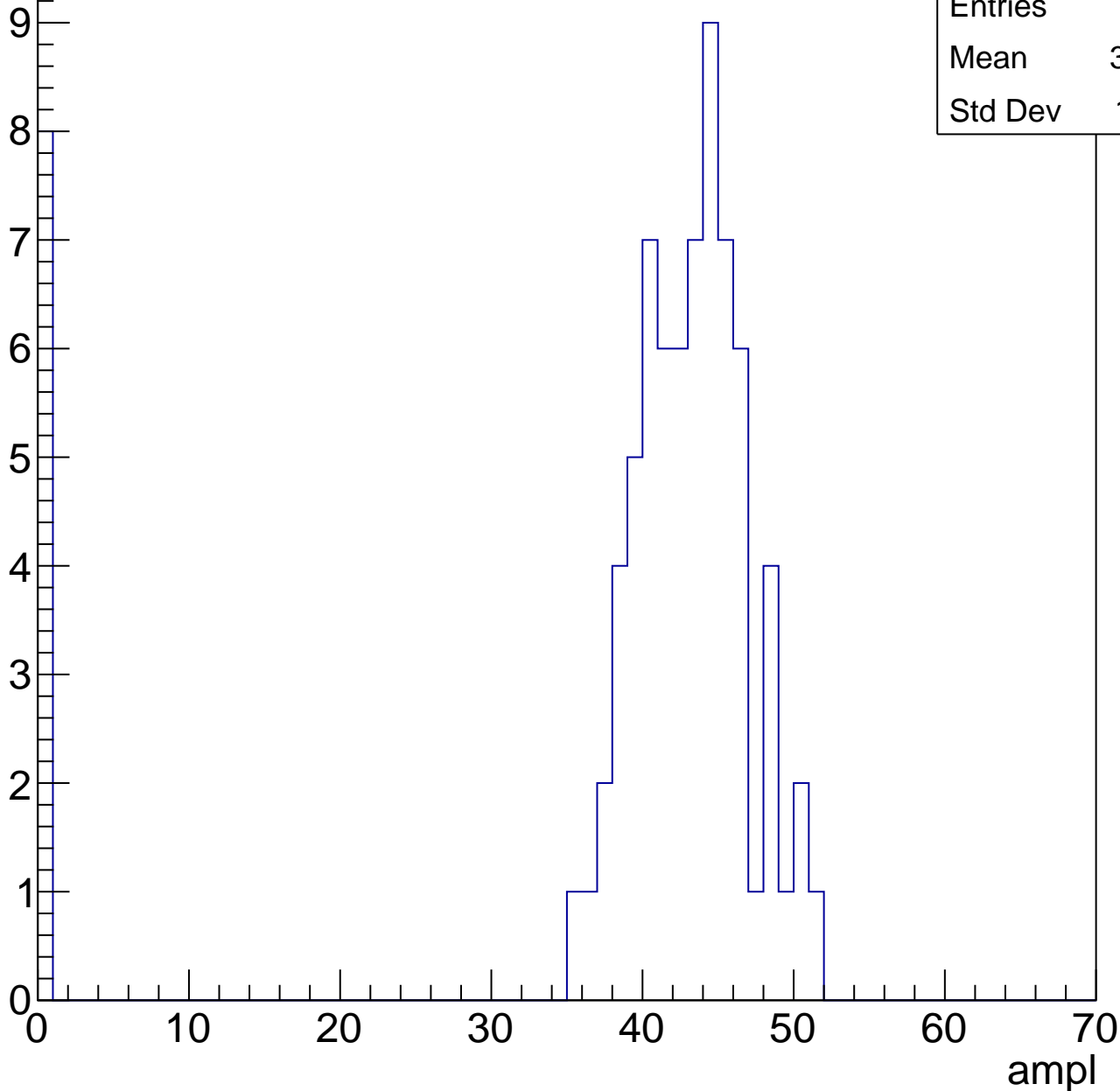


B1L103S, U11-ch35, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	38.42
Std Dev	13.41

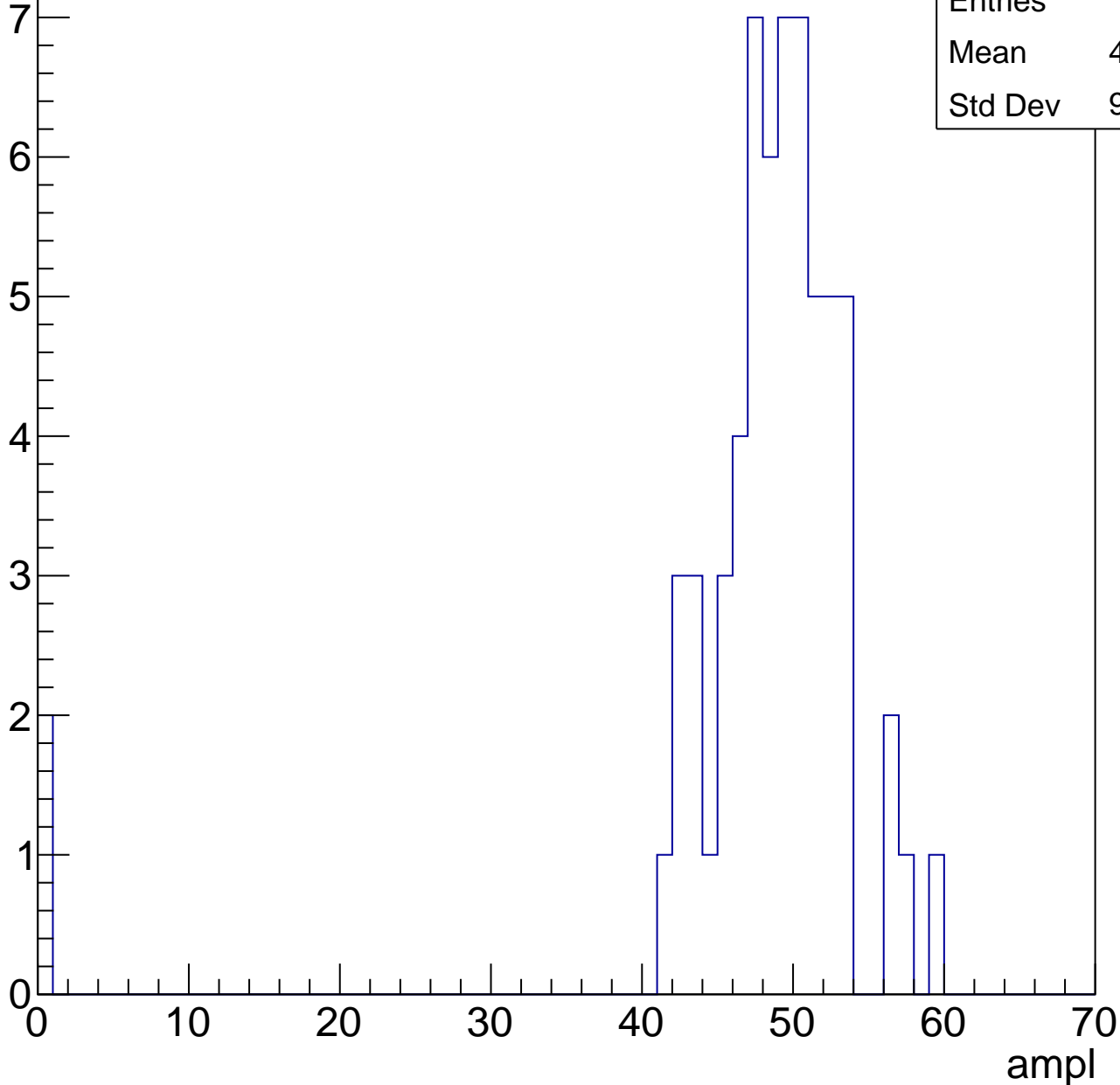


B1L103S, U11-ch35, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	47.25
Std Dev	9.332



B1L103S, U11-ch35, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	63
Mean	55.17
Std Dev	3.36

Entry

10

8

6

4

2

0

0

10

20

30

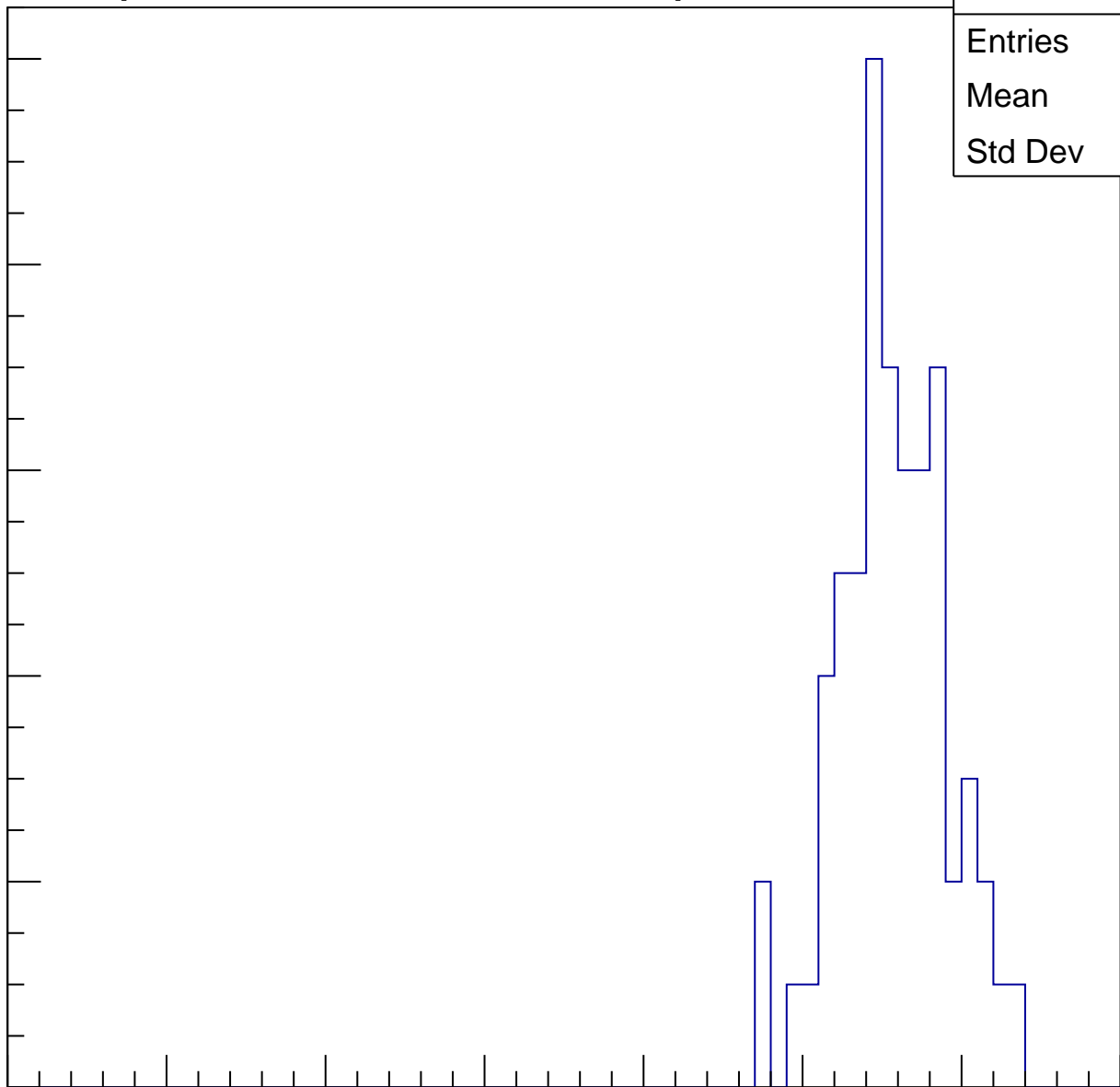
40

50

60

70

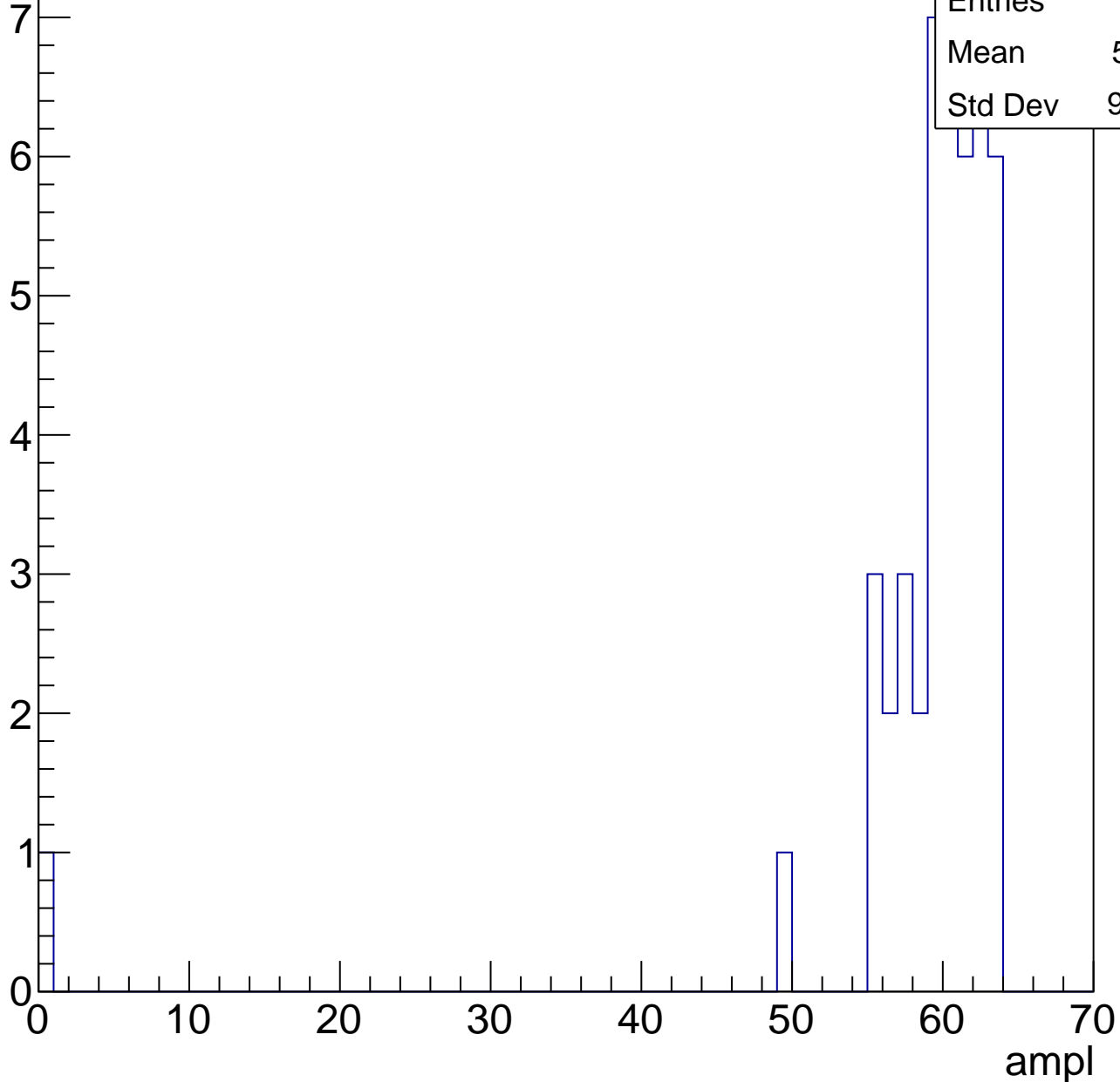
ampl



B1L103S, U11-ch35, adc5

calib_packv5_041523_1651.root, FC#0, port C2

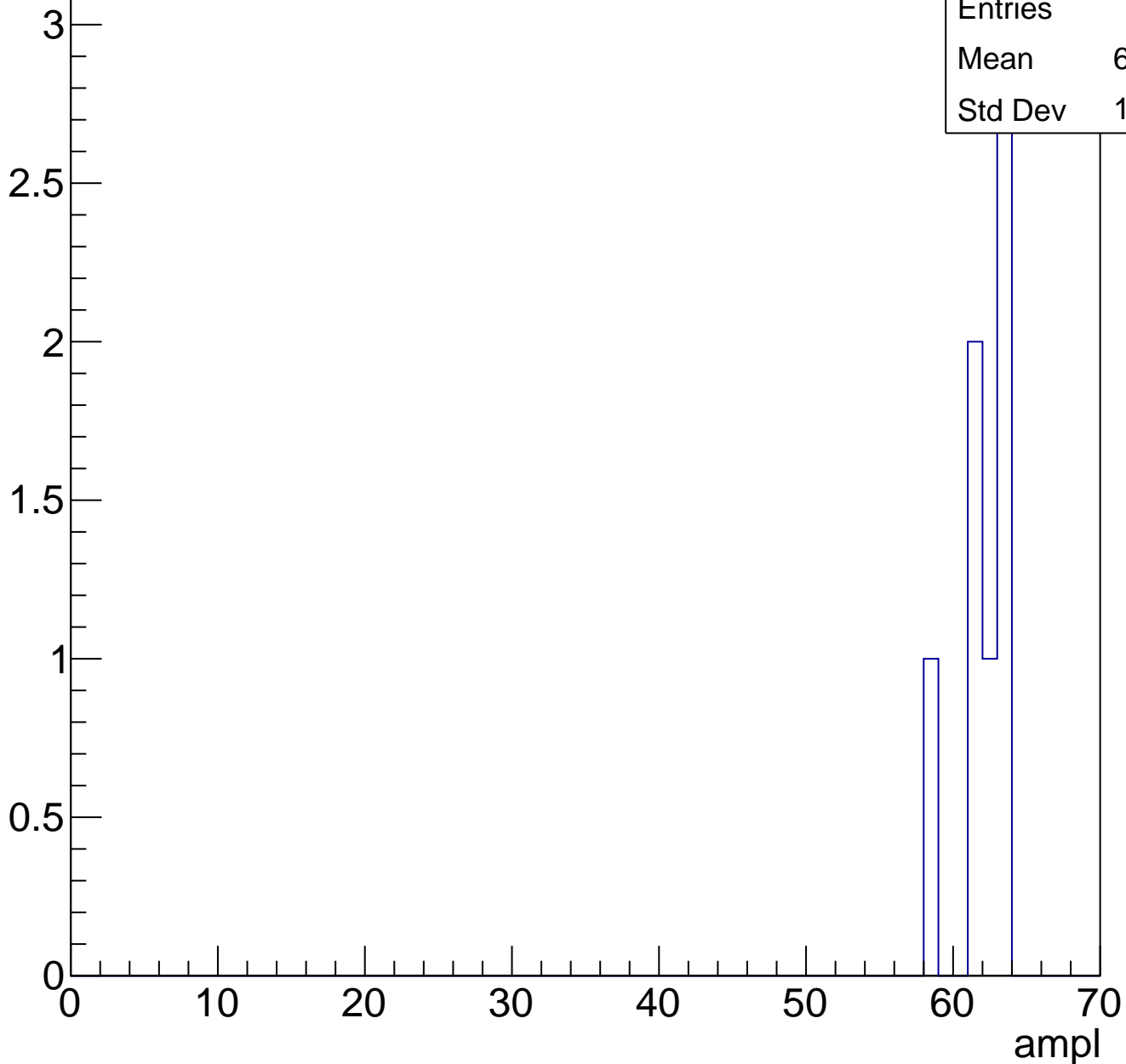
Entry



B1L103S, U11-ch35, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch35, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51

Entry

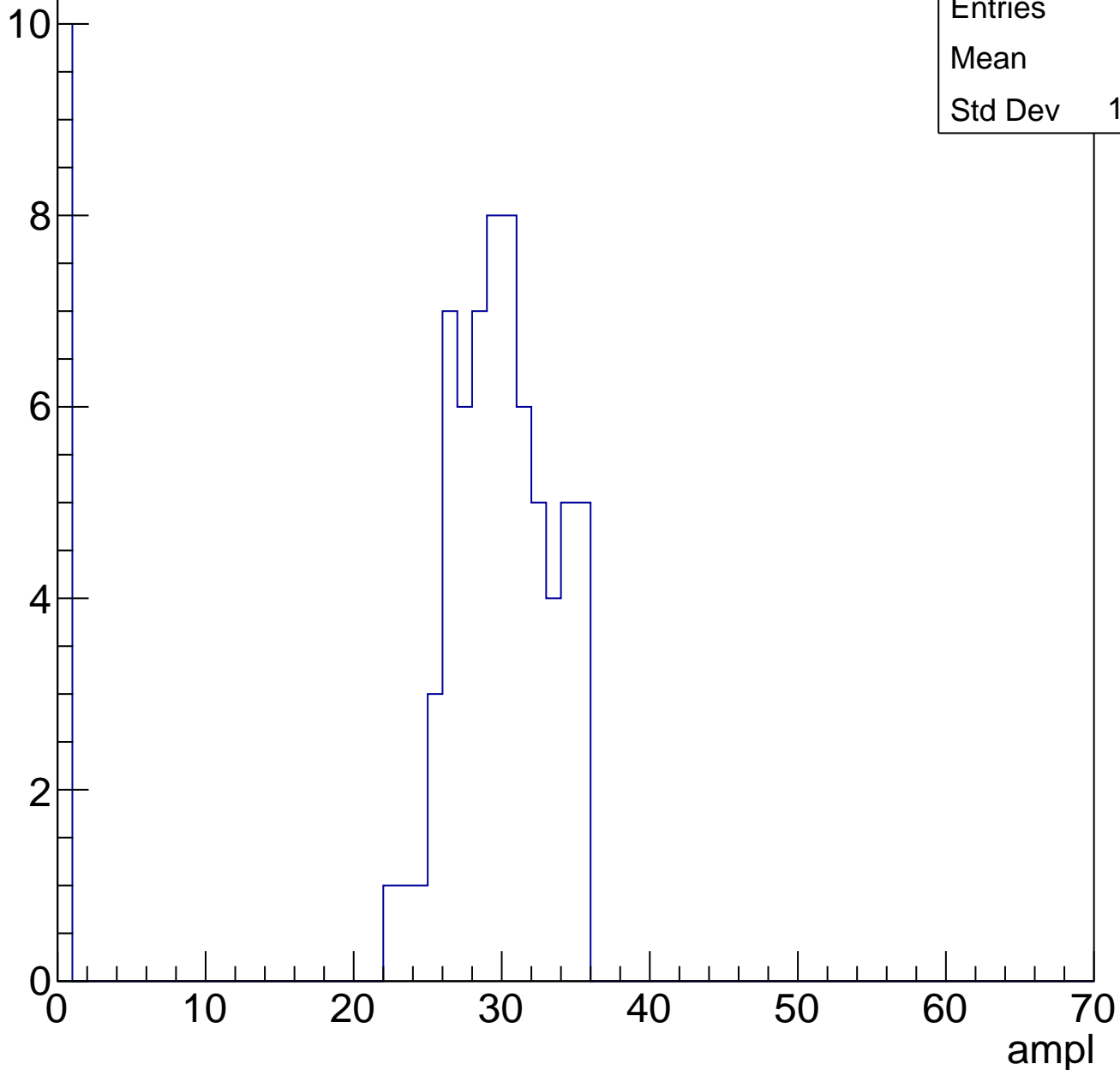


B1L103S, U11-ch36, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	77
Mean	25.7
Std Dev	10.36

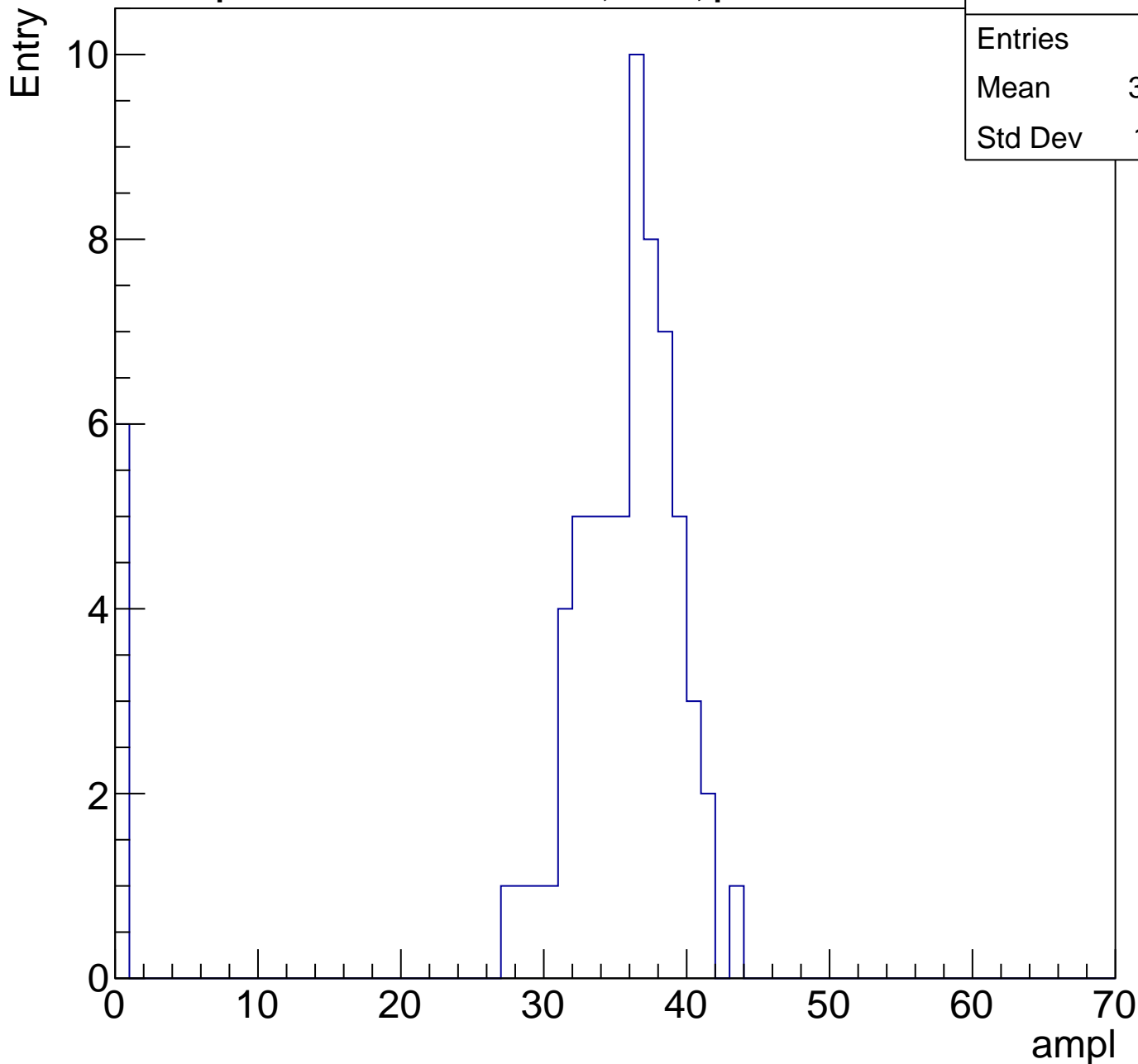
Entry



B1L103S, U11-ch36, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	70
Mean	32.43
Std Dev	10.41

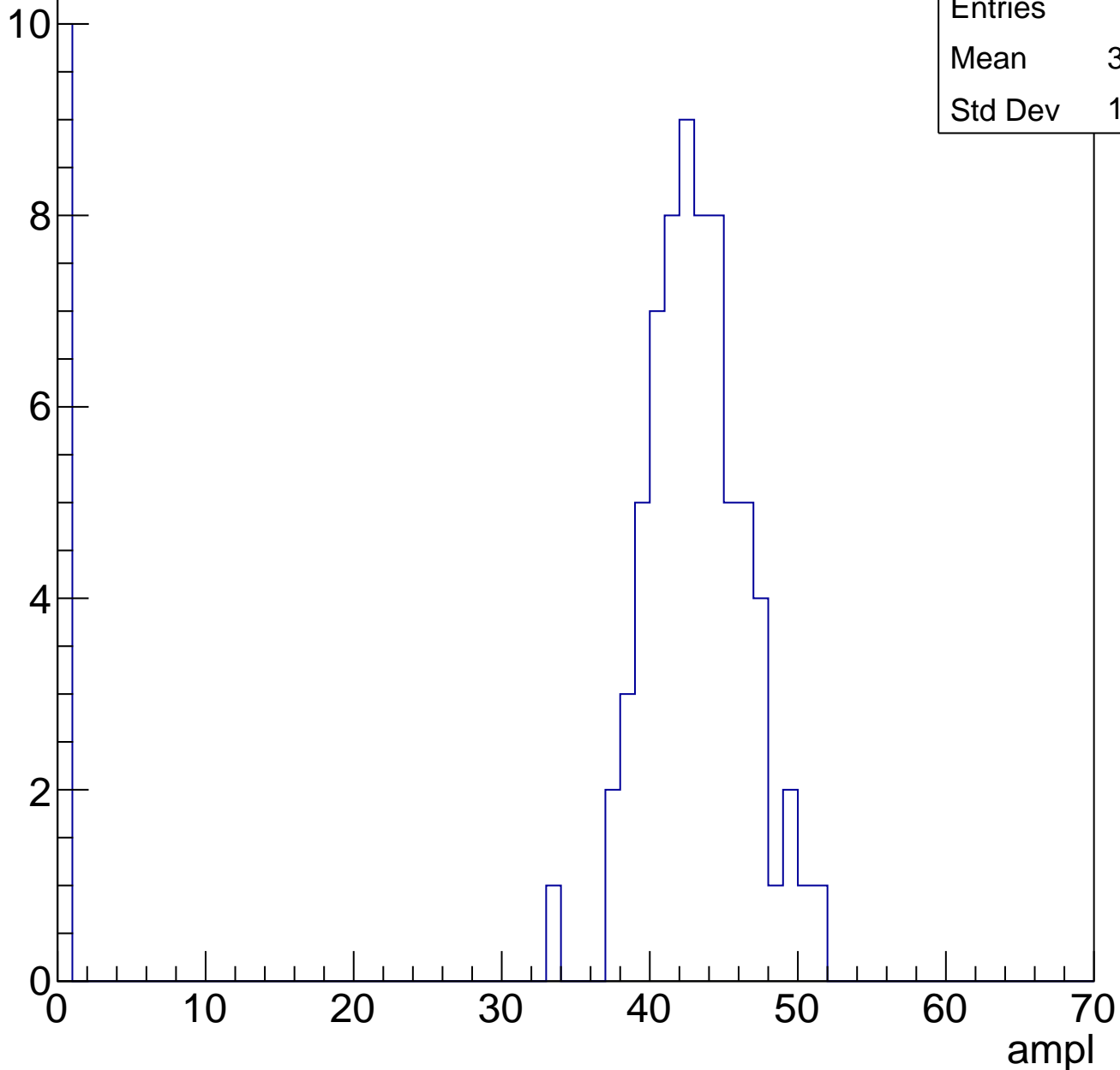


B1L103S, U11-ch36, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	37.35
Std Dev	14.45

Entry

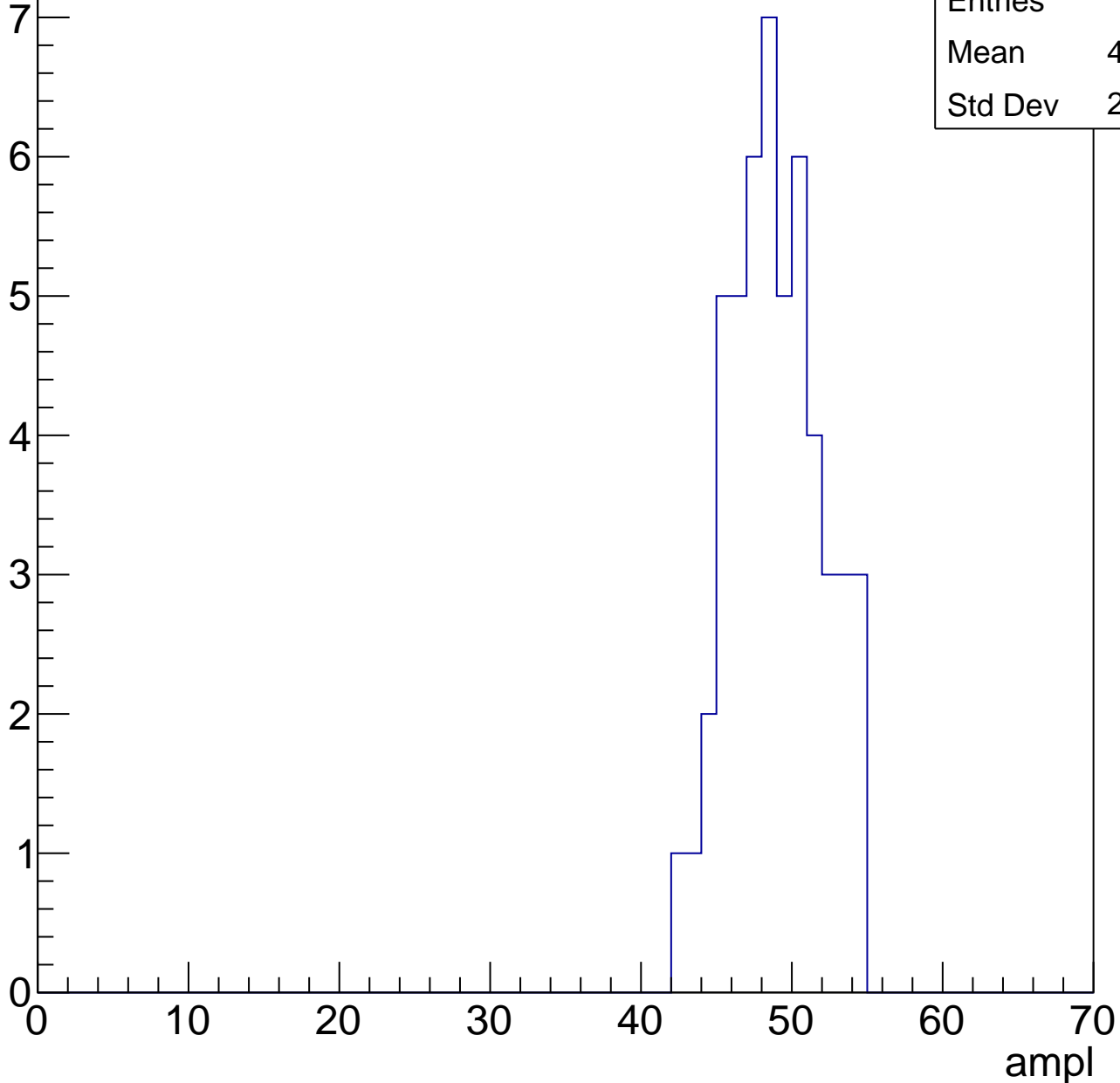


B1L103S, U11-ch36, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	48.47
Std Dev	2.966

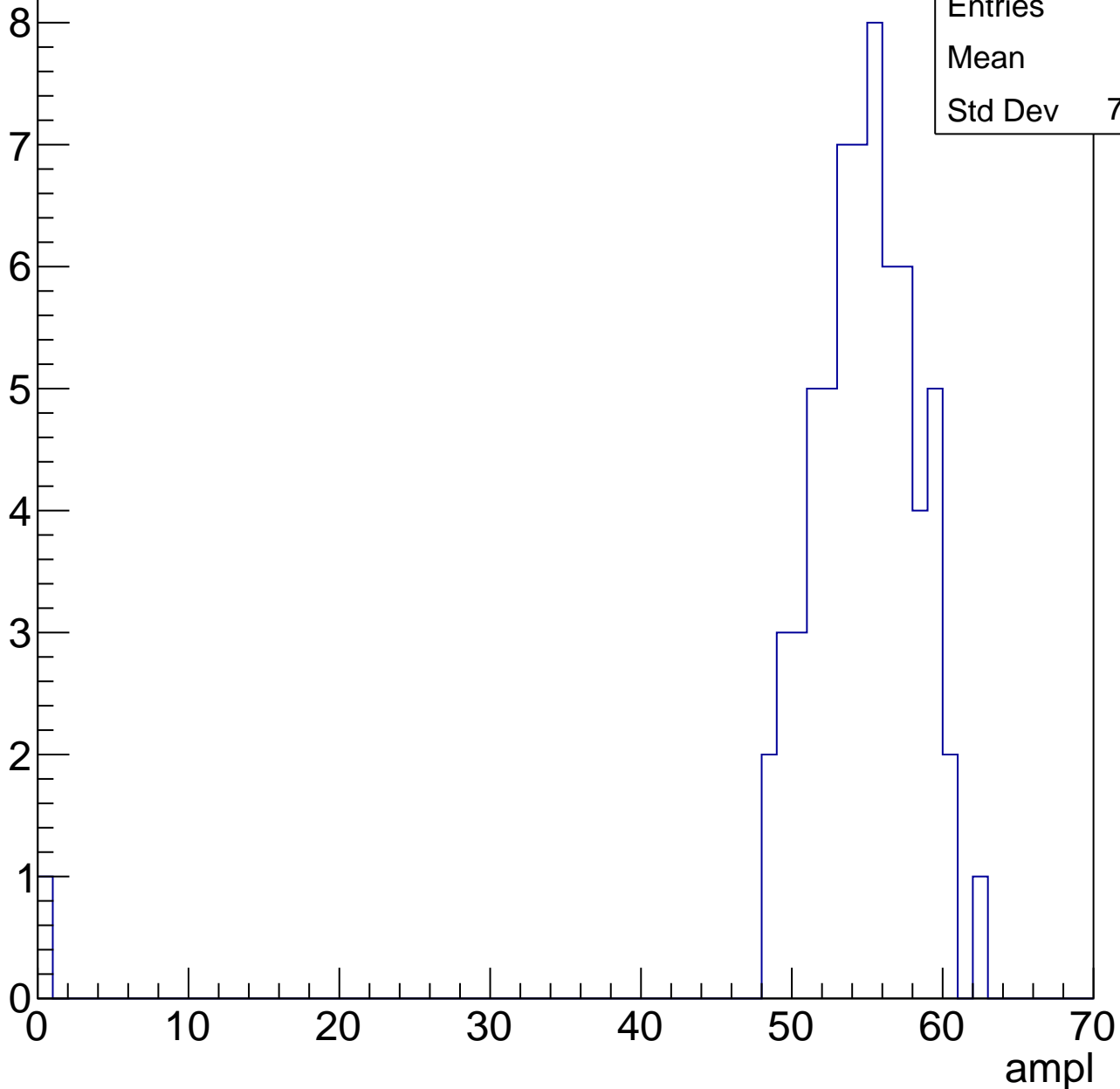


B1L103S, U11-ch36, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	53.6
Std Dev	7.425



B1L103S, U11-ch36, adc5

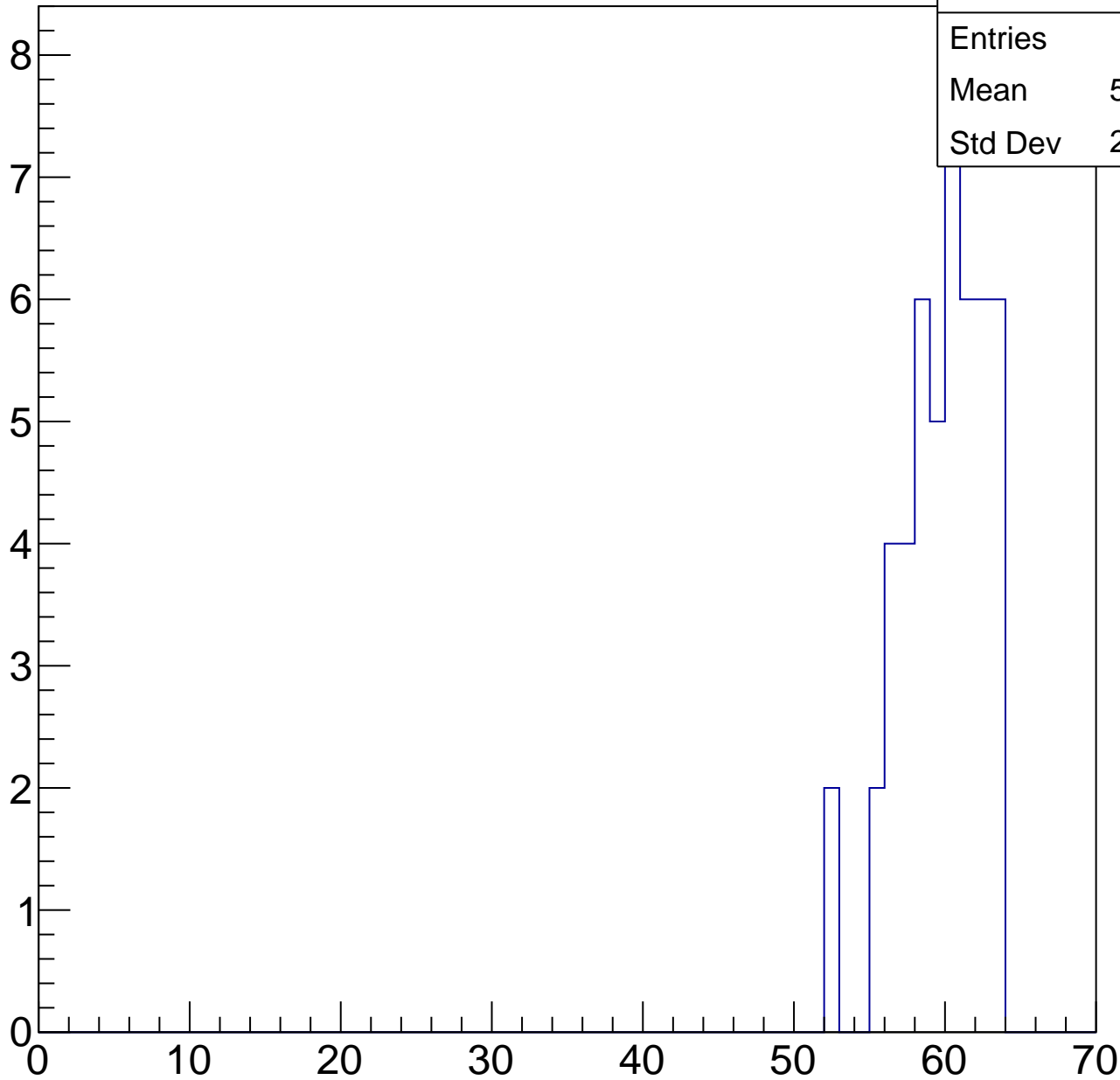
calib_packv5_041523_1651.root, FC#0, port C2

Entry

8
7
6
5
4
3
2
1
0

Entries	49
Mean	59.29
Std Dev	2.733

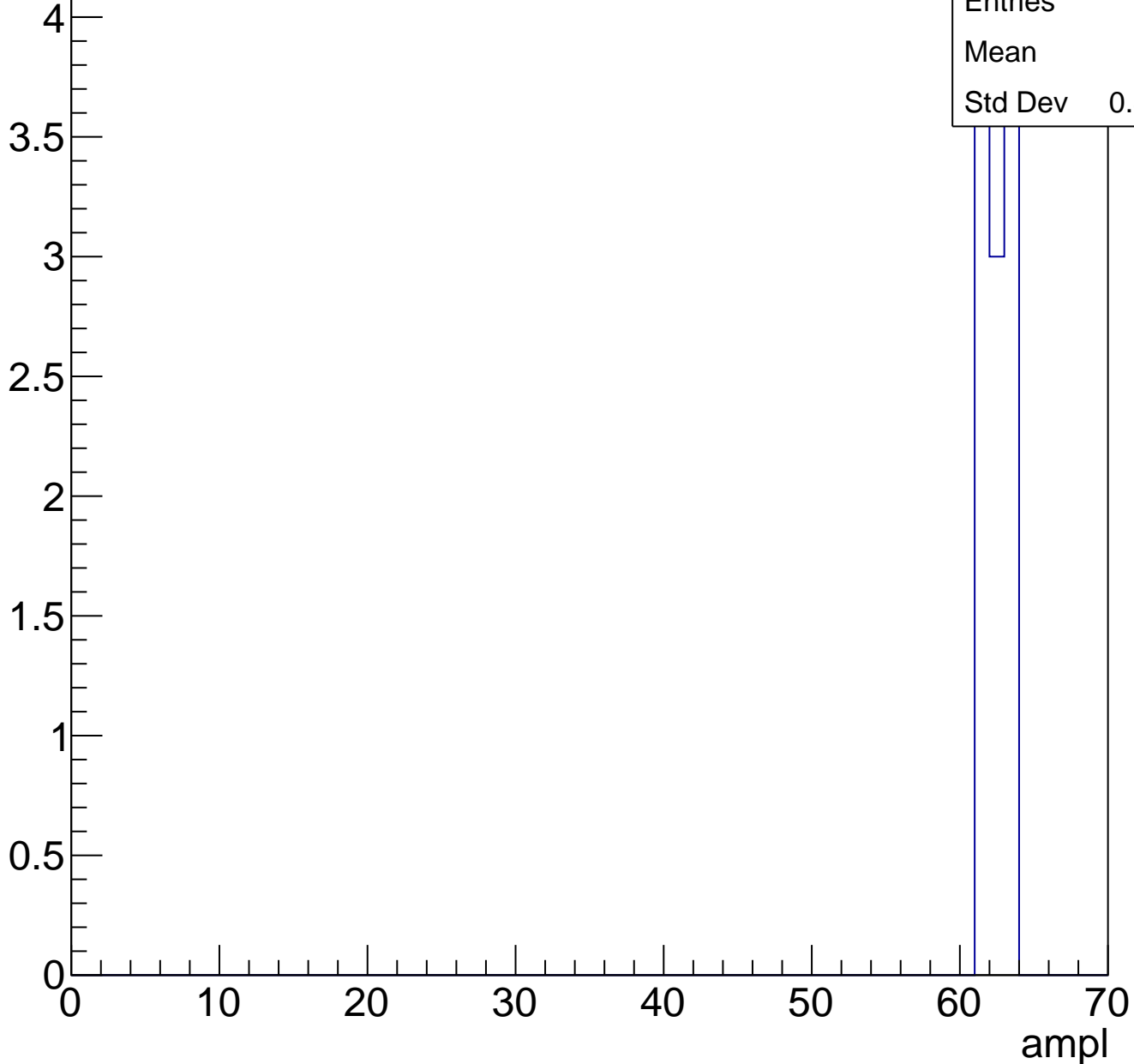
ampl



B1L103S, U11-ch36, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch36, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch37, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	24.78
Std Dev	11.17

Entry

12

10

8

6

4

2

0

0

10

20

30

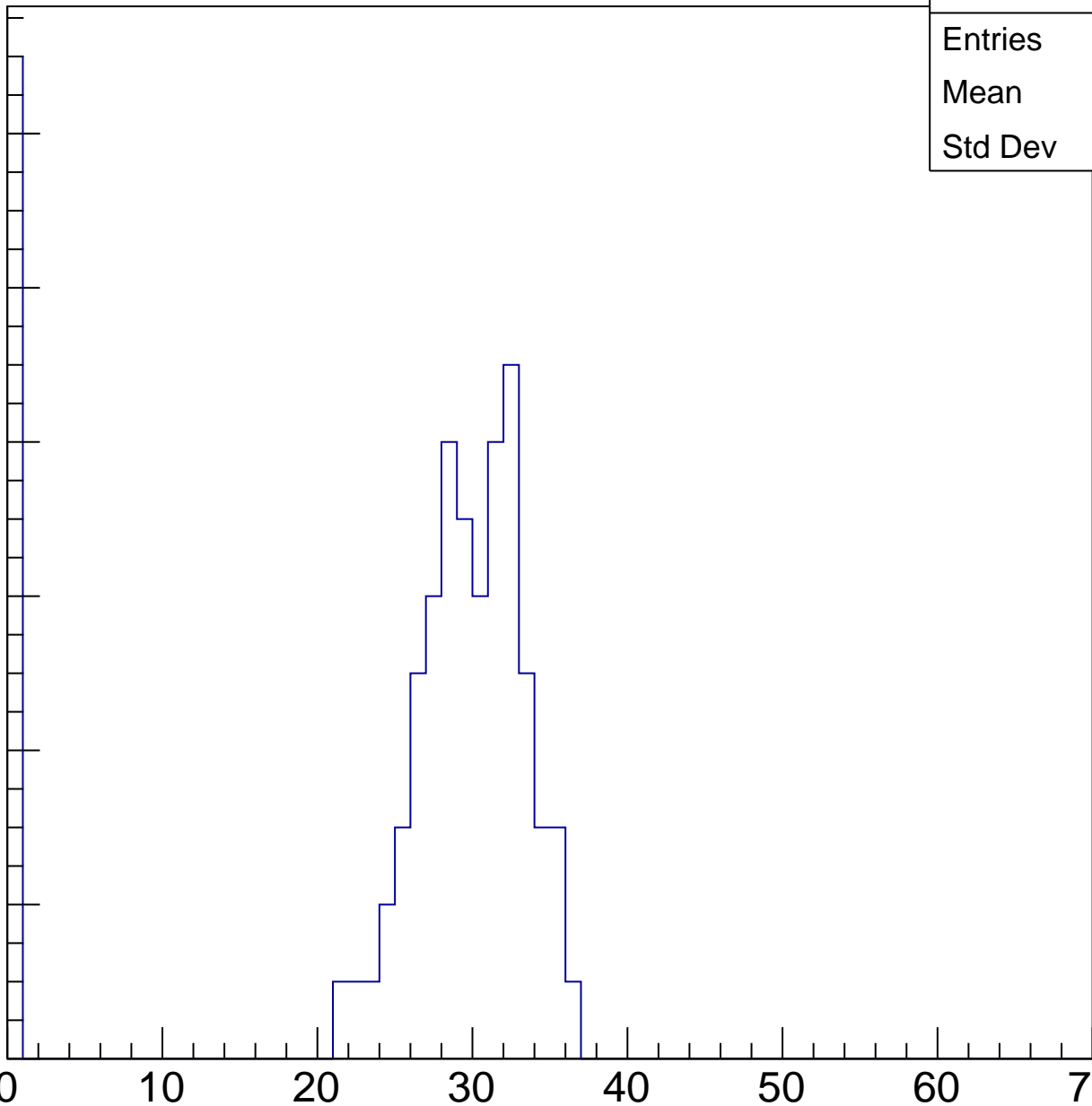
40

50

60

70

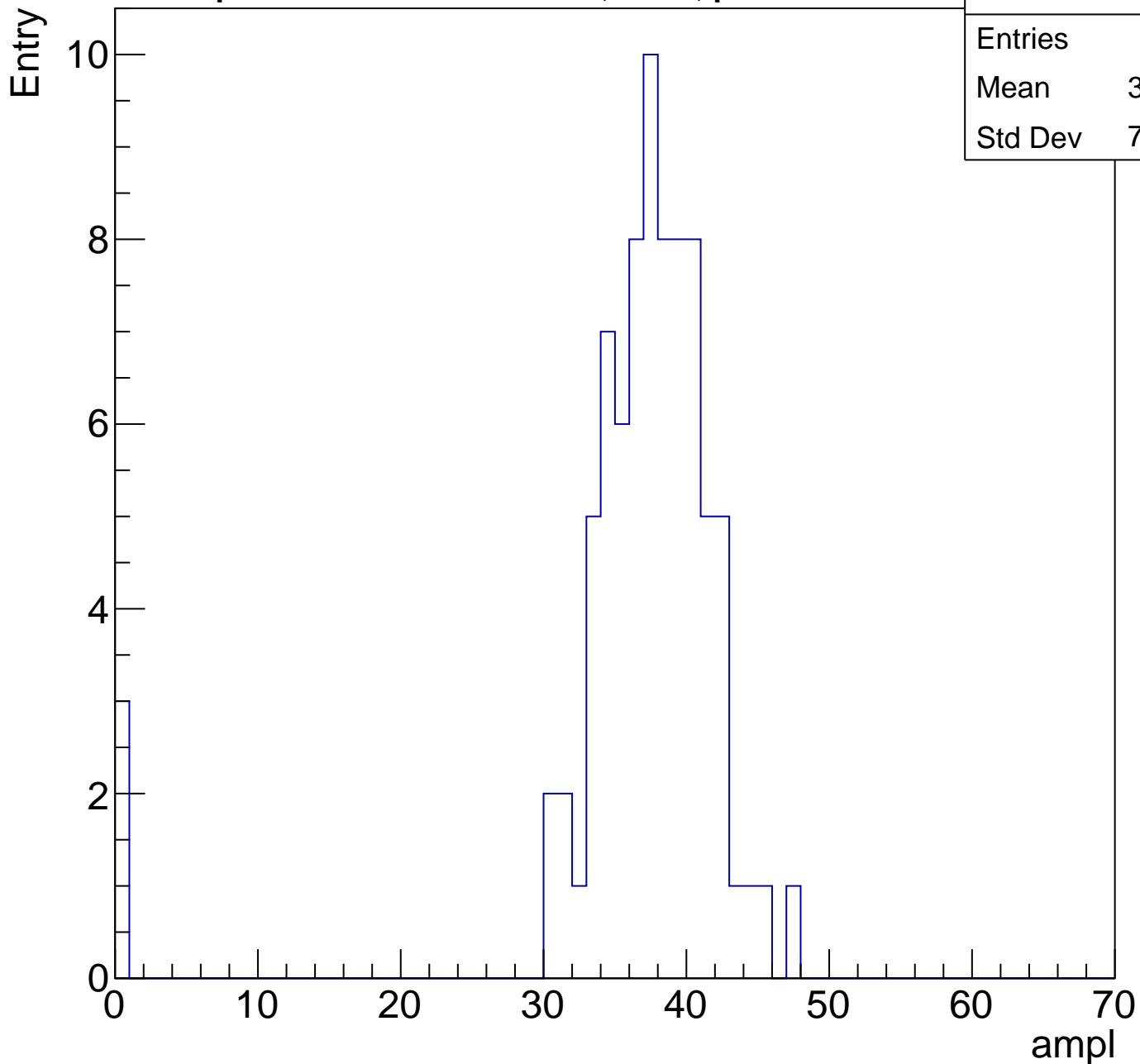
ampl



B1L103S, U11-ch37, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	36.04
Std Dev	7.783

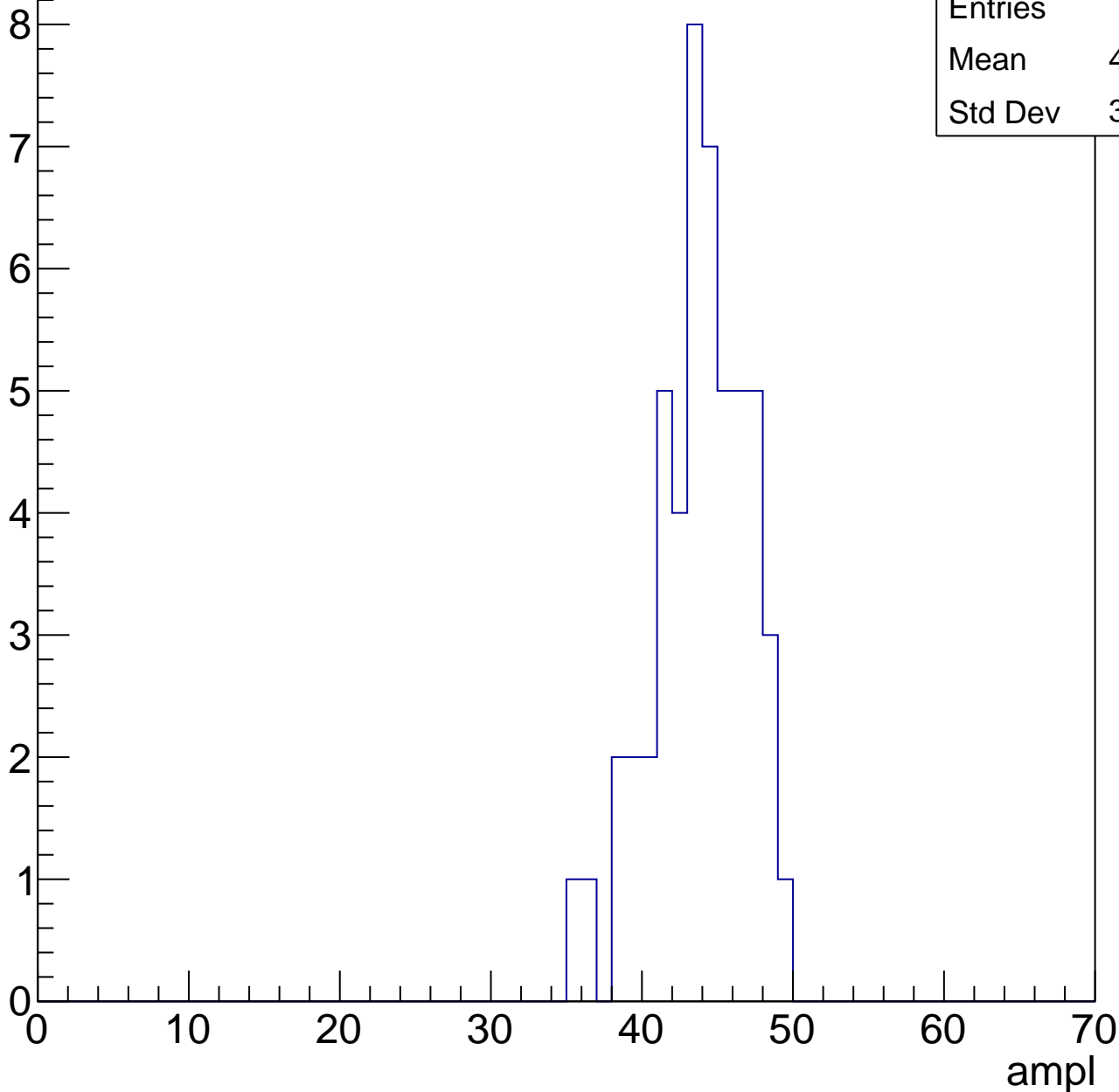


B1L103S, U11-ch37, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	43.39
Std Dev	3.106



B1L103S, U11-ch37, adc3

calib_packv5_041523_1651.root, FC#0, port C2

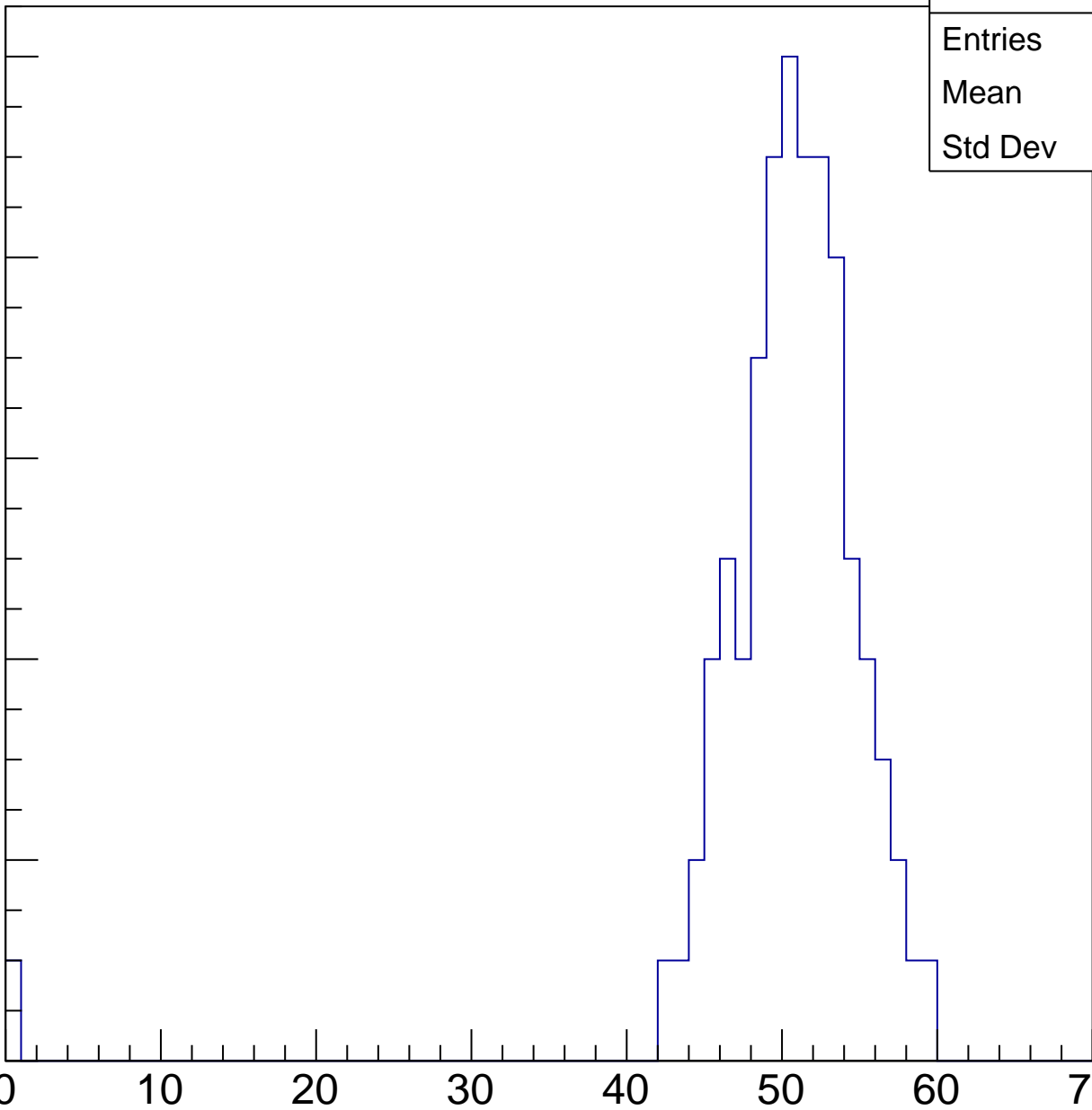
Entries	86
Mean	49.86
Std Dev	6.456

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

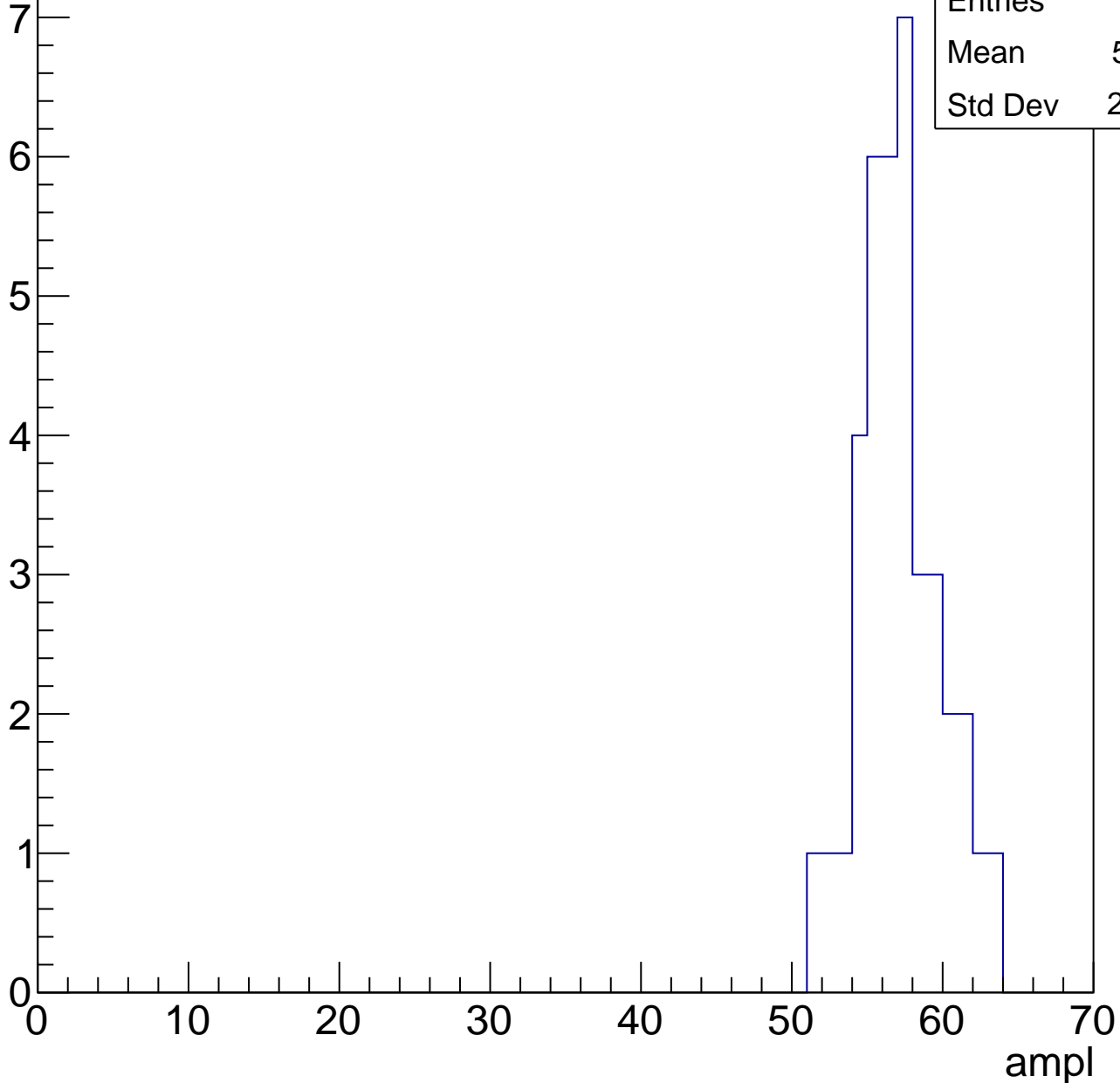


B1L103S, U11-ch37, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	38
Mean	56.71
Std Dev	2.645

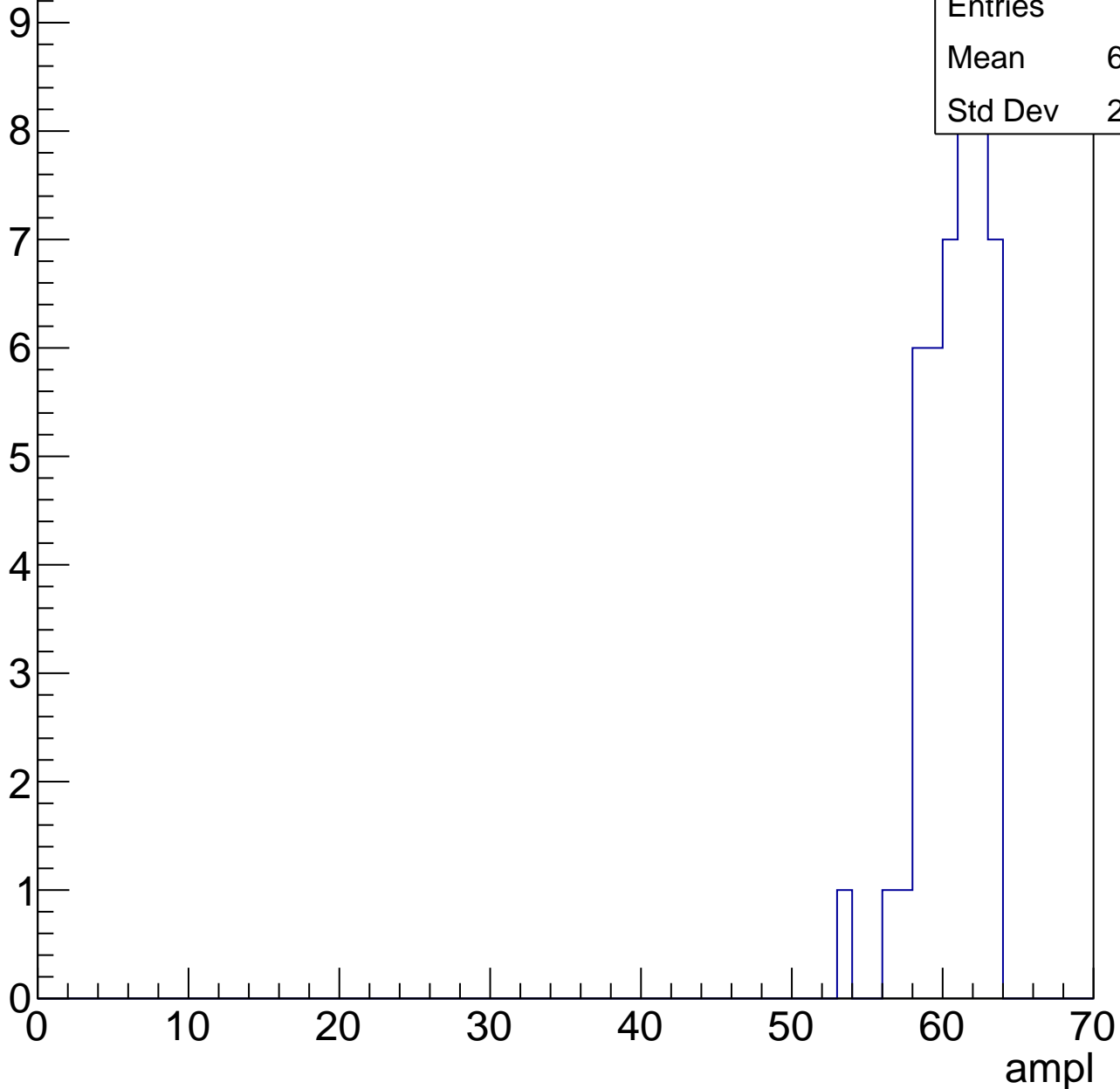


B1L103S, U11-ch37, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

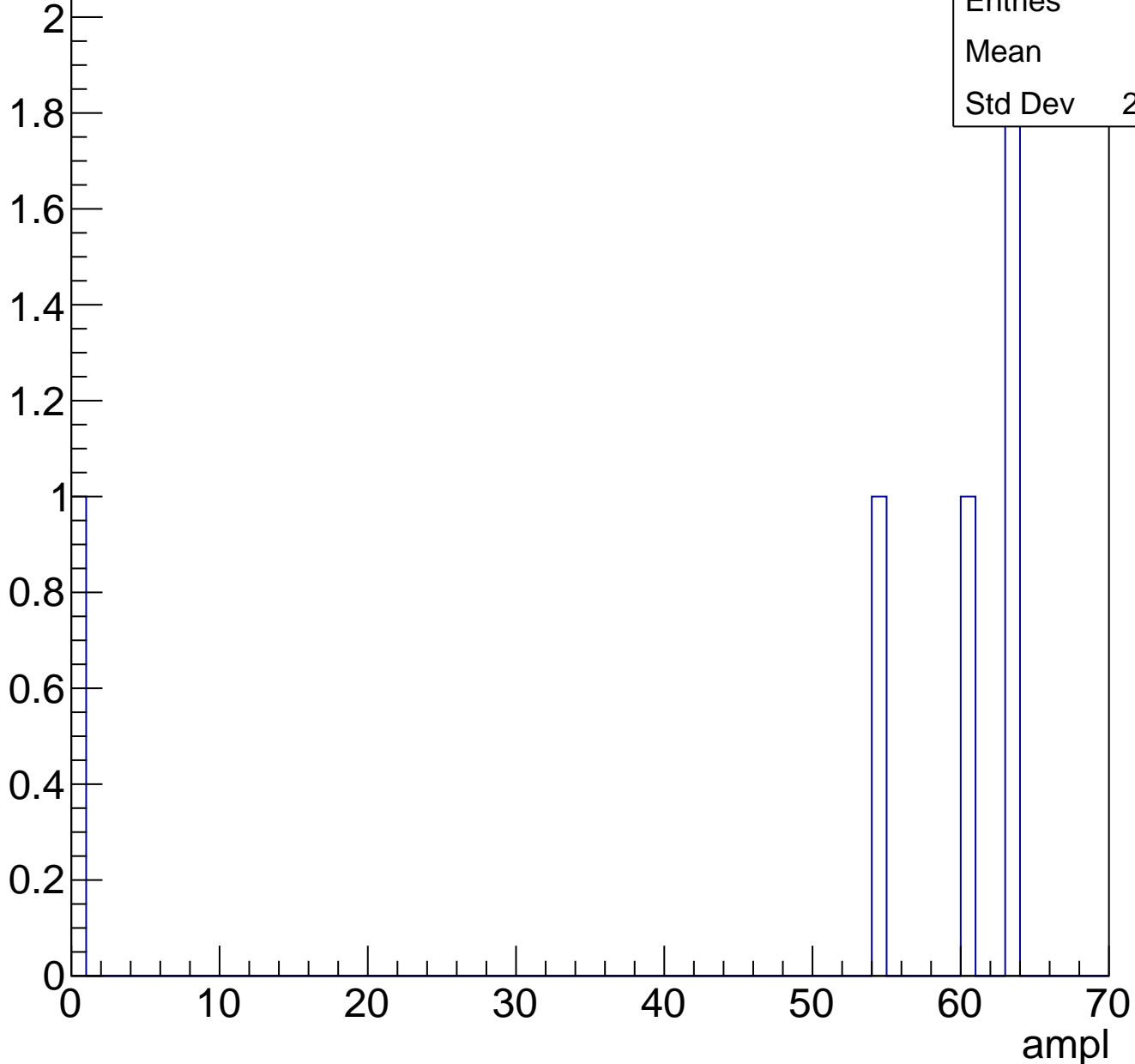
Entries	46
Mean	60.33
Std Dev	2.117



B1L103S, U11-ch37, adc6

calib_packv5_041523_1651.root, FC#0, port C2

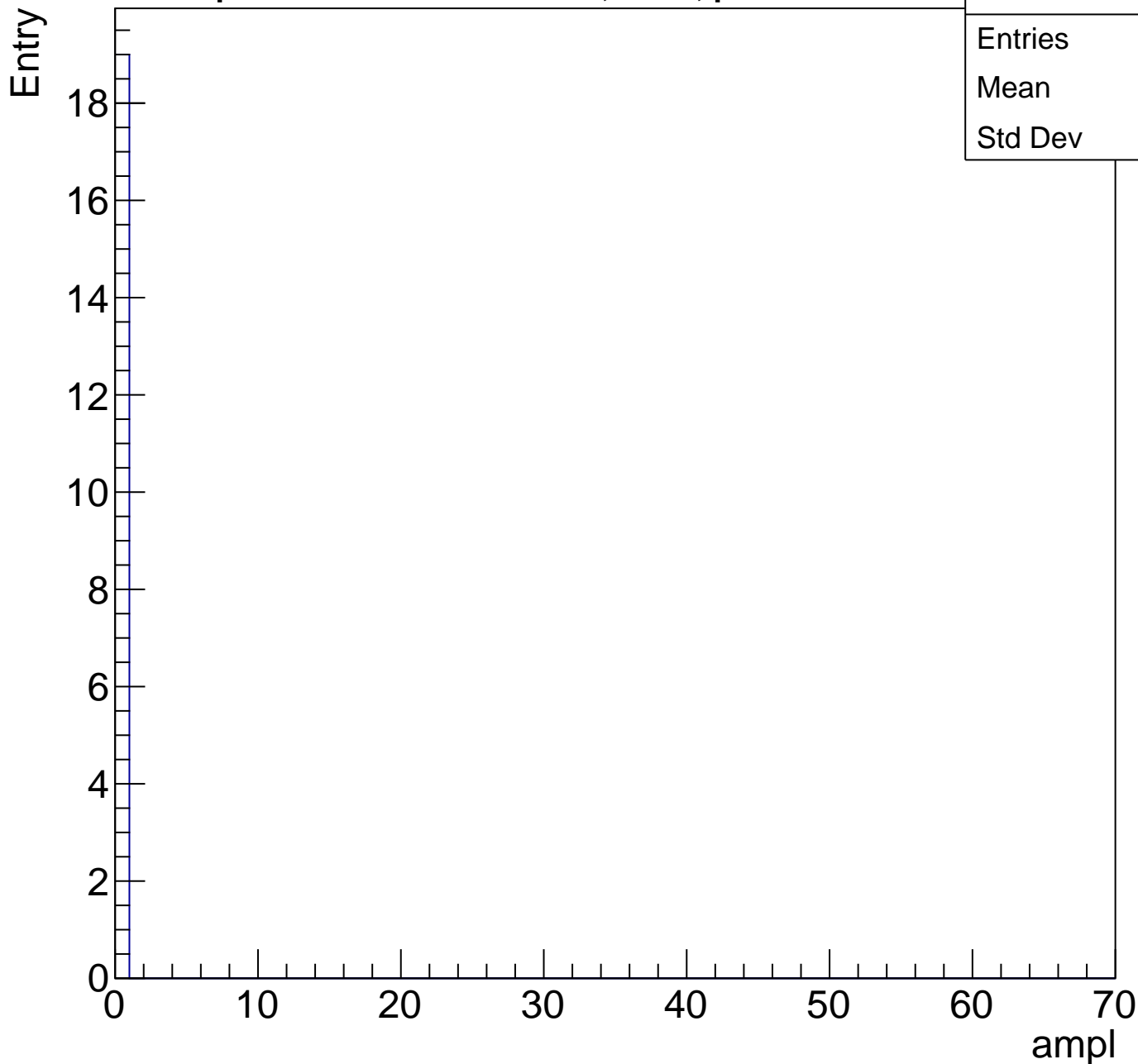
Entry



B1L103S, U11-ch37, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	0
Std Dev	0

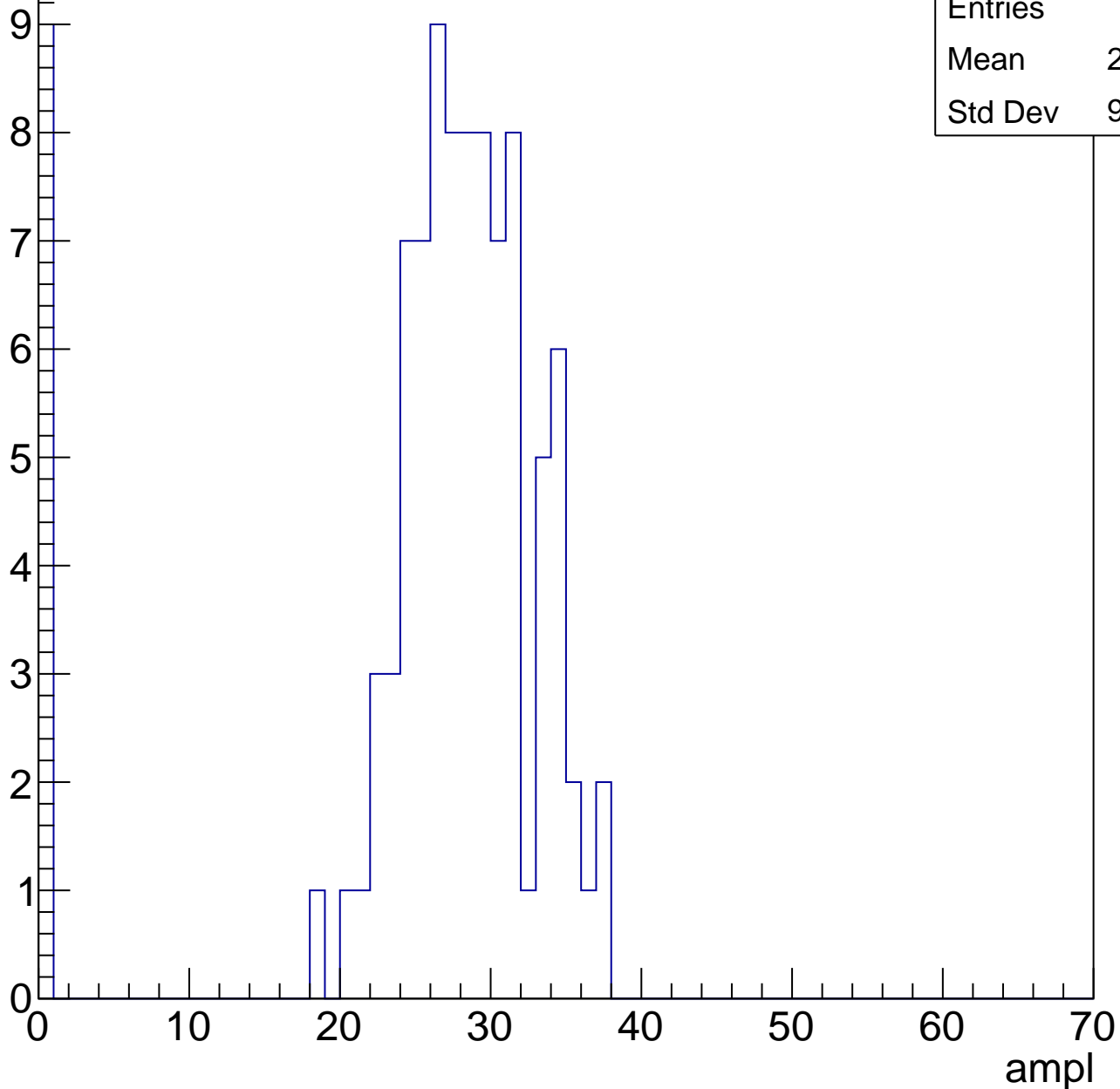


B1L103S, U11-ch38, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	97
Mean	25.59
Std Dev	9.022

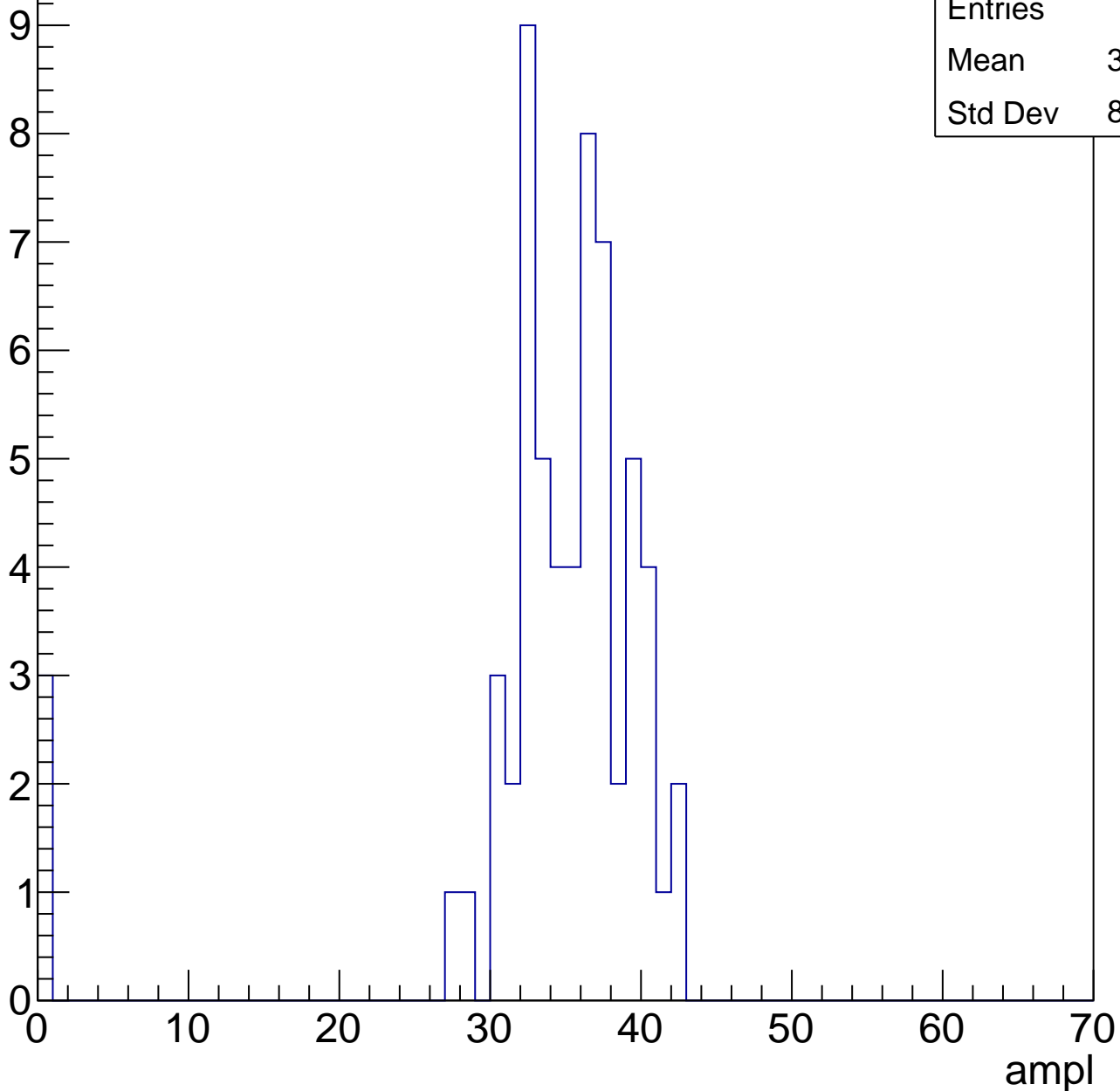


B1L103S, U11-ch38, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

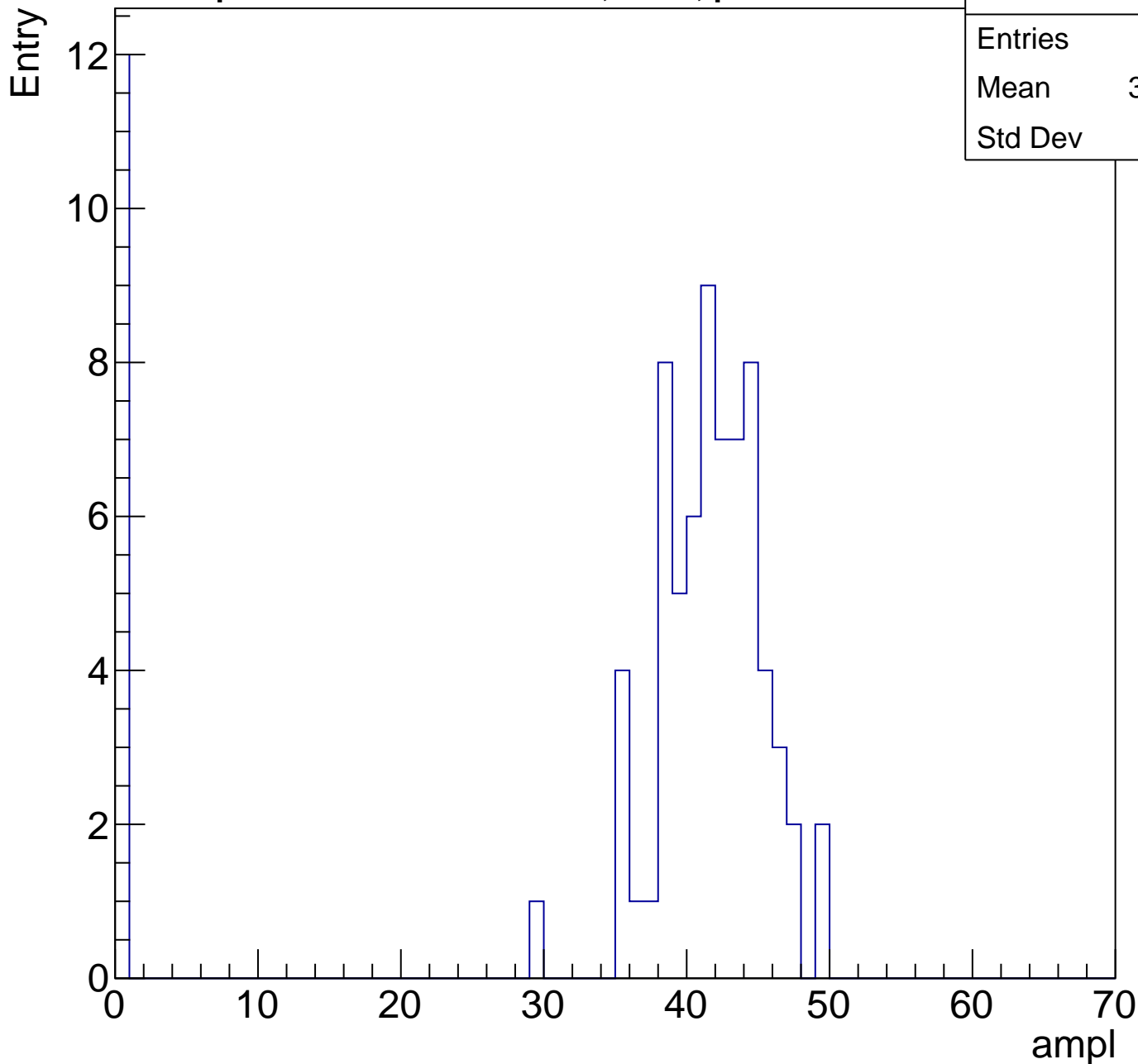
Entries	61
Mean	33.43
Std Dev	8.314



B1L103S, U11-ch38, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	35.09
Std Dev	15.1

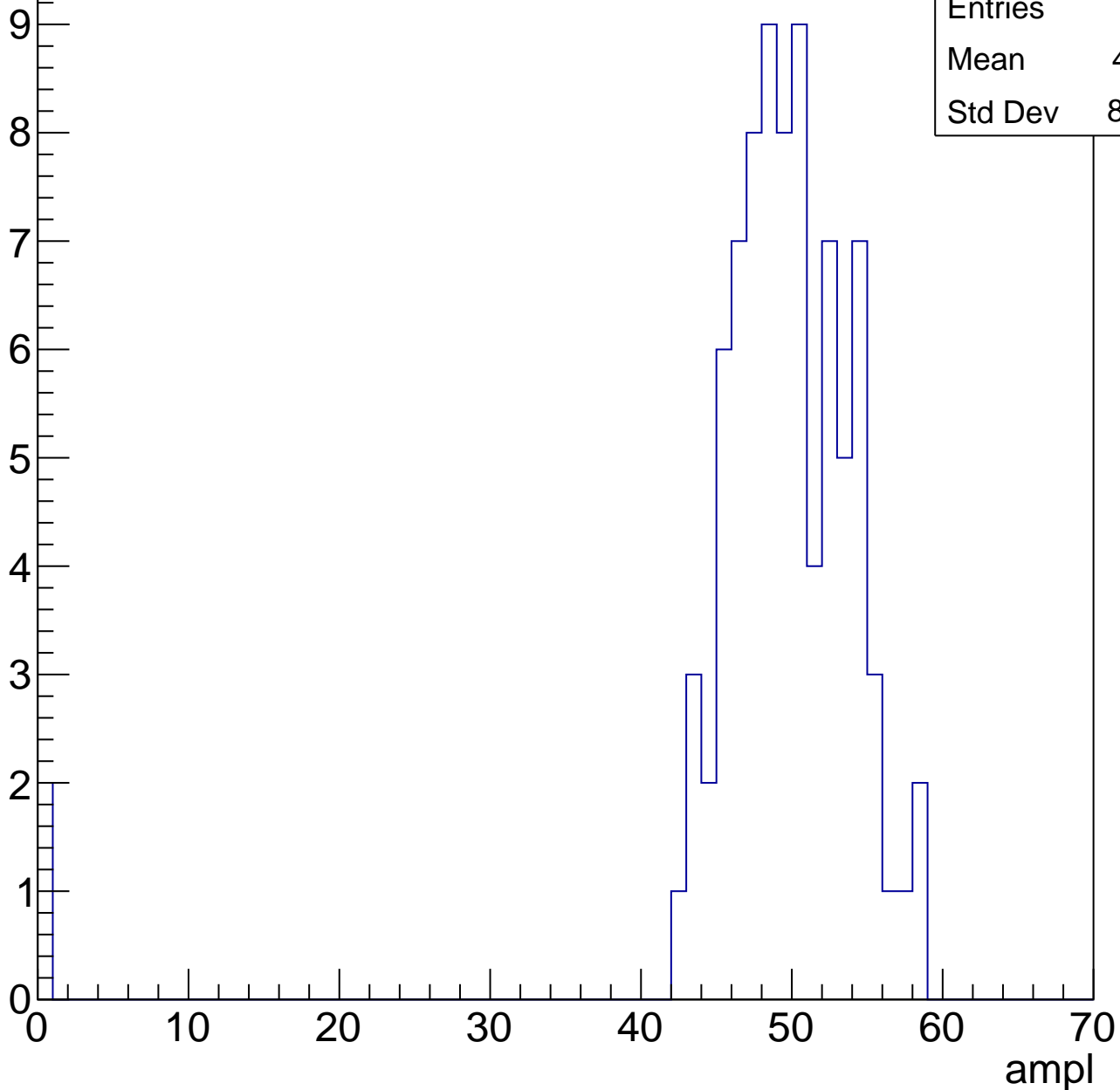


B1L103S, U11-ch38, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	85
Mean	48.31
Std Dev	8.327

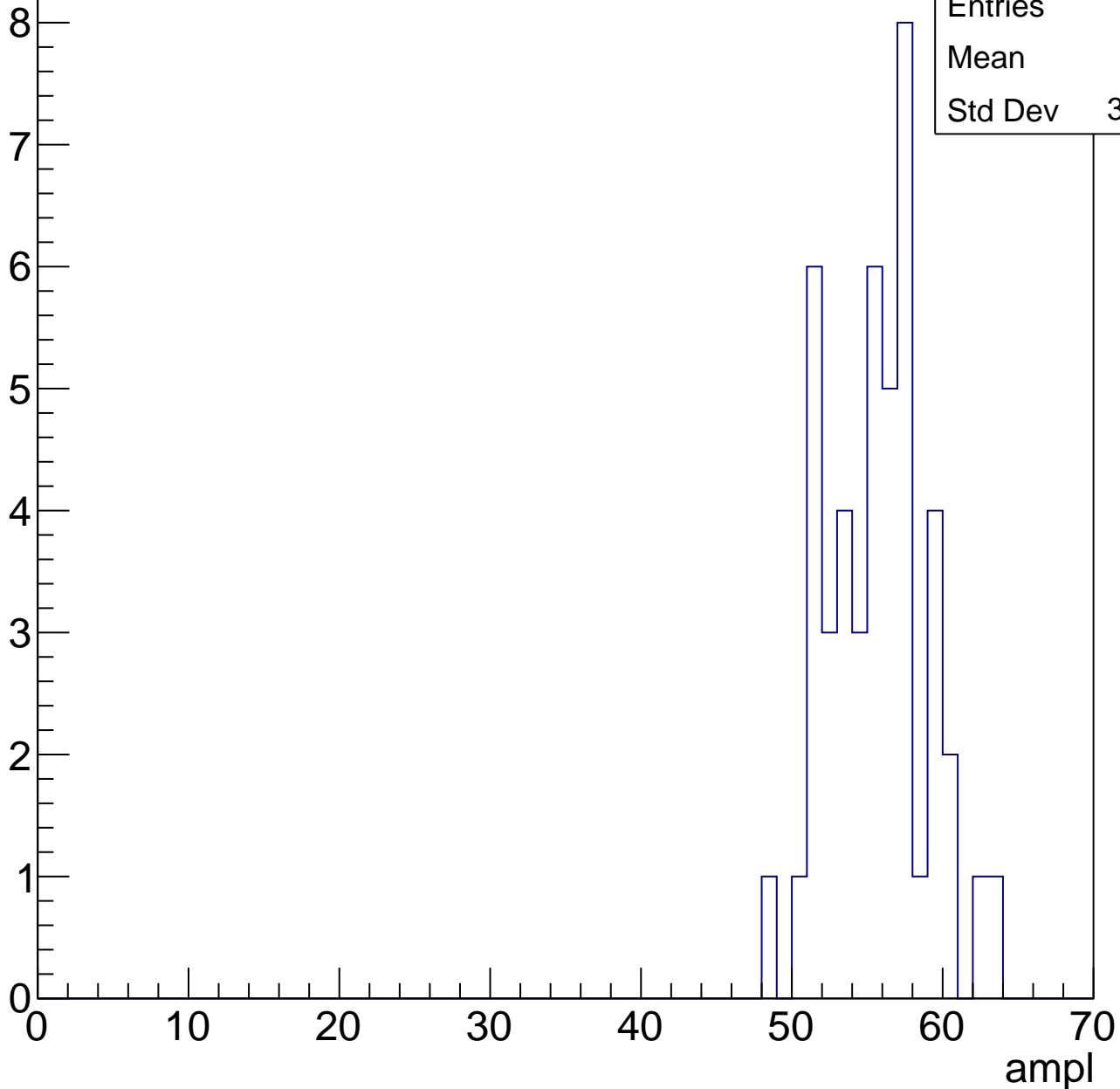


B1L103S, U11-ch38, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	46
Mean	55.2
Std Dev	3.255

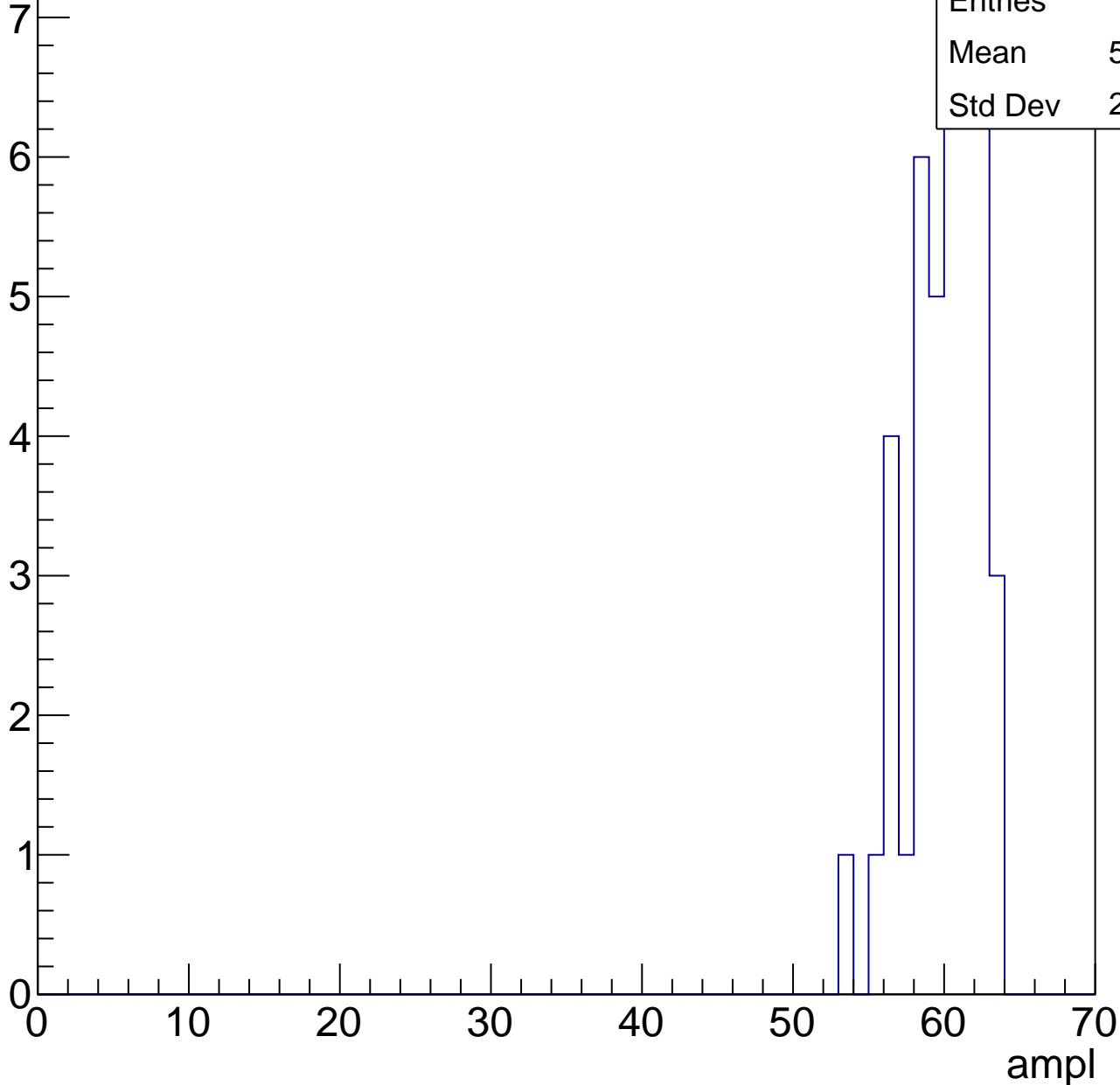


B1L103S, U11-ch38, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	42
Mean	59.57
Std Dev	2.342

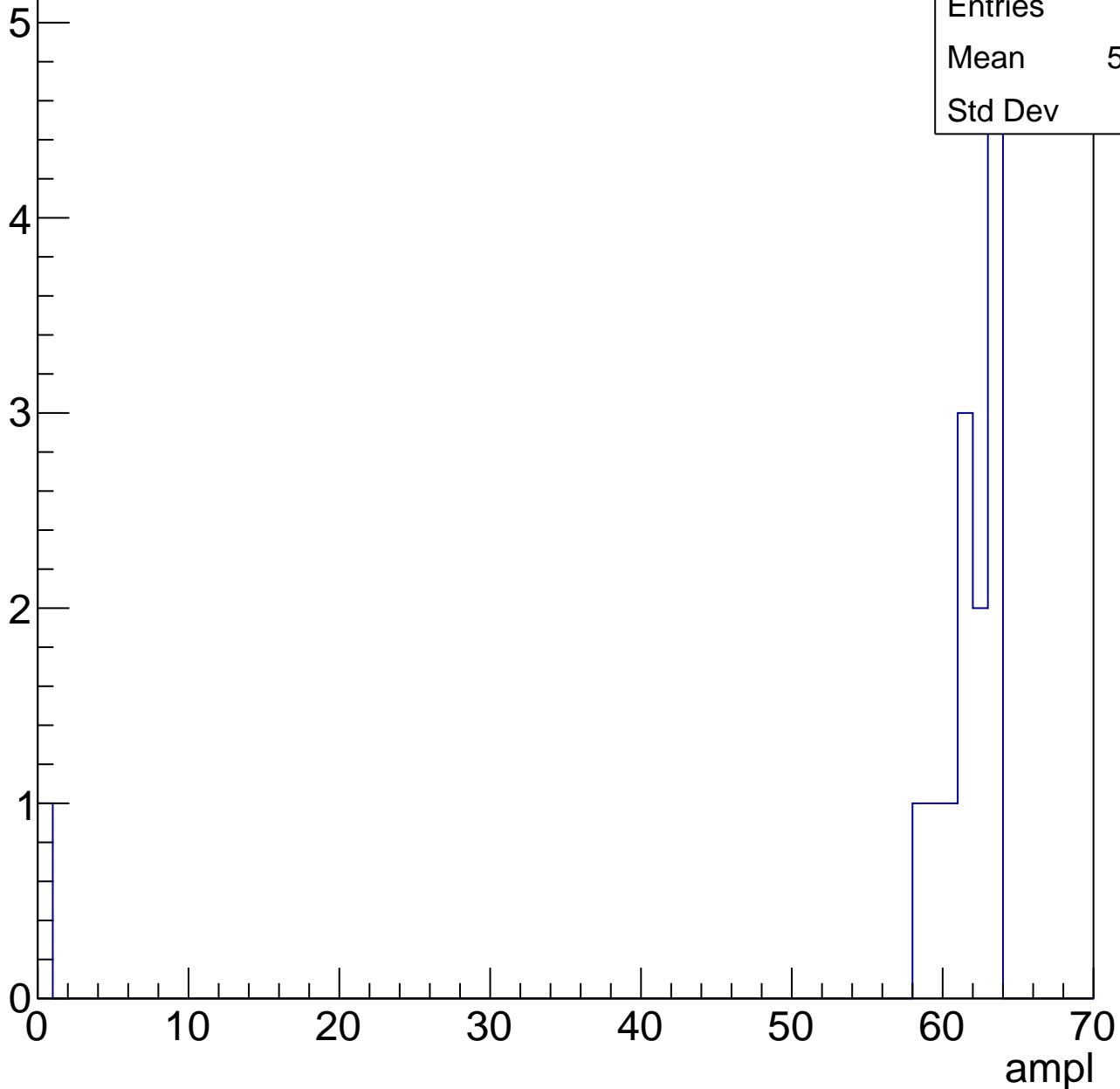


B1L103S, U11-ch38, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	14
Mean	57.07
Std Dev	15.9

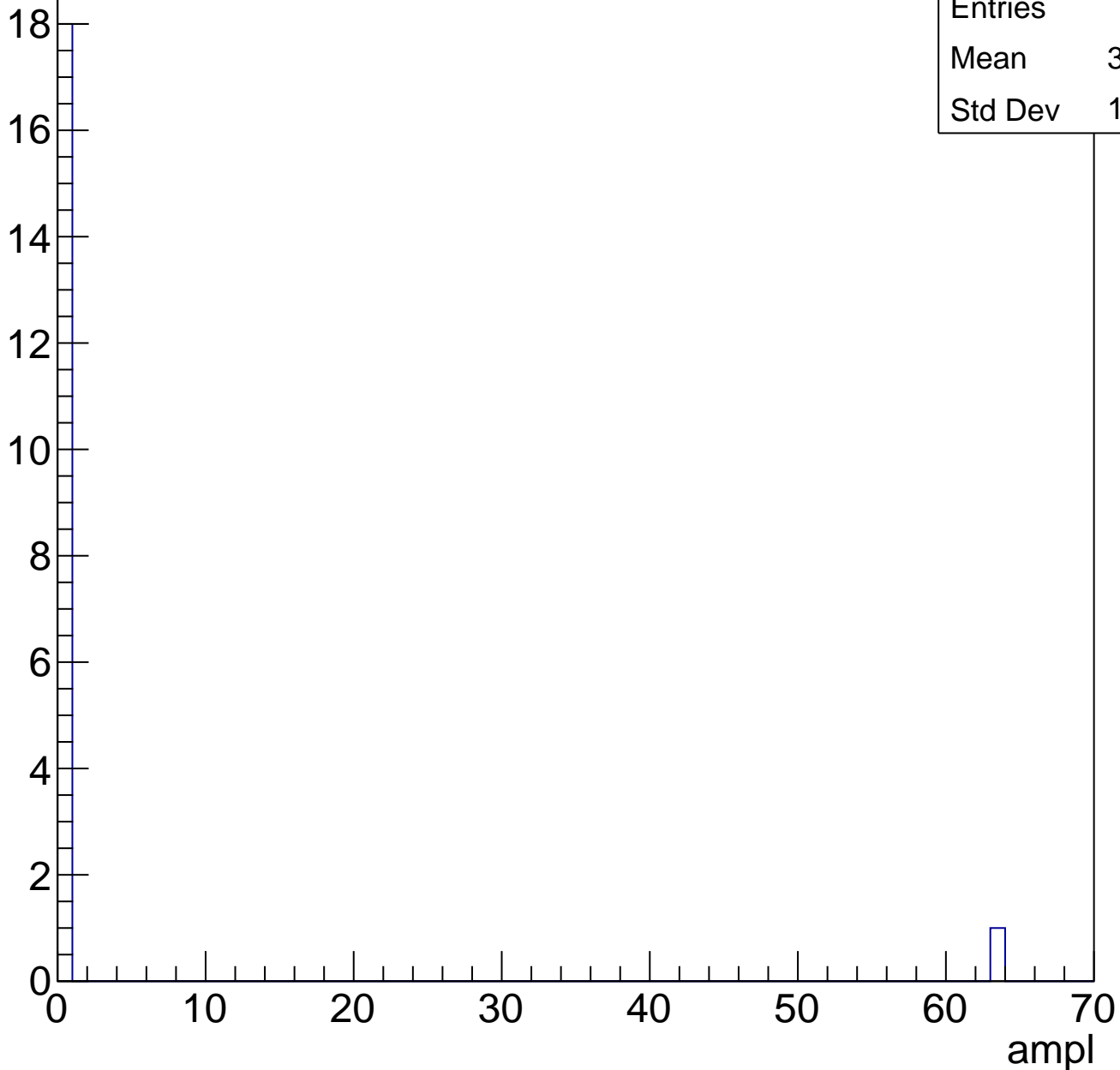


B1L103S, U11-ch38, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	3.316
Std Dev	14.07

Entry



B1L103S, U11-ch39, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	92
Mean	26.55
Std Dev	10.36

Entry

10

8

6

4

2

0

0

10

20

30

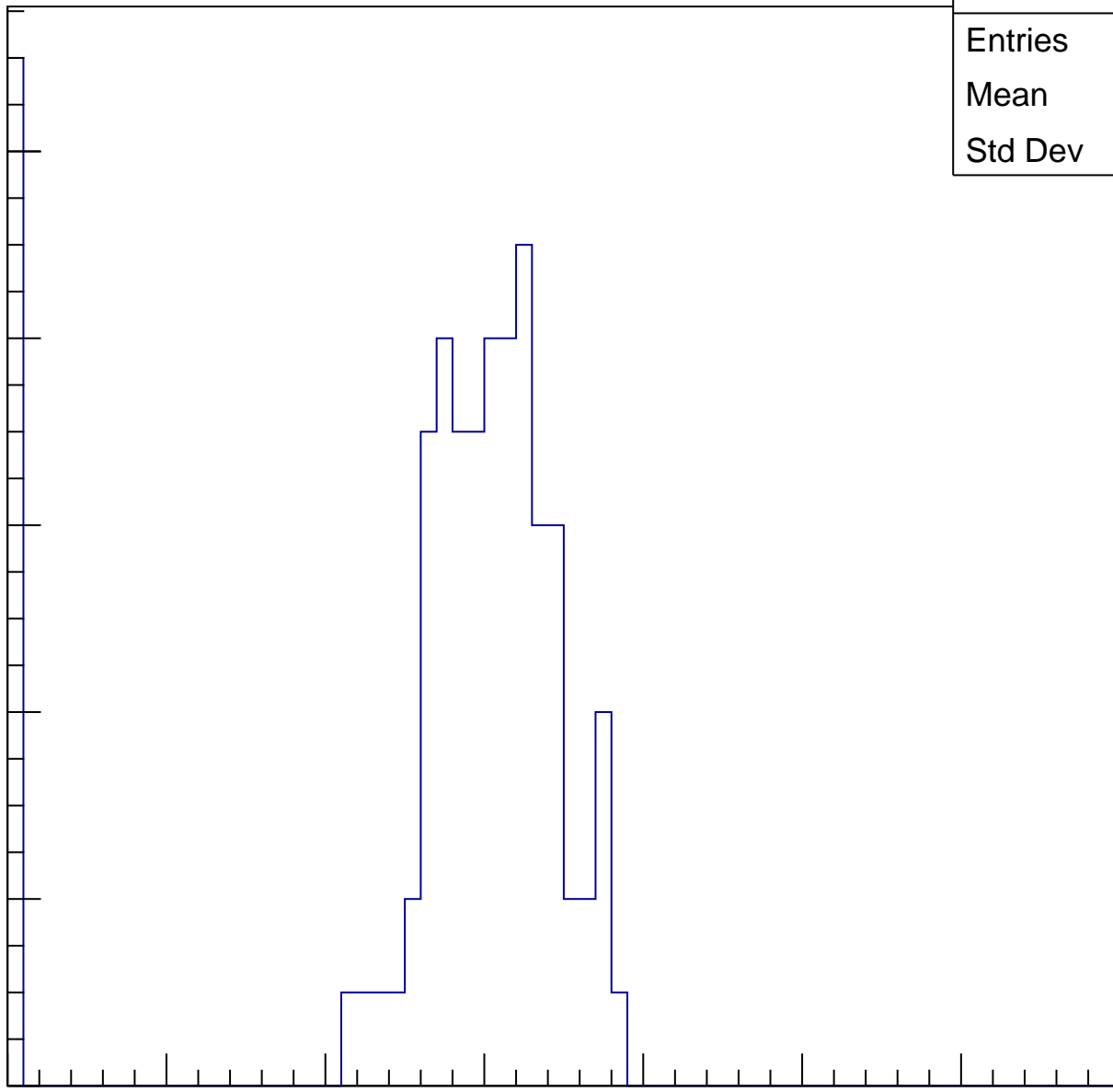
40

50

60

70

ampl

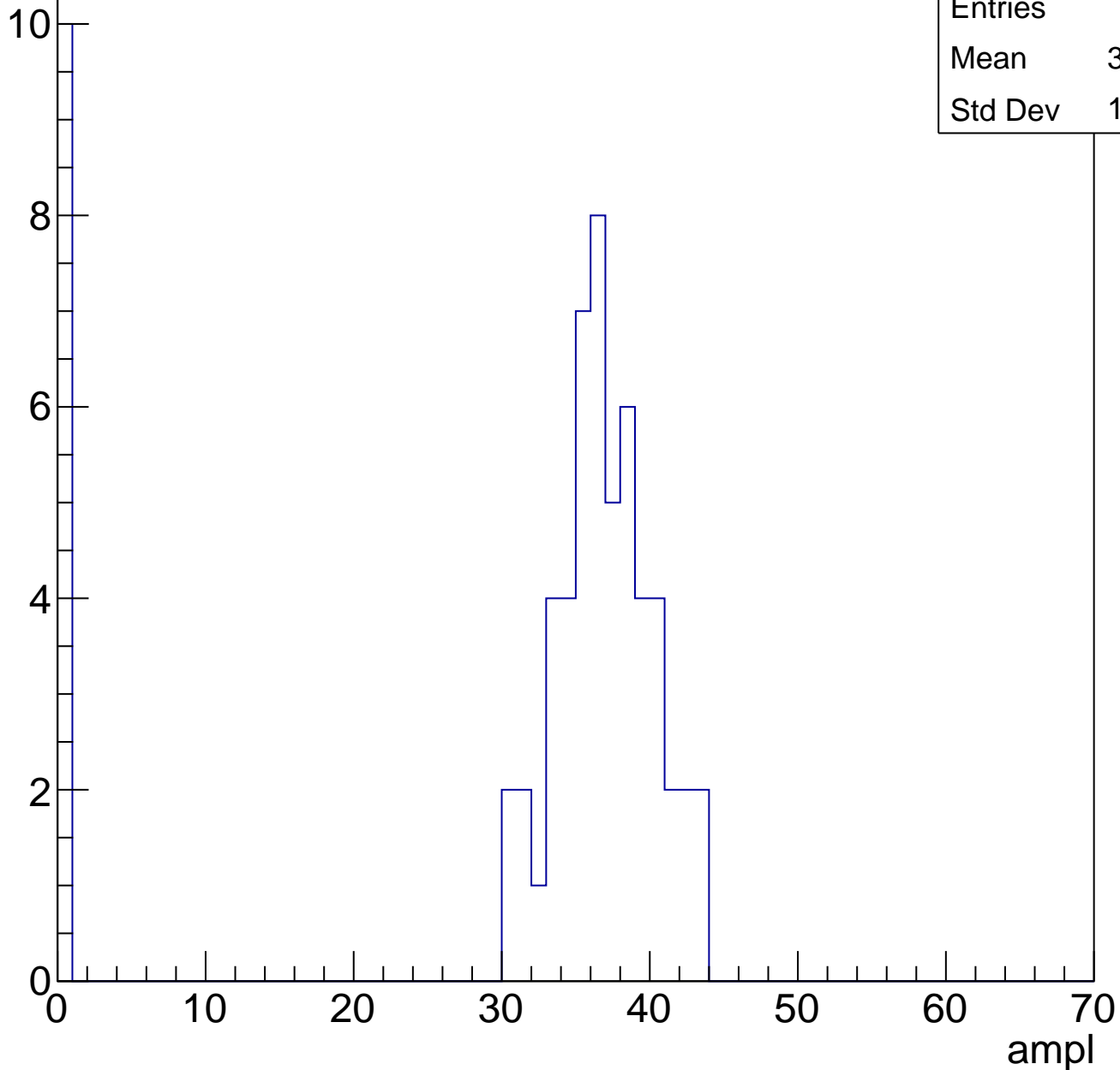


B1L103S, U11-ch39, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	63
Mean	30.73
Std Dev	13.66

Entry

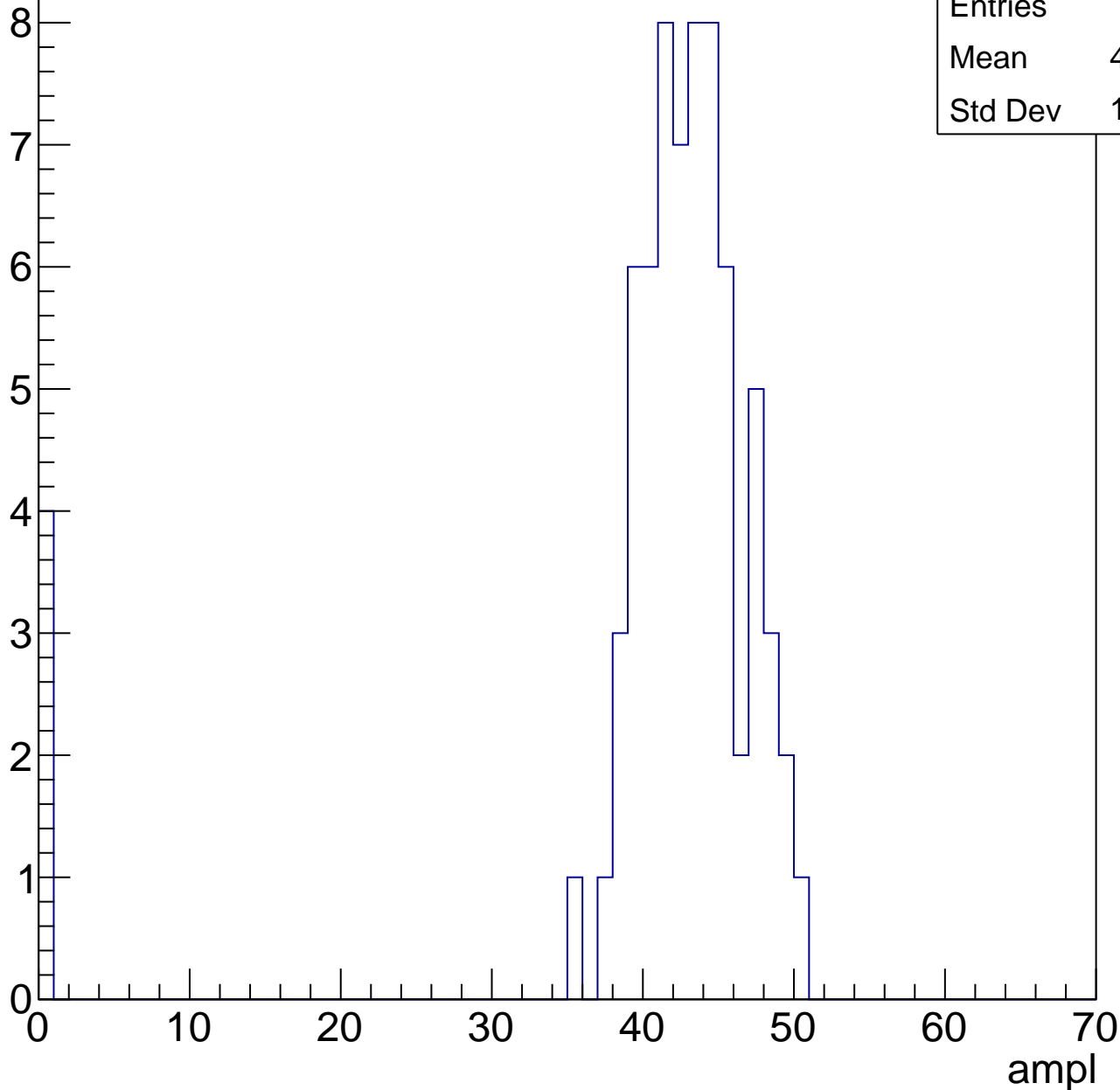


B1L103S, U11-ch39, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	40.38
Std Dev	10.35

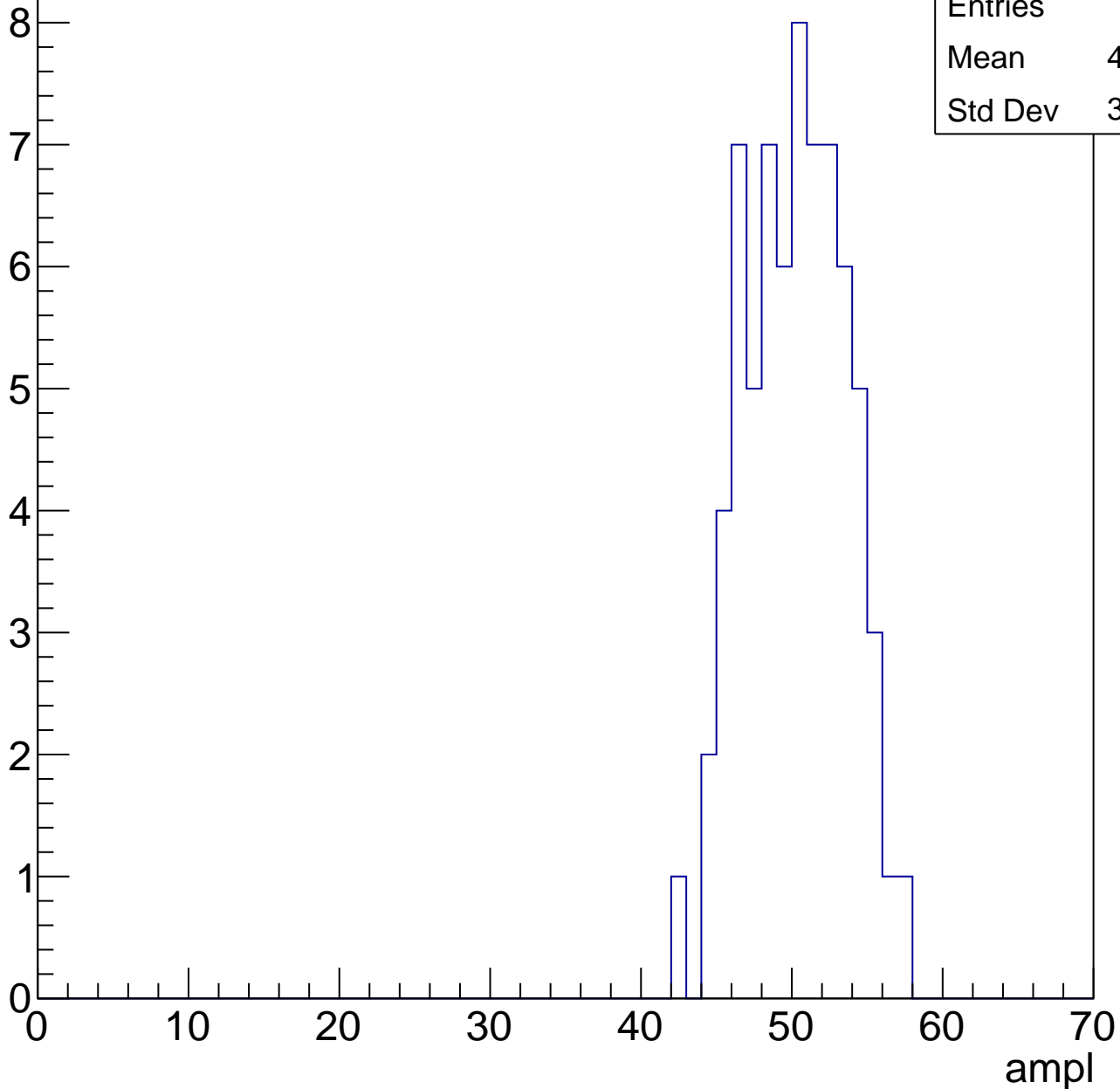


B1L103S, U11-ch39, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	49.77
Std Dev	3.278

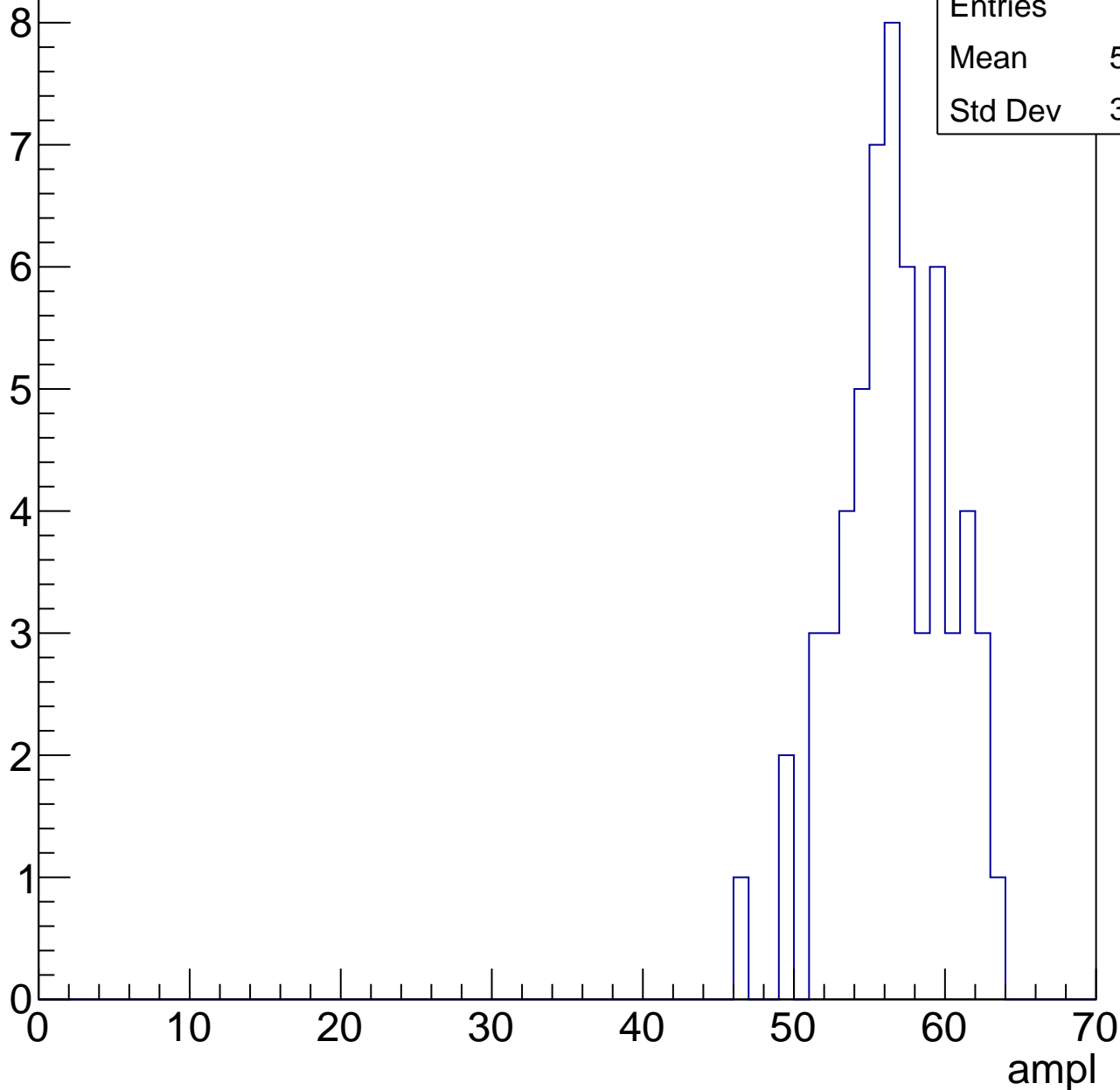


B1L103S, U11-ch39, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	56.12
Std Dev	3.589

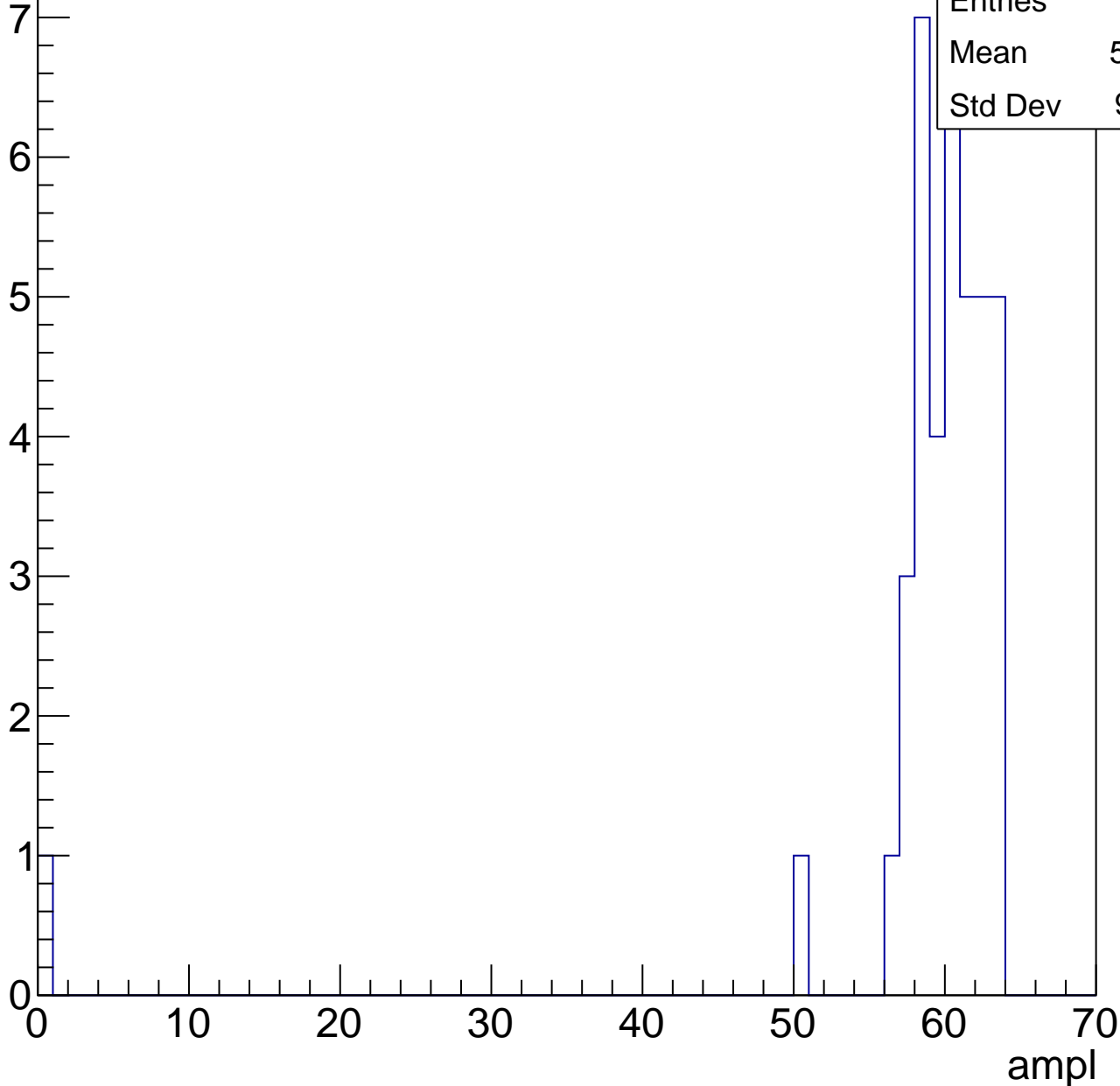


B1L103S, U11-ch39, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	58.18
Std Dev	9.761



B1L103S, U11-ch39, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch39, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	3.316
Std Dev	14.07

Entry

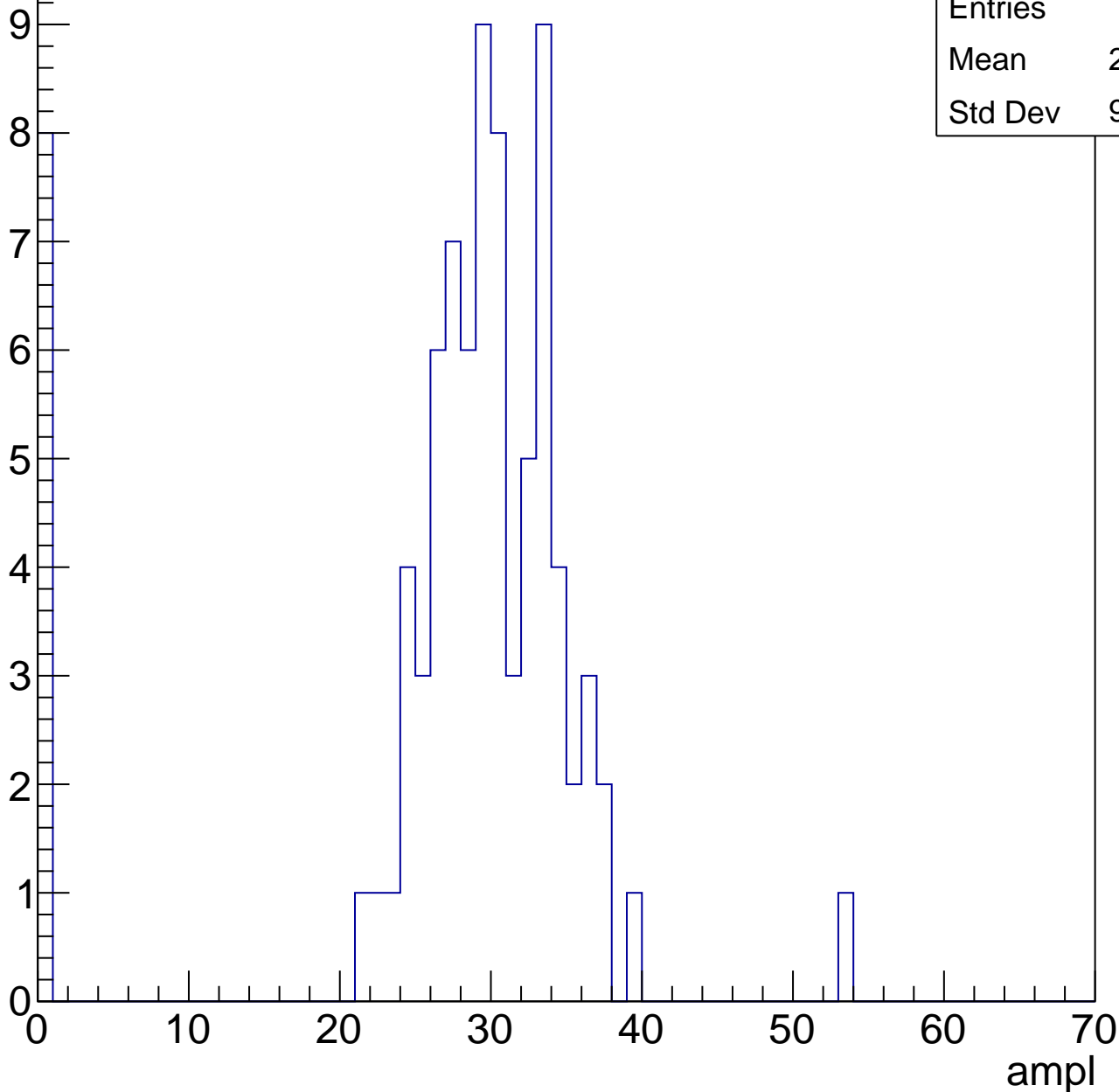


B1L103S, U11-ch40, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	84
Mean	27.15
Std Dev	9.855

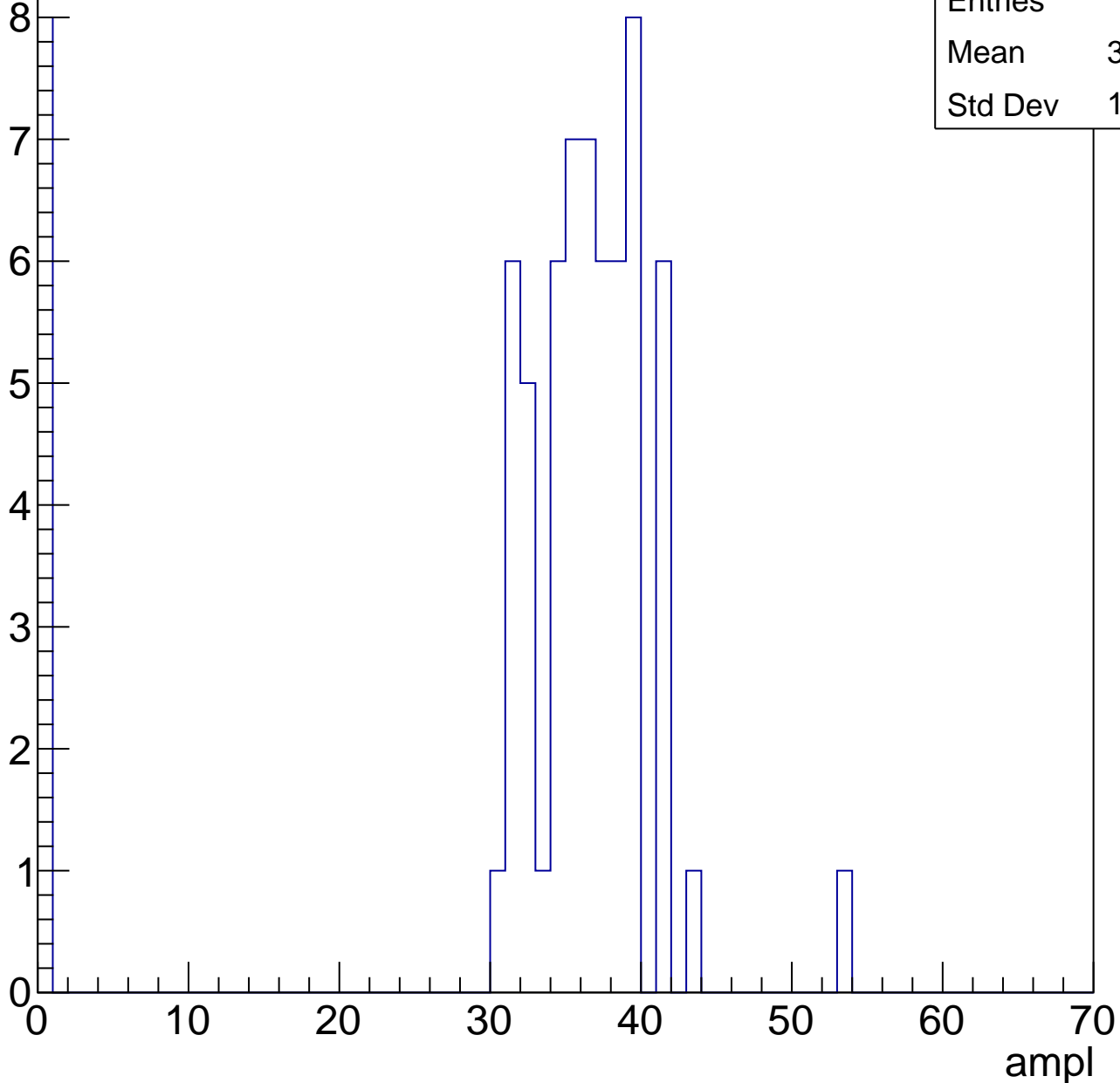


B1L103S, U11-ch40, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	32.09
Std Dev	12.16



B1L103S, U11-ch40, adc2

calib_packv5_041523_1651.root, FC#0, port C2

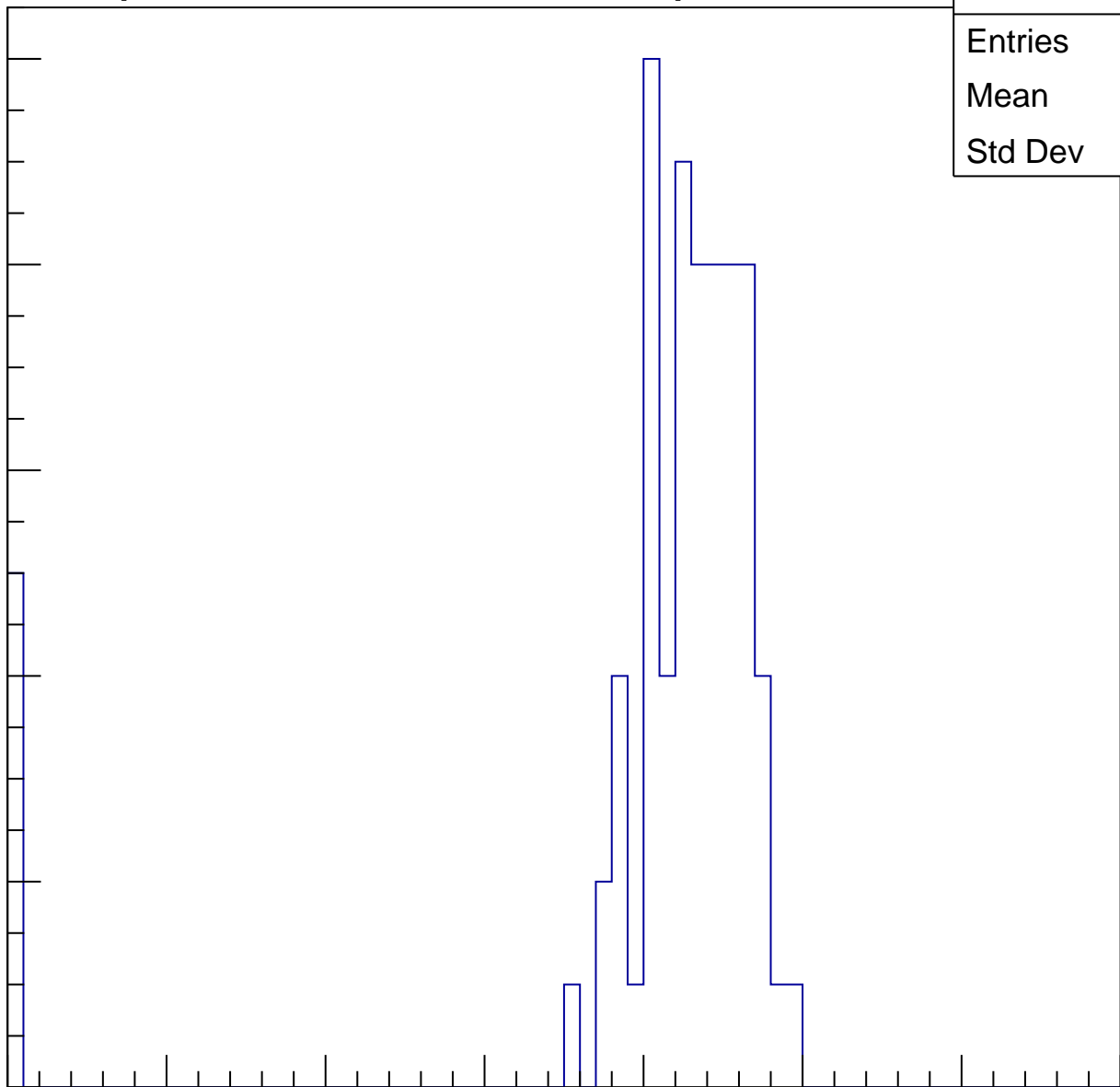
Entries	74
Mean	39.88
Std Dev	11.11

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

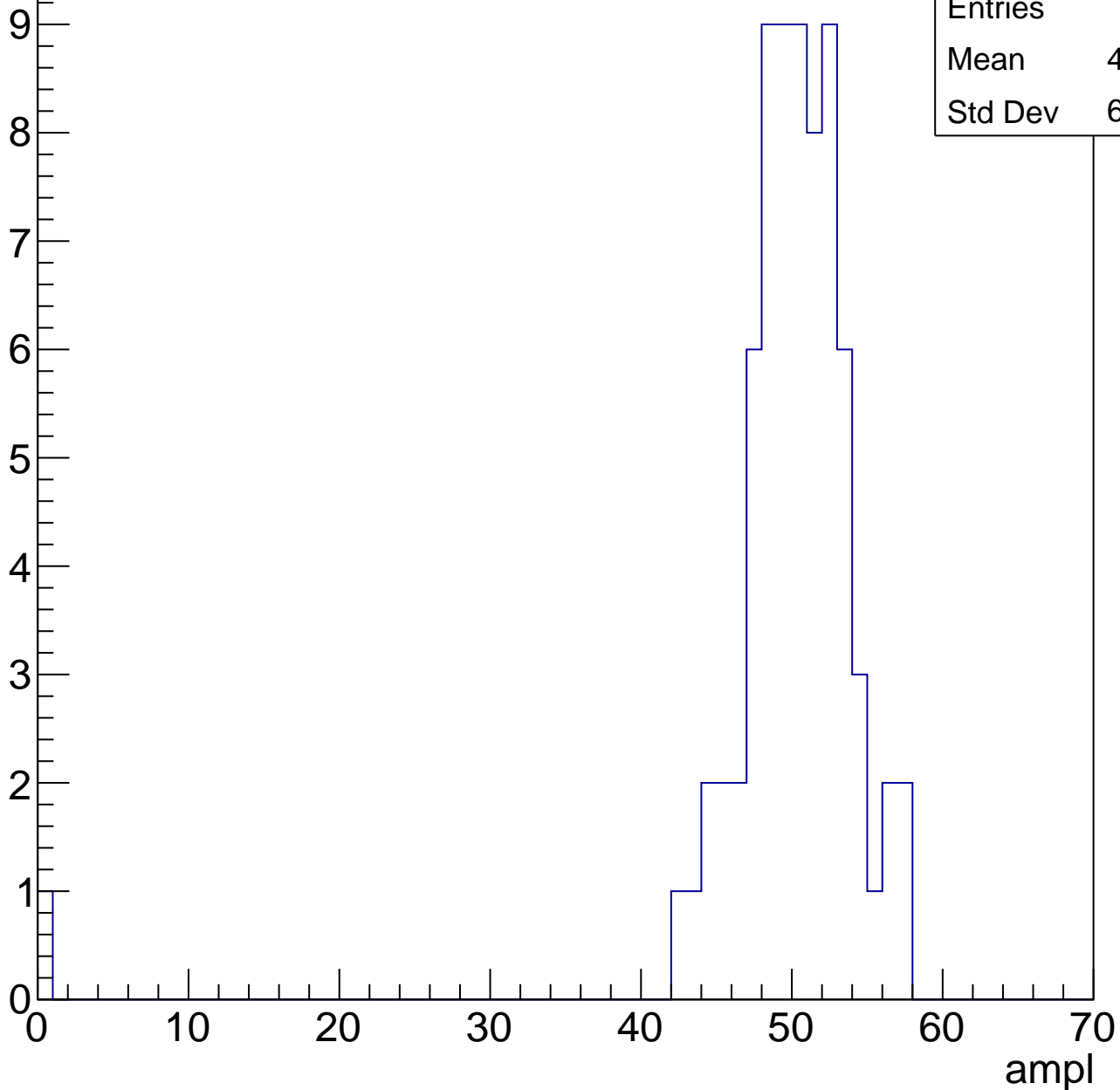


B1L103S, U11-ch40, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	49.27
Std Dev	6.588

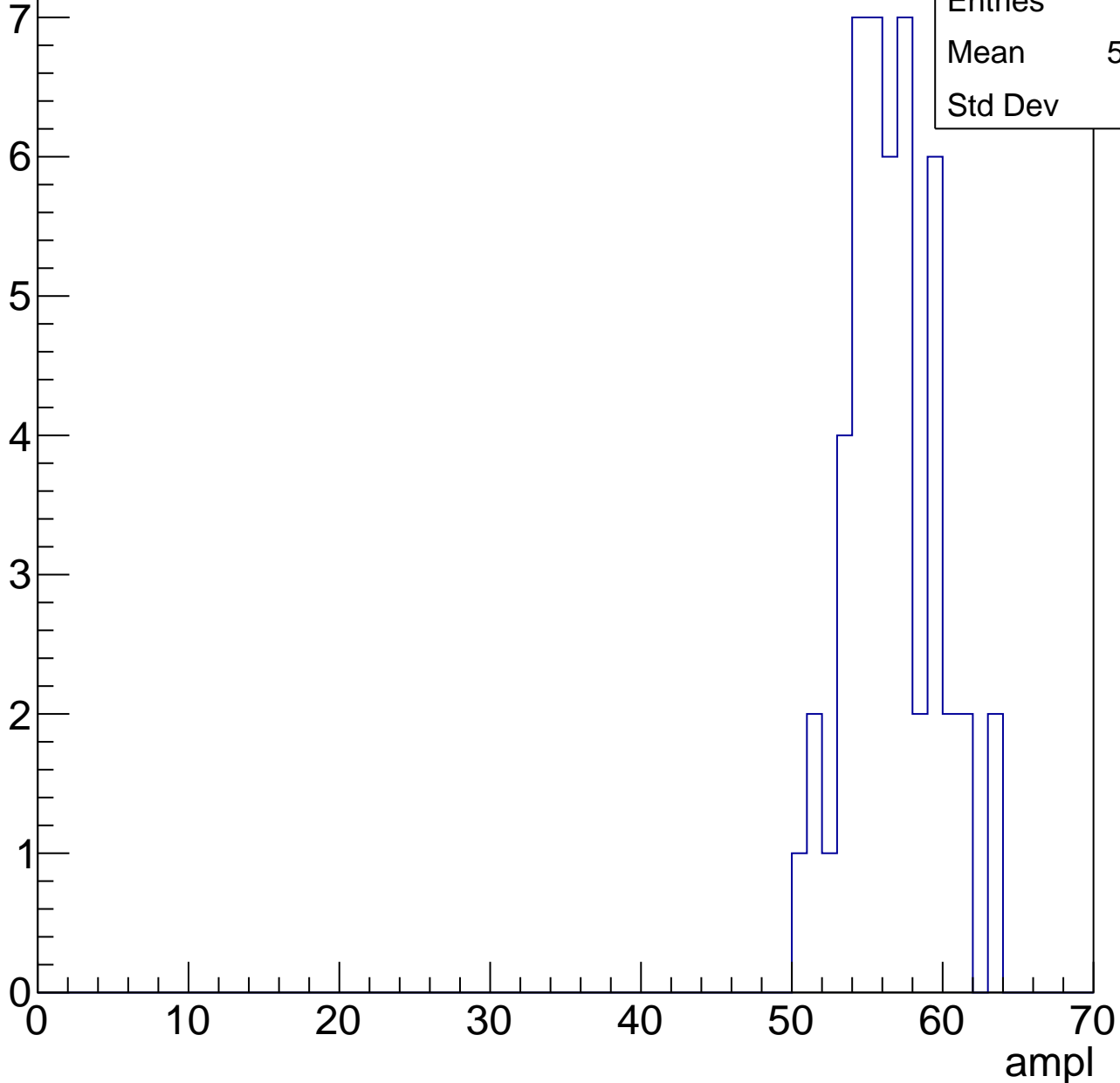


B1L103S, U11-ch40, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

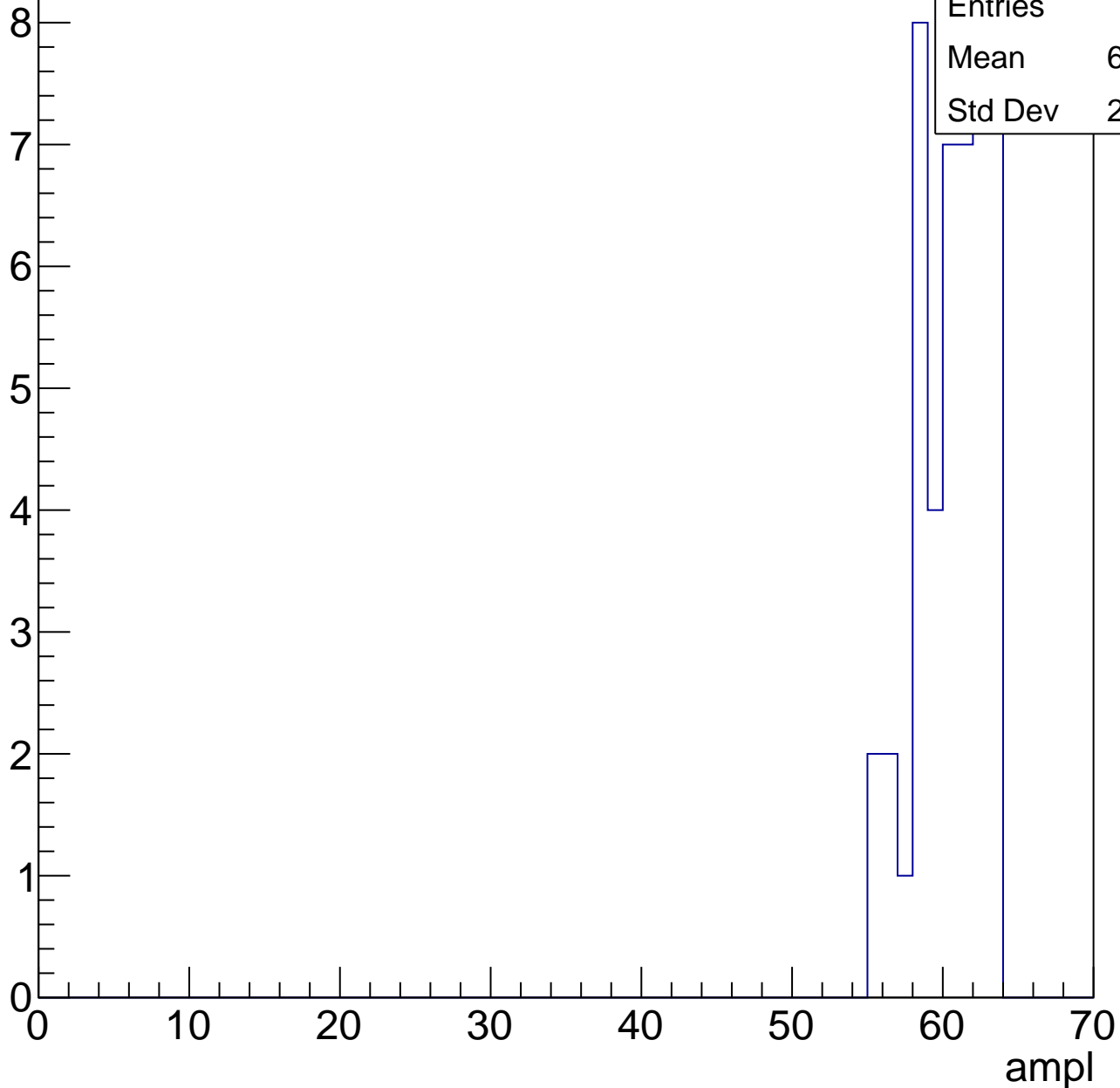
Entries	49
Mean	56.16
Std Dev	2.93



B1L103S, U11-ch40, adc5

calib_packv5_041523_1651.root, FC#0, port C2

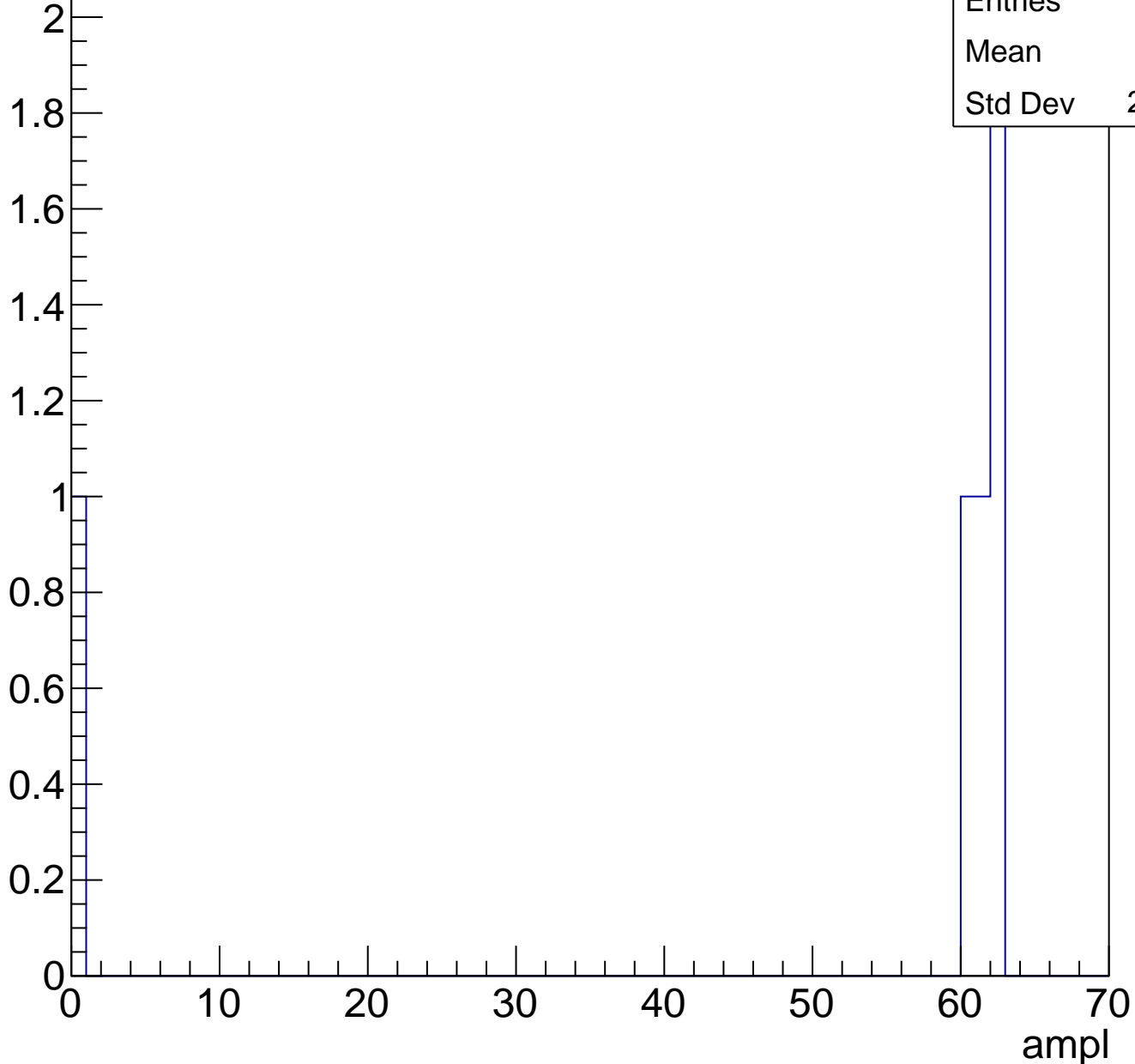
Entry



B1L103S, U11-ch40, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



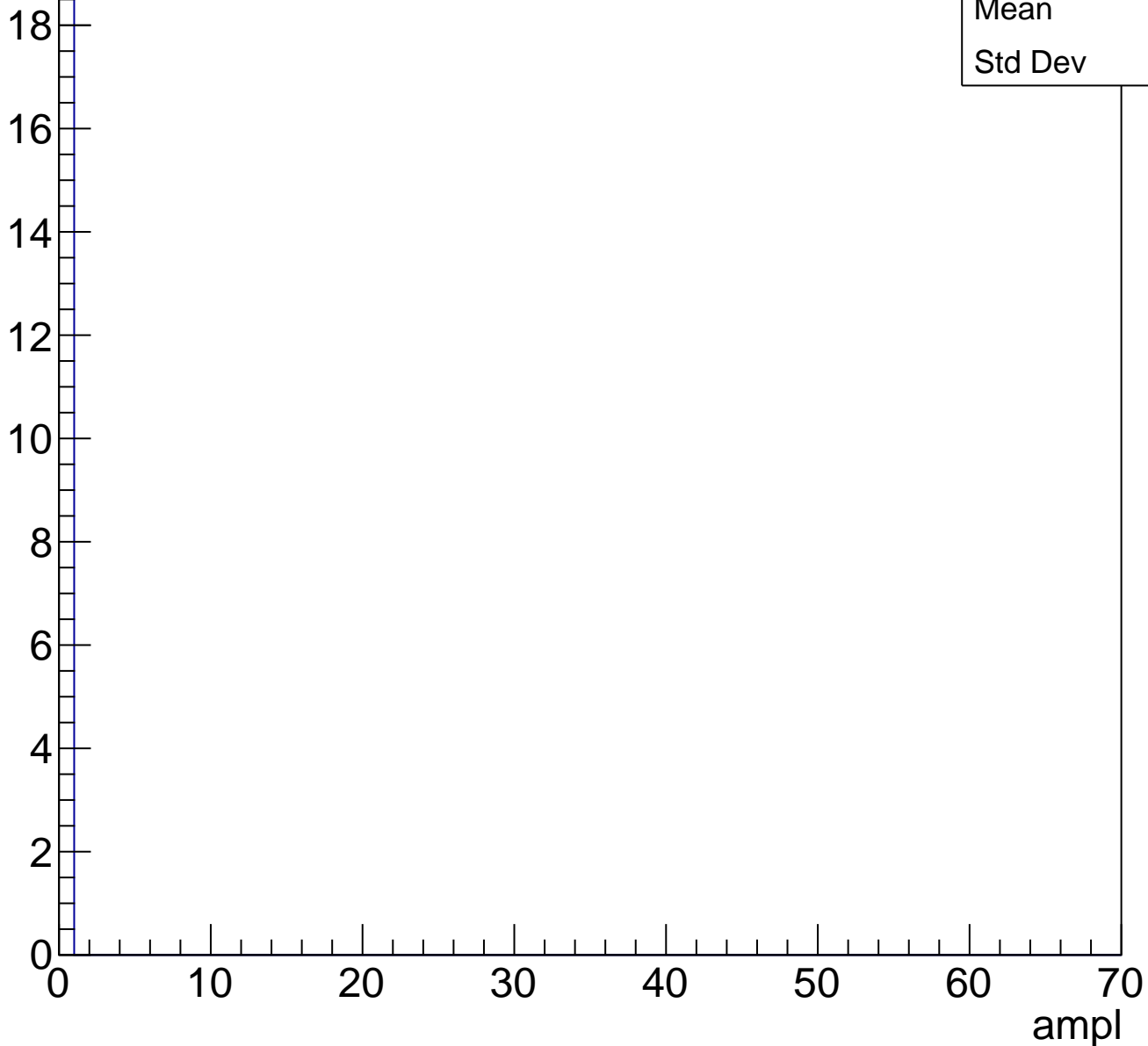
Entries	5
Mean	49
Std Dev	24.51

B1L103S, U11-ch40, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	0
Std Dev	0

Entry



B1L103S, U11-ch41, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	98
Mean	20.91
Std Dev	13.51

Entry

25

20

15

10

5

0

0

10

20

30

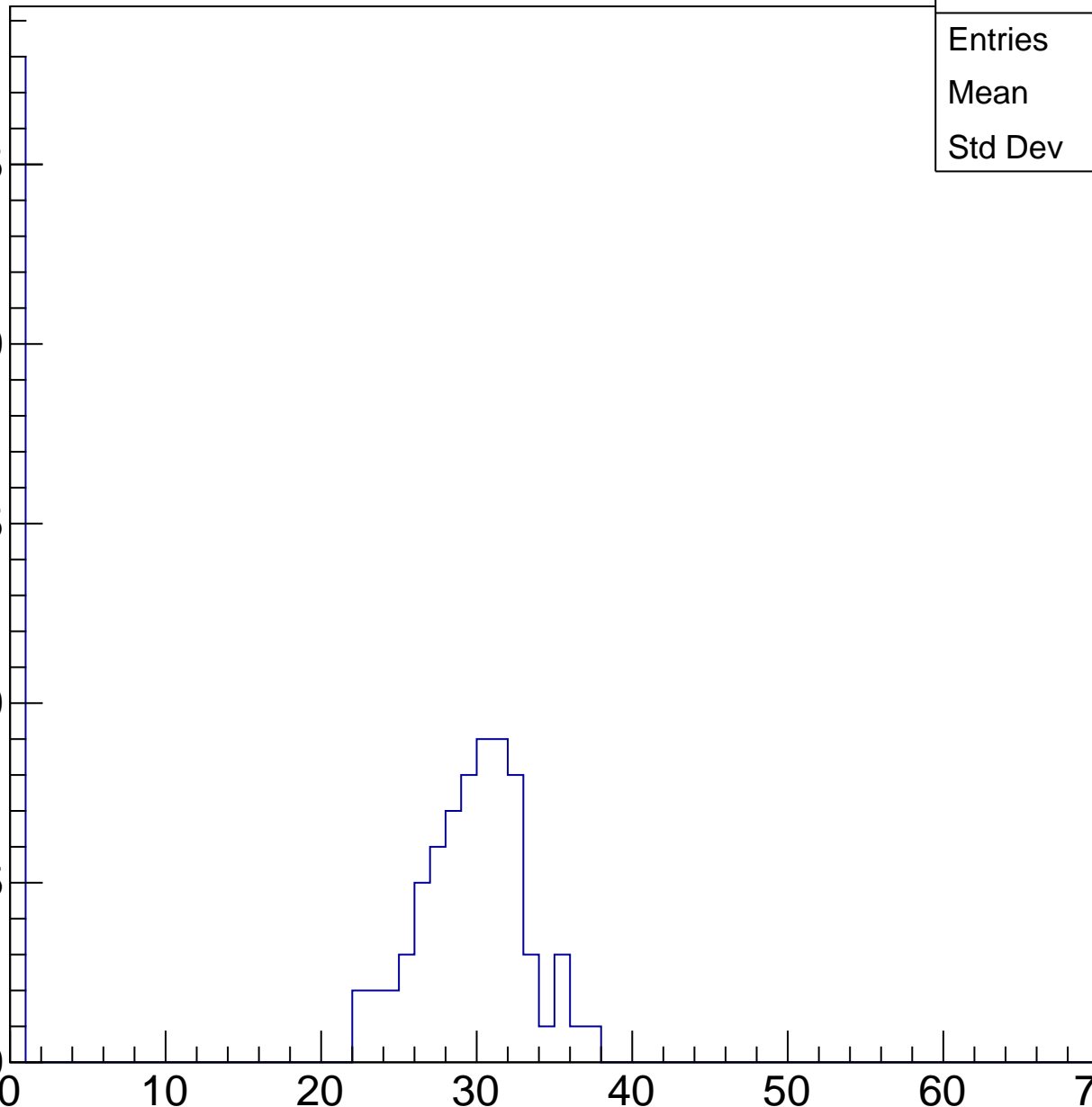
40

50

60

70

ampl

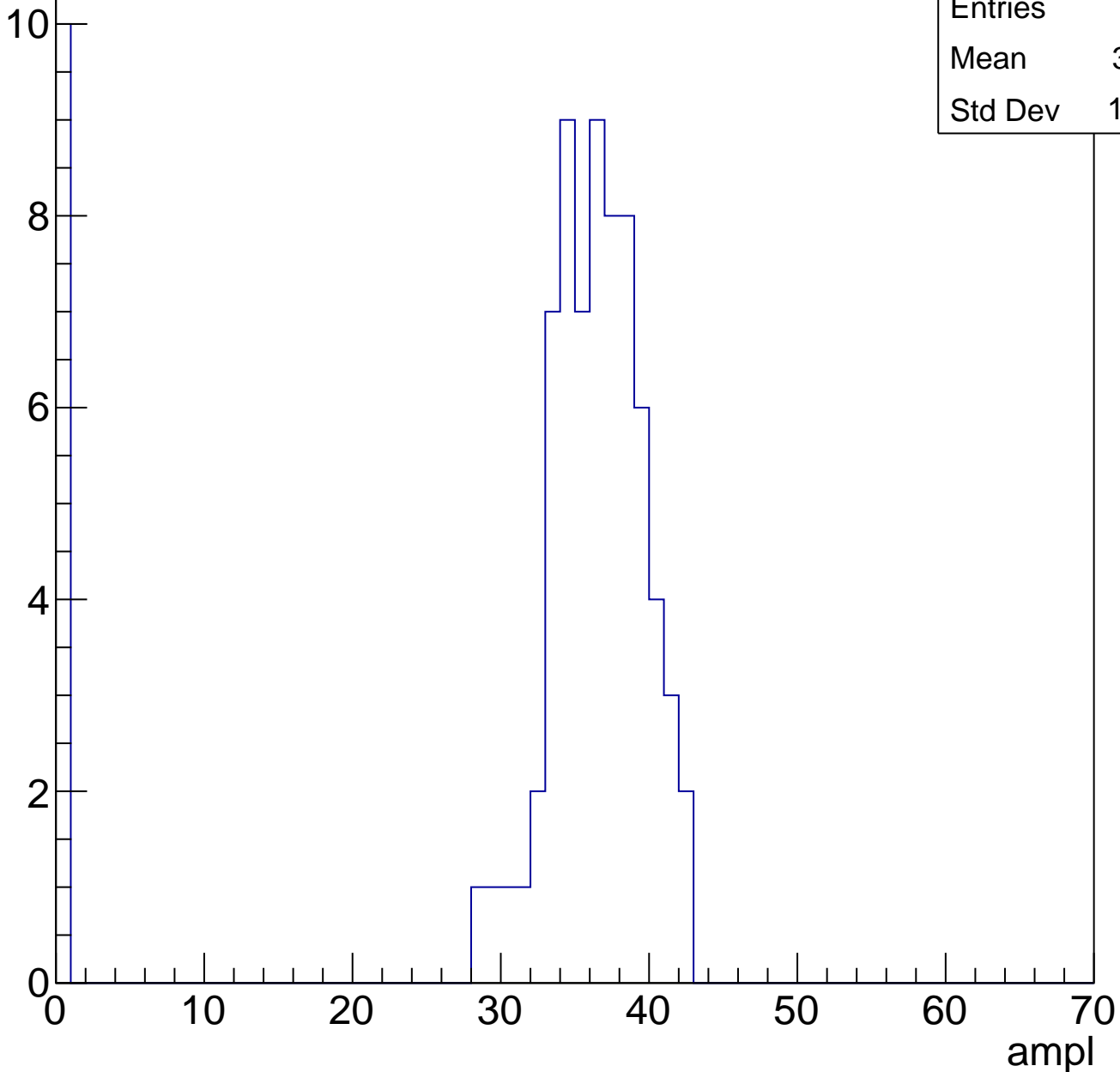


B1L103S, U11-ch41, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	79
Mean	31.51
Std Dev	12.32

Entry

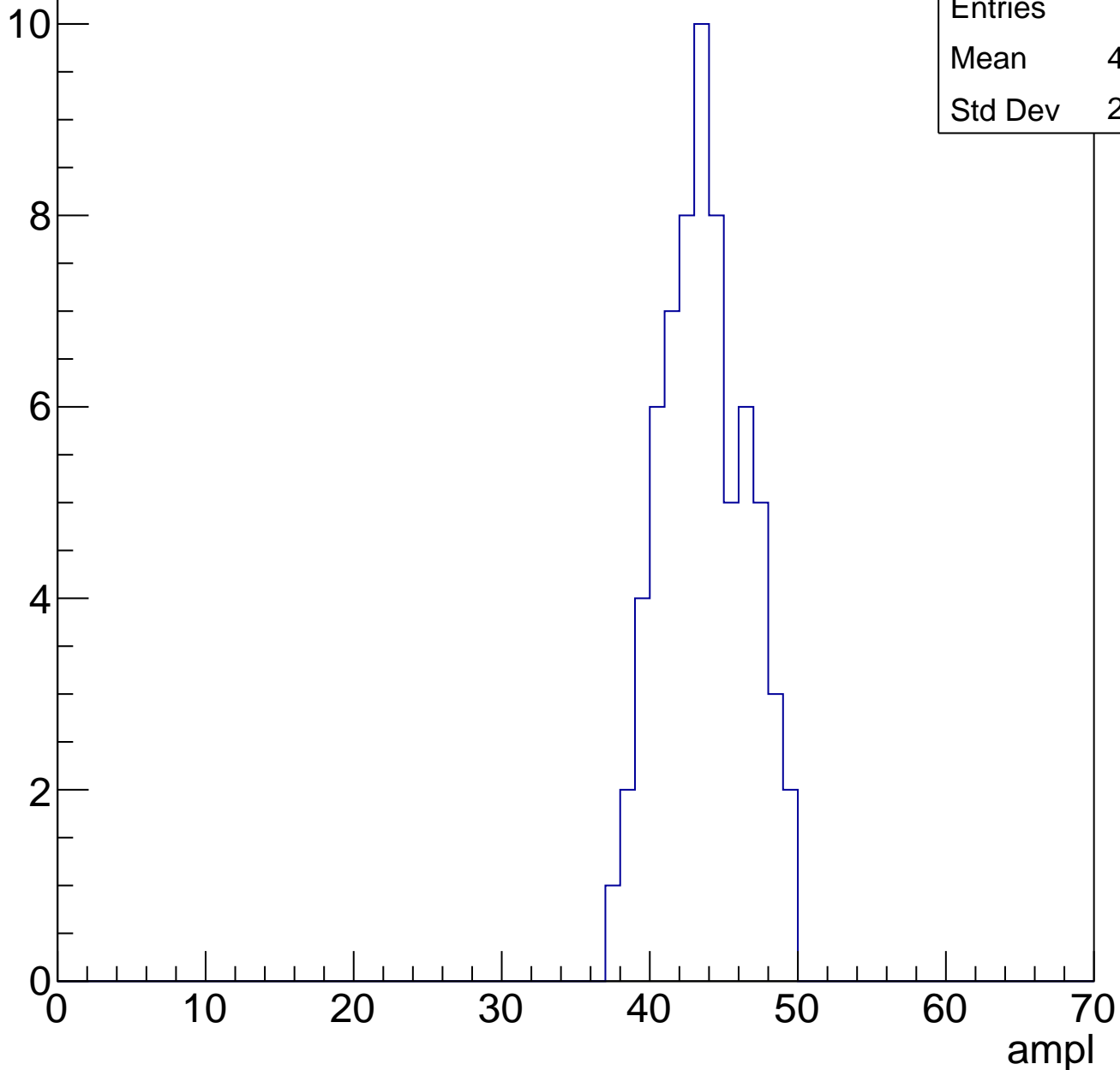


B1L103S, U11-ch41, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	67
Mean	43.16
Std Dev	2.858

Entry

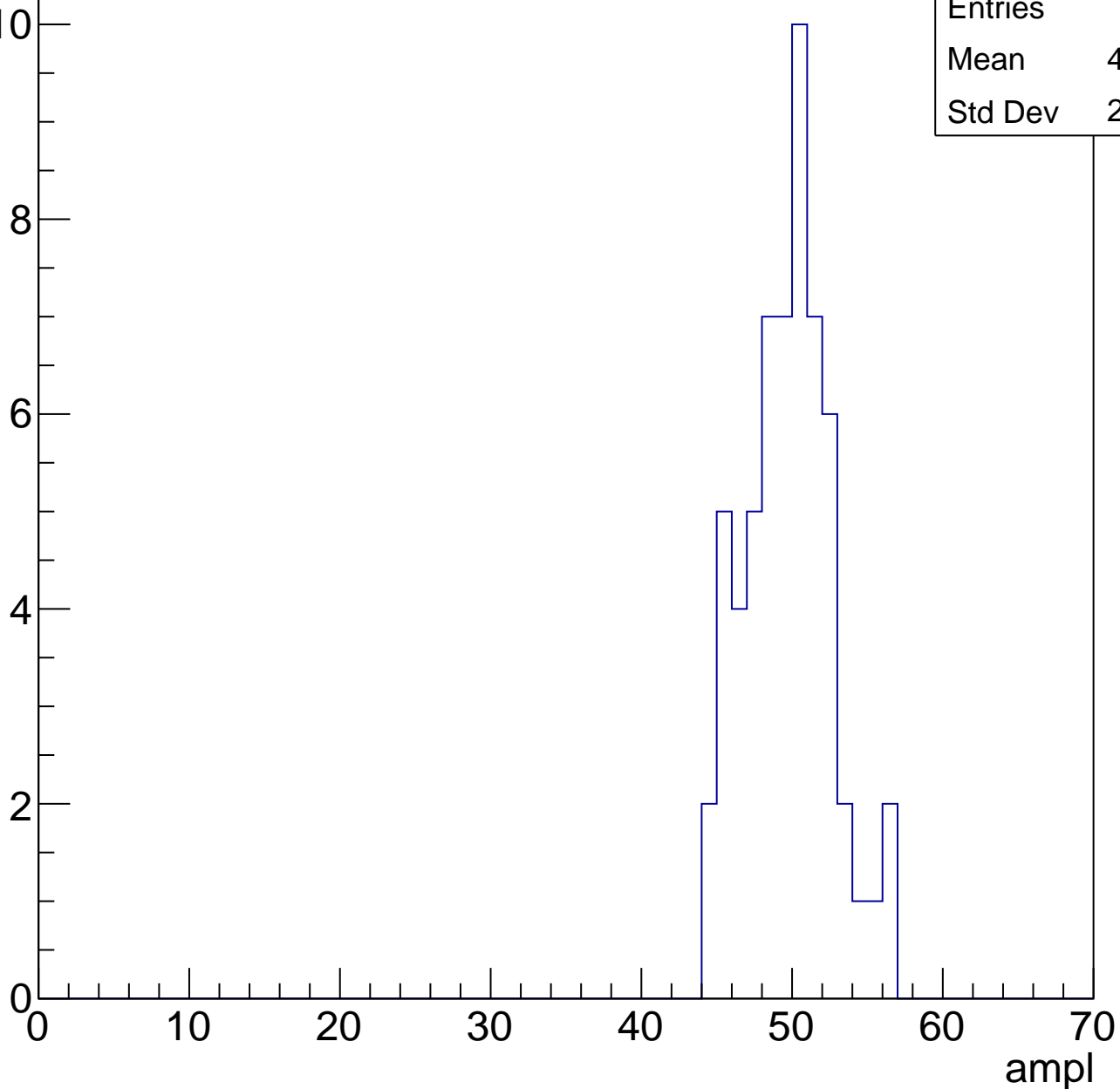


B1L103S, U11-ch41, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	49.27
Std Dev	2.827

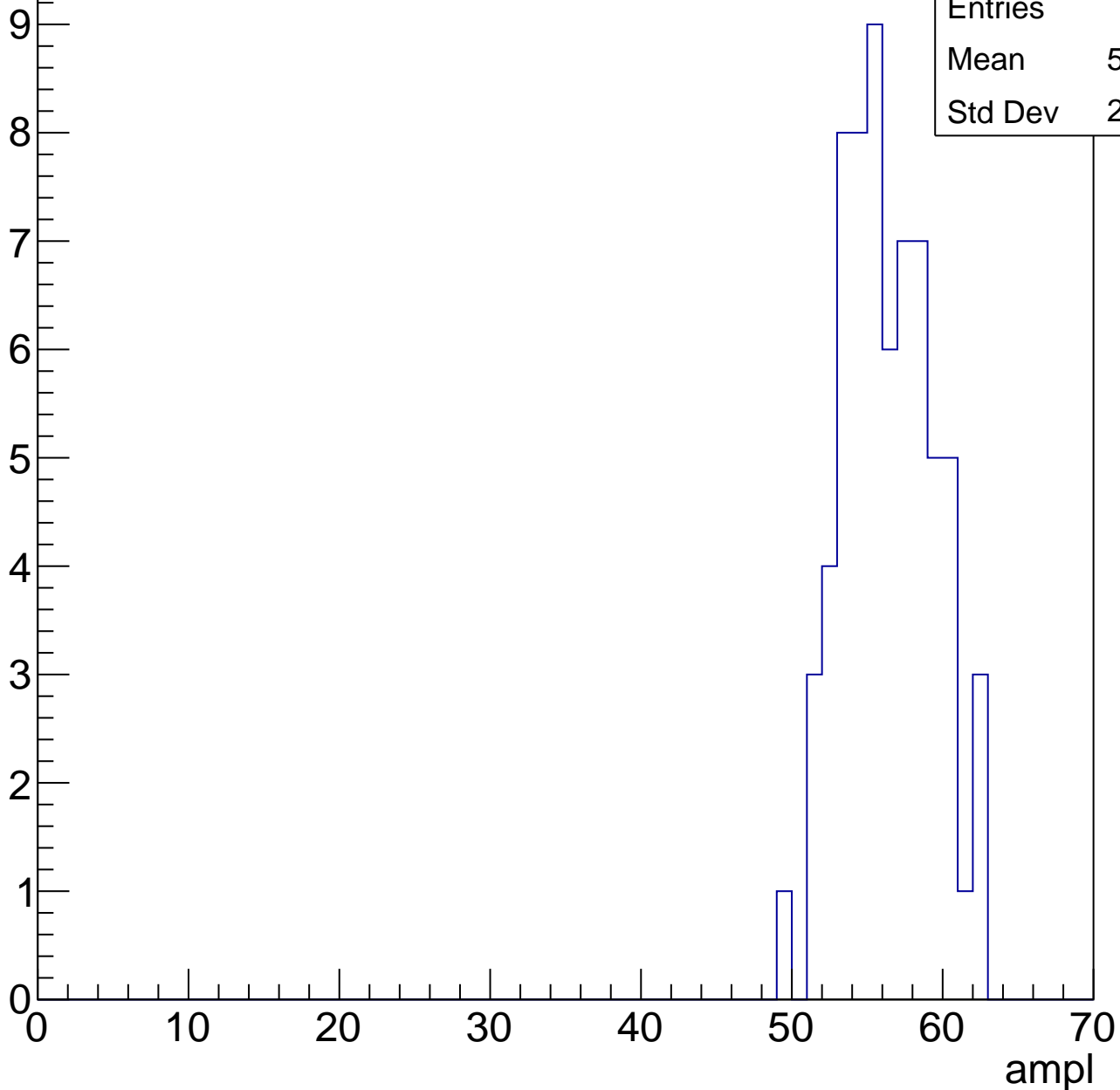


B1L103S, U11-ch41, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	55.88
Std Dev	2.975

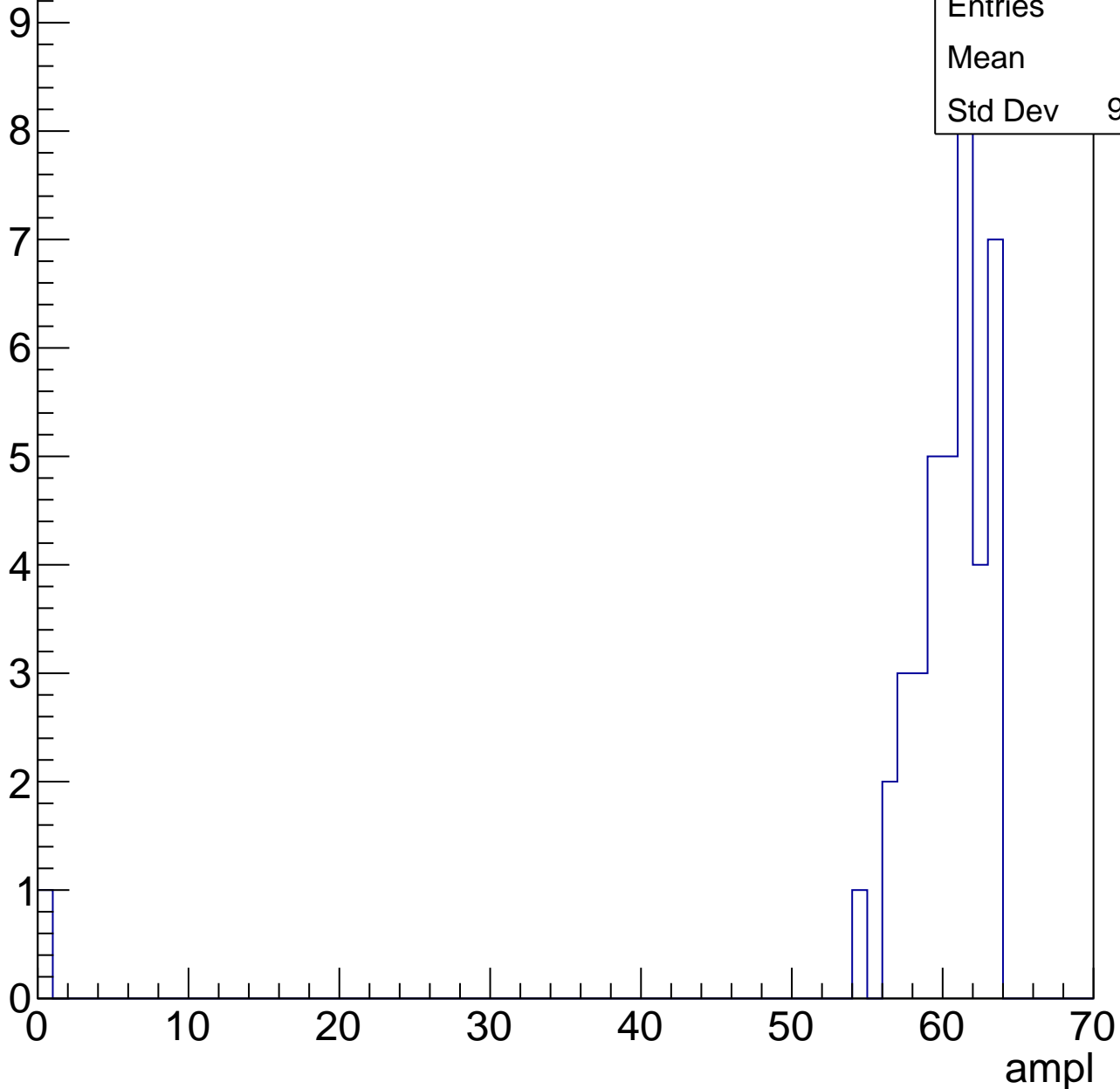


B1L103S, U11-ch41, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

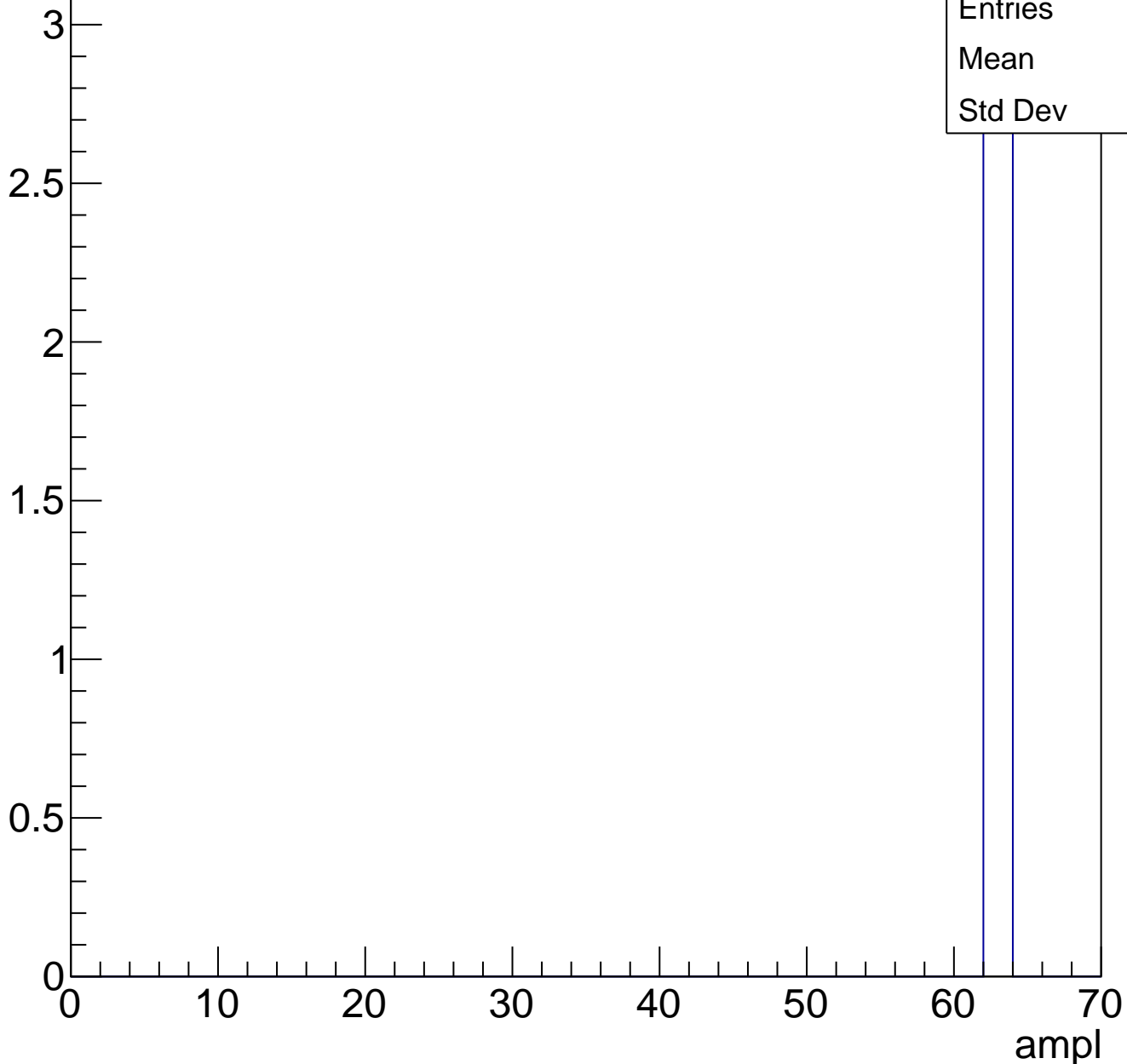
Entries	40
Mean	58.6
Std Dev	9.646



B1L103S, U11-ch41, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch41, adc7

calib_packv5_041523_1651.root, FC#0, port C2

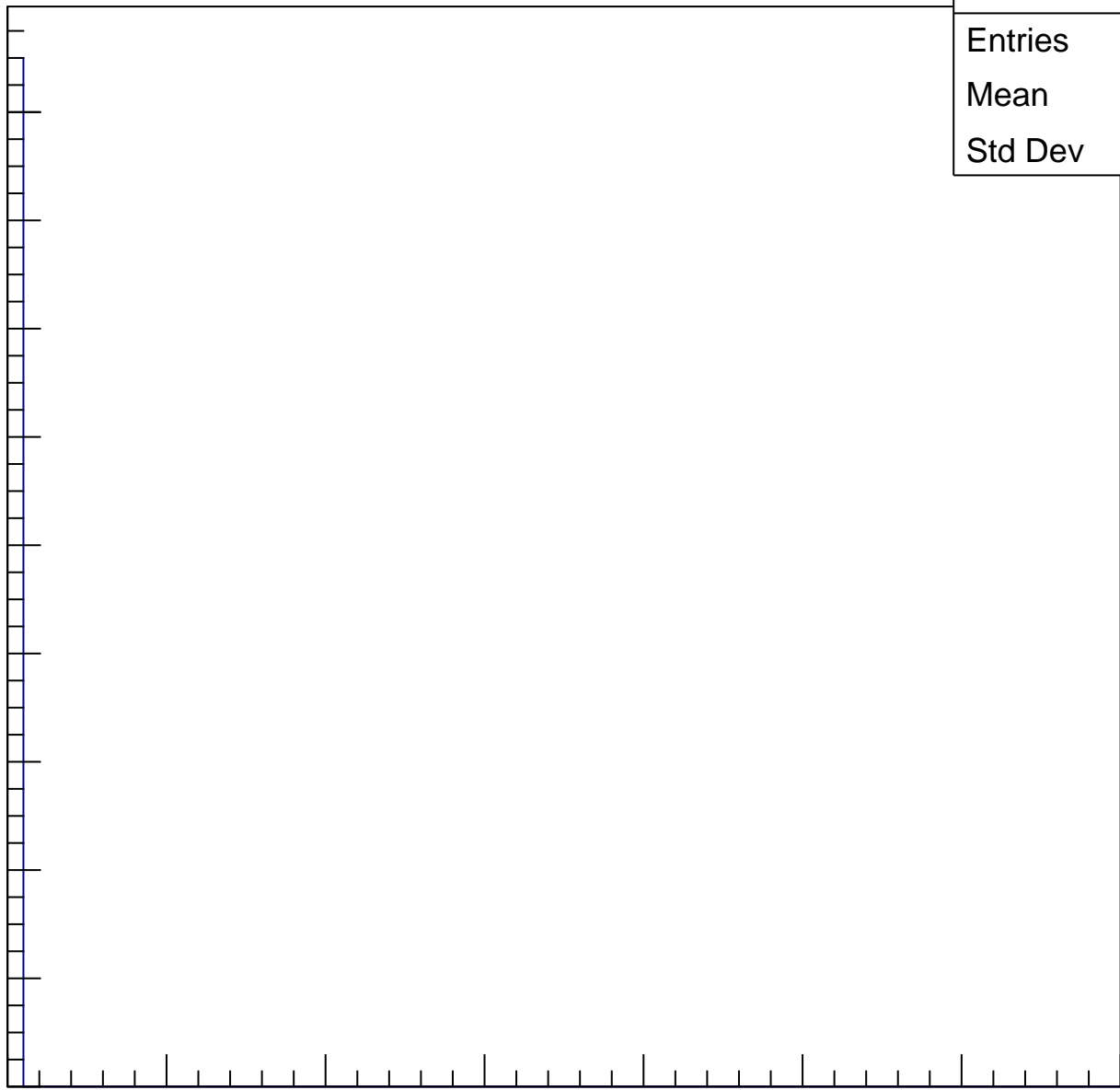
Entries	19
Mean	0
Std Dev	0

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl



B1L103S, U11-ch42, adc0

calib_packv5_041523_1651.root, FC#0, port C2

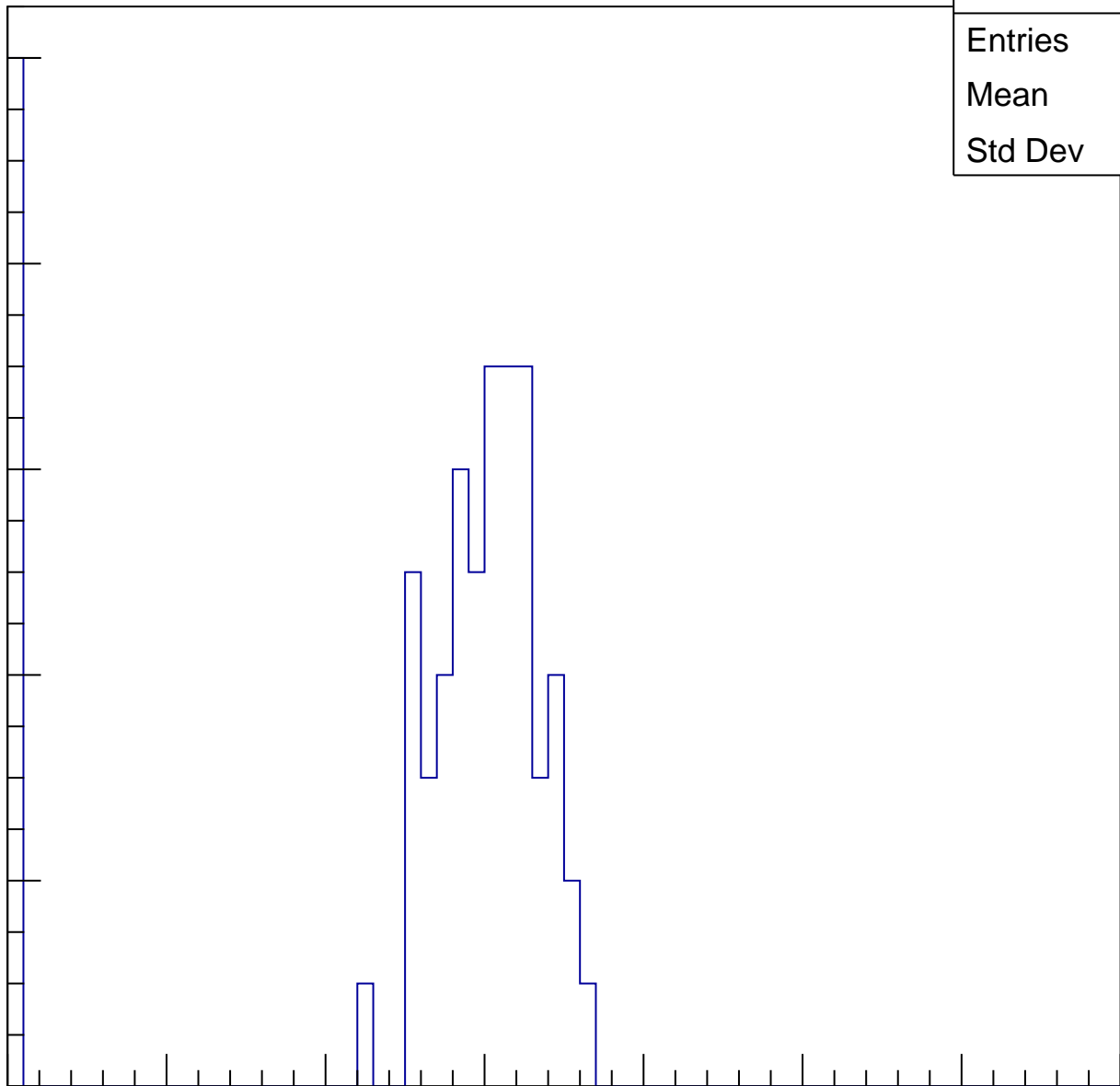
Entries	65
Mean	25.2
Std Dev	11.11

Entry

10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

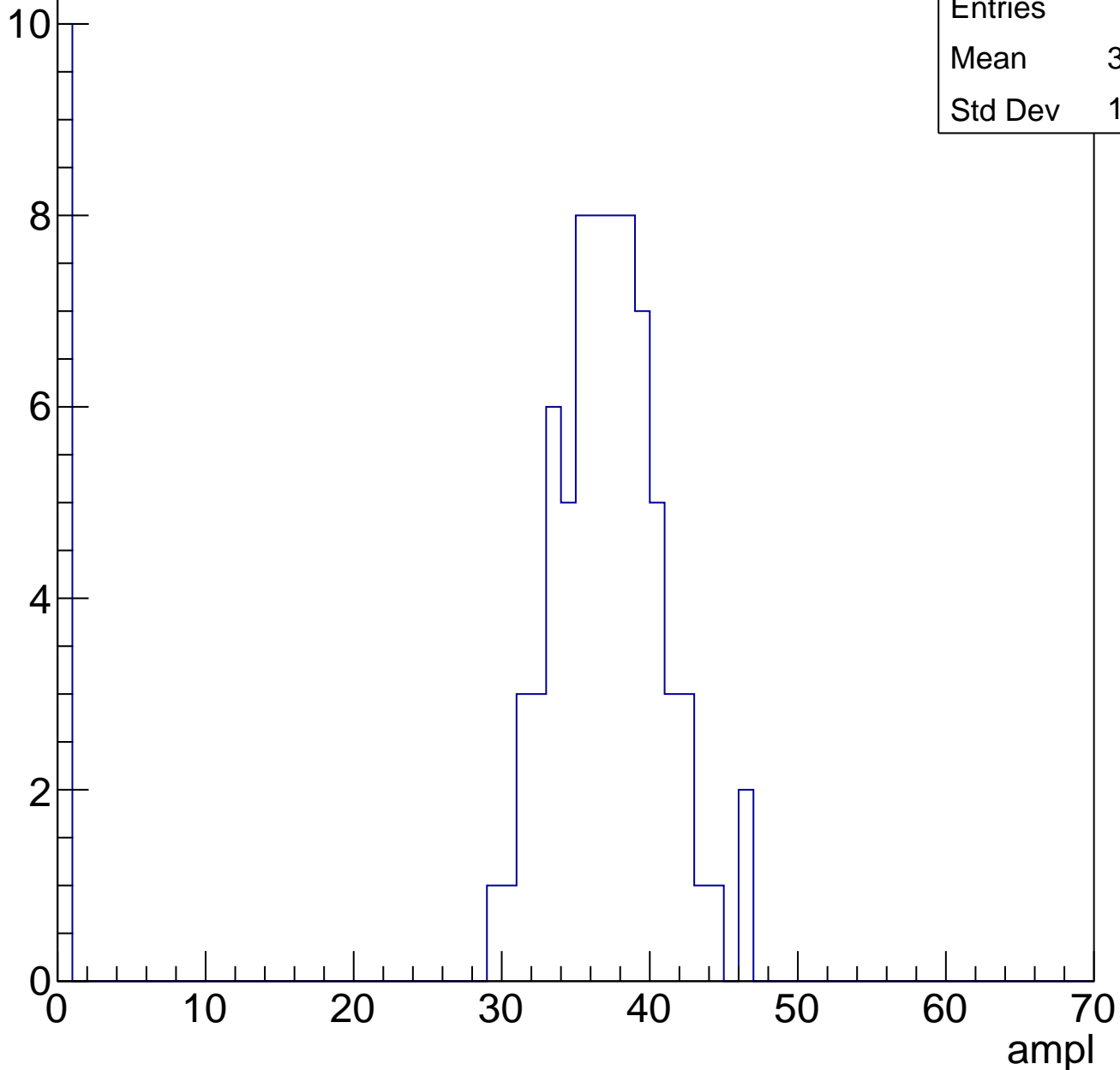


B1L103S, U11-ch42, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	83
Mean	32.35
Std Dev	12.43

Entry



B1L103S, U11-ch42, adc2

calib_packv5_041523_1651.root, FC#0, port C2

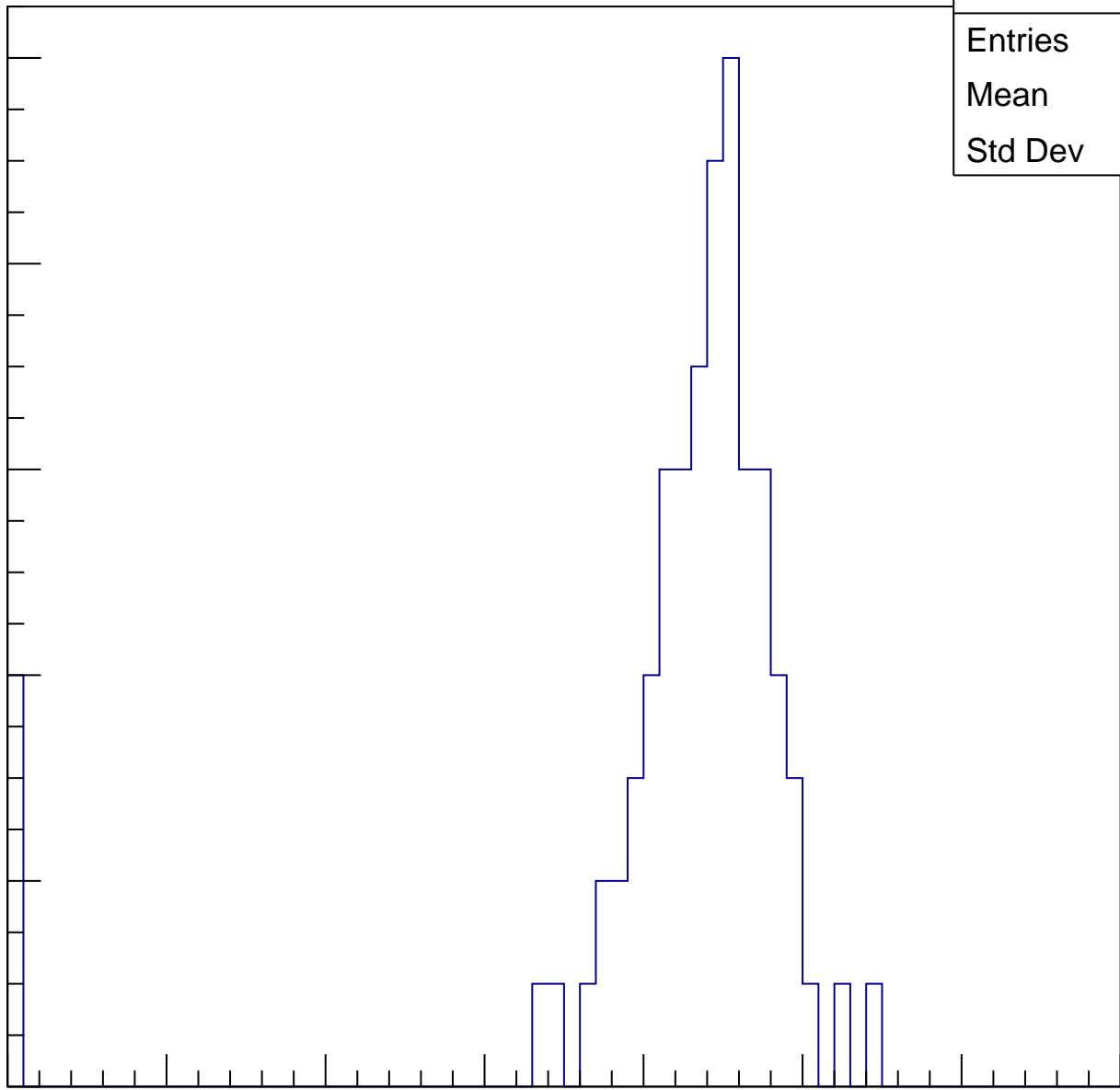
Entries	78
Mean	41.38
Std Dev	10.33

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

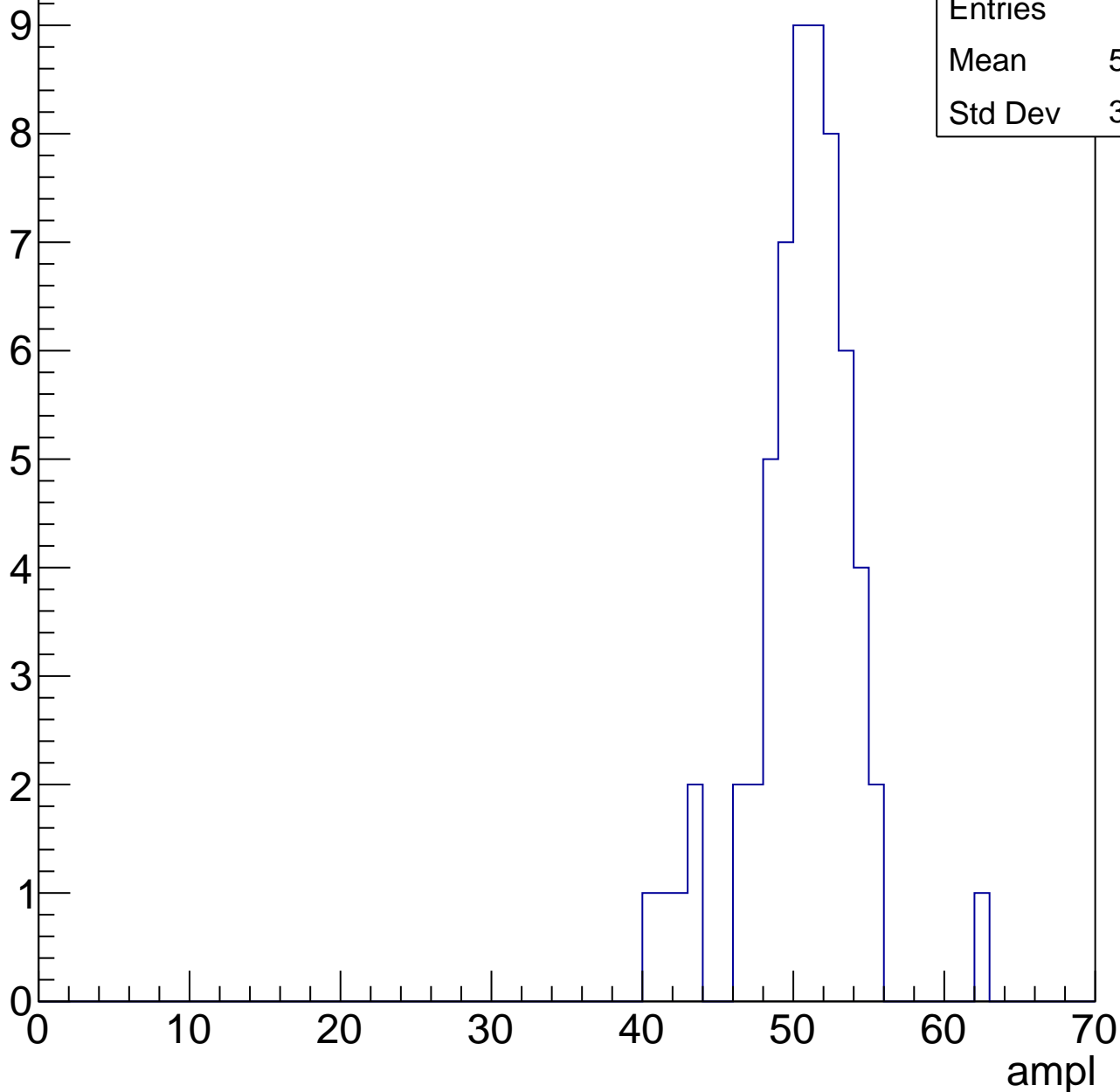


B1L103S, U11-ch42, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	50.15
Std Dev	3.586

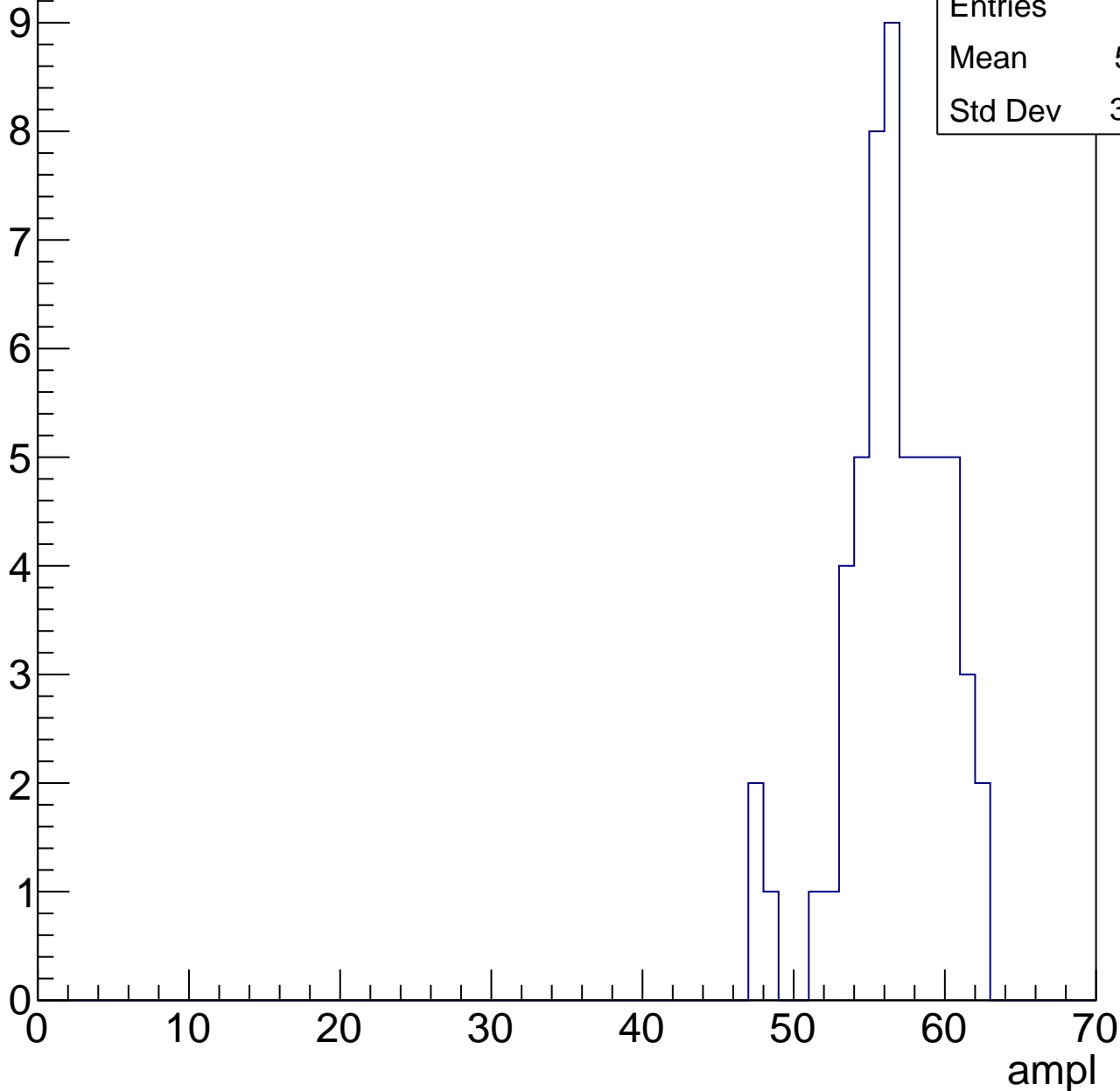


B1L103S, U11-ch42, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	56.21
Std Dev	3.342

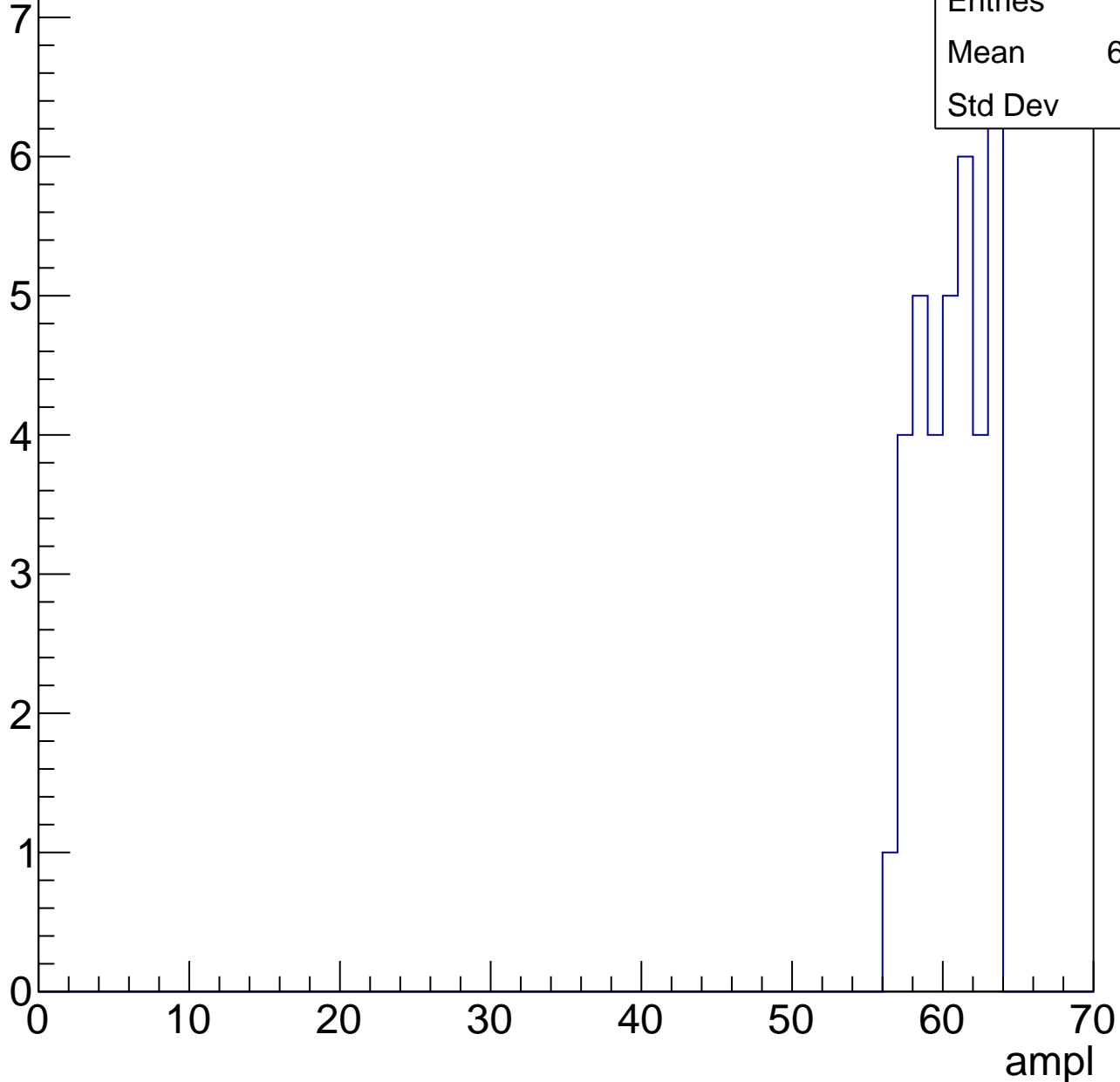


B1L103S, U11-ch42, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	36
Mean	60.14
Std Dev	2.11



B1L103S, U11-ch42, adc6

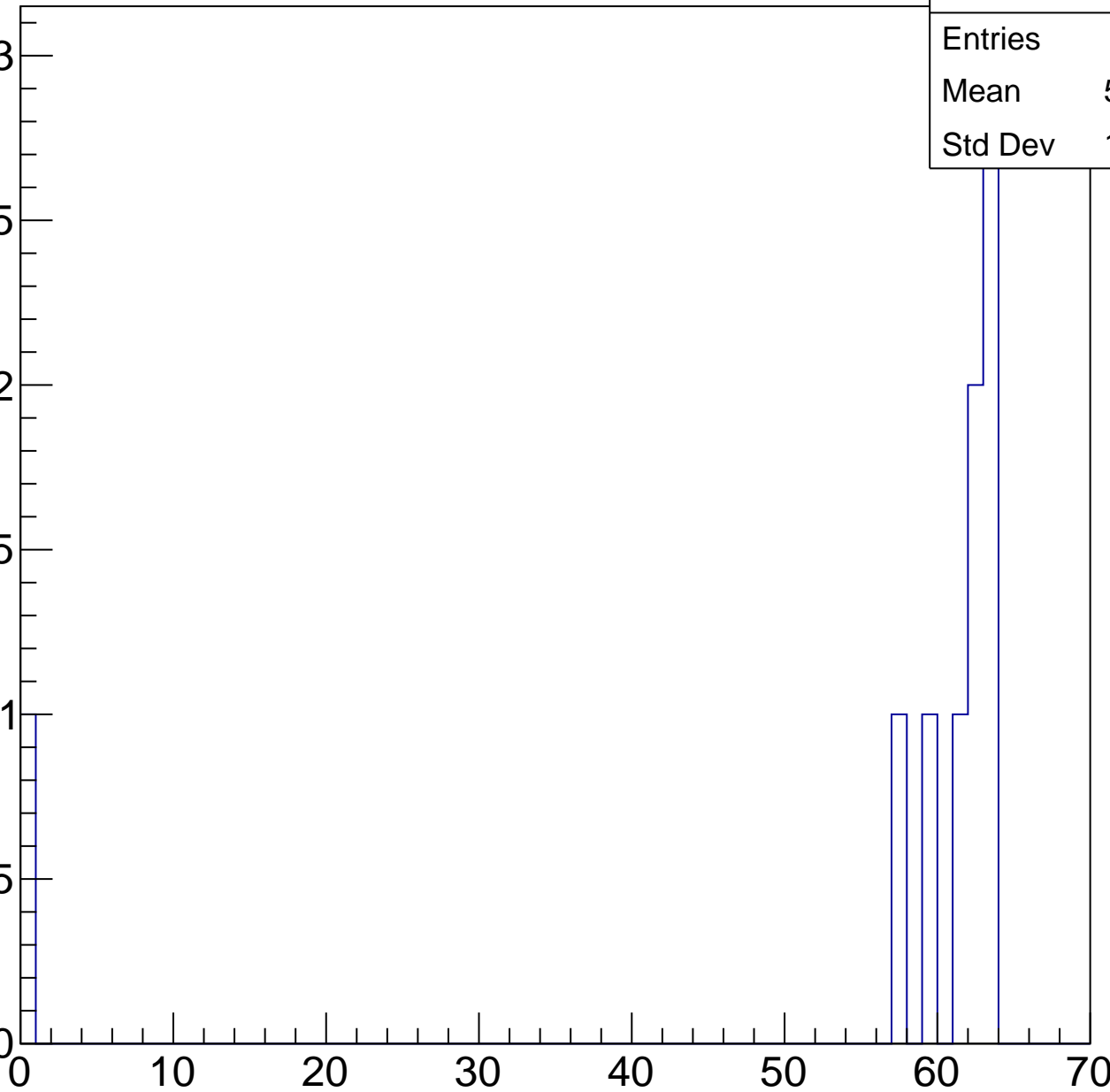
calib_packv5_041523_1651.root, FC#0, port C2

Entry

3
2.5
2
1.5
1
0.5
0

Entries	9
Mean	54.44
Std Dev	19.35

ampl



B1L103S, U11-ch42, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51

Entry



B1L103S, U11-ch43, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	71
Mean	25.58
Std Dev	11.33

Entry

10

8

6

4

2

0

0

10

20

30

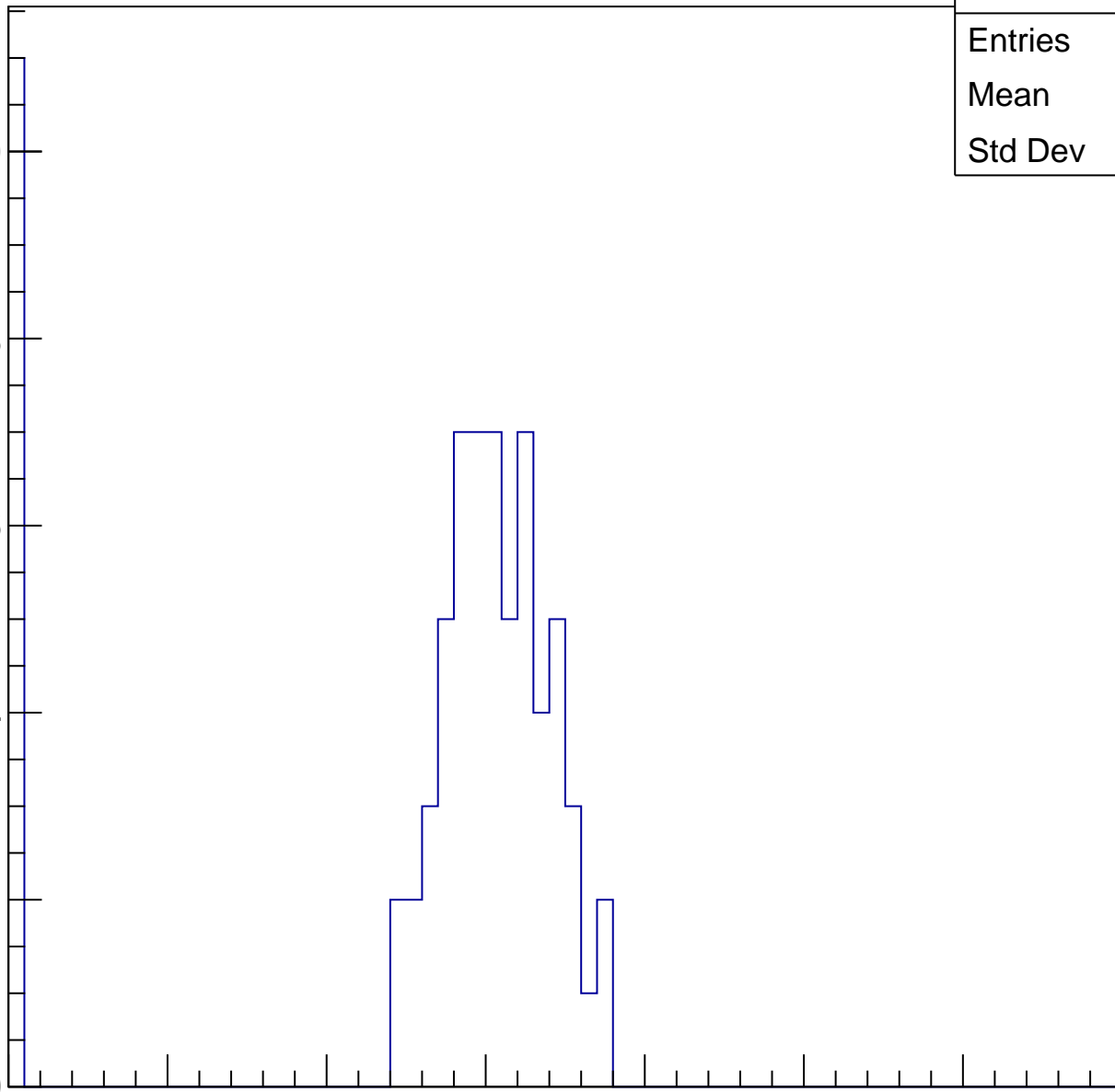
40

50

60

70

ampl



B1L103S, U11-ch43, adc1

calib_packv5_041523_1651.root, FC#0, port C2

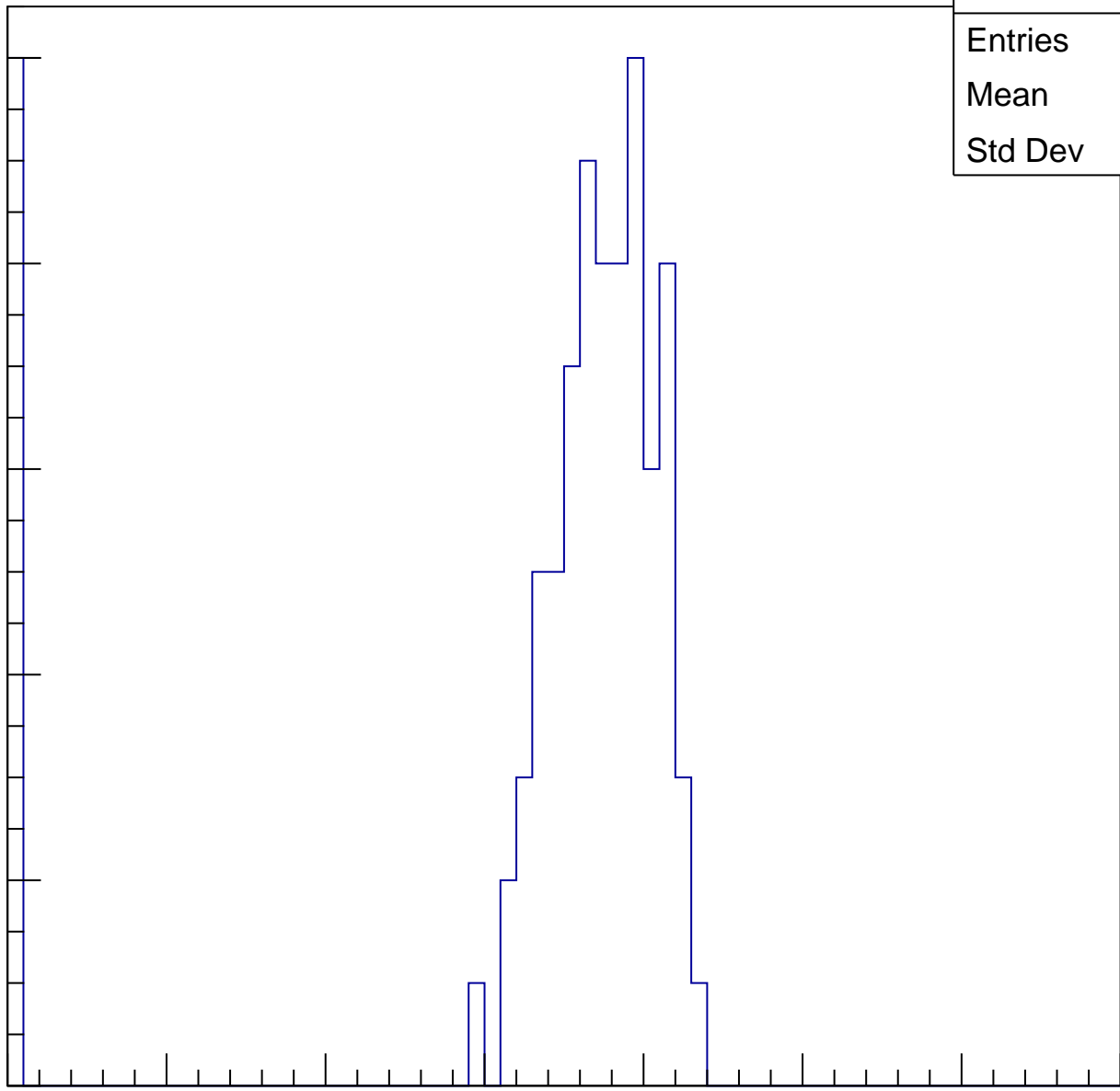
Entries	86
Mean	32.77
Std Dev	12.23

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

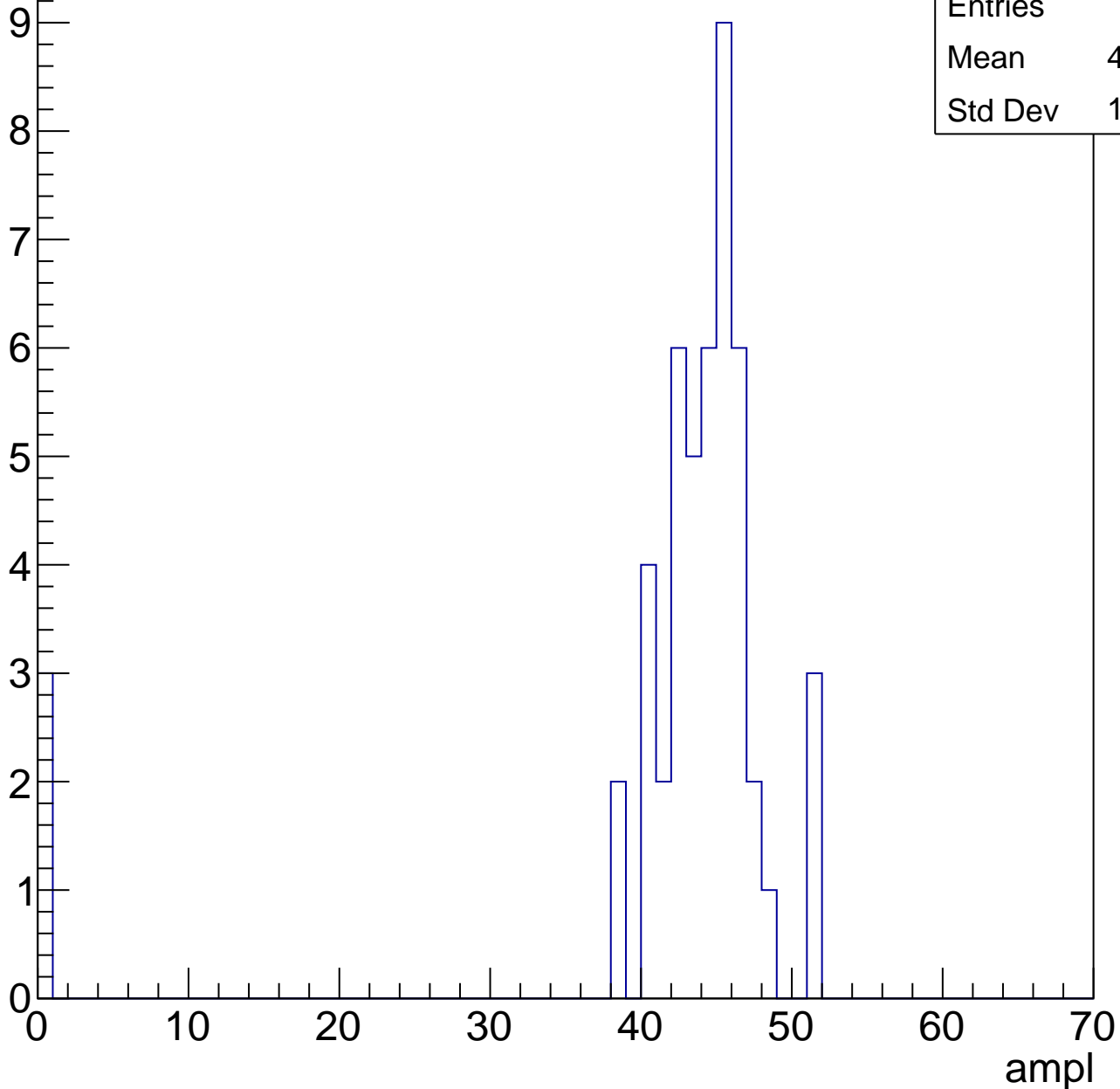


B1L103S, U11-ch43, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	41.33
Std Dev	10.93

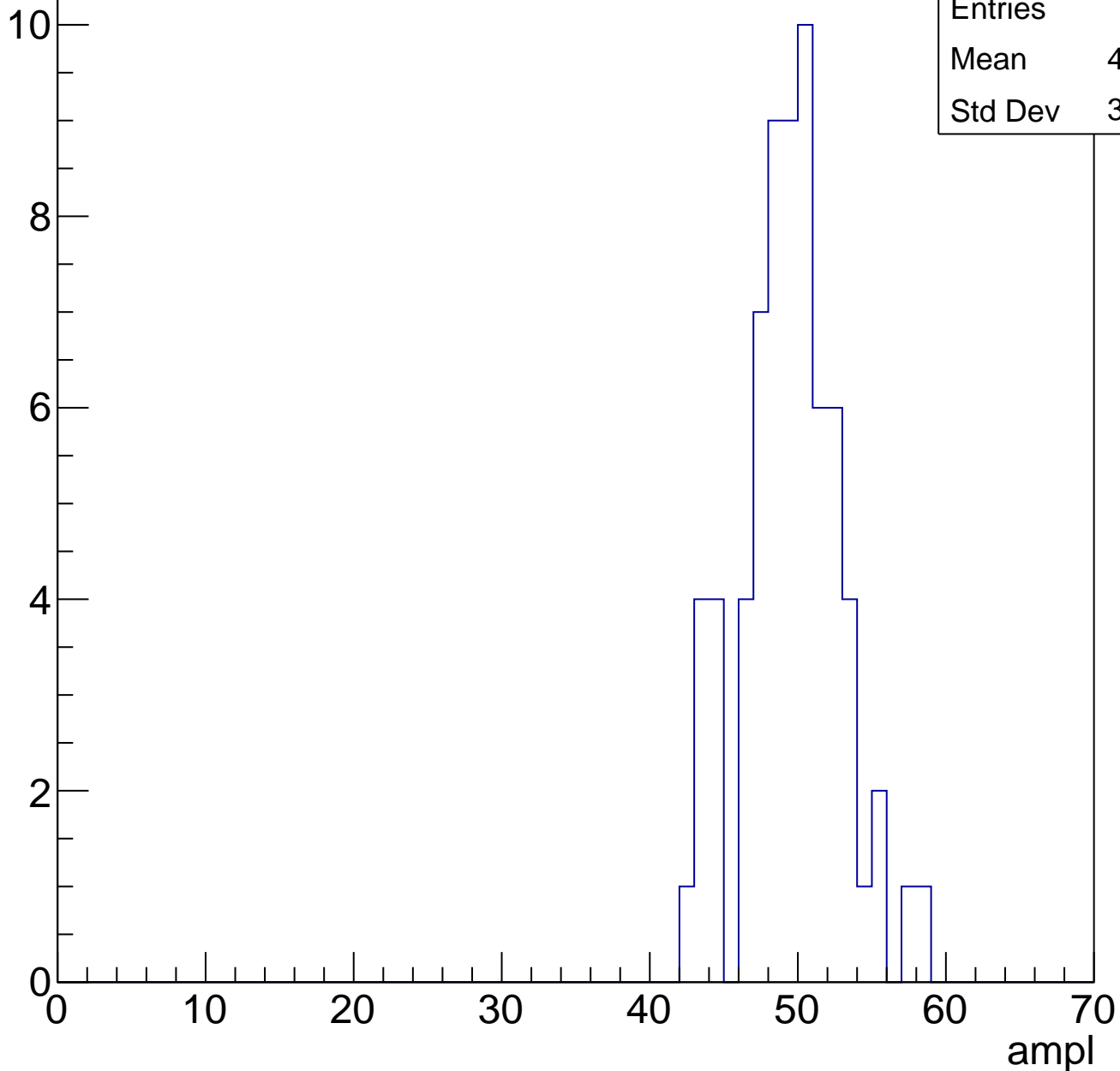


B1L103S, U11-ch43, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	69
Mean	49.06
Std Dev	3.318

Entry

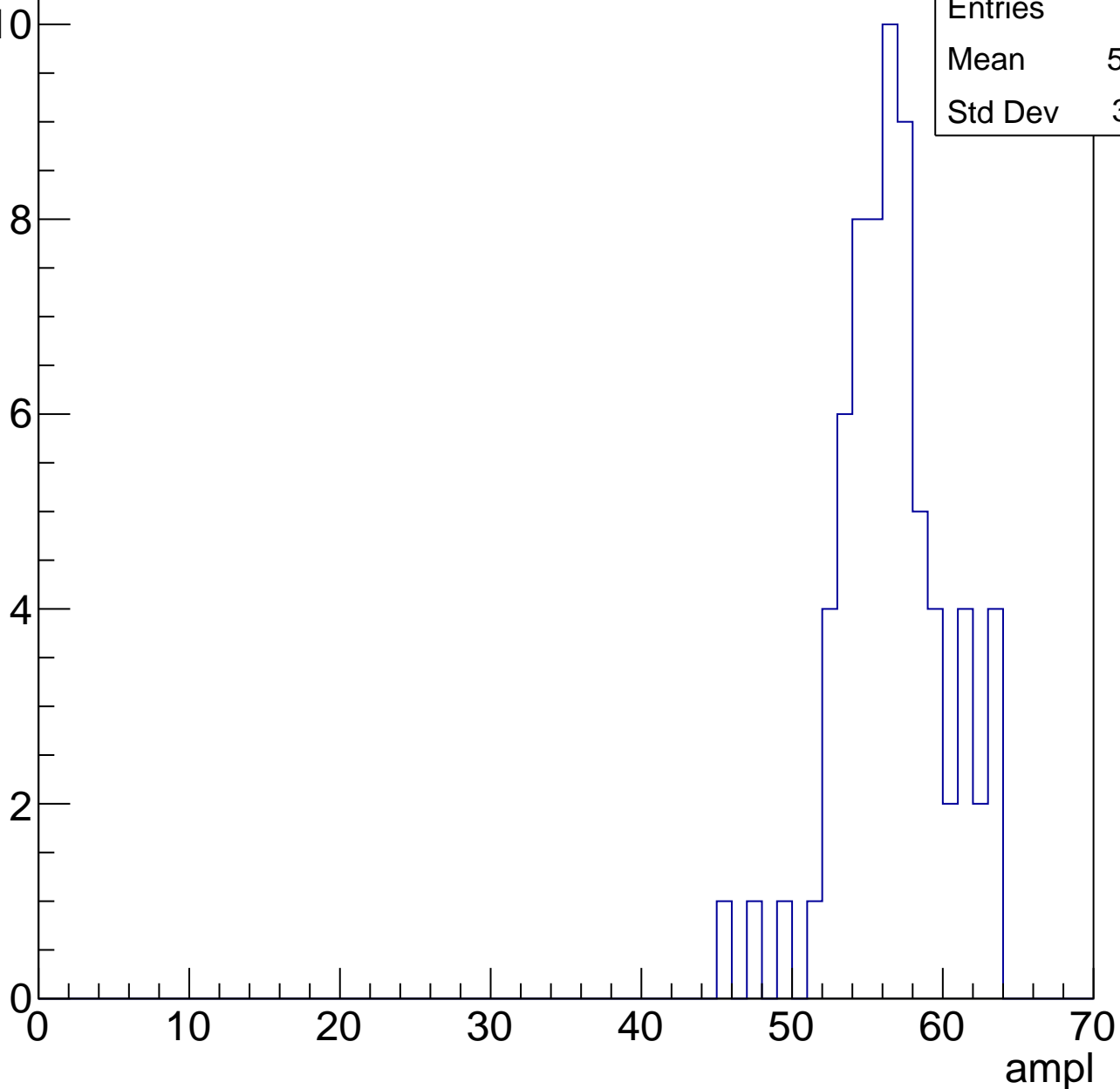


B1L103S, U11-ch43, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	56.13
Std Dev	3.581

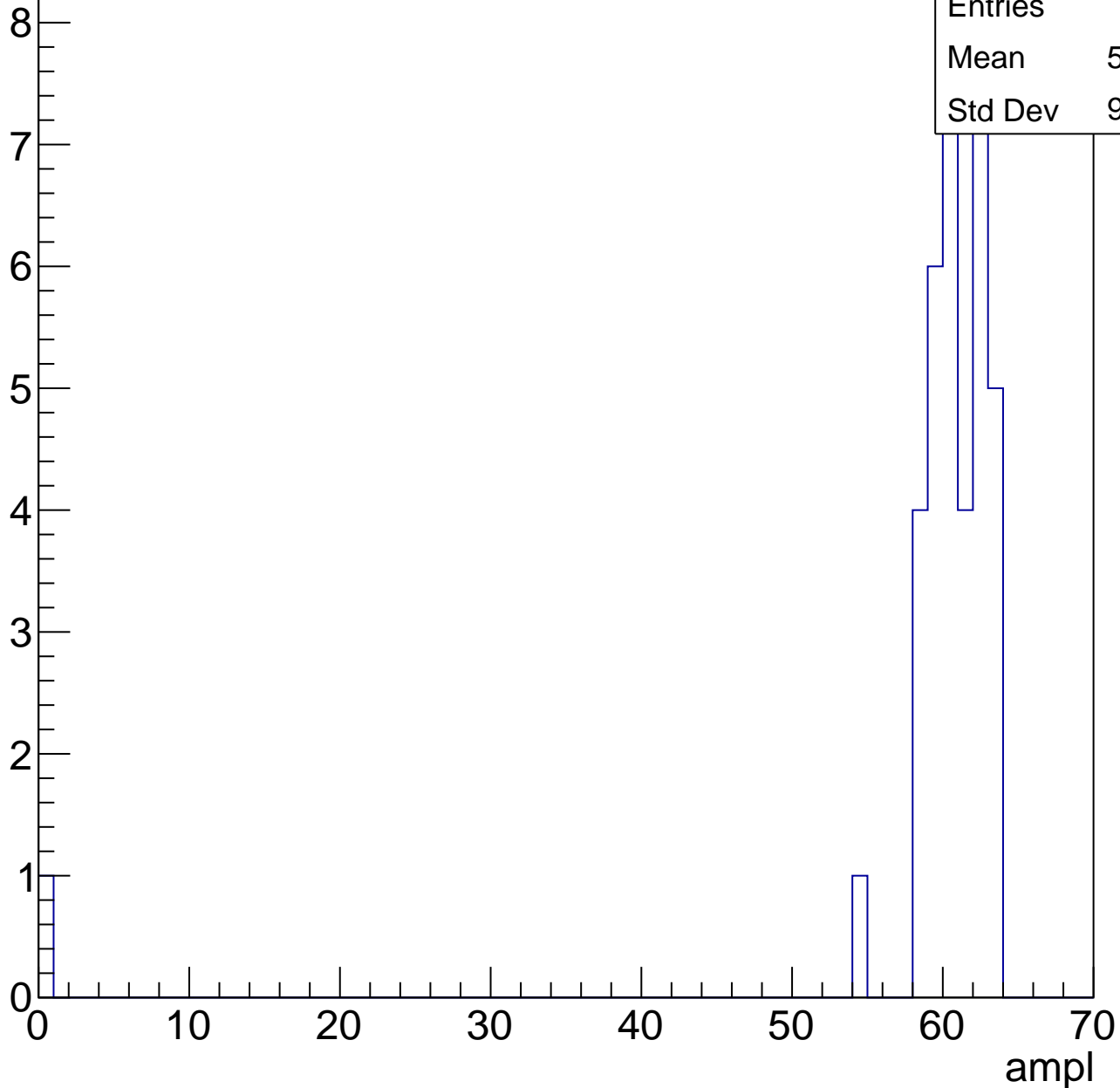


B1L103S, U11-ch43, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	37
Mean	58.78
Std Dev	9.979



B1L103S, U11-ch43, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



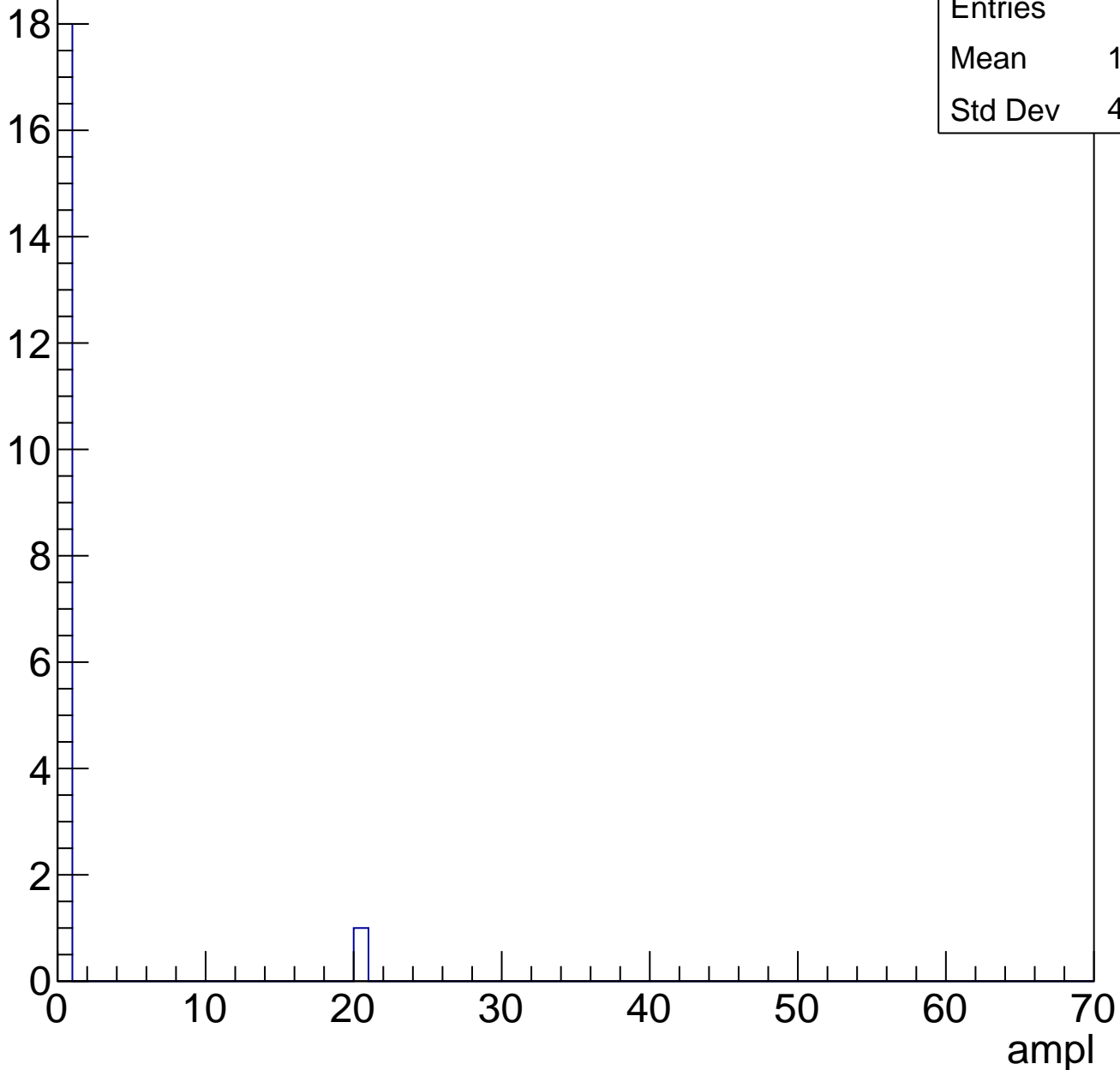
Entries	3
Mean	61.67
Std Dev	0.9428

B1L103S, U11-ch43, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.053
Std Dev	4.466

Entry



B1L103S, U11-ch44, adc0

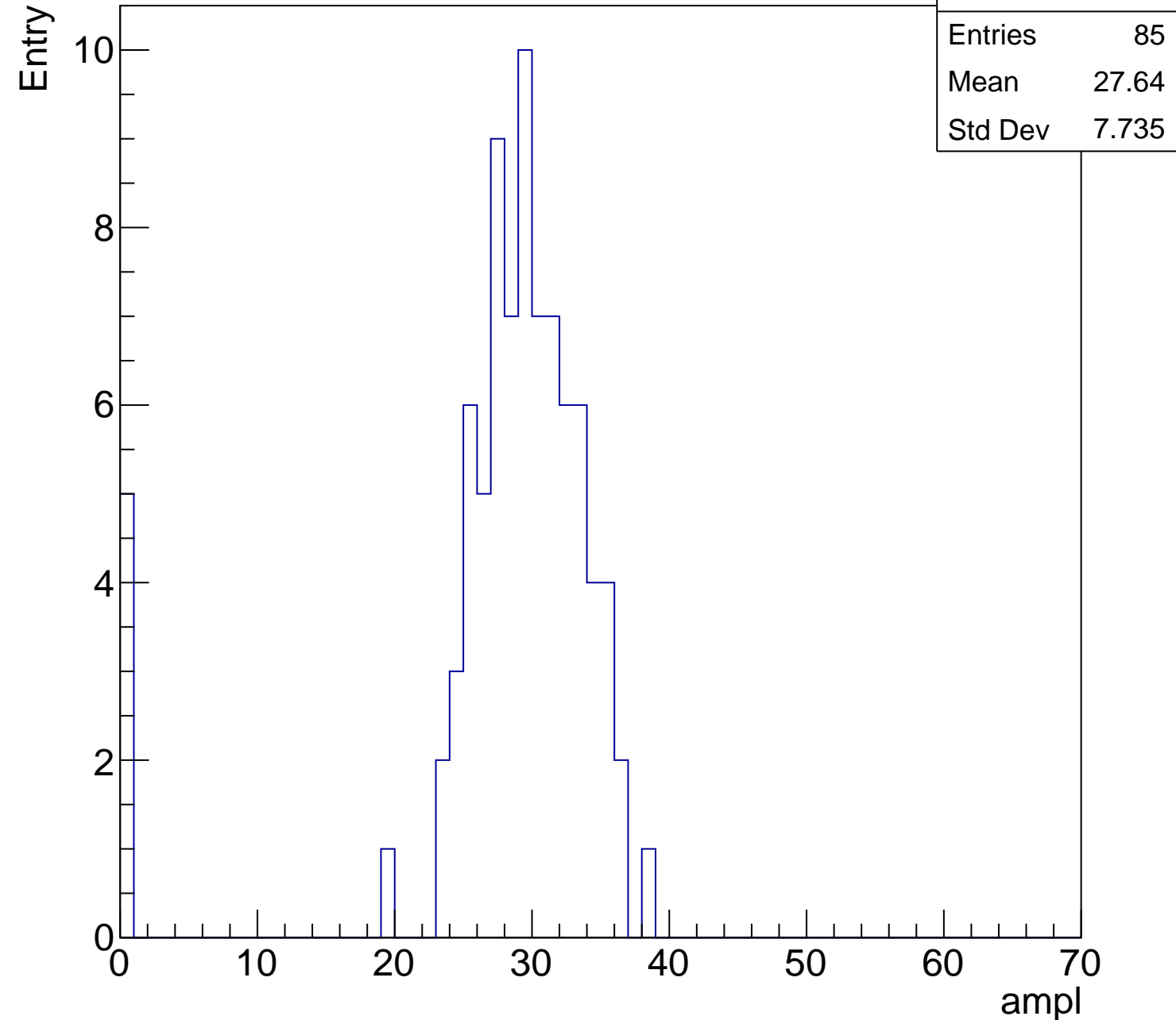
calib_packv5_041523_1651.root, FC#0, port C2

Entries	85
Mean	27.64
Std Dev	7.735

Entry

10
8
6
4
2
0

ampl

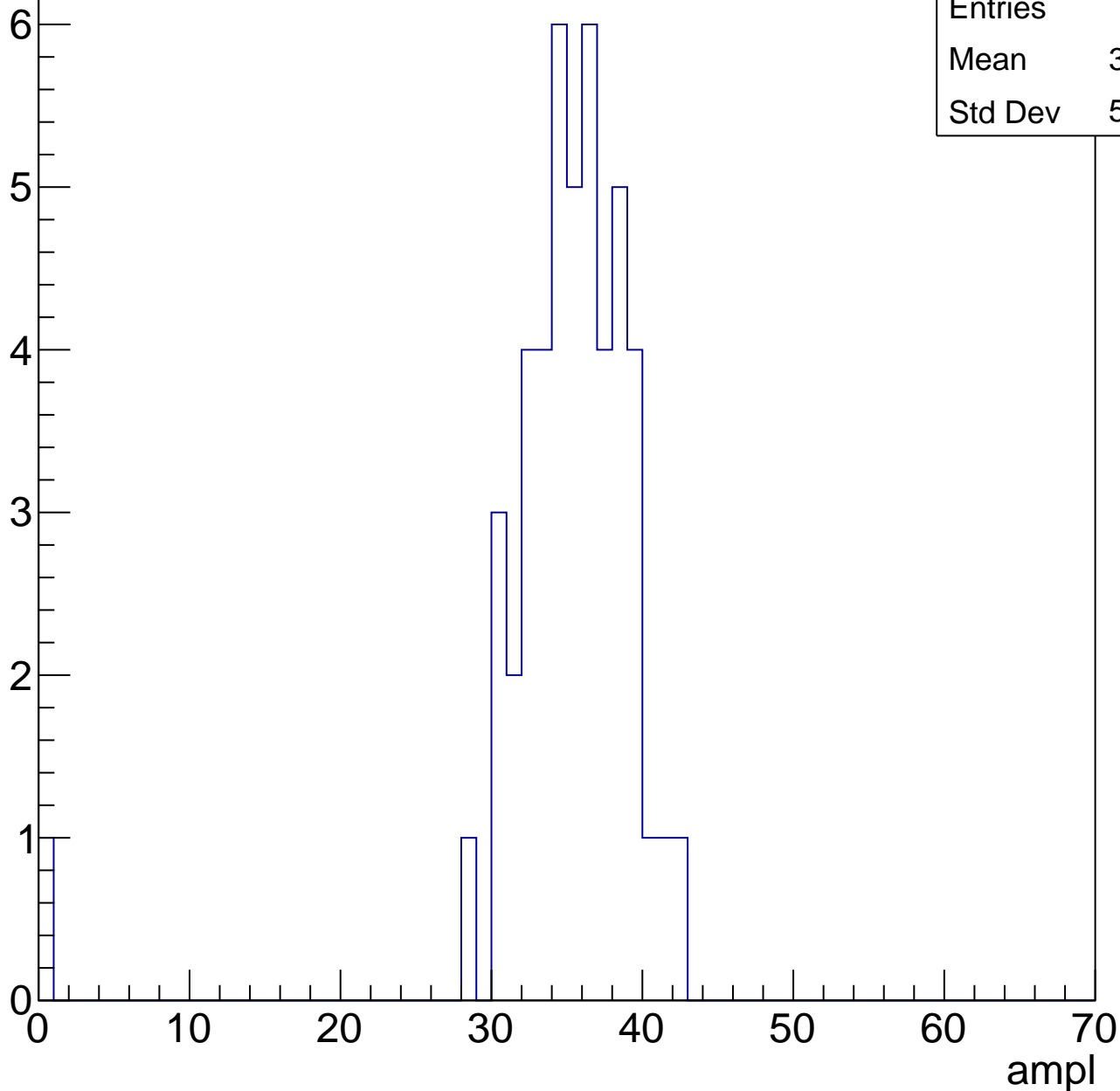


B1L103S, U11-ch44, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	48
Mean	34.42
Std Dev	5.887

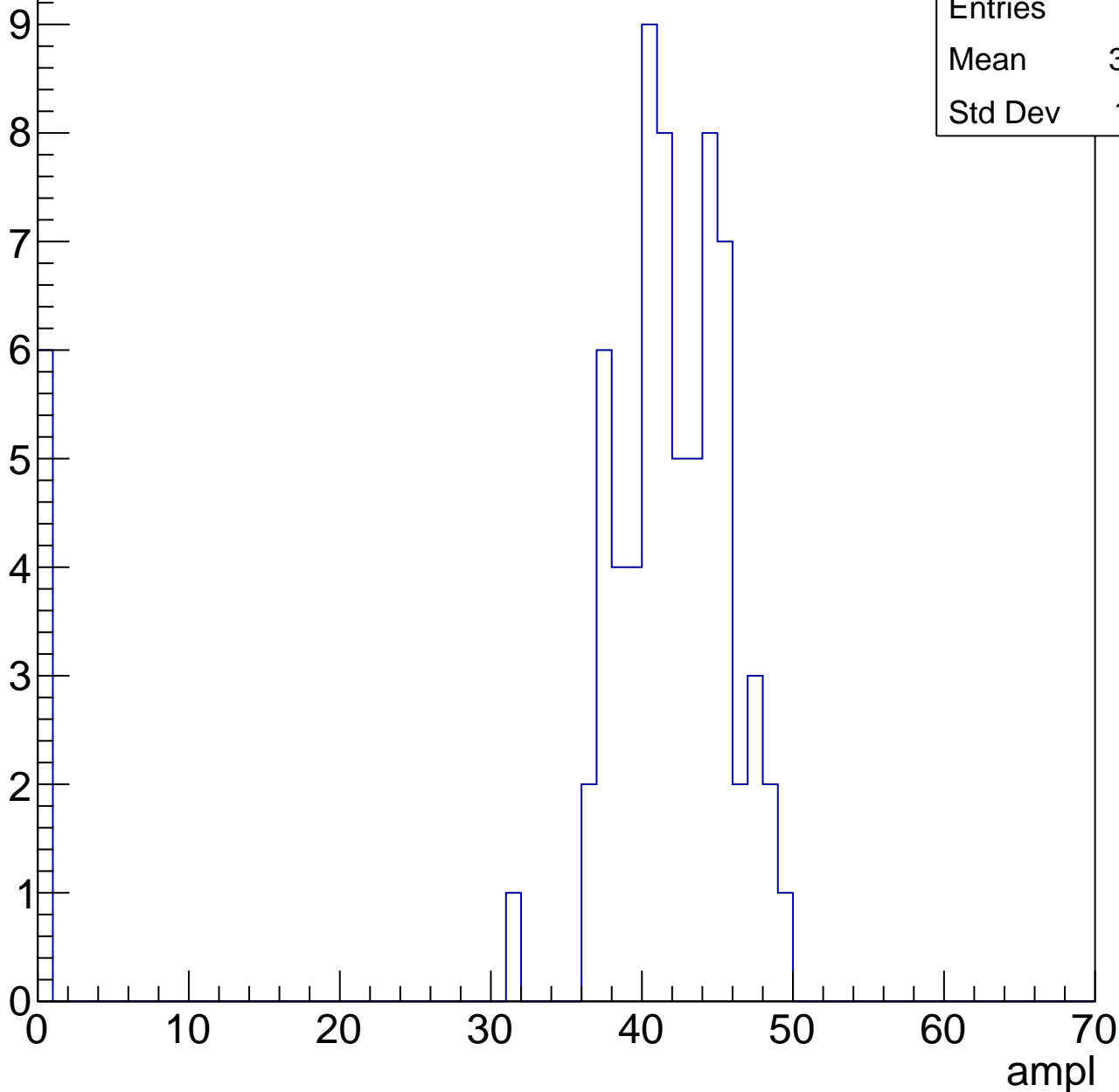


B1L103S, U11-ch44, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	38.23
Std Dev	11.91

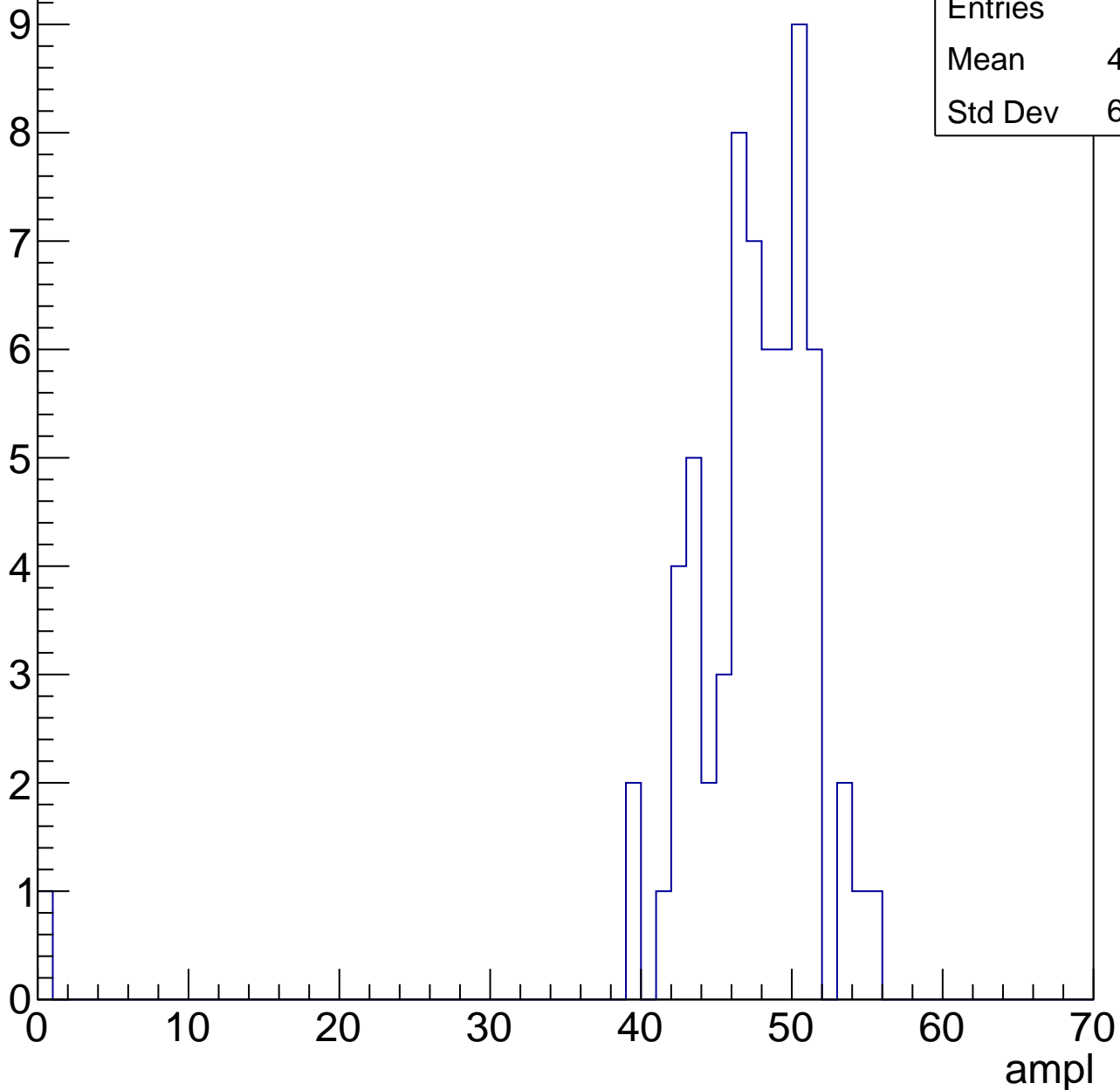


B1L103S, U11-ch44, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	46.48
Std Dev	6.808

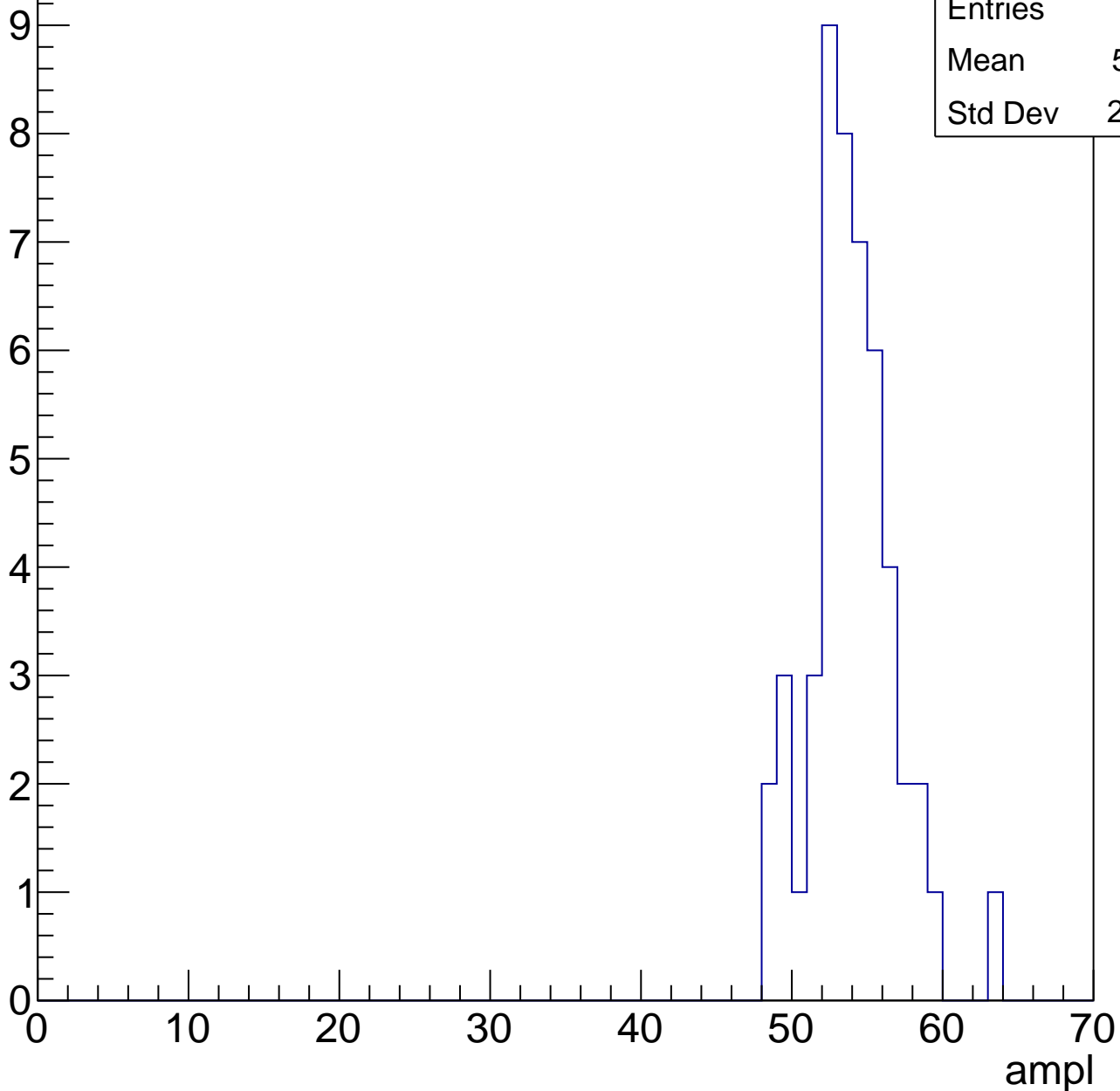


B1L103S, U11-ch44, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	53.51
Std Dev	2.858

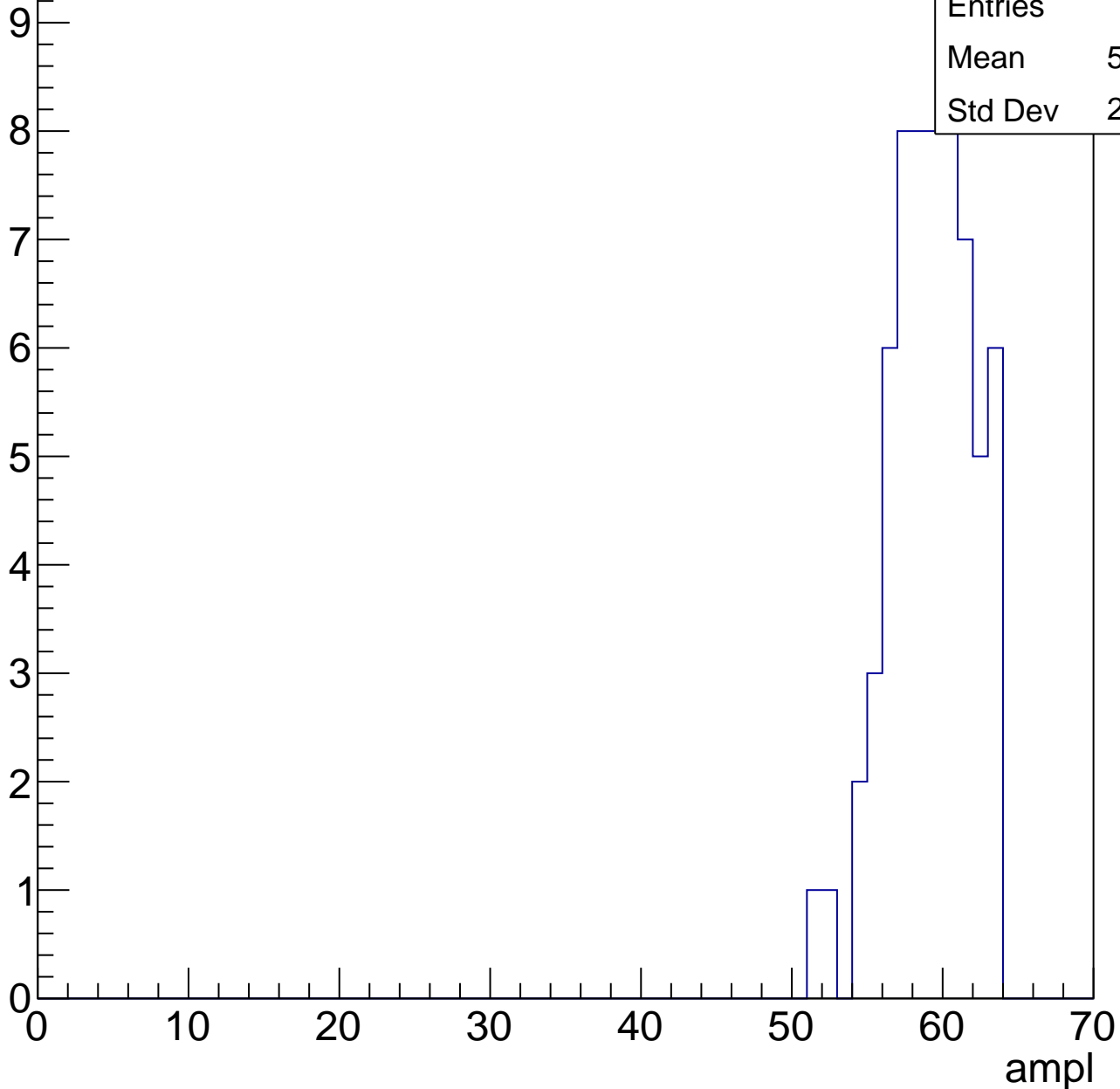


B1L103S, U11-ch44, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	58.73
Std Dev	2.734

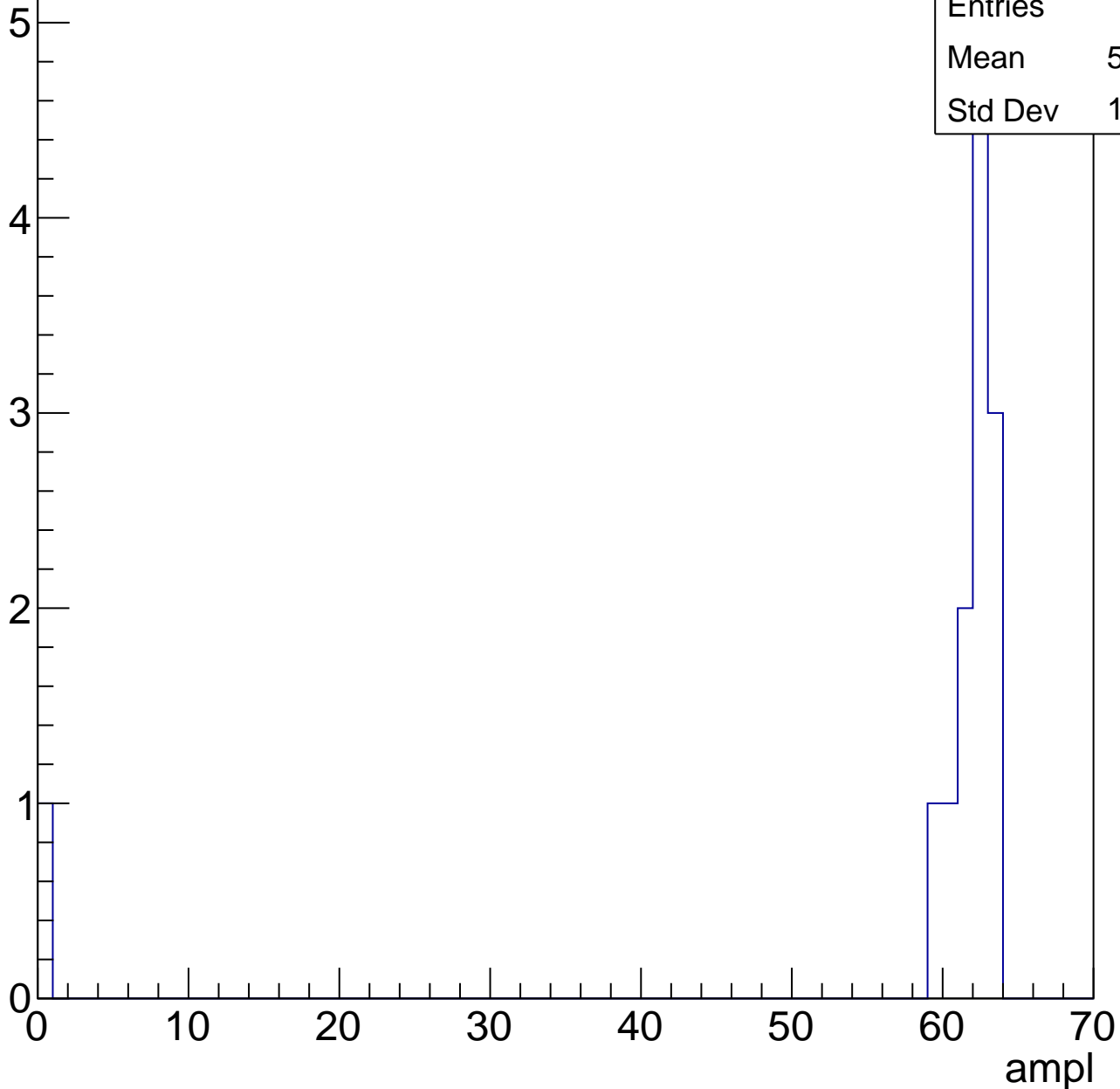


B1L103S, U11-ch44, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	13
Mean	56.92
Std Dev	16.47



B1L103S, U11-ch44, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.05
Std Dev	13.29

Entry

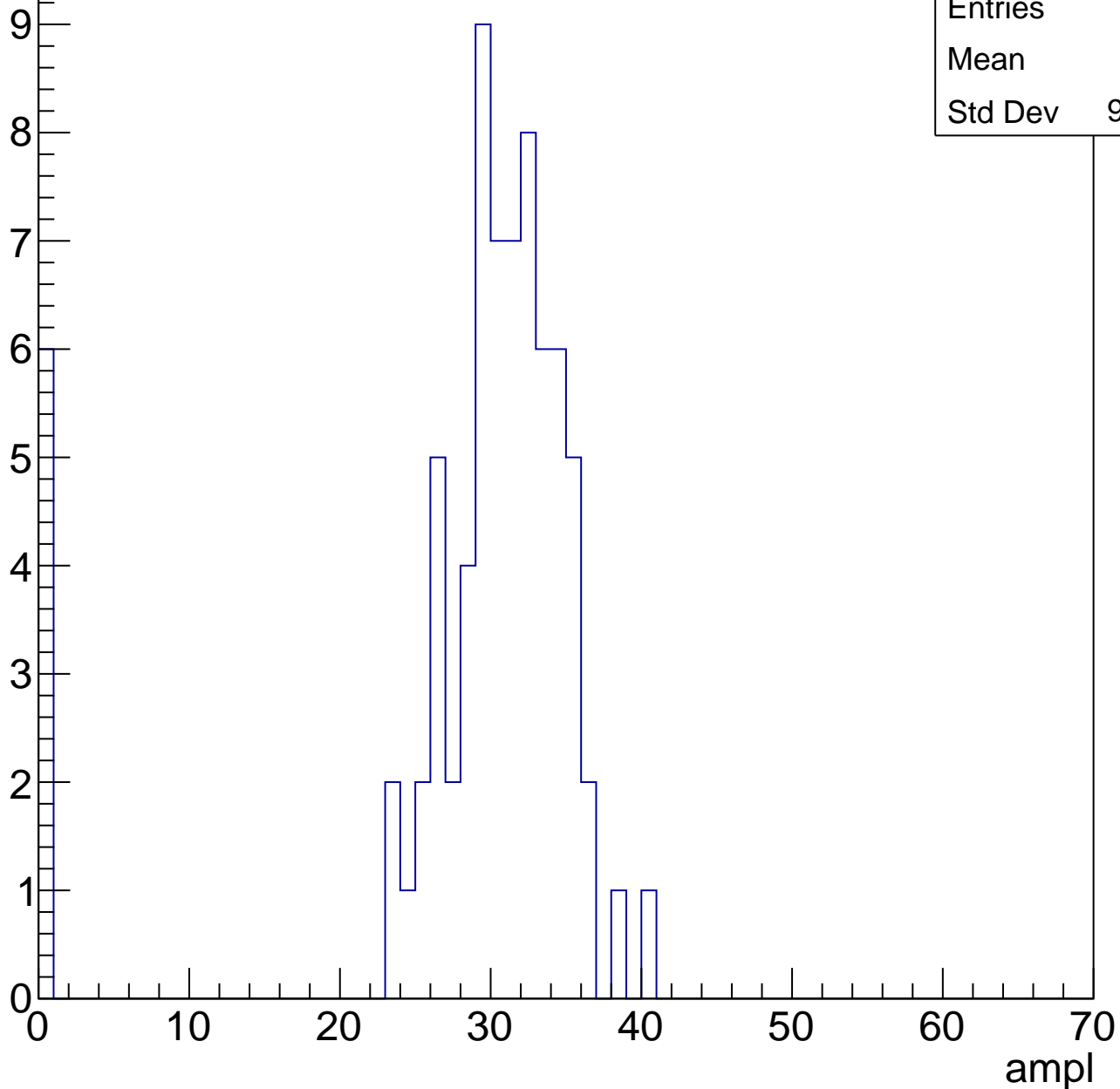


B1L103S, U11-ch45, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	28.2
Std Dev	9.018



B1L103S, U11-ch45, adc1

calib_packv5_041523_1651.root, FC#0, port C2

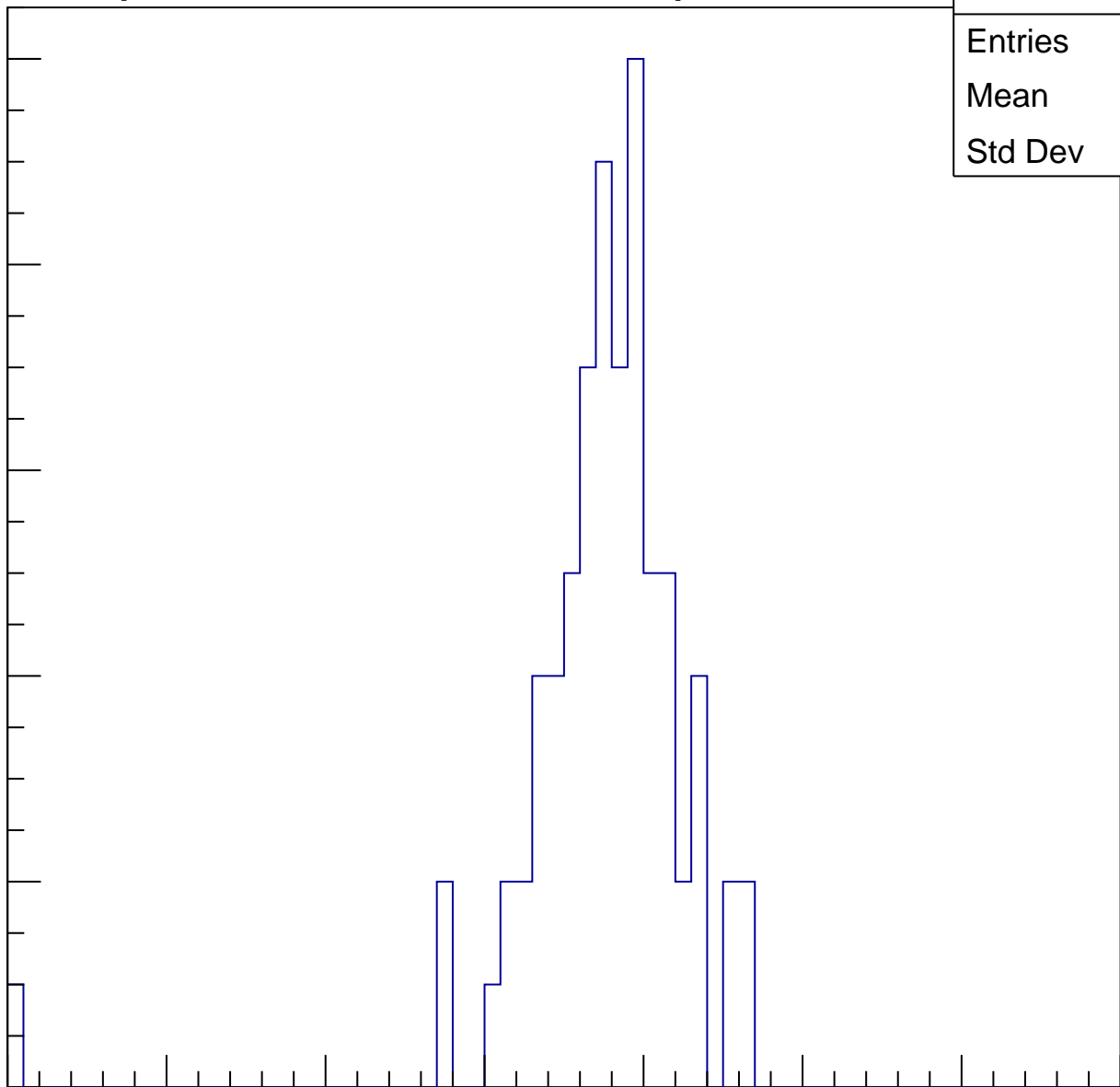
Entries	74
Mean	36.99
Std Dev	5.839

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

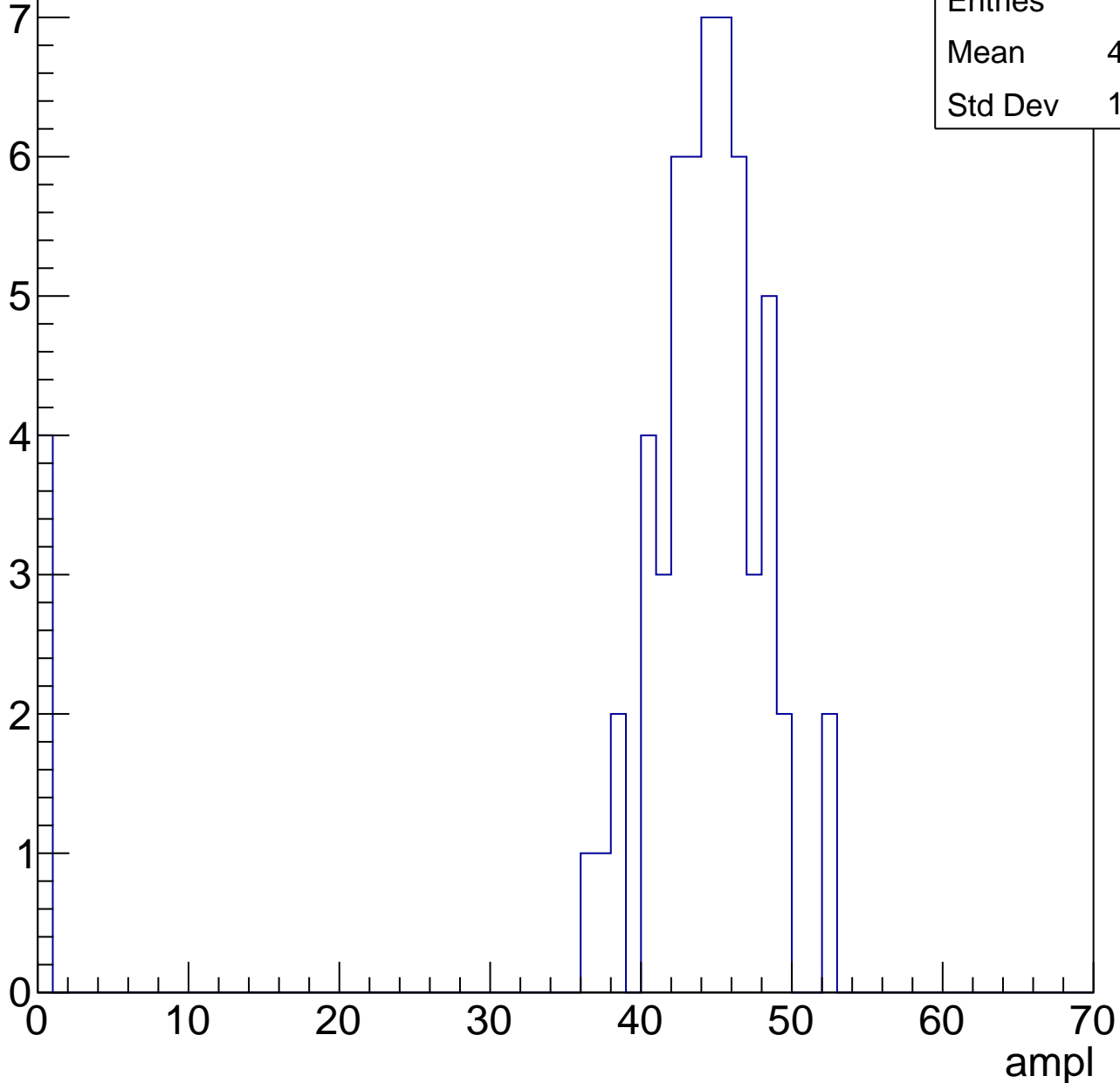


B1L103S, U11-ch45, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	41.08
Std Dev	11.55



B1L103S, U11-ch45, adc3

calib_packv5_041523_1651.root, FC#0, port C2

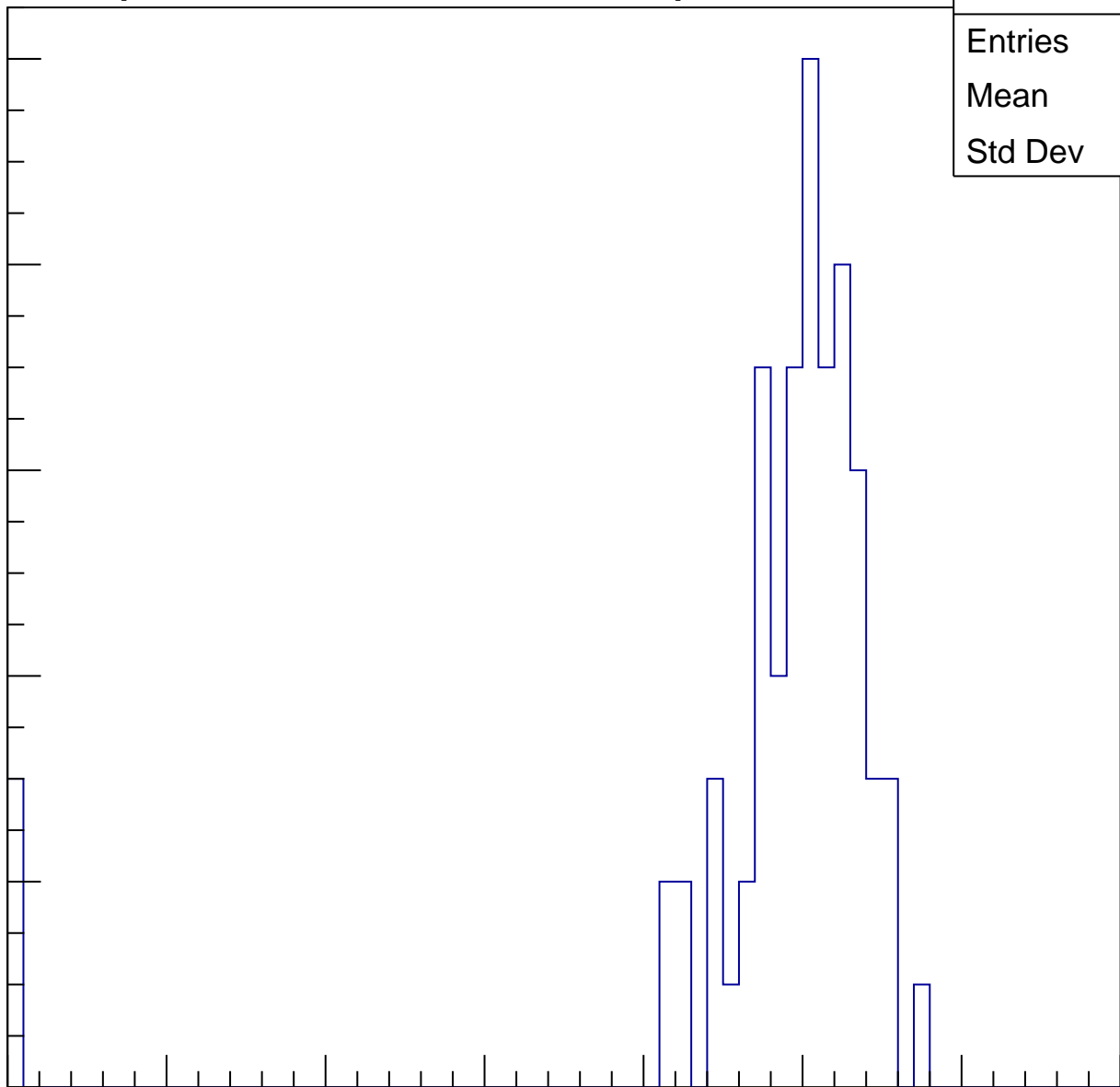
Entries	69
Mean	47.45
Std Dev	10.67

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

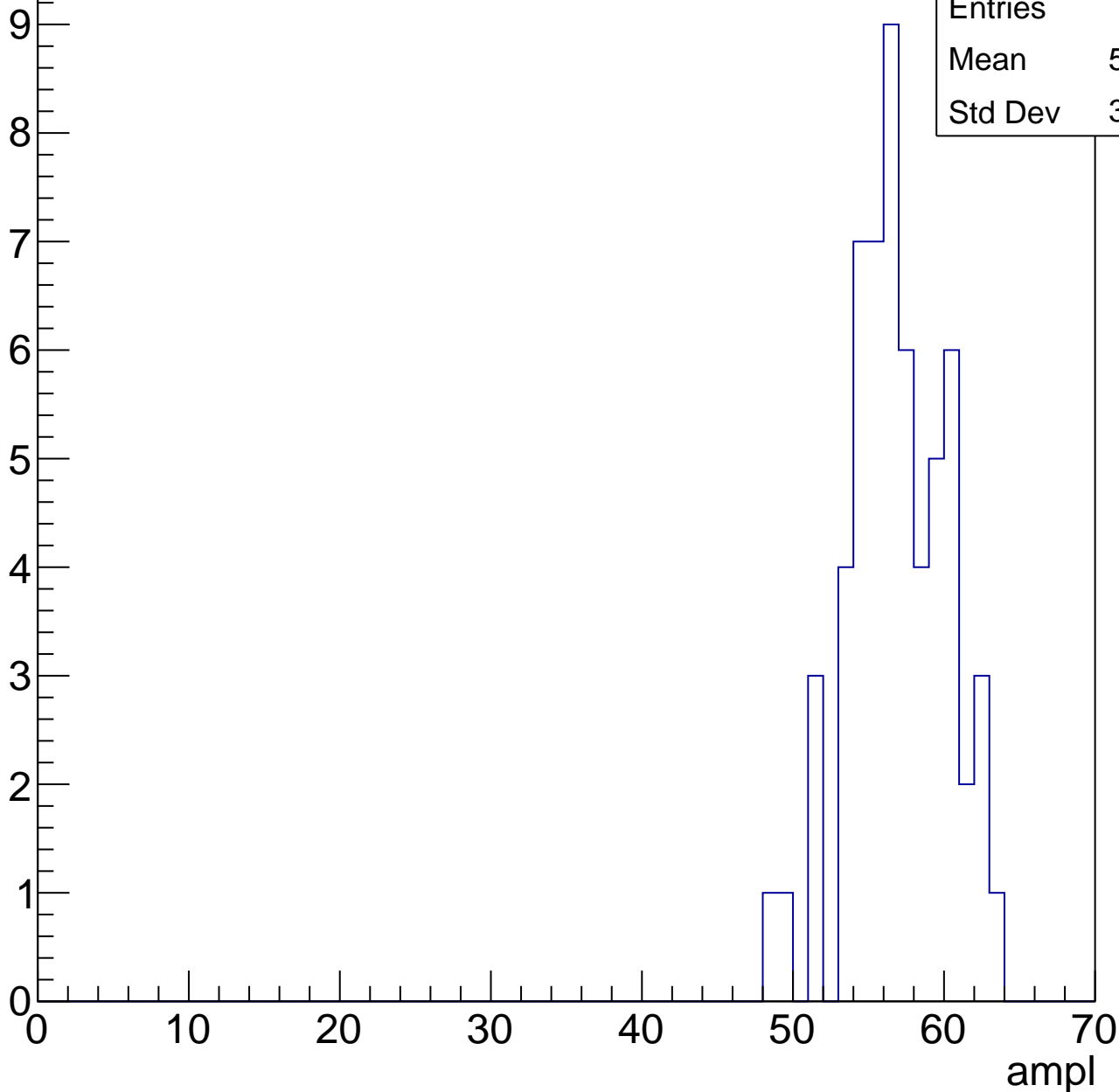


B1L103S, U11-ch45, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	56.42
Std Dev	3.238

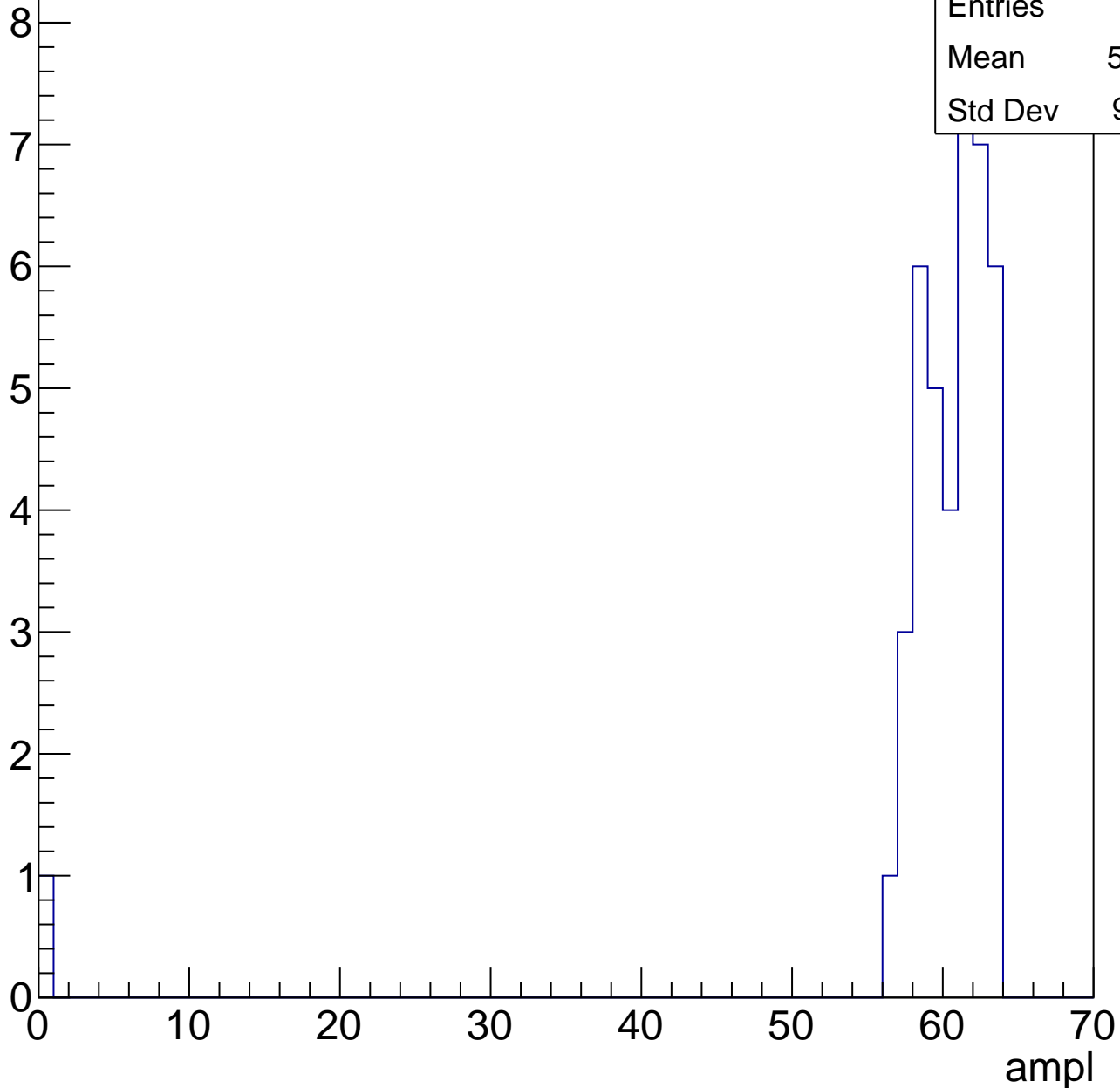


B1L103S, U11-ch45, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	41
Mean	58.78
Std Dev	9.501



B1L103S, U11-ch45, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch45, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch46, adc0

calib_packv5_041523_1651.root, FC#0, port C2

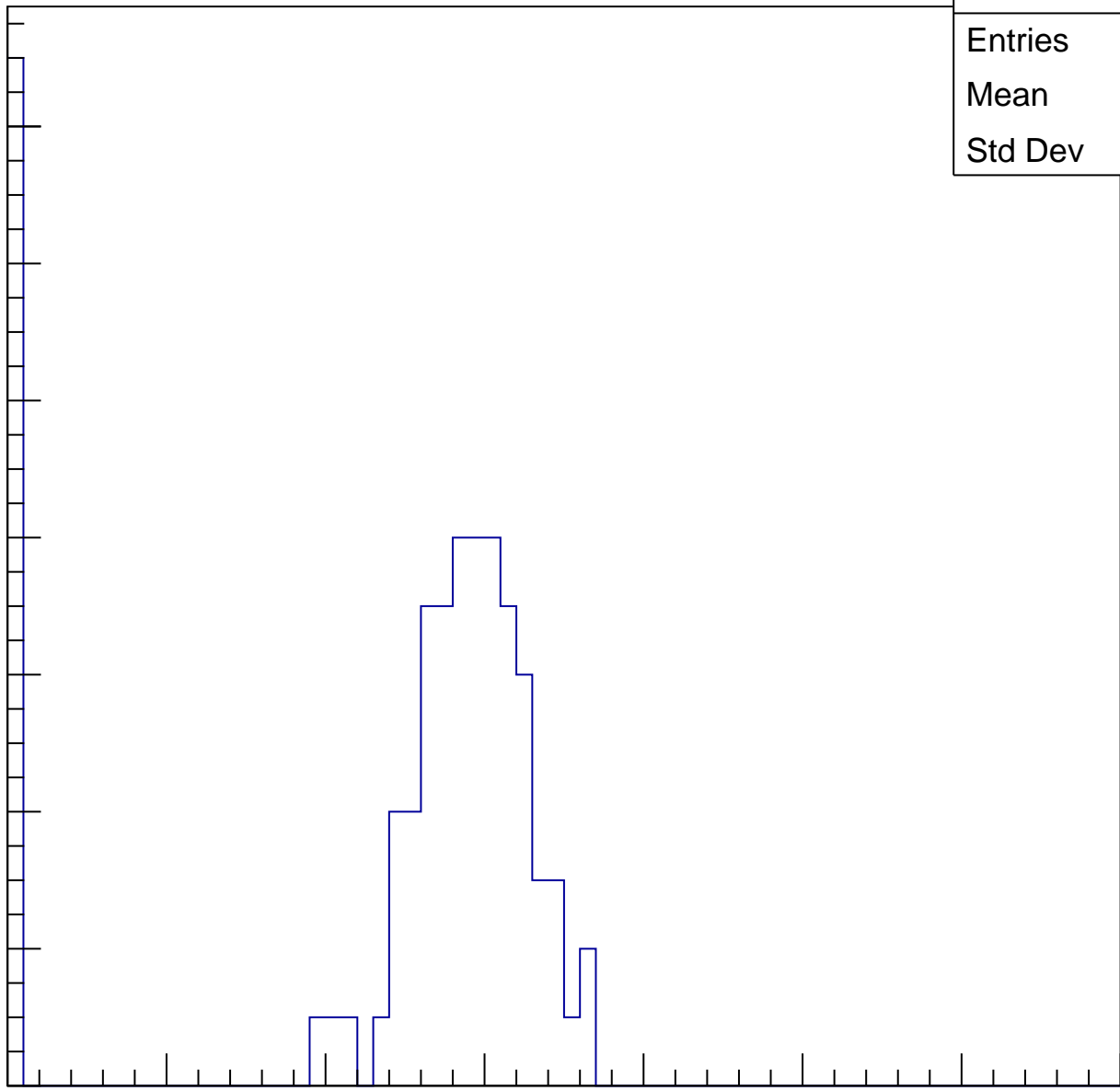
Entries	87
Mean	23.71
Std Dev	11.28

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

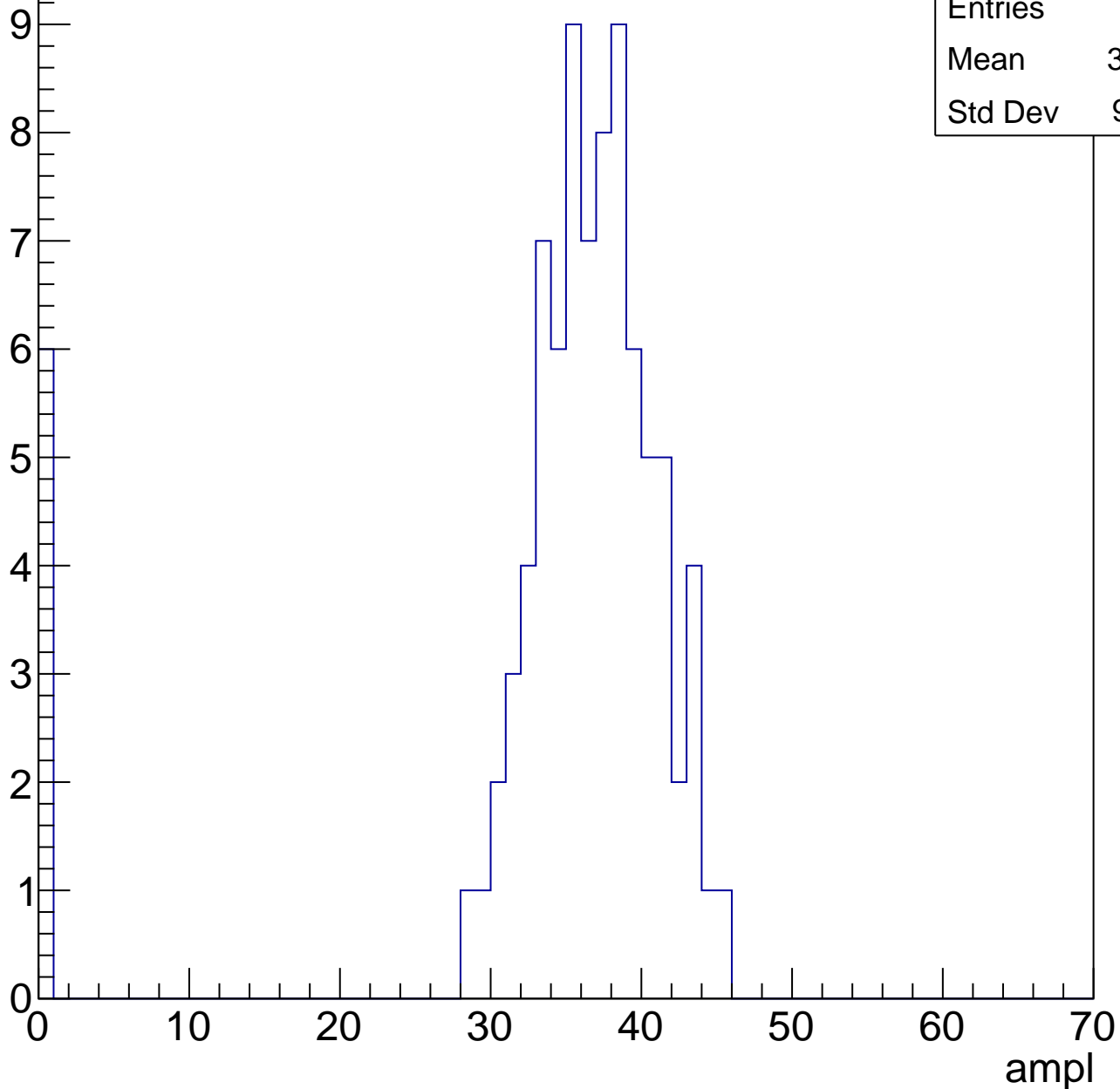


B1L103S, U11-ch46, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	87
Mean	34.05
Std Dev	9.931

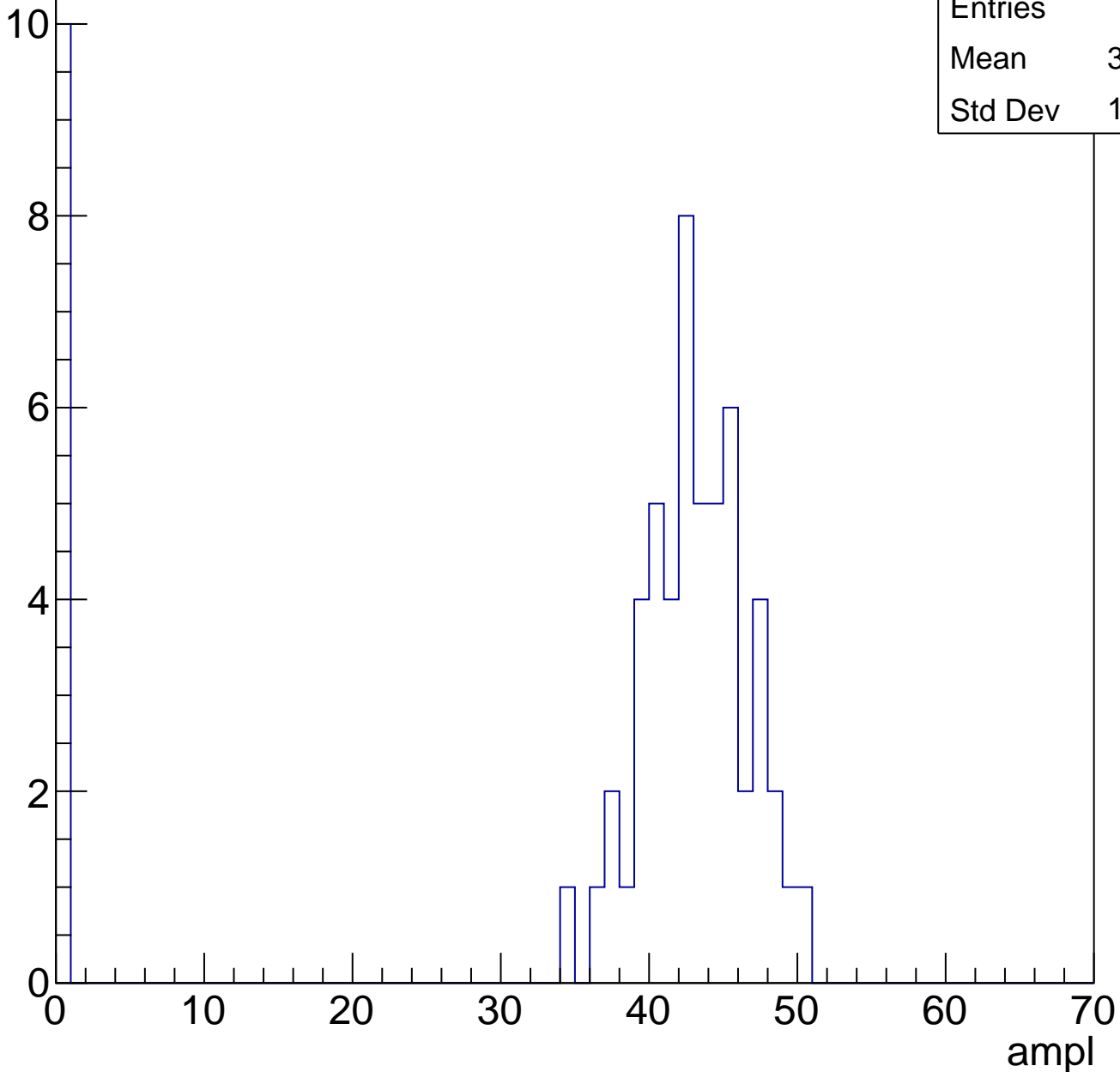


B1L103S, U11-ch46, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	62
Mean	35.77
Std Dev	15.99

Entry

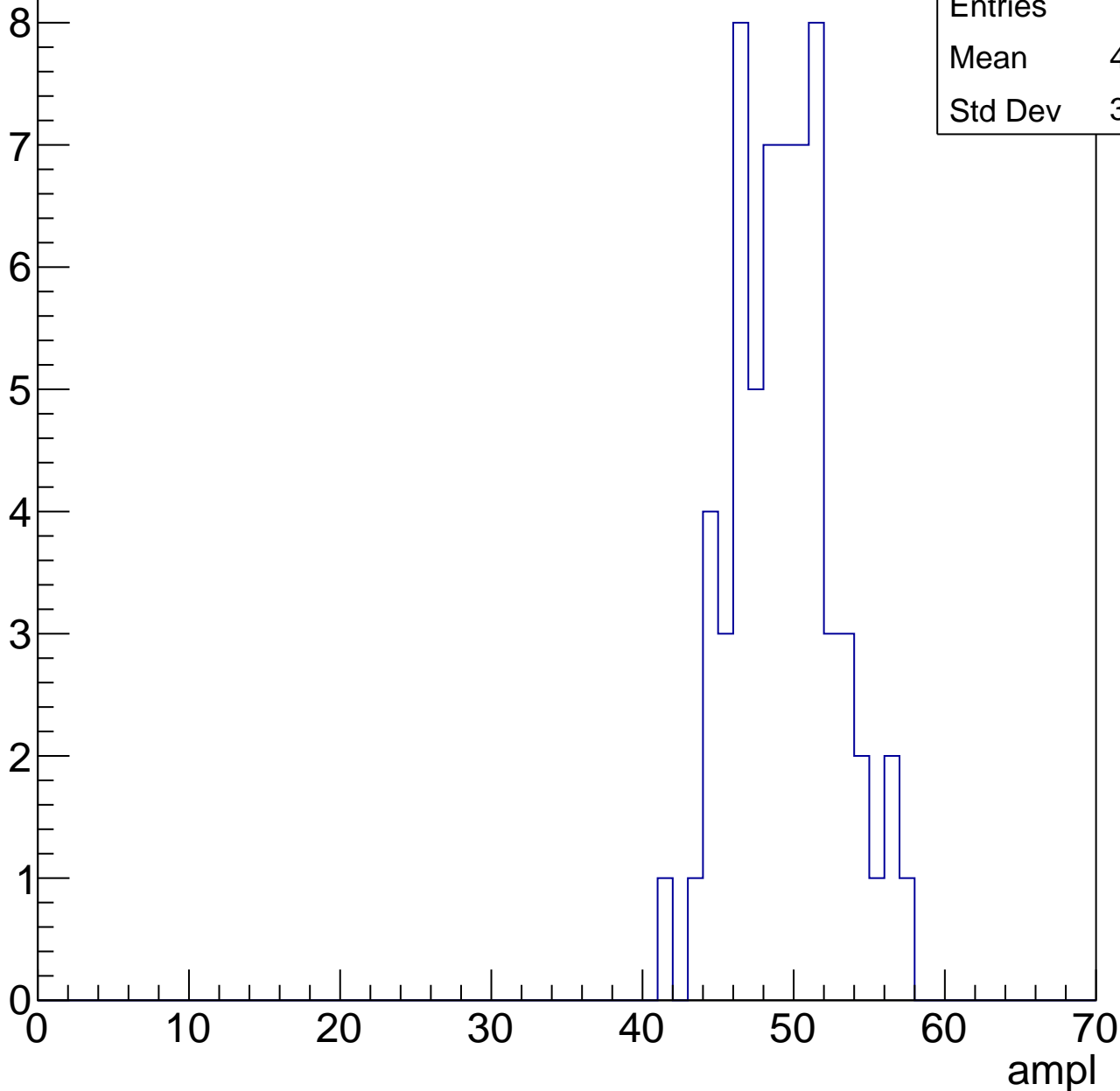


B1L103S, U11-ch46, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	48.92
Std Dev	3.354

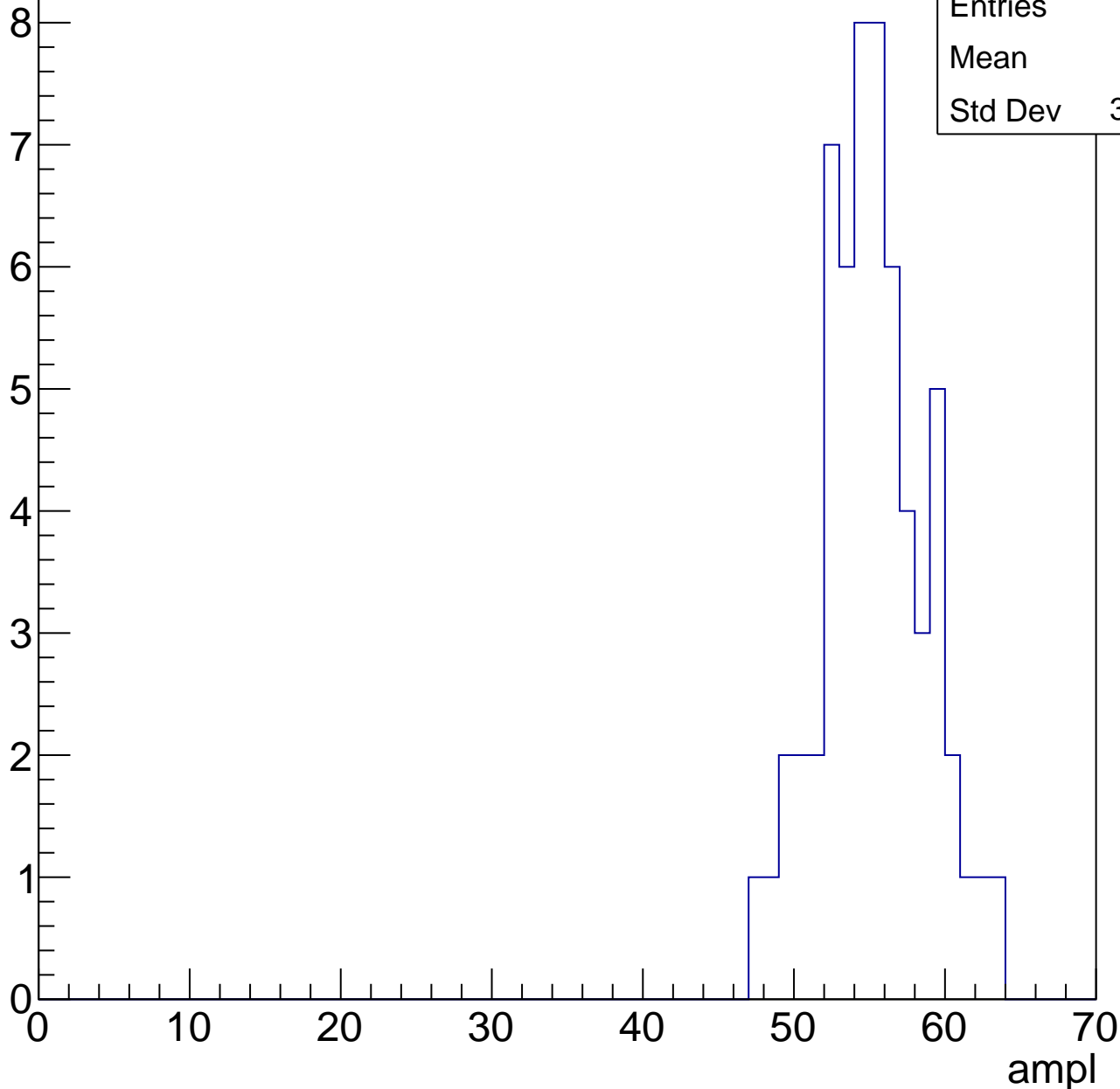


B1L103S, U11-ch46, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	54.8
Std Dev	3.385

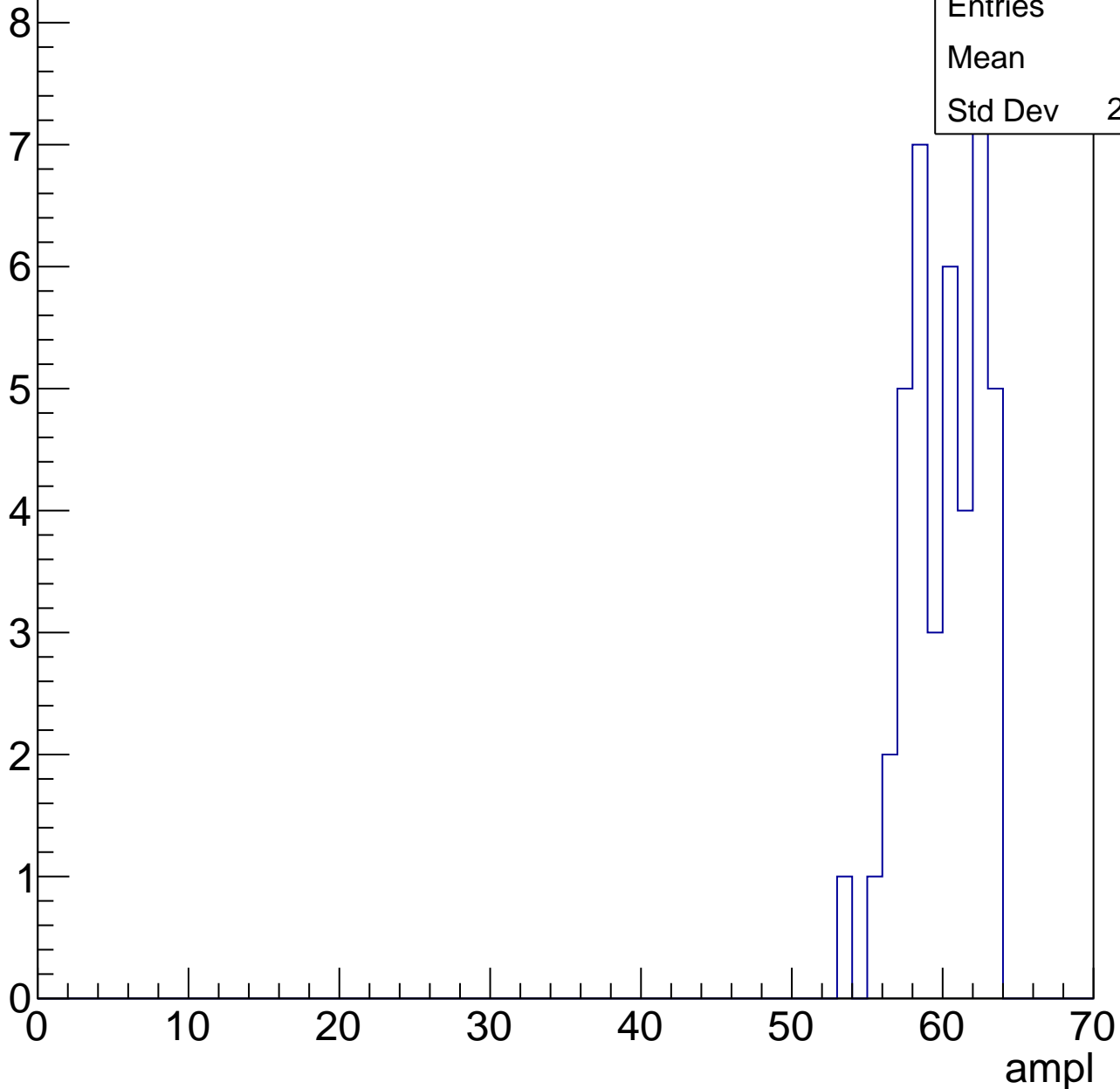


B1L103S, U11-ch46, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	42
Mean	59.6
Std Dev	2.469

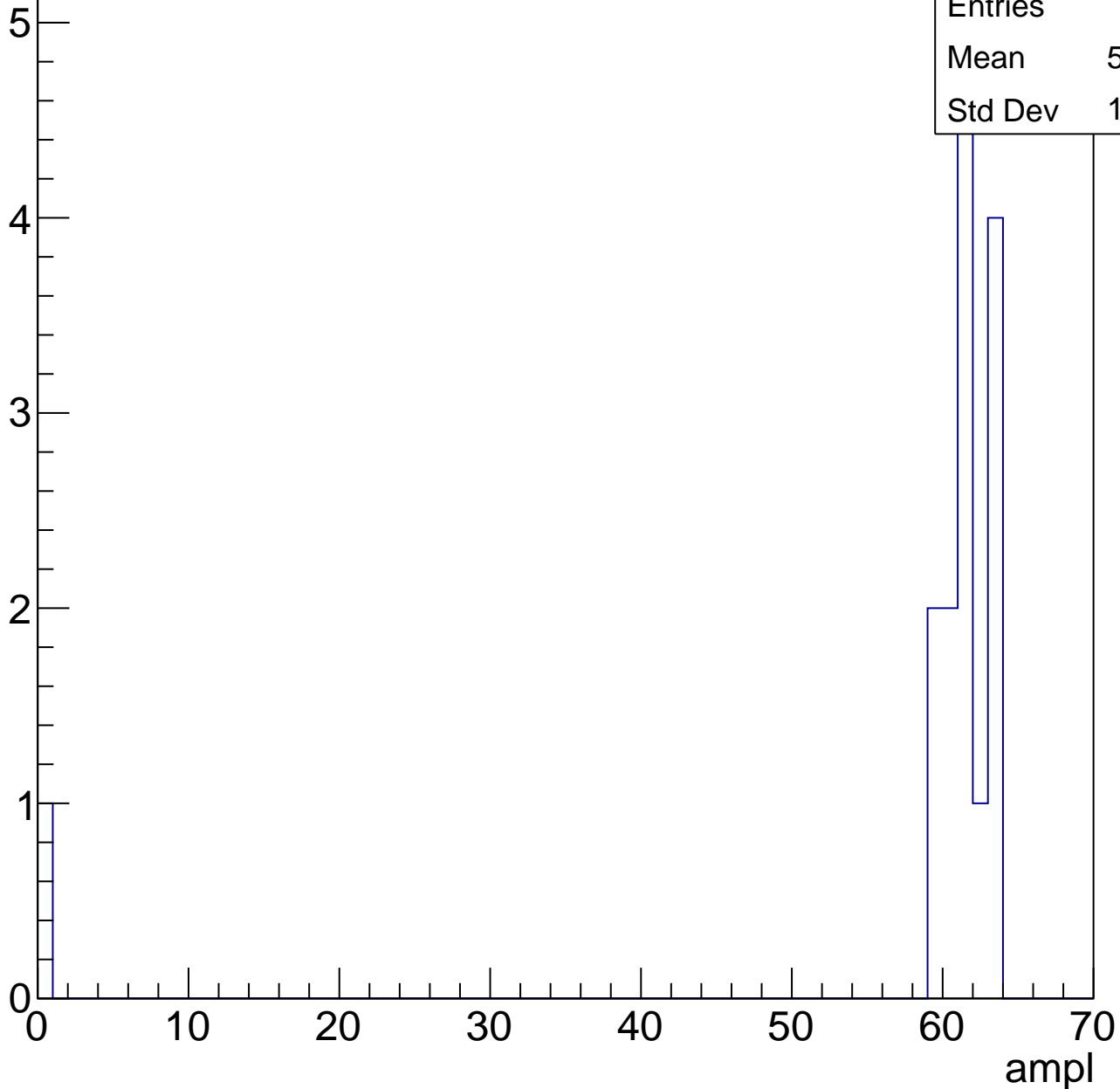


B1L103S, U11-ch46, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	15
Mean	57.13
Std Dev	15.33



B1L103S, U11-ch46, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

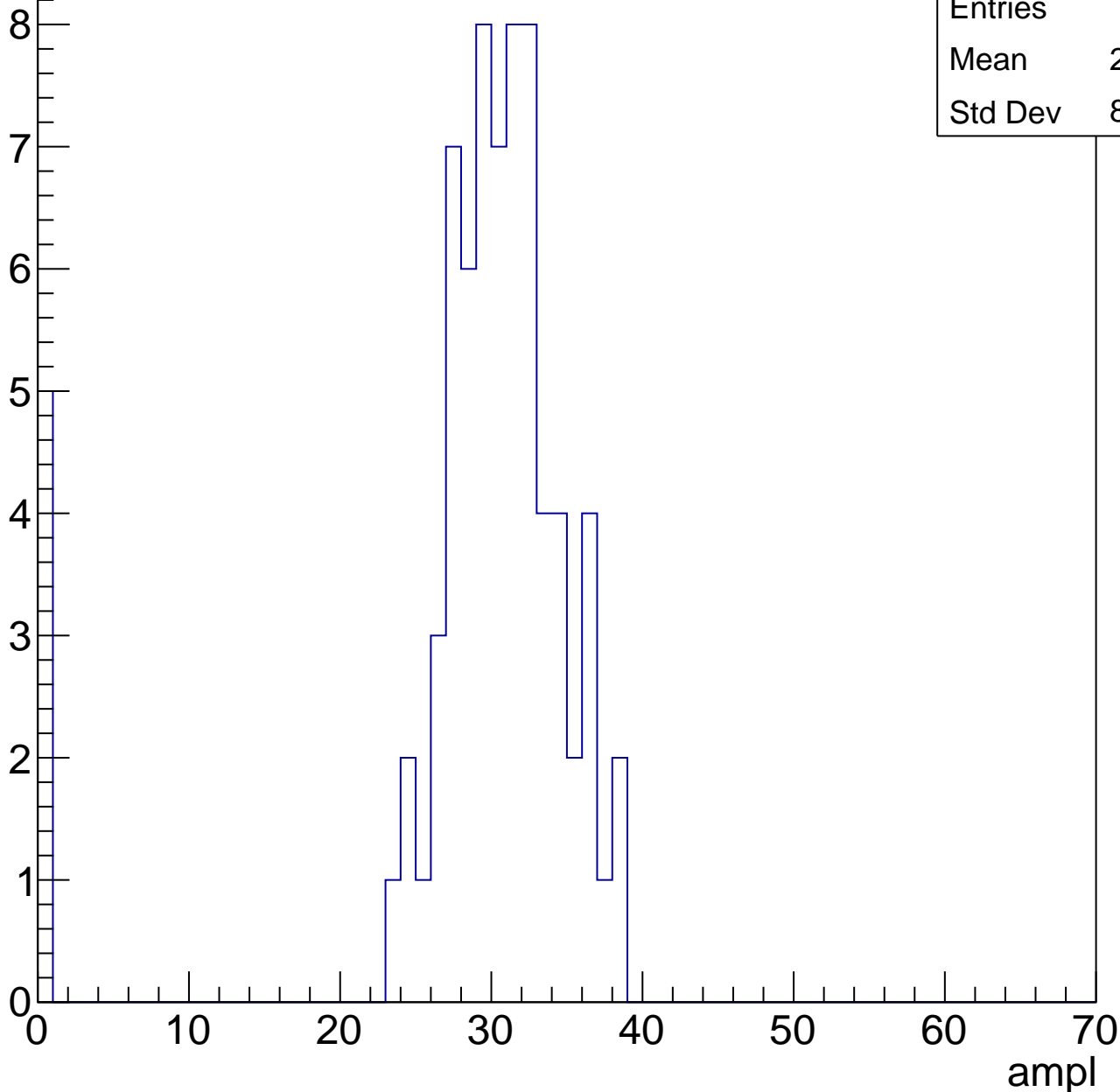


B1L103S, U11-ch47, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	28.38
Std Dev	8.366

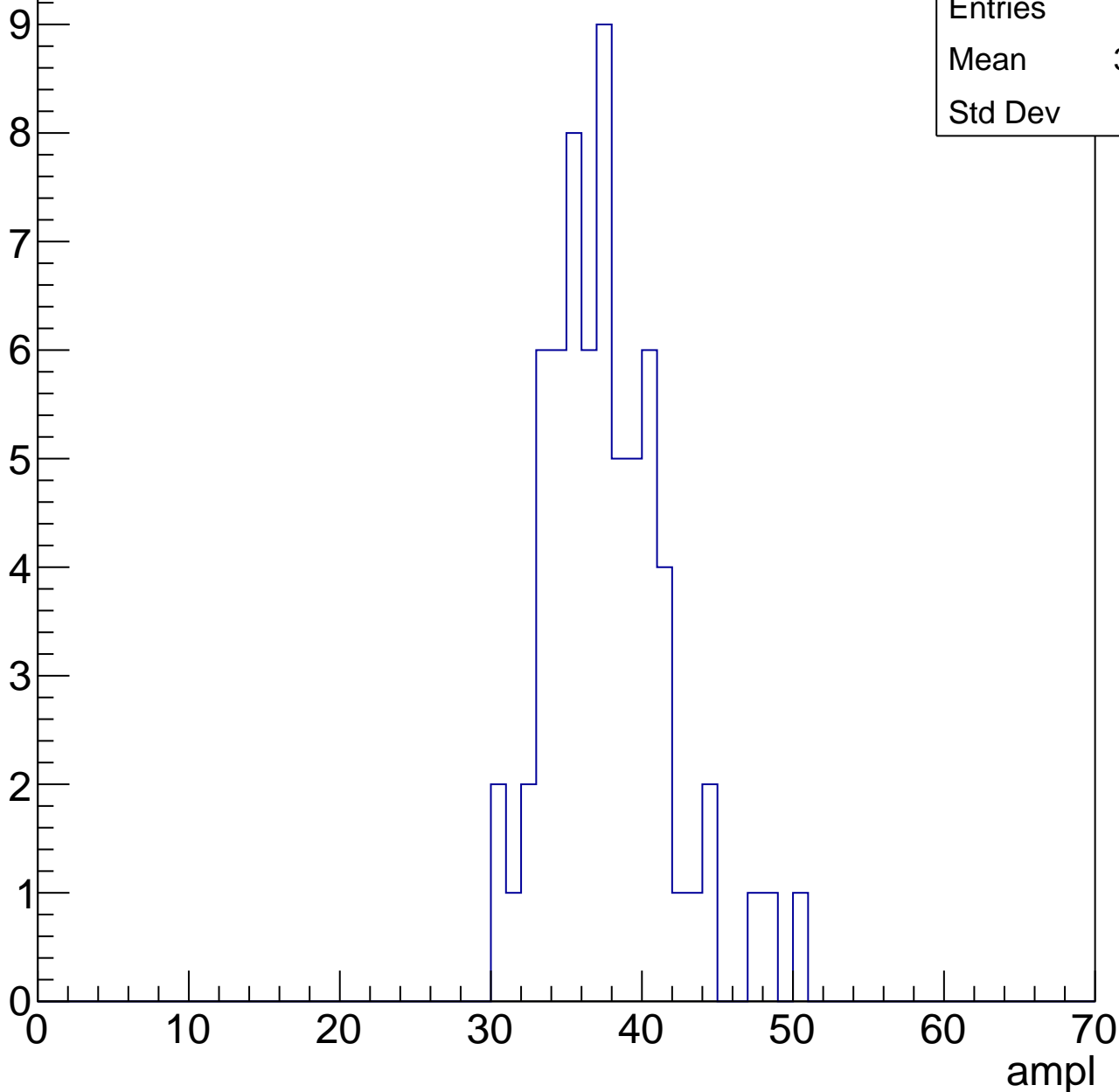


B1L103S, U11-ch47, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

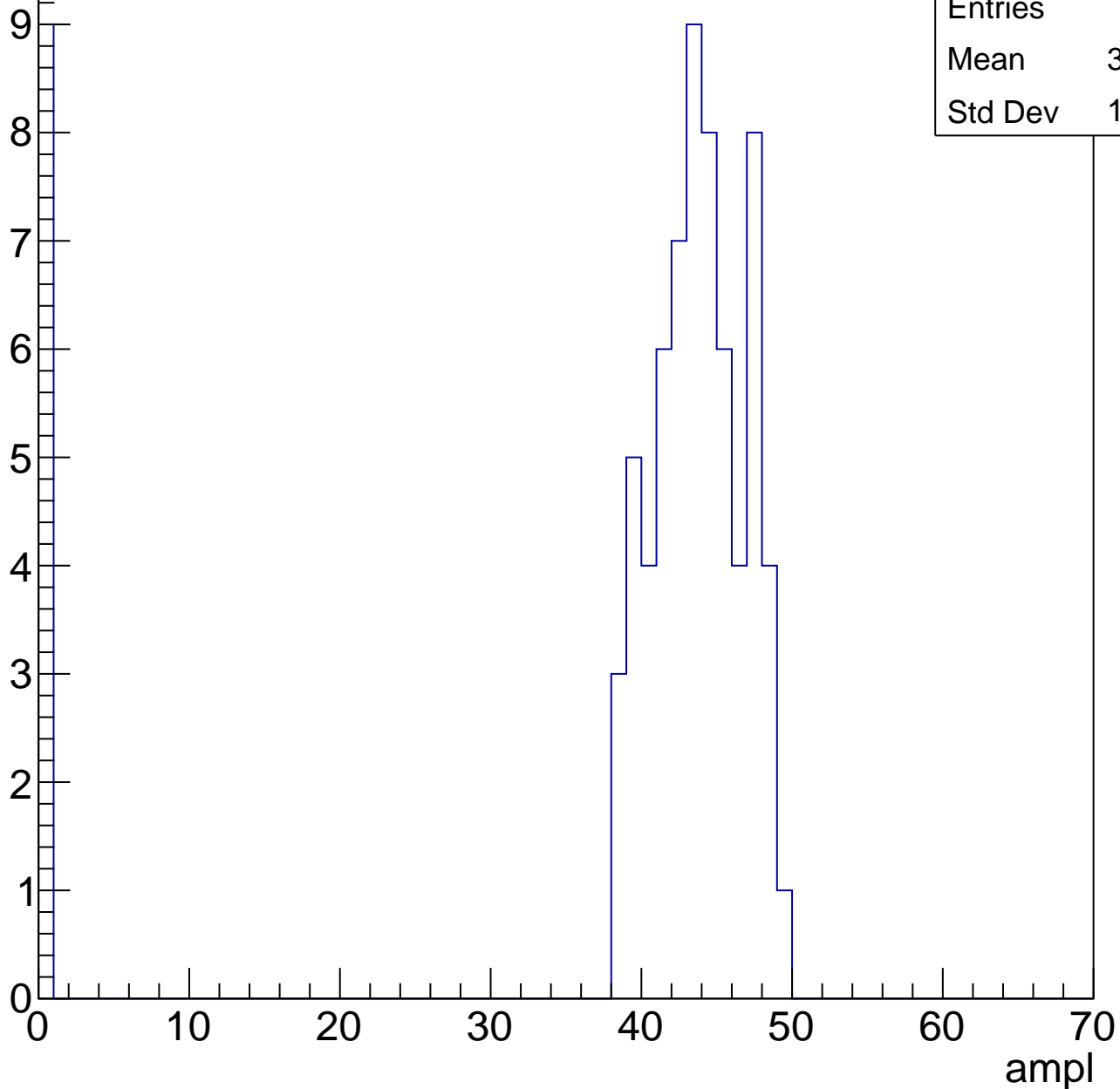
Entries	67
Mean	37.21
Std Dev	3.98



B1L103S, U11-ch47, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

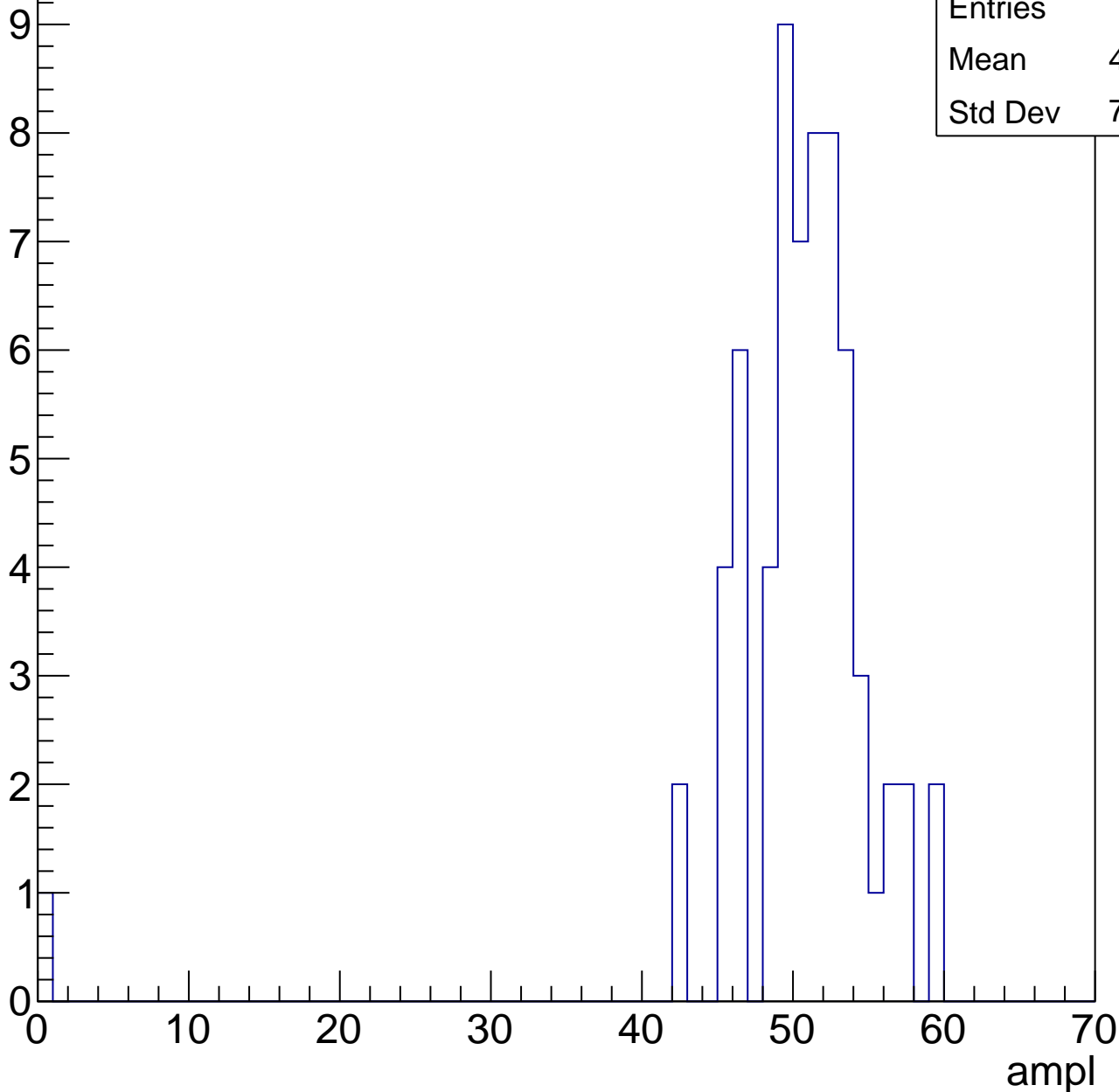


B1L103S, U11-ch47, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	49.63
Std Dev	7.167

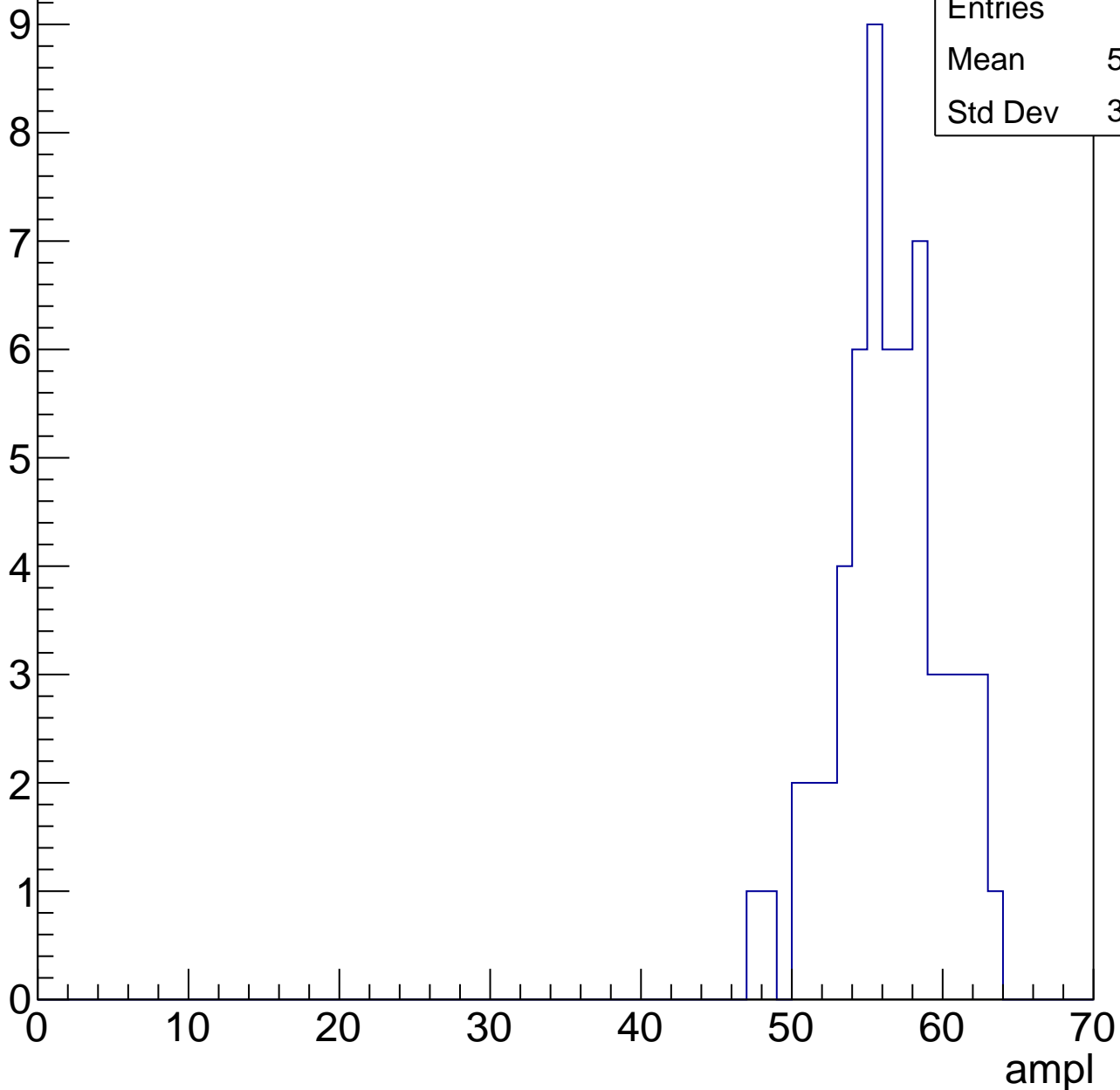


B1L103S, U11-ch47, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	56.02
Std Dev	3.467

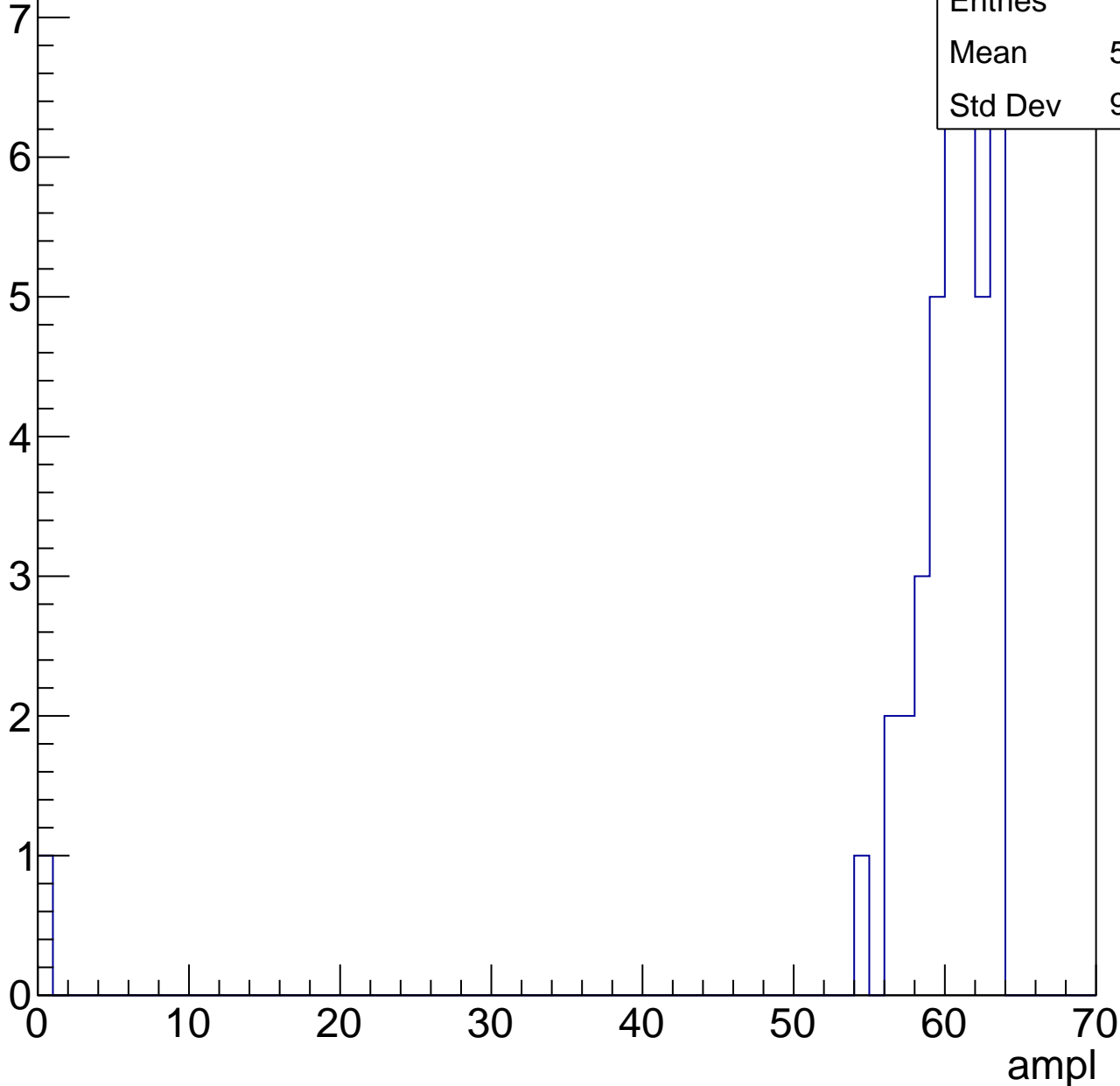


B1L103S, U11-ch47, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	58.67
Std Dev	9.647



B1L103S, U11-ch47, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch47, adc7

calib_packv5_041523_1651.root, FC#0, port C2

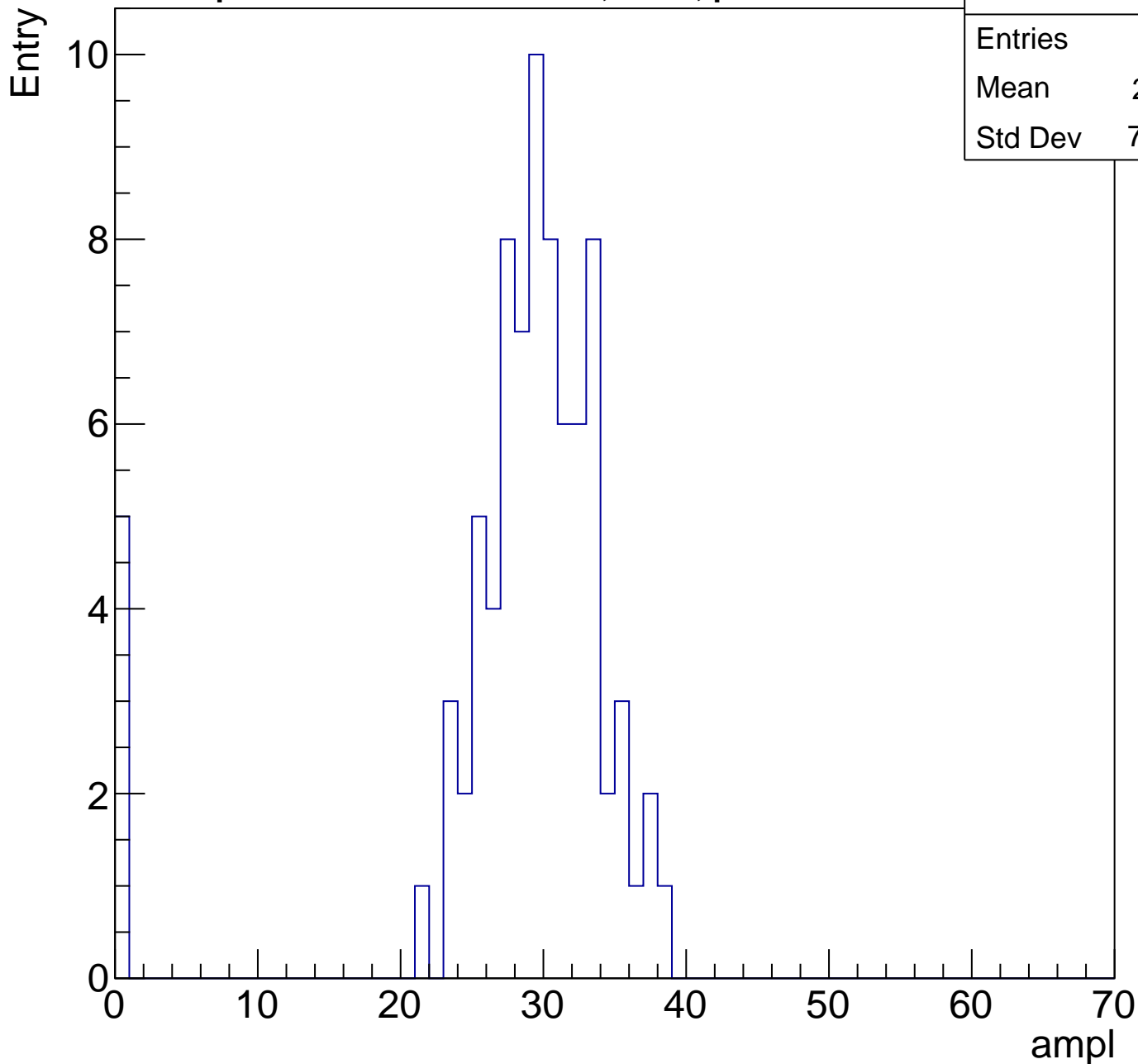
Entry



B1L103S, U11-ch48, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	27.71
Std Dev	7.867

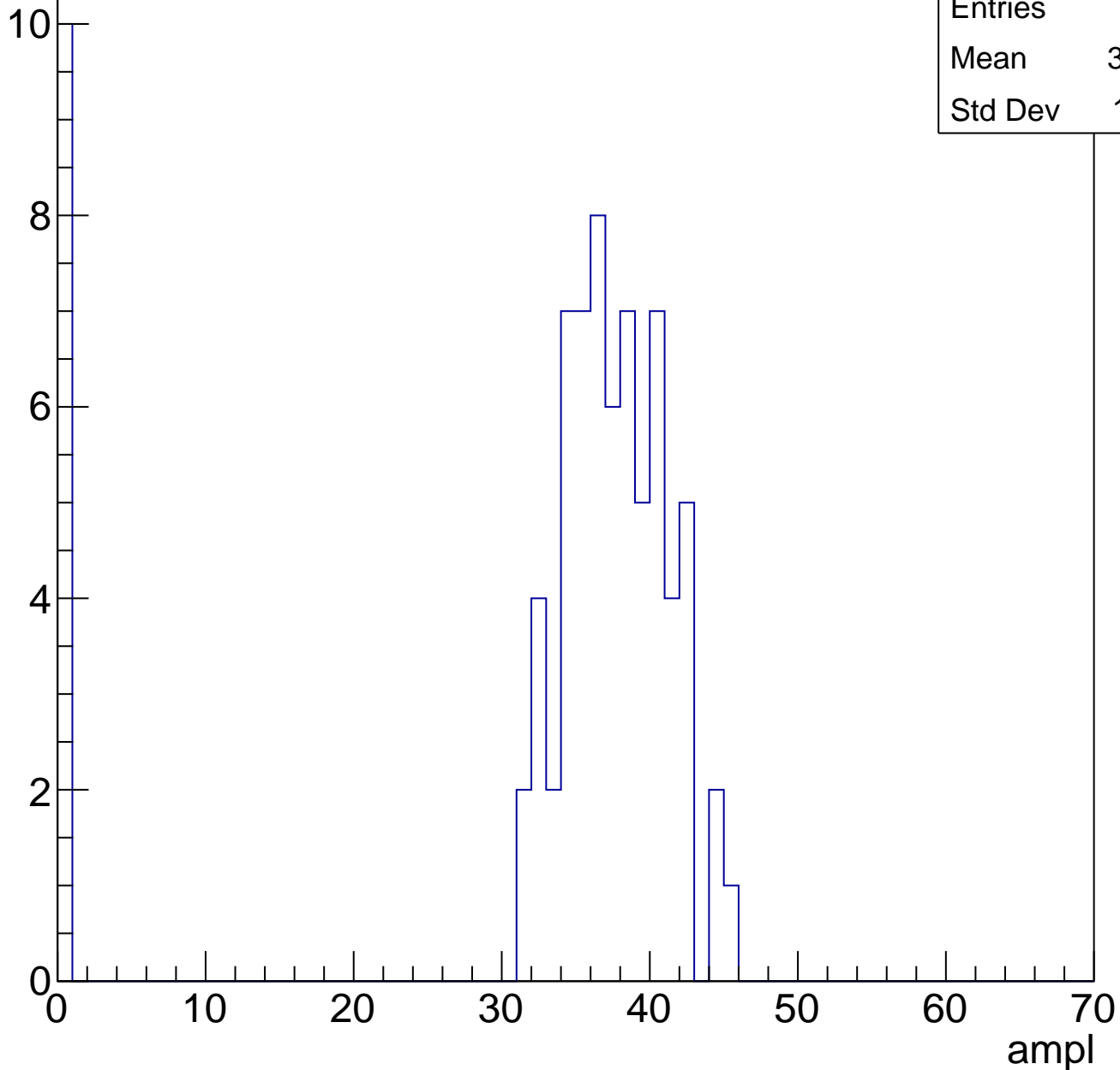


B1L103S, U11-ch48, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	77
Mean	32.43
Std Dev	12.91

Entry

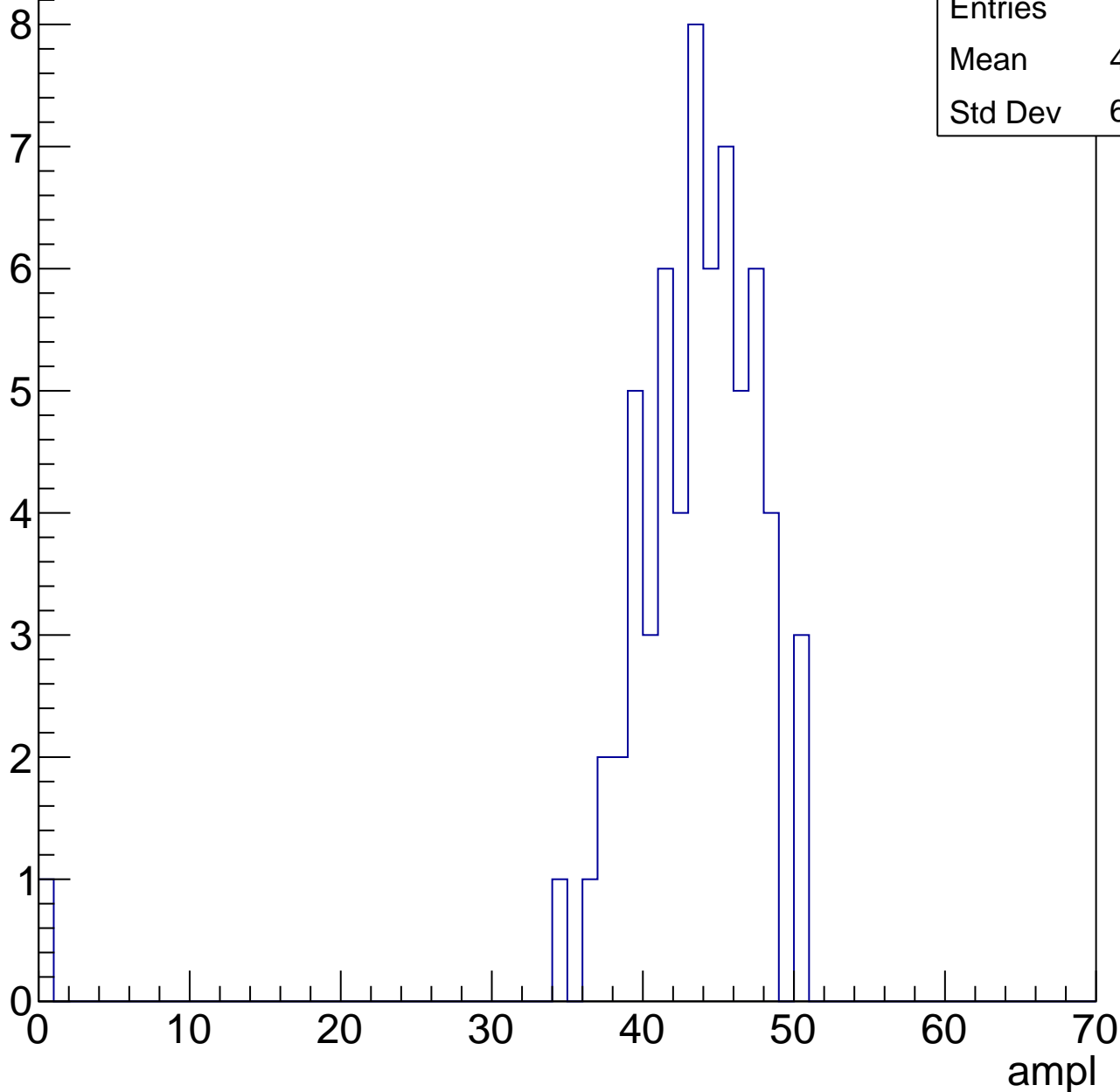


B1L103S, U11-ch48, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

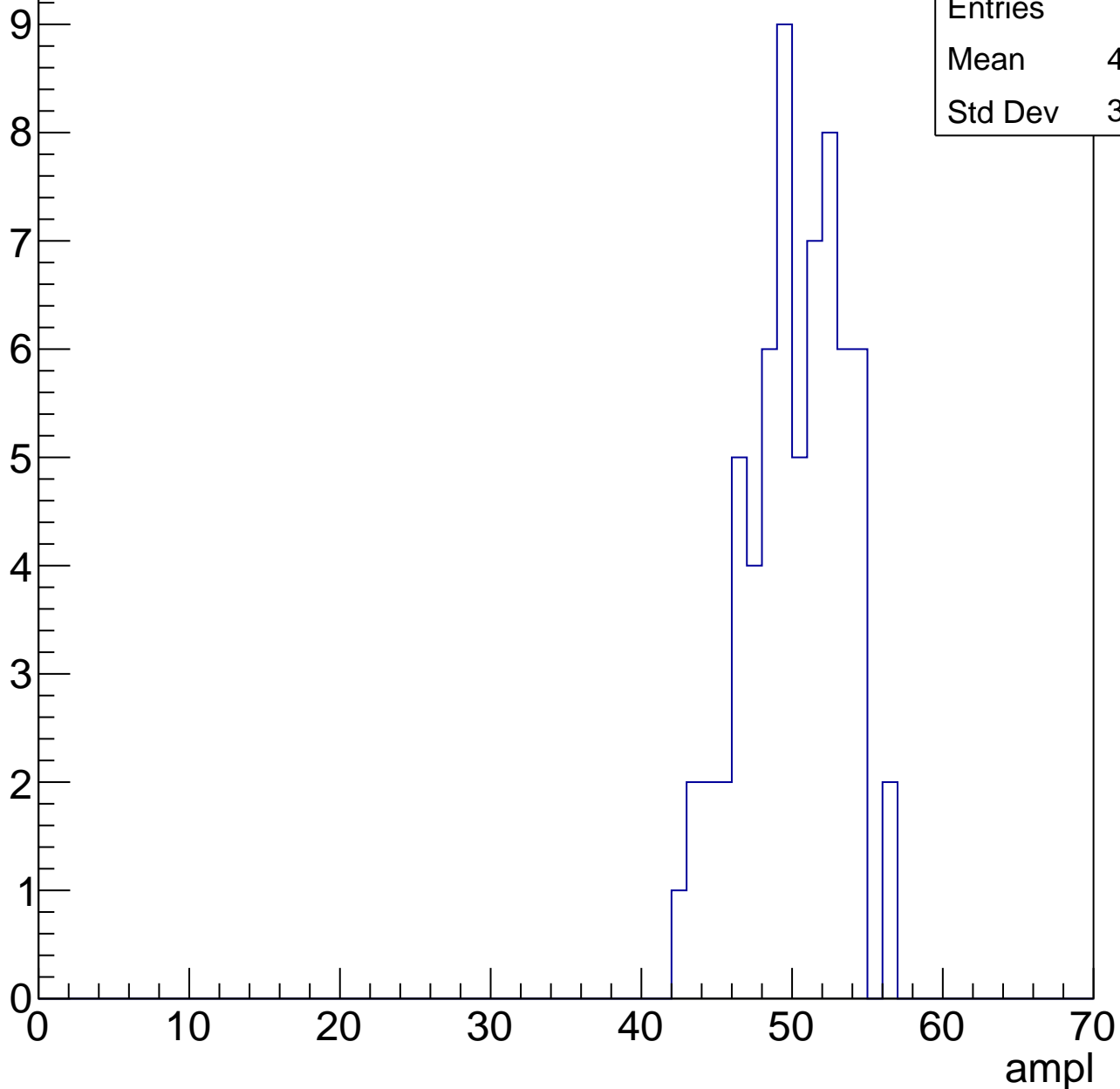
Entries	64
Mean	42.59
Std Dev	6.432



B1L103S, U11-ch48, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

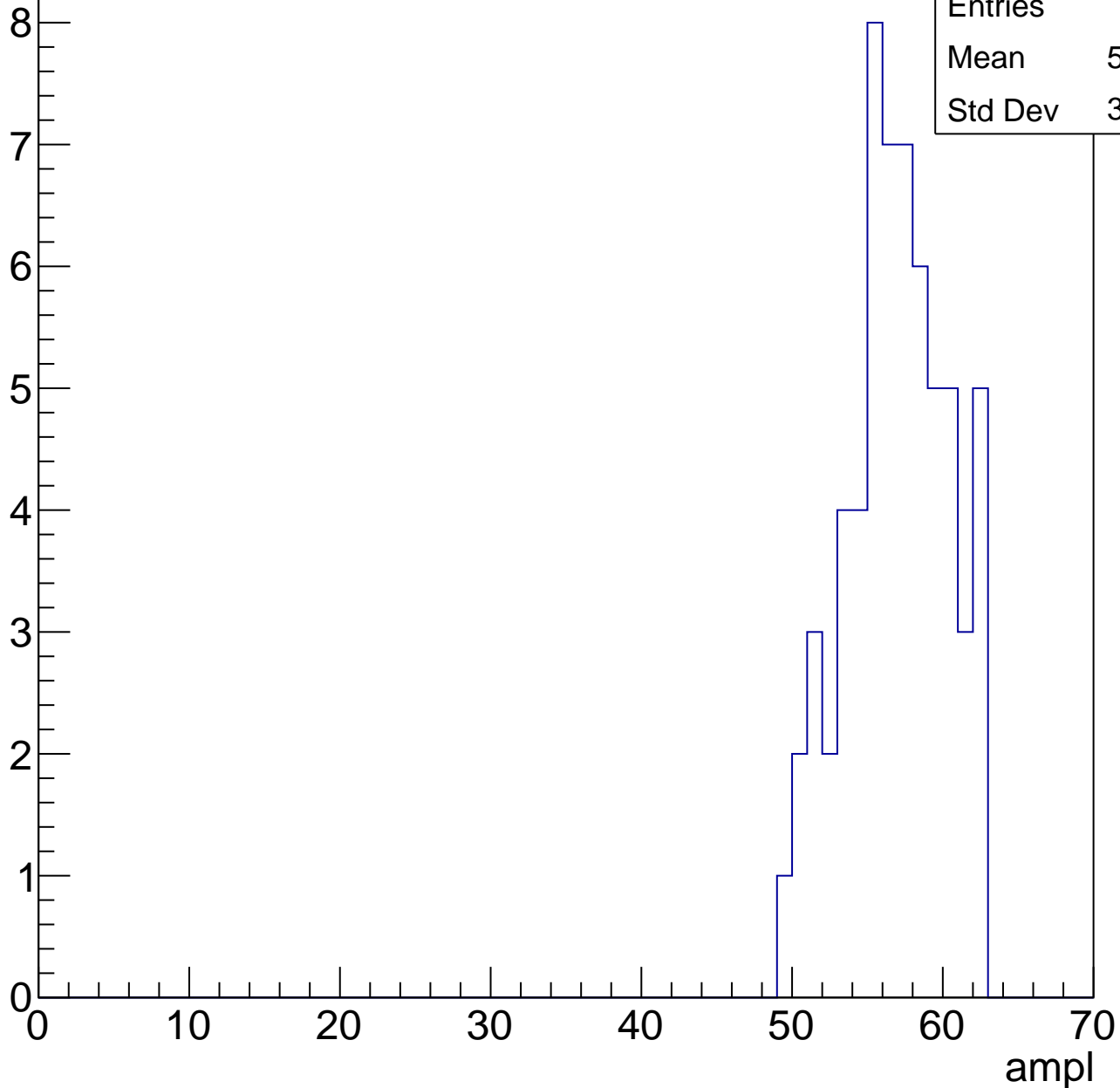


B1L103S, U11-ch48, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	56.47
Std Dev	3.325

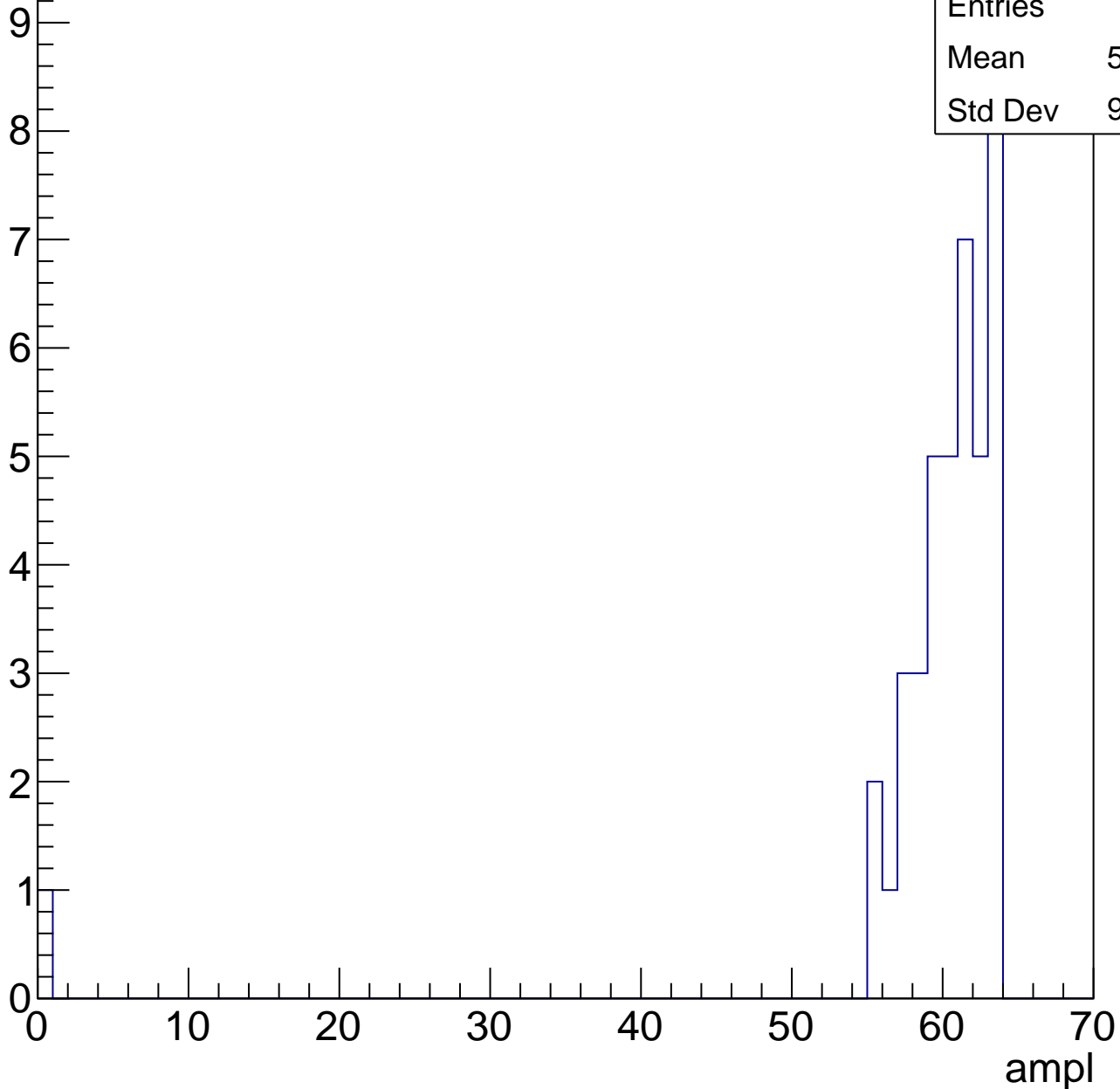


B1L103S, U11-ch48, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	41
Mean	58.78
Std Dev	9.573



B1L103S, U11-ch48, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

1
0.8
0.6
0.4
0.2
0

Entries	2
Mean	60.5
Std Dev	2.5

ampl

B1L103S, U11-ch48, adc7

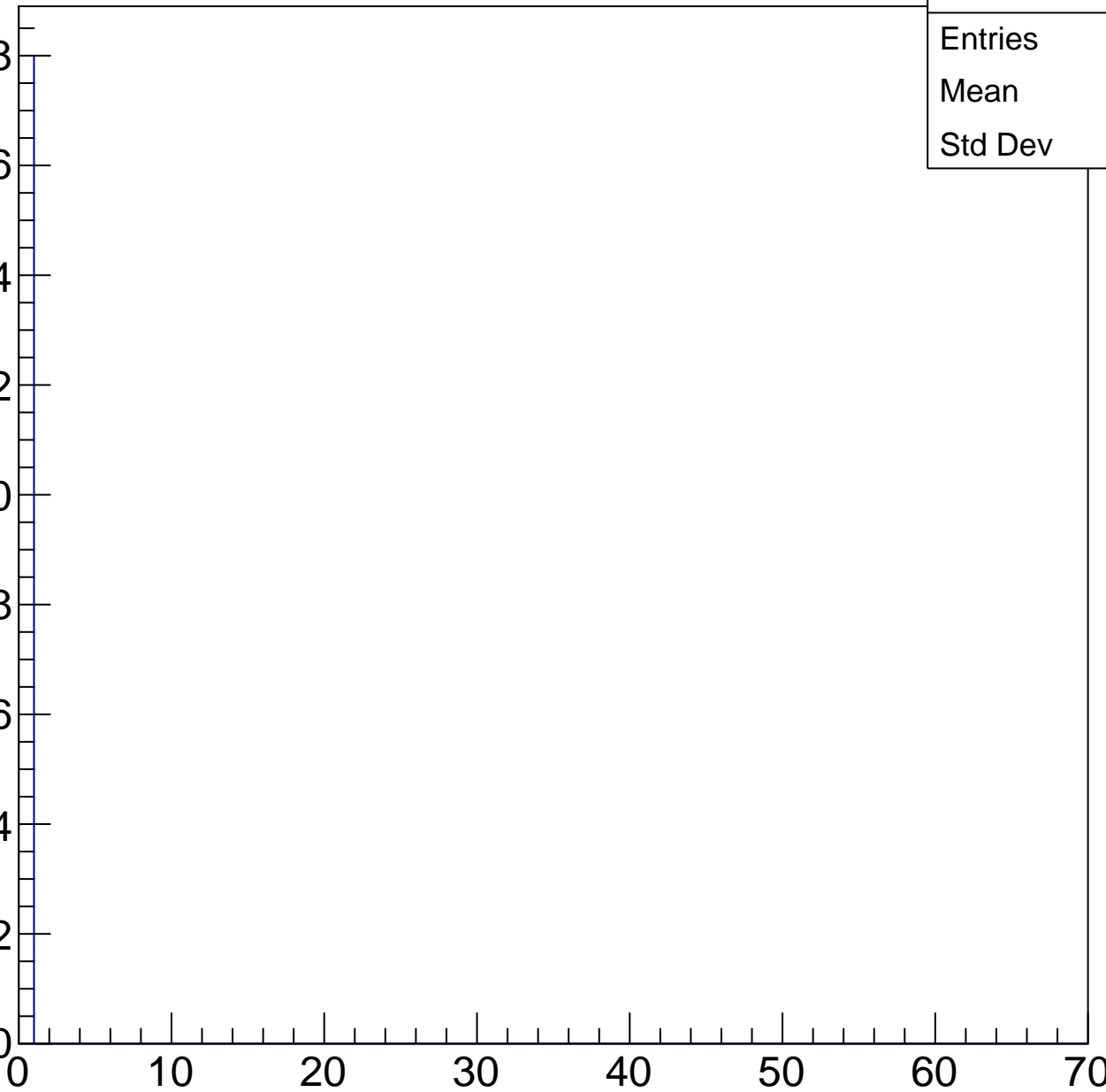
calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	18
Mean	0
Std Dev	0

ampl

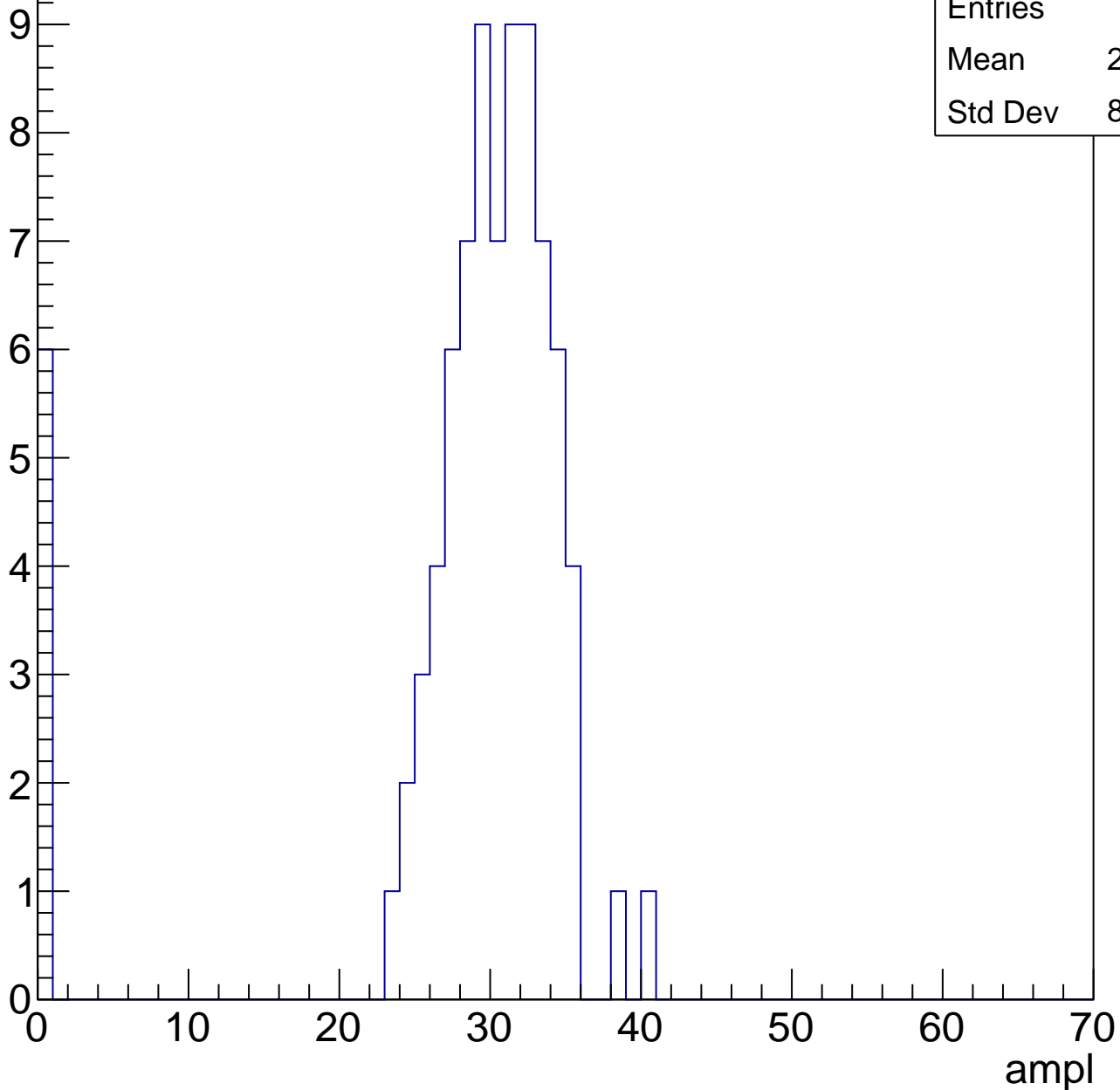


B1L103S, U11-ch49, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	82
Mean	28.04
Std Dev	8.484



B1L103S, U11-ch49, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	71
Mean	31.41
Std Dev	13.69

Entry

10

8

6

4

2

0

0

10

20

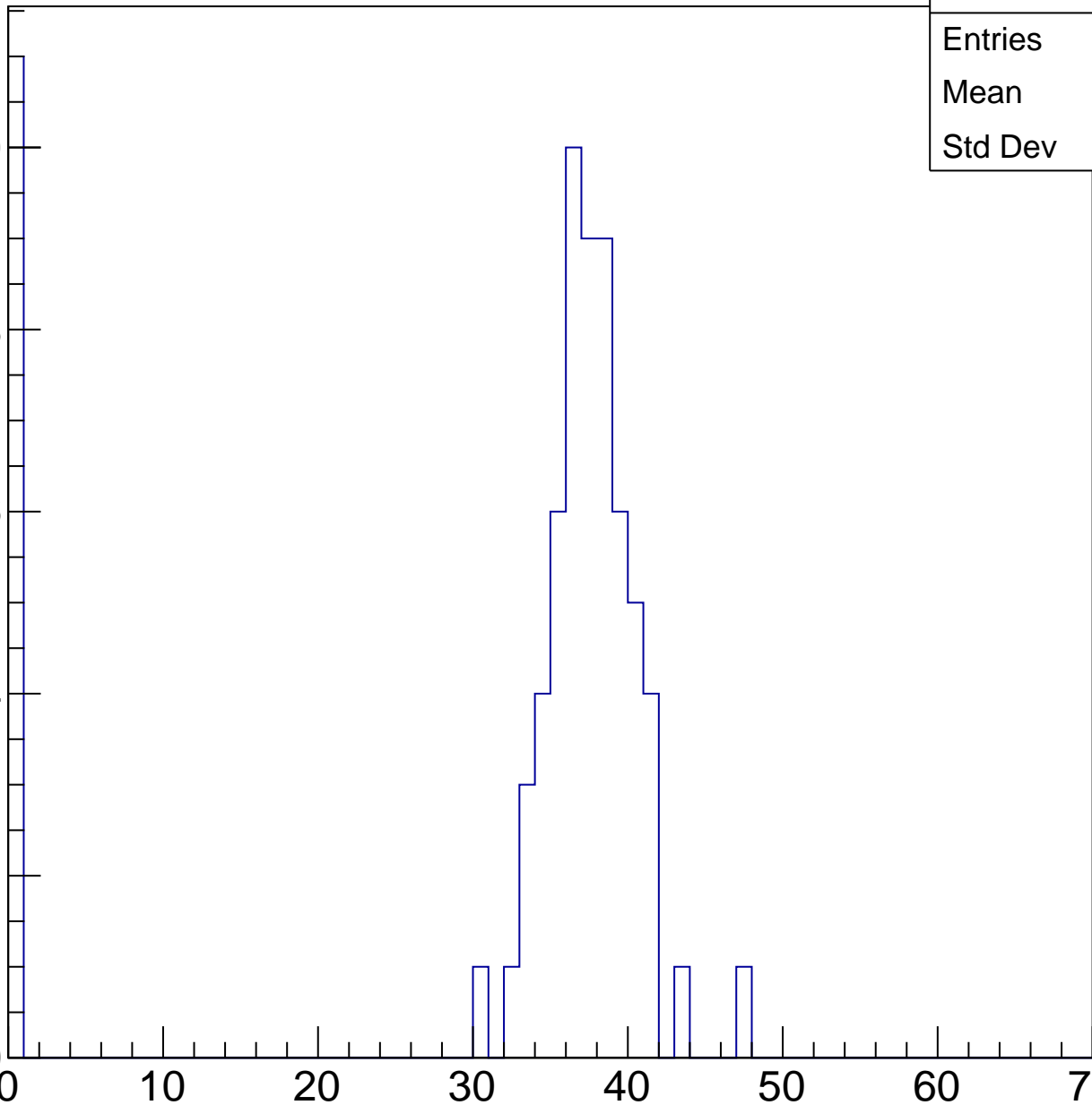
30

40

50

60

ampl

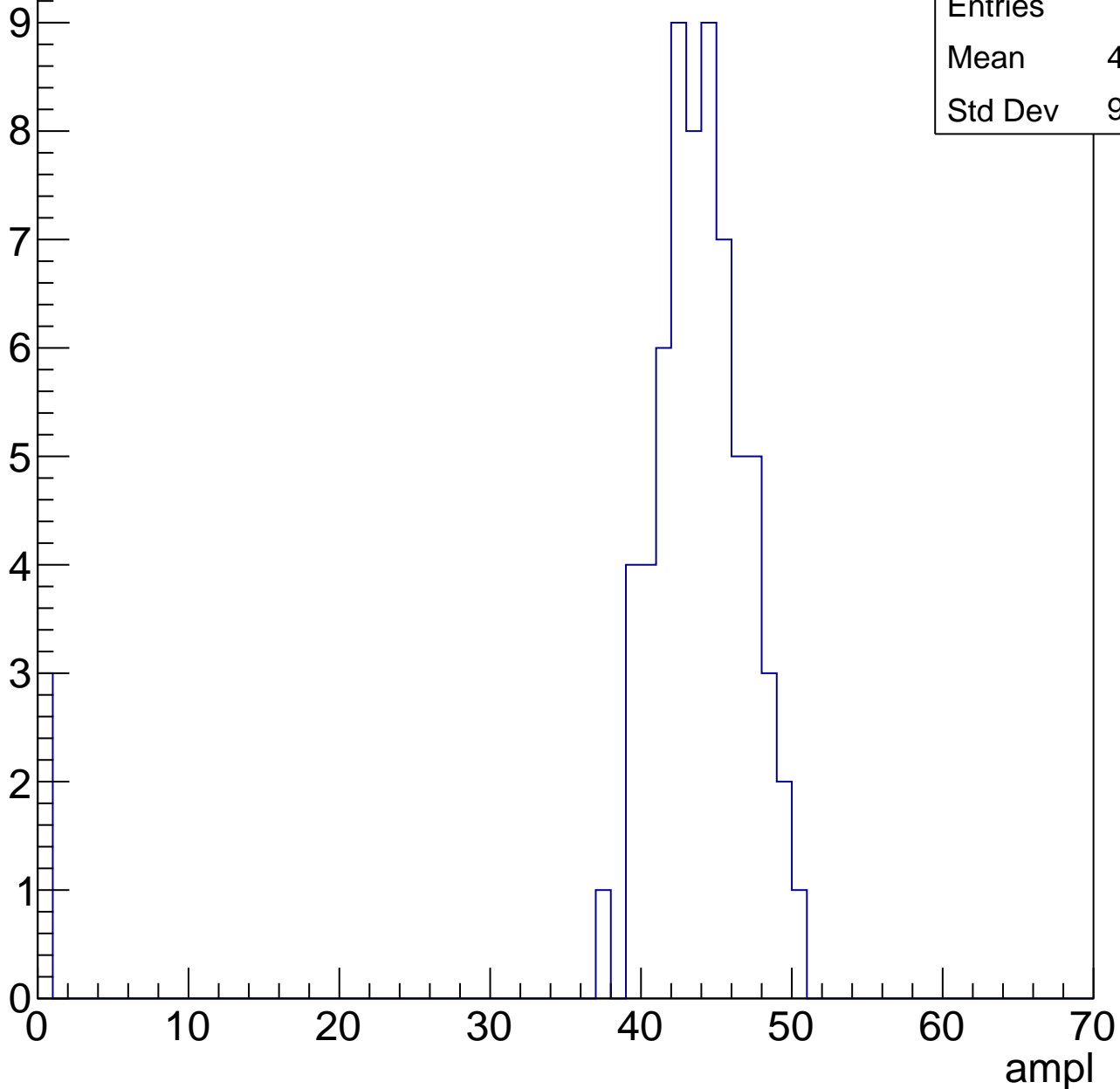


B1L103S, U11-ch49, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	41.63
Std Dev	9.422

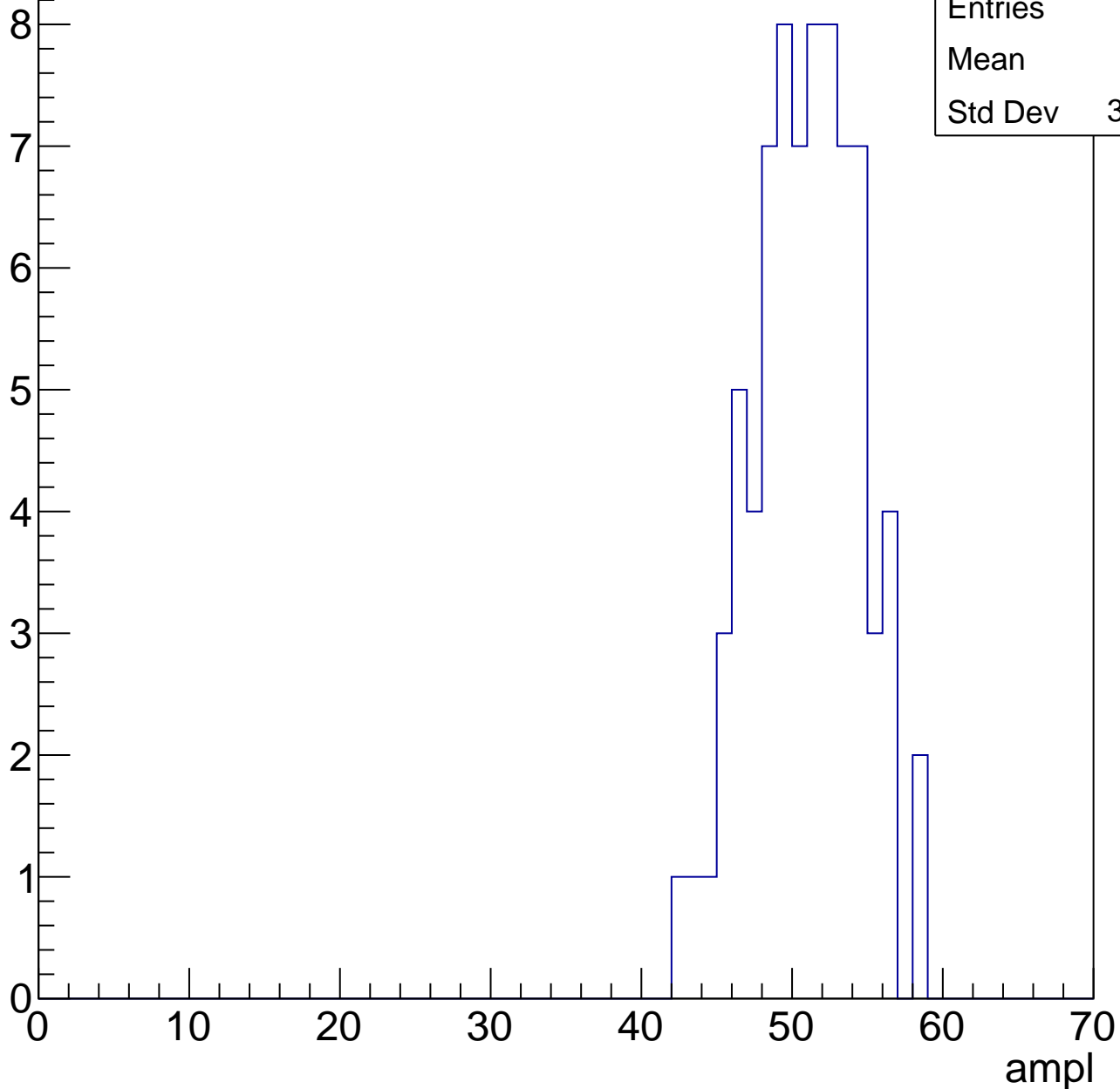


B1L103S, U11-ch49, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	50.5
Std Dev	3.477

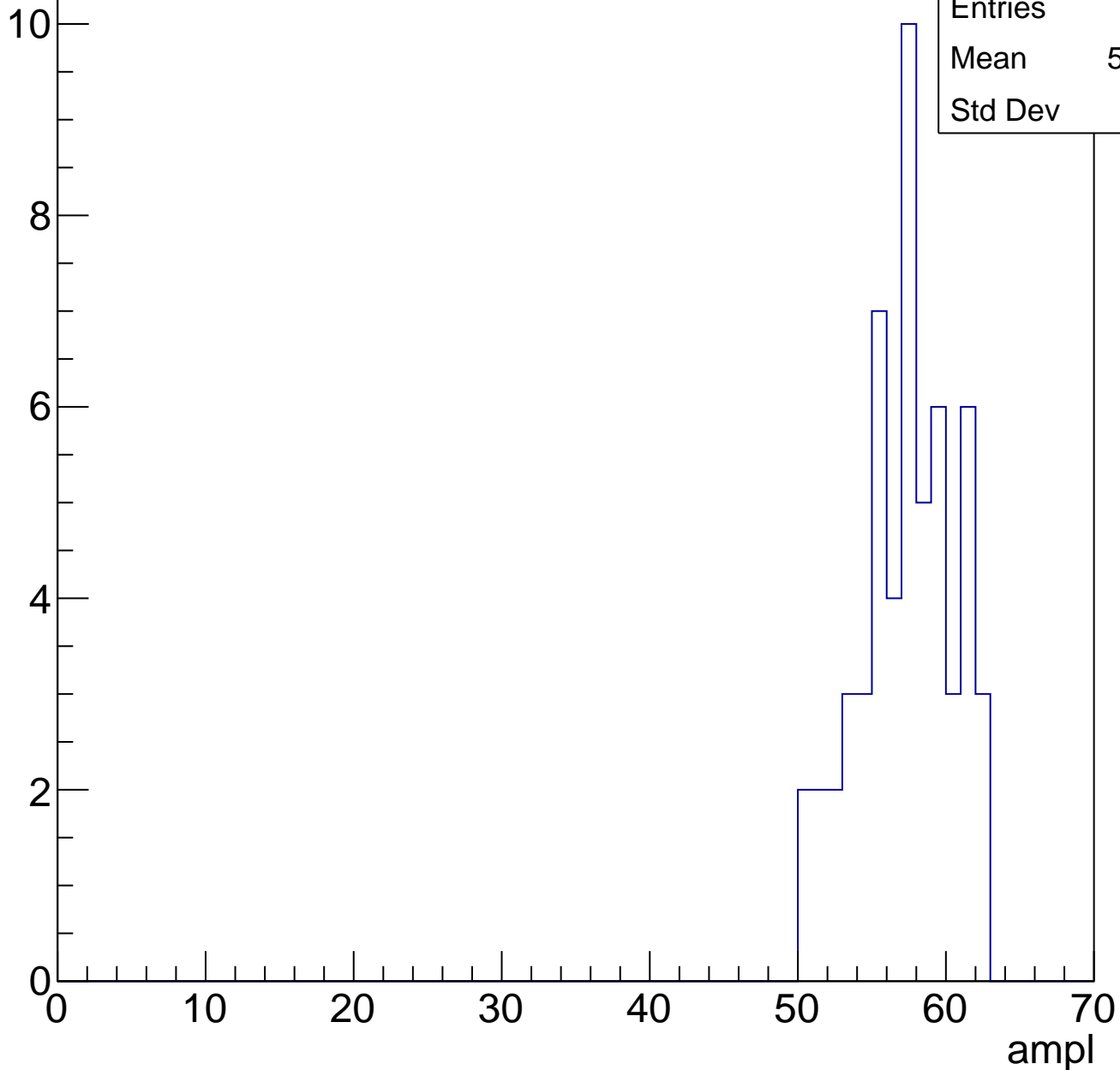


B1L103S, U11-ch49, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	56
Mean	56.82
Std Dev	3.14

Entry

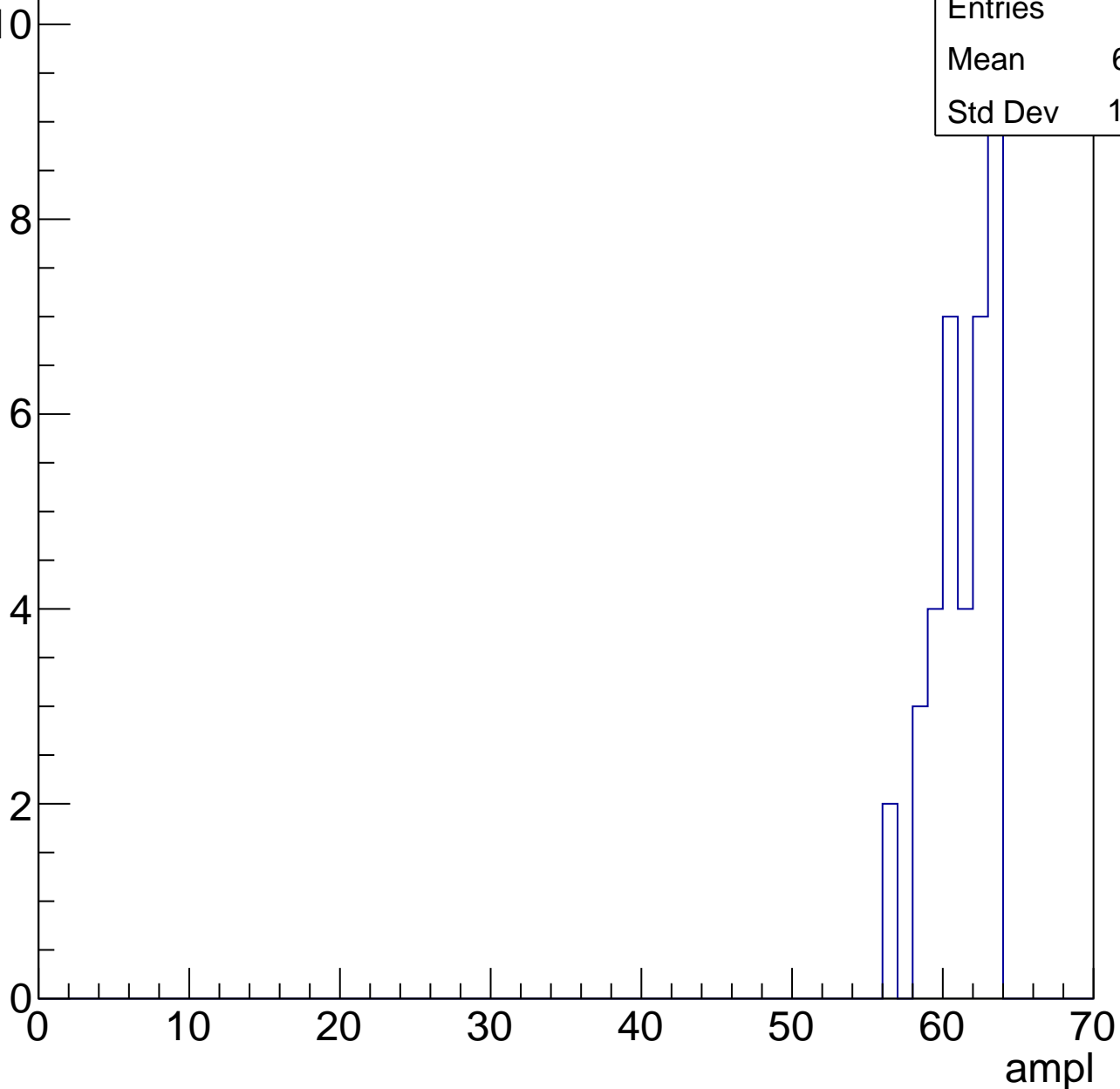


B1L103S, U11-ch49, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	37
Mean	60.81
Std Dev	1.984



B1L103S, U11-ch49, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch49, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

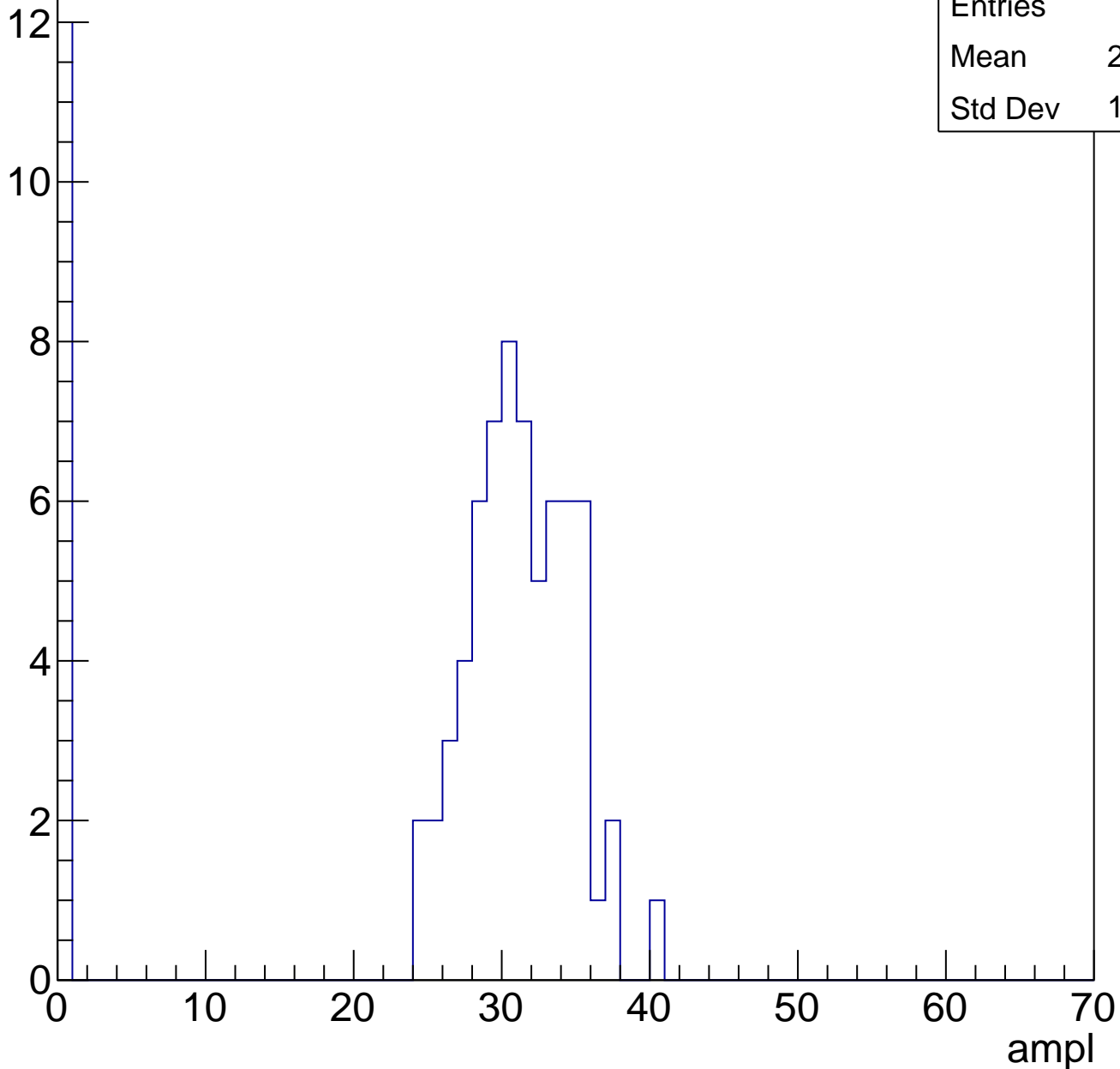
ampl

B1L103S, U11-ch50, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	78
Mean	26.08
Std Dev	11.55

Entry

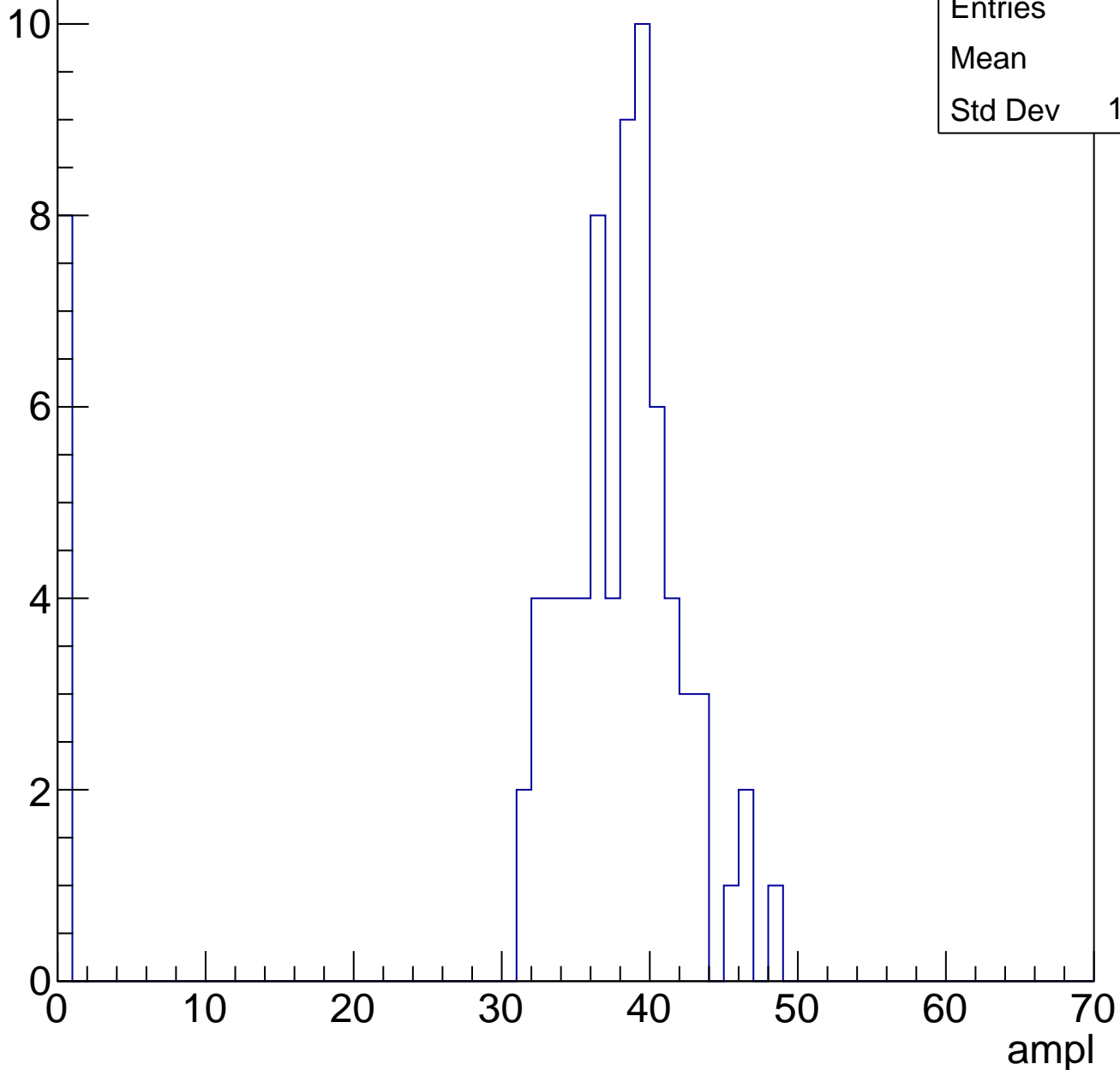


B1L103S, U11-ch50, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	77
Mean	33.9
Std Dev	12.06

Entry

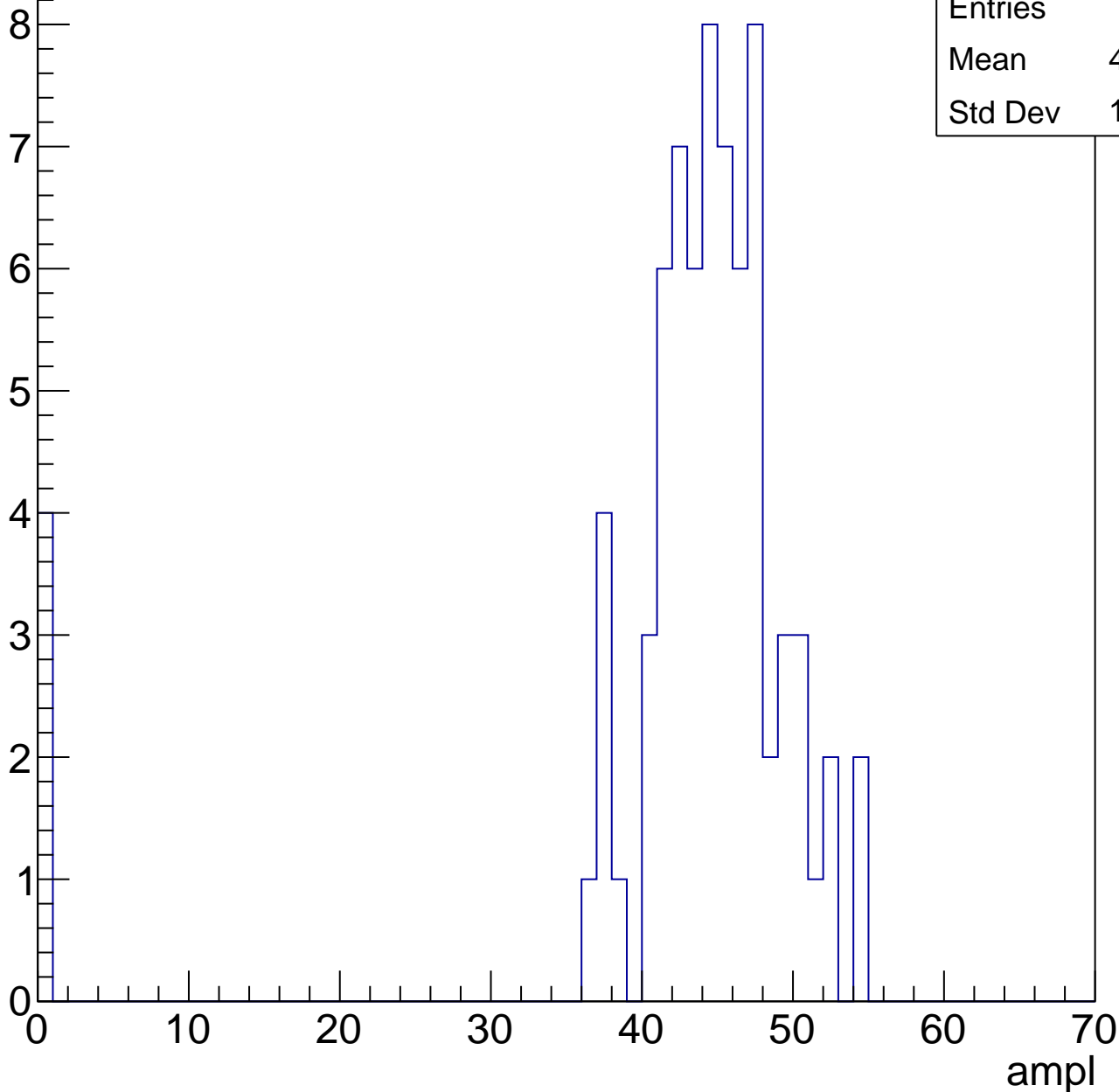


B1L103S, U11-ch50, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	42.09
Std Dev	10.78

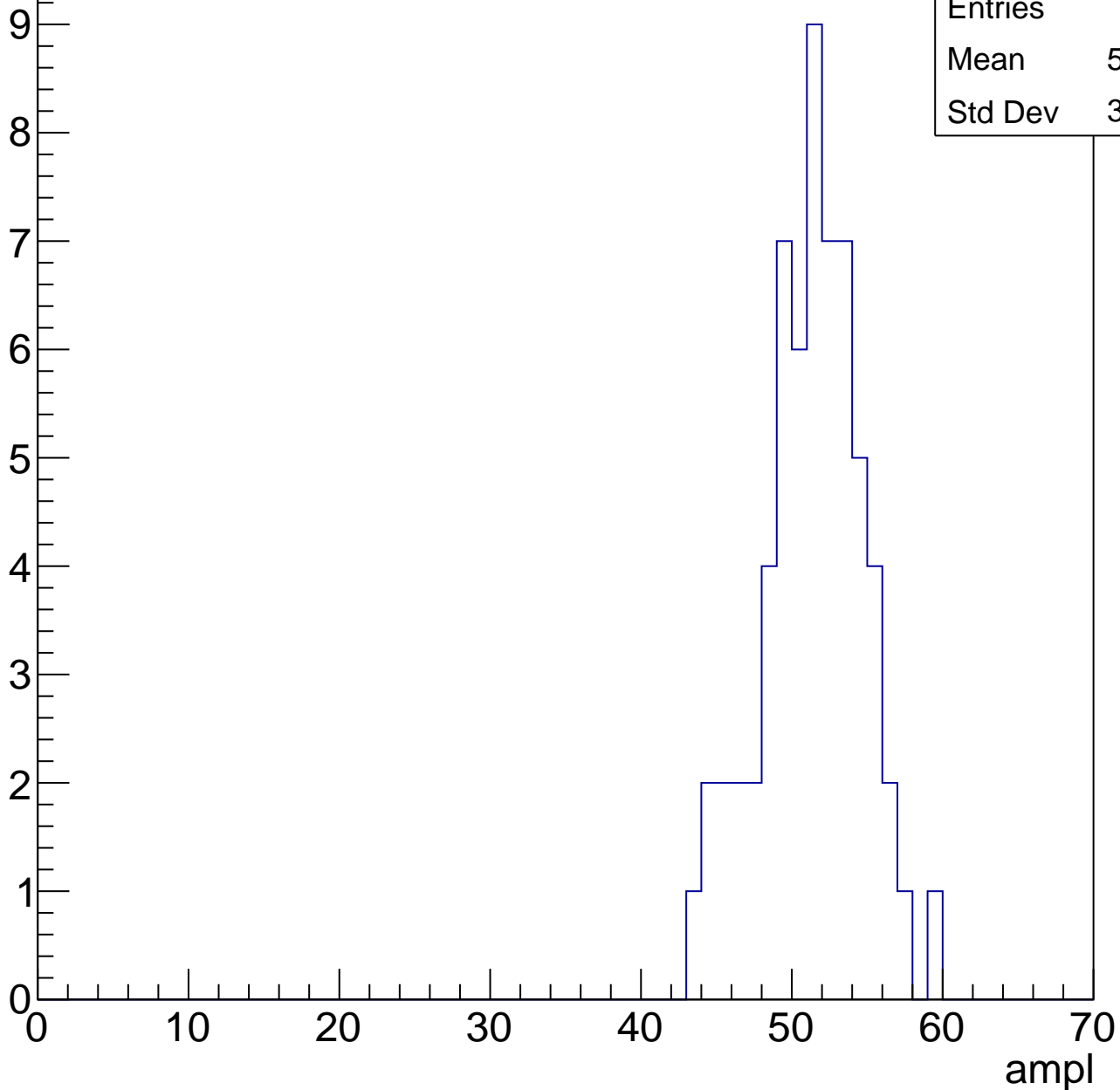


B1L103S, U11-ch50, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	50.87
Std Dev	3.309

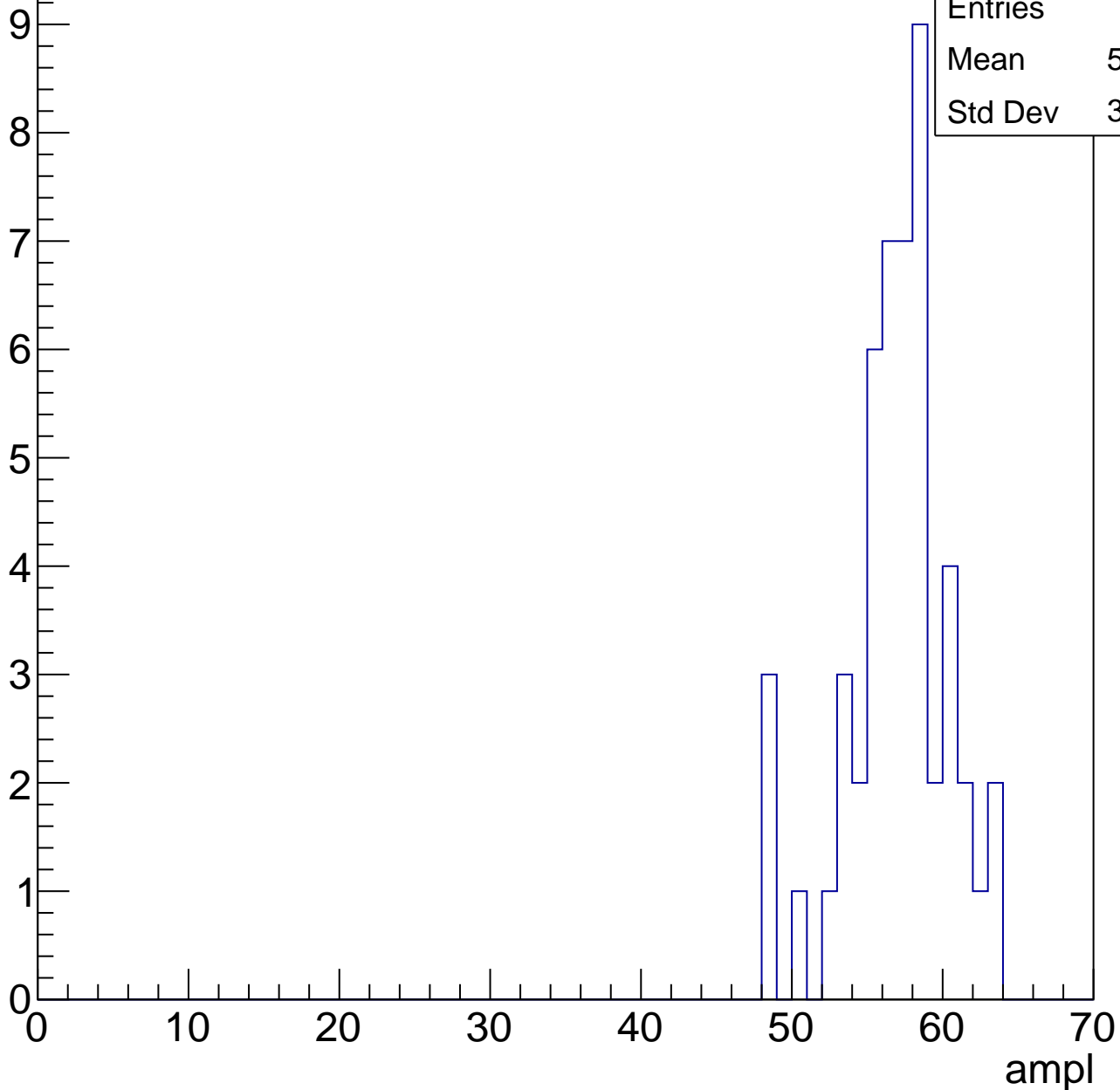


B1L103S, U11-ch50, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	56.48
Std Dev	3.413

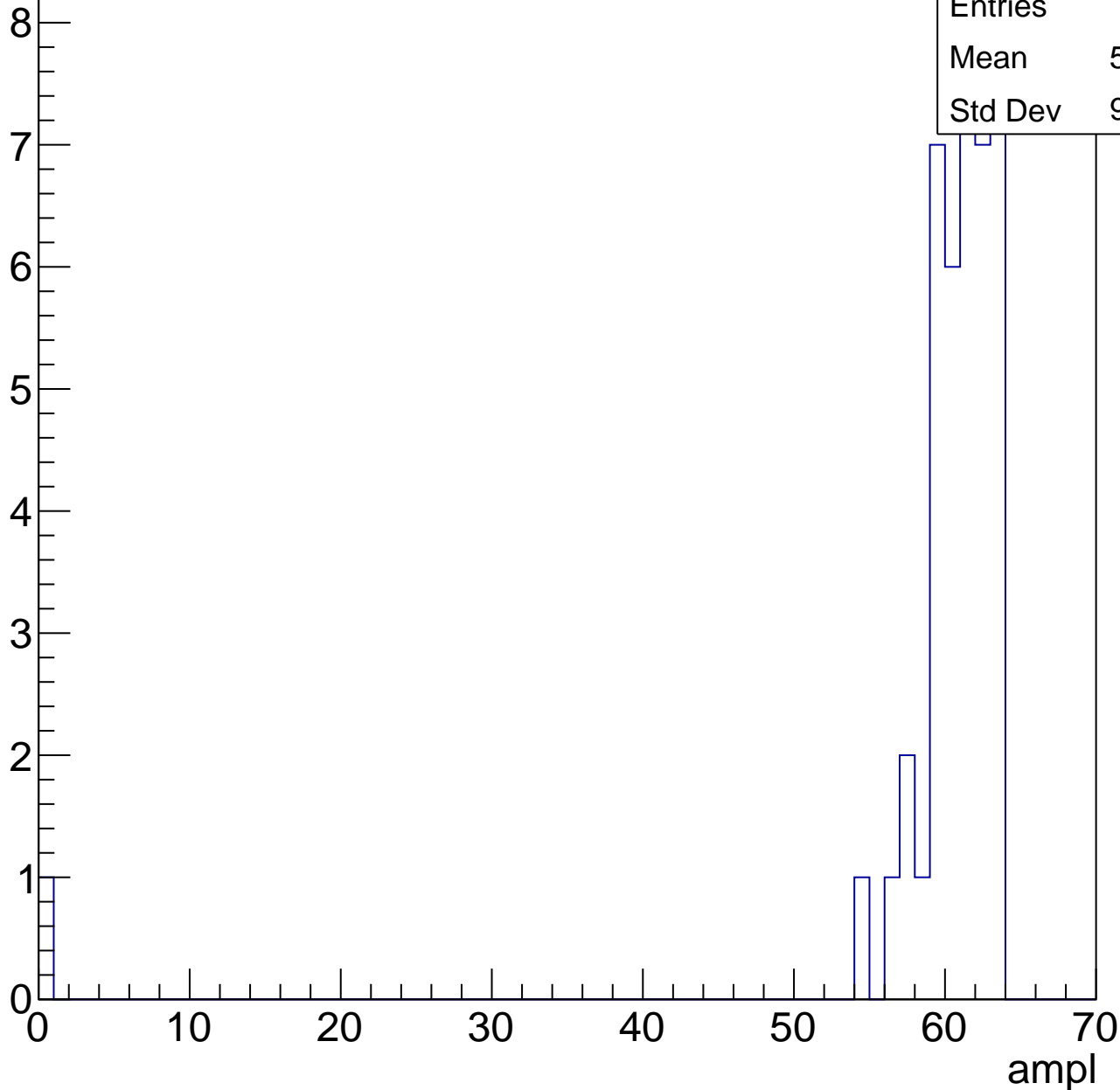


B1L103S, U11-ch50, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	42
Mean	59.07
Std Dev	9.453



B1L103S, U11-ch50, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch50, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

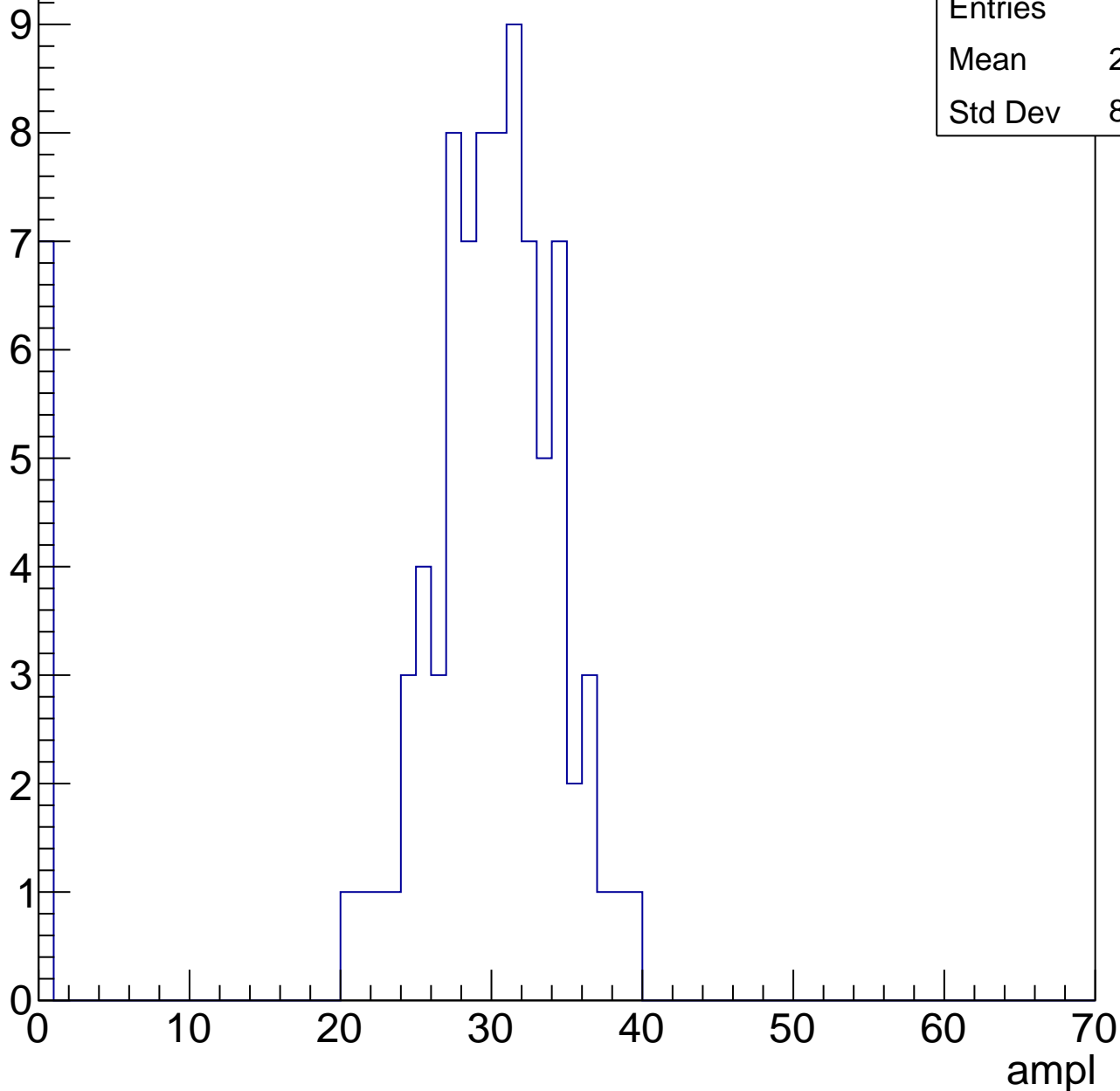


B1L103S, U11-ch51, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	88
Mean	27.48
Std Dev	8.883

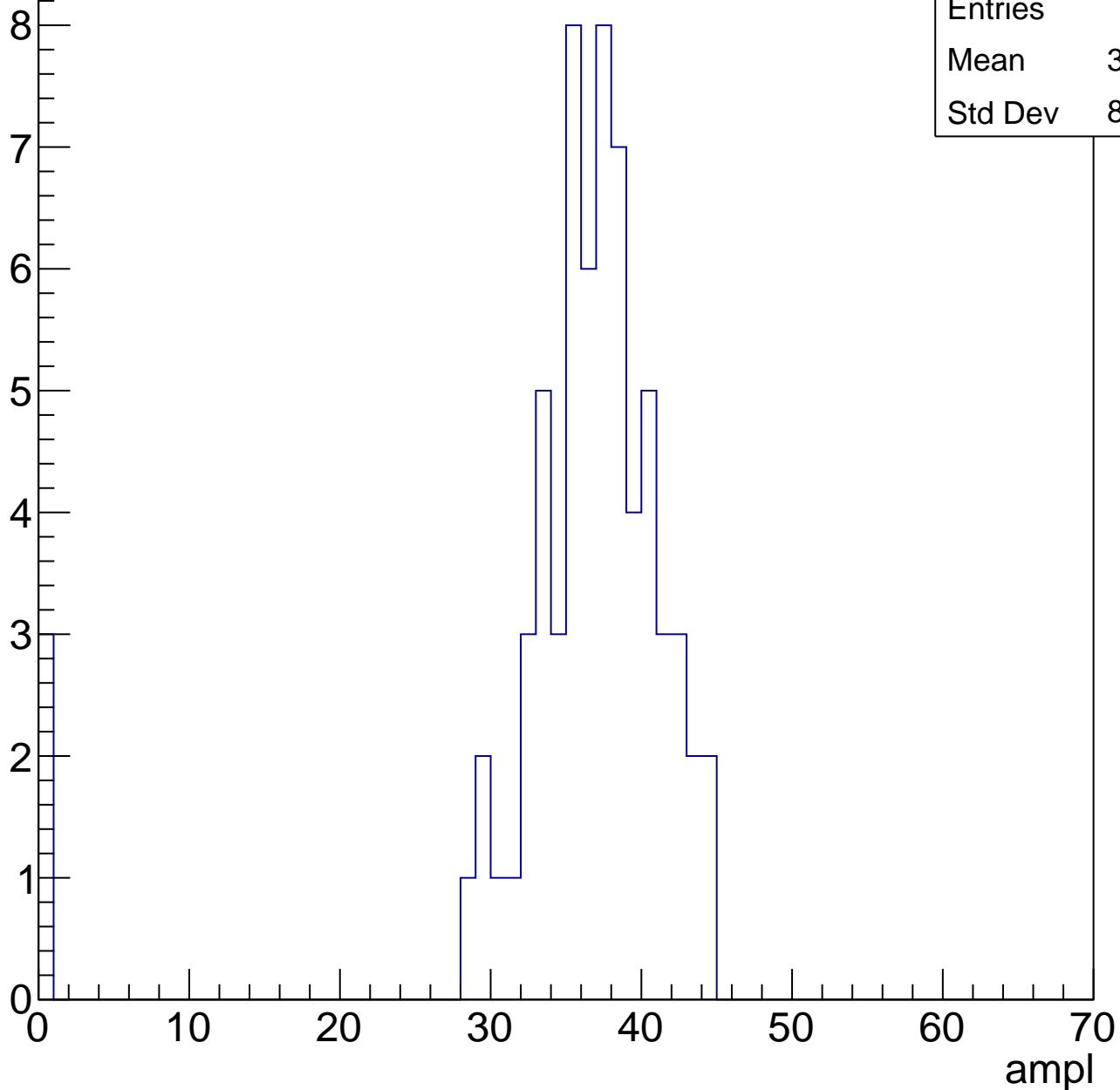


B1L103S, U11-ch51, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	35.03
Std Dev	8.395

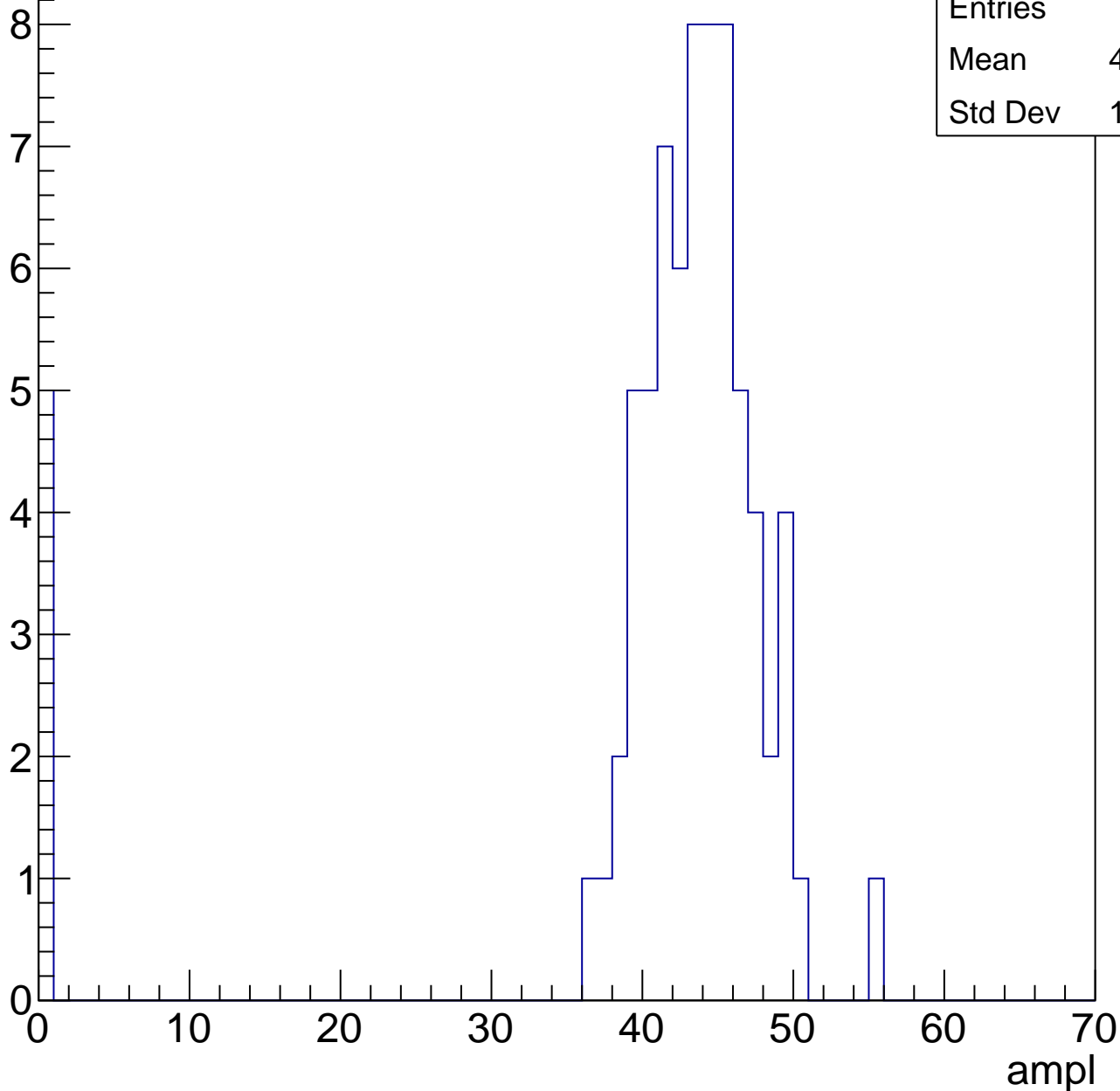


B1L103S, U11-ch51, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

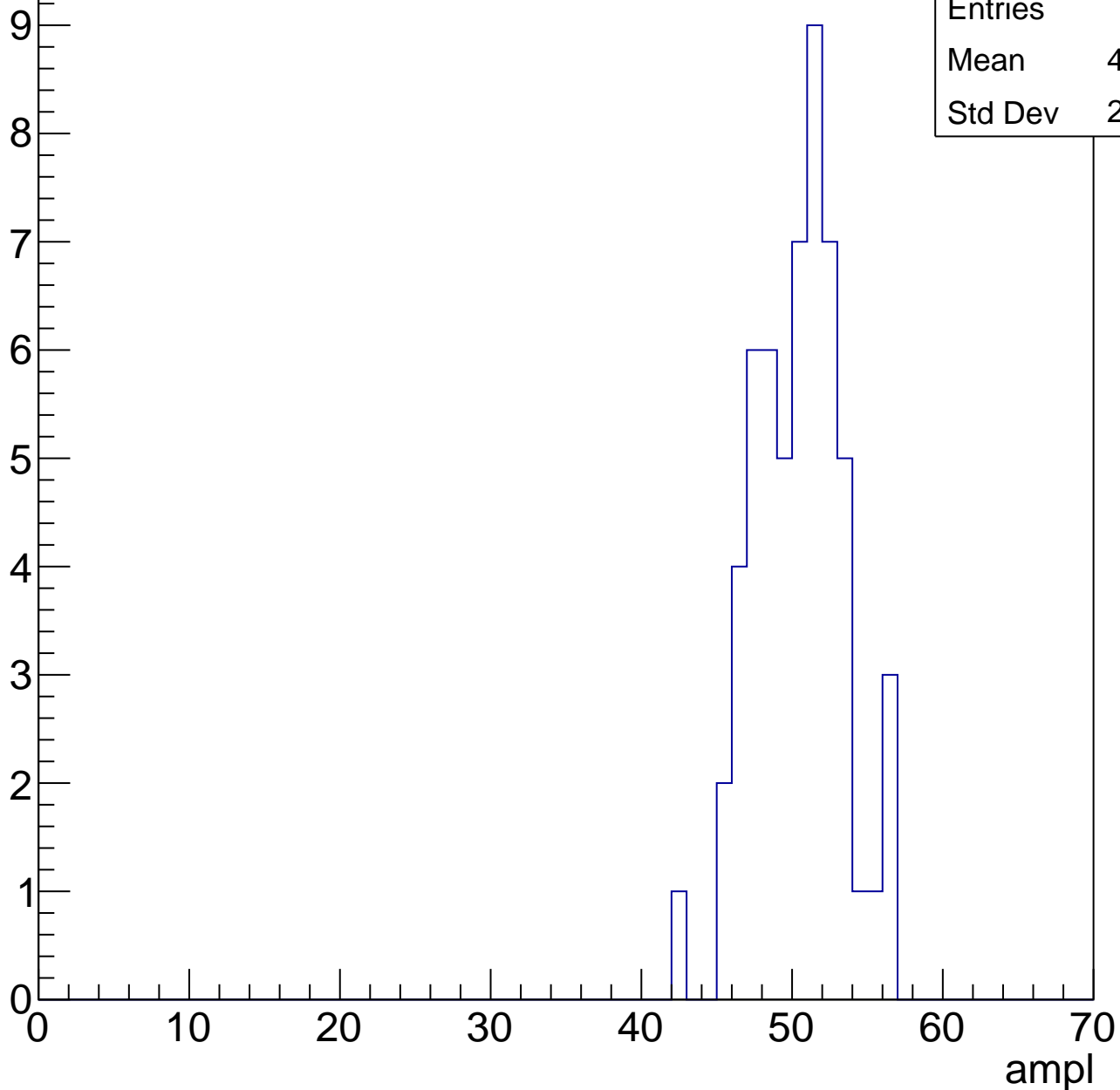
Entries	73
Mean	40.47
Std Dev	11.47



B1L103S, U11-ch51, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

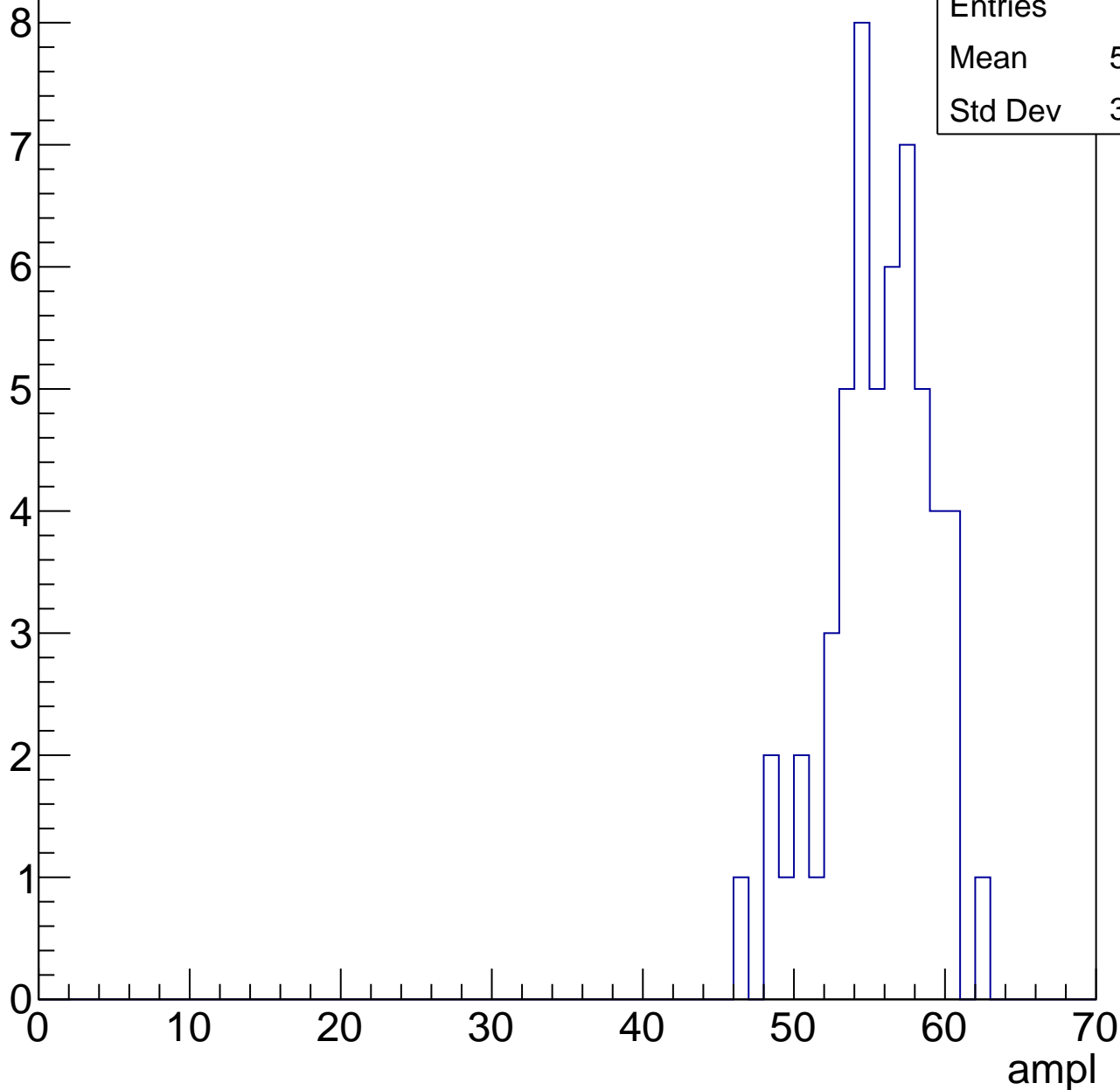


B1L103S, U11-ch51, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	55.15
Std Dev	3.376

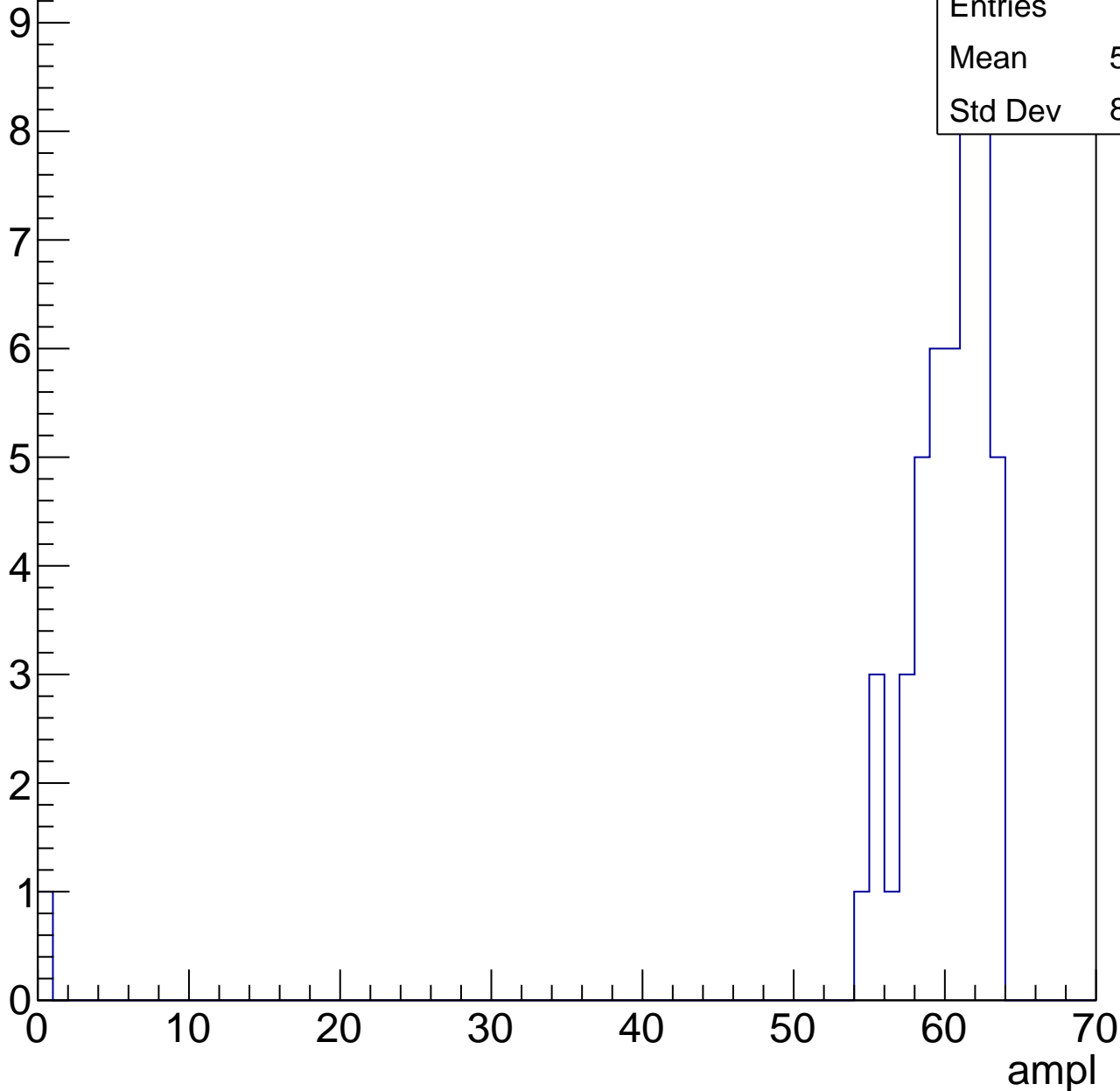


B1L103S, U11-ch51, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	48
Mean	58.54
Std Dev	8.855

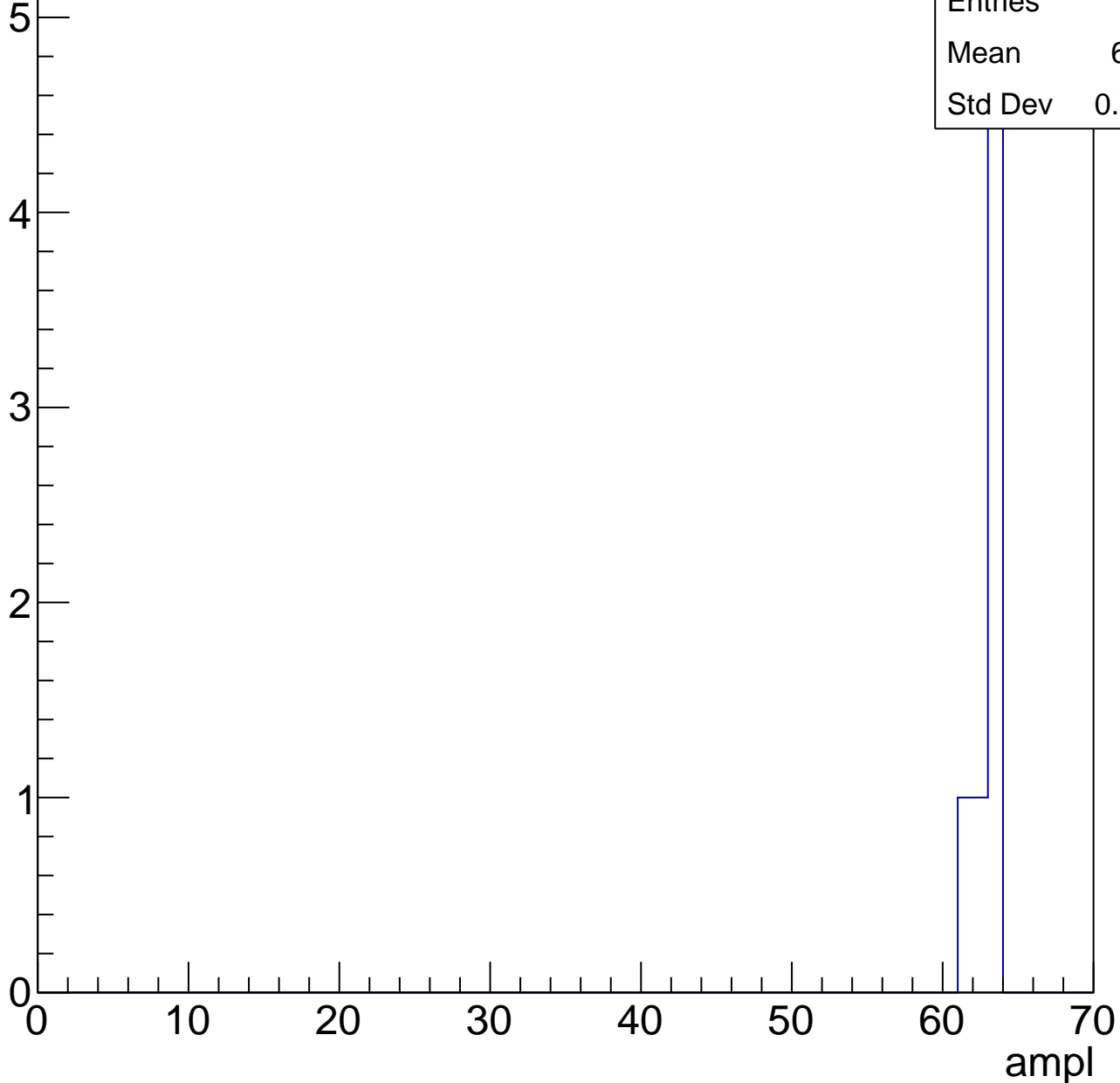


B1L103S, U11-ch51, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	7
Mean	62.57
Std Dev	0.7284



B1L103S, U11-ch51, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

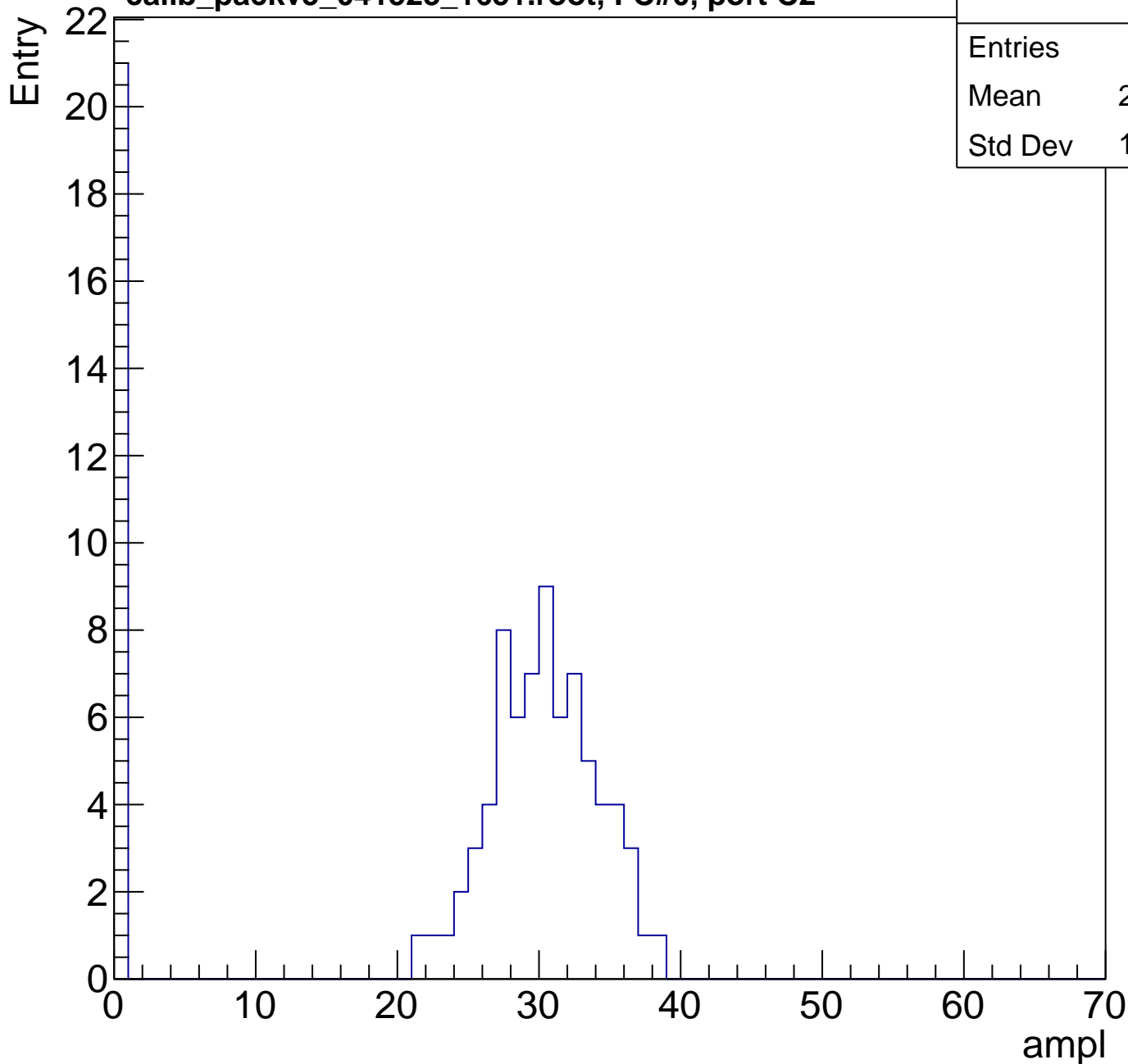
ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U11-ch52, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	94
Mean	23.23
Std Dev	12.87



B1L103S, U11-ch52, adc1

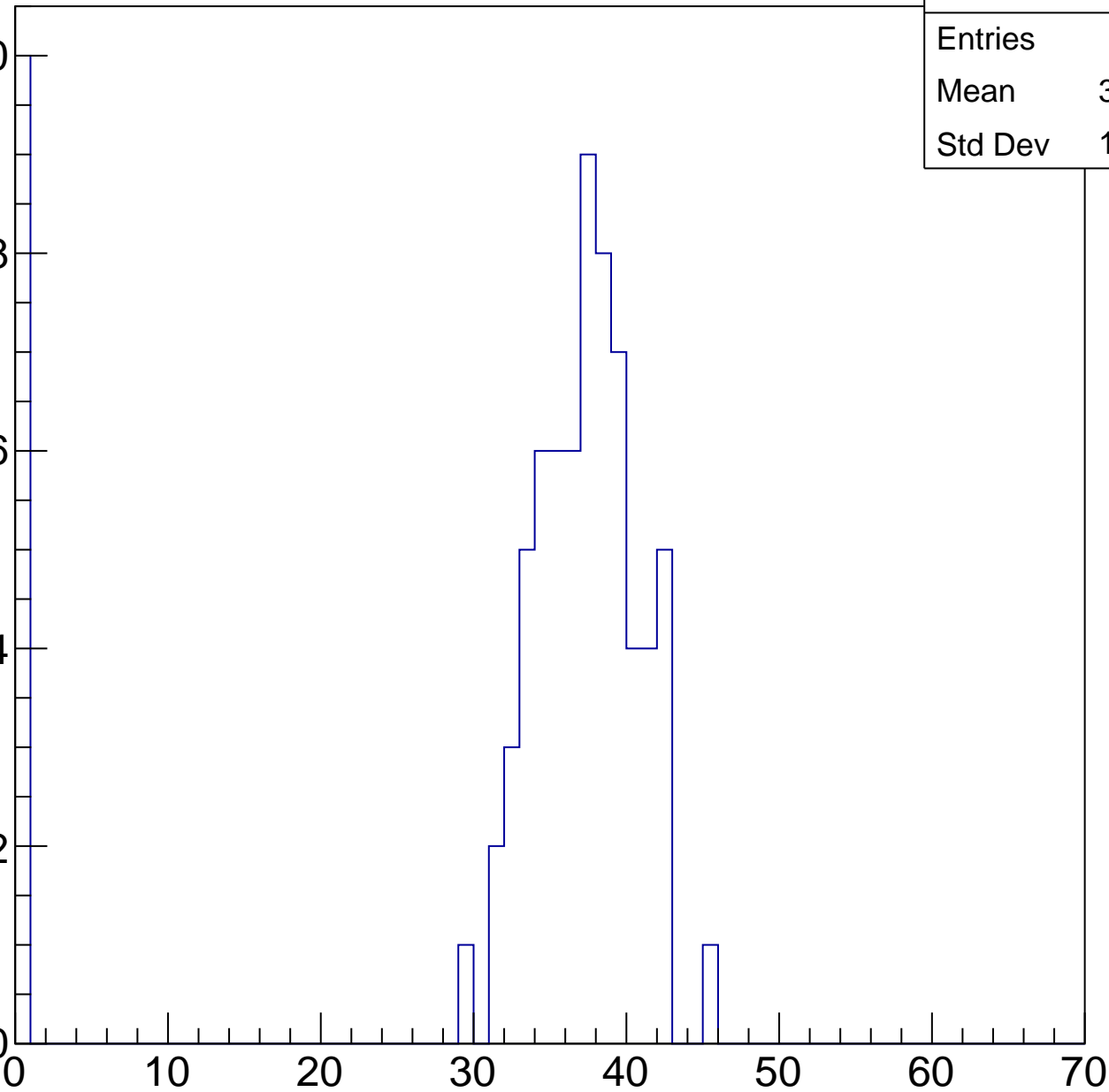
calib_packv5_041523_1651.root, FC#0, port C2

Entries	77
Mean	32.09
Std Dev	12.76

Entry

10
8
6
4
2
0

ampl

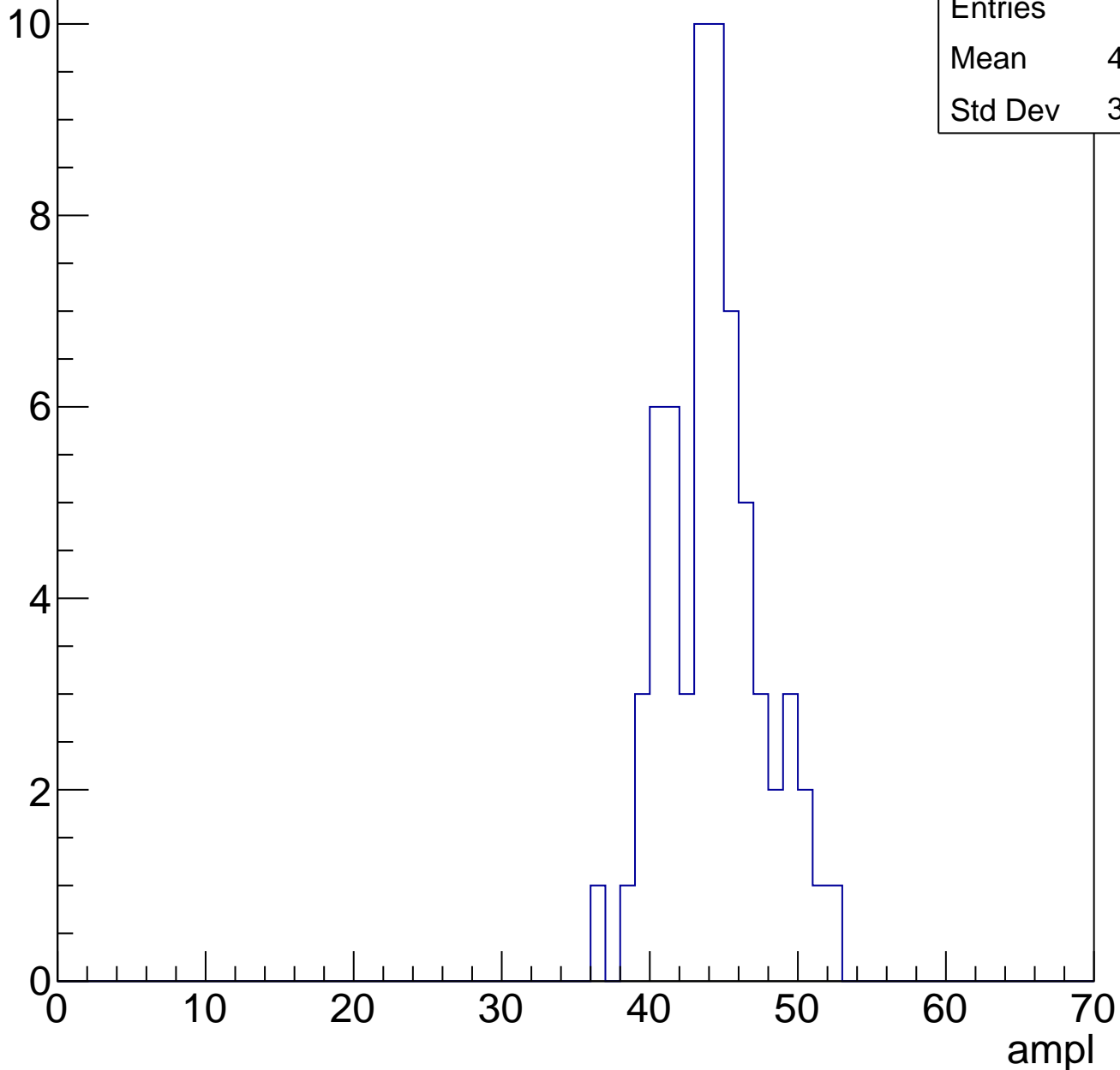


B1L103S, U11-ch52, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	64
Mean	43.83
Std Dev	3.286

Entry

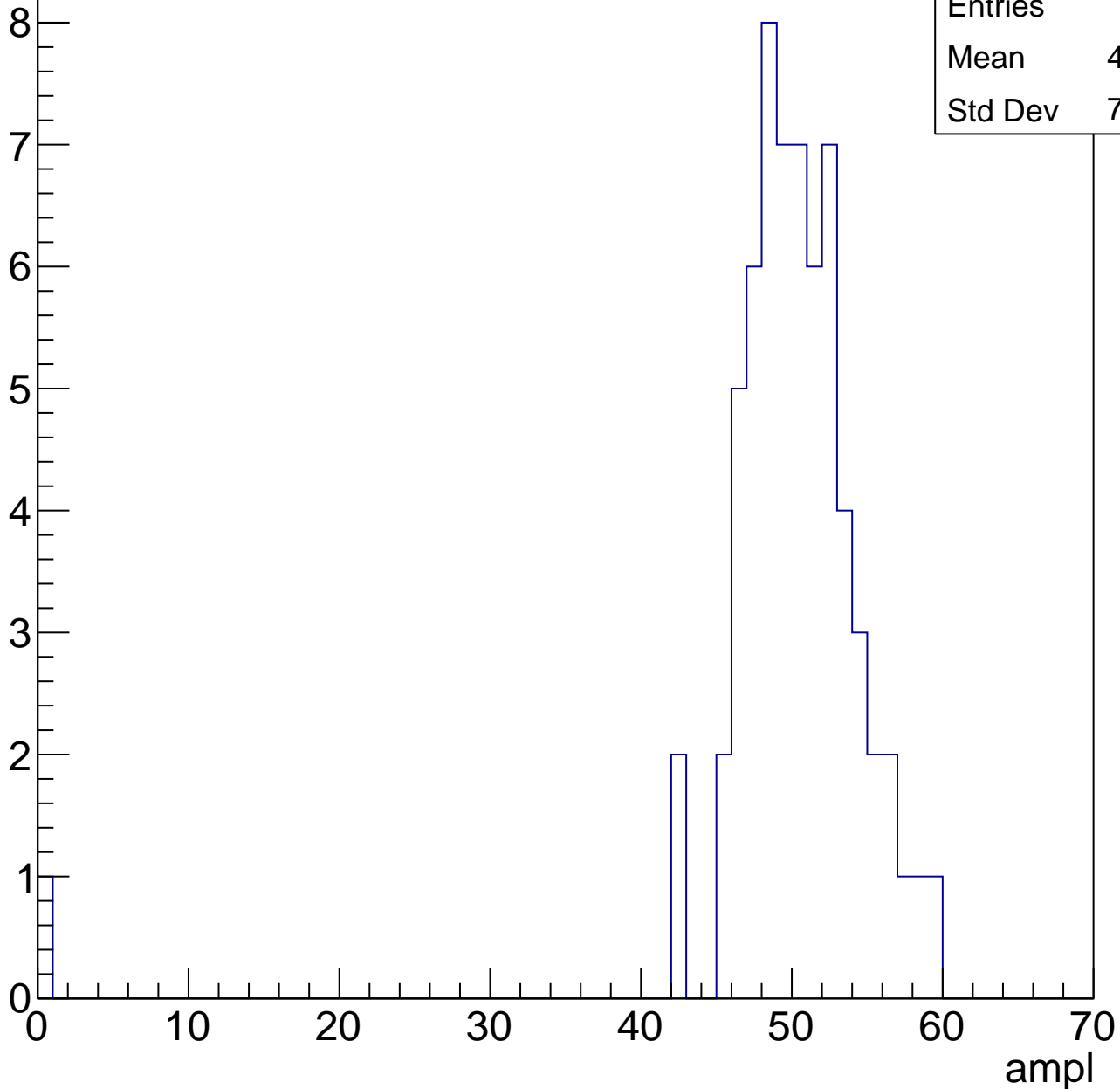


B1L103S, U11-ch52, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

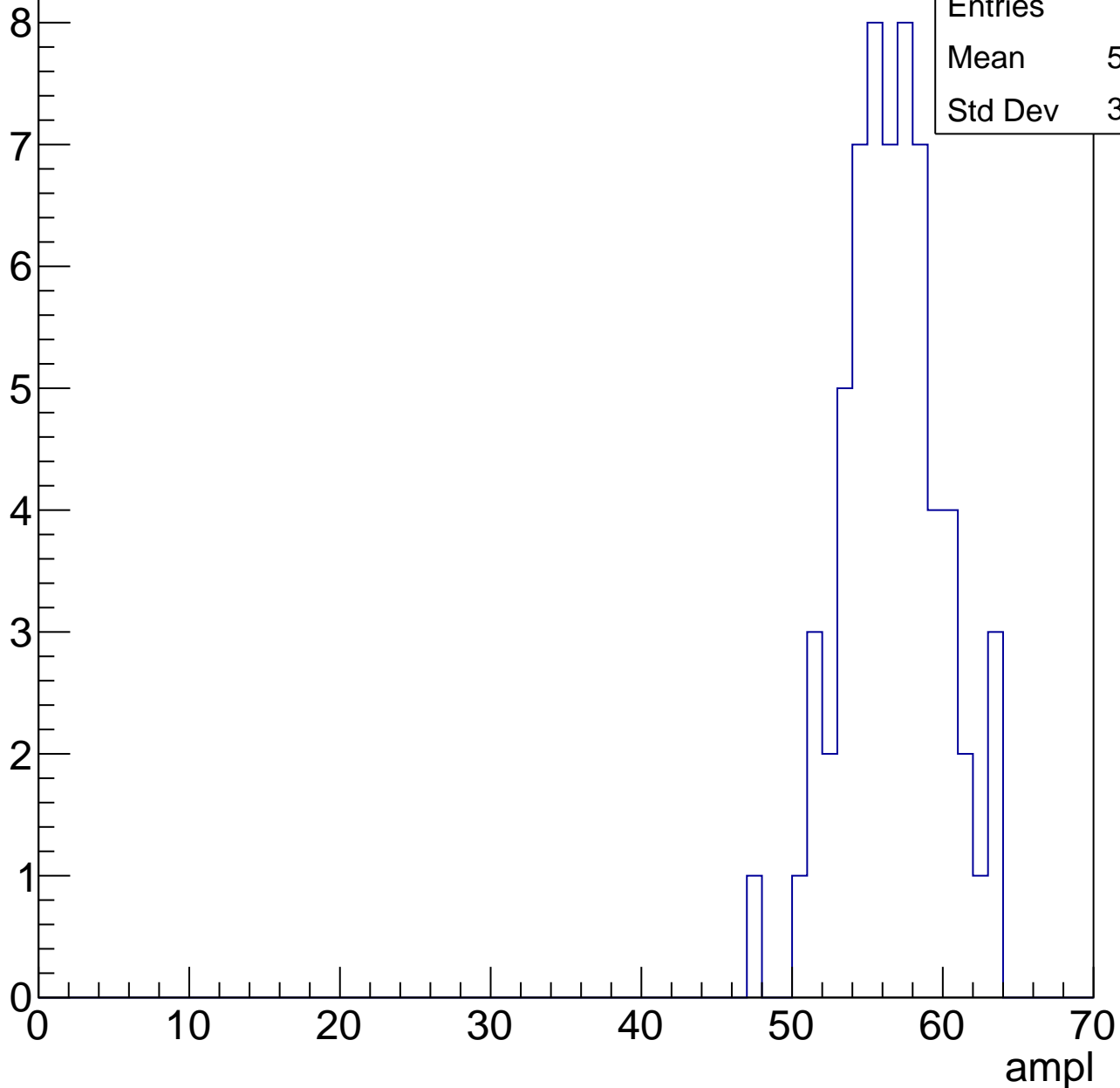
Entries	65
Mean	49.28
Std Dev	7.072



B1L103S, U11-ch52, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

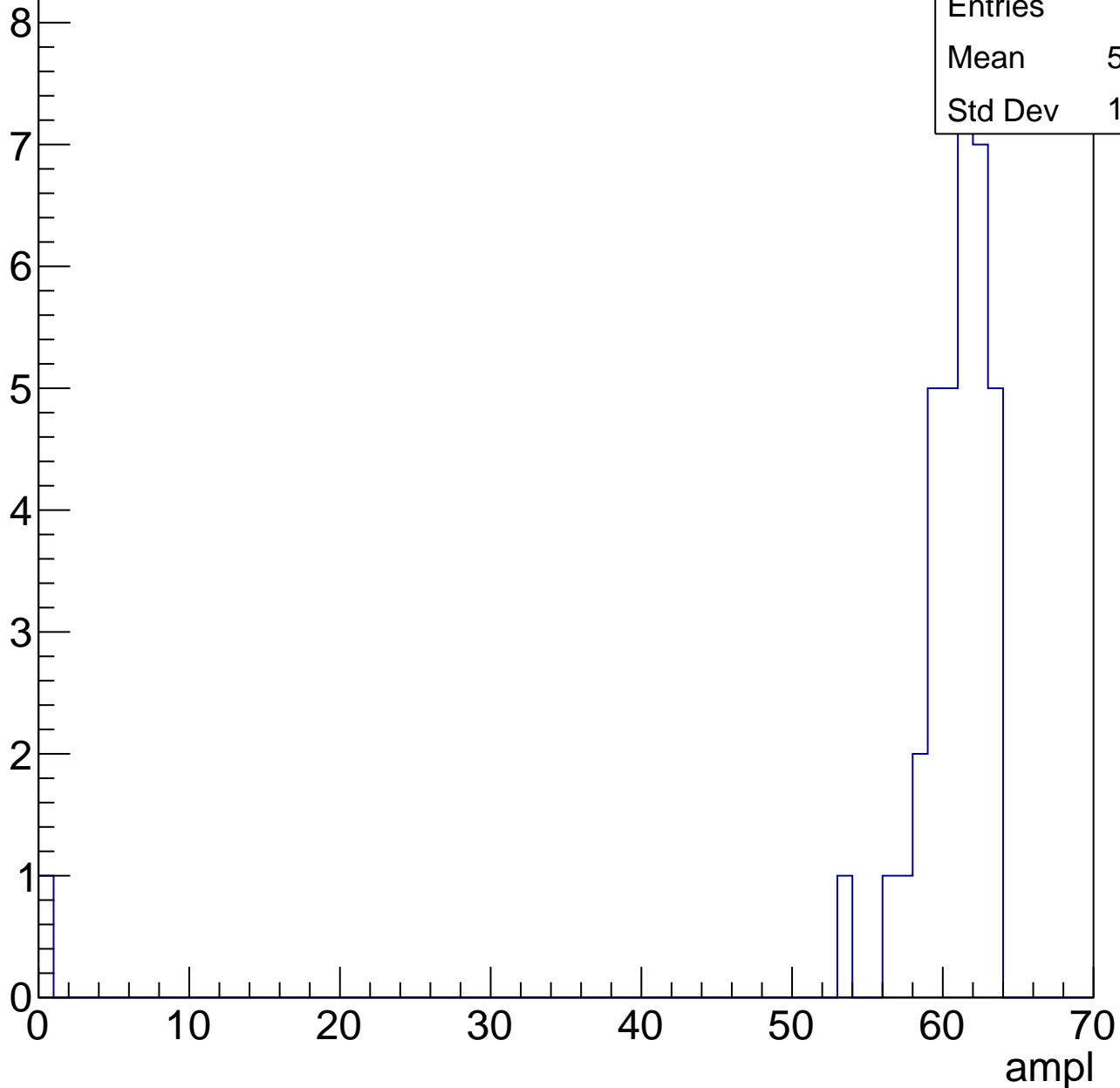


B1L103S, U11-ch52, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	36
Mean	58.72
Std Dev	10.15



B1L103S, U11-ch52, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	5
Mean	62
Std Dev	1.095

B1L103S, U11-ch52, adc7

calib_packv5_041523_1651.root, FC#0, port C2

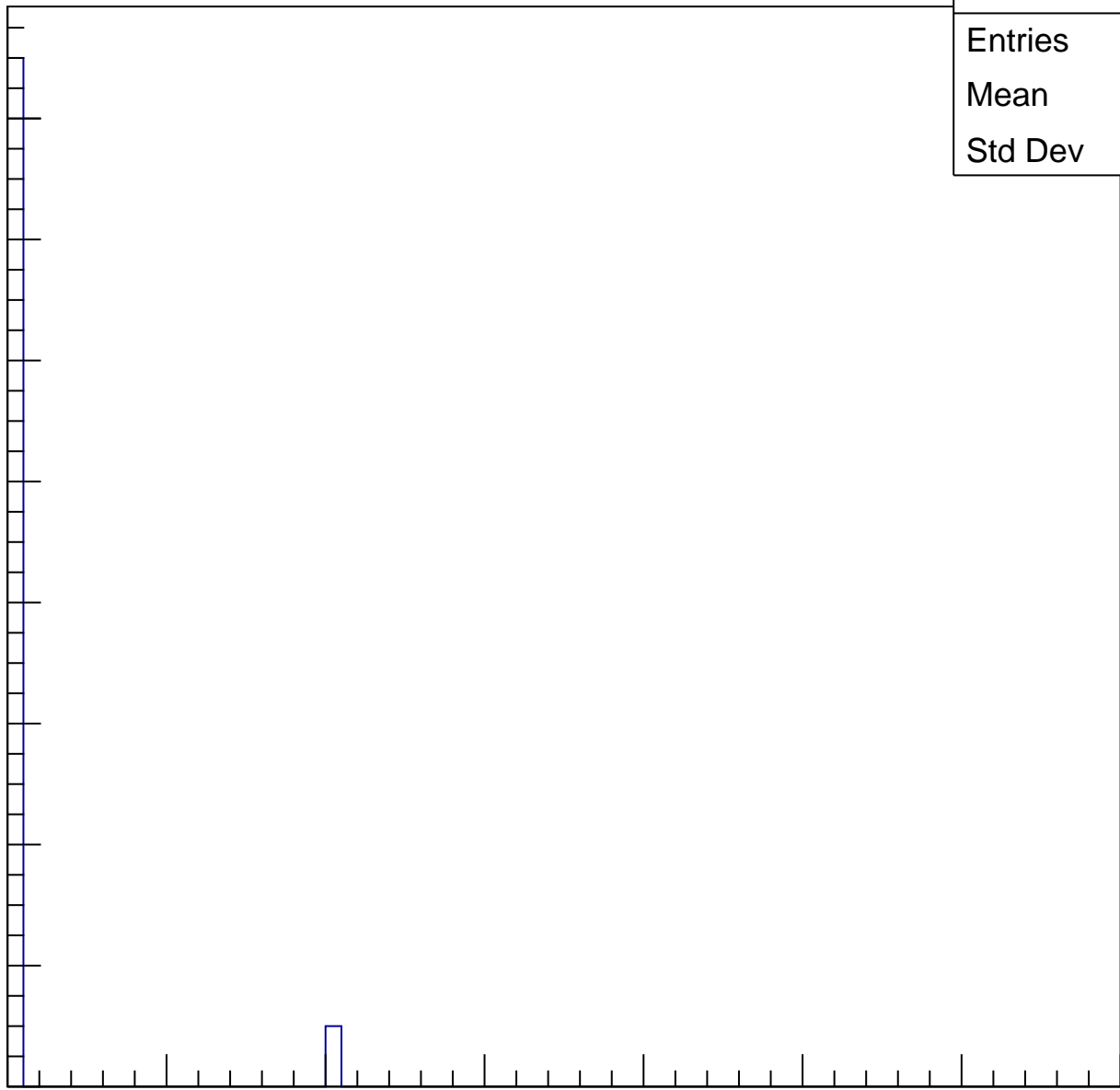
Entries	18
Mean	1.111
Std Dev	4.581

Entry

16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

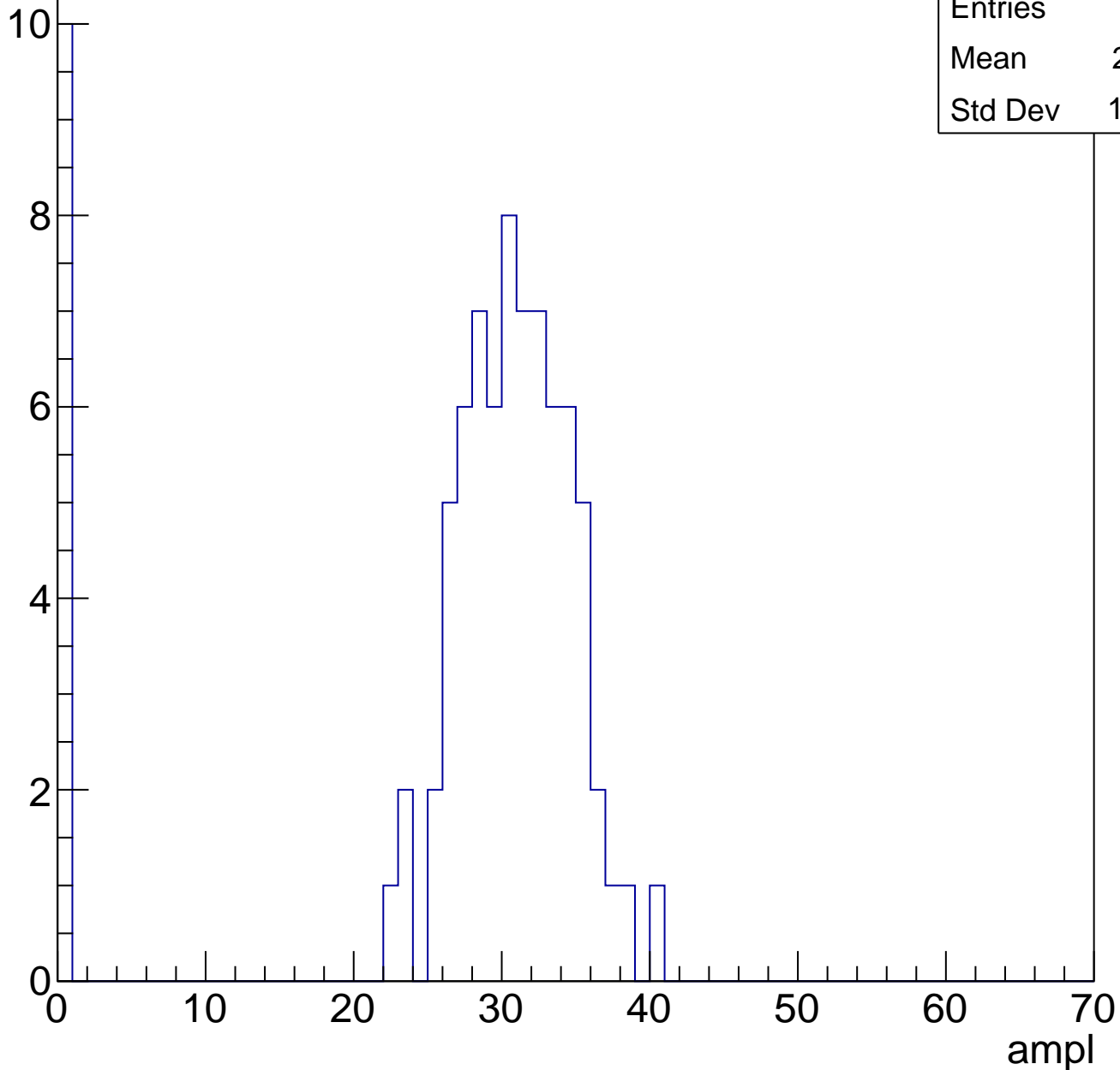


B1L103S, U11-ch53, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	83
Mean	26.81
Std Dev	10.49

Entry

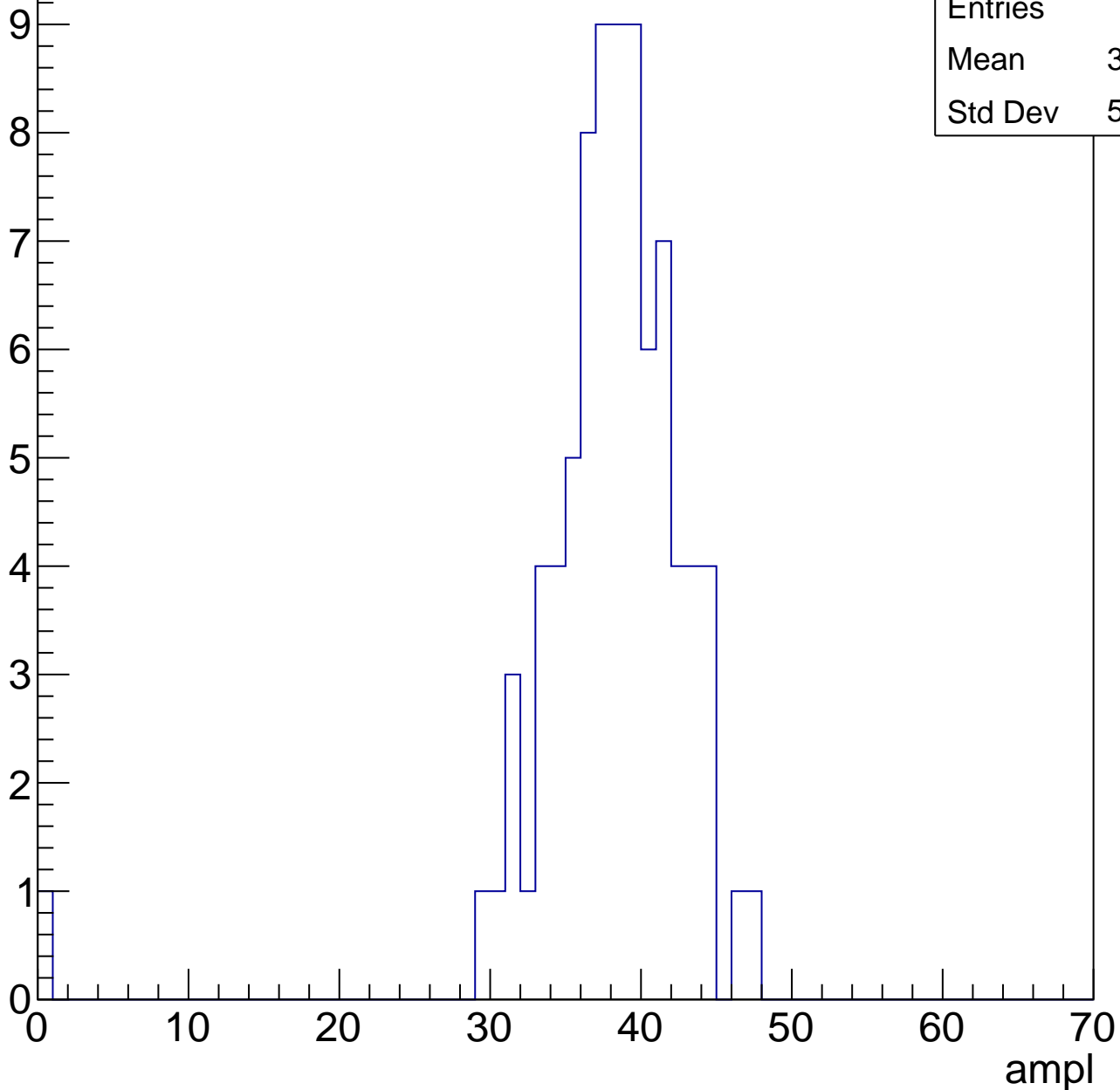


B1L103S, U11-ch53, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	82
Mean	37.52
Std Dev	5.579

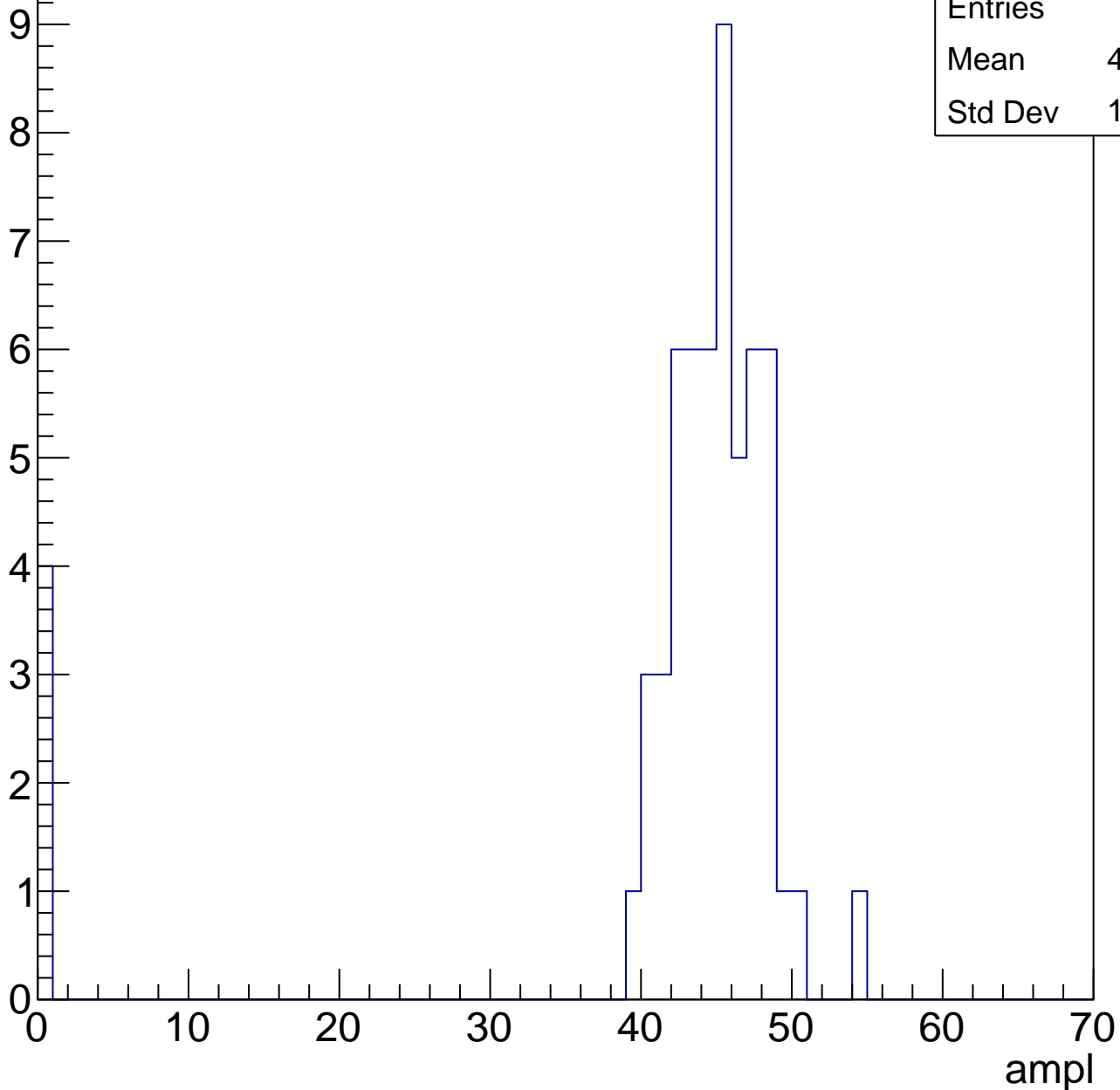


B1L103S, U11-ch53, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	41.62
Std Dev	11.66

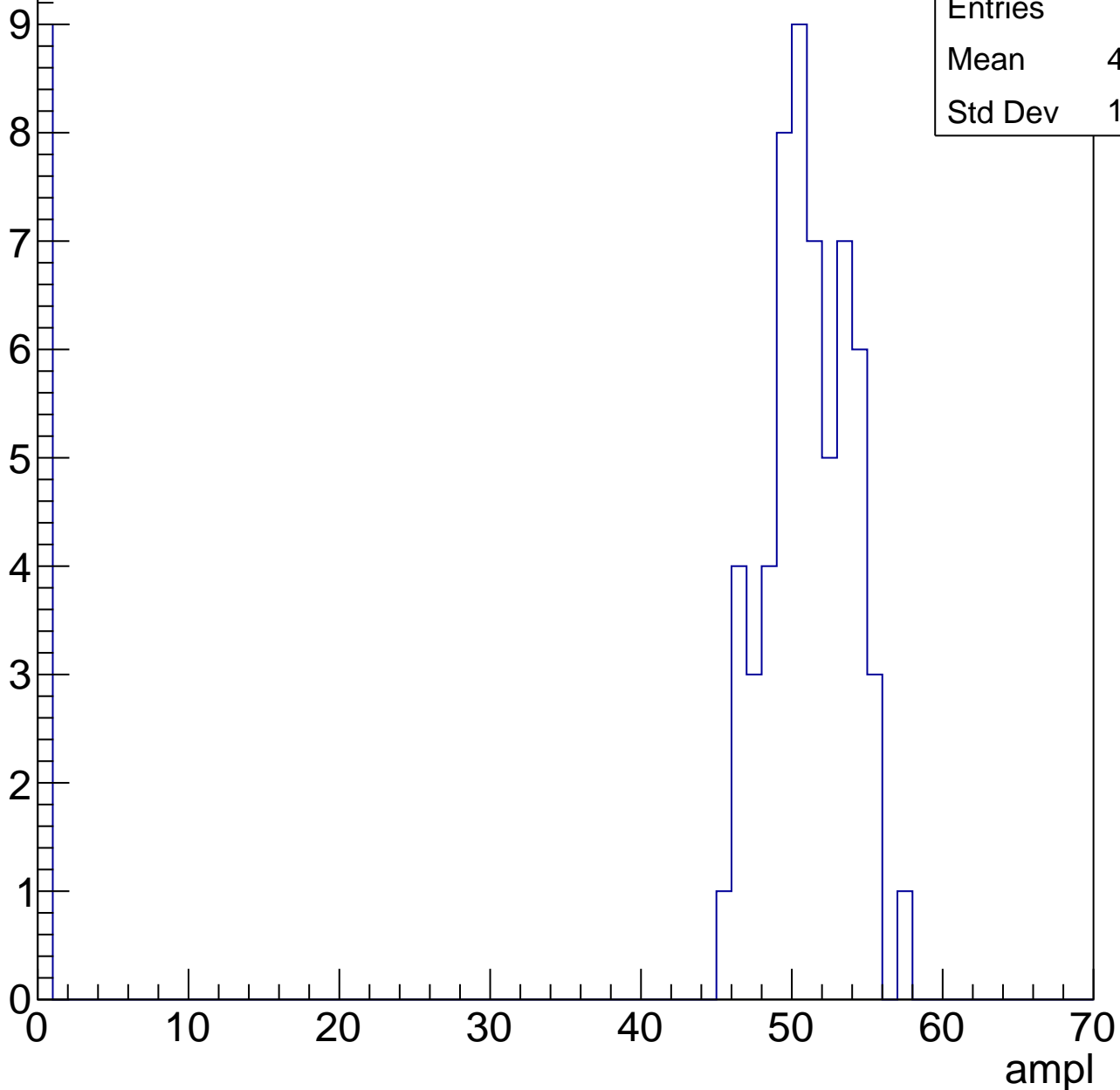


B1L103S, U11-ch53, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	43.85
Std Dev	17.46



B1L103S, U11-ch53, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	59
Mean	56.53
Std Dev	3.264

Entry

10

8

6

4

2

0

0

10

20

30

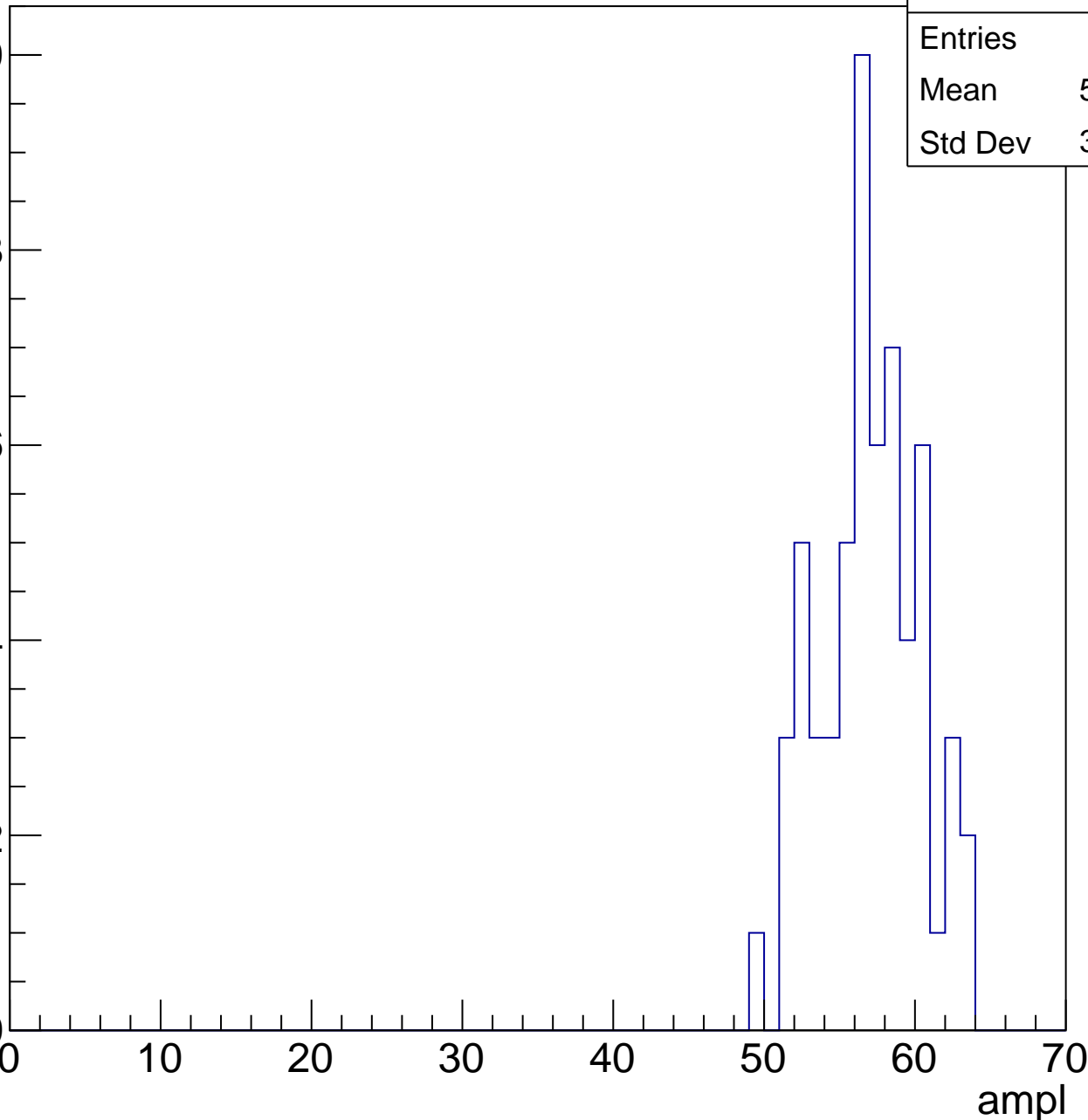
40

50

ampl

60

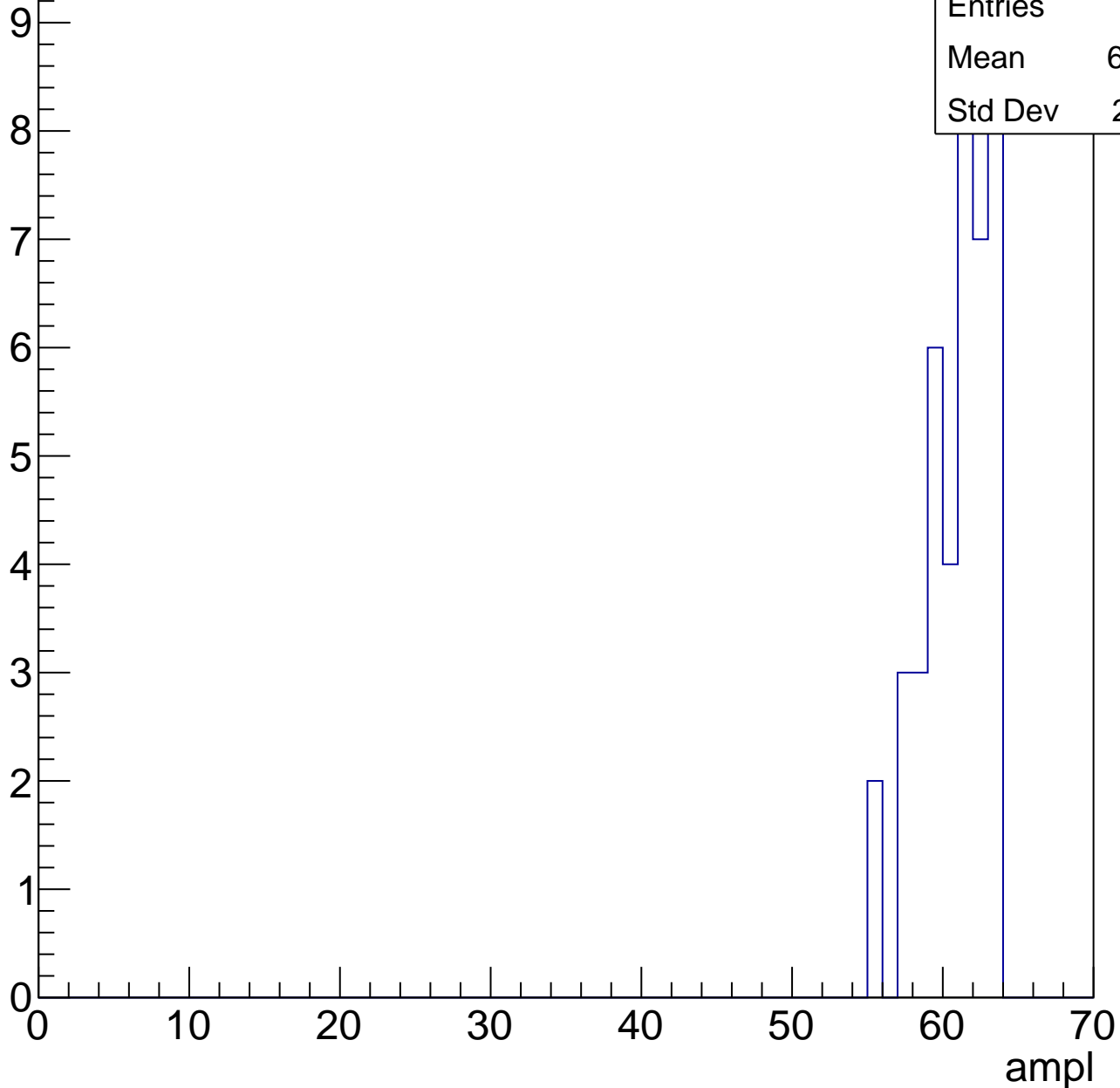
70



B1L103S, U11-ch53, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	42
Mean	60.38
Std Dev	2.171

B1L103S, U11-ch53, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	1
Mean	0
Std Dev	0

B1L103S, U11-ch53, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U11-ch54, adc0

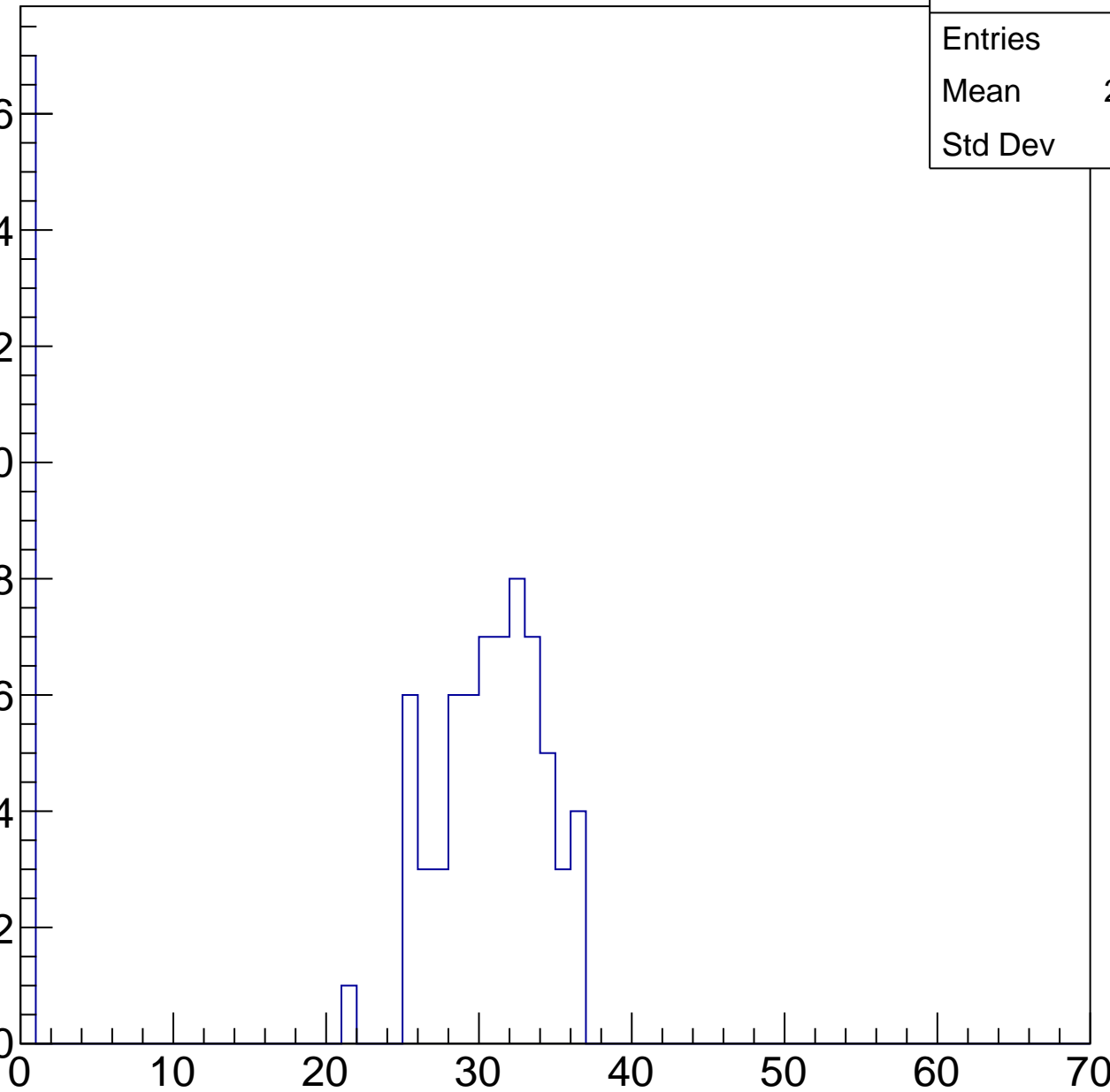
calib_packv5_041523_1651.root, FC#0, port C2

Entries	83
Mean	24.16
Std Dev	12.61

Entry

16
14
12
10
8
6
4
2
0

ampl

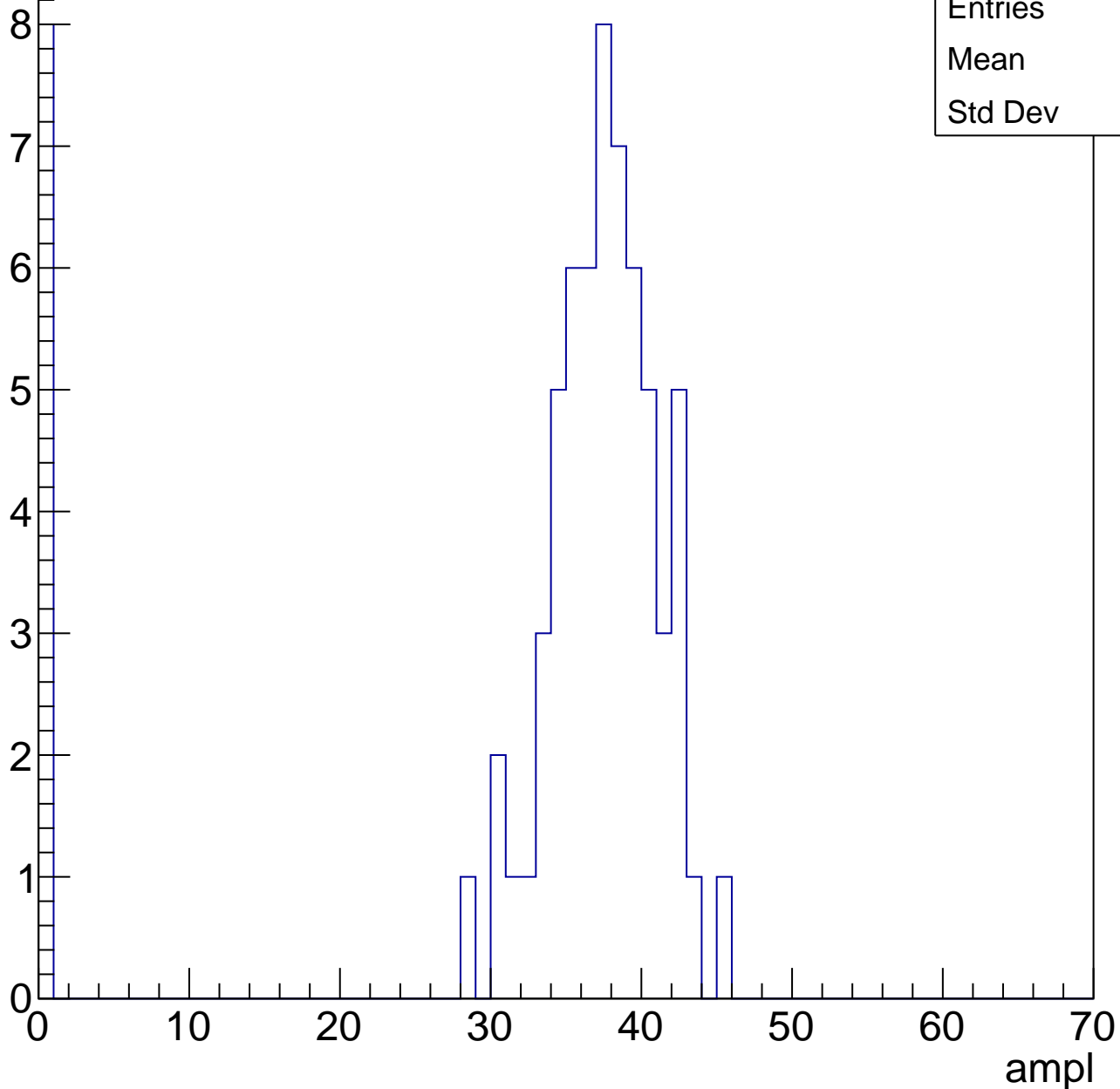


B1L103S, U11-ch54, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	32.8
Std Dev	12.3

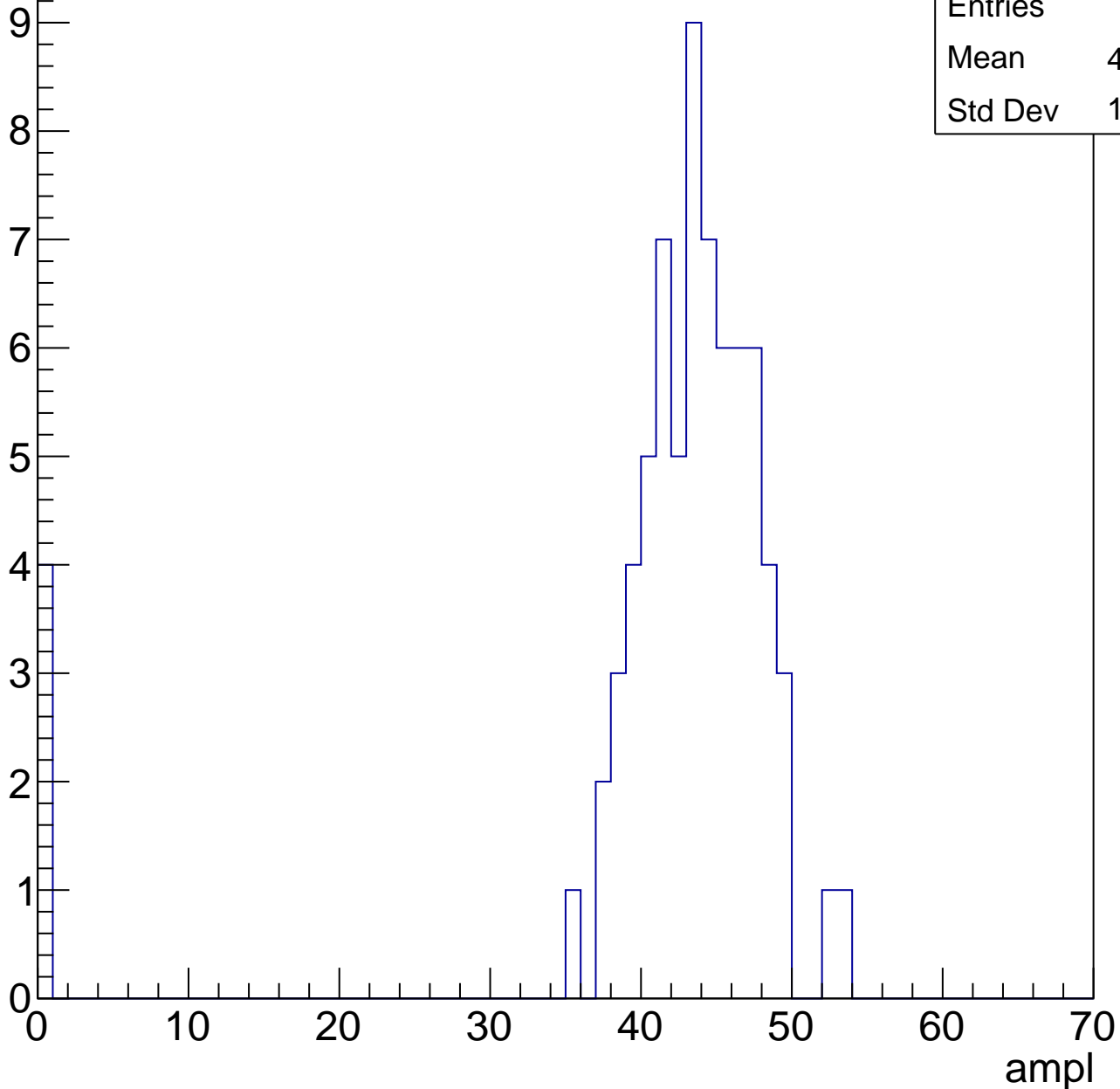


B1L103S, U11-ch54, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

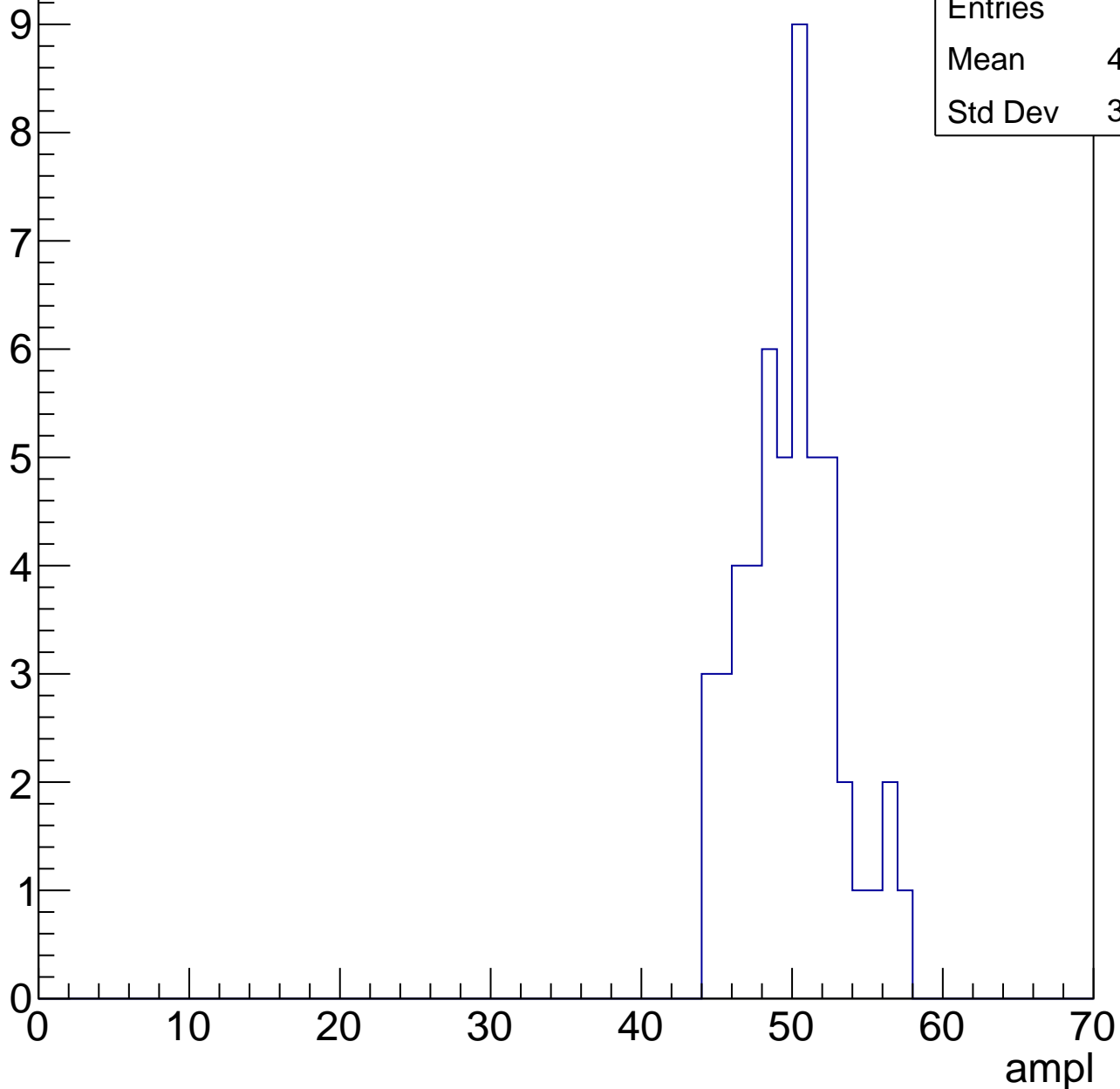
Entries	74
Mean	41.12
Std Dev	10.44



B1L103S, U11-ch54, adc3

calib_packv5_041523_1651.root, FC#0, port C2

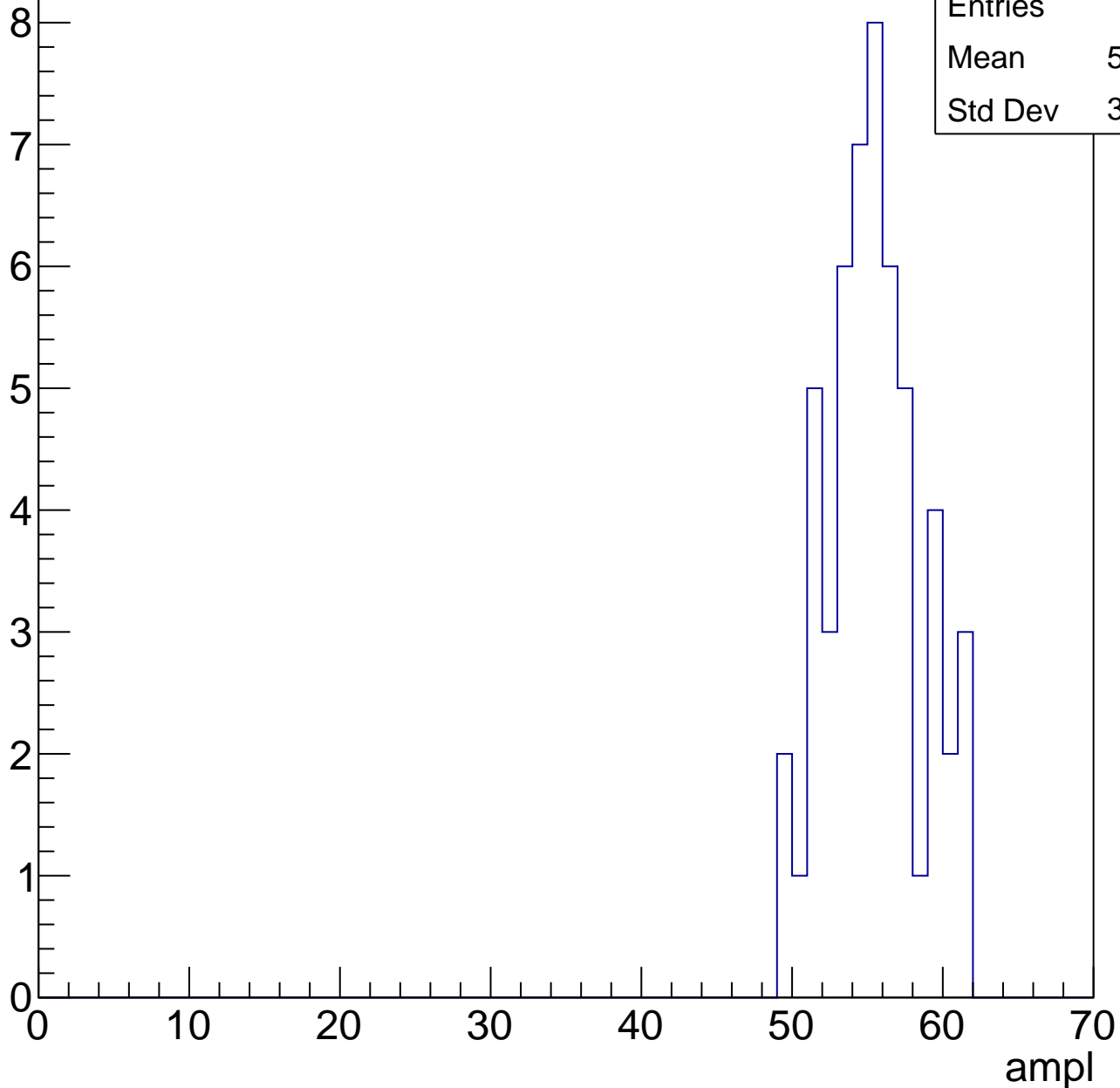
Entry



B1L103S, U11-ch54, adc4

calib_packv5_041523_1651.root, FC#0, port C2

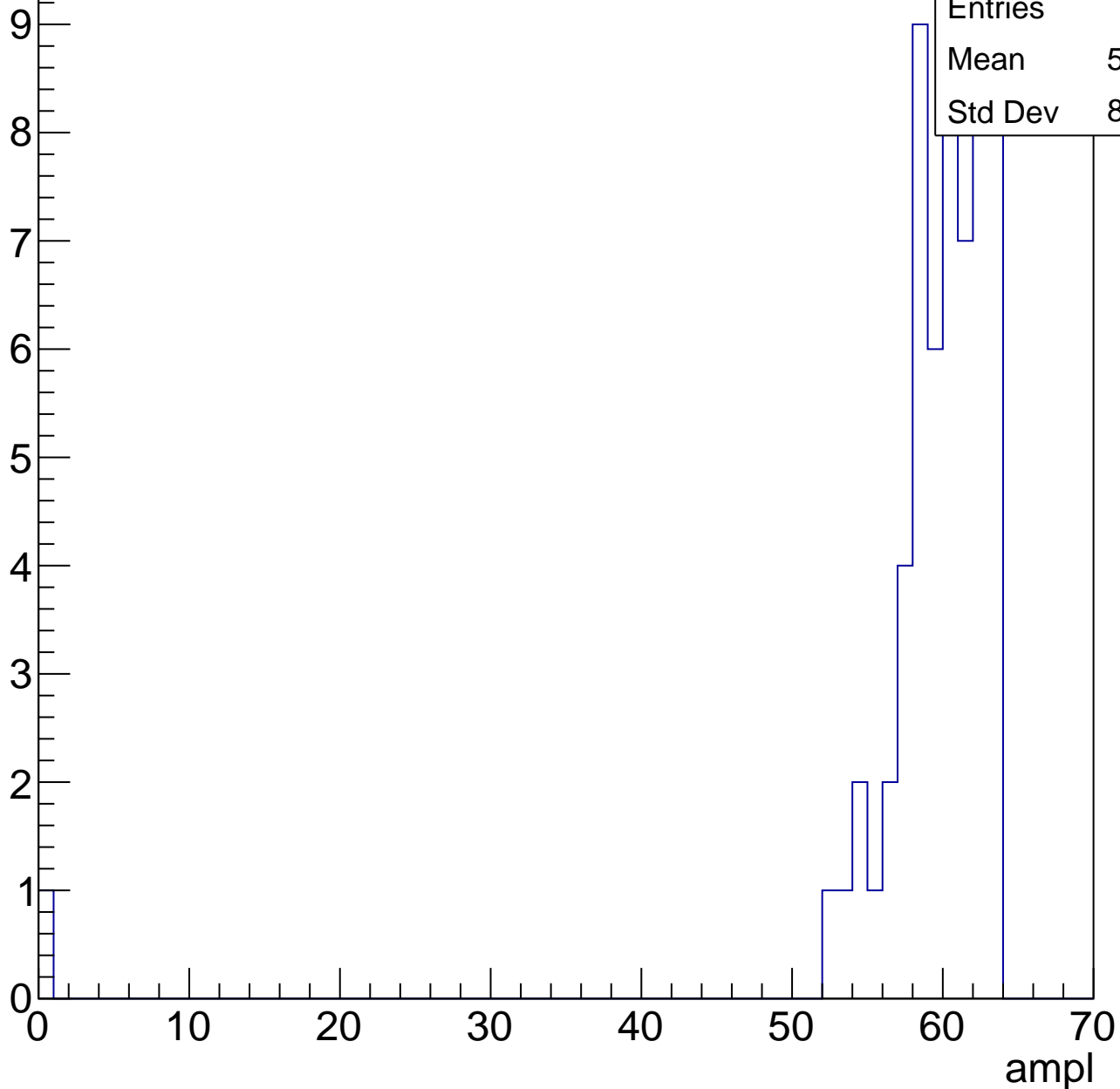
Entry



B1L103S, U11-ch54, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	59
Mean	58.54
Std Dev	8.146

B1L103S, U11-ch54, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch54, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



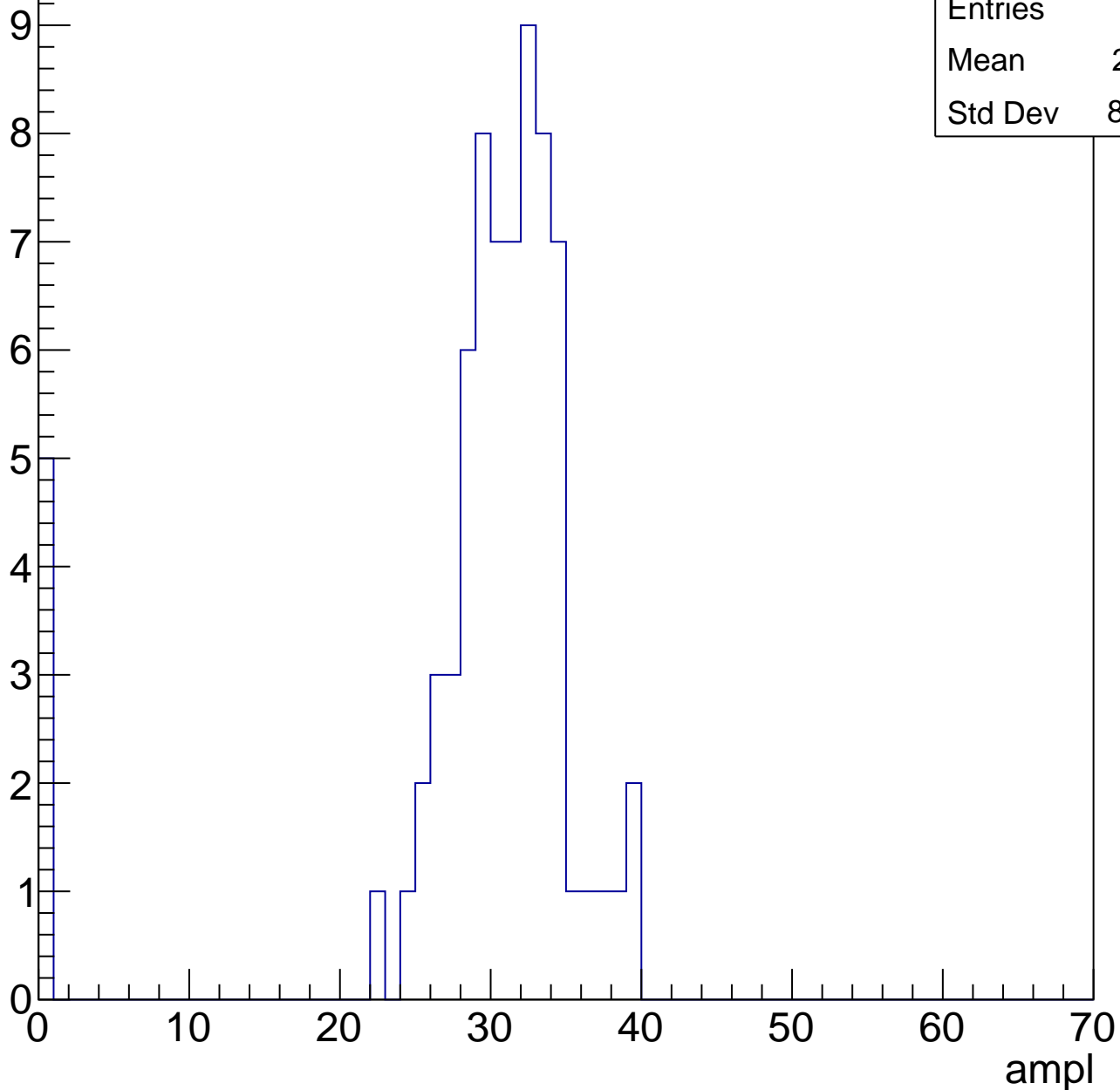
Entries	19
Mean	0
Std Dev	0

B1L103S, U11-ch55, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	28.71
Std Dev	8.439

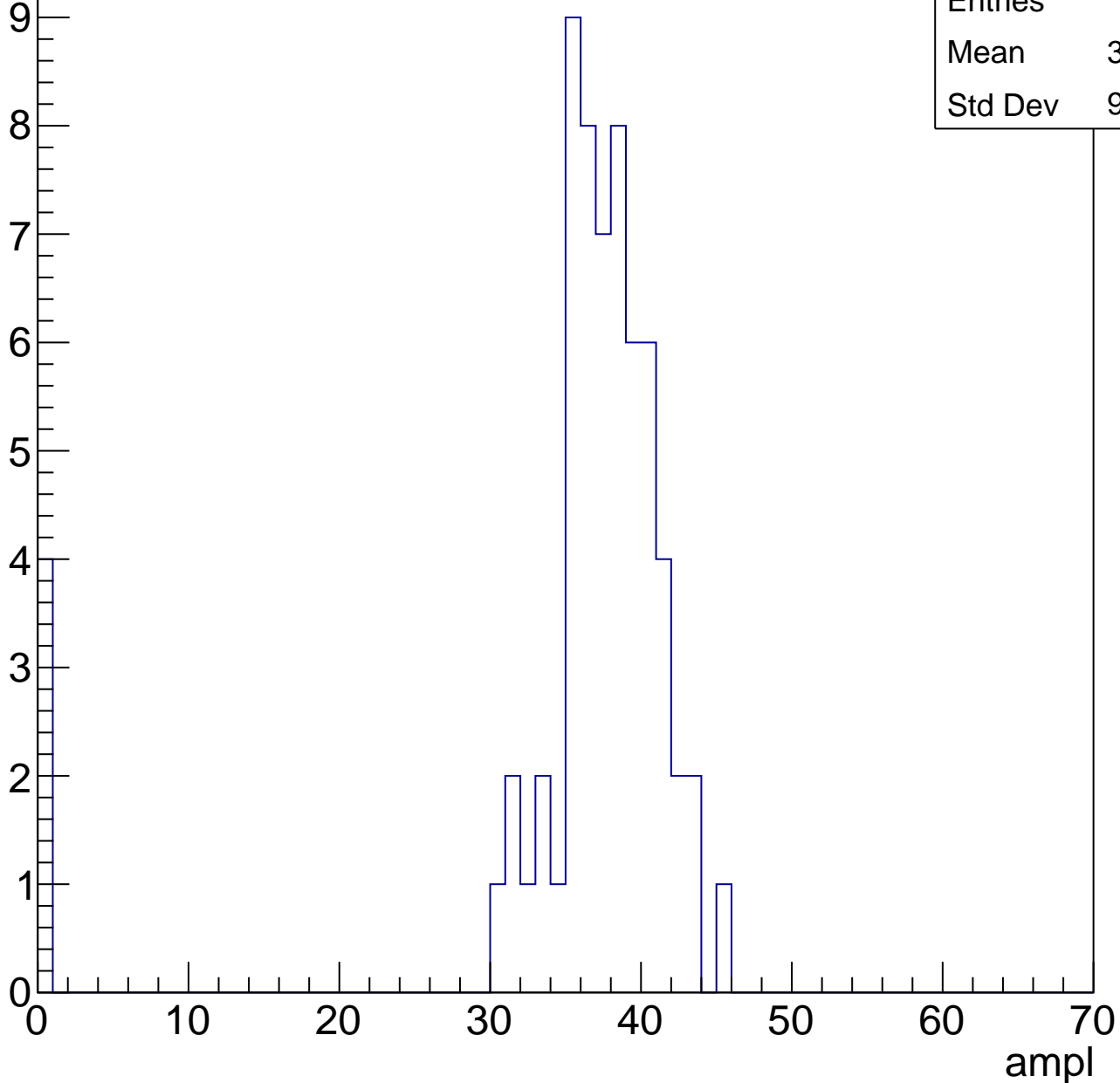


B1L103S, U11-ch55, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	35.05
Std Dev	9.519

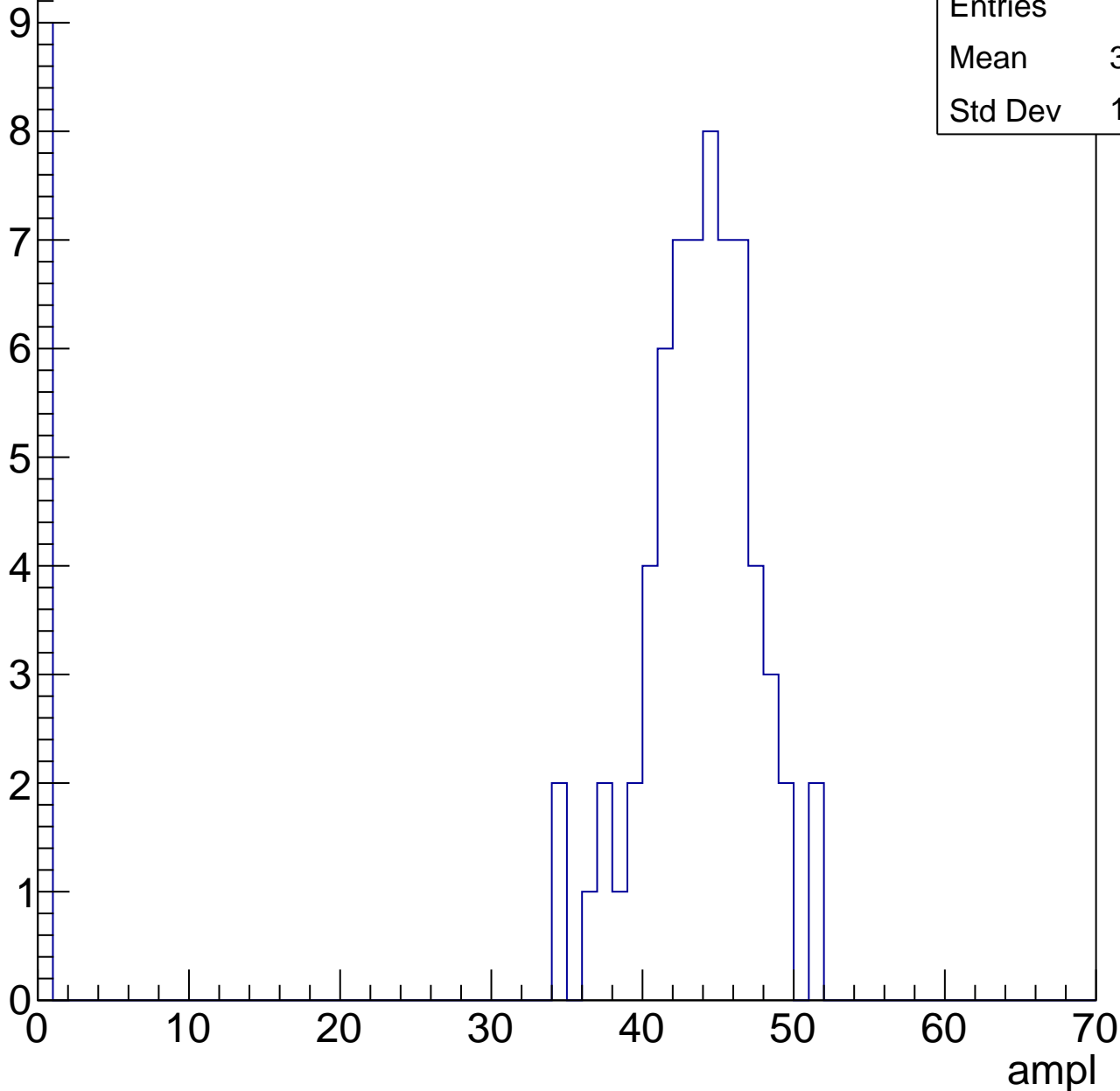


B1L103S, U11-ch55, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	38.05
Std Dev	14.55



B1L103S, U11-ch55, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	50.66
Std Dev	3.482

Entry

10

8

6

4

2

0

0

10

20

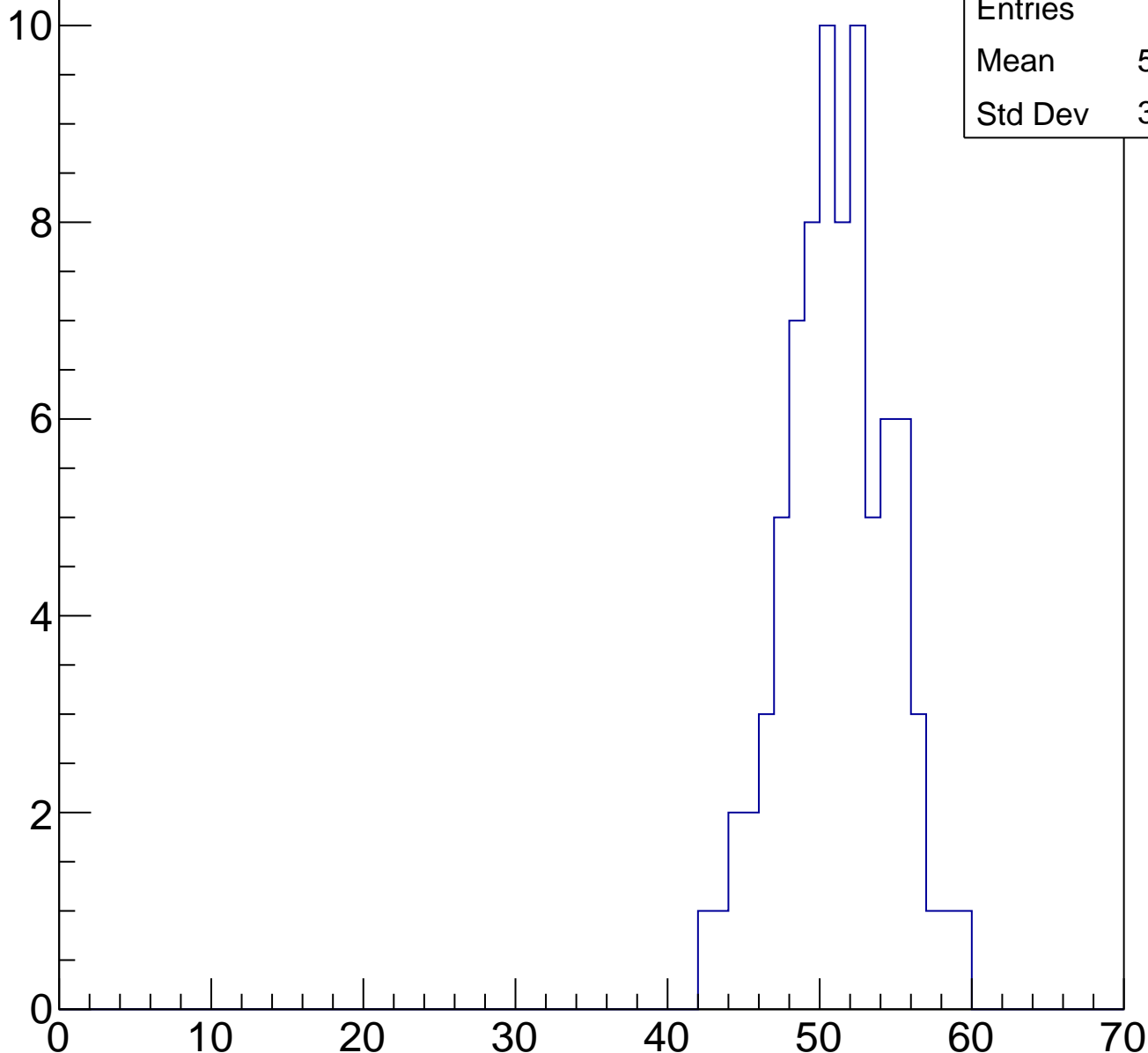
30

40

50

60

ampl

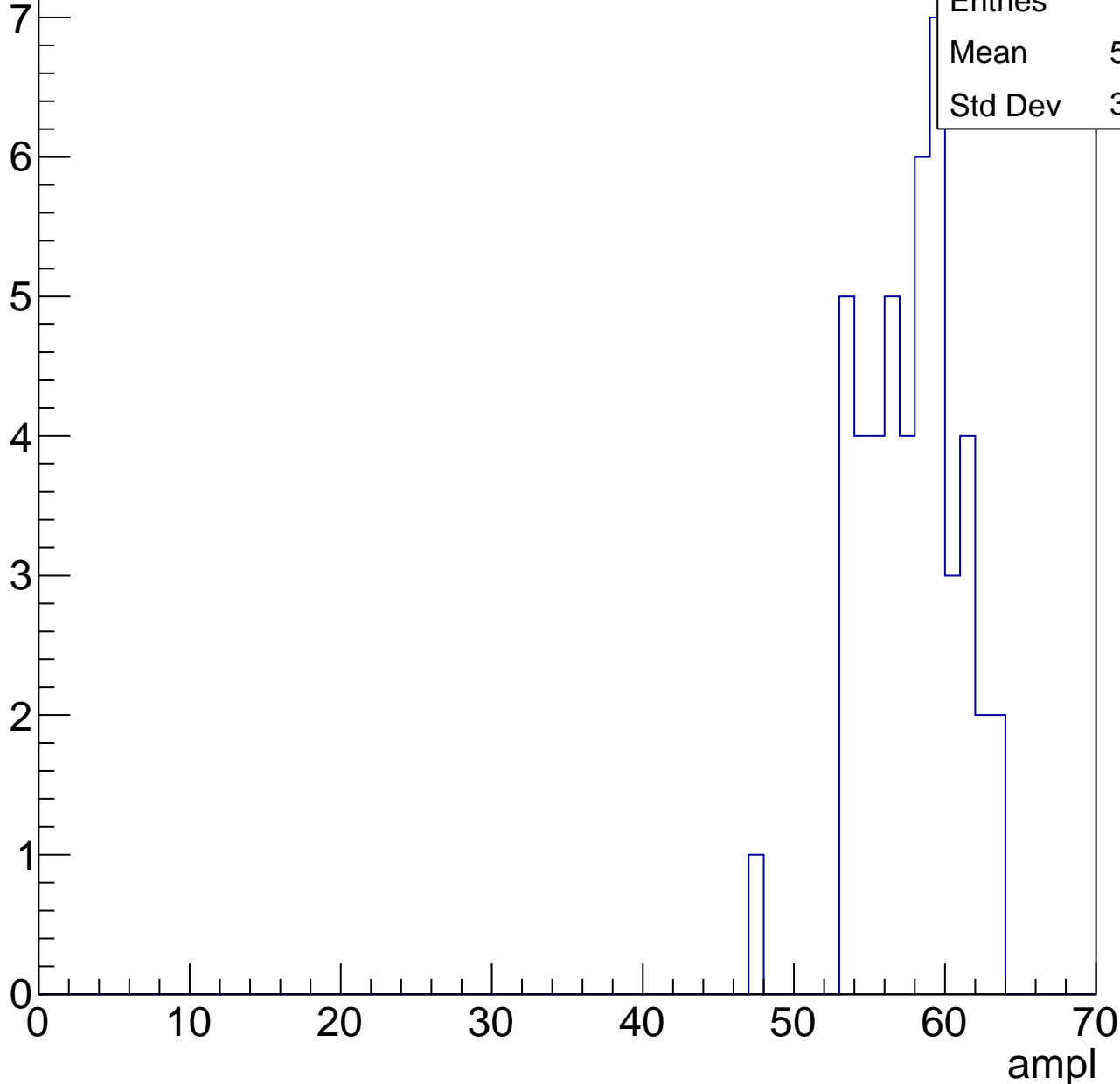


B1L103S, U11-ch55, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	47
Mean	57.26
Std Dev	3.199

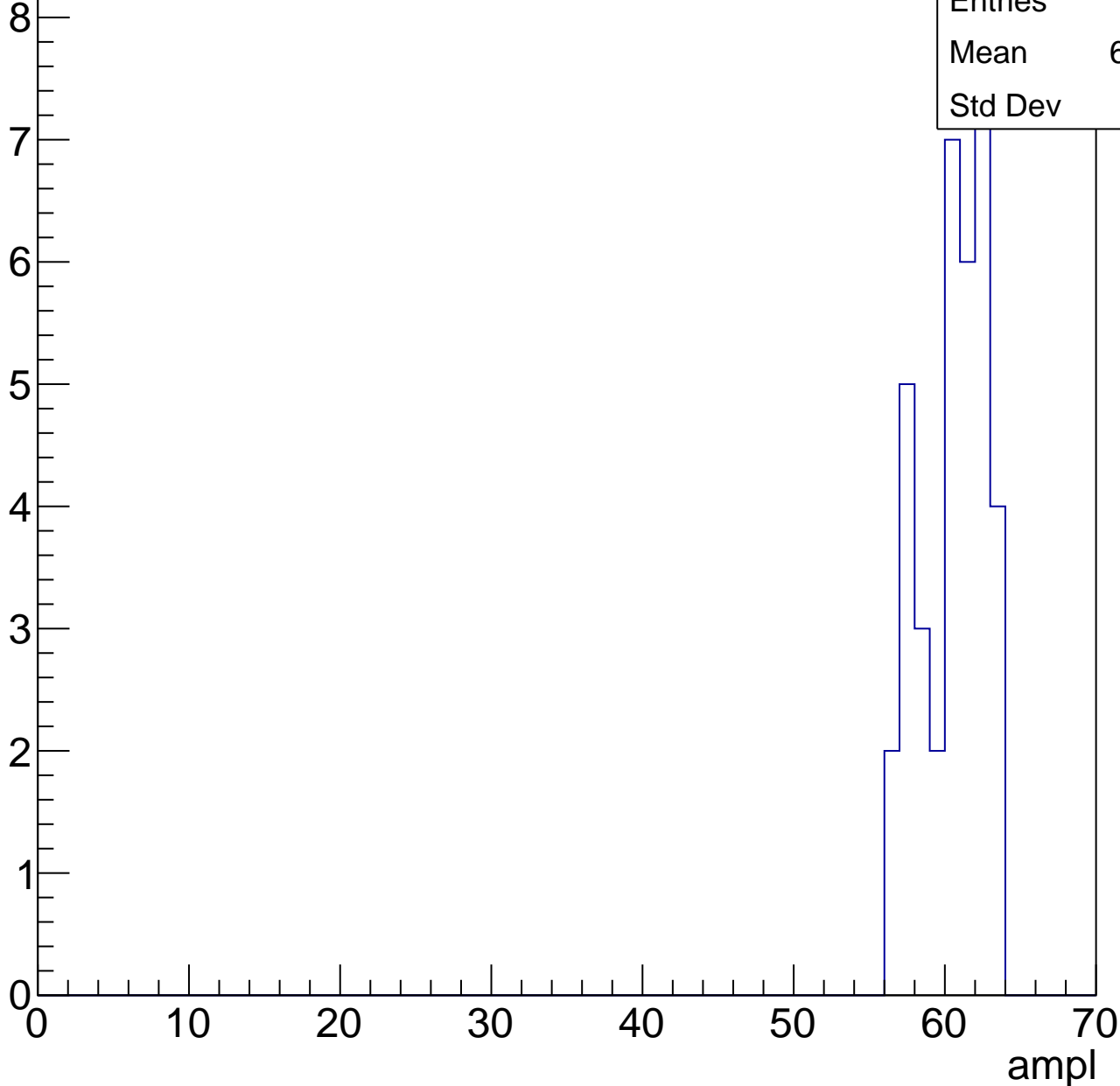


B1L103S, U11-ch55, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

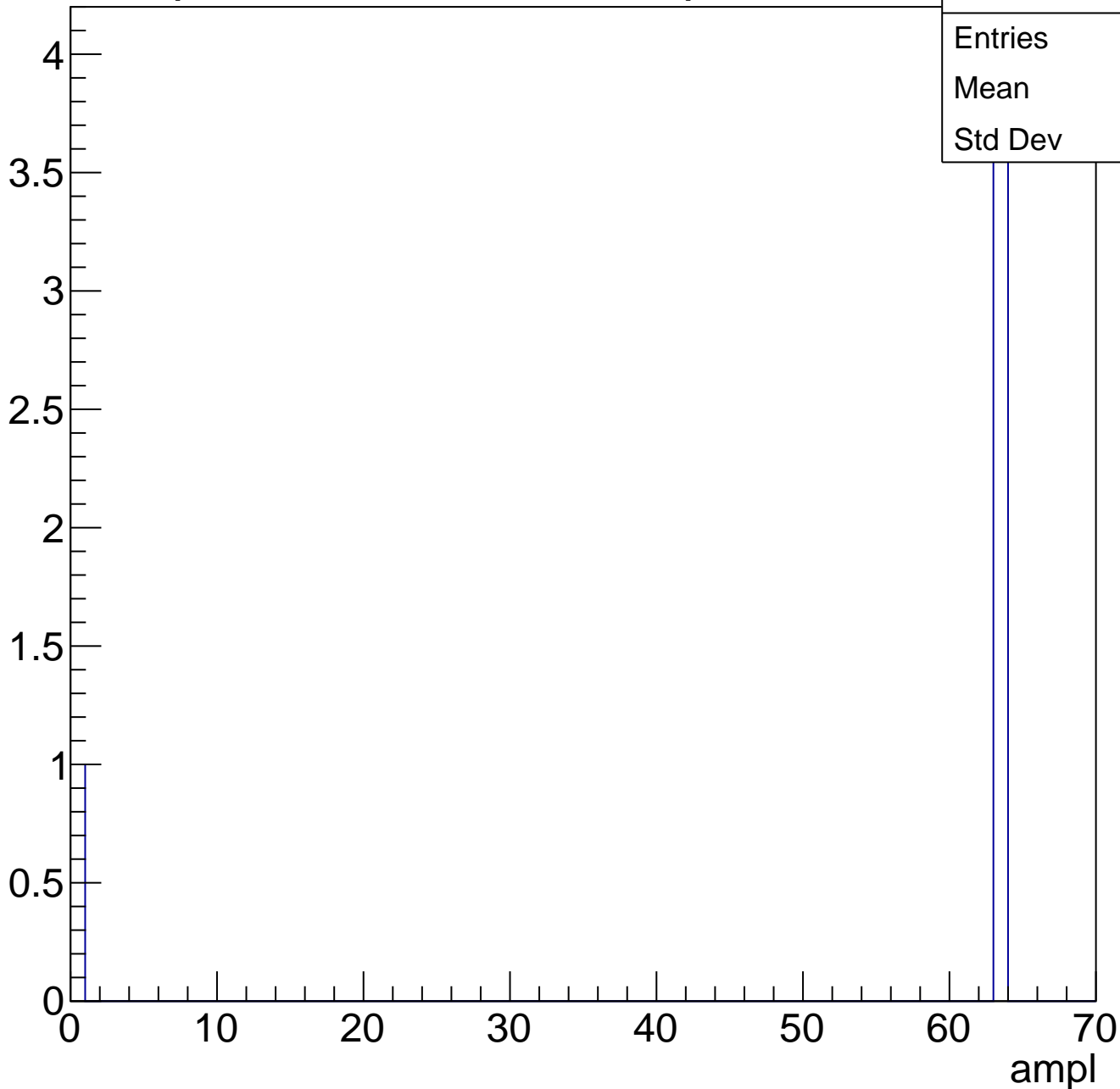
Entries	37
Mean	60.08
Std Dev	2.11



B1L103S, U11-ch55, adc6

calib_packv5_041523_1651.root, FC#0, port C2

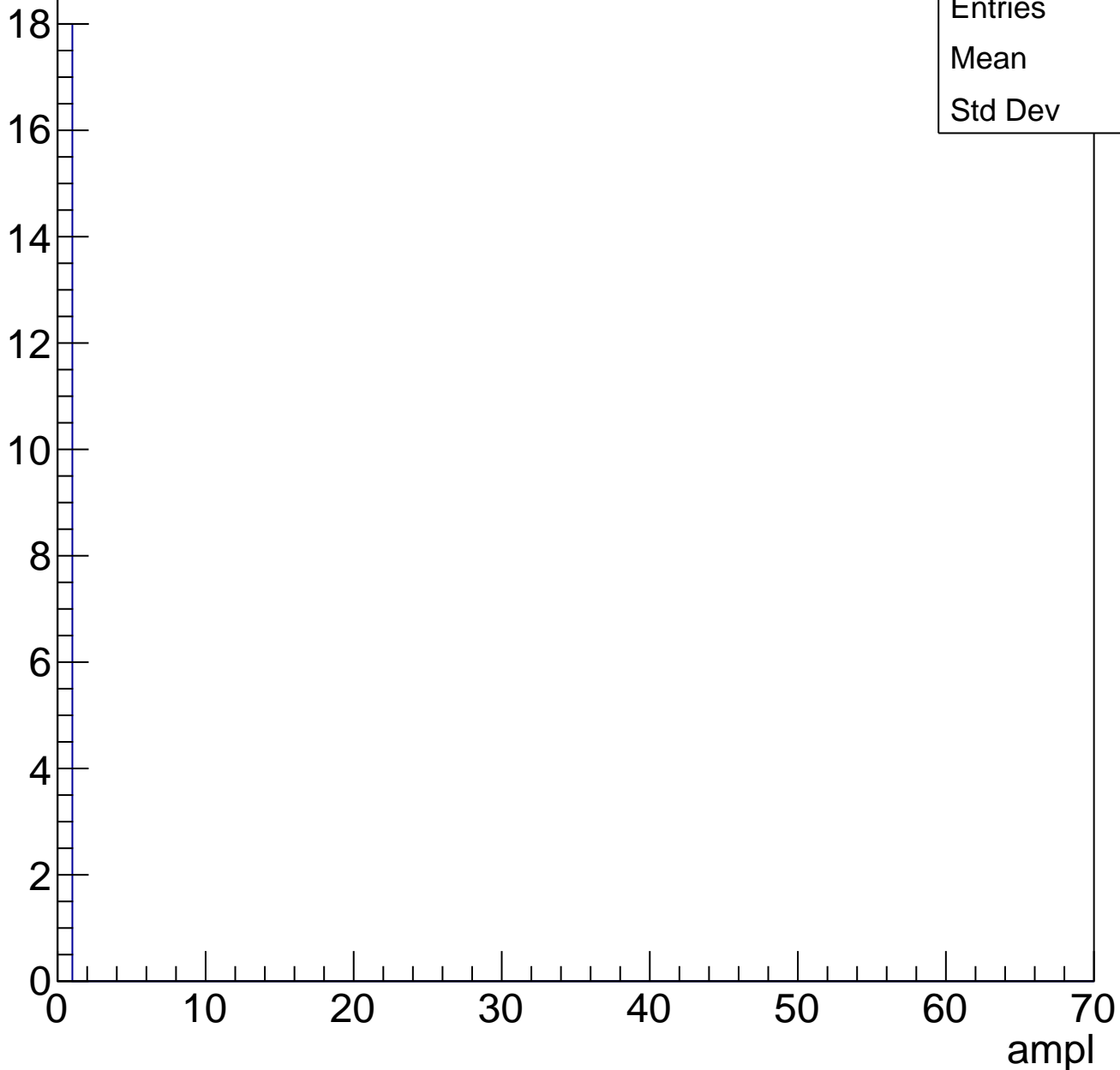
Entry



B1L103S, U11-ch55, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch56, adc0

calib_packv5_041523_1651.root, FC#0, port C2

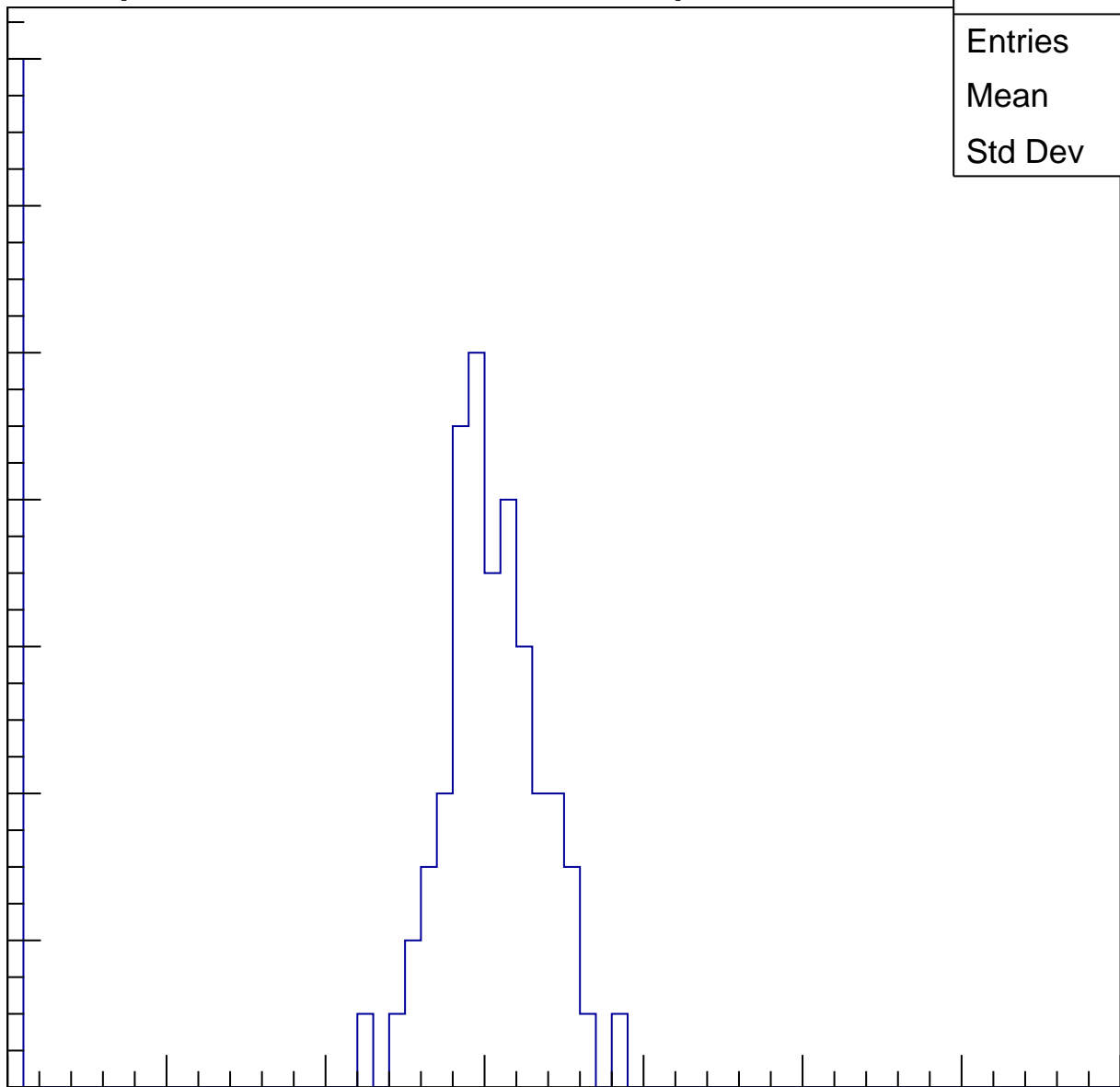
Entries	78
Mean	24.63
Std Dev	11.84

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

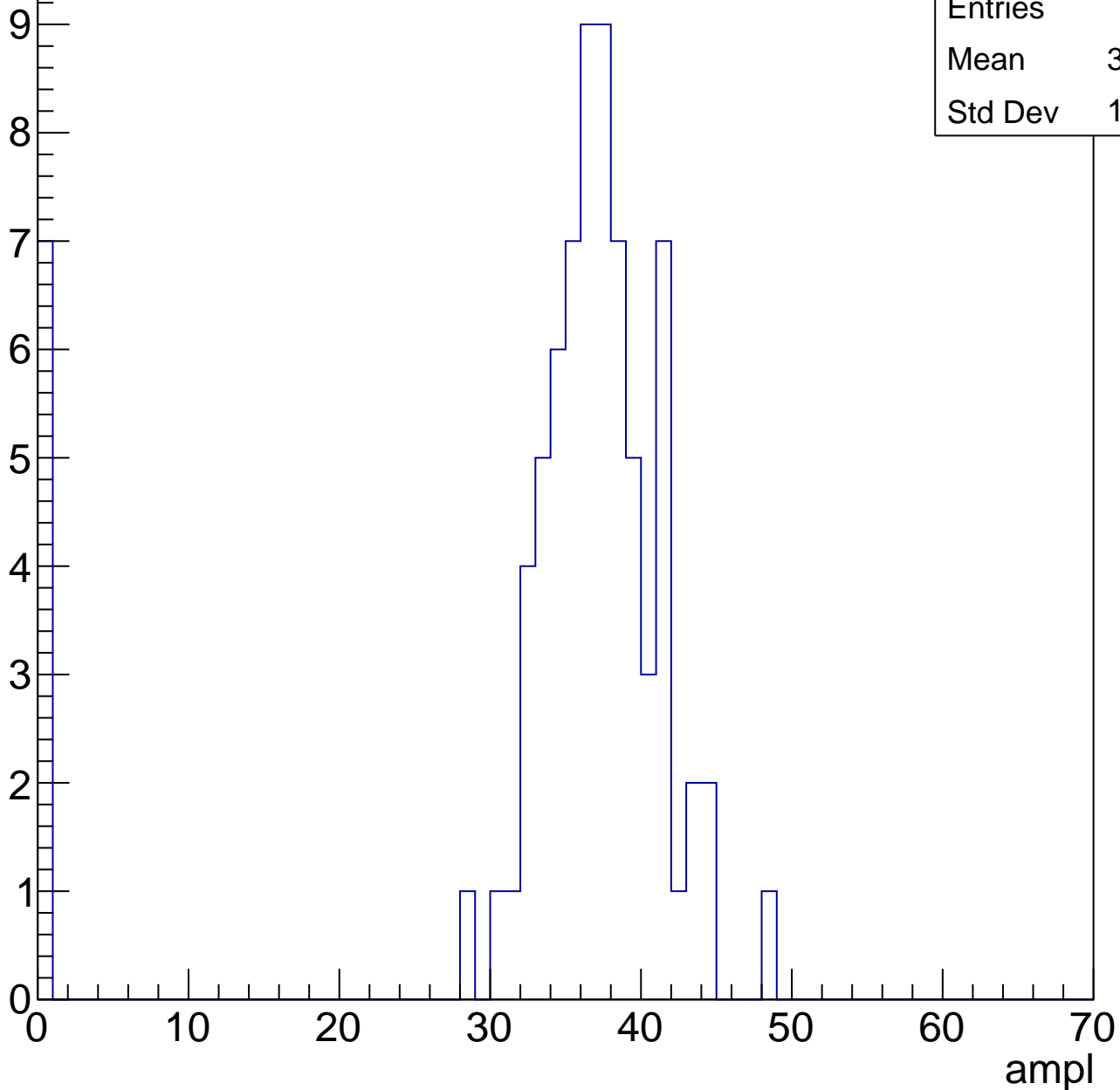


B1L103S, U11-ch56, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	33.59
Std Dev	11.09

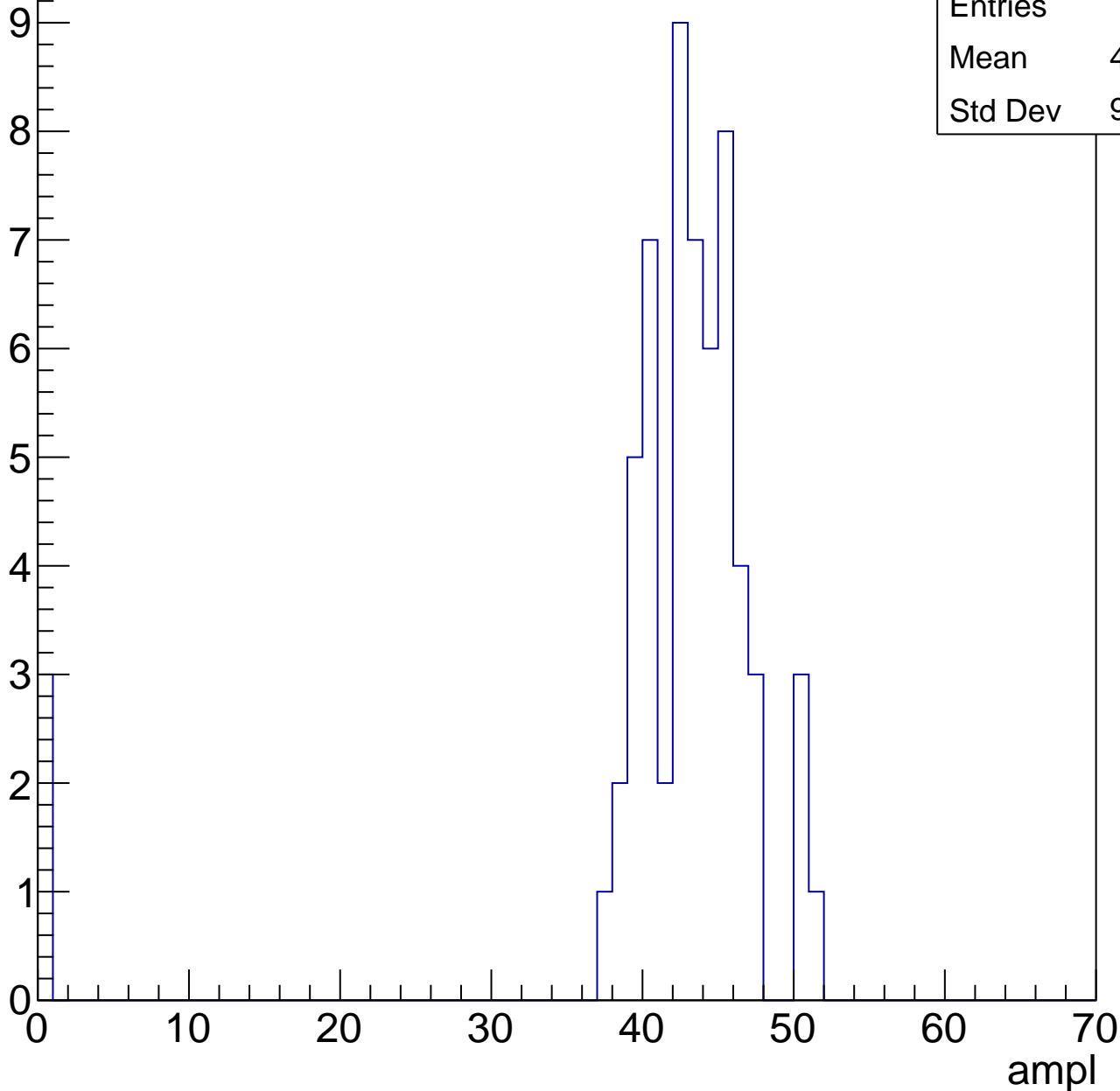


B1L103S, U11-ch56, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	40.97
Std Dev	9.813

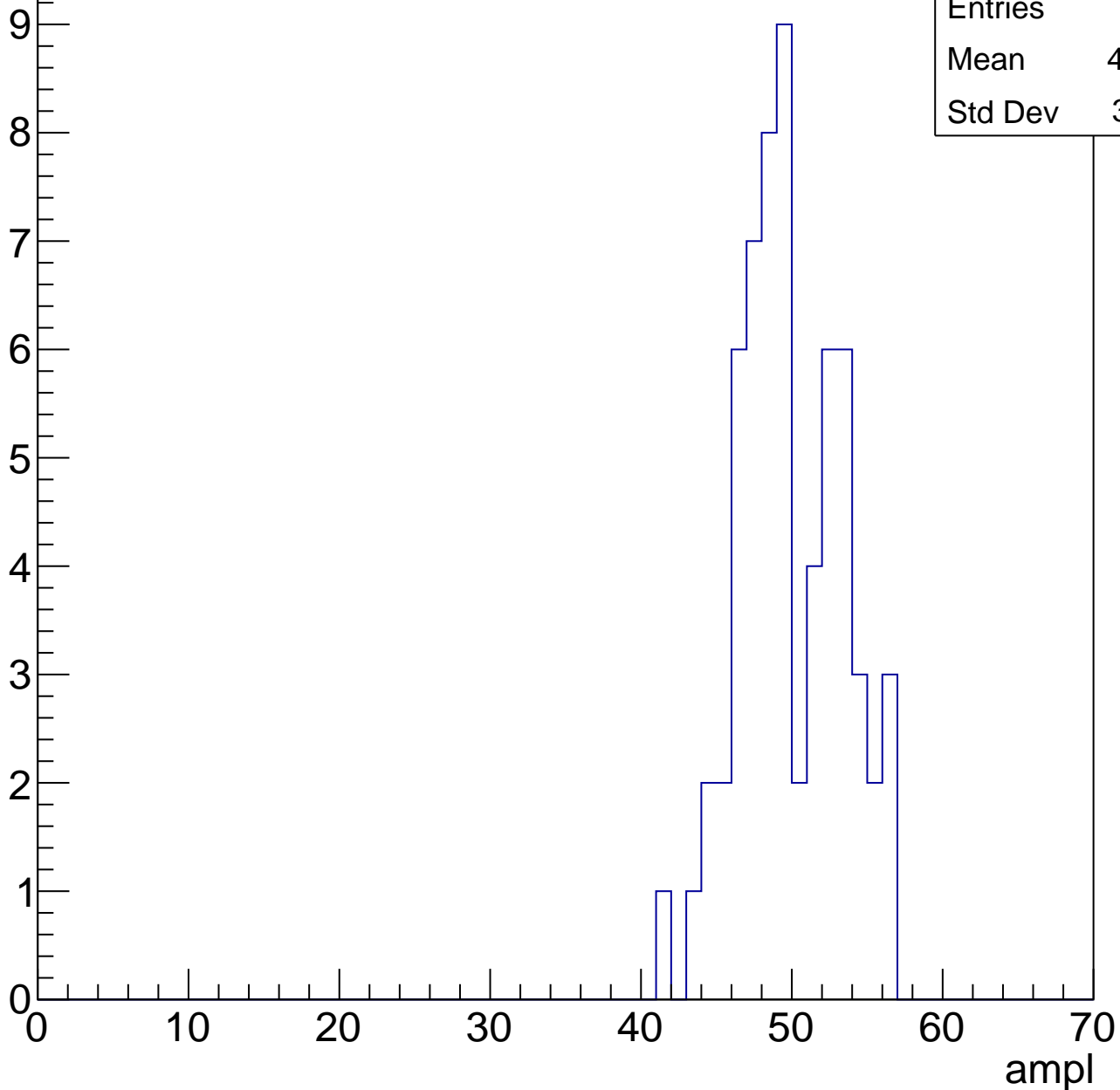


B1L103S, U11-ch56, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	49.45
Std Dev	3.411

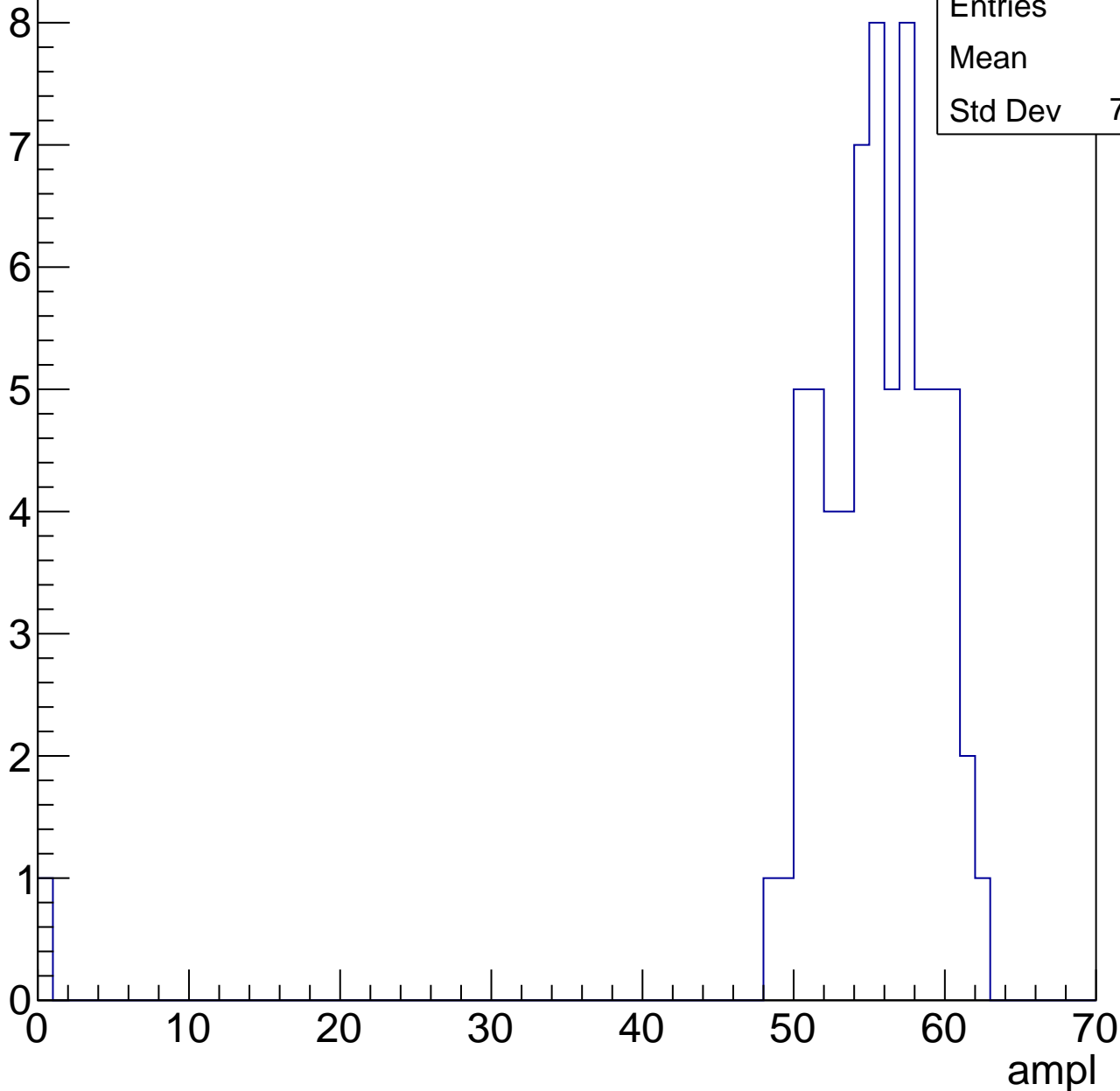


B1L103S, U11-ch56, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	54.4
Std Dev	7.489

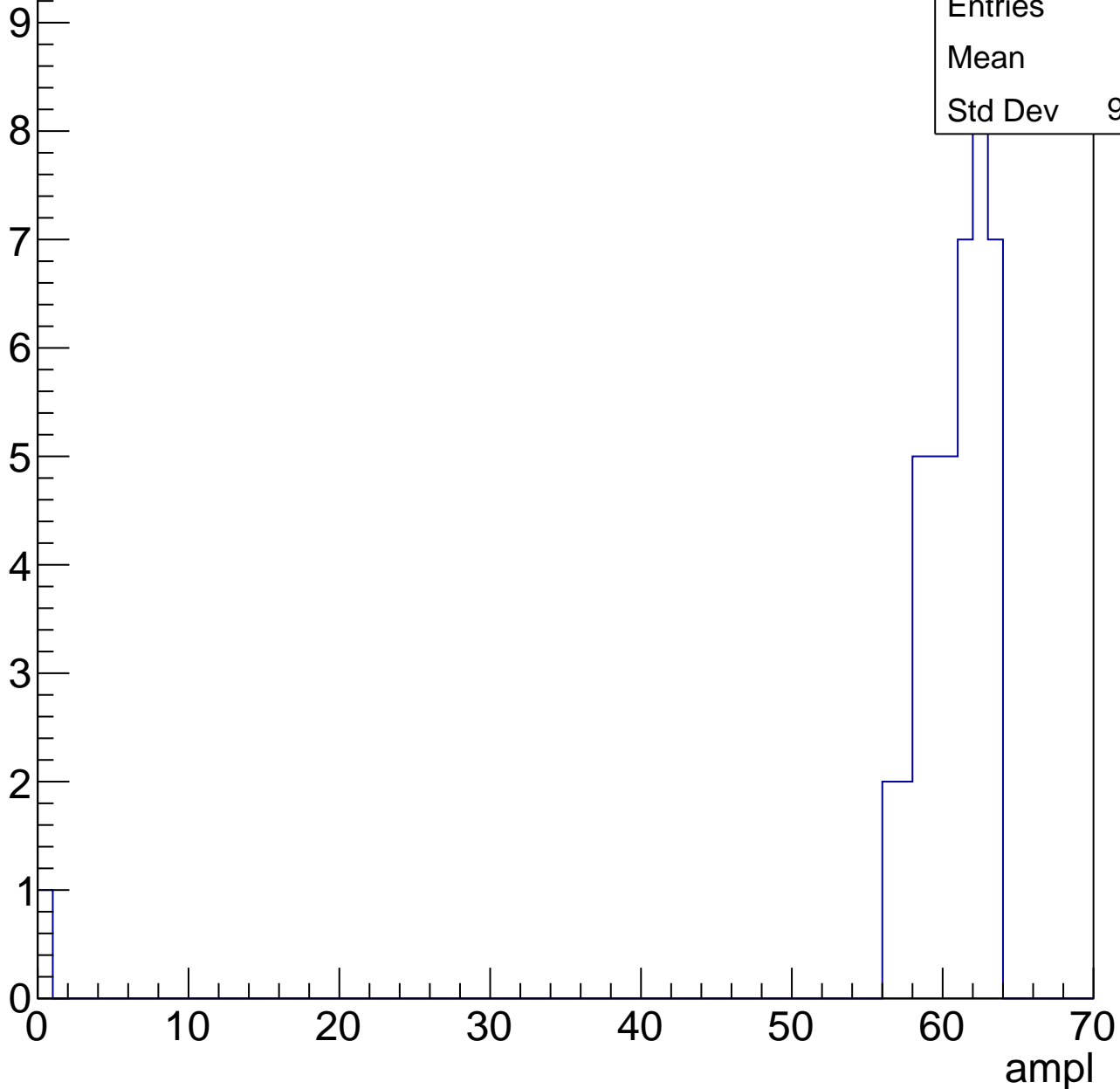


B1L103S, U11-ch56, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	43
Mean	59
Std Dev	9.324



B1L103S, U11-ch56, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch56, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

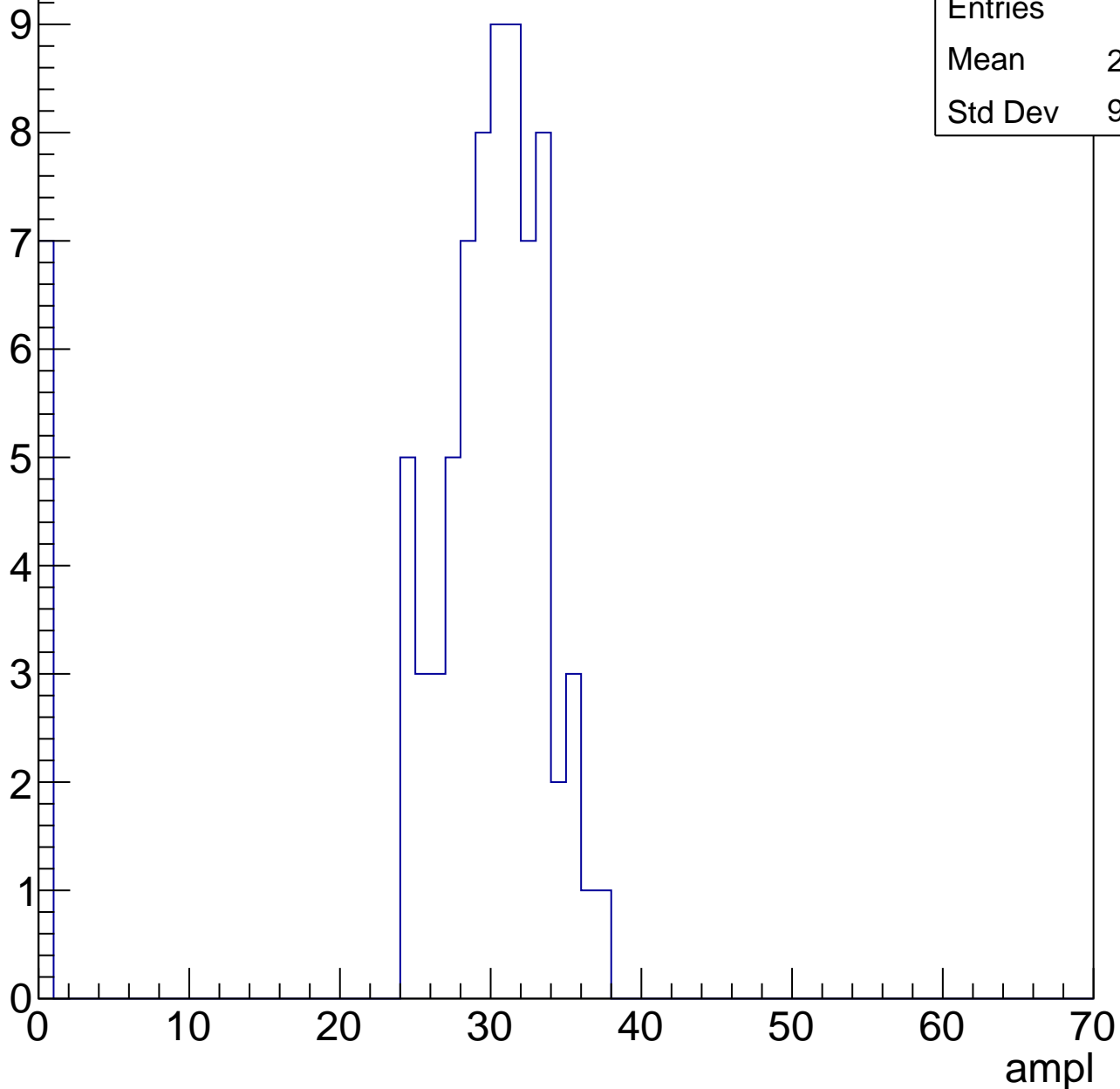
Entries	19
Mean	0
Std Dev	0

B1L103S, U11-ch57, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	27.17
Std Dev	9.029



B1L103S, U11-ch57, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	83
Mean	32.33
Std Dev	12.95

Entry

10

8

6

4

2

0

0

10

20

30

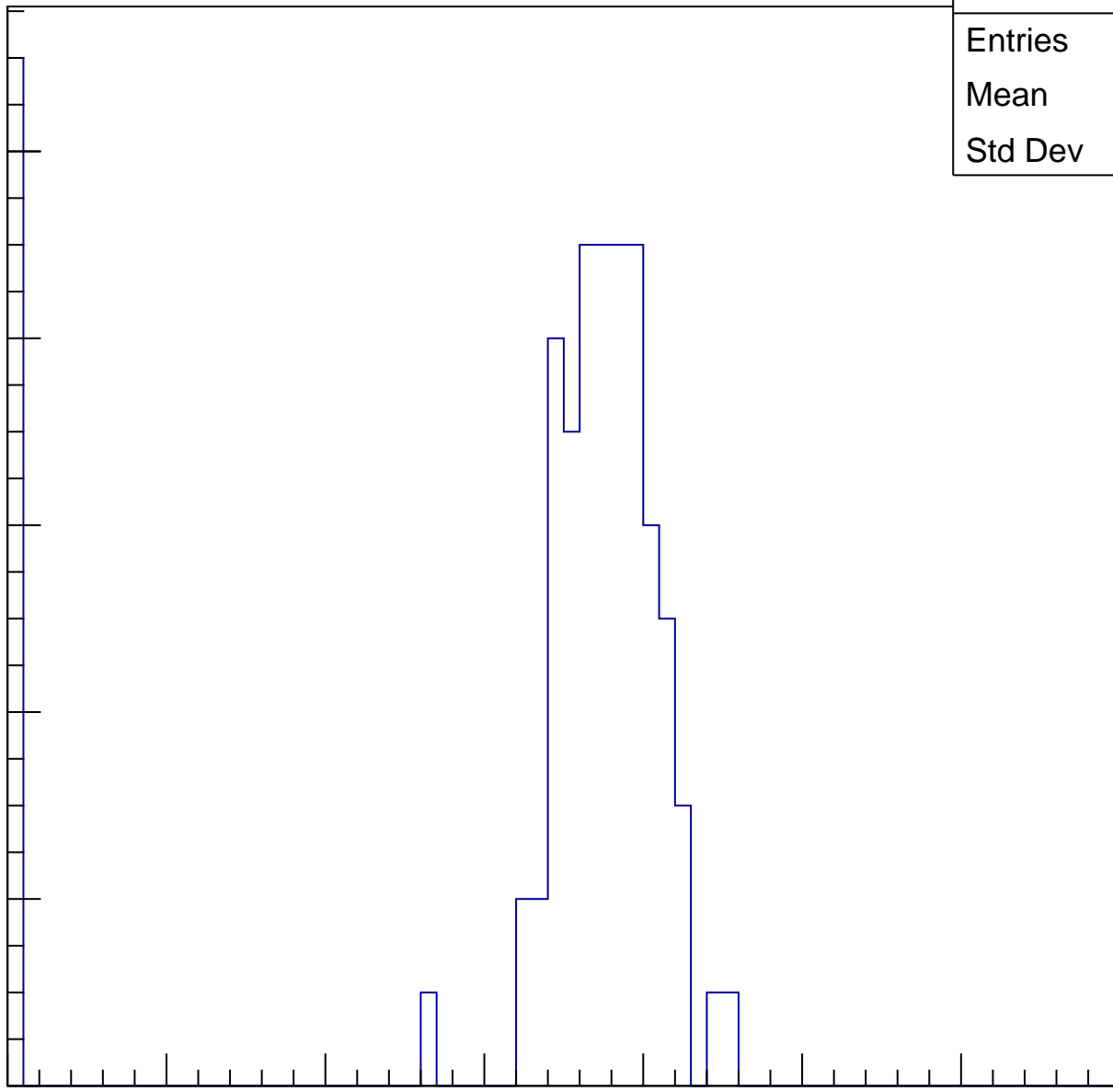
40

50

60

70

ampl

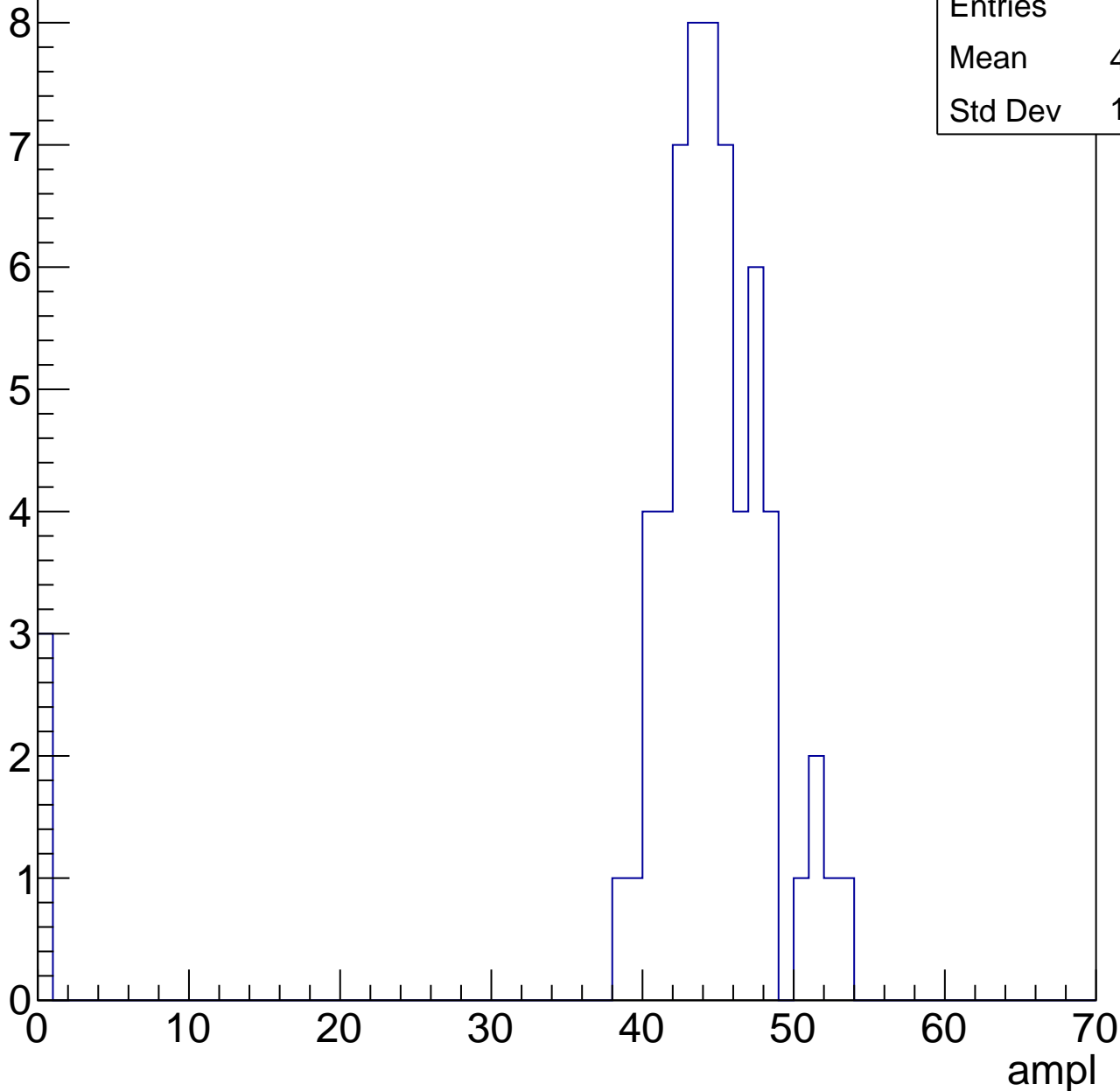


B1L103S, U11-ch57, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	42.27
Std Dev	10.03

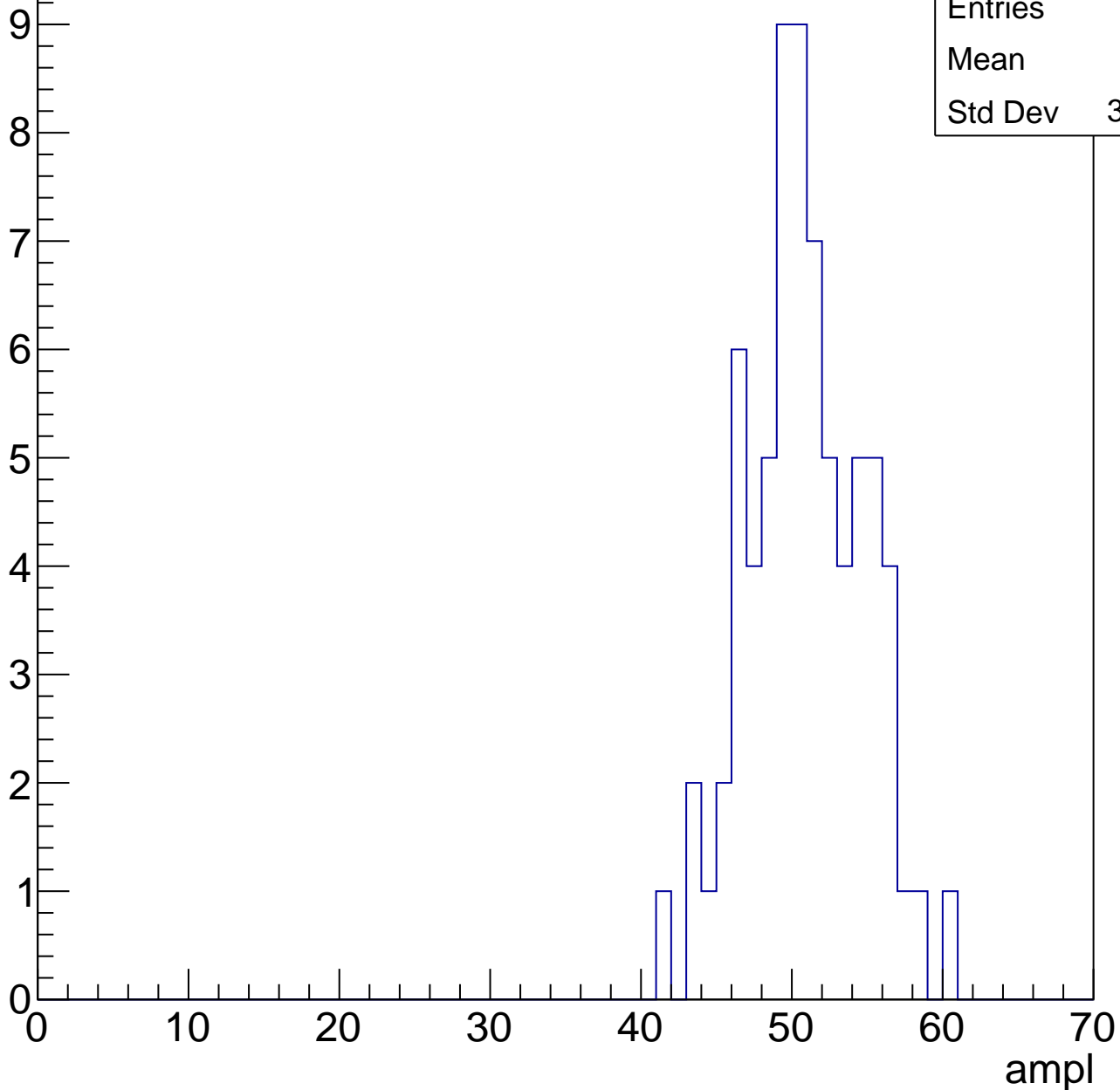


B1L103S, U11-ch57, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	50.4
Std Dev	3.799

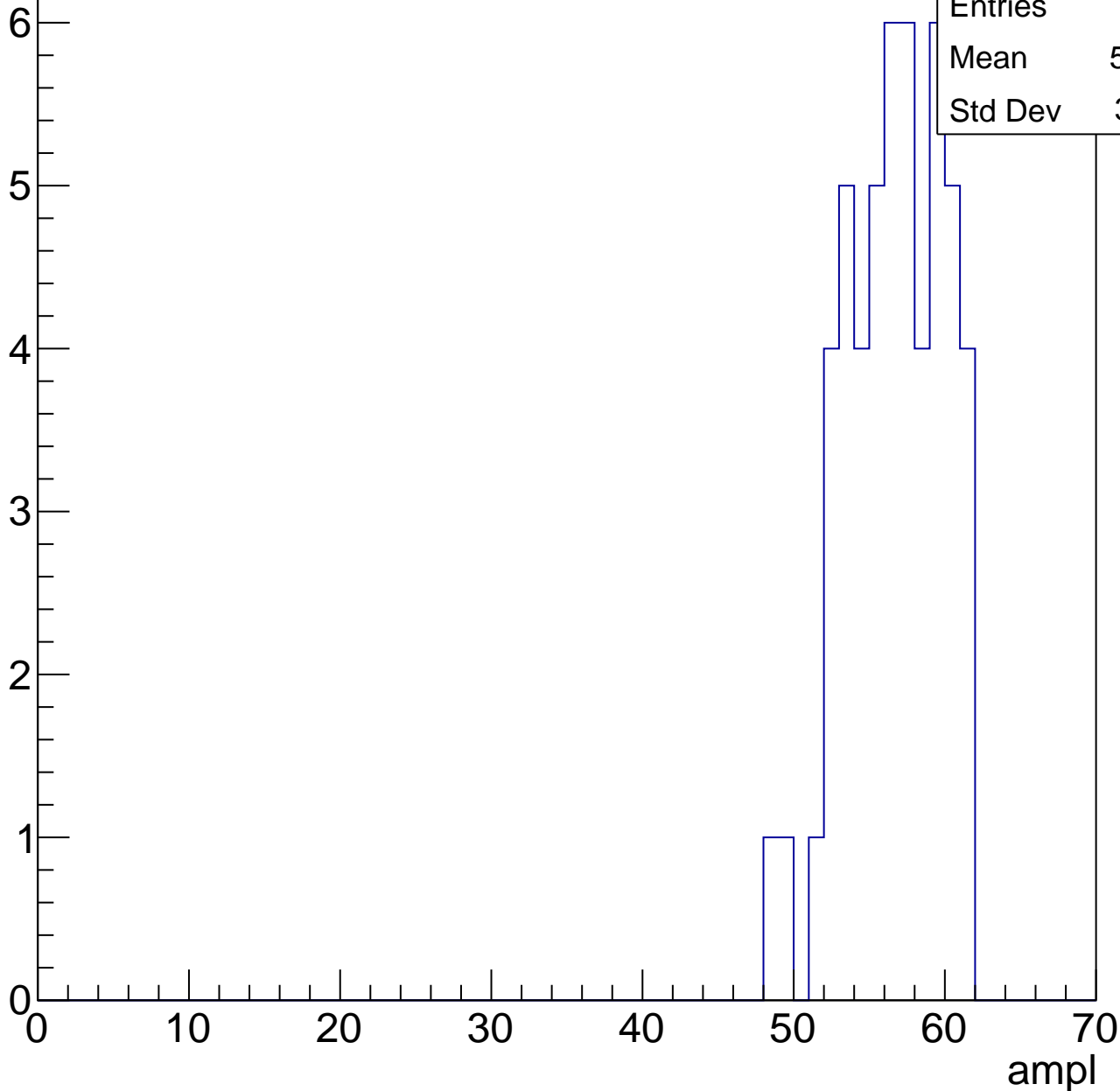


B1L103S, U11-ch57, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	56.15
Std Dev	3.171



B1L103S, U11-ch57, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entries	43
Mean	59.16
Std Dev	9.381

Entry

10

8

6

4

2

0

0

10

20

30

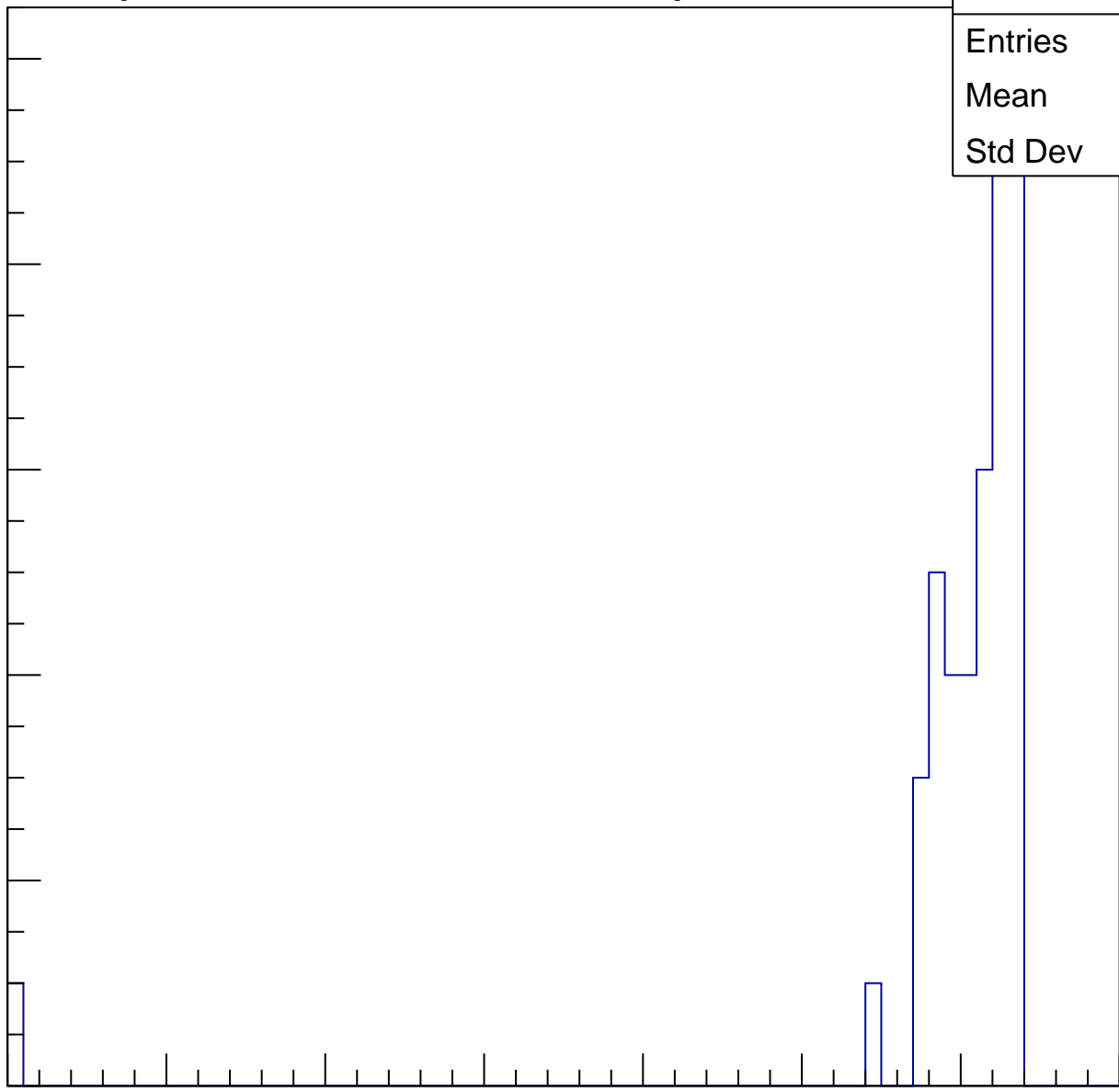
40

50

60

ampl

70



B1L103S, U11-ch57, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch57, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

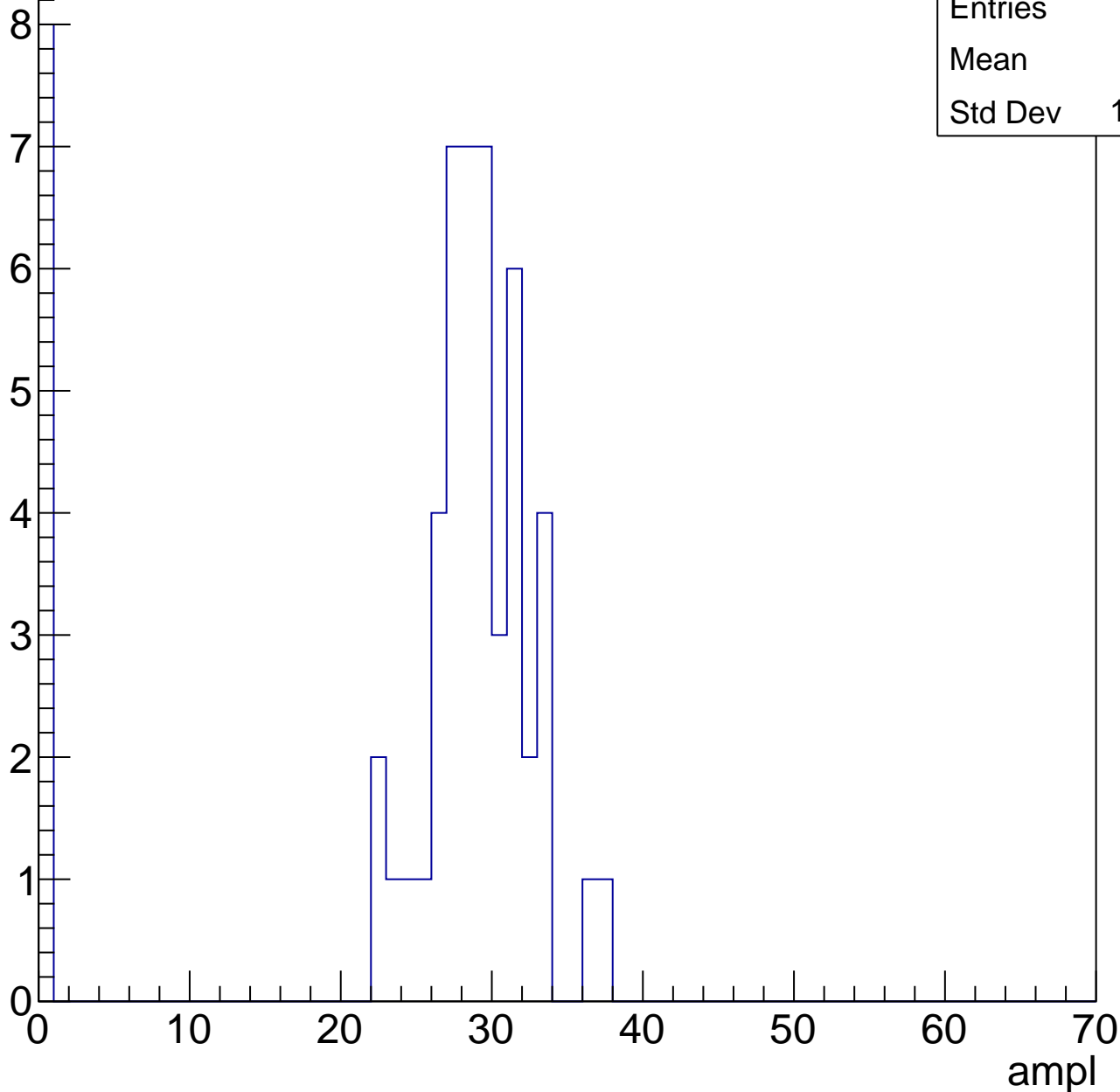
Entries	19
Mean	0
Std Dev	0

B1L103S, U11-ch58, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	24.6
Std Dev	10.56

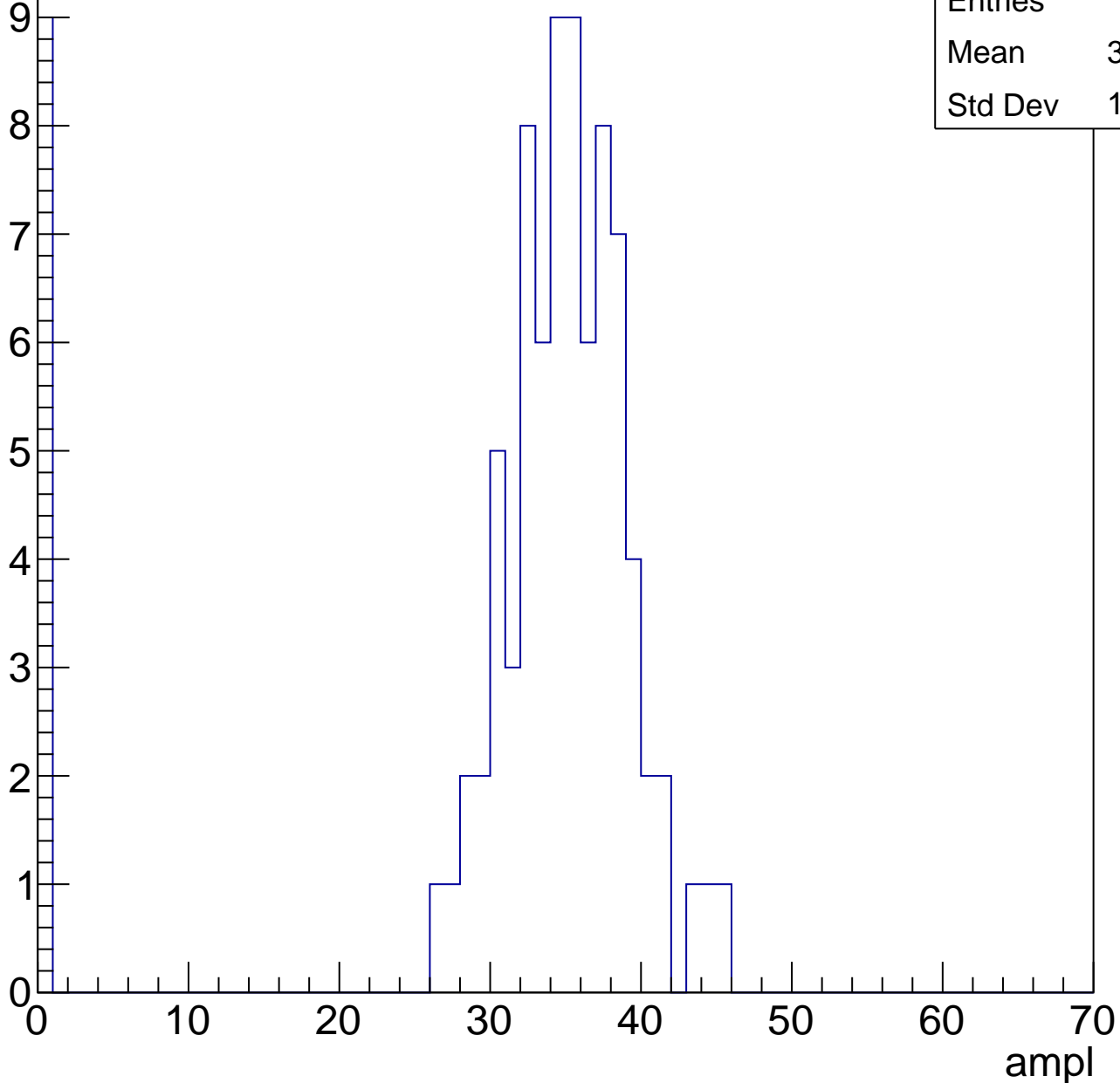


B1L103S, U11-ch58, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	87
Mean	31.18
Std Dev	11.18

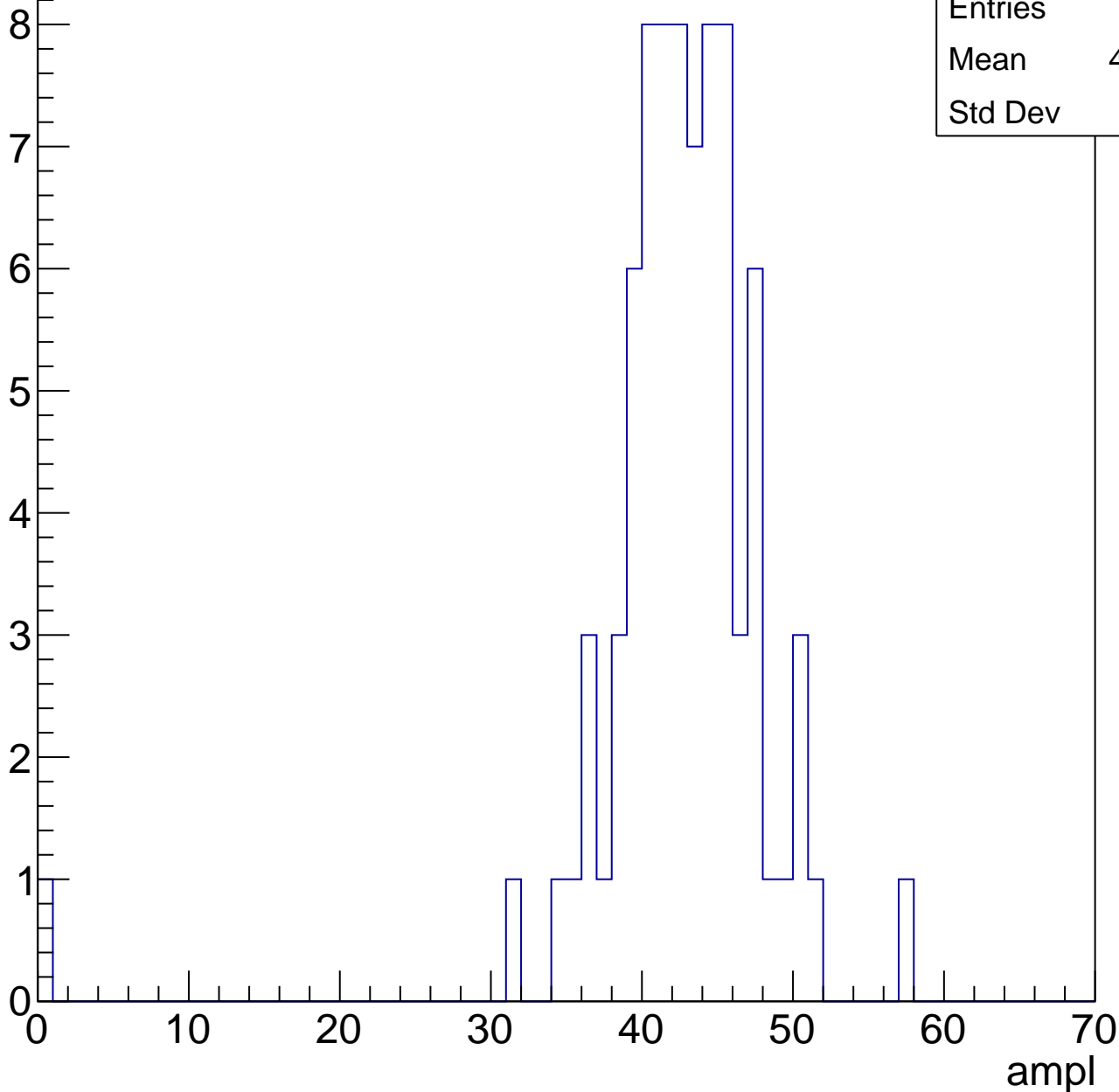


B1L103S, U11-ch58, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	80
Mean	42.06
Std Dev	6.29

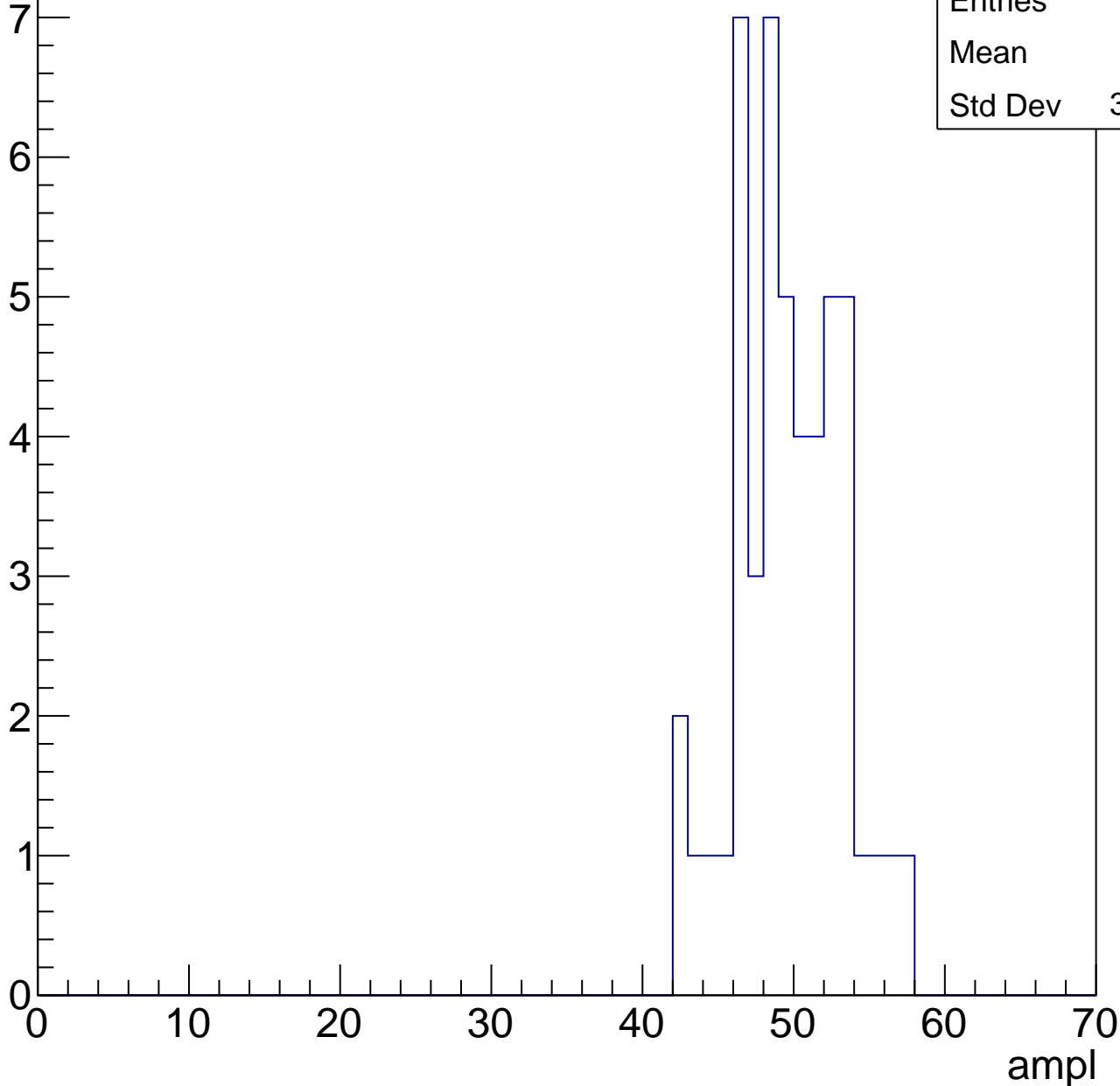


B1L103S, U11-ch58, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	49.2
Std Dev	3.422

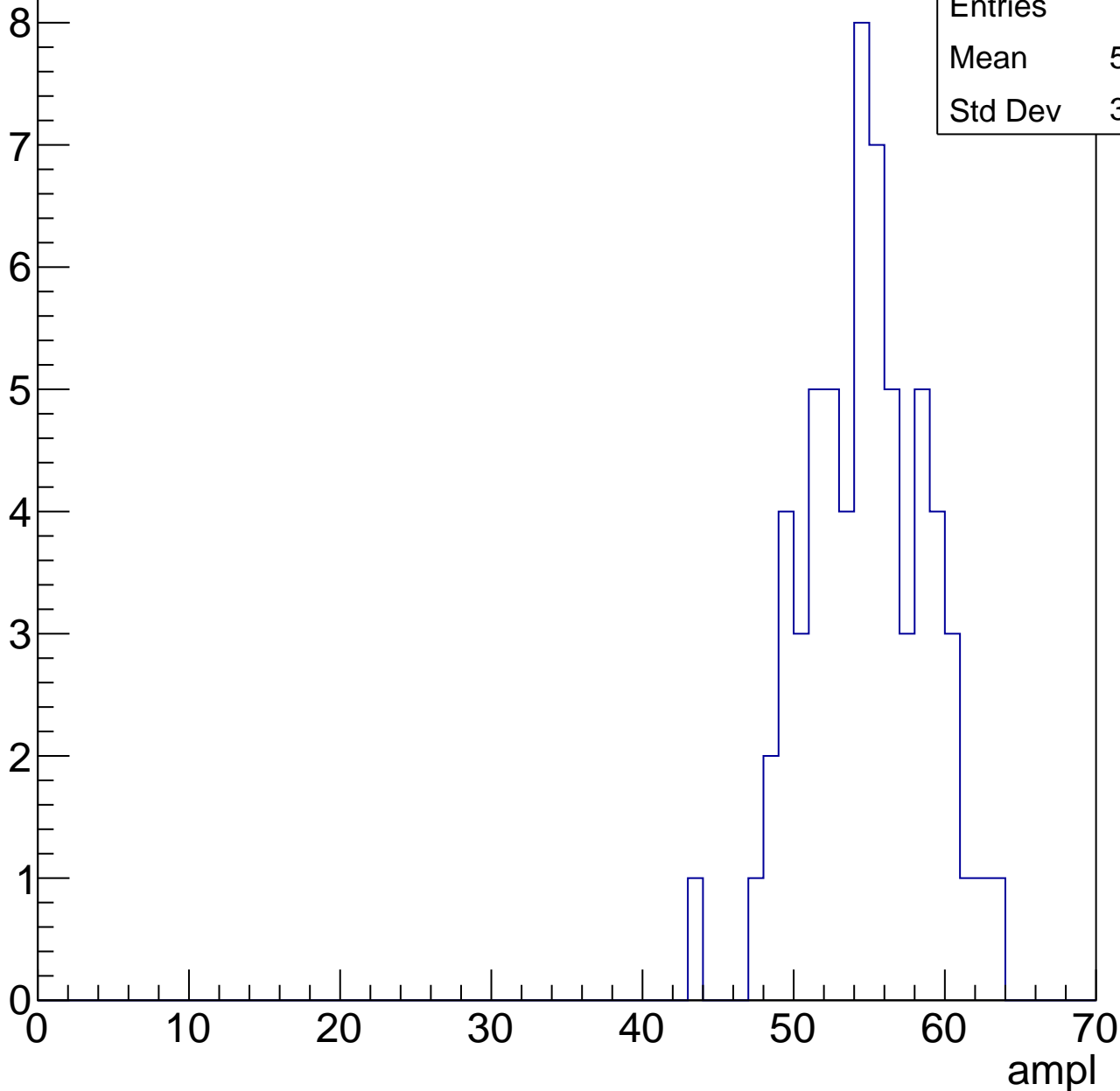


B1L103S, U11-ch58, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	54.27
Std Dev	3.965

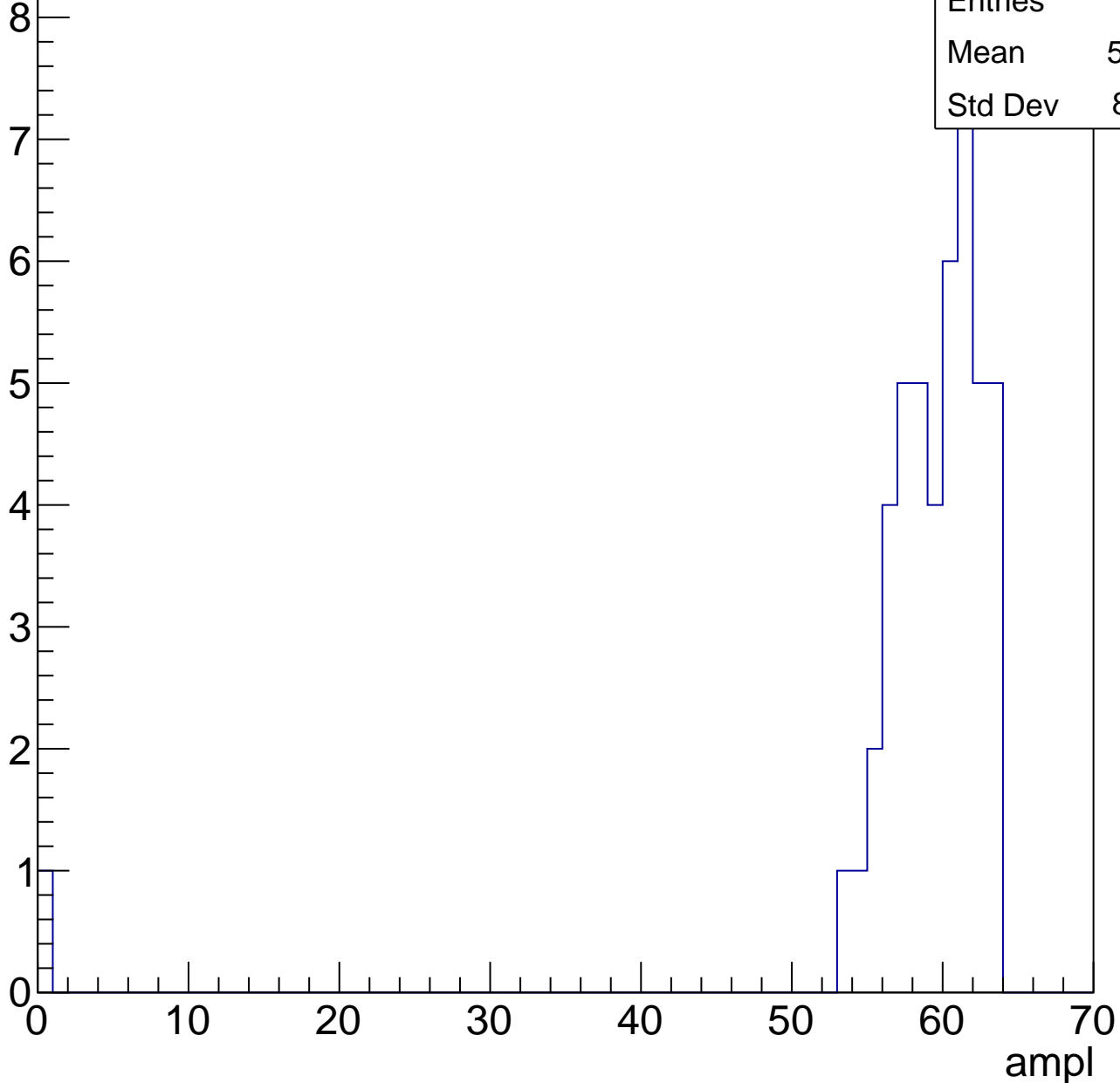


B1L103S, U11-ch58, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

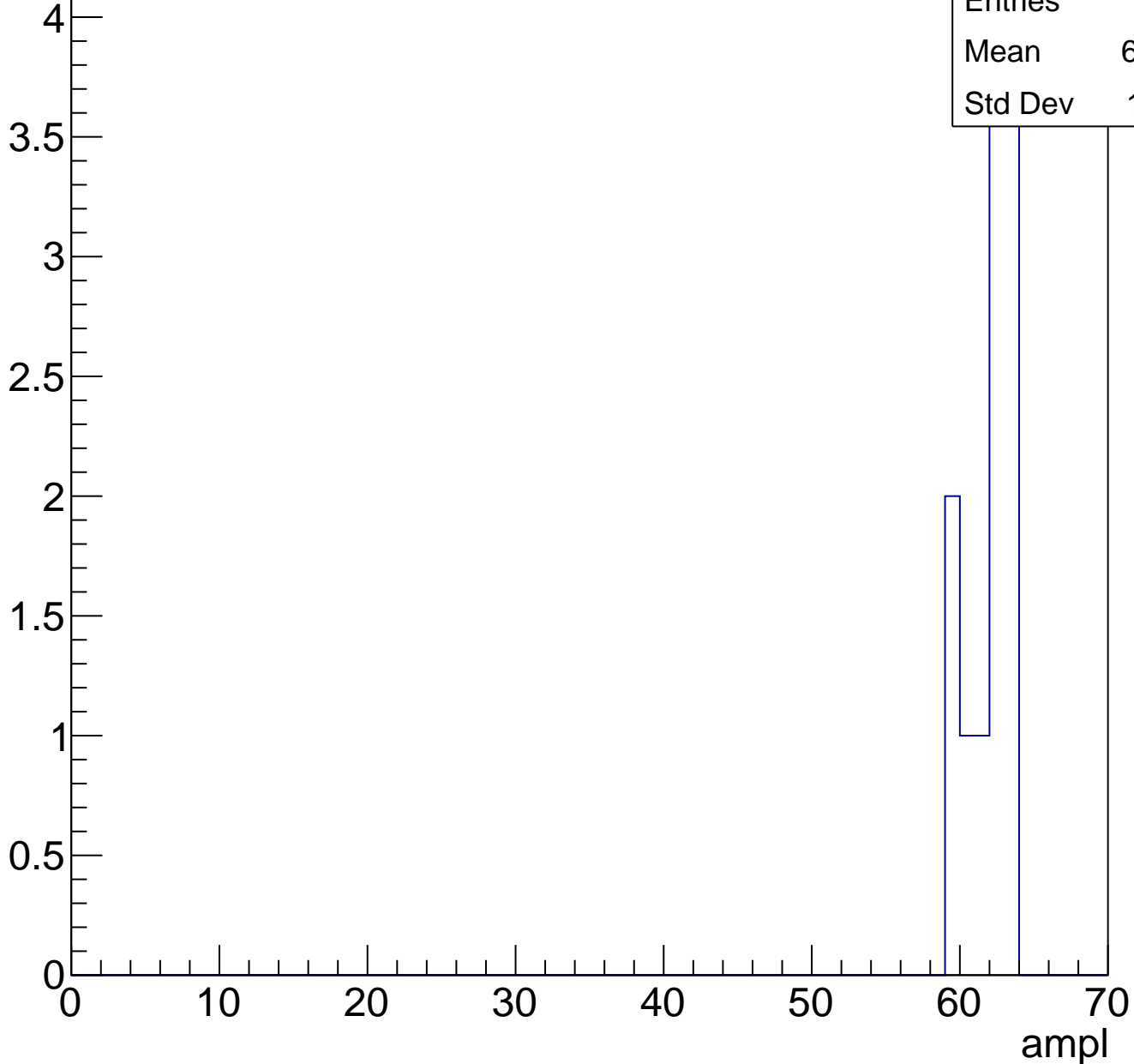
Entries	47
Mean	57.98
Std Dev	8.931



B1L103S, U11-ch58, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch58, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch59, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	72
Mean	25.38
Std Dev	11.18

Entry

10

8

6

4

2

0

0

10

20

30

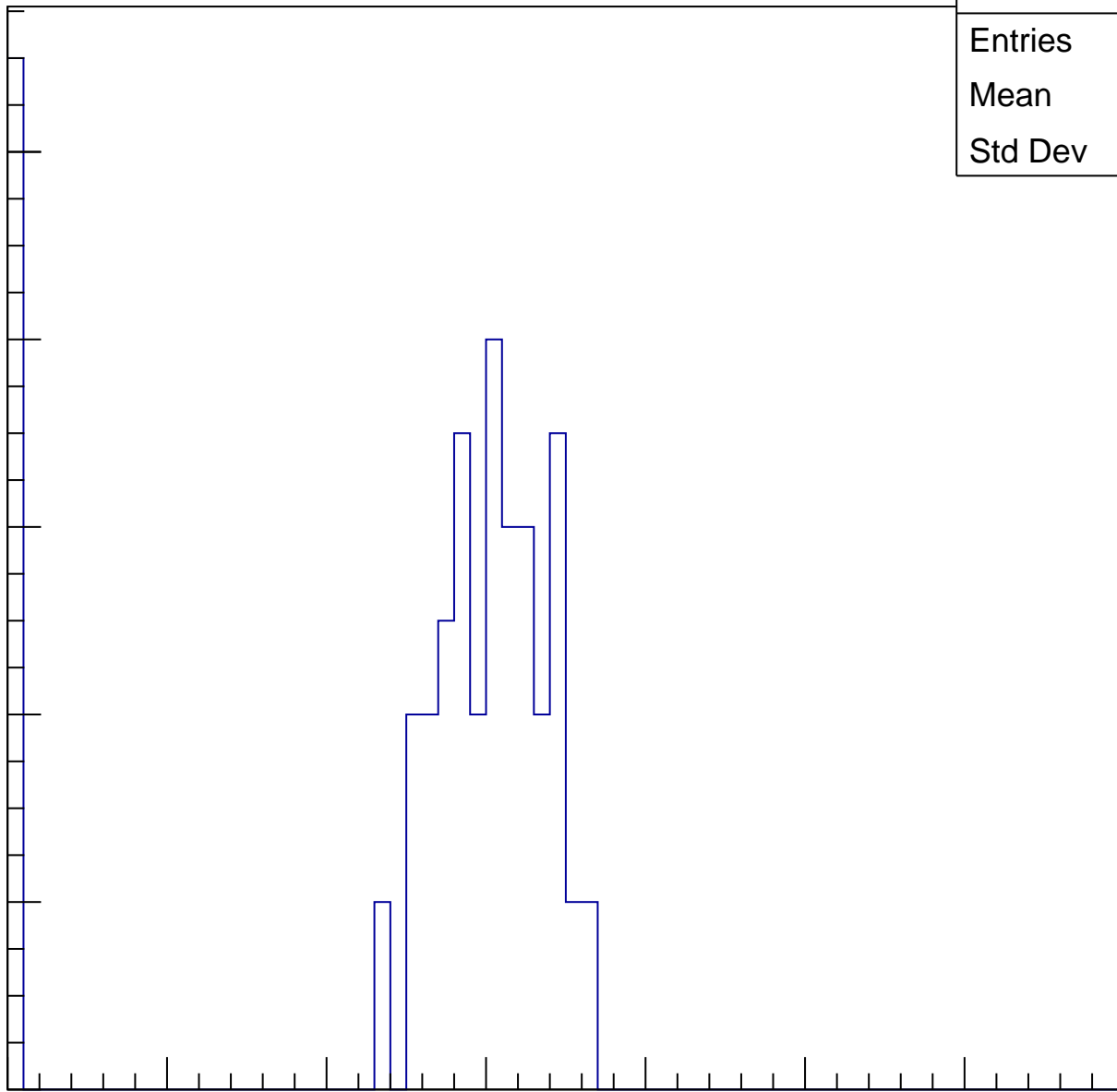
40

50

60

70

ampl



B1L103S, U11-ch59, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	83
Mean	31.29
Std Dev	12.79

Entry

10

8

6

4

2

0

0

10

20

ampl

70

50

60

40

30

20

10

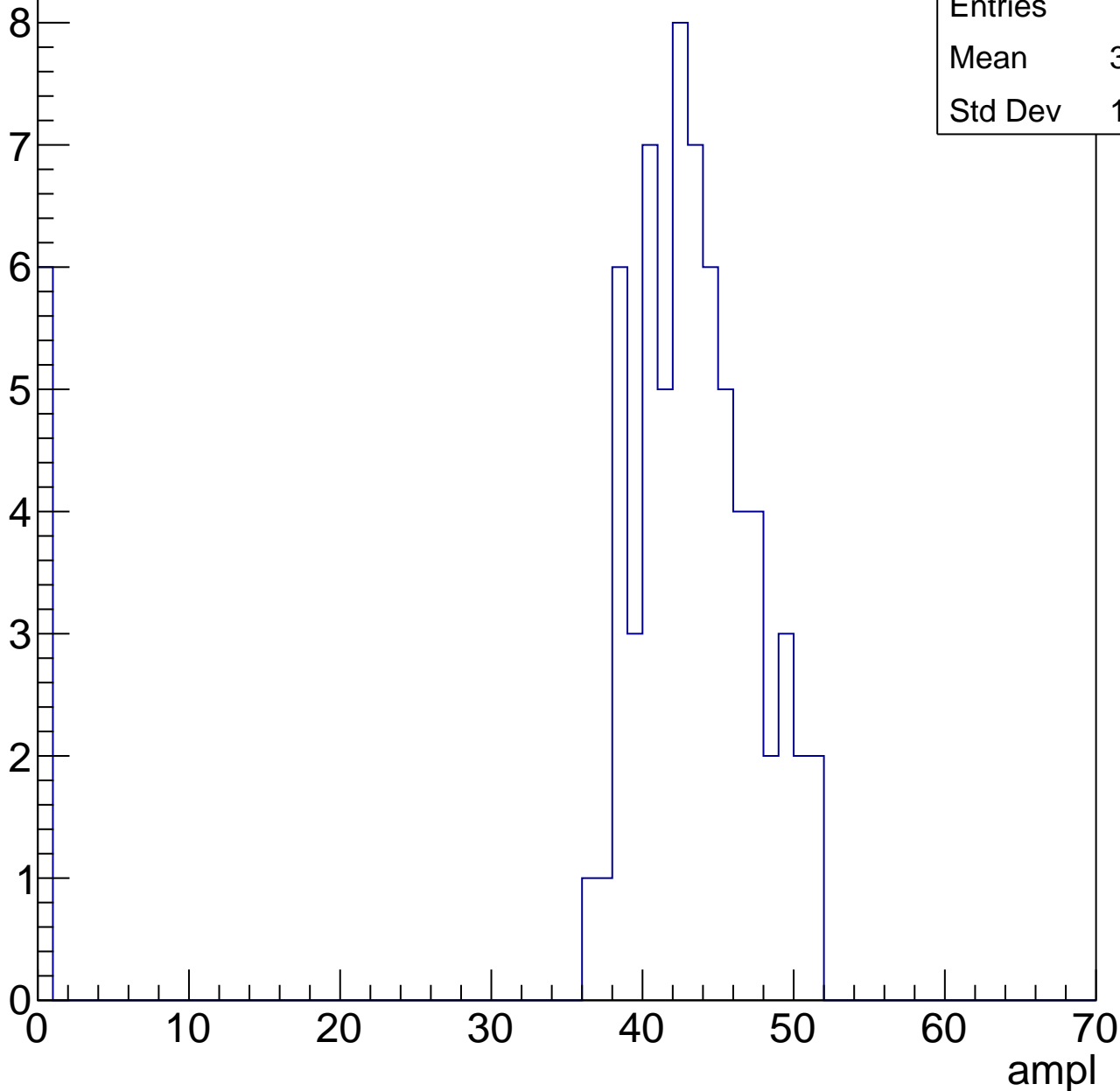
0

B1L103S, U11-ch59, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	39.53
Std Dev	12.42

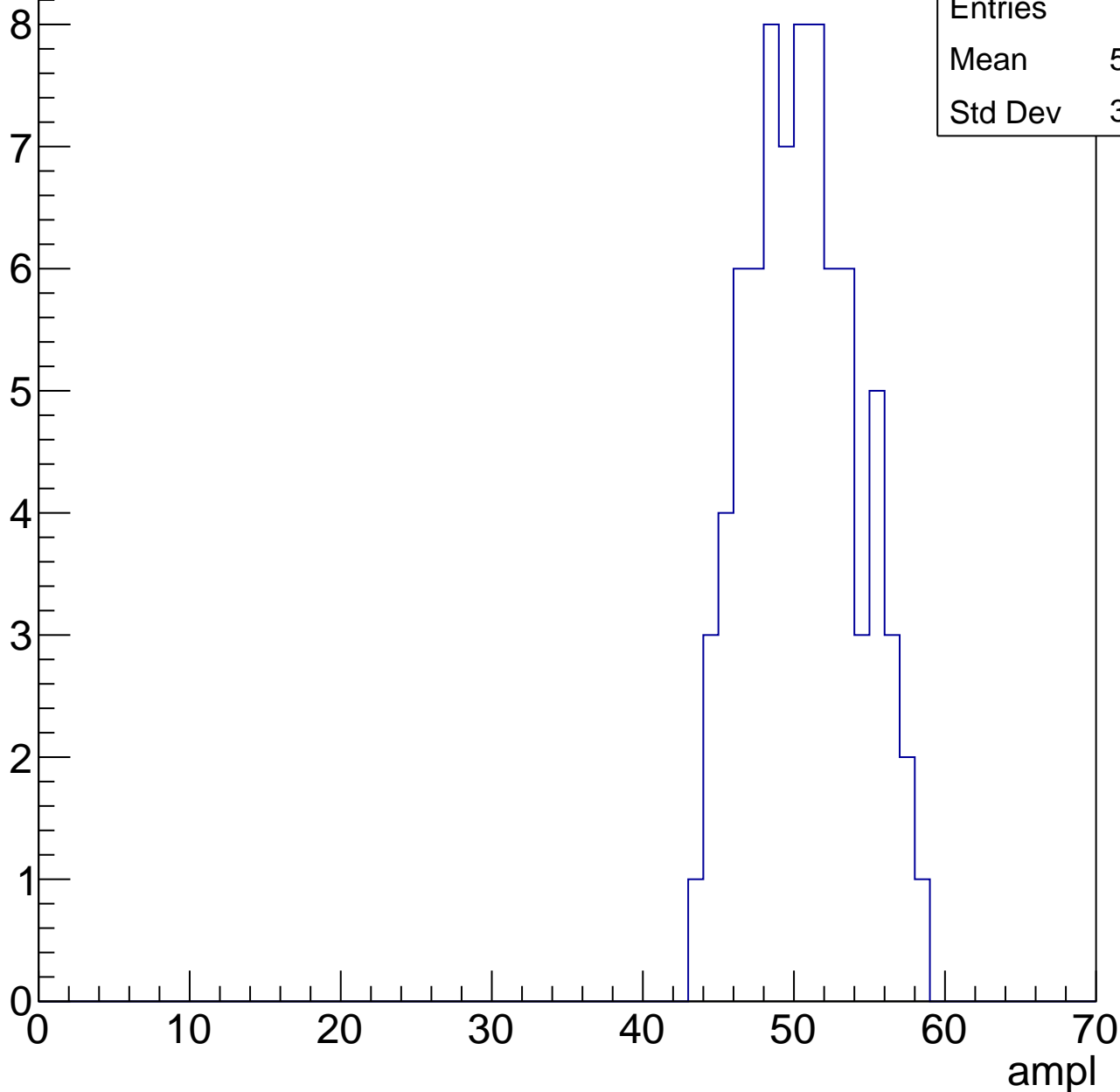


B1L103S, U11-ch59, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	50.06
Std Dev	3.558

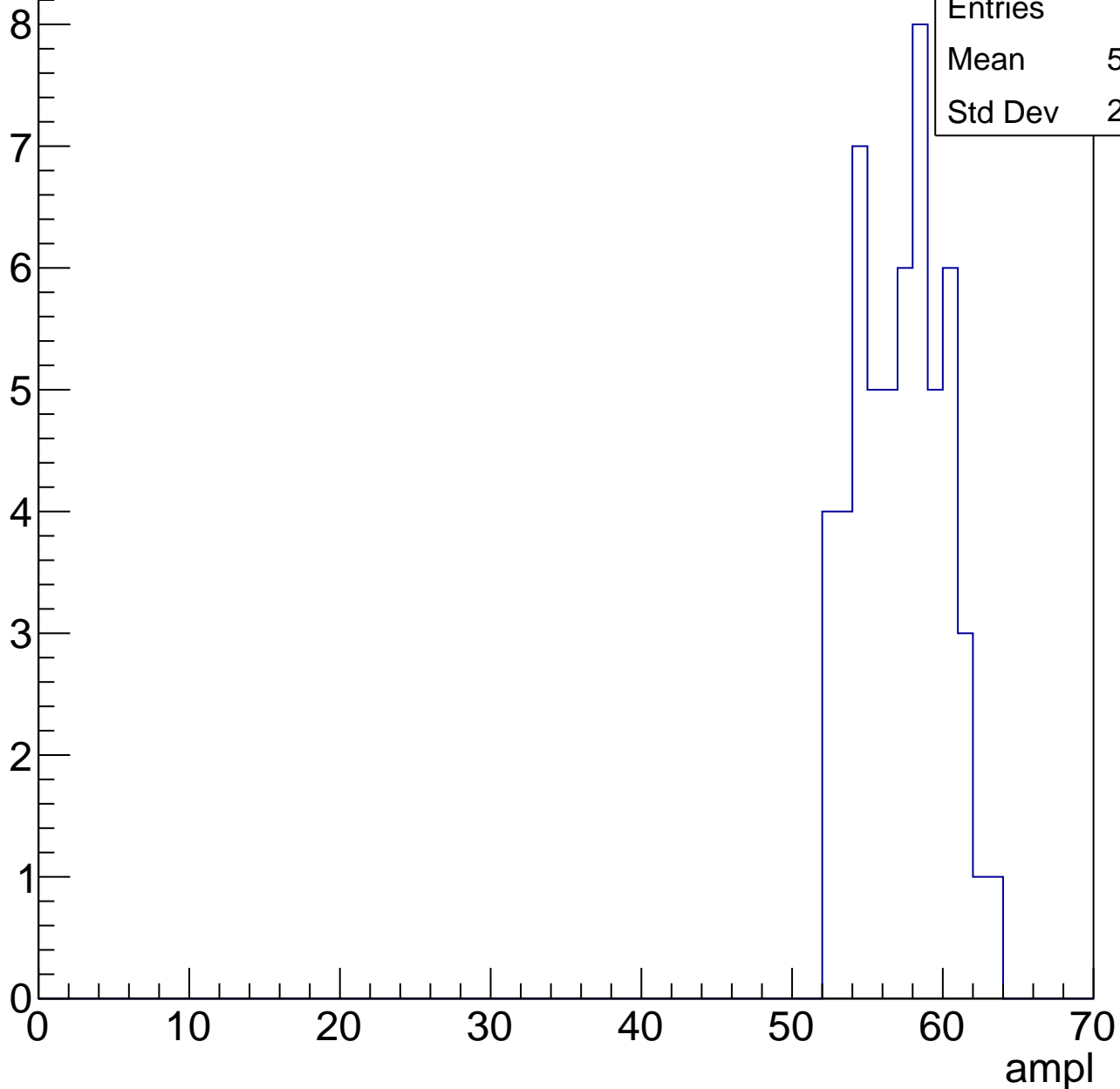


B1L103S, U11-ch59, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	56.76
Std Dev	2.828

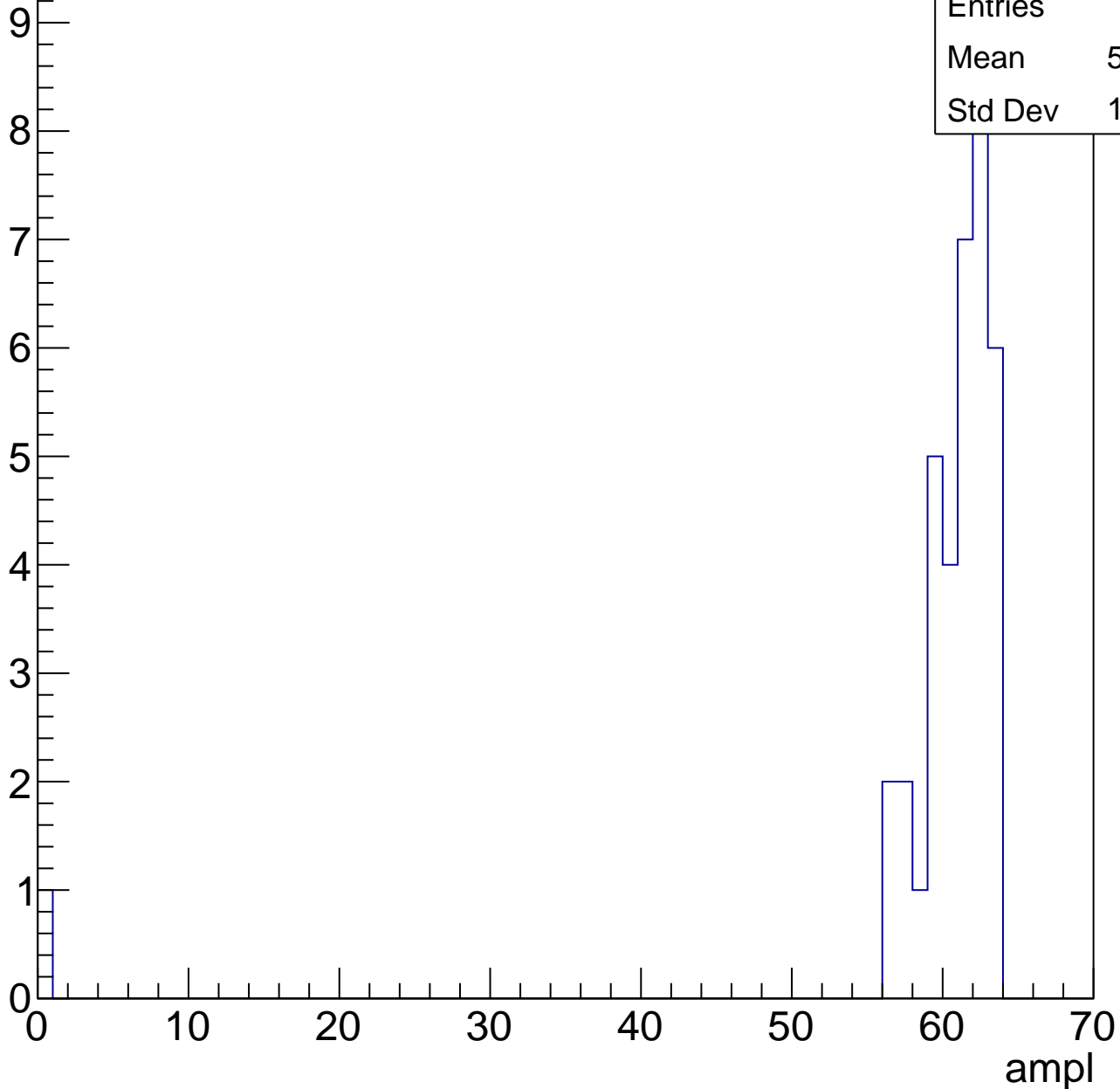


B1L103S, U11-ch59, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	37
Mean	58.97
Std Dev	10.02



B1L103S, U11-ch59, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch59, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

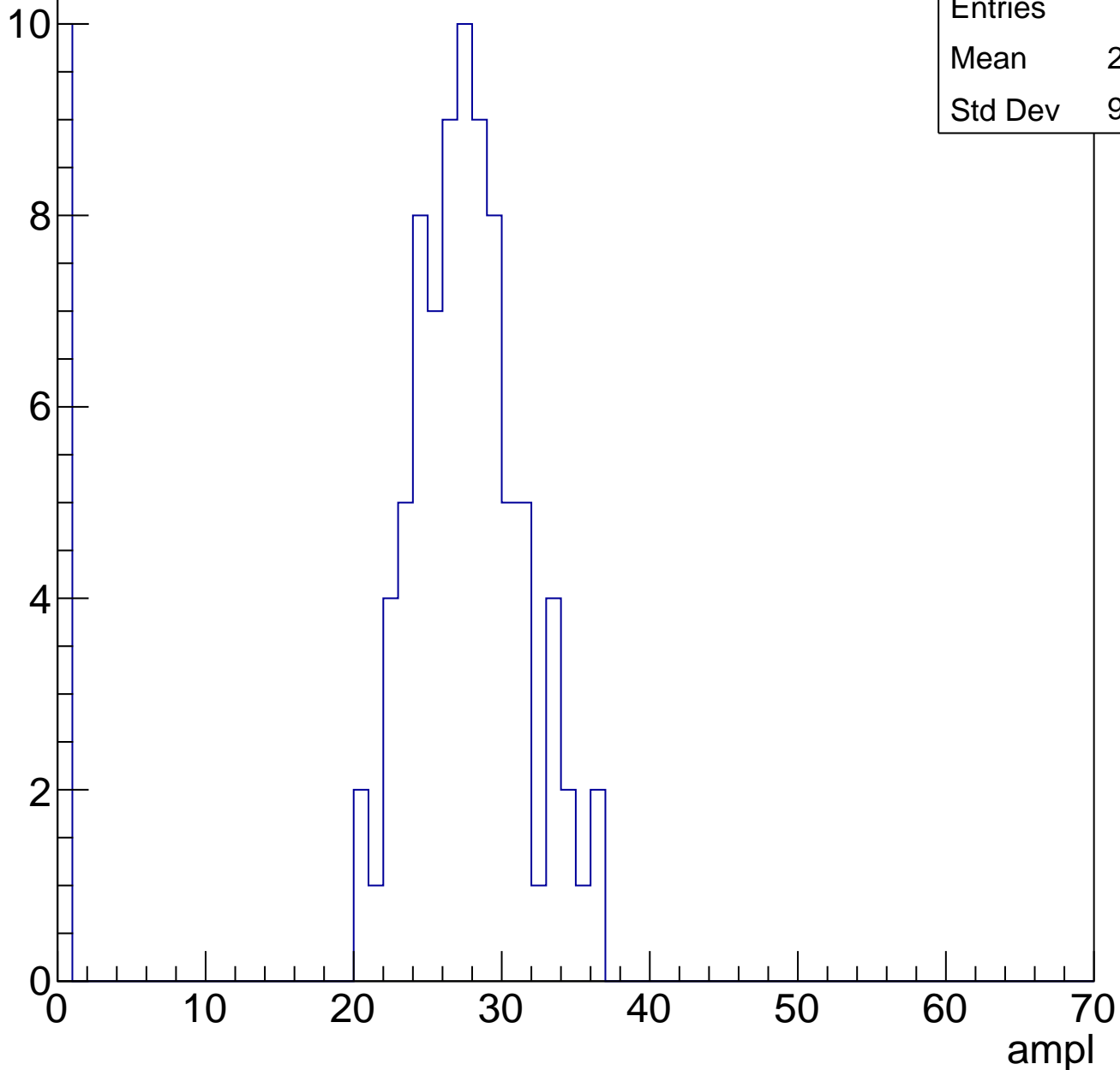


B1L103S, U11-ch60, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	93
Mean	24.33
Std Dev	9.106

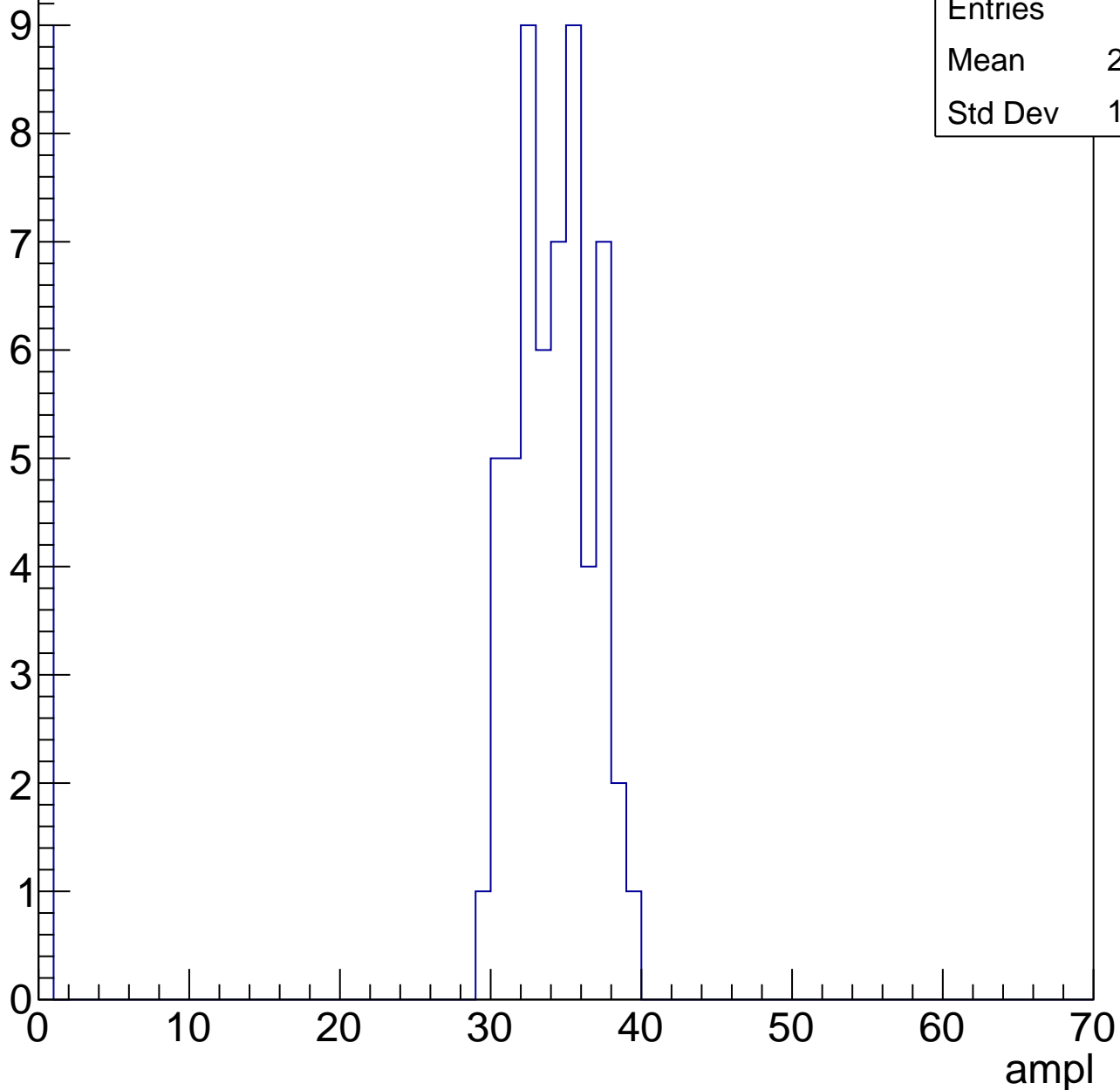
Entry



B1L103S, U11-ch60, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

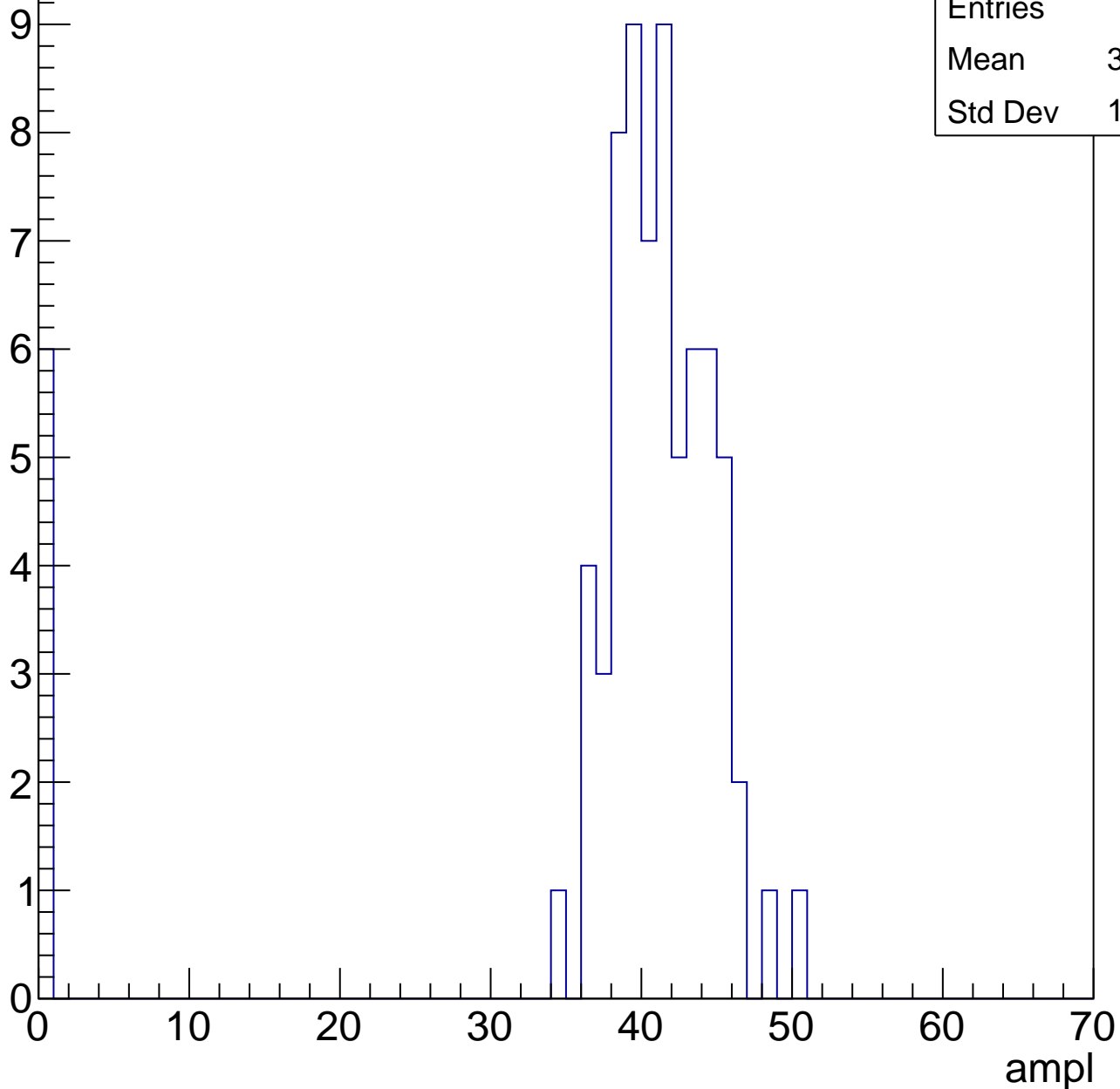


Entries	65
Mean	29.09
Std Dev	11.88

B1L103S, U11-ch60, adc2

calib_packv5_041523_1651.root, FC#0, port C2

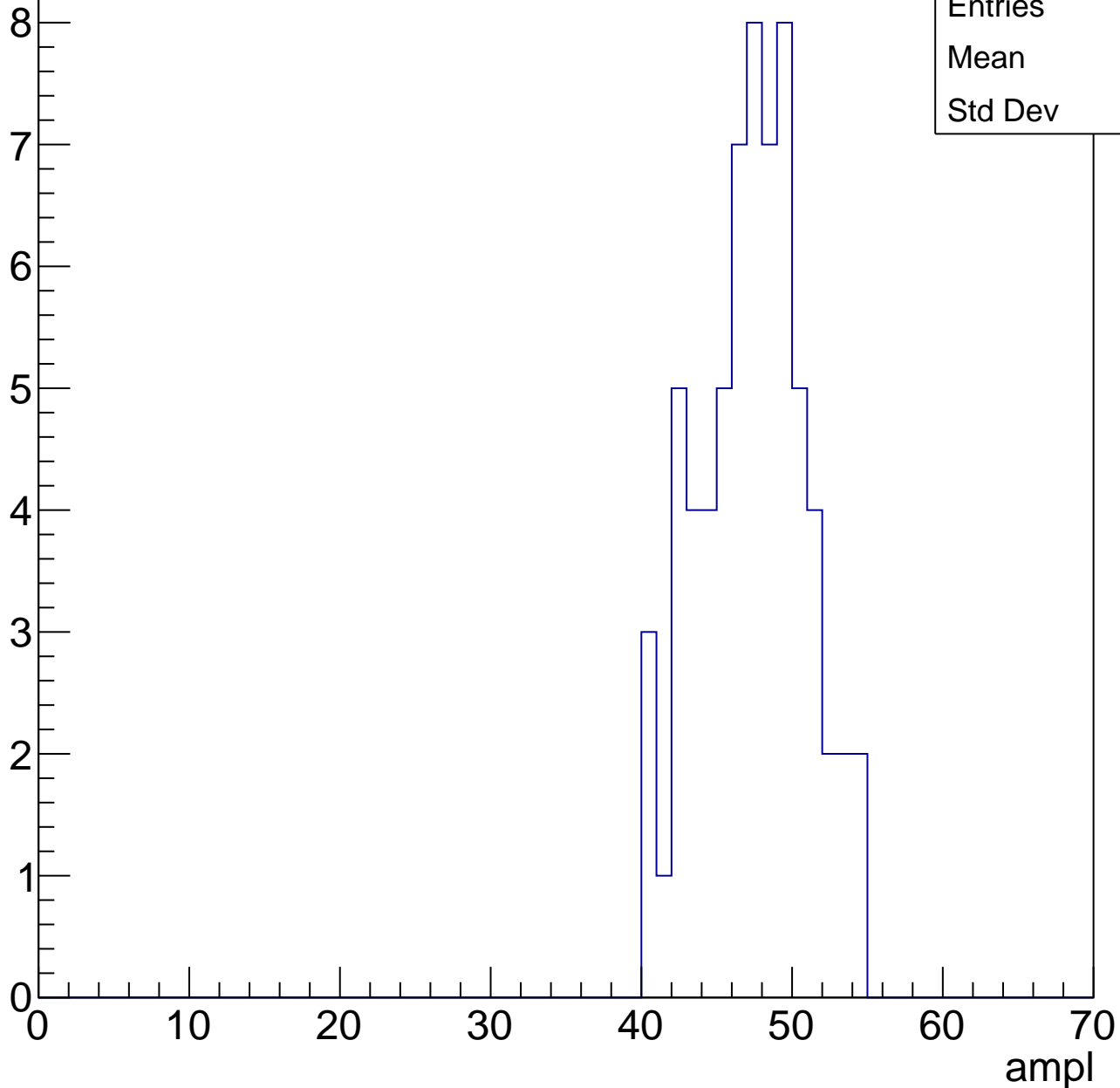
Entry



B1L103S, U11-ch60, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

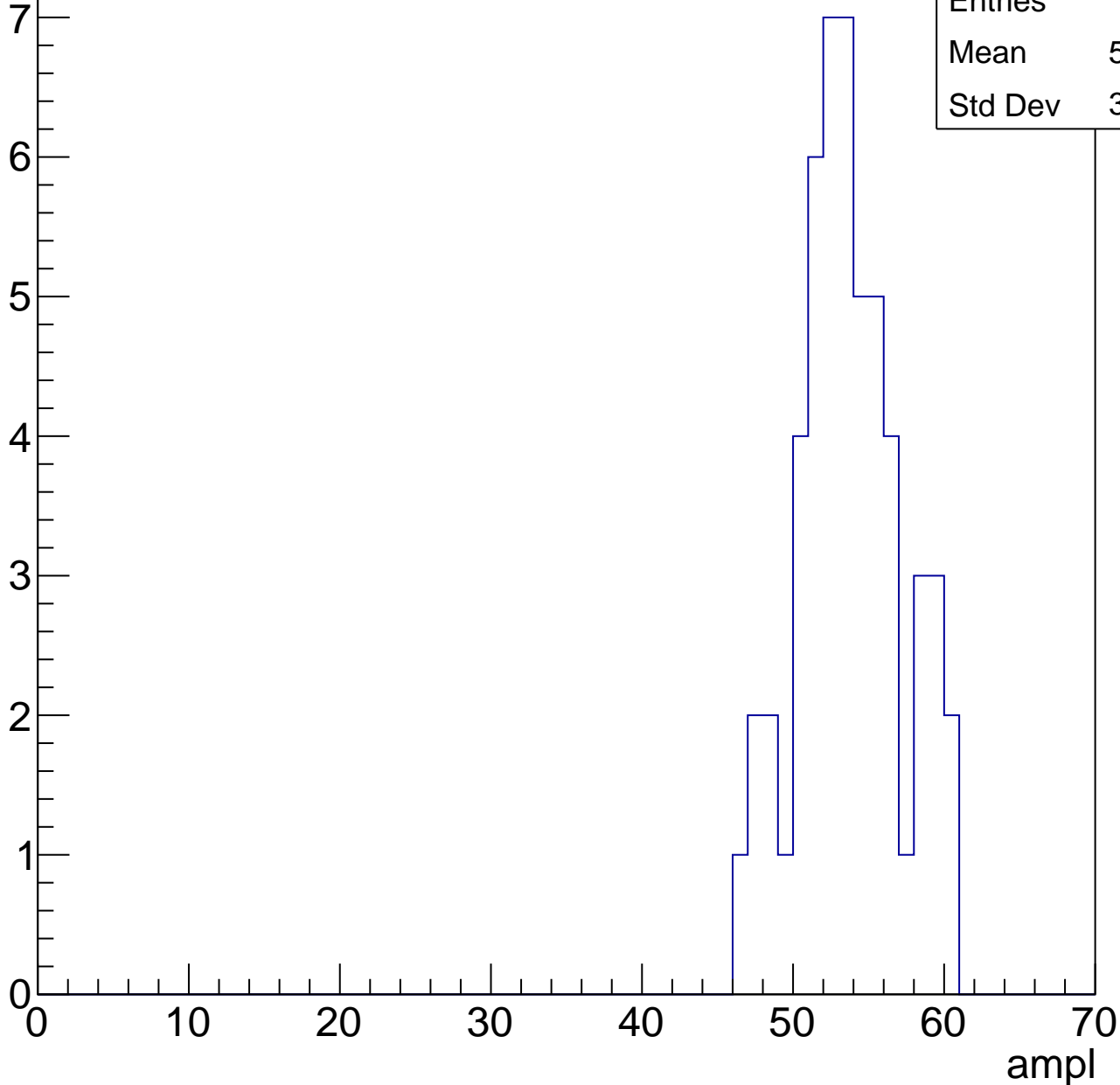


B1L103S, U11-ch60, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

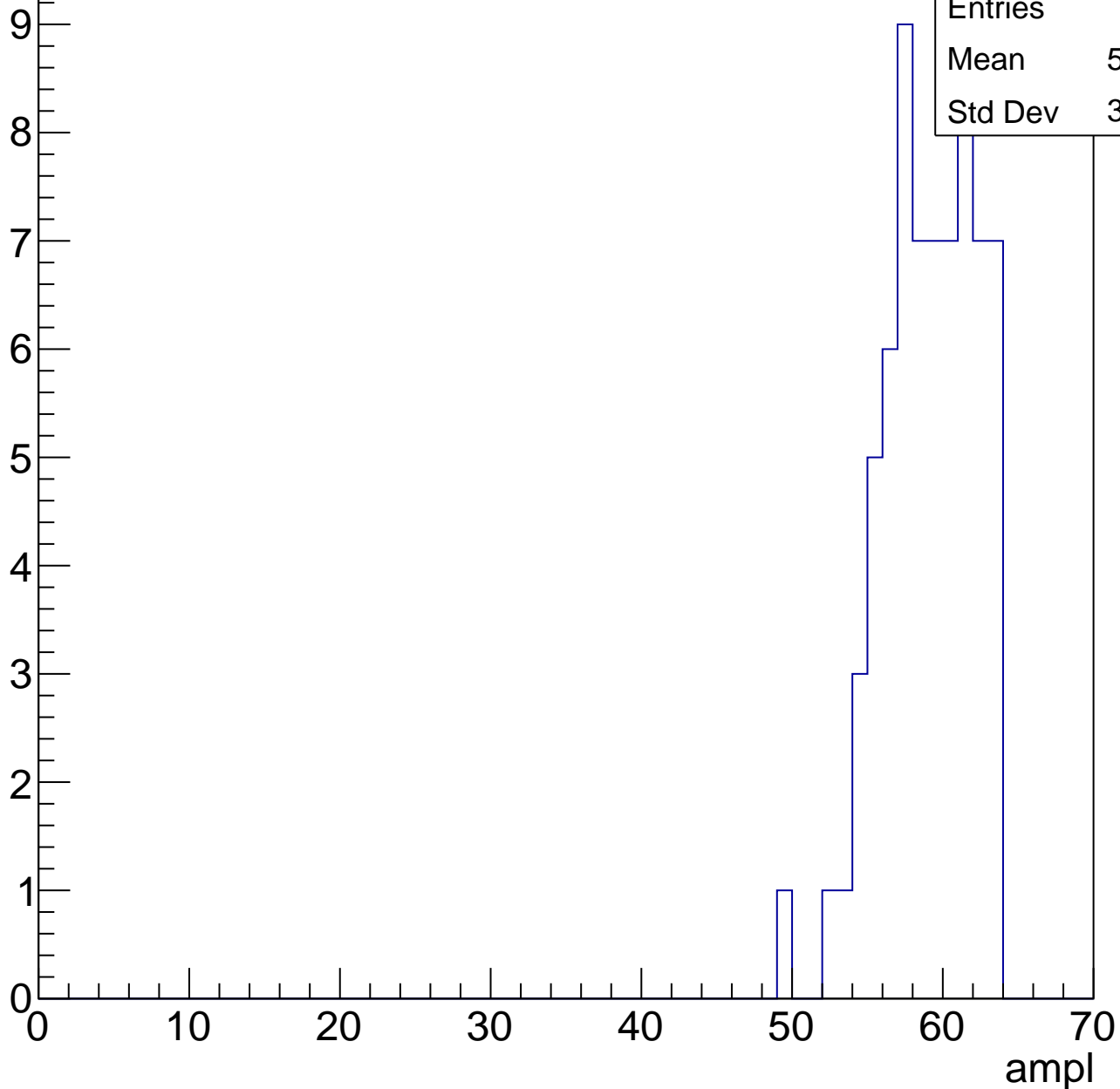
Entries	53
Mean	53.26
Std Dev	3.388



B1L103S, U11-ch60, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

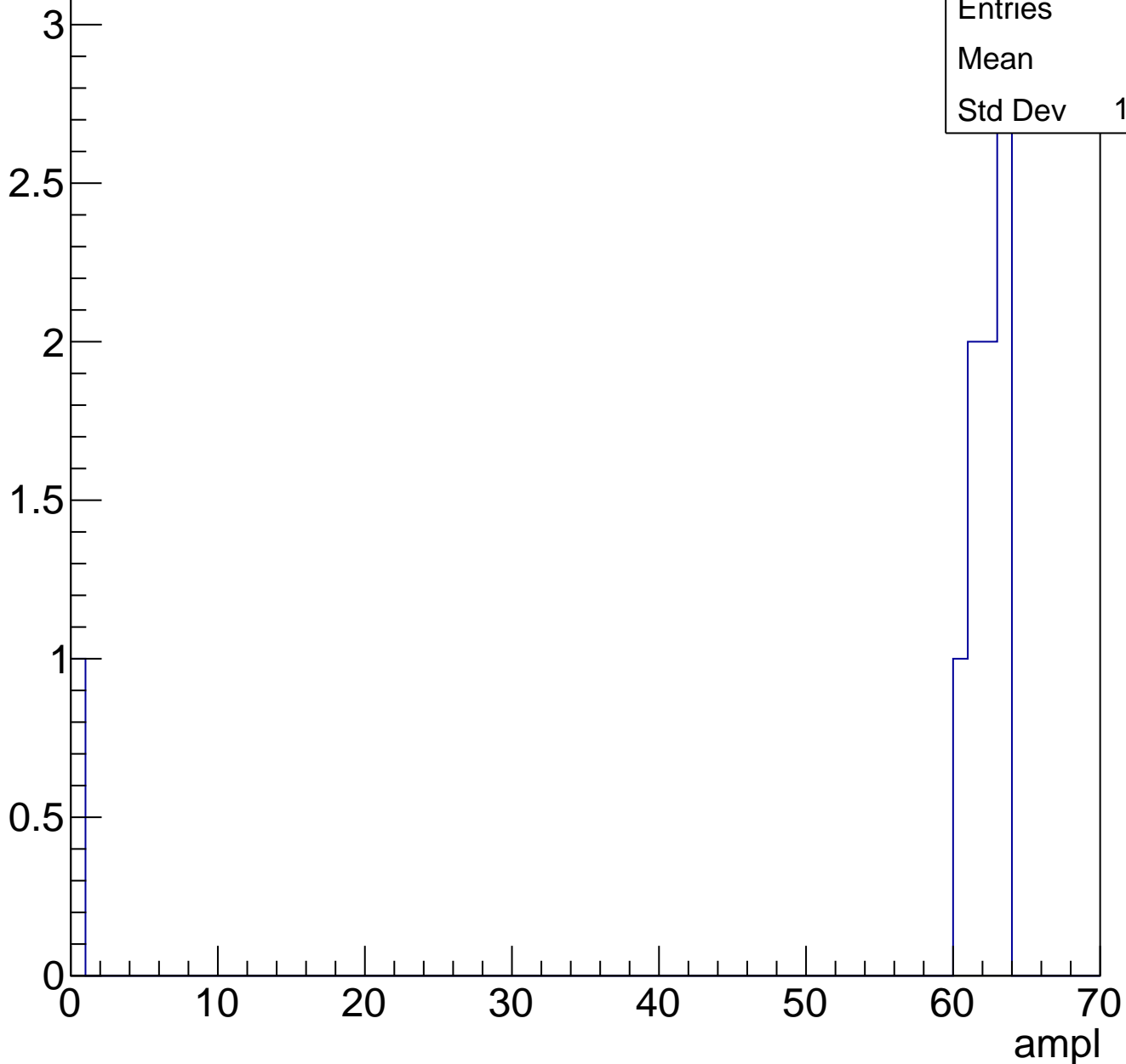


Entries	69
Mean	58.58
Std Dev	3.043

B1L103S, U11-ch60, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch60, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51

Entry

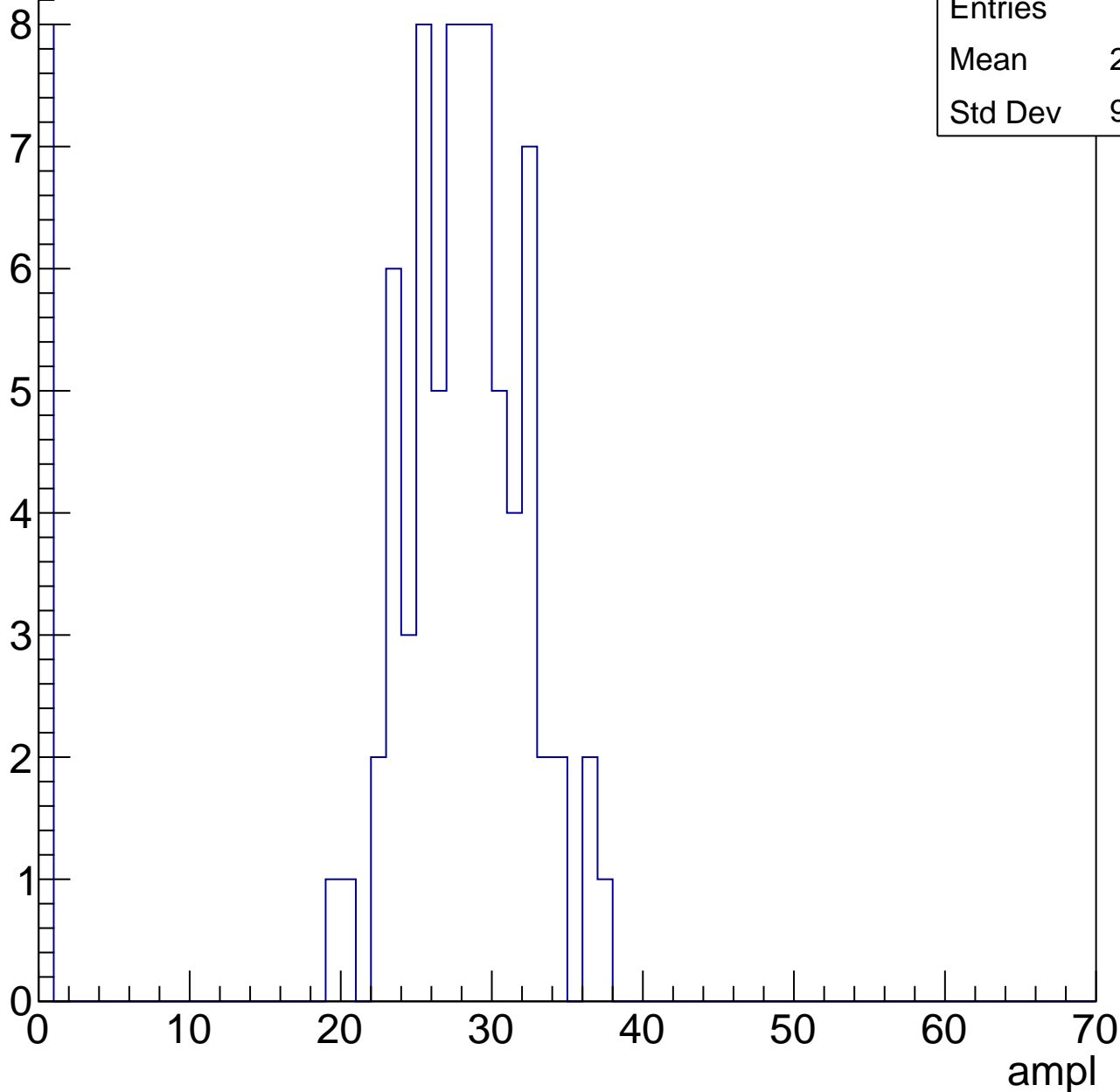


B1L103S, U11-ch61, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	81
Mean	25.14
Std Dev	9.047

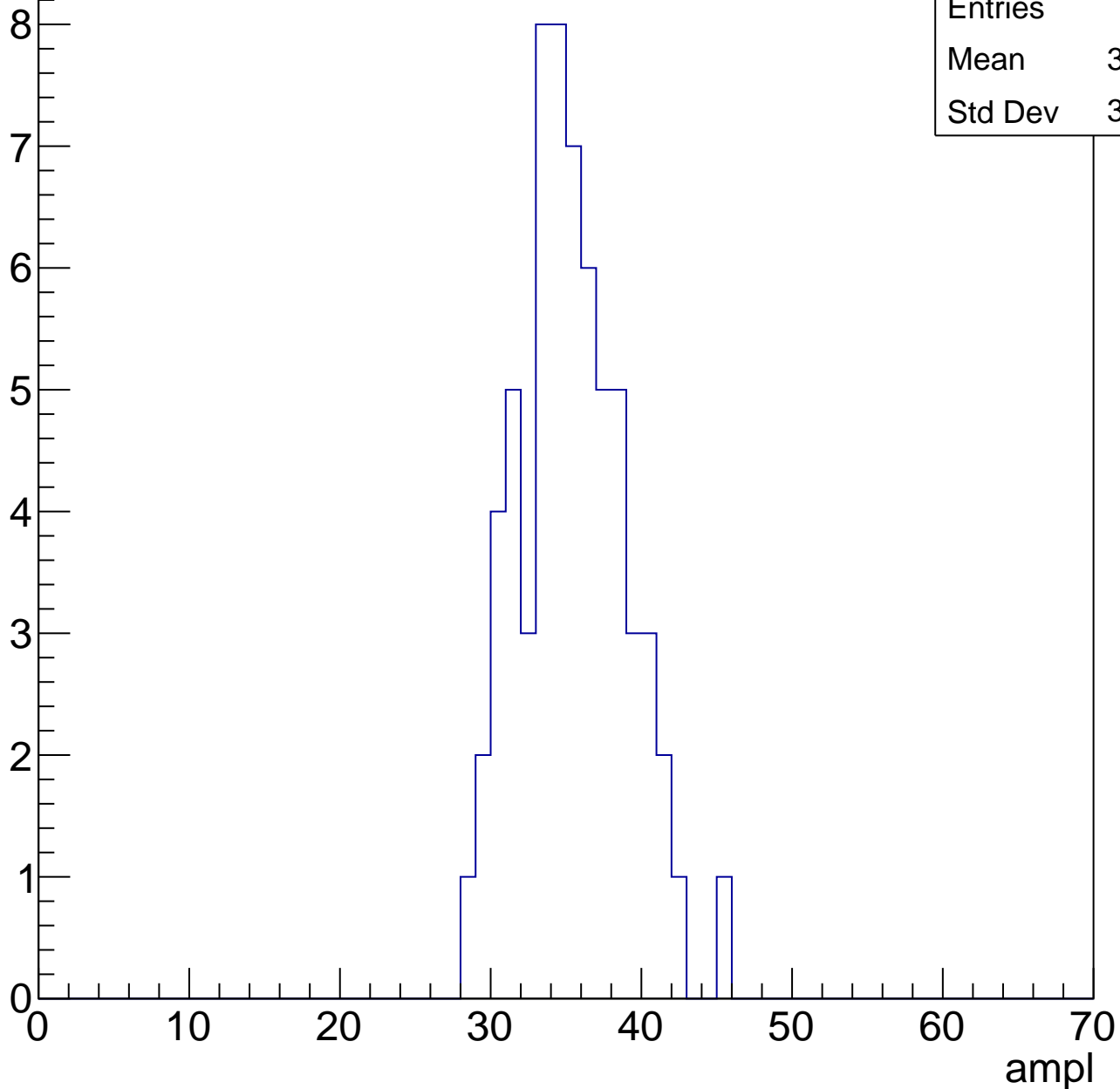


B1L103S, U11-ch61, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

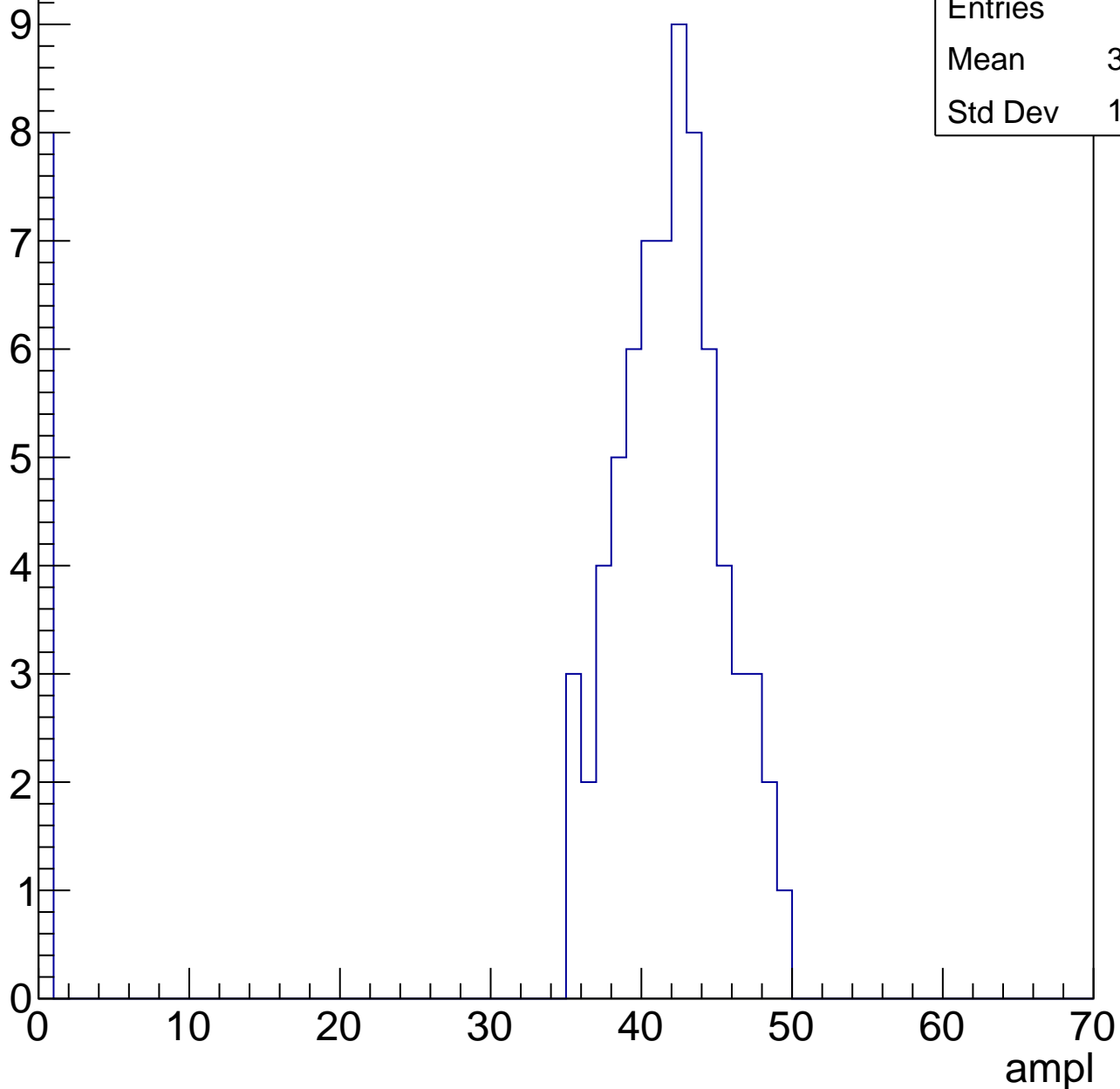
Entries	64
Mean	34.92
Std Dev	3.497



B1L103S, U11-ch61, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry



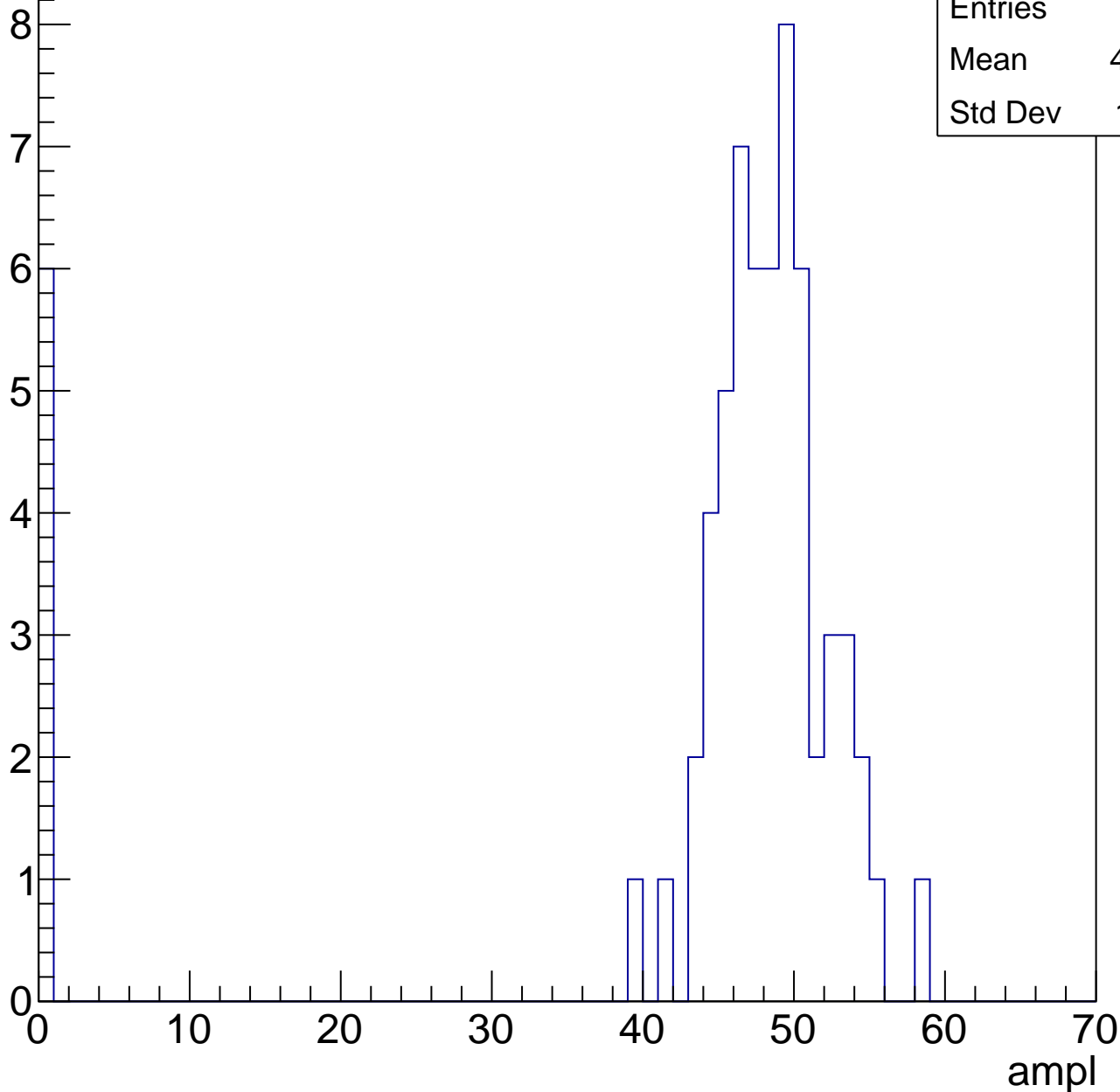
Entries	78
Mean	37.26
Std Dev	12.99

B1L103S, U11-ch61, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	43.58
Std Dev	14.41

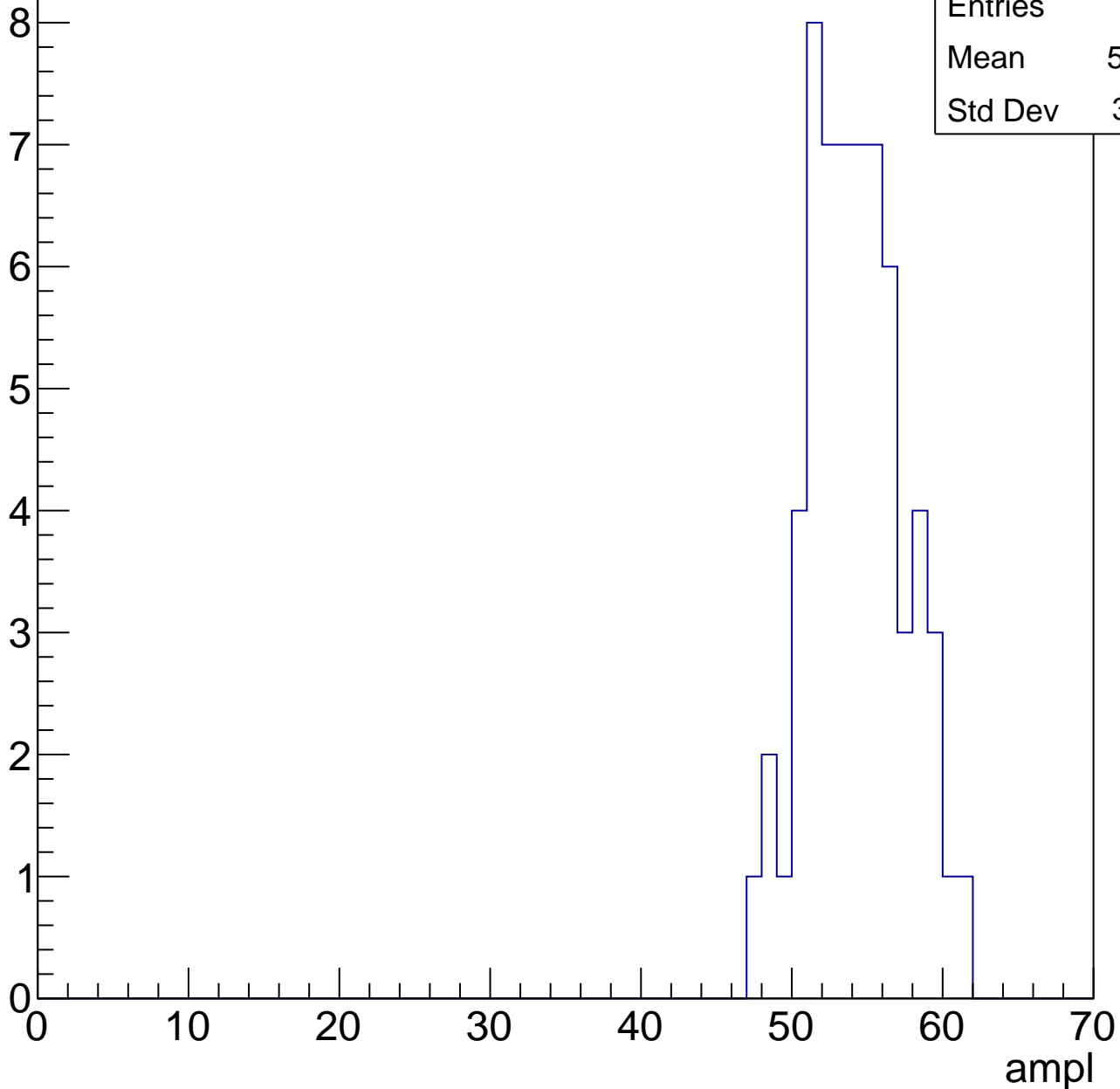


B1L103S, U11-ch61, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

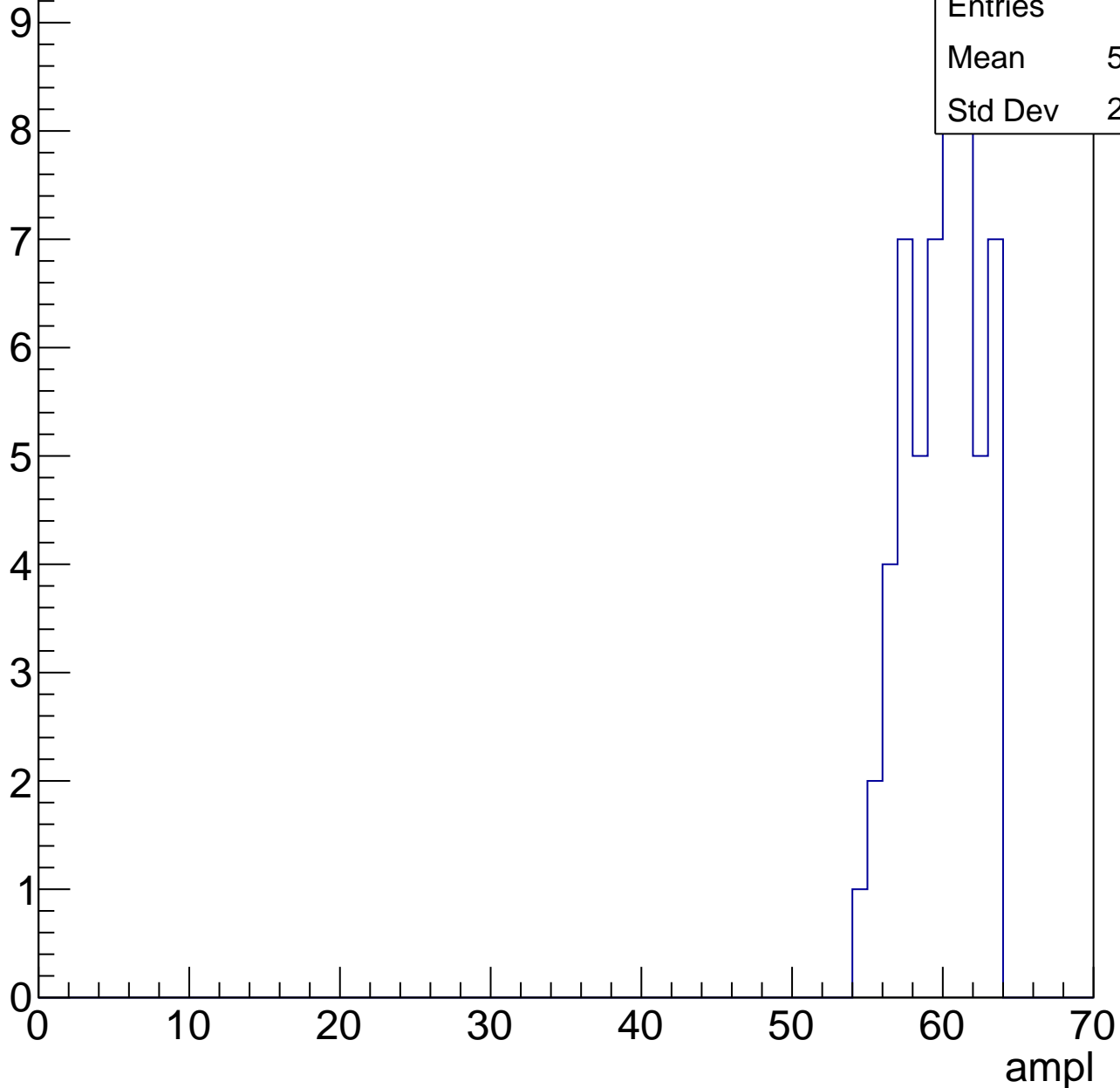
Entries	62
Mean	53.79
Std Dev	3.101



B1L103S, U11-ch61, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



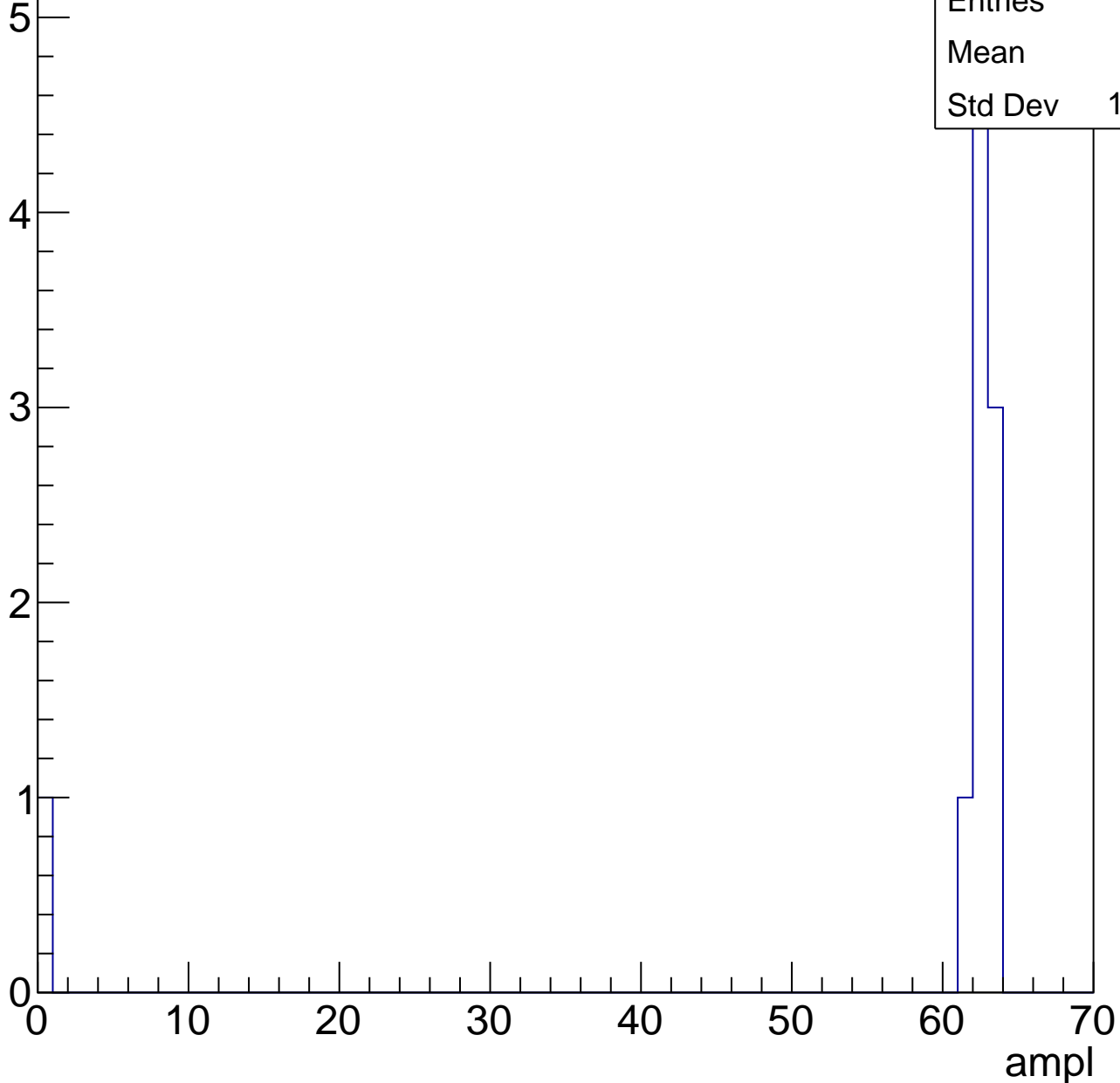
Entries	55
Mean	59.44
Std Dev	2.388

B1L103S, U11-ch61, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	10
Mean	56
Std Dev	18.68

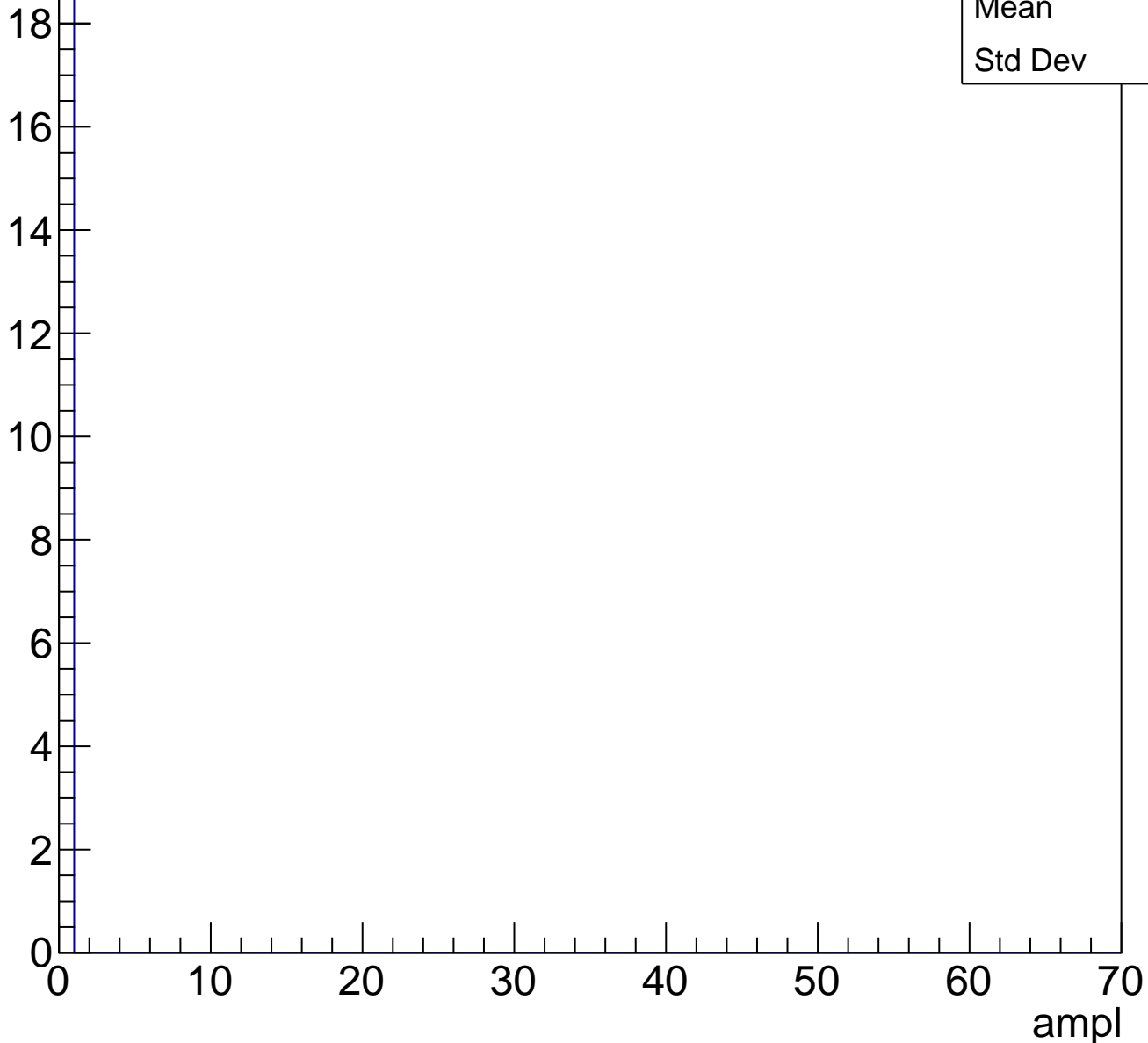


B1L103S, U11-ch61, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	0
Std Dev	0

Entry

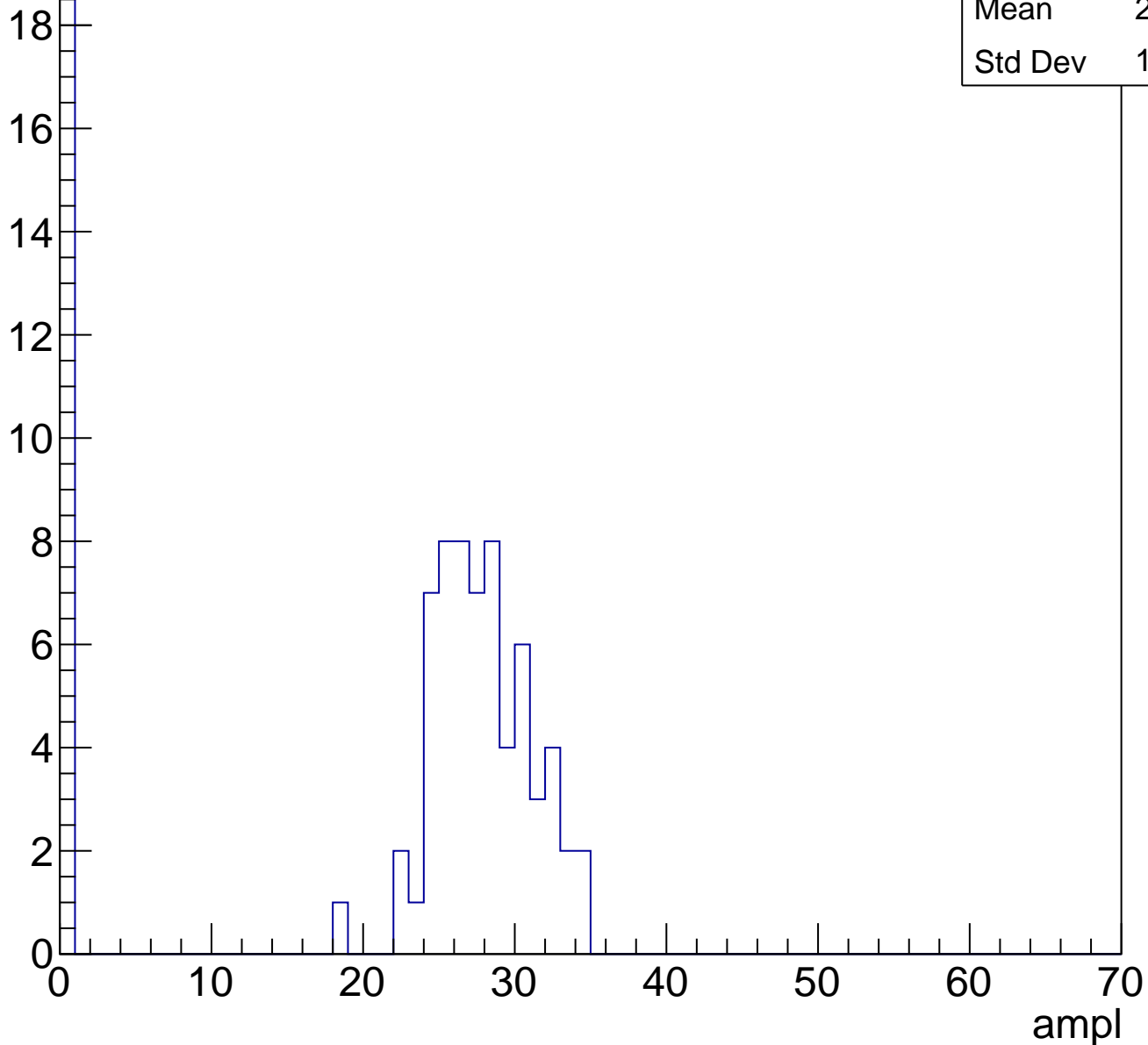


B1L103S, U11-ch62, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	21.04
Std Dev	11.88

Entry

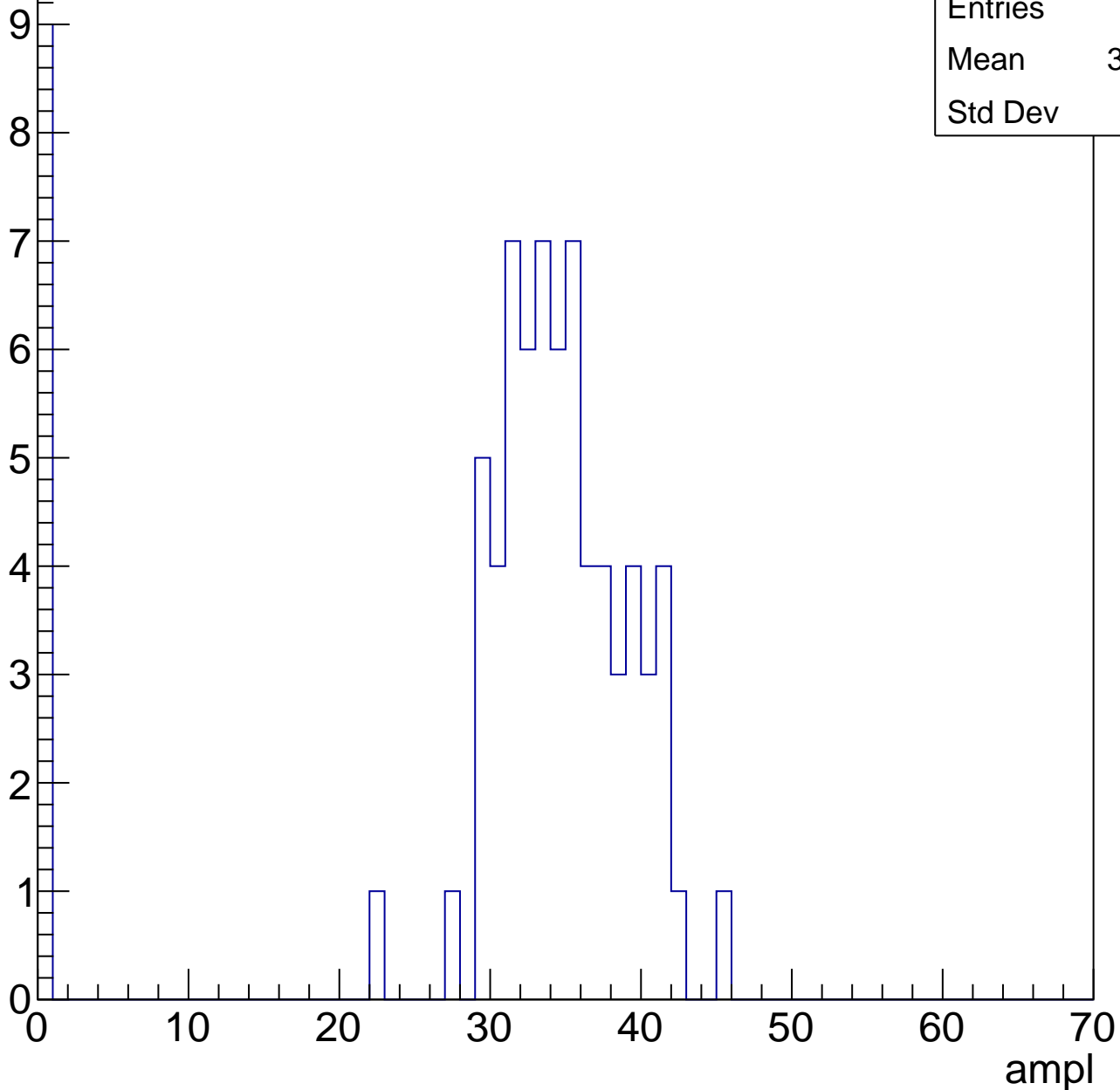


B1L103S, U11-ch62, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	30.34
Std Dev	11.7

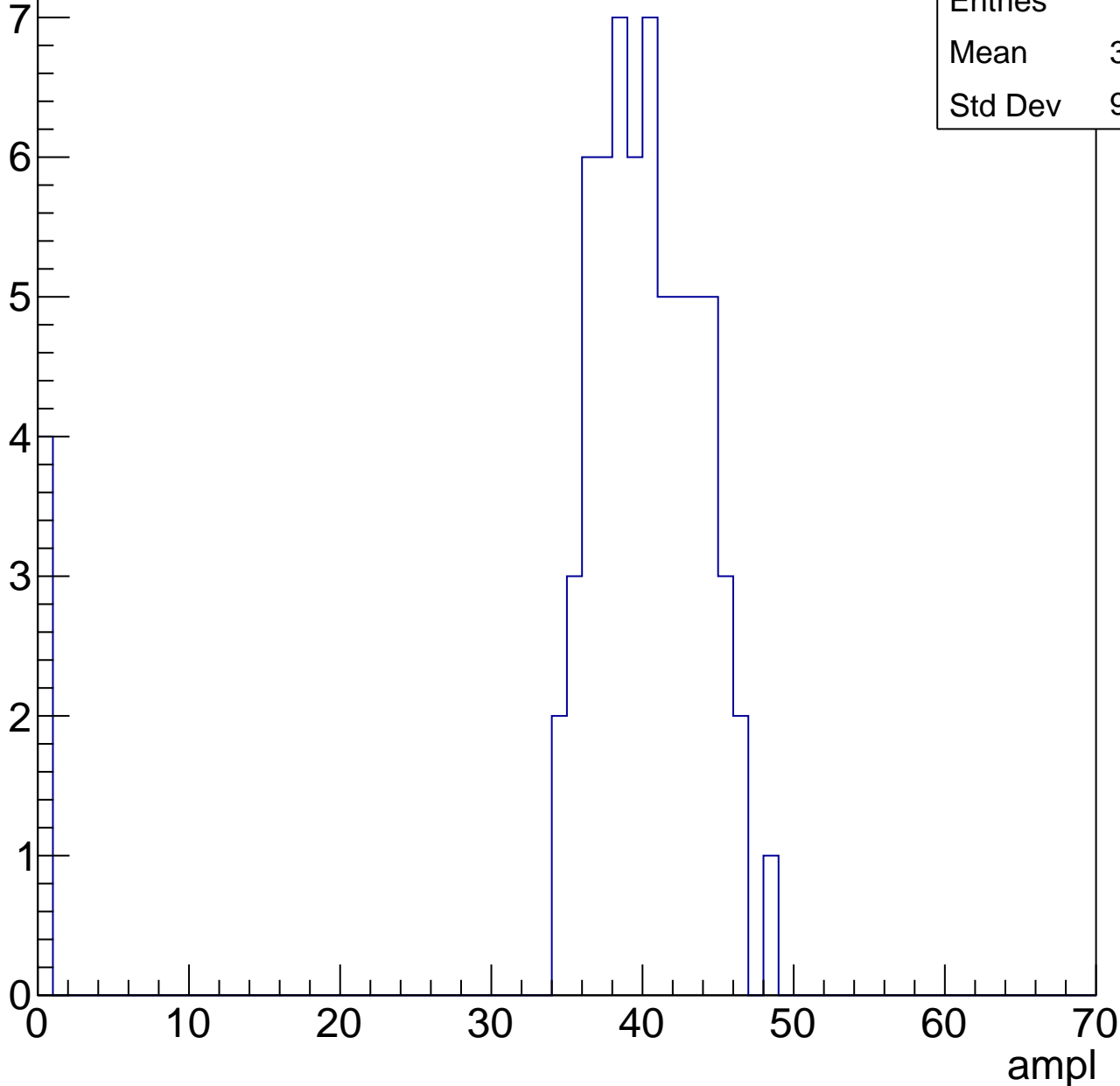


B1L103S, U11-ch62, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	37.55
Std Dev	9.993

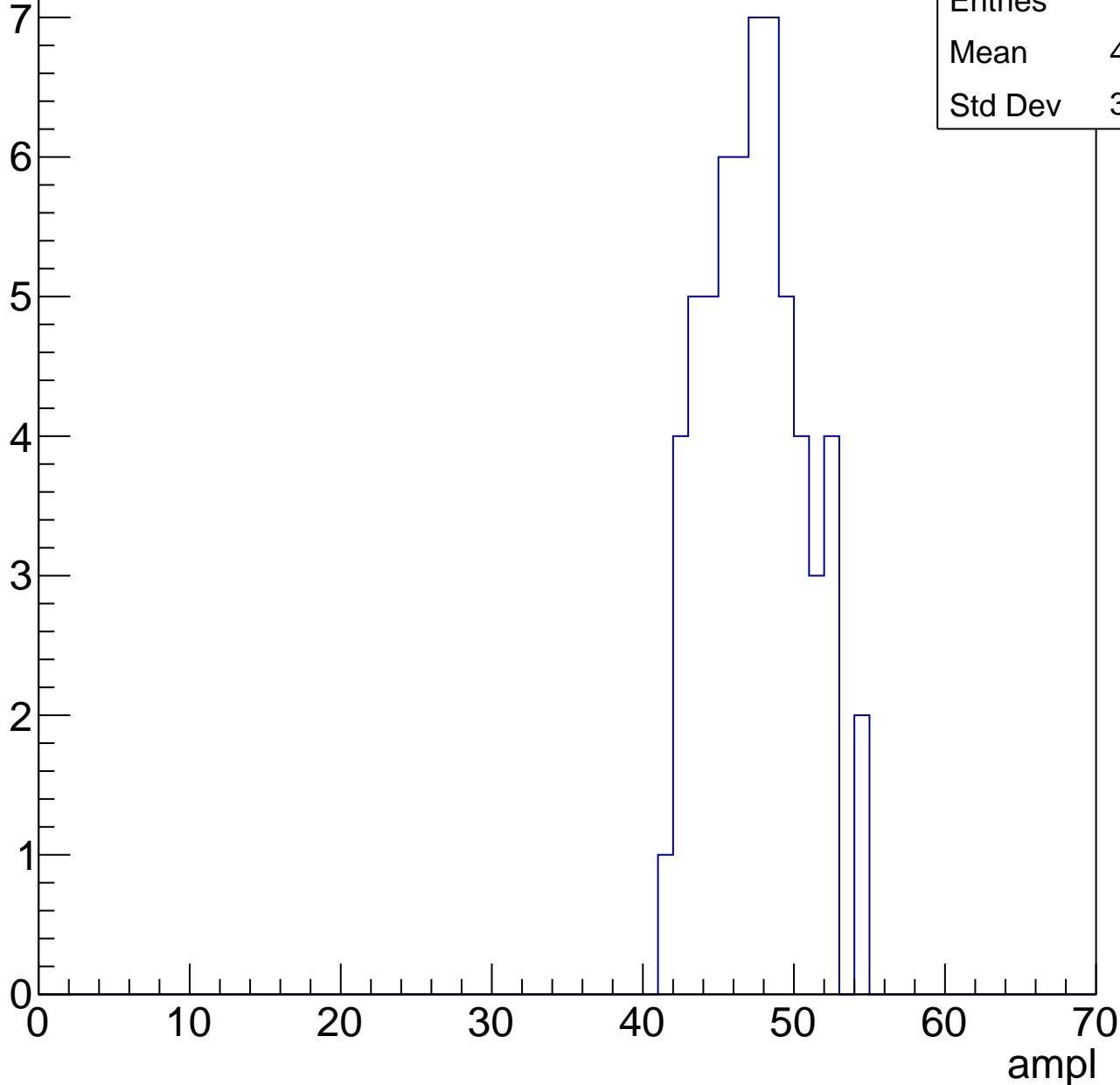


B1L103S, U11-ch62, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

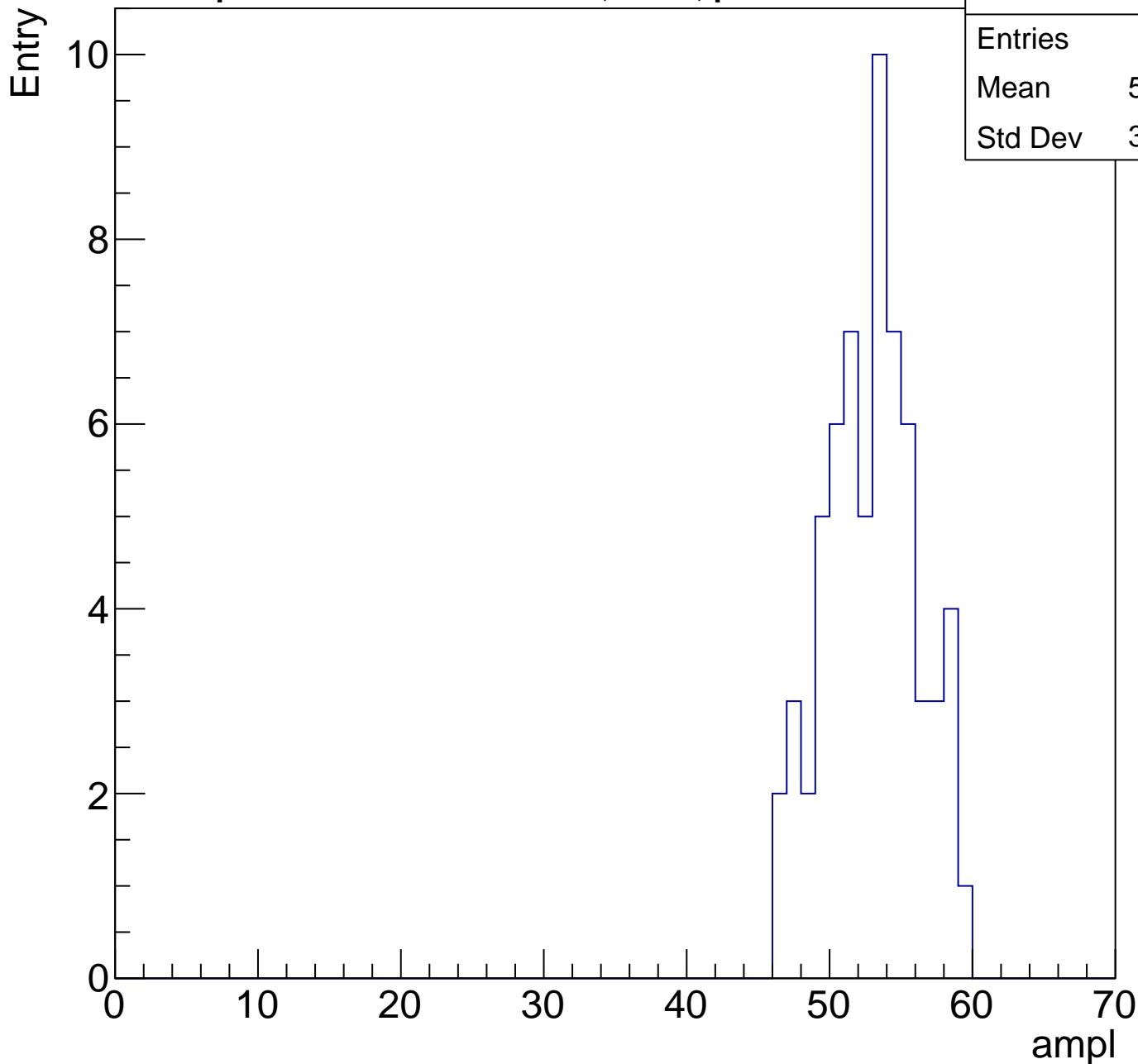
Entries	59
Mean	46.93
Std Dev	3.188



B1L103S, U11-ch62, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	64
Mean	52.48
Std Dev	3.182

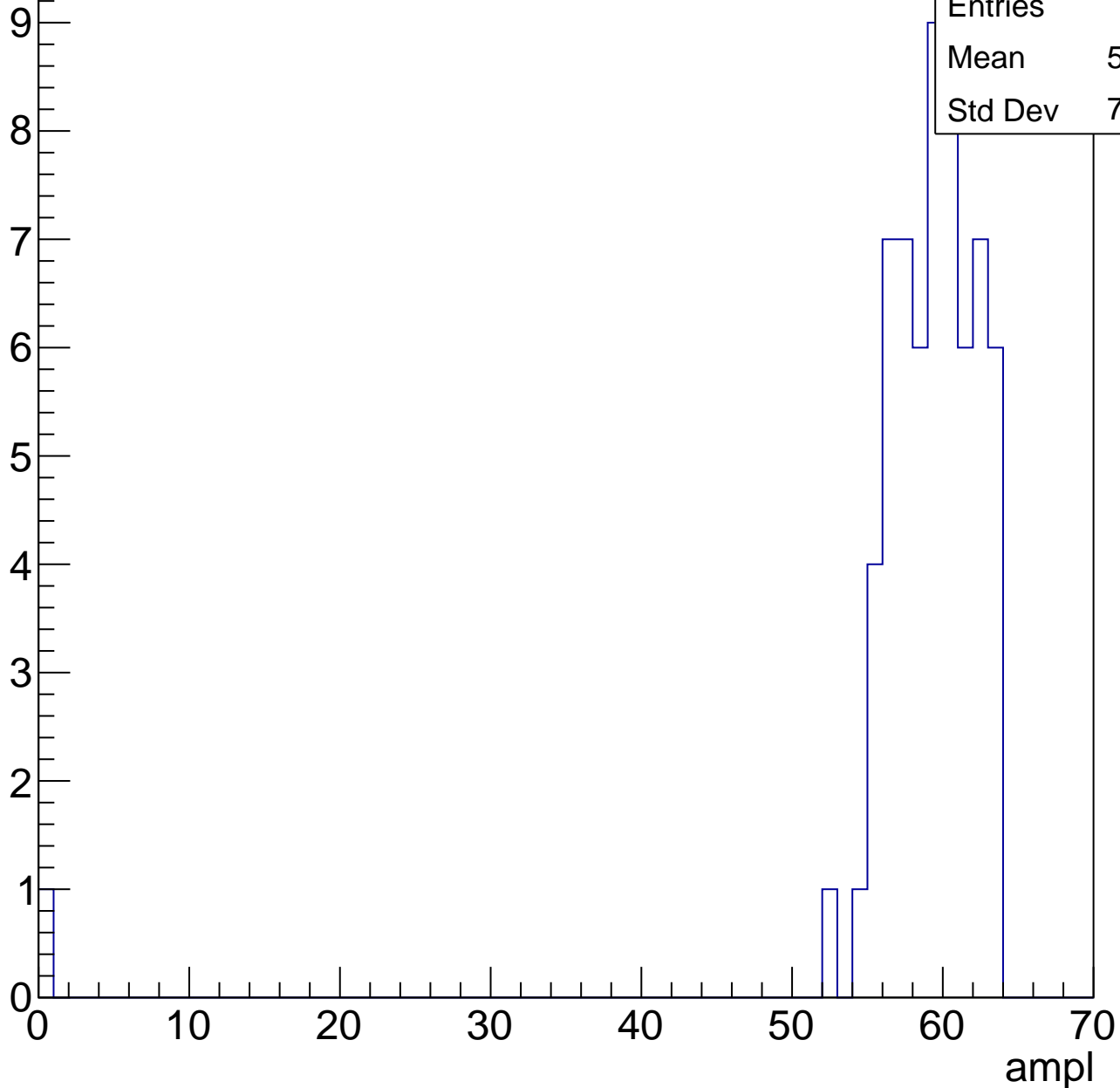


B1L103S, U11-ch62, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

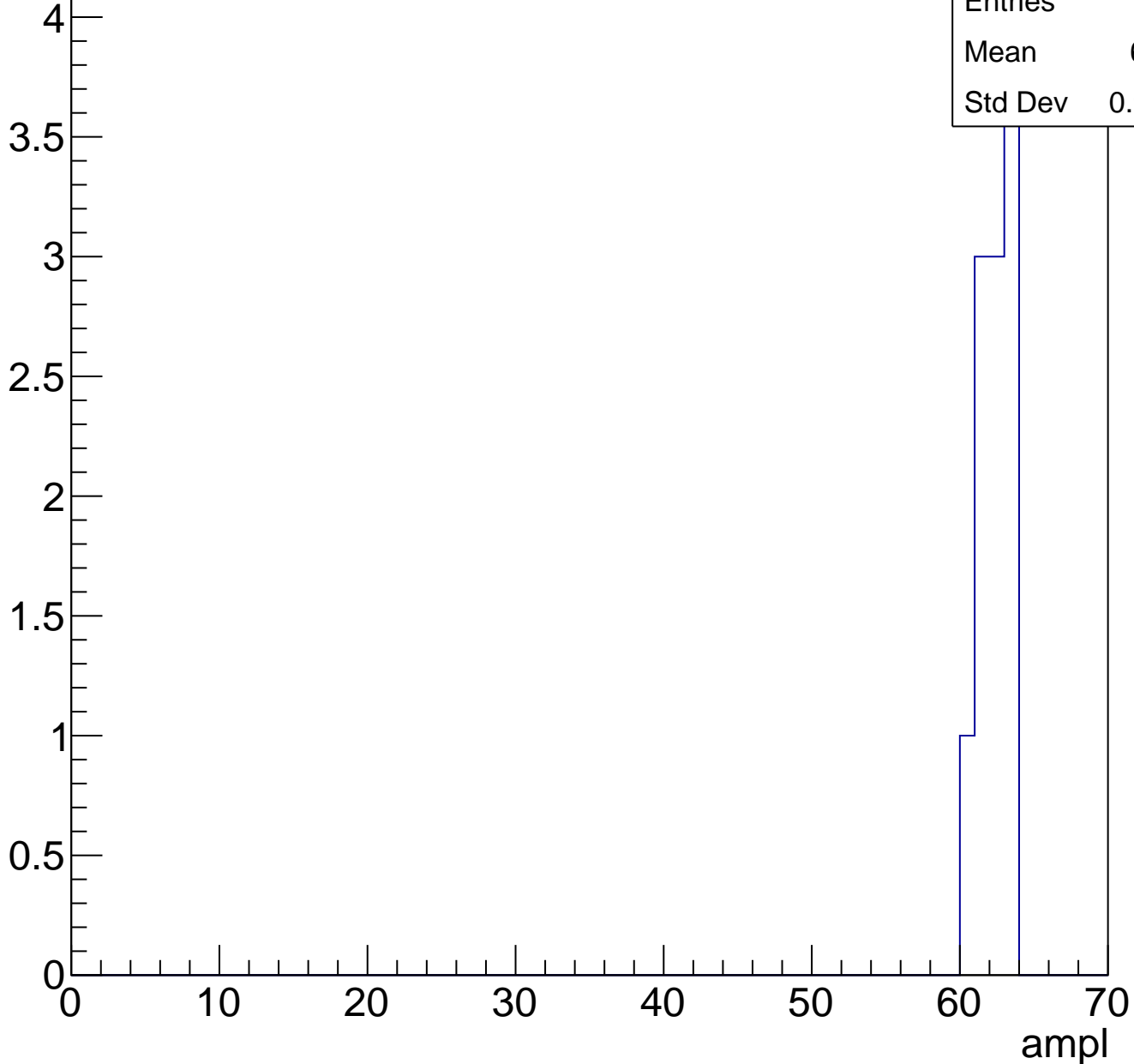
Entries	64
Mean	58.03
Std Dev	7.754



B1L103S, U11-ch62, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

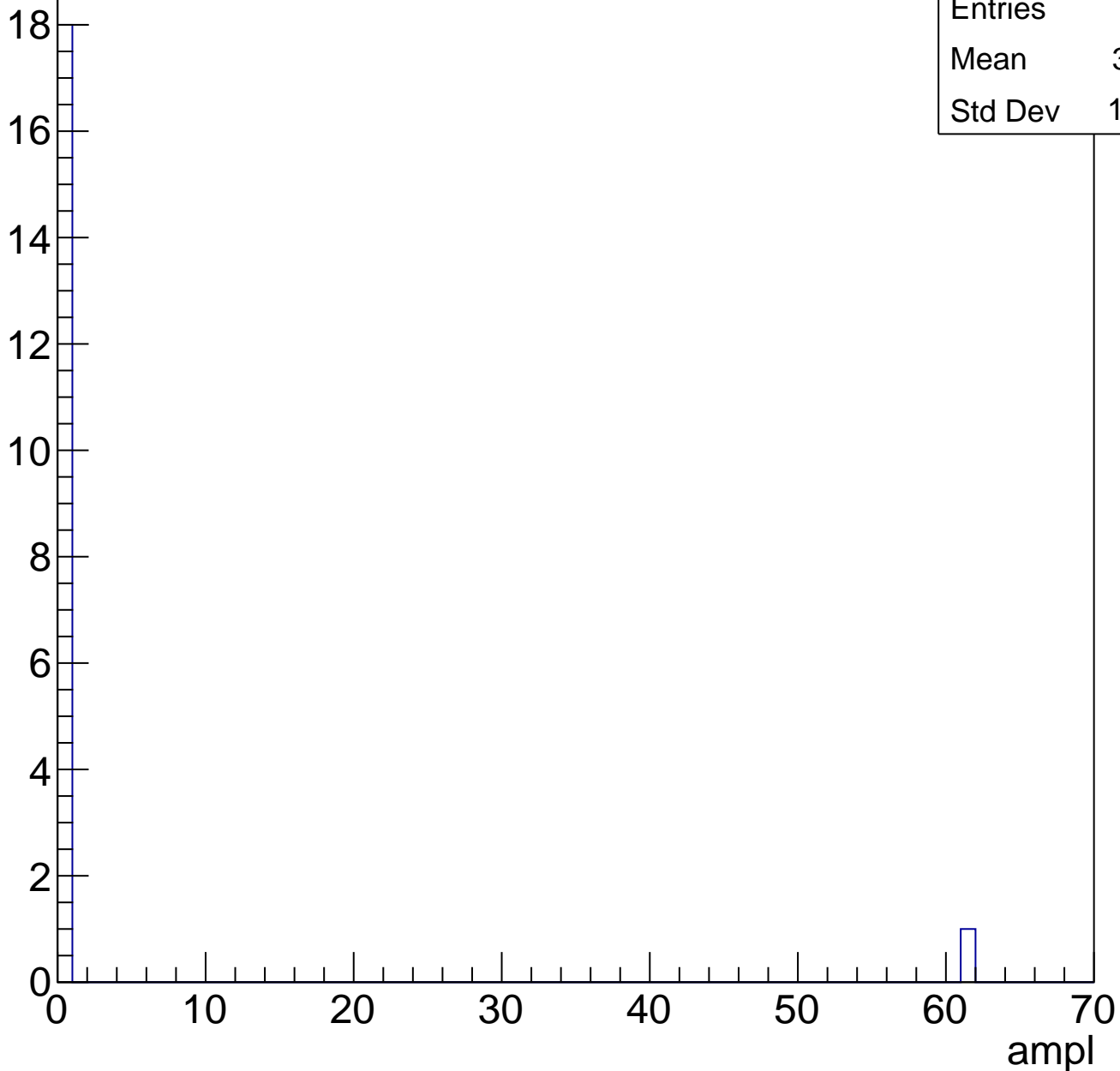


B1L103S, U11-ch62, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	3.211
Std Dev	13.62

Entry

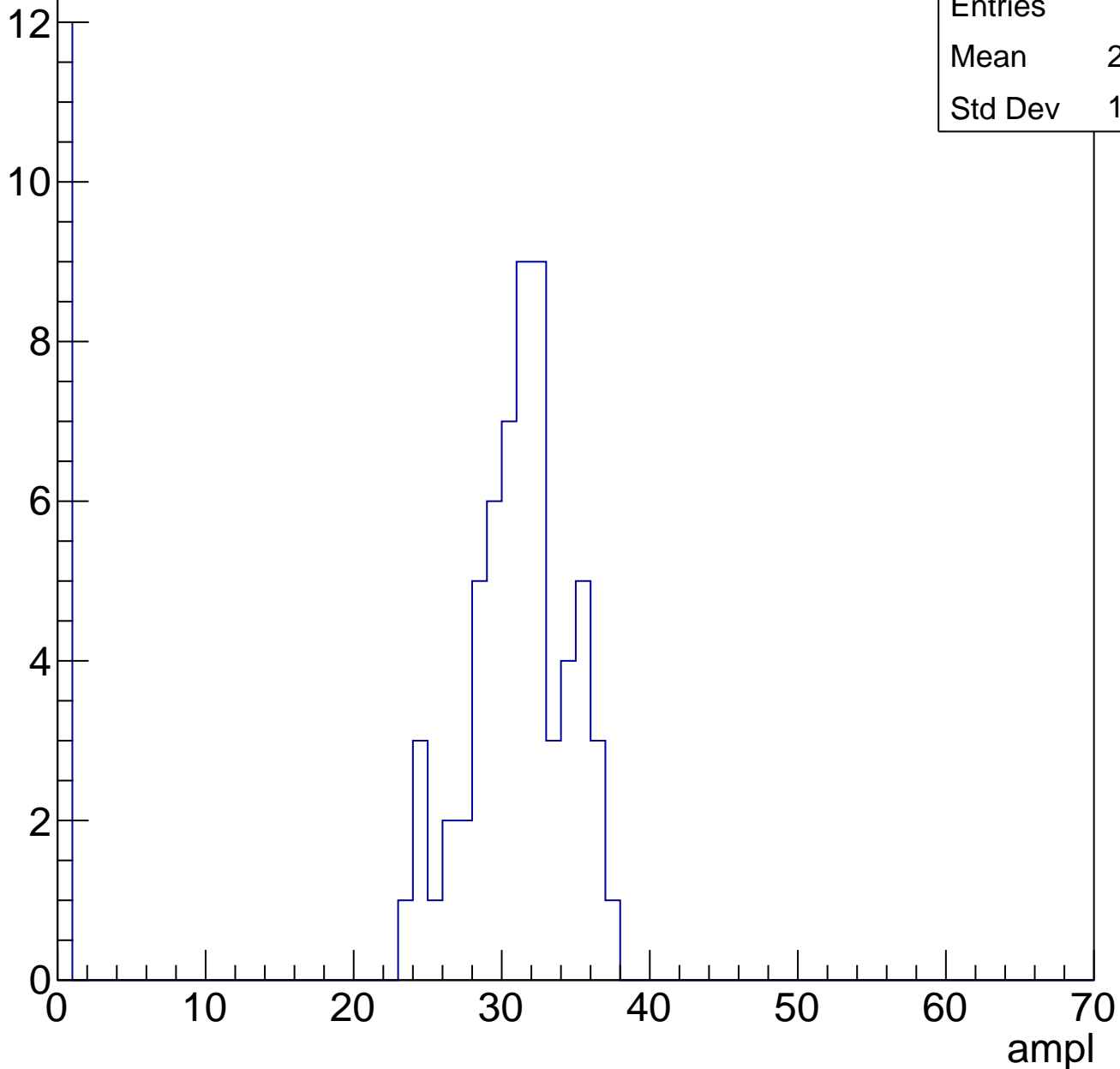


B1L103S, U11-ch63, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	73
Mean	25.64
Std Dev	11.76

Entry

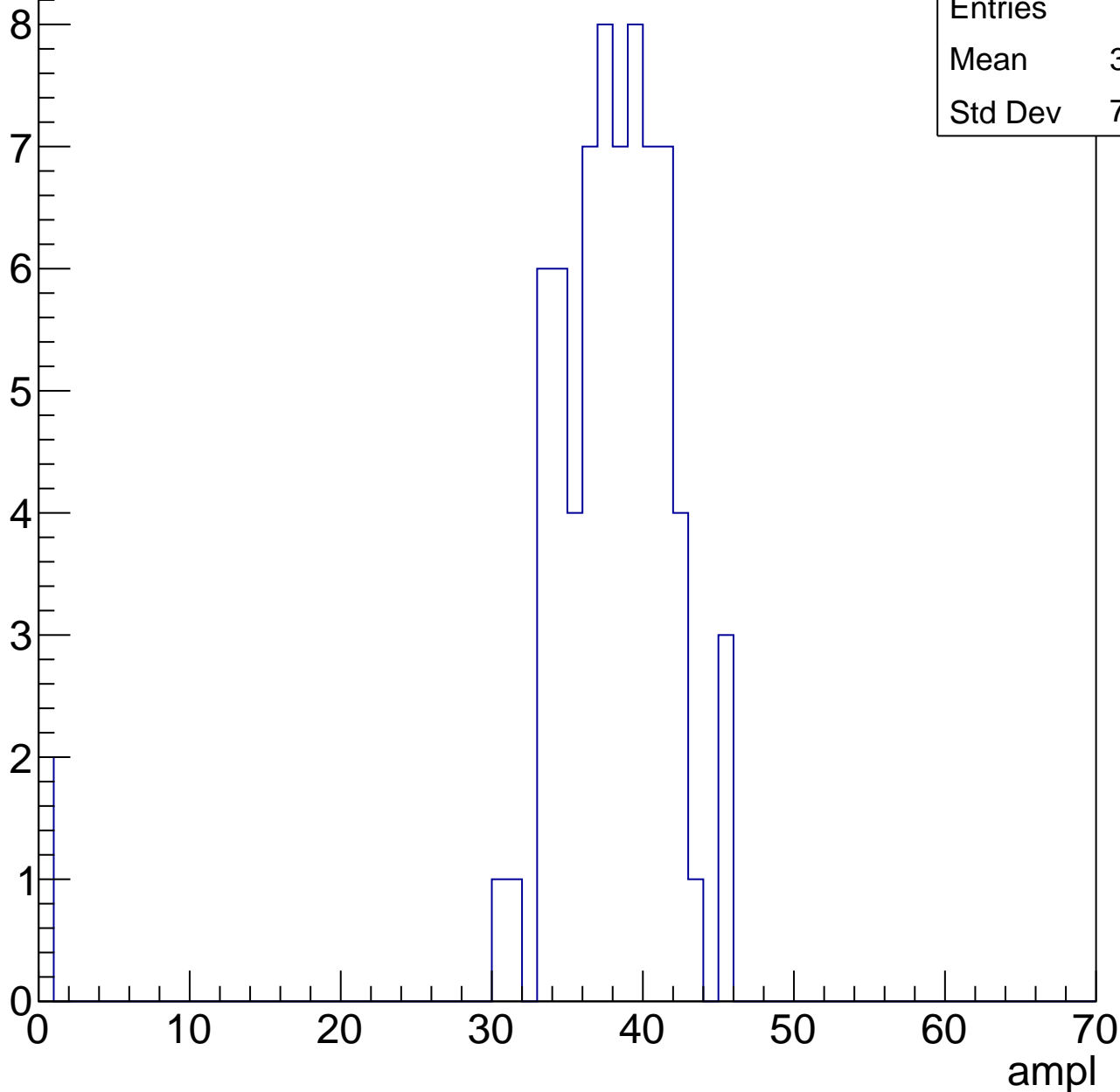


B1L103S, U11-ch63, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	36.69
Std Dev	7.003



B1L103S, U11-ch63, adc2

calib_packv5_041523_1651.root, FC#0, port C2

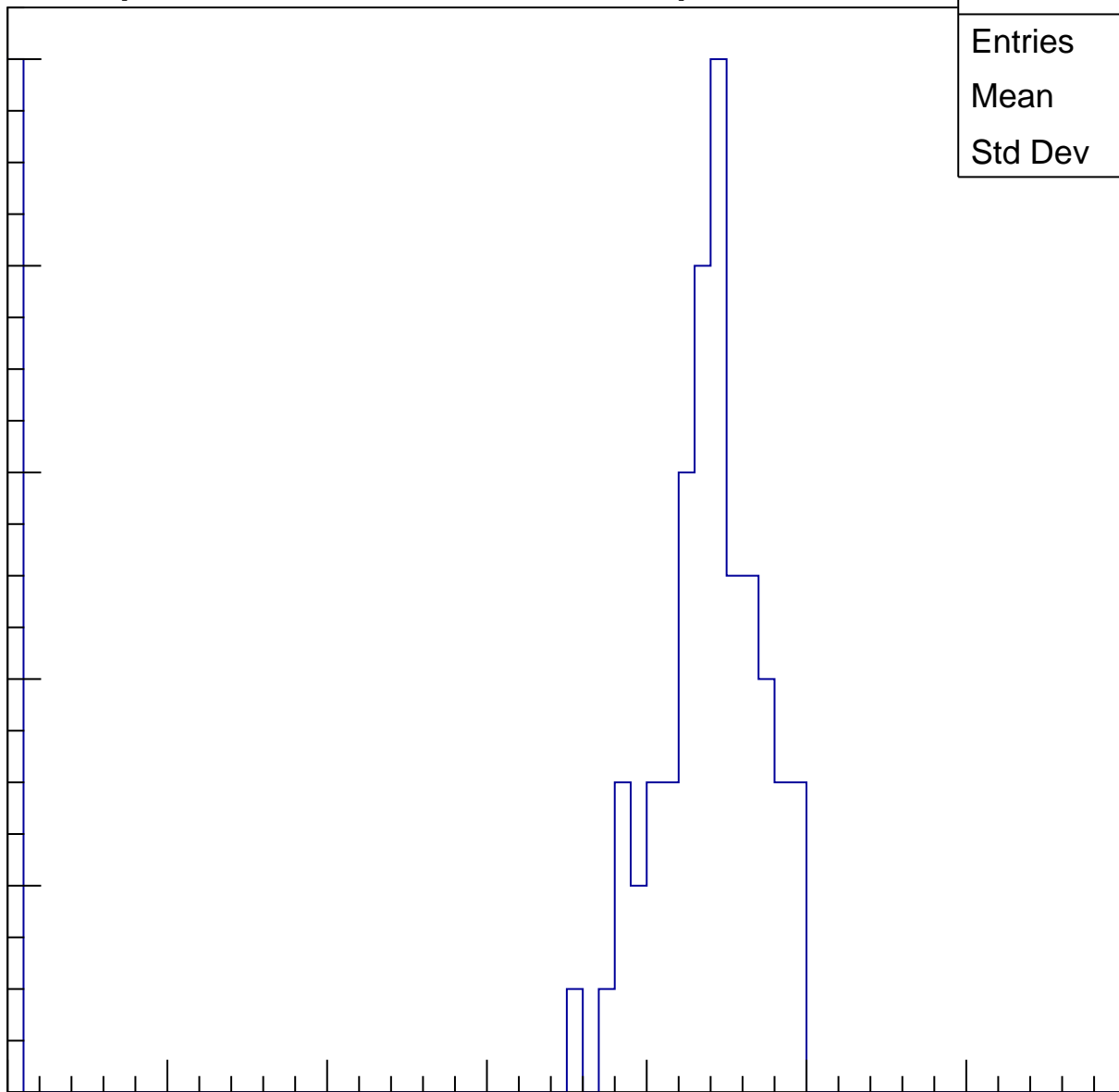
Entries	67
Mean	36.97
Std Dev	15.75

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl



B1L103S, U11-ch63, adc3

calib_packv5_041523_1651.root, FC#0, port C2

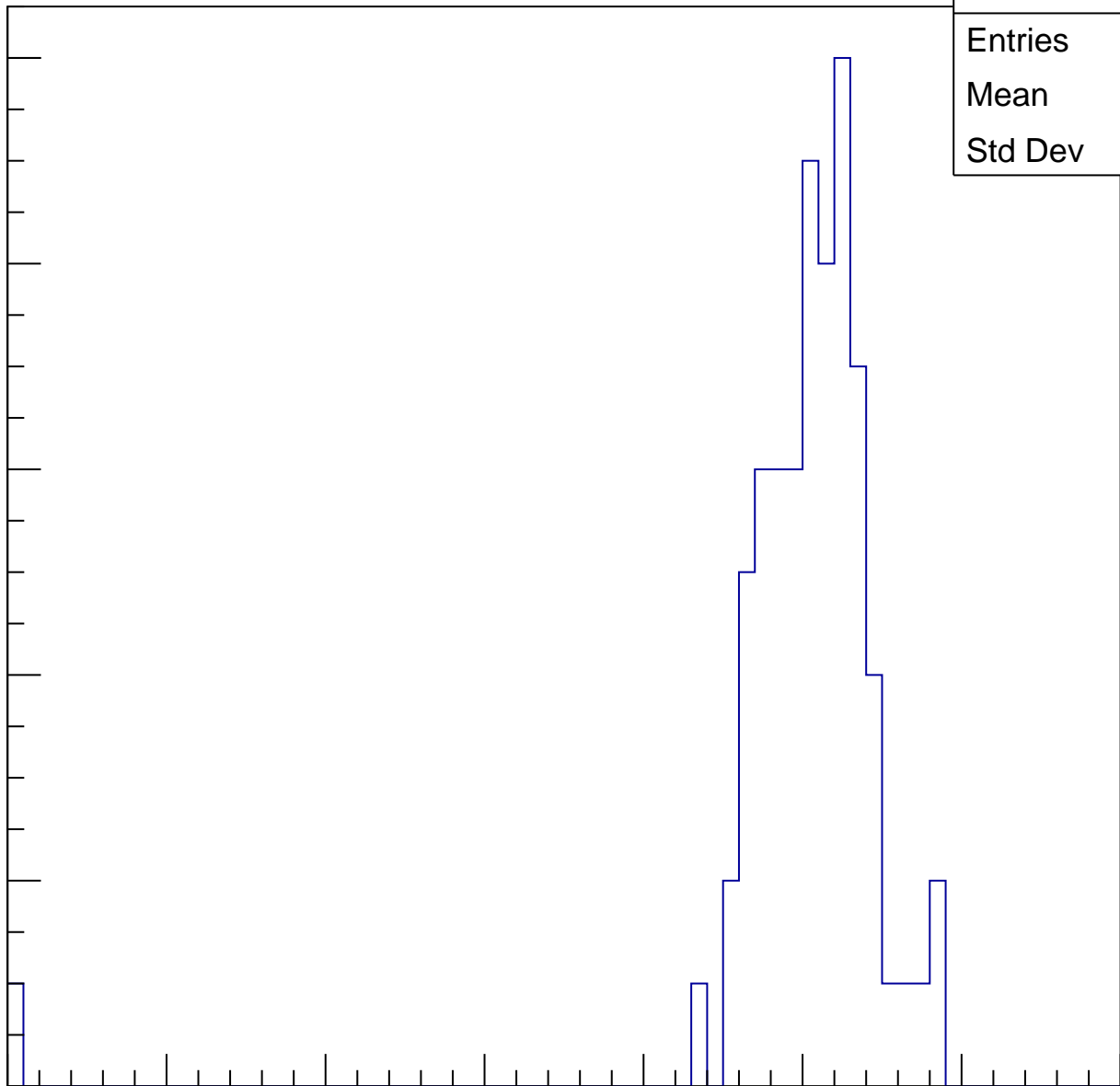
Entries	70
Mean	49.66
Std Dev	6.727

Entry

10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

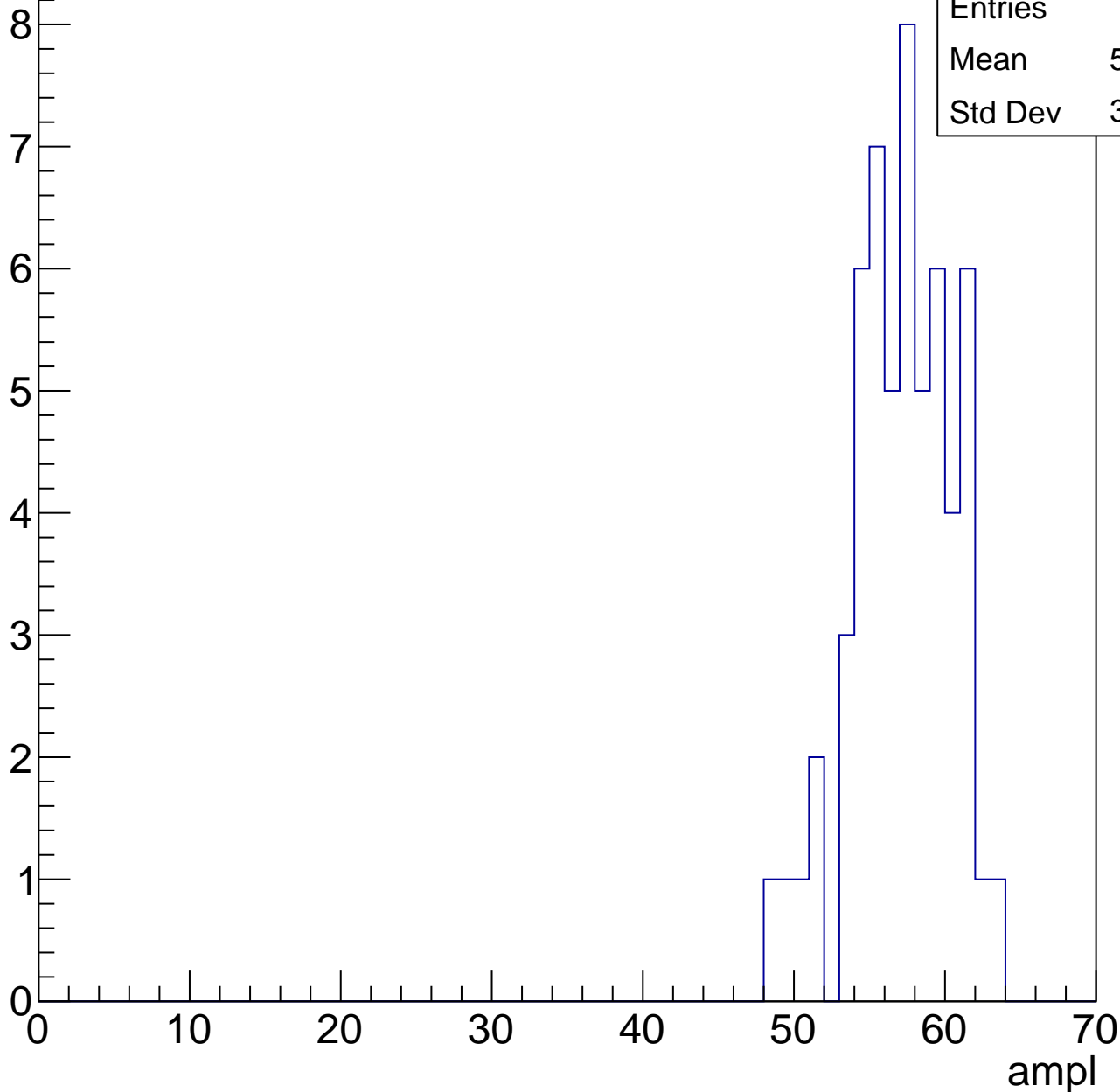


B1L103S, U11-ch63, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	56.63
Std Dev	3.285

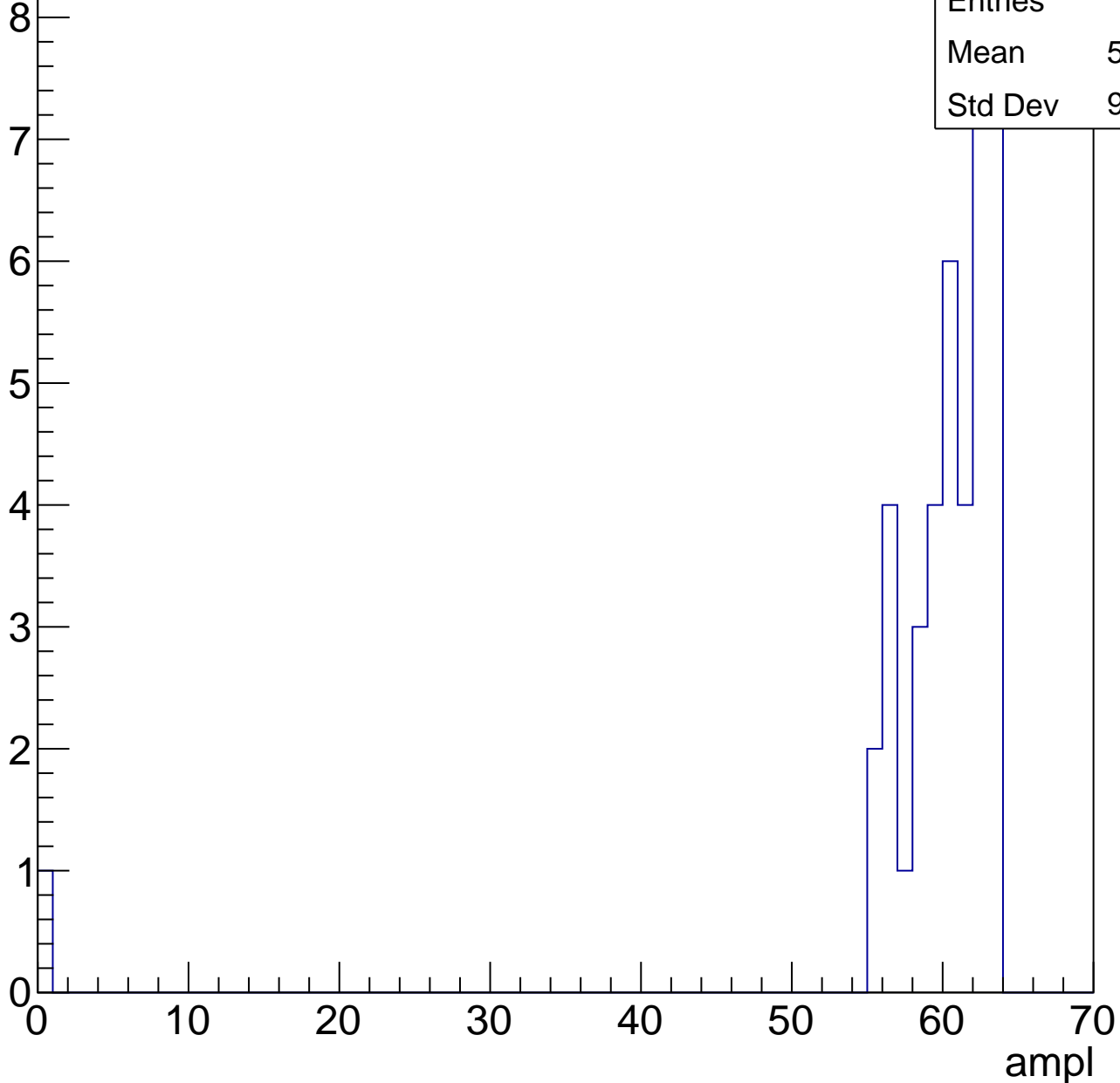


B1L103S, U11-ch63, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	41
Mean	58.66
Std Dev	9.593



B1L103S, U11-ch63, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch63, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.211
Std Dev	5.136

Entry



B1L103S, U11-ch64, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	76
Mean	24.76
Std Dev	10.62

Entry

10

8

6

4

2

0

ampl

0

10

20

30

40

50

60

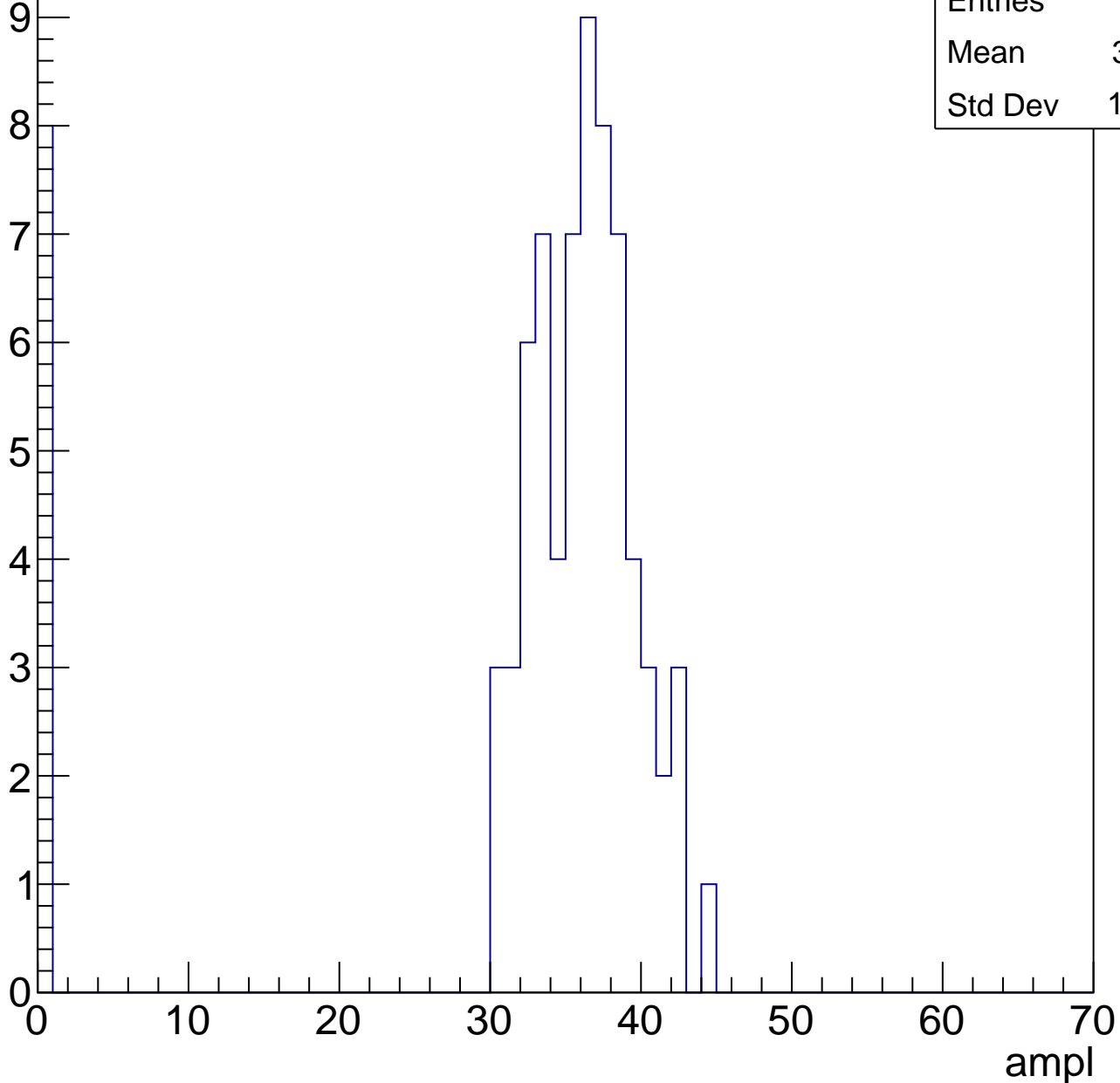
70

B1L103S, U11-ch64, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	32.01
Std Dev	11.48

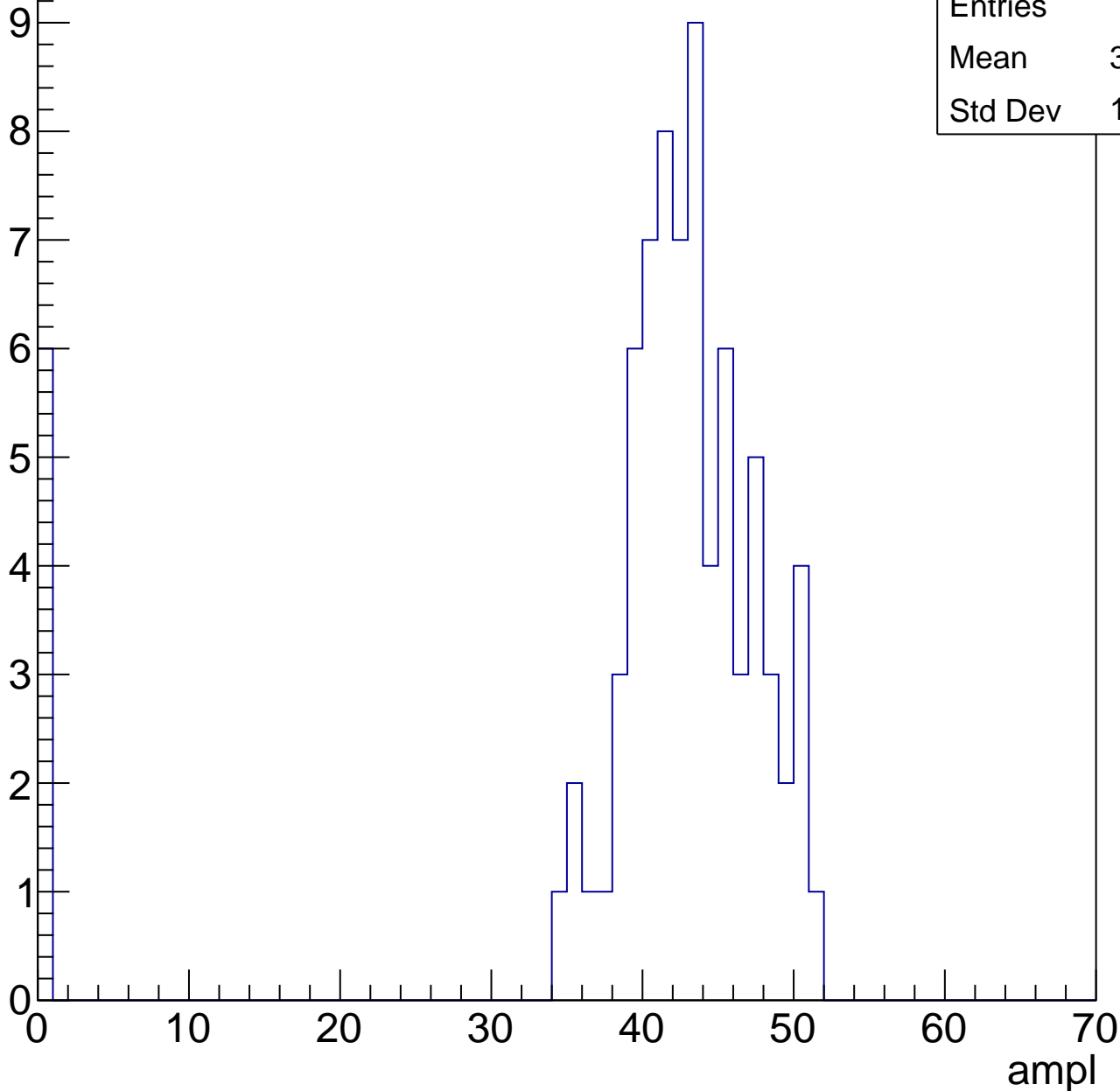


B1L103S, U11-ch64, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	79
Mean	39.57
Std Dev	11.95

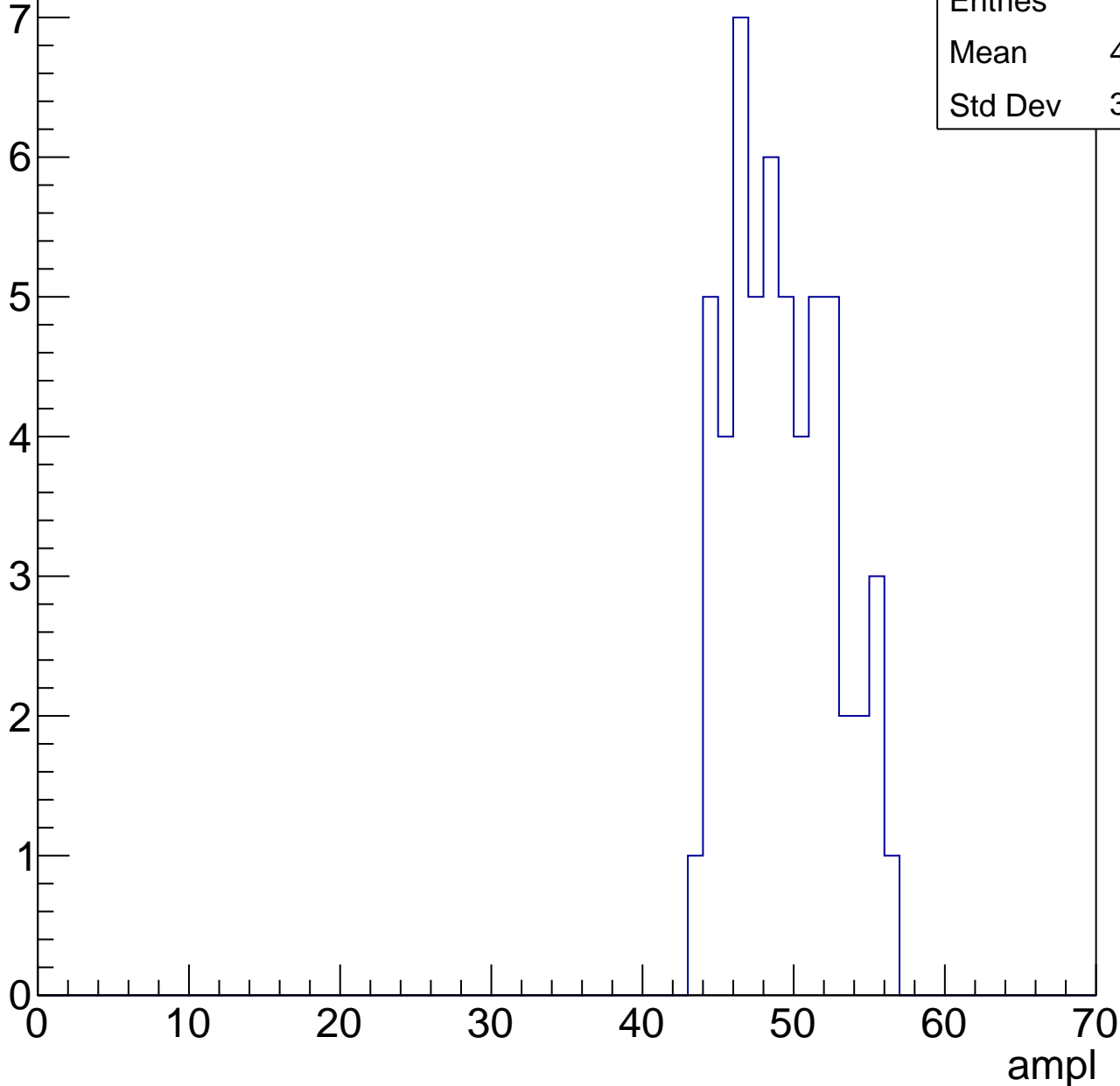


B1L103S, U11-ch64, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	48.78
Std Dev	3.356

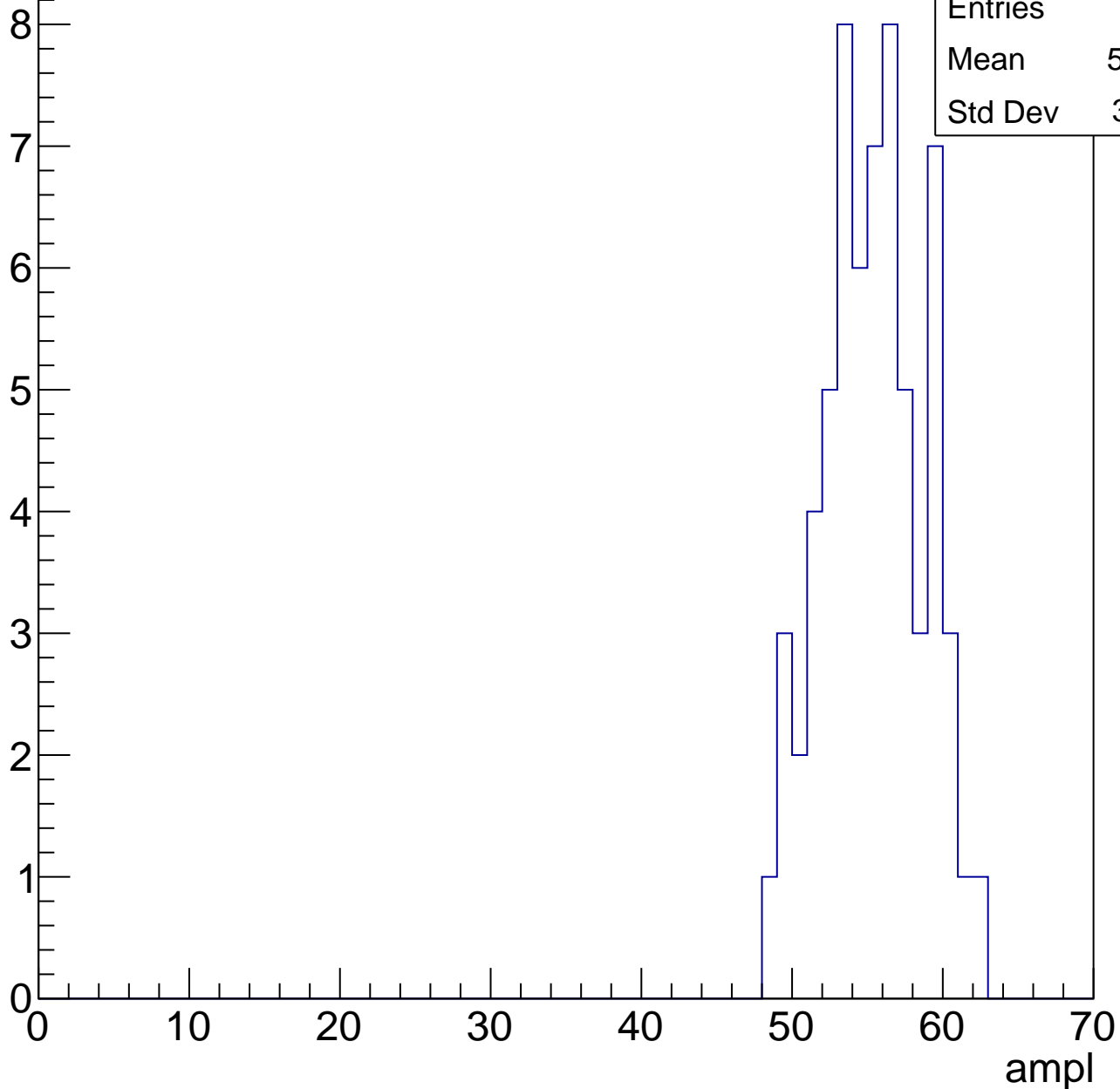


B1L103S, U11-ch64, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	54.92
Std Dev	3.261

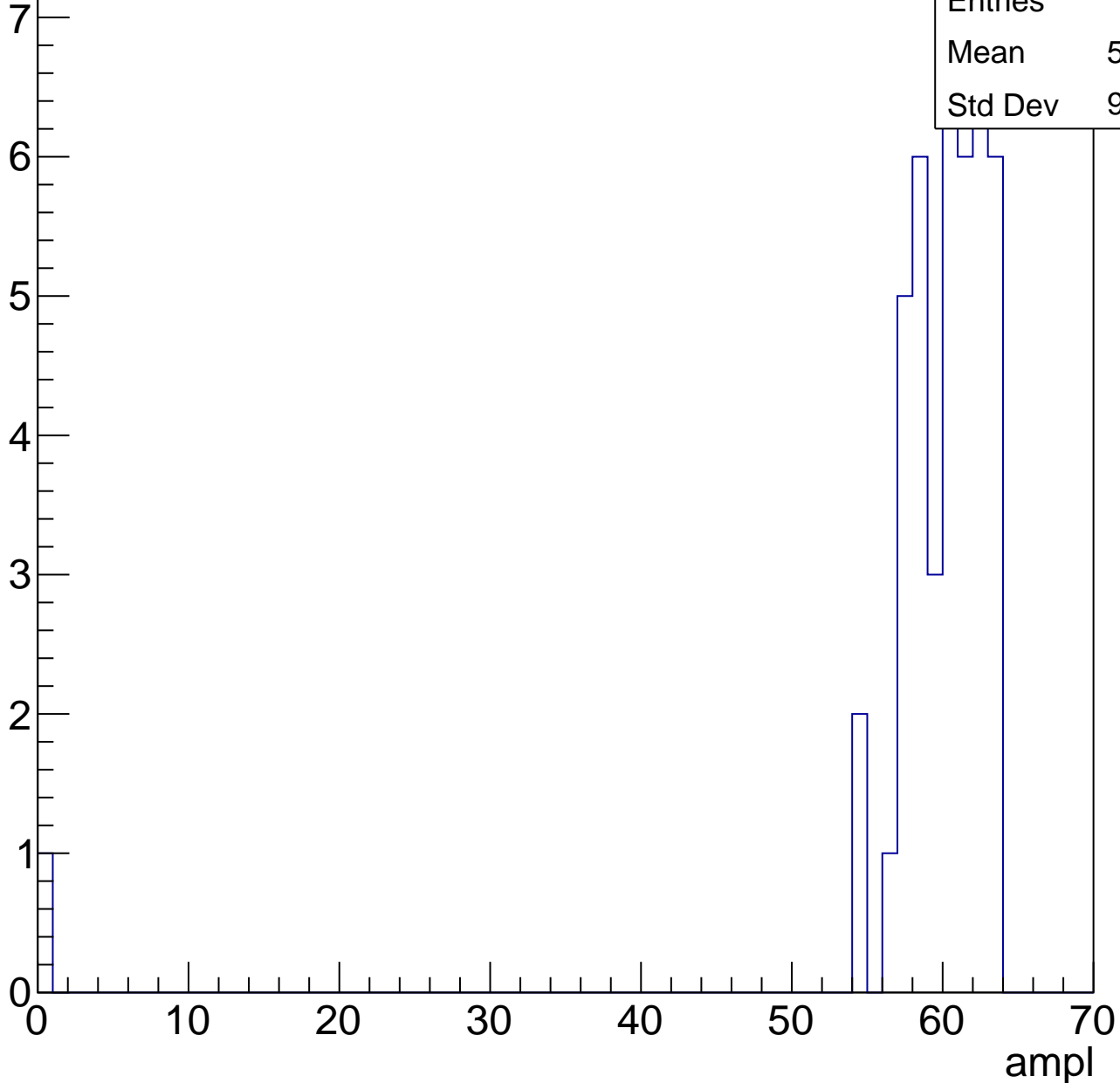


B1L103S, U11-ch64, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

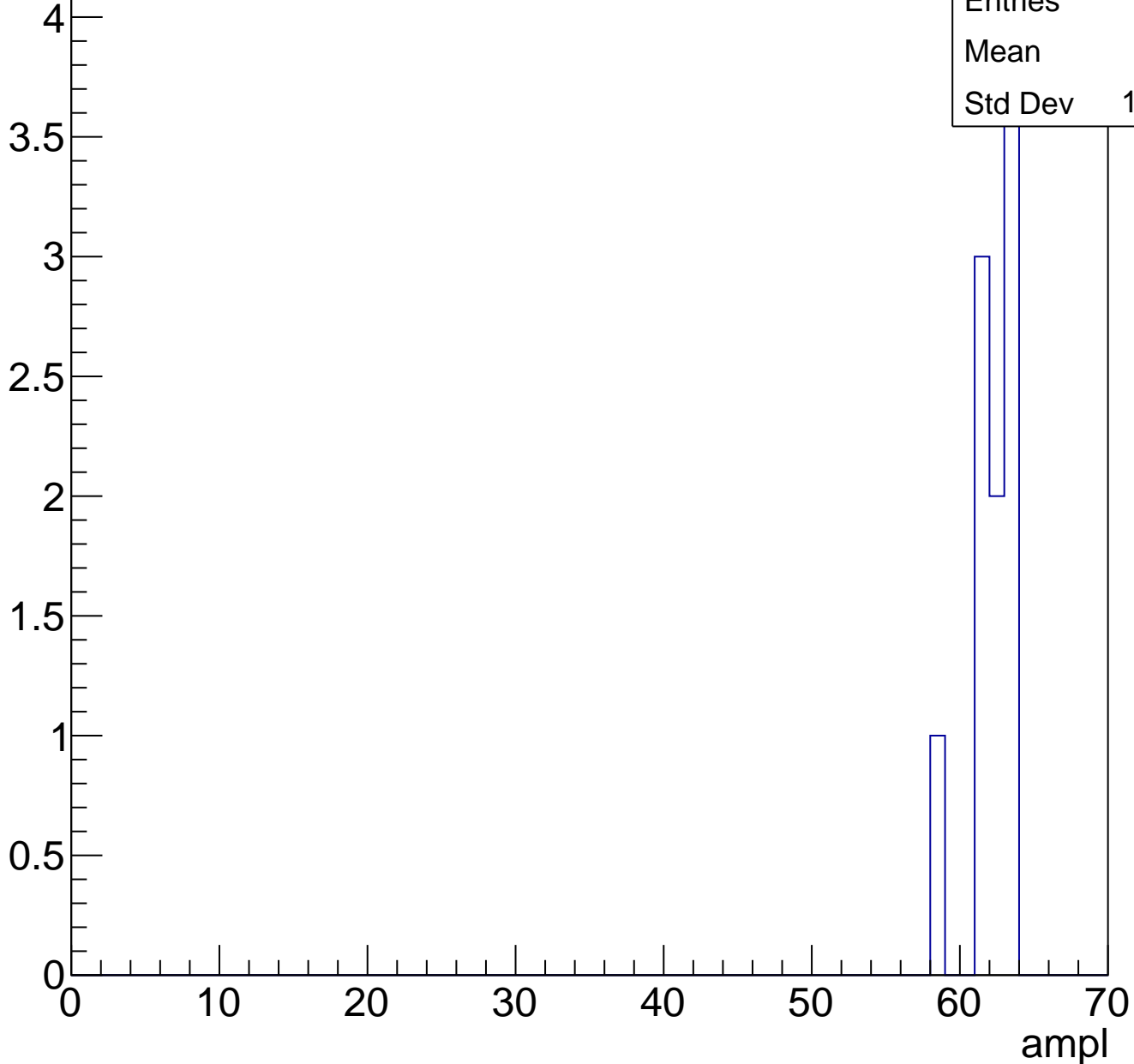
Entries	44
Mean	58.45
Std Dev	9.223



B1L103S, U11-ch64, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

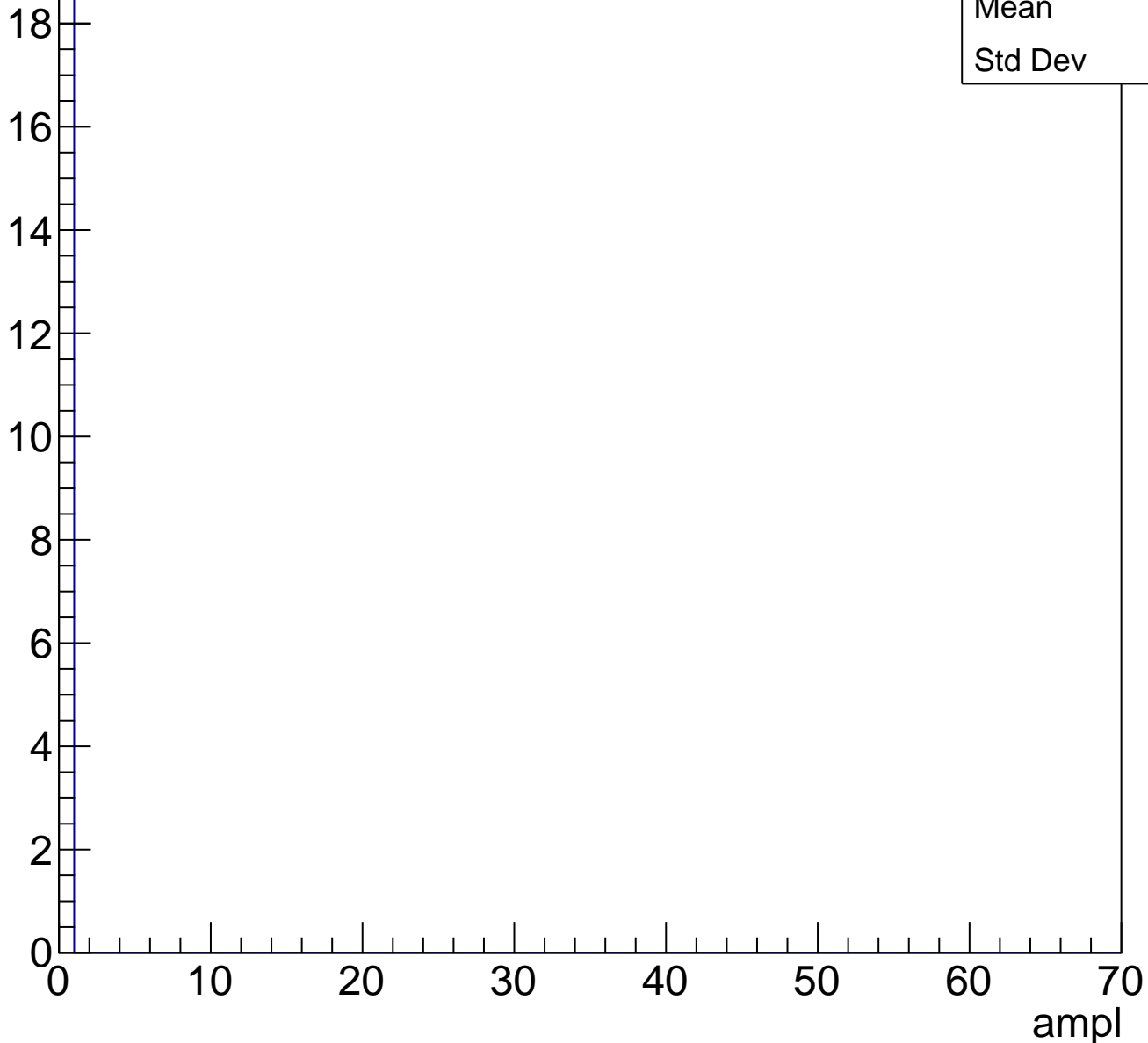


B1L103S, U11-ch64, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	0
Std Dev	0

Entry



B1L103S, U11-ch65, adc0

calib_packv5_041523_1651.root, FC#0, port C2

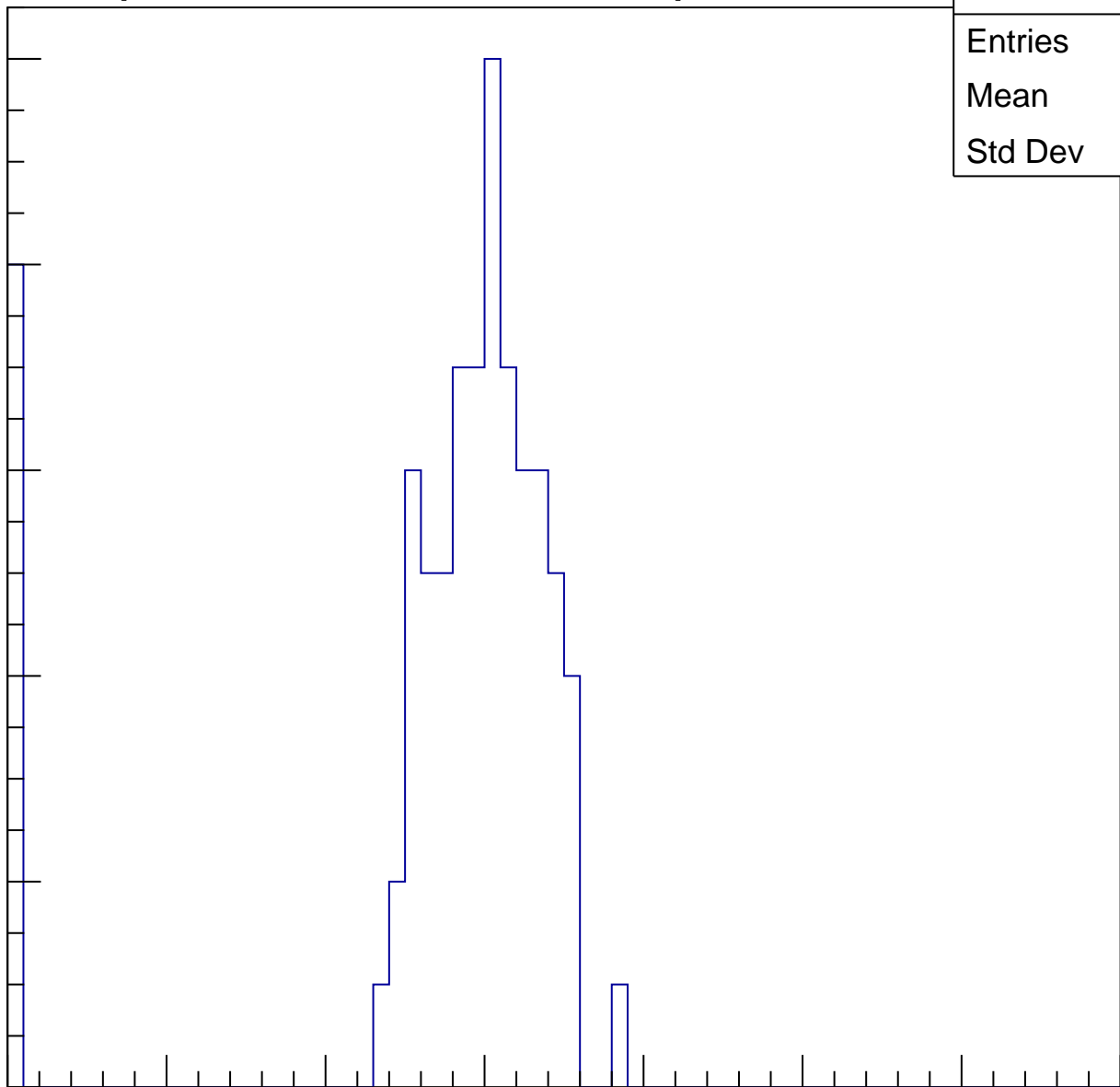
Entries	80
Mean	26.75
Std Dev	9.431

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

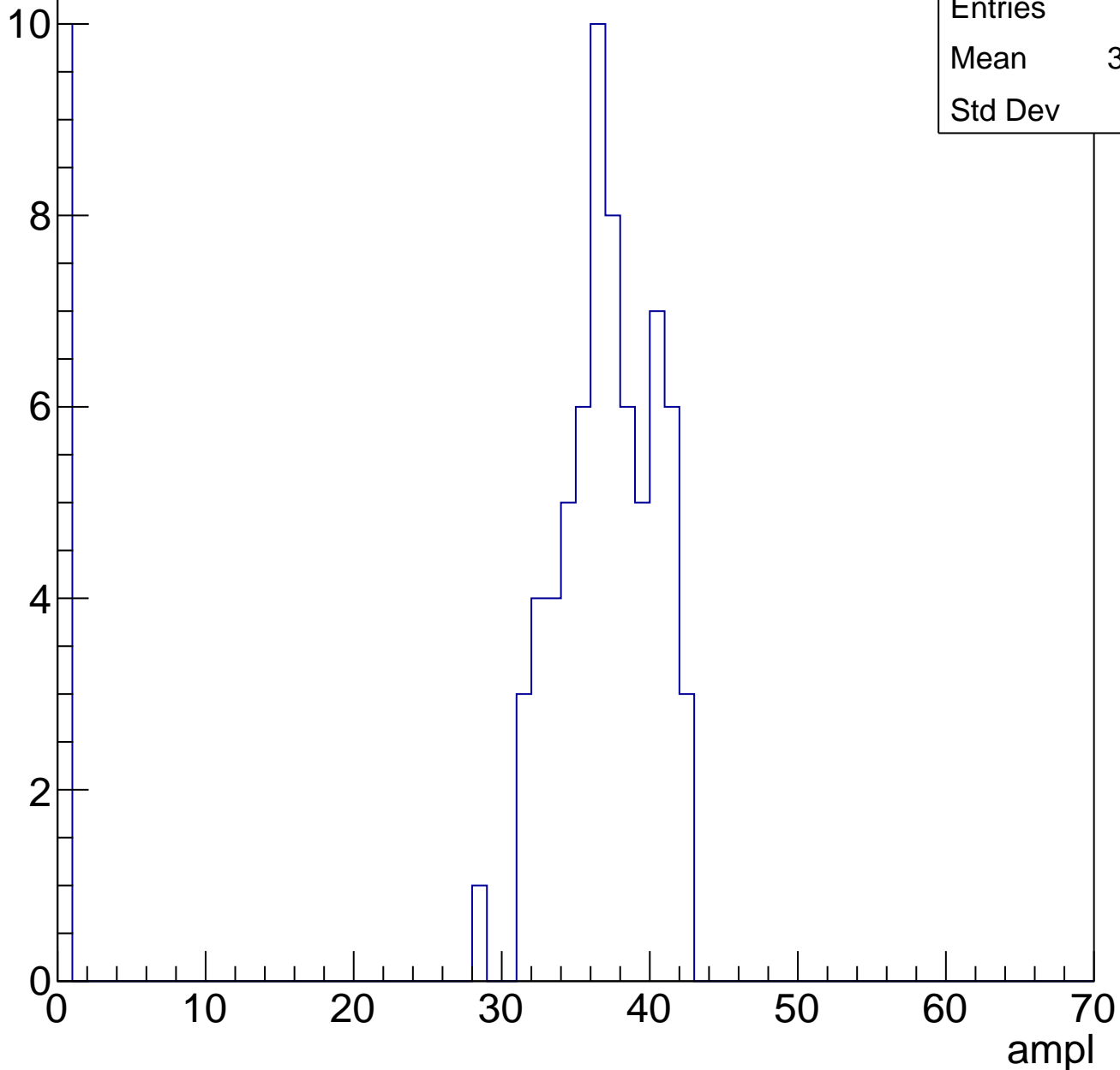


B1L103S, U11-ch65, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	78
Mean	31.95
Std Dev	12.6

Entry

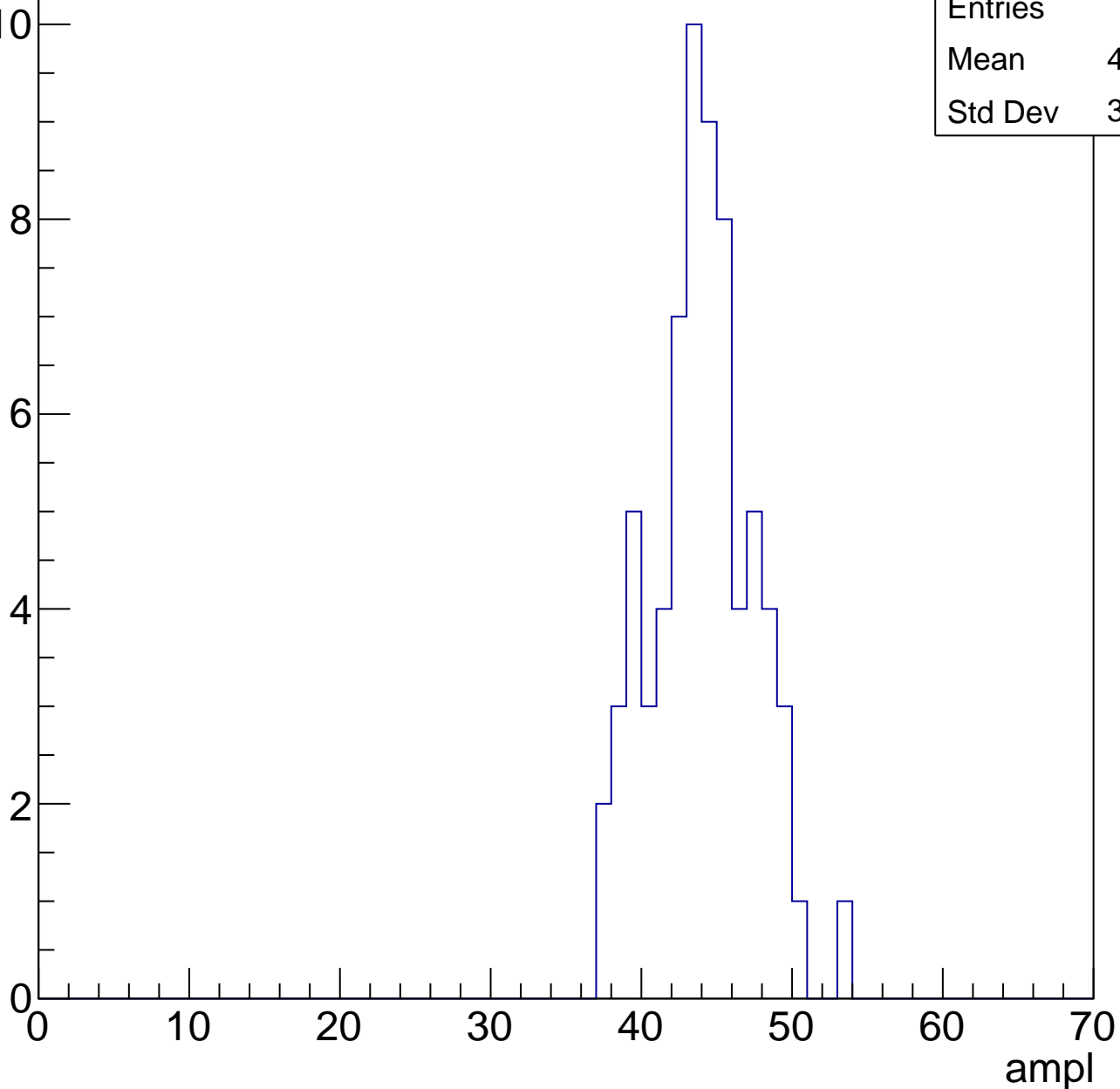


B1L103S, U11-ch65, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	43.59
Std Dev	3.333

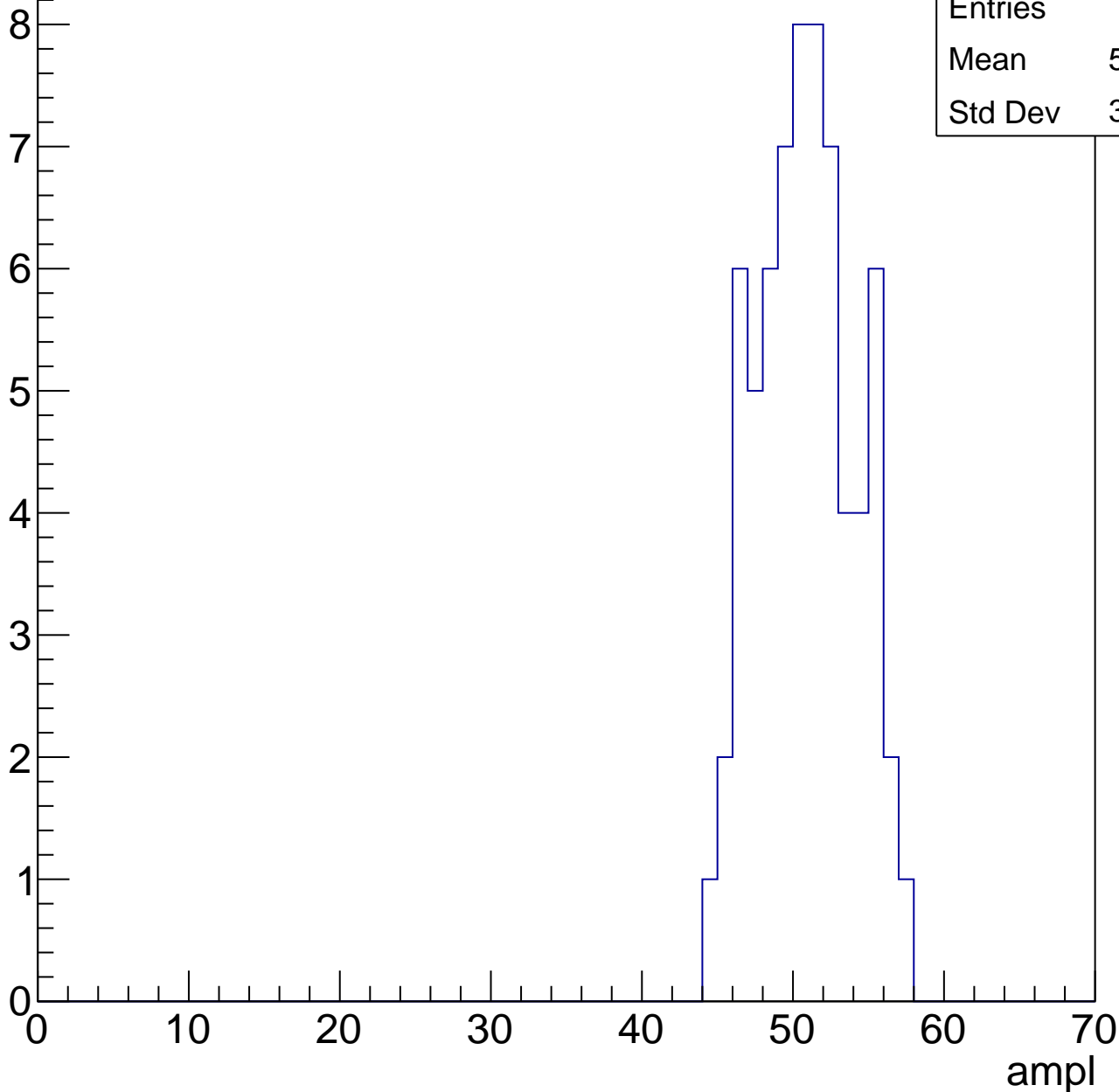


B1L103S, U11-ch65, adc3

calib_packv5_041523_1651.root, FC#0, port C2

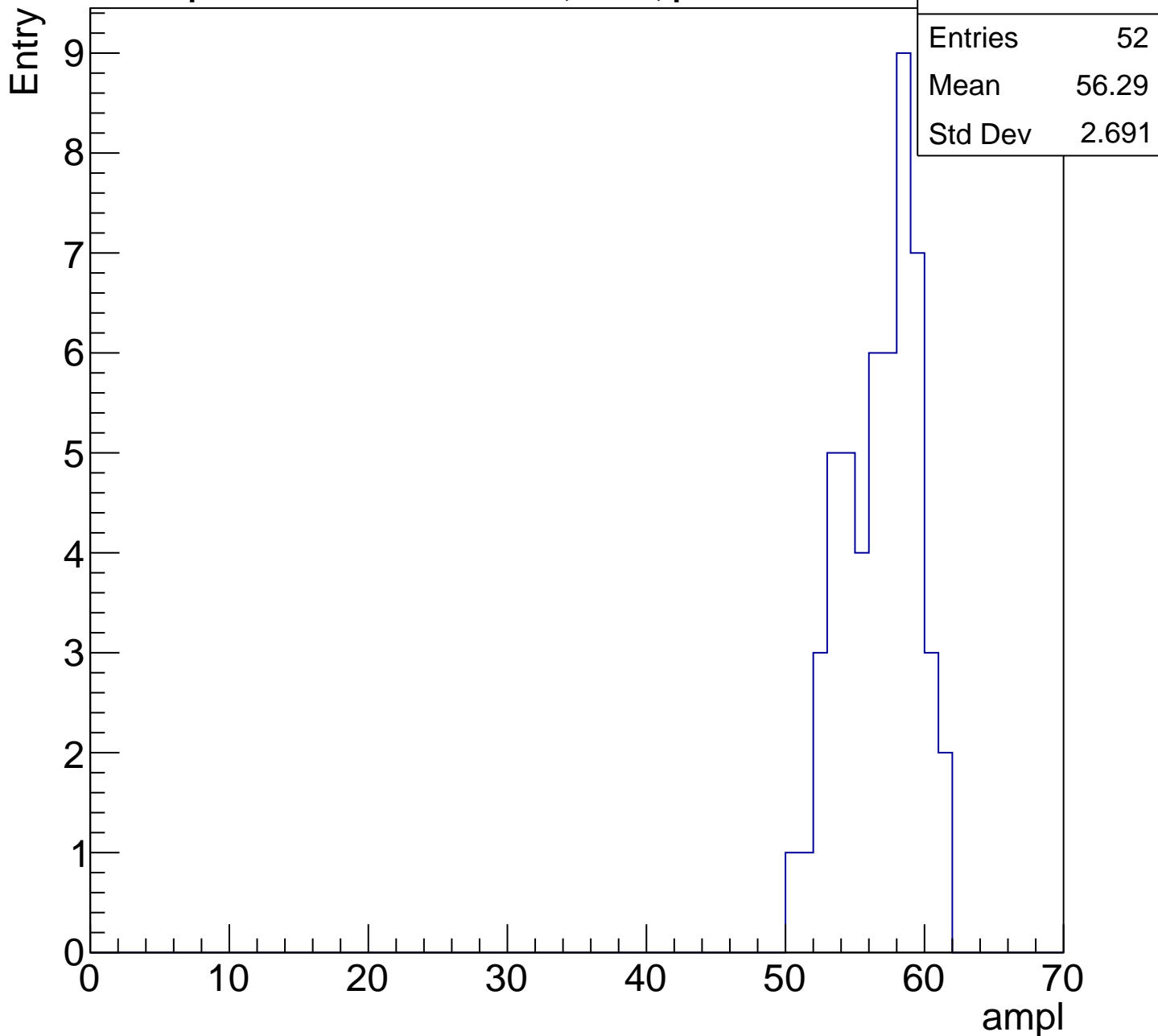
Entry

Entries	67
Mean	50.37
Std Dev	3.128



B1L103S, U11-ch65, adc4

calib_packv5_041523_1651.root, FC#0, port C2

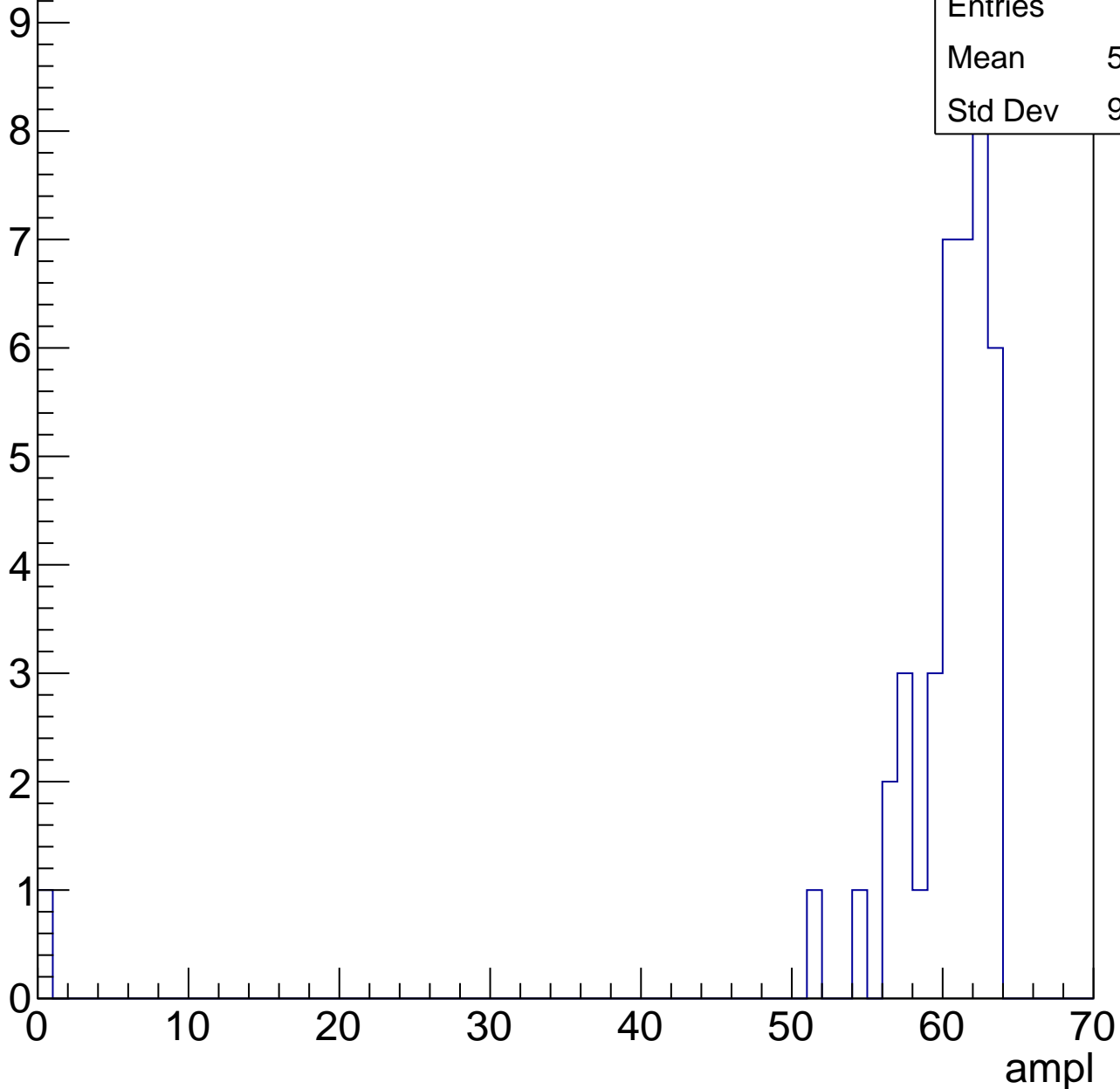


B1L103S, U11-ch65, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	41
Mean	58.68
Std Dev	9.638



B1L103S, U11-ch65, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch65, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

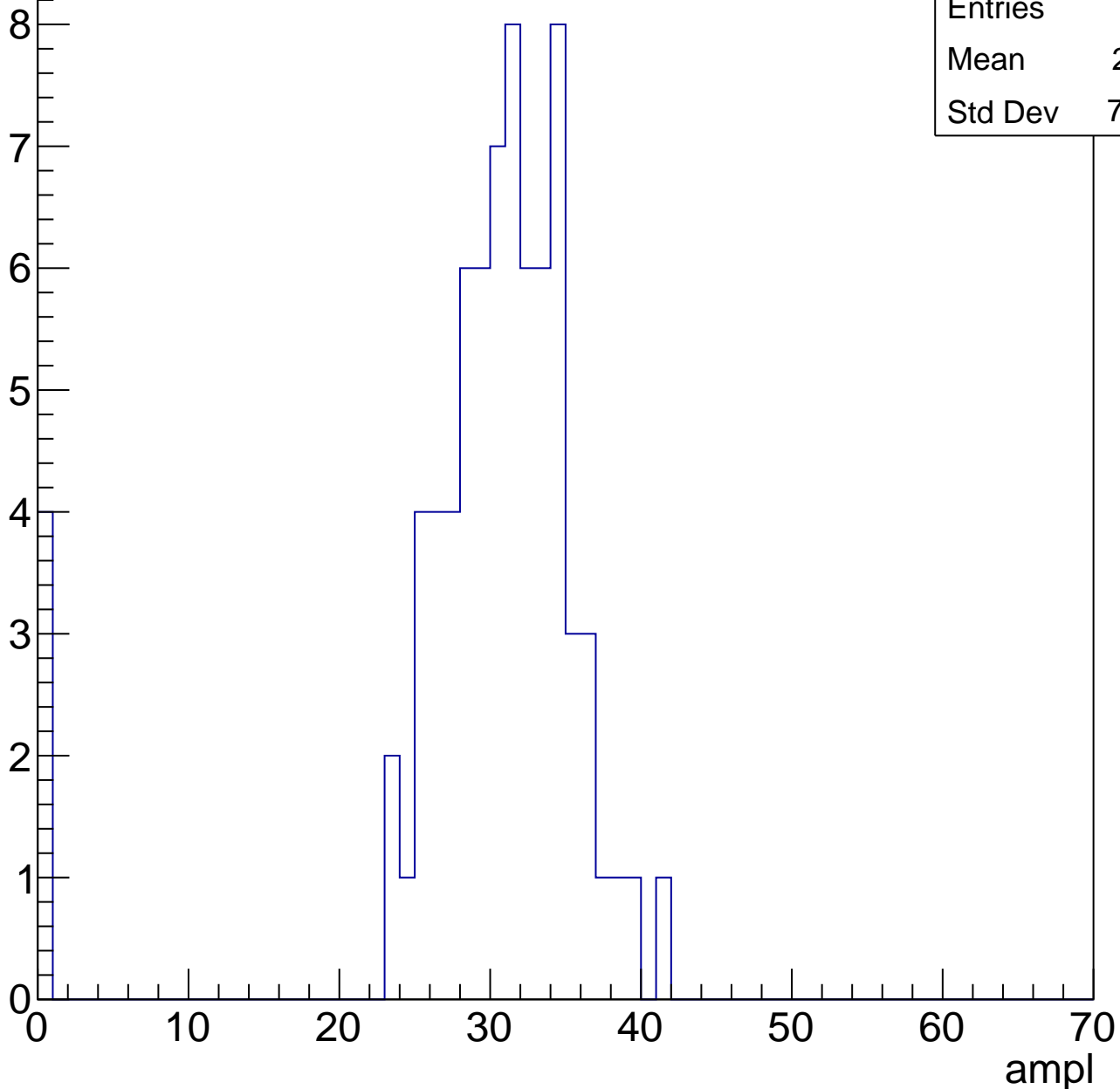
Entries	19
Mean	0
Std Dev	0

B1L103S, U11-ch66, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	29.11
Std Dev	7.793

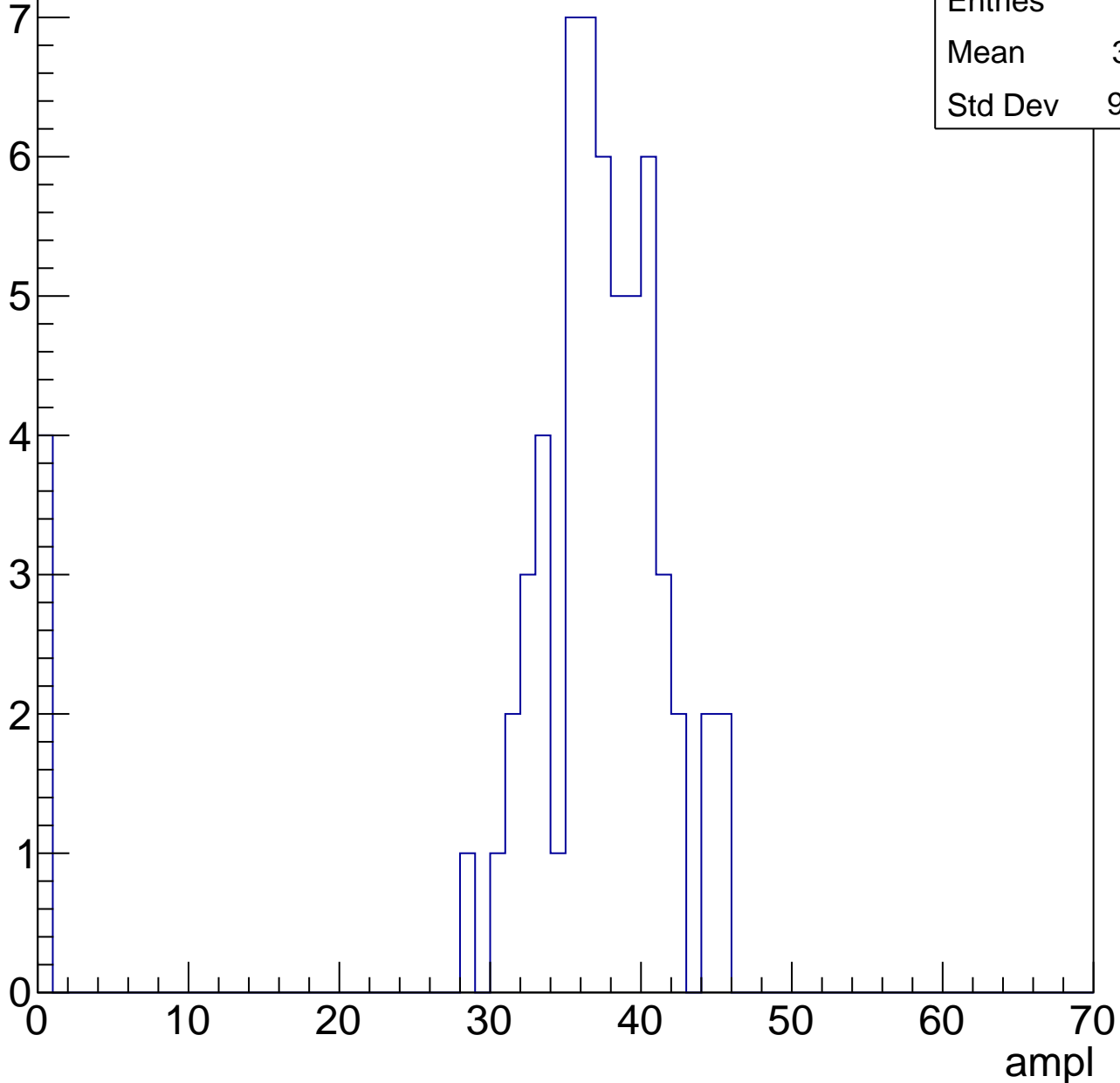


B1L103S, U11-ch66, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	34.61
Std Dev	9.847

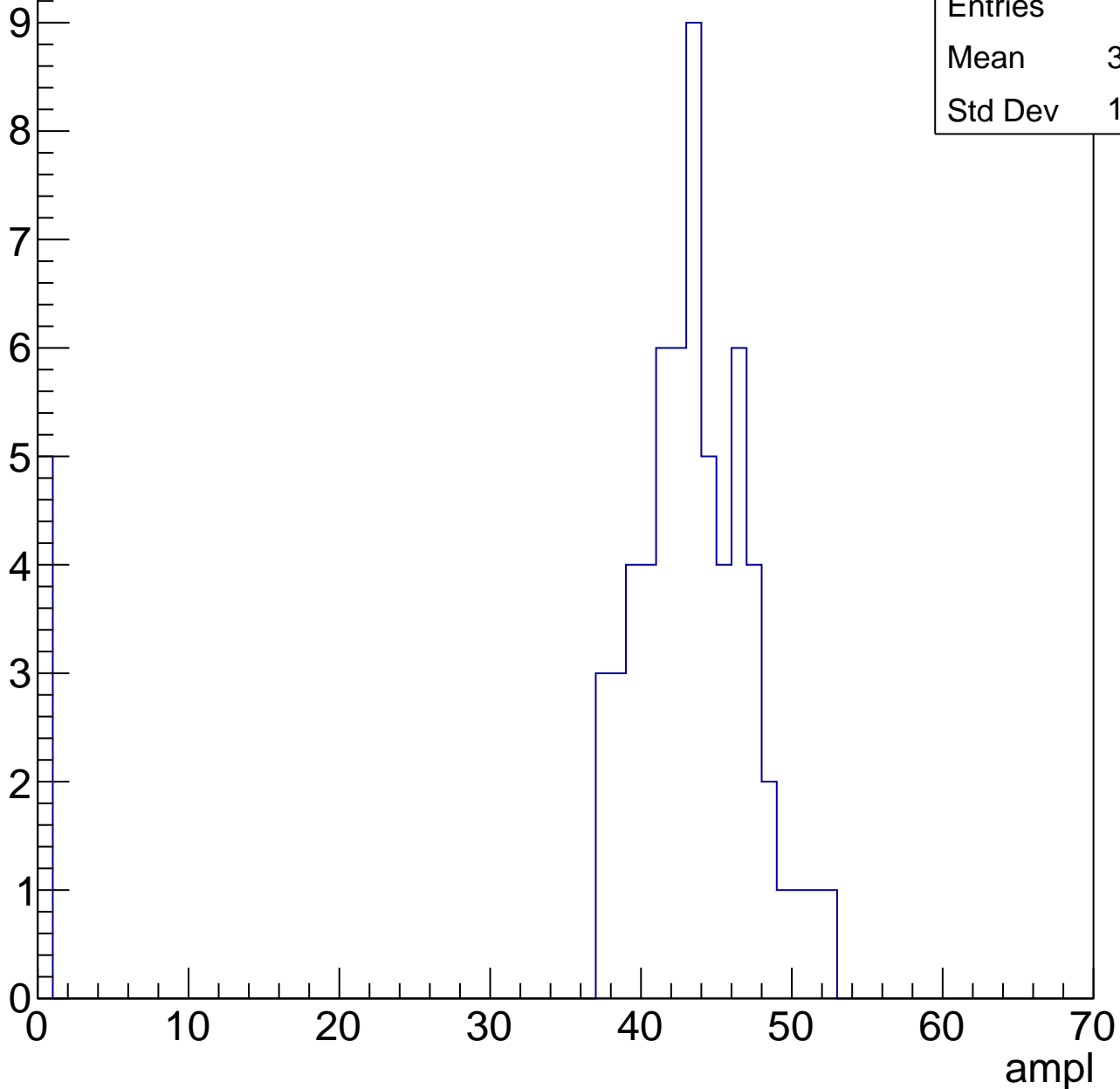


B1L103S, U11-ch66, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

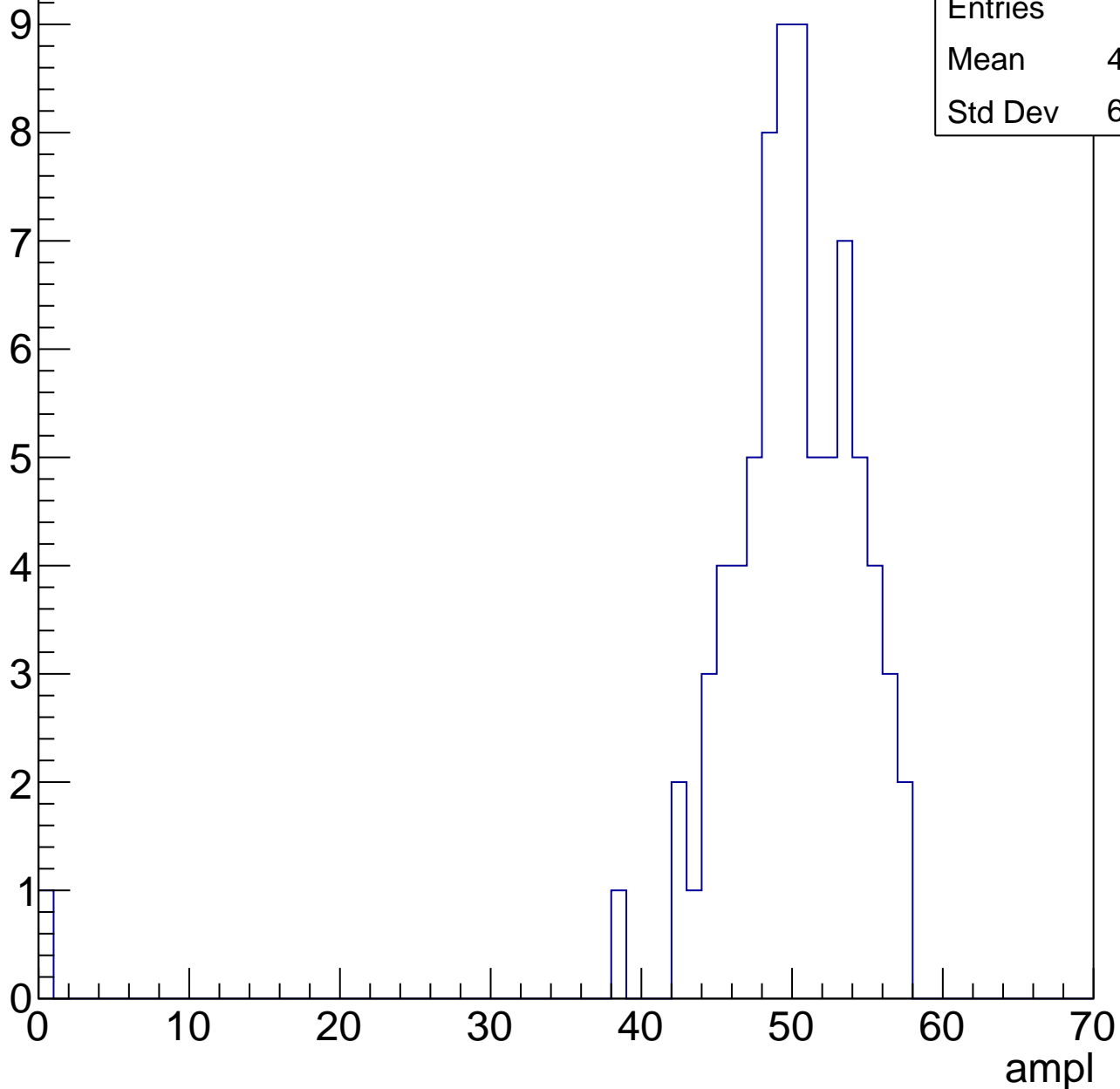
Entries	65
Mean	39.82
Std Dev	11.97



B1L103S, U11-ch66, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

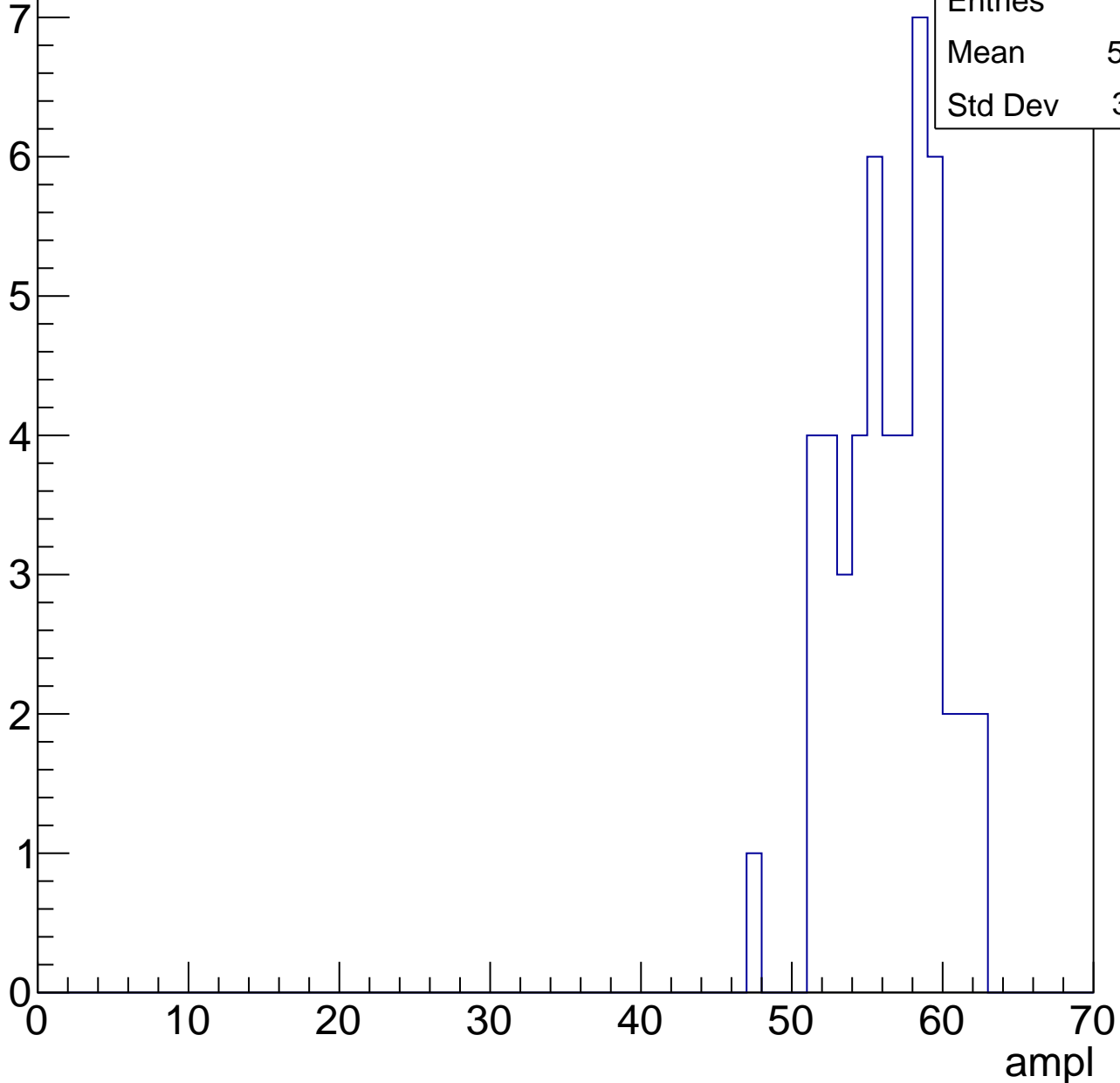


B1L103S, U11-ch66, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	55.96
Std Dev	3.301

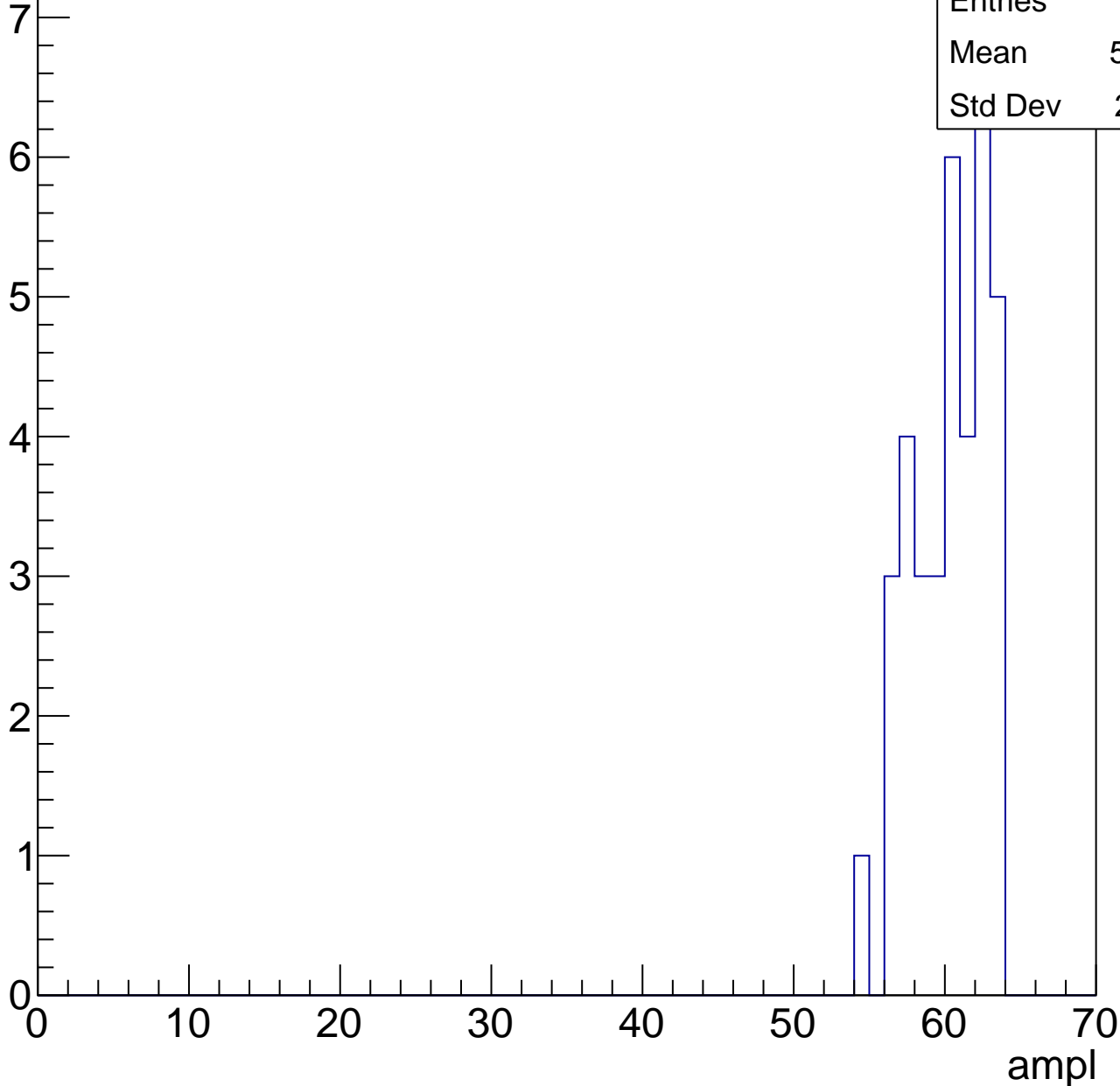


B1L103S, U11-ch66, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	36
Mean	59.83
Std Dev	2.421

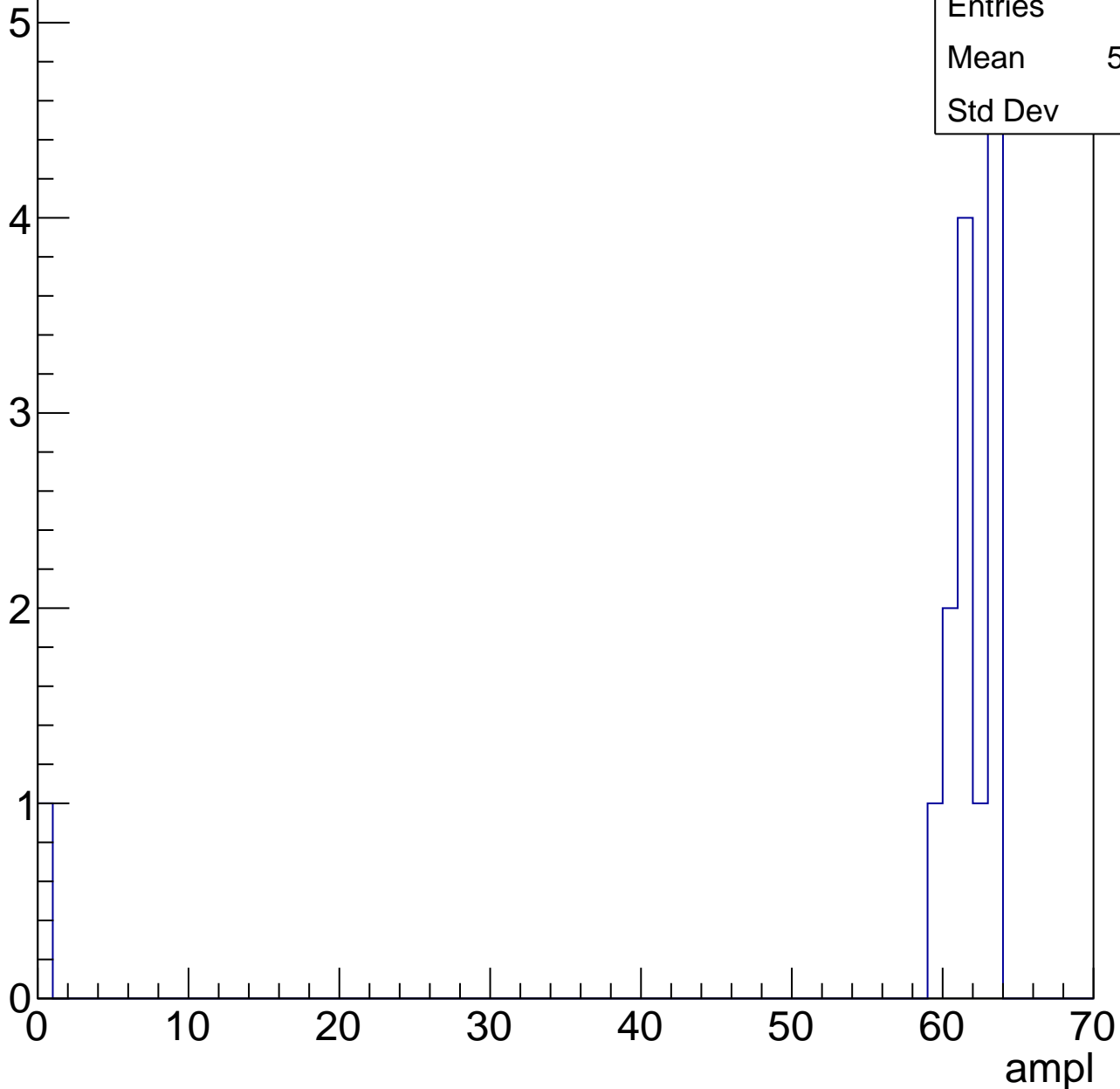


B1L103S, U11-ch66, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	14
Mean	57.14
Std Dev	15.9



B1L103S, U11-ch66, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

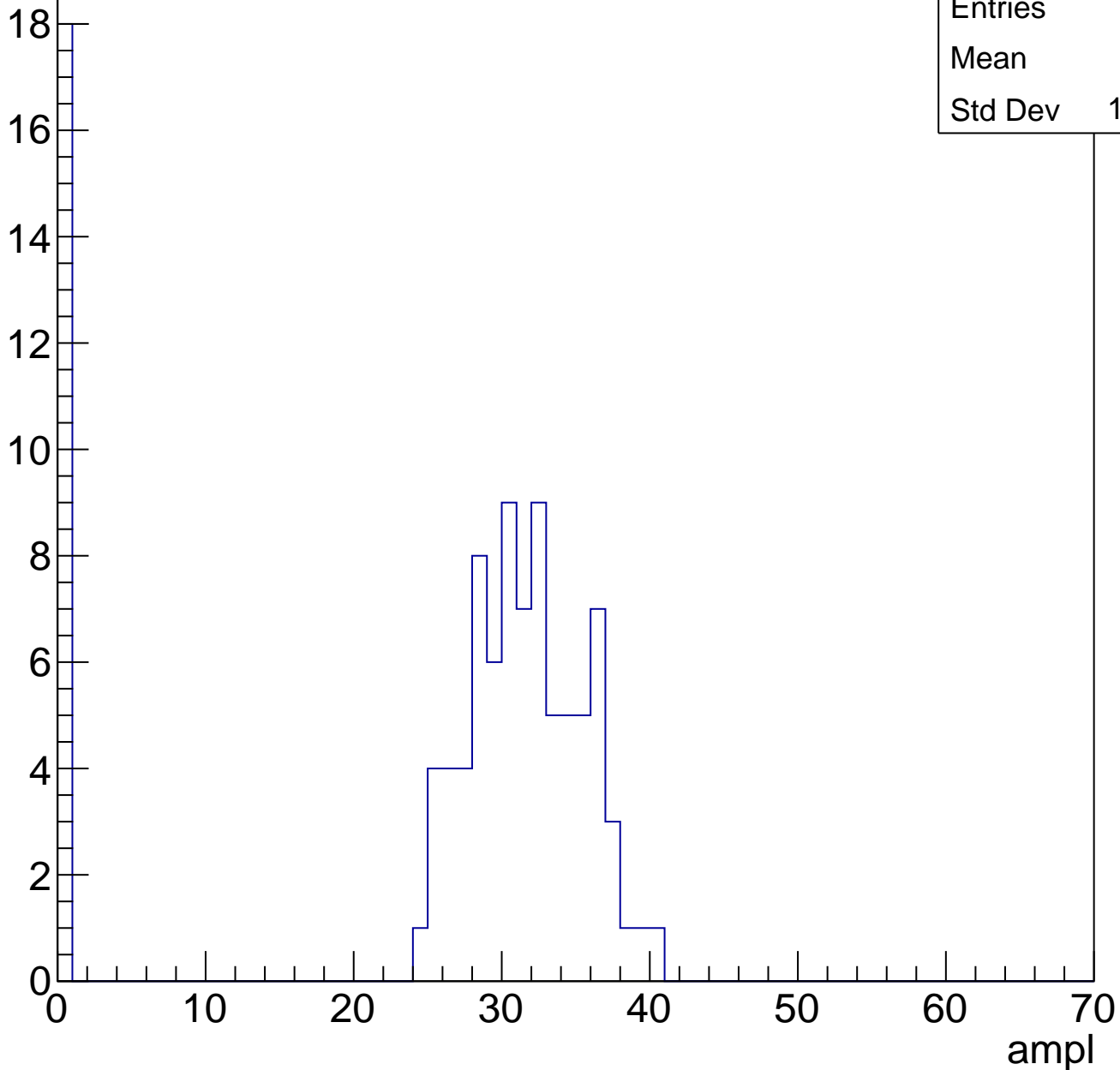


B1L103S, U11-ch67, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	98
Mean	25.5
Std Dev	12.55

Entry

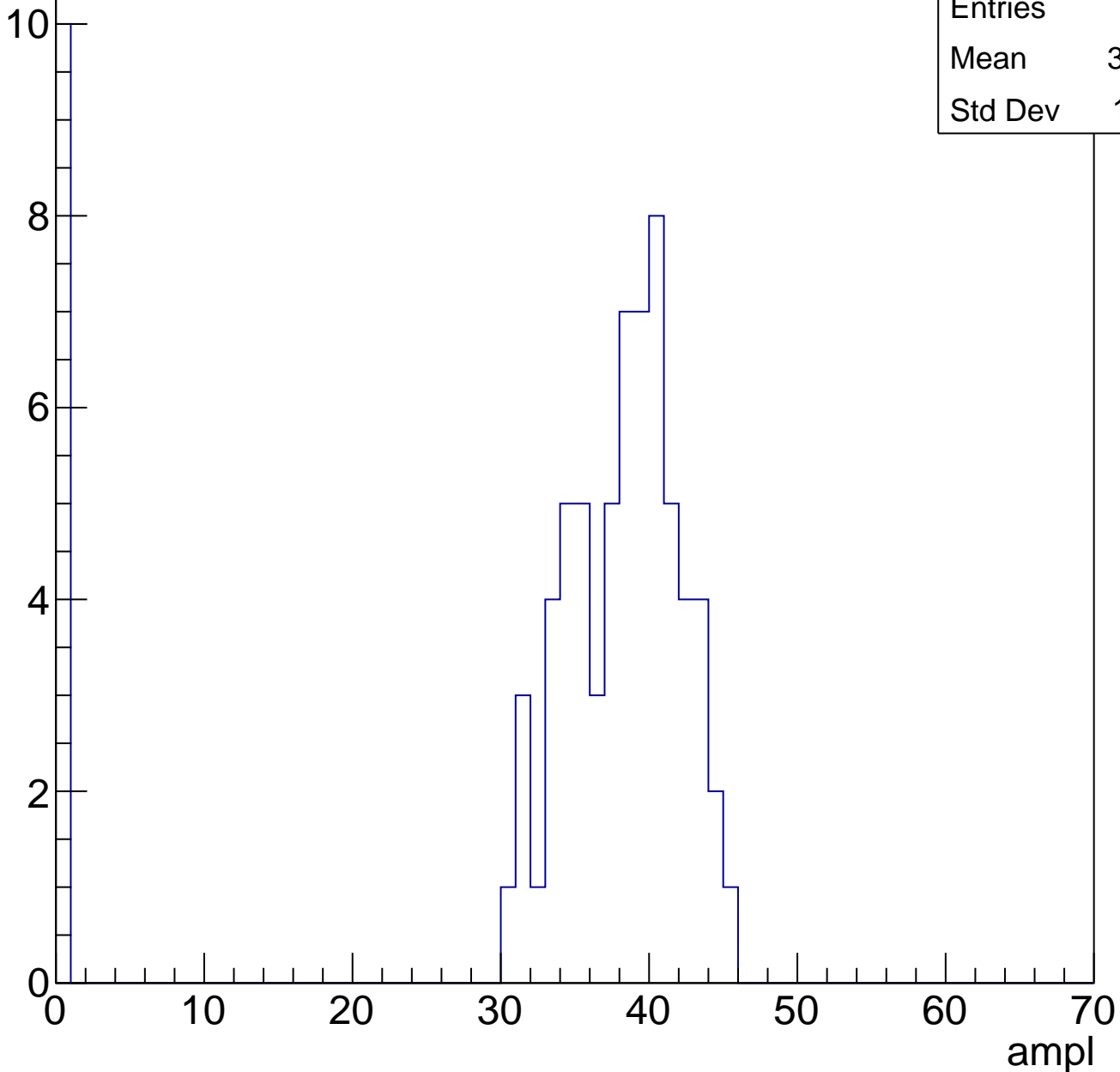


B1L103S, U11-ch67, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	32.83
Std Dev	13.31

Entry

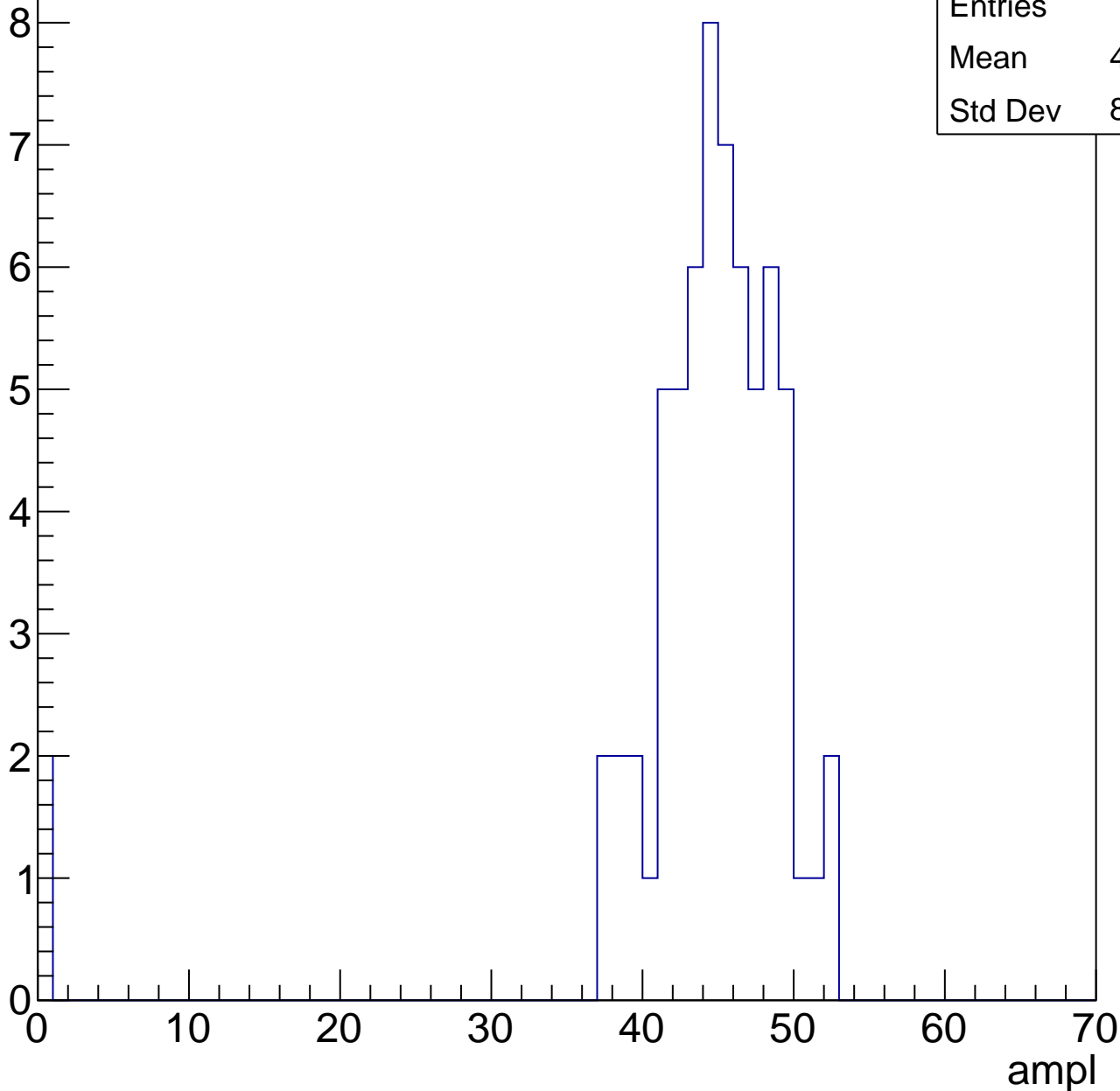


B1L103S, U11-ch67, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	43.29
Std Dev	8.399

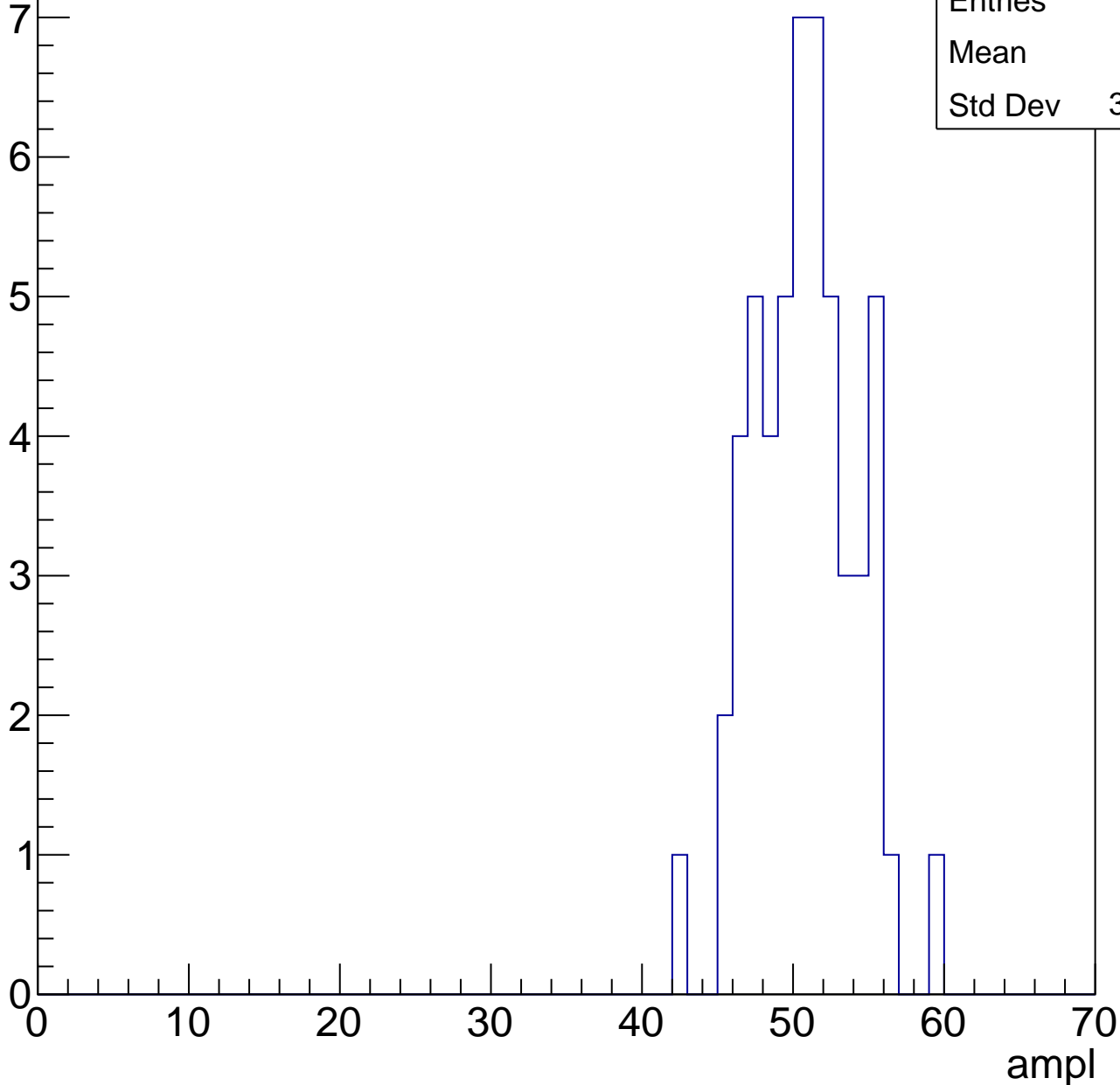


B1L103S, U11-ch67, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	50.3
Std Dev	3.317

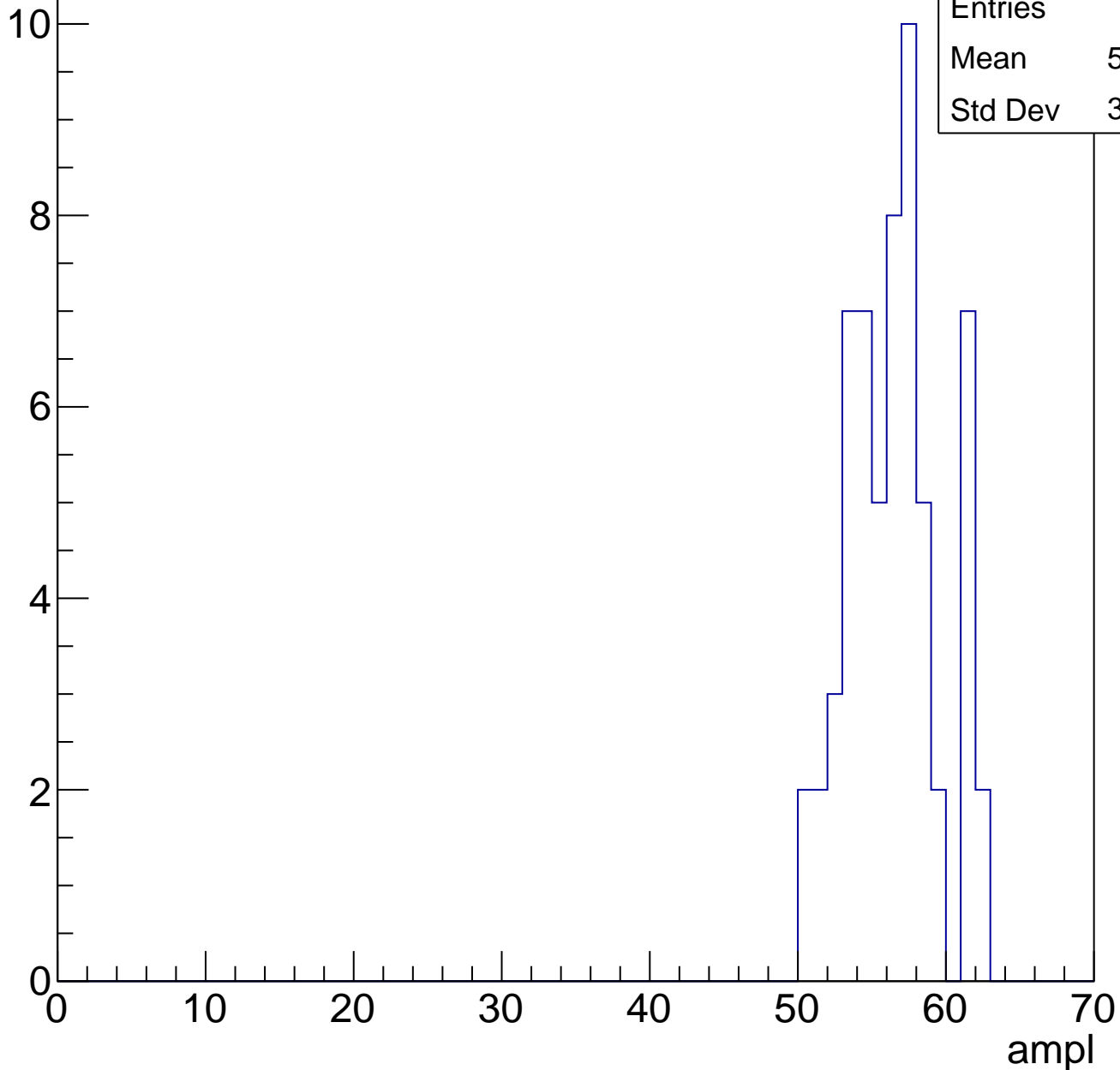


B1L103S, U11-ch67, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	60
Mean	55.98
Std Dev	3.058

Entry

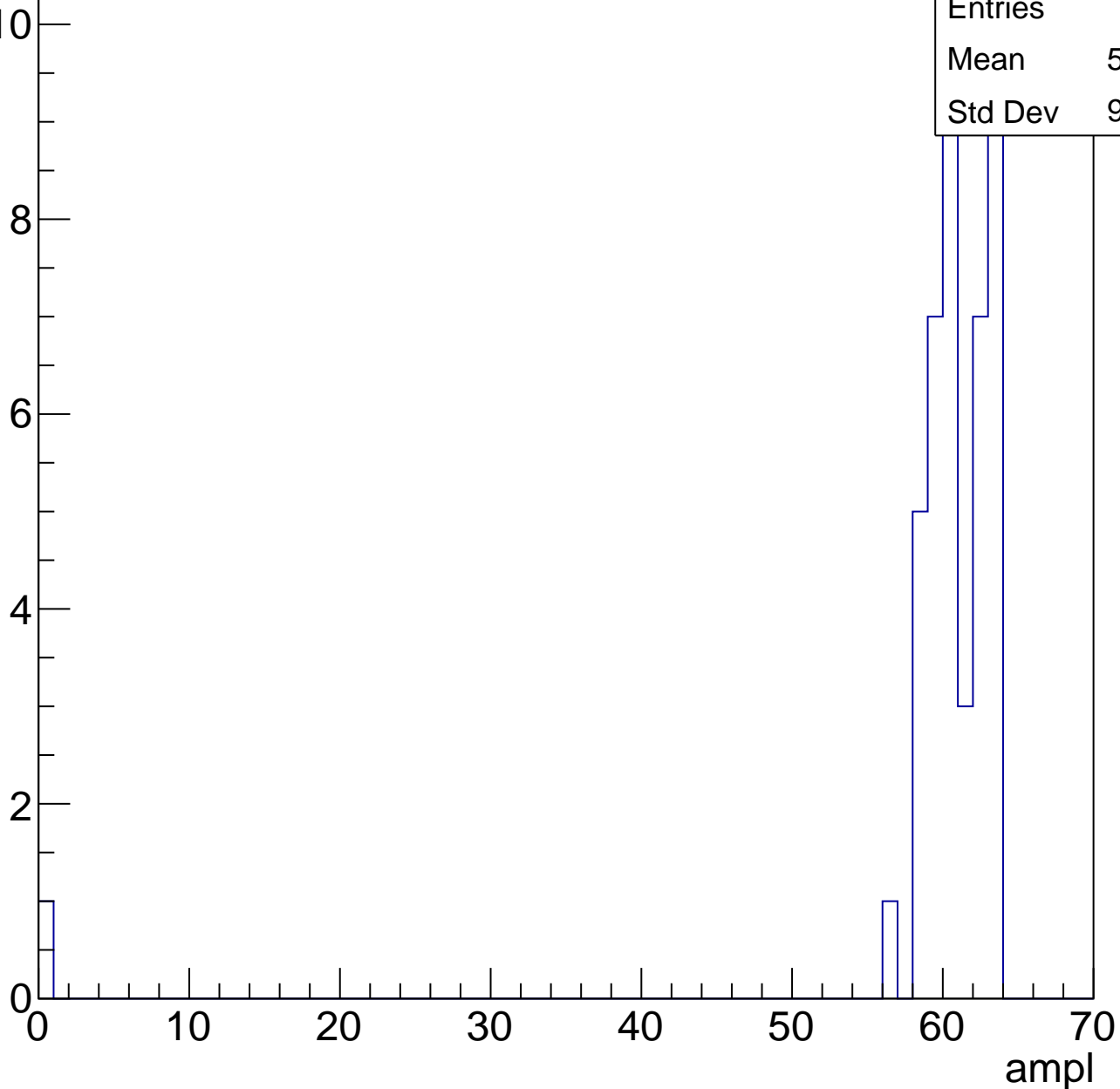


B1L103S, U11-ch67, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	44
Mean	59.23
Std Dev	9.217



B1L103S, U11-ch67, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch67, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

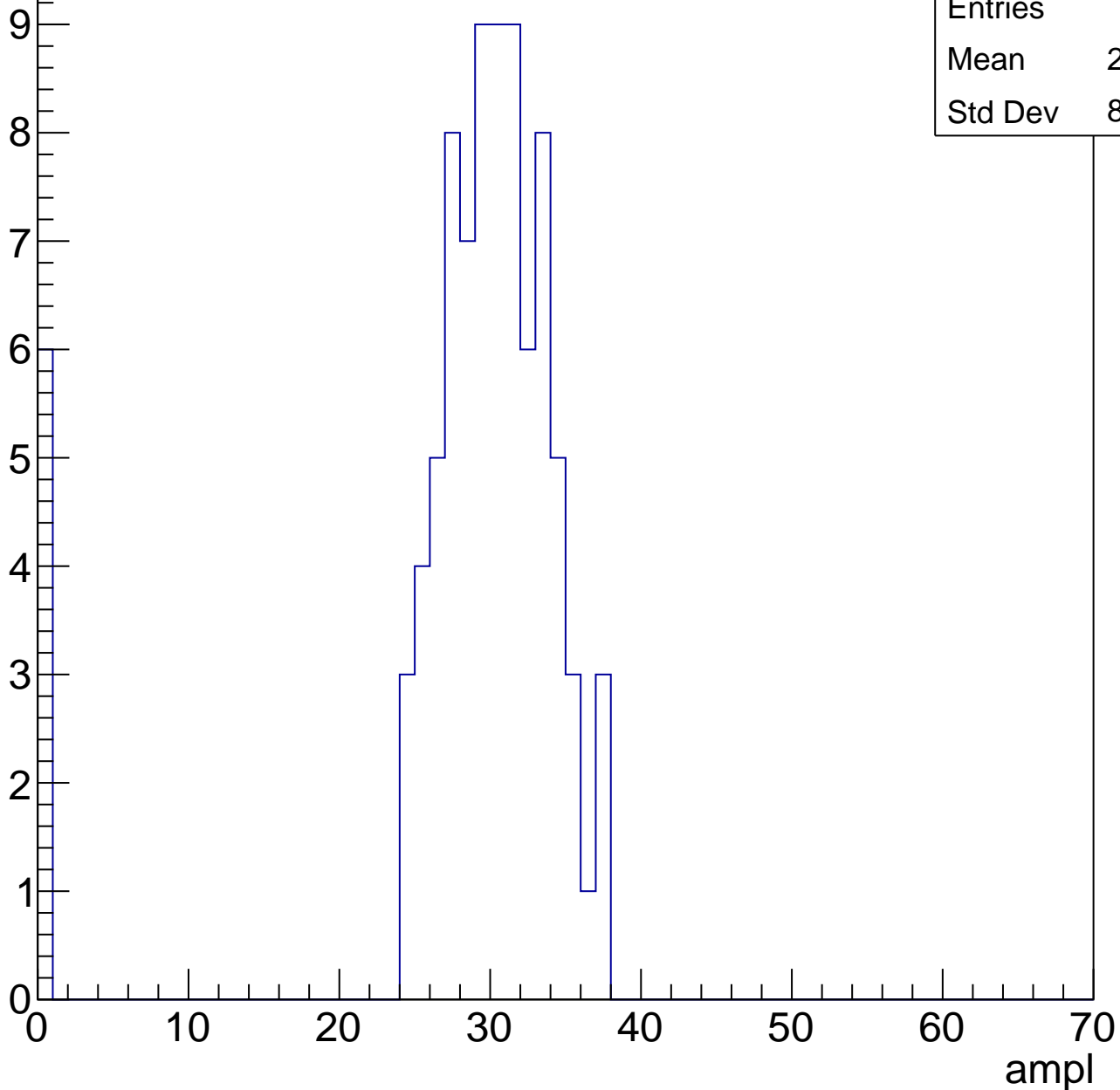


B1L103S, U11-ch68, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	86
Mean	27.93
Std Dev	8.263

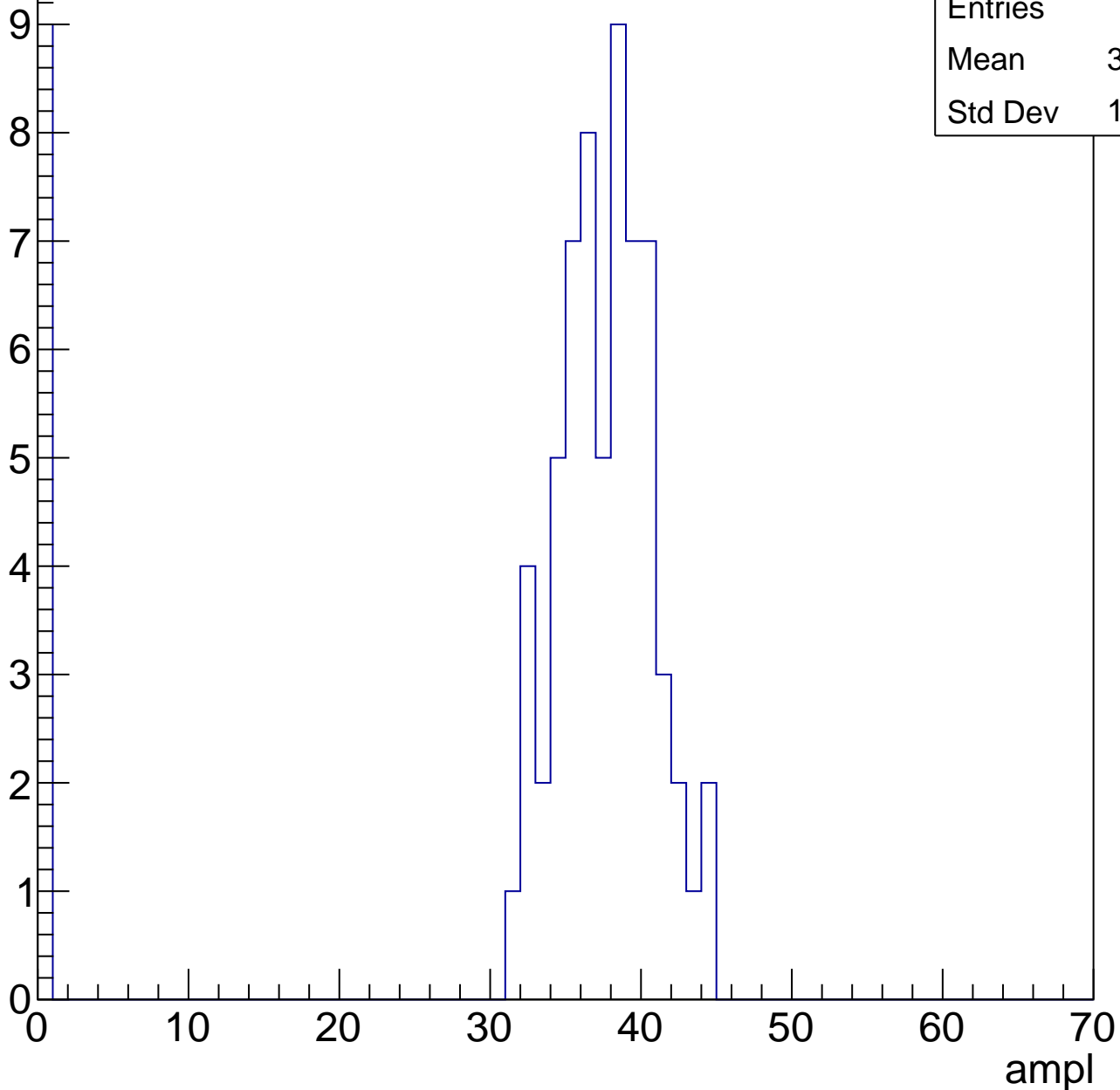


B1L103S, U11-ch68, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	32.58
Std Dev	12.64

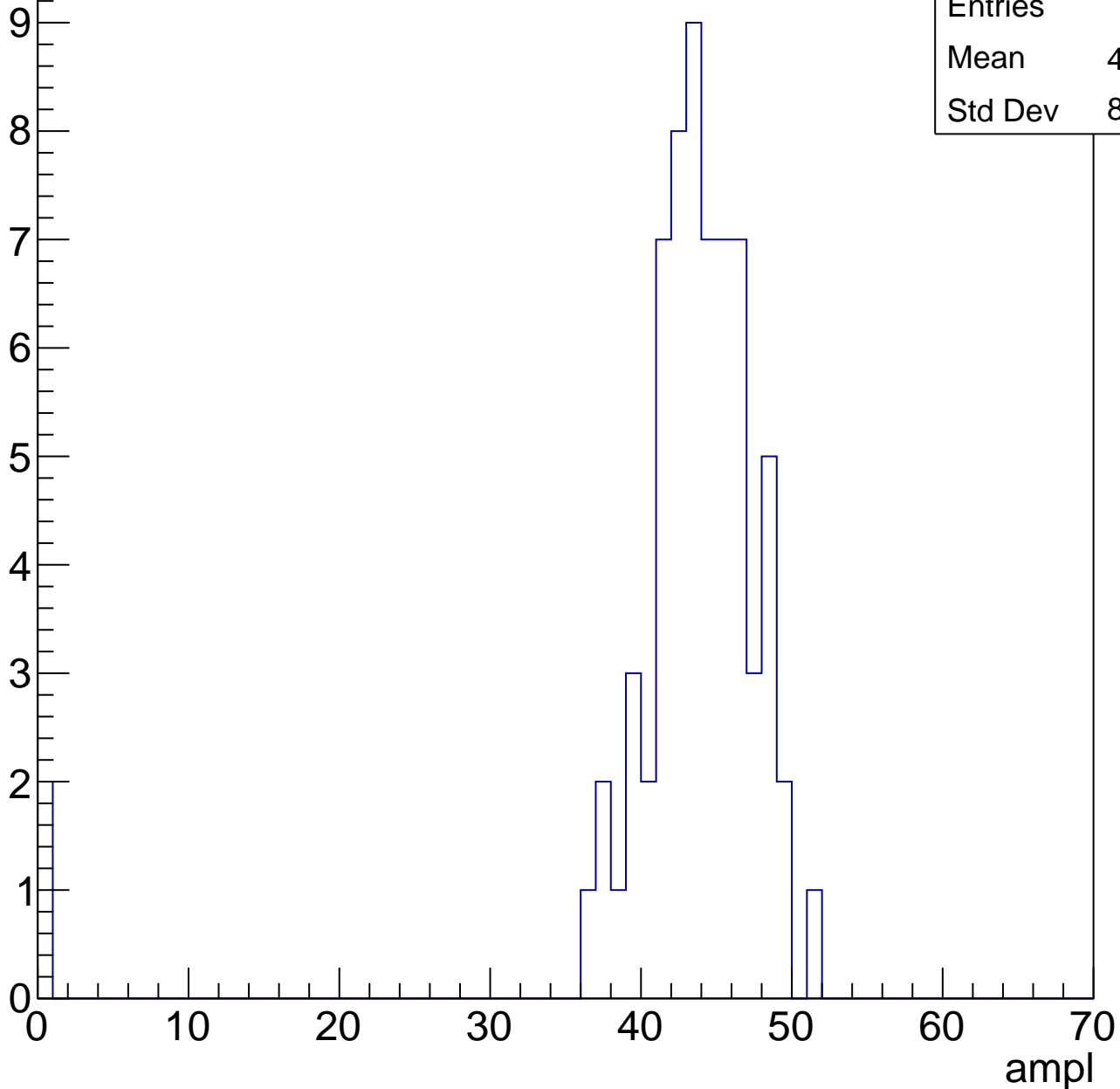


B1L103S, U11-ch68, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	42.24
Std Dev	8.024

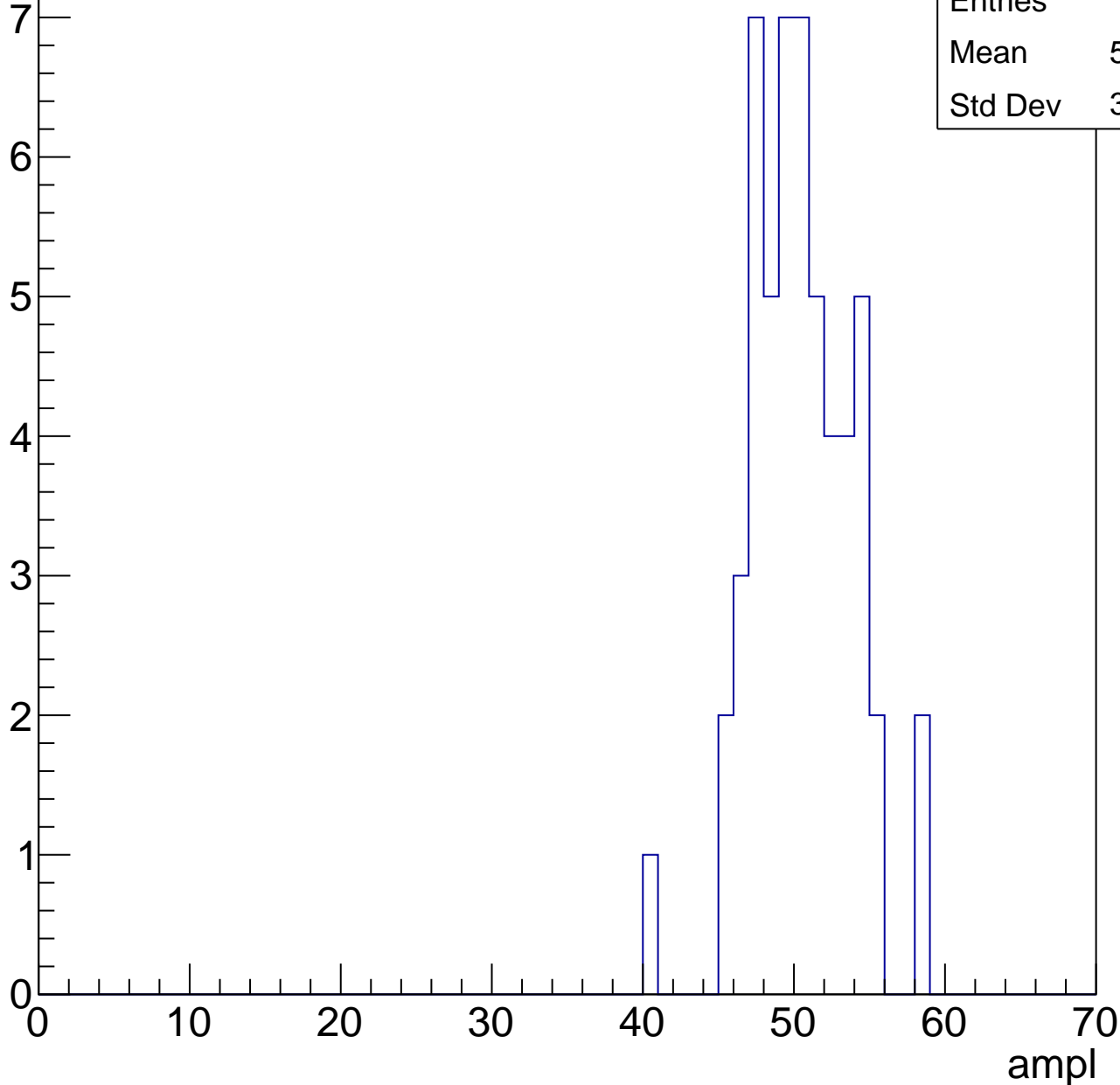


B1L103S, U11-ch68, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	50.02
Std Dev	3.342

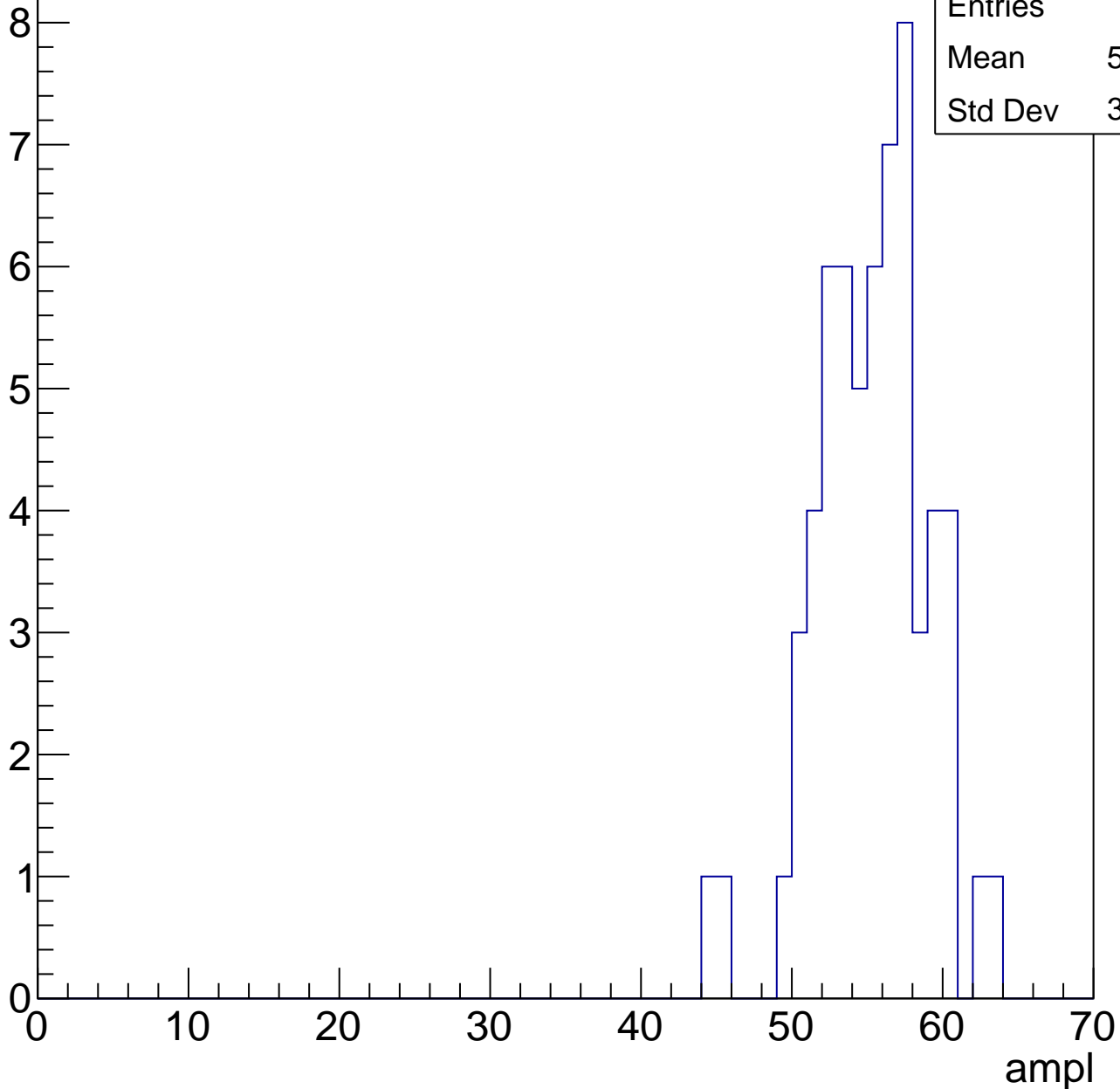


B1L103S, U11-ch68, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	54.84
Std Dev	3.667



B1L103S, U11-ch68, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entries	47
Mean	59.94
Std Dev	2.206

Entry

10

8

6

4

2

0

0

10

20

30

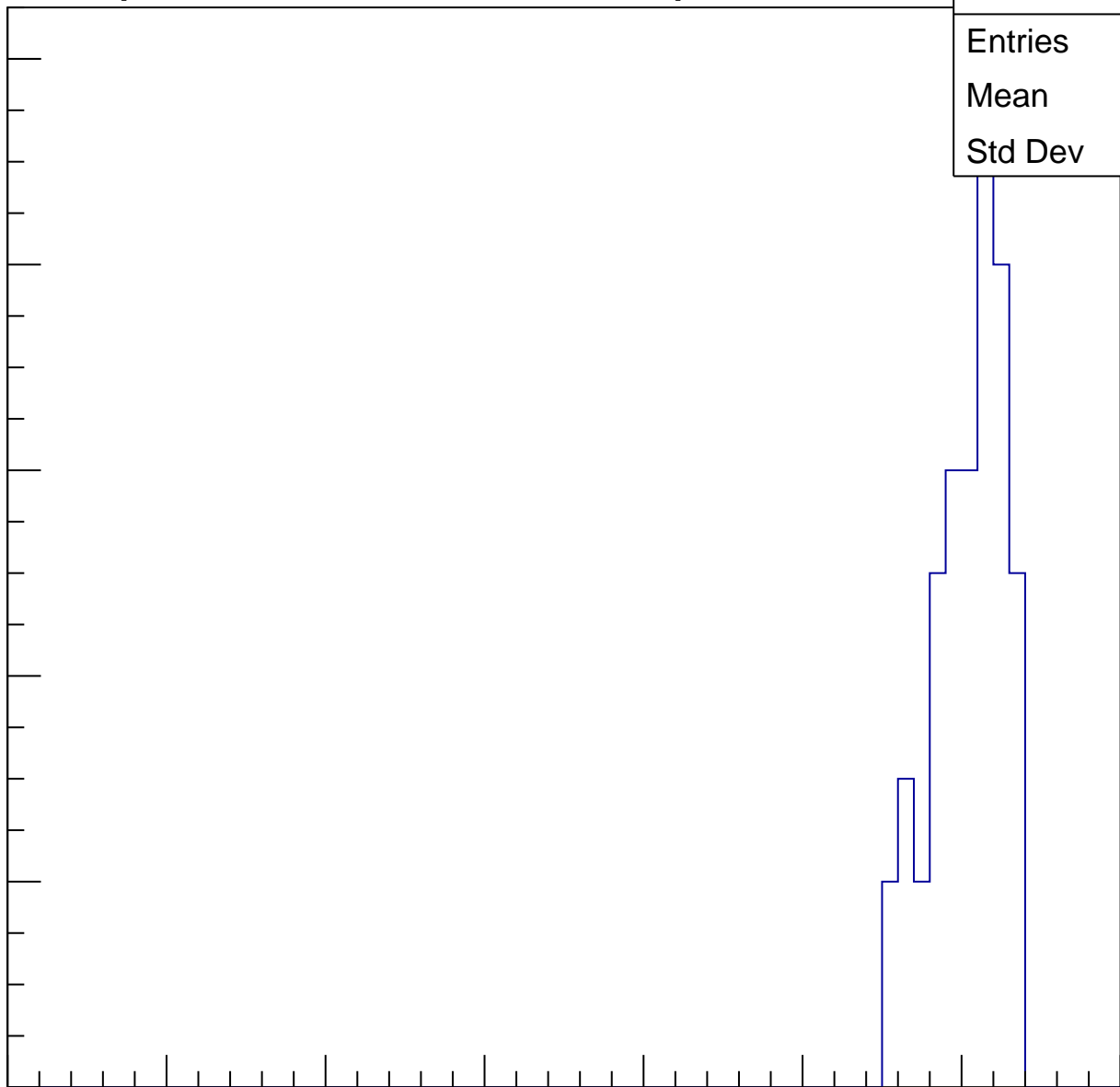
40

50

60

70

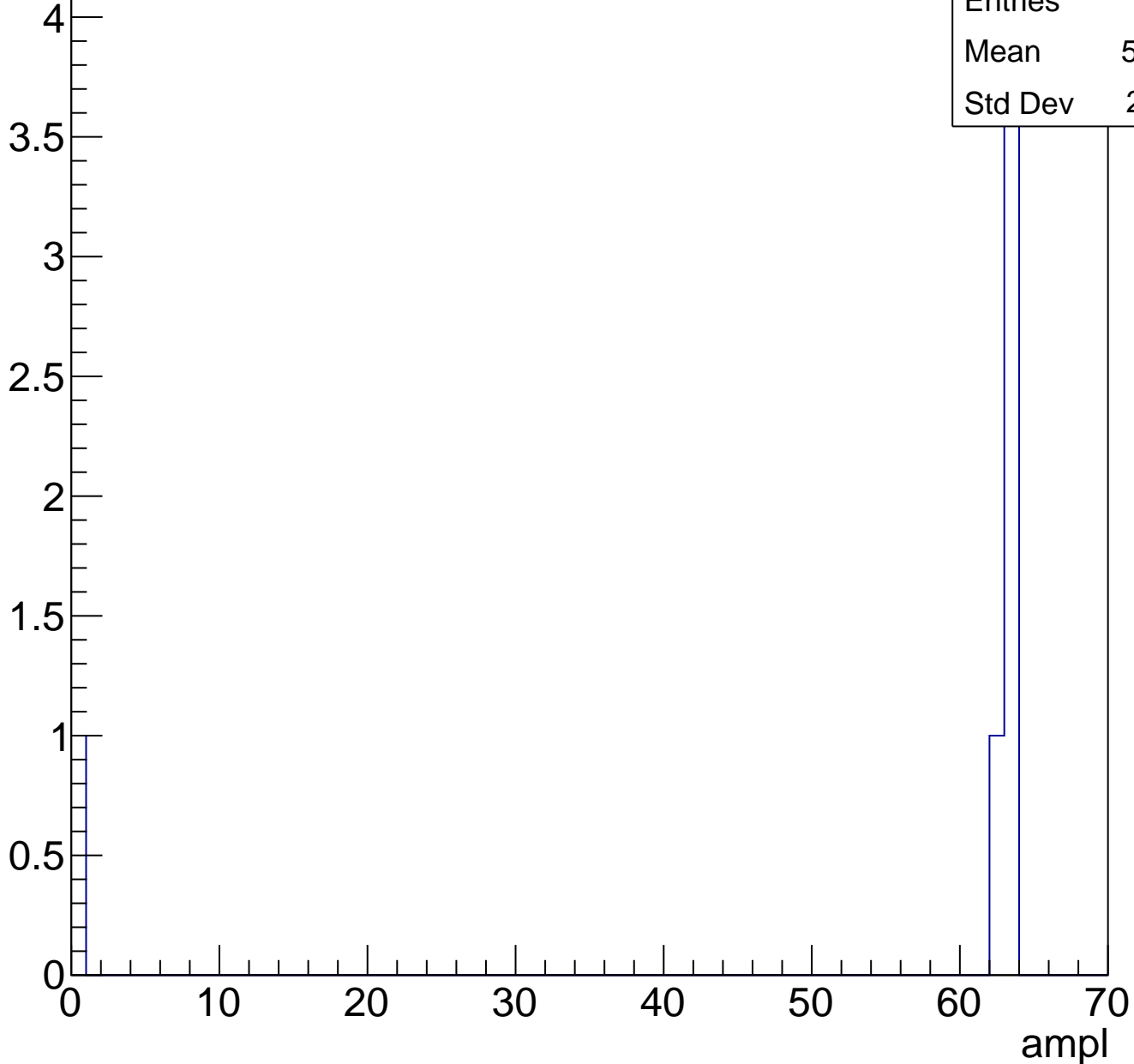
ampl



B1L103S, U11-ch68, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

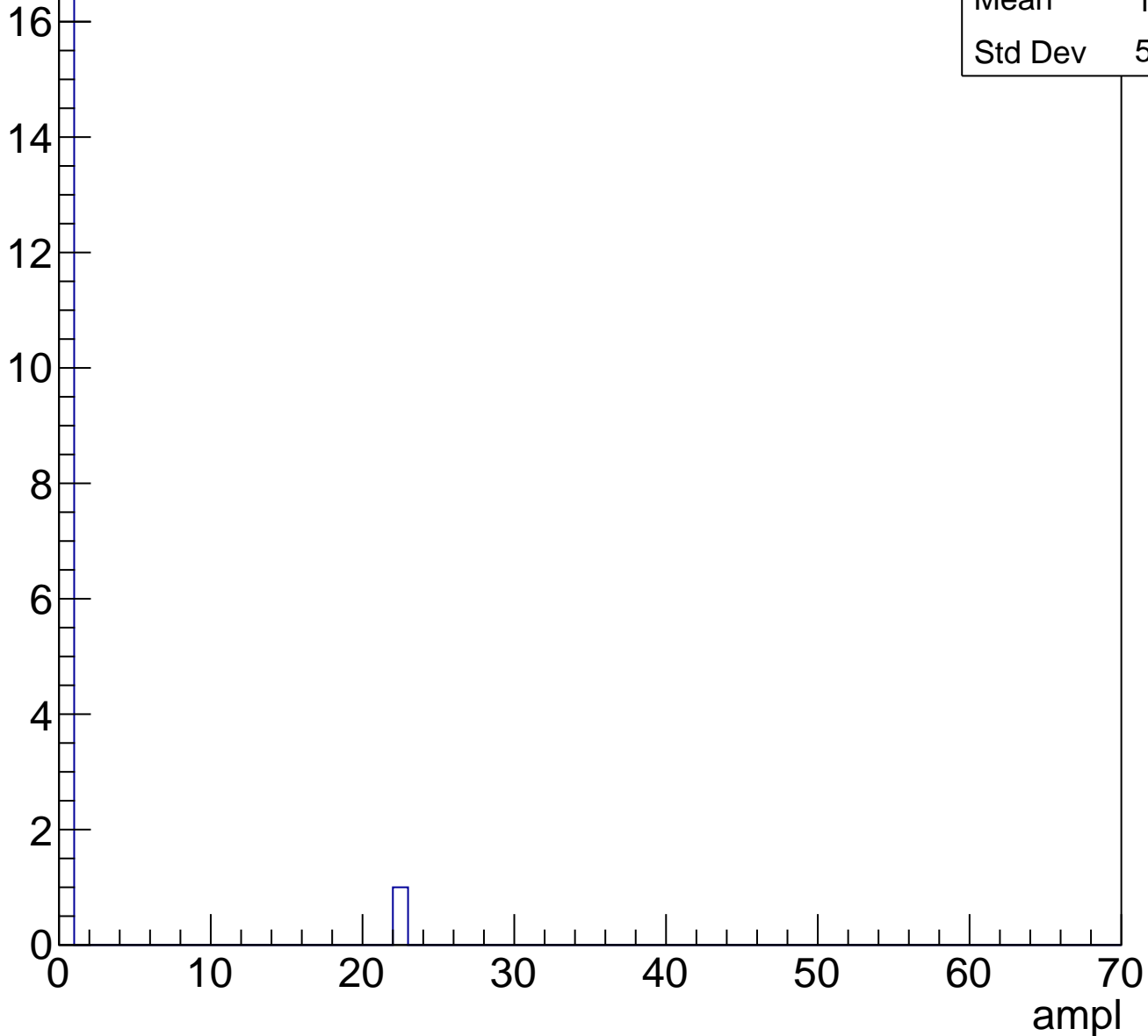


B1L103S, U11-ch68, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	18
Mean	1.222
Std Dev	5.039

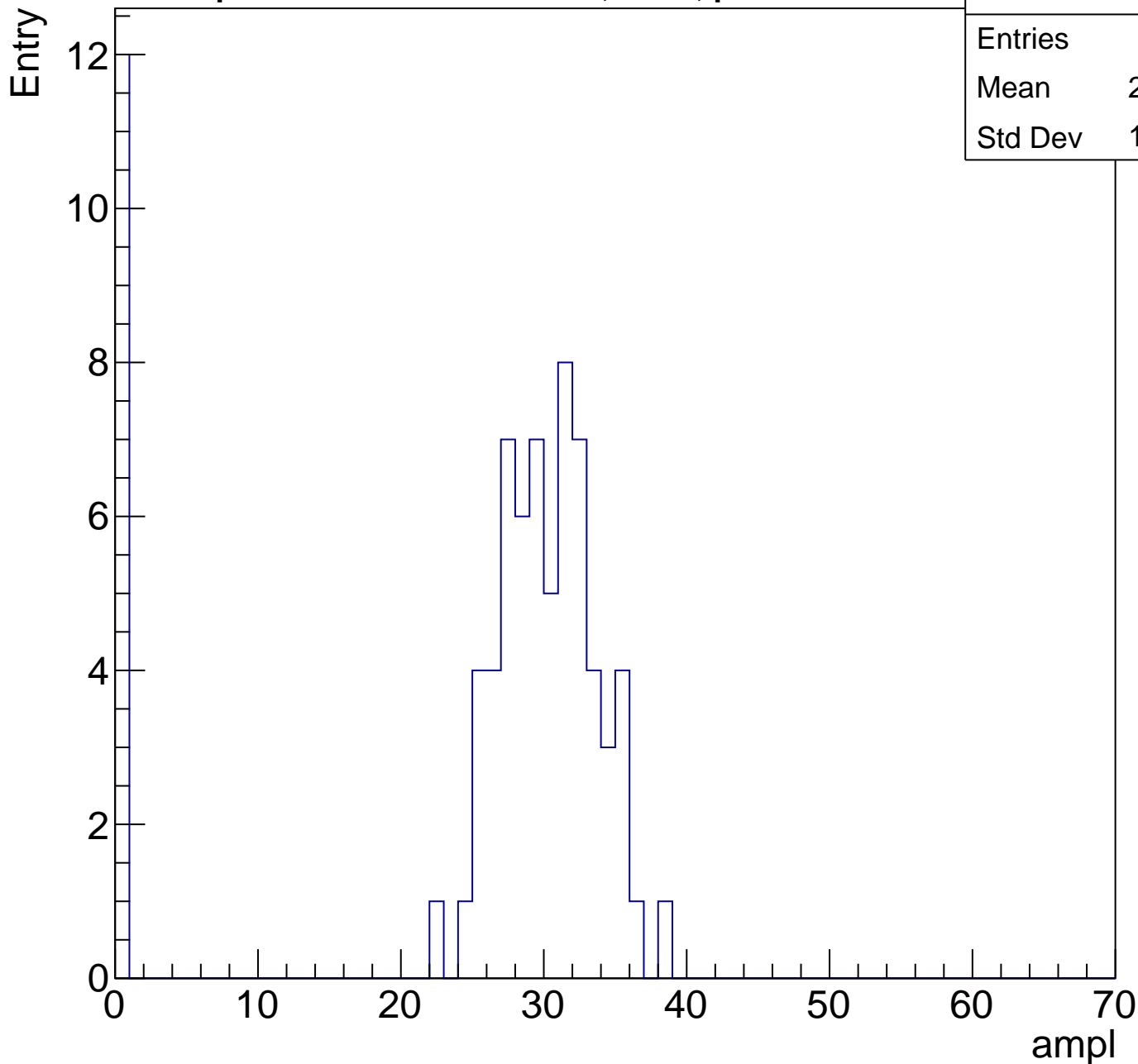
Entry



B1L103S, U11-ch69, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	25.07
Std Dev	11.34



B1L103S, U11-ch69, adc1

calib_packv5_041523_1651.root, FC#0, port C2

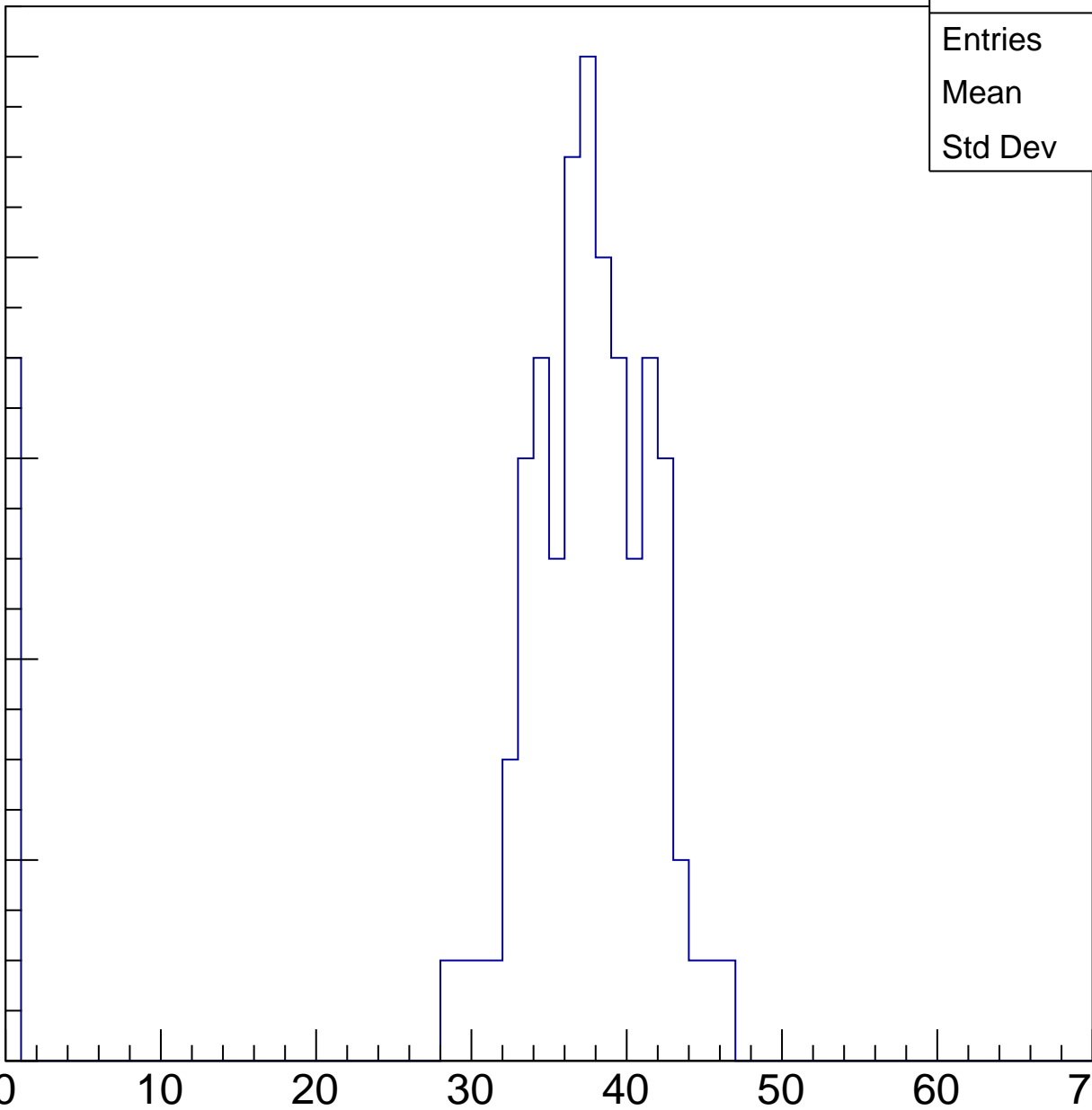
Entries	89
Mean	34.34
Std Dev	10.63

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

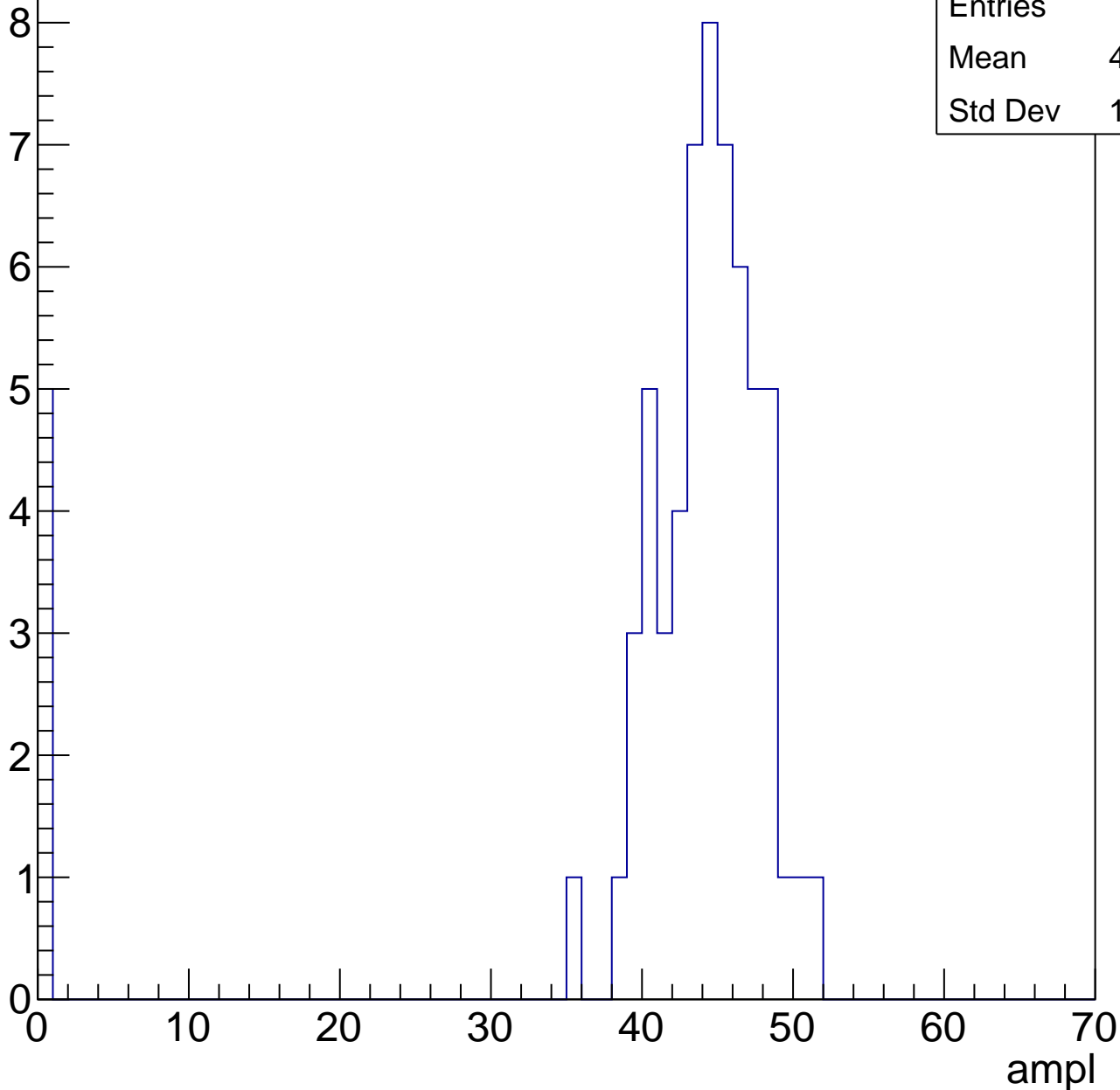


B1L103S, U11-ch69, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	40.48
Std Dev	12.27

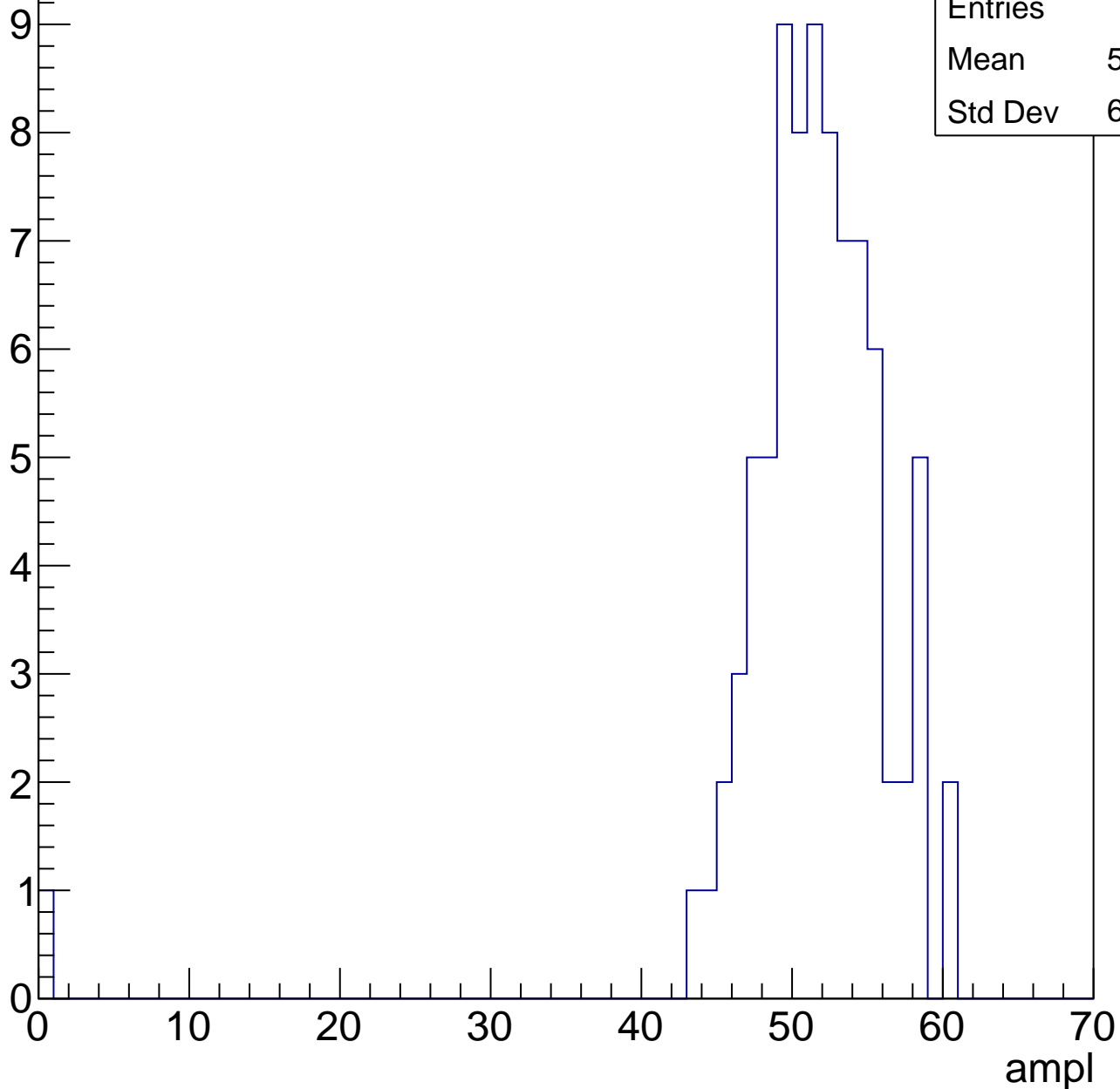


B1L103S, U11-ch69, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	83
Mean	50.86
Std Dev	6.724

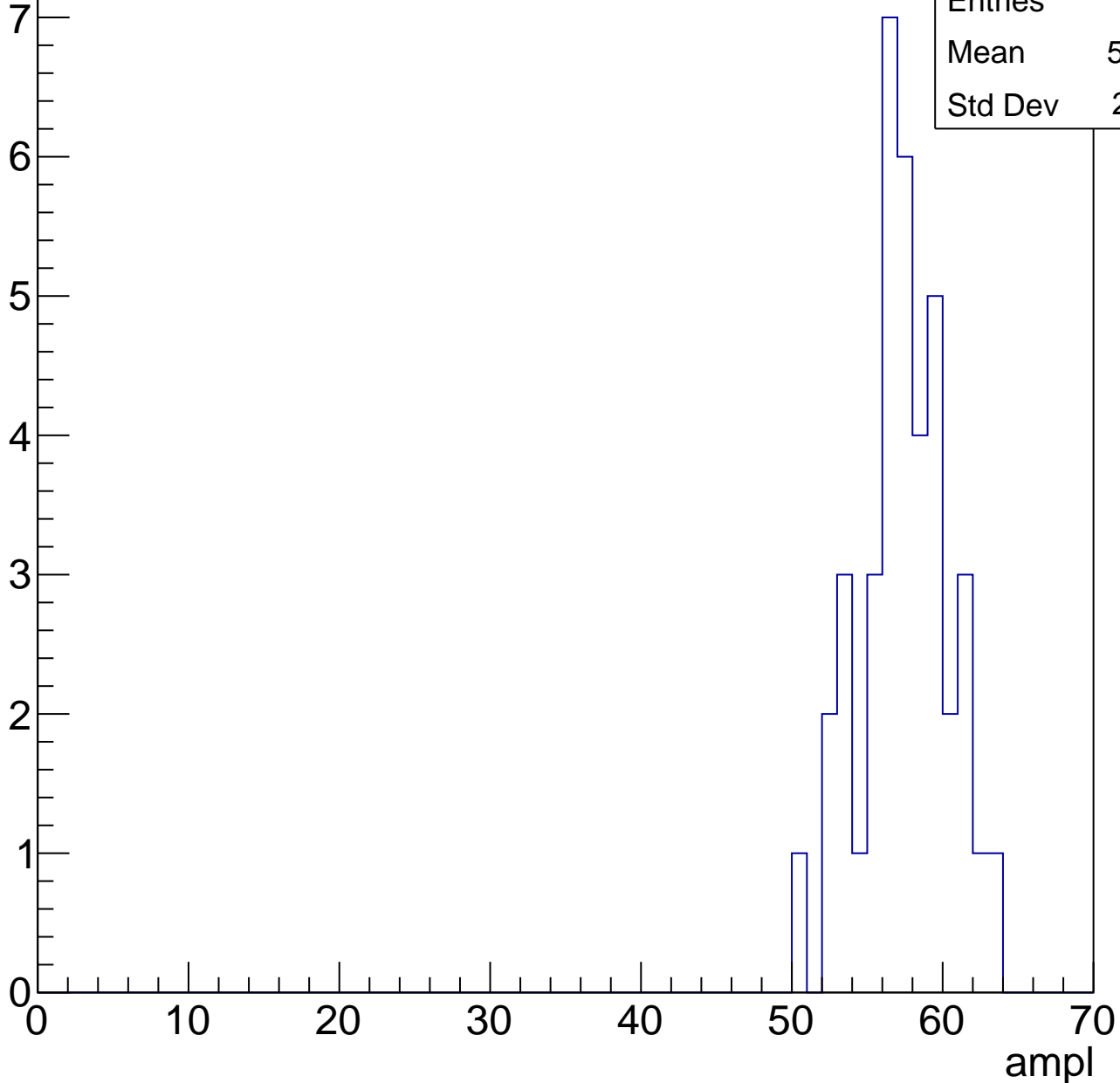


B1L103S, U11-ch69, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

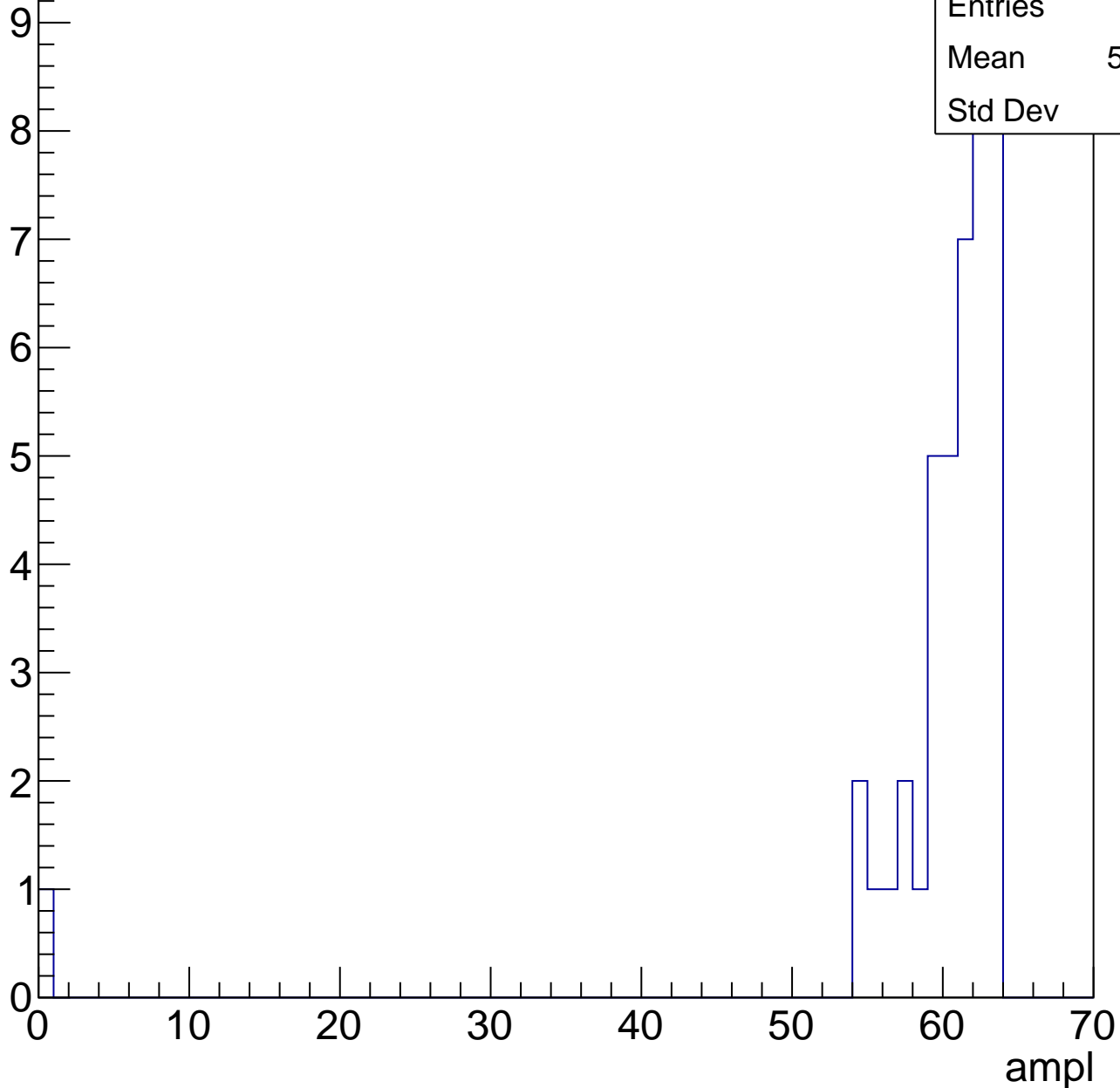
Entries	39
Mean	56.95
Std Dev	2.891



B1L103S, U11-ch69, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch69, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch69, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.158
Std Dev	4.913

Entry

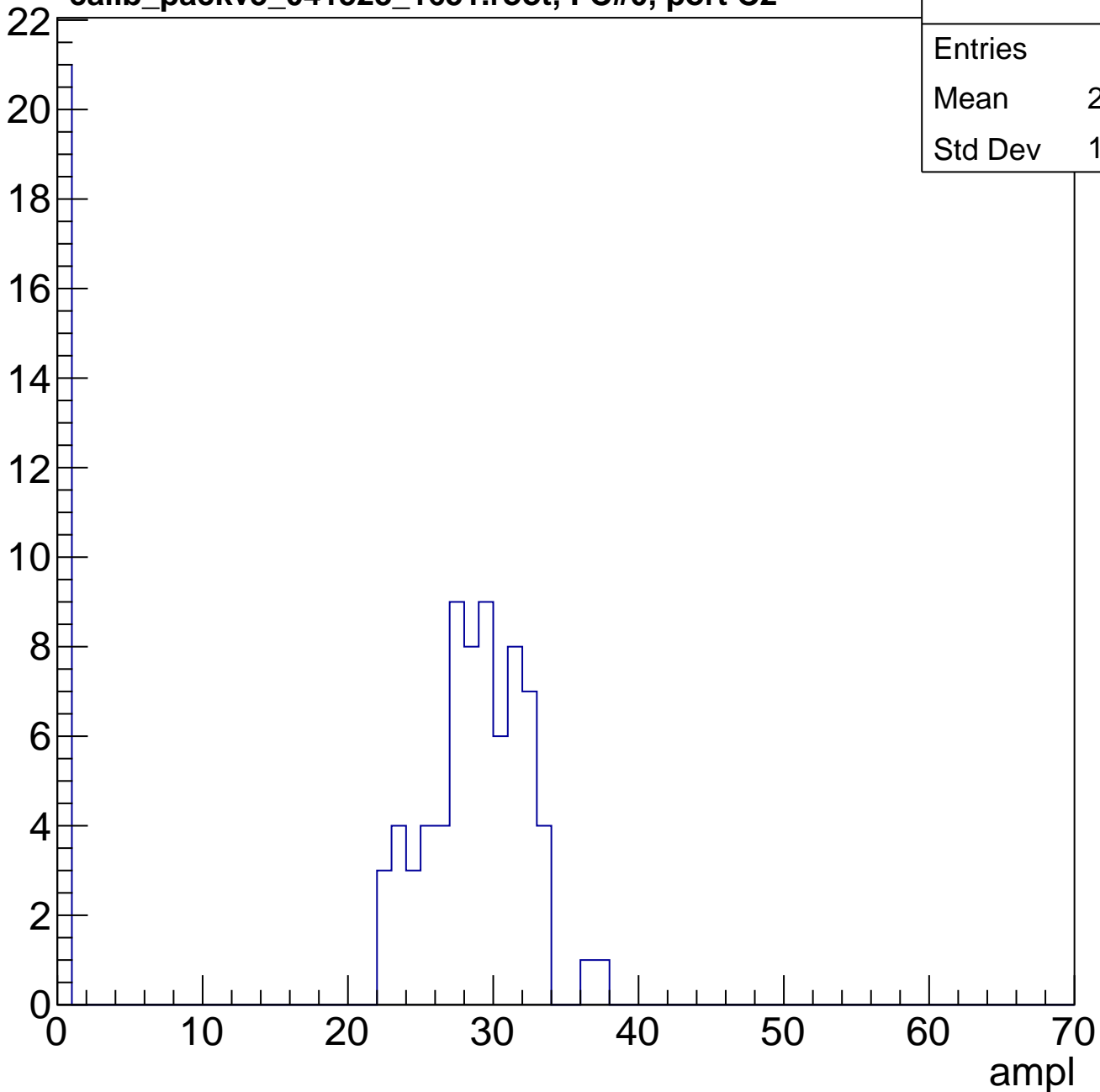


B1L103S, U11-ch70, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	92
Mean	21.95
Std Dev	12.28

Entry

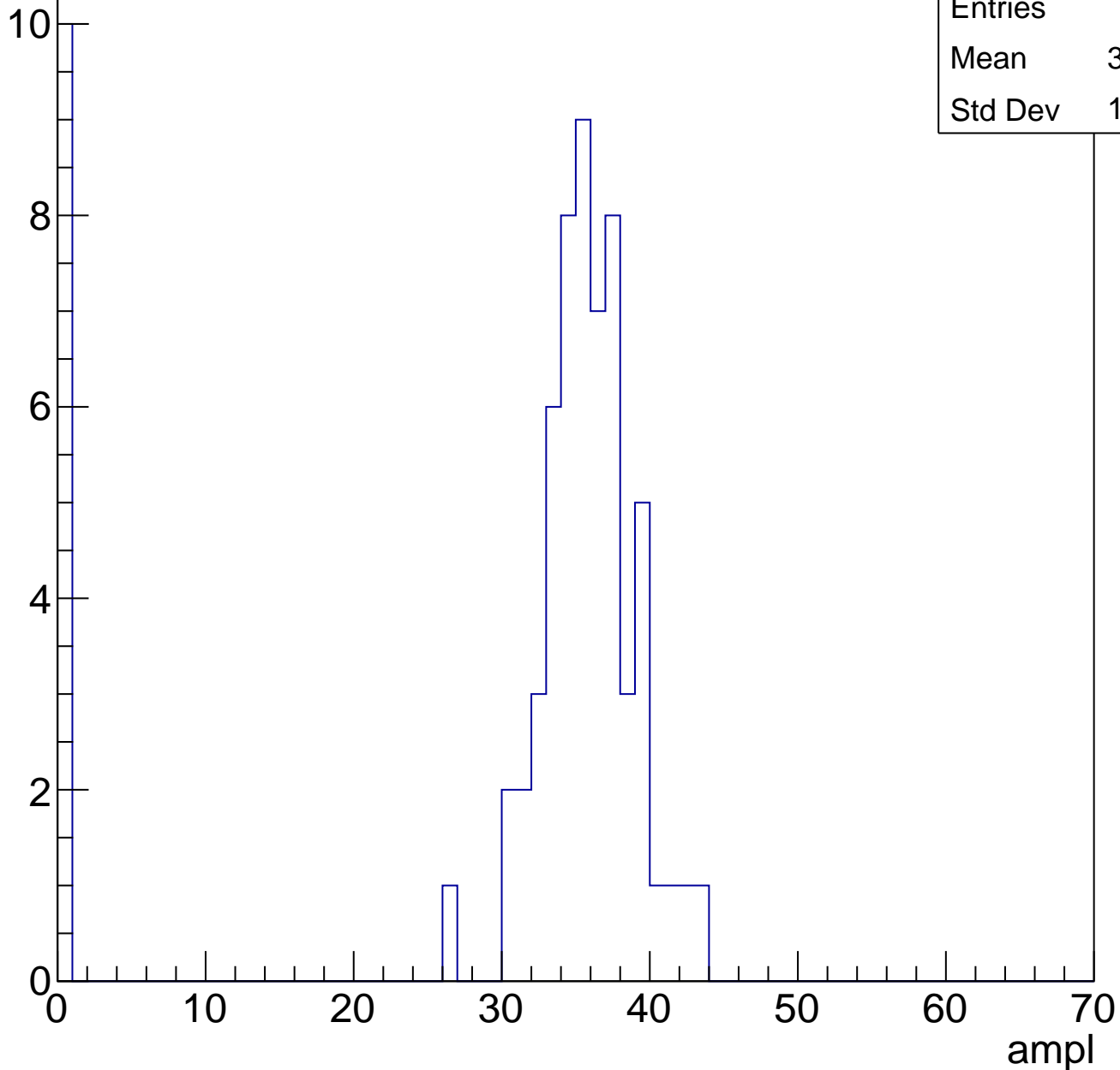


B1L103S, U11-ch70, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	68
Mean	30.18
Std Dev	12.84

Entry

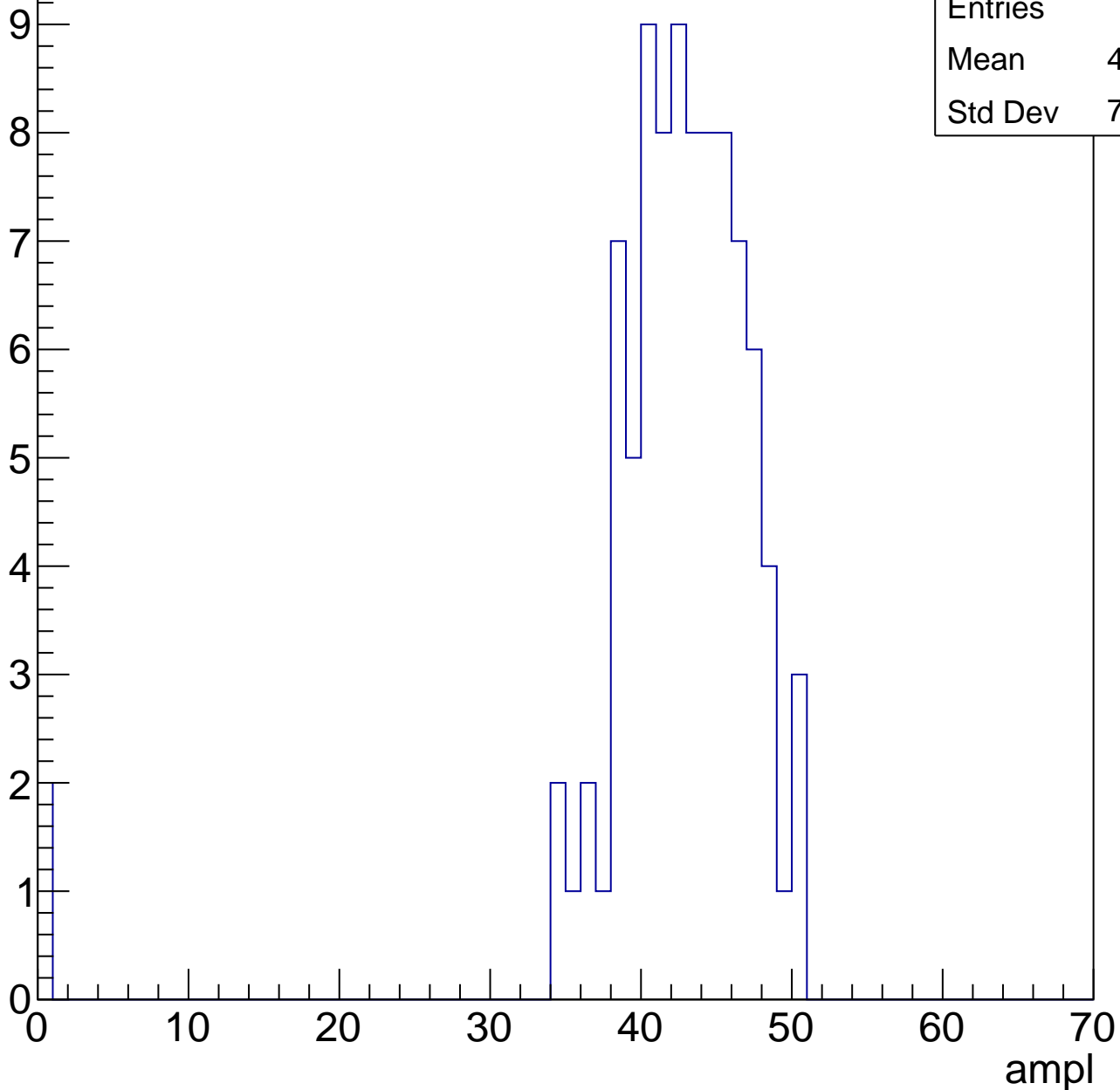


B1L103S, U11-ch70, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

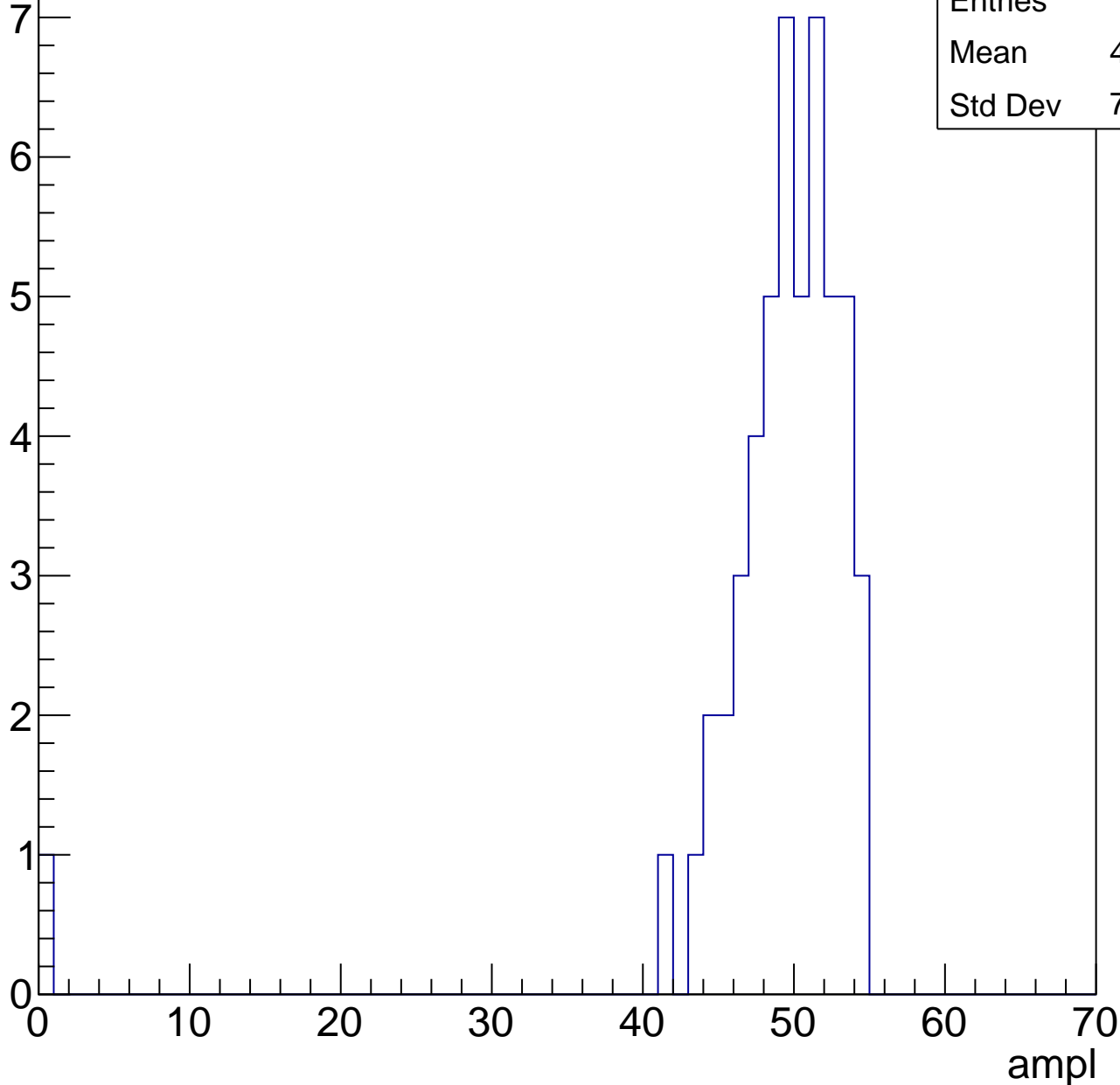
Entries	91
Mean	41.65
Std Dev	7.225



B1L103S, U11-ch70, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

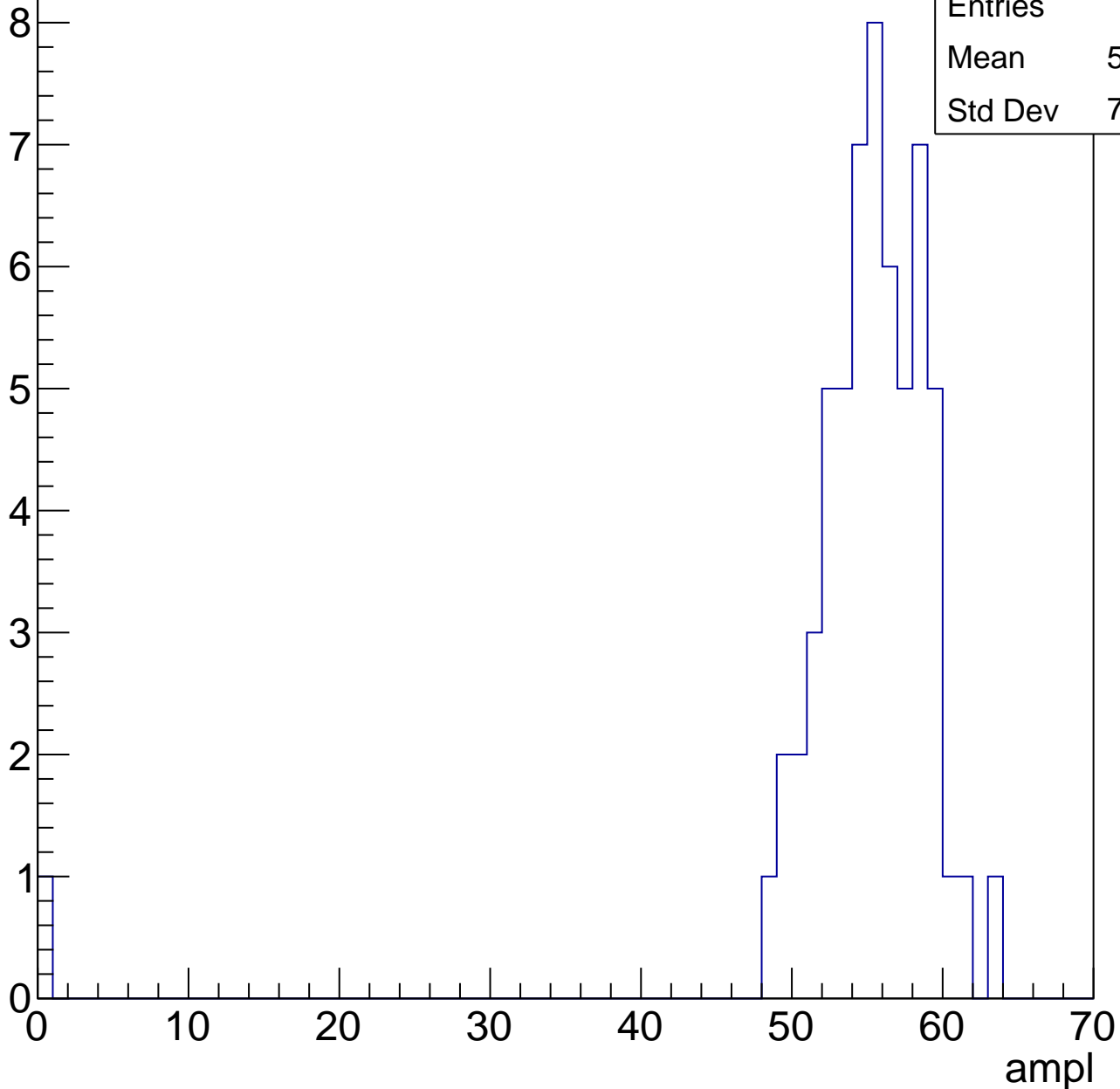


B1L103S, U11-ch70, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	54.13
Std Dev	7.708

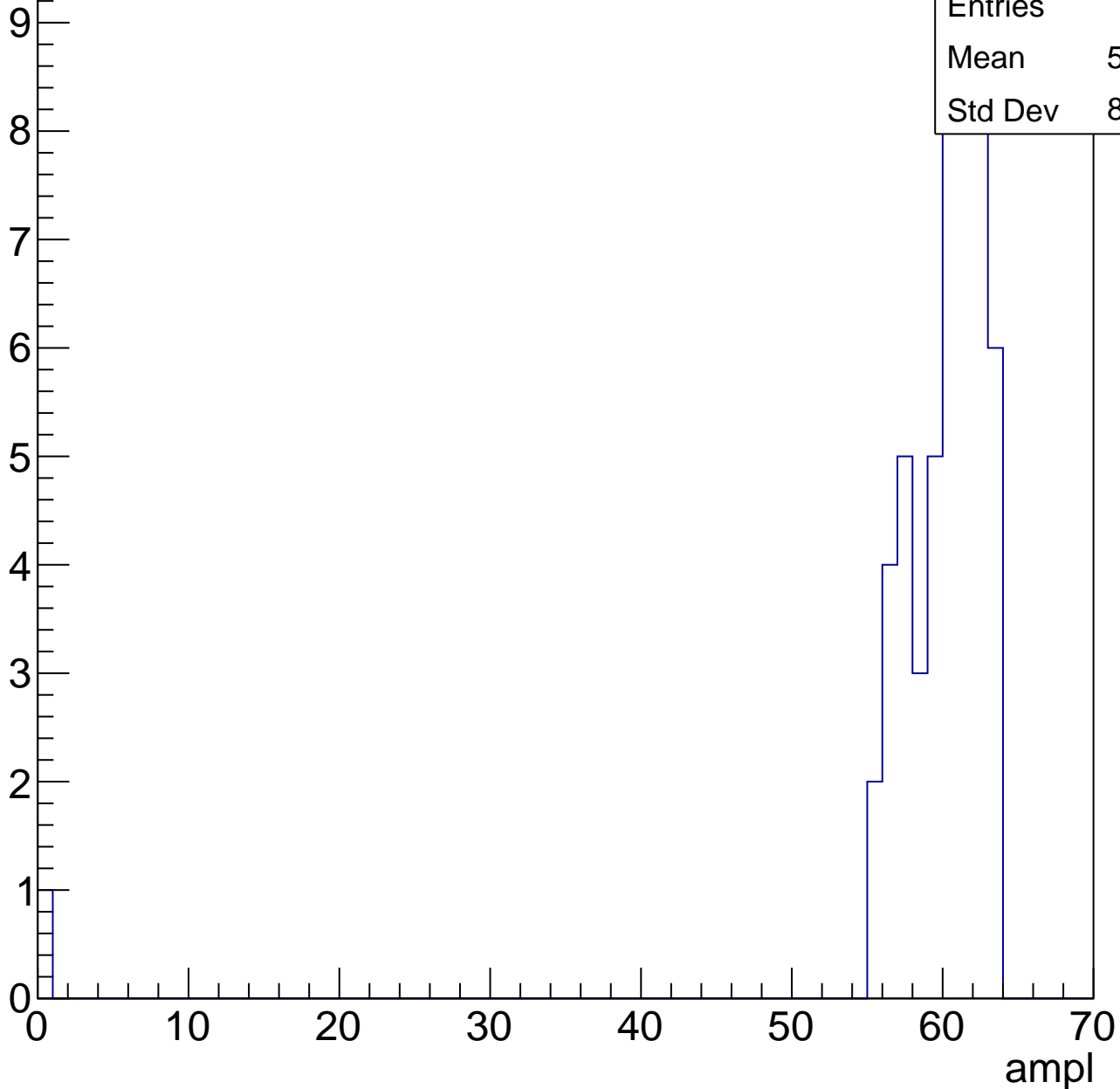


B1L103S, U11-ch70, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

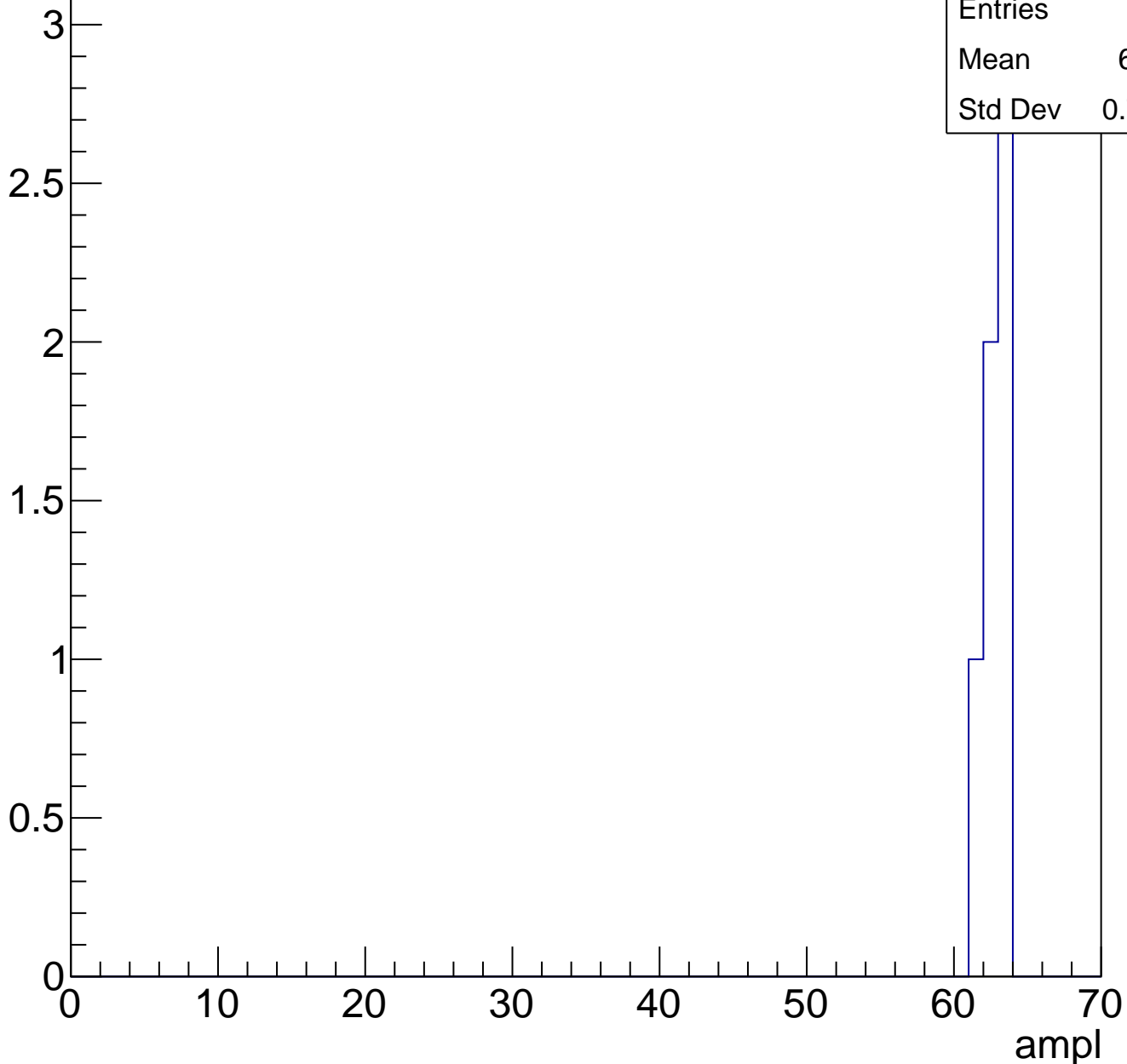
Entries	51
Mean	58.63
Std Dev	8.602



B1L103S, U11-ch70, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	6
Mean	62.33
Std Dev	0.7454

B1L103S, U11-ch70, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U11-ch71, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	87
Mean	26.64
Std Dev	11.54

Entry

12

10

8

6

4

2

0

0

10

20

30

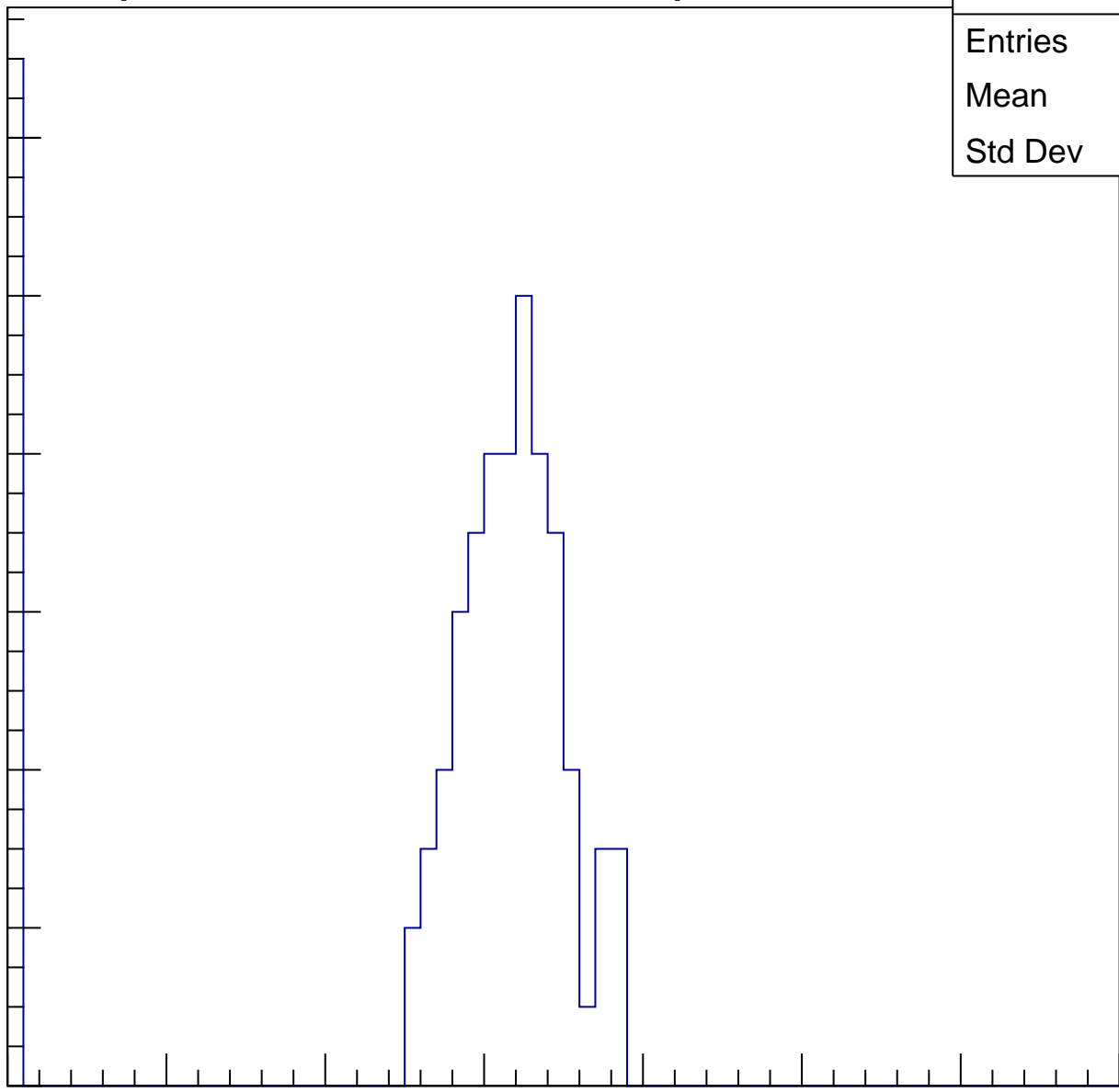
40

50

60

70

ampl

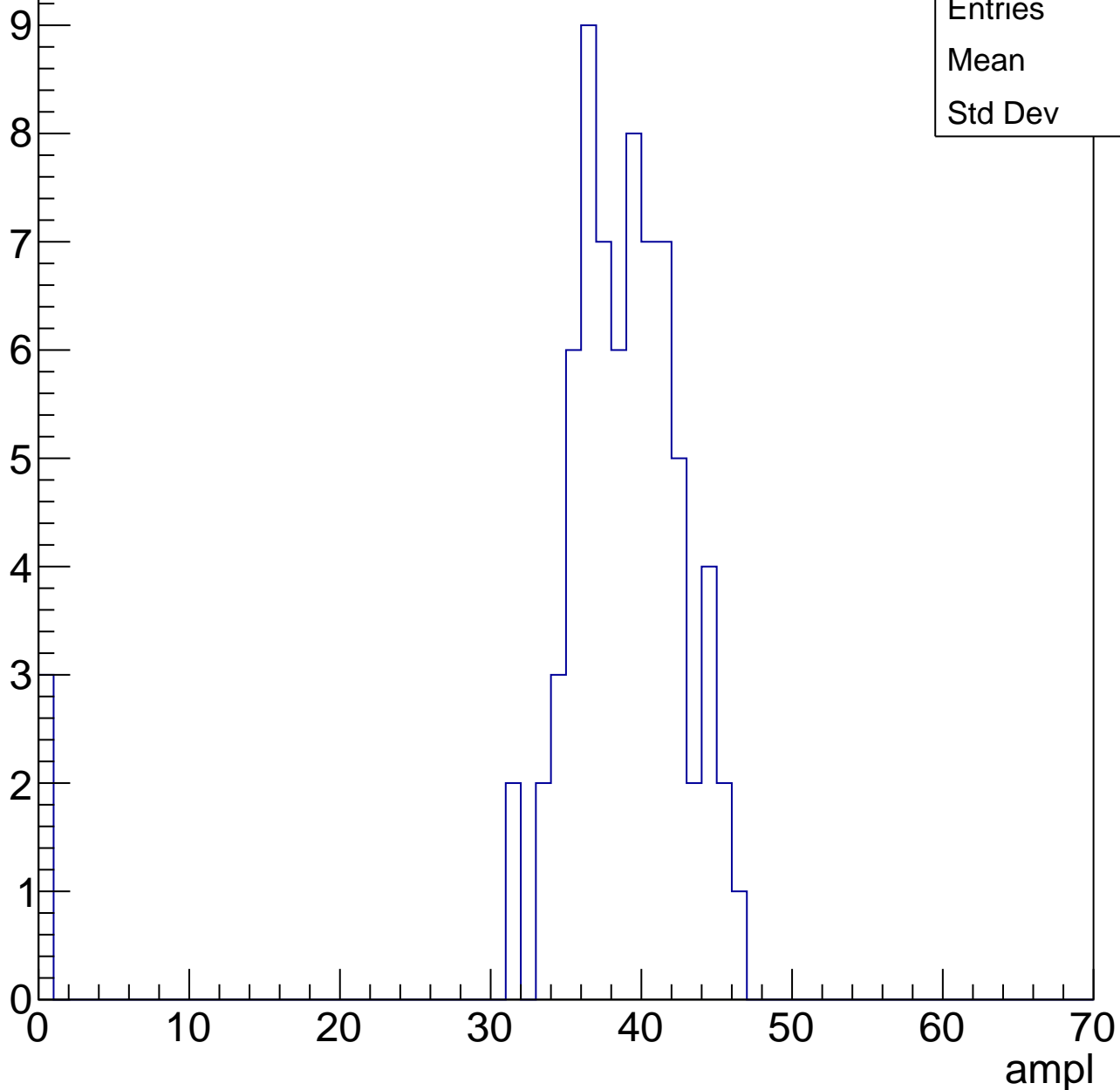


B1L103S, U11-ch71, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	37
Std Dev	8.29

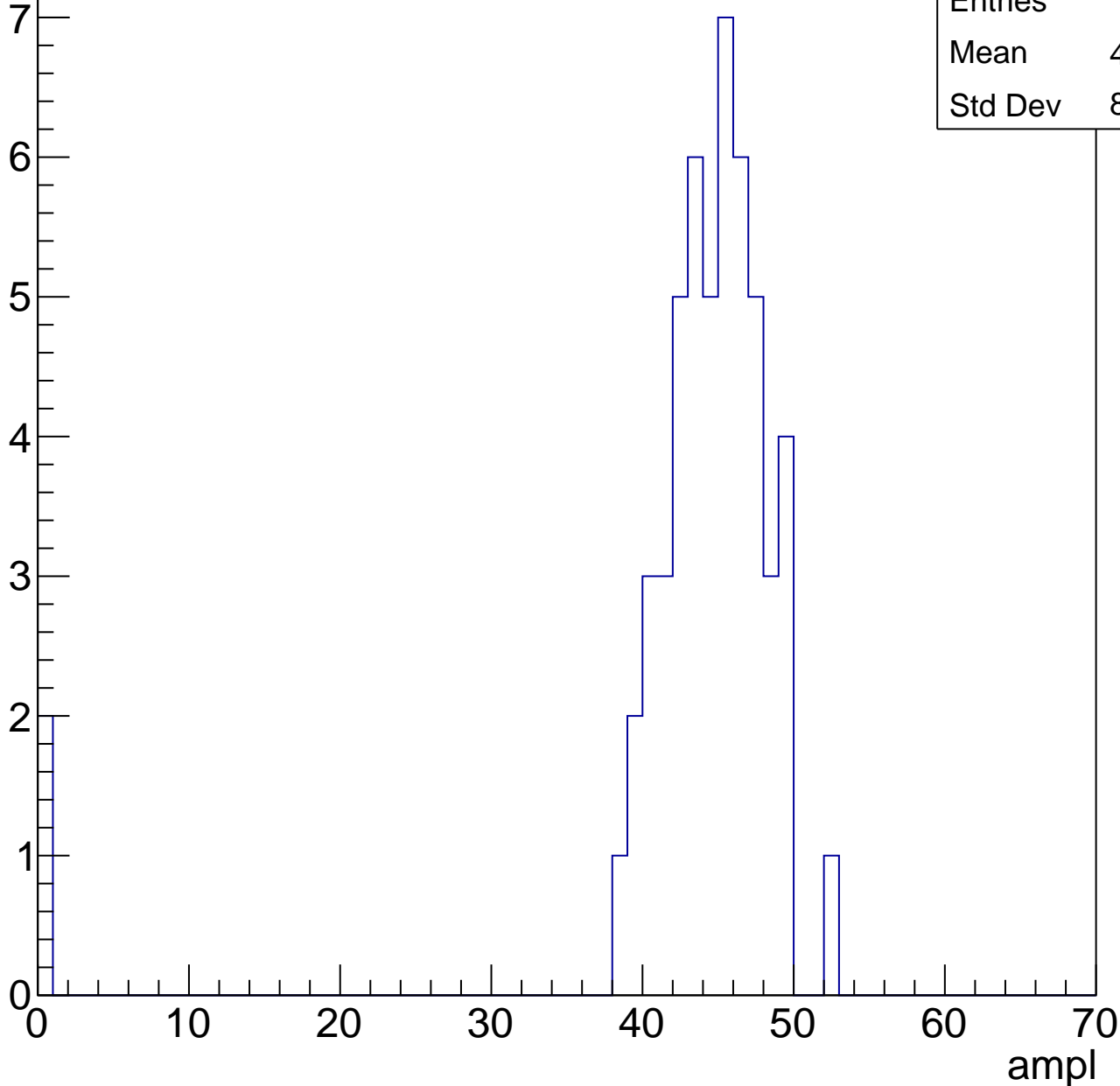


B1L103S, U11-ch71, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	42.74
Std Dev	8.968



B1L103S, U11-ch71, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	90
Mean	48.62
Std Dev	12.34

Entry

10

8

6

4

2

0

0

10

20

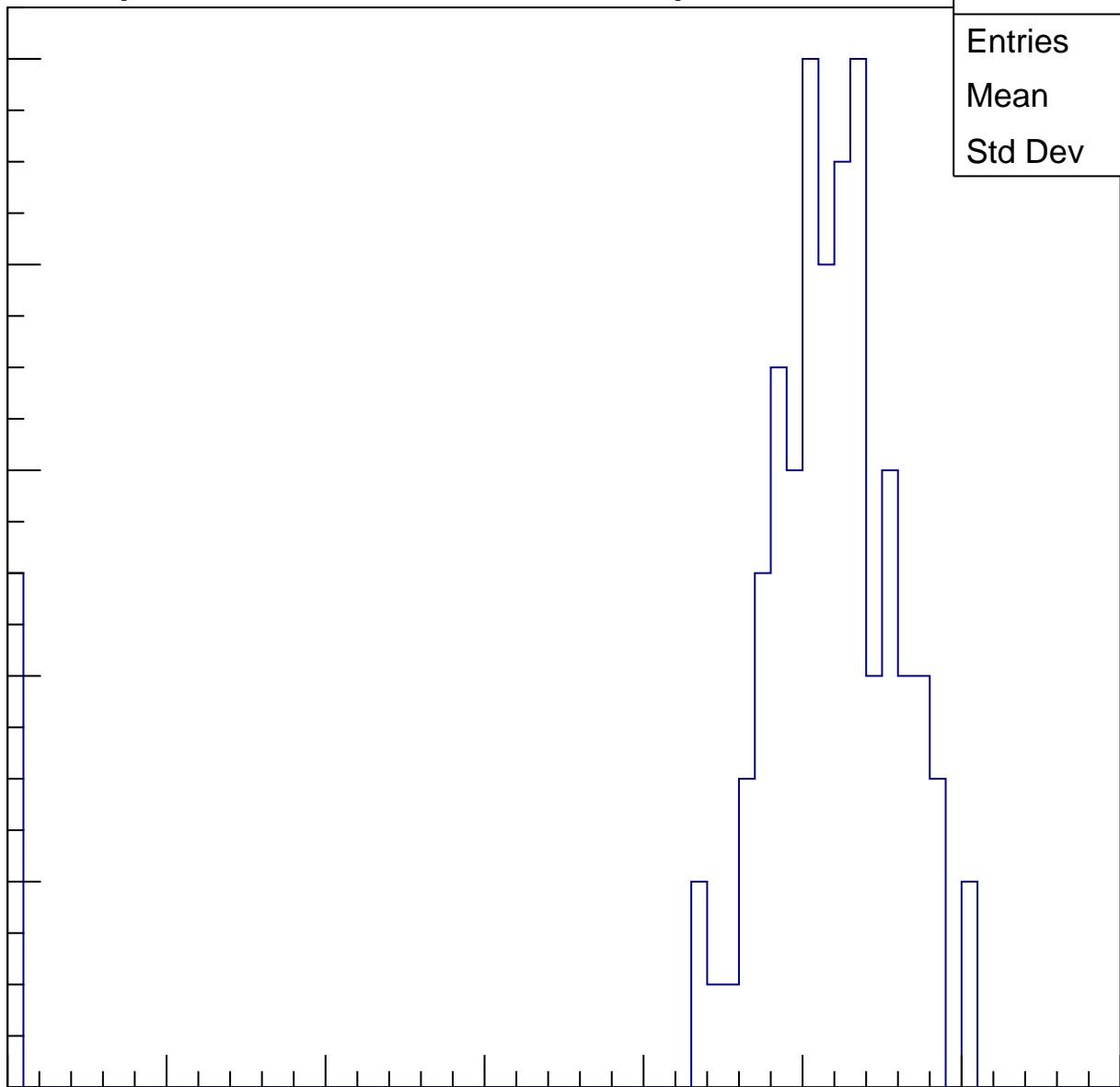
30

40

50

60

ampl



B1L103S, U11-ch71, adc4

calib_packv5_041523_1651.root, FC#0, port C2

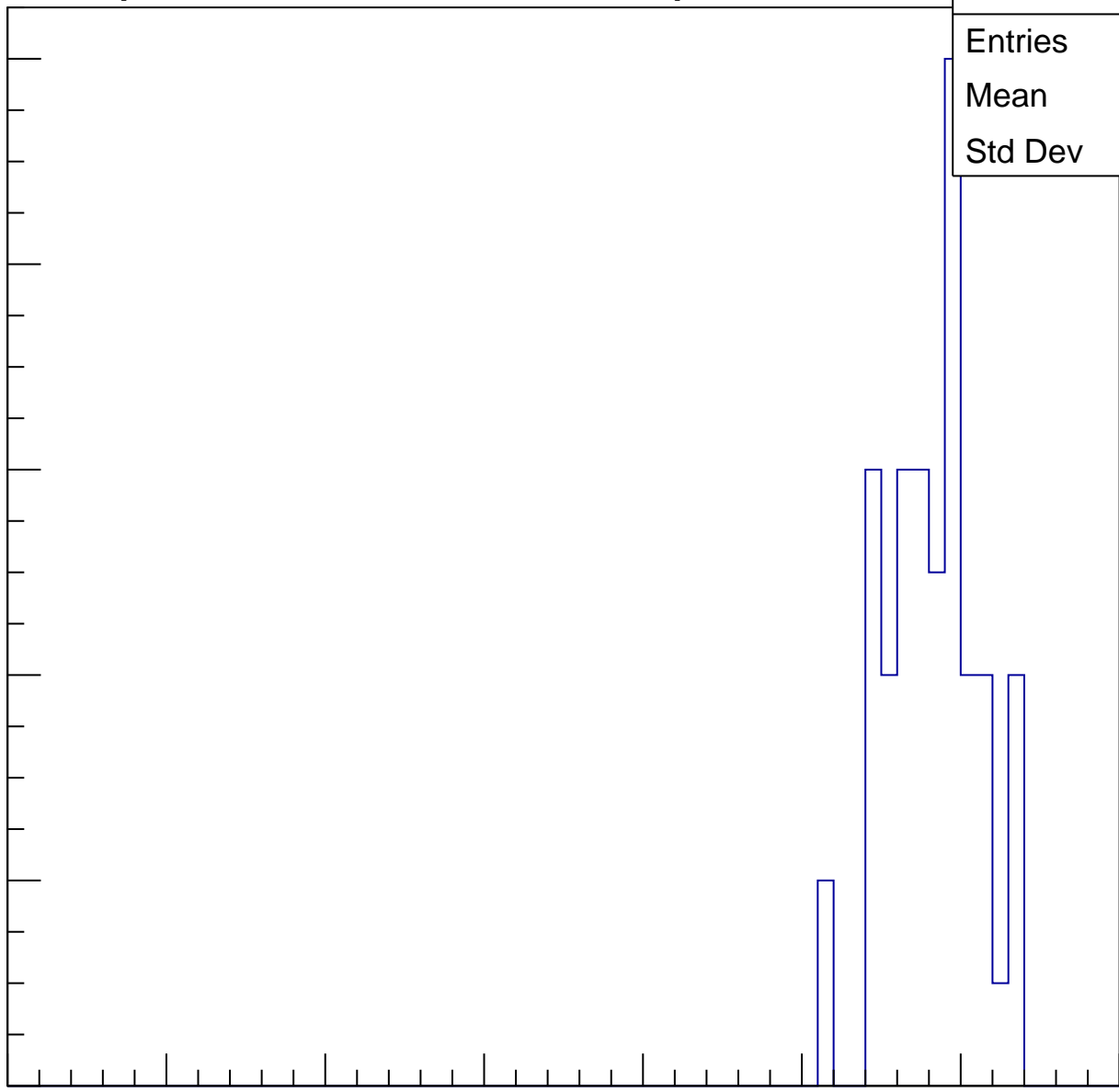
Entries	52
Mean	57.73
Std Dev	2.89

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

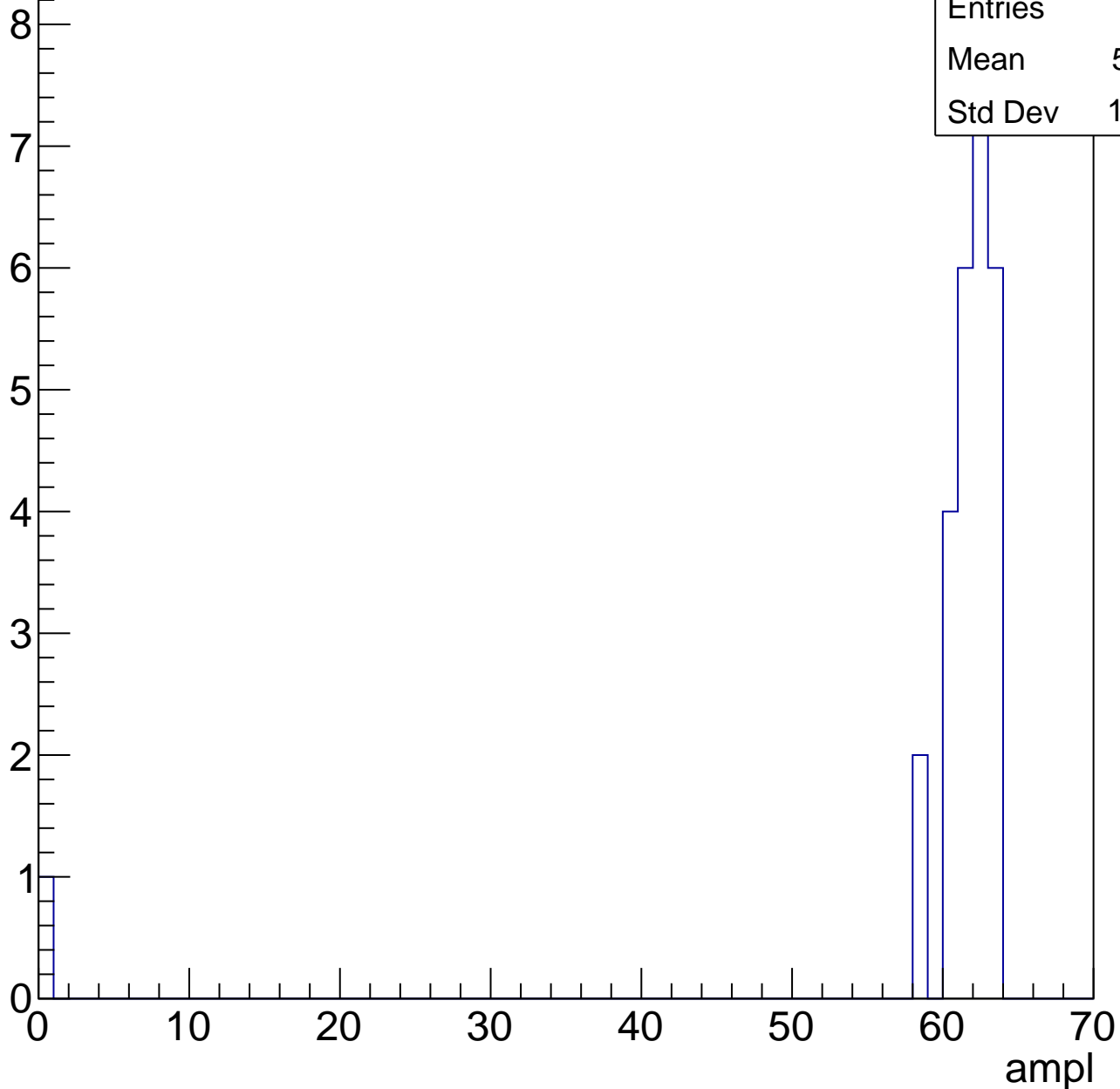


B1L103S, U11-ch71, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	27
Mean	59.11
Std Dev	11.67



B1L103S, U11-ch71, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

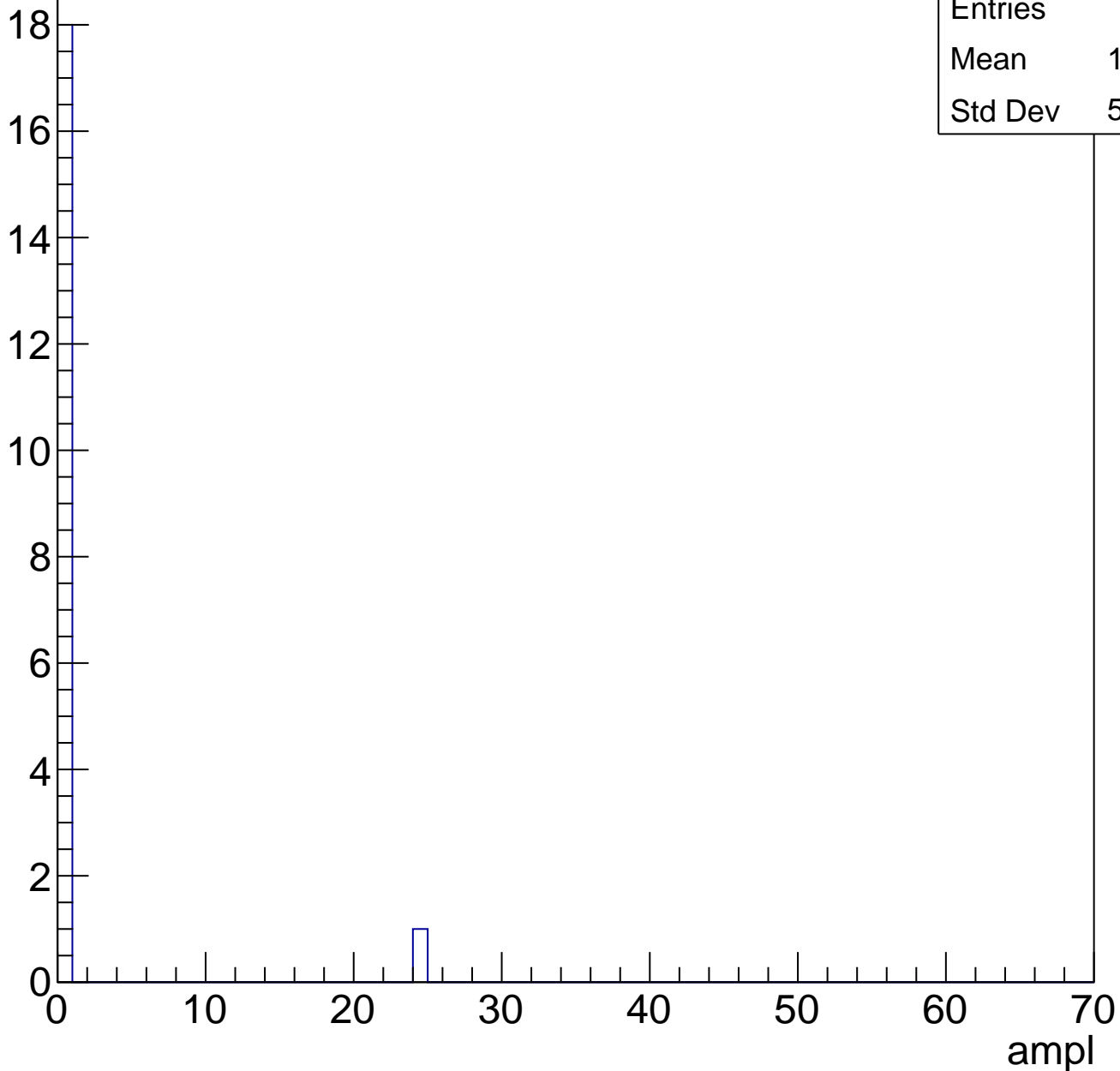


B1L103S, U11-ch71, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.263
Std Dev	5.359

Entry

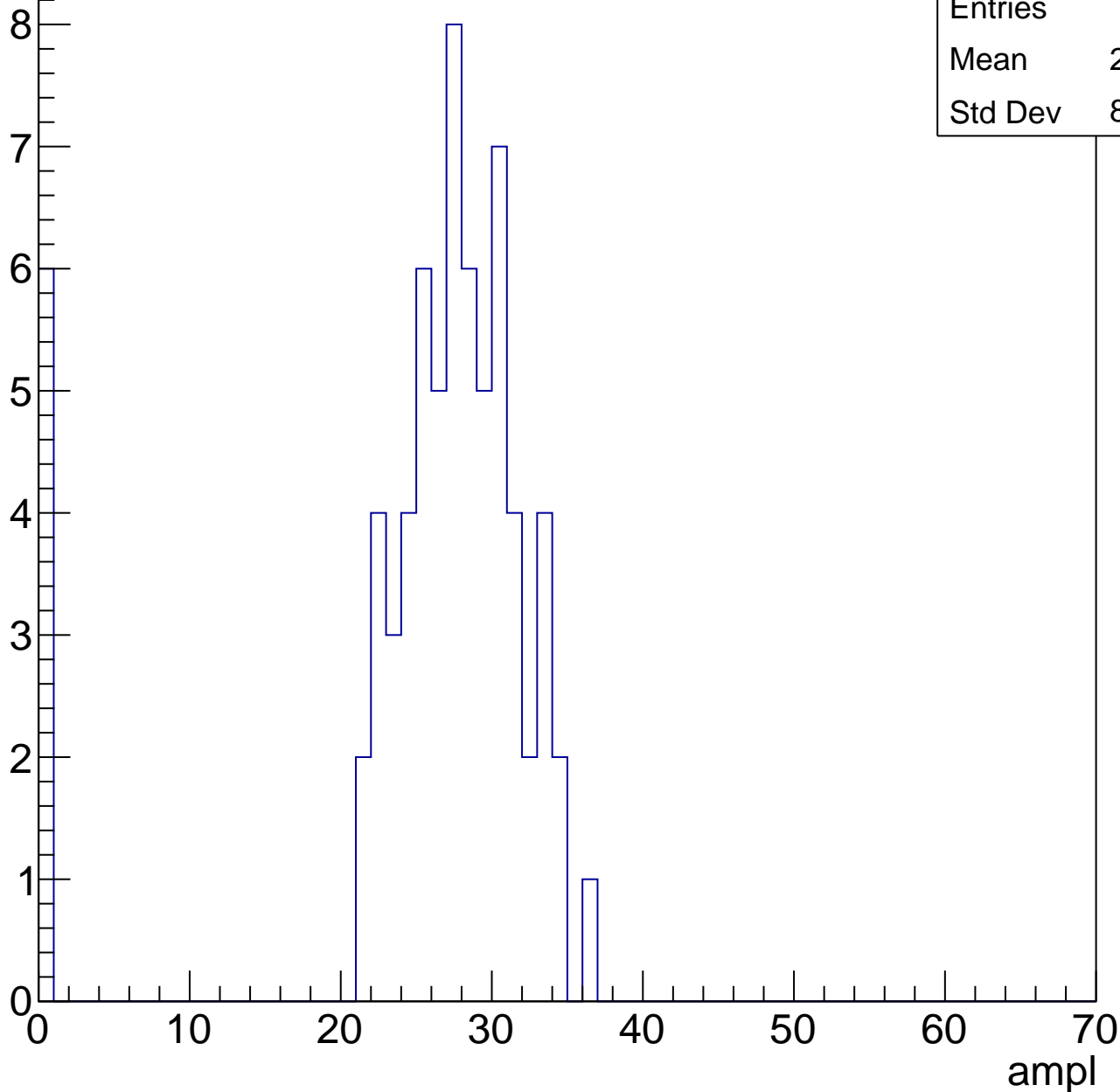


B1L103S, U11-ch72, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	25.19
Std Dev	8.477

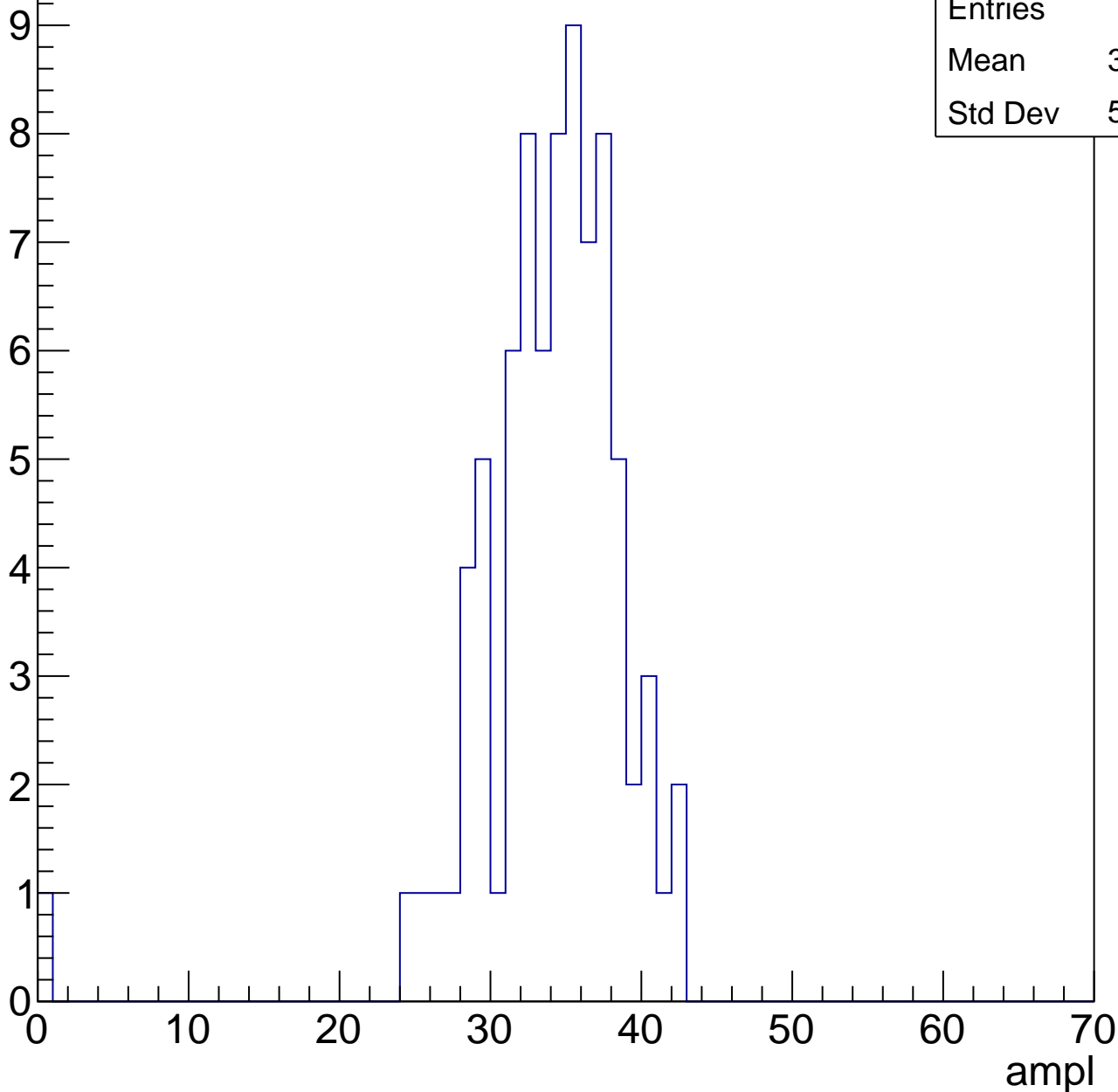


B1L103S, U11-ch72, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	80
Mean	33.46
Std Dev	5.394



B1L103S, U11-ch72, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	84
Mean	35.45
Std Dev	15.47

Entry

12

10

8

6

4

2

0

0

10

20

30

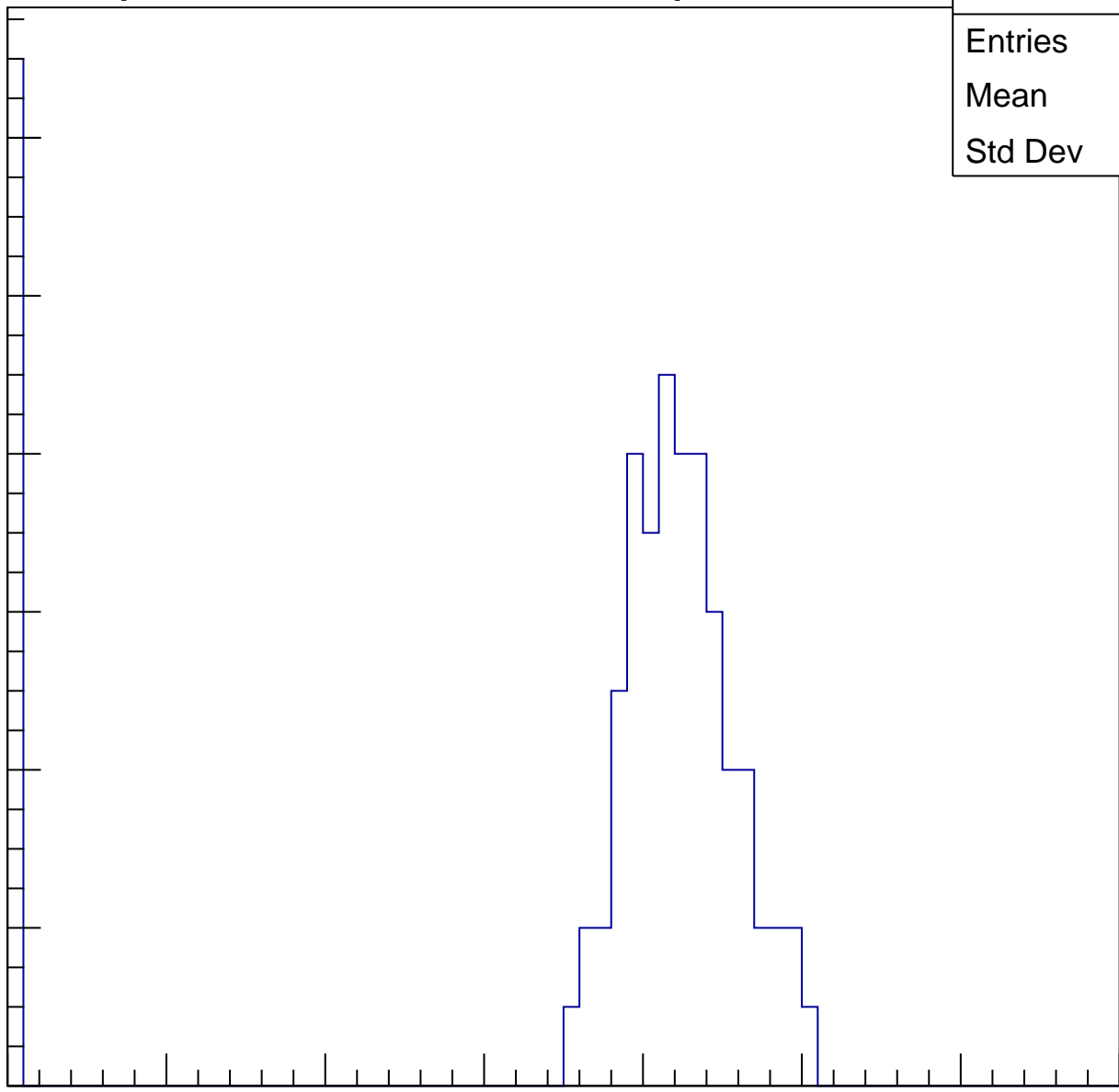
40

50

60

70

ampl

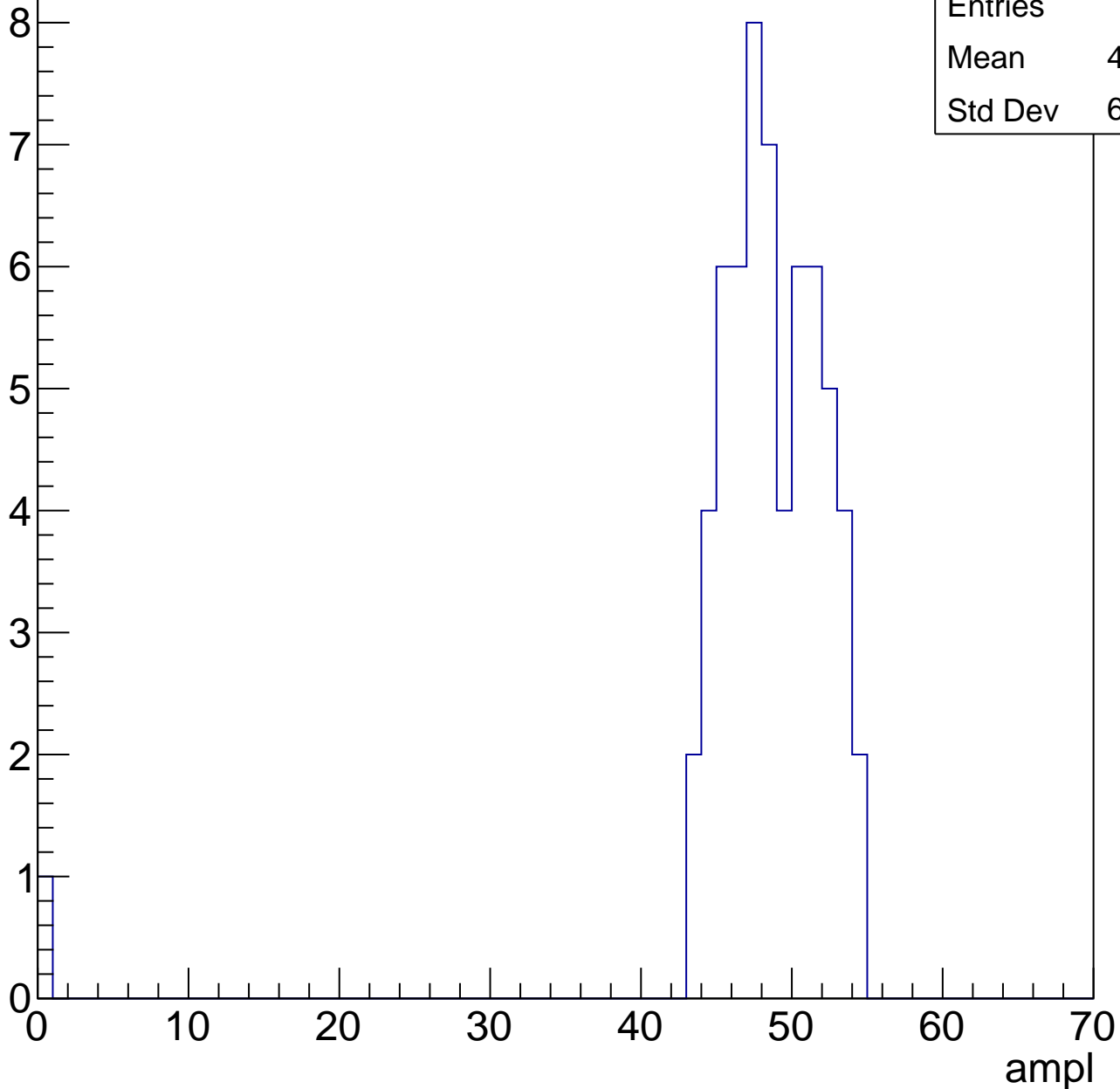


B1L103S, U11-ch72, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	47.57
Std Dev	6.808

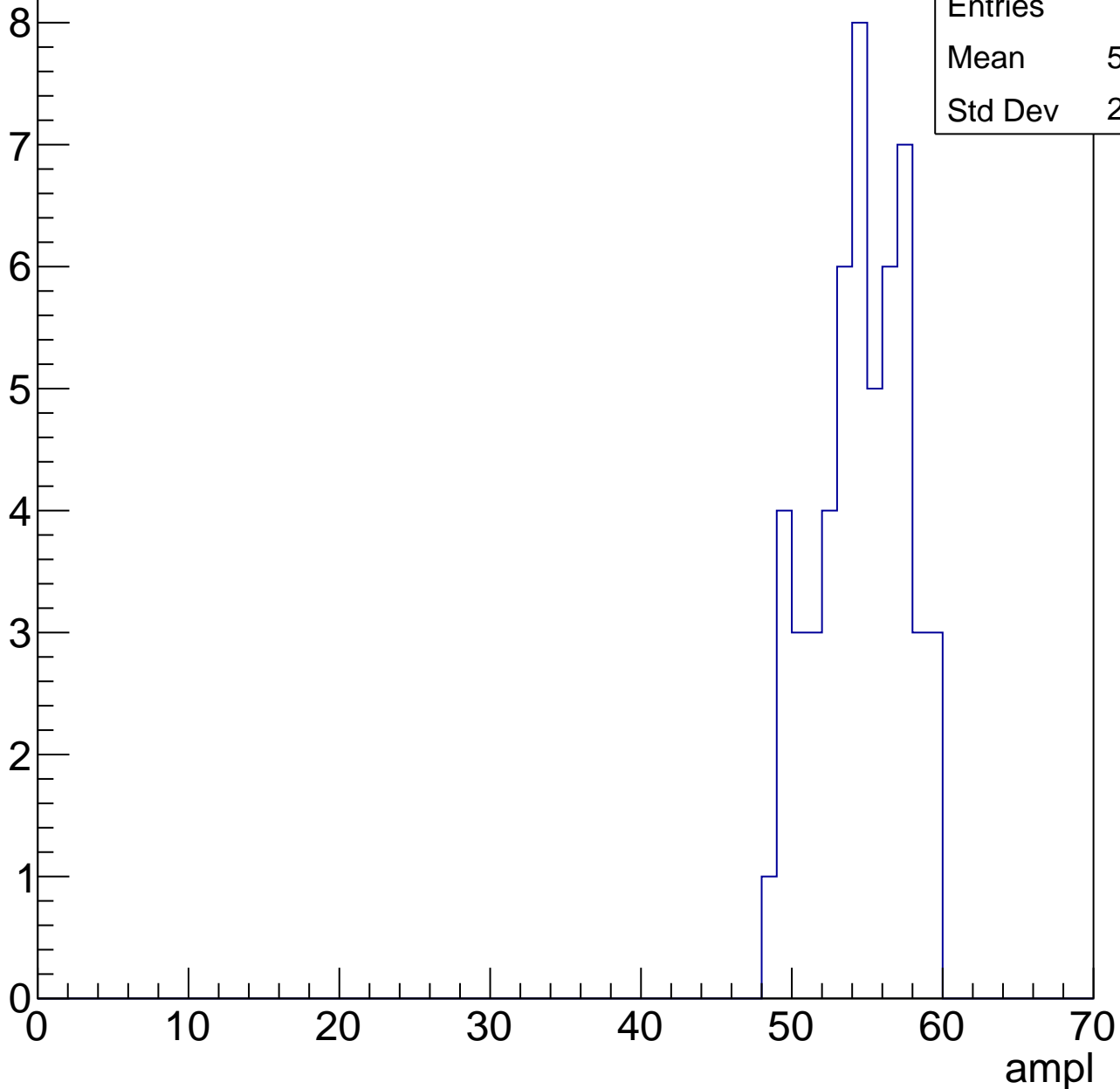


B1L103S, U11-ch72, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	54.08
Std Dev	2.906

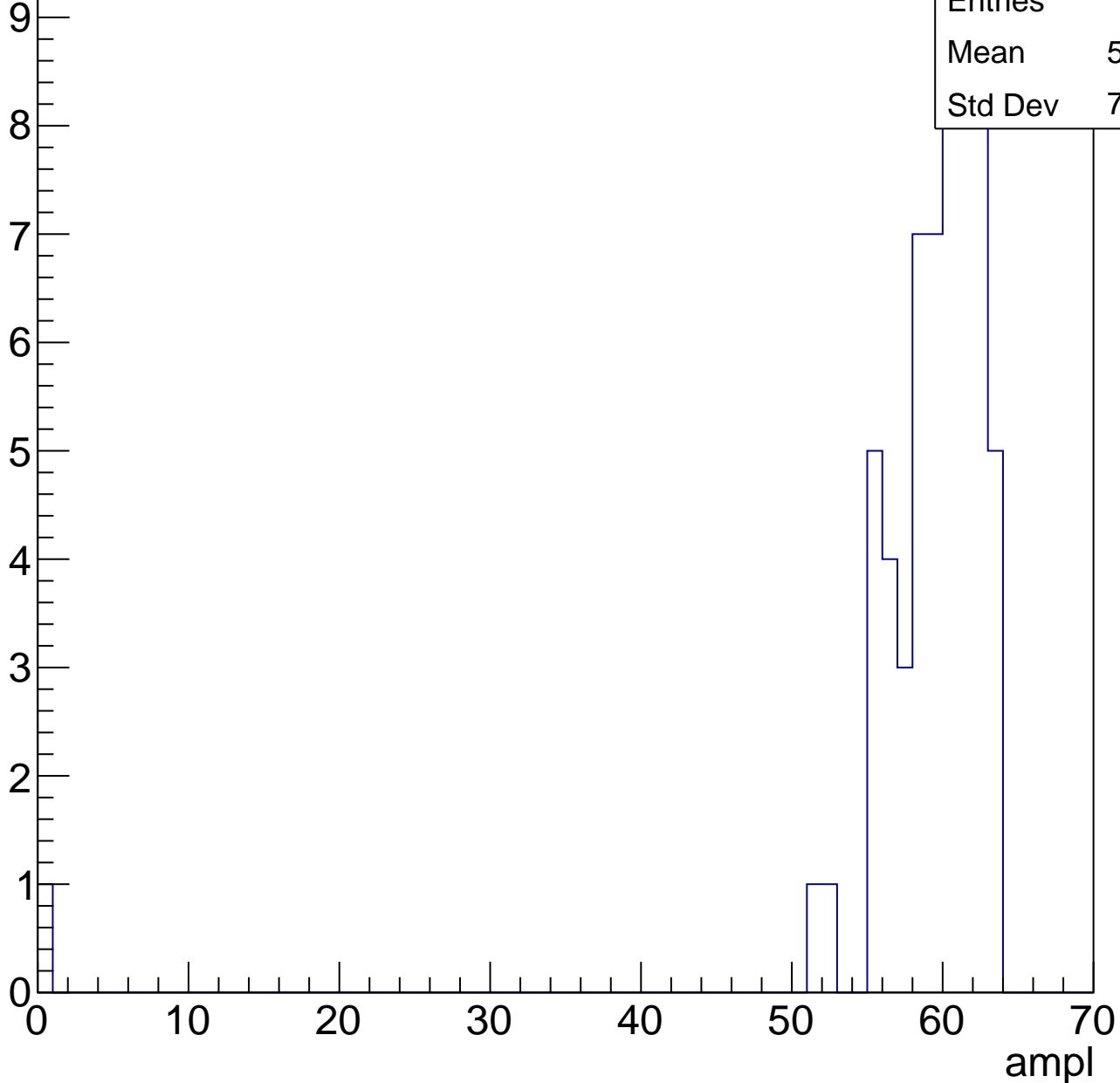


B1L103S, U11-ch72, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	58.26
Std Dev	7.998

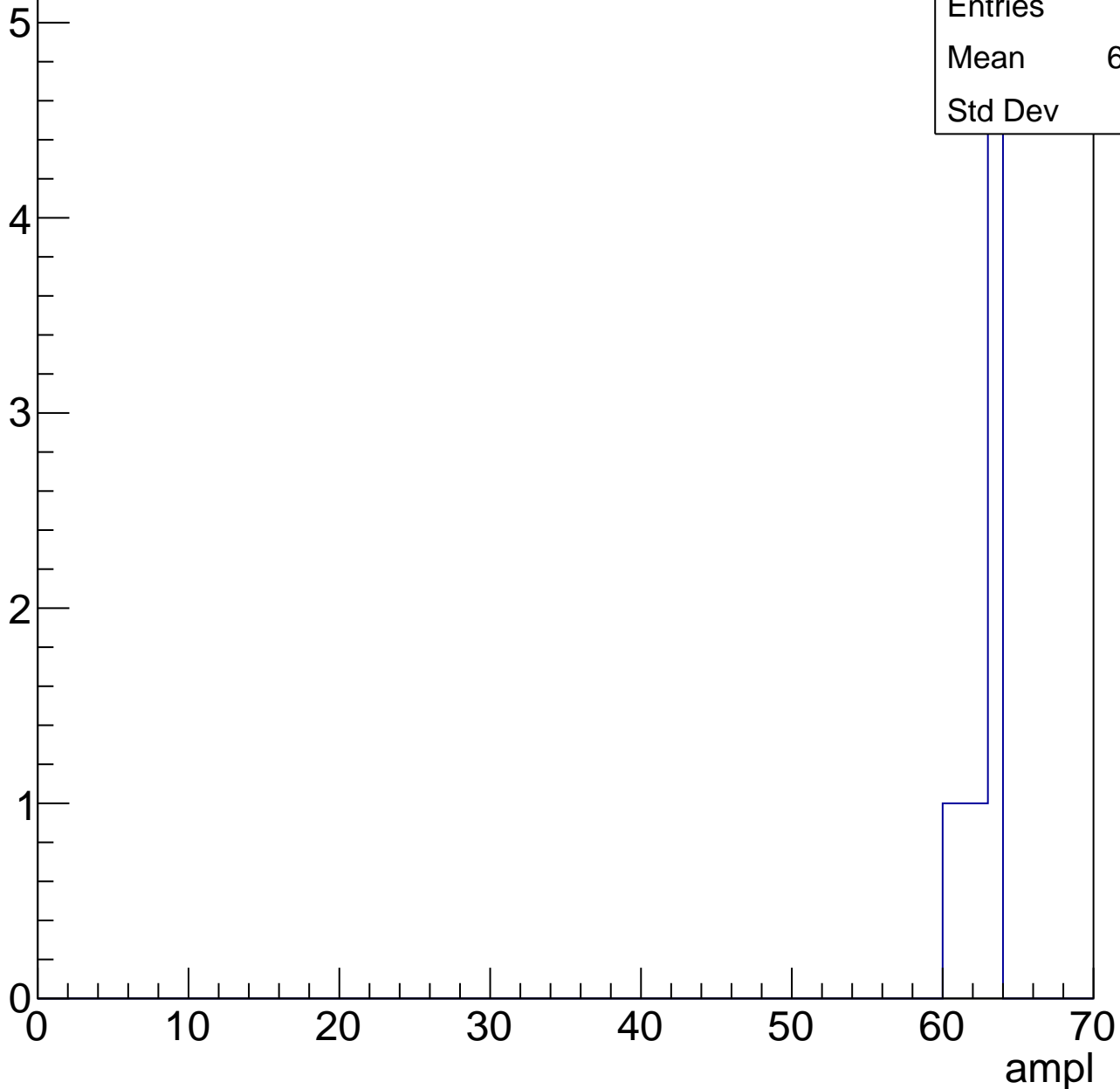


B1L103S, U11-ch72, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	8
Mean	62.25
Std Dev	1.09

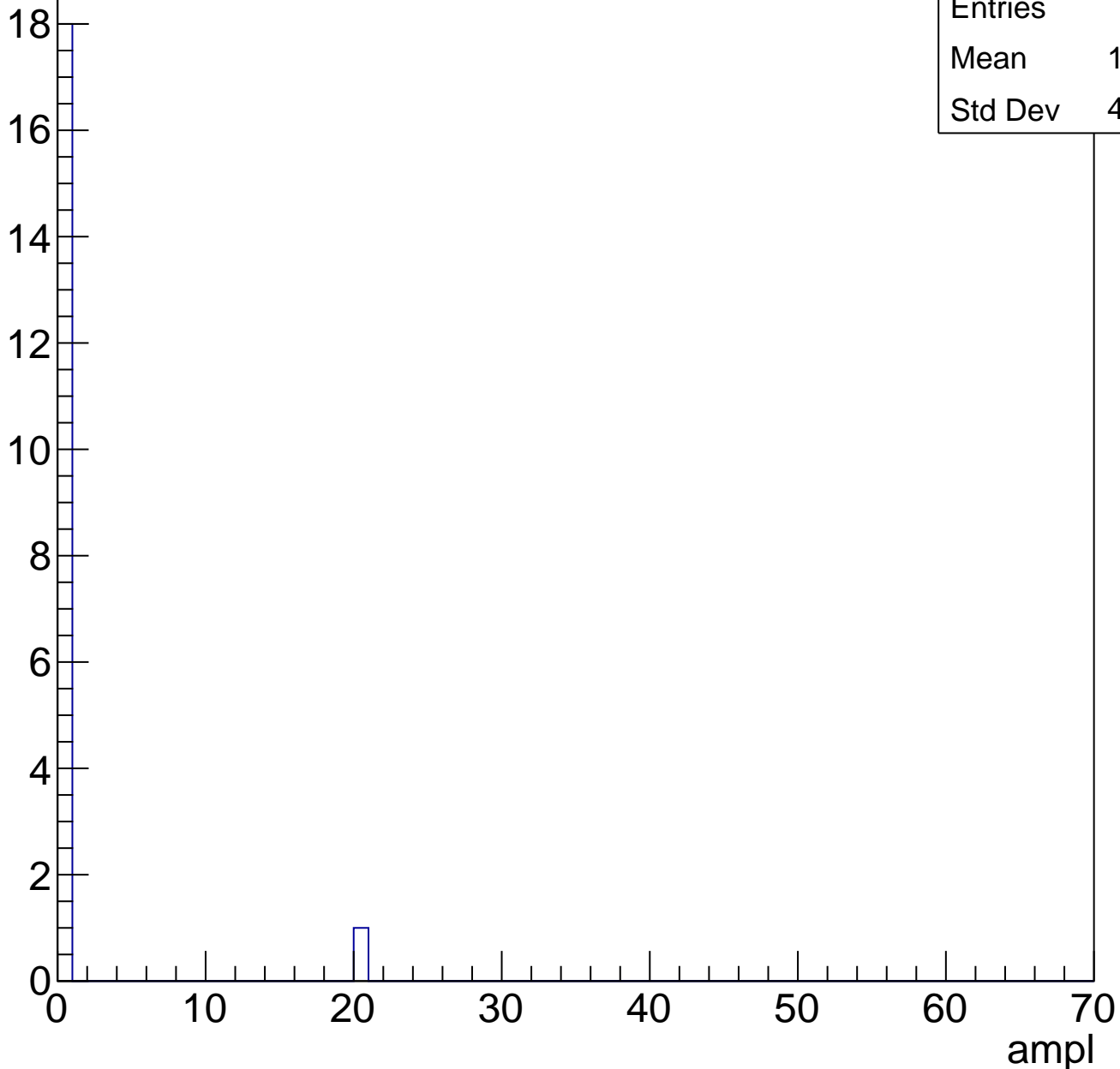


B1L103S, U11-ch72, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.053
Std Dev	4.466

Entry

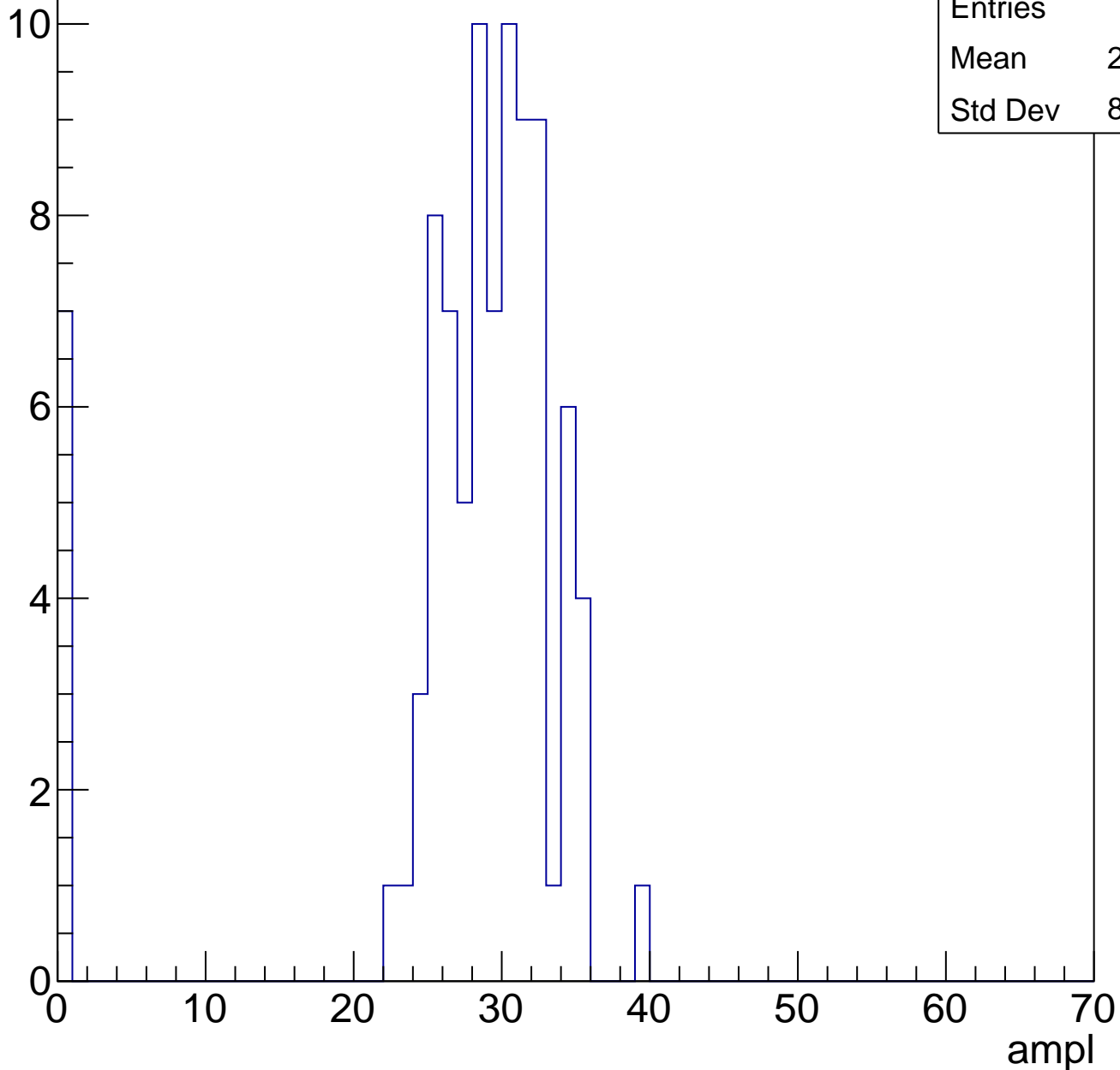


B1L103S, U11-ch73, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	26.97
Std Dev	8.504

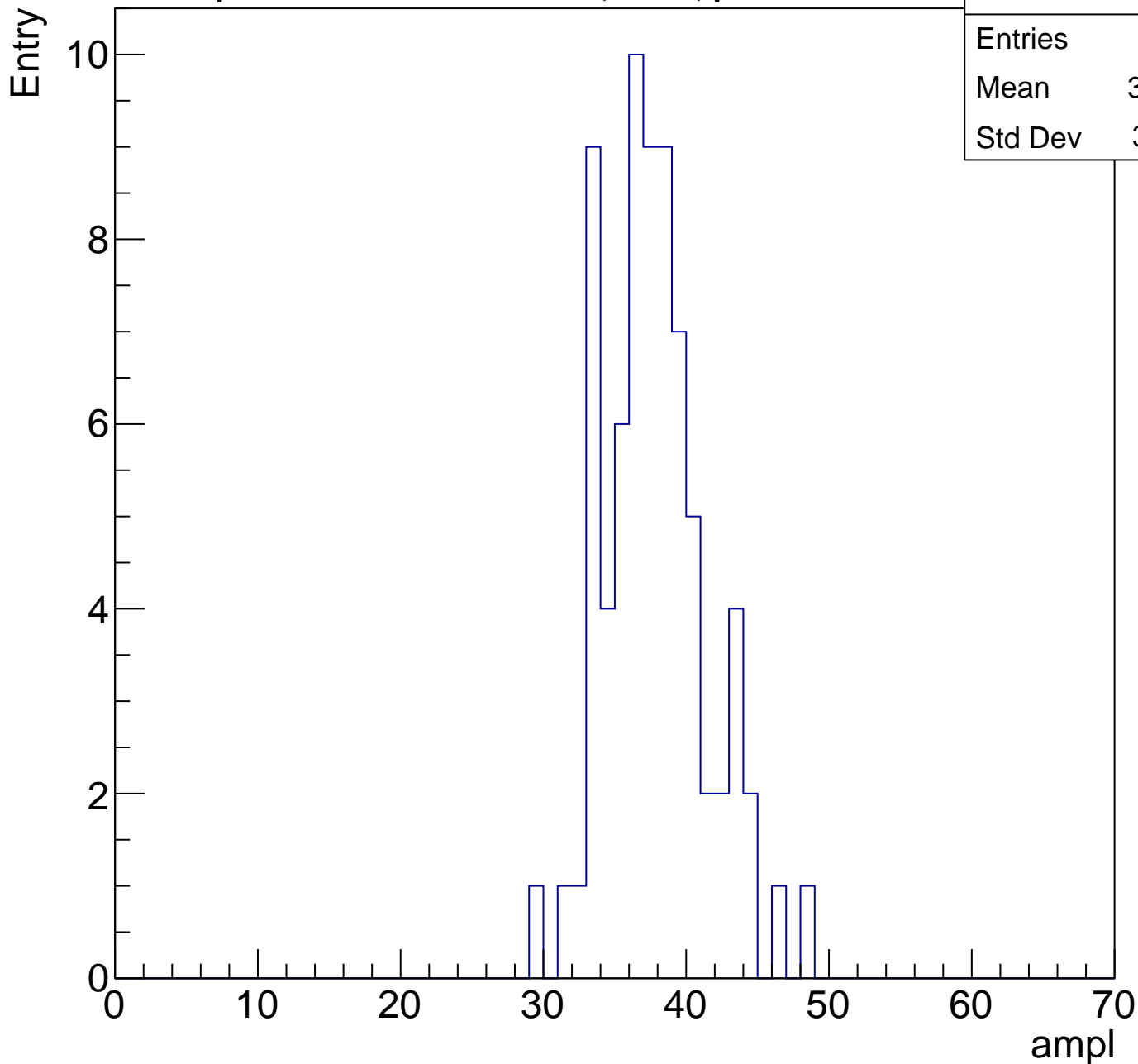
Entry



B1L103S, U11-ch73, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	74
Mean	37.34
Std Dev	3.561

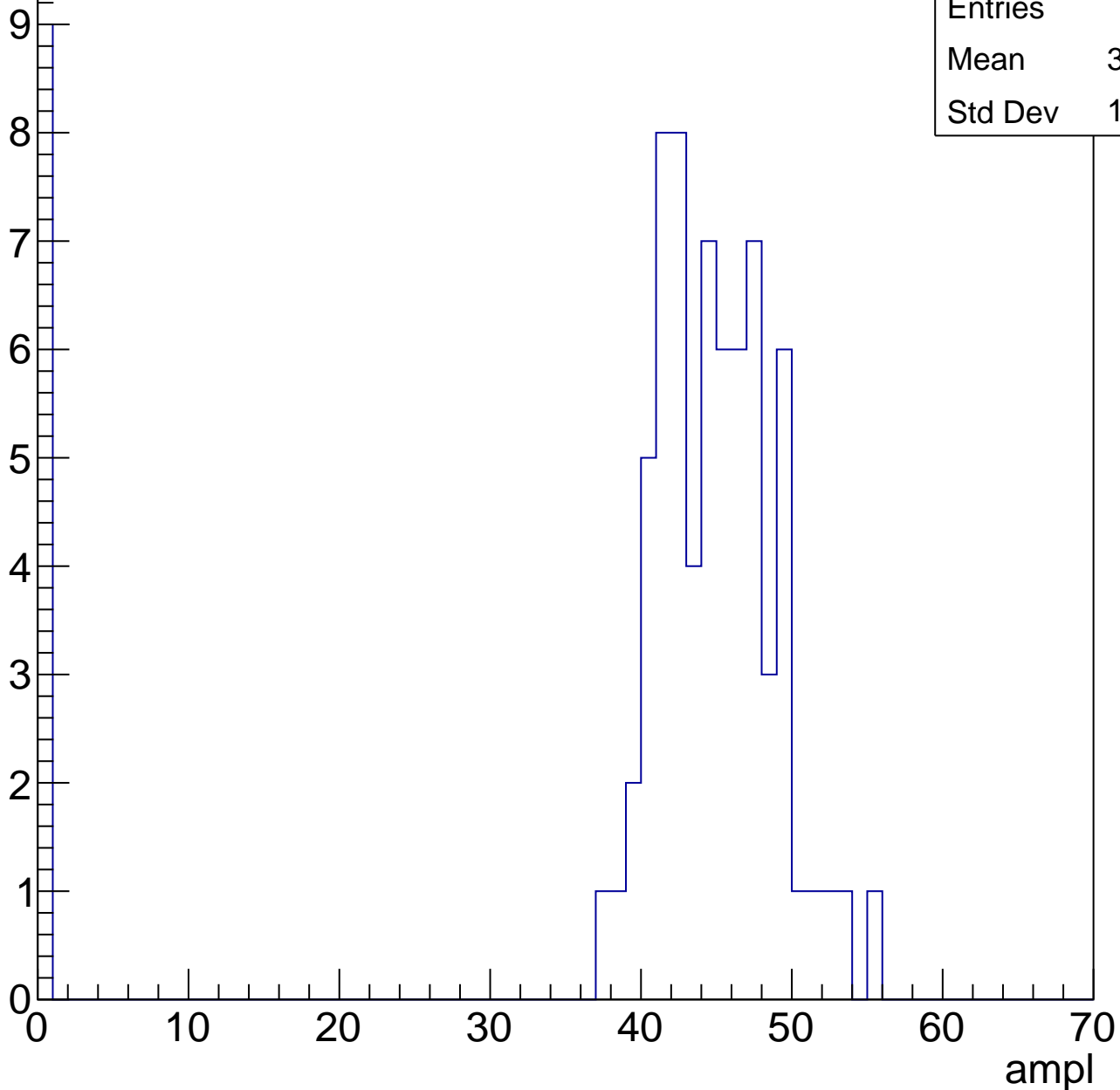


B1L103S, U11-ch73, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	39.37
Std Dev	14.64

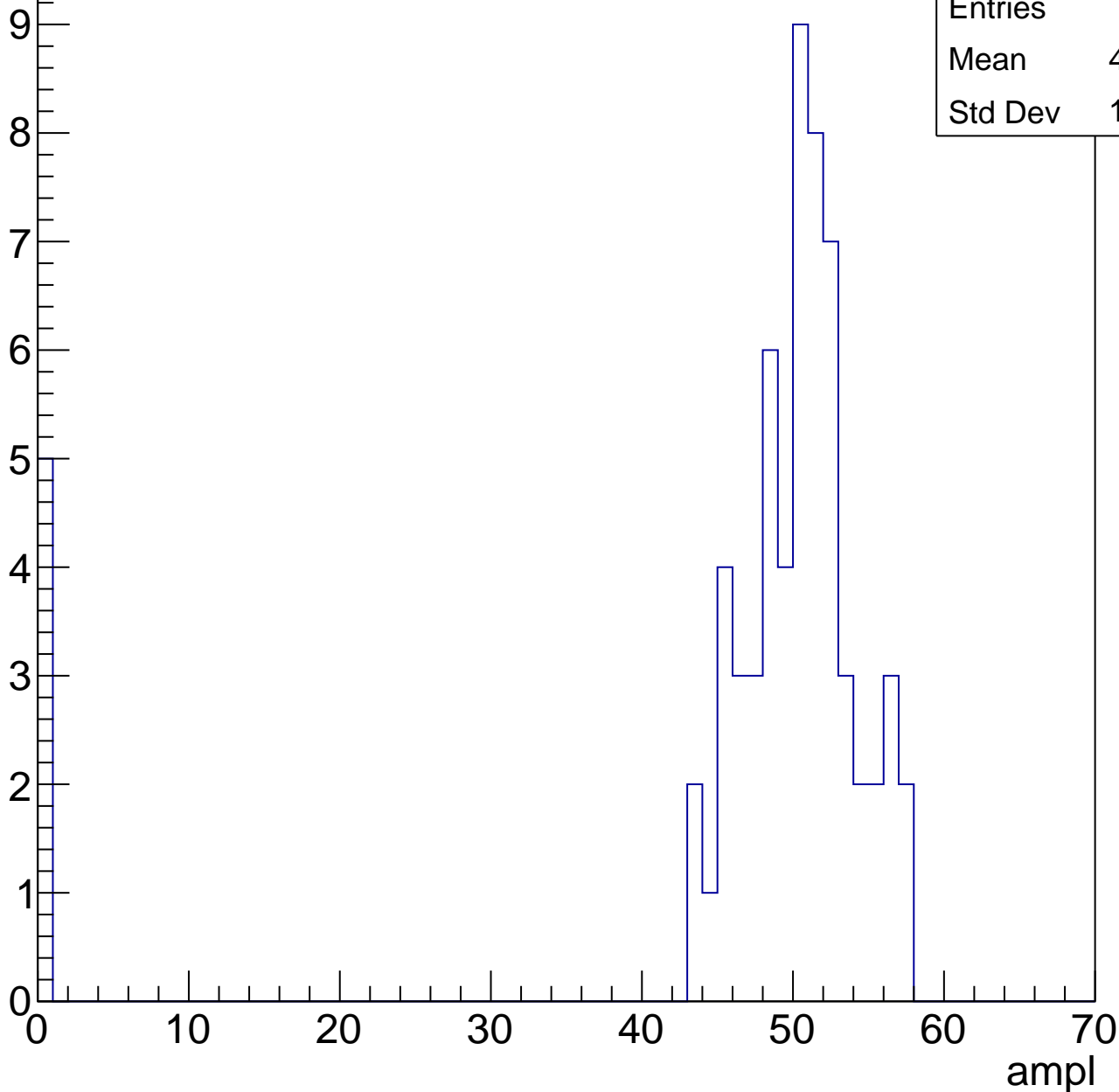


B1L103S, U11-ch73, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

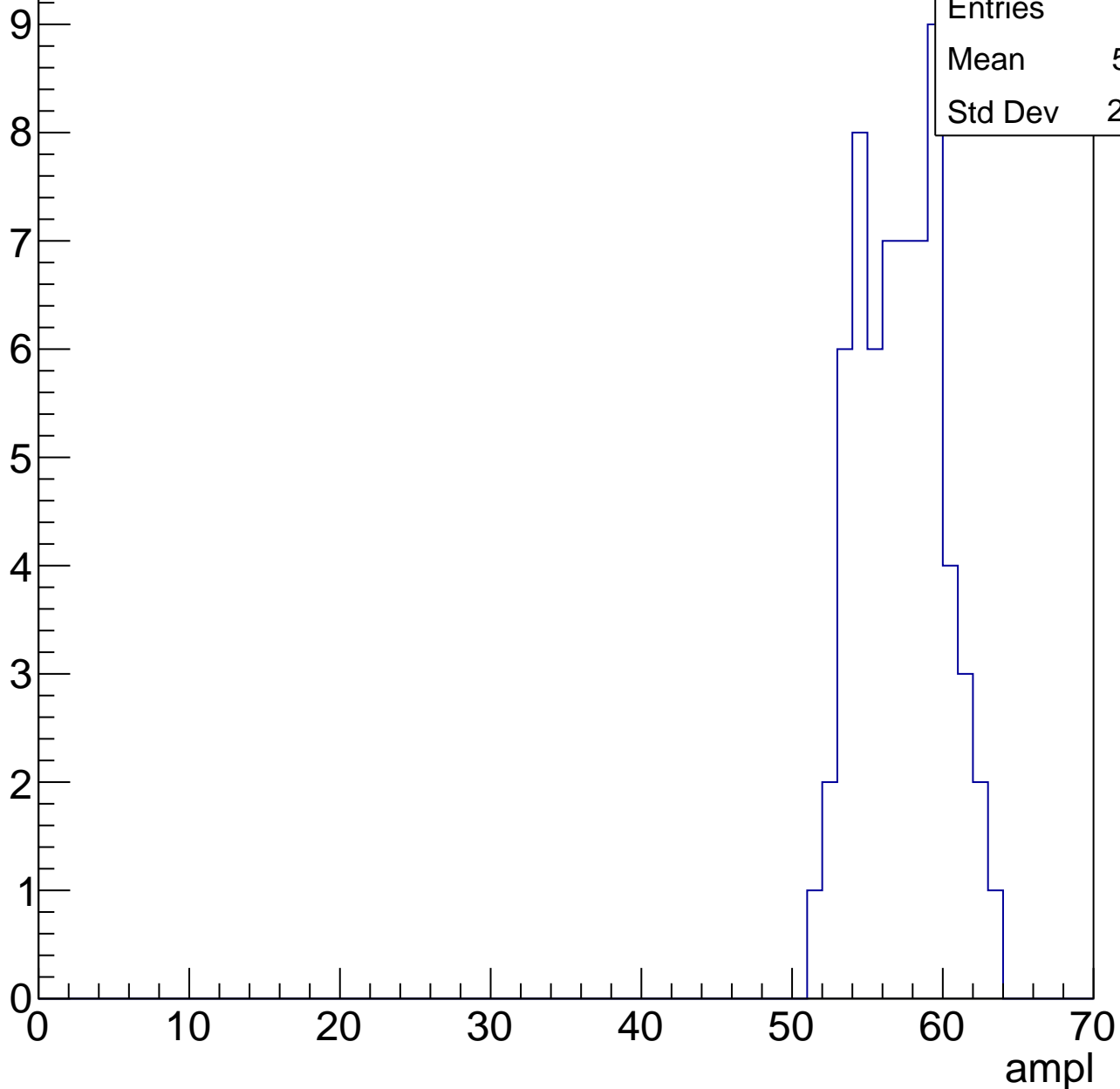
Entries	64
Mean	46.16
Std Dev	13.83



B1L103S, U11-ch73, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



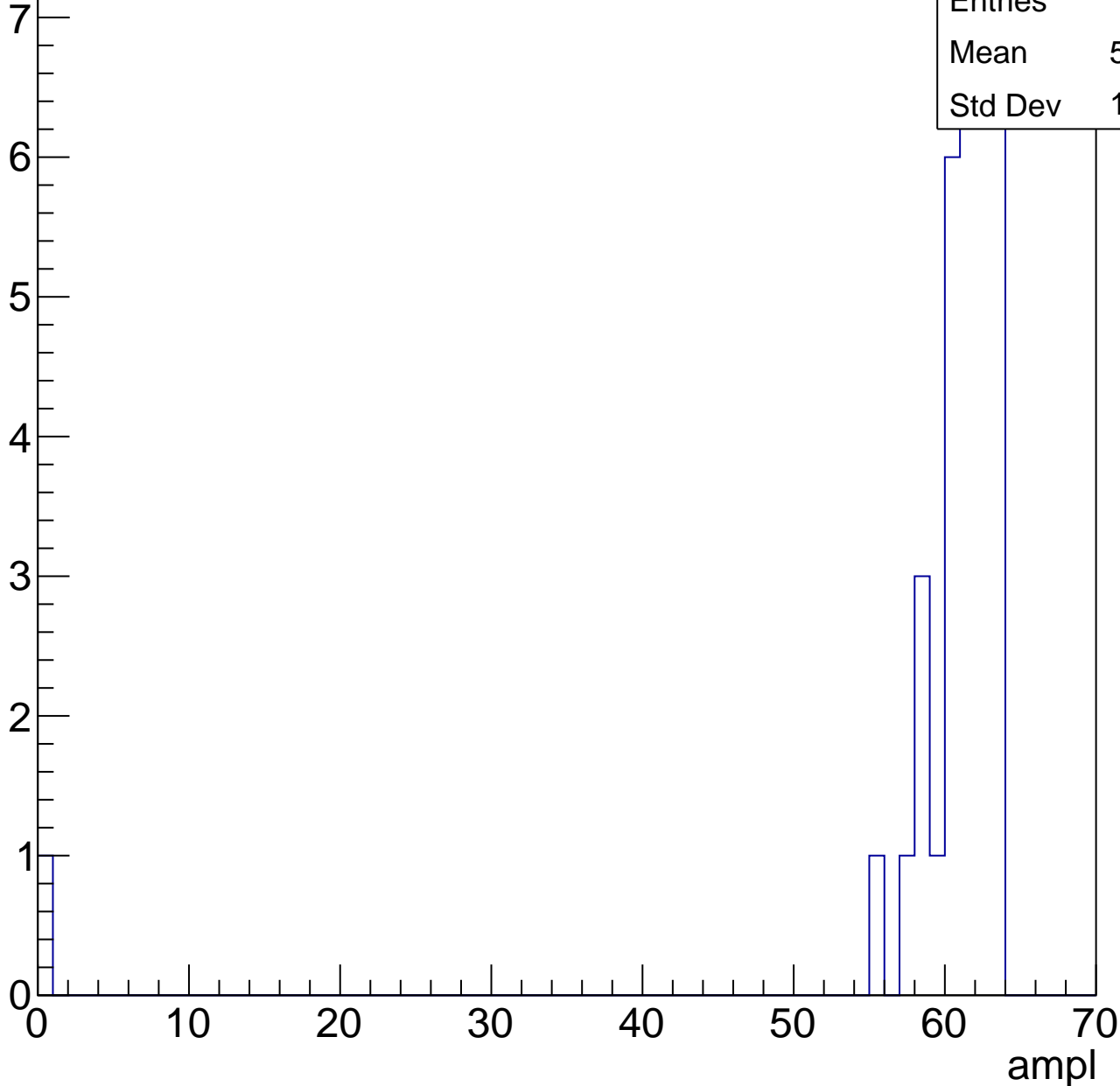
Entries	63
Mean	56.71
Std Dev	2.797

B1L103S, U11-ch73, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	34
Mean	59.03
Std Dev	10.45



B1L103S, U11-ch73, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch73, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

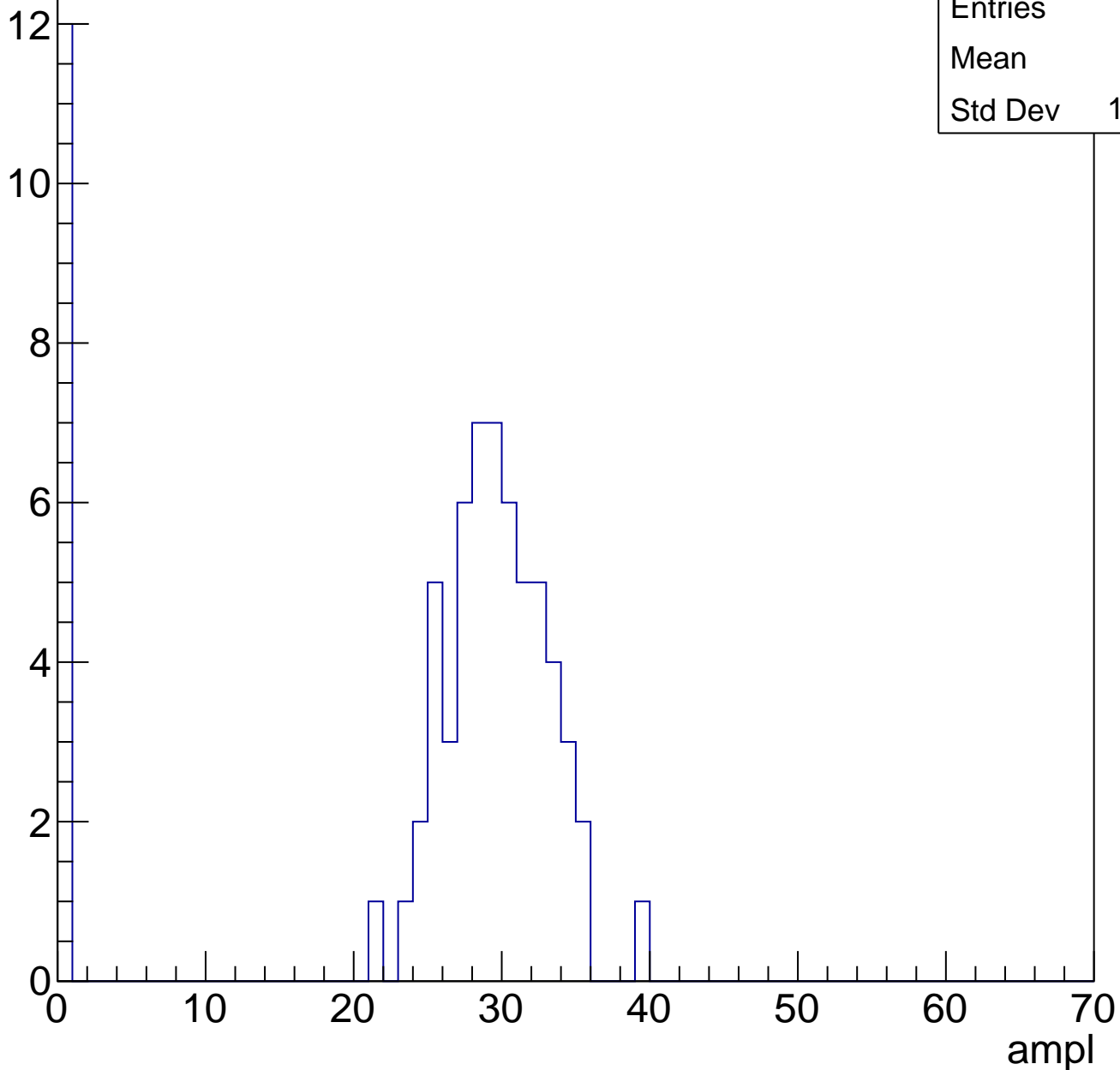


B1L103S, U11-ch74, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	70
Mean	24.2
Std Dev	11.43

Entry

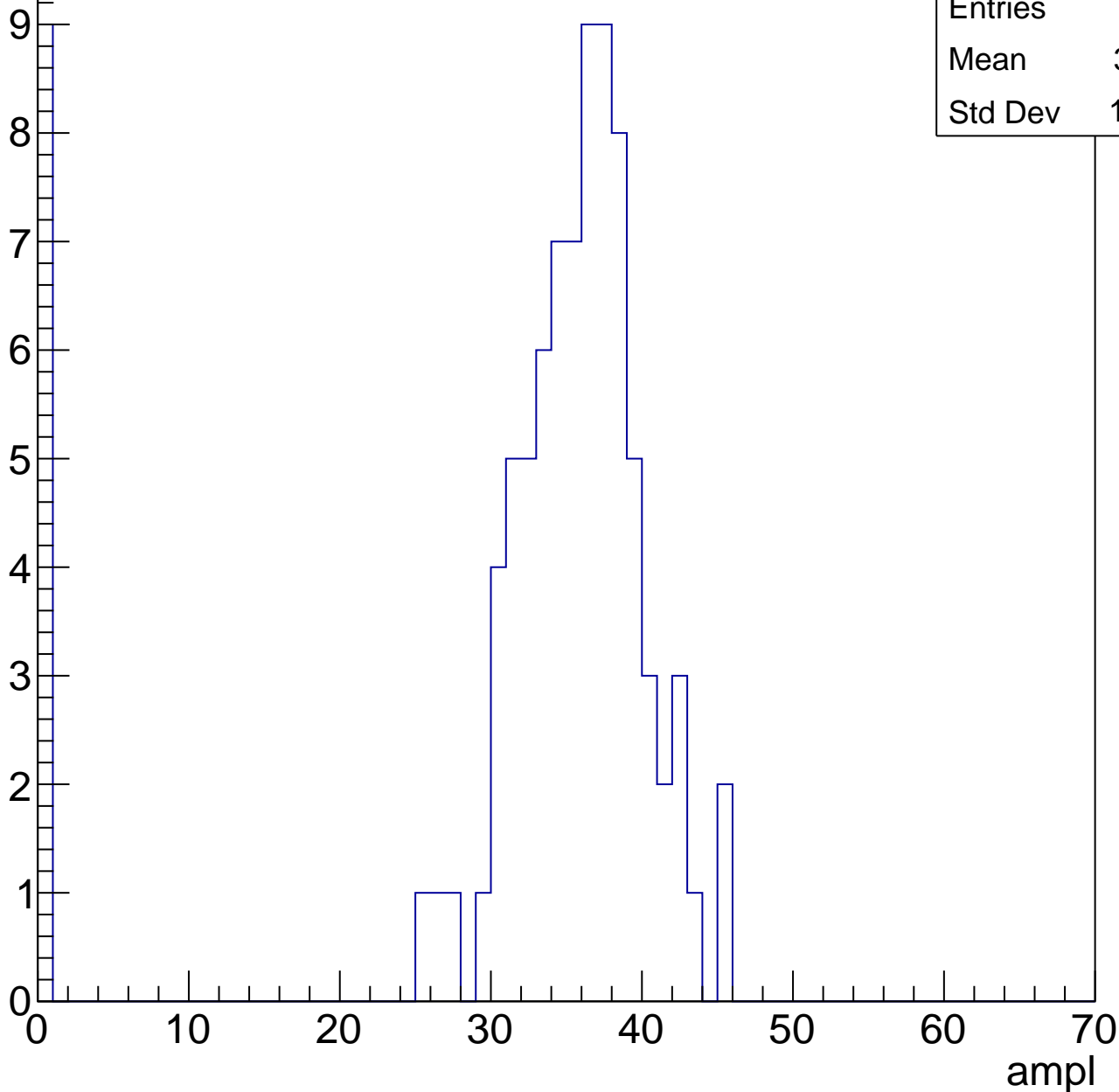


B1L103S, U11-ch74, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

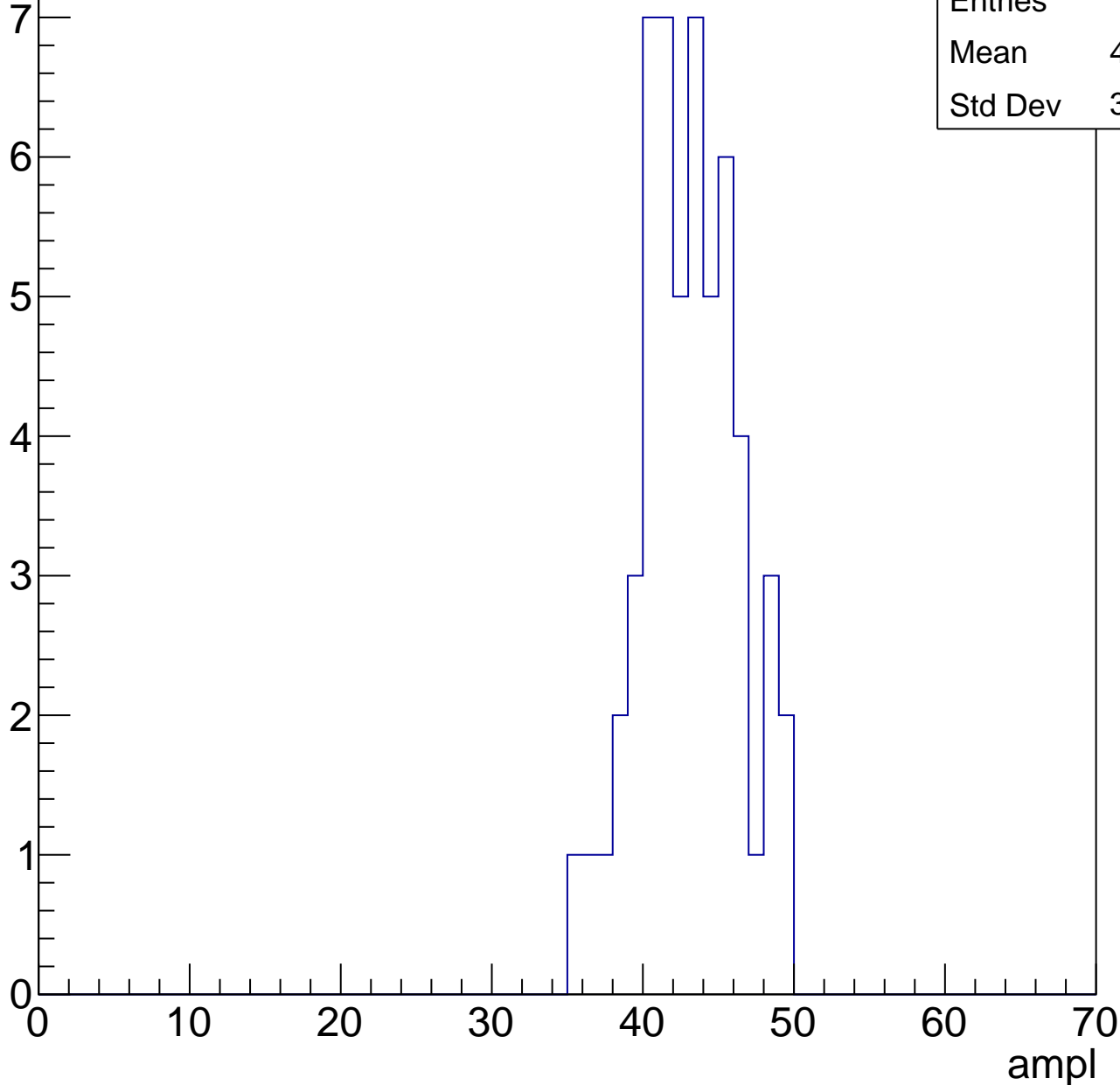
Entries	89
Mean	31.91
Std Dev	11.35



B1L103S, U11-ch74, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry



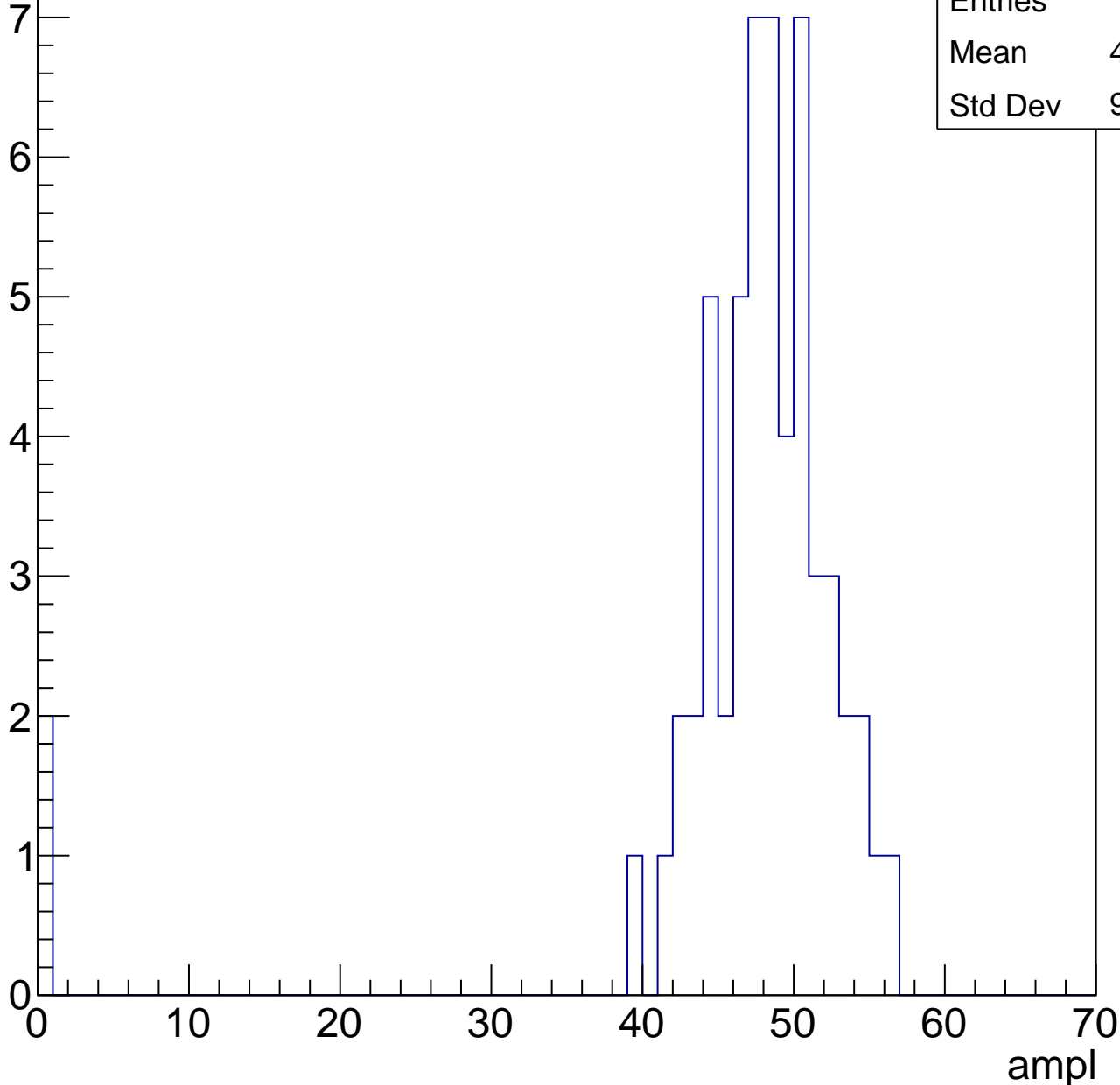
Entries	55
Mean	42.58
Std Dev	3.195

B1L103S, U11-ch74, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	46.23
Std Dev	9.503

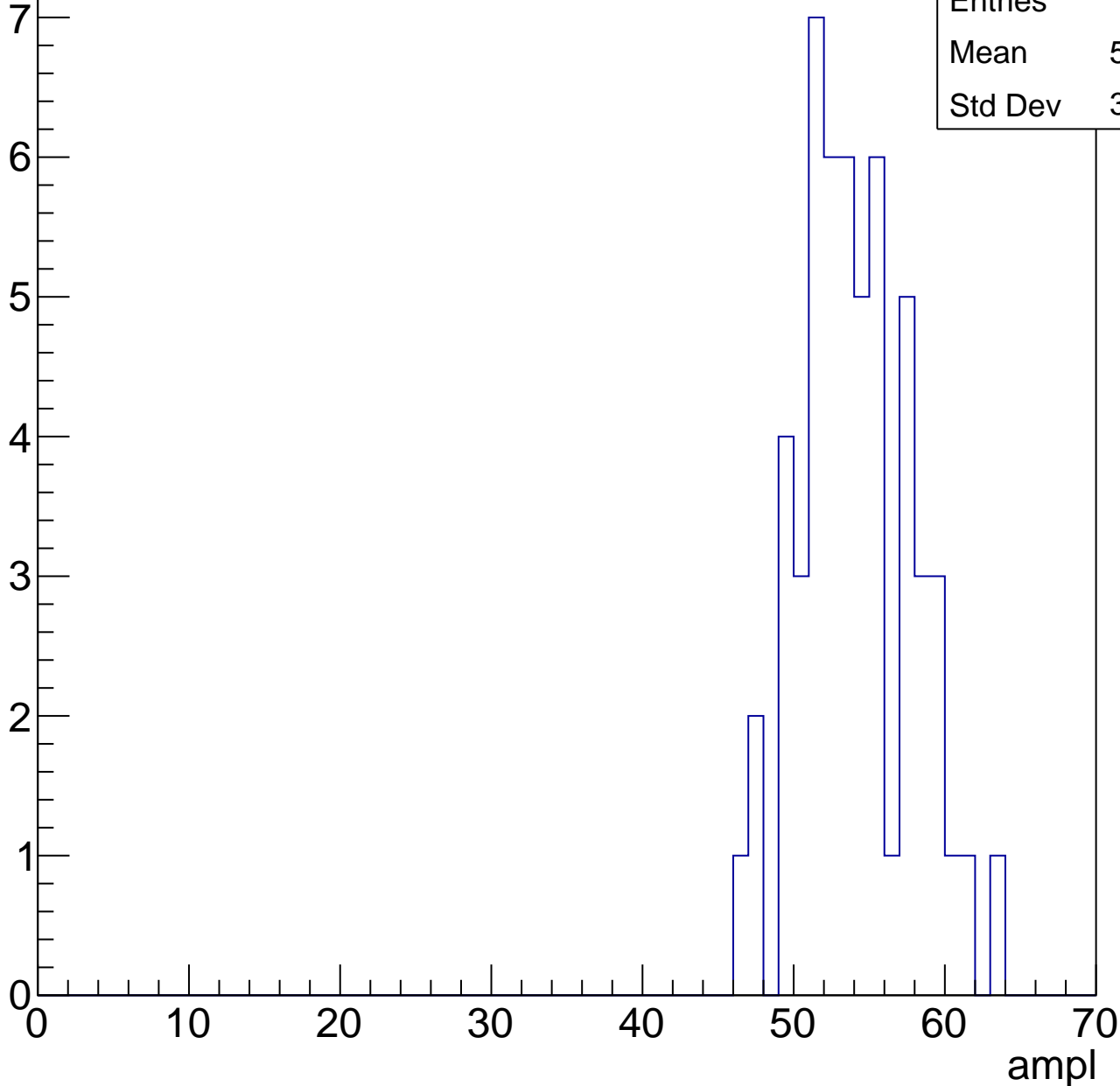


B1L103S, U11-ch74, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	53.62
Std Dev	3.666

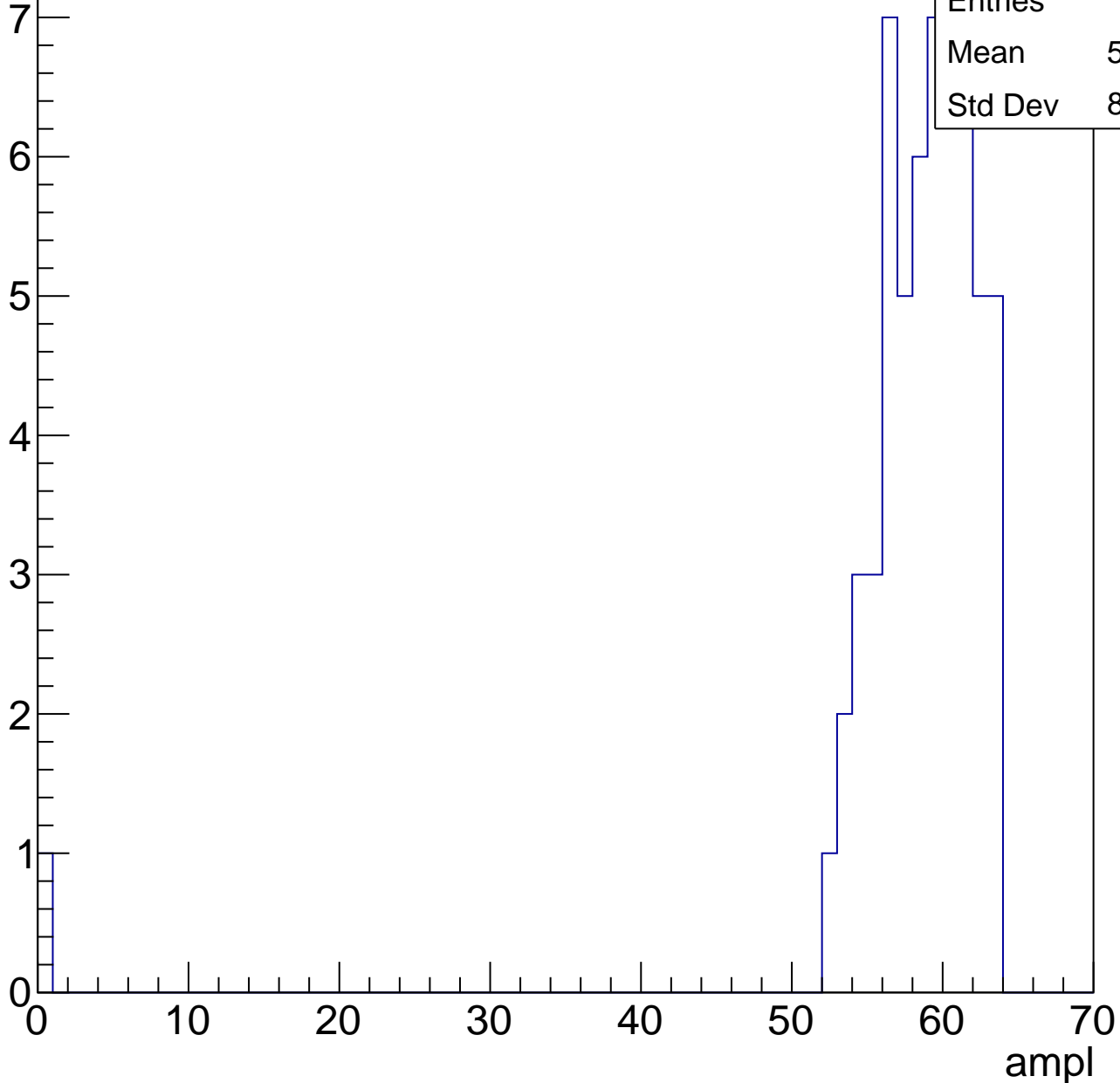


B1L103S, U11-ch74, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	57.54
Std Dev	8.077

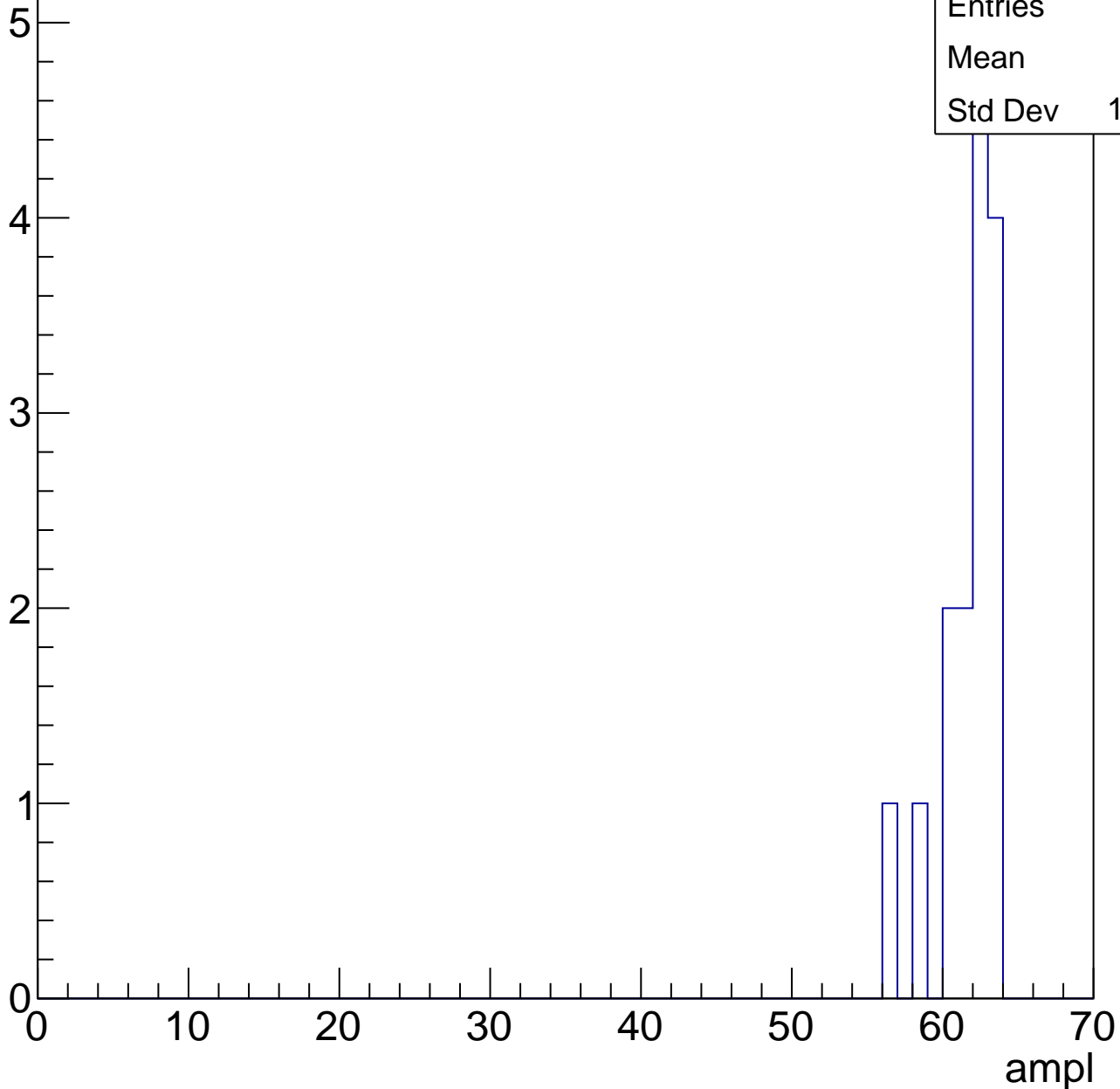


B1L103S, U11-ch74, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	15
Mean	61.2
Std Dev	1.939



B1L103S, U11-ch74, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.105
Std Dev	4.689

Entry

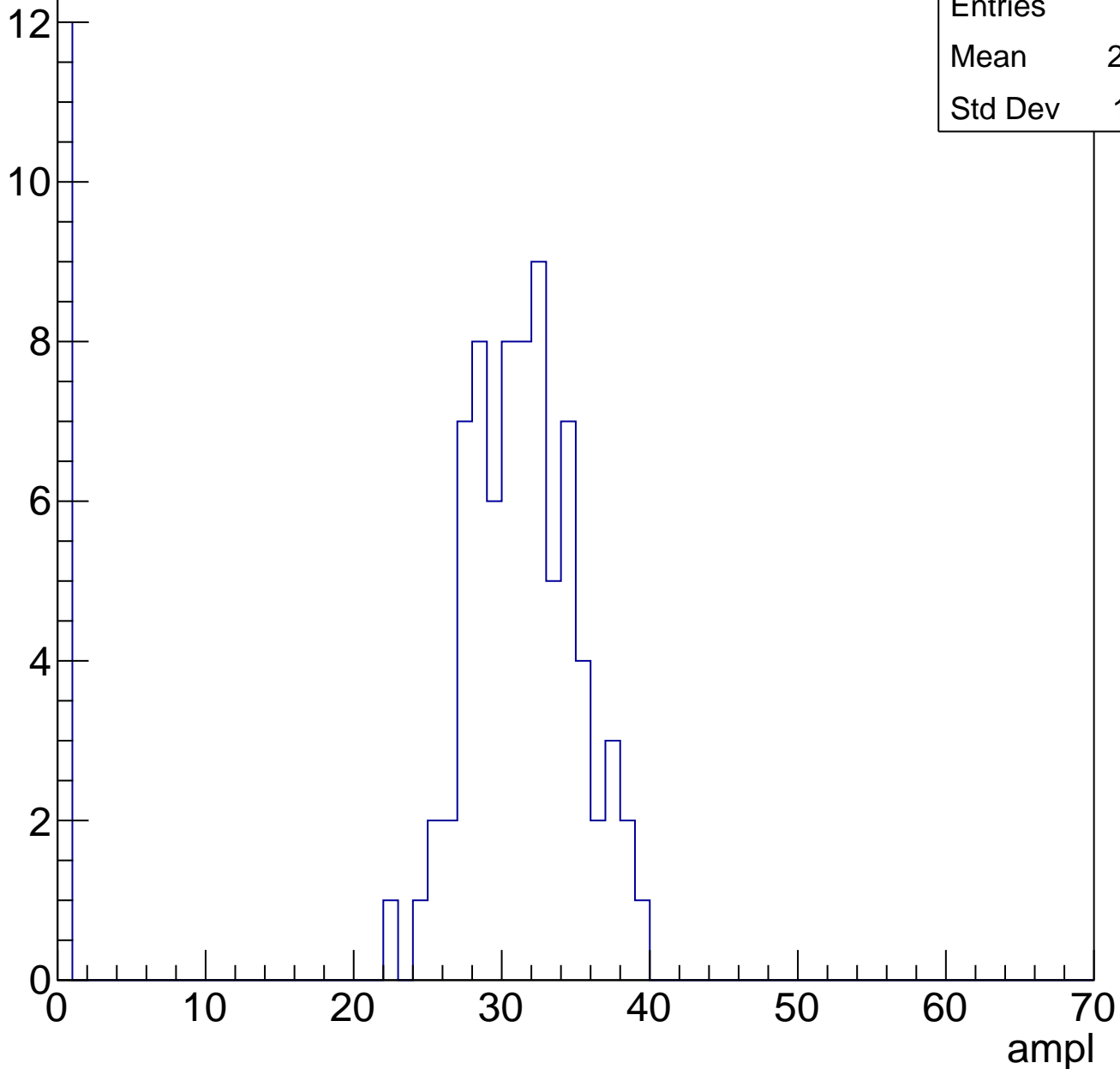


B1L103S, U11-ch75, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	88
Mean	26.73
Std Dev	11.11

Entry

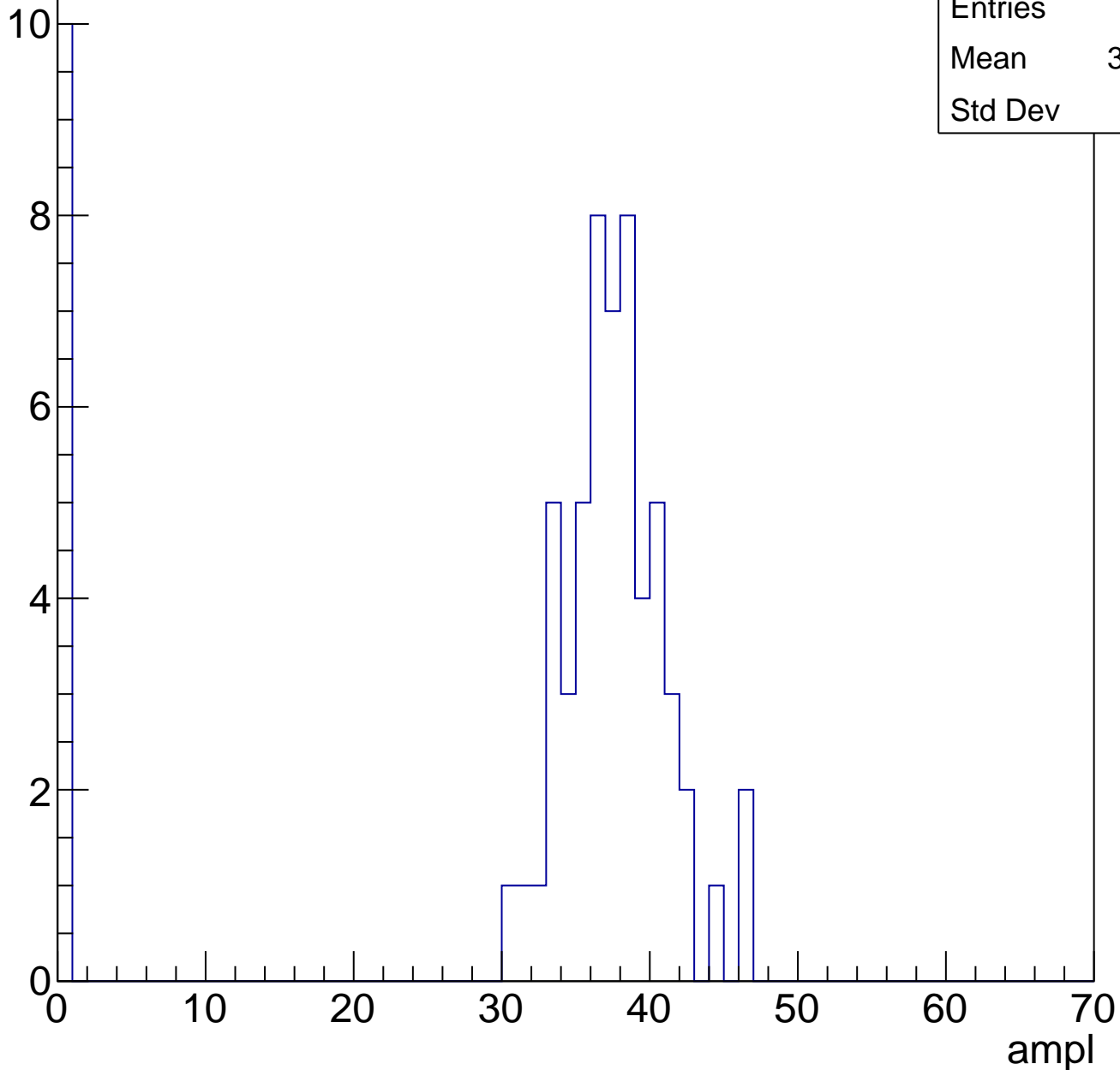


B1L103S, U11-ch75, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	66
Mean	31.59
Std Dev	13.7

Entry

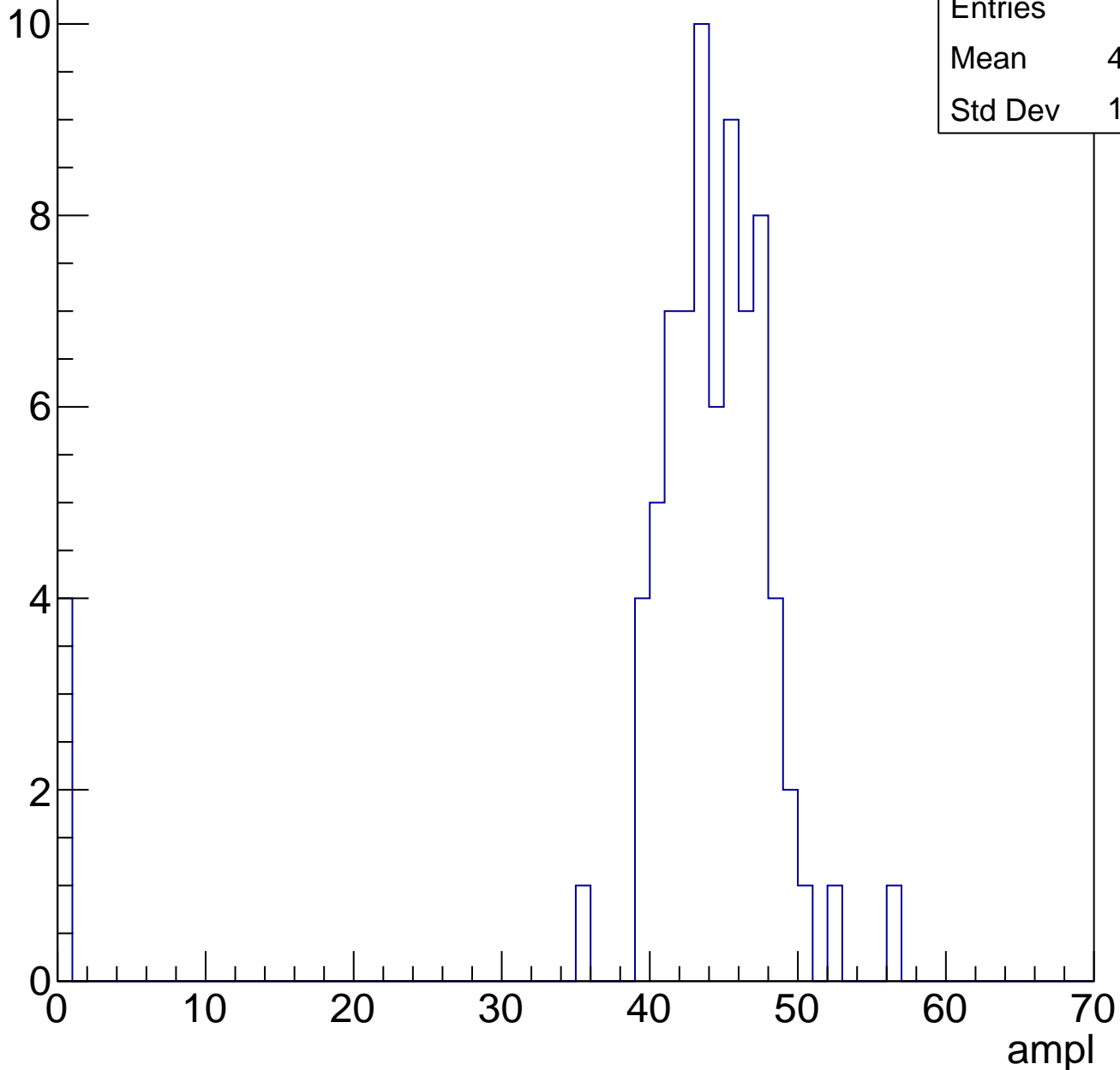


B1L103S, U11-ch75, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	77
Mean	41.78
Std Dev	10.32

Entry

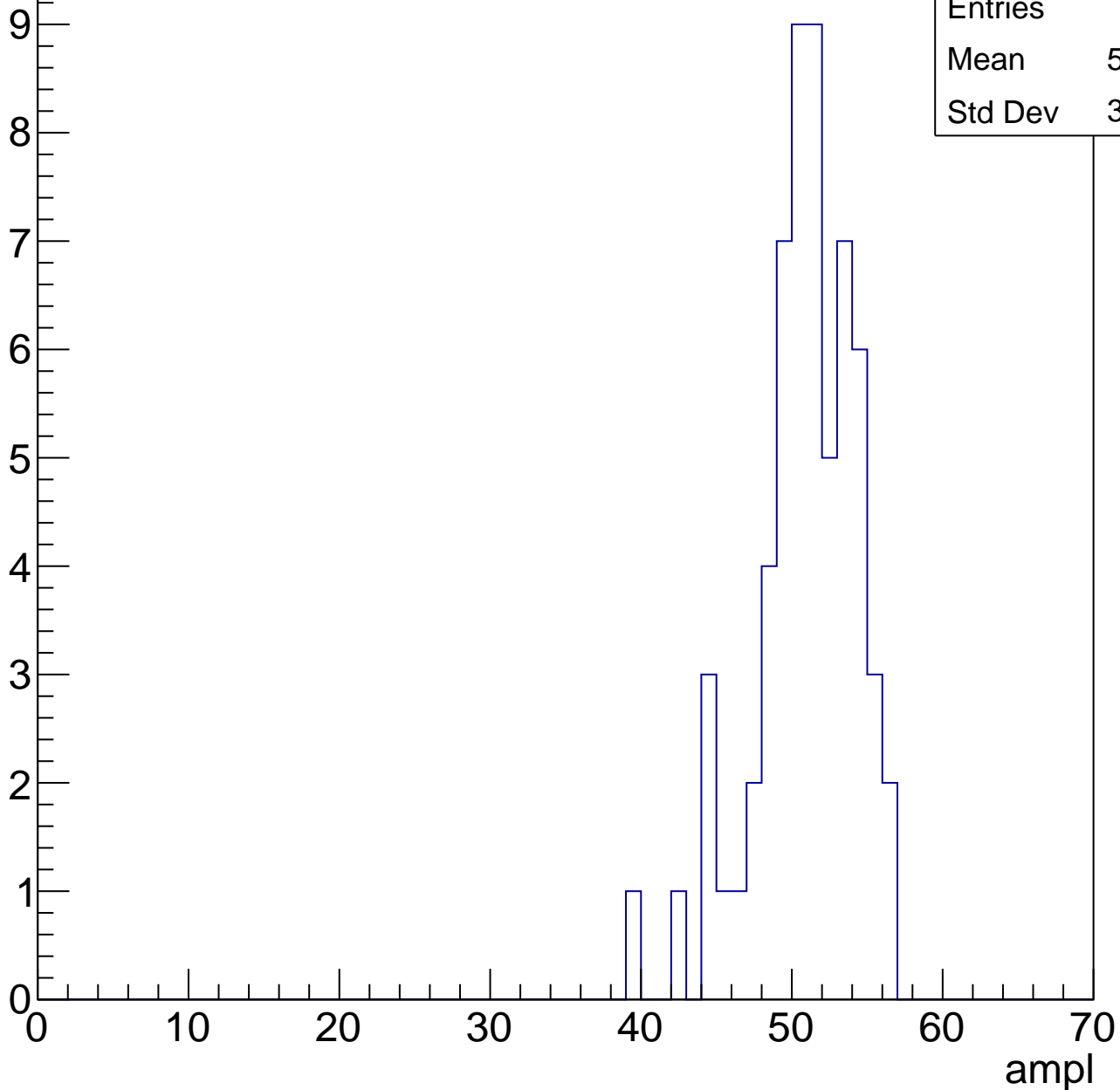


B1L103S, U11-ch75, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	50.39
Std Dev	3.389

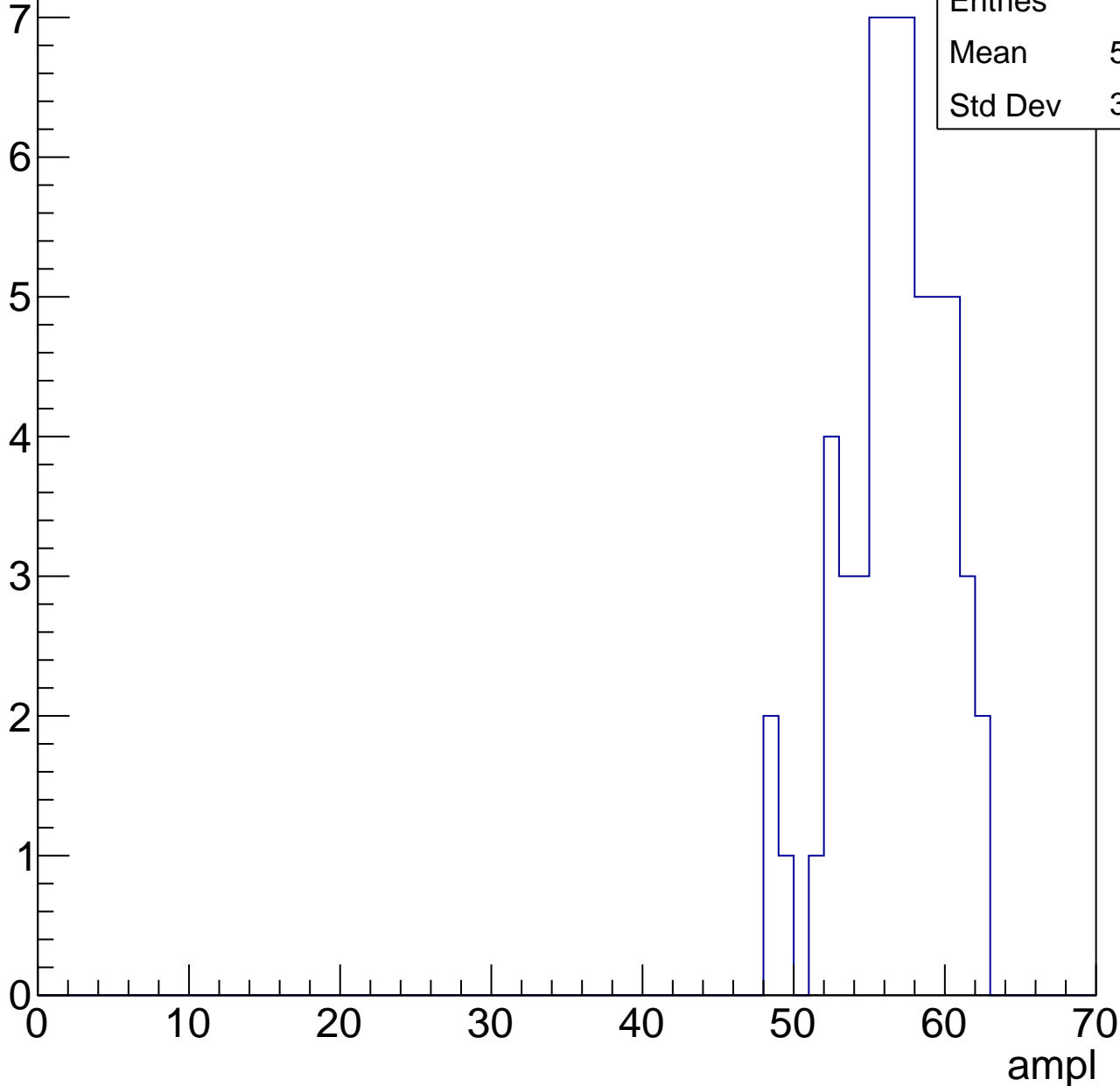


B1L103S, U11-ch75, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	56.24
Std Dev	3.325

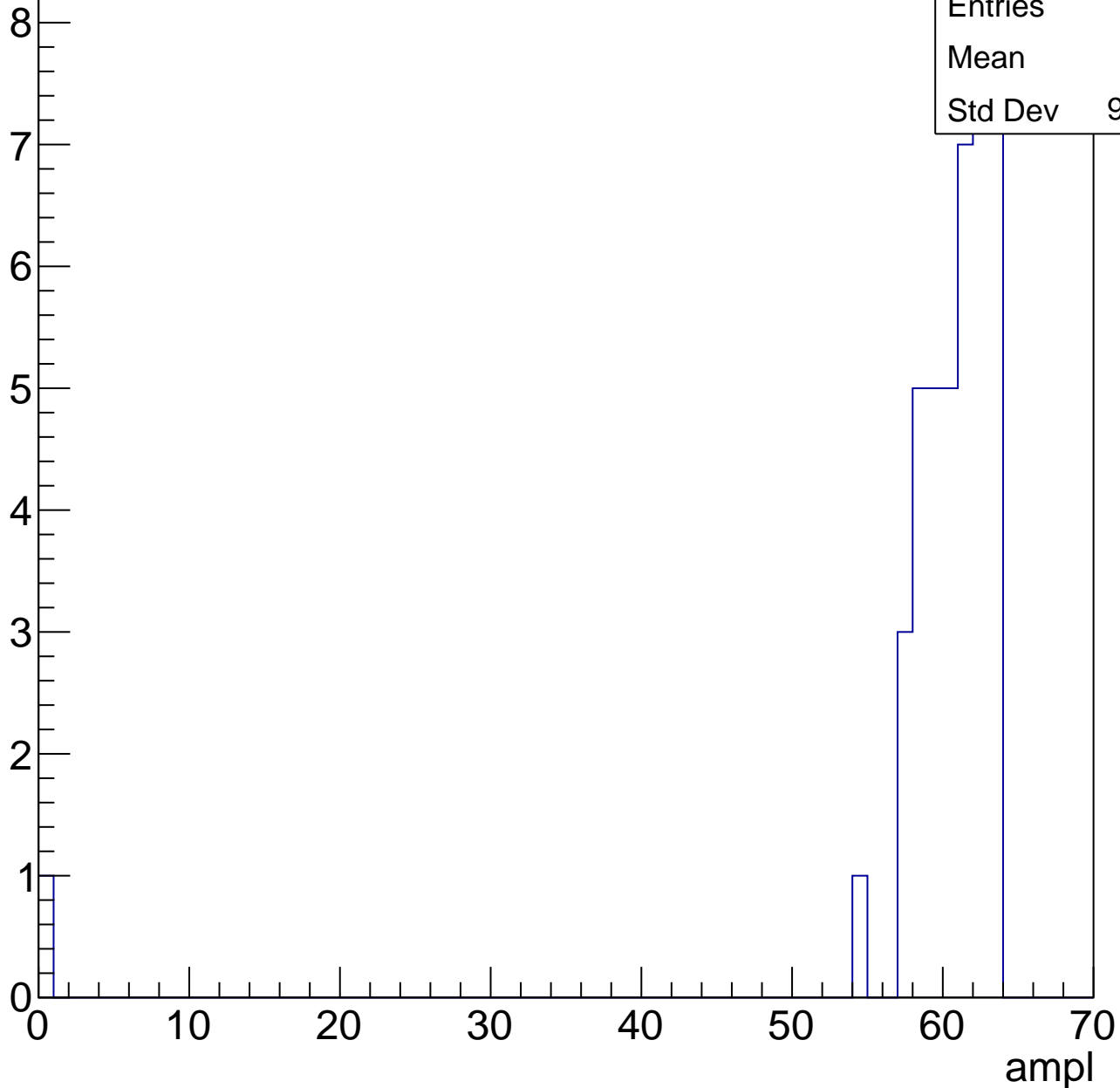


B1L103S, U11-ch75, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	43
Mean	59
Std Dev	9.346



B1L103S, U11-ch75, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch75, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch76, adc0

calib_packv5_041523_1651.root, FC#0, port C2

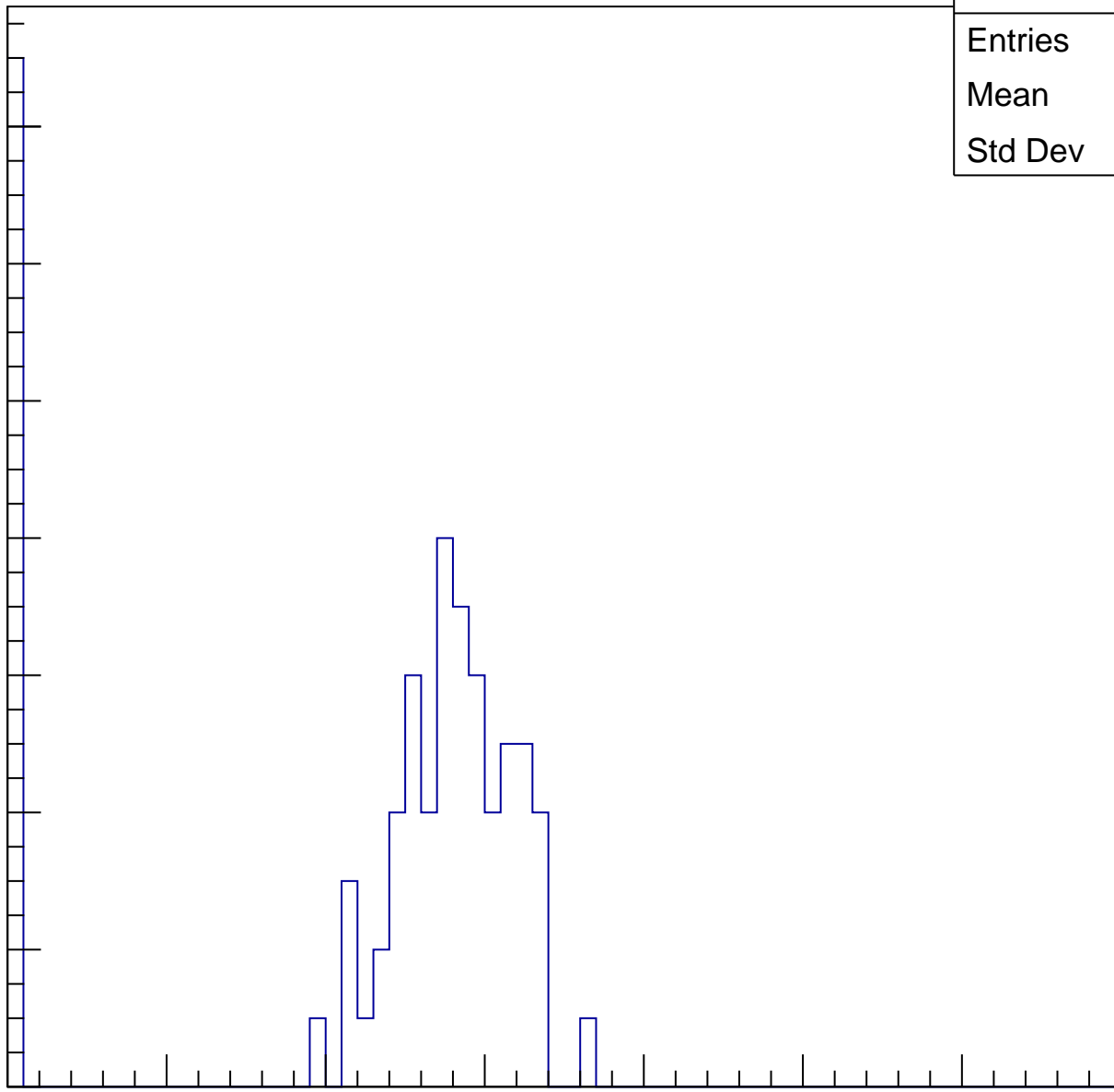
Entries	76
Mean	22.22
Std Dev	11.47

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

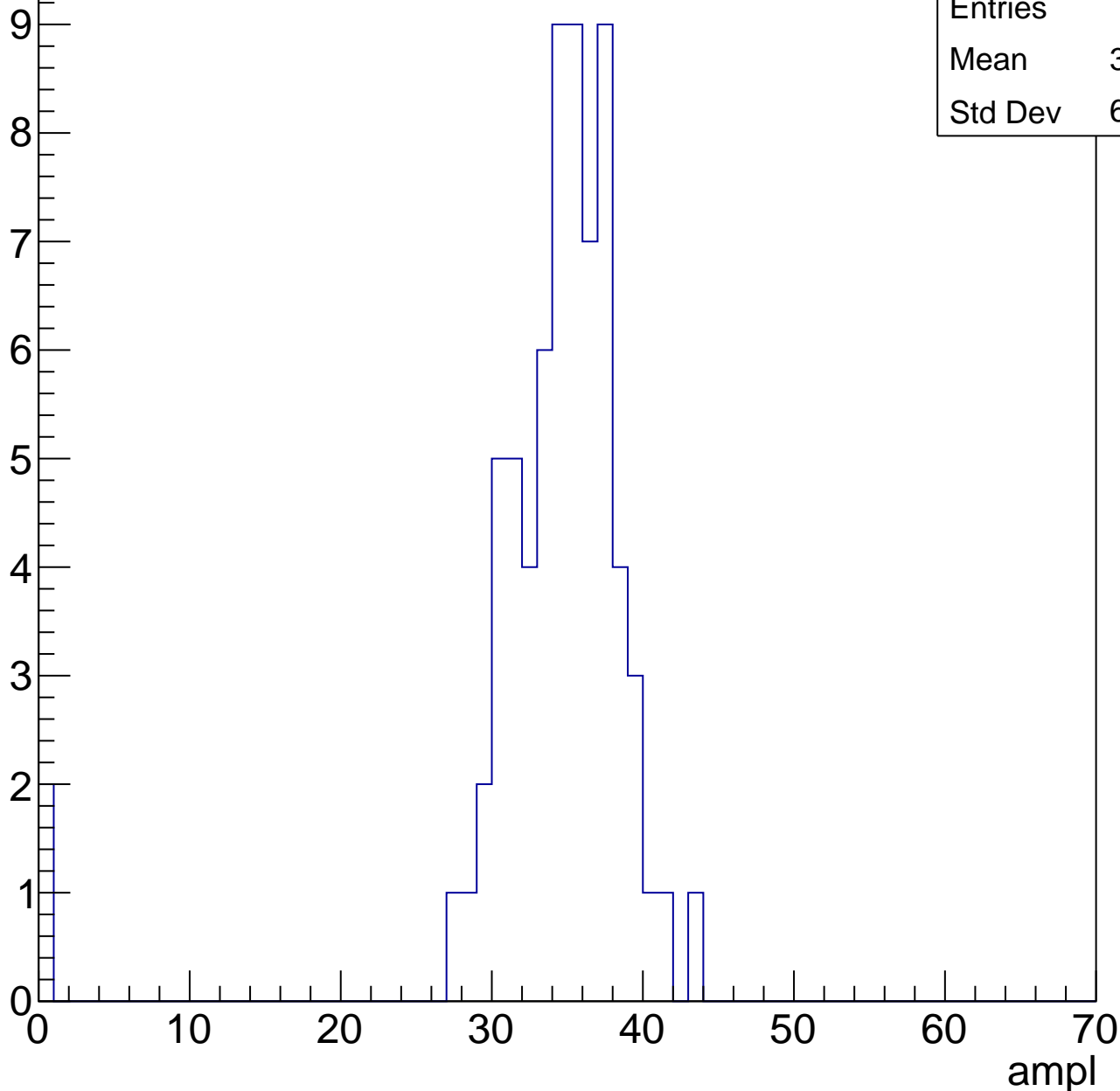


B1L103S, U11-ch76, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	33.47
Std Dev	6.544

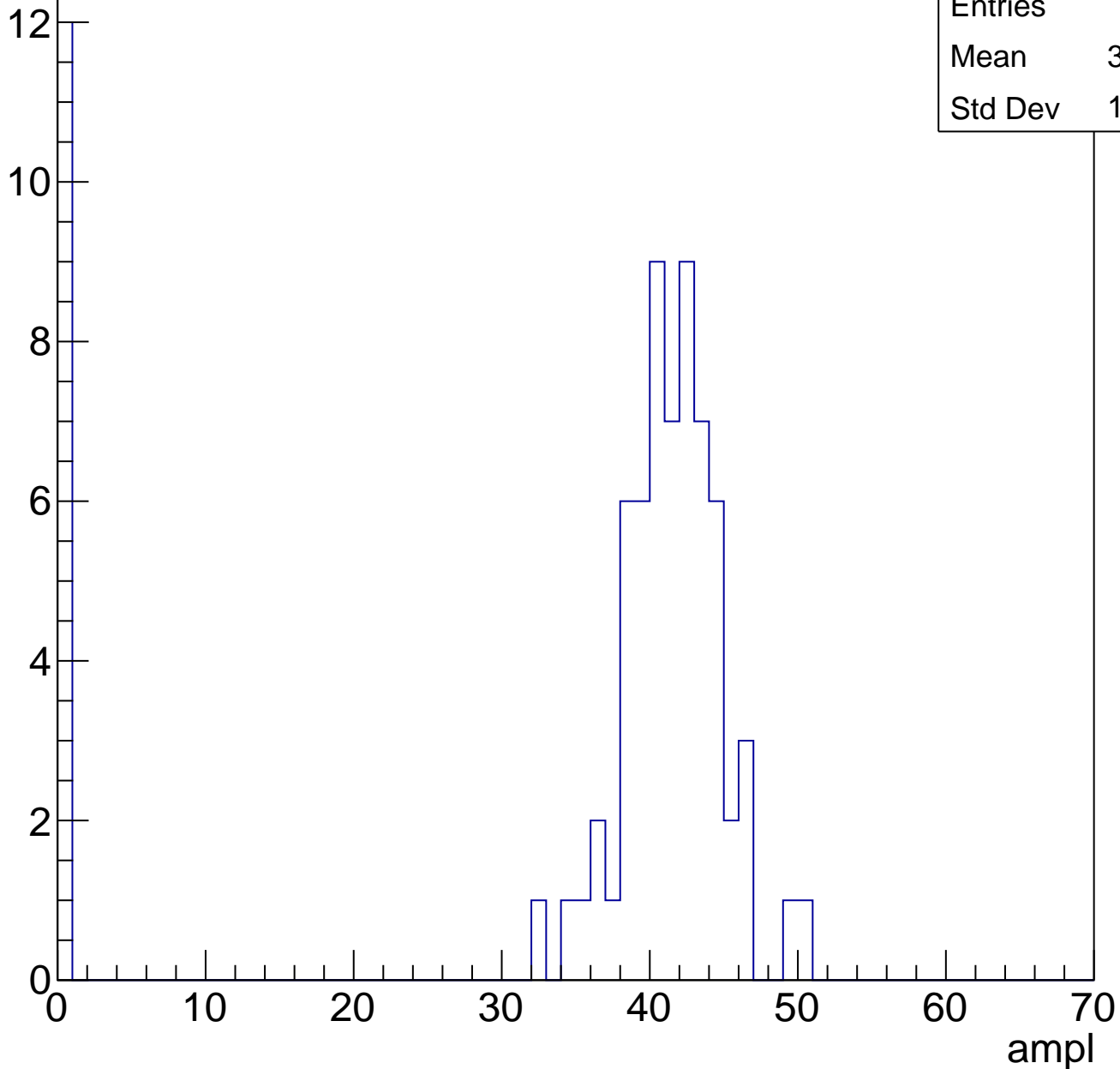


B1L103S, U11-ch76, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	34.52
Std Dev	15.36

Entry

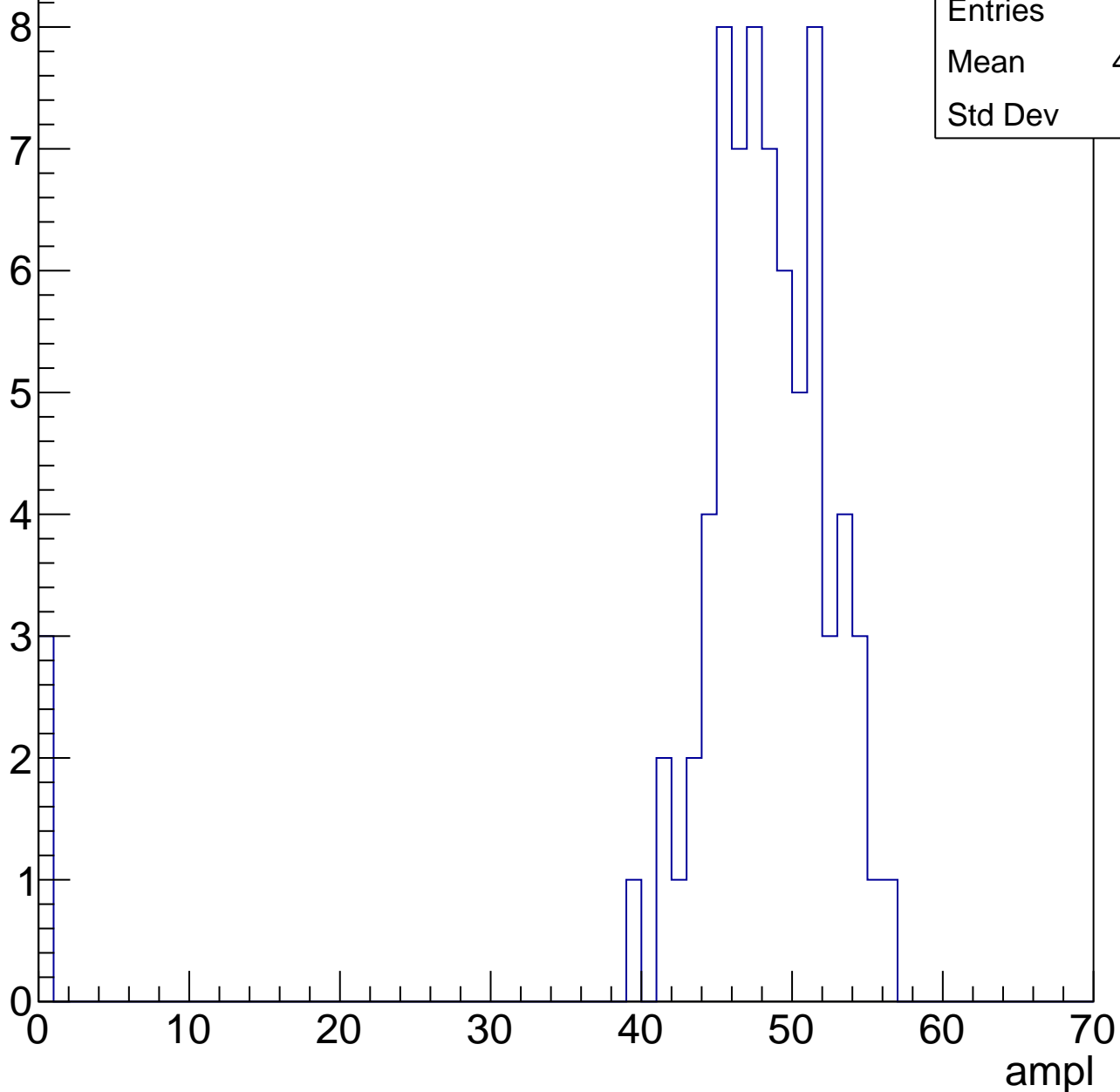


B1L103S, U11-ch76, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	46.11
Std Dev	10.1

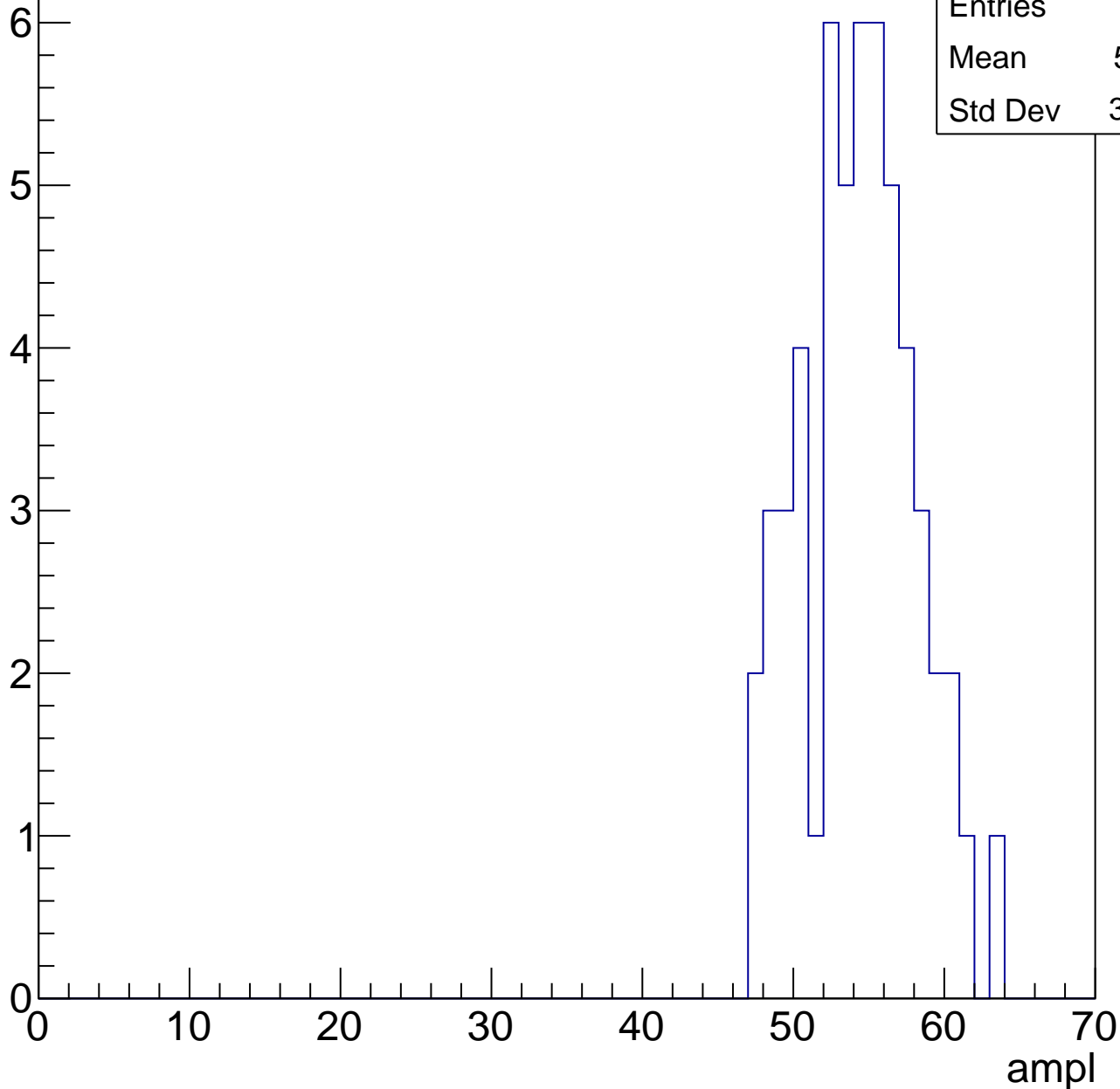


B1L103S, U11-ch76, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	53.91
Std Dev	3.713

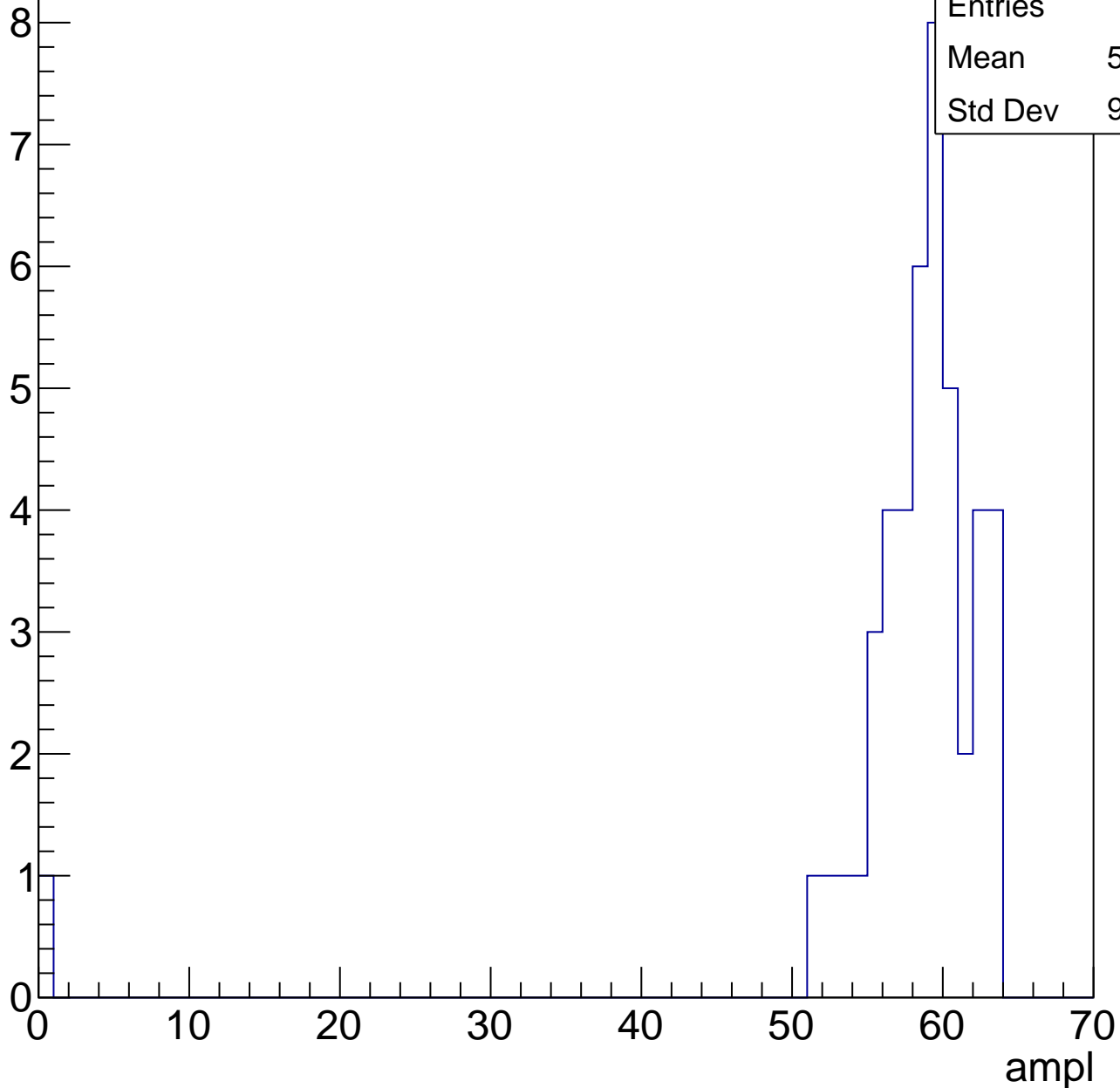


B1L103S, U11-ch76, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	45
Mean	57.09
Std Dev	9.079

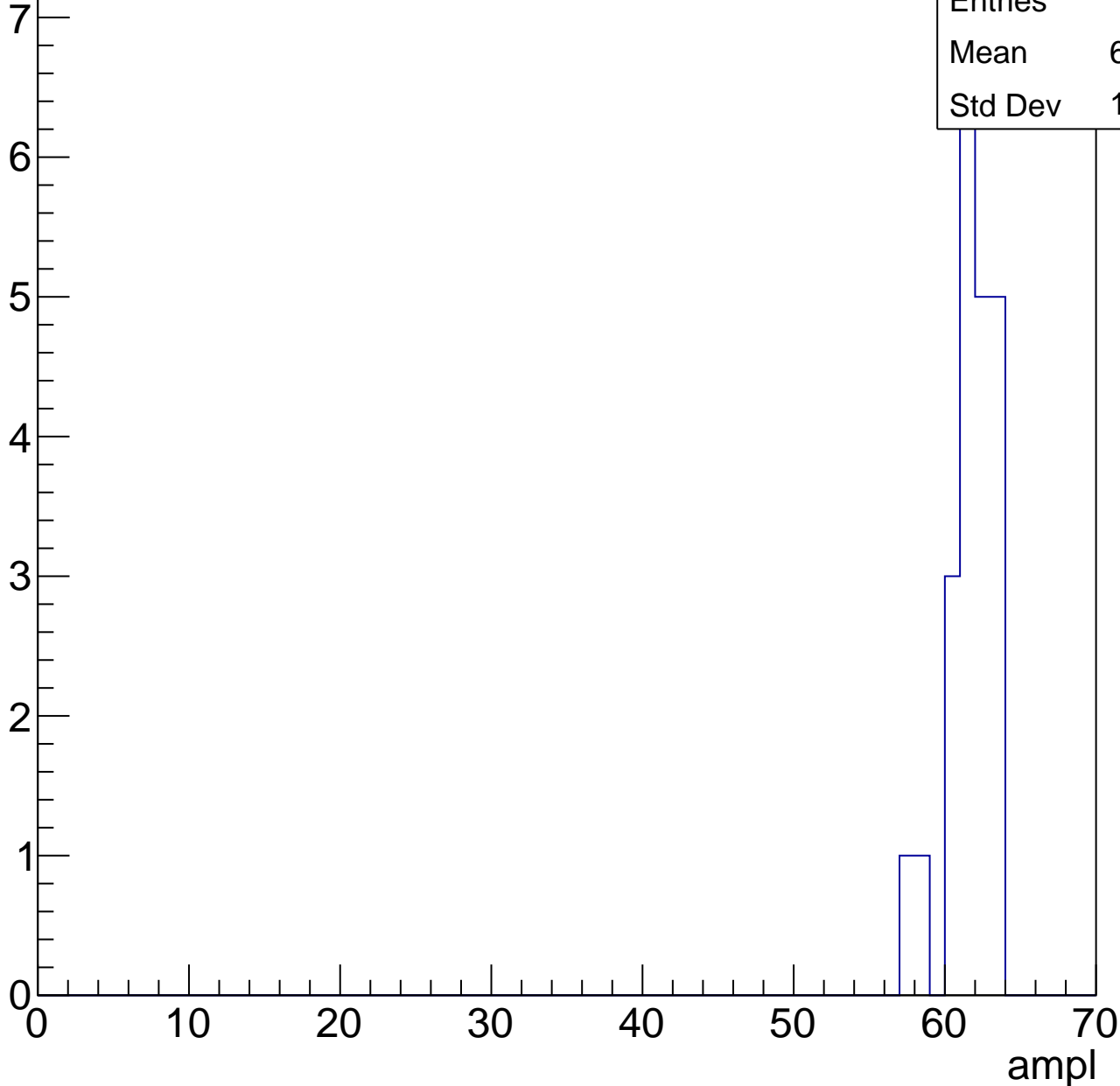


B1L103S, U11-ch76, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	22
Mean	61.23
Std Dev	1.535

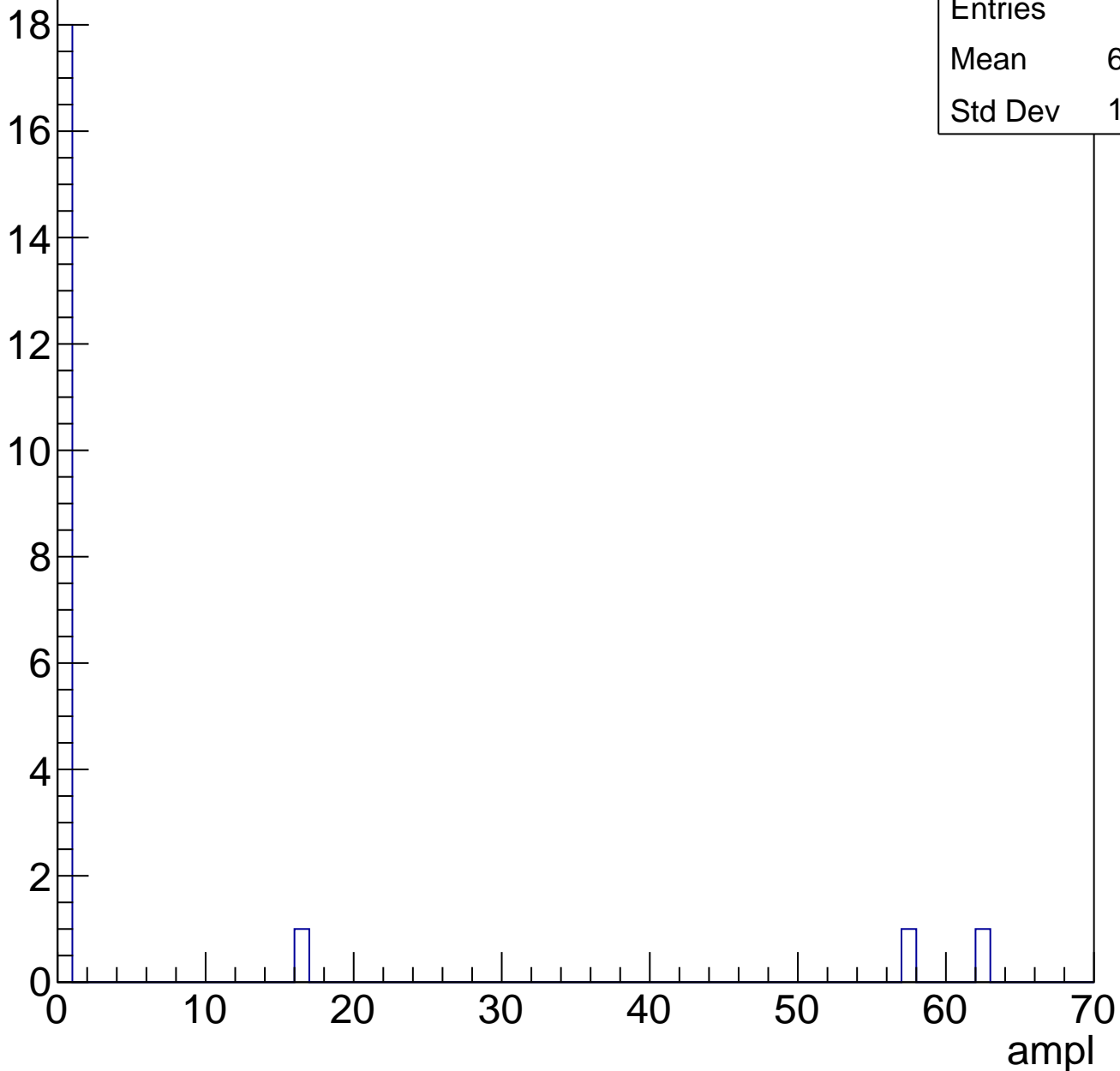


B1L103S, U11-ch76, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	6.429
Std Dev	17.57

Entry

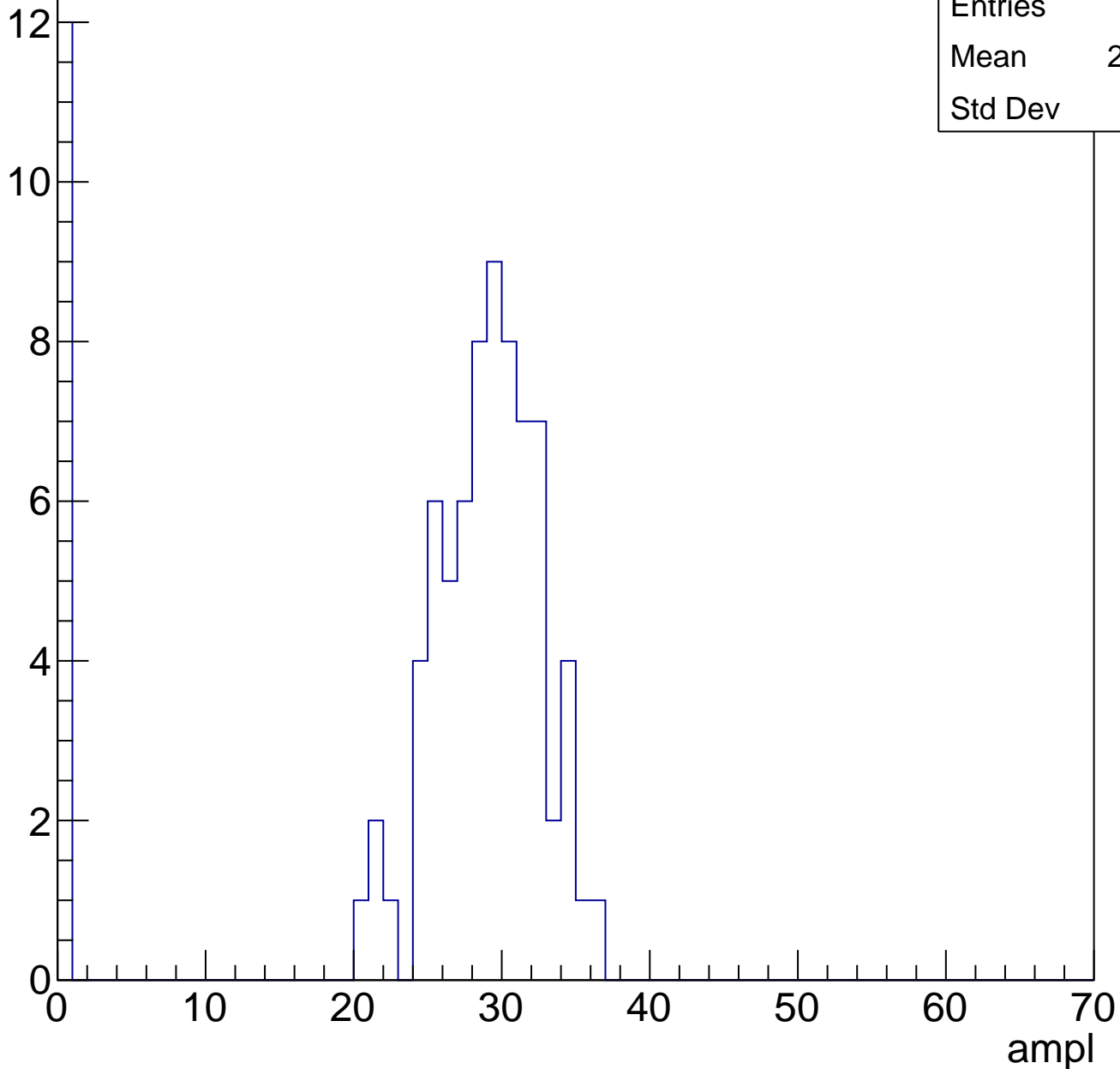


B1L103S, U11-ch77, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	84
Mean	24.54
Std Dev	10.5

Entry

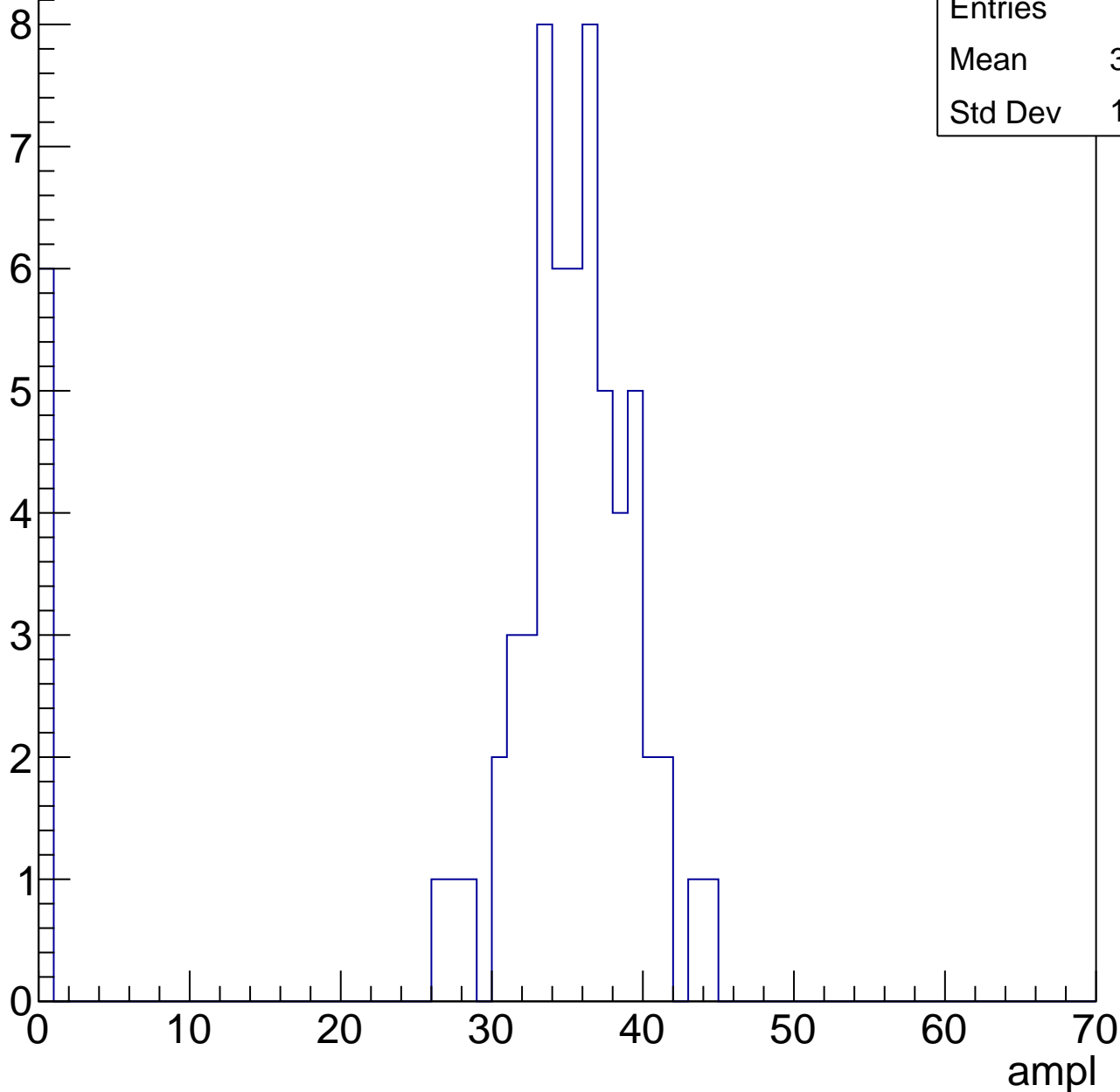


B1L103S, U11-ch77, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	31.95
Std Dev	10.75

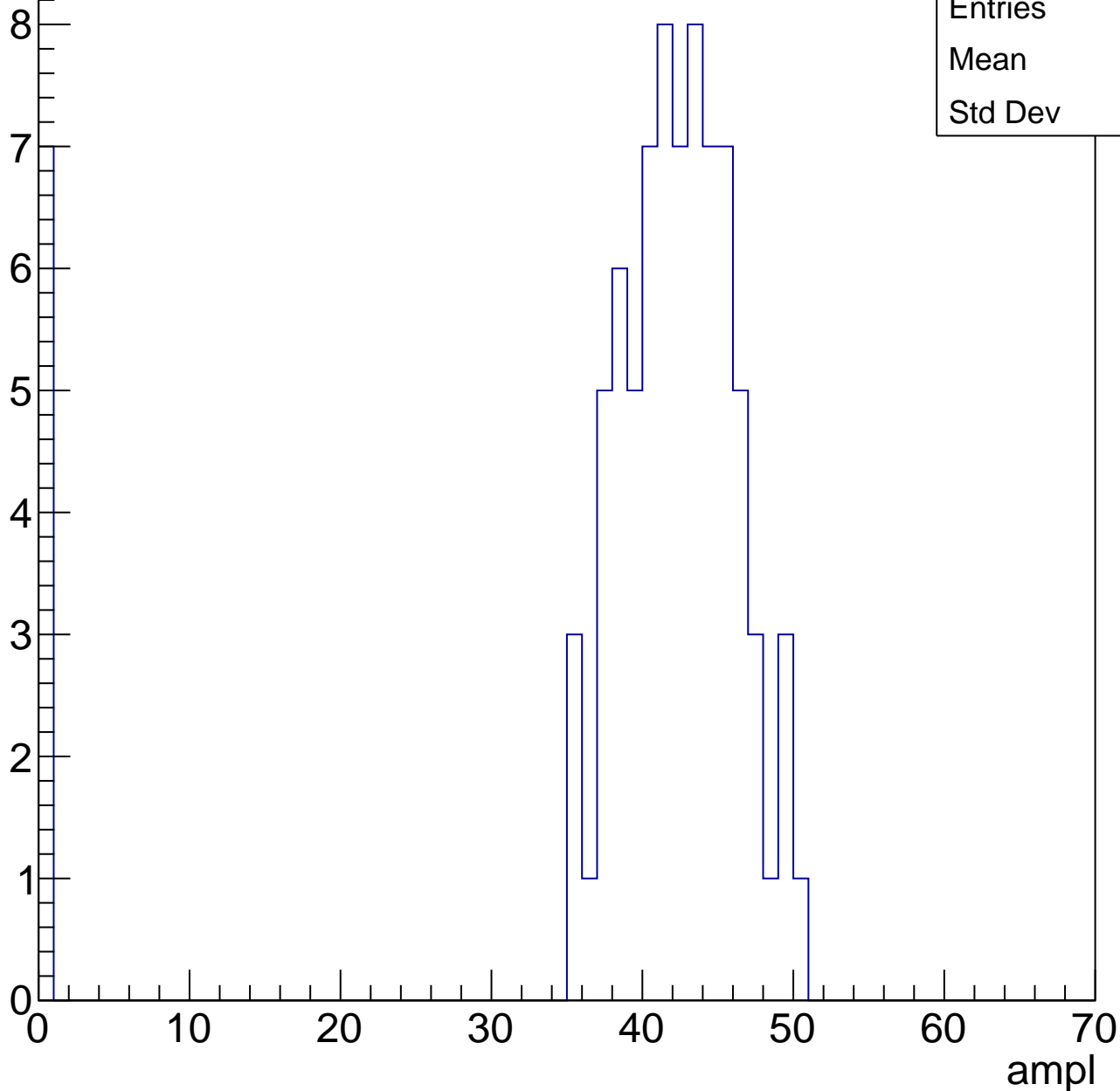


B1L103S, U11-ch77, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	84
Mean	38.5
Std Dev	12.1

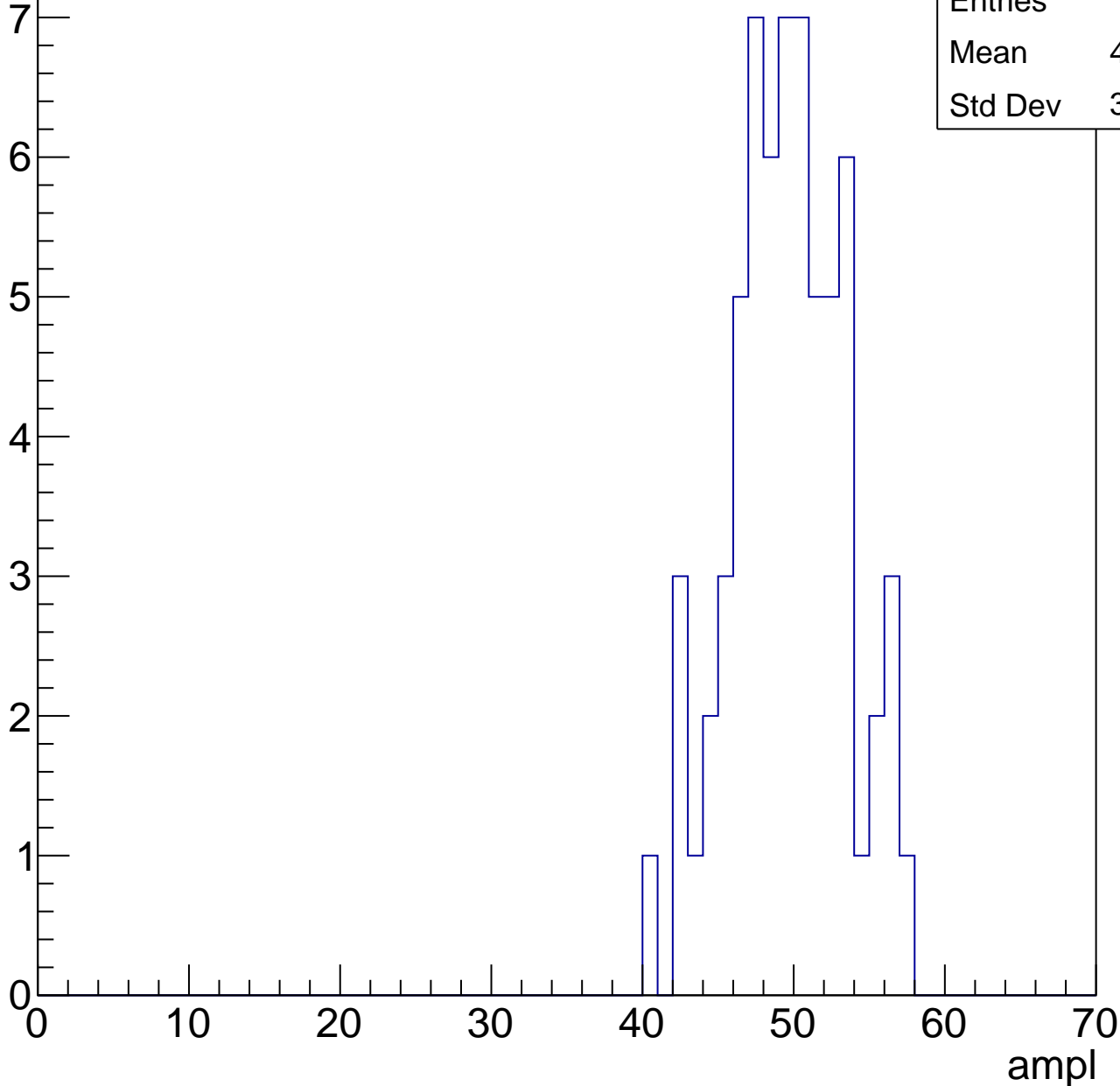


B1L103S, U11-ch77, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	49.14
Std Dev	3.753

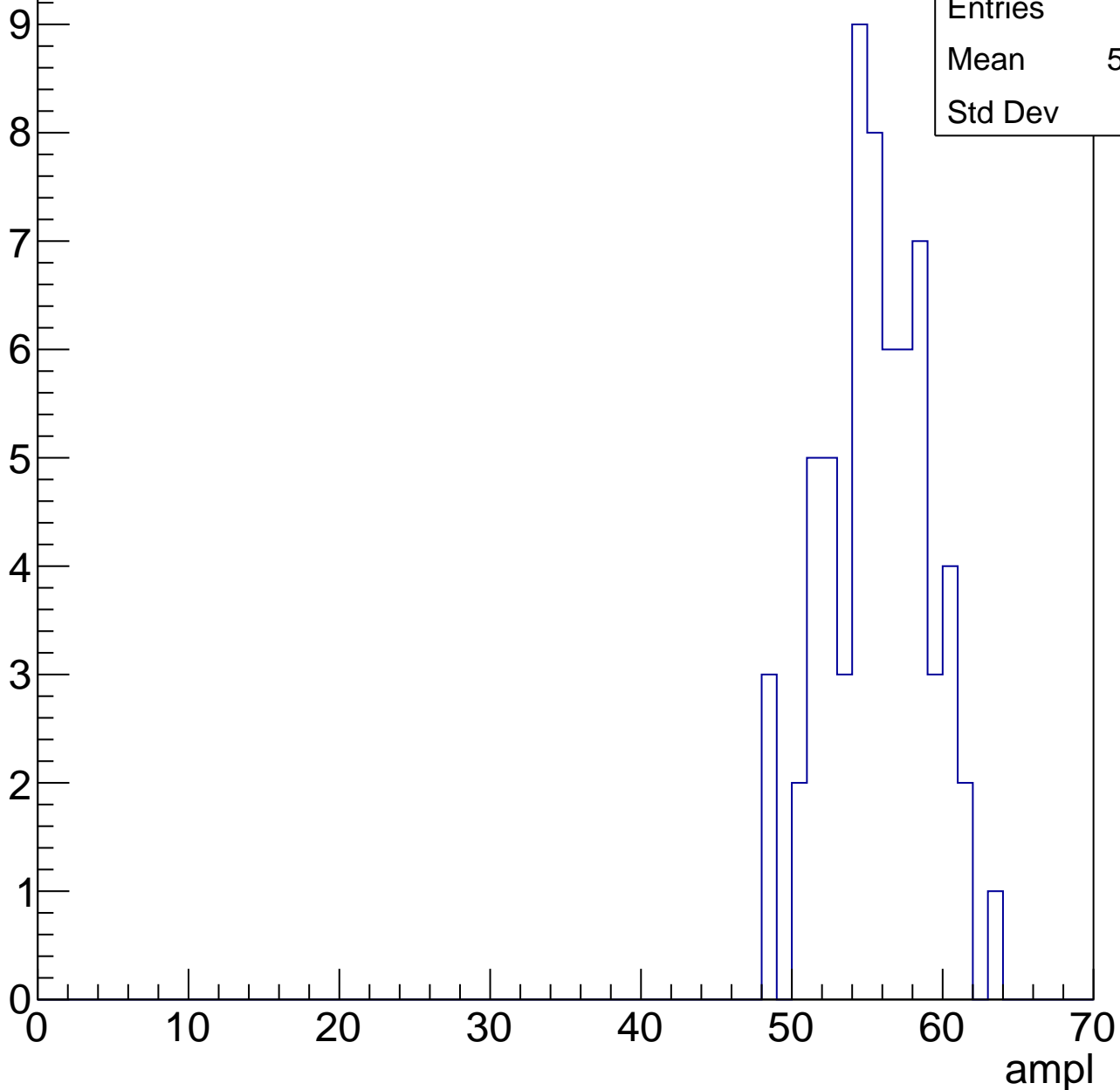


B1L103S, U11-ch77, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	55.16
Std Dev	3.35

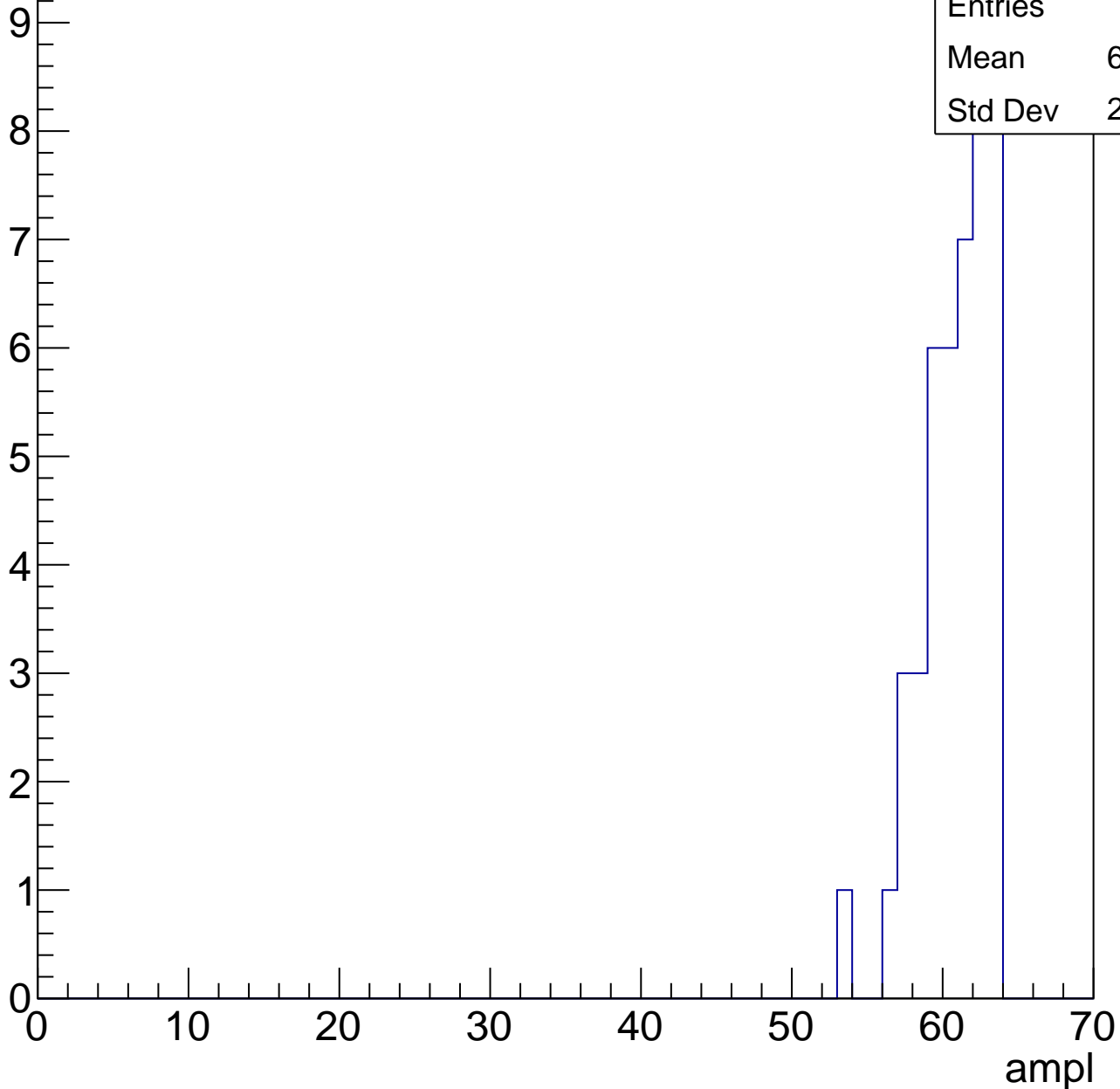


B1L103S, U11-ch77, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

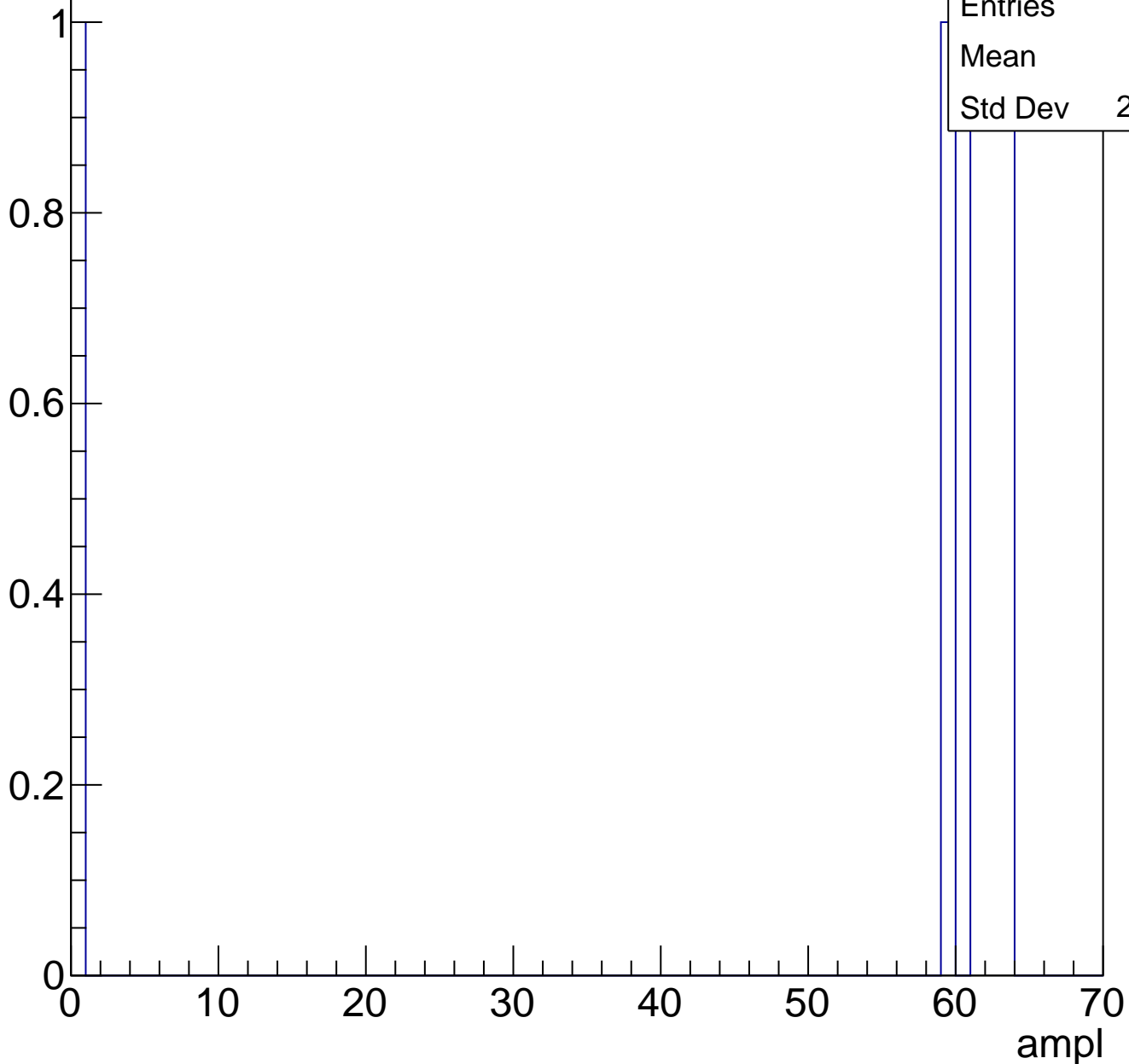
Entries	44
Mean	60.39
Std Dev	2.228



B1L103S, U11-ch77, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch77, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

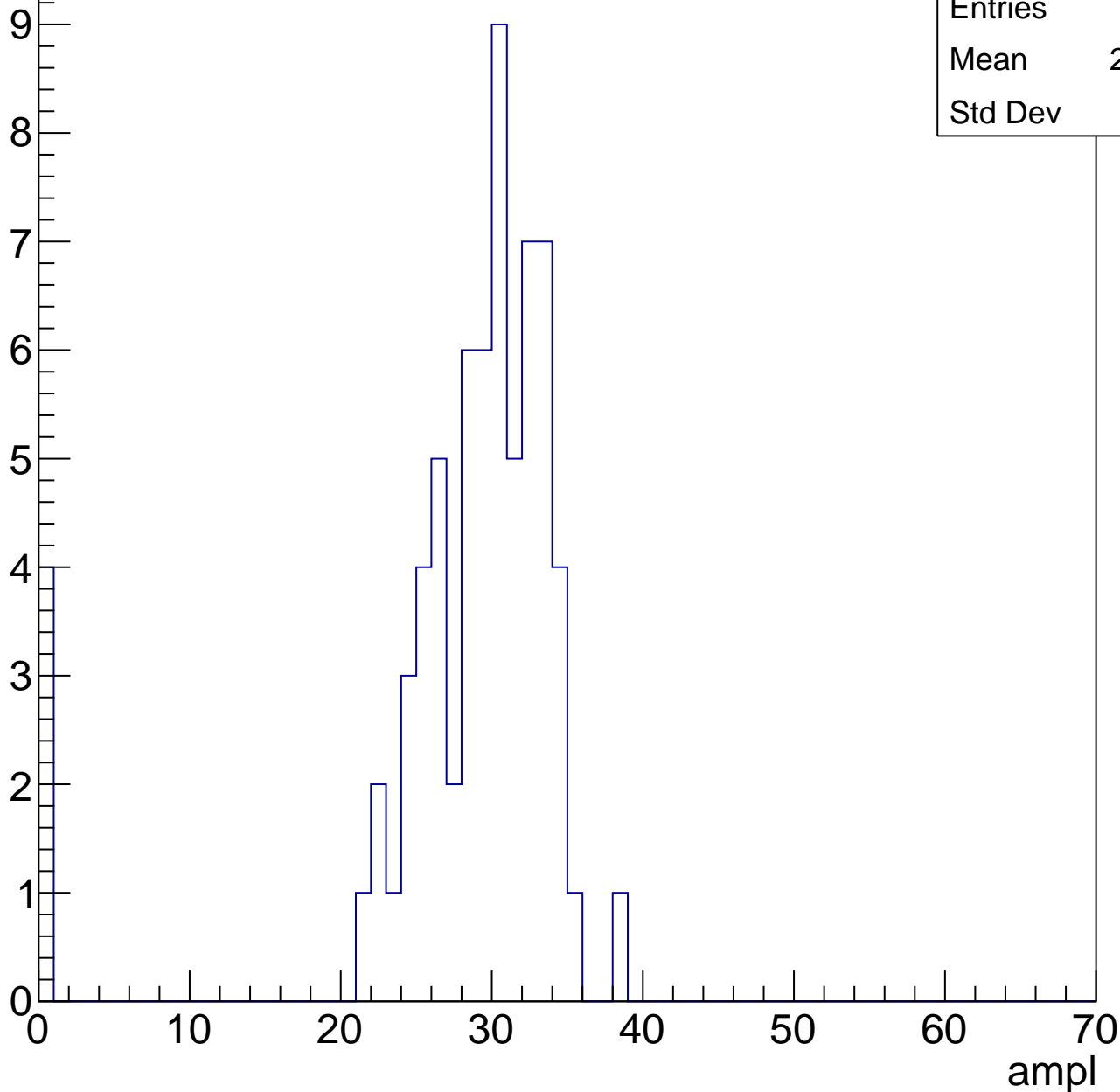
ampl

B1L103S, U11-ch78, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	27.57
Std Dev	7.71



B1L103S, U11-ch78, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

12

10

8

6

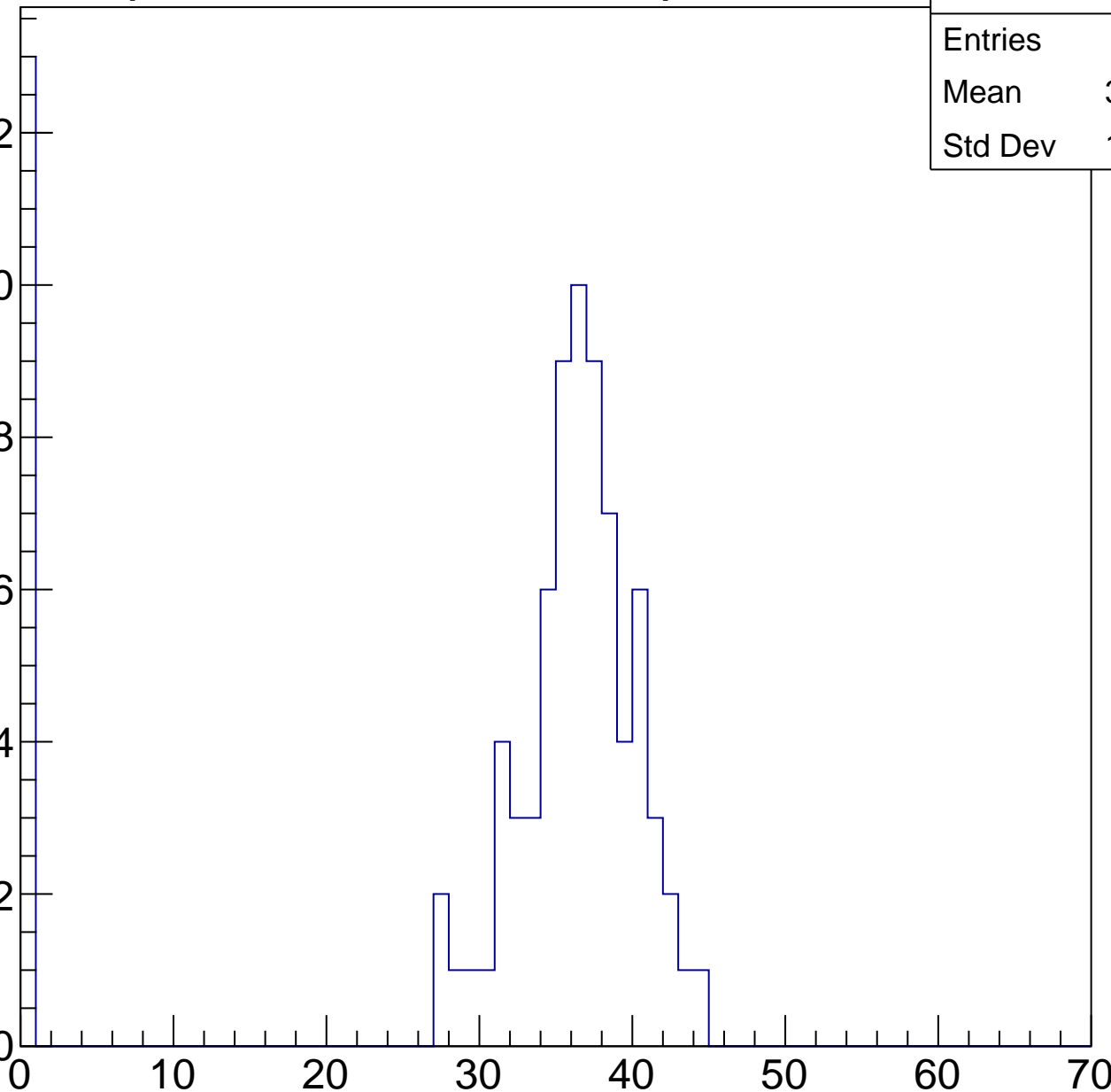
4

2

0

Entries	86
Mean	30.56
Std Dev	13.32

ampl

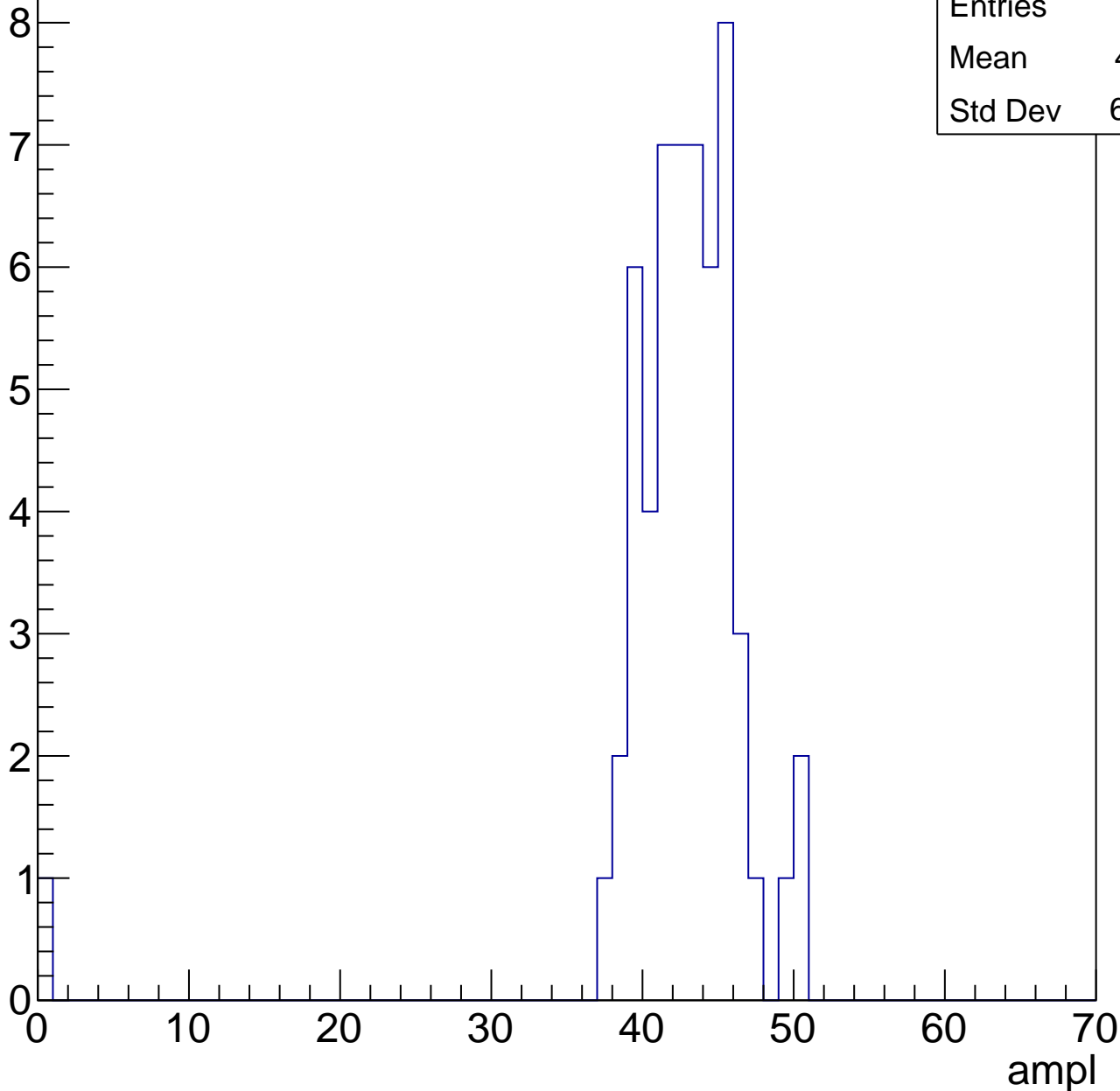


B1L103S, U11-ch78, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	41.91
Std Dev	6.339



B1L103S, U11-ch78, adc3

calib_packv5_041523_1651.root, FC#0, port C2

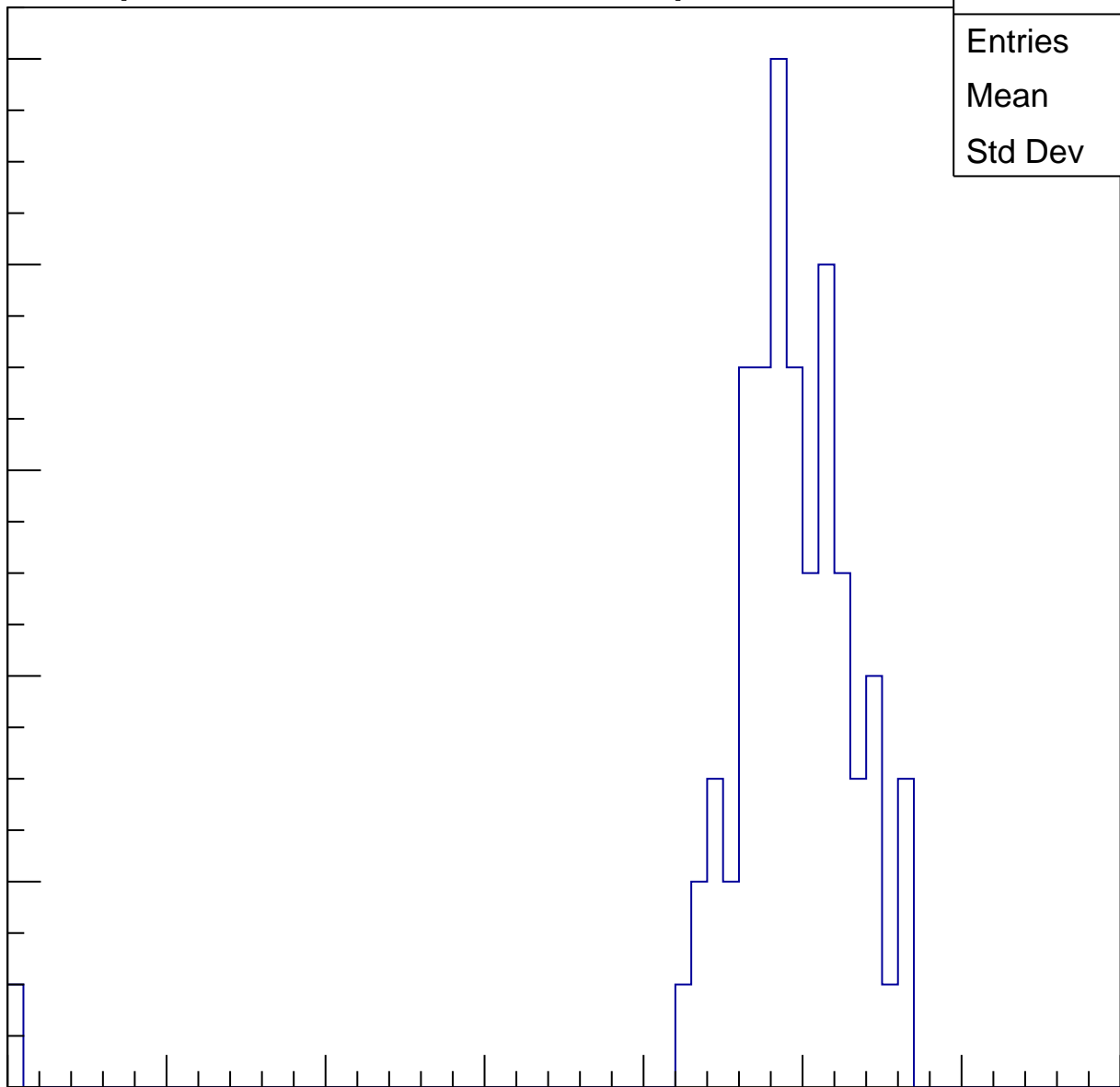
Entries	69
Mean	48.41
Std Dev	6.723

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

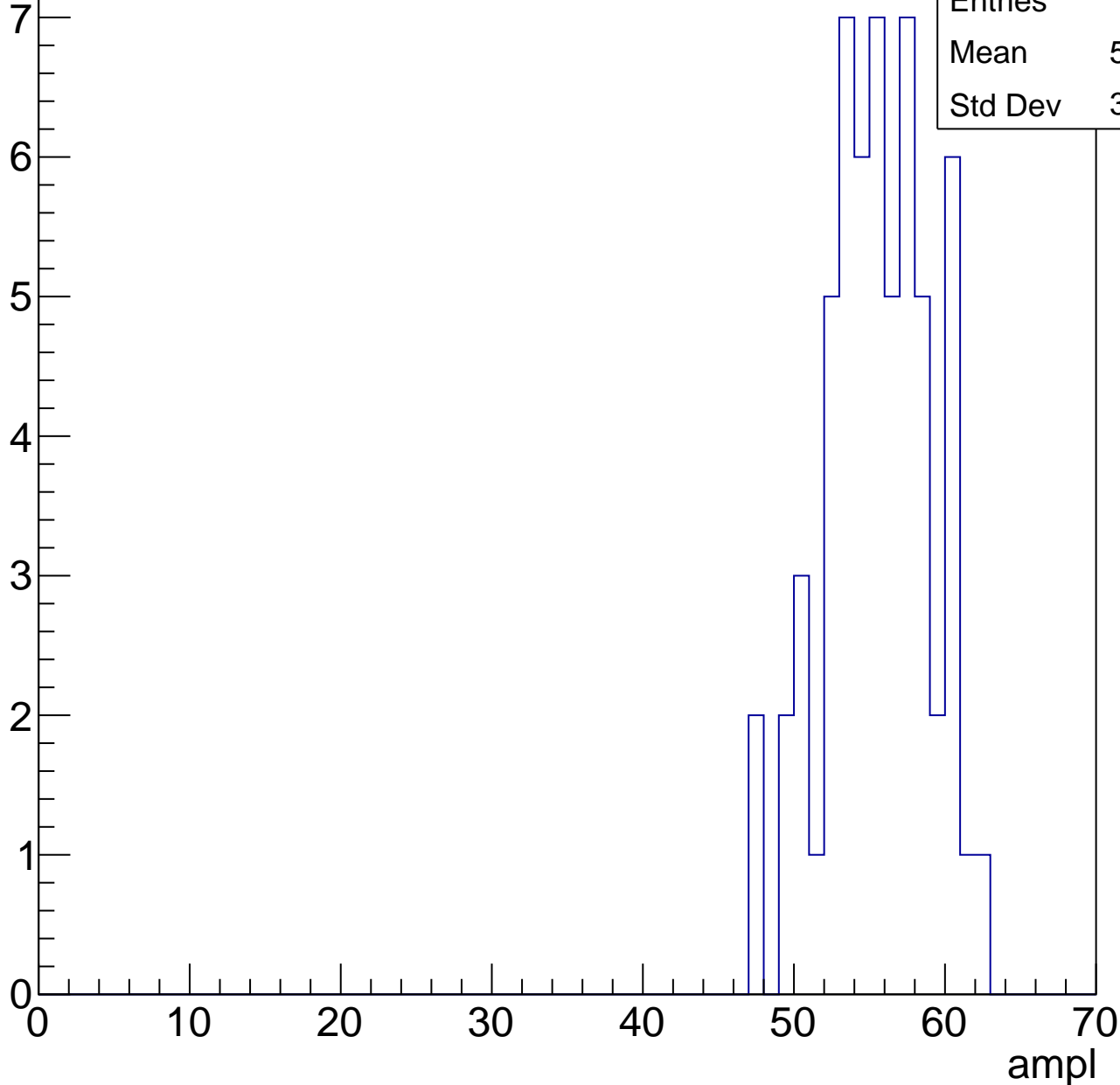
ampl



B1L103S, U11-ch78, adc4

calib_packv5_041523_1651.root, FC#0, port C2

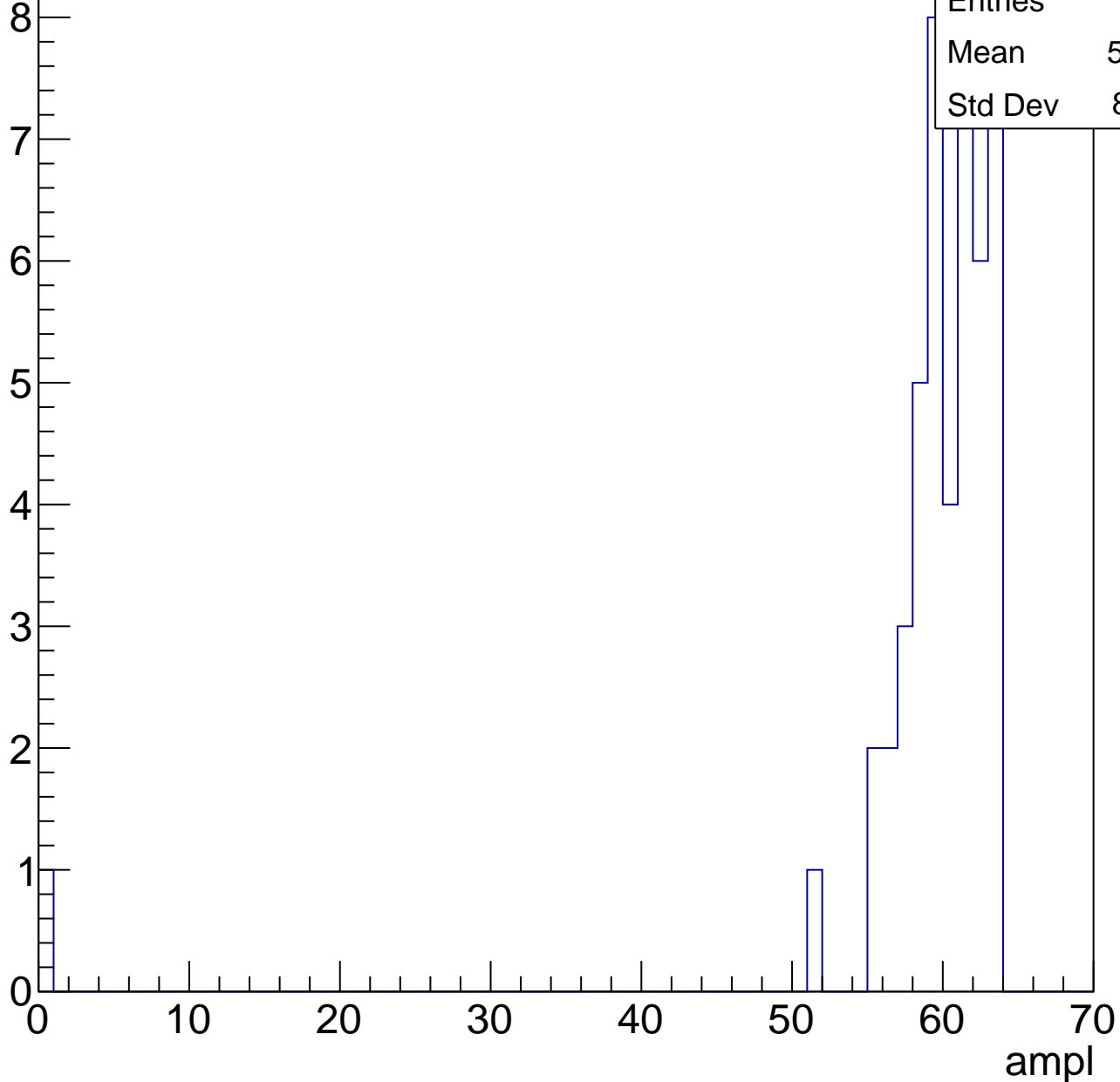
Entry



B1L103S, U11-ch78, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch78, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



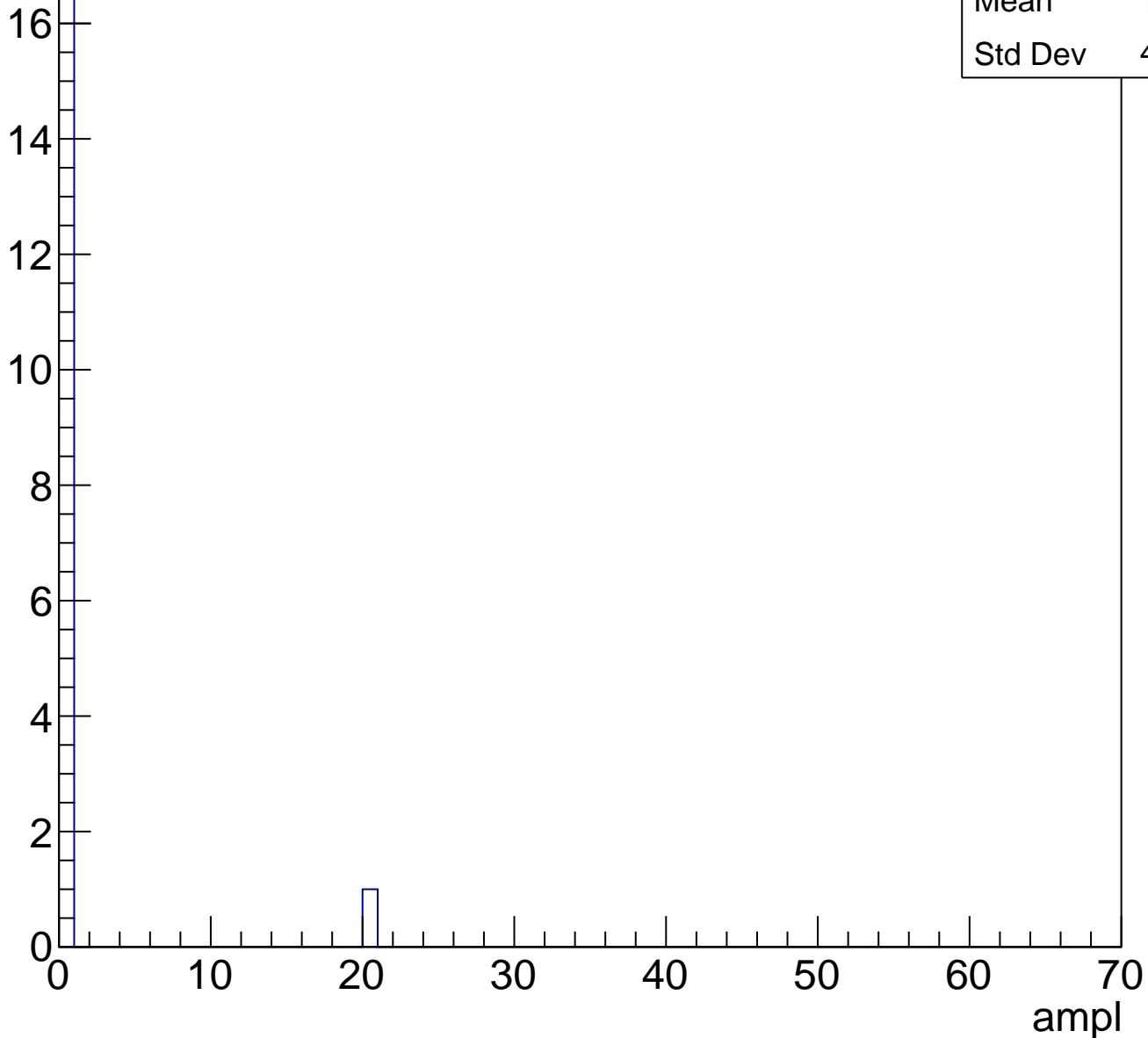
Entries	6
Mean	62.17
Std Dev	0.6872

B1L103S, U11-ch78, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	18
Mean	1.111
Std Dev	4.581

Entry

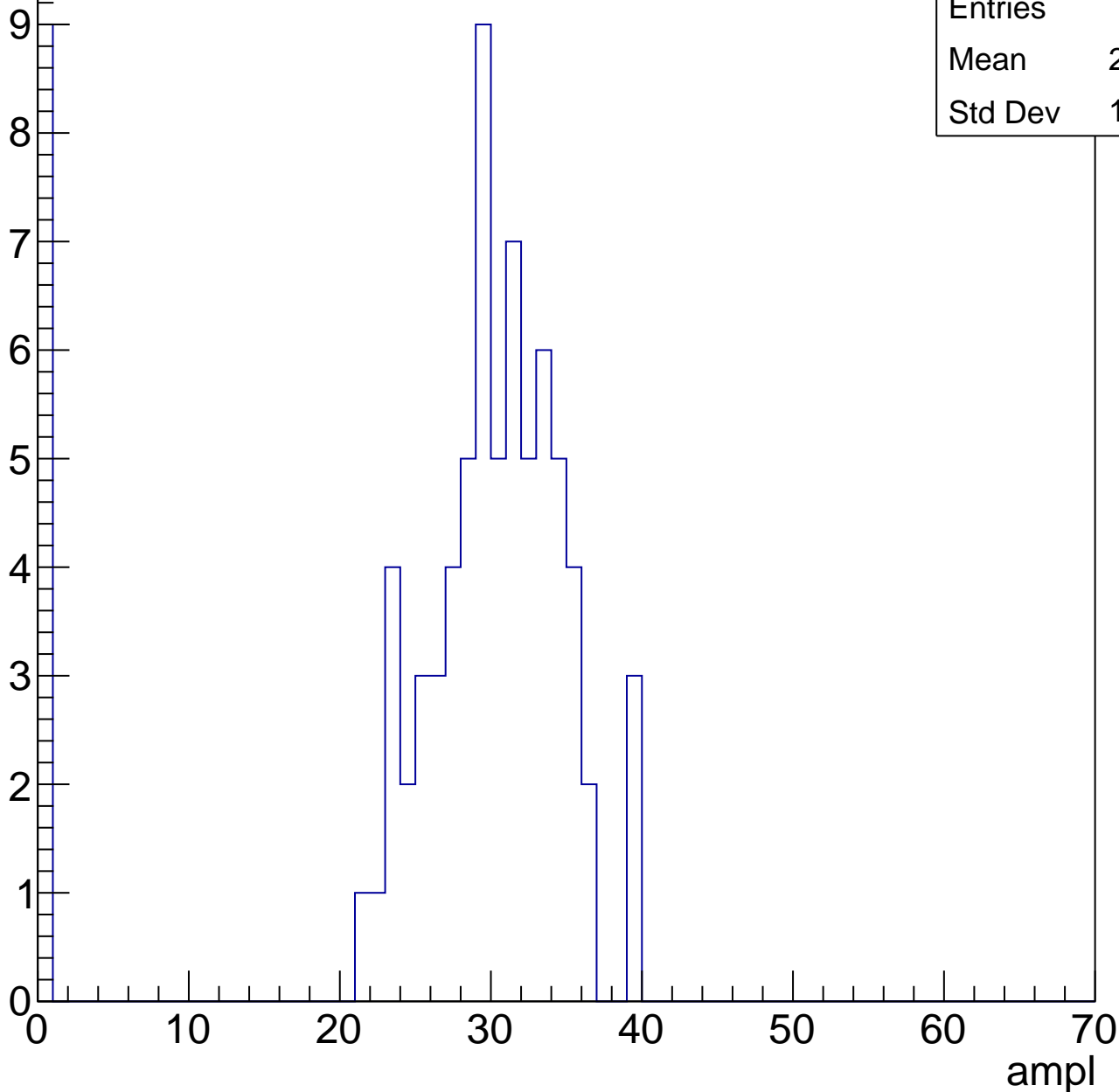


B1L103S, U11-ch79, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	26.53
Std Dev	10.34

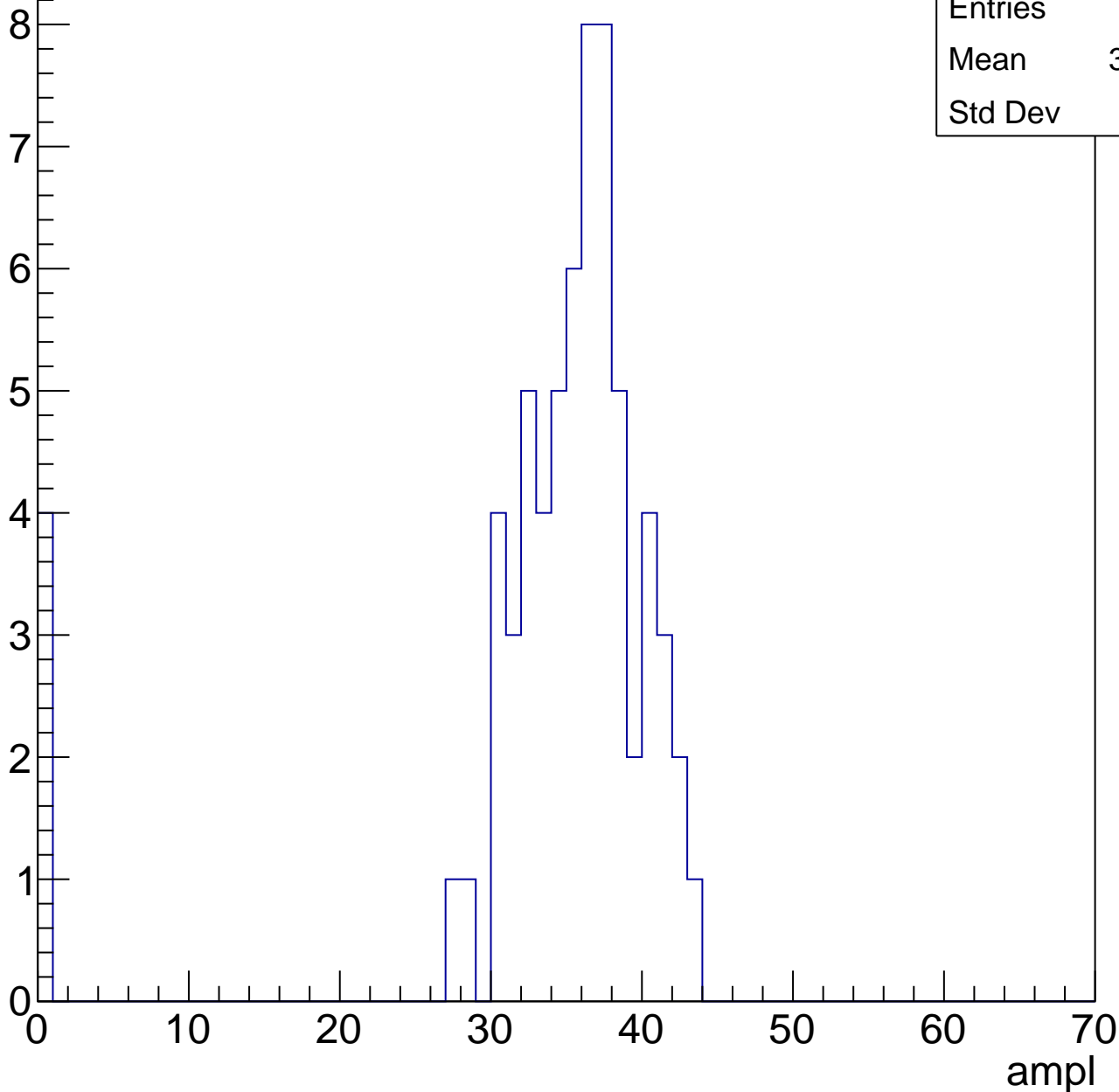


B1L103S, U11-ch79, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

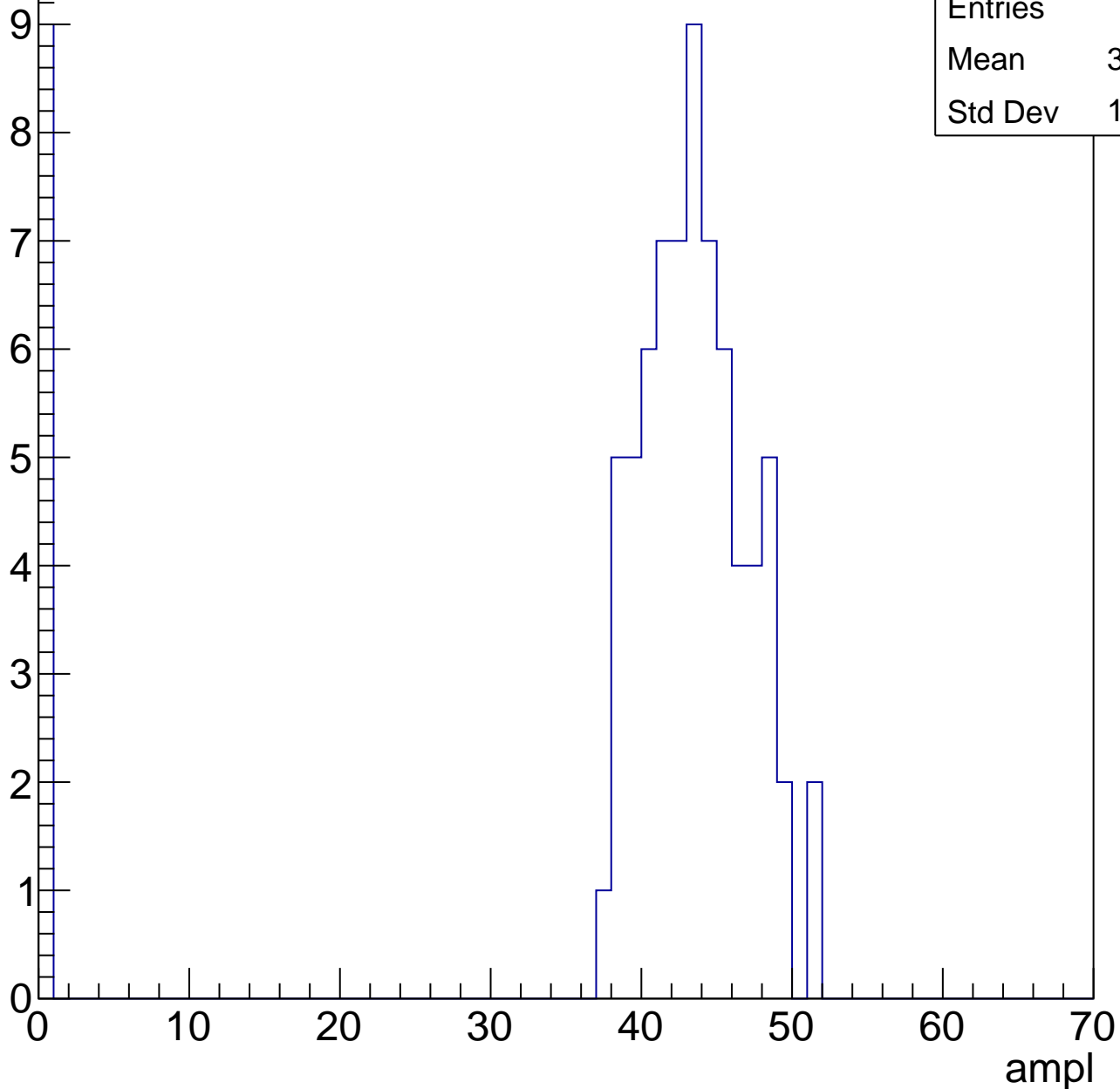
Entries	66
Mean	33.36
Std Dev	9.16



B1L103S, U11-ch79, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

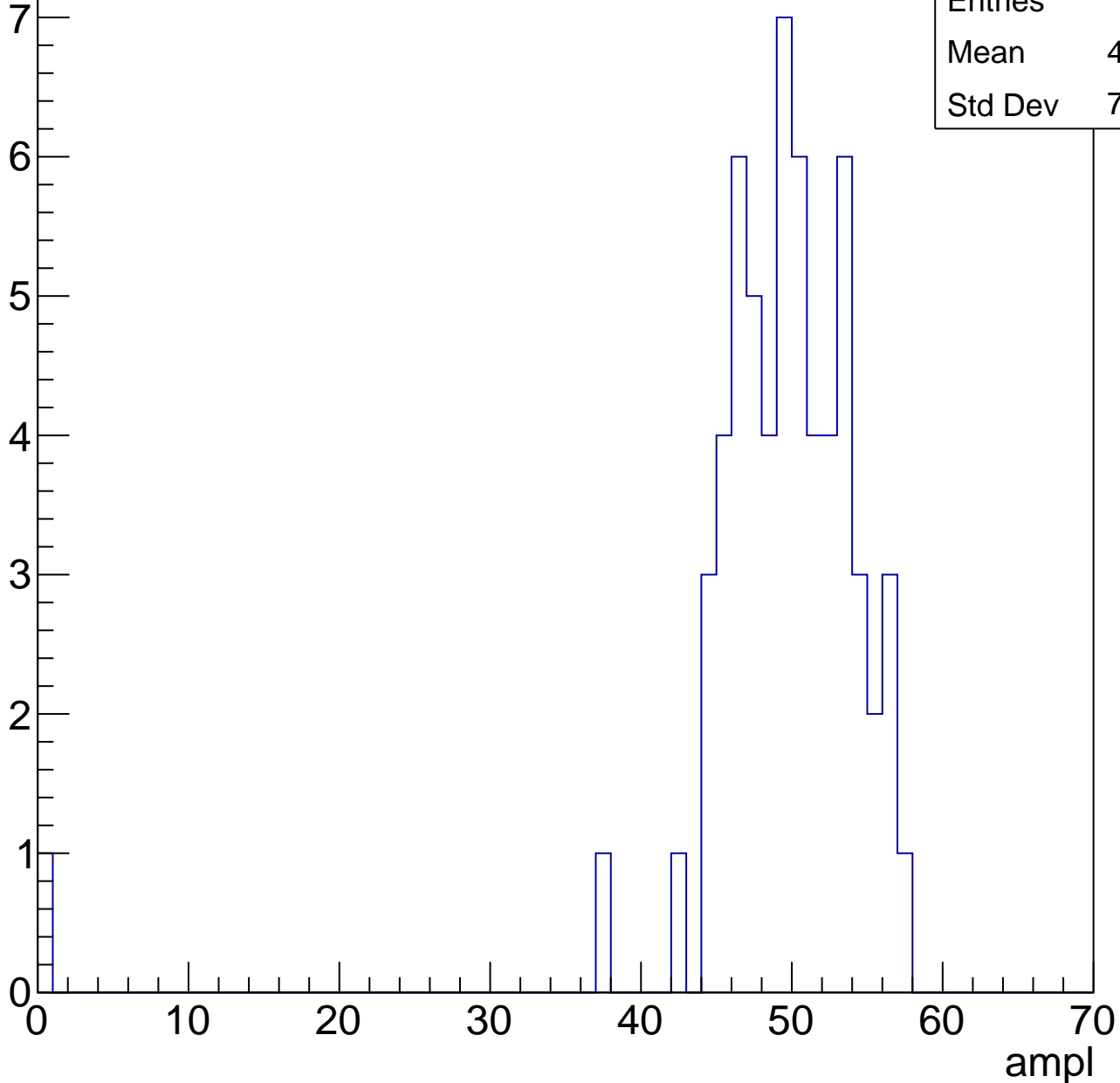


B1L103S, U11-ch79, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	48.59
Std Dev	7.369

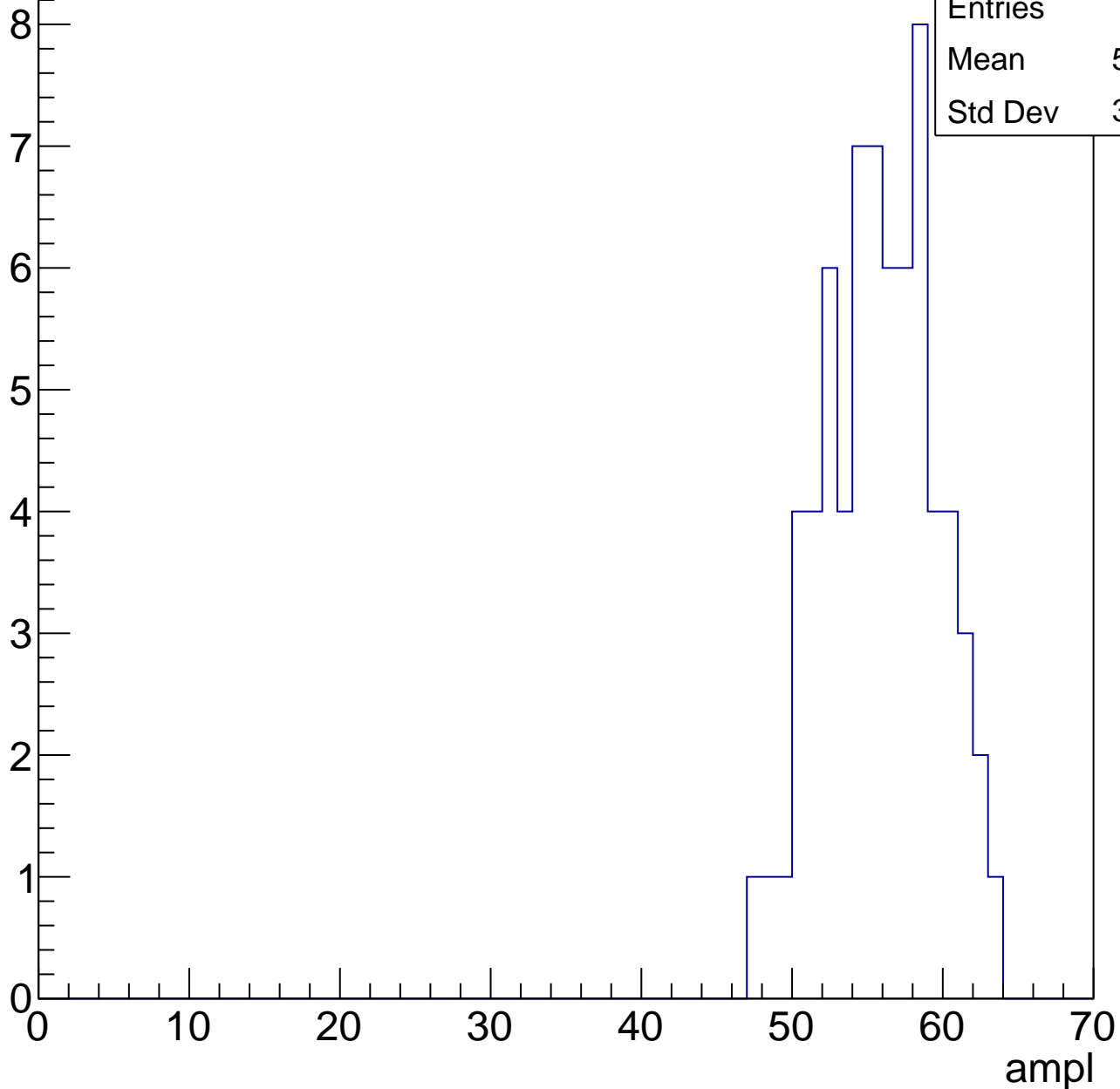


B1L103S, U11-ch79, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	55.41
Std Dev	3.641

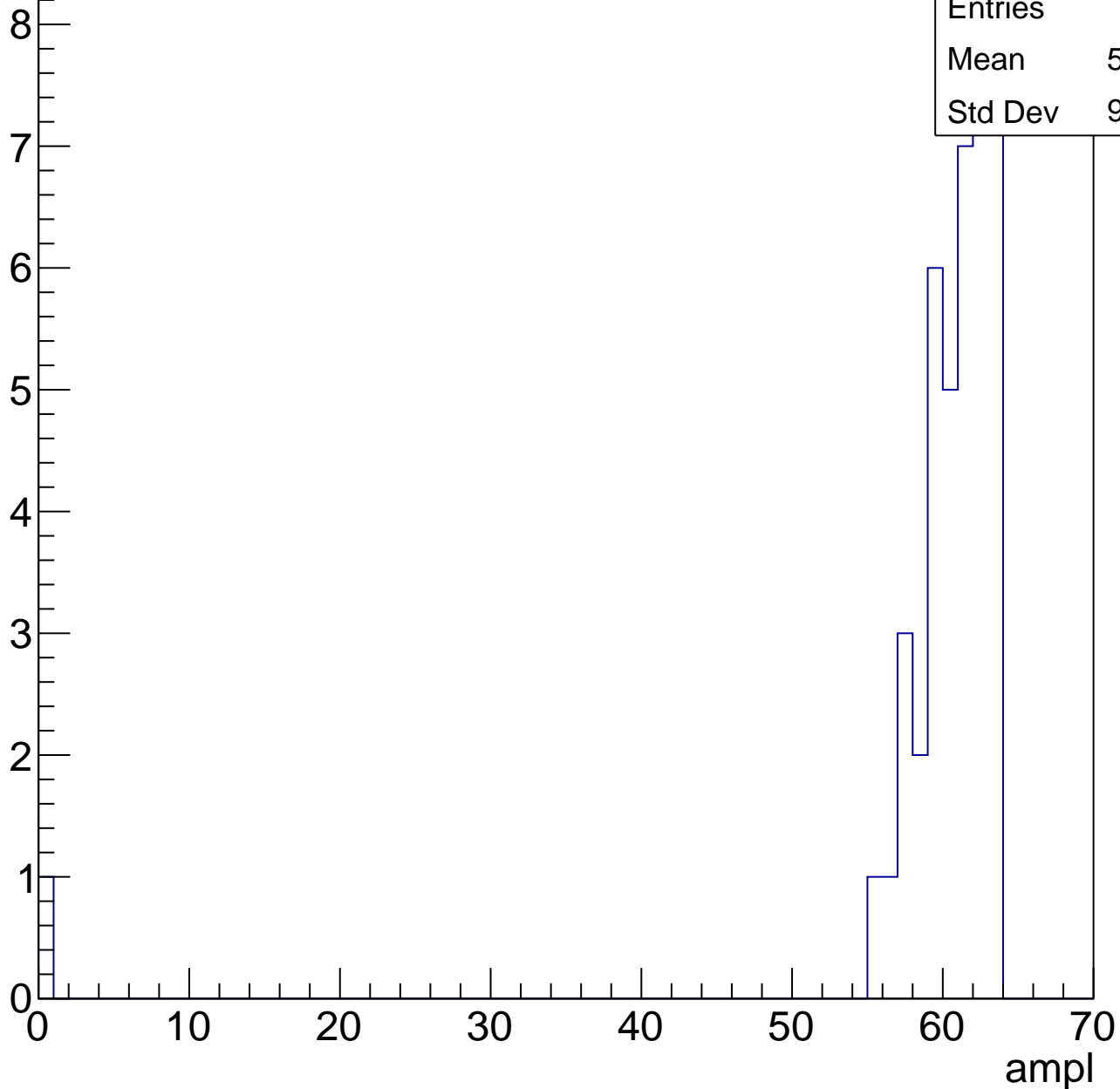


B1L103S, U11-ch79, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	42
Mean	59.02
Std Dev	9.453



B1L103S, U11-ch79, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

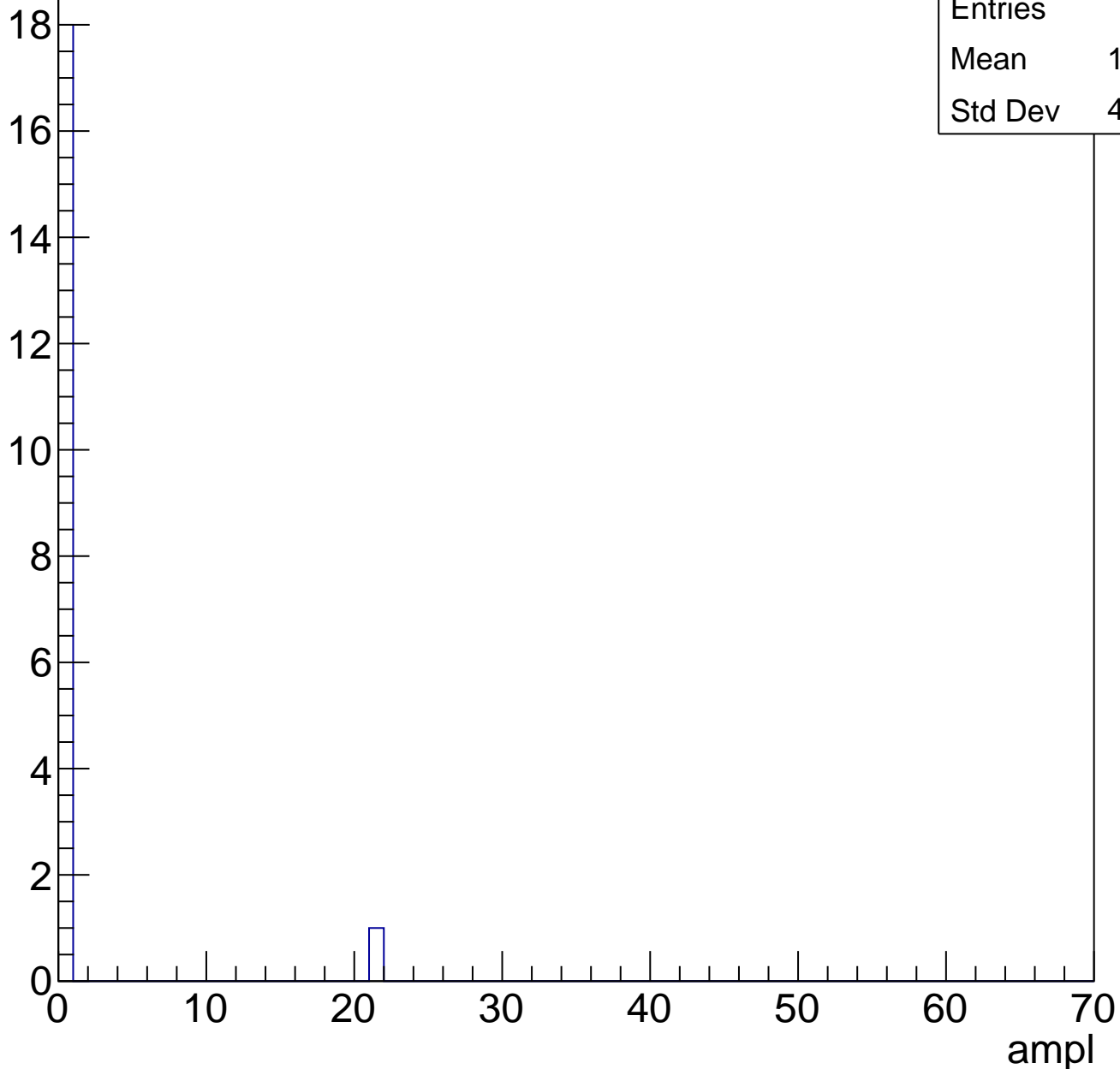


B1L103S, U11-ch79, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.105
Std Dev	4.689

Entry



B1L103S, U11-ch80, adc0

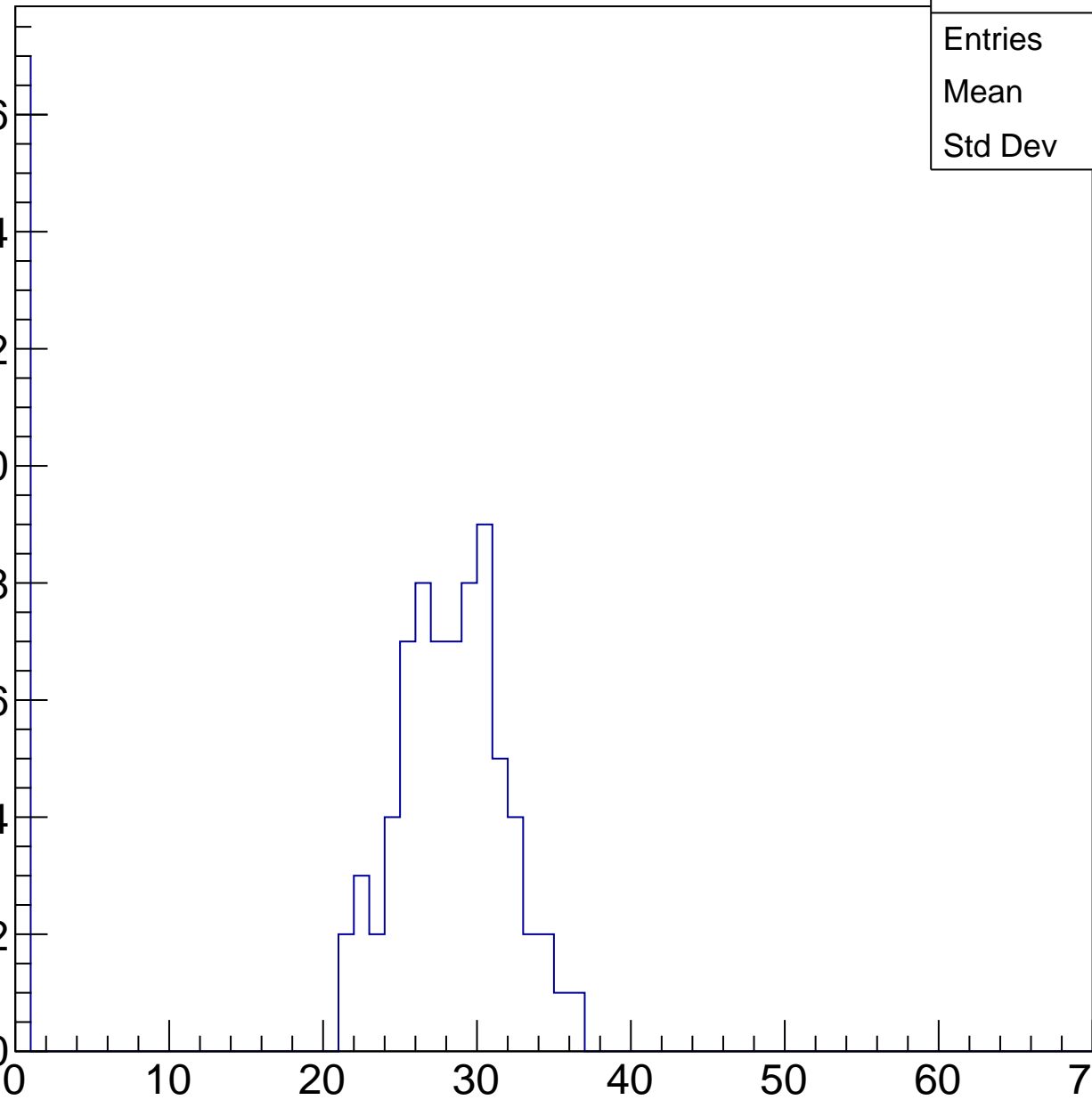
calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	22.56
Std Dev	11.37

Entry

16
14
12
10
8
6
4
2
0

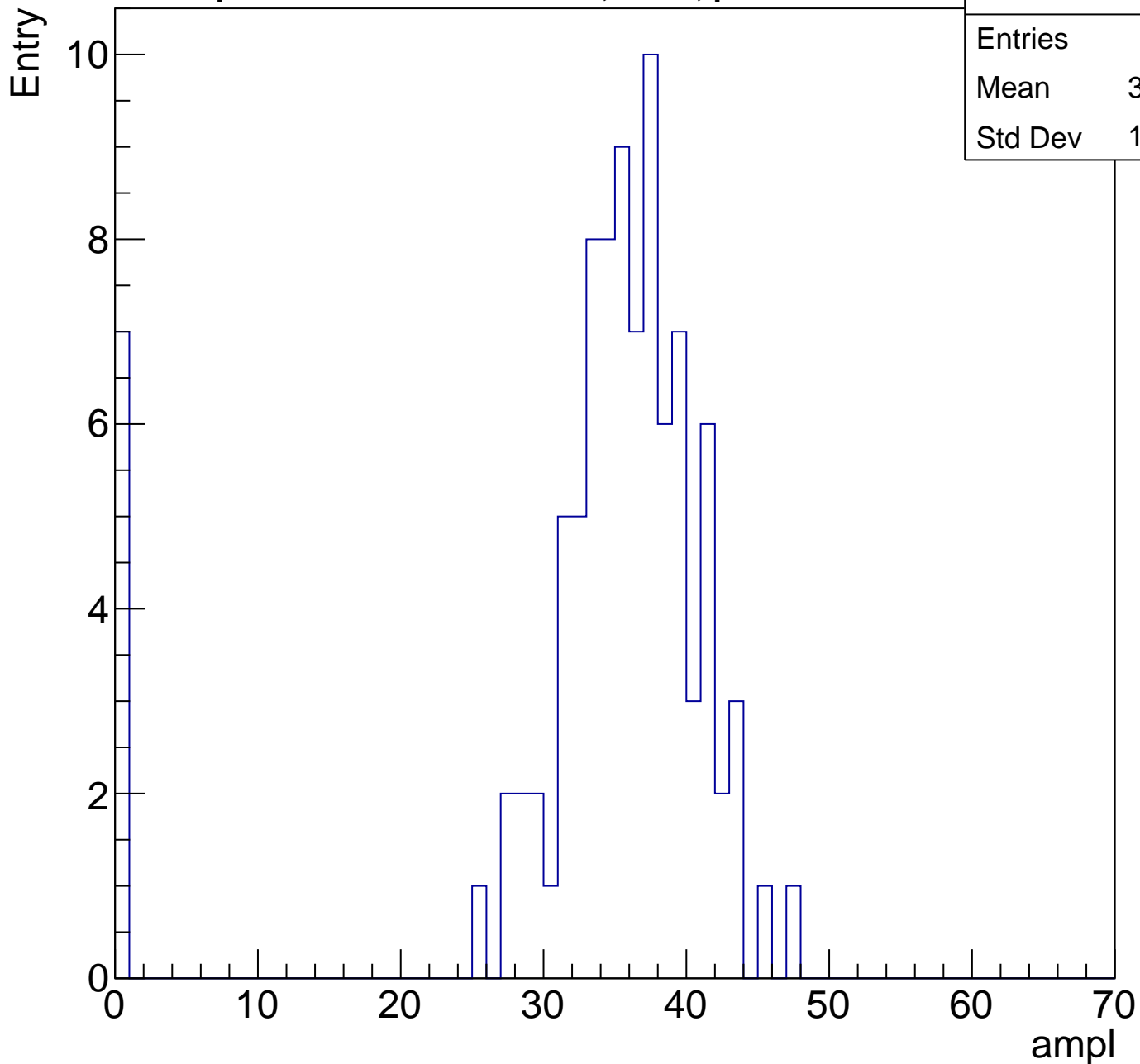
ampl



B1L103S, U11-ch80, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	96
Mean	33.16
Std Dev	10.14

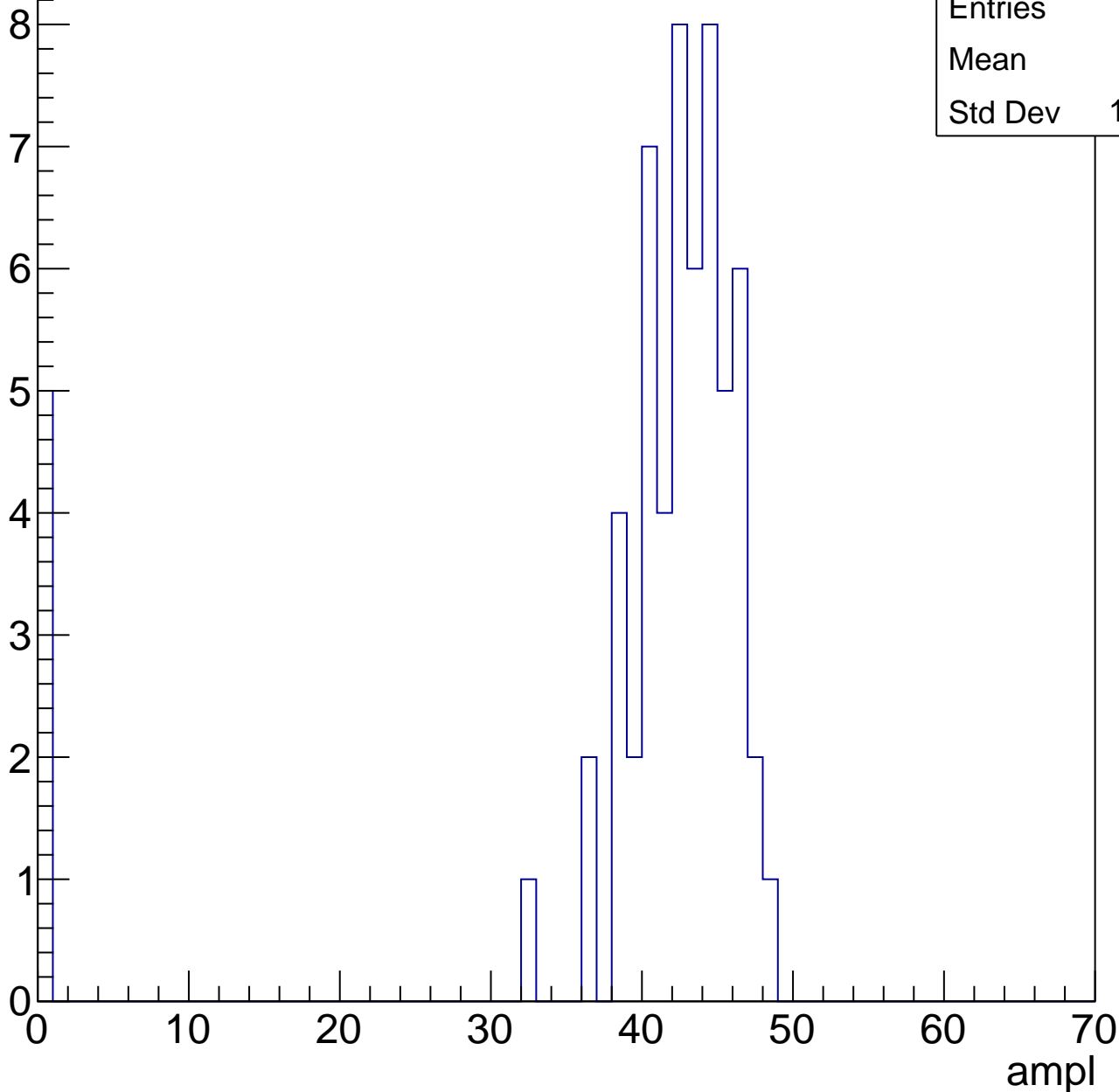


B1L103S, U11-ch80, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	38.8
Std Dev	11.98

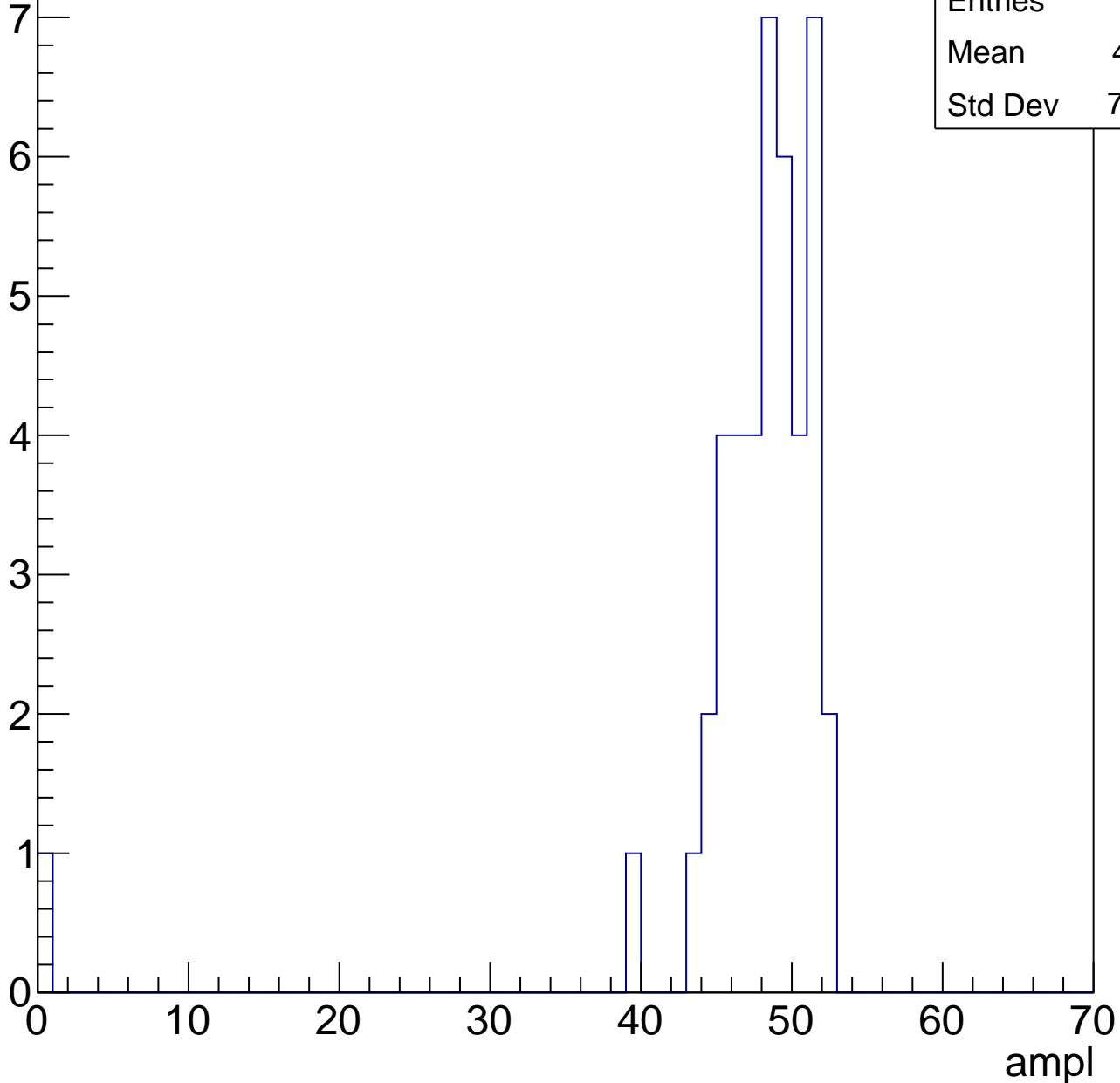


B1L103S, U11-ch80, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	43
Mean	46.81
Std Dev	7.708

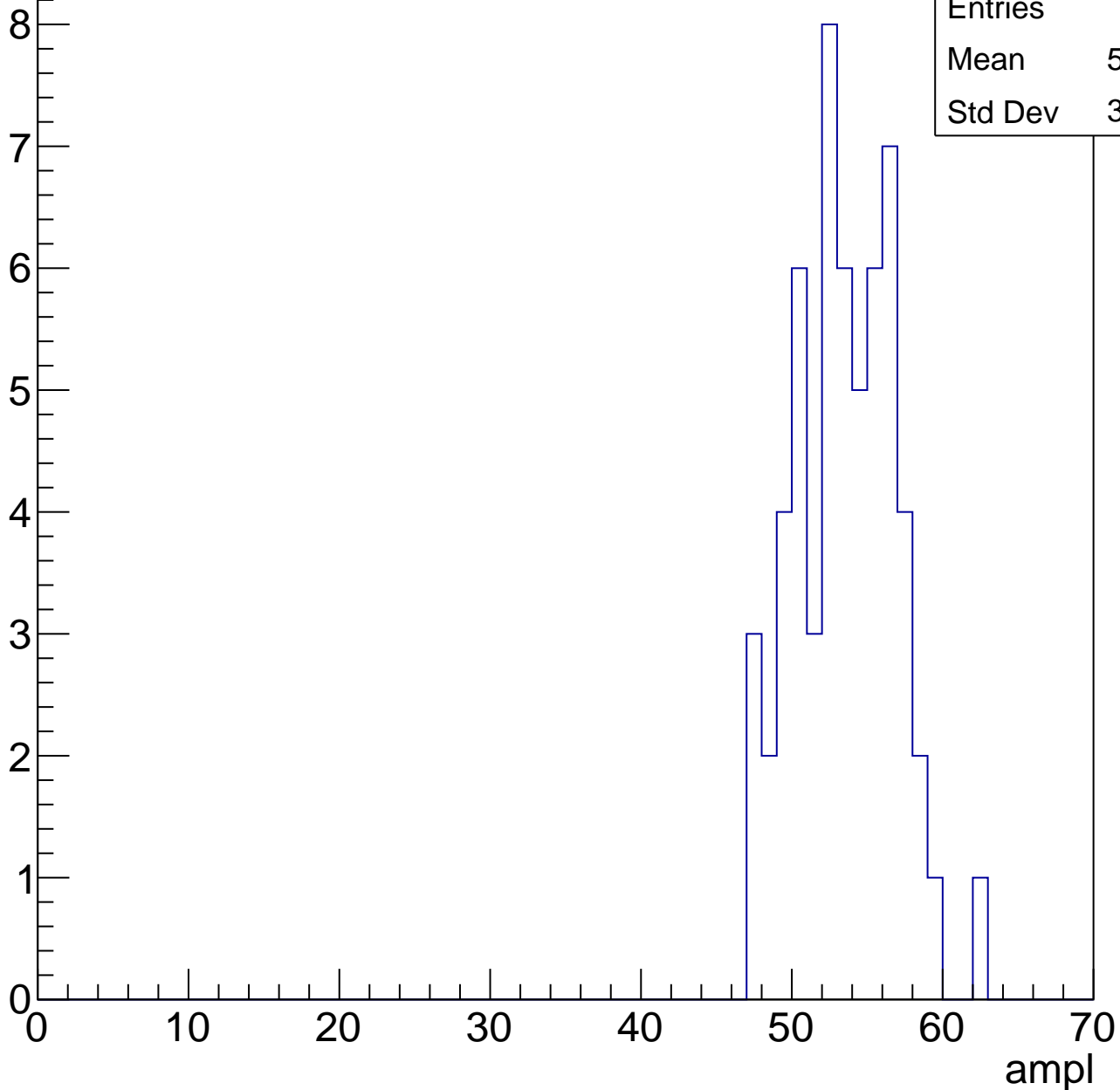


B1L103S, U11-ch80, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	53.05
Std Dev	3.266



B1L103S, U11-ch80, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

Entries	71
Mean	58.7
Std Dev	2.885

0

2

4

6

8

10

B1L103S, U11-ch80, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch80, adc7

calib_packv5_041523_1651.root, FC#0, port C2

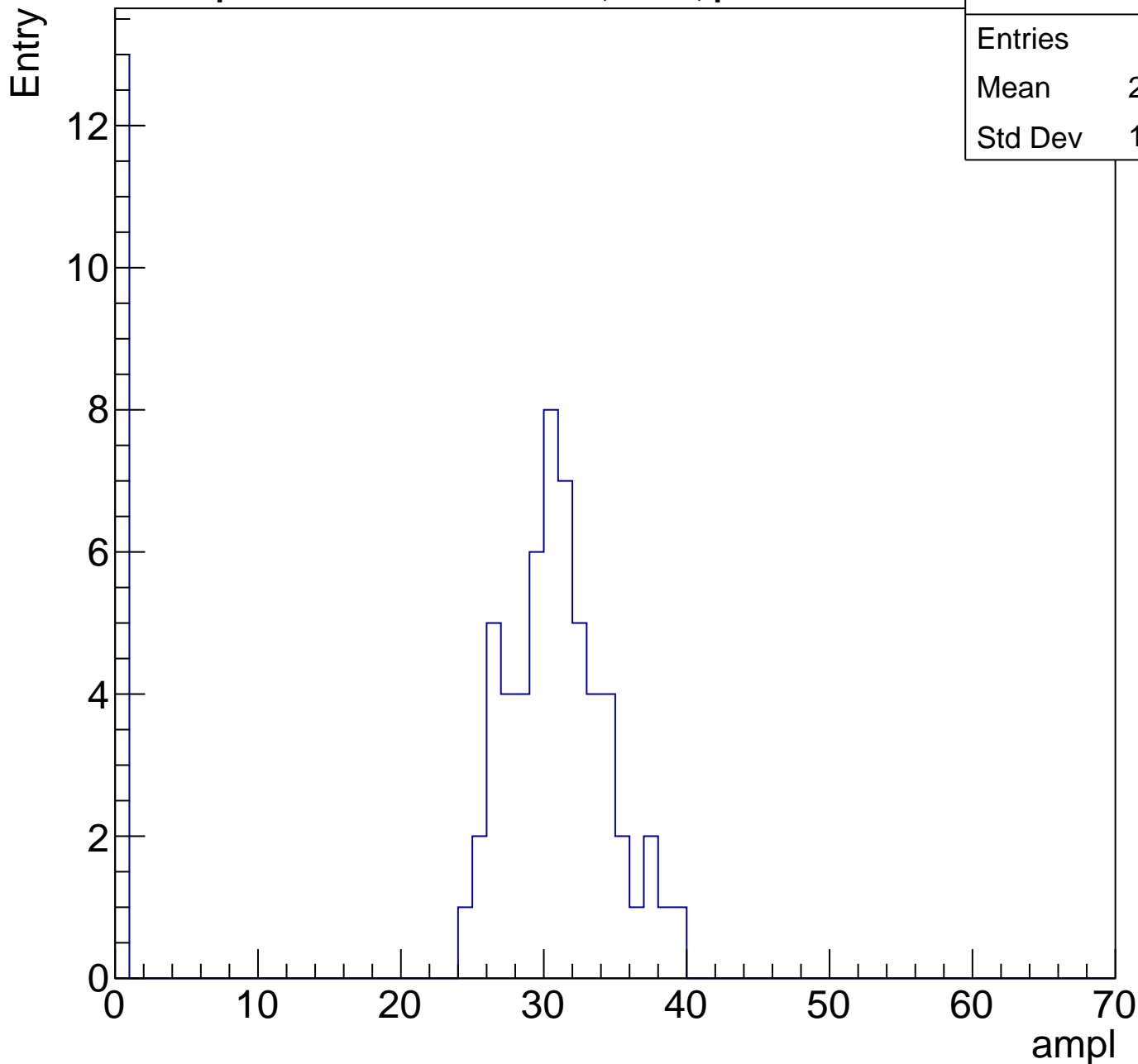
Entry



B1L103S, U11-ch81, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	70
Mean	24.86
Std Dev	12.26

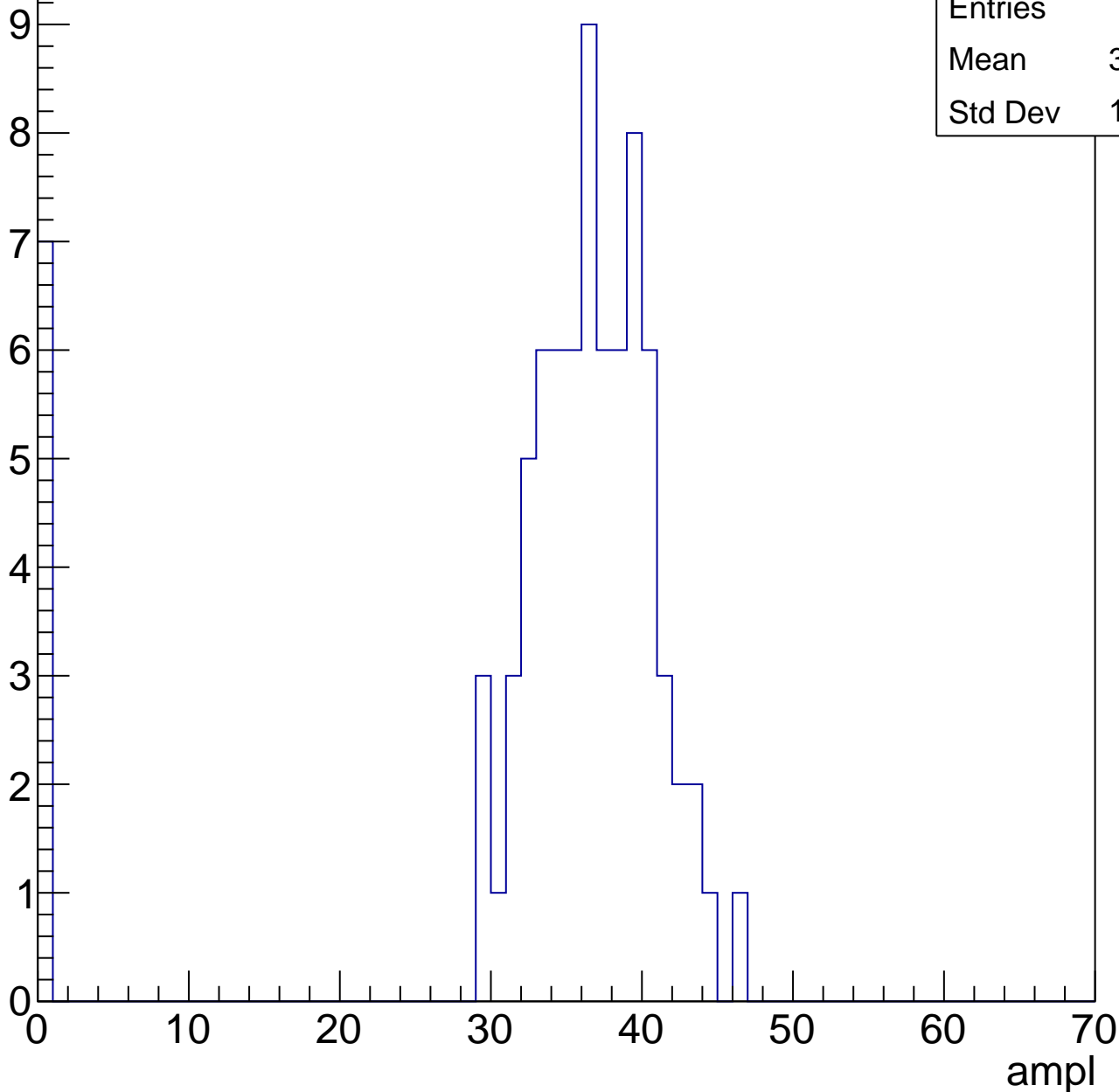


B1L103S, U11-ch81, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	81
Mean	33.22
Std Dev	10.82

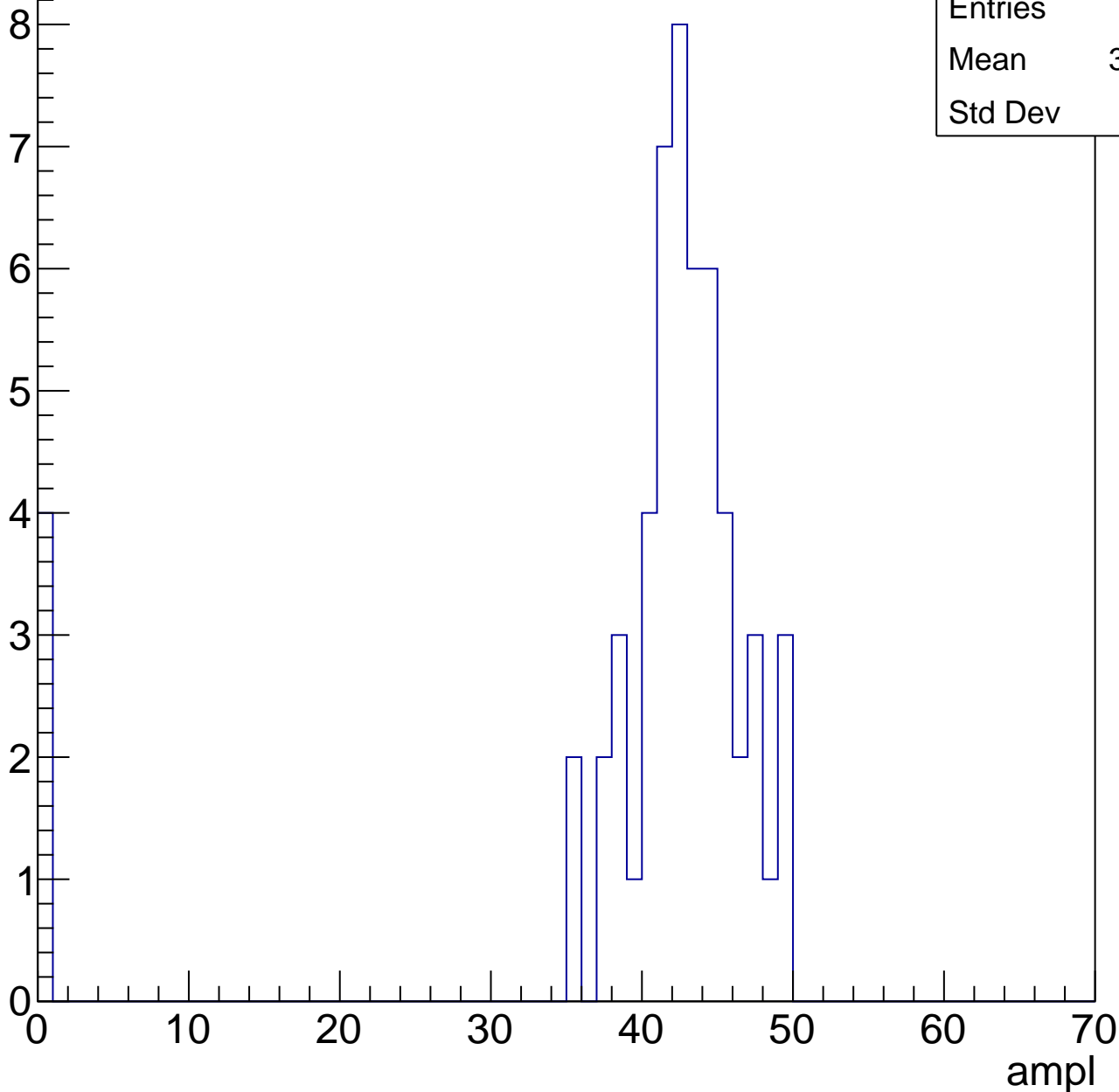


B1L103S, U11-ch81, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

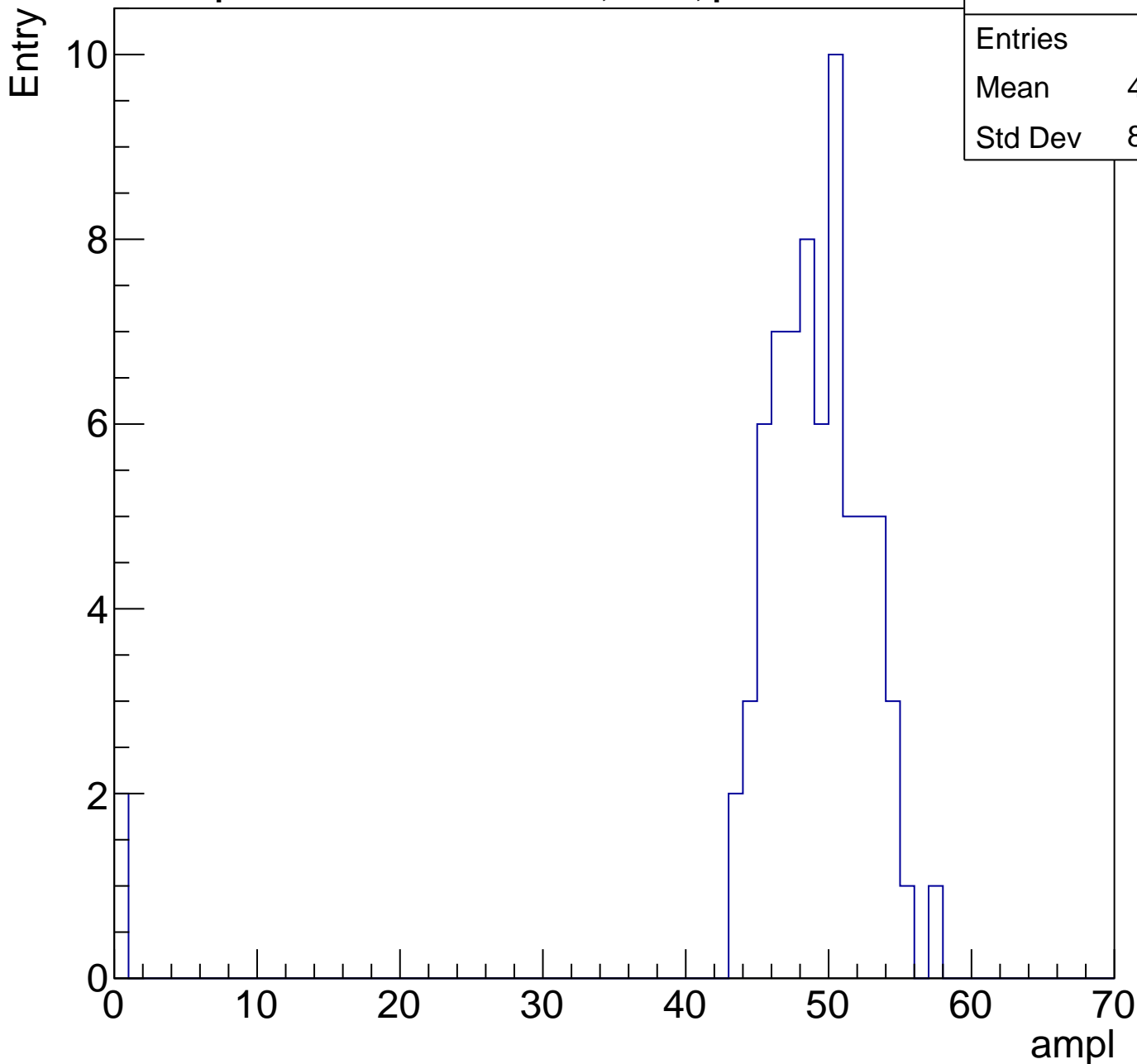
Entries	56
Mean	39.46
Std Dev	11.4



B1L103S, U11-ch81, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	71
Mean	47.48
Std Dev	8.648

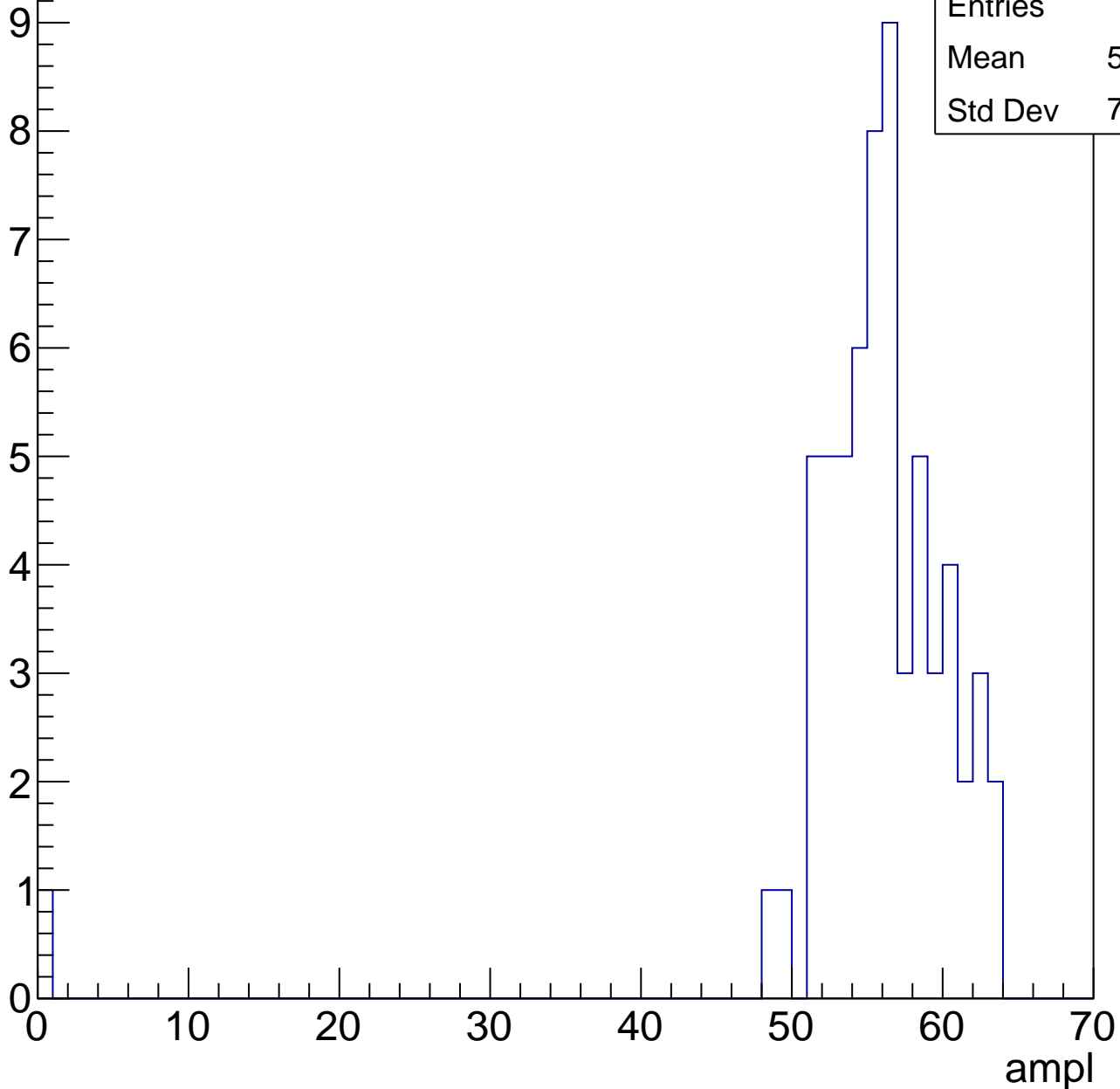


B1L103S, U11-ch81, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

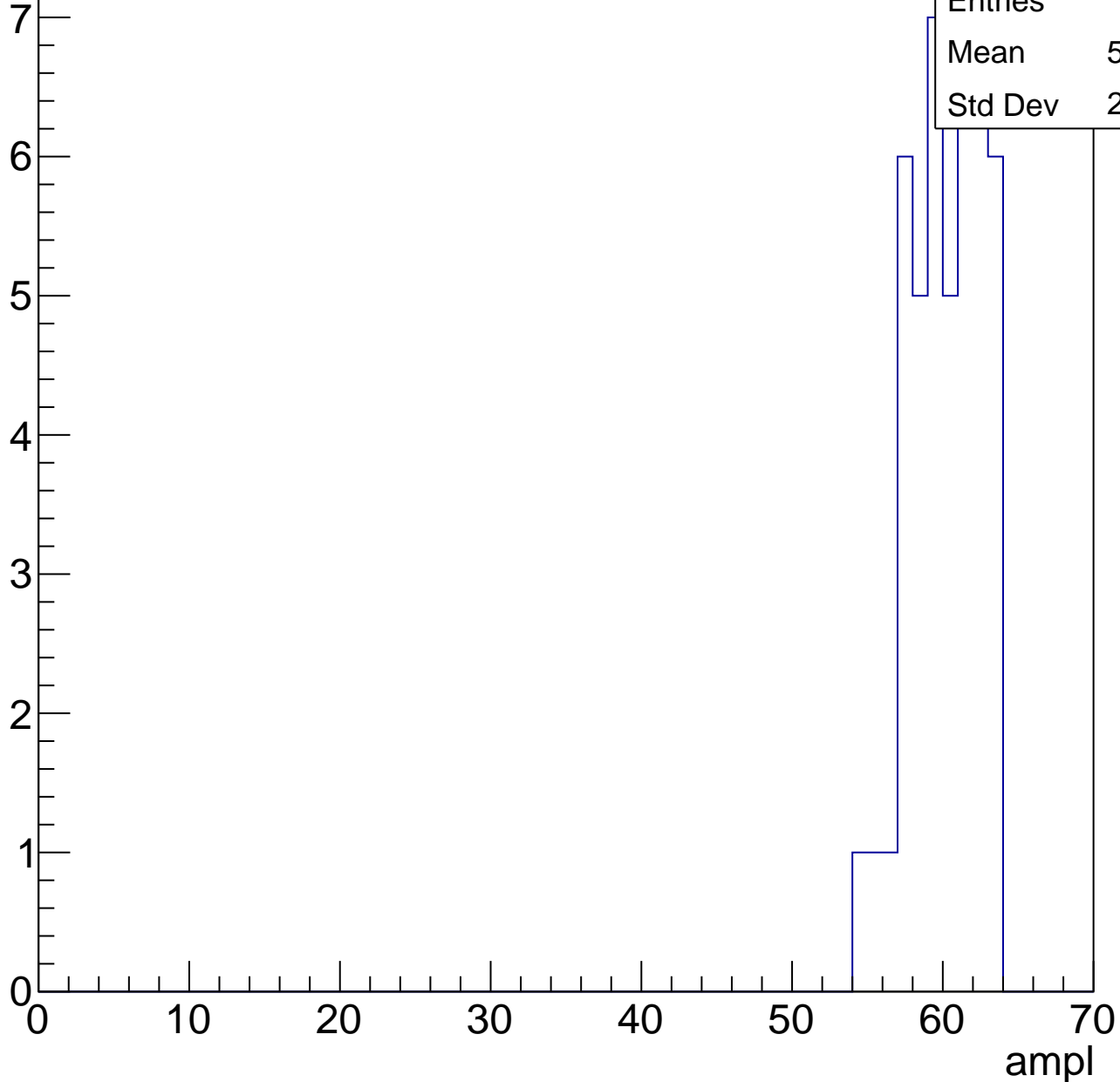
Entries	63
Mean	54.87
Std Dev	7.788



B1L103S, U11-ch81, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch81, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch81, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

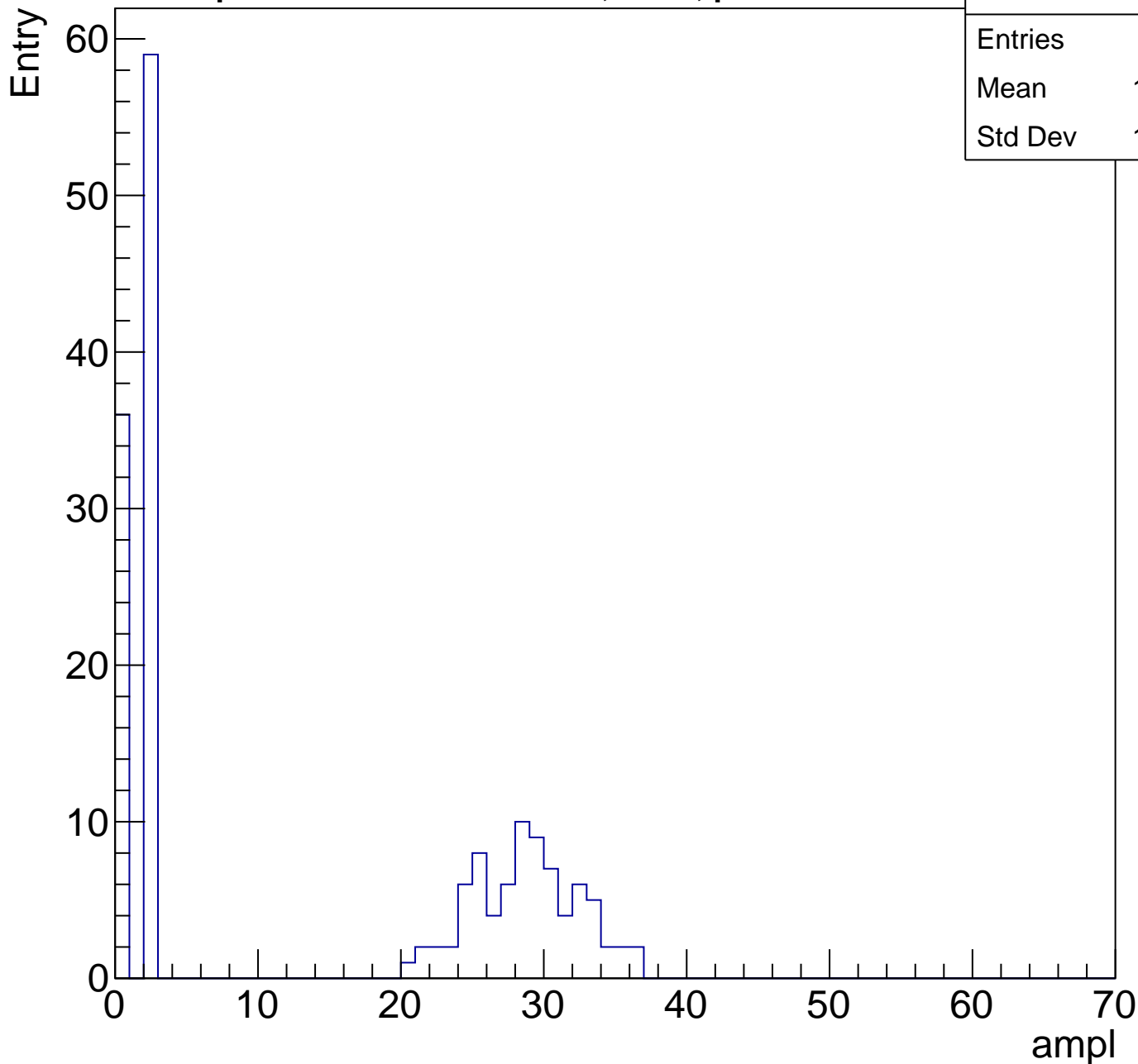
Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U11-ch82, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	173
Mean	13.42
Std Dev	13.69



B1L103S, U11-ch82, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	76
Mean	28.54
Std Dev	14.22

Entry

10

8

6

4

2

0

ampl

0

10

20

30

40

50

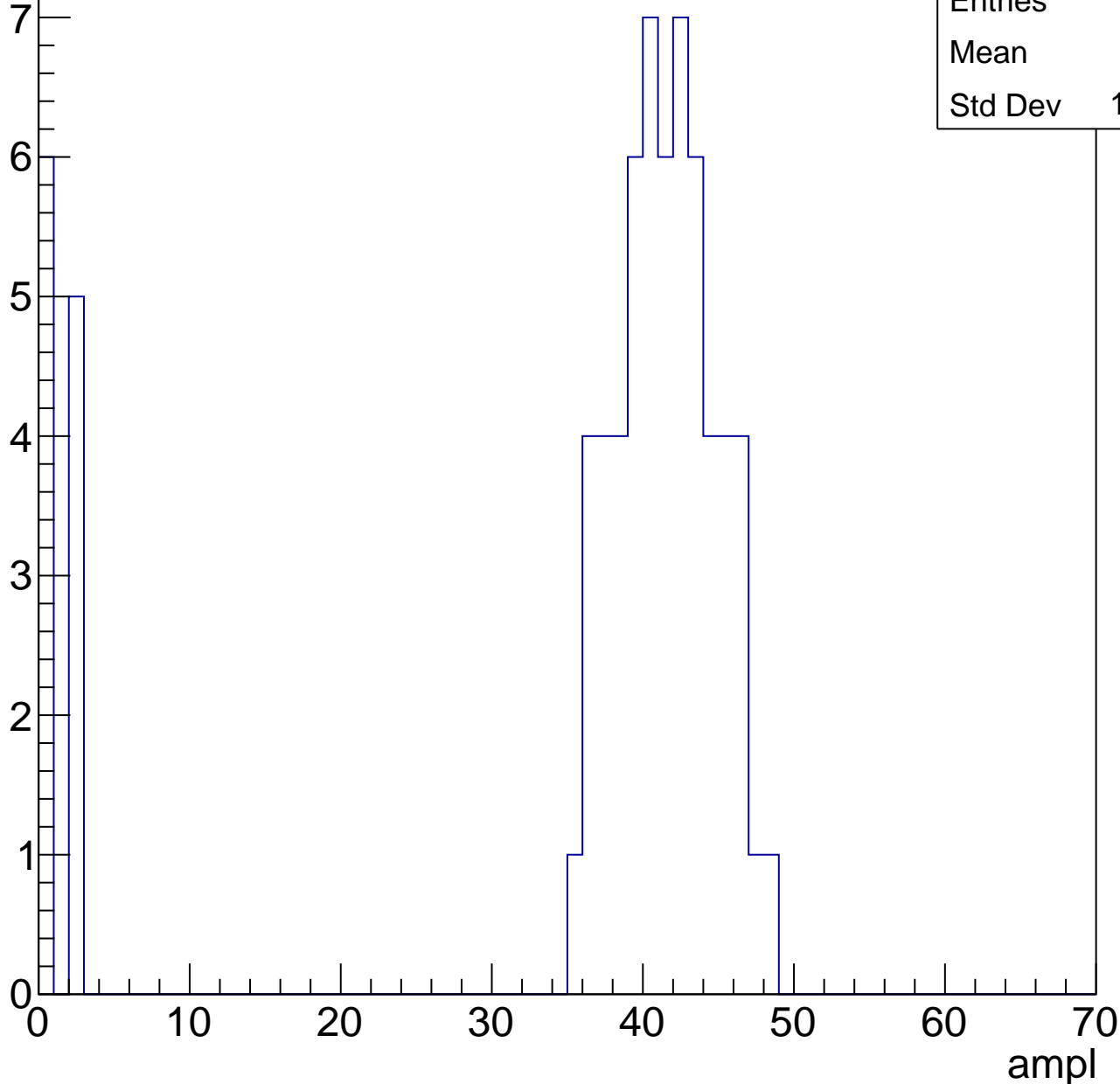
60

70

B1L103S, U11-ch82, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry



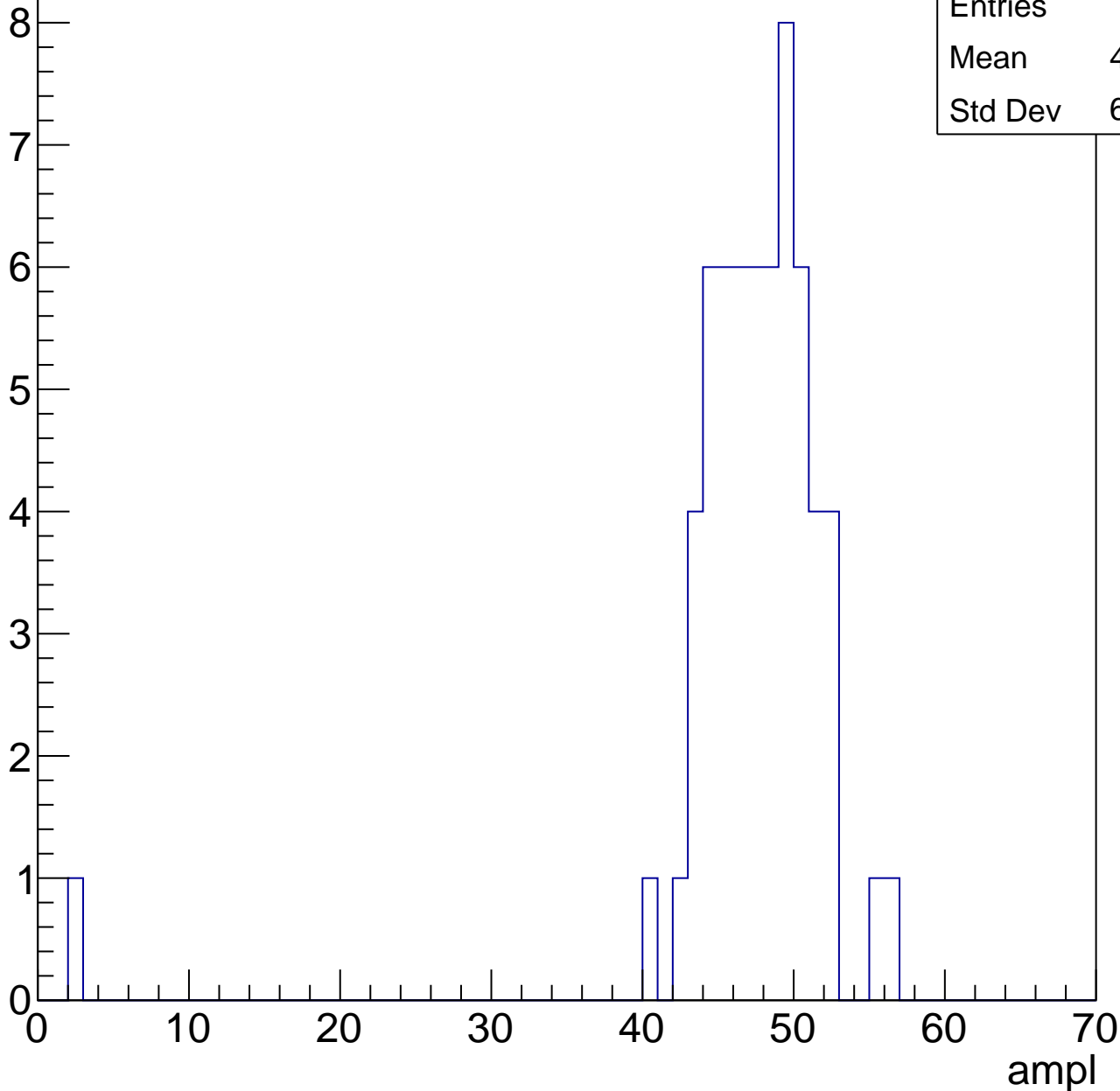
Entries	70
Mean	34.8
Std Dev	14.92

B1L103S, U11-ch82, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	46.74
Std Dev	6.583

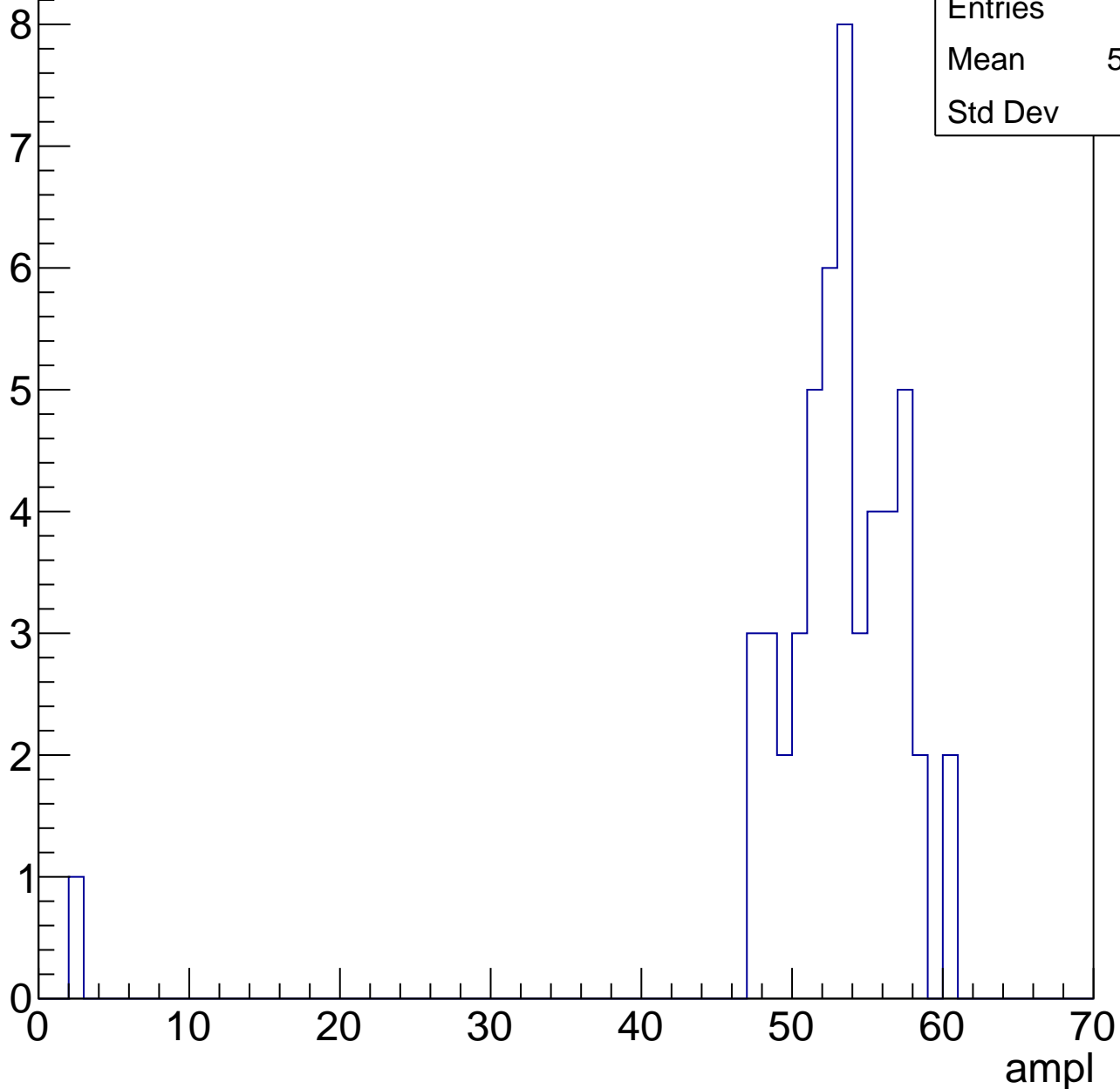


B1L103S, U11-ch82, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

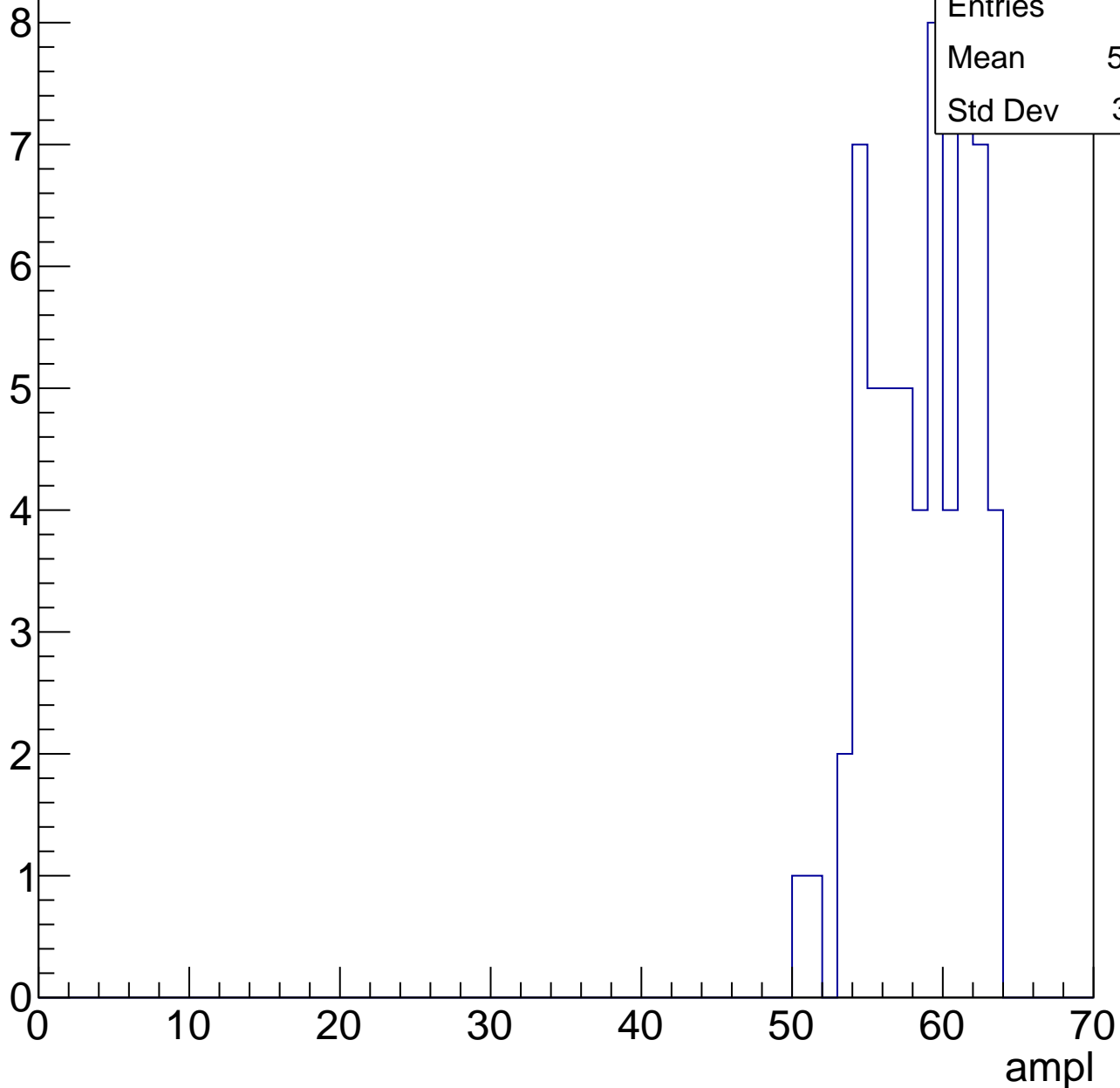
Entries	51
Mean	52.02
Std Dev	7.8



B1L103S, U11-ch82, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



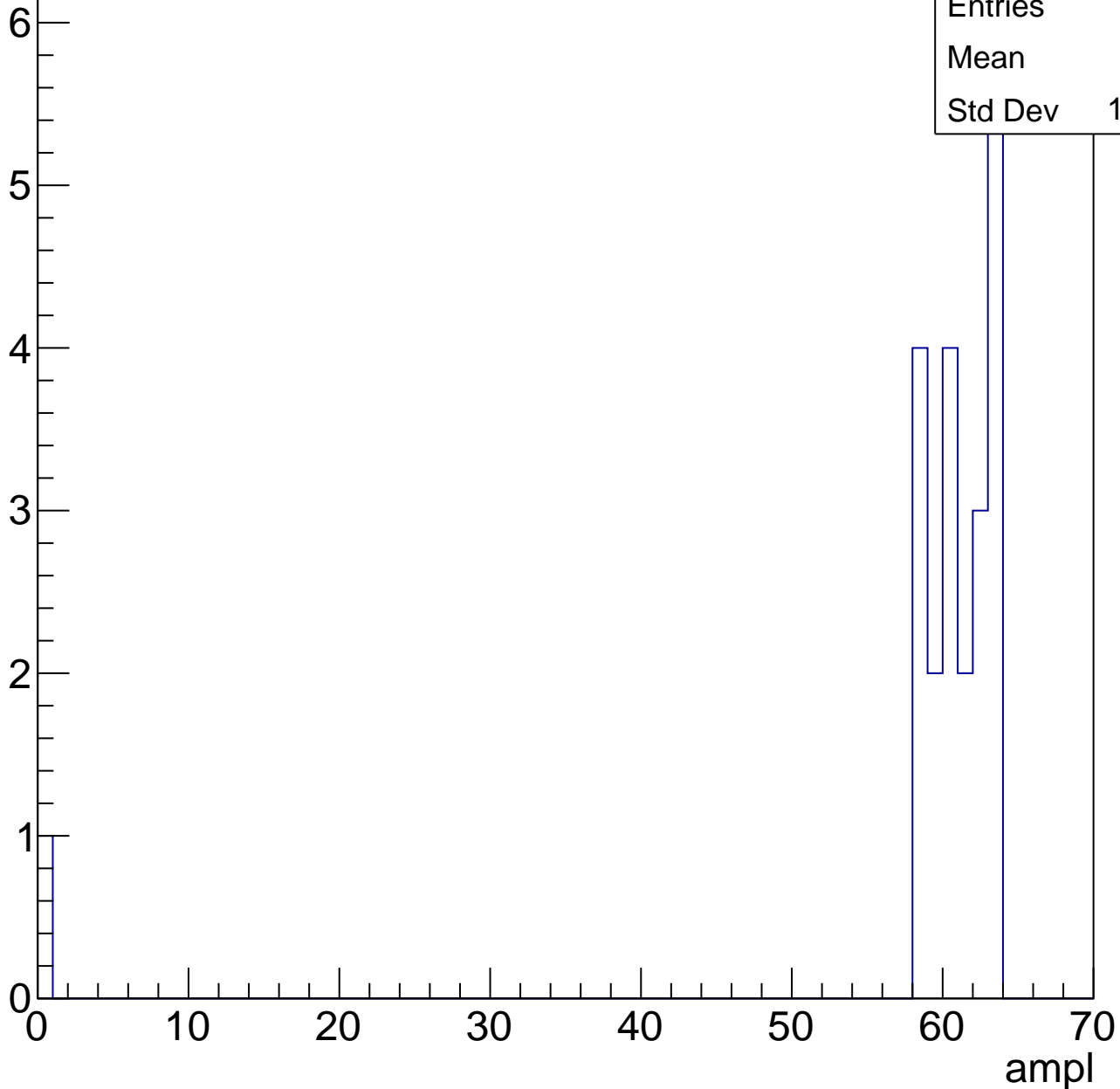
Entries	61
Mean	58.08
Std Dev	3.271

B1L103S, U11-ch82, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	22
Mean	58
Std Dev	12.79

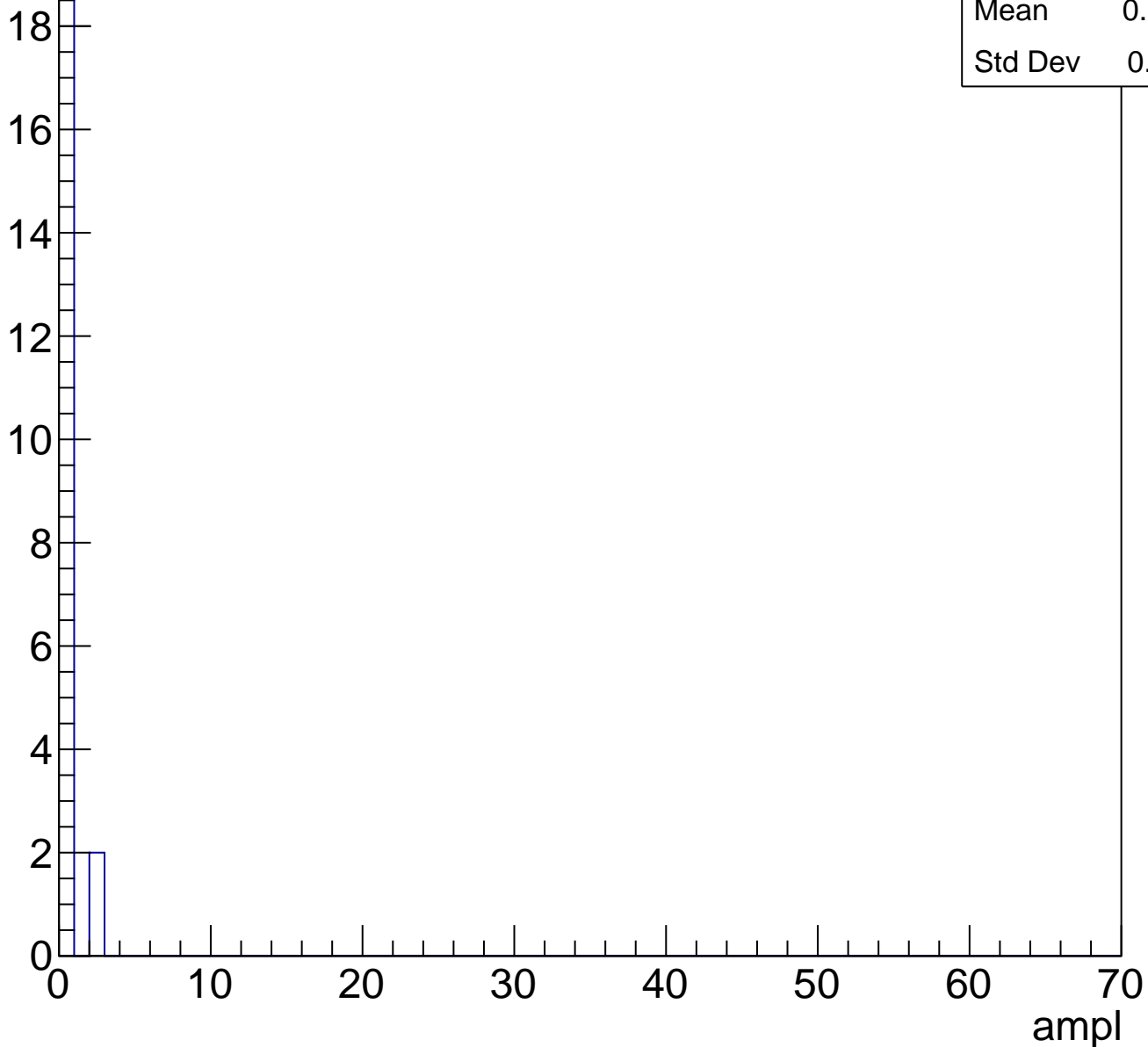


B1L103S, U11-ch82, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	0.1905
Std Dev	0.5871

Entry

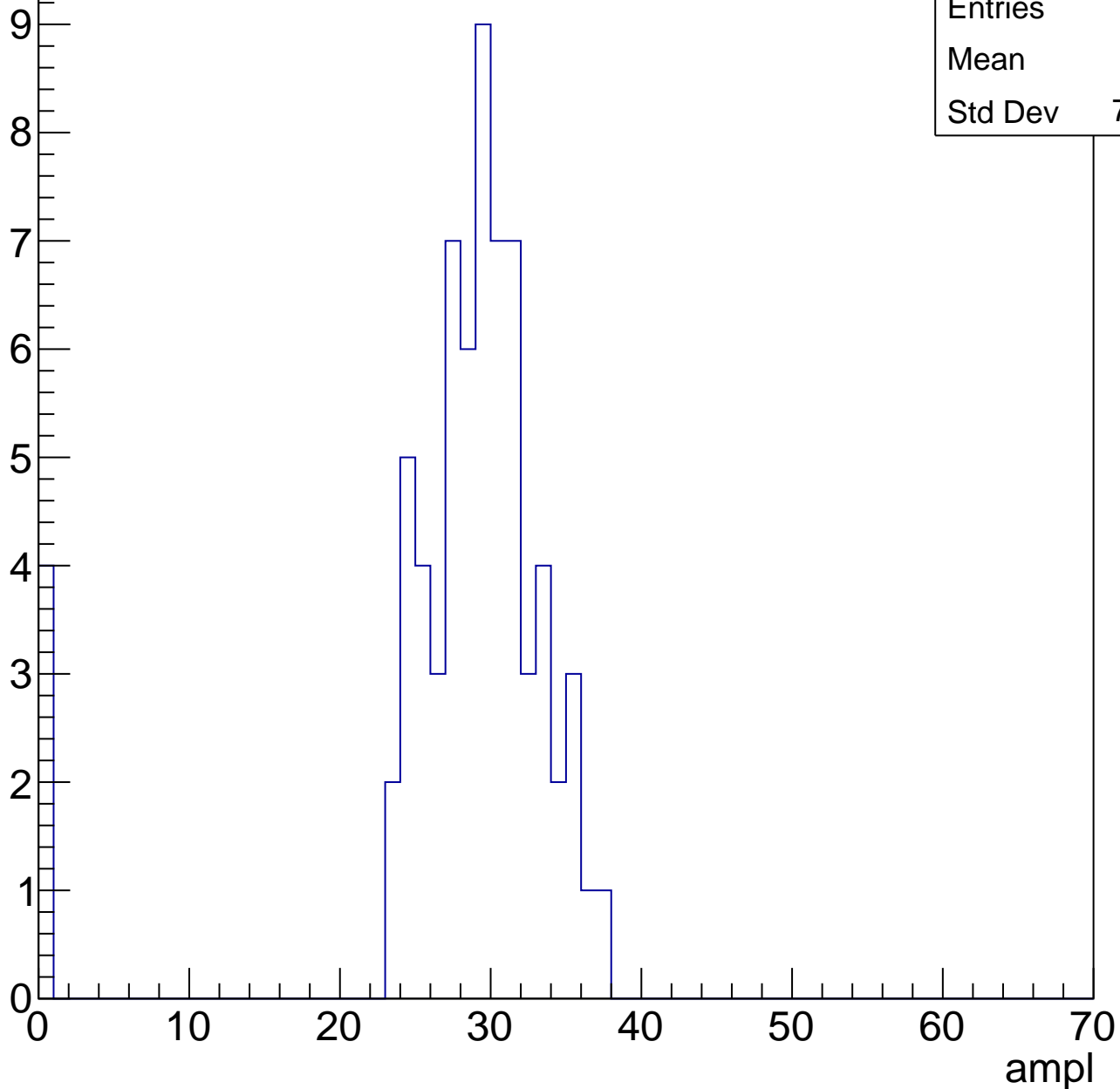


B1L103S, U11-ch83, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	27.4
Std Dev	7.581

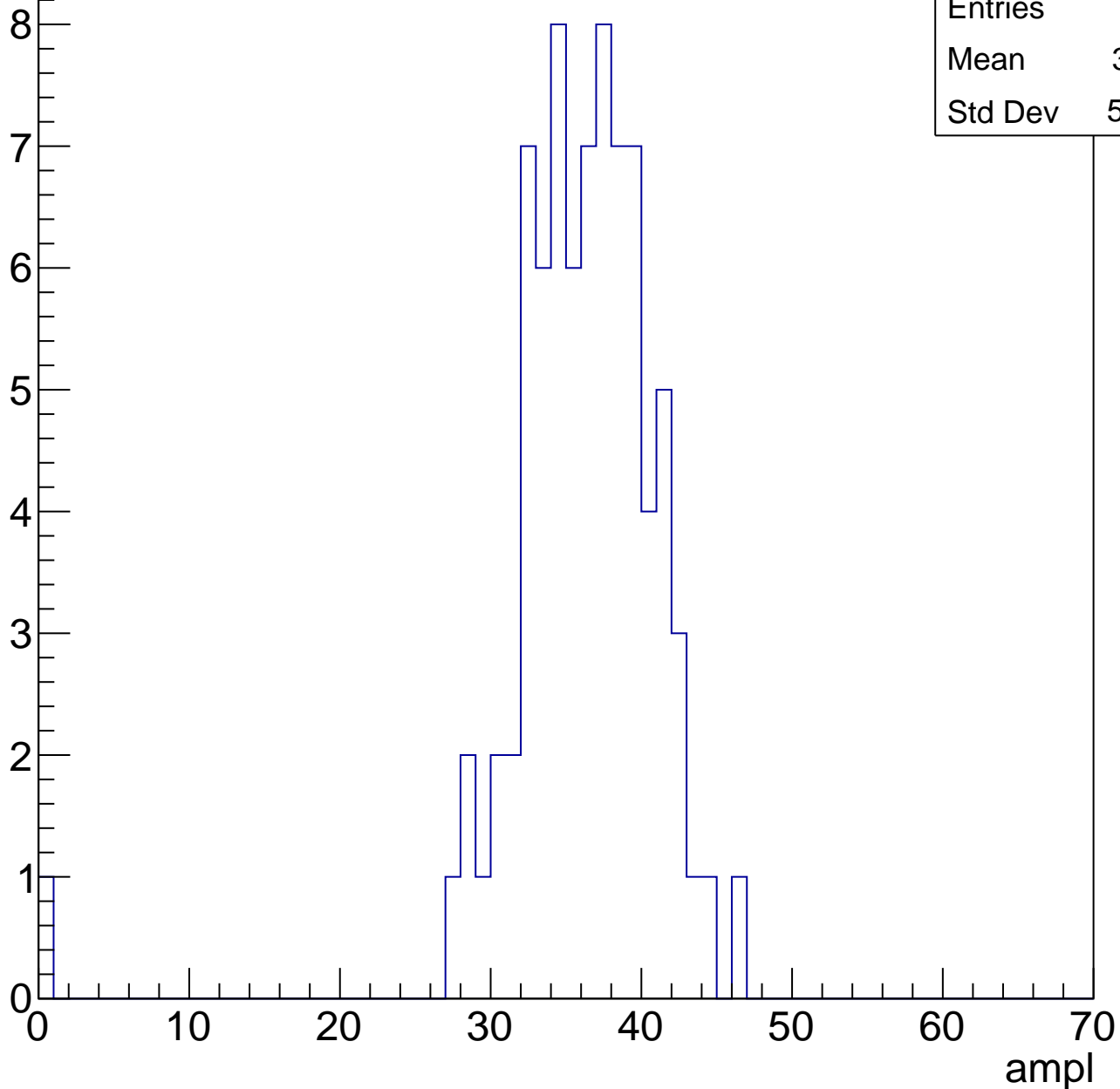


B1L103S, U11-ch83, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	80
Mean	35.61
Std Dev	5.564

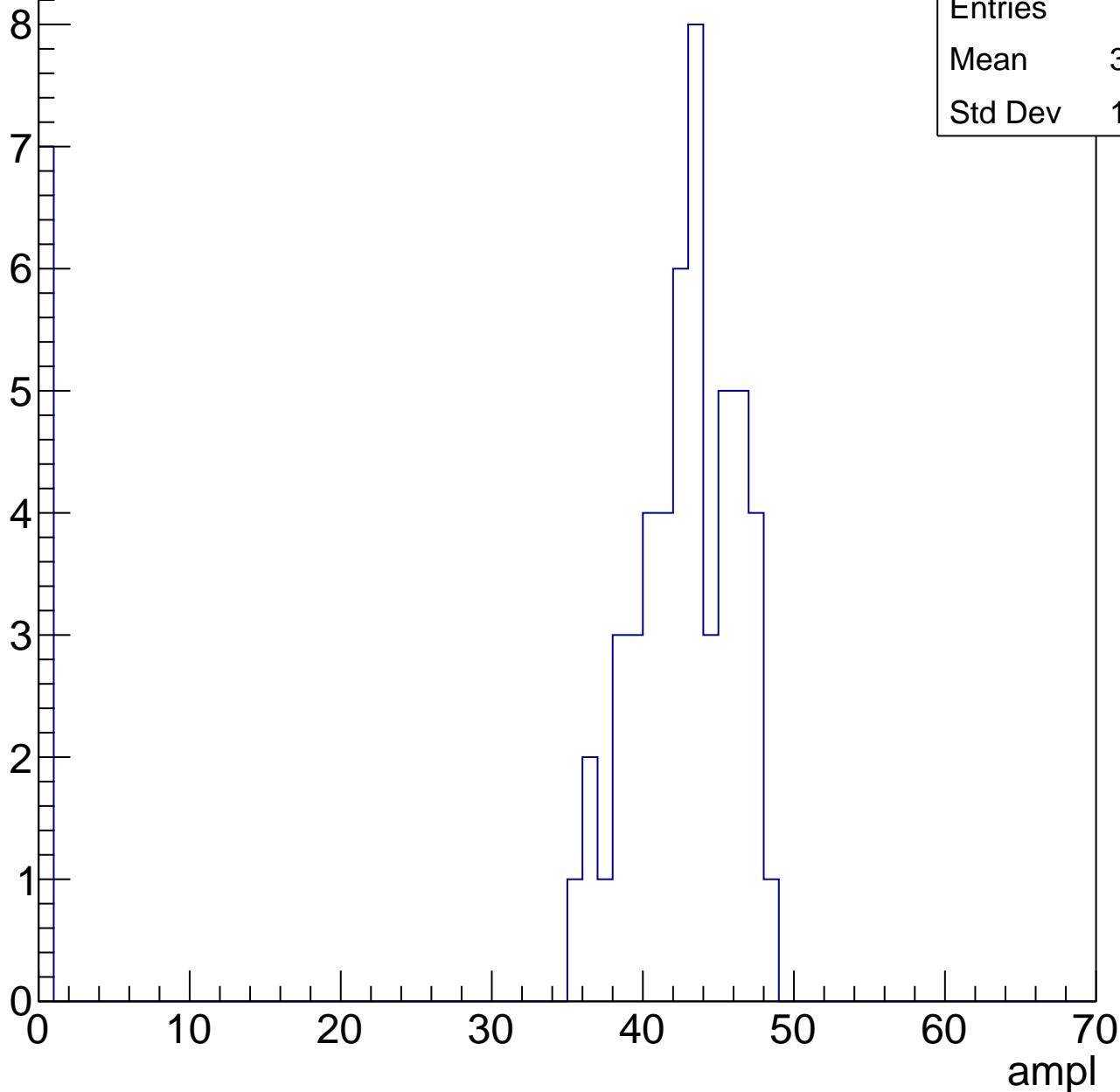


B1L103S, U11-ch83, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

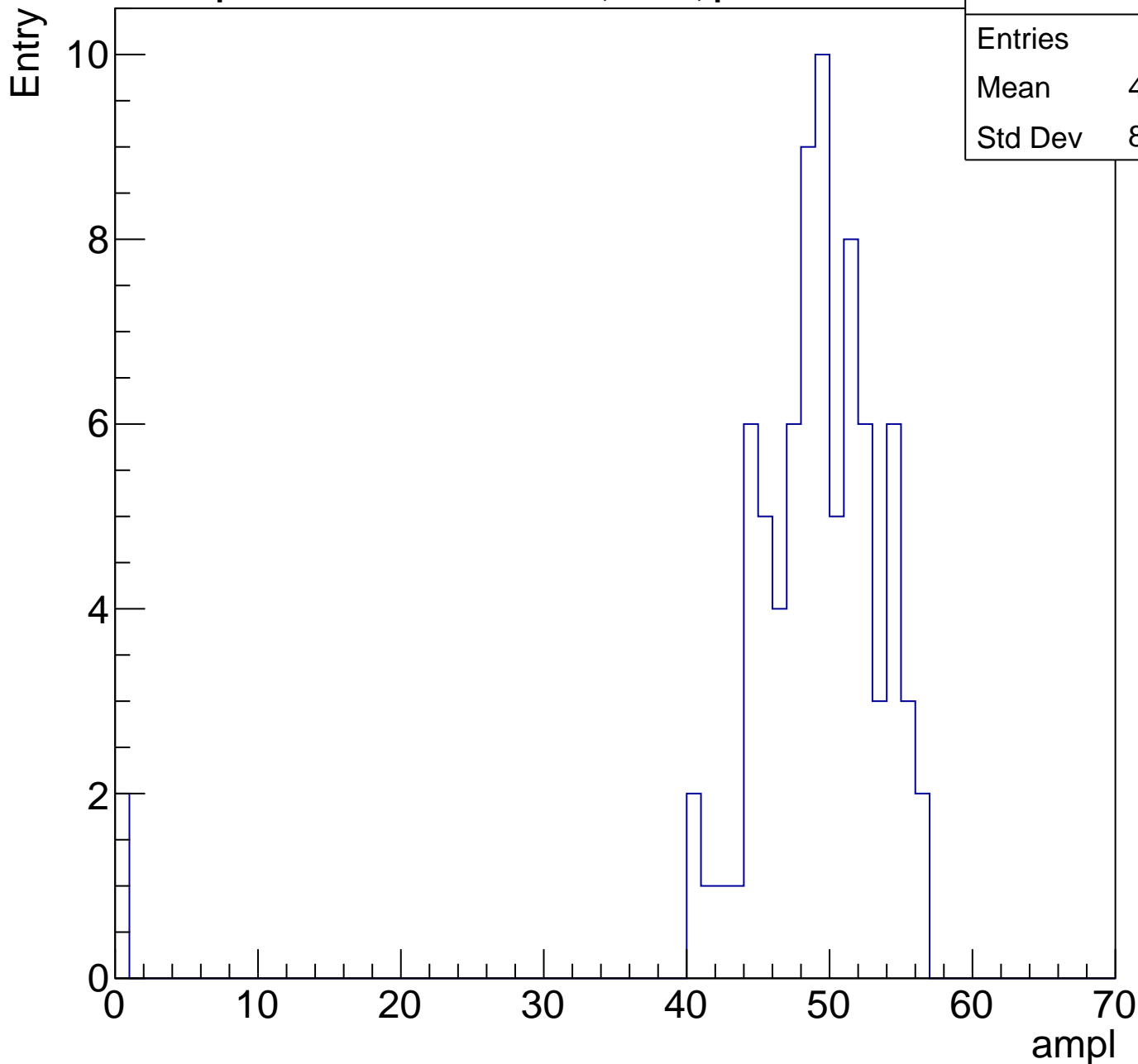
Entries	57
Mean	37.16
Std Dev	14.22



B1L103S, U11-ch83, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	47.66
Std Dev	8.488

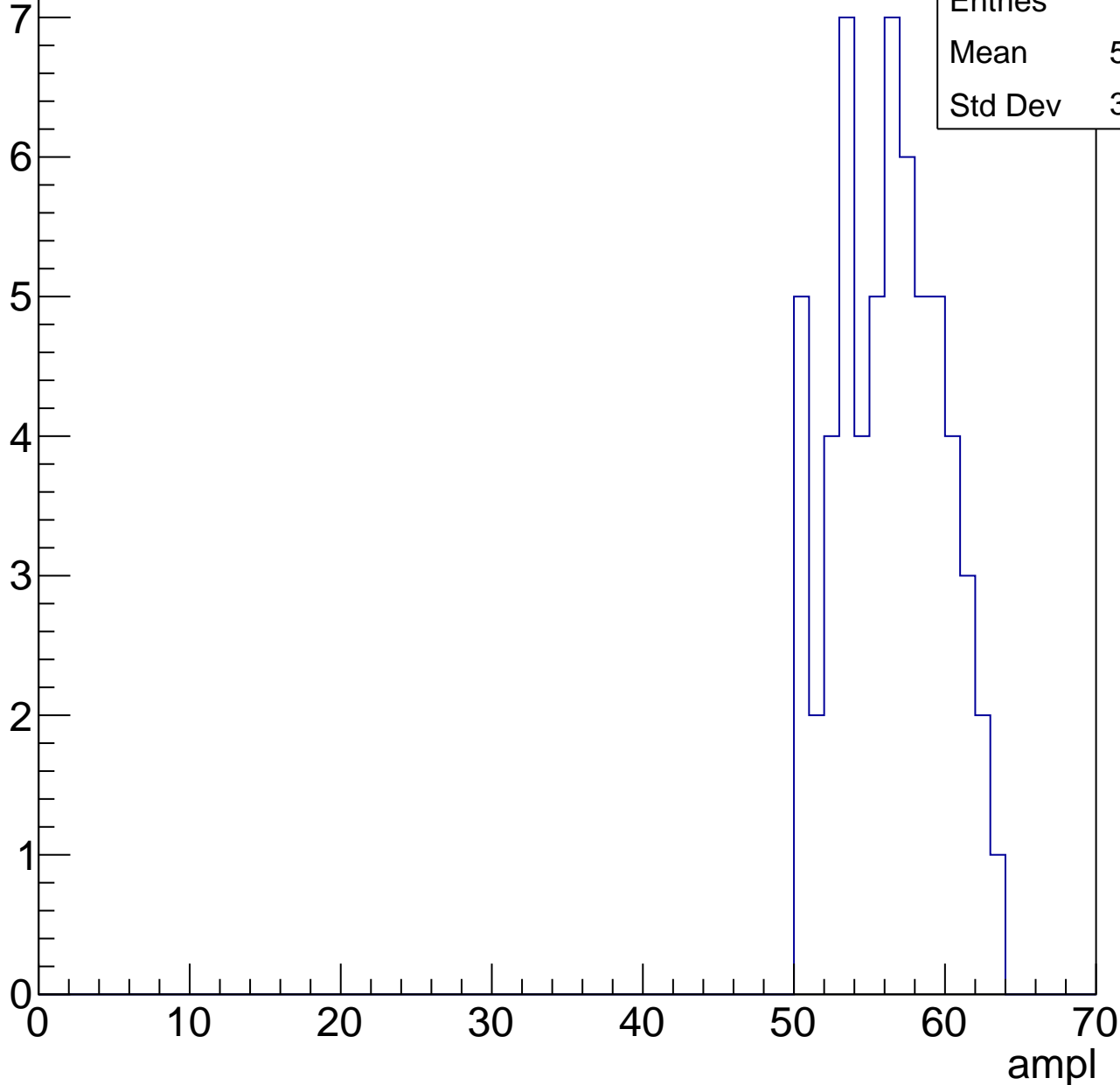


B1L103S, U11-ch83, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	55.85
Std Dev	3.434



B1L103S, U11-ch83, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

7

6

5

4

3

2

1

0

Entries

41

Mean

58.51

Std Dev

9.528

ampl

0

10

20

30

40

50

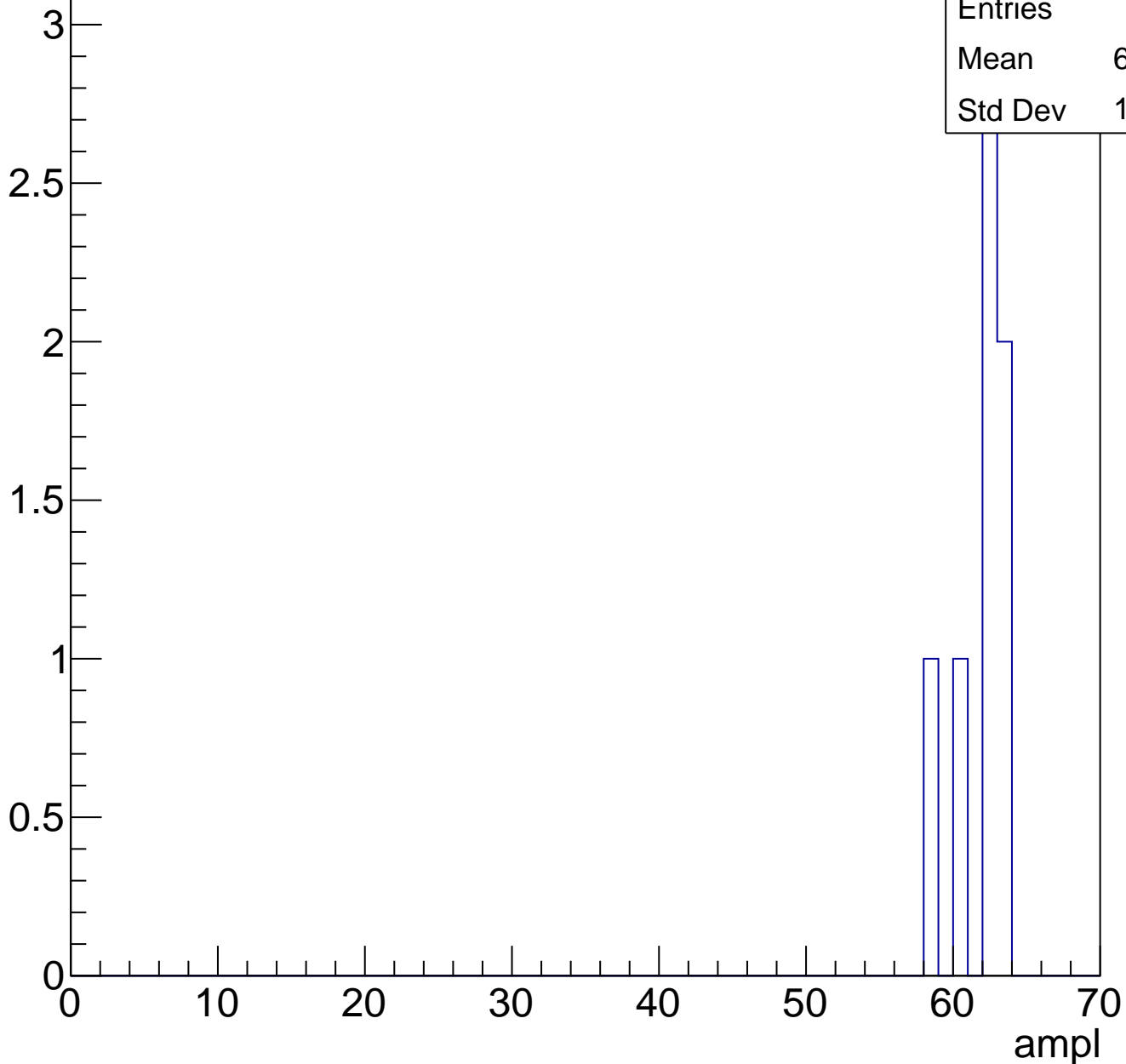
60

70

B1L103S, U11-ch83, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch83, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch84, adc0

calib_packv5_041523_1651.root, FC#0, port C2

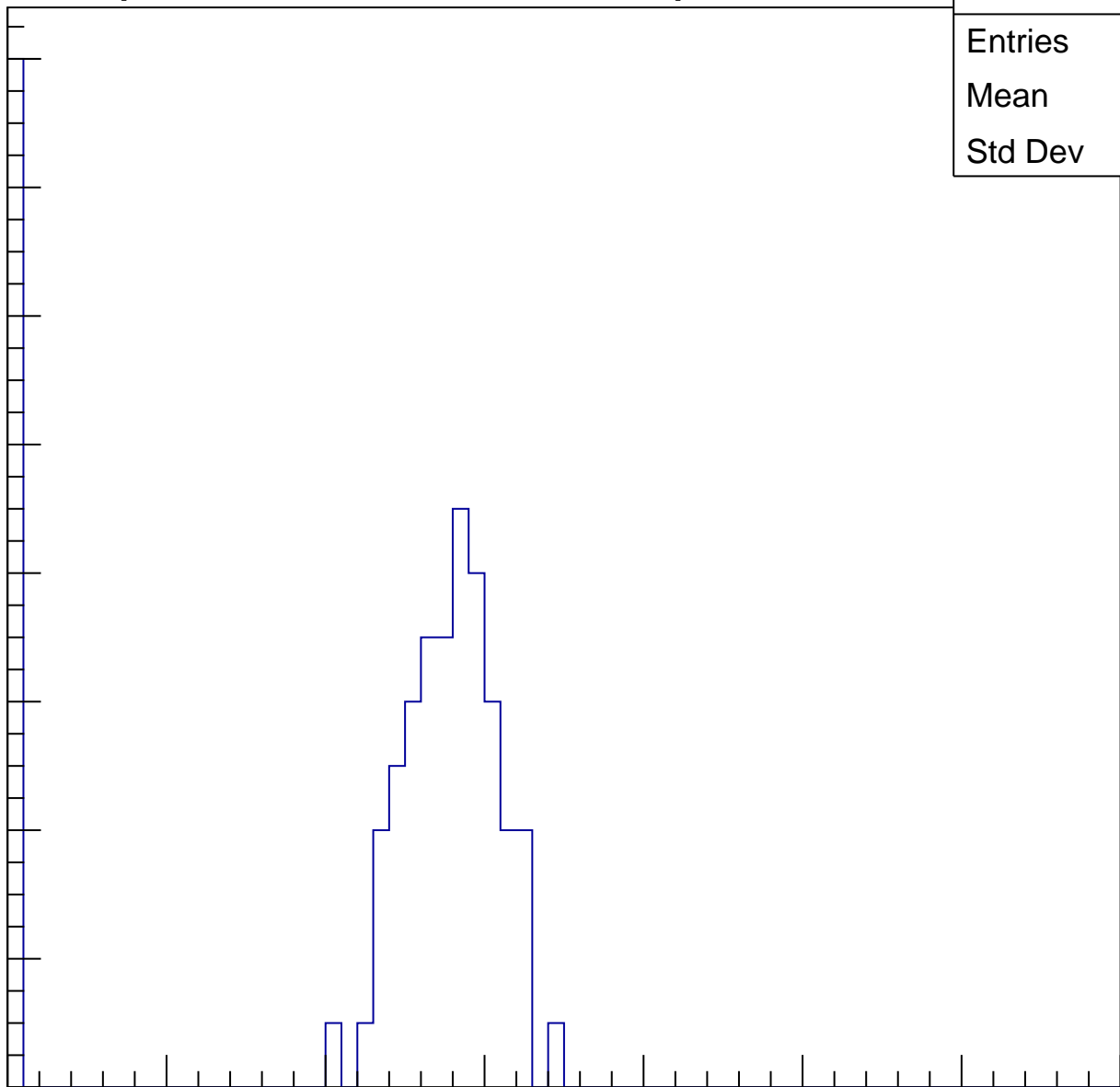
Entries	79
Mean	21.84
Std Dev	11.3

Entry

16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

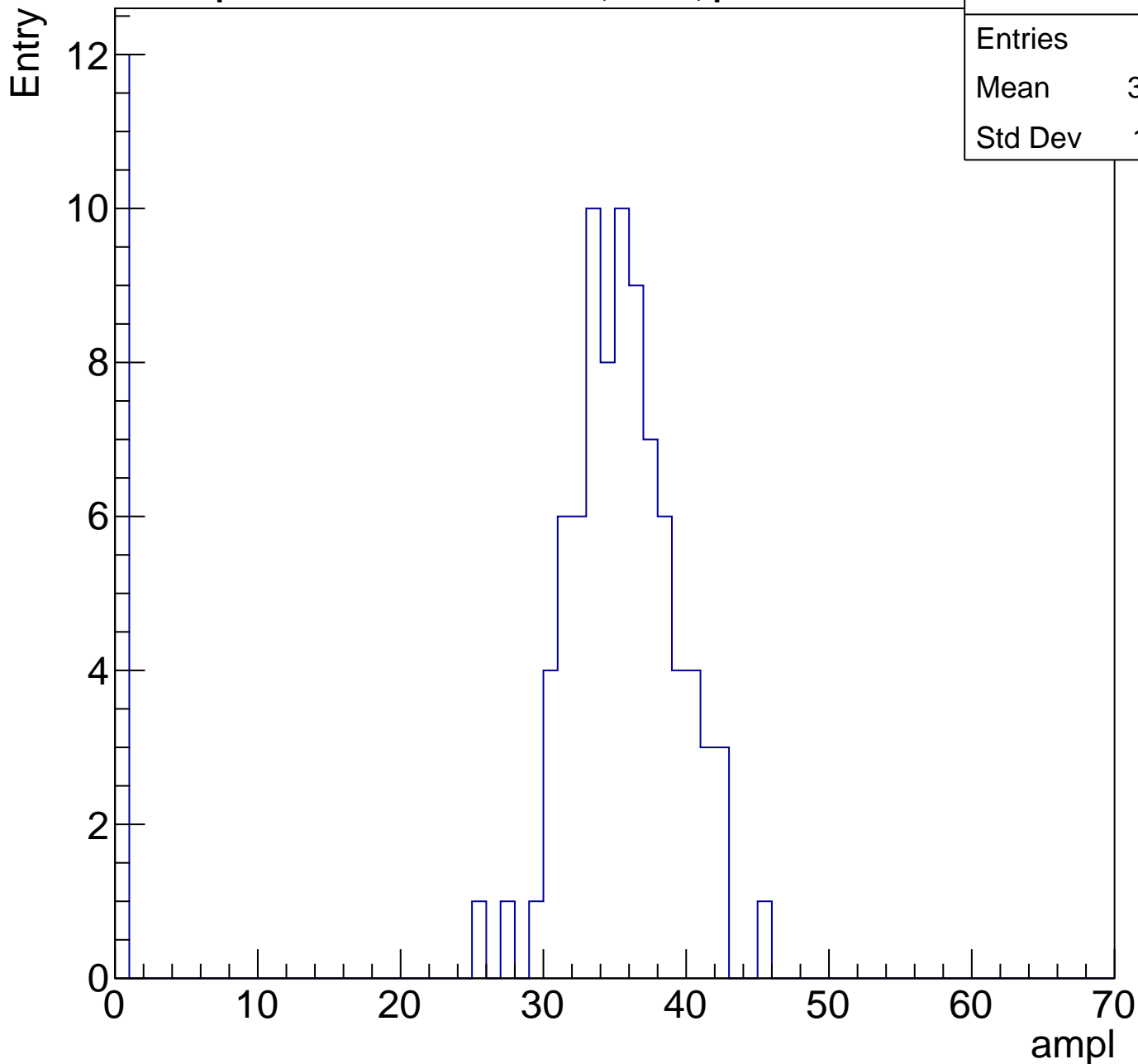
ampl



B1L103S, U11-ch84, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	96
Mean	30.75
Std Dev	12.11

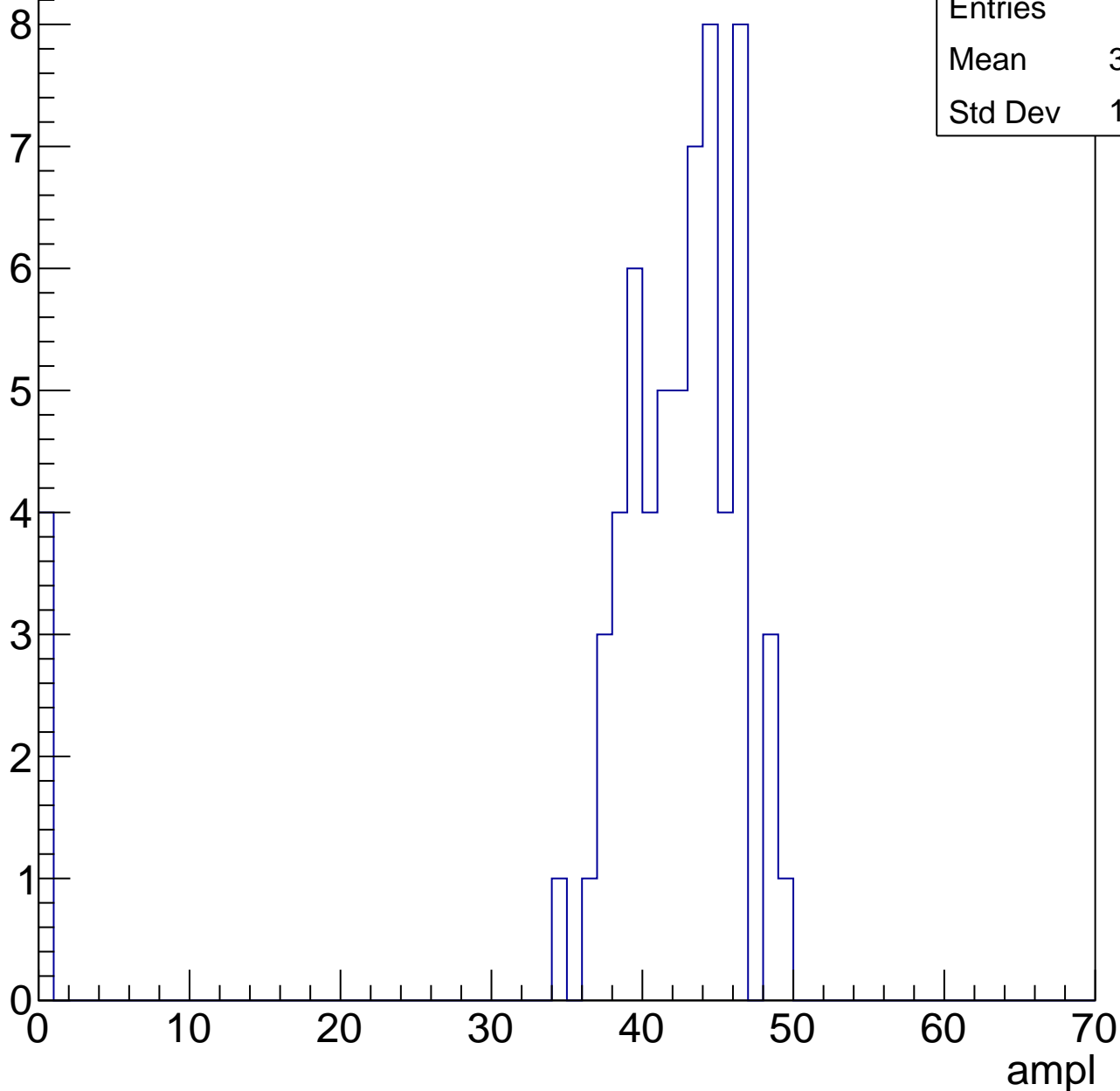


B1L103S, U11-ch84, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	39.62
Std Dev	10.73

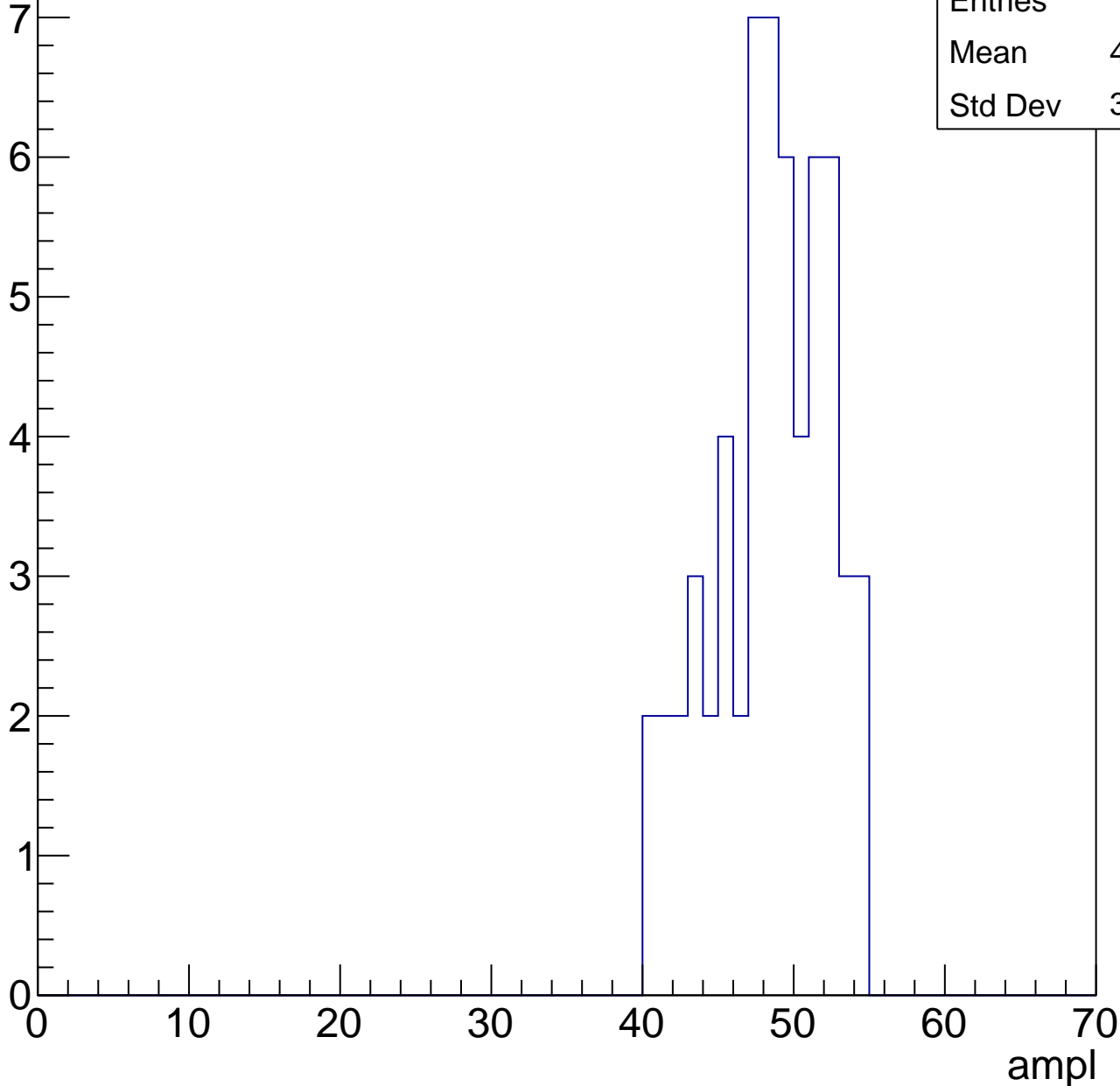


B1L103S, U11-ch84, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	48.02
Std Dev	3.707

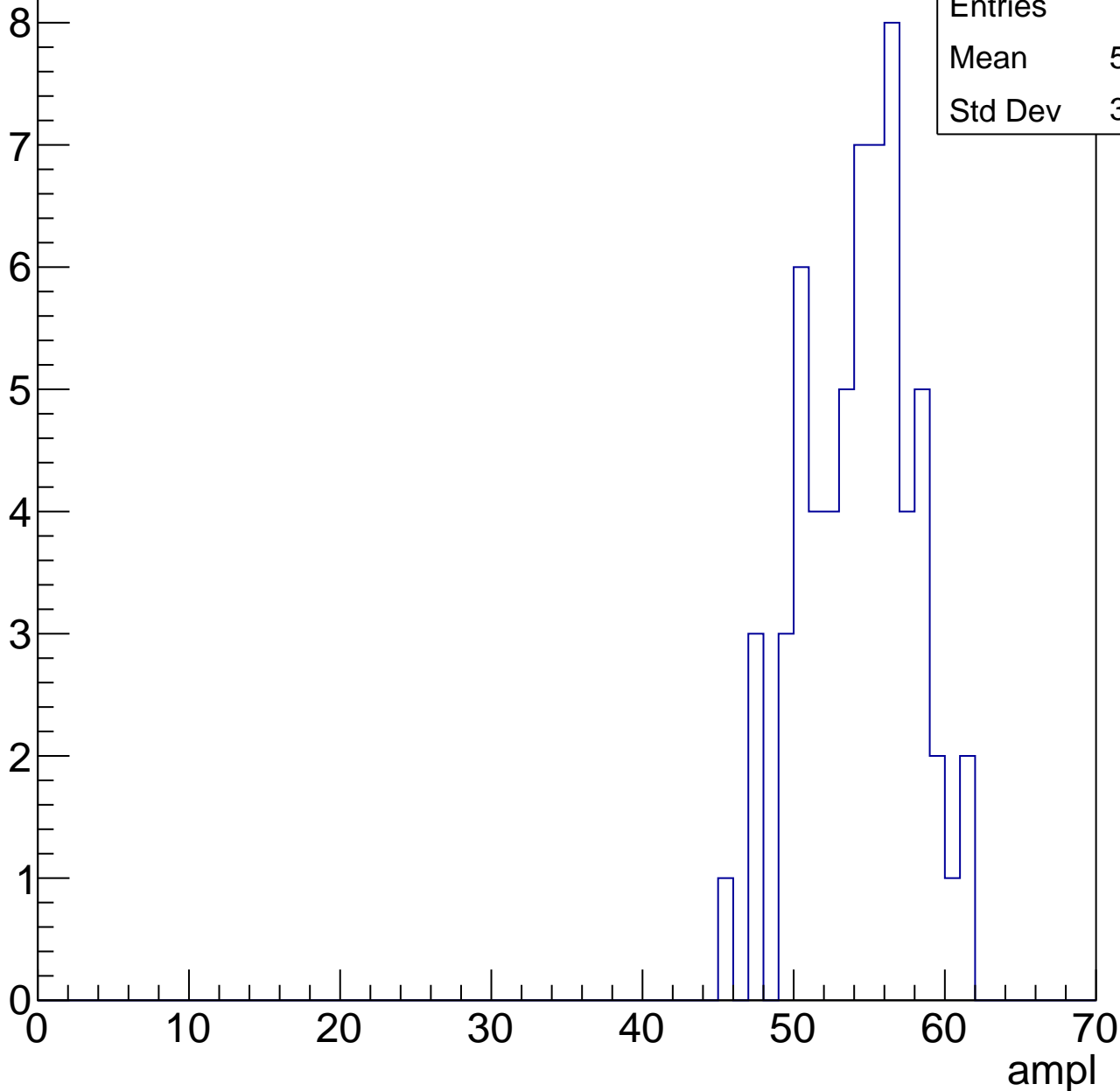


B1L103S, U11-ch84, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	53.85
Std Dev	3.578

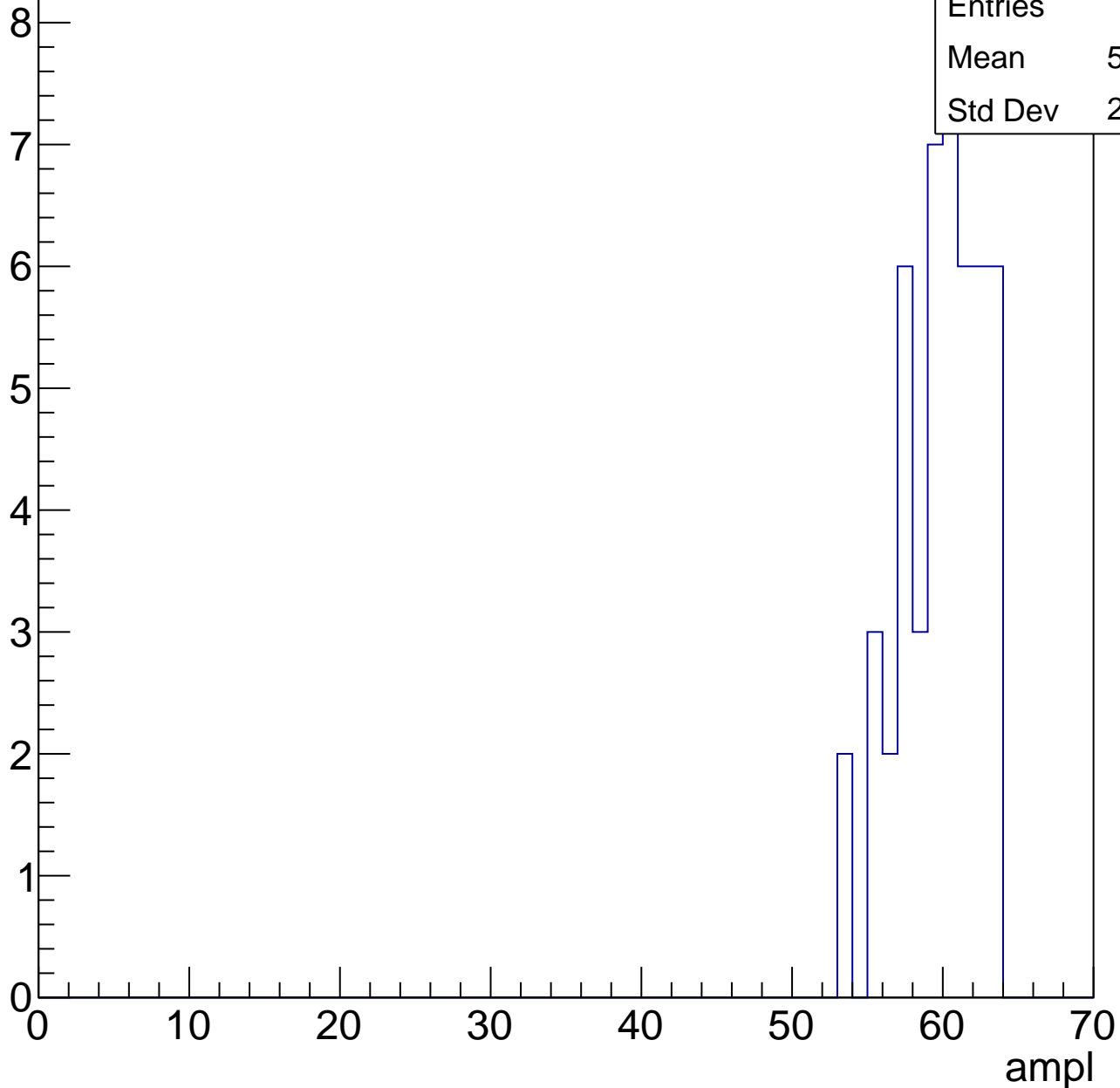


B1L103S, U11-ch84, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

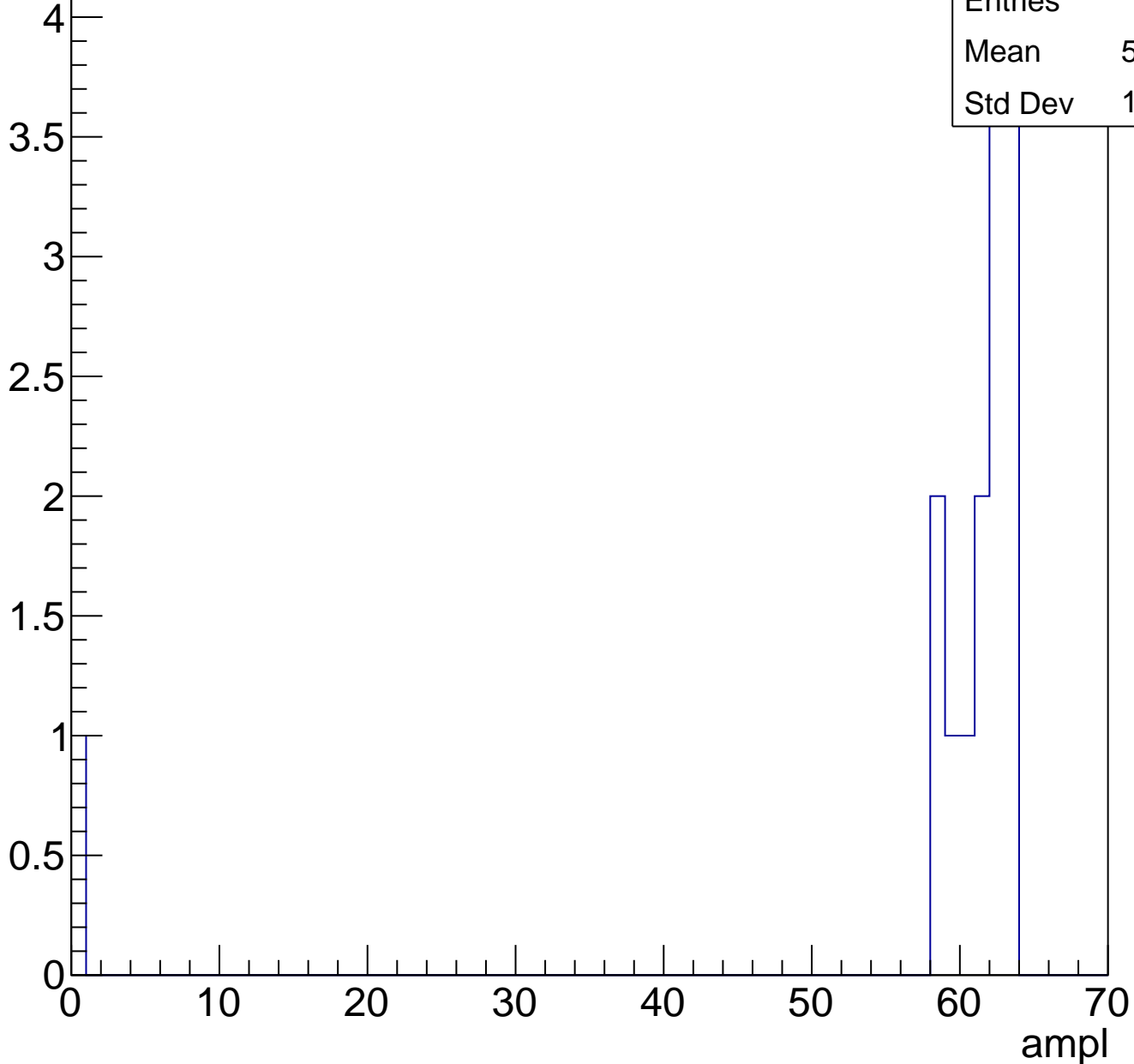
Entries	49
Mean	59.35
Std Dev	2.638



B1L103S, U11-ch84, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch84, adc7

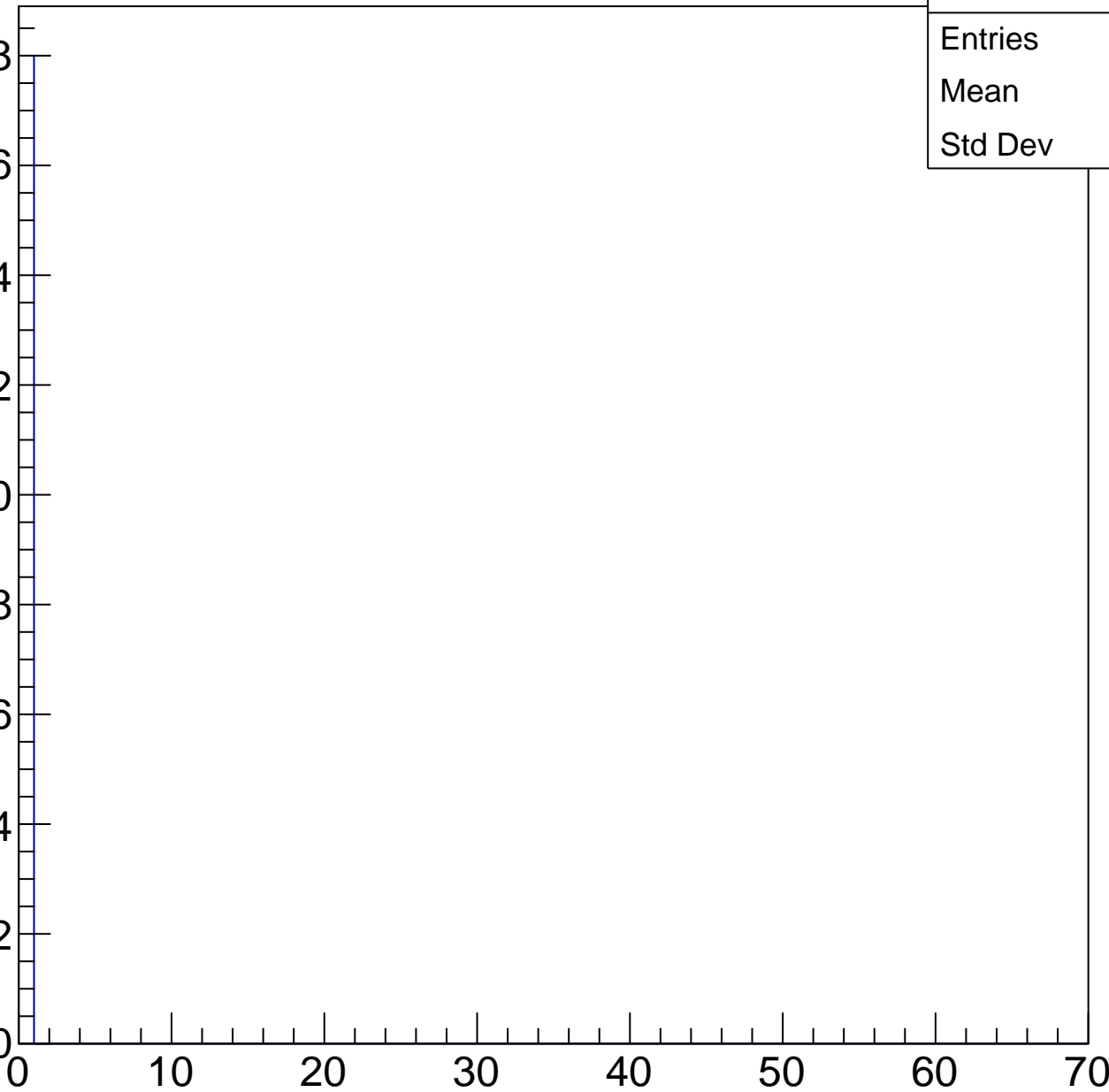
calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	18
Mean	0
Std Dev	0

ampl

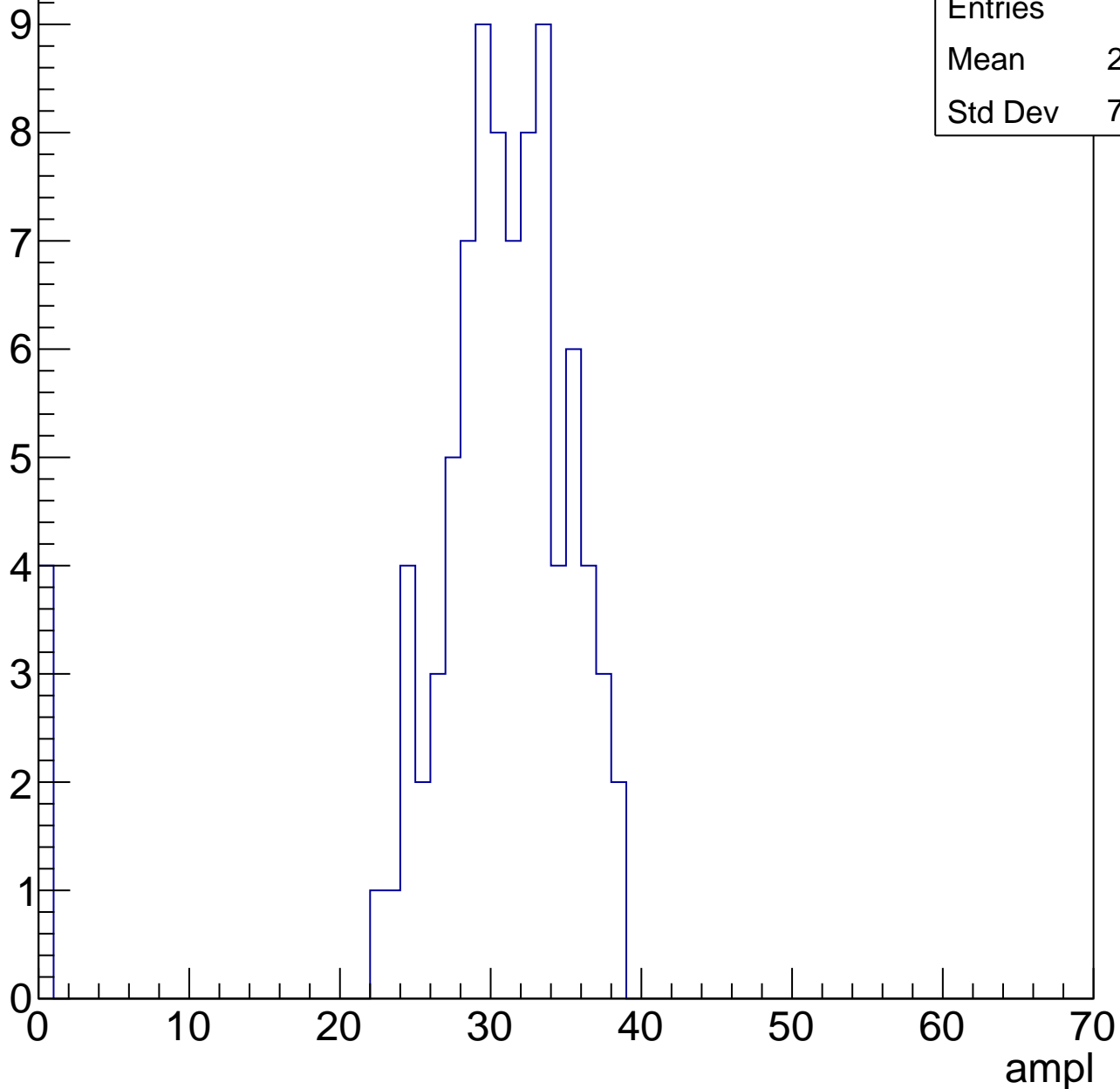


B1L103S, U11-ch85, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	87
Mean	29.29
Std Dev	7.386

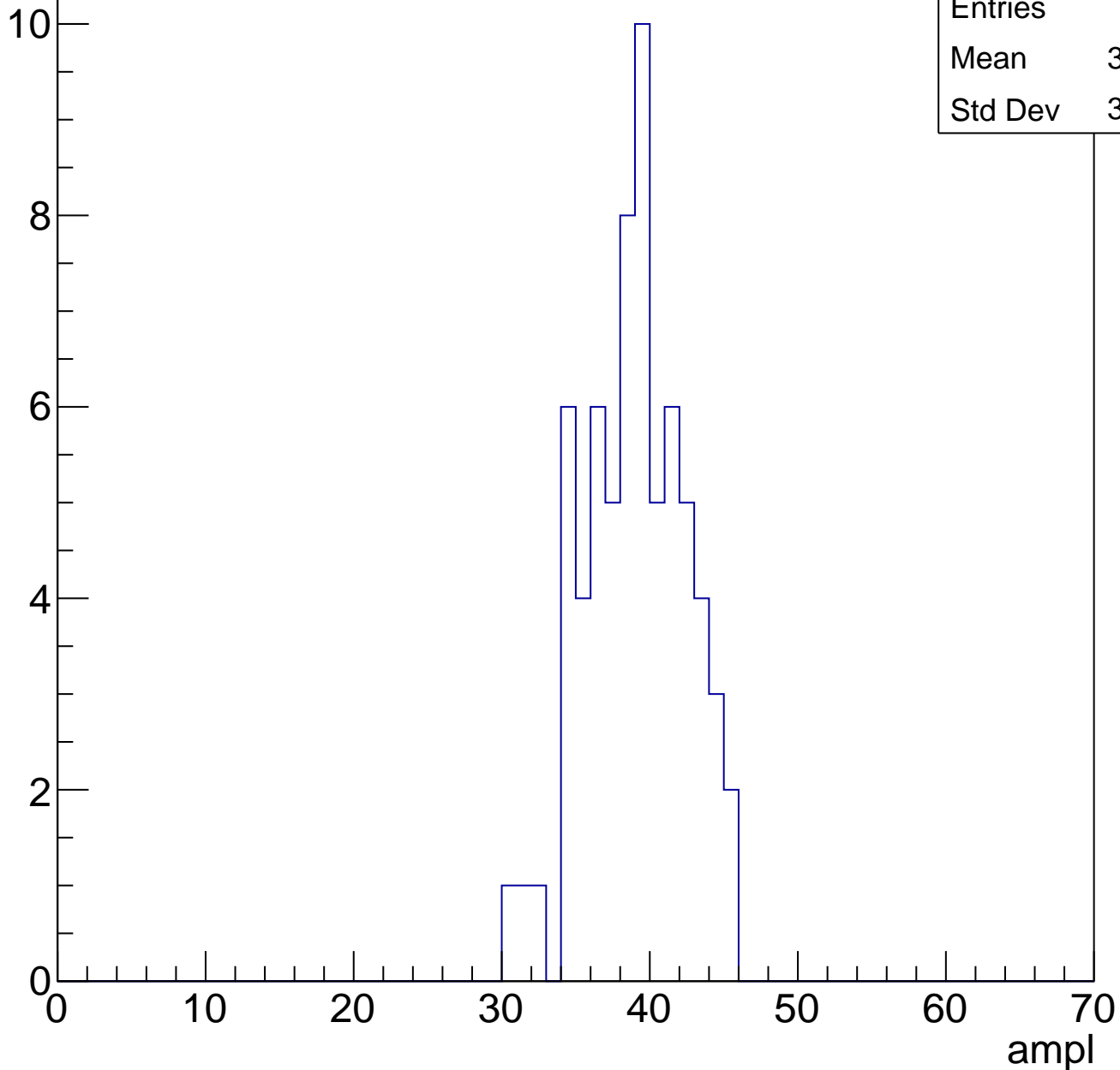


B1L103S, U11-ch85, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	67
Mean	38.54
Std Dev	3.369

Entry

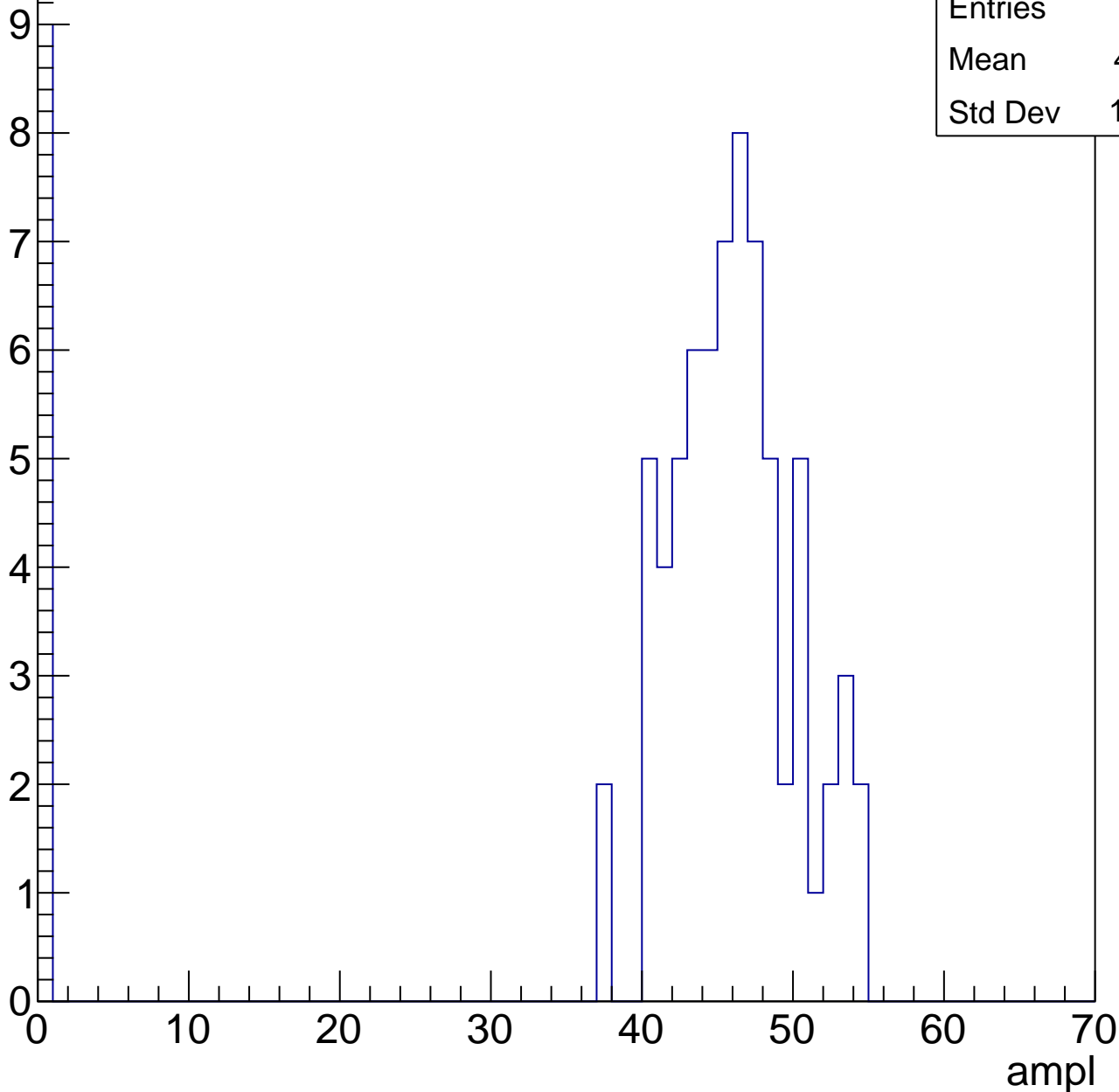


B1L103S, U11-ch85, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	79
Mean	40.41
Std Dev	14.96

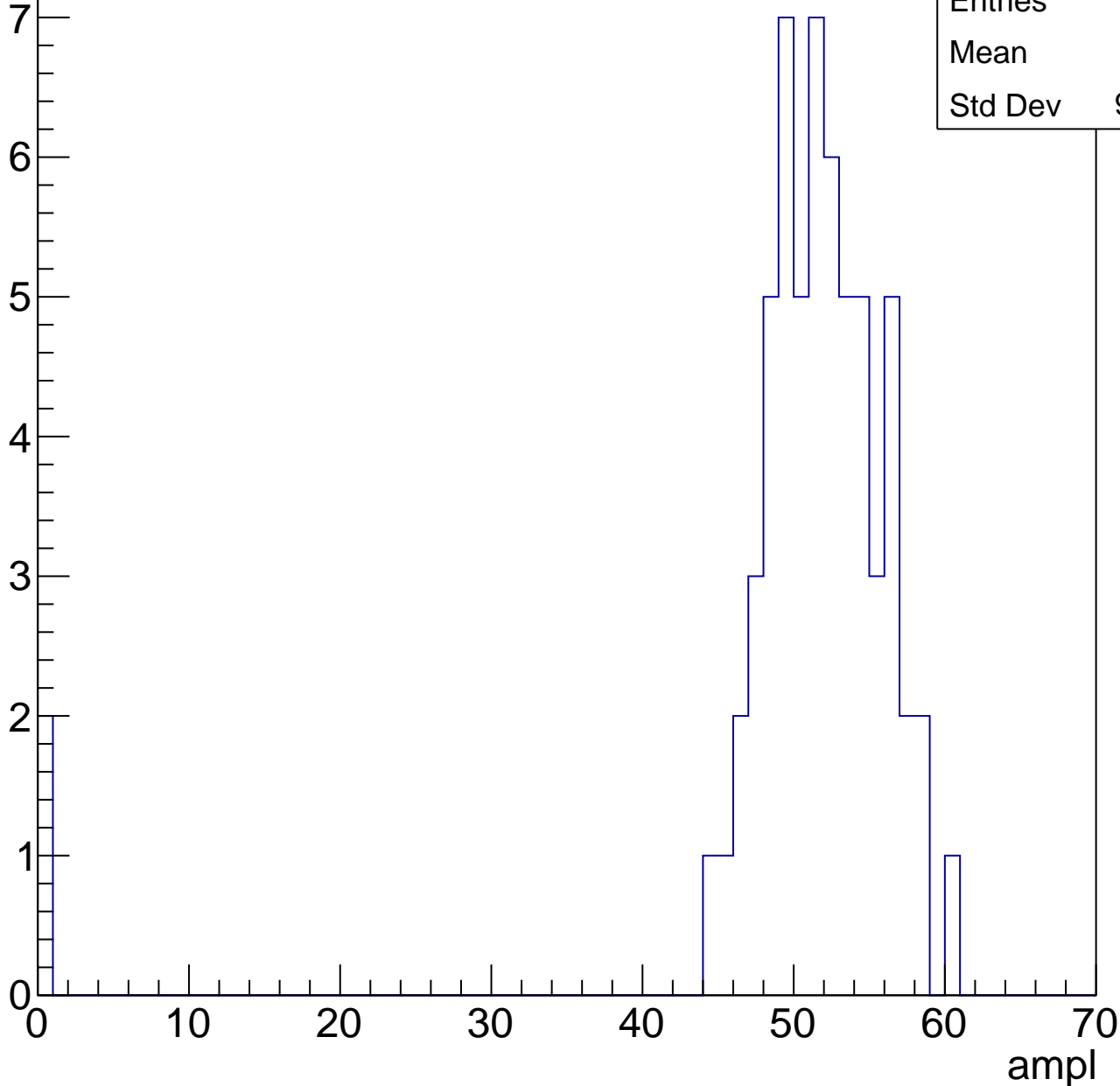


B1L103S, U11-ch85, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

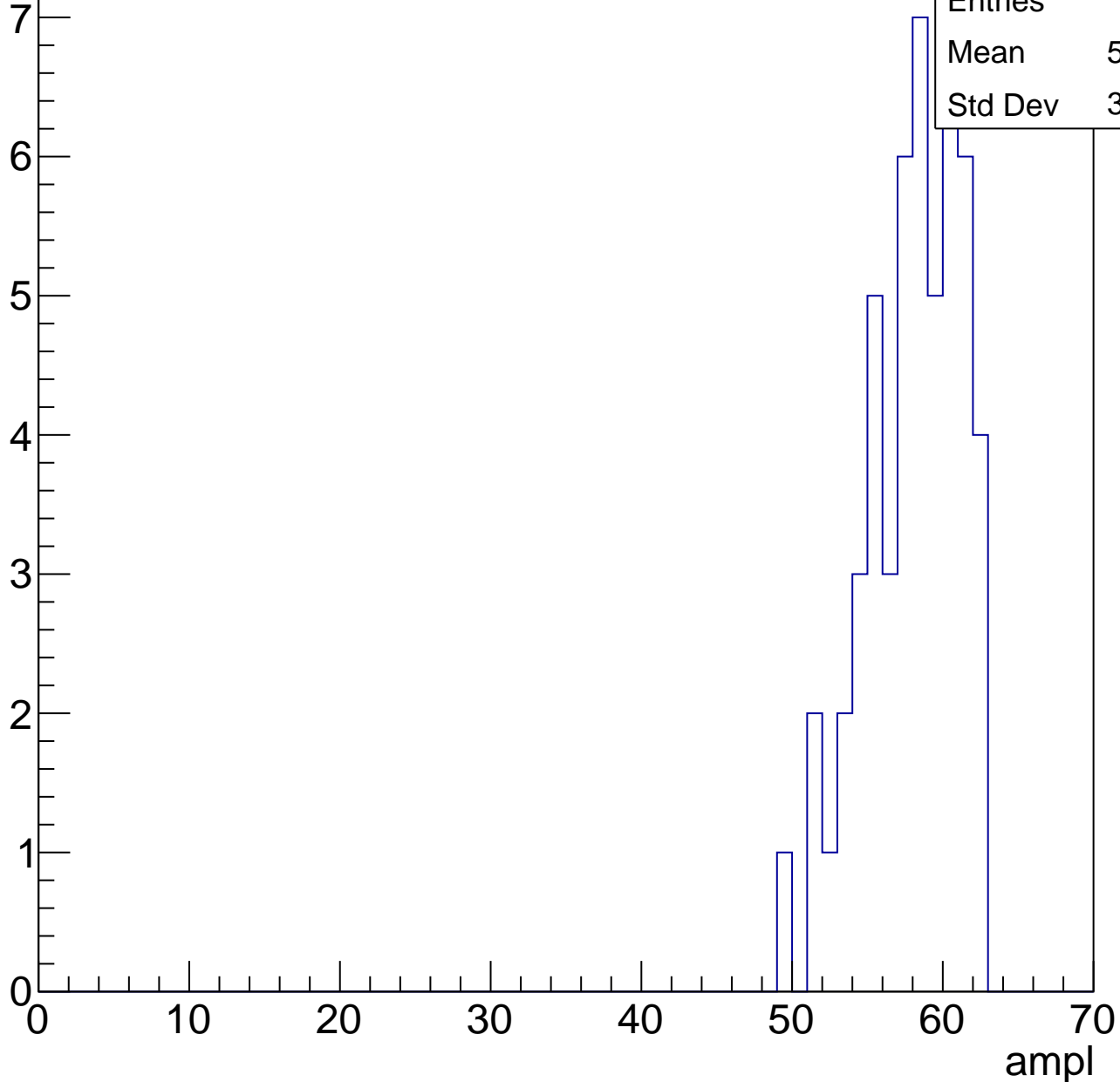
Entries	62
Mean	49.9
Std Dev	9.741



B1L103S, U11-ch85, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	52
Mean	57.52
Std Dev	3.147

B1L103S, U11-ch85, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entries	36
Mean	58.53
Std Dev	10.29

Entry

10

8

6

4

2

0

0

10

20

30

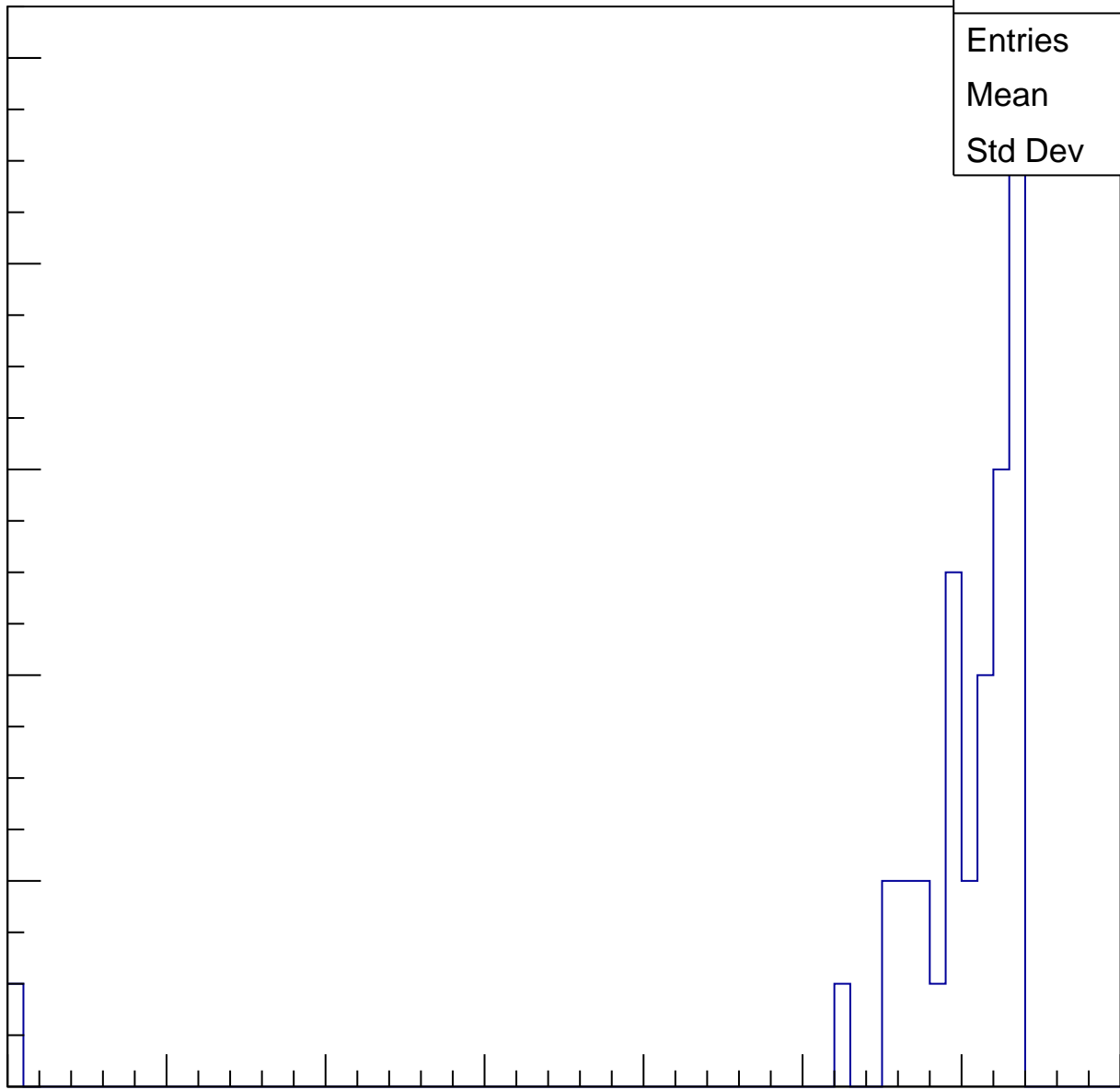
40

50

60

70

ampl



B1L103S, U11-ch85, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	0
Mean	0
Std Dev	0

B1L103S, U11-ch85, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	18
Mean	1.167
Std Dev	4.81

Entry

16
14
12
10
8
6
4
2
0

ampl

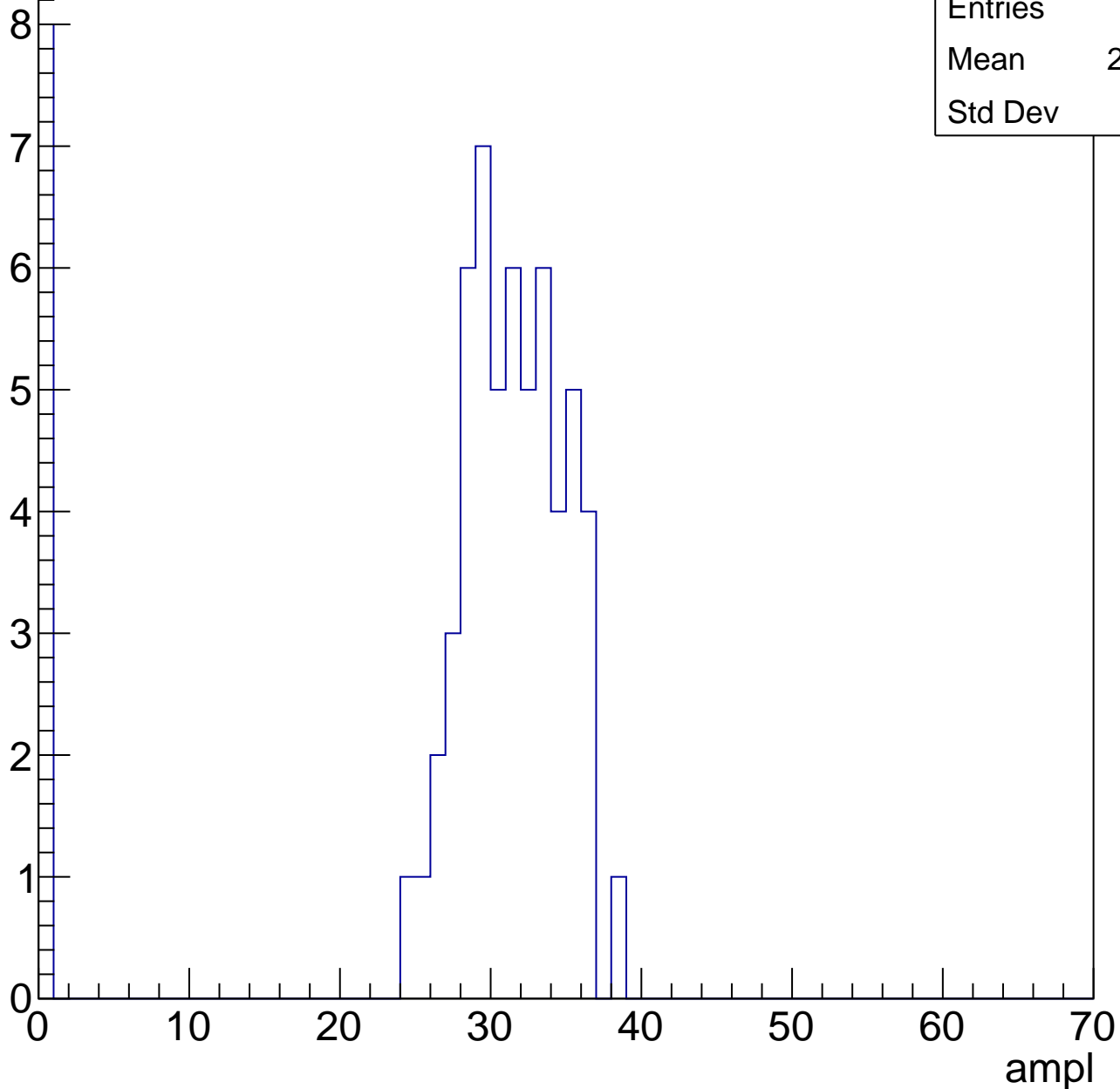
0 10 20 30 40 50 60 70

B1L103S, U11-ch86, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

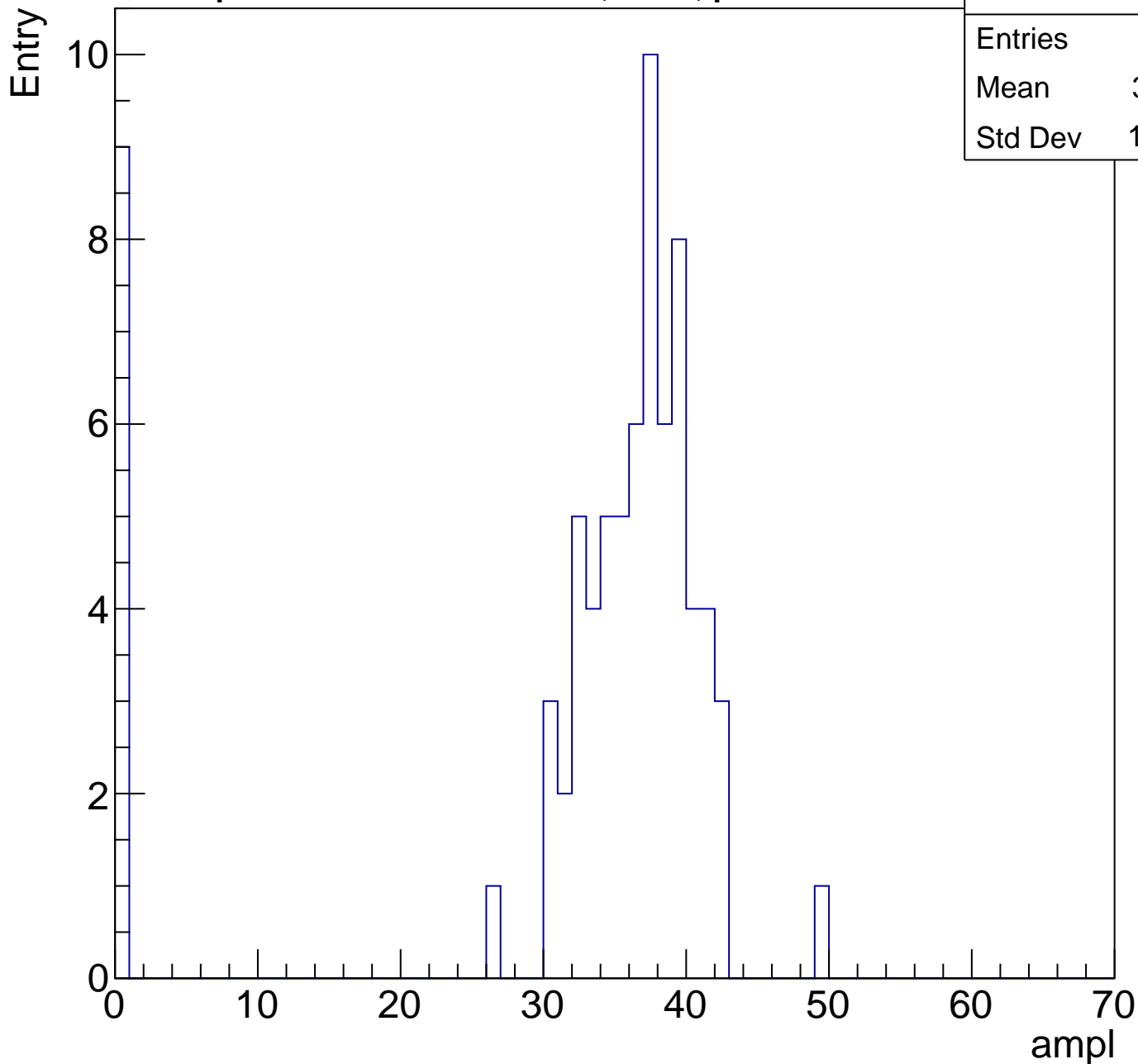
Entries	64
Mean	27.19
Std Dev	10.7



B1L103S, U11-ch86, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	76
Mean	32.11
Std Dev	12.28

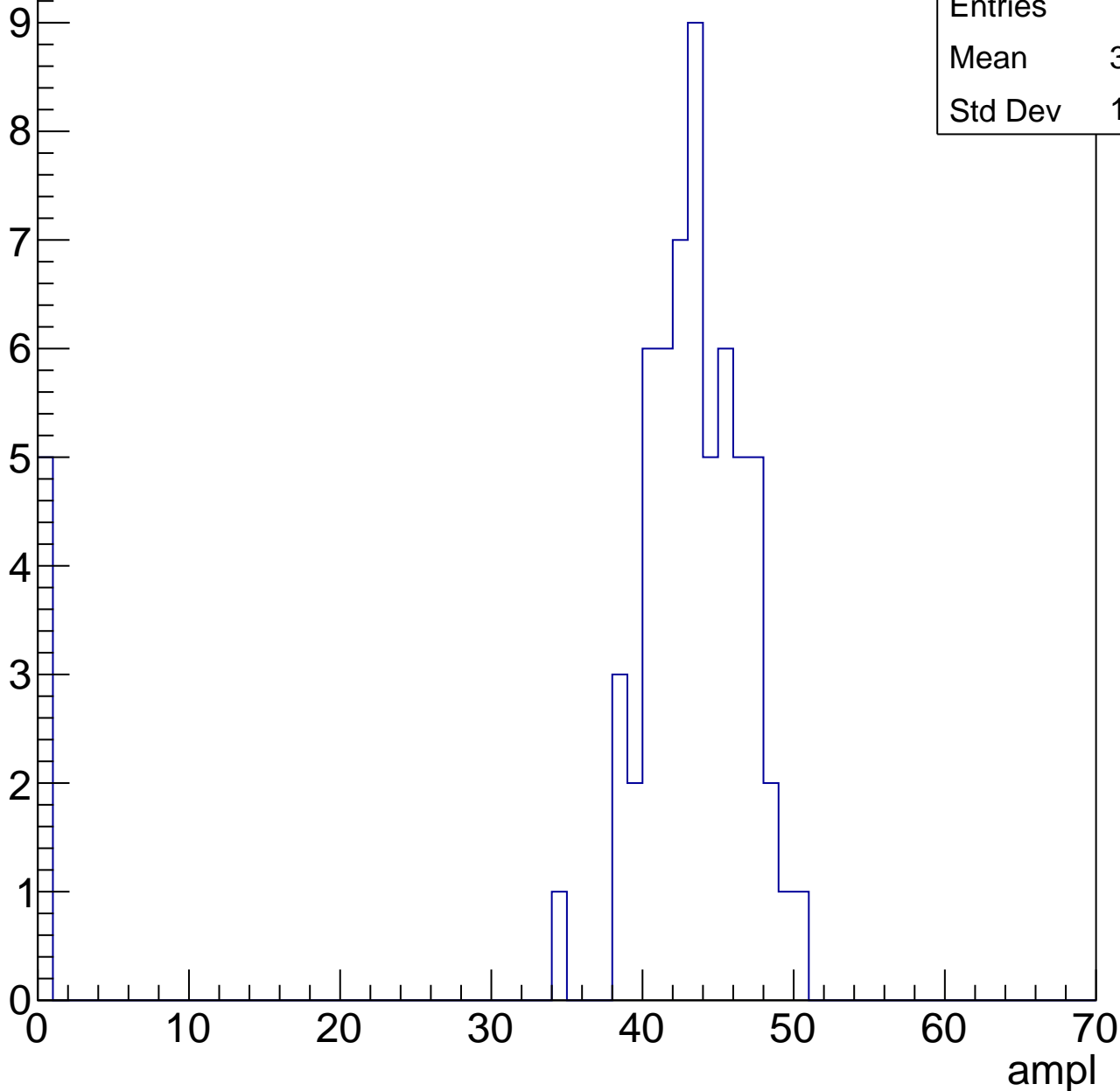


B1L103S, U11-ch86, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	39.73
Std Dev	11.94

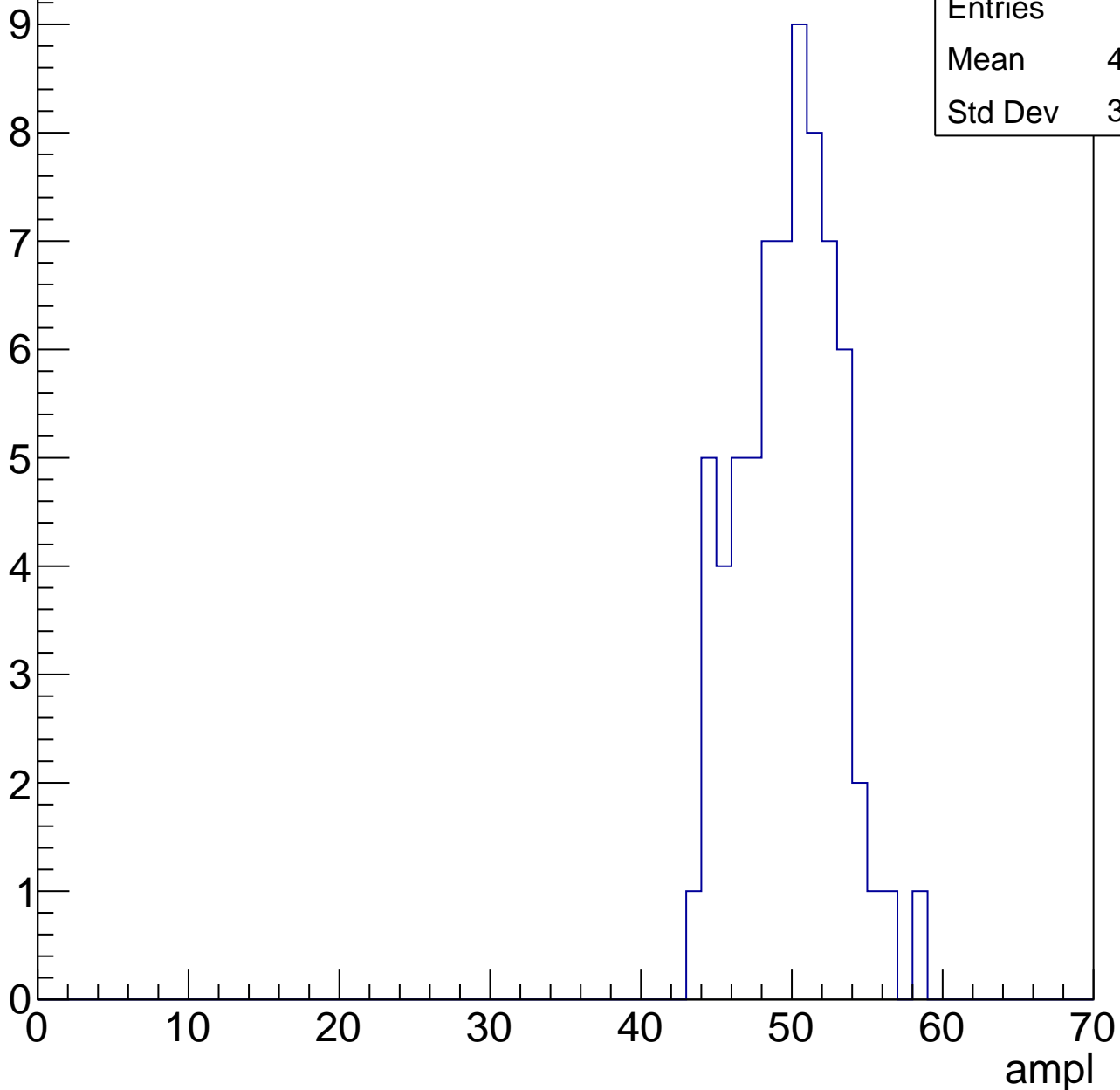


B1L103S, U11-ch86, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

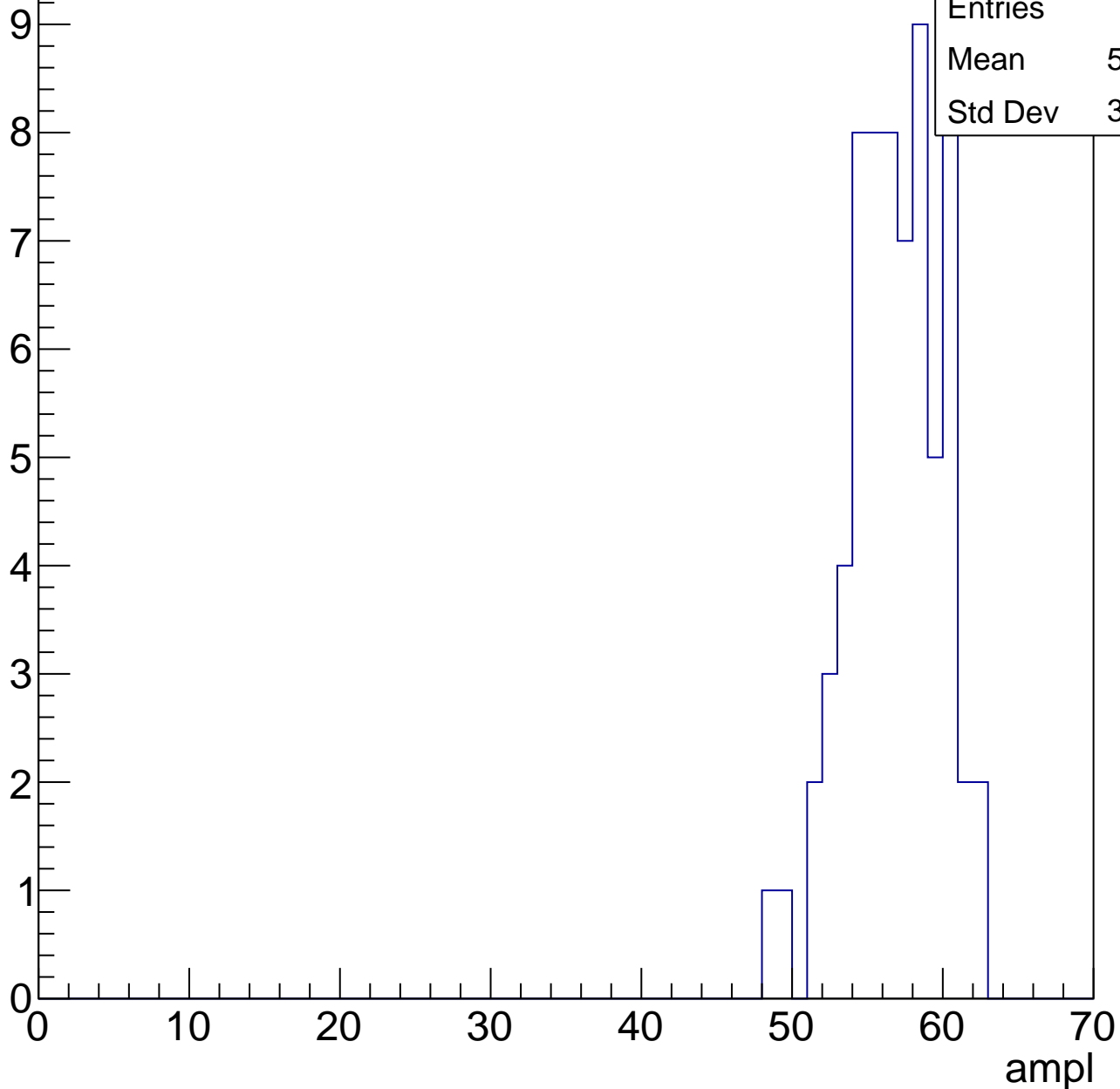
Entries	69
Mean	49.33
Std Dev	3.197



B1L103S, U11-ch86, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



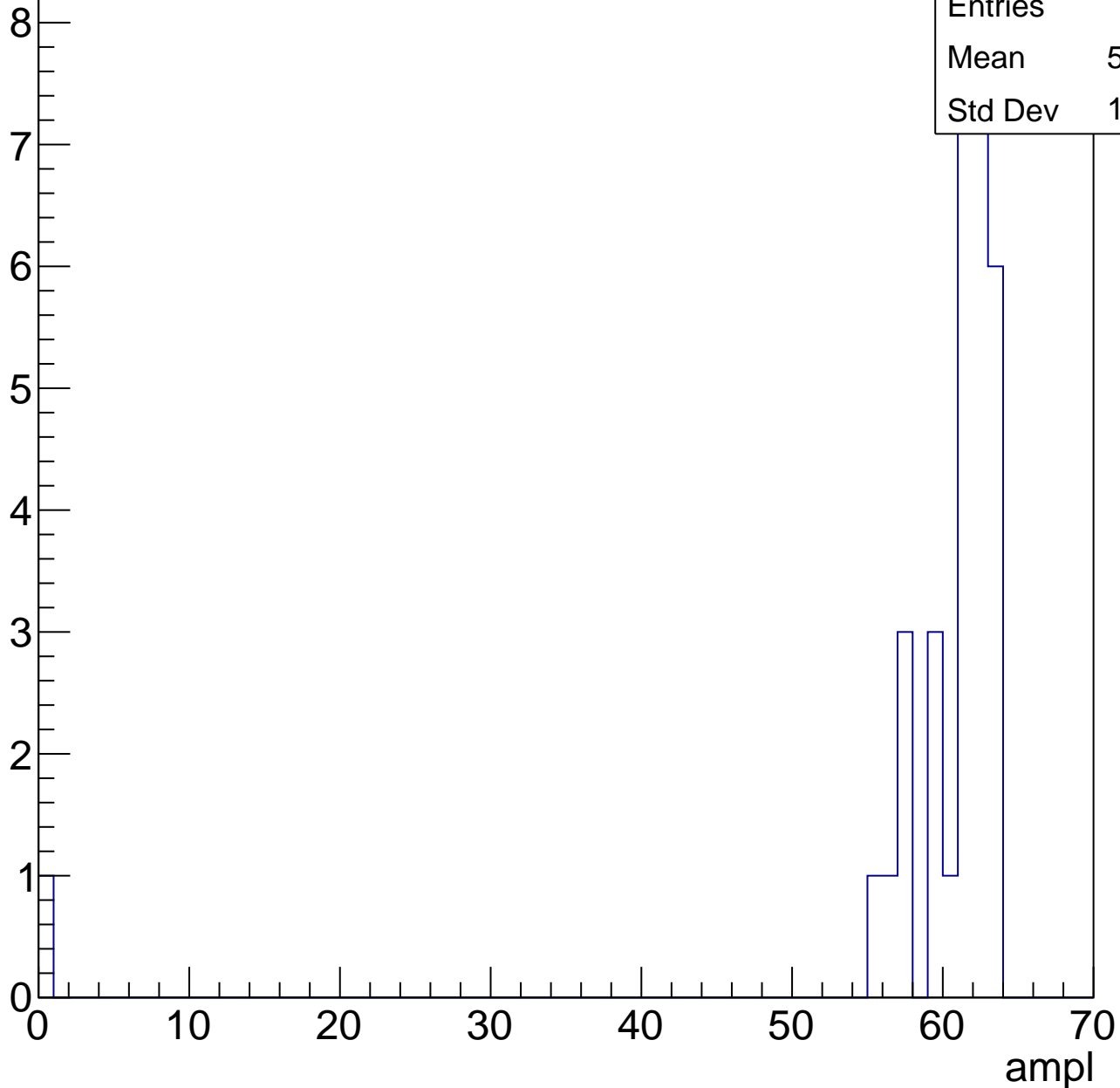
Entries	69
Mean	56.36
Std Dev	3.026

B1L103S, U11-ch86, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

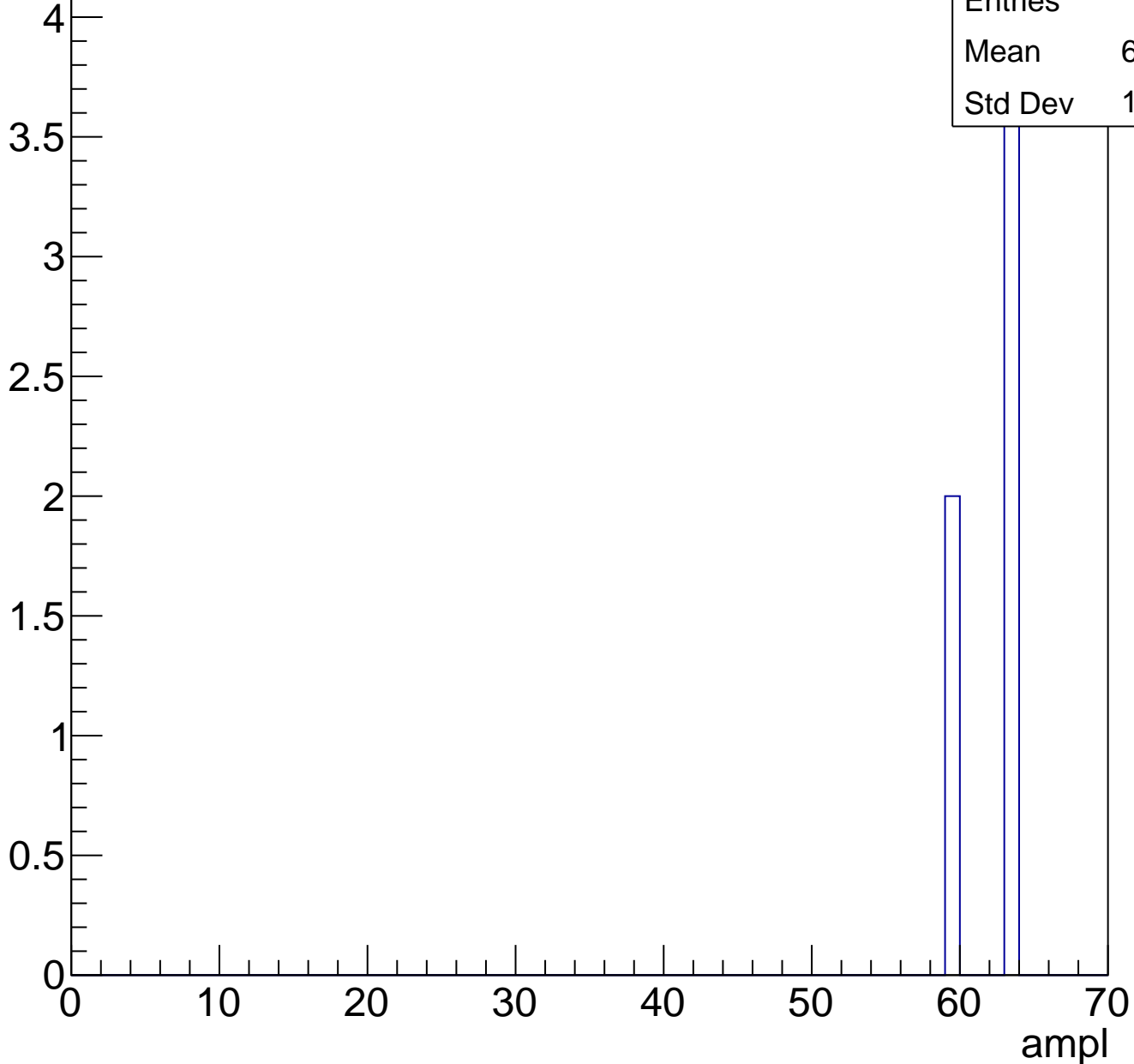
Entries	32
Mean	58.78
Std Dev	10.78



B1L103S, U11-ch86, adc6

calib_packv5_041523_1651.root, FC#0, port C2

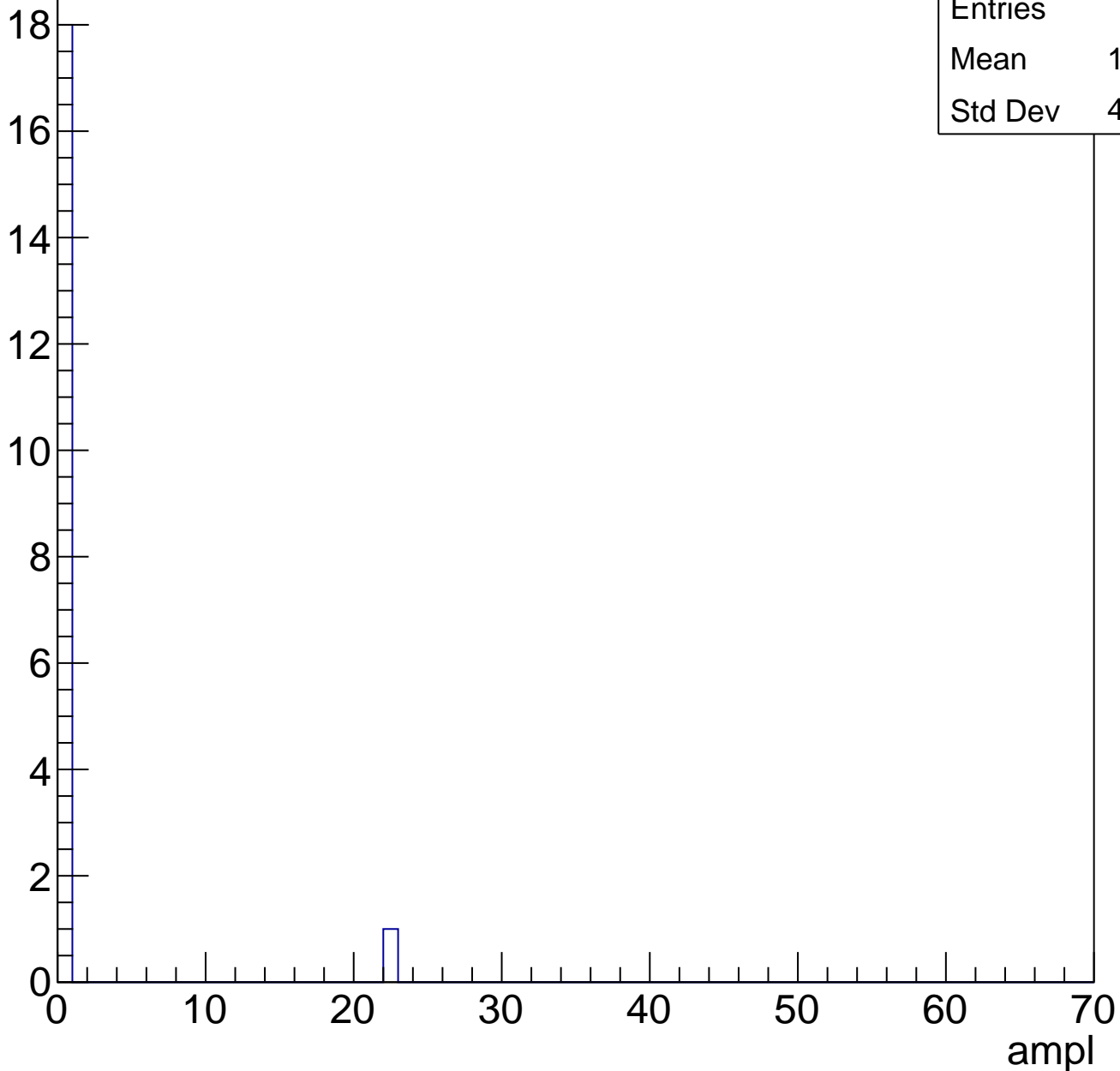
Entry



B1L103S, U11-ch86, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

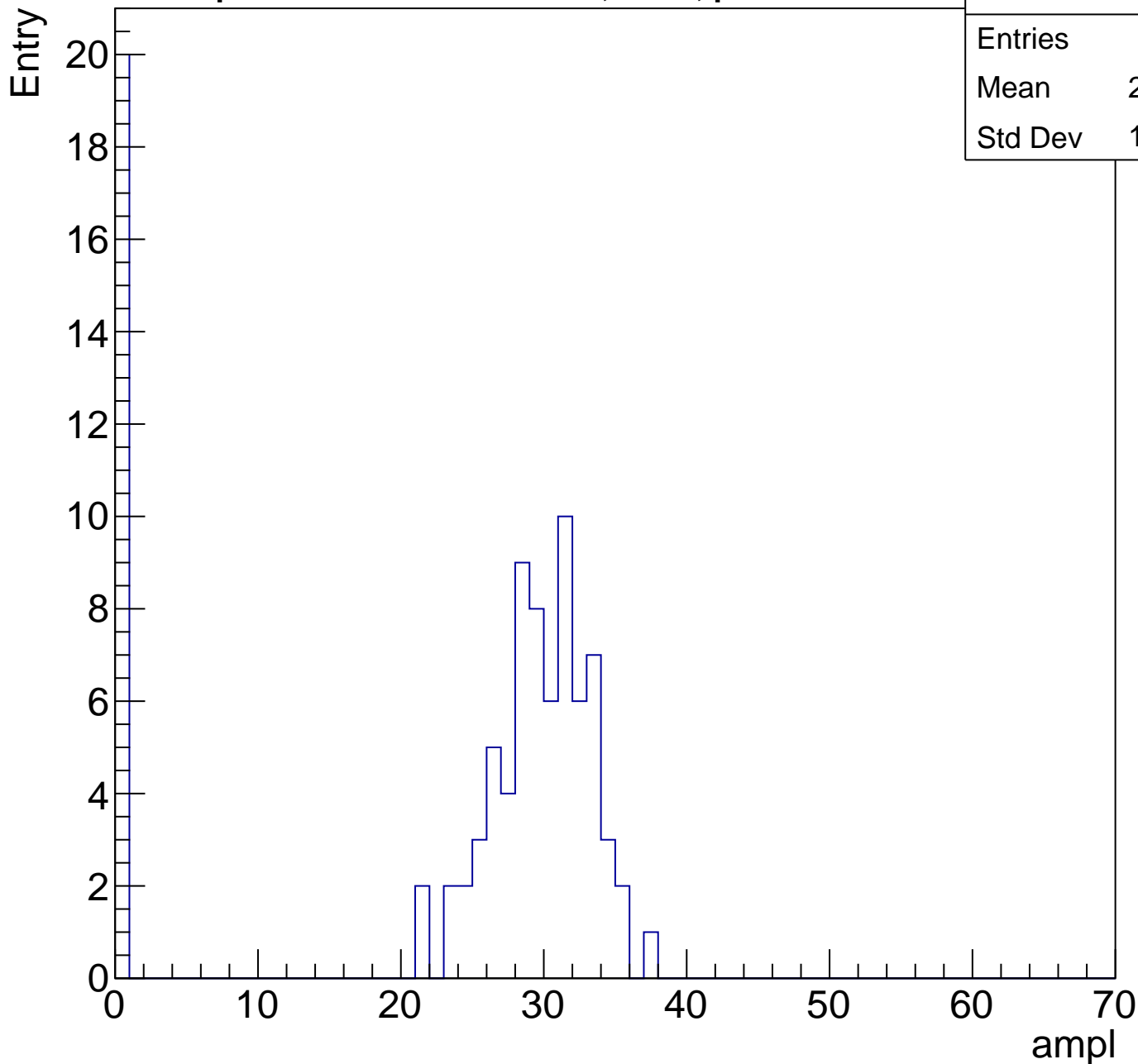


Entries	19
Mean	1.158
Std Dev	4.913

B1L103S, U11-ch87, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	90
Mean	22.83
Std Dev	12.56



B1L103S, U11-ch87, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	91
Mean	32.74
Std Dev	12.53

Entry

10

8

6

4

2

0

ampl

0

10

20

30

40

50

60

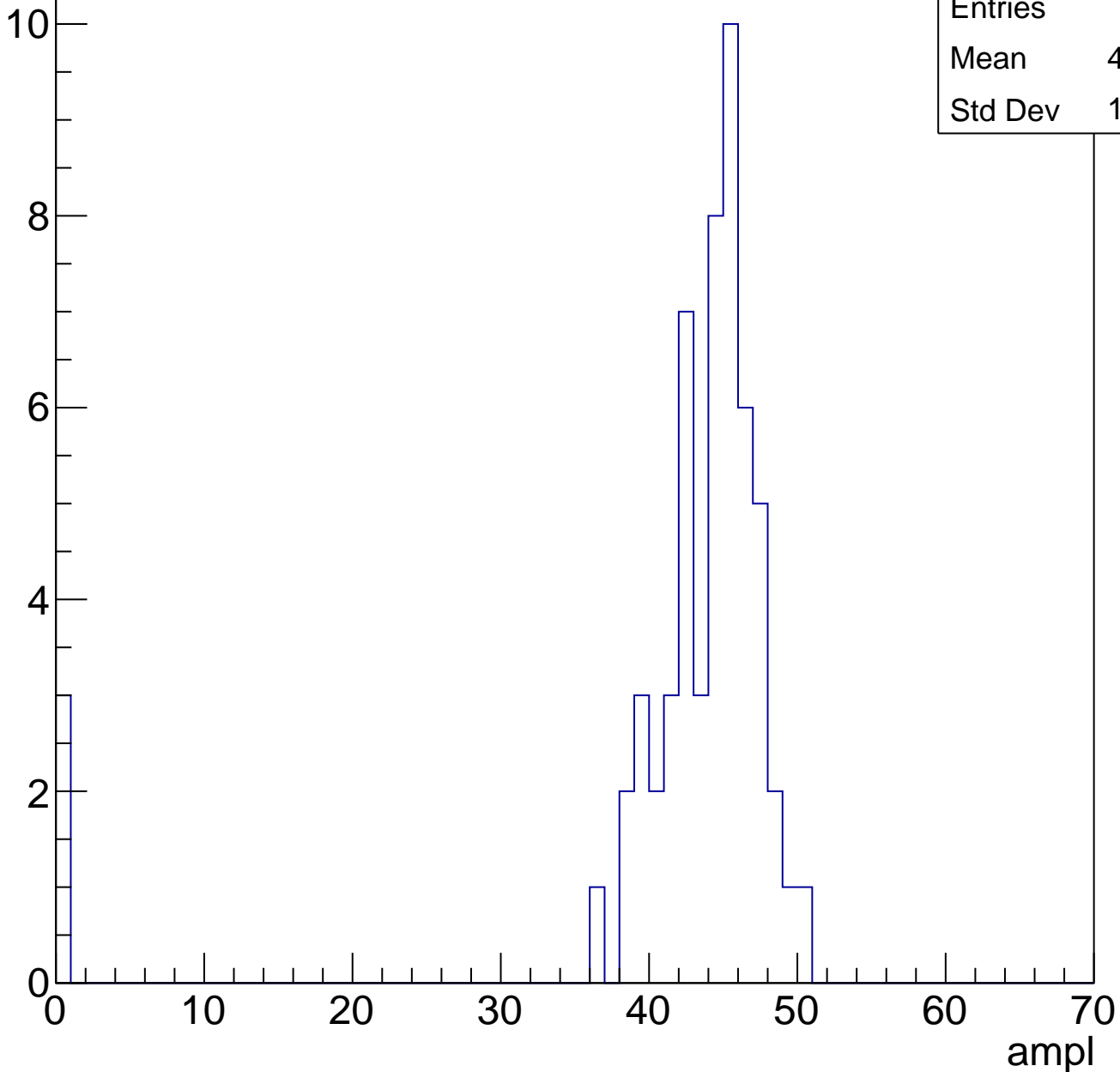
70

B1L103S, U11-ch87, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	57
Mean	41.46
Std Dev	10.18

Entry

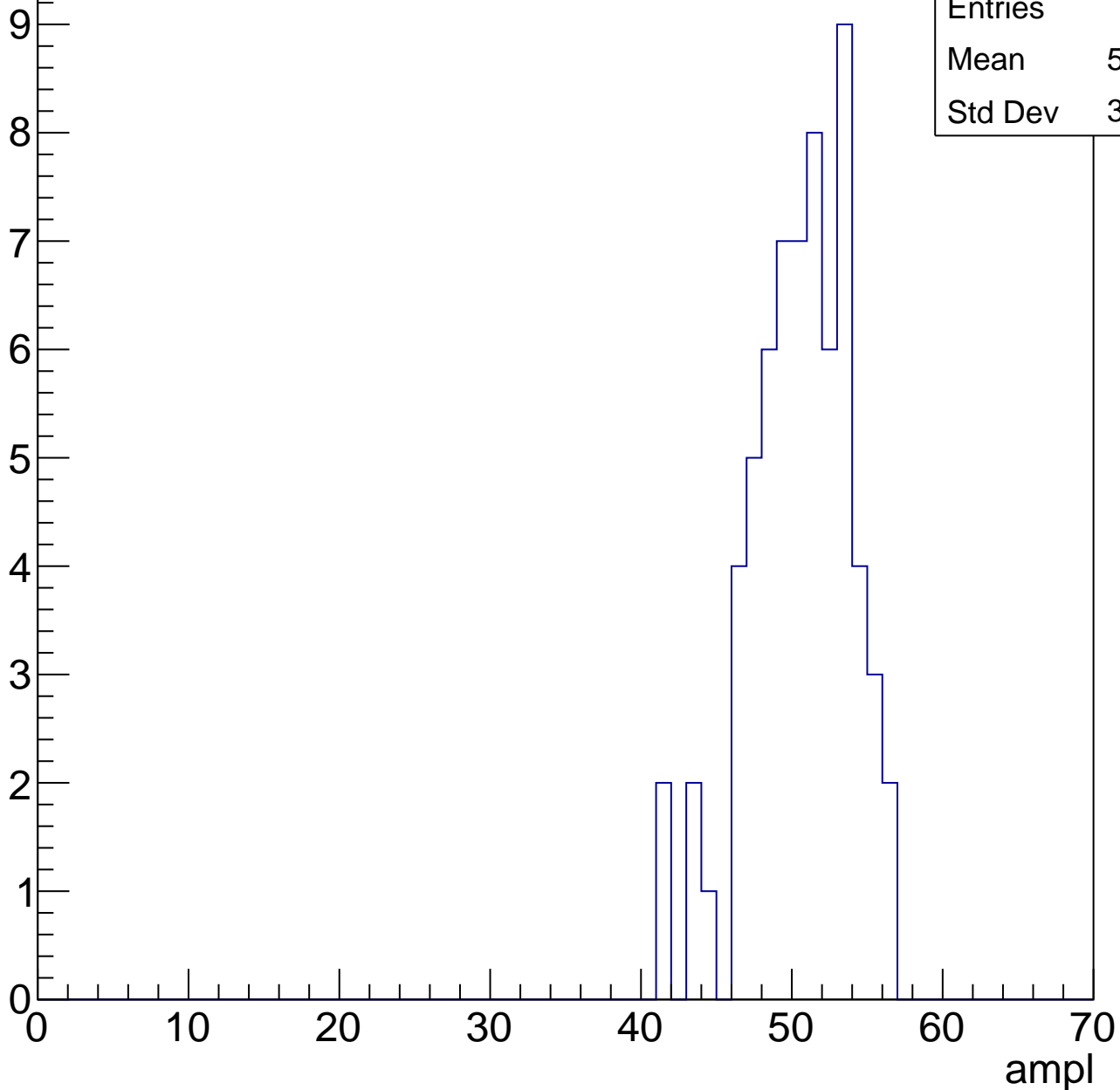


B1L103S, U11-ch87, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	50.03
Std Dev	3.393

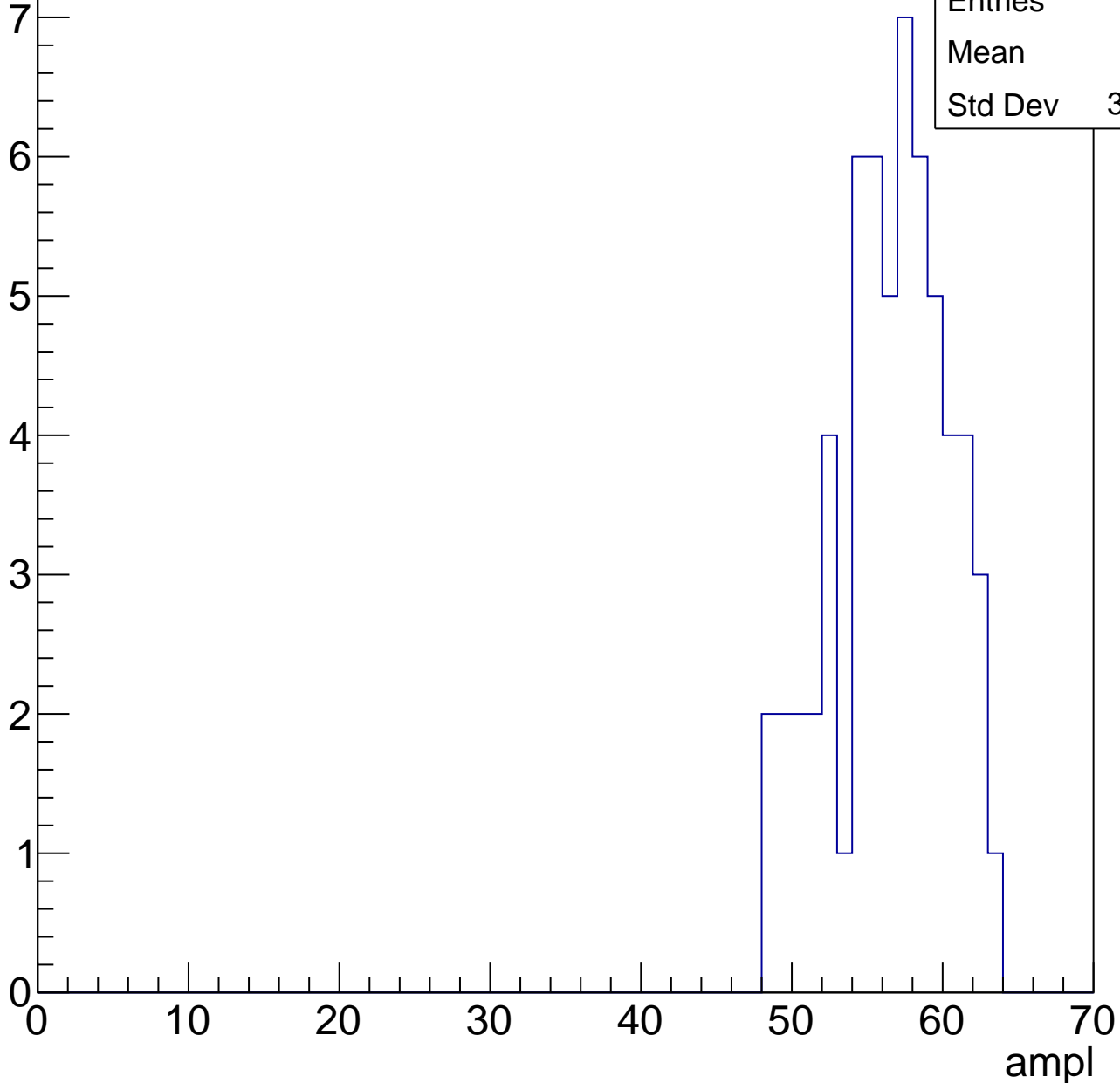


B1L103S, U11-ch87, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	56.1
Std Dev	3.758

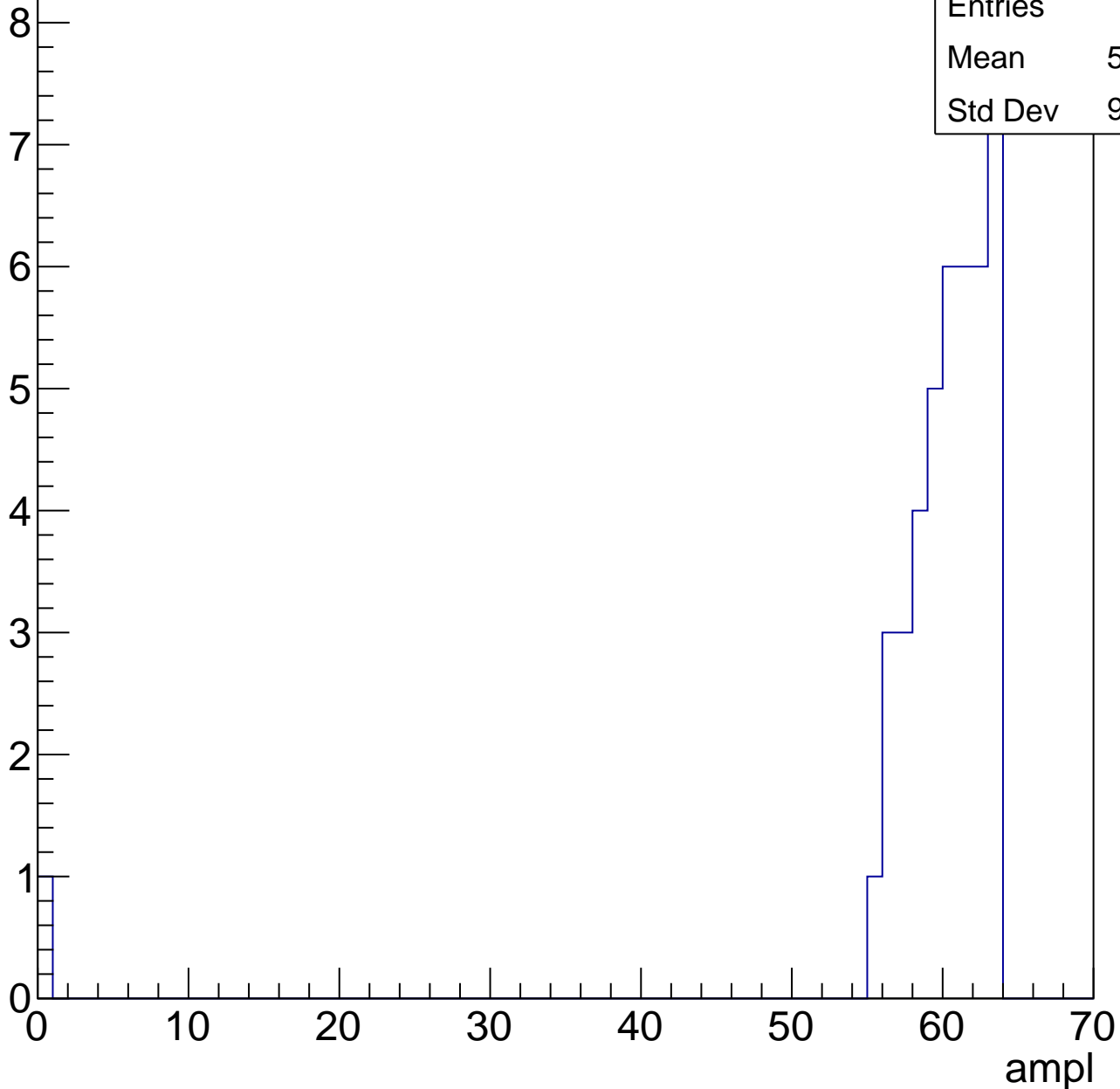


B1L103S, U11-ch87, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	43
Mean	58.67
Std Dev	9.335



B1L103S, U11-ch87, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch87, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

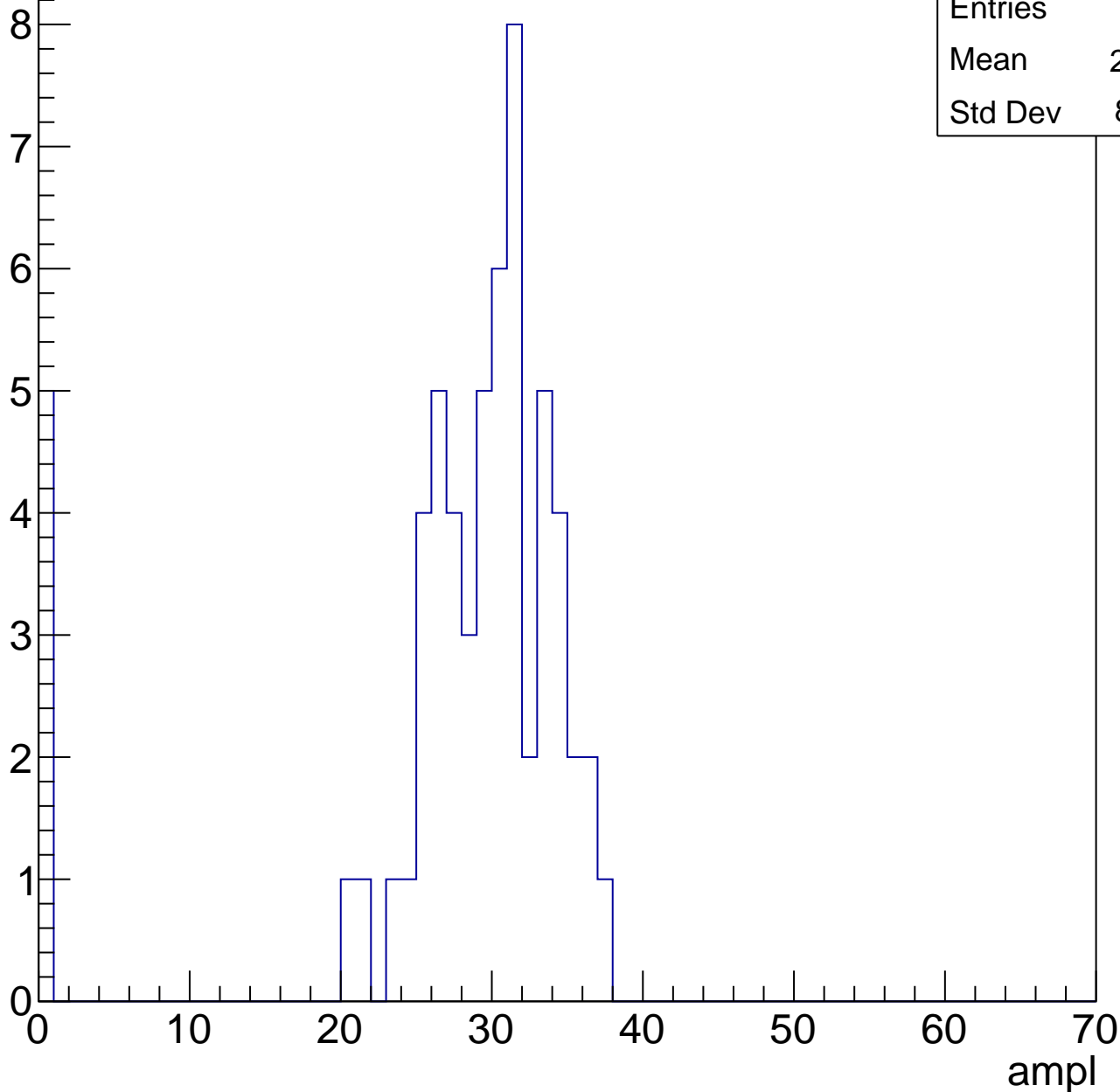
ampl

B1L103S, U11-ch88, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	27.12
Std Dev	8.941

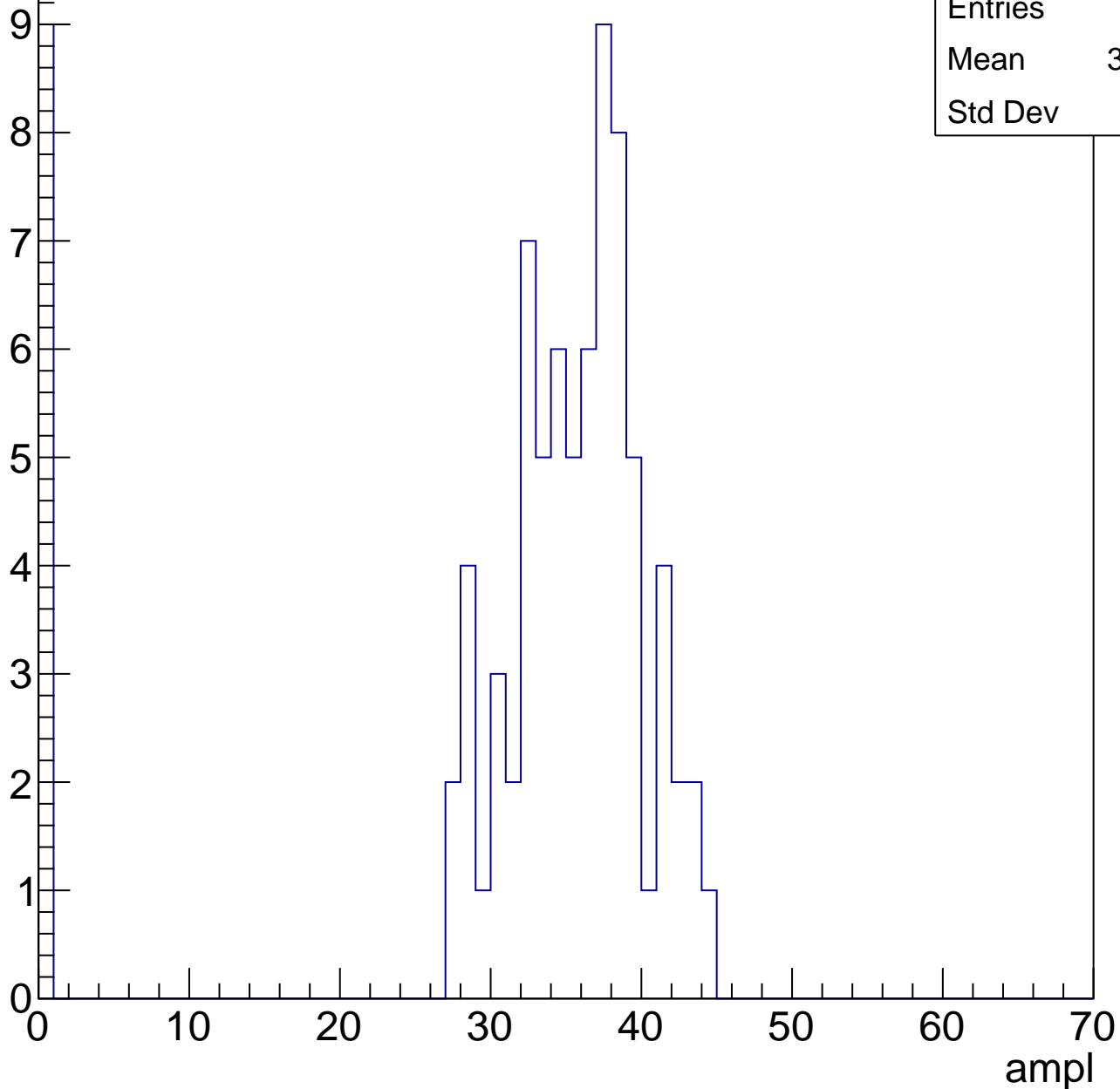


B1L103S, U11-ch88, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	82
Mean	31.48
Std Dev	11.7

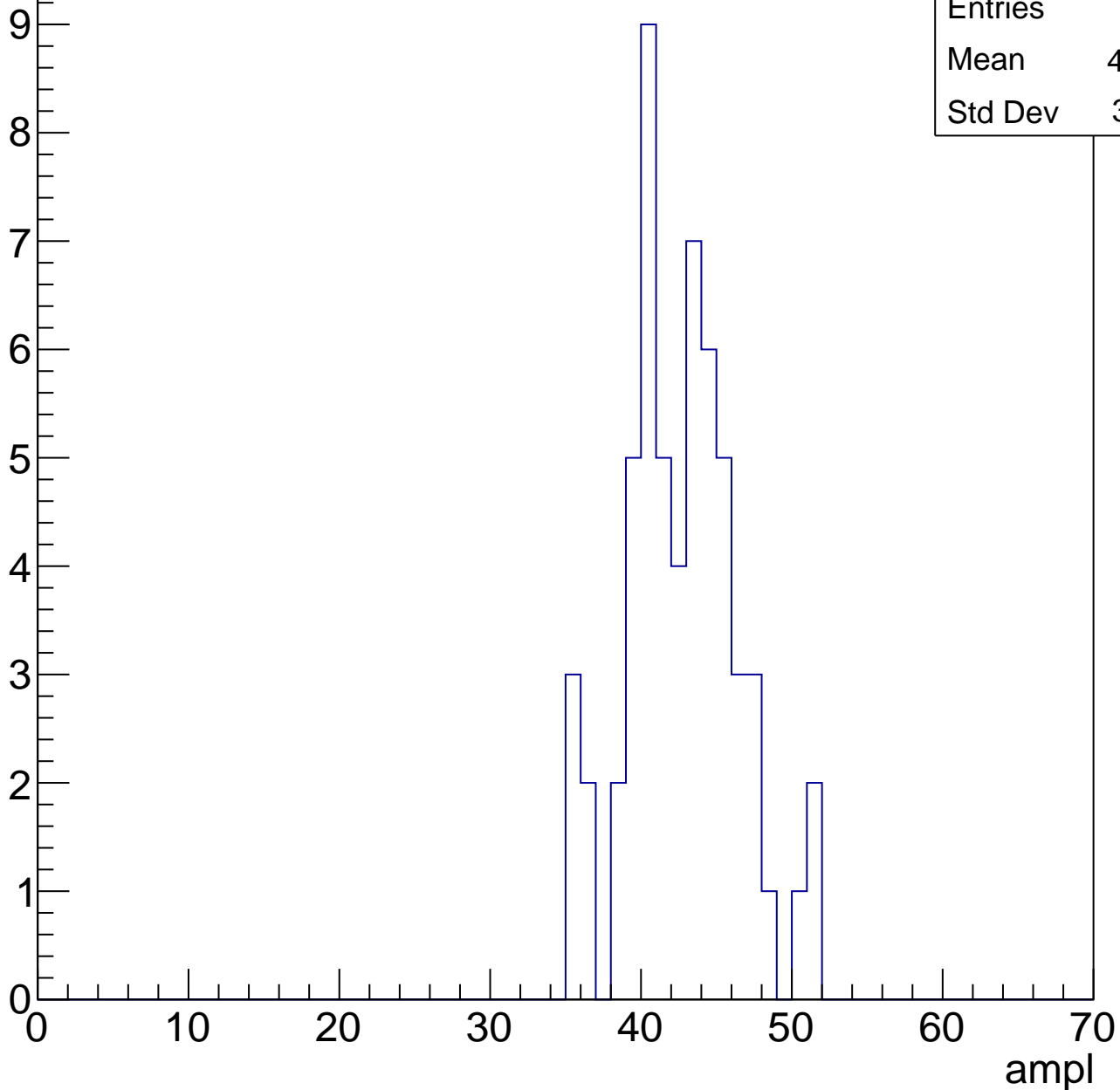


B1L103S, U11-ch88, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	42.24
Std Dev	3.701

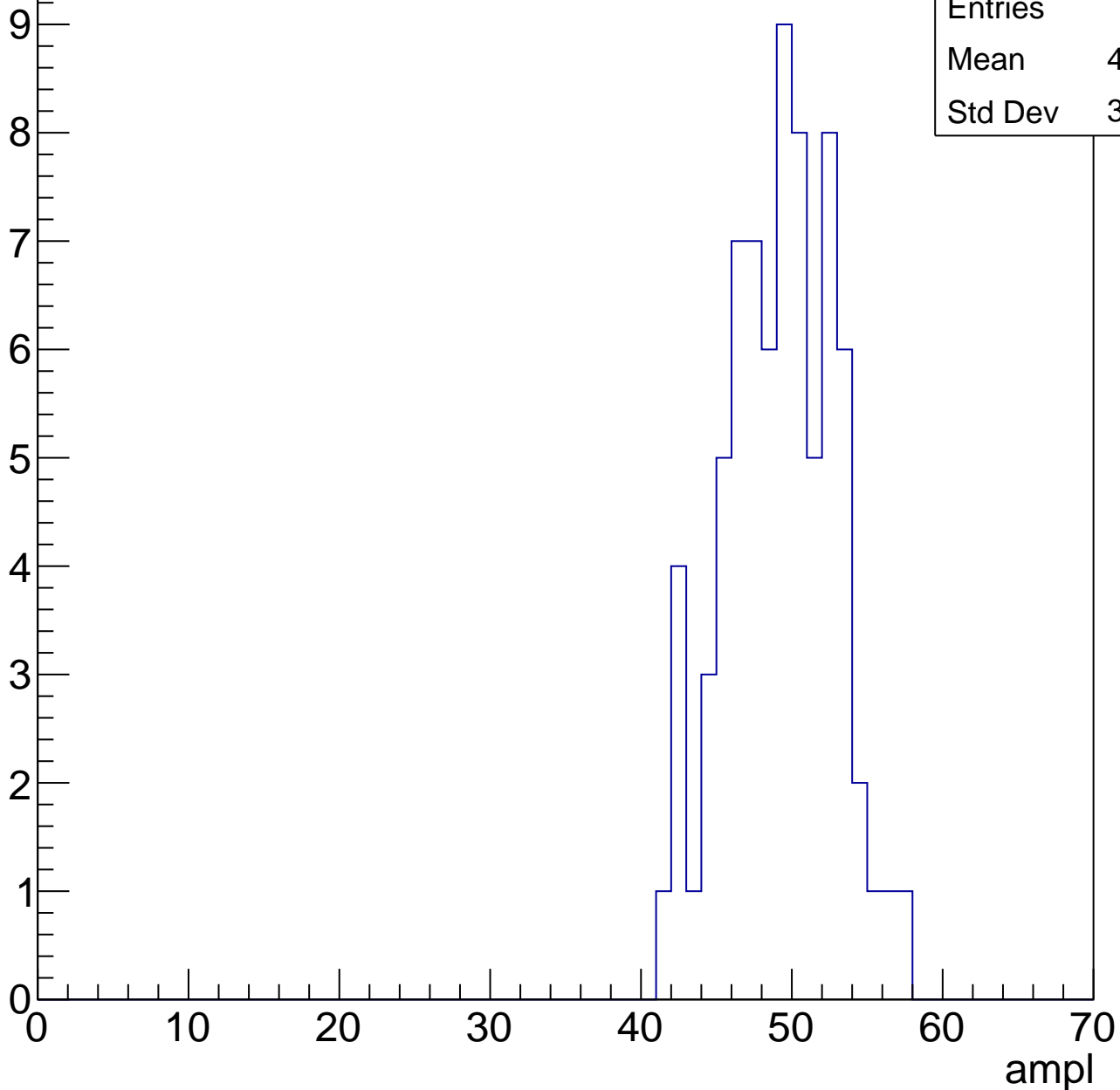


B1L103S, U11-ch88, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	48.72
Std Dev	3.535

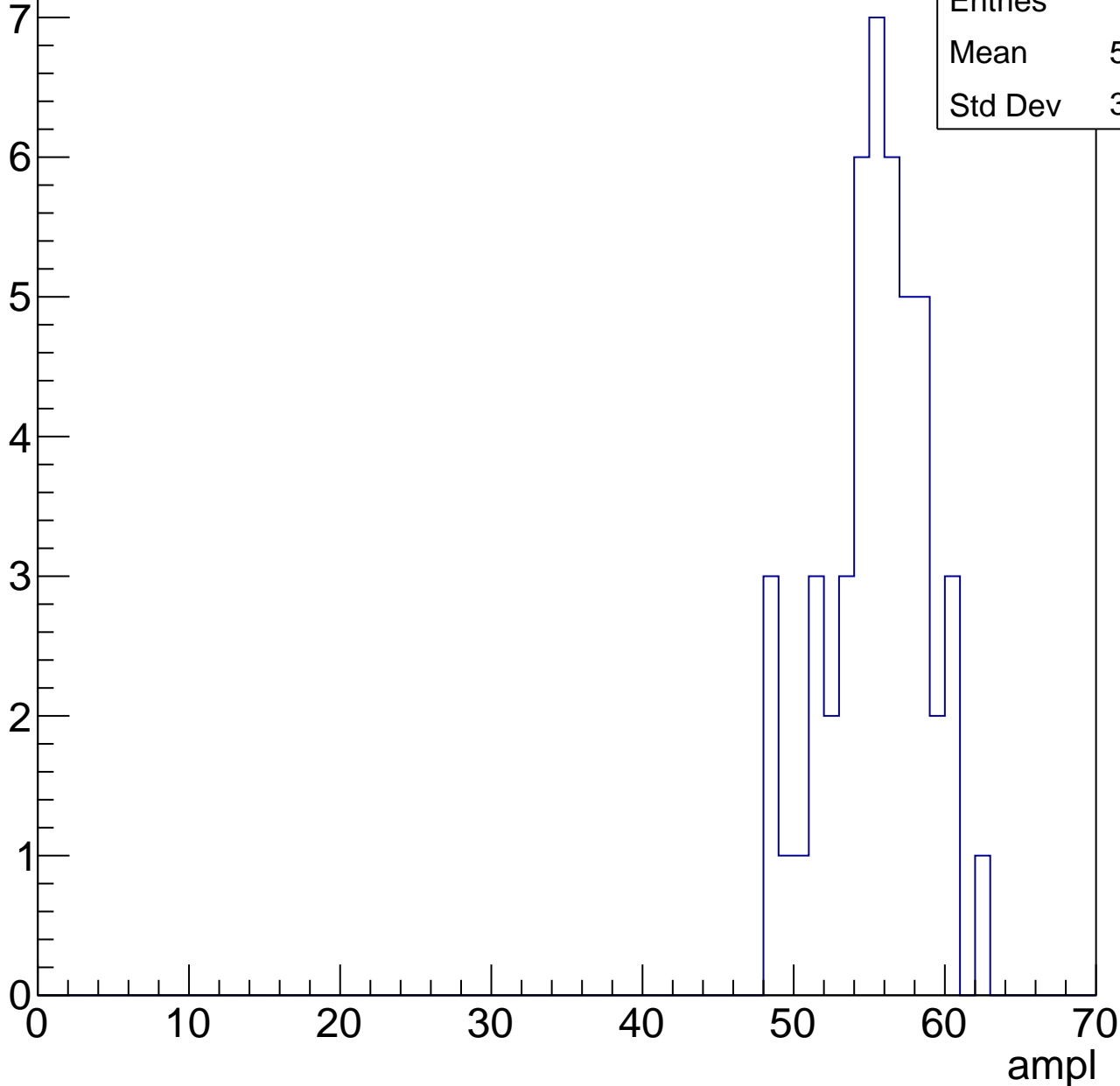


B1L103S, U11-ch88, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

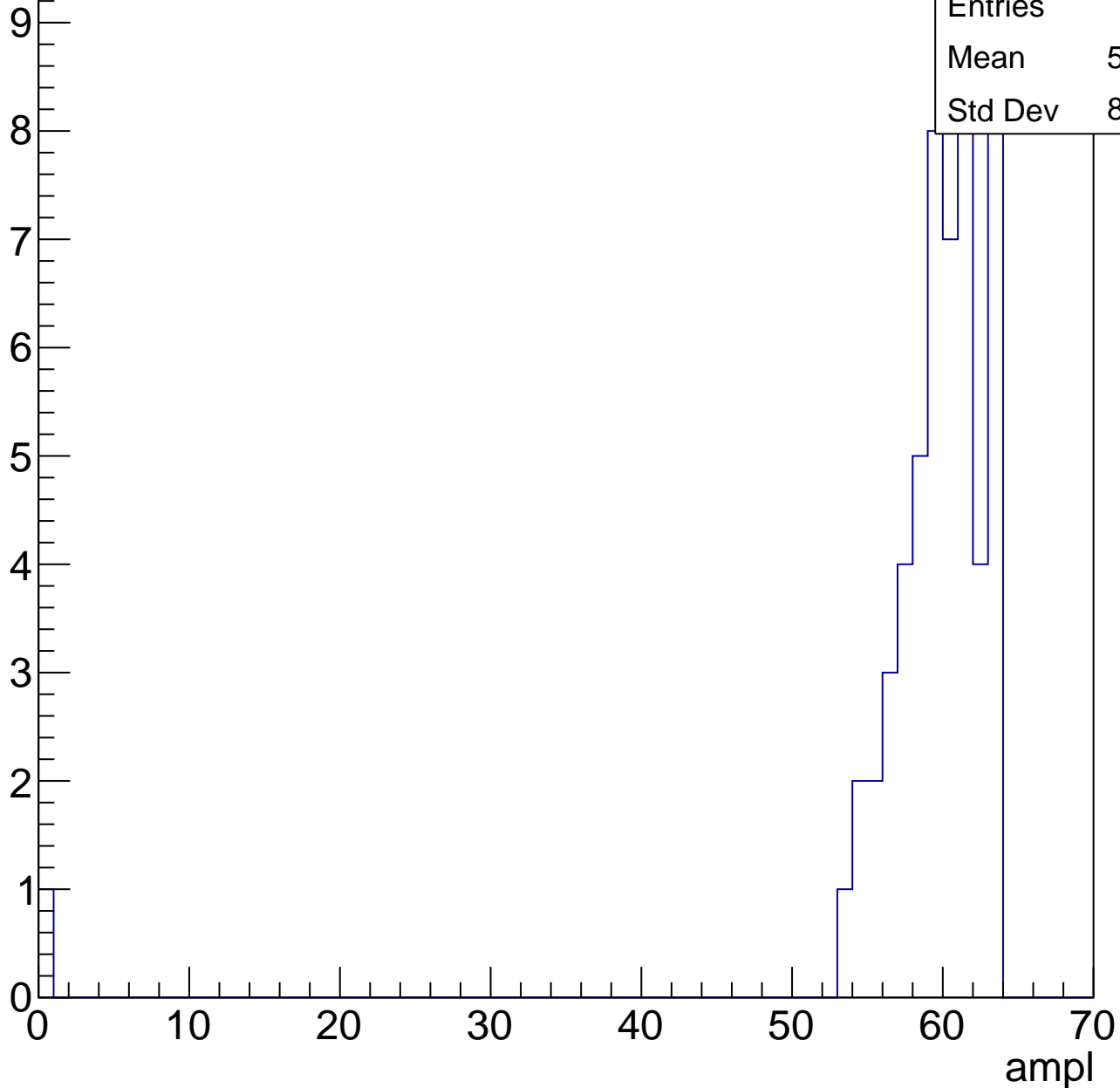
Entries	48
Mean	54.98
Std Dev	3.288



B1L103S, U11-ch88, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



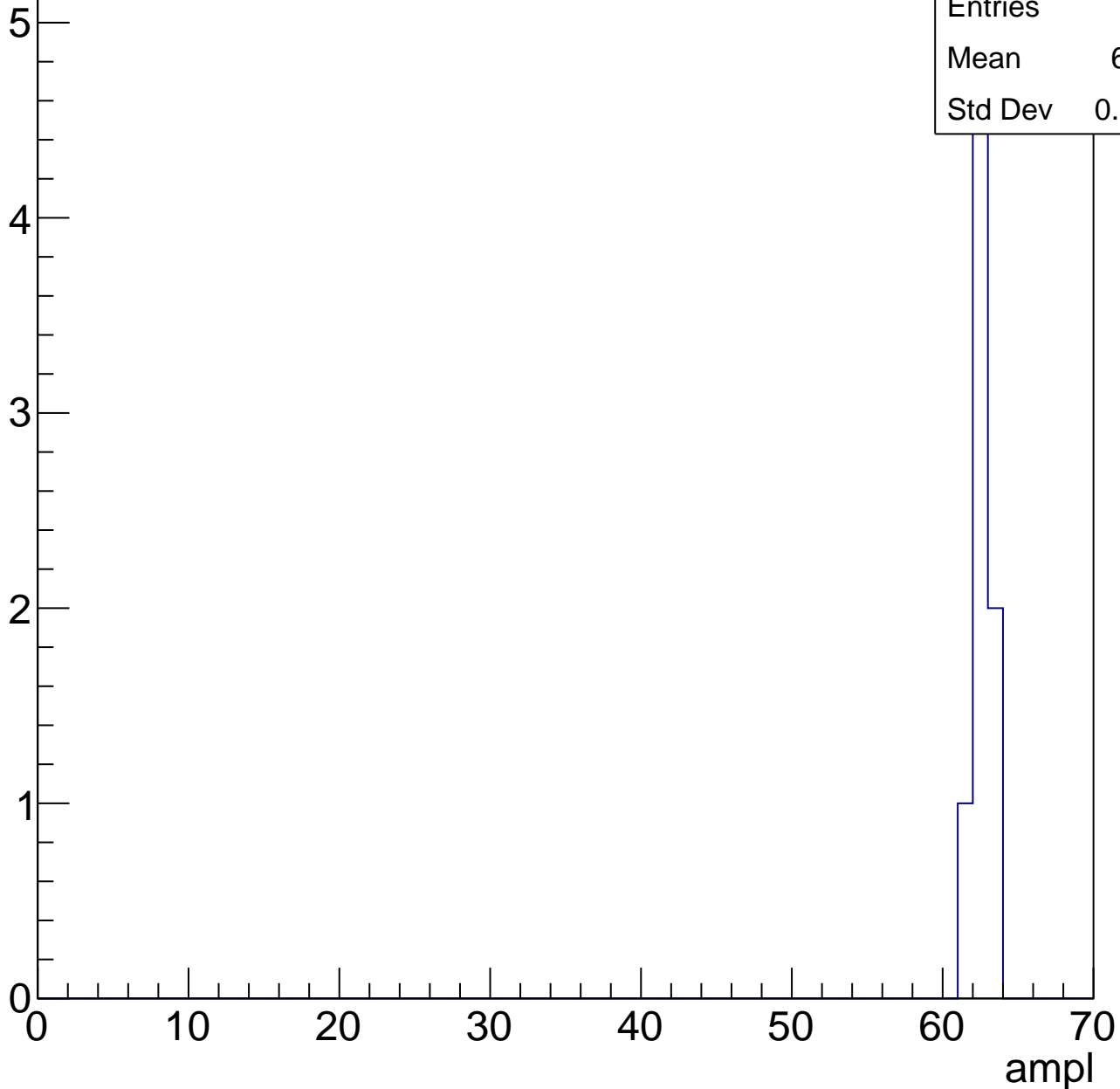
Entries	54
Mean	58.33
Std Dev	8.422

B1L103S, U11-ch88, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	8
Mean	62.12
Std Dev	0.5995



B1L103S, U11-ch88, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

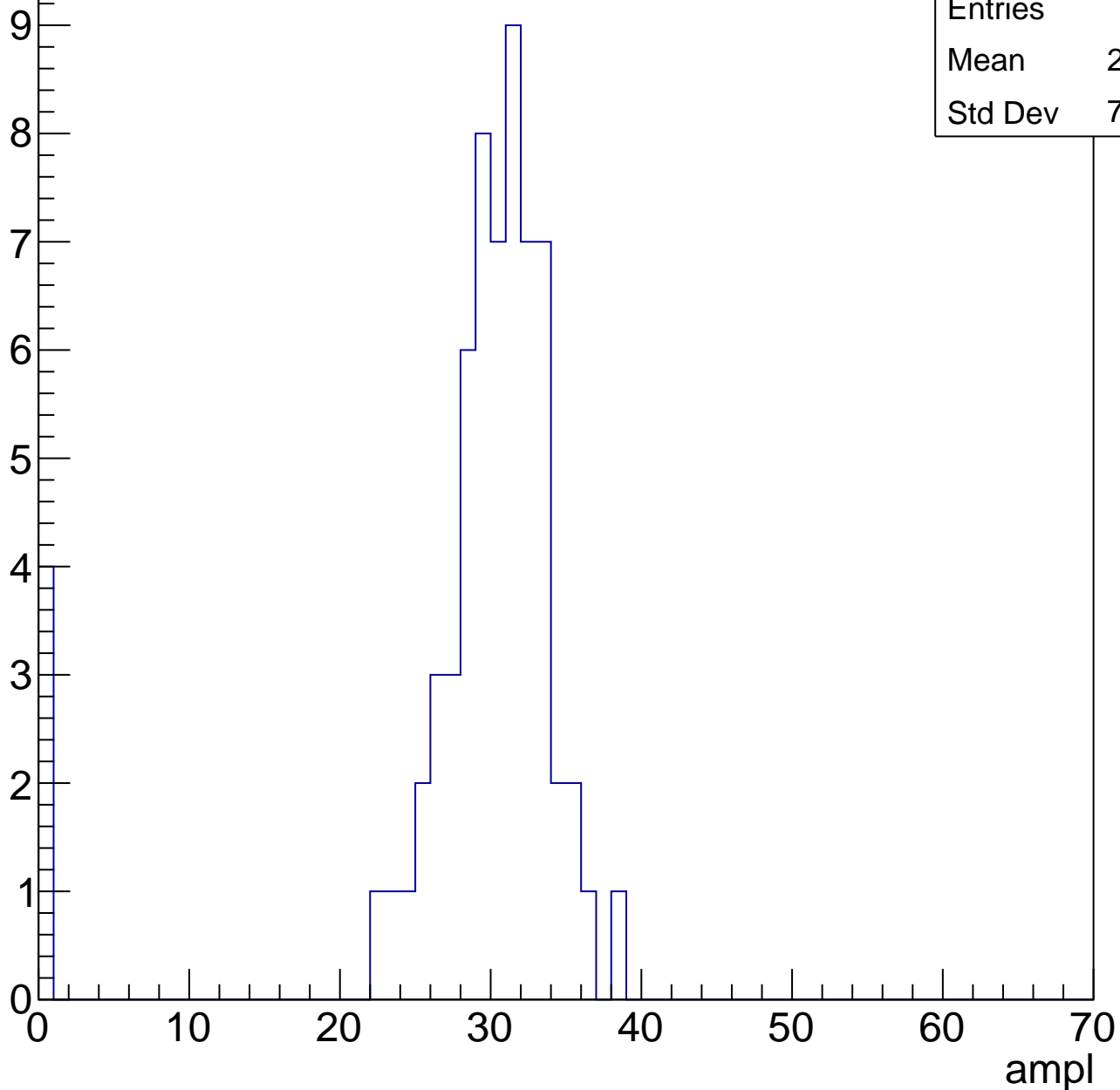
Entries	19
Mean	0
Std Dev	0

B1L103S, U11-ch89, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	28.22
Std Dev	7.826

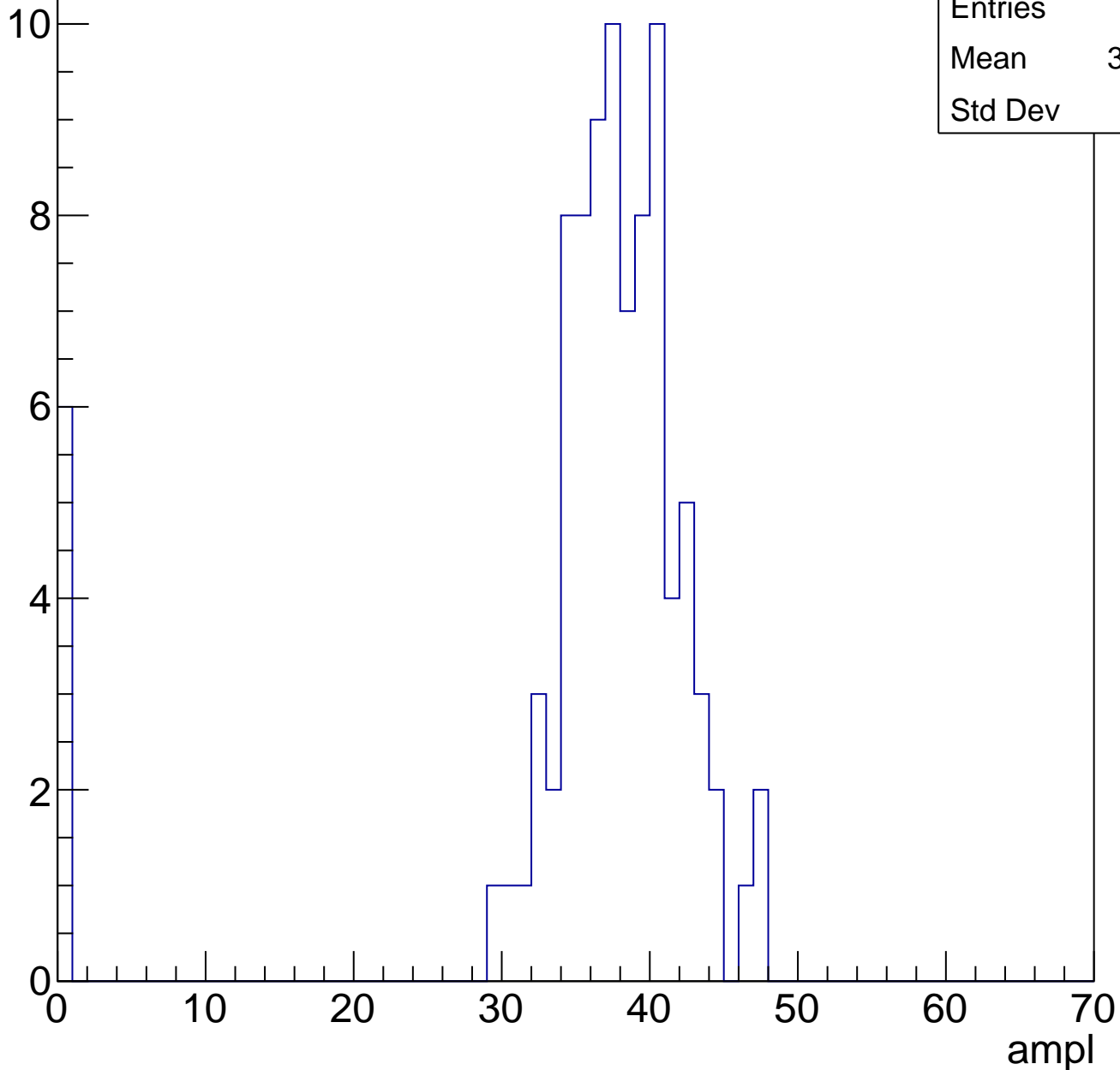


B1L103S, U11-ch89, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	91
Mean	35.24
Std Dev	10

Entry

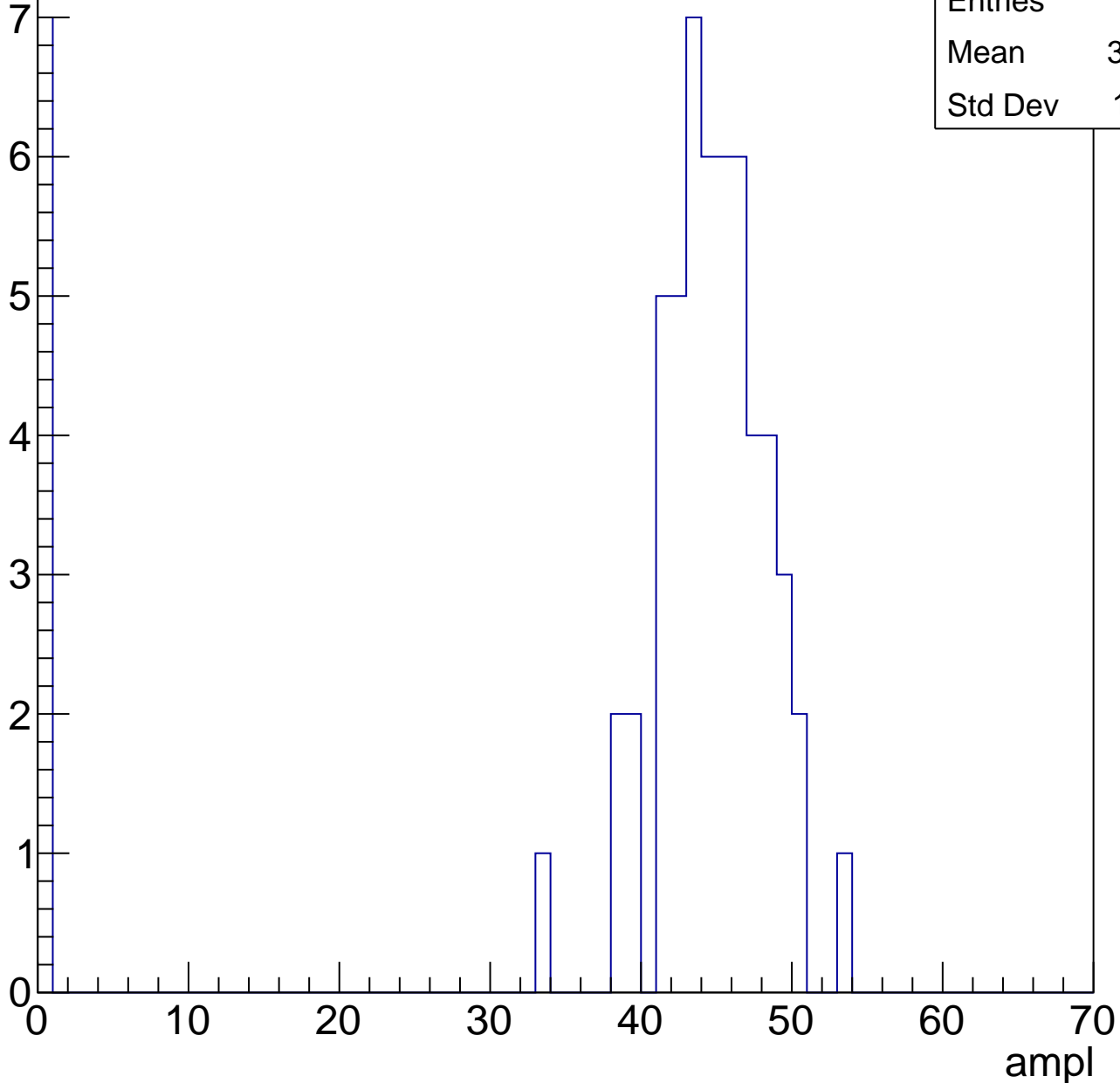


B1L103S, U11-ch89, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	39.23
Std Dev	14.51

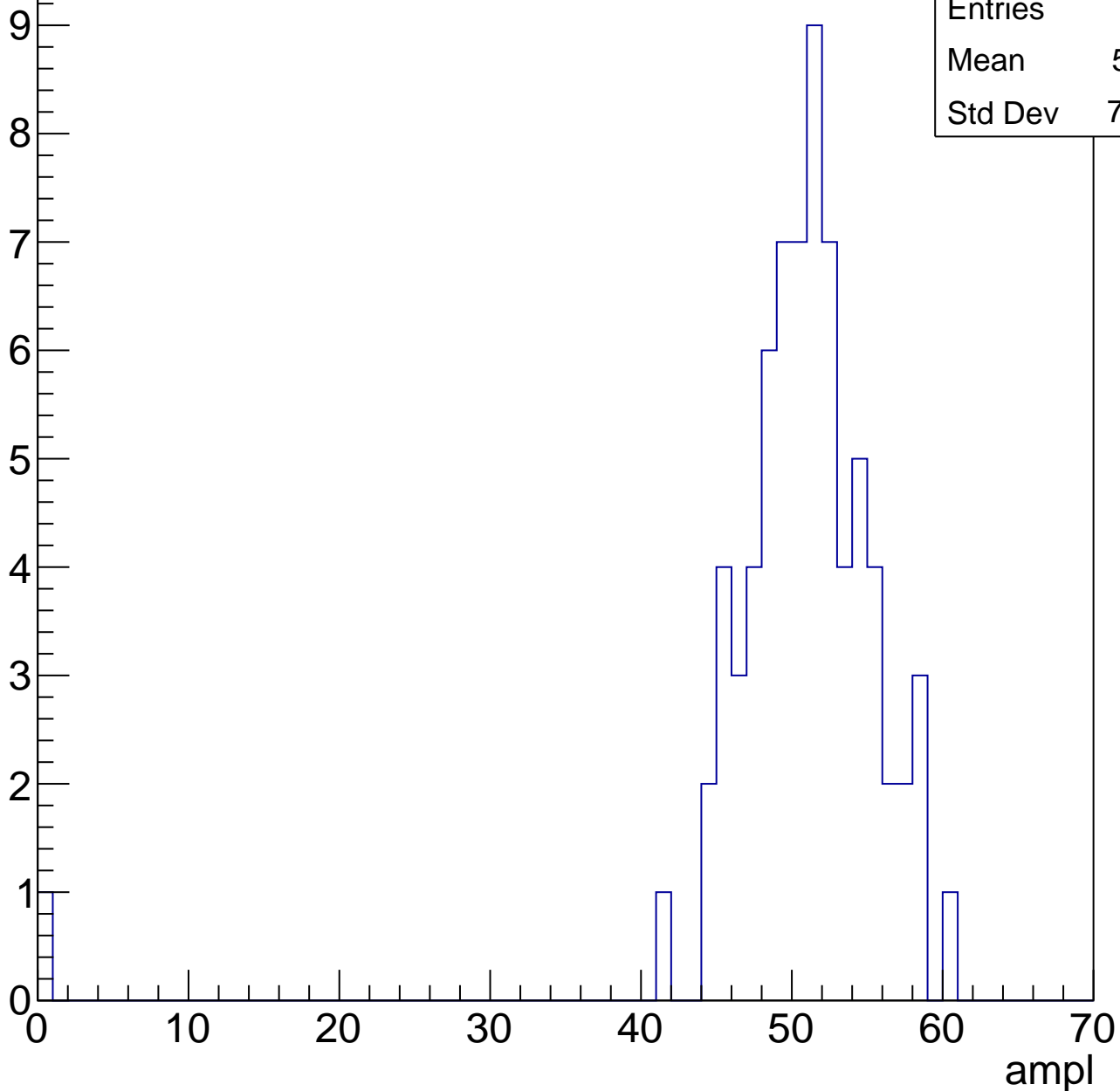


B1L103S, U11-ch89, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

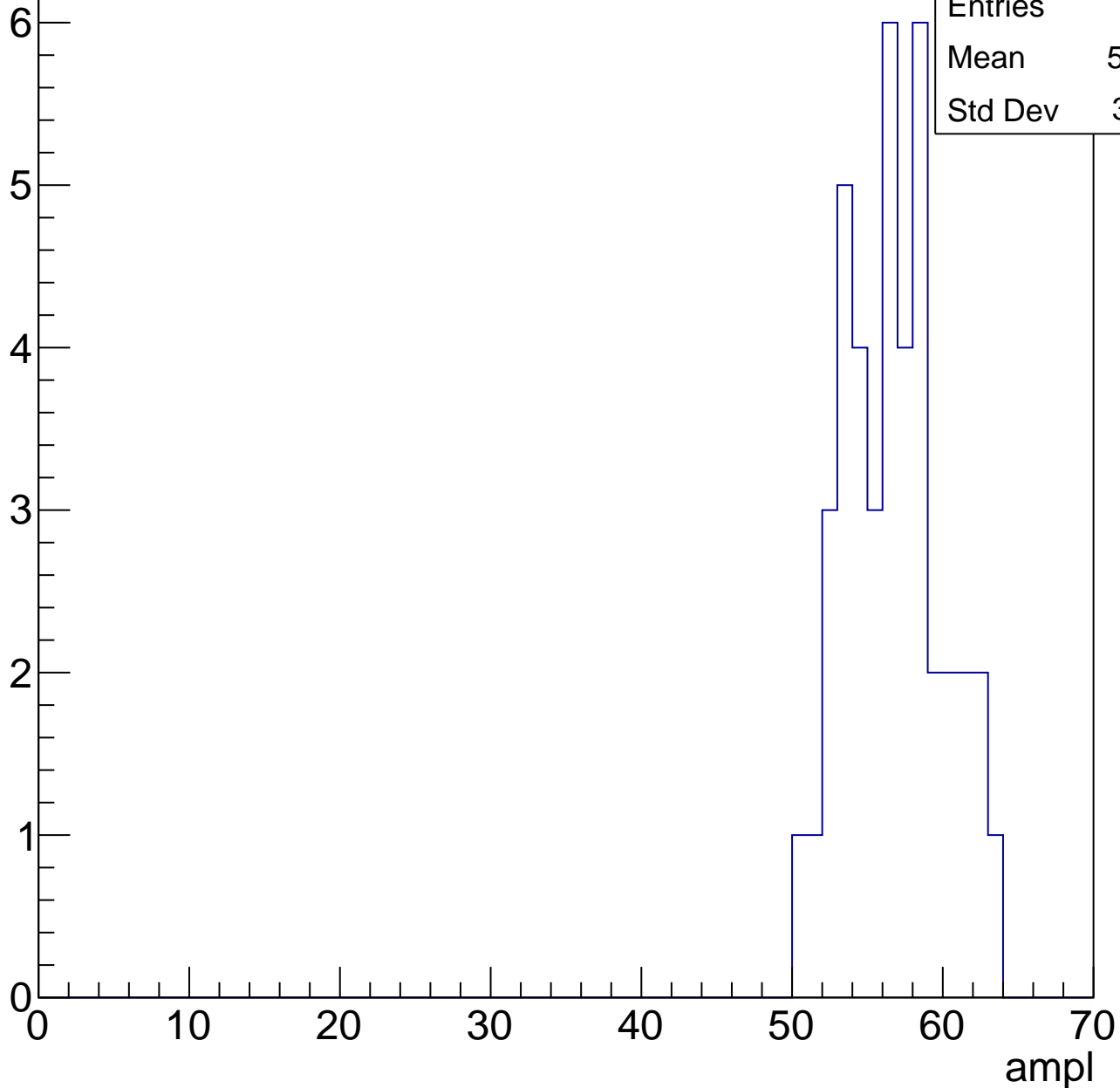
Entries	72
Mean	50.01
Std Dev	7.054



B1L103S, U11-ch89, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

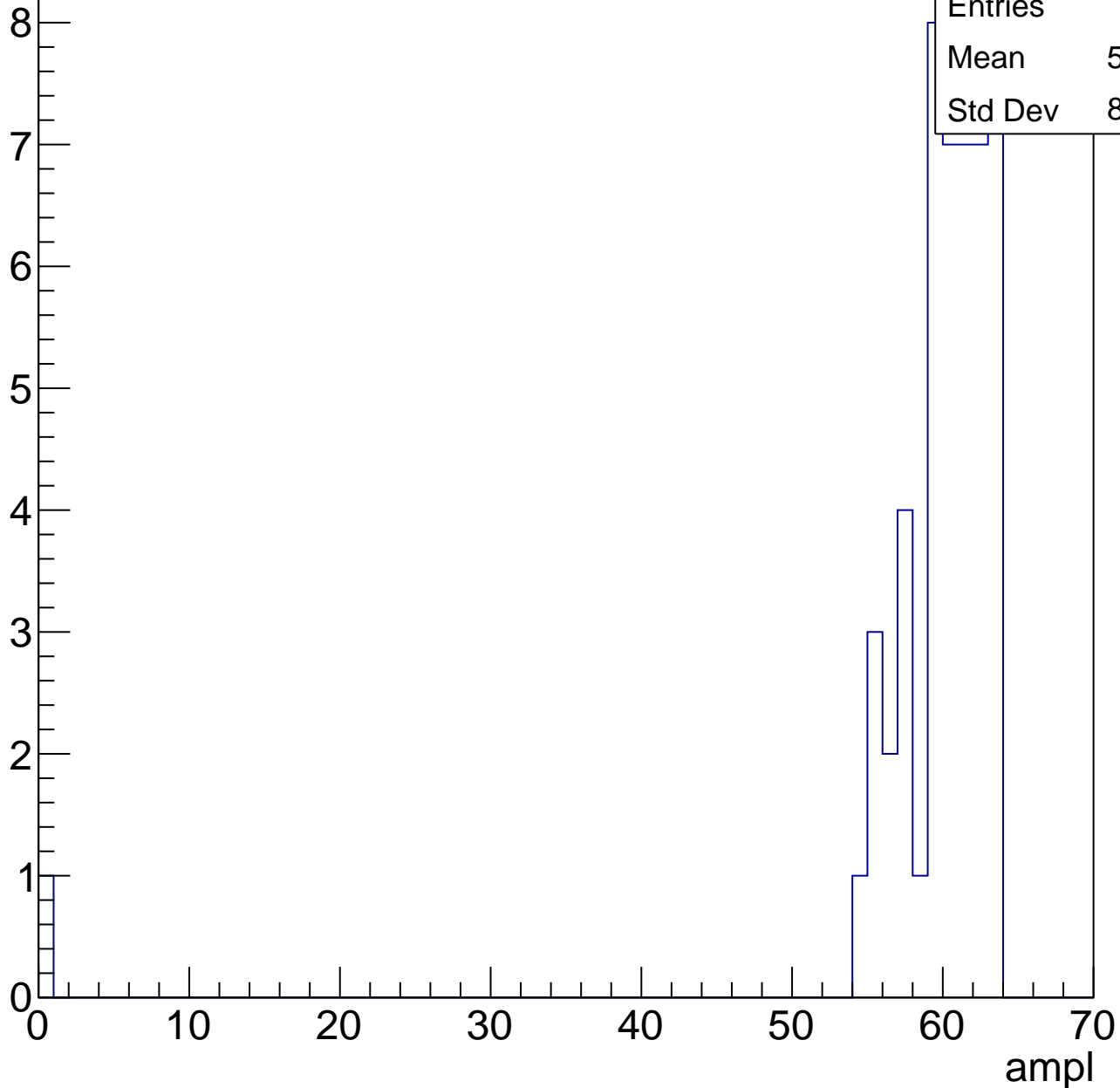


Entries	42
Mean	56.24
Std Dev	3.161

B1L103S, U11-ch89, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch89, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch89, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

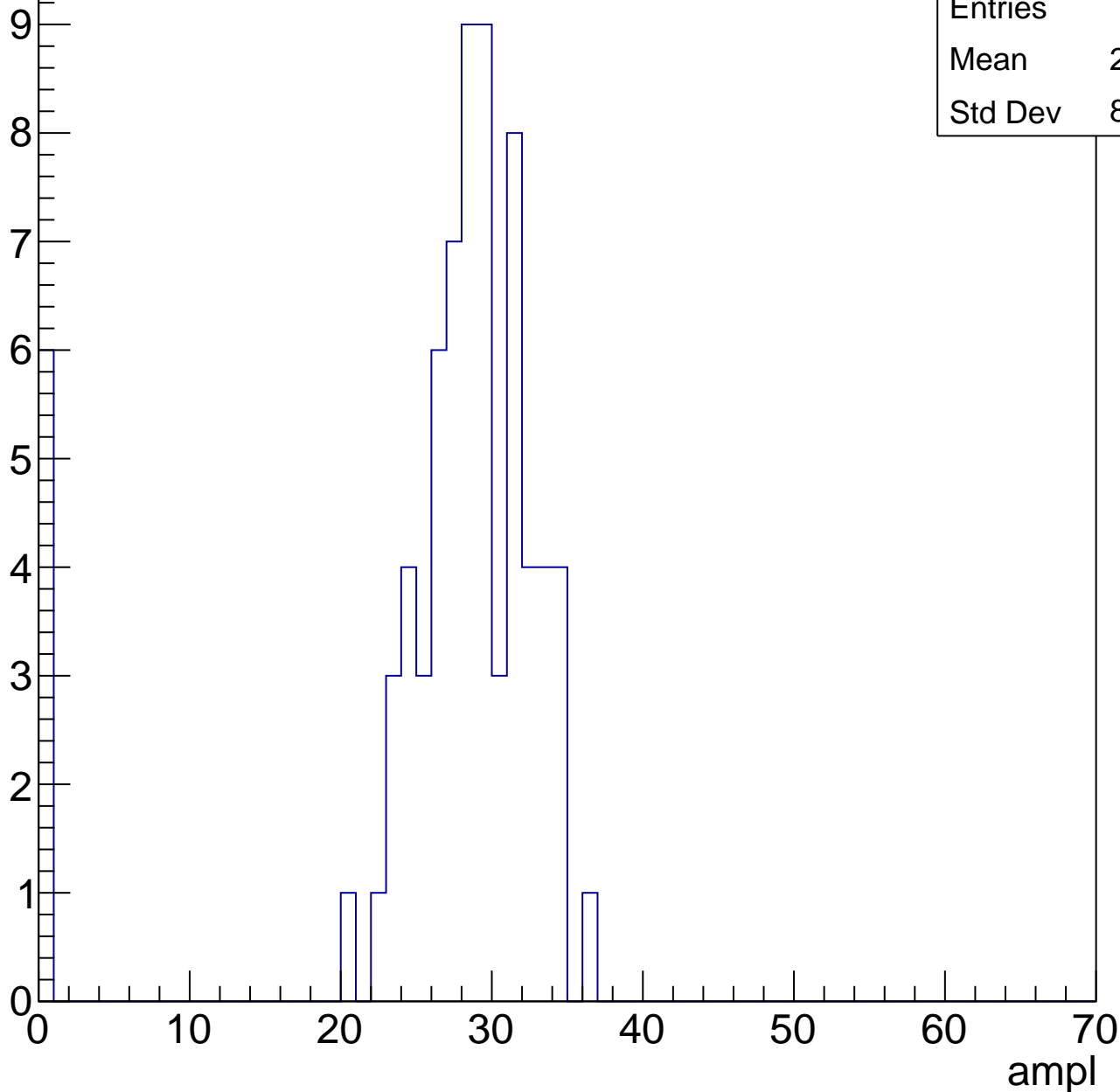


B1L103S, U11-ch90, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	26.16
Std Dev	8.456

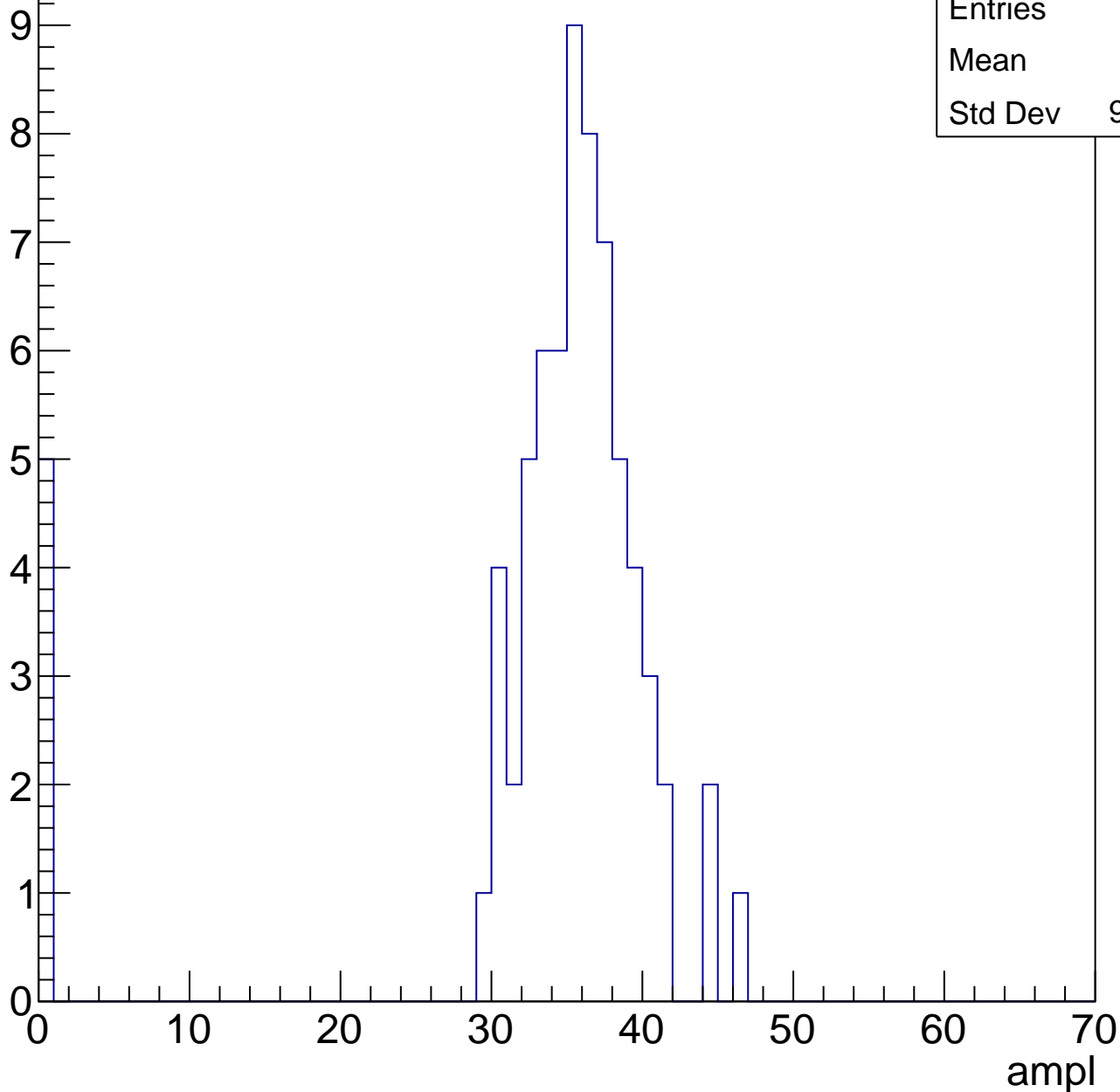


B1L103S, U11-ch90, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	33.1
Std Dev	9.776

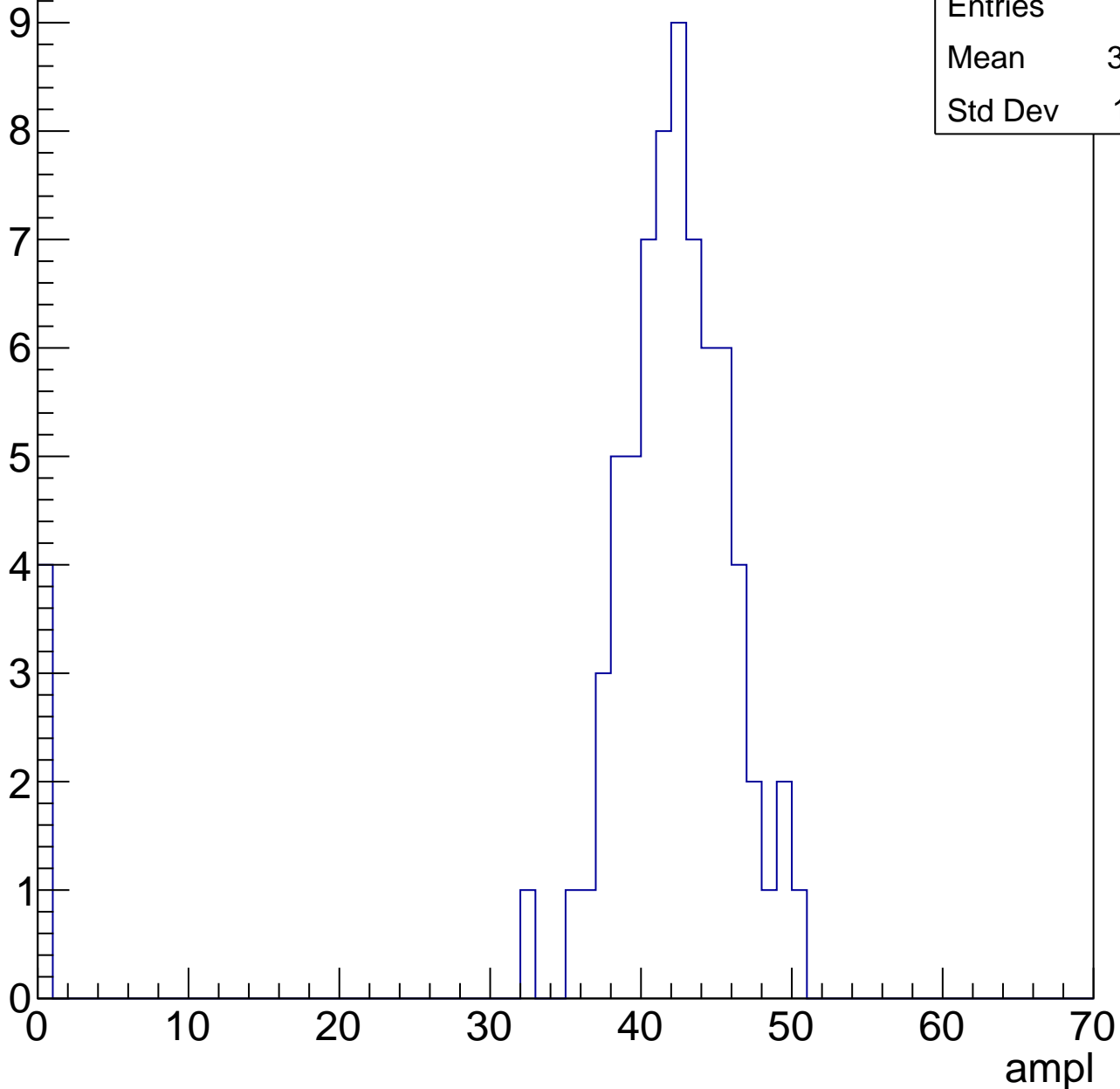


B1L103S, U11-ch90, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	39.64
Std Dev	10.11

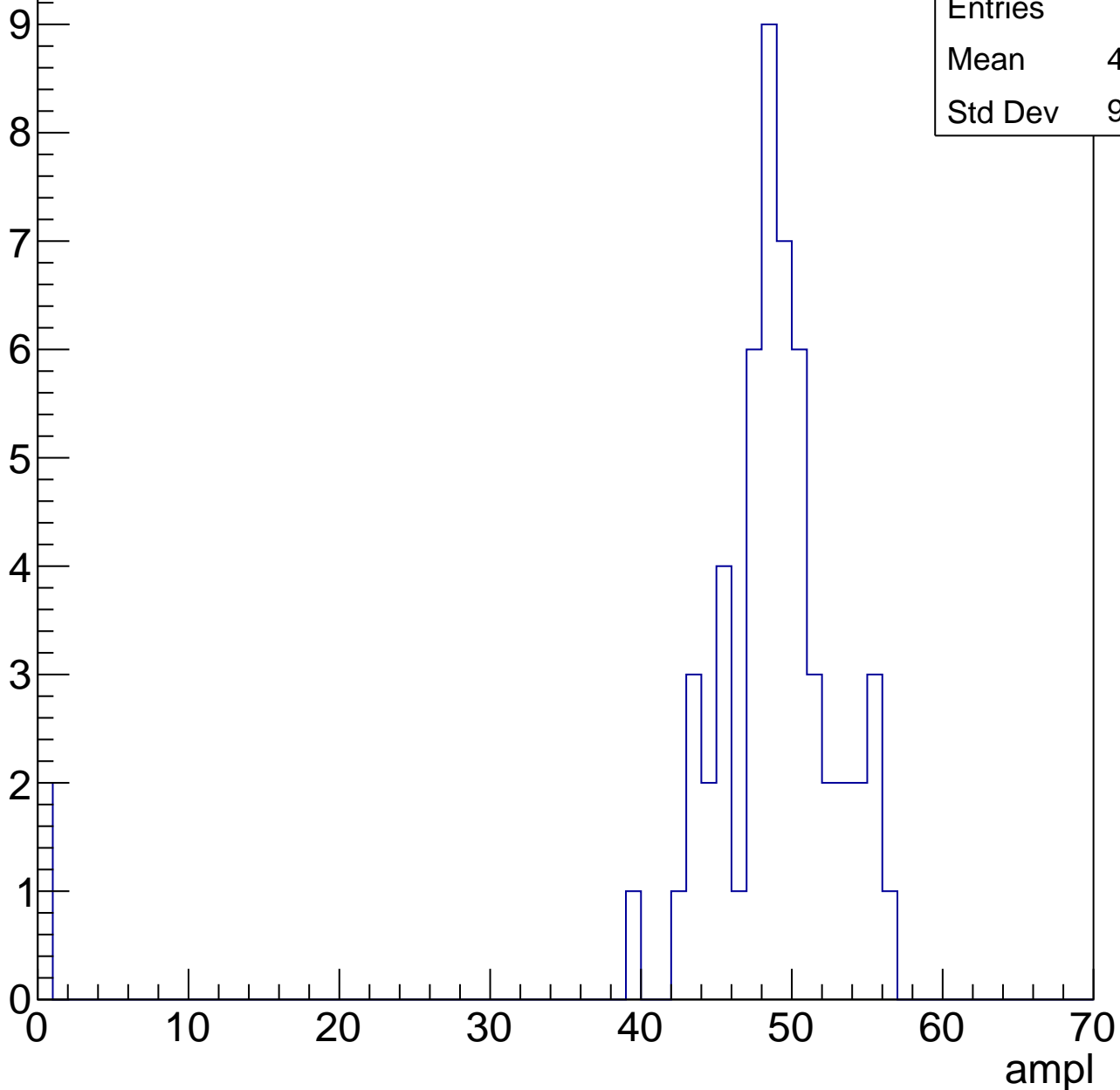


B1L103S, U11-ch90, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	46.78
Std Dev	9.742

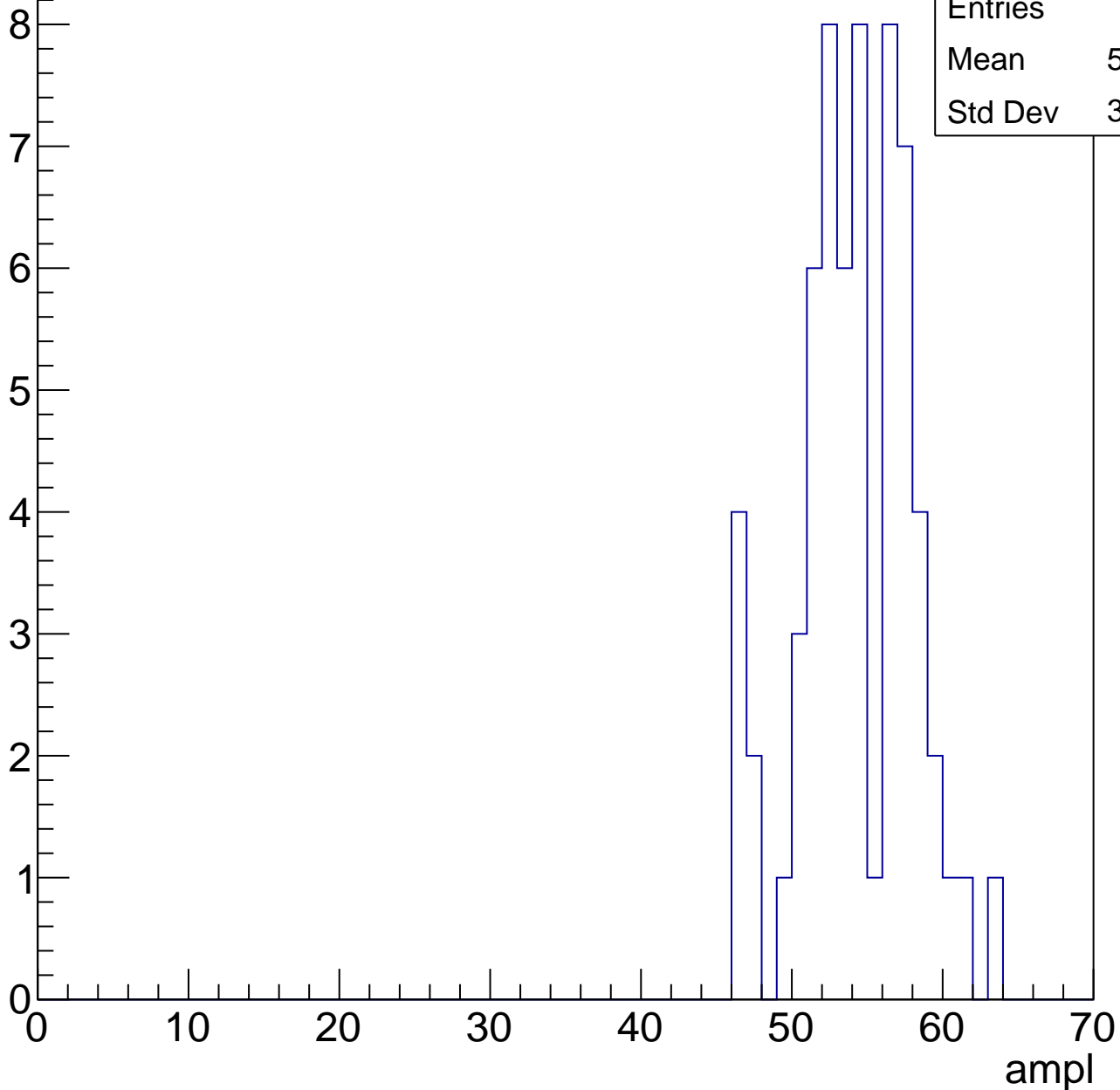


B1L103S, U11-ch90, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	53.73
Std Dev	3.759

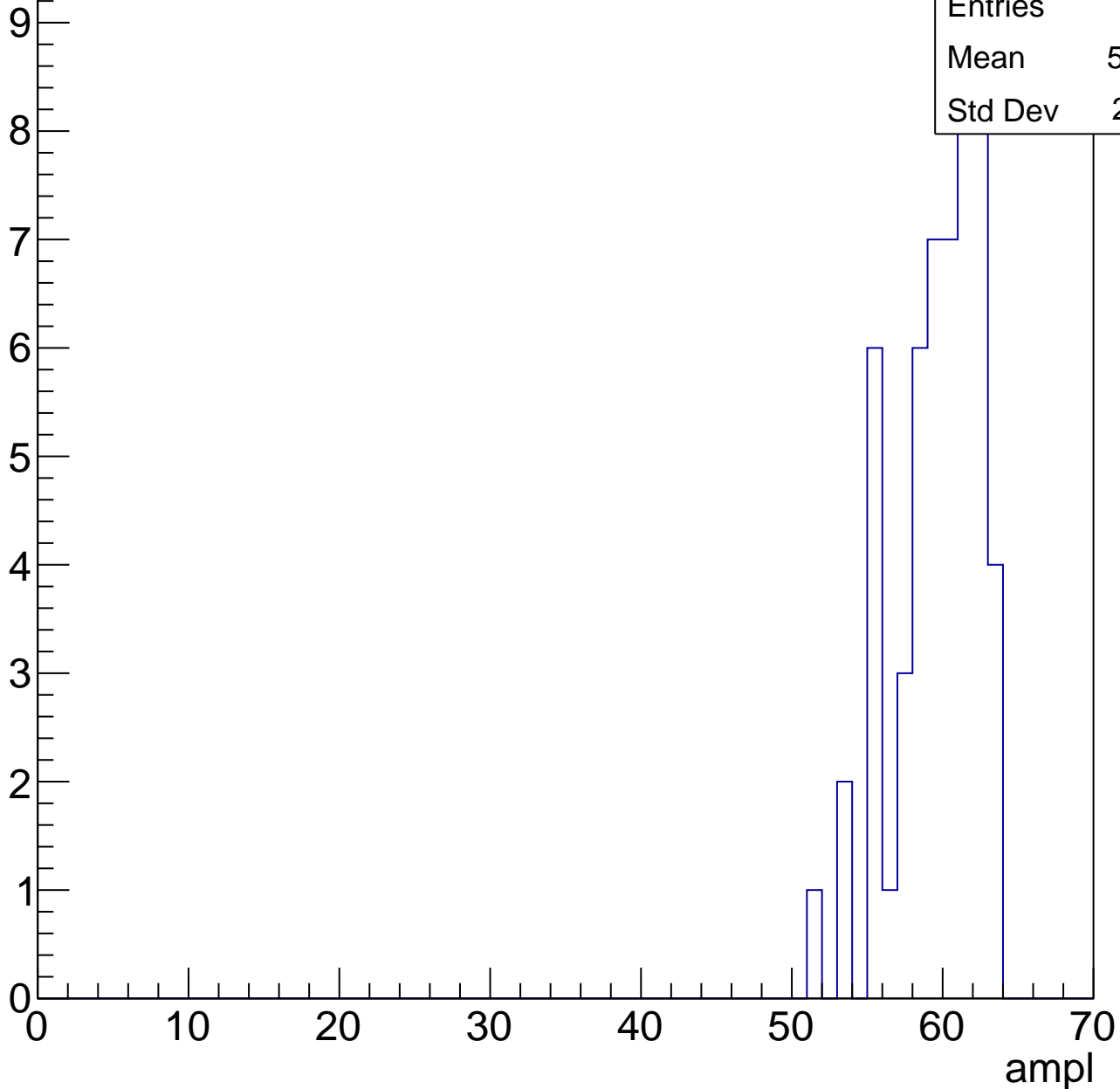


B1L103S, U11-ch90, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	59.13
Std Dev	2.861

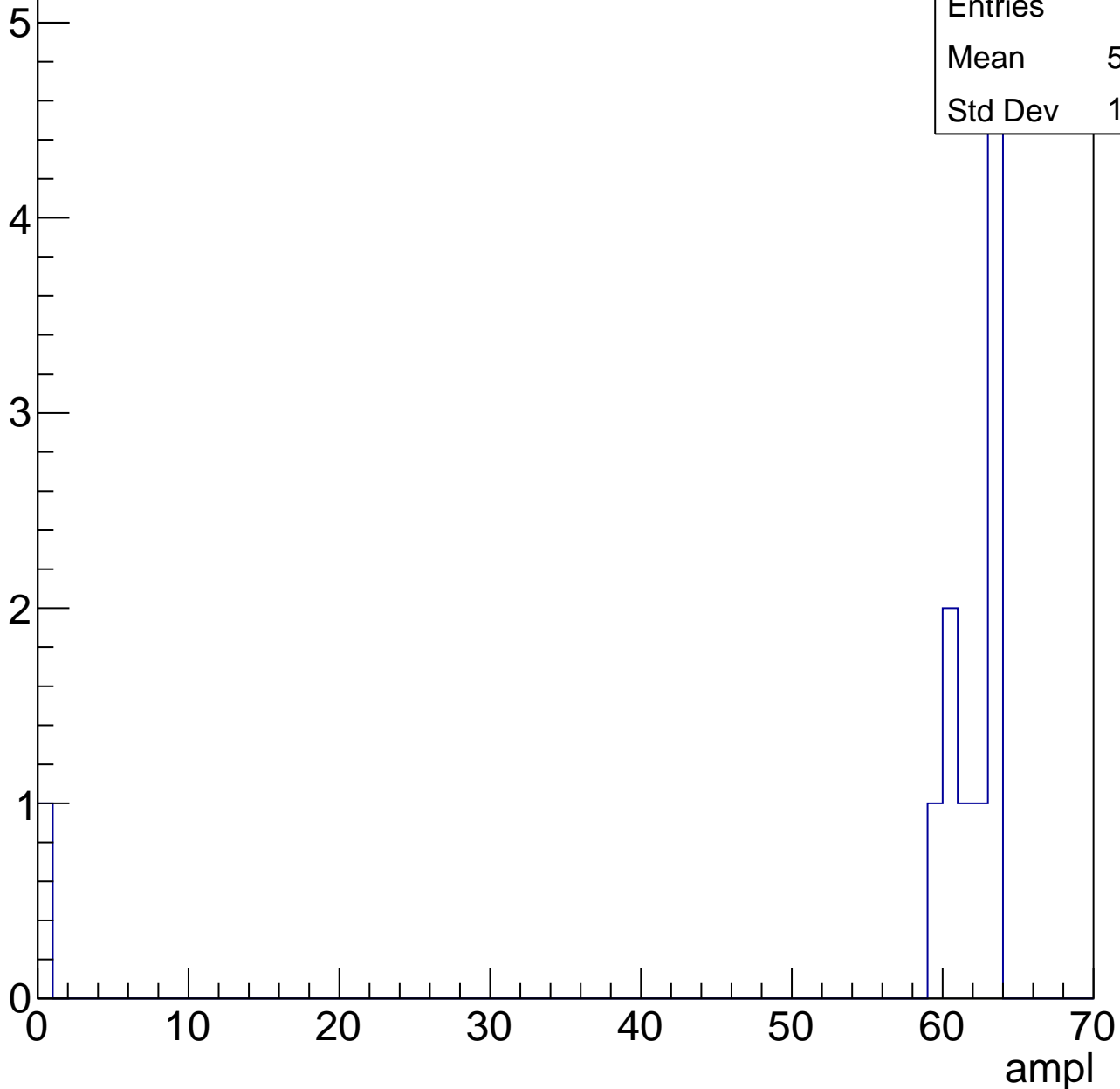


B1L103S, U11-ch90, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	11
Mean	56.09
Std Dev	17.79



B1L103S, U11-ch90, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

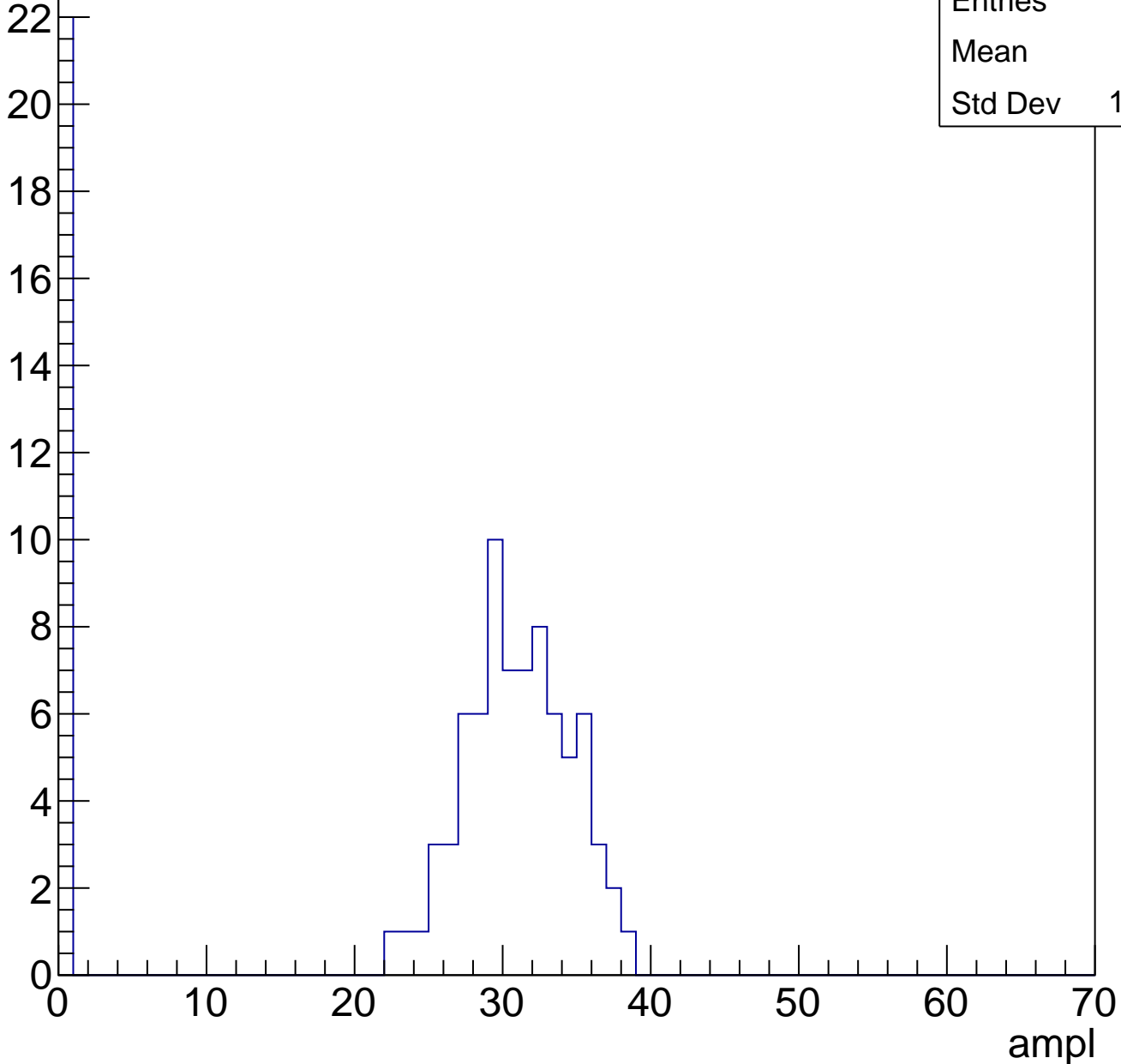
Entries	19
Mean	0
Std Dev	0

B1L103S, U11-ch91, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	98
Mean	23.7
Std Dev	13.12

Entry



B1L103S, U11-ch91, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	30.69
Std Dev	14.4

Entry

12

10

8

6

4

2

0

0

10

20

30

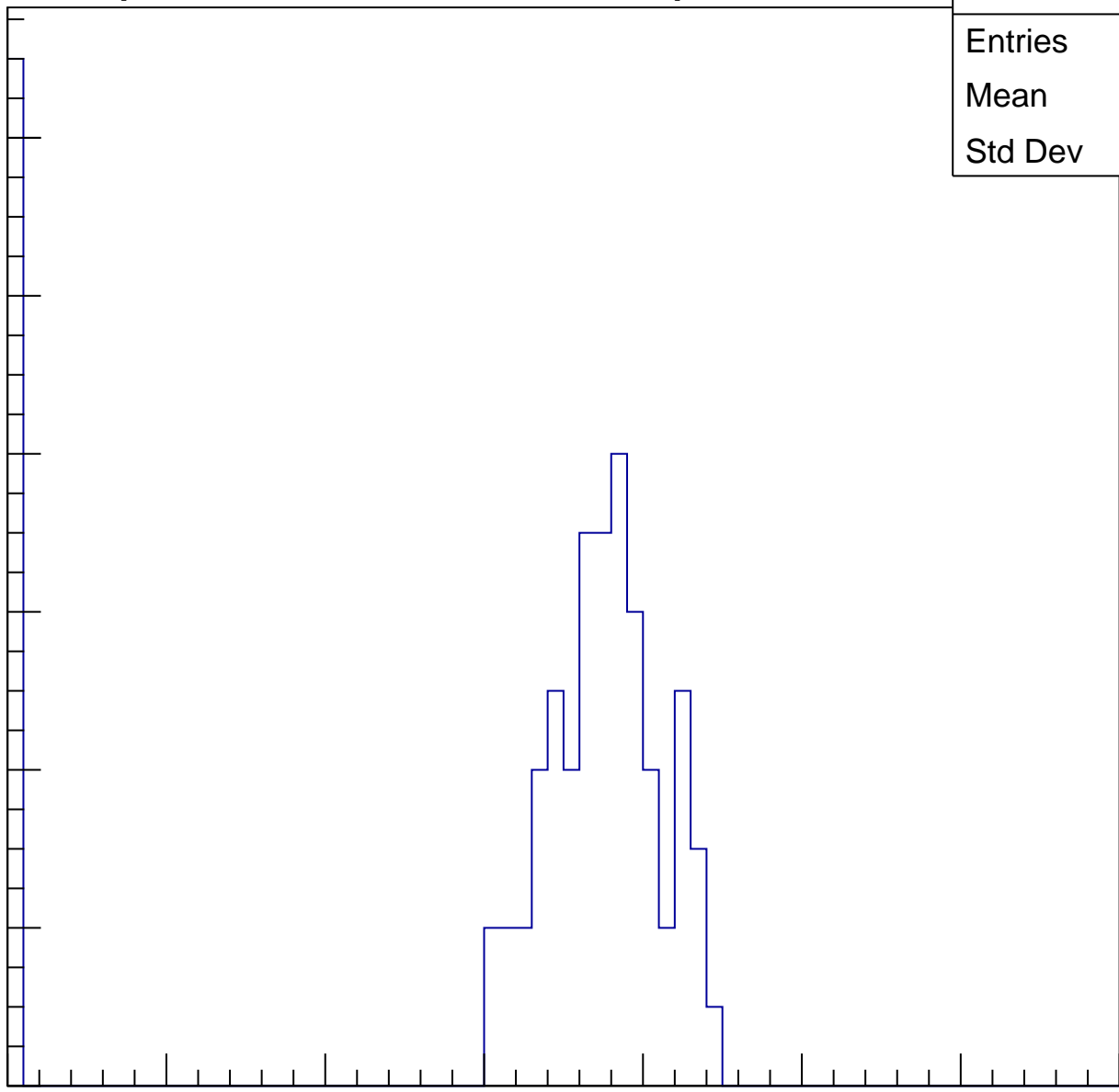
40

50

60

70

ampl

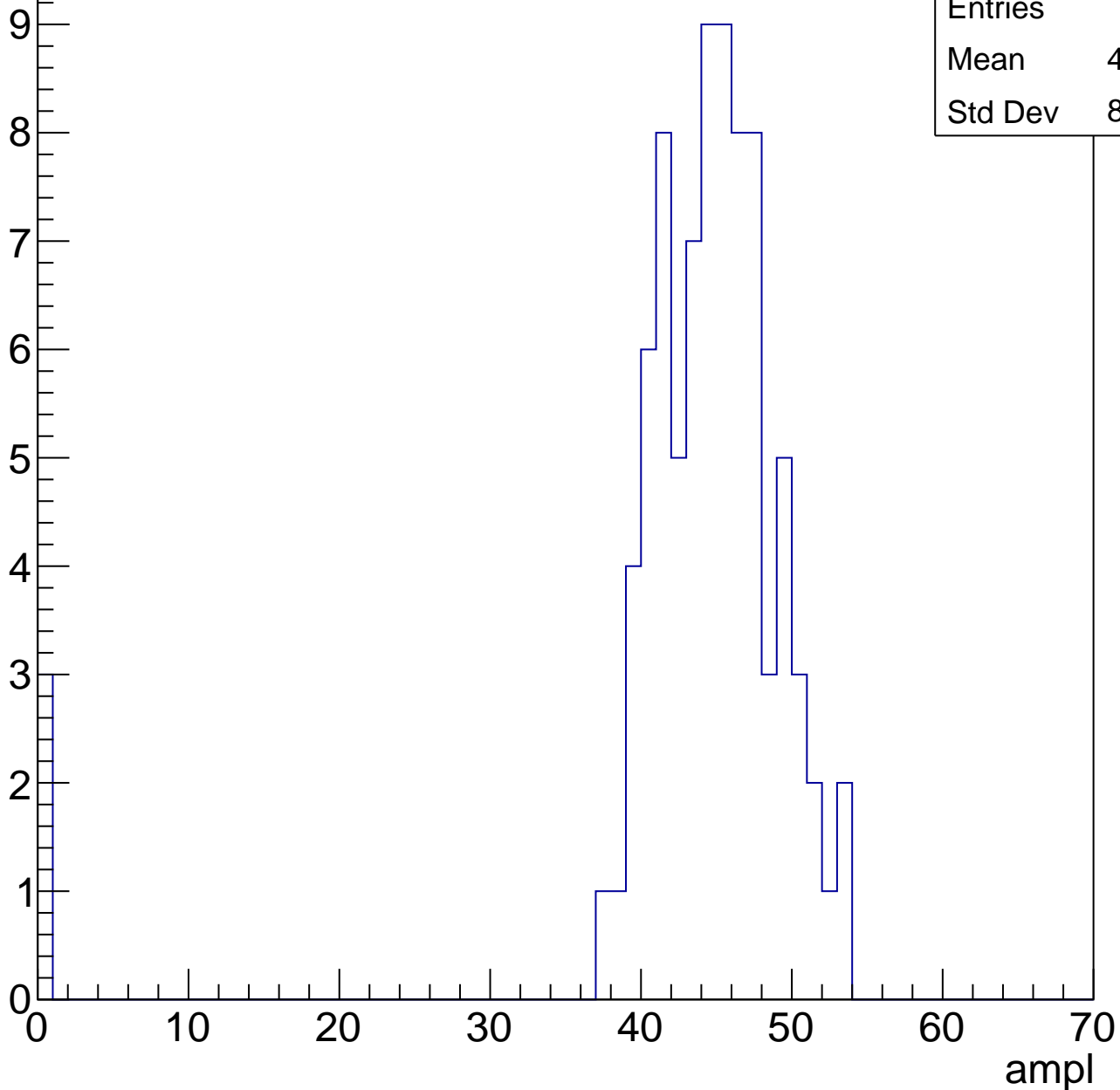


B1L103S, U11-ch91, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	85
Mean	42.99
Std Dev	8.957

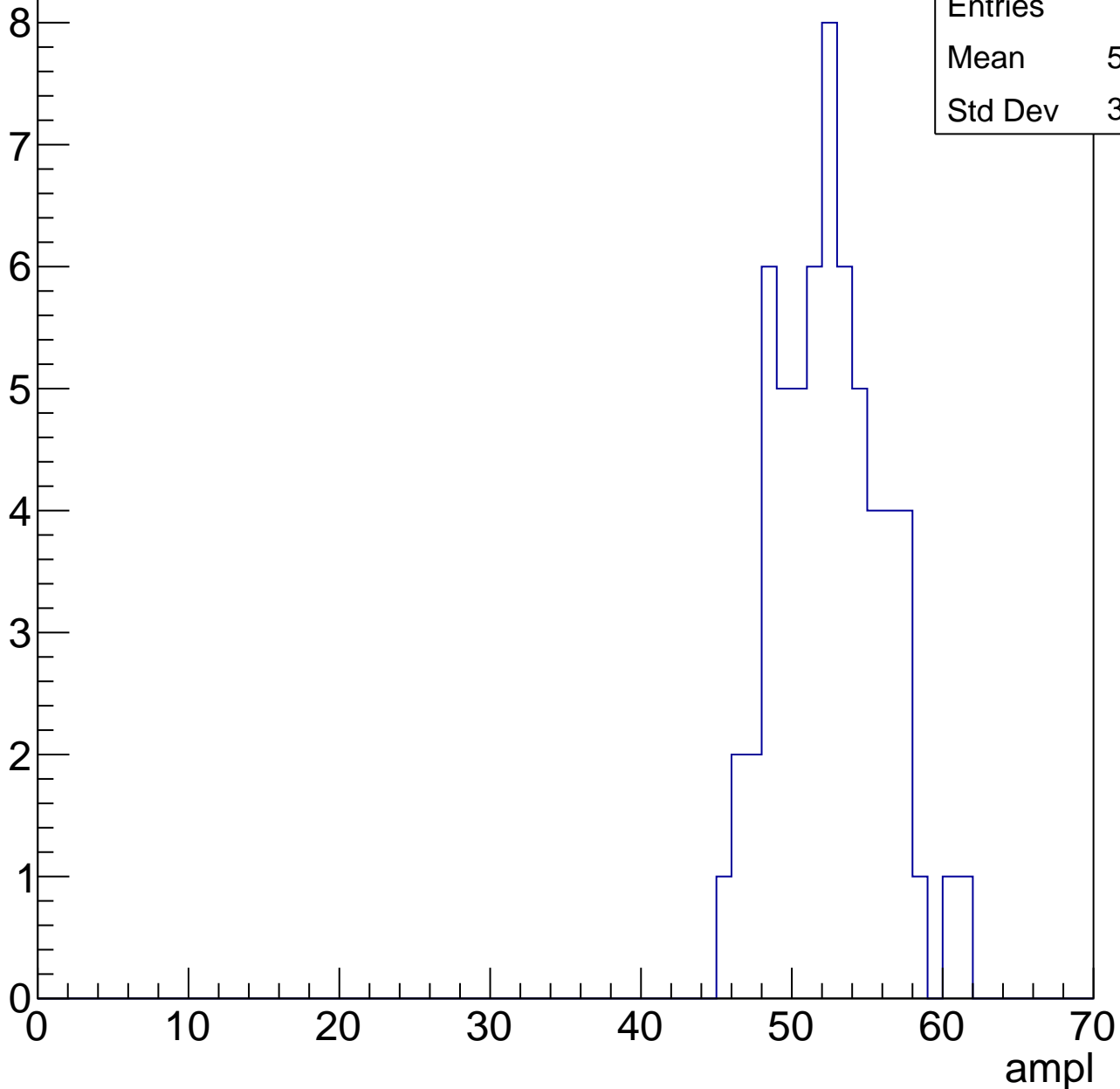


B1L103S, U11-ch91, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

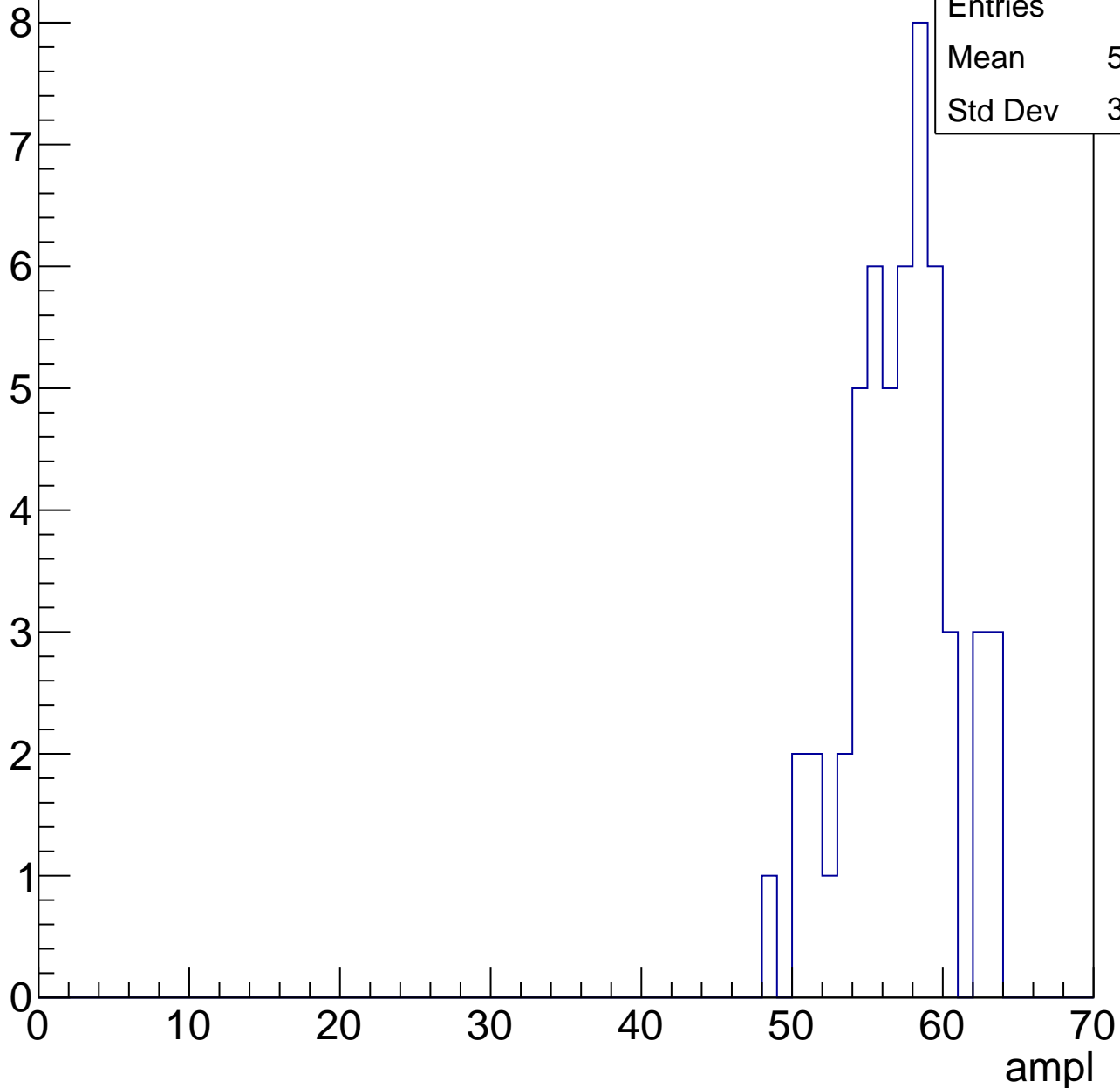
Entries	61
Mean	52.05
Std Dev	3.494



B1L103S, U11-ch91, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

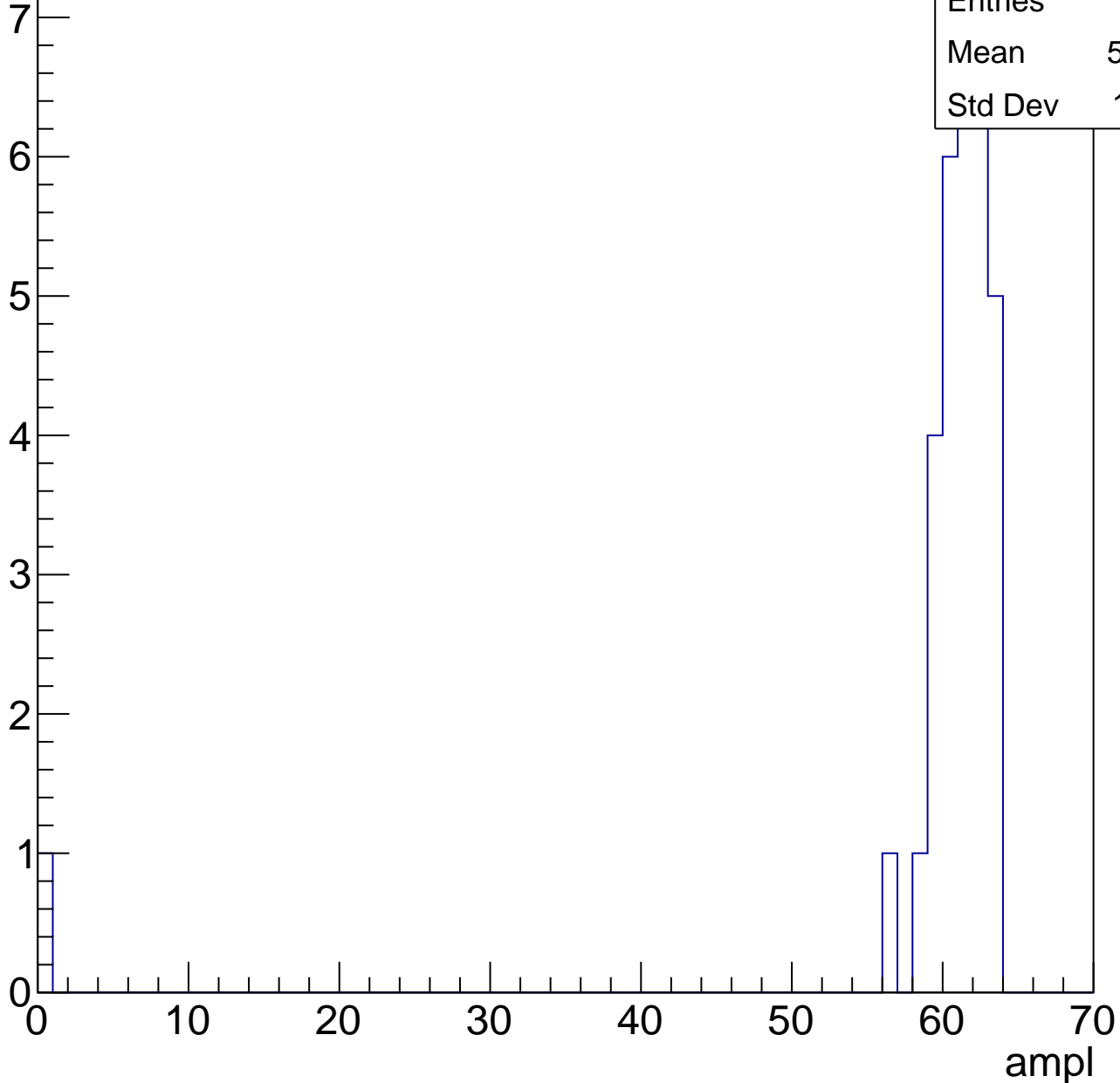


B1L103S, U11-ch91, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

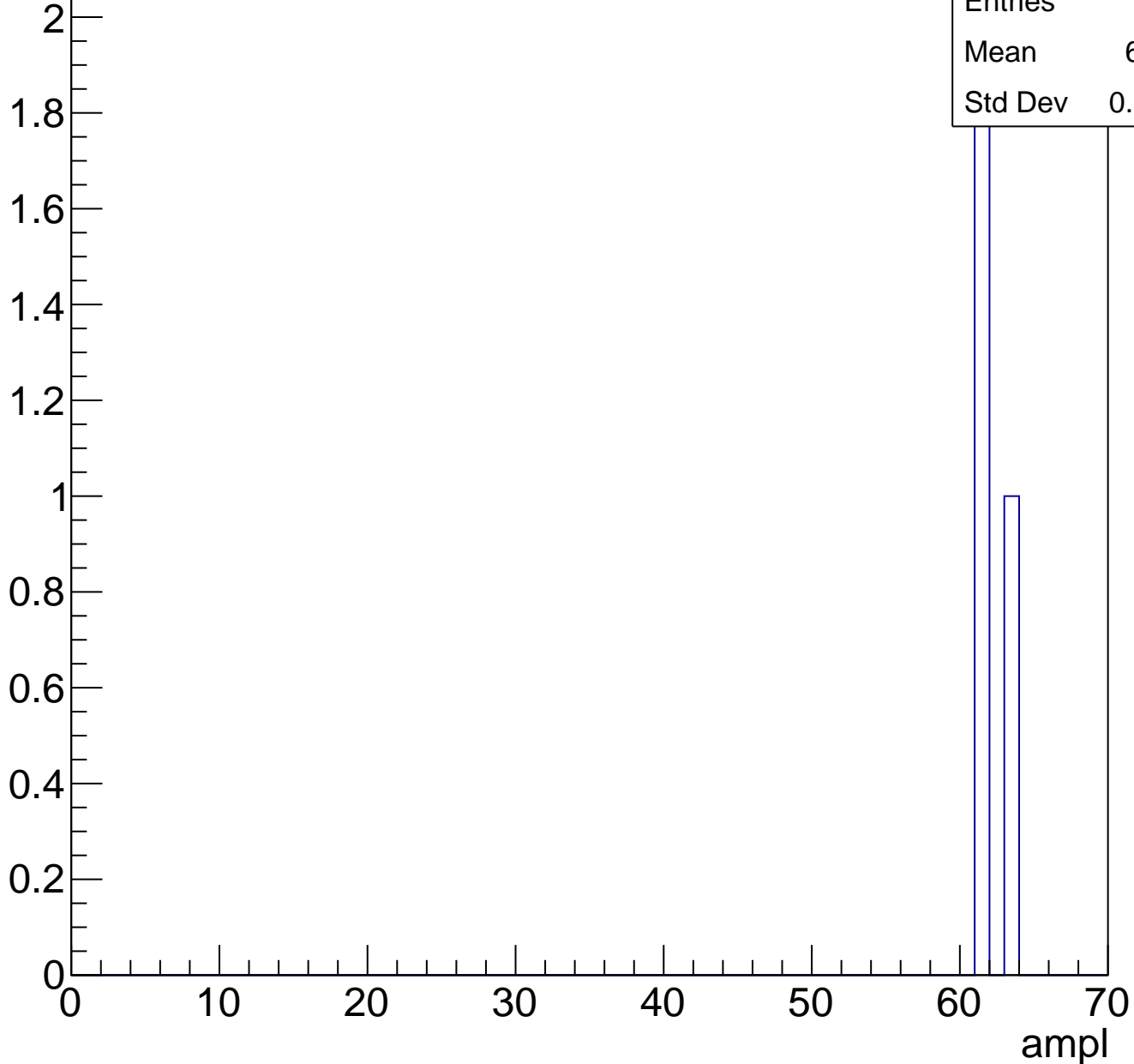
Entries	32
Mean	58.94
Std Dev	10.71



B1L103S, U11-ch91, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	3
Mean	61.67
Std Dev	0.9428

B1L103S, U11-ch91, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

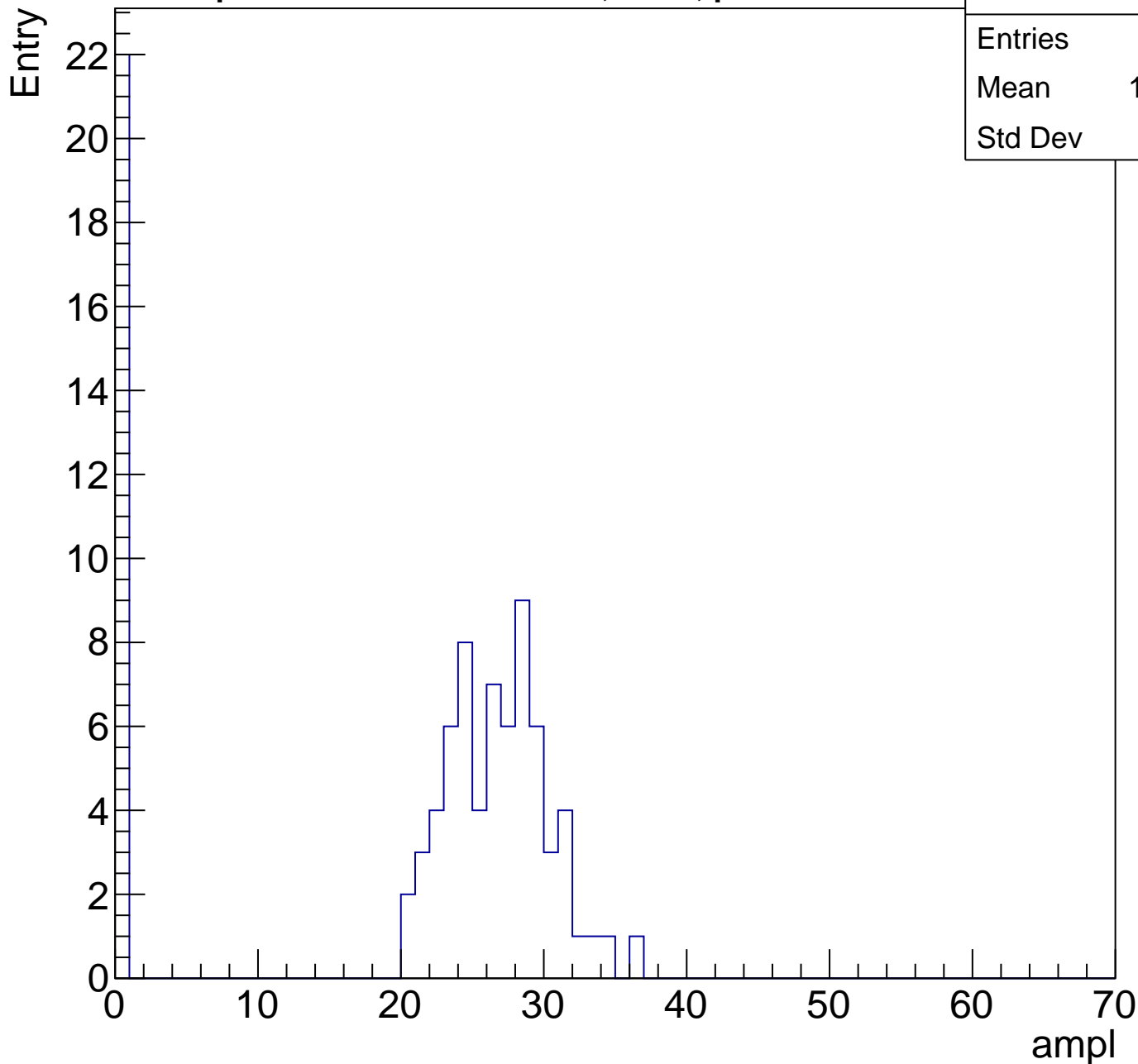
Entry



B1L103S, U11-ch92, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	88
Mean	19.77
Std Dev	11.8

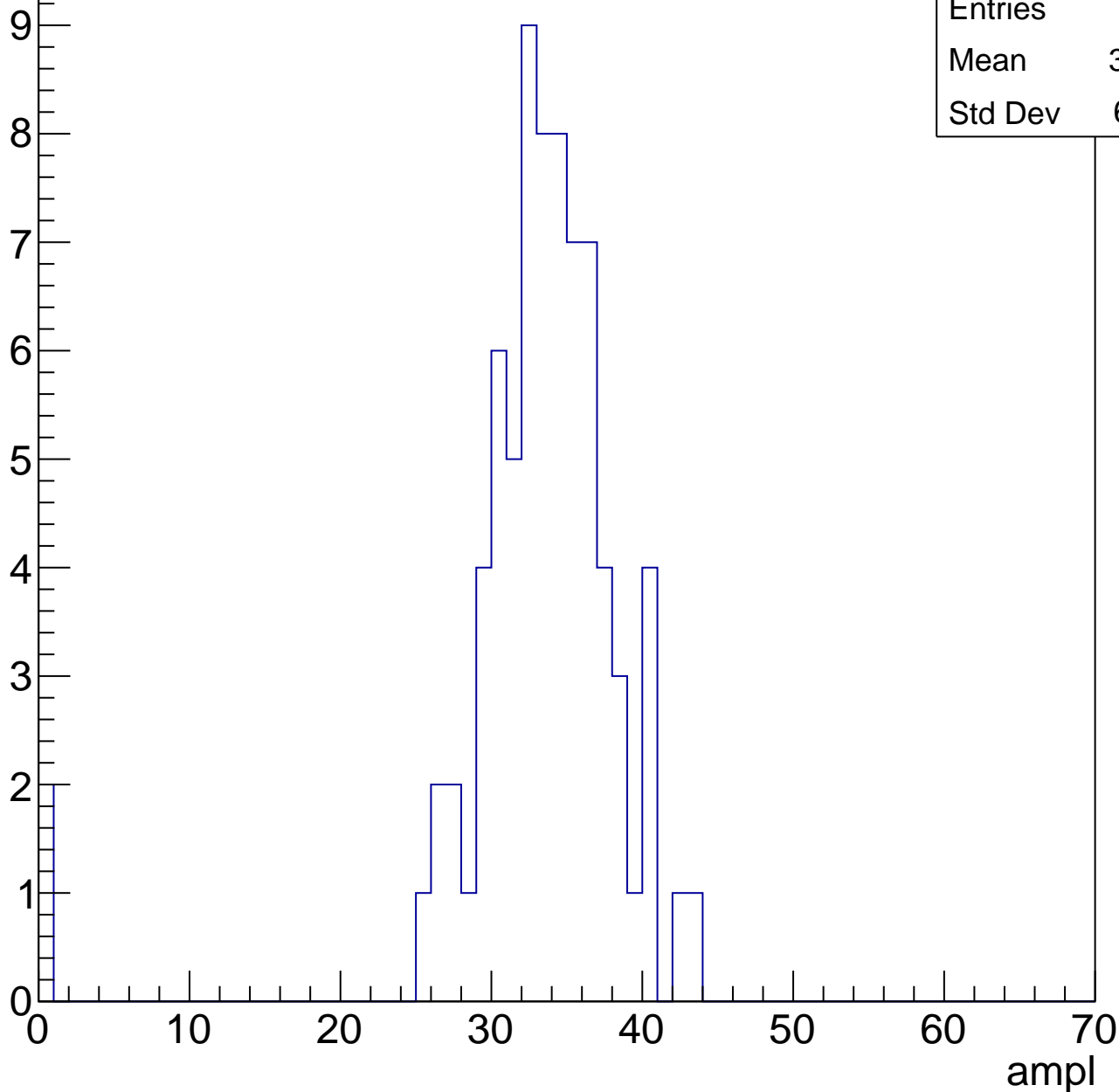


B1L103S, U11-ch92, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	32.59
Std Dev	6.511

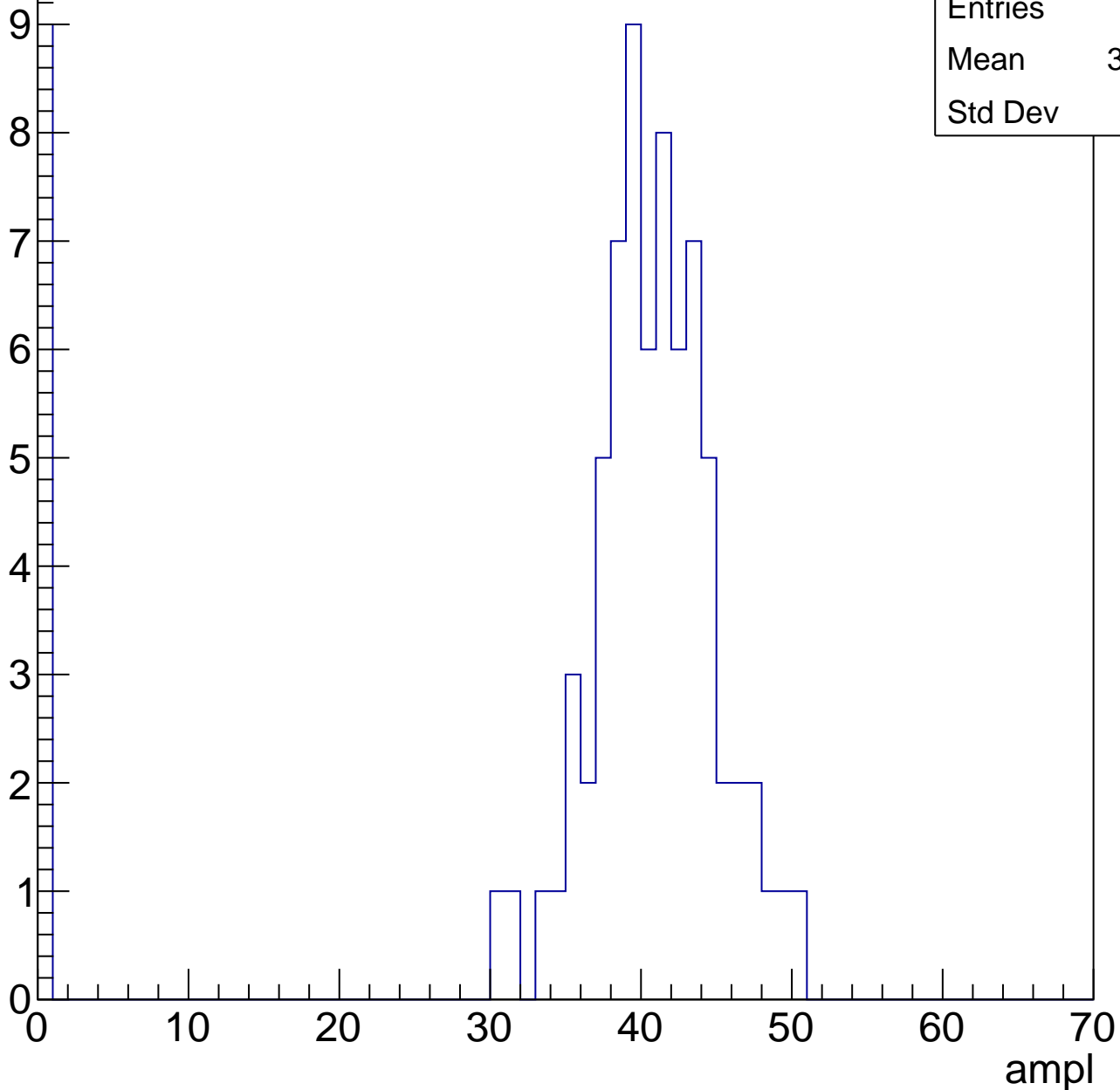


B1L103S, U11-ch92, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	80
Mean	35.89
Std Dev	13.3

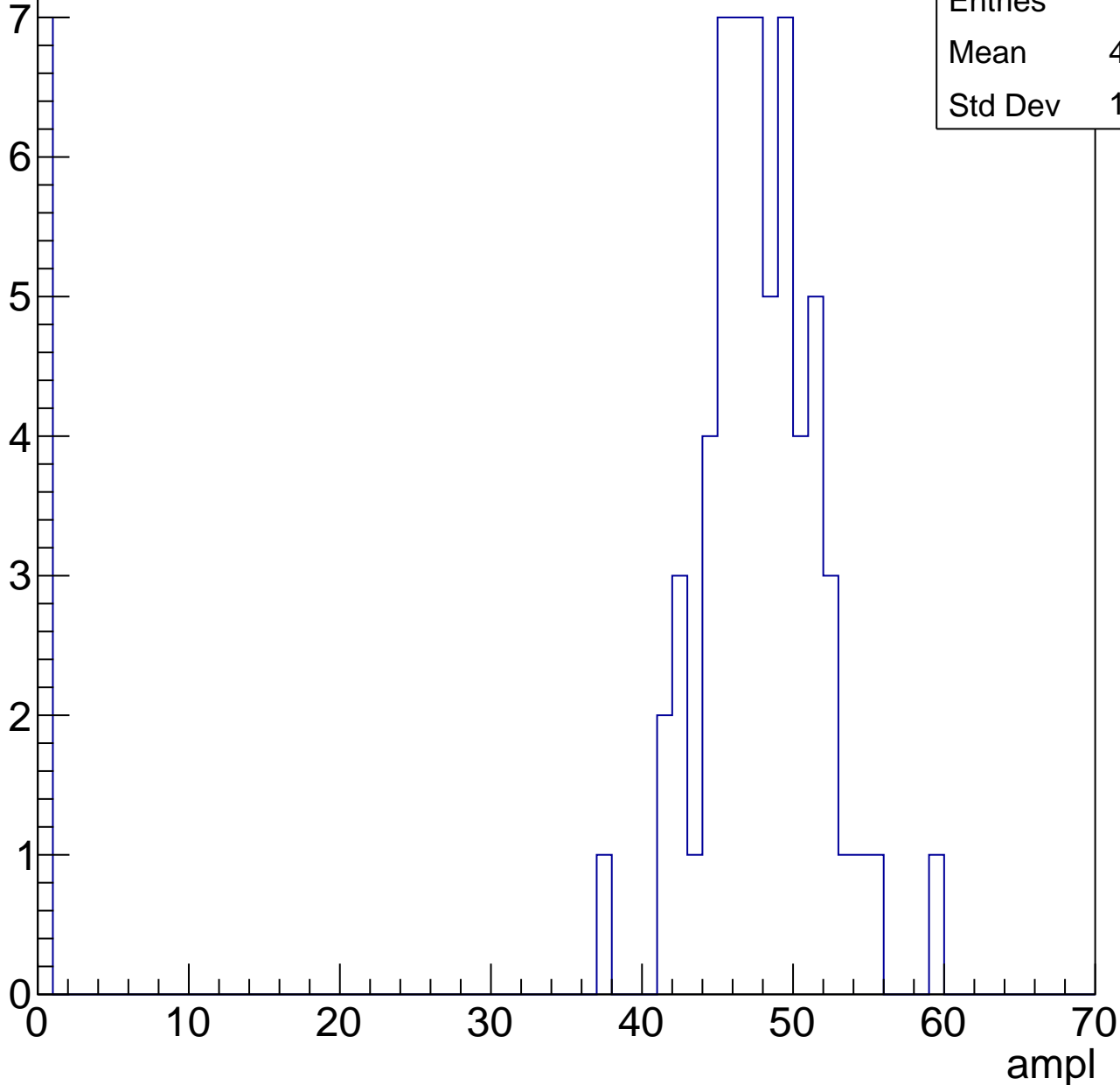


B1L103S, U11-ch92, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

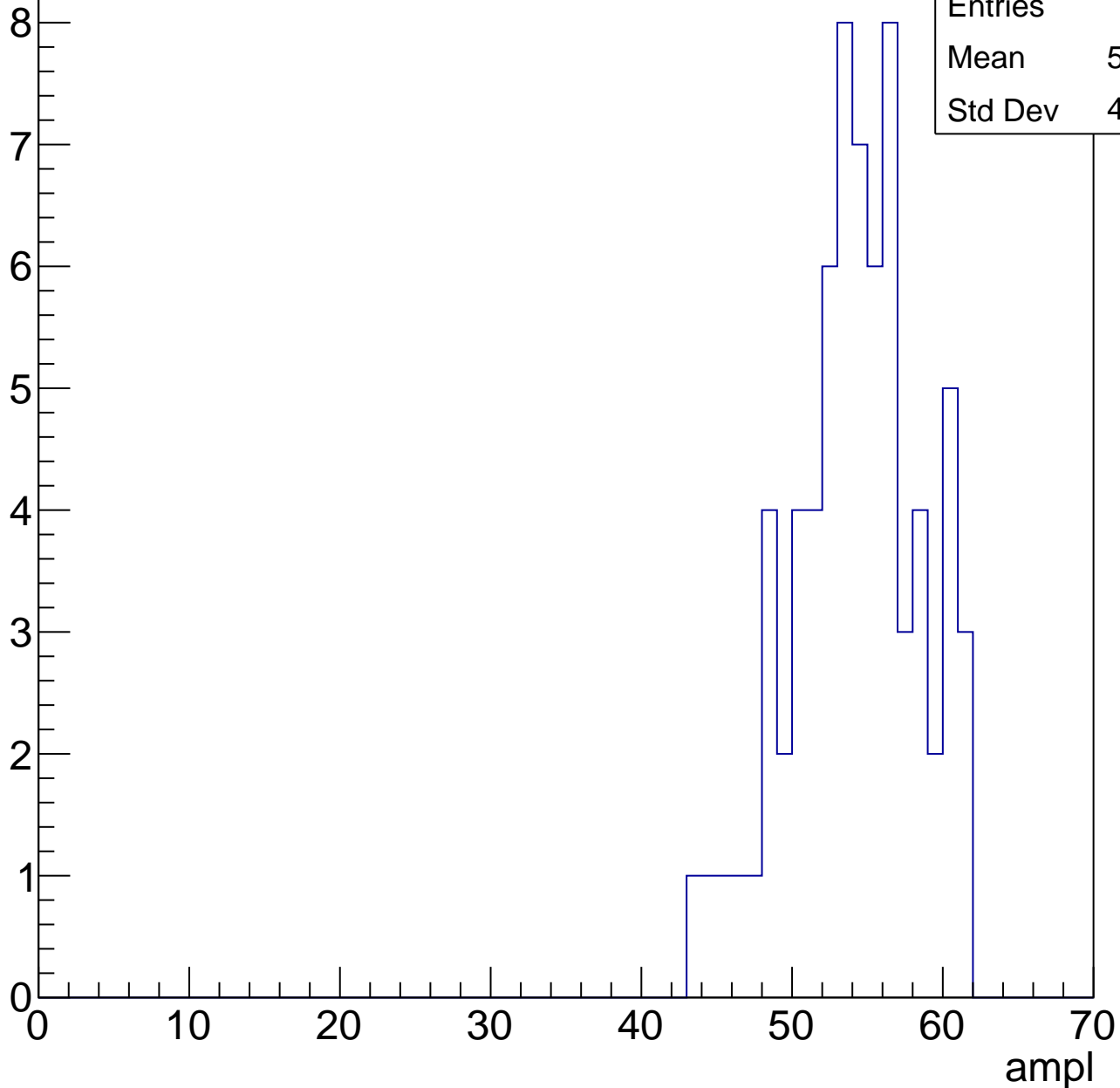
Entries	67
Mean	42.46
Std Dev	14.93



B1L103S, U11-ch92, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	71
Mean	53.73
Std Dev	4.182

B1L103S, U11-ch92, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

6

5

4

3

2

1

0

0

10

20

30

40

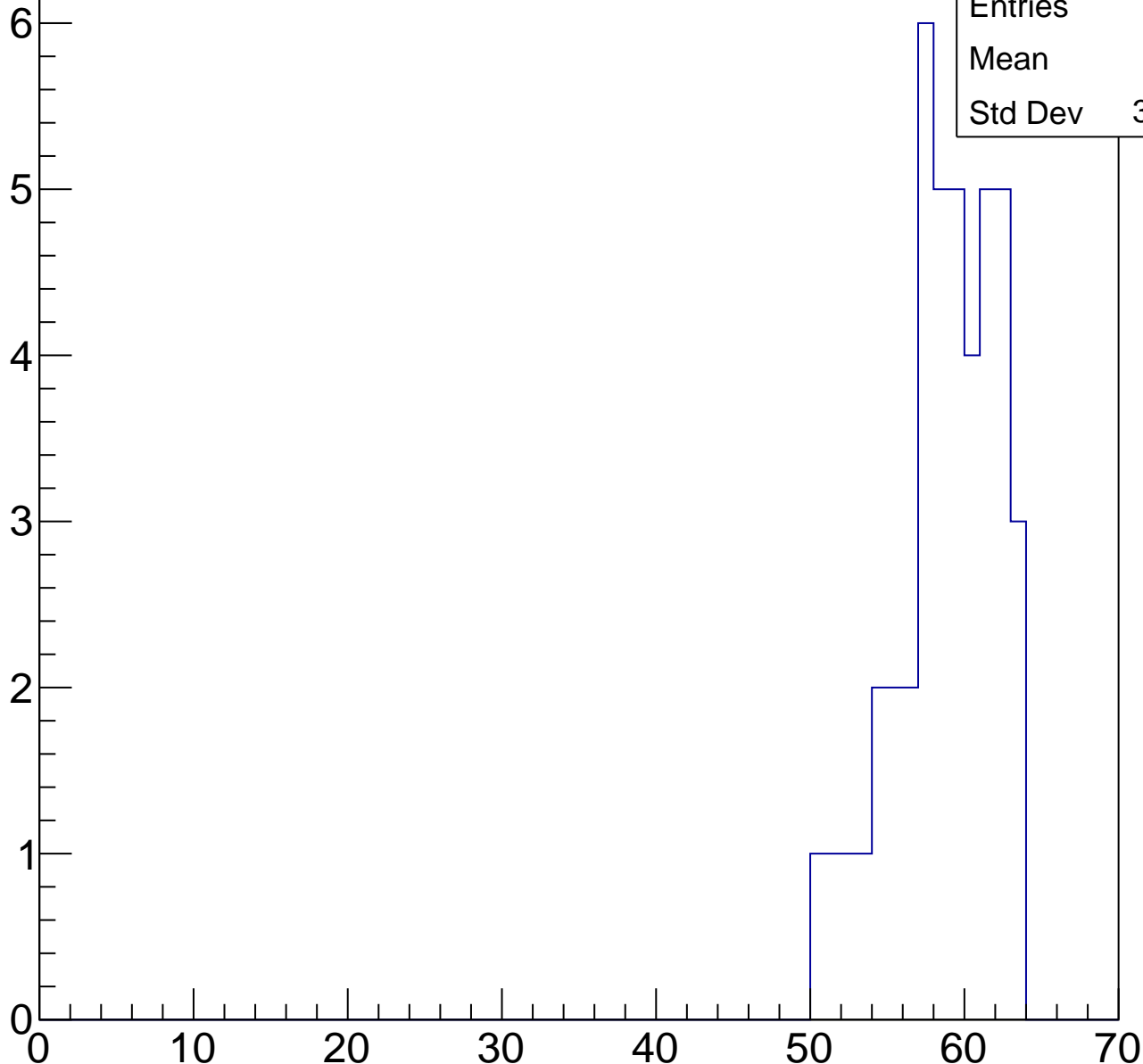
50

60

70

ampl

Entries	43
Mean	58.3
Std Dev	3.253

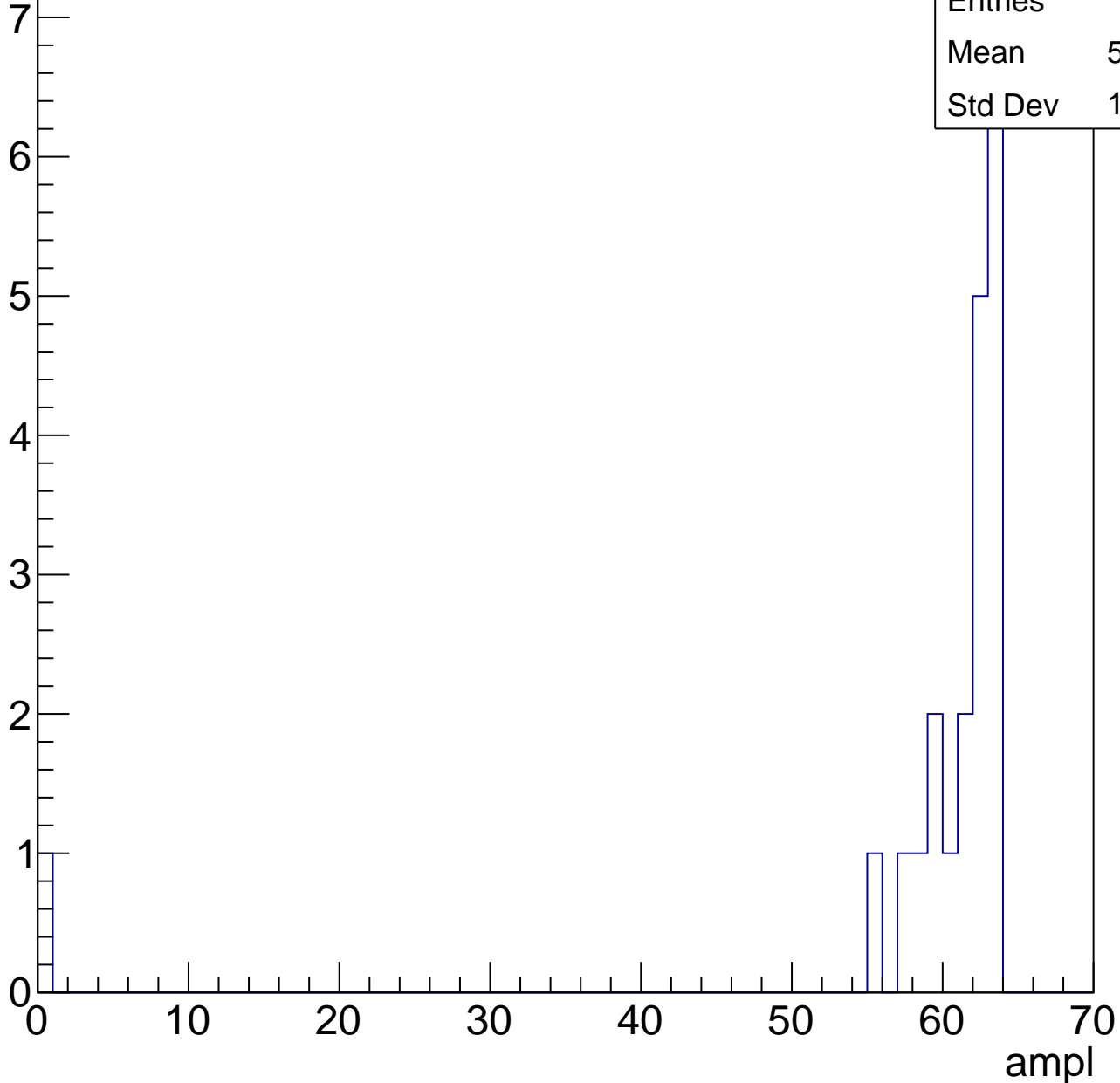


B1L103S, U11-ch92, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	21
Mean	58.14
Std Dev	13.19



B1L103S, U11-ch92, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch93, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	87
Mean	25.31
Std Dev	11.08

Entry

12

10

8

6

4

2

0

0

10

20

30

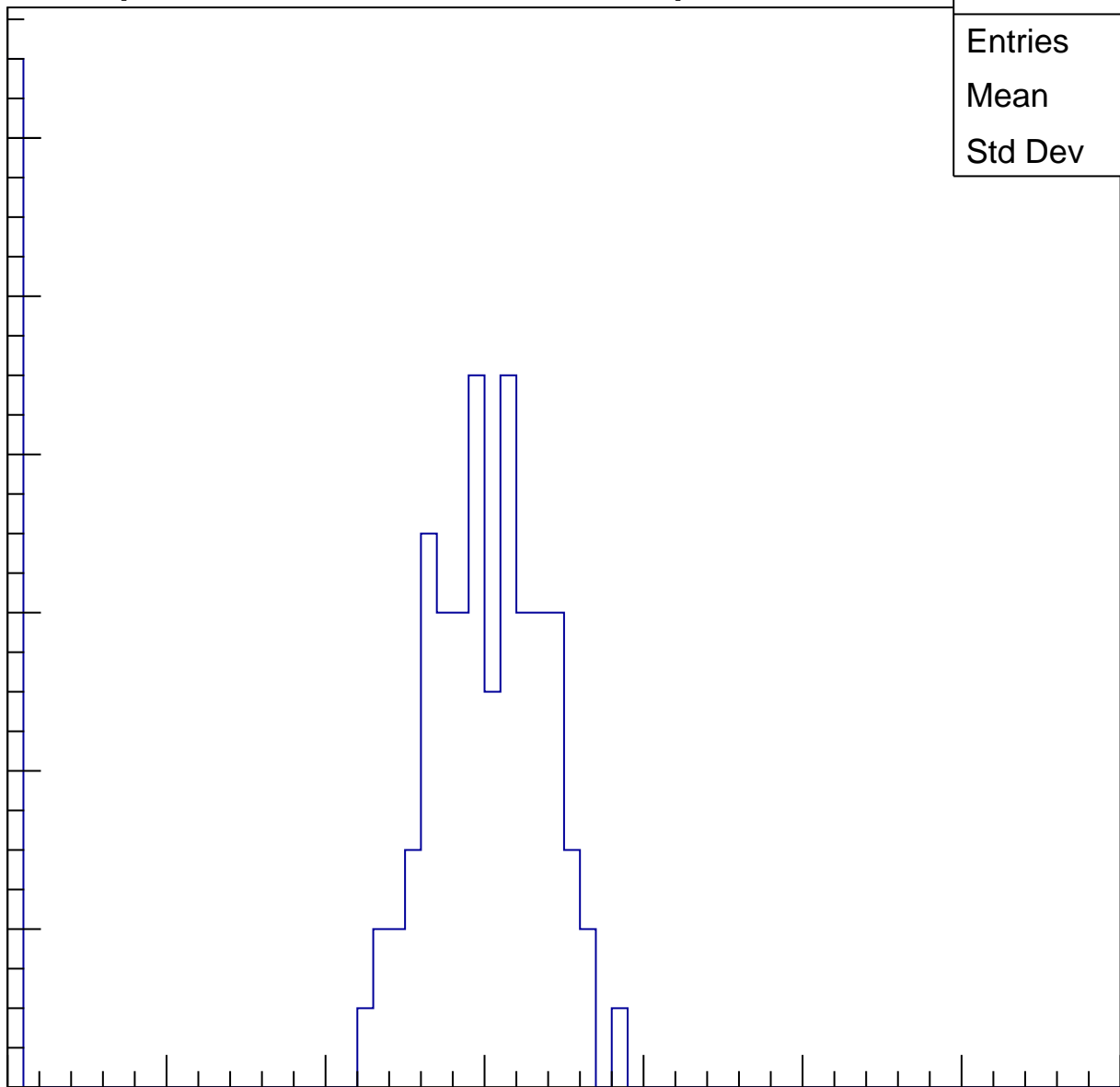
40

50

60

70

ampl

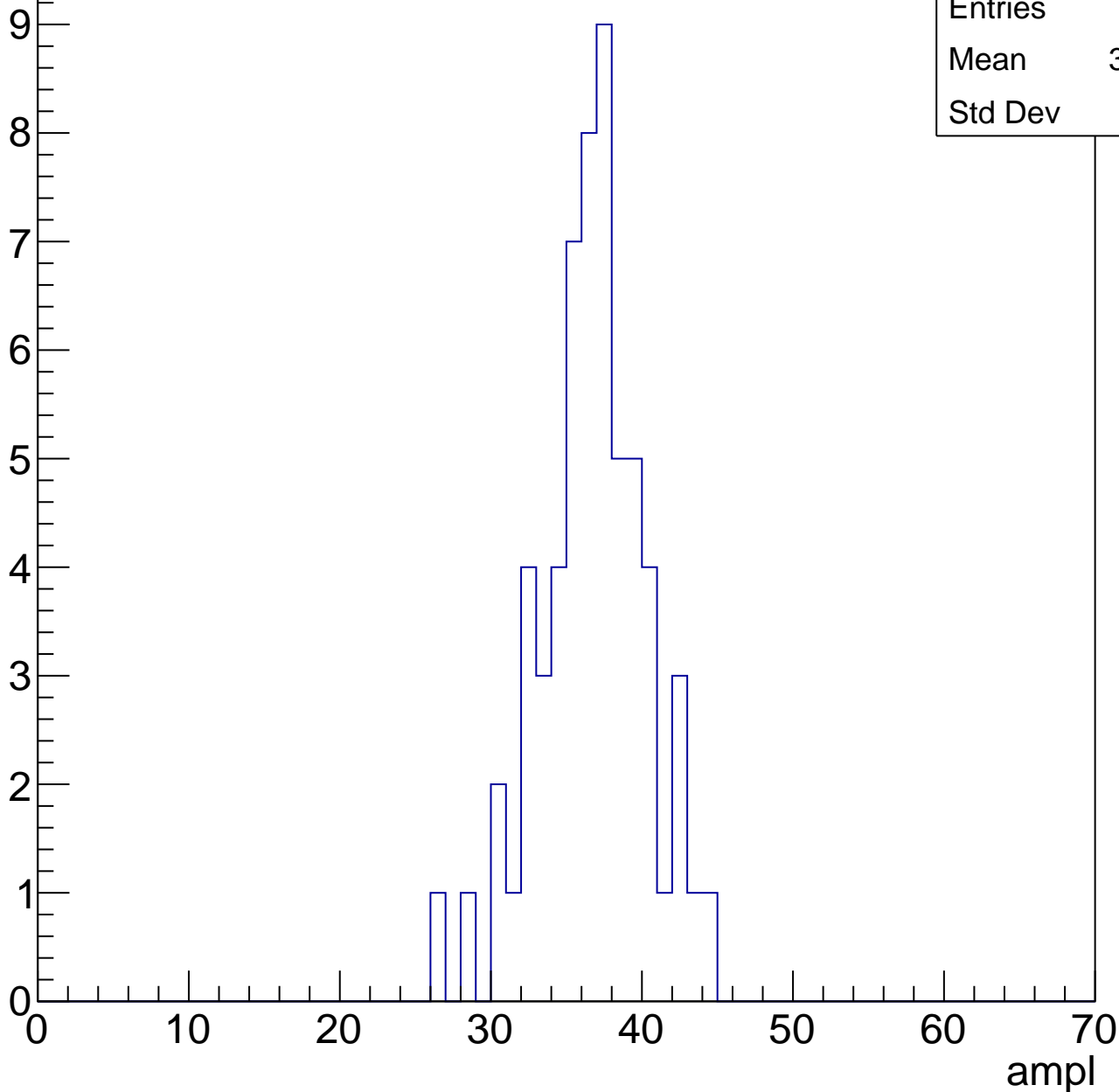


B1L103S, U11-ch93, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	36.22
Std Dev	3.55

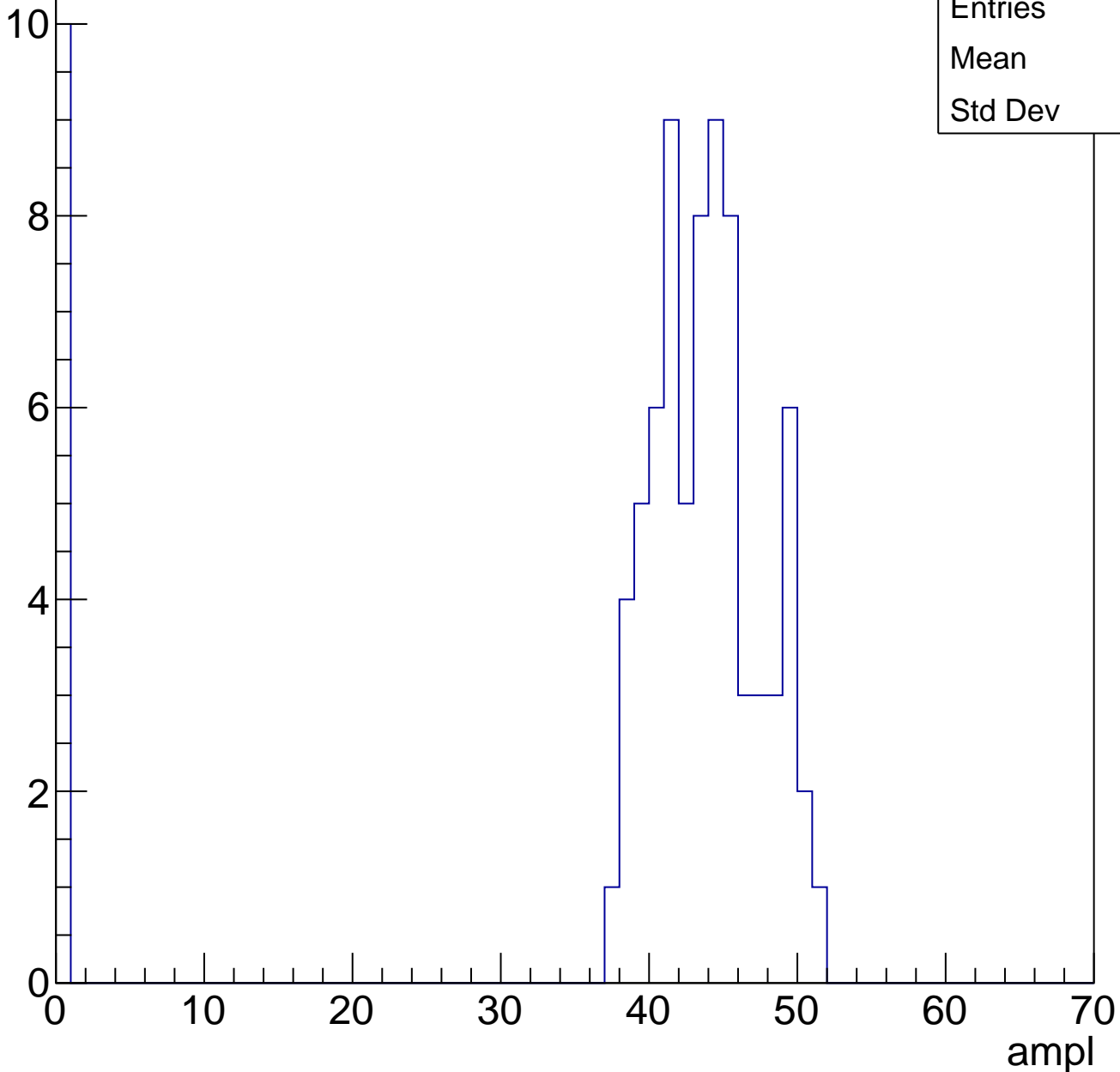


B1L103S, U11-ch93, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	83
Mean	38.2
Std Dev	14.5

Entry

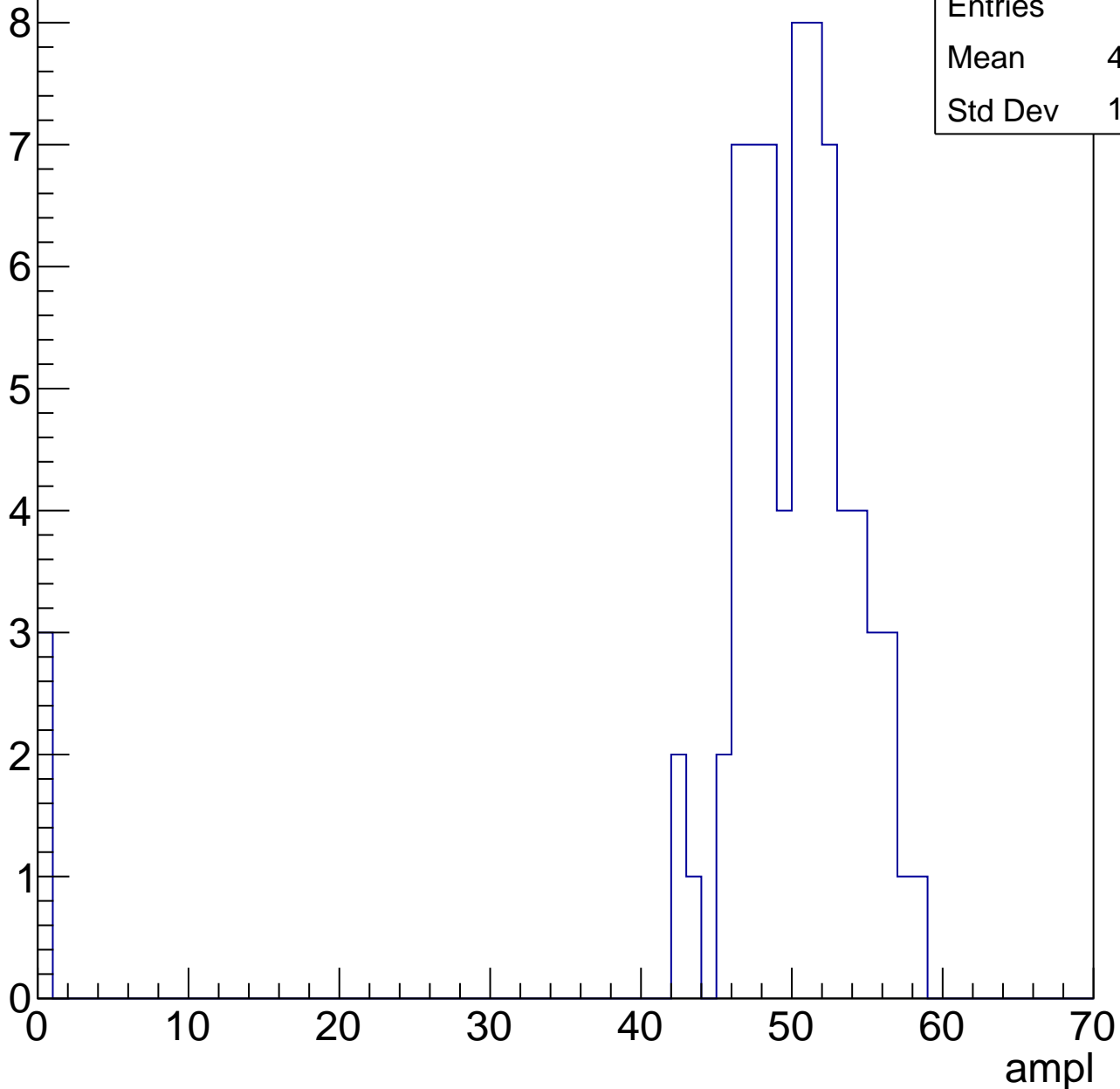


B1L103S, U11-ch93, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	47.89
Std Dev	10.57

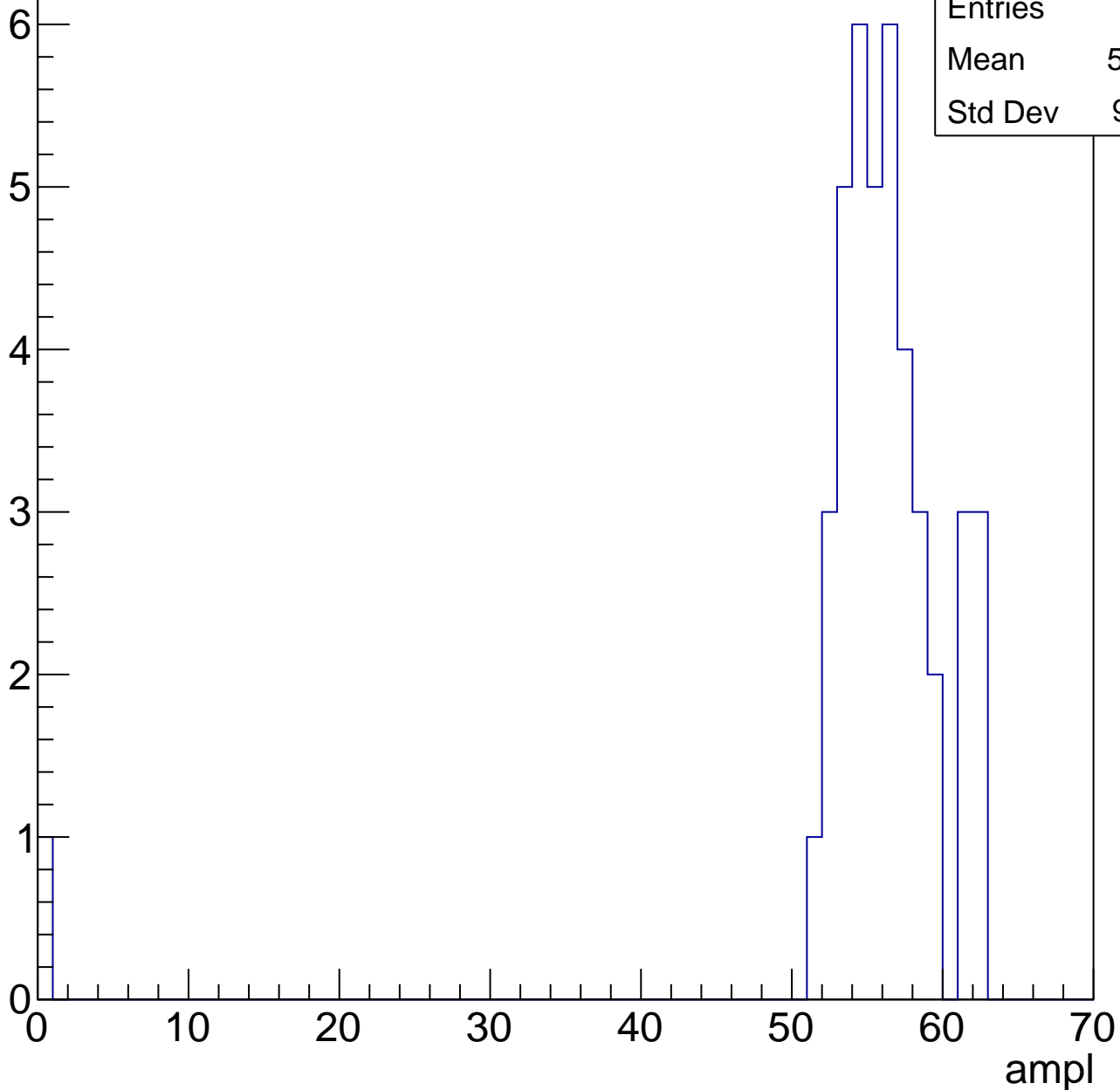


B1L103S, U11-ch93, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	42
Mean	54.67
Std Dev	9.031



B1L103S, U11-ch93, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

8

6

4

2

0

0

10

20

30

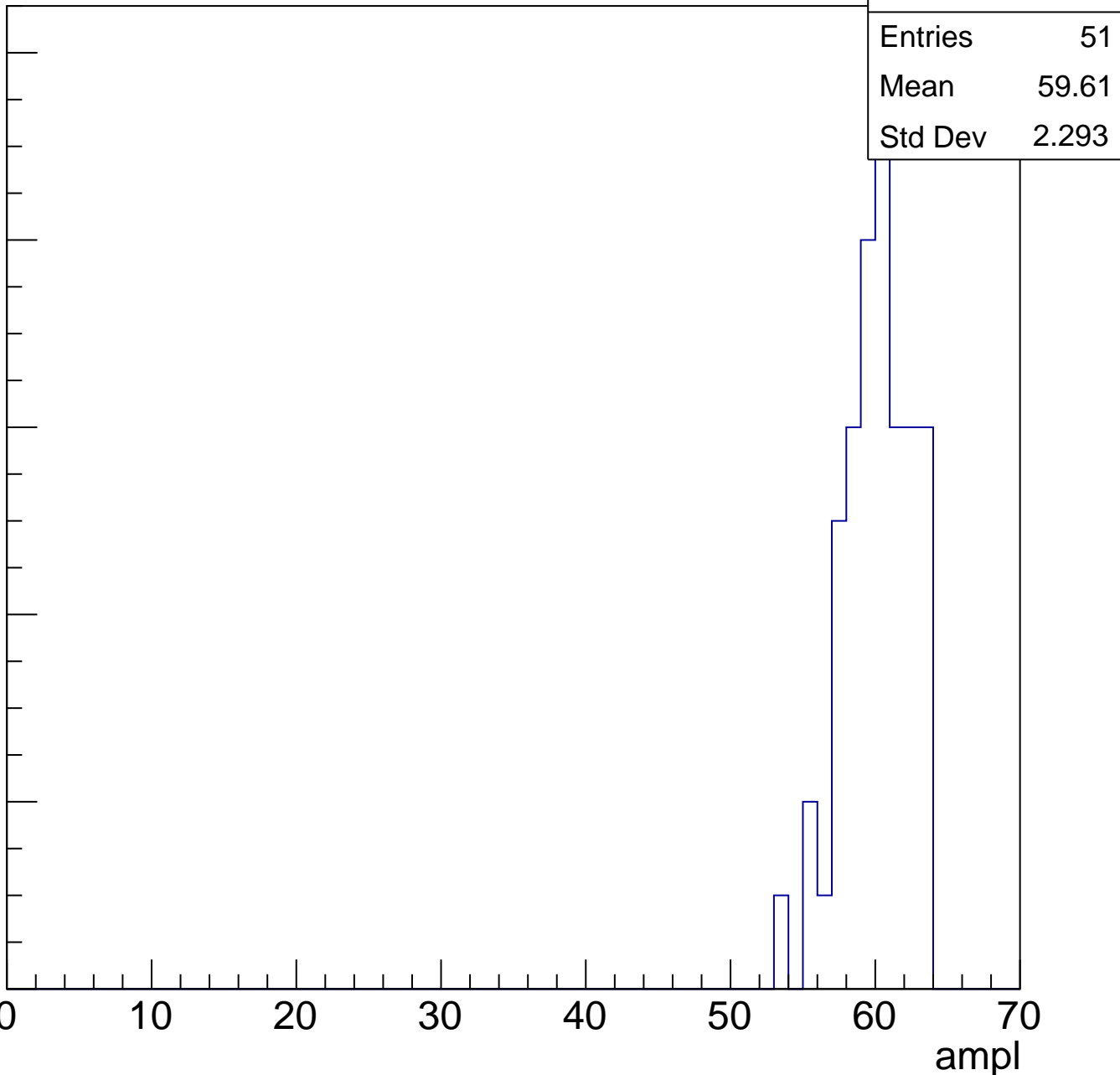
40

50

60

ampl

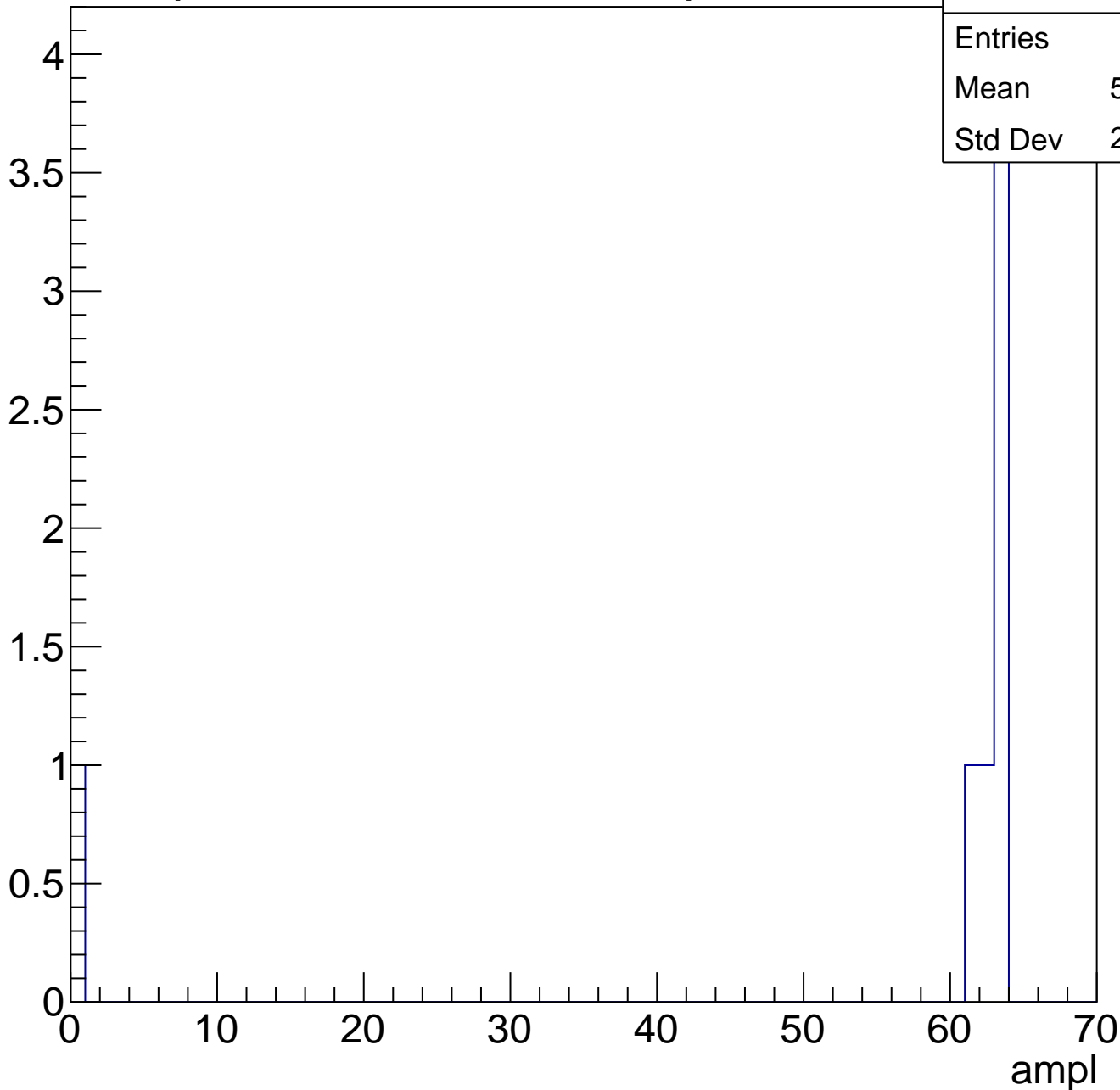
Entries	51
Mean	59.61
Std Dev	2.293



B1L103S, U11-ch93, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch93, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

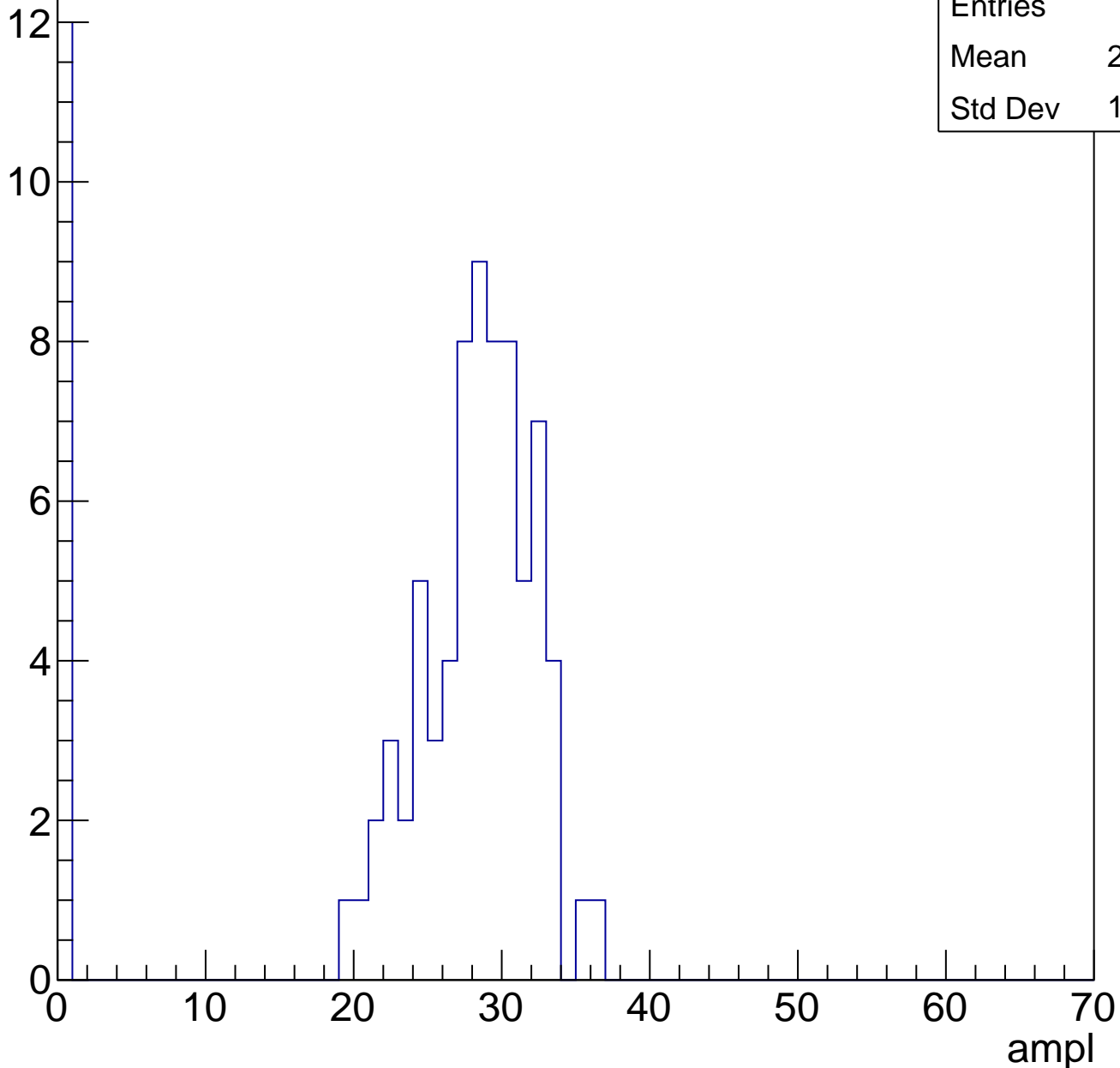
Entries	19
Mean	0
Std Dev	0

B1L103S, U11-ch94, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	84
Mean	23.98
Std Dev	10.35

Entry



B1L103S, U11-ch94, adc1

calib_packv5_041523_1651.root, FC#0, port C2

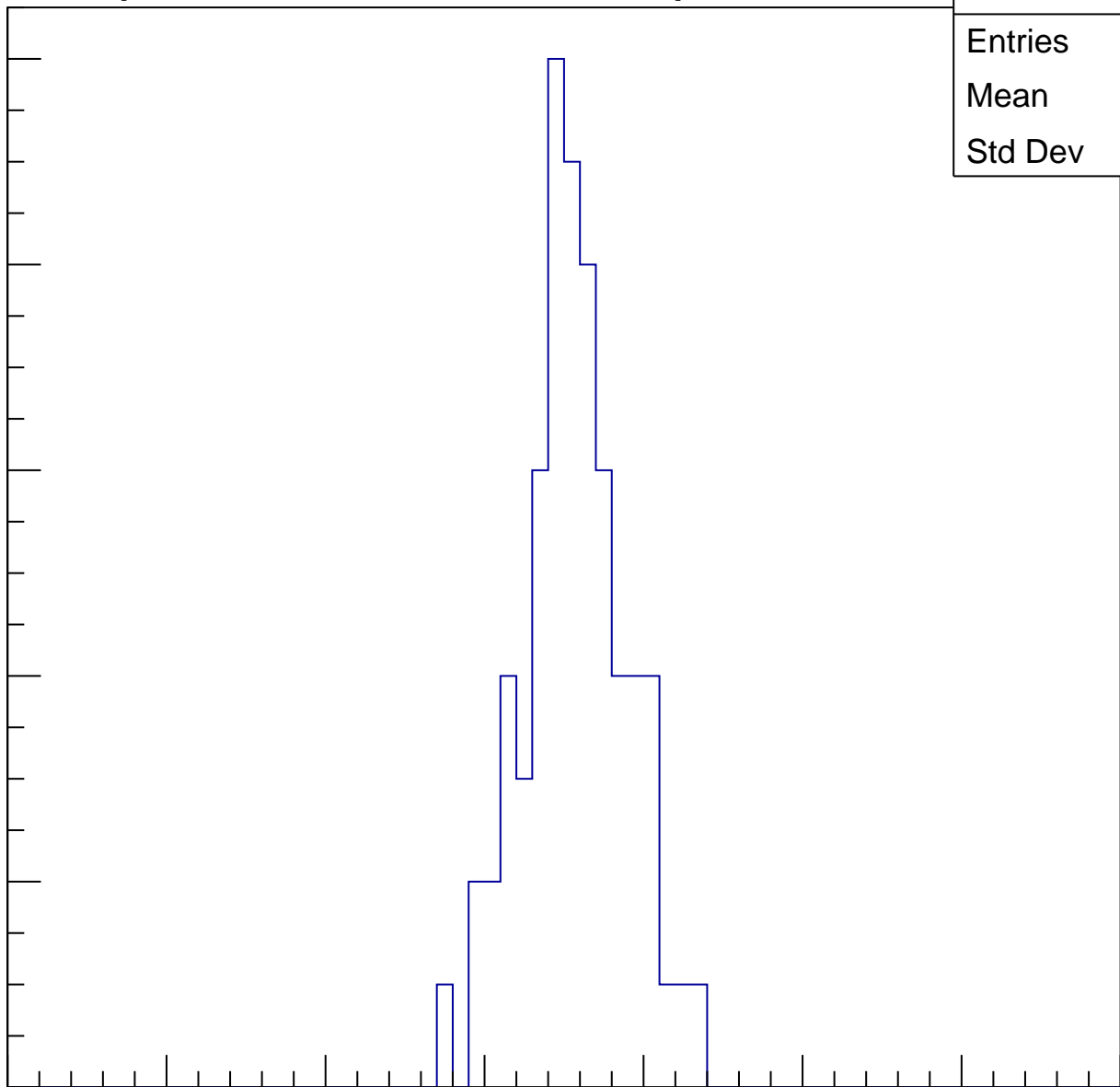
Entries	66
Mean	35.18
Std Dev	3.233

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

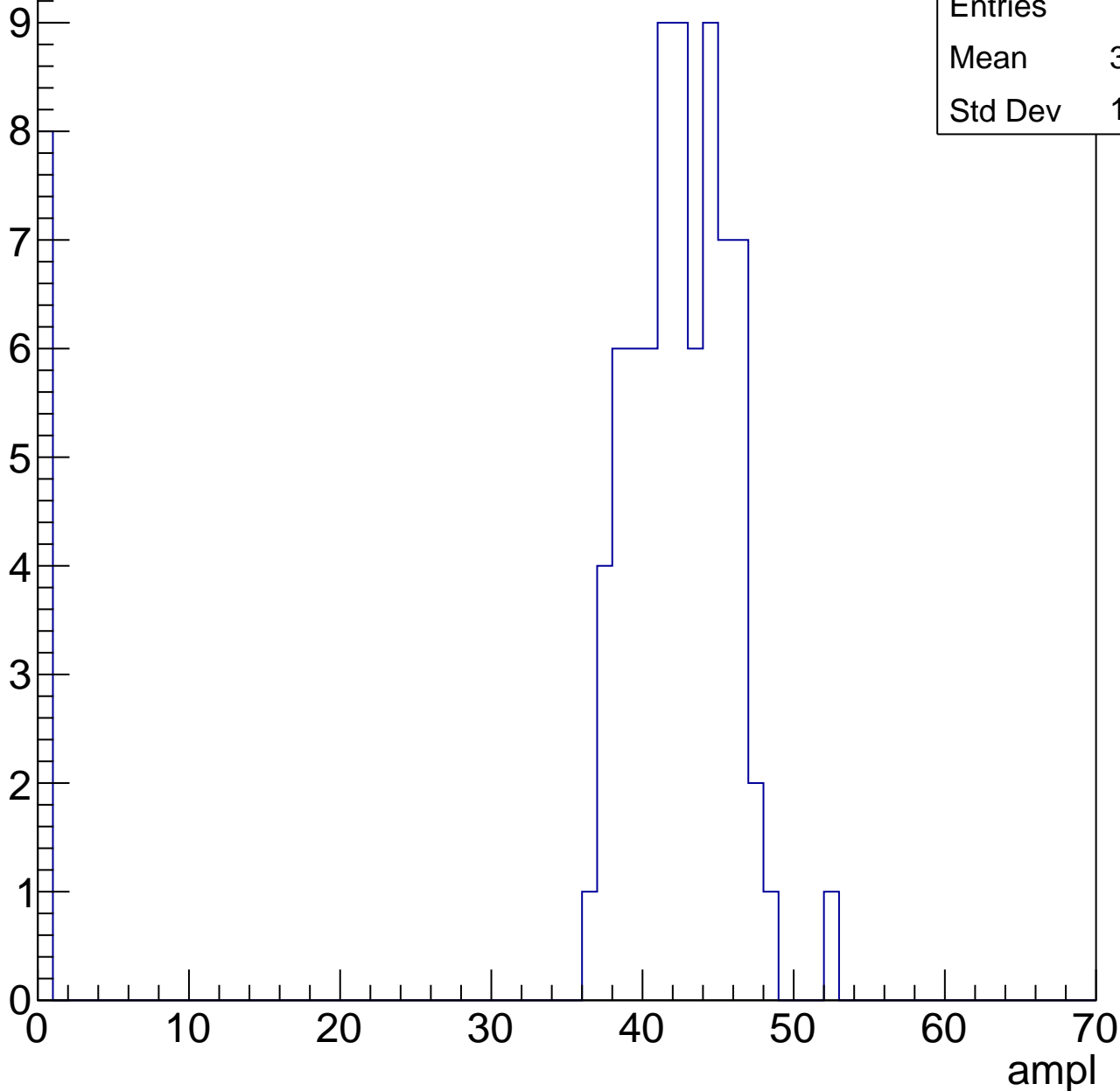


B1L103S, U11-ch94, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	82
Mean	38.02
Std Dev	12.85

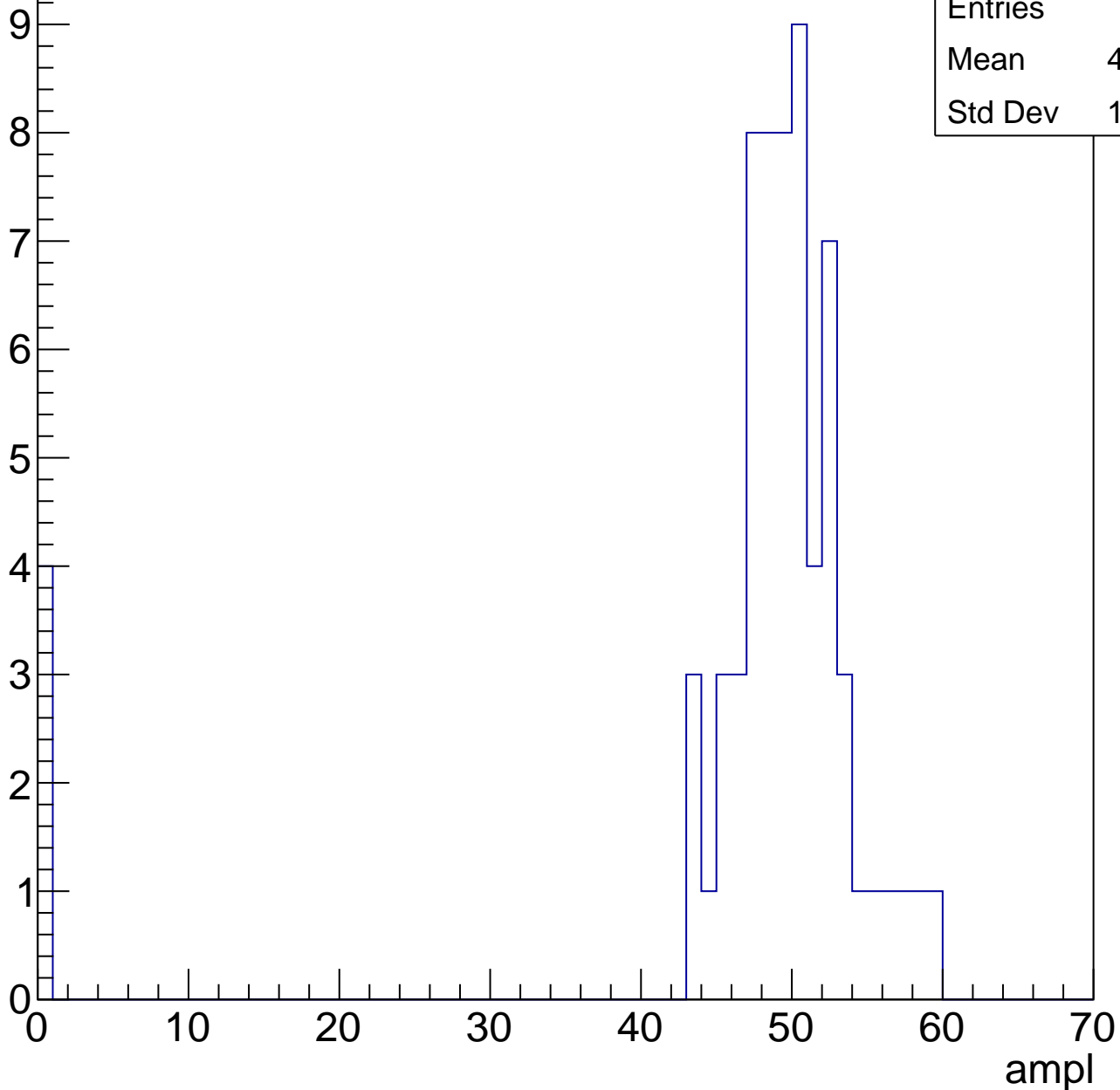


B1L103S, U11-ch94, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	46.48
Std Dev	12.17

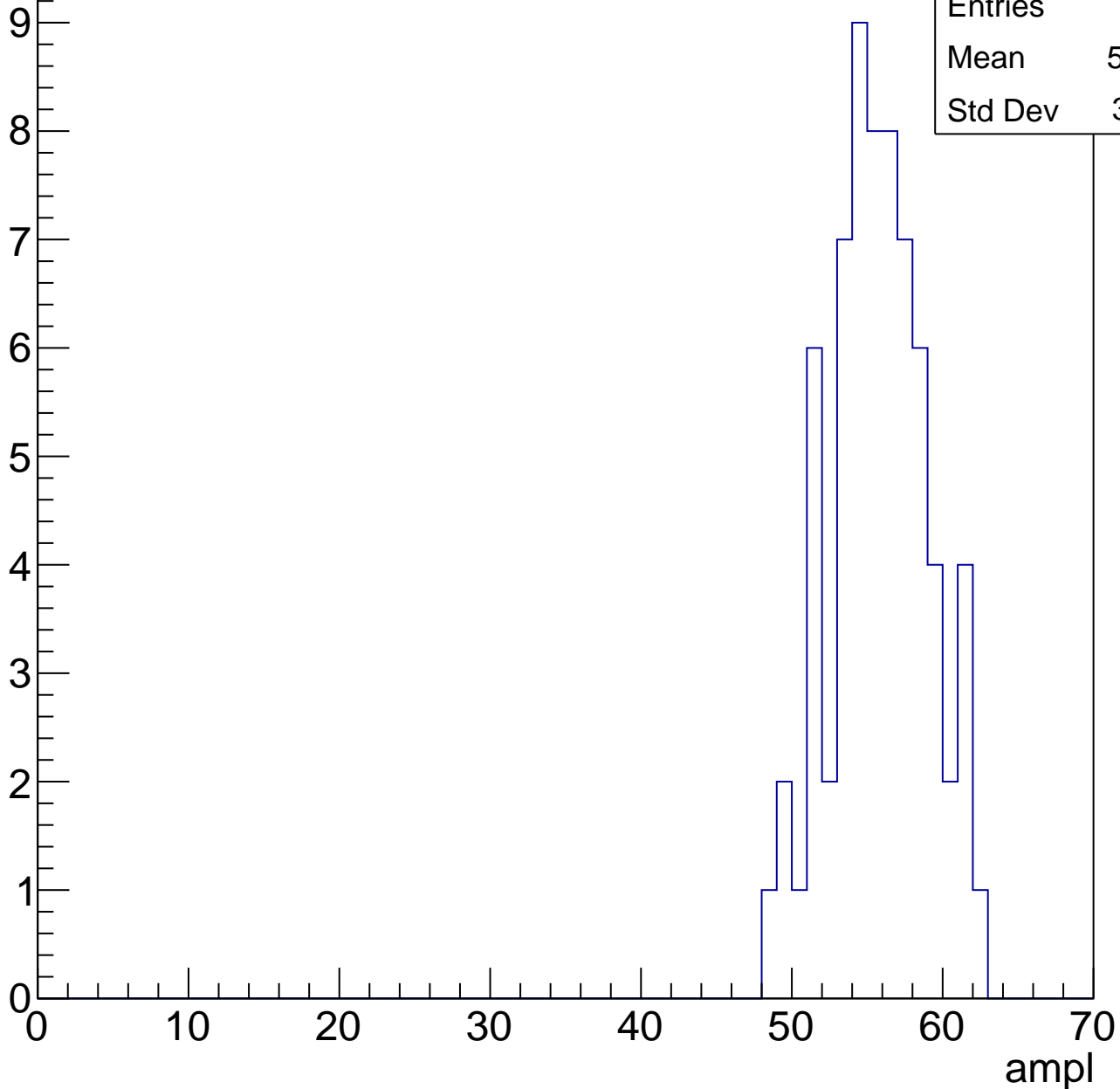


B1L103S, U11-ch94, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

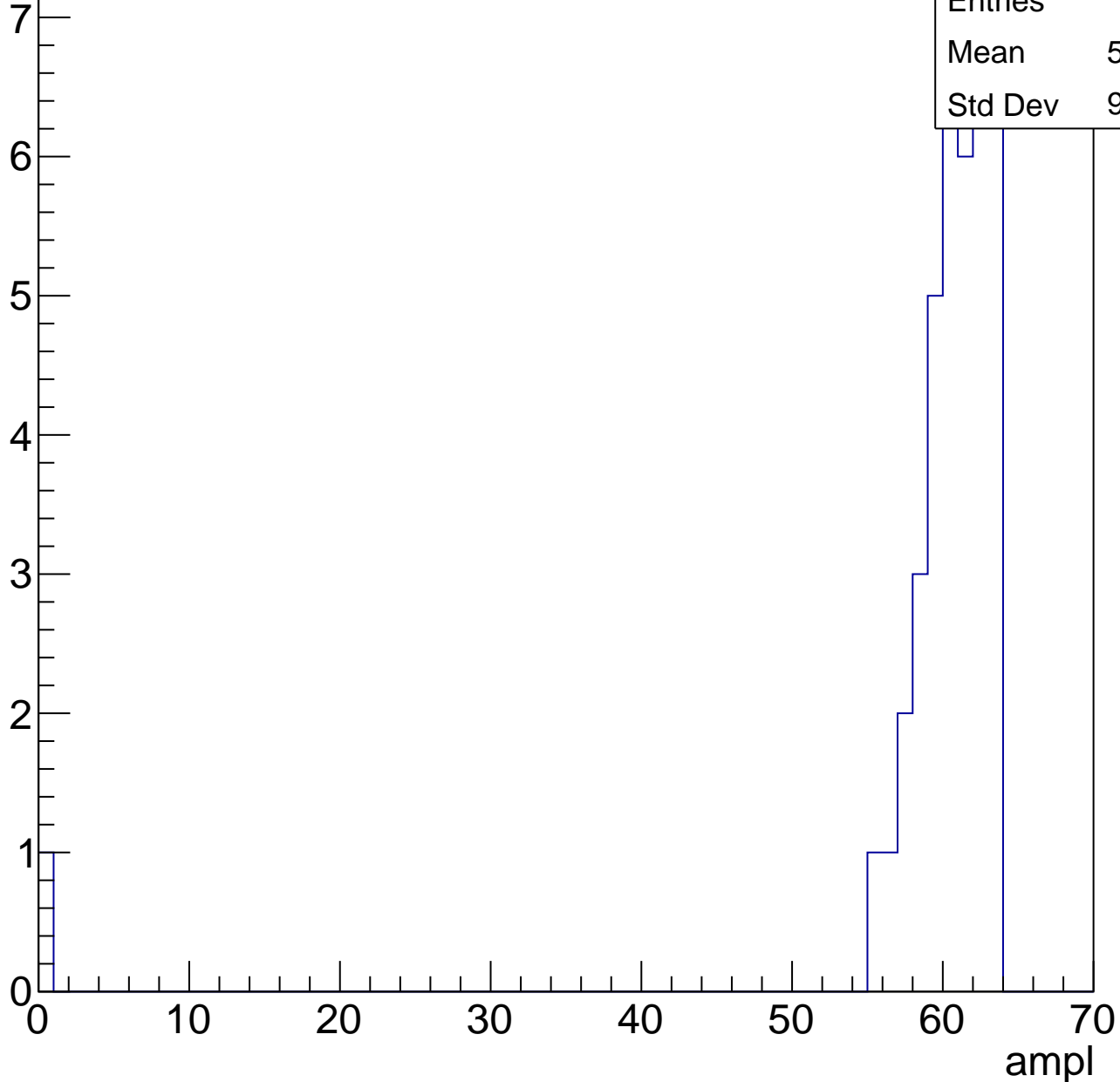
Entries	68
Mean	55.29
Std Dev	3.181



B1L103S, U11-ch94, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch94, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

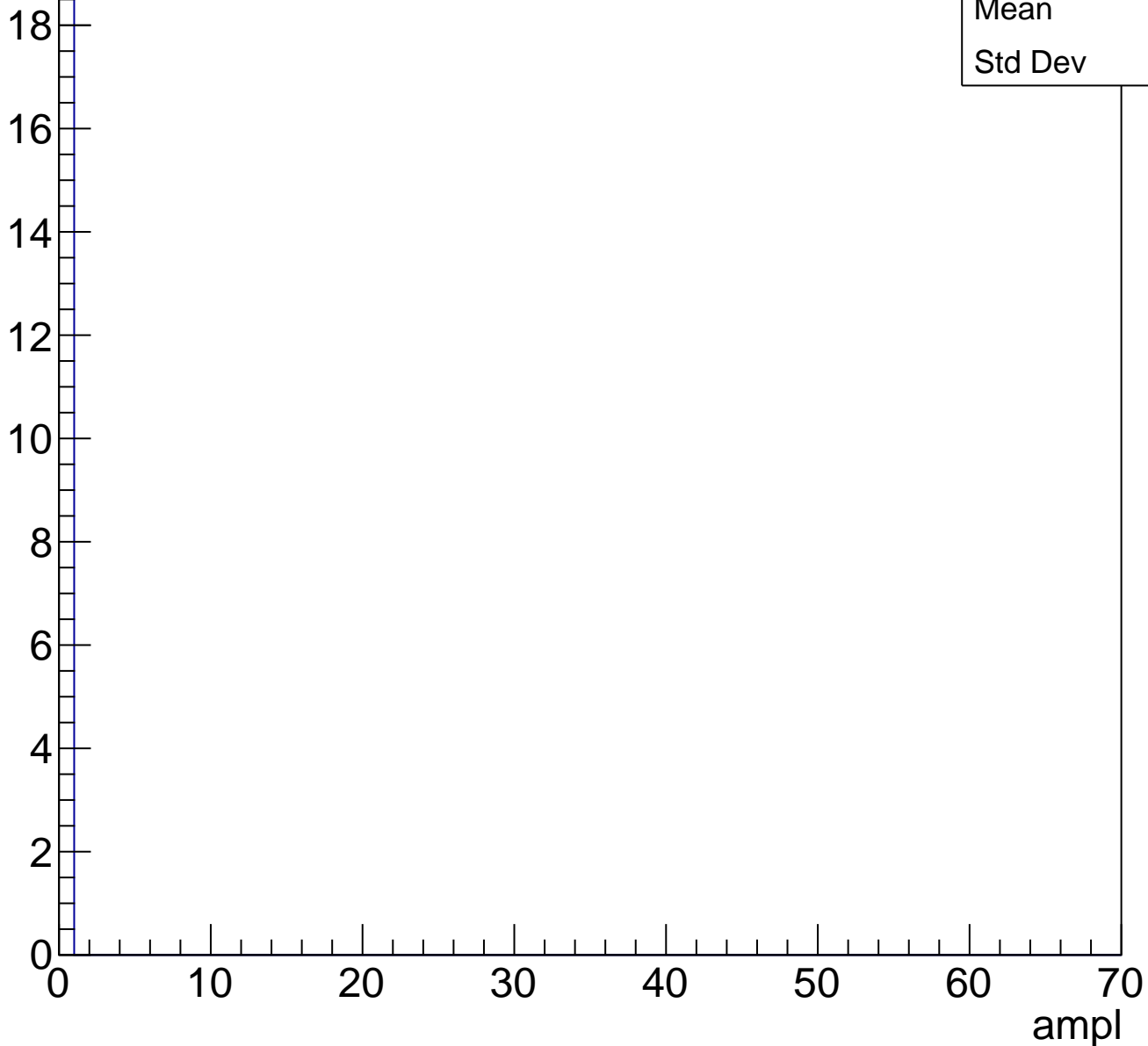


B1L103S, U11-ch94, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	0
Std Dev	0

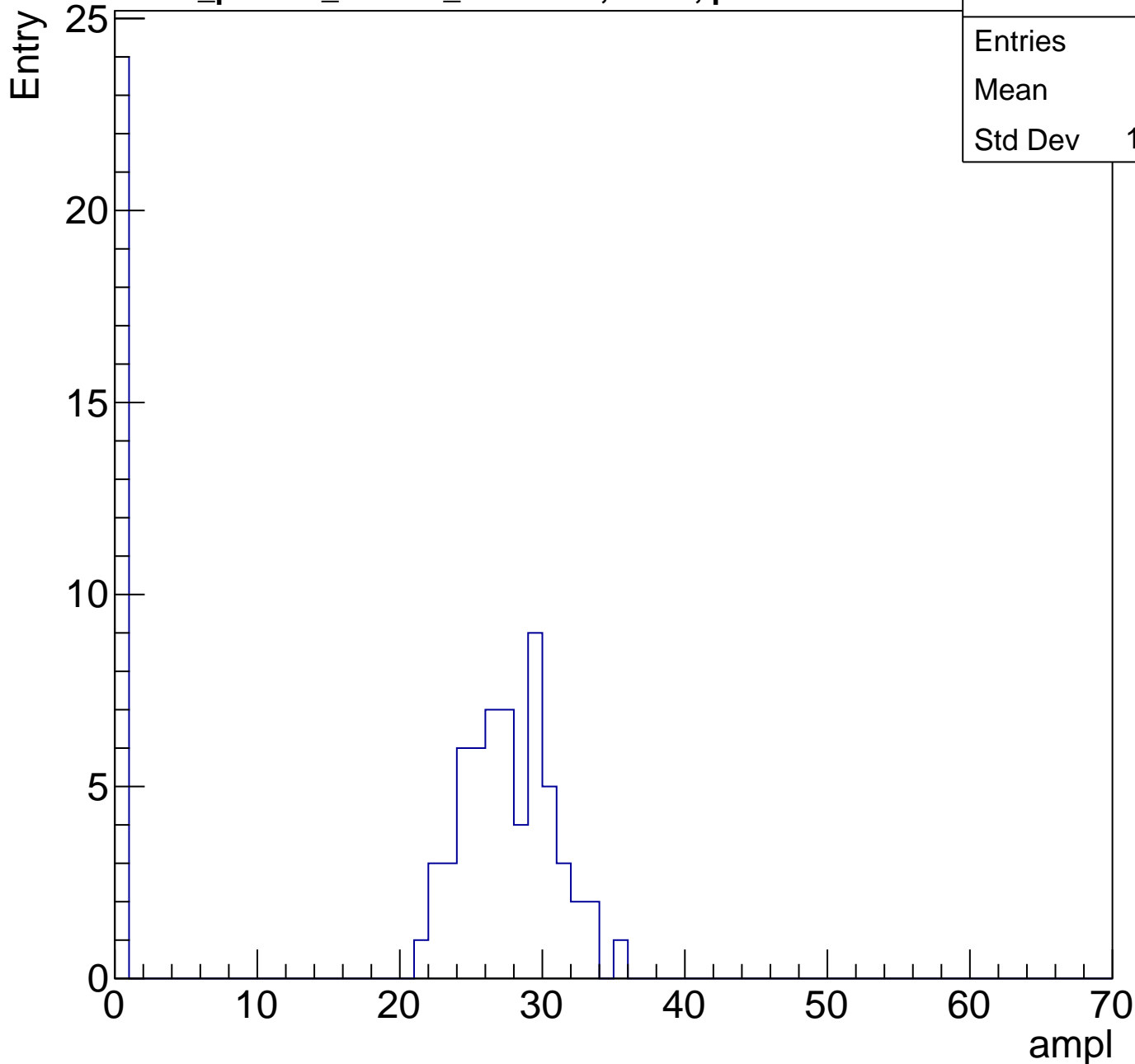
Entry



B1L103S, U11-ch95, adc0

calib_packv5_041523_1651.root, FC#0, port C2

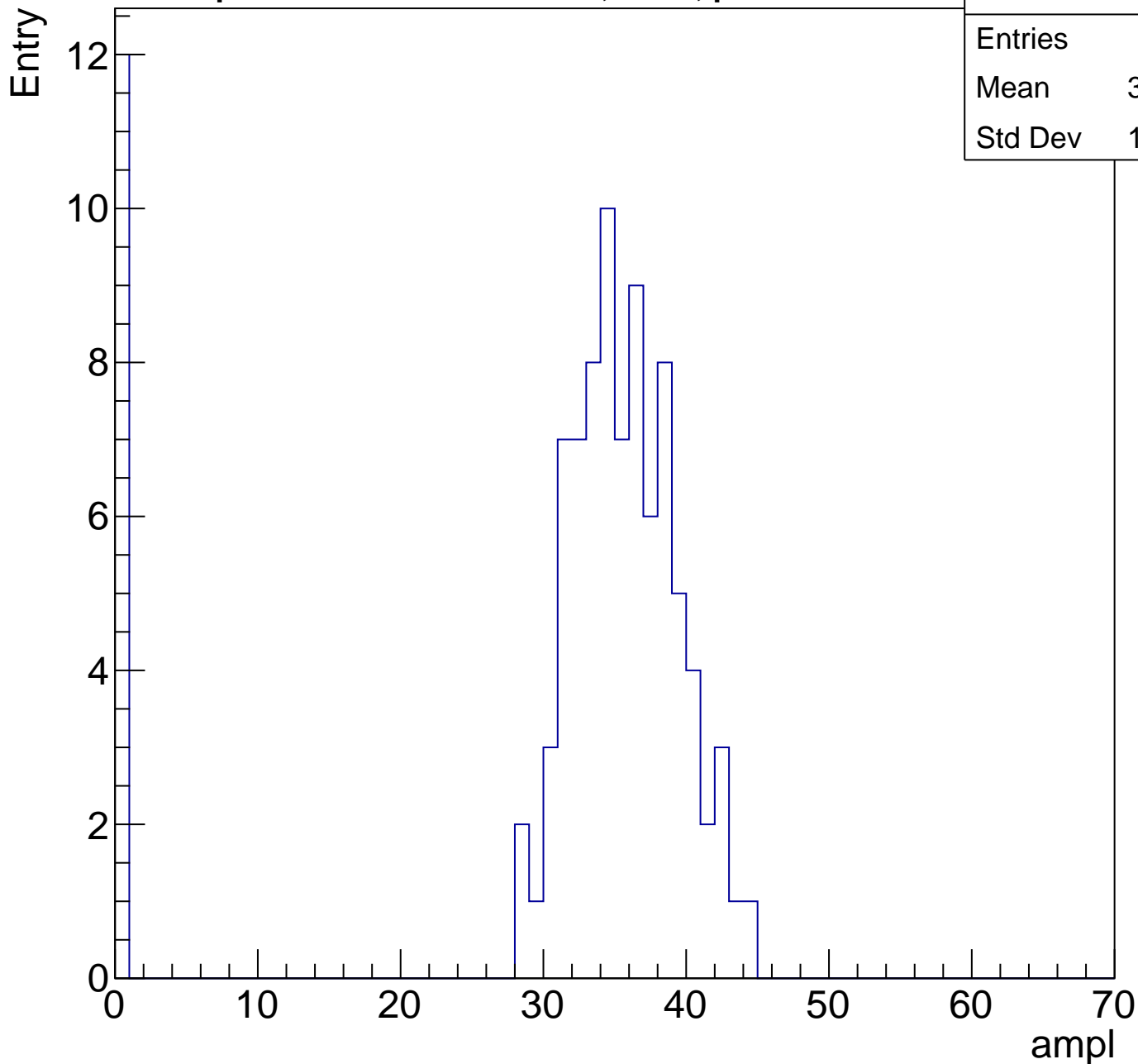
Entries	83
Mean	19.3
Std Dev	12.58



B1L103S, U11-ch95, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	96
Mean	30.89
Std Dev	12.14

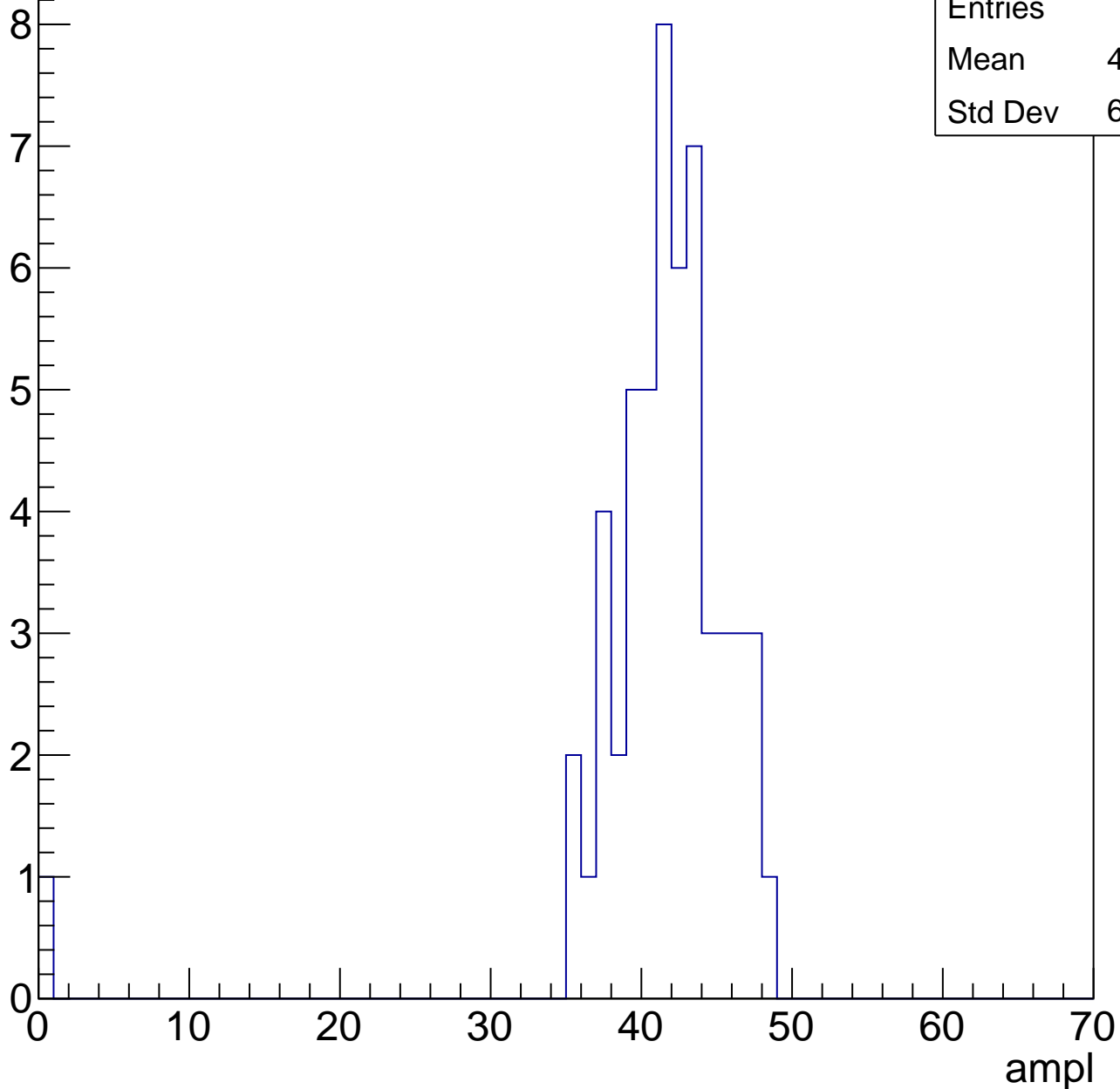


B1L103S, U11-ch95, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	40.74
Std Dev	6.415

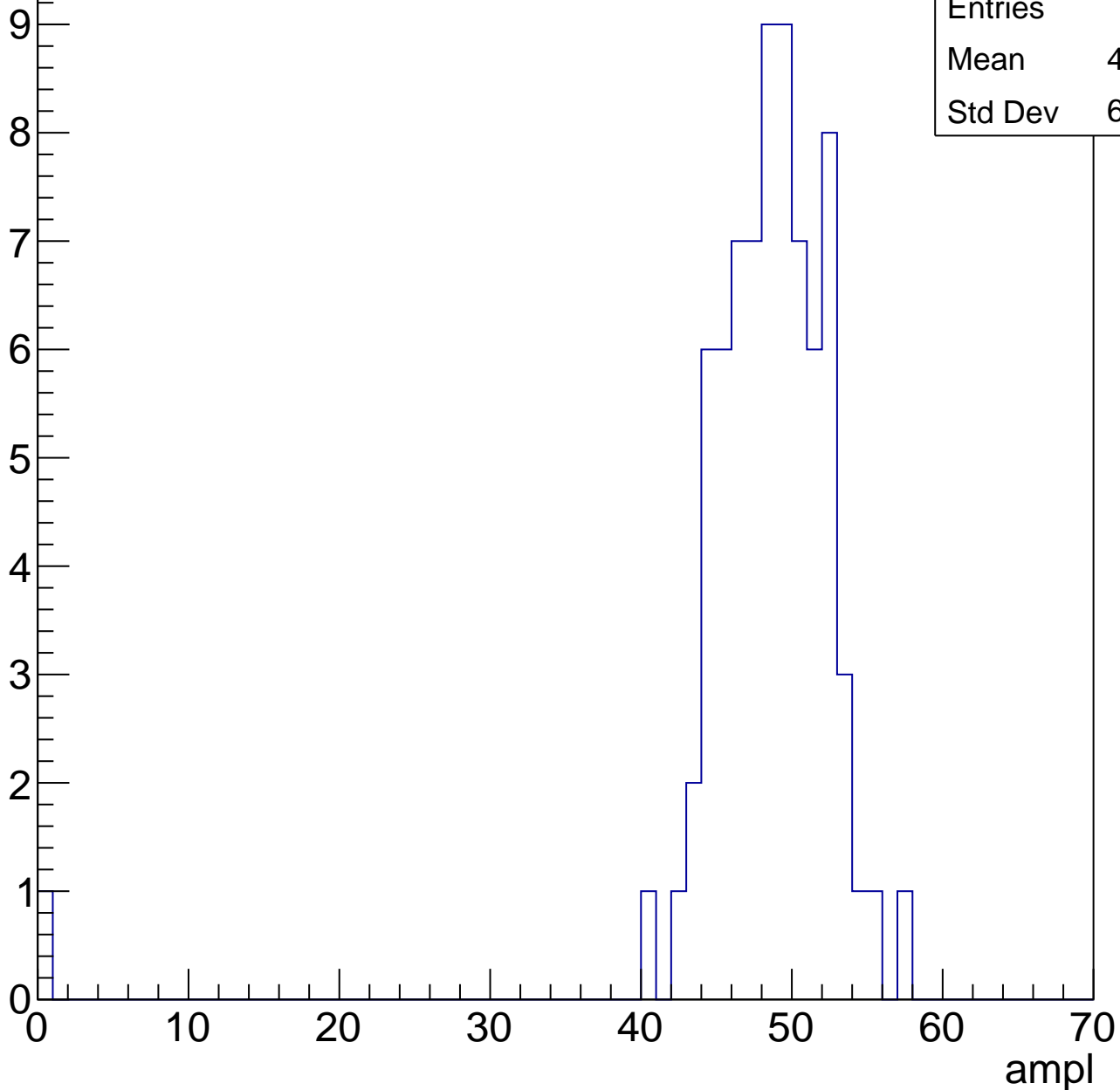


B1L103S, U11-ch95, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	47.67
Std Dev	6.377

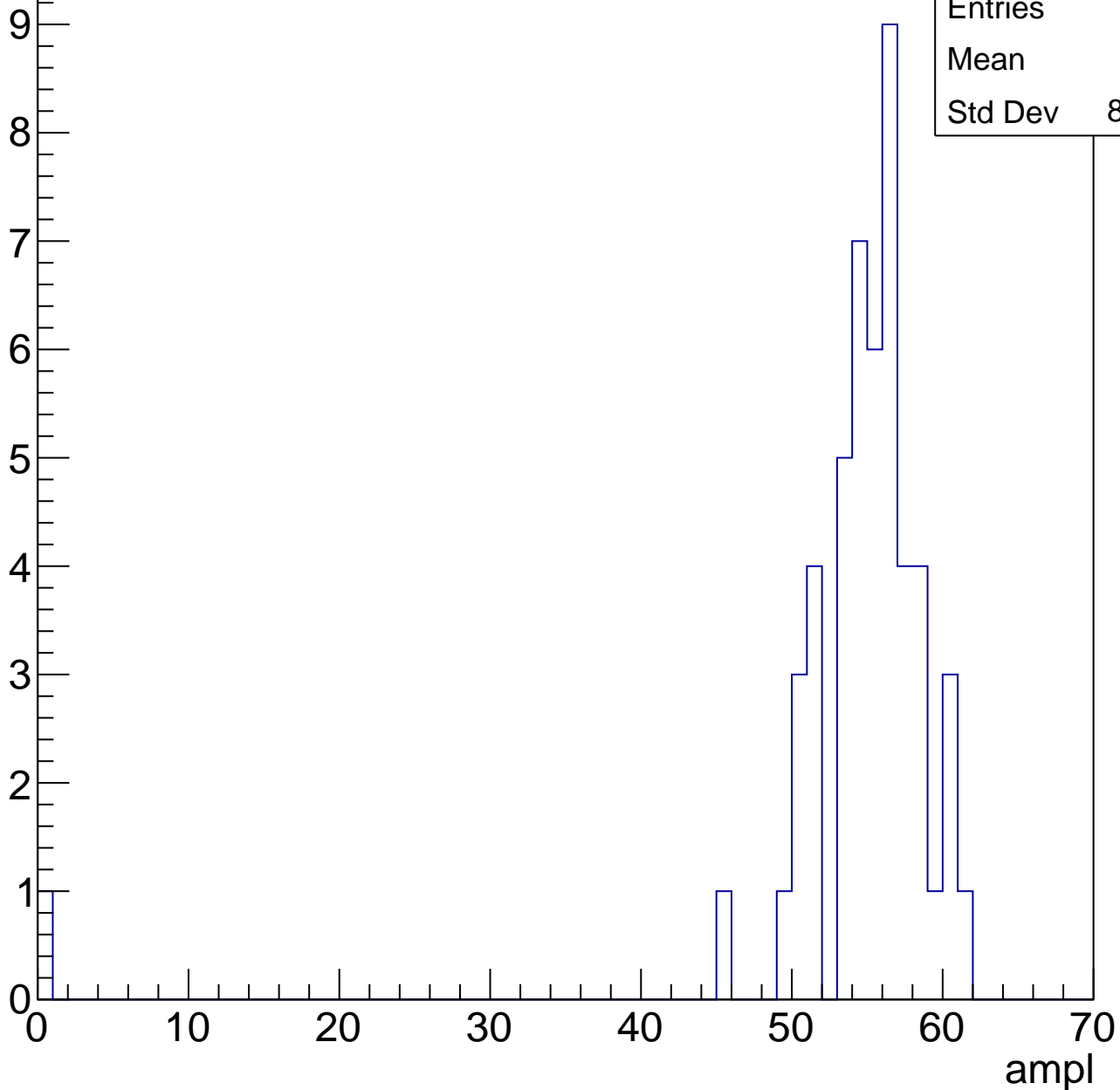


B1L103S, U11-ch95, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

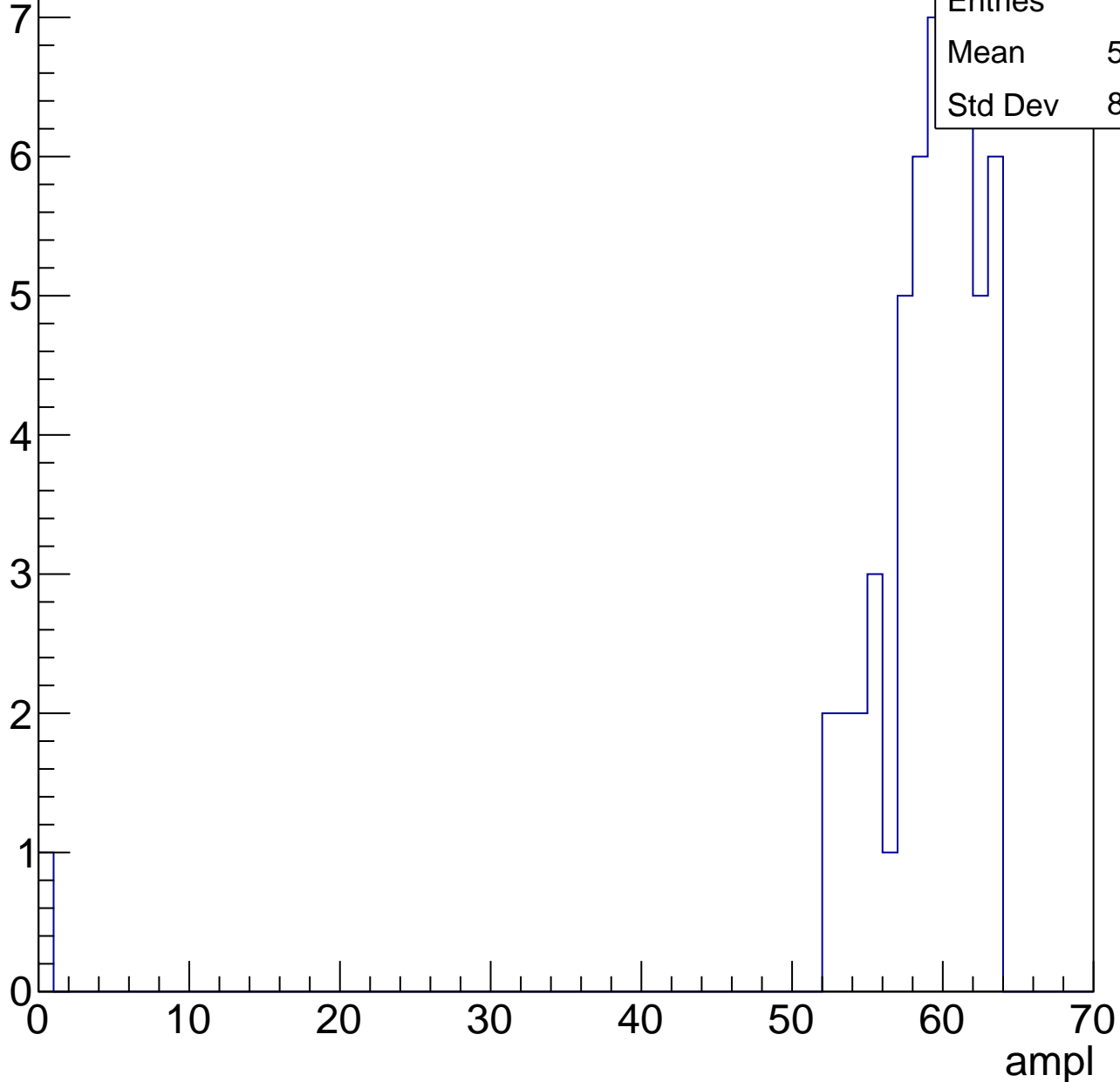
Entries	50
Mean	53.7
Std Dev	8.283



B1L103S, U11-ch95, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

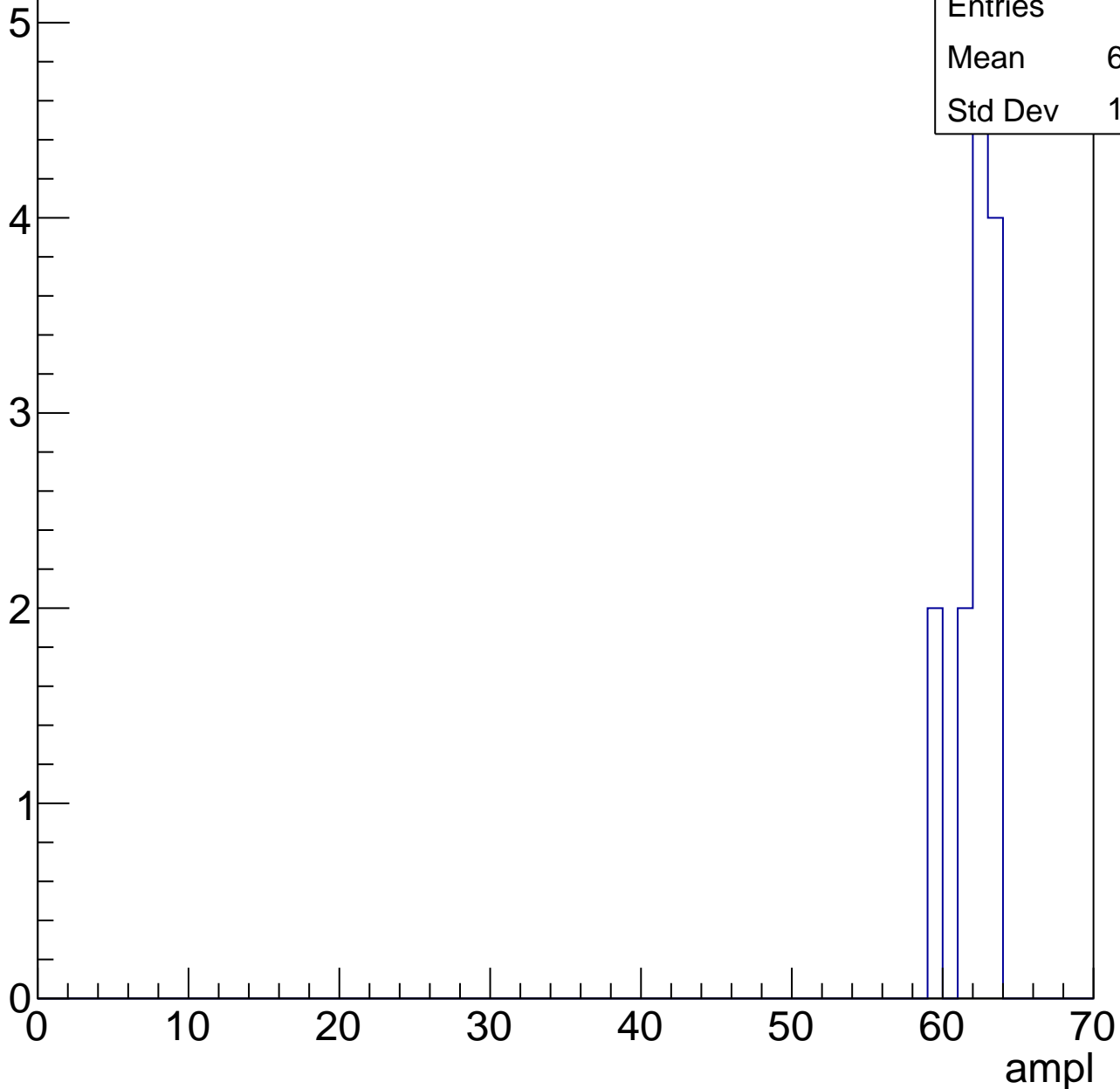


B1L103S, U11-ch95, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	13
Mean	61.69
Std Dev	1.323



B1L103S, U11-ch95, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch96, adc0

calib_packv5_041523_1651.root, FC#0, port C2

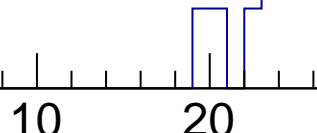
Entries	76
Mean	23.57
Std Dev	11.74

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

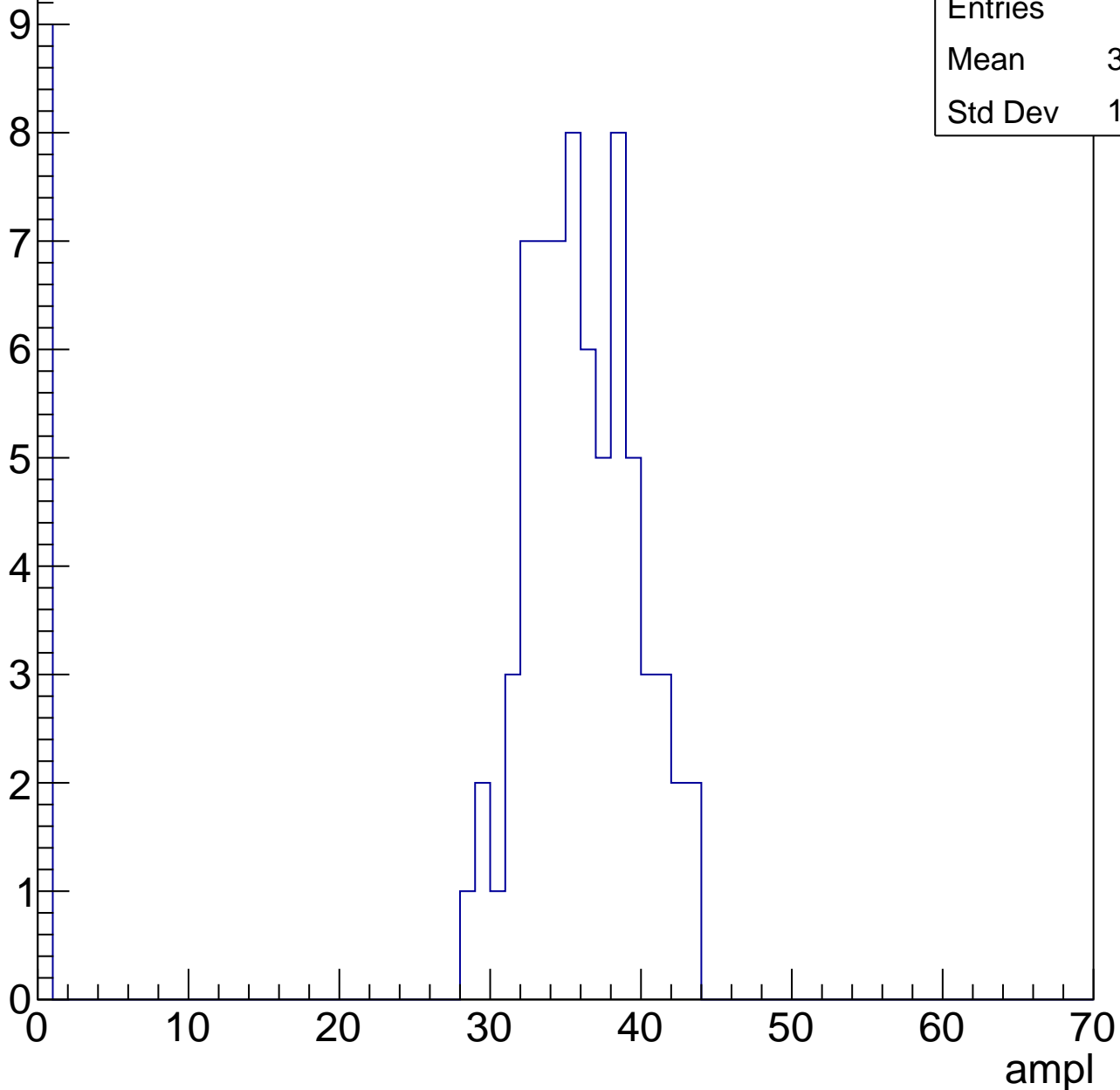


B1L103S, U11-ch96, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	79
Mean	31.58
Std Dev	11.79

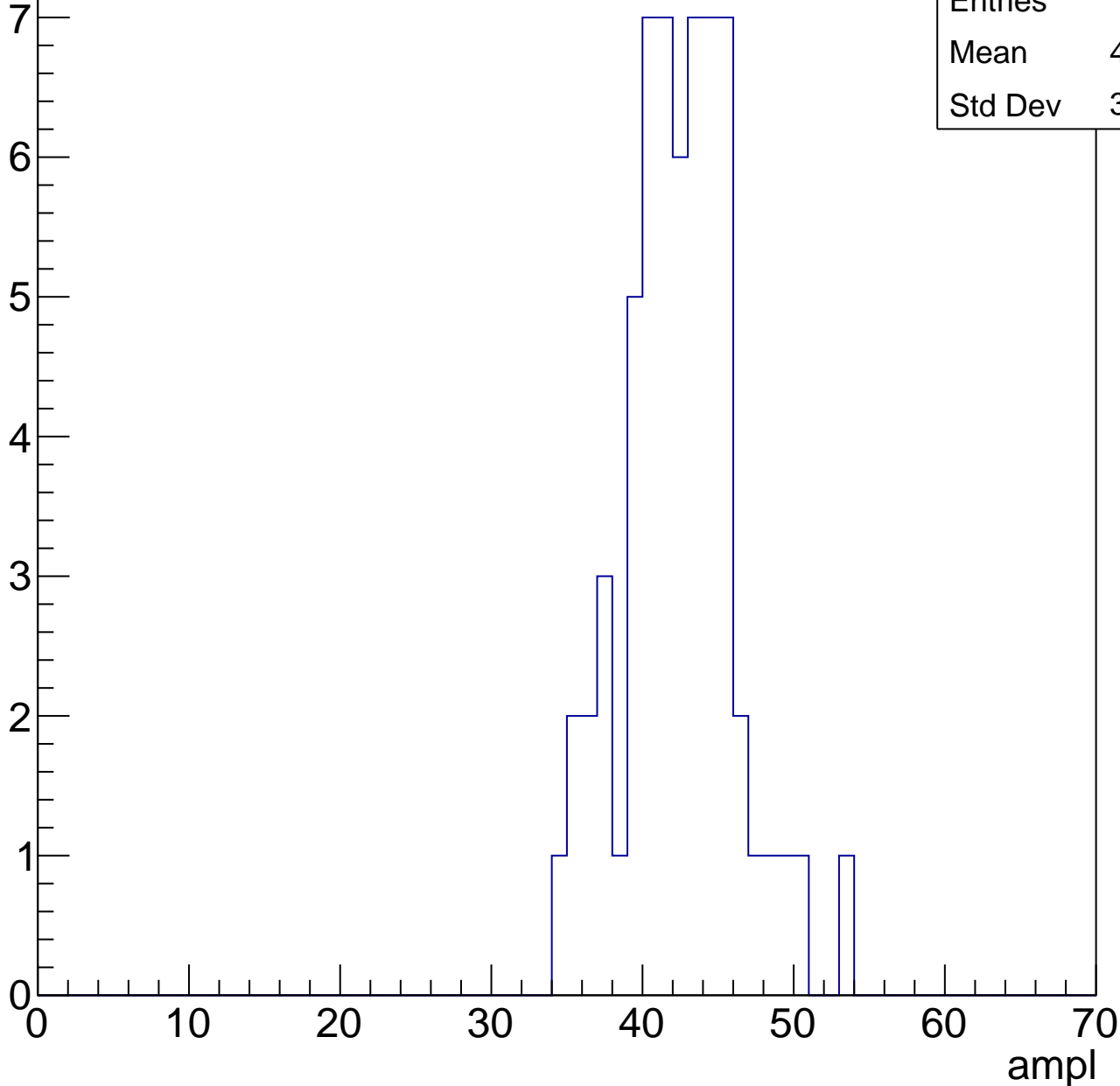


B1L103S, U11-ch96, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

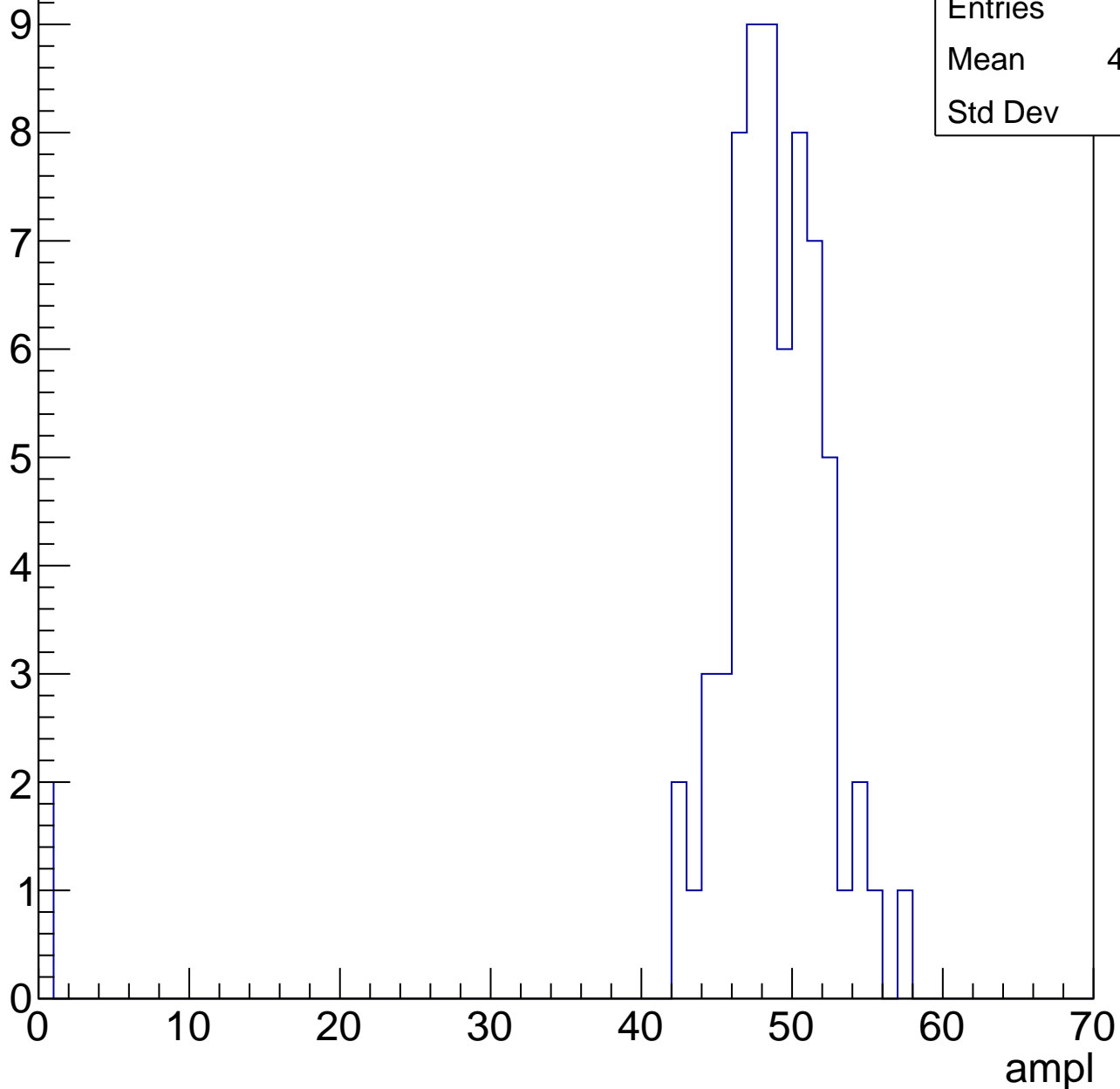
Entries	62
Mean	41.97
Std Dev	3.659



B1L103S, U11-ch96, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry



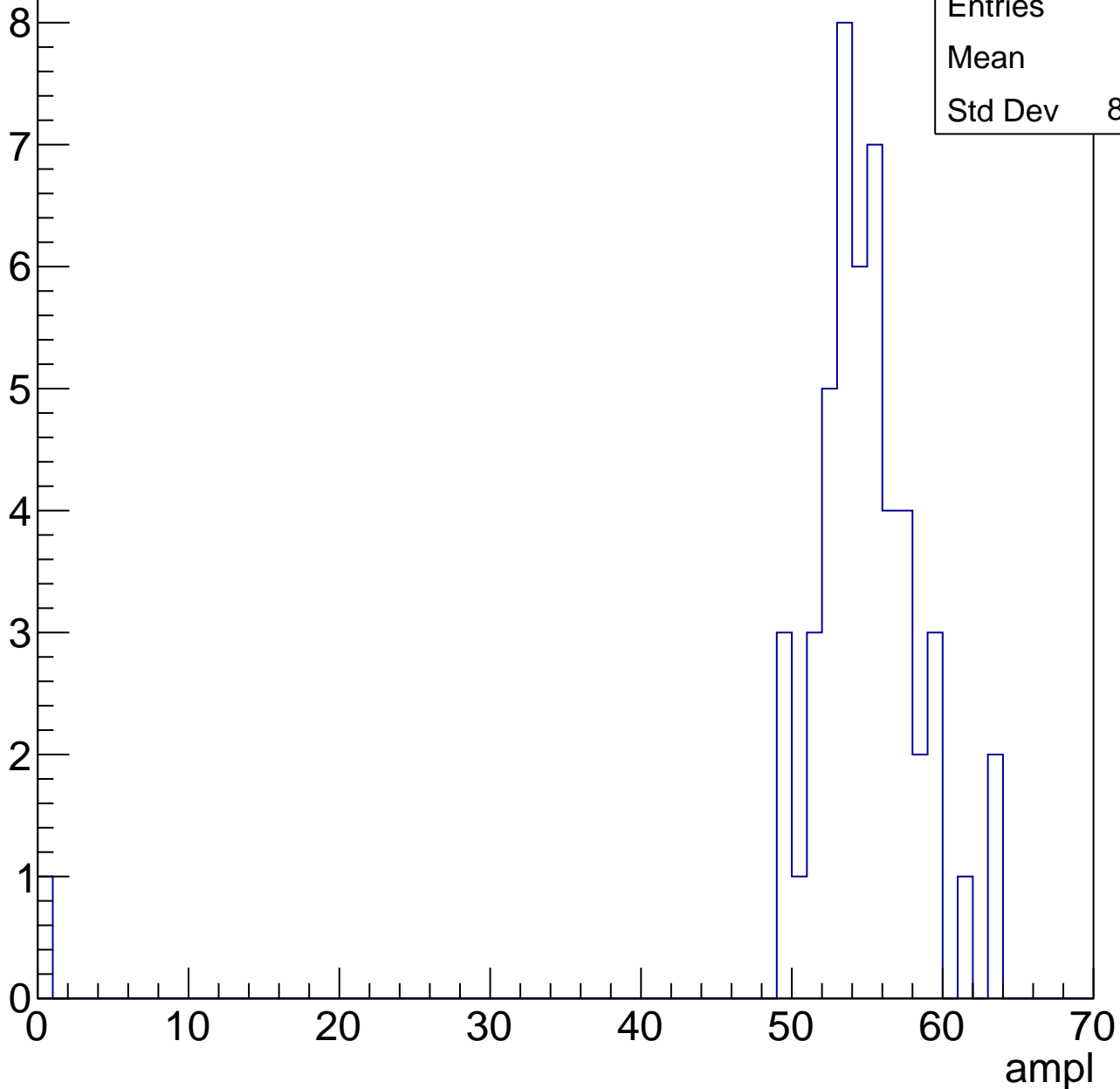
Entries	68
Mean	47.07
Std Dev	8.72

B1L103S, U11-ch96, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

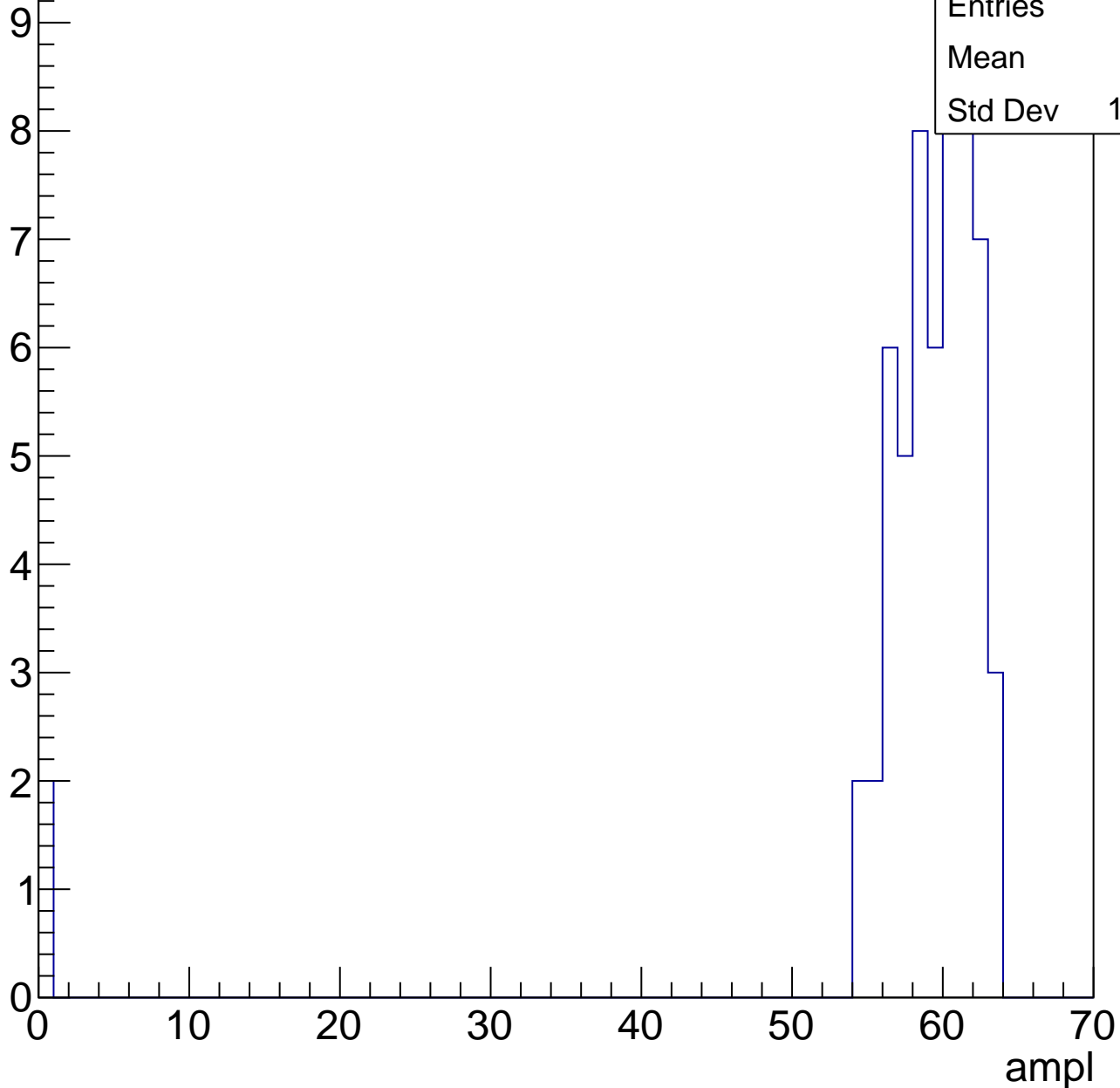
Entries	50
Mean	53.5
Std Dev	8.278



B1L103S, U11-ch96, adc5

calib_packv5_041523_1651.root, FC#0, port C2

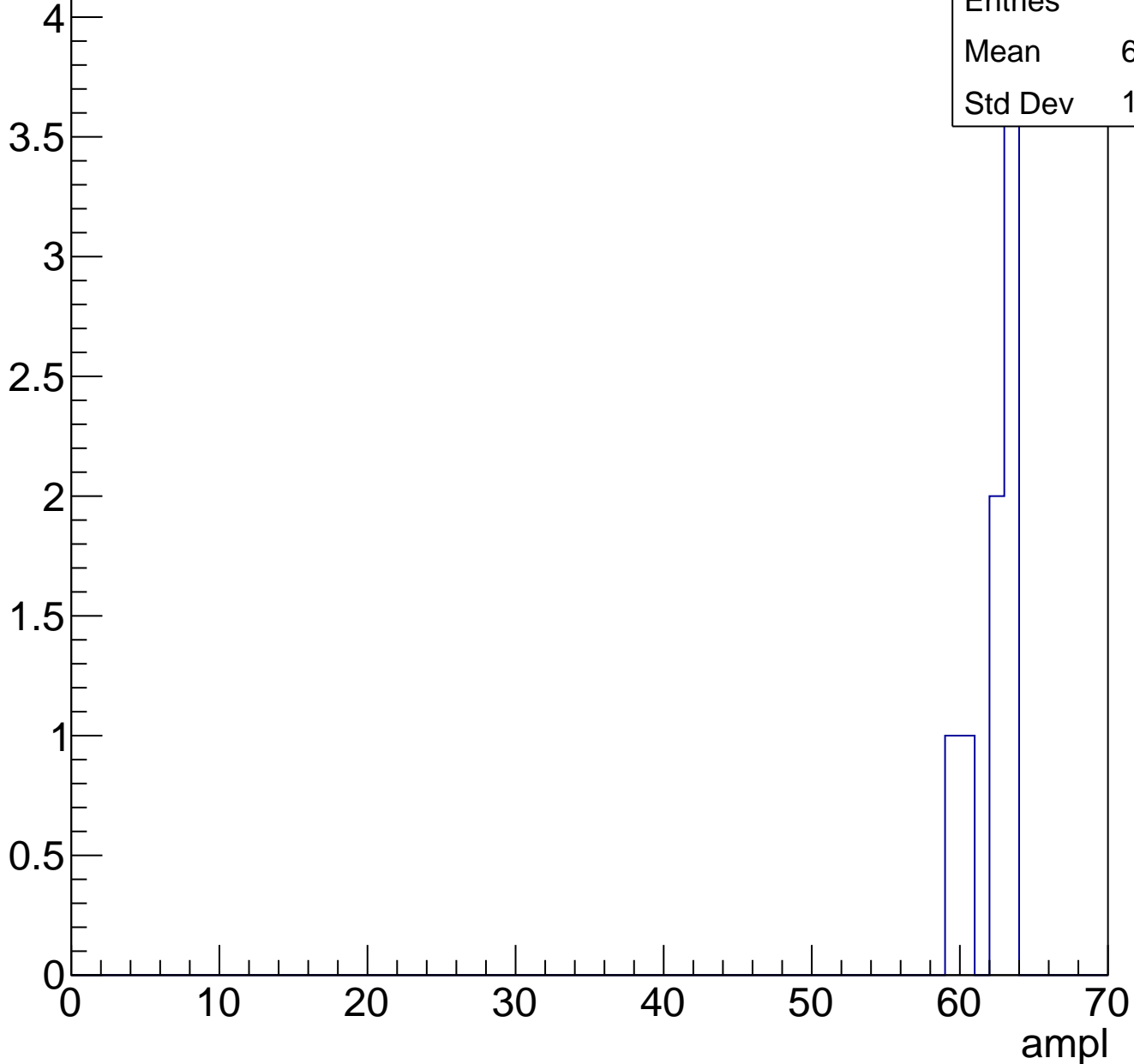
Entry



B1L103S, U11-ch96, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

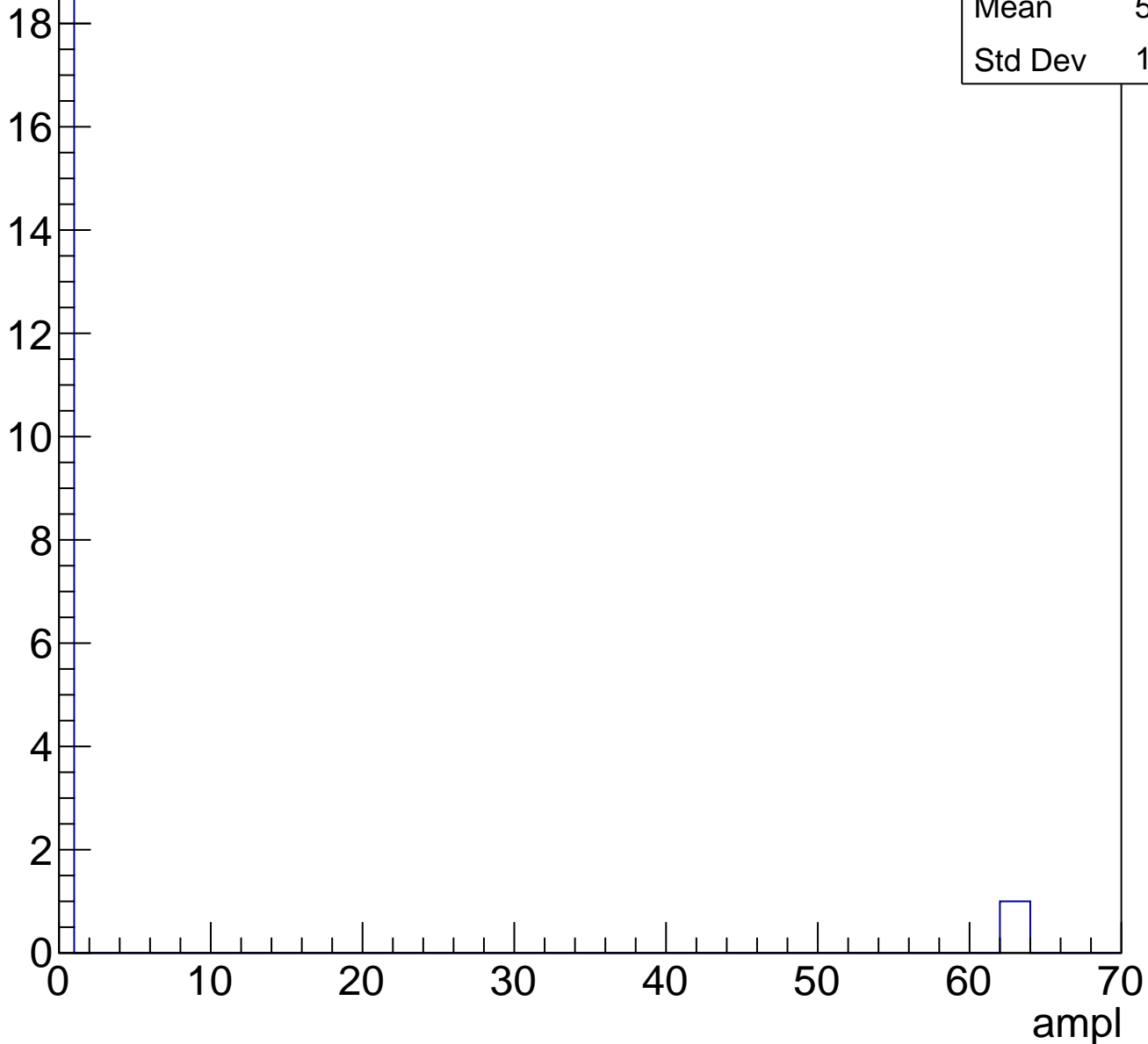


B1L103S, U11-ch96, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	5.952
Std Dev	18.35

Entry

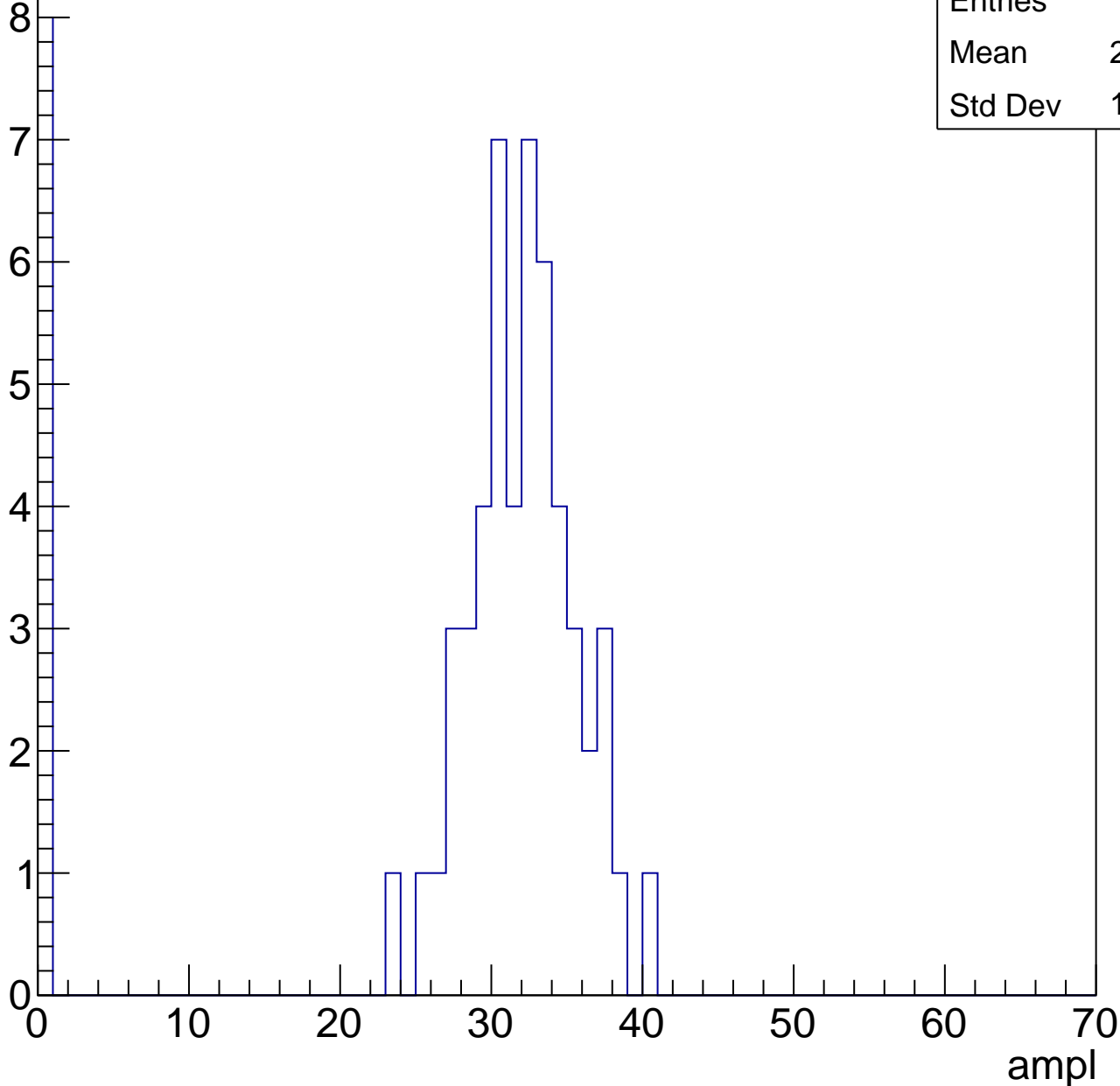


B1L103S, U11-ch97, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	27.34
Std Dev	11.29

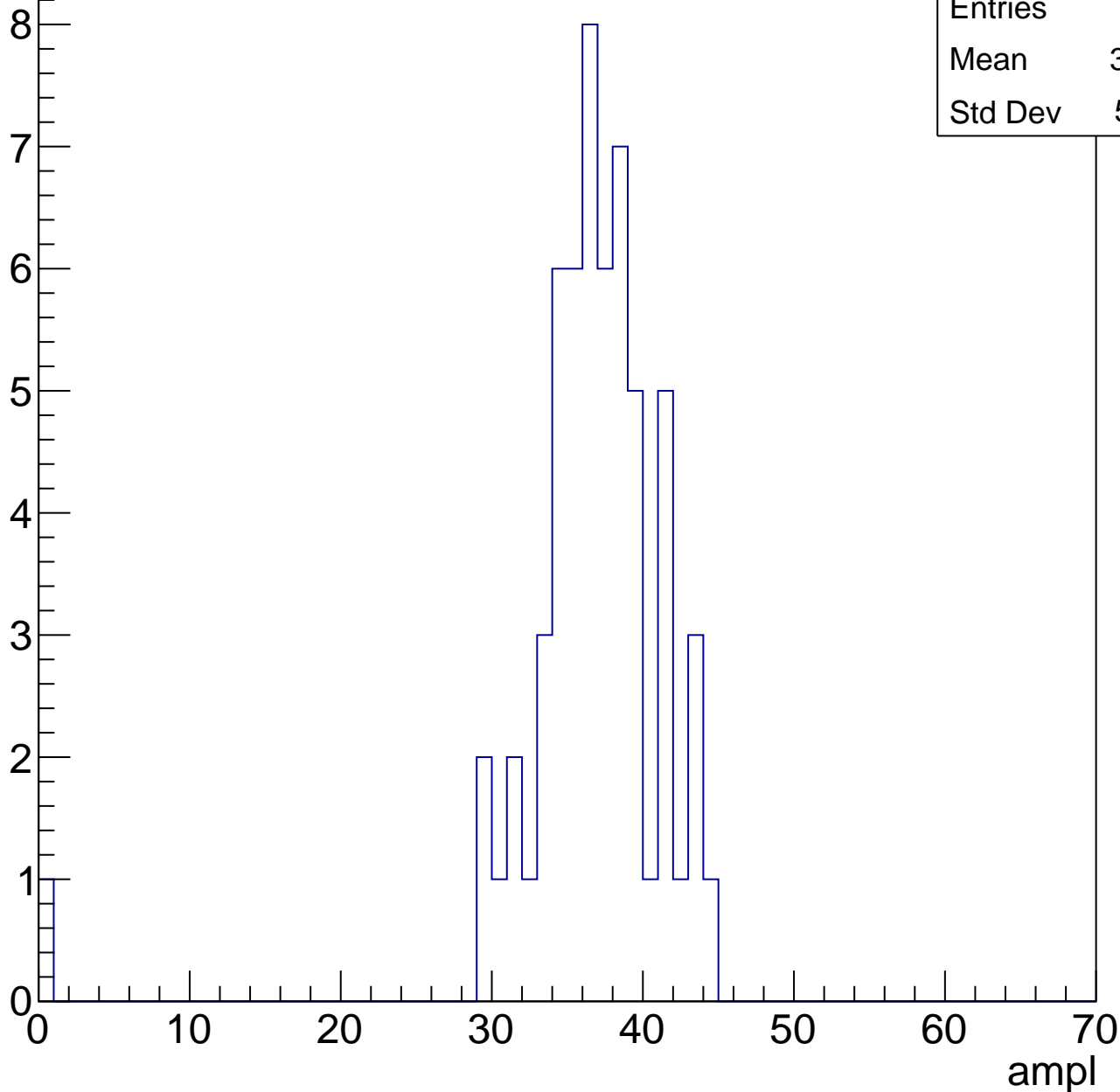


B1L103S, U11-ch97, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	36.03
Std Dev	5.851



B1L103S, U11-ch97, adc2

calib_packv5_041523_1651.root, FC#0, port C2

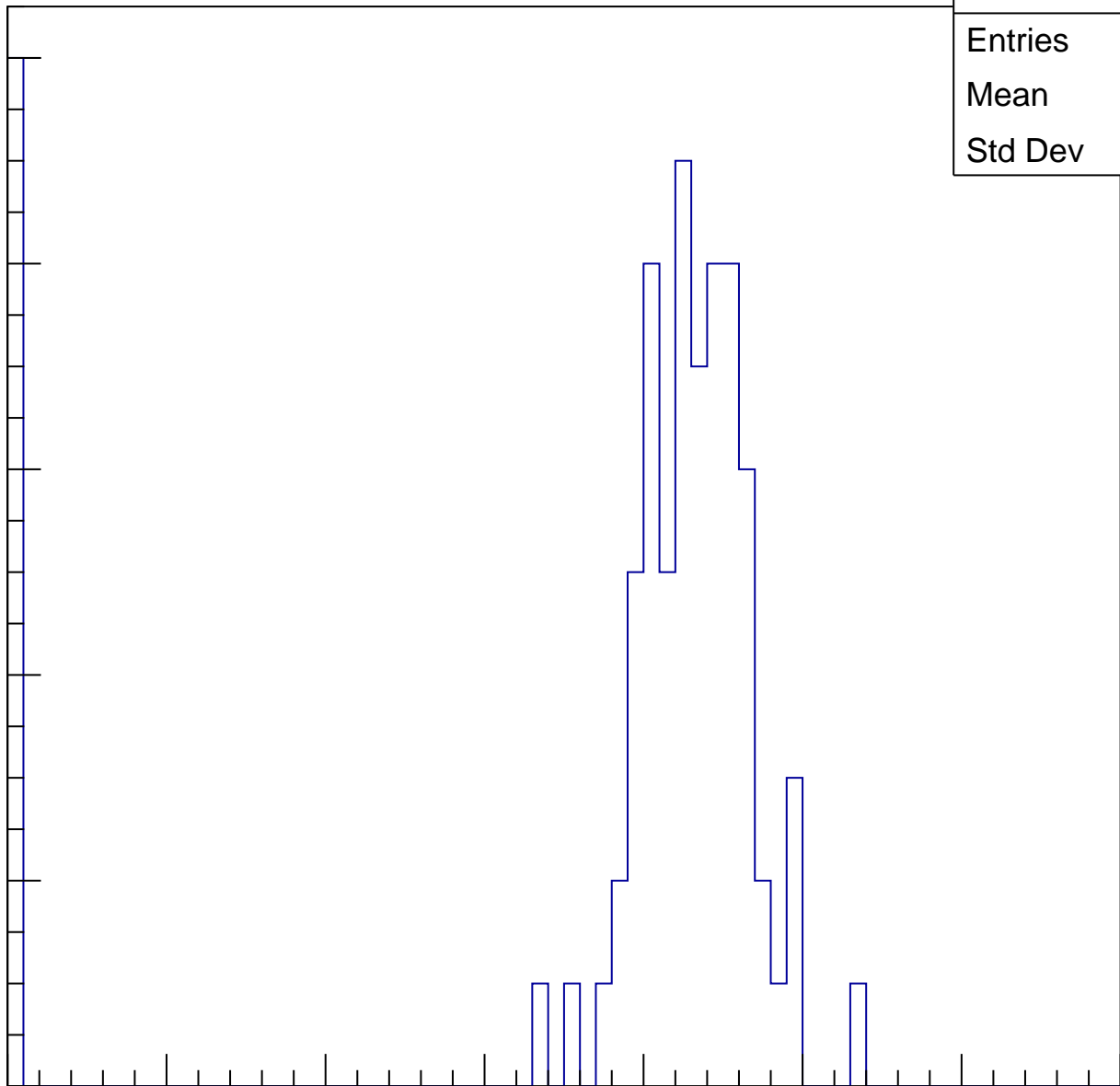
Entries	78
Mean	37.31
Std Dev	14.66

Entry

10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U11-ch97, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	84
Mean	47.54
Std Dev	12.36

Entry

10

8

6

4

2

0

0

10

20

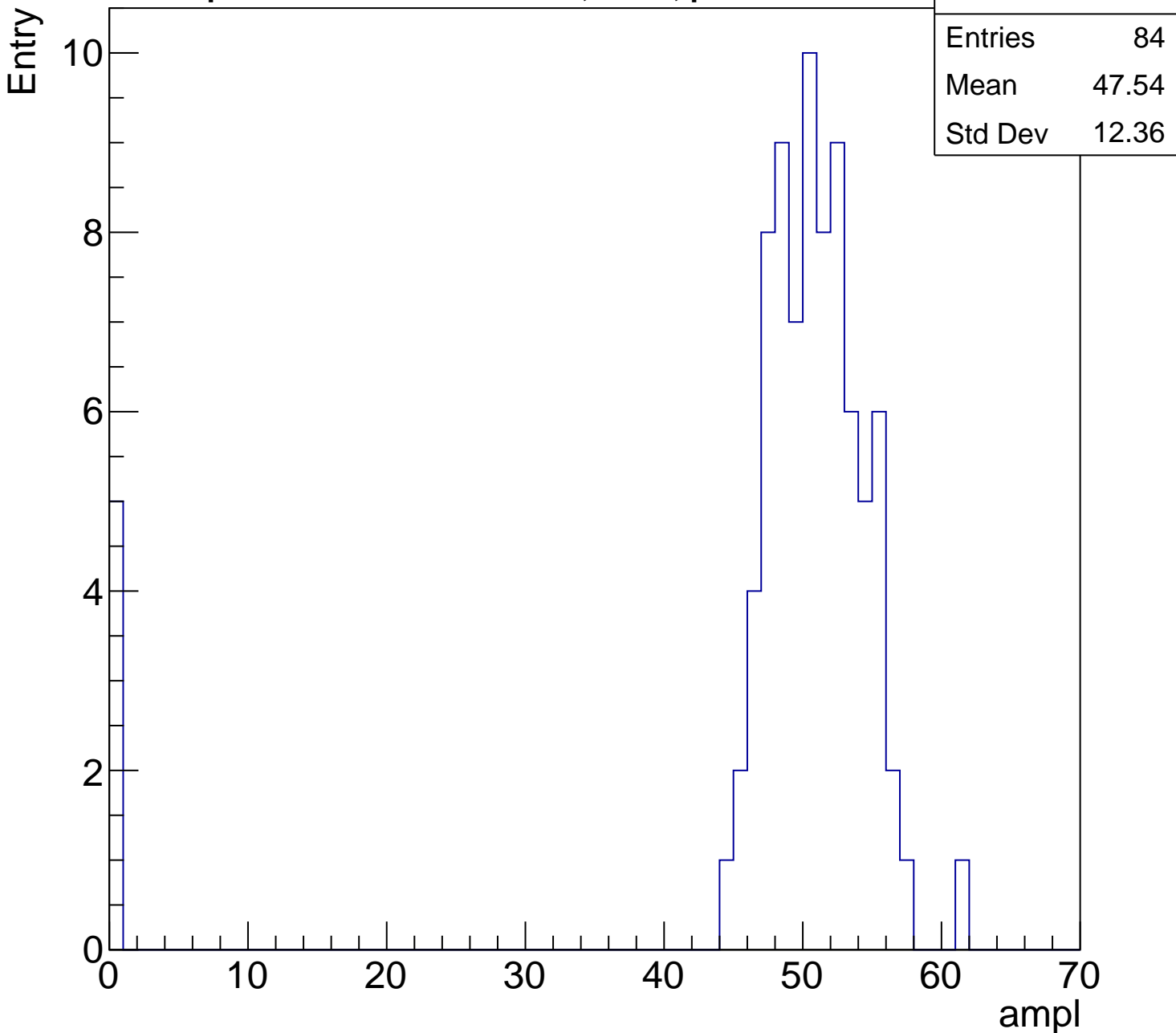
30

40

50

60

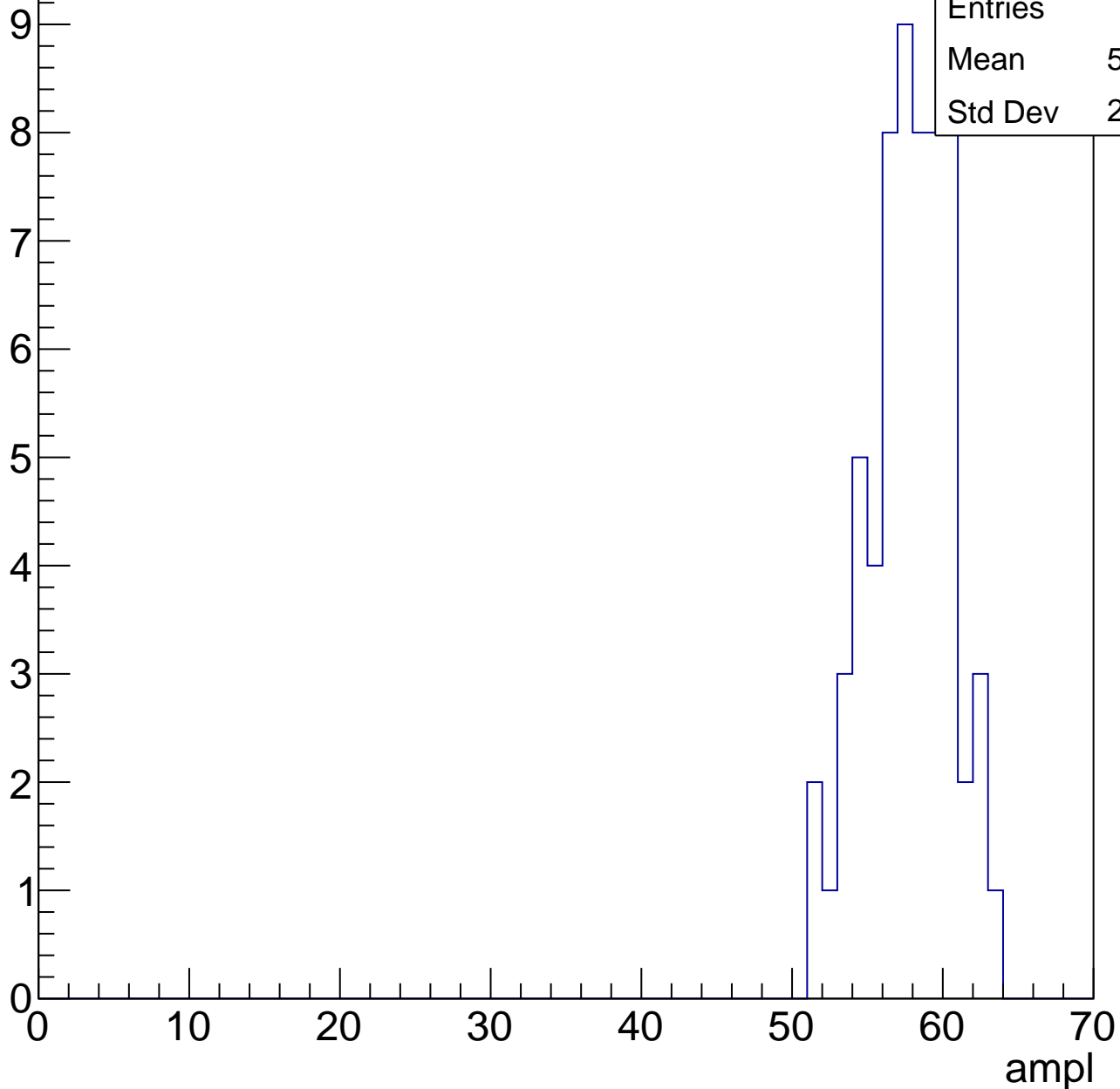
ampl



B1L103S, U11-ch97, adc4

calib_packv5_041523_1651.root, FC#0, port C2

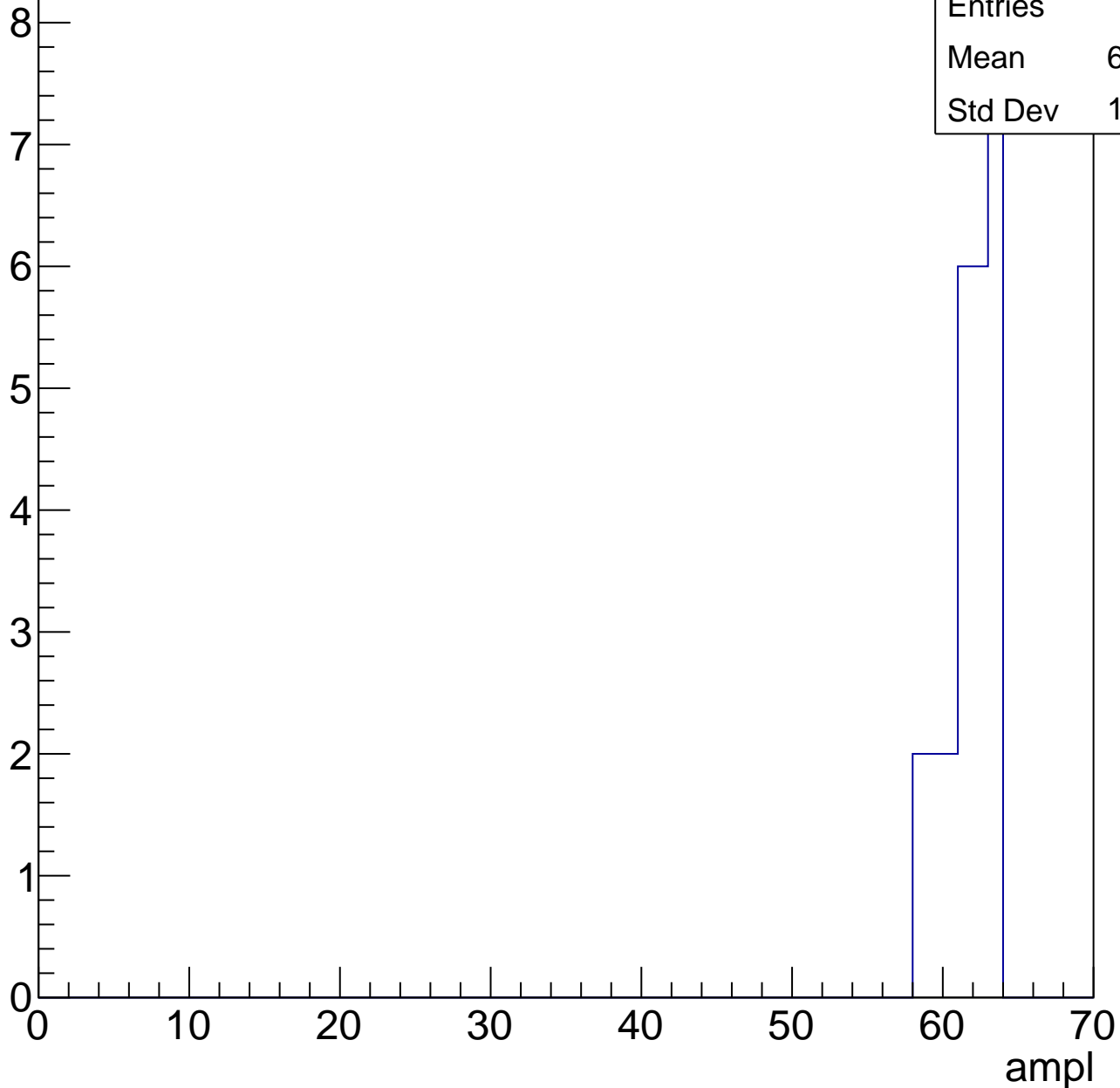
Entry



B1L103S, U11-ch97, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

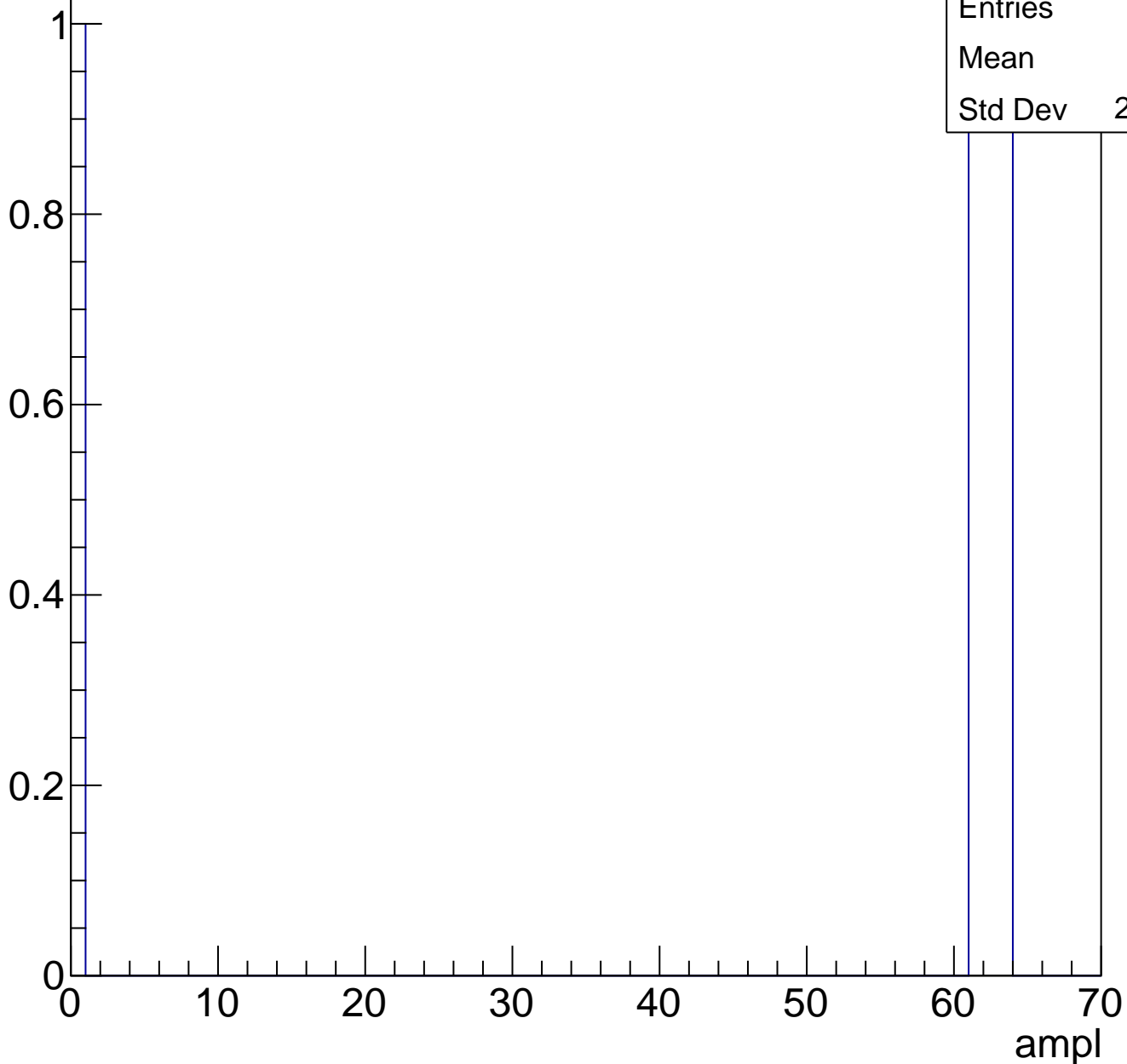


Entries	26
Mean	61.38
Std Dev	1.546

B1L103S, U11-ch97, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch97, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



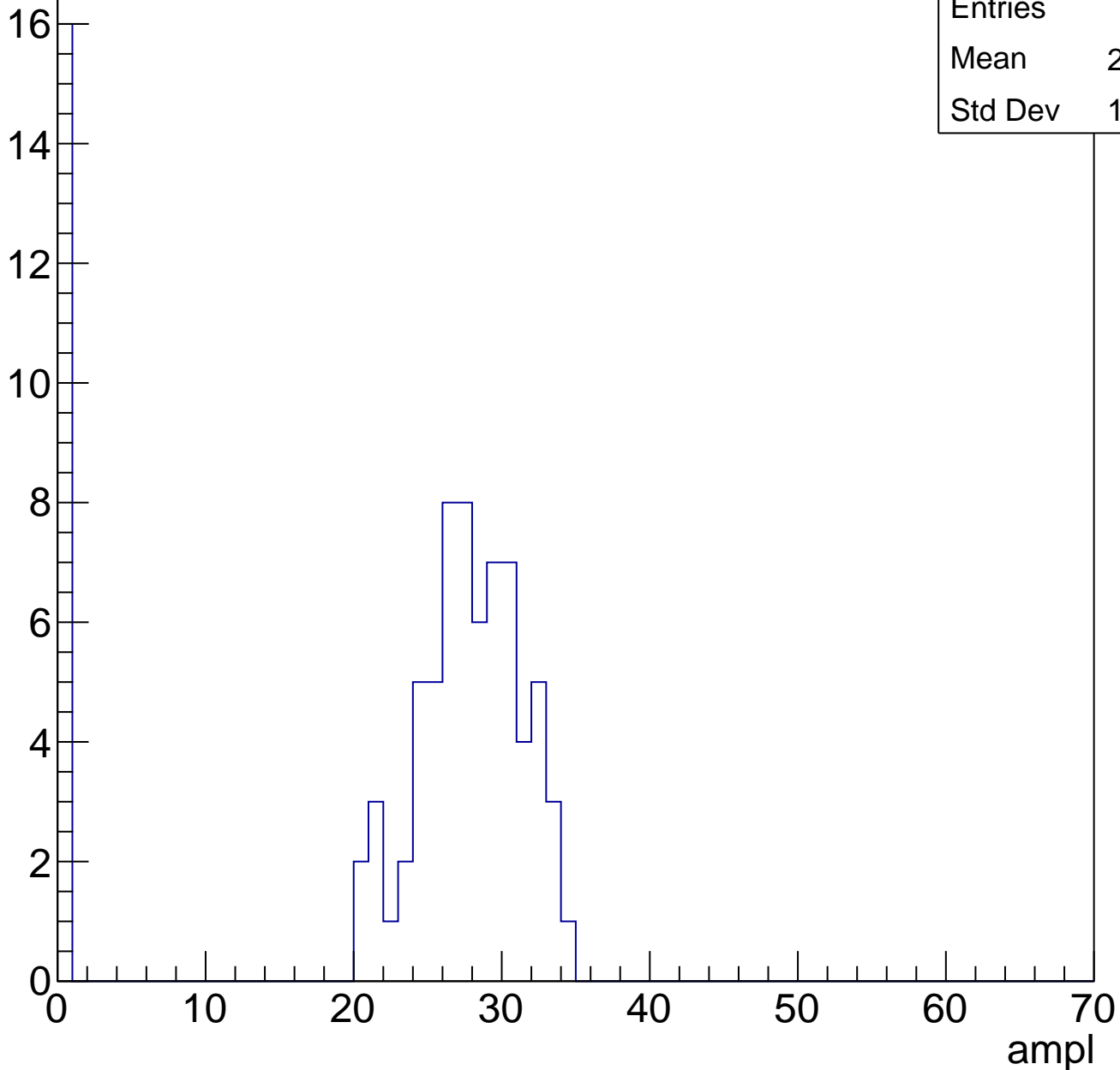
Entries	19
Mean	0
Std Dev	0

B1L103S, U11-ch98, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	83
Mean	22.14
Std Dev	11.24

Entry

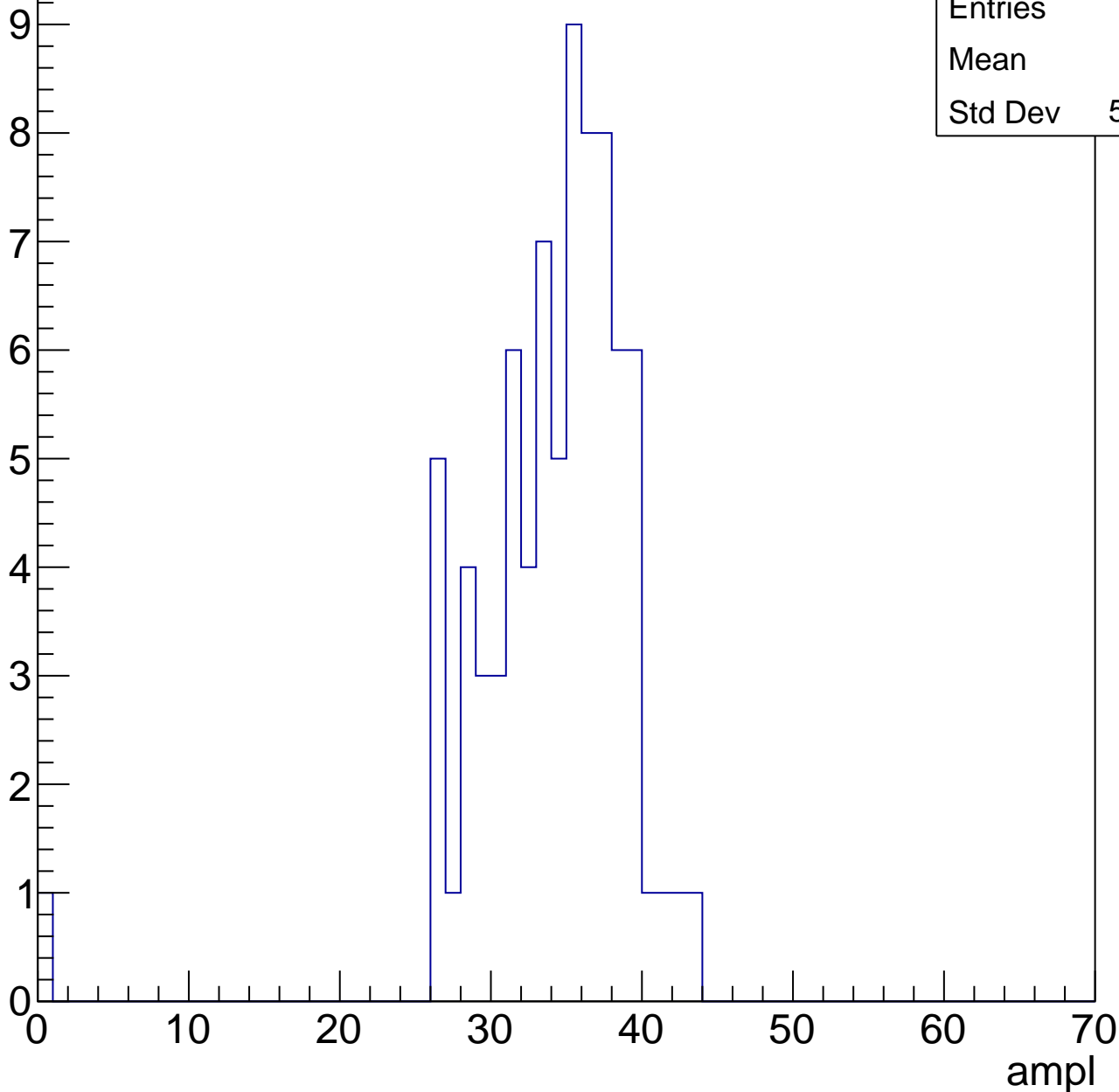


B1L103S, U11-ch98, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	80
Mean	33.6
Std Dev	5.529

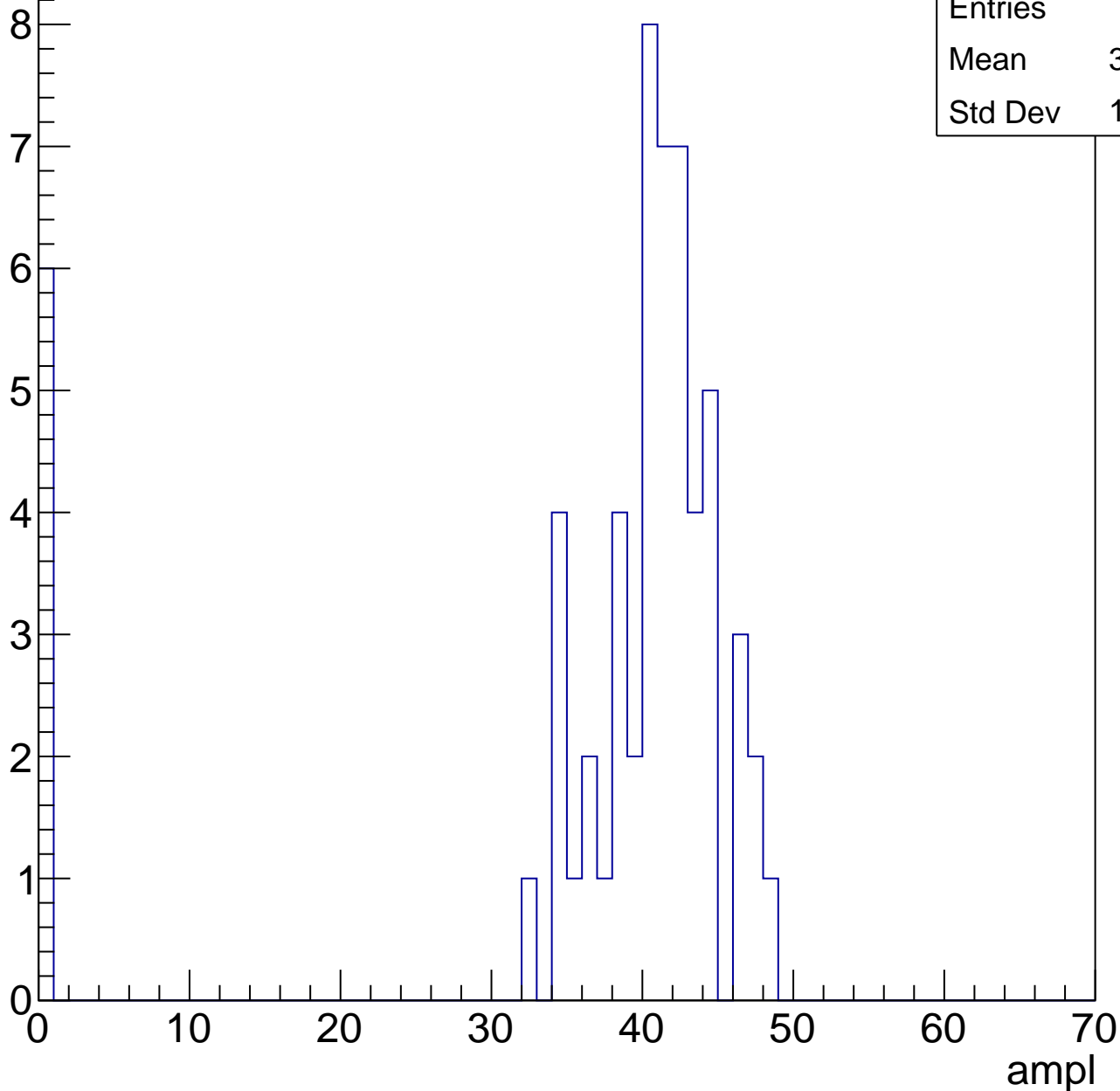


B1L103S, U11-ch98, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	36.47
Std Dev	12.86



B1L103S, U11-ch98, adc3

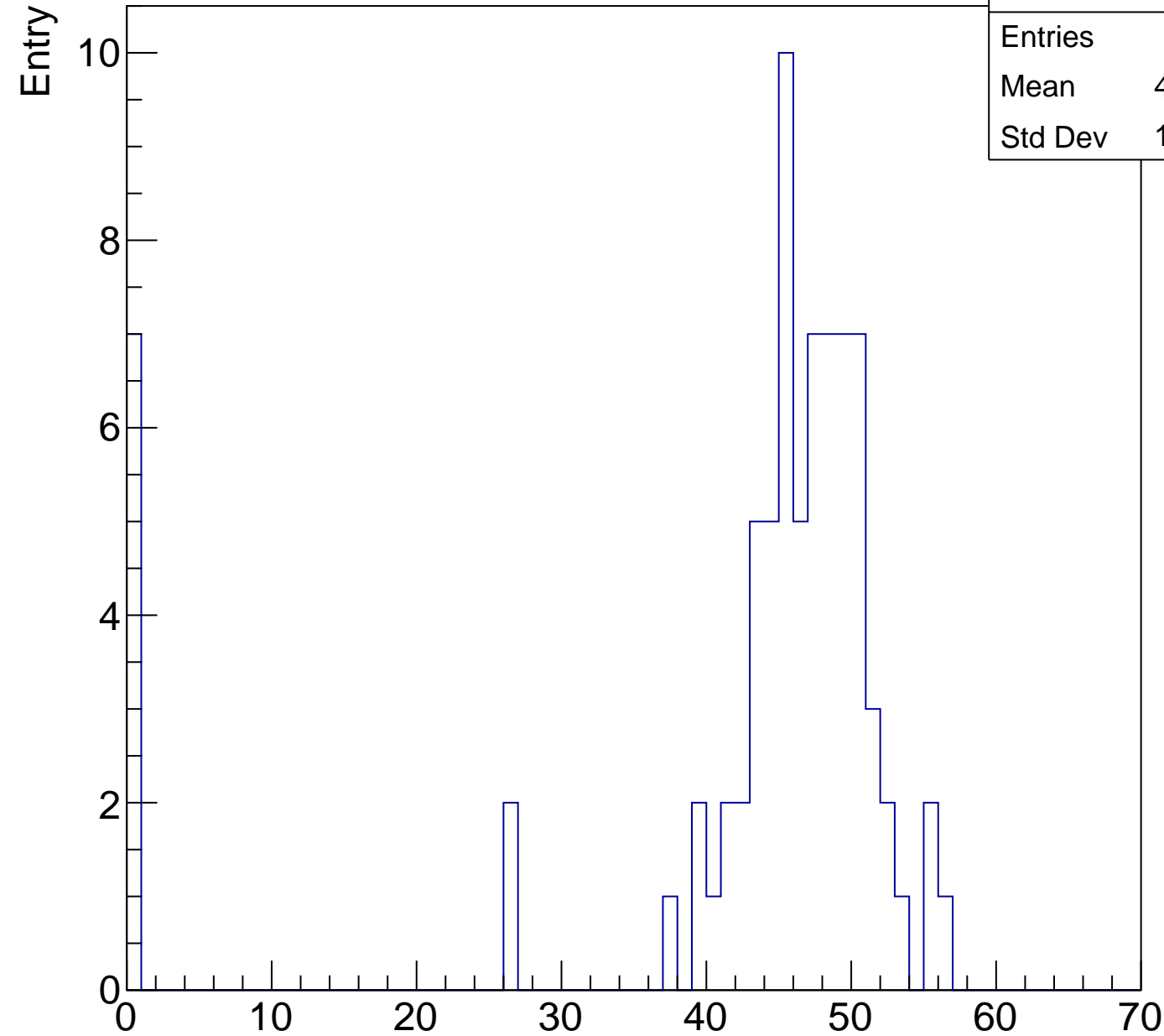
calib_packv5_041523_1651.root, FC#0, port C2

Entries	79
Mean	42.05
Std Dev	13.97

Entry

10
8
6
4
2
0

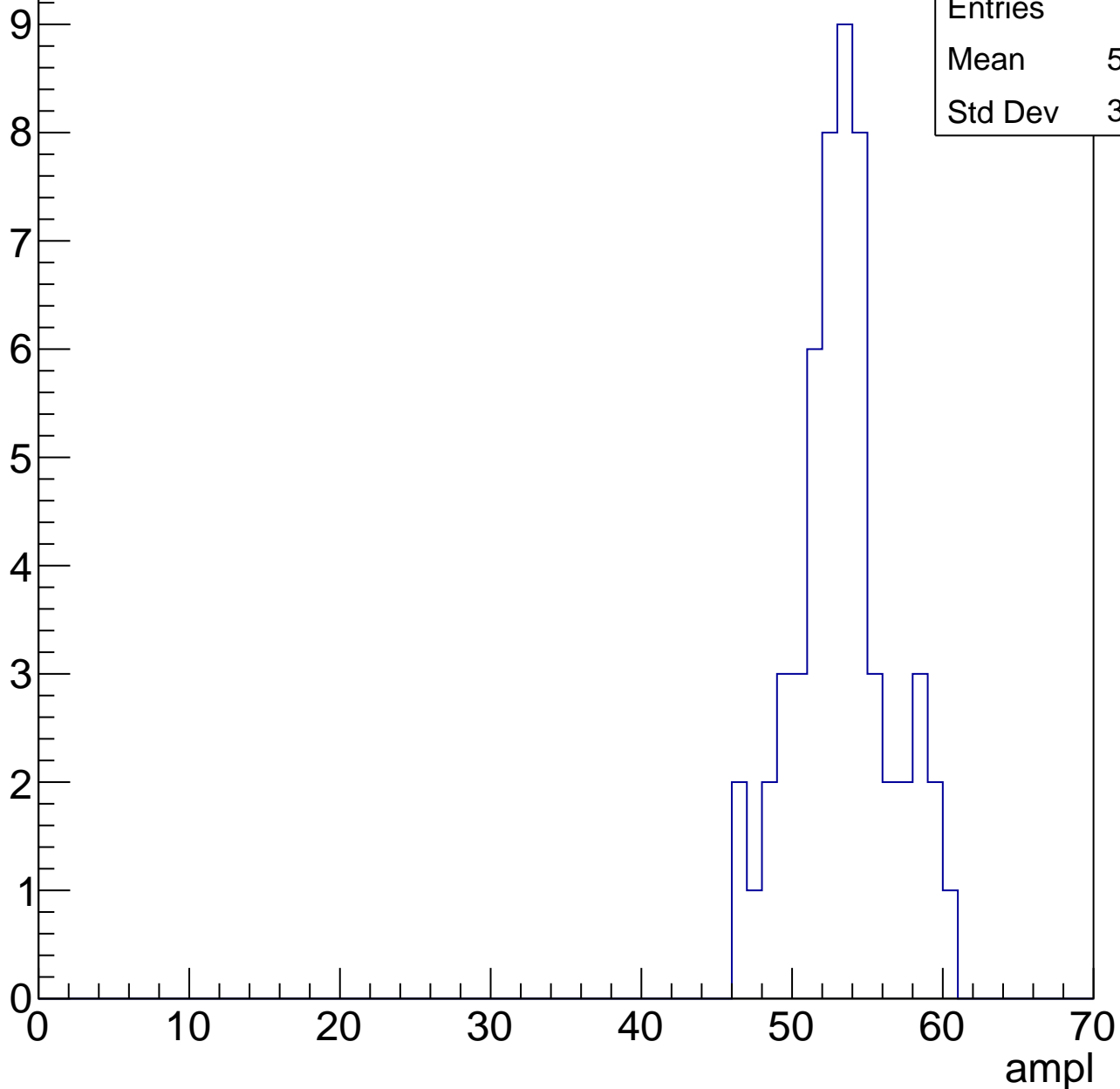
ampl



B1L103S, U11-ch98, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

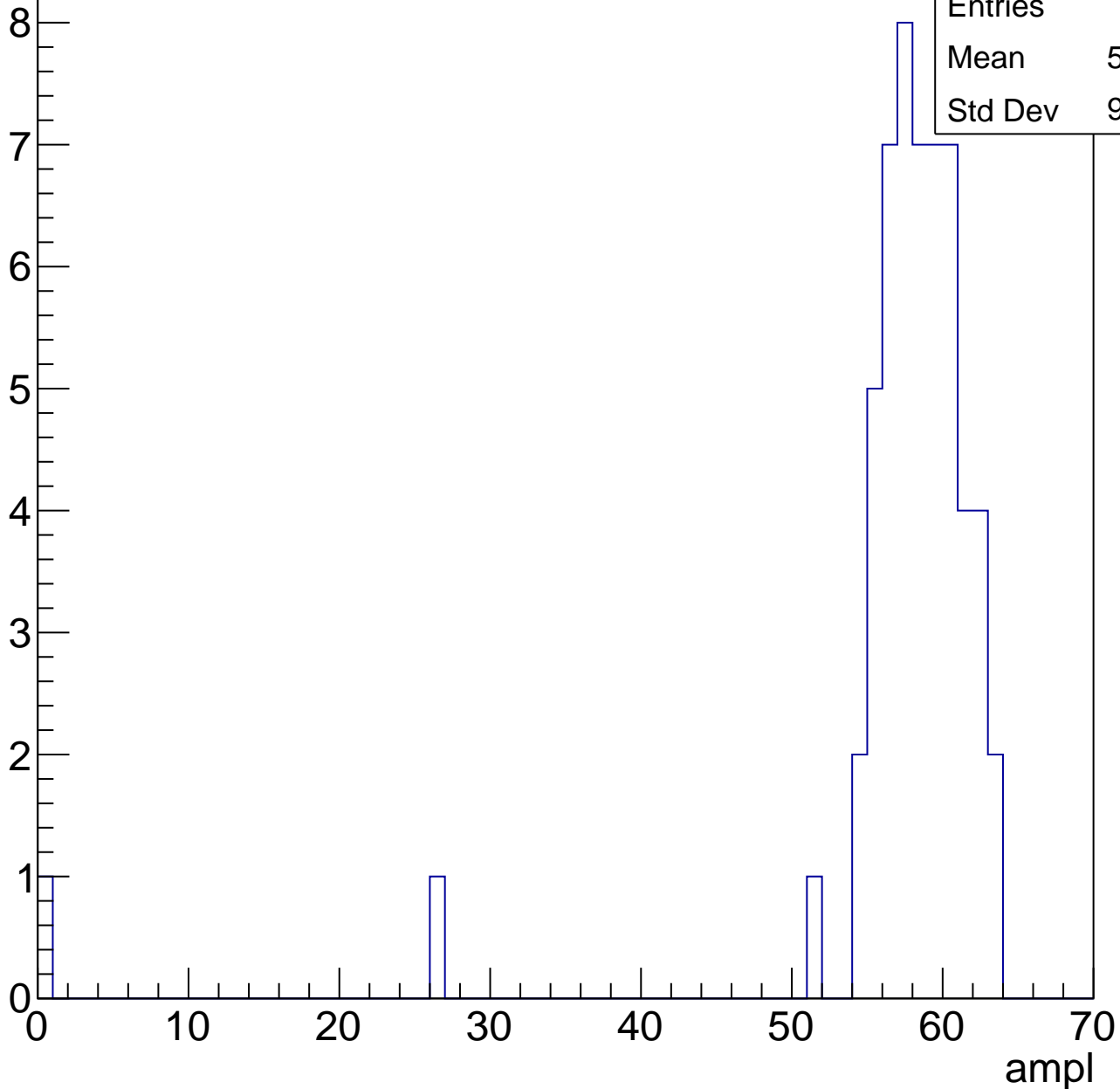


B1L103S, U11-ch98, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	56.52
Std Dev	9.075

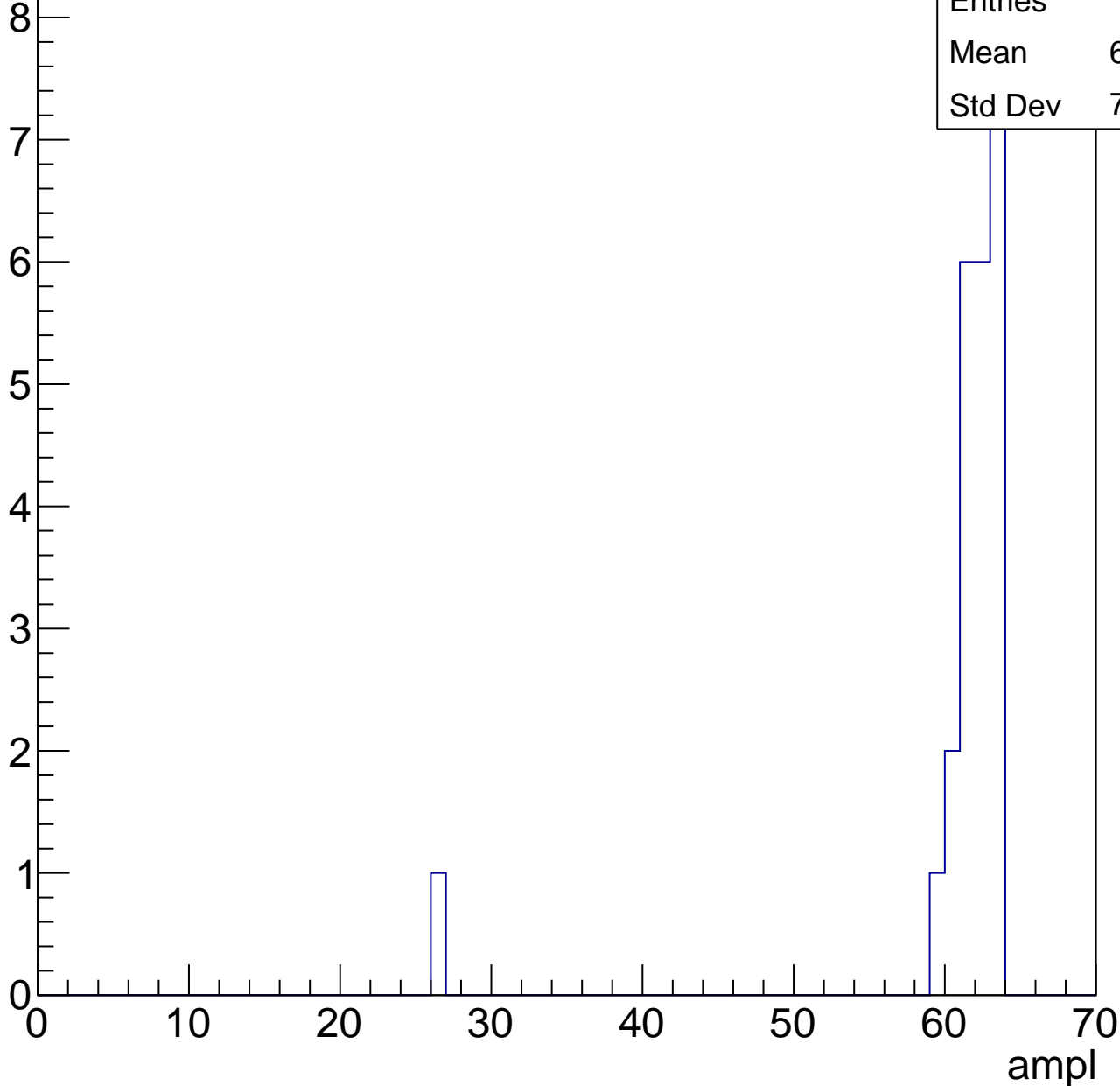


B1L103S, U11-ch98, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	24
Mean	60.29
Std Dev	7.237



B1L103S, U11-ch98, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

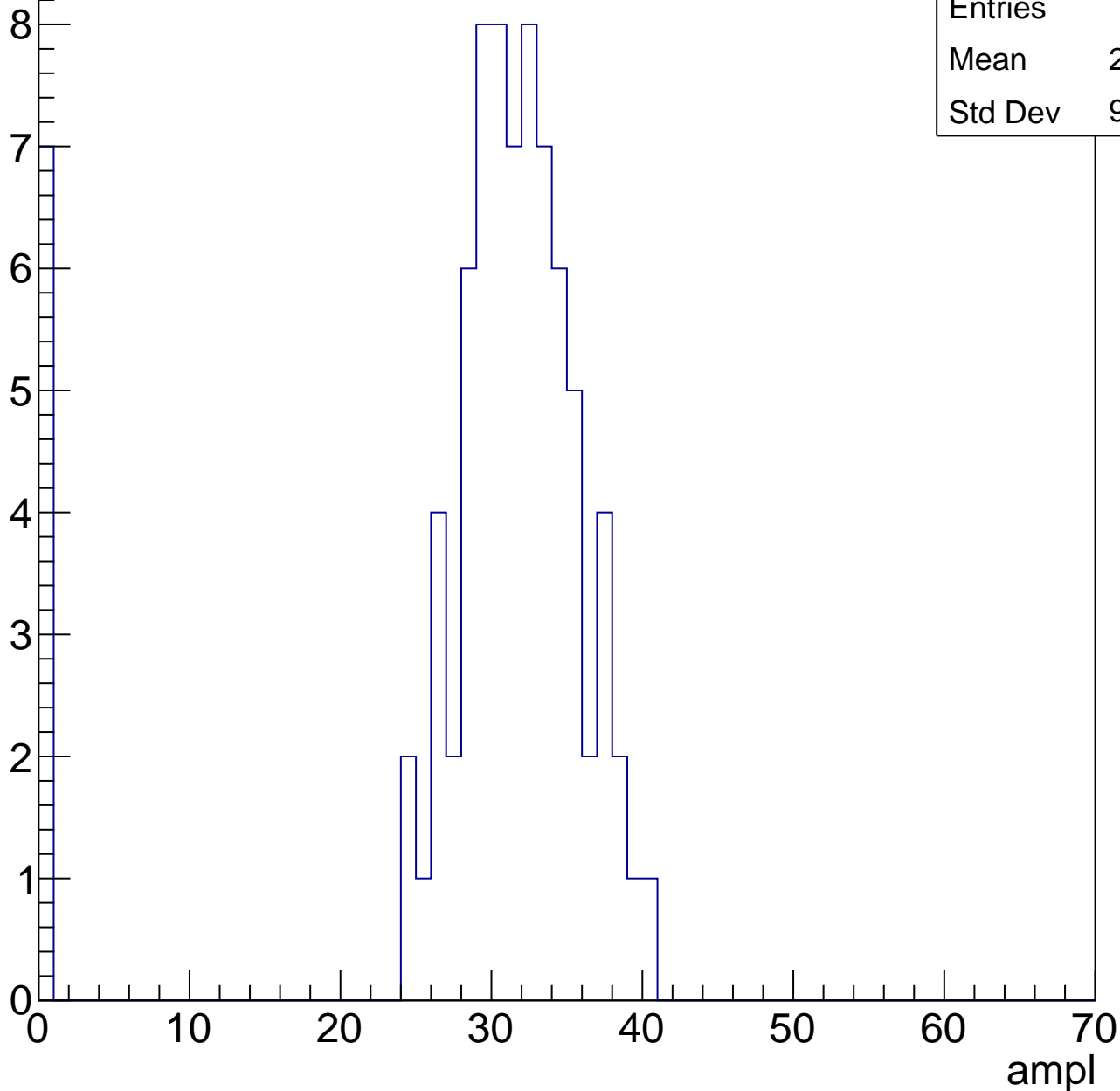
Entries	19
Mean	0
Std Dev	0

B1L103S, U11-ch99, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	81
Mean	28.75
Std Dev	9.484

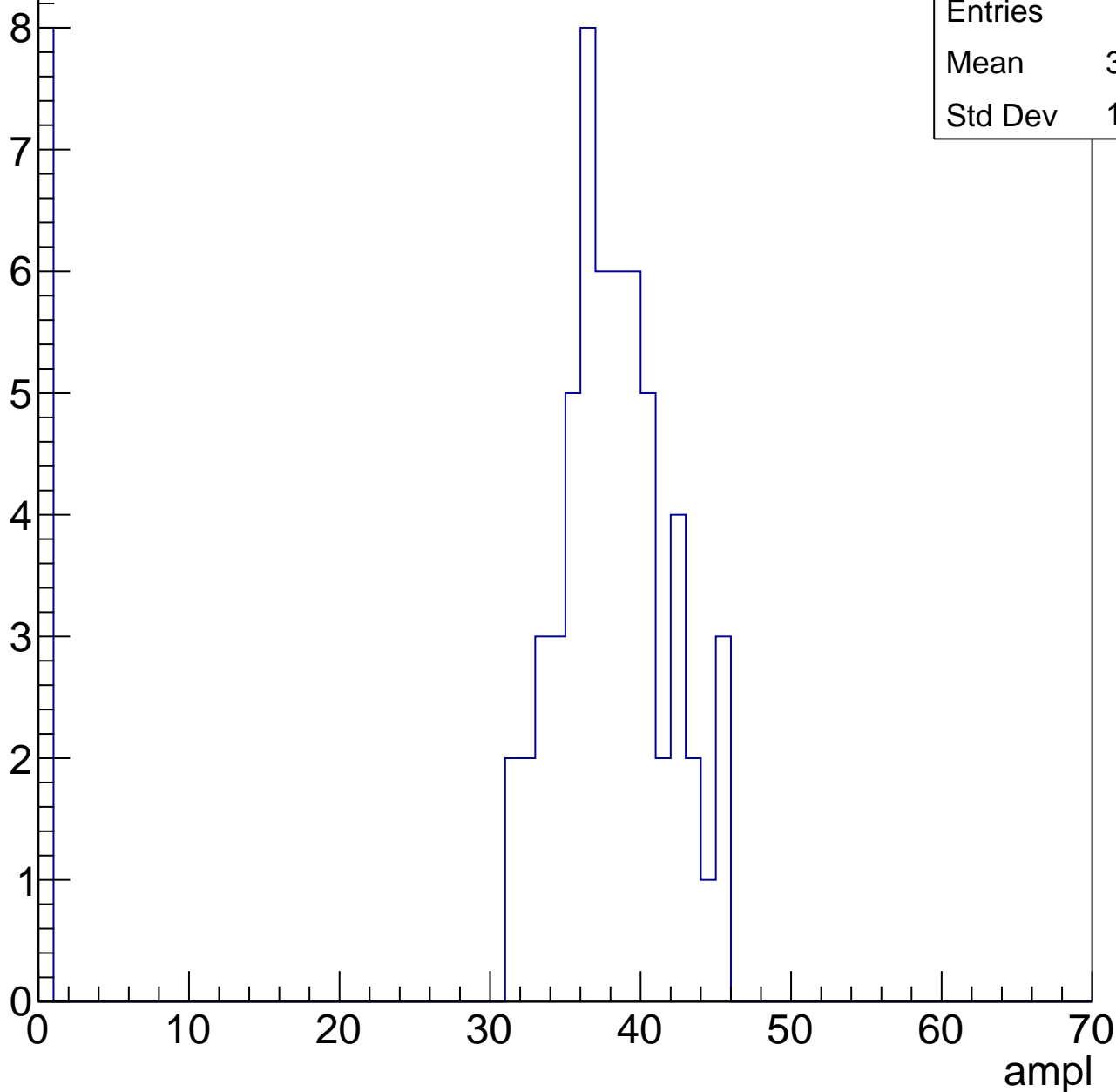


B1L103S, U11-ch99, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	33.17
Std Dev	12.75

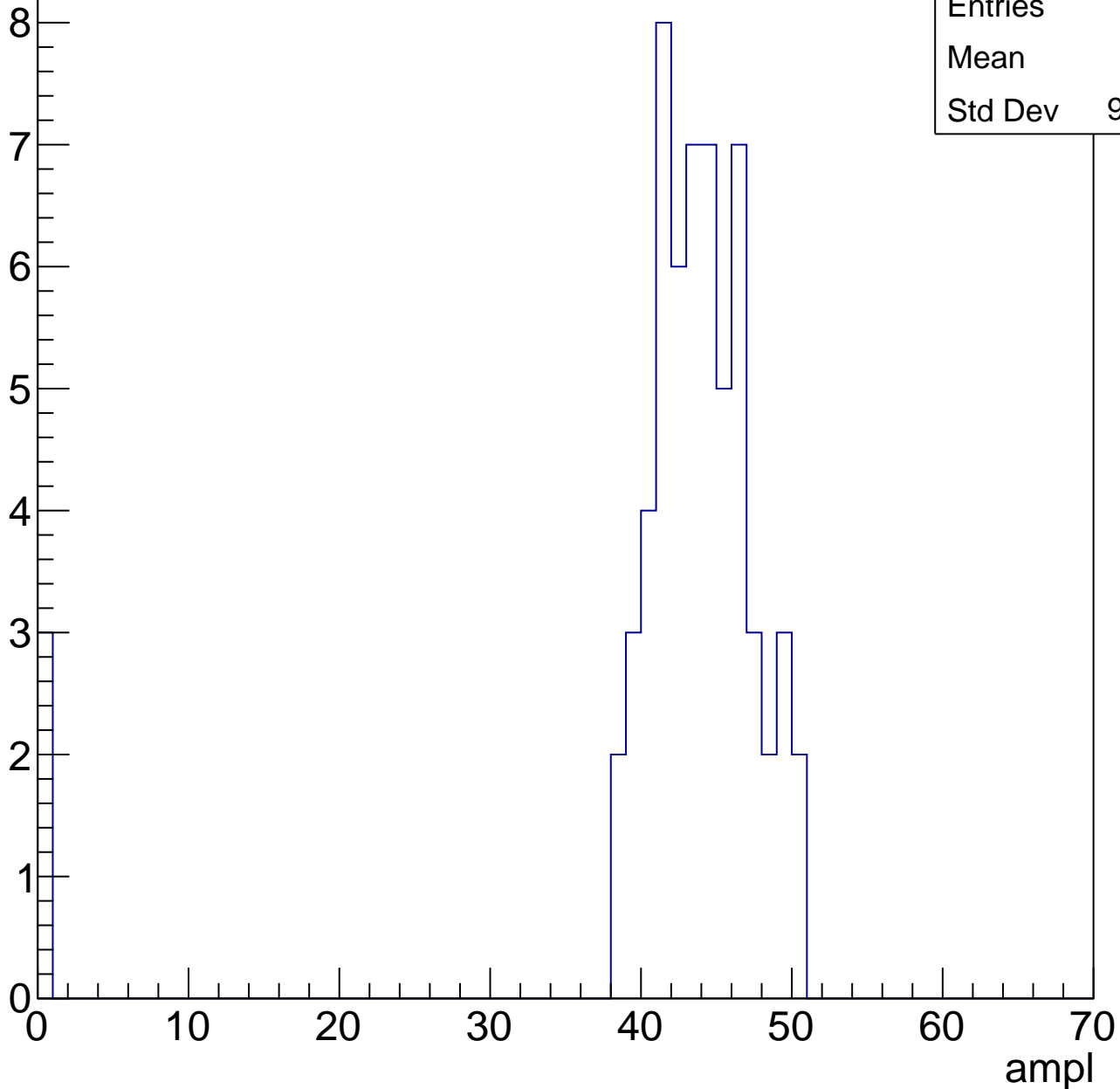


B1L103S, U11-ch99, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

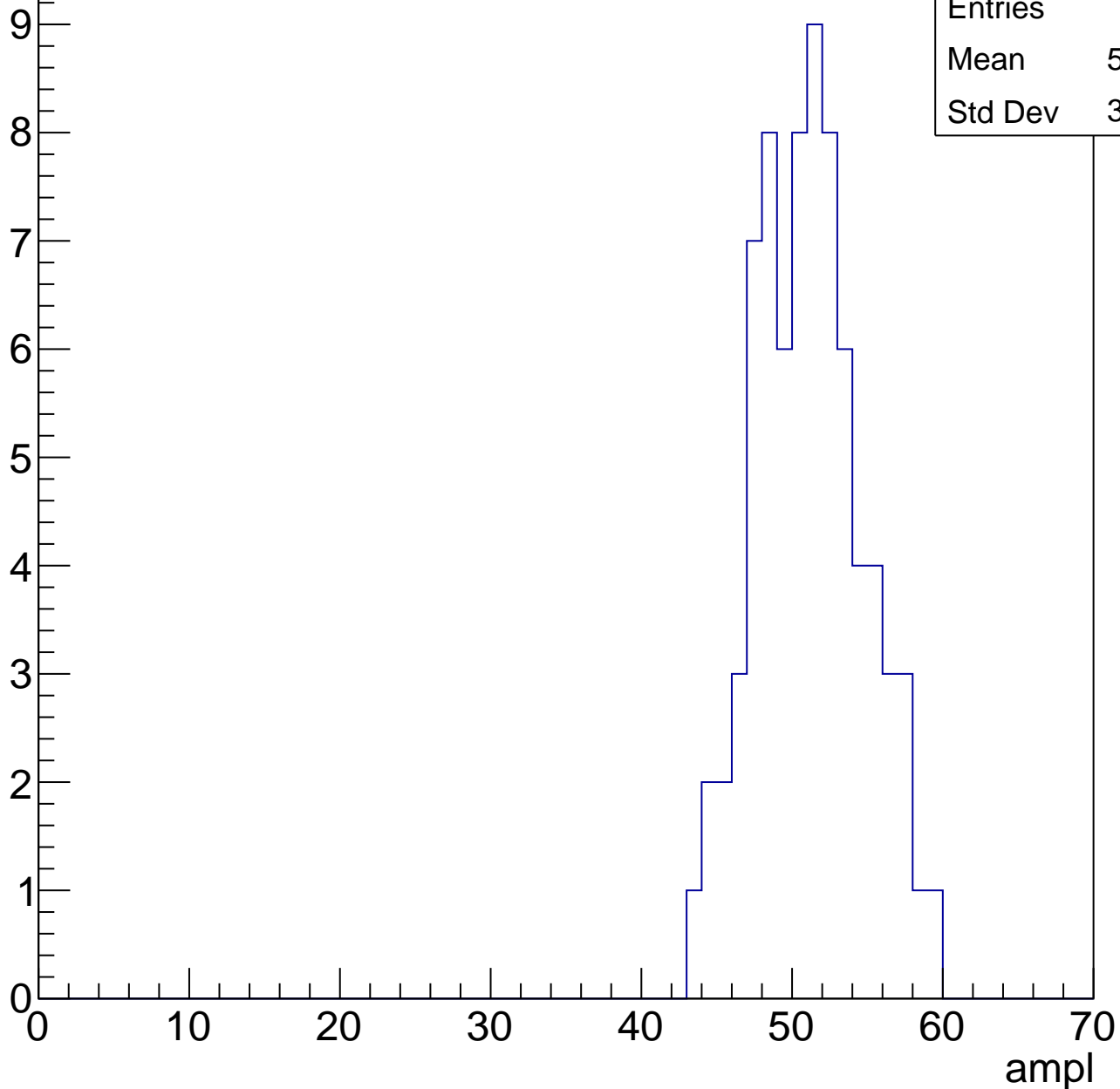
Entries	62
Mean	41.5
Std Dev	9.816



B1L103S, U11-ch99, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry



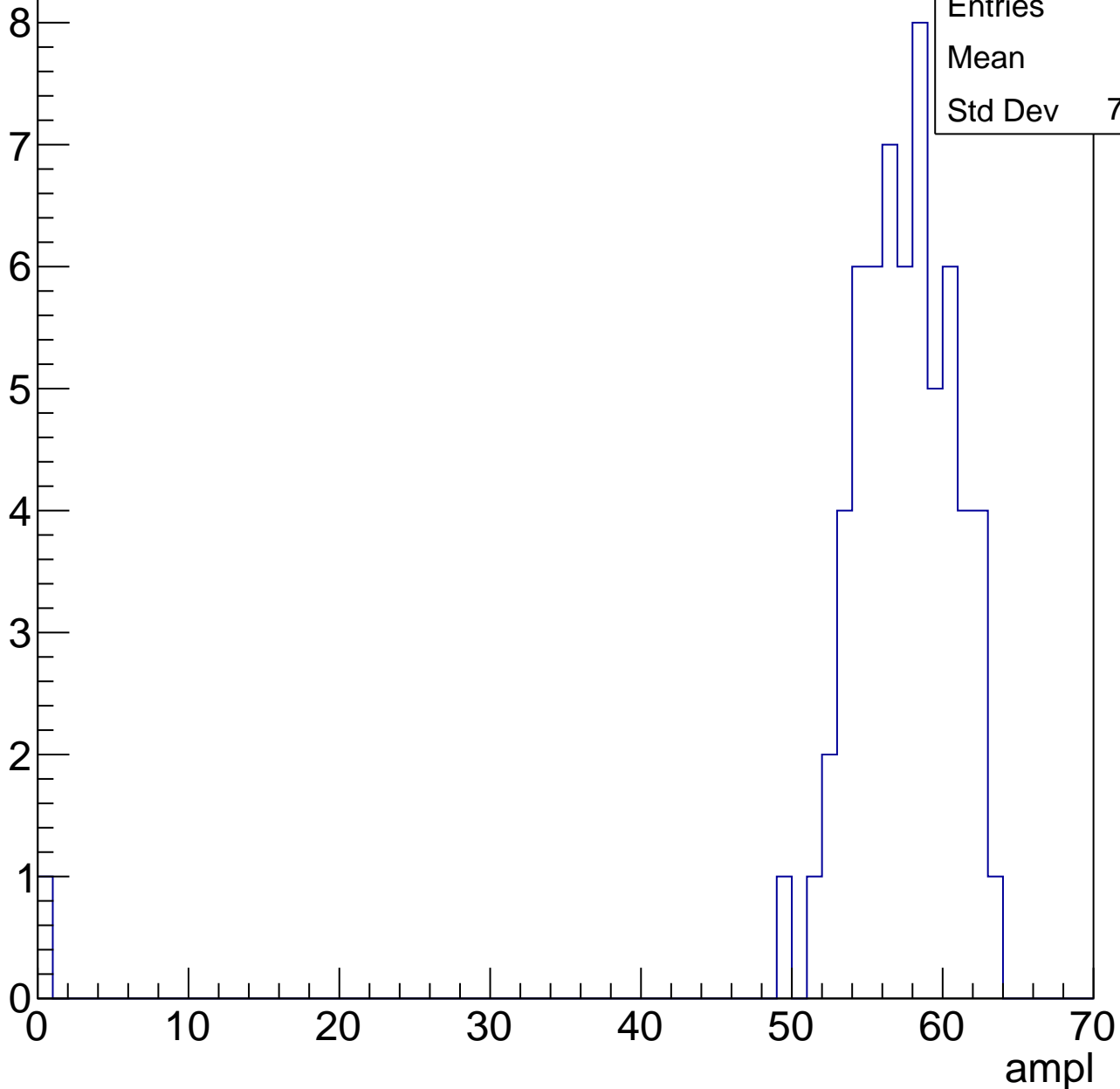
Entries	76
Mean	50.67
Std Dev	3.526

B1L103S, U11-ch99, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

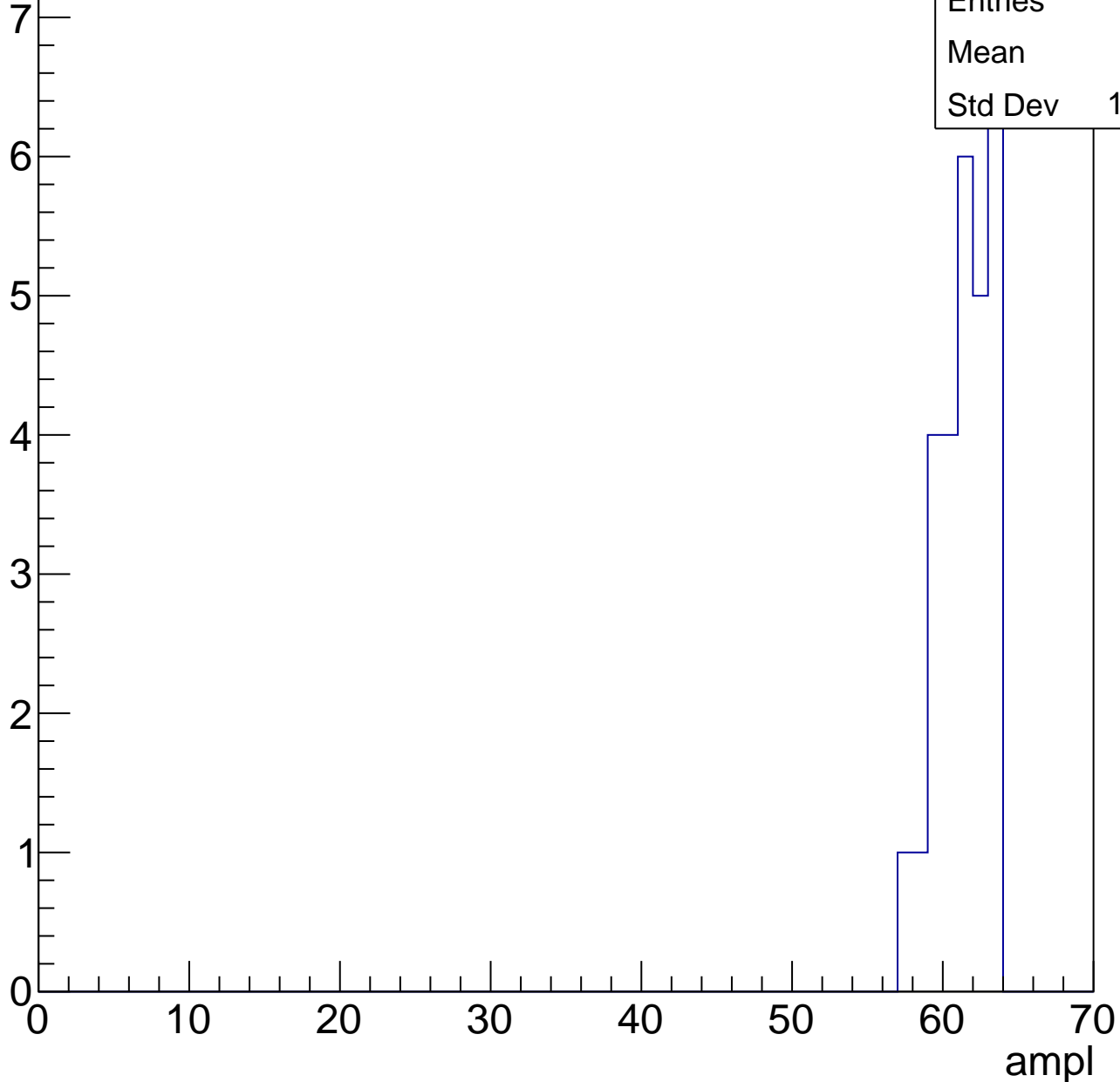
Entries	62
Mean	56.1
Std Dev	7.808



B1L103S, U11-ch99, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch99, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

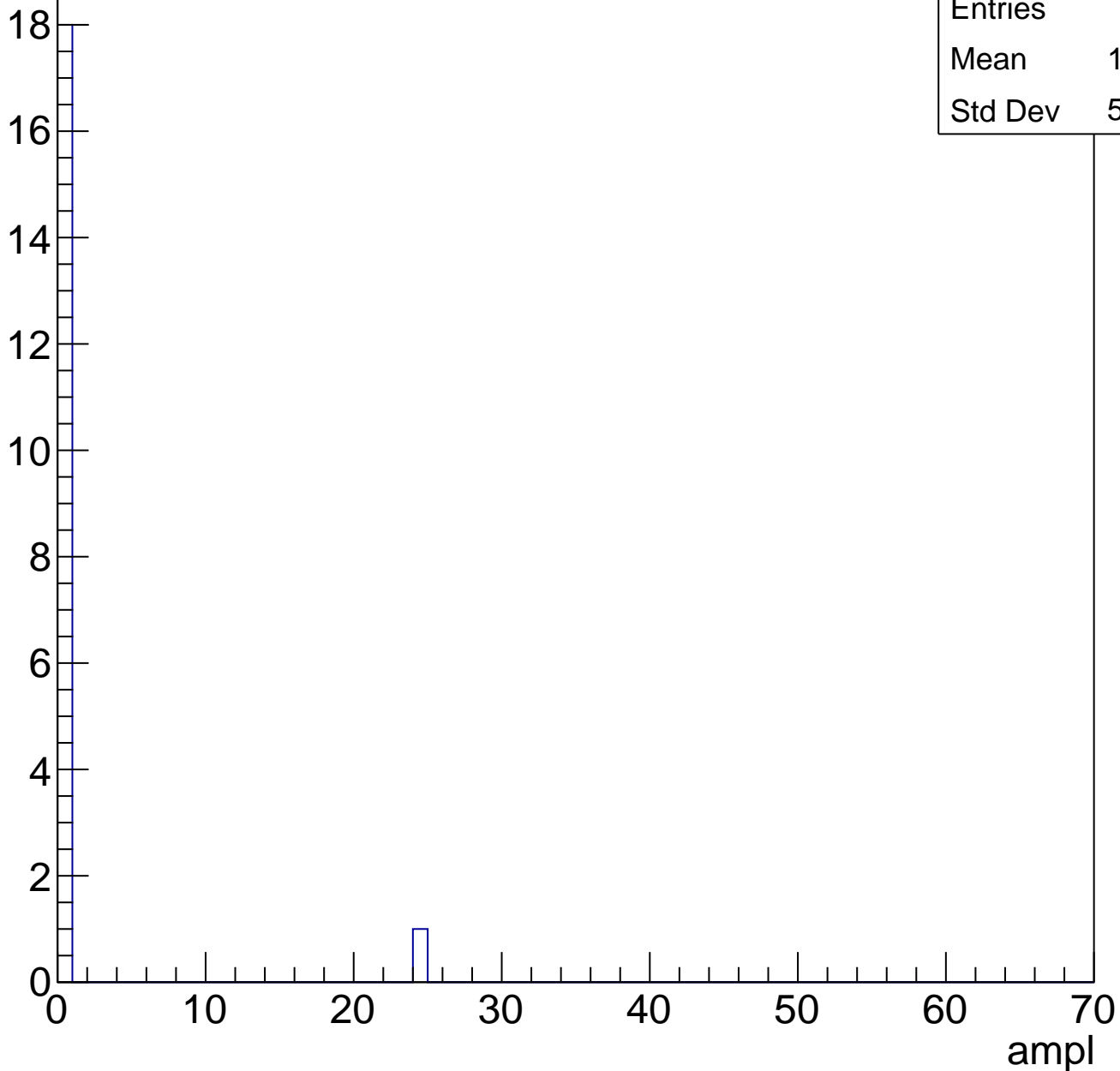
0 10 20 30 40 50 60 70

B1L103S, U11-ch99, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.263
Std Dev	5.359

Entry



B1L103S, U11-ch100, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	92
Mean	25.09
Std Dev	9.871

Entry

10

8

6

4

2

0

ampl

0

10

20

30

40

50

60

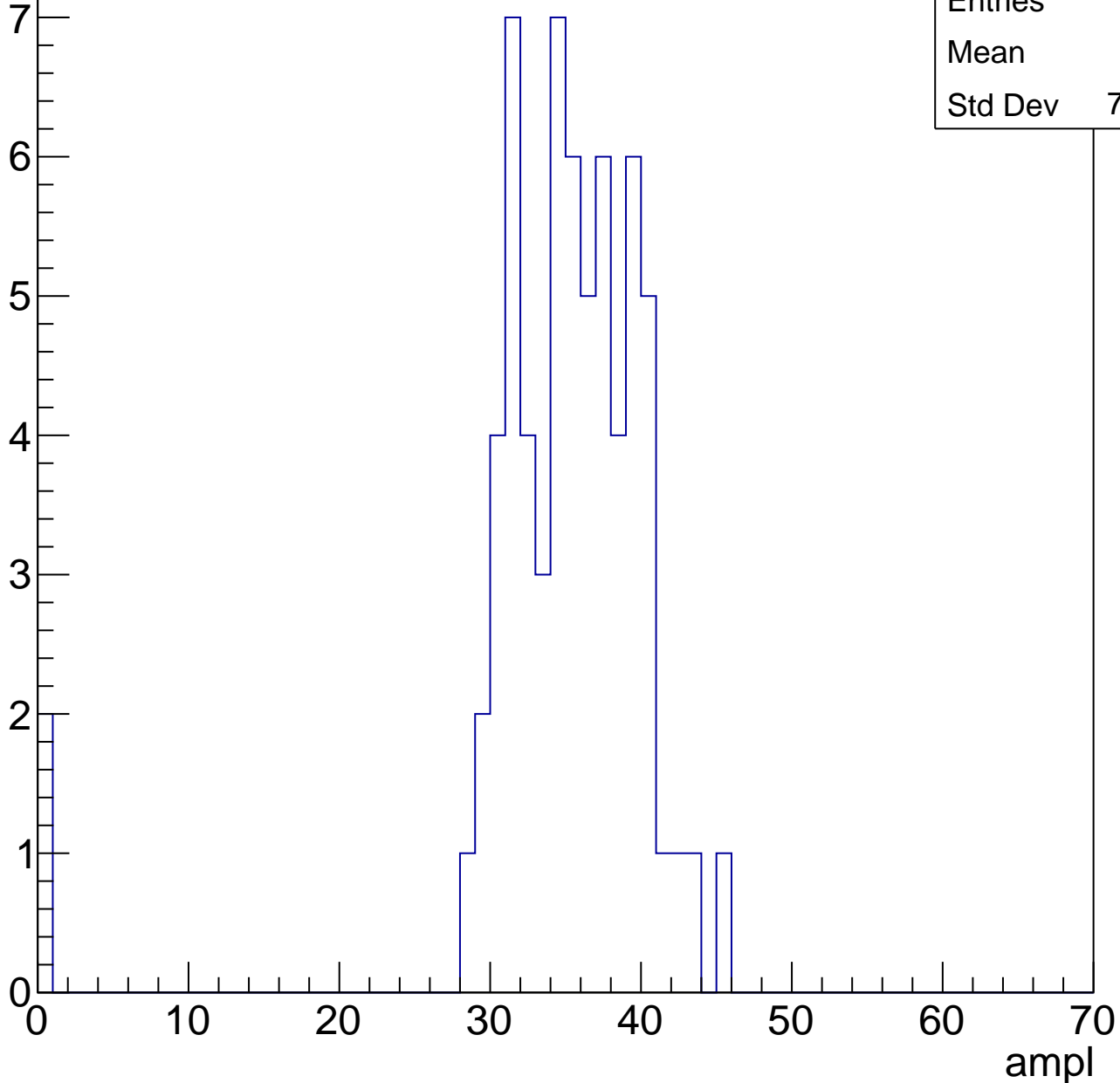
70

B1L103S, U11-ch100, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

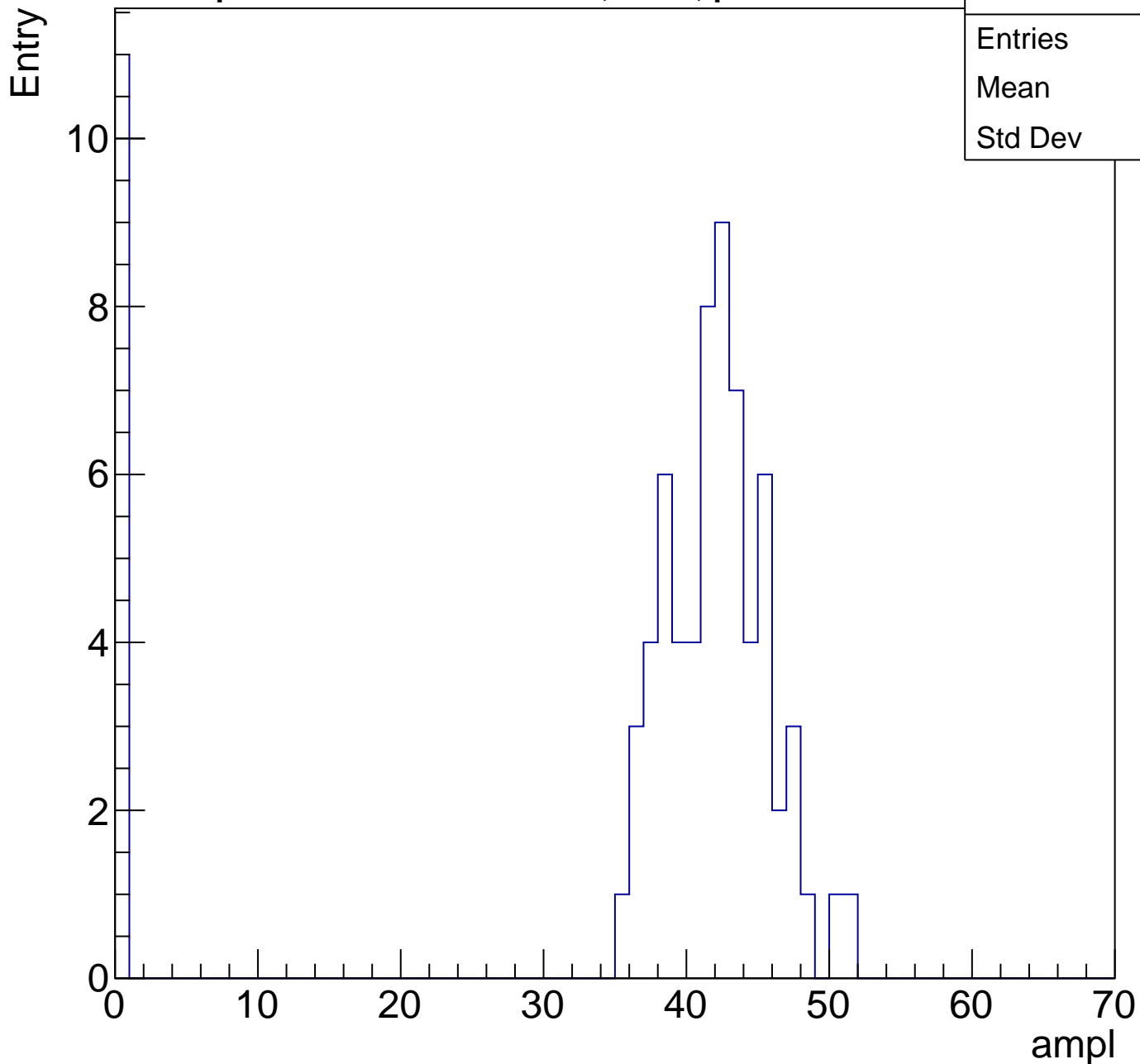
Entries	66
Mean	34.2
Std Dev	7.104



B1L103S, U11-ch100, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	35.6
Std Dev	15.1

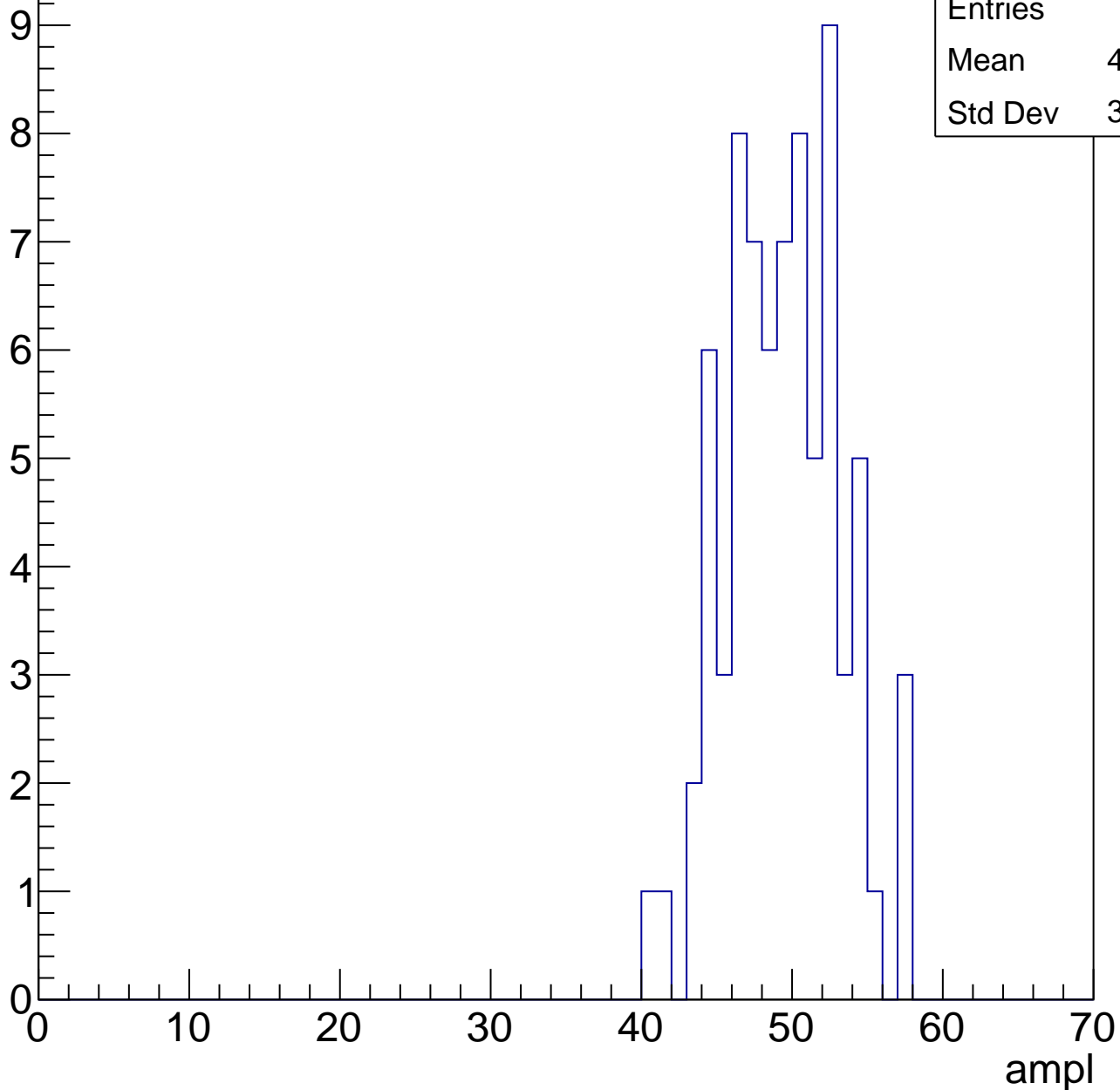


B1L103S, U11-ch100, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	48.96
Std Dev	3.707

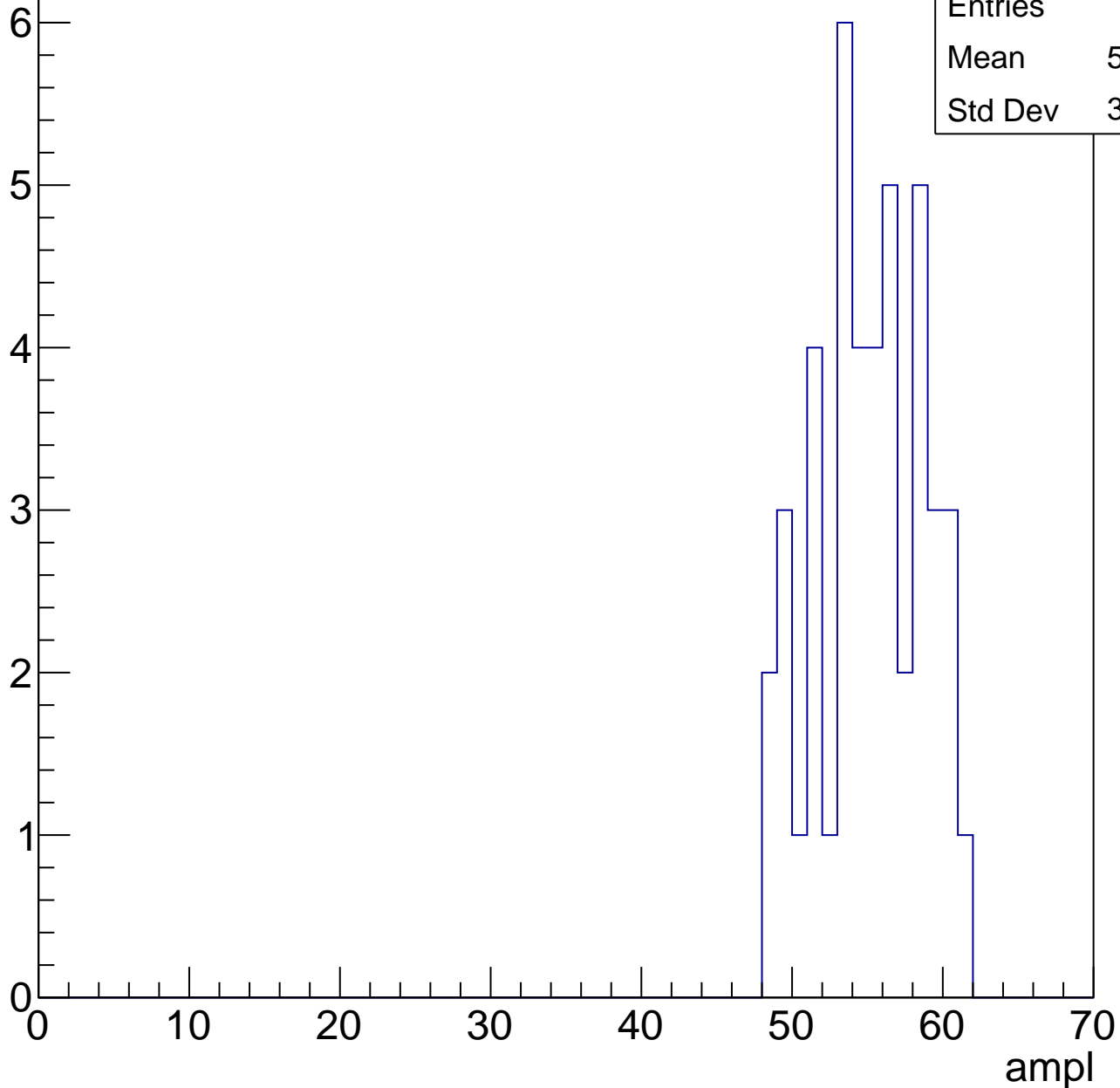


B1L103S, U11-ch100, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	44
Mean	54.66
Std Dev	3.516



B1L103S, U11-ch100, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entries	62
Mean	58.23
Std Dev	8.051

Entry

10

8

6

4

2

0

0

10

20

30

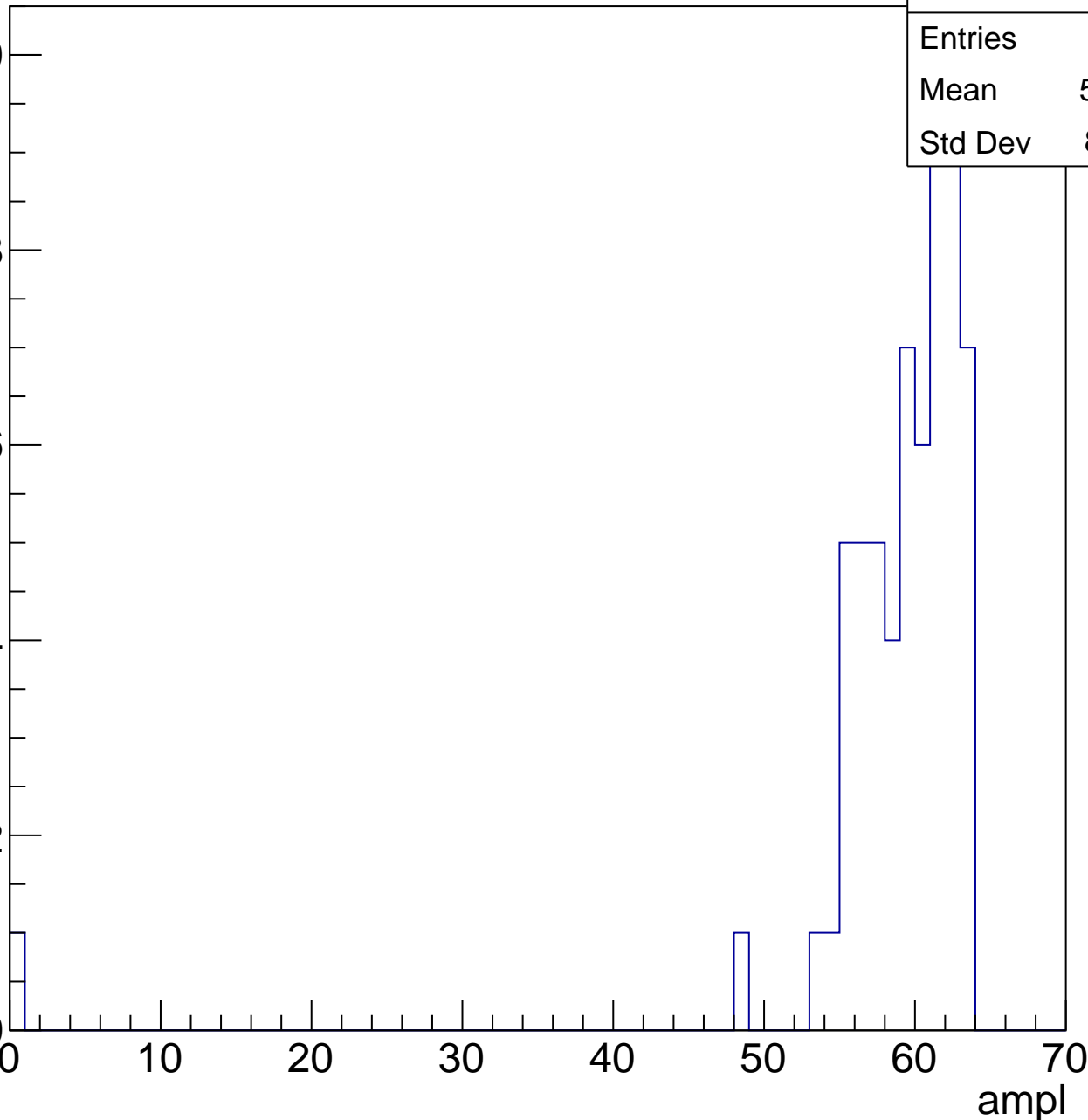
40

50

60

70

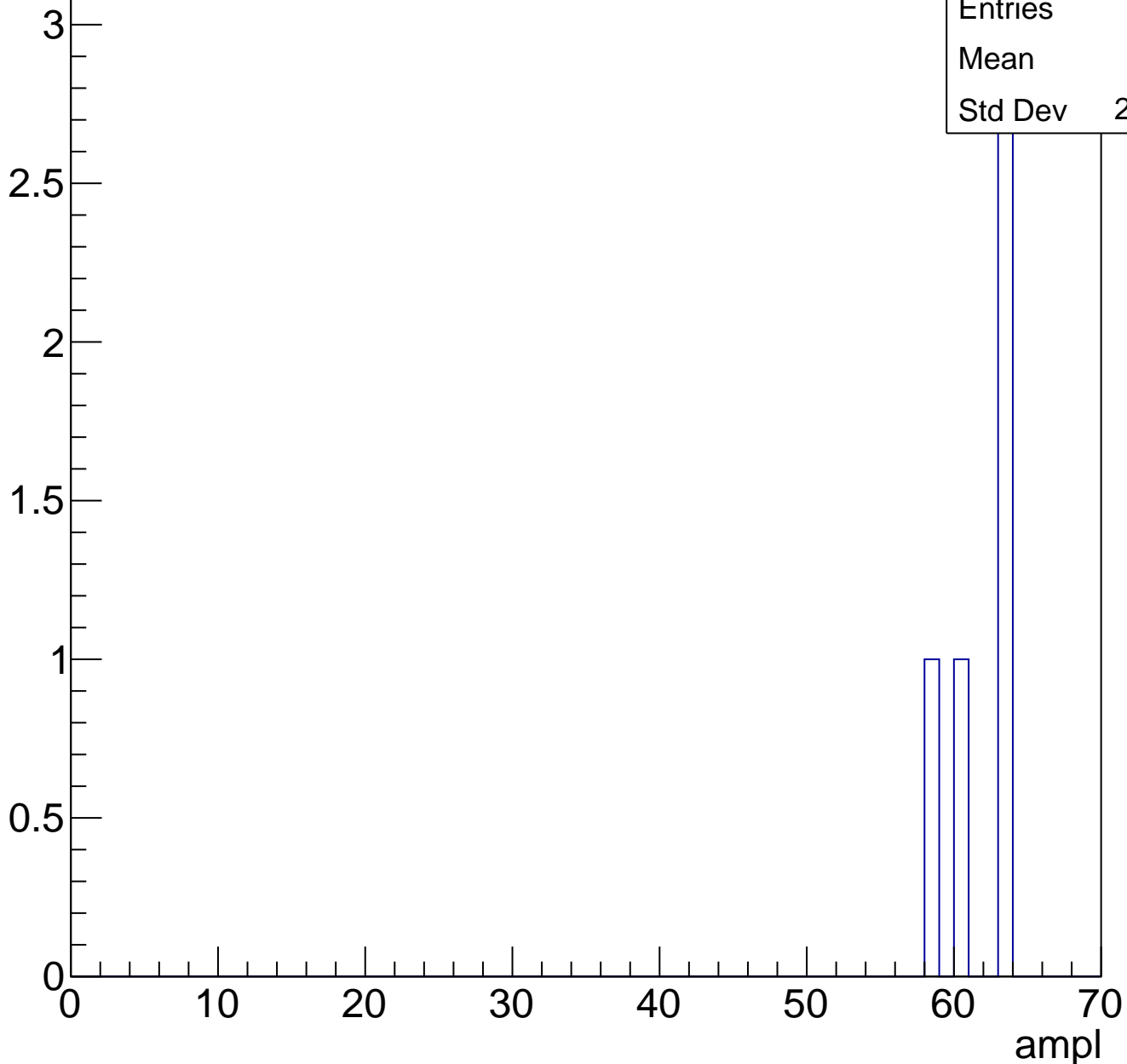
ampl



B1L103S, U11-ch100, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

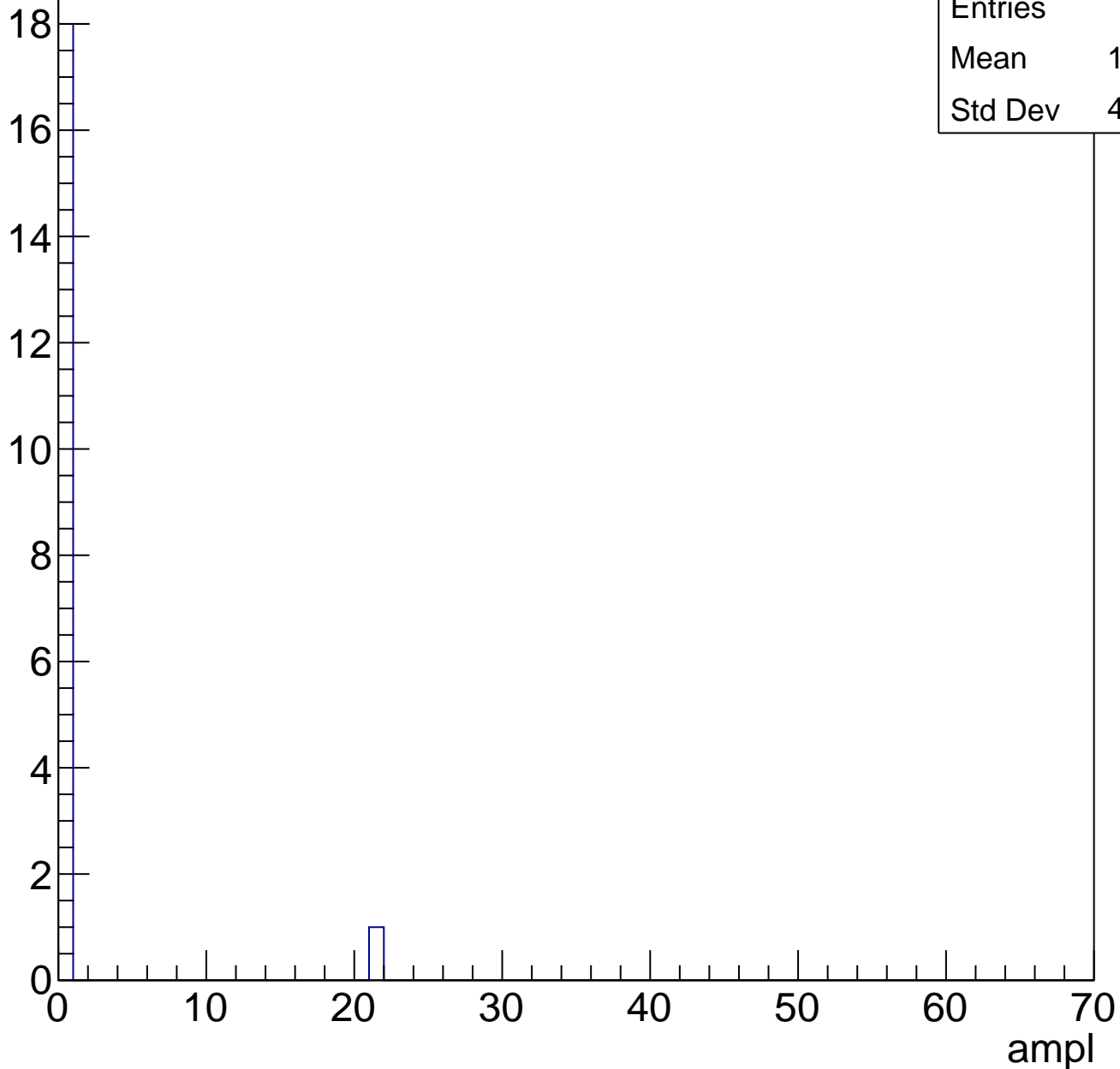


B1L103S, U11-ch100, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.105
Std Dev	4.689

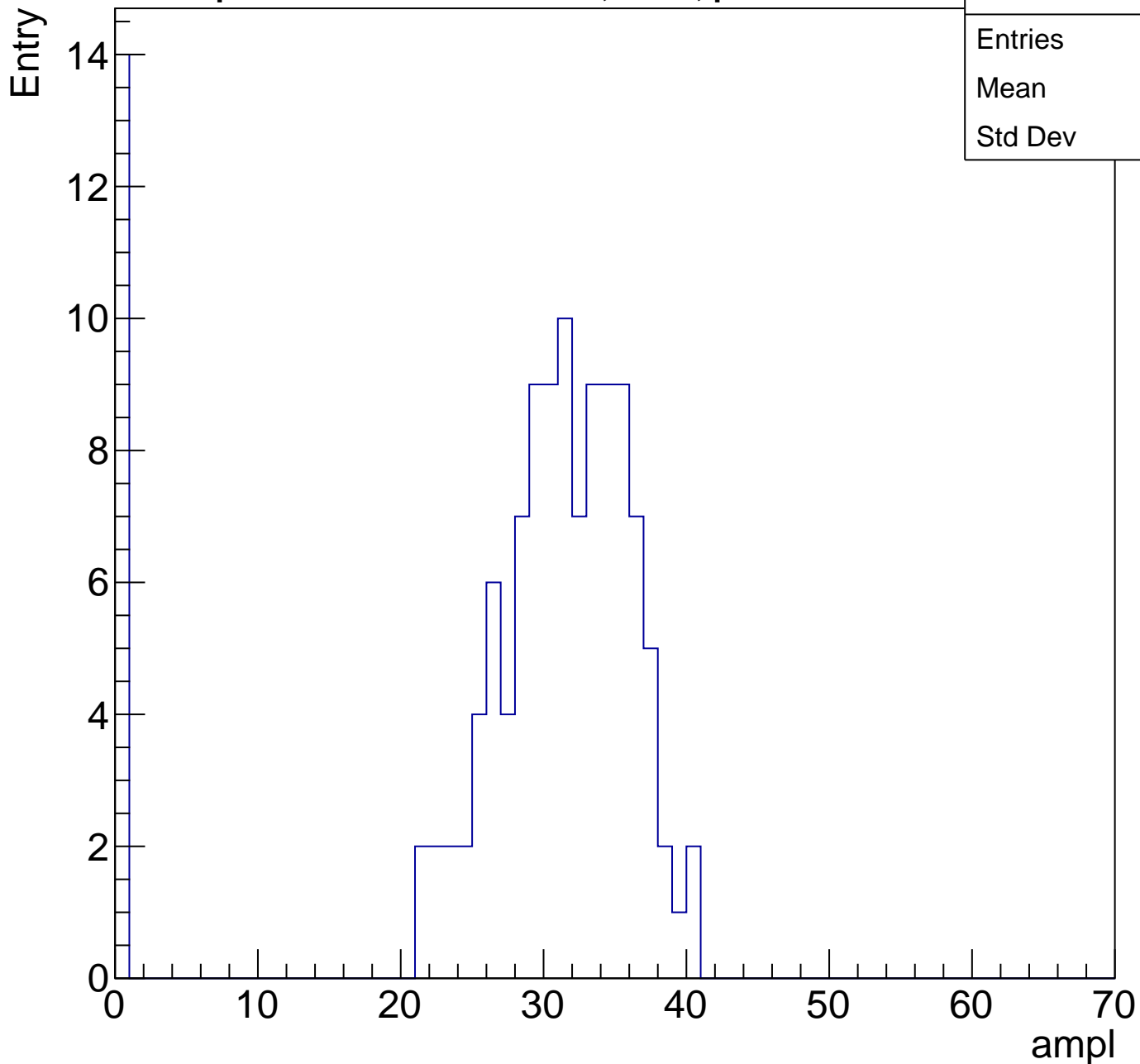
Entry



B1L103S, U11-ch101, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	122
Mean	27.5
Std Dev	10.7

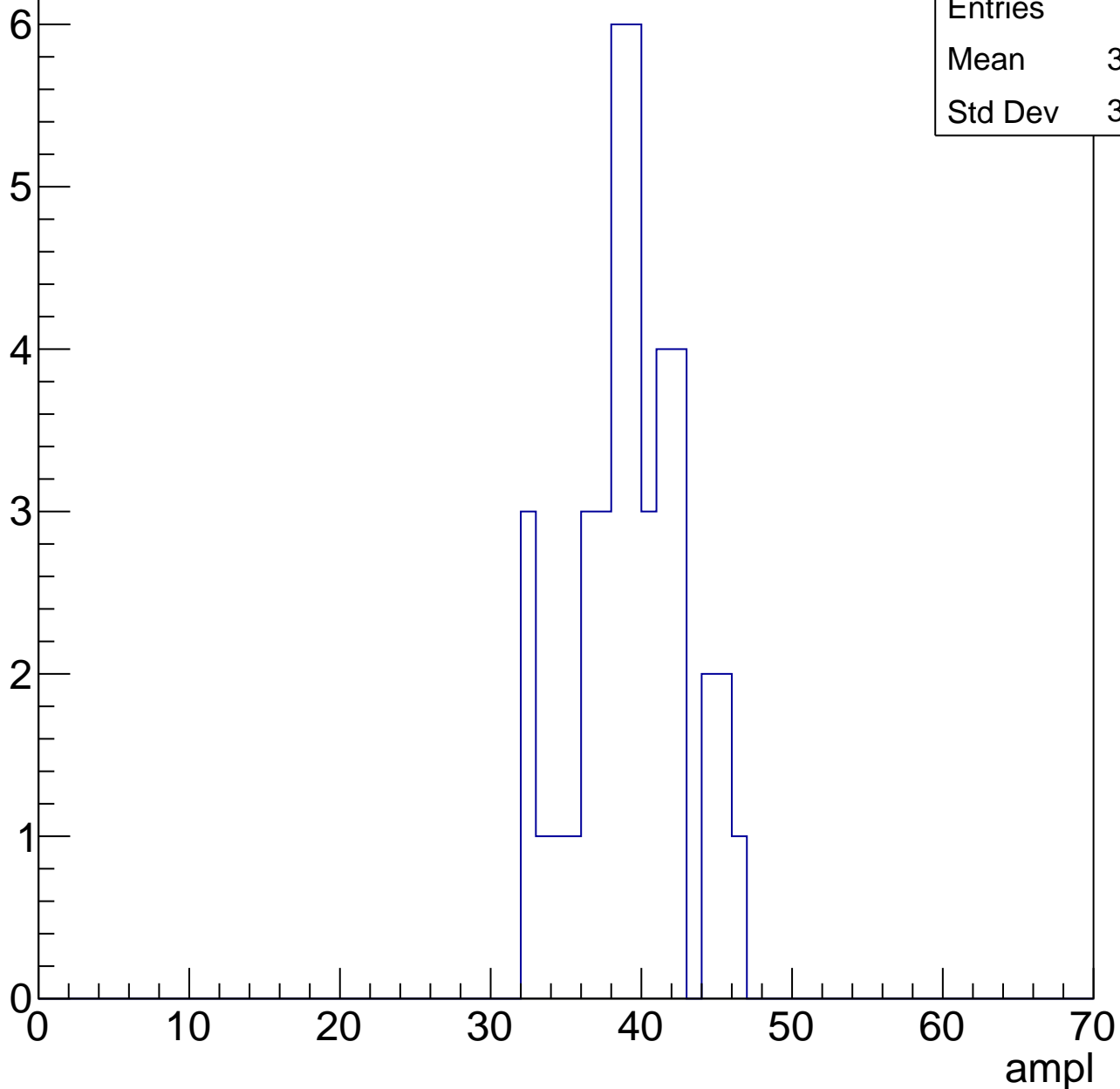


B1L103S, U11-ch101, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	38.88
Std Dev	3.516

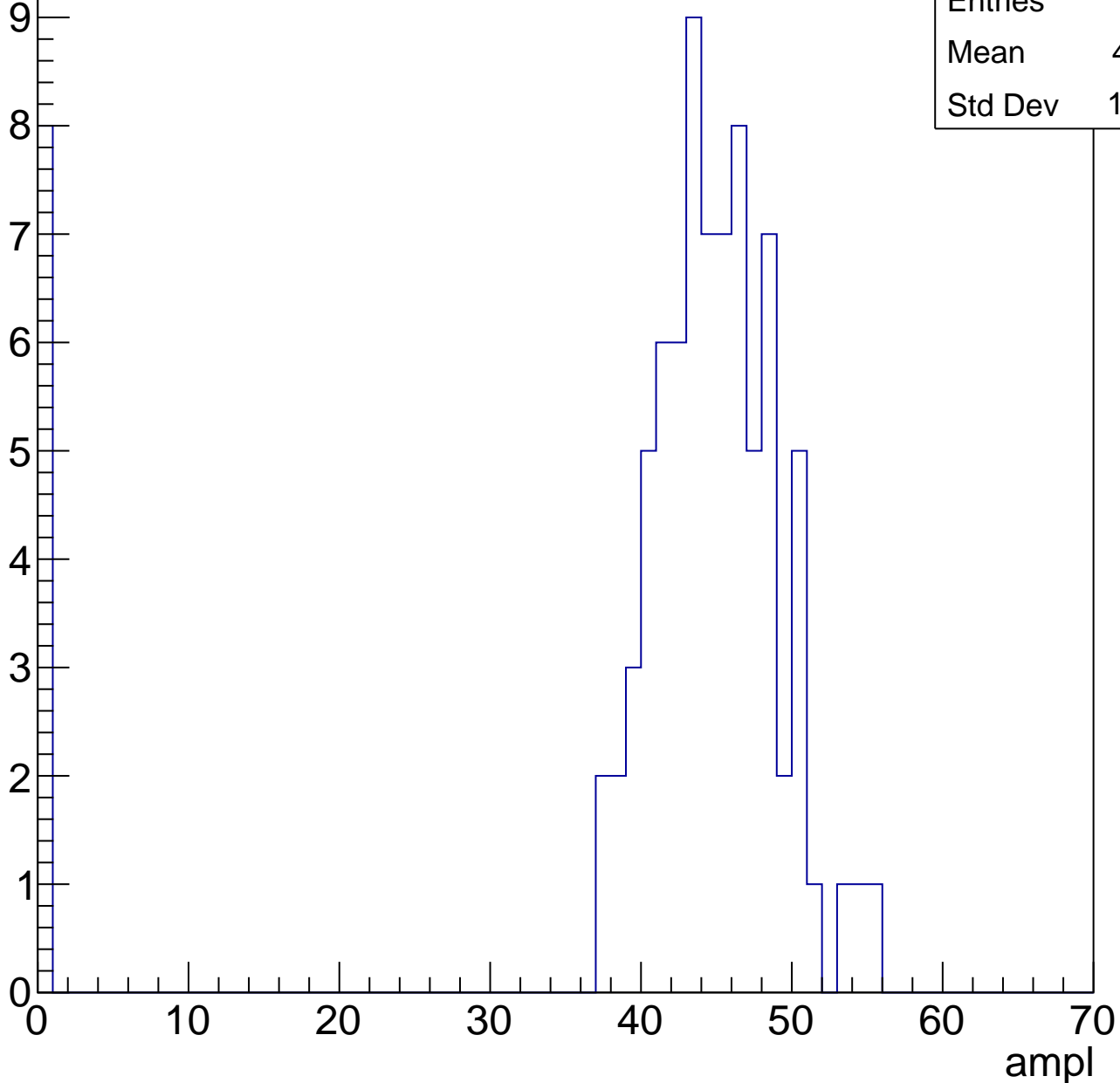


B1L103S, U11-ch101, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	86
Mean	40.41
Std Dev	13.45

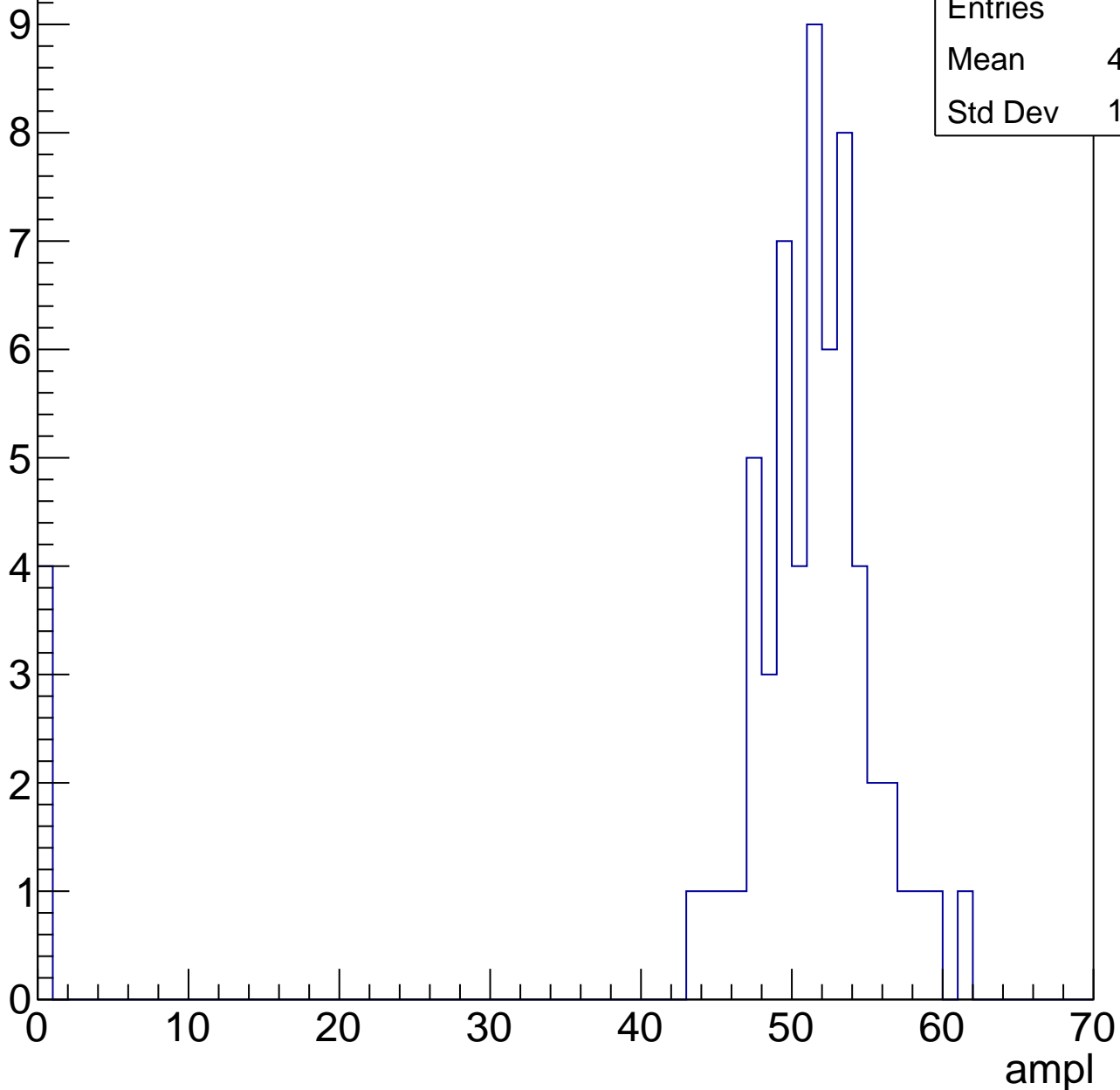


B1L103S, U11-ch101, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	47.87
Std Dev	13.02

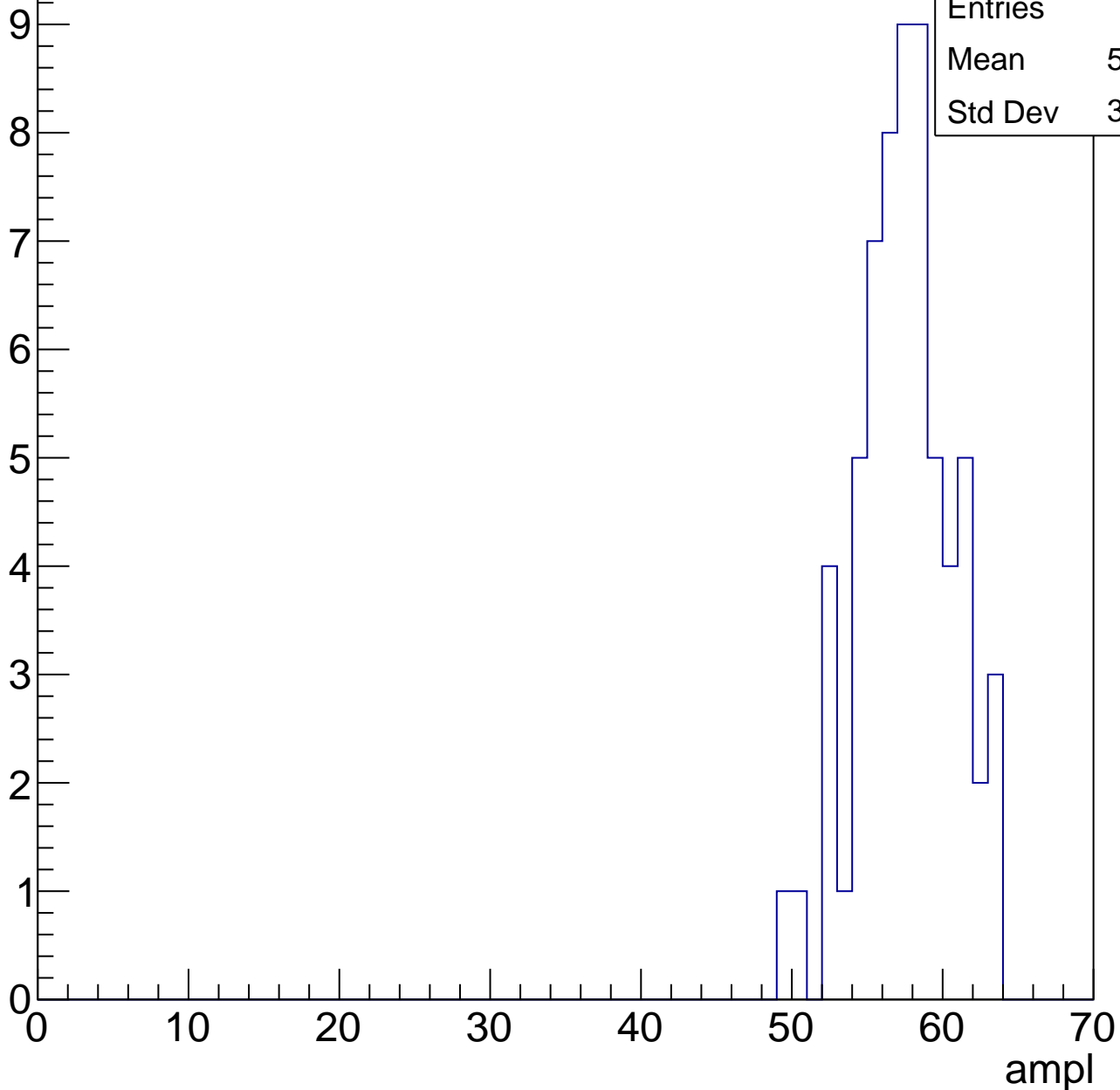


B1L103S, U11-ch101, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	57.05
Std Dev	3.094

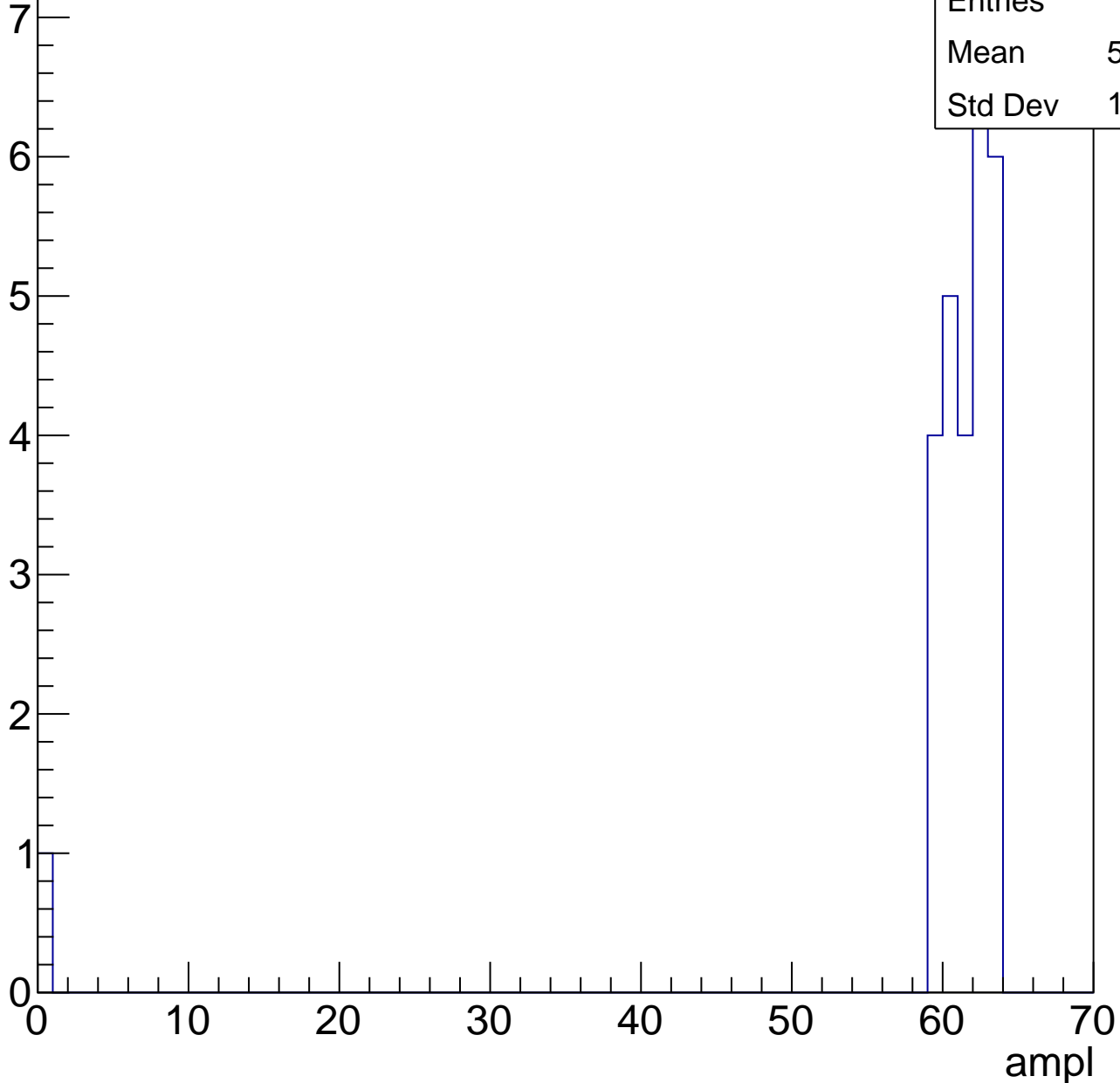


B1L103S, U11-ch101, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	27
Mean	58.96
Std Dev	11.64



B1L103S, U11-ch101, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch101, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	18
Mean	0
Std Dev	0

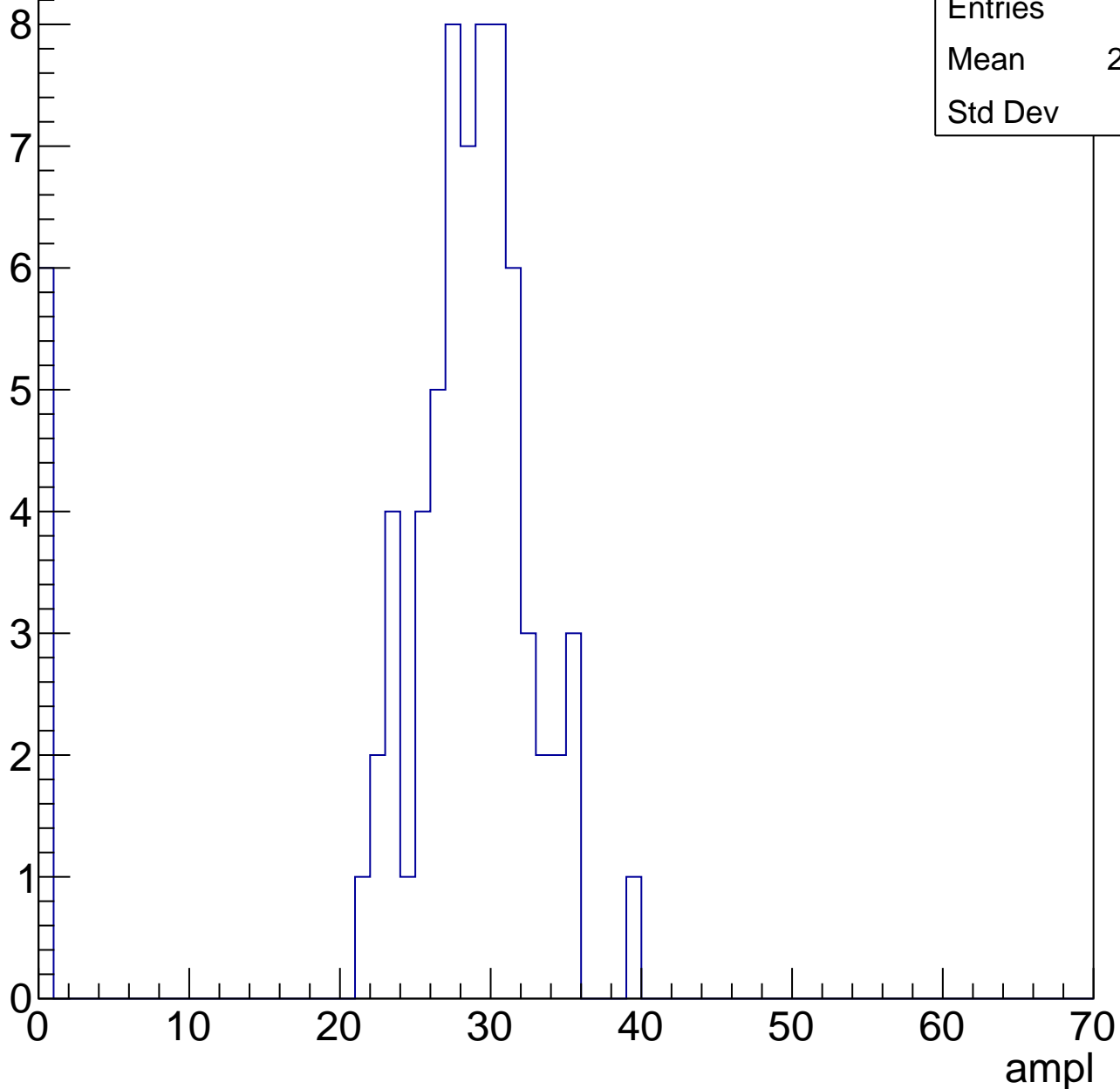
ampl

B1L103S, U11-ch102, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	26.13
Std Dev	8.63

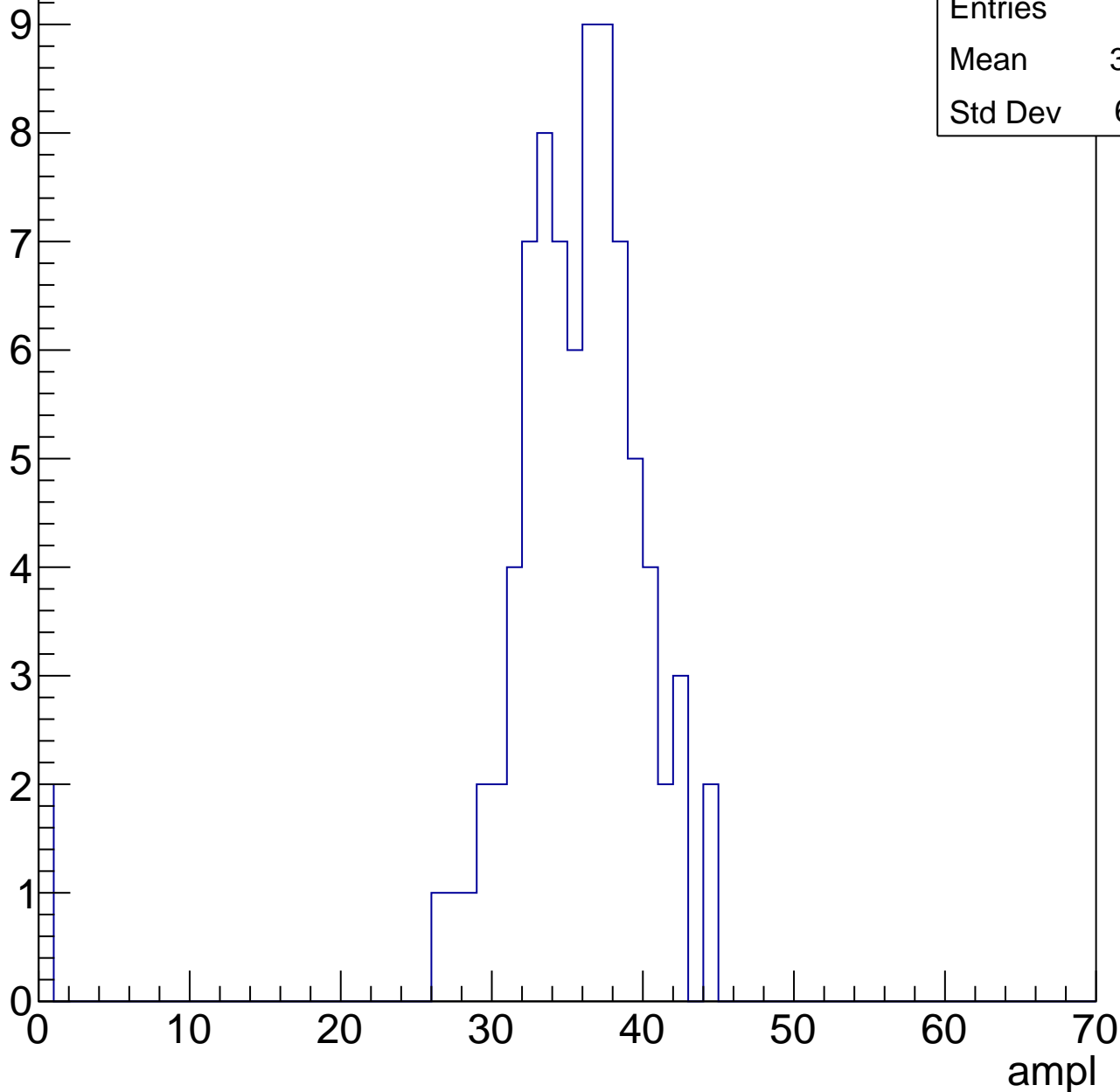


B1L103S, U11-ch102, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	82
Mean	34.55
Std Dev	6.611

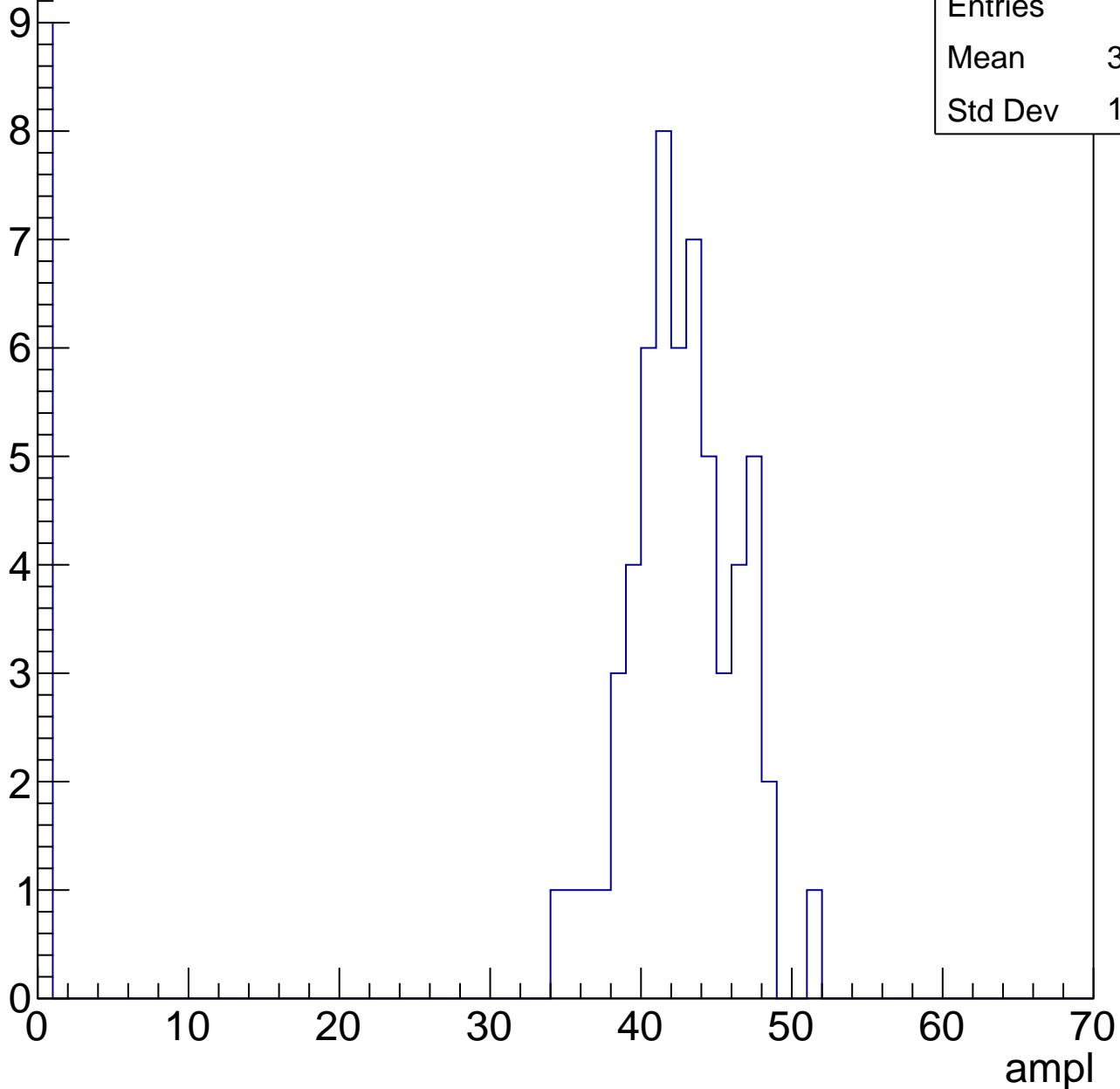


B1L103S, U11-ch102, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	36.63
Std Dev	14.78

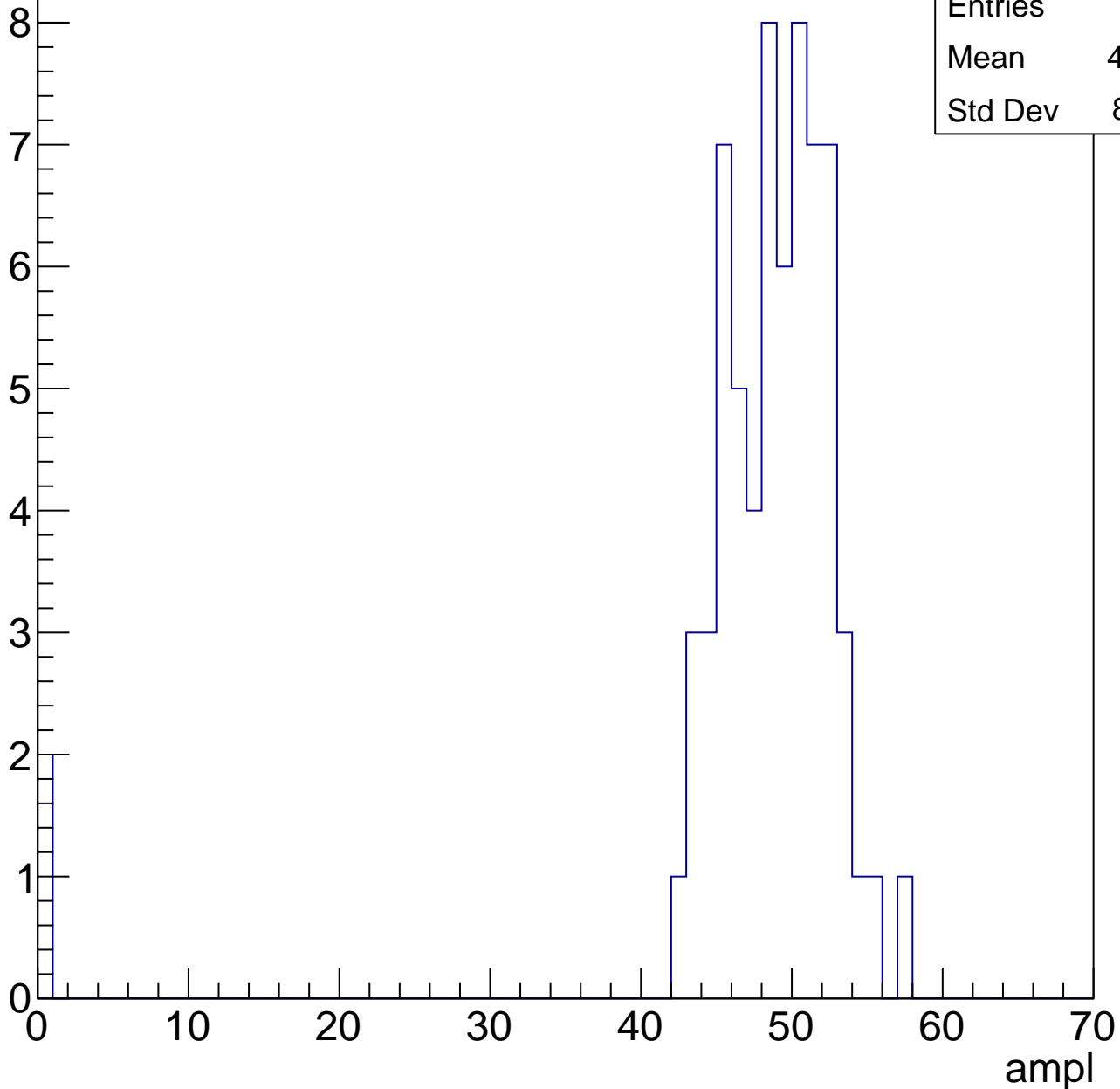


B1L103S, U11-ch102, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	47.16
Std Dev	8.861

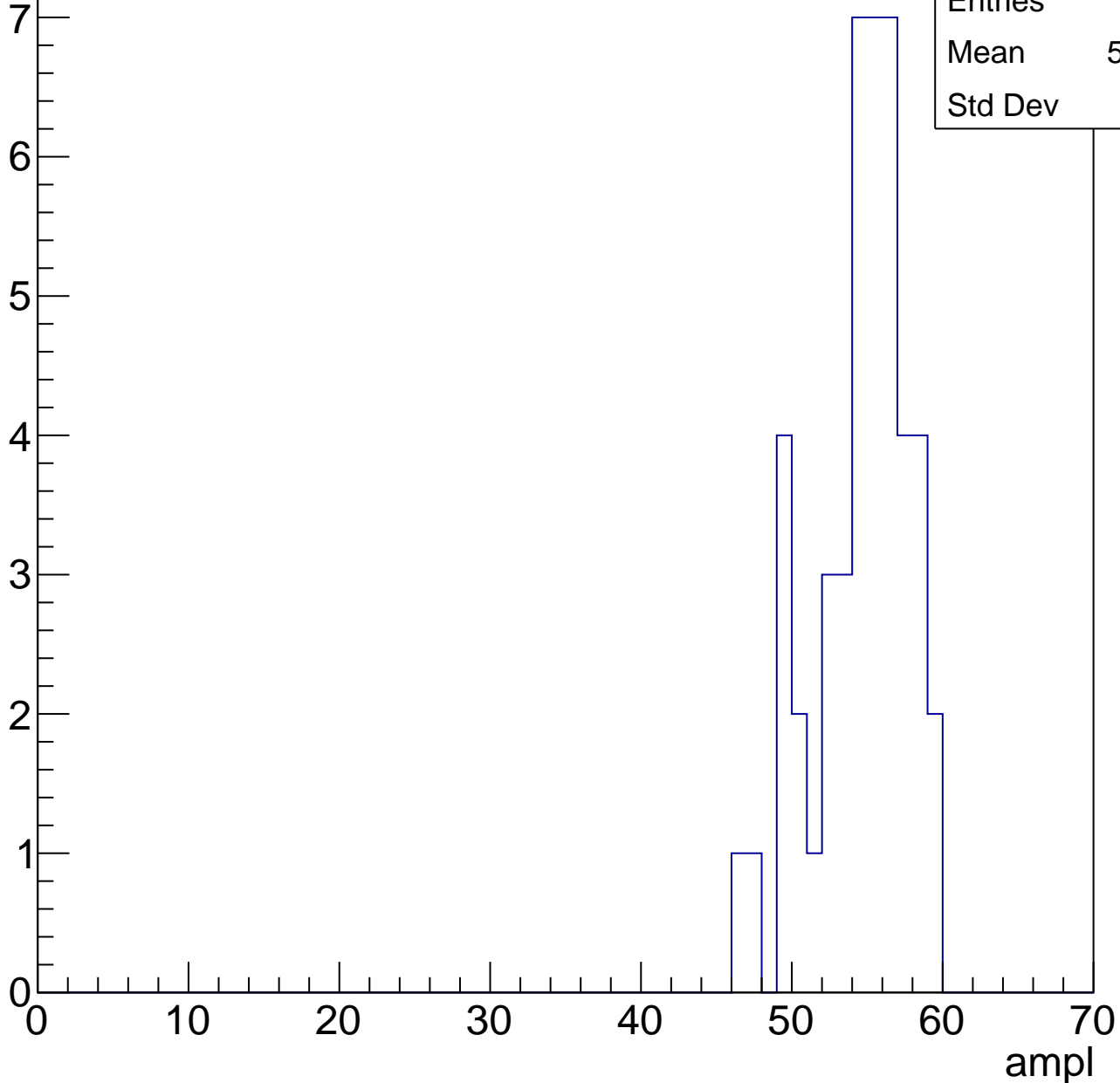


B1L103S, U11-ch102, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	46
Mean	54.09
Std Dev	3.14

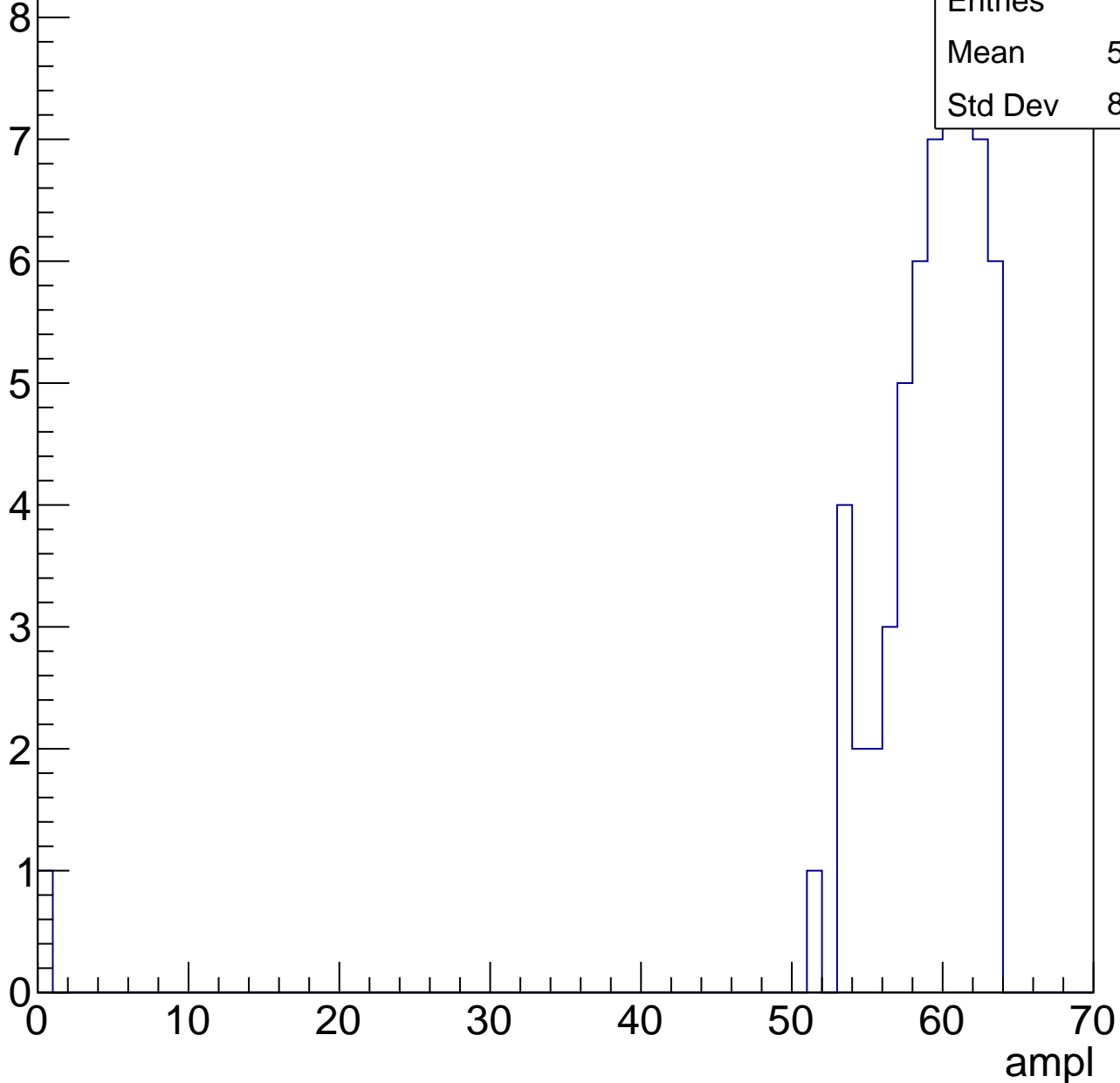


B1L103S, U11-ch102, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	57.92
Std Dev	8.116



B1L103S, U11-ch102, adc6

calib_packv5_041523_1651.root, FC#0, port C2

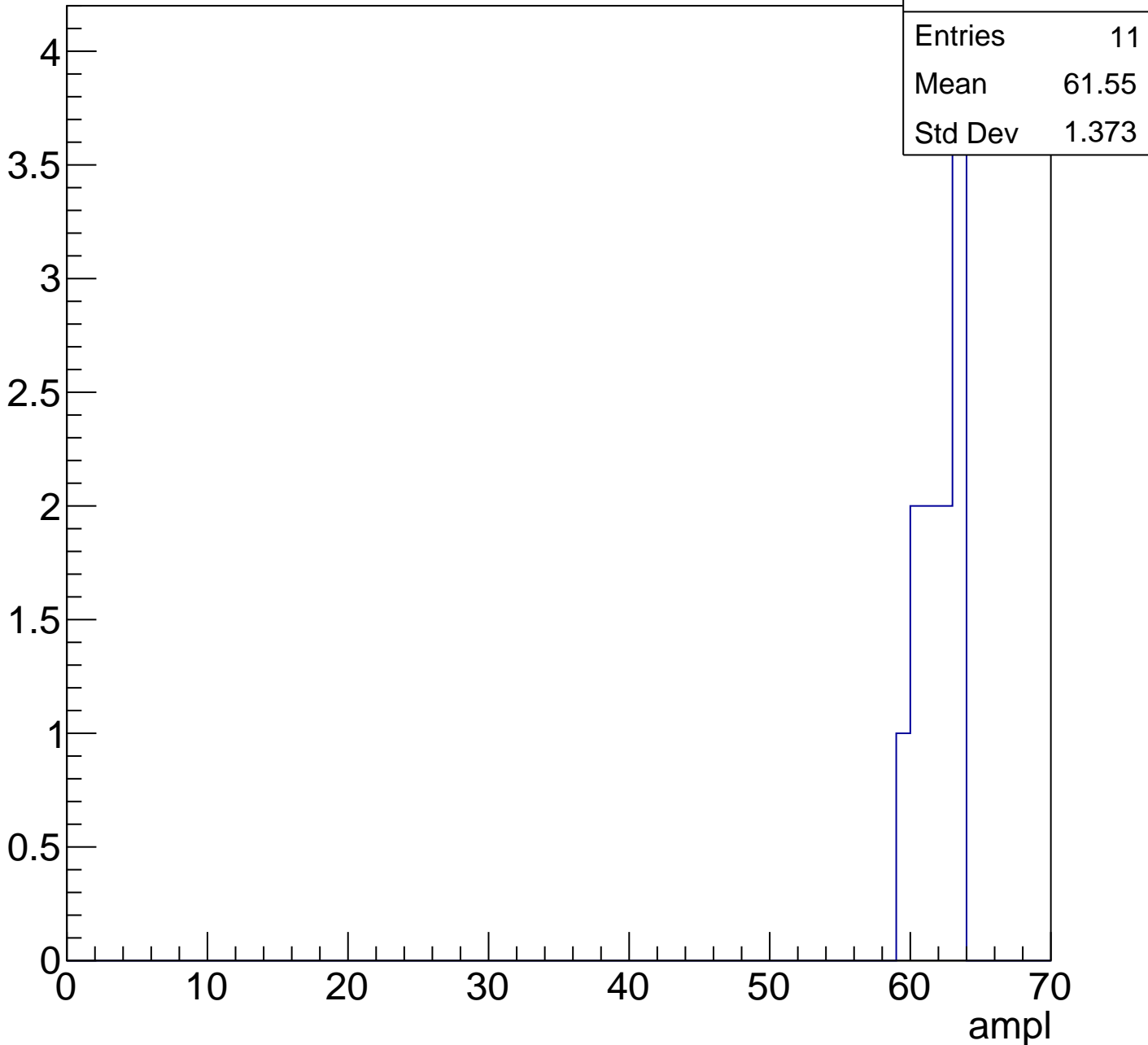
Entry

4
3.5
3
2.5
2
1.5
1
0.5
0

Entries	11
Mean	61.55
Std Dev	1.373

0 10 20 30 40 50 60 70

ampl



B1L103S, U11-ch102, adc7

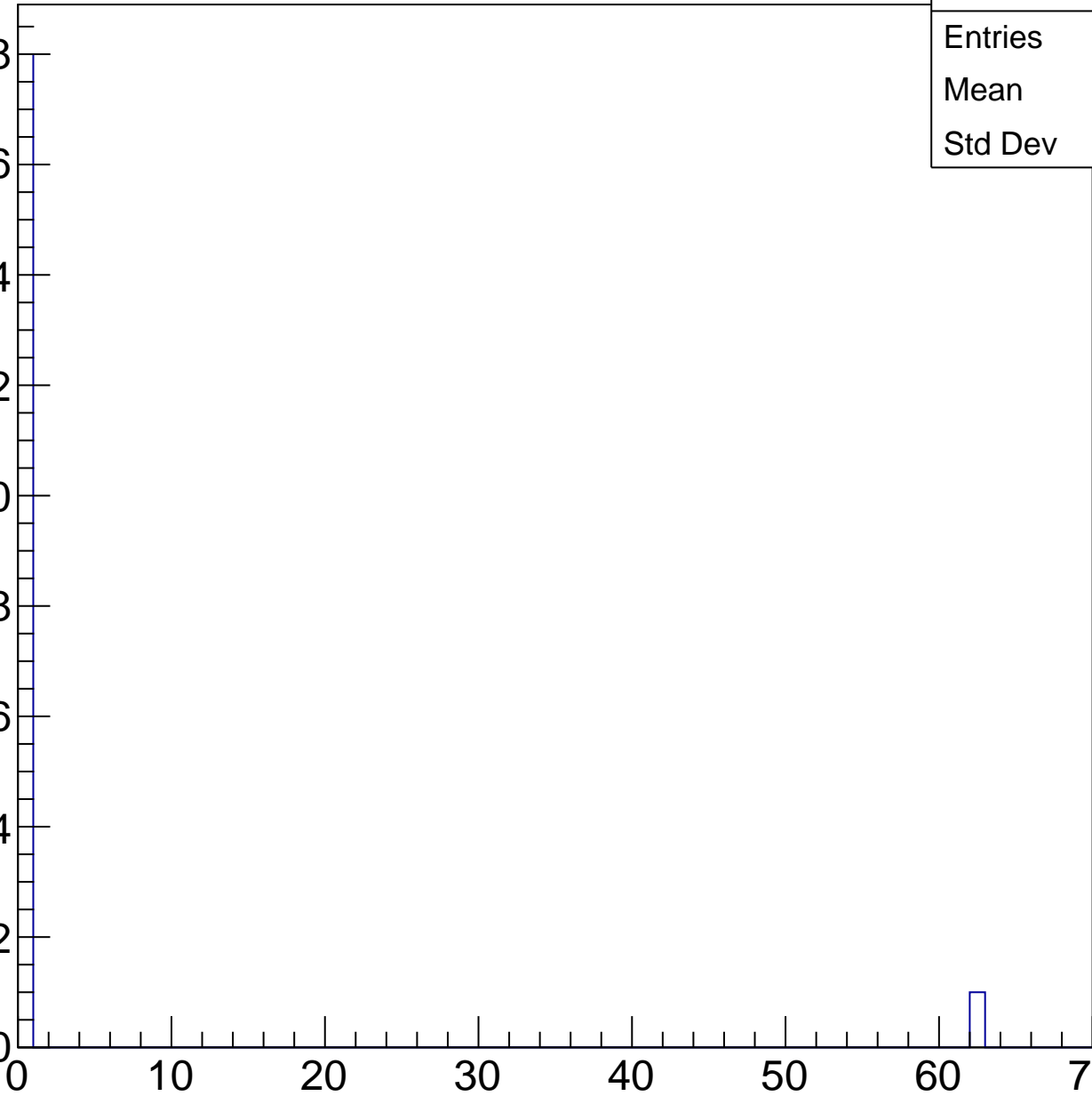
calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	3.263
Std Dev	13.84

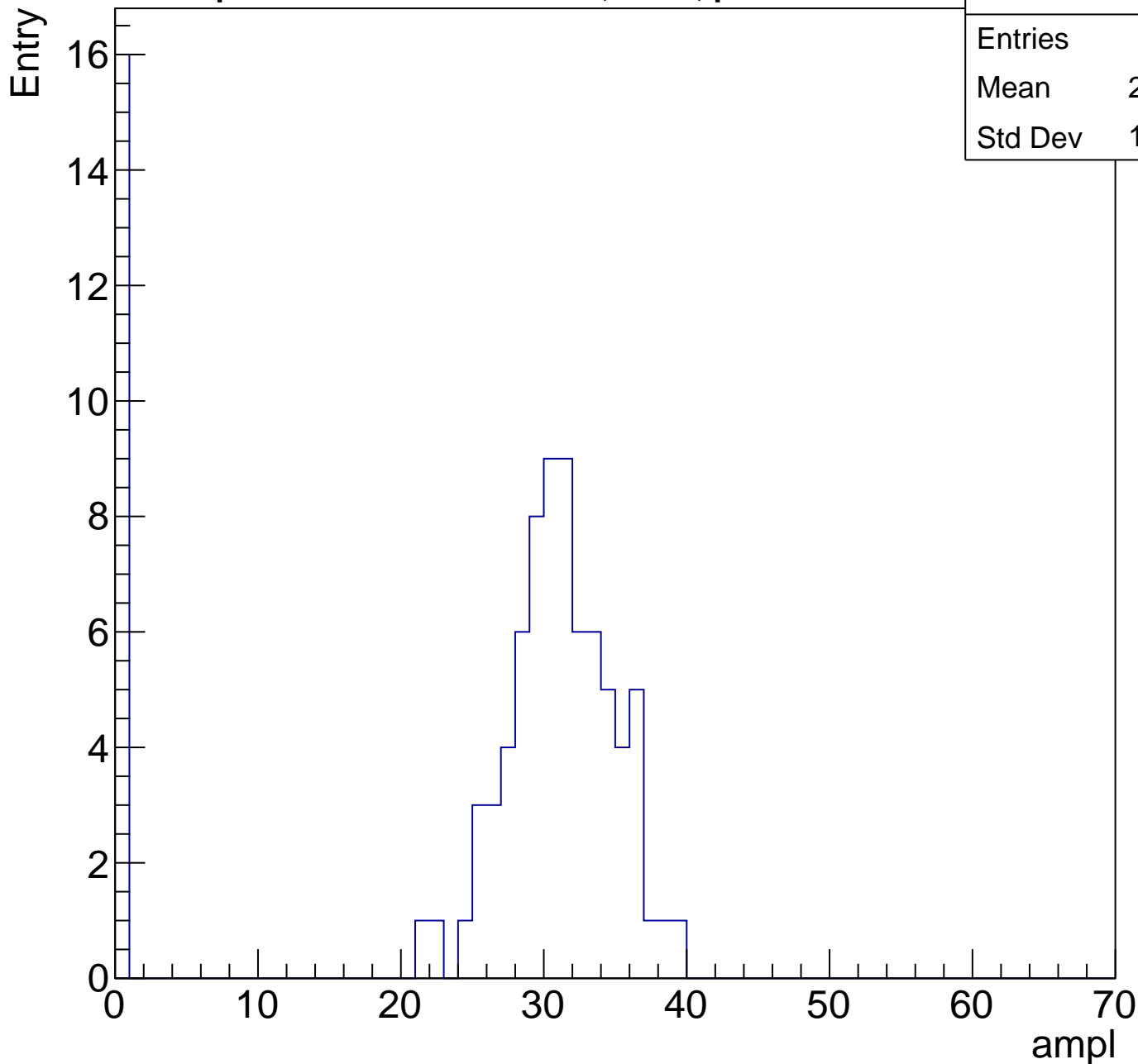
ampl



B1L103S, U11-ch103, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	90
Mean	25.23
Std Dev	12.19



B1L103S, U11-ch103, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	93
Mean	34
Std Dev	12.98

Entry

10

8

6

4

2

0

0

10

20

30

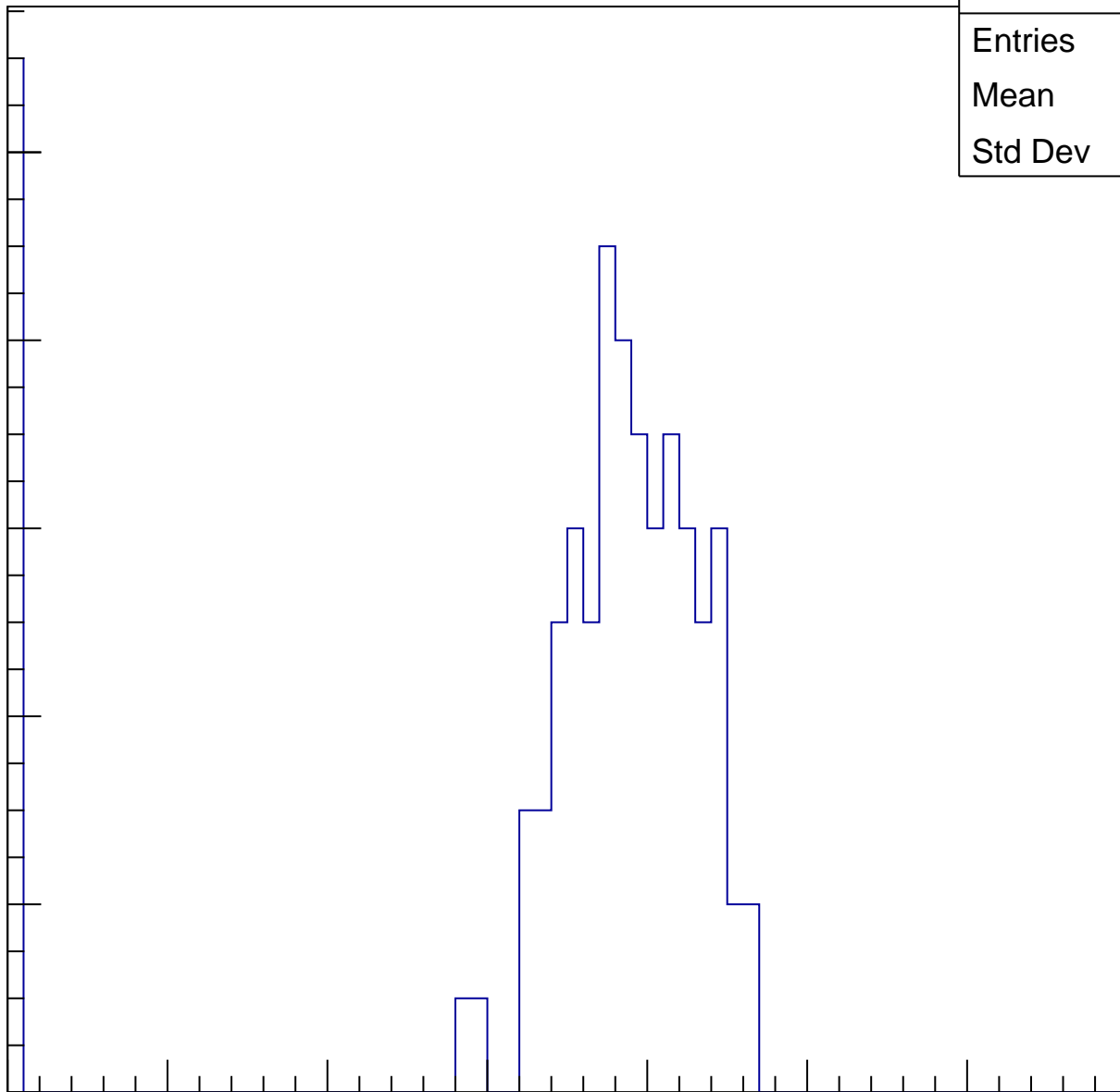
40

50

60

70

ampl

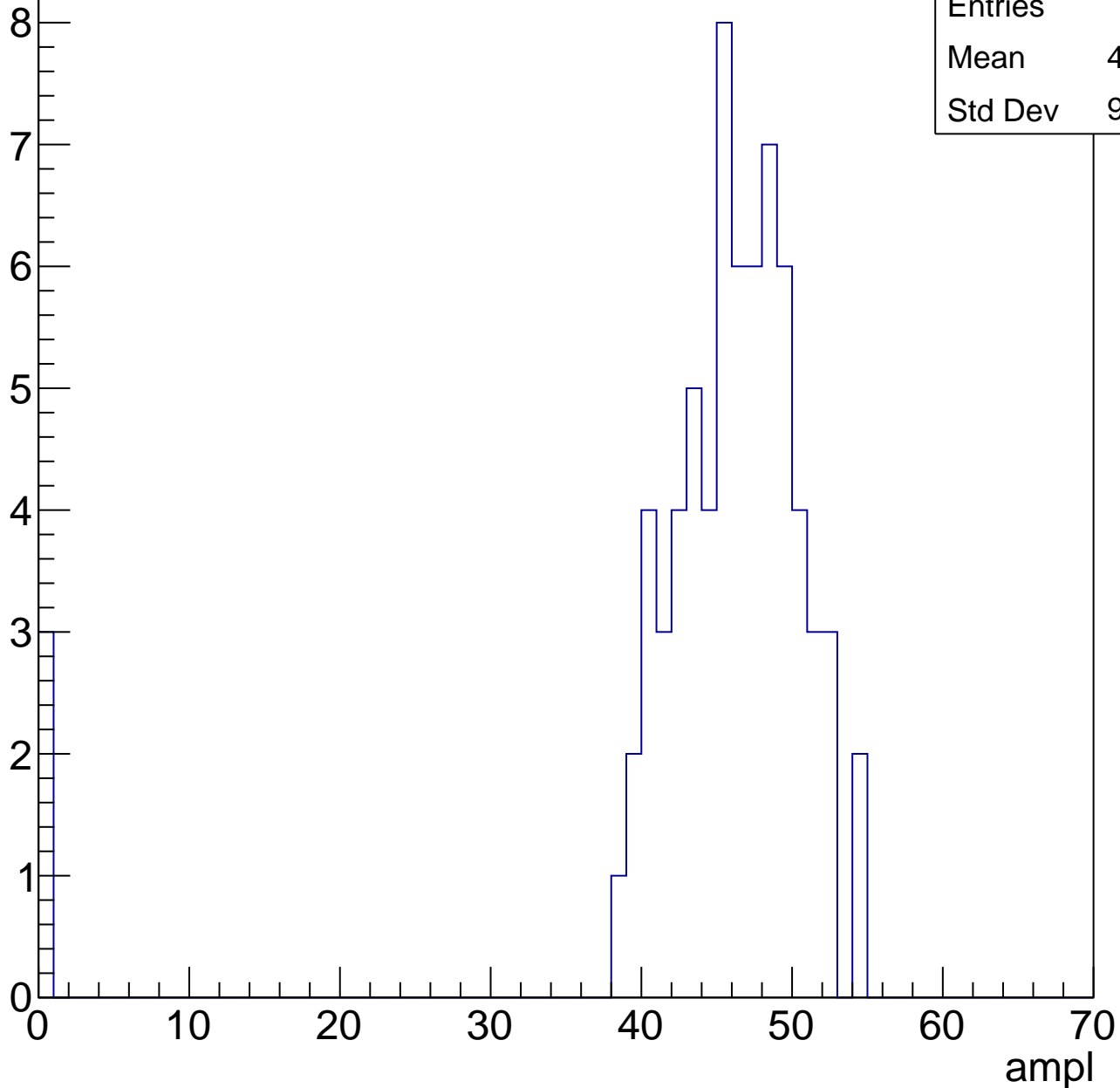


B1L103S, U11-ch103, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	43.99
Std Dev	9.956

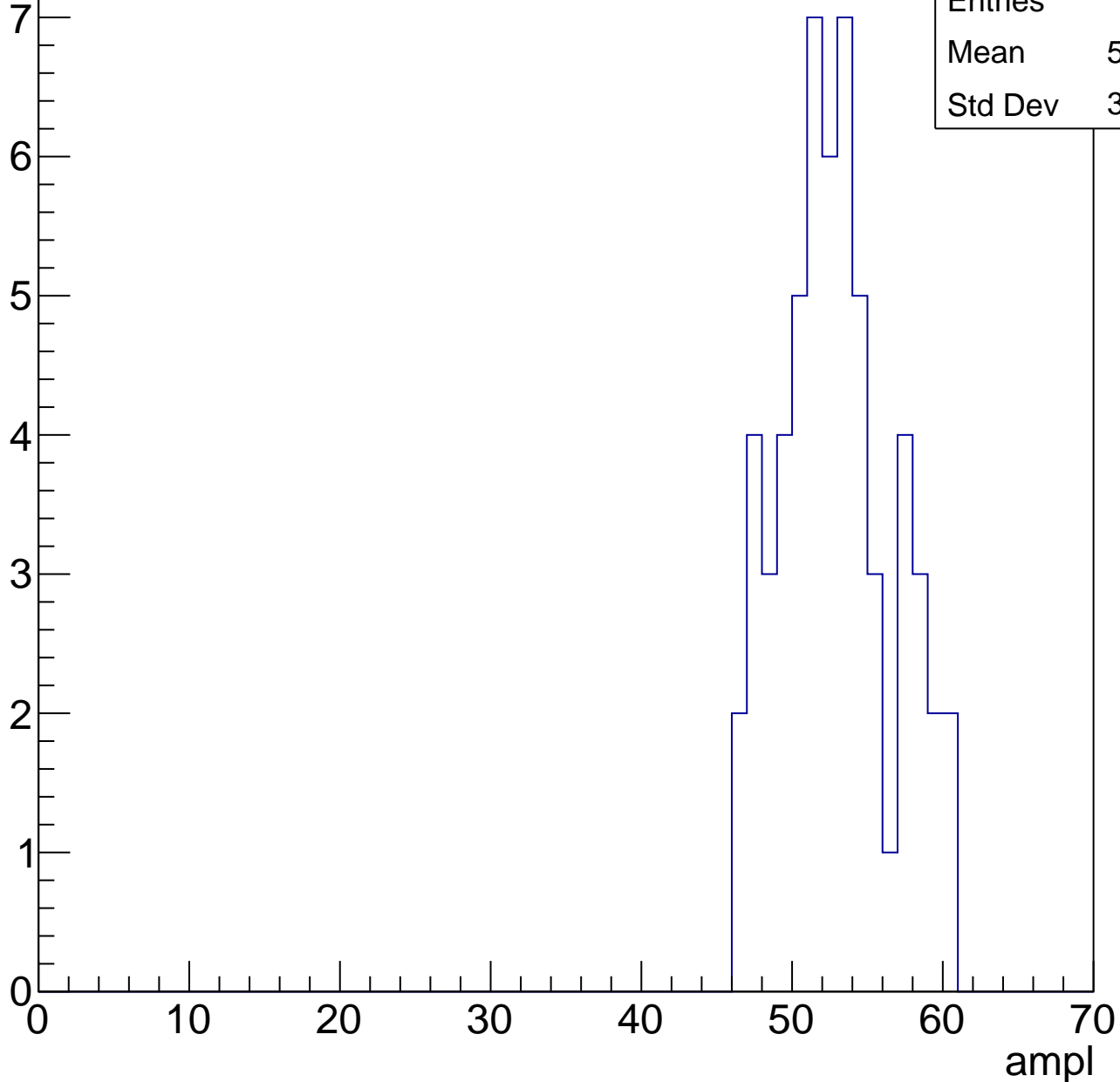


B1L103S, U11-ch103, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	52.43
Std Dev	3.658

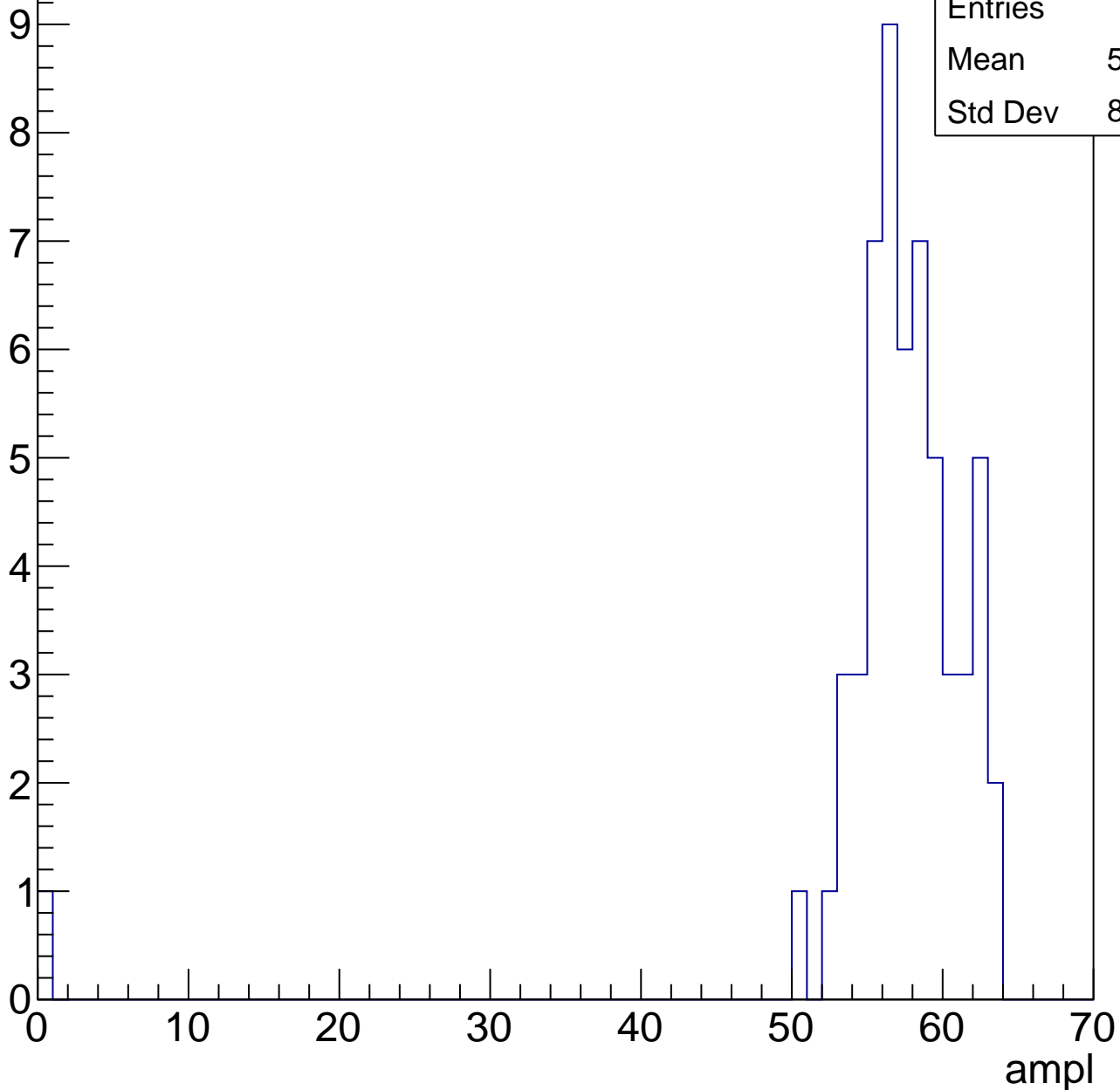


B1L103S, U11-ch103, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	56.32
Std Dev	8.137

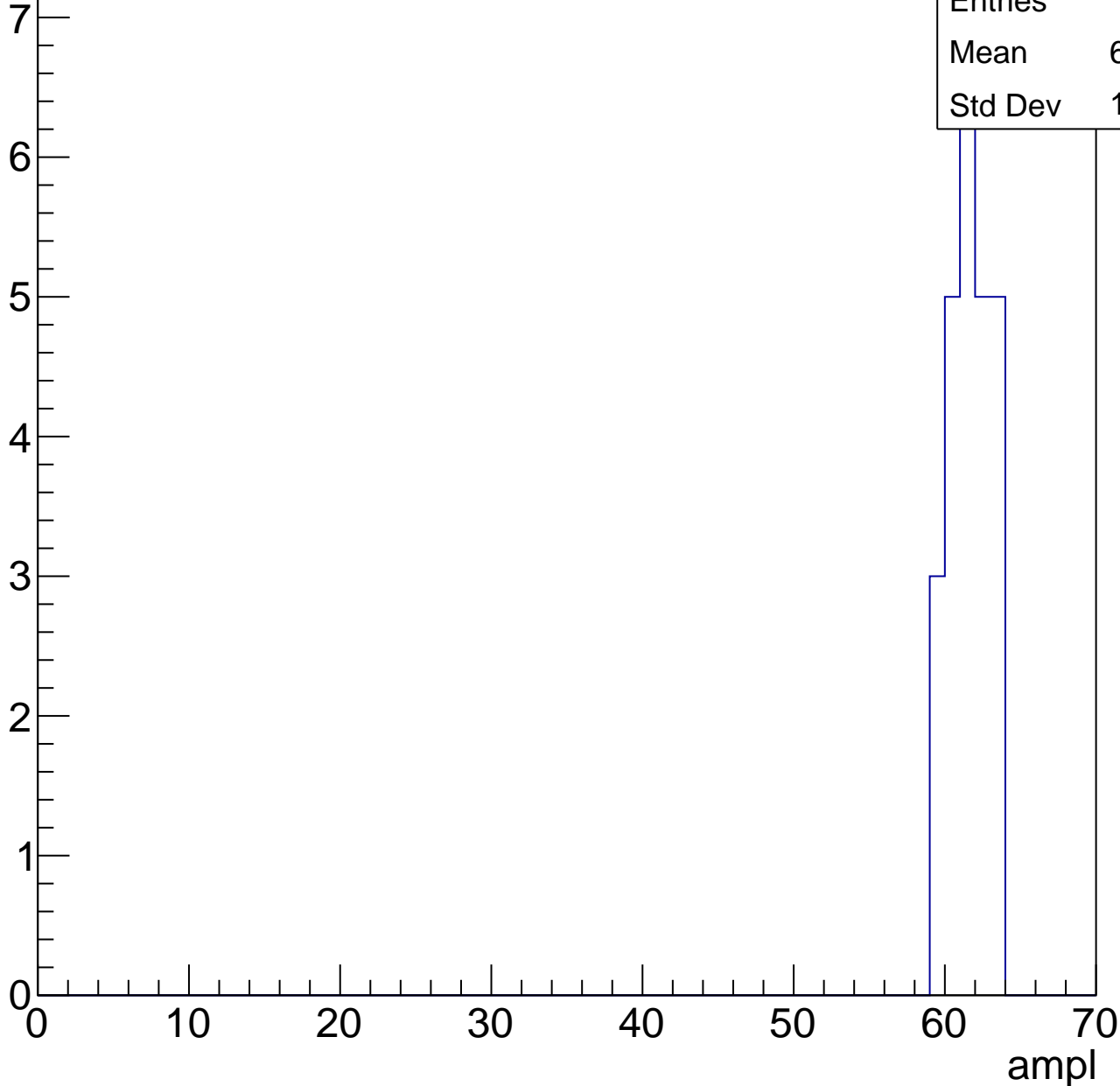


B1L103S, U11-ch103, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	25
Mean	61.16
Std Dev	1.286



B1L103S, U11-ch103, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch103, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

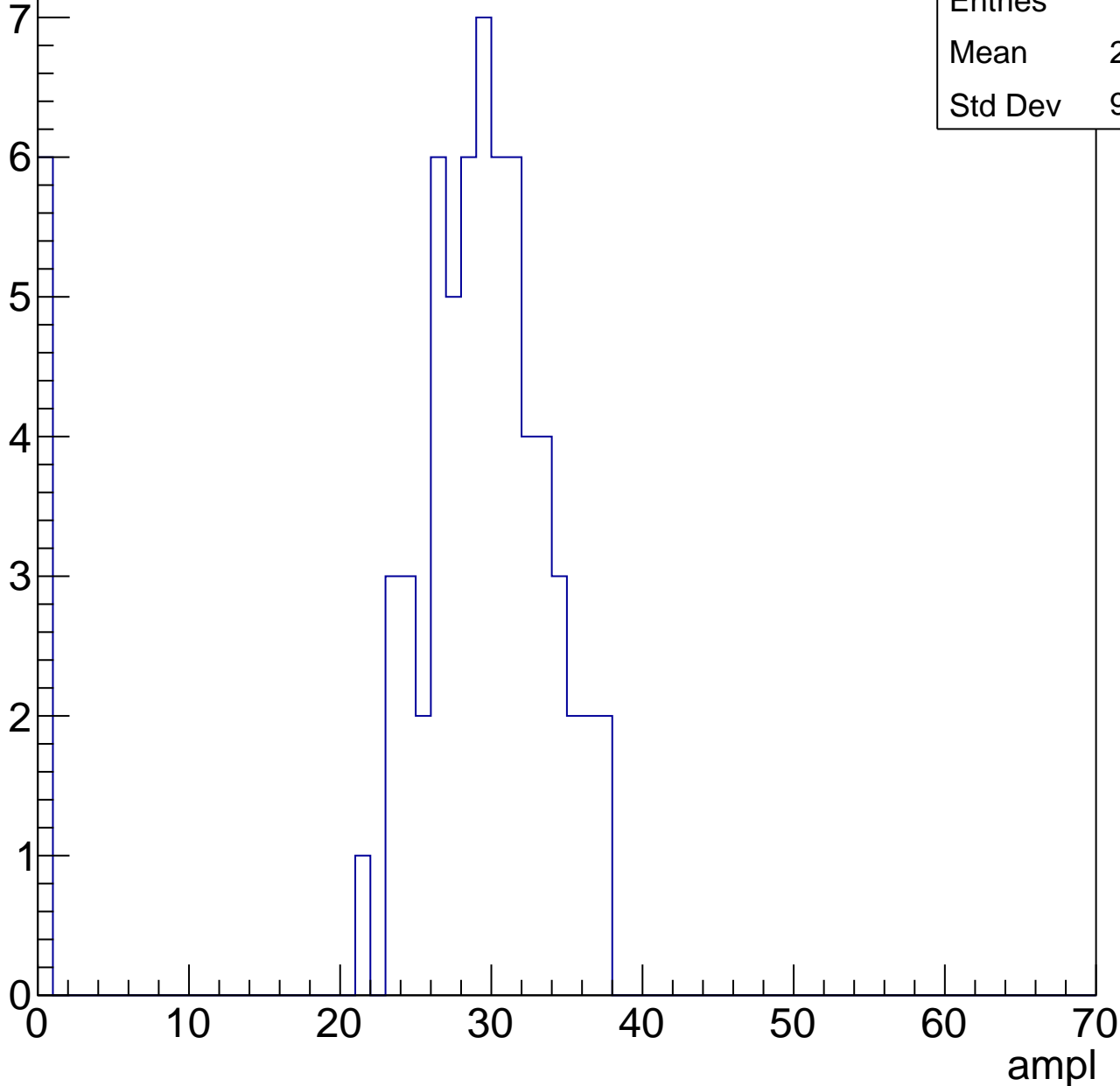


B1L103S, U11-ch104, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	26.74
Std Dev	9.042

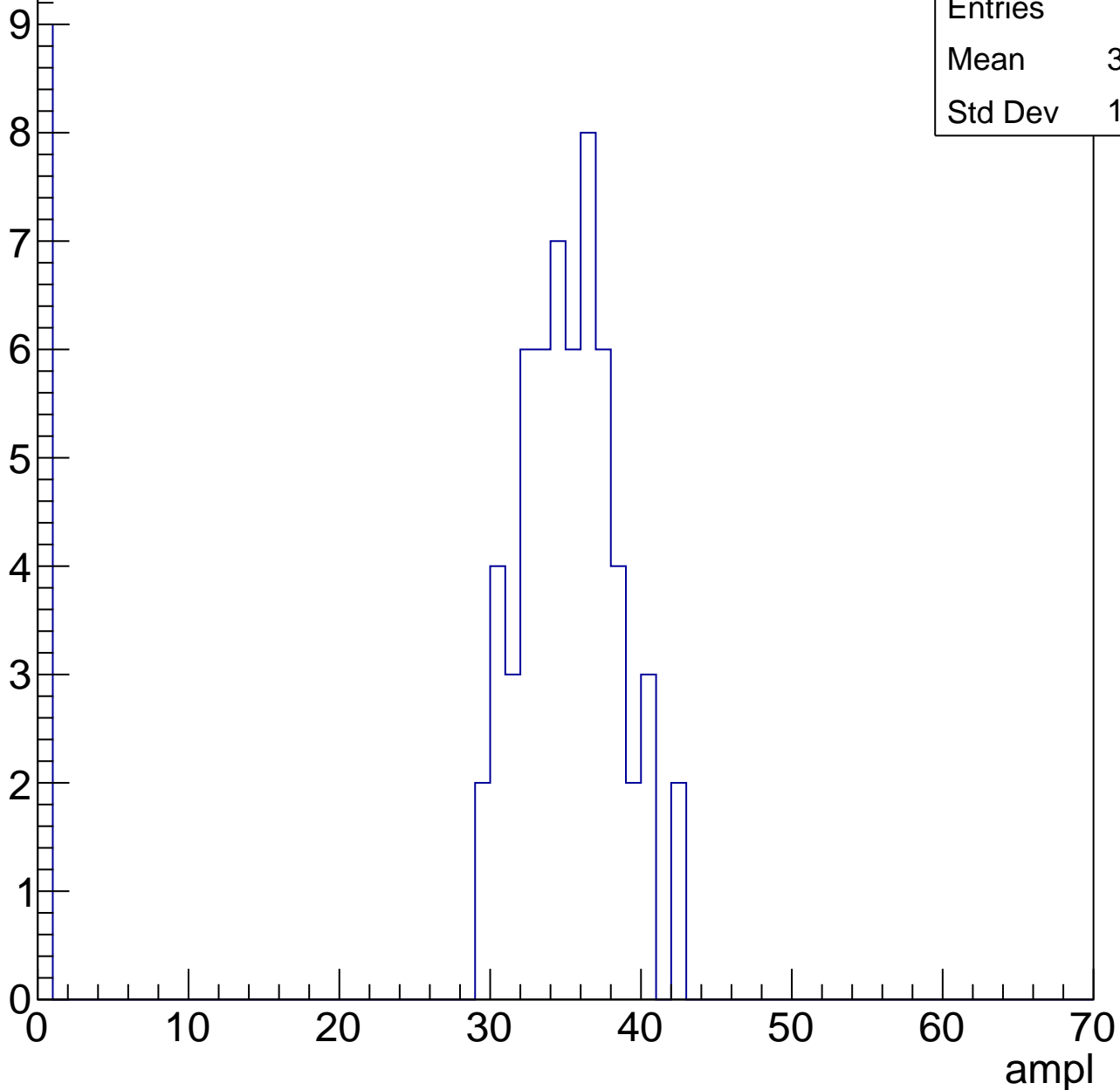


B1L103S, U11-ch104, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	30.19
Std Dev	12.15

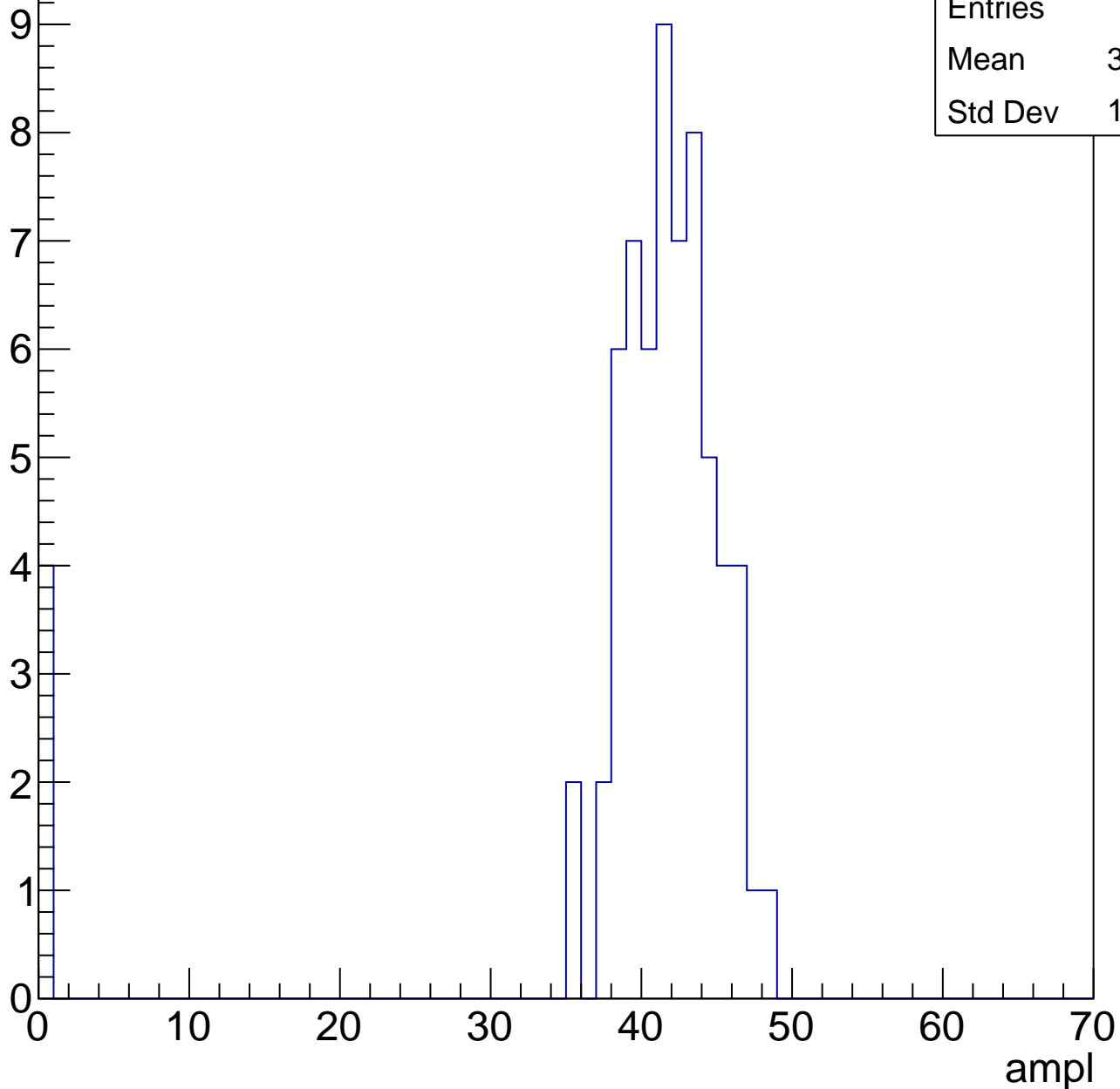


B1L103S, U11-ch104, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	38.95
Std Dev	10.28



B1L103S, U11-ch104, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	91
Mean	49.02
Std Dev	3.843

Entry

10

8

6

4

2

0

0

10

20

30

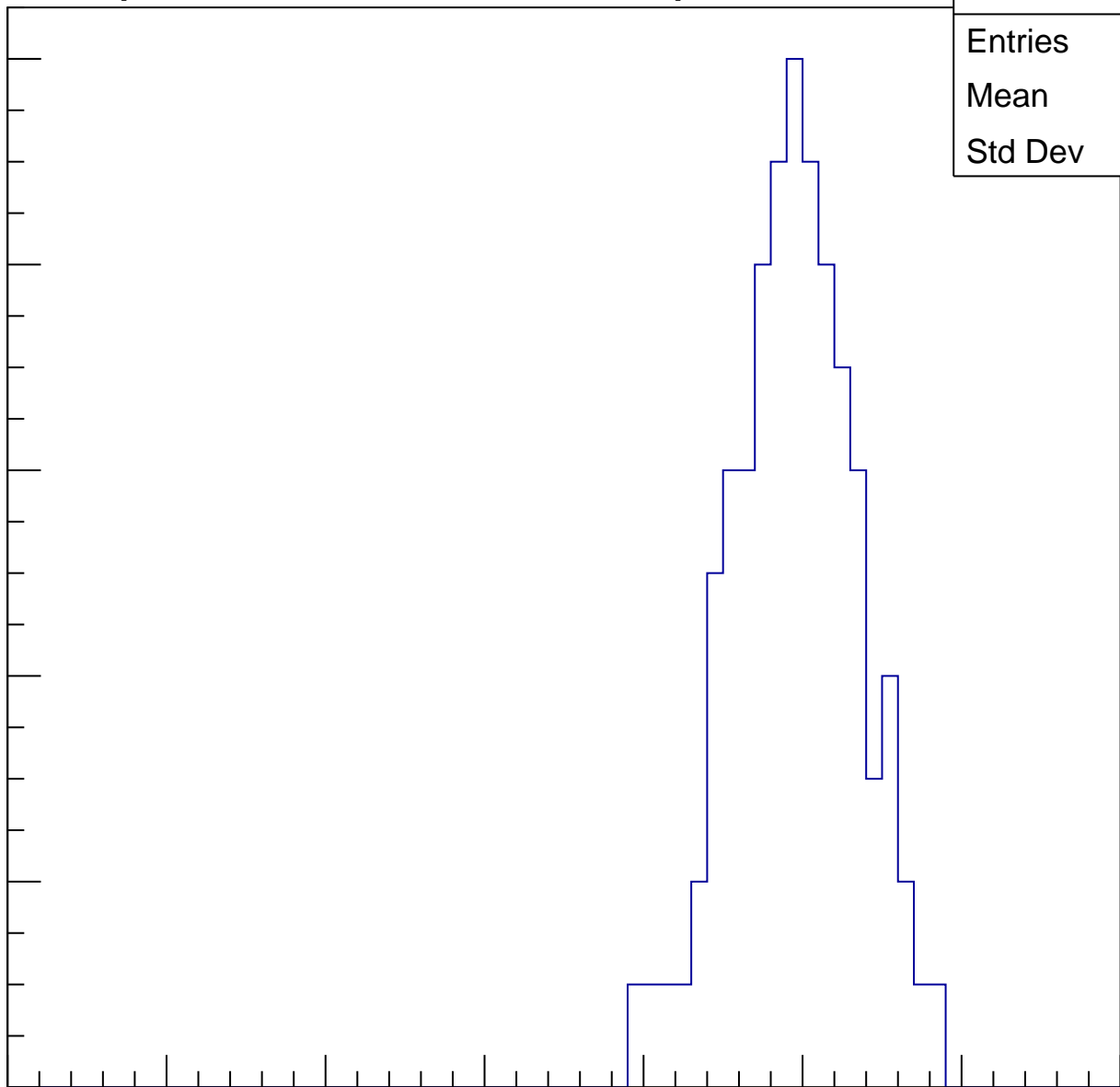
40

50

60

70

ampl

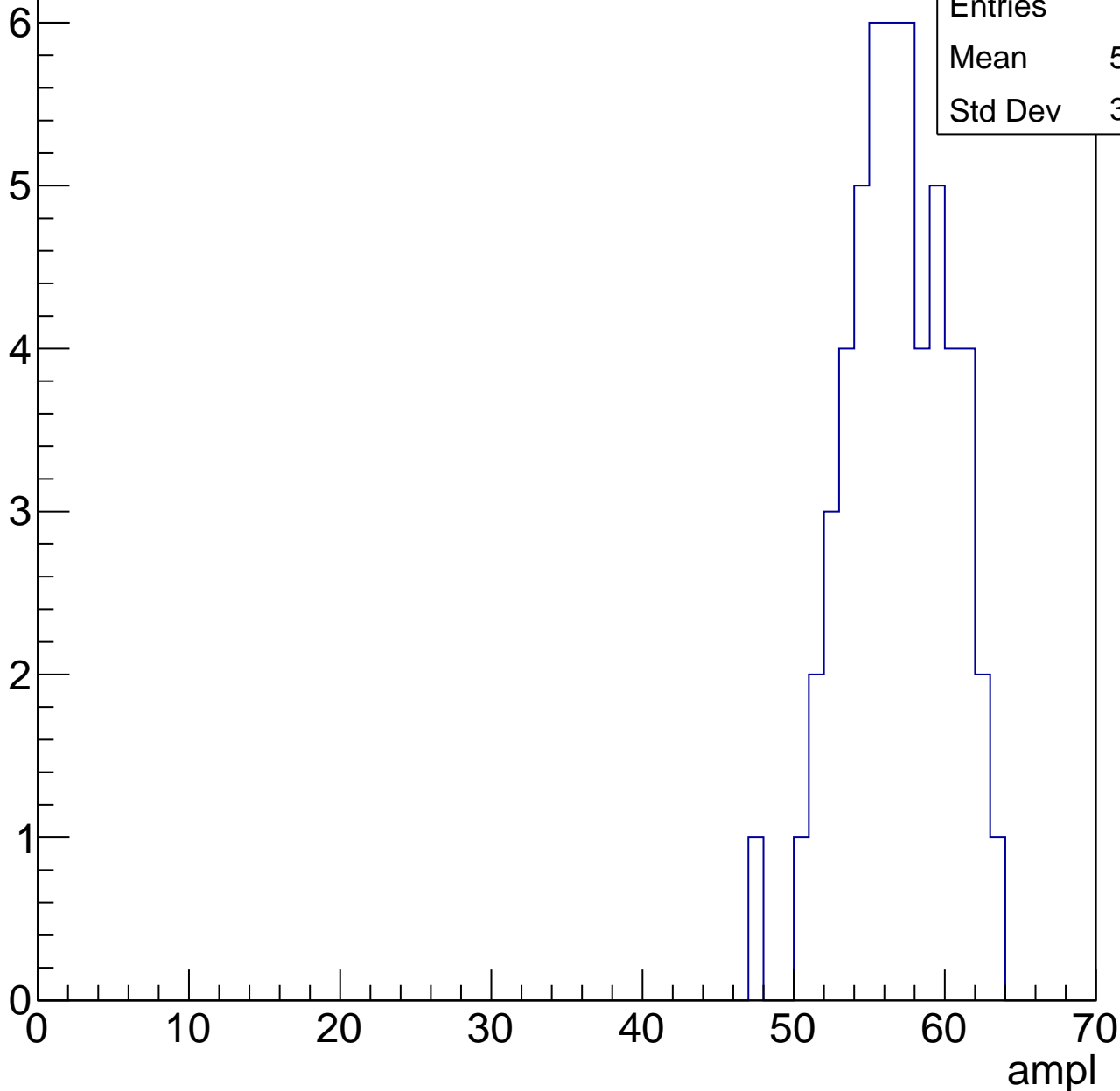


B1L103S, U11-ch104, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	56.35
Std Dev	3.395

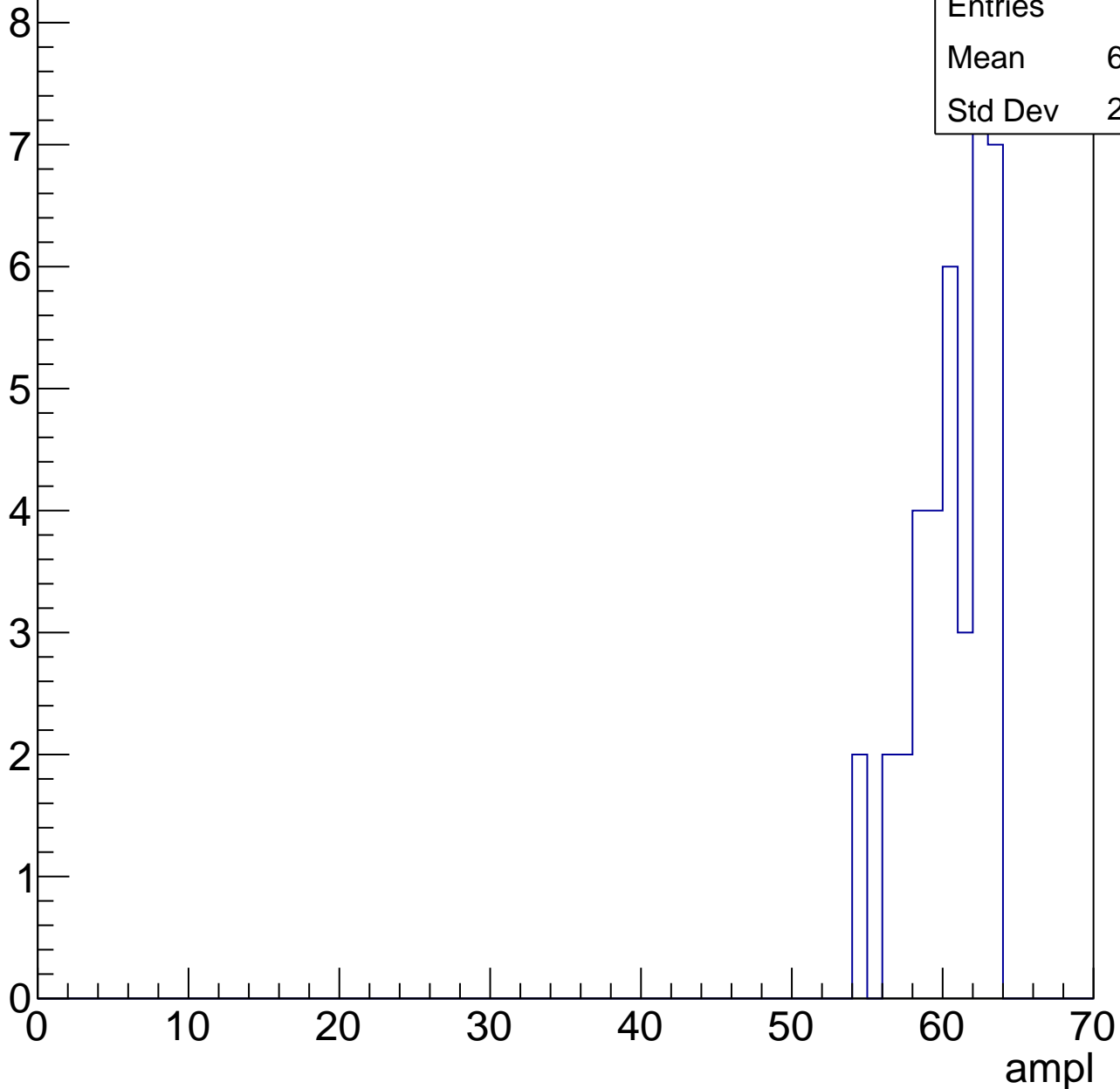


B1L103S, U11-ch104, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

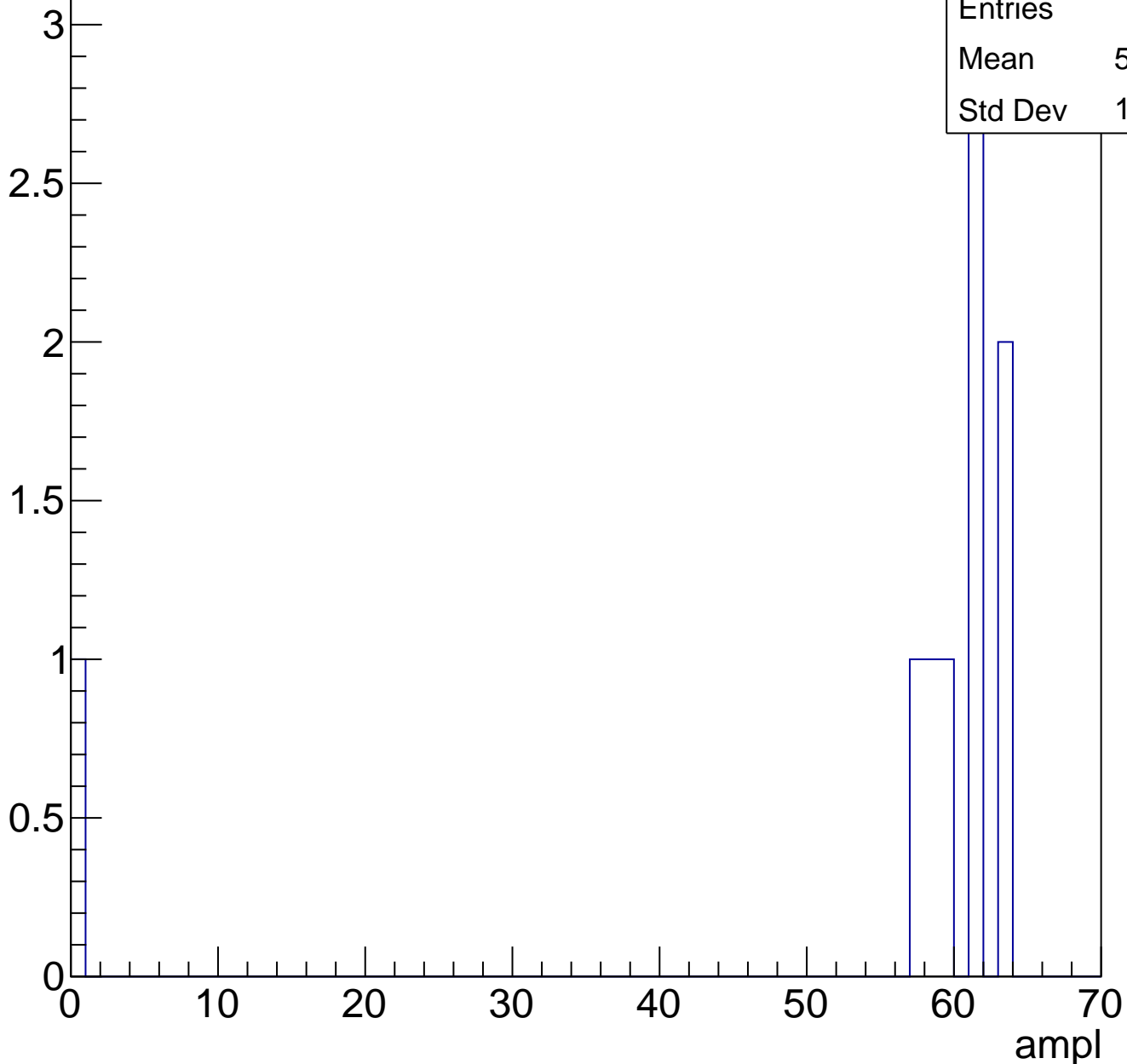
Entries	38
Mean	60.05
Std Dev	2.513



B1L103S, U11-ch104, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch104, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

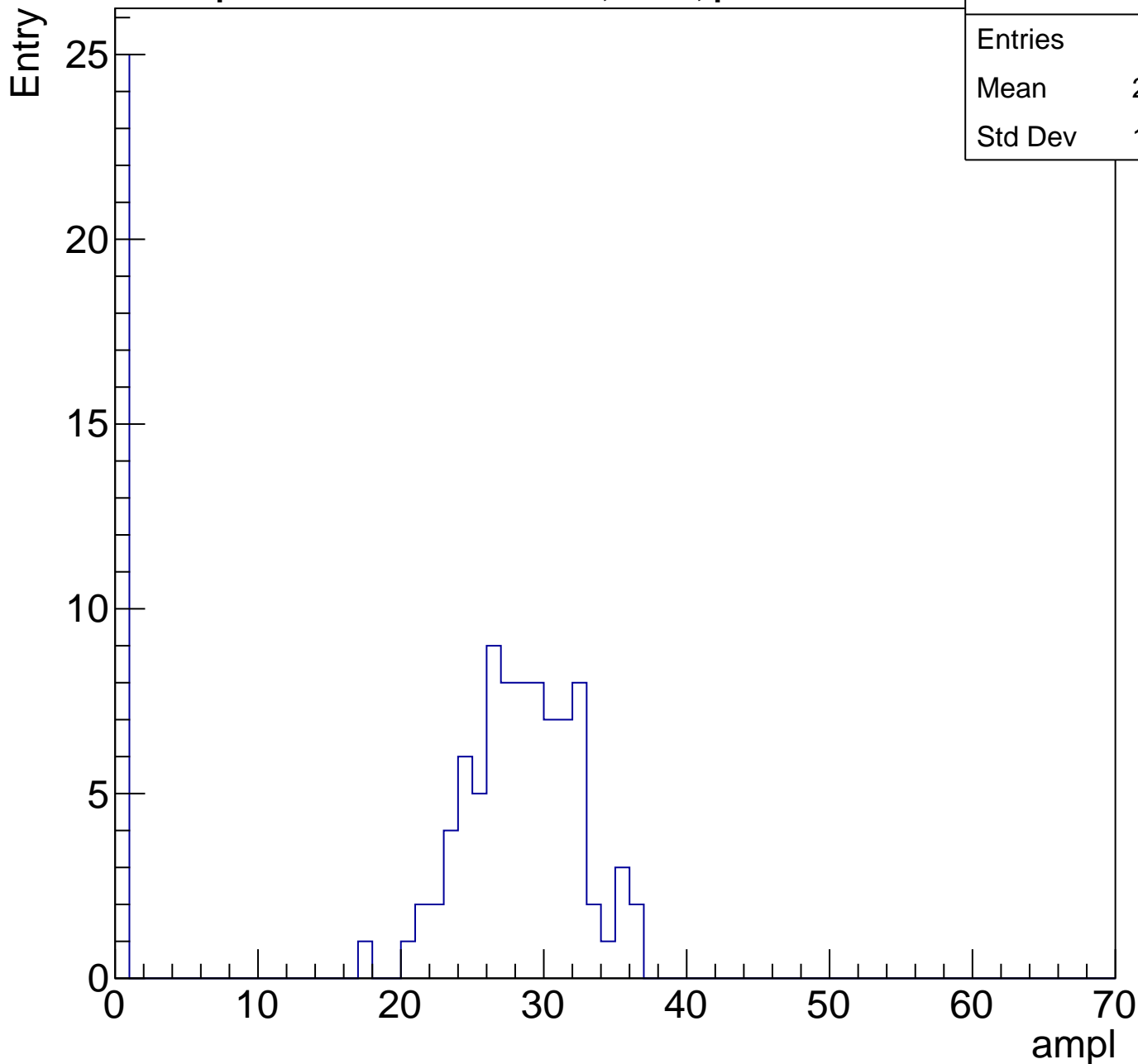


Entries	19
Mean	0
Std Dev	0

B1L103S, U11-ch105, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	109
Mean	21.56
Std Dev	12.23

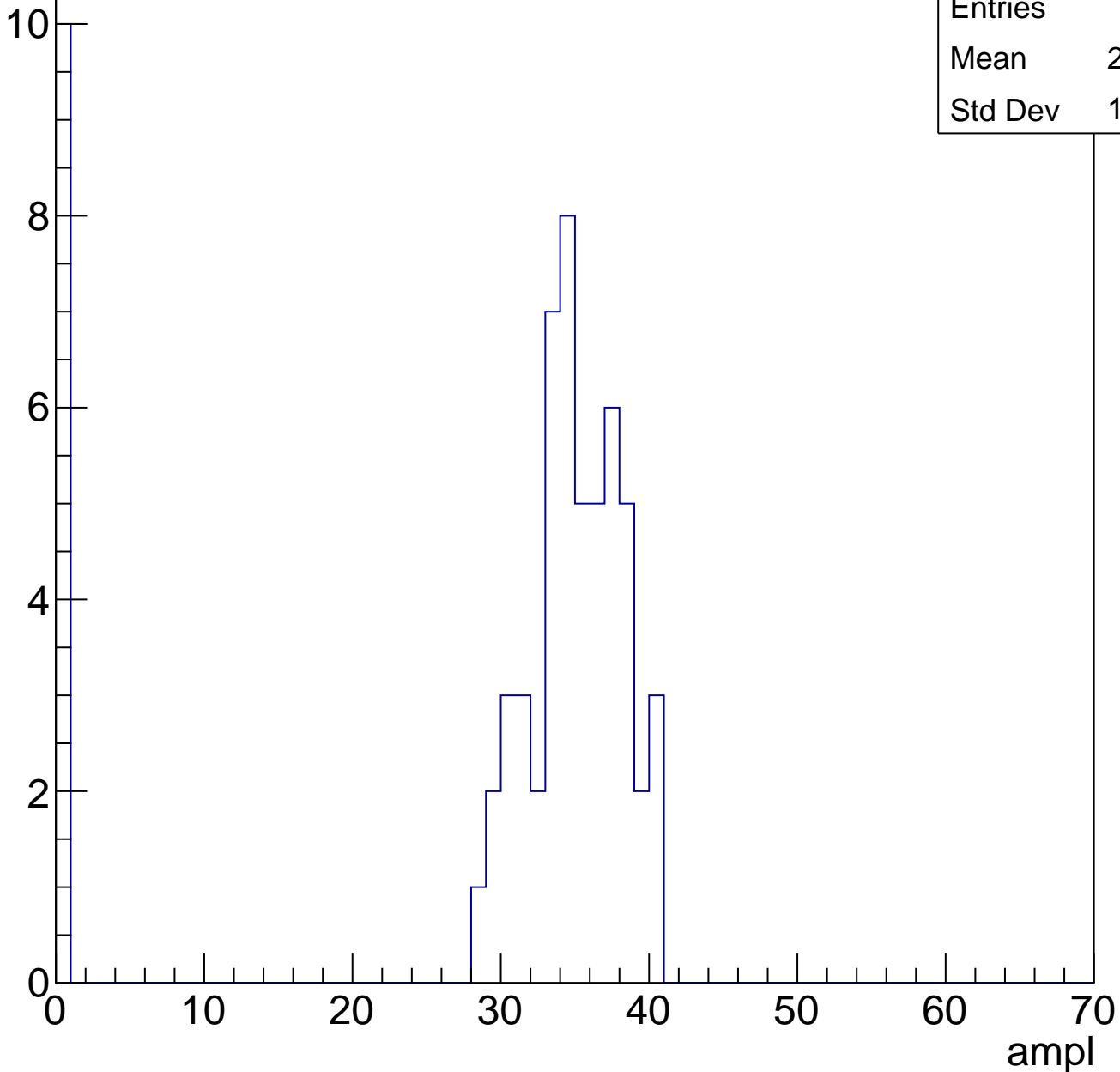


B1L103S, U11-ch105, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	62
Mean	29.05
Std Dev	13.03

Entry

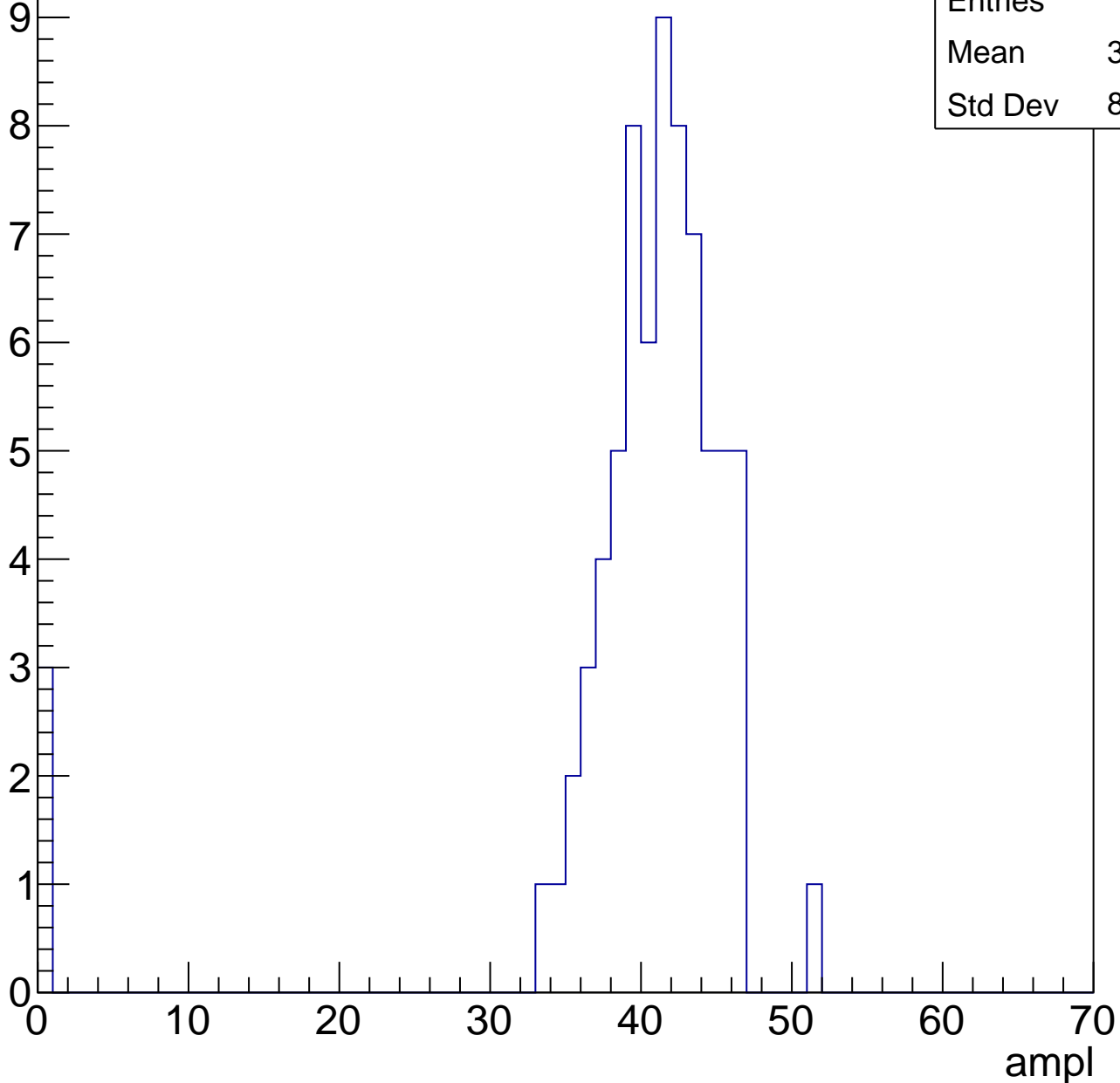


B1L103S, U11-ch105, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	39.27
Std Dev	8.773

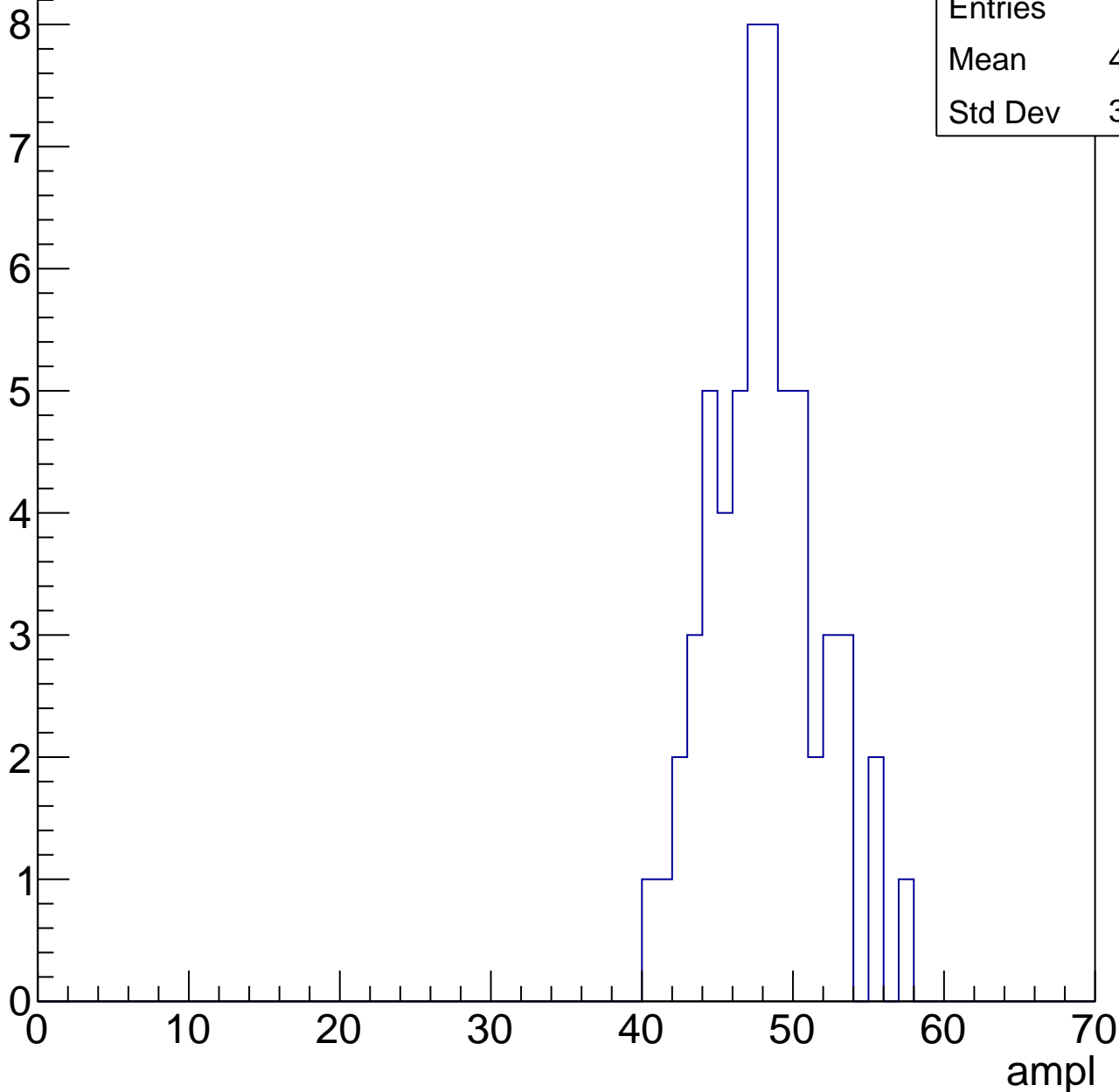


B1L103S, U11-ch105, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	47.64
Std Dev	3.575

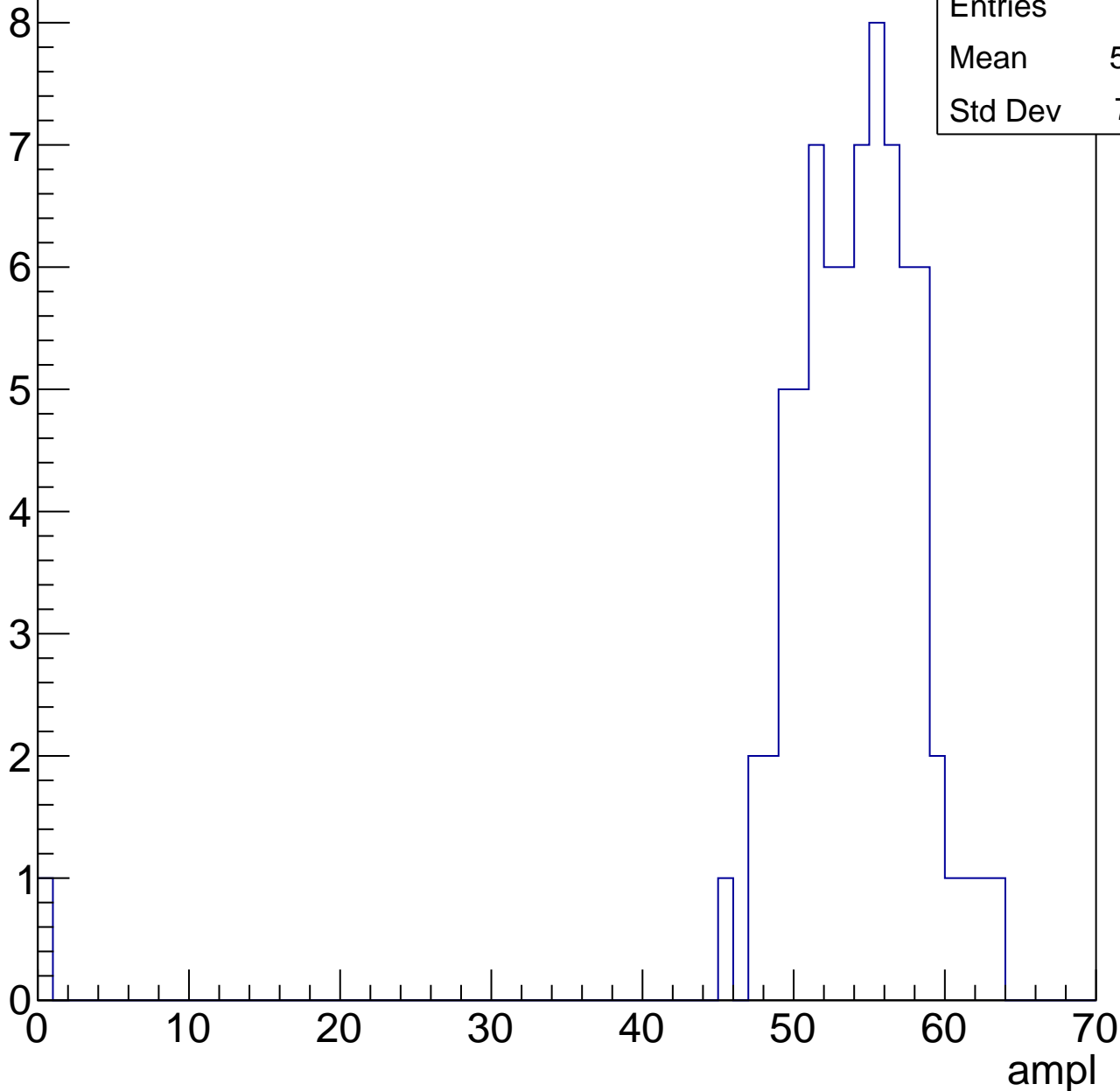


B1L103S, U11-ch105, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

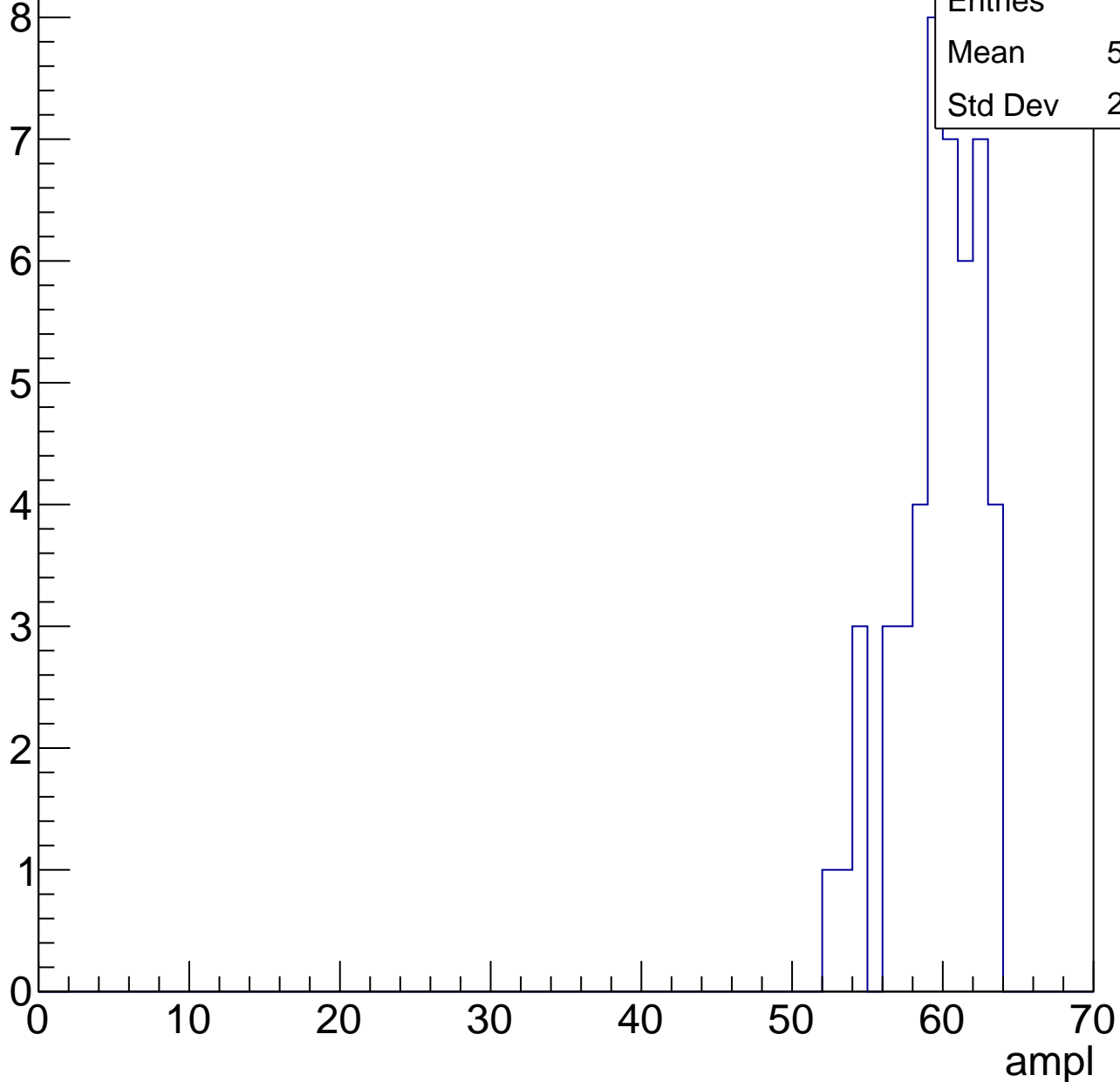
Entries	75
Mean	53.08
Std Dev	7.181



B1L103S, U11-ch105, adc5

calib_packv5_041523_1651.root, FC#0, port C2

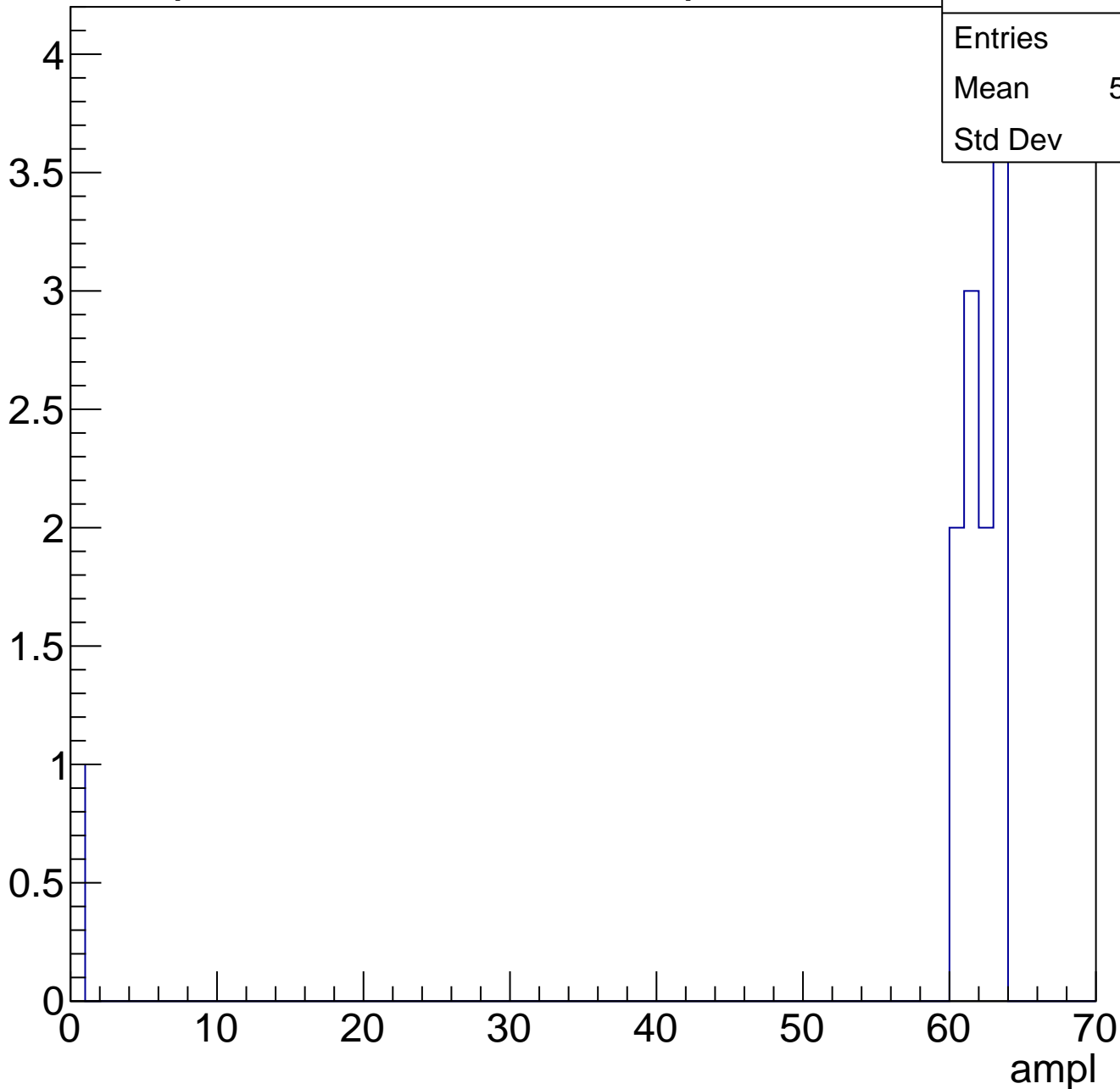
Entry



B1L103S, U11-ch105, adc6

calib_packv5_041523_1651.root, FC#0, port C2

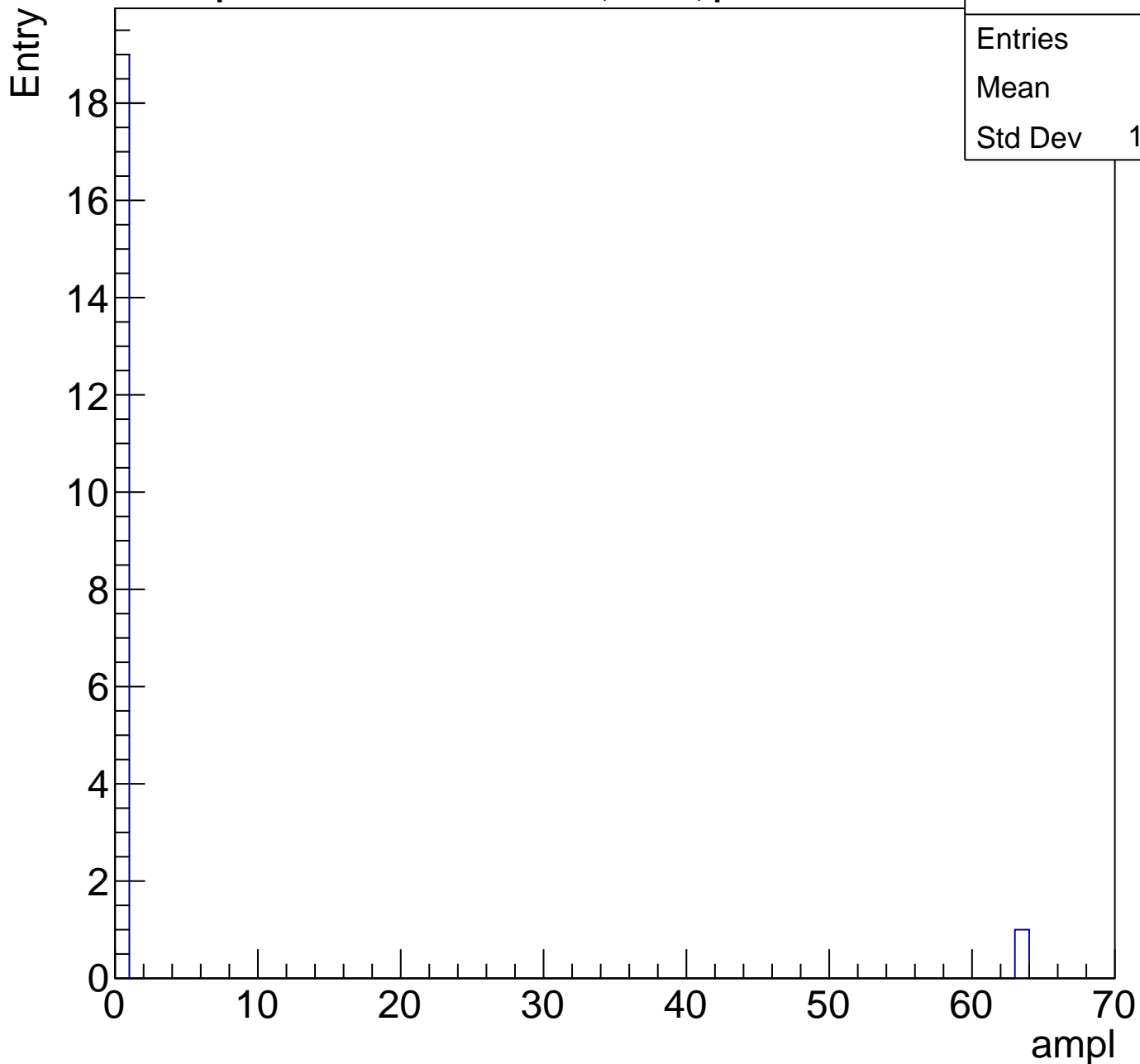
Entry



B1L103S, U11-ch105, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

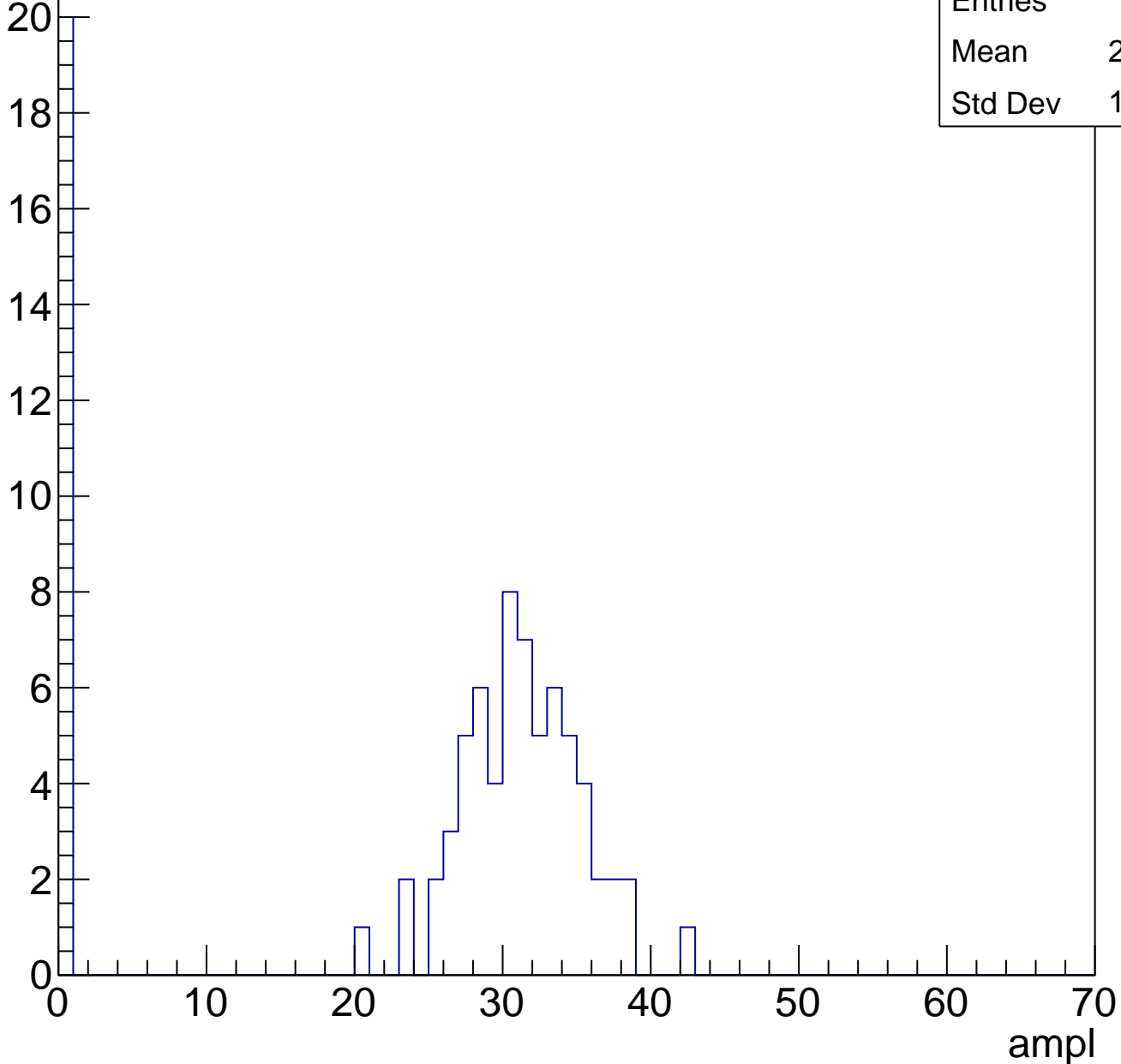


B1L103S, U11-ch106, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	85
Mean	23.55
Std Dev	13.52

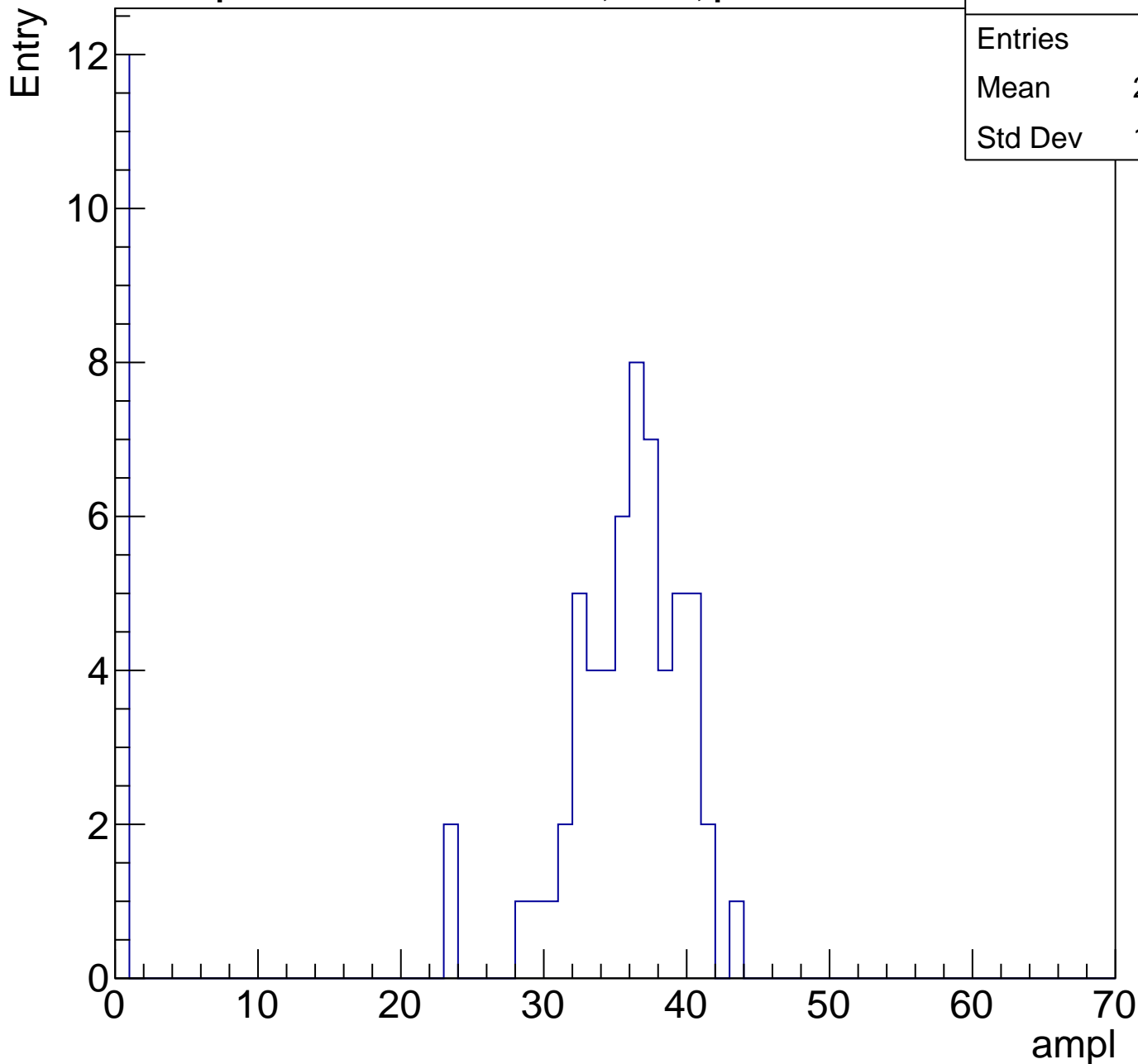
Entry



B1L103S, U11-ch106, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	70
Mean	29.31
Std Dev	13.81

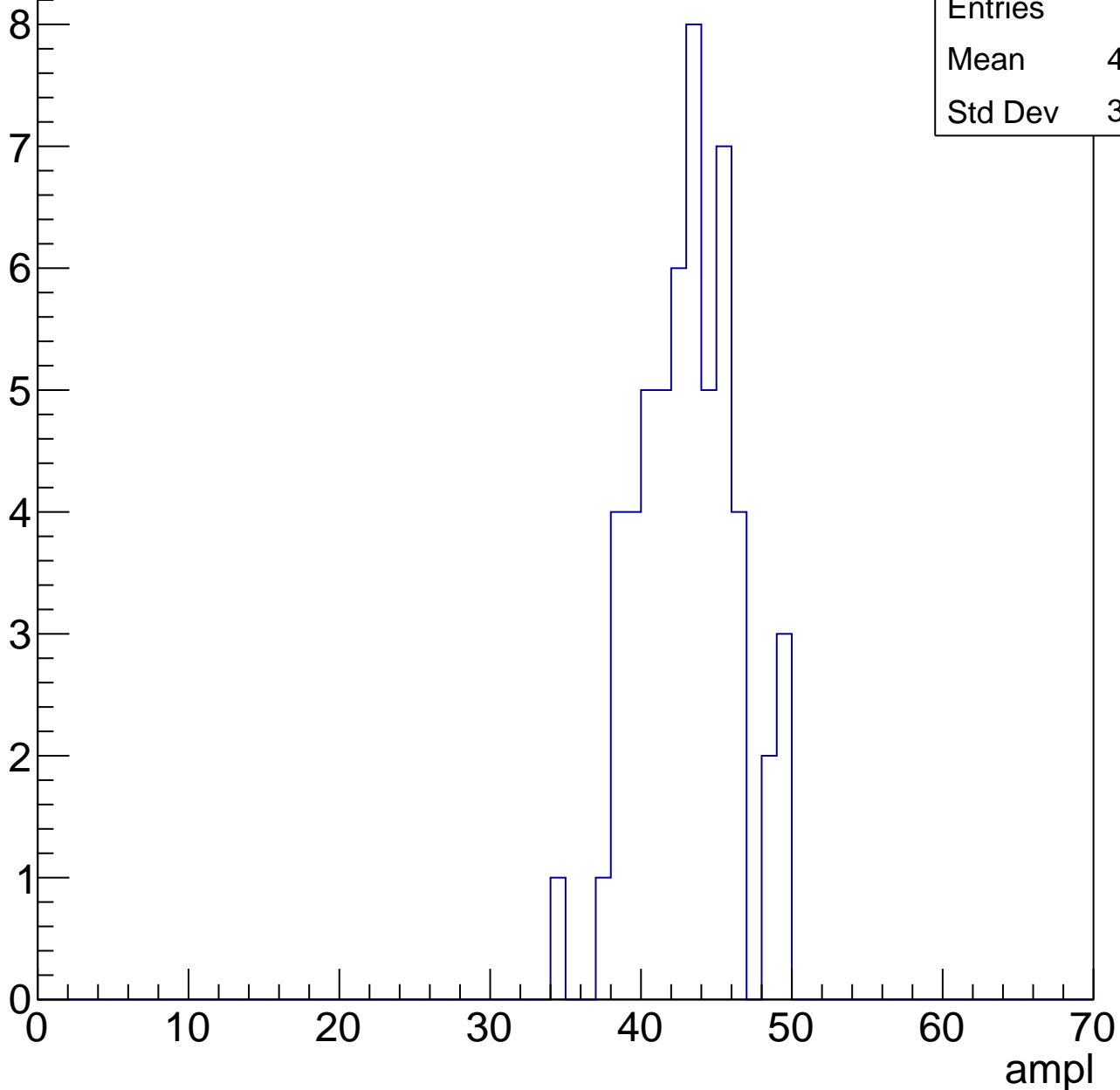


B1L103S, U11-ch106, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	42.58
Std Dev	3.218

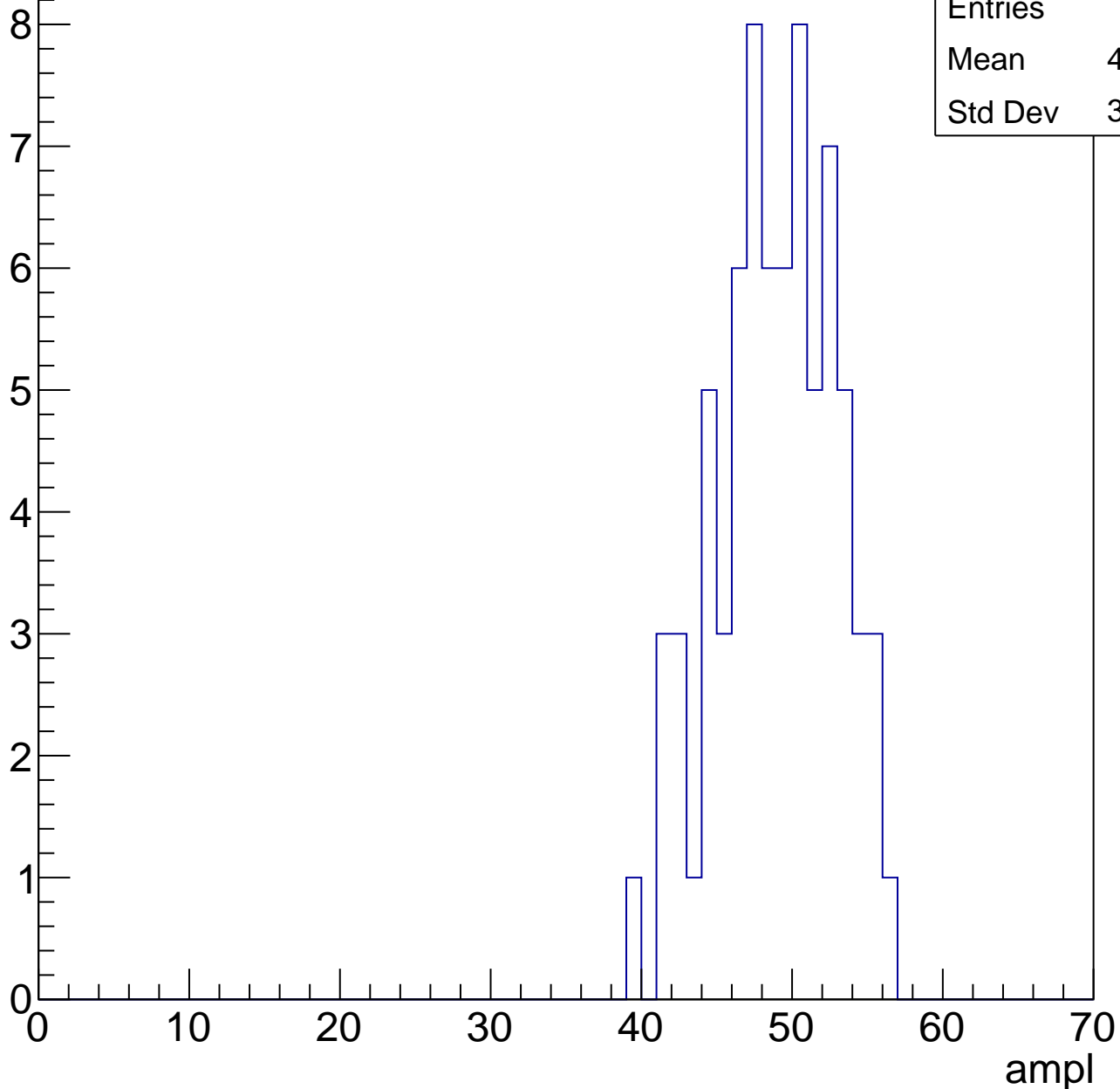


B1L103S, U11-ch106, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	48.47
Std Dev	3.895

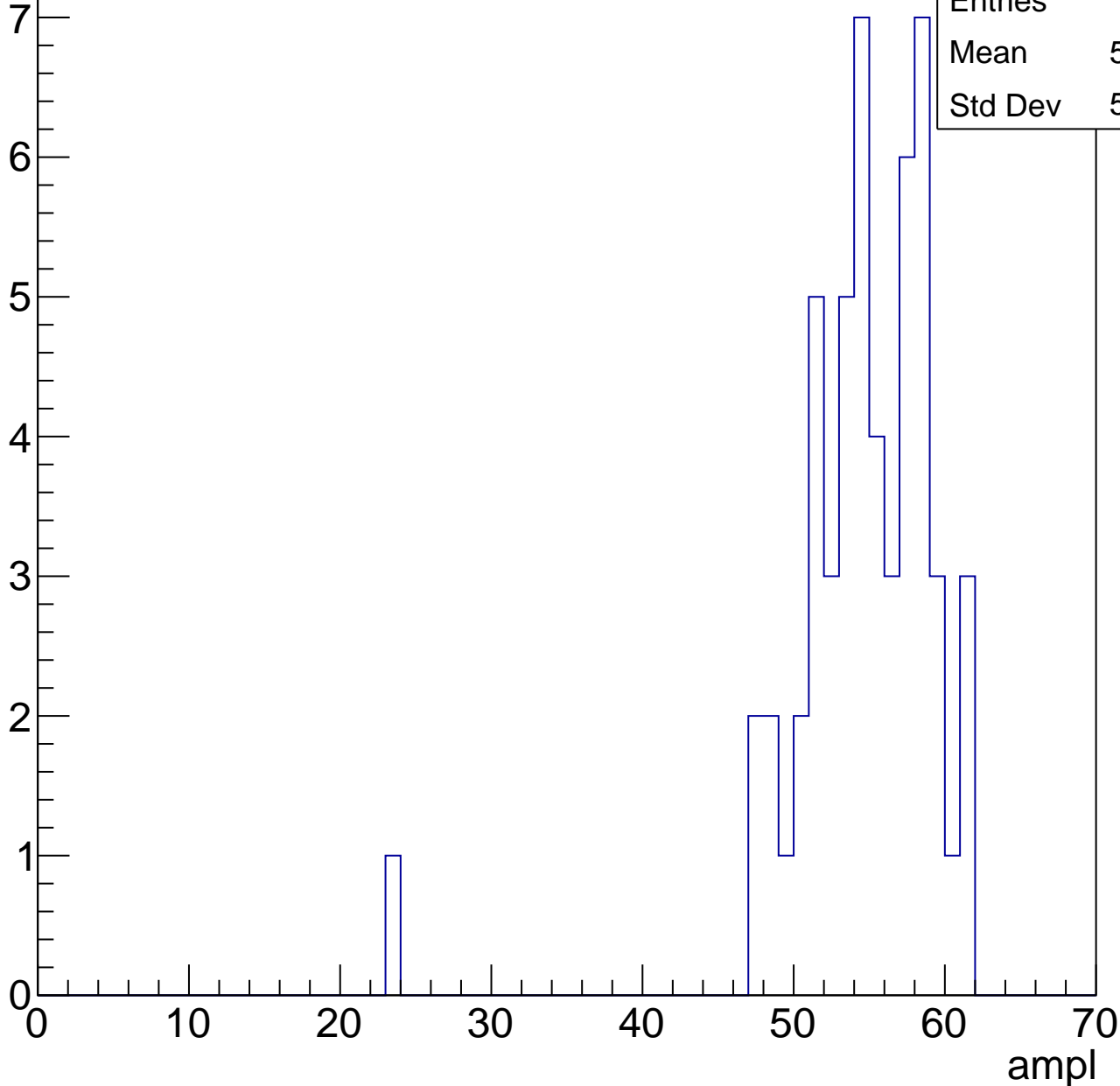


B1L103S, U11-ch106, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	54.04
Std Dev	5.543

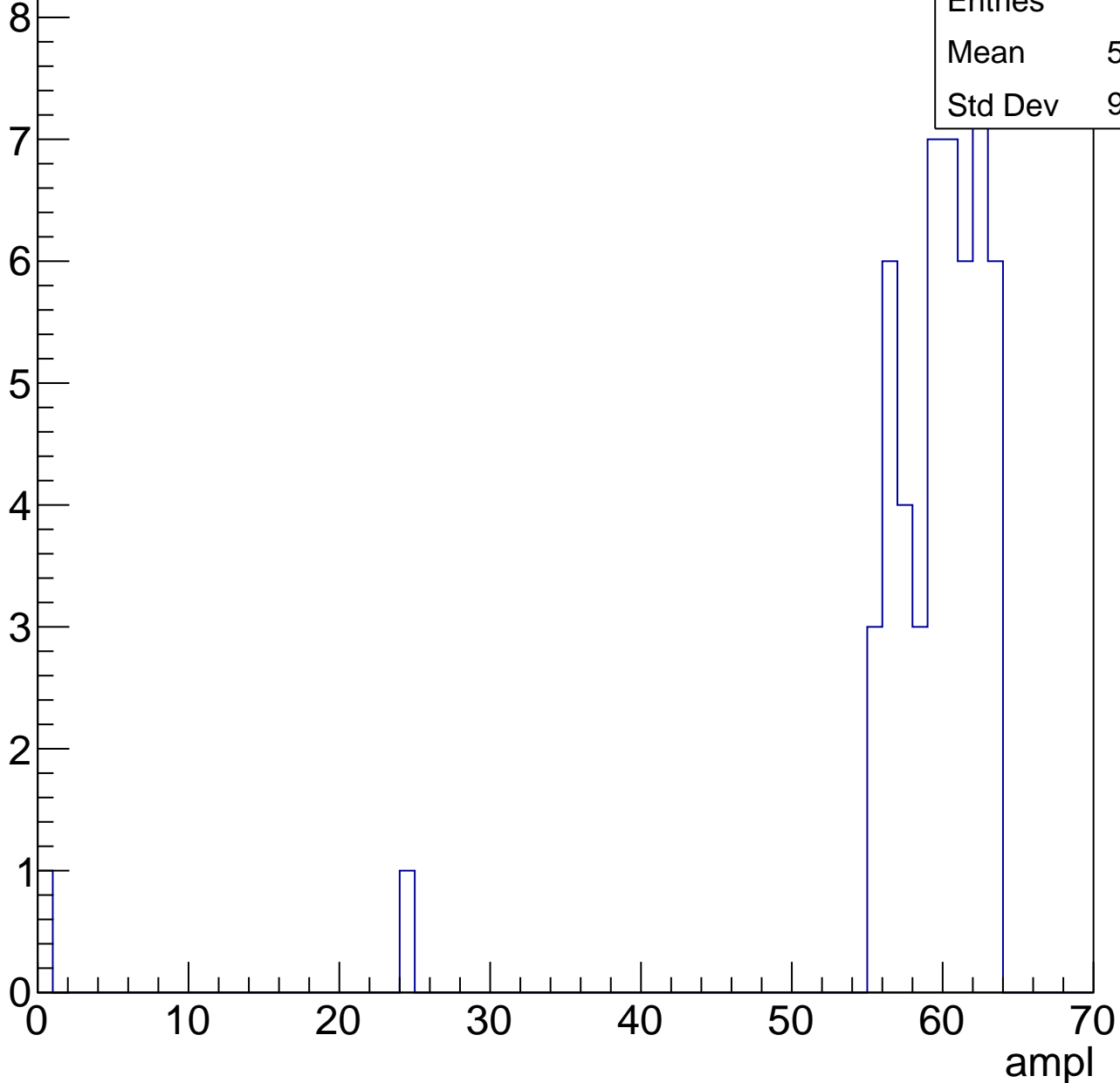


B1L103S, U11-ch106, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	57.69
Std Dev	9.744



B1L103S, U11-ch106, adc6

calib_packv5_041523_1651.root, FC#0, port C2

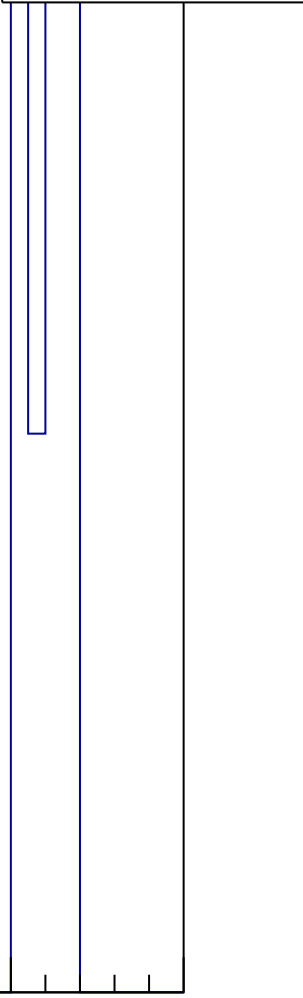
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	7
Mean	61.57
Std Dev	1.178

0 10 20 30 40 50 60 70

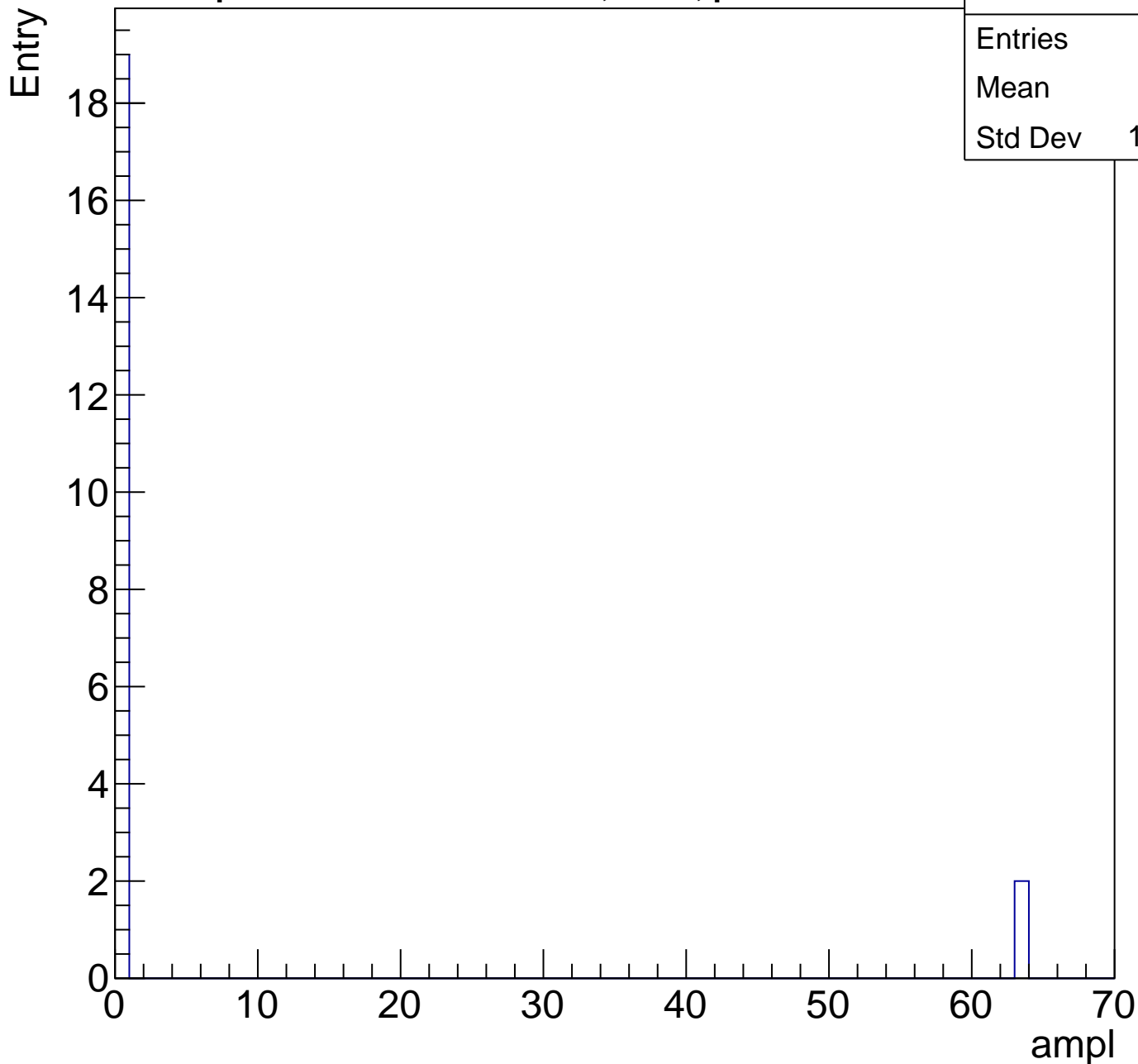
ampl



B1L103S, U11-ch106, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	6
Std Dev	18.49



B1L103S, U11-ch107, adc0

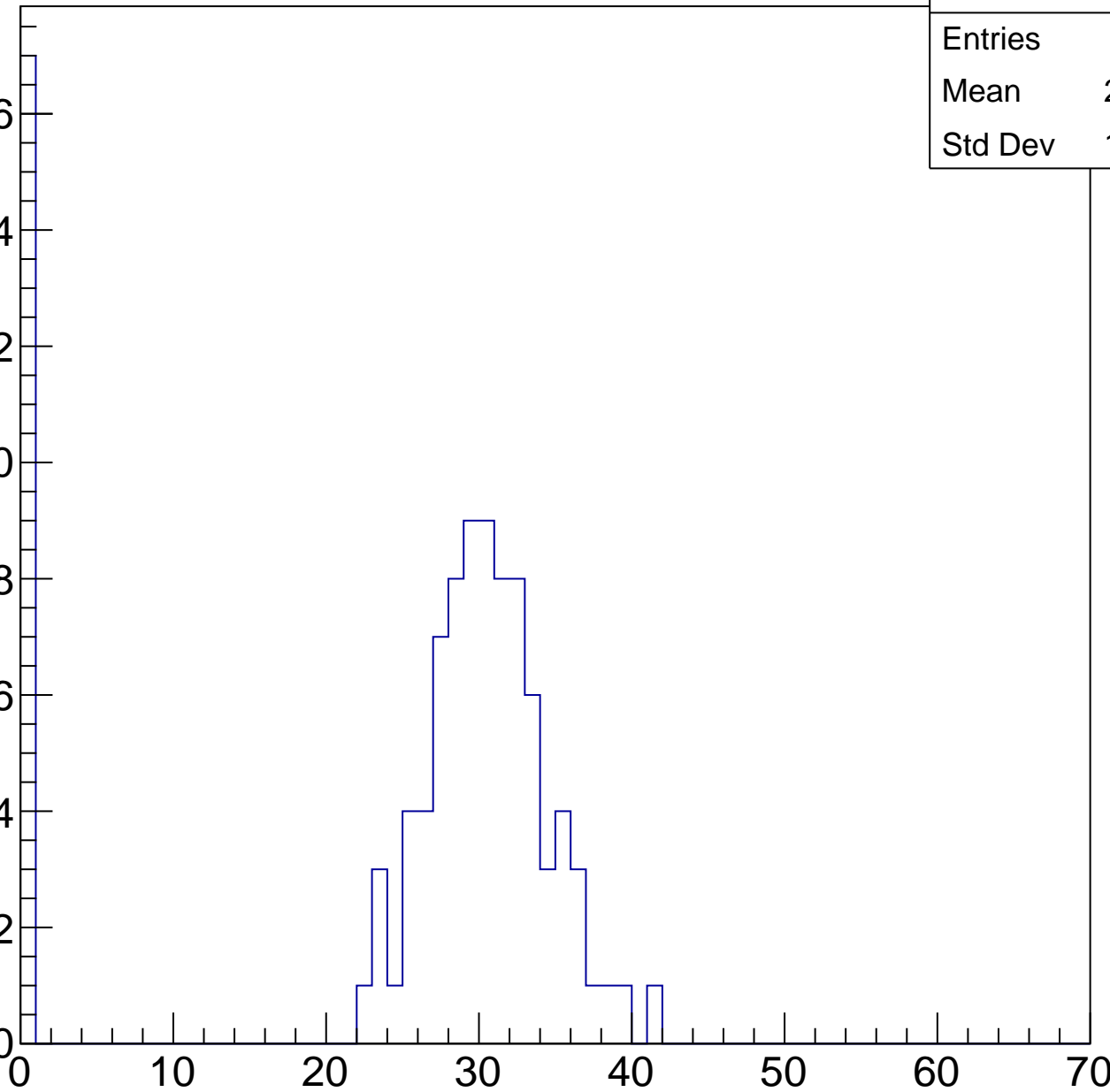
calib_packv5_041523_1651.root, FC#0, port C2

Entries	99
Mean	24.95
Std Dev	11.87

Entry

16
14
12
10
8
6
4
2
0

ampl



B1L103S, U11-ch107, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	79
Mean	31.9
Std Dev	13.19

Entry

10

8

6

4

2

0

0

10

20

30

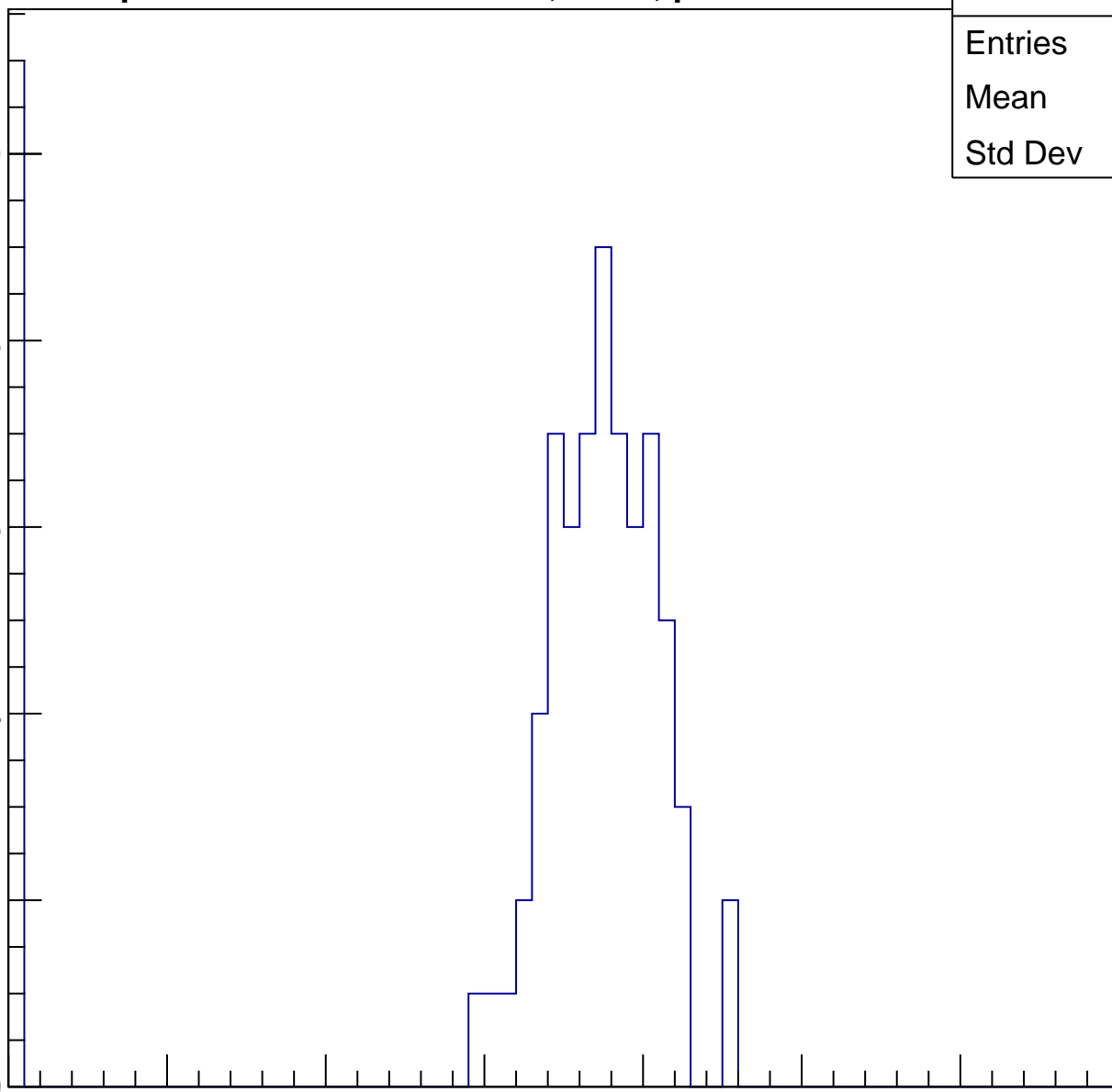
40

50

60

70

ampl

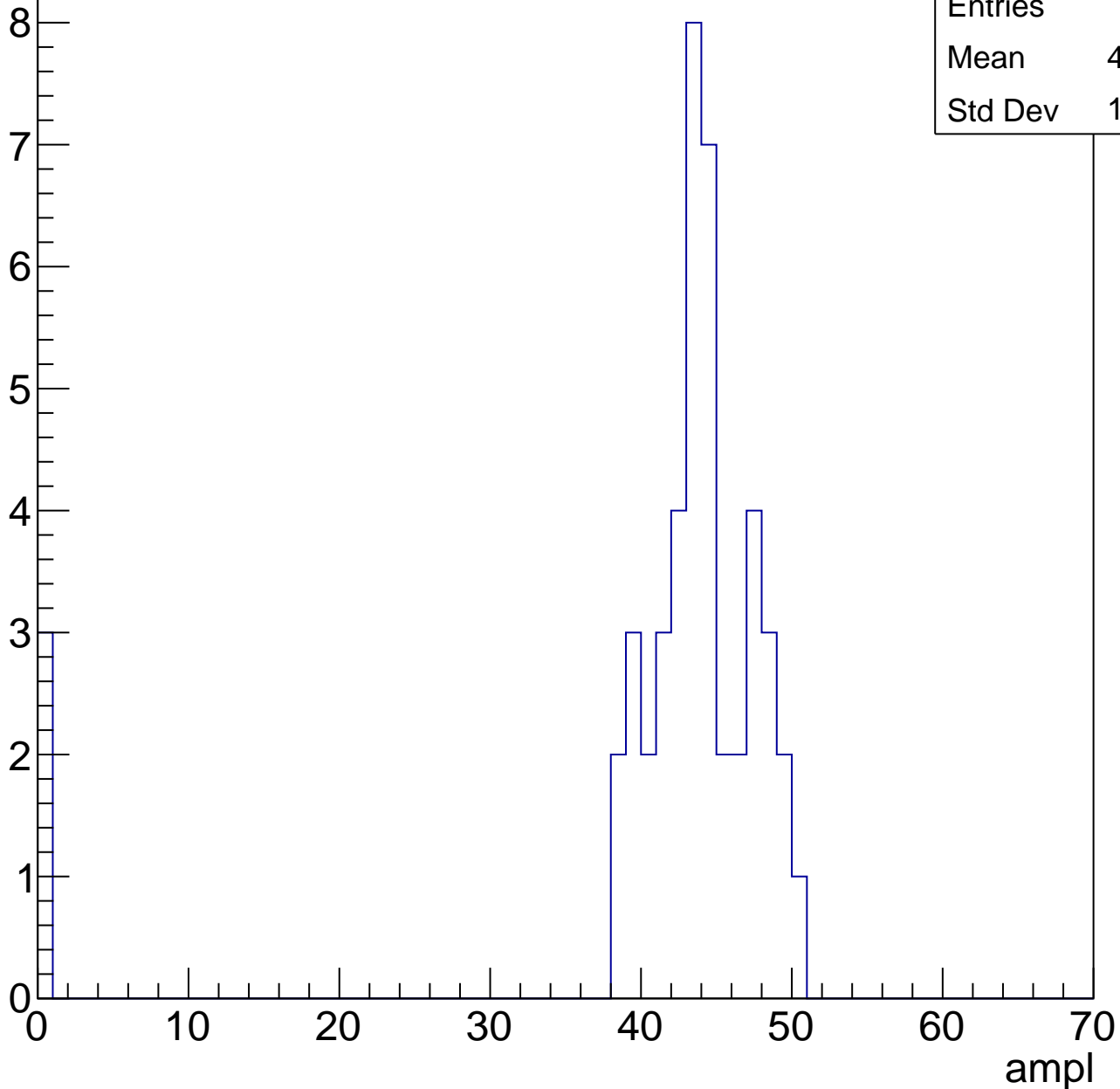


B1L103S, U11-ch107, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	46
Mean	40.83
Std Dev	11.18

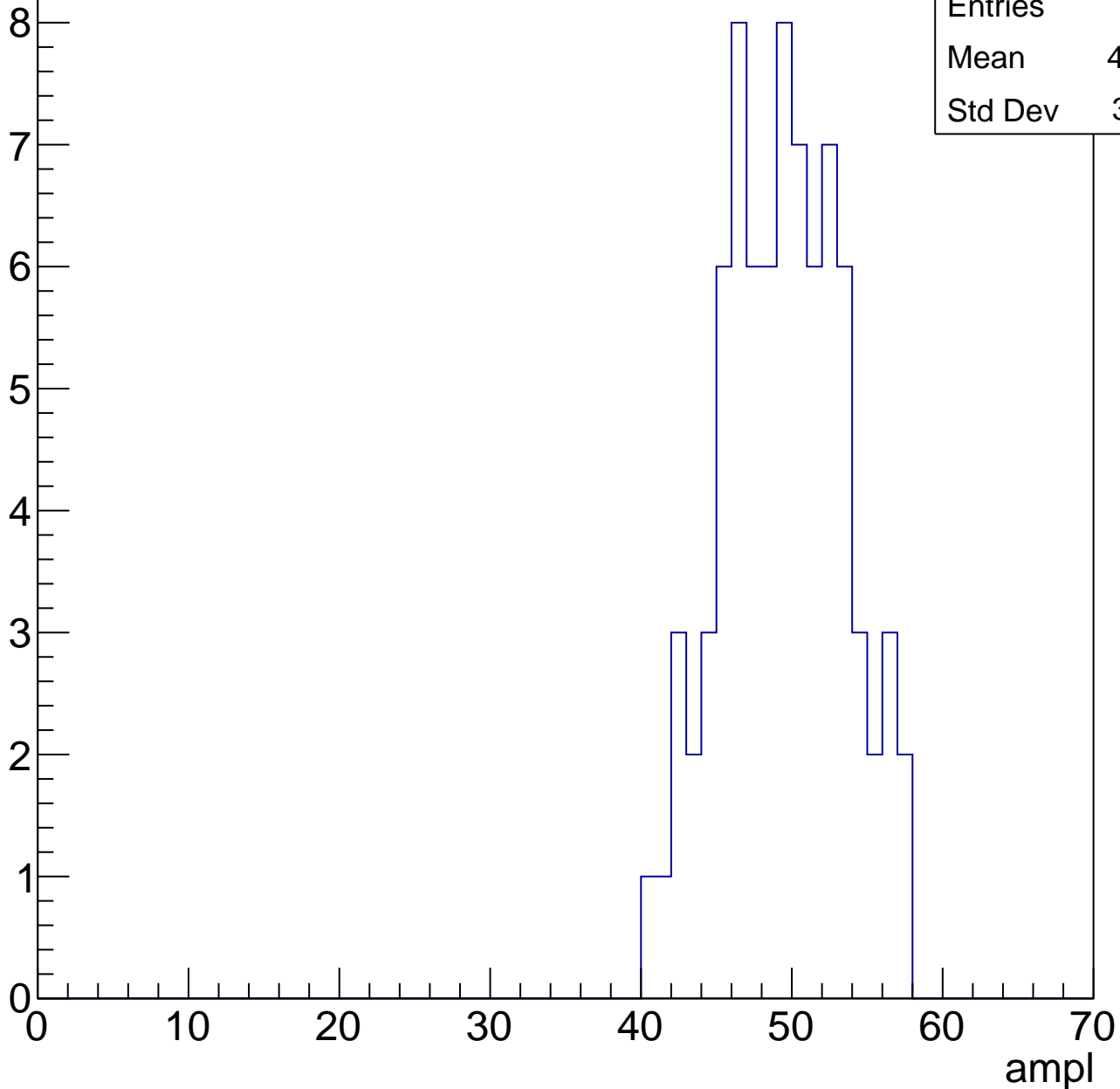


B1L103S, U11-ch107, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	80
Mean	48.96
Std Dev	3.951

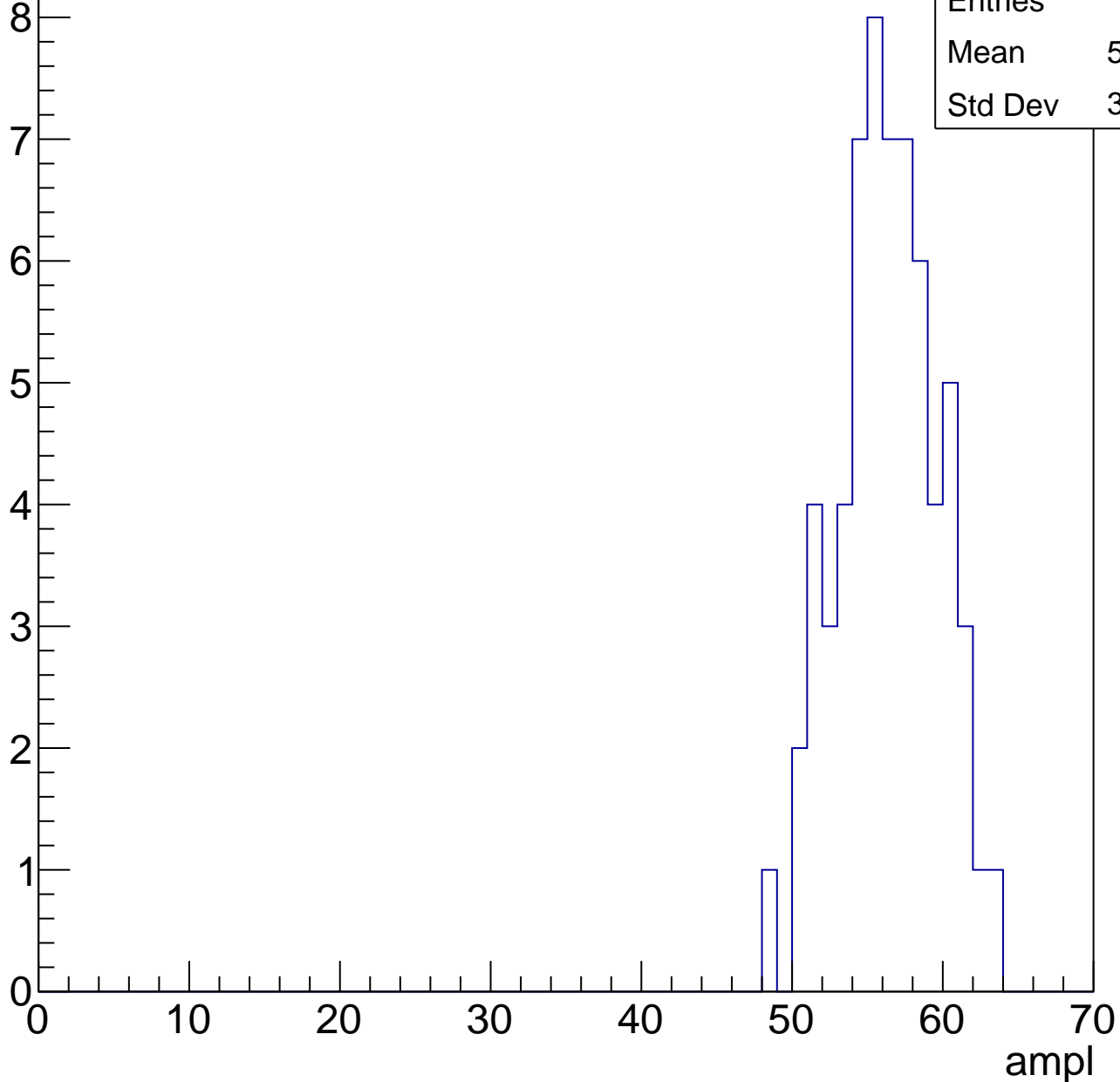


B1L103S, U11-ch107, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	55.89
Std Dev	3.242

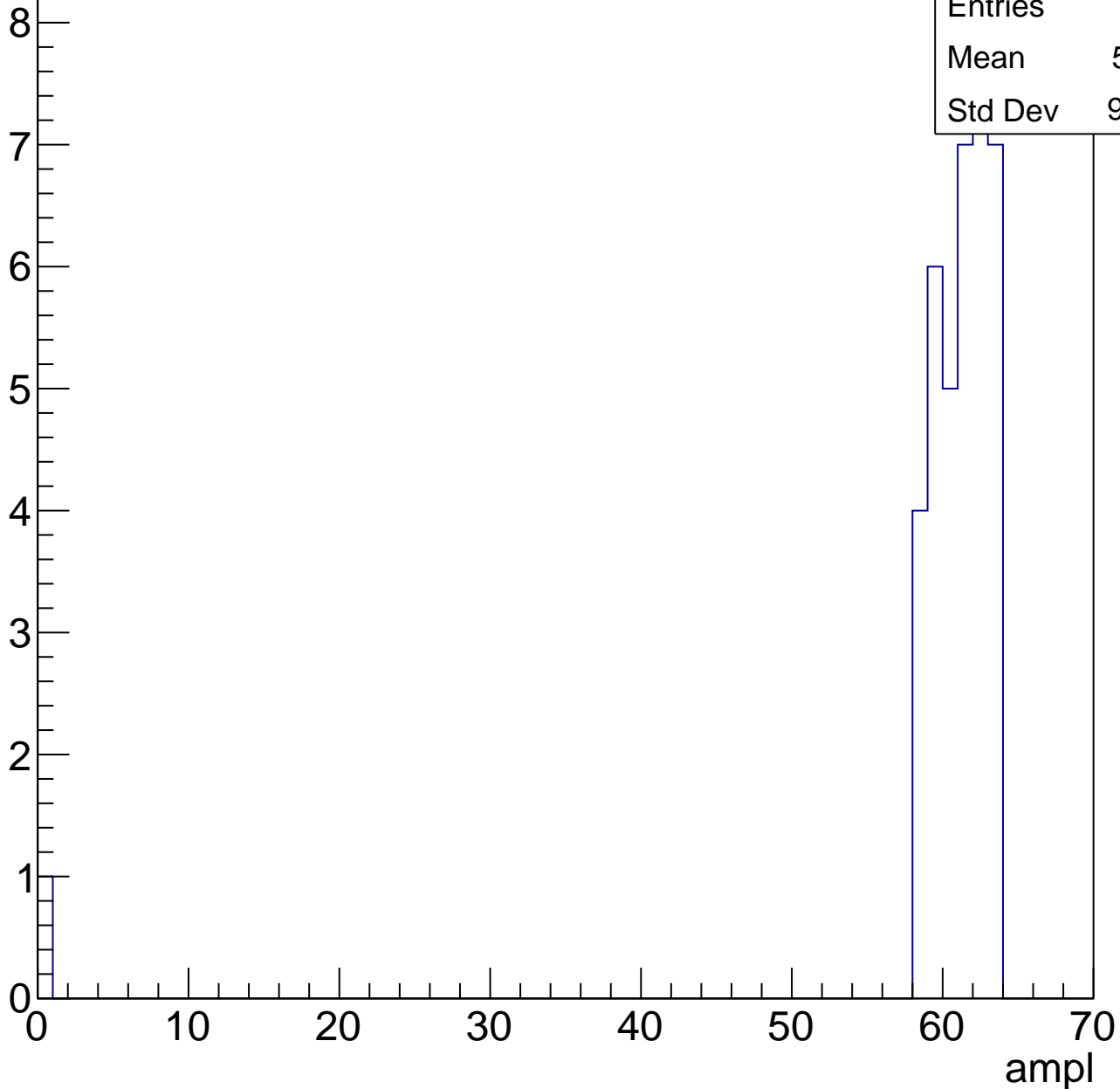


B1L103S, U11-ch107, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	38
Mean	59.21
Std Dev	9.868



B1L103S, U11-ch107, adc6

calib_packv5_041523_1651.root, FC#0, port C2

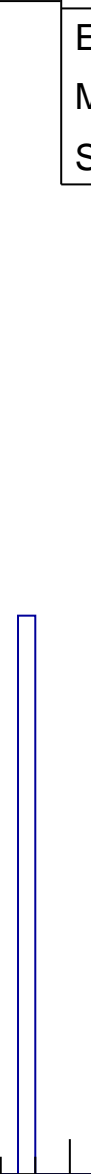
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	4
Mean	61.25
Std Dev	2.487

0 10 20 30 40 50 60 70

ampl



B1L103S, U11-ch107, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

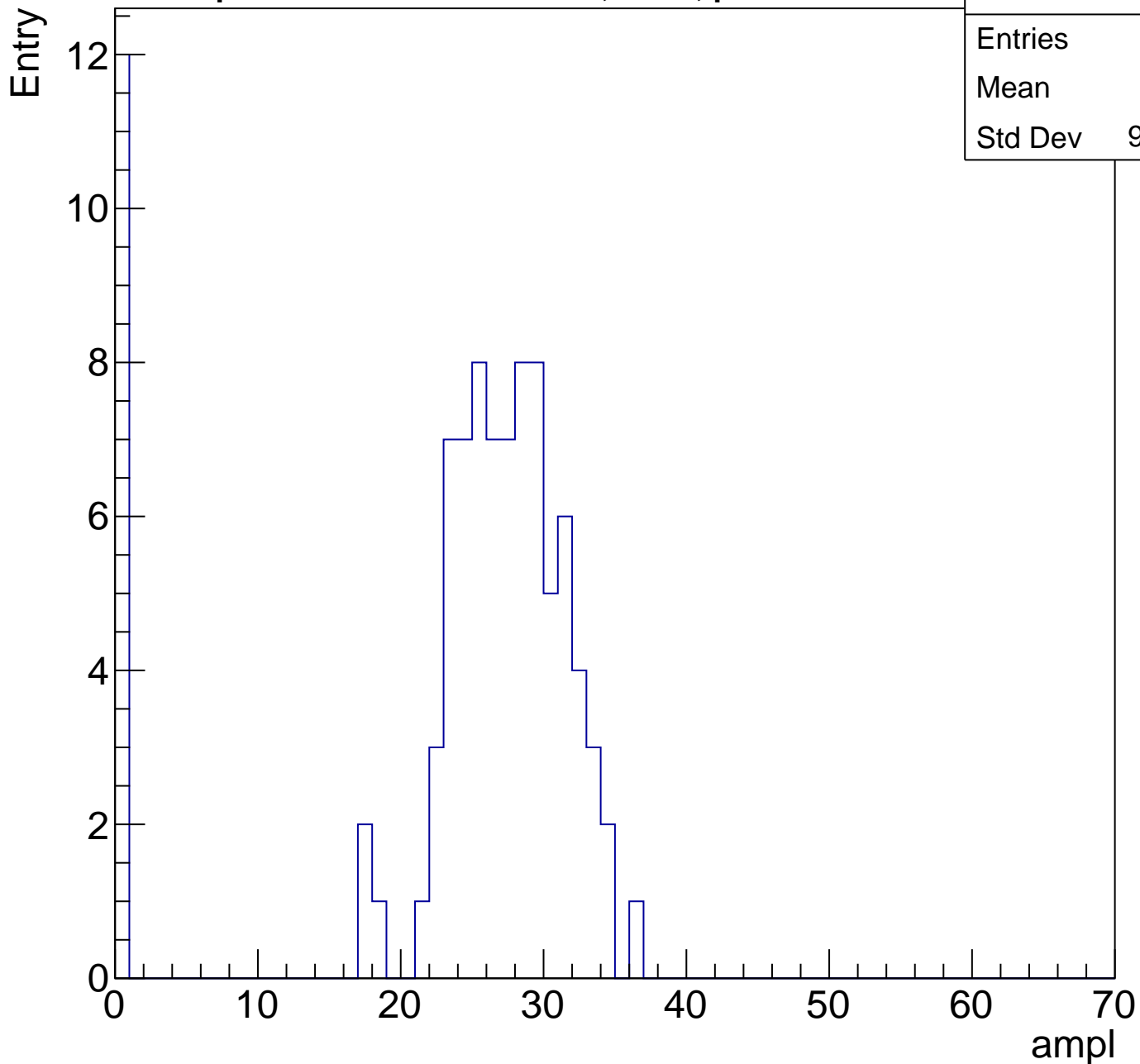
Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U11-ch108, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	92
Mean	23.5
Std Dev	9.777

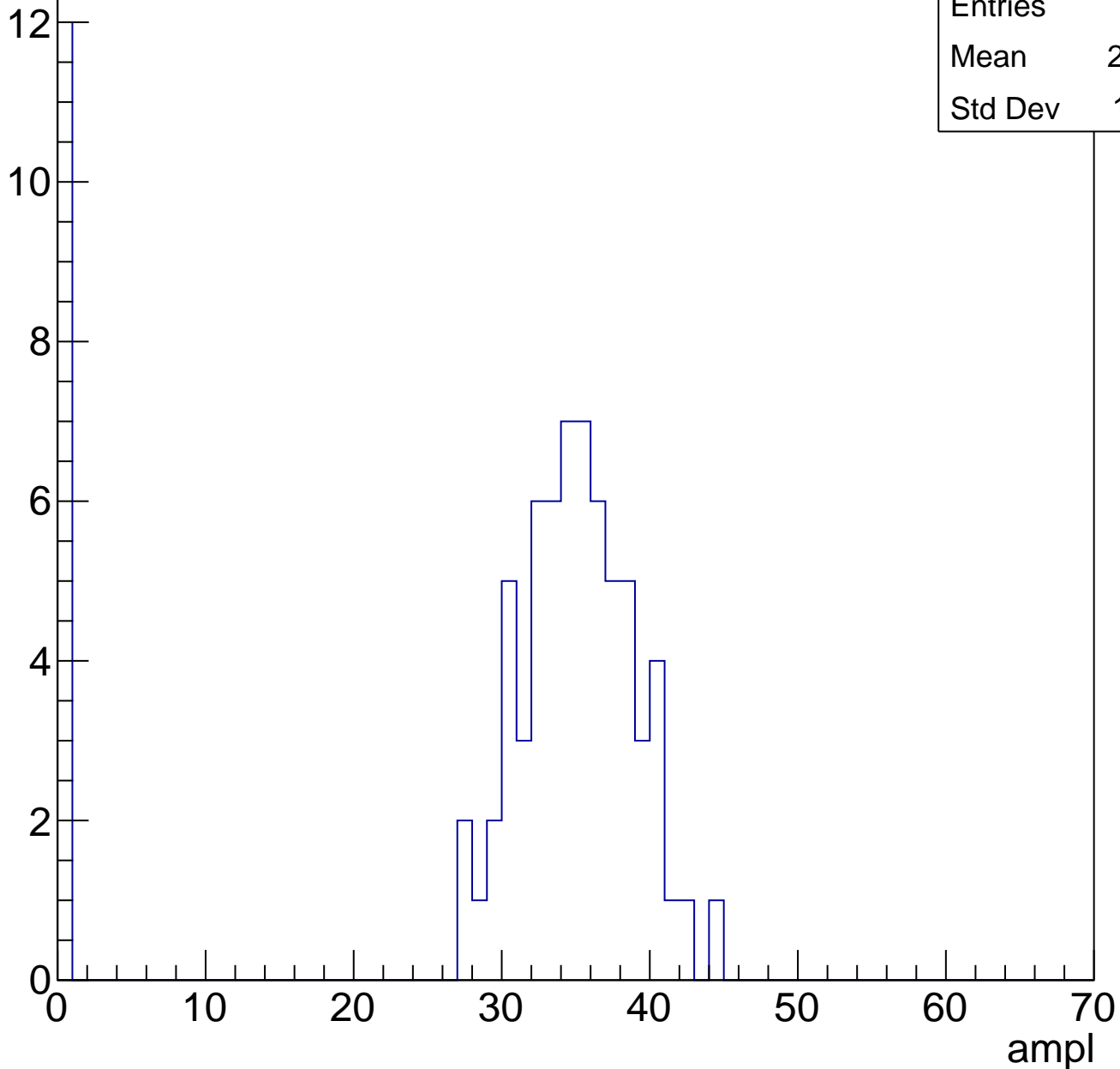


B1L103S, U11-ch108, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	77
Mean	29.23
Std Dev	13.01

Entry

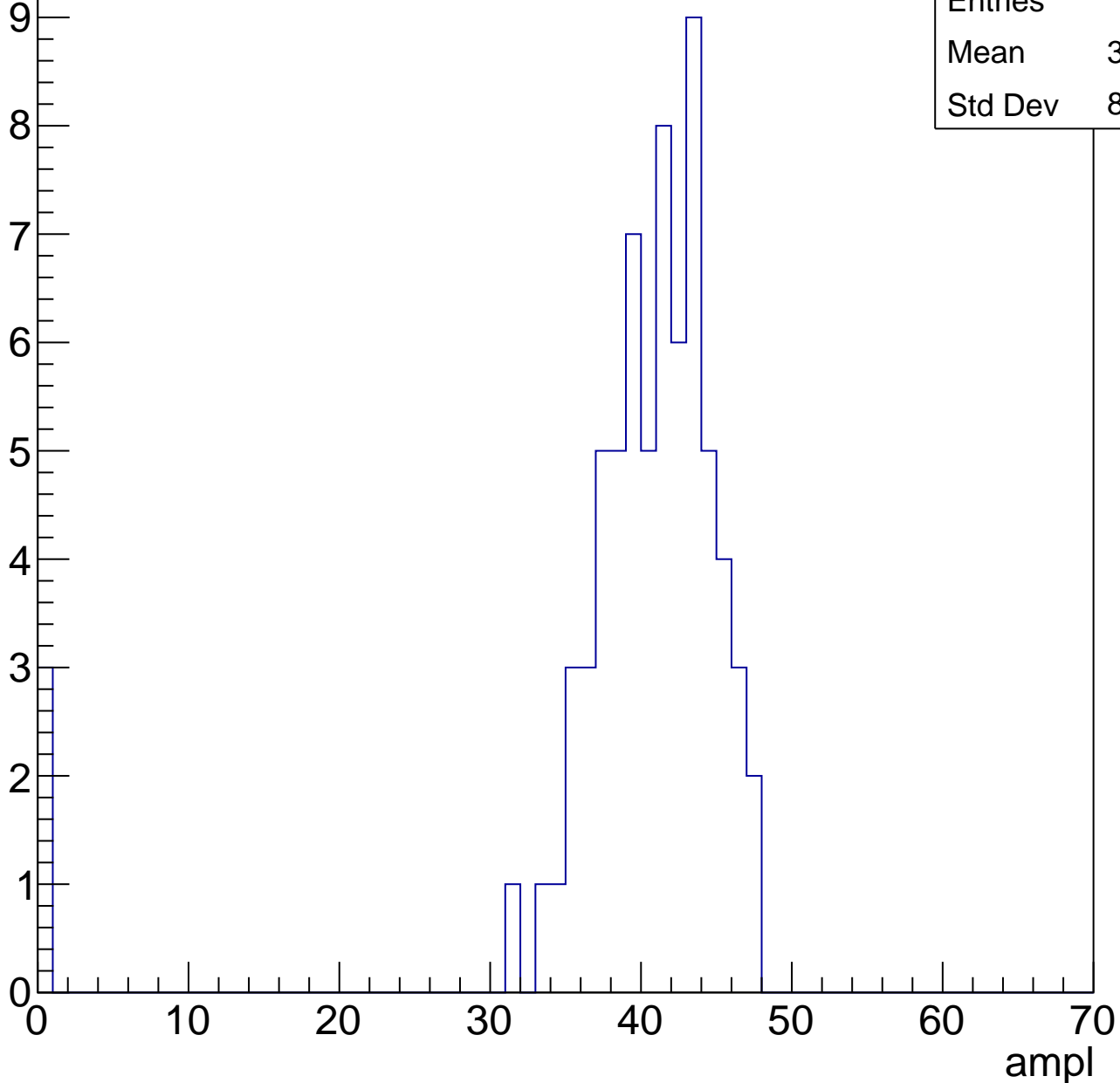


B1L103S, U11-ch108, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	38.85
Std Dev	8.853

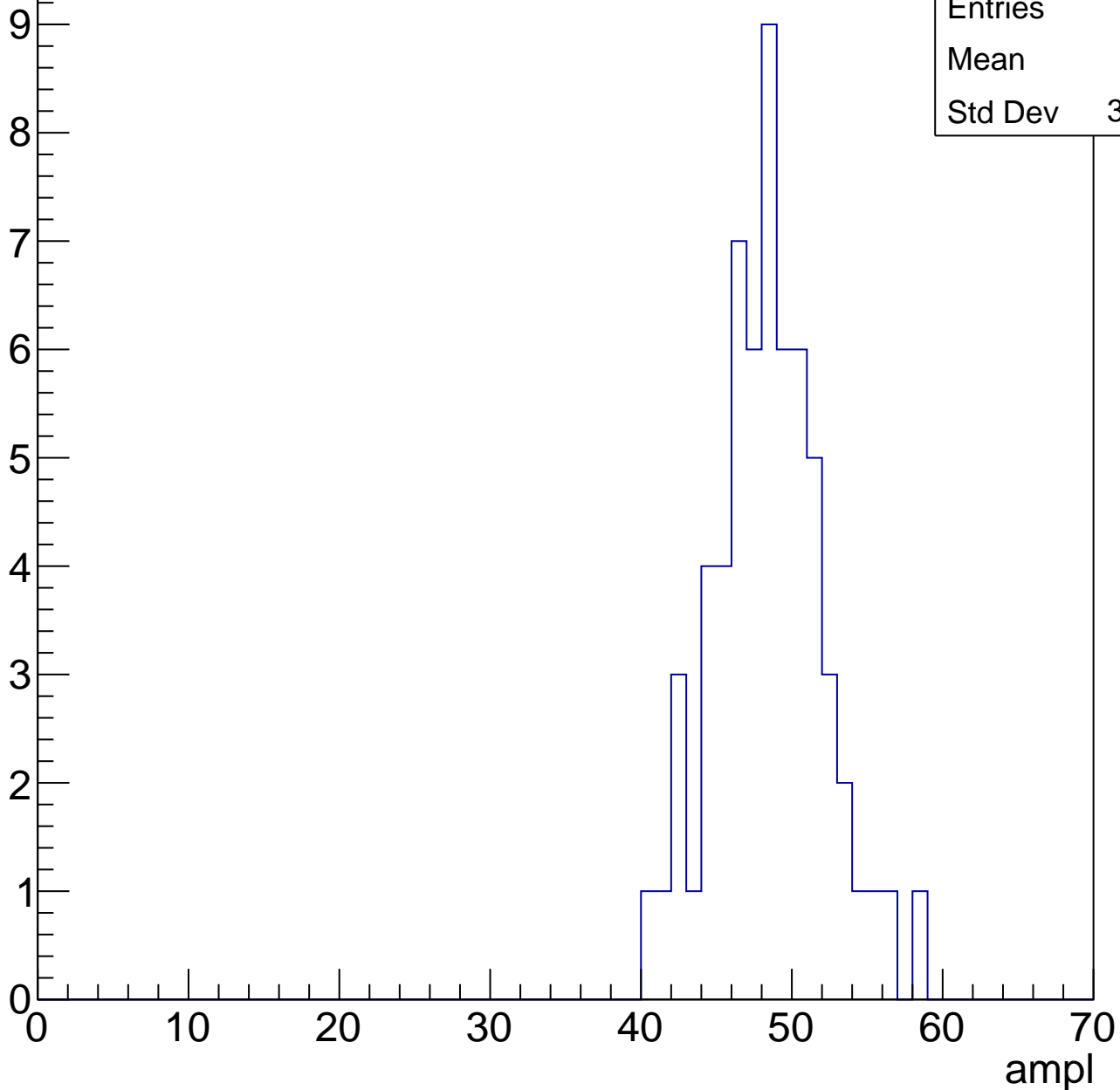


B1L103S, U11-ch108, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	48
Std Dev	3.597

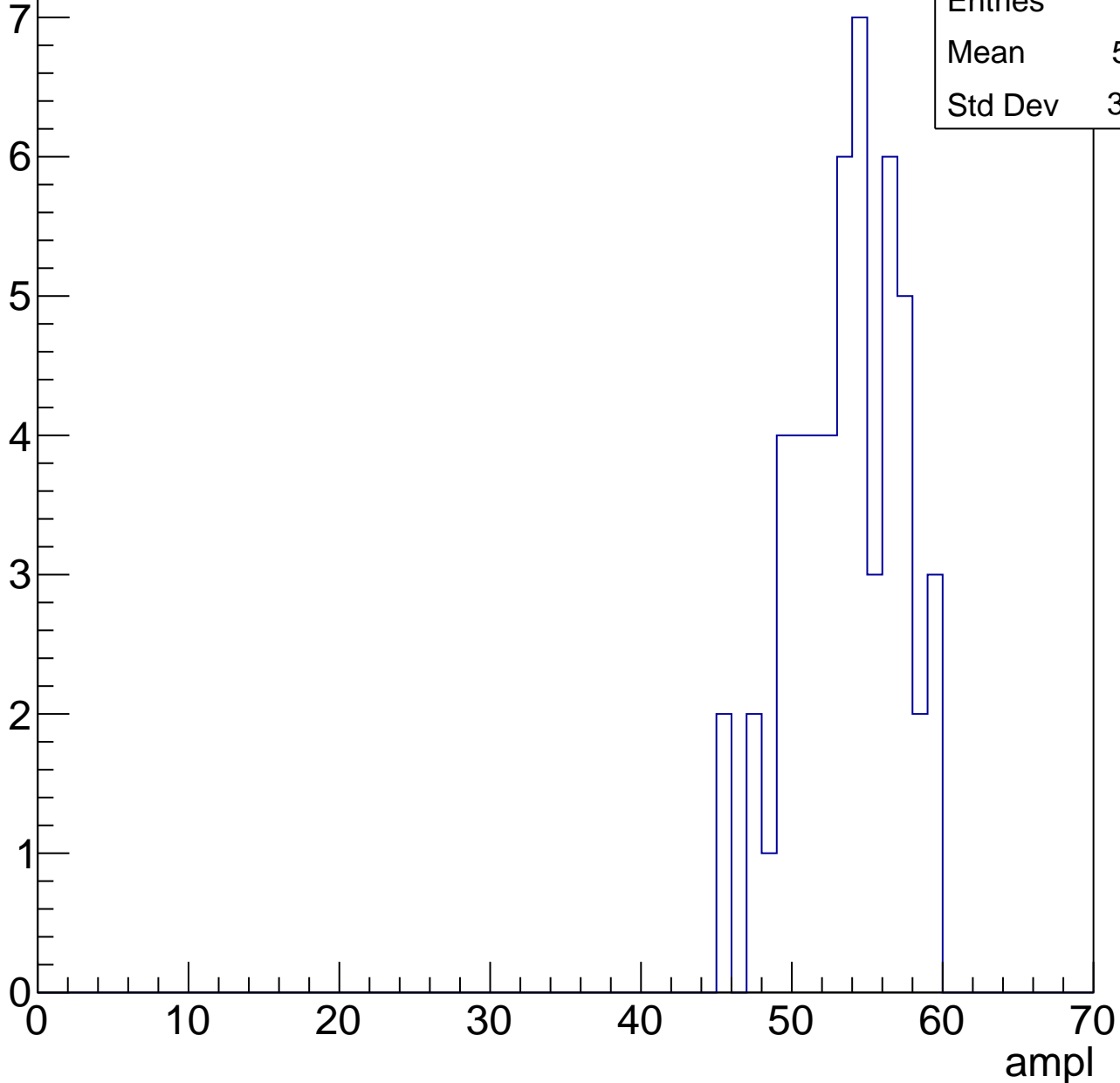


B1L103S, U11-ch108, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

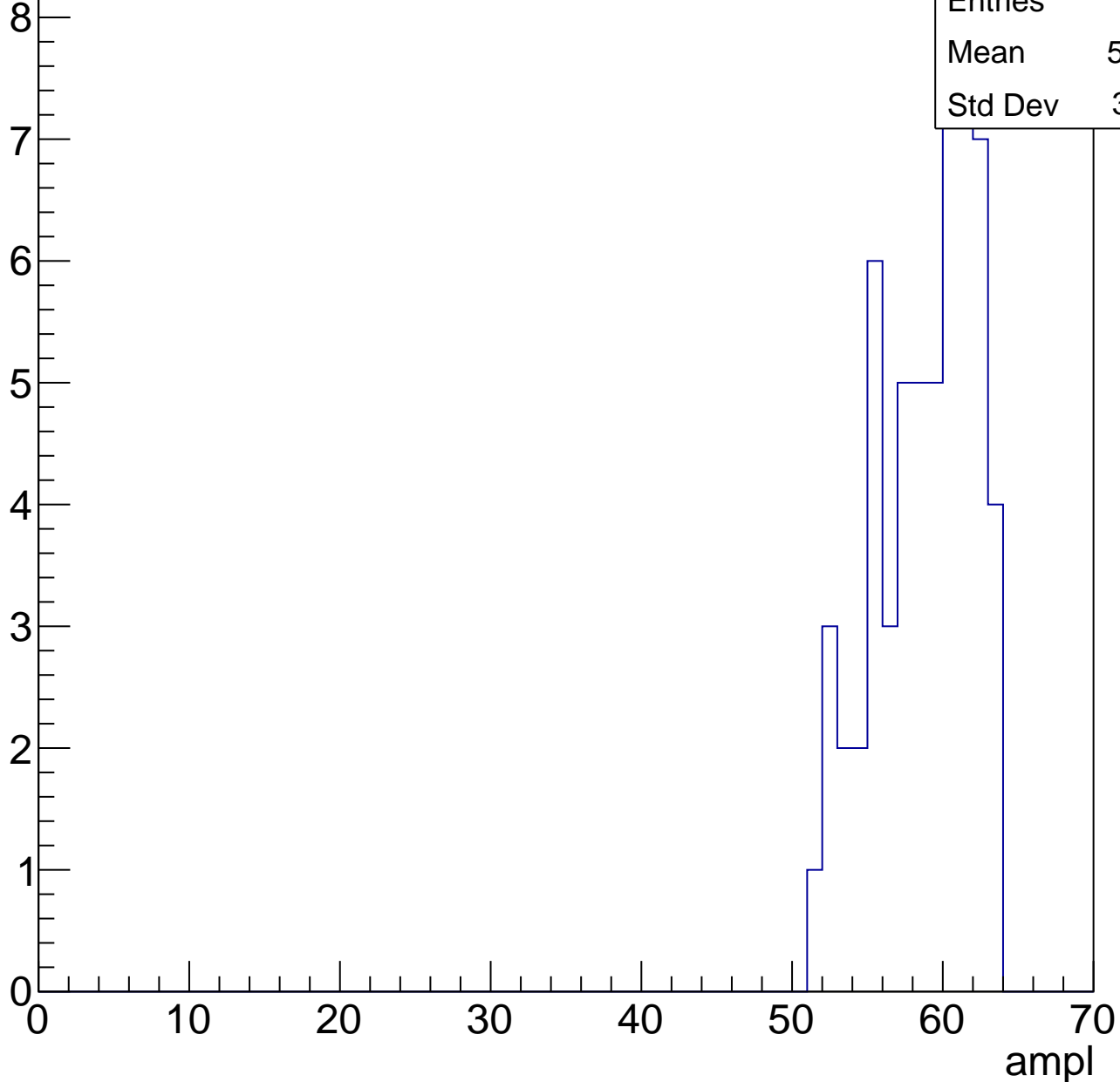
Entries	53
Mean	53.11
Std Dev	3.516



B1L103S, U11-ch108, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

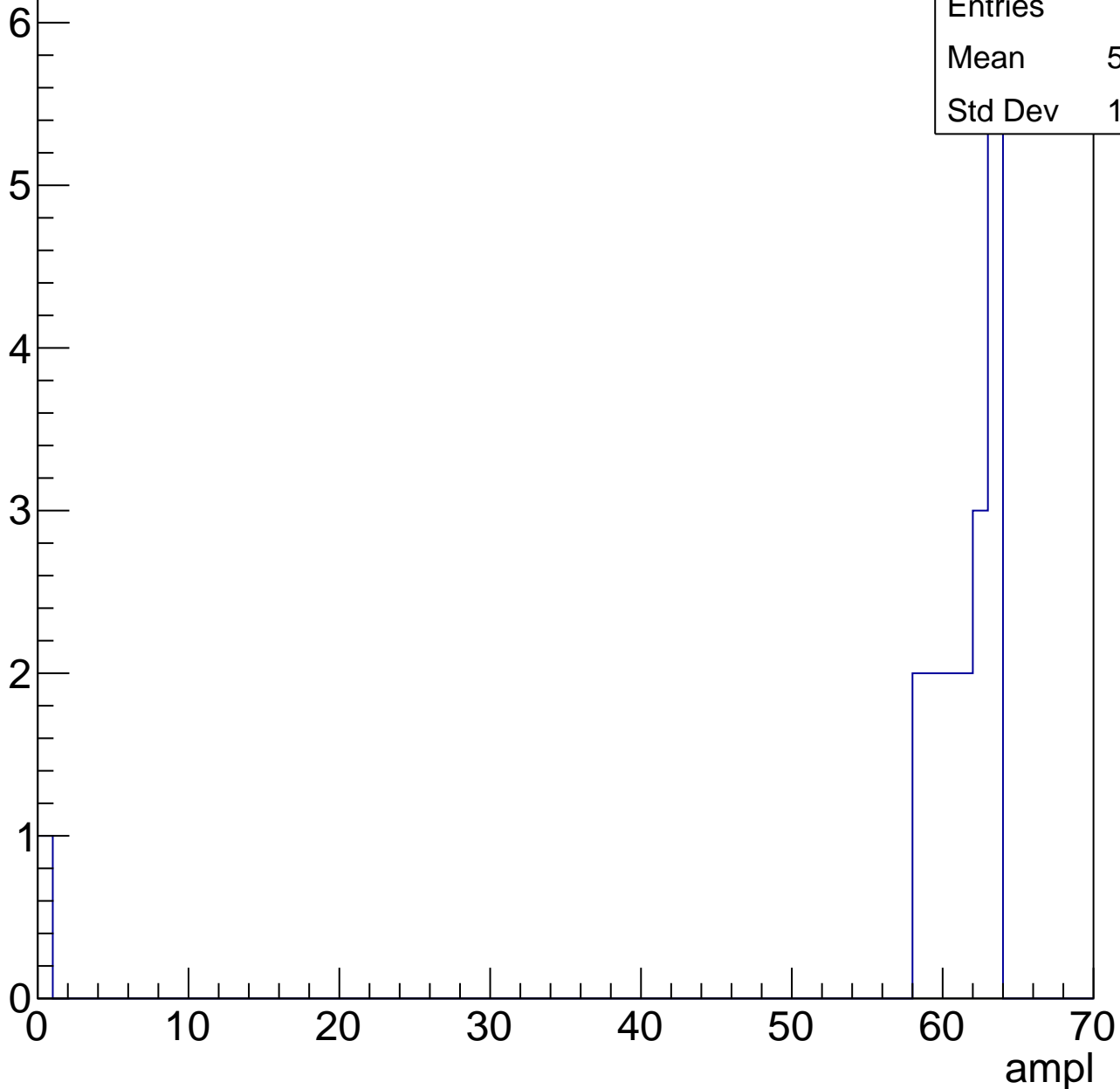


B1L103S, U11-ch108, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	18
Mean	57.78
Std Dev	14.12



B1L103S, U11-ch108, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

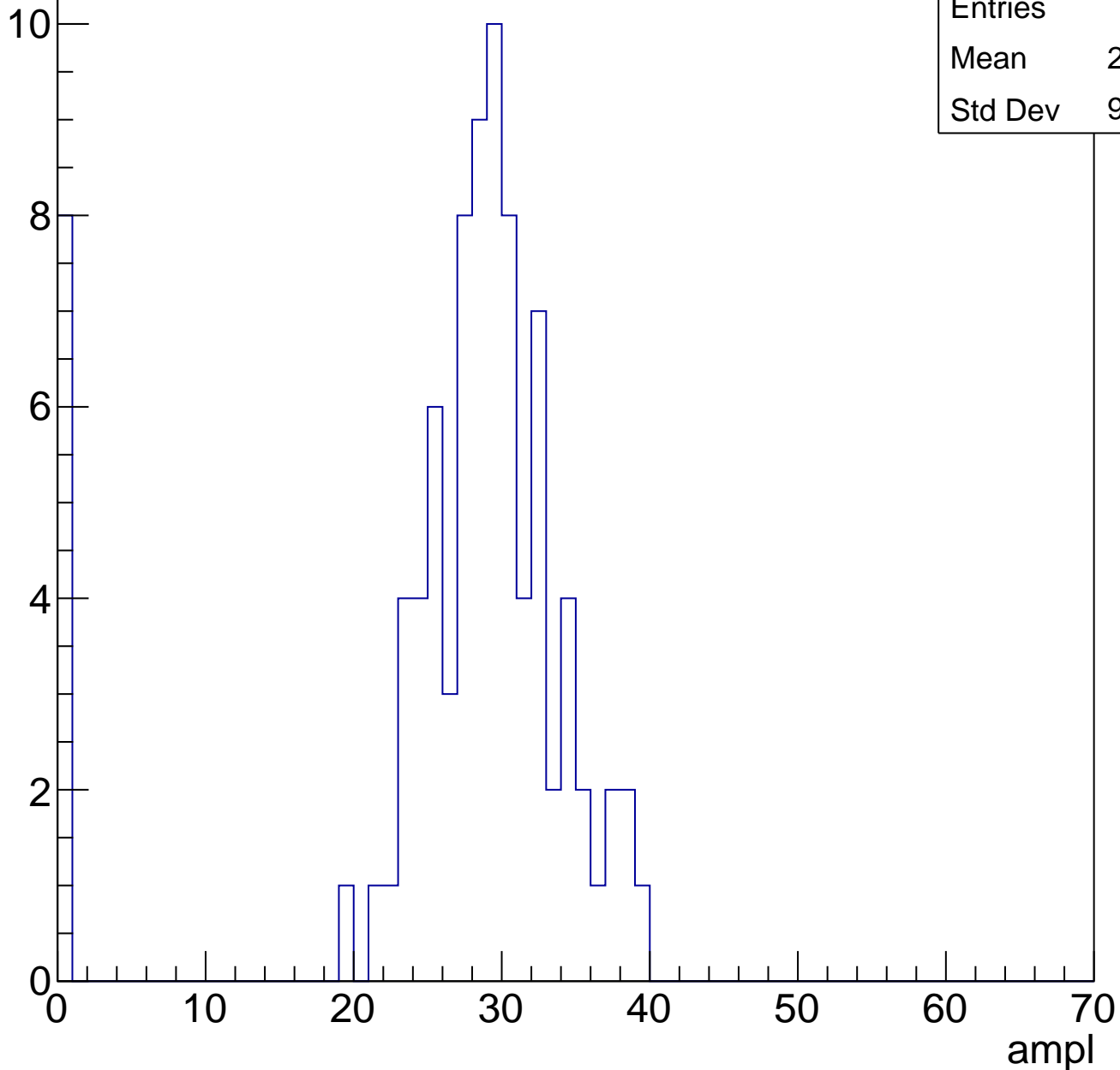
ampl

B1L103S, U11-ch109, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	88
Mean	26.38
Std Dev	9.215

Entry

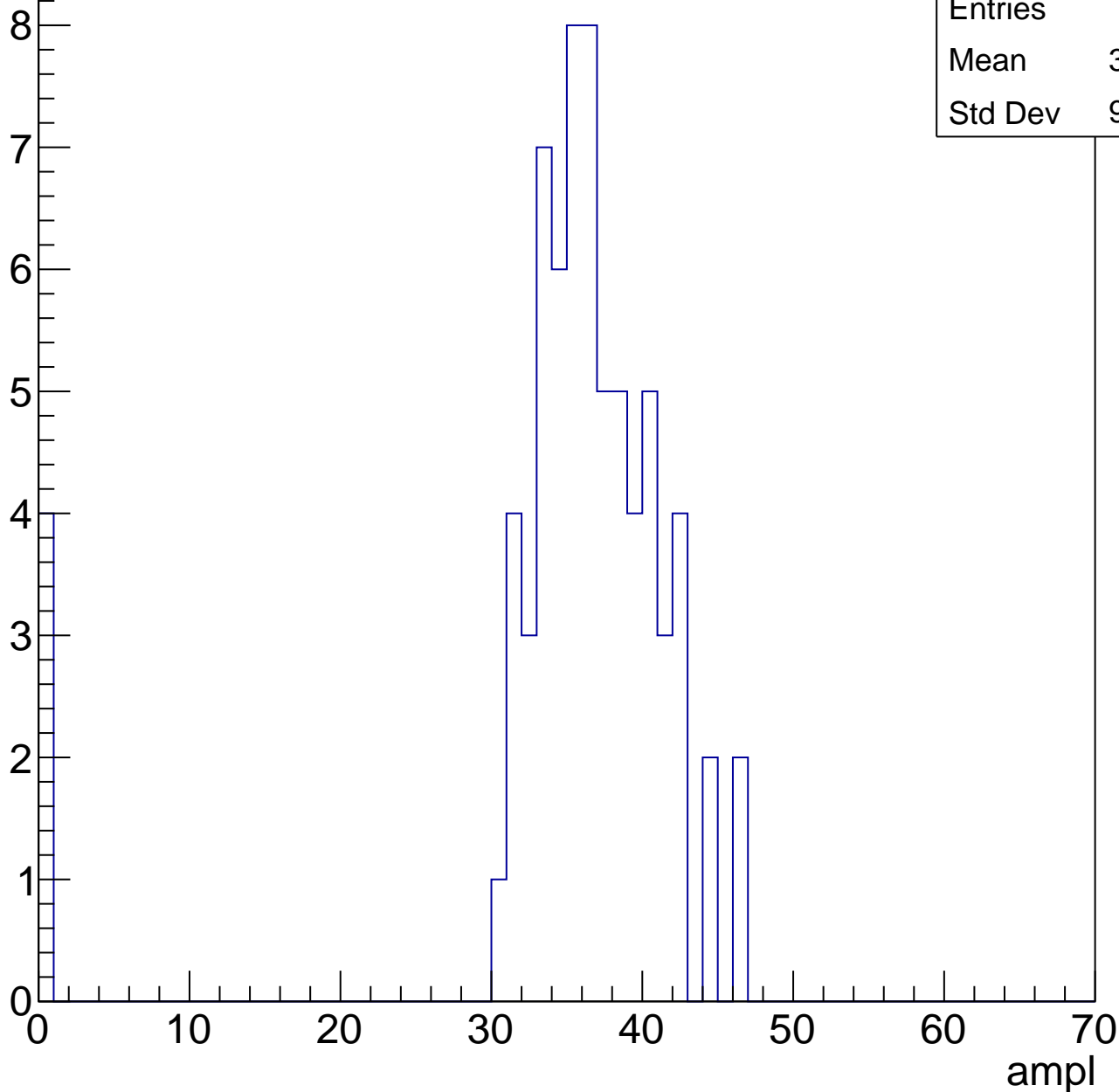


B1L103S, U11-ch109, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	34.58
Std Dev	9.198

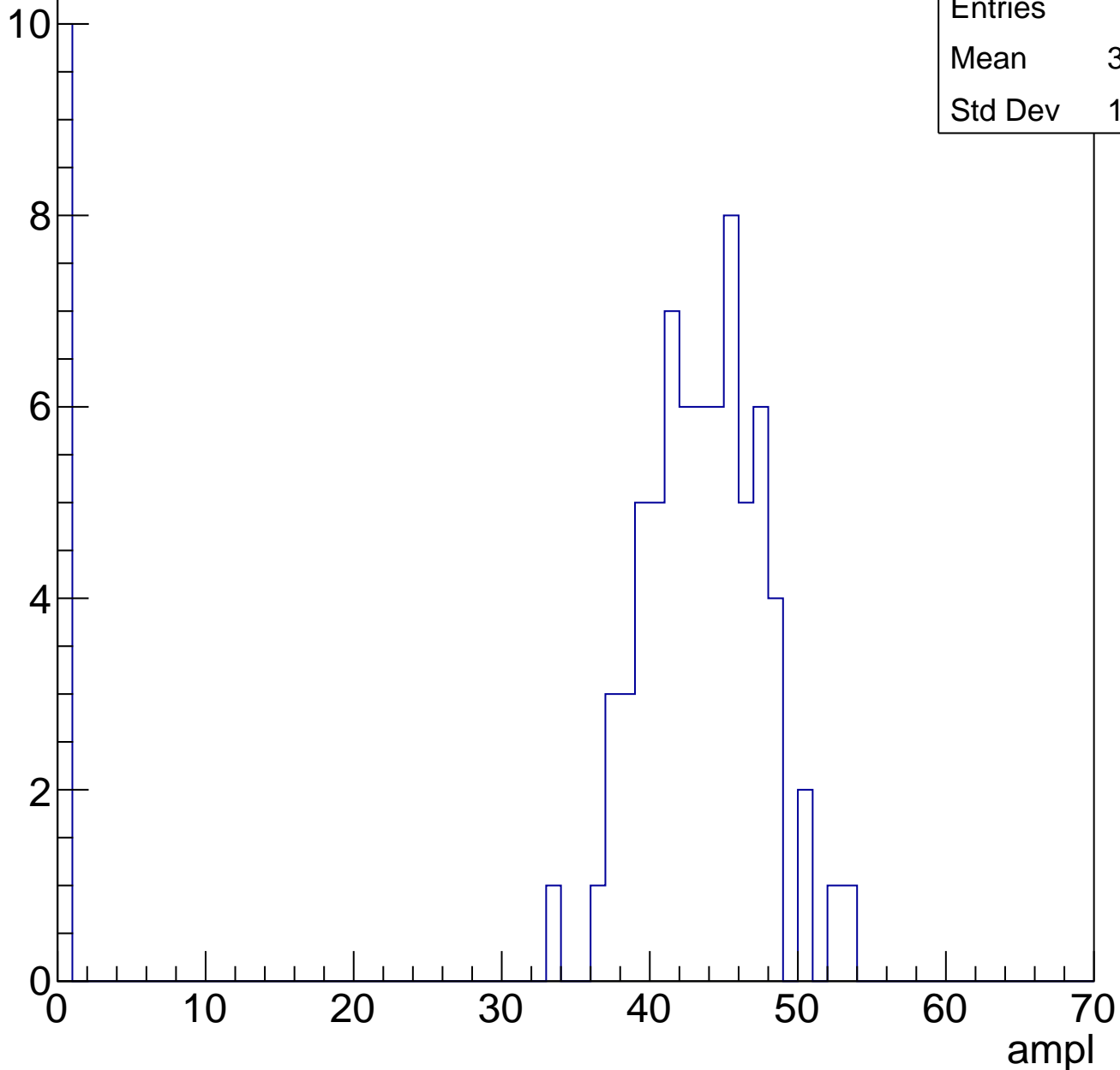


B1L103S, U11-ch109, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	37.74
Std Dev	14.72

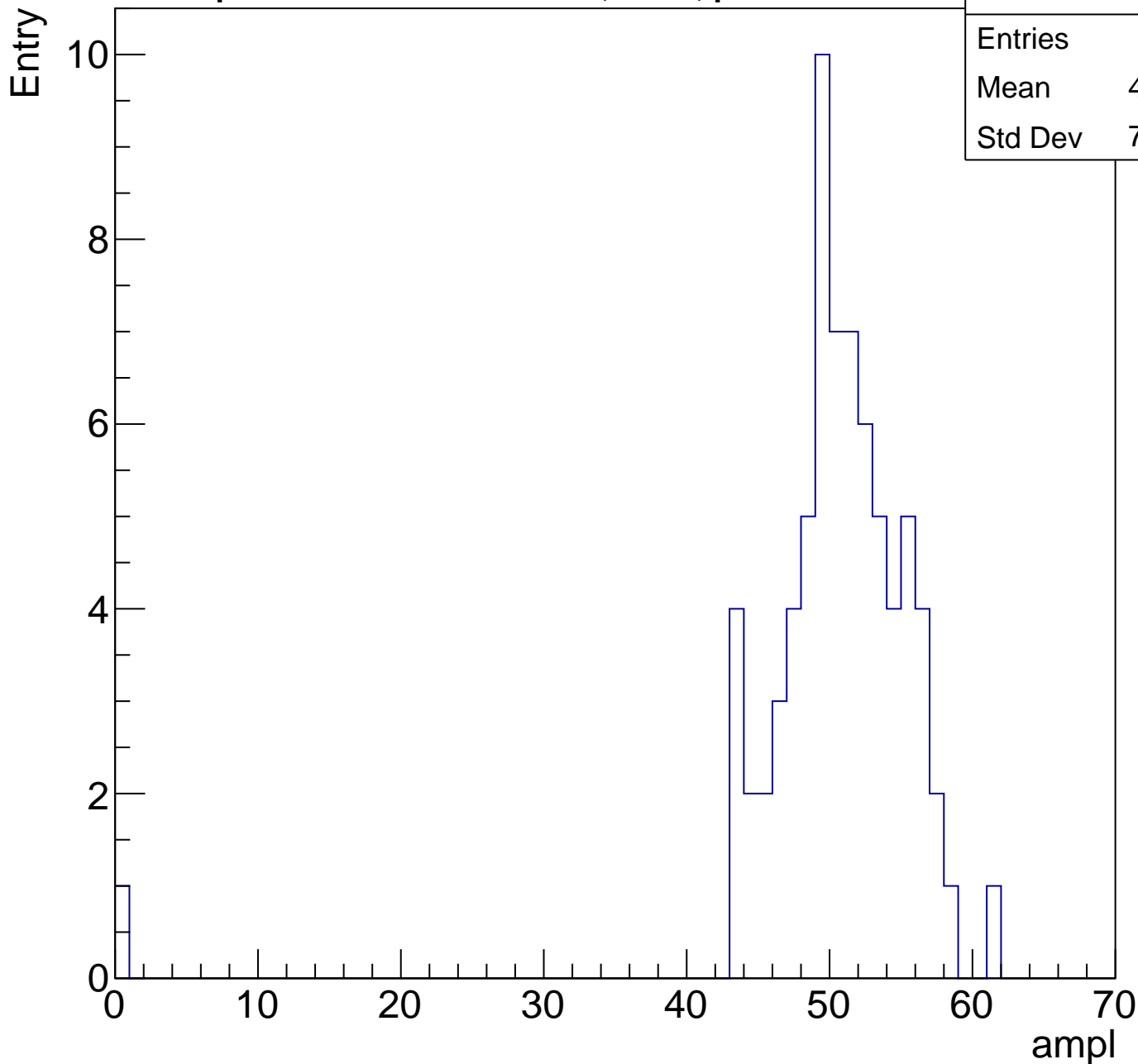
Entry



B1L103S, U11-ch109, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	73
Mean	49.84
Std Dev	7.044

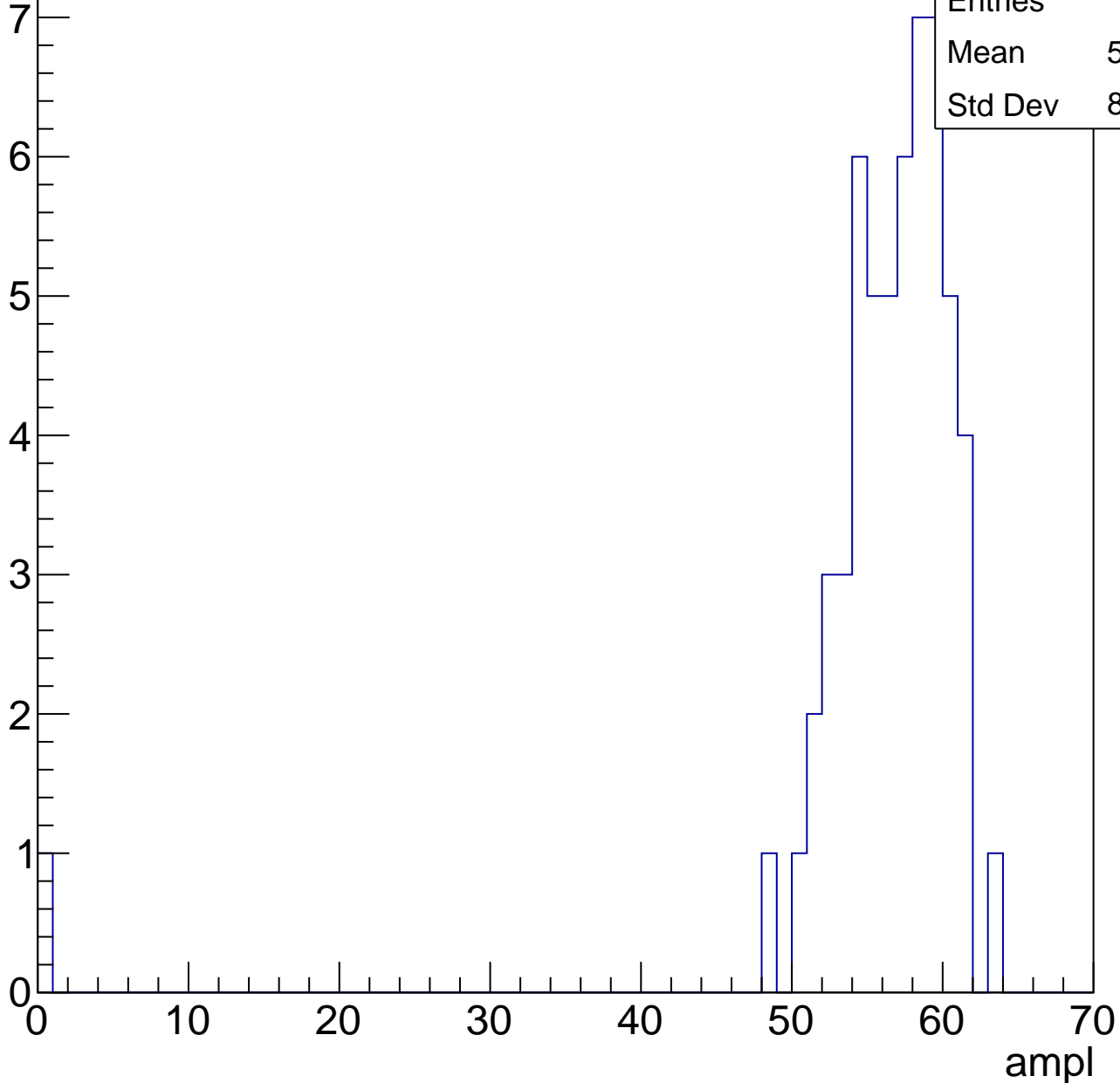


B1L103S, U11-ch109, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	55.47
Std Dev	8.057

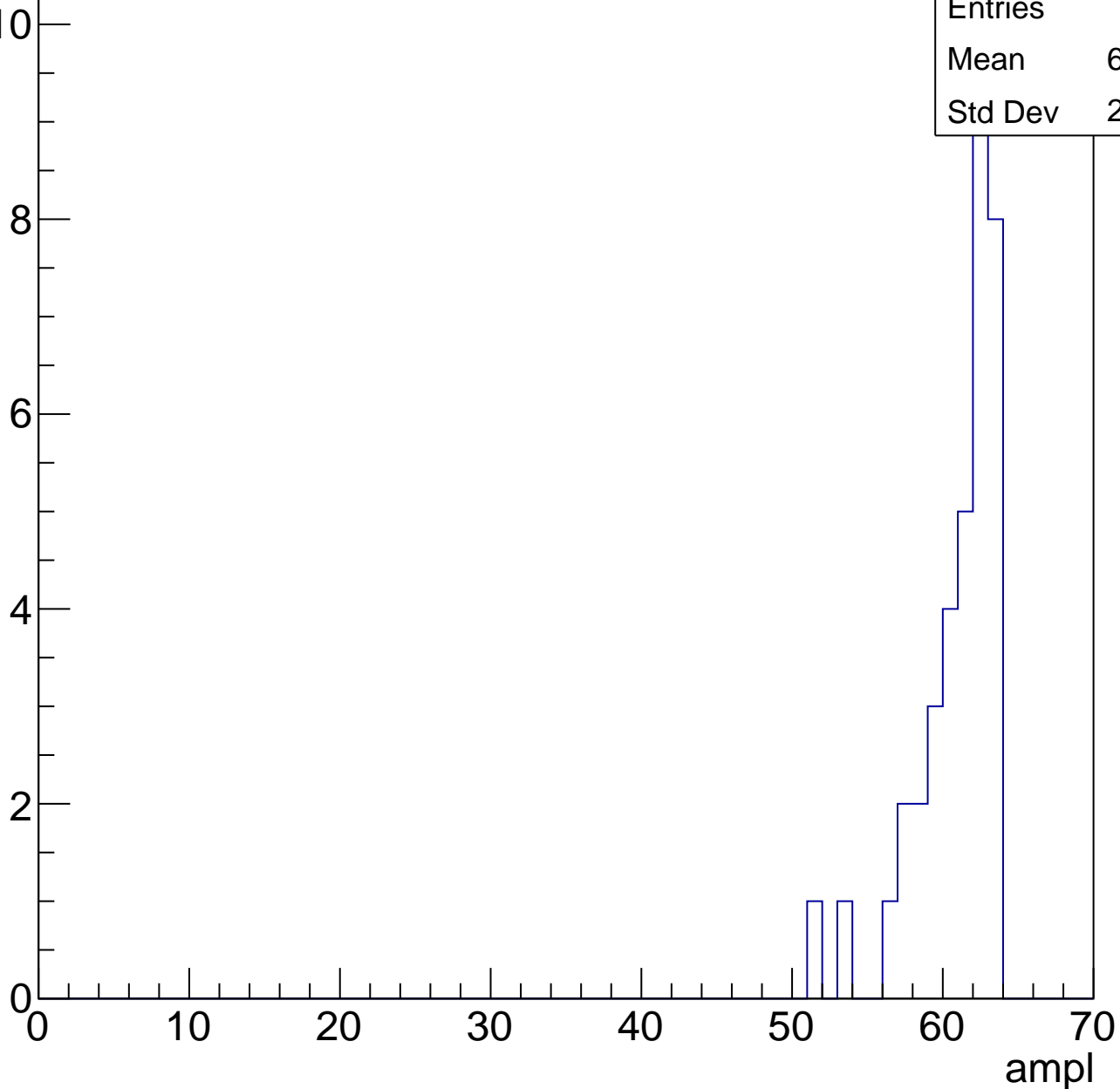


B1L103S, U11-ch109, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	37
Mean	60.43
Std Dev	2.776



B1L103S, U11-ch109, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch109, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

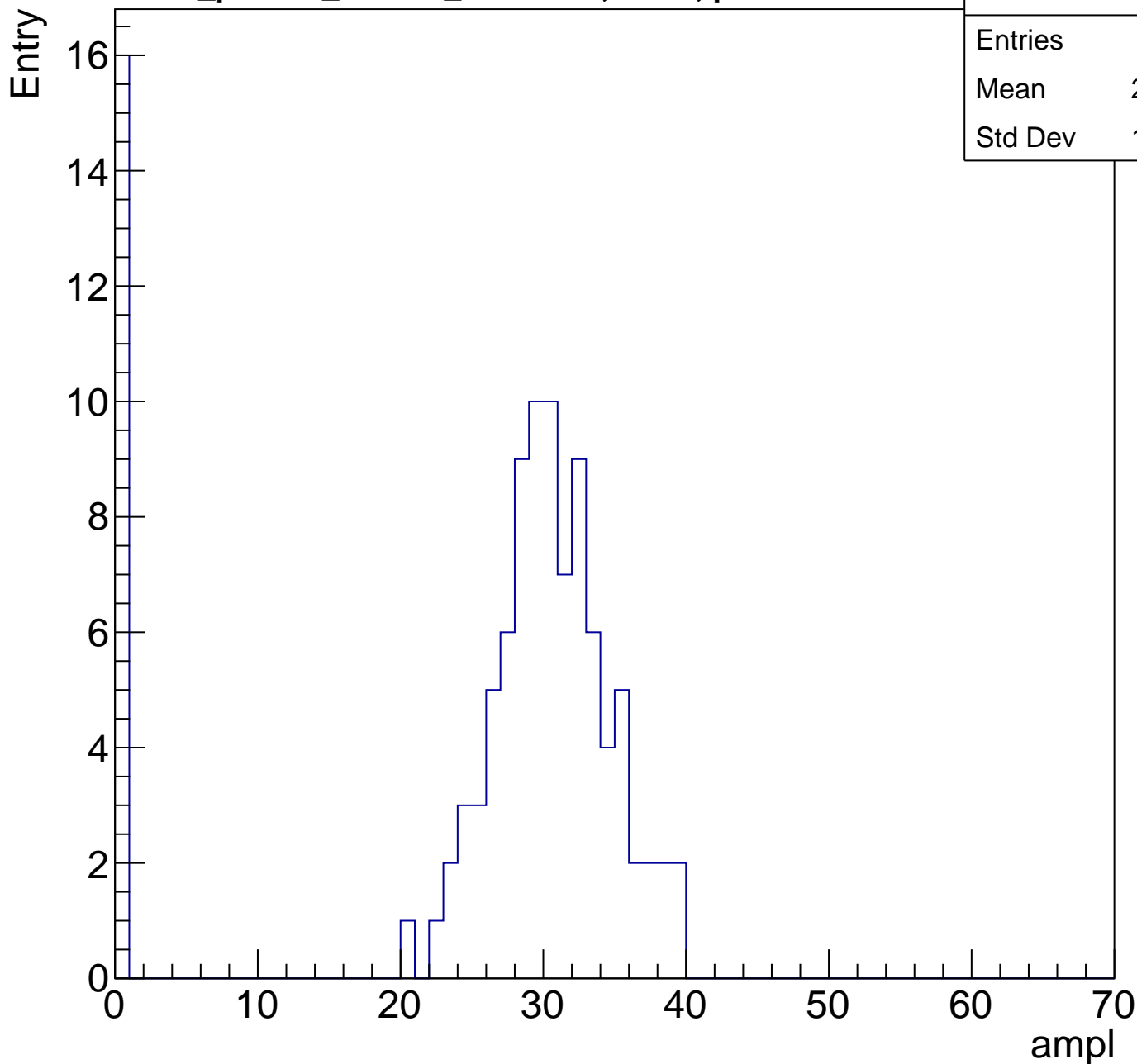
Entries	18
Mean	0
Std Dev	0

ampl

B1L103S, U11-ch110, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	105
Mean	25.55
Std Dev	11.42

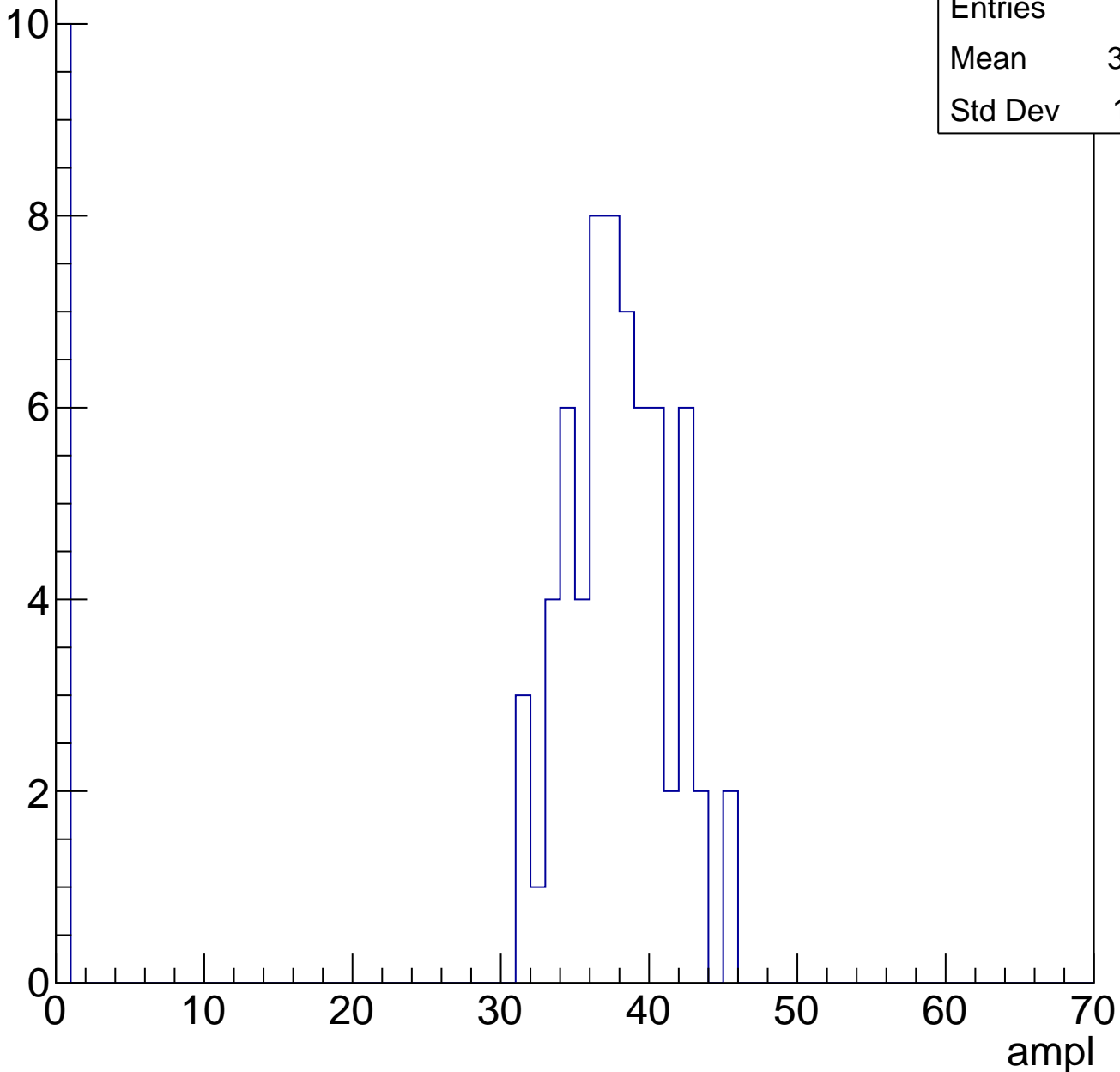


B1L103S, U11-ch110, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	32.47
Std Dev	13.11

Entry

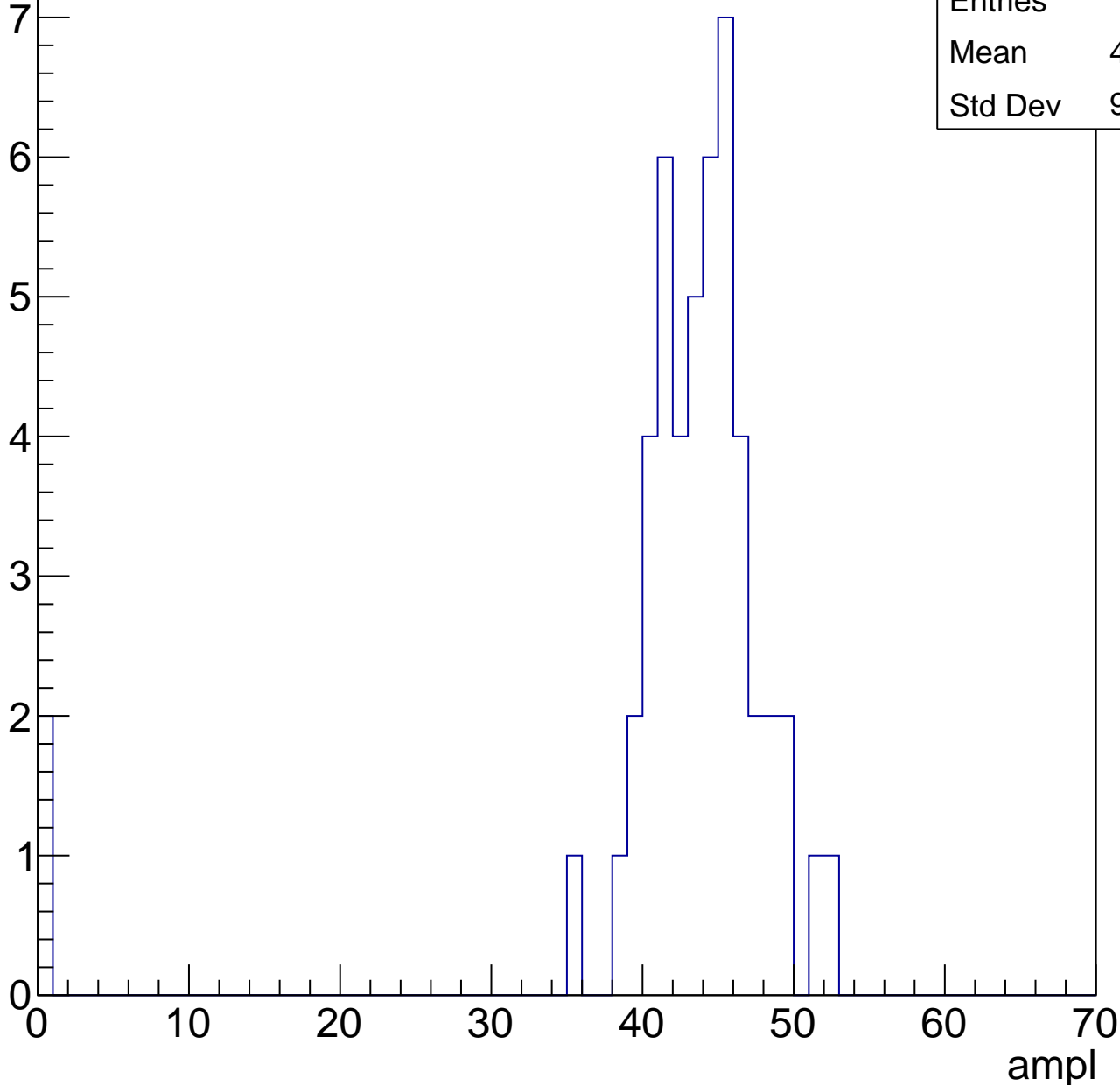


B1L103S, U11-ch110, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	41.88
Std Dev	9.153

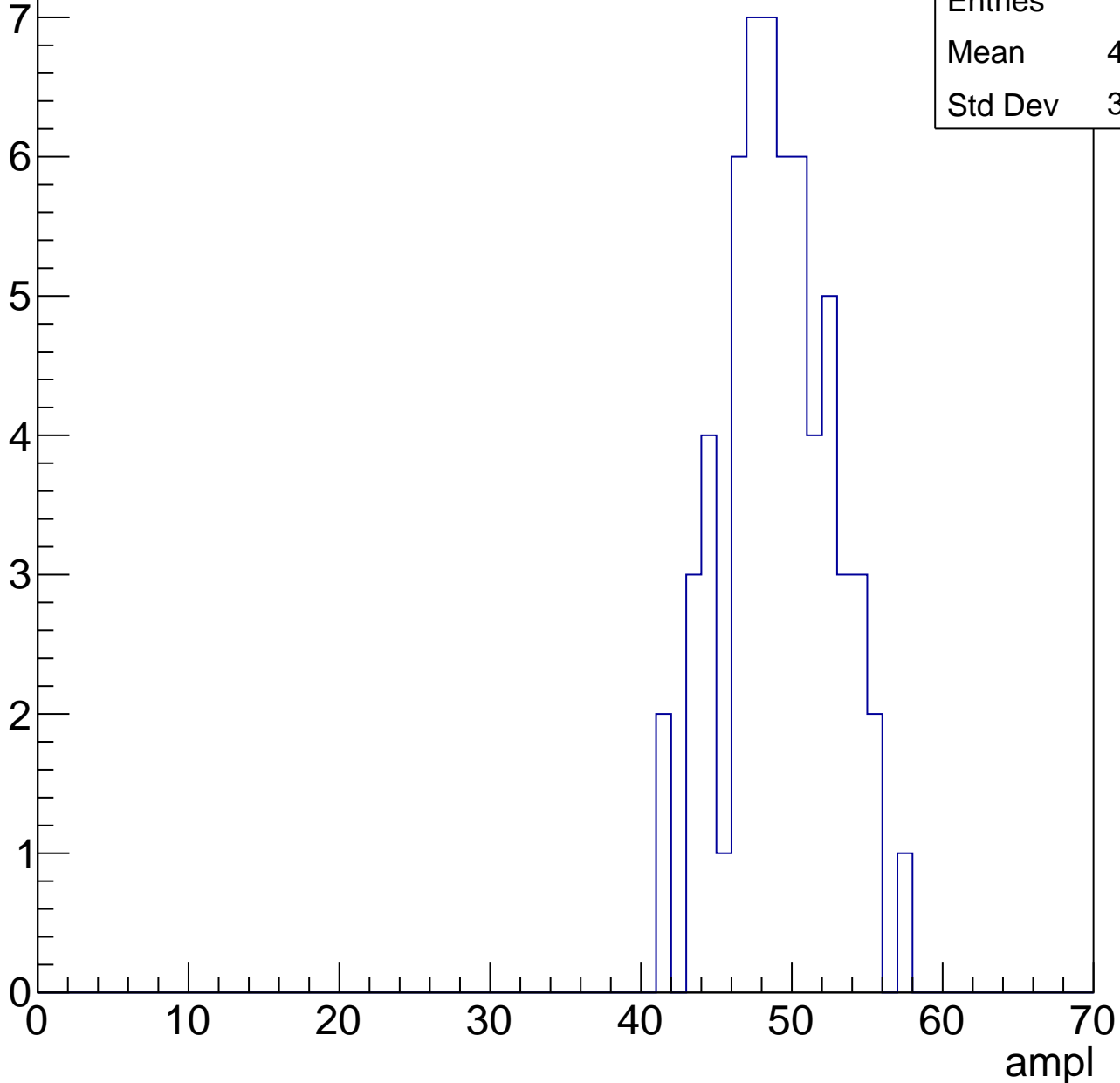


B1L103S, U11-ch110, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	48.65
Std Dev	3.558

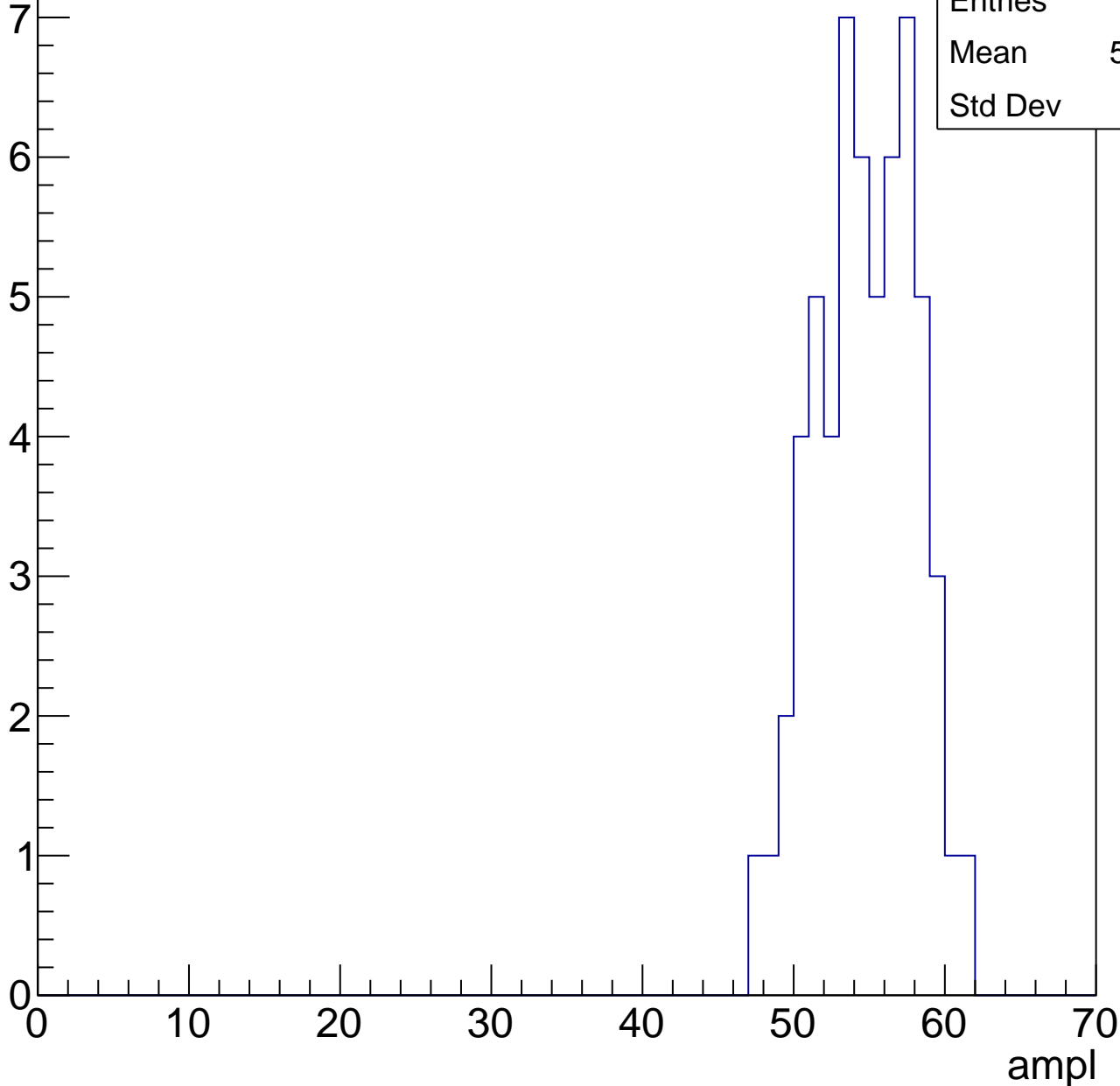


B1L103S, U11-ch110, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

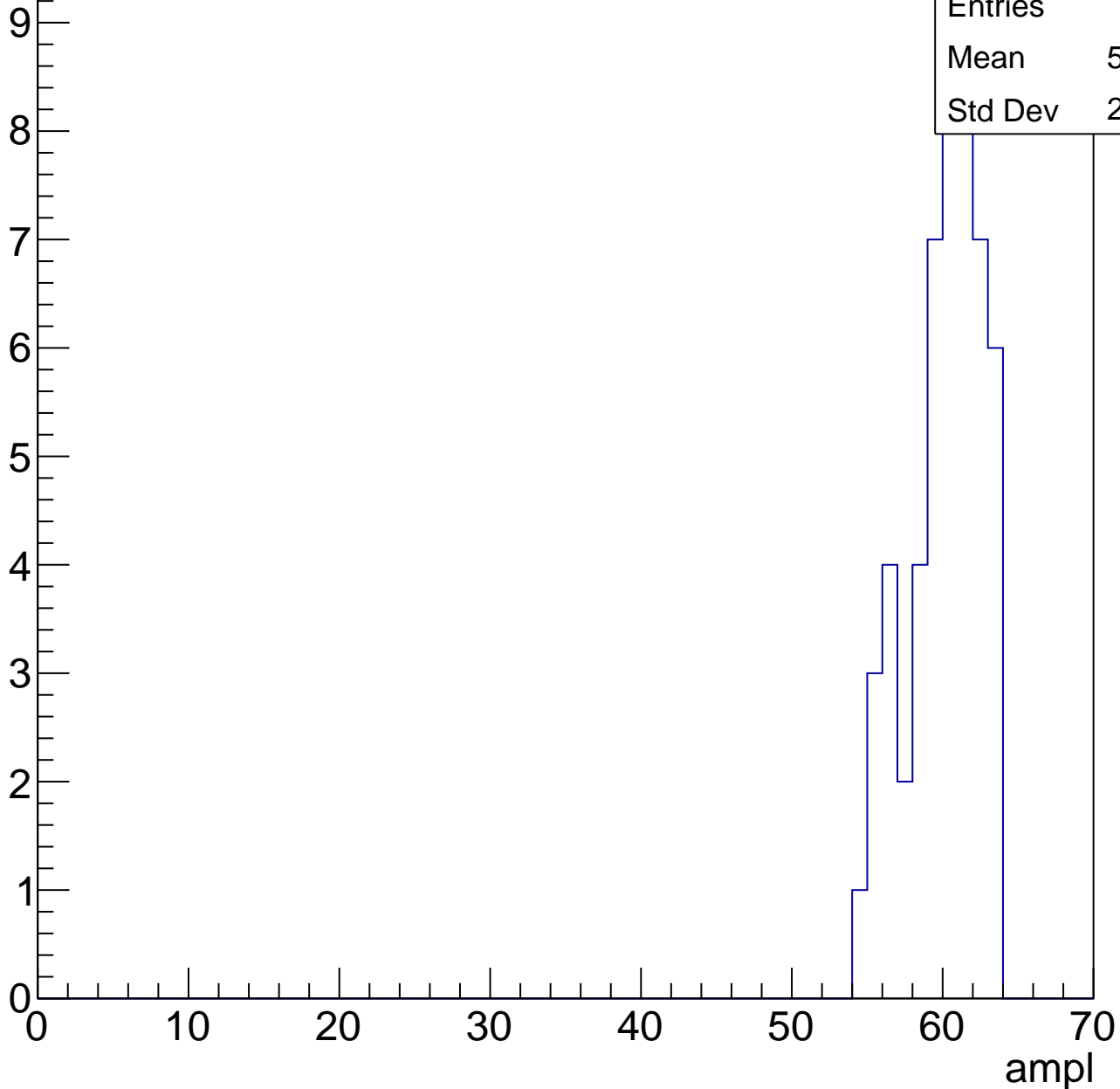
Entries	58
Mean	54.29
Std Dev	3.2



B1L103S, U11-ch110, adc5

calib_packv5_041523_1651.root, FC#0, port C2

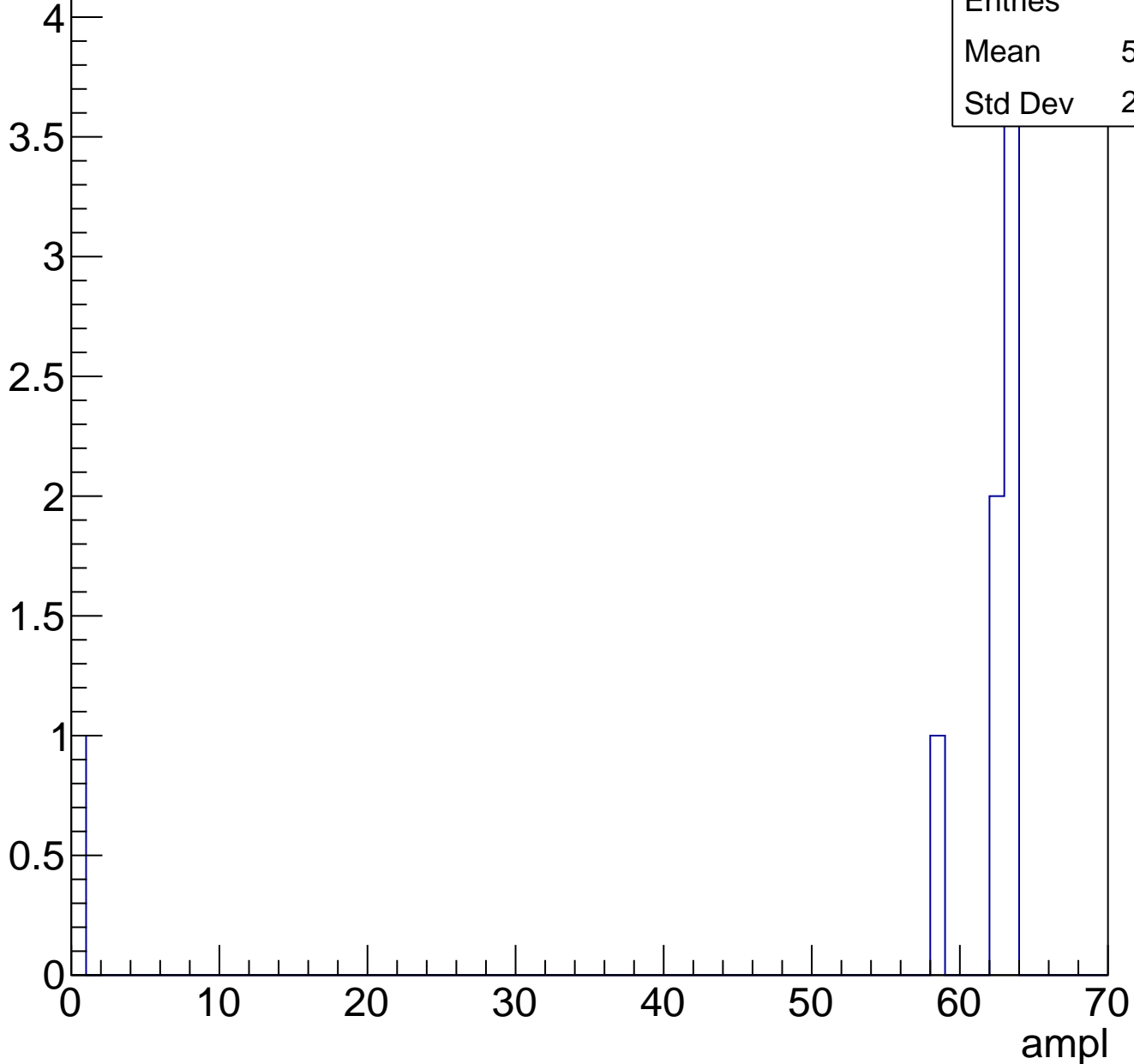
Entry



B1L103S, U11-ch110, adc6

calib_packv5_041523_1651.root, FC#0, port C2

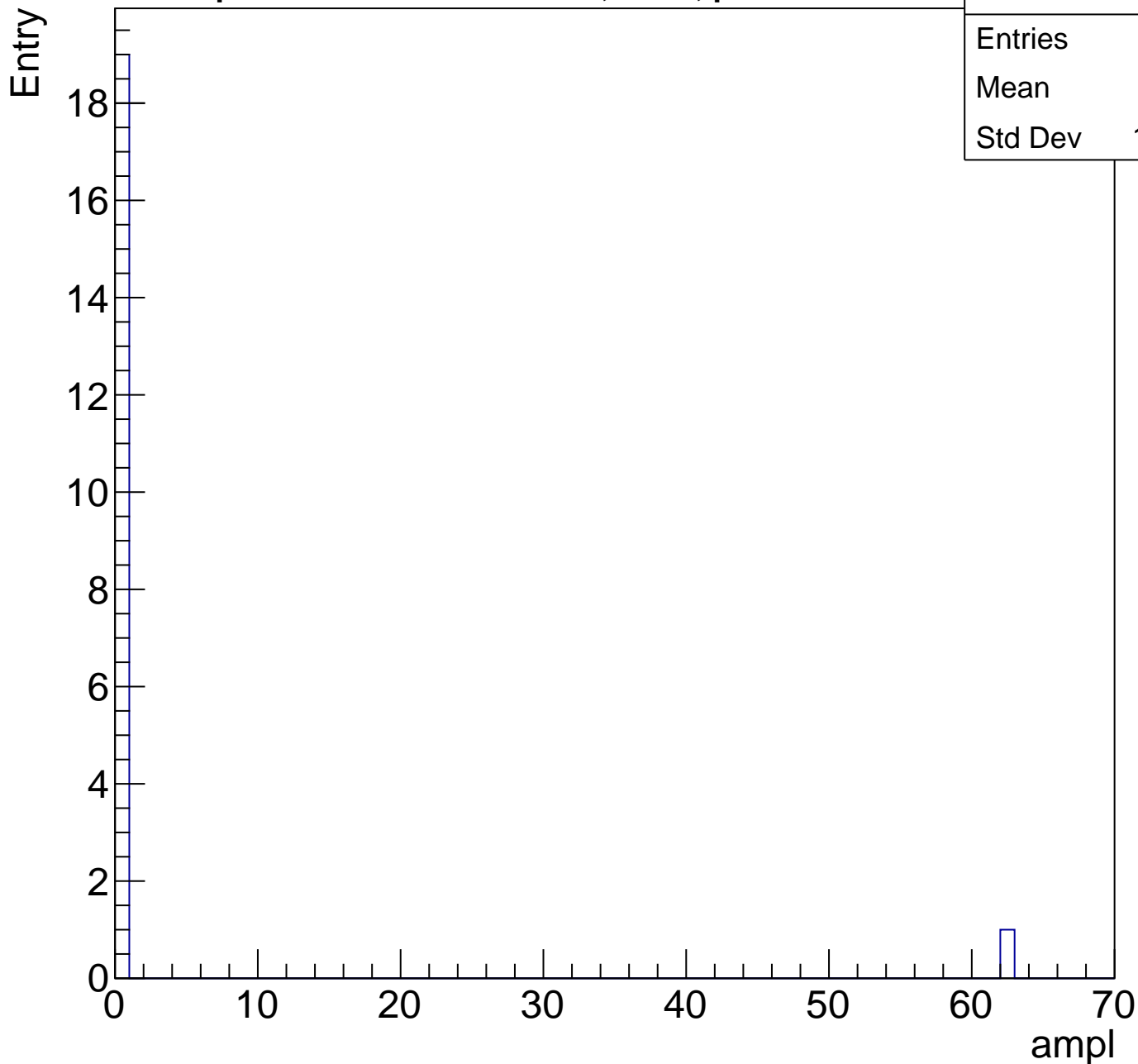
Entry



B1L103S, U11-ch110, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51



B1L103S, U11-ch111, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	87
Mean	29.21
Std Dev	10.05

Entry

10
8
6
4
2
0

0

10

20

30

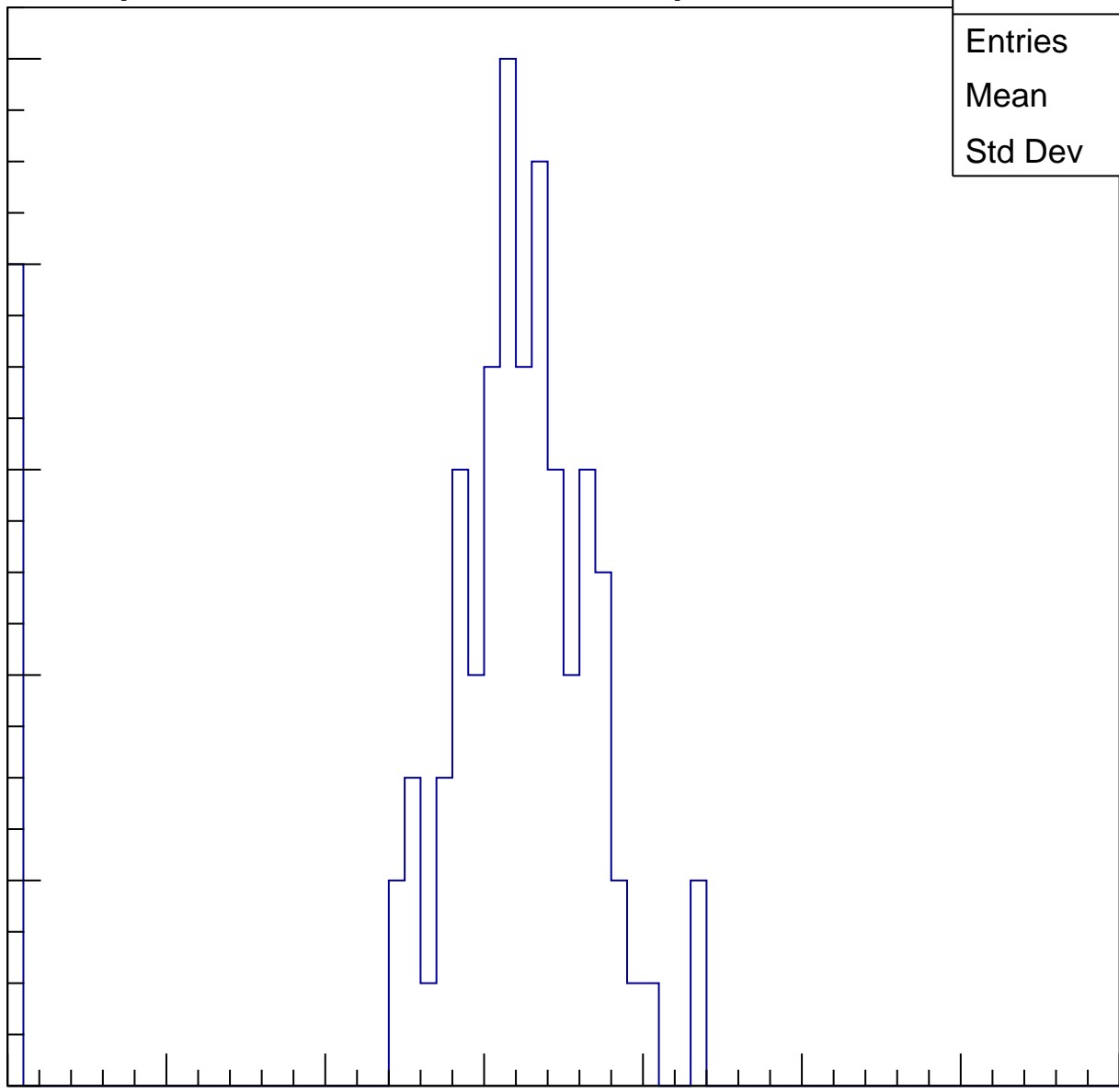
40

50

60

70

ampl

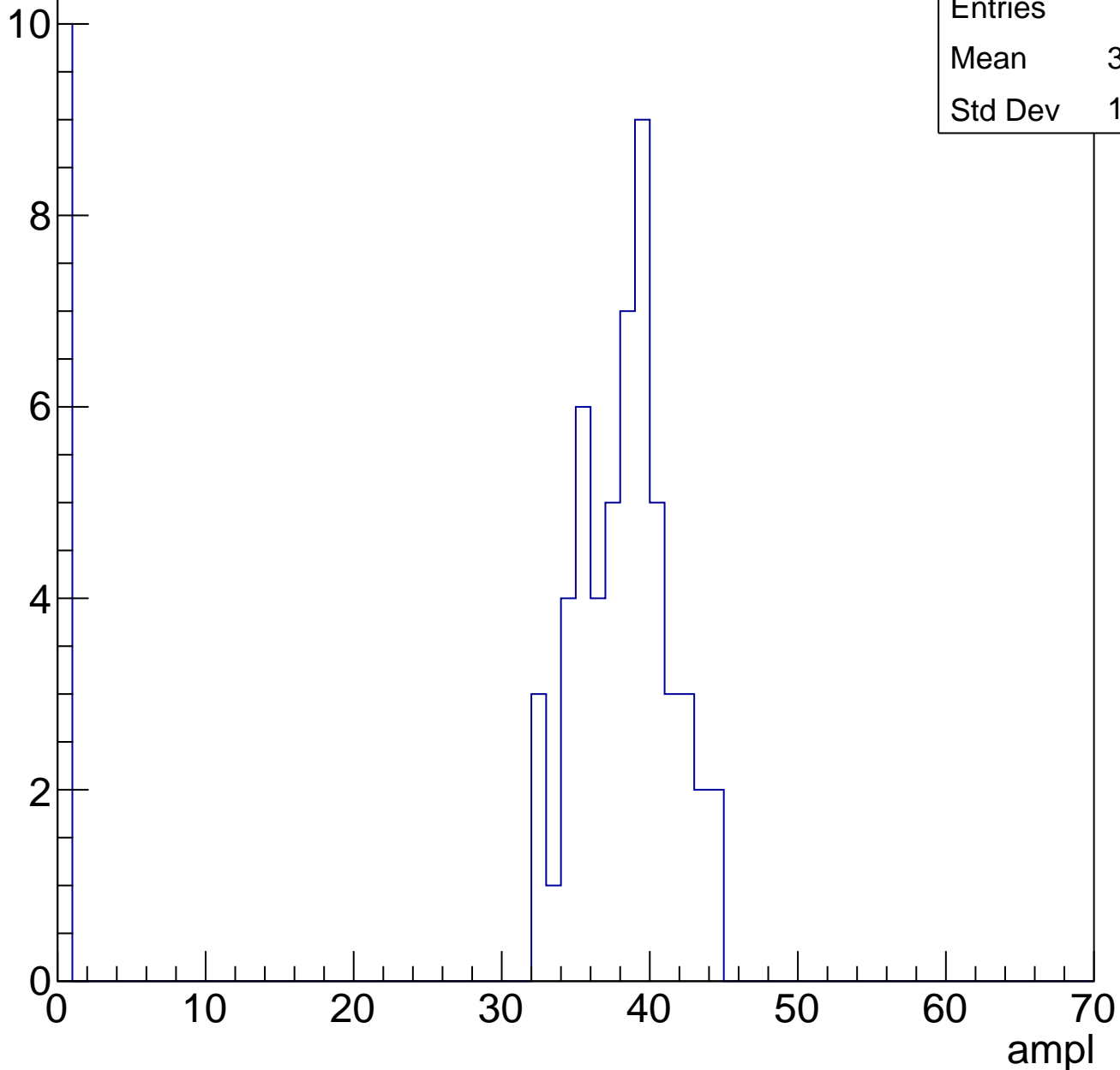


B1L103S, U11-ch111, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	64
Mean	31.94
Std Dev	14.02

Entry

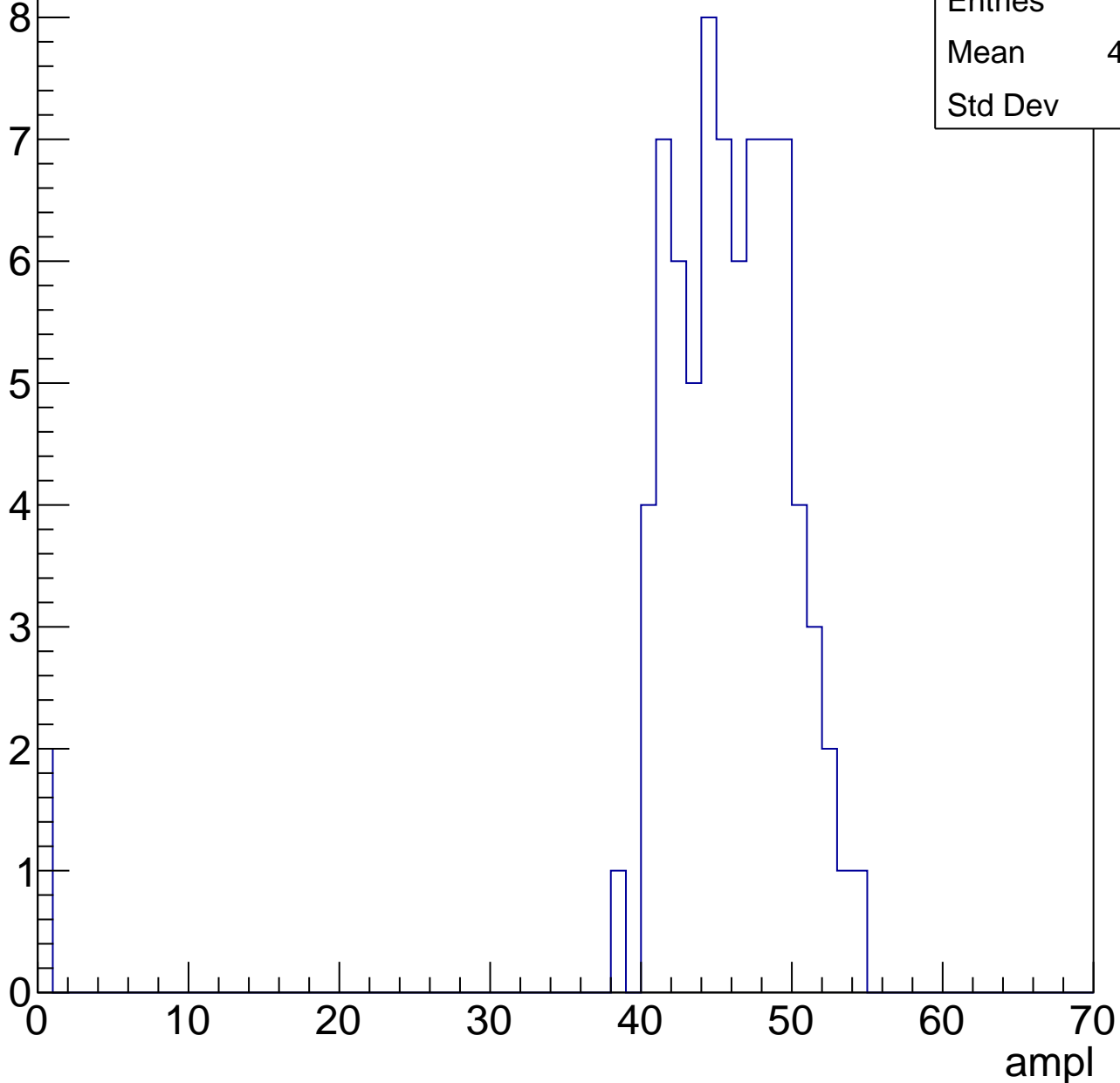


B1L103S, U11-ch111, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	44.45
Std Dev	8.03

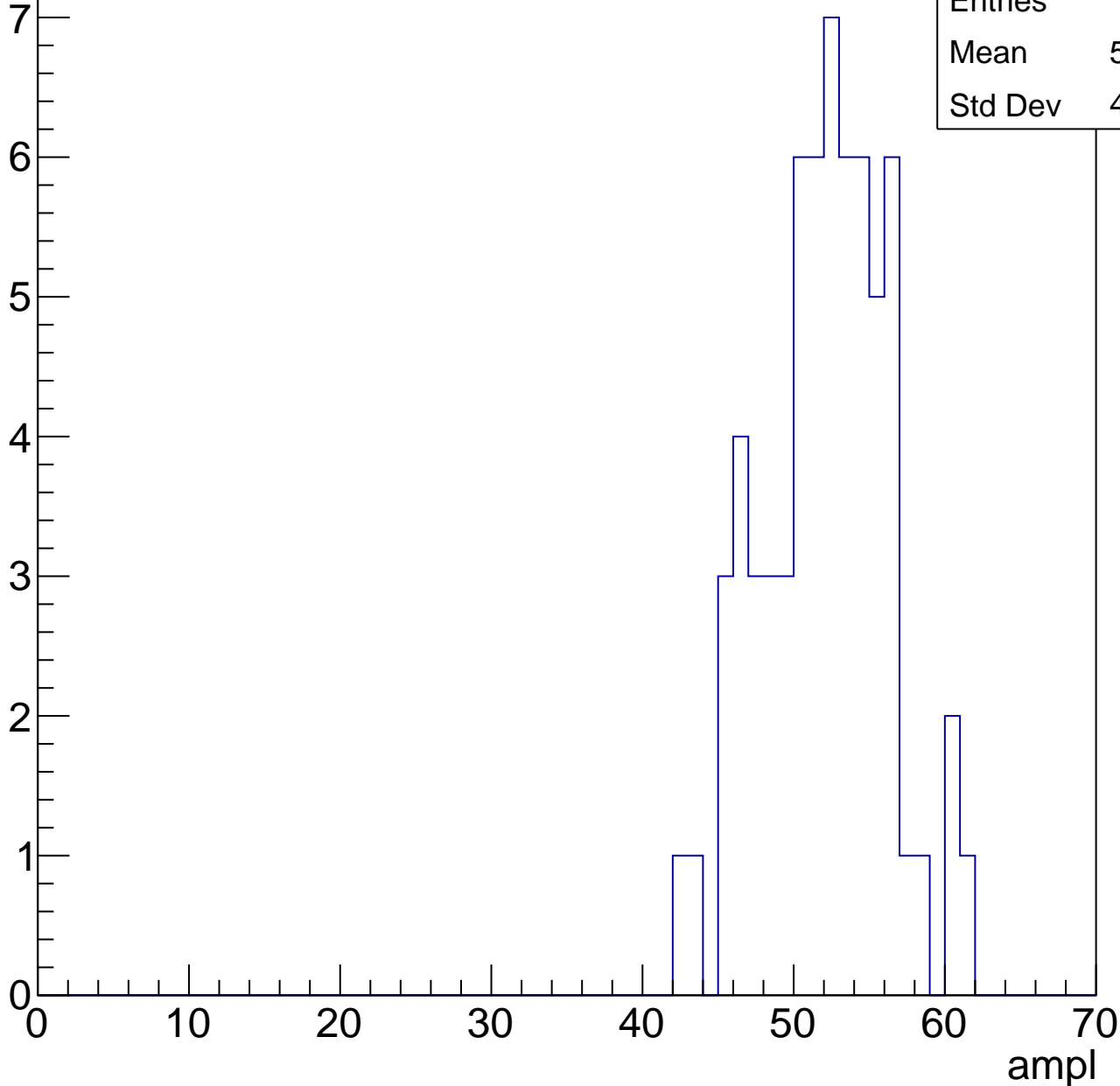


B1L103S, U11-ch111, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	51.62
Std Dev	4.083

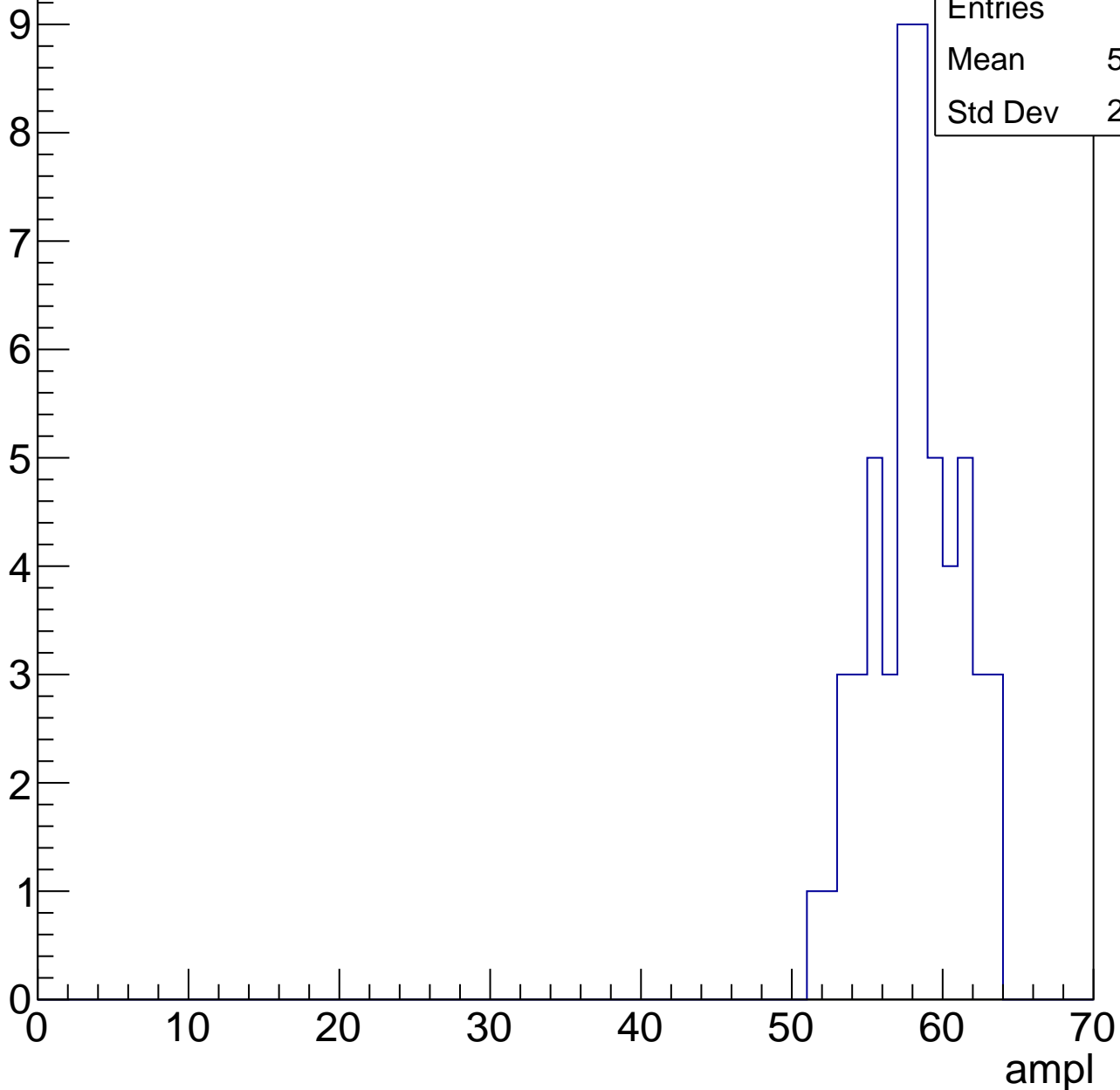


B1L103S, U11-ch111, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	57.72
Std Dev	2.915

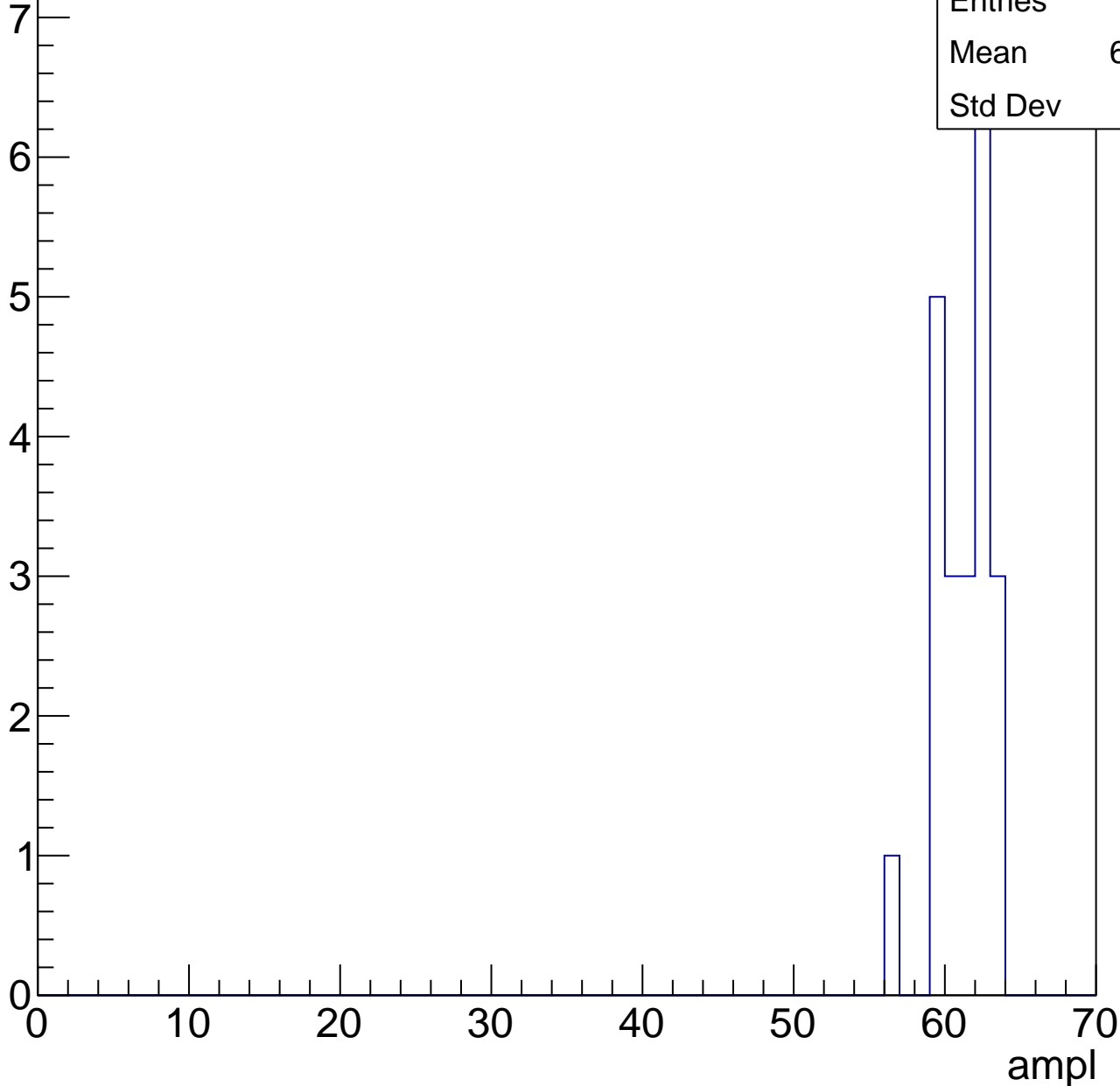


B1L103S, U11-ch111, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

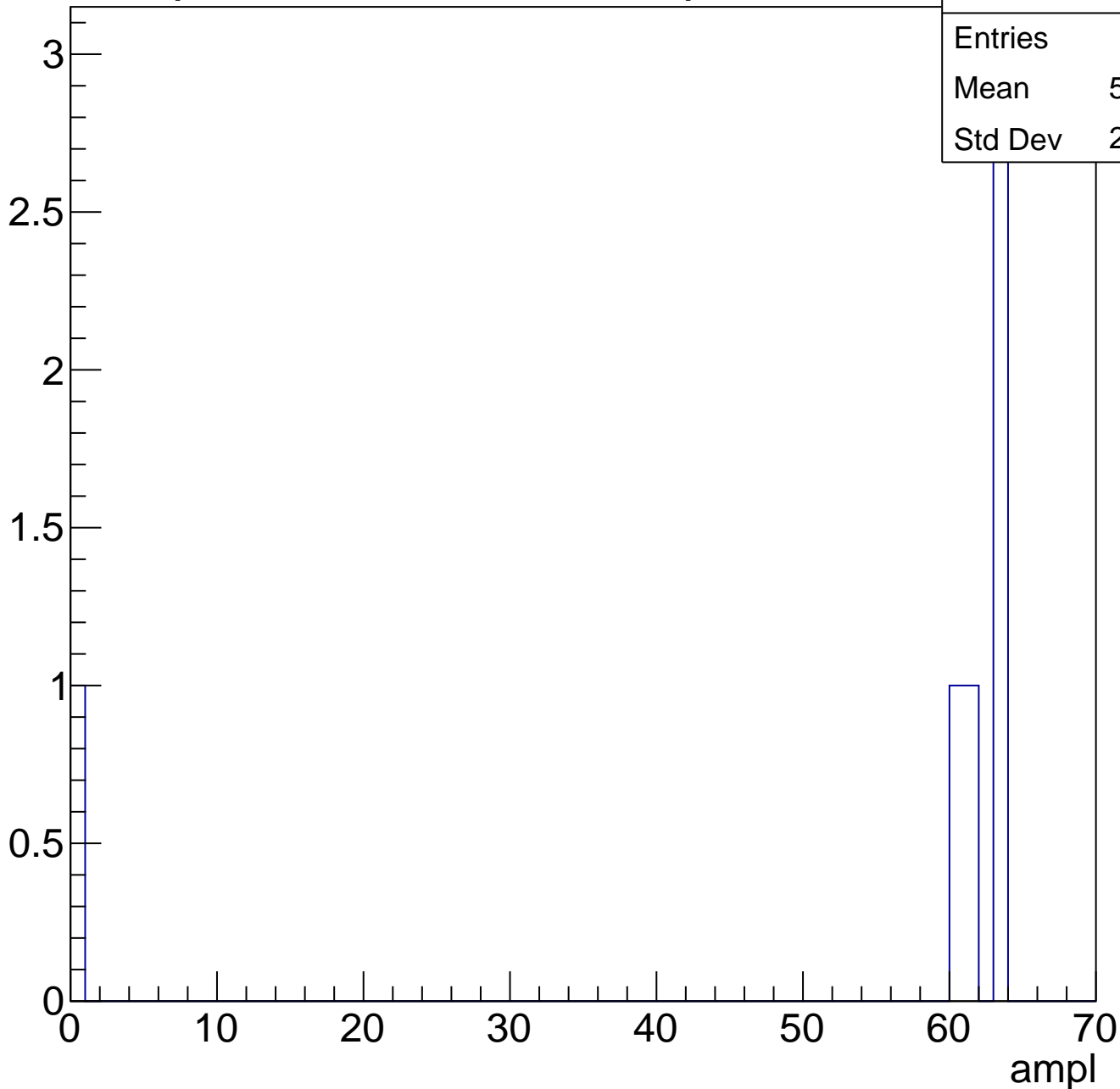
Entries	22
Mean	60.77
Std Dev	1.73



B1L103S, U11-ch111, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	6
Mean	51.67
Std Dev	23.13

B1L103S, U11-ch111, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

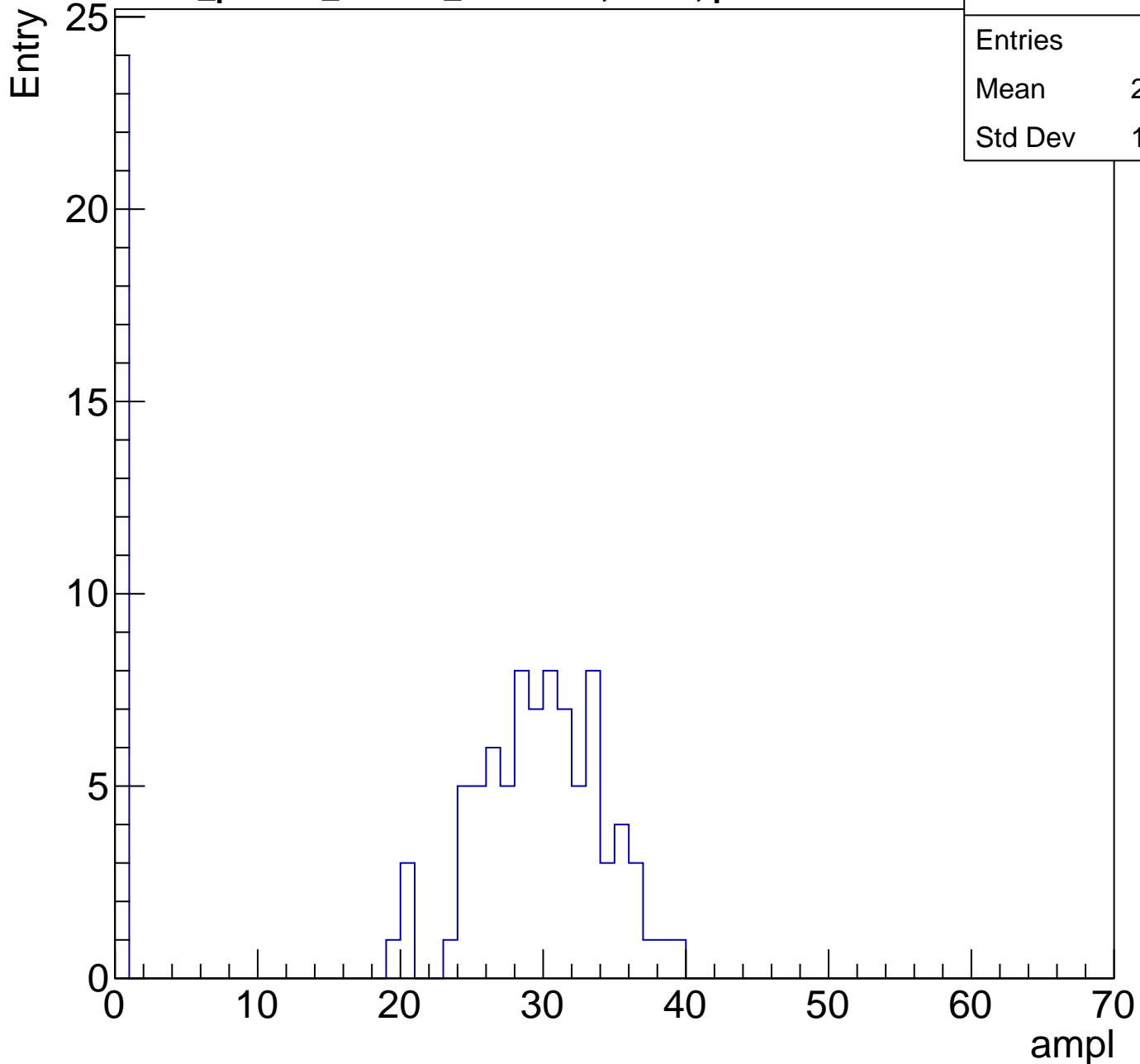
Entry



B1L103S, U11-ch112, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	106
Mean	22.74
Std Dev	12.85

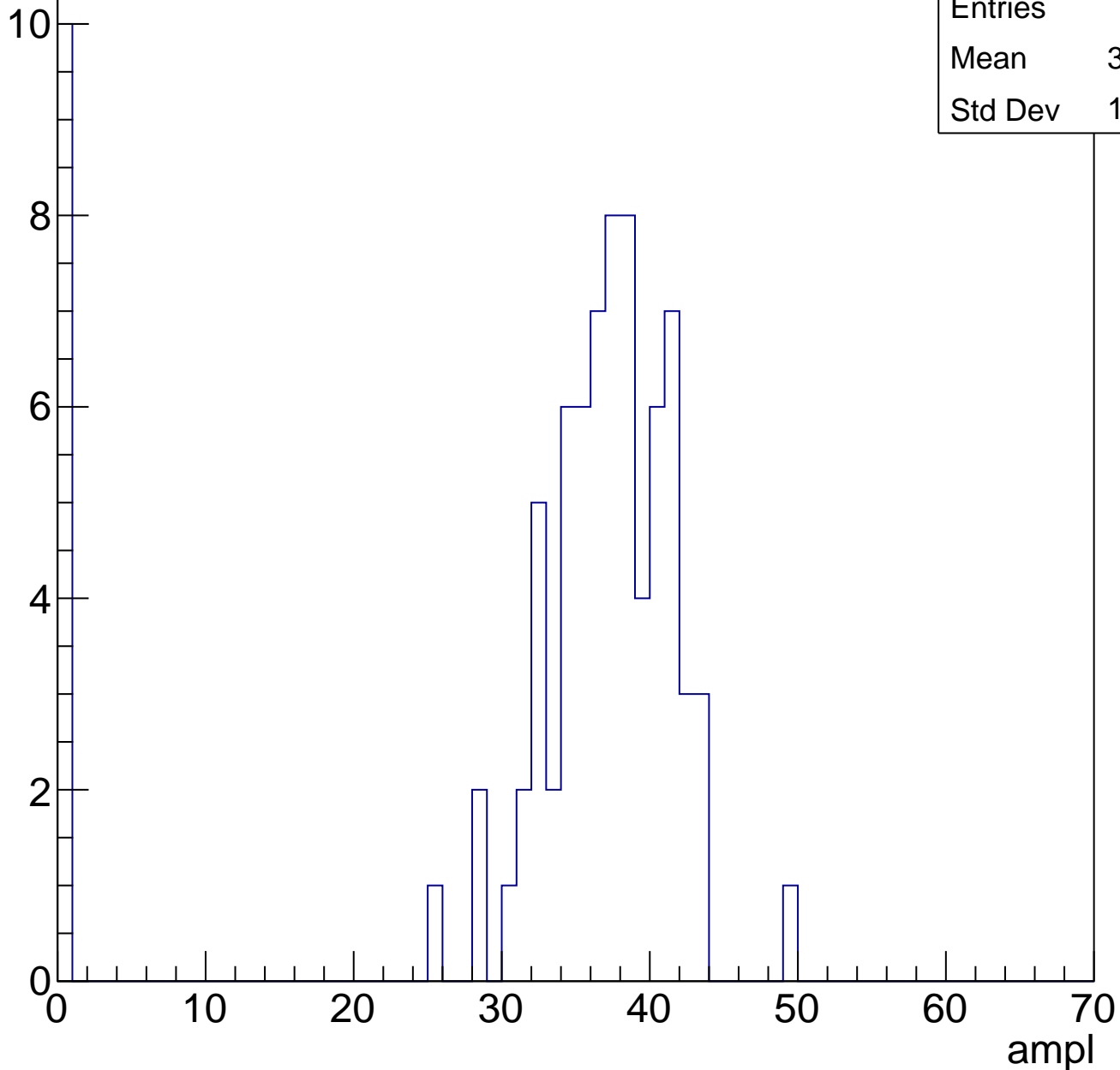


B1L103S, U11-ch112, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	32.34
Std Dev	12.64

Entry

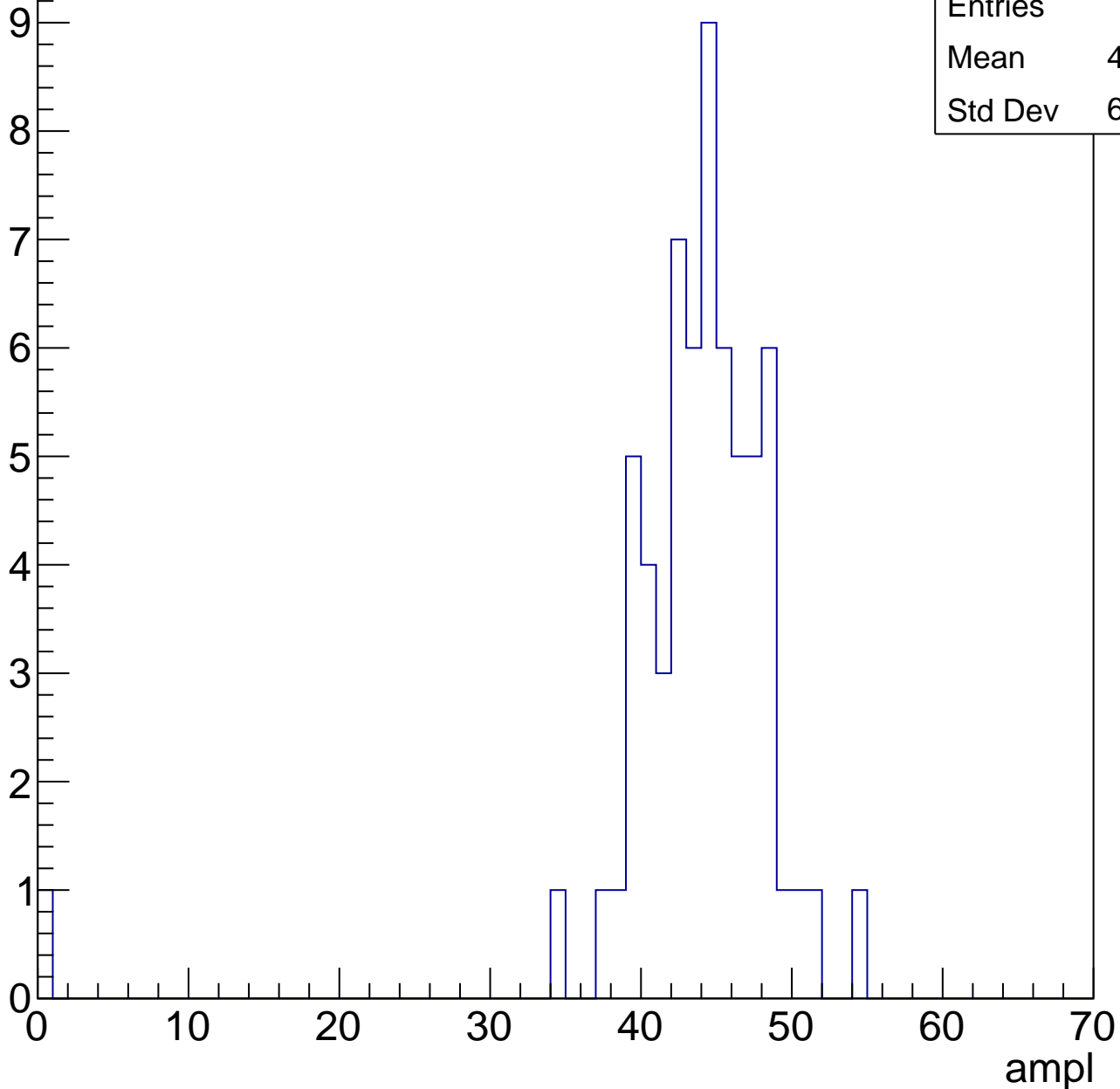


B1L103S, U11-ch112, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	43.16
Std Dev	6.498

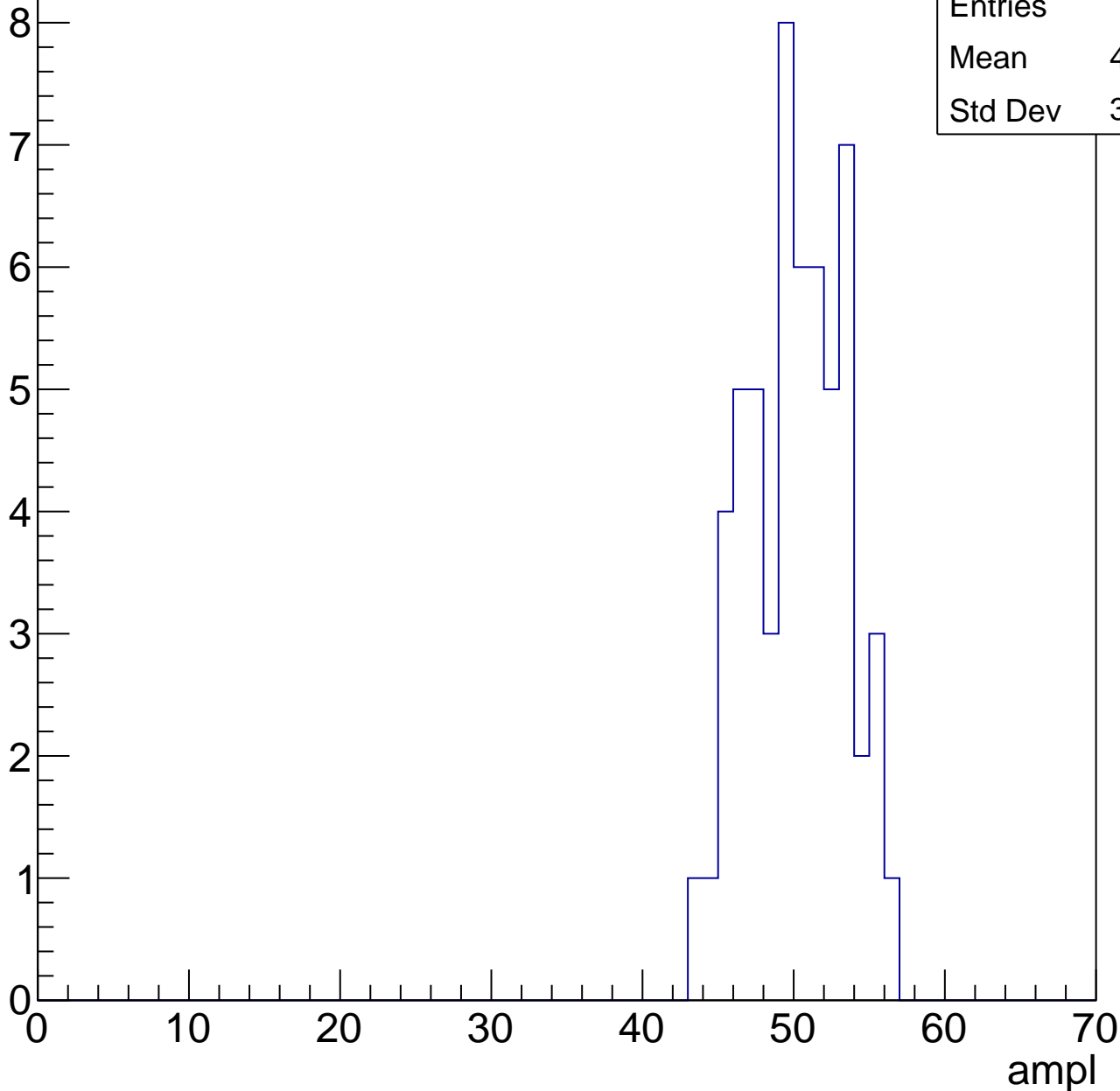


B1L103S, U11-ch112, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	49.72
Std Dev	3.127

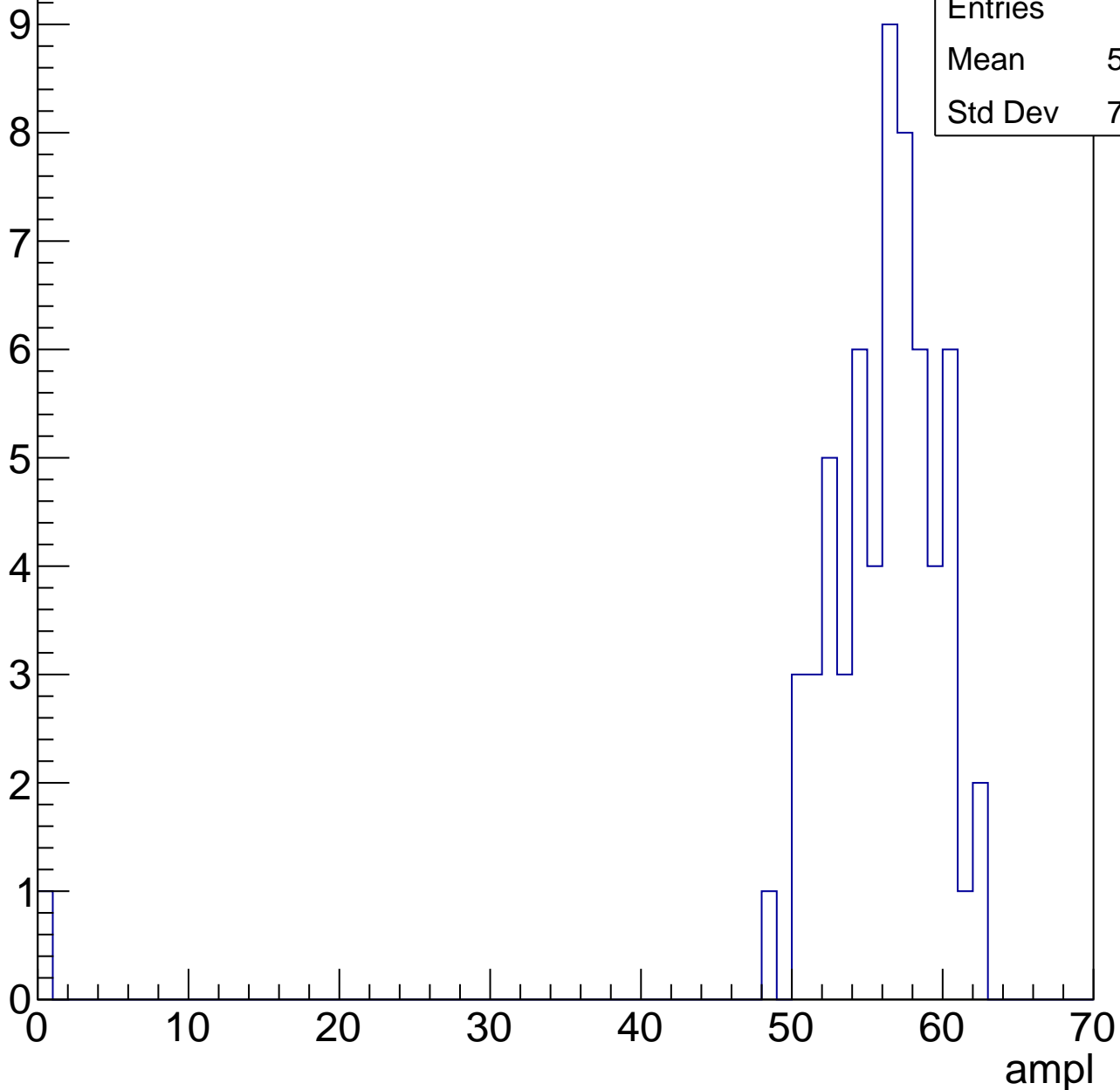


B1L103S, U11-ch112, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	54.89
Std Dev	7.727

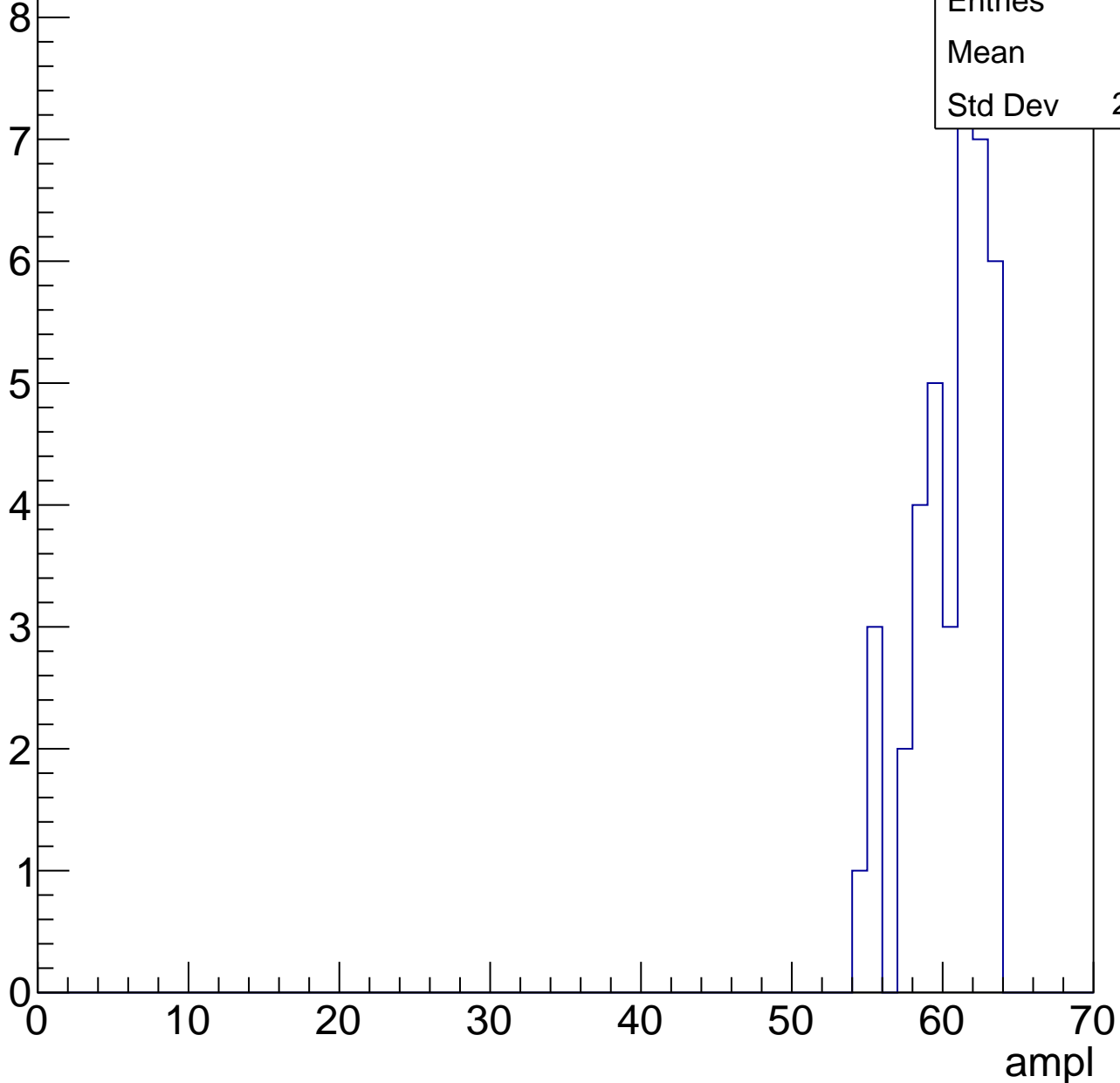


B1L103S, U11-ch112, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

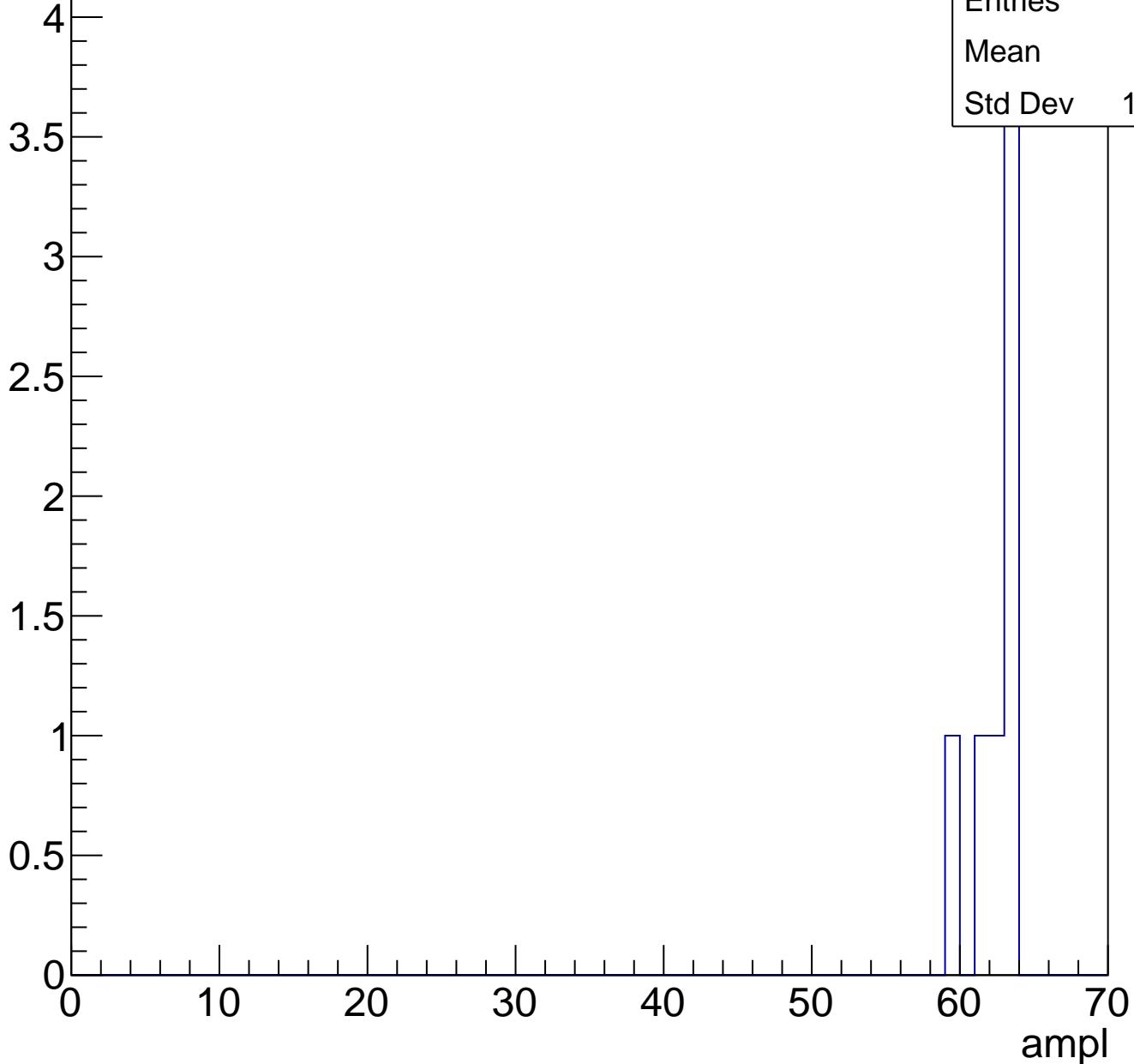
Entries	39
Mean	60
Std Dev	2.481



B1L103S, U11-ch112, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch112, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3
Std Dev	13.08

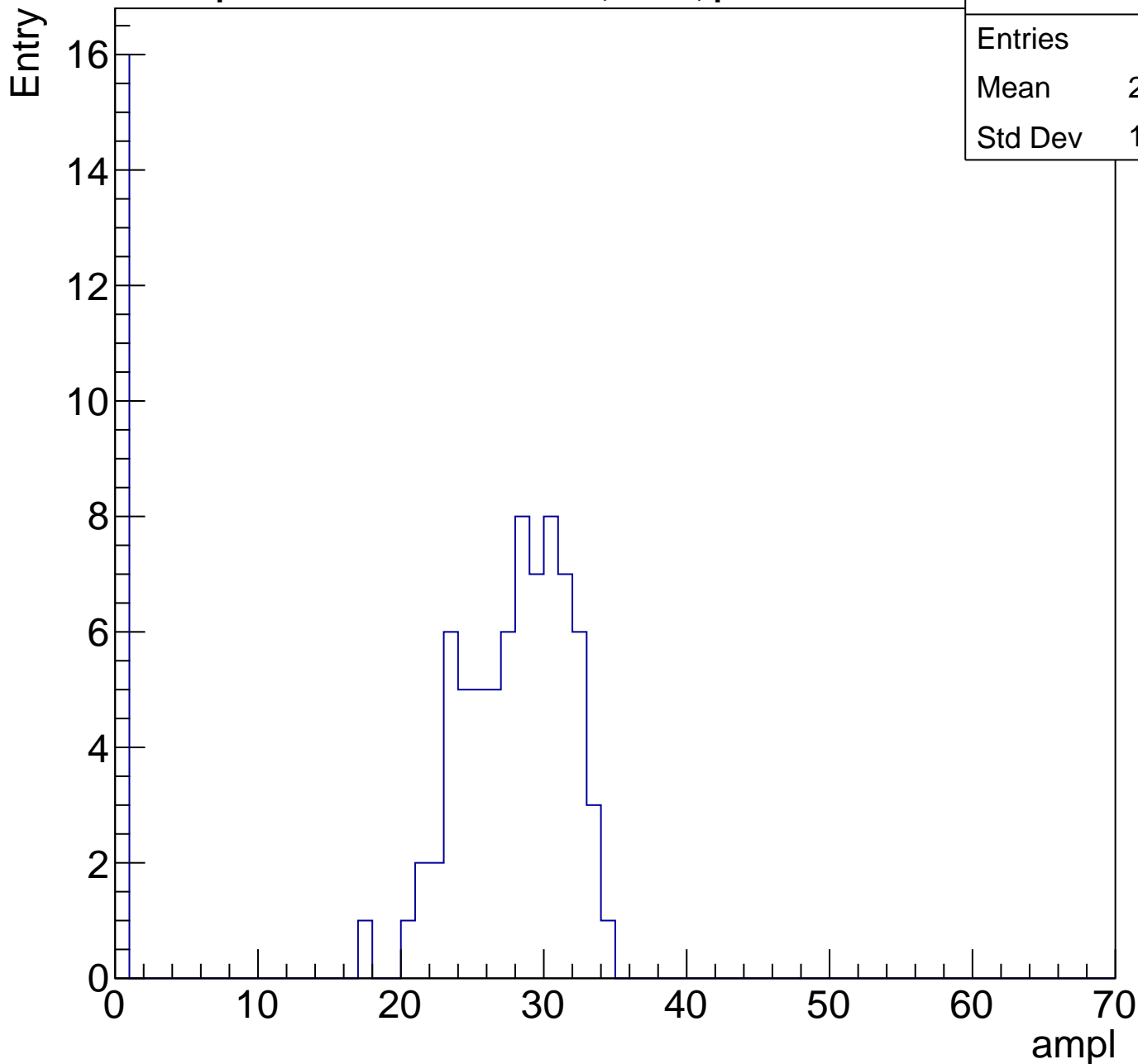
Entry



B1L103S, U11-ch113, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	22.55
Std Dev	11.05

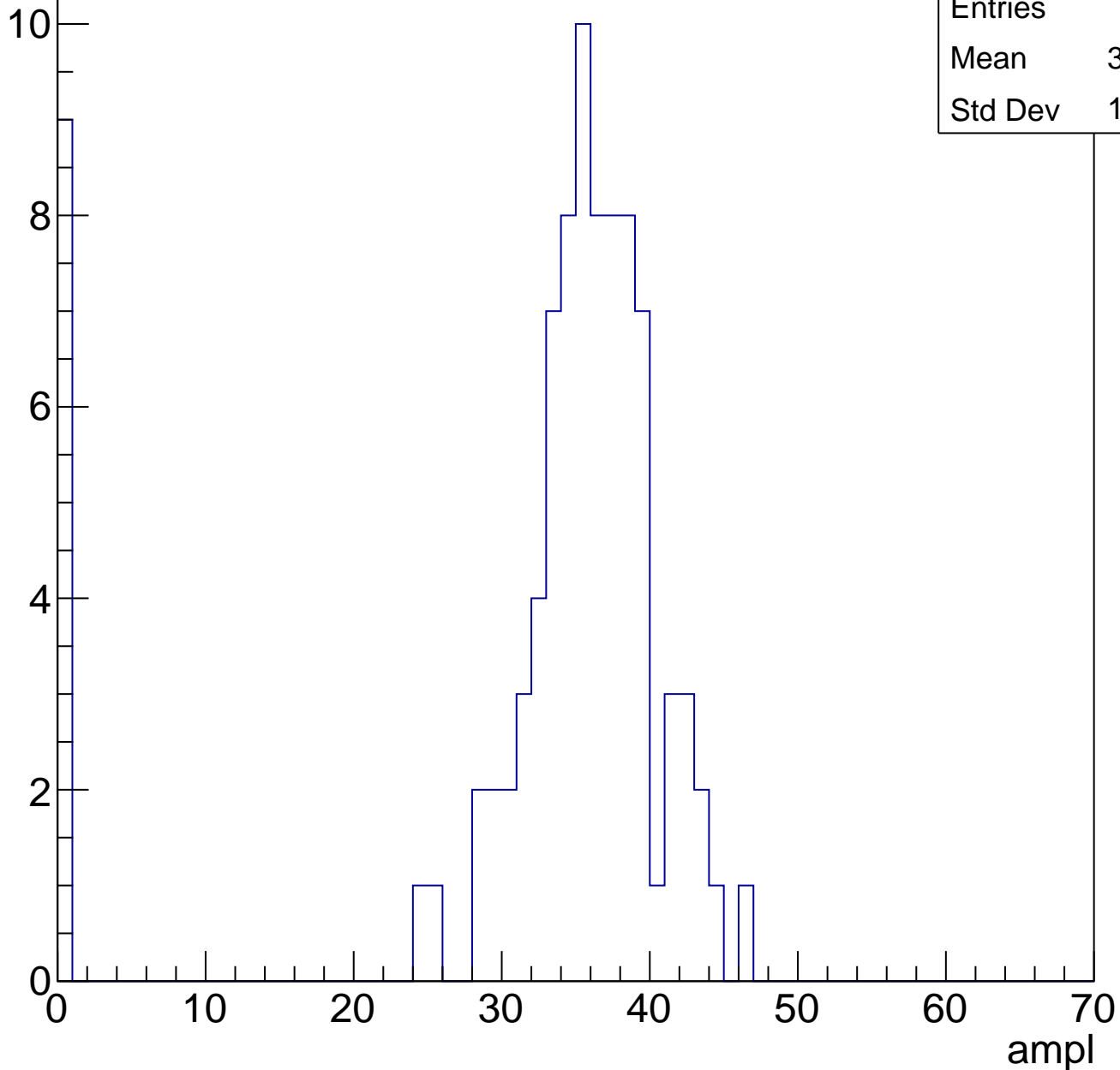


B1L103S, U11-ch113, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	91
Mean	32.12
Std Dev	11.32

Entry

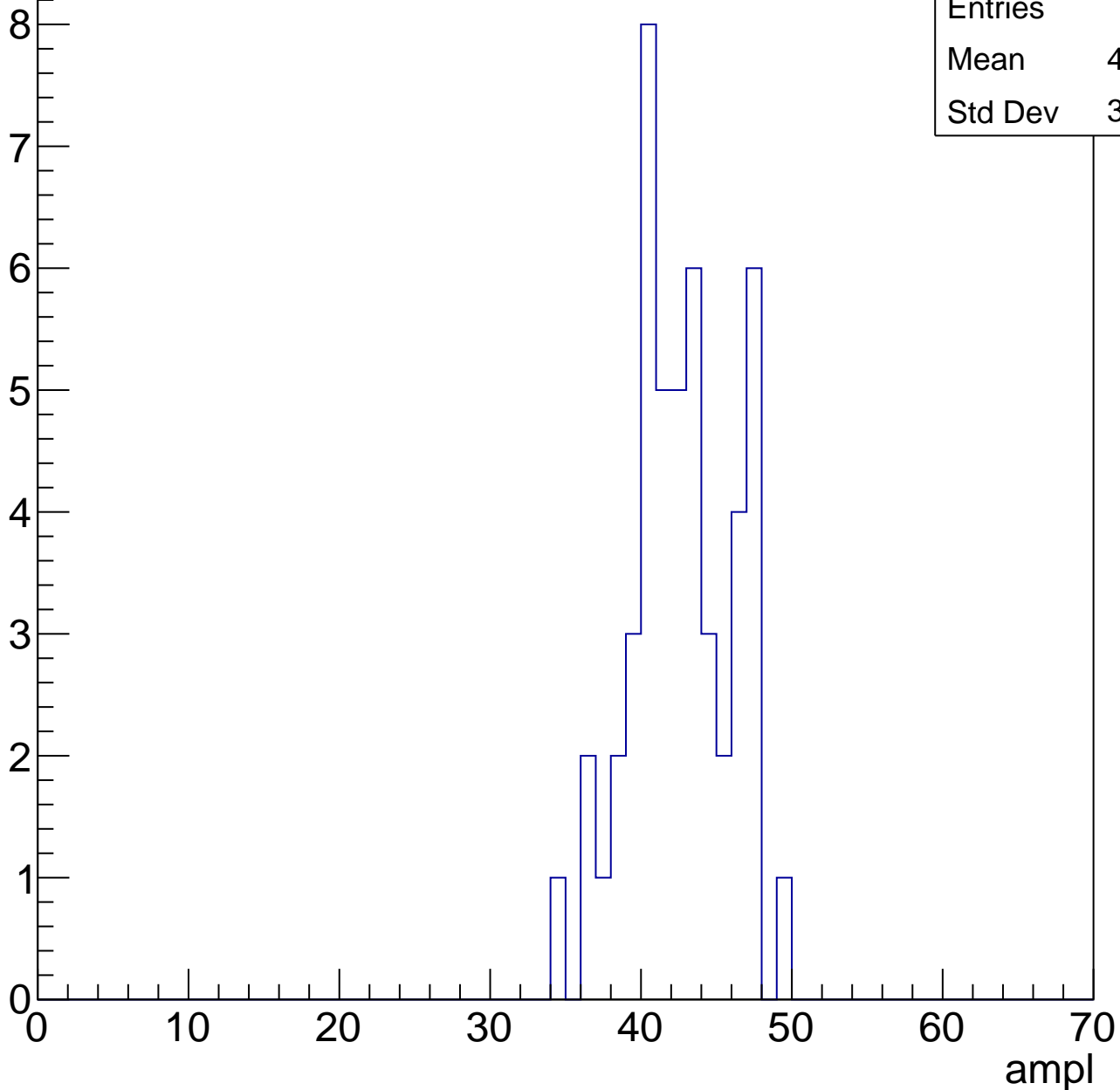


B1L103S, U11-ch113, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	42.16
Std Dev	3.365

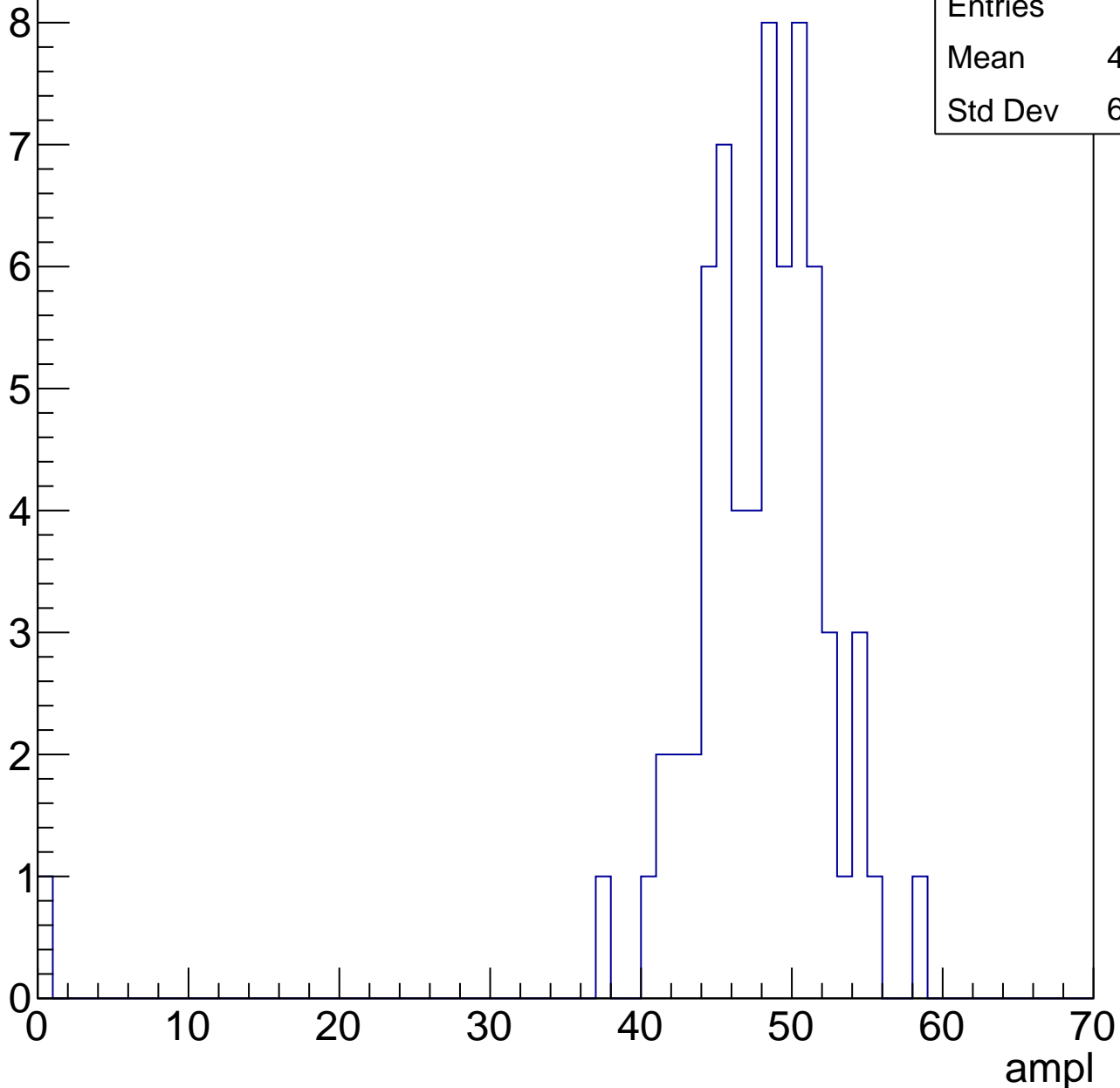


B1L103S, U11-ch113, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	46.99
Std Dev	6.955

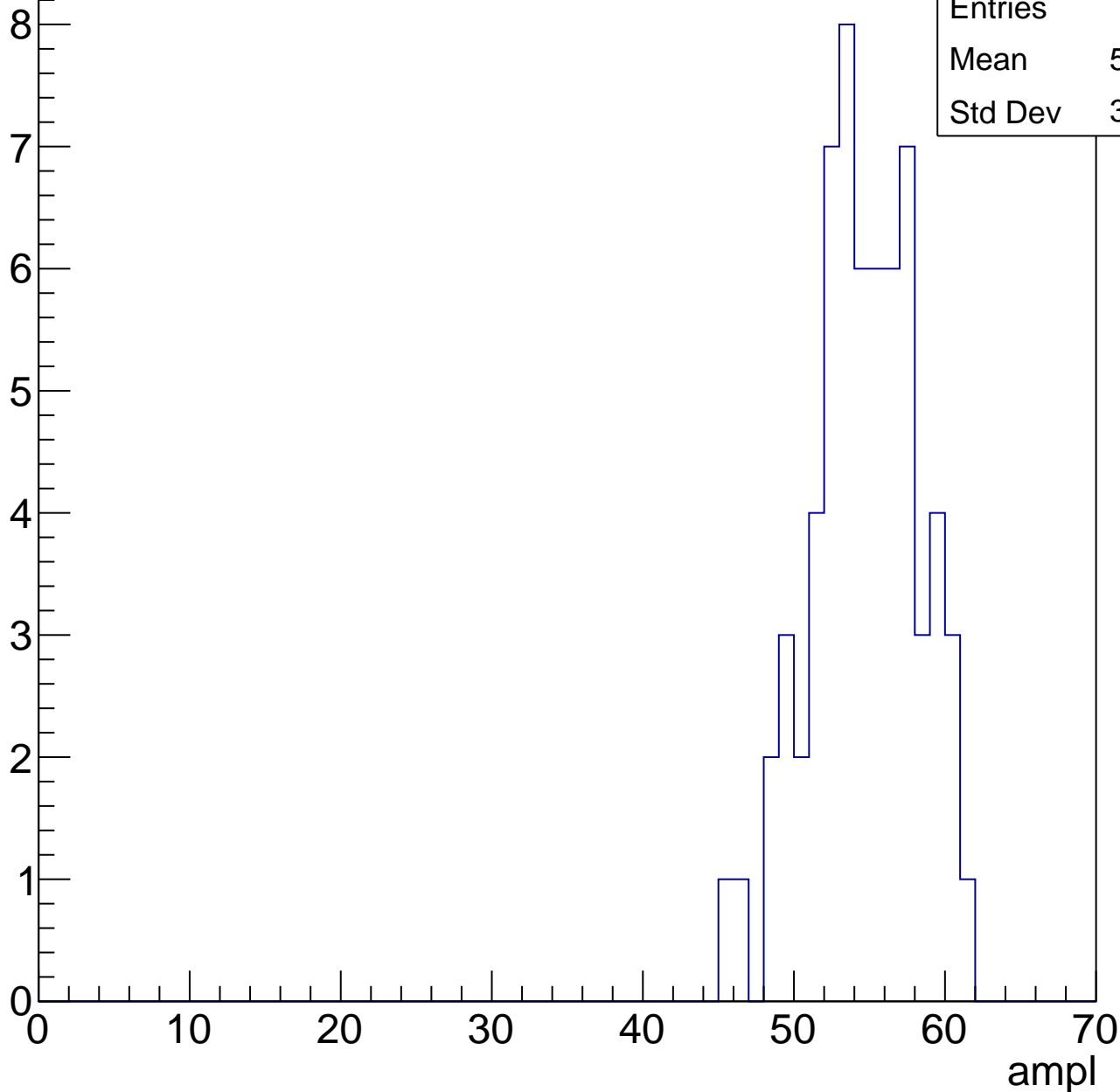


B1L103S, U11-ch113, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	54.16
Std Dev	3.519

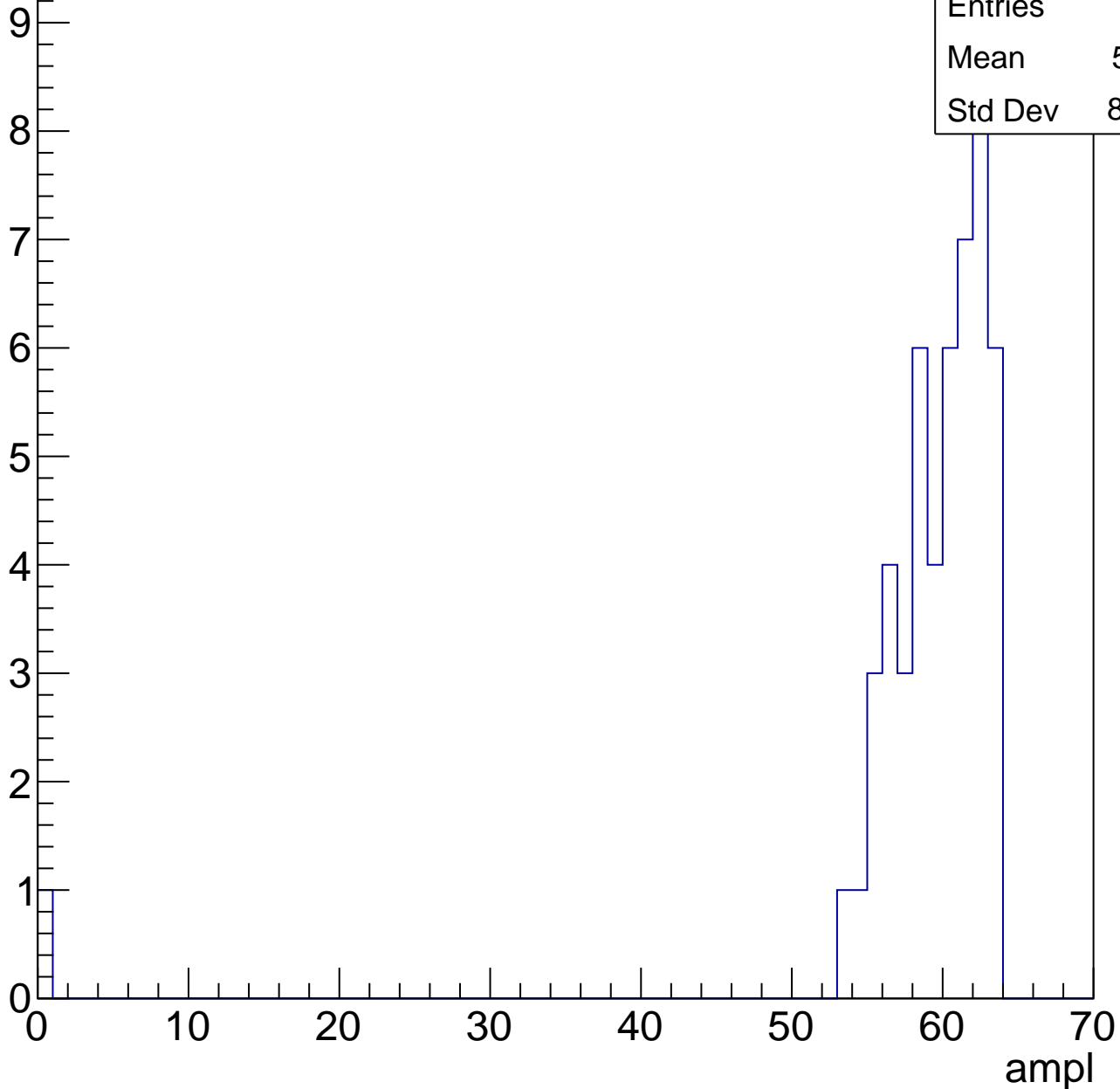


B1L103S, U11-ch113, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

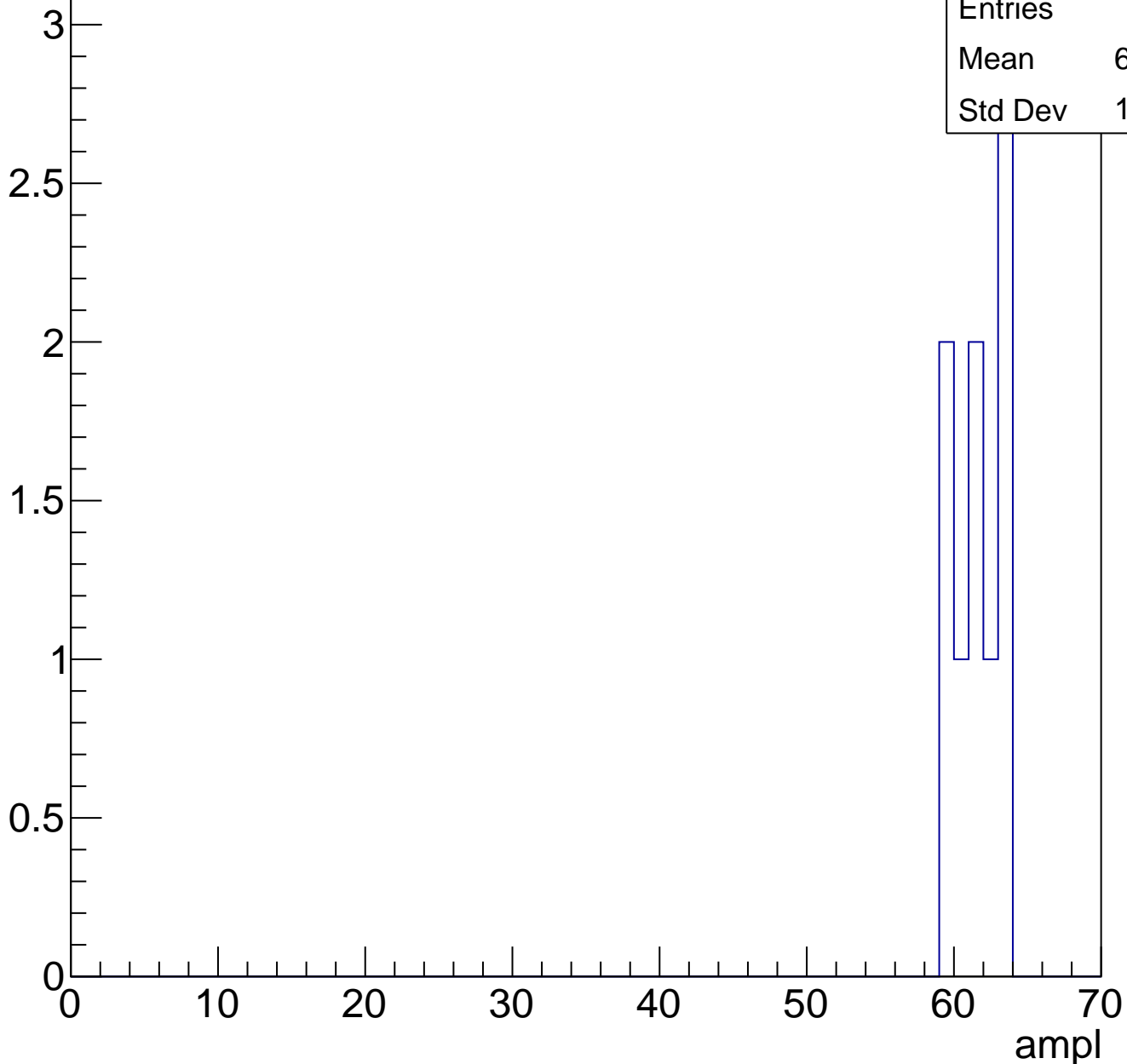
Entries	51
Mean	58.31
Std Dev	8.667



B1L103S, U11-ch113, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	9
Mean	61.22
Std Dev	1.548

B1L103S, U11-ch113, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

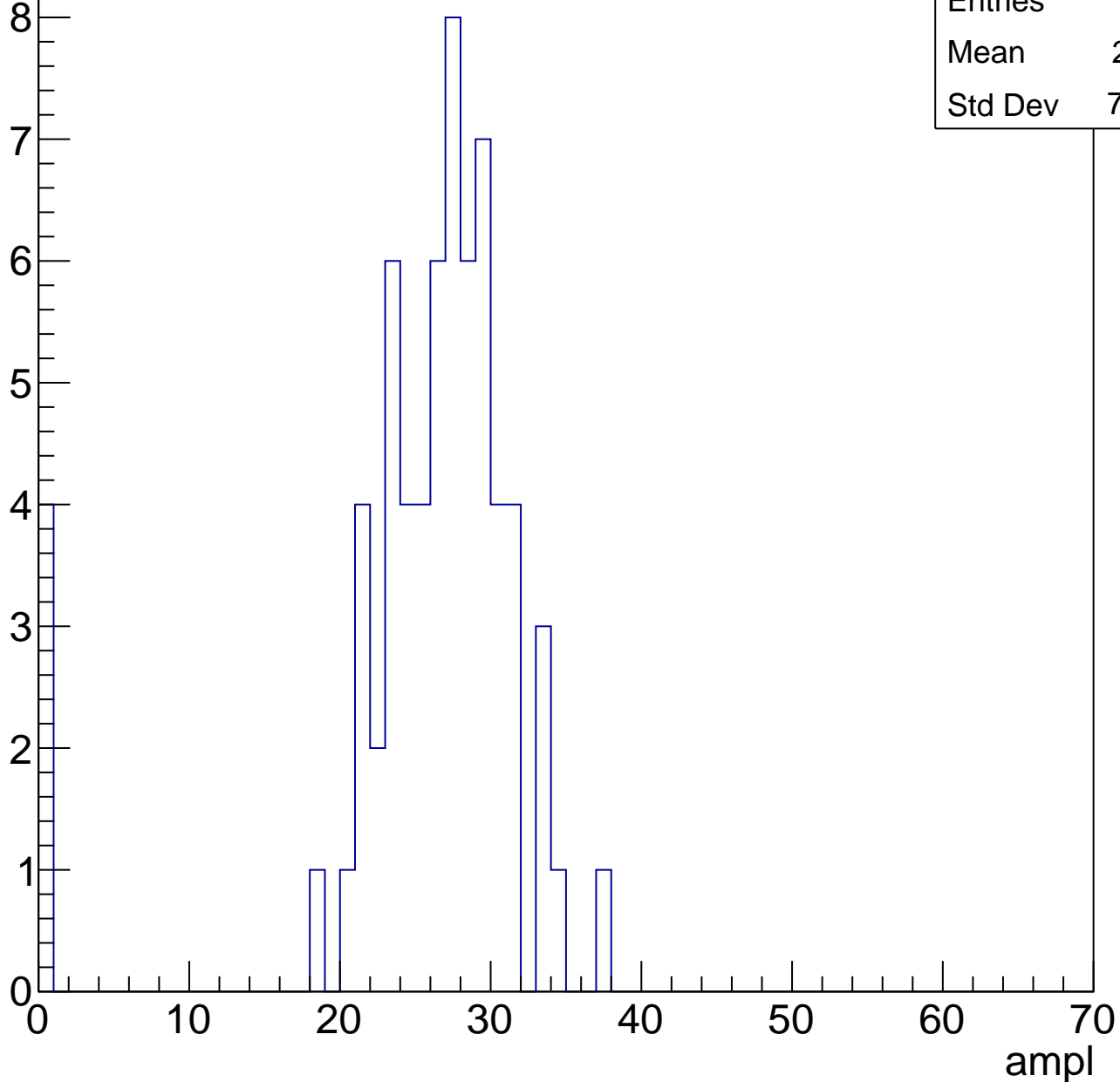


B1L103S, U11-ch114, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

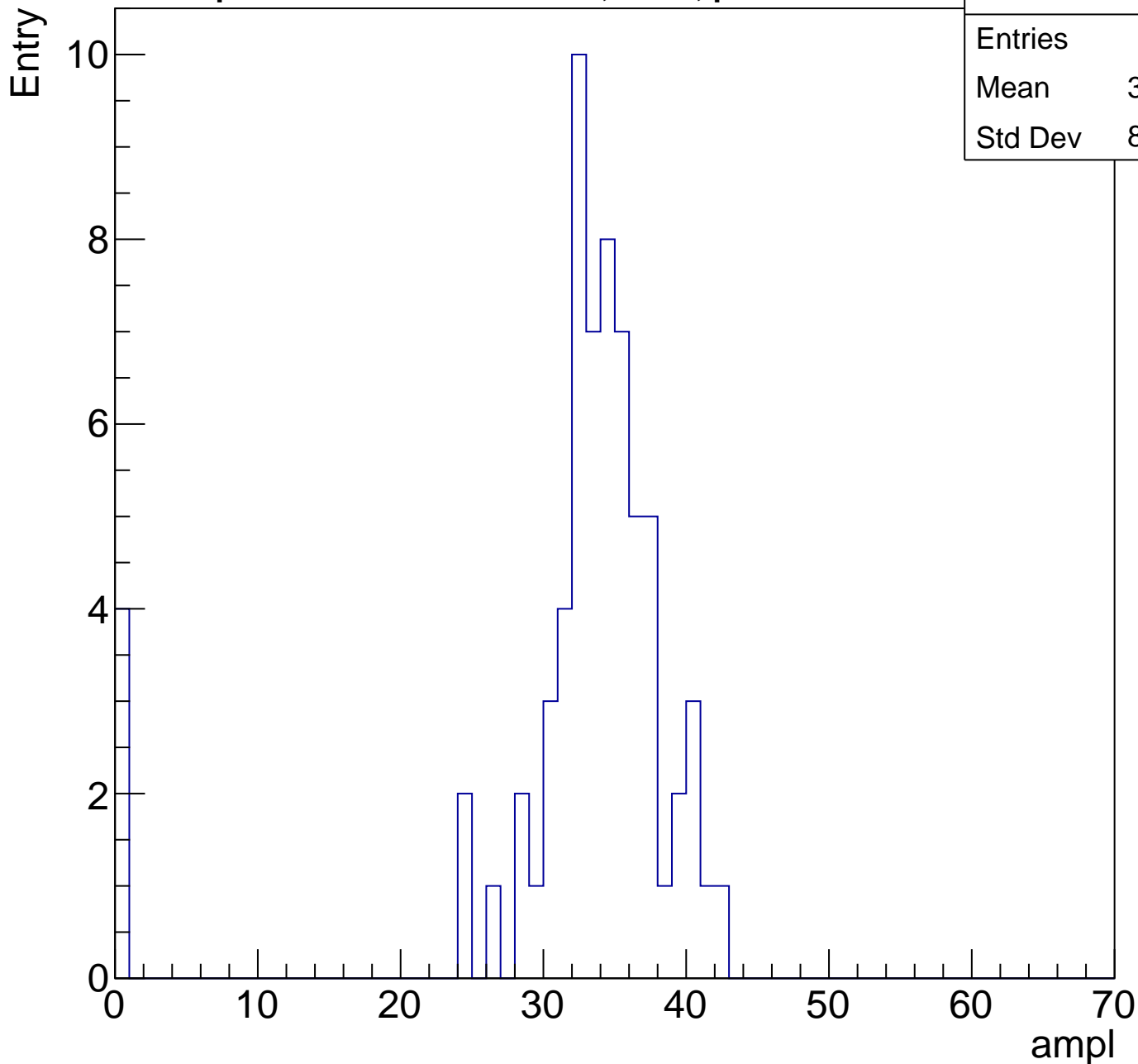
Entries	66
Mean	25.11
Std Dev	7.332



B1L103S, U11-ch114, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	67
Mean	31.72
Std Dev	8.747

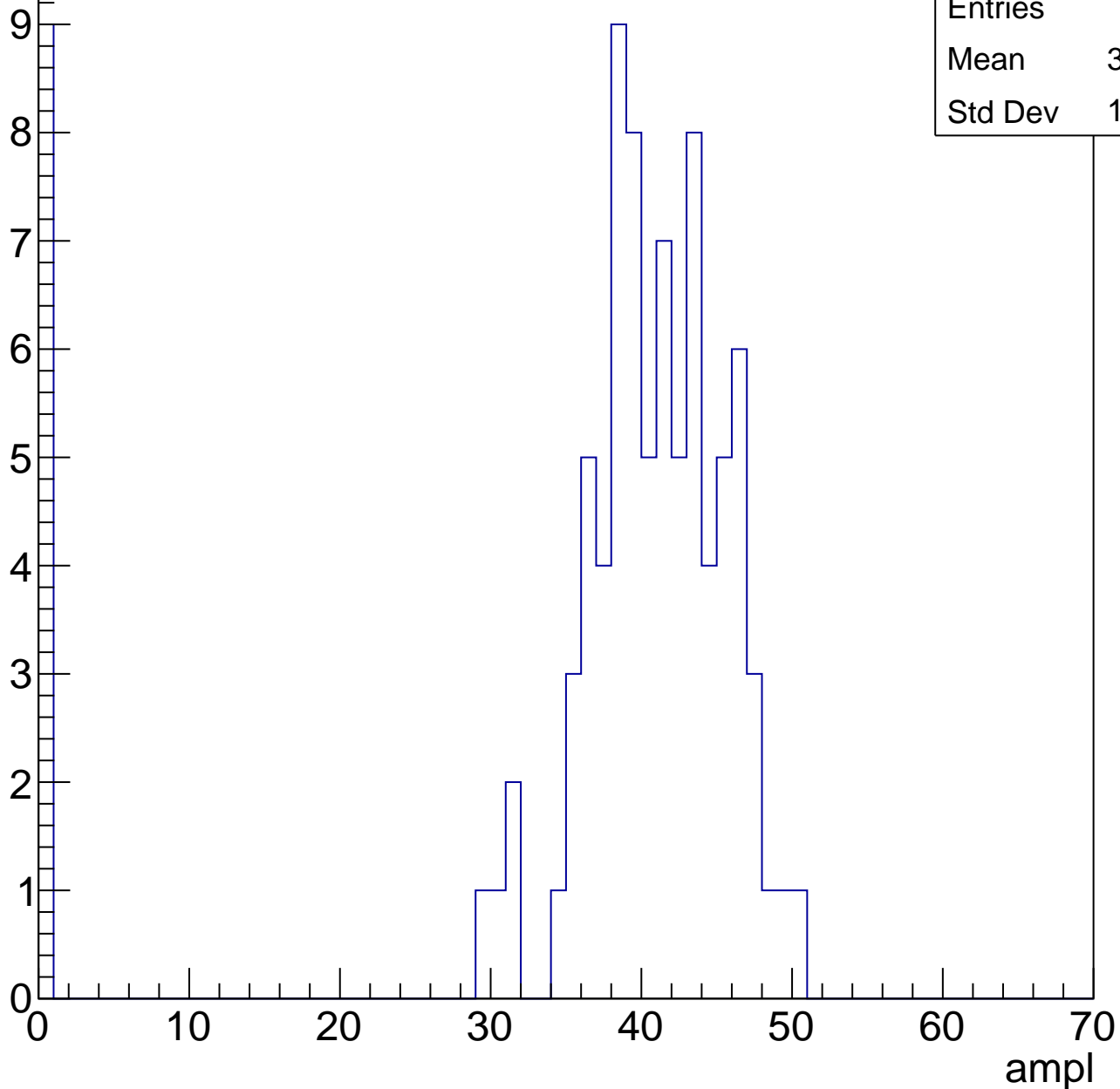


B1L103S, U11-ch114, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	89
Mean	36.49
Std Dev	12.92

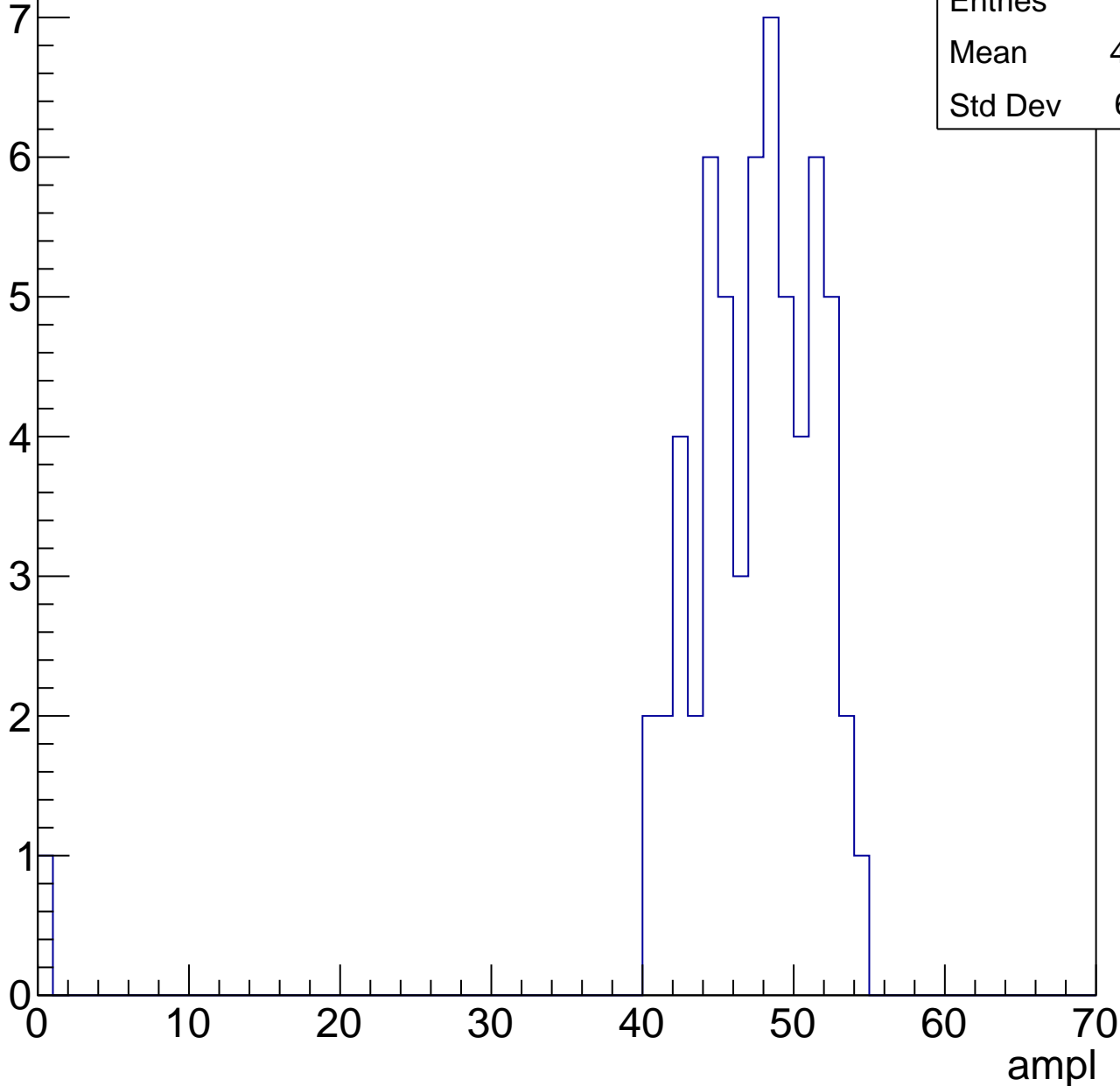


B1L103S, U11-ch114, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	46.43
Std Dev	6.981

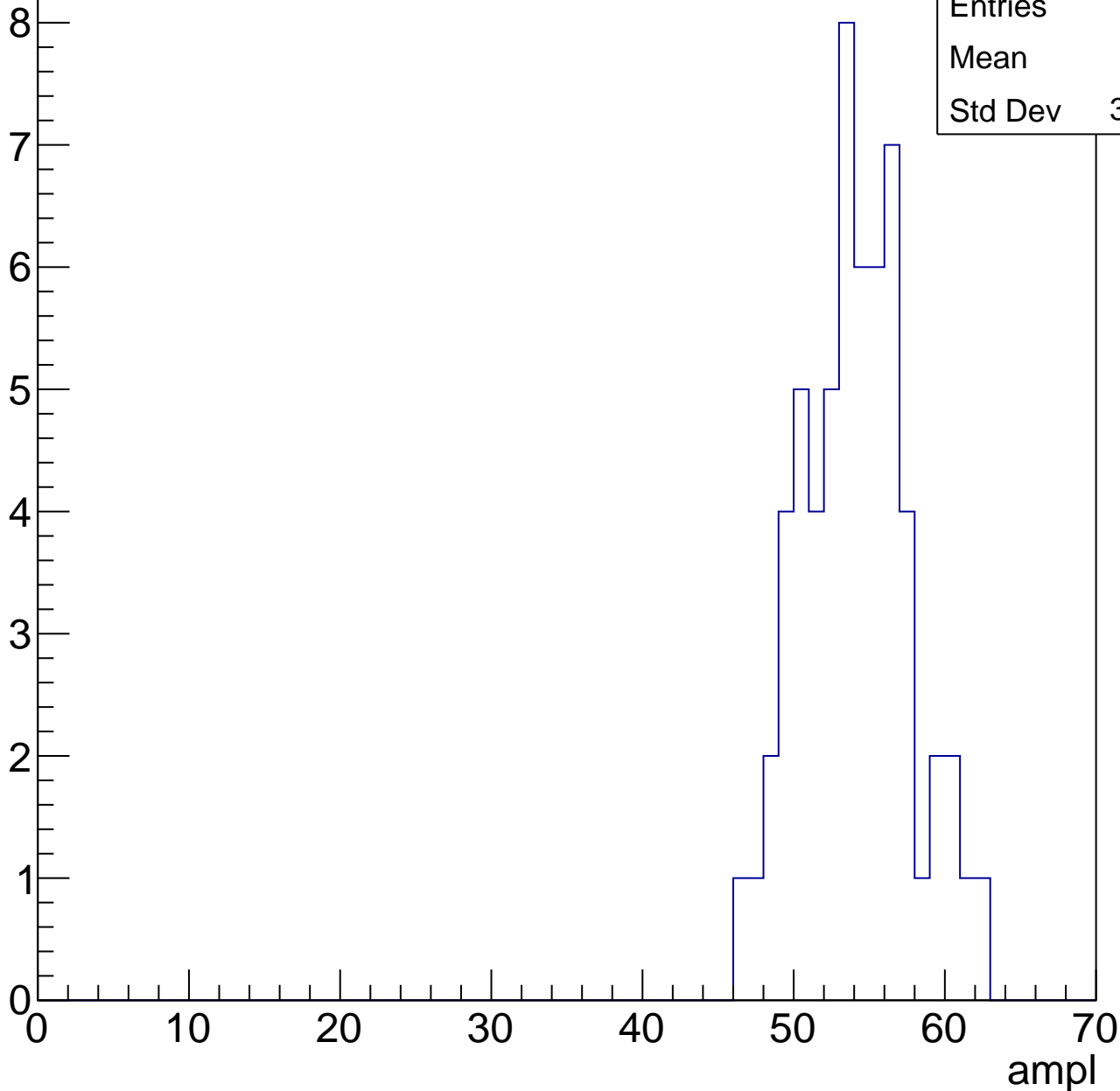


B1L103S, U11-ch114, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	53.6
Std Dev	3.513

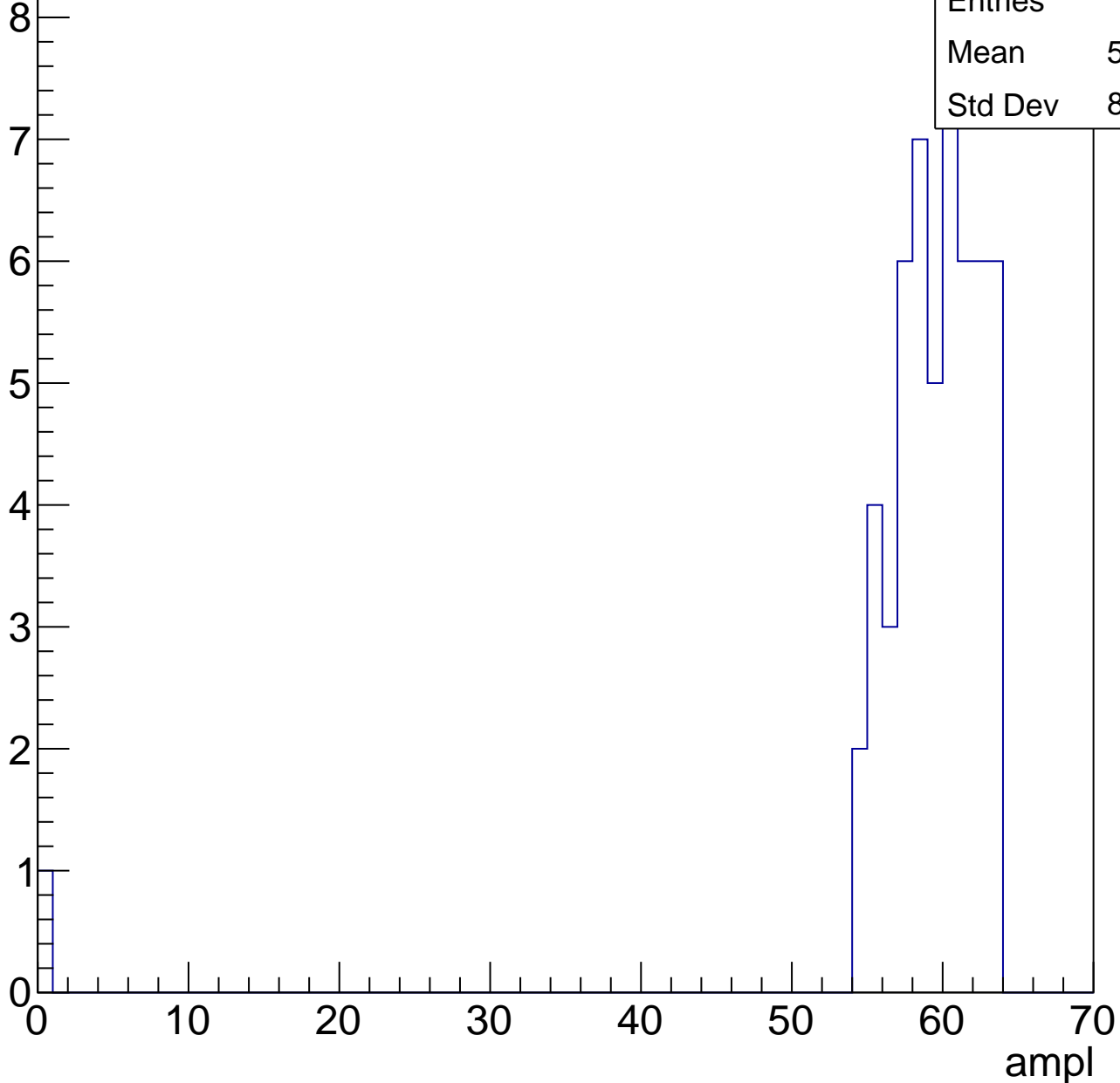


B1L103S, U11-ch114, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

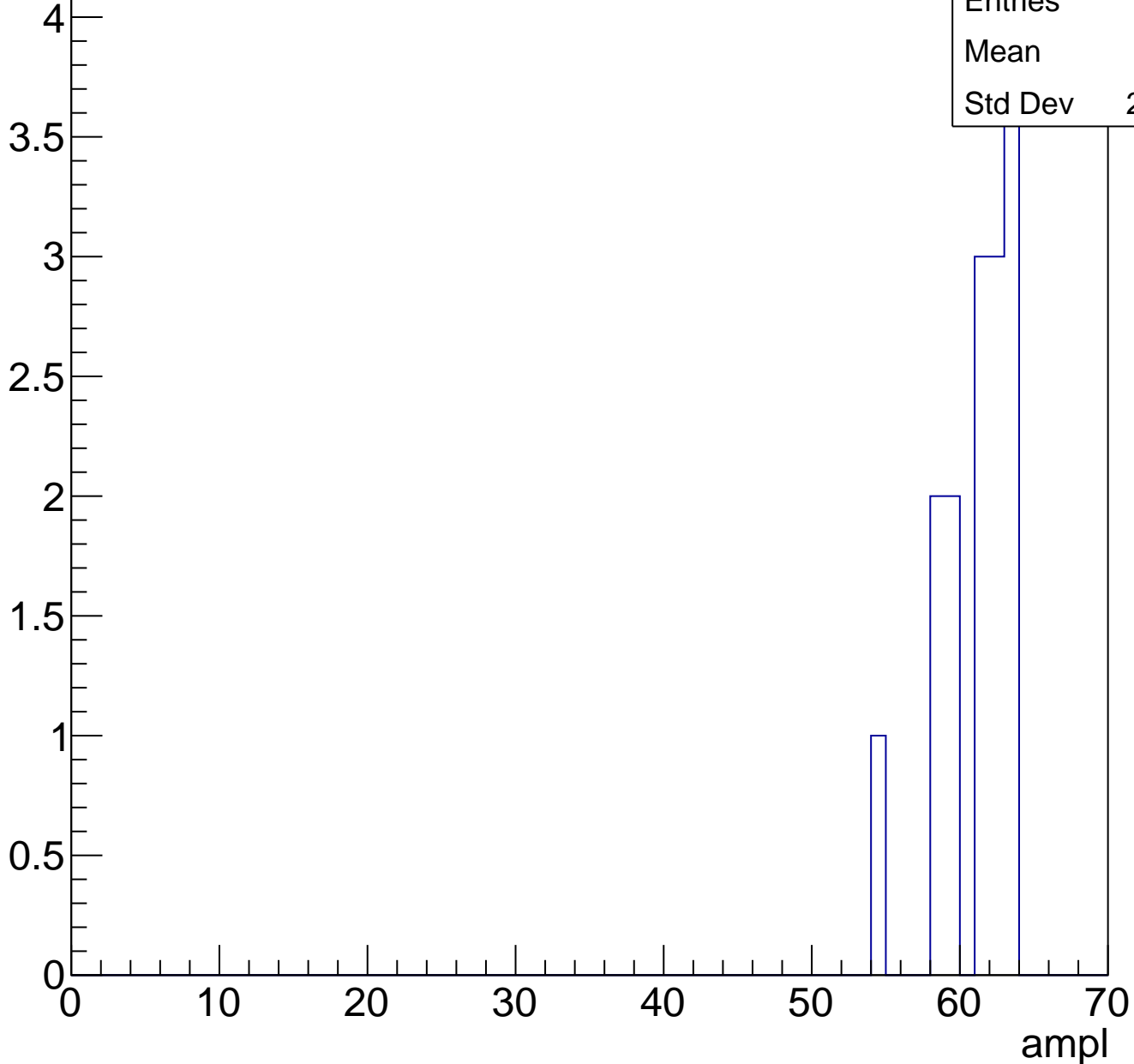
Entries	54
Mean	58.06
Std Dev	8.374



B1L103S, U11-ch114, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

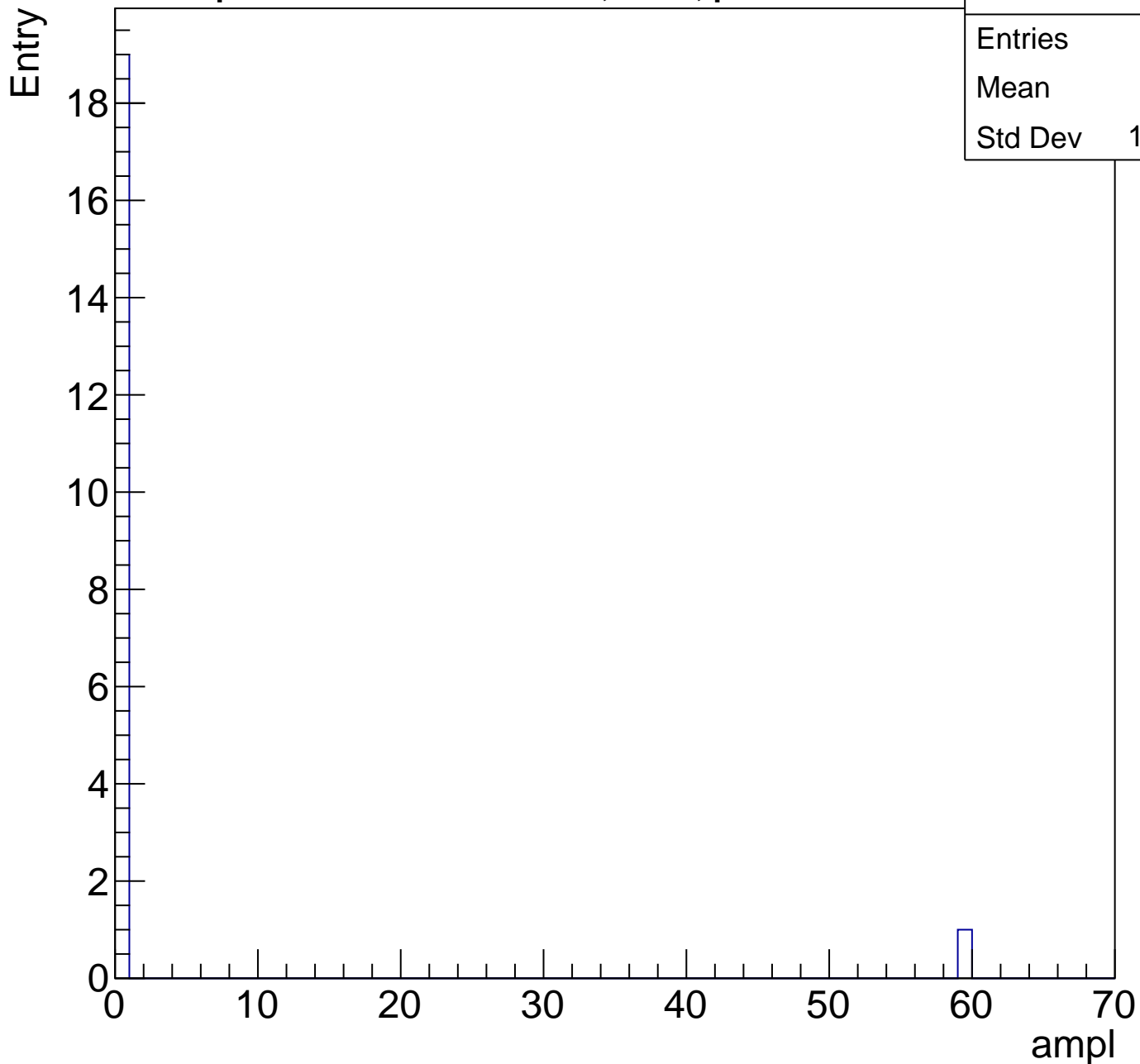


Entries	15
Mean	60.6
Std Dev	2.471

B1L103S, U11-ch114, adc7

calib_packv5_041523_1651.root, FC#0, port C2

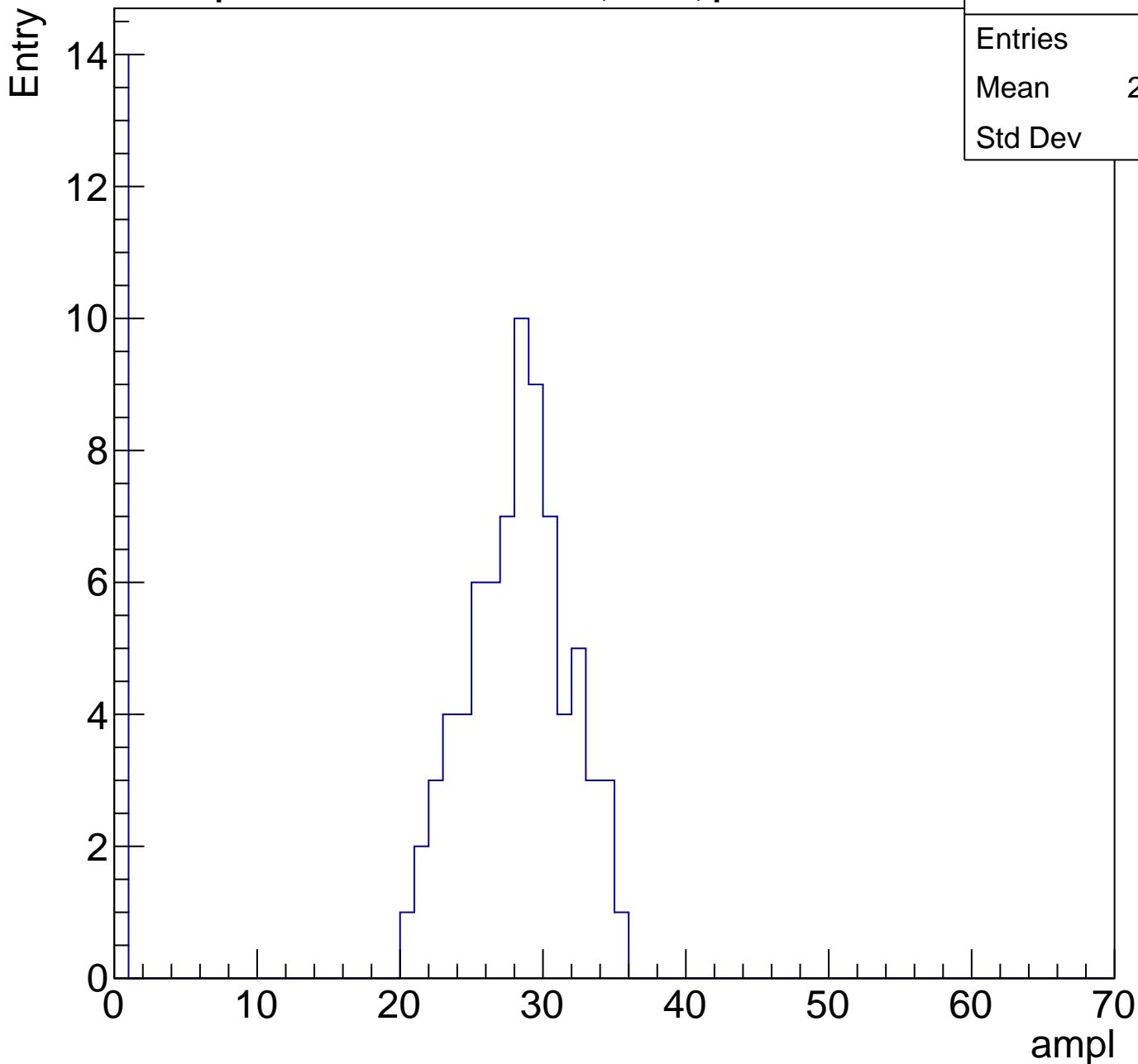
Entries	20
Mean	2.95
Std Dev	12.86



B1L103S, U11-ch115, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	23.39
Std Dev	10.6

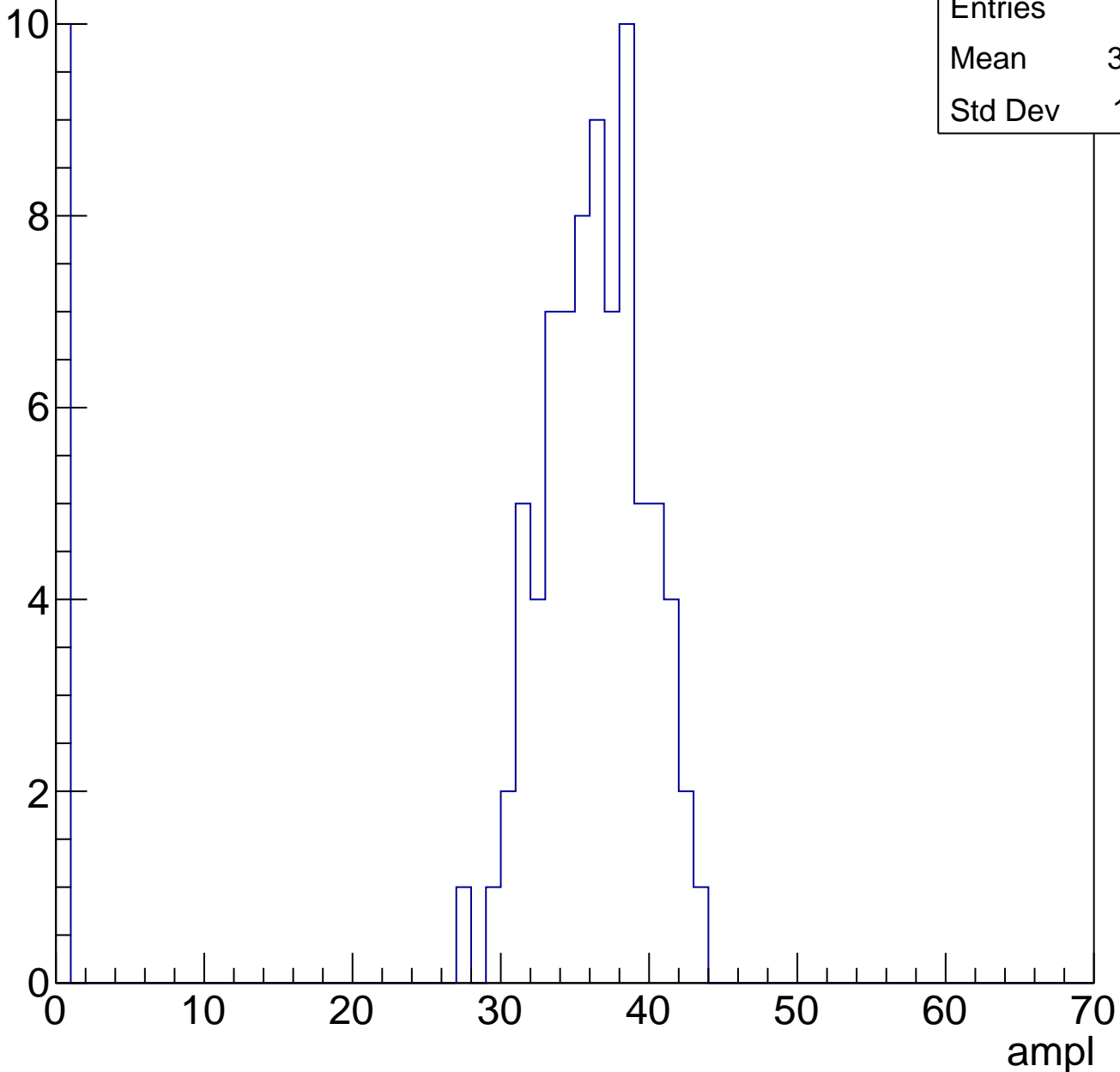


B1L103S, U11-ch115, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	88
Mean	31.78
Std Dev	11.81

Entry

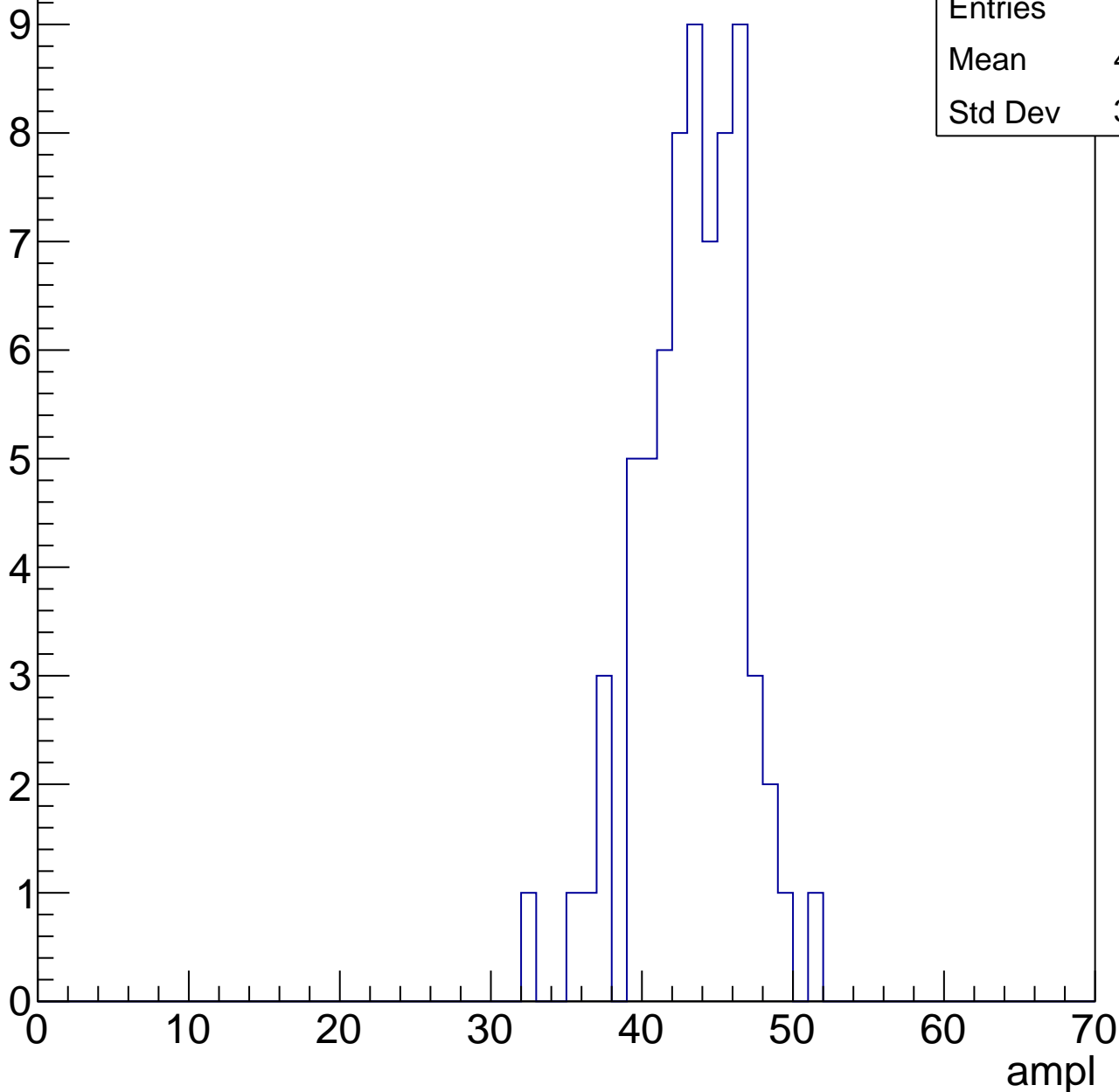


B1L103S, U11-ch115, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	42.81
Std Dev	3.411

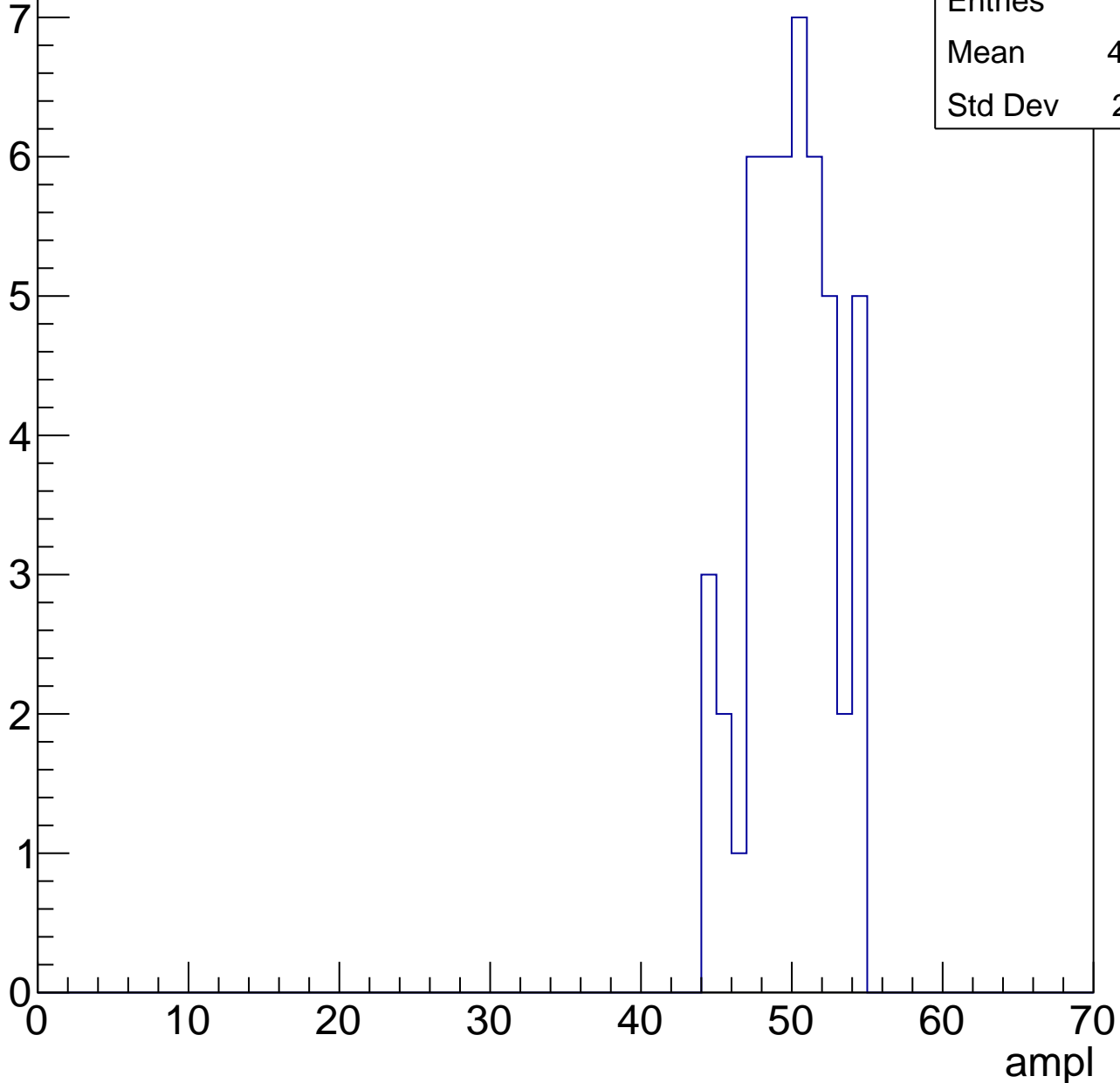


B1L103S, U11-ch115, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	49.47
Std Dev	2.741

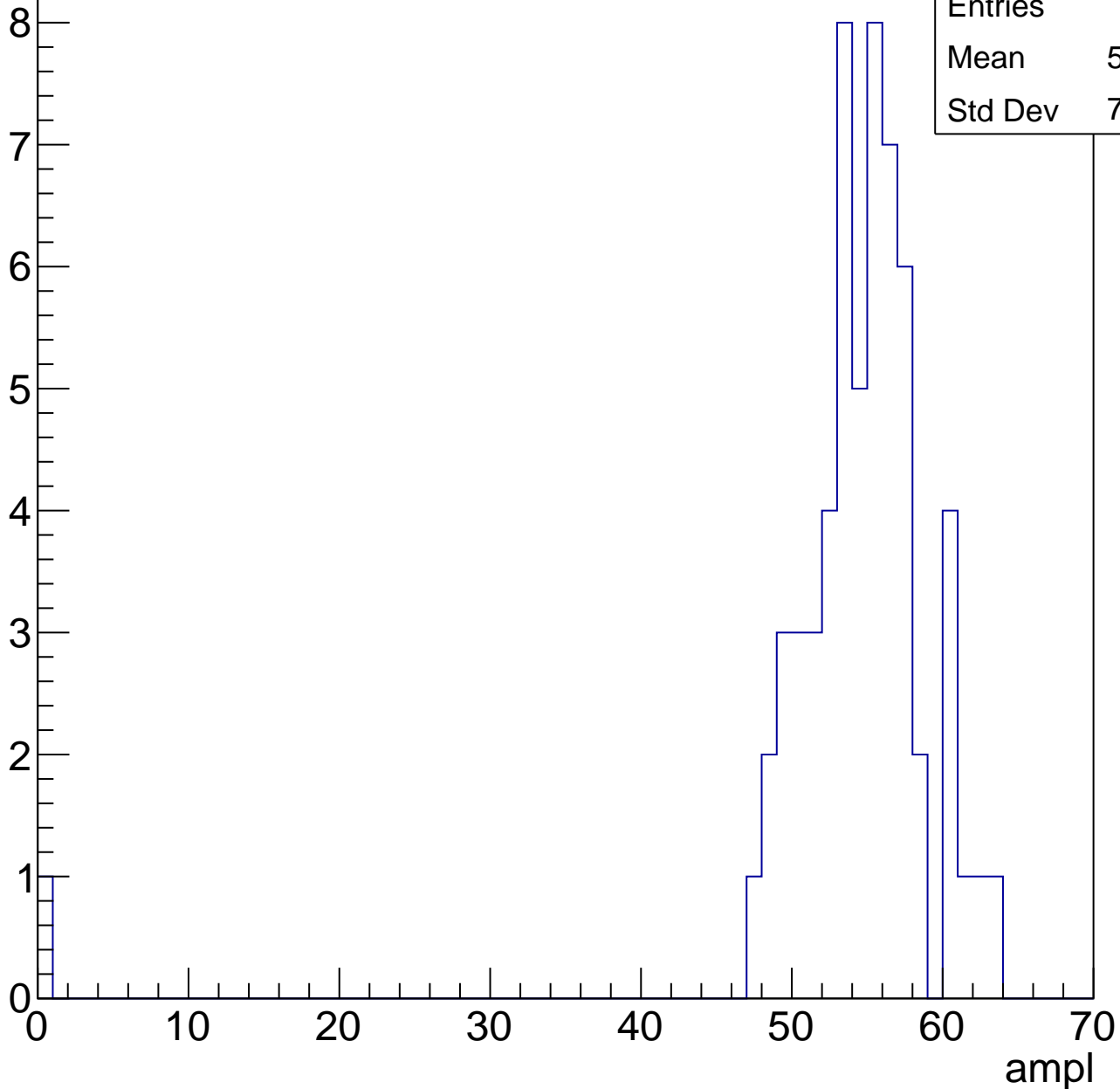


B1L103S, U11-ch115, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	53.52
Std Dev	7.807



B1L103S, U11-ch115, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	59.4
Std Dev	2.374

10

8

6

4

2

0

ampl

0

10

20

30

40

50

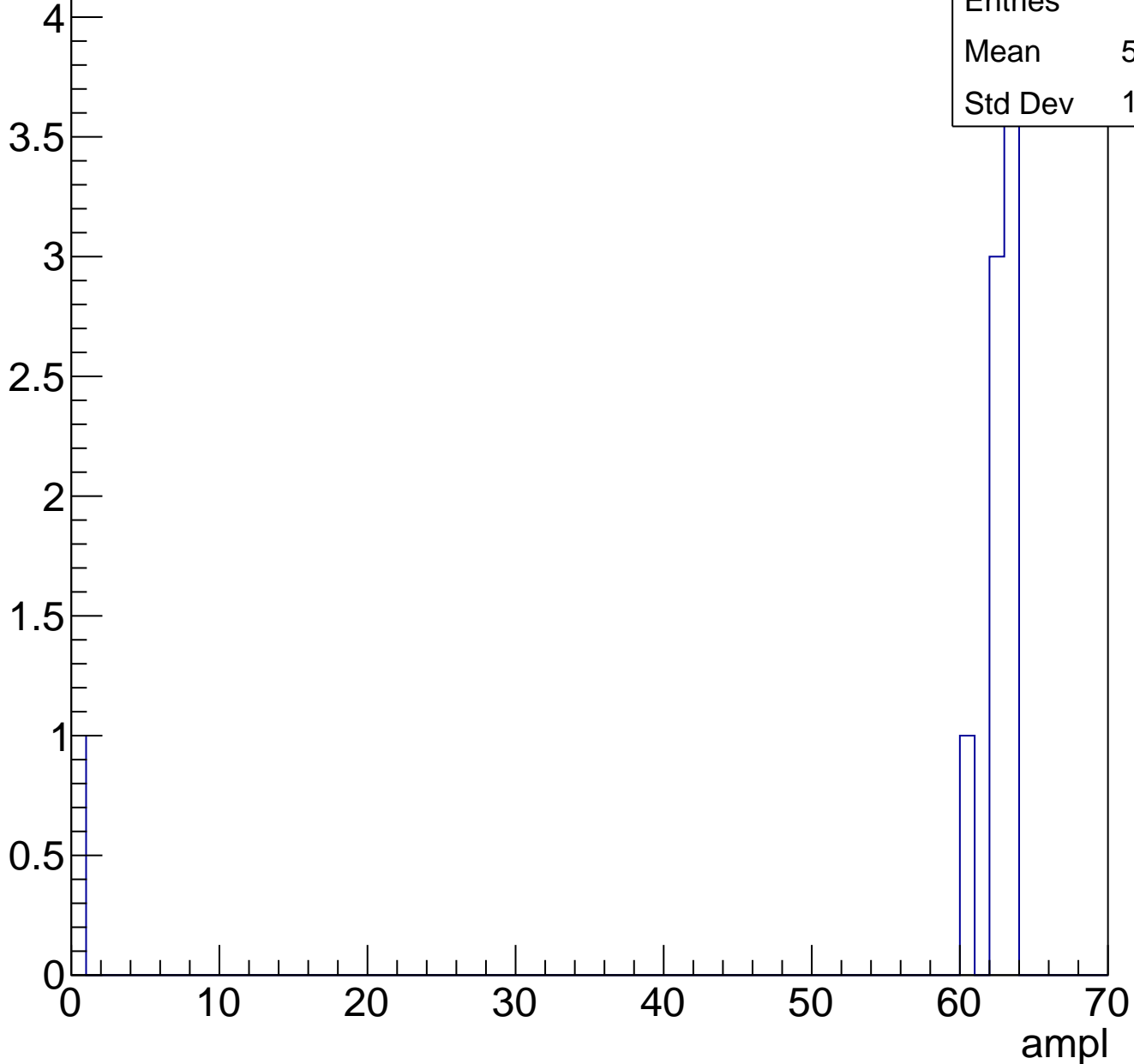
60

70

B1L103S, U11-ch115, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch115, adc7

calib_packv5_041523_1651.root, FC#0, port C2

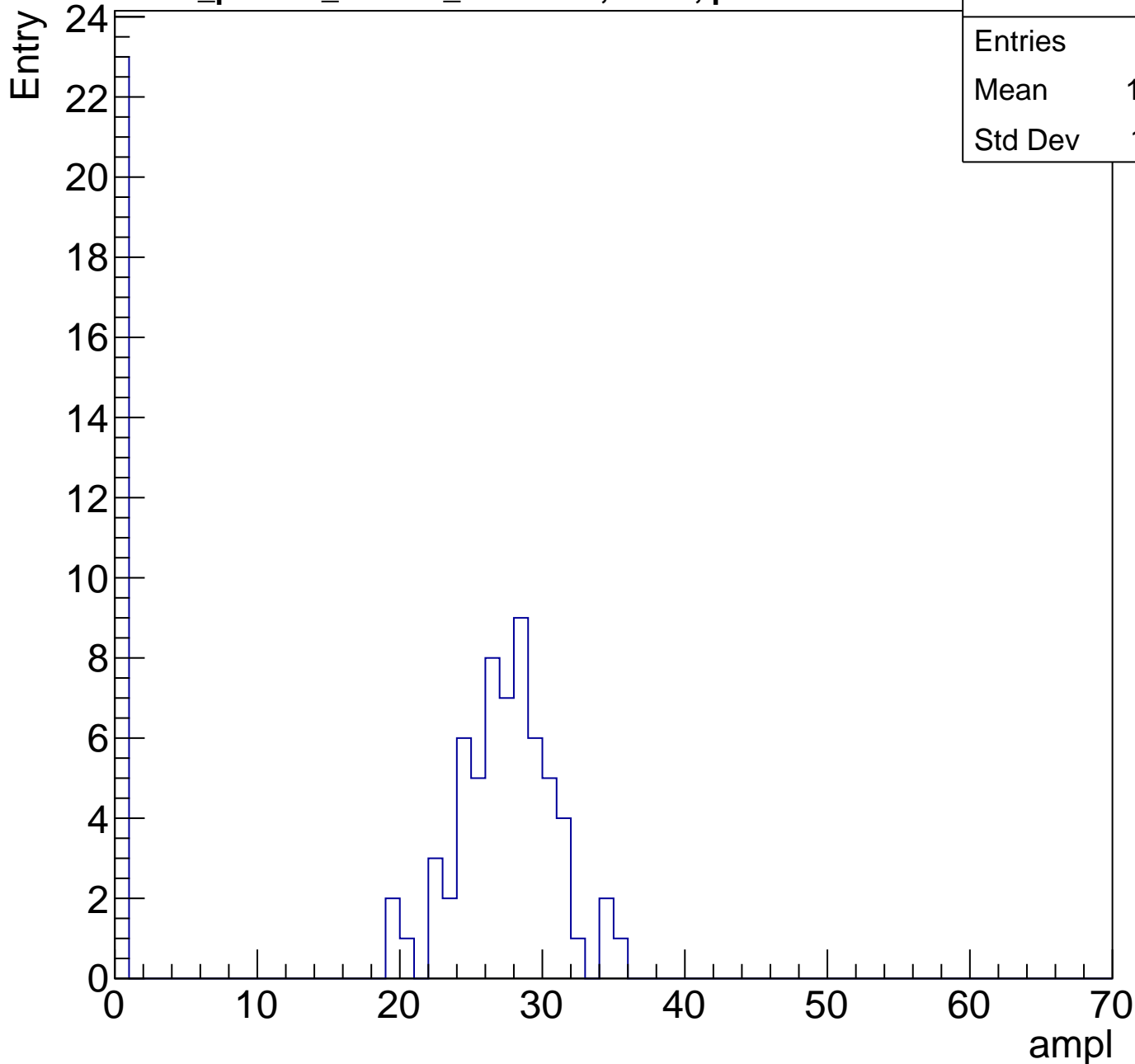
Entry



B1L103S, U11-ch116, adc0

calib_packv5_041523_1651.root, FC#0, port C2

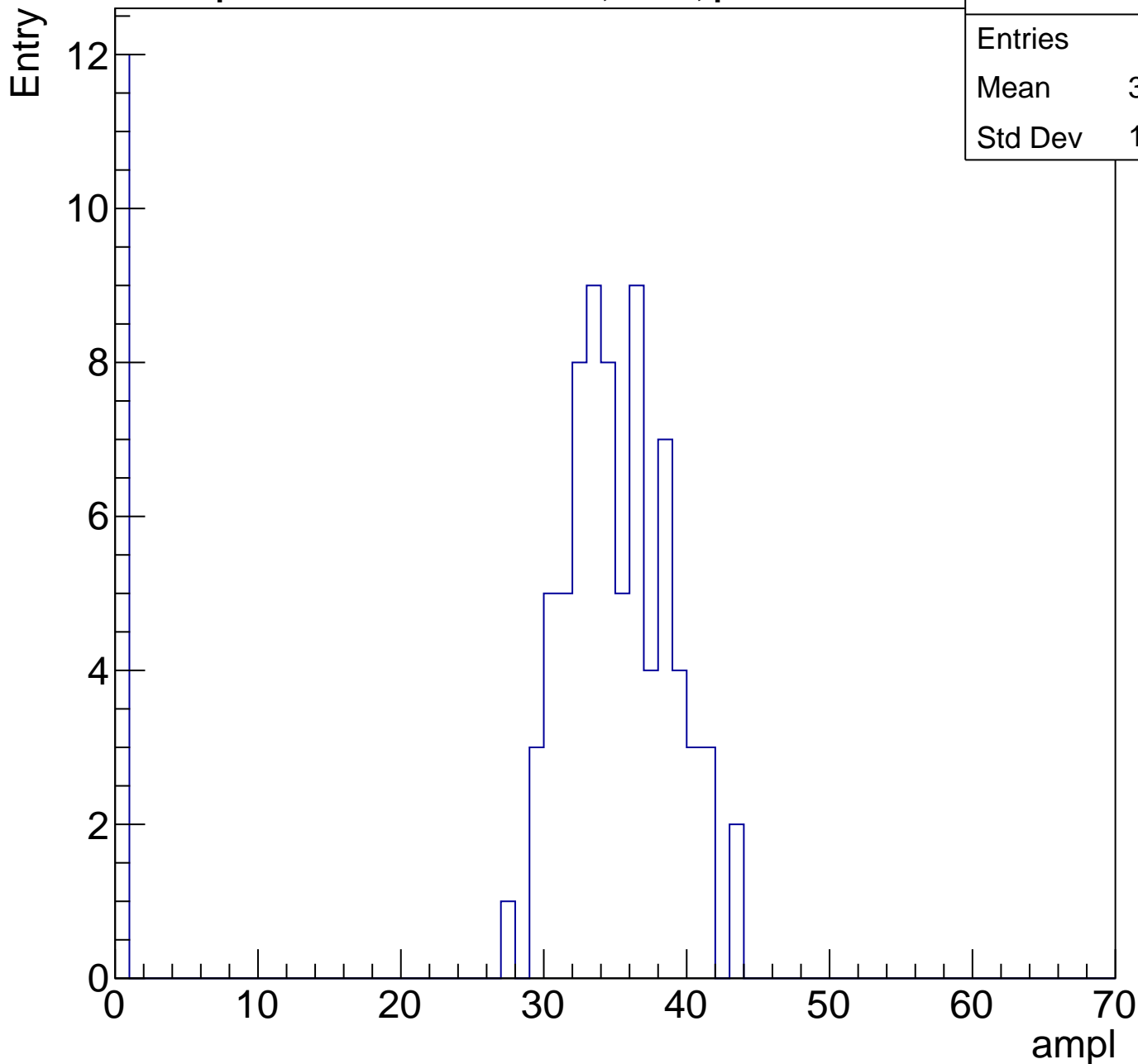
Entries	85
Mean	19.66
Std Dev	12.31



B1L103S, U11-ch116, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	88
Mean	30.02
Std Dev	12.37

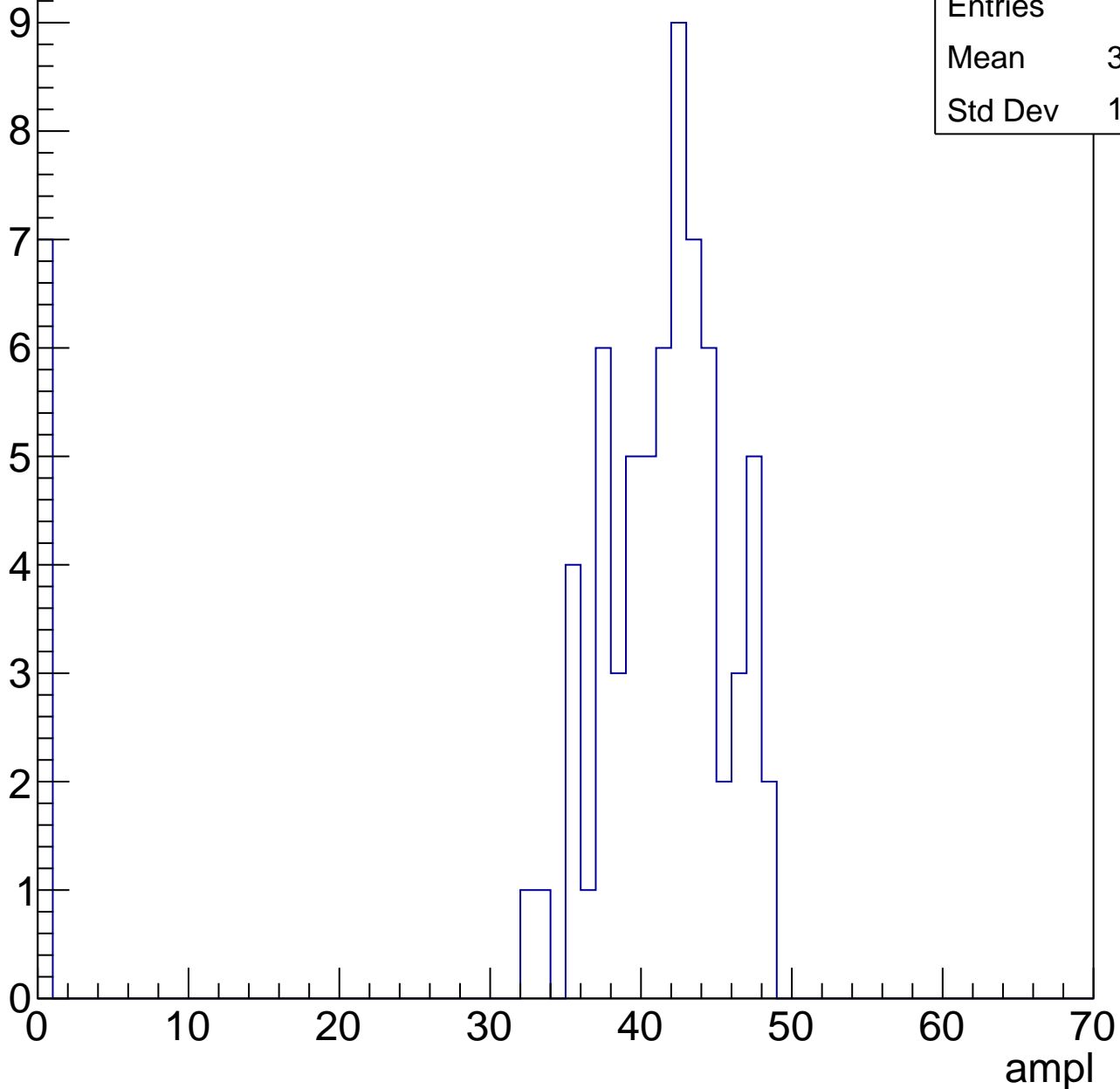


B1L103S, U11-ch116, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	37.26
Std Dev	12.65

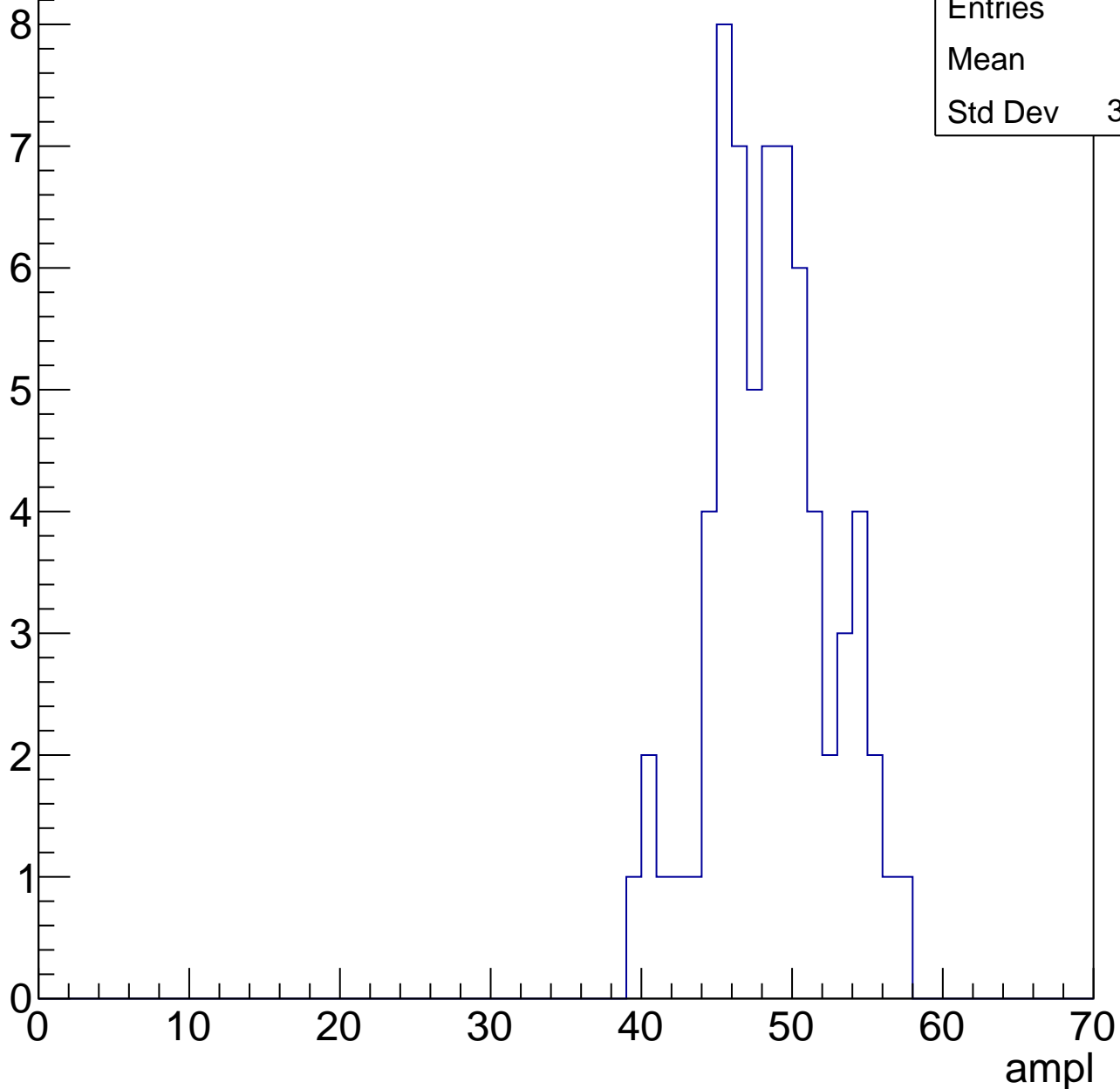


B1L103S, U11-ch116, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	48.1
Std Dev	3.955

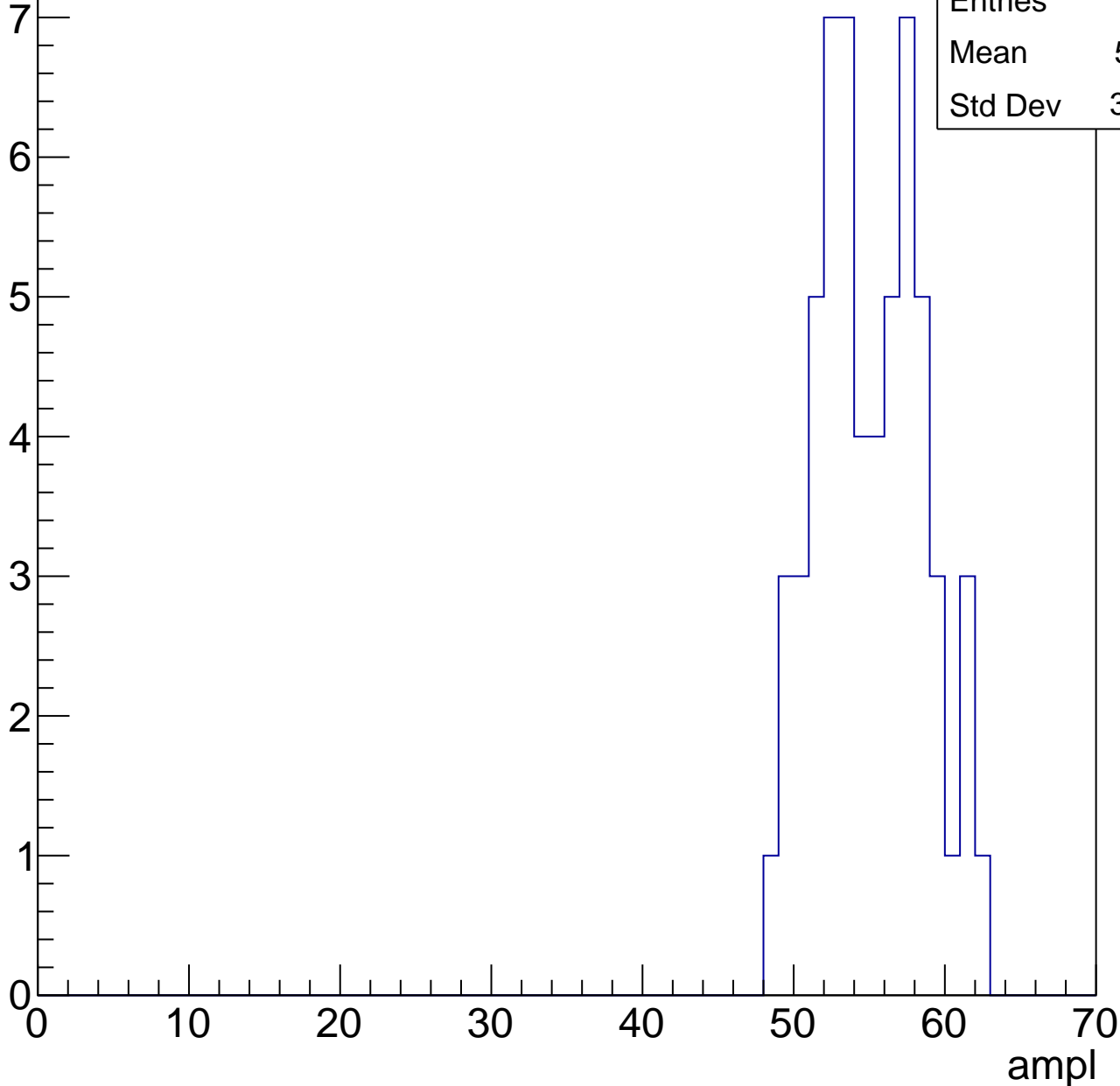


B1L103S, U11-ch116, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	54.61
Std Dev	3.459

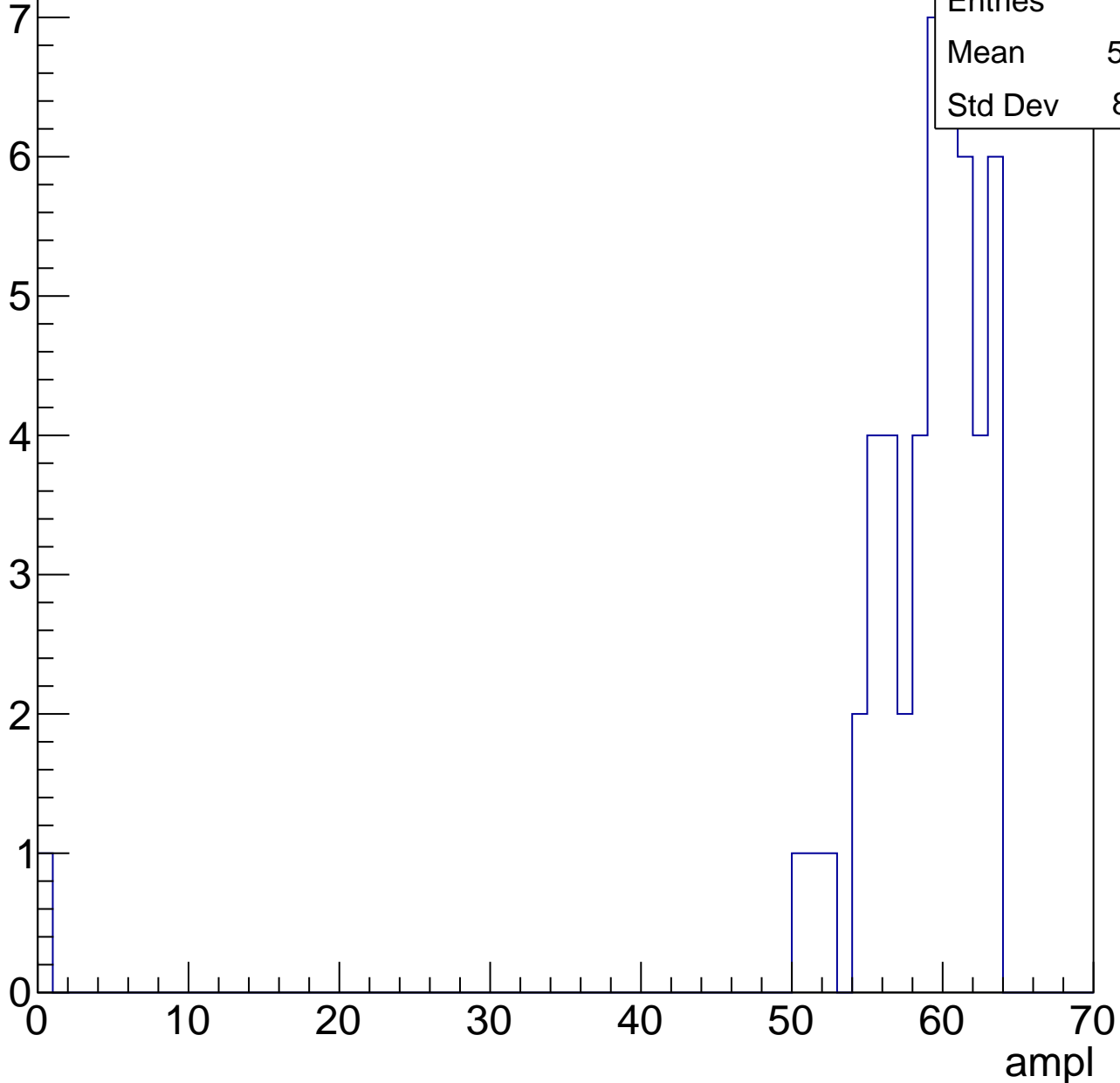


B1L103S, U11-ch116, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	57.52
Std Dev	8.821

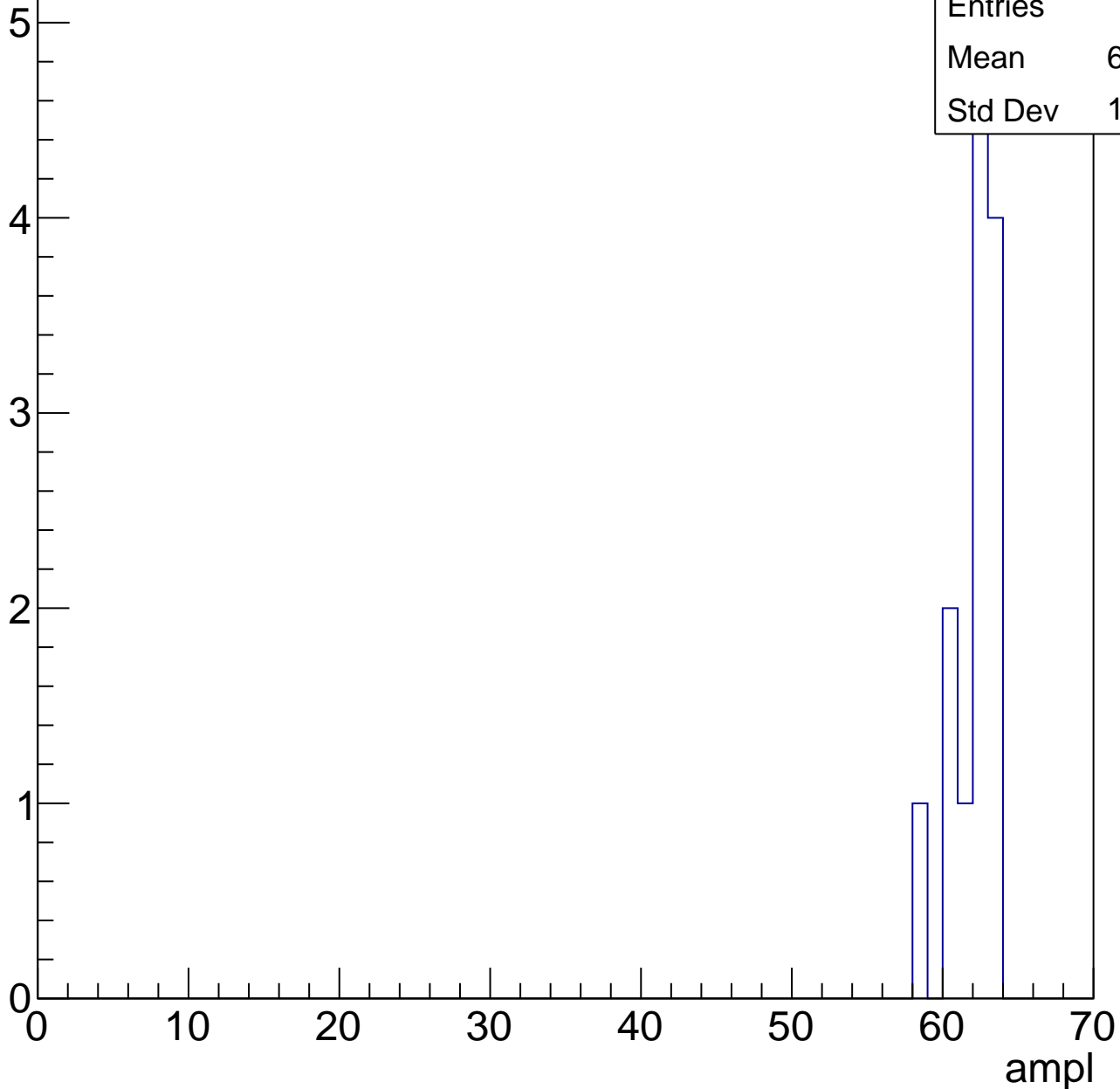


B1L103S, U11-ch116, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	13
Mean	61.62
Std Dev	1.443



B1L103S, U11-ch116, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

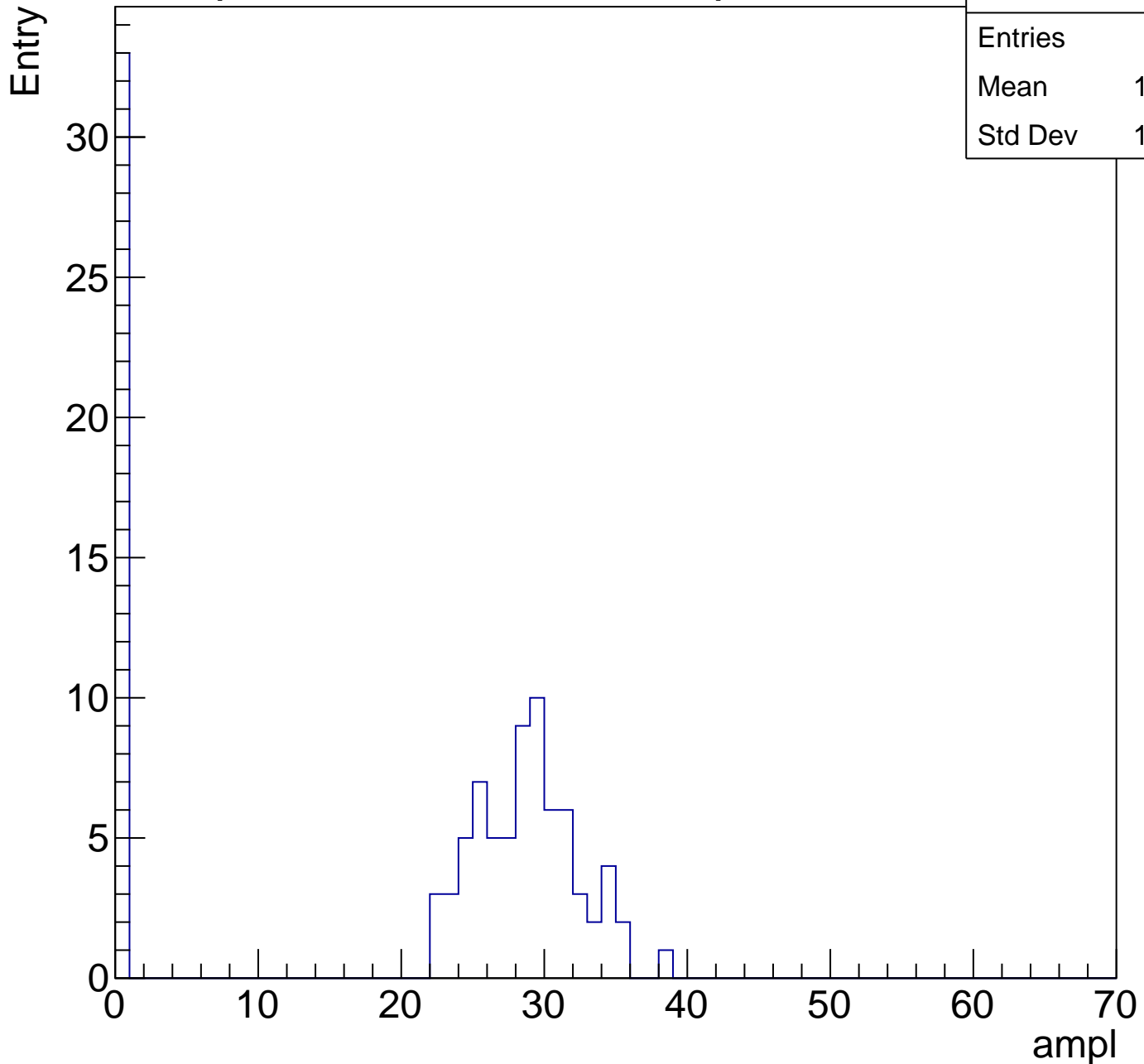
ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U11-ch117, adc0

calib_packv5_041523_1651.root, FC#0, port C2

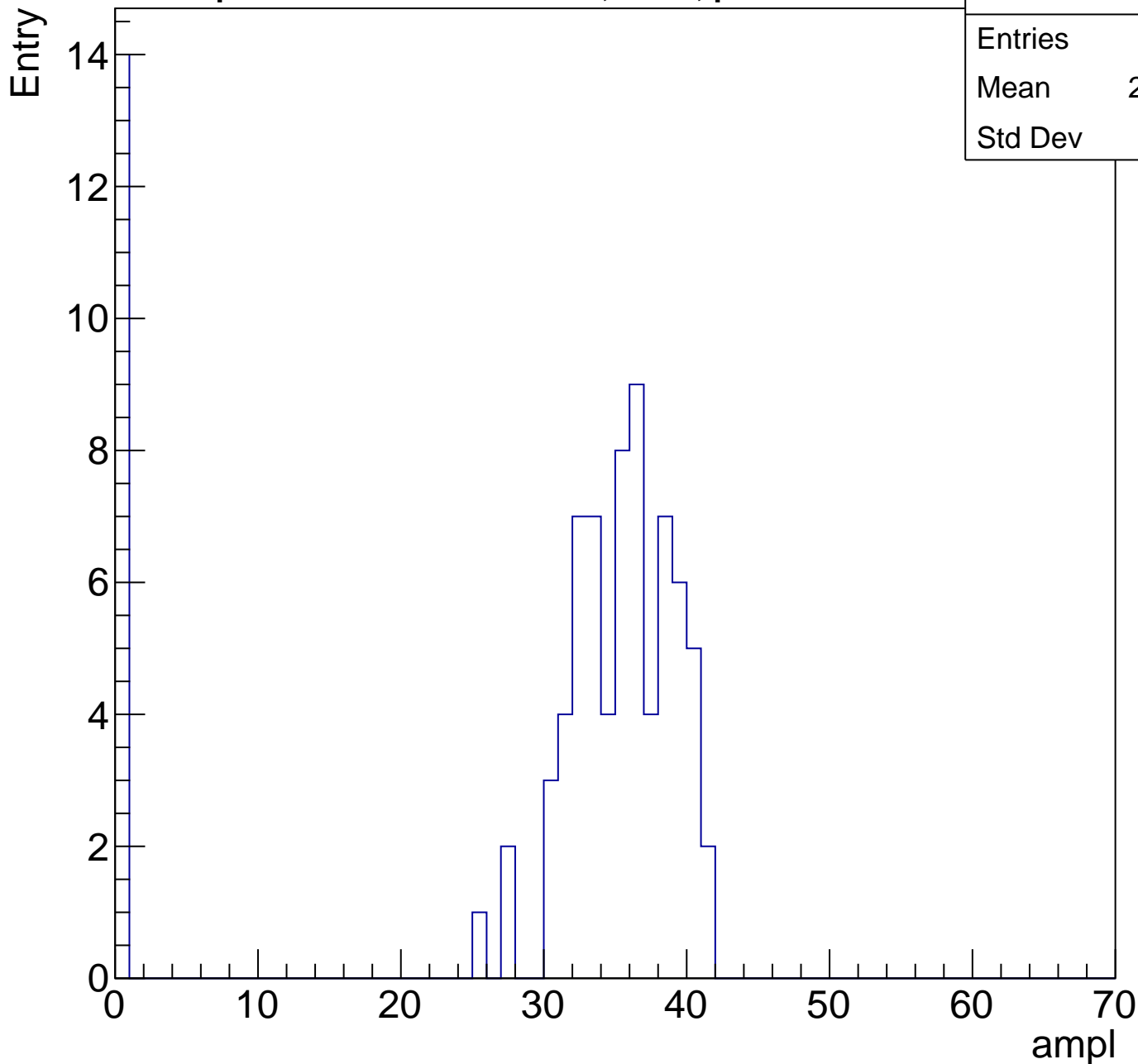
Entries	104
Mean	19.32
Std Dev	13.48



B1L103S, U11-ch117, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	83
Mean	29.13
Std Dev	13.5

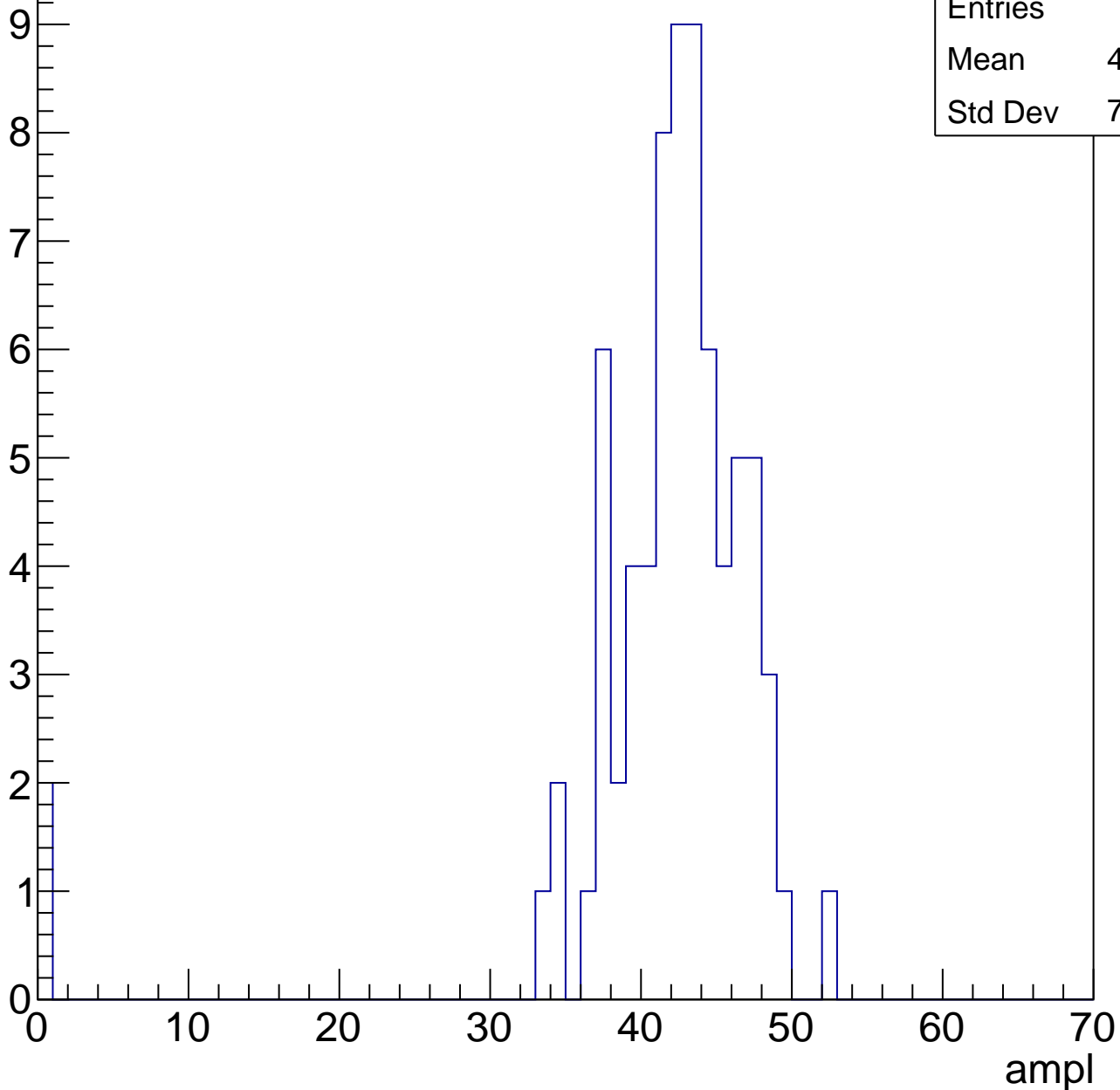


B1L103S, U11-ch117, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	41.07
Std Dev	7.836

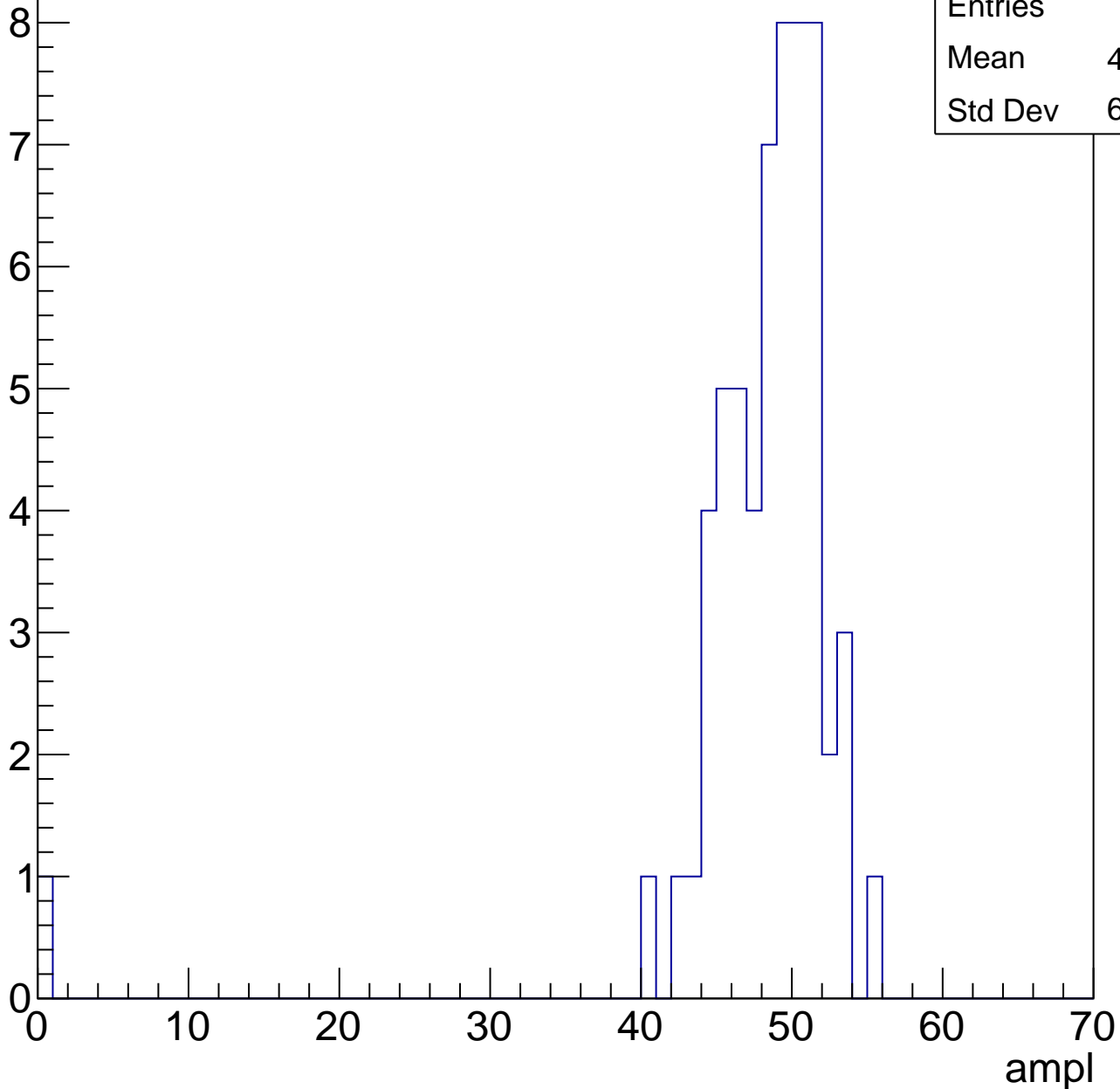


B1L103S, U11-ch117, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	47.42
Std Dev	6.902

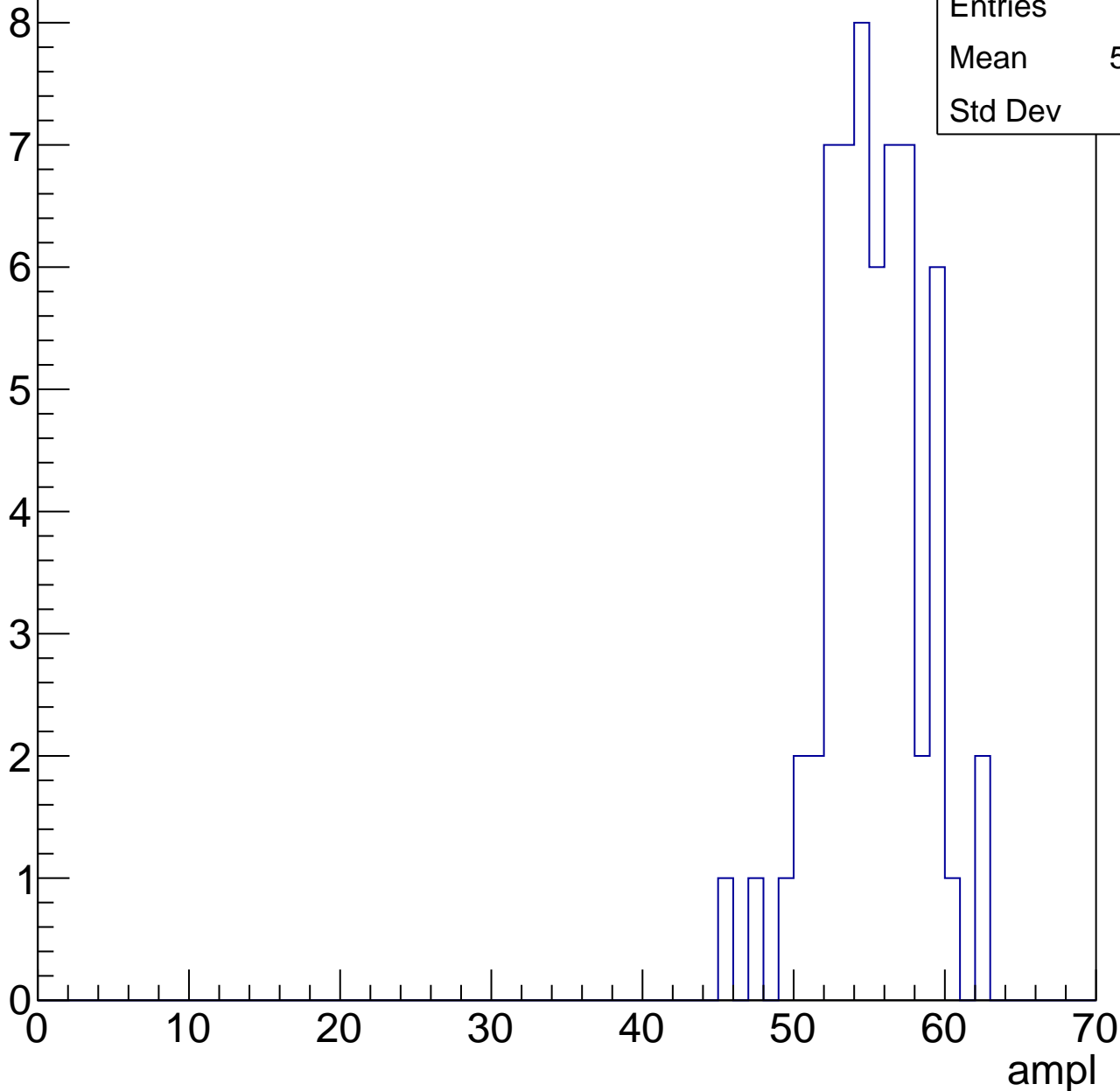


B1L103S, U11-ch117, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	54.75
Std Dev	3.29

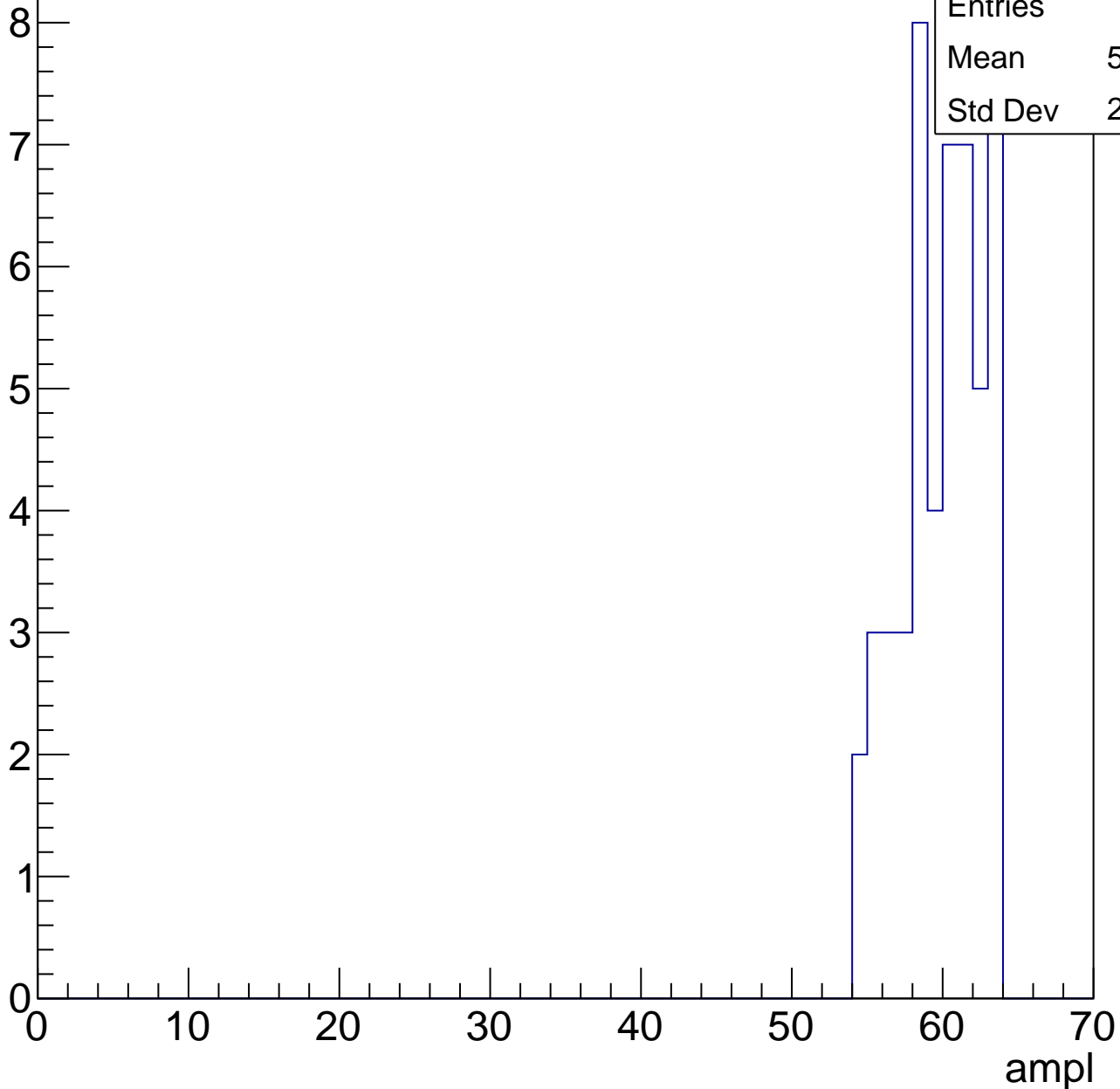


B1L103S, U11-ch117, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

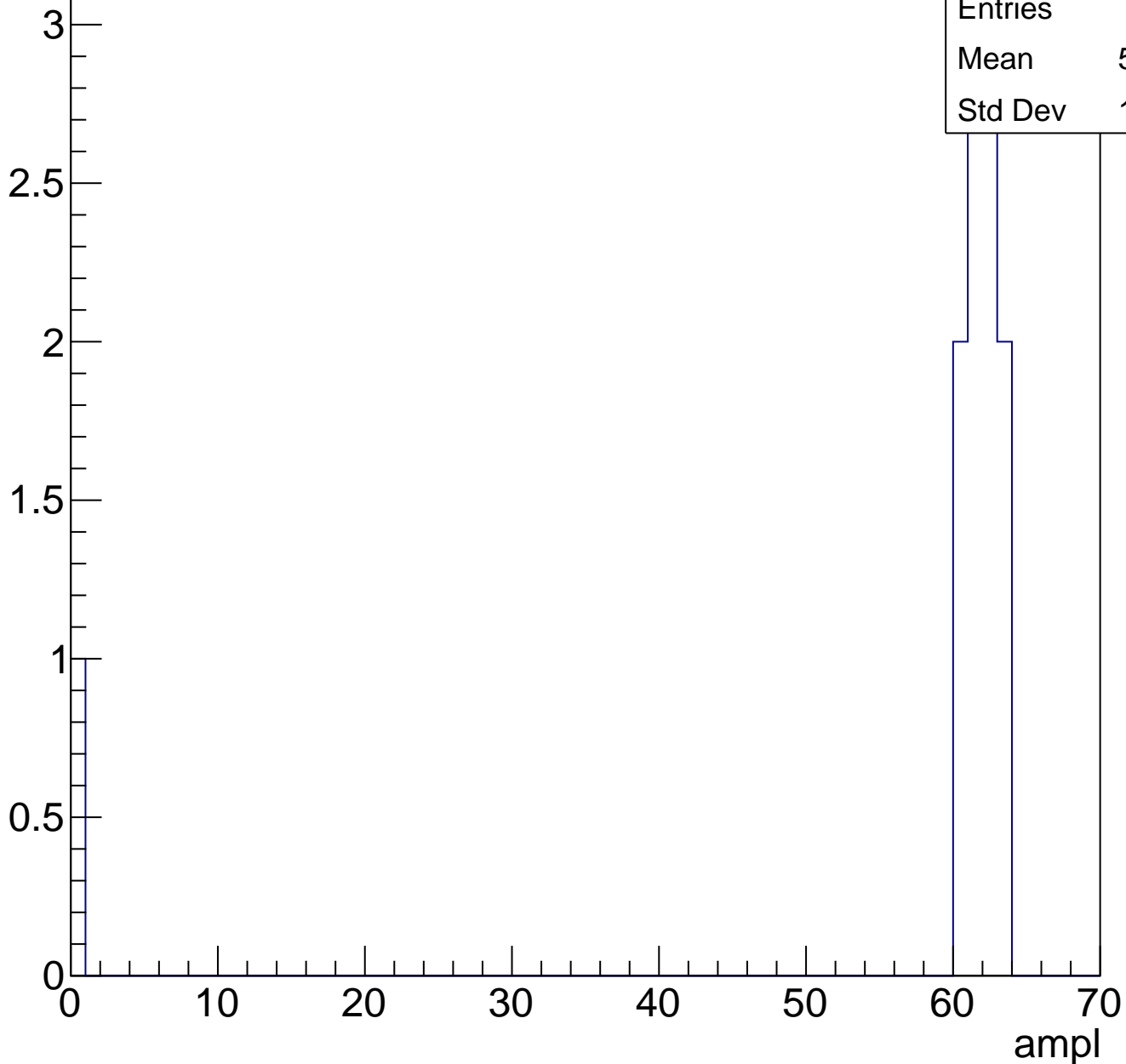
Entries	50
Mean	59.46
Std Dev	2.617



B1L103S, U11-ch117, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

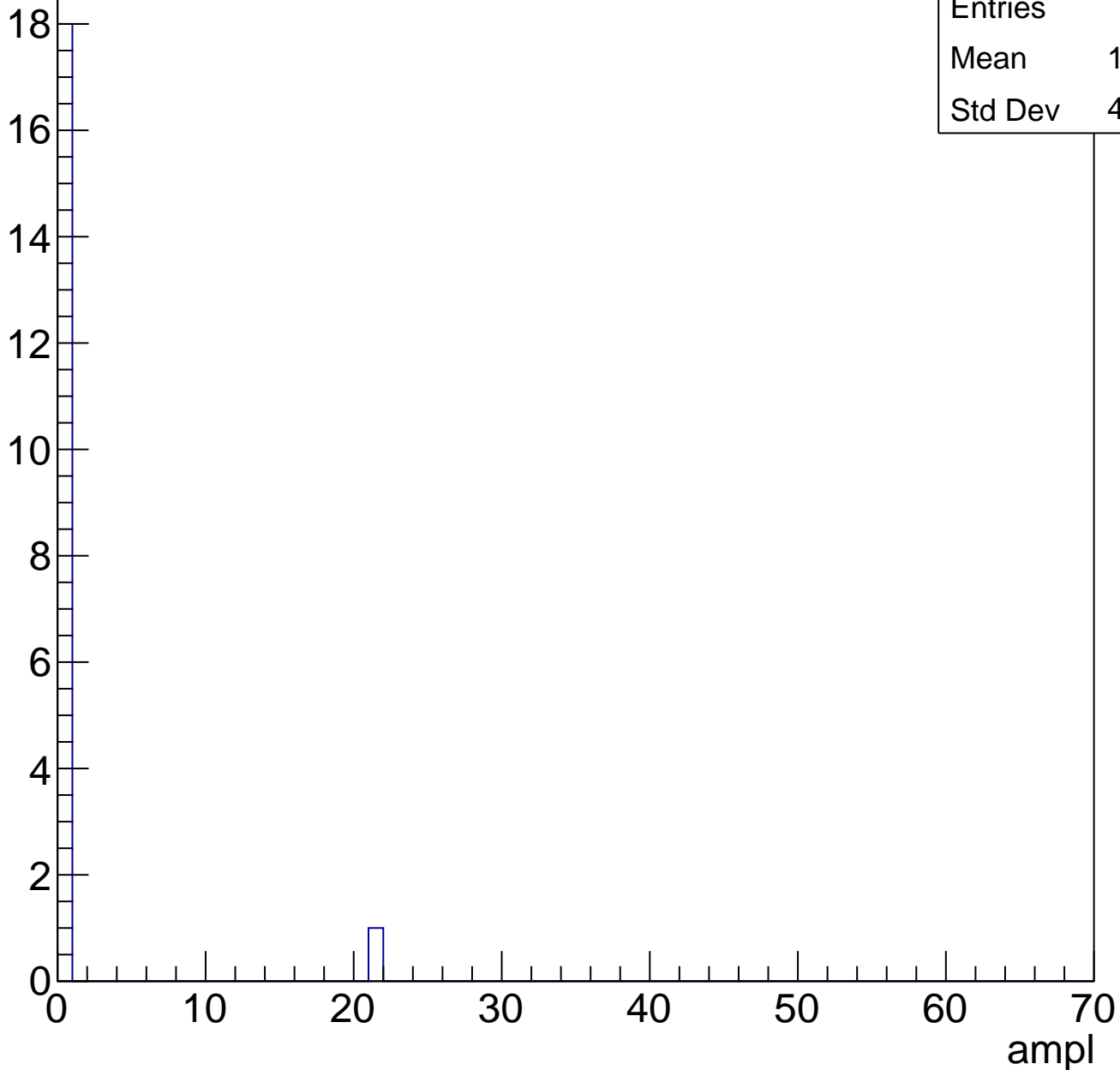


B1L103S, U11-ch117, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.105
Std Dev	4.689

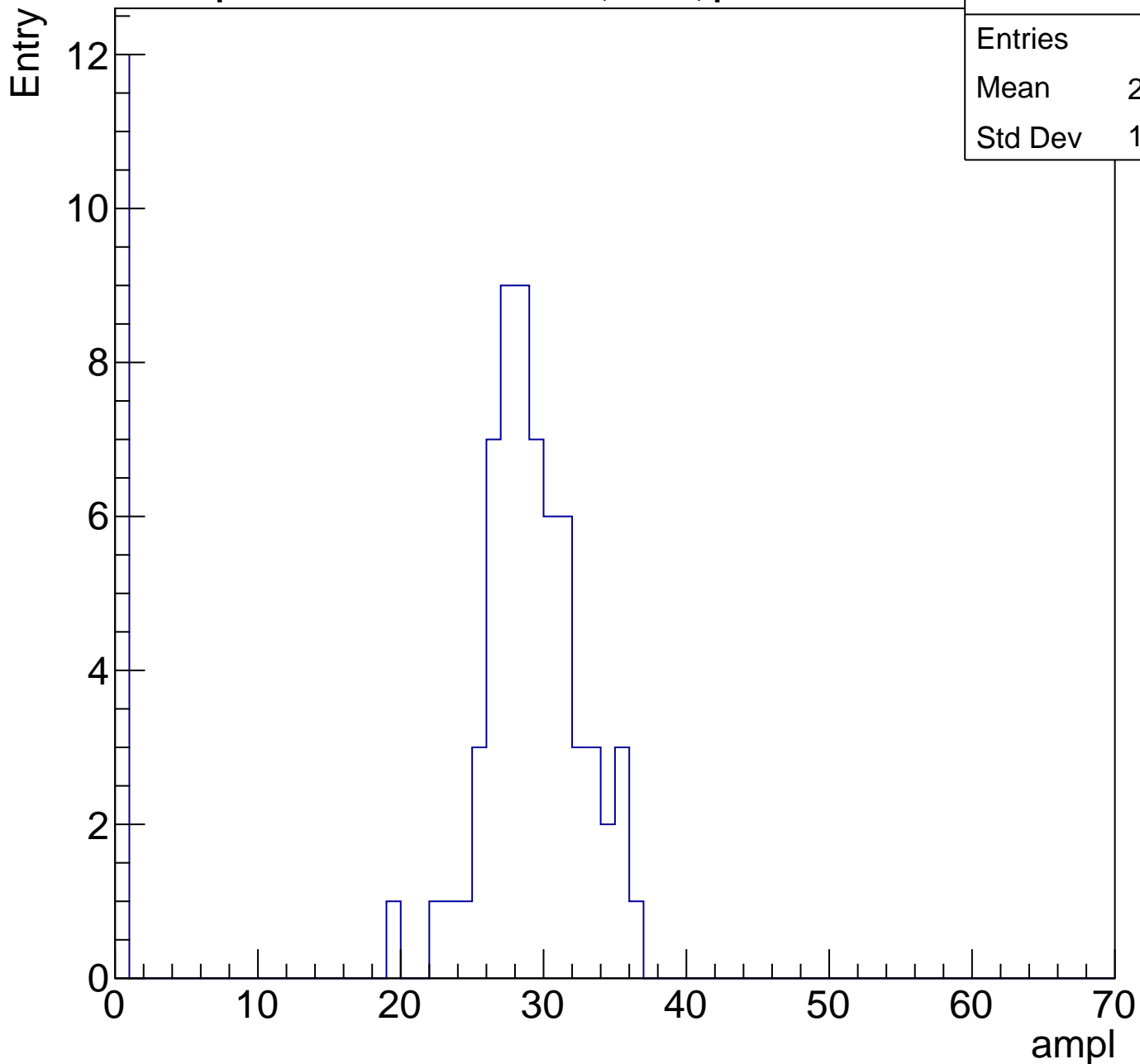
Entry



B1L103S, U11-ch118, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	24.17
Std Dev	10.97

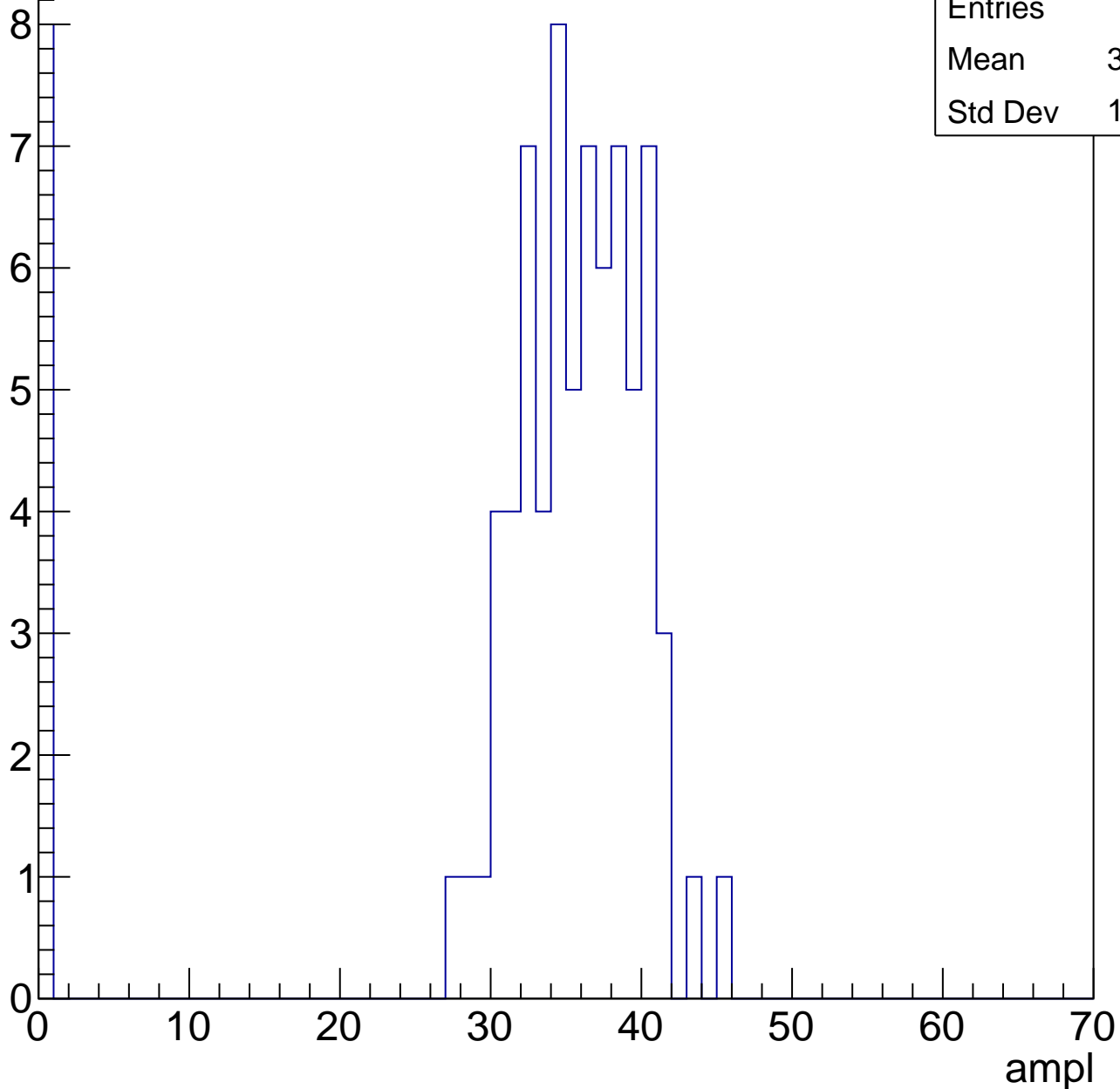


B1L103S, U11-ch118, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	80
Mean	31.96
Std Dev	11.23

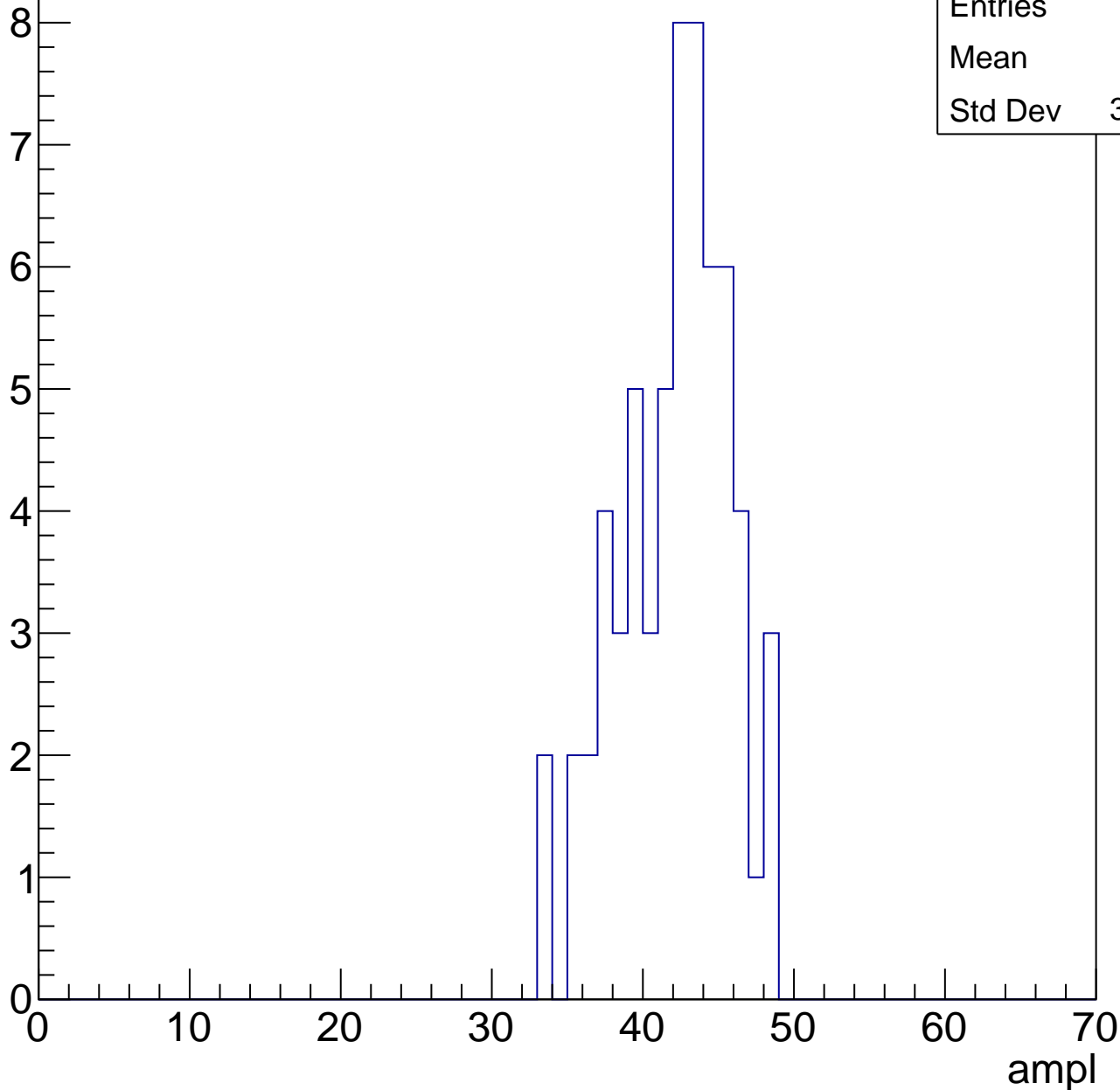


B1L103S, U11-ch118, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	41.6
Std Dev	3.625

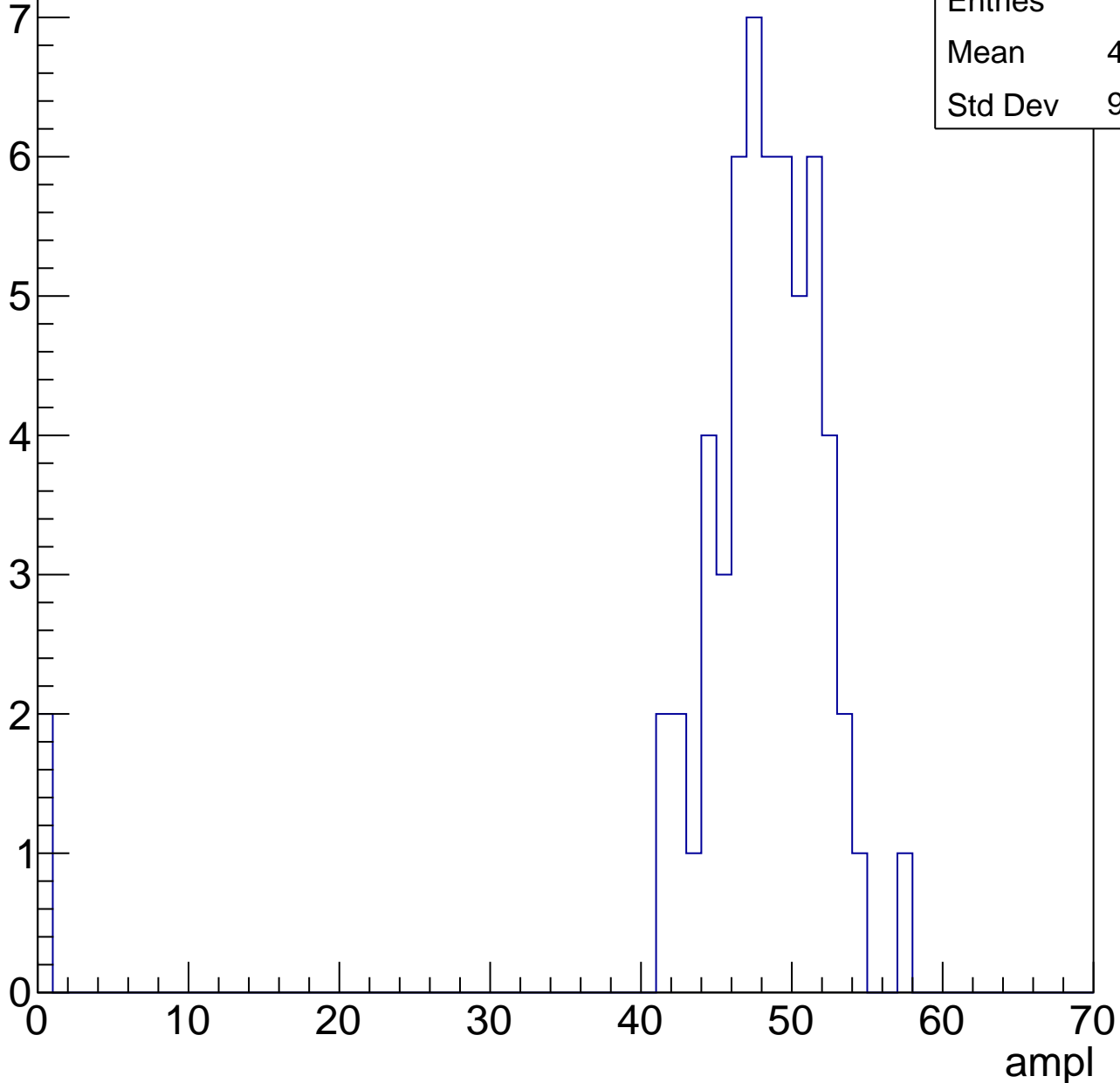


B1L103S, U11-ch118, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	46.34
Std Dev	9.356

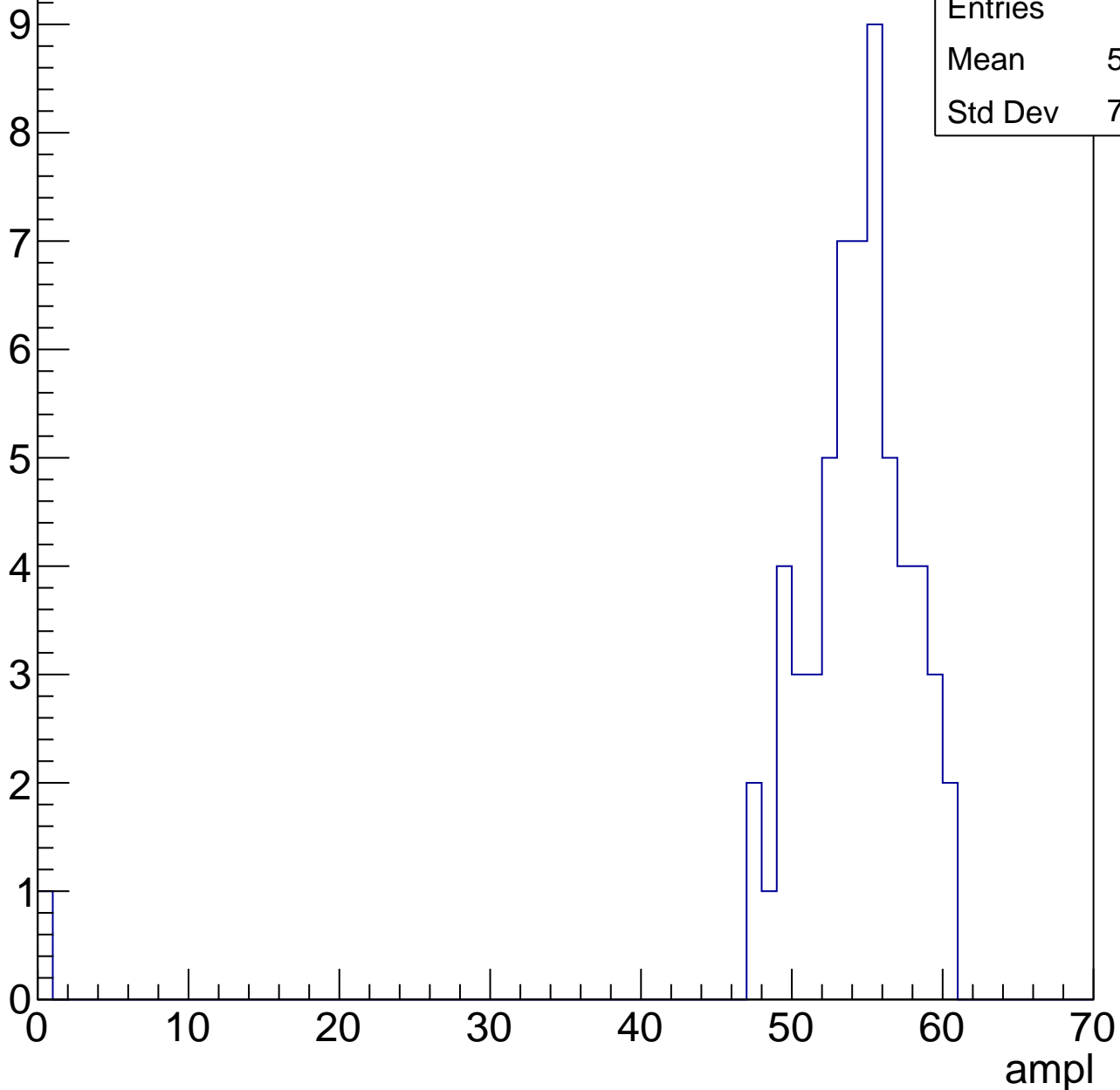


B1L103S, U11-ch118, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	53.03
Std Dev	7.607

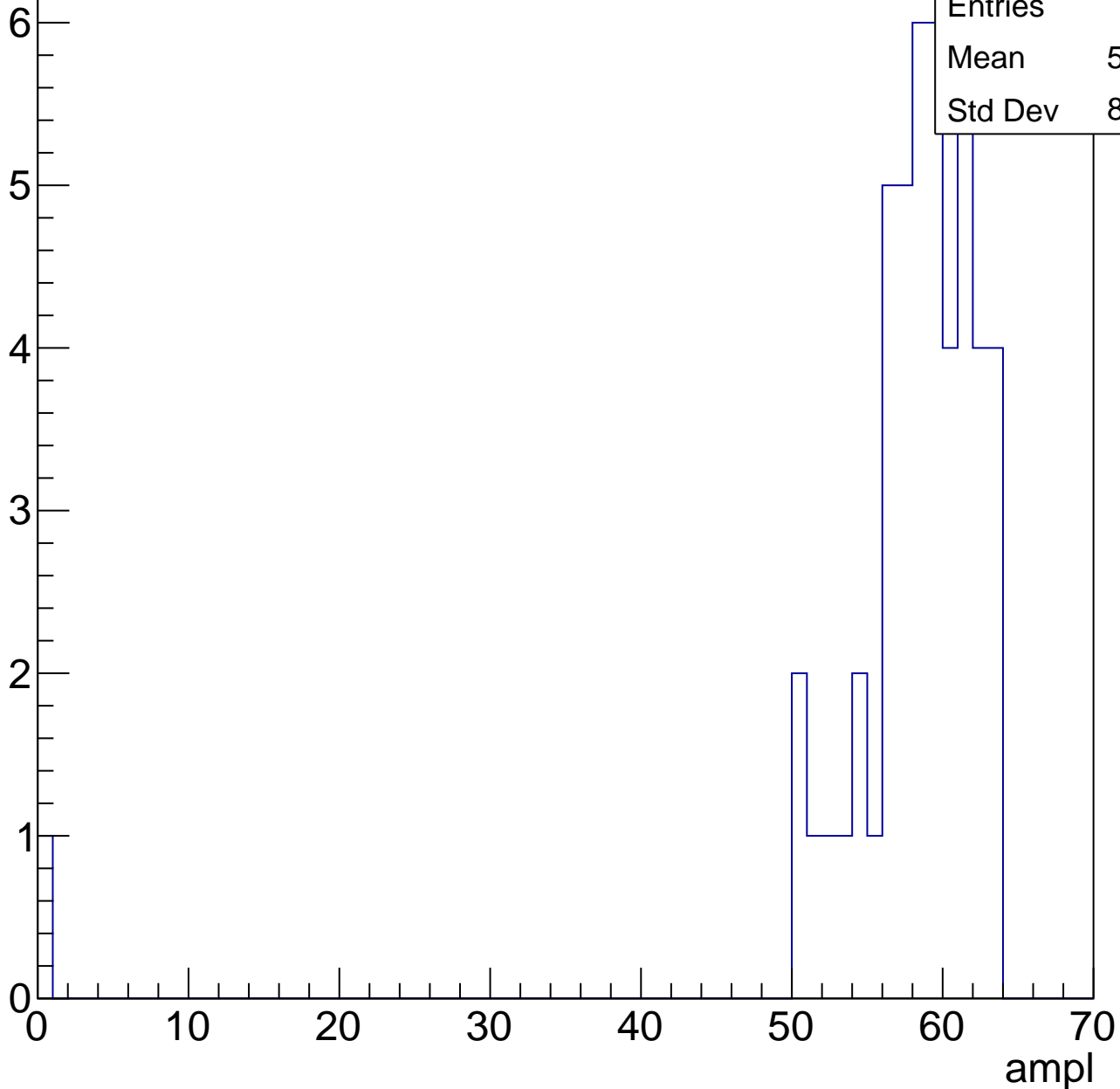


B1L103S, U11-ch118, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	56.98
Std Dev	8.872

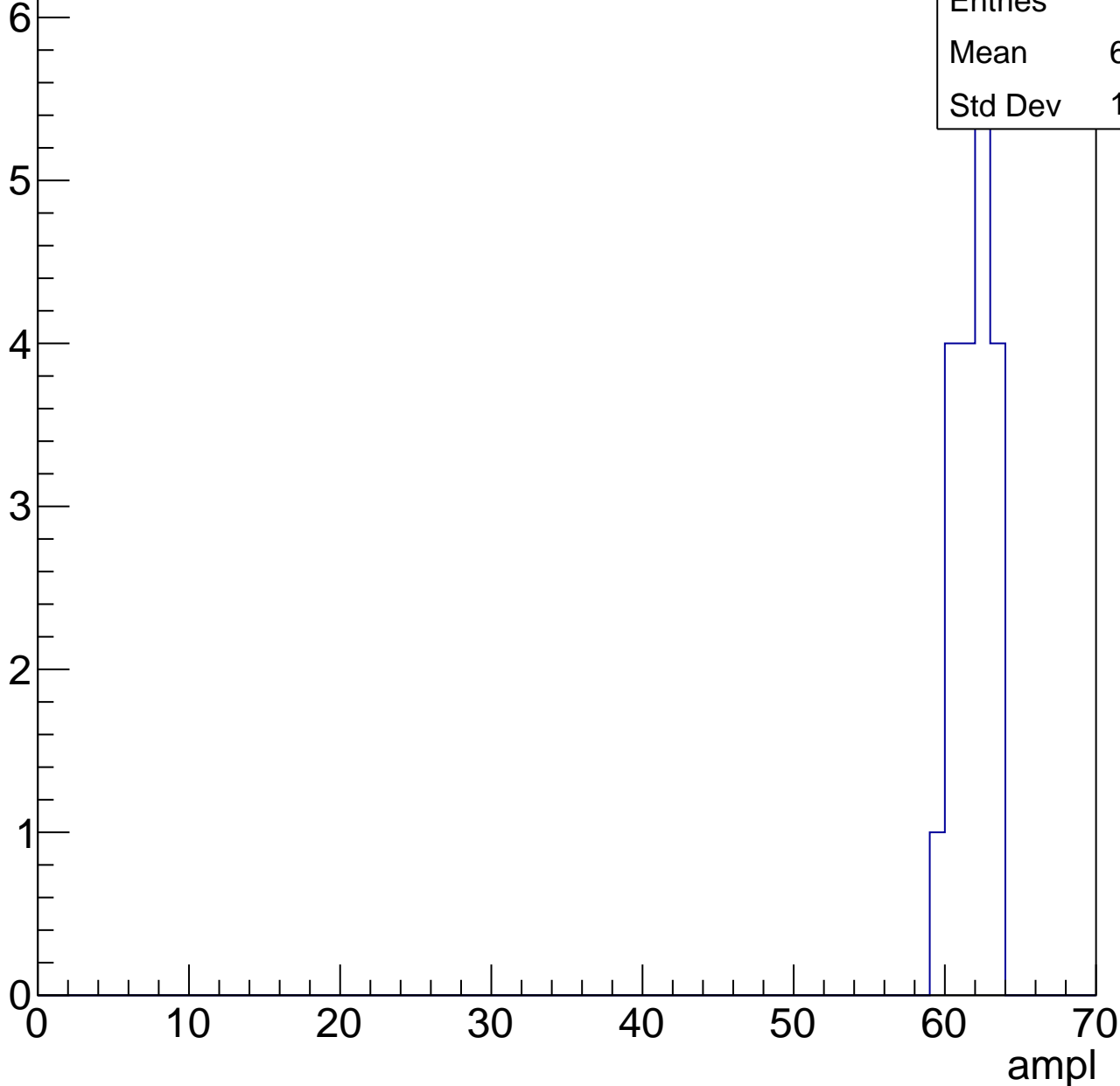


B1L103S, U11-ch118, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	19
Mean	61.42
Std Dev	1.184



B1L103S, U11-ch118, adc7

calib_packv5_041523_1651.root, FC#0, port C2

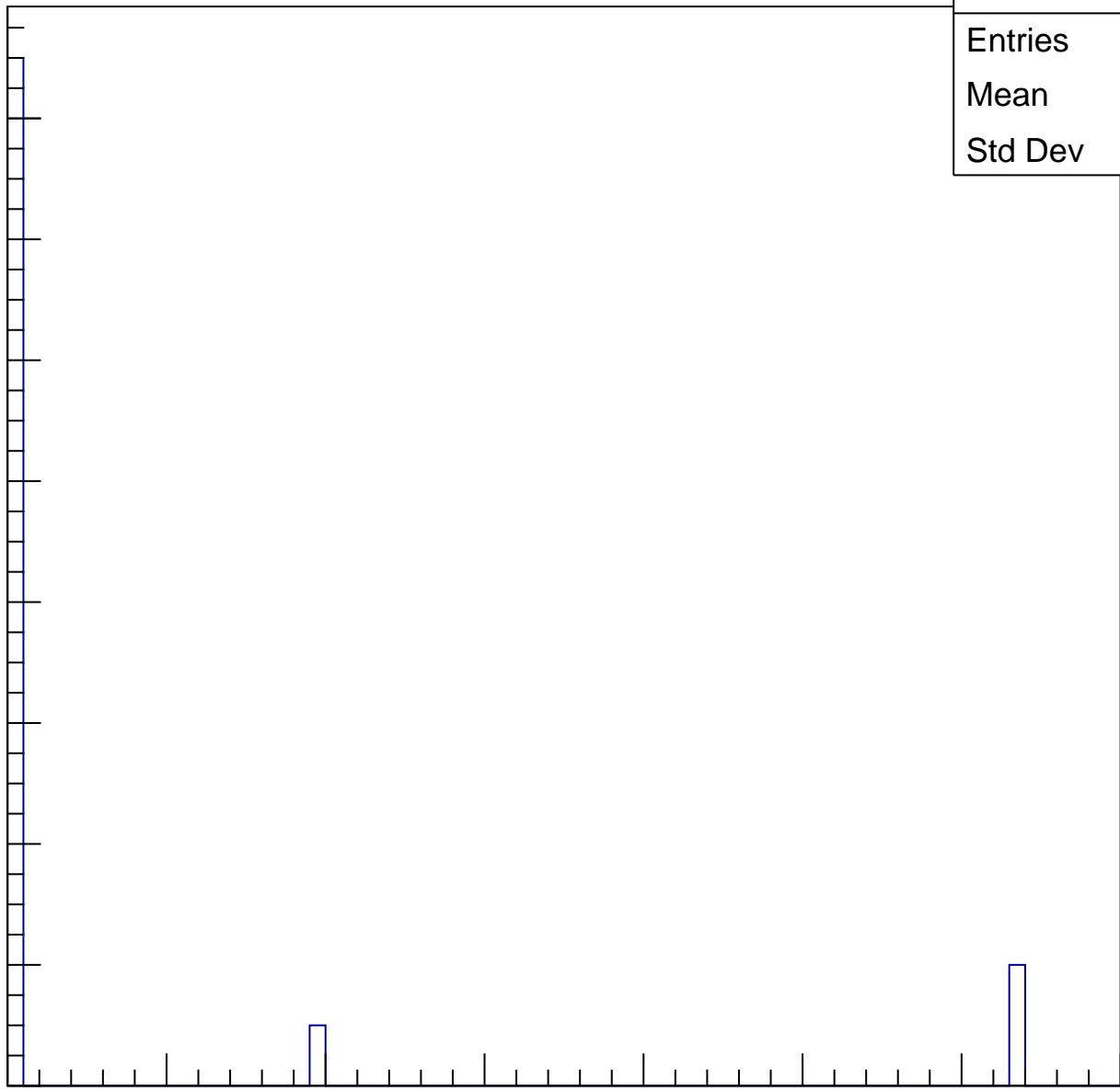
Entries	20
Mean	7.25
Std Dev	19.04

Entry

16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

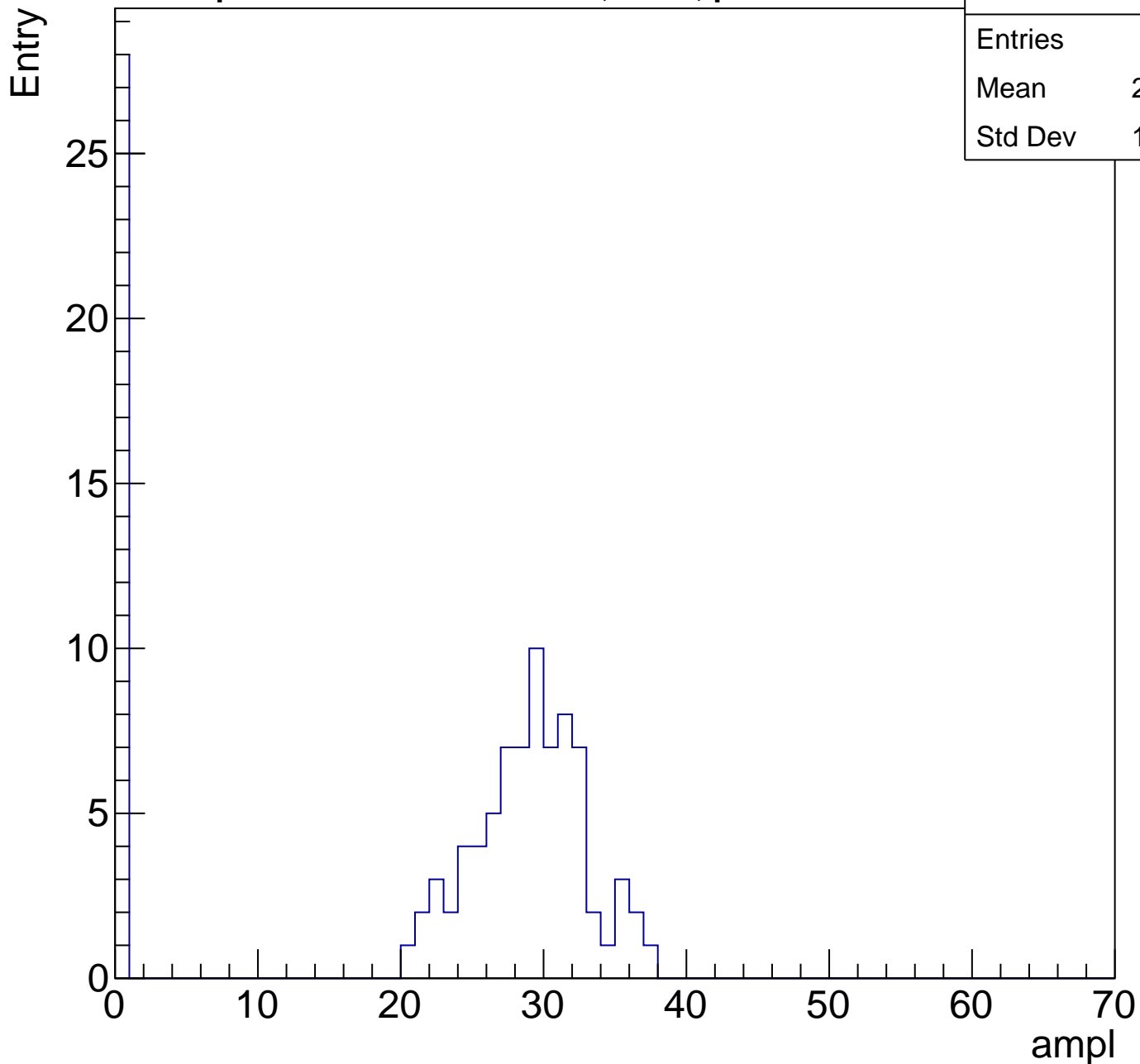
ampl



B1L103S, U11-ch119, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	104
Mean	20.88
Std Dev	13.08



B1L103S, U11-ch119, adc1

calib_packv5_041523_1651.root, FC#0, port C2

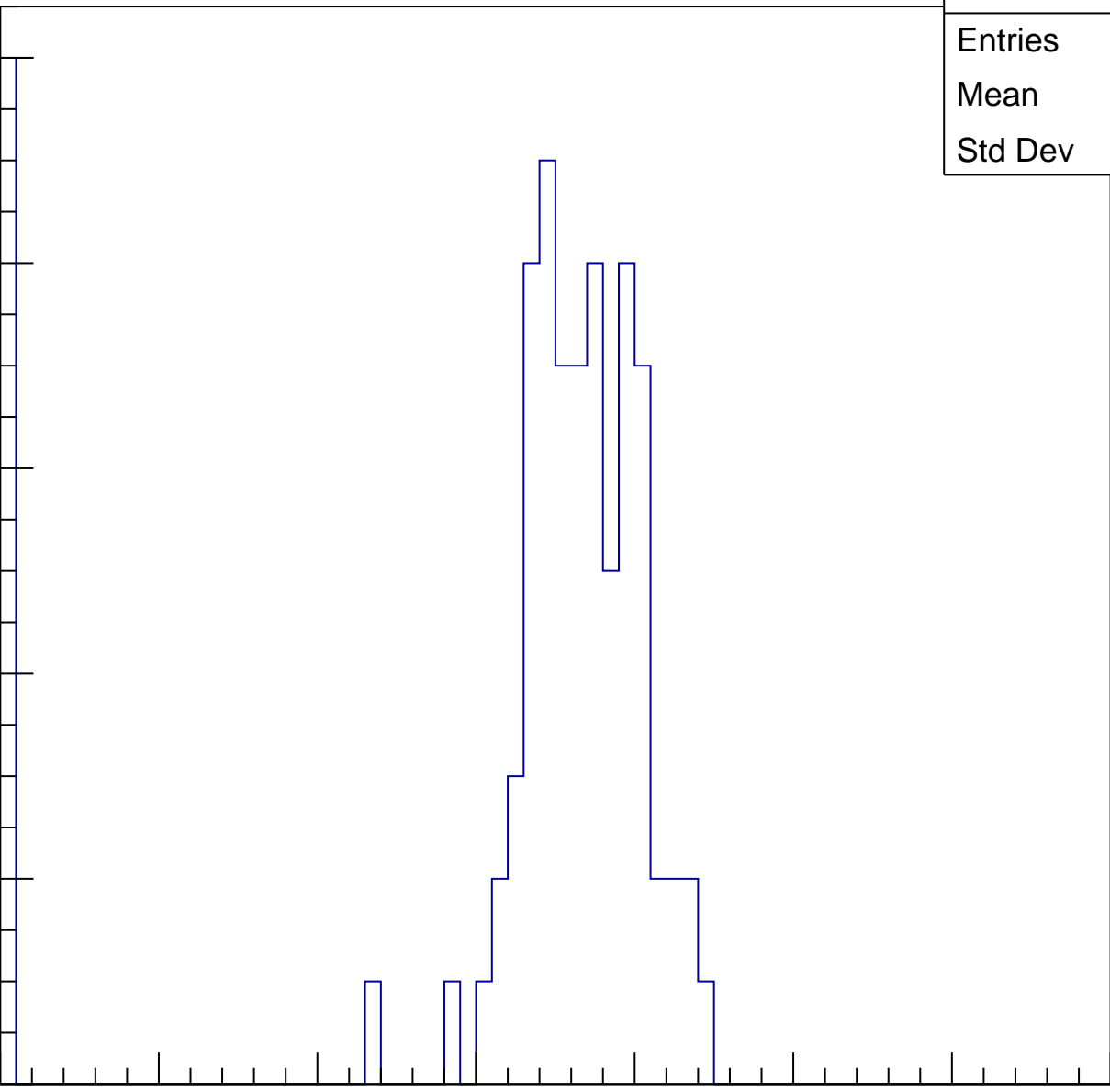
Entries	84
Mean	31.9
Std Dev	12.21

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

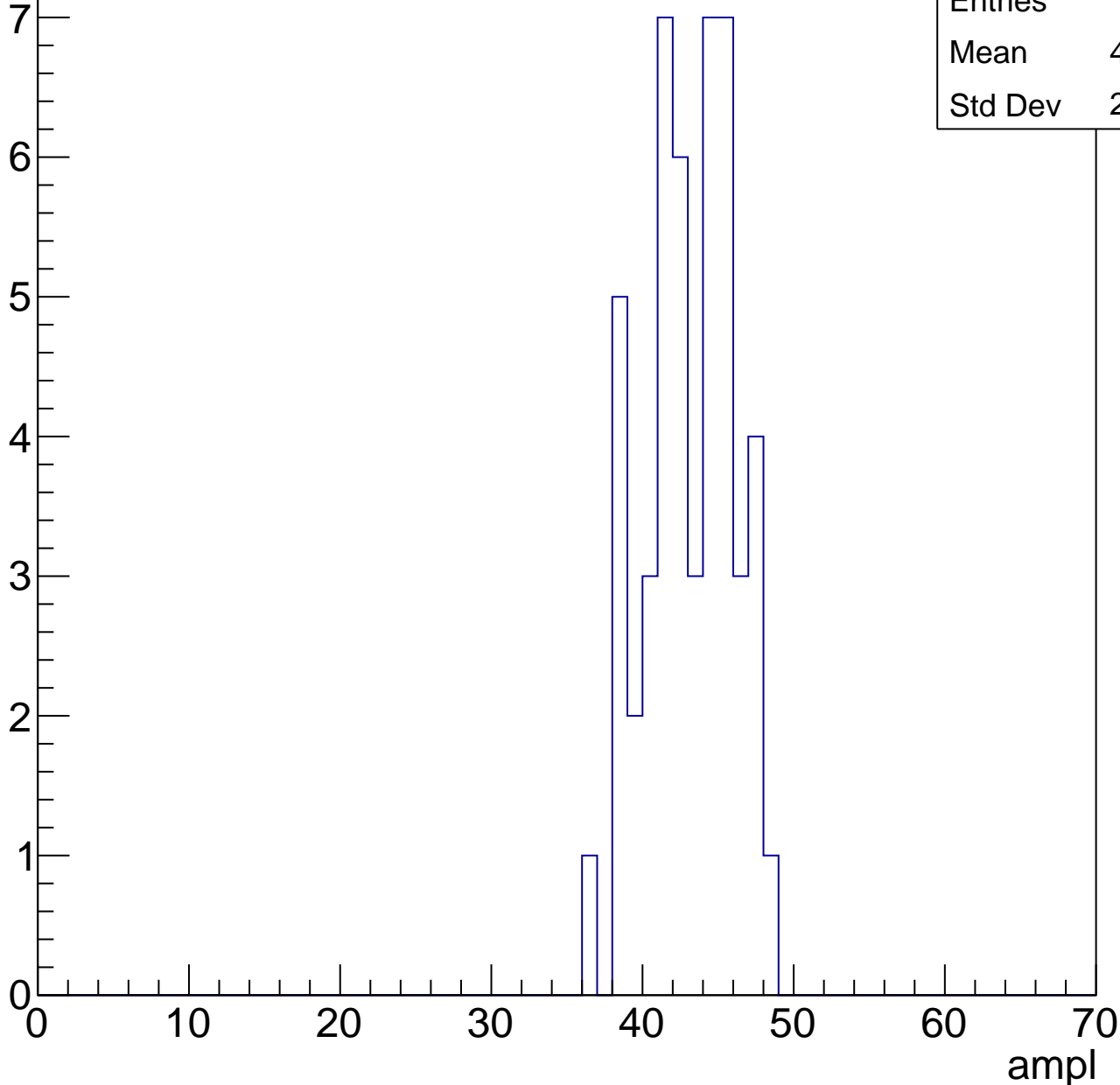


B1L103S, U11-ch119, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	42.63
Std Dev	2.898

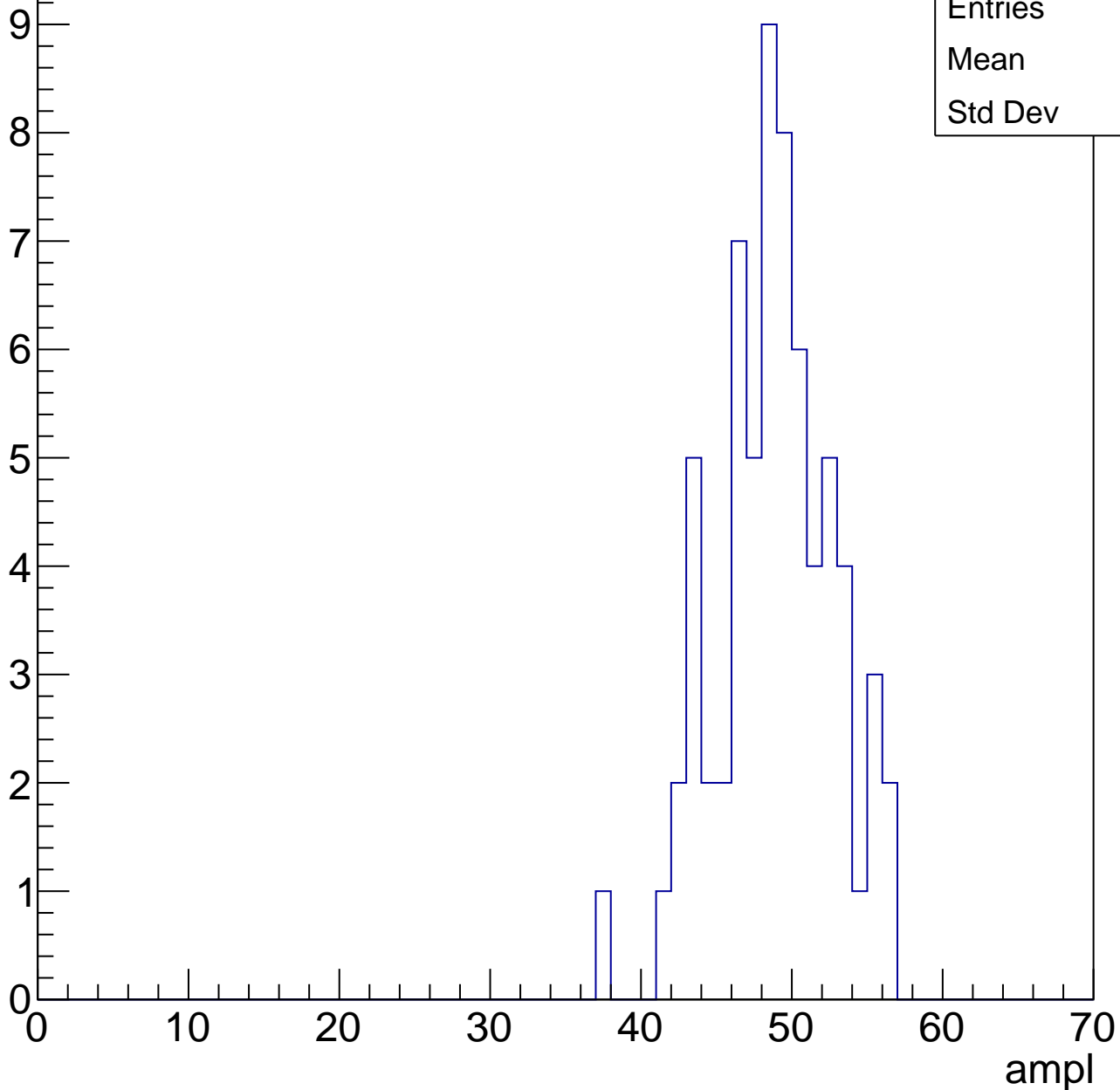


B1L103S, U11-ch119, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	48.4
Std Dev	3.86

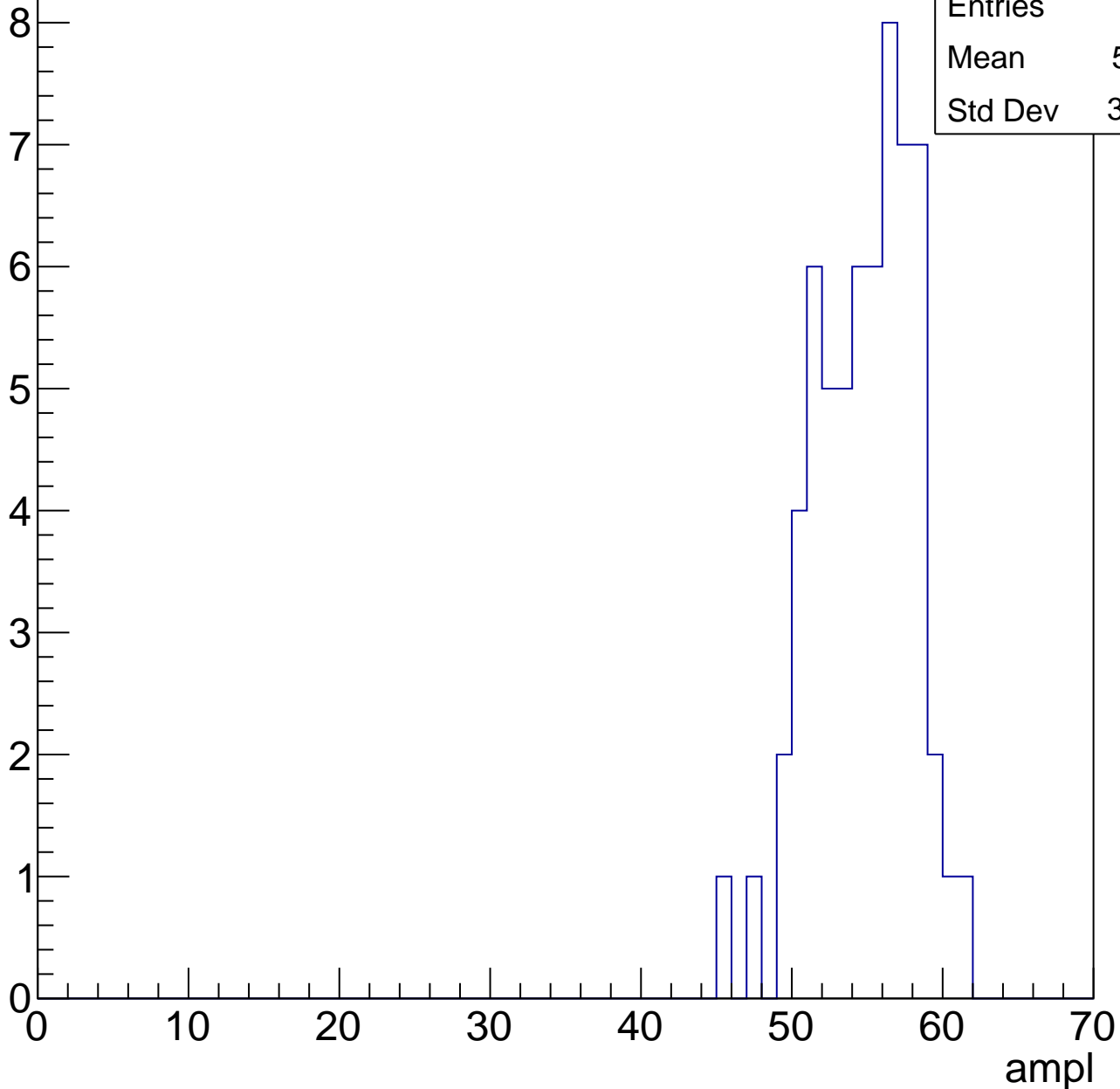


B1L103S, U11-ch119, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	54.31
Std Dev	3.275

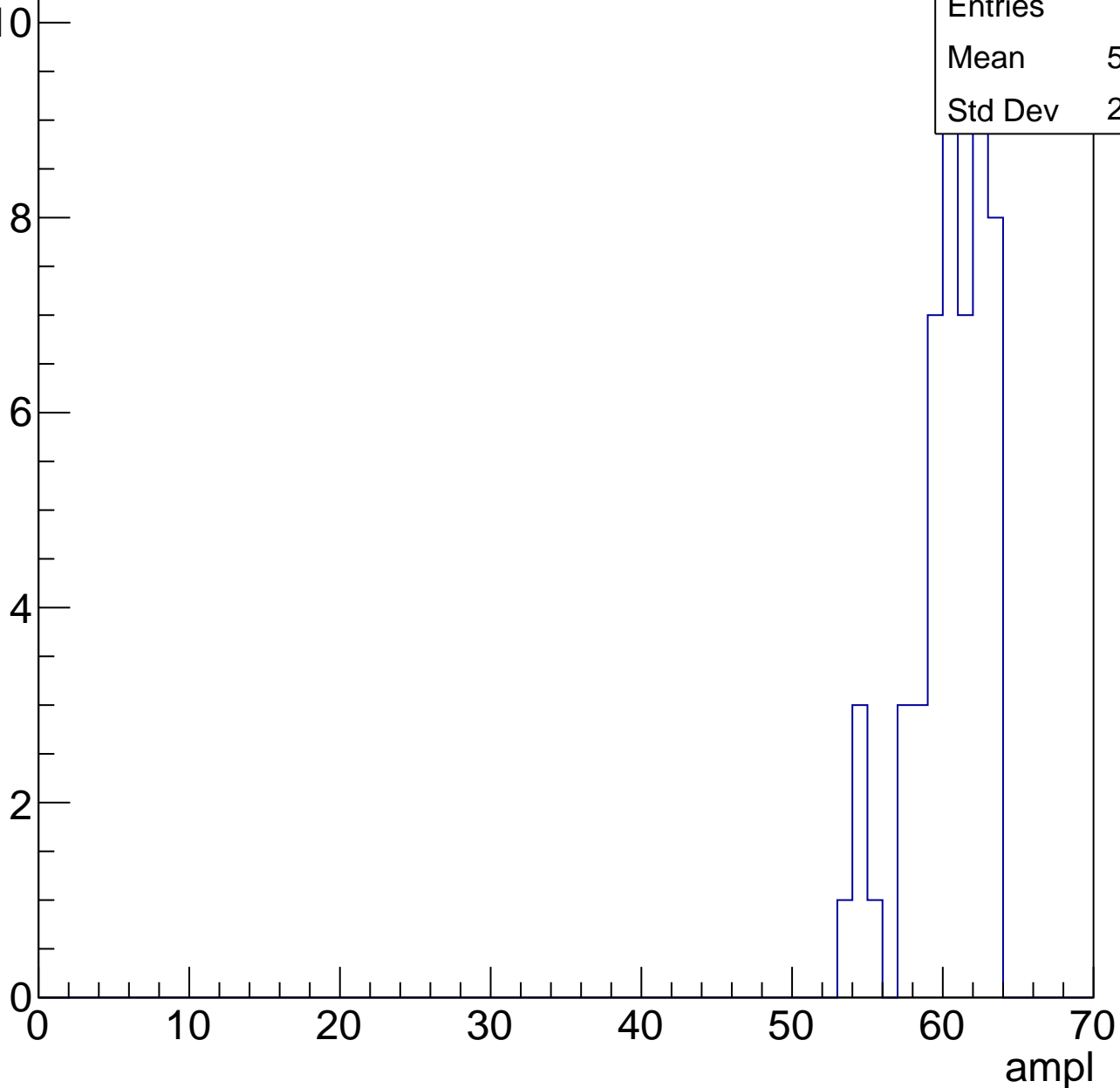


B1L103S, U11-ch119, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	59.98
Std Dev	2.583



B1L103S, U11-ch119, adc6

calib_packv5_041523_1651.root, FC#0, port C2

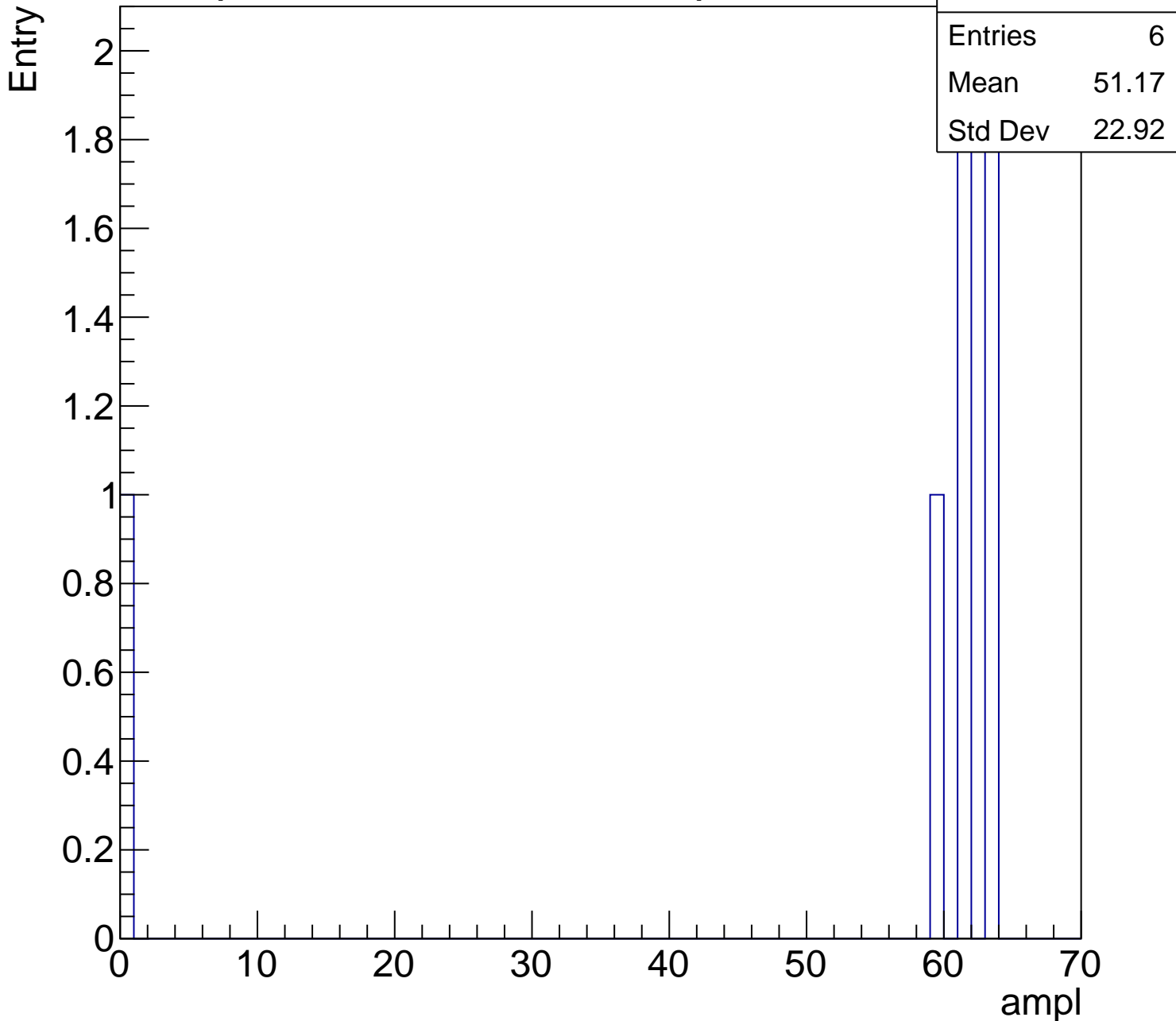
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	6
Mean	51.17
Std Dev	22.92

0 10 20 30 40 50 60 70

ampl



B1L103S, U11-ch119, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

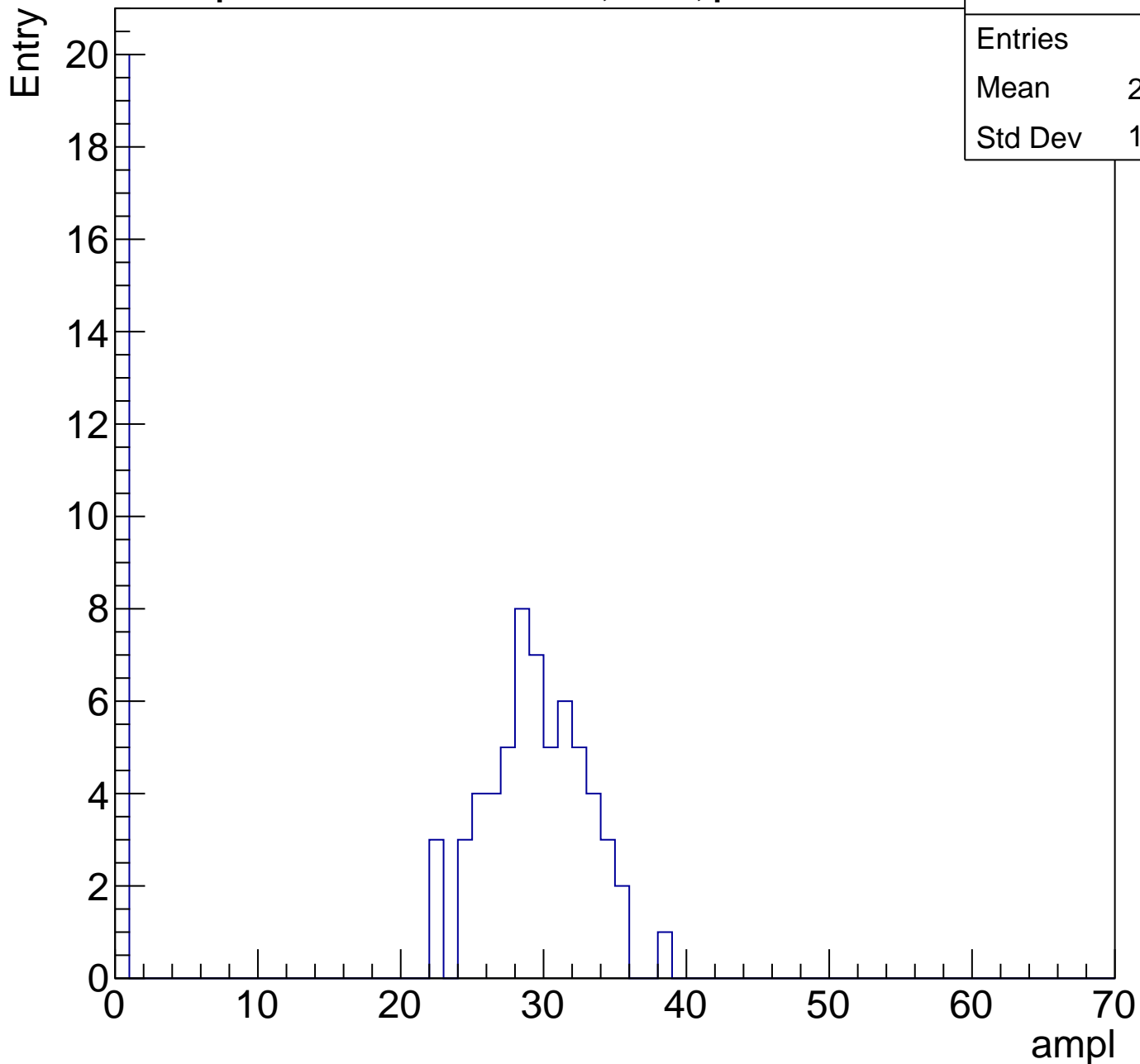
ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U11-ch120, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	21.77
Std Dev	12.92



B1L103S, U11-ch120, adc1

calib_packv5_041523_1651.root, FC#0, port C2

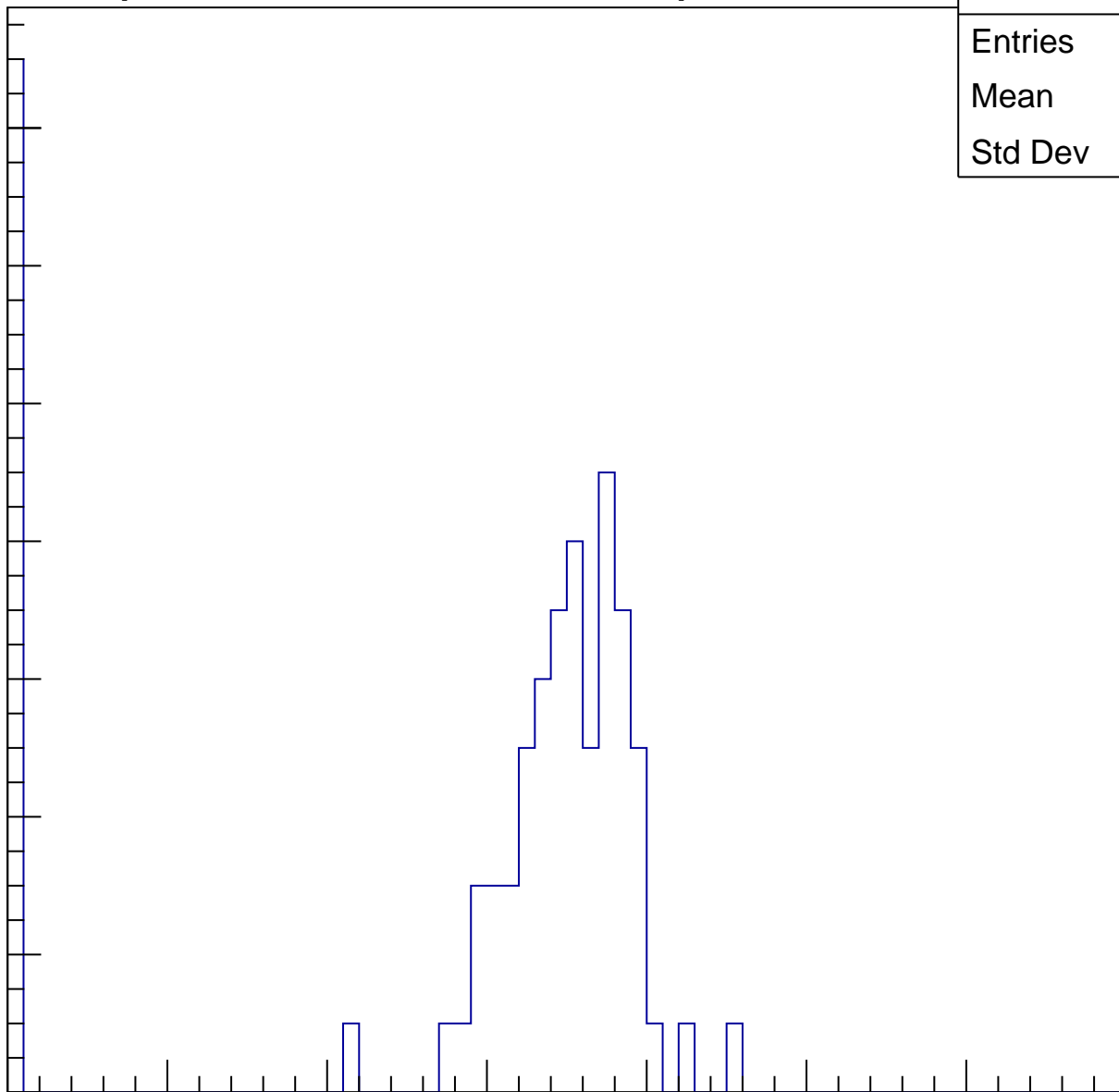
Entries	82
Mean	28.33
Std Dev	13.84

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl



B1L103S, U11-ch120, adc2

calib_packv5_041523_1651.root, FC#0, port C2

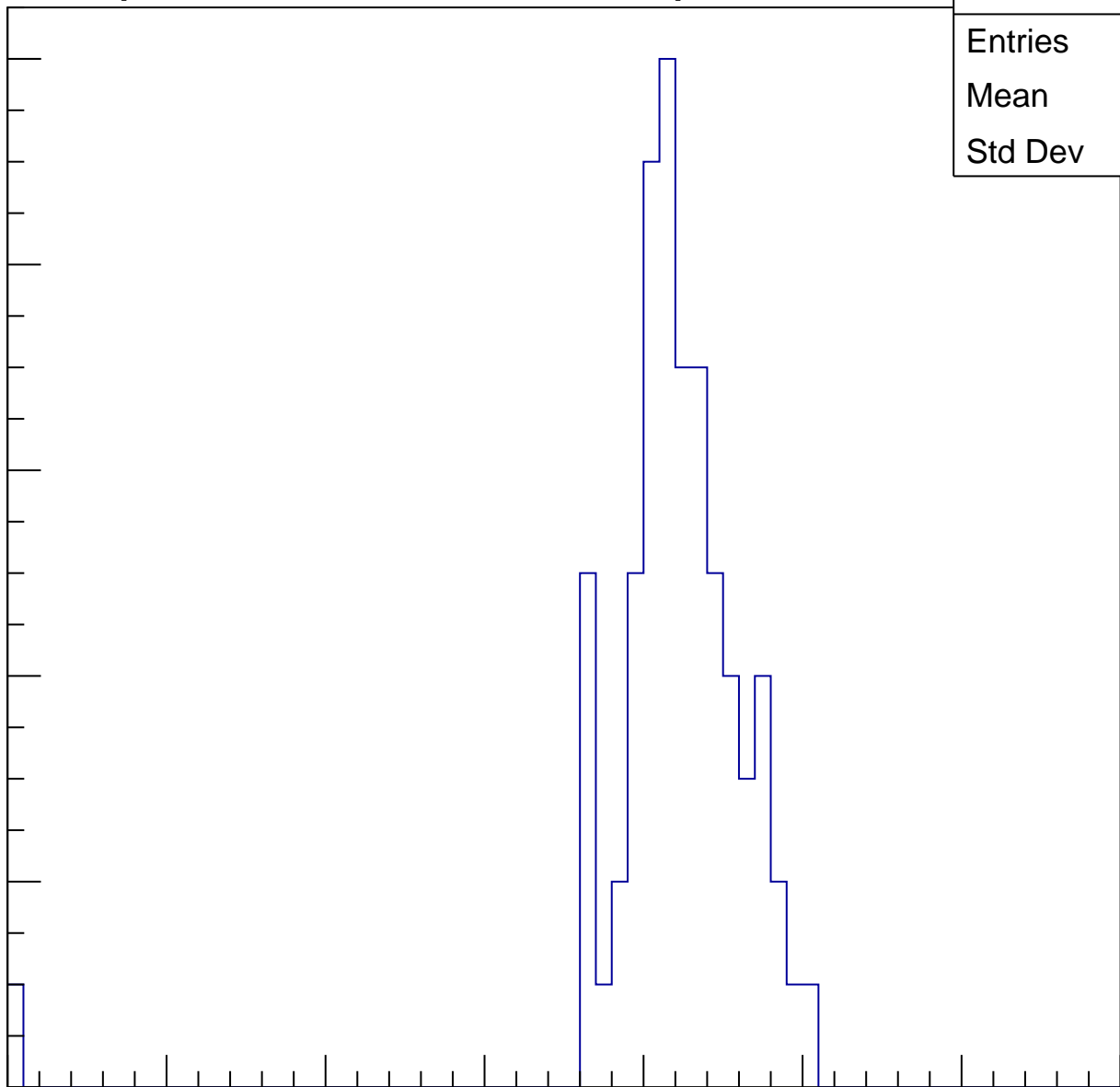
Entries	67
Mean	41.4
Std Dev	6.064

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

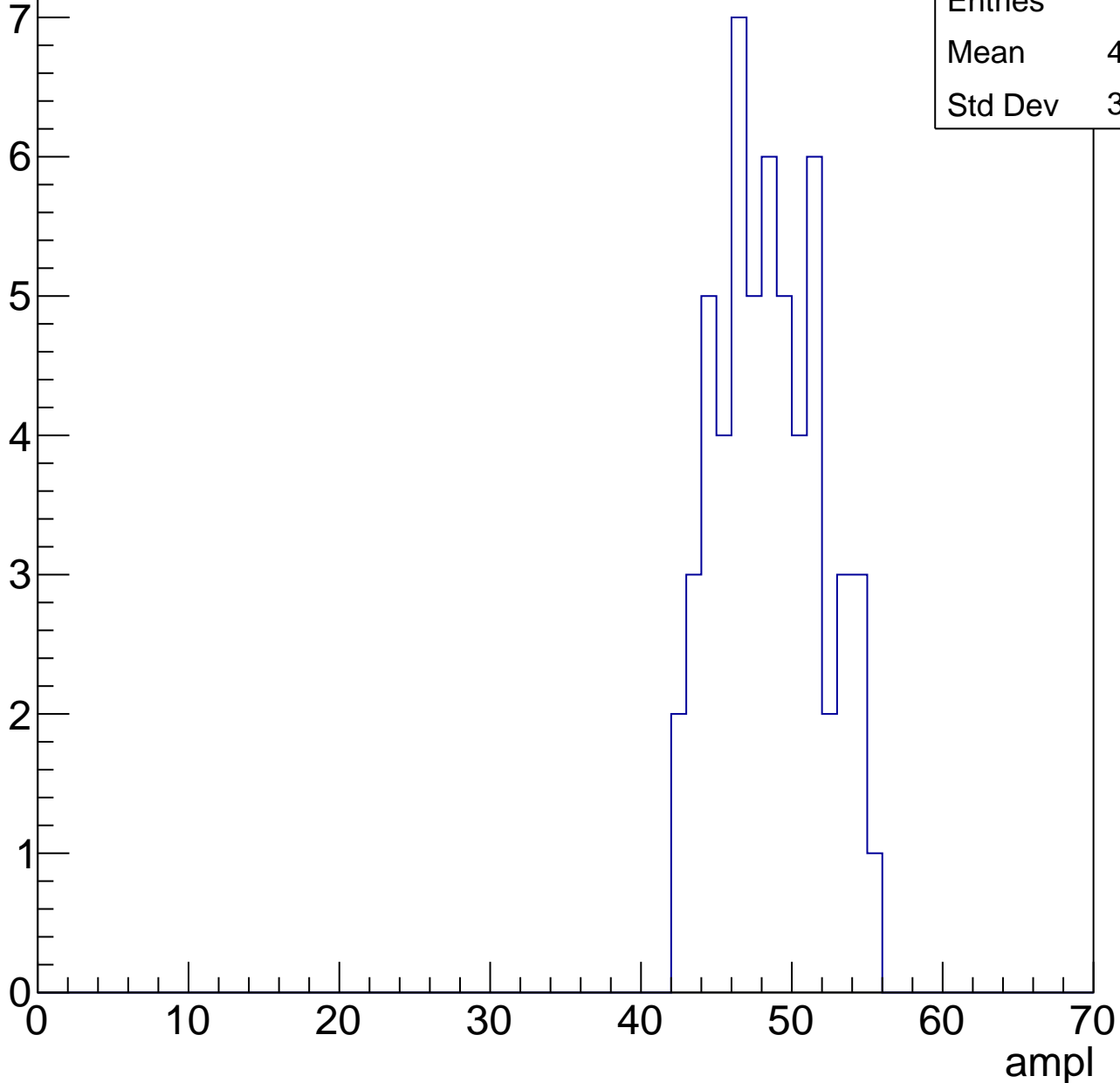


B1L103S, U11-ch120, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	48.02
Std Dev	3.367

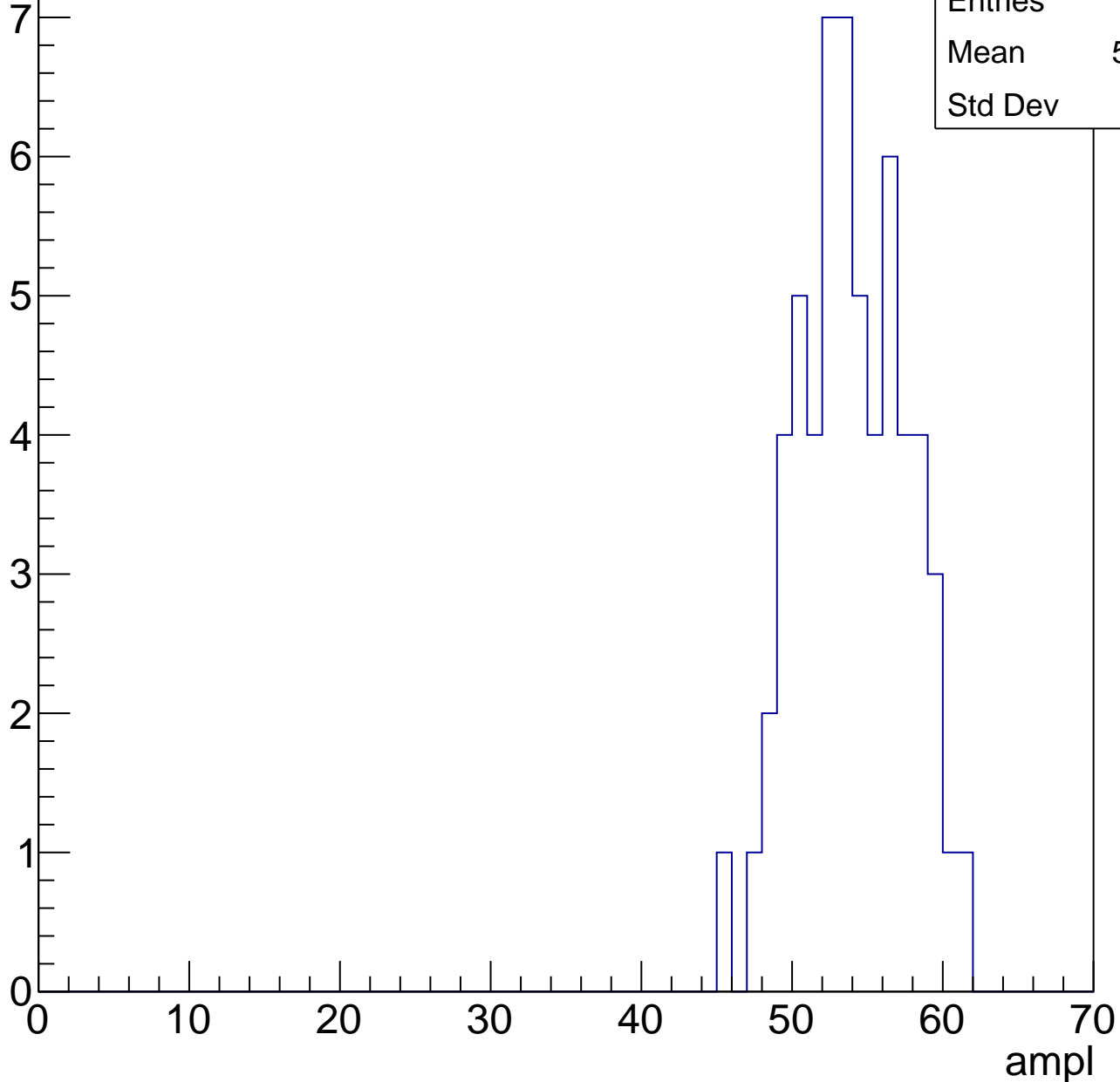


B1L103S, U11-ch120, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	53.51
Std Dev	3.51

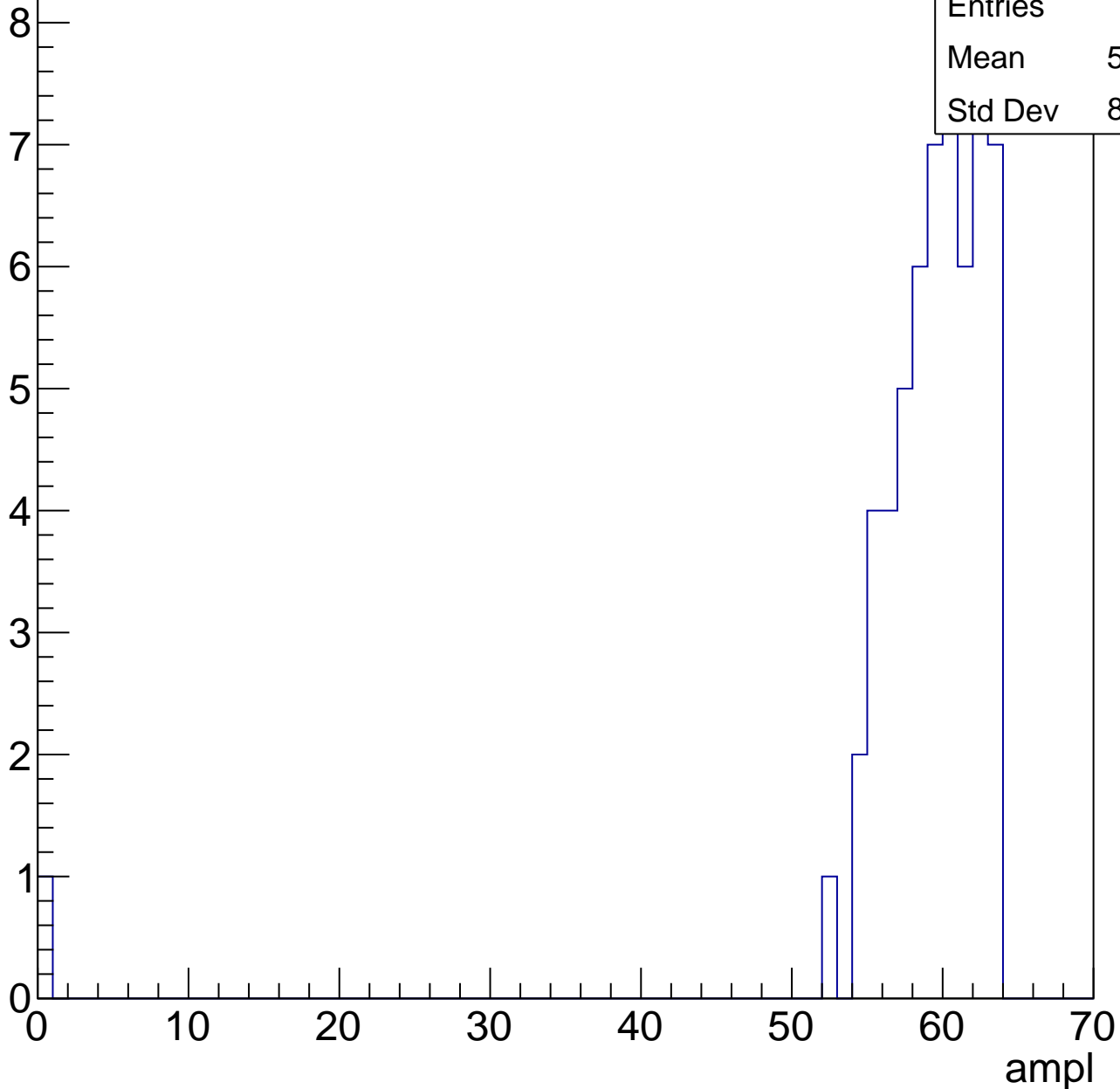


B1L103S, U11-ch120, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	58.19
Std Dev	8.113



B1L103S, U11-ch120, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

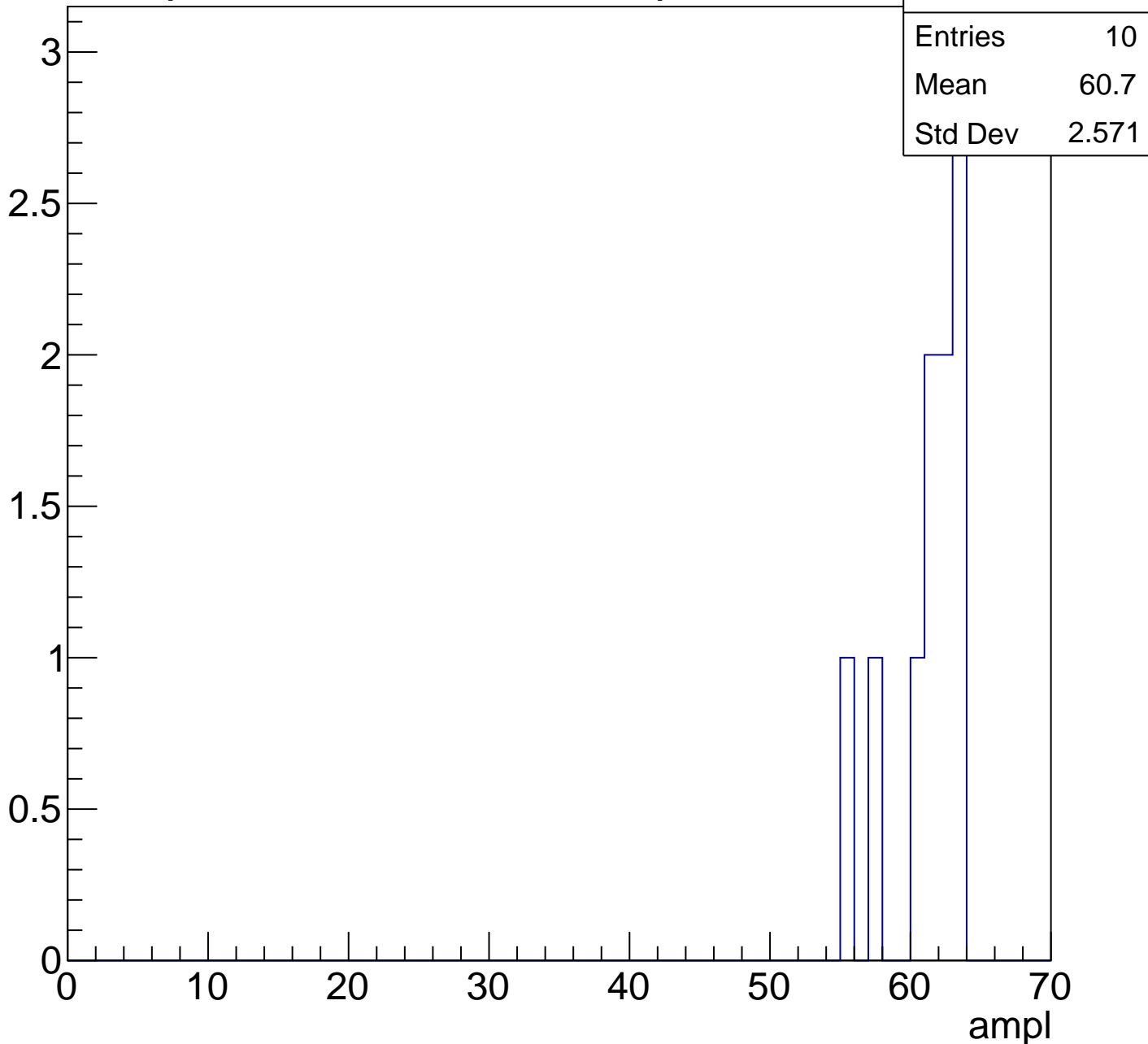
50

60

70

ampl

Entries	10
Mean	60.7
Std Dev	2.571



B1L103S, U11-ch120, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.05
Std Dev	13.29

Entry

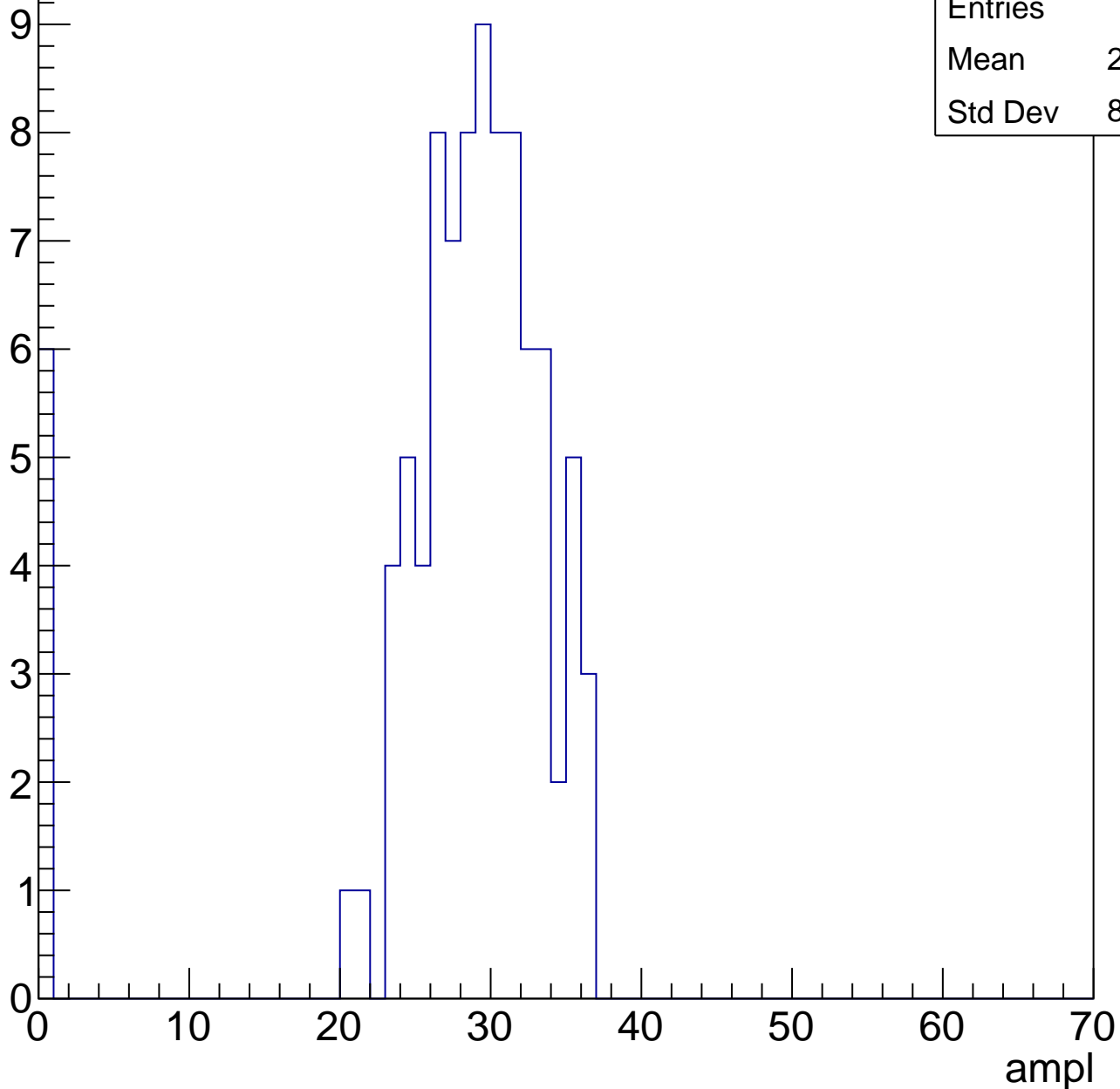


B1L103S, U11-ch121, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	91
Mean	27.08
Std Dev	8.026



B1L103S, U11-ch121, adc1

calib_packv5_041523_1651.root, FC#0, port C2

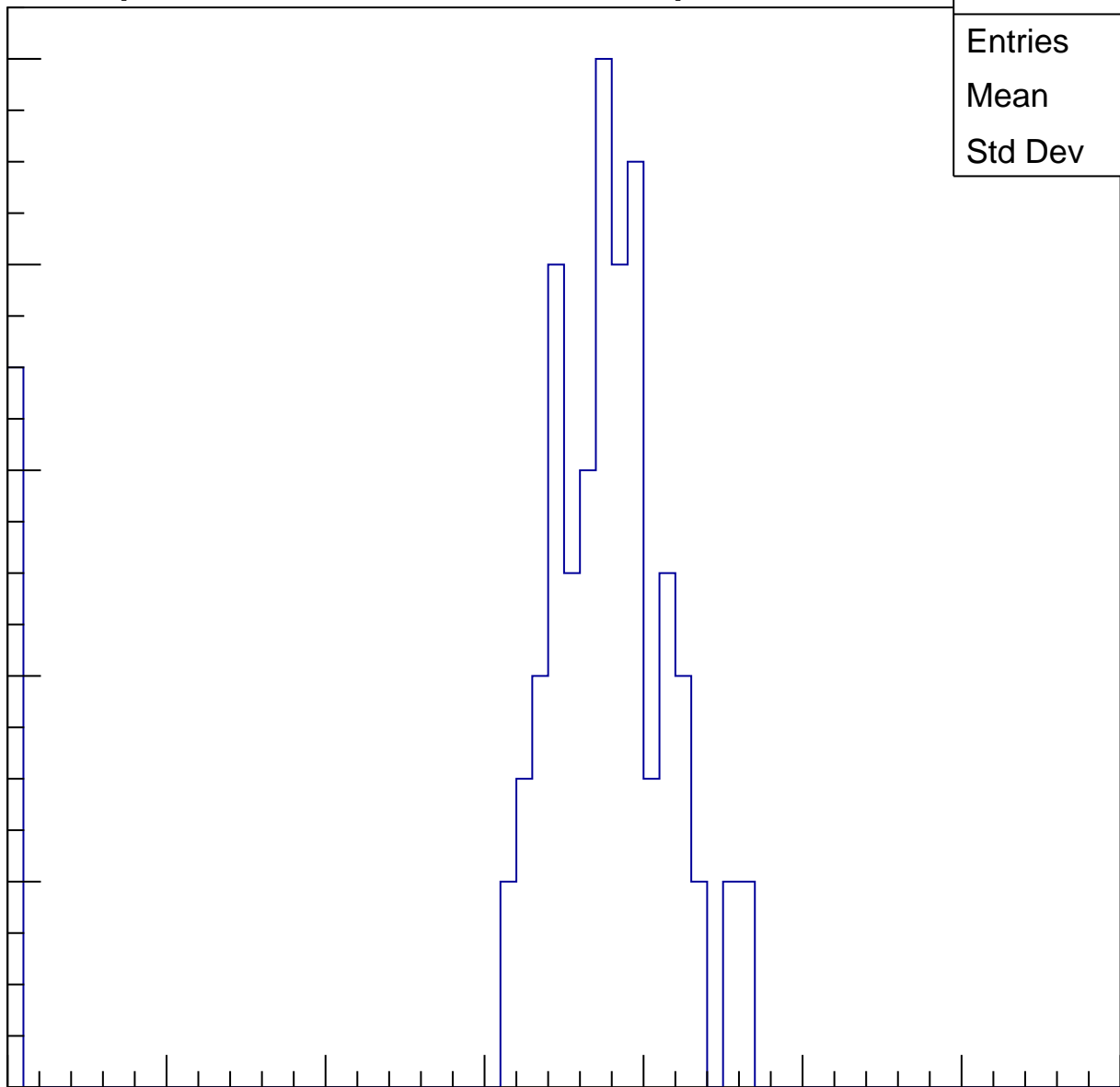
Entries	80
Mean	34.24
Std Dev	11.12

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

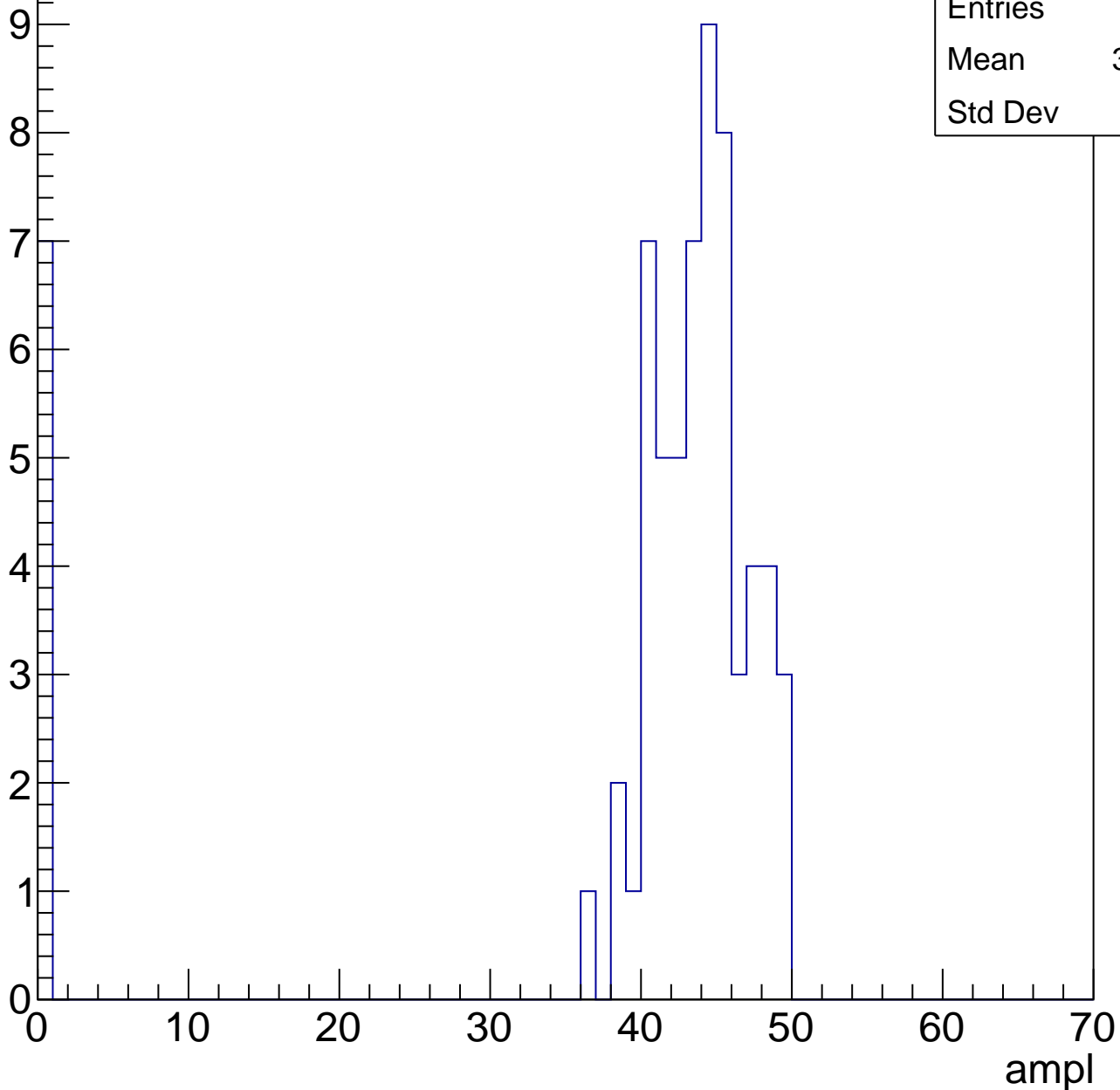


B1L103S, U11-ch121, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

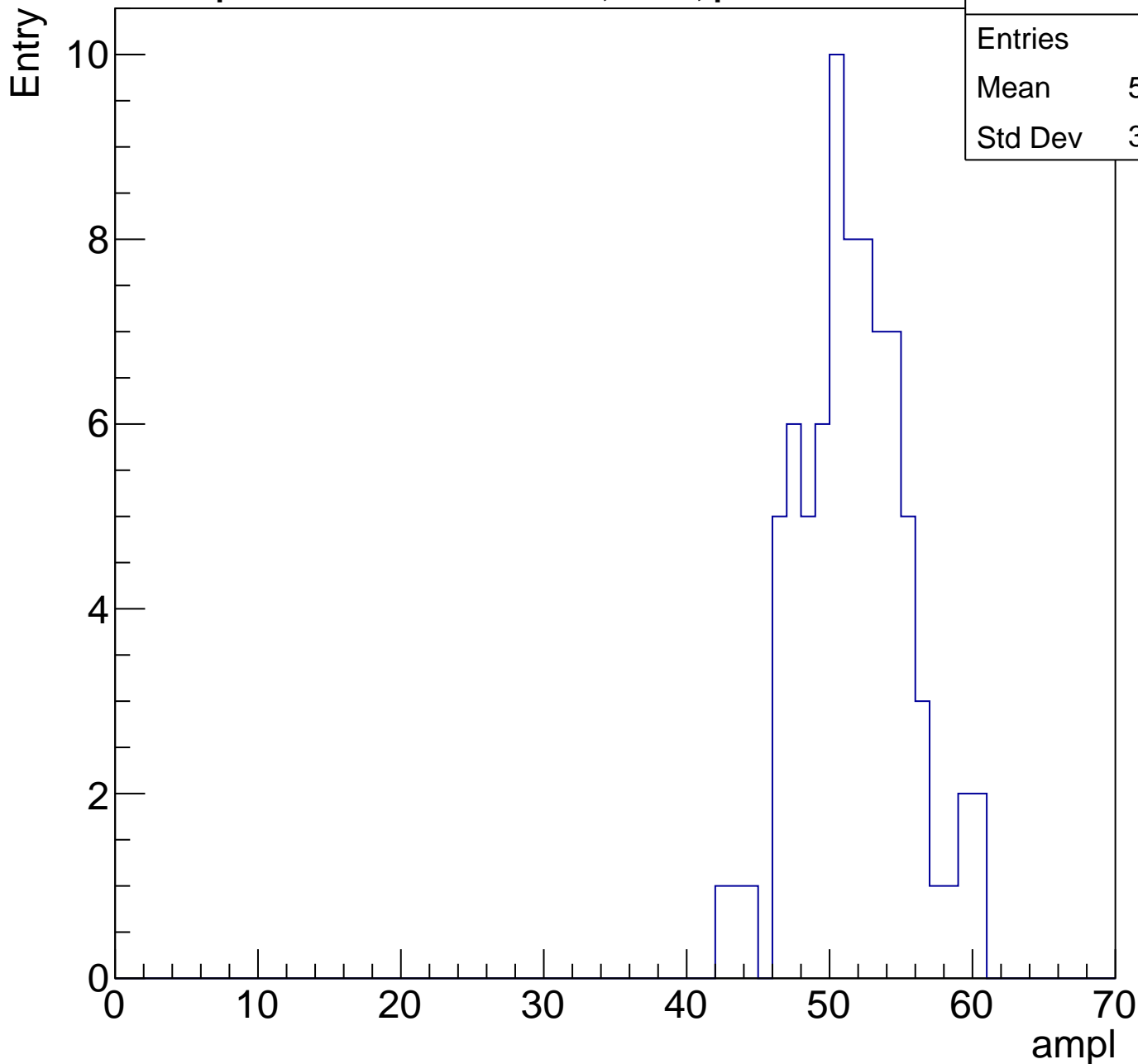
Entries	66
Mean	38.91
Std Dev	13.7



B1L103S, U11-ch121, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	79
Mean	51.19
Std Dev	3.766

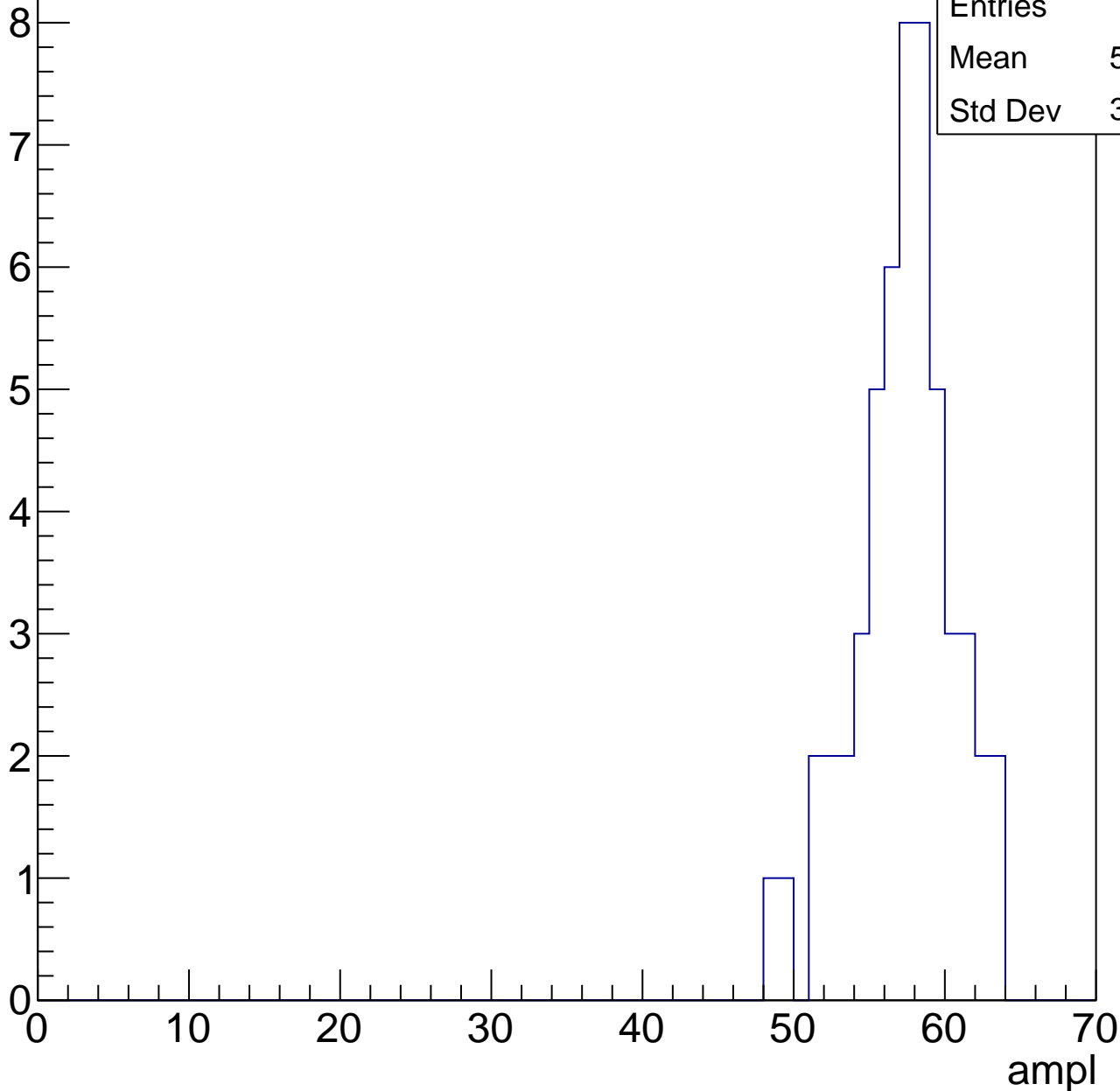


B1L103S, U11-ch121, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	56.79
Std Dev	3.293

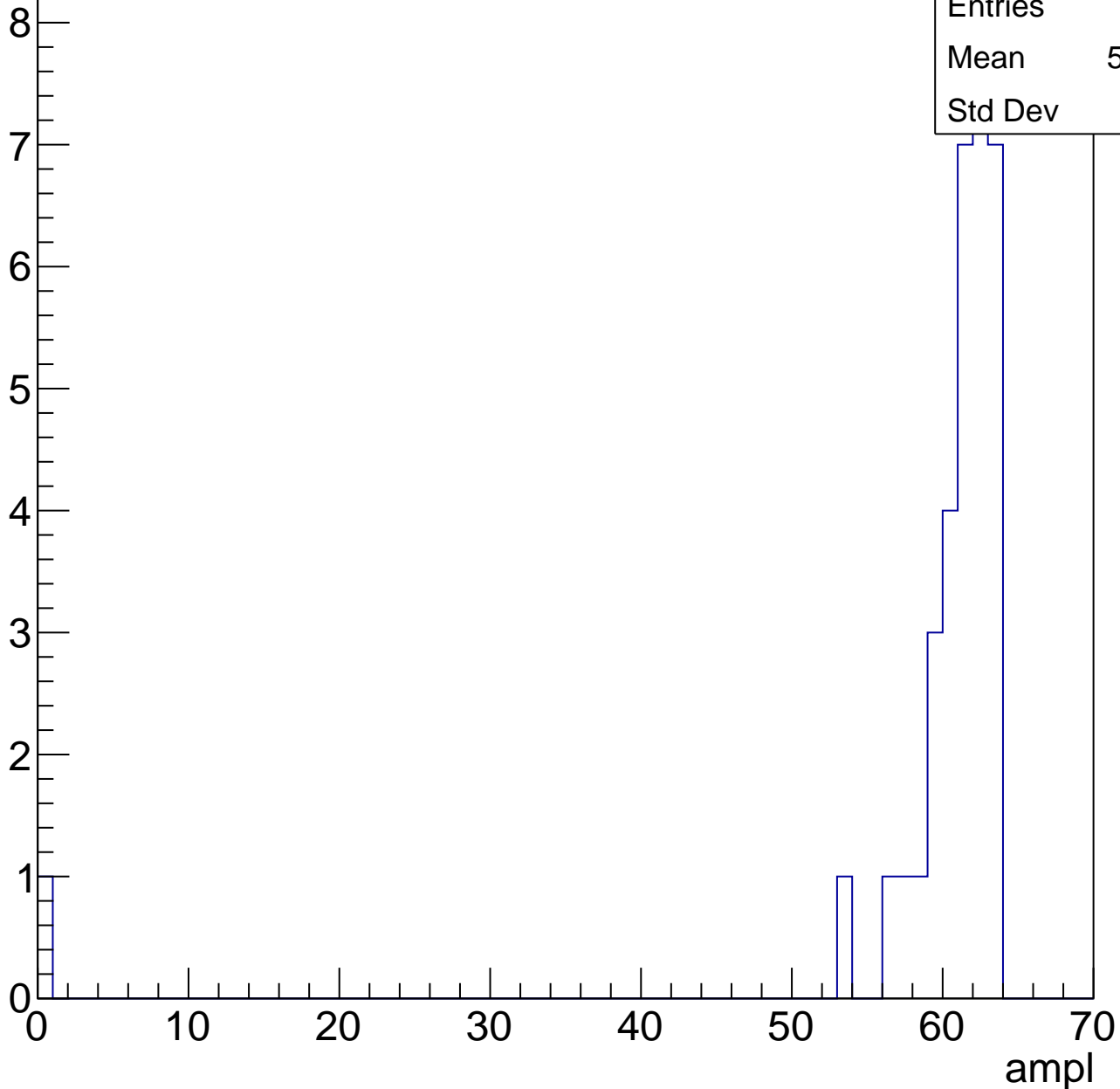


B1L103S, U11-ch121, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

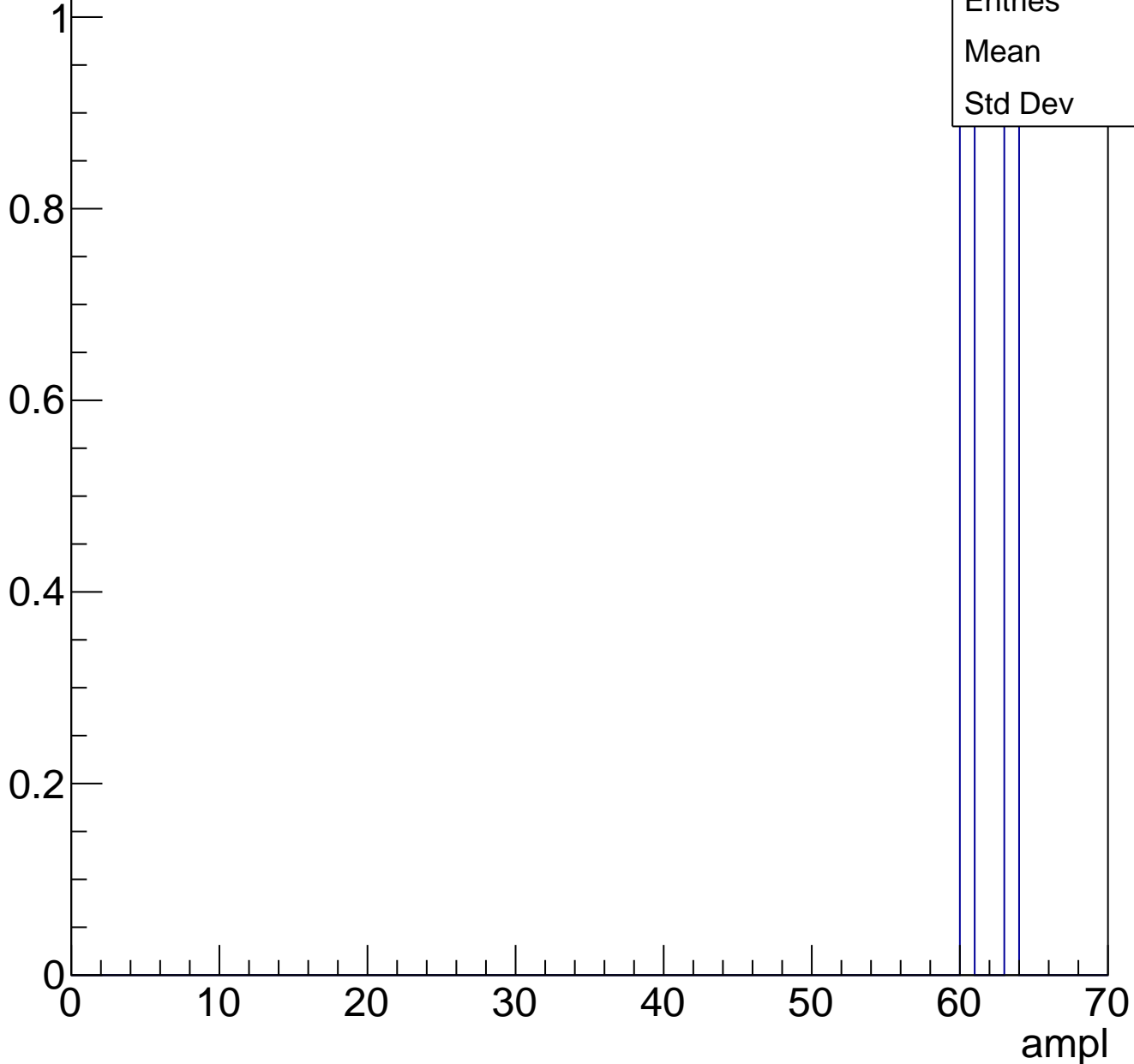
Entries	34
Mean	58.97
Std Dev	10.5



B1L103S, U11-ch121, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

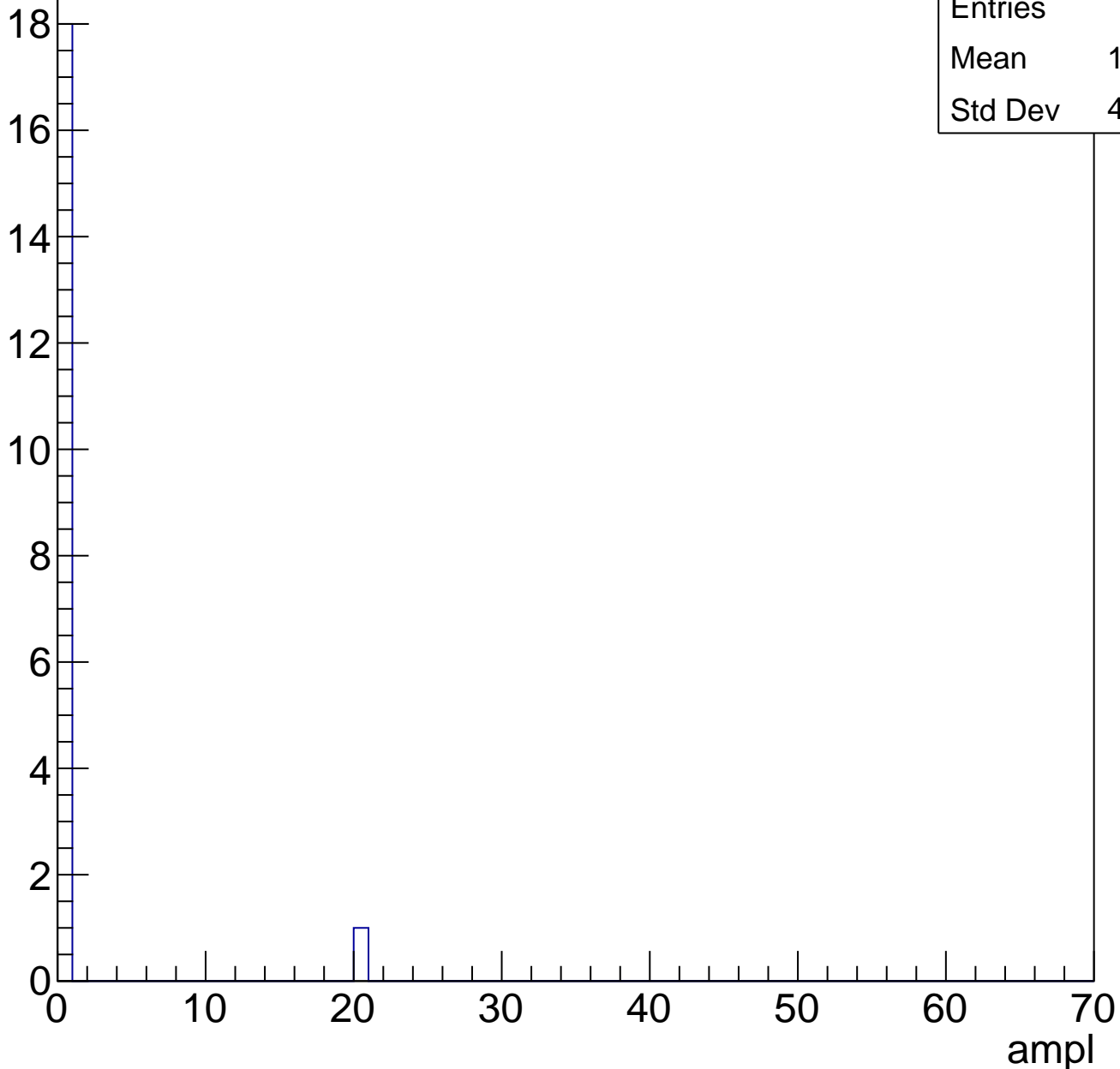


B1L103S, U11-ch121, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.053
Std Dev	4.466

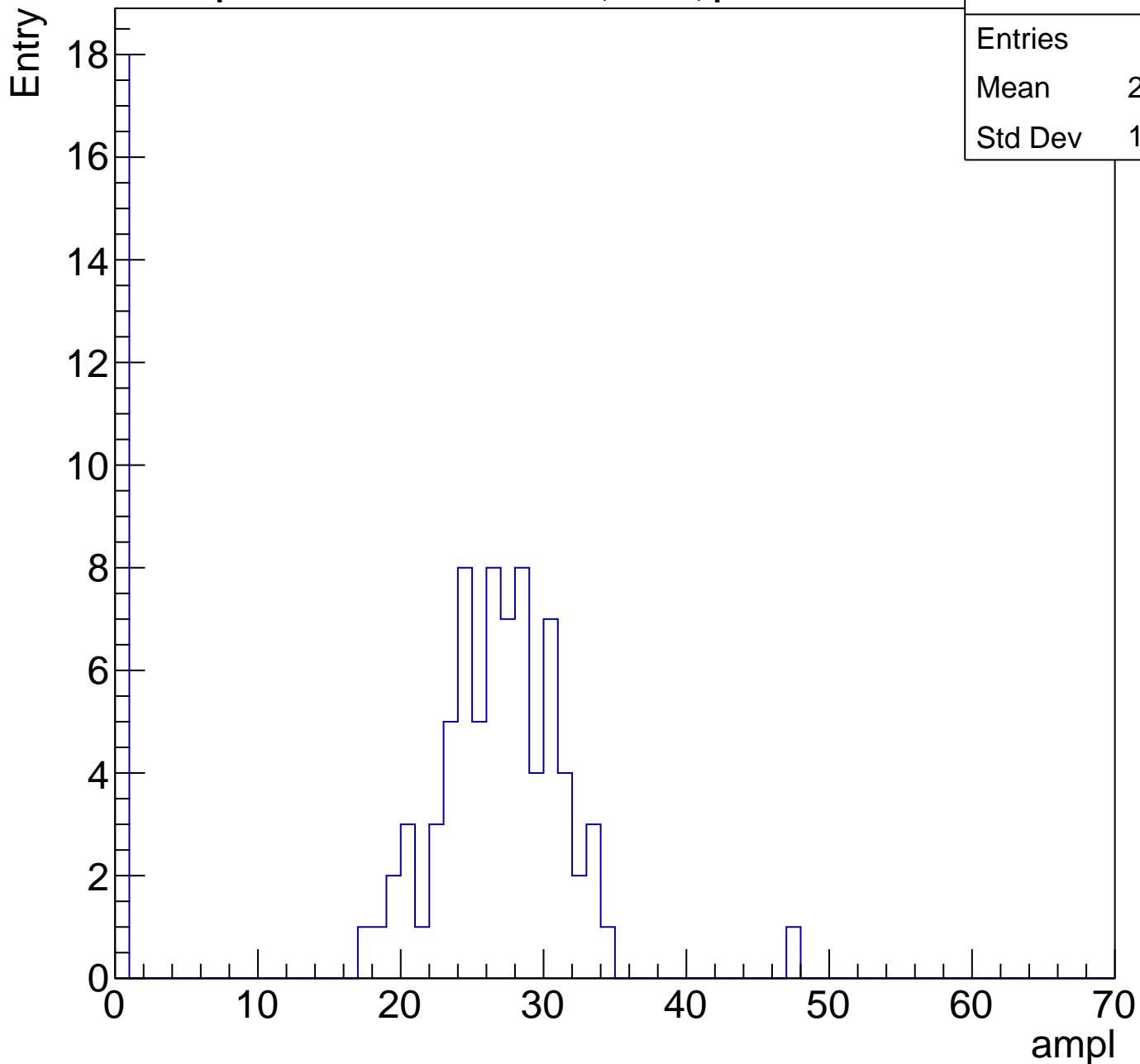
Entry



B1L103S, U11-ch122, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	92
Mean	21.38
Std Dev	11.29

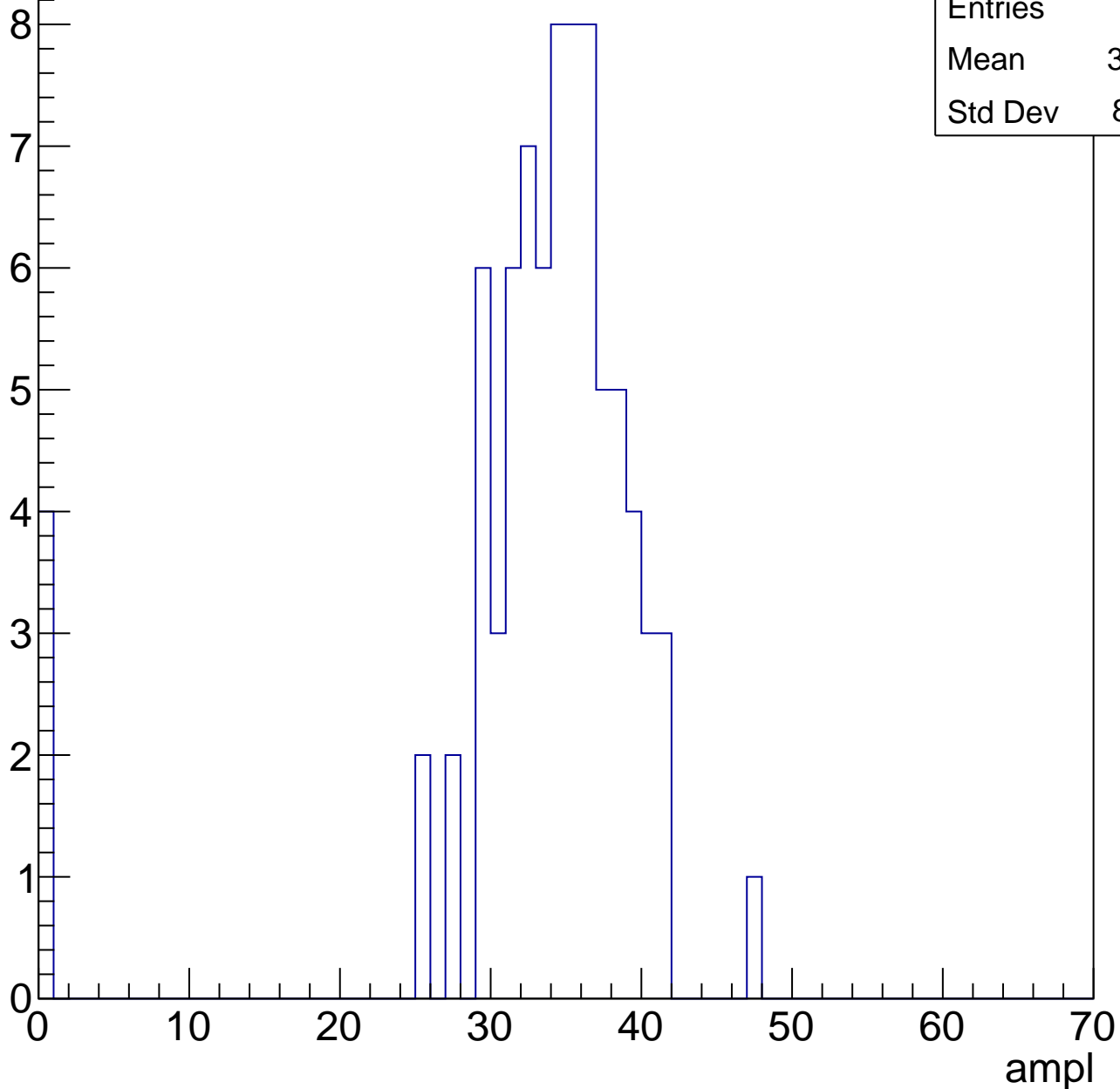


B1L103S, U11-ch122, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	81
Mean	32.56
Std Dev	8.381

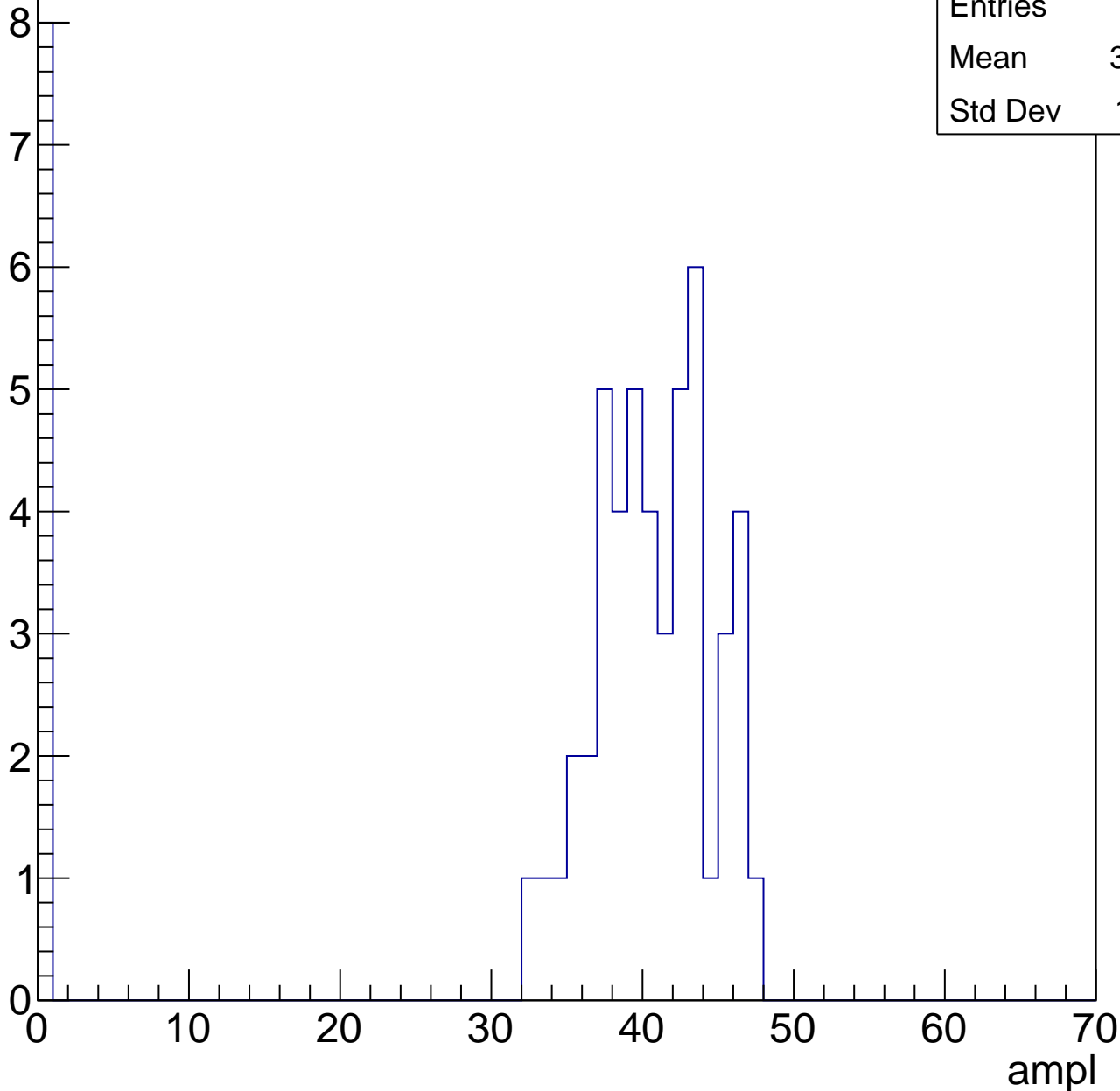


B1L103S, U11-ch122, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	34.54
Std Dev	14.51

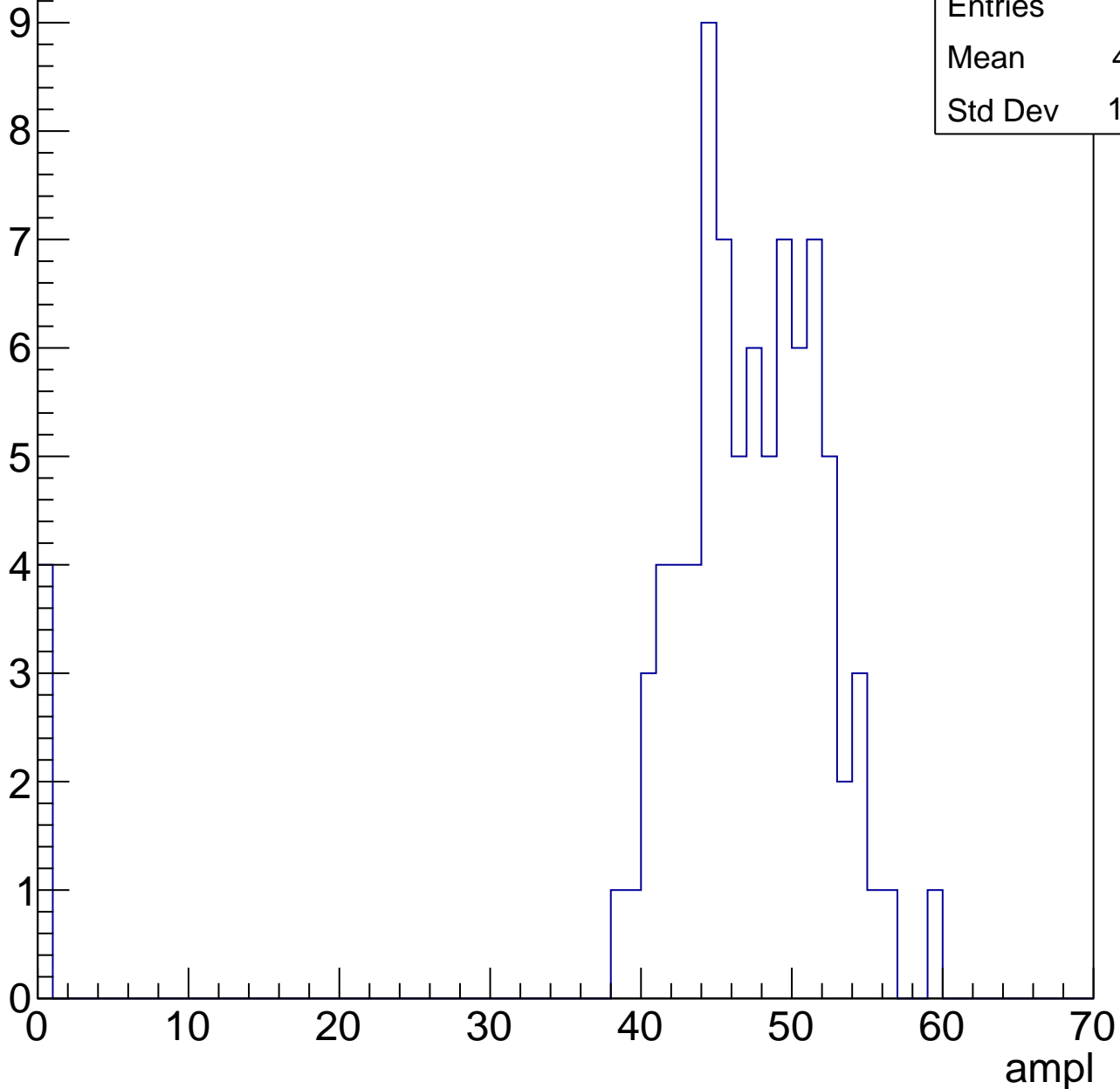


B1L103S, U11-ch122, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	86
Mean	44.91
Std Dev	10.79

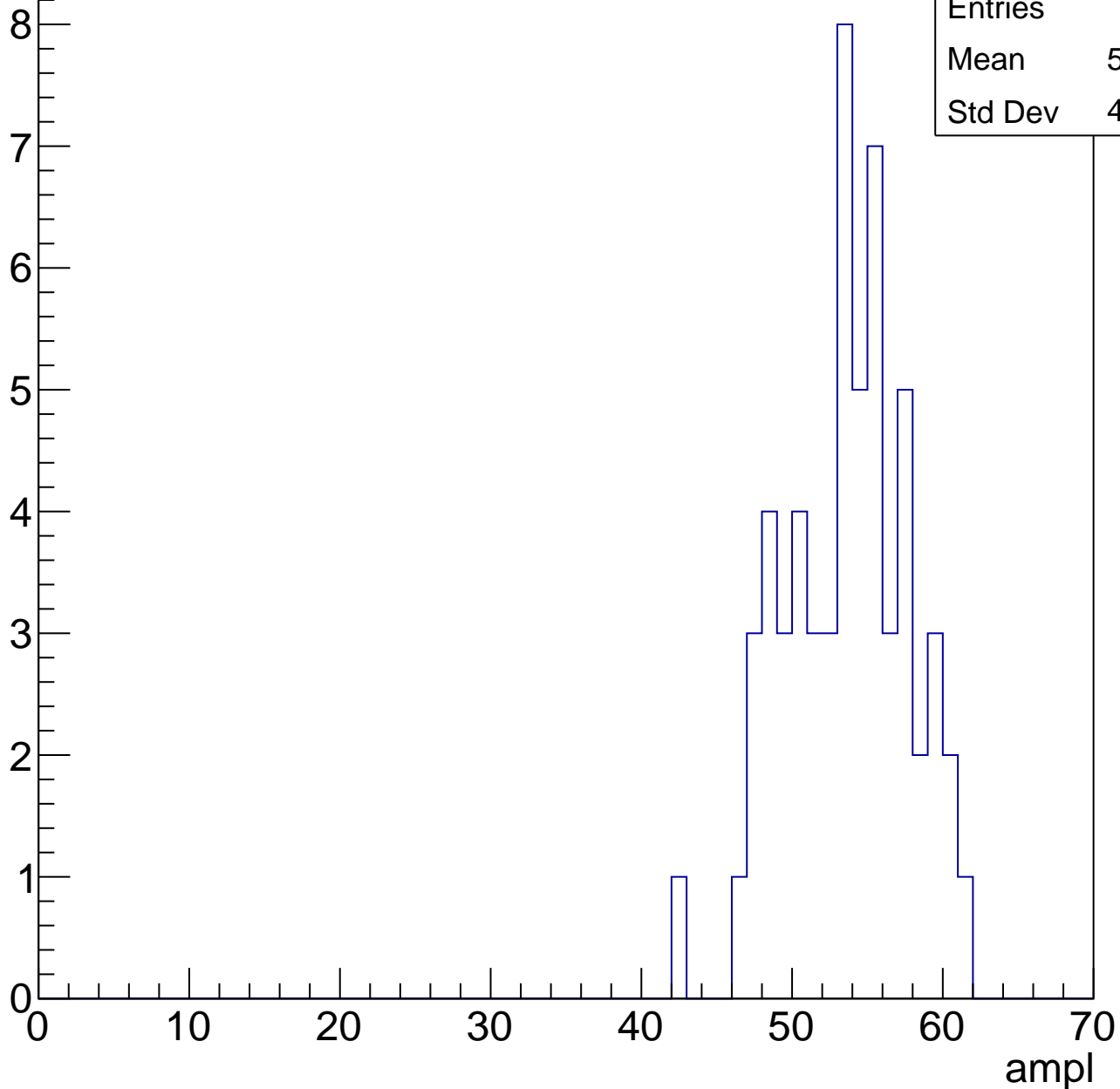


B1L103S, U11-ch122, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	53.16
Std Dev	4.016

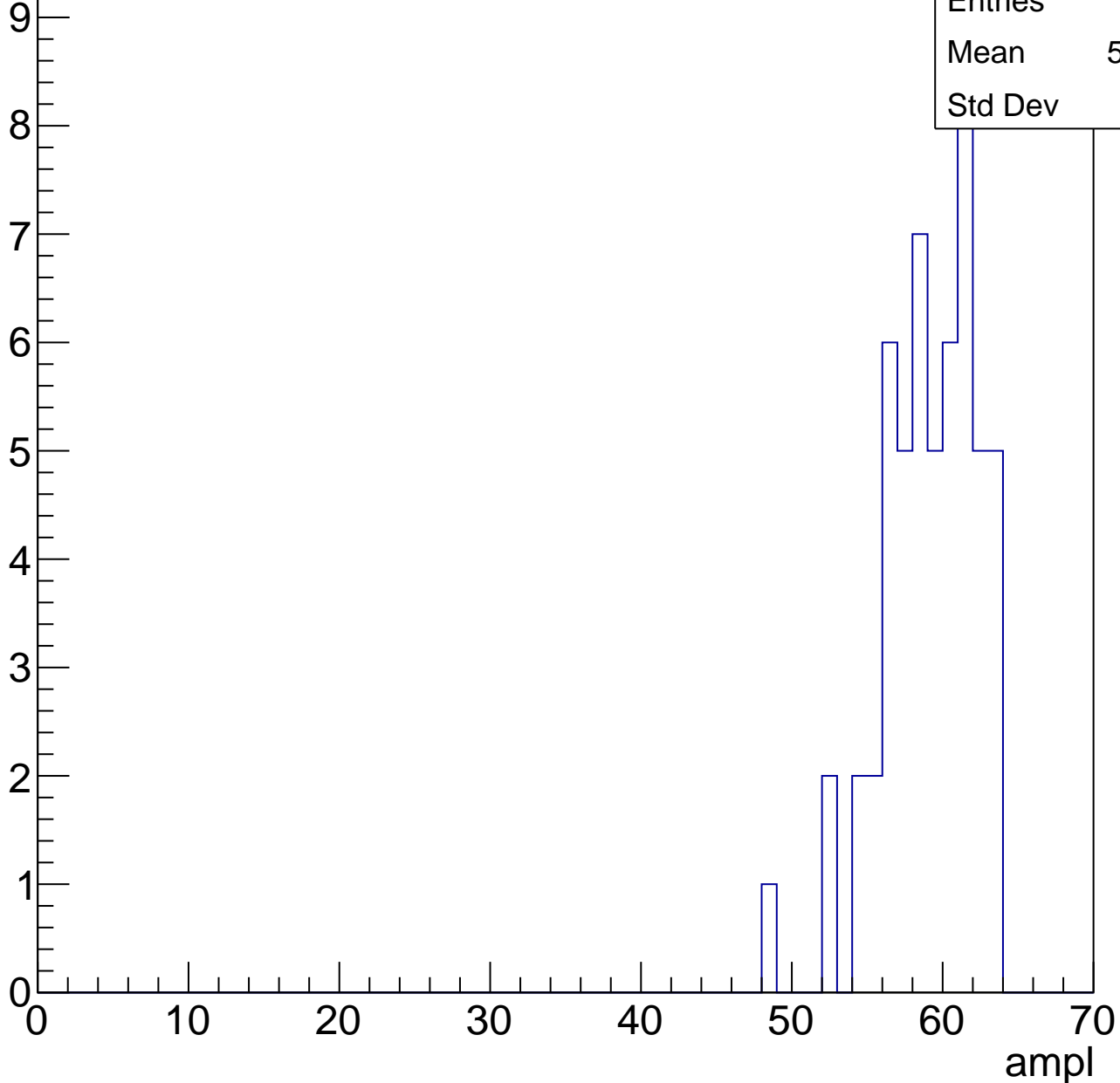


B1L103S, U11-ch122, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	58.65
Std Dev	3.14

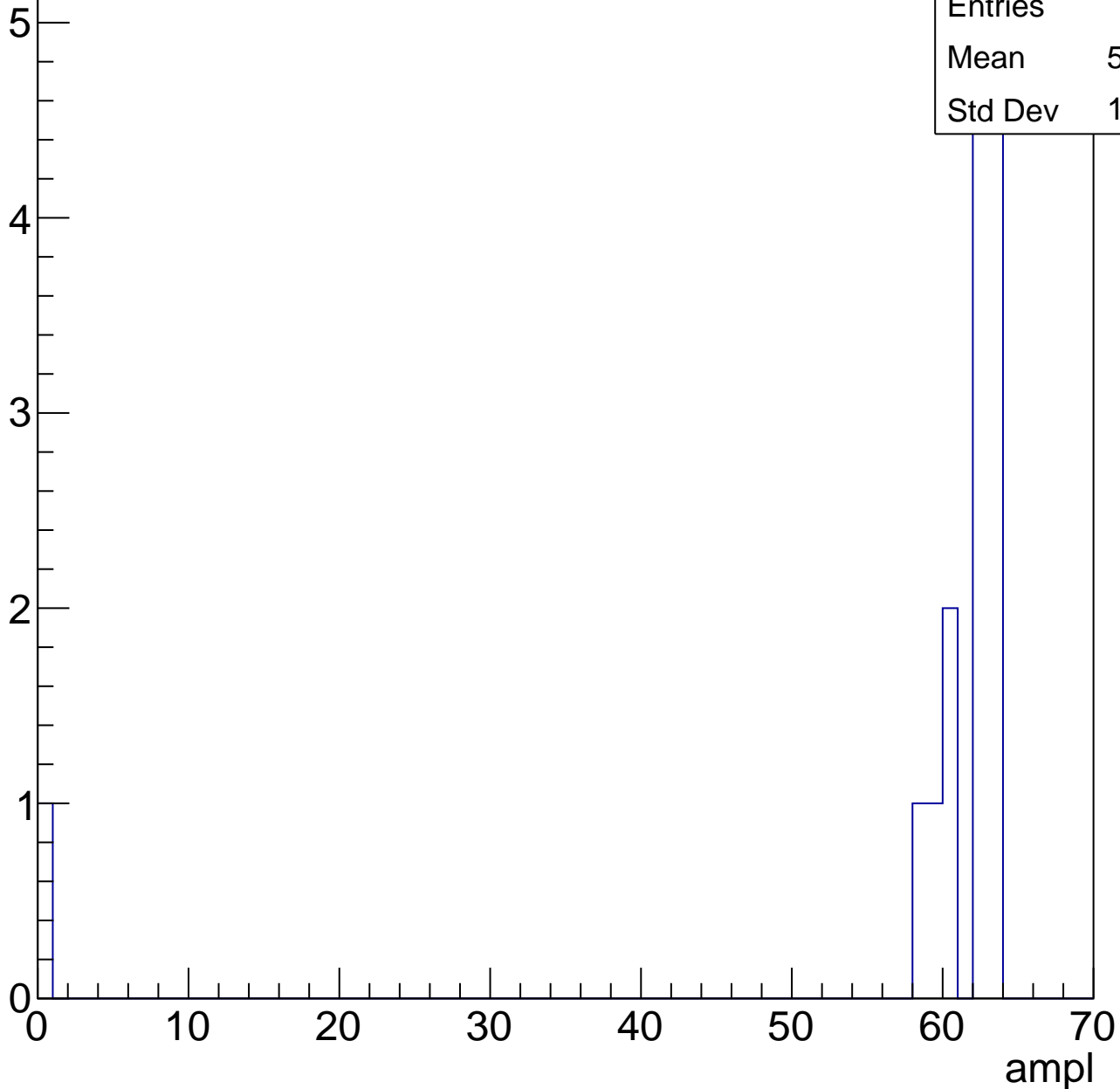


B1L103S, U11-ch122, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	15
Mean	57.47
Std Dev	15.44

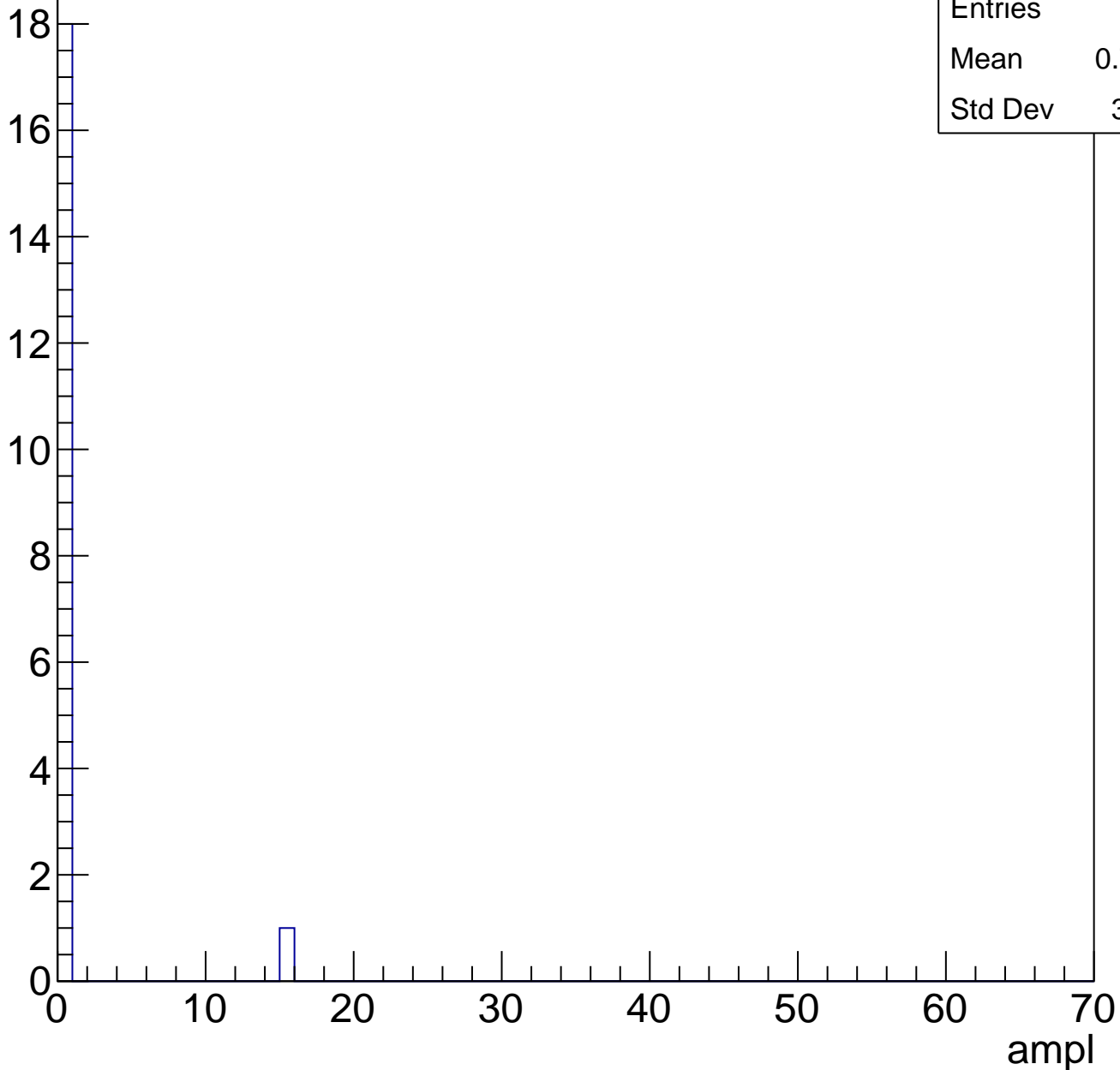


B1L103S, U11-ch122, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	0.7895
Std Dev	3.349

Entry

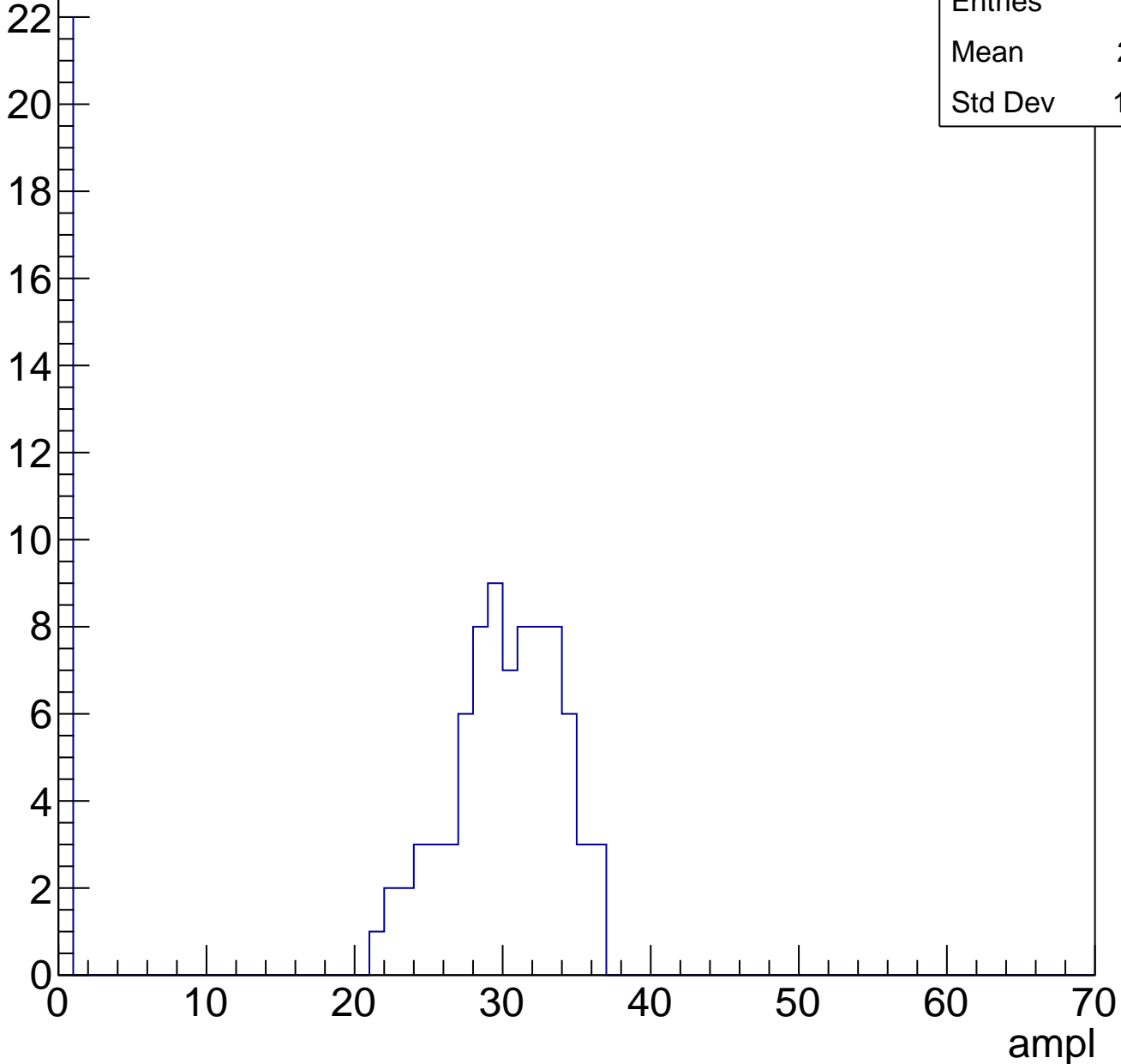


B1L103S, U11-ch123, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	102
Mean	23.31
Std Dev	12.63

Entry



B1L103S, U11-ch123, adc1

calib_packv5_041523_1651.root, FC#0, port C2

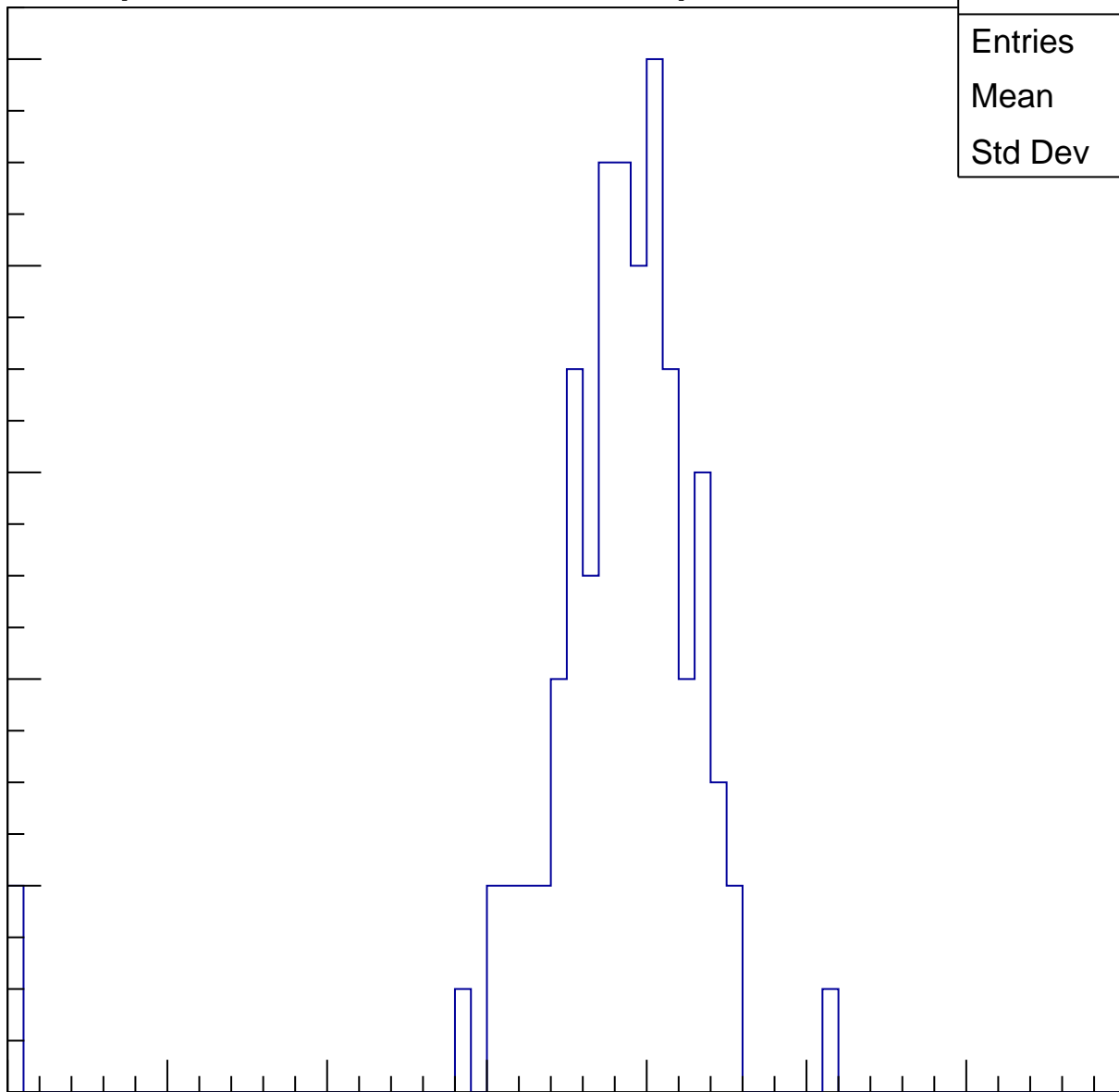
Entries	86
Mean	37.37
Std Dev	6.953

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

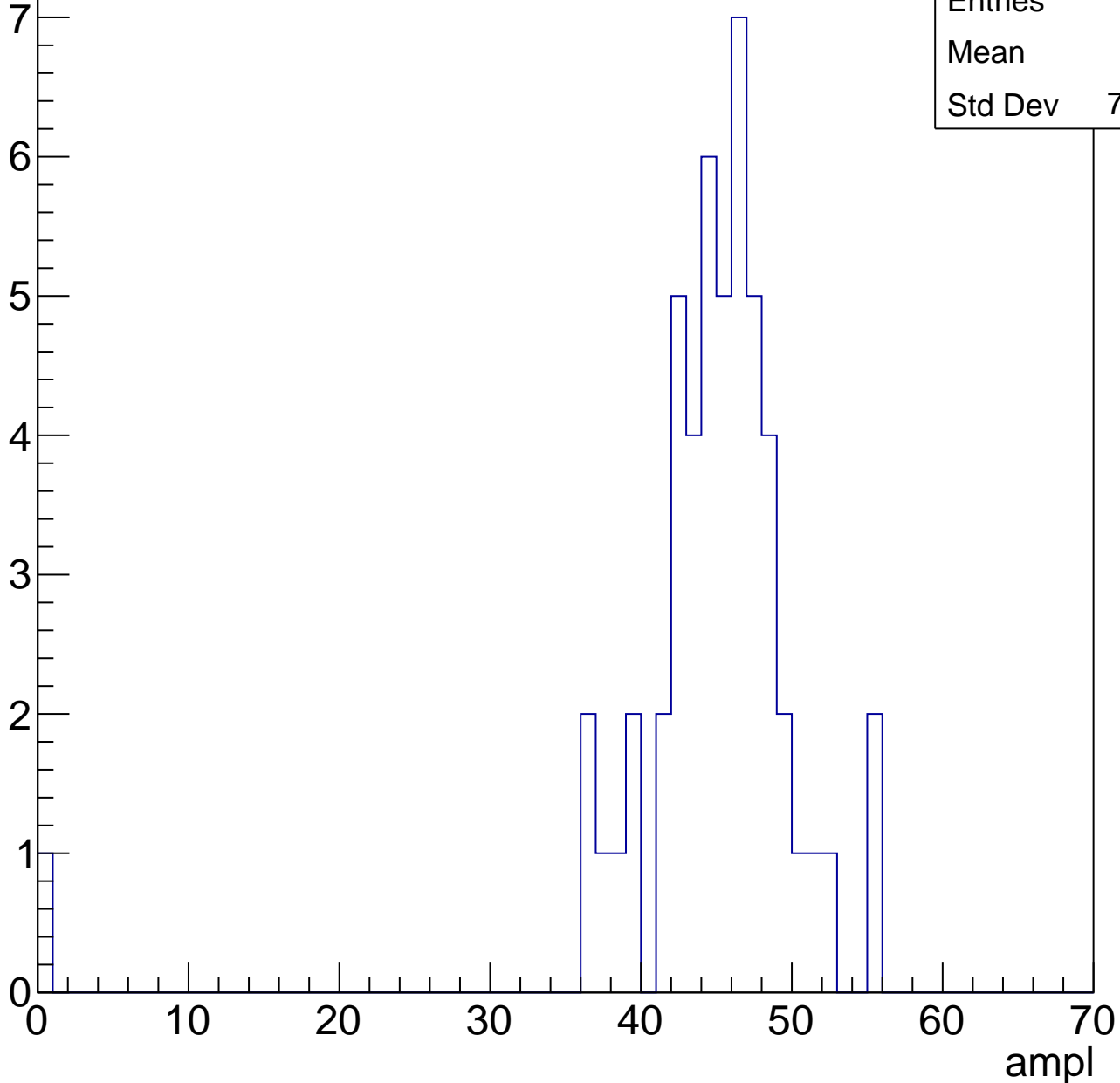


B1L103S, U11-ch123, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	44
Std Dev	7.369

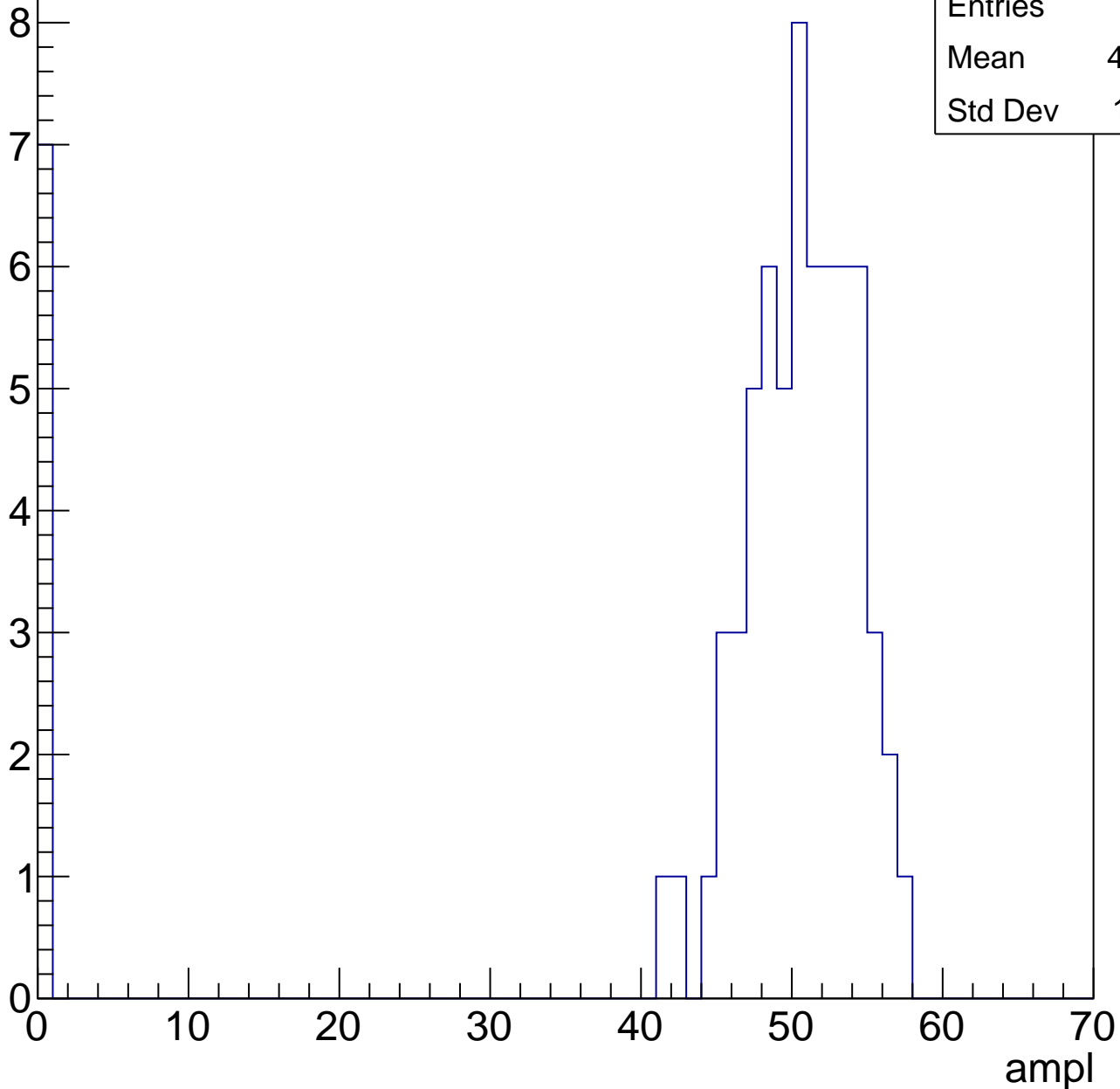


B1L103S, U11-ch123, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	45.17
Std Dev	15.41

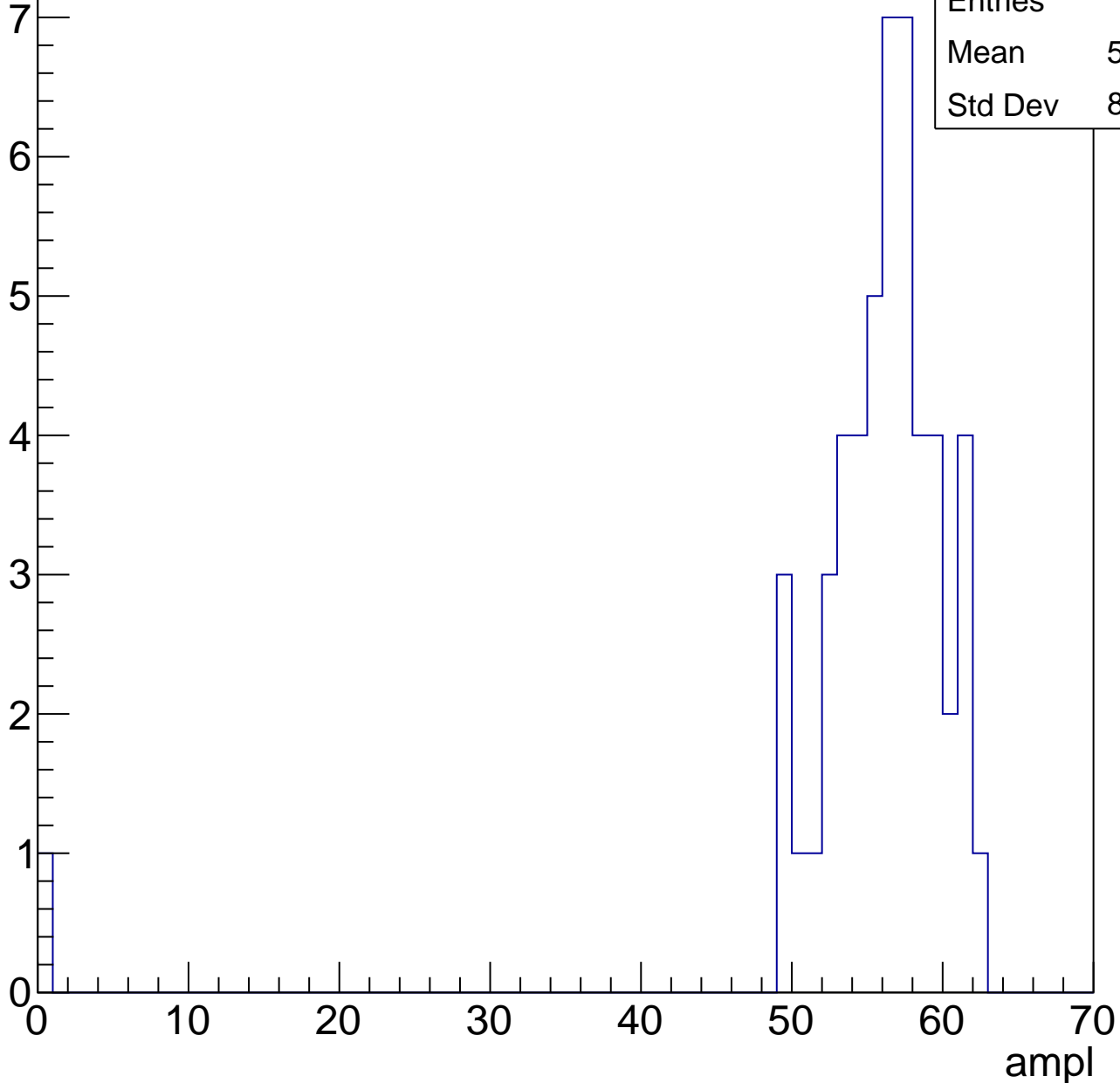


B1L103S, U11-ch123, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	54.75
Std Dev	8.397

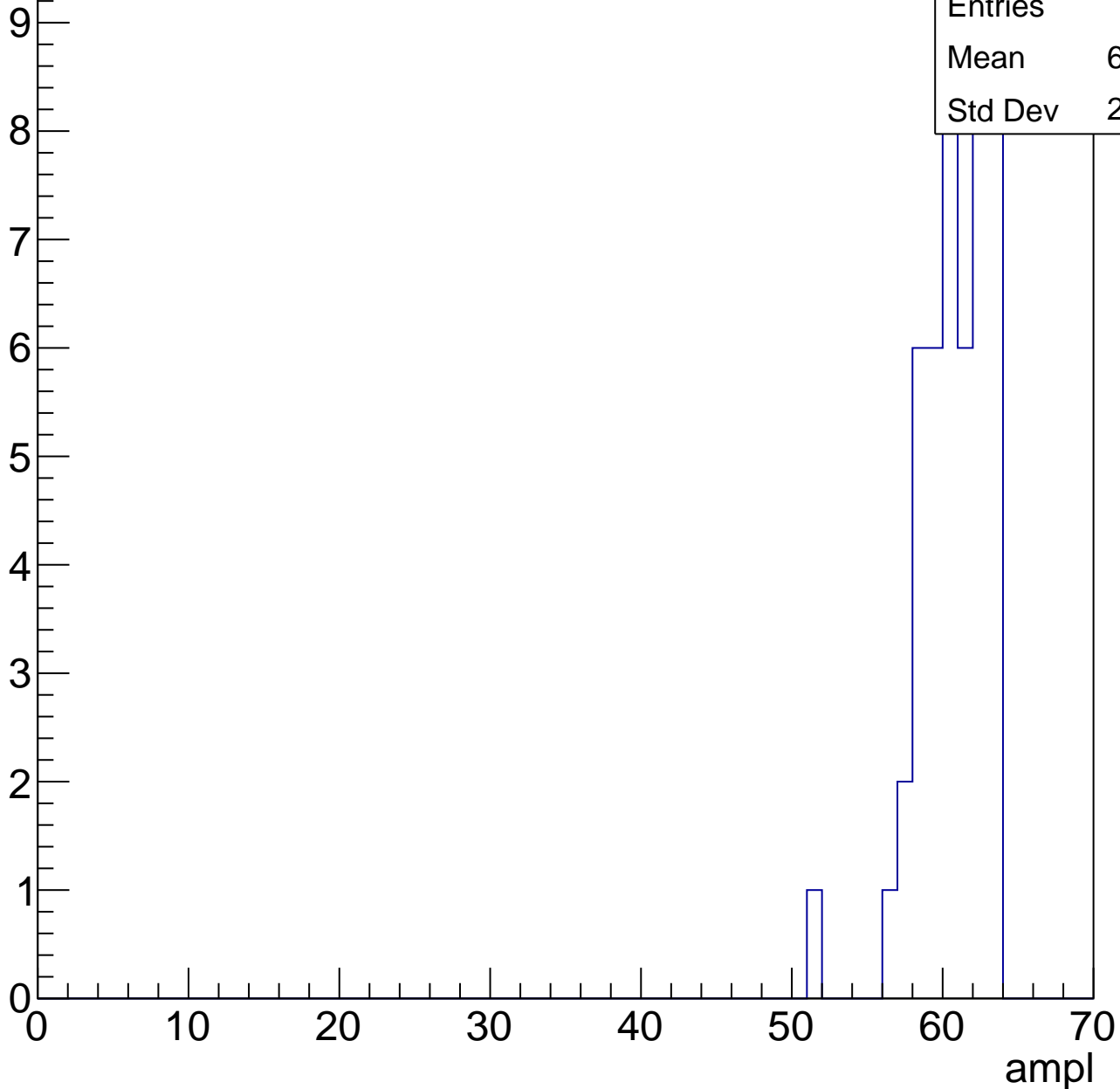


B1L103S, U11-ch123, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	48
Mean	60.29
Std Dev	2.345



B1L103S, U11-ch123, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U11-ch123, adc7

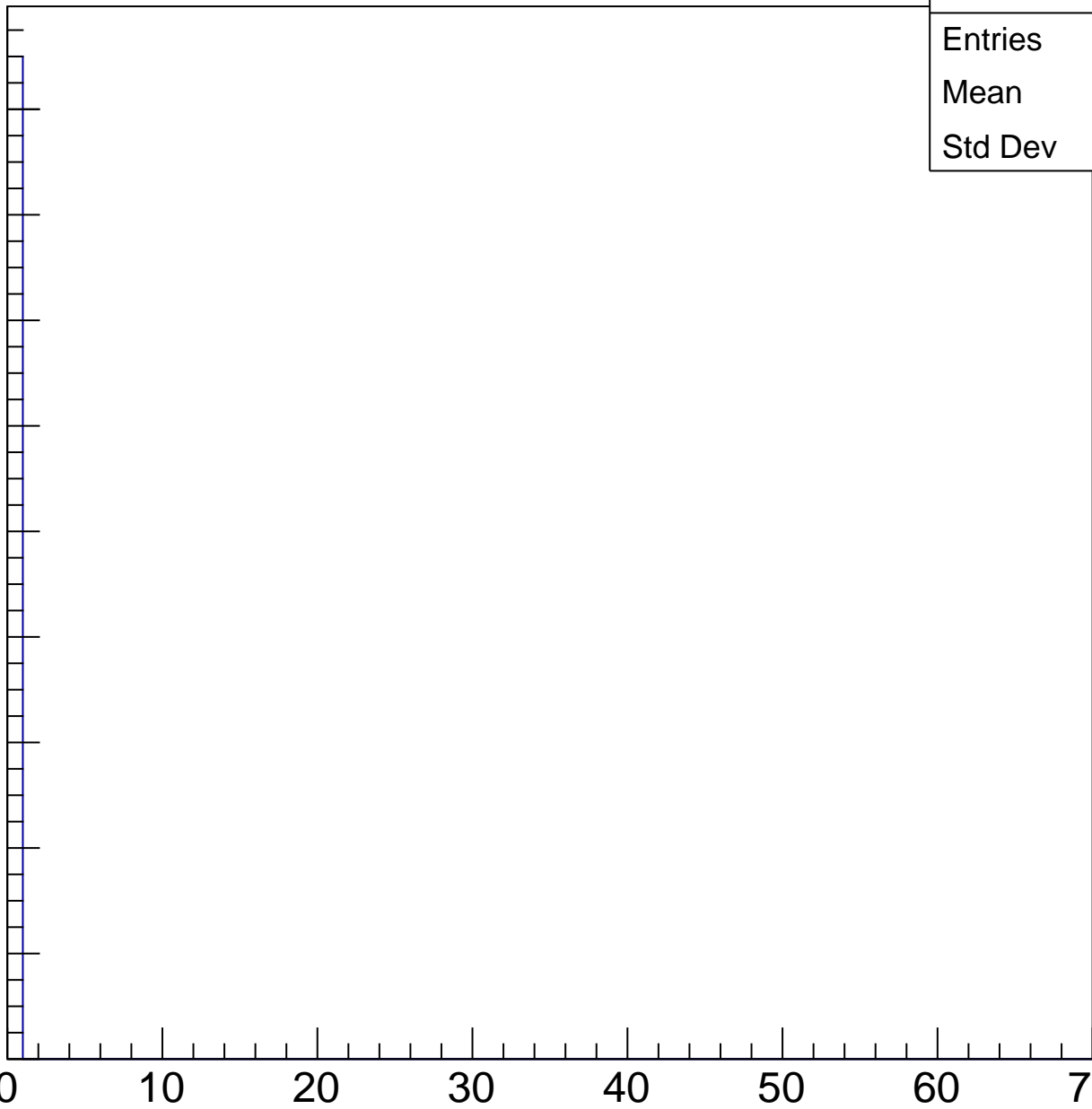
calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

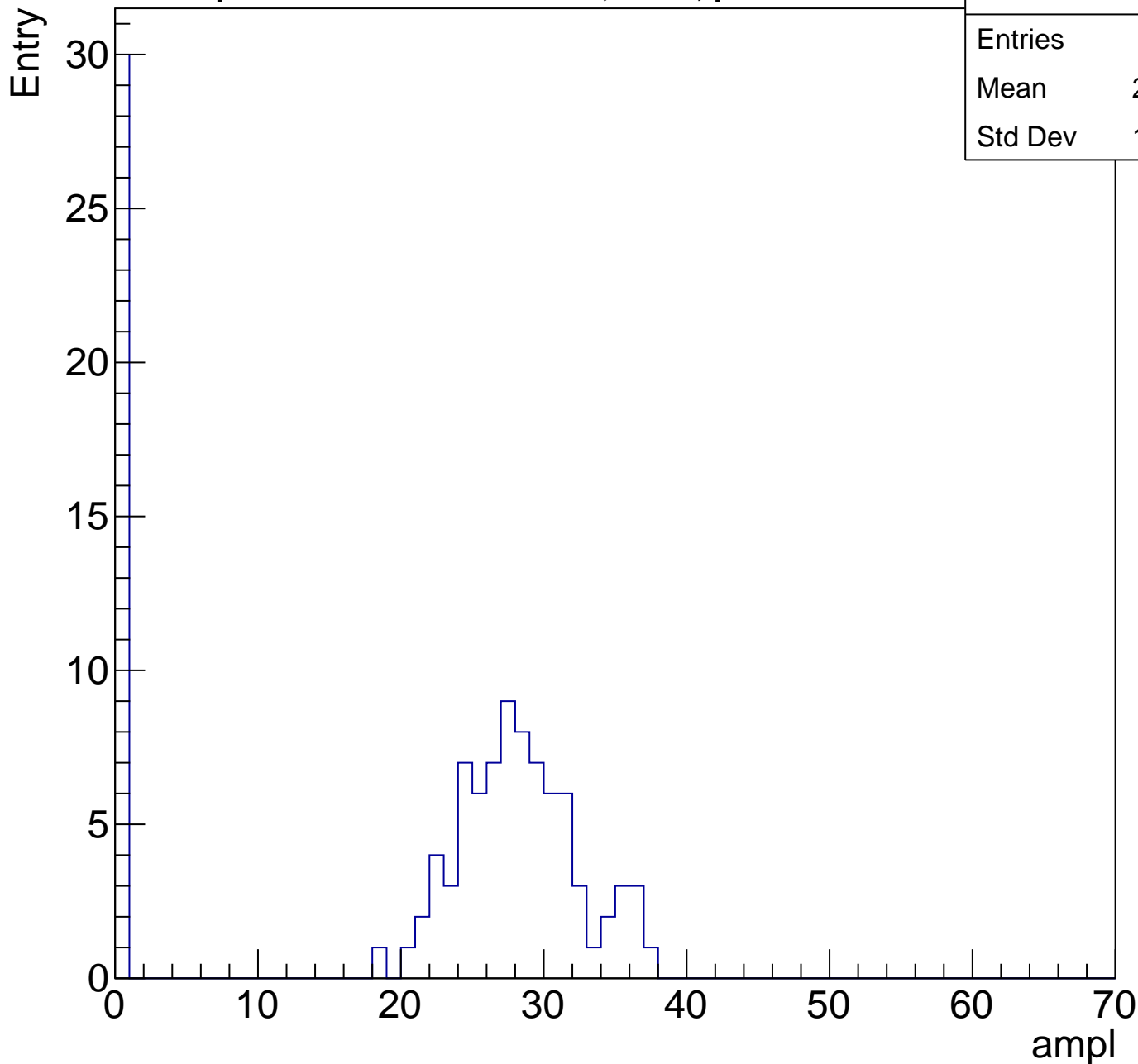
ampl



B1L103S, U11-ch124, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	110
Mean	20.18
Std Dev	12.84

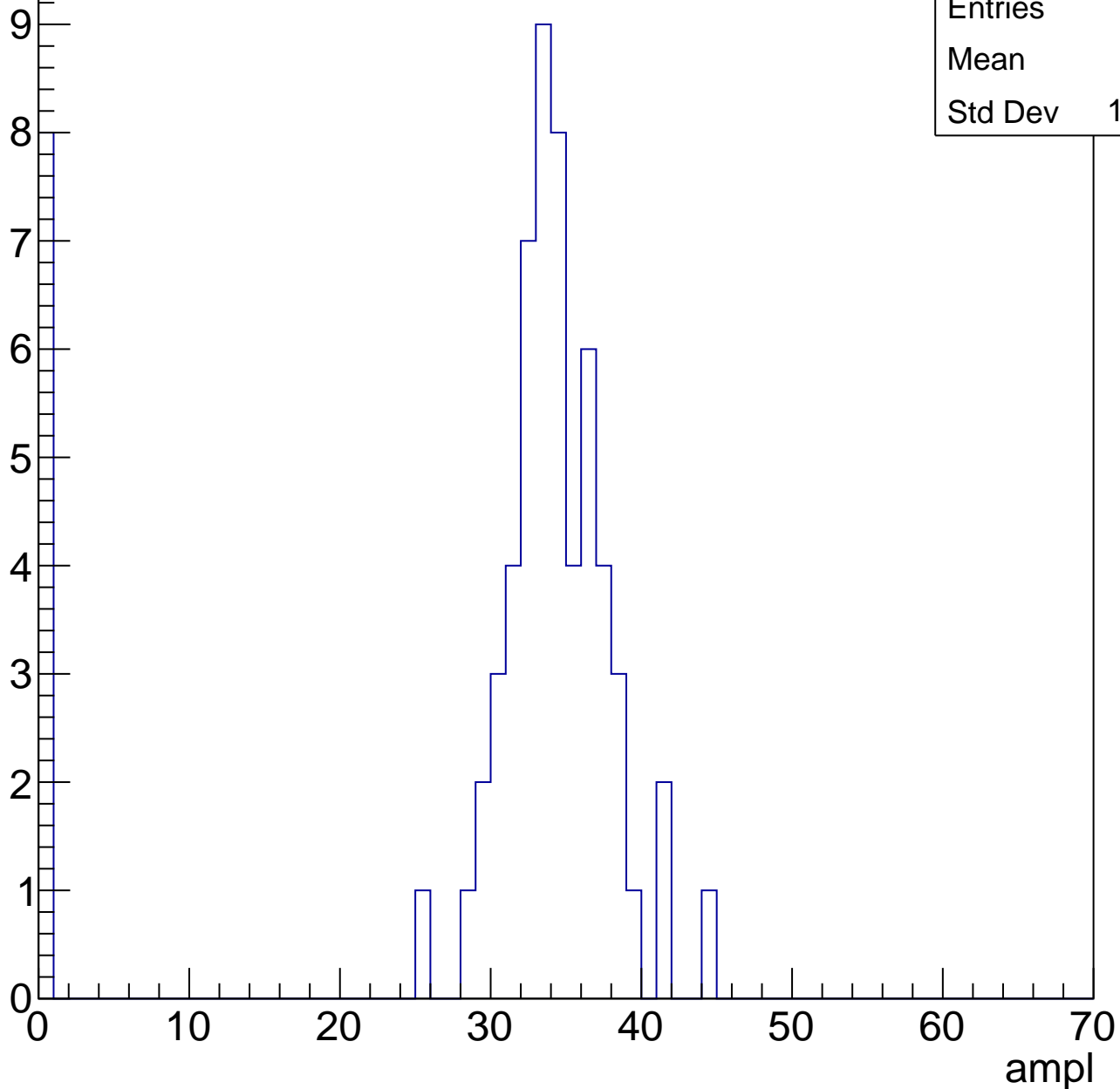


B1L103S, U11-ch124, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

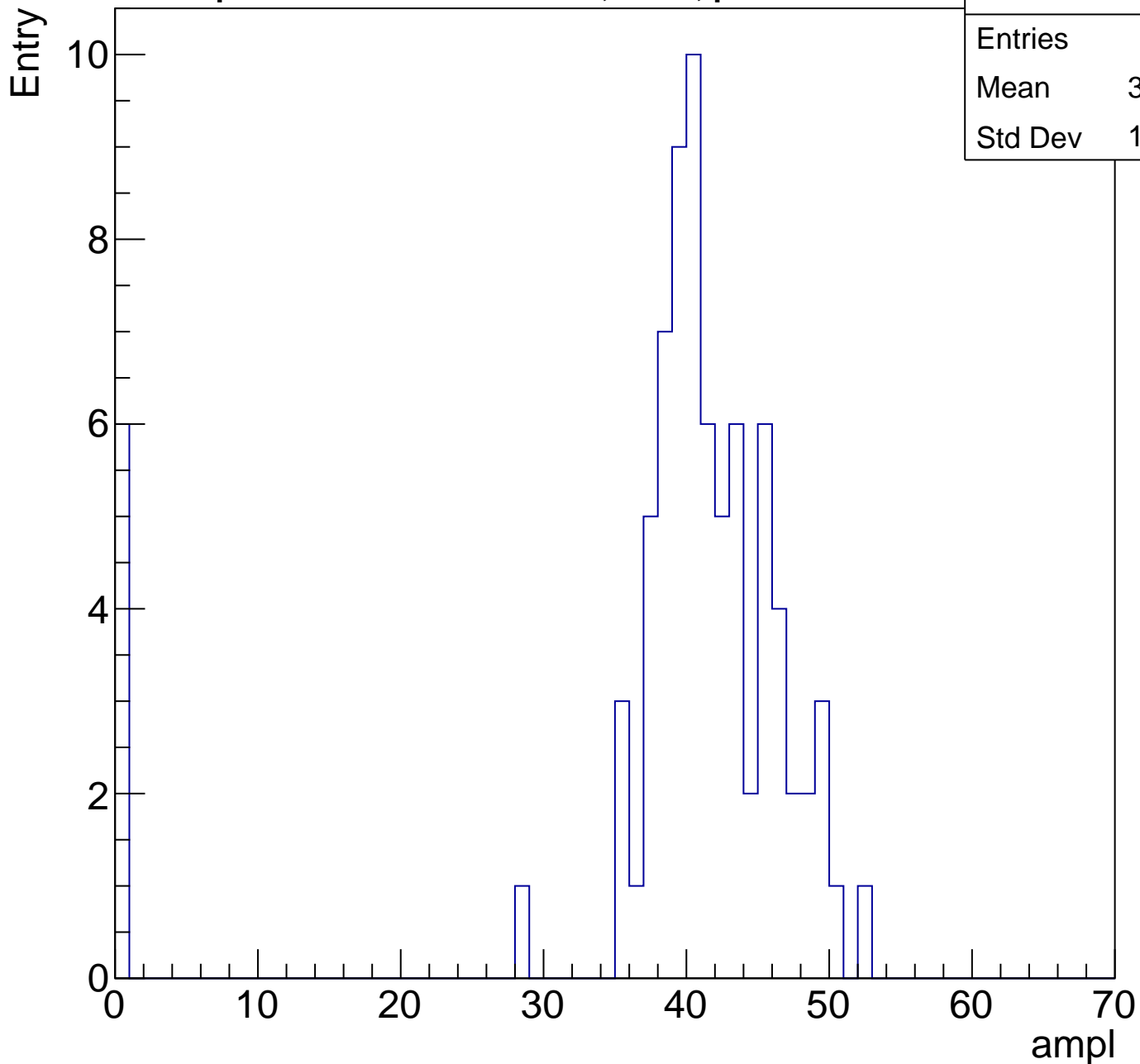
Entries	64
Mean	29.7
Std Dev	11.65



B1L103S, U11-ch124, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	38.33
Std Dev	11.63

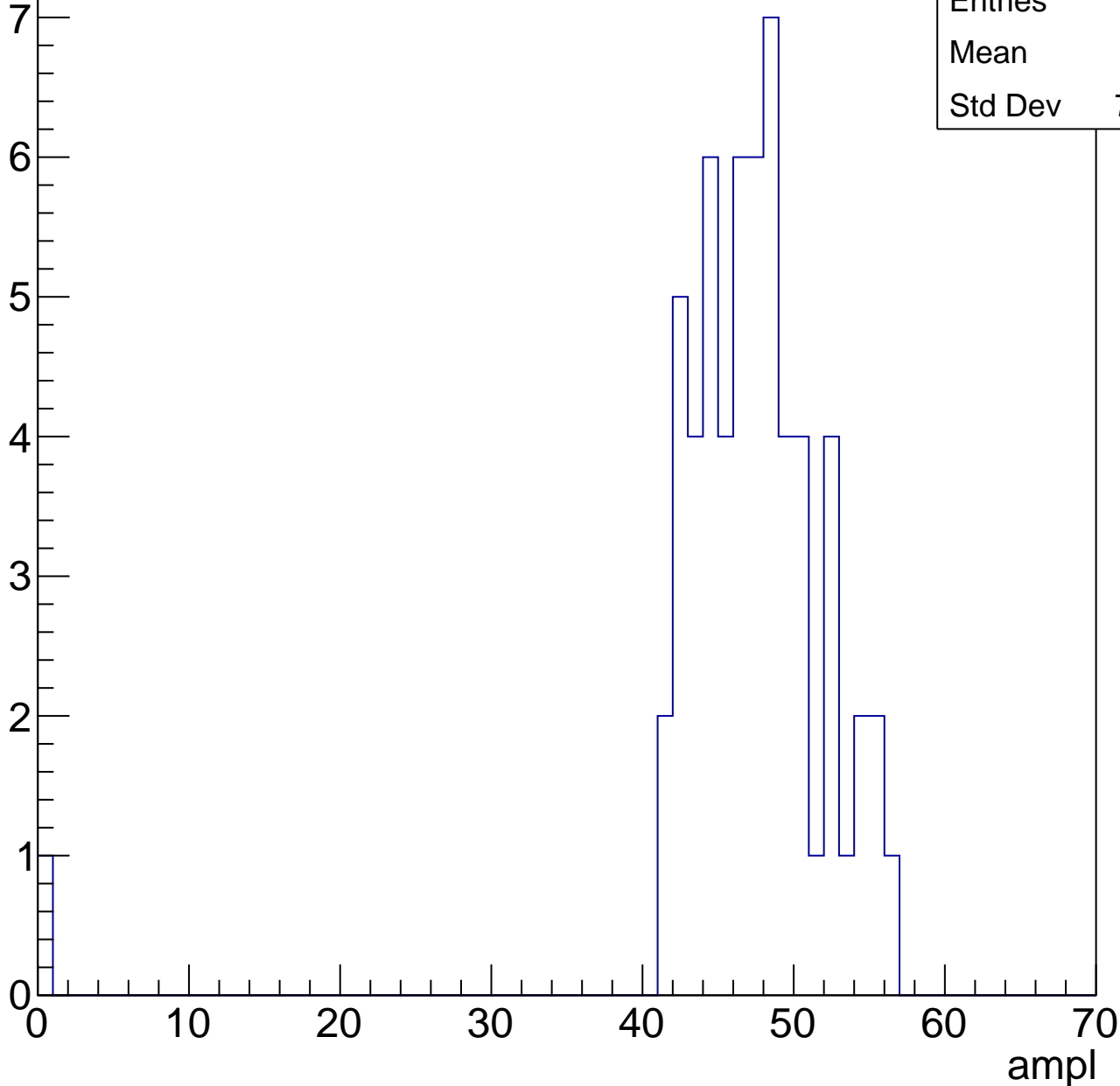


B1L103S, U11-ch124, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	46.4
Std Dev	7.121

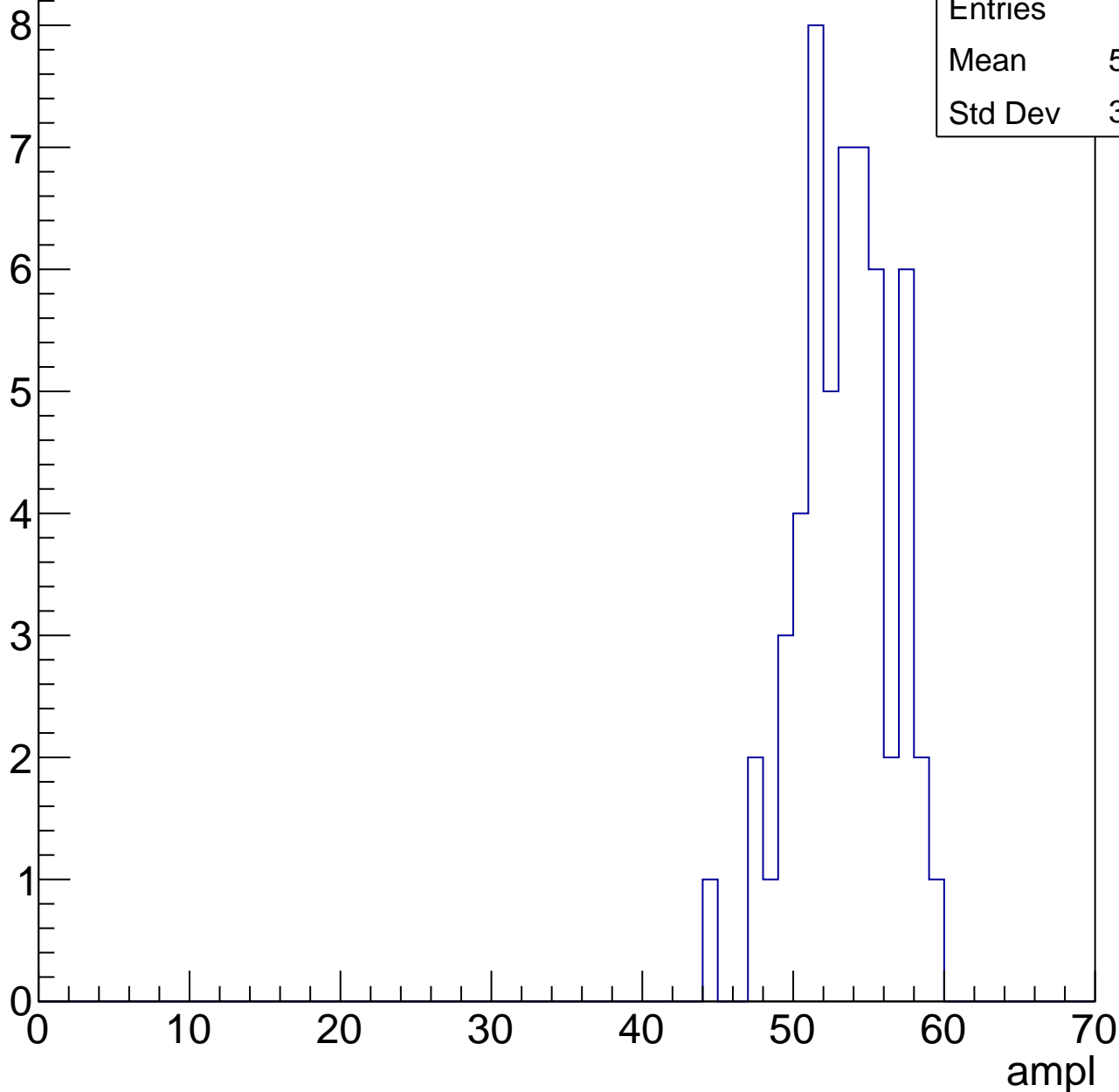


B1L103S, U11-ch124, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	52.89
Std Dev	3.102

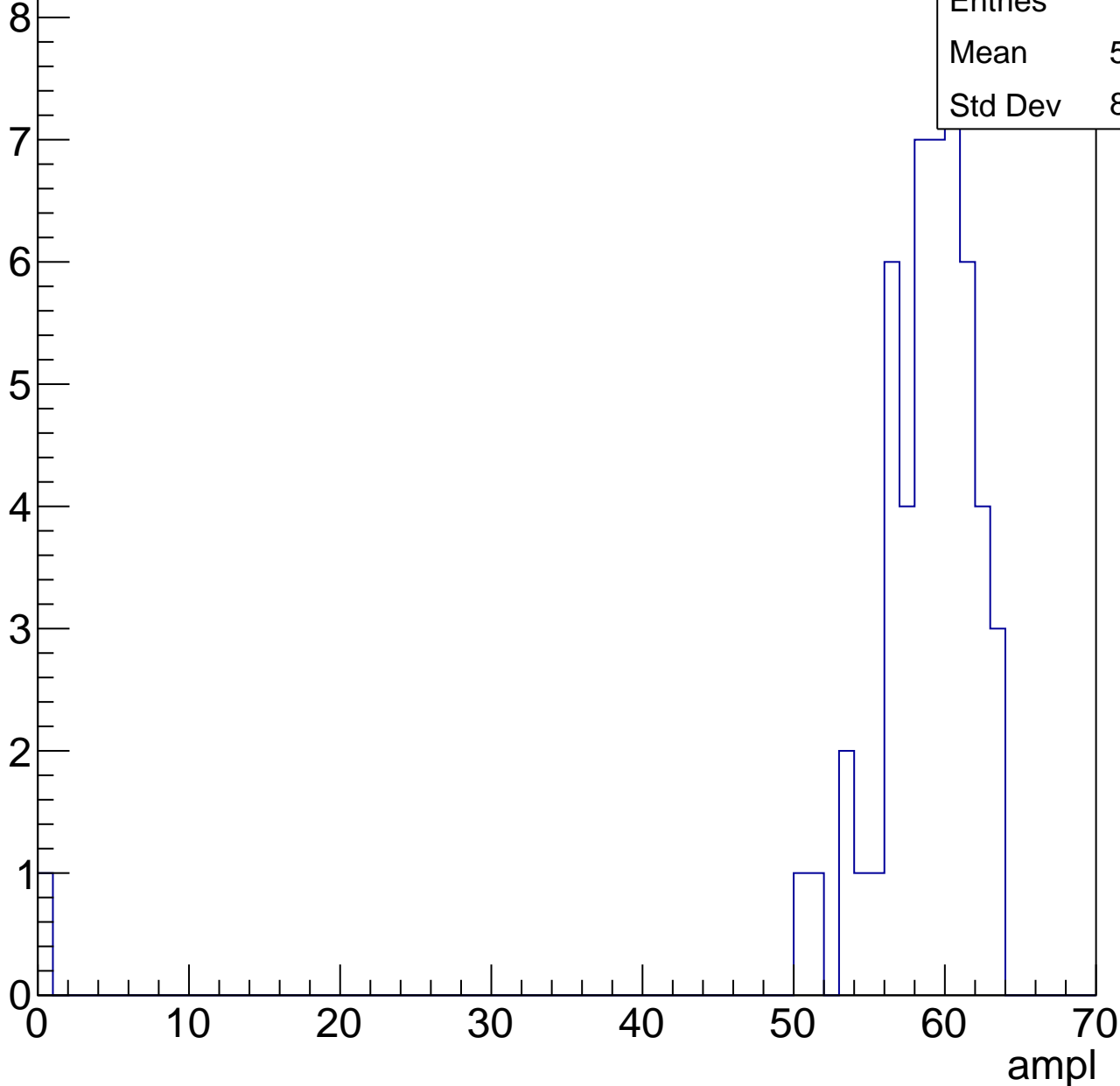


B1L103S, U11-ch124, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	57.35
Std Dev	8.537

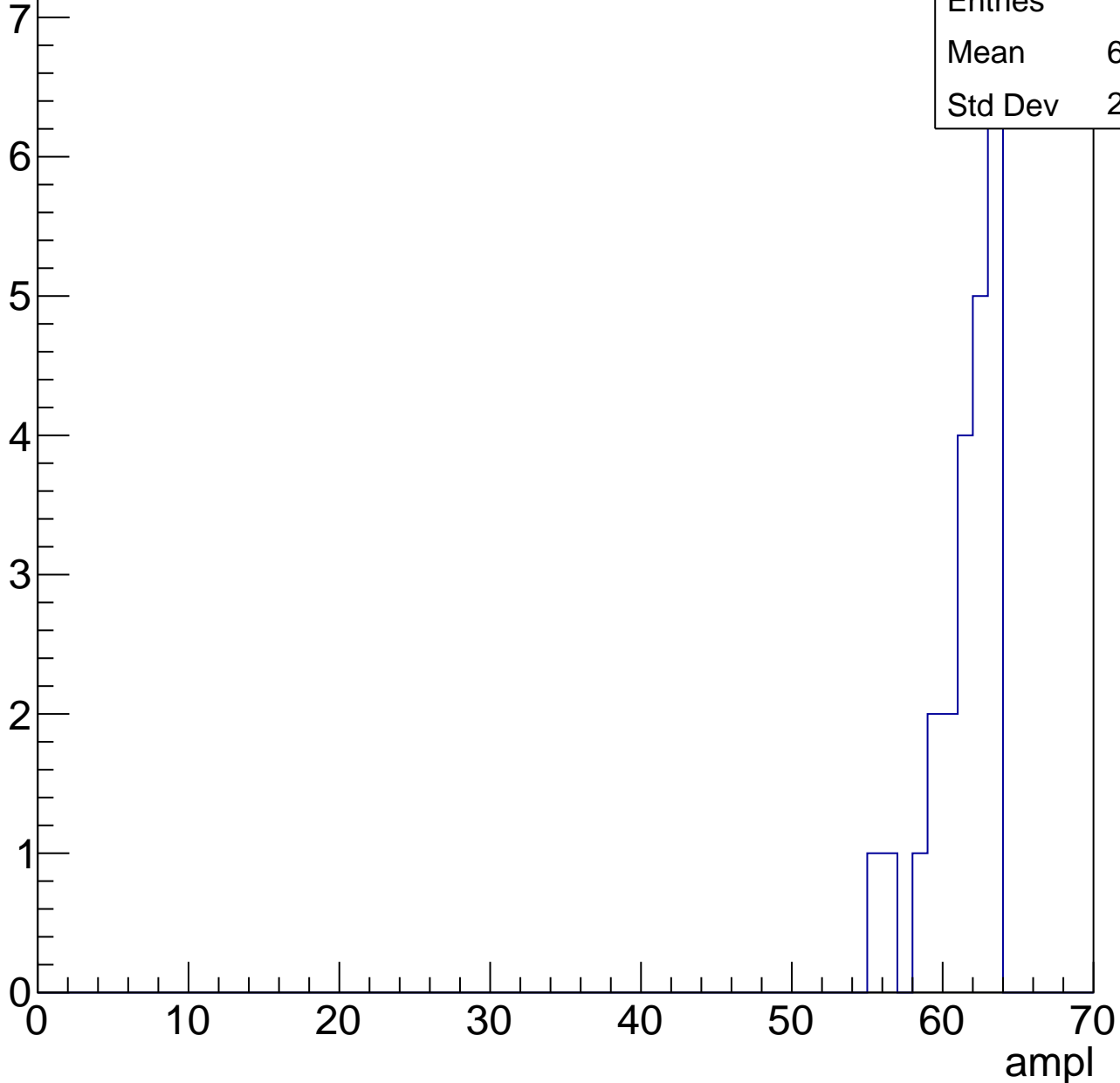


B1L103S, U11-ch124, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	23
Mean	60.96
Std Dev	2.216

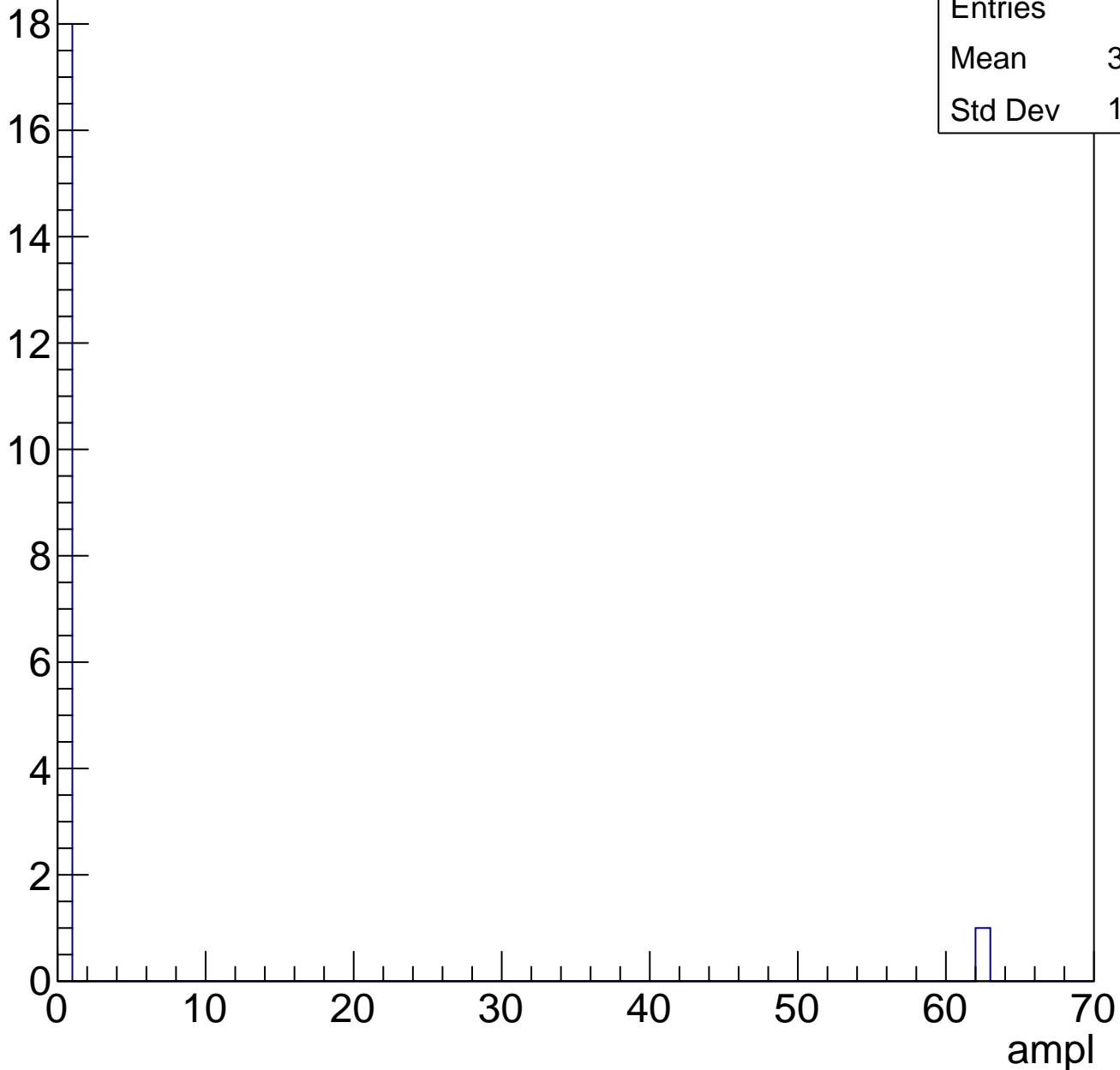


B1L103S, U11-ch124, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	3.263
Std Dev	13.84

Entry



B1L103S, U11-ch125, adc0

calib_packv5_041523_1651.root, FC#0, port C2

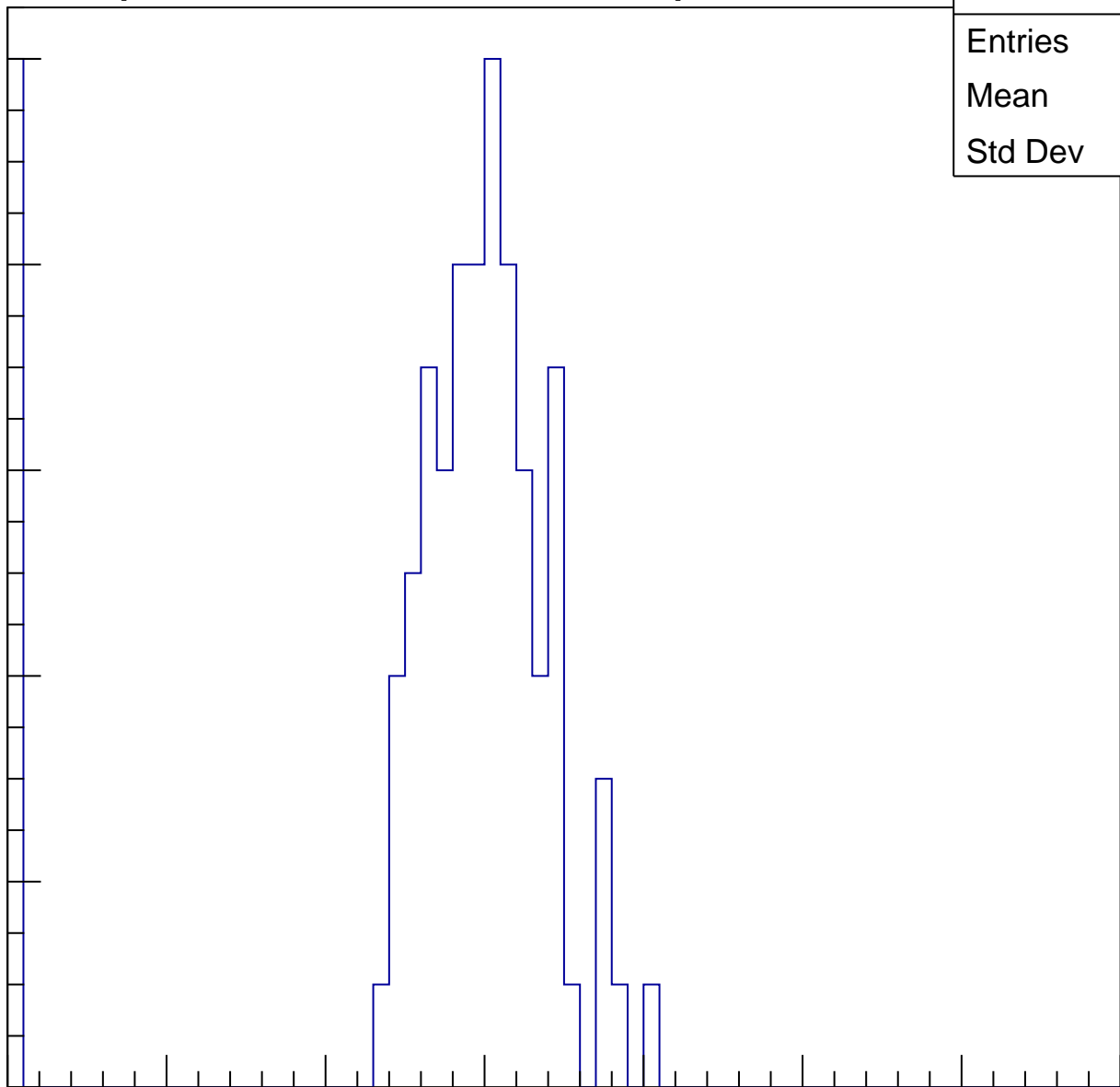
Entries	90
Mean	26.42
Std Dev	9.938

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

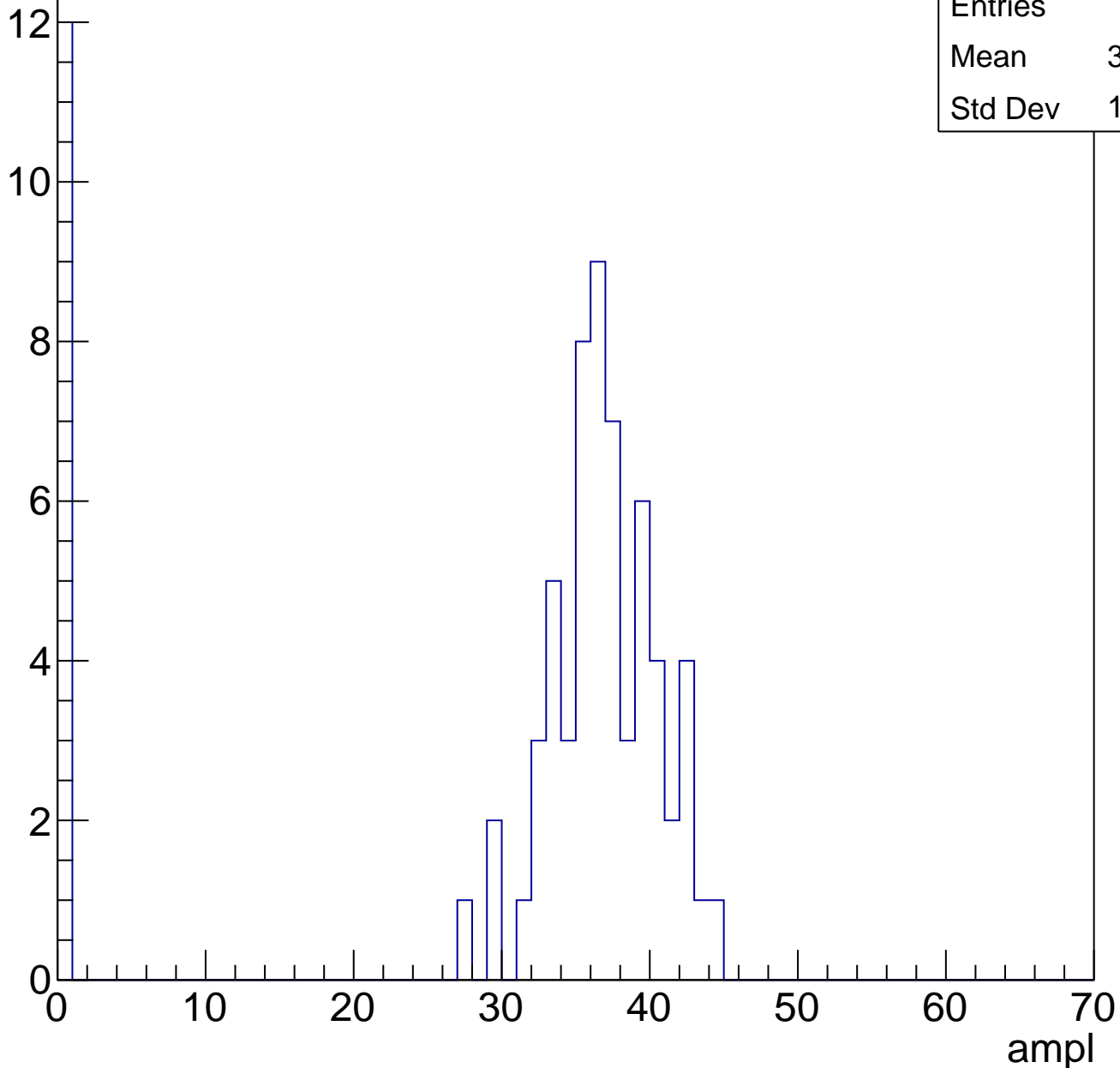


B1L103S, U11-ch125, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	72
Mean	30.38
Std Dev	13.96

Entry

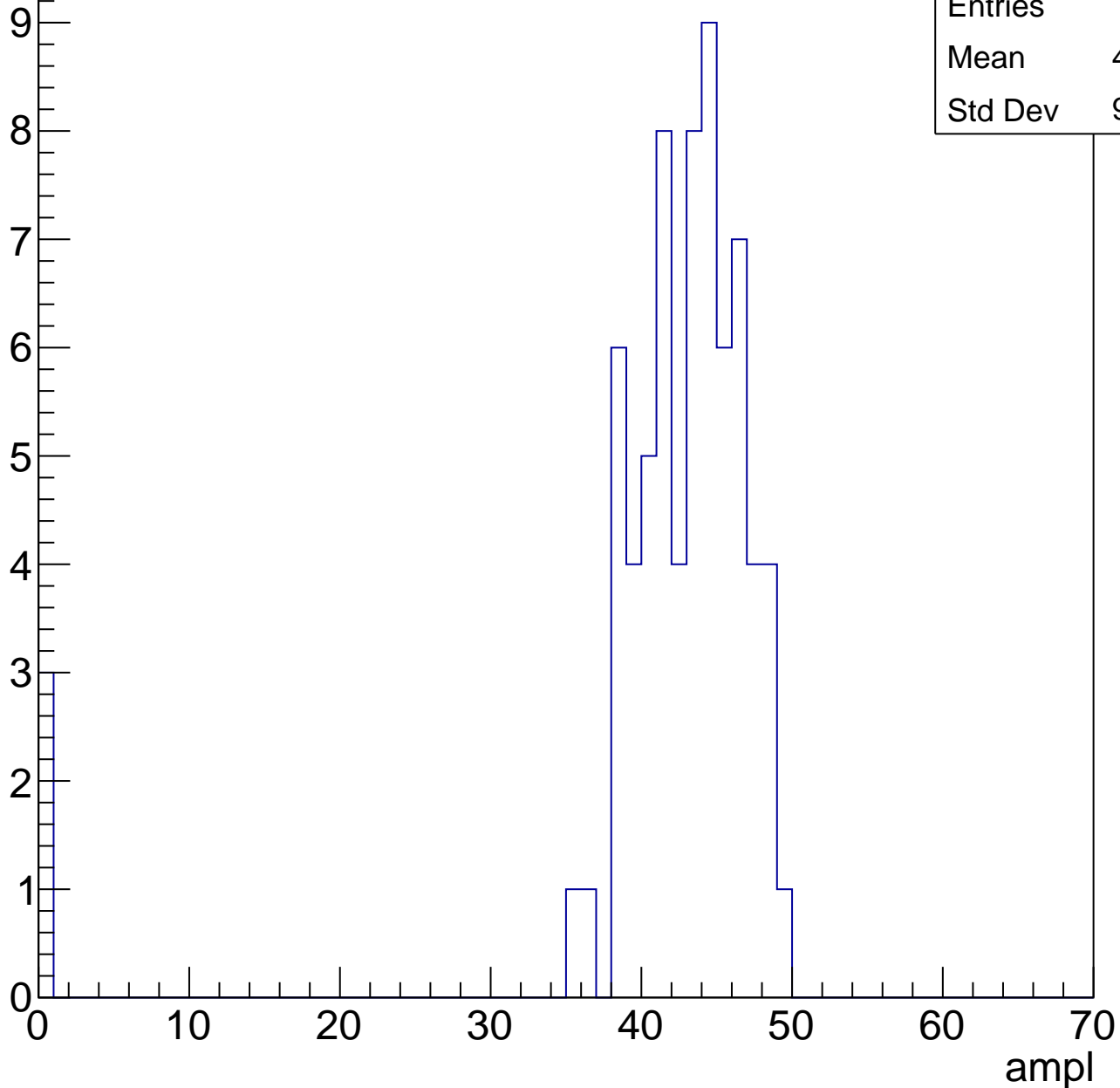


B1L103S, U11-ch125, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	41.01
Std Dev	9.171

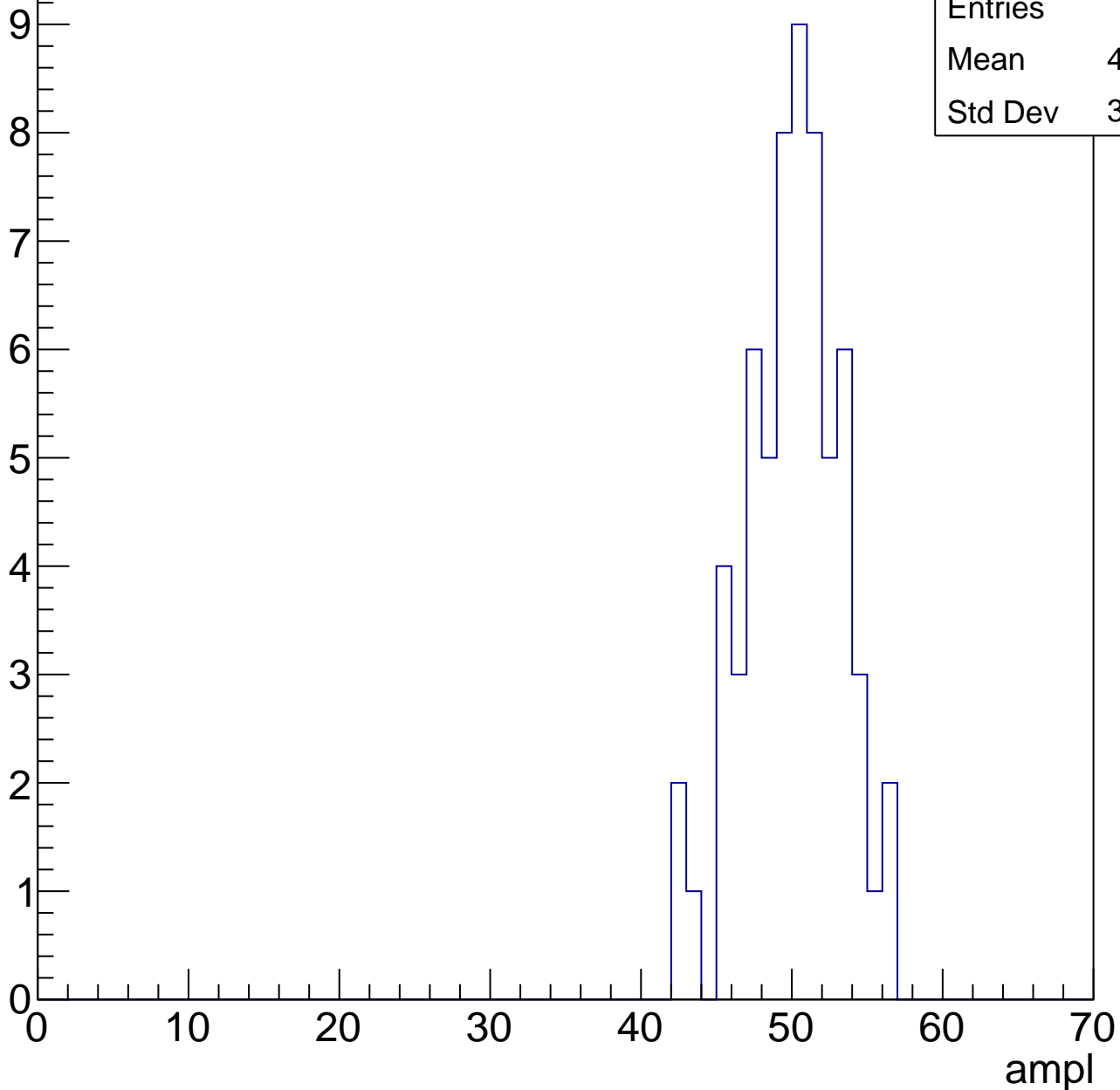


B1L103S, U11-ch125, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

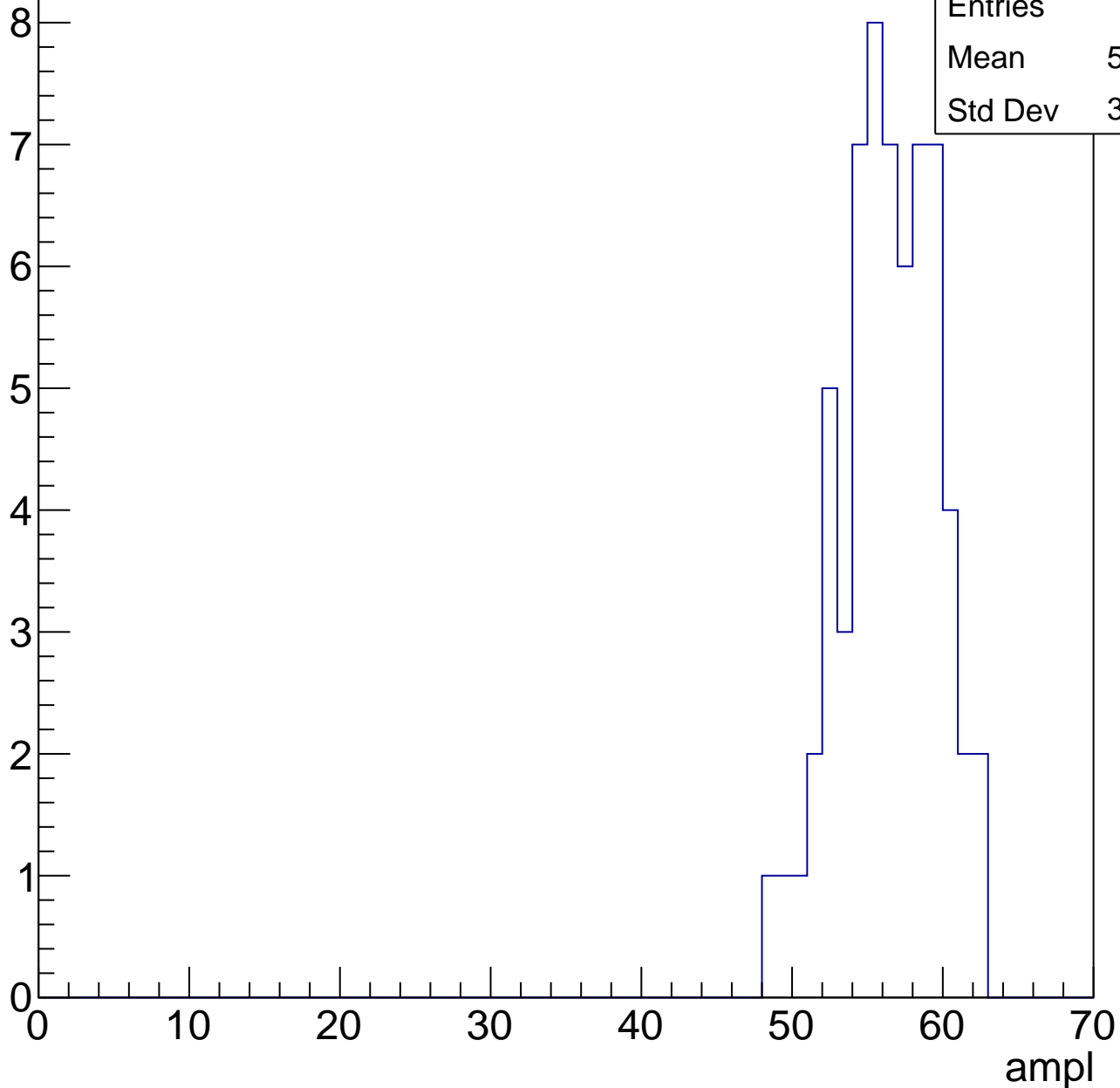
Entries	63
Mean	49.59
Std Dev	3.145



B1L103S, U11-ch125, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



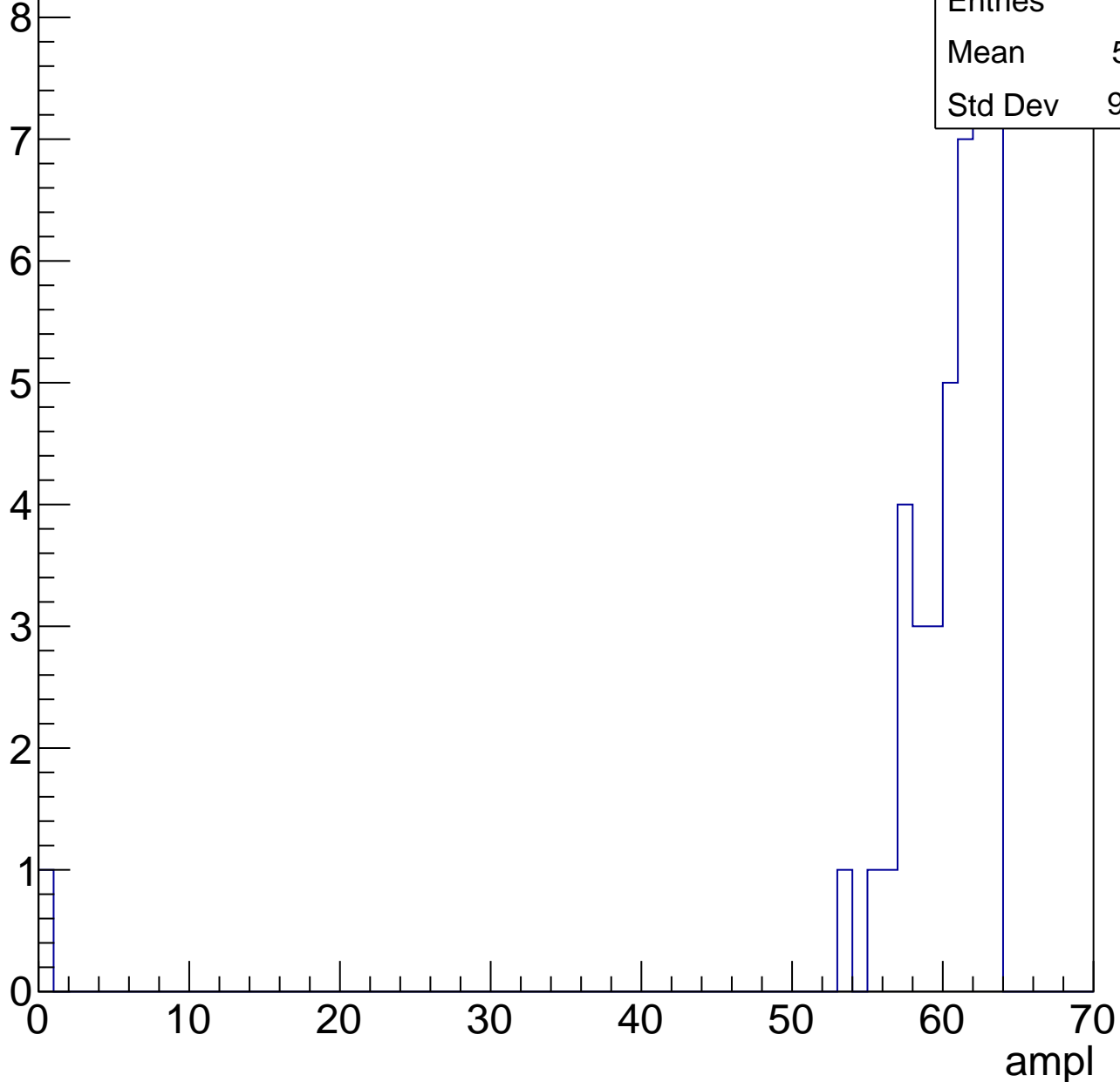
Entries	63
Mean	55.95
Std Dev	3.149

B1L103S, U11-ch125, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	42
Mean	58.81
Std Dev	9.502



B1L103S, U11-ch125, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	4
Mean	61.75
Std Dev	1.299

0 10 20 30 40 50 60 70

ampl

1

B1L103S, U11-ch125, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.211
Std Dev	5.136

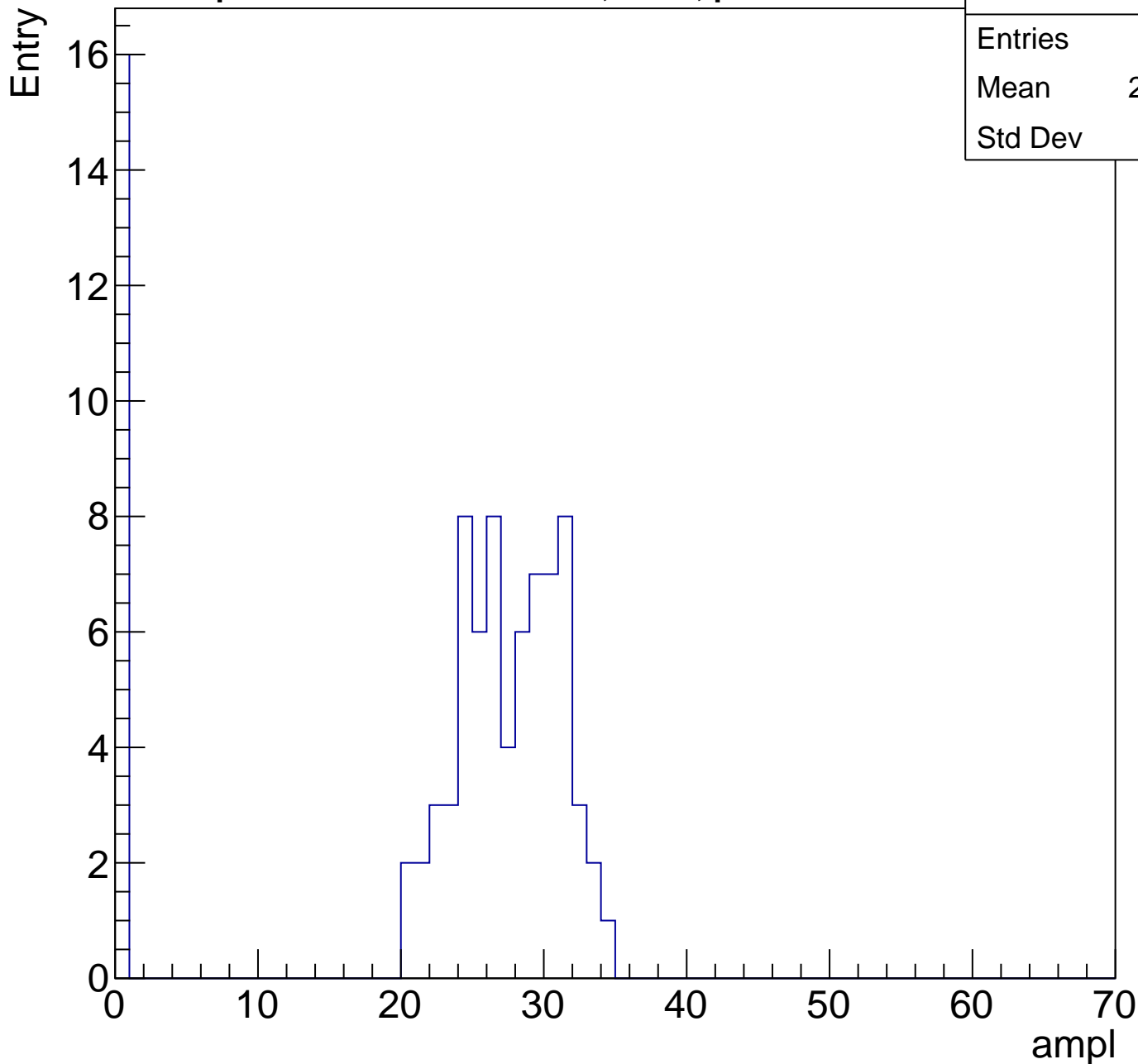
Entry



B1L103S, U11-ch126, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	86
Mean	22.09
Std Dev	11



B1L103S, U11-ch126, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	95
Mean	30.86
Std Dev	11.77

Entry

10

8

6

4

2

0

0

10

20

30

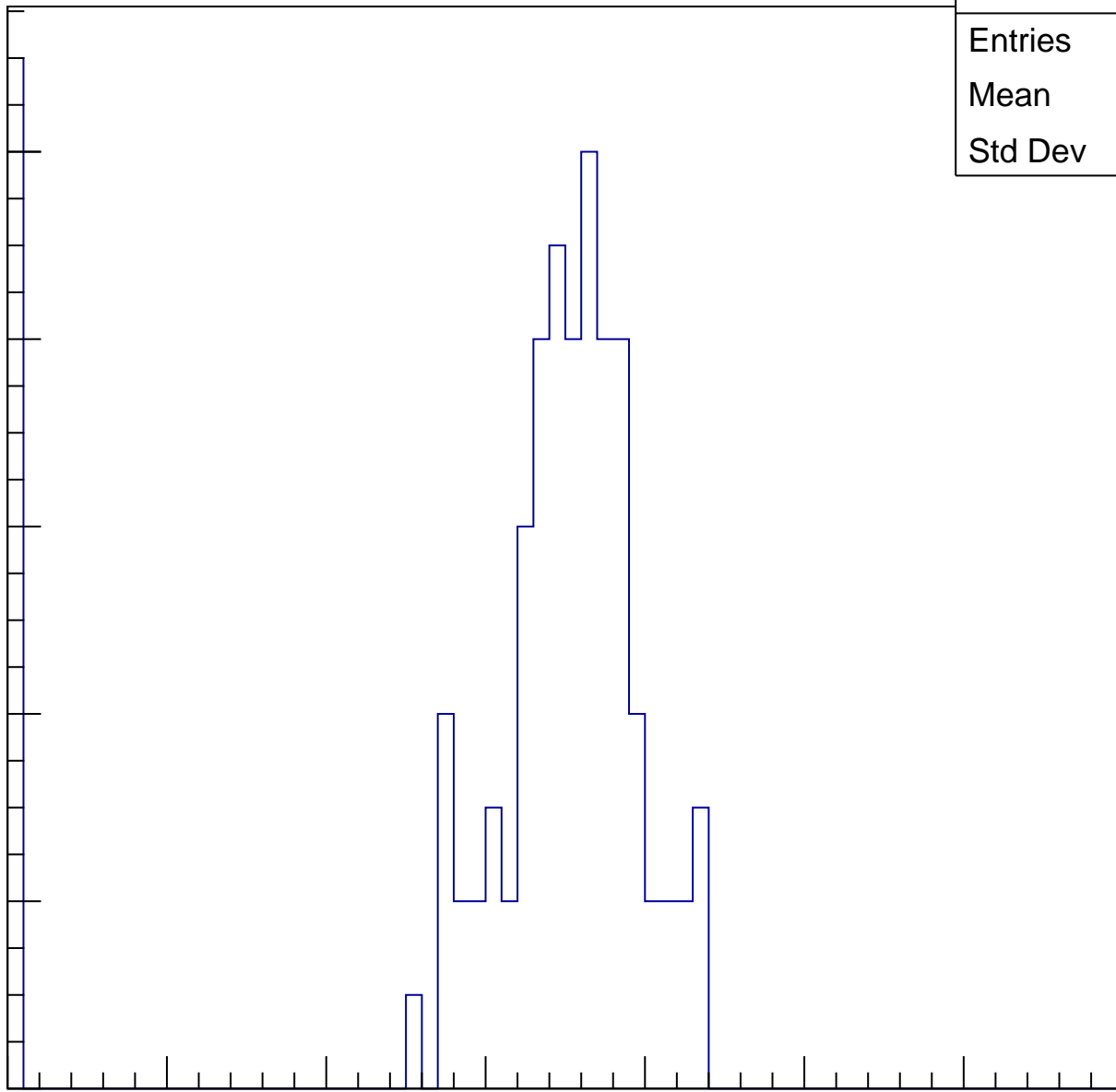
40

50

60

70

ampl

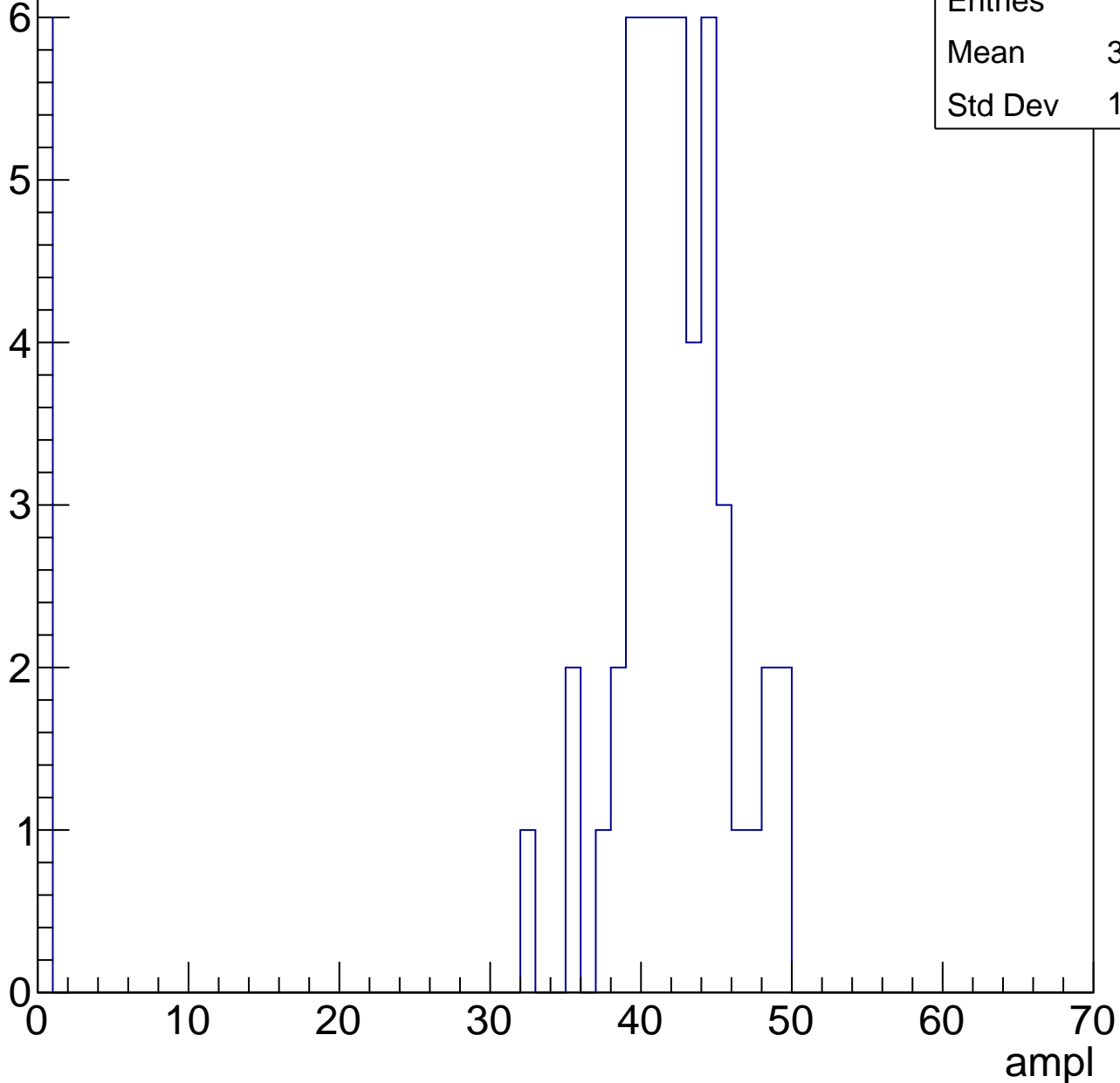


B1L103S, U11-ch126, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	37.18
Std Dev	13.42

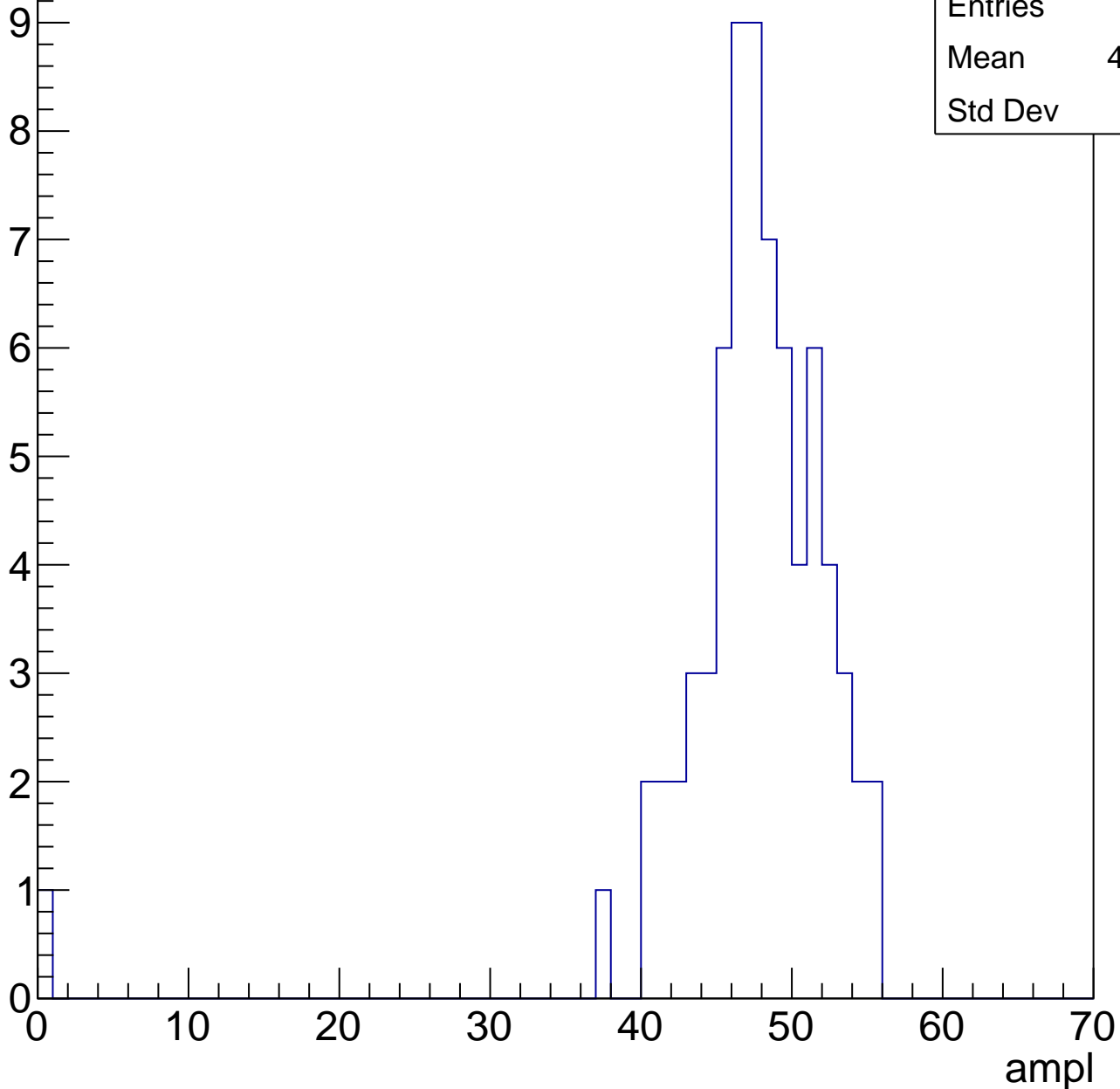


B1L103S, U11-ch126, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	46.83
Std Dev	6.7

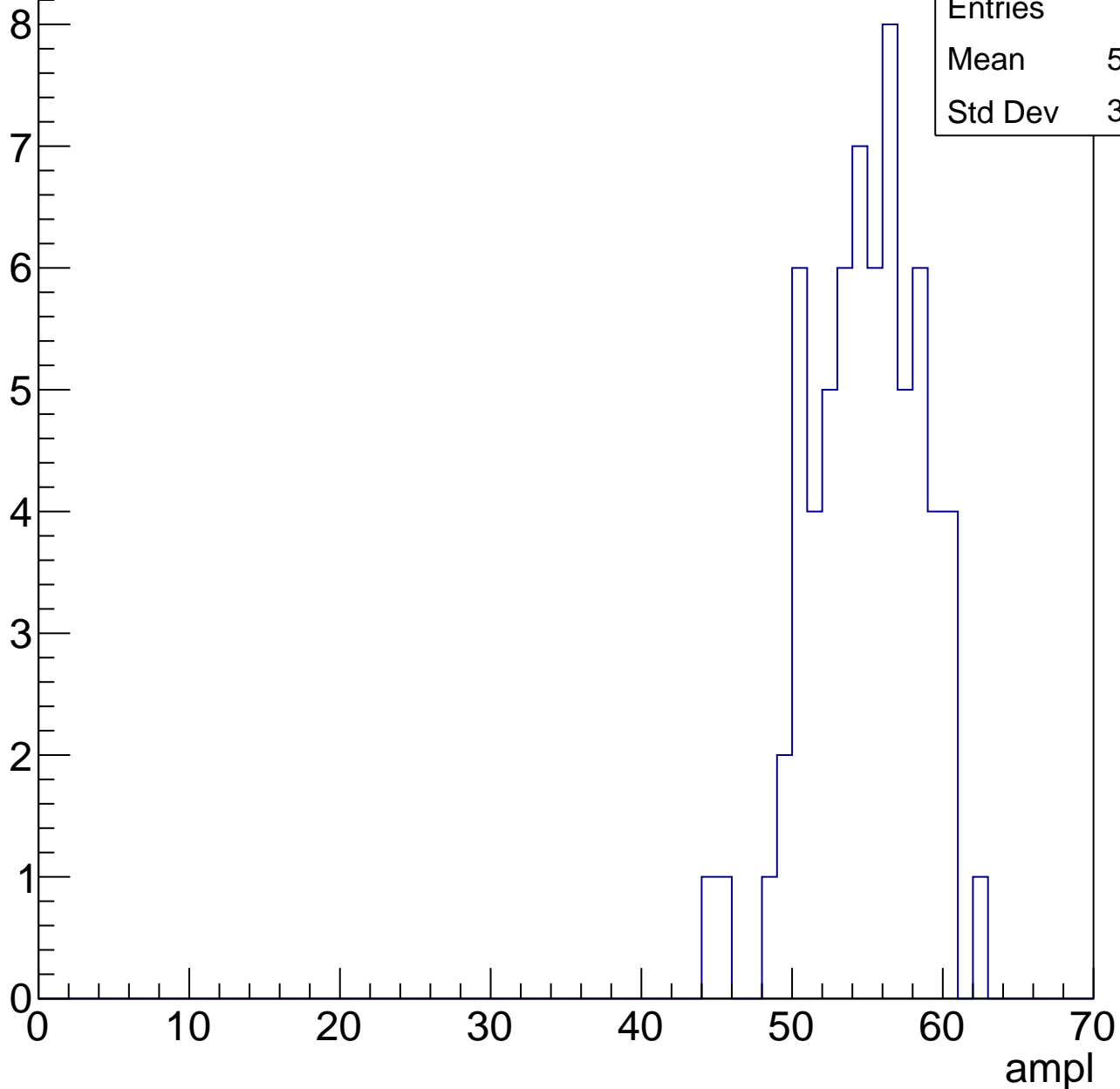


B1L103S, U11-ch126, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	54.39
Std Dev	3.669

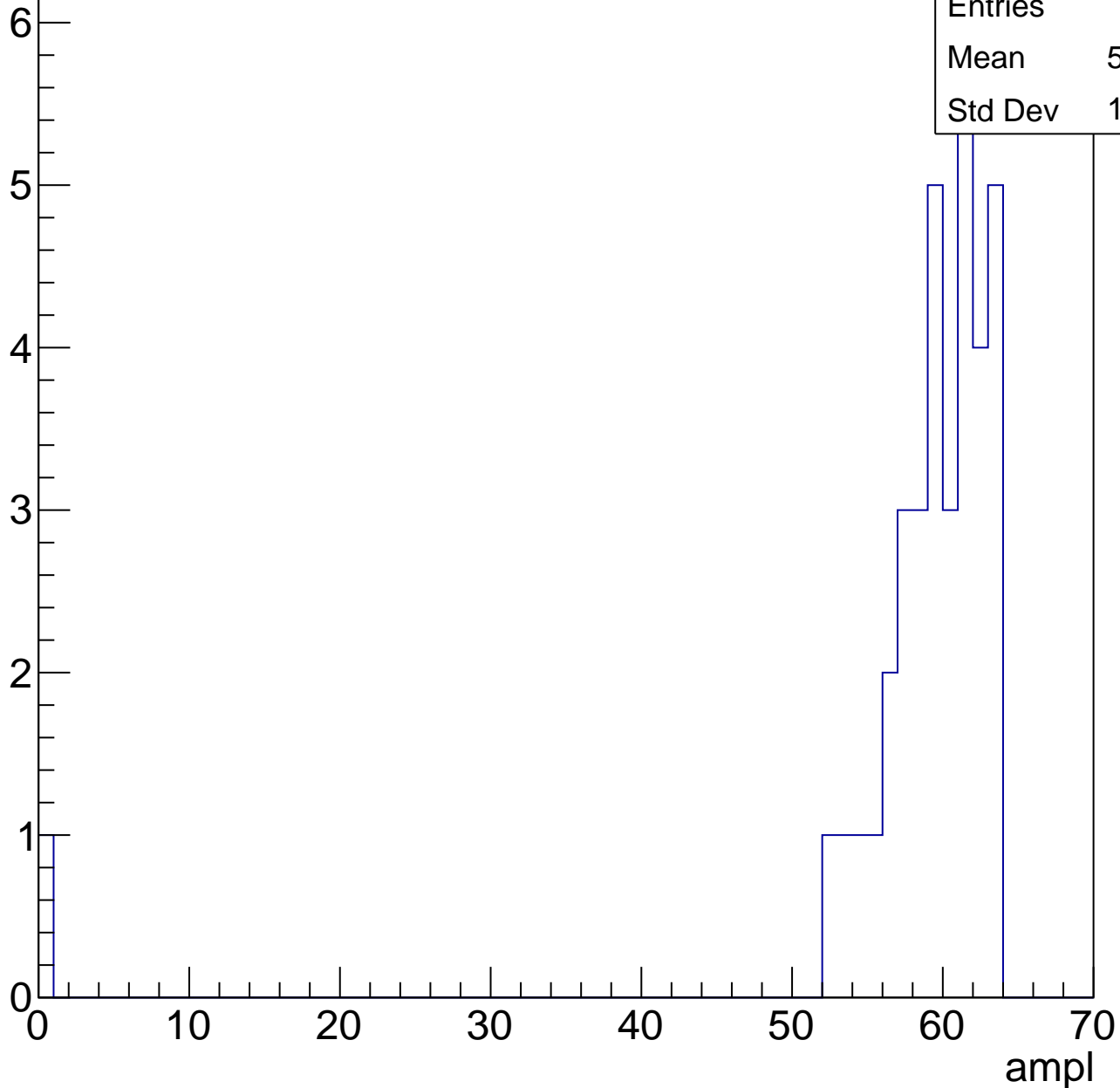


B1L103S, U11-ch126, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	36
Mean	57.64
Std Dev	10.16

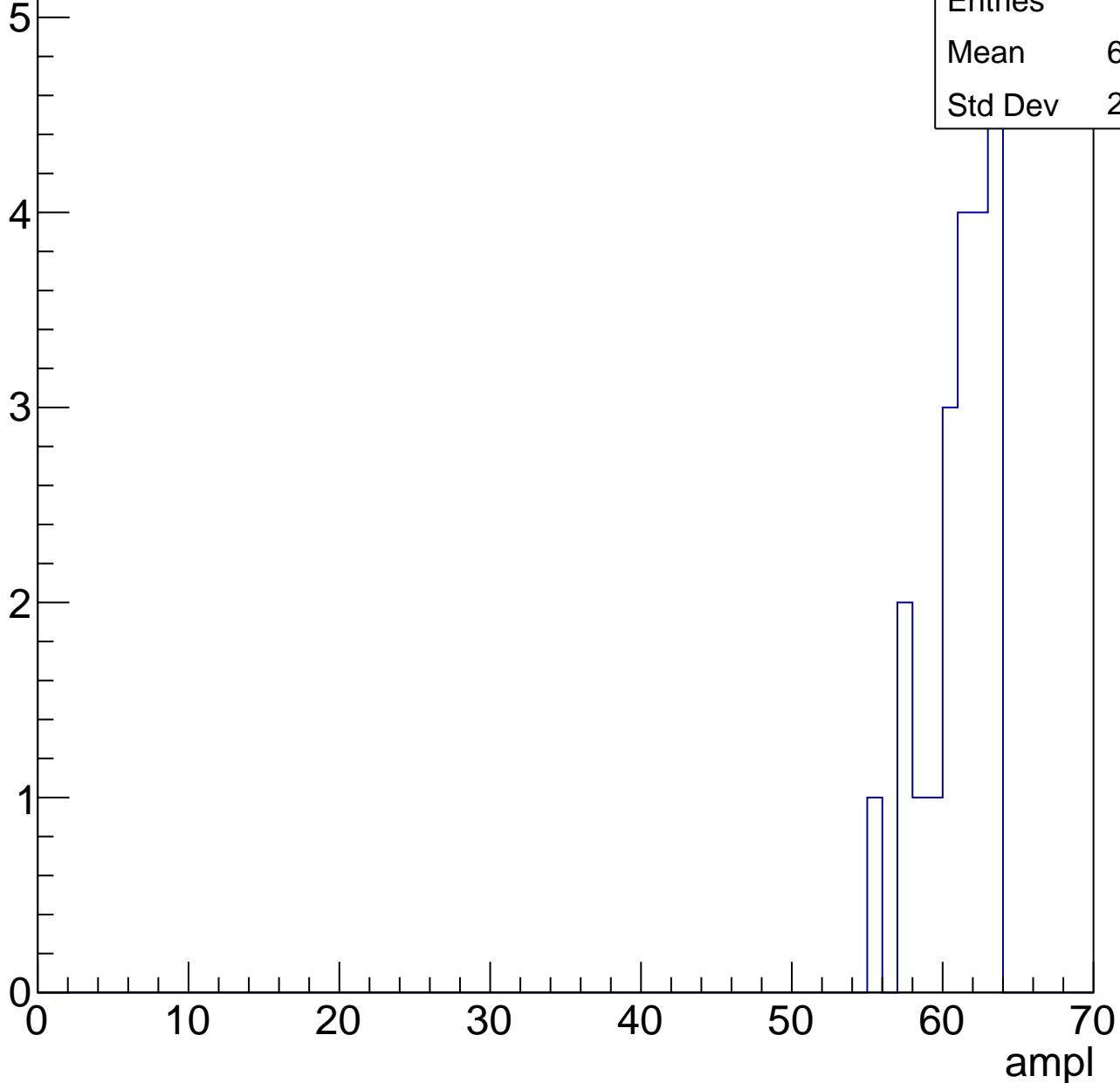


B1L103S, U11-ch126, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	21
Mean	60.62
Std Dev	2.236



B1L103S, U11-ch126, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51

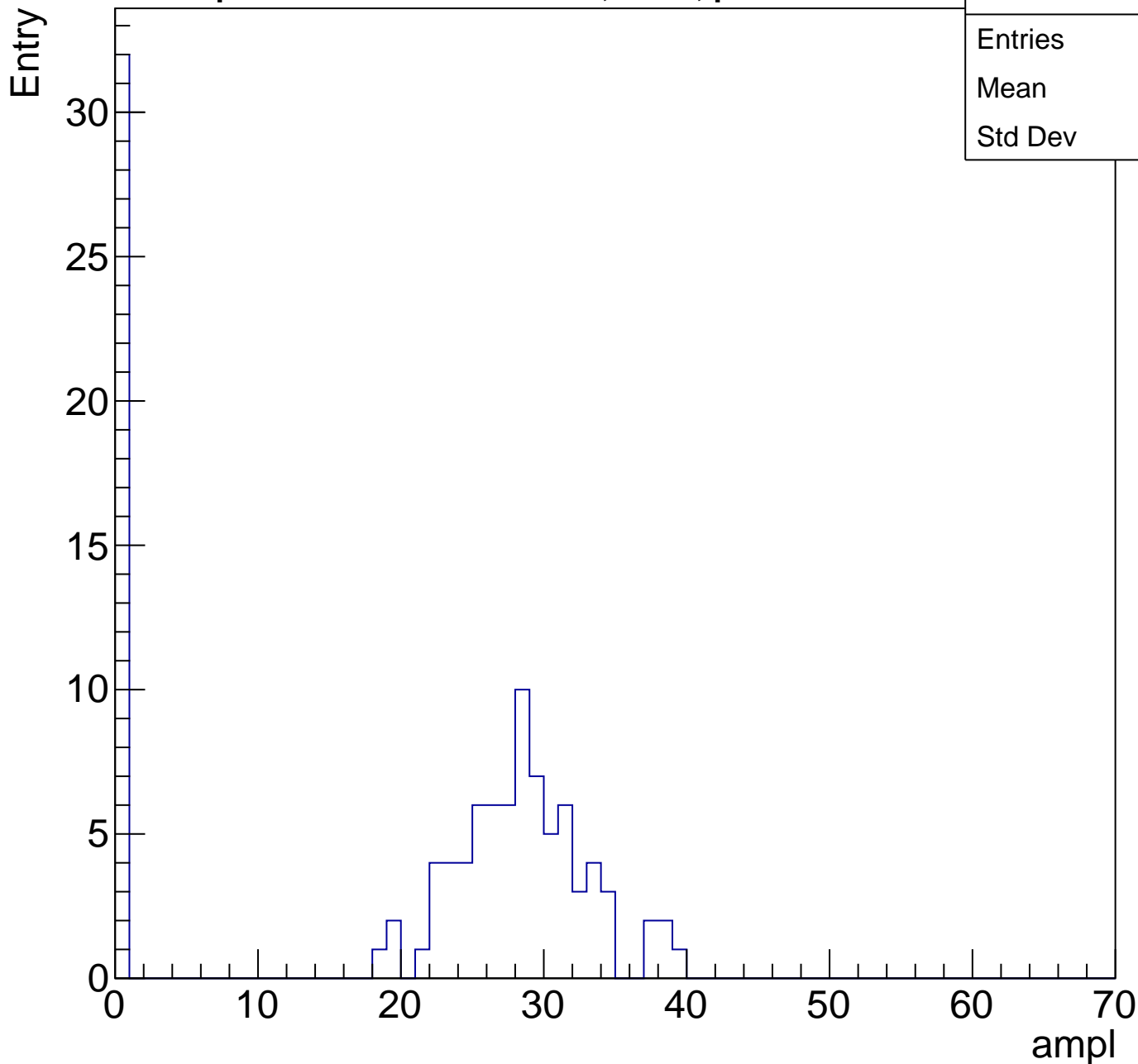
Entry



B1L103S, U11-ch127, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	109
Mean	19.81
Std Dev	13.3

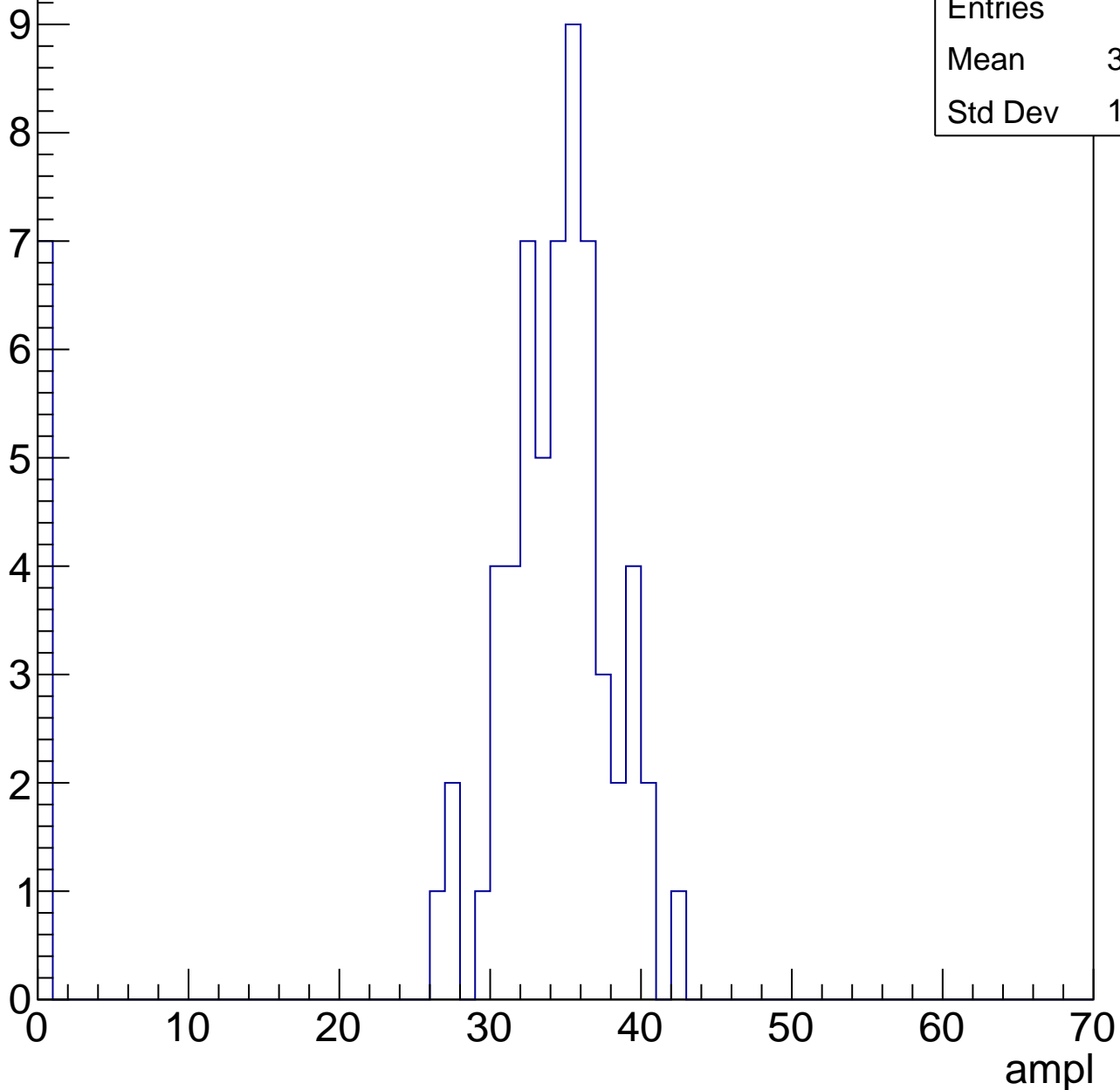


B1L103S, U11-ch127, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	30.48
Std Dev	10.96

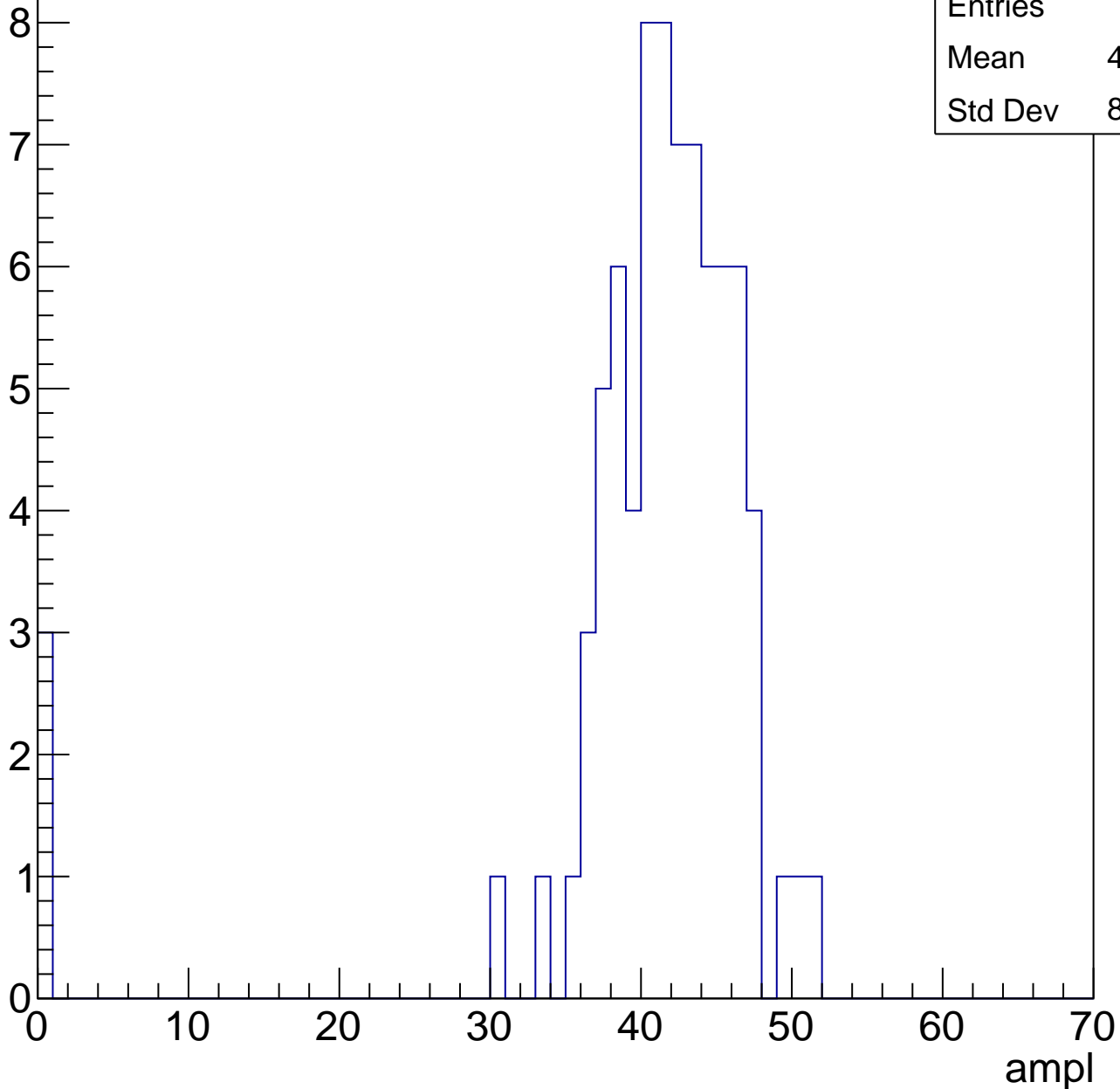


B1L103S, U11-ch127, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	79
Mean	40.08
Std Dev	8.826

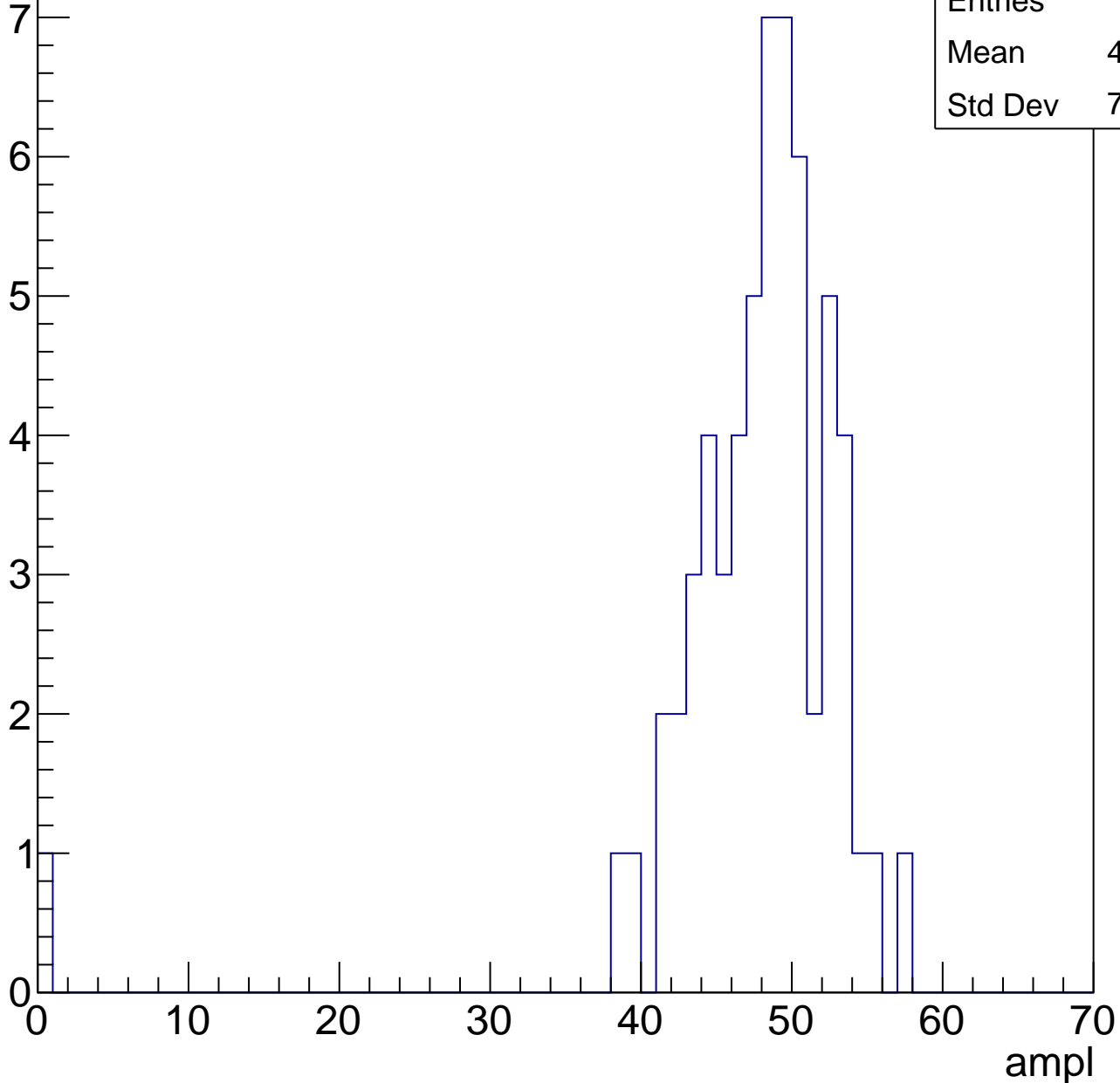


B1L103S, U11-ch127, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	47.02
Std Dev	7.279

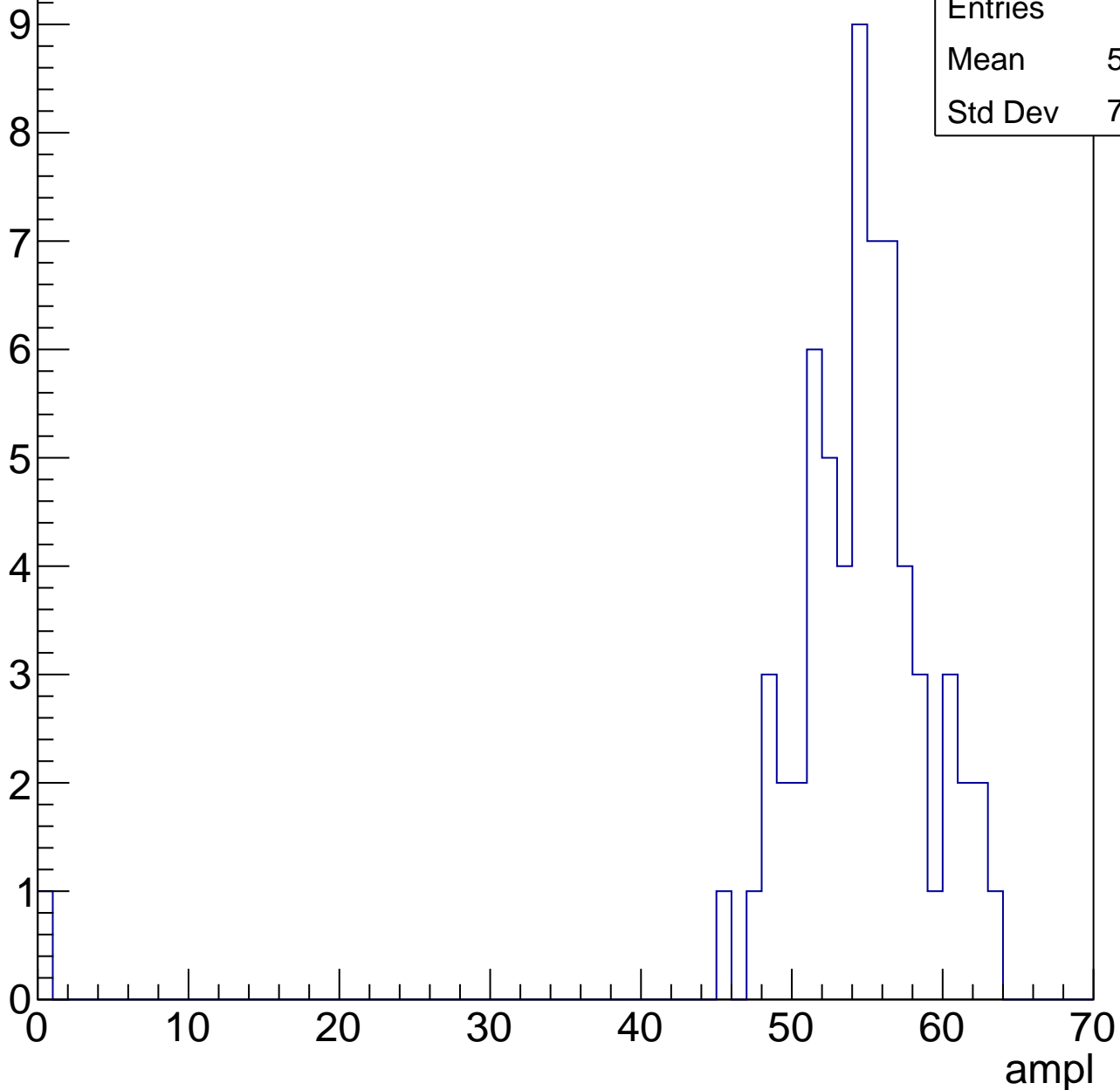


B1L103S, U11-ch127, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	53.52
Std Dev	7.764

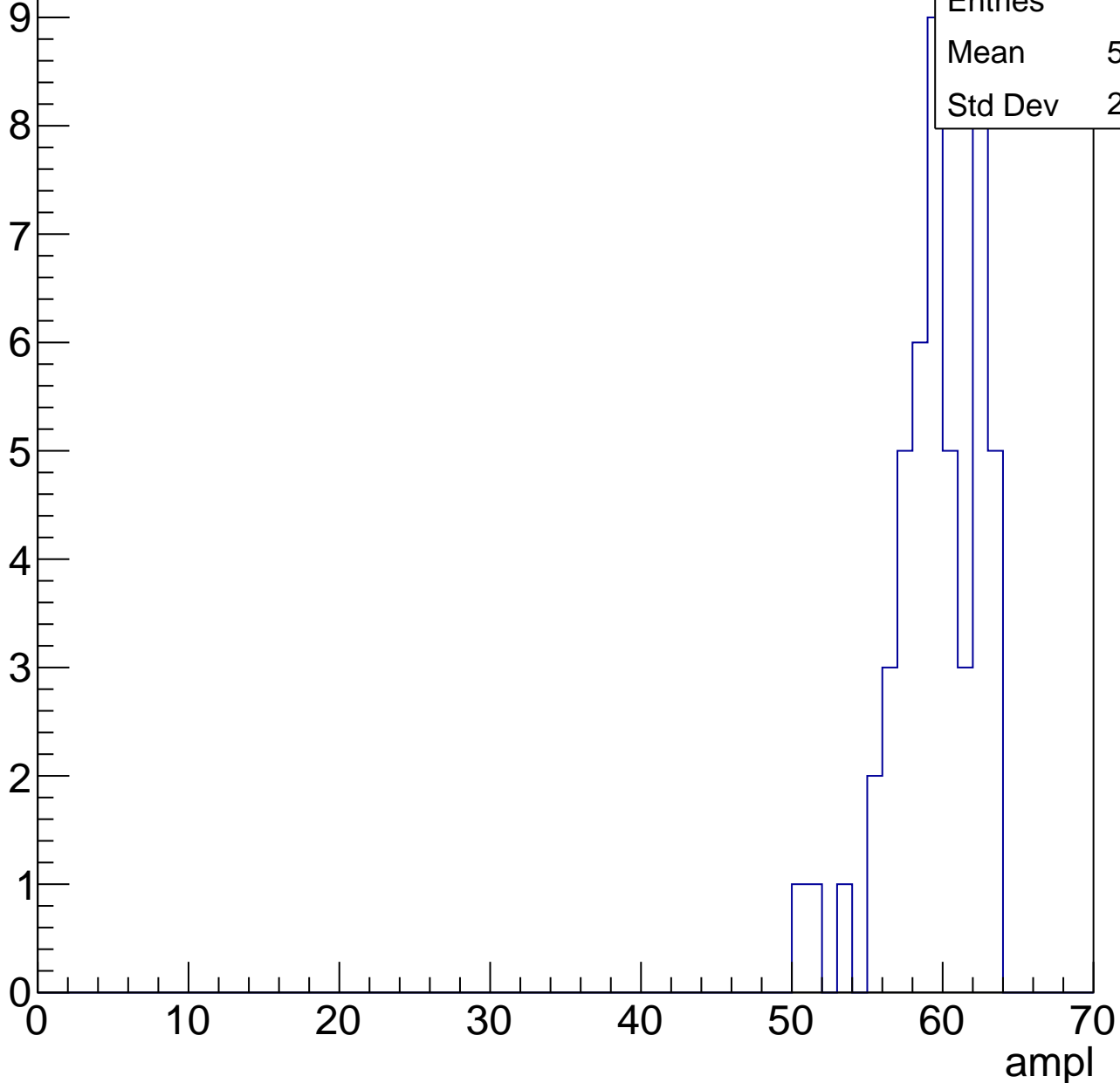


B1L103S, U11-ch127, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	58.98
Std Dev	2.979

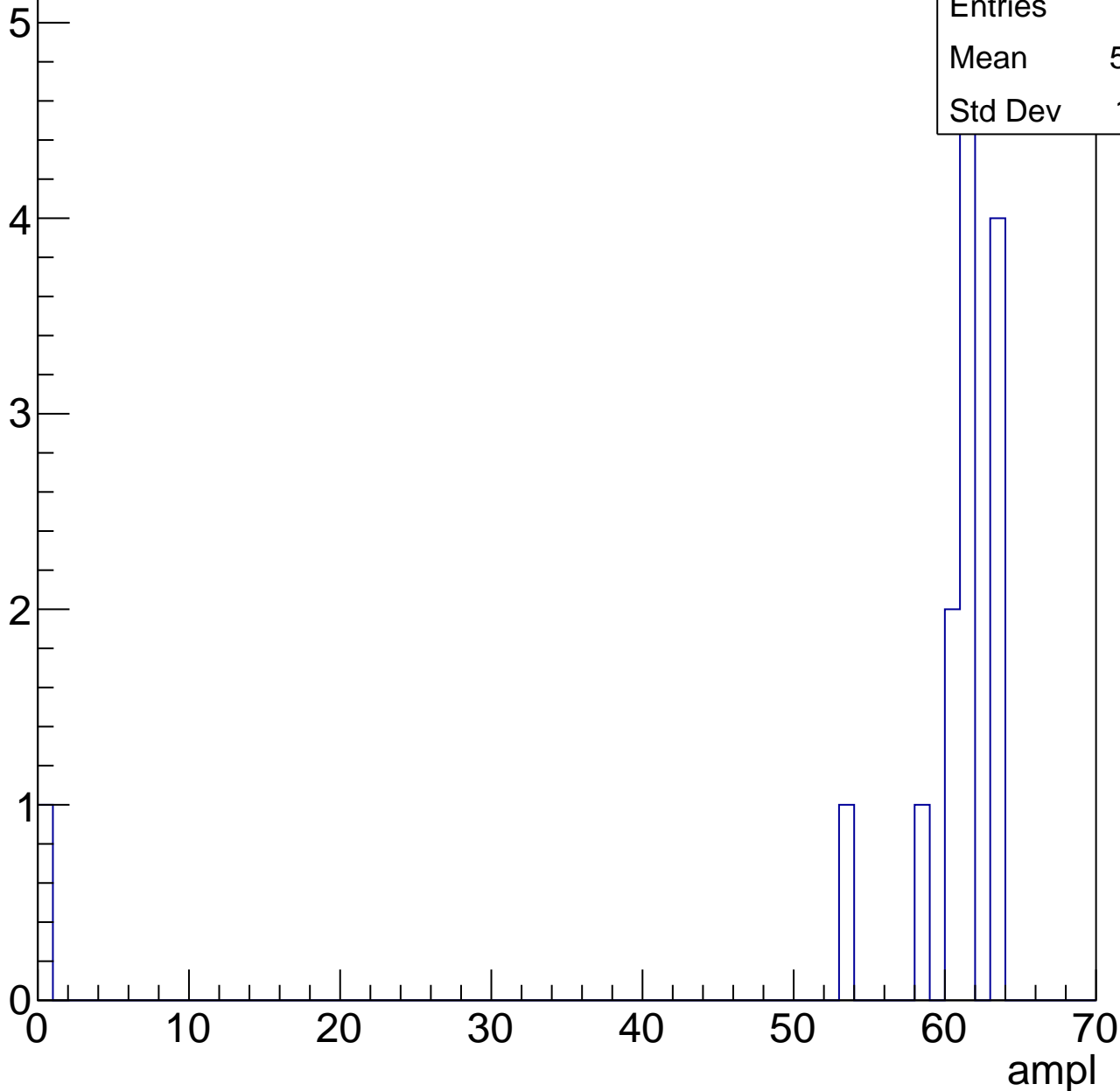


B1L103S, U11-ch127, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	14
Mean	56.29
Std Dev	15.81

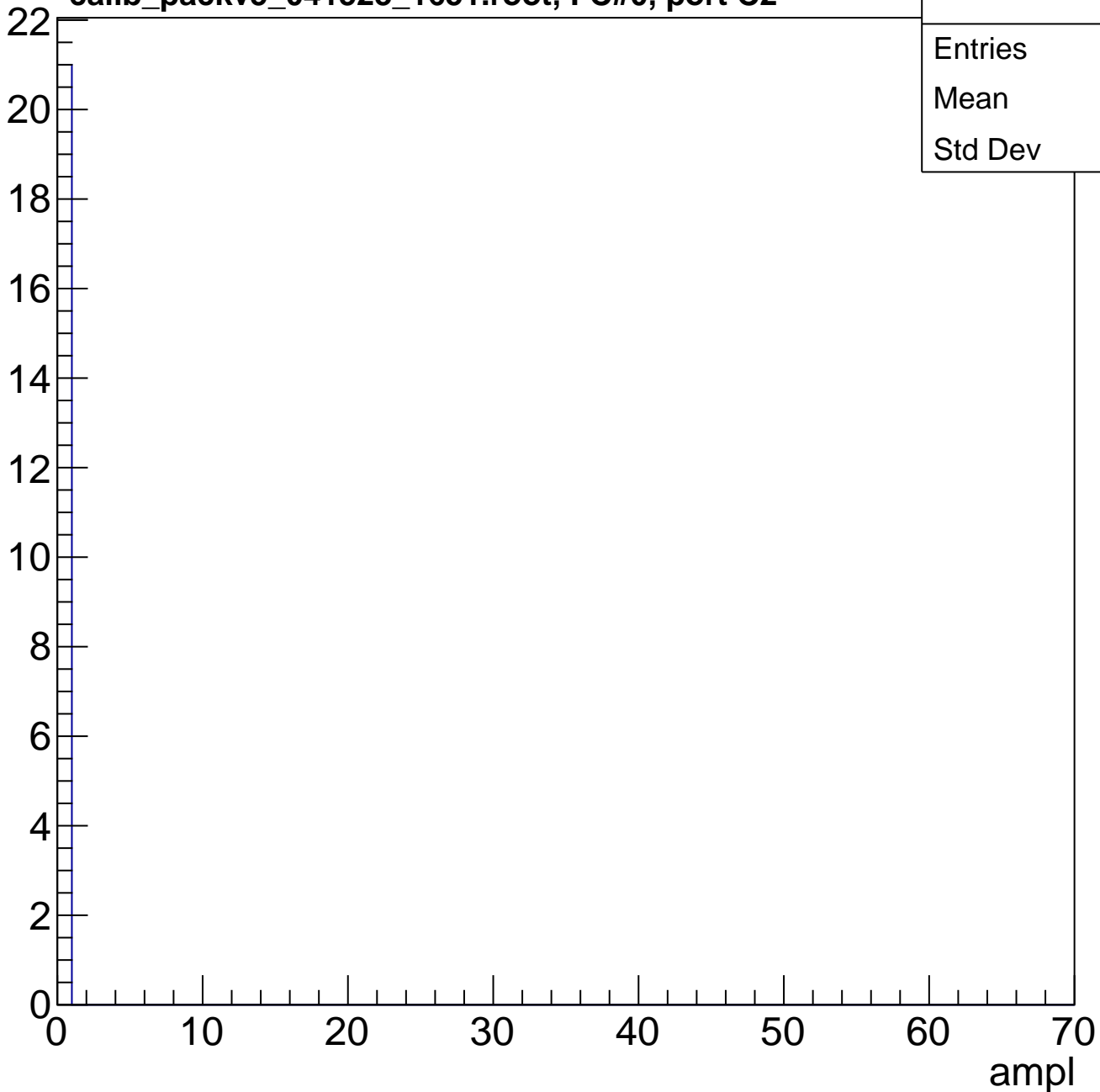


B1L103S, U11-ch127, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	0
Std Dev	0

Entry



B1L103S, U11-ch127, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	0
Std Dev	0

