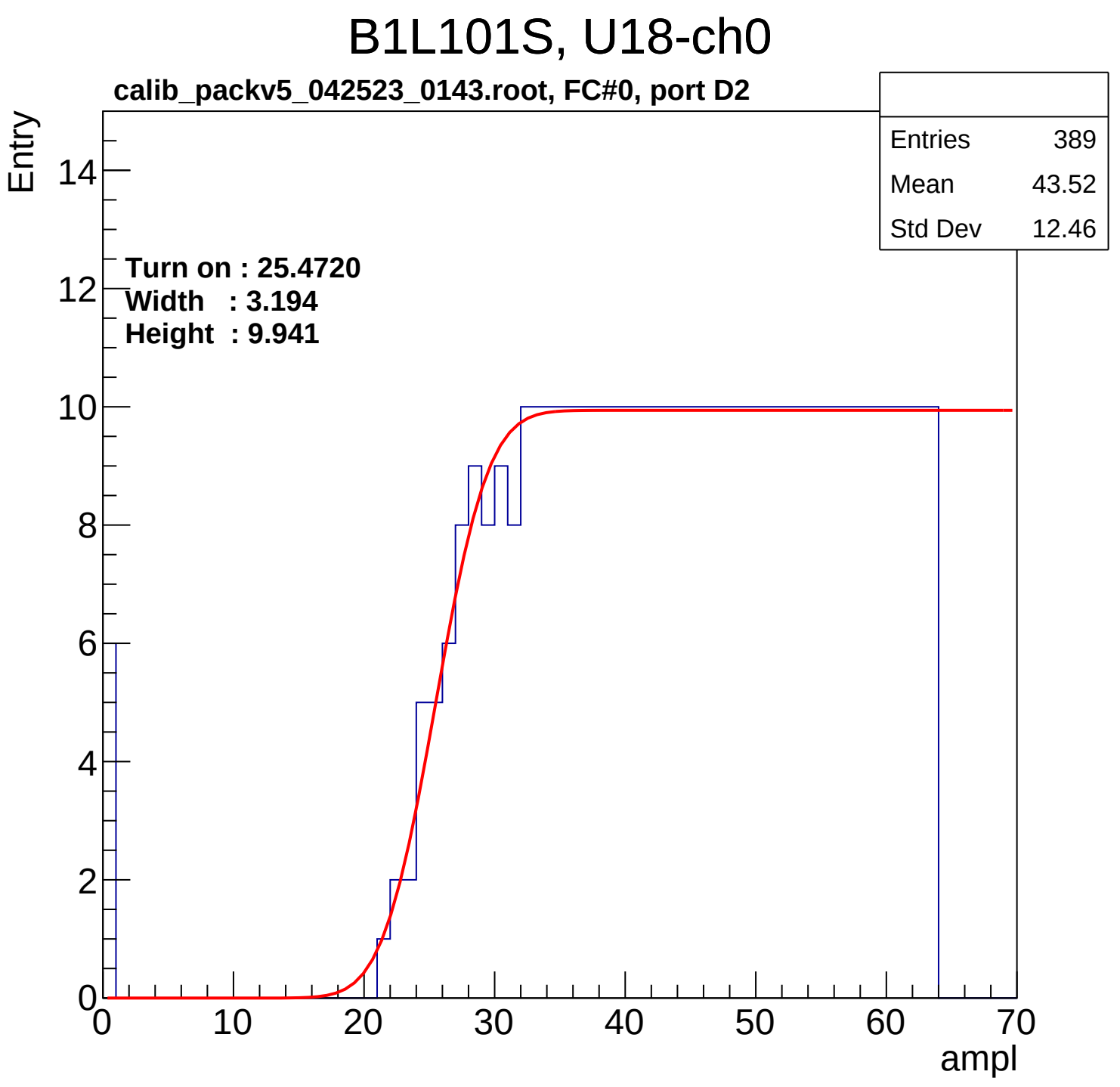
B1L101S, U18-ch0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 389
Mean 43.52
Std Dev 12.46
Turn on : 25.4720
Width : 3.194
Height : 9.941
Entry
ampl
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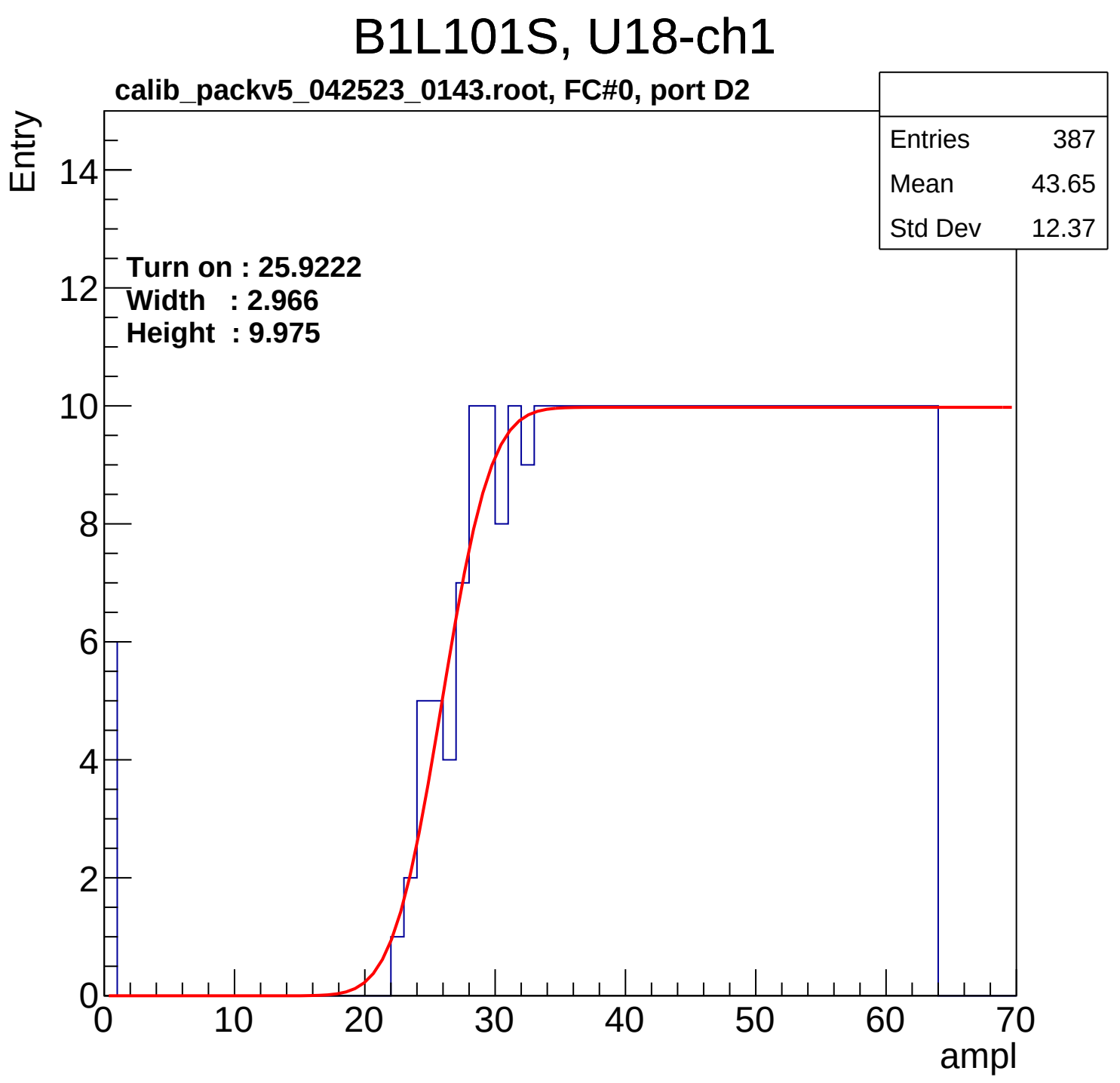
B1L101S, U18-ch1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.65
Std Dev 12.37
Turn on : 25.9222
Width : 2.966
Height : 9.975
Entry
ampl
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6
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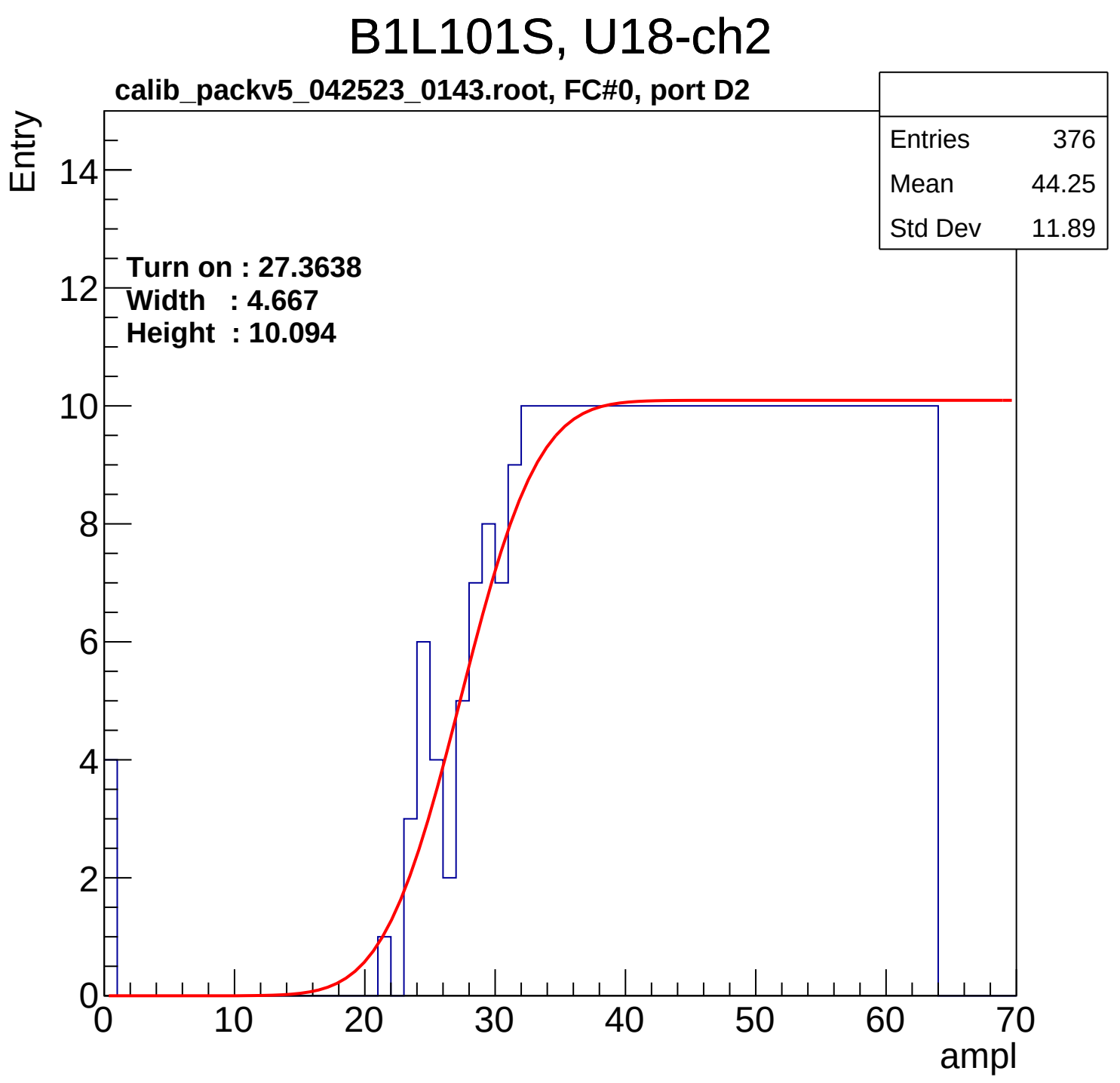
B1L101S, U18-ch2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.25
Std Dev 11.89
Turn on : 27.3638
Width : 4.667
Height : 10.094
Entry
ampl
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2
4
6
8
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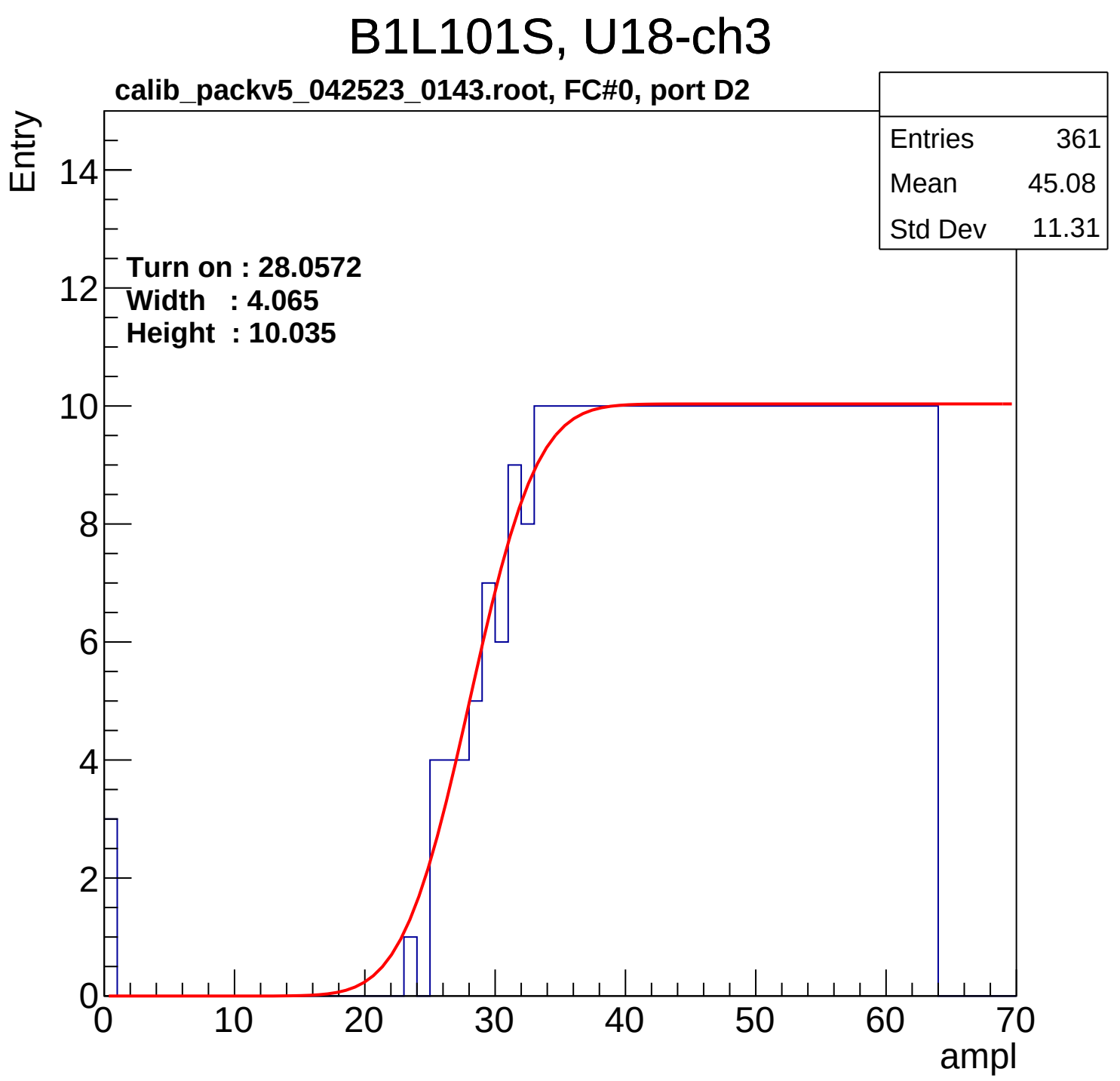
B1L101S, U18-ch3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 361
Mean 45.08
Std Dev 11.31
Turn on : 28.0572
Width : 4.065
Height : 10.035
Entry
ampl
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4
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8
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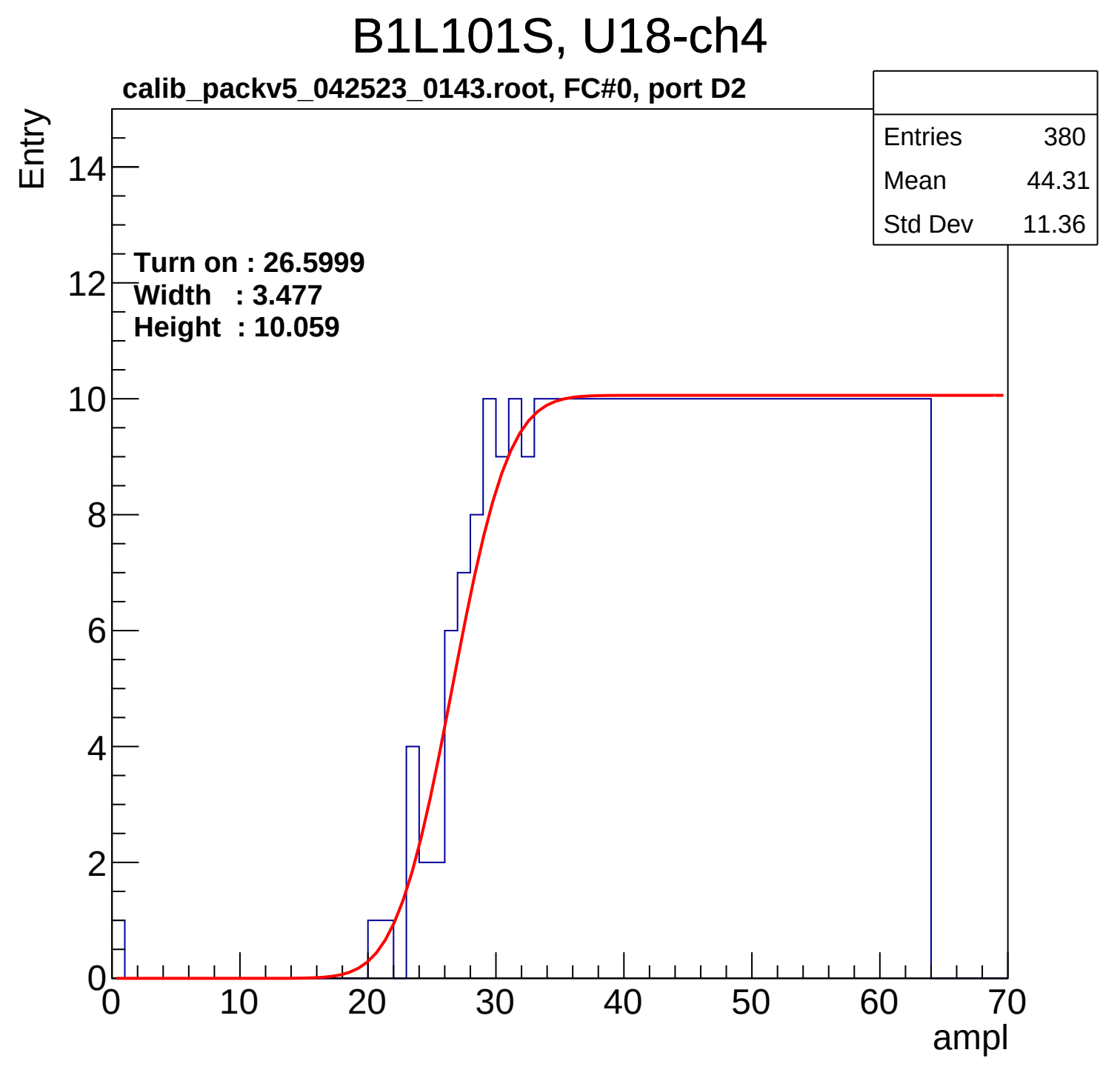
B1L101S, U18-ch4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 380
Mean 44.31
Std Dev 11.36
Turn on : 26.5999
Width : 3.477
Height : 10.059
Entry
ampl
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4
6
8
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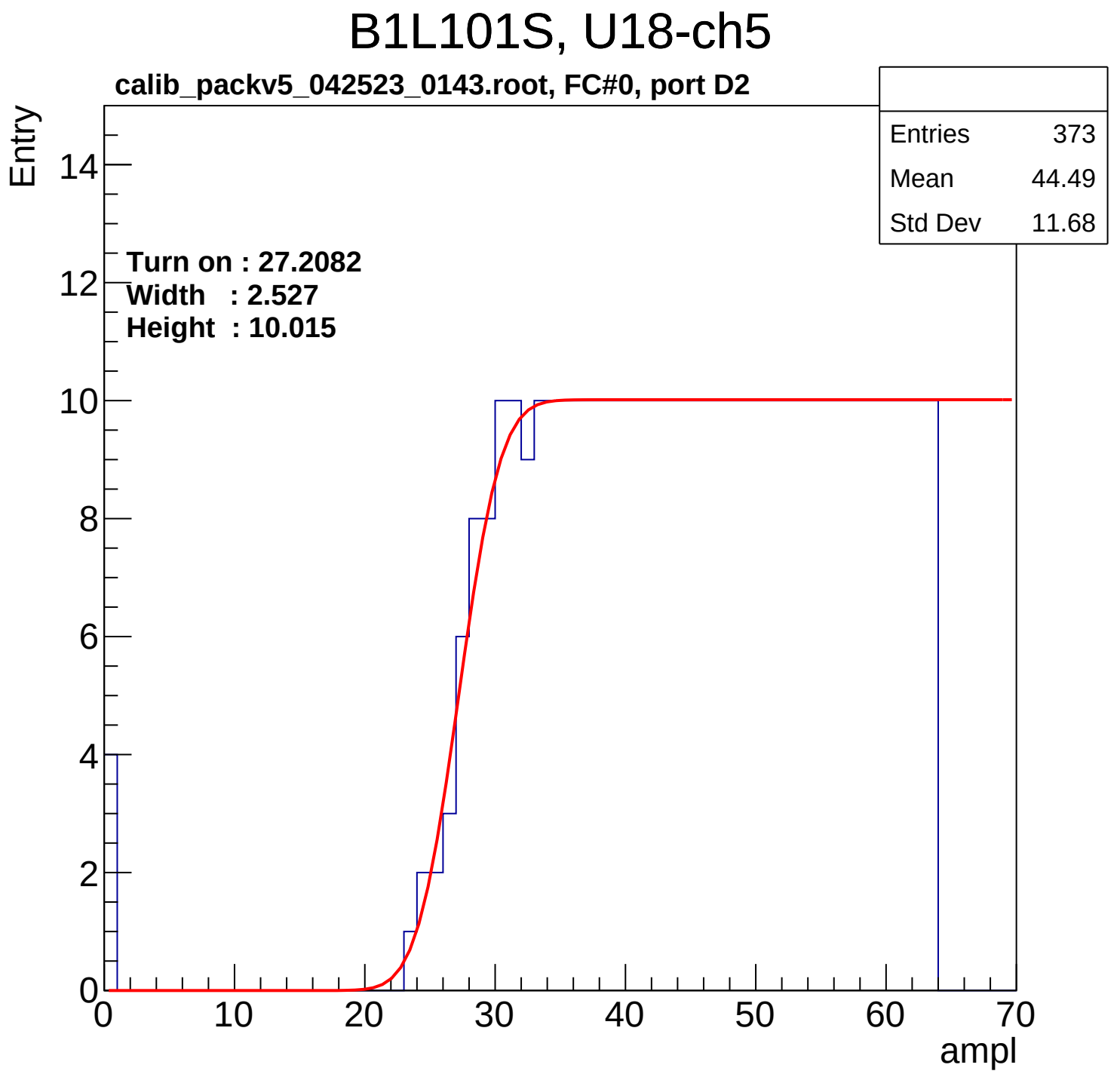
B1L101S, U18-ch5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.49
Std Dev 11.68
Turn on : 27.2082
Width : 2.527
Height : 10.015
Entry
ampl
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2
4
6
8
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0
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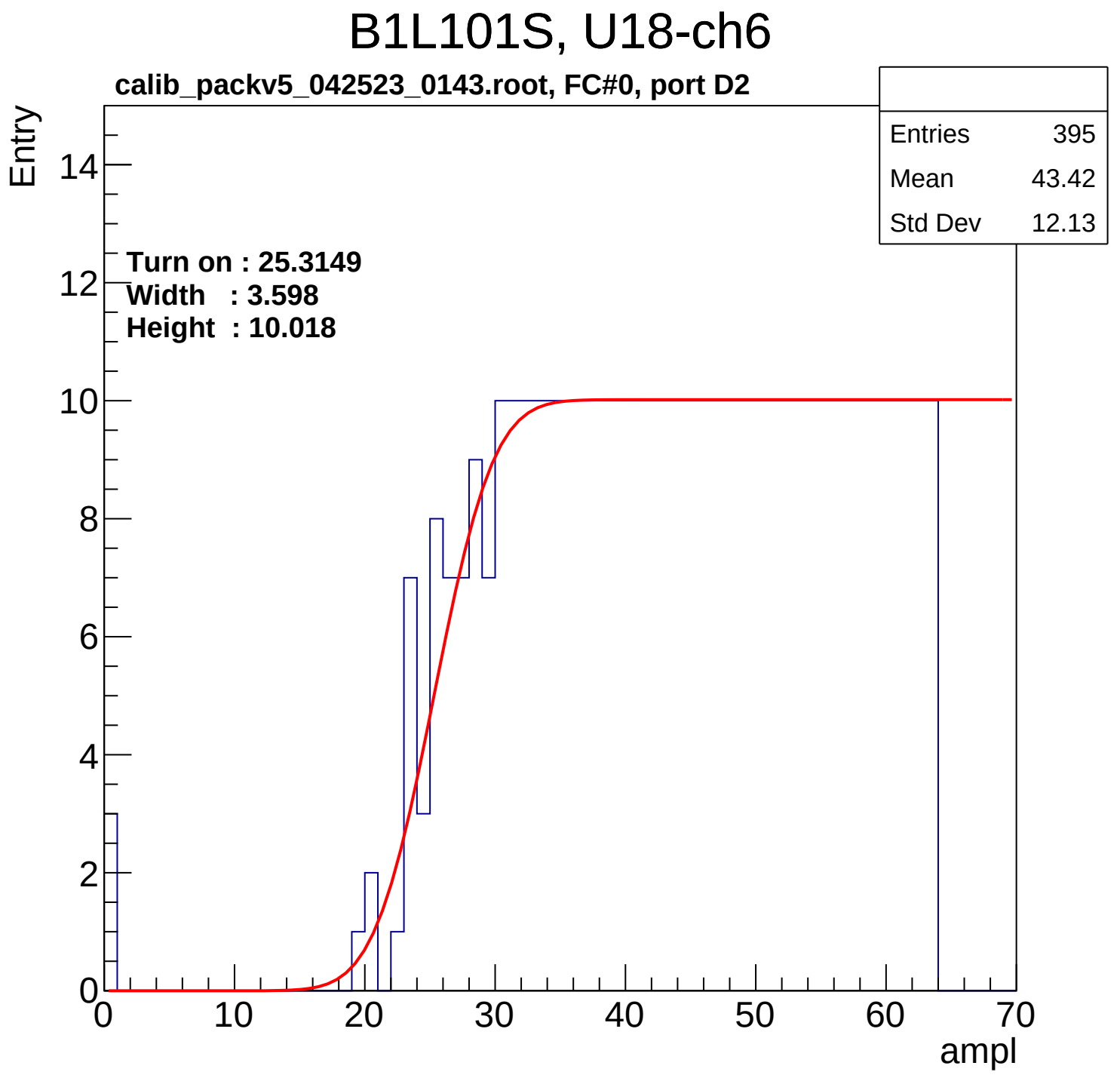
B1L101S, U18-ch6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 395
Mean 43.42
Std Dev 12.13
Turn on : 25.3149
Width : 3.598
Height : 10.018
Entry
ampl
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2
4
6
8
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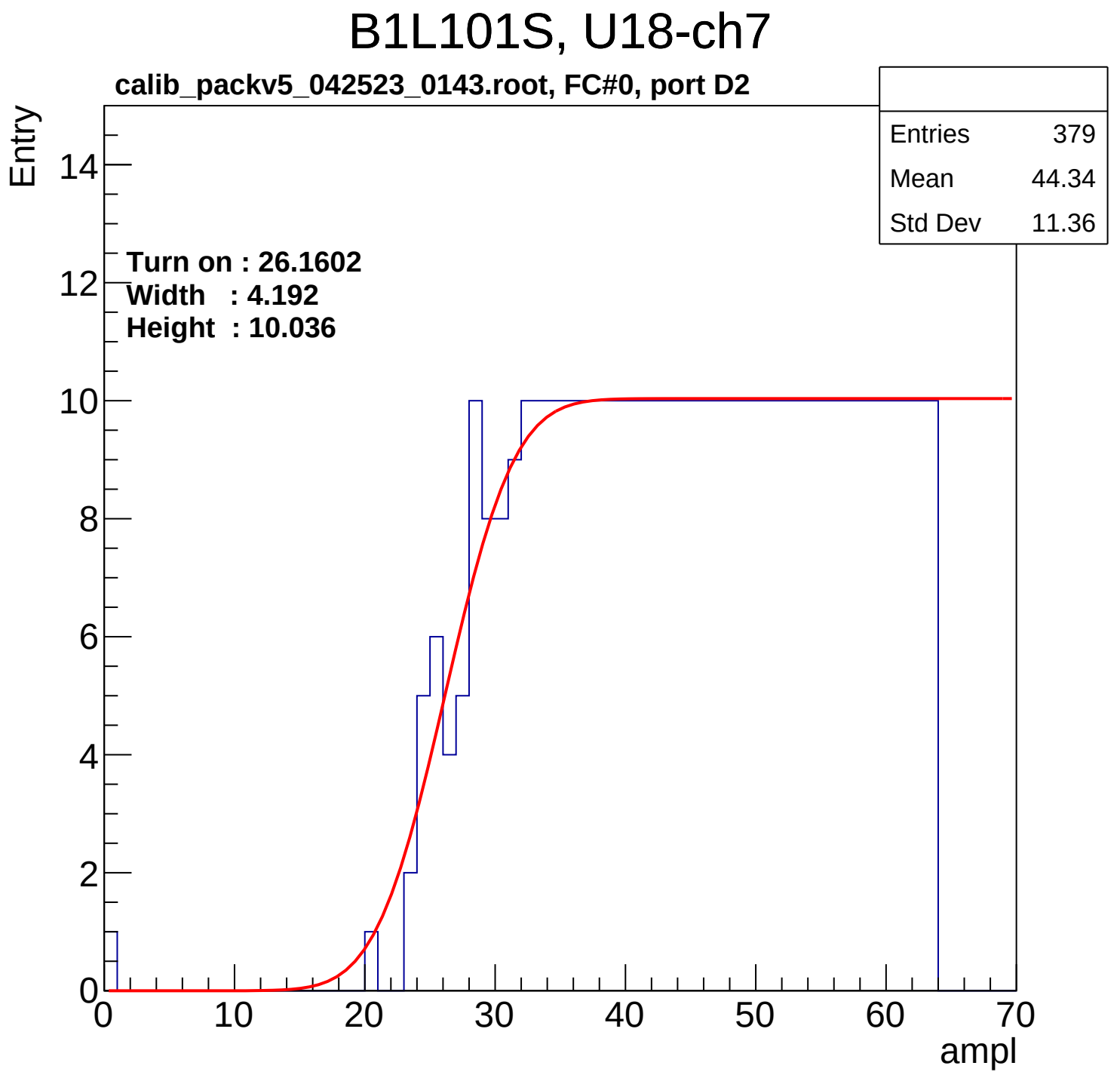
B1L101S, U18-ch7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 379
Mean 44.34
Std Dev 11.36
Turn on : 26.1602
Width : 4.192
Height : 10.036
Entry
ampl
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2
4
6
8
10
12
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0
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60
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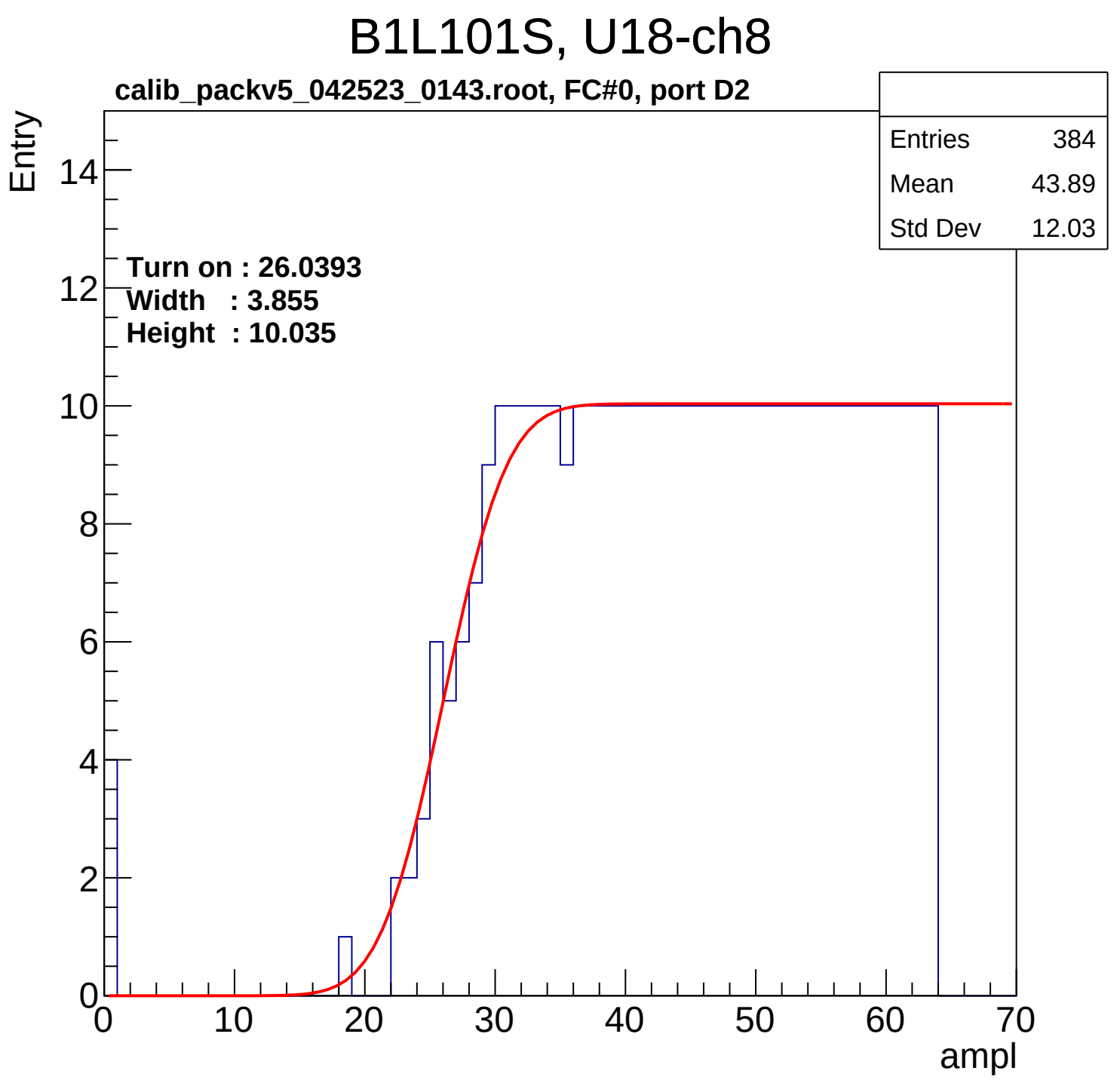
B1L101S, U18-ch8
calib_packv5_042523_0143.root, FC#0, port D2
Entries 384
Mean 43.89
Std Dev 12.03
Turn on : 26.0393
Width : 3.855
Height : 10.035
Entry
ampl
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4
6
8
10
12
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0
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60
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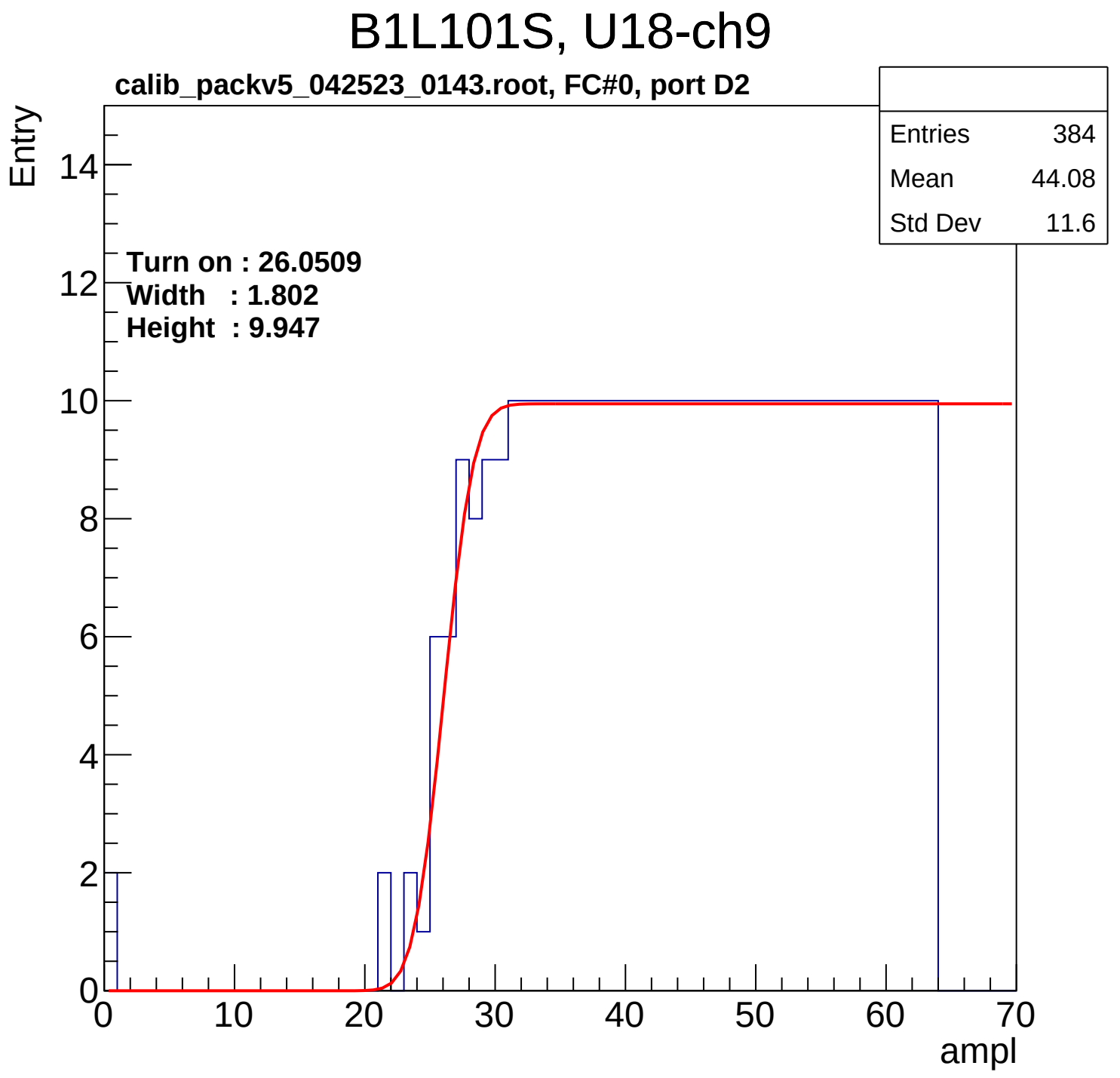
B1L101S, U18-ch9
calib_packv5_042523_0143.root, FC#0, port D2
Entries 384
Mean 44.08
Std Dev 11.6
Turn on : 26.0509
Width : 1.802
Height : 9.947
Entry
ampl
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2
4
6
8
10
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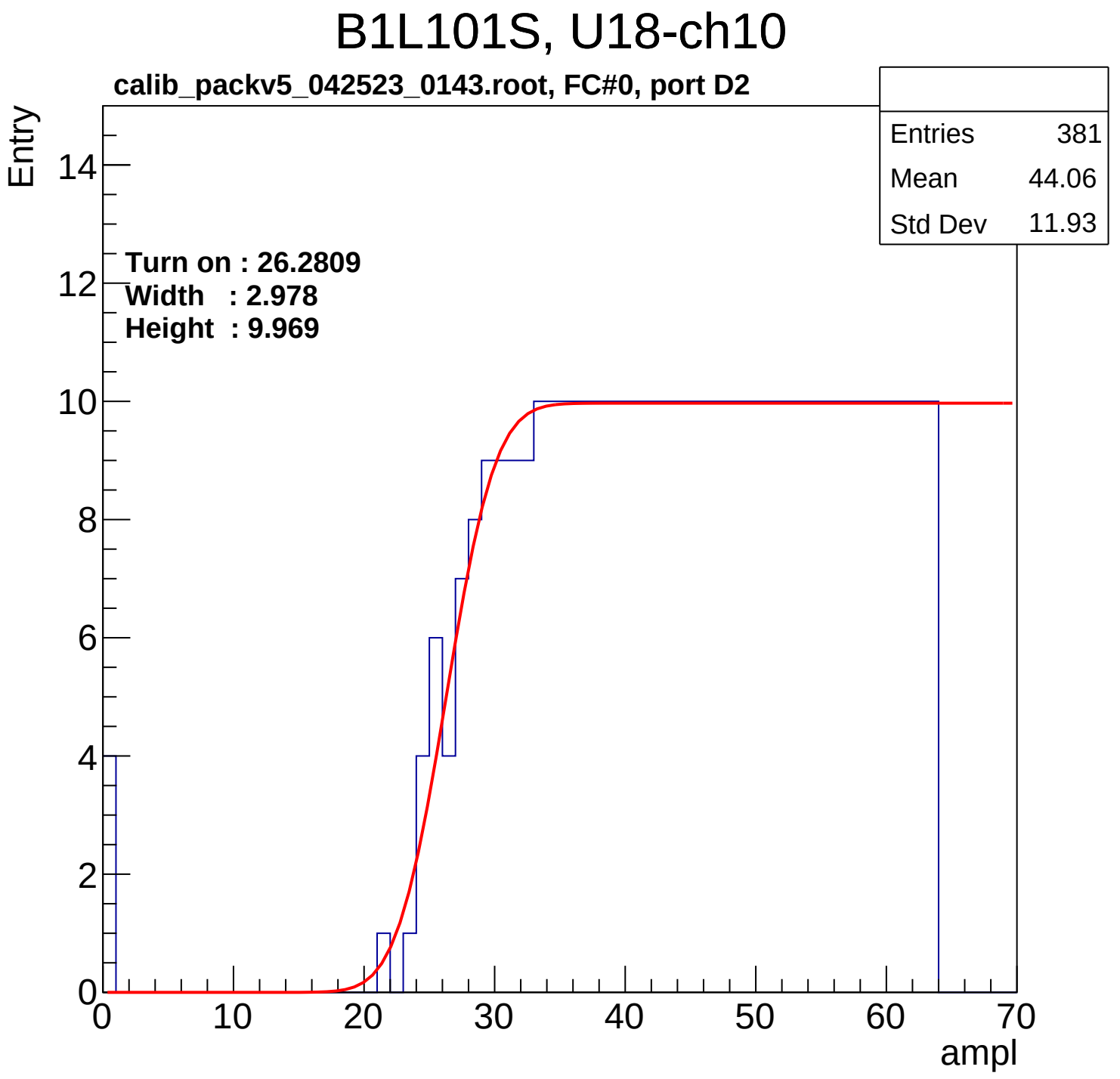
B1L101S, U18-ch10
calib_packv5_042523_0143.root, FC#0, port D2
Entries 381
Mean 44.06
Std Dev 11.93
Turn on : 26.2809
Width : 2.978
Height : 9.969
Entry
ampl
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2
4
6
8
10
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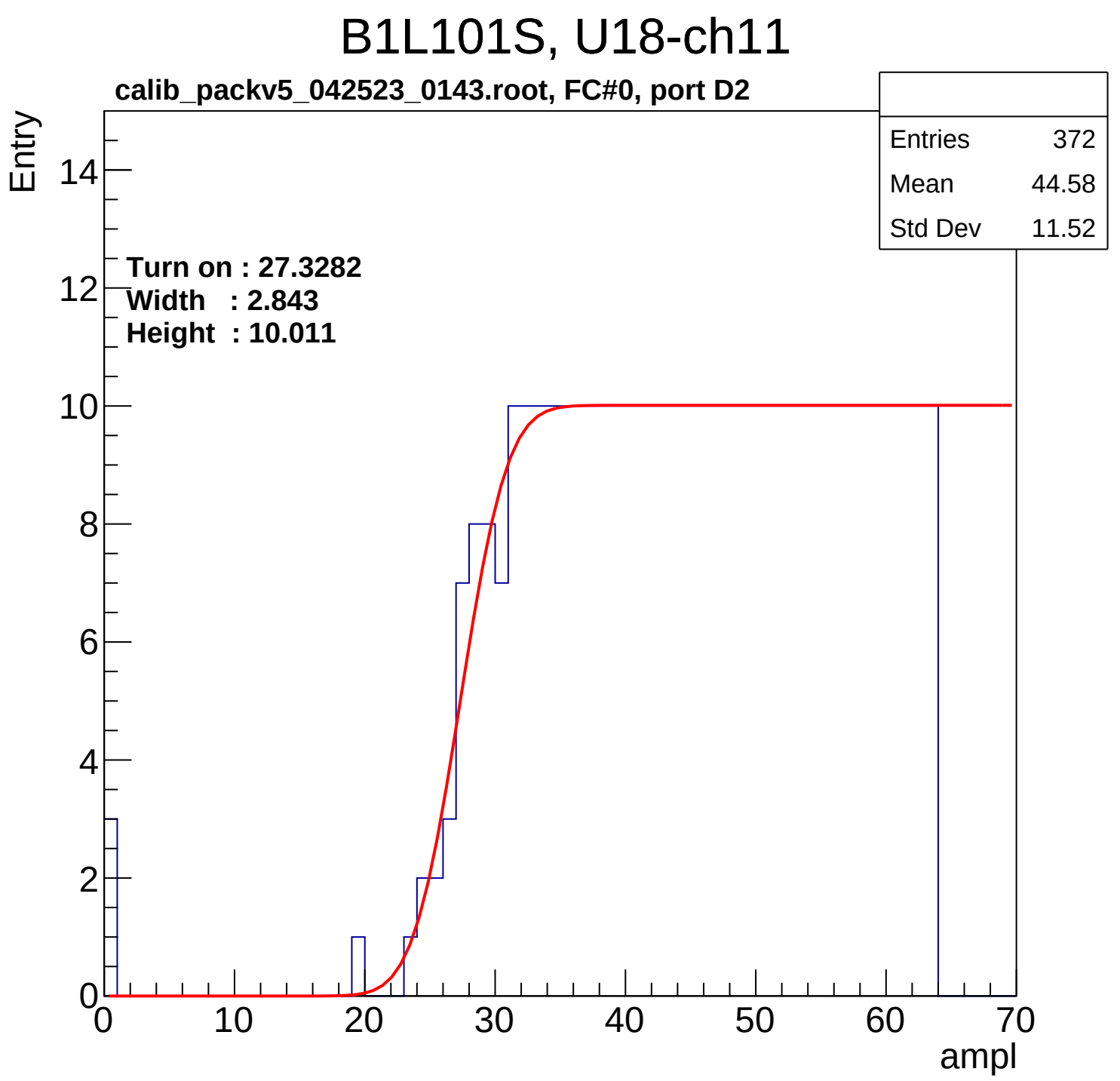
B1L101S, U18-ch11
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.58
Std Dev 11.52
Turn on : 27.3282
Width : 2.843
Height : 10.011
Entry
ampl
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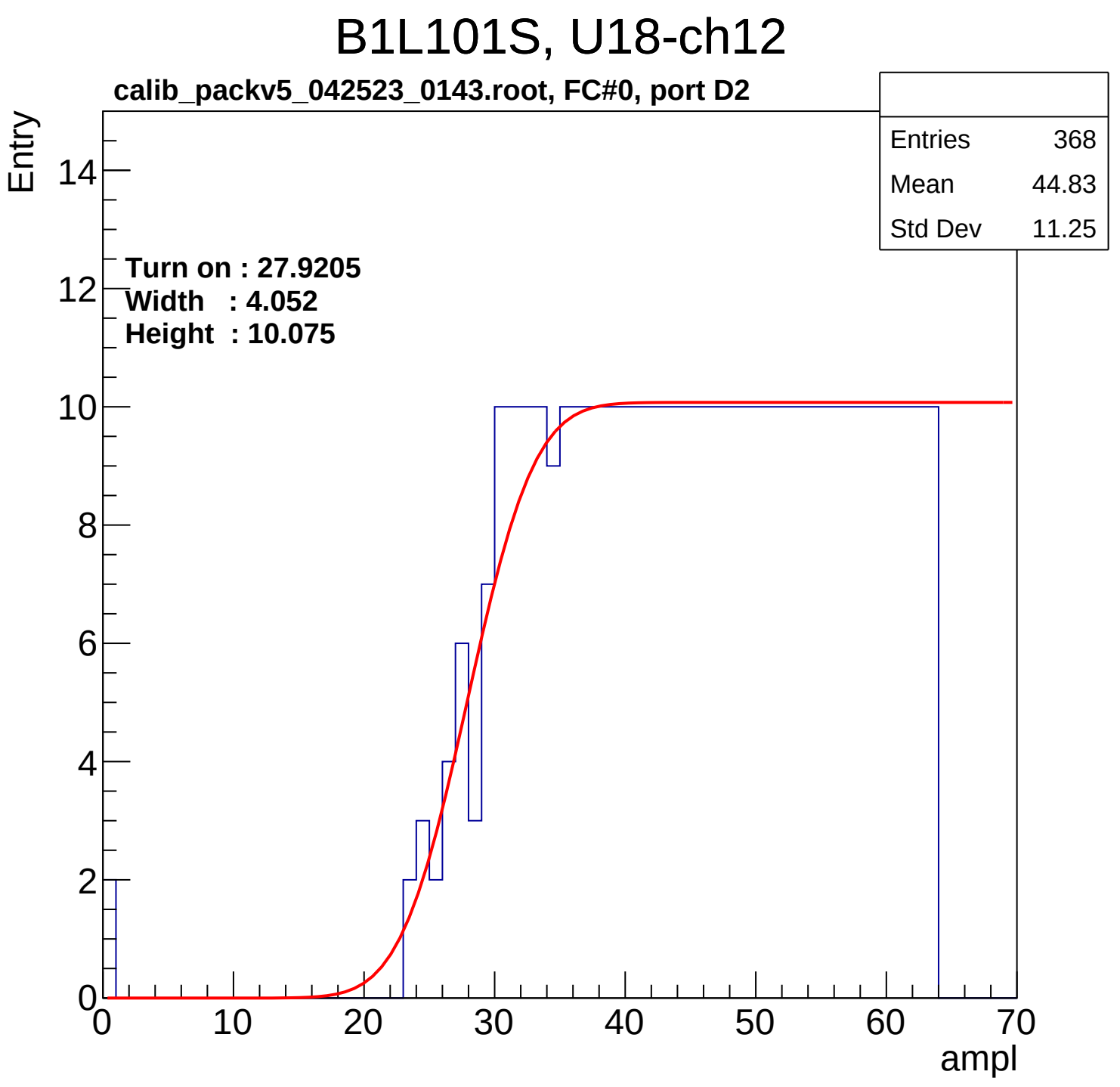
B1L101S, U18-ch12
calib_packv5_042523_0143.root, FC#0, port D2
Entries 368
Mean 44.83
Std Dev 11.25
Turn on : 27.9205
Width : 4.052
Height : 10.075
Entry
ampl
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6
8
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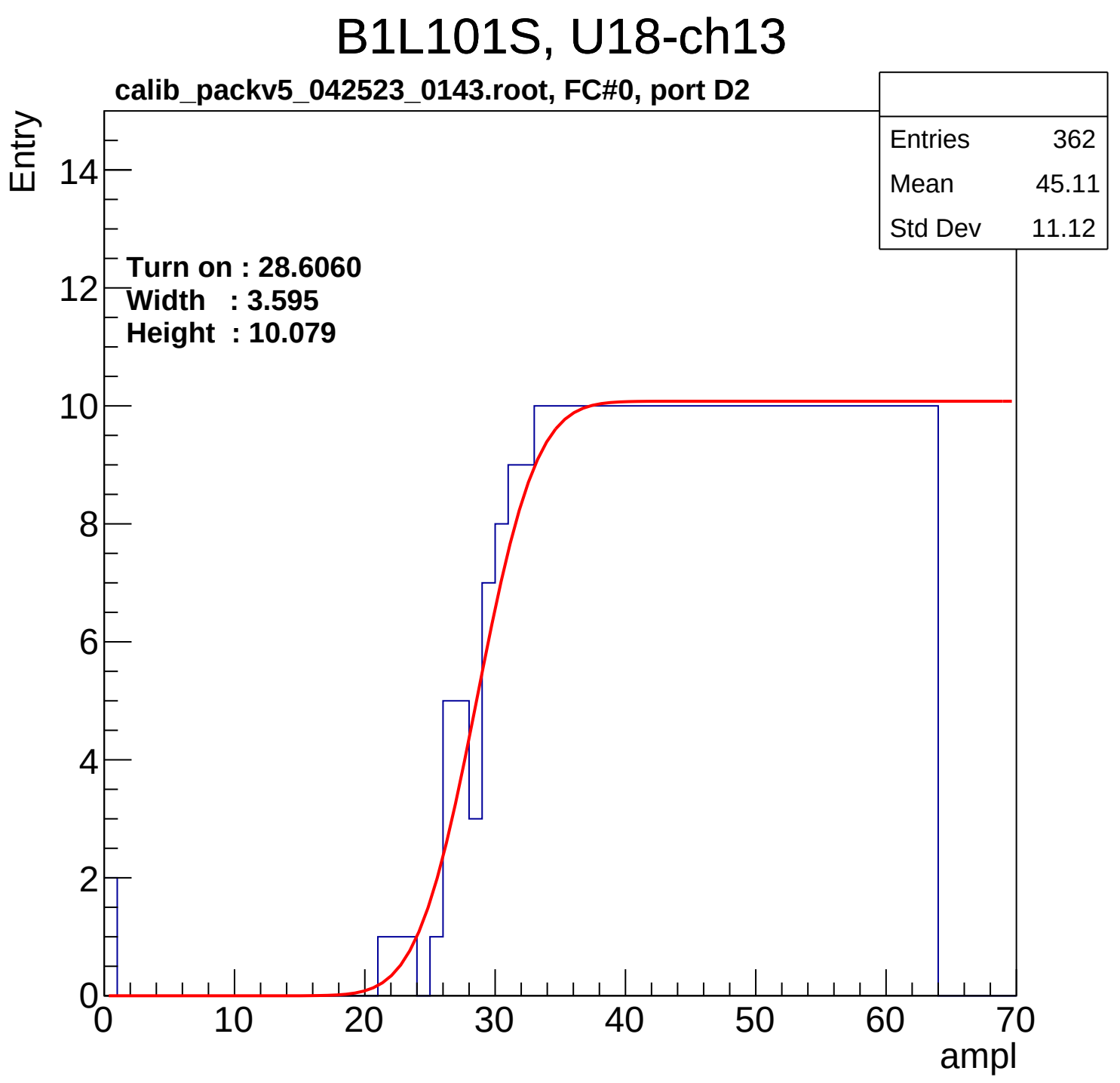
B1L101S, U18-ch13
calib_packv5_042523_0143.root, FC#0, port D2
Entries 362
Mean 45.11
Std Dev 11.12
Turn on : 28.6060
Width : 3.595
Height : 10.079
Entry
ampl
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8
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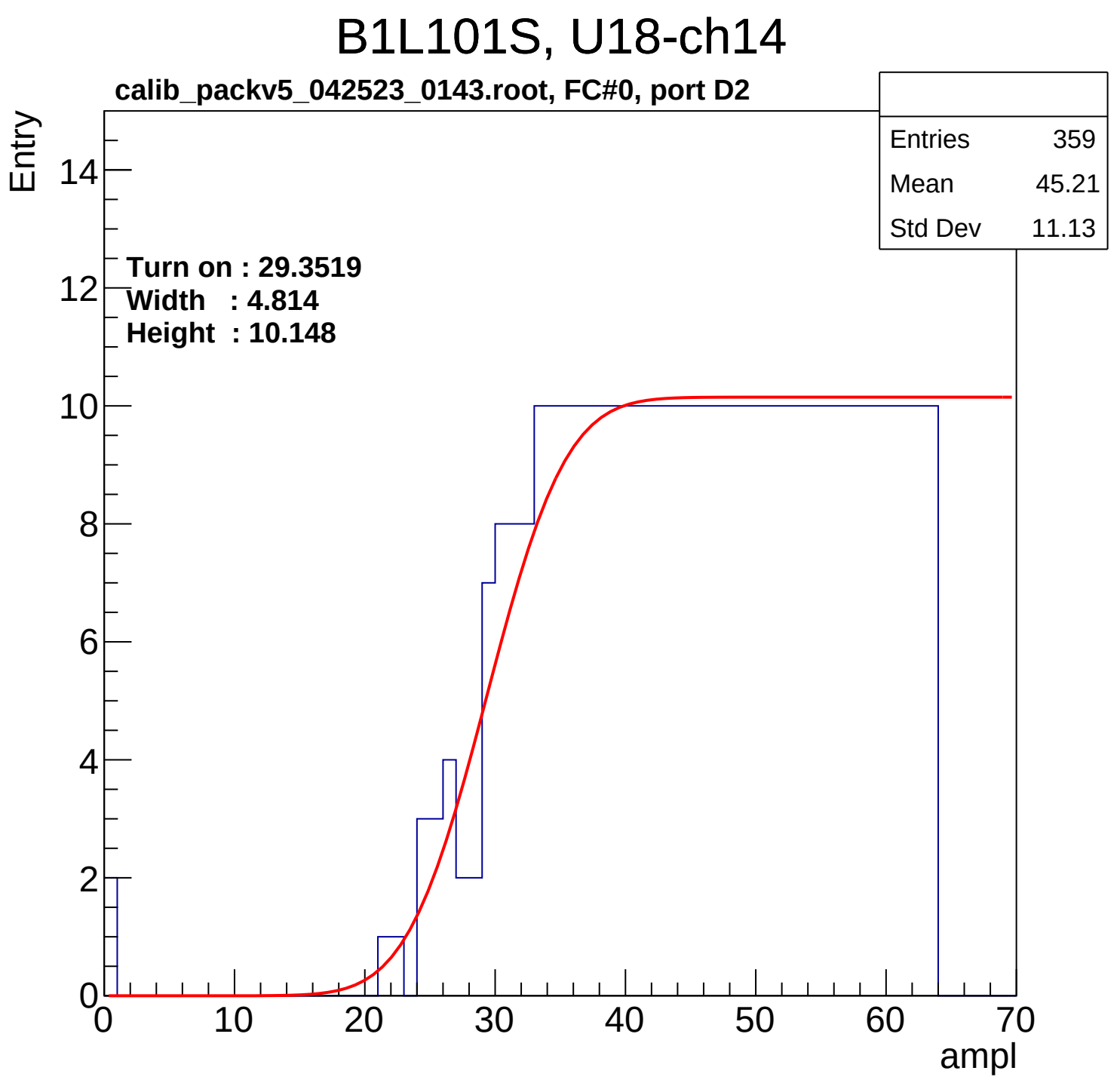
B1L101S, U18-ch14
calib_packv5_042523_0143.root, FC#0, port D2
Entries 359
Mean 45.21
Std Dev 11.13
Turn on : 29.3519
Width : 4.814
Height : 10.148
Entry
ampl
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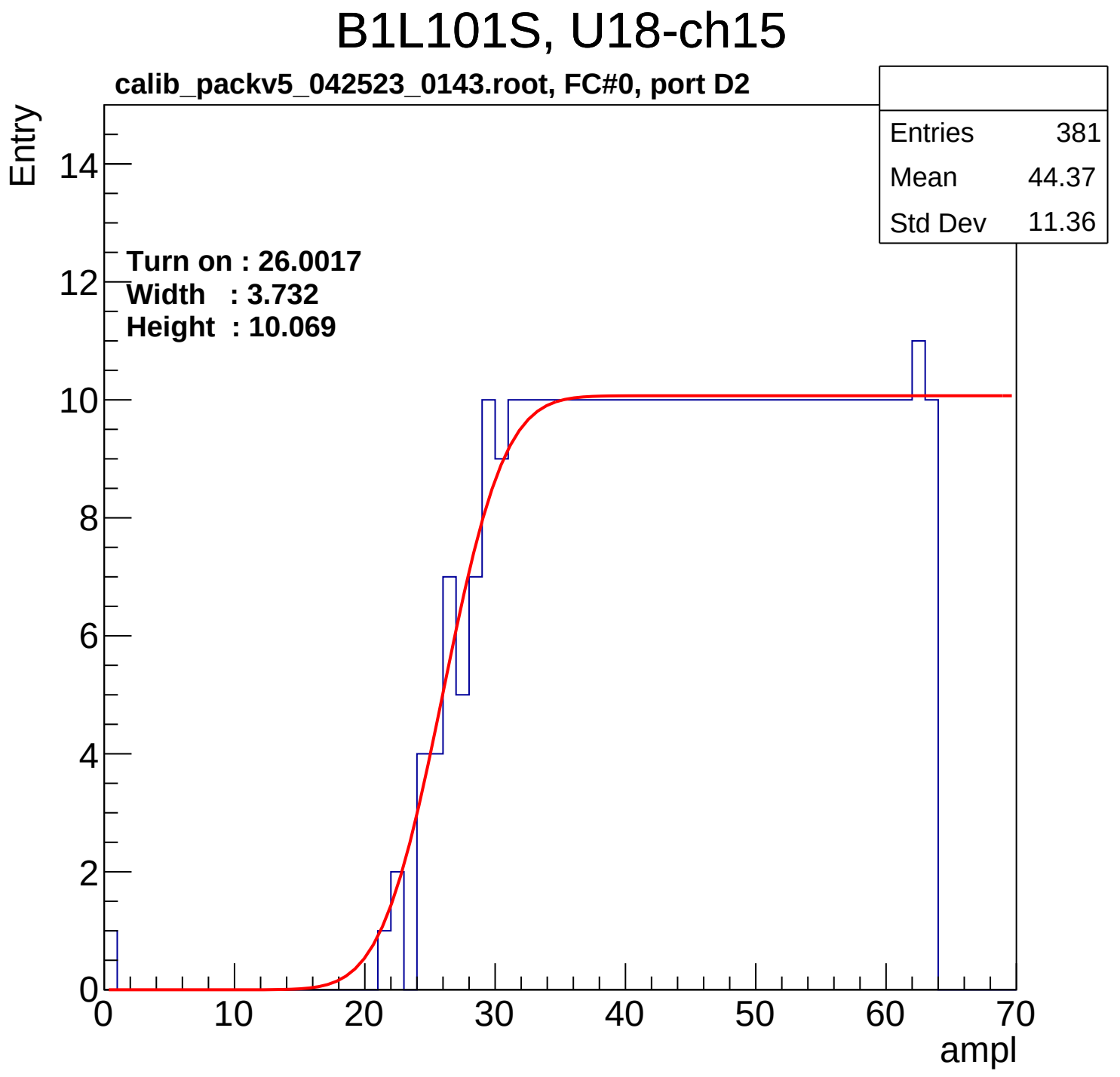
B1L101S, U18-ch15
calib_packv5_042523_0143.root, FC#0, port D2
Entries 381
Mean 44.37
Std Dev 11.36
Turn on : 26.0017
Width : 3.732
Height : 10.069
Entry
ampl
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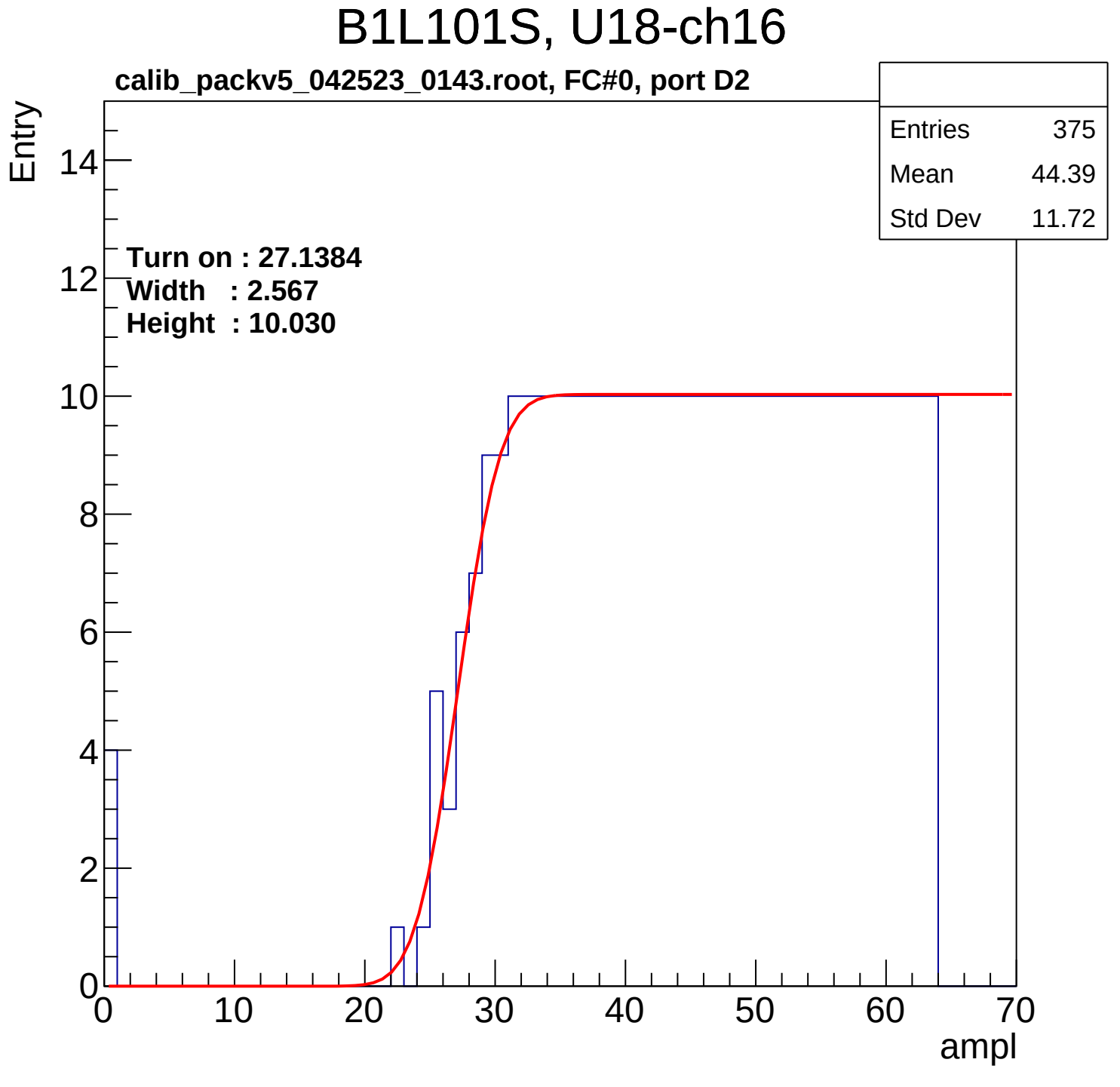
B1L101S, U18-ch16
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.39
Std Dev 11.72
Turn on : 27.1384
Width : 2.567
Height : 10.030
Entry
ampl
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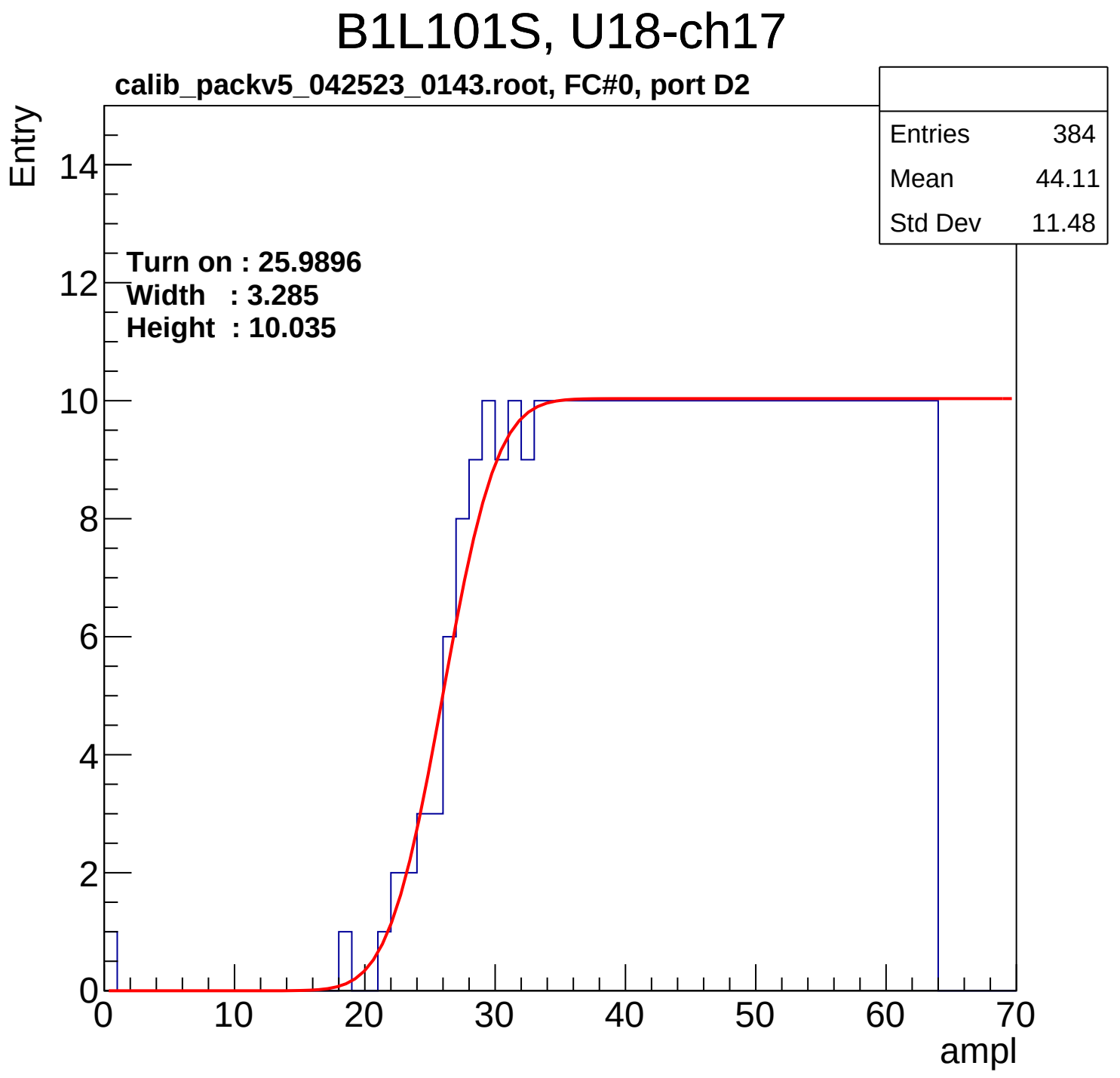
B1L101S, U18-ch17
calib_packv5_042523_0143.root, FC#0, port D2
Entries 384
Mean 44.11
Std Dev 11.48
Turn on : 25.9896
Width : 3.285
Height : 10.035
Entry
ampl
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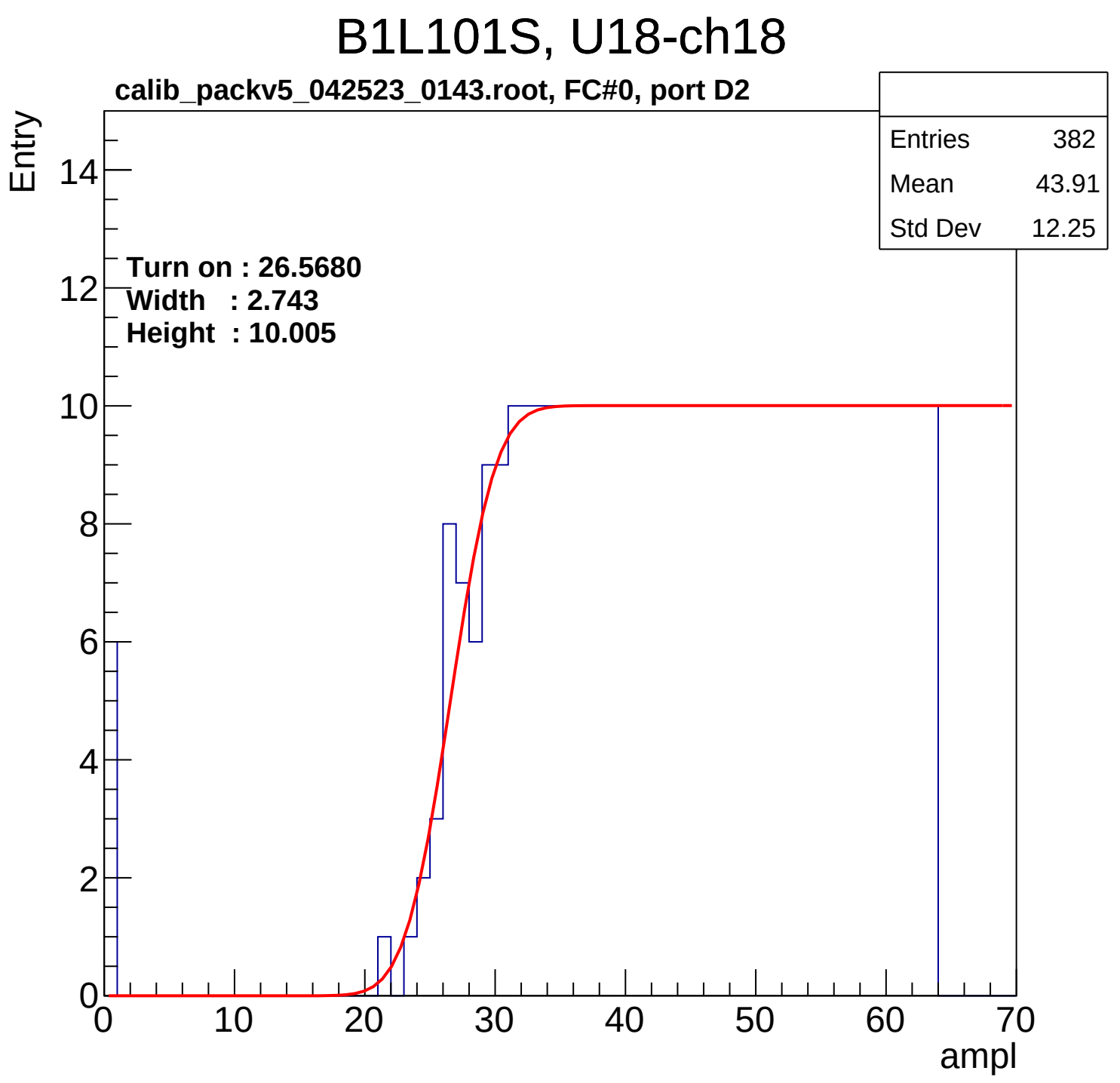
B1L101S, U18-ch18
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 43.91
Std Dev 12.25
Turn on : 26.5680
Width : 2.743
Height : 10.005
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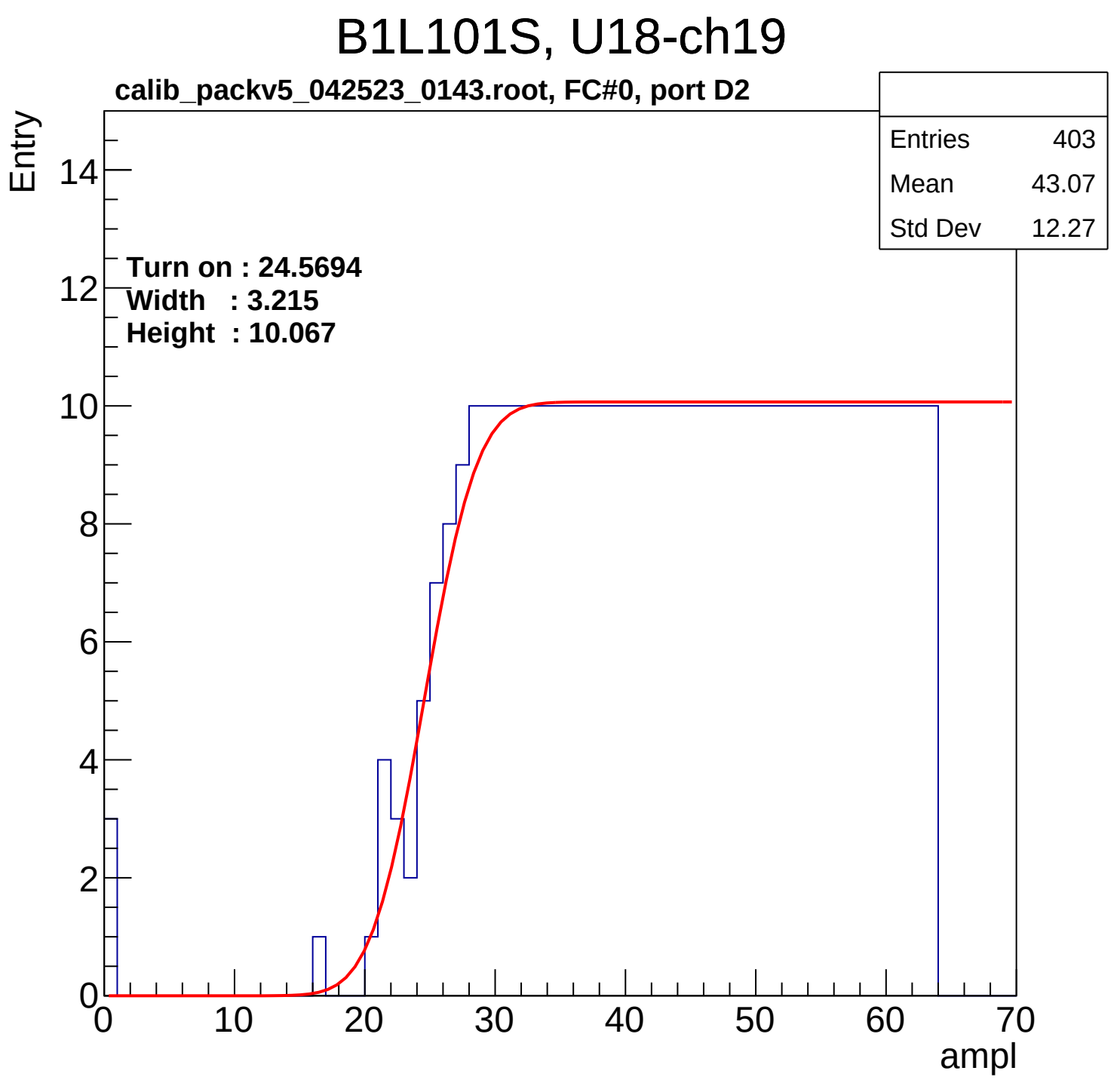
B1L101S, U18-ch19
calib_packv5_042523_0143.root, FC#0, port D2
Entries 403
Mean 43.07
Std Dev 12.27
Turn on : 24.5694
Width : 3.215
Height : 10.067
Entry
ampl
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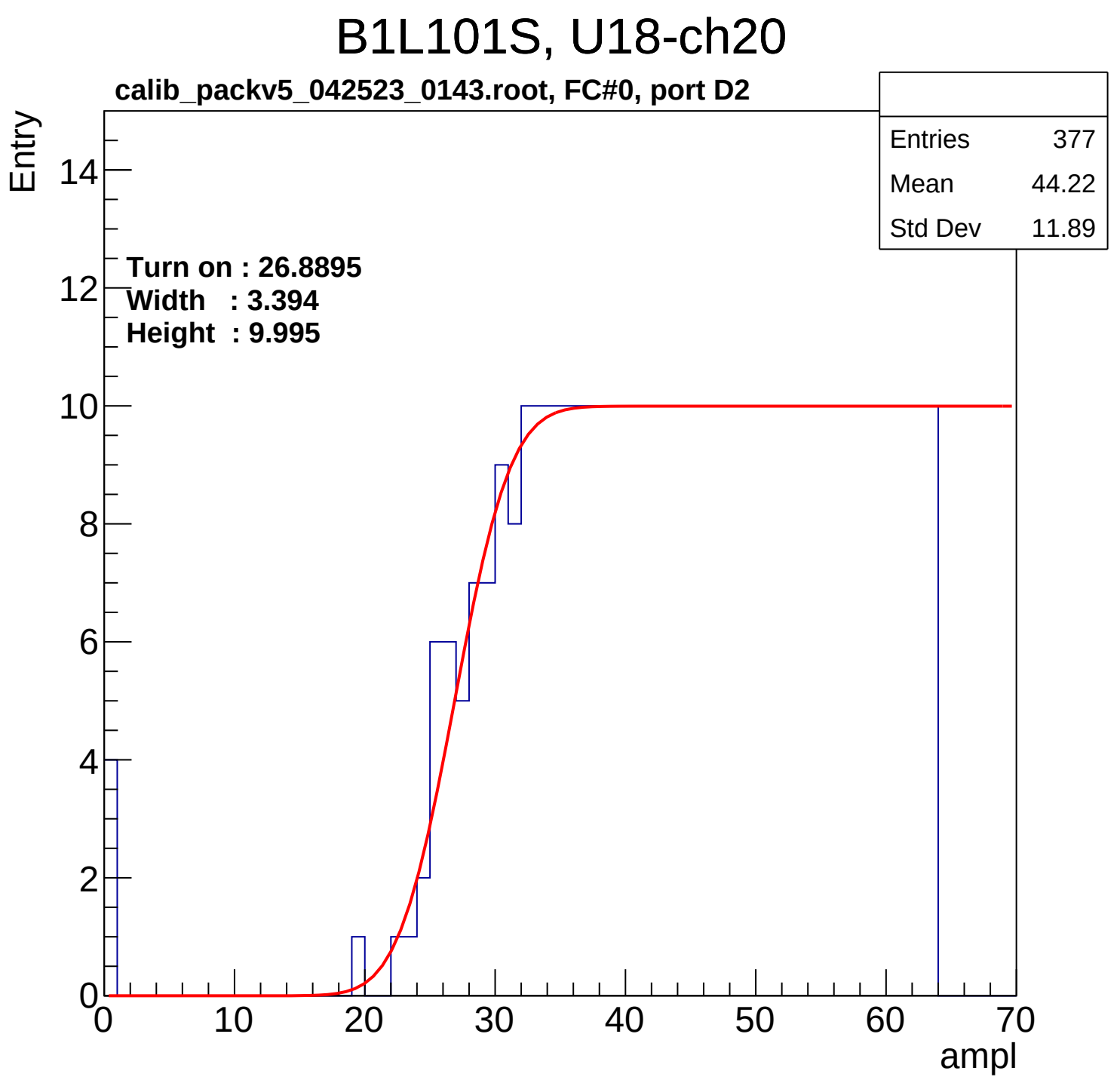
B1L101S, U18-ch20
calib_packv5_042523_0143.root, FC#0, port D2
Entries 377
Mean 44.22
Std Dev 11.89
Turn on : 26.8895
Width : 3.394
Height : 9.995
Entry
ampl
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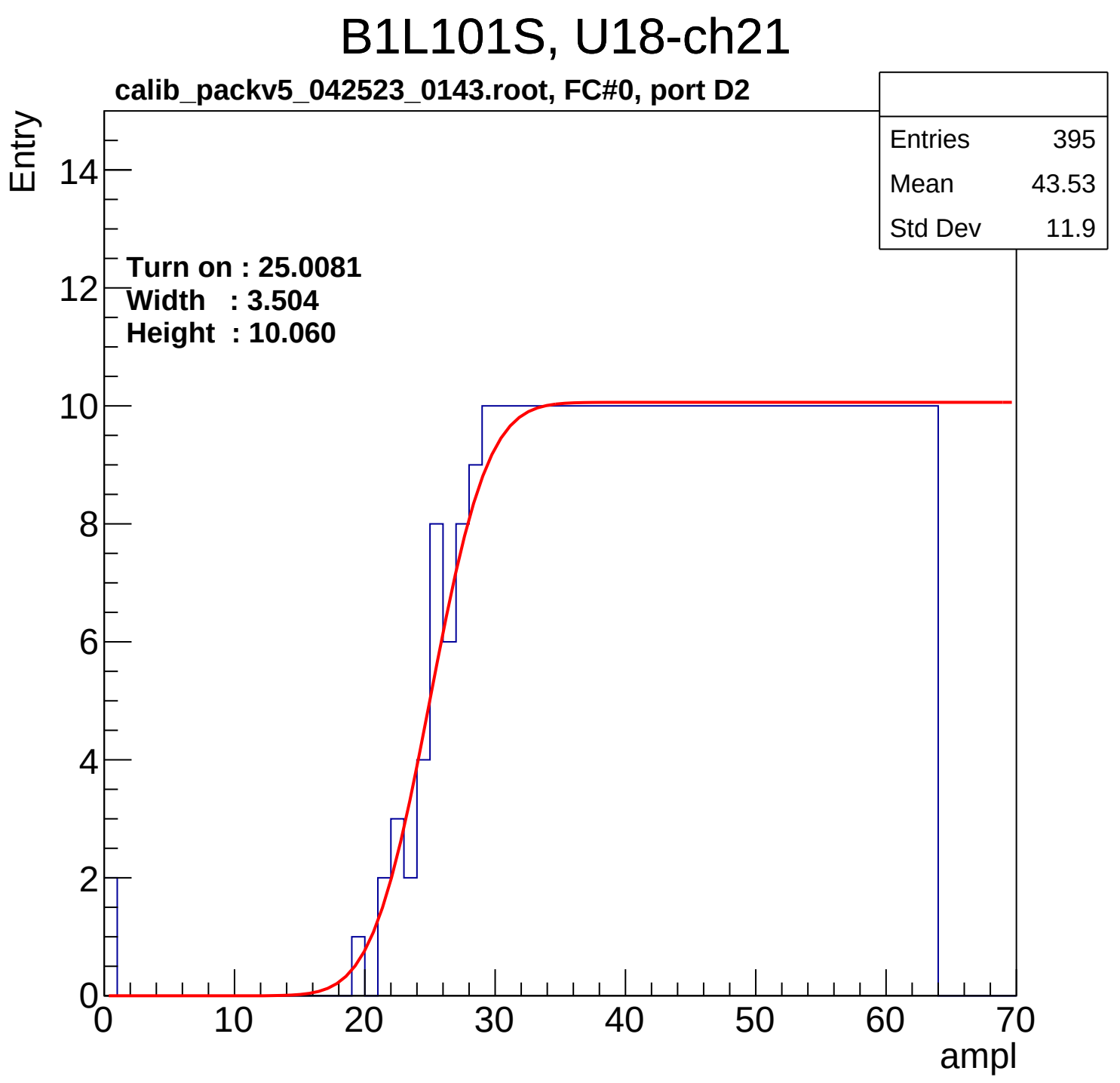
B1L101S, U18-ch21
calib_packv5_042523_0143.root, FC#0, port D2
Entries 395
Mean 43.53
Std Dev 11.9
Turn on : 25.0081
Width : 3.504
Height : 10.060
Entry
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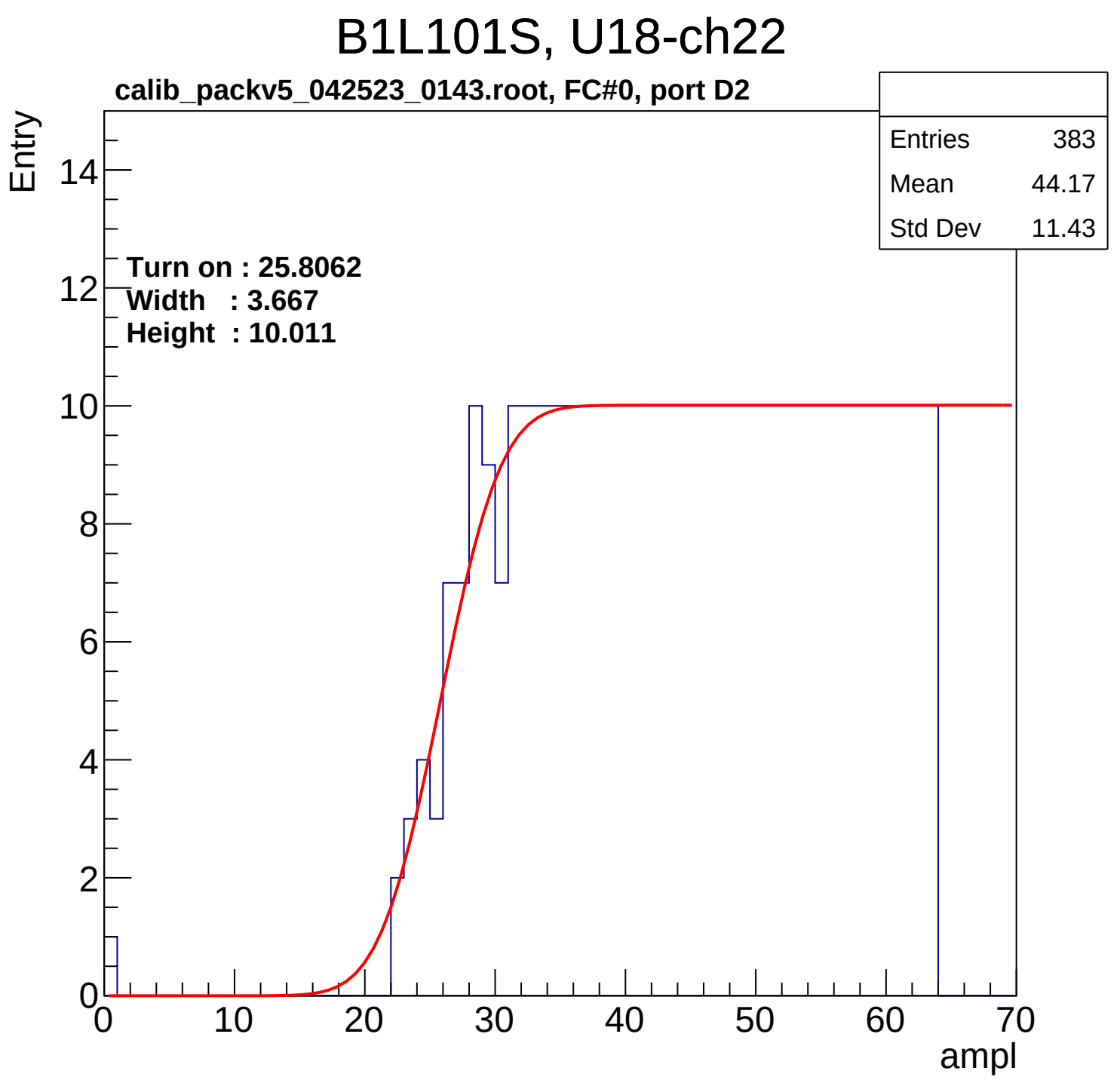
B1L101S, U18-ch22
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 44.17
Std Dev 11.43
Turn on : 25.8062
Width : 3.667
Height : 10.011
Entry
ampl
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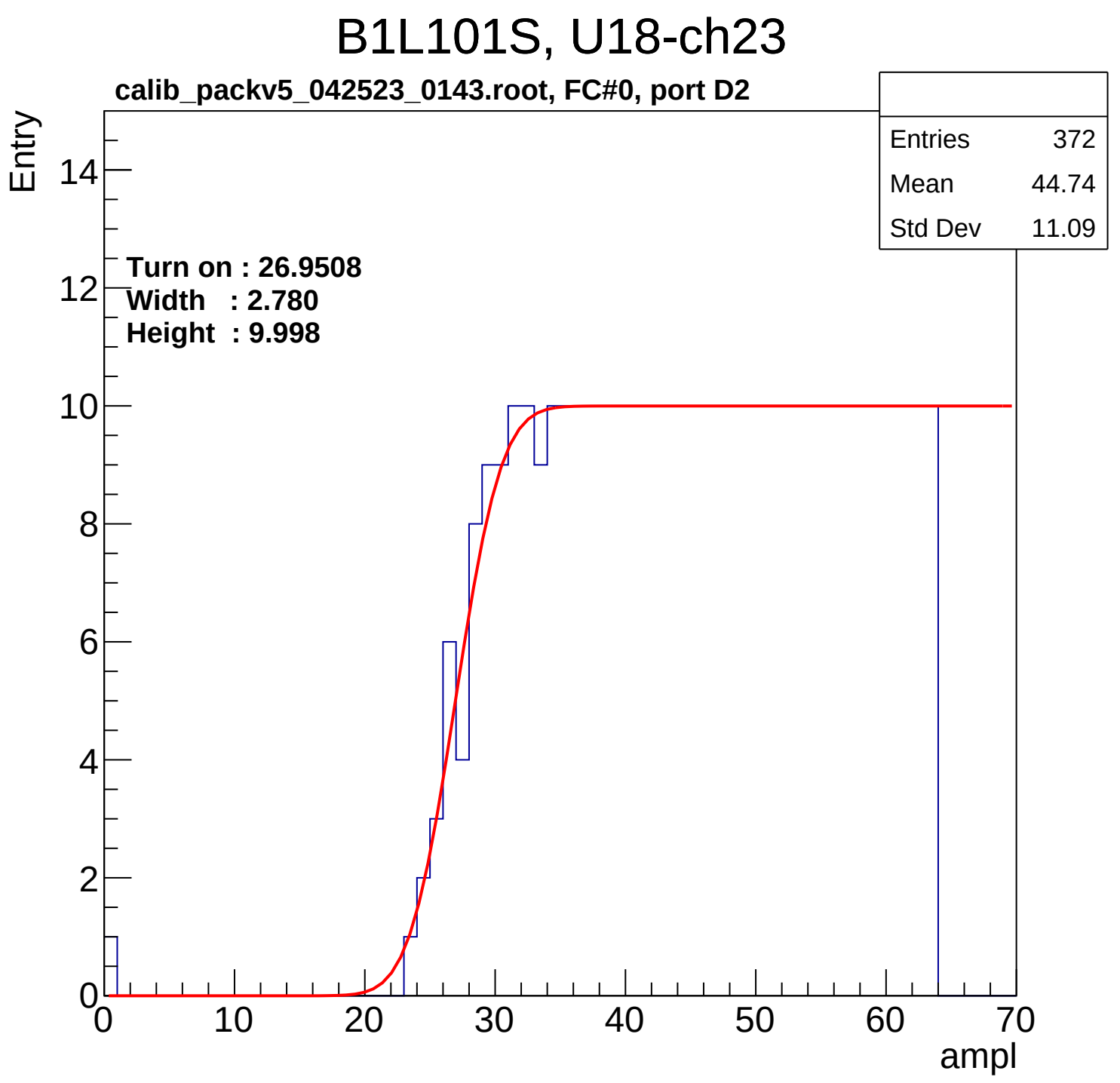
B1L101S, U18-ch23
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.74
Std Dev 11.09
Turn on : 26.9508
Width : 2.780
Height : 9.998
Entry
ampl
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6
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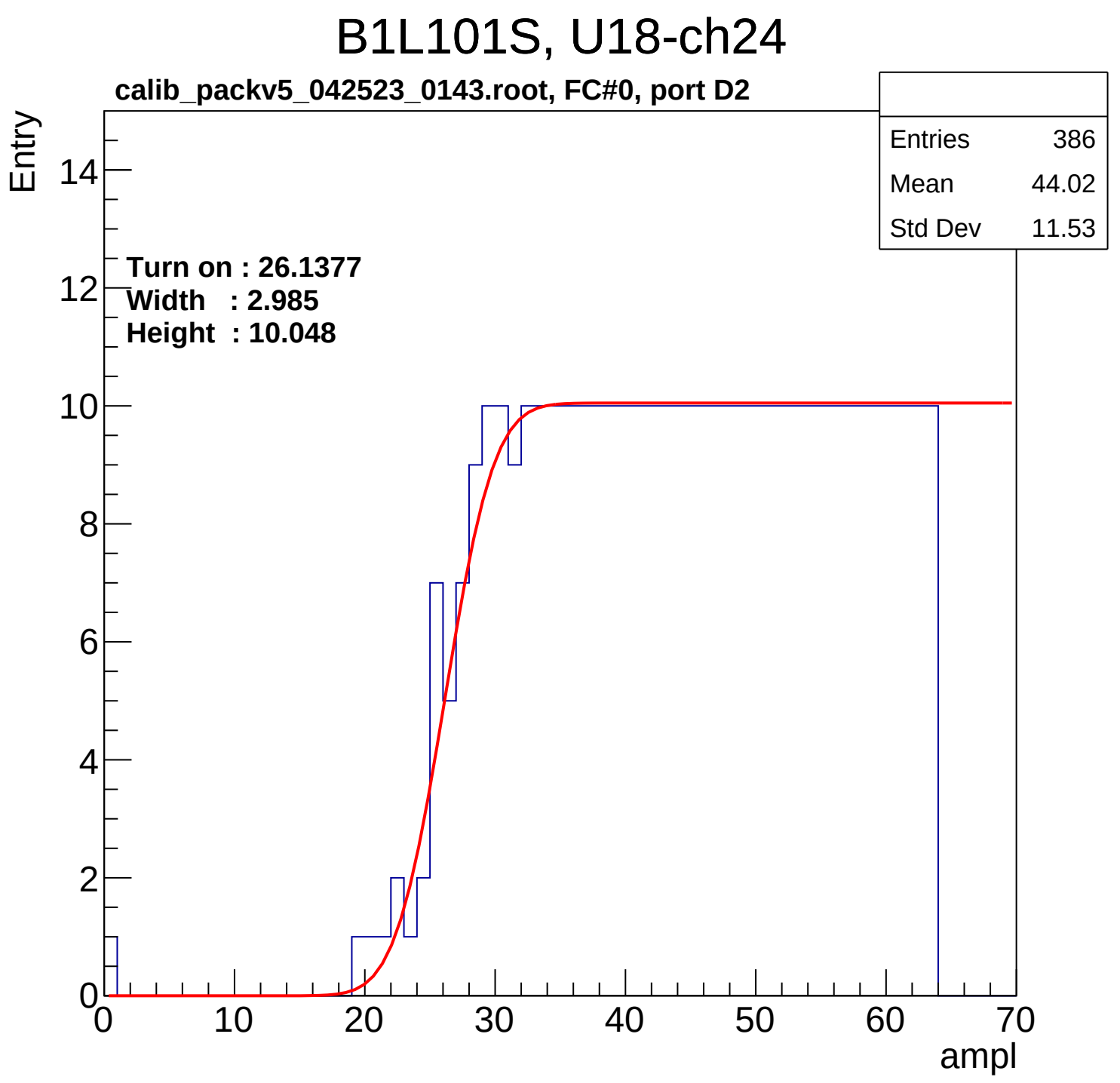
B1L101S, U18-ch24
calib_packv5_042523_0143.root, FC#0, port D2
Entries 386
Mean 44.02
Std Dev 11.53
Turn on : 26.1377
Width : 2.985
Height : 10.048
Entry
ampl
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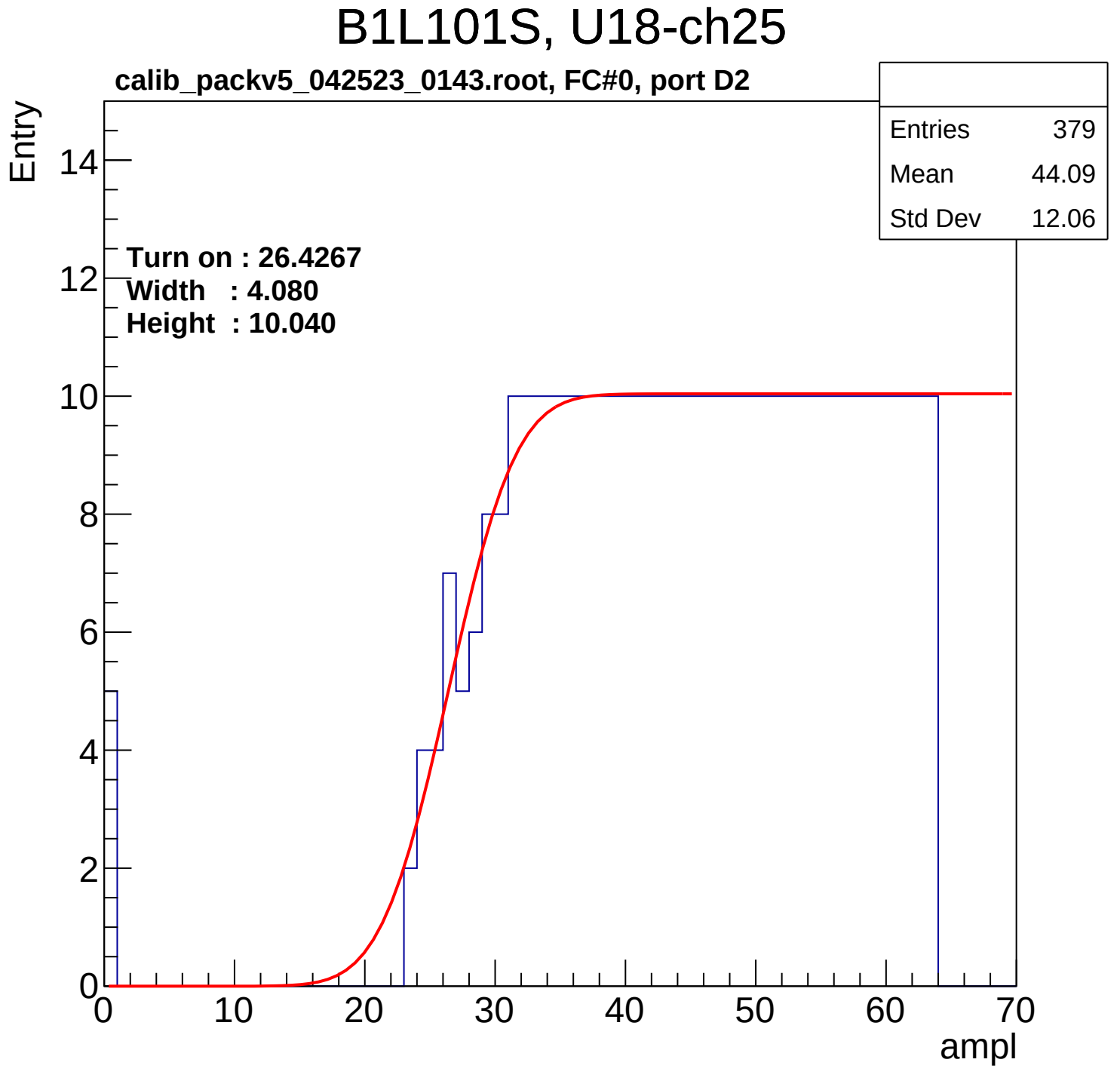
B1L101S, U18-ch25
calib_packv5_042523_0143.root, FC#0, port D2
Entries 379
Mean 44.09
Std Dev 12.06
Turn on : 26.4267
Width : 4.080
Height : 10.040
Entry
ampl
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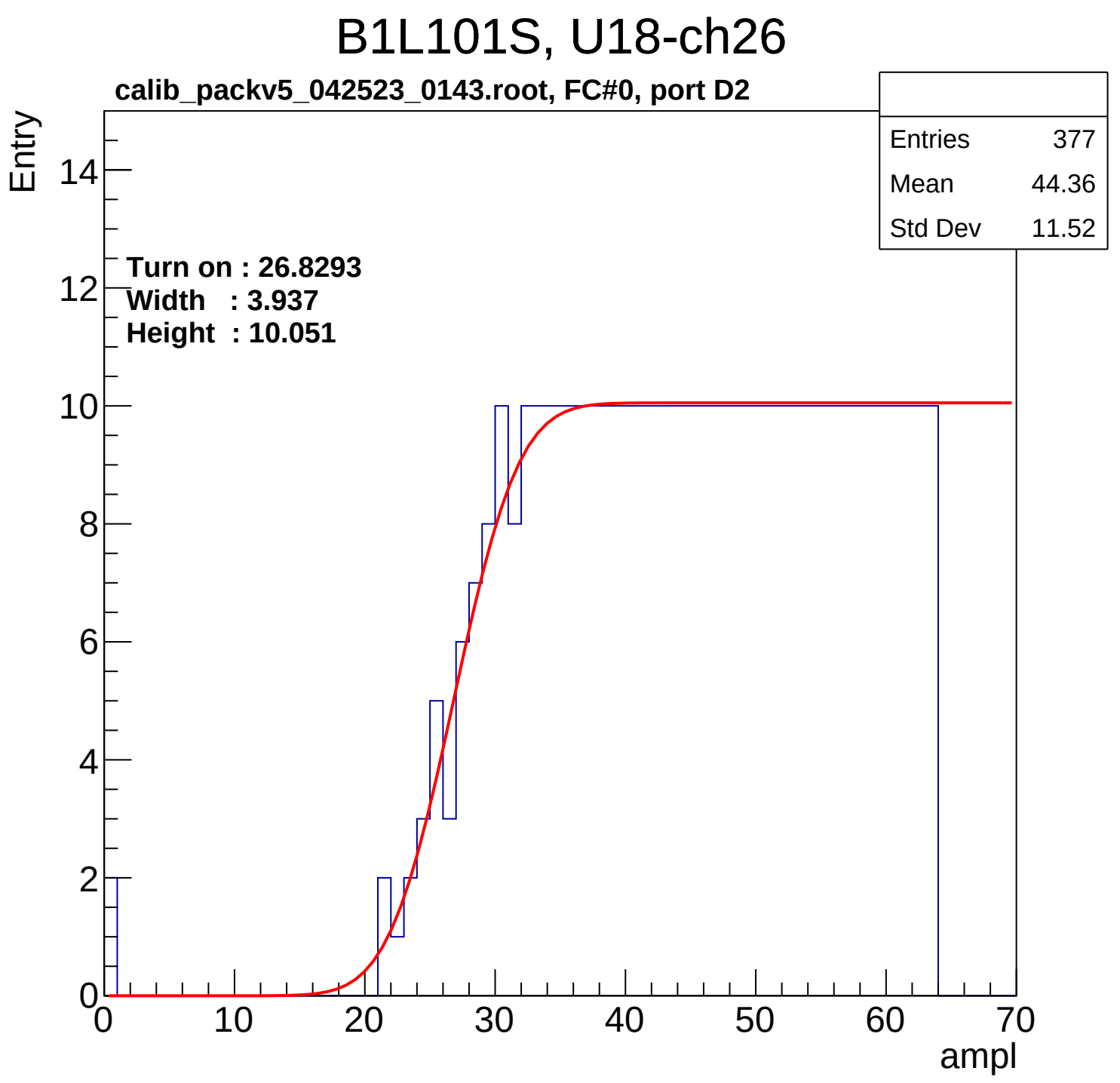
B1L101S, U18-ch26
calib_packv5_042523_0143.root, FC#0, port D2
Entries 377
Mean 44.36
Std Dev 11.52
Turn on : 26.8293
Width : 3.937
Height : 10.051
Entry
ampl
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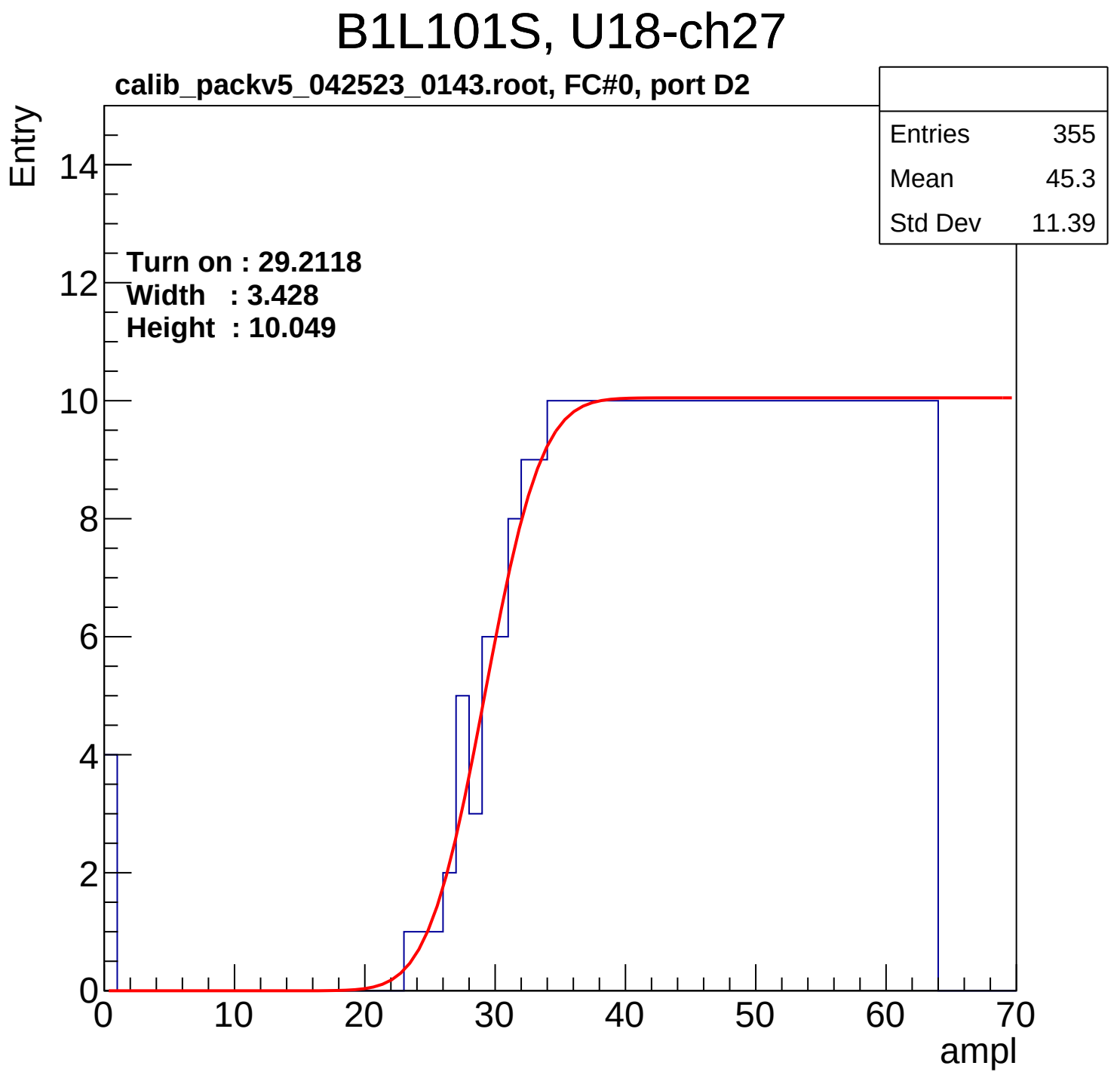
B1L101S, U18-ch27
calib_packv5_042523_0143.root, FC#0, port D2
Entries 355
Mean 45.3
Std Dev 11.39
Turn on : 29.2118
Width : 3.428
Height : 10.049
Entry
ampl
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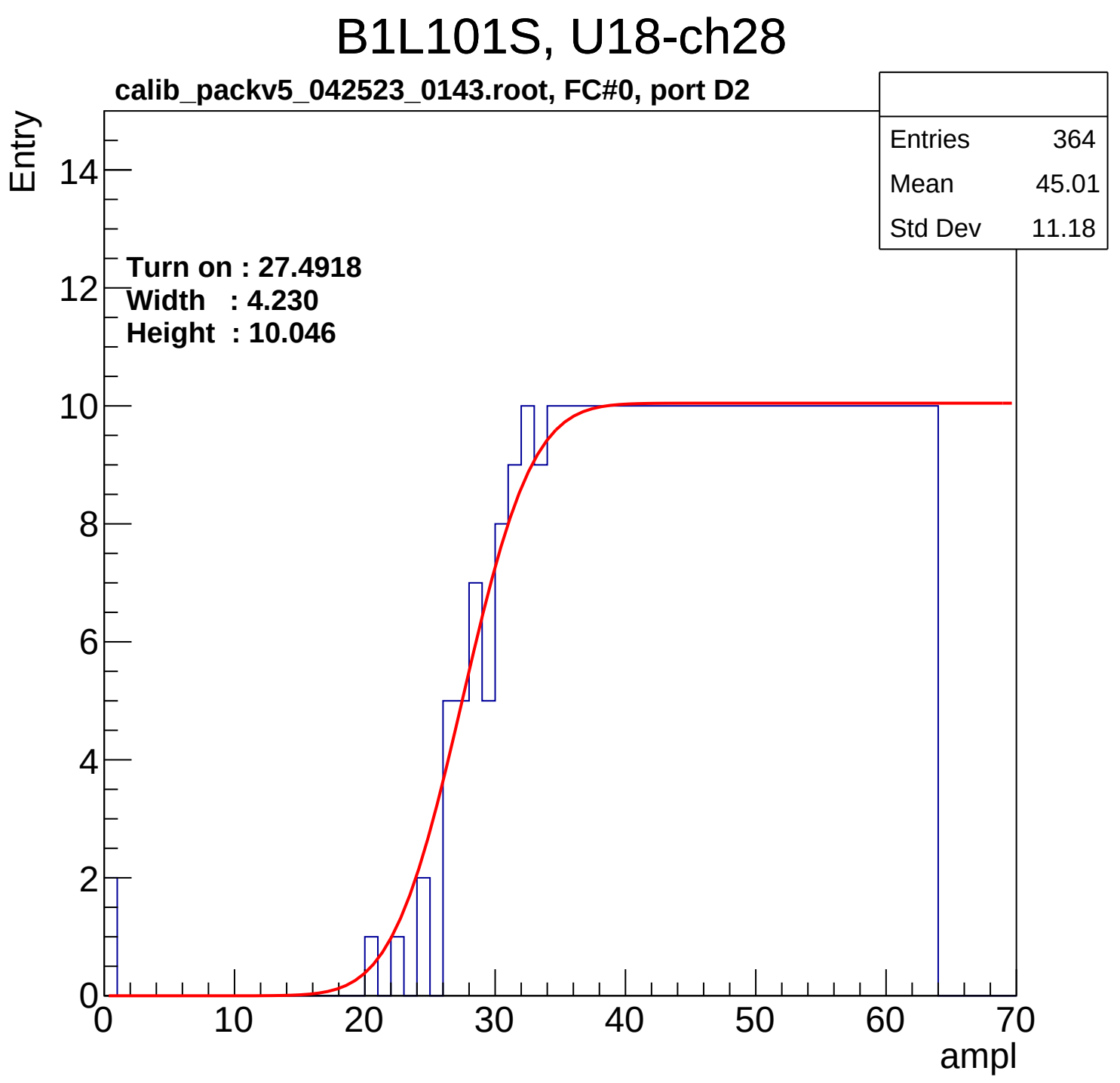
B1L101S, U18-ch28
calib_packv5_042523_0143.root, FC#0, port D2
Entries 364
Mean 45.01
Std Dev 11.18
Turn on : 27.4918
Width : 4.230
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
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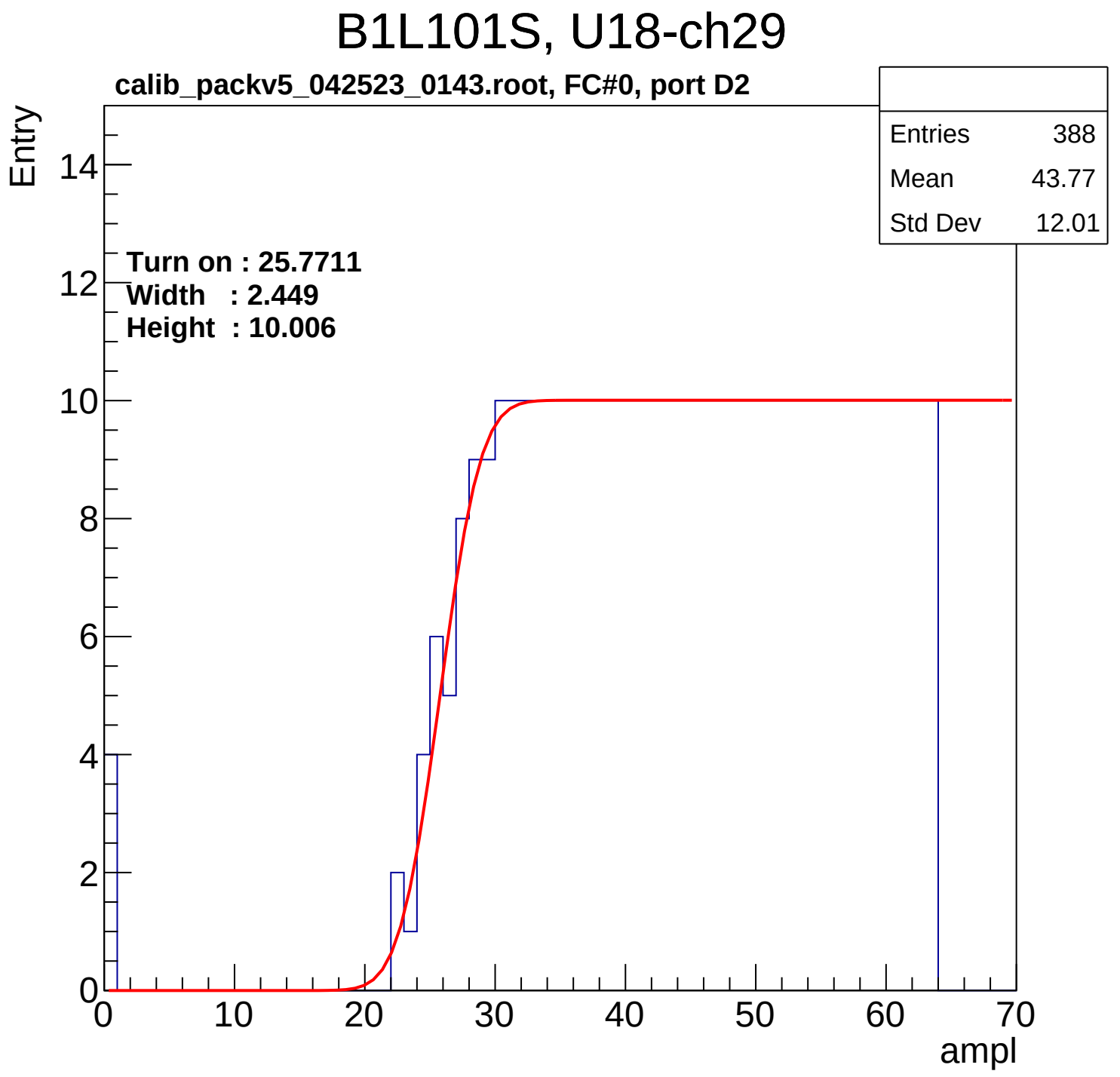
B1L101S, U18-ch29
calib_packv5_042523_0143.root, FC#0, port D2
Entries 388
Mean 43.77
Std Dev 12.01
Turn on : 25.7711
Width : 2.449
Height : 10.006
Entry
ampl
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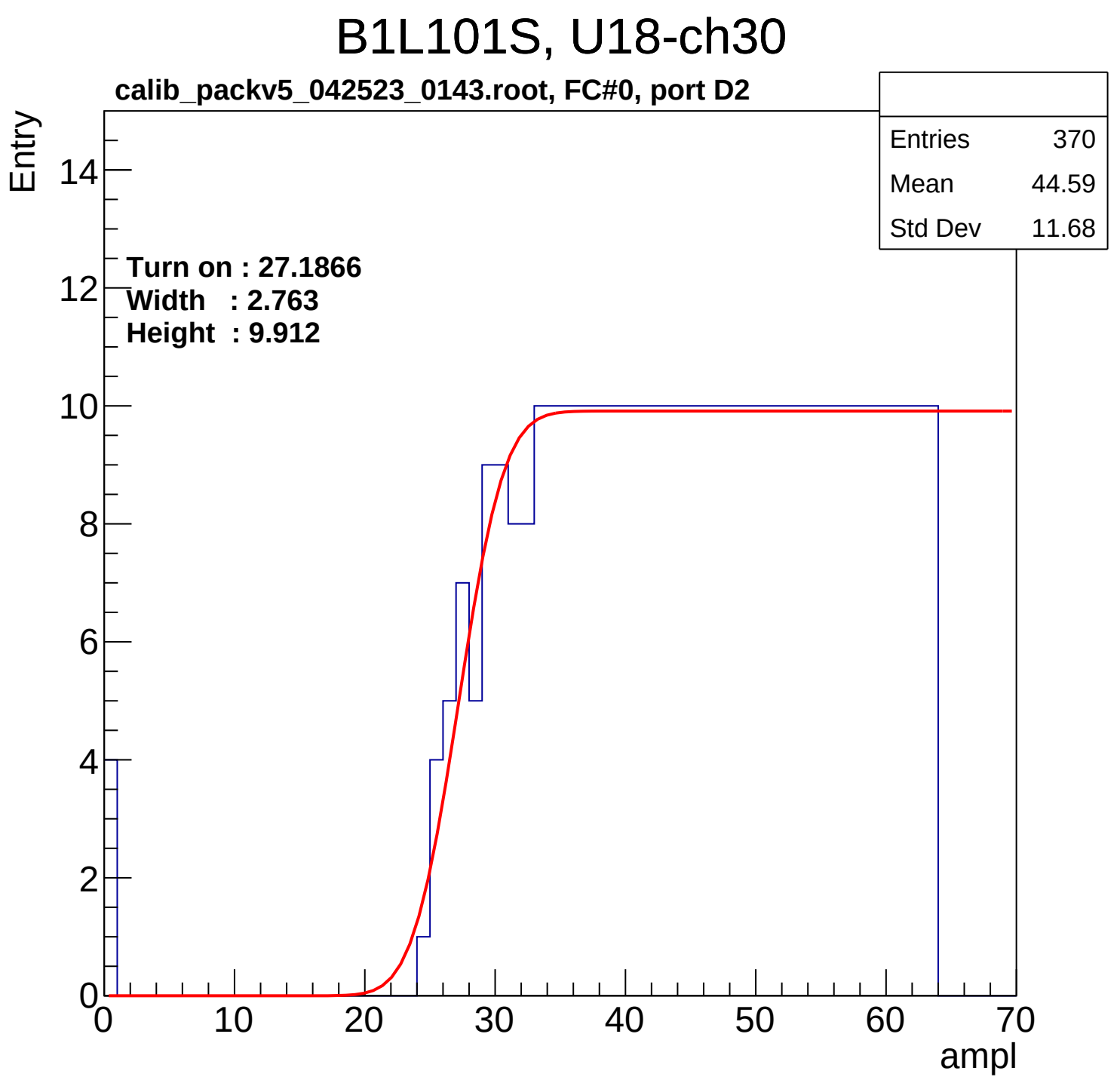
B1L101S, U18-ch30
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.59
Std Dev 11.68
Turn on : 27.1866
Width : 2.763
Height : 9.912
Entry
ampl
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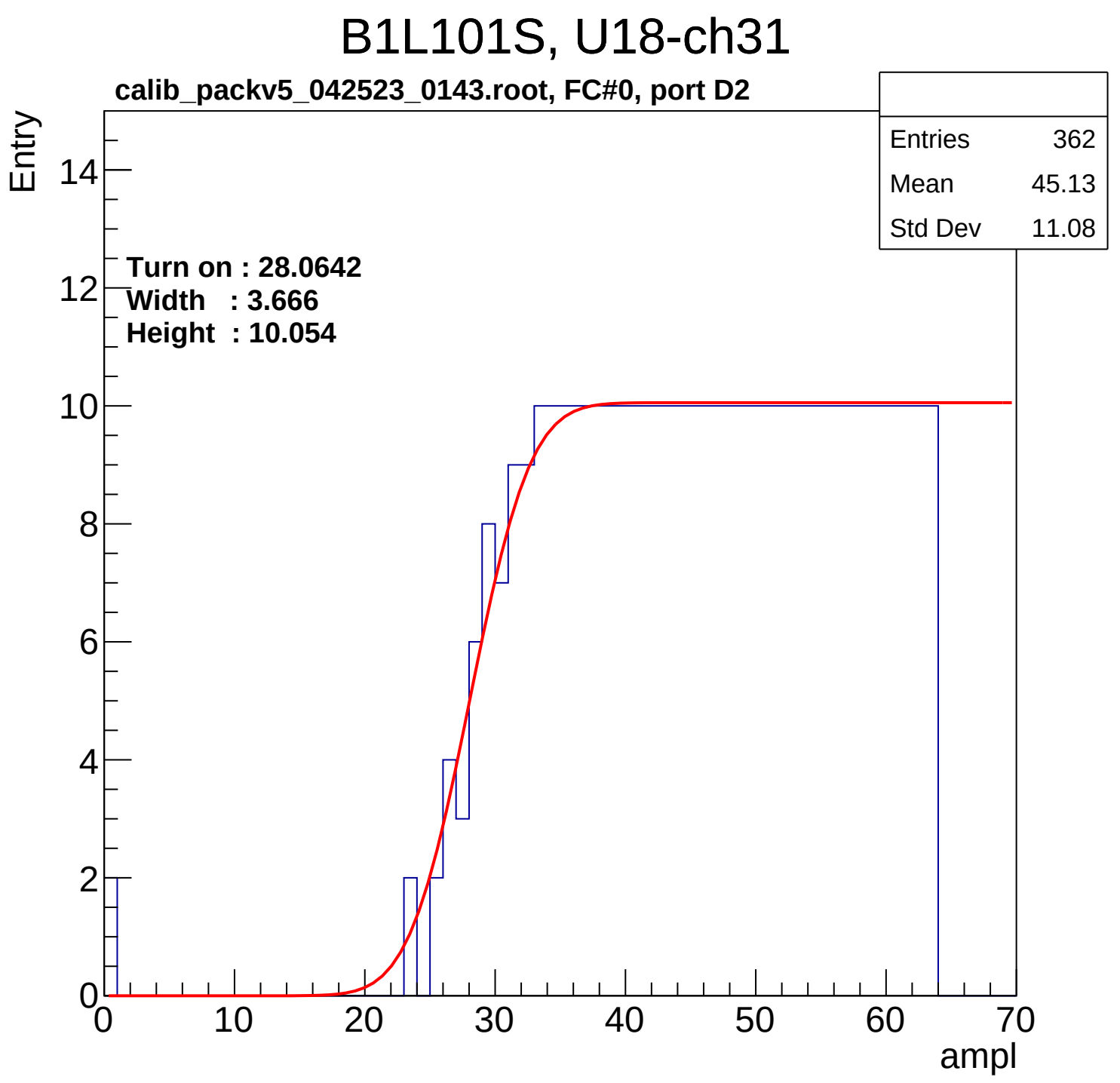
B1L101S, U18-ch31
calib_packv5_042523_0143.root, FC#0, port D2
Entries 362
Mean 45.13
Std Dev 11.08
Turn on : 28.0642
Width : 3.666
Height : 10.054
Entry
ampl
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2
4
6
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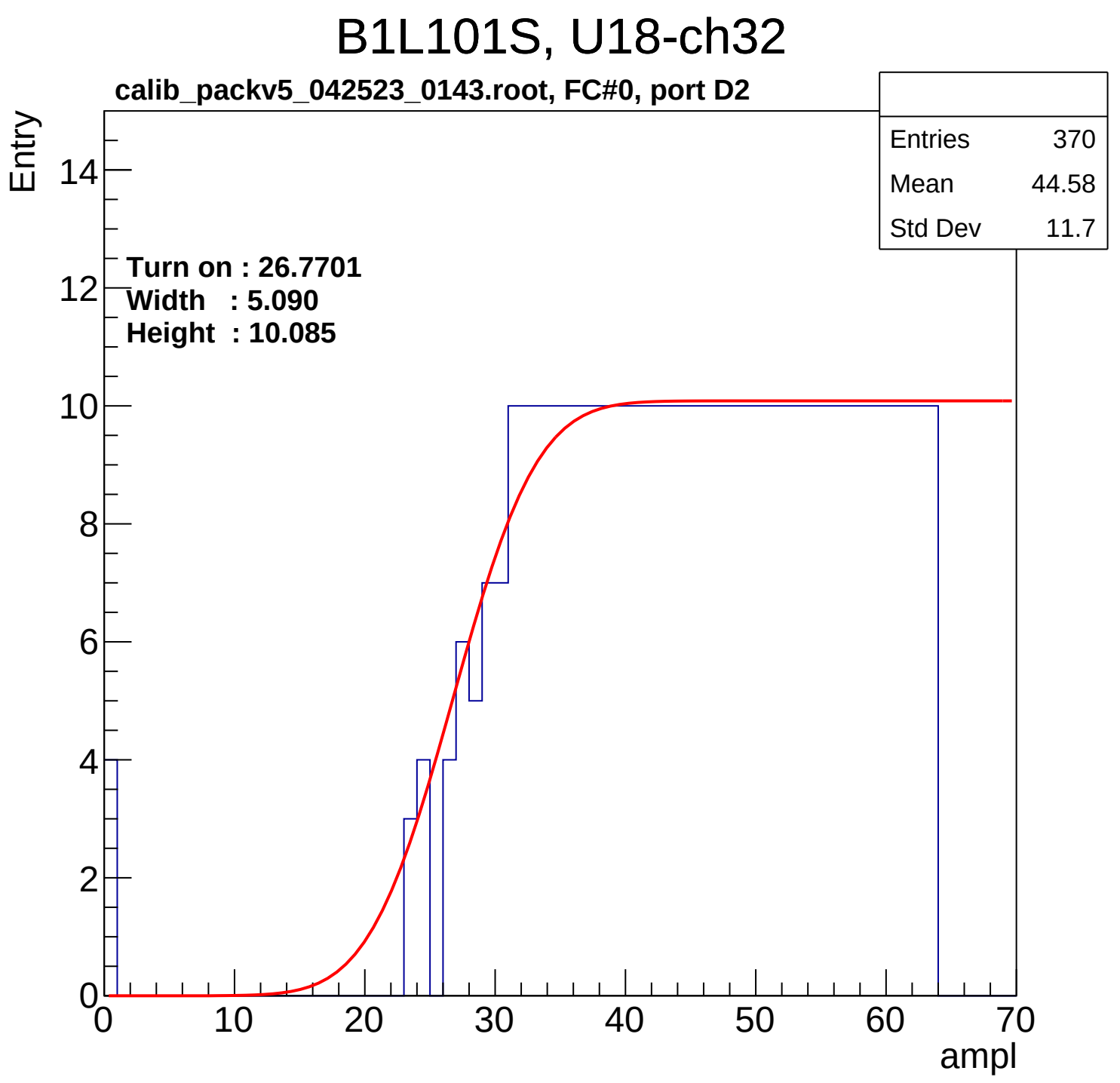
B1L101S, U18-ch32
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.58
Std Dev 11.7
Turn on : 26.7701
Width : 5.090
Height : 10.085
Entry
ampl
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2
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6
8
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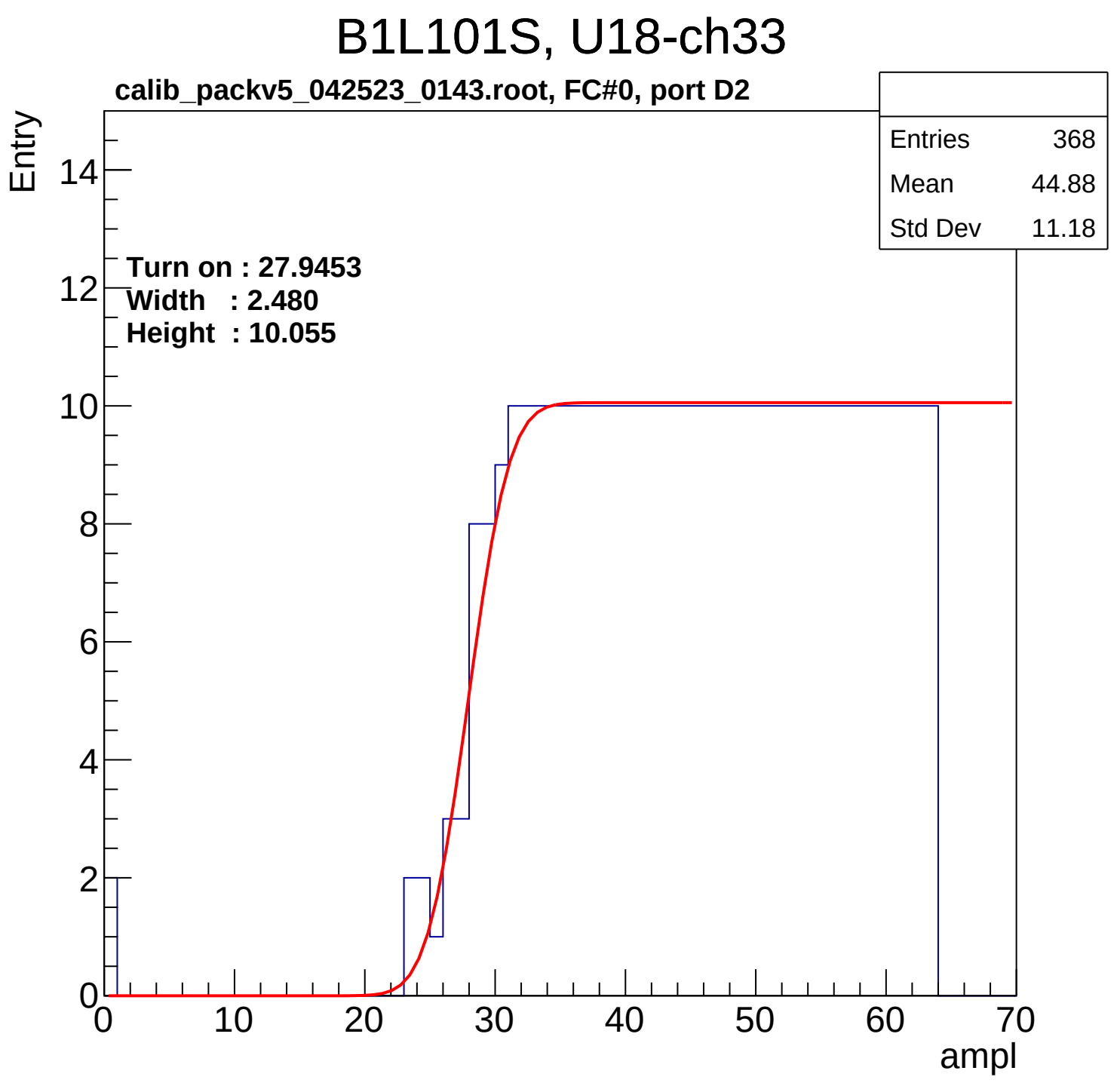
B1L101S, U18-ch33
calib_packv5_042523_0143.root, FC#0, port D2
Entries 368
Mean 44.88
Std Dev 11.18
Turn on : 27.9453
Width : 2.480
Height : 10.055
Entry
ampl
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6
8
10
12
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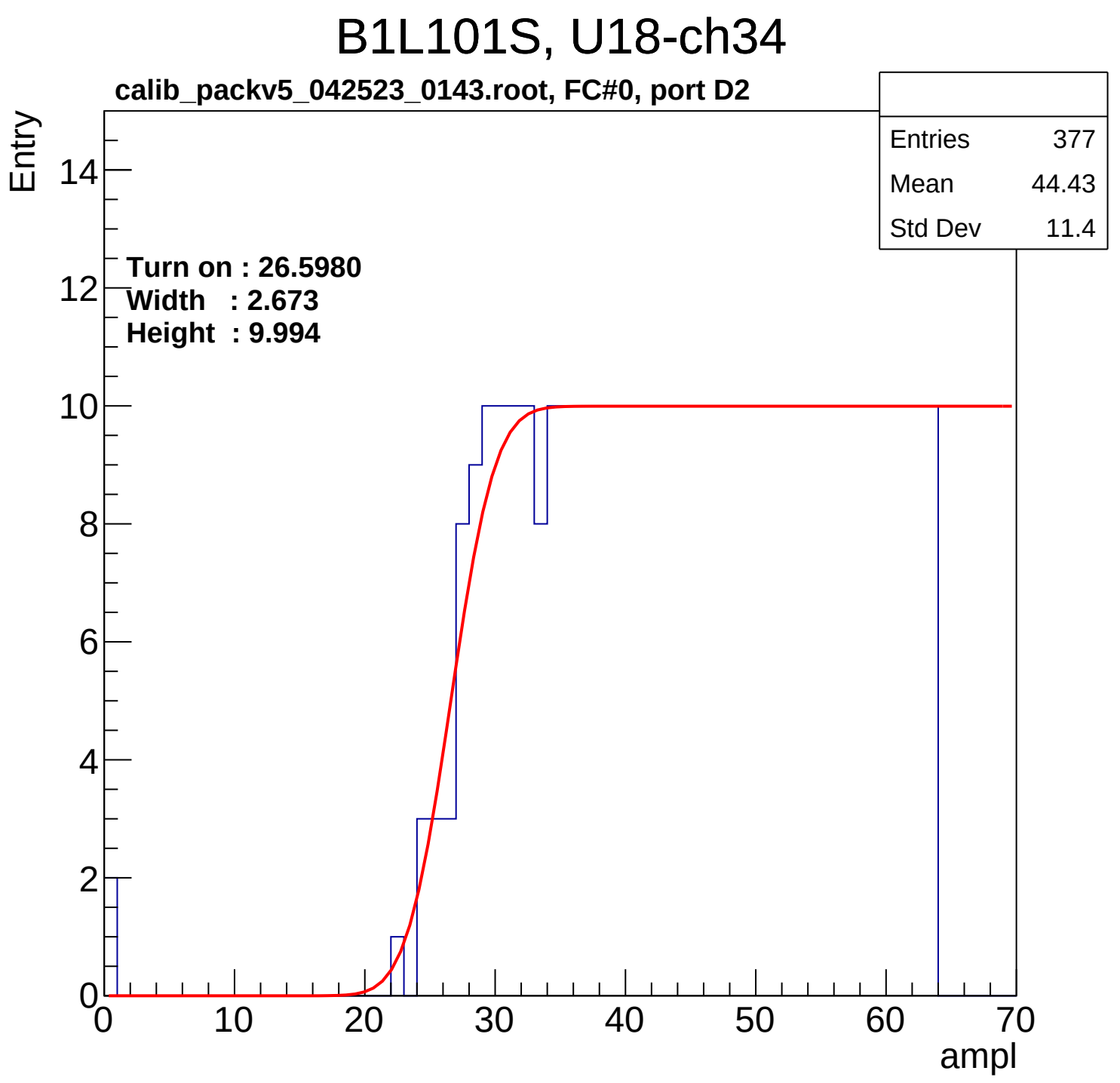
B1L101S, U18-ch34
calib_packv5_042523_0143.root, FC#0, port D2
Entries 377
Mean 44.43
Std Dev 11.4
Turn on : 26.5980
Width : 2.673
Height : 9.994
Entry
ampl
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2
4
6
8
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12
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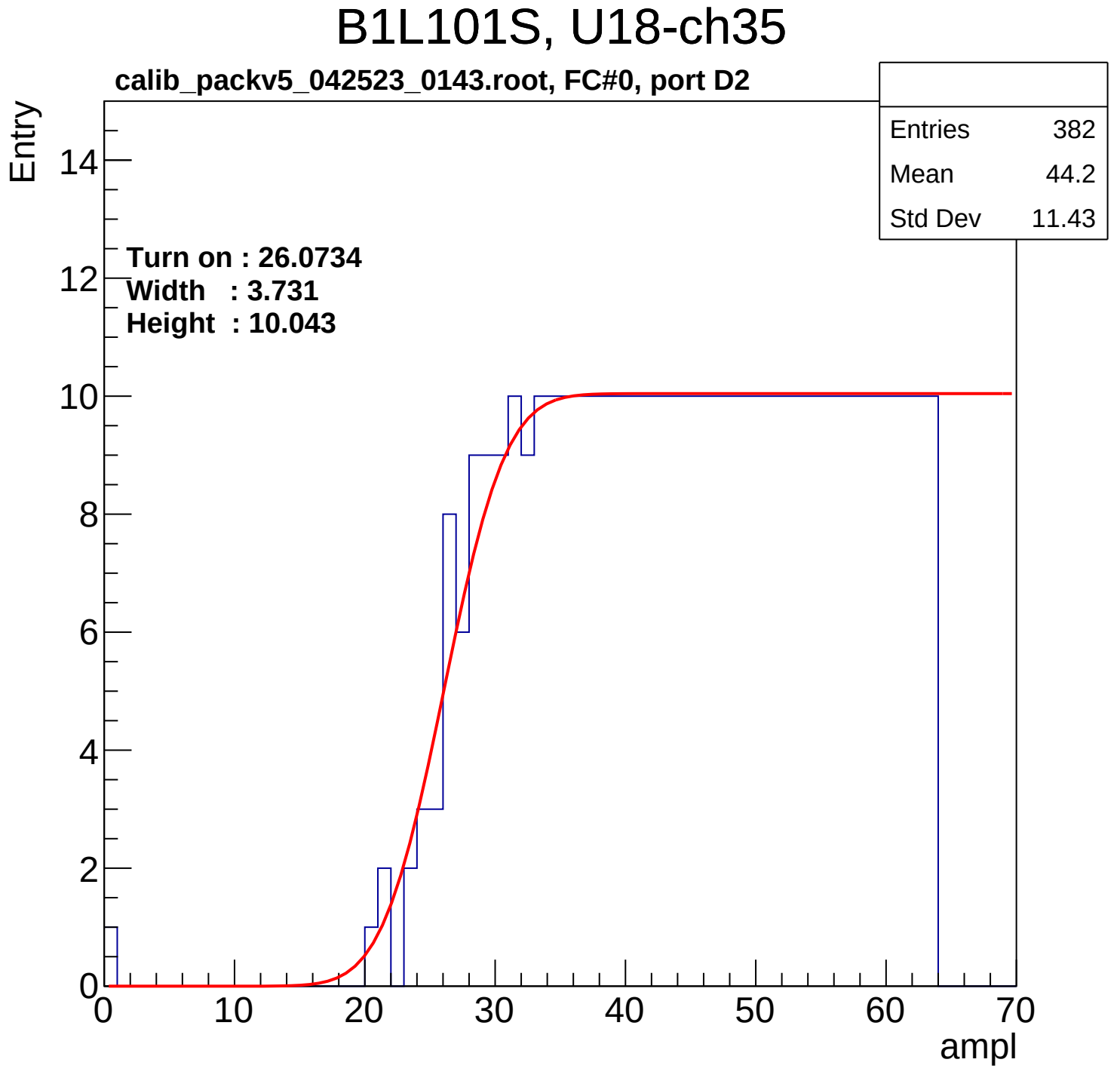
B1L101S, U18-ch35
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 44.2
Std Dev 11.43
Turn on : 26.0734
Width : 3.731
Height : 10.043
Entry
ampl
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2
4
6
8
10
12
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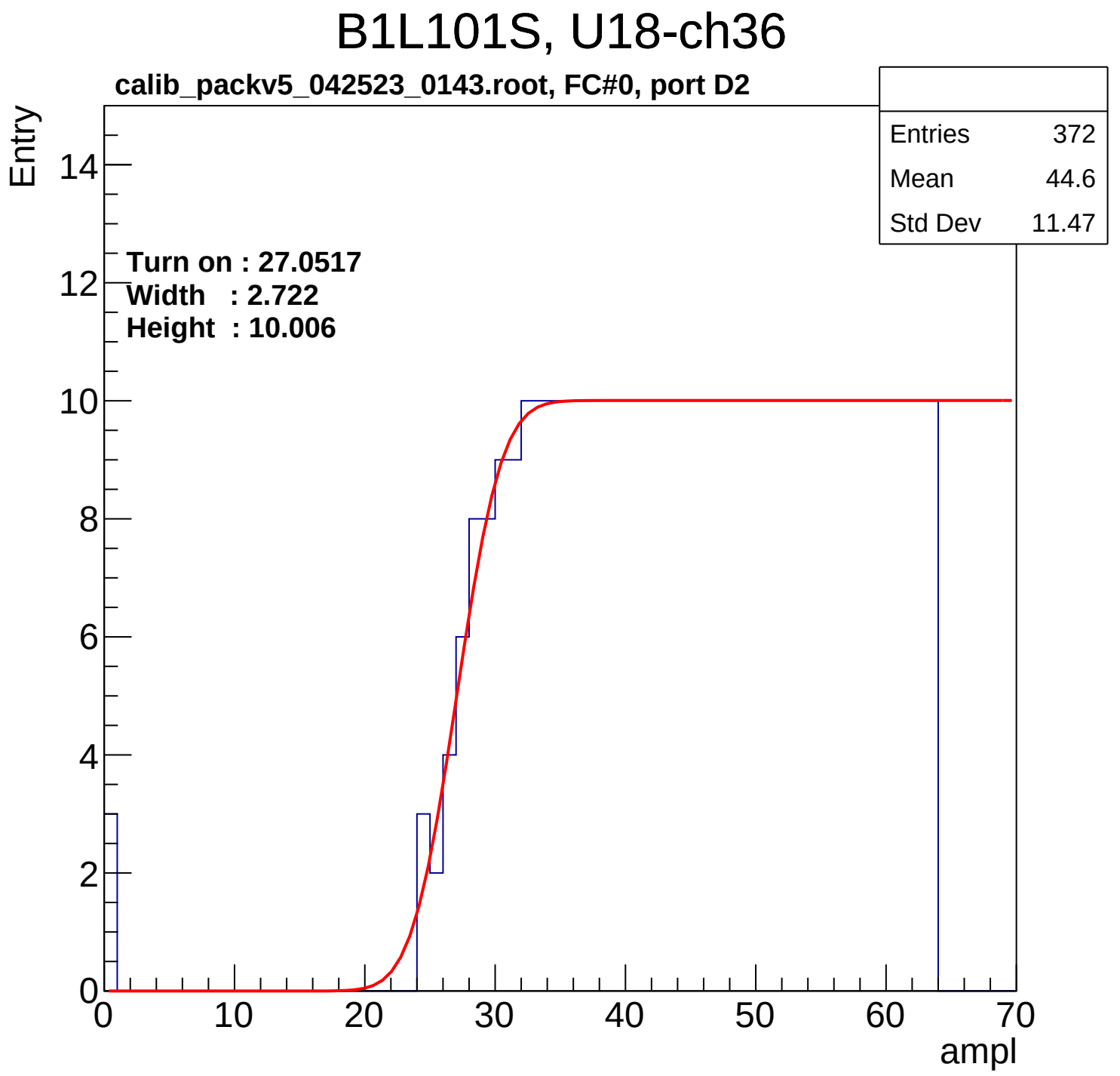
B1L101S, U18-ch36
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.6
Std Dev 11.47
Turn on : 27.0517
Width : 2.722
Height : 10.006
Entry
ampl
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6
8
10
12
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20
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60
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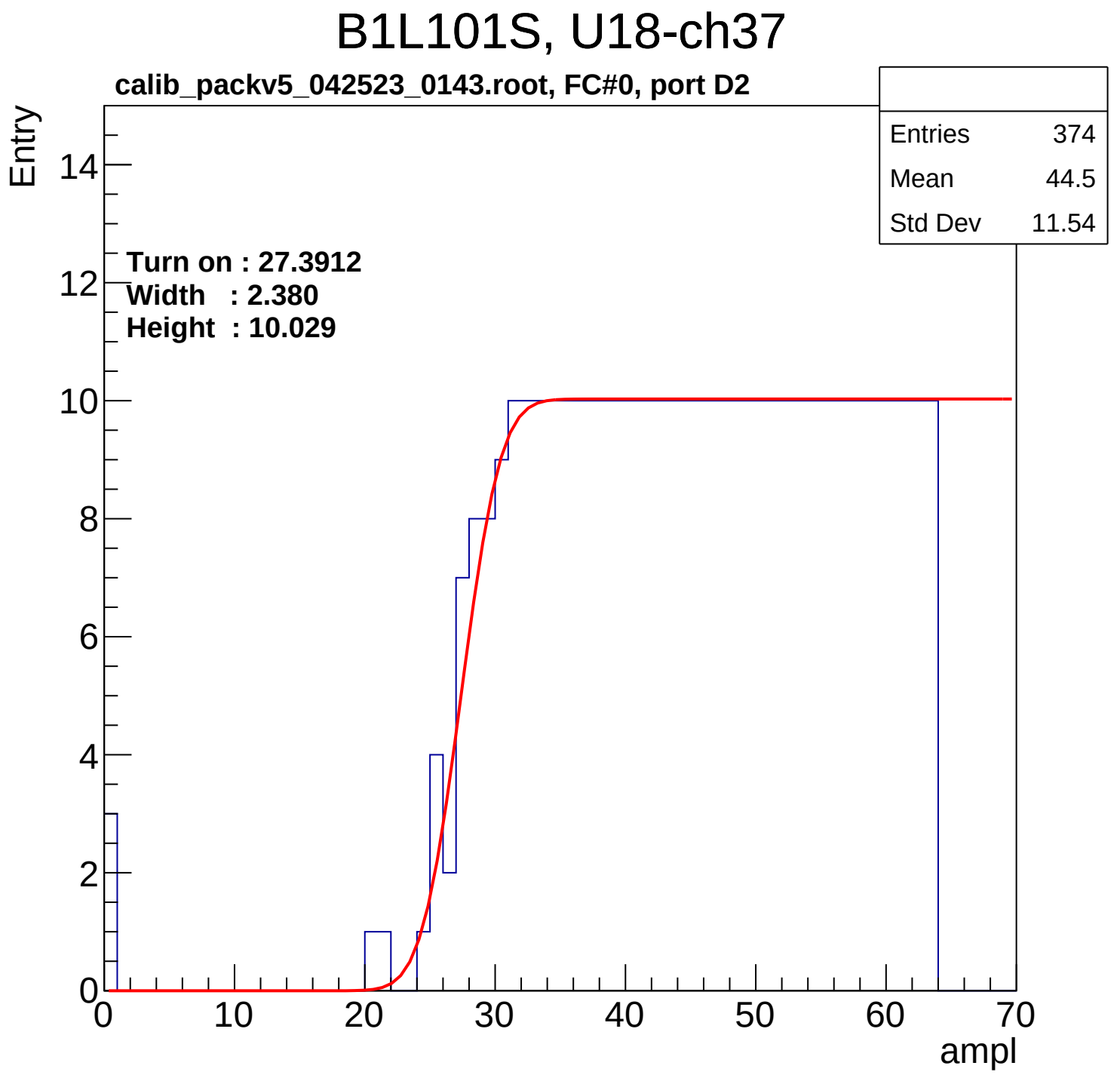
B1L101S, U18-ch37
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.5
Std Dev 11.54
Turn on : 27.3912
Width : 2.380
Height : 10.029
Entry
ampl
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4
6
8
10
12
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0
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20
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60
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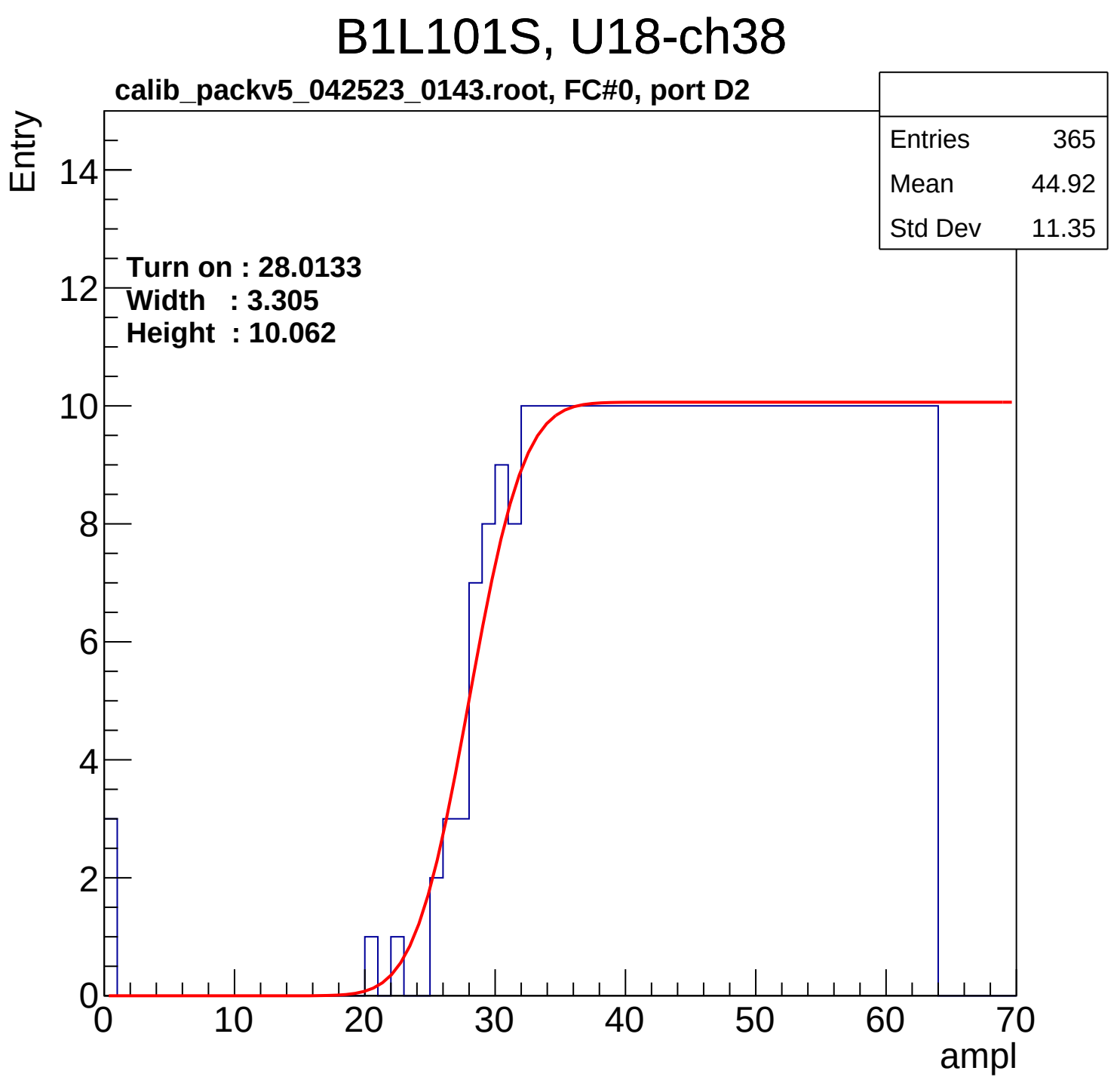
B1L101S, U18-ch38
calib_packv5_042523_0143.root, FC#0, port D2
Entries 365
Mean 44.92
Std Dev 11.35
Turn on : 28.0133
Width : 3.305
Height : 10.062
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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40
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60
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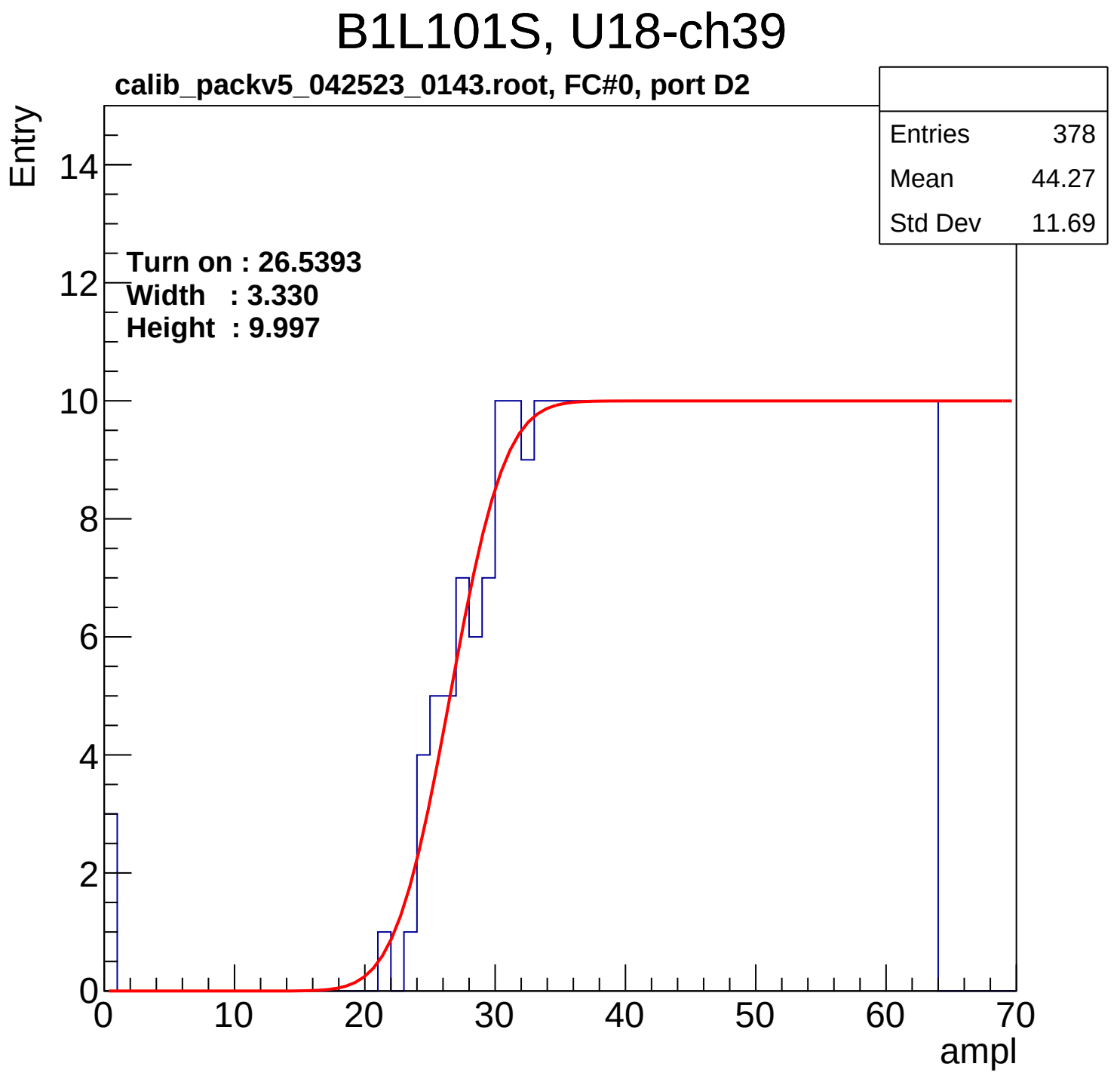
B1L101S, U18-ch39
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.27
Std Dev 11.69
Turn on : 26.5393
Width : 3.330
Height : 9.997
Entry
ampl
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4
6
8
10
12
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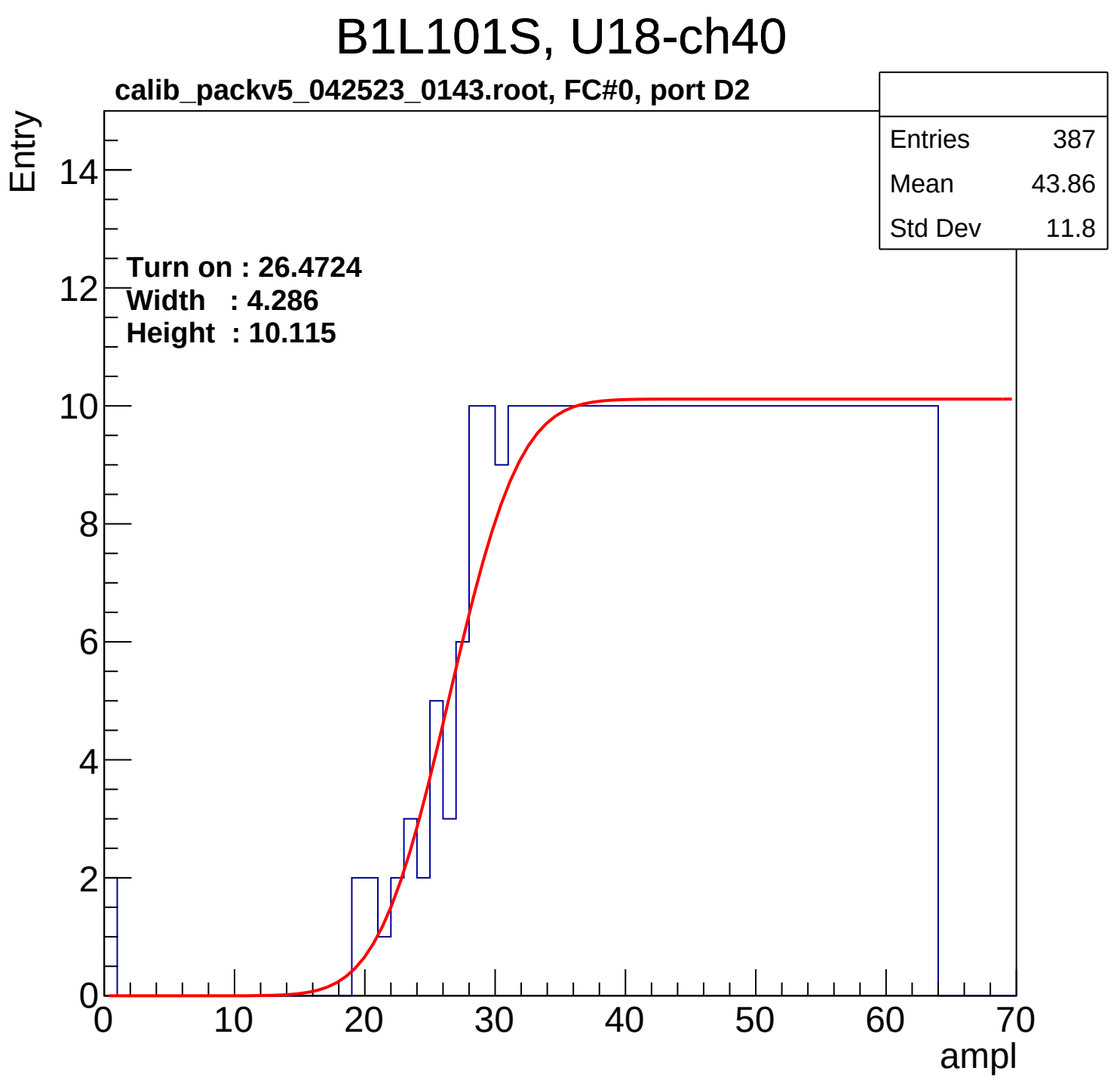
B1L101S, U18-ch40
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.86
Std Dev 11.8
Turn on : 26.4724
Width : 4.286
Height : 10.115
Entry
ampl
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8
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12
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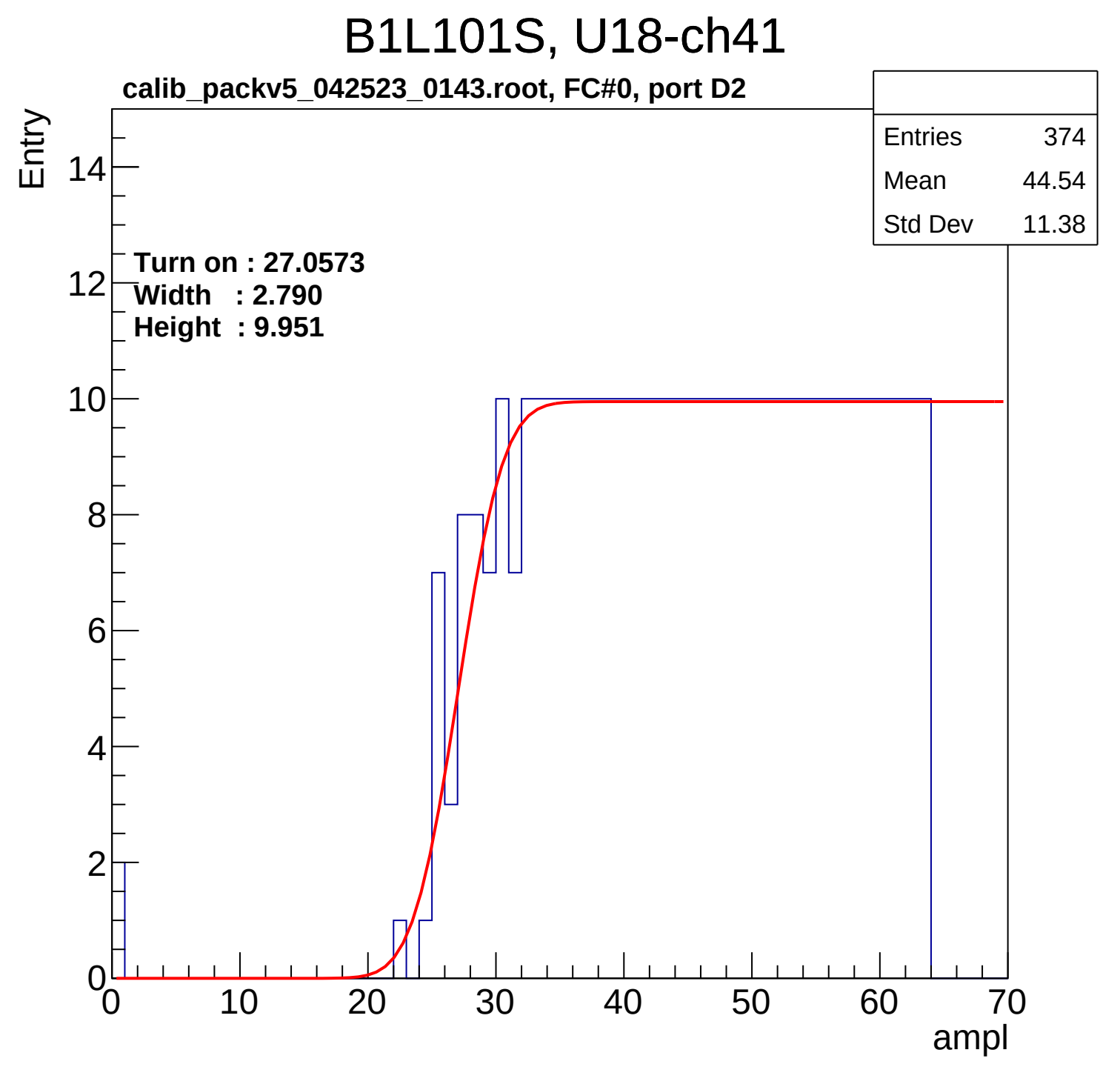
B1L101S, U18-ch41
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.54
Std Dev 11.38
Turn on : 27.0573
Width : 2.790
Height : 9.951
Entry
ampl
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4
6
8
10
12
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0
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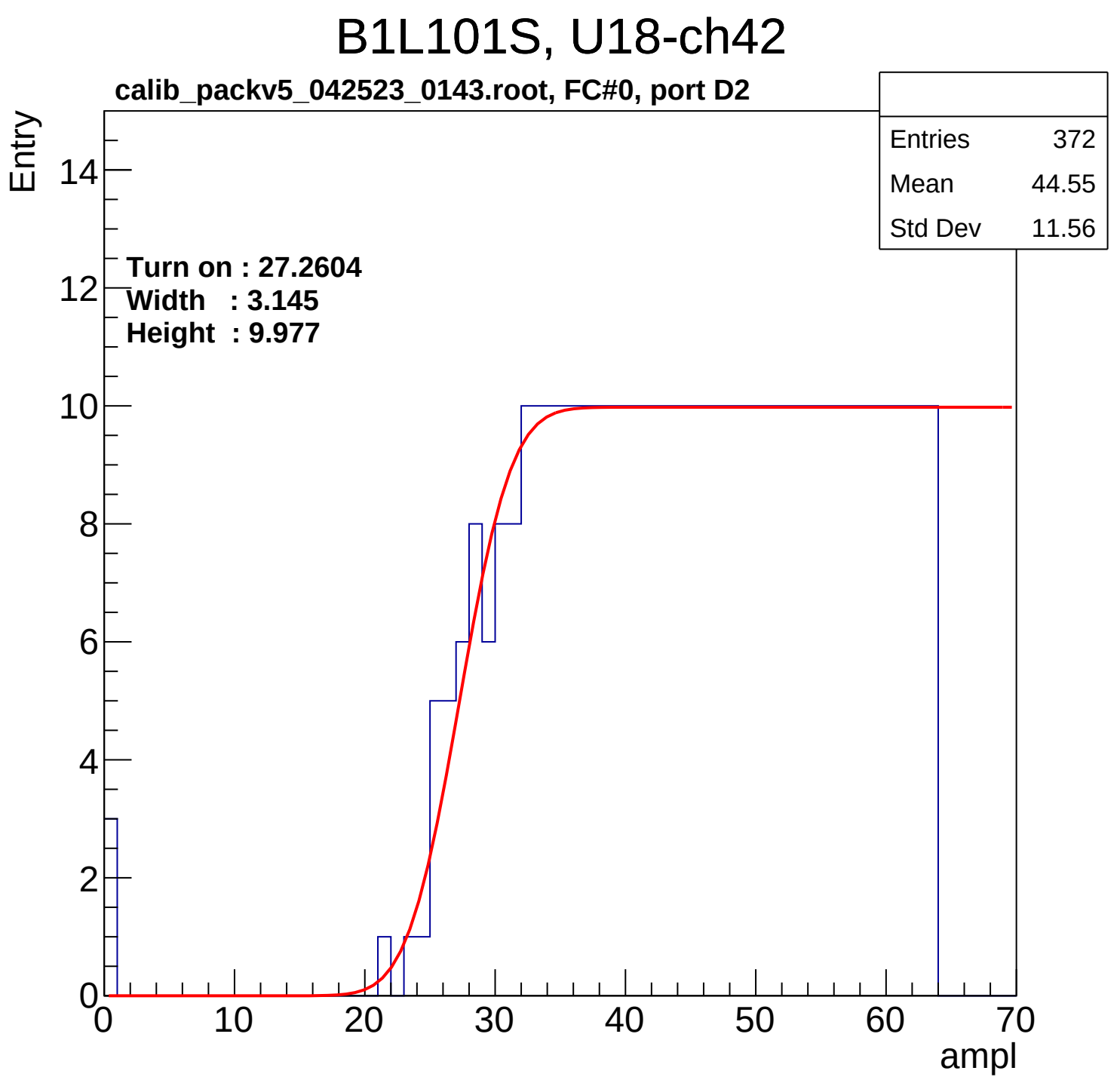
B1L101S, U18-ch42
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.55
Std Dev 11.56
Turn on : 27.2604
Width : 3.145
Height : 9.977
Entry
ampl
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2
4
6
8
10
12
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0
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20
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60
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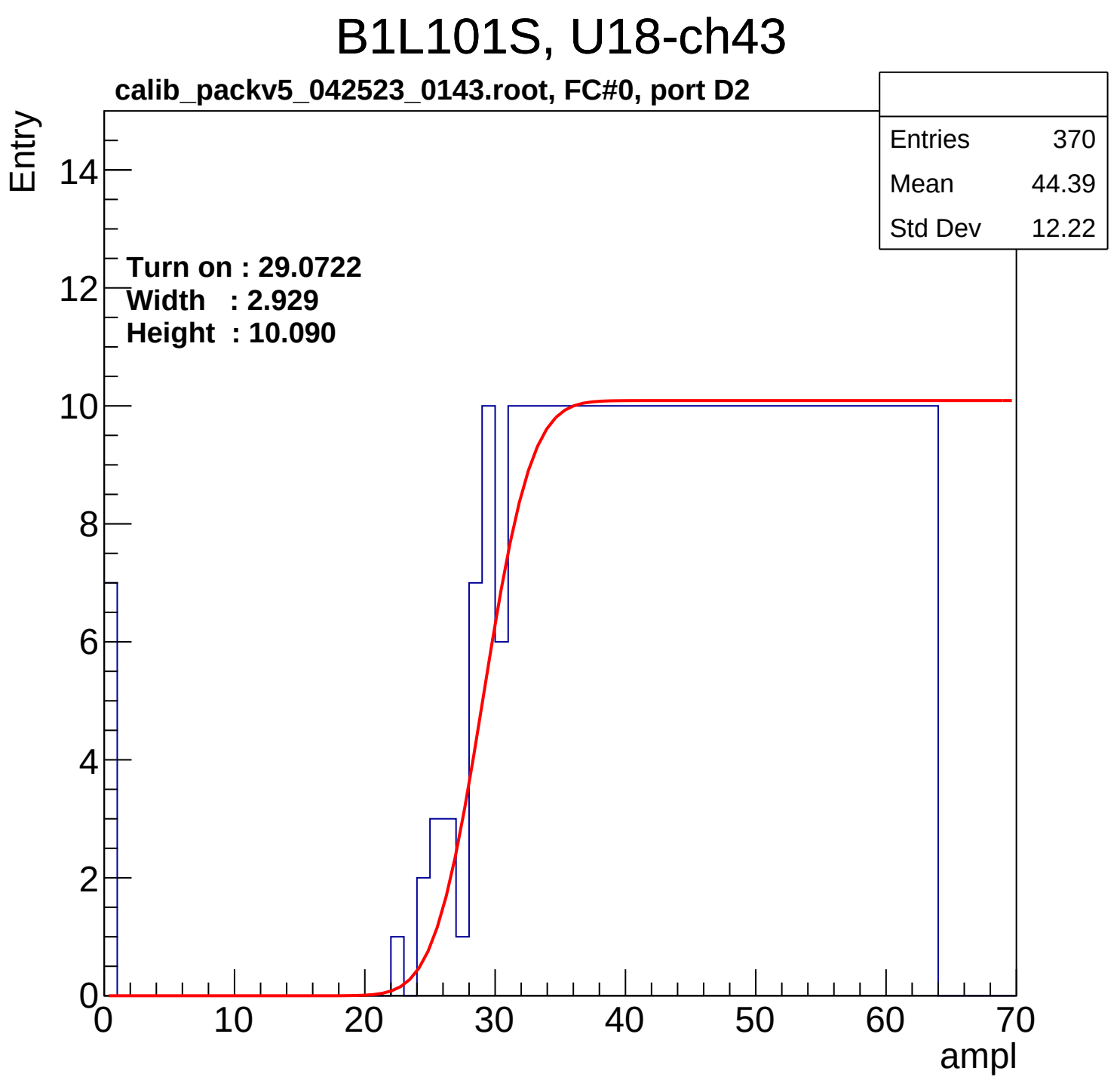
B1L101S, U18-ch43
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.39
Std Dev 12.22
Turn on : 29.0722
Width : 2.929
Height : 10.090
Entry
ampl
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8
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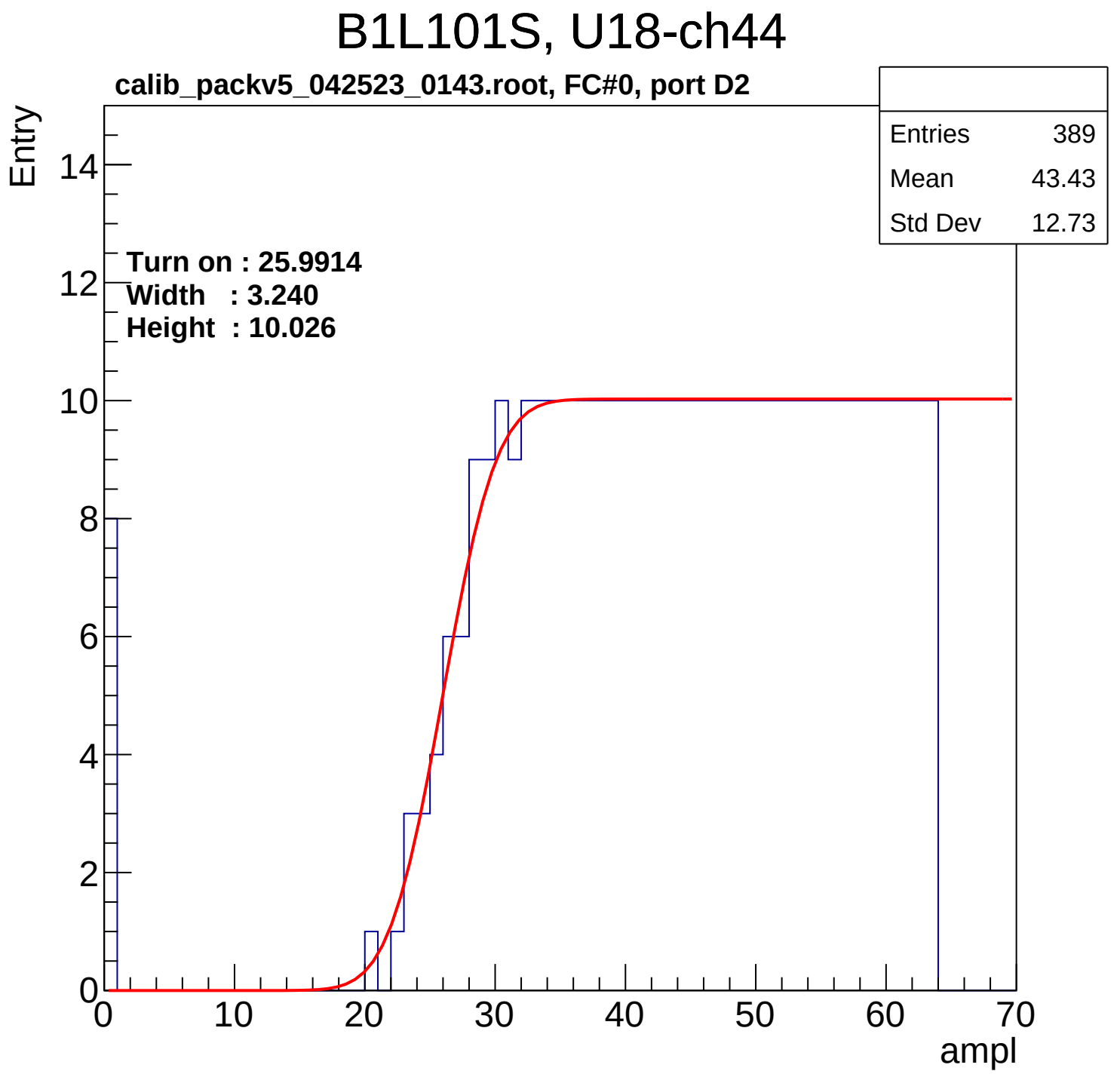
B1L101S, U18-ch44
calib_packv5_042523_0143.root, FC#0, port D2
Entries 389
Mean 43.43
Std Dev 12.73
Turn on : 25.9914
Width : 3.240
Height : 10.026
Entry
ampl
0
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6
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10
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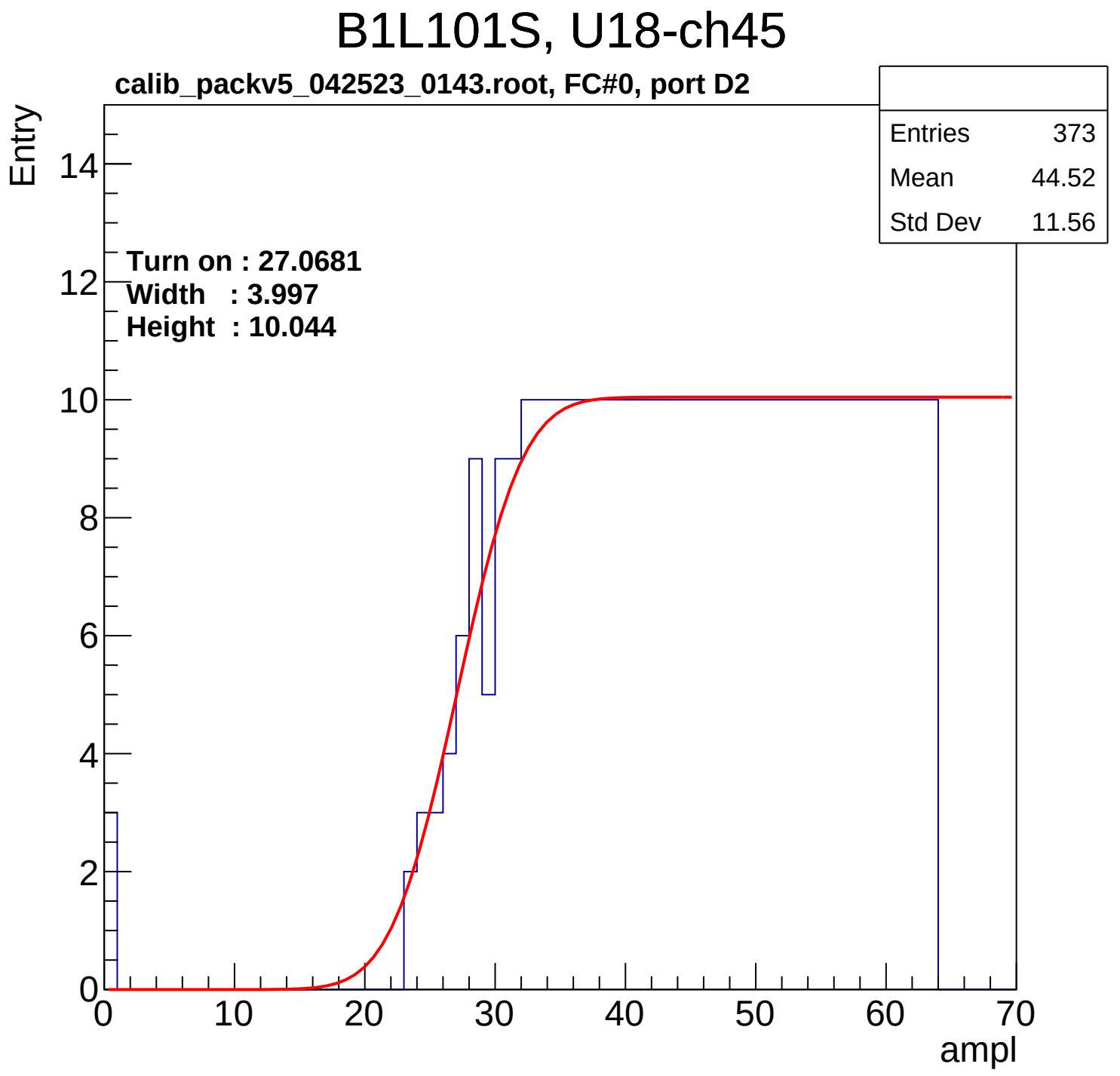
B1L101S, U18-ch45
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.52
Std Dev 11.56
Turn on : 27.0681
Width : 3.997
Height : 10.044
Entry
ampl
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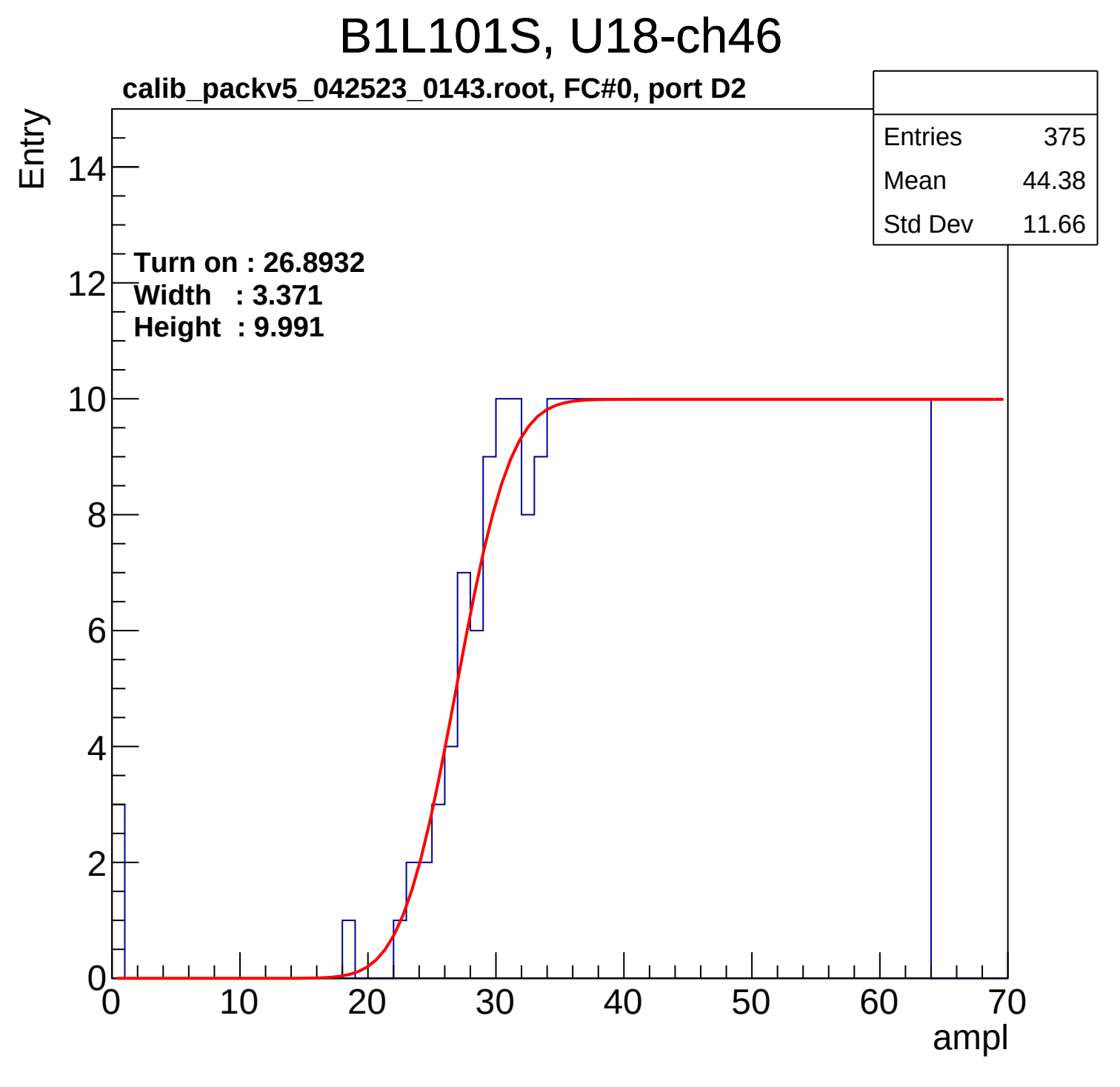
B1L101S, U18-ch46
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.38
Std Dev 11.66
Turn on : 26.8932
Width : 3.371
Height : 9.991
Entry
ampl
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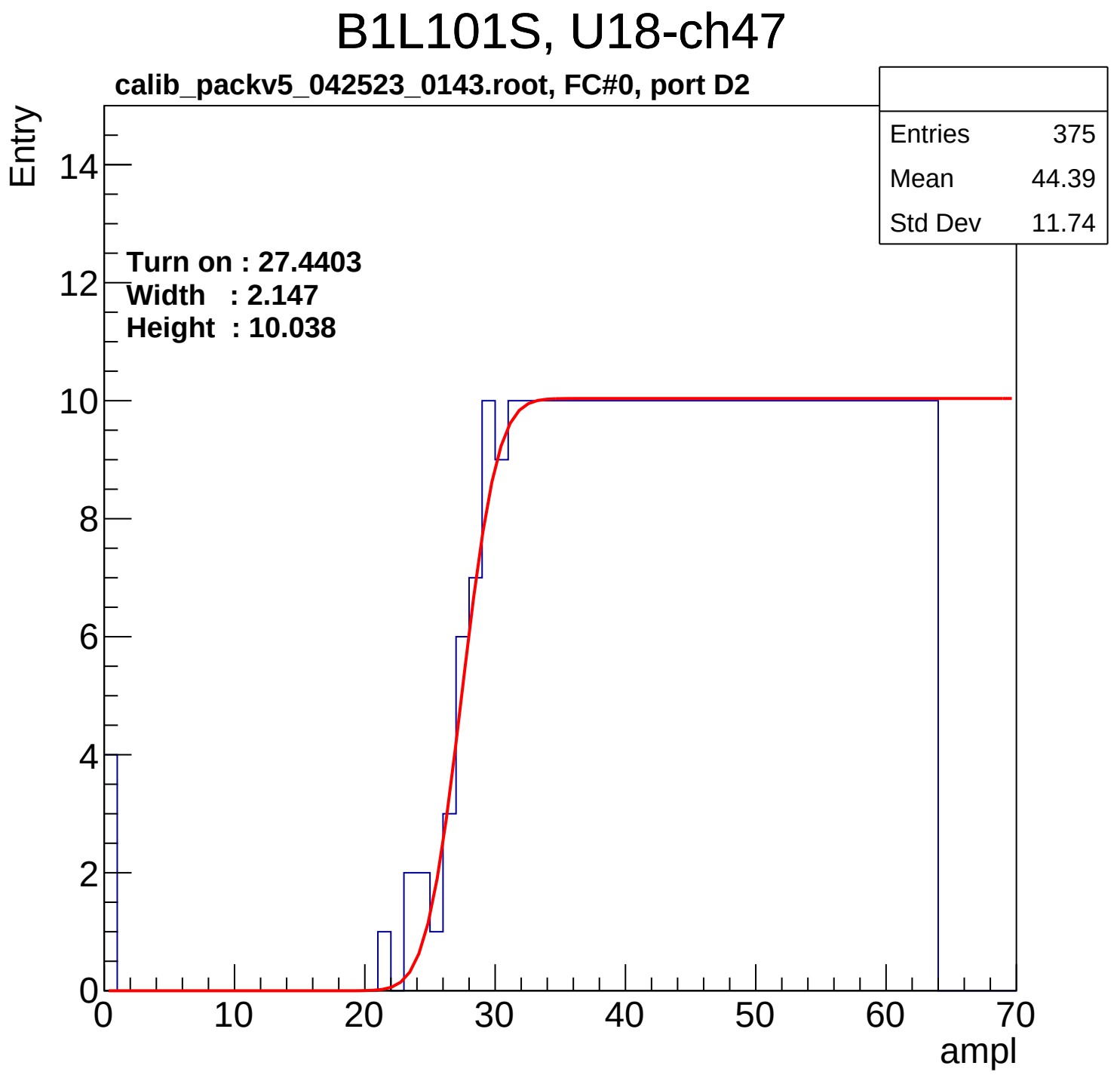
B1L101S, U18-ch47
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.39
Std Dev 11.74
Turn on : 27.4403
Width : 2.147
Height : 10.038
Entry
ampl
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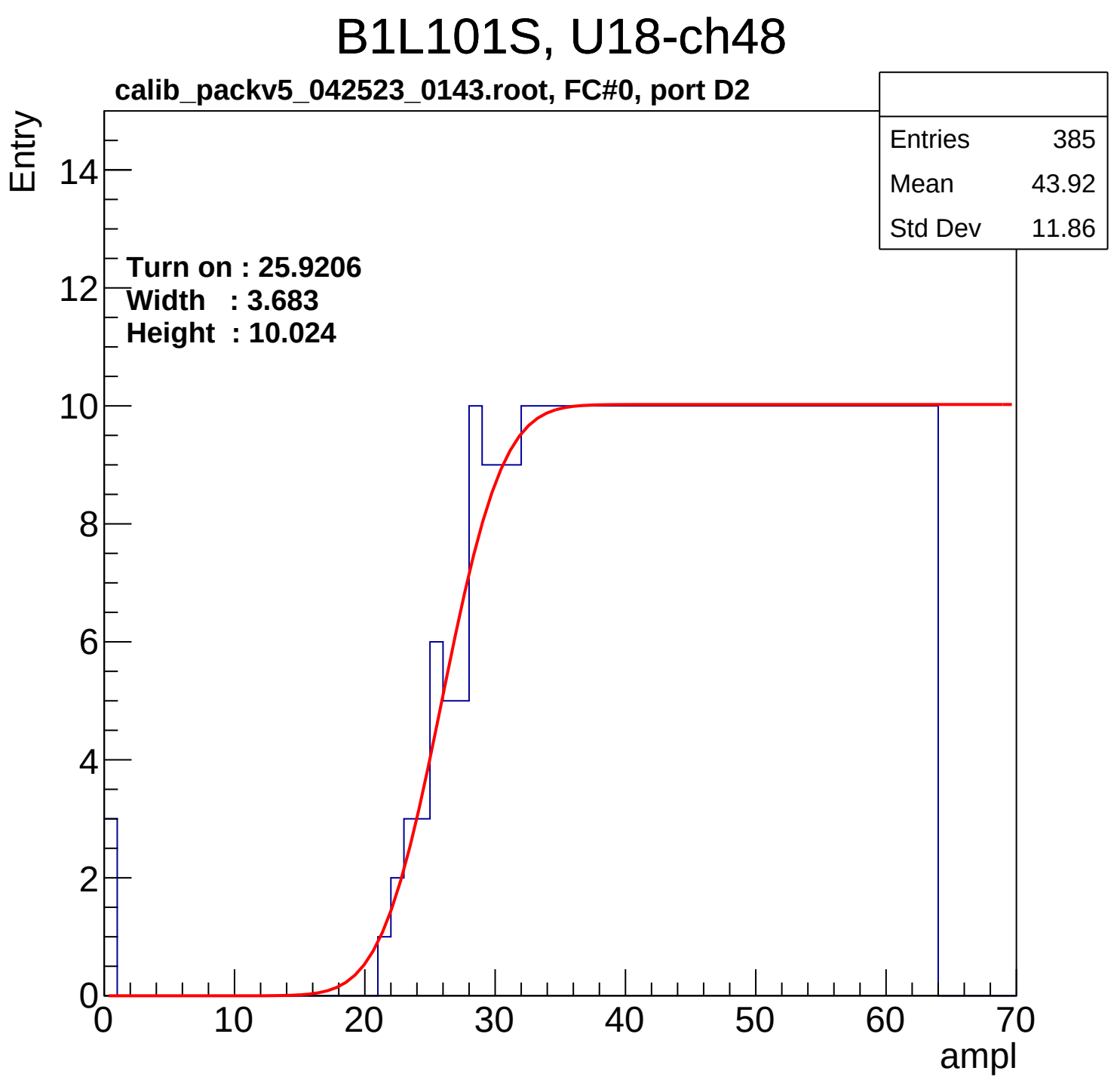
B1L101S, U18-ch48
calib_packv5_042523_0143.root, FC#0, port D2
Entries 385
Mean 43.92
Std Dev 11.86
Turn on : 25.9206
Width : 3.683
Height : 10.024
Entry
ampl
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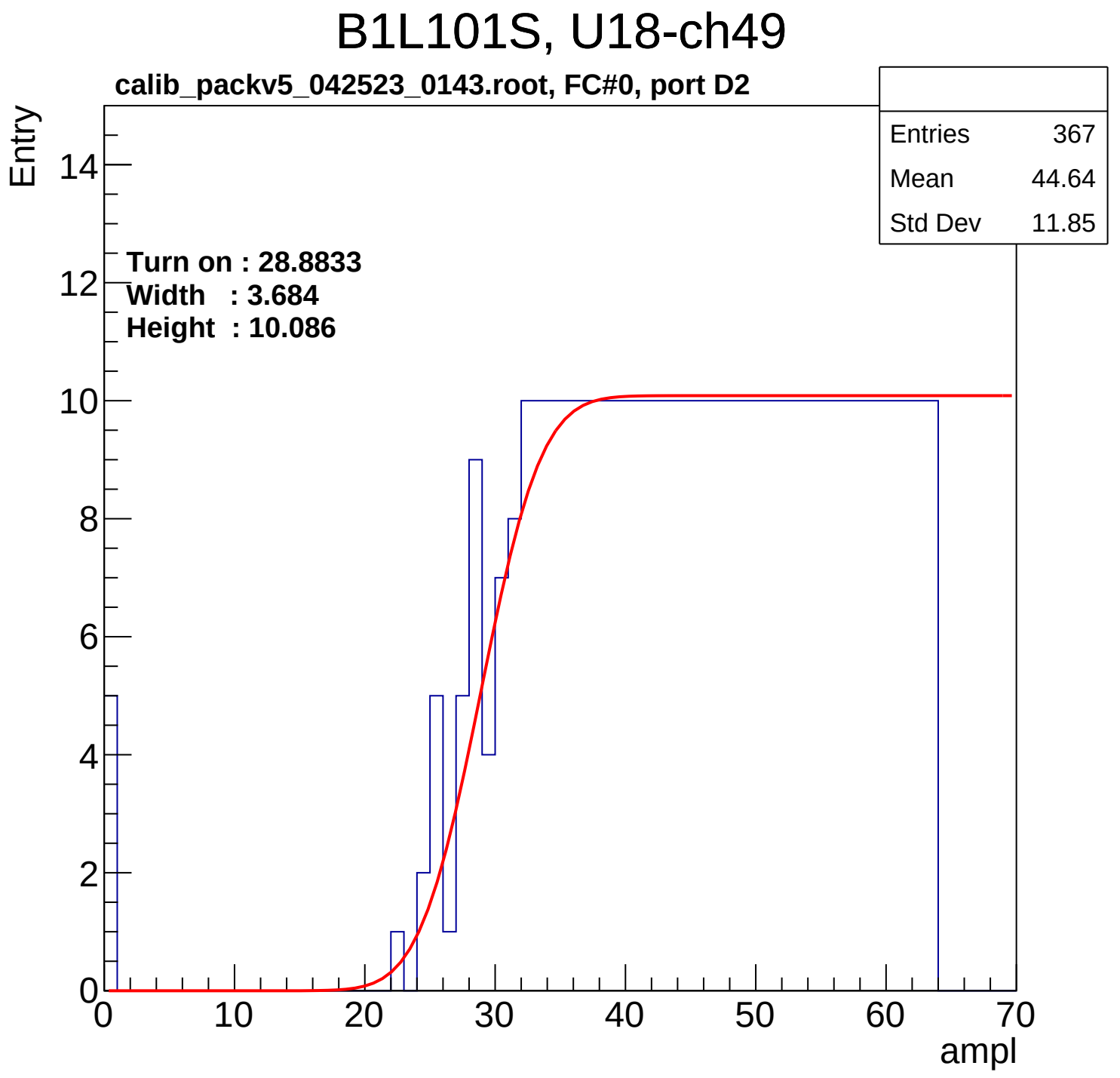
B1L101S, U18-ch49
calib_packv5_042523_0143.root, FC#0, port D2
Entries 367
Mean 44.64
Std Dev 11.85
Turn on : 28.8833
Width : 3.684
Height : 10.086
Entry
ampl
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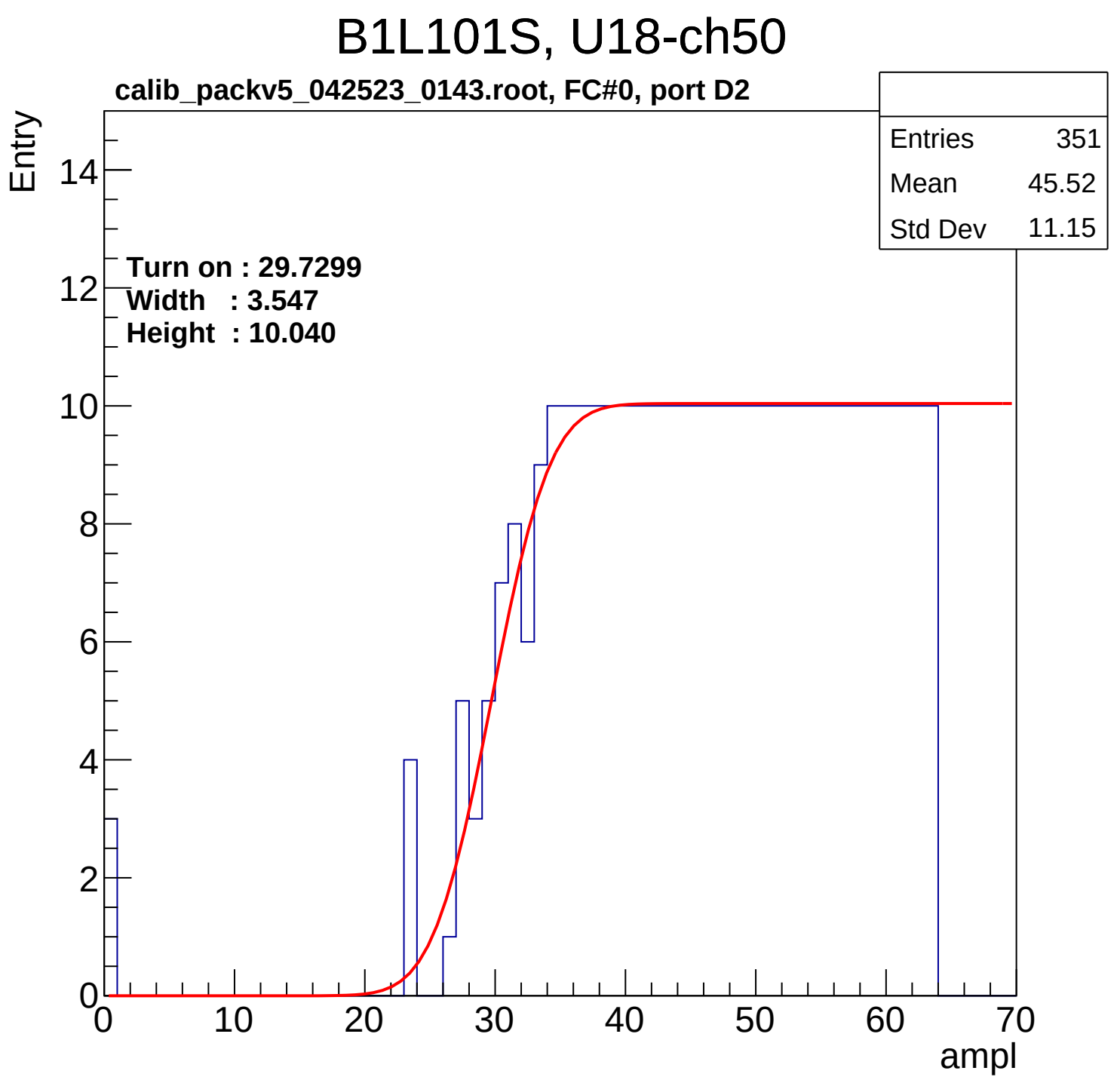
B1L101S, U18-ch50
calib_packv5_042523_0143.root, FC#0, port D2
Entries 351
Mean 45.52
Std Dev 11.15
Turn on : 29.7299
Width : 3.547
Height : 10.040
Entry
ampl
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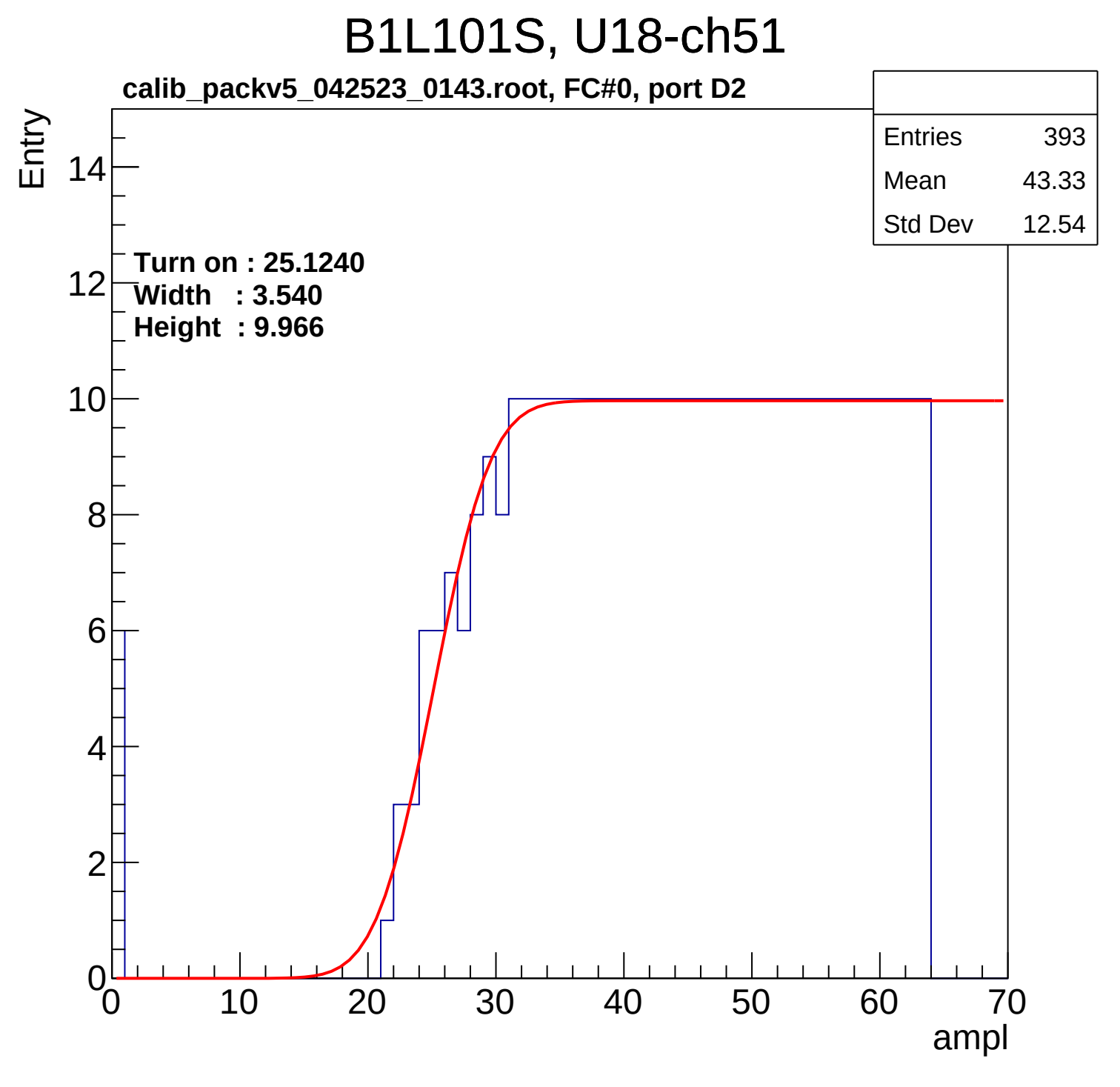
B1L101S, U18-ch51
calib_packv5_042523_0143.root, FC#0, port D2
Entries 393
Mean 43.33
Std Dev 12.54
Turn on : 25.1240
Width : 3.540
Height : 9.966
Entry
ampl
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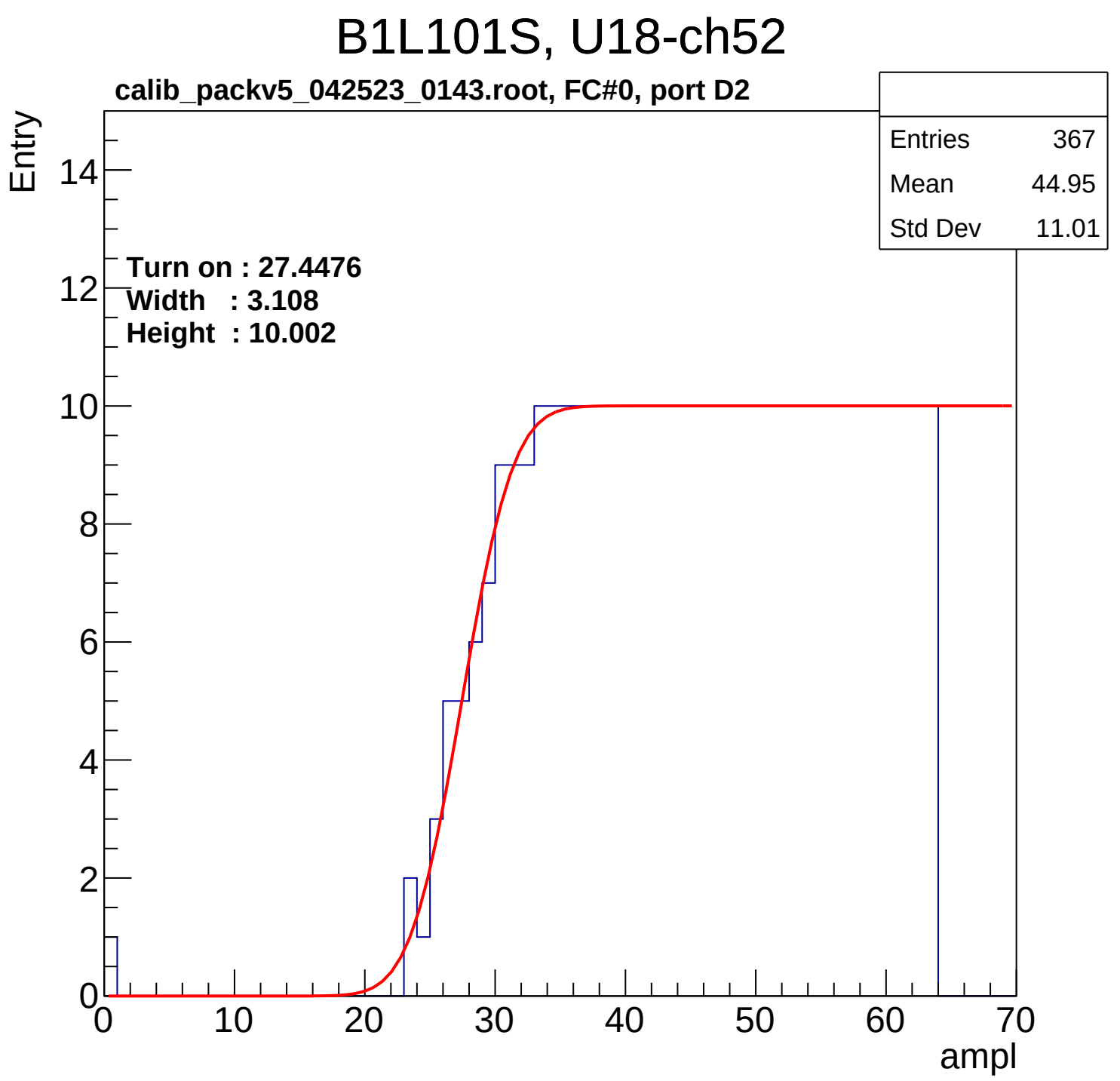
B1L101S, U18-ch52
calib_packv5_042523_0143.root, FC#0, port D2
Entries 367
Mean 44.95
Std Dev 11.01
Turn on : 27.4476
Width : 3.108
Height : 10.002
Entry
ampl
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6
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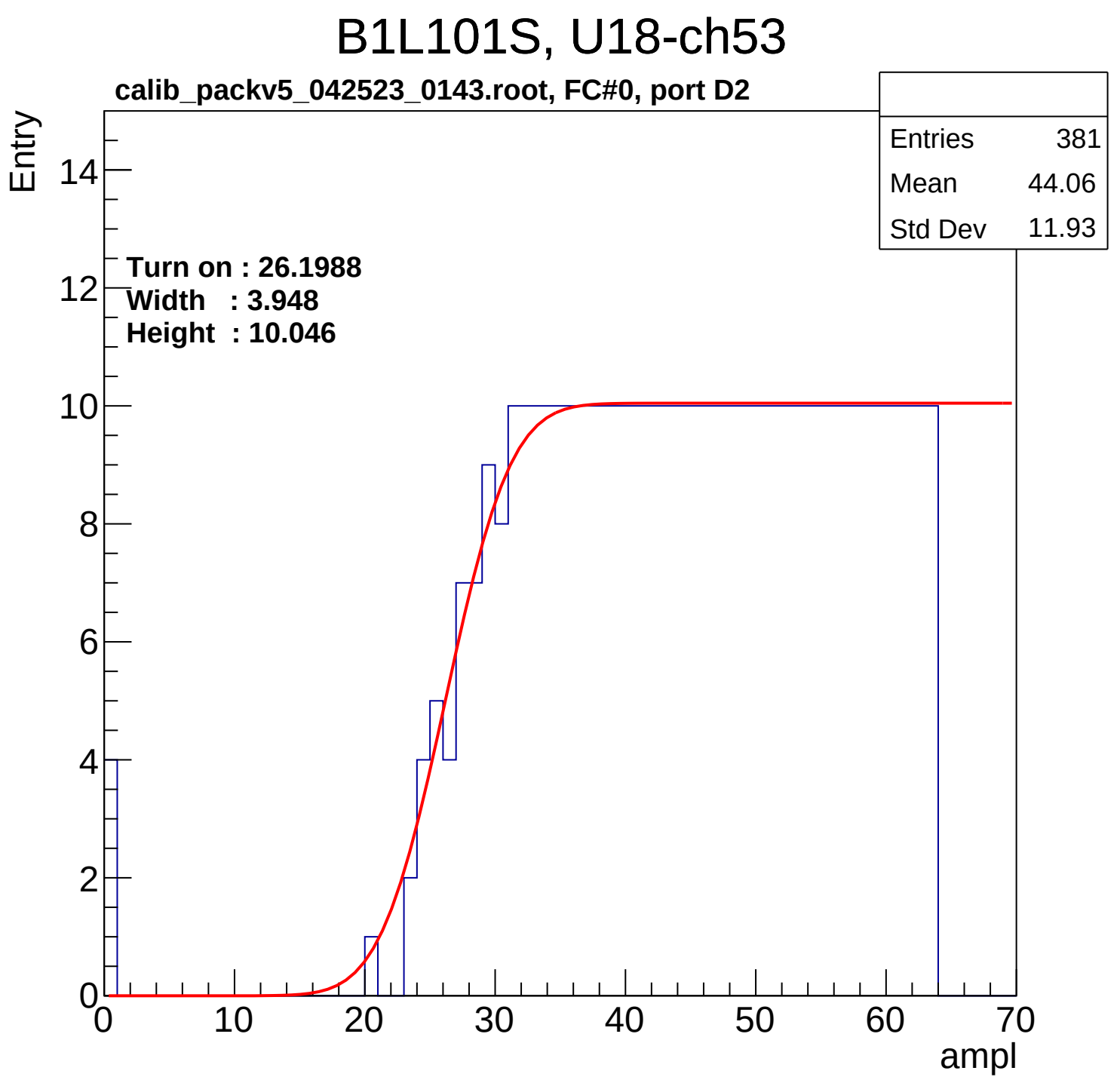
B1L101S, U18-ch53
calib_packv5_042523_0143.root, FC#0, port D2
Entries 381
Mean 44.06
Std Dev 11.93
Turn on : 26.1988
Width : 3.948
Height : 10.046
Entry
ampl
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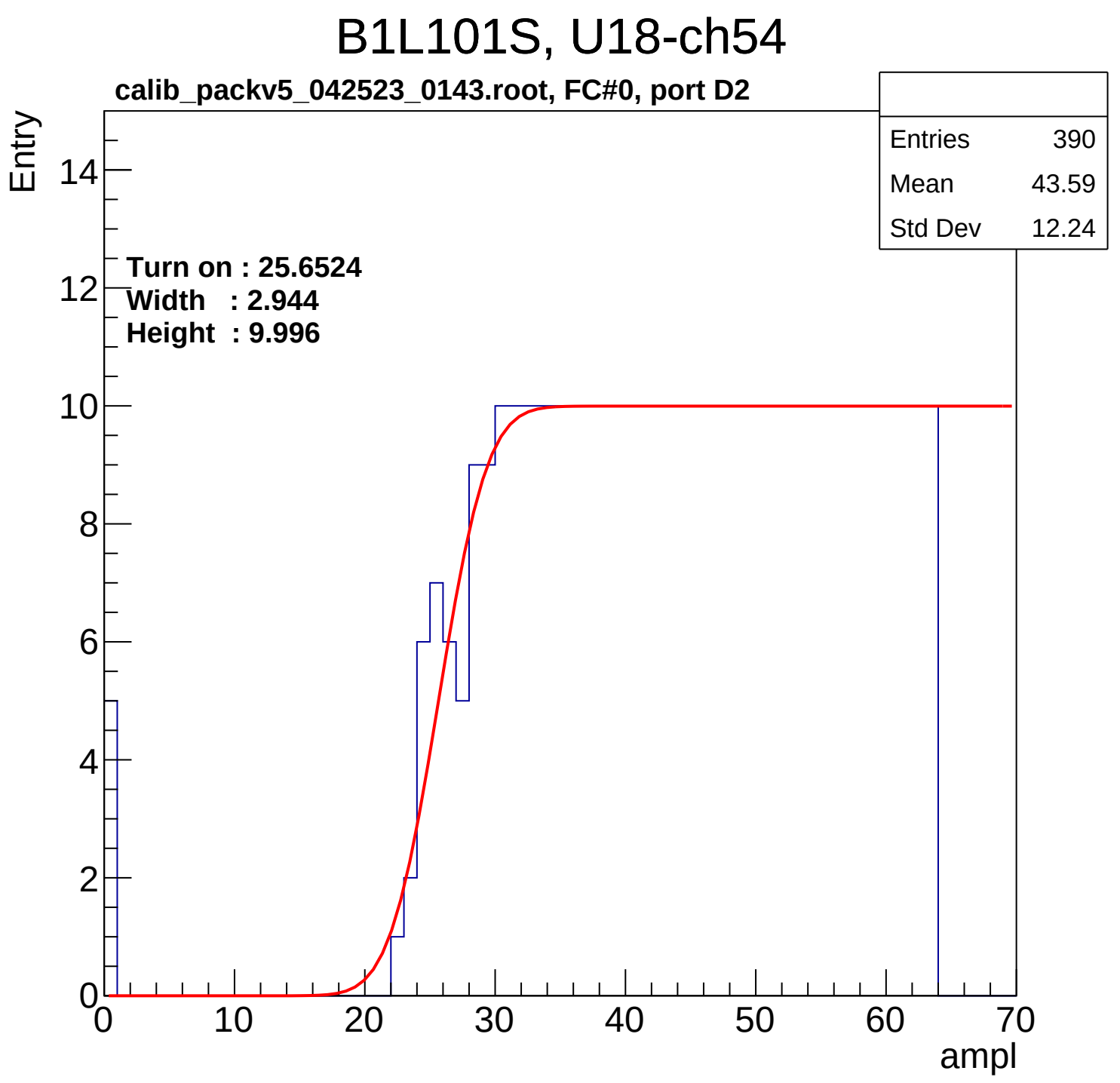
B1L101S, U18-ch54
calib_packv5_042523_0143.root, FC#0, port D2
Entries 390
Mean 43.59
Std Dev 12.24
Turn on : 25.6524
Width : 2.944
Height : 9.996
Entry
ampl
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6
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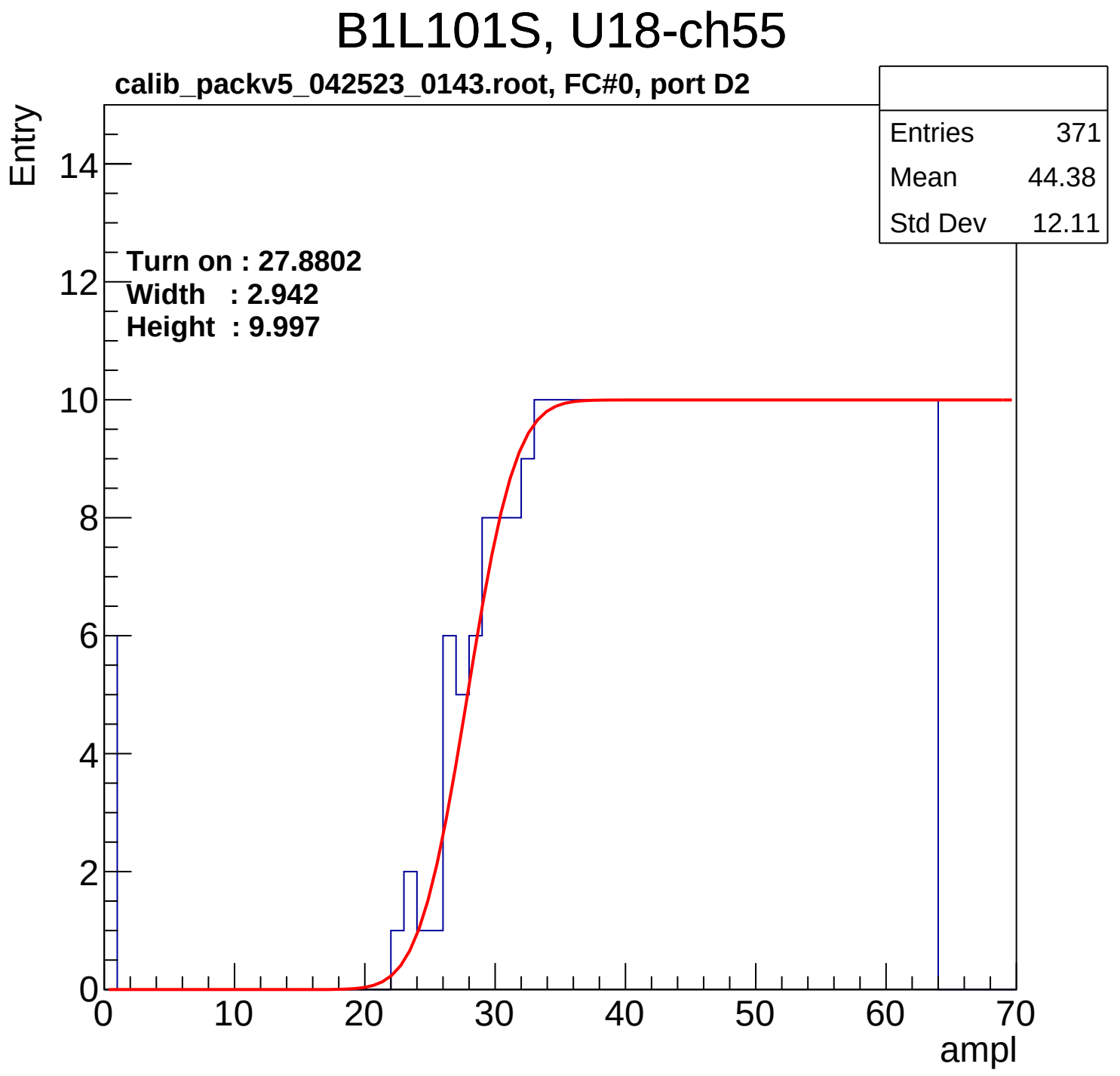
B1L101S, U18-ch55
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.38
Std Dev 12.11
Turn on : 27.8802
Width : 2.942
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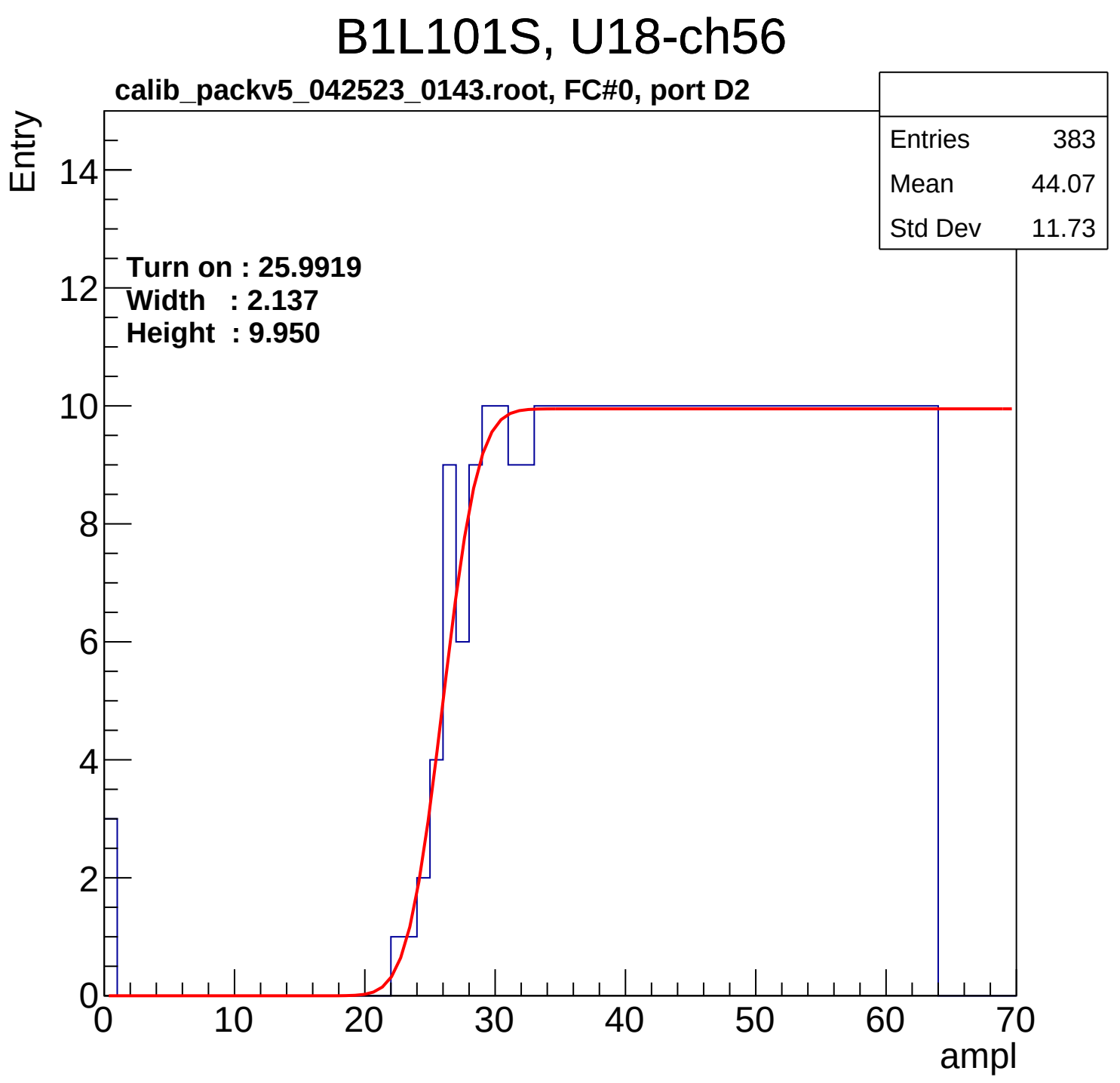
B1L101S, U18-ch56
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 44.07
Std Dev 11.73
Turn on : 25.9919
Width : 2.137
Height : 9.950
Entry
ampl
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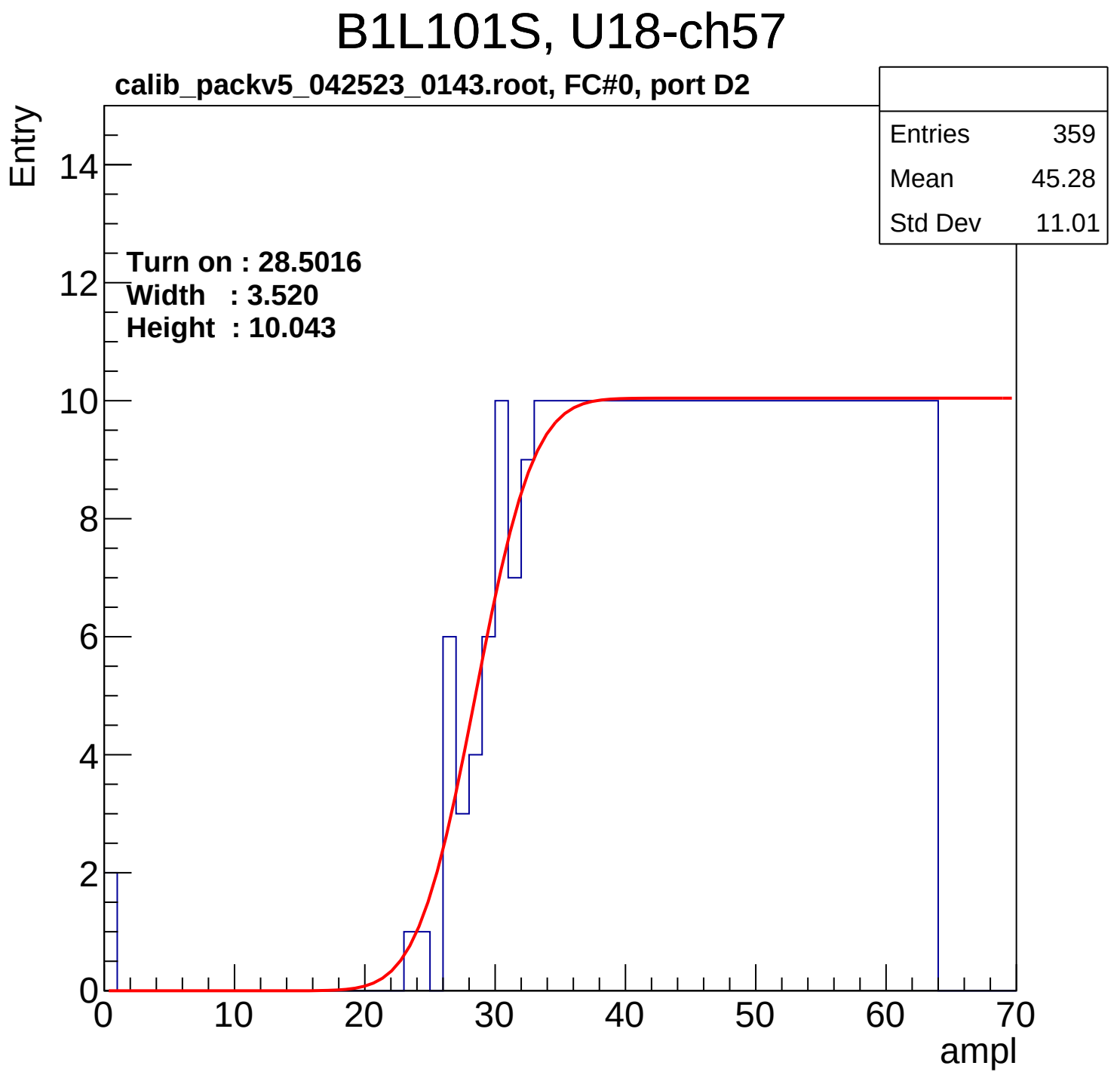
B1L101S, U18-ch57
calib_packv5_042523_0143.root, FC#0, port D2
Entries 359
Mean 45.28
Std Dev 11.01
Turn on : 28.5016
Width : 3.520
Height : 10.043
Entry
ampl
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4
6
8
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12
14
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20
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40
50
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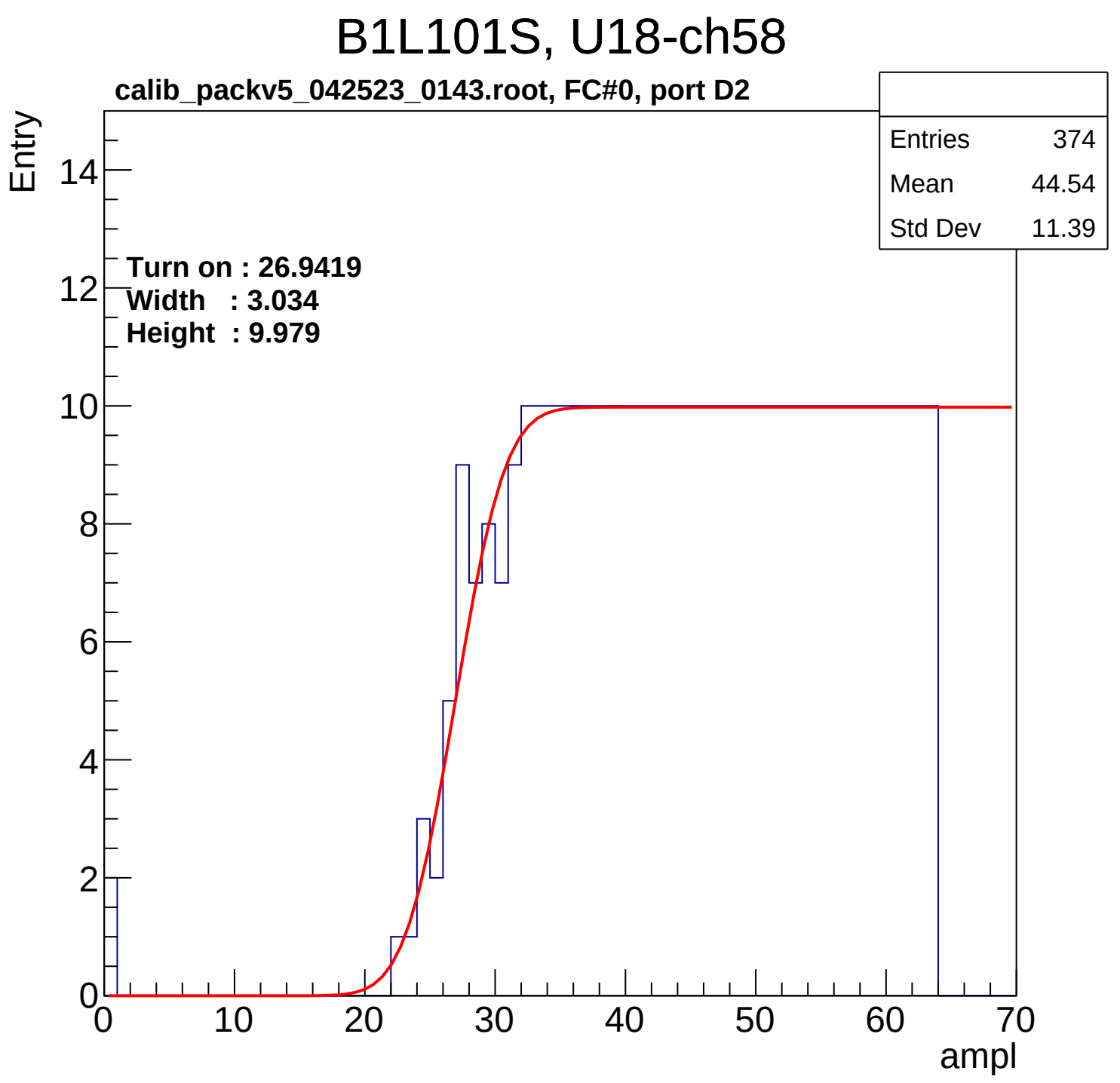
B1L101S, U18-ch58
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.54
Std Dev 11.39
Turn on : 26.9419
Width : 3.034
Height : 9.979
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ampl
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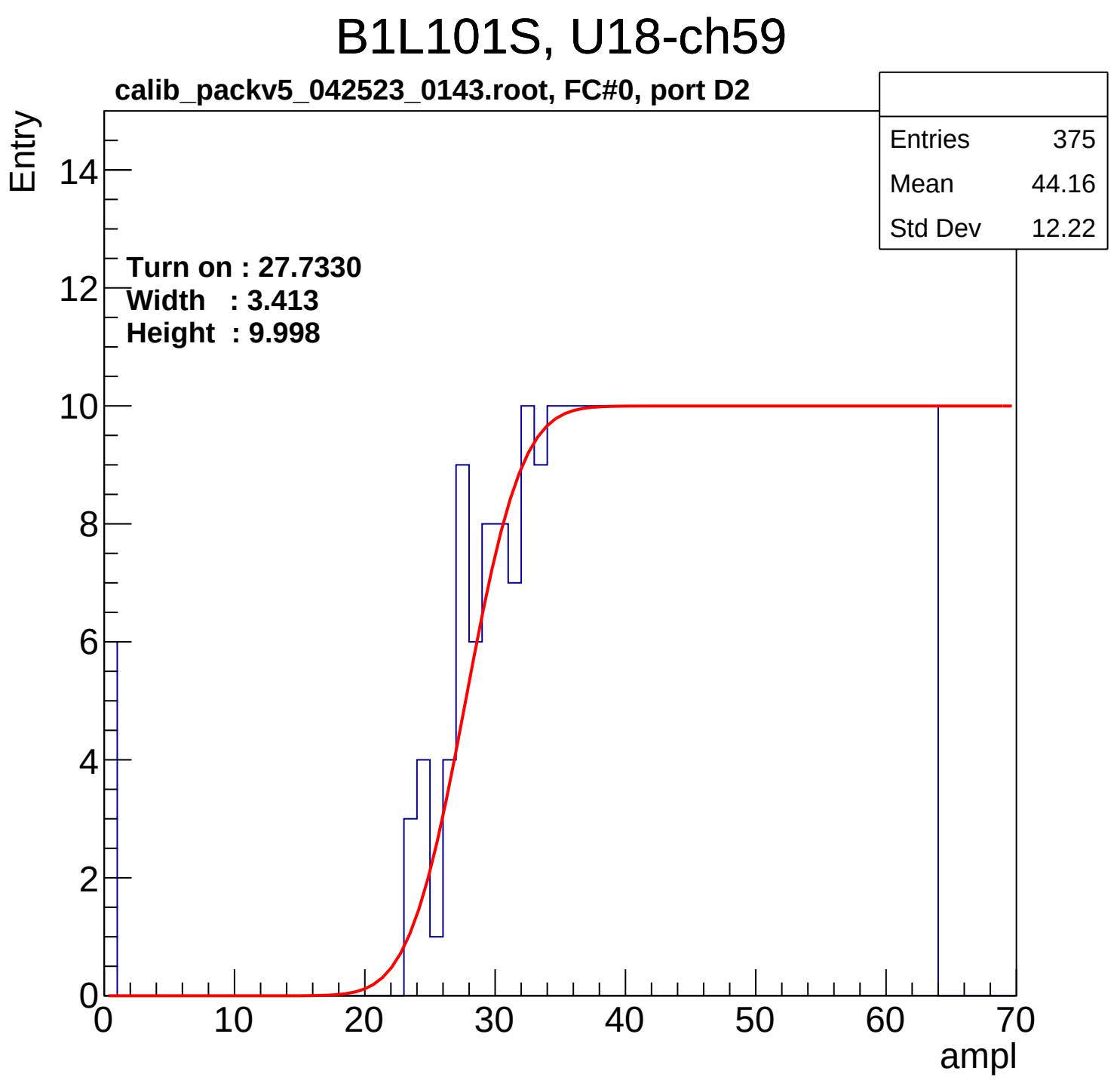
B1L101S, U18-ch59
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.16
Std Dev 12.22
Turn on : 27.7330
Width : 3.413
Height : 9.998
Entry
ampl
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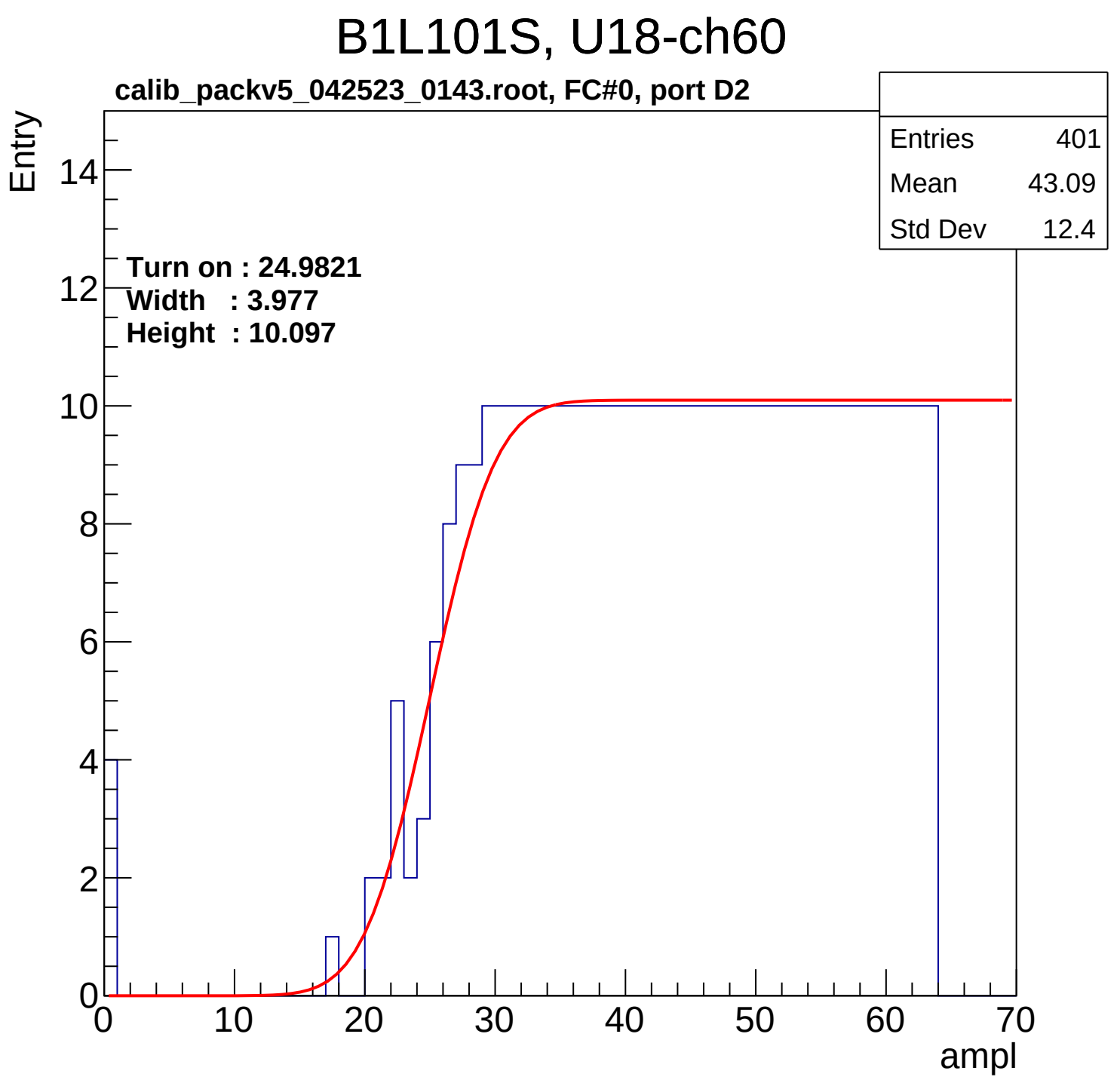
B1L101S, U18-ch60
calib_packv5_042523_0143.root, FC#0, port D2
Entries 401
Mean 43.09
Std Dev 12.4
Turn on : 24.9821
Width : 3.977
Height : 10.097
Entry
ampl
0
2
4
6
8
10
12
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0
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40
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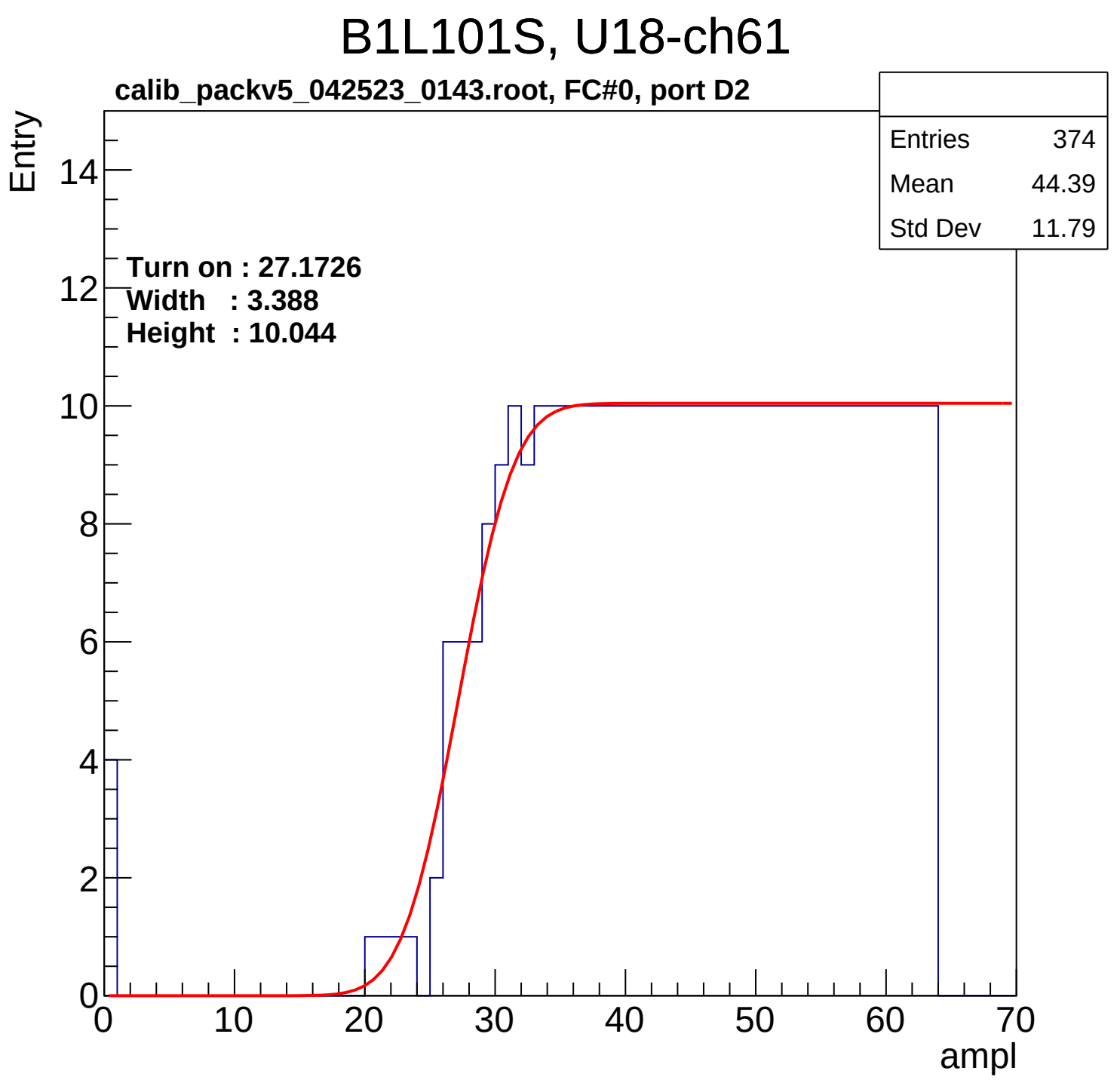
B1L101S, U18-ch61
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.39
Std Dev 11.79
Turn on : 27.1726
Width : 3.388
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
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0
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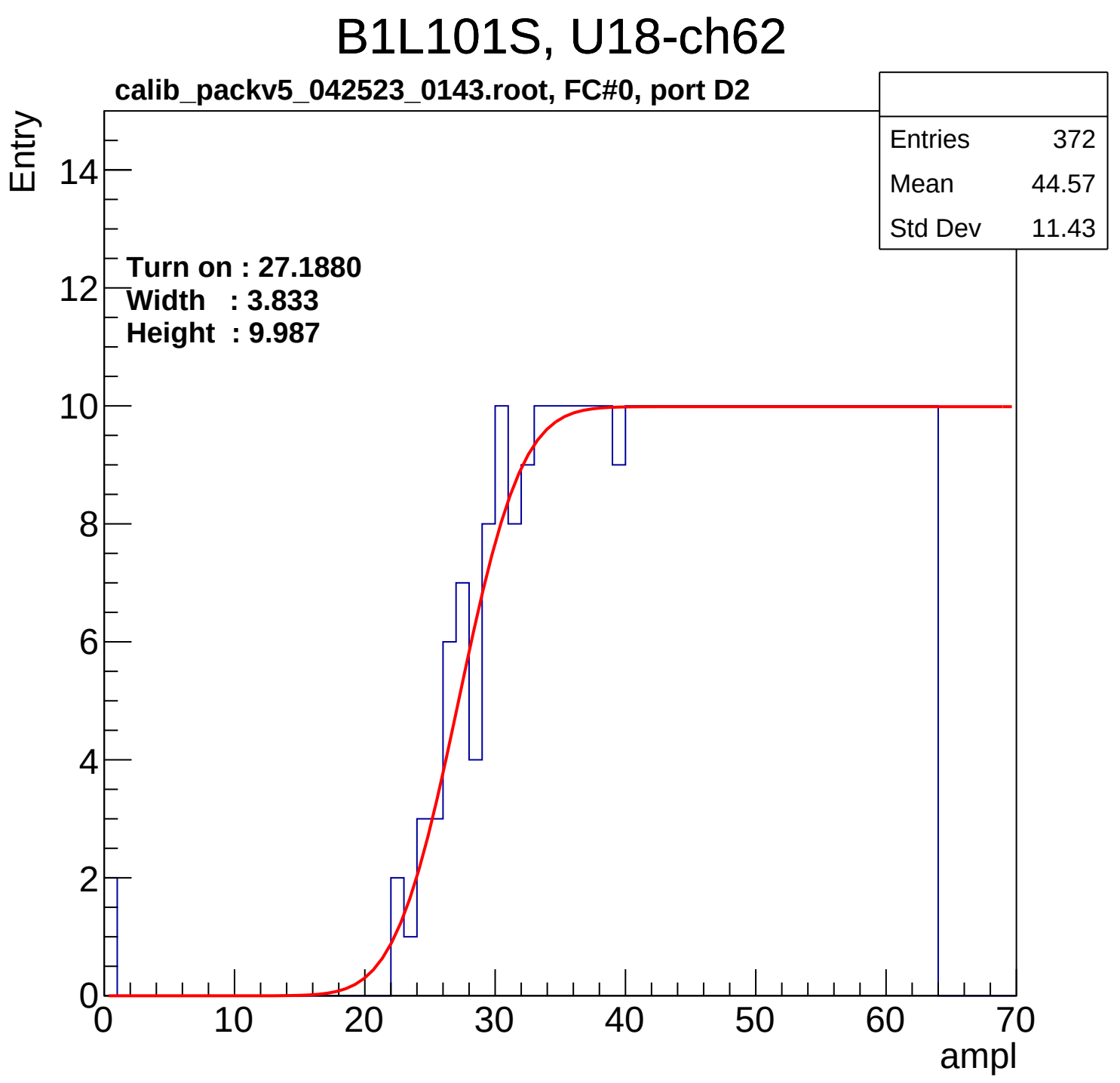
B1L101S, U18-ch62
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.57
Std Dev 11.43
Turn on : 27.1880
Width : 3.833
Height : 9.987
Entry
ampl
0
2
4
6
8
10
12
14
0
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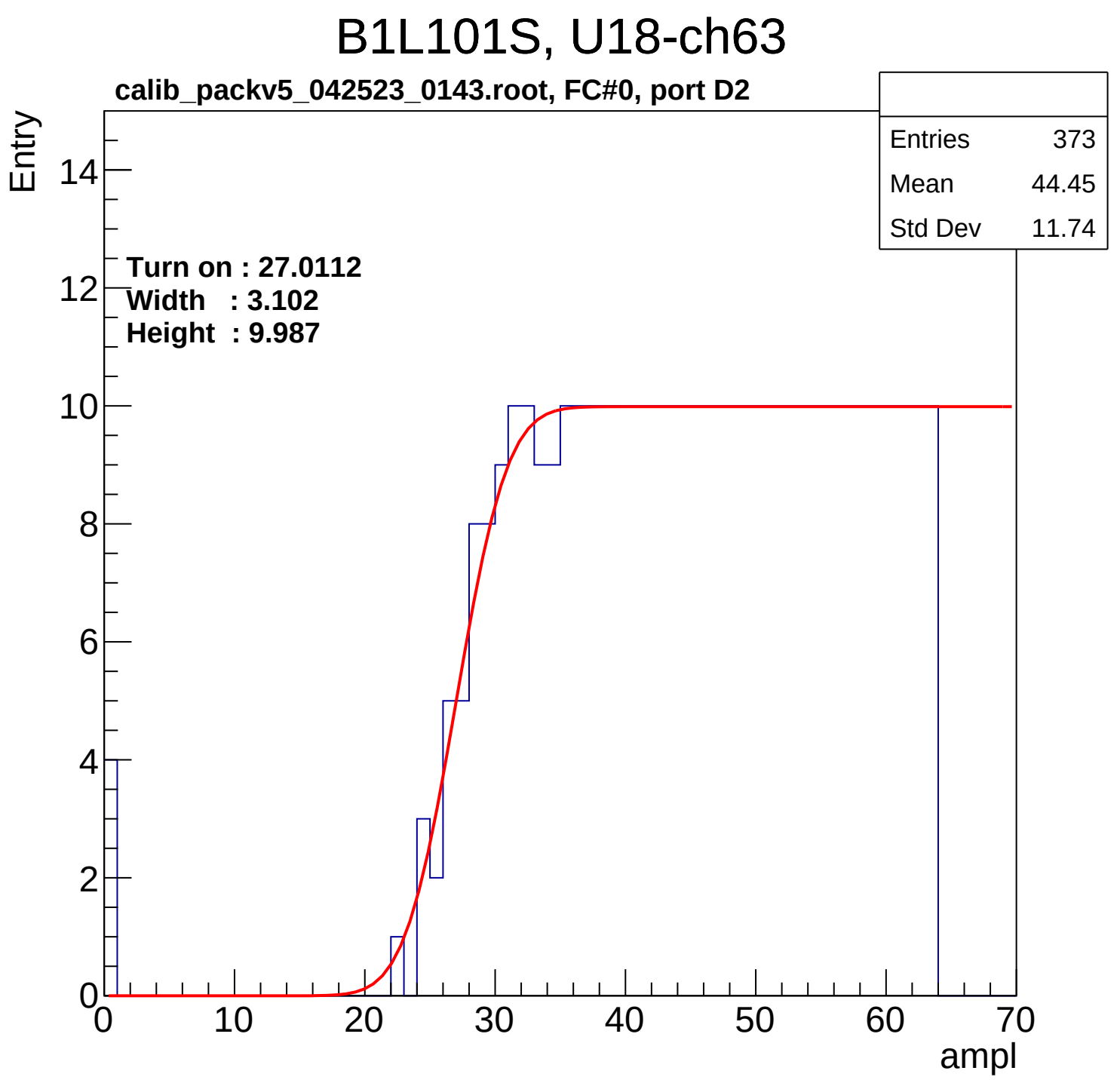
B1L101S, U18-ch63
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.45
Std Dev 11.74
Turn on : 27.0112
Width : 3.102
Height : 9.987
Entry
ampl
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2
4
6
8
10
12
14
0
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60
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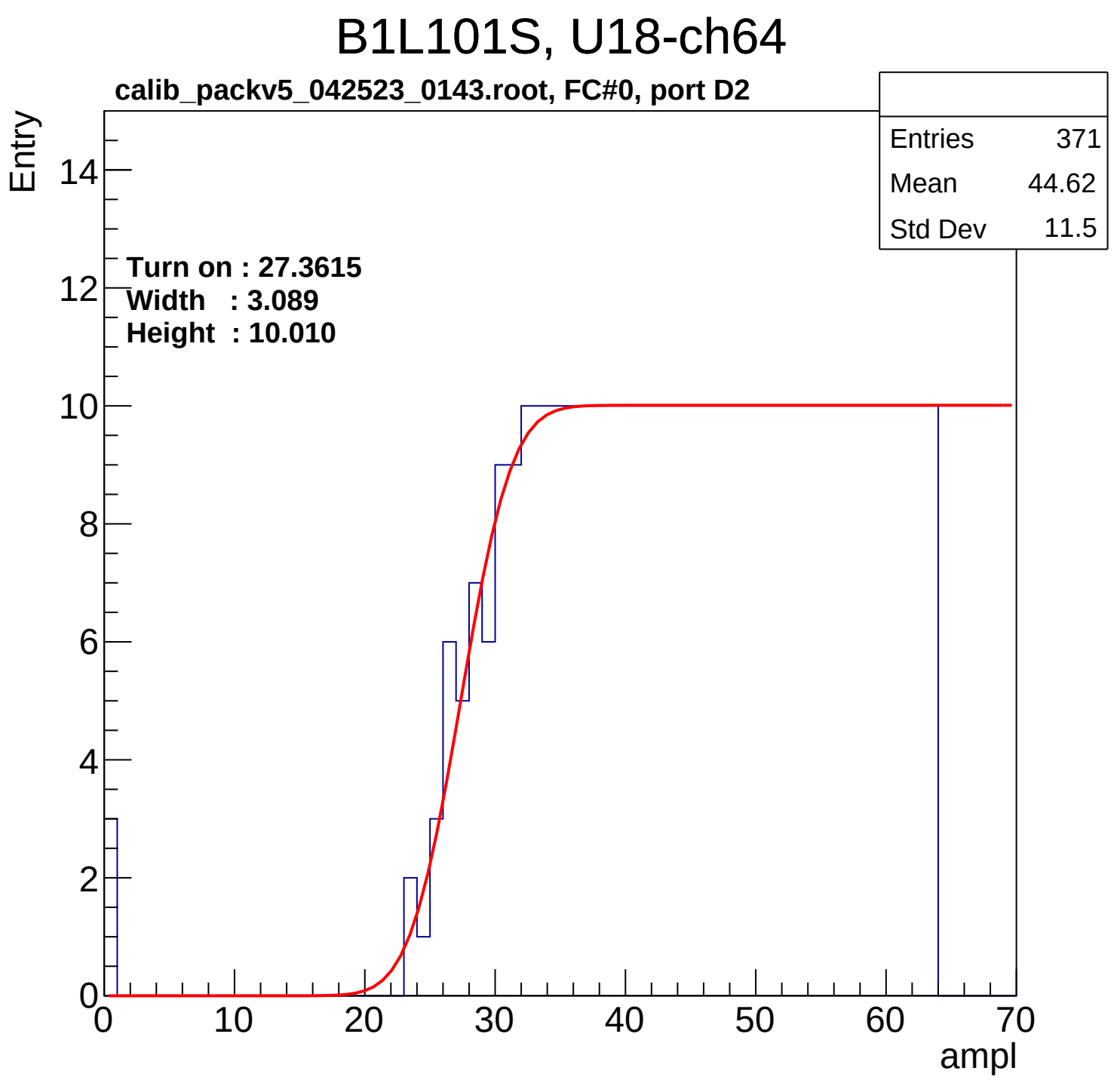
B1L101S, U18-ch64
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.62
Std Dev 11.5
Turn on : 27.3615
Width : 3.089
Height : 10.010
Entry
ampl
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6
8
10
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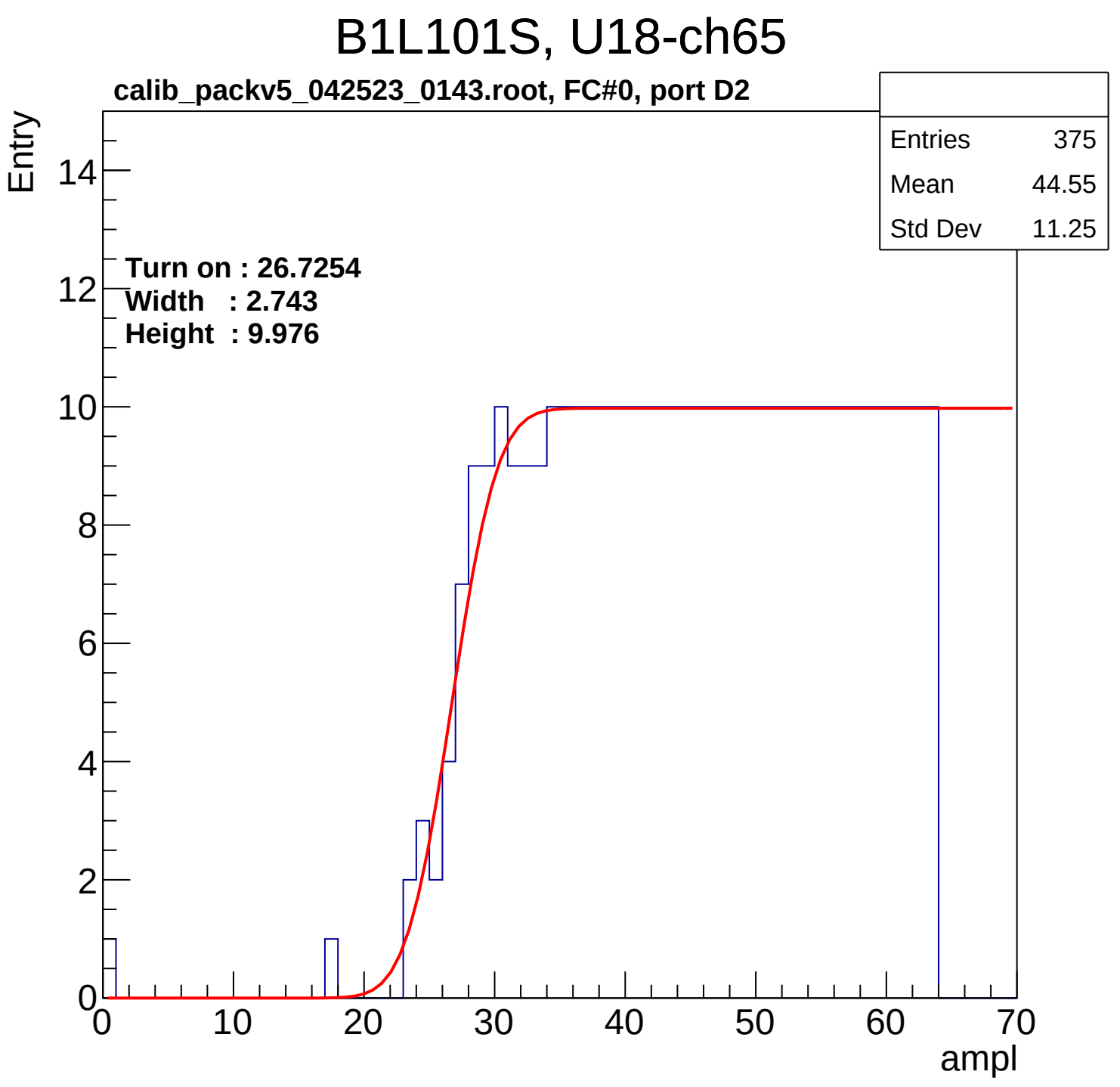
B1L101S, U18-ch65
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.55
Std Dev 11.25
Turn on : 26.7254
Width : 2.743
Height : 9.976
Entry
ampl
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2
4
6
8
10
12
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0
10
20
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40
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60
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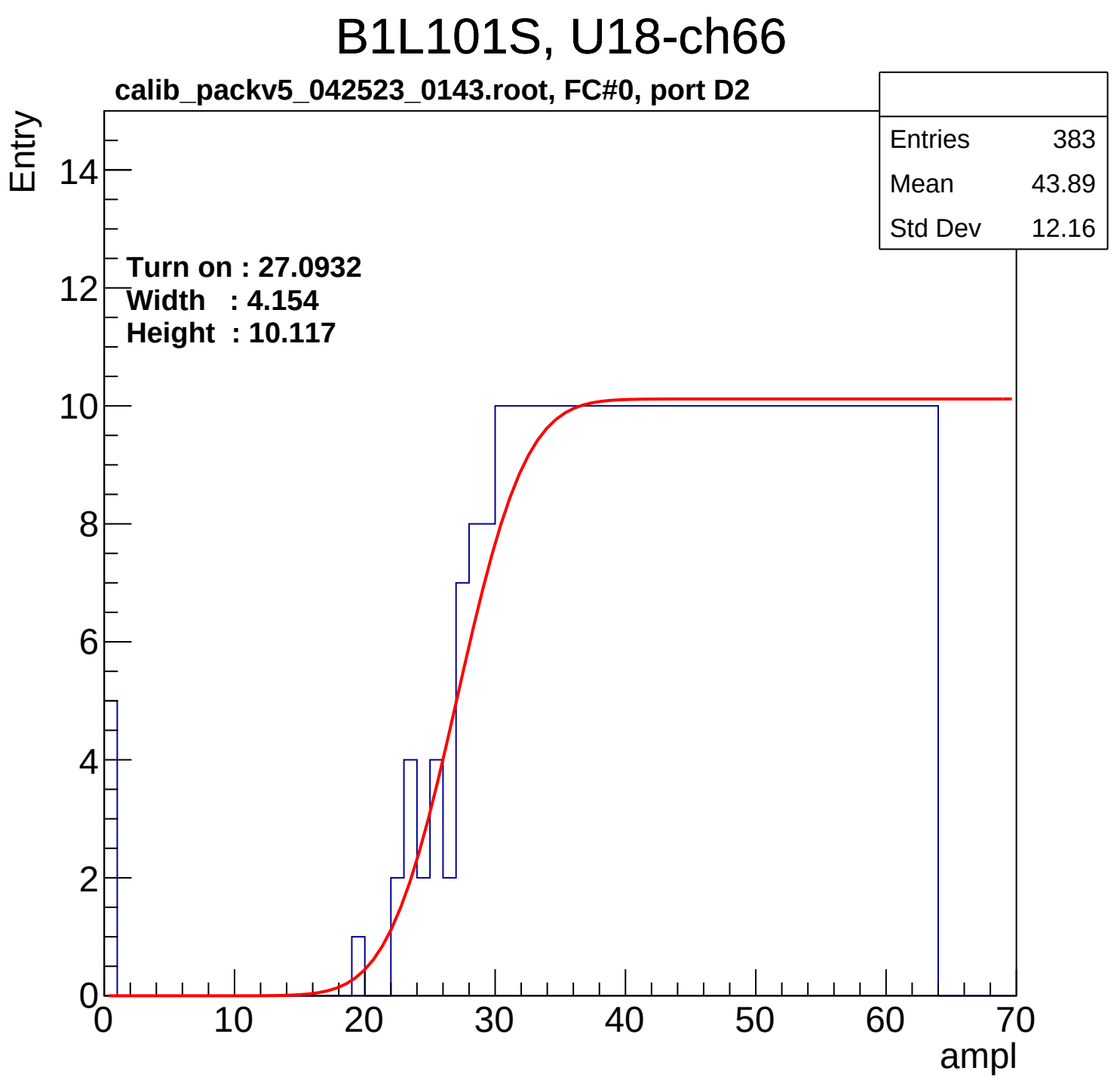
B1L101S, U18-ch66
calib_packv5_042523_0143.root, FC#0, port D2
Entries 383
Mean 43.89
Std Dev 12.16
Turn on : 27.0932
Width : 4.154
Height : 10.117
Entry
ampl
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2
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8
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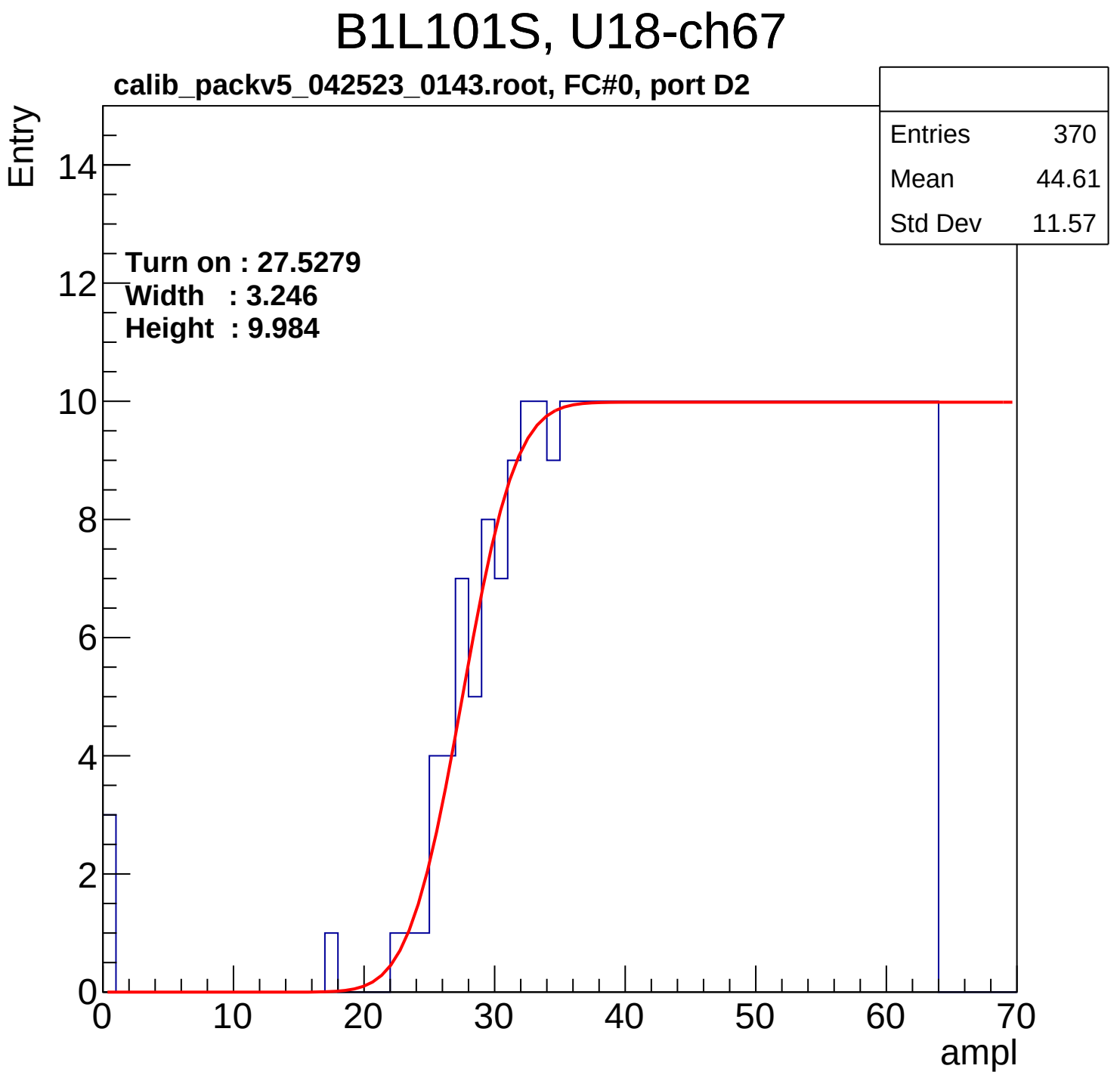
B1L101S, U18-ch67
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.61
Std Dev 11.57
Turn on : 27.5279
Width : 3.246
Height : 9.984
Entry
ampl
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2
4
6
8
10
12
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0
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60
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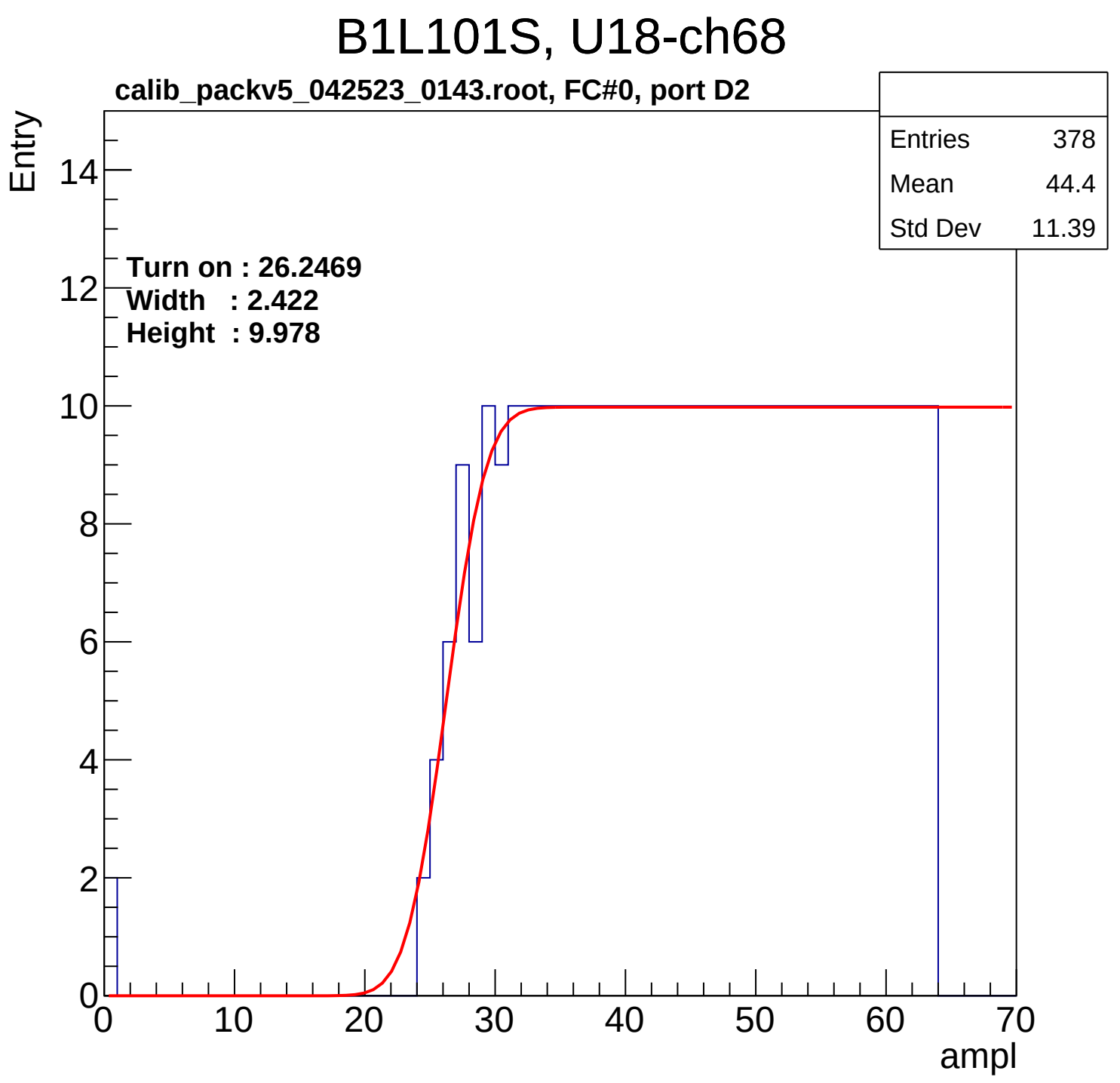
B1L101S, U18-ch68
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.4
Std Dev 11.39
Turn on : 26.2469
Width : 2.422
Height : 9.978
Entry
ampl
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4
6
8
10
12
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0
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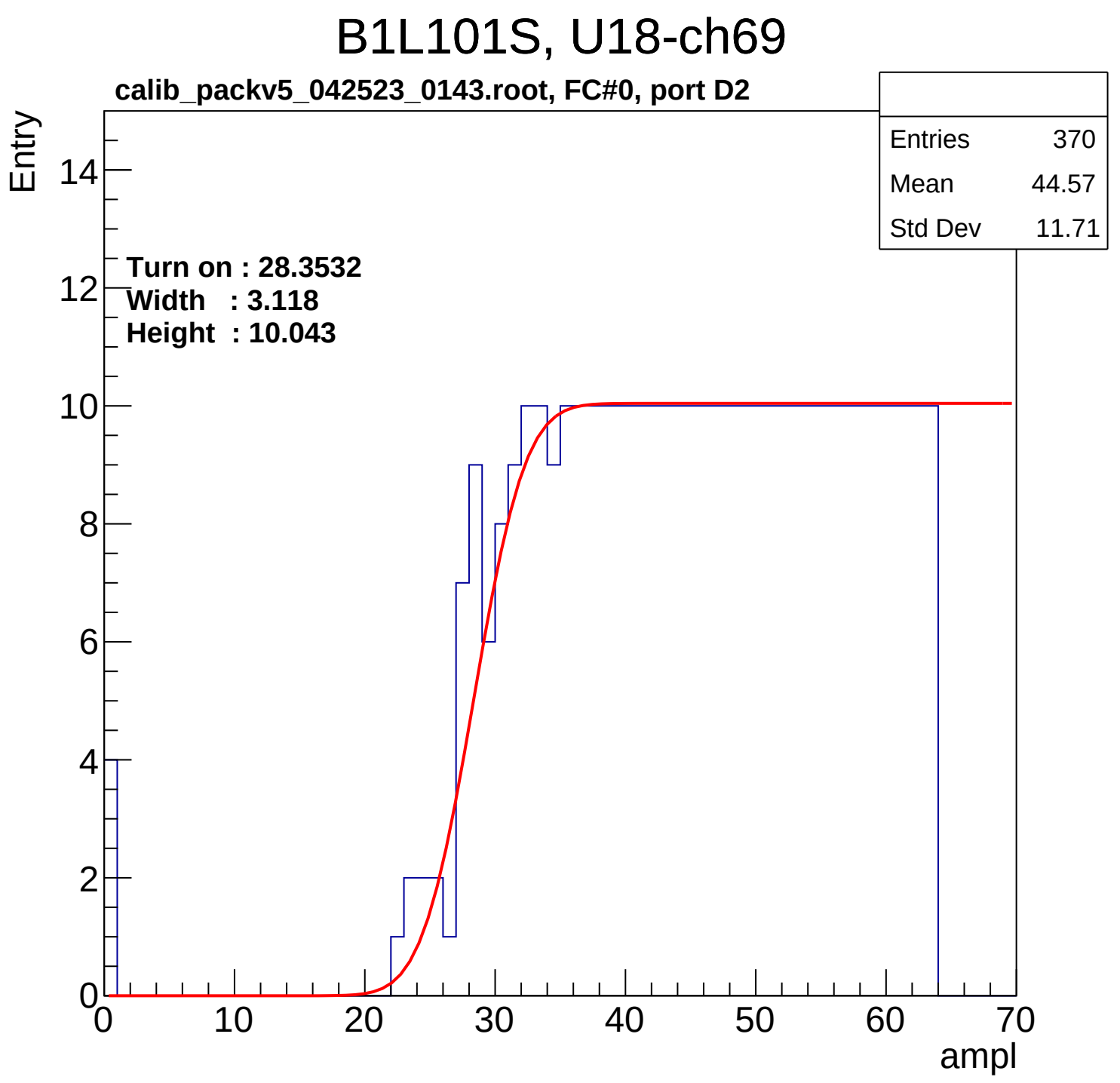
B1L101S, U18-ch69
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.57
Std Dev 11.71
Turn on : 28.3532
Width : 3.118
Height : 10.043
Entry
ampl
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4
6
8
10
12
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0
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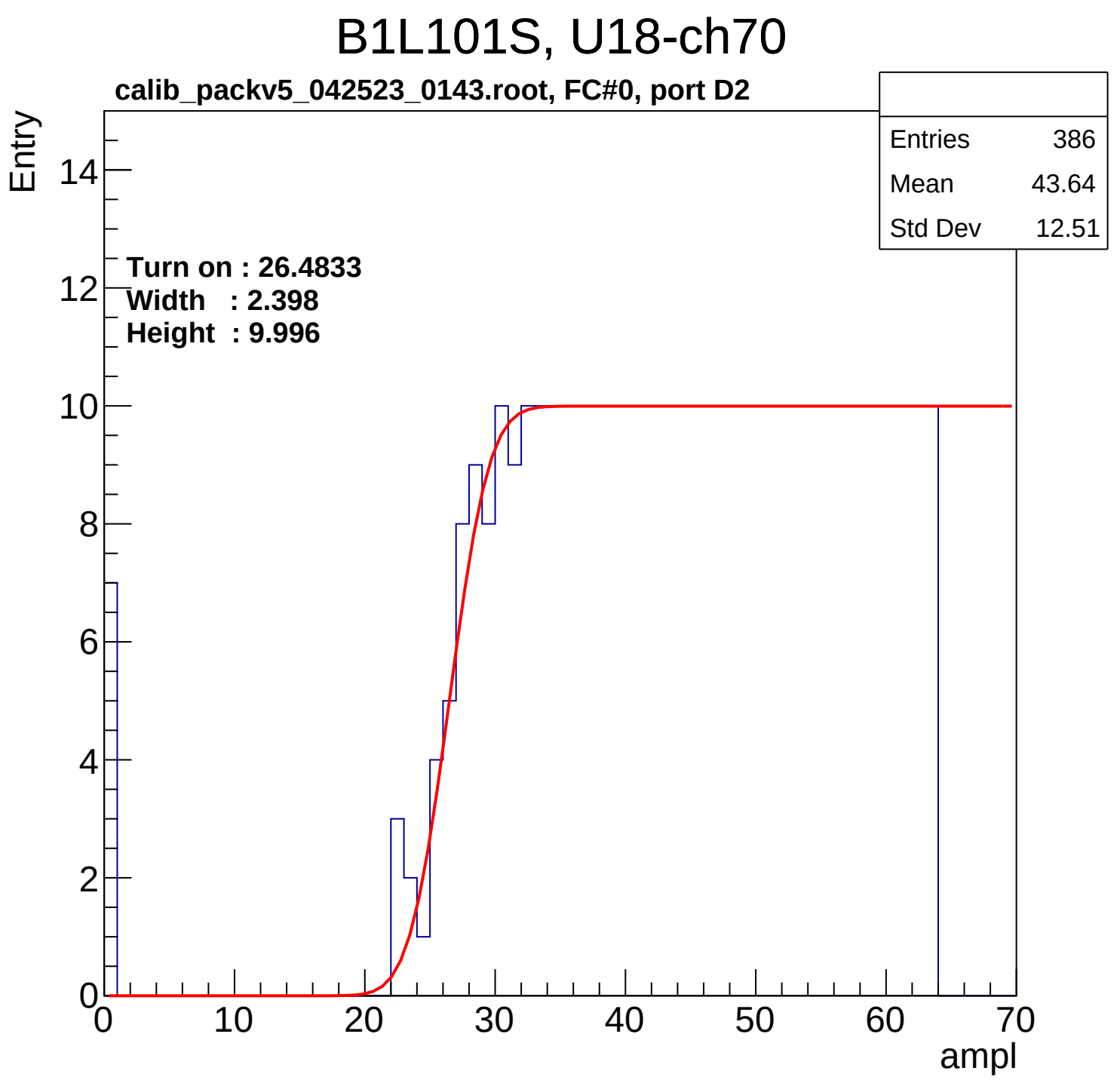
B1L101S, U18-ch70
calib_packv5_042523_0143.root, FC#0, port D2
Entries 386
Mean 43.64
Std Dev 12.51
Turn on : 26.4833
Width : 2.398
Height : 9.996
Entry
ampl
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2
4
6
8
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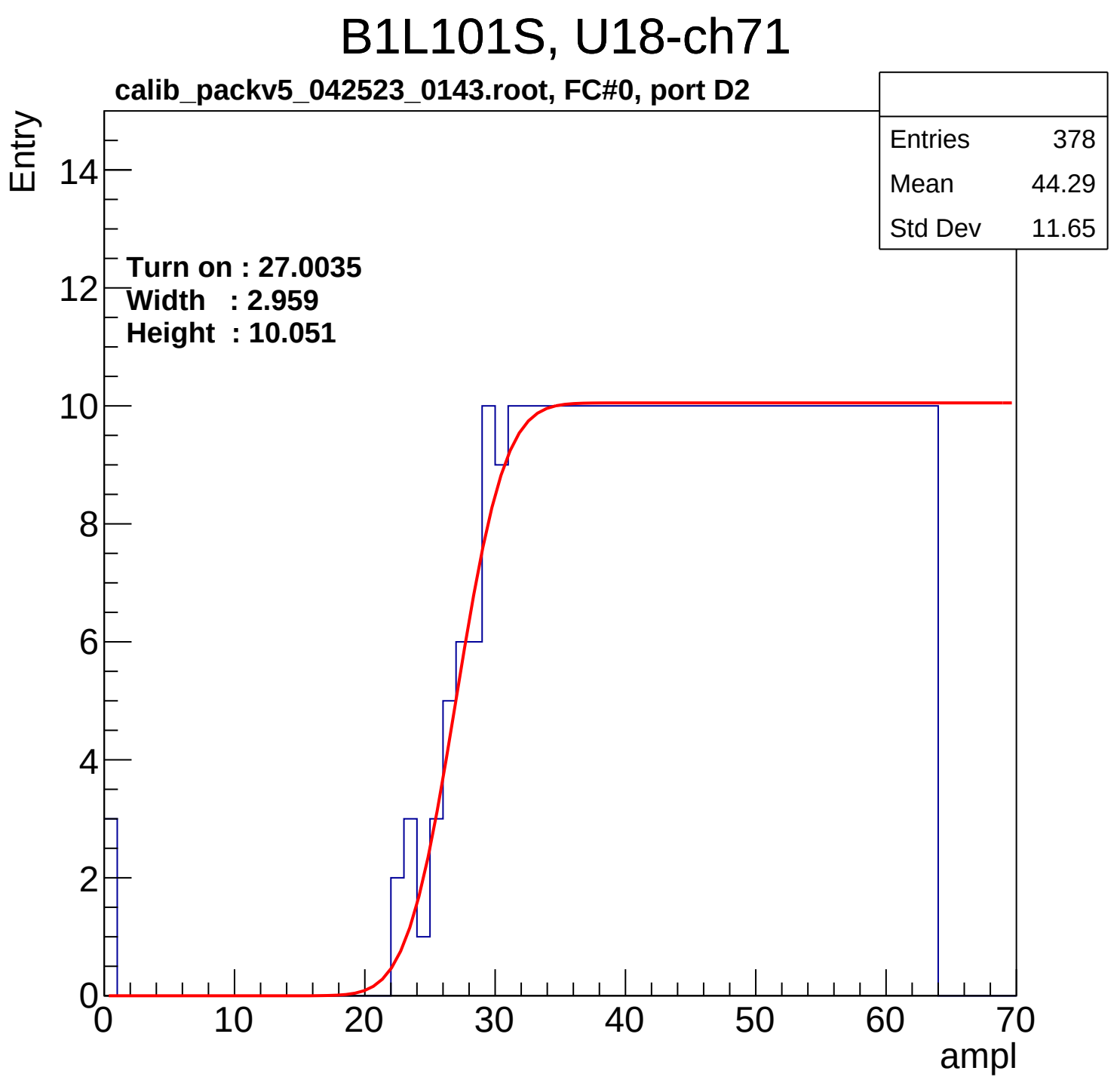
B1L101S, U18-ch71
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.29
Std Dev 11.65
Turn on : 27.0035
Width : 2.959
Height : 10.051
Entry
ampl
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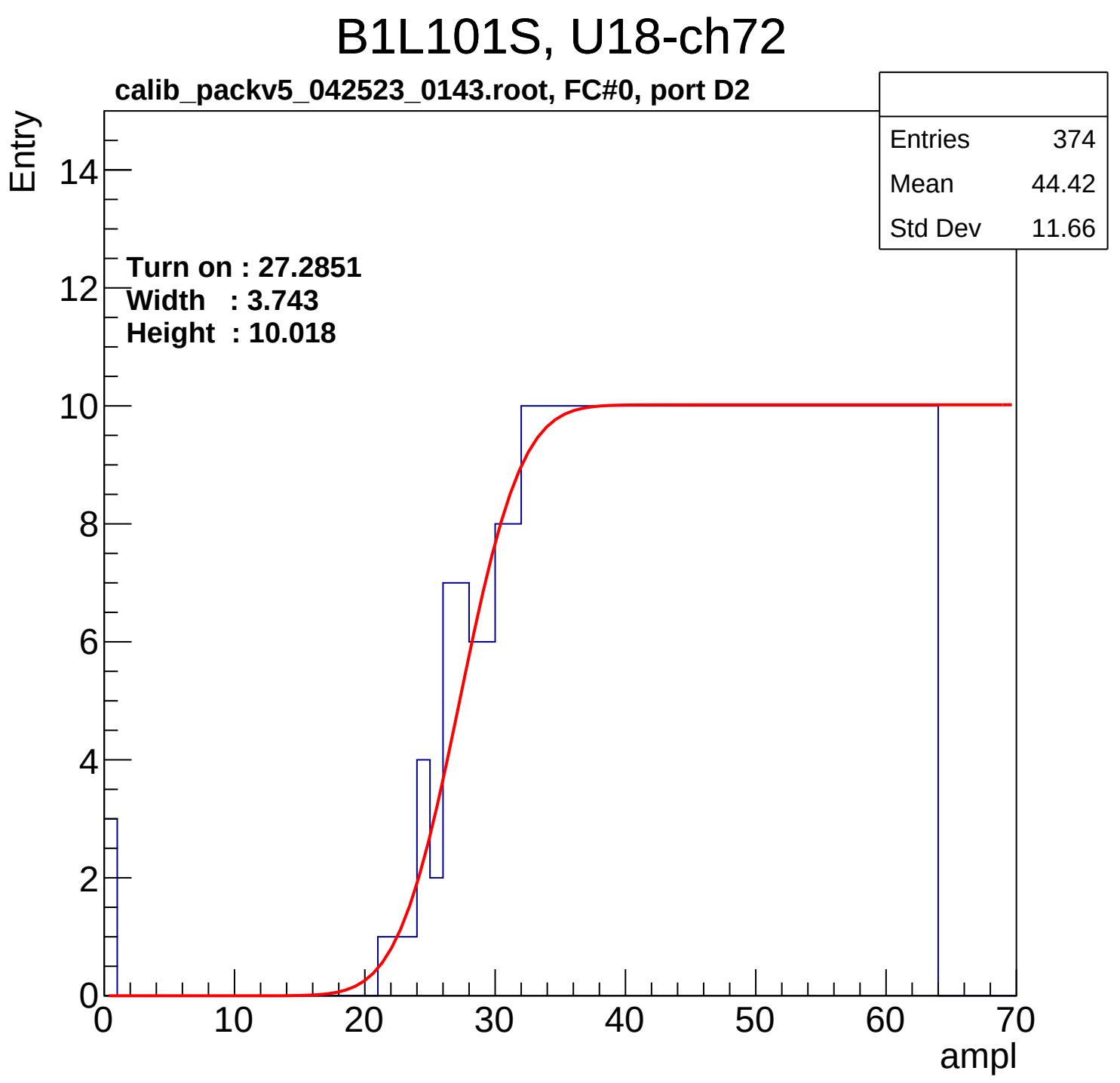
B1L101S, U18-ch72
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.42
Std Dev 11.66
Turn on : 27.2851
Width : 3.743
Height : 10.018
Entry
ampl
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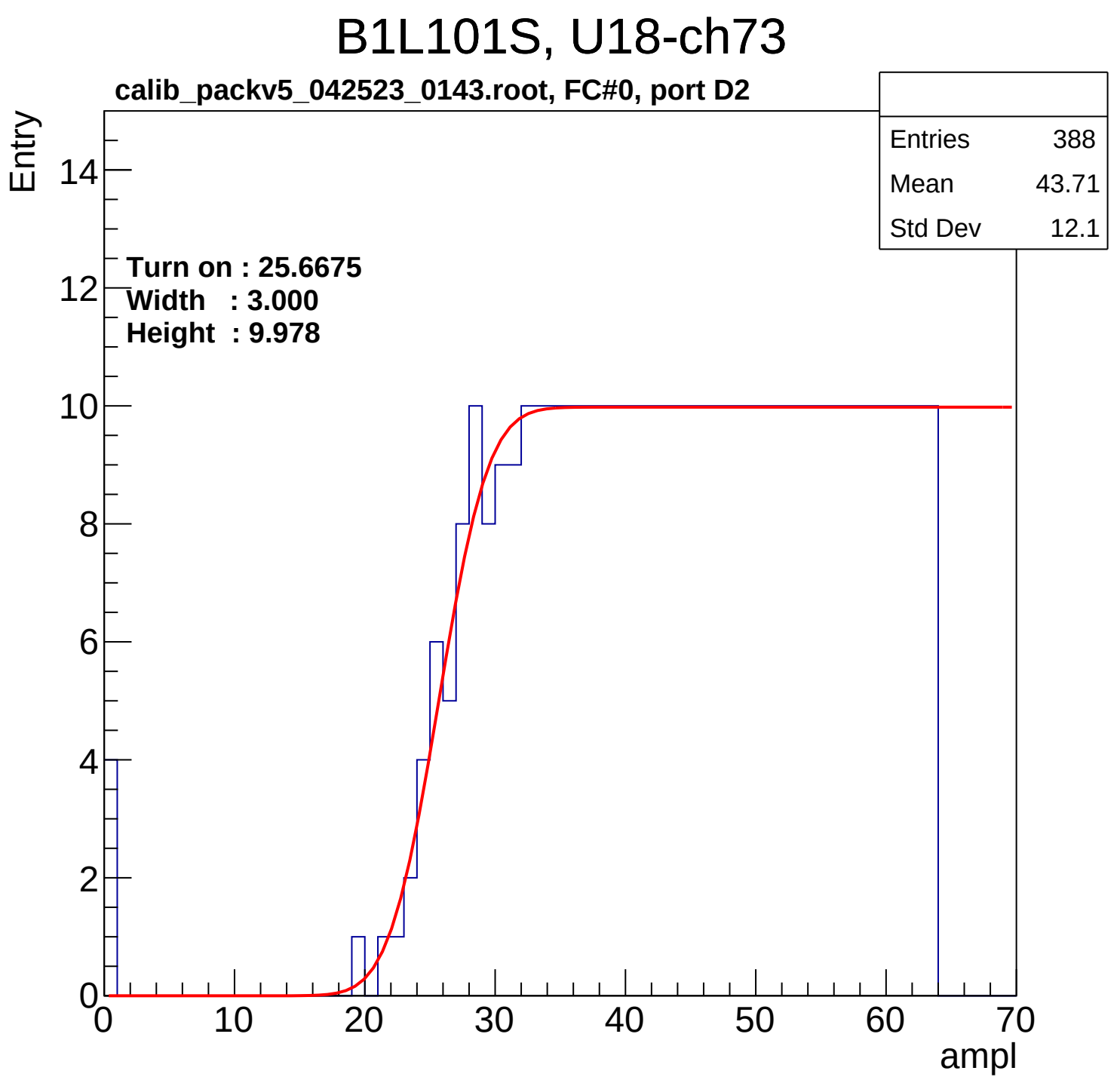
B1L101S, U18-ch73
calib_packv5_042523_0143.root, FC#0, port D2
Entries 388
Mean 43.71
Std Dev 12.1
Turn on : 25.6675
Width : 3.000
Height : 9.978
Entry
ampl
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6
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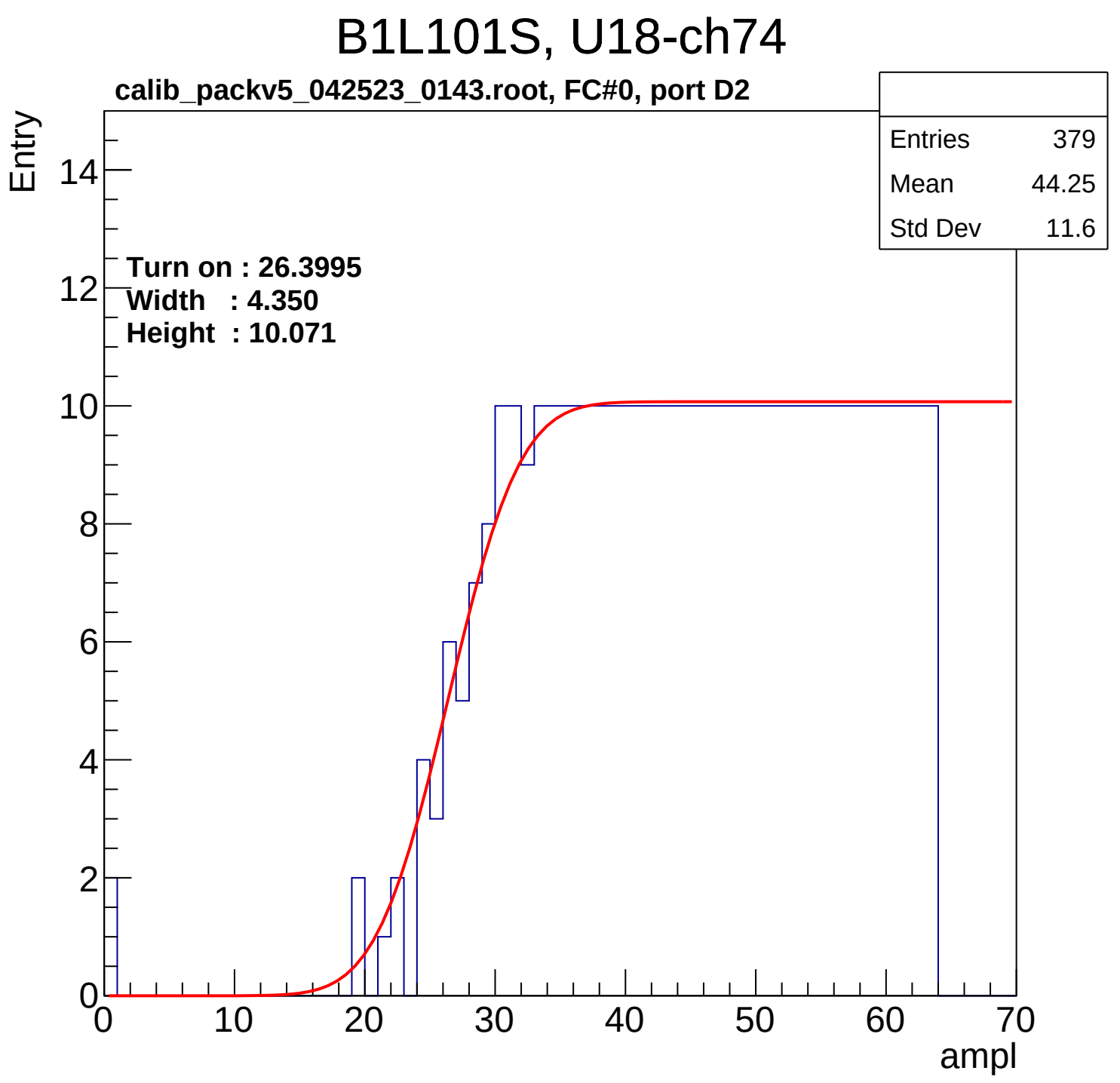
B1L101S, U18-ch74
calib_packv5_042523_0143.root, FC#0, port D2
Entries 379
Mean 44.25
Std Dev 11.6
Turn on : 26.3995
Width : 4.350
Height : 10.071
Entry
ampl
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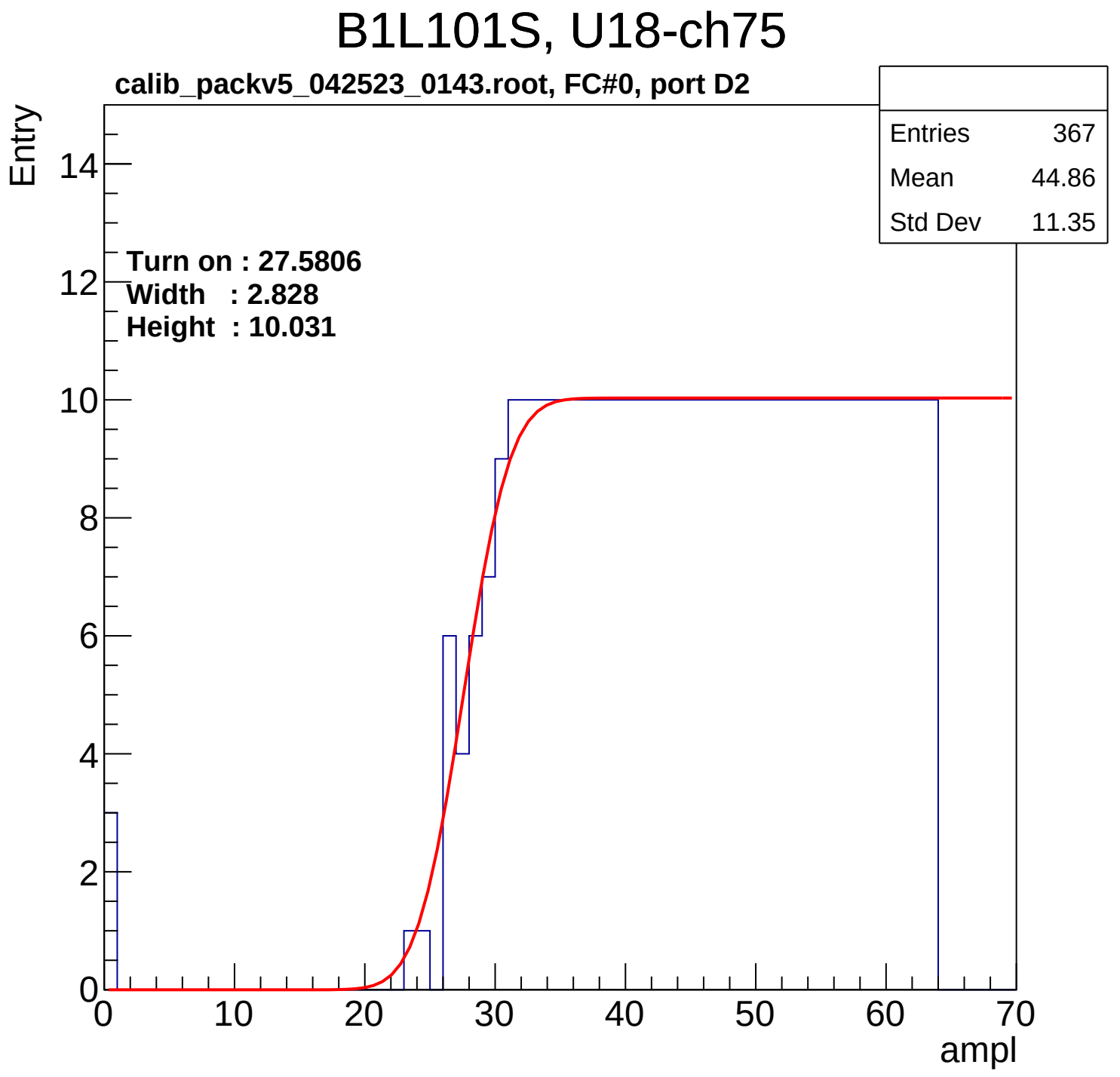
B1L101S, U18-ch75
calib_packv5_042523_0143.root, FC#0, port D2
Entries 367
Mean 44.86
Std Dev 11.35
Turn on : 27.5806
Width : 2.828
Height : 10.031
Entry
ampl
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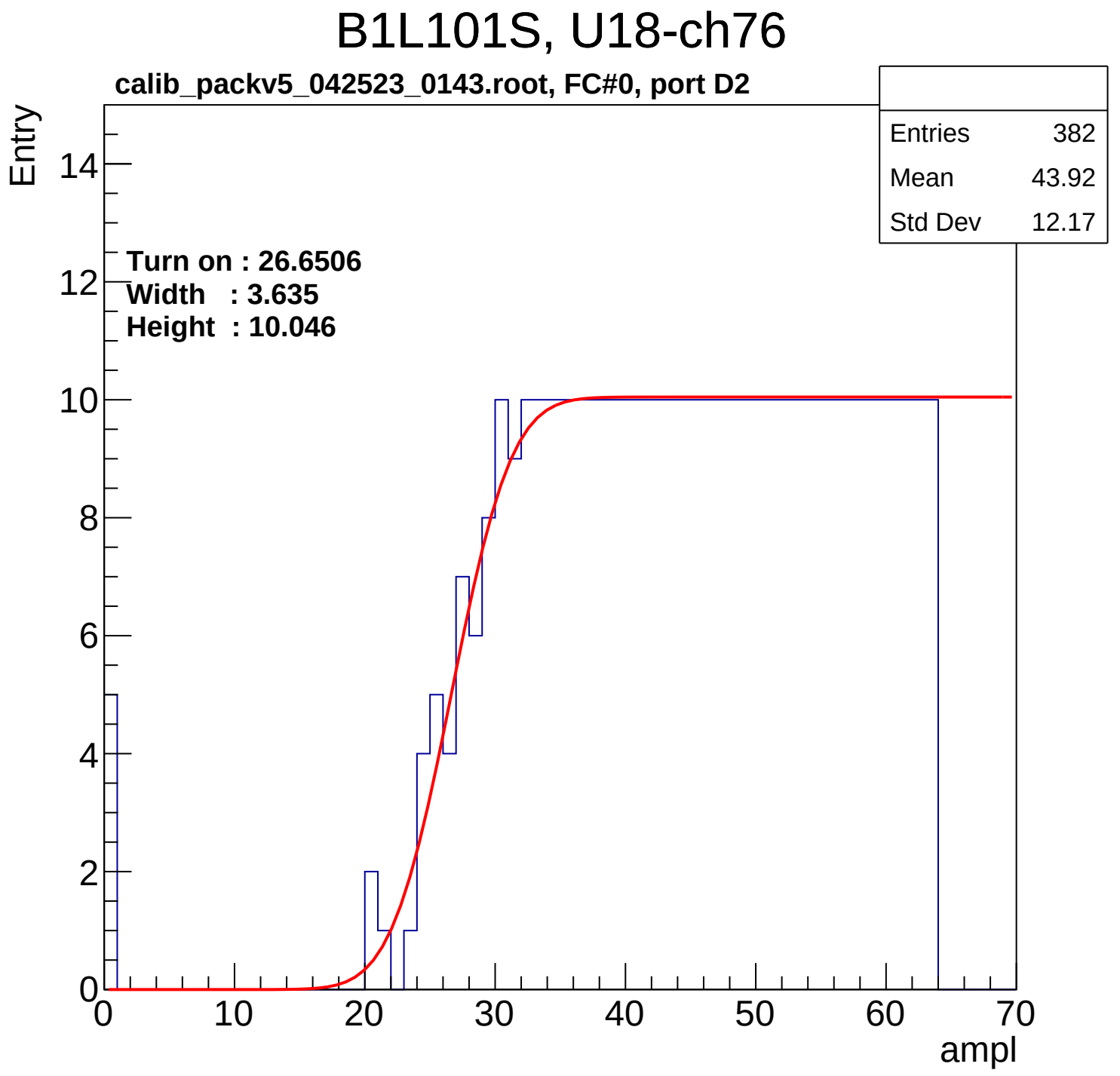
B1L101S, U18-ch76
calib_packv5_042523_0143.root, FC#0, port D2
Entries 382
Mean 43.92
Std Dev 12.17
Turn on : 26.6506
Width : 3.635
Height : 10.046
Entry
ampl
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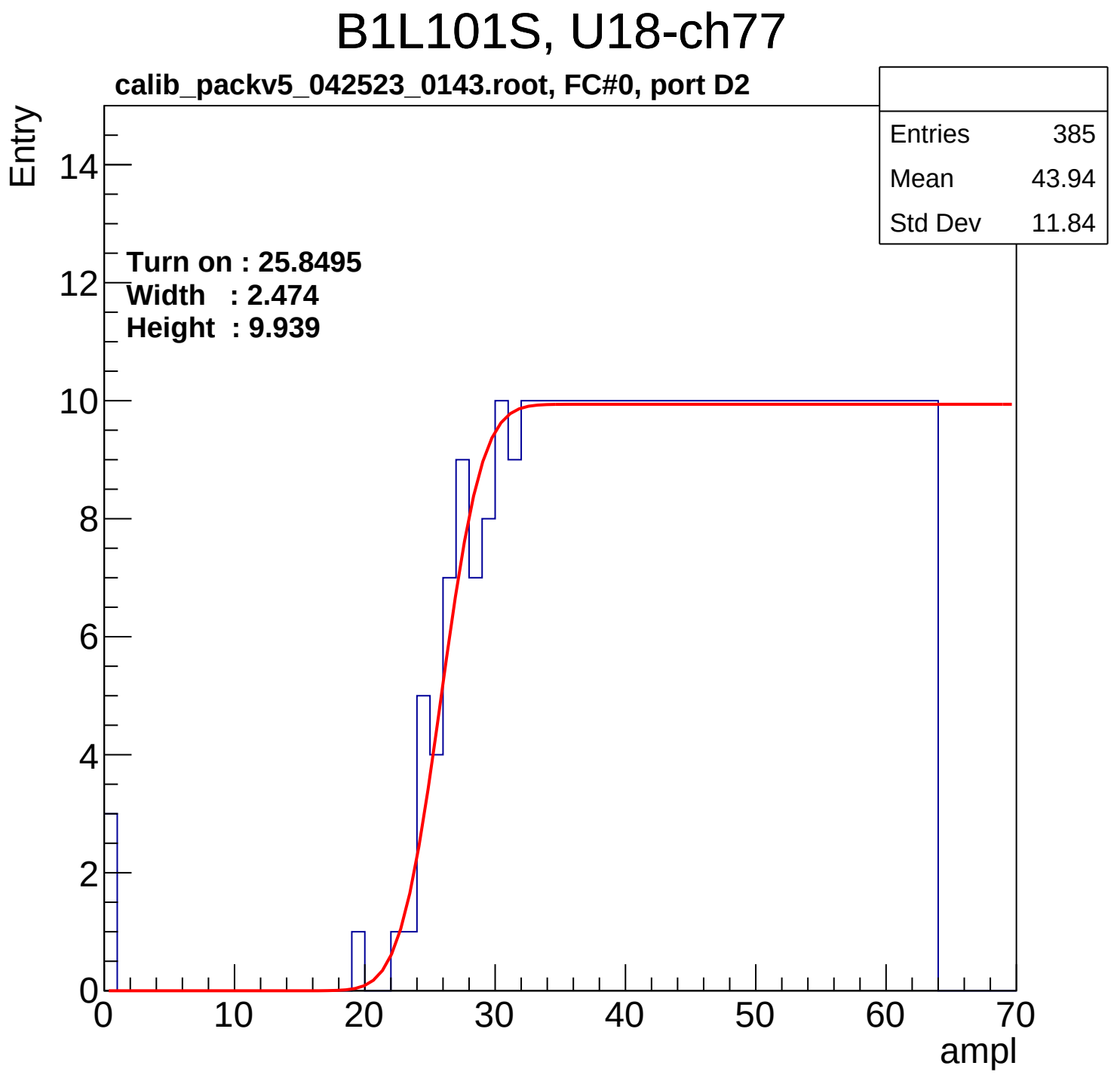
B1L101S, U18-ch77
calib_packv5_042523_0143.root, FC#0, port D2
Entries 385
Mean 43.94
Std Dev 11.84
Turn on : 25.8495
Width : 2.474
Height : 9.939
Entry
ampl
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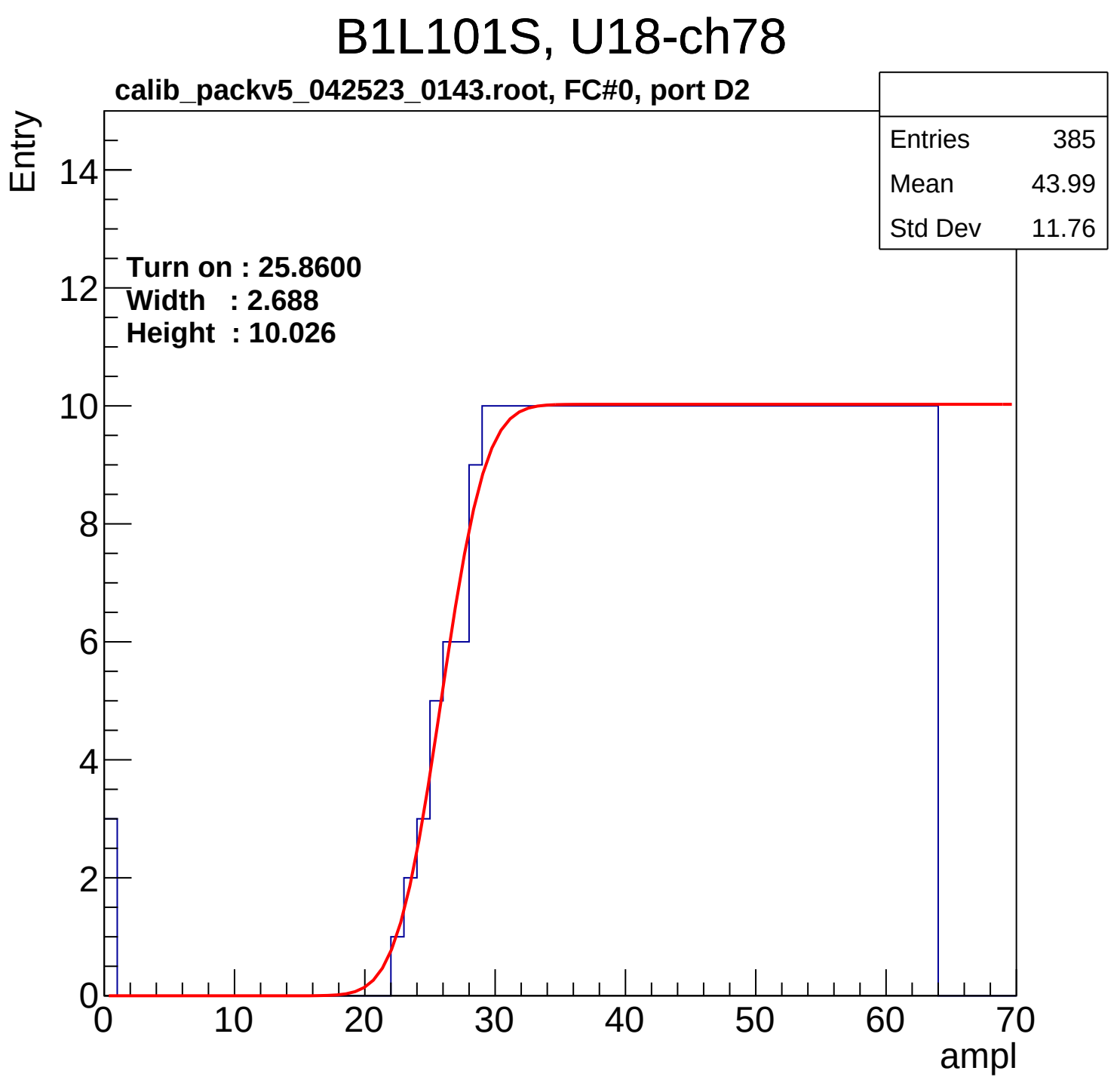
B1L101S, U18-ch78
calib_packv5_042523_0143.root, FC#0, port D2
Entries 385
Mean 43.99
Std Dev 11.76
Turn on : 25.8600
Width : 2.688
Height : 10.026
Entry
ampl
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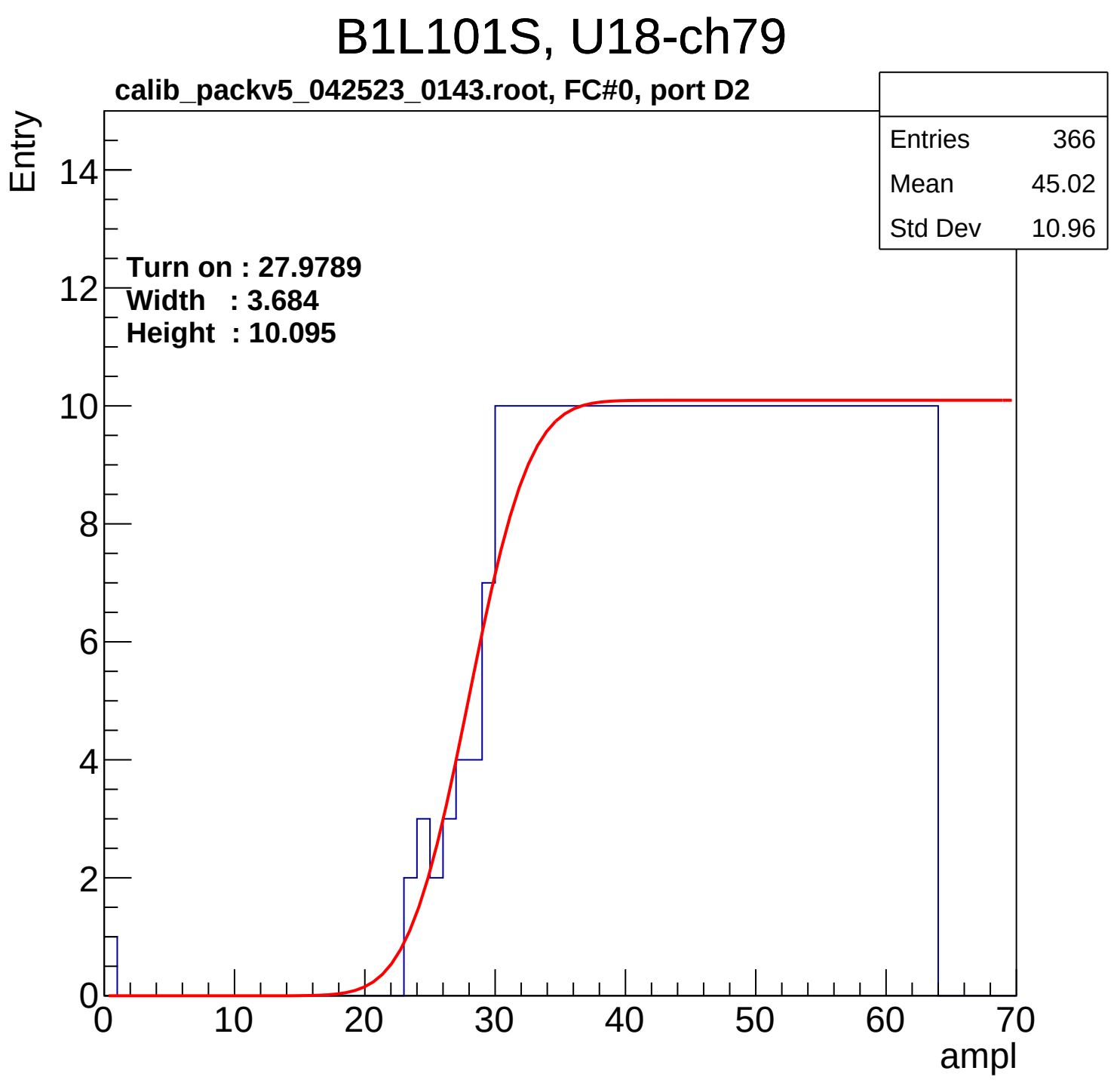
B1L101S, U18-ch79
calib_packv5_042523_0143.root, FC#0, port D2
Entries 366
Mean 45.02
Std Dev 10.96
Turn on : 27.9789
Width : 3.684
Height : 10.095
Entry
ampl
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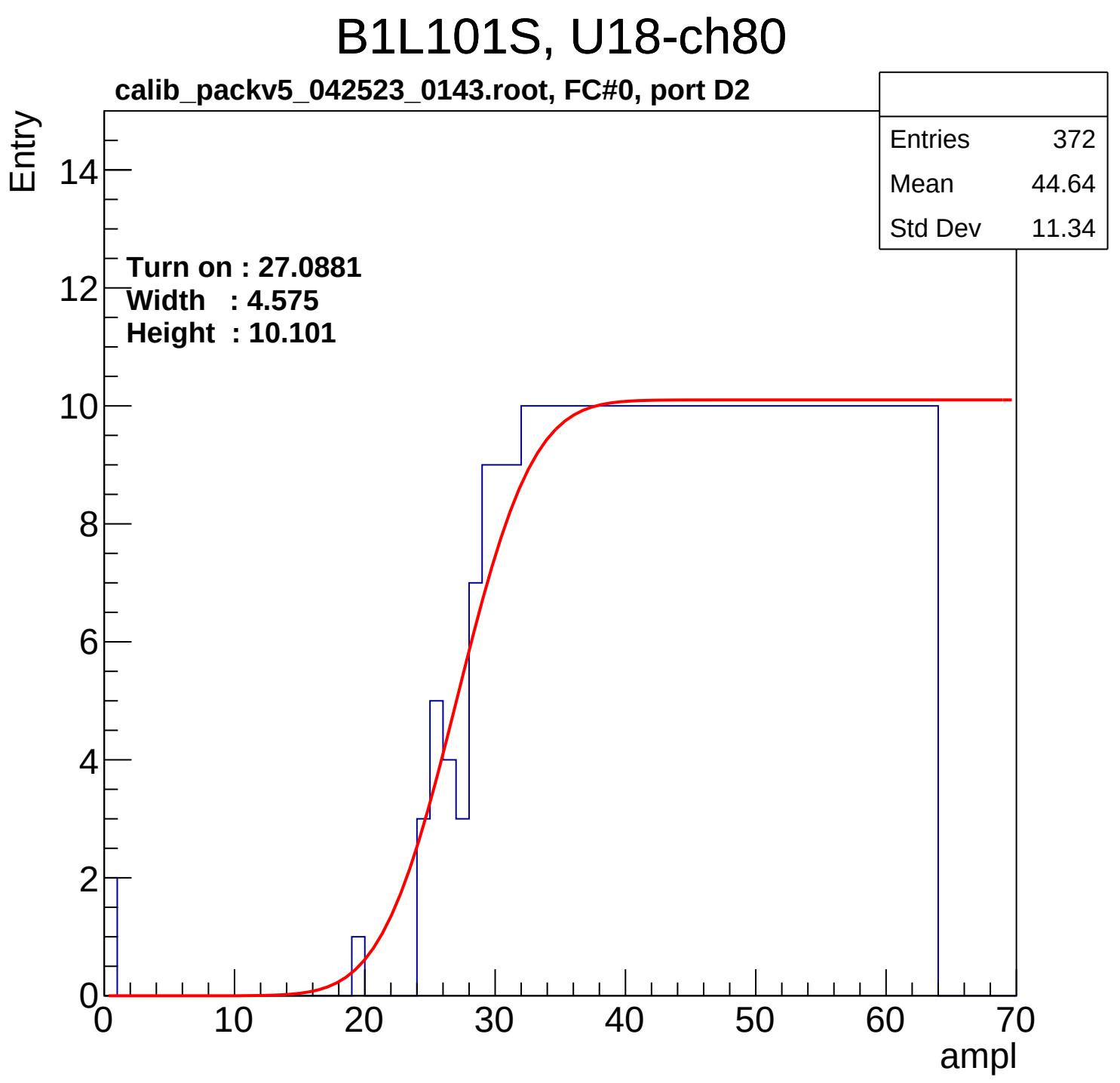
B1L101S, U18-ch80
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.64
Std Dev 11.34
Turn on : 27.0881
Width : 4.575
Height : 10.101
Entry
ampl
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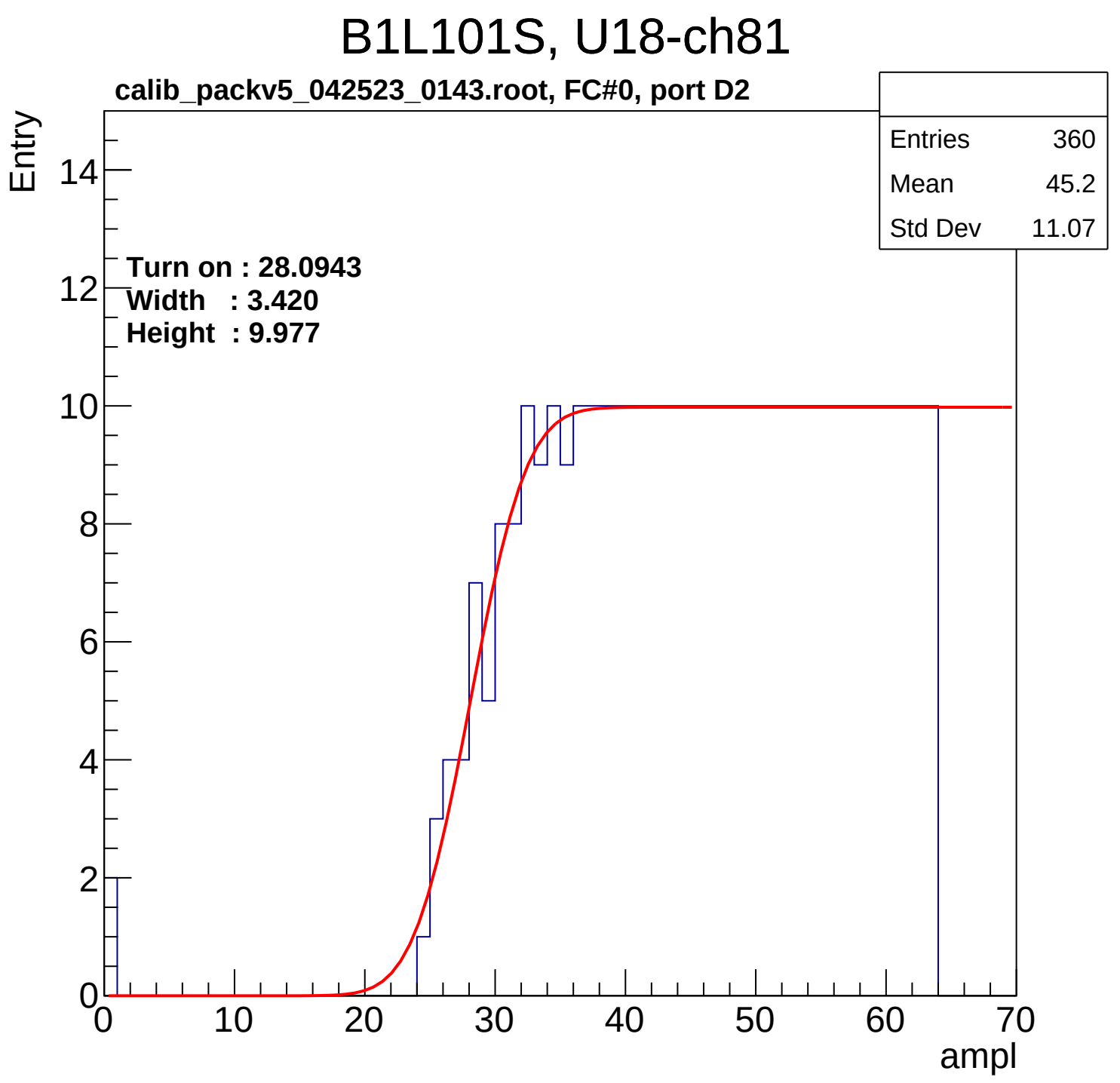
B1L101S, U18-ch81
calib_packv5_042523_0143.root, FC#0, port D2
Entries 360
Mean 45.2
Std Dev 11.07
Turn on : 28.0943
Width : 3.420
Height : 9.977
Entry
ampl
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4
6
8
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0
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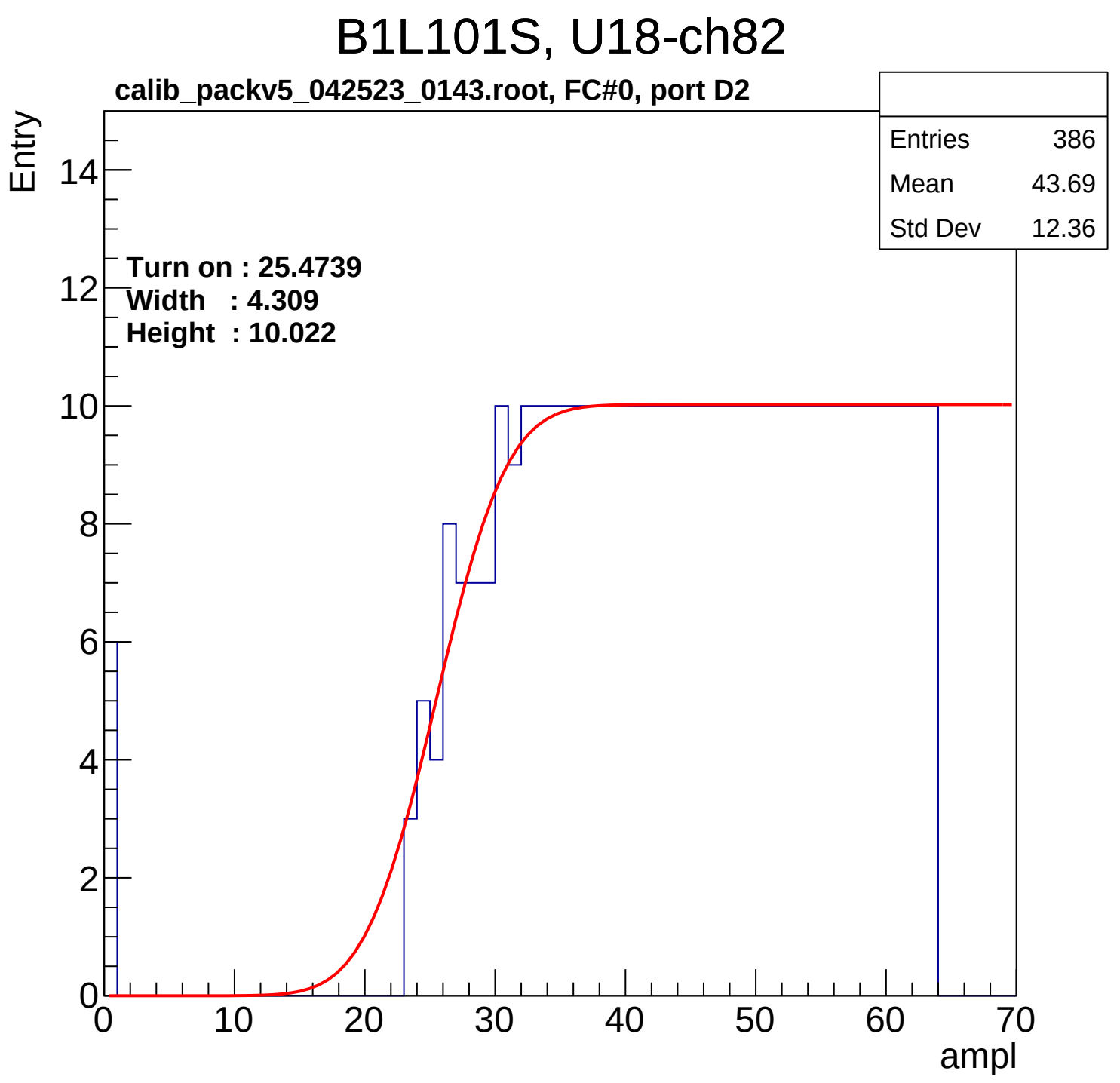
B1L101S, U18-ch82
calib_packv5_042523_0143.root, FC#0, port D2
Entries 386
Mean 43.69
Std Dev 12.36
Turn on : 25.4739
Width : 4.309
Height : 10.022
Entry
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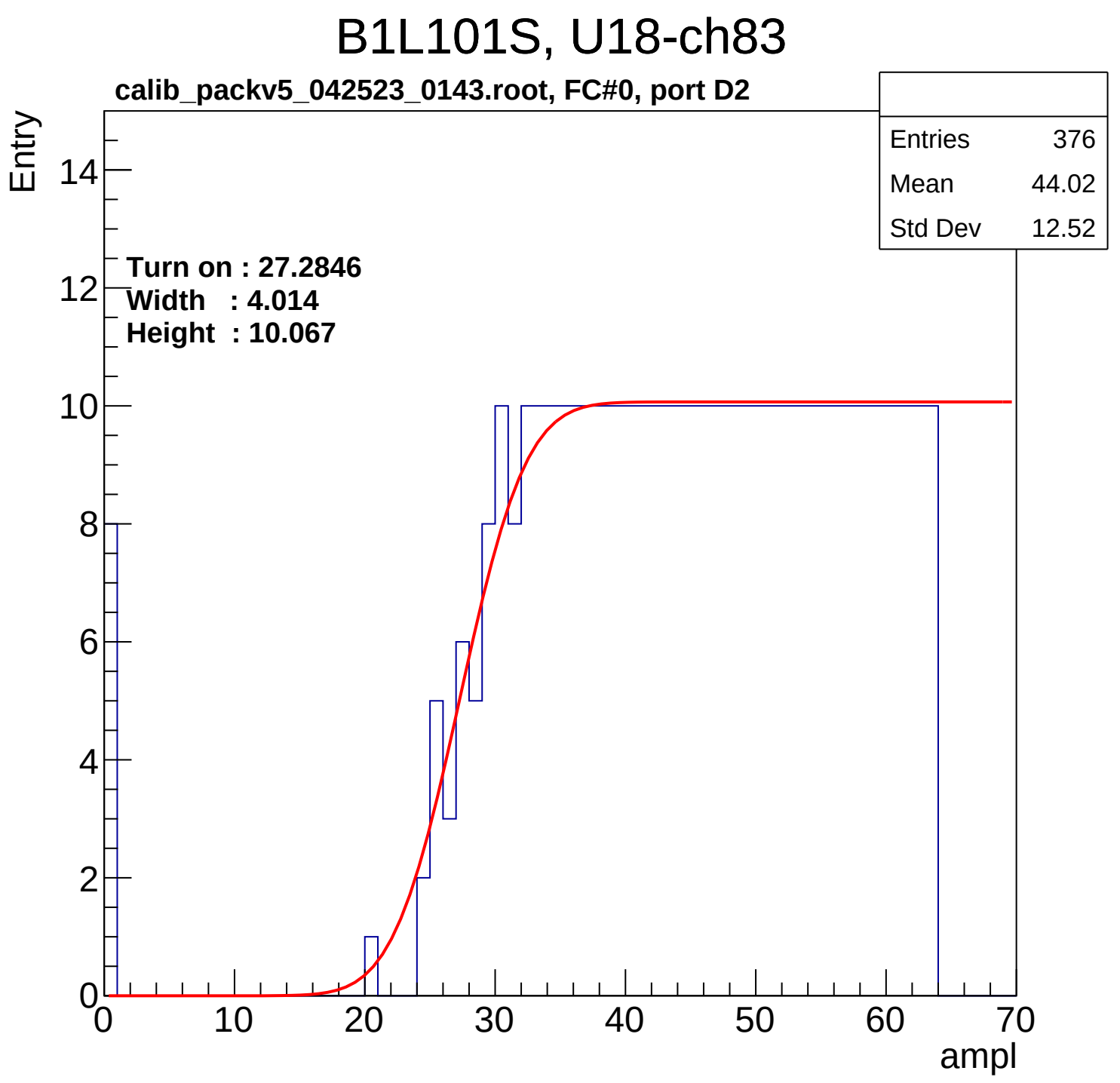
B1L101S, U18-ch83
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.02
Std Dev 12.52
Turn on : 27.2846
Width : 4.014
Height : 10.067
Entry
ampl
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8
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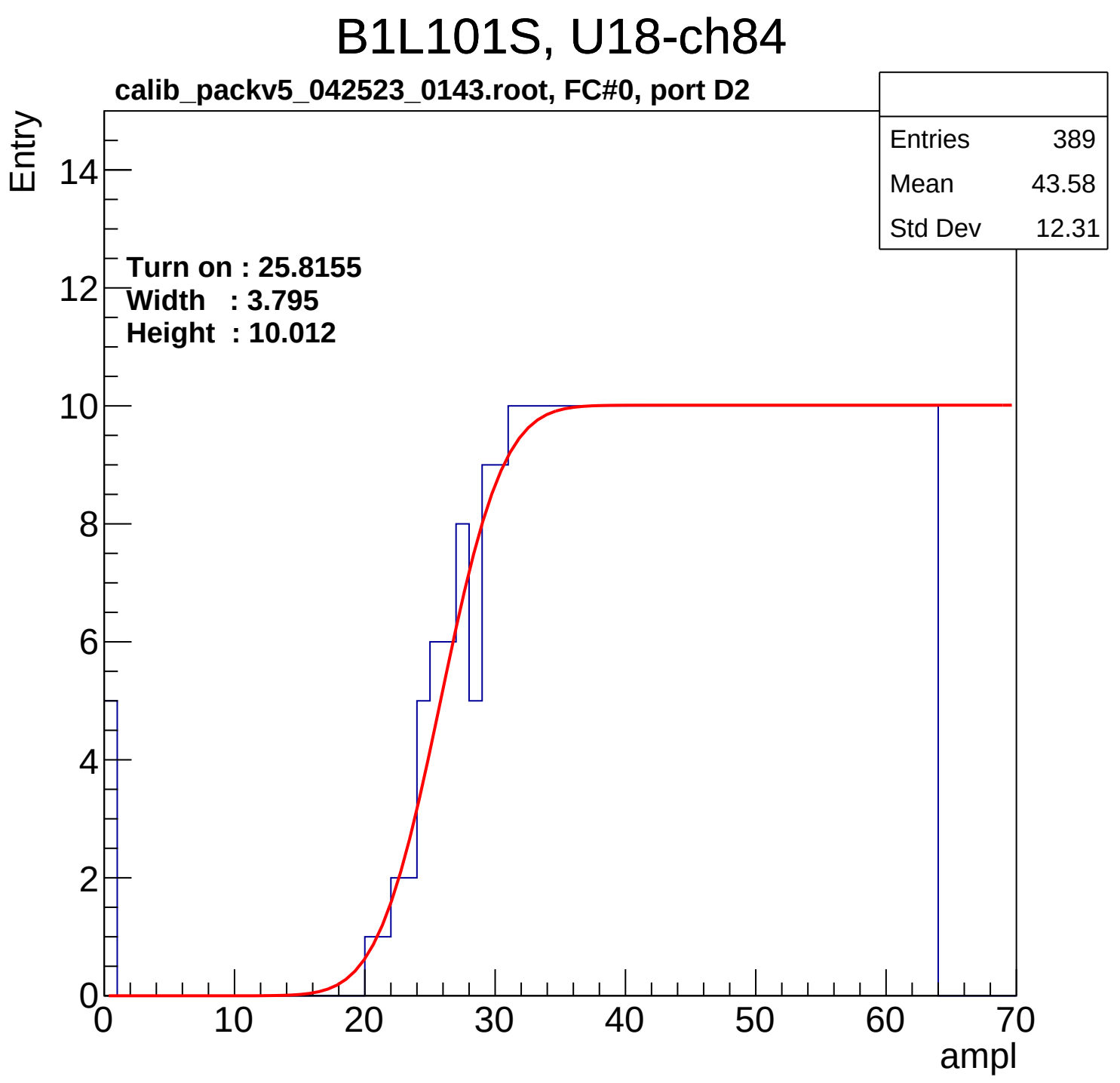
B1L101S, U18-ch84
calib_packv5_042523_0143.root, FC#0, port D2
Entries 389
Mean 43.58
Std Dev 12.31
Turn on : 25.8155
Width : 3.795
Height : 10.012
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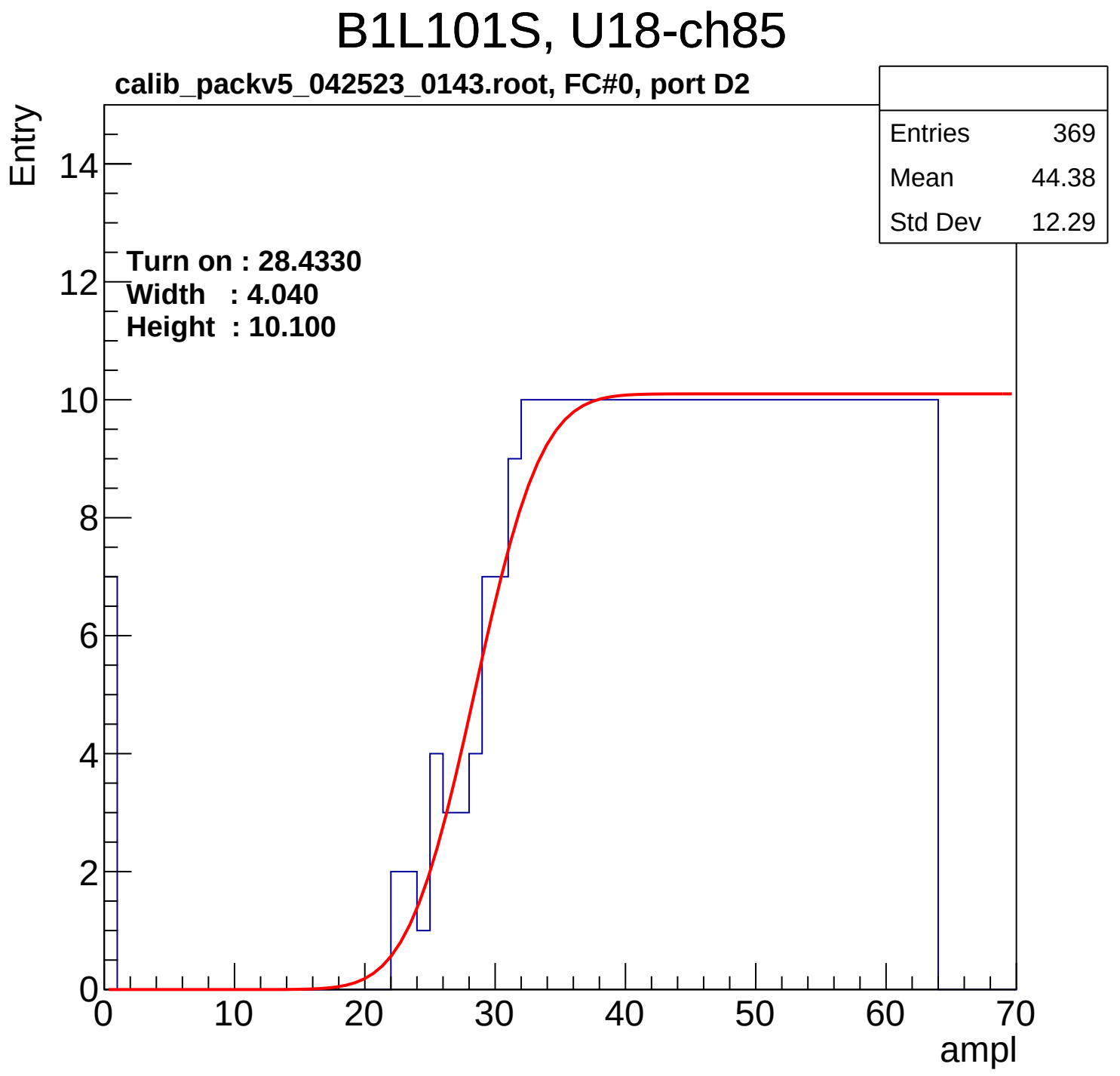
B1L101S, U18-ch85
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.38
Std Dev 12.29
Turn on : 28.4330
Width : 4.040
Height : 10.100
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ampl
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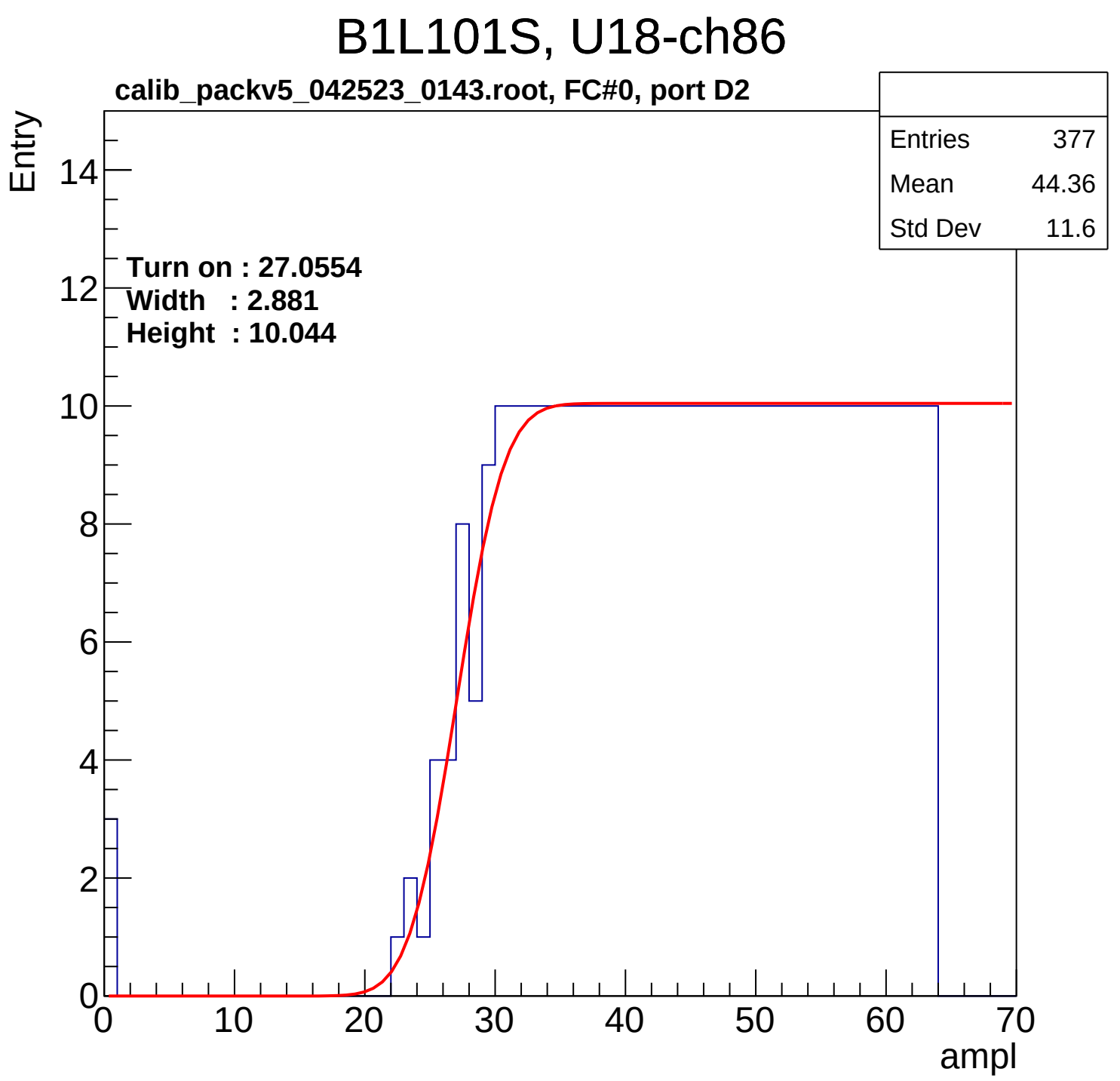
B1L101S, U18-ch86
calib_packv5_042523_0143.root, FC#0, port D2
Entries 377
Mean 44.36
Std Dev 11.6
Turn on : 27.0554
Width : 2.881
Height : 10.044
Entry
ampl
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4
6
8
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12
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10
20
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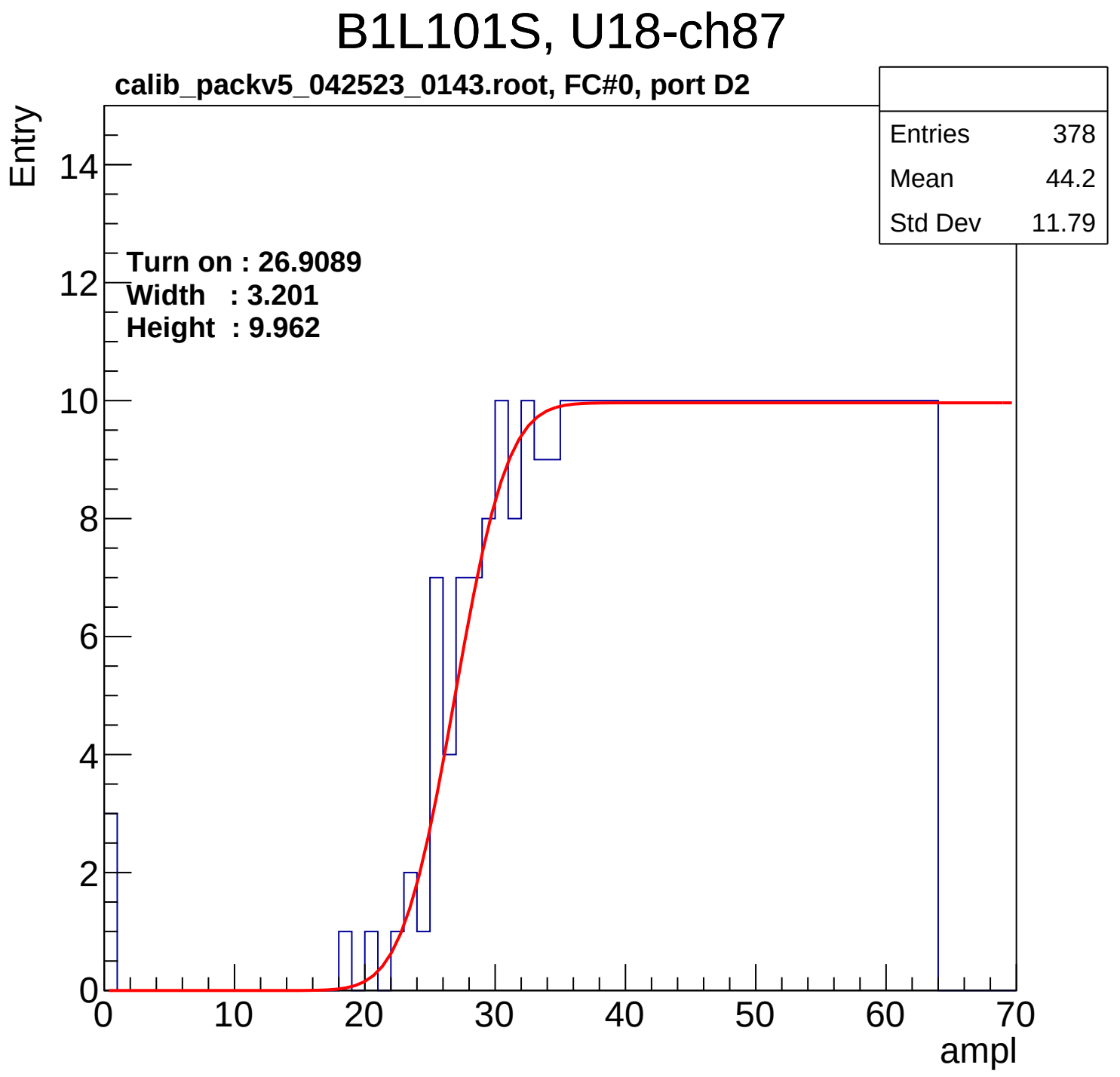
B1L101S, U18-ch87
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.2
Std Dev 11.79
Turn on : 26.9089
Width : 3.201
Height : 9.962
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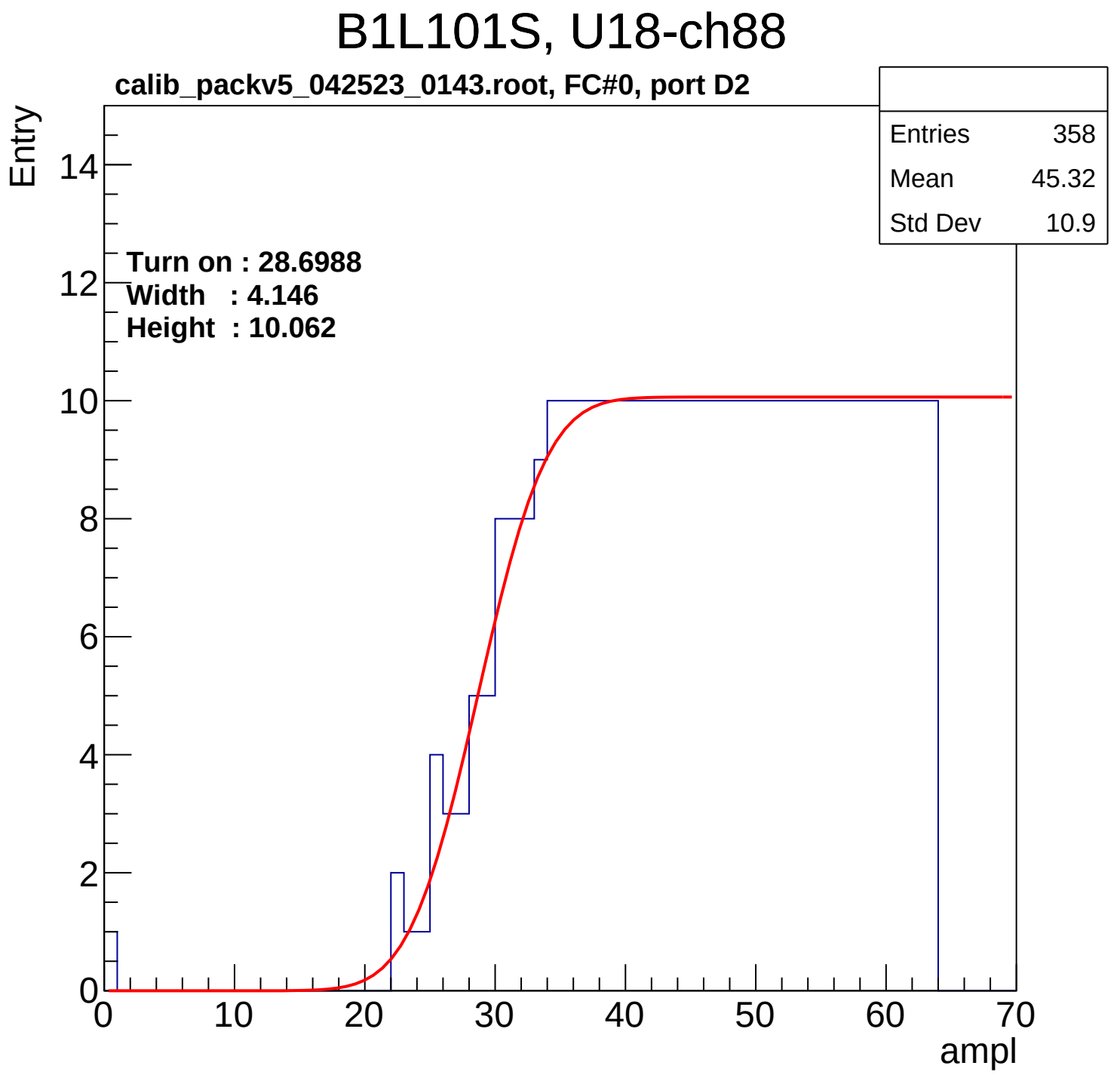
B1L101S, U18-ch88
calib_packv5_042523_0143.root, FC#0, port D2
Entries 358
Mean 45.32
Std Dev 10.9
Turn on : 28.6988
Width : 4.146
Height : 10.062
Entry
ampl
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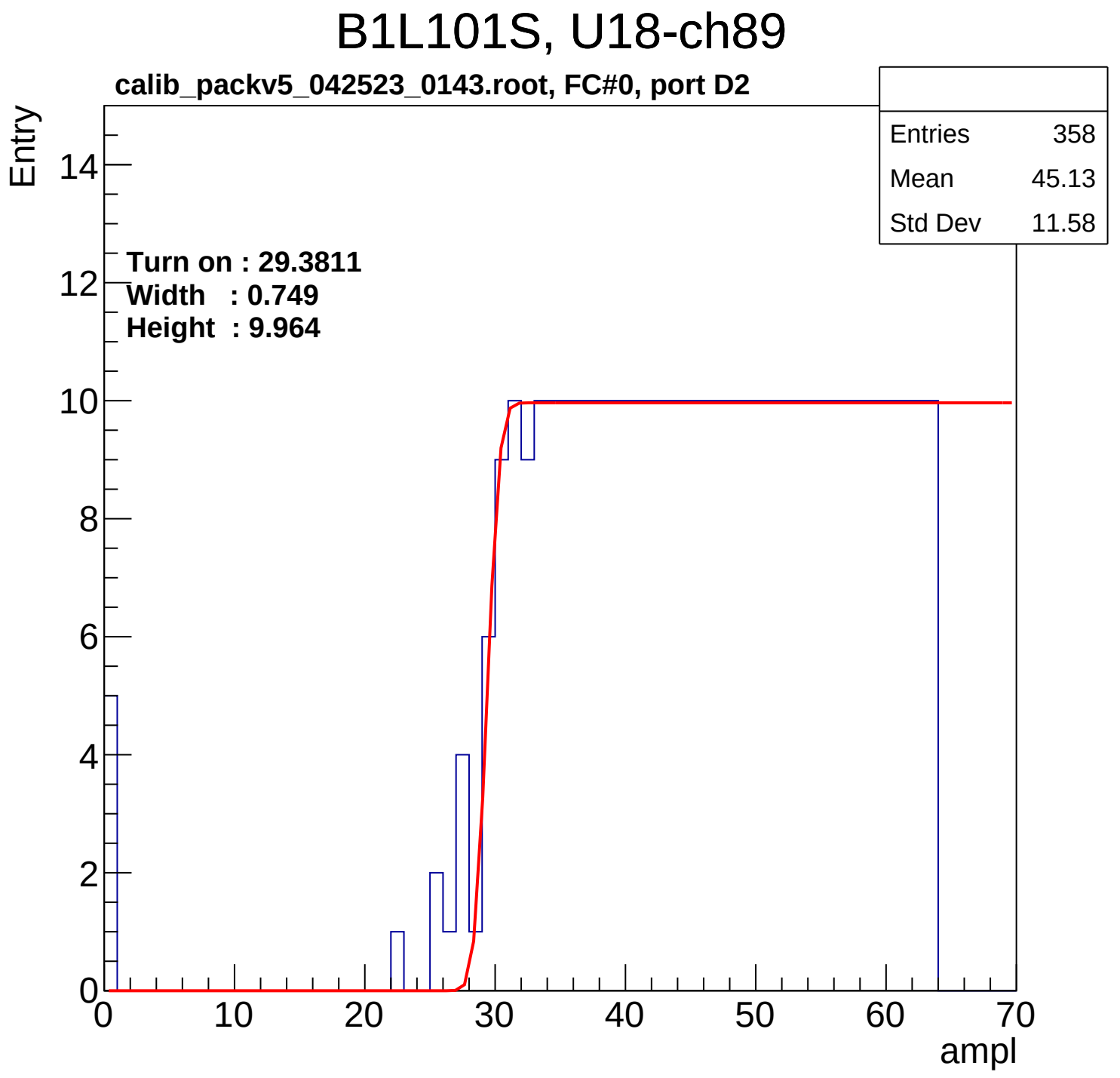
B1L101S, U18-ch89
calib_packv5_042523_0143.root, FC#0, port D2
Entries 358
Mean 45.13
Std Dev 11.58
Turn on : 29.3811
Width : 0.749
Height : 9.964
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ampl
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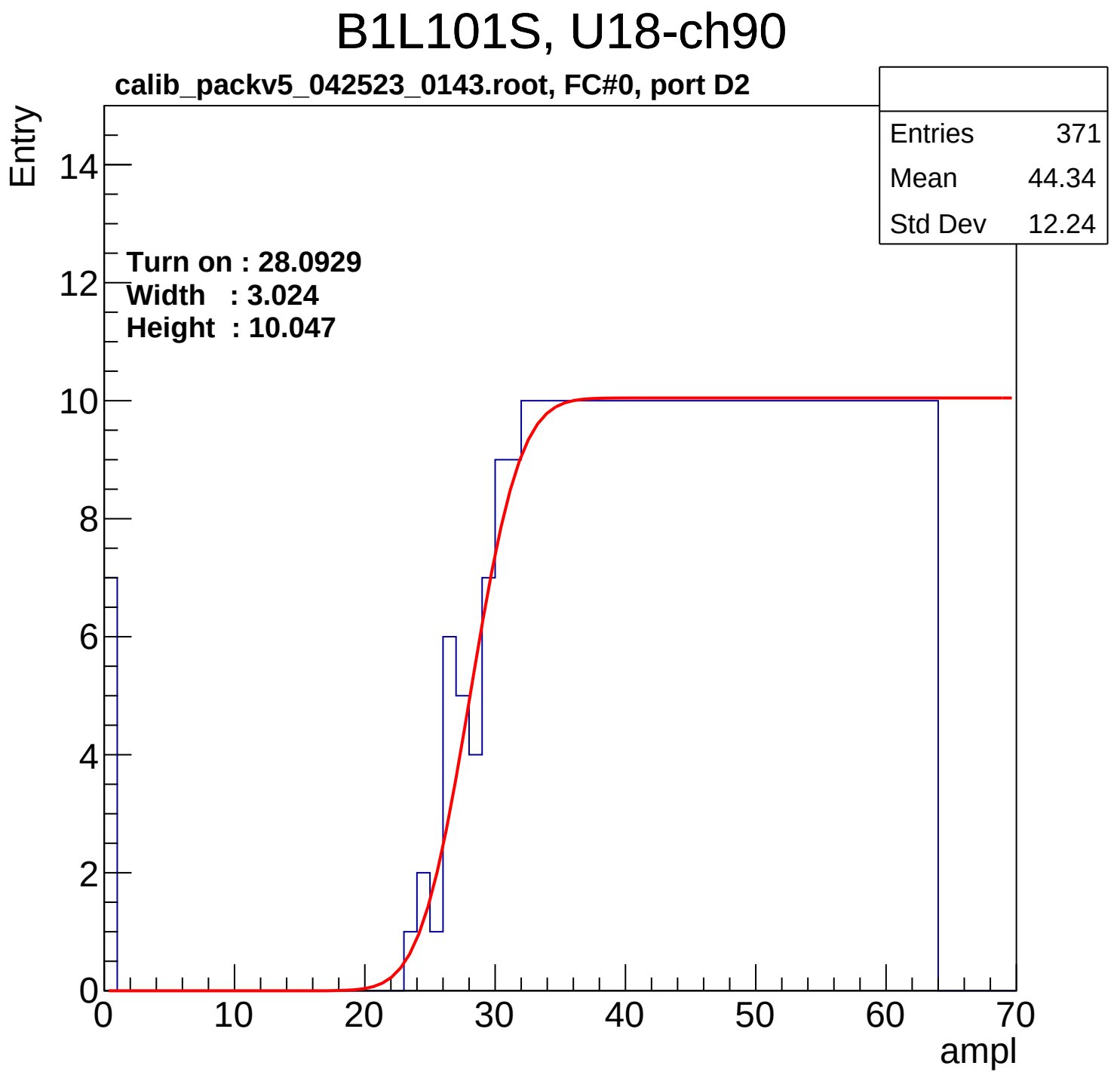
B1L101S, U18-ch90
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.34
Std Dev 12.24
Turn on : 28.0929
Width : 3.024
Height : 10.047
Entry
ampl
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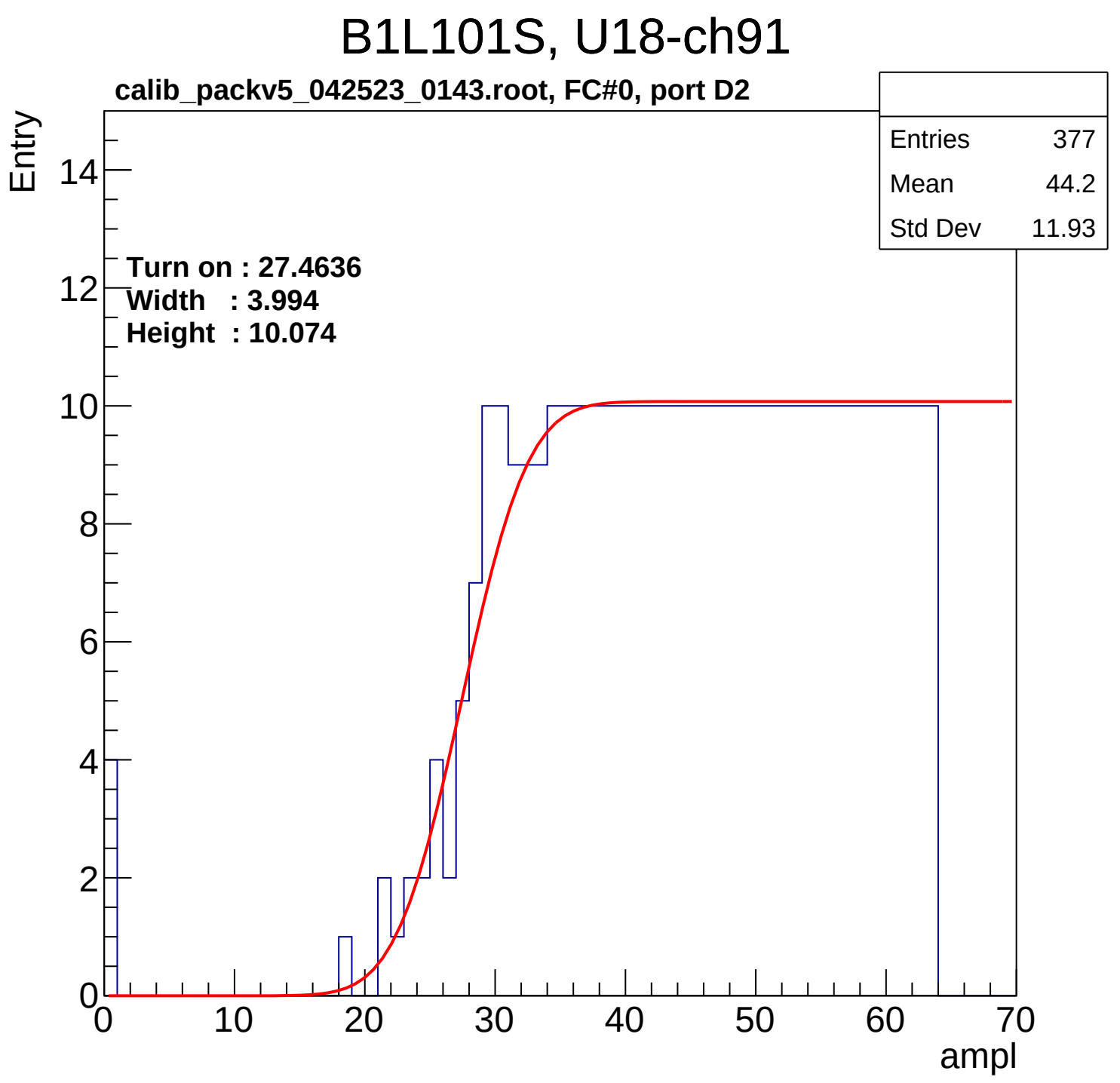
B1L101S, U18-ch91
calib_packv5_042523_0143.root, FC#0, port D2
Entries 377
Mean 44.2
Std Dev 11.93
Turn on : 27.4636
Width : 3.994
Height : 10.074
Entry
ampl
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2
4
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8
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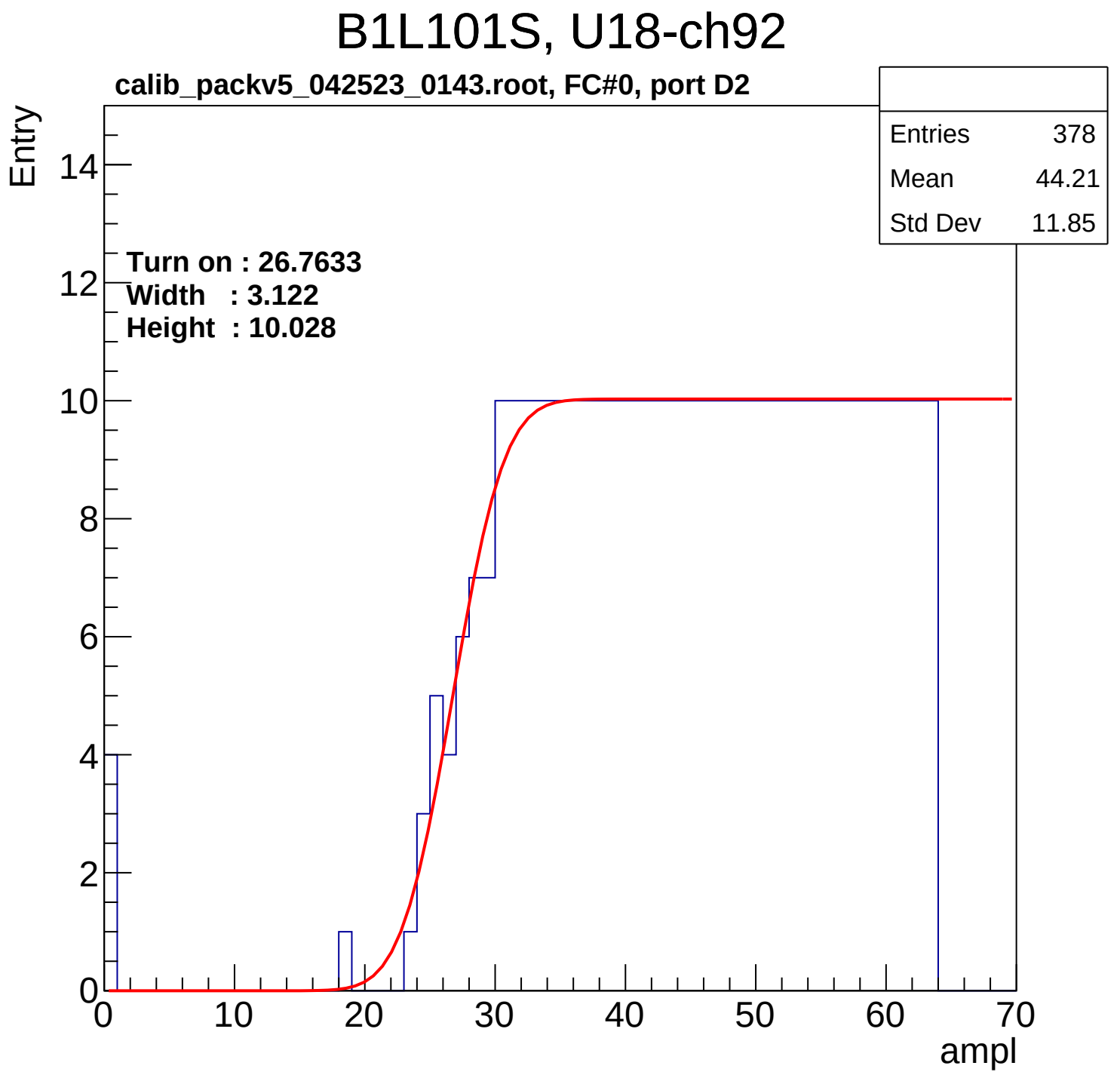
B1L101S, U18-ch92
calib_packv5_042523_0143.root, FC#0, port D2
Entries 378
Mean 44.21
Std Dev 11.85
Turn on : 26.7633
Width : 3.122
Height : 10.028
Entry
ampl
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2
4
6
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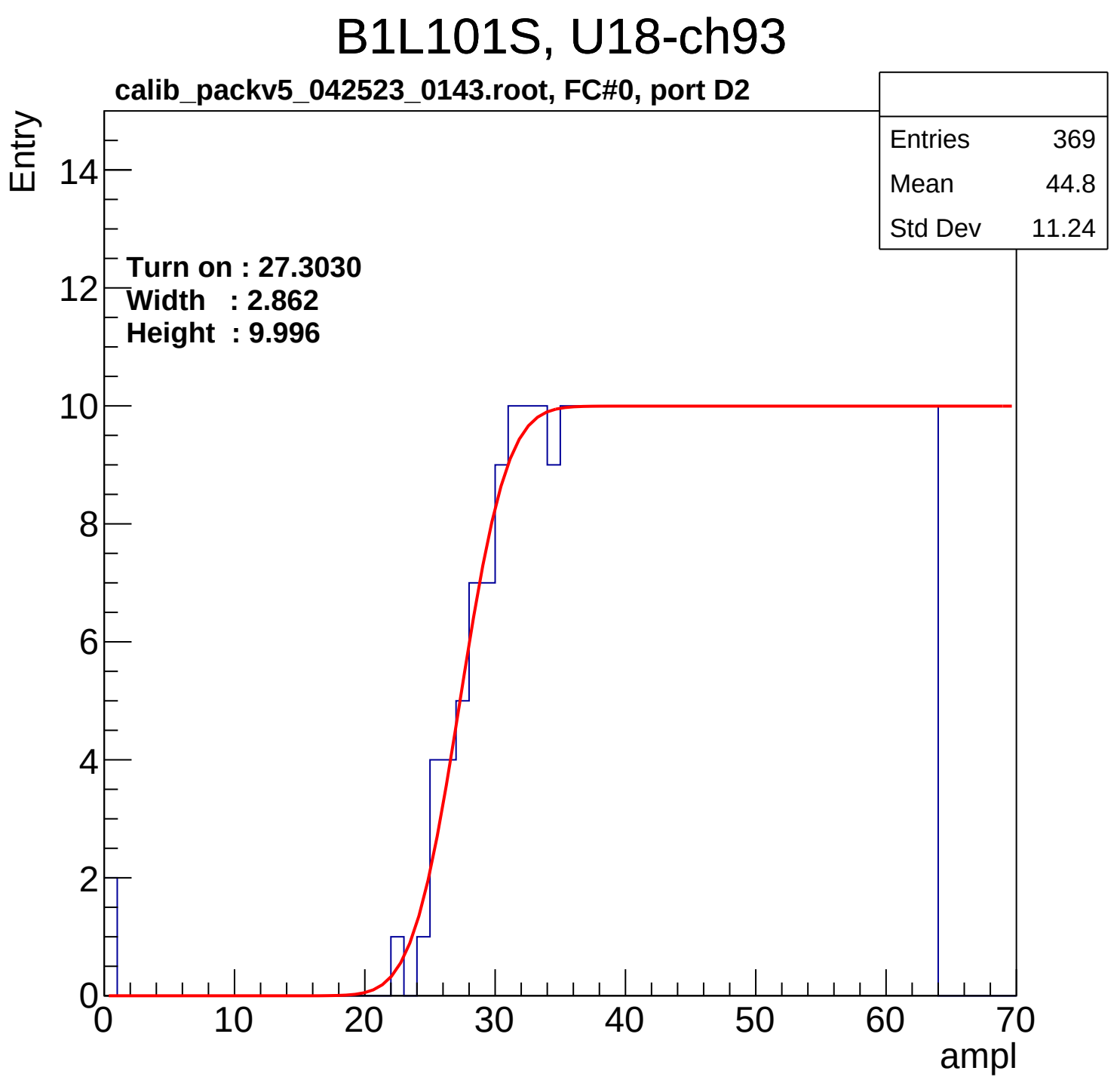
B1L101S, U18-ch93
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.8
Std Dev 11.24
Turn on : 27.3030
Width : 2.862
Height : 9.996
Entry
ampl
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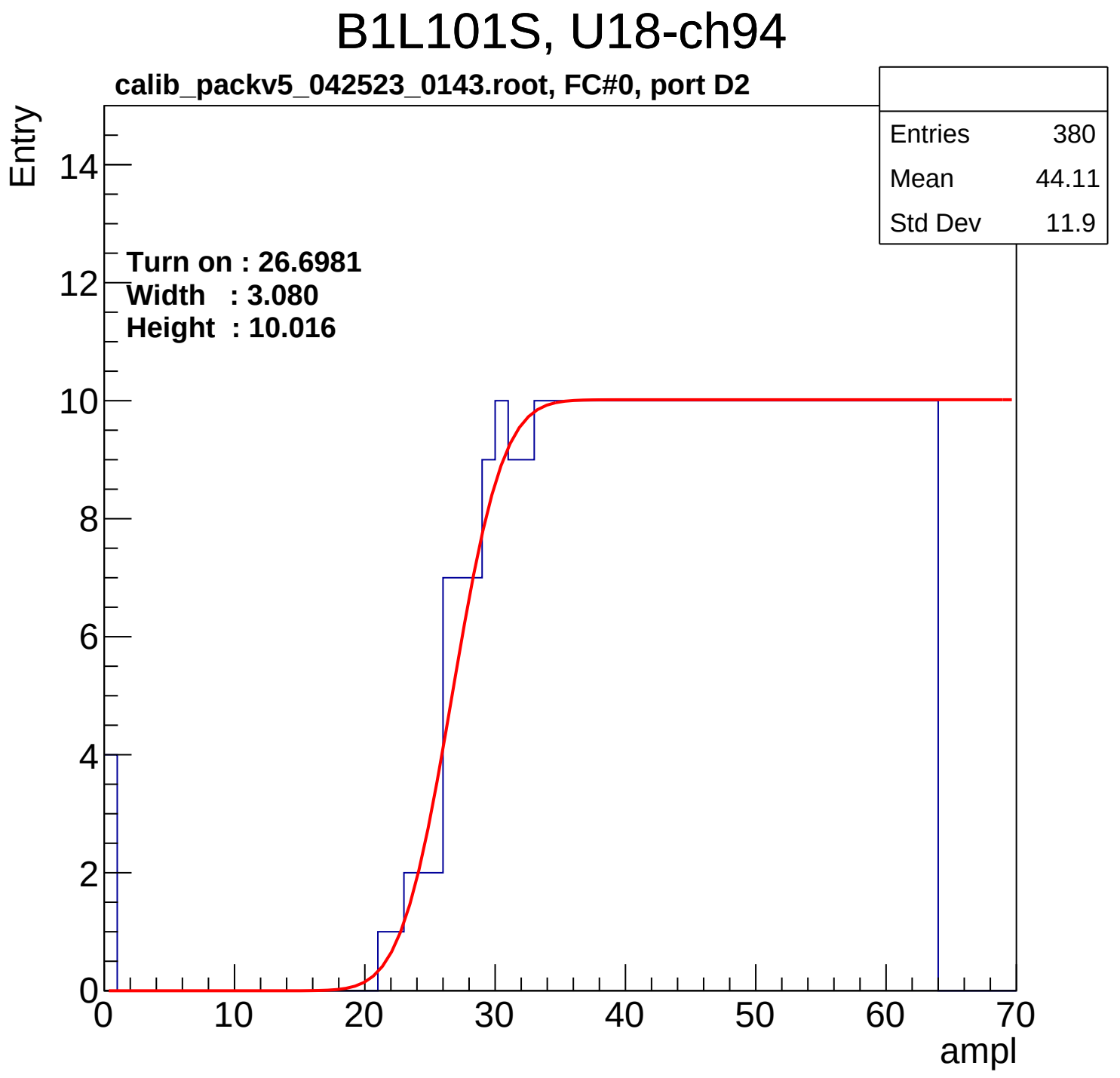
B1L101S, U18-ch94
calib_packv5_042523_0143.root, FC#0, port D2
Entries 380
Mean 44.11
Std Dev 11.9
Turn on : 26.6981
Width : 3.080
Height : 10.016
Entry
ampl
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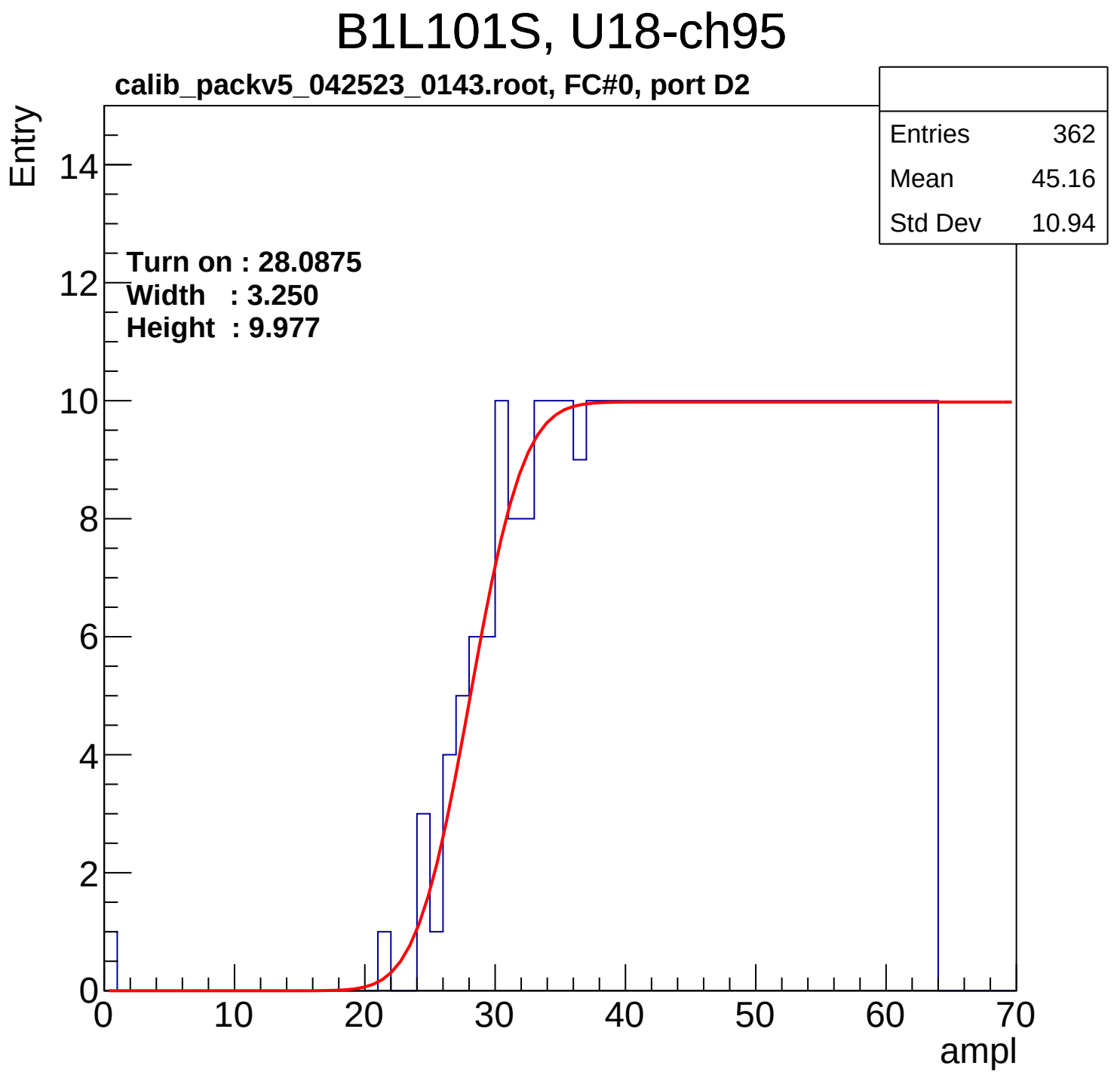
B1L101S, U18-ch95
calib_packv5_042523_0143.root, FC#0, port D2
Entries 362
Mean 45.16
Std Dev 10.94
Turn on : 28.0875
Width : 3.250
Height : 9.977
Entry
ampl
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6
8
10
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60
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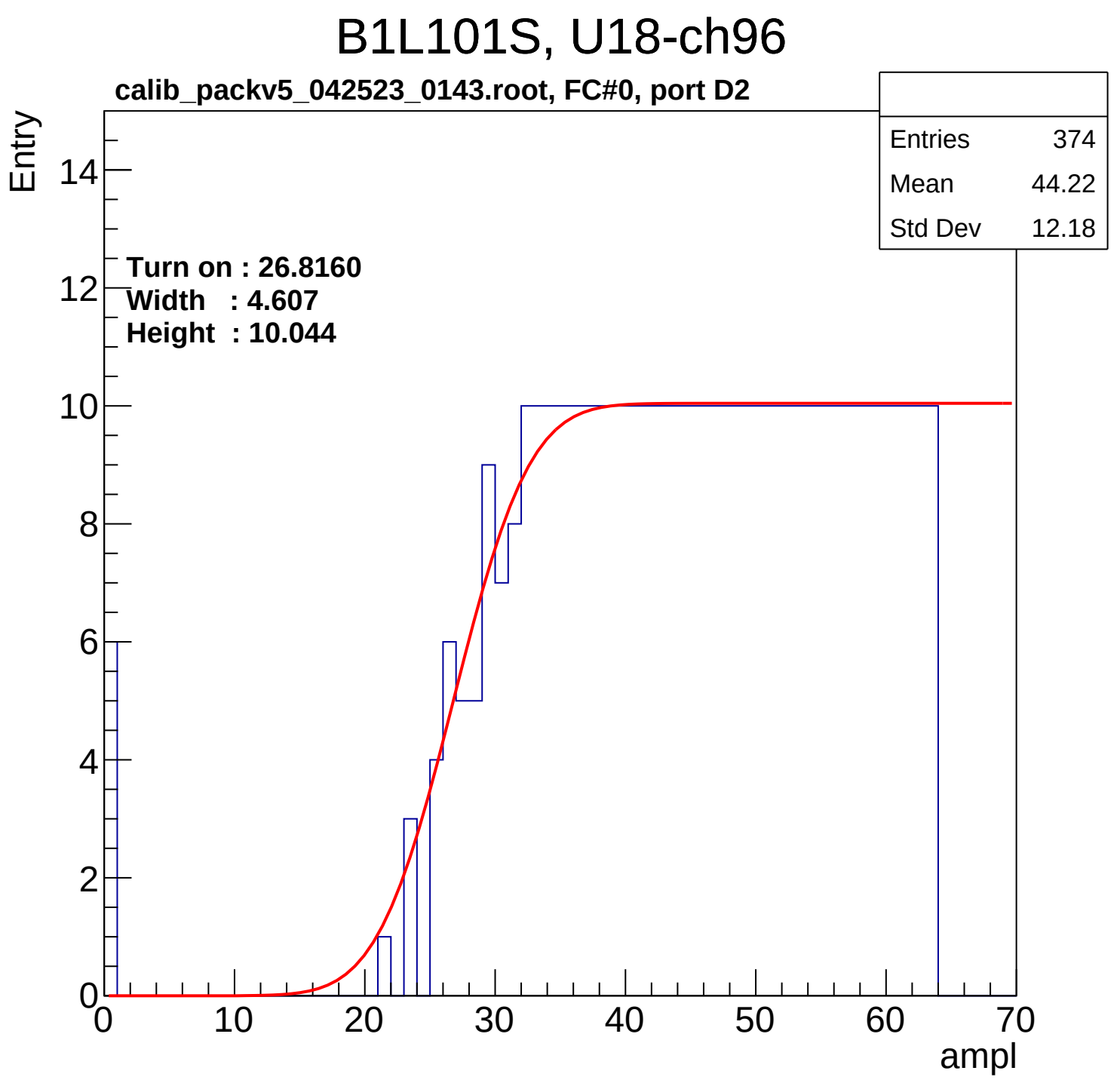
B1L101S, U18-ch96
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.22
Std Dev 12.18
Turn on : 26.8160
Width : 4.607
Height : 10.044
Entry
ampl
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6
8
10
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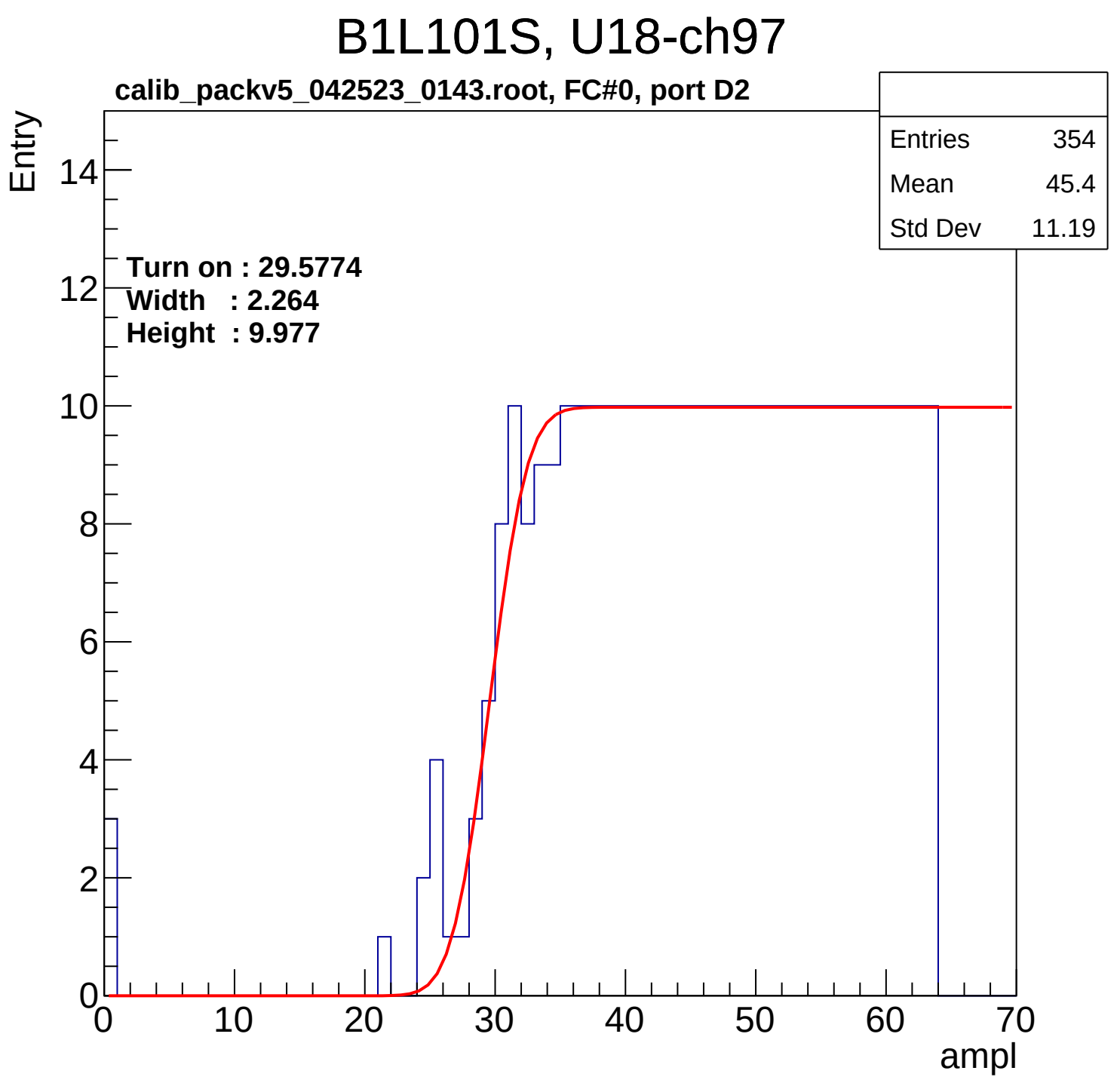
B1L101S, U18-ch97
calib_packv5_042523_0143.root, FC#0, port D2
Entries 354
Mean 45.4
Std Dev 11.19
Turn on : 29.5774
Width : 2.264
Height : 9.977
Entry
ampl
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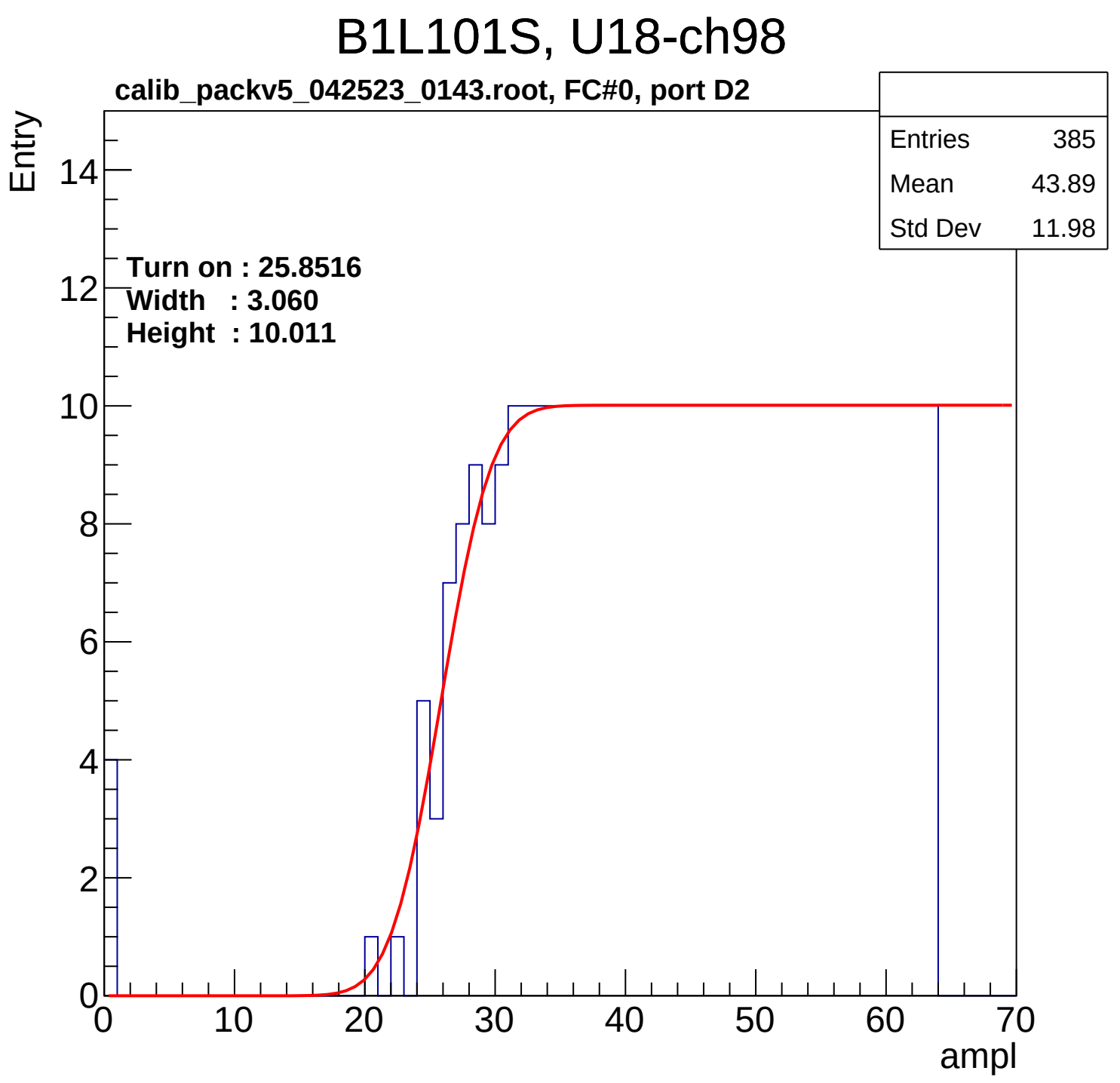
B1L101S, U18-ch98
calib_packv5_042523_0143.root, FC#0, port D2
Entries 385
Mean 43.89
Std Dev 11.98
Turn on : 25.8516
Width : 3.060
Height : 10.011
Entry
ampl
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8
10
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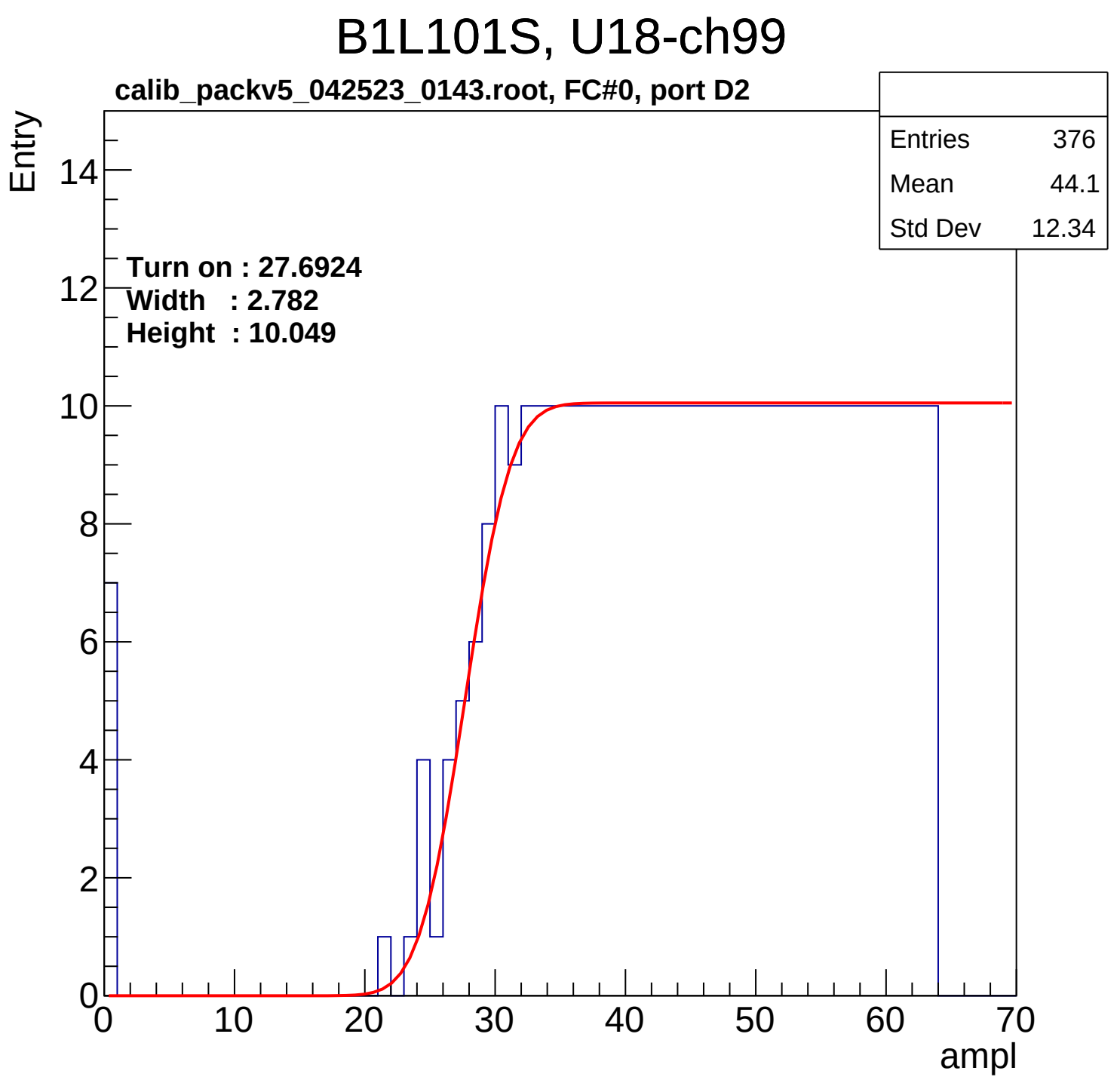
B1L101S, U18-ch99
calib_packv5_042523_0143.root, FC#0, port D2
Entries 376
Mean 44.1
Std Dev 12.34
Turn on : 27.6924
Width : 2.782
Height : 10.049
Entry
ampl
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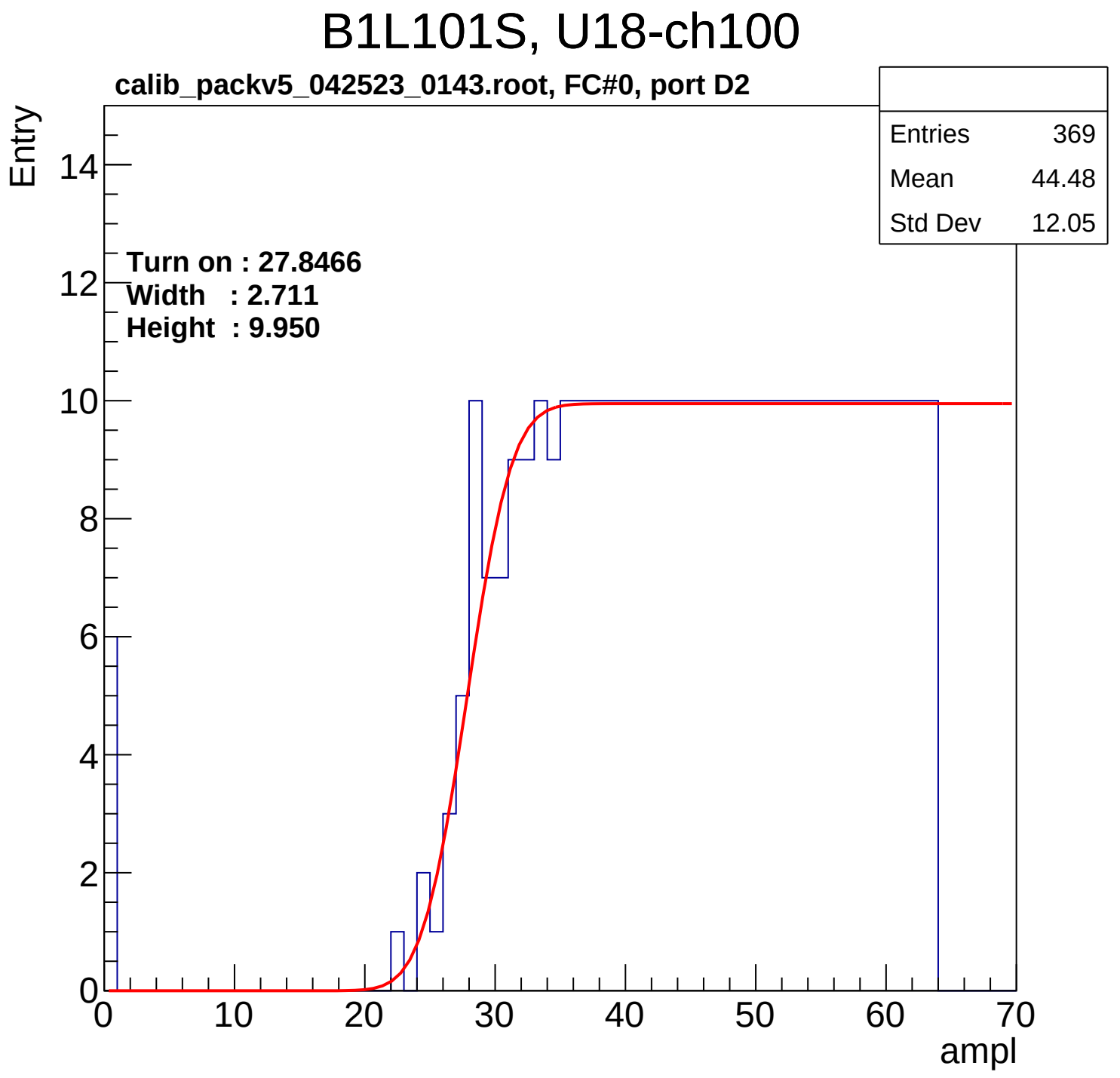
B1L101S, U18-ch100
calib_packv5_042523_0143.root, FC#0, port D2
Entries 369
Mean 44.48
Std Dev 12.05
Turn on : 27.8466
Width : 2.711
Height : 9.950
Entry
ampl
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6
8
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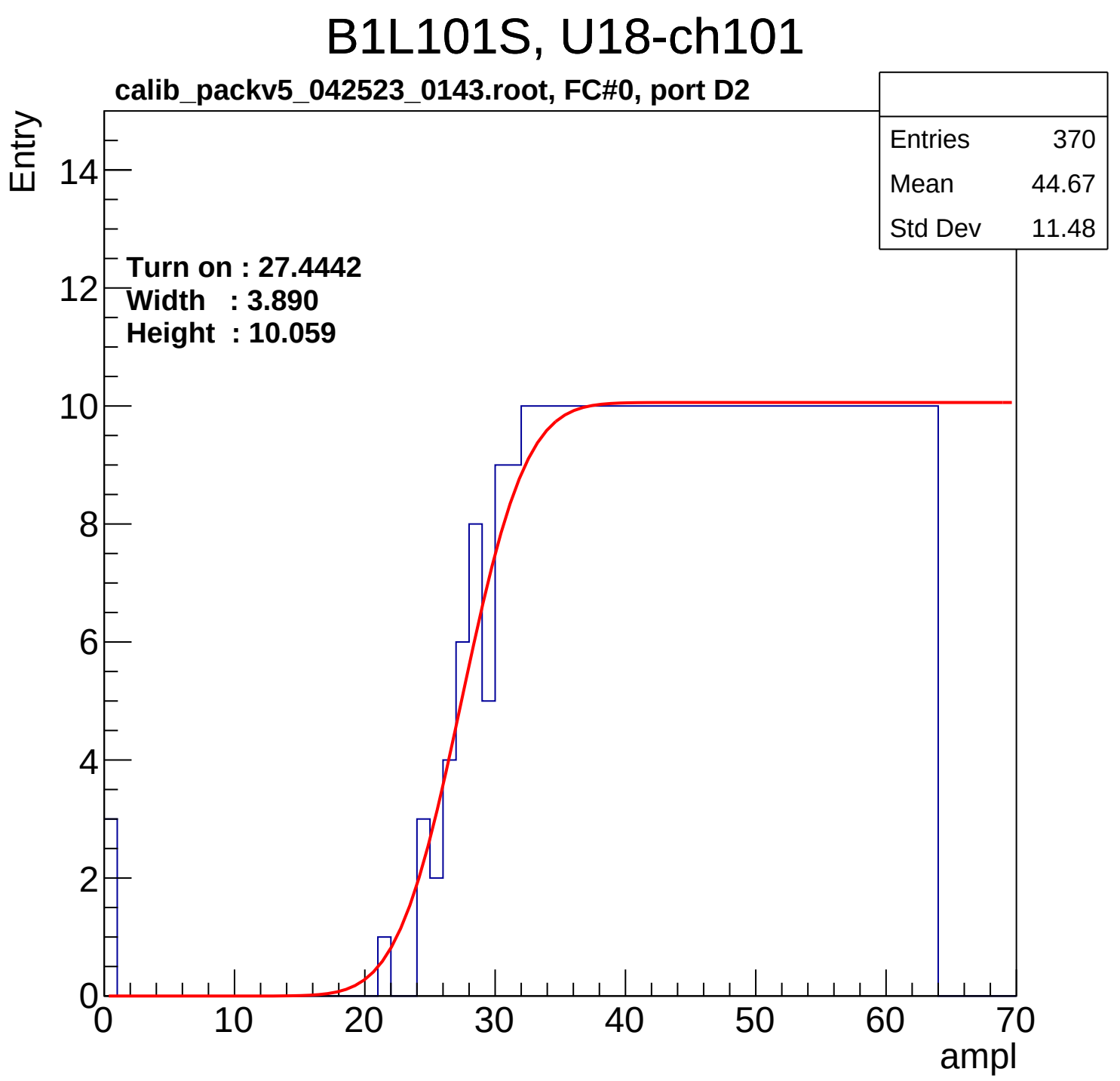
B1L101S, U18-ch101
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.67
Std Dev 11.48
Turn on : 27.4442
Width : 3.890
Height : 10.059
Entry
ampl
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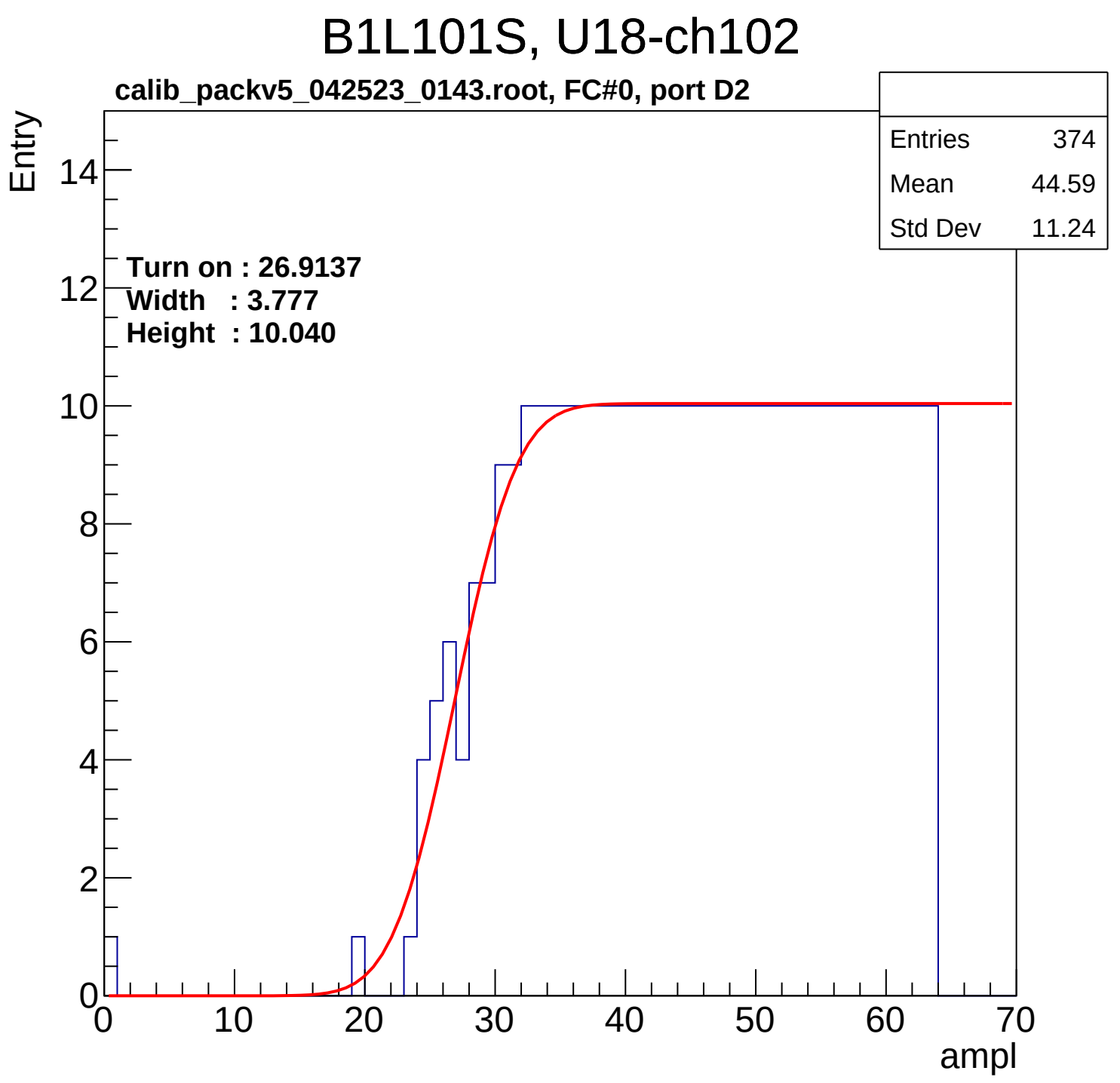
B1L101S, U18-ch102
calib_packv5_042523_0143.root, FC#0, port D2
Entries 374
Mean 44.59
Std Dev 11.24
Turn on : 26.9137
Width : 3.777
Height : 10.040
Entry
ampl
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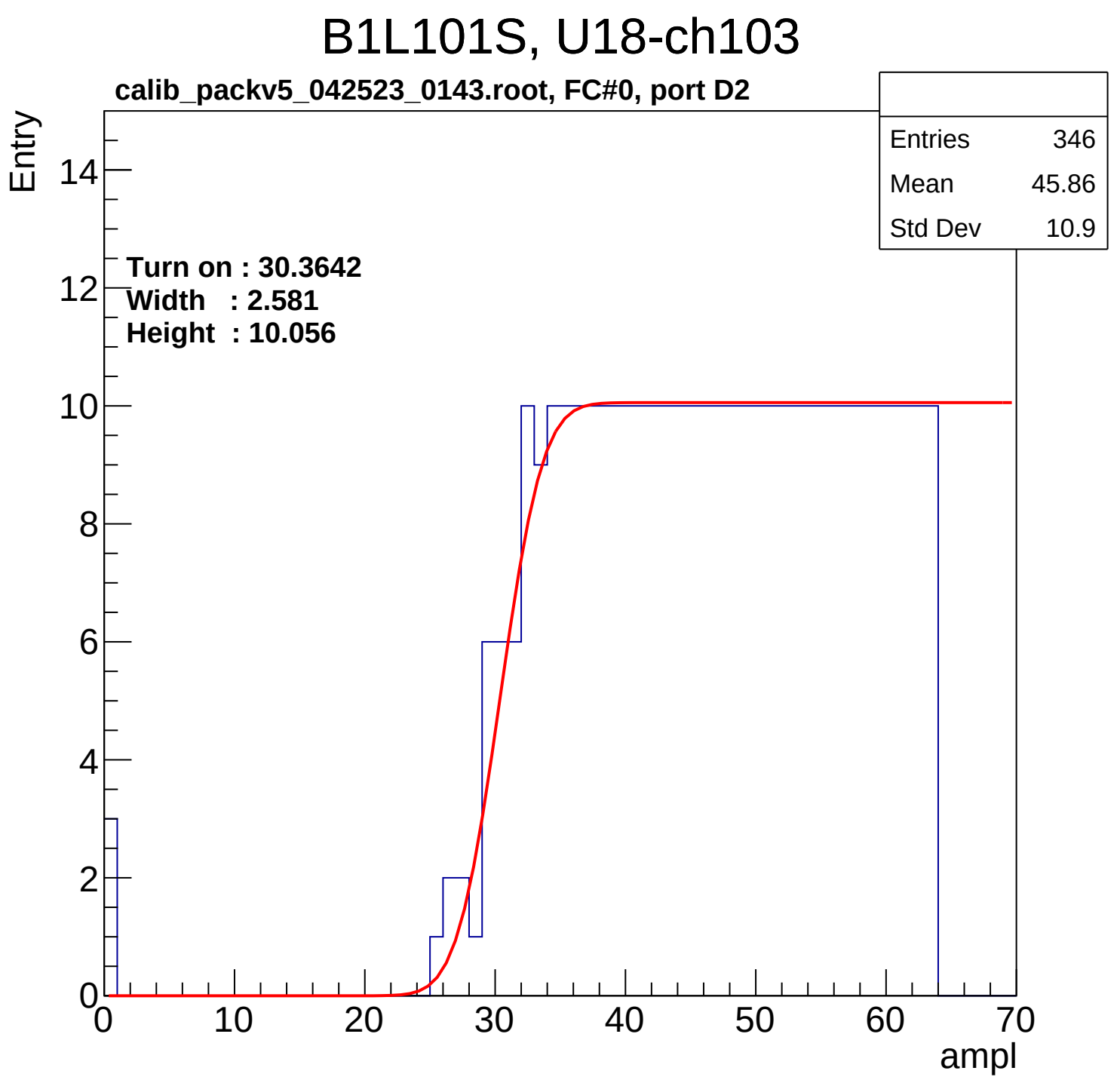
B1L101S, U18-ch103
calib_packv5_042523_0143.root, FC#0, port D2
Entries 346
Mean 45.86
Std Dev 10.9
Turn on : 30.3642
Width : 2.581
Height : 10.056
Entry
ampl
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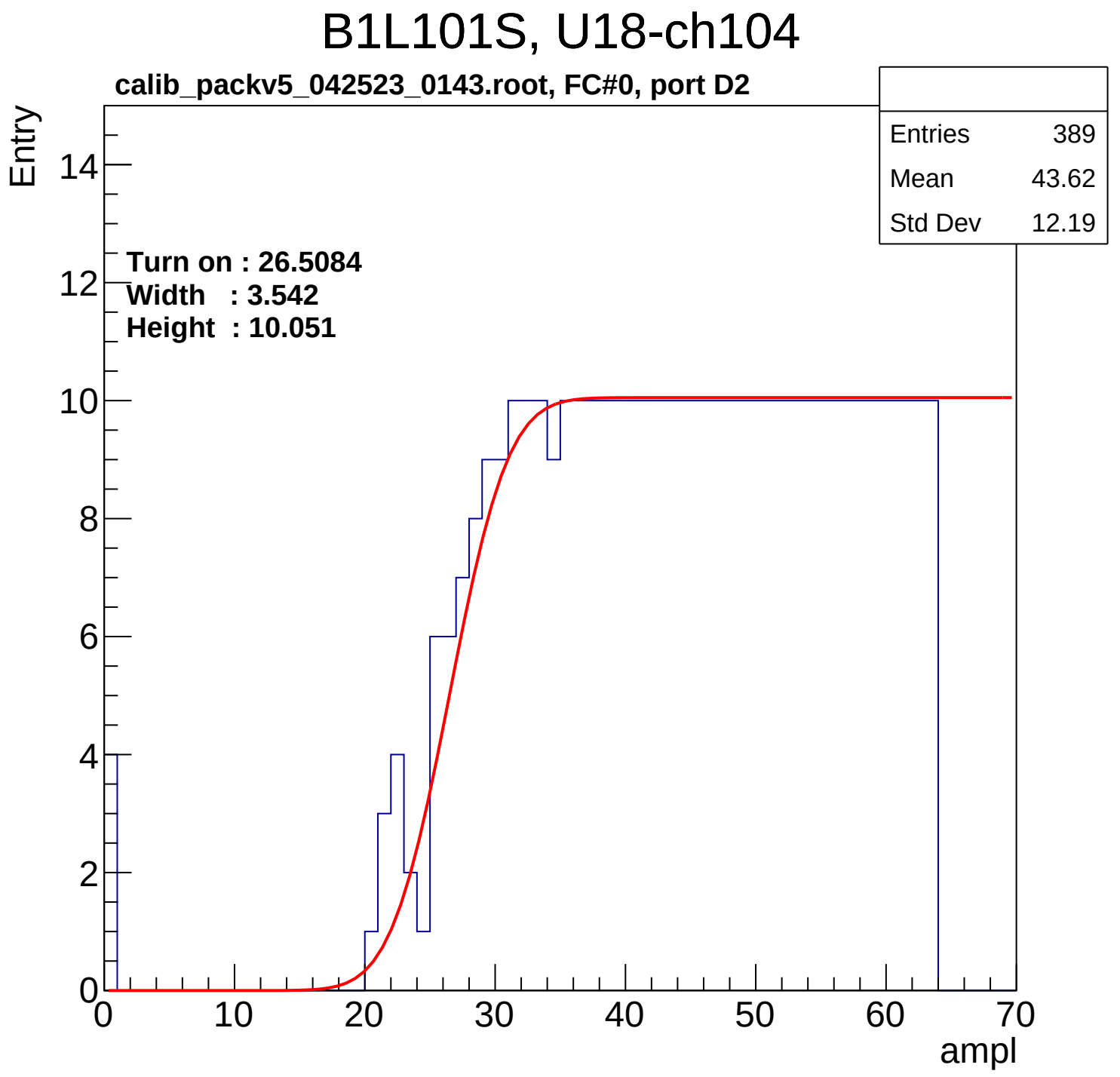
B1L101S, U18-ch104
calib_packv5_042523_0143.root, FC#0, port D2
Entries 389
Mean 43.62
Std Dev 12.19
Turn on : 26.5084
Width : 3.542
Height : 10.051
Entry
ampl
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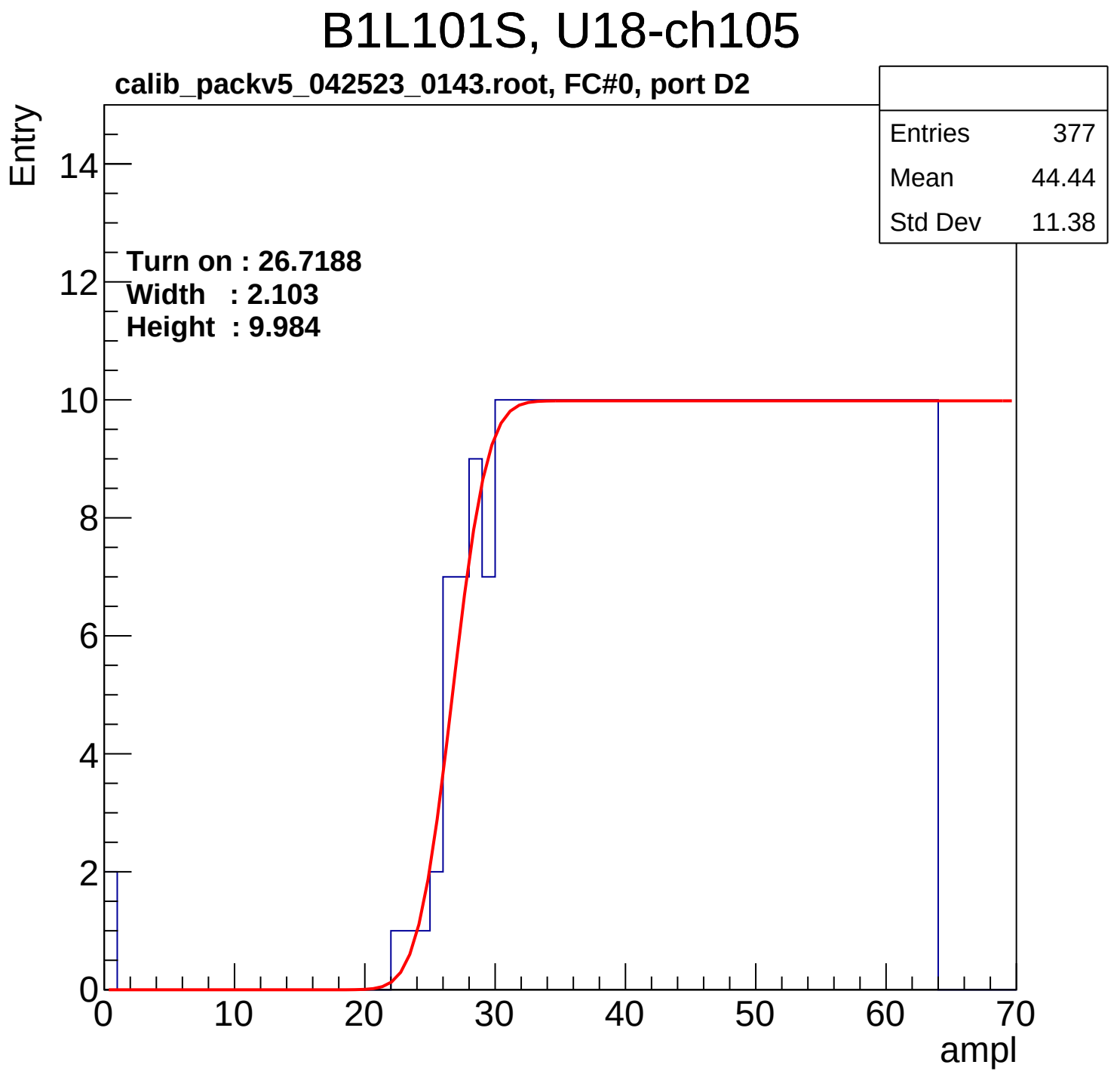
B1L101S, U18-ch105
calib_packv5_042523_0143.root, FC#0, port D2
Entries 377
Mean 44.44
Std Dev 11.38
Turn on : 26.7188
Width : 2.103
Height : 9.984
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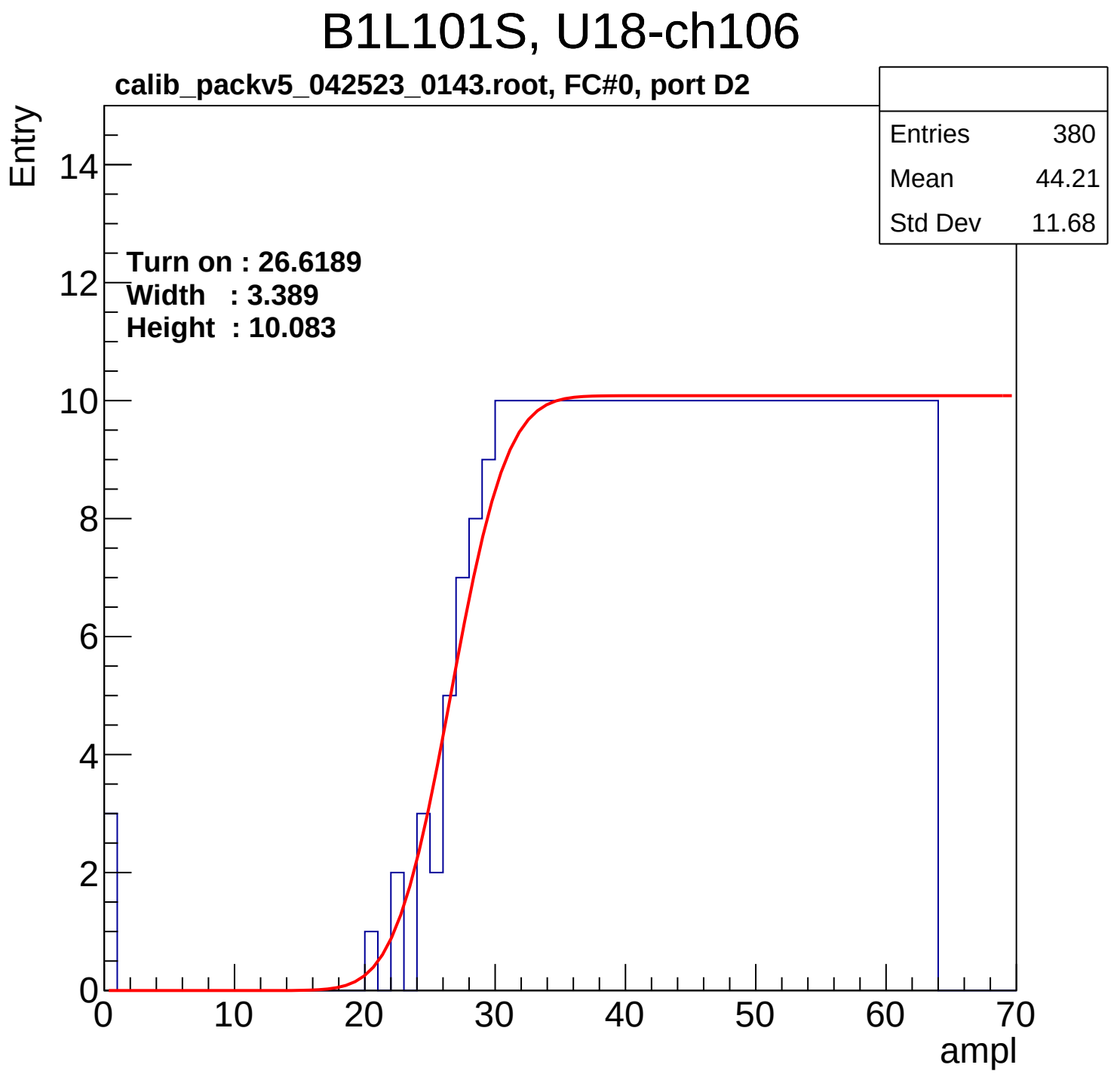
B1L101S, U18-ch106
calib_packv5_042523_0143.root, FC#0, port D2
Entries 380
Mean 44.21
Std Dev 11.68
Turn on : 26.6189
Width : 3.389
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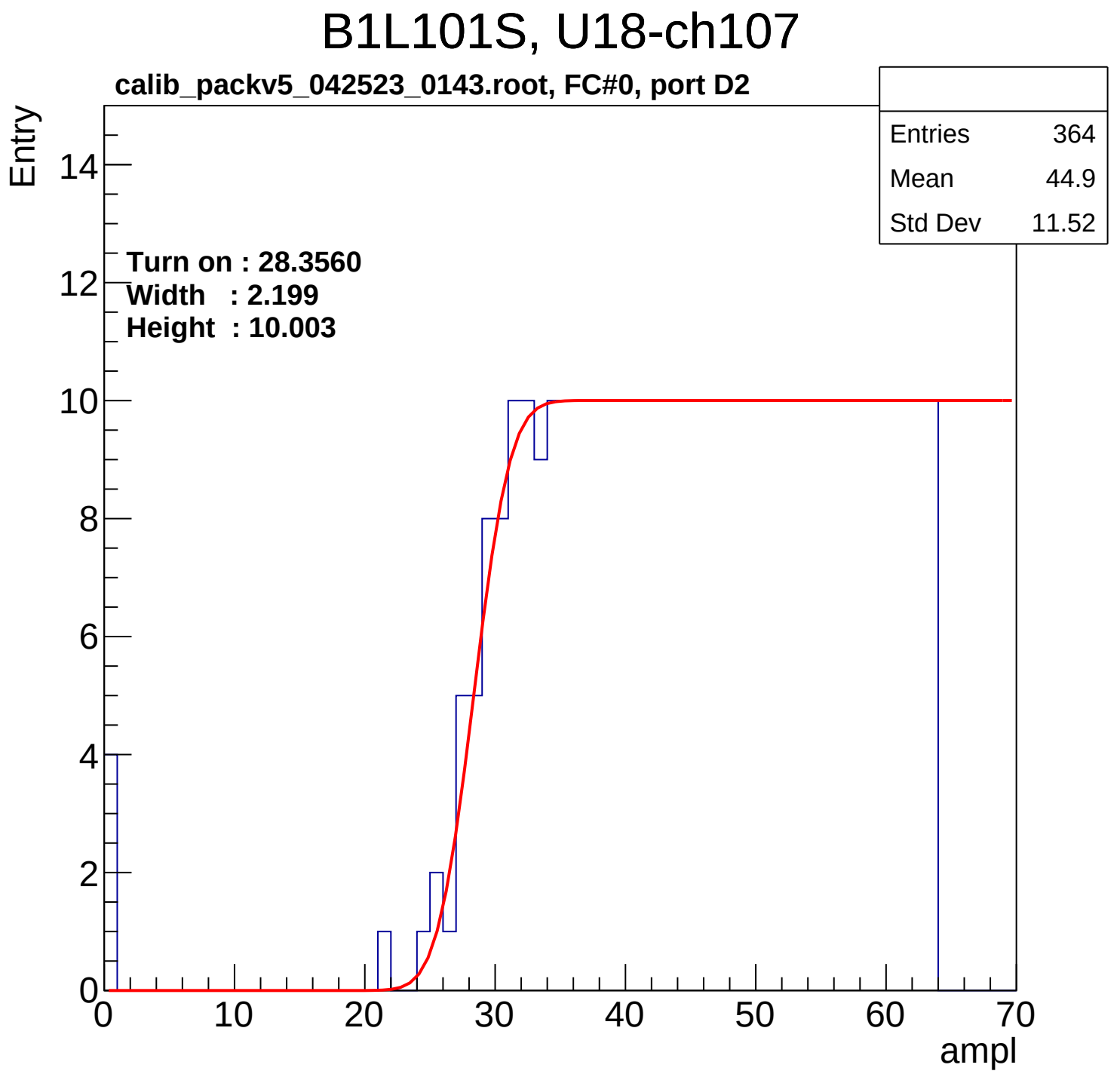
B1L101S, U18-ch107
calib_packv5_042523_0143.root, FC#0, port D2
Entries 364
Mean 44.9
Std Dev 11.52
Turn on : 28.3560
Width : 2.199
Height : 10.003
Entry
ampl
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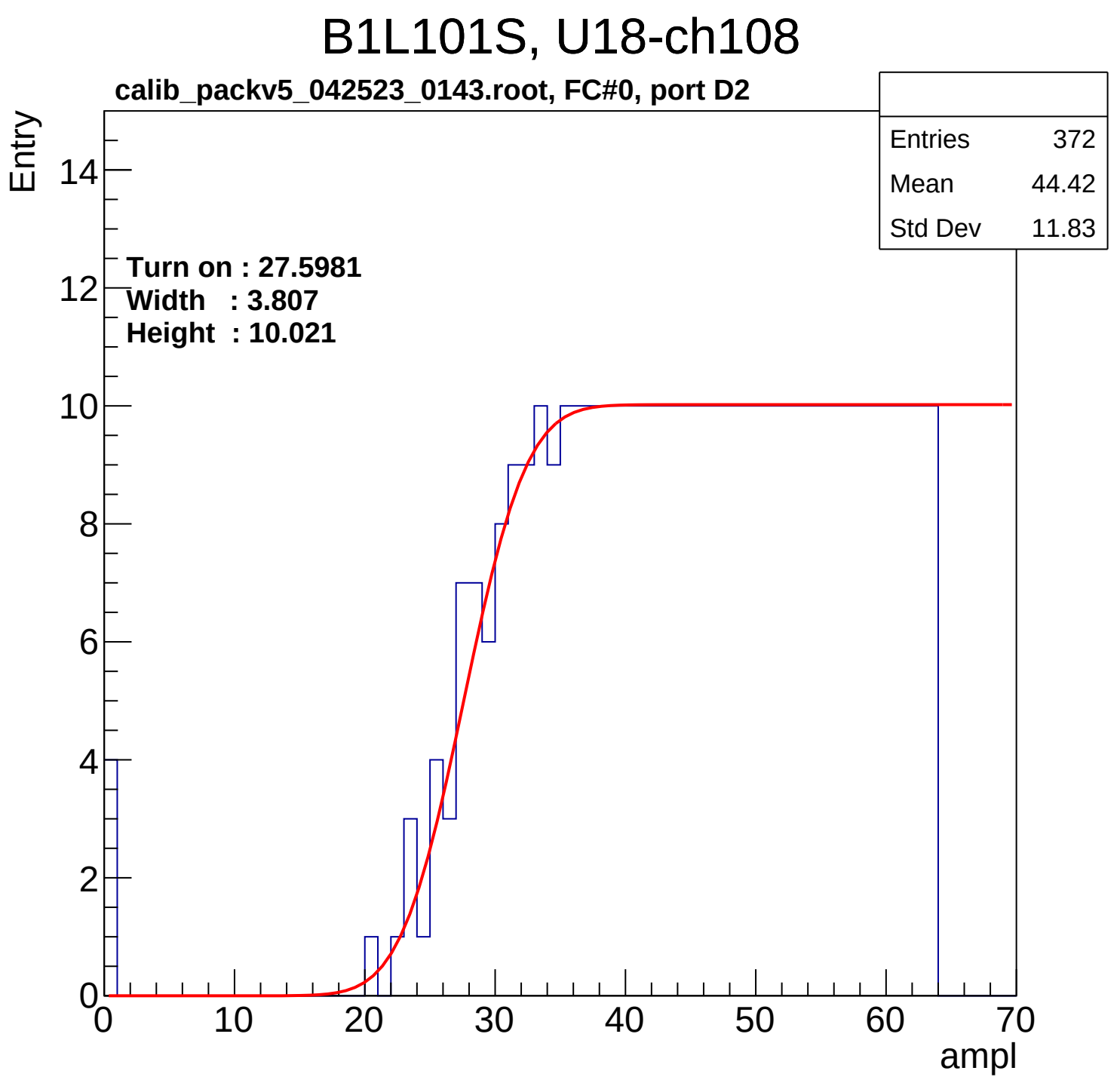
B1L101S, U18-ch108
calib_packv5_042523_0143.root, FC#0, port D2
Entries 372
Mean 44.42
Std Dev 11.83
Turn on : 27.5981
Width : 3.807
Height : 10.021
Entry
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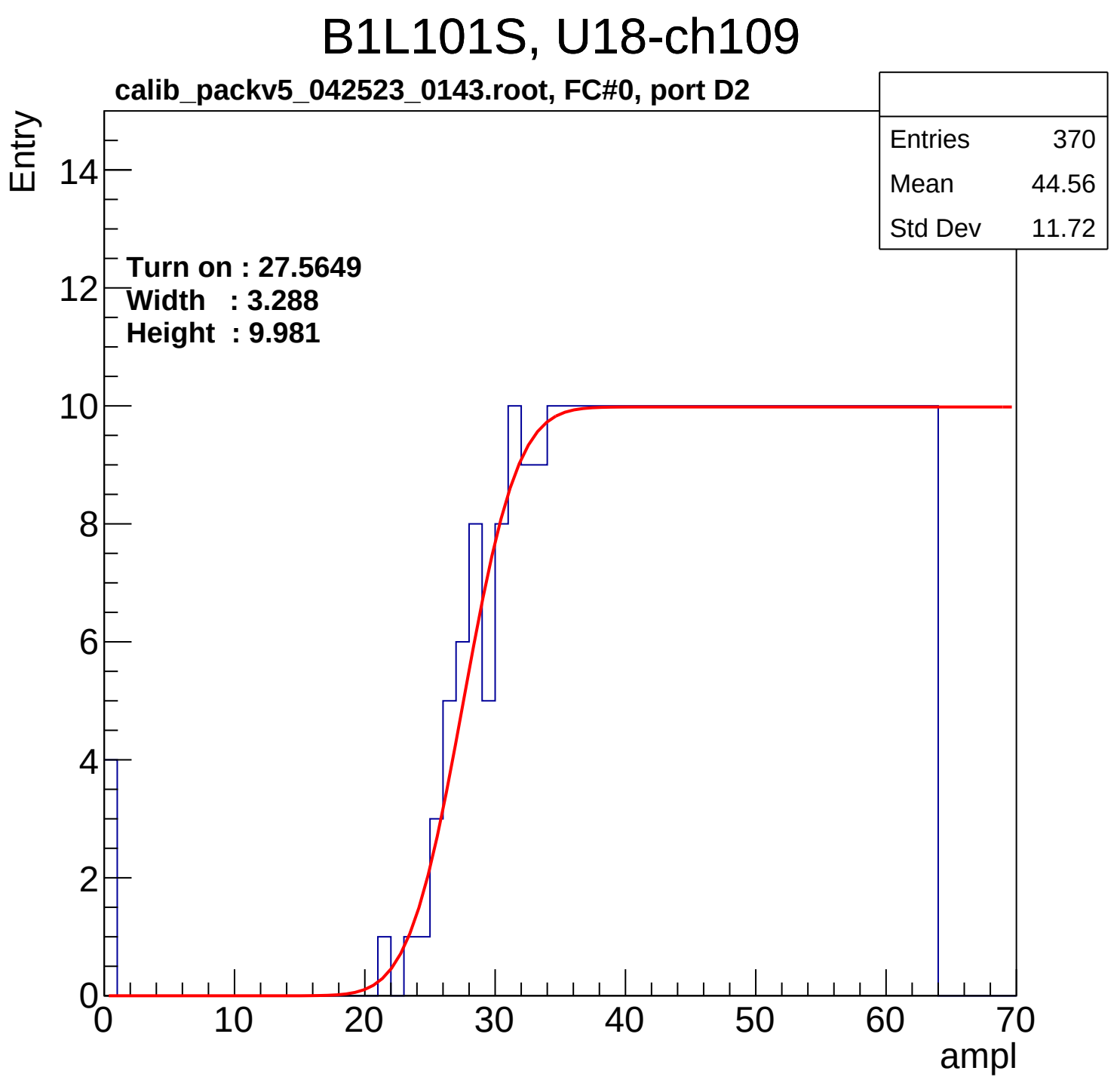
B1L101S, U18-ch109
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.56
Std Dev 11.72
Turn on : 27.5649
Width : 3.288
Height : 9.981
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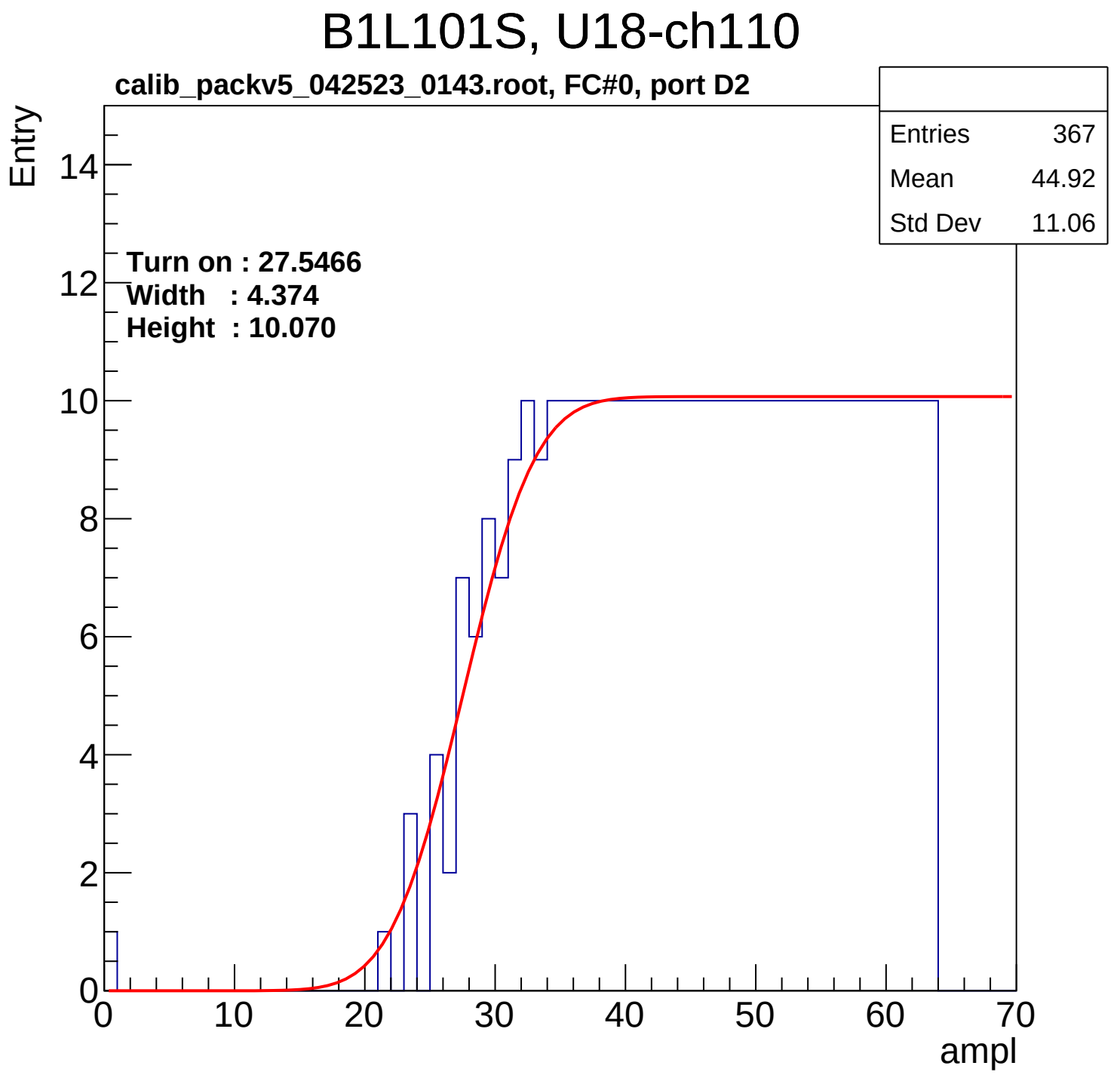
B1L101S, U18-ch110
calib_packv5_042523_0143.root, FC#0, port D2
Entries 367
Mean 44.92
Std Dev 11.06
Turn on : 27.5466
Width : 4.374
Height : 10.070
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ampl
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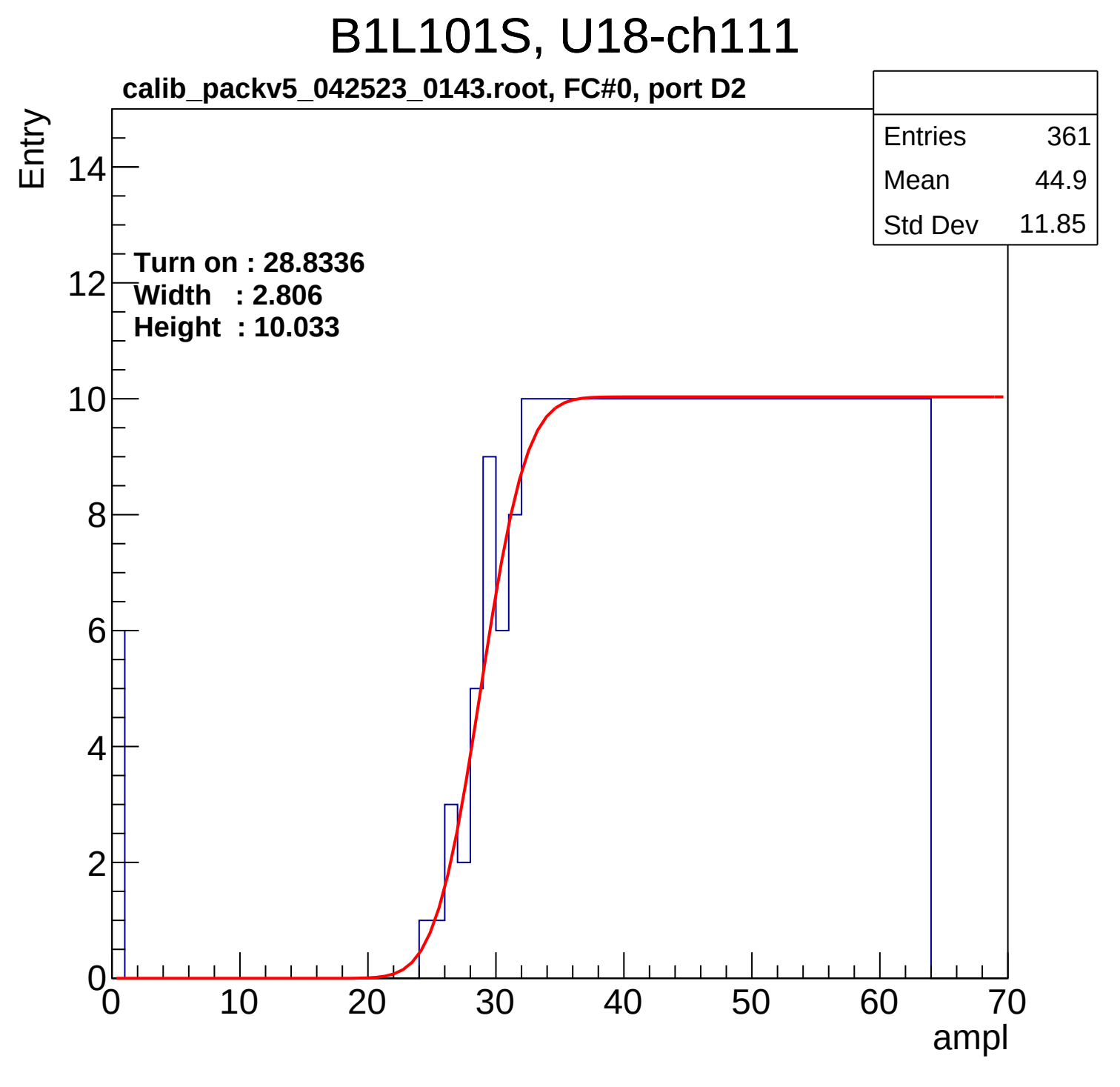
B1L101S, U18-ch111
calib_packv5_042523_0143.root, FC#0, port D2
Entries 361
Mean 44.9
Std Dev 11.85
Turn on : 28.8336
Width : 2.806
Height : 10.033
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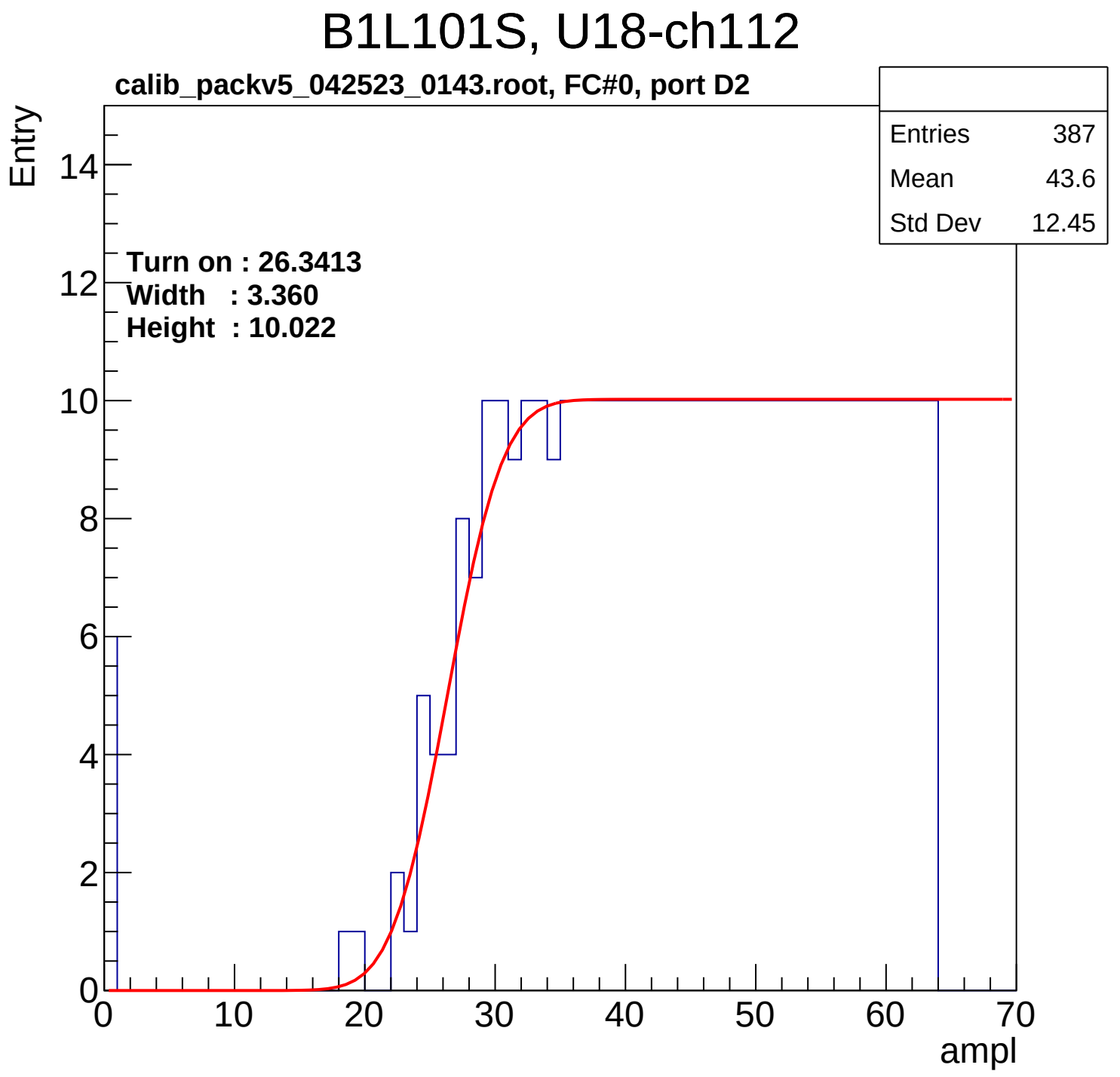
B1L101S, U18-ch112
calib_packv5_042523_0143.root, FC#0, port D2
Entries 387
Mean 43.6
Std Dev 12.45
Turn on : 26.3413
Width : 3.360
Height : 10.022
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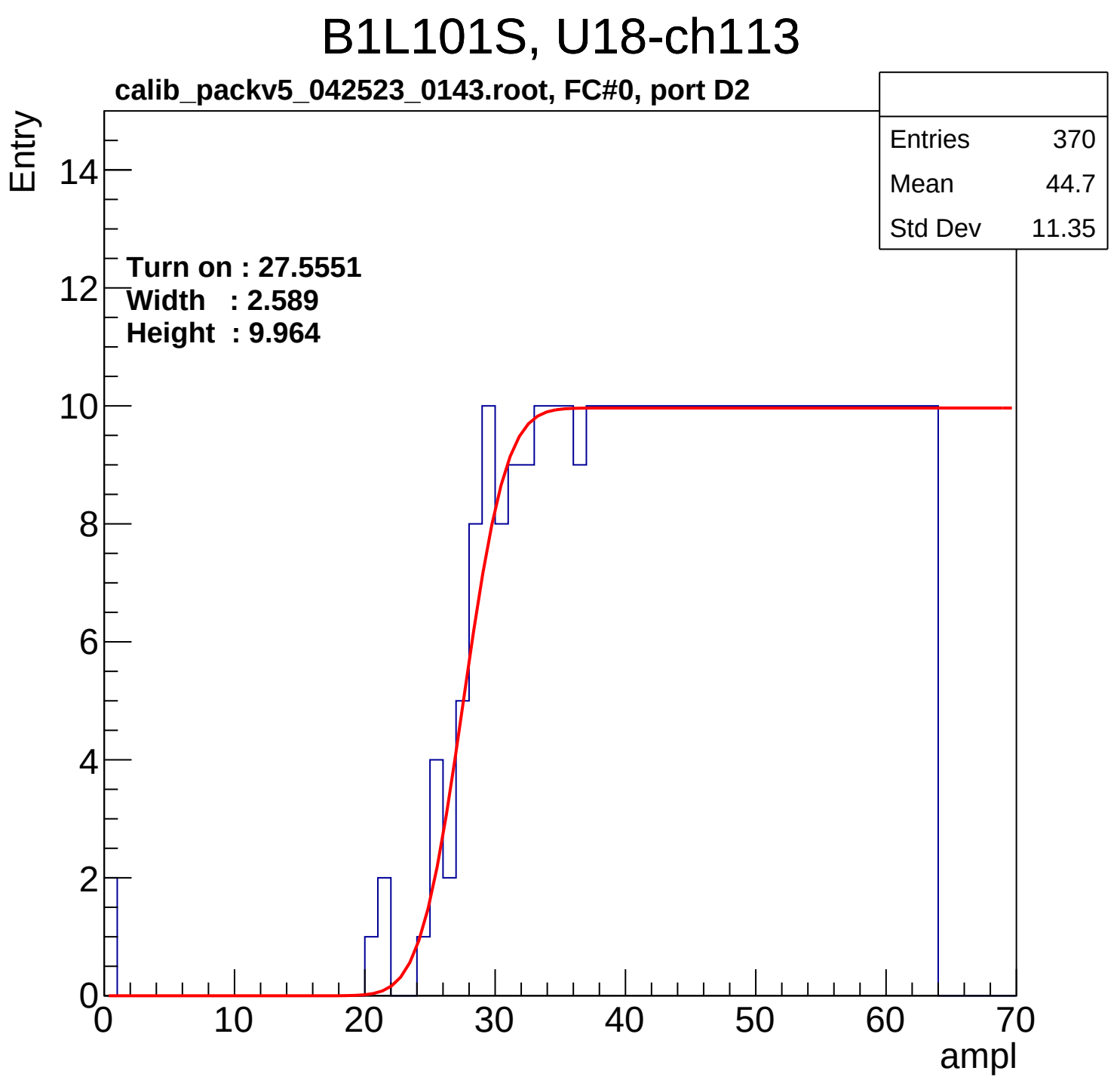
B1L101S, U18-ch113
calib_packv5_042523_0143.root, FC#0, port D2
Entries 370
Mean 44.7
Std Dev 11.35
Turn on : 27.5551
Width : 2.589
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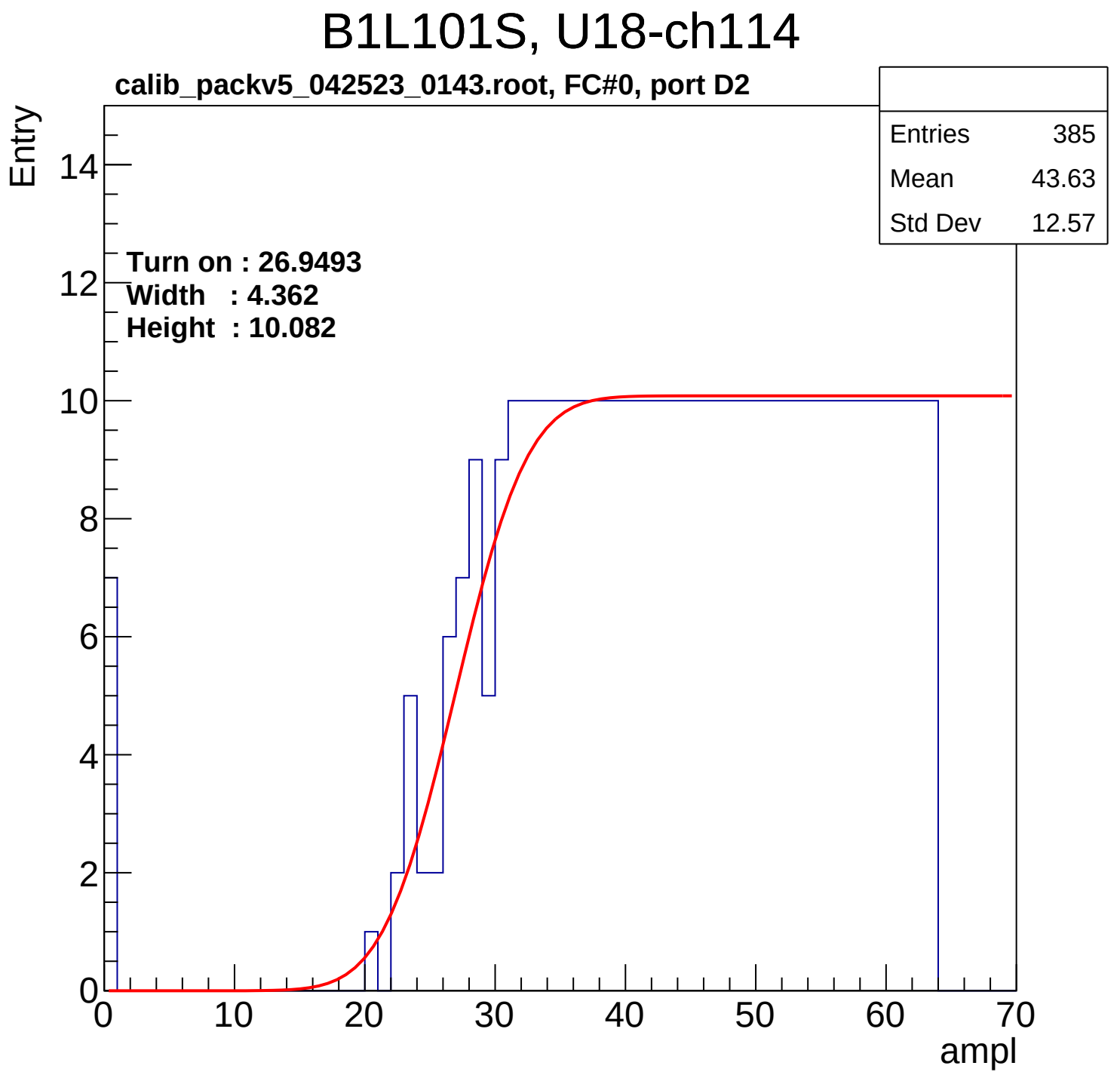
B1L101S, U18-ch114
calib_packv5_042523_0143.root, FC#0, port D2
Entries 385
Mean 43.63
Std Dev 12.57
Turn on : 26.9493
Width : 4.362
Height : 10.082
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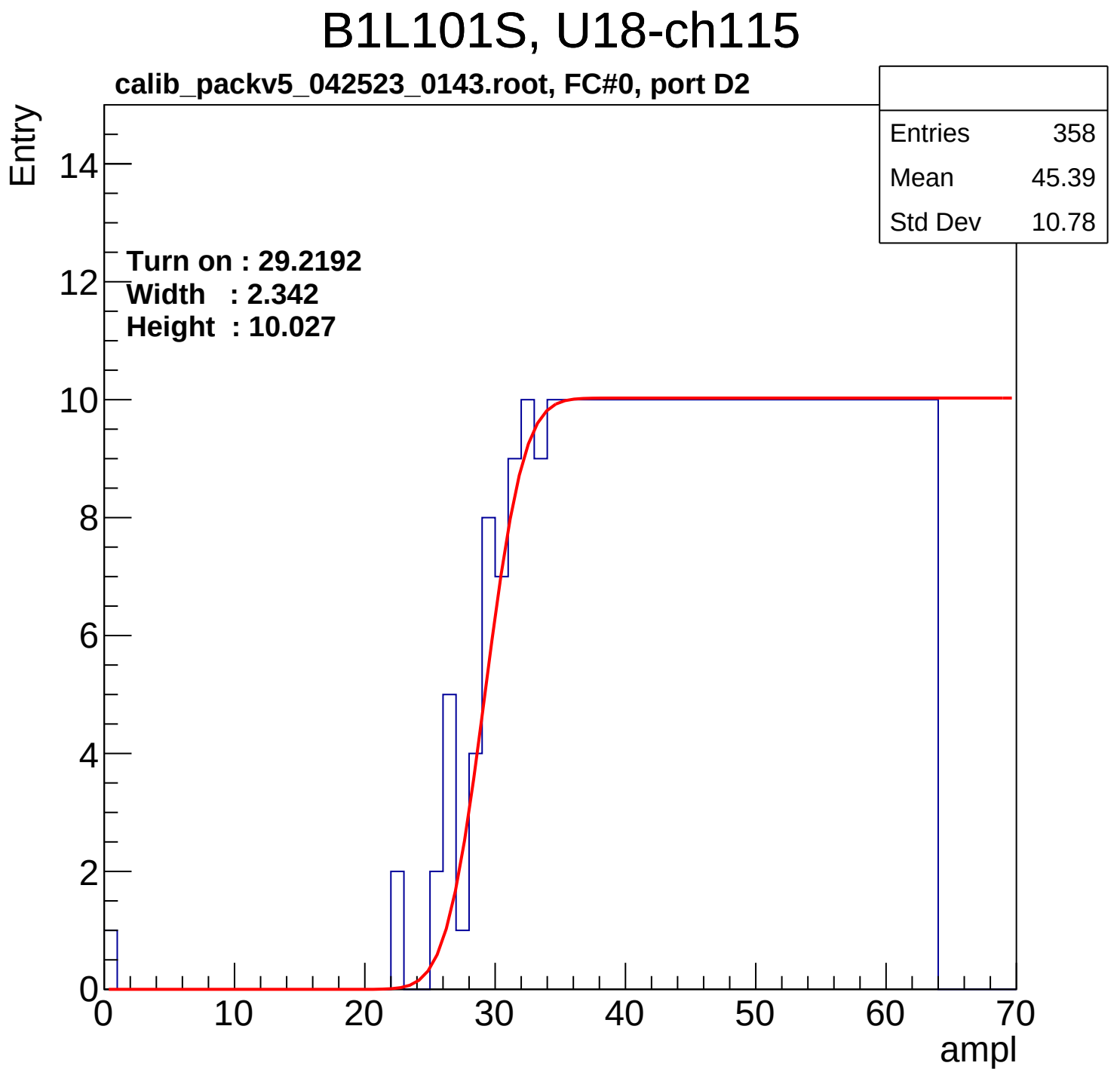
B1L101S, U18-ch115
calib_packv5_042523_0143.root, FC#0, port D2
Entries 358
Mean 45.39
Std Dev 10.78
Turn on : 29.2192
Width : 2.342
Height : 10.027
Entry
ampl
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4
6
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20
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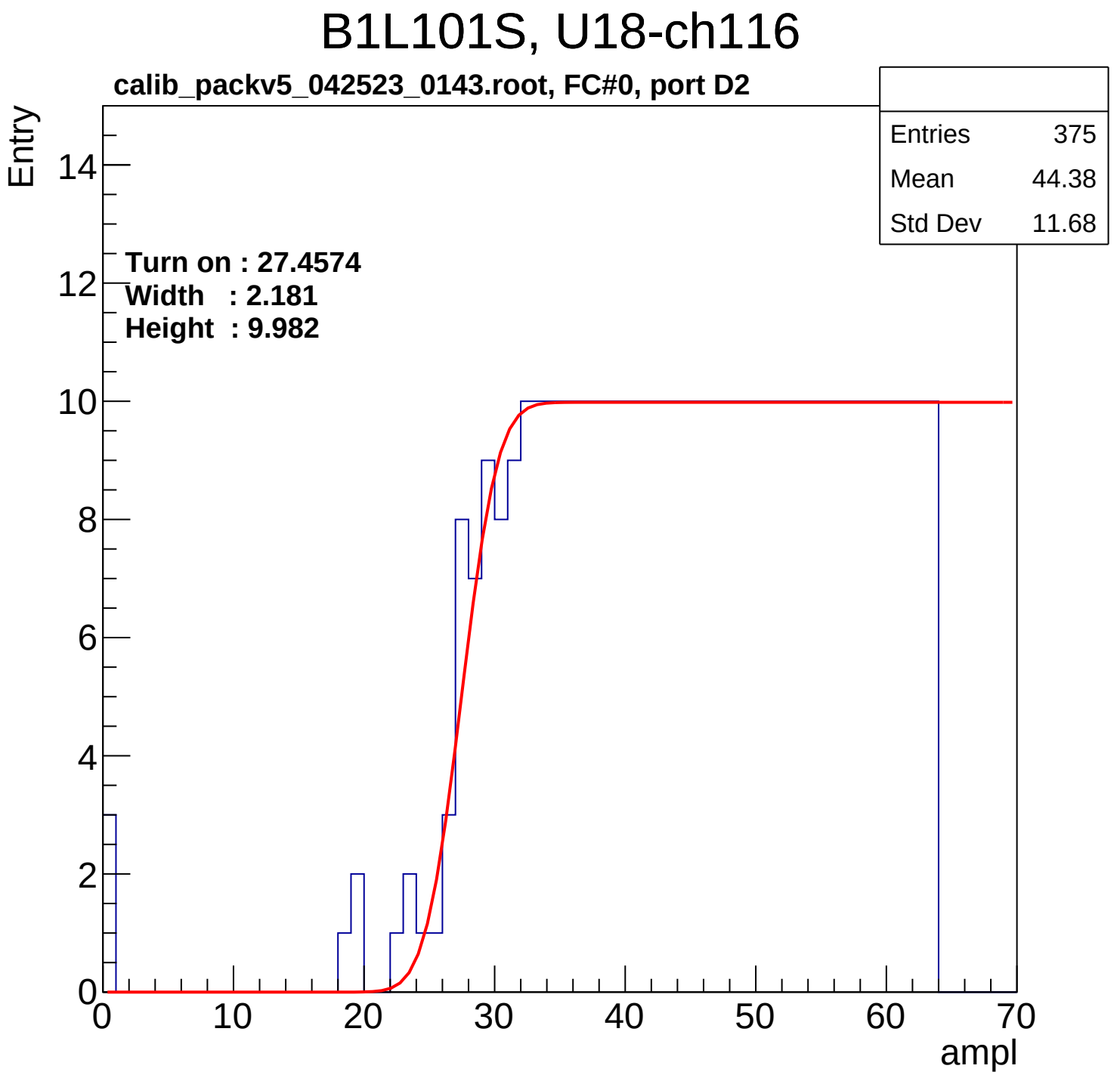
B1L101S, U18-ch116
calib_packv5_042523_0143.root, FC#0, port D2
Entries 375
Mean 44.38
Std Dev 11.68
Turn on : 27.4574
Width : 2.181
Height : 9.982
Entry
ampl
0
2
4
6
8
10
12
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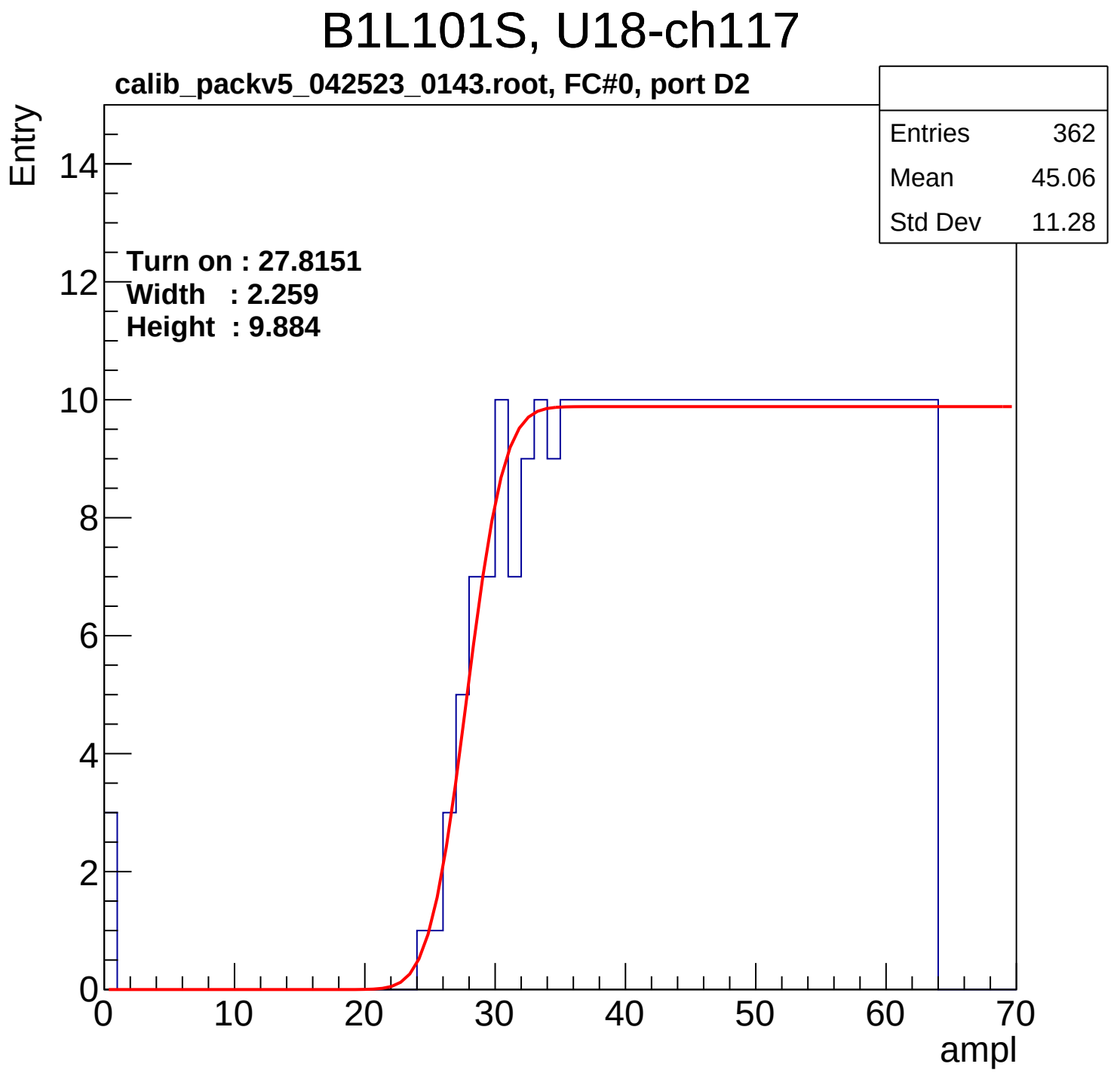
B1L101S, U18-ch117
calib_packv5_042523_0143.root, FC#0, port D2
Entries 362
Mean 45.06
Std Dev 11.28
Turn on : 27.8151
Width : 2.259
Height : 9.884
Entry
ampl
0
2
4
6
8
10
12
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0
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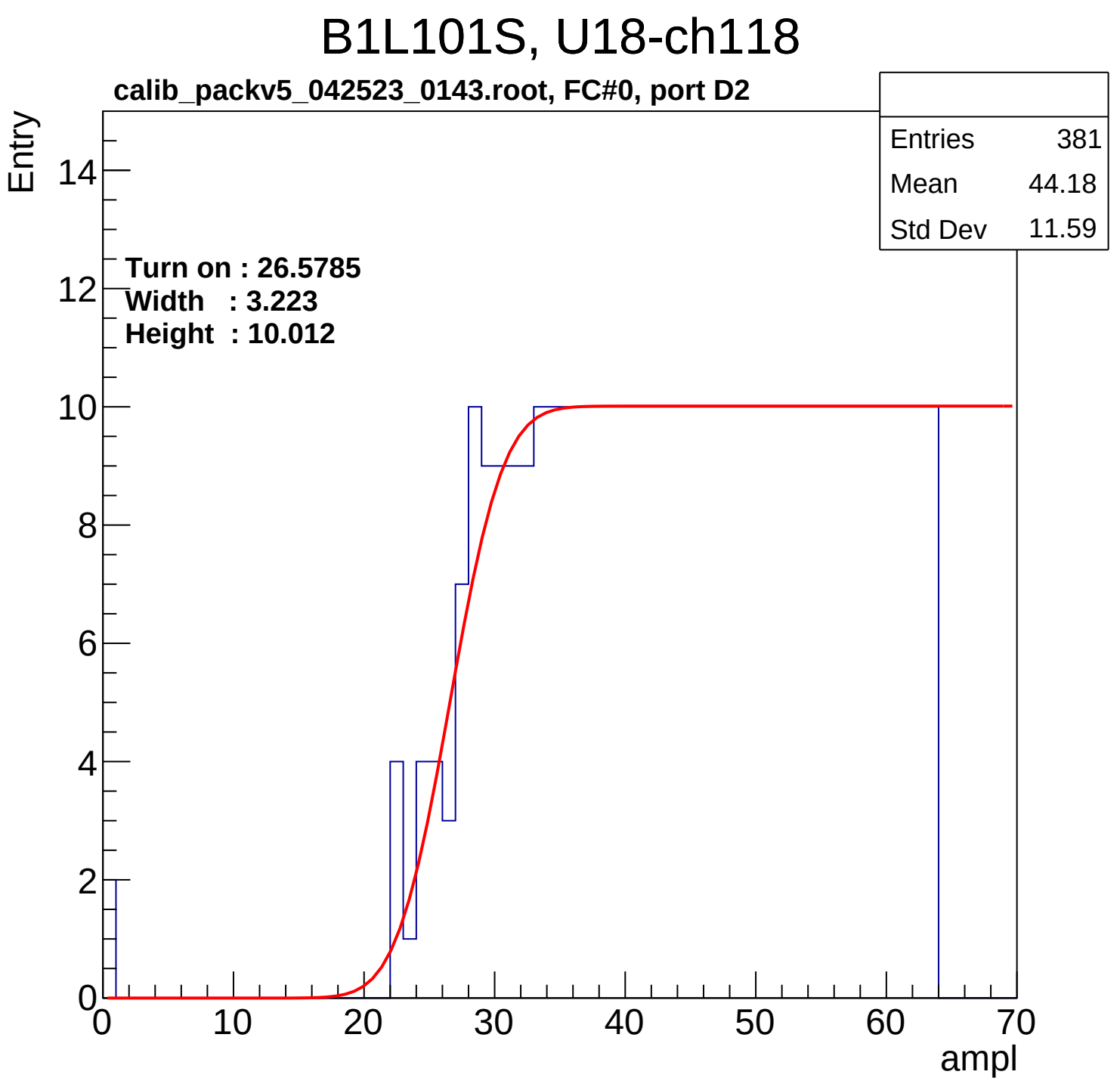
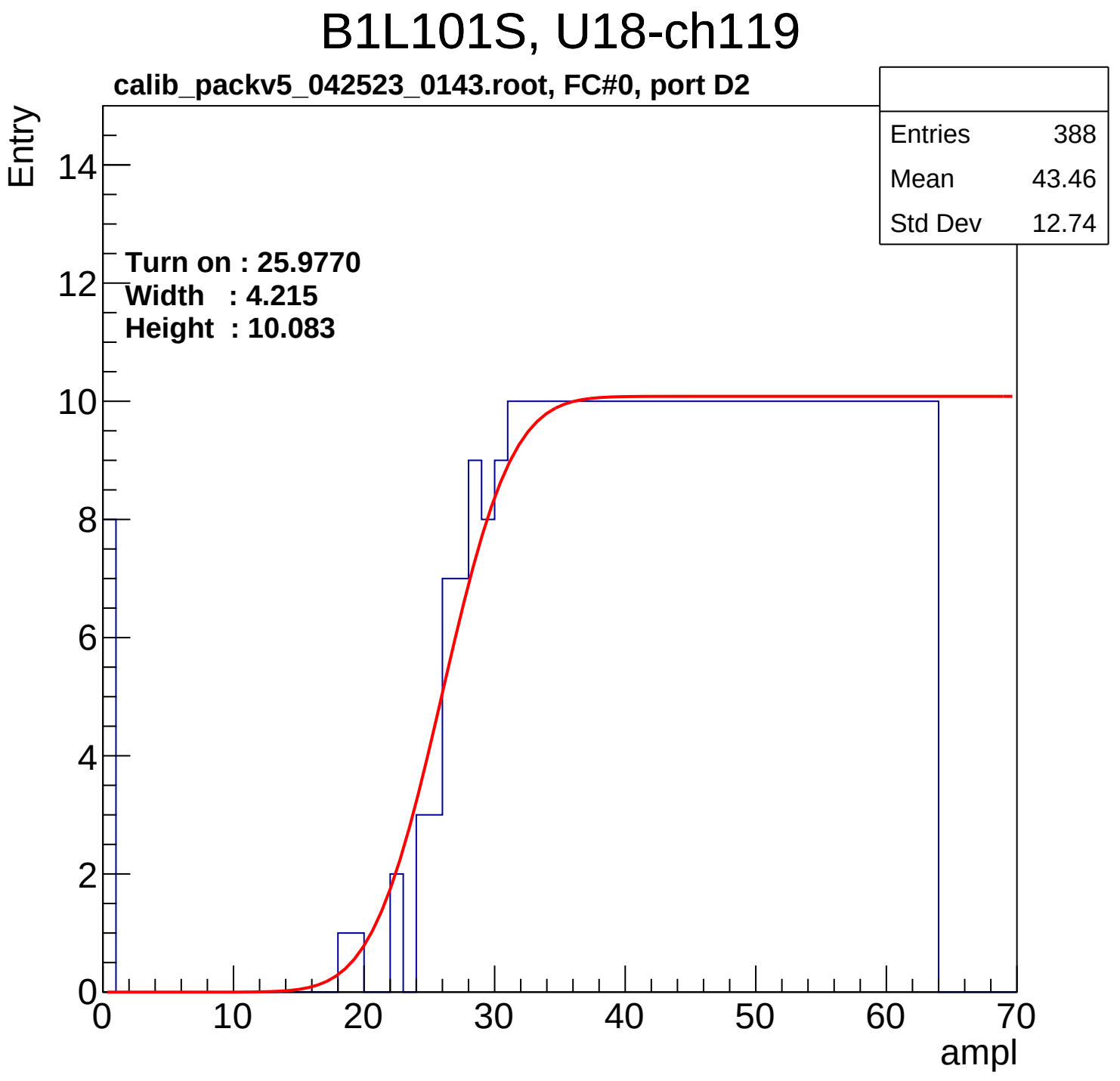
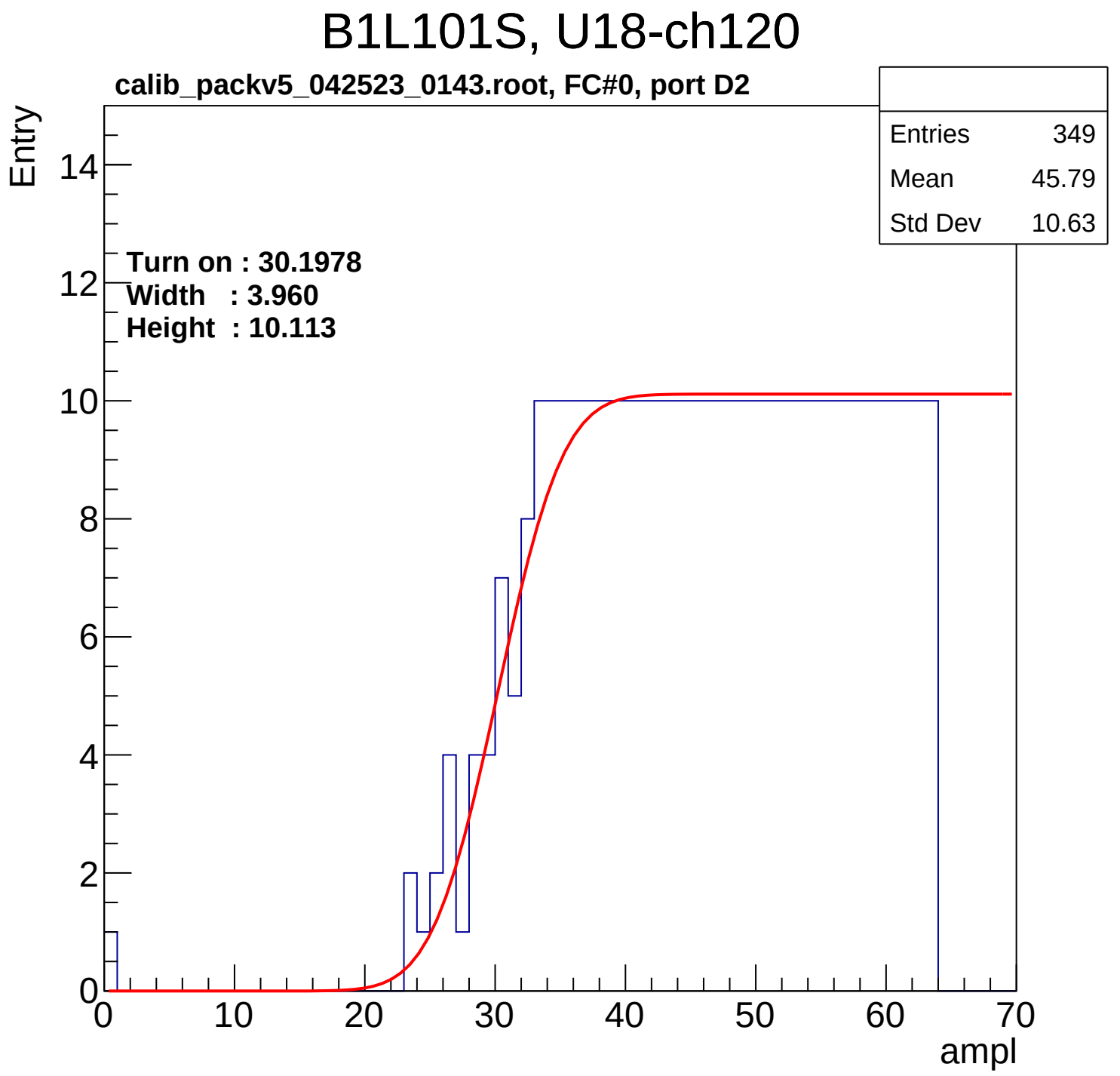

B1L101S, U18-ch118
calib_packv5_042523_0143.root, FC#0, port D2
Entries 381
Mean 44.18
Std Dev 11.59
Turn on : 26.5785
Width : 3.223
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U18-ch119
calib_packv5_042523_0143.root, FC#0, port D2
Entries 388
Mean 43.46
Std Dev 12.74
Turn on : 25.9770
Width : 4.215
Height : 10.083
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U18-ch120
calib_packv5_042523_0143.root, FC#0, port D2
Entries 349
Mean 45.79
Std Dev 10.63
Turn on : 30.1978
Width : 3.960
Height : 10.113
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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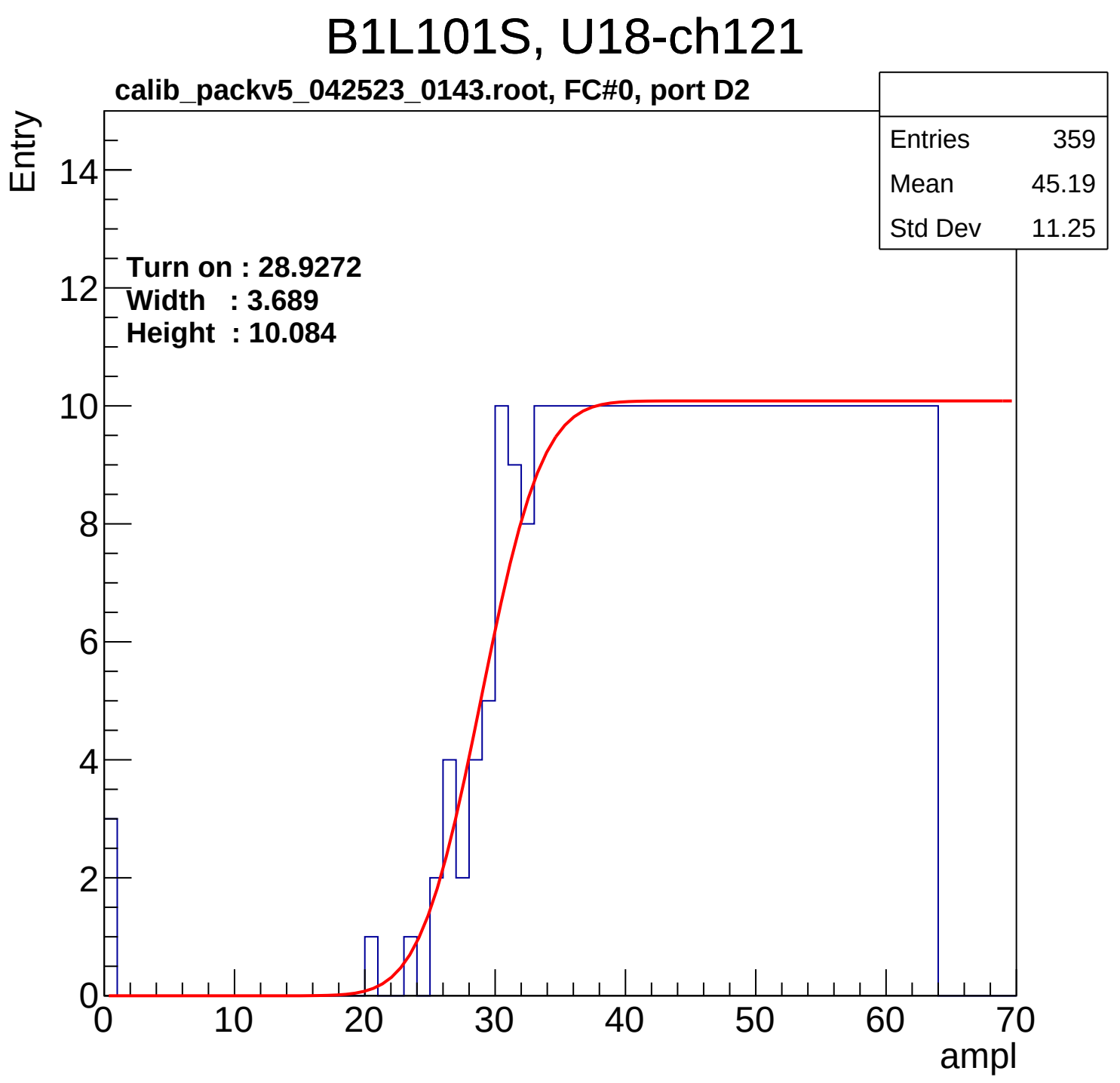
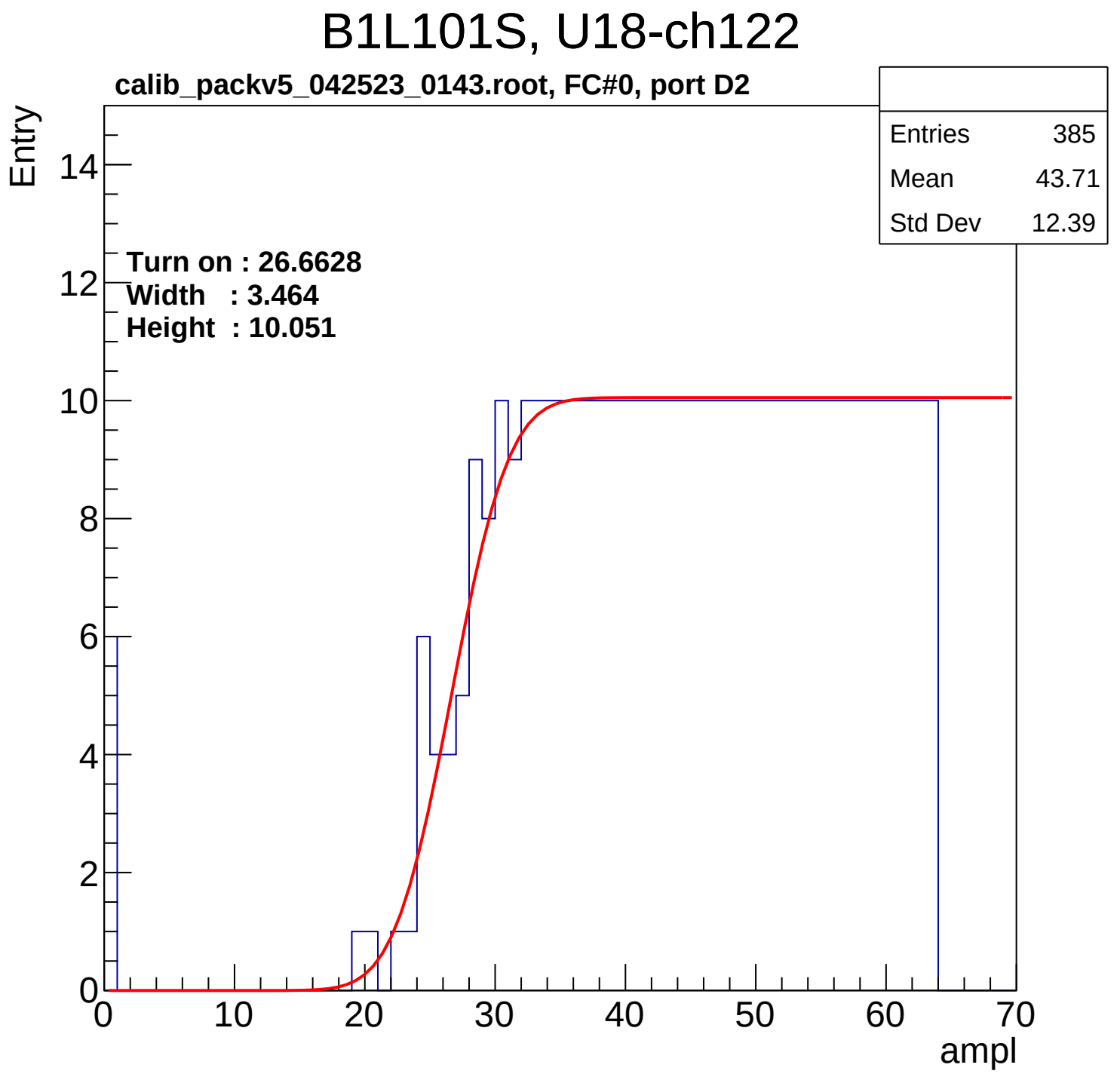
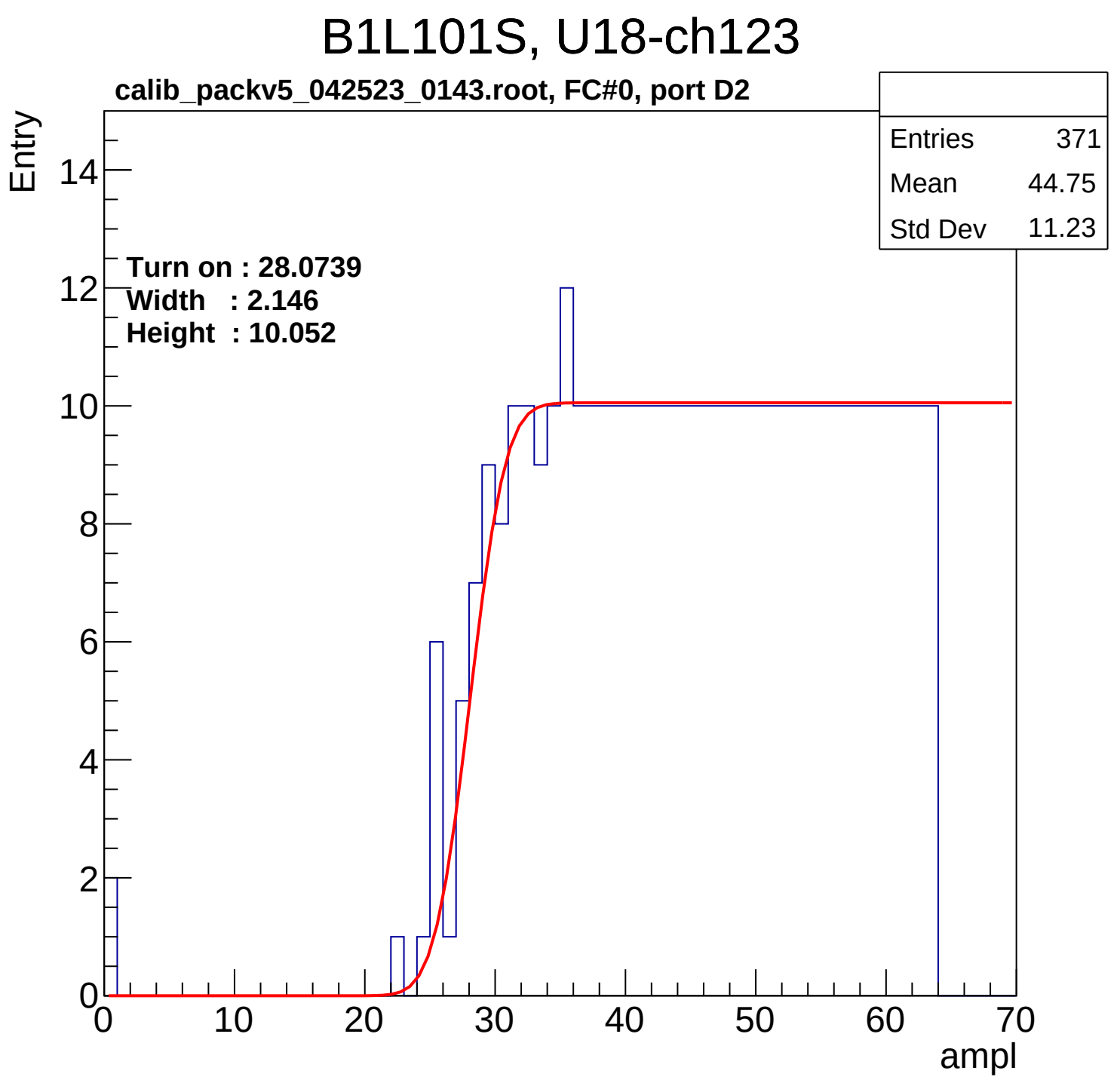

B1L101S, U18-ch121
calib_packv5_042523_0143.root, FC#0, port D2
Entries 359
Mean 45.19
Std Dev 11.25
Turn on : 28.9272
Width : 3.689
Height : 10.084
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U18-ch122
calib_packv5_042523_0143.root, FC#0, port D2
Entries 385
Mean 43.71
Std Dev 12.39
Turn on : 26.6628
Width : 3.464
Height : 10.051
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U18-ch123
calib_packv5_042523_0143.root, FC#0, port D2
Entries 371
Mean 44.75
Std Dev 11.23
Turn on : 28.0739
Width : 2.146
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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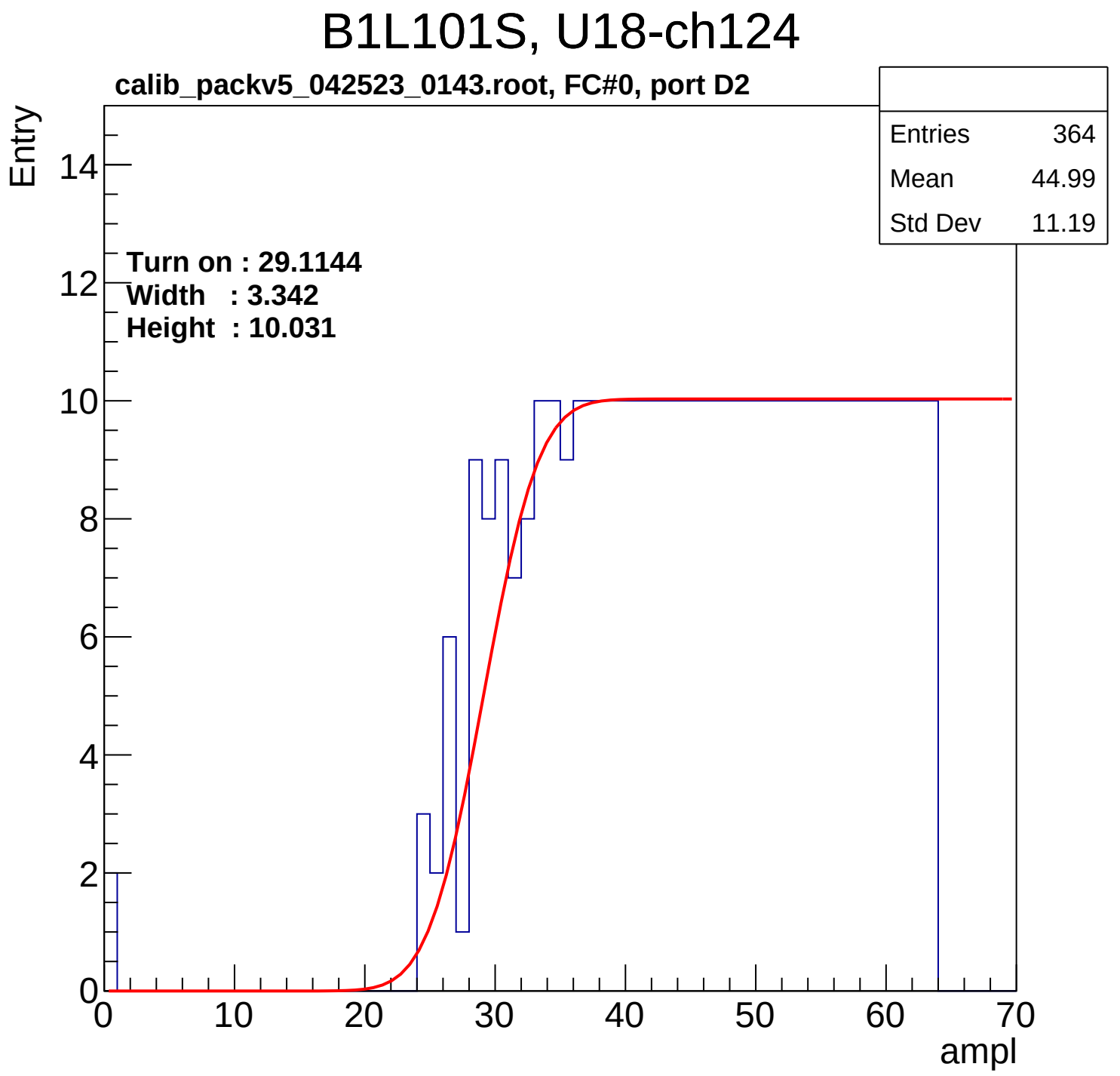
40
50
60
70


B1L101S, U18-ch124
calib_packv5_042523_0143.root, FC#0, port D2
Entries 364
Mean 44.99
Std Dev 11.19
Turn on : 29.1144
Width : 3.342
Height : 10.031
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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40
50
60
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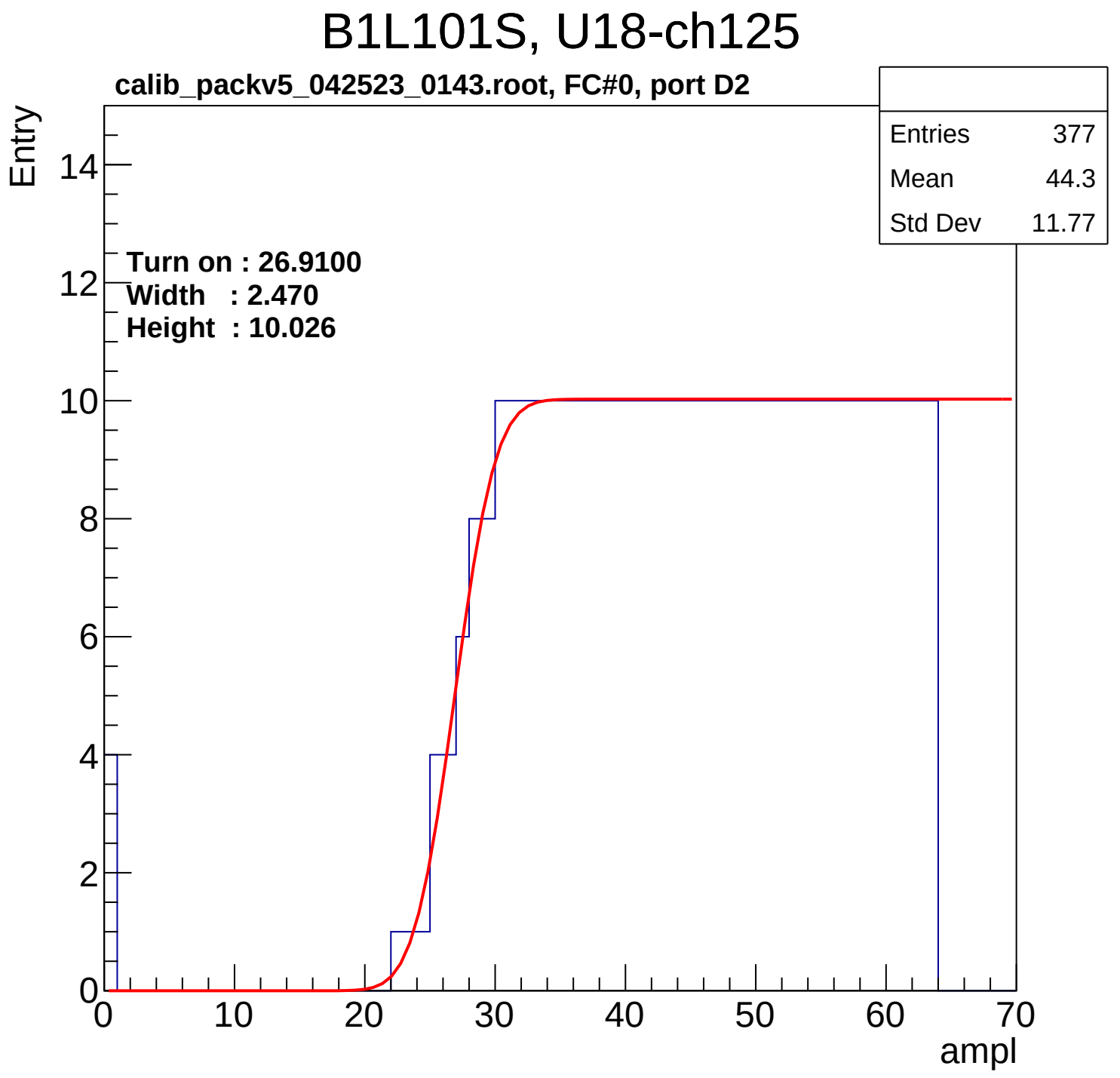
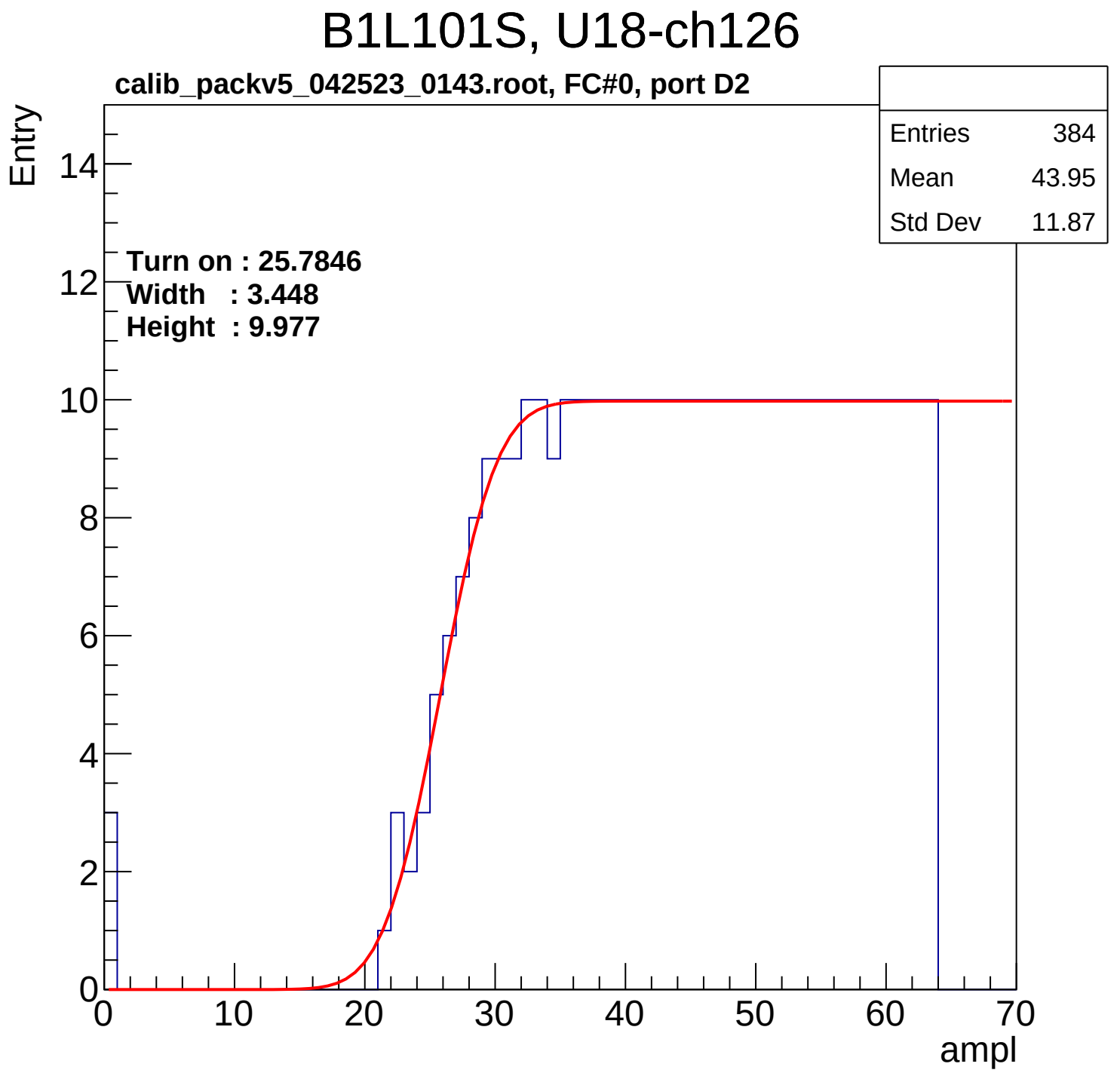

B1L101S, U18-ch125
calib_packv5_042523_0143.root, FC#0, port D2
Entries 377
Mean 44.3
Std Dev 11.77
Turn on : 26.9100
Width : 2.470
Height : 10.026
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U18-ch126
calib_packv5_042523_0143.root, FC#0, port D2
Entries 384
Mean 43.95
Std Dev 11.87
Turn on : 25.7846
Width : 3.448
Height : 9.977
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
50
60
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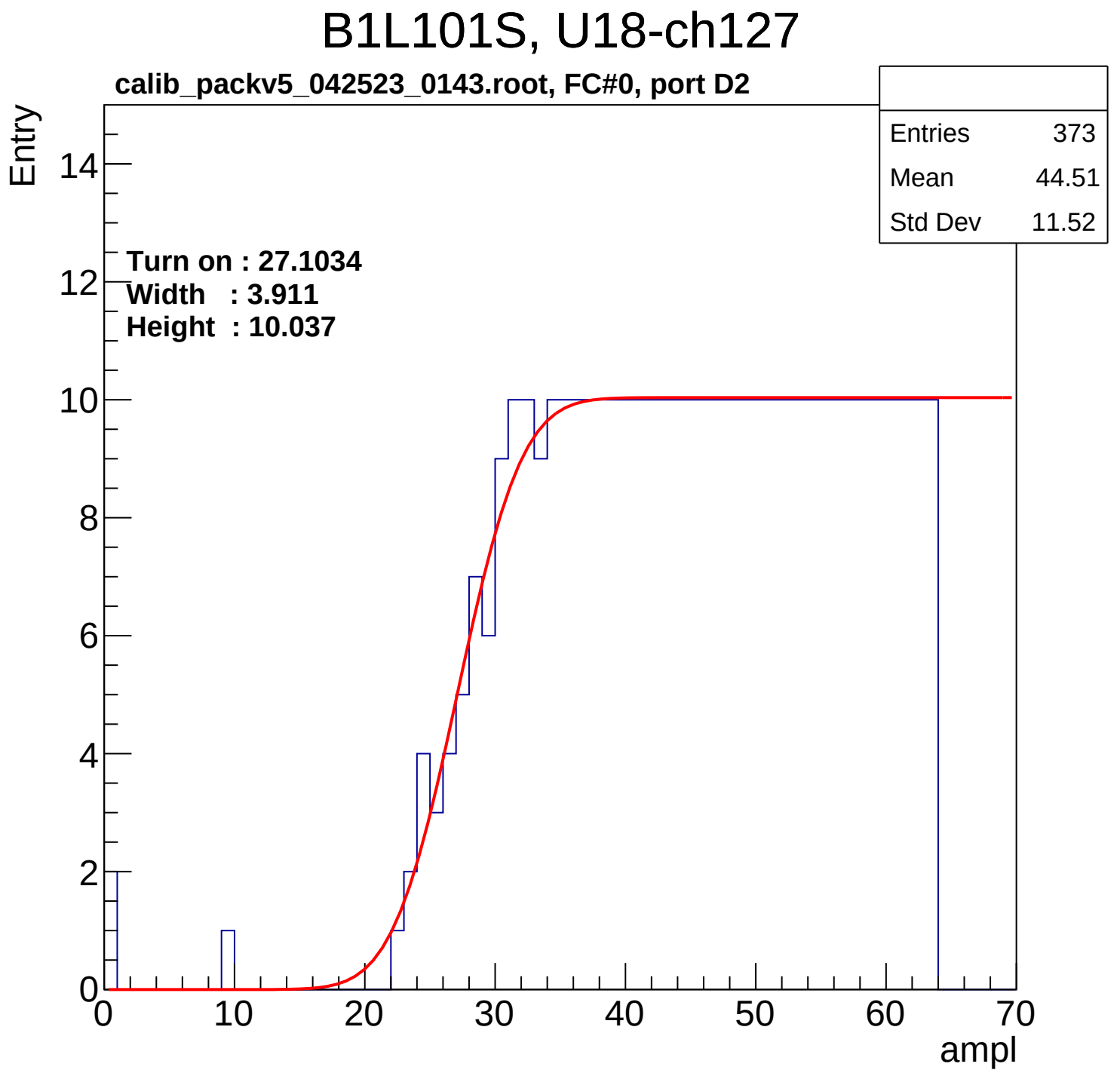
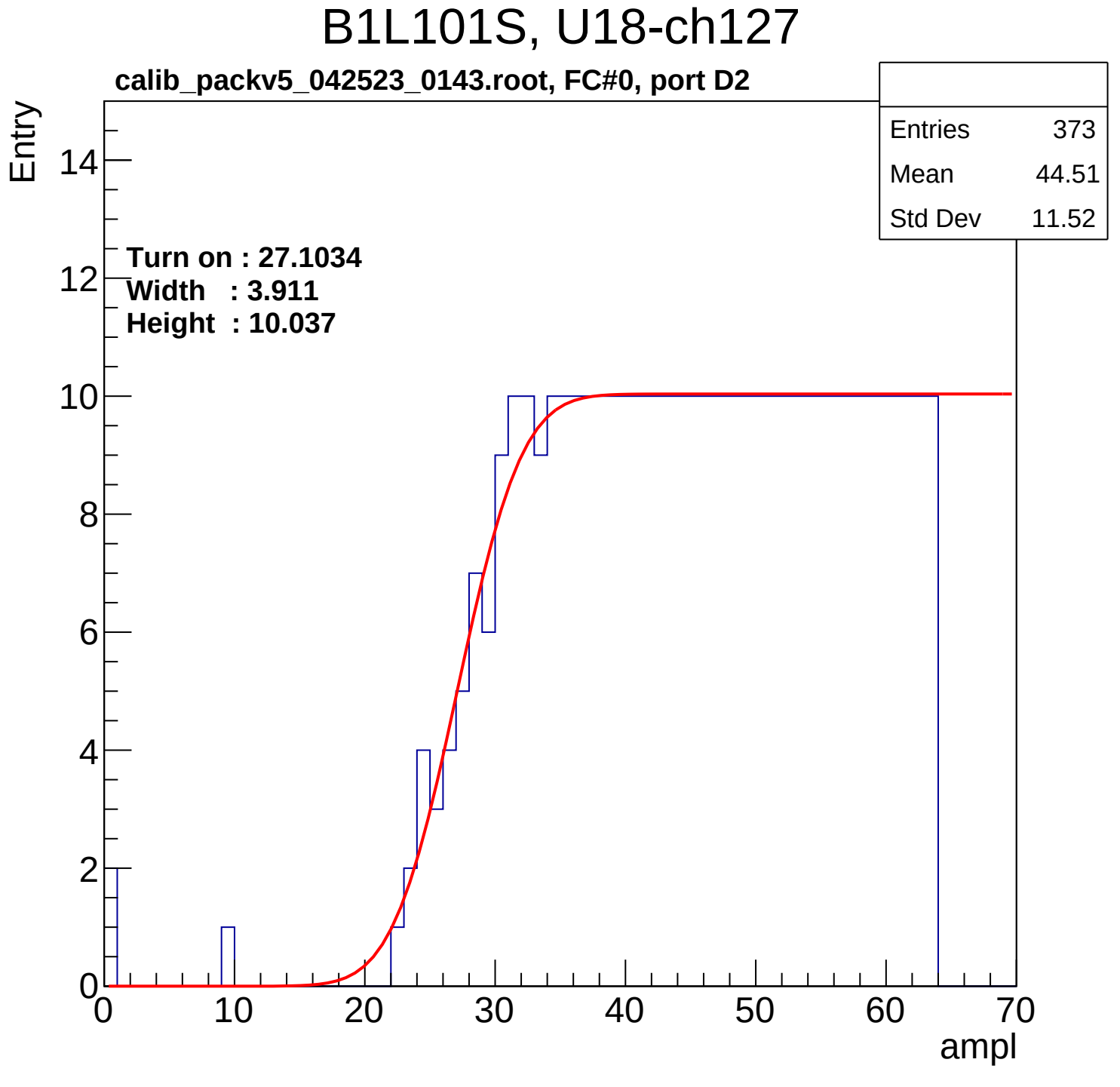

B1L101S, U18-ch127
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.51
Std Dev 11.52
Turn on : 27.1034
Width : 3.911
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L101S, U18-ch127
calib_packv5_042523_0143.root, FC#0, port D2
Entries 373
Mean 44.51
Std Dev 11.52
Turn on : 27.1034
Width : 3.911
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70