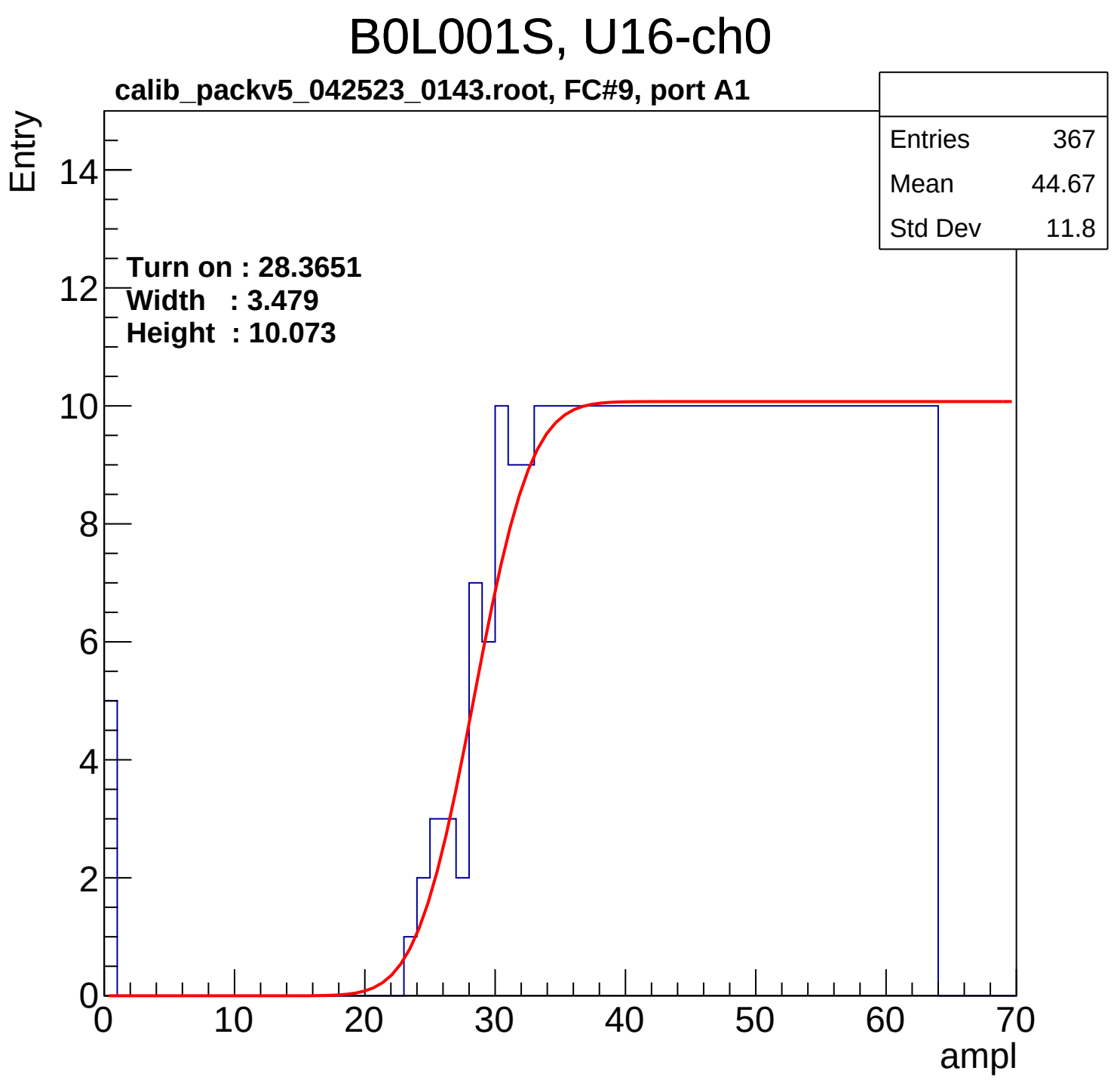
B0L001S, U16-ch0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.67
Std Dev 11.8
Turn on : 28.3651
Width : 3.479
Height : 10.073
Entry
ampl
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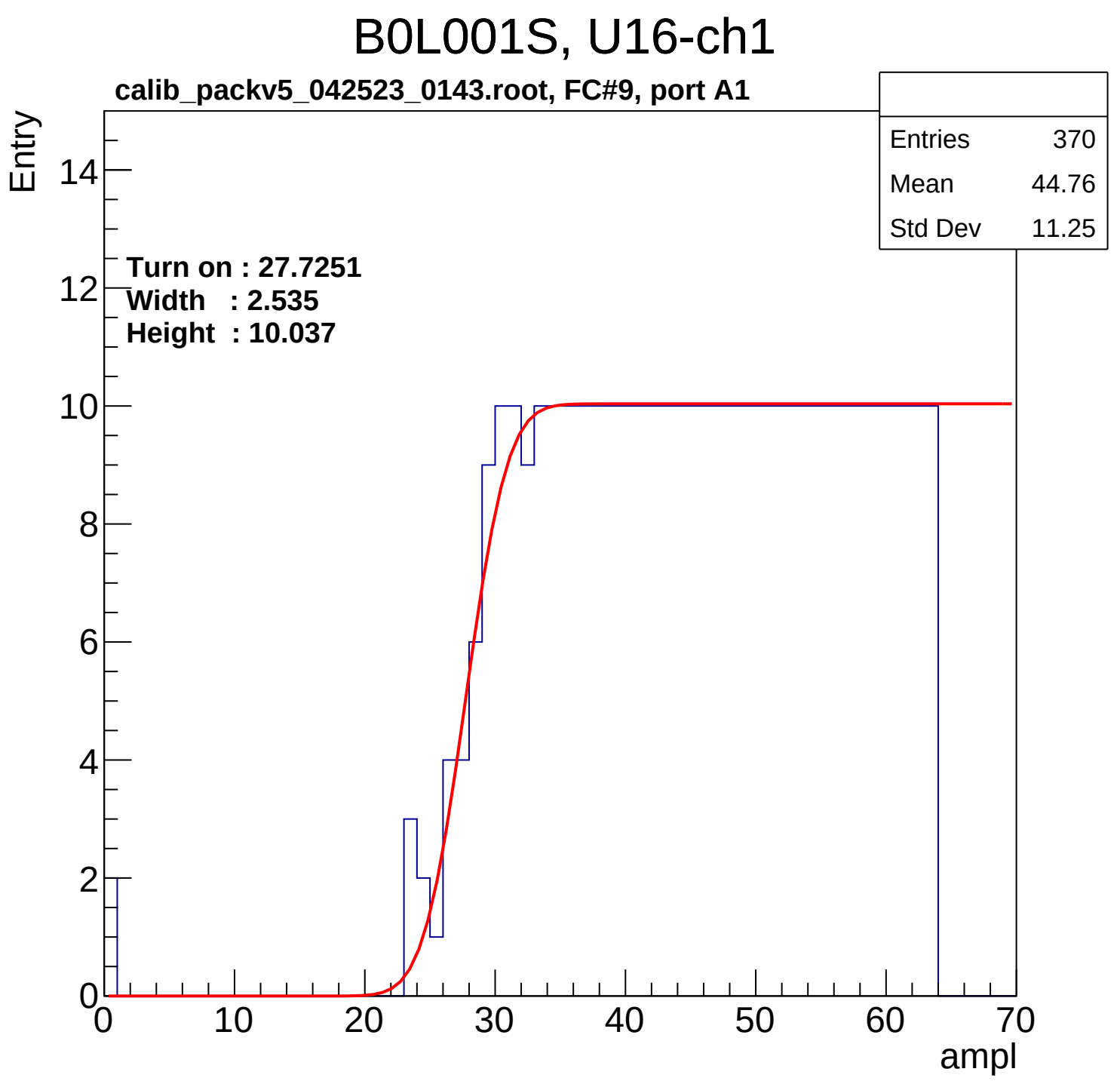
B0L001S, U16-ch1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.76
Std Dev 11.25
Turn on : 27.7251
Width : 2.535
Height : 10.037
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ampl
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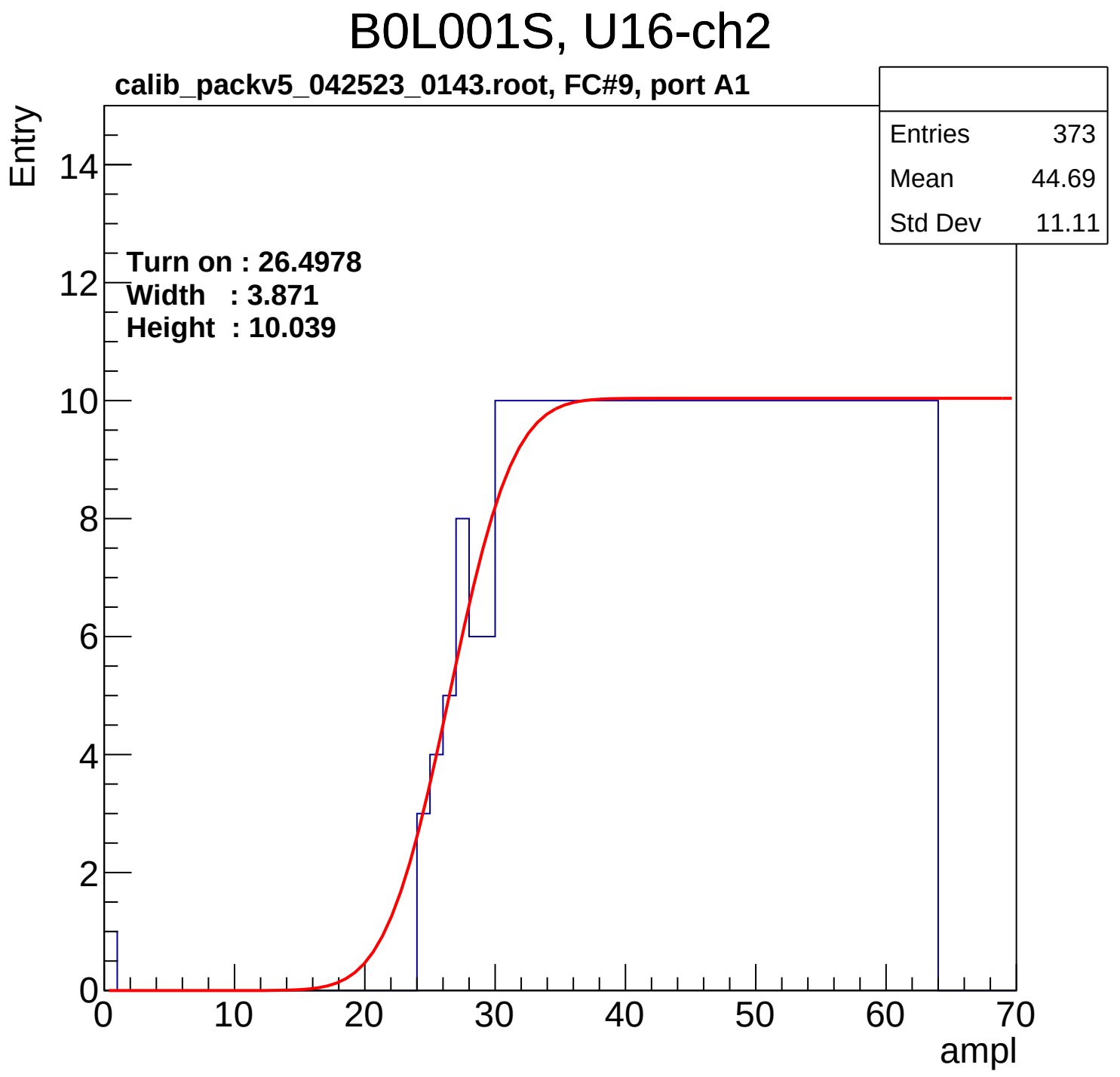
B0L001S, U16-ch2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.69
Std Dev 11.11
Turn on : 26.4978
Width : 3.871
Height : 10.039
Entry
ampl
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2
4
6
8
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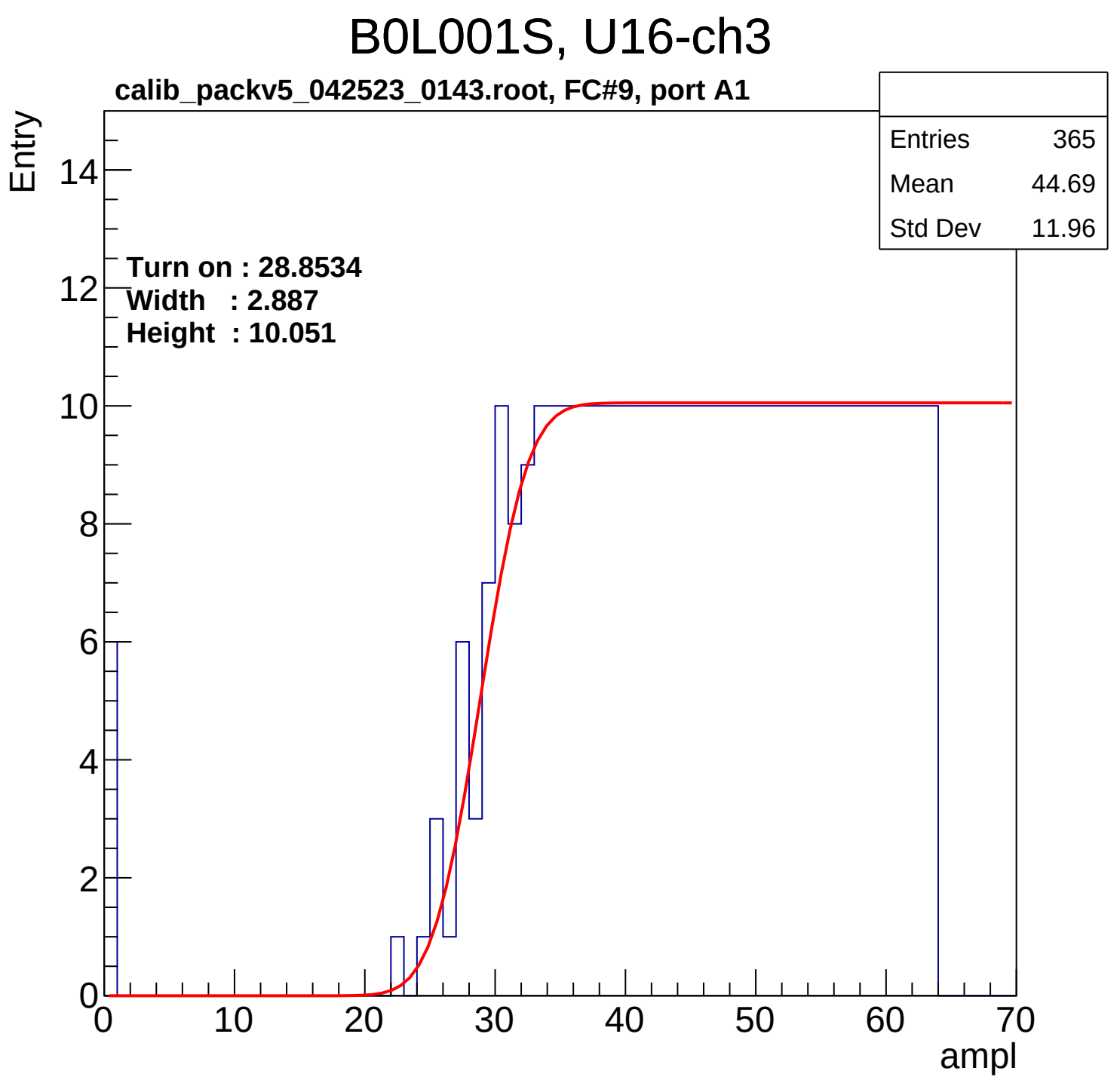
B0L001S, U16-ch3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.69
Std Dev 11.96
Turn on : 28.8534
Width : 2.887
Height : 10.051
Entry
ampl
0
2
4
6
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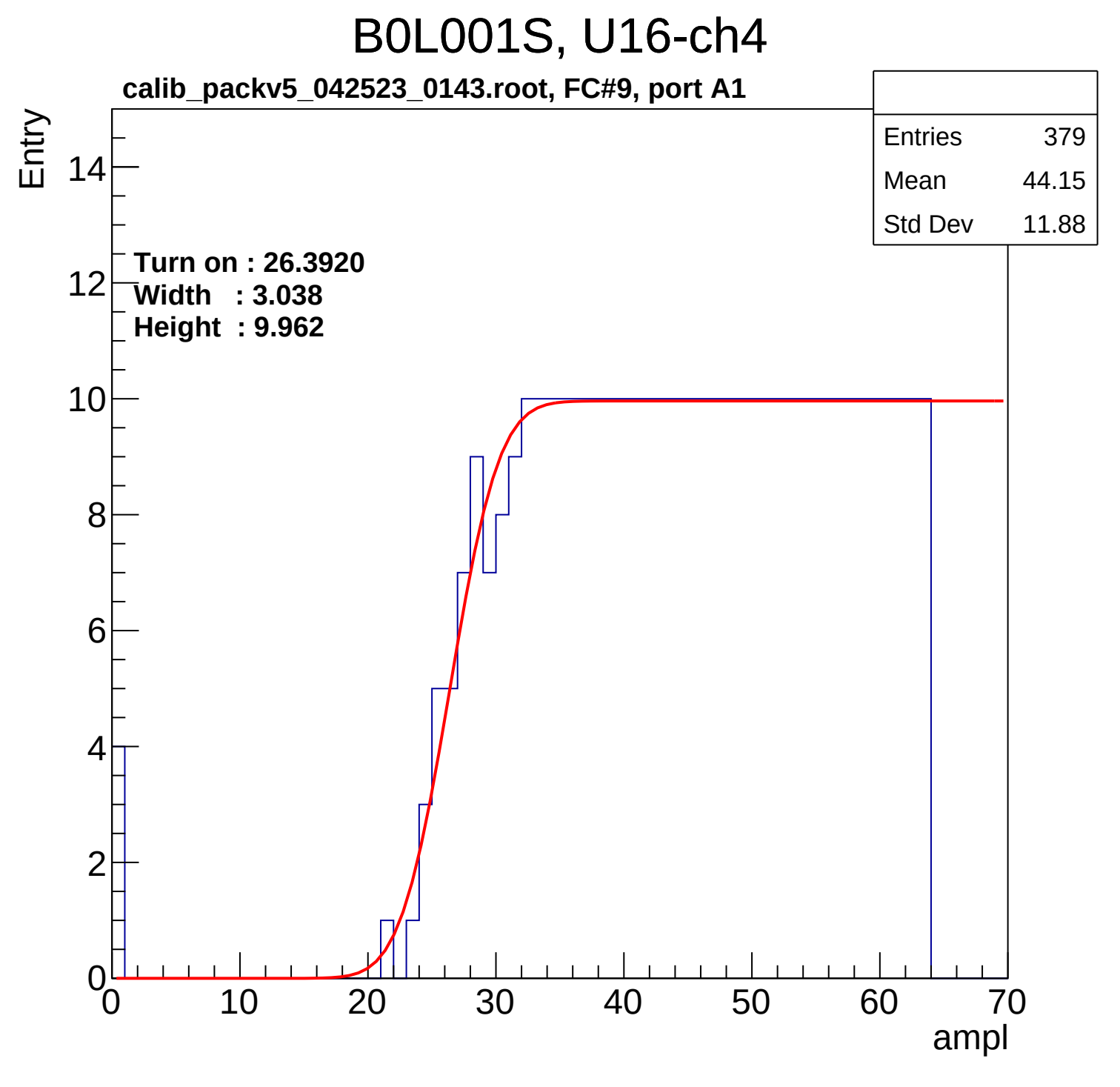
B0L001S, U16-ch4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 379
Mean 44.15
Std Dev 11.88
Turn on : 26.3920
Width : 3.038
Height : 9.962
Entry
ampl
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2
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6
8
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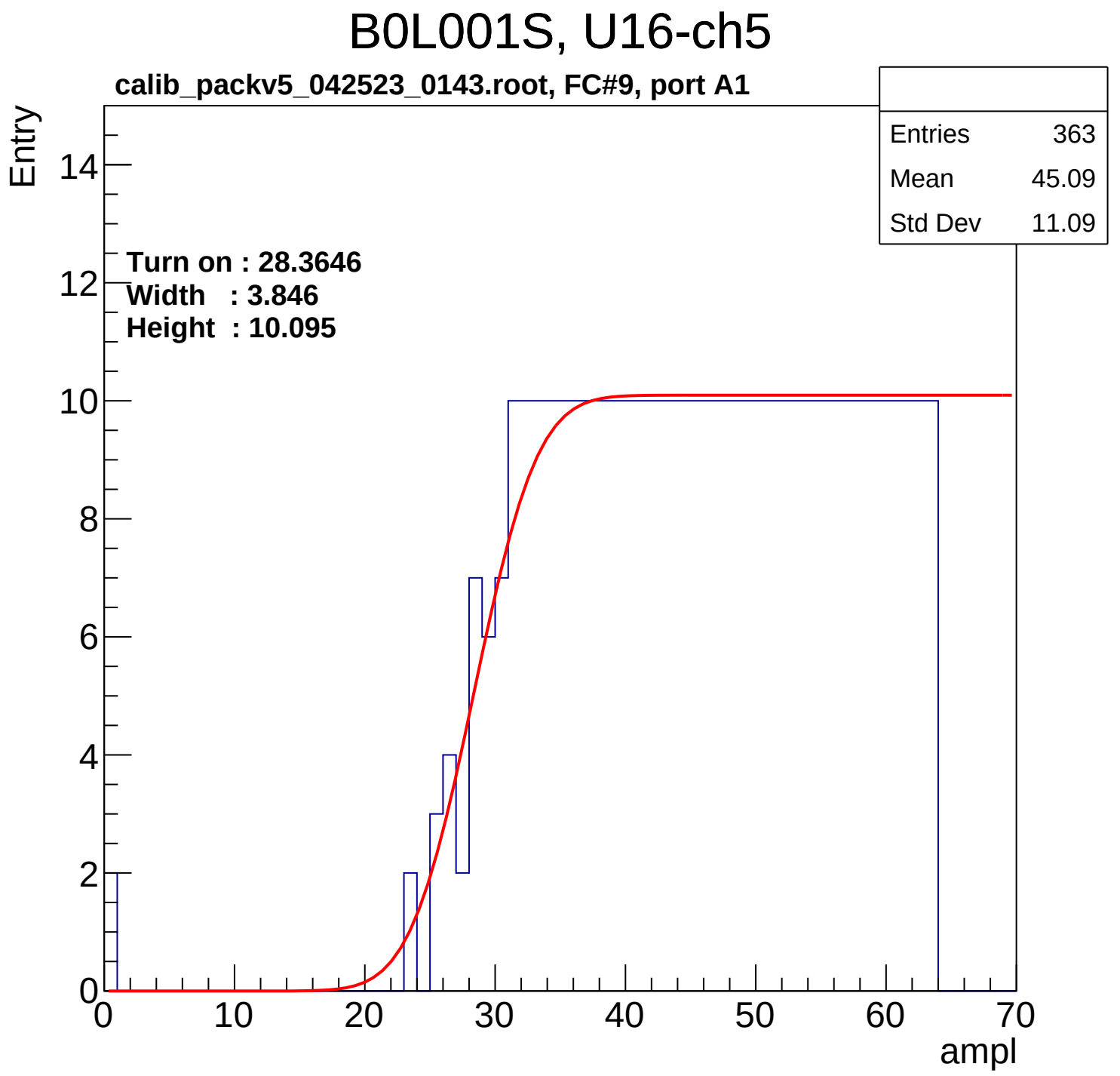
B0L001S, U16-ch5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.09
Std Dev 11.09
Turn on : 28.3646
Width : 3.846
Height : 10.095
Entry
ampl
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4
6
8
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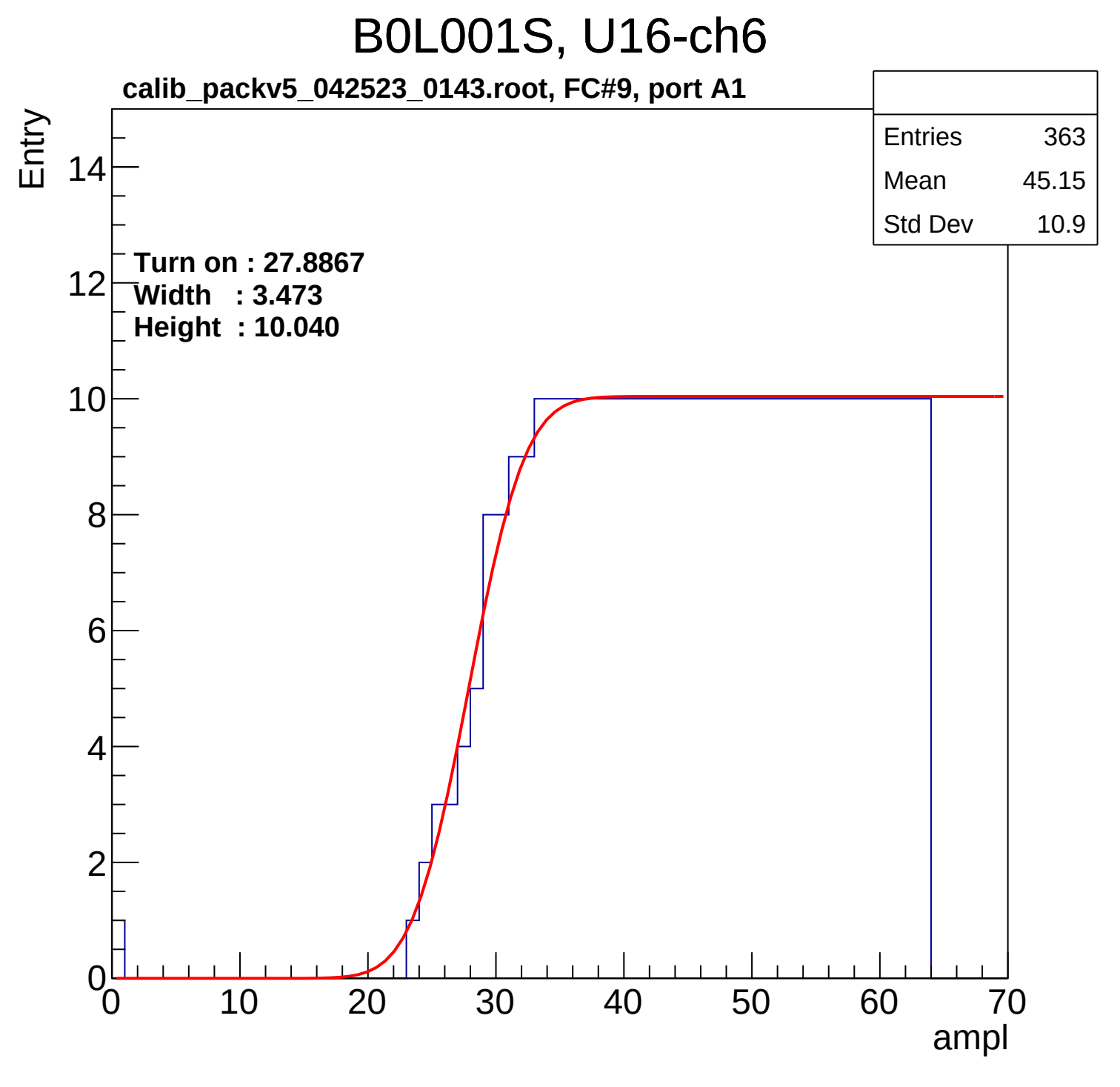
B0L001S, U16-ch6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.15
Std Dev 10.9
Turn on : 27.8867
Width : 3.473
Height : 10.040
Entry
ampl
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4
6
8
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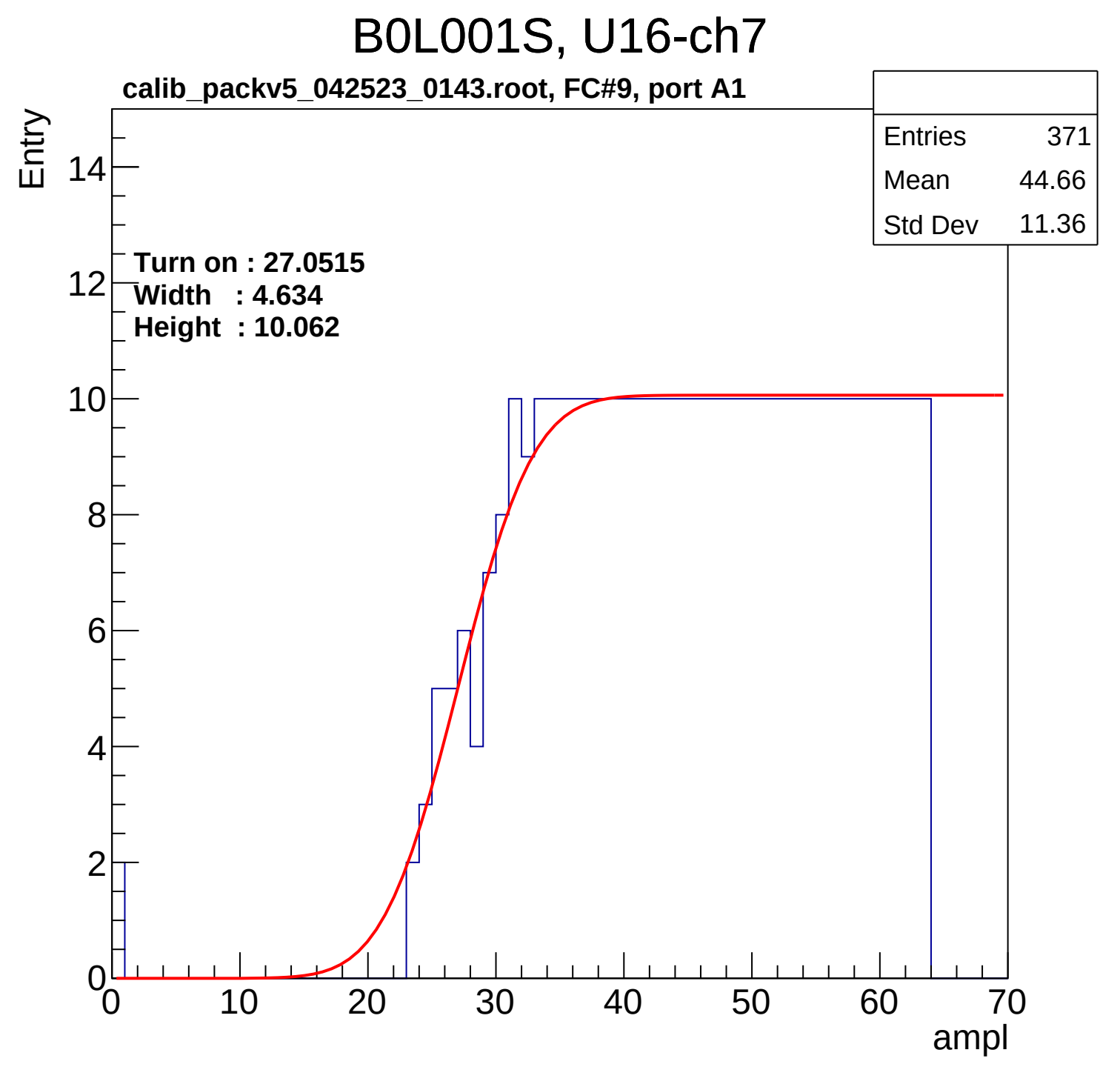
B0L001S, U16-ch7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.66
Std Dev 11.36
Turn on : 27.0515
Width : 4.634
Height : 10.062
Entry
ampl
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4
6
8
10
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60
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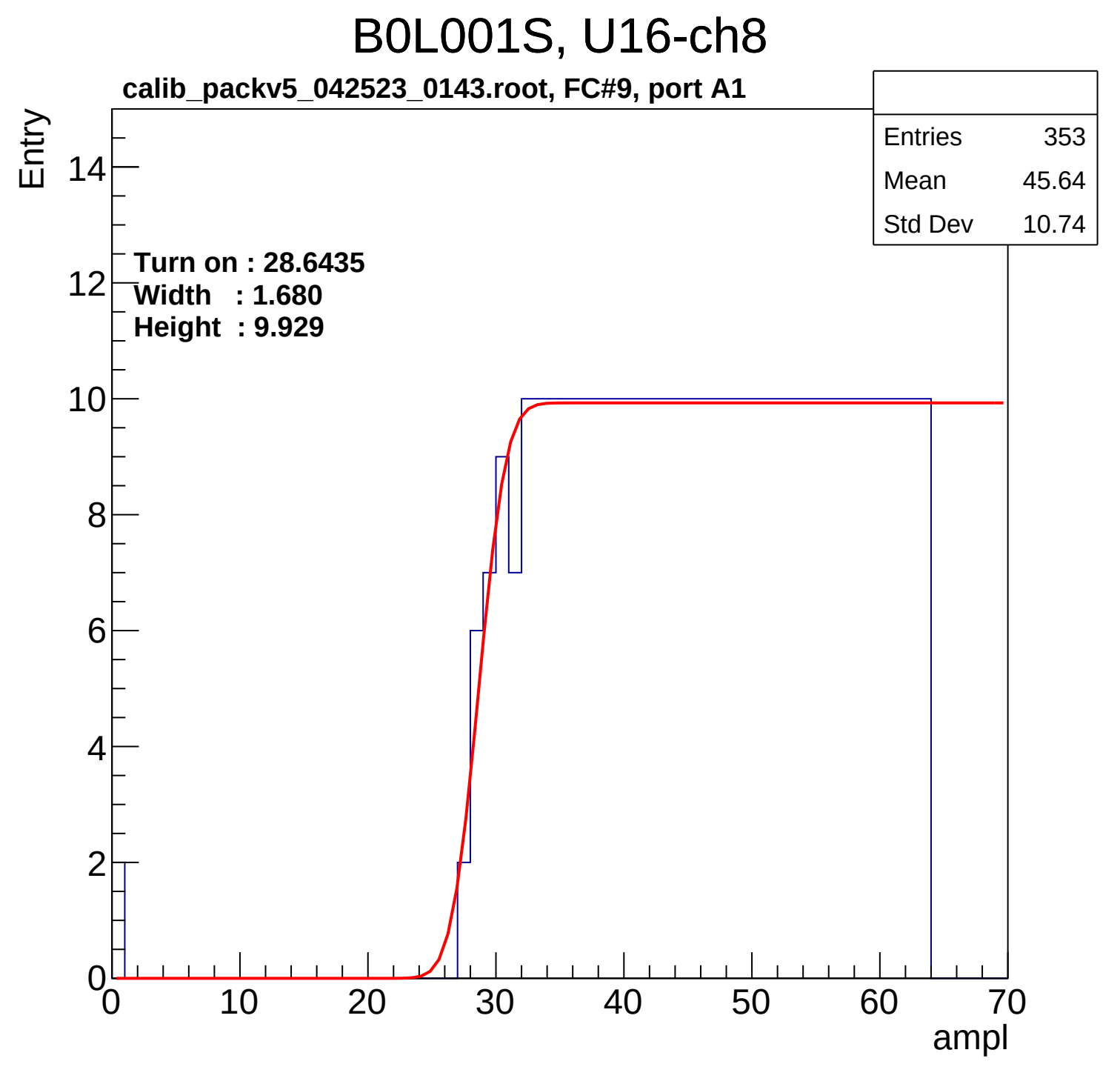
B0L001S, U16-ch8
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.64
Std Dev 10.74
Turn on : 28.6435
Width : 1.680
Height : 9.929
Entry
ampl
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6
8
10
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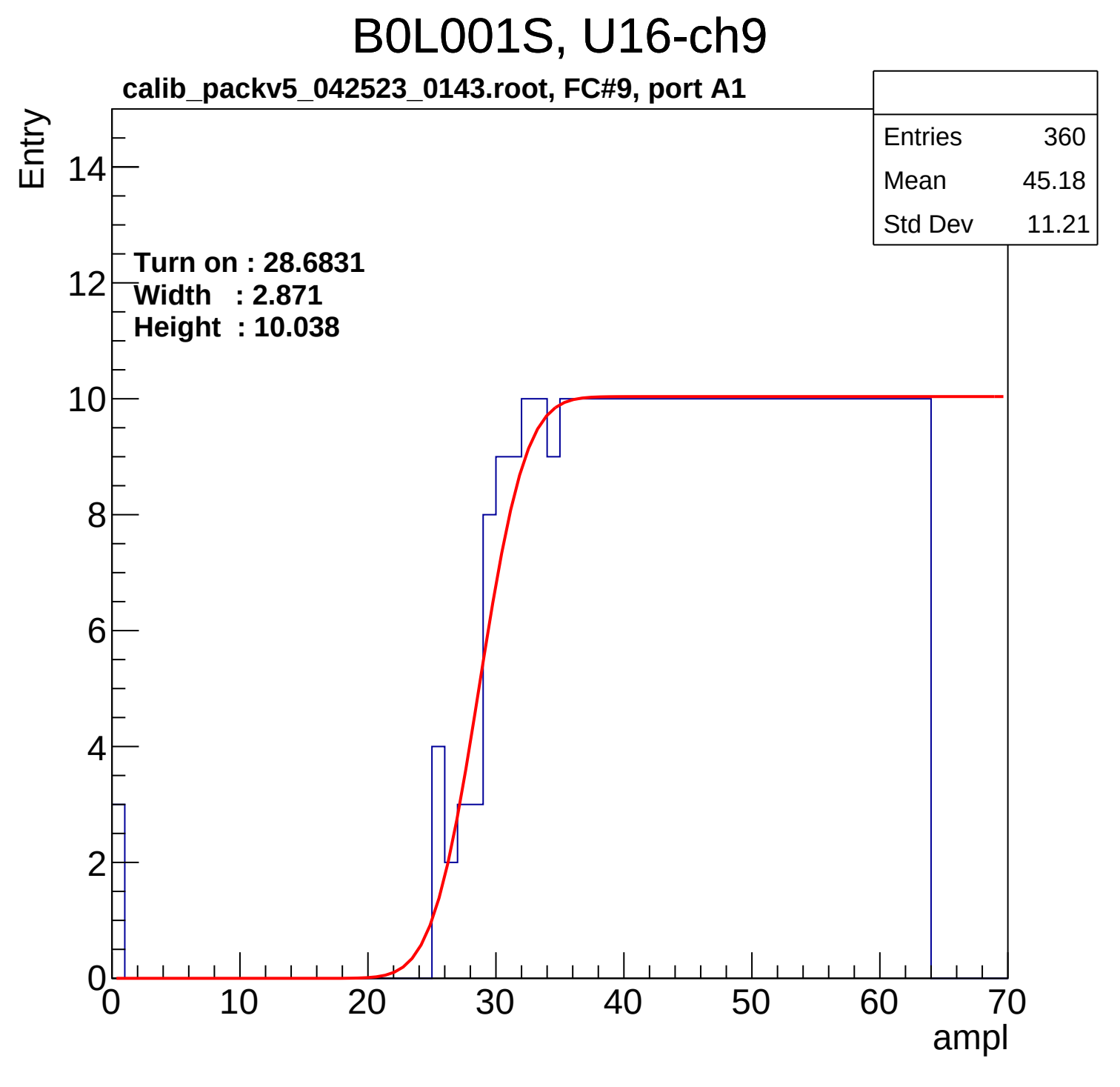
B0L001S, U16-ch9
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.18
Std Dev 11.21
Turn on : 28.6831
Width : 2.871
Height : 10.038
Entry
ampl
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2
4
6
8
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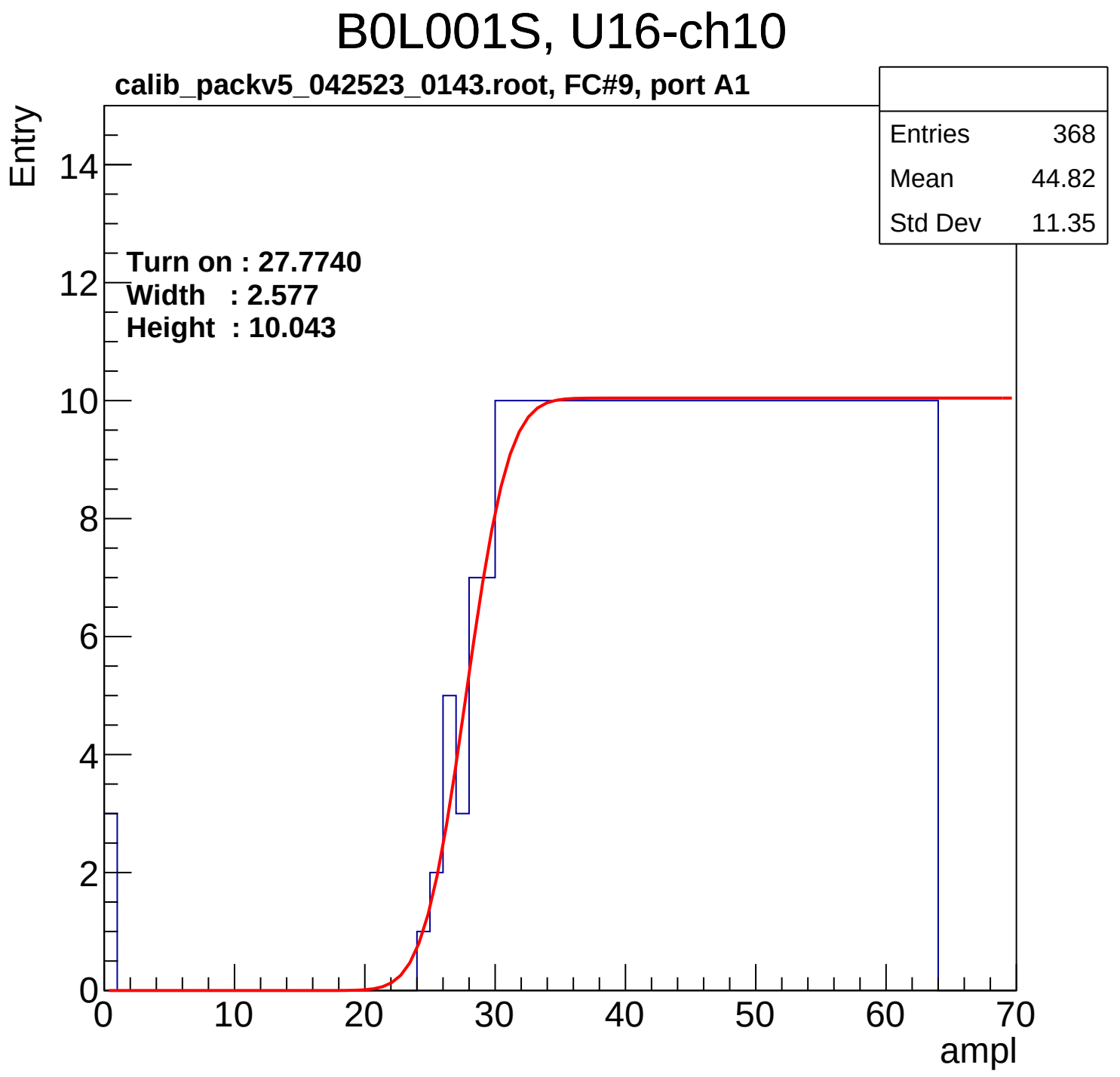
B0L001S, U16-ch10
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.82
Std Dev 11.35
Turn on : 27.7740
Width : 2.577
Height : 10.043
Entry
ampl
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2
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6
8
10
12
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0
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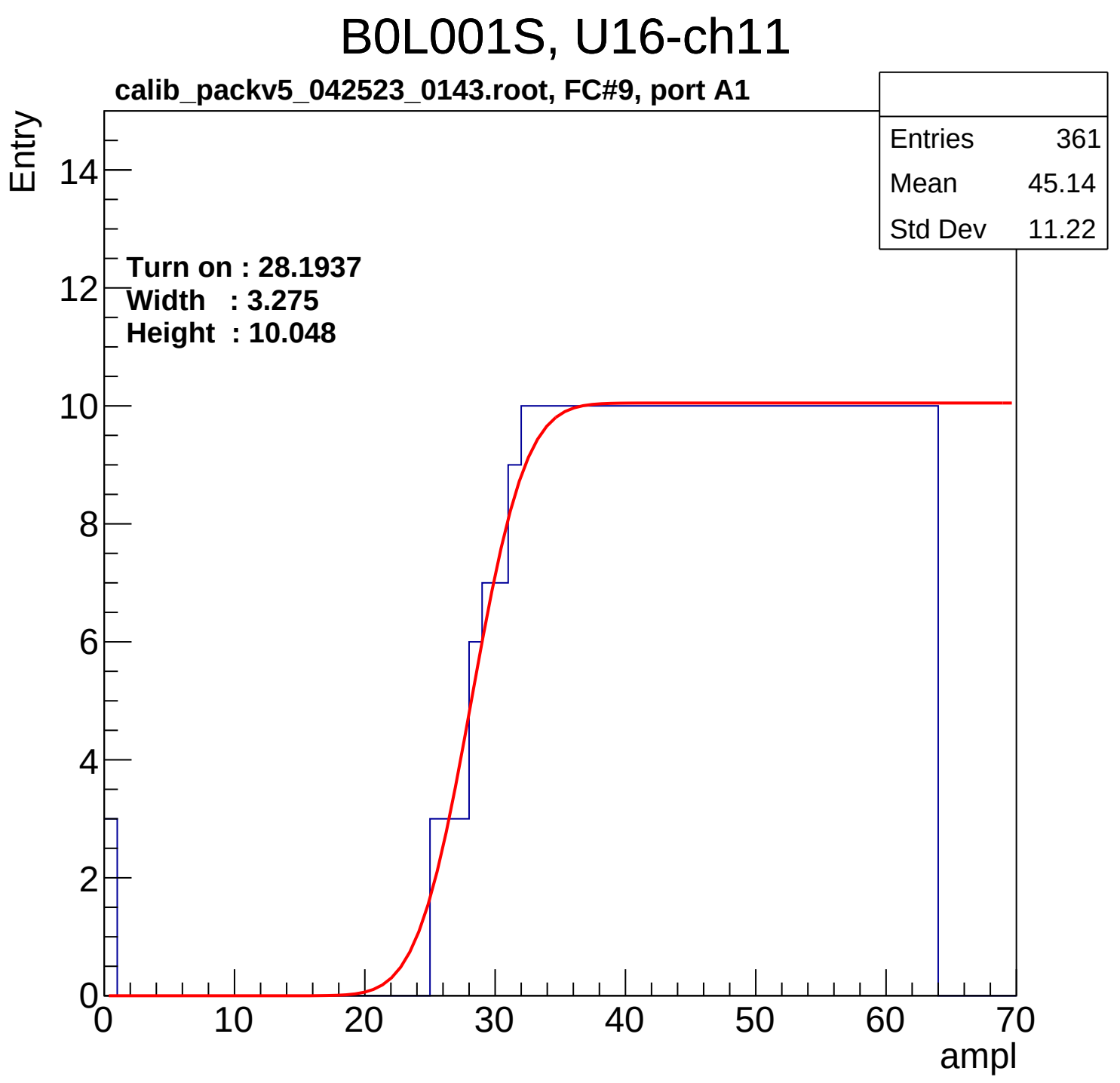
B0L001S, U16-ch11
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.14
Std Dev 11.22
Turn on : 28.1937
Width : 3.275
Height : 10.048
Entry
ampl
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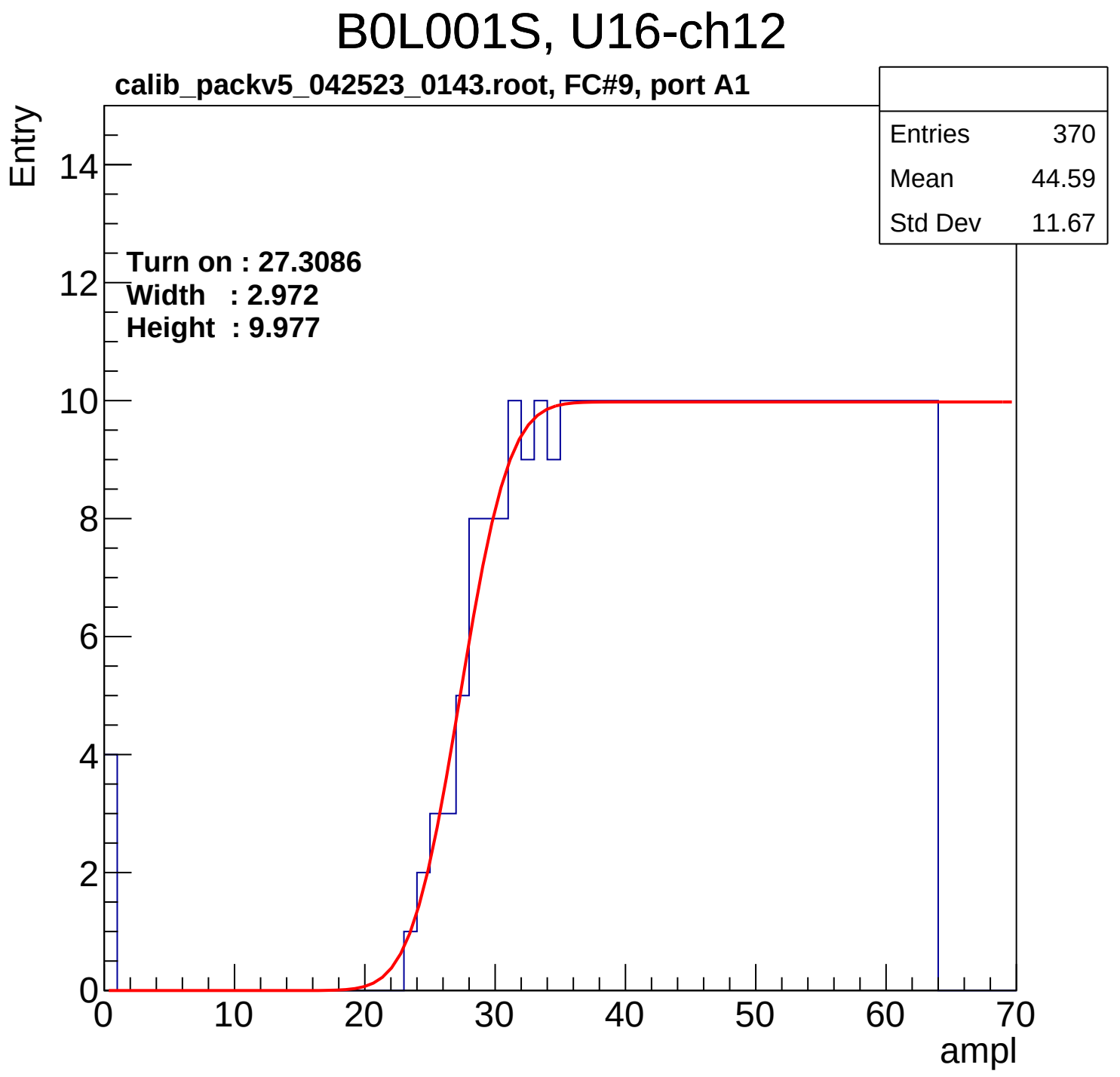
B0L001S, U16-ch12
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.59
Std Dev 11.67
Turn on : 27.3086
Width : 2.972
Height : 9.977
Entry
ampl
0
2
4
6
8
10
12
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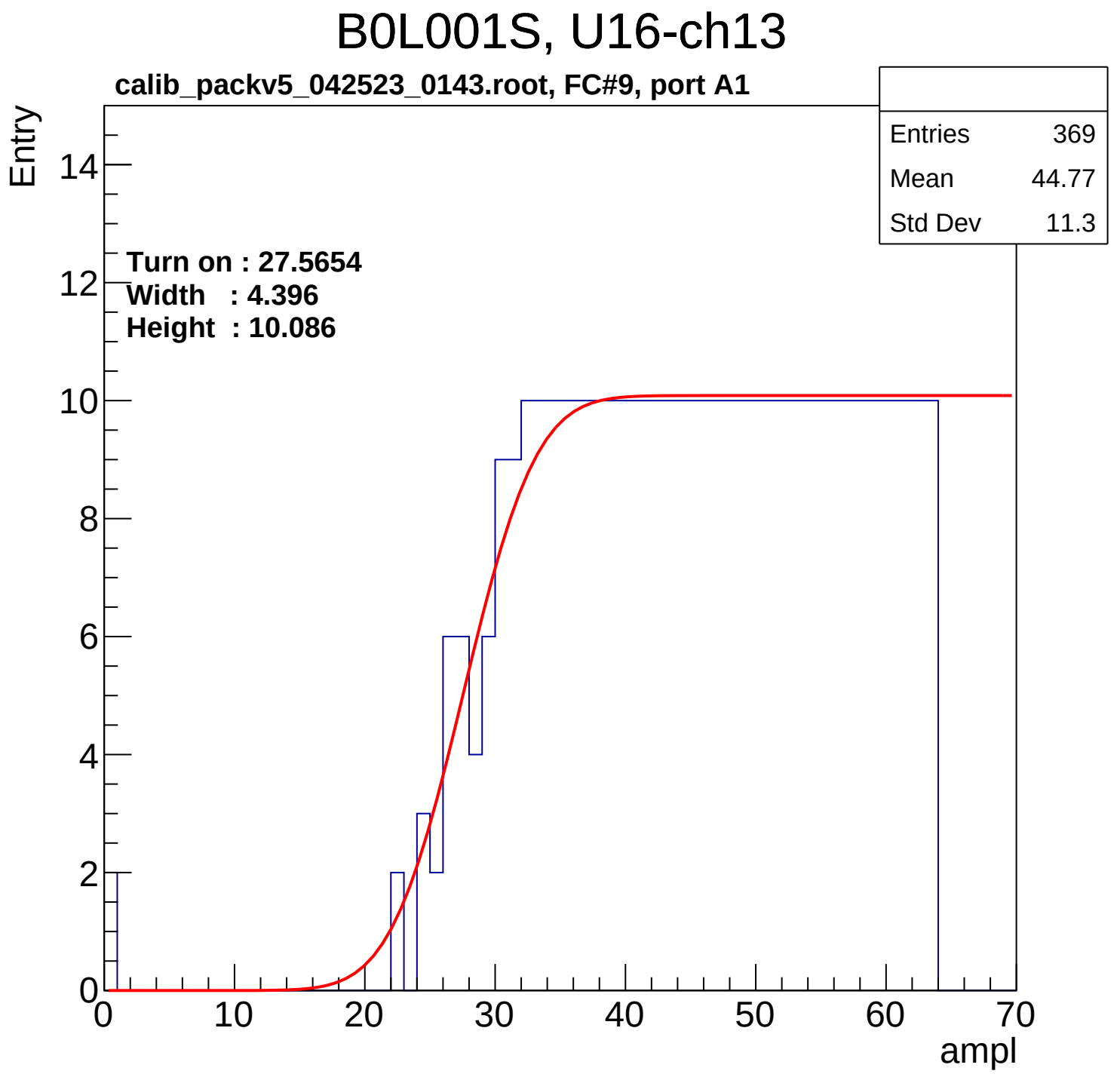
B0L001S, U16-ch13
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.77
Std Dev 11.3
Turn on : 27.5654
Width : 4.396
Height : 10.086
Entry
ampl
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6
8
10
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0
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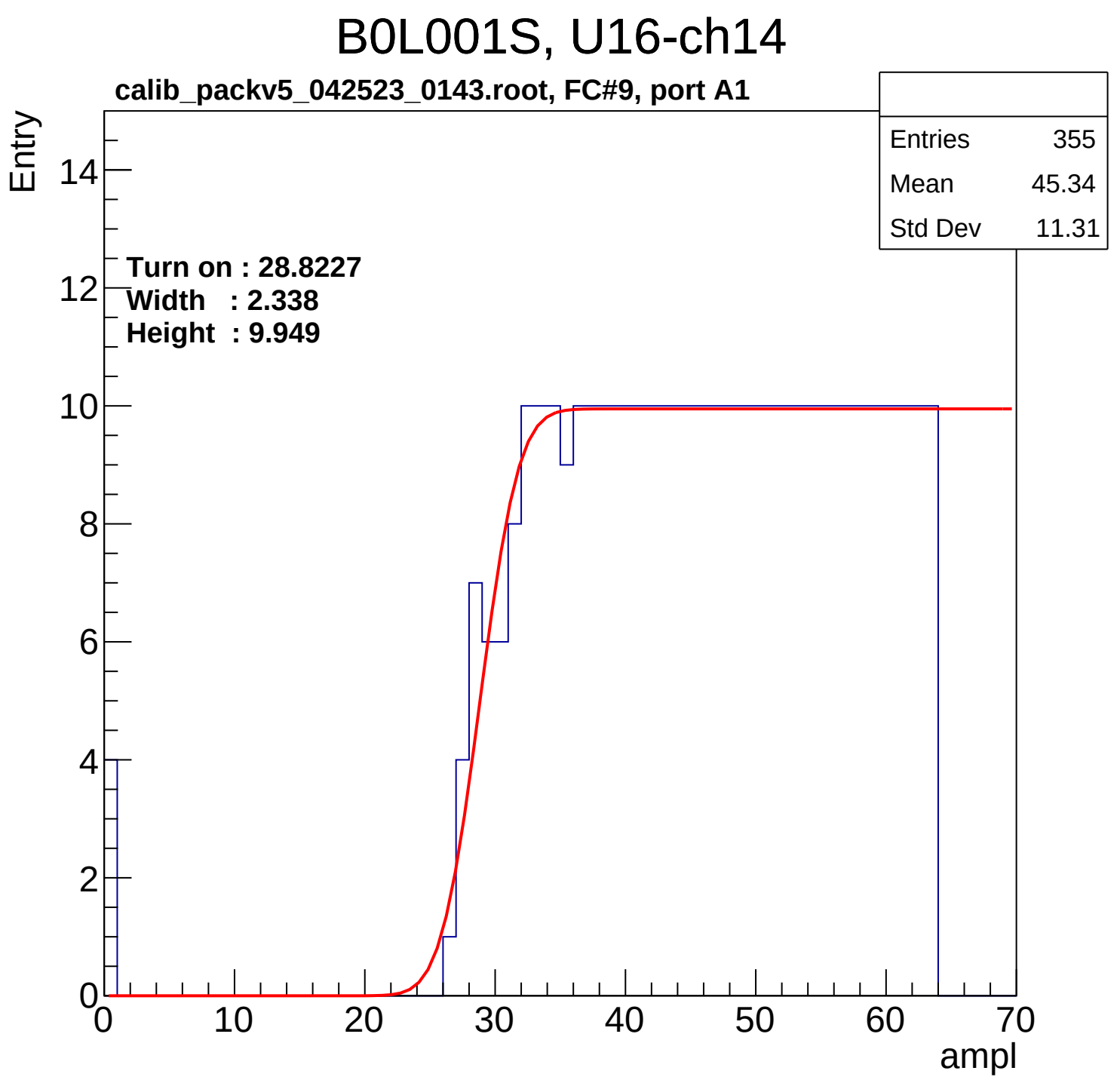
B0L001S, U16-ch14
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.34
Std Dev 11.31
Turn on : 28.8227
Width : 2.338
Height : 9.949
Entry
ampl
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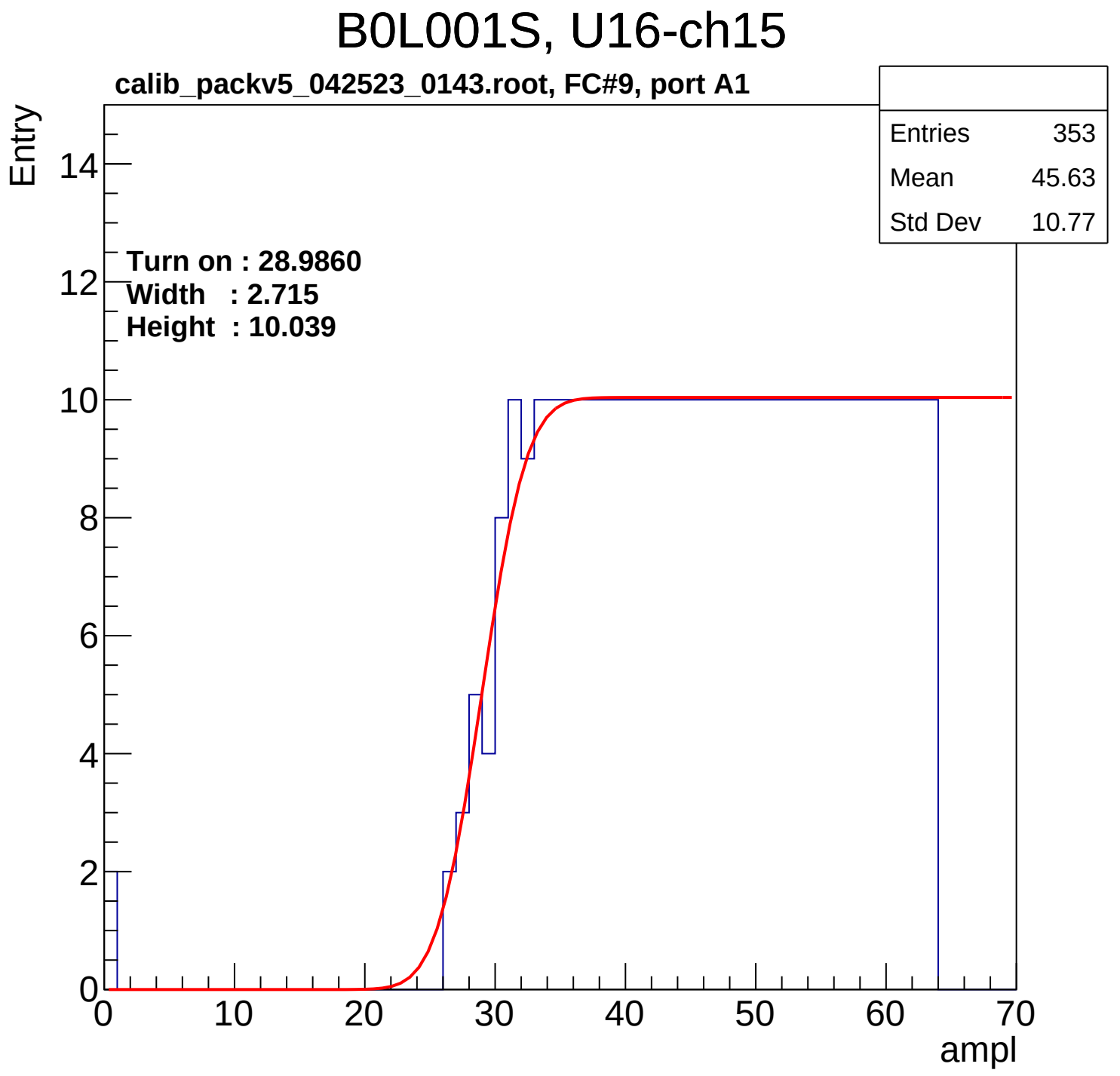
B0L001S, U16-ch15
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.63
Std Dev 10.77
Turn on : 28.9860
Width : 2.715
Height : 10.039
Entry
ampl
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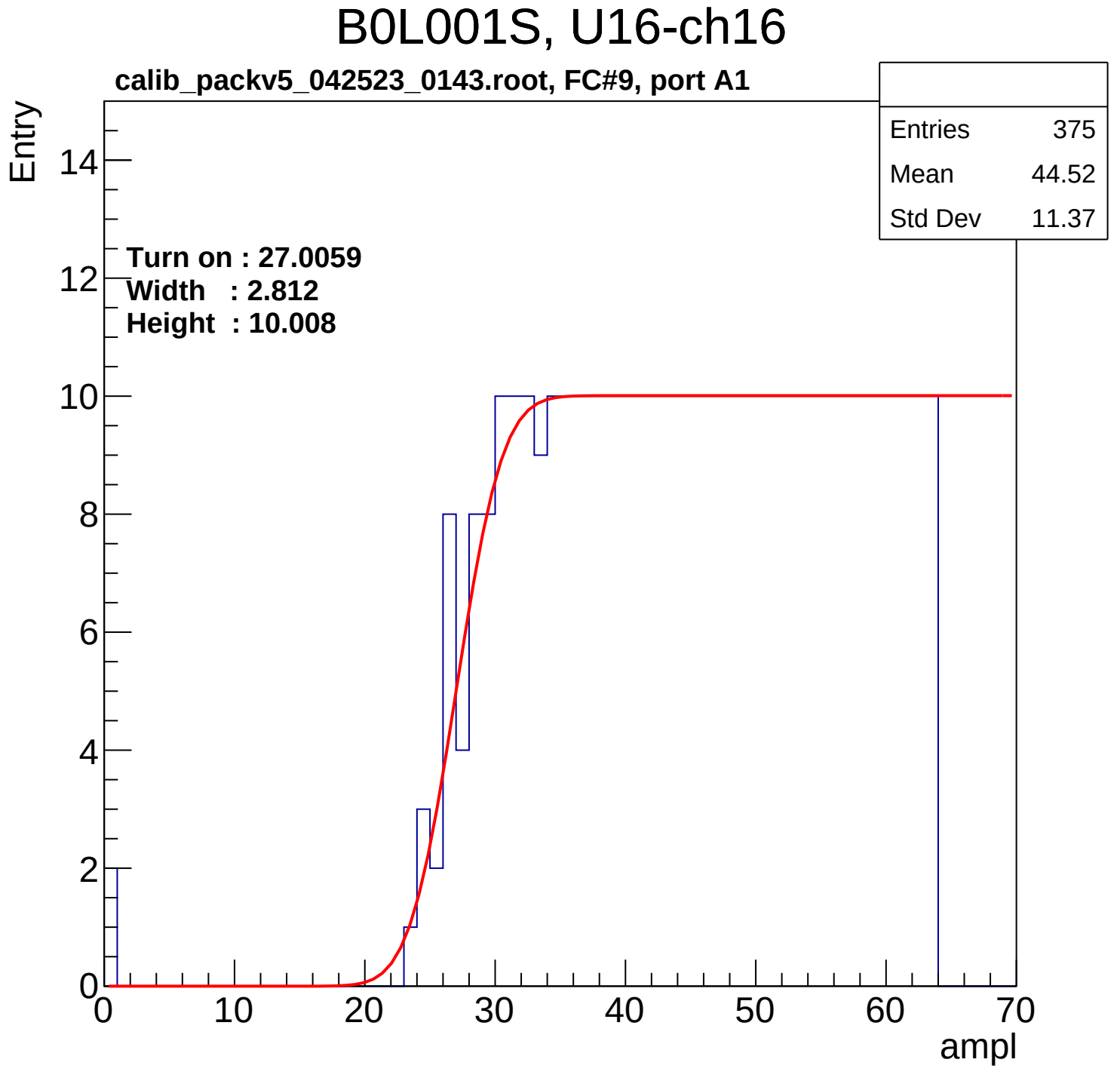
B0L001S, U16-ch16
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.52
Std Dev 11.37
Turn on : 27.0059
Width : 2.812
Height : 10.008
Entry
ampl
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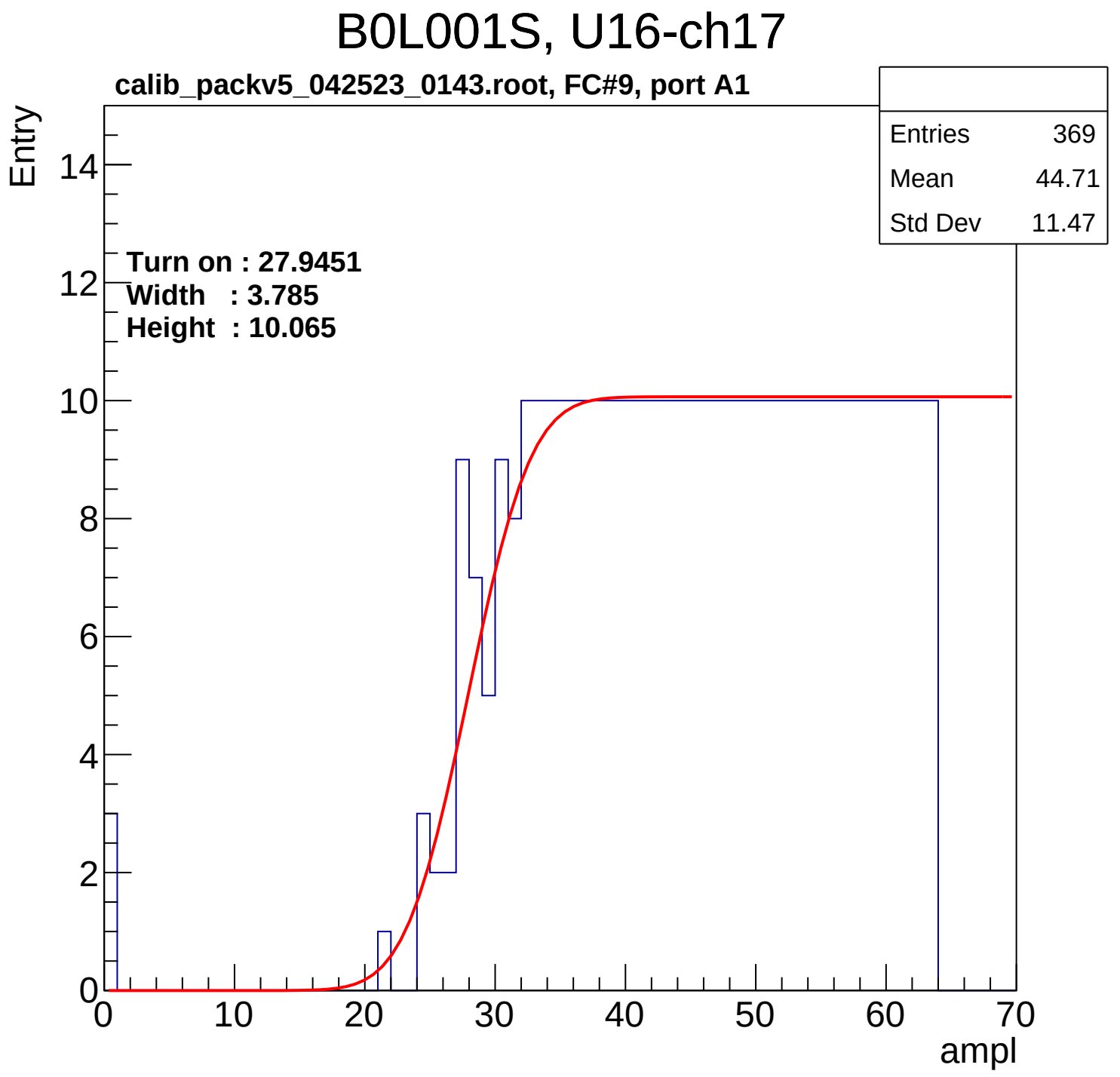
B0L001S, U16-ch17
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.71
Std Dev 11.47
Turn on : 27.9451
Width : 3.785
Height : 10.065
Entry
ampl
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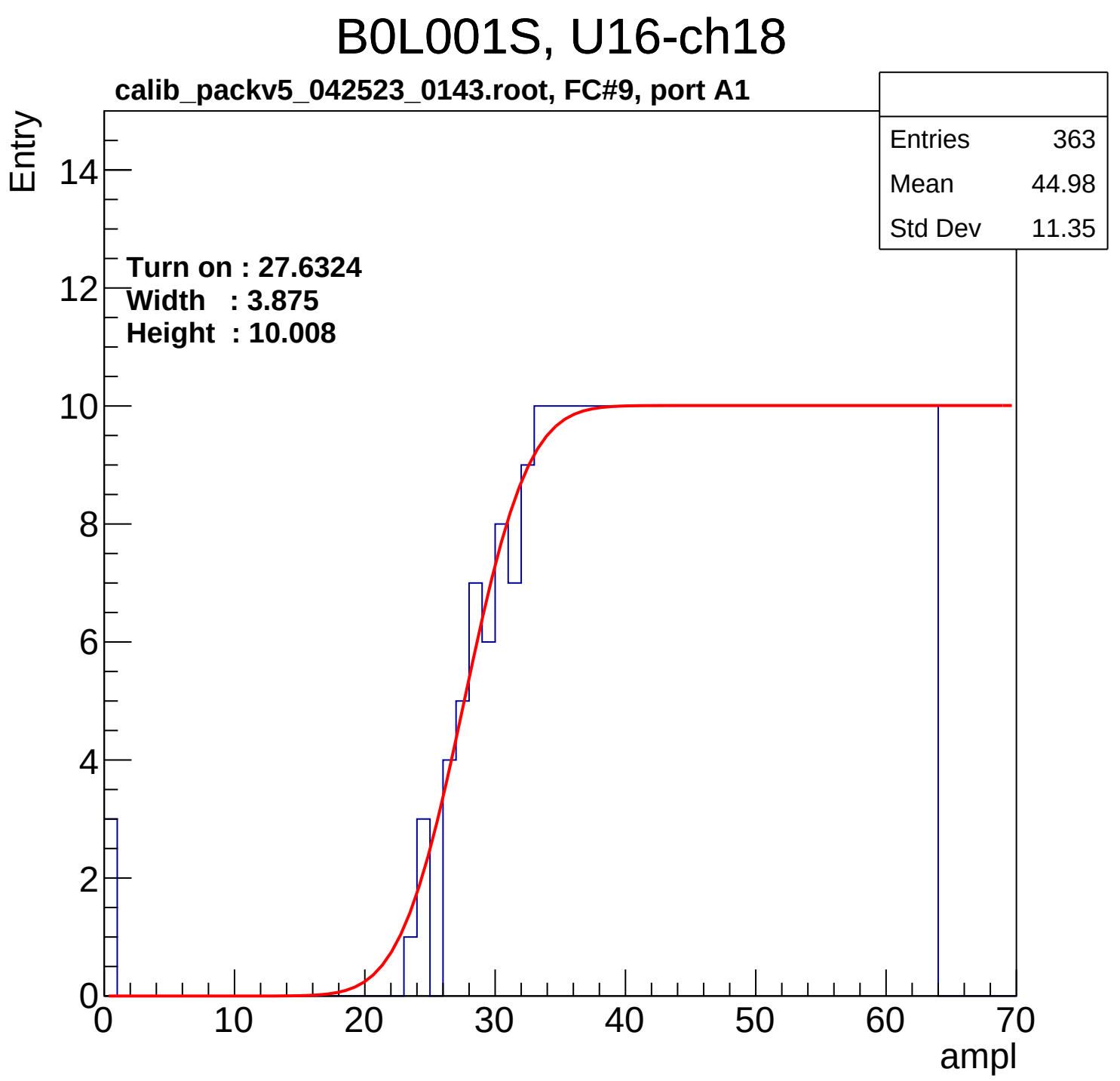
B0L001S, U16-ch18
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 44.98
Std Dev 11.35
Turn on : 27.6324
Width : 3.875
Height : 10.008
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ampl
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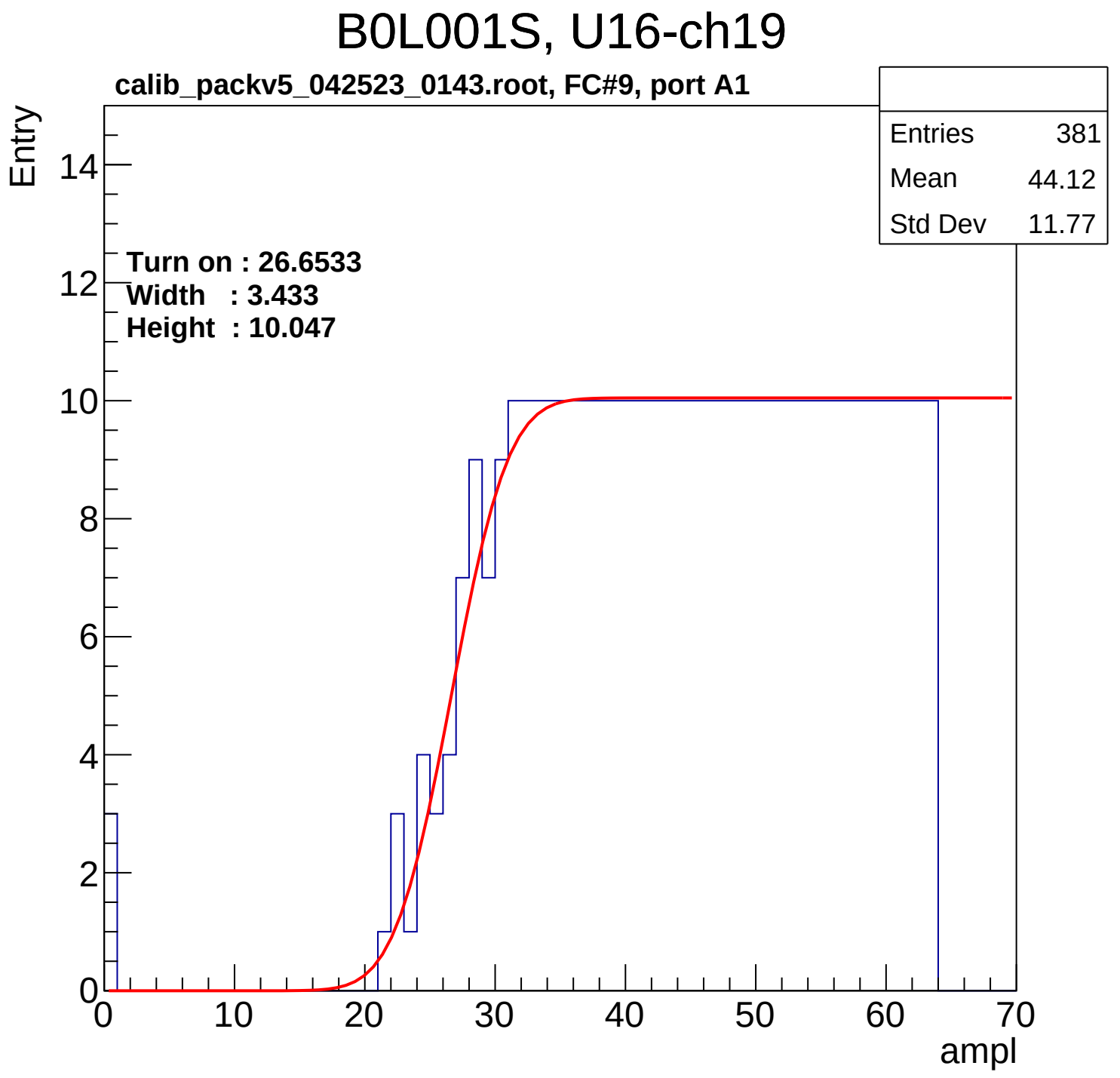
B0L001S, U16-ch19
calib_packv5_042523_0143.root, FC#9, port A1
Entries 381
Mean 44.12
Std Dev 11.77
Turn on : 26.6533
Width : 3.433
Height : 10.047
Entry
ampl
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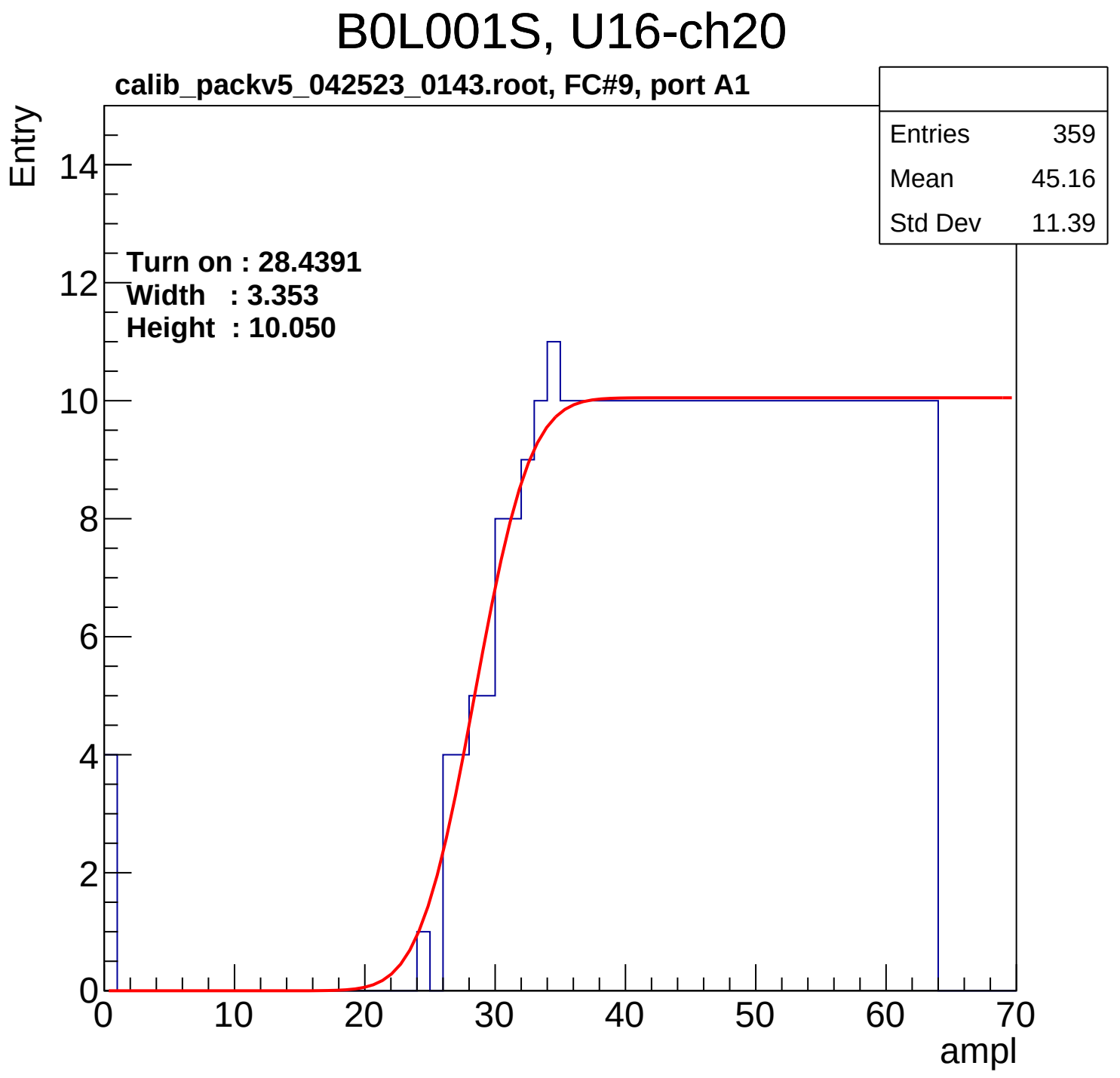
B0L001S, U16-ch20
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.16
Std Dev 11.39
Turn on : 28.4391
Width : 3.353
Height : 10.050
Entry
ampl
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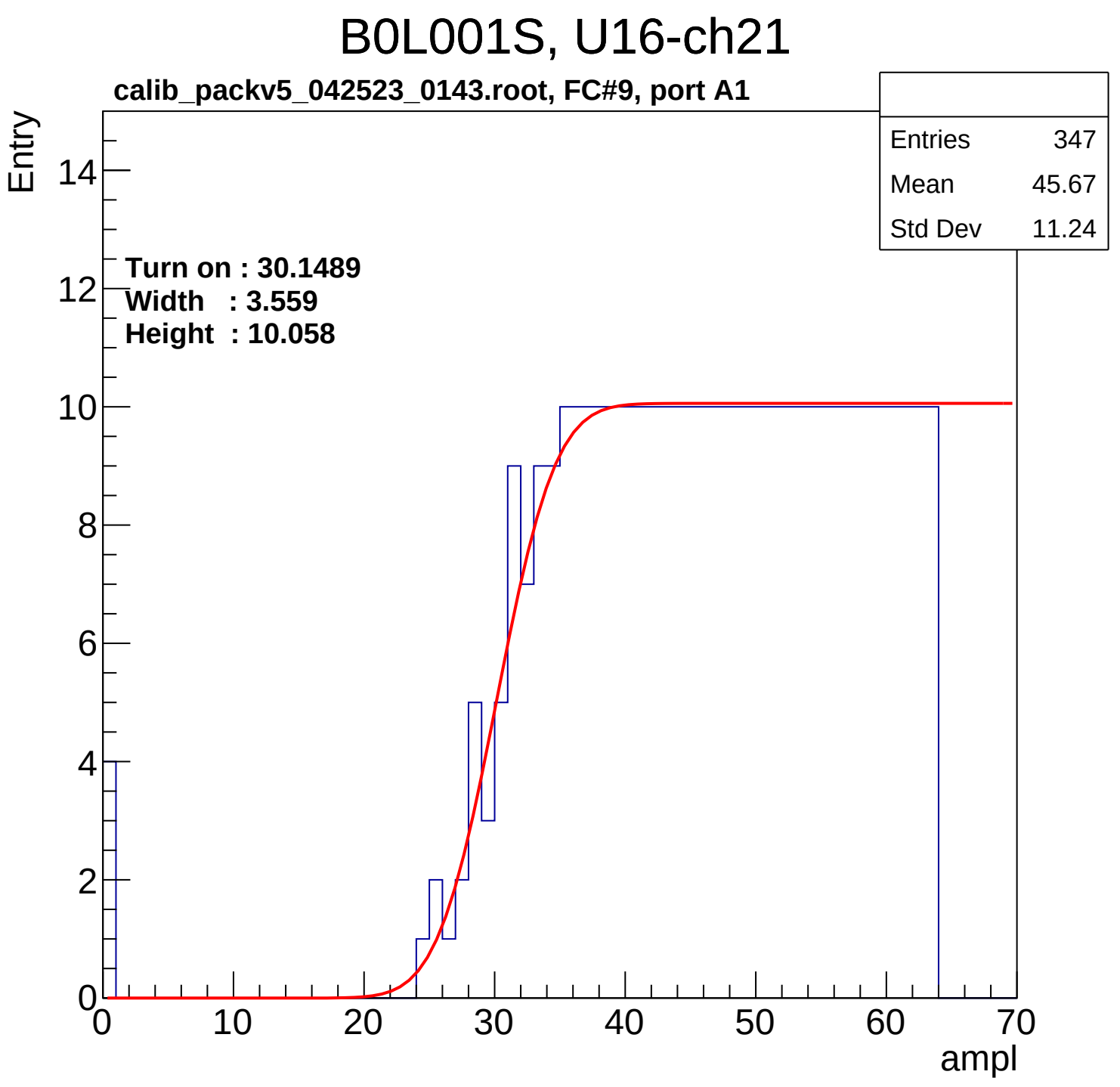
B0L001S, U16-ch21
calib_packv5_042523_0143.root, FC#9, port A1
Entries 347
Mean 45.67
Std Dev 11.24
Turn on : 30.1489
Width : 3.559
Height : 10.058
Entry
ampl
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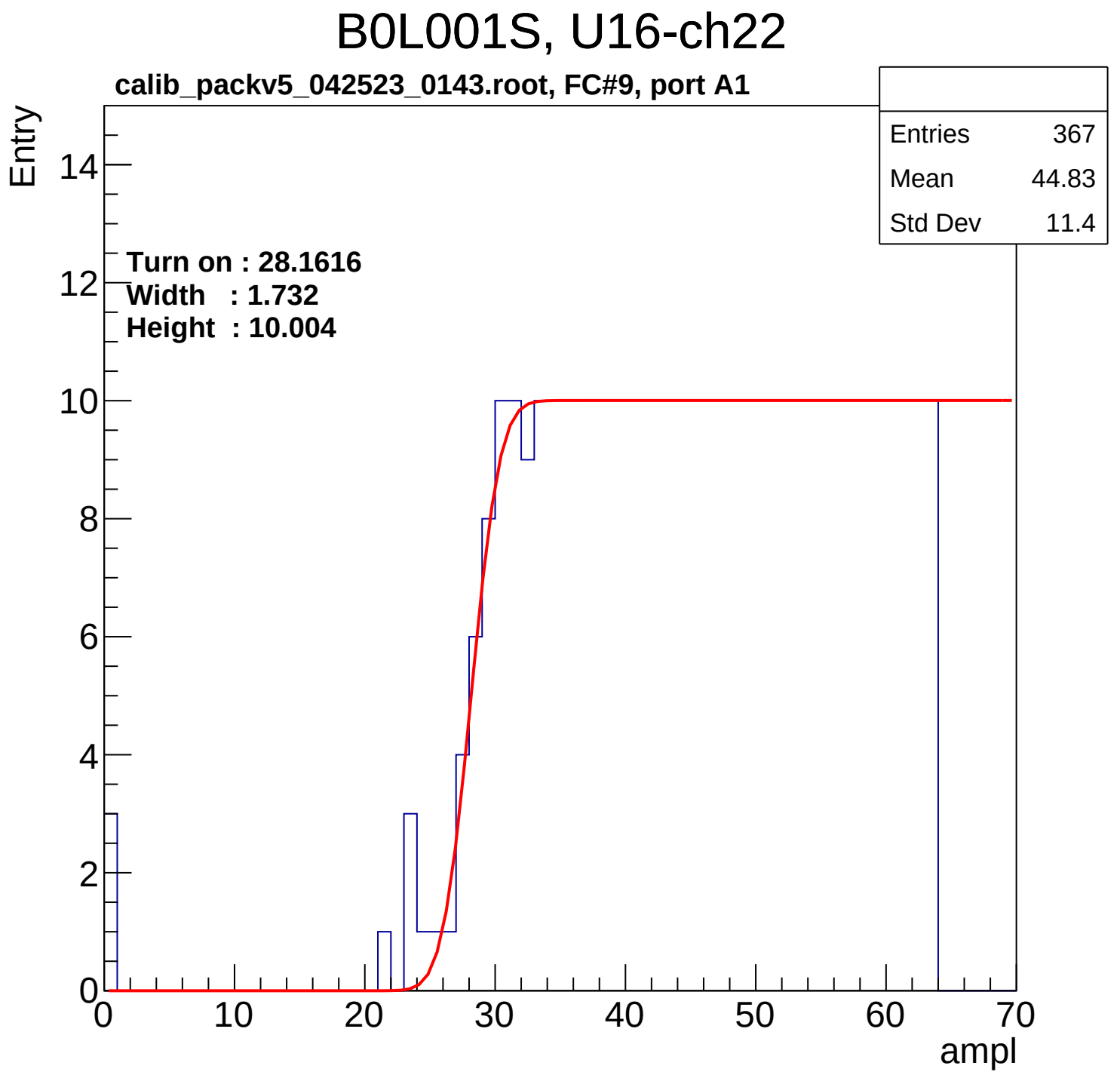
B0L001S, U16-ch22
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.83
Std Dev 11.4
Turn on : 28.1616
Width : 1.732
Height : 10.004
Entry
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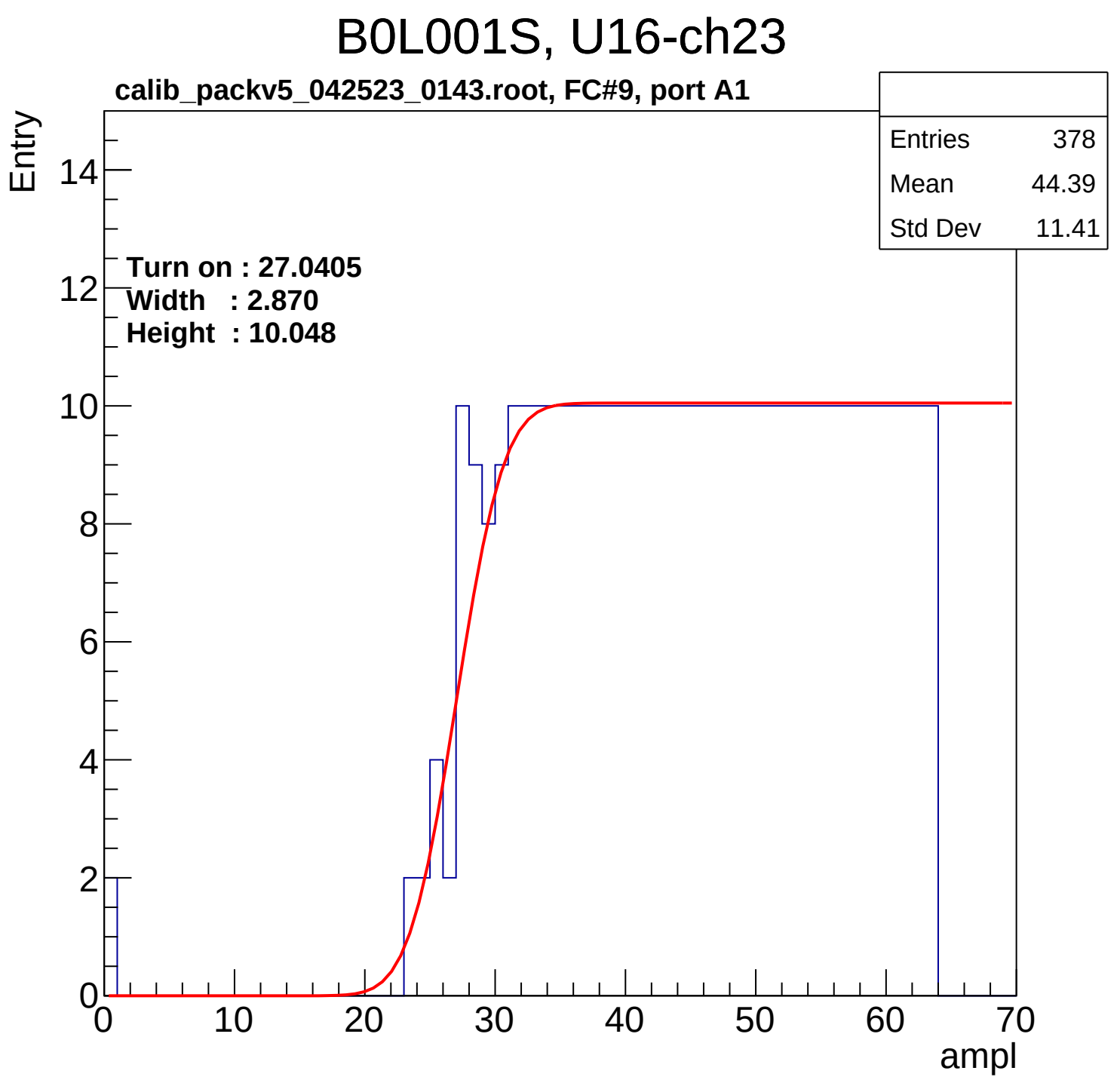
B0L001S, U16-ch23
calib_packv5_042523_0143.root, FC#9, port A1
Entries 378
Mean 44.39
Std Dev 11.41
Turn on : 27.0405
Width : 2.870
Height : 10.048
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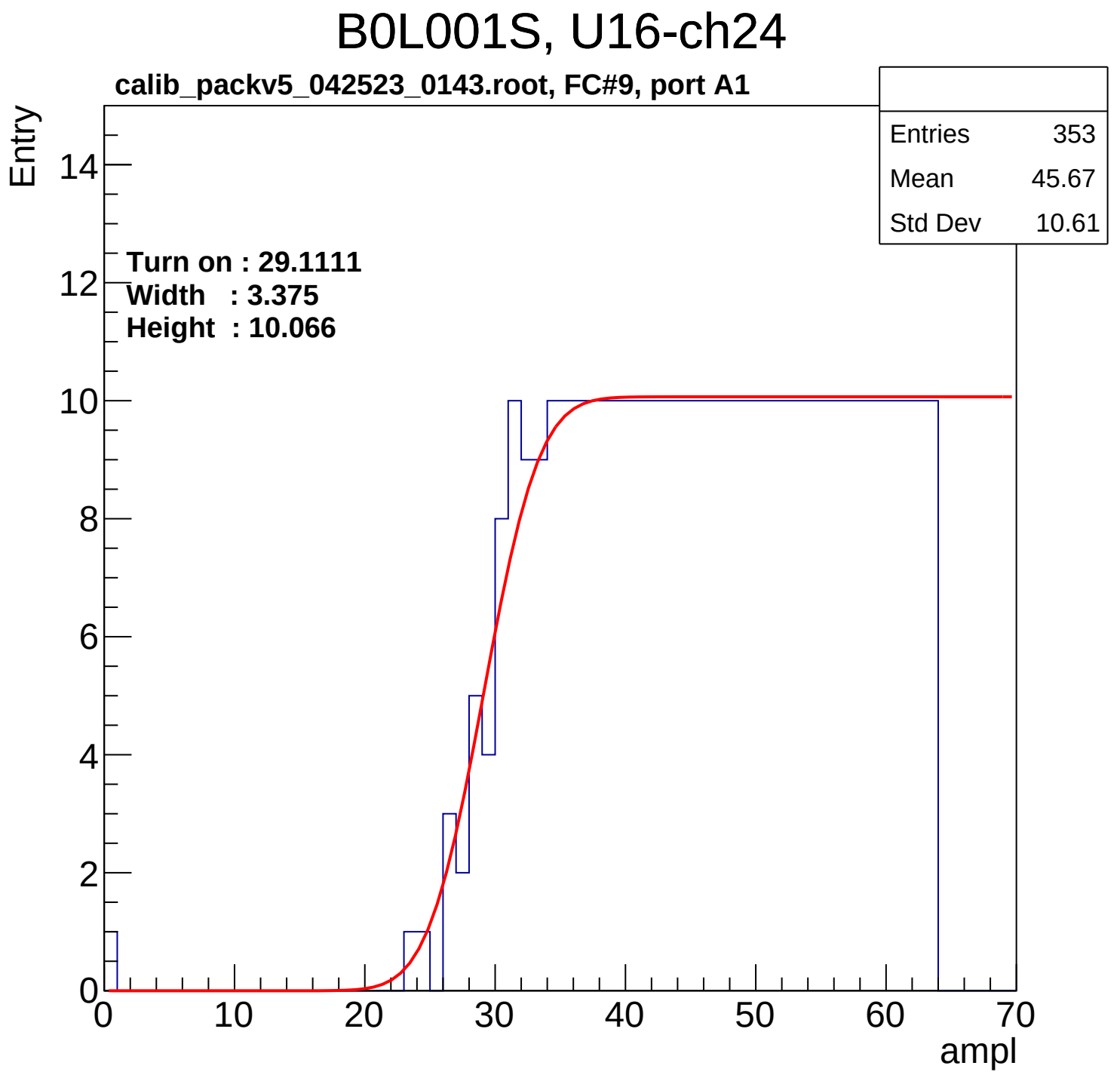
B0L001S, U16-ch24
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.67
Std Dev 10.61
Turn on : 29.1111
Width : 3.375
Height : 10.066
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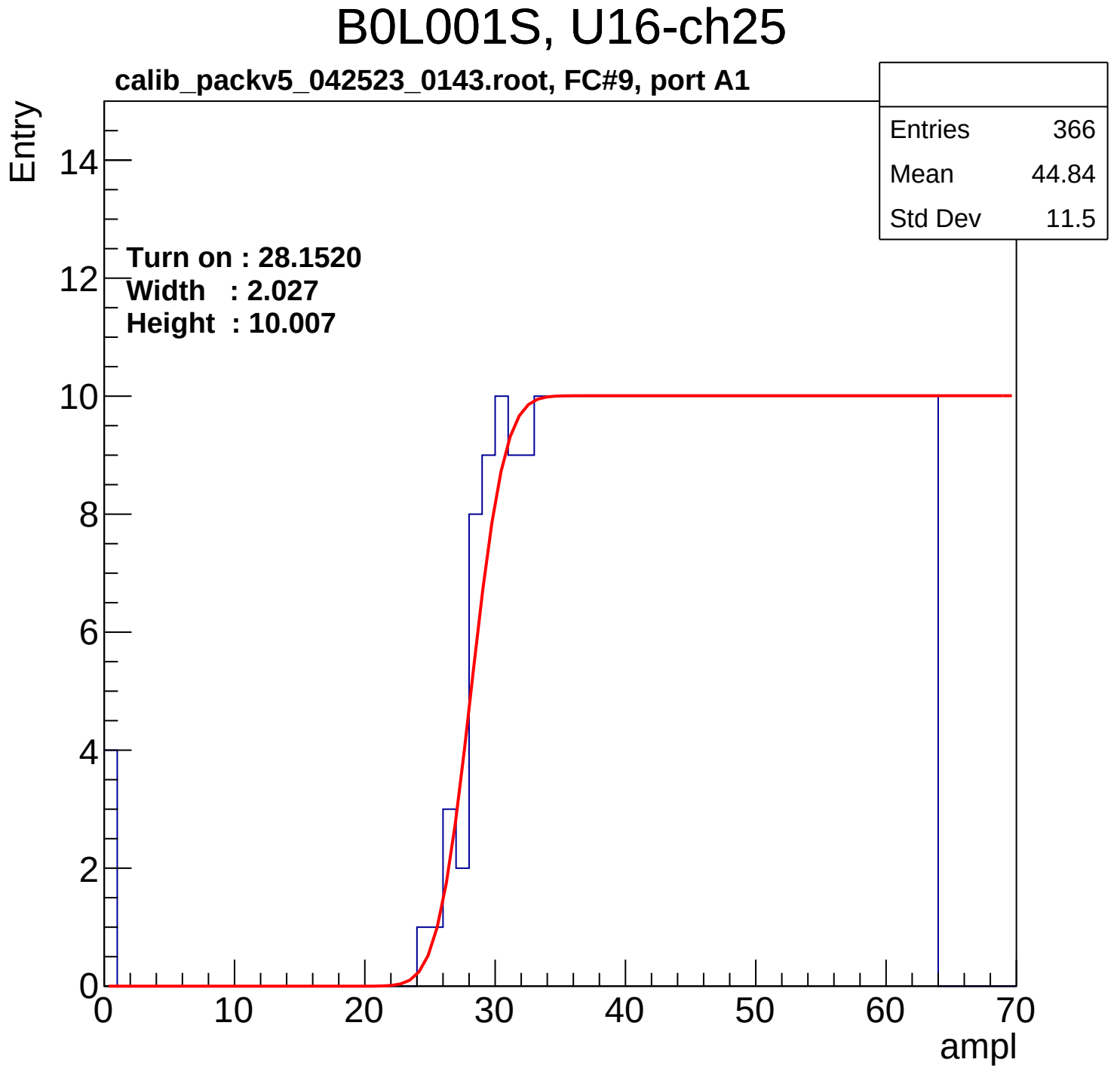
B0L001S, U16-ch25
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.84
Std Dev 11.5
Turn on : 28.1520
Width : 2.027
Height : 10.007
Entry
ampl
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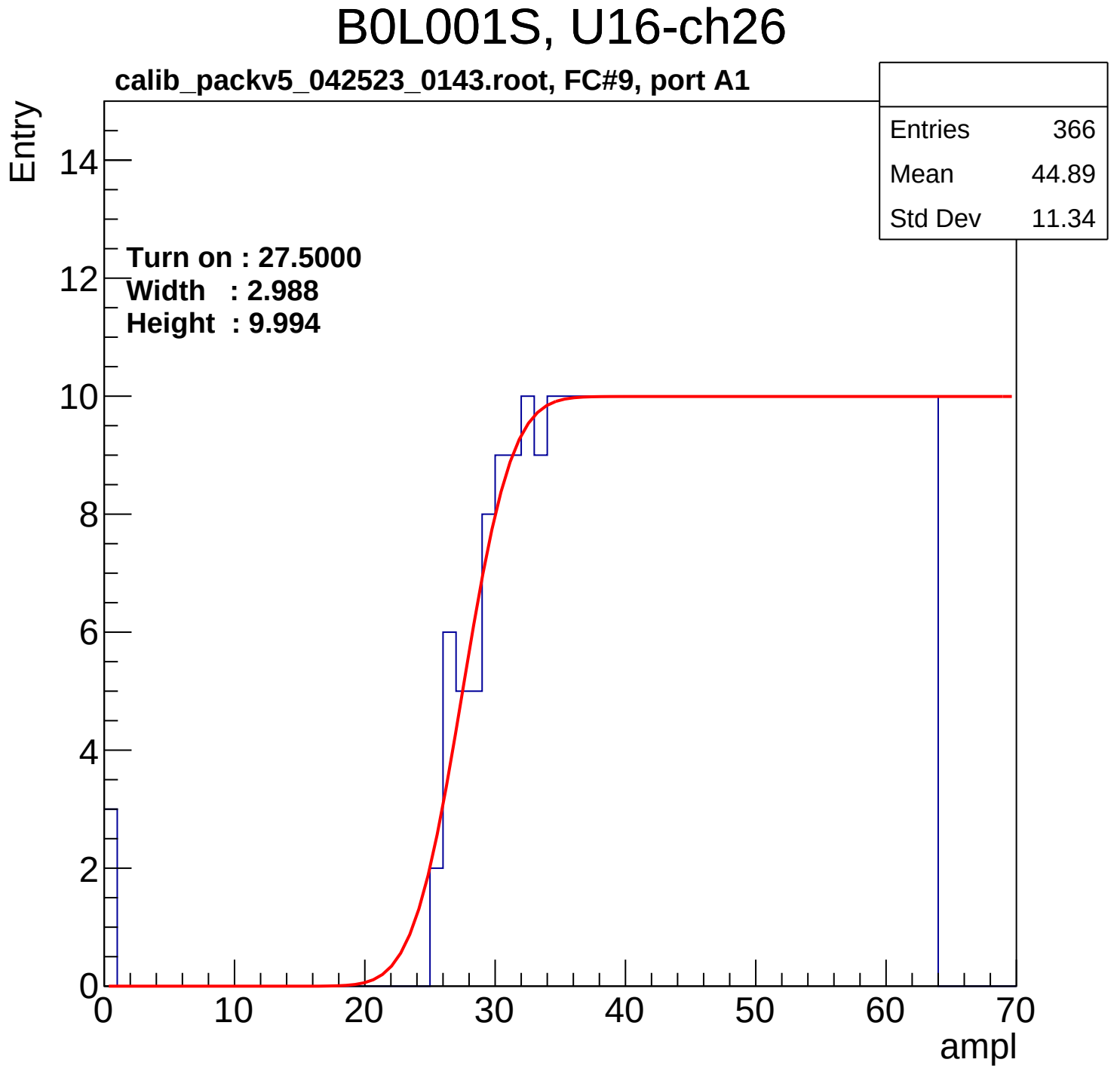
B0L001S, U16-ch26
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.89
Std Dev 11.34
Turn on : 27.5000
Width : 2.988
Height : 9.994
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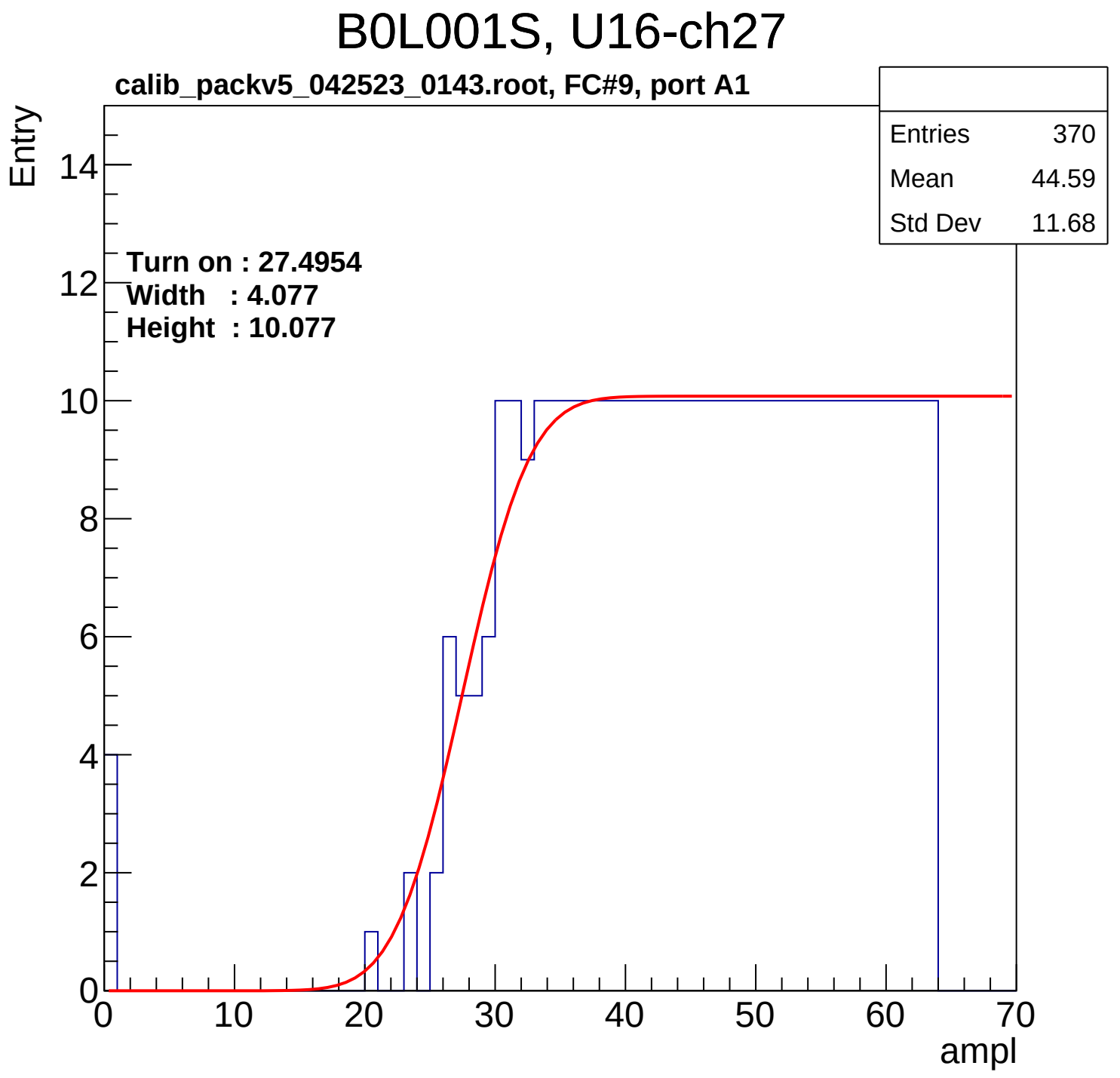
B0L001S, U16-ch27
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.59
Std Dev 11.68
Turn on : 27.4954
Width : 4.077
Height : 10.077
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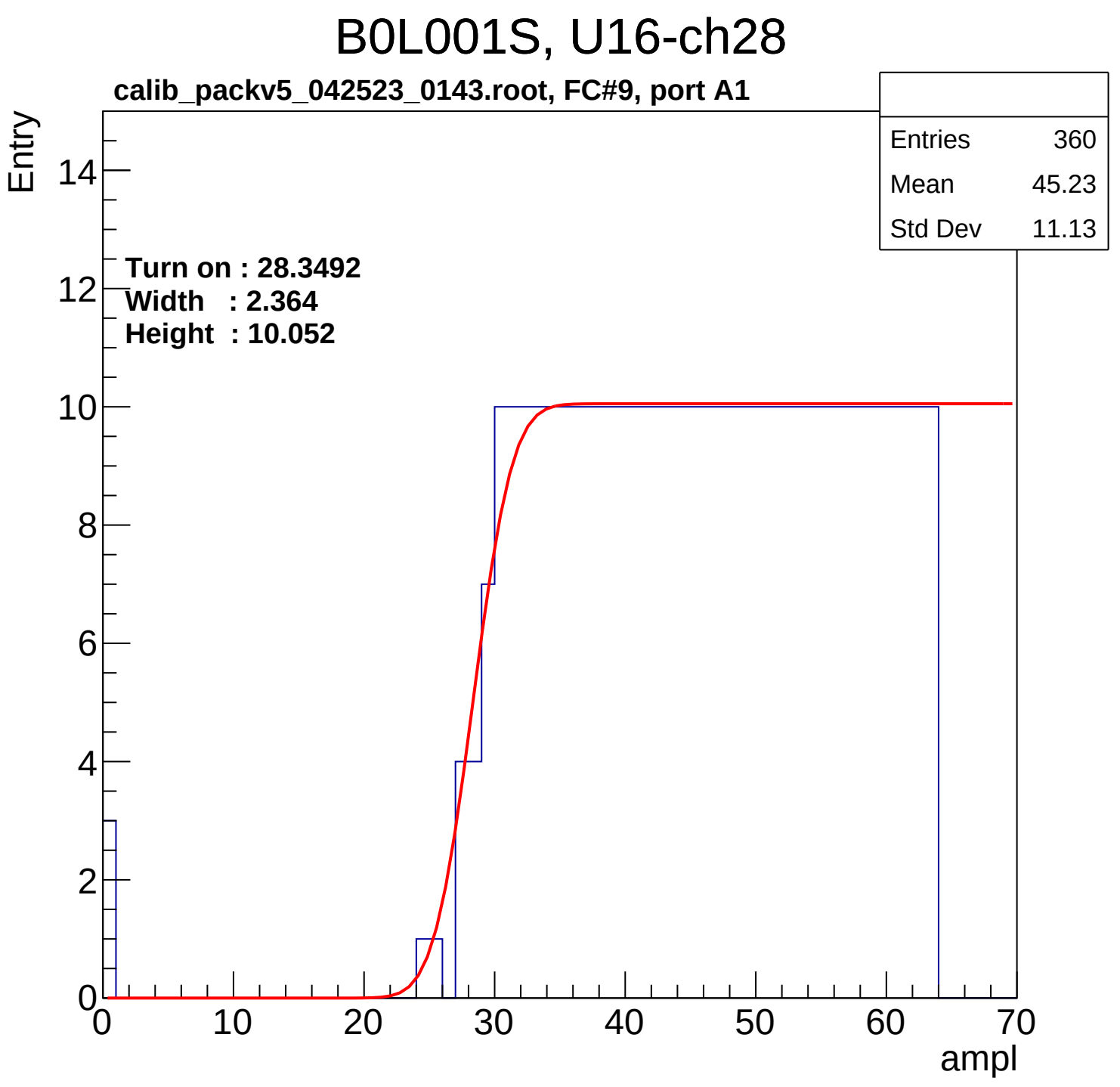
B0L001S, U16-ch28
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.23
Std Dev 11.13
Turn on : 28.3492
Width : 2.364
Height : 10.052
Entry
ampl
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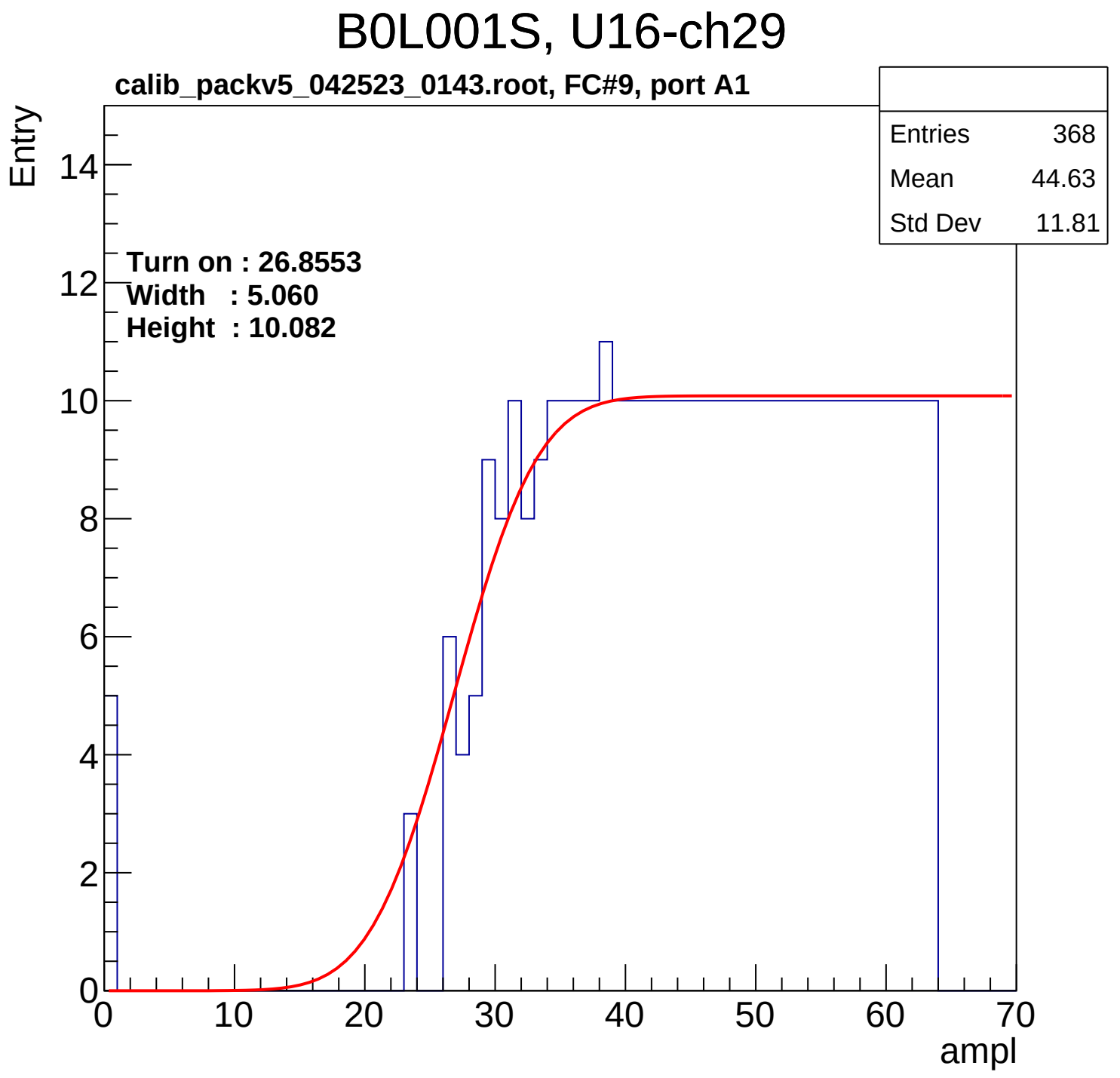
B0L001S, U16-ch29
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.63
Std Dev 11.81
Turn on : 26.8553
Width : 5.060
Height : 10.082
Entry
ampl
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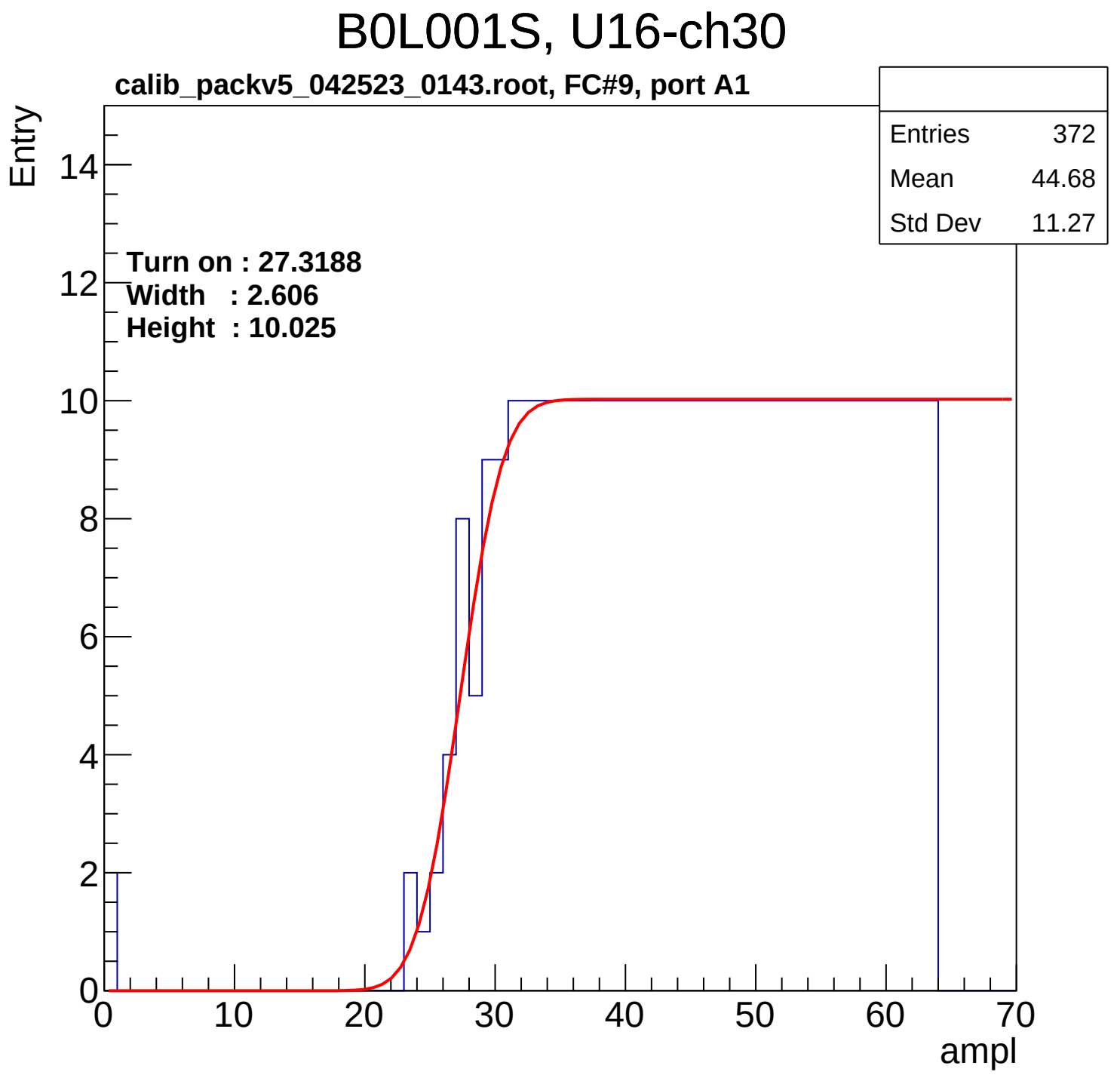
B0L001S, U16-ch30
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.68
Std Dev 11.27
Turn on : 27.3188
Width : 2.606
Height : 10.025
Entry
ampl
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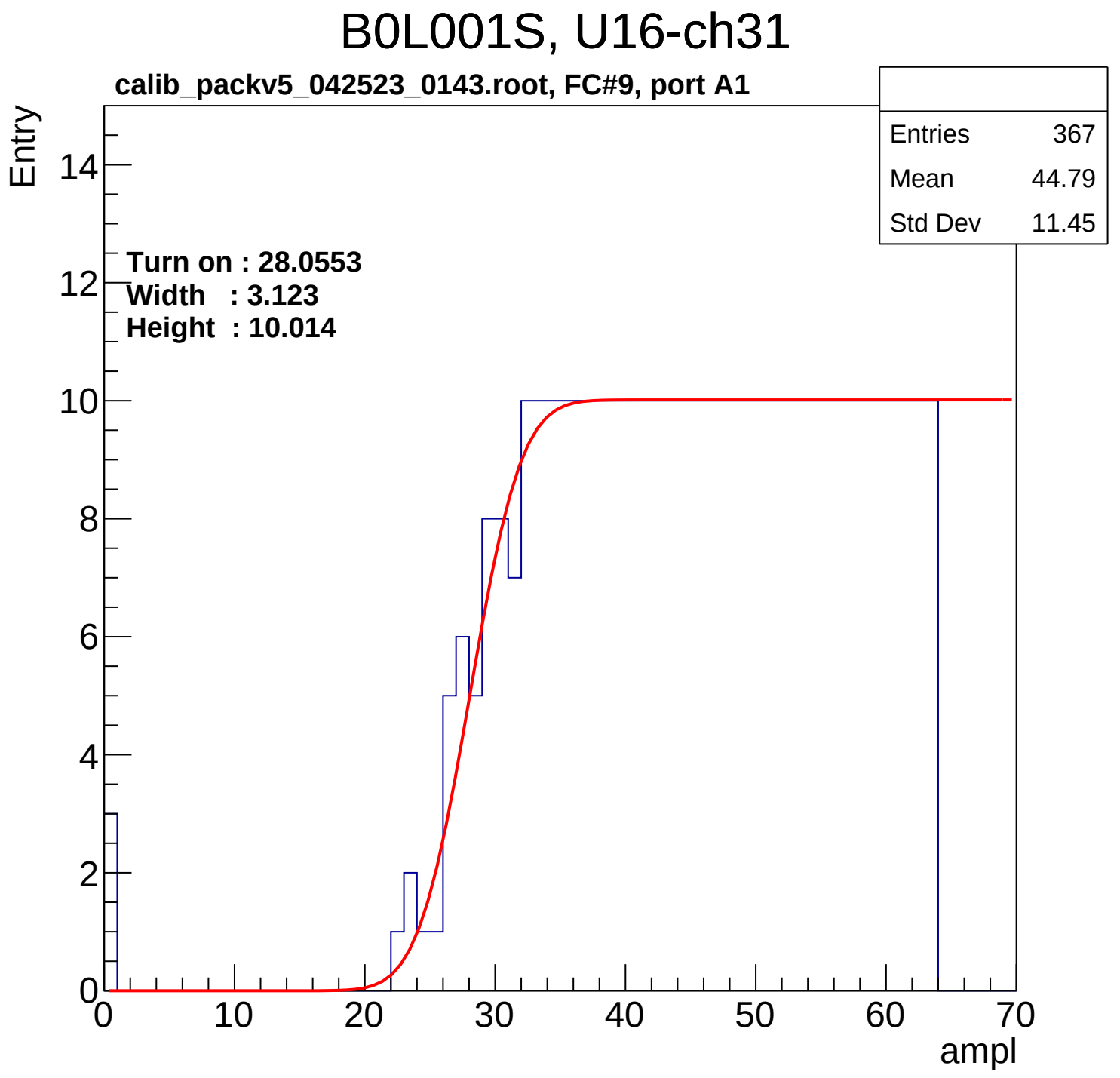
B0L001S, U16-ch31
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.79
Std Dev 11.45
Turn on : 28.0553
Width : 3.123
Height : 10.014
Entry
ampl
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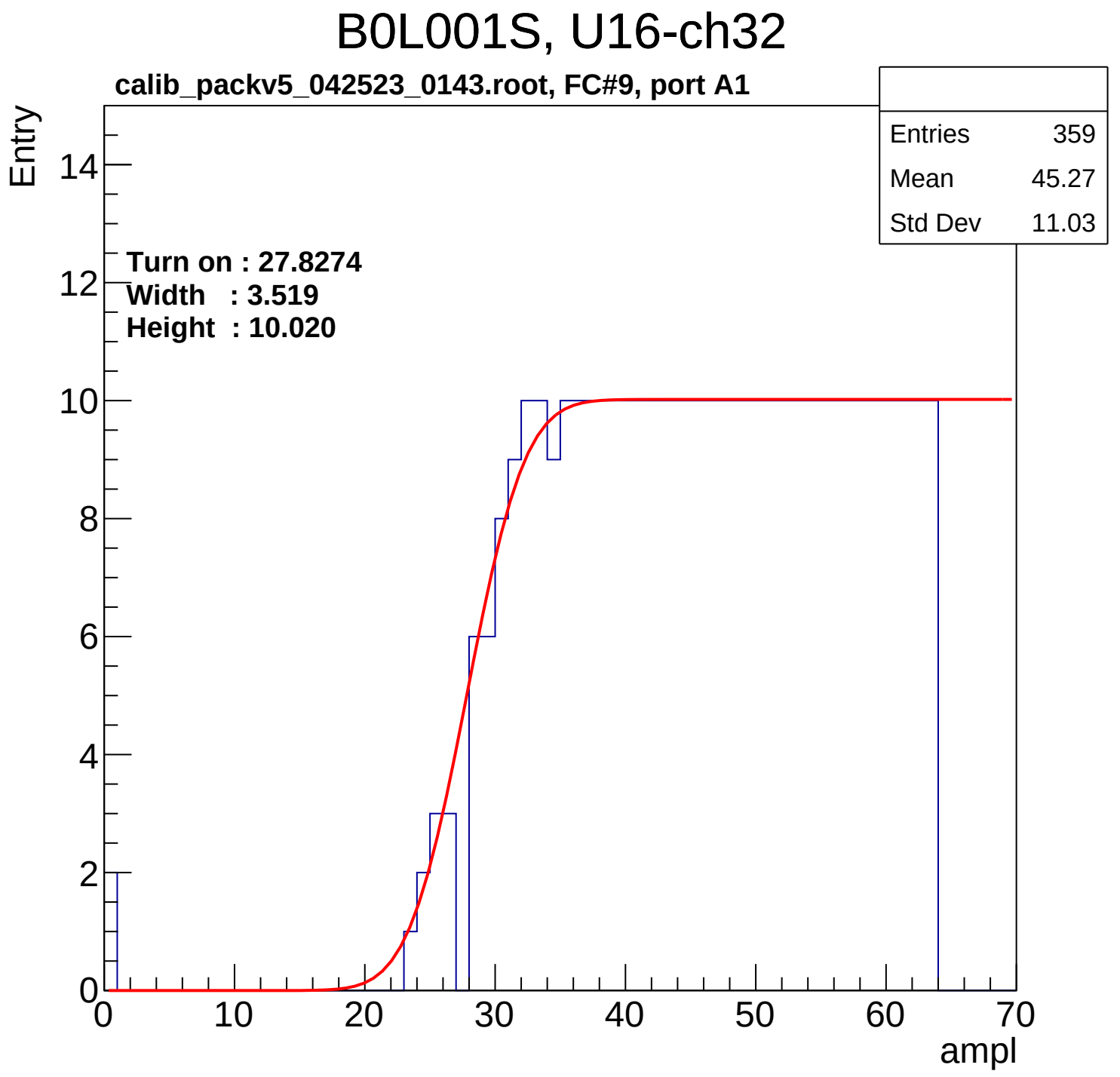
B0L001S, U16-ch32
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.27
Std Dev 11.03
Turn on : 27.8274
Width : 3.519
Height : 10.020
Entry
ampl
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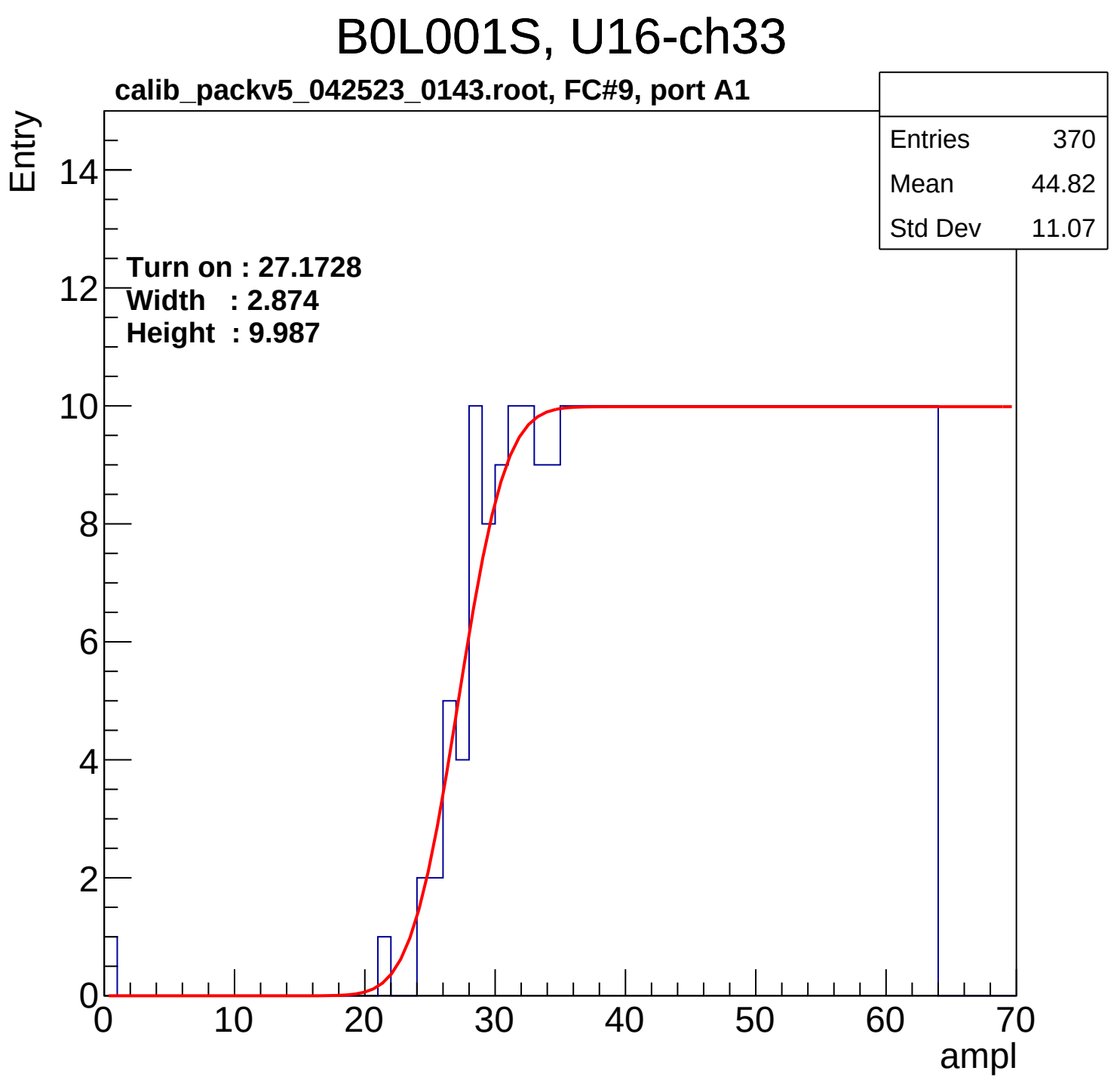
B0L001S, U16-ch33
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.82
Std Dev 11.07
Turn on : 27.1728
Width : 2.874
Height : 9.987
Entry
ampl
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4
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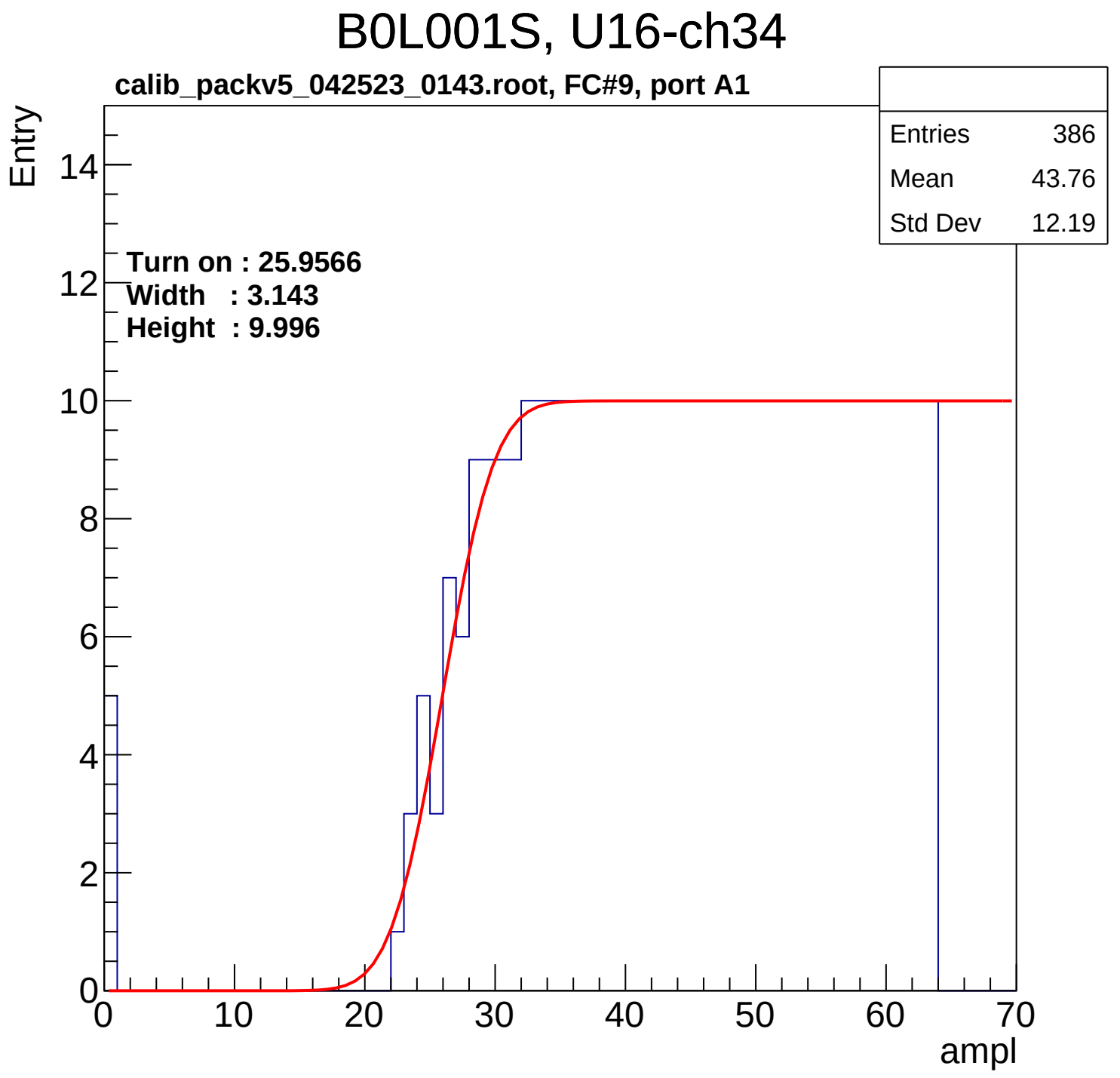
B0L001S, U16-ch34
calib_packv5_042523_0143.root, FC#9, port A1
Entries 386
Mean 43.76
Std Dev 12.19
Turn on : 25.9566
Width : 3.143
Height : 9.996
Entry
ampl
0
2
4
6
8
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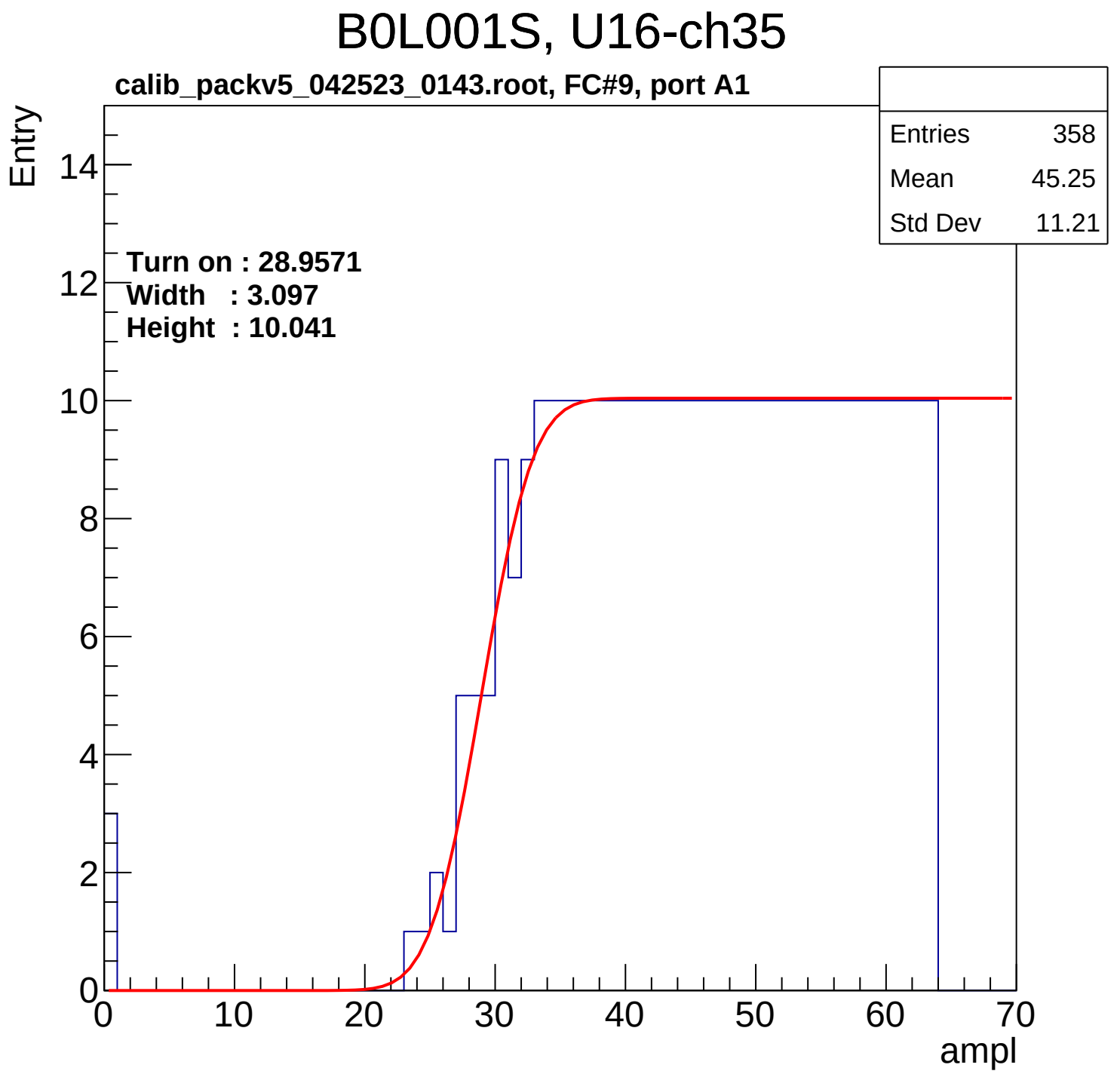
B0L001S, U16-ch35
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.25
Std Dev 11.21
Turn on : 28.9571
Width : 3.097
Height : 10.041
Entry
ampl
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2
4
6
8
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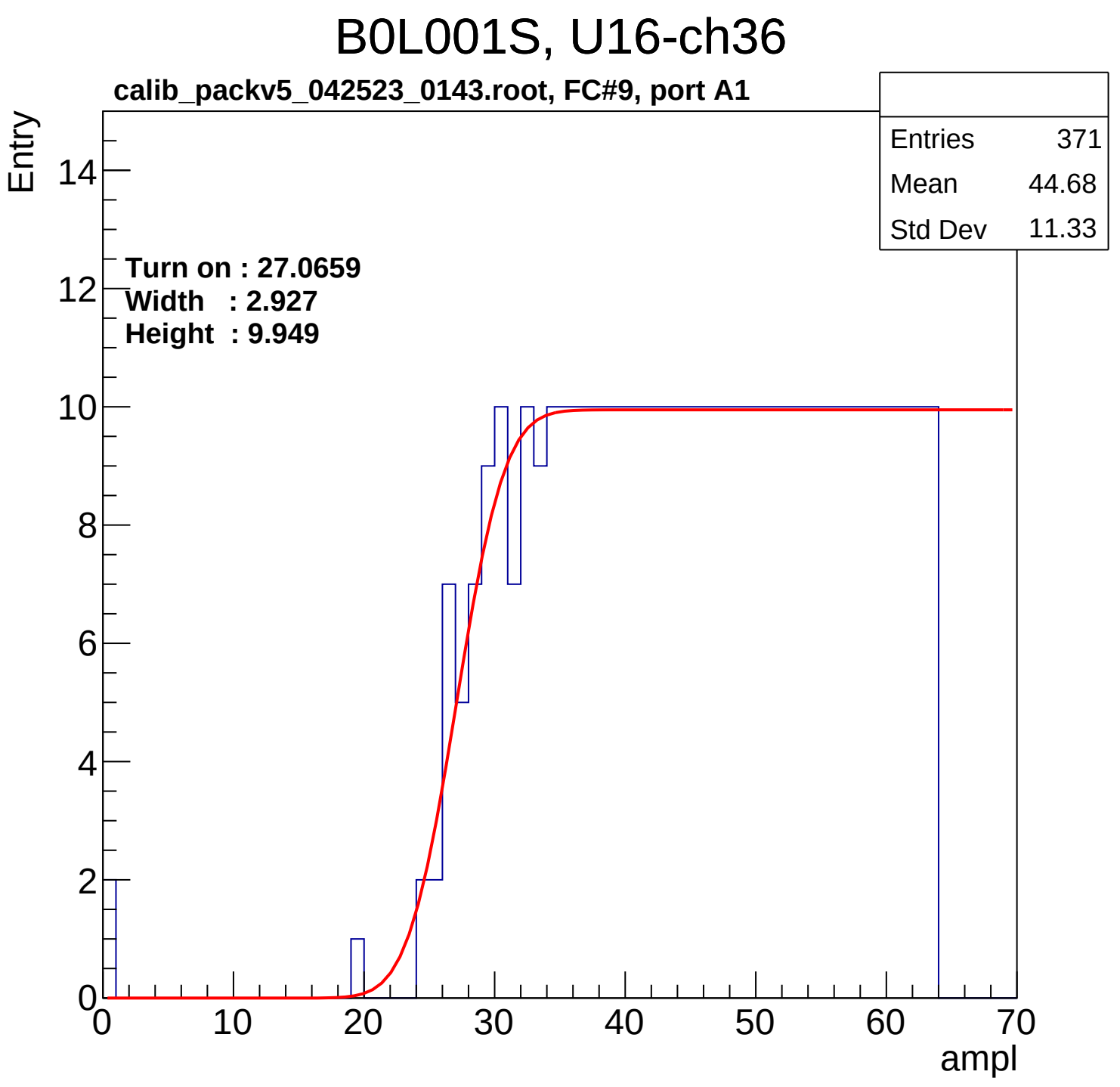
B0L001S, U16-ch36
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.68
Std Dev 11.33
Turn on : 27.0659
Width : 2.927
Height : 9.949
Entry
ampl
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2
4
6
8
10
12
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0
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40
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60
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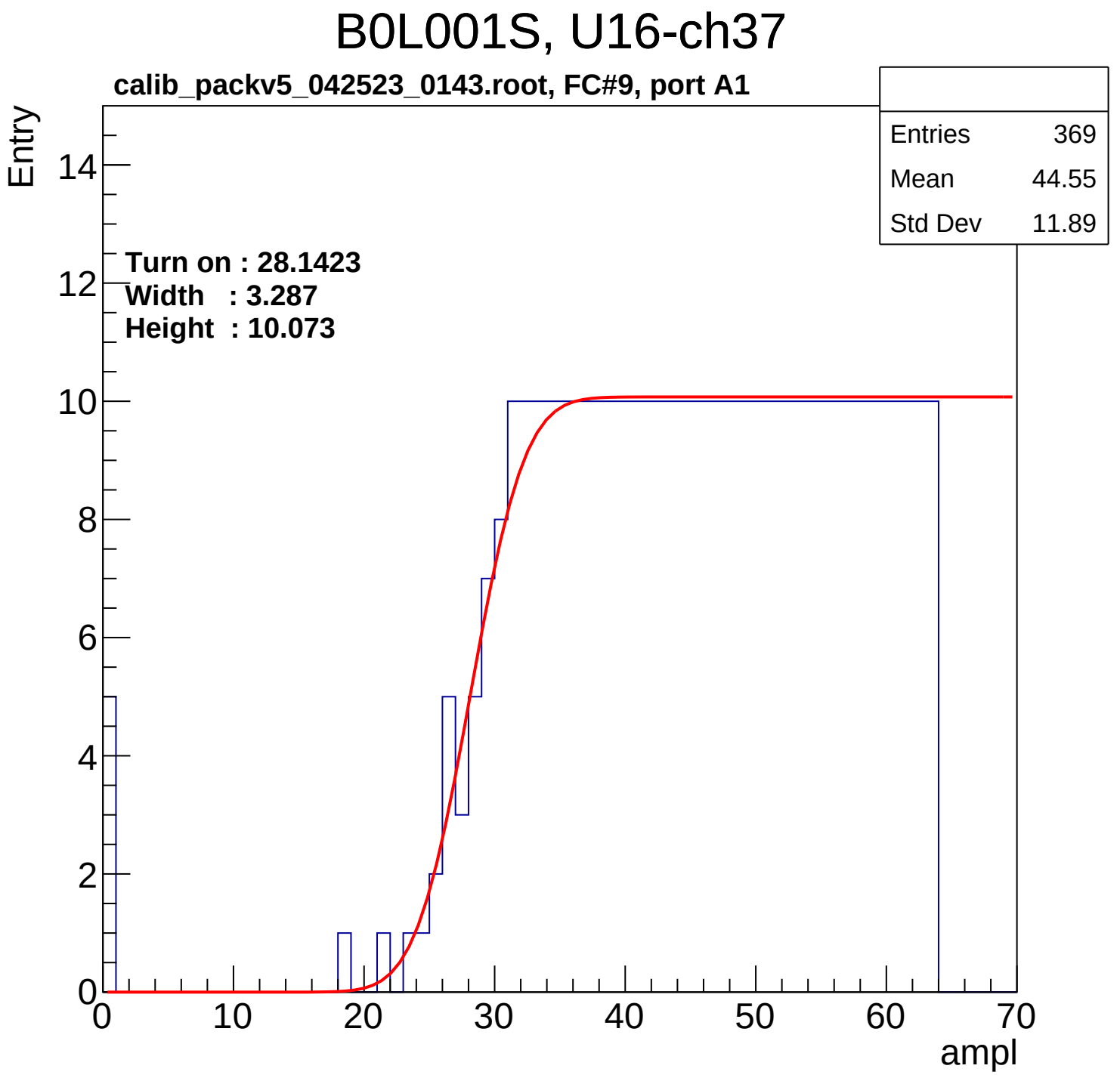
B0L001S, U16-ch37
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.55
Std Dev 11.89
Turn on : 28.1423
Width : 3.287
Height : 10.073
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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40
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60
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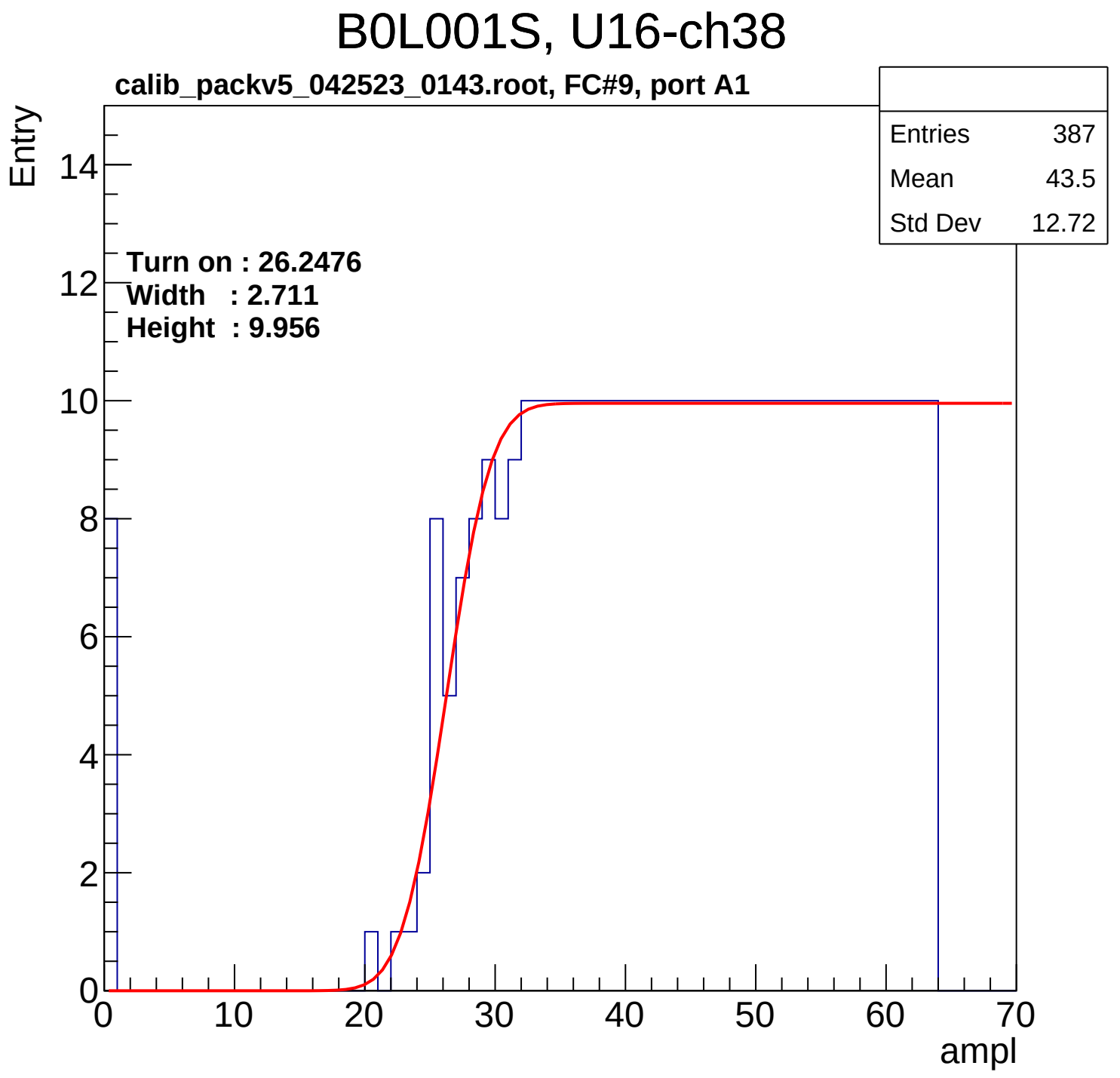
B0L001S, U16-ch38
calib_packv5_042523_0143.root, FC#9, port A1
Entries 387
Mean 43.5
Std Dev 12.72
Turn on : 26.2476
Width : 2.711
Height : 9.956
Entry
ampl
0
2
4
6
8
10
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0
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60
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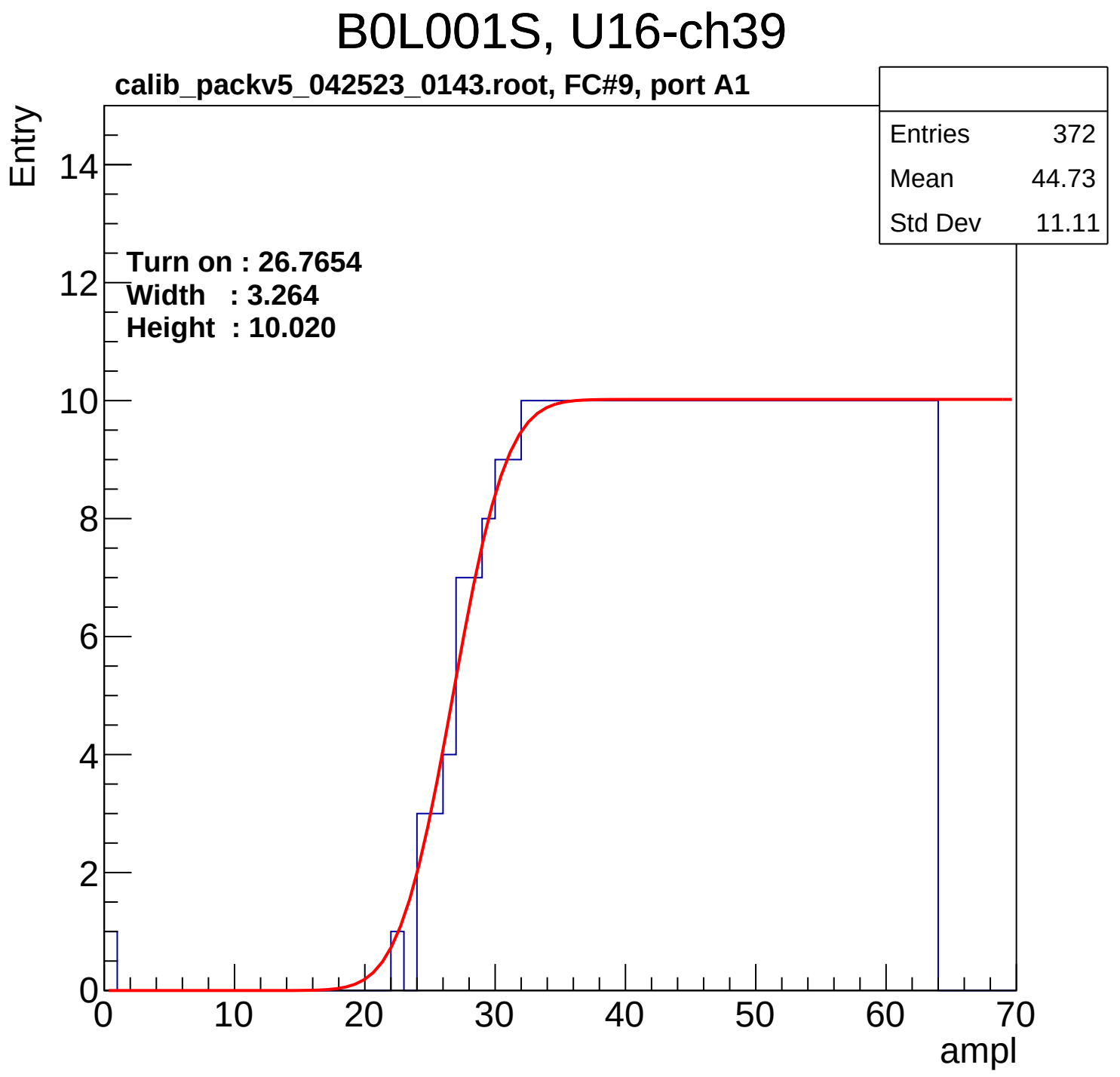
B0L001S, U16-ch39
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.73
Std Dev 11.11
Turn on : 26.7654
Width : 3.264
Height : 10.020
Entry
ampl
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0
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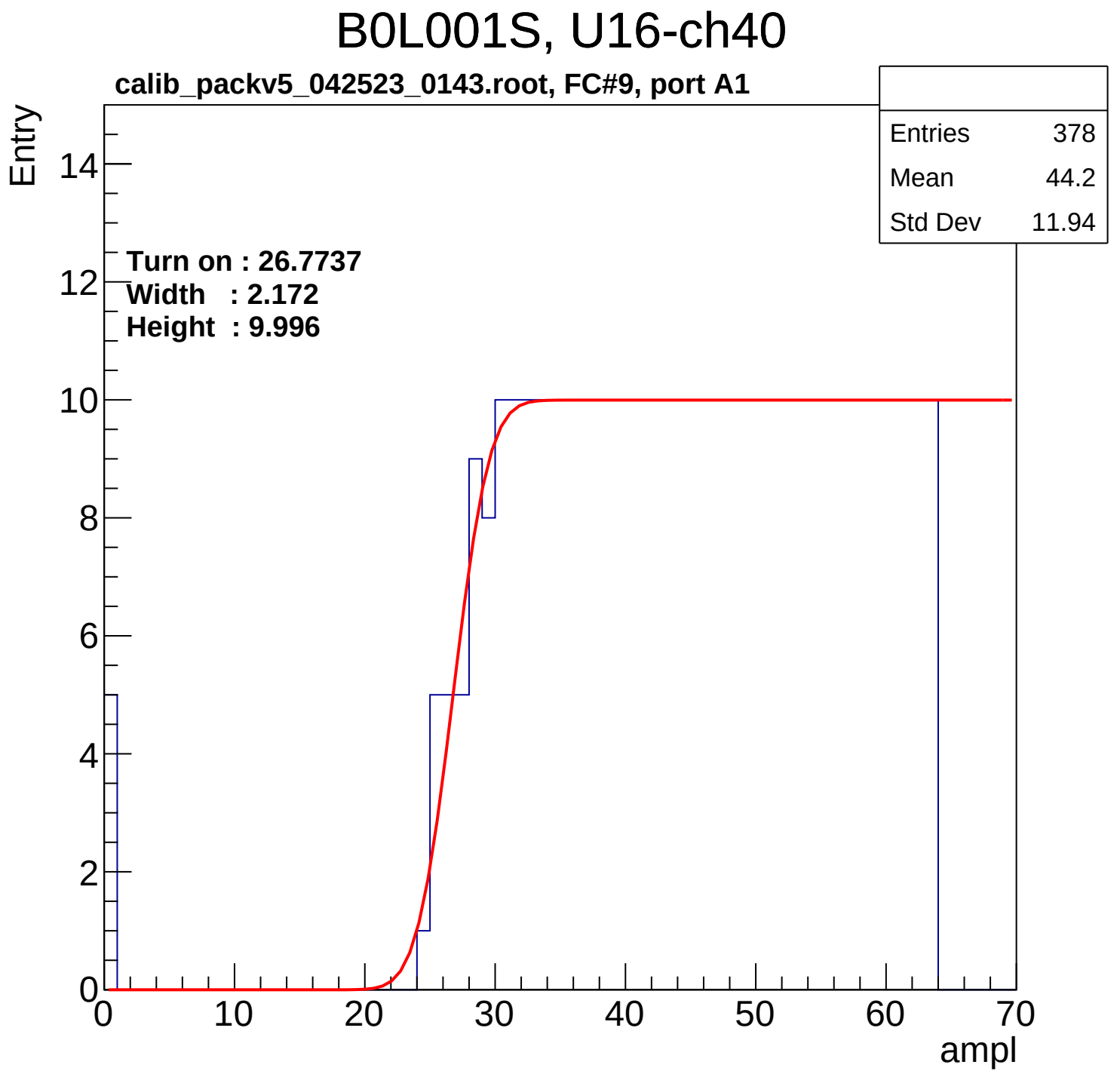
B0L001S, U16-ch40
calib_packv5_042523_0143.root, FC#9, port A1
Entries 378
Mean 44.2
Std Dev 11.94
Turn on : 26.7737
Width : 2.172
Height : 9.996
Entry
ampl
0
2
4
6
8
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0
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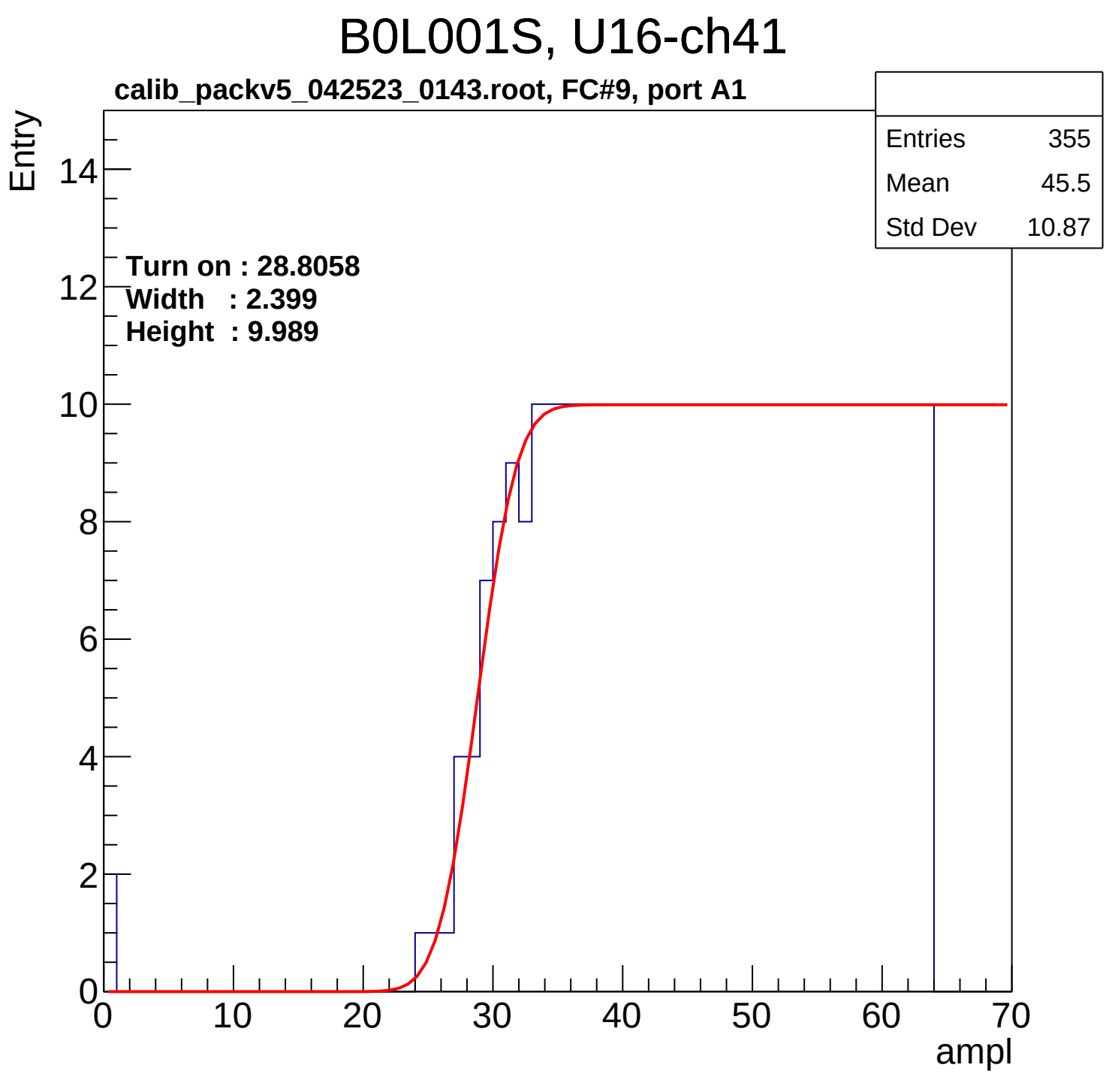
B0L001S, U16-ch41
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.5
Std Dev 10.87
Turn on : 28.8058
Width : 2.399
Height : 9.989
Entry
ampl
0
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4
6
8
10
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0
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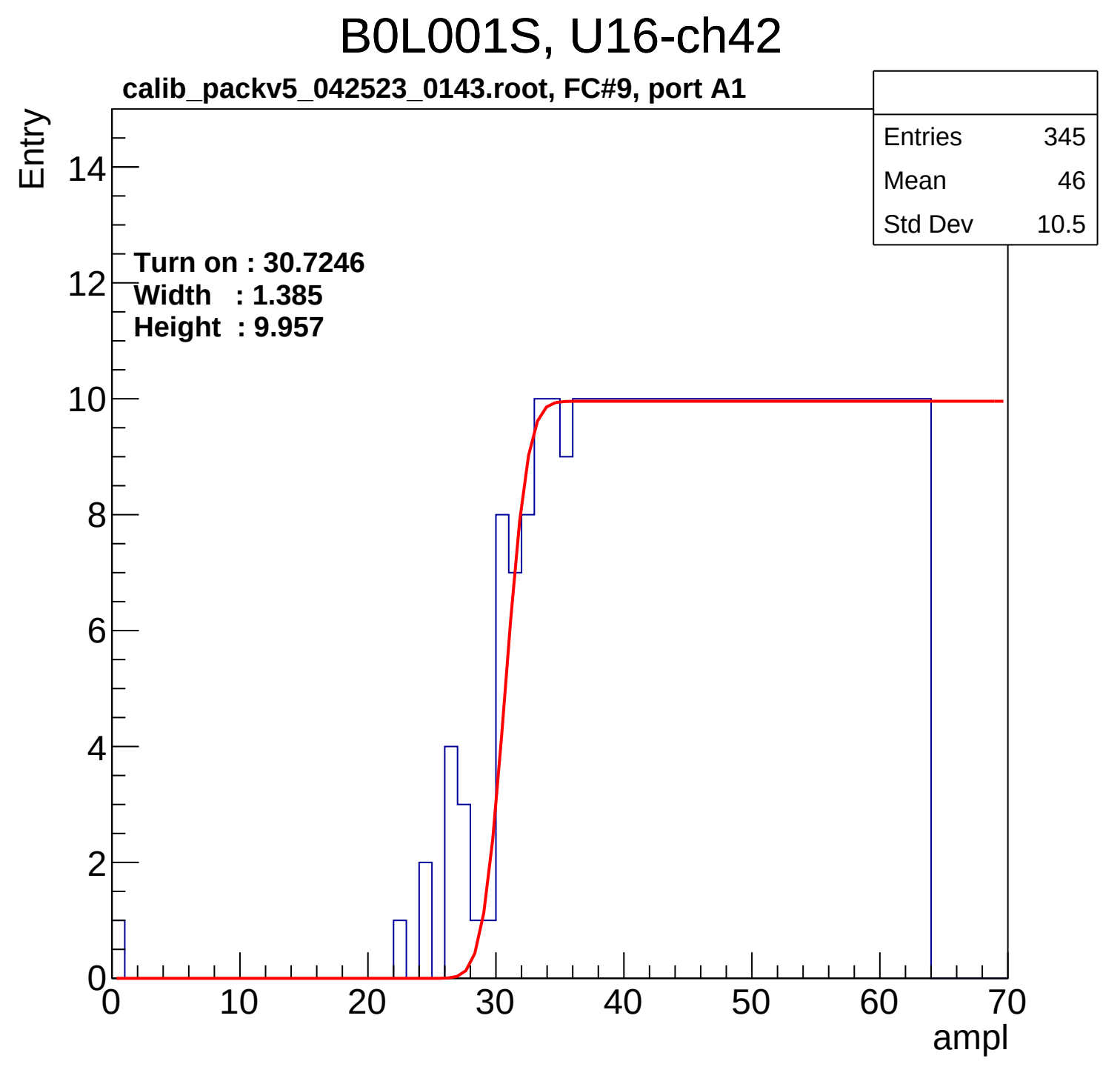
B0L001S, U16-ch42
calib_packv5_042523_0143.root, FC#9, port A1
Entries 345
Mean 46
Std Dev 10.5
Turn on : 30.7246
Width : 1.385
Height : 9.957
Entry
ampl
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6
8
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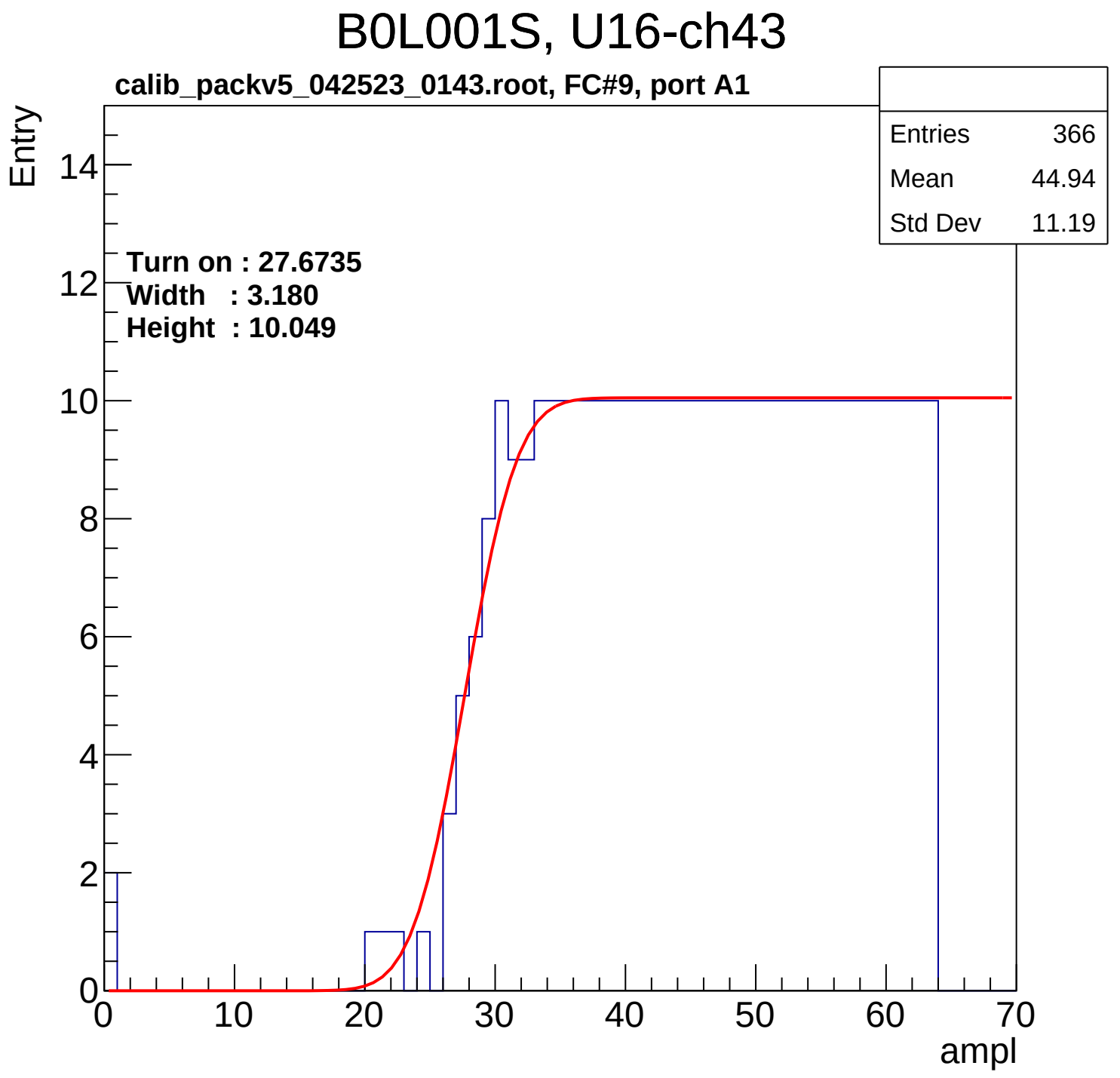
B0L001S, U16-ch43
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.94
Std Dev 11.19
Turn on : 27.6735
Width : 3.180
Height : 10.049
Entry
ampl
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6
8
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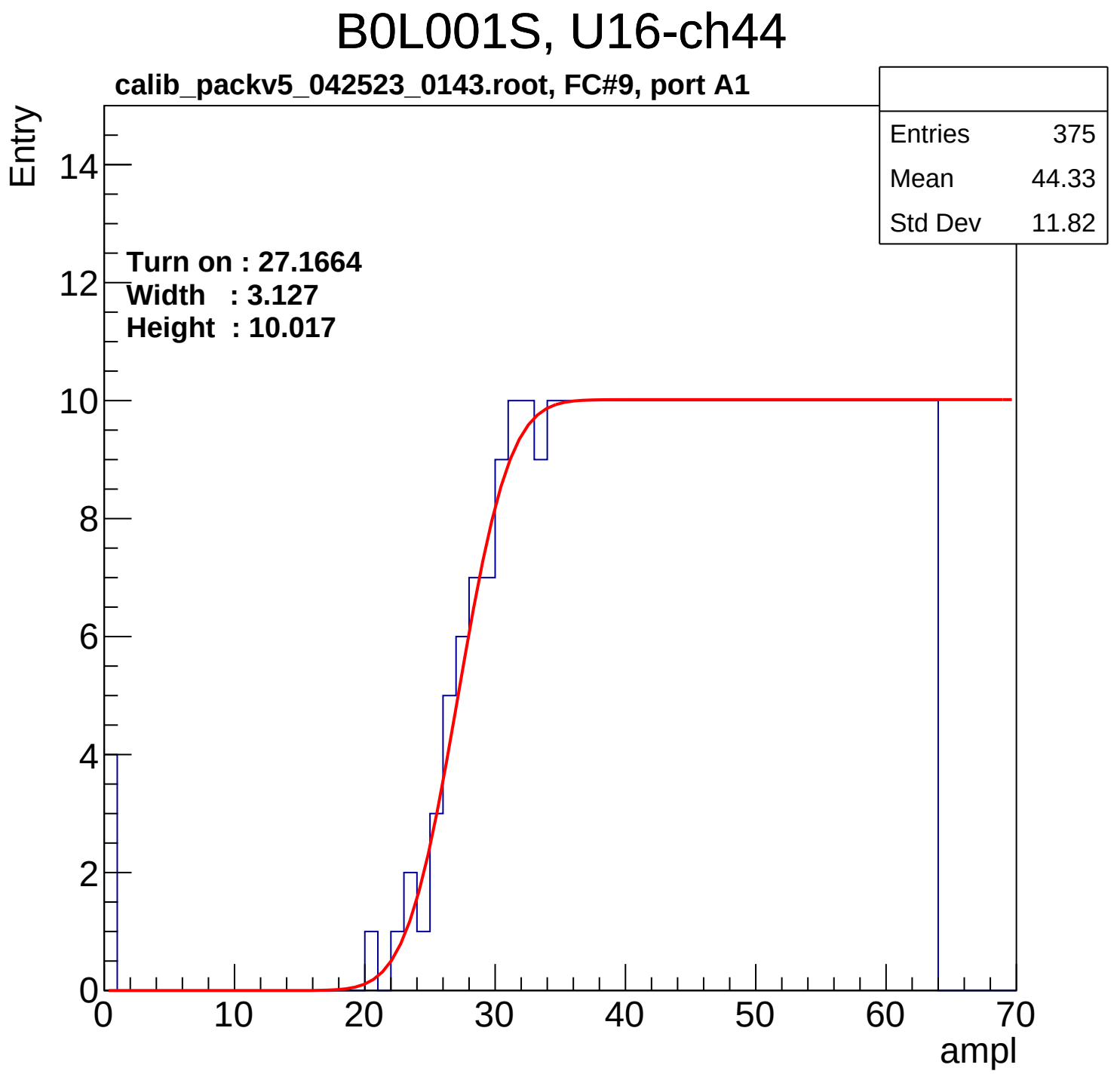
B0L001S, U16-ch44
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.33
Std Dev 11.82
Turn on : 27.1664
Width : 3.127
Height : 10.017
Entry
ampl
0
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4
6
8
10
12
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0
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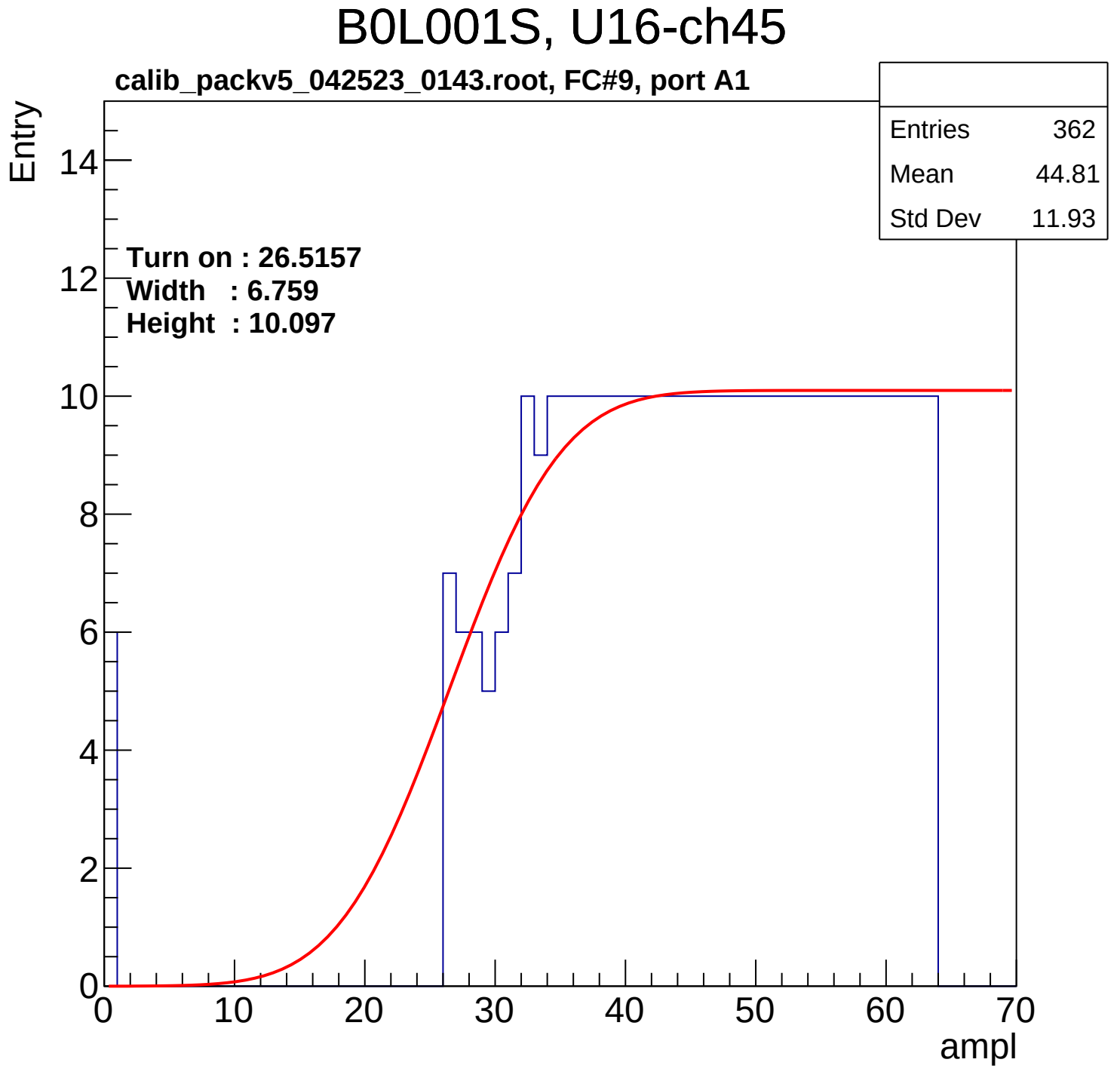
B0L001S, U16-ch45
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 44.81
Std Dev 11.93
Turn on : 26.5157
Width : 6.759
Height : 10.097
Entry
ampl
0
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4
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8
10
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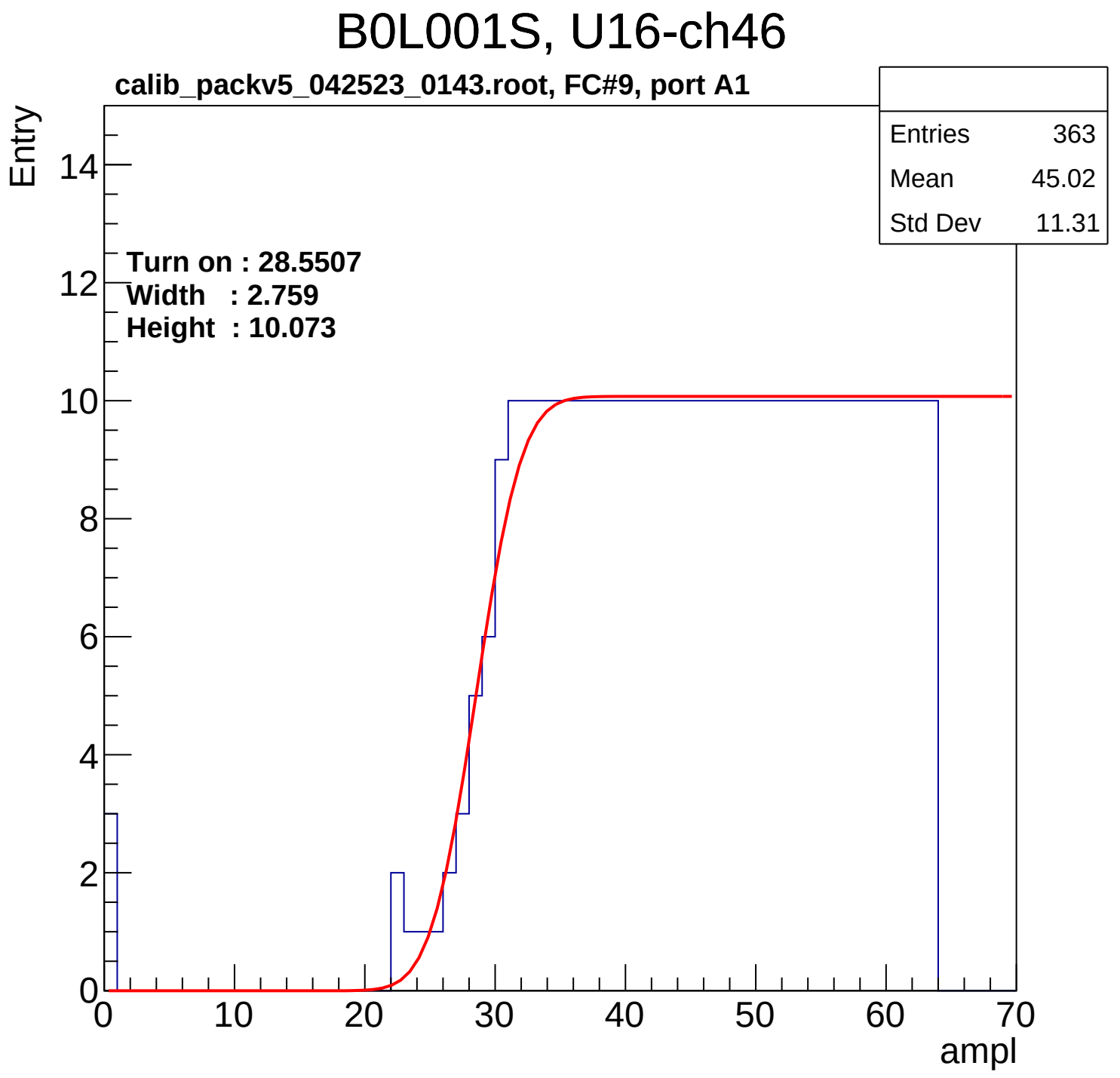
B0L001S, U16-ch46
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.02
Std Dev 11.31
Turn on : 28.5507
Width : 2.759
Height : 10.073
Entry
ampl
0
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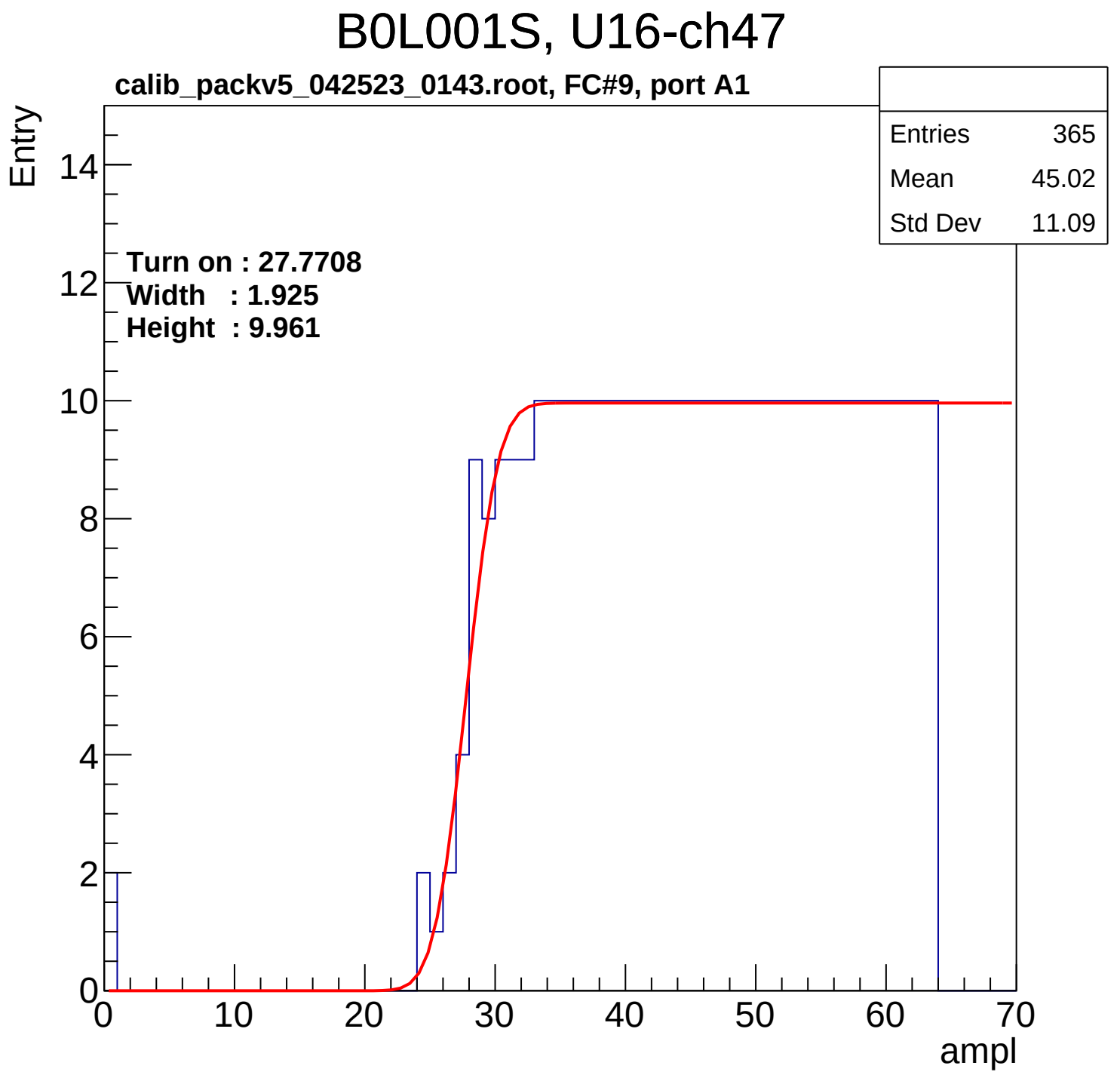
B0L001S, U16-ch47
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 45.02
Std Dev 11.09
Turn on : 27.7708
Width : 1.925
Height : 9.961
Entry
ampl
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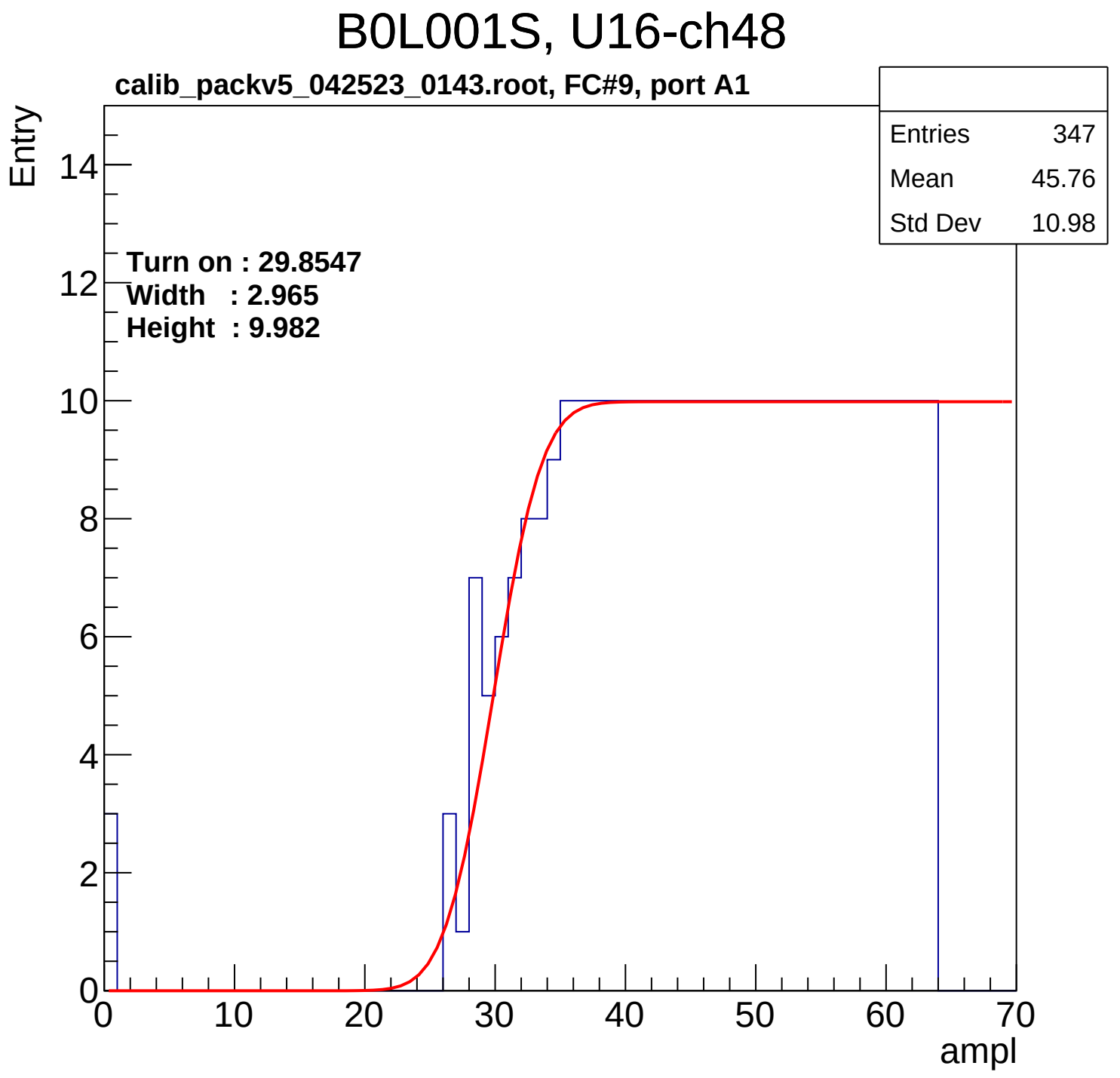
B0L001S, U16-ch48
calib_packv5_042523_0143.root, FC#9, port A1
Entries 347
Mean 45.76
Std Dev 10.98
Turn on : 29.8547
Width : 2.965
Height : 9.982
Entry
ampl
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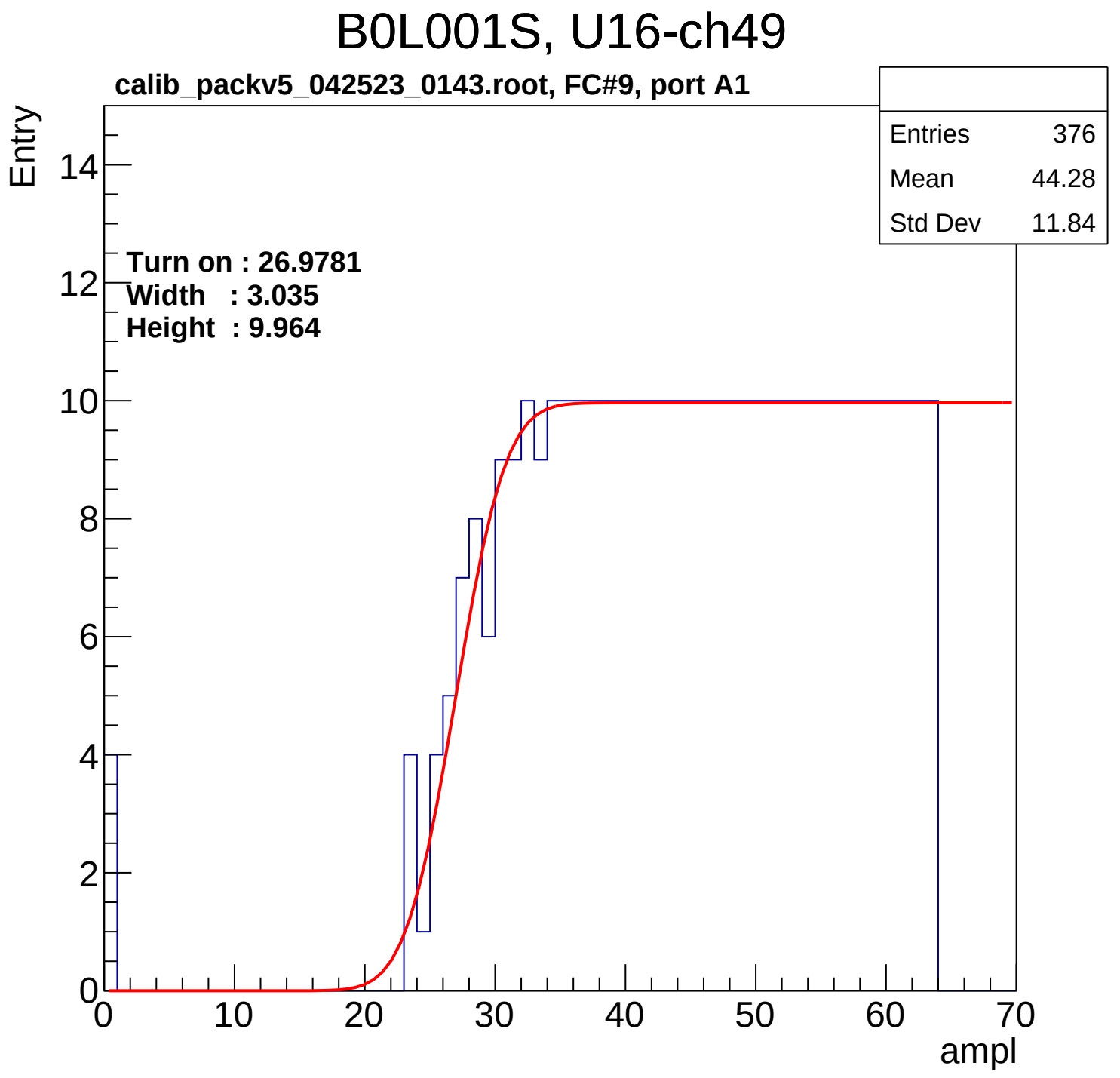
B0L001S, U16-ch49
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.28
Std Dev 11.84
Turn on : 26.9781
Width : 3.035
Height : 9.964
Entry
ampl
0
2
4
6
8
10
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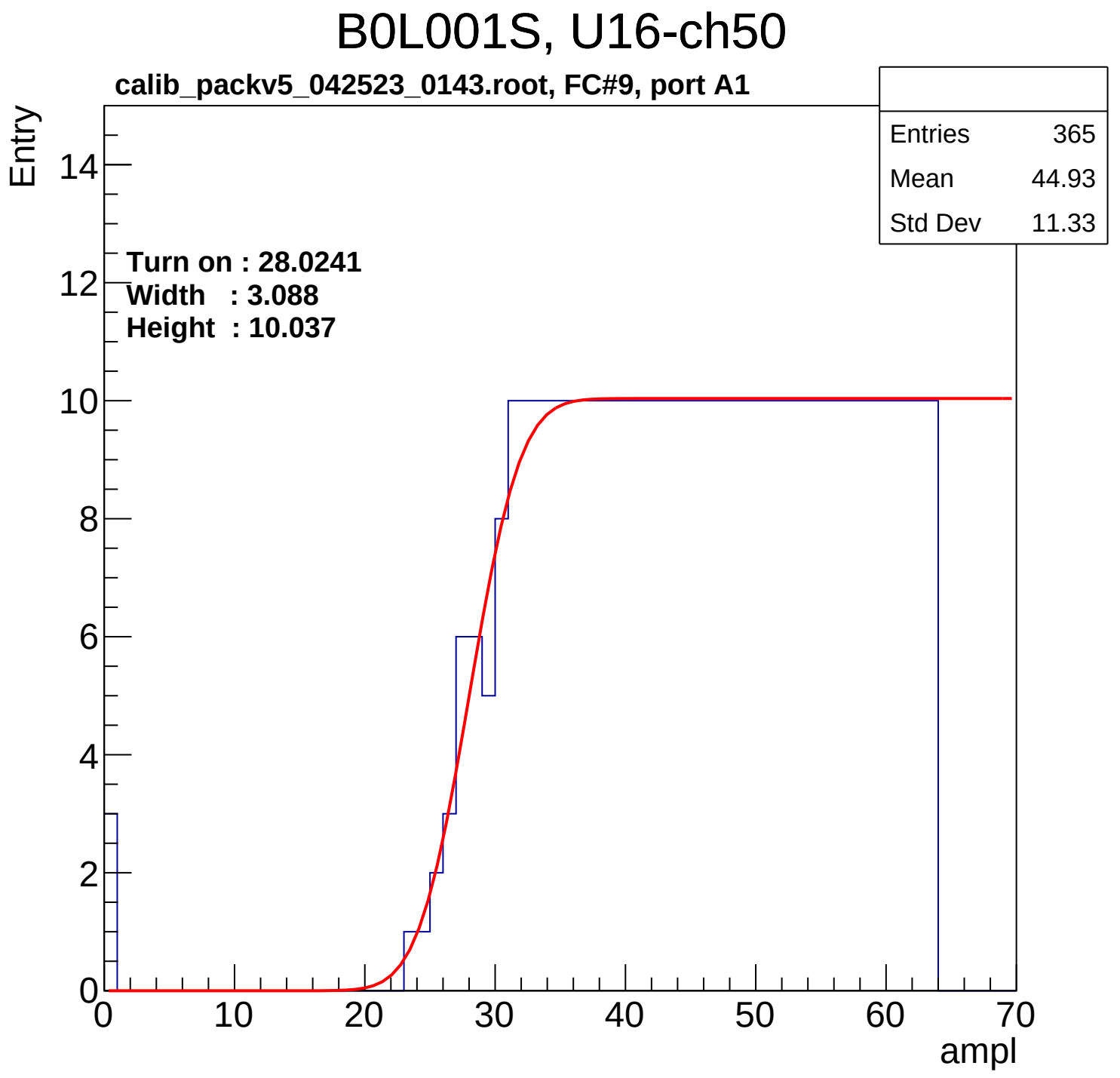
B0L001S, U16-ch50
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.93
Std Dev 11.33
Turn on : 28.0241
Width : 3.088
Height : 10.037
Entry
ampl
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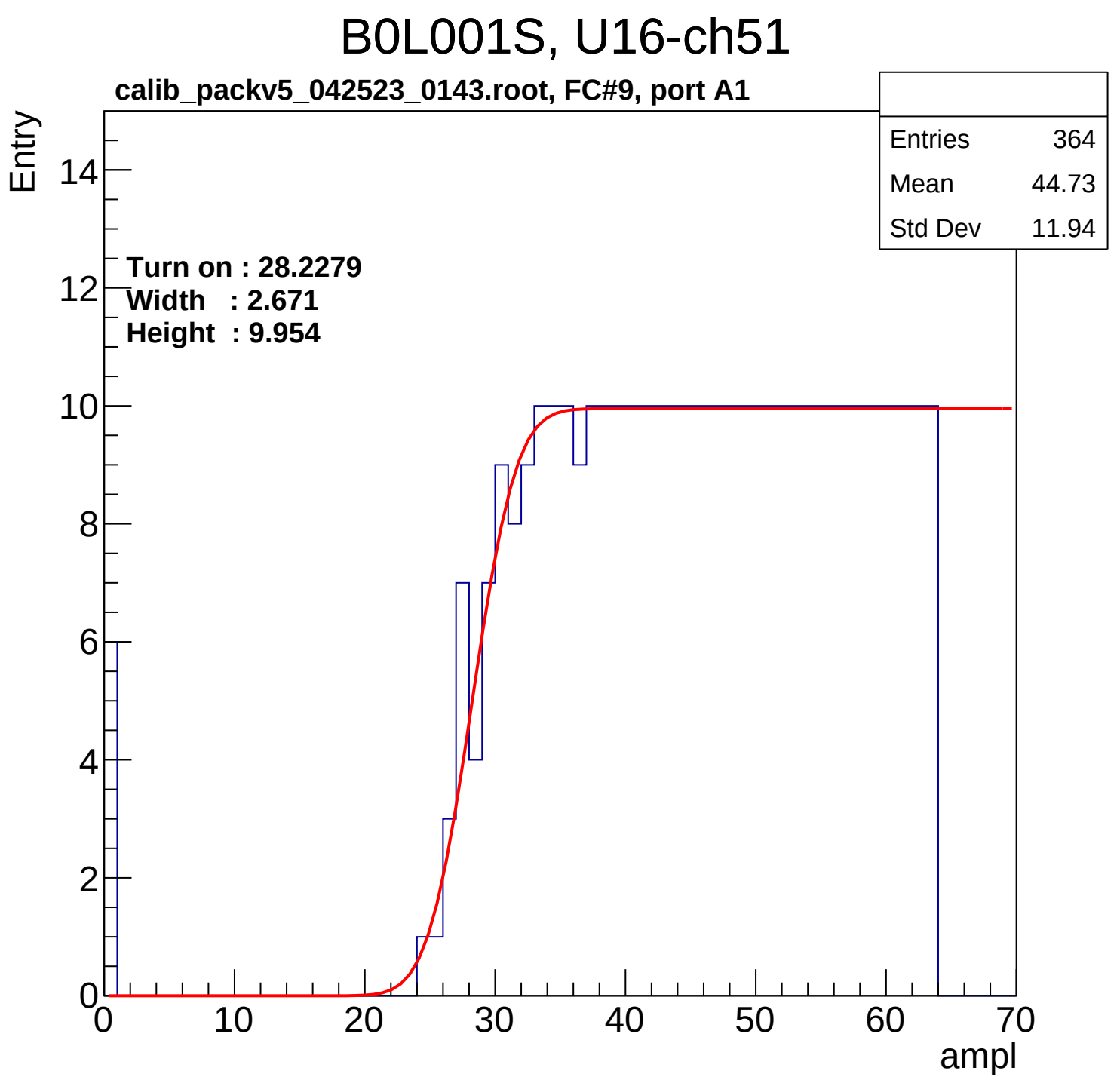
B0L001S, U16-ch51
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.73
Std Dev 11.94
Turn on : 28.2279
Width : 2.671
Height : 9.954
Entry
ampl
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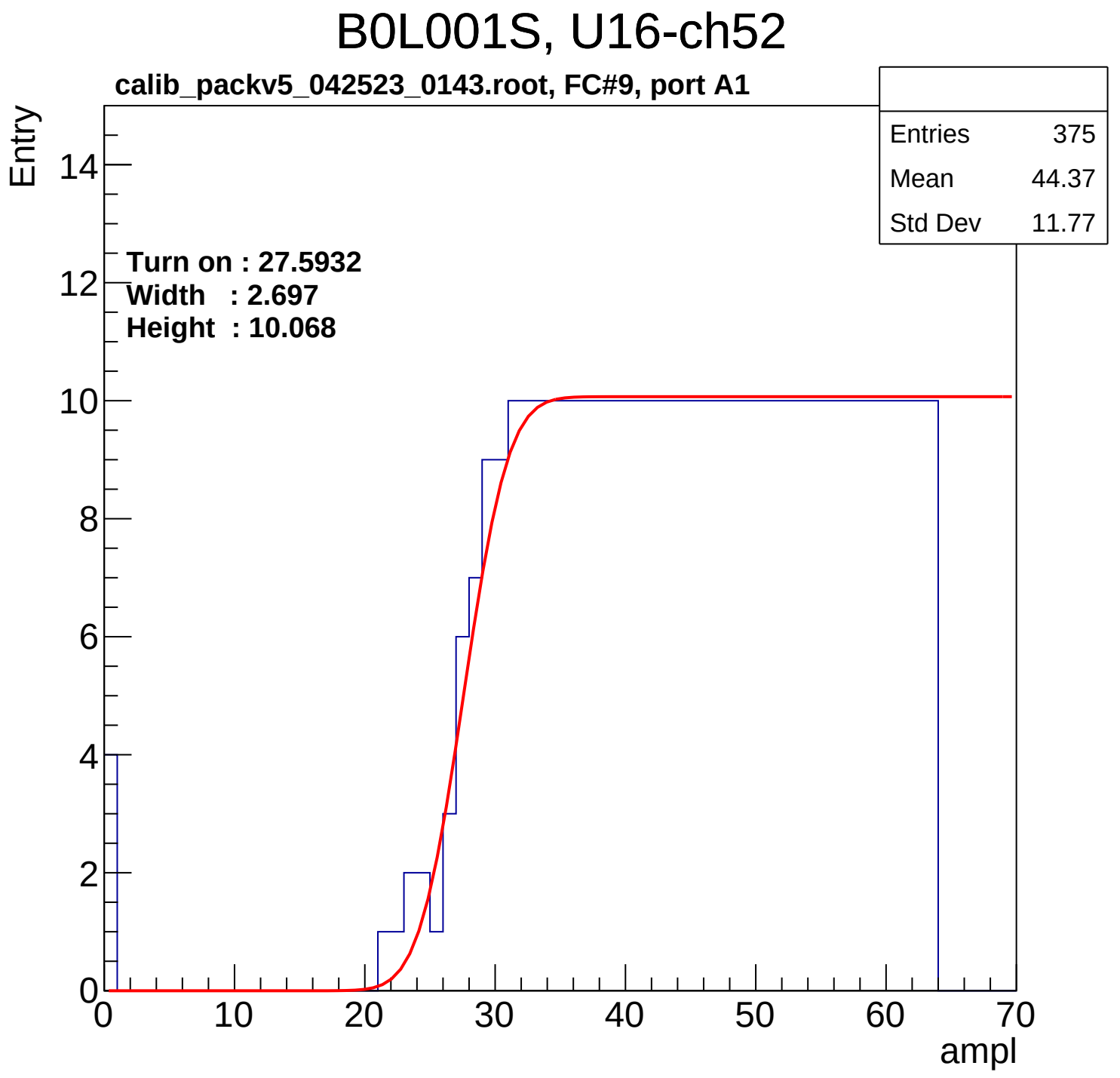
B0L001S, U16-ch52
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.37
Std Dev 11.77
Turn on : 27.5932
Width : 2.697
Height : 10.068
Entry
ampl
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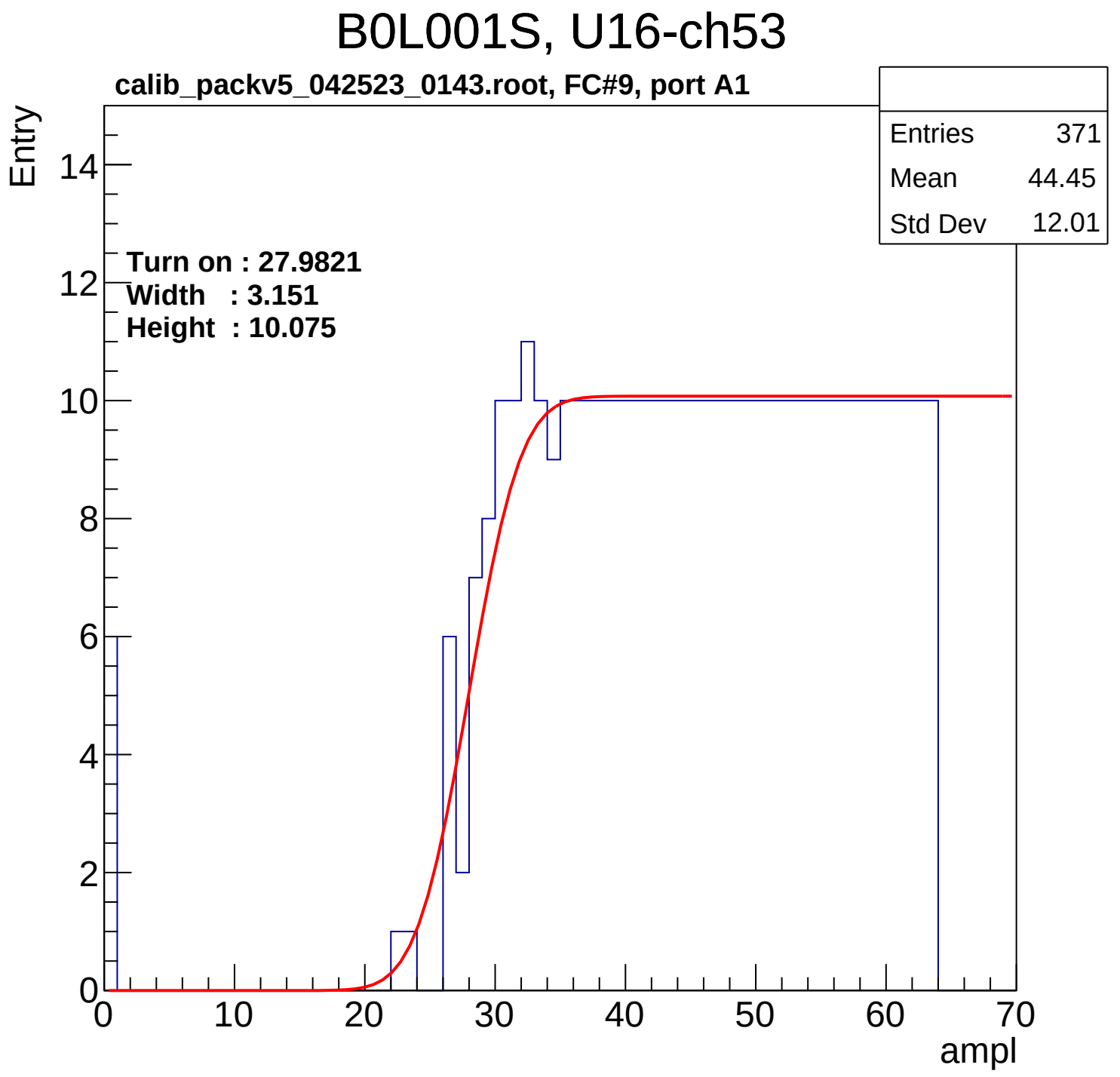
B0L001S, U16-ch53
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.45
Std Dev 12.01
Turn on : 27.9821
Width : 3.151
Height : 10.075
Entry
ampl
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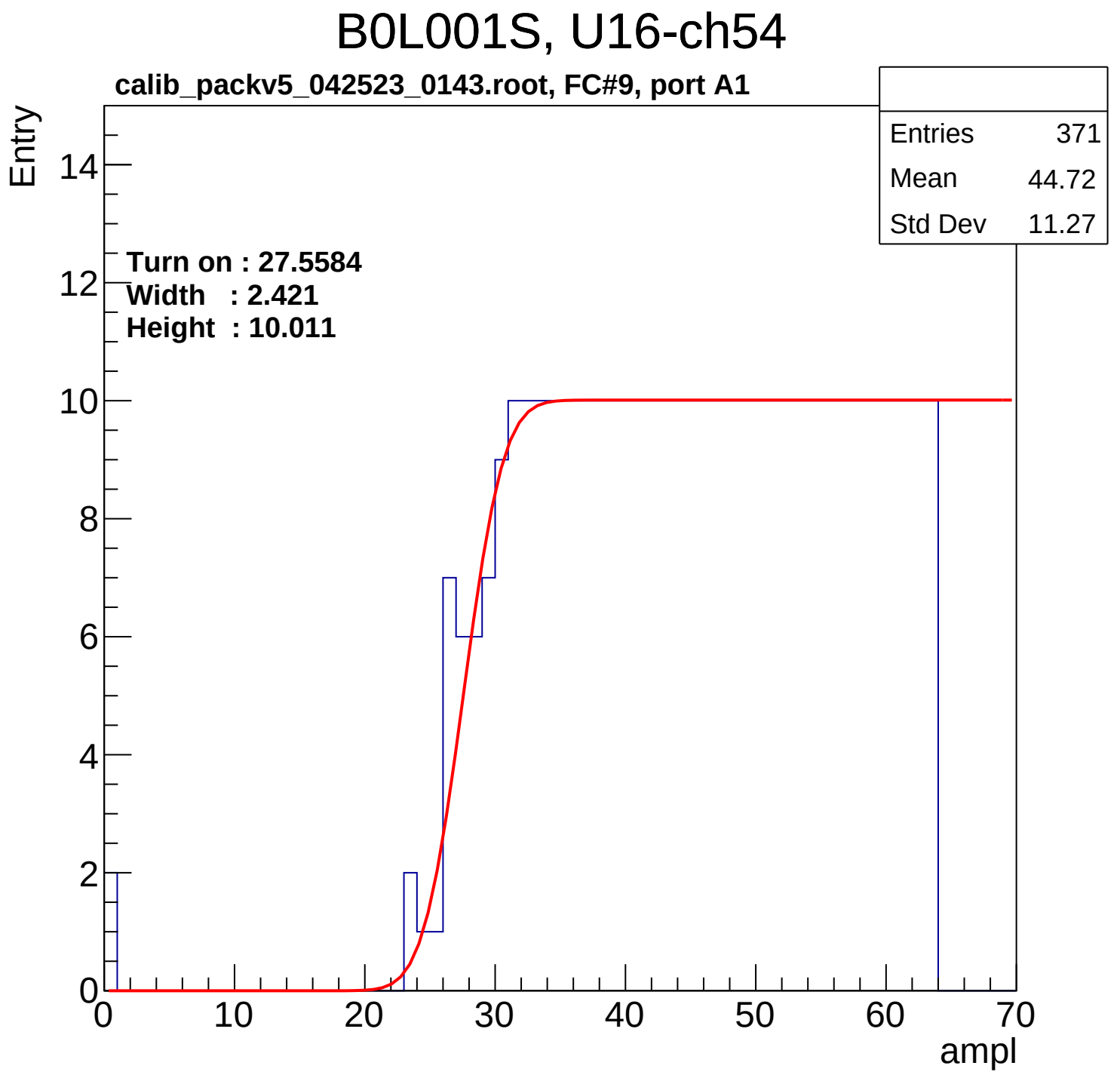
B0L001S, U16-ch54
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.72
Std Dev 11.27
Turn on : 27.5584
Width : 2.421
Height : 10.011
Entry
ampl
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6
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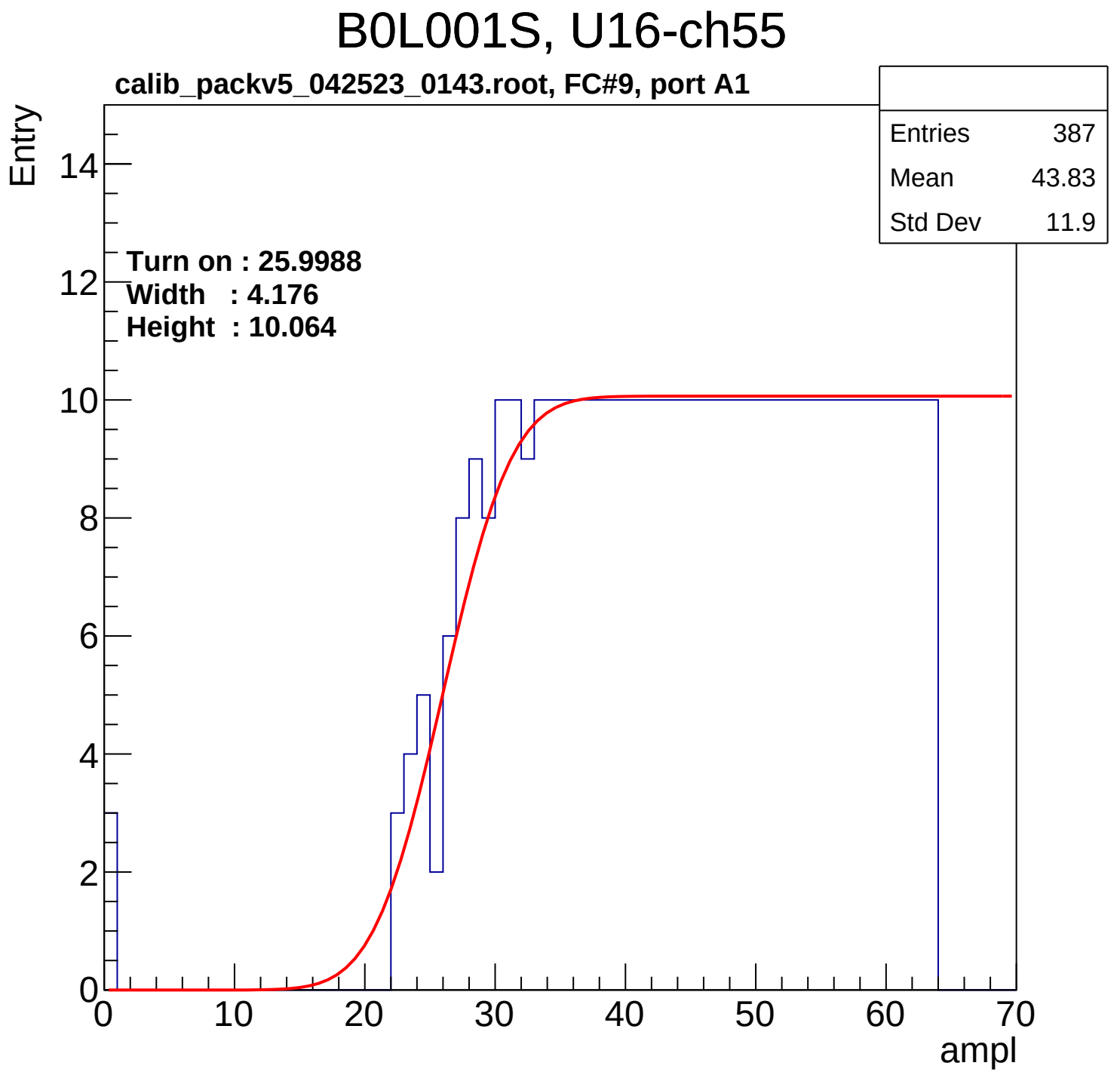
B0L001S, U16-ch55
calib_packv5_042523_0143.root, FC#9, port A1
Entries 387
Mean 43.83
Std Dev 11.9
Turn on : 25.9988
Width : 4.176
Height : 10.064
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ampl
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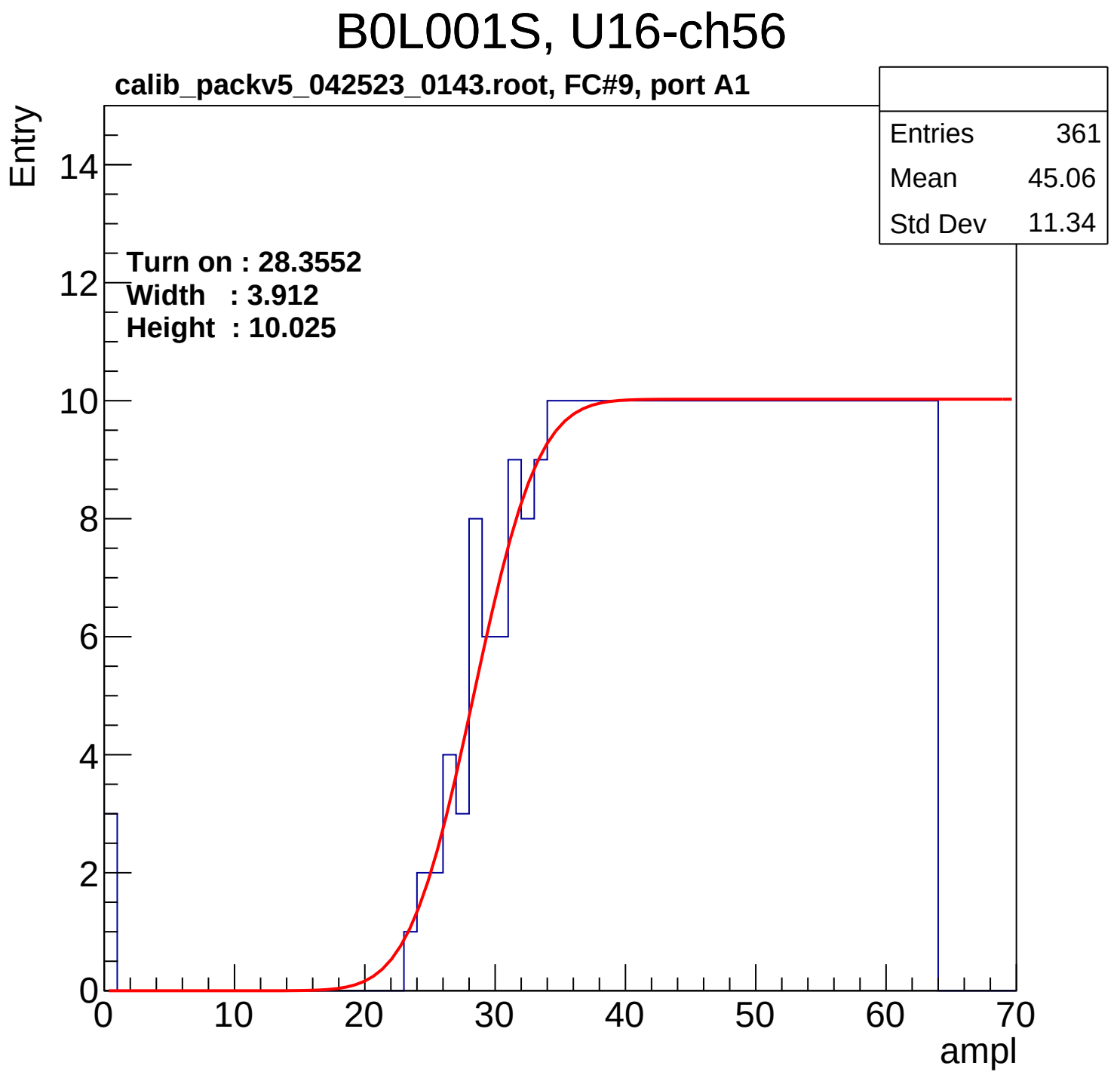
B0L001S, U16-ch56
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.06
Std Dev 11.34
Turn on : 28.3552
Width : 3.912
Height : 10.025
Entry
ampl
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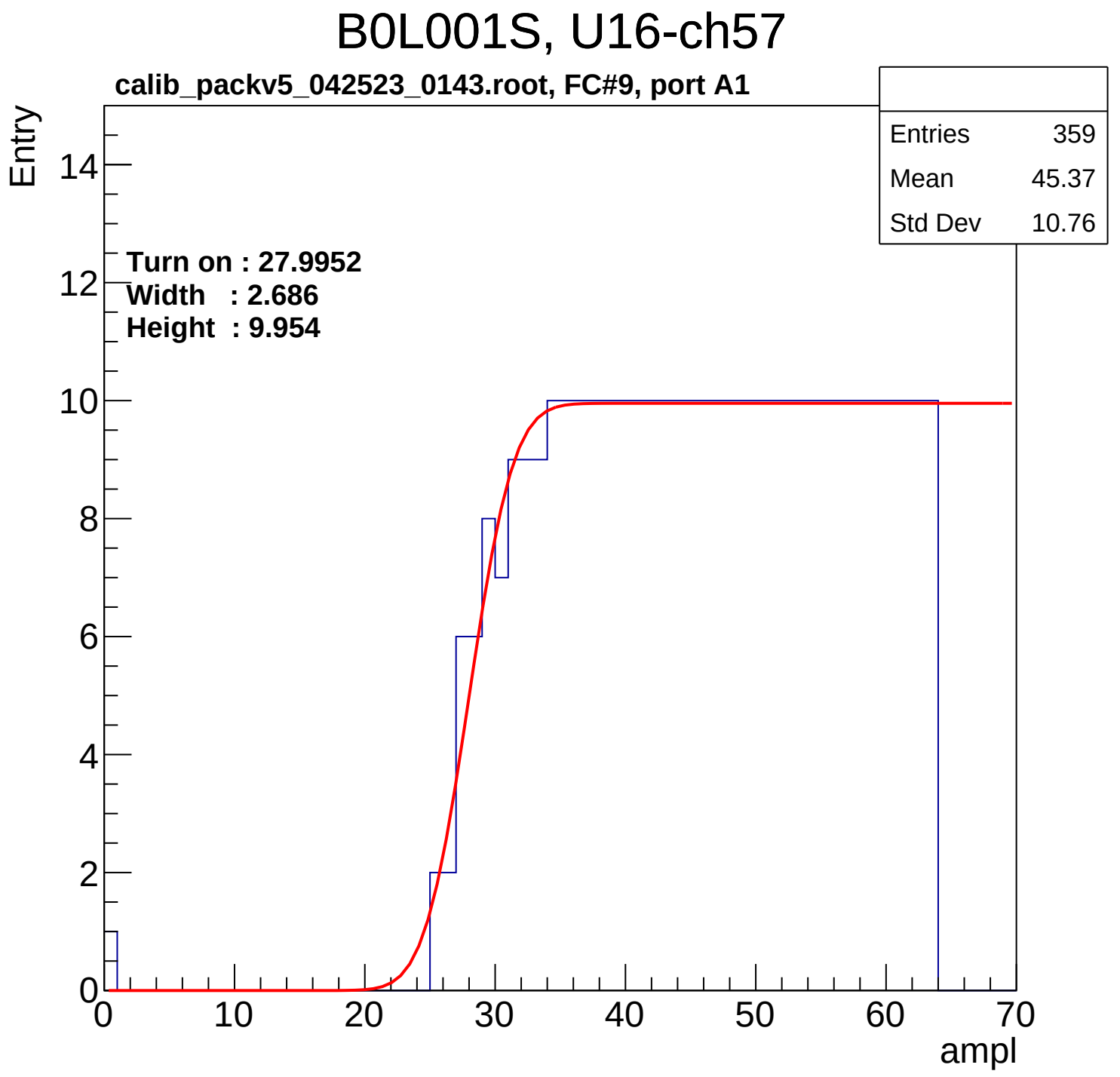
B0L001S, U16-ch57
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.37
Std Dev 10.76
Turn on : 27.9952
Width : 2.686
Height : 9.954
Entry
ampl
0
2
4
6
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12
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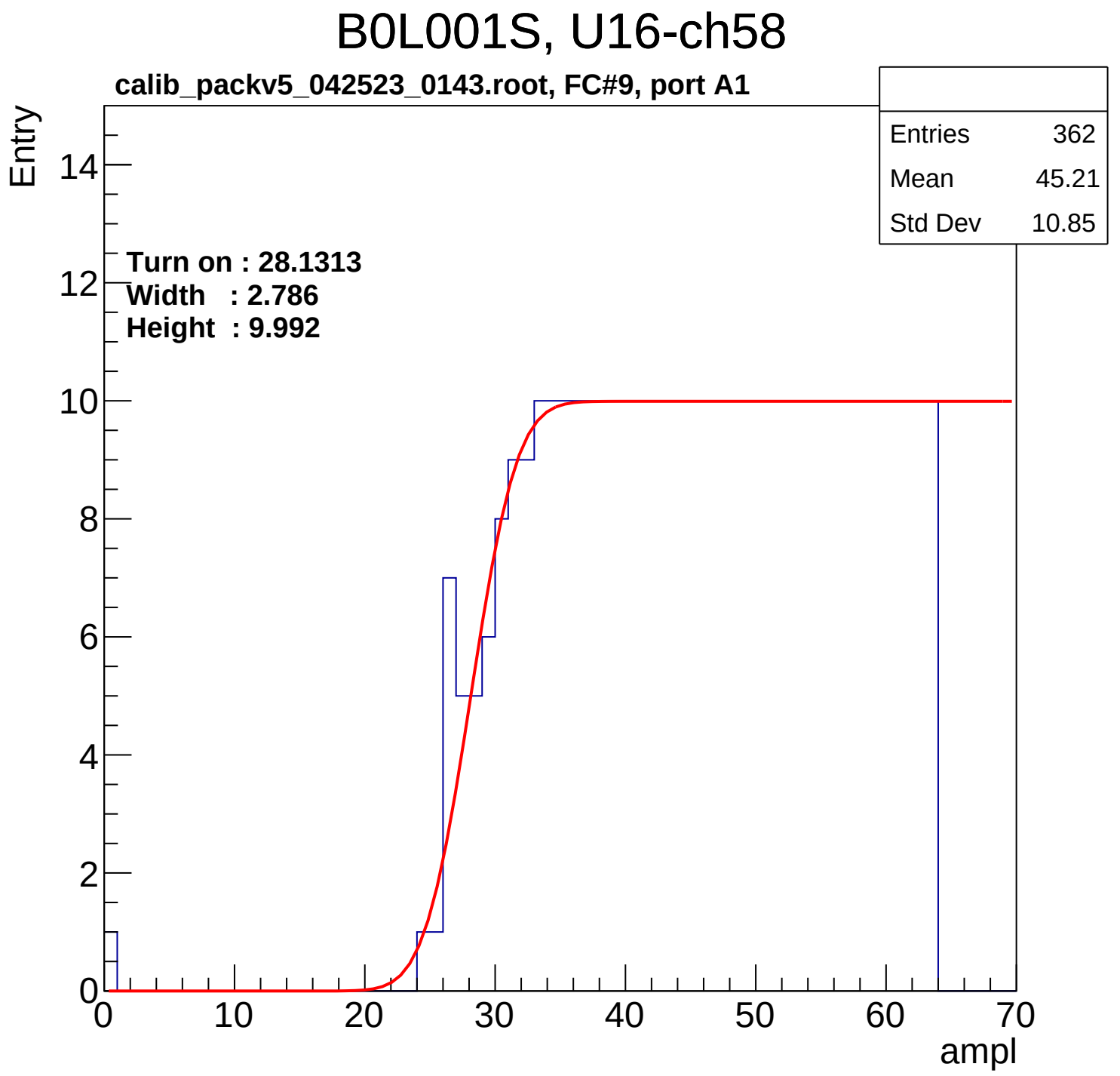
B0L001S, U16-ch58
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.21
Std Dev 10.85
Turn on : 28.1313
Width : 2.786
Height : 9.992
Entry
ampl
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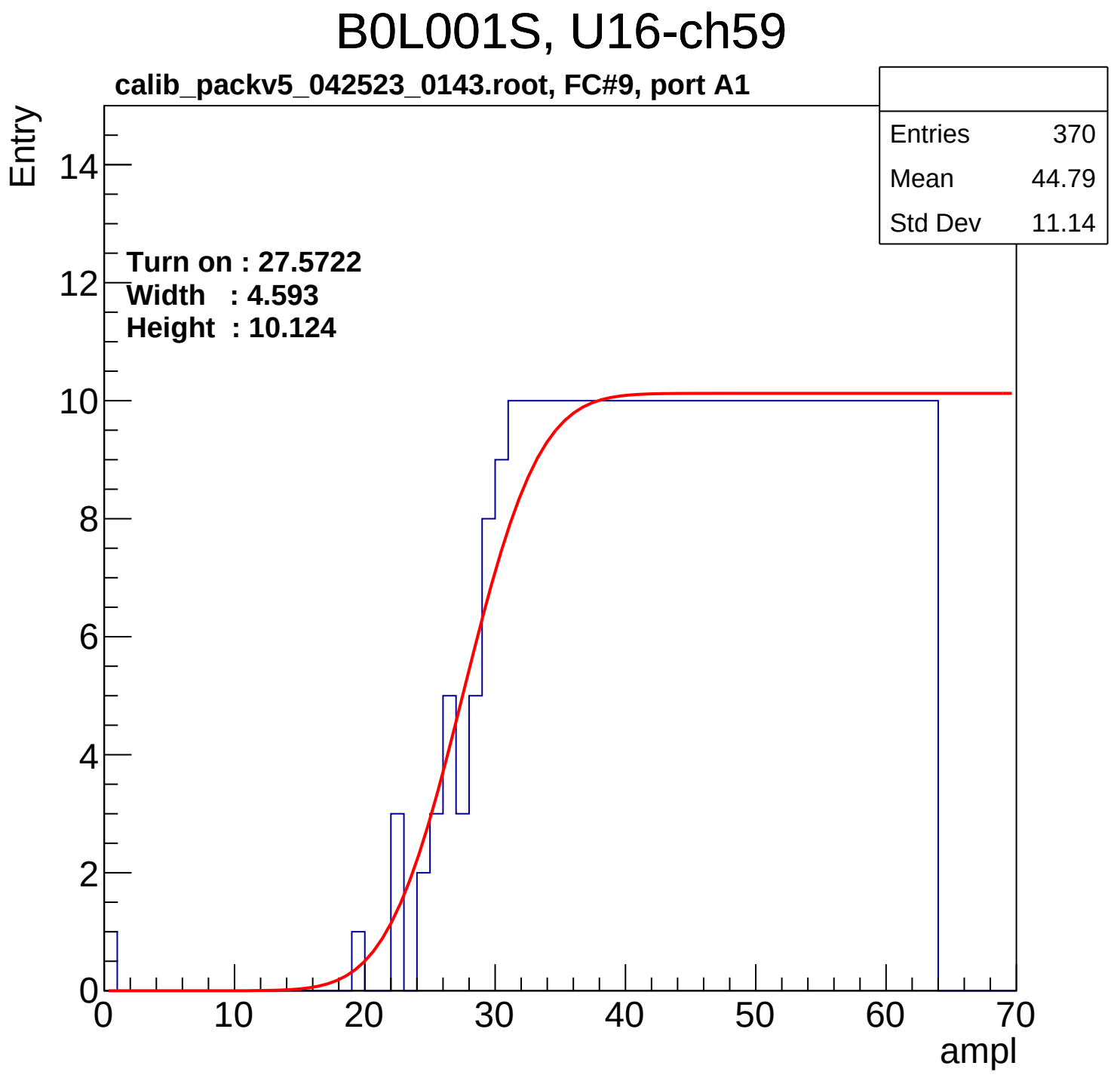
B0L001S, U16-ch59
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.79
Std Dev 11.14
Turn on : 27.5722
Width : 4.593
Height : 10.124
Entry
ampl
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4
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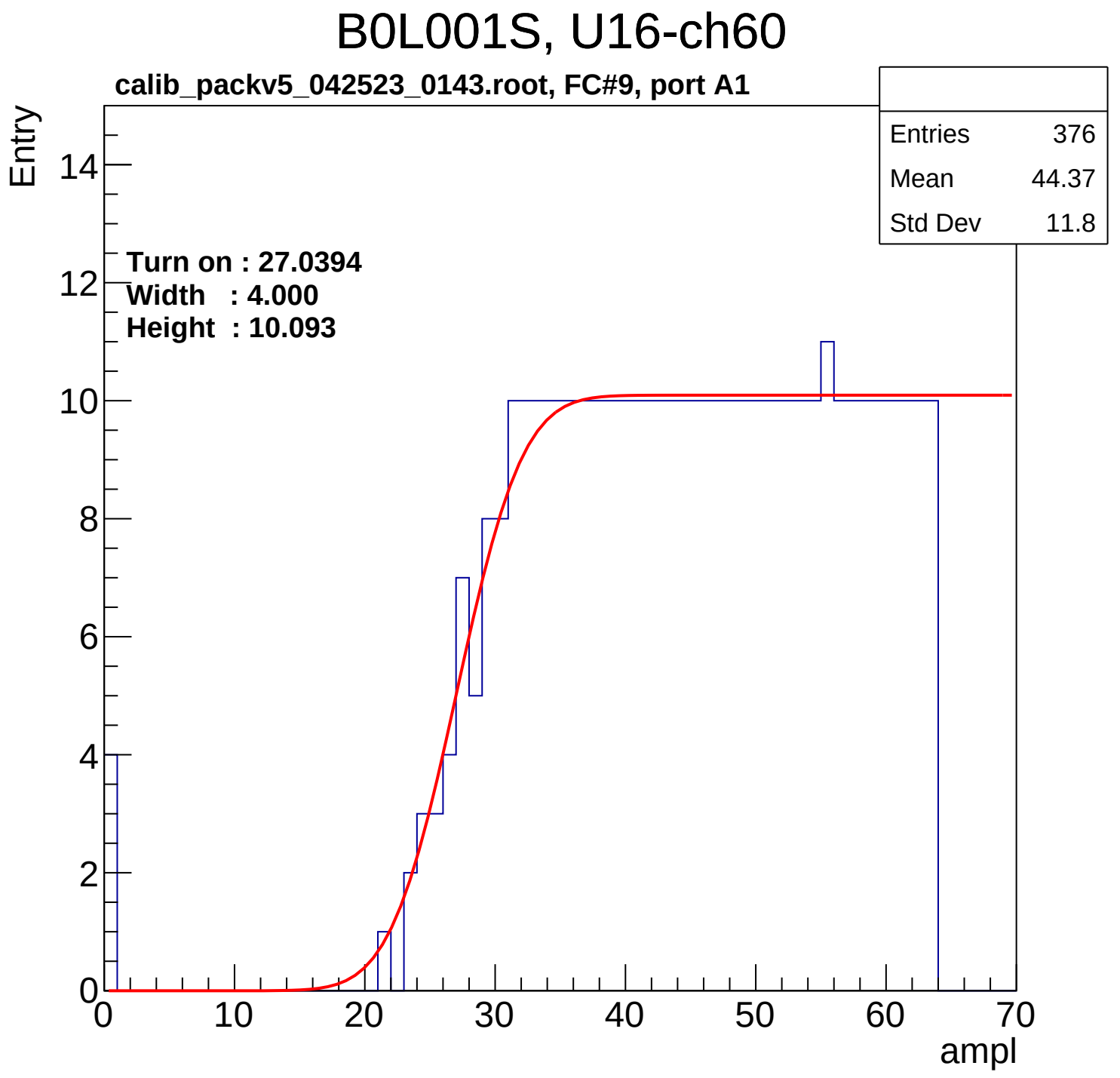
B0L001S, U16-ch60
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.37
Std Dev 11.8
Turn on : 27.0394
Width : 4.000
Height : 10.093
Entry
ampl
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2
4
6
8
10
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0
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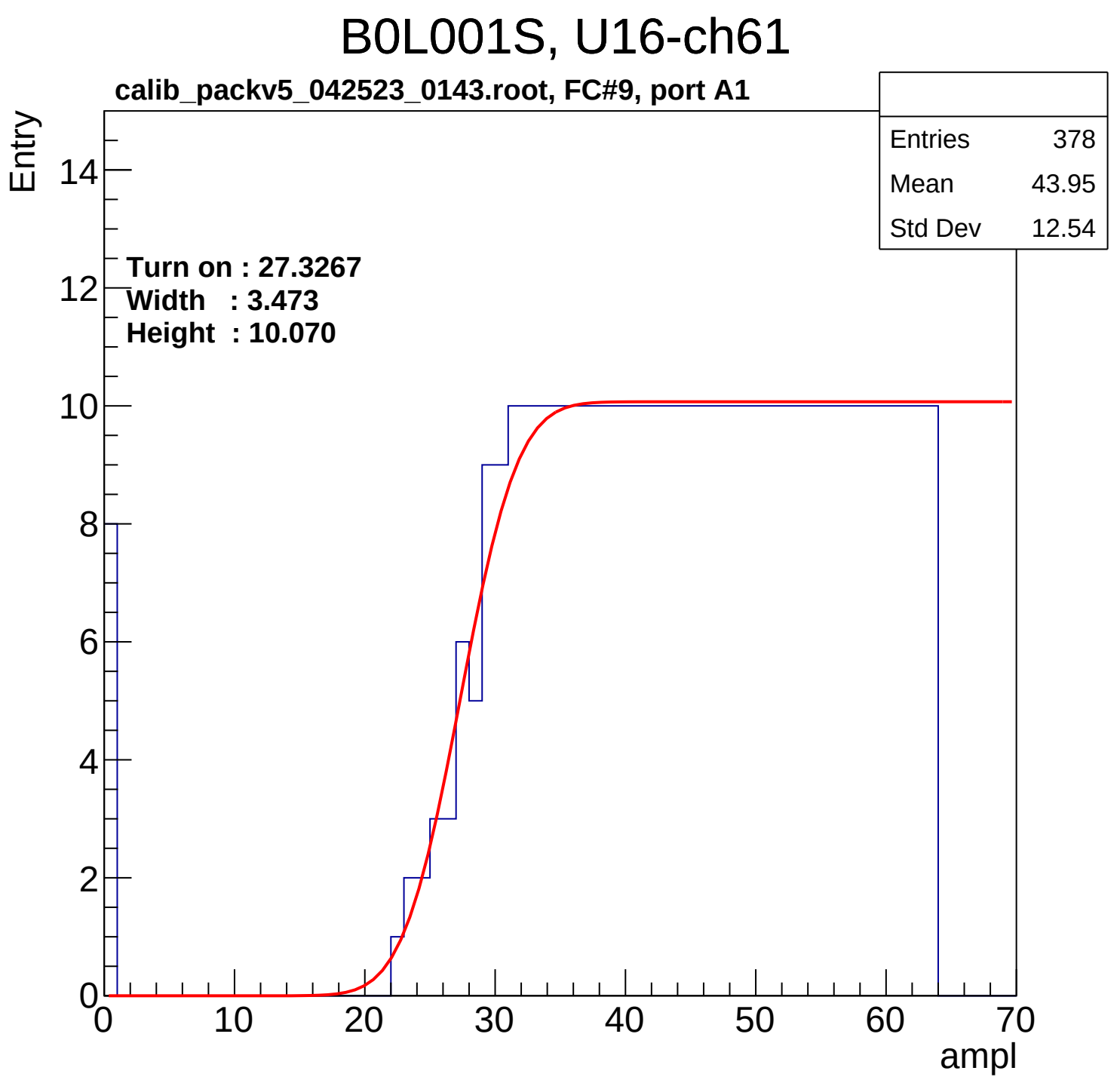
B0L001S, U16-ch61
calib_packv5_042523_0143.root, FC#9, port A1
Entries 378
Mean 43.95
Std Dev 12.54
Turn on : 27.3267
Width : 3.473
Height : 10.070
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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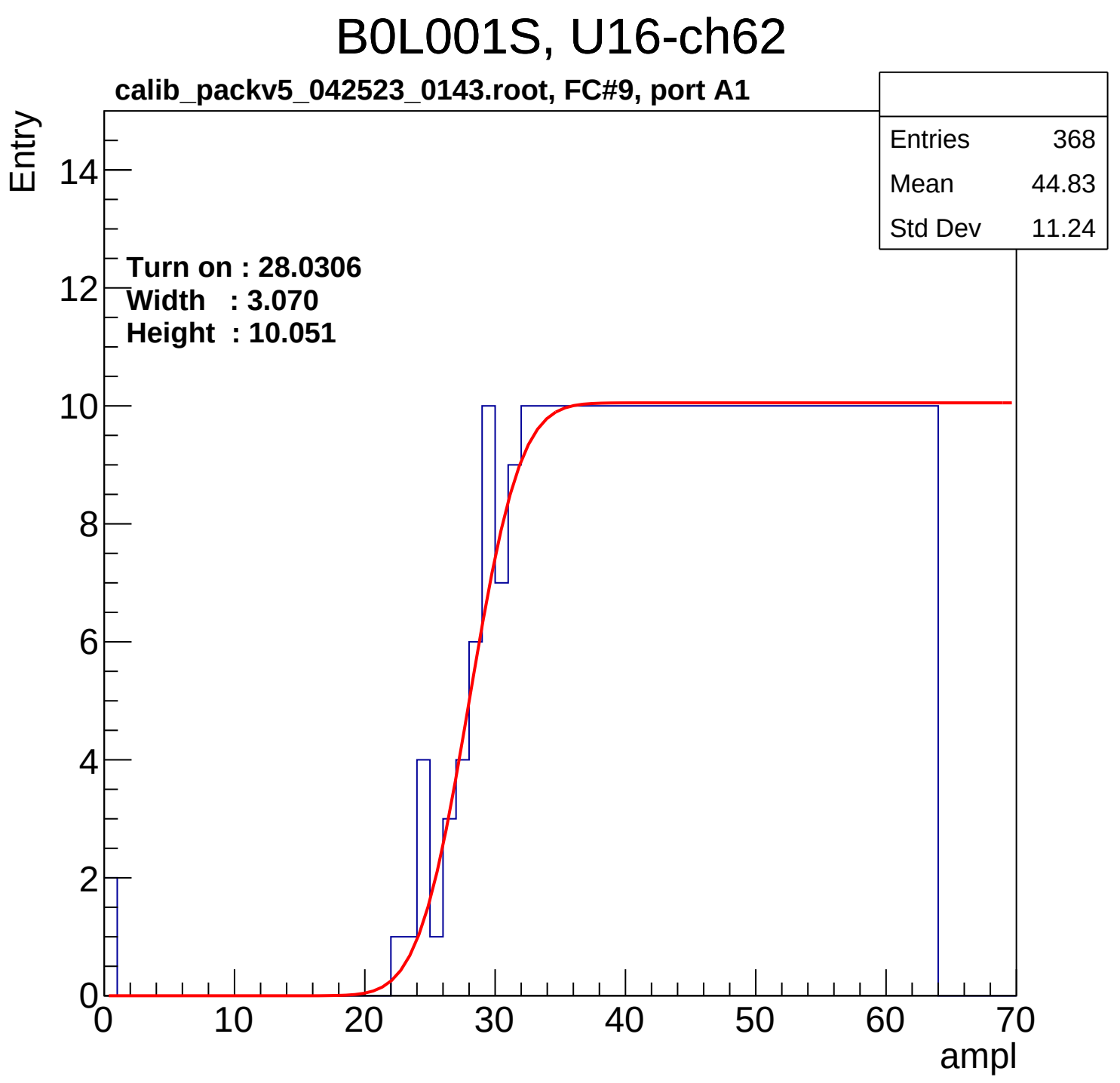
B0L001S, U16-ch62
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.83
Std Dev 11.24
Turn on : 28.0306
Width : 3.070
Height : 10.051
Entry
ampl
0
2
4
6
8
10
12
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0
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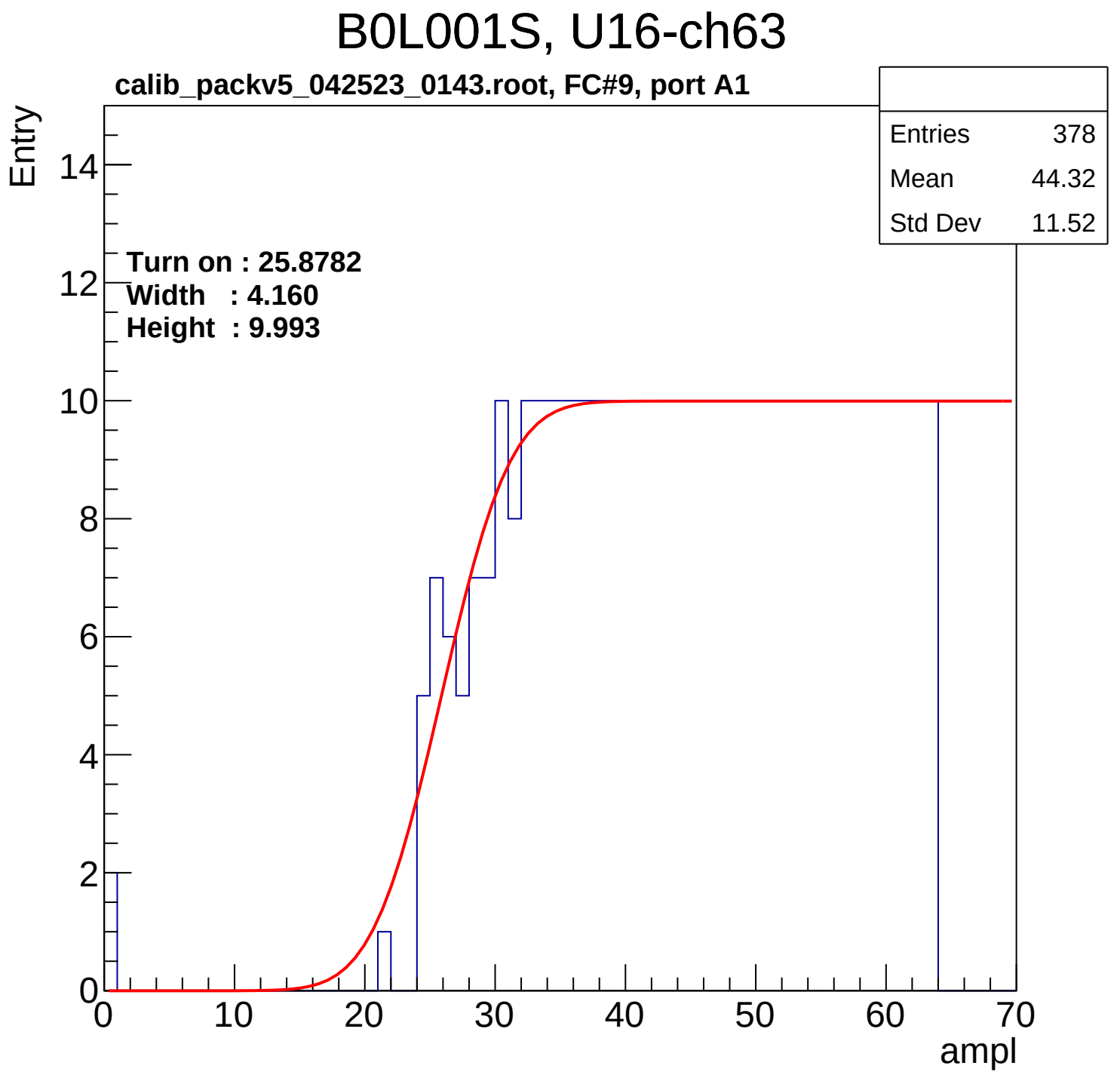
B0L001S, U16-ch63
calib_packv5_042523_0143.root, FC#9, port A1
Entries 378
Mean 44.32
Std Dev 11.52
Turn on : 25.8782
Width : 4.160
Height : 9.993
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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60
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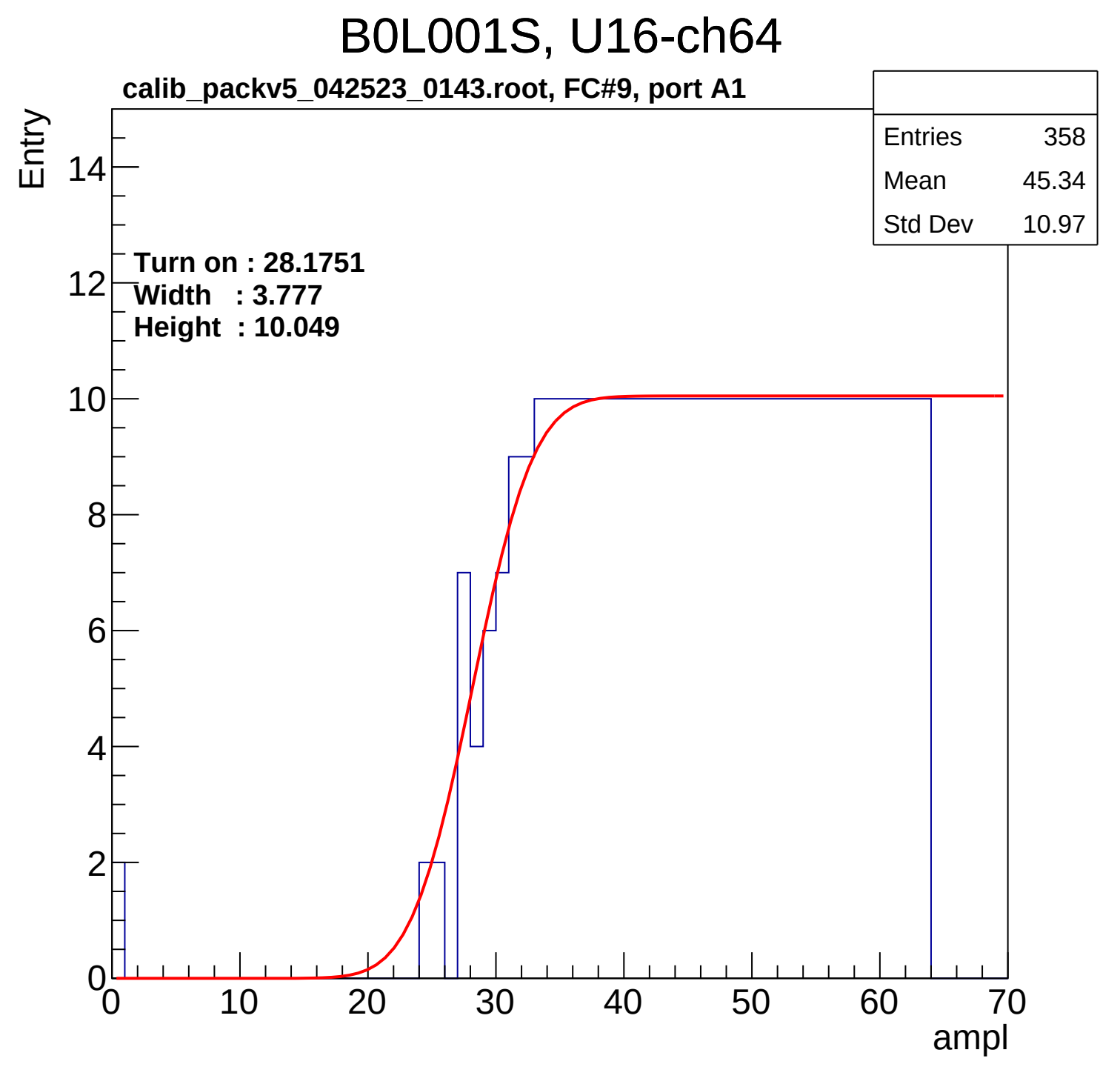
B0L001S, U16-ch64
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.34
Std Dev 10.97
Turn on : 28.1751
Width : 3.777
Height : 10.049
Entry
ampl
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2
4
6
8
10
12
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0
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20
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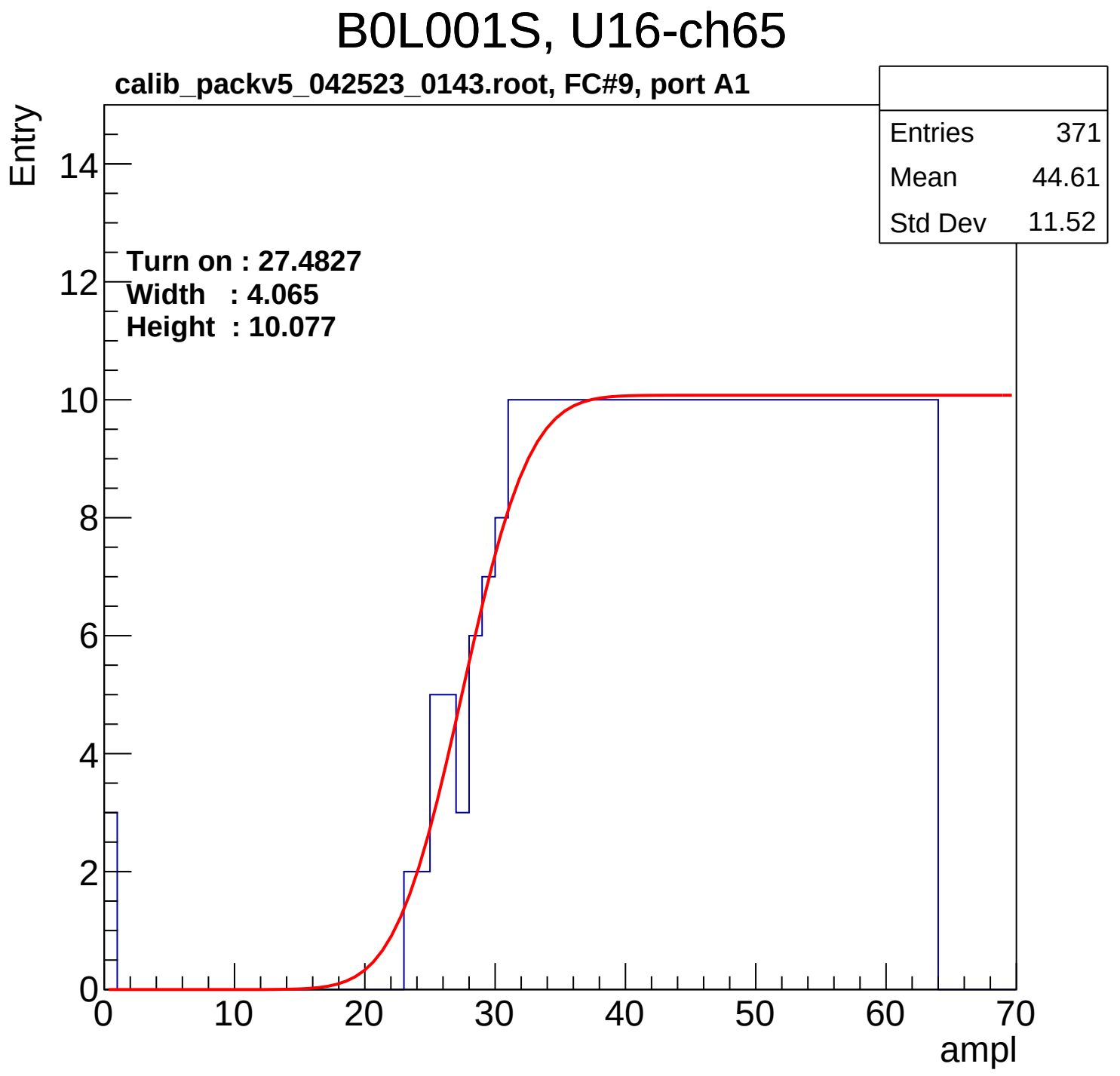
B0L001S, U16-ch65
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.61
Std Dev 11.52
Turn on : 27.4827
Width : 4.065
Height : 10.077
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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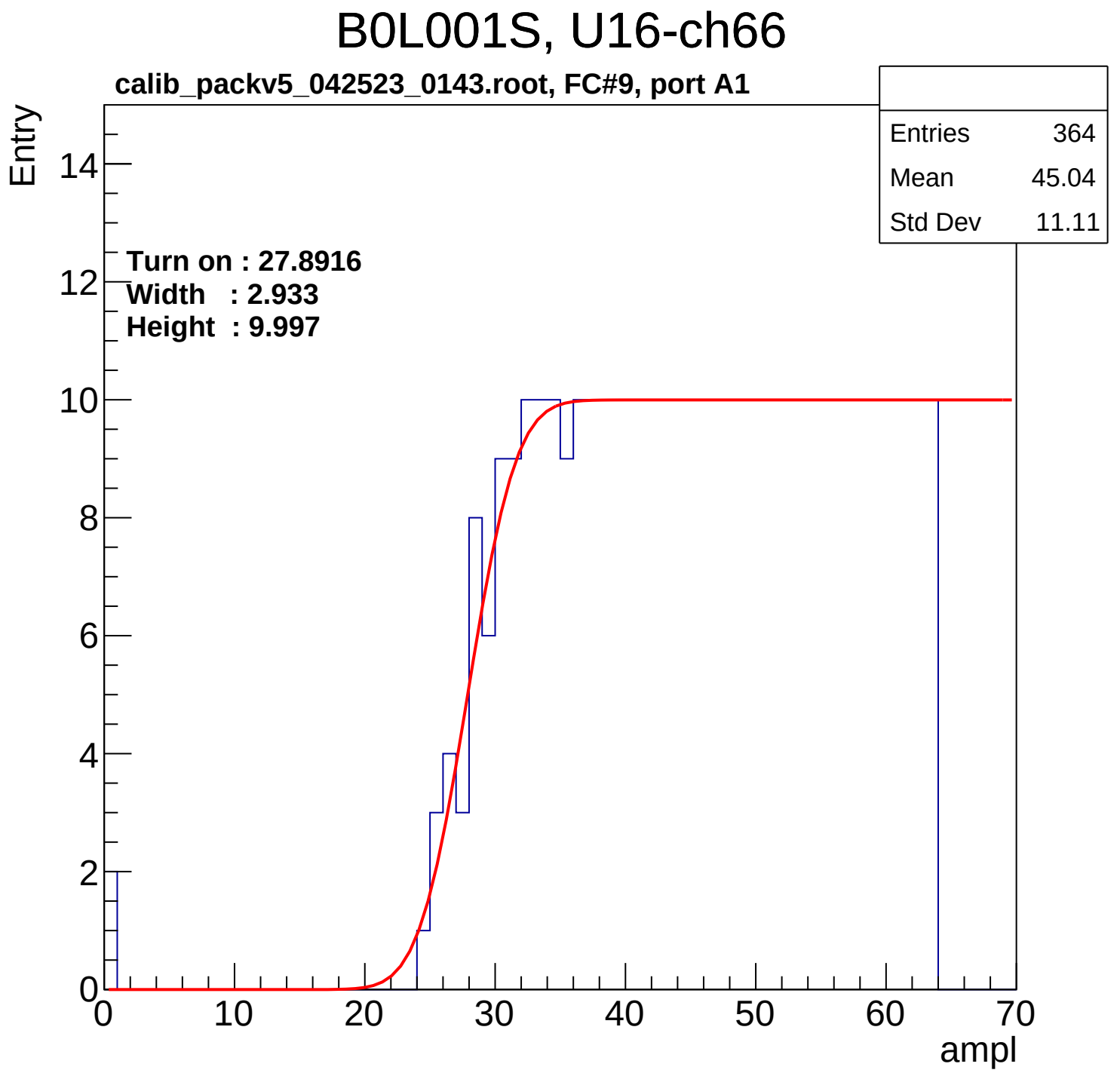
B0L001S, U16-ch66
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 45.04
Std Dev 11.11
Turn on : 27.8916
Width : 2.933
Height : 9.997
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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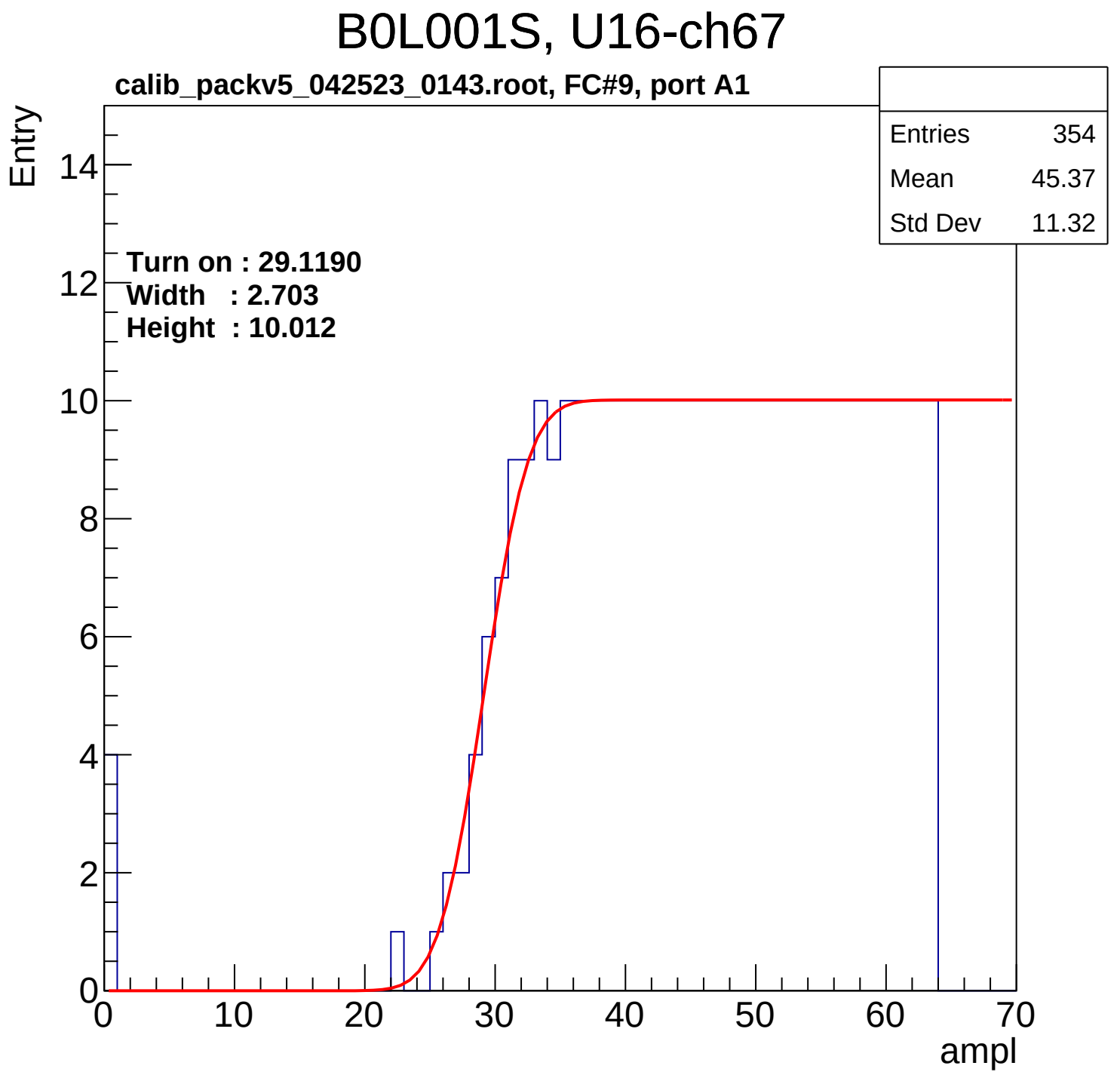
B0L001S, U16-ch67
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.37
Std Dev 11.32
Turn on : 29.1190
Width : 2.703
Height : 10.012
Entry
ampl
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2
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6
8
10
12
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0
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60
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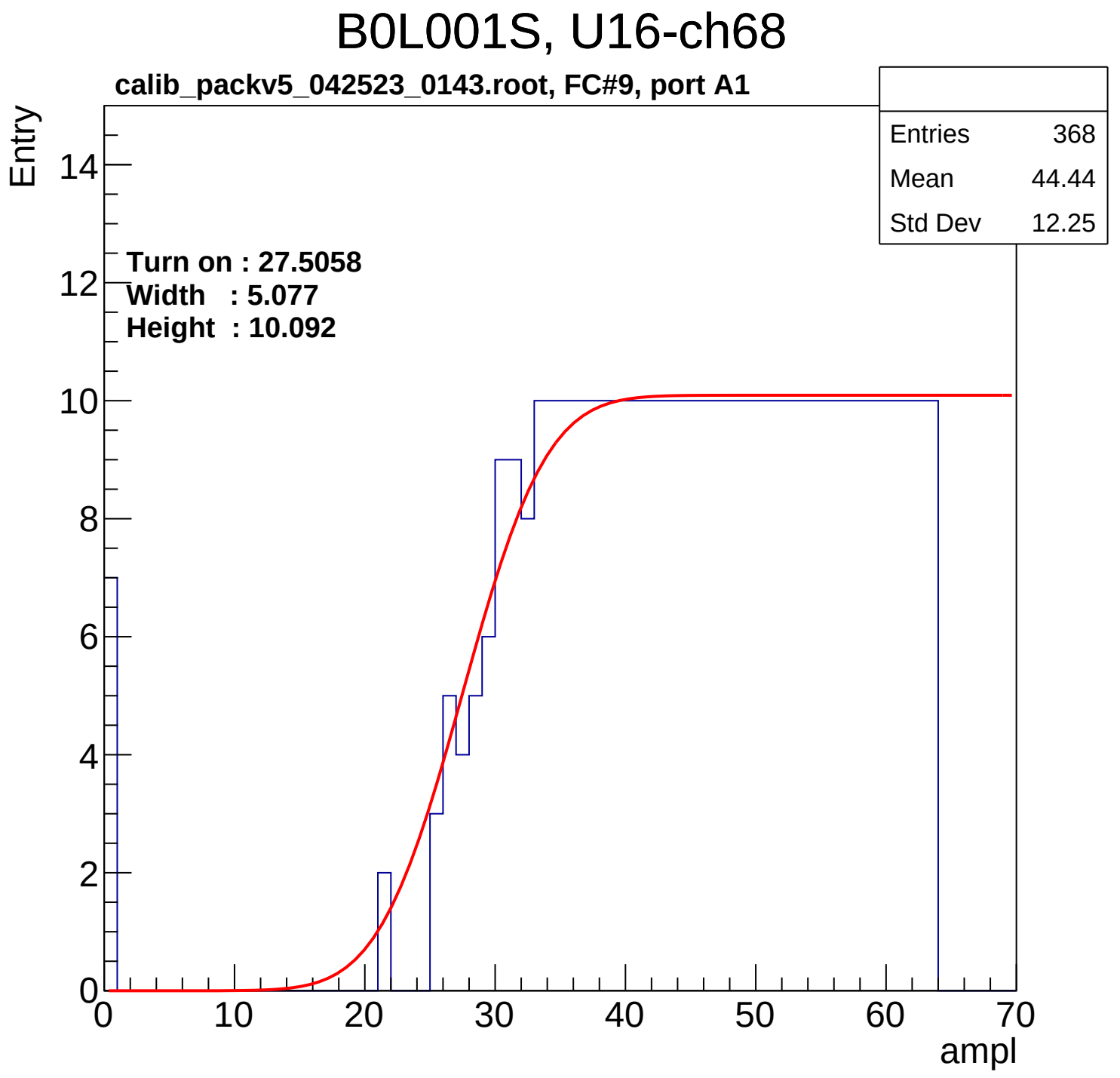
B0L001S, U16-ch68
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.44
Std Dev 12.25
Turn on : 27.5058
Width : 5.077
Height : 10.092
Entry
ampl
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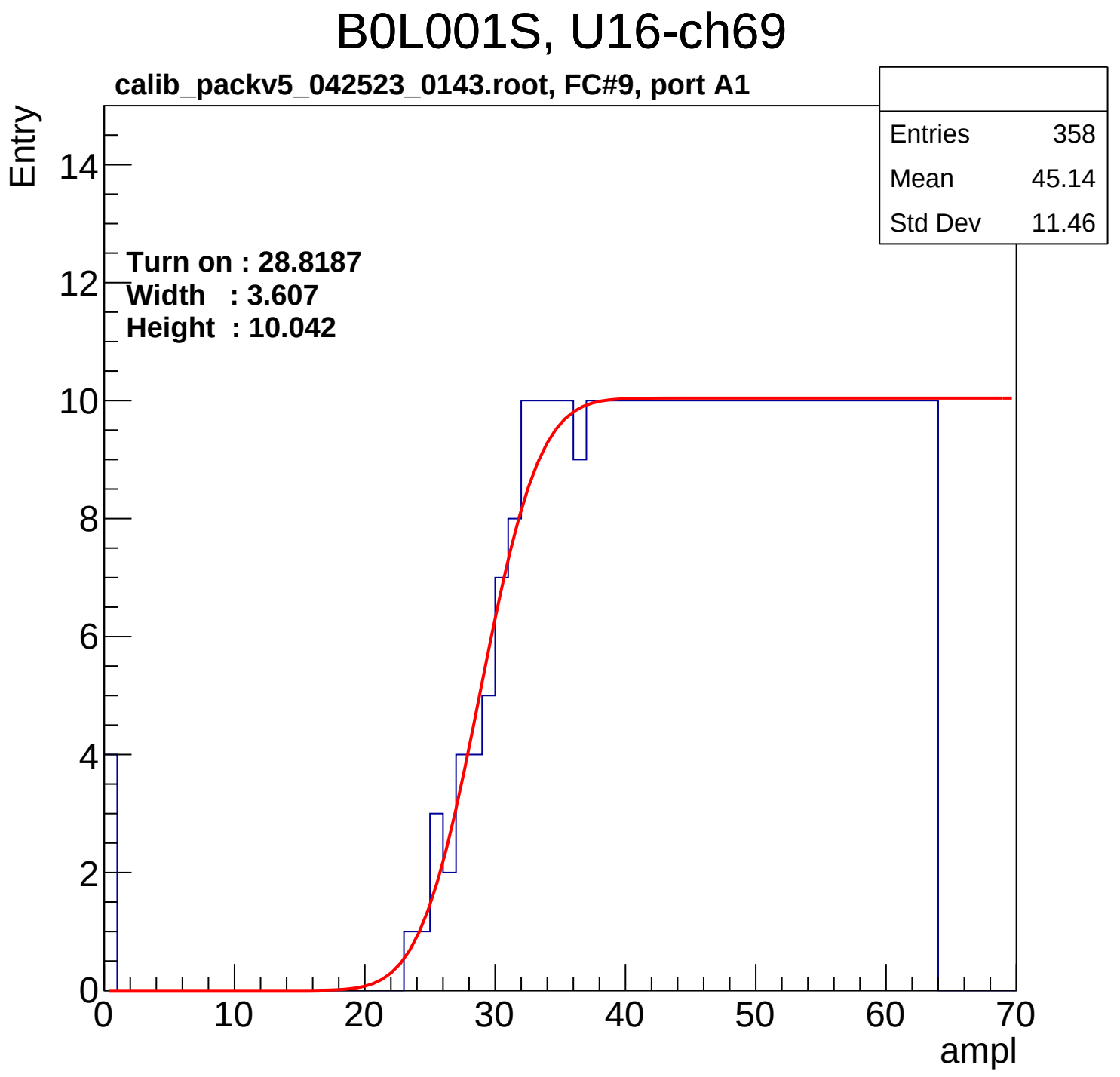
B0L001S, U16-ch69
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.14
Std Dev 11.46
Turn on : 28.8187
Width : 3.607
Height : 10.042
Entry
ampl
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6
8
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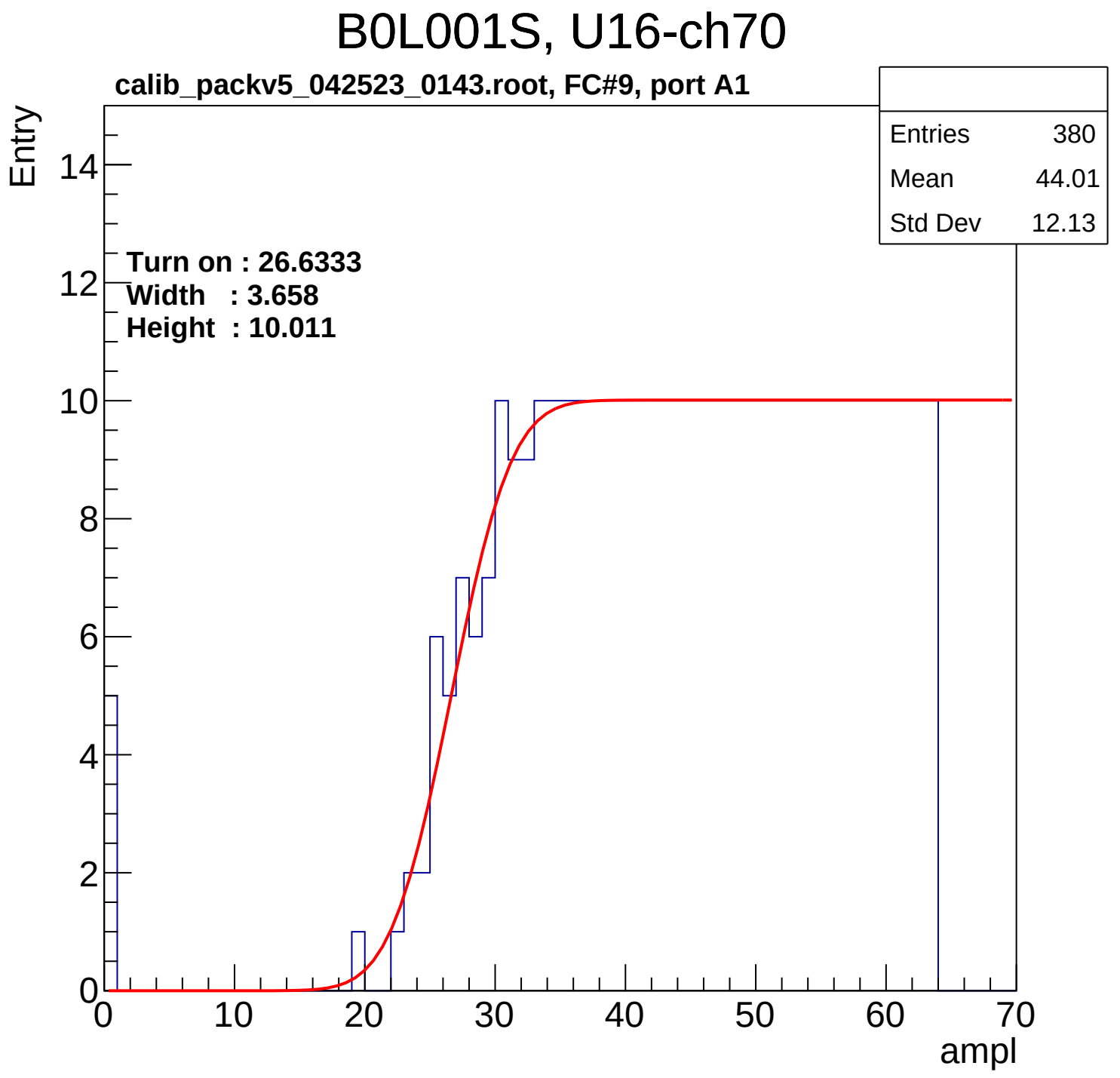
B0L001S, U16-ch70
calib_packv5_042523_0143.root, FC#9, port A1
Entries 380
Mean 44.01
Std Dev 12.13
Turn on : 26.6333
Width : 3.658
Height : 10.011
Entry
ampl
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8
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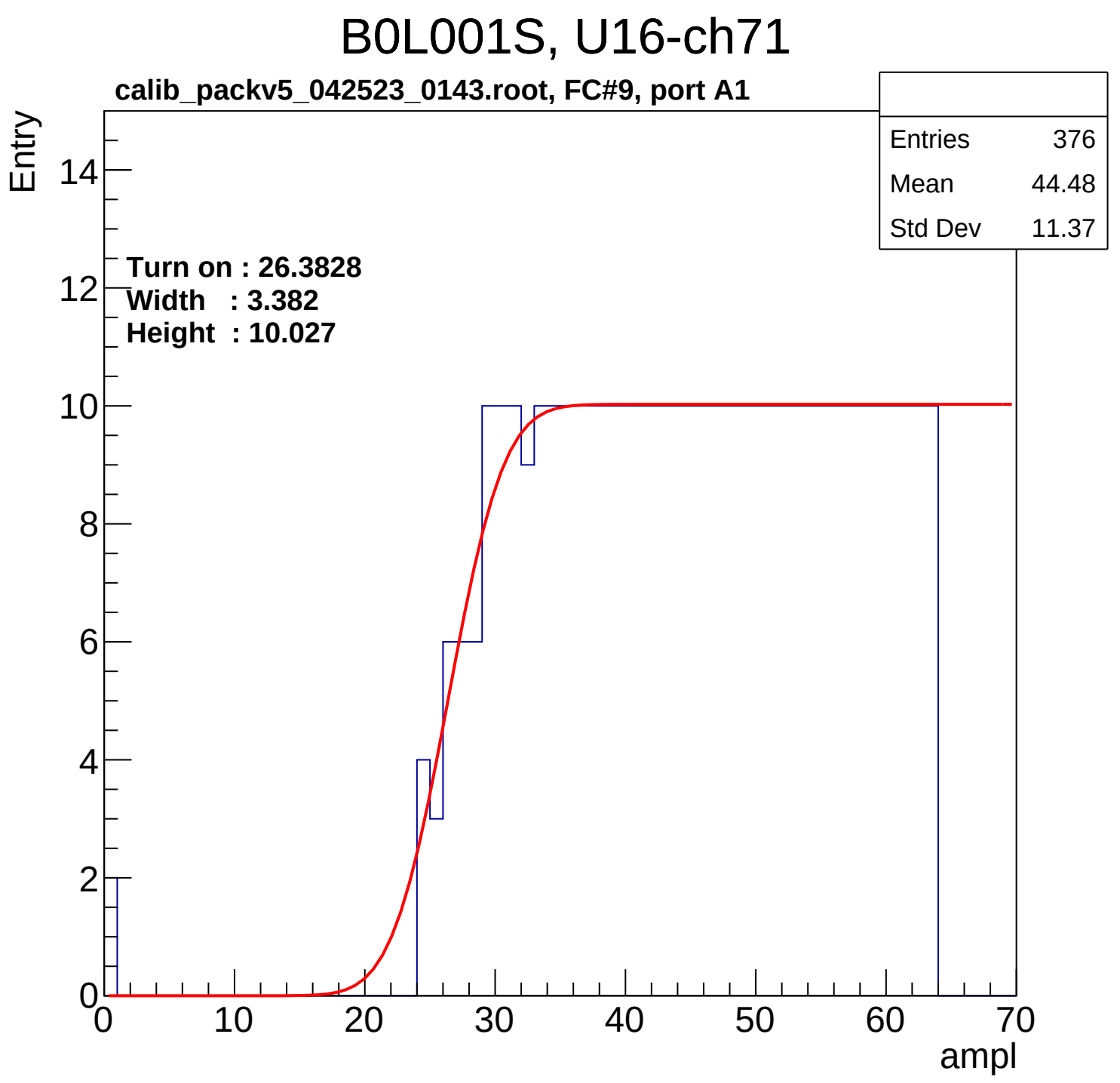
B0L001S, U16-ch71
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.48
Std Dev 11.37
Turn on : 26.3828
Width : 3.382
Height : 10.027
Entry
ampl
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6
8
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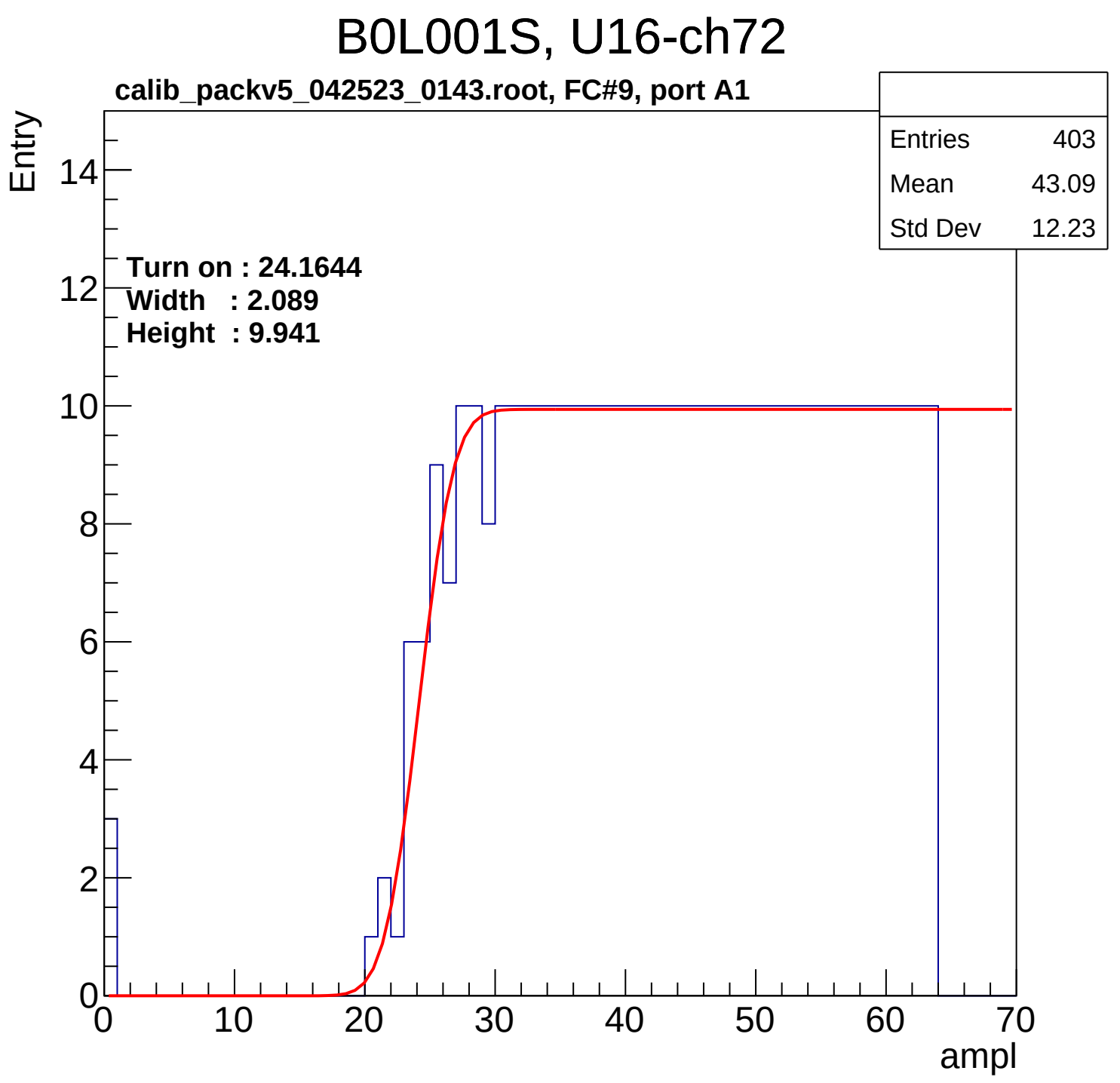
B0L001S, U16-ch72
calib_packv5_042523_0143.root, FC#9, port A1
Entries 403
Mean 43.09
Std Dev 12.23
Turn on : 24.1644
Width : 2.089
Height : 9.941
Entry
ampl
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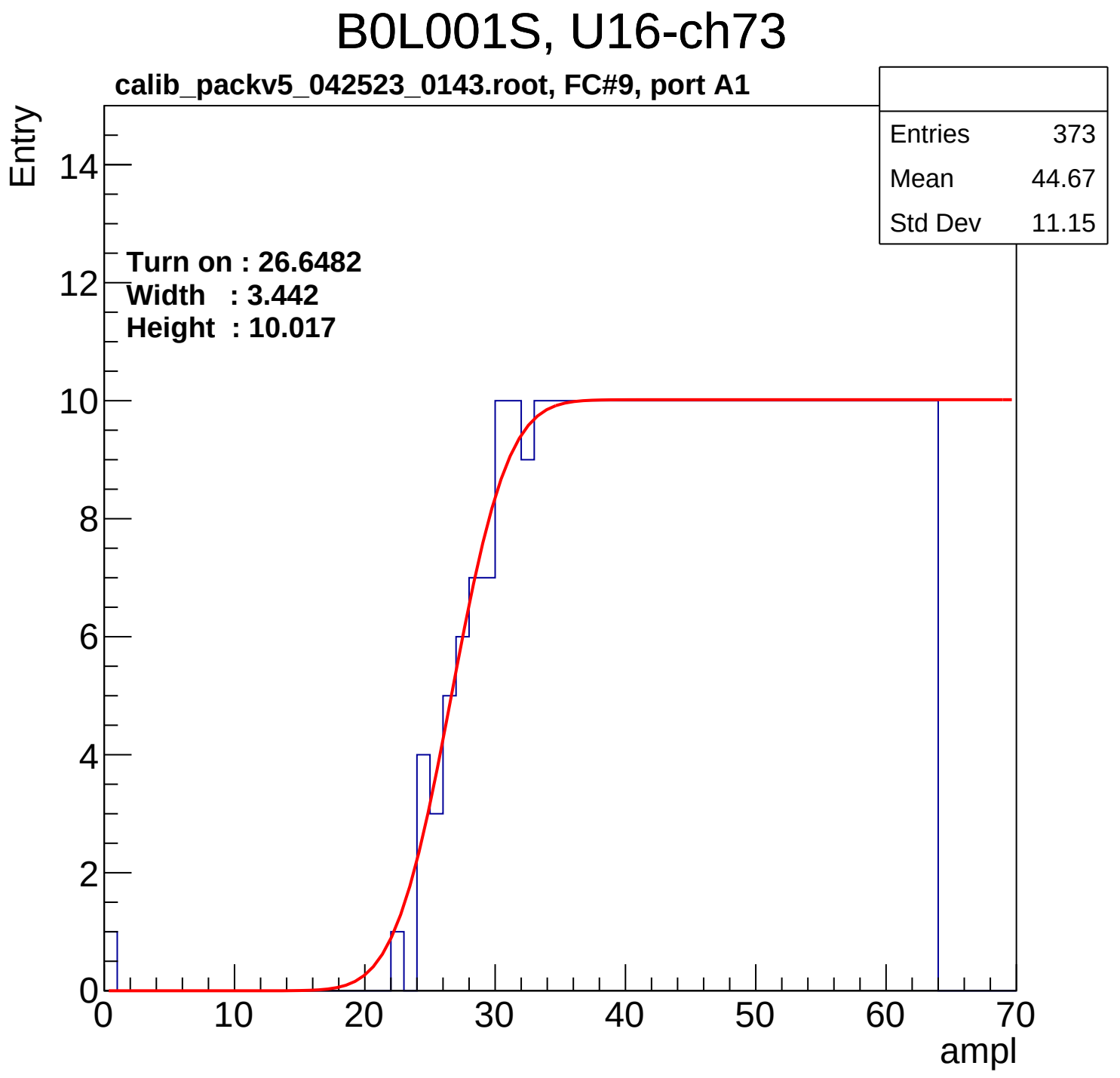
B0L001S, U16-ch73
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.67
Std Dev 11.15
Turn on : 26.6482
Width : 3.442
Height : 10.017
Entry
ampl
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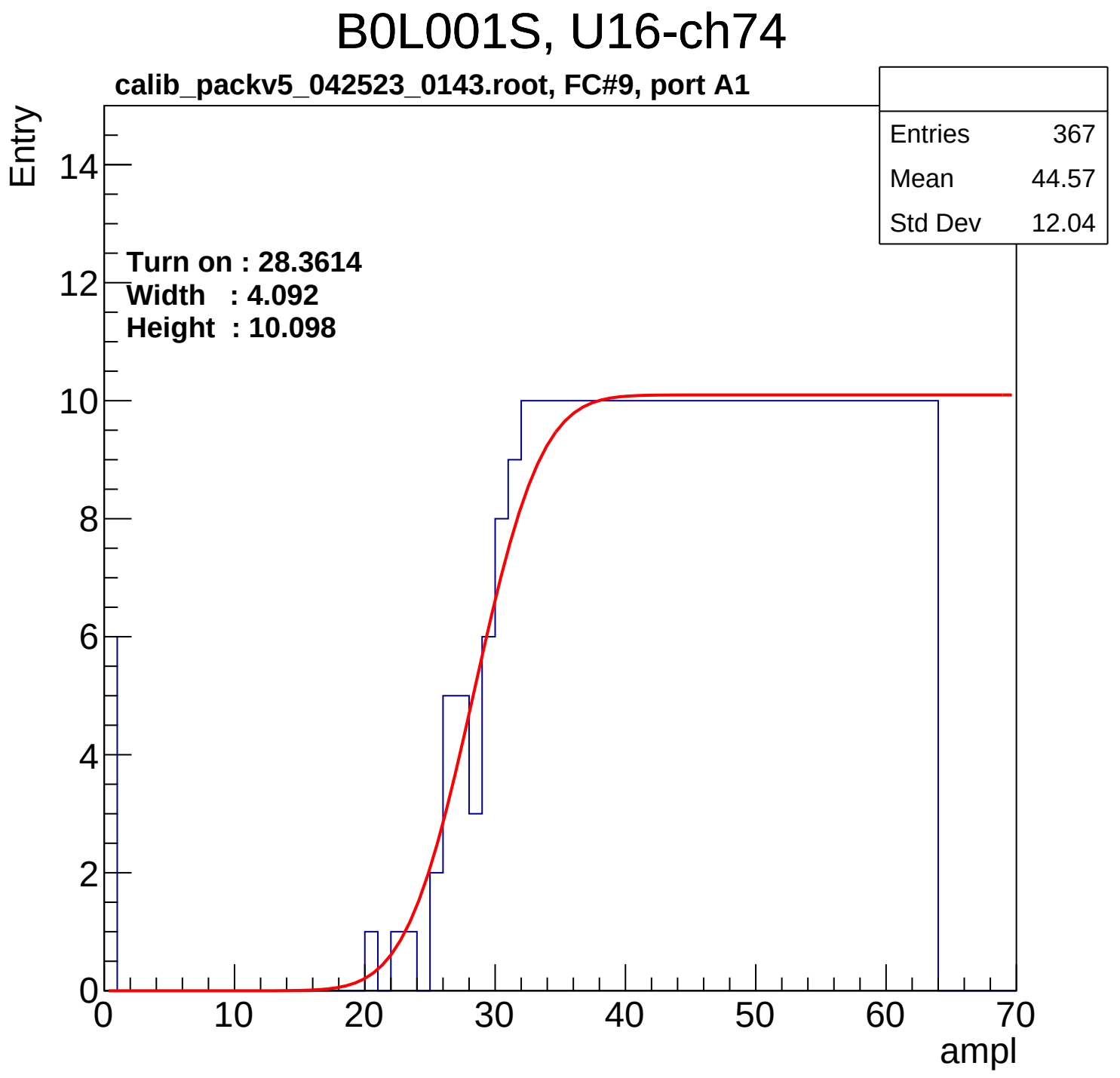
B0L001S, U16-ch74
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.57
Std Dev 12.04
Turn on : 28.3614
Width : 4.092
Height : 10.098
Entry
ampl
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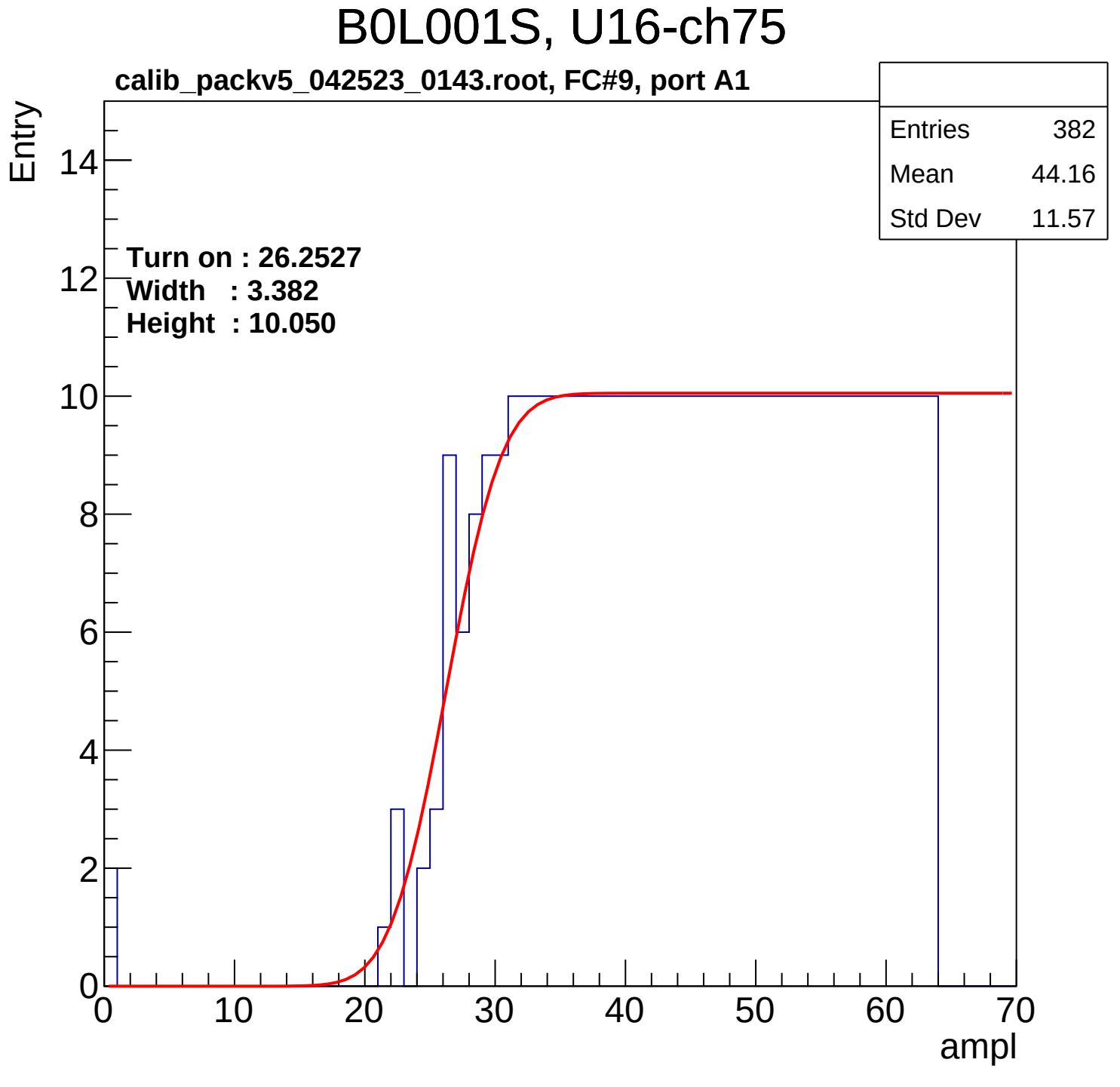
B0L001S, U16-ch75
calib_packv5_042523_0143.root, FC#9, port A1
Entries 382
Mean 44.16
Std Dev 11.57
Turn on : 26.2527
Width : 3.382
Height : 10.050
Entry
ampl
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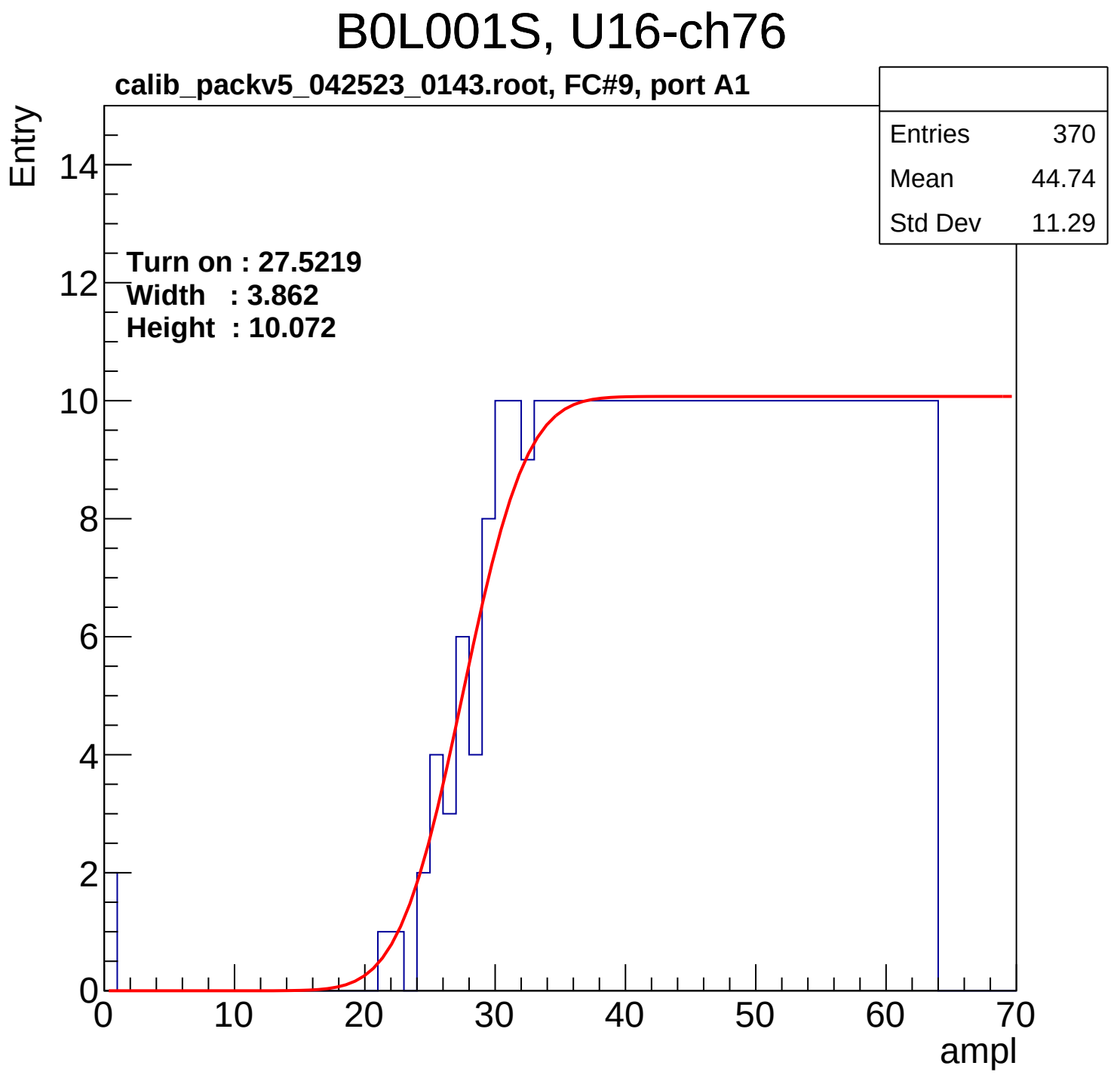
B0L001S, U16-ch76
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.74
Std Dev 11.29
Turn on : 27.5219
Width : 3.862
Height : 10.072
Entry
ampl
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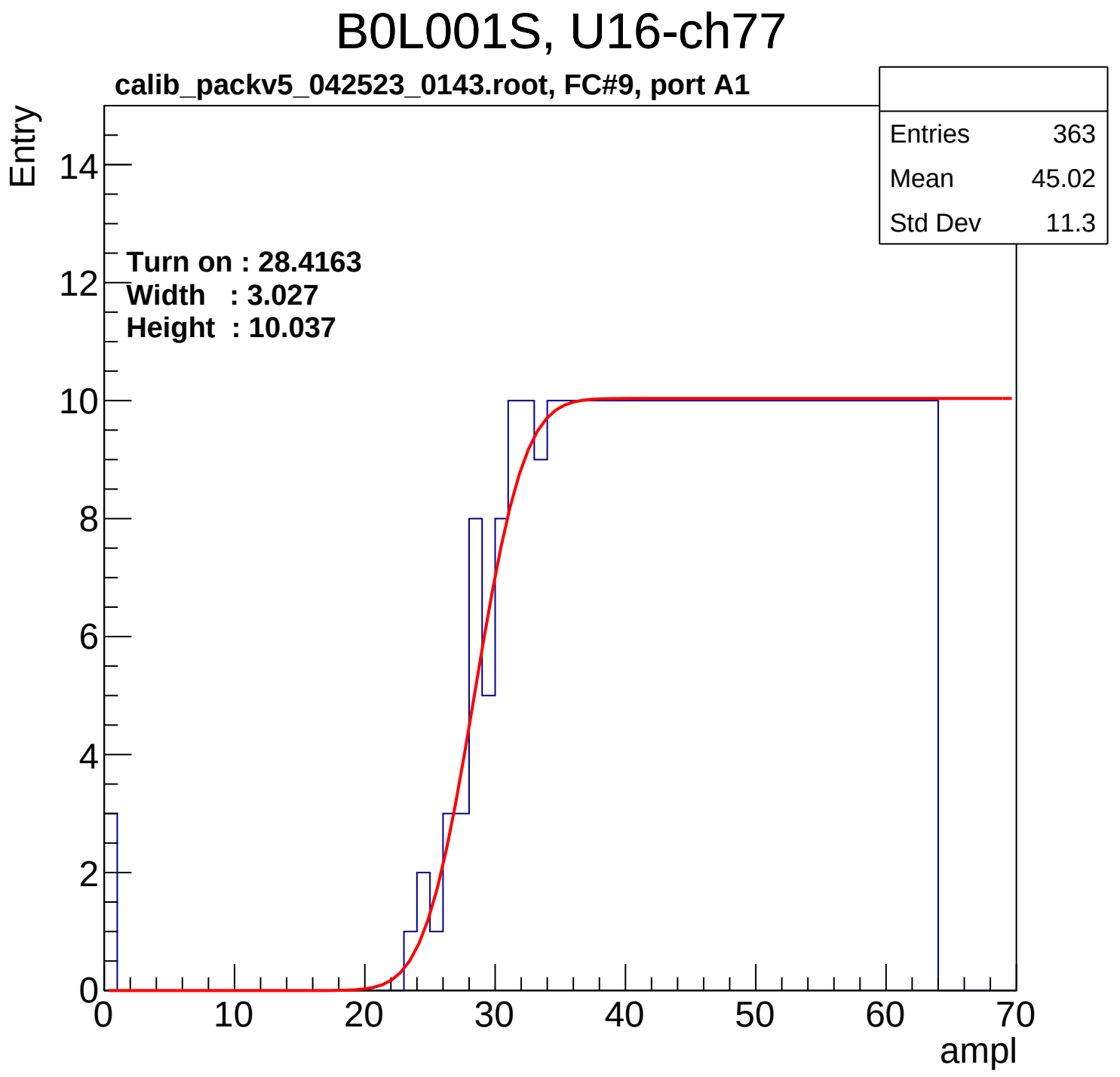
B0L001S, U16-ch77
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.02
Std Dev 11.3
Turn on : 28.4163
Width : 3.027
Height : 10.037
Entry
ampl
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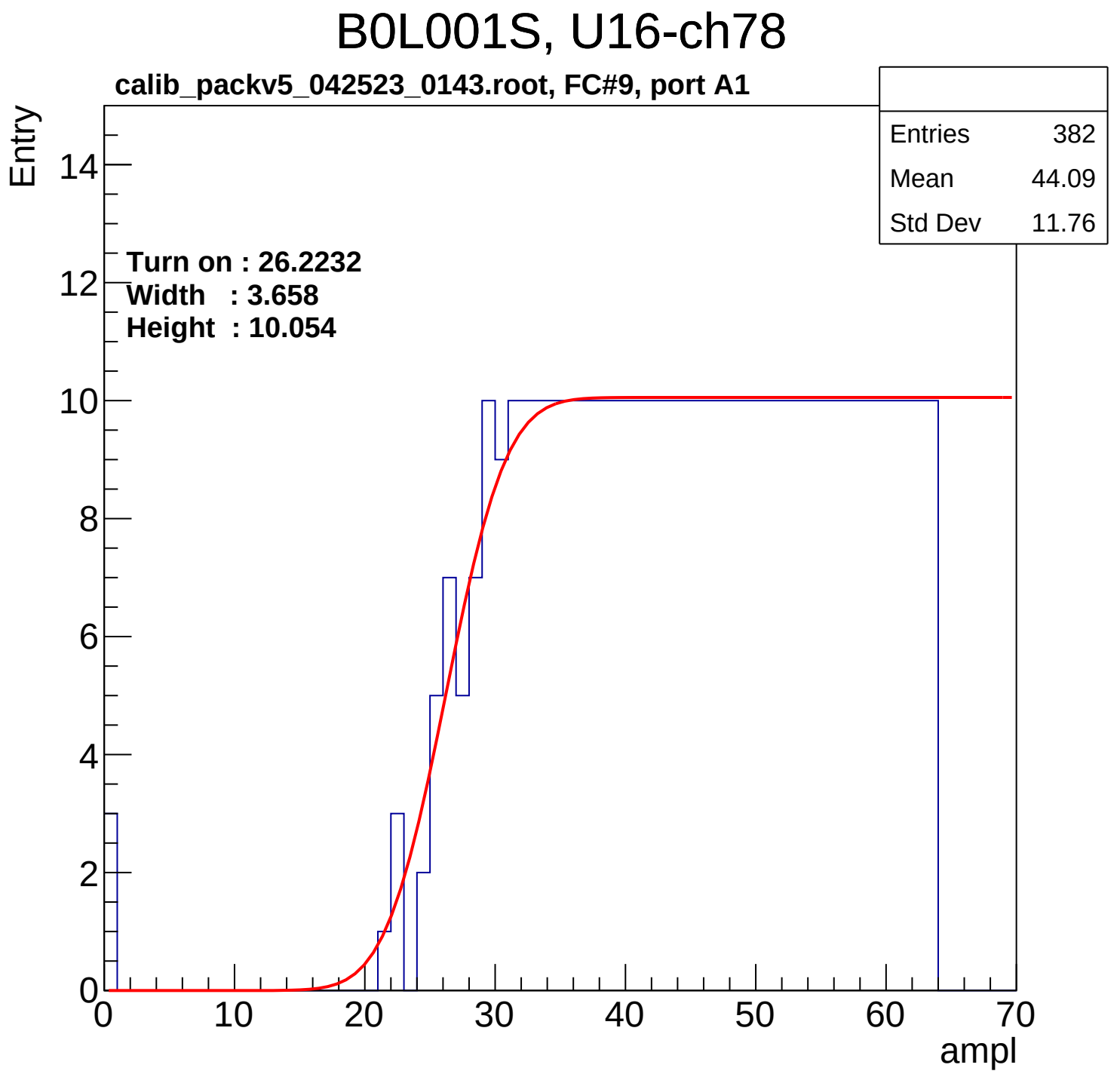
B0L001S, U16-ch78
calib_packv5_042523_0143.root, FC#9, port A1
Entries 382
Mean 44.09
Std Dev 11.76
Turn on : 26.2232
Width : 3.658
Height : 10.054
Entry
ampl
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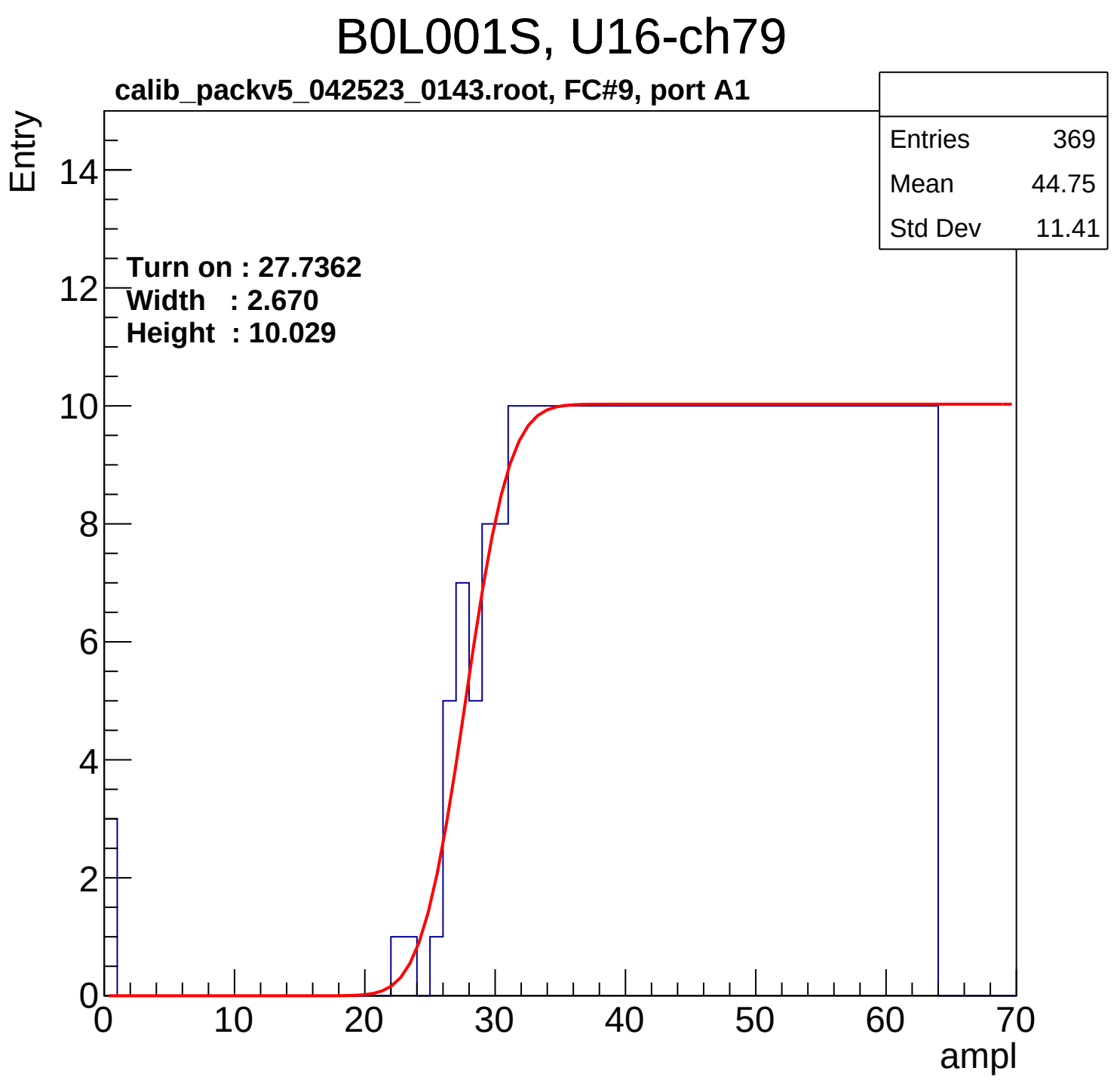
B0L001S, U16-ch79
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.75
Std Dev 11.41
Turn on : 27.7362
Width : 2.670
Height : 10.029
Entry
ampl
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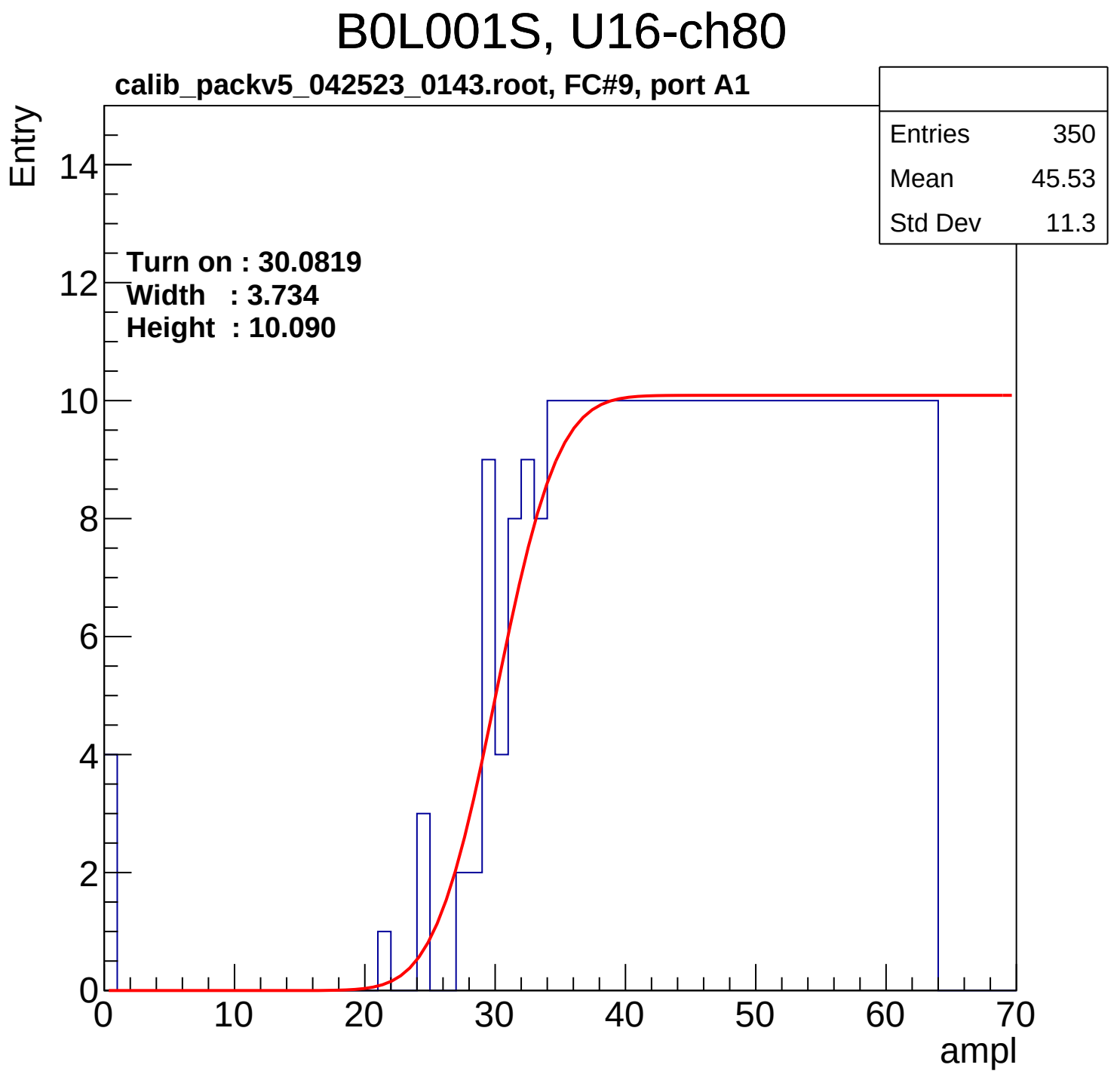
B0L001S, U16-ch80
calib_packv5_042523_0143.root, FC#9, port A1
Entries 350
Mean 45.53
Std Dev 11.3
Turn on : 30.0819
Width : 3.734
Height : 10.090
Entry
ampl
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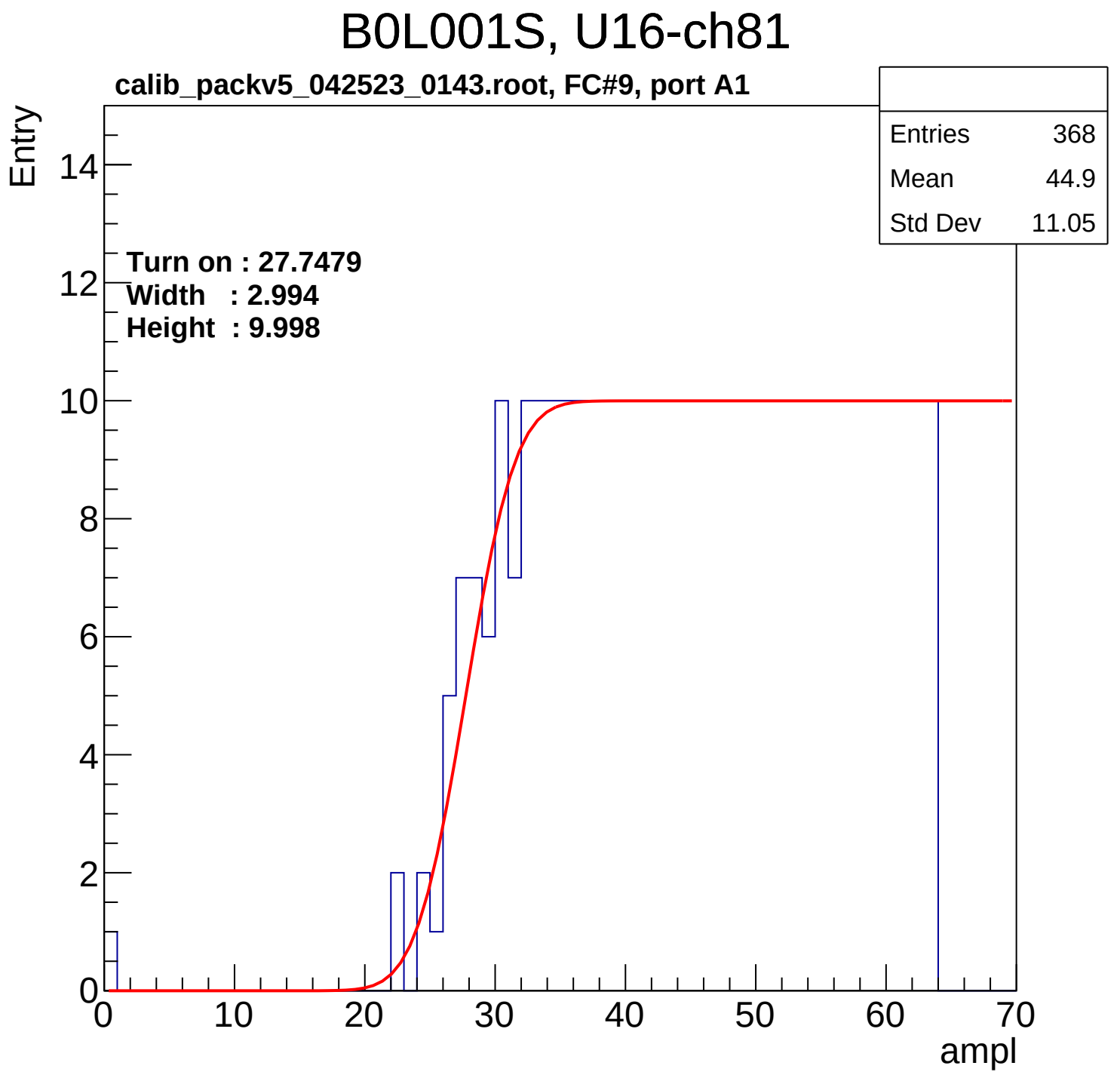
B0L001S, U16-ch81
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.9
Std Dev 11.05
Turn on : 27.7479
Width : 2.994
Height : 9.998
Entry
ampl
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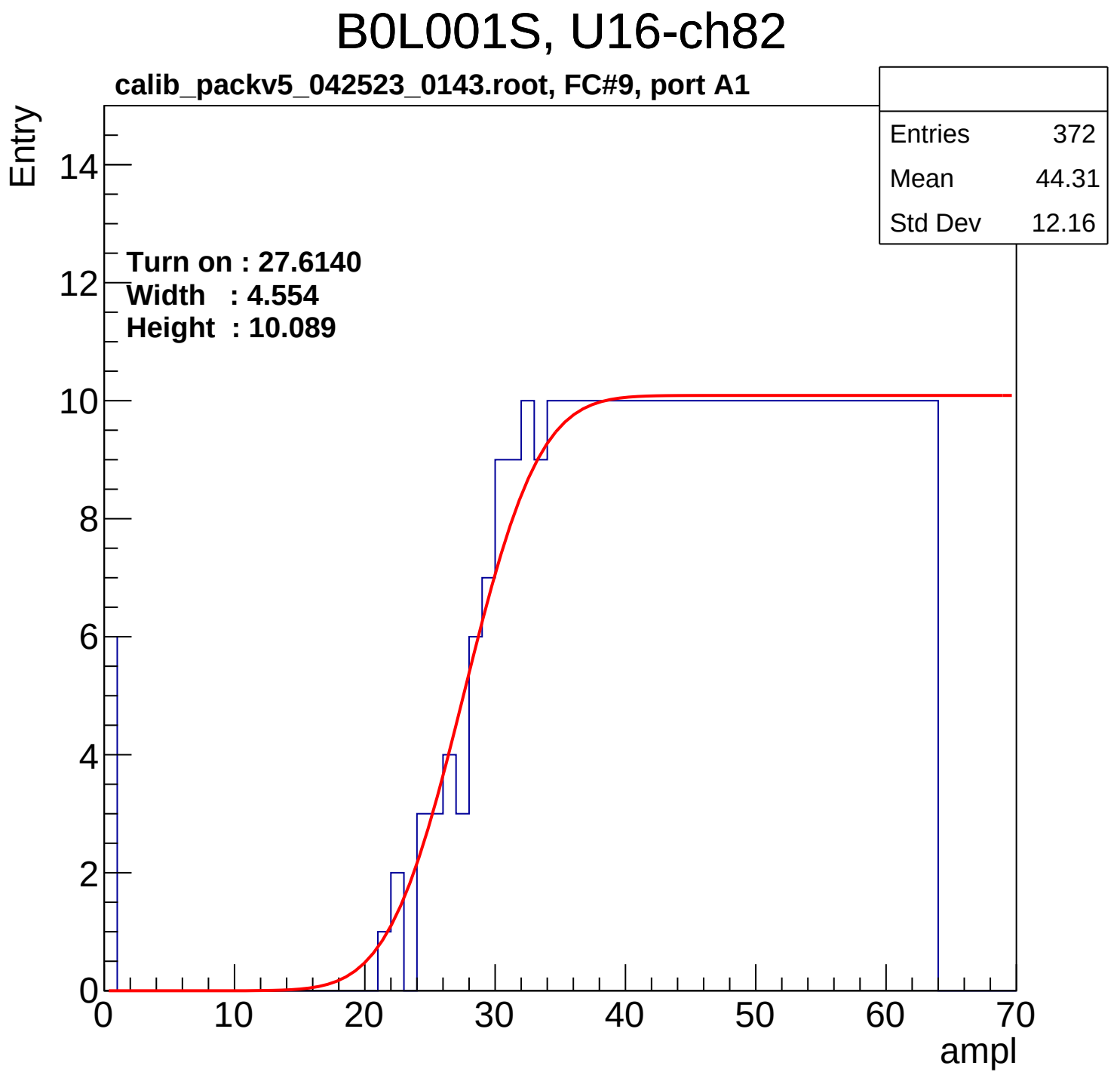
B0L001S, U16-ch82
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.31
Std Dev 12.16
Turn on : 27.6140
Width : 4.554
Height : 10.089
Entry
ampl
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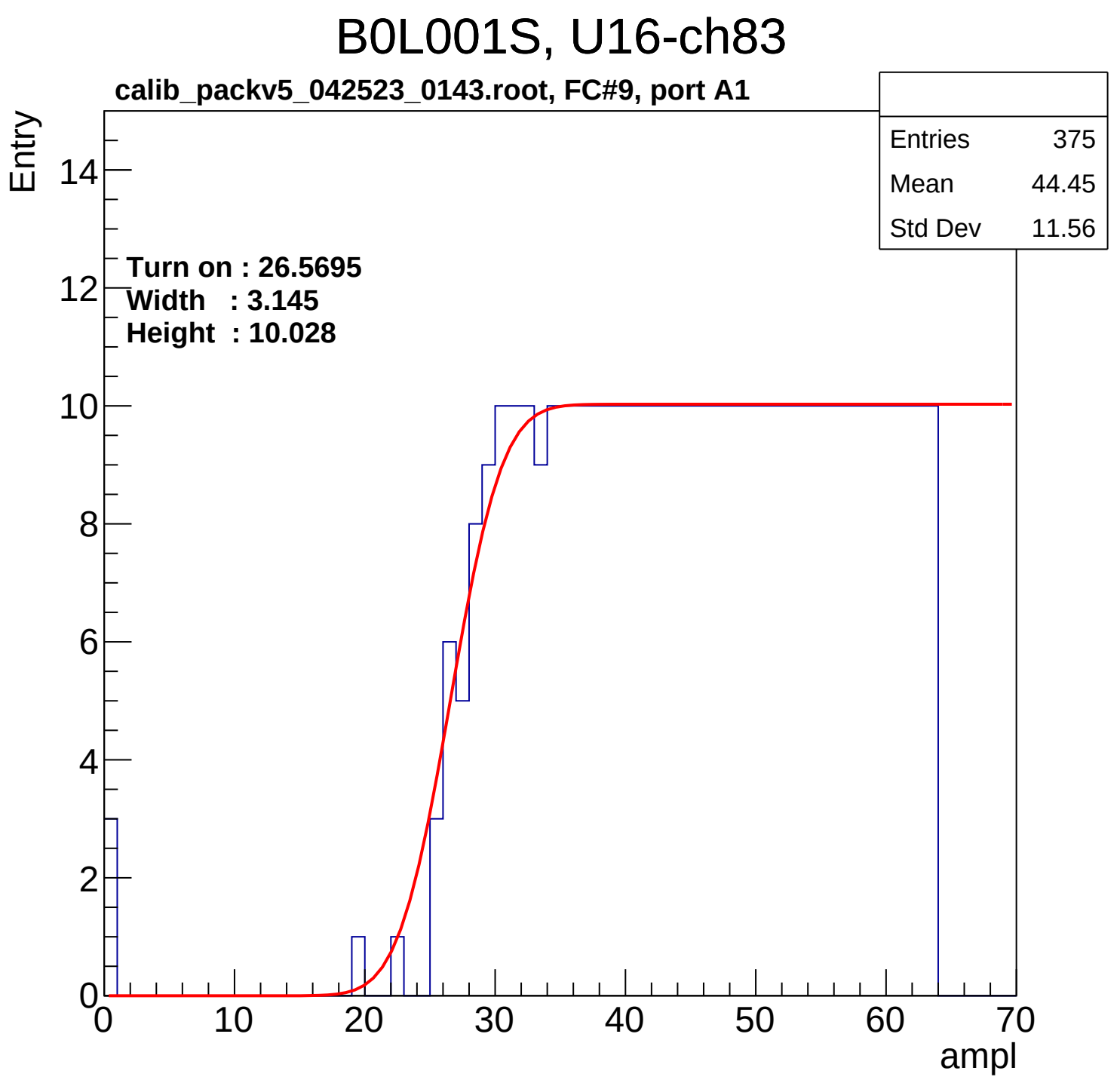
B0L001S, U16-ch83
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.45
Std Dev 11.56
Turn on : 26.5695
Width : 3.145
Height : 10.028
Entry
ampl
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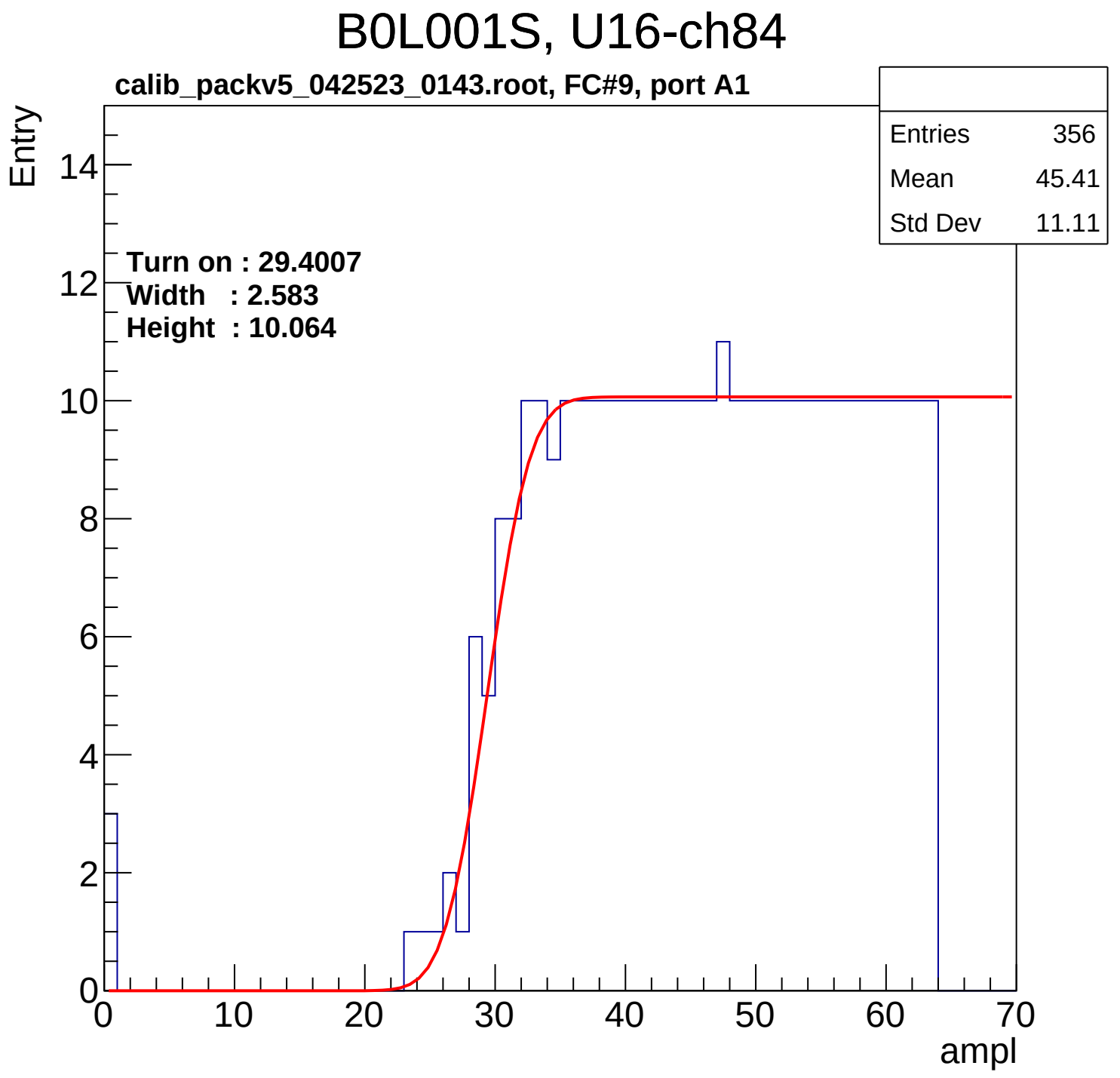
B0L001S, U16-ch84
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.41
Std Dev 11.11
Turn on : 29.4007
Width : 2.583
Height : 10.064
Entry
ampl
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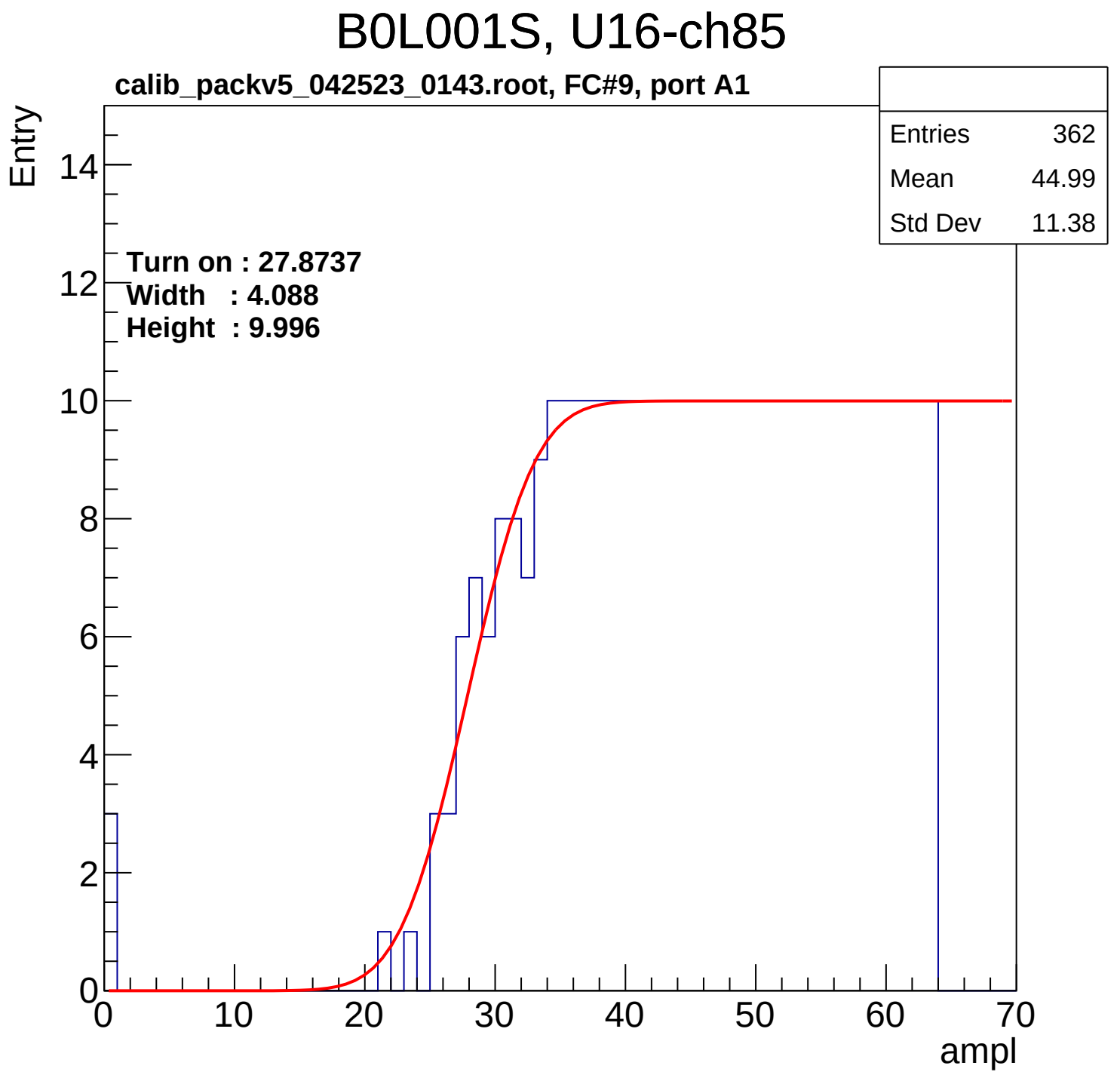
B0L001S, U16-ch85
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 44.99
Std Dev 11.38
Turn on : 27.8737
Width : 4.088
Height : 9.996
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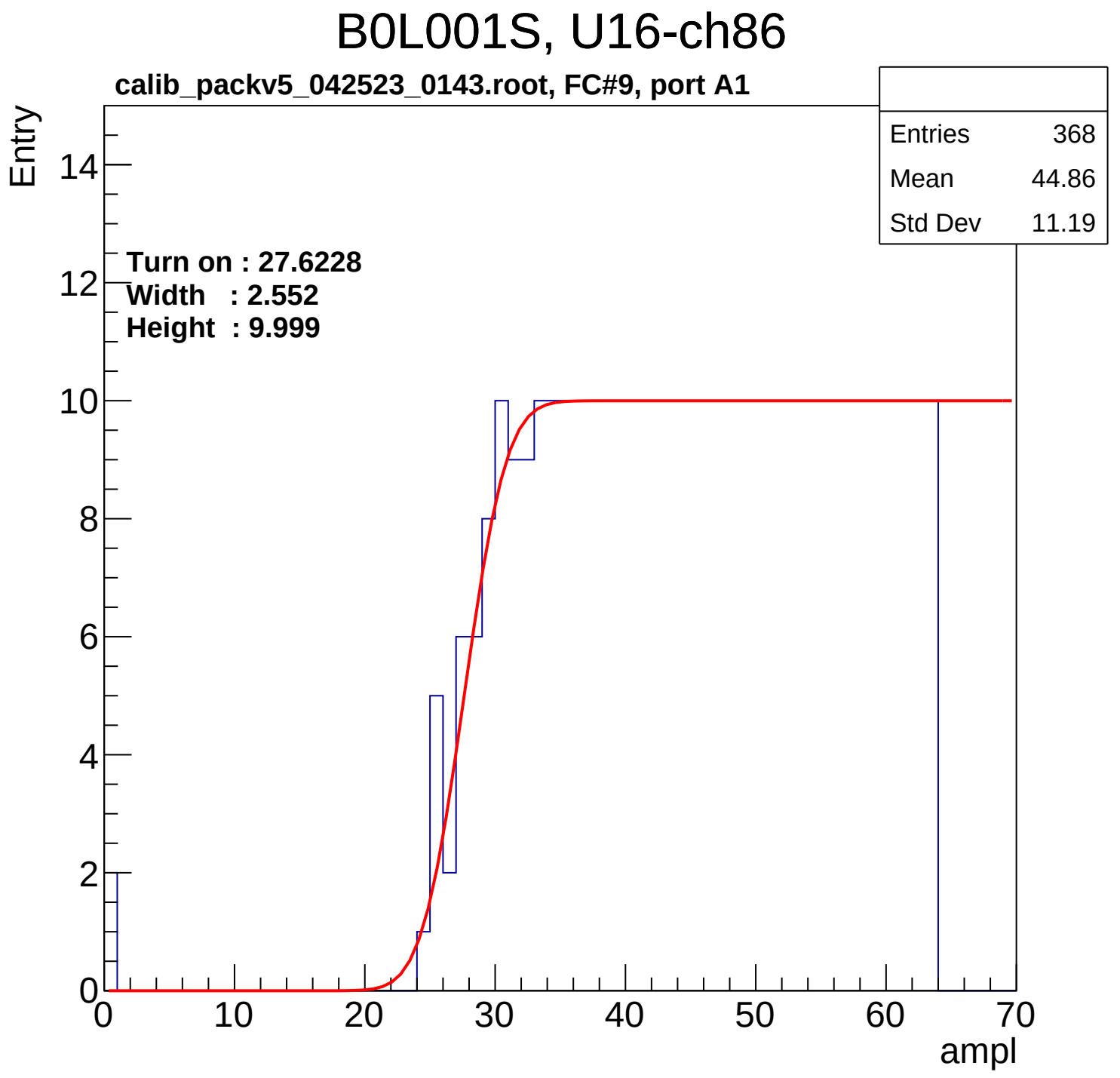
B0L001S, U16-ch86
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.86
Std Dev 11.19
Turn on : 27.6228
Width : 2.552
Height : 9.999
Entry
ampl
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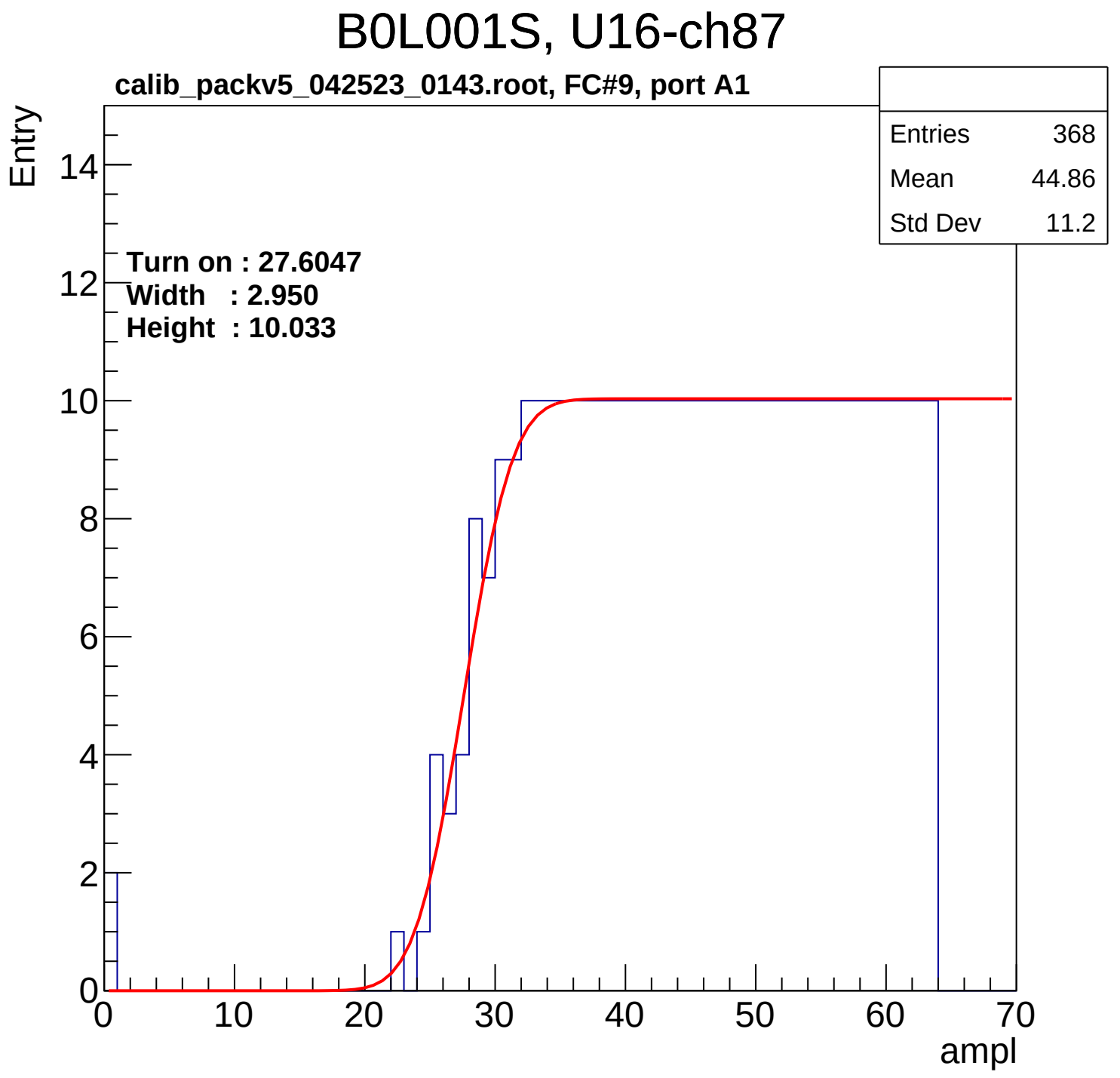
B0L001S, U16-ch87
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.86
Std Dev 11.2
Turn on : 27.6047
Width : 2.950
Height : 10.033
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ampl
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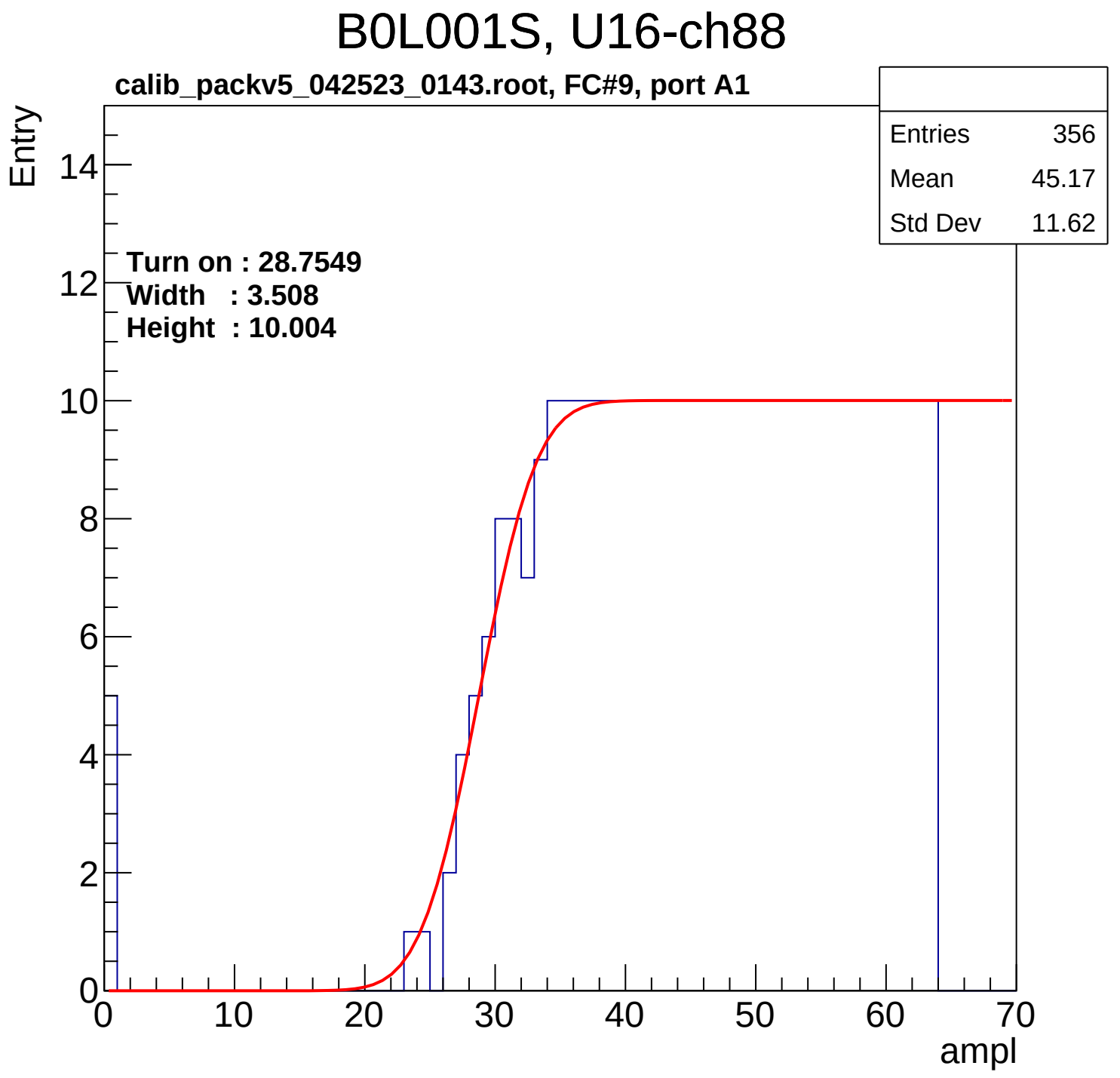
B0L001S, U16-ch88
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.17
Std Dev 11.62
Turn on : 28.7549
Width : 3.508
Height : 10.004
Entry
ampl
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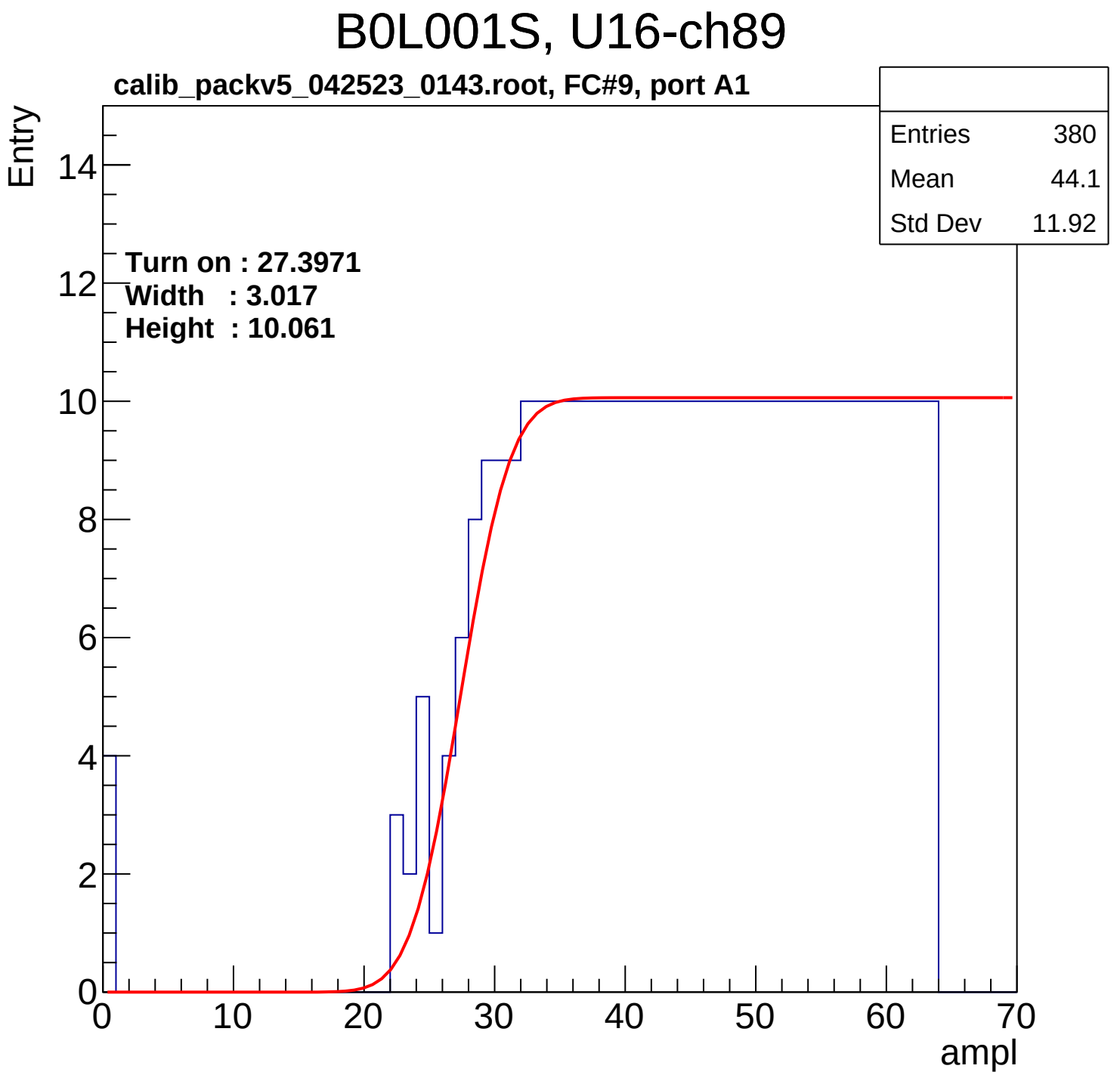
B0L001S, U16-ch89
calib_packv5_042523_0143.root, FC#9, port A1
Entries 380
Mean 44.1
Std Dev 11.92
Turn on : 27.3971
Width : 3.017
Height : 10.061
Entry
ampl
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2
4
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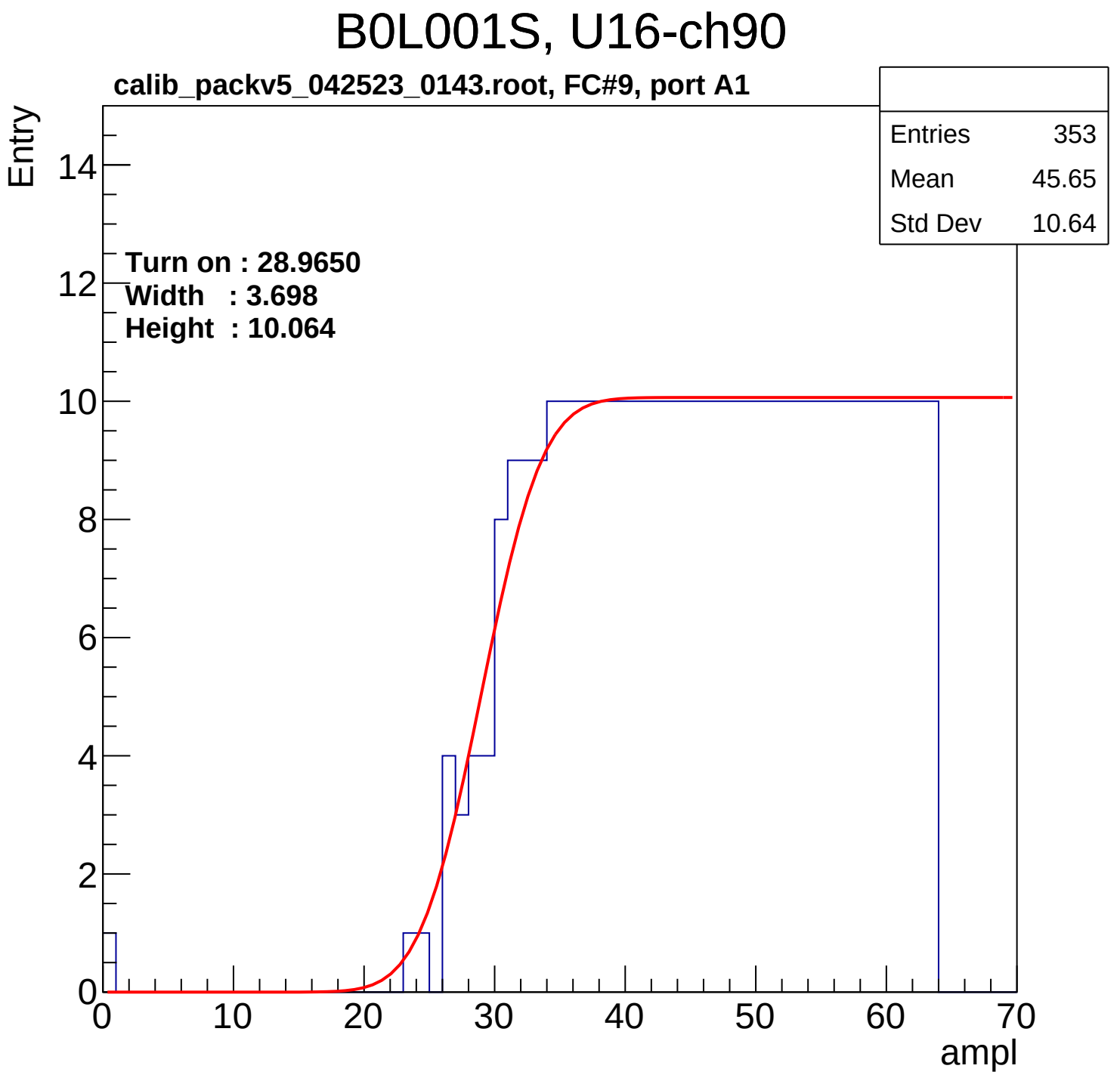
B0L001S, U16-ch90
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.65
Std Dev 10.64
Turn on : 28.9650
Width : 3.698
Height : 10.064
Entry
ampl
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4
6
8
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12
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0
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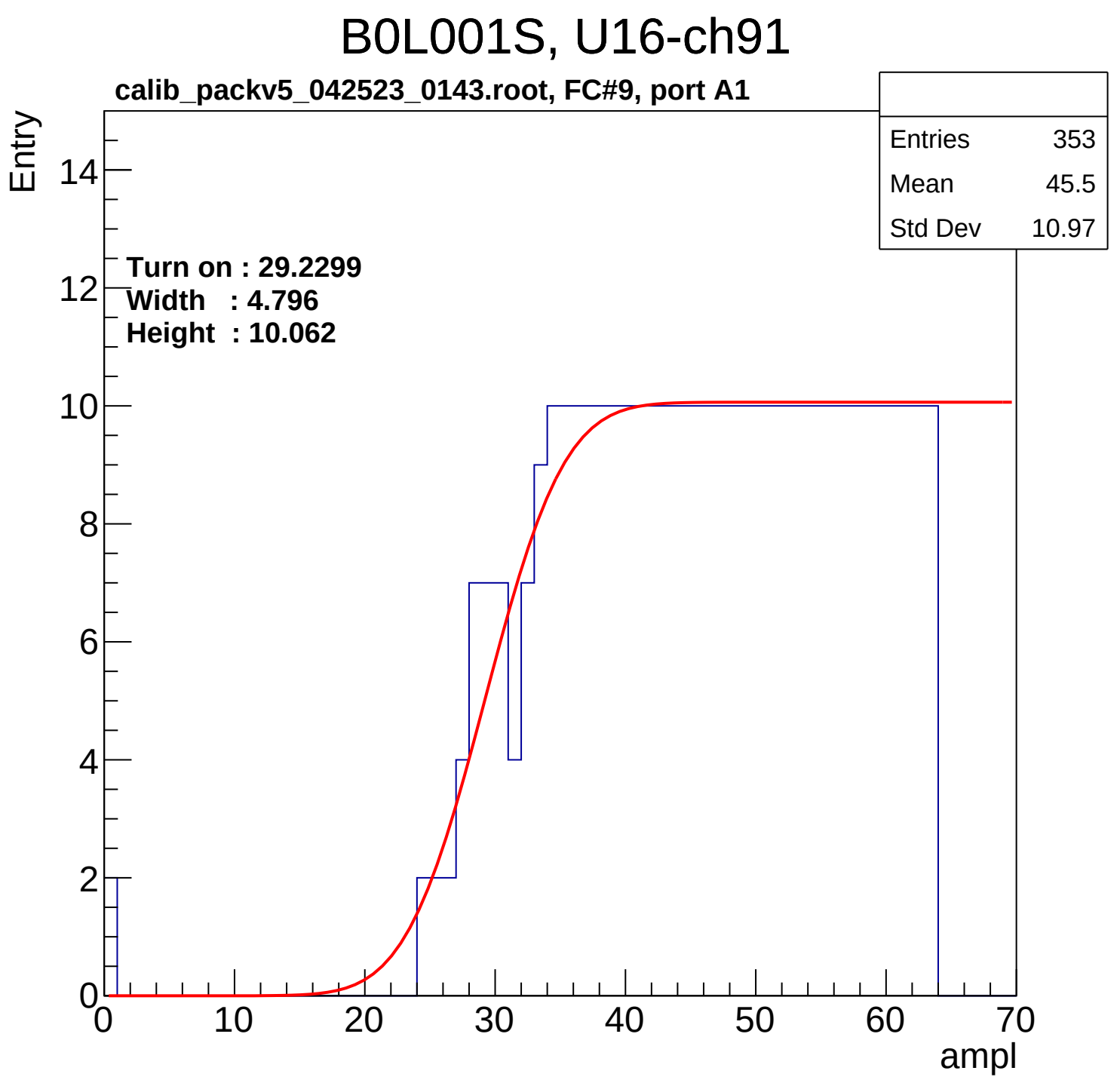
B0L001S, U16-ch91
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.5
Std Dev 10.97
Turn on : 29.2299
Width : 4.796
Height : 10.062
Entry
ampl
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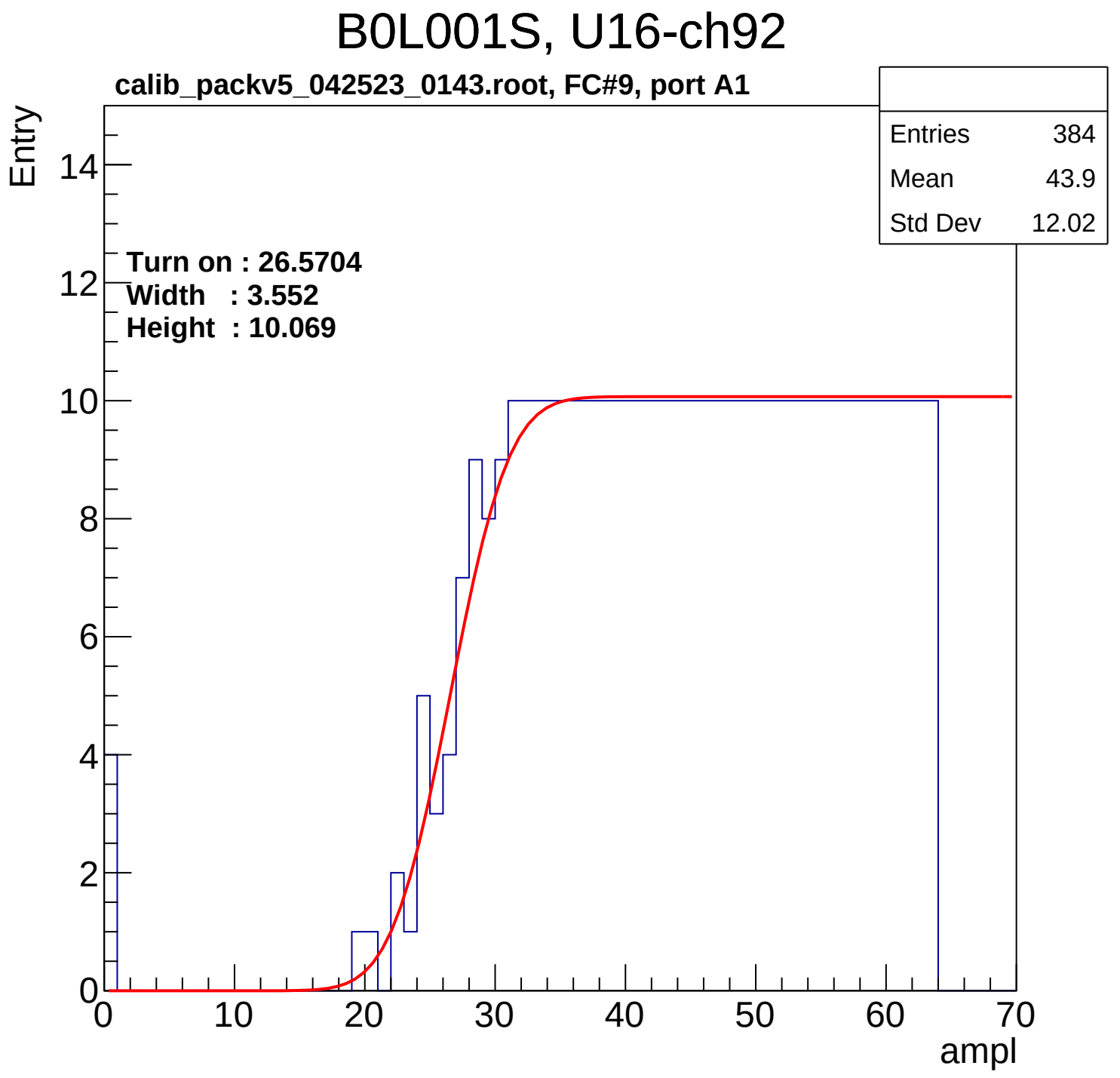
B0L001S, U16-ch92
calib_packv5_042523_0143.root, FC#9, port A1
Entries 384
Mean 43.9
Std Dev 12.02
Turn on : 26.5704
Width : 3.552
Height : 10.069
Entry
ampl
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6
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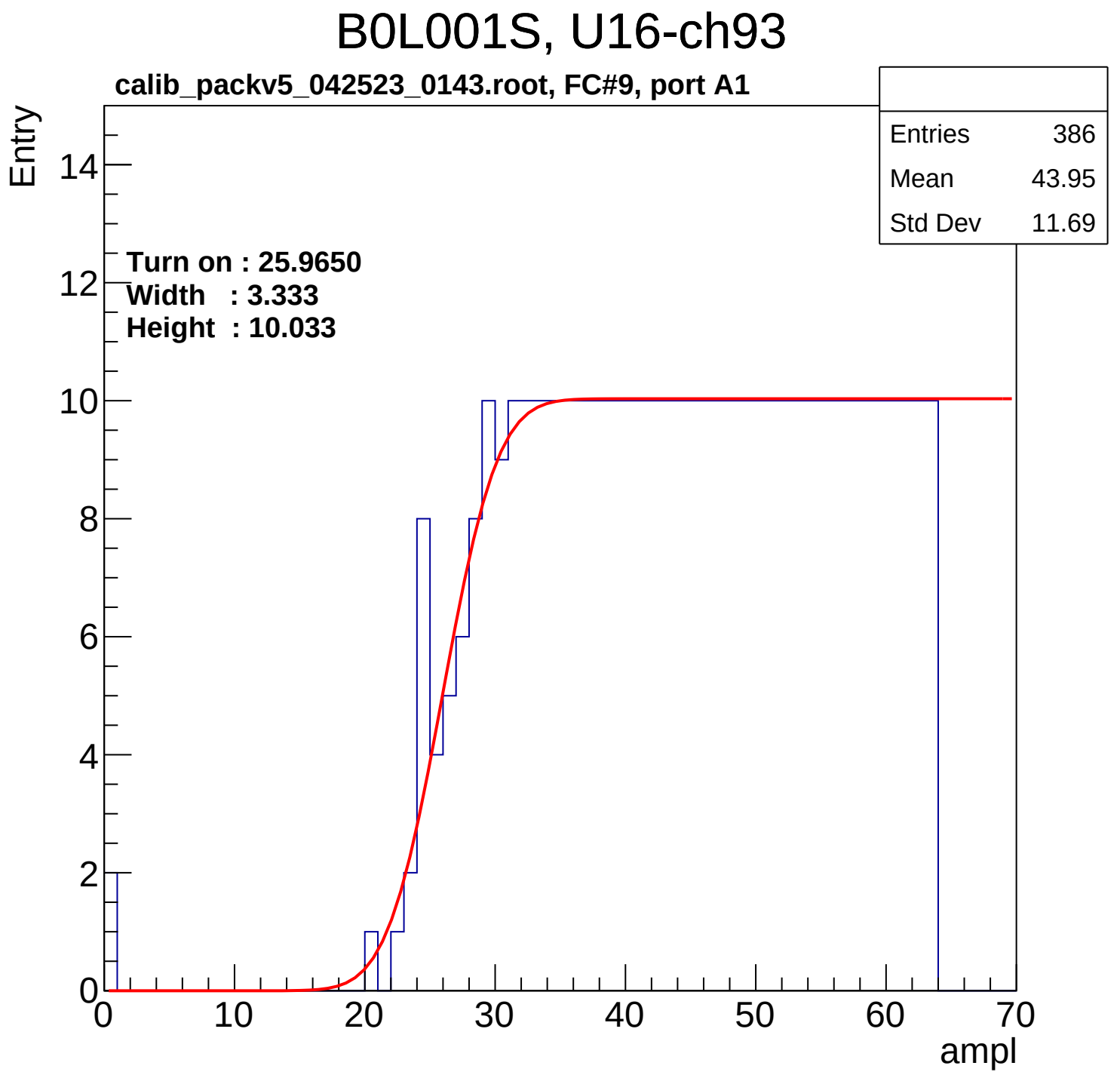
B0L001S, U16-ch93
calib_packv5_042523_0143.root, FC#9, port A1
Entries 386
Mean 43.95
Std Dev 11.69
Turn on : 25.9650
Width : 3.333
Height : 10.033
Entry
ampl
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6
8
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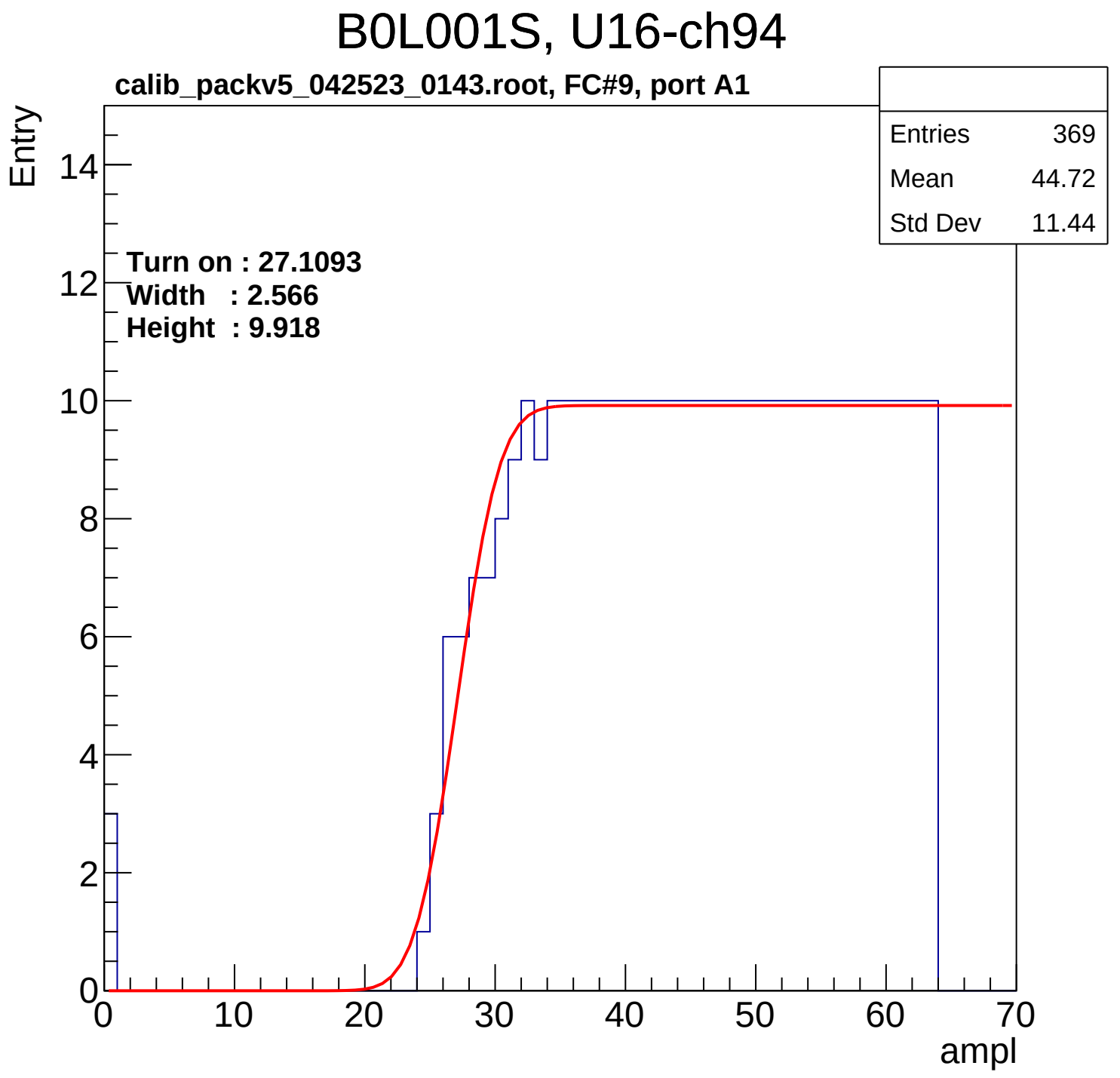
B0L001S, U16-ch94
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.72
Std Dev 11.44
Turn on : 27.1093
Width : 2.566
Height : 9.918
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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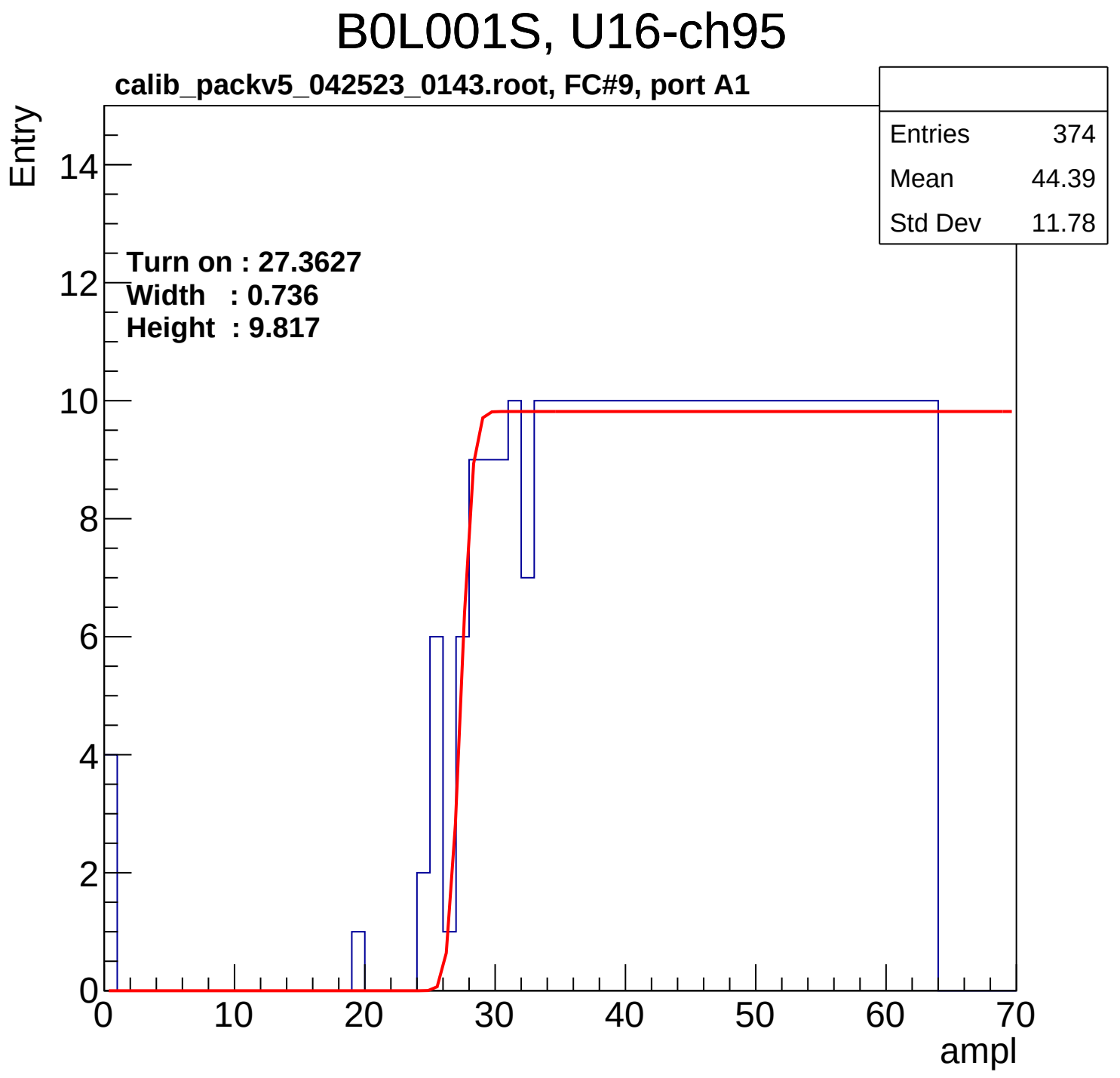
B0L001S, U16-ch95
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.39
Std Dev 11.78
Turn on : 27.3627
Width : 0.736
Height : 9.817
Entry
ampl
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2
4
6
8
10
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0
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60
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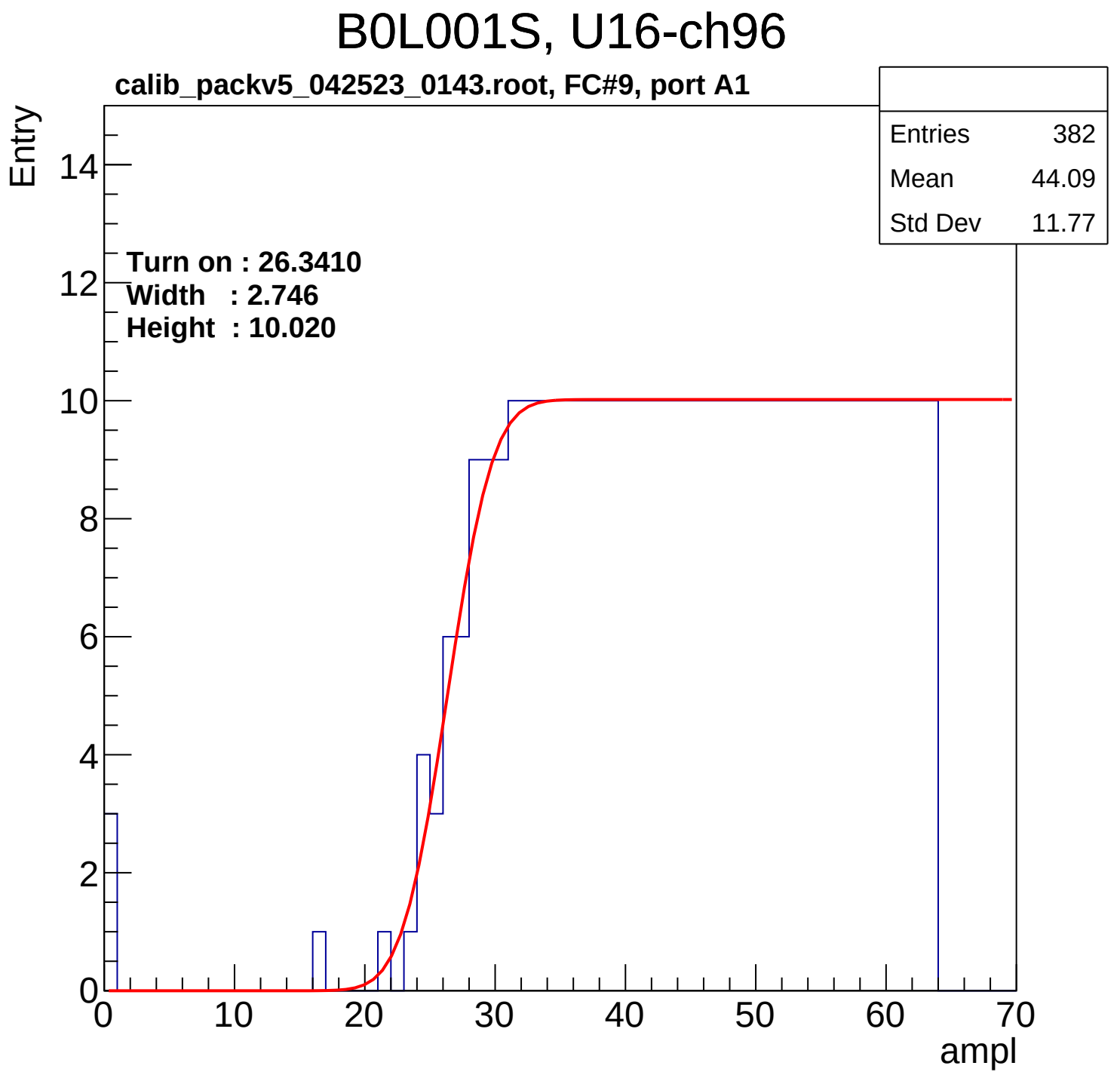
B0L001S, U16-ch96
calib_packv5_042523_0143.root, FC#9, port A1
Entries 382
Mean 44.09
Std Dev 11.77
Turn on : 26.3410
Width : 2.746
Height : 10.020
Entry
ampl
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2
4
6
8
10
12
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60
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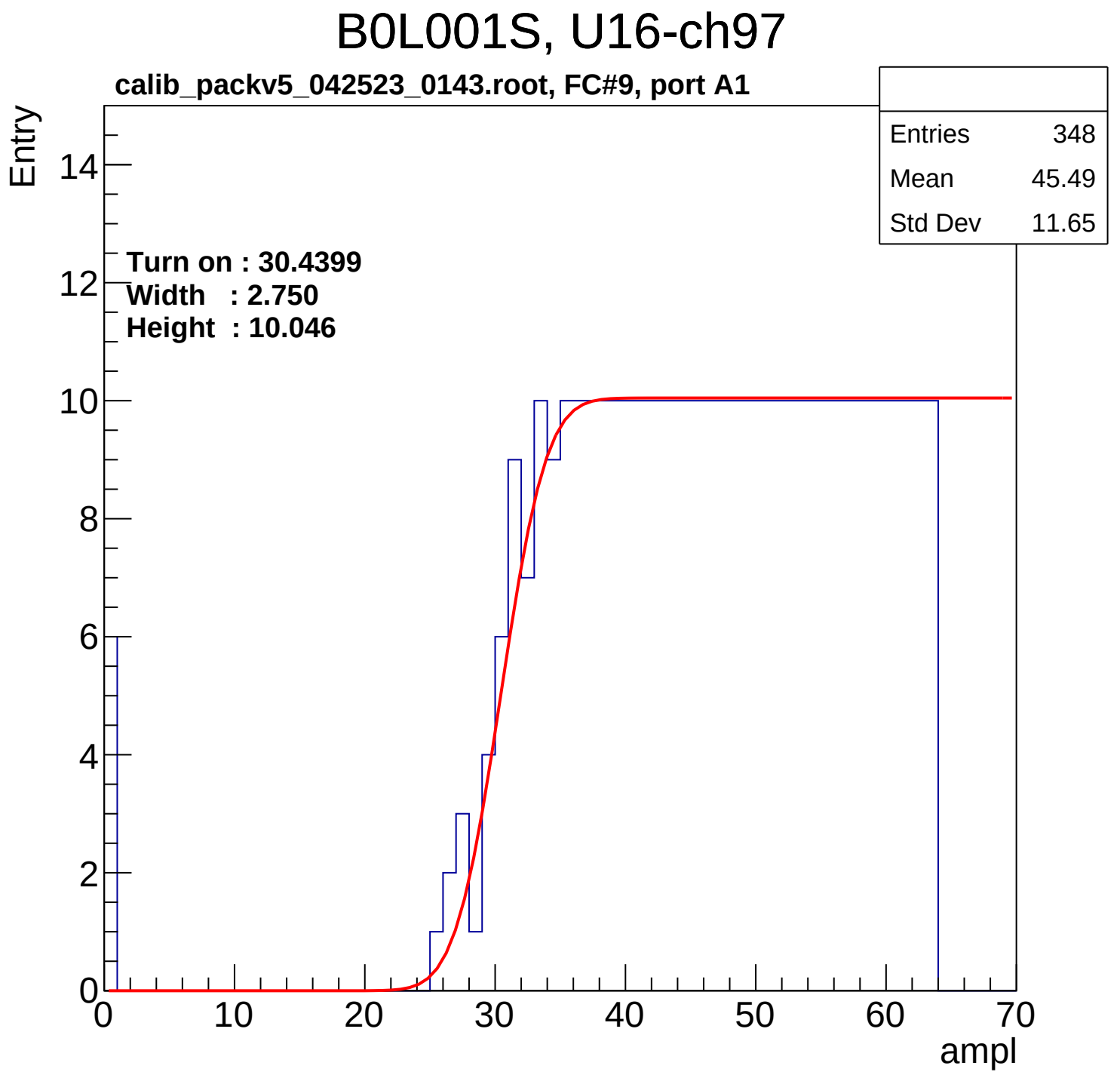
B0L001S, U16-ch97
calib_packv5_042523_0143.root, FC#9, port A1
Entries 348
Mean 45.49
Std Dev 11.65
Turn on : 30.4399
Width : 2.750
Height : 10.046
Entry
ampl
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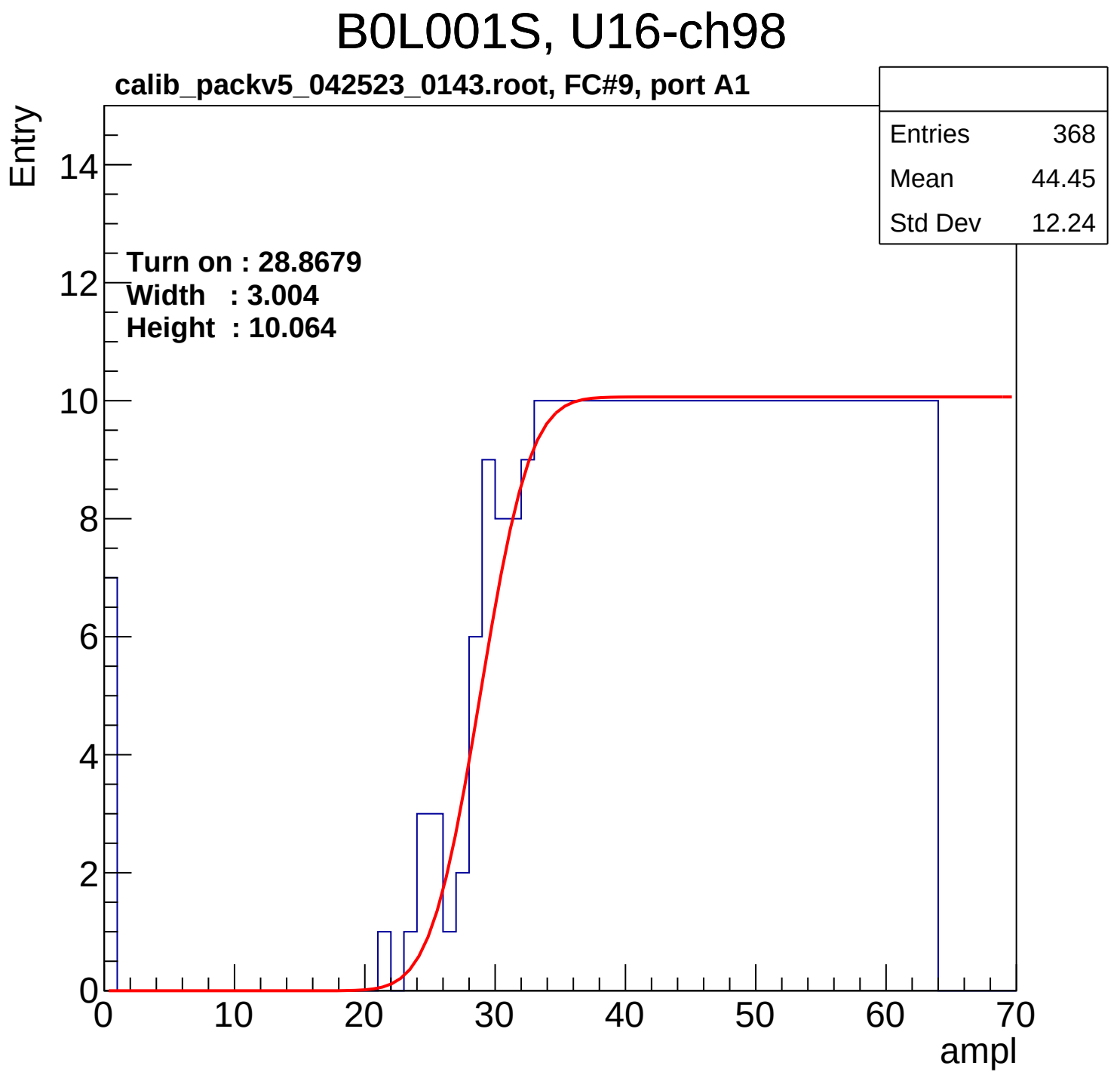
B0L001S, U16-ch98
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.45
Std Dev 12.24
Turn on : 28.8679
Width : 3.004
Height : 10.064
Entry
ampl
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6
8
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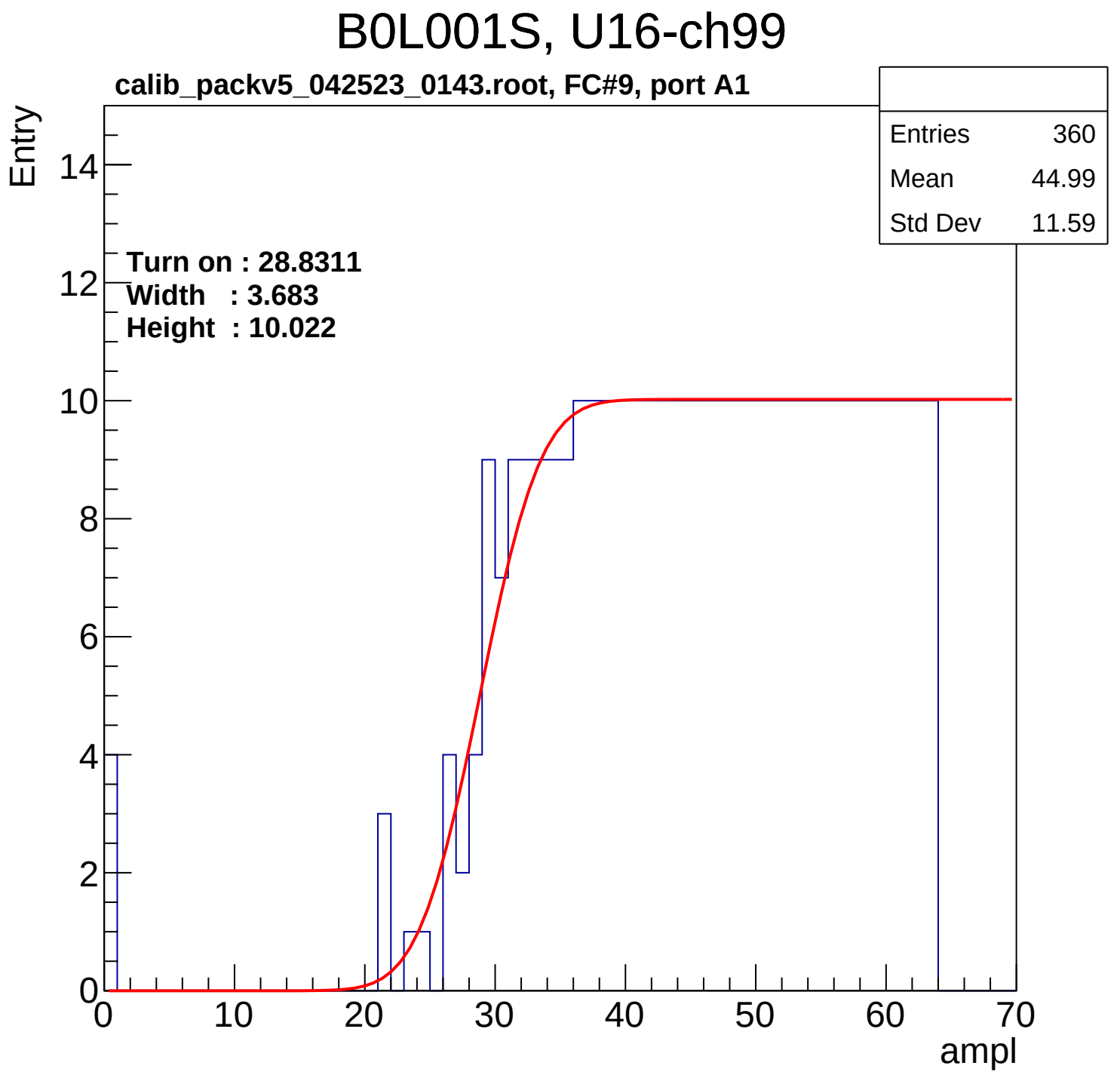
B0L001S, U16-ch99
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 44.99
Std Dev 11.59
Turn on : 28.8311
Width : 3.683
Height : 10.022
Entry
ampl
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6
8
10
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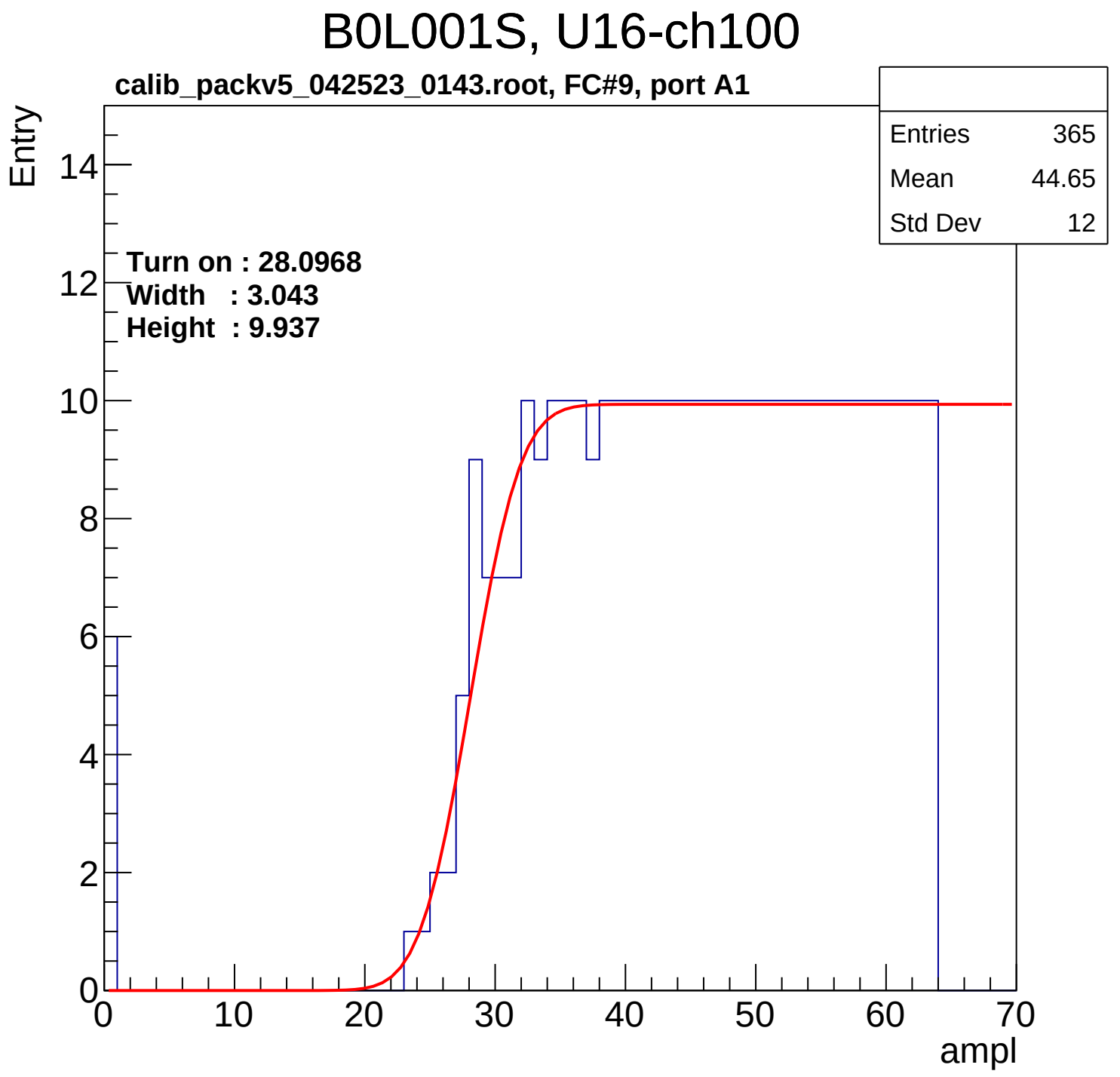
B0L001S, U16-ch100
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.65
Std Dev 12
Turn on : 28.0968
Width : 3.043
Height : 9.937
Entry
ampl
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6
8
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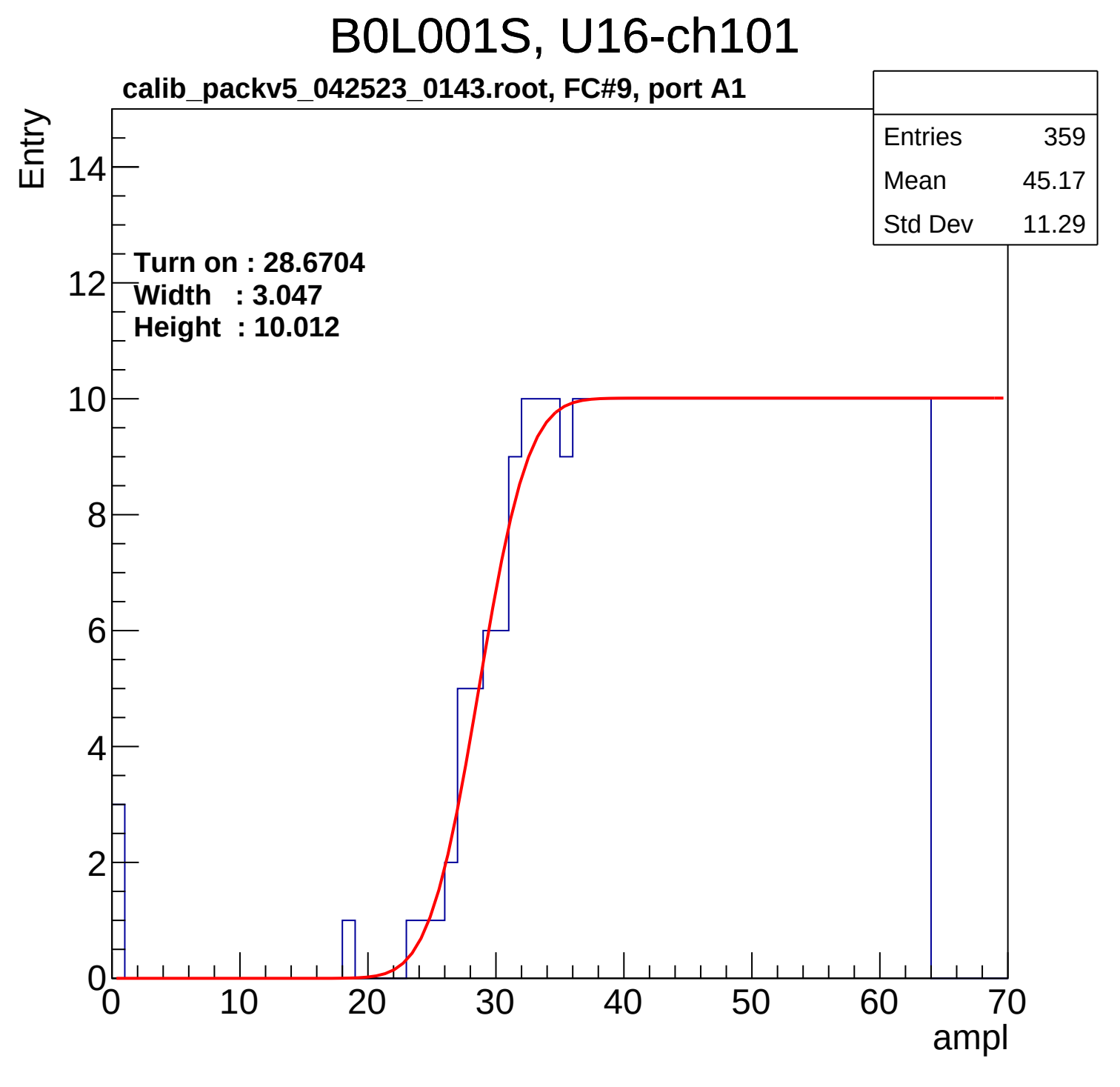
B0L001S, U16-ch101
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.17
Std Dev 11.29
Turn on : 28.6704
Width : 3.047
Height : 10.012
Entry
ampl
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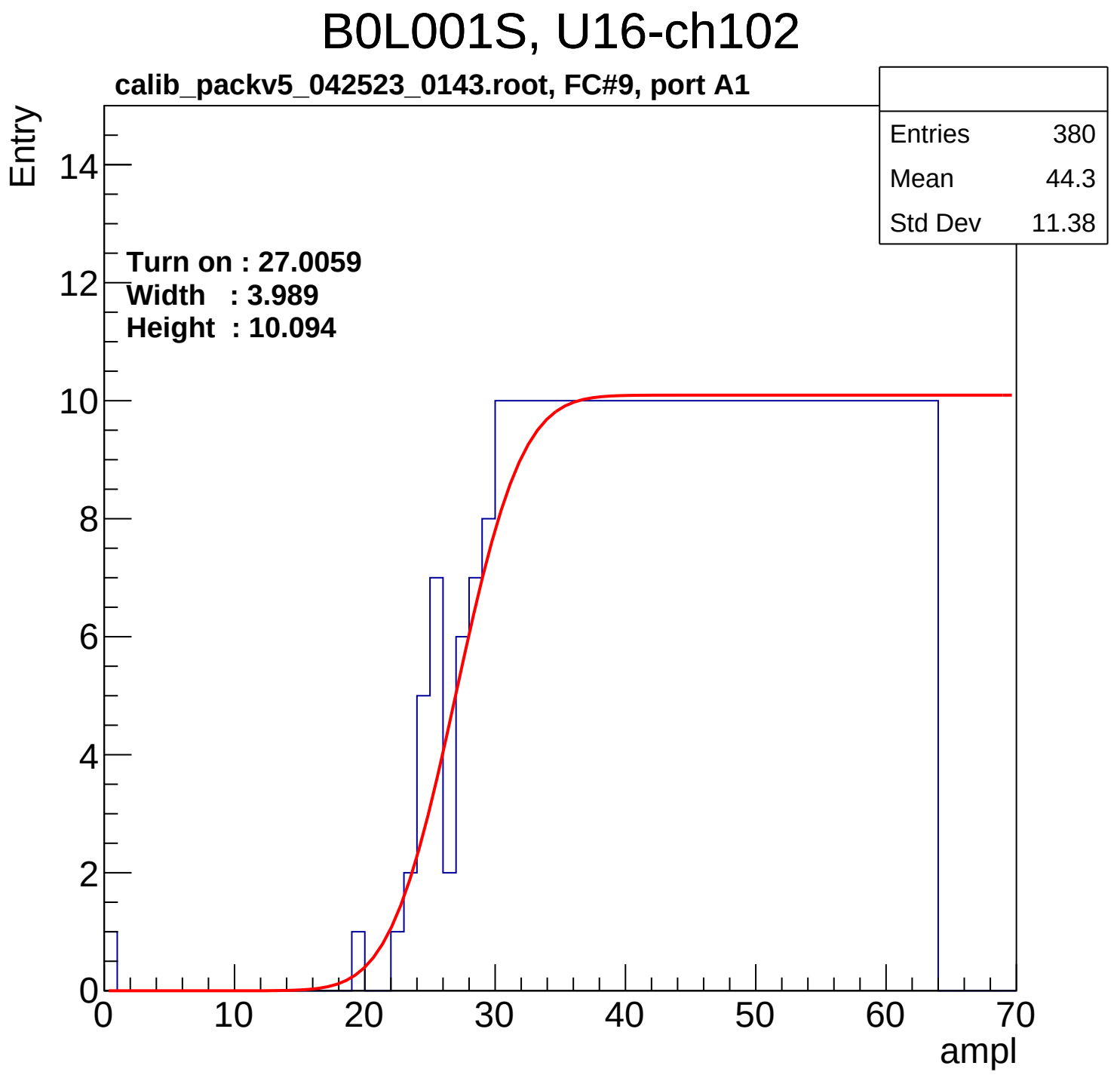
B0L001S, U16-ch102
calib_packv5_042523_0143.root, FC#9, port A1
Entries 380
Mean 44.3
Std Dev 11.38
Turn on : 27.0059
Width : 3.989
Height : 10.094
Entry
ampl
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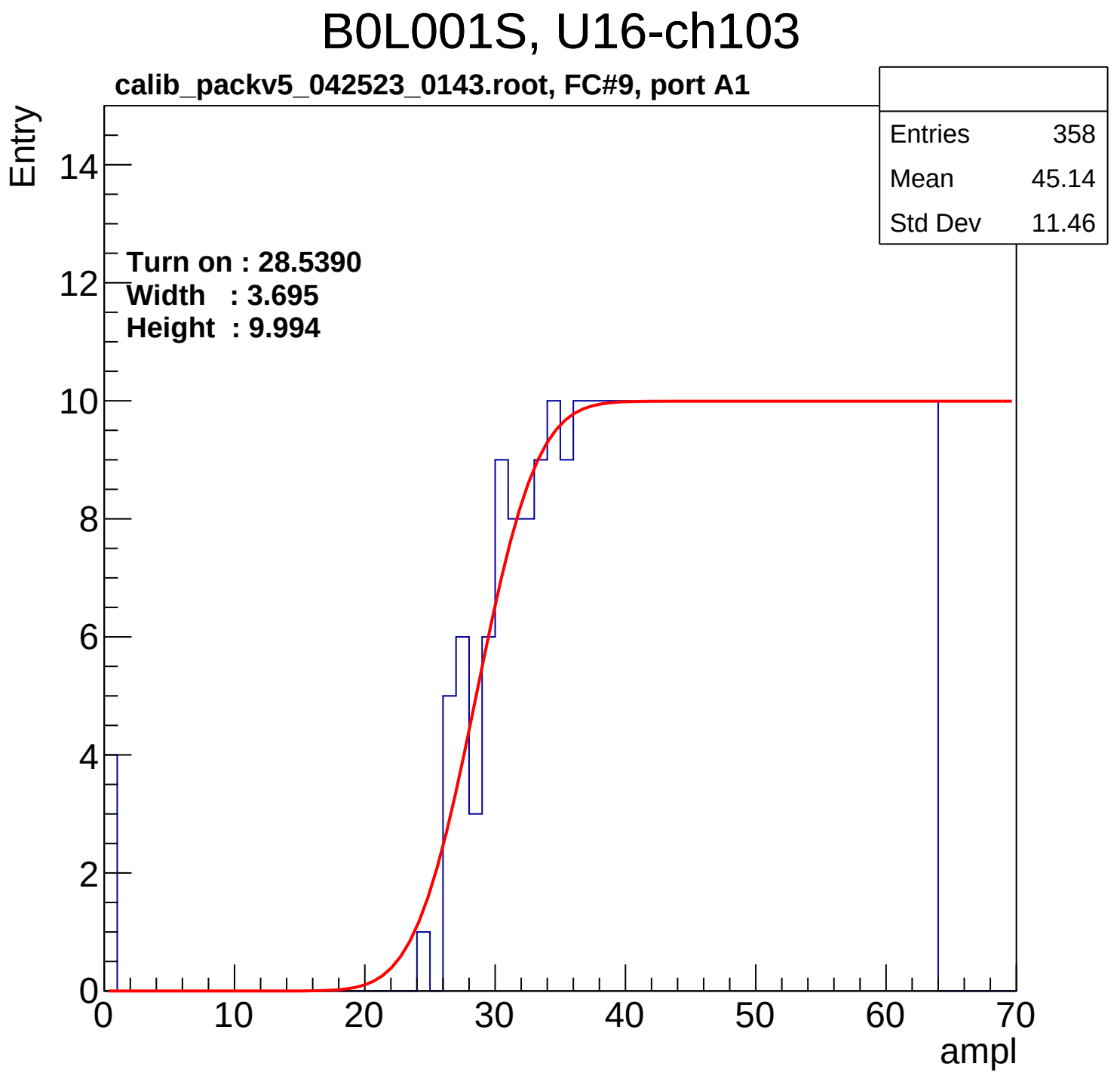
B0L001S, U16-ch103
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.14
Std Dev 11.46
Turn on : 28.5390
Width : 3.695
Height : 9.994
Entry
ampl
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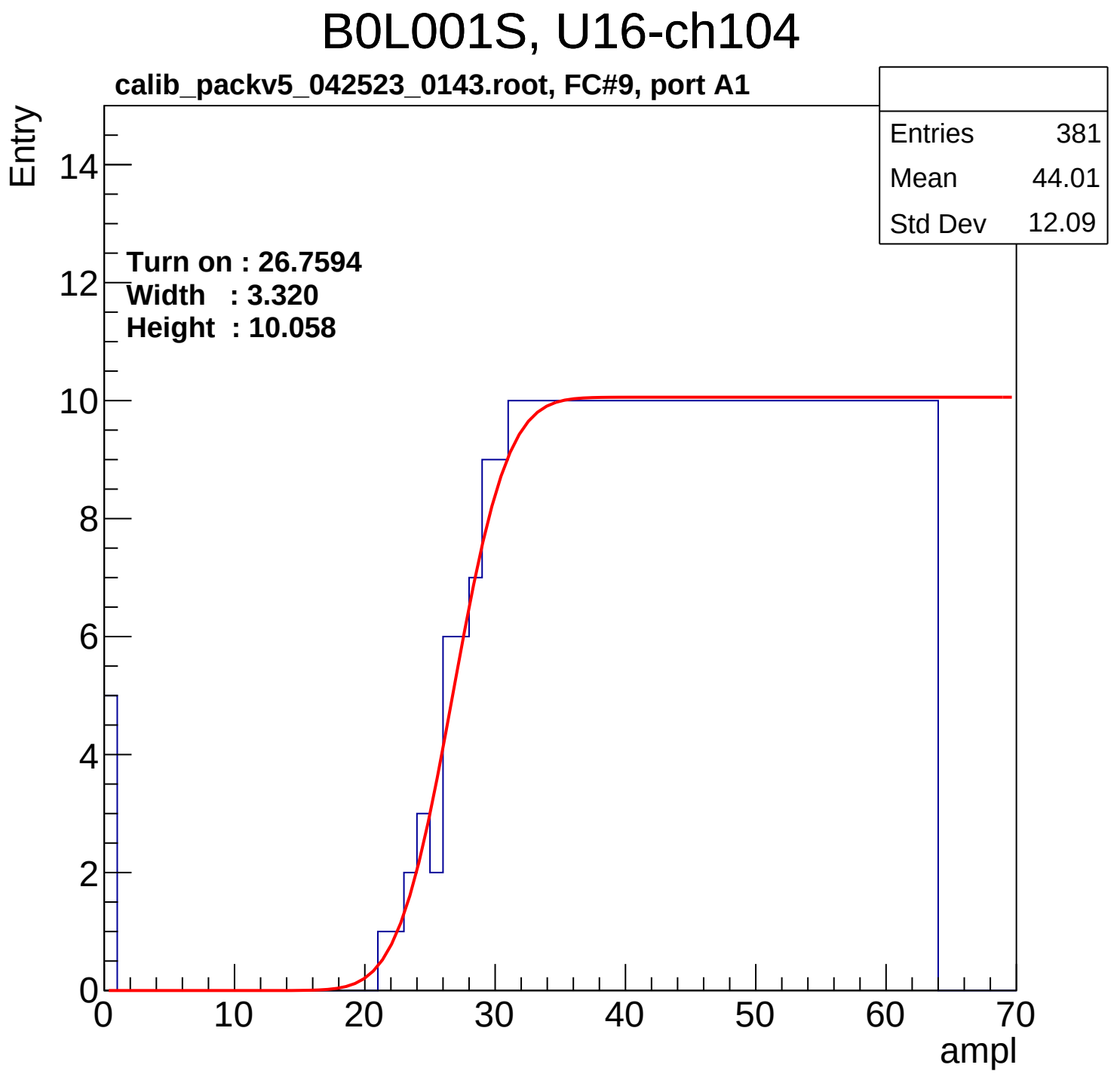
B0L001S, U16-ch104
calib_packv5_042523_0143.root, FC#9, port A1
Entries 381
Mean 44.01
Std Dev 12.09
Turn on : 26.7594
Width : 3.320
Height : 10.058
Entry
ampl
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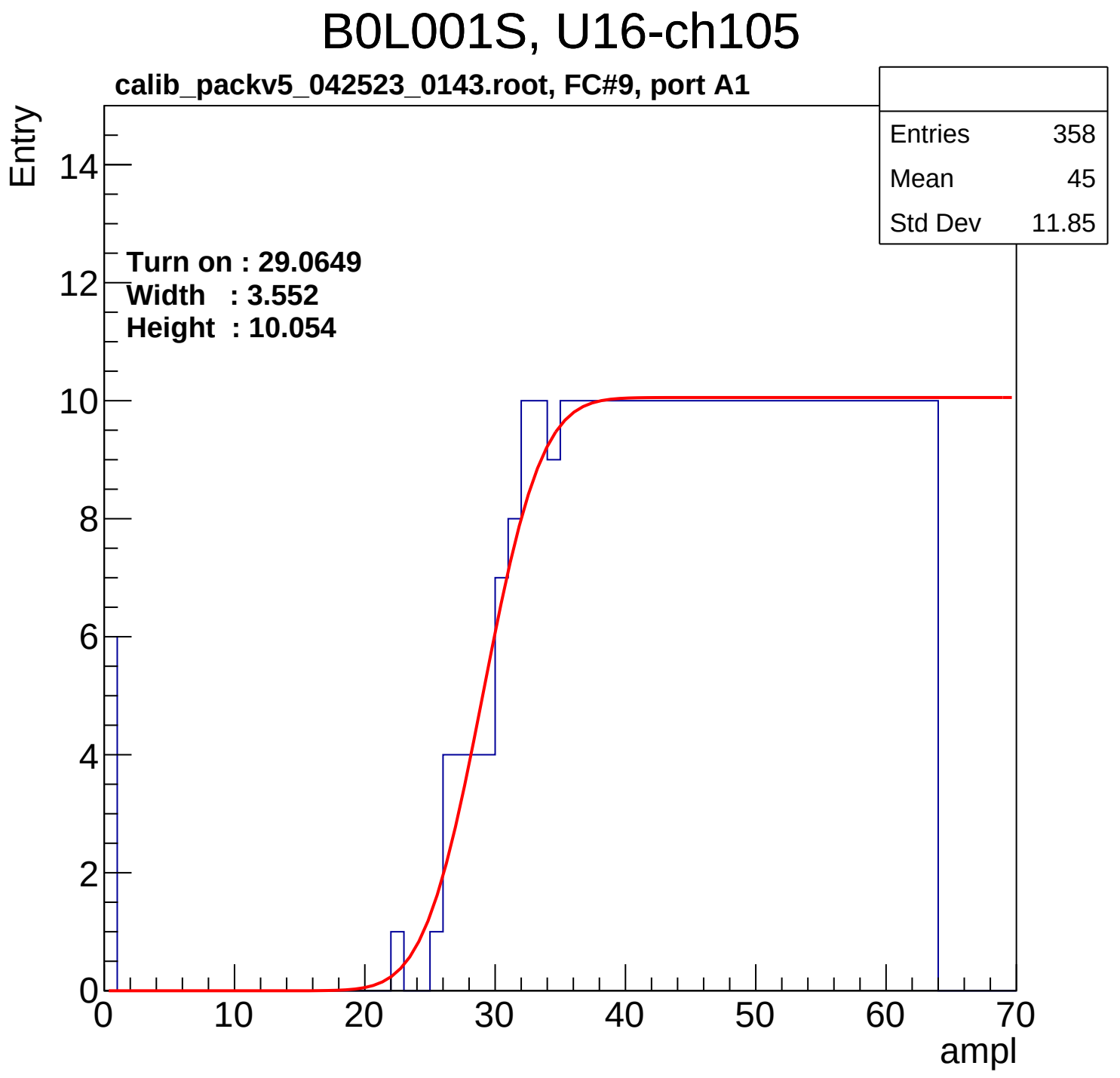
B0L001S, U16-ch105
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45
Std Dev 11.85
Turn on : 29.0649
Width : 3.552
Height : 10.054
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ampl
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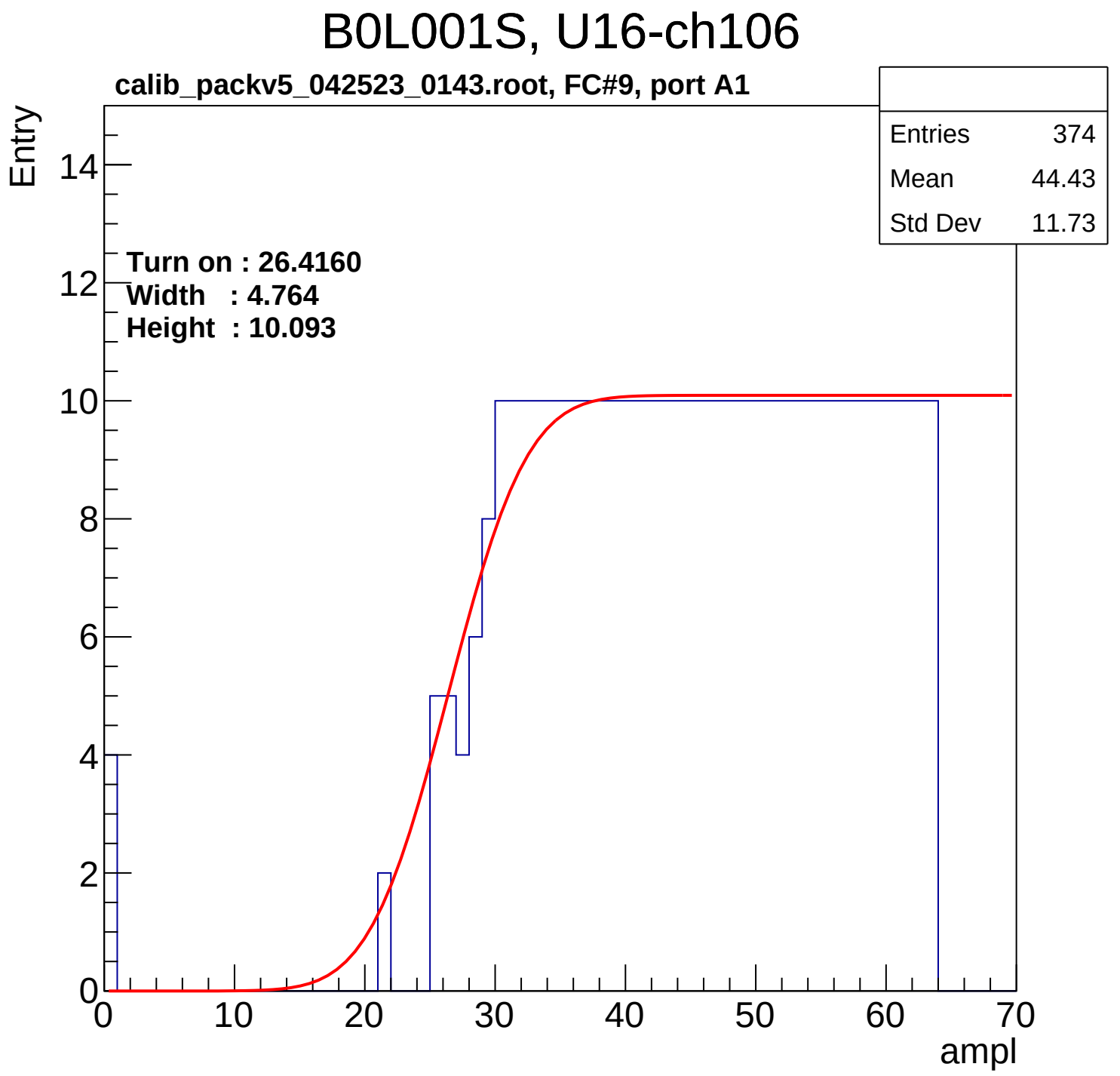
B0L001S, U16-ch106
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.43
Std Dev 11.73
Turn on : 26.4160
Width : 4.764
Height : 10.093
Entry
ampl
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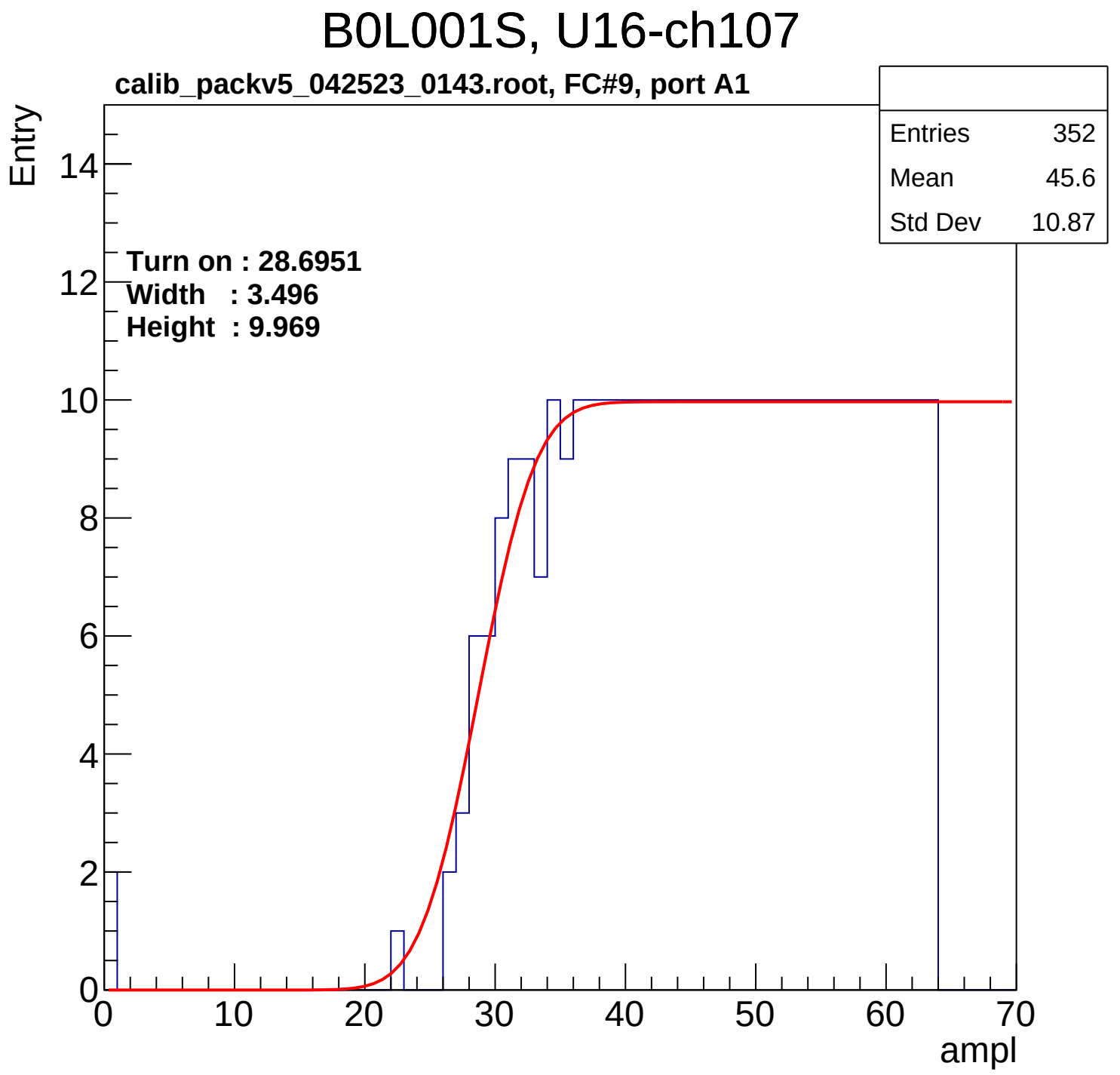
B0L001S, U16-ch107
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.6
Std Dev 10.87
Turn on : 28.6951
Width : 3.496
Height : 9.969
Entry
ampl
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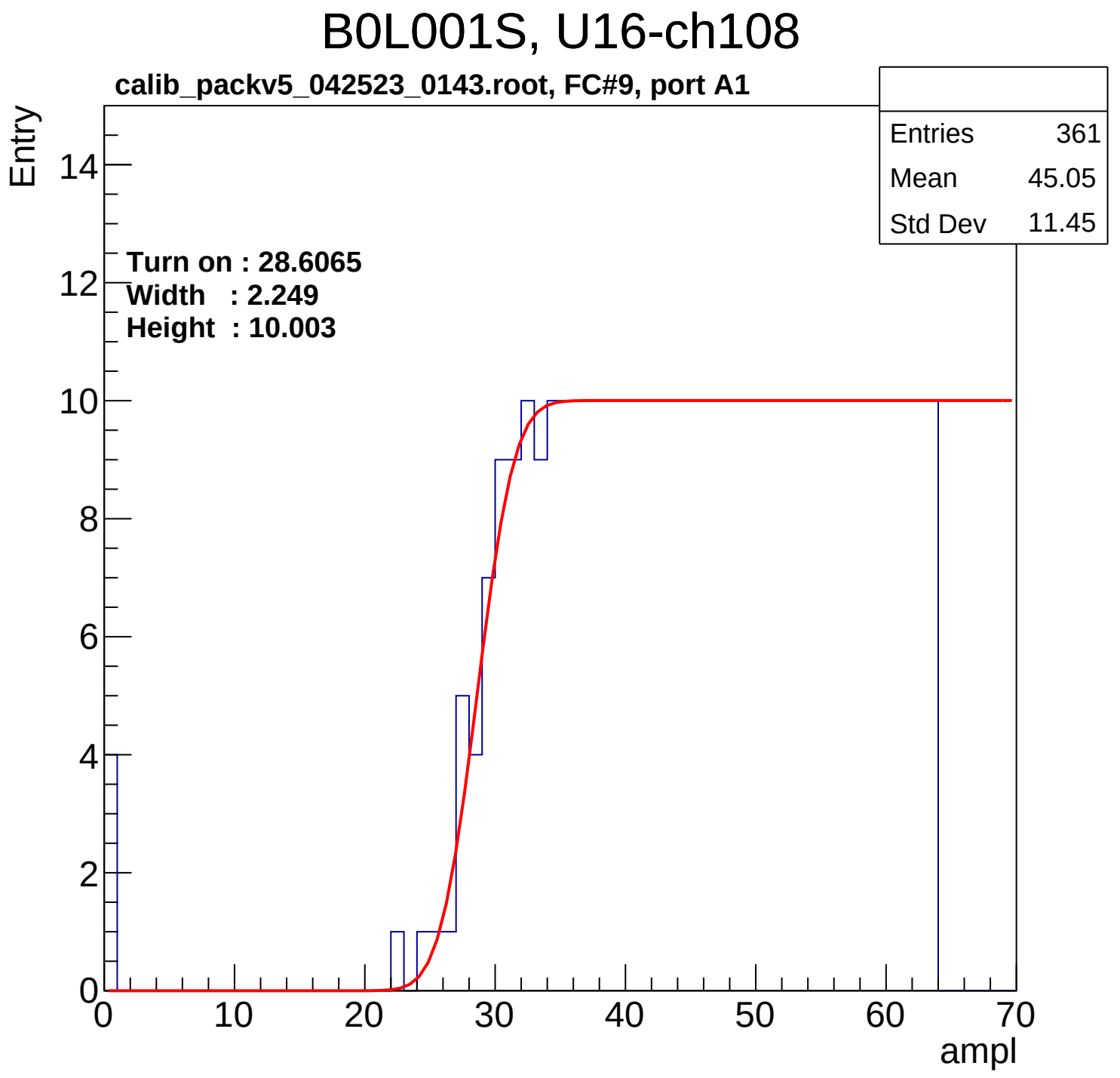
B0L001S, U16-ch108
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.05
Std Dev 11.45
Turn on : 28.6065
Width : 2.249
Height : 10.003
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ampl
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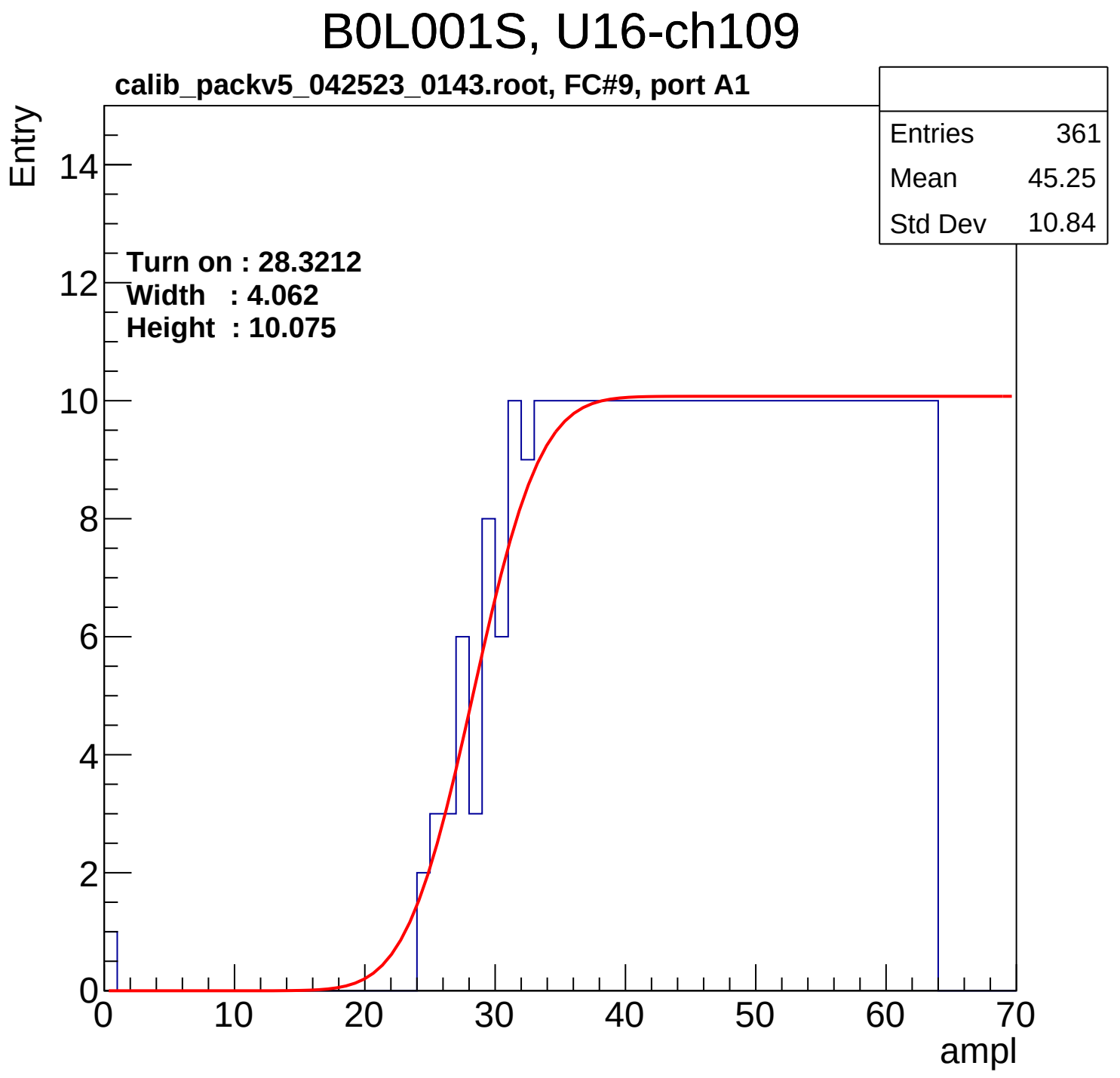
B0L001S, U16-ch109
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.25
Std Dev 10.84
Turn on : 28.3212
Width : 4.062
Height : 10.075
Entry
ampl
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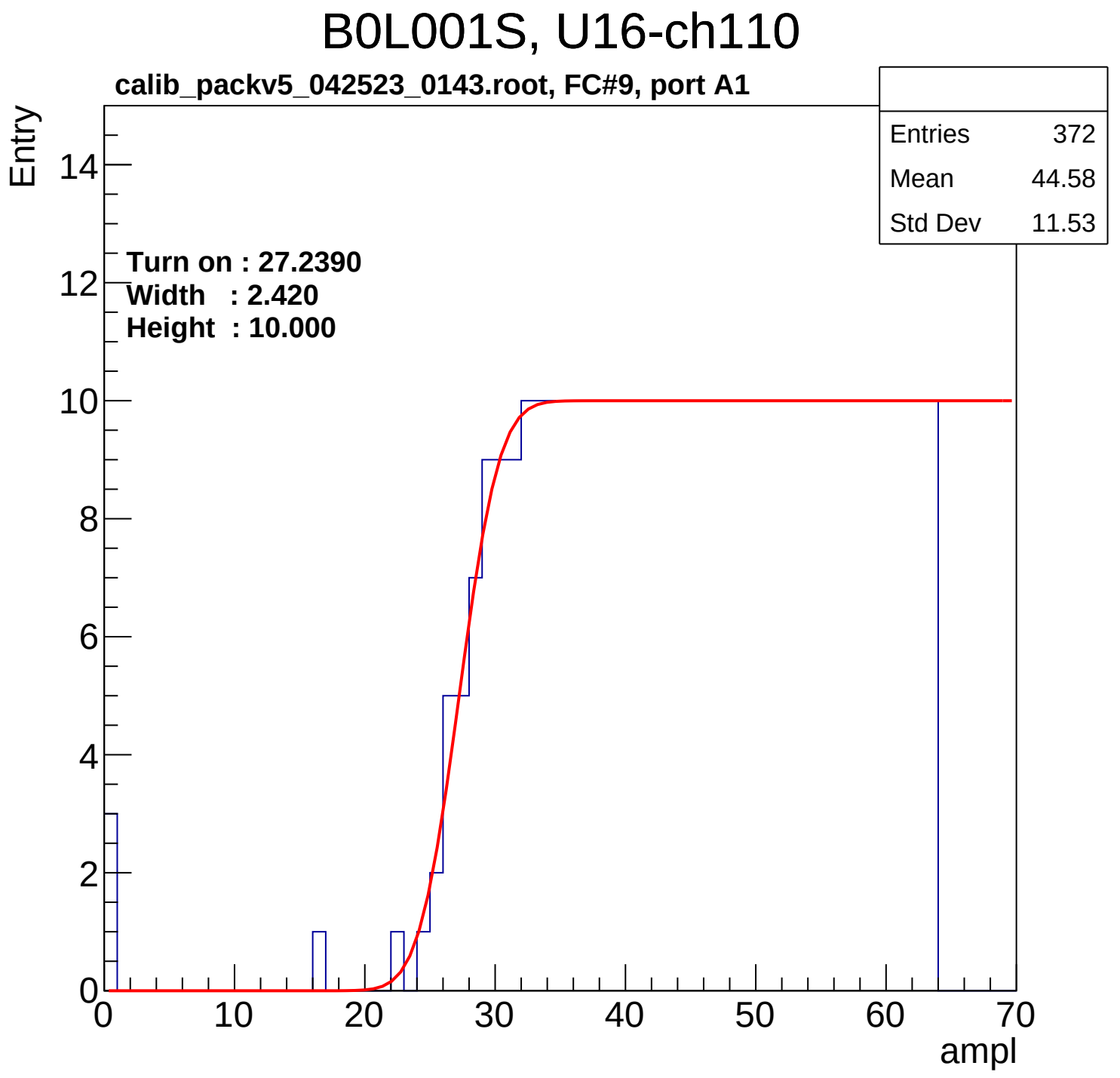
B0L001S, U16-ch110
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.58
Std Dev 11.53
Turn on : 27.2390
Width : 2.420
Height : 10.000
Entry
ampl
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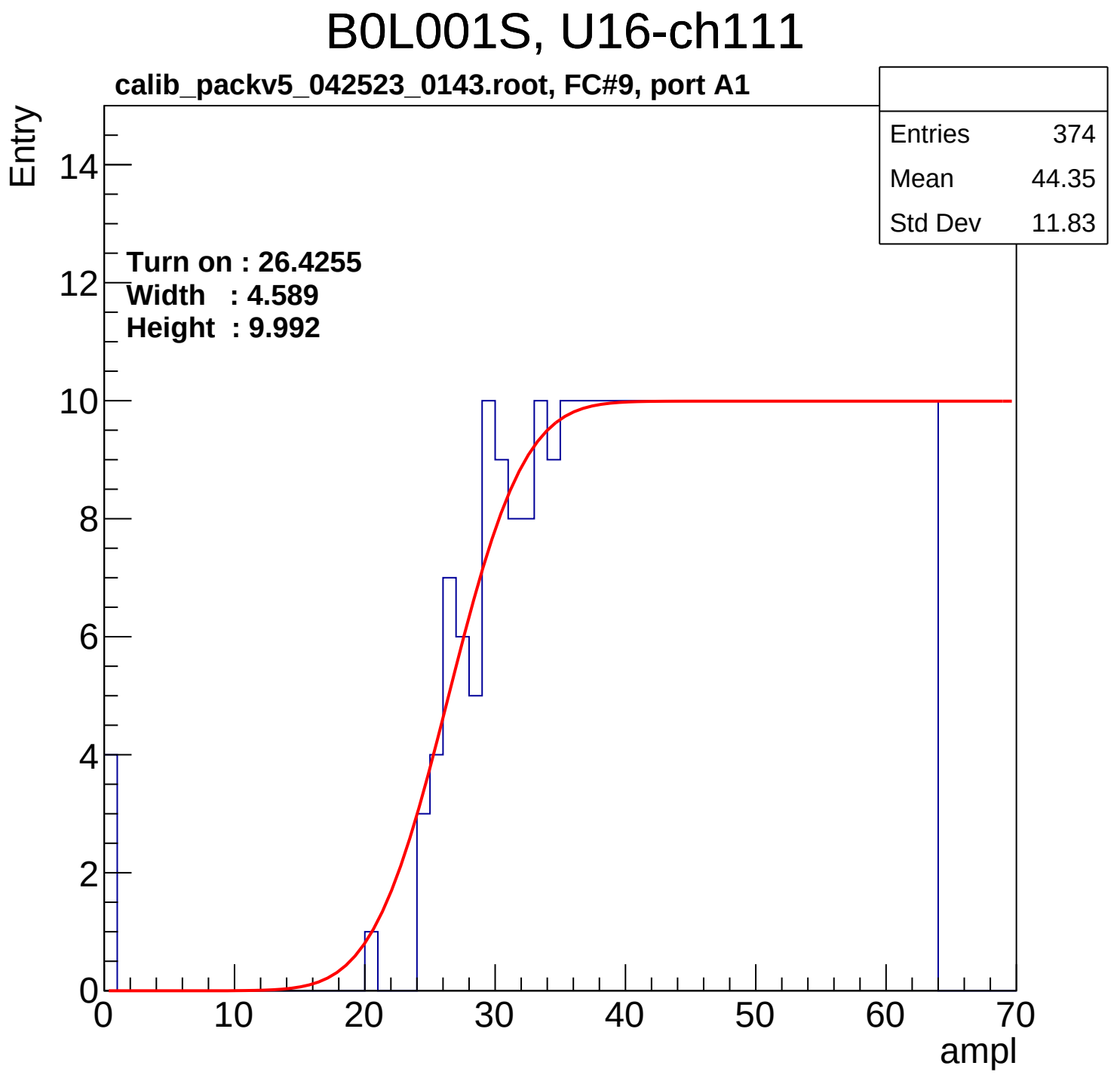
B0L001S, U16-ch111
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.35
Std Dev 11.83
Turn on : 26.4255
Width : 4.589
Height : 9.992
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ampl
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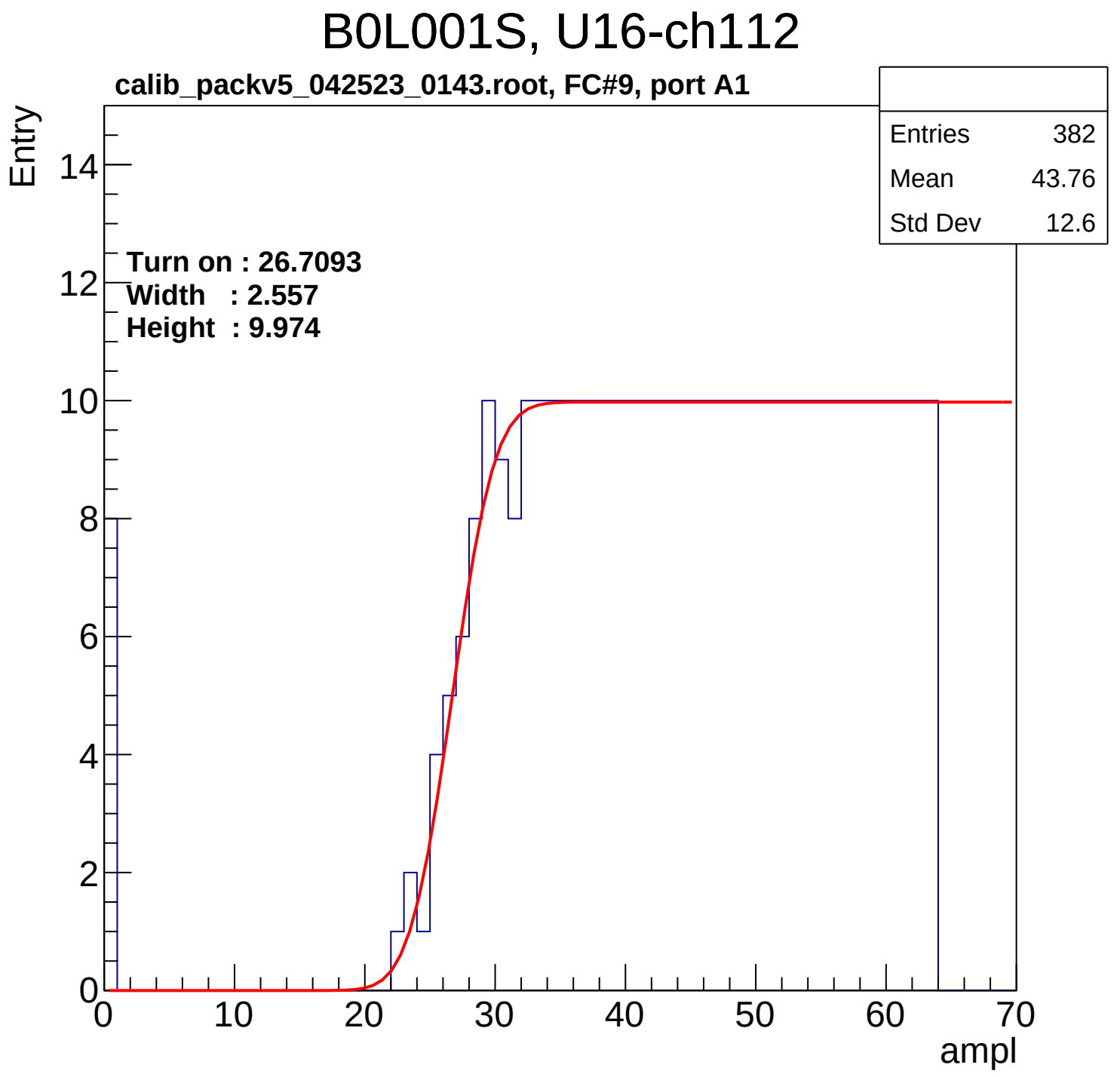
B0L001S, U16-ch112
calib_packv5_042523_0143.root, FC#9, port A1
Entries 382
Mean 43.76
Std Dev 12.6
Turn on : 26.7093
Width : 2.557
Height : 9.974
Entry
ampl
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6
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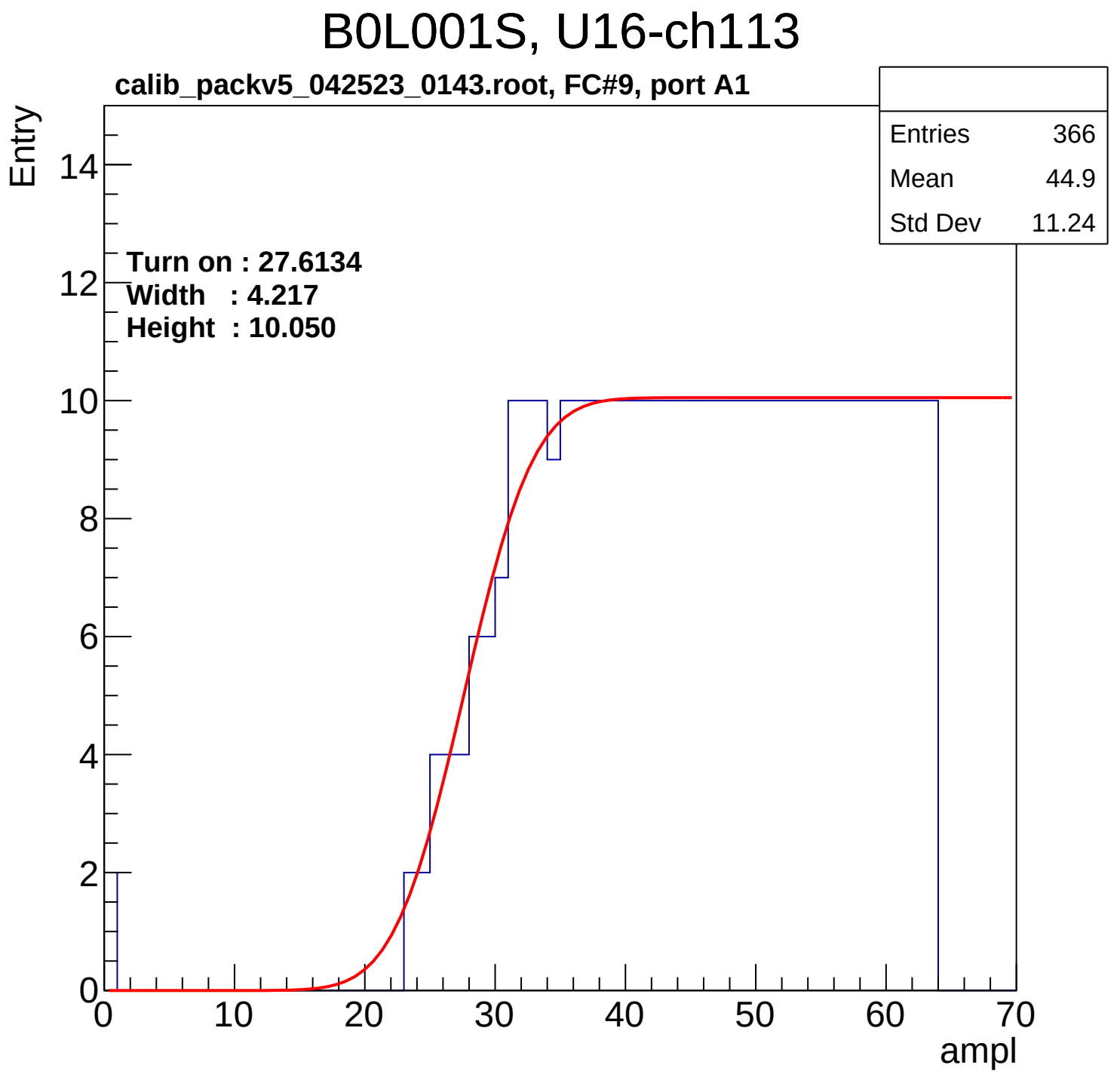
B0L001S, U16-ch113
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.9
Std Dev 11.24
Turn on : 27.6134
Width : 4.217
Height : 10.050
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ampl
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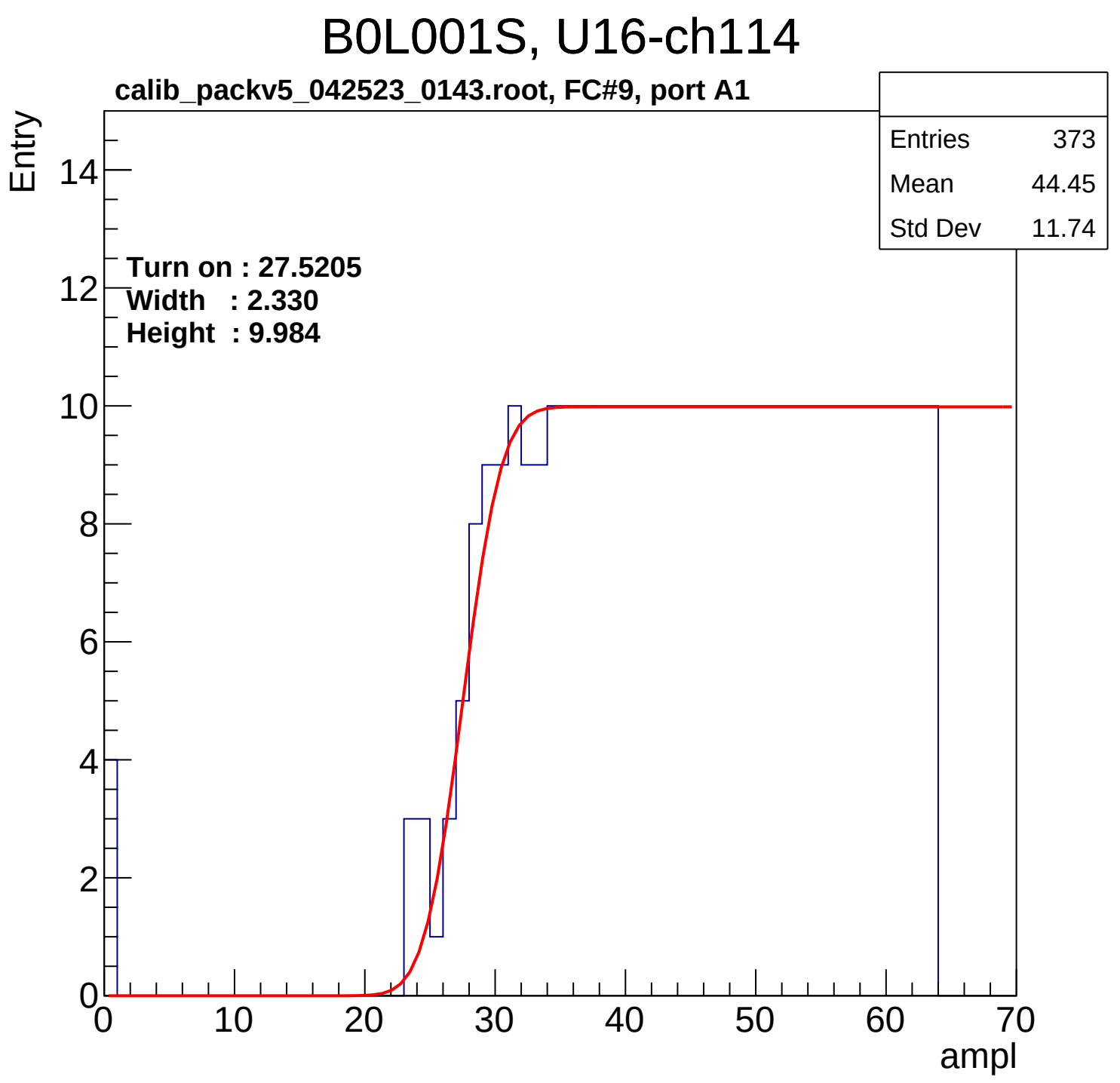
B0L001S, U16-ch114
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.45
Std Dev 11.74
Turn on : 27.5205
Width : 2.330
Height : 9.984
Entry
ampl
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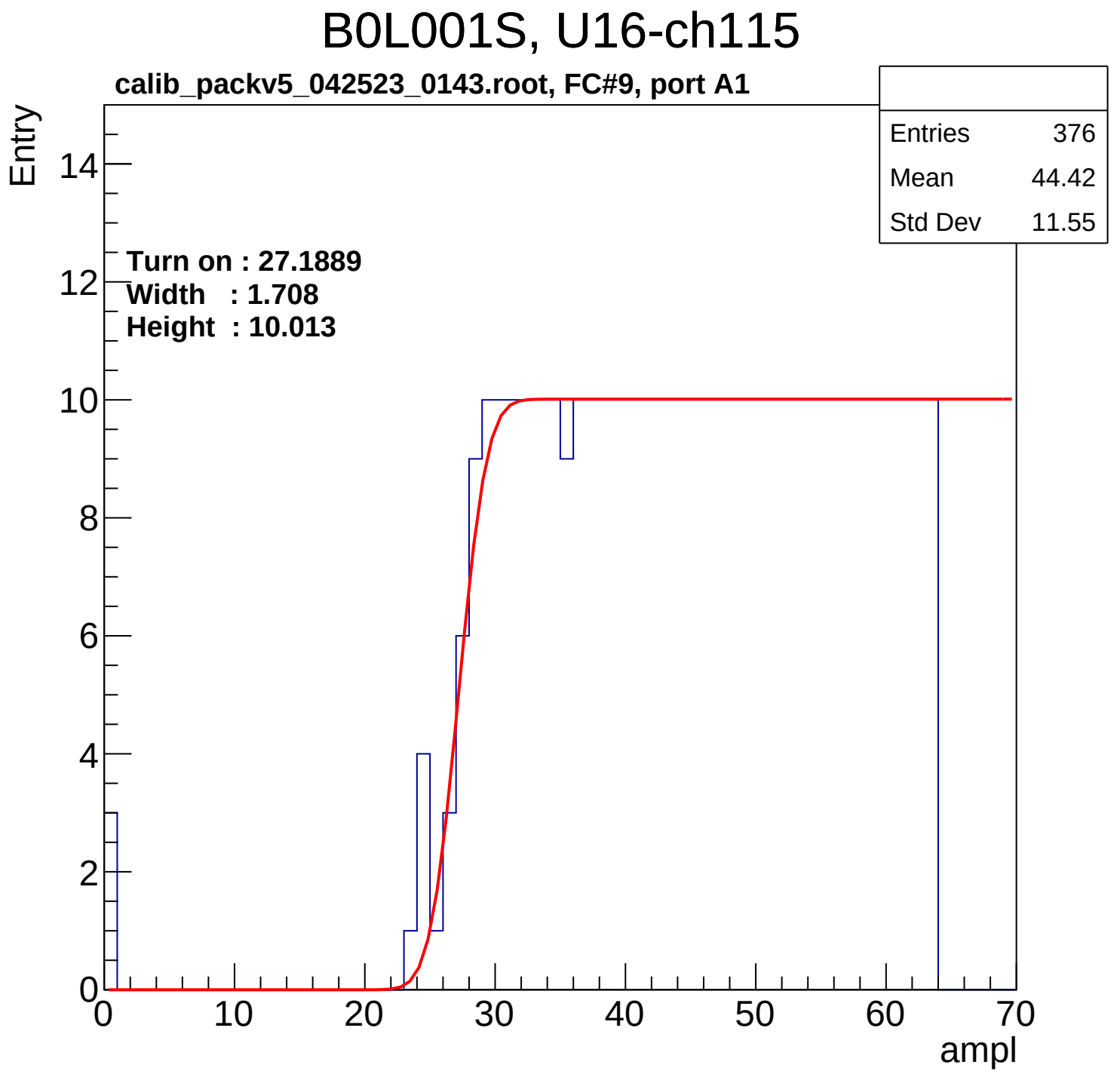
B0L001S, U16-ch115
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.42
Std Dev 11.55
Turn on : 27.1889
Width : 1.708
Height : 10.013
Entry
ampl
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4
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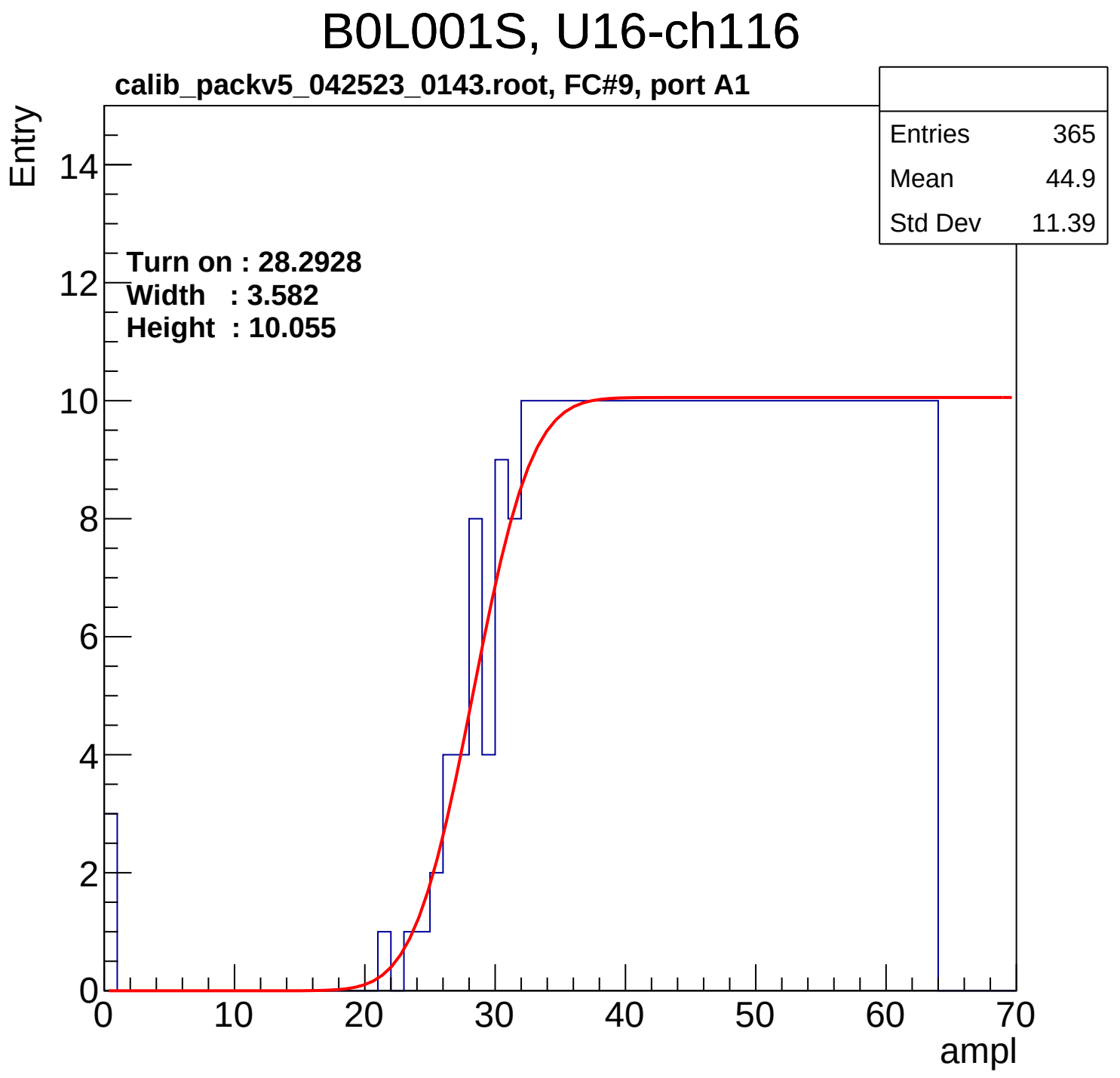
B0L001S, U16-ch116
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.9
Std Dev 11.39
Turn on : 28.2928
Width : 3.582
Height : 10.055
Entry
ampl
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2
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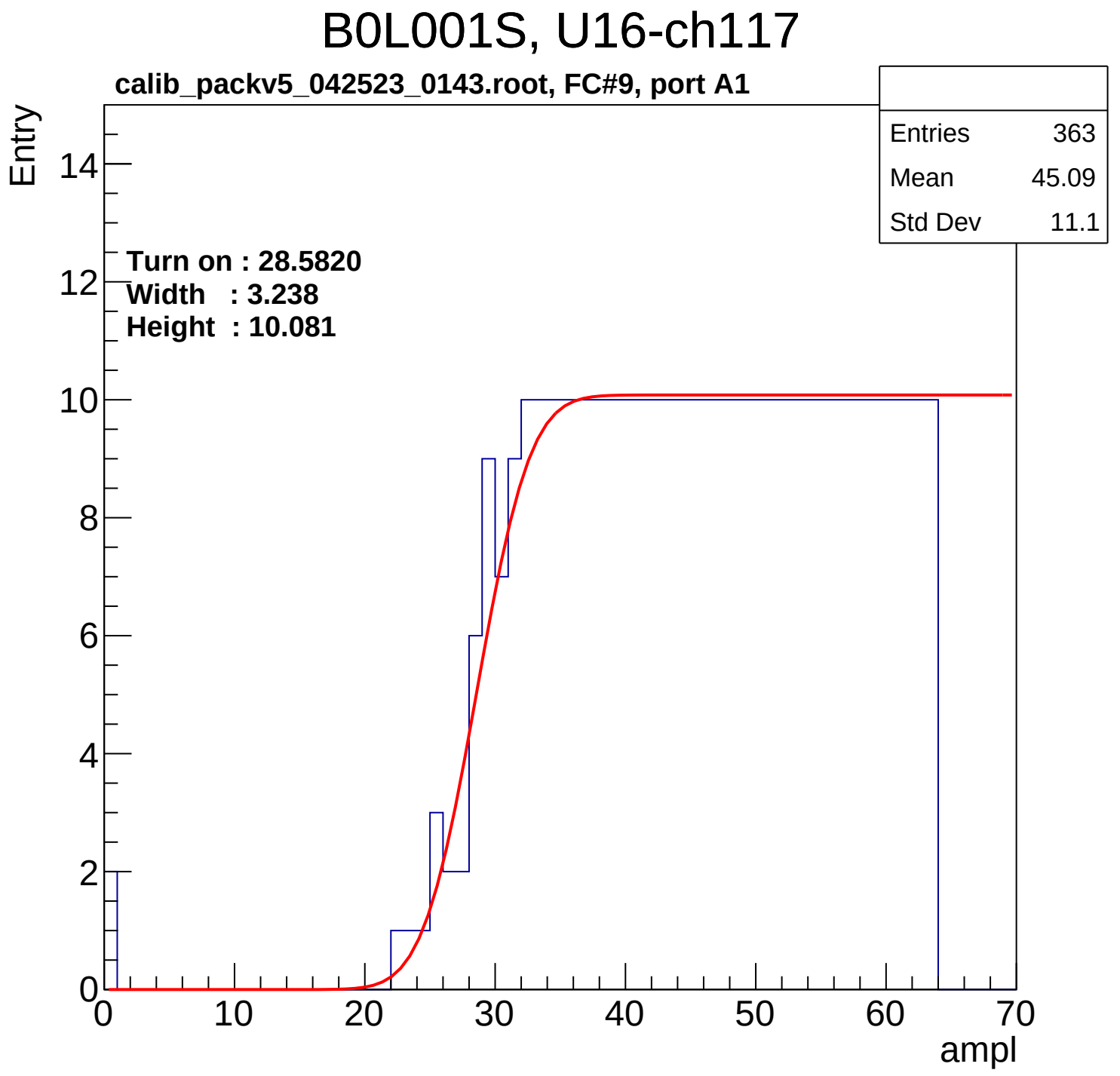
B0L001S, U16-ch117
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.09
Std Dev 11.1
Turn on : 28.5820
Width : 3.238
Height : 10.081
Entry
ampl
0
2
4
6
8
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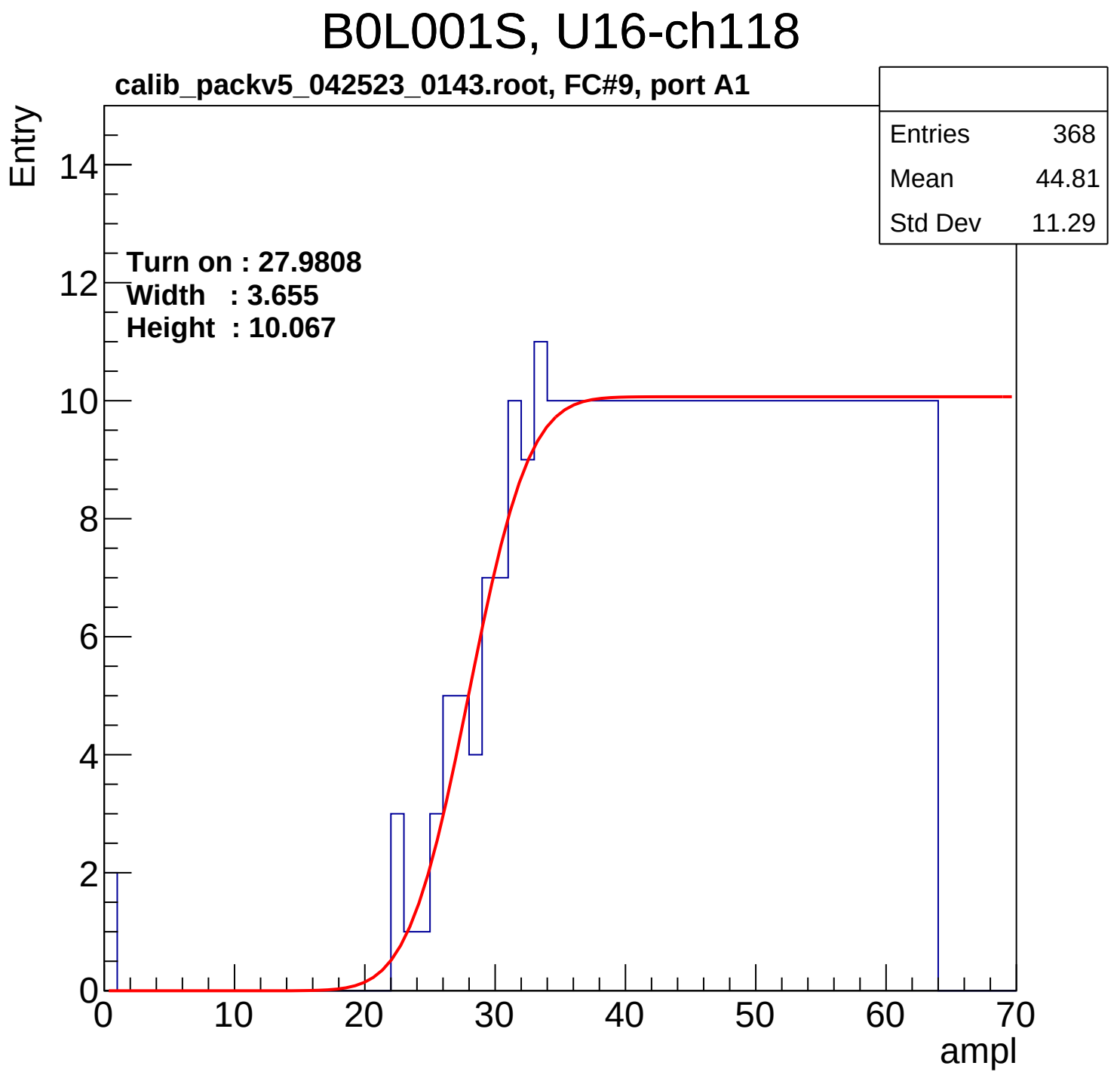
B0L001S, U16-ch118
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.81
Std Dev 11.29
Turn on : 27.9808
Width : 3.655
Height : 10.067
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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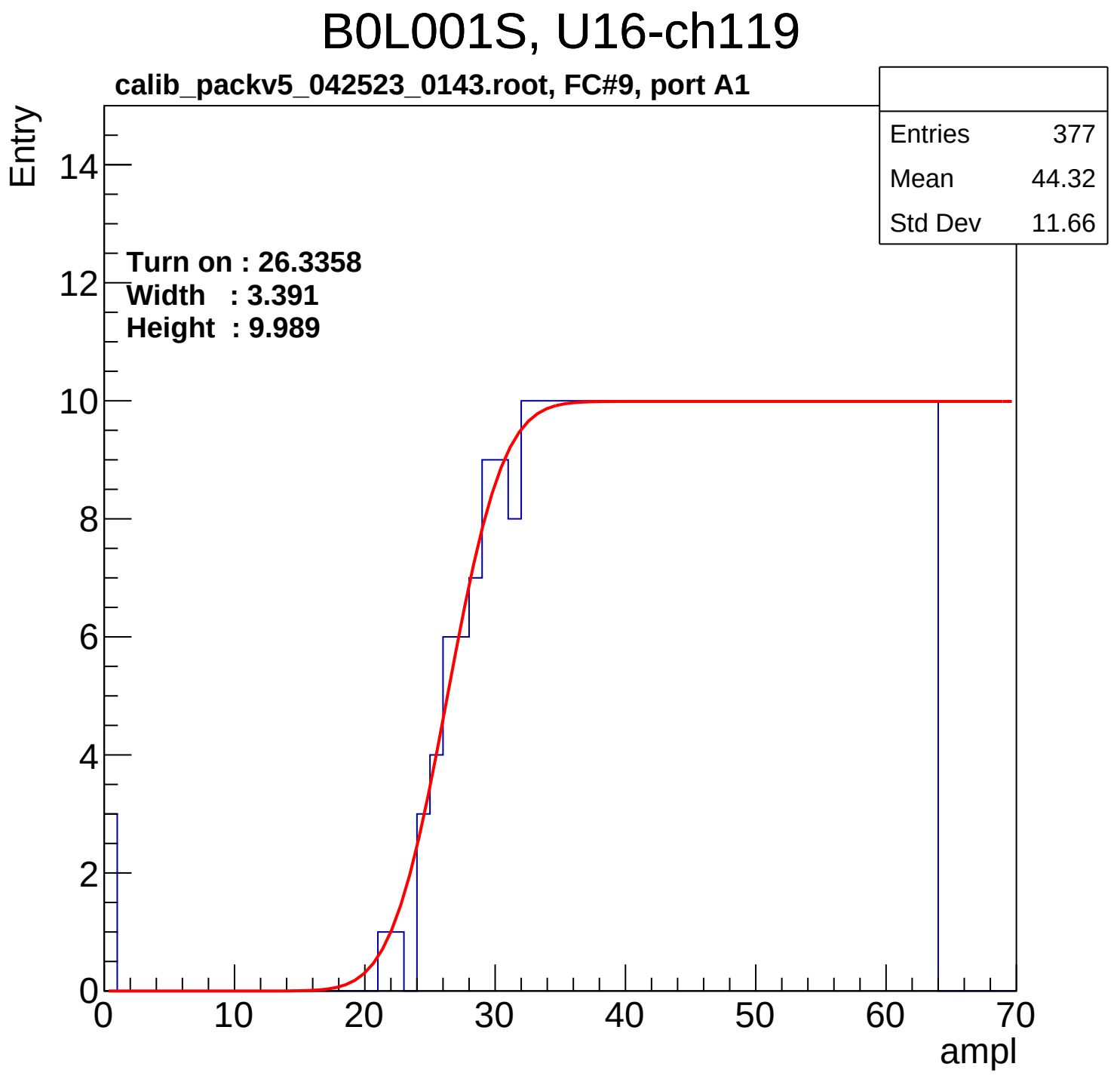
B0L001S, U16-ch119
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.32
Std Dev 11.66
Turn on : 26.3358
Width : 3.391
Height : 9.989
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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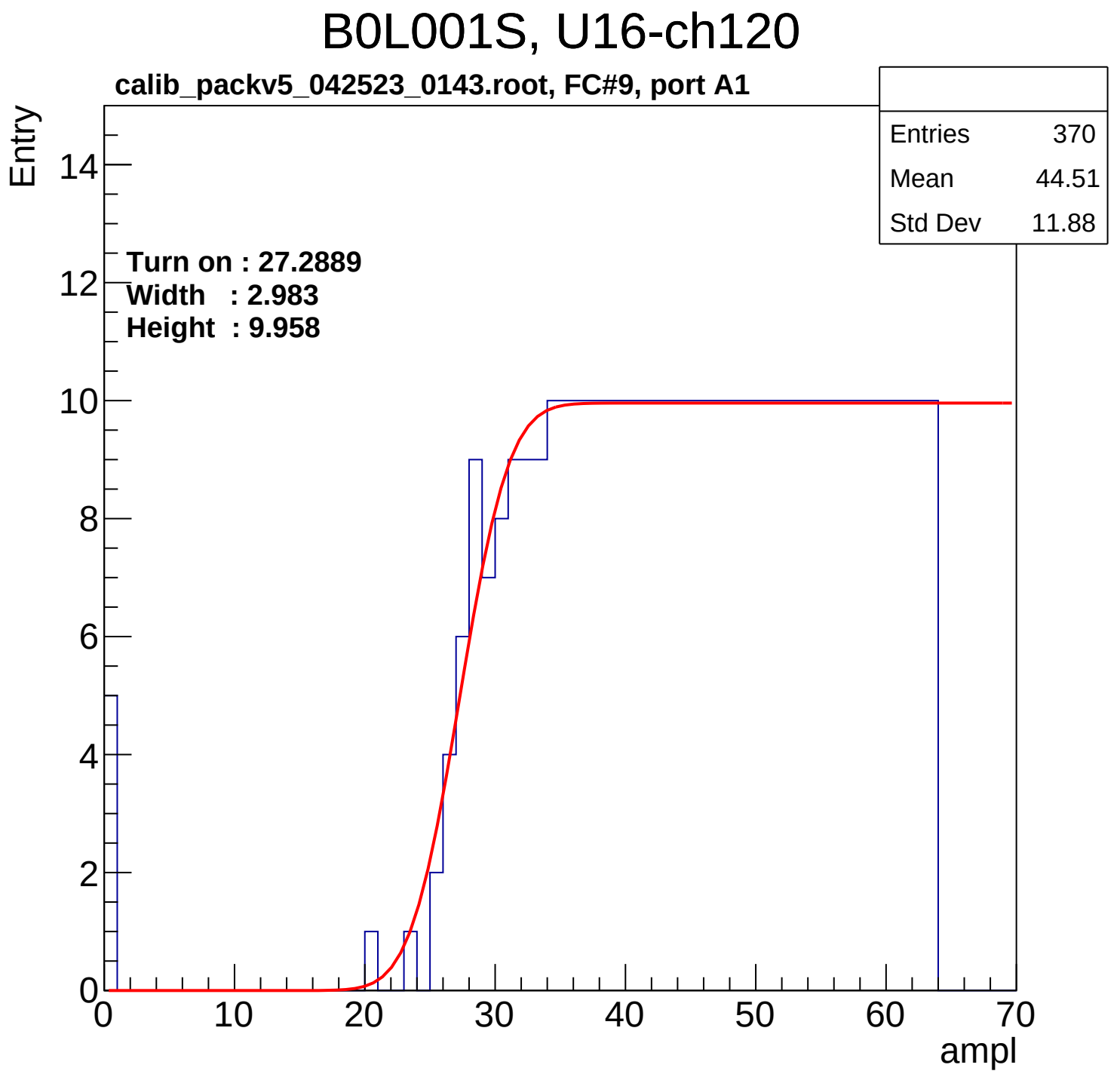
B0L001S, U16-ch120
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.51
Std Dev 11.88
Turn on : 27.2889
Width : 2.983
Height : 9.958
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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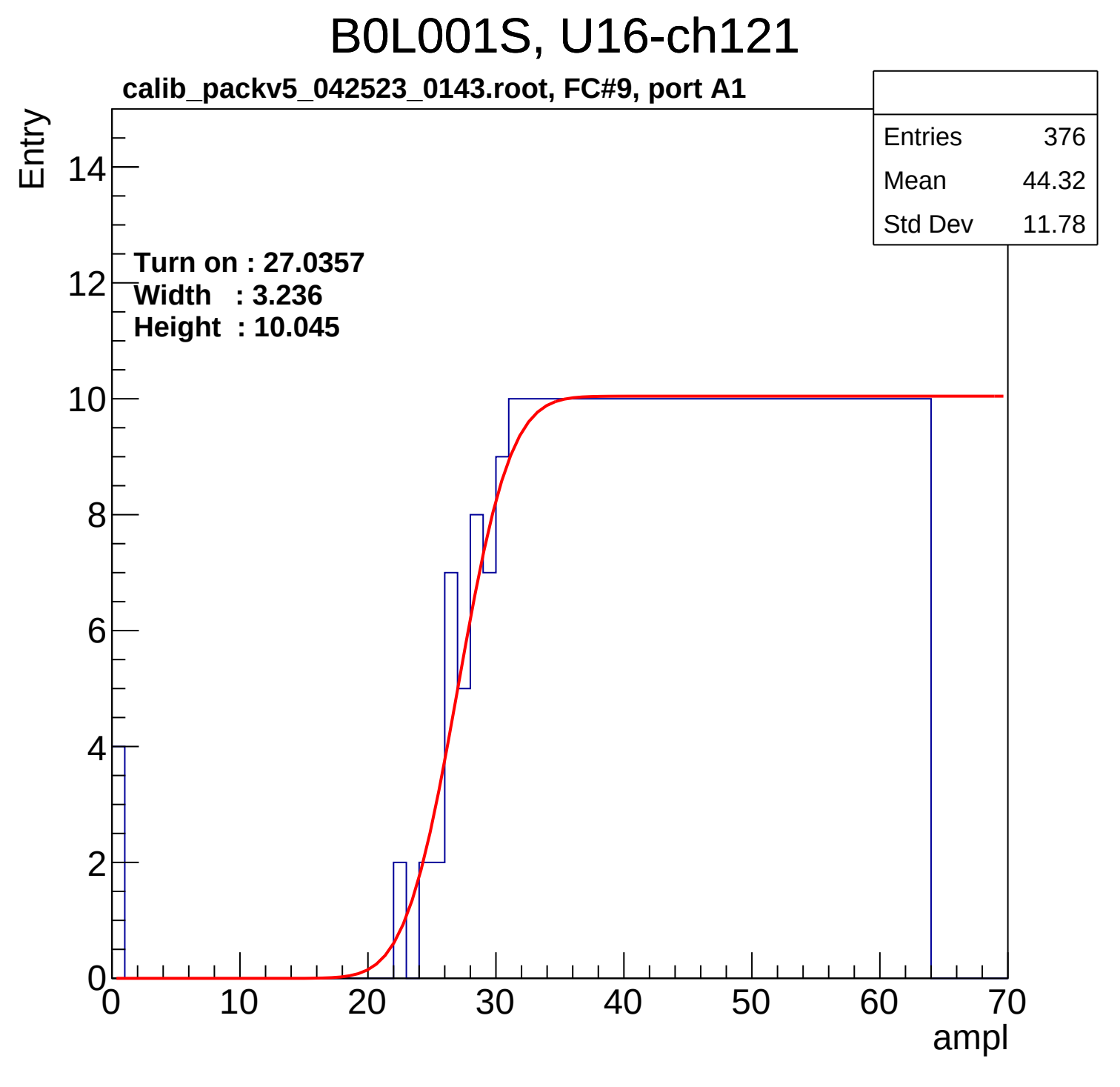
B0L001S, U16-ch121
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.32
Std Dev 11.78
Turn on : 27.0357
Width : 3.236
Height : 10.045
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
50
60
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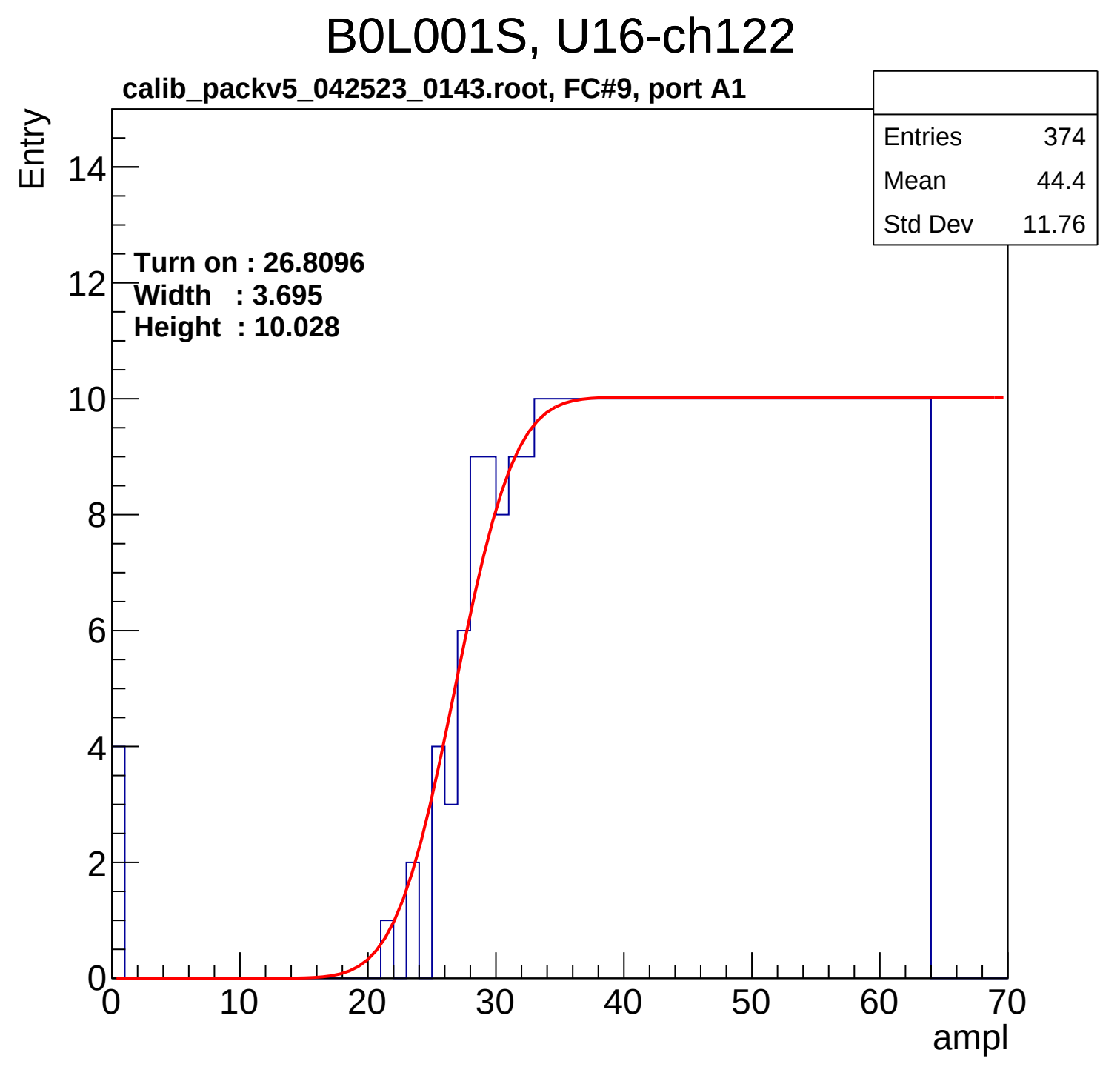
B0L001S, U16-ch122
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.4
Std Dev 11.76
Turn on : 26.8096
Width : 3.695
Height : 10.028
Entry
ampl
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2
4
6
8
10
12
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0
10
20
30
40
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60
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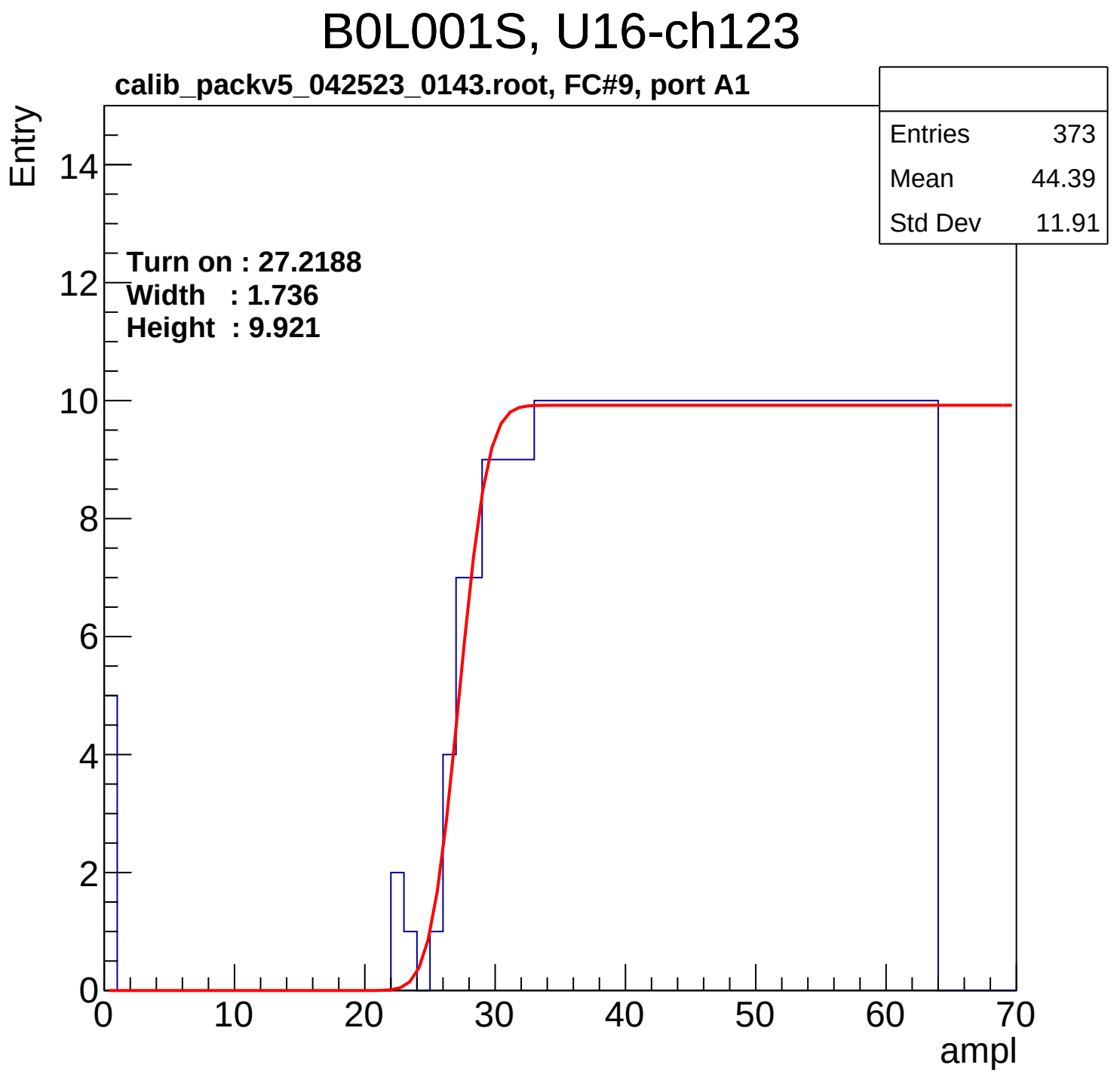
B0L001S, U16-ch123
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.39
Std Dev 11.91
Turn on : 27.2188
Width : 1.736
Height : 9.921
Entry
ampl
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2
4
6
8
10
12
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0
10
20
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40
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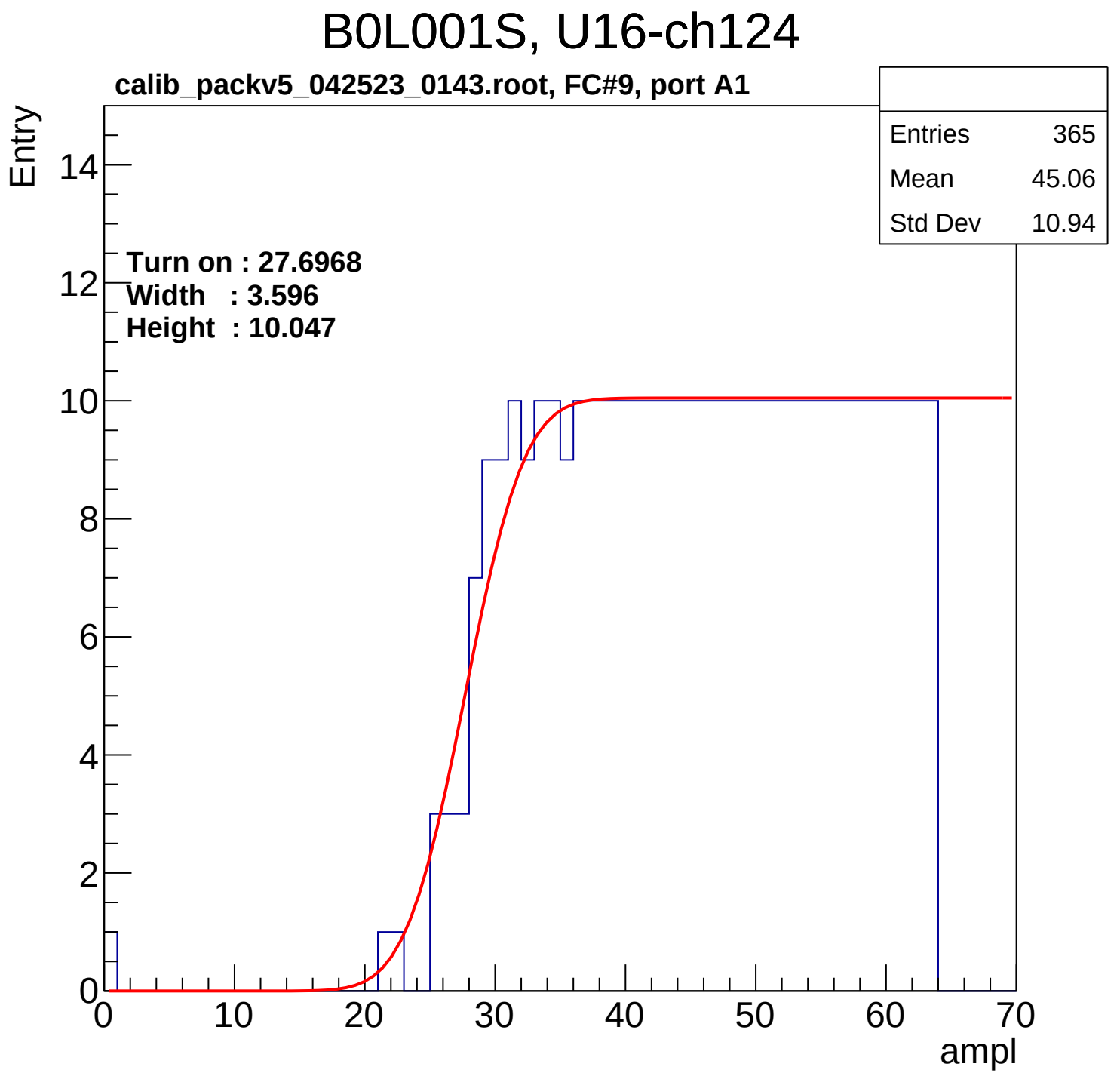
60
70


B0L001S, U16-ch124
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 45.06
Std Dev 10.94
Turn on : 27.6968
Width : 3.596
Height : 10.047
Entry
ampl
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4
6
8
10
12
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20
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40
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60
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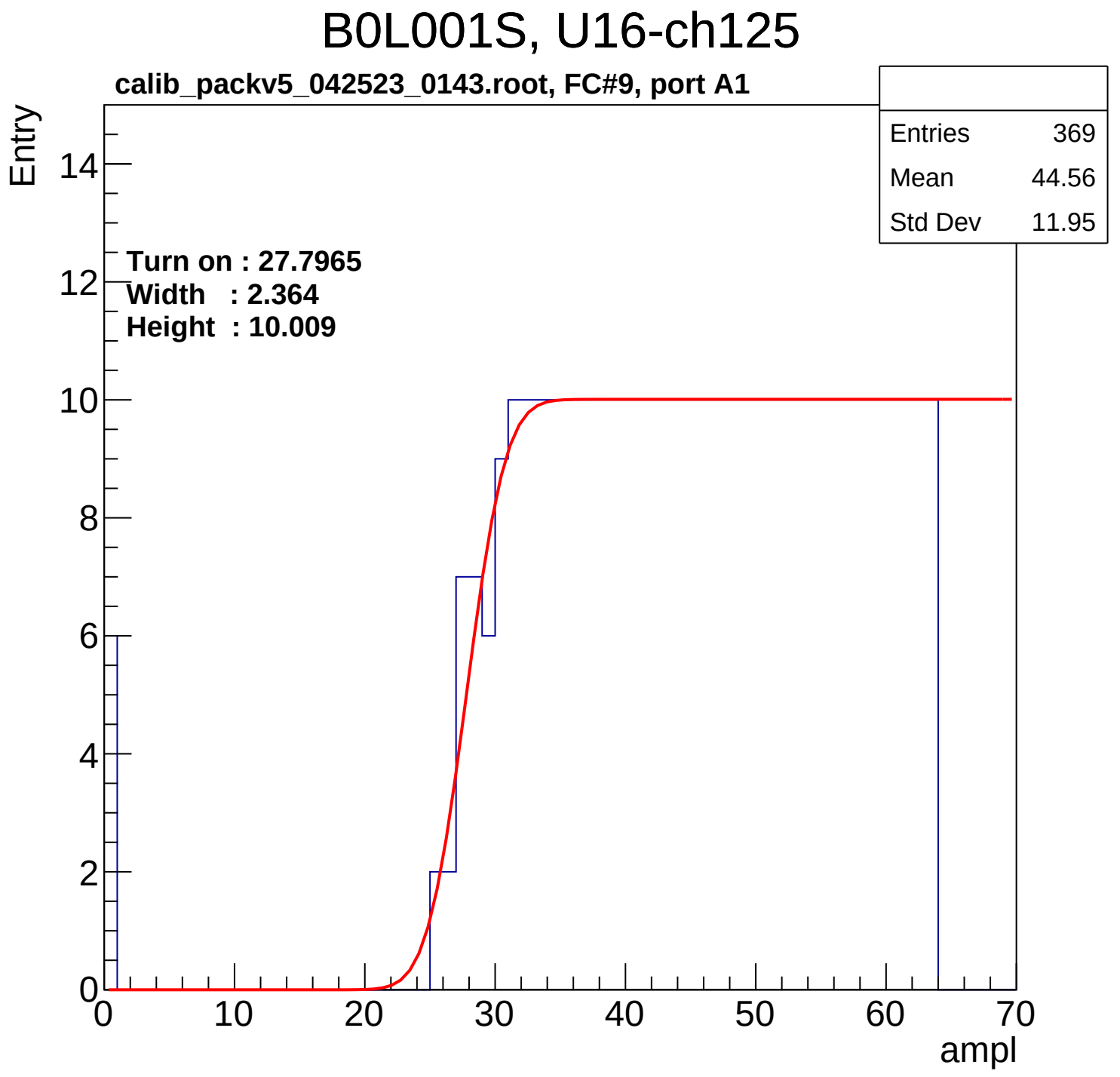
B0L001S, U16-ch125
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.56
Std Dev 11.95
Turn on : 27.7965
Width : 2.364
Height : 10.009
Entry
ampl
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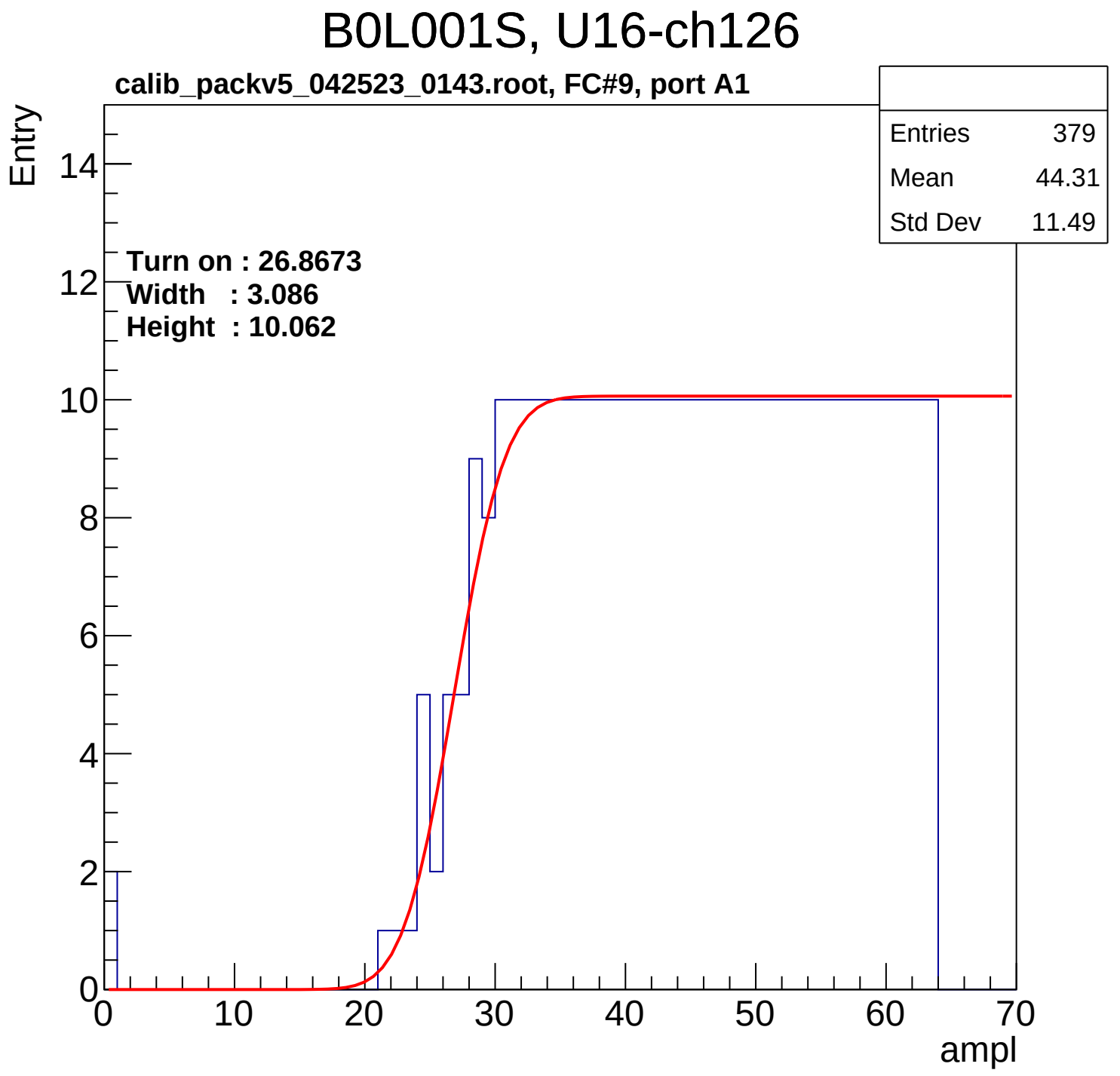
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U16-ch126
calib_packv5_042523_0143.root, FC#9, port A1
Entries 379
Mean 44.31
Std Dev 11.49
Turn on : 26.8673
Width : 3.086
Height : 10.062
Entry
ampl
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4
6
8
10
12
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0
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60
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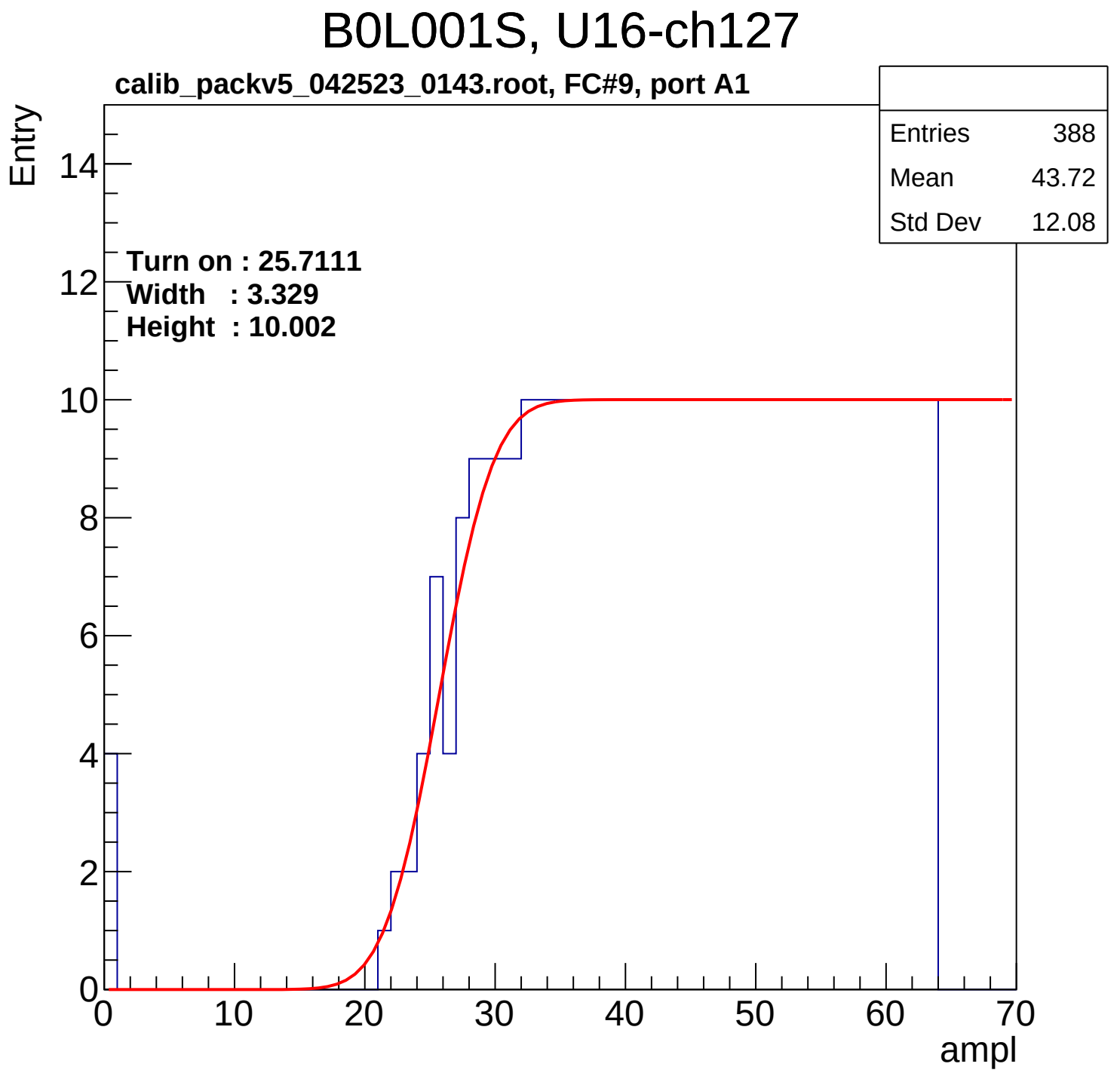
B0L001S, U16-ch127
calib_packv5_042523_0143.root, FC#9, port A1
Entries 388
Mean 43.72
Std Dev 12.08
Turn on : 25.7111
Width : 3.329
Height : 10.002
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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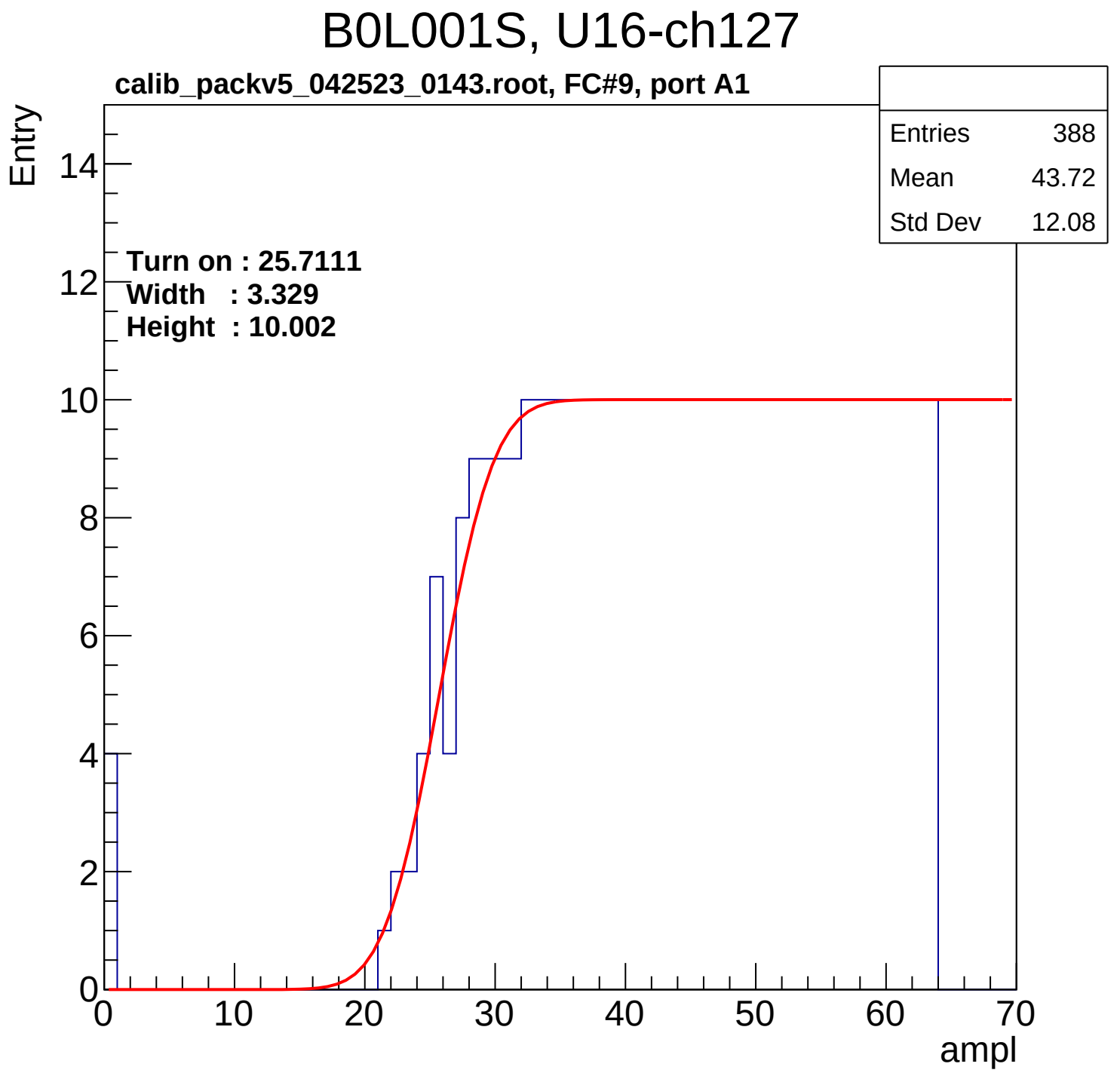
B0L001S, U16-ch127
calib_packv5_042523_0143.root, FC#9, port A1
Entries 388
Mean 43.72
Std Dev 12.08
Turn on : 25.7111
Width : 3.329
Height : 10.002
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
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70