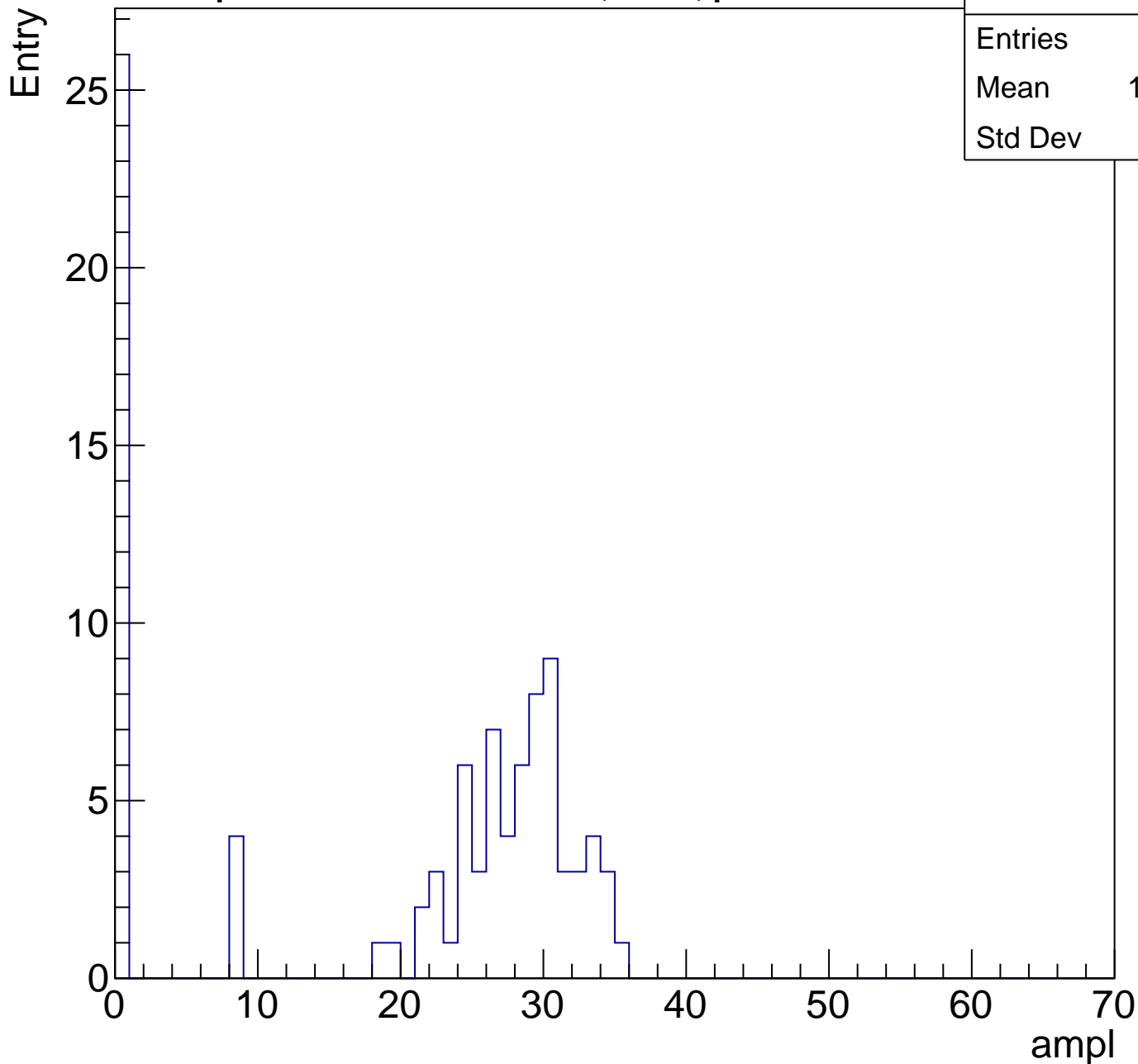


B1L103S, U5-ch0, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	95
Mean	19.34
Std Dev	12.9



B1L103S, U5-ch0, adc1

calib_packv5_041523_1651.root, FC#0, port C2

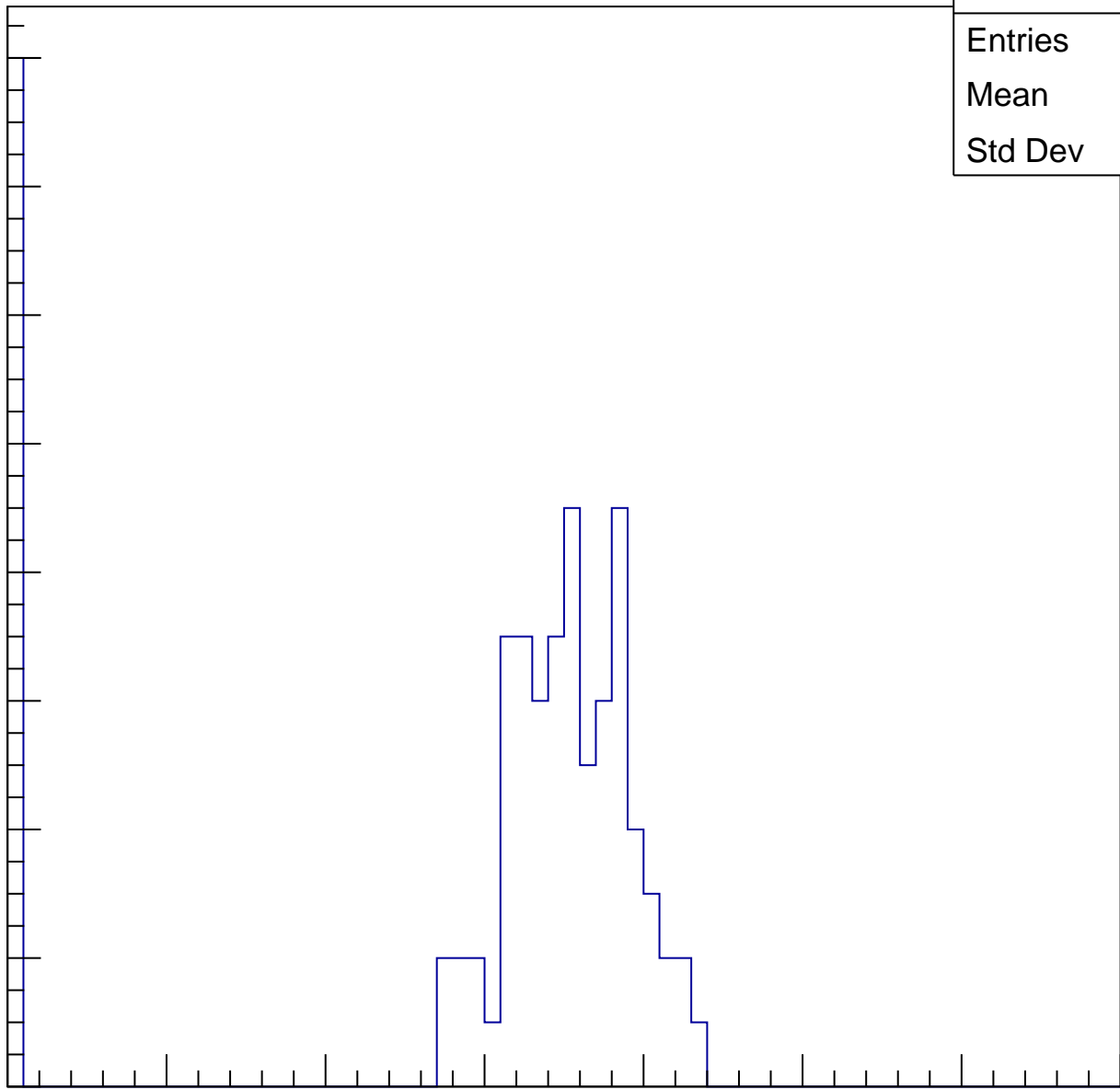
Entries	91
Mean	28.78
Std Dev	13.7

Entry

16
14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

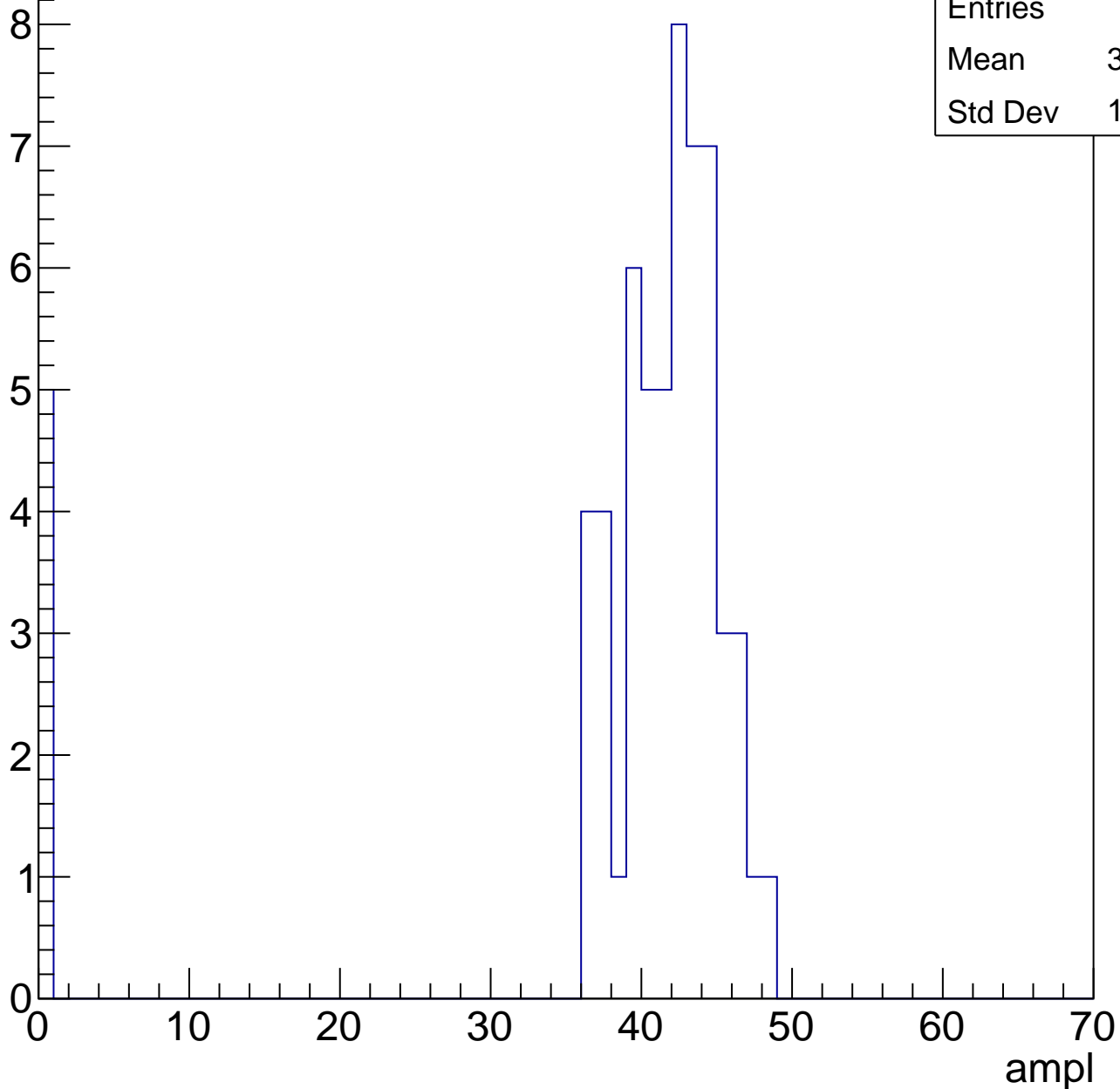


B1L103S, U5-ch0, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	38.03
Std Dev	11.82

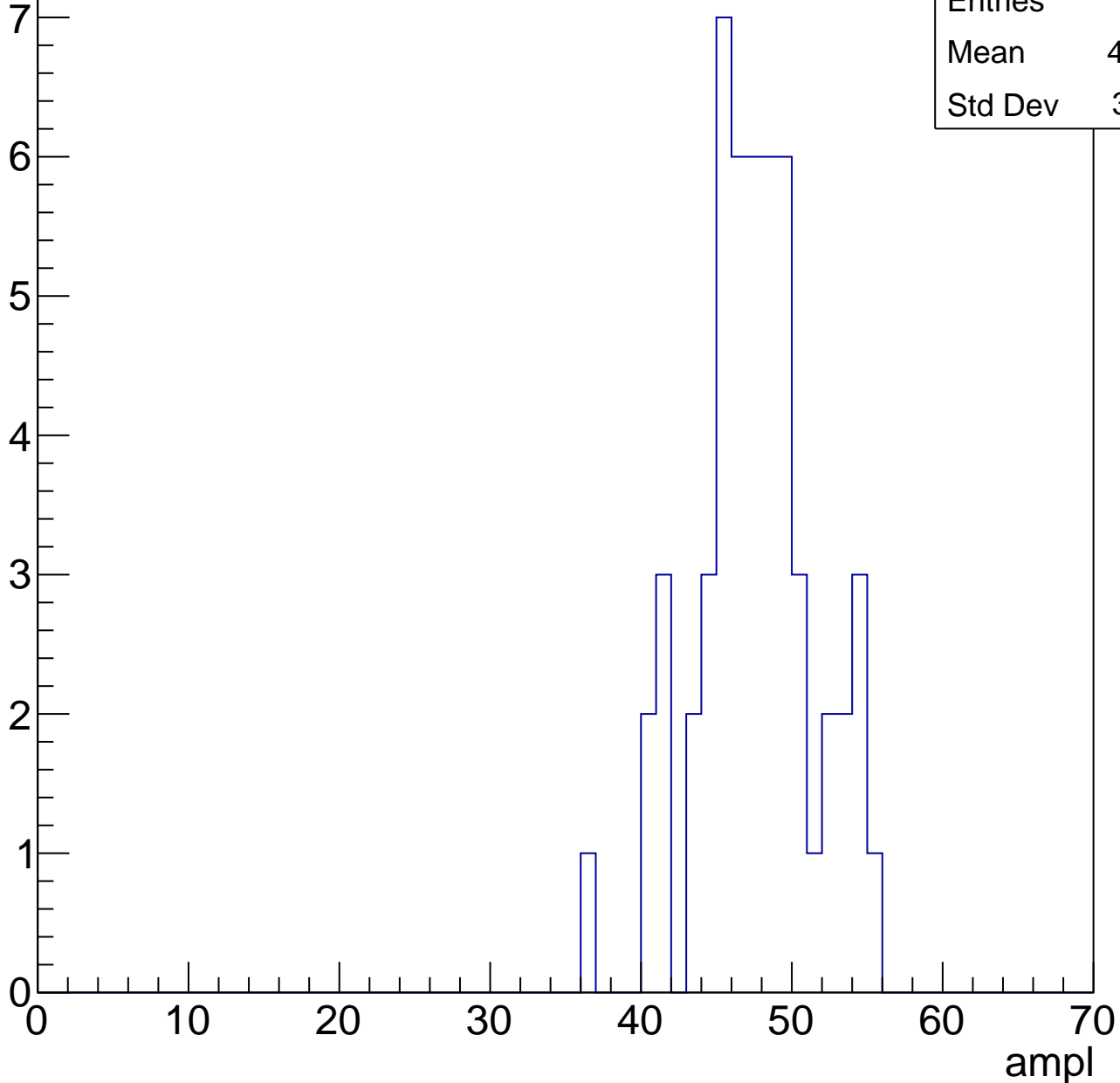


B1L103S, U5-ch0, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	47.04
Std Dev	3.911

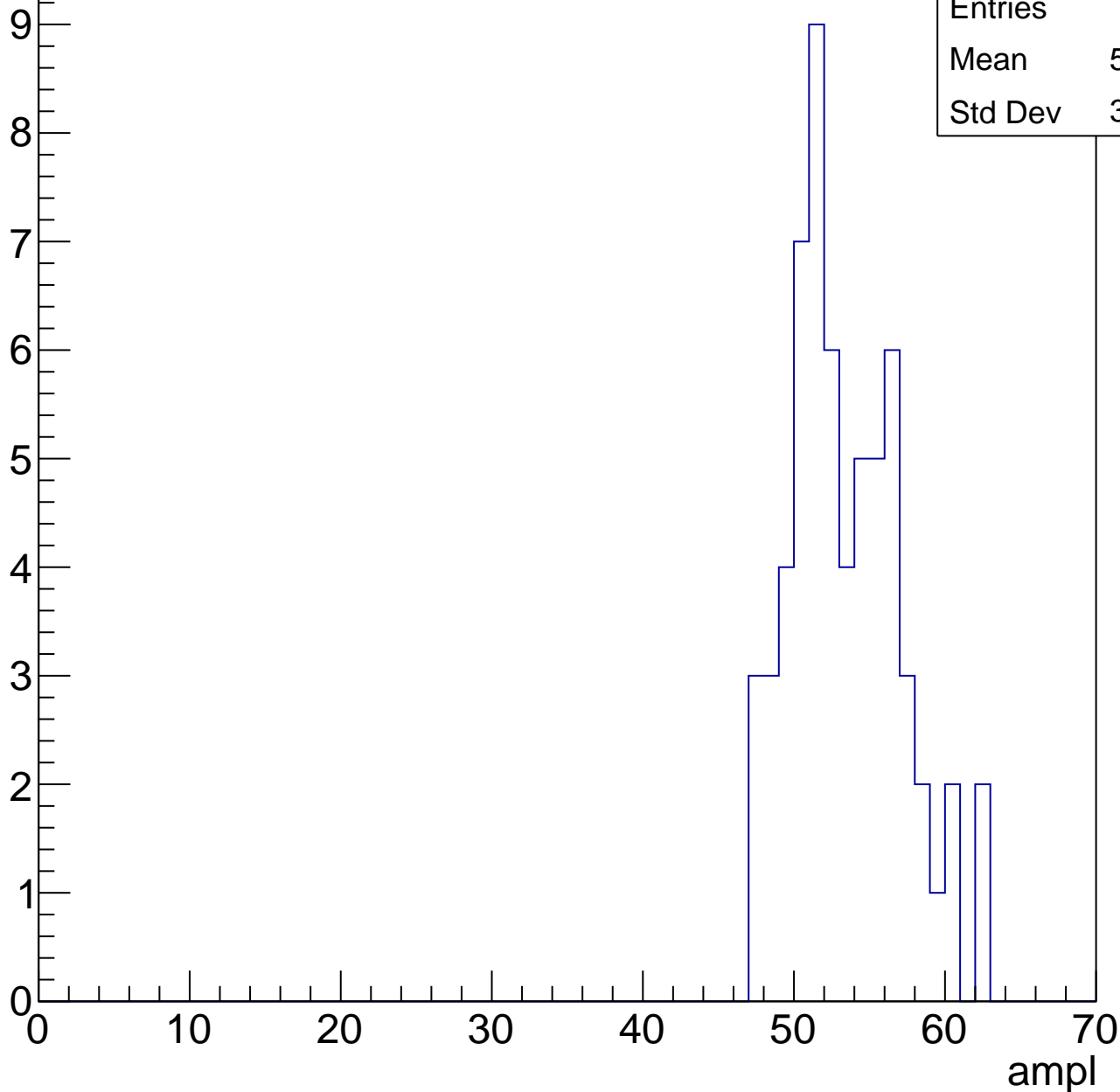


B1L103S, U5-ch0, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

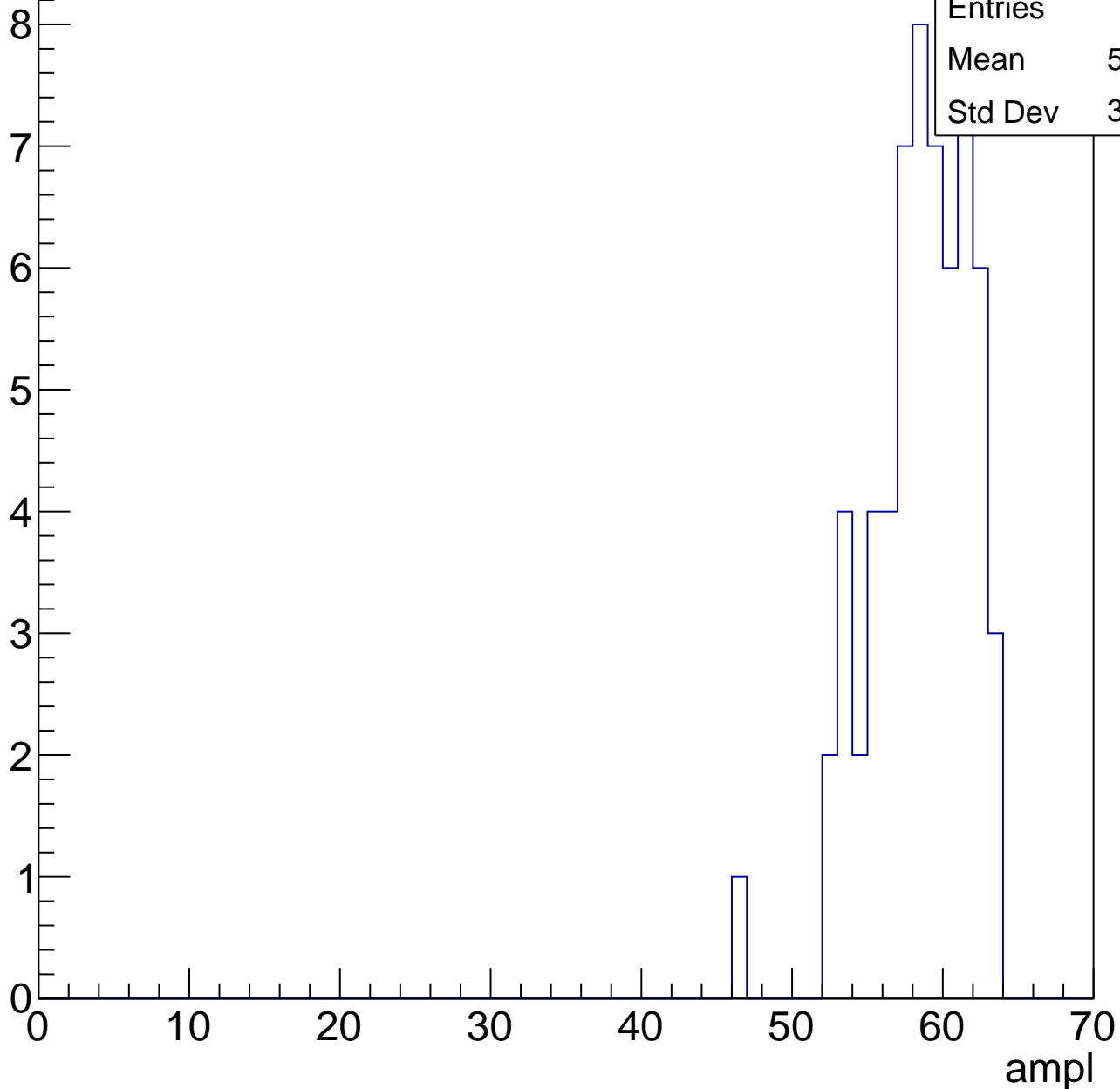
Entries	62
Mean	52.98
Std Dev	3.648



B1L103S, U5-ch0, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



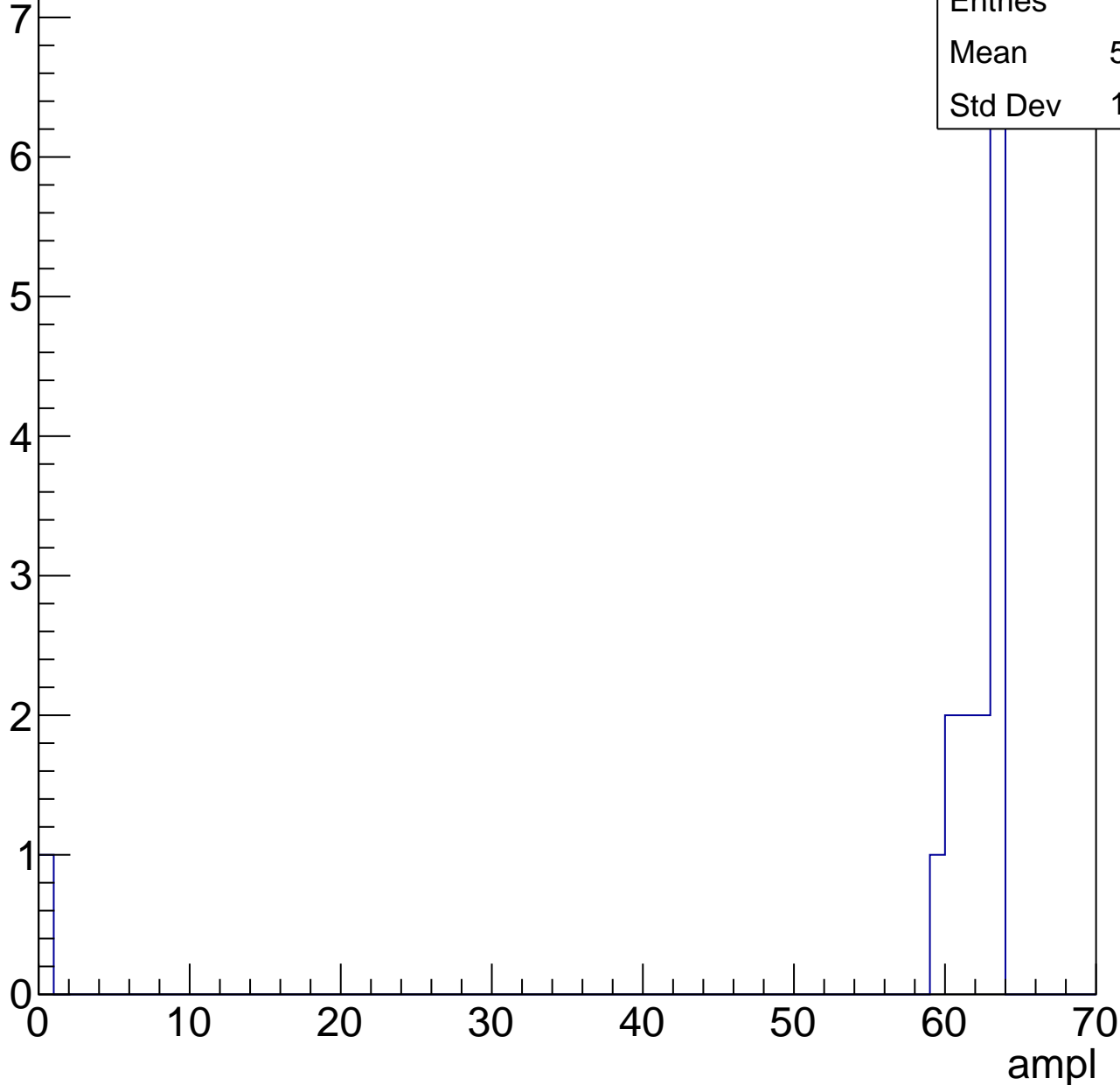
Entries	62
Mean	58.05
Std Dev	3.314

B1L103S, U5-ch0, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

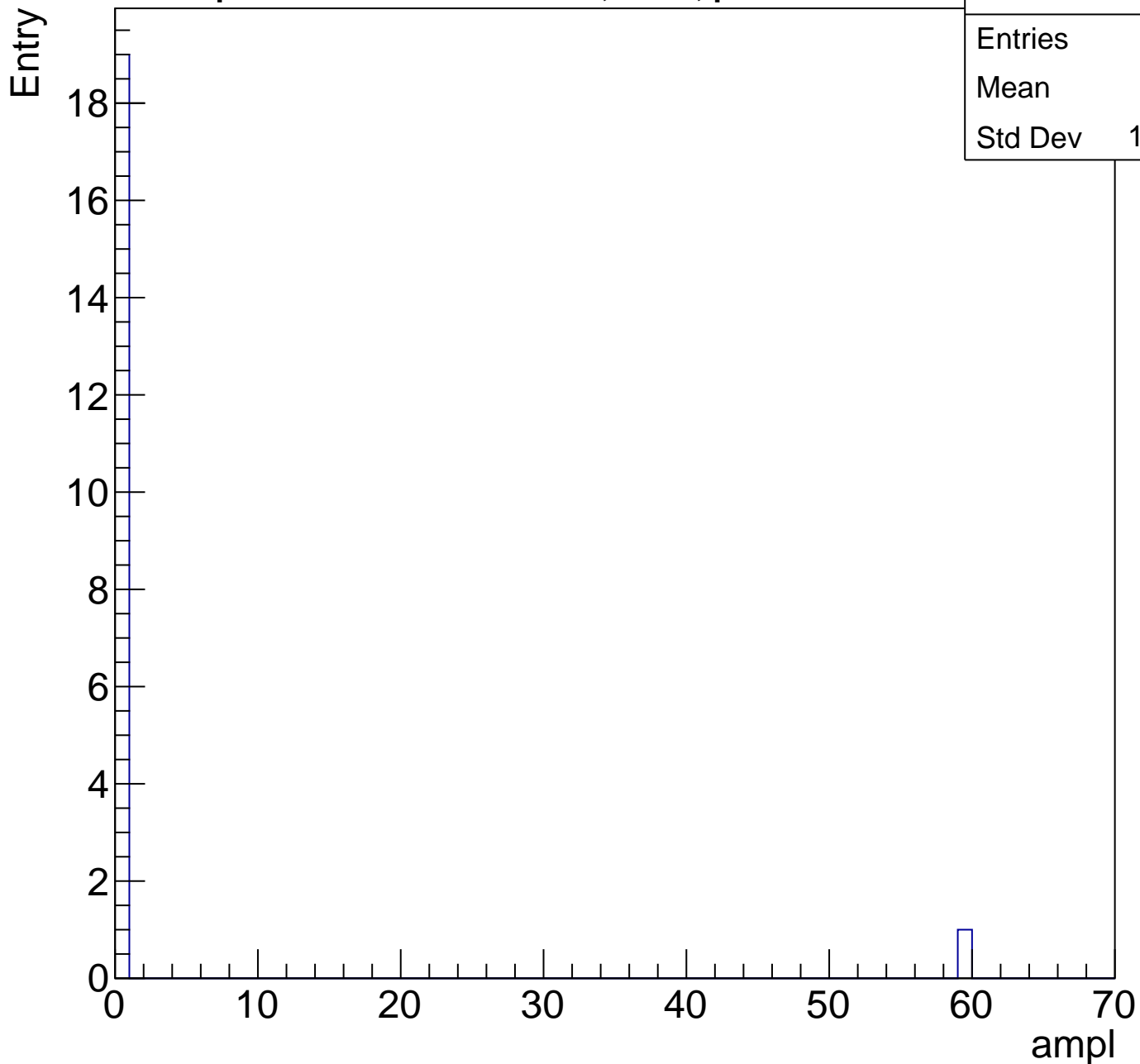
Entries	15
Mean	57.73
Std Dev	15.49



B1L103S, U5-ch0, adc7

calib_packv5_041523_1651.root, FC#0, port C2

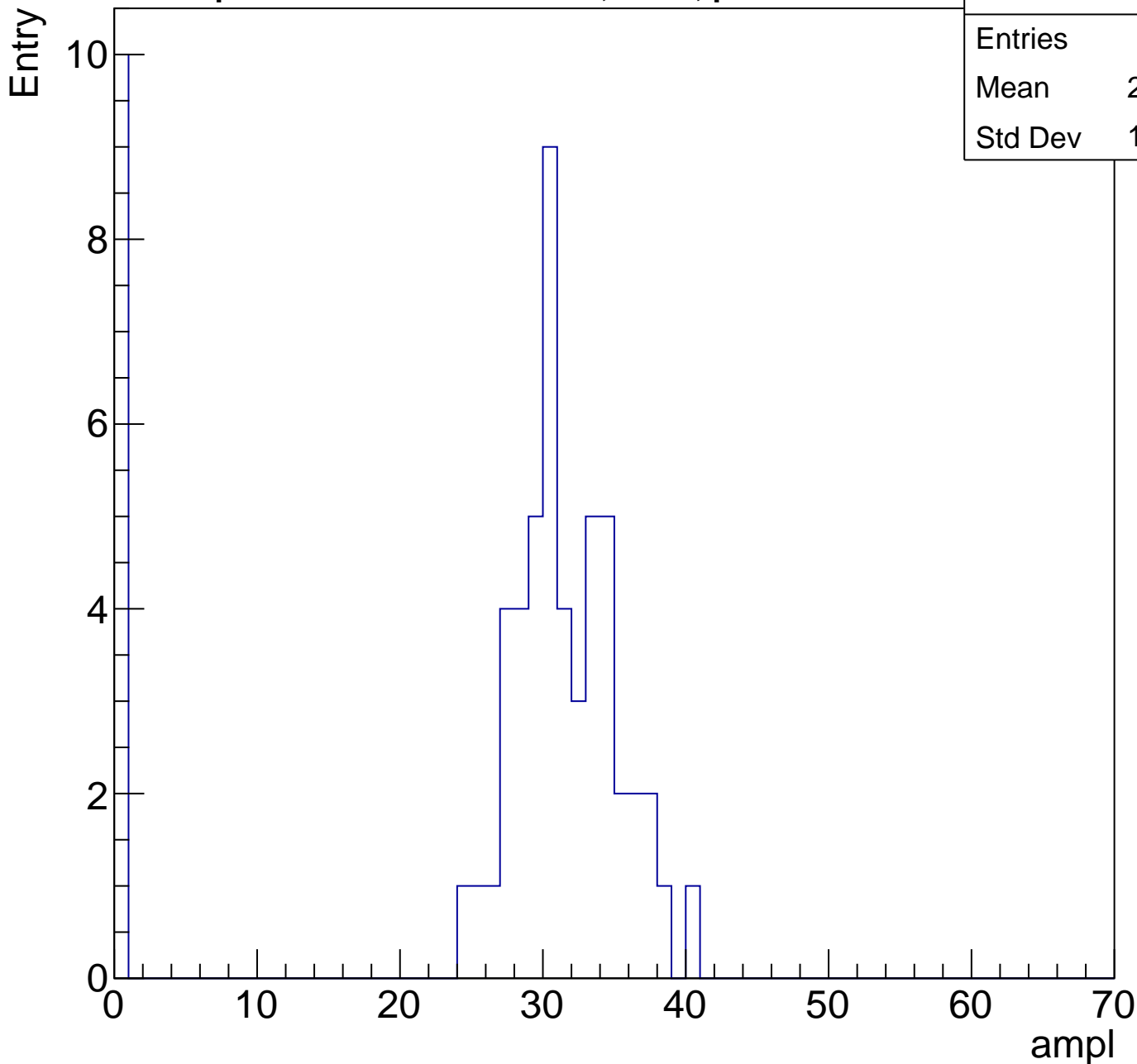
Entries	20
Mean	2.95
Std Dev	12.86



B1L103S, U5-ch1, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	60
Mean	25.98
Std Dev	12.04

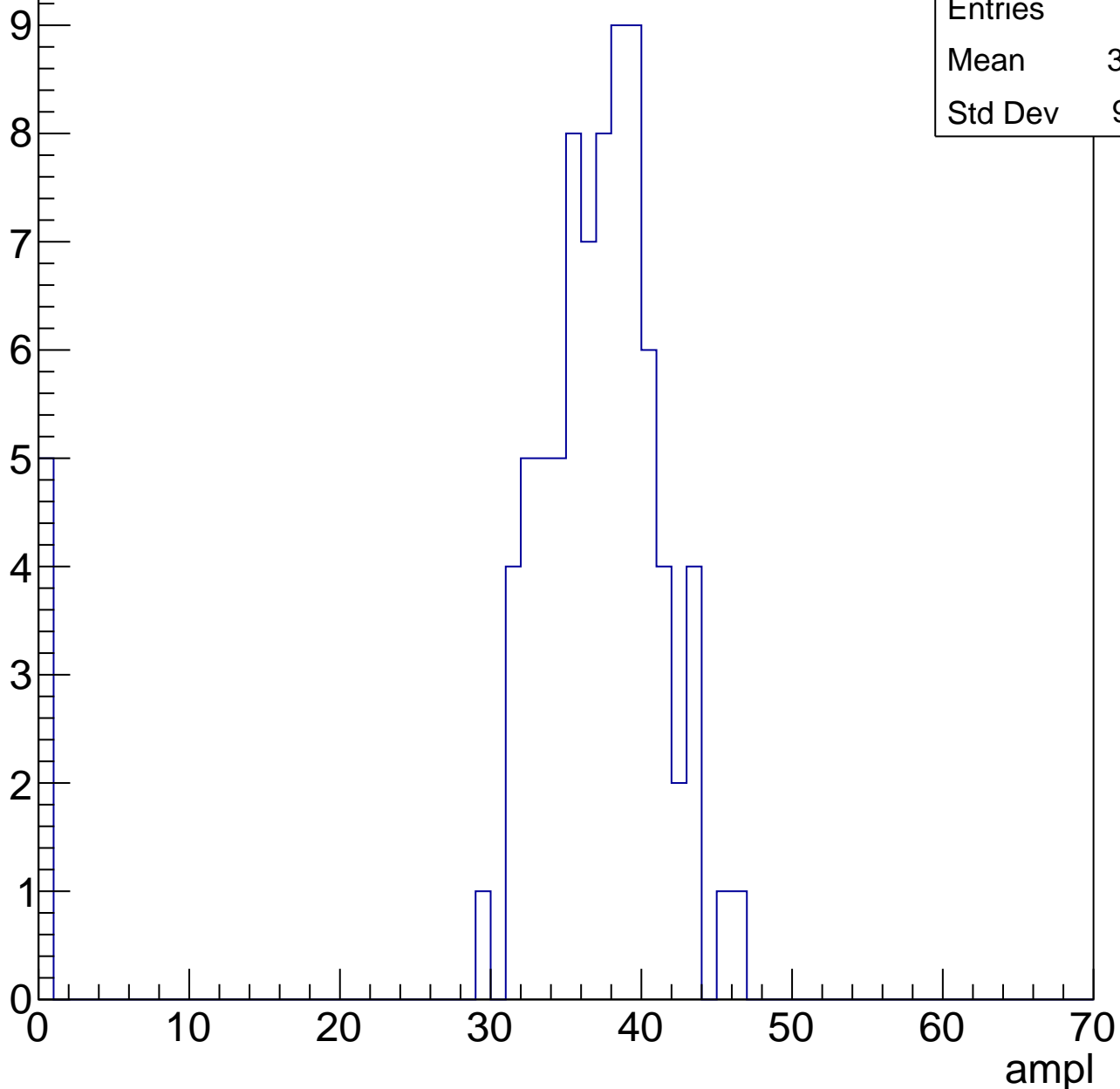


B1L103S, U5-ch1, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	84
Mean	34.76
Std Dev	9.401

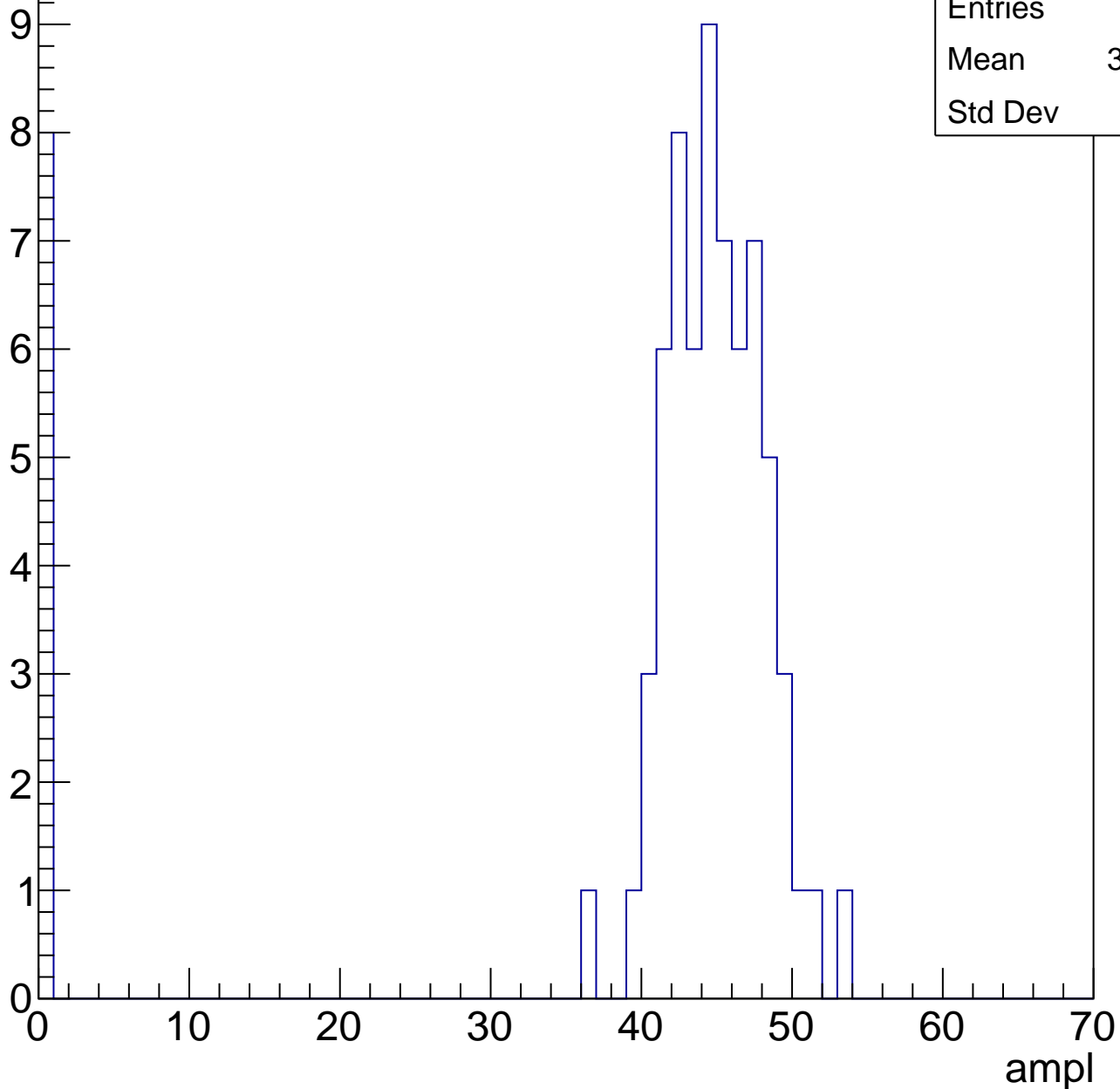


B1L103S, U5-ch1, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

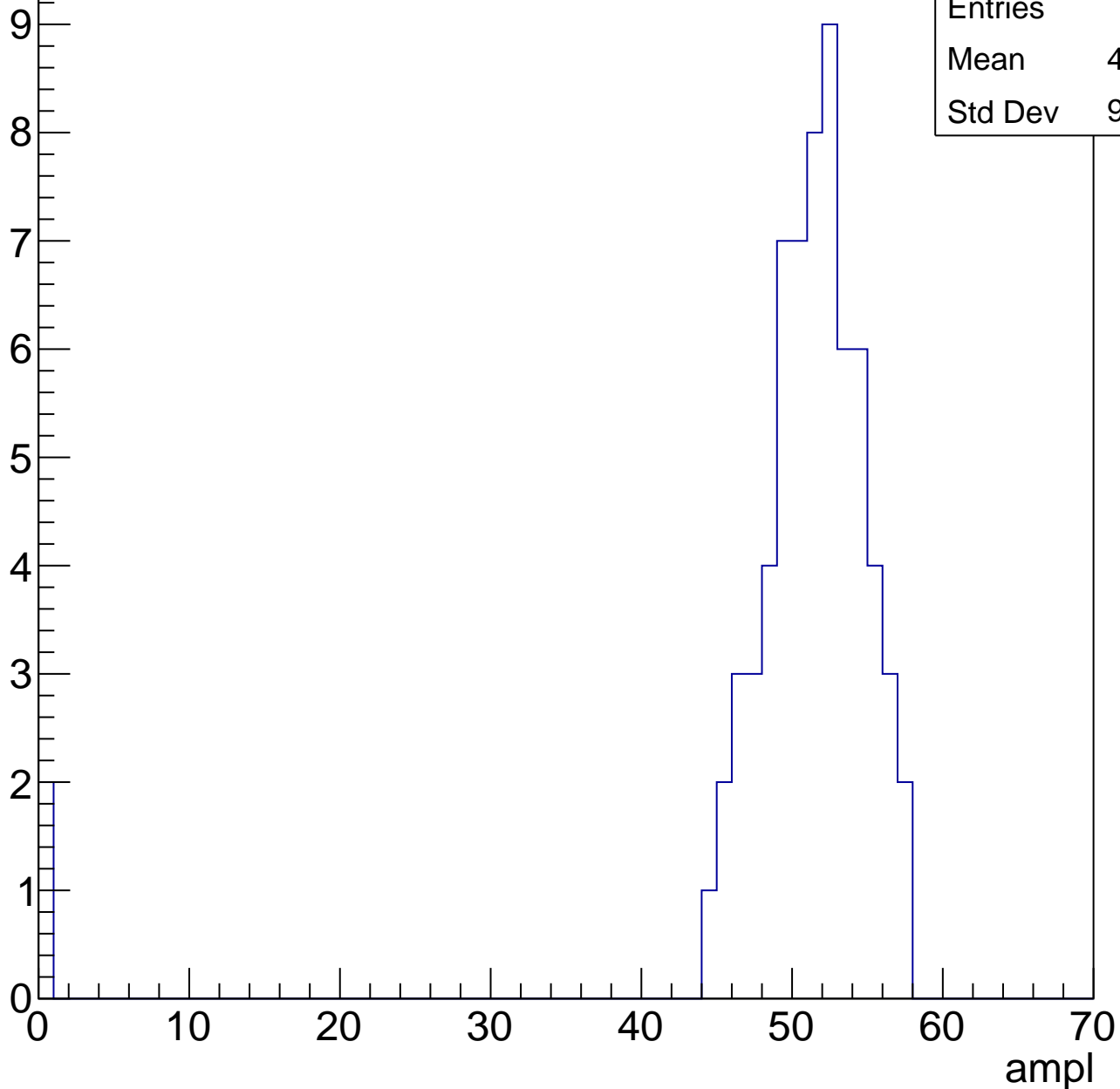
Entries	73
Mean	39.62
Std Dev	14.2



B1L103S, U5-ch1, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

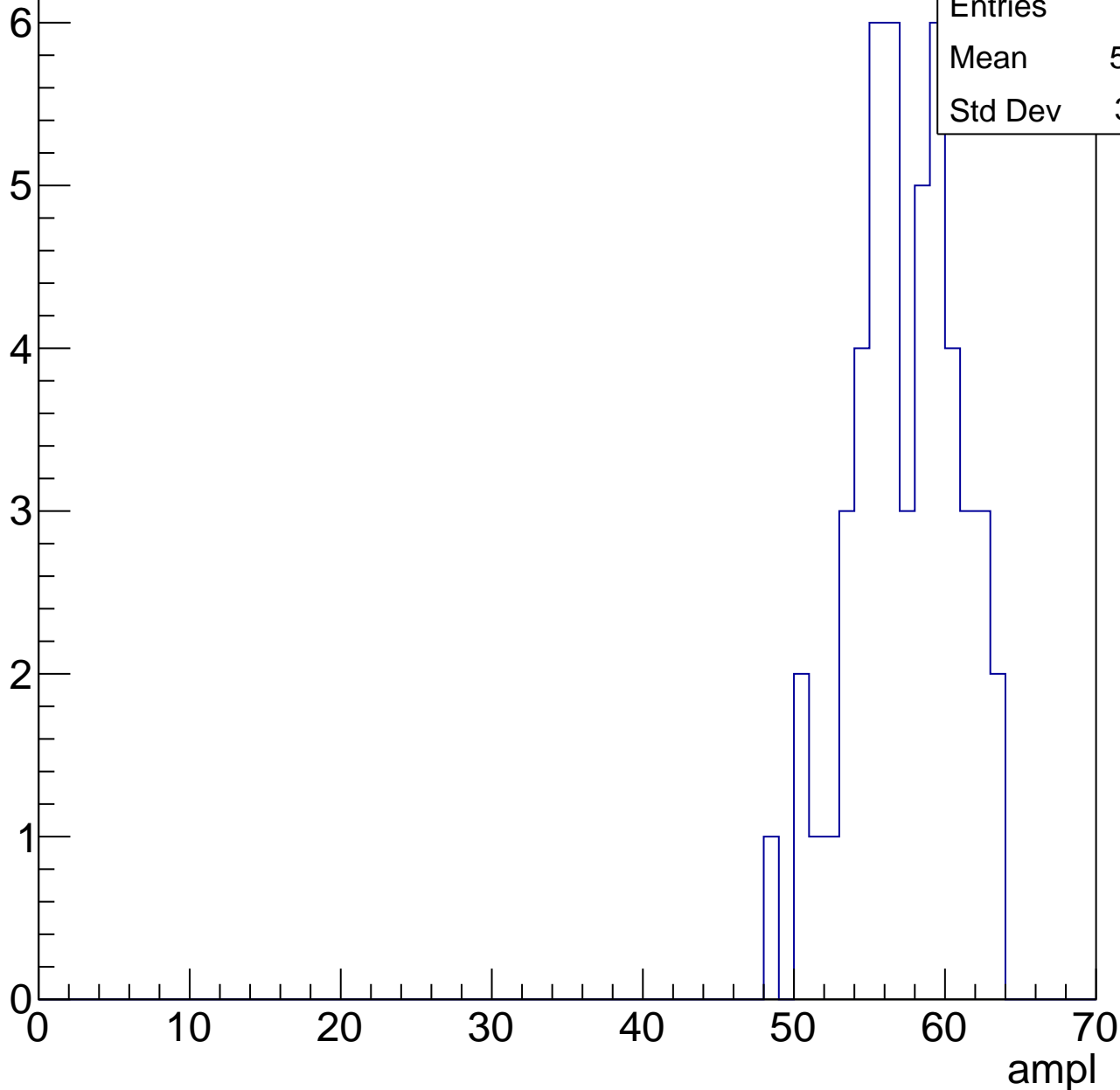


Entries	67
Mean	49.52
Std Dev	9.198

B1L103S, U5-ch1, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

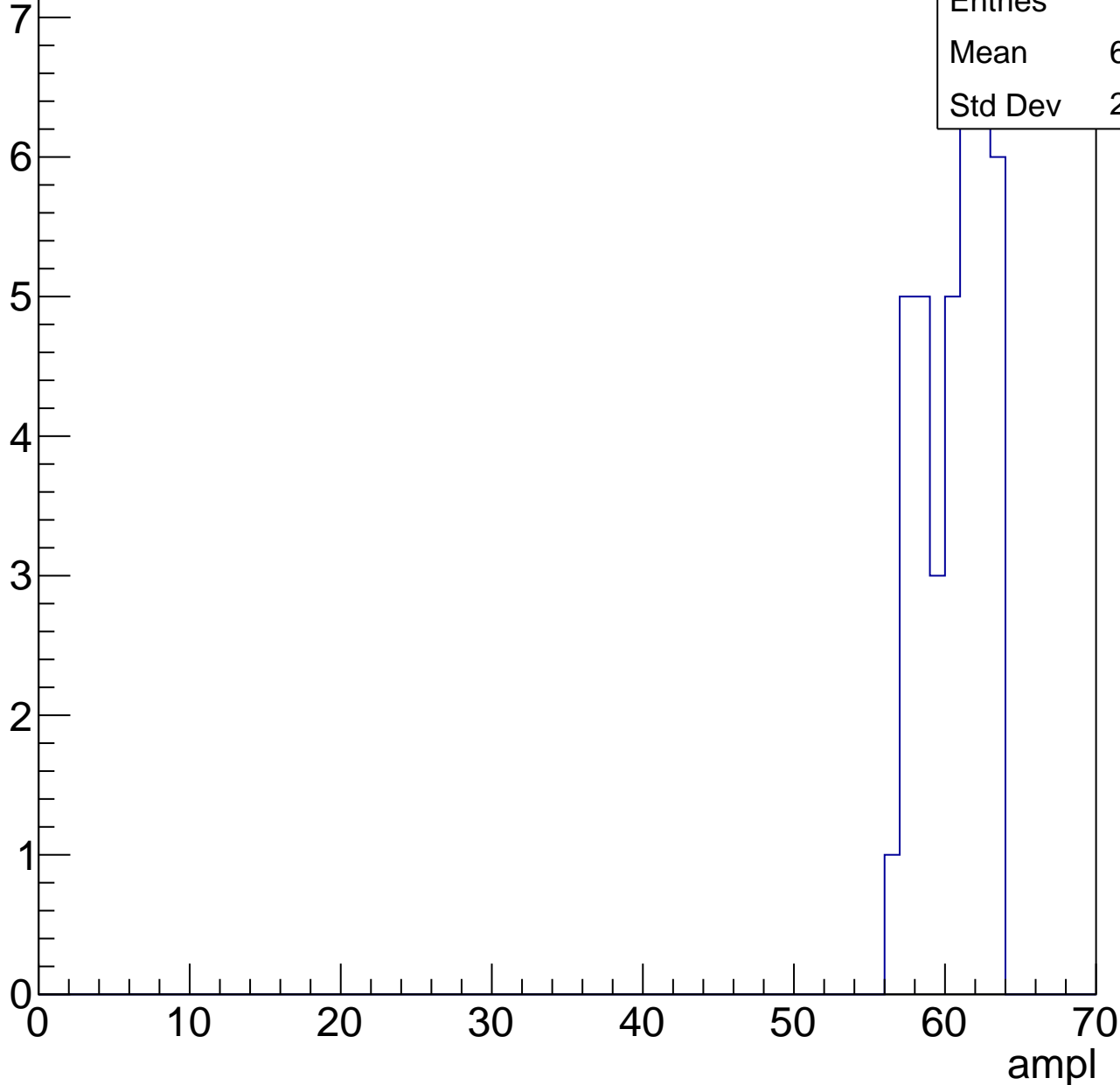


B1L103S, U5-ch1, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

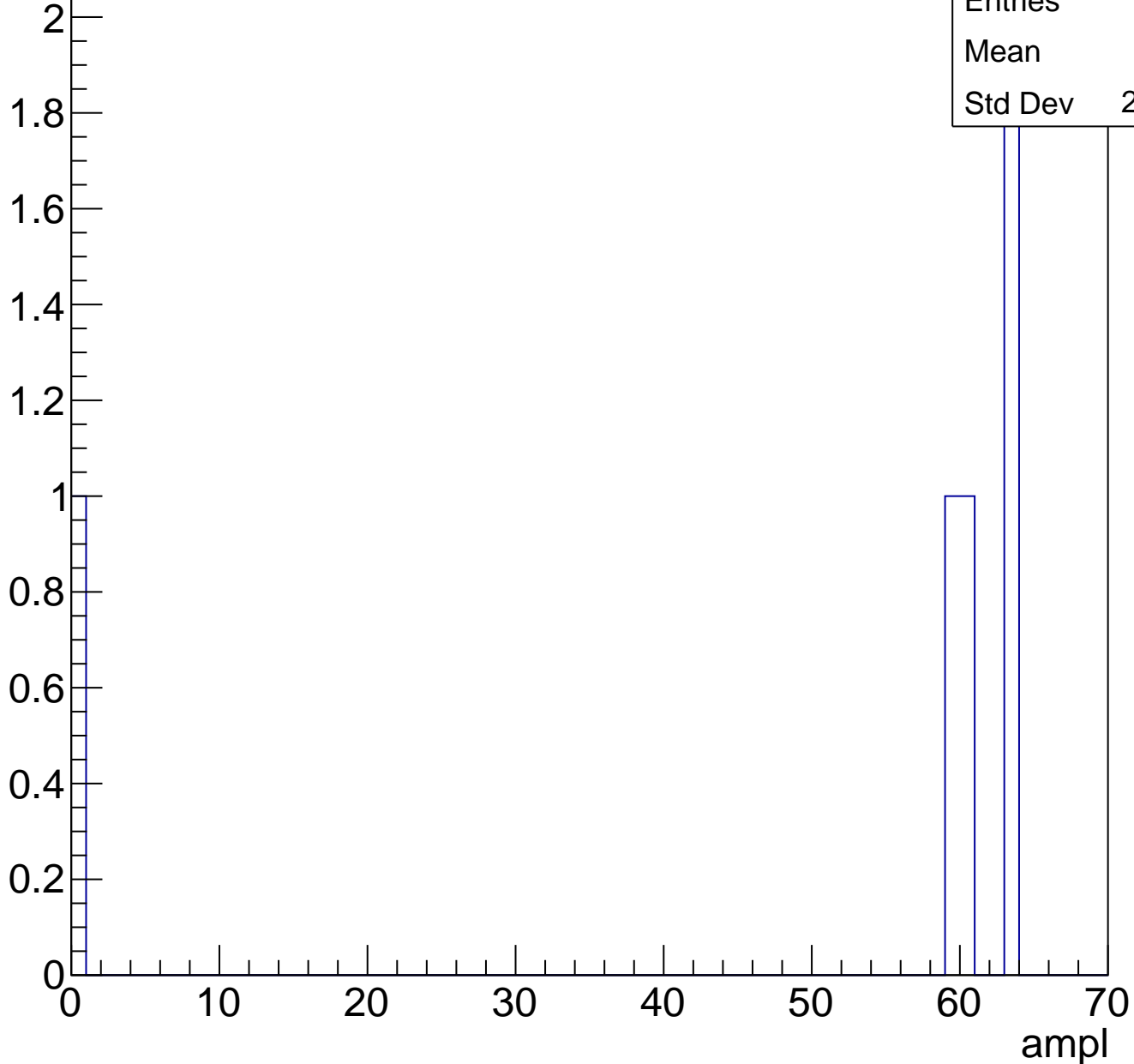
Entries	39
Mean	60.18
Std Dev	2.098



B1L103S, U5-ch1, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

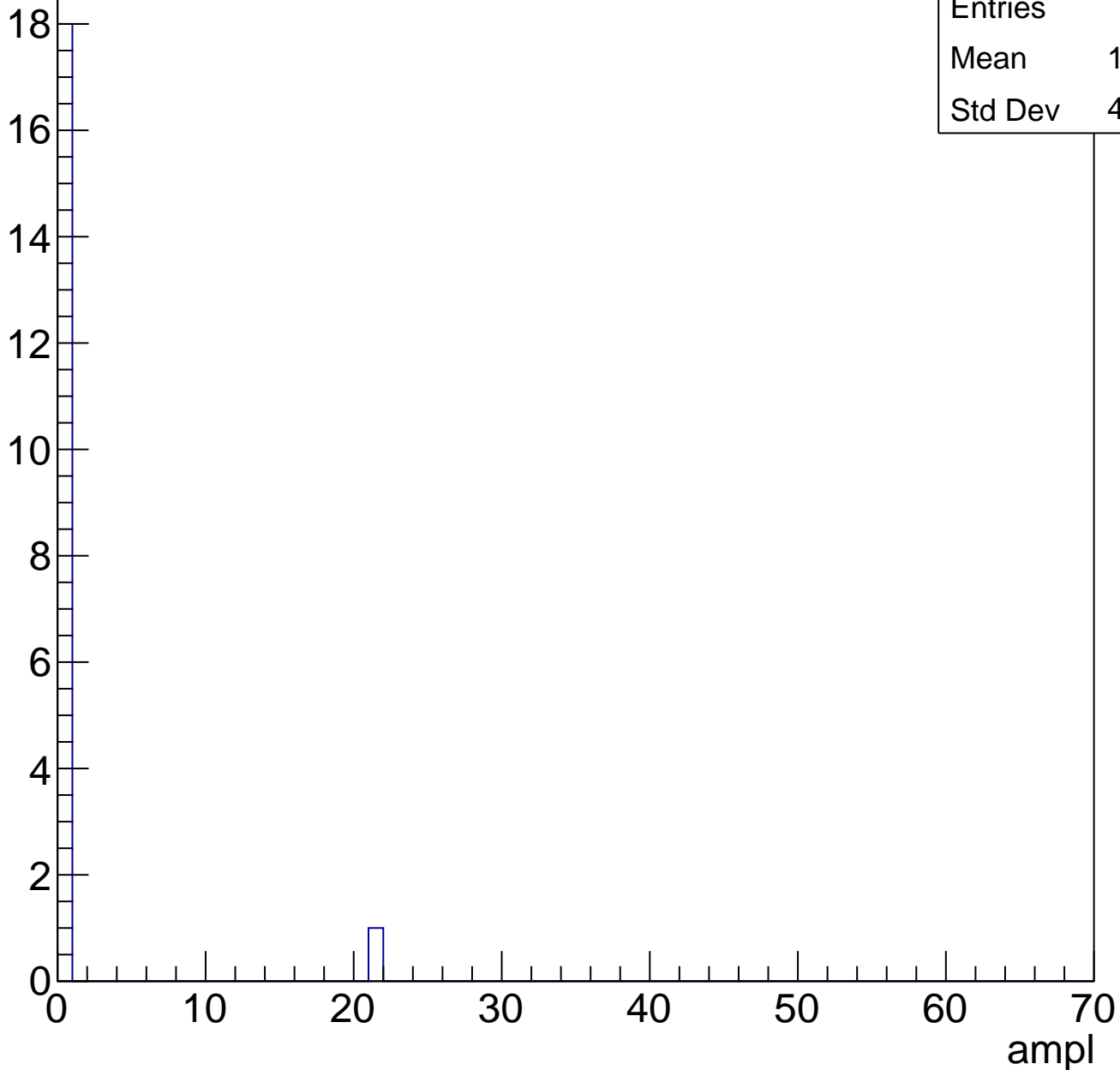


B1L103S, U5-ch1, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.105
Std Dev	4.689

Entry

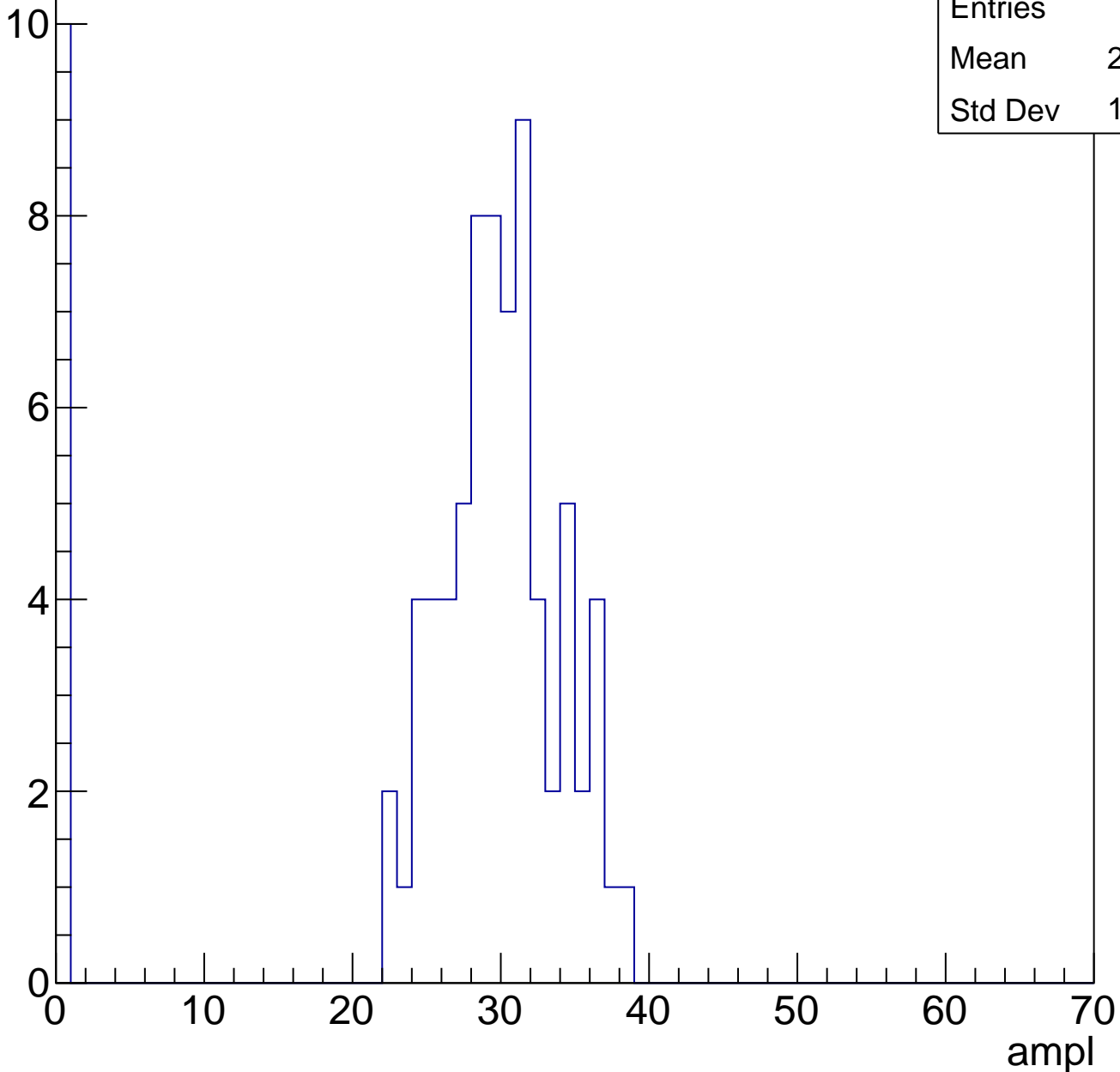


B1L103S, U5-ch2, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	25.93
Std Dev	10.34

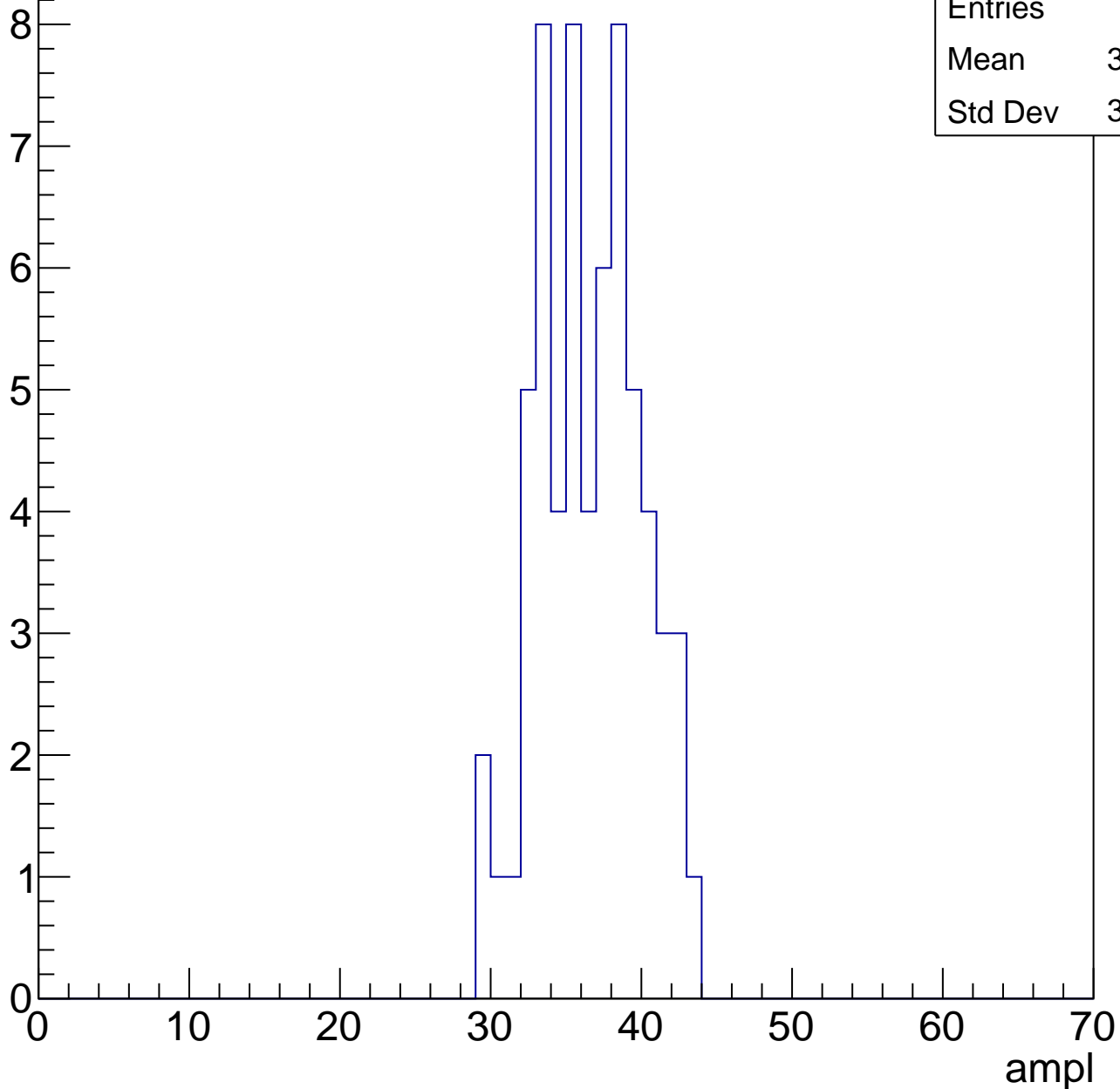
Entry



B1L103S, U5-ch2, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry



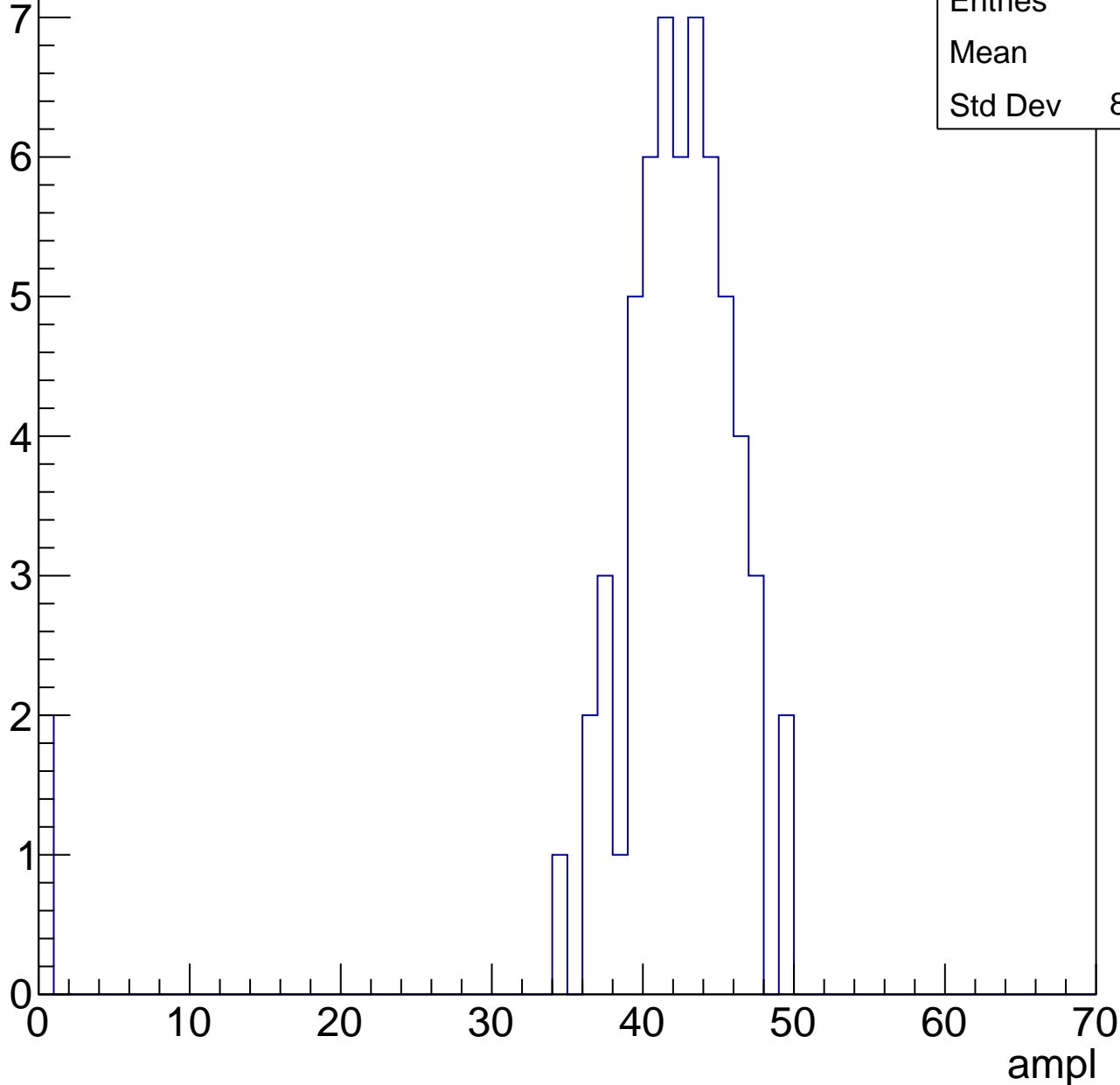
Entries	63
Mean	36.13
Std Dev	3.364

B1L103S, U5-ch2, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	40.7
Std Dev	8.208



B1L103S, U5-ch2, adc3

calib_packv5_041523_1651.root, FC#0, port C2

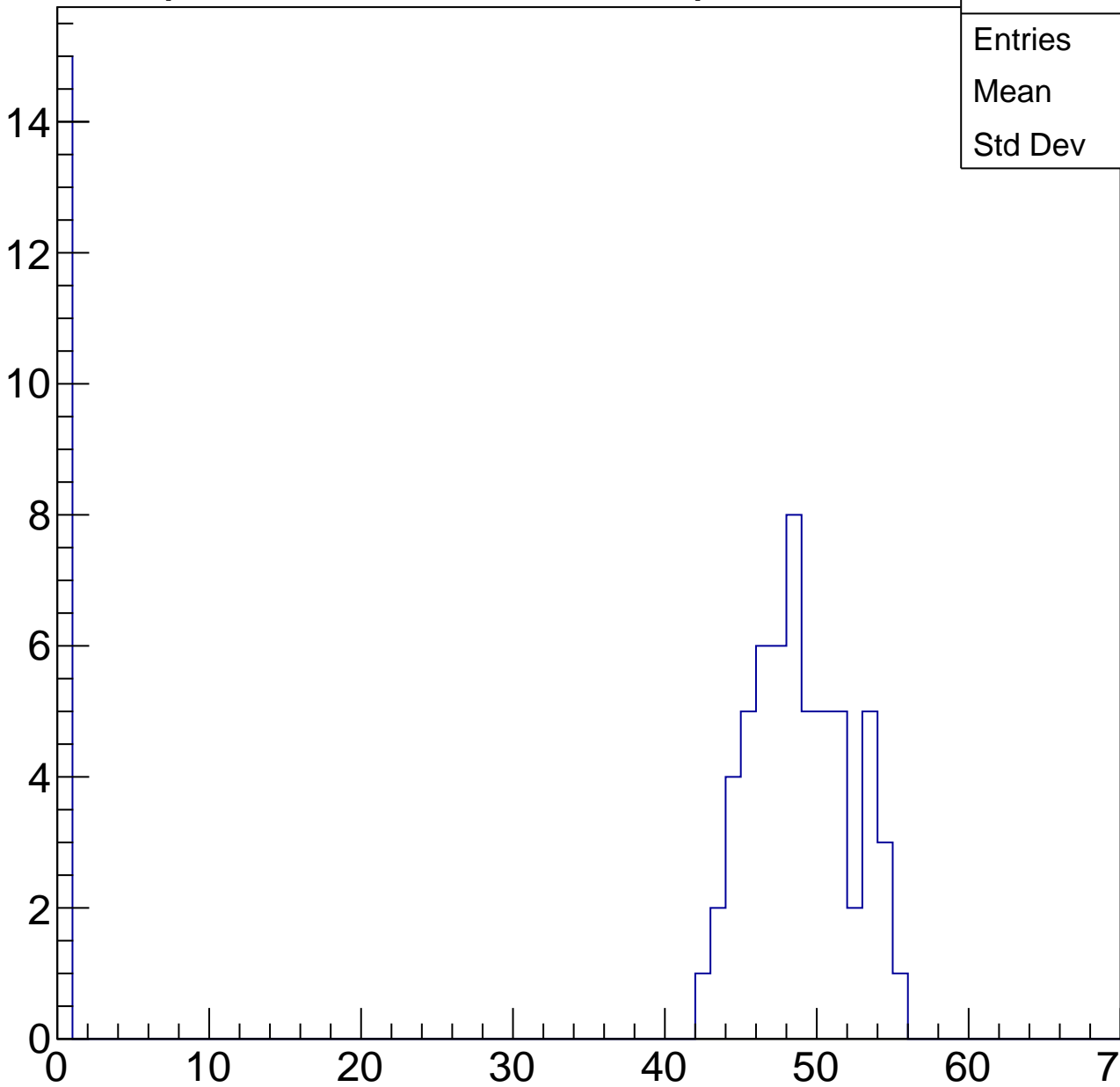
Entries	73
Mean	38.45
Std Dev	19.76

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

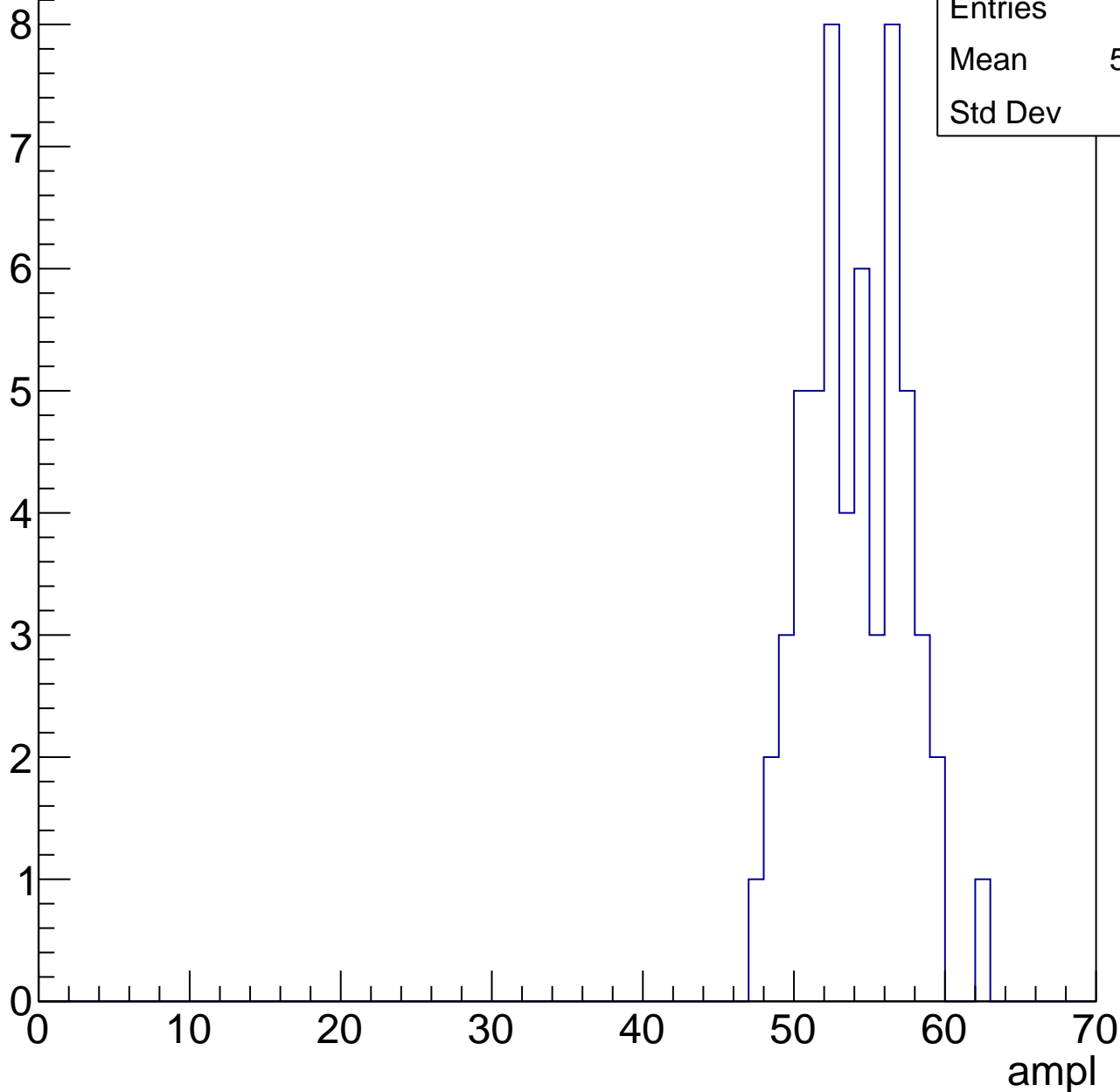


B1L103S, U5-ch2, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	53.55
Std Dev	3.24



B1L103S, U5-ch2, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entries	60
Mean	59.25
Std Dev	2.592

Entry

10

8

6

4

2

0

0

10

20

30

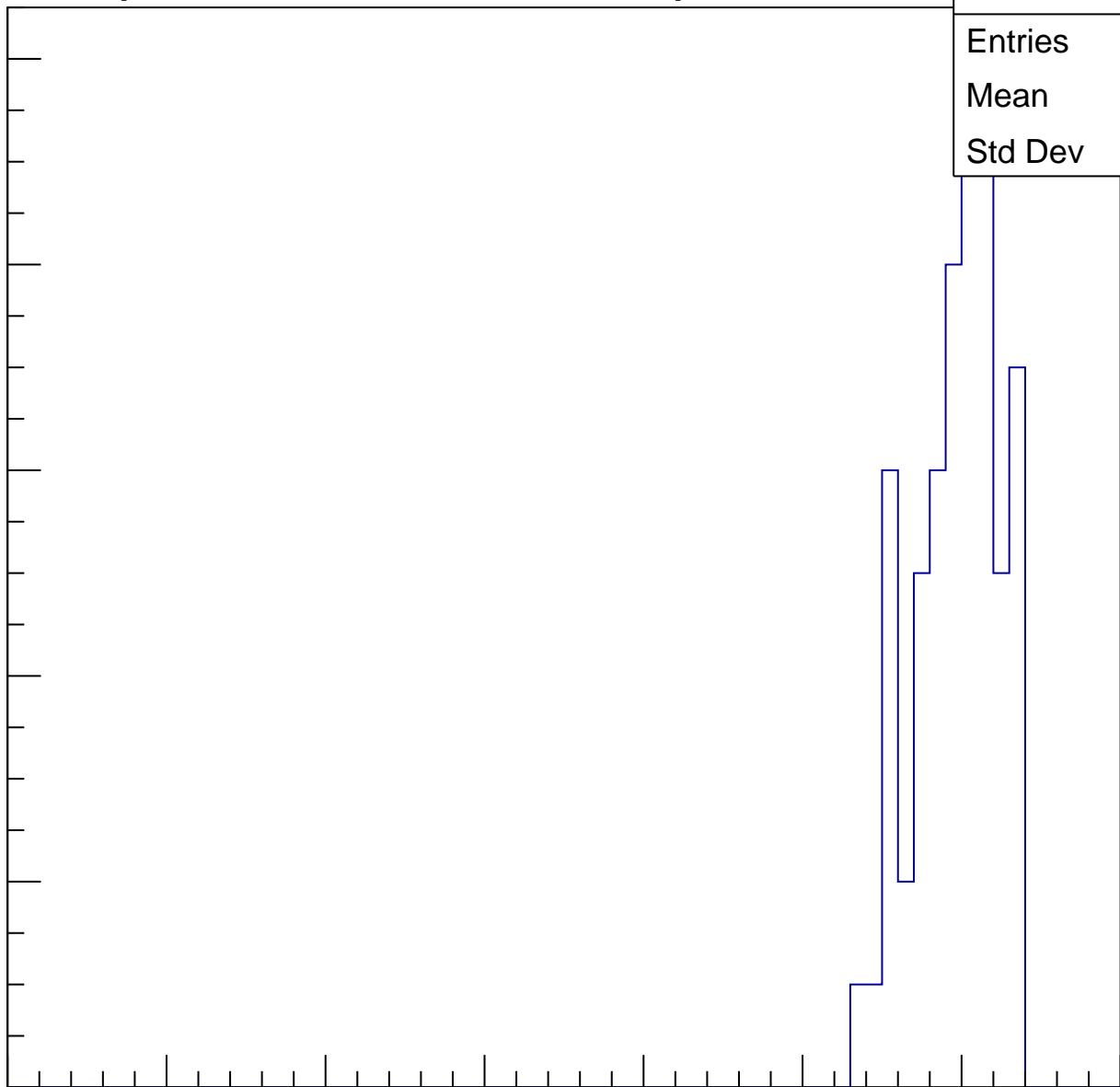
40

50

60

70

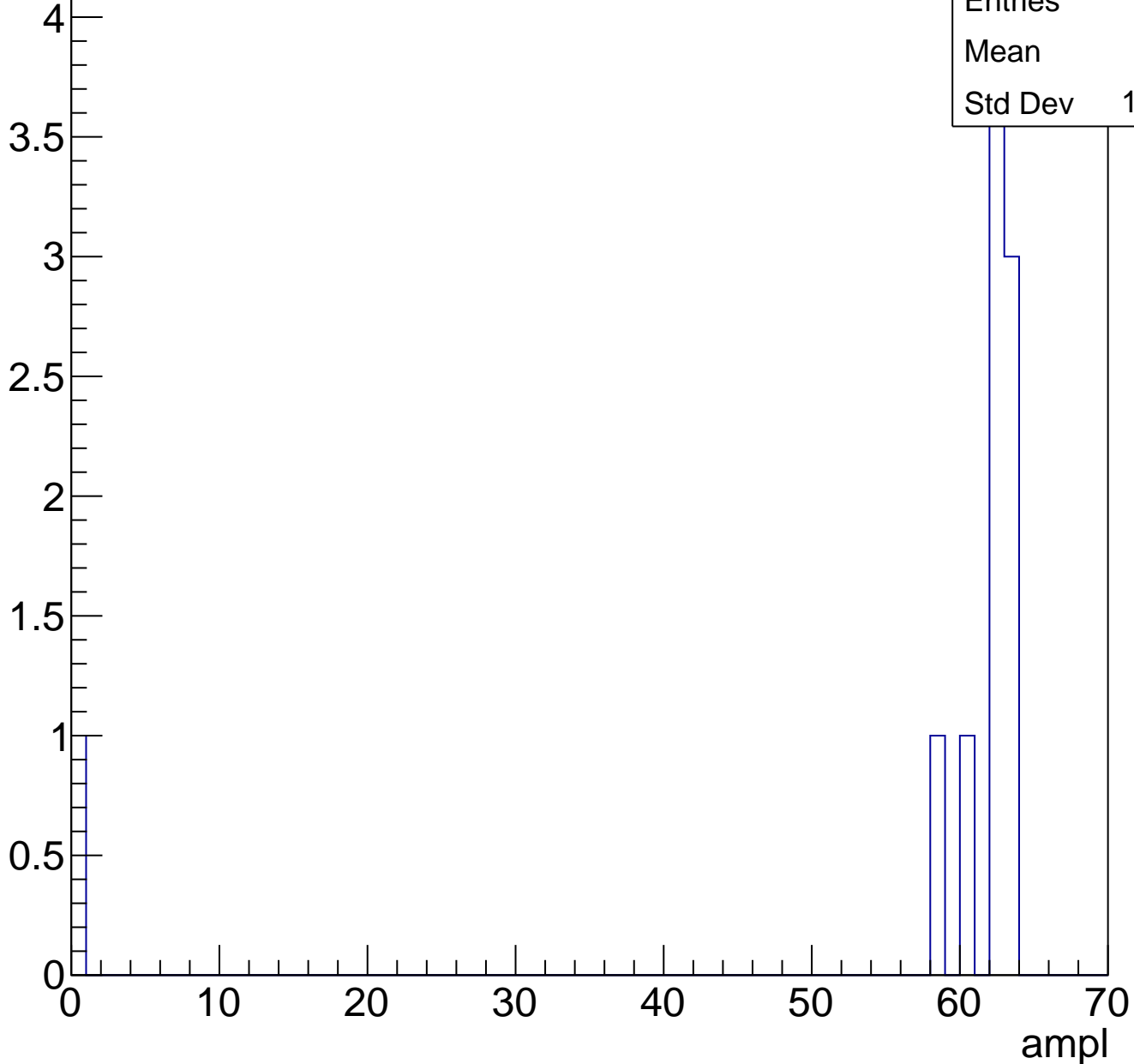
ampl



B1L103S, U5-ch2, adc6

calib_packv5_041523_1651.root, FC#0, port C2

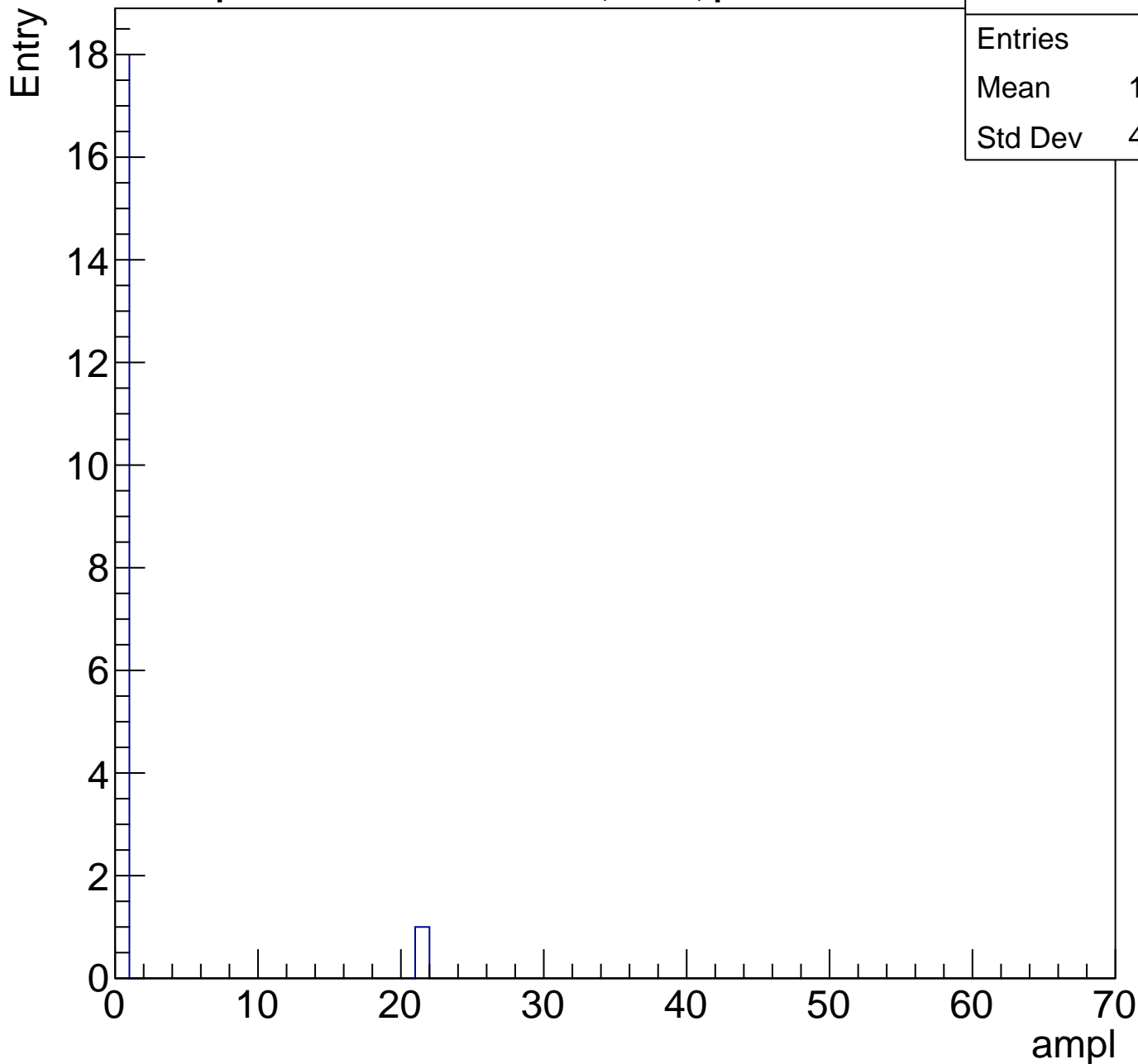
Entry



B1L103S, U5-ch2, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.105
Std Dev	4.689

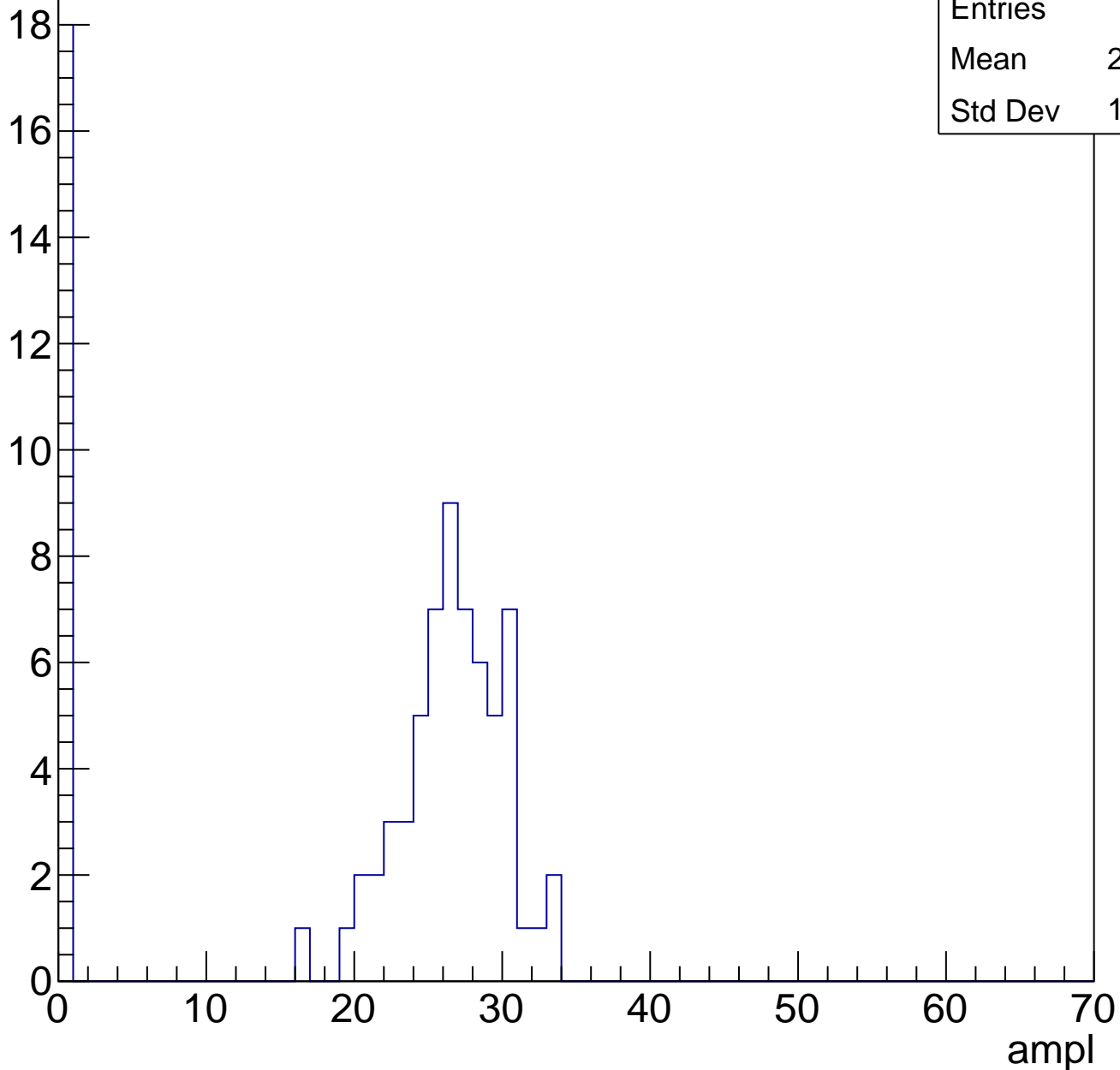


B1L103S, U5-ch3, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	20.27
Std Dev	11.33

Entry



B1L103S, U5-ch3, adc1

calib_packv5_041523_1651.root, FC#0, port C2

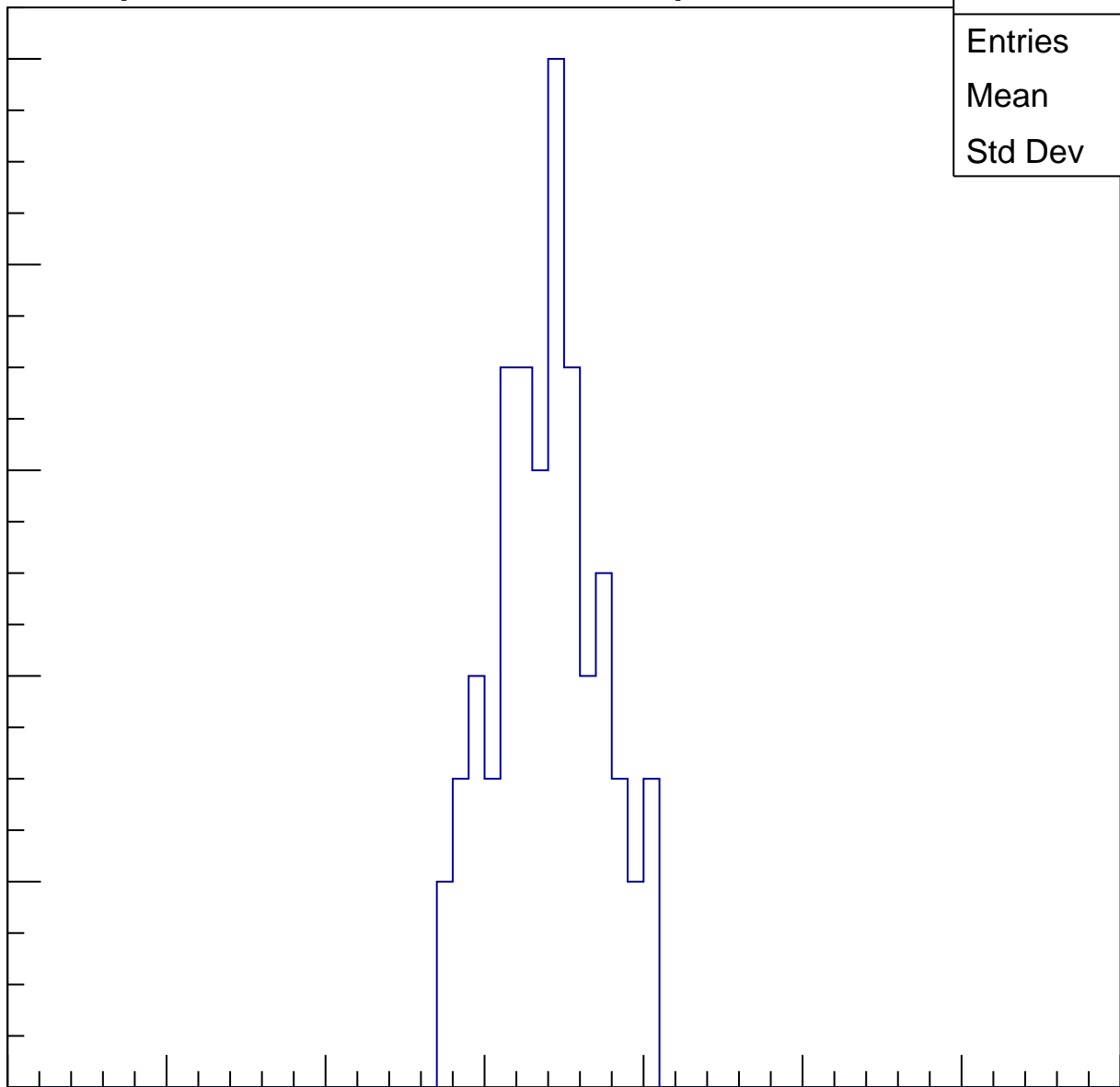
Entries	66
Mean	33.47
Std Dev	3.272

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl



B1L103S, U5-ch3, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	88
Mean	35.01
Std Dev	13.76

Entry

10

8

6

4

2

0

0

10

20

30

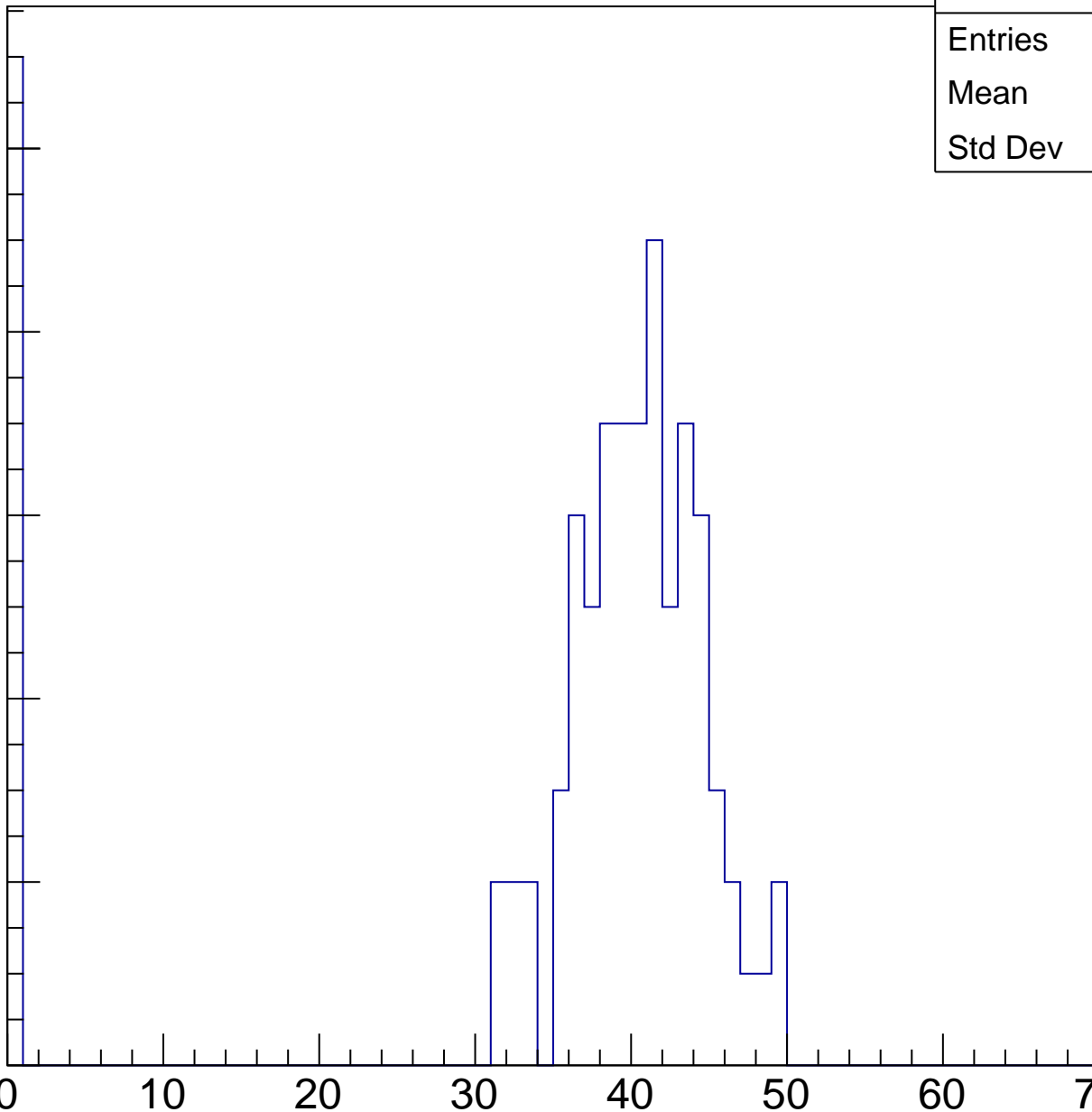
40

50

60

70

ampl

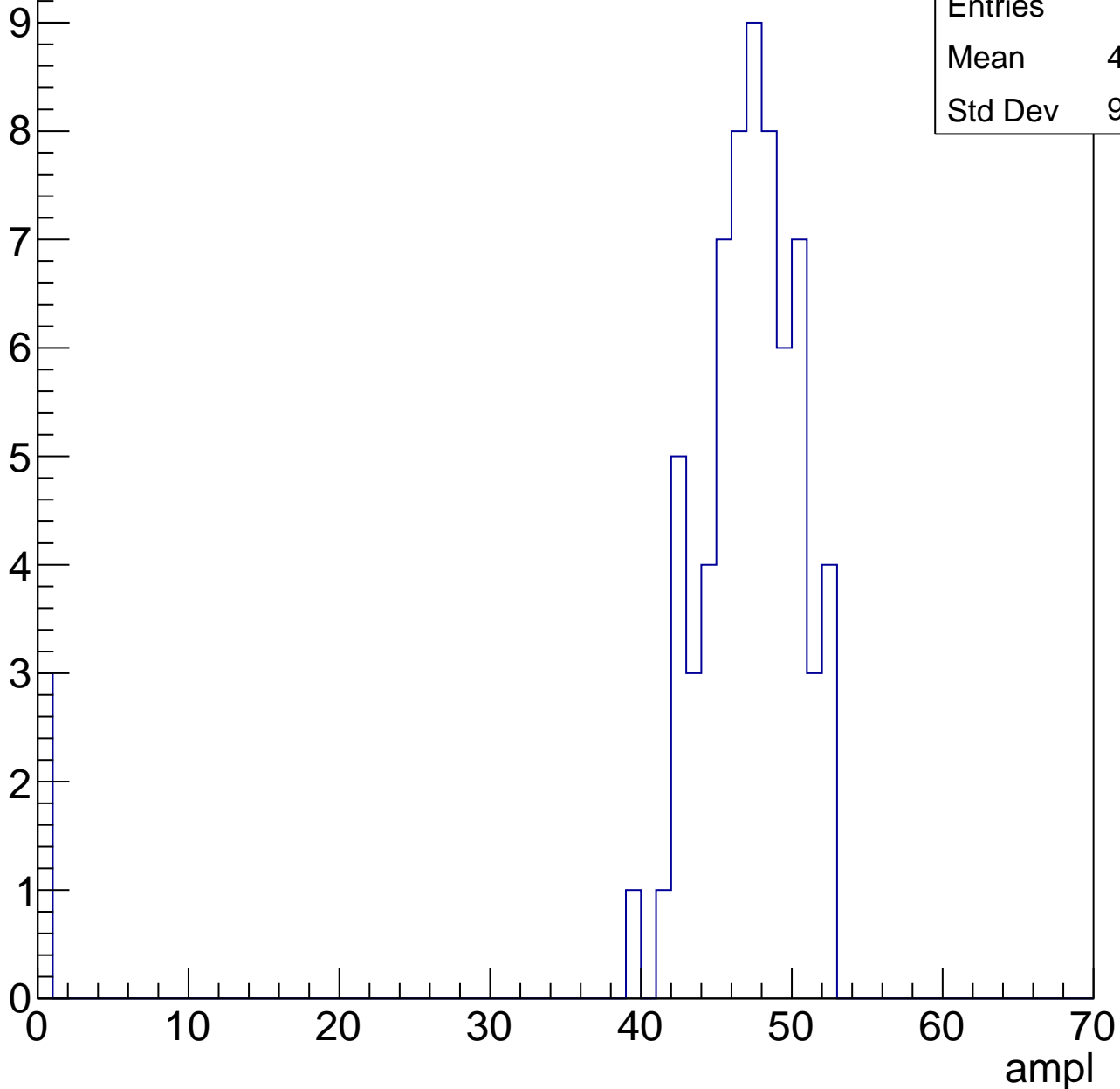


B1L103S, U5-ch3, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	44.78
Std Dev	9.982

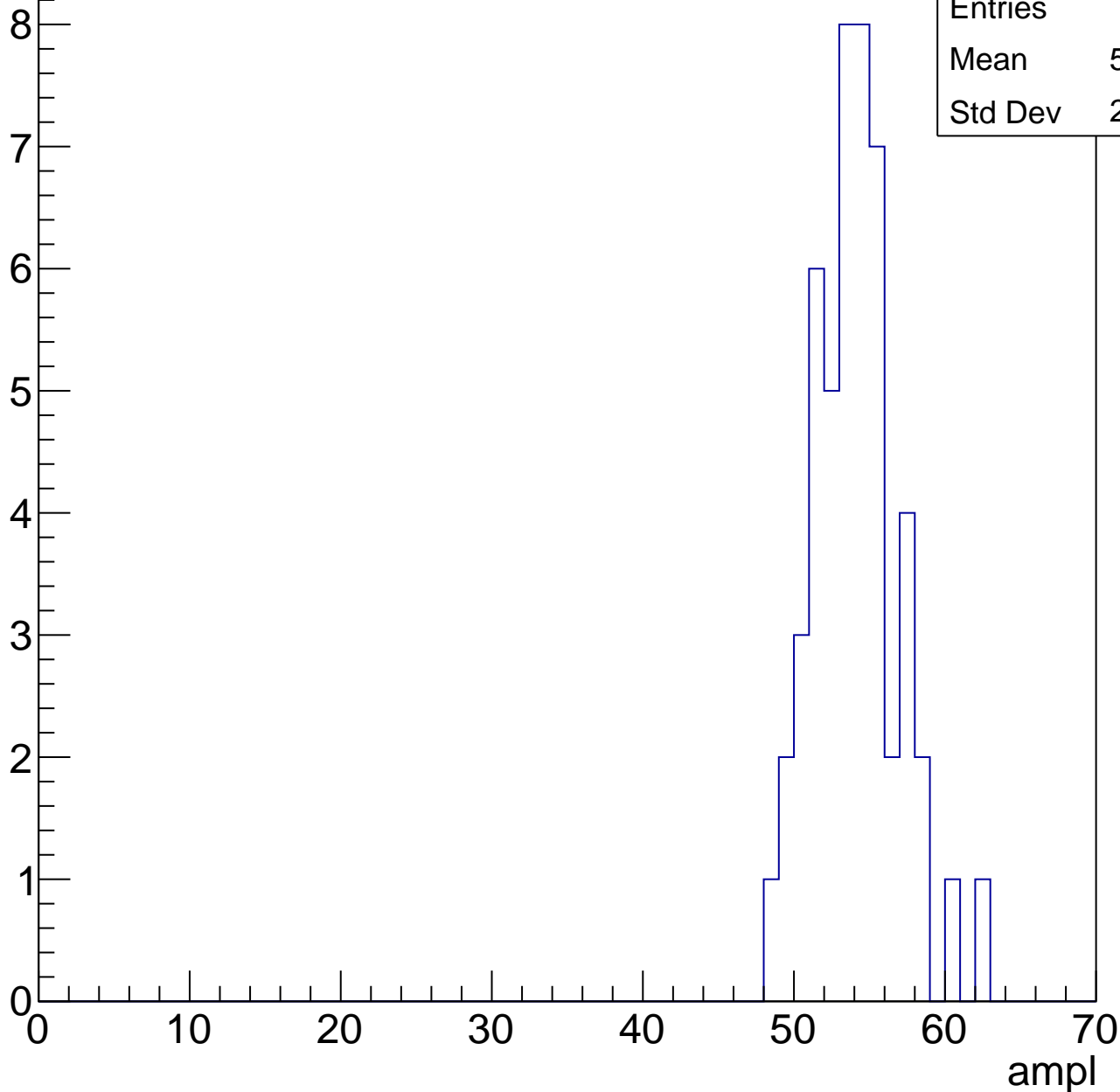


B1L103S, U5-ch3, adc4

calib_packv5_041523_1651.root, FC#0, port C2

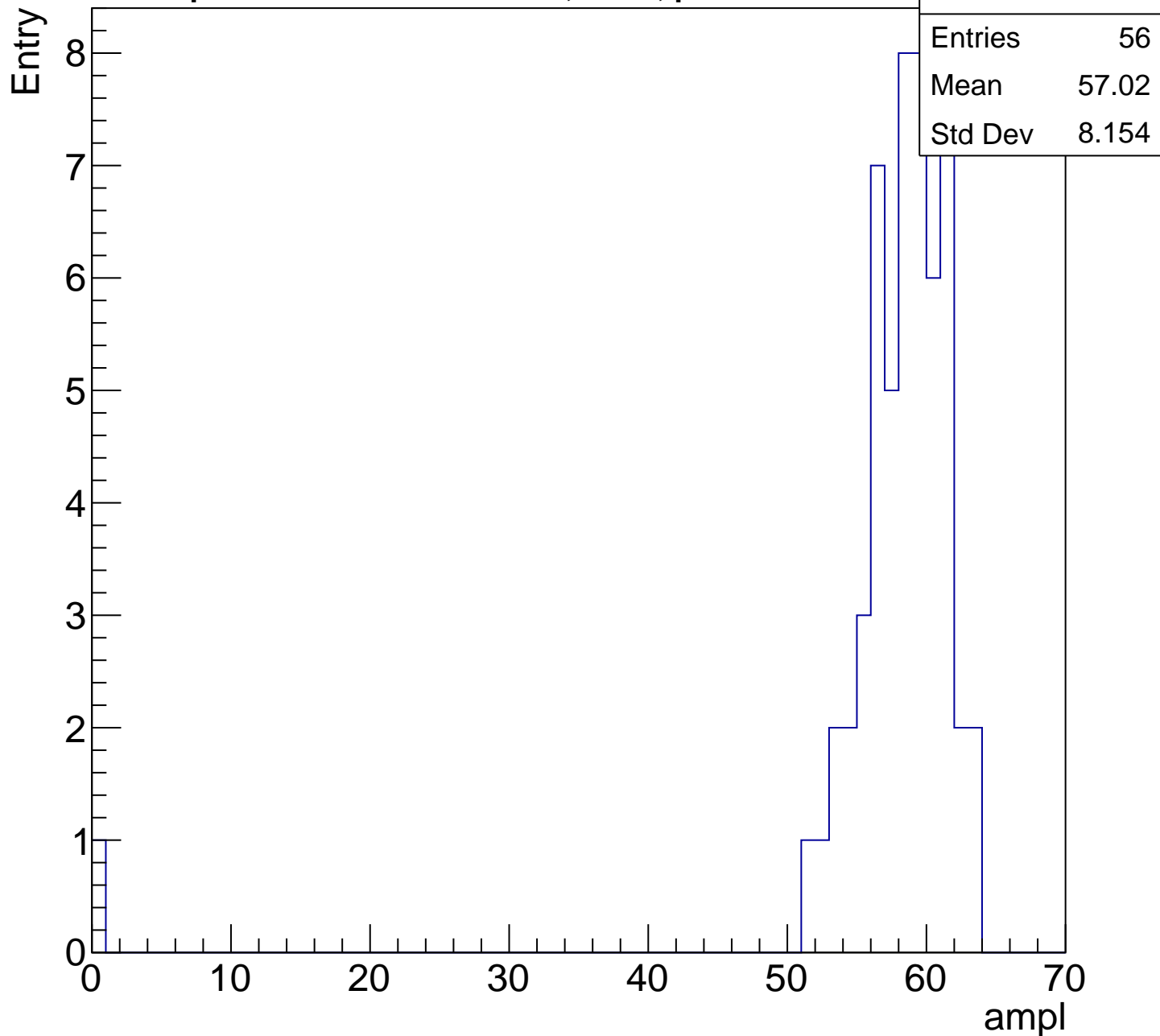
Entry

Entries	50
Mean	53.62
Std Dev	2.799



B1L103S, U5-ch3, adc5

calib_packv5_041523_1651.root, FC#0, port C2

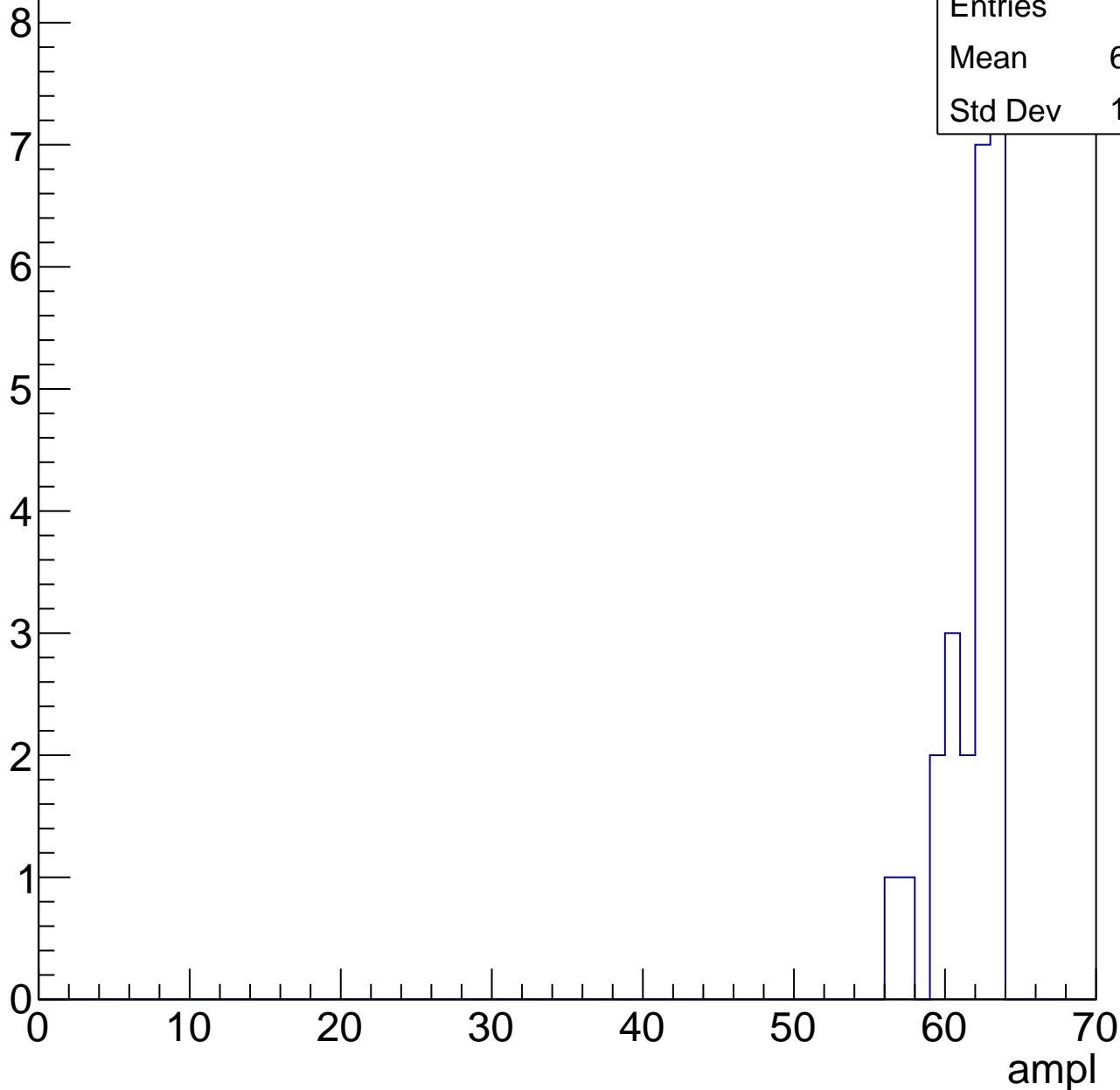


B1L103S, U5-ch3, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

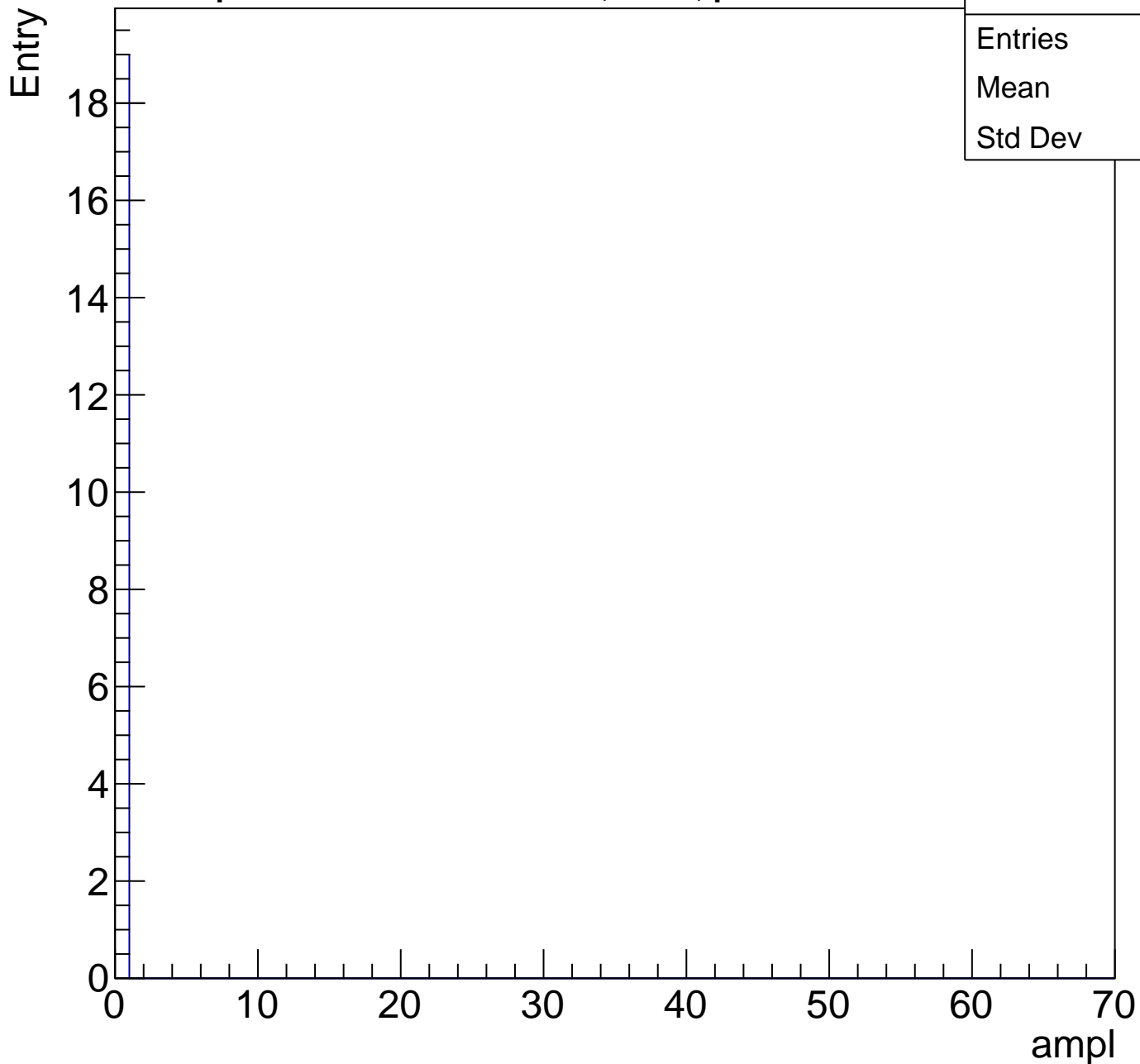
Entries	24
Mean	61.29
Std Dev	1.925



B1L103S, U5-ch3, adc7

calib_packv5_041523_1651.root, FC#0, port C2

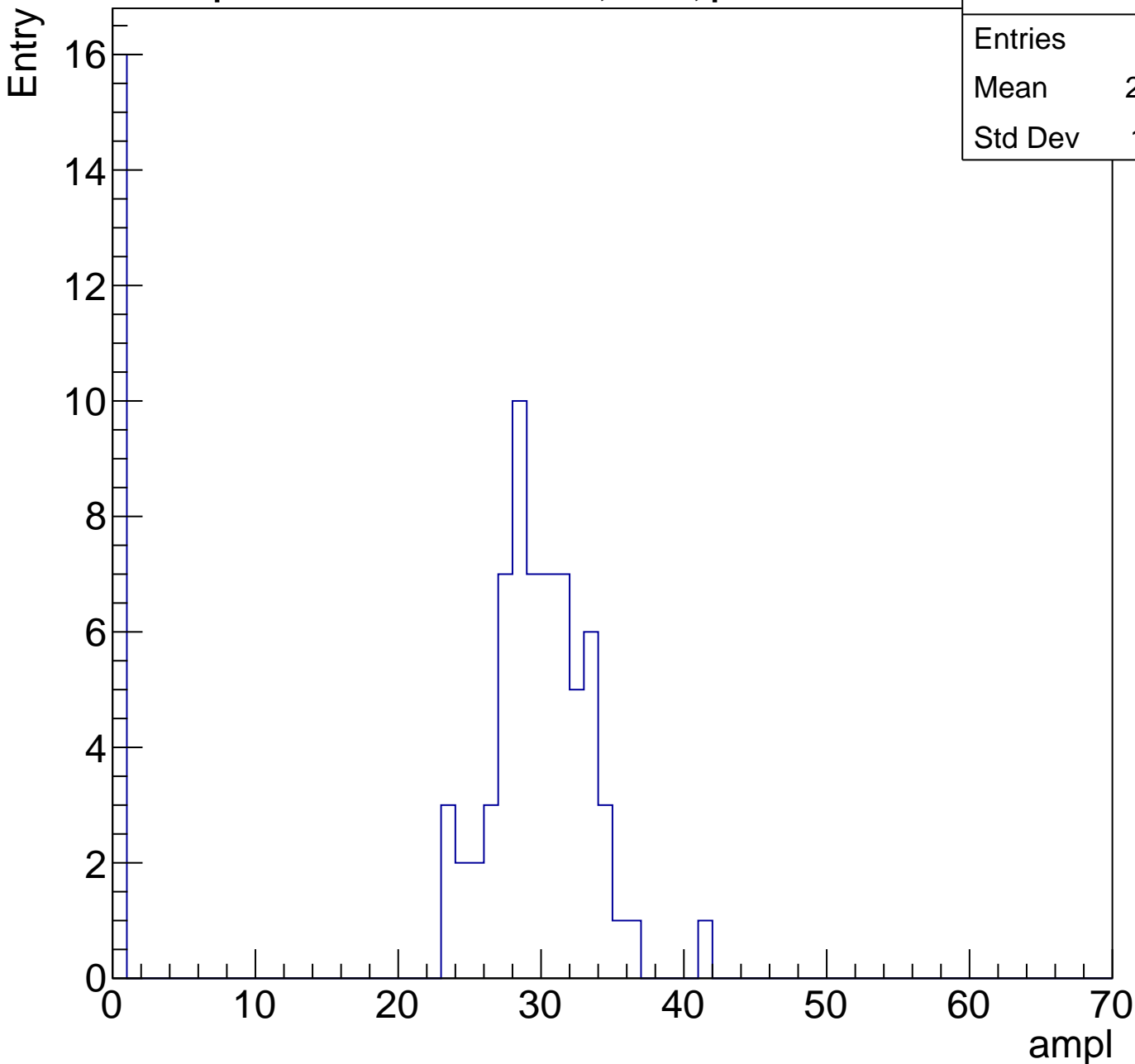
Entries	19
Mean	0
Std Dev	0



B1L103S, U5-ch4, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	23.65
Std Dev	12.11

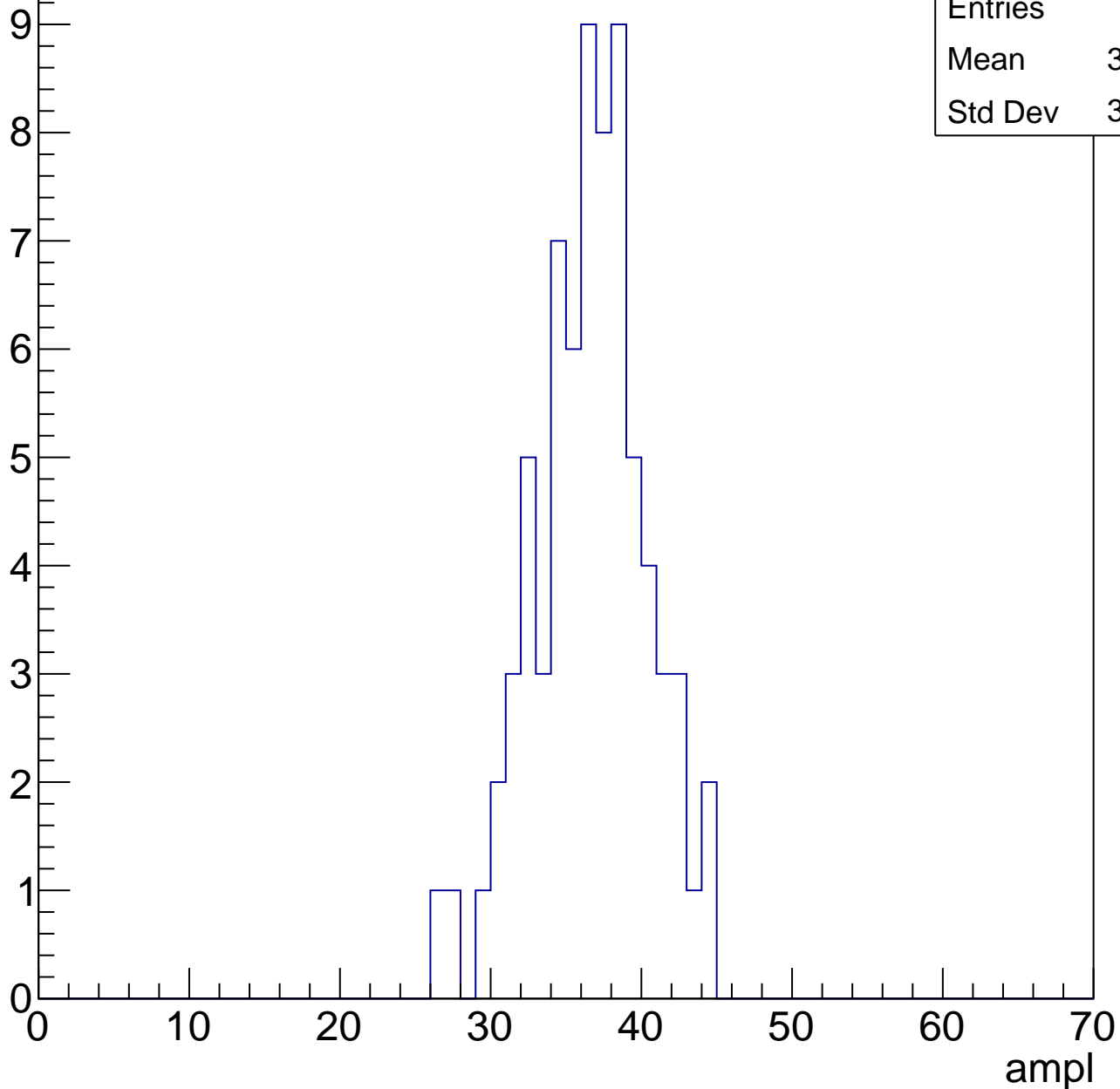


B1L103S, U5-ch4, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	36.15
Std Dev	3.755



B1L103S, U5-ch4, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	73
Mean	36
Std Dev	15.51

Entry

10

8

6

4

2

0

0

10

20

30

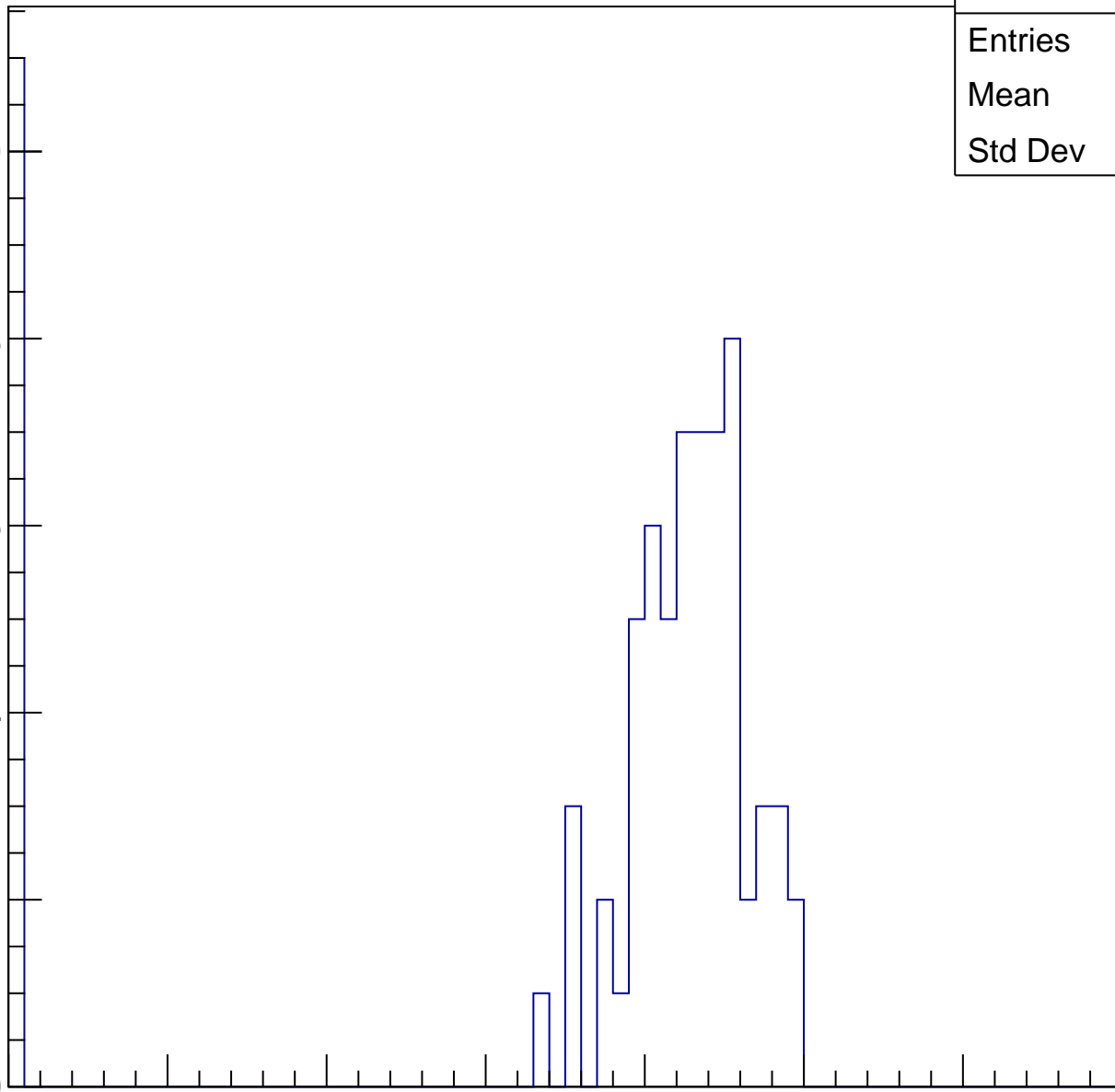
40

50

60

70

ampl

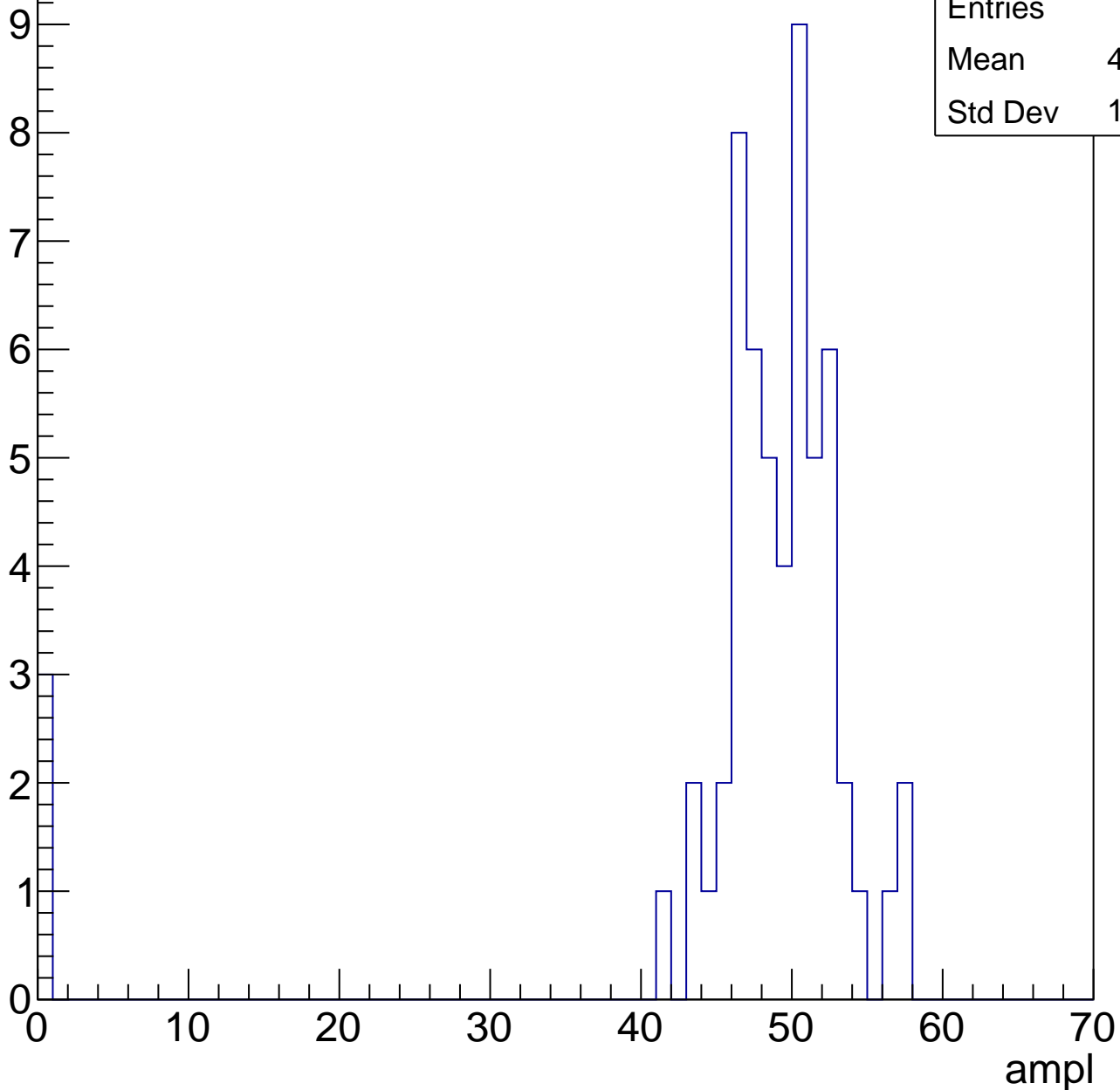


B1L103S, U5-ch4, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

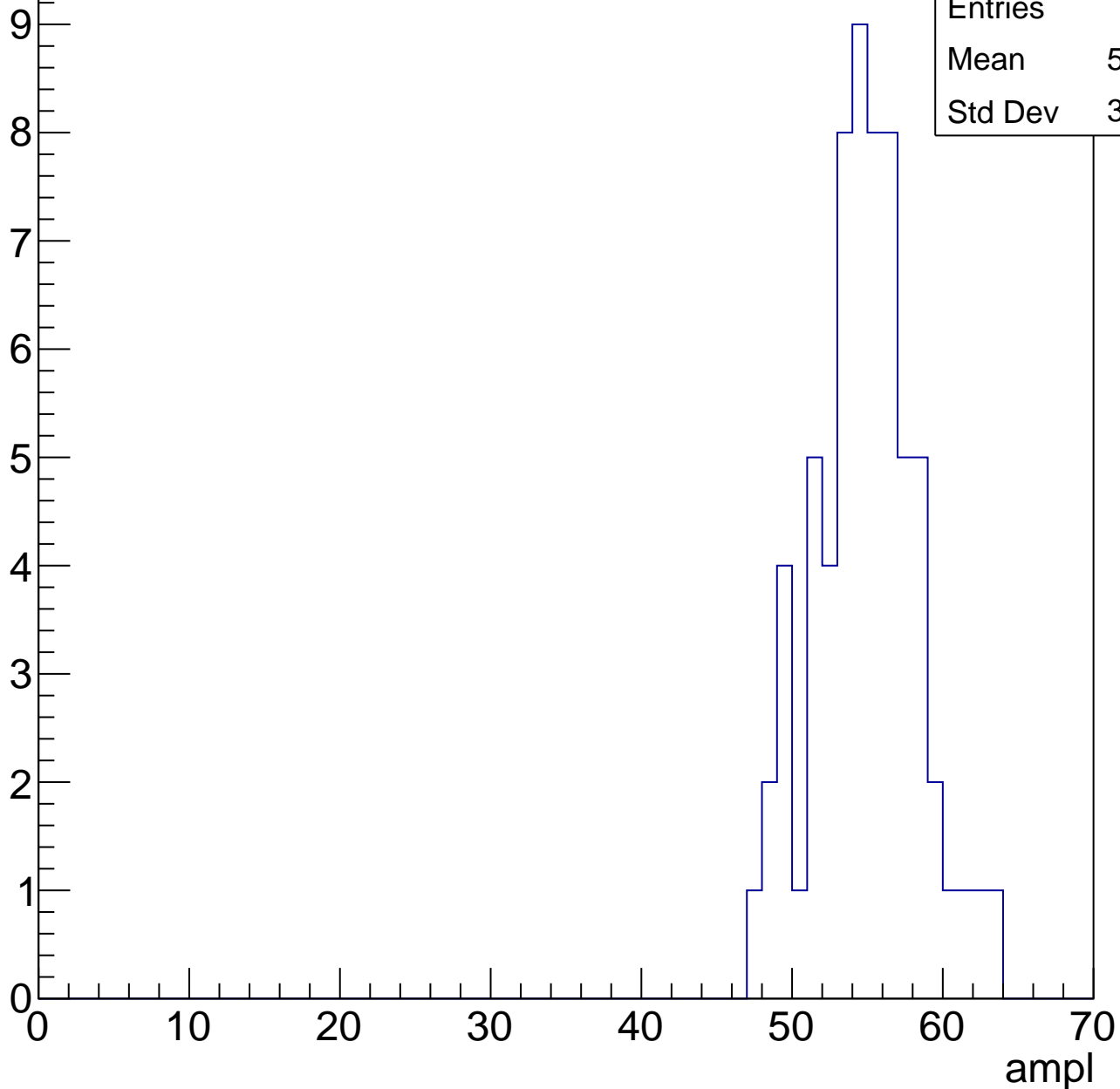
Entries	58
Mean	46.45
Std Dev	11.32



B1L103S, U5-ch4, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

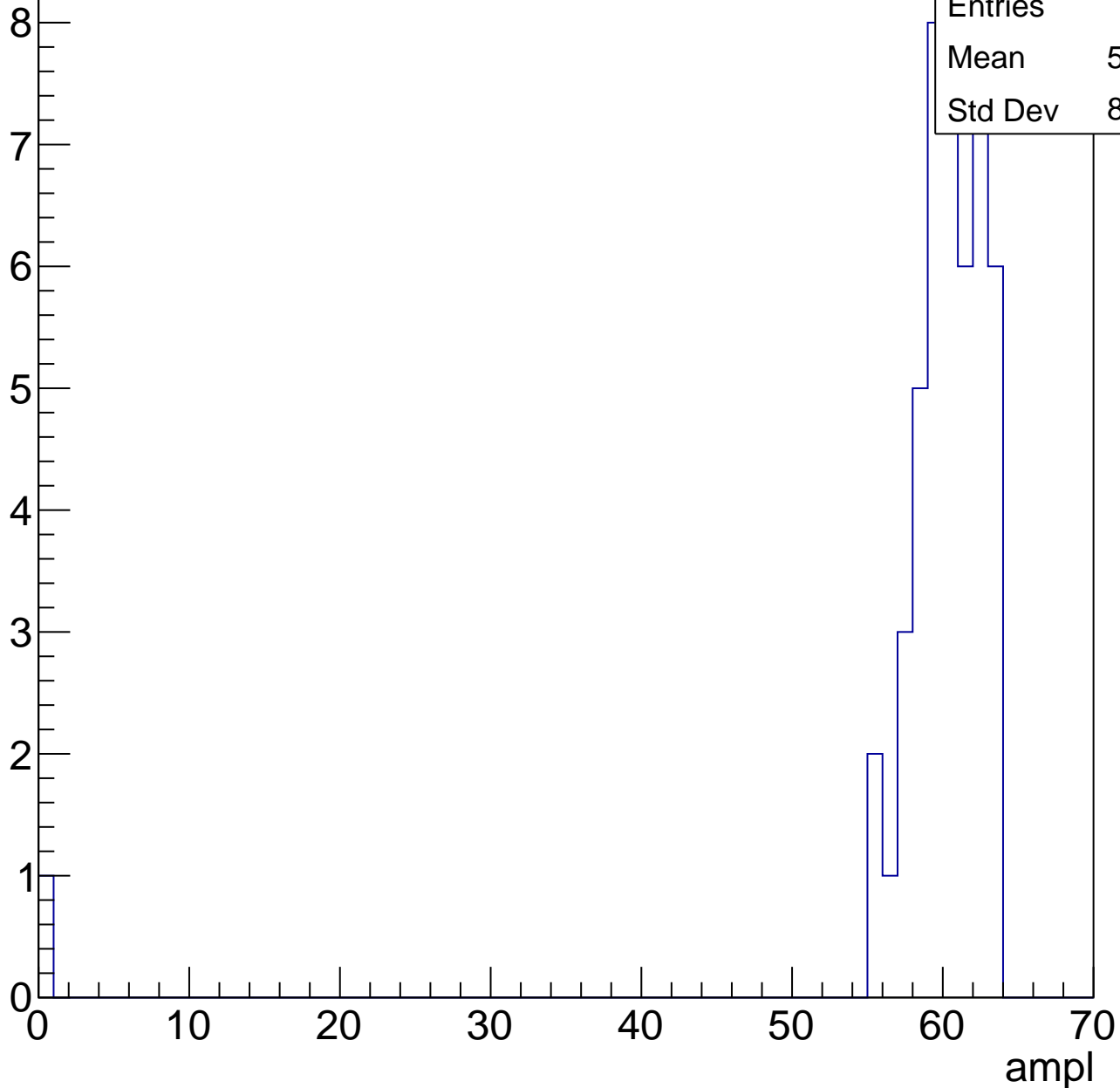


B1L103S, U5-ch4, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

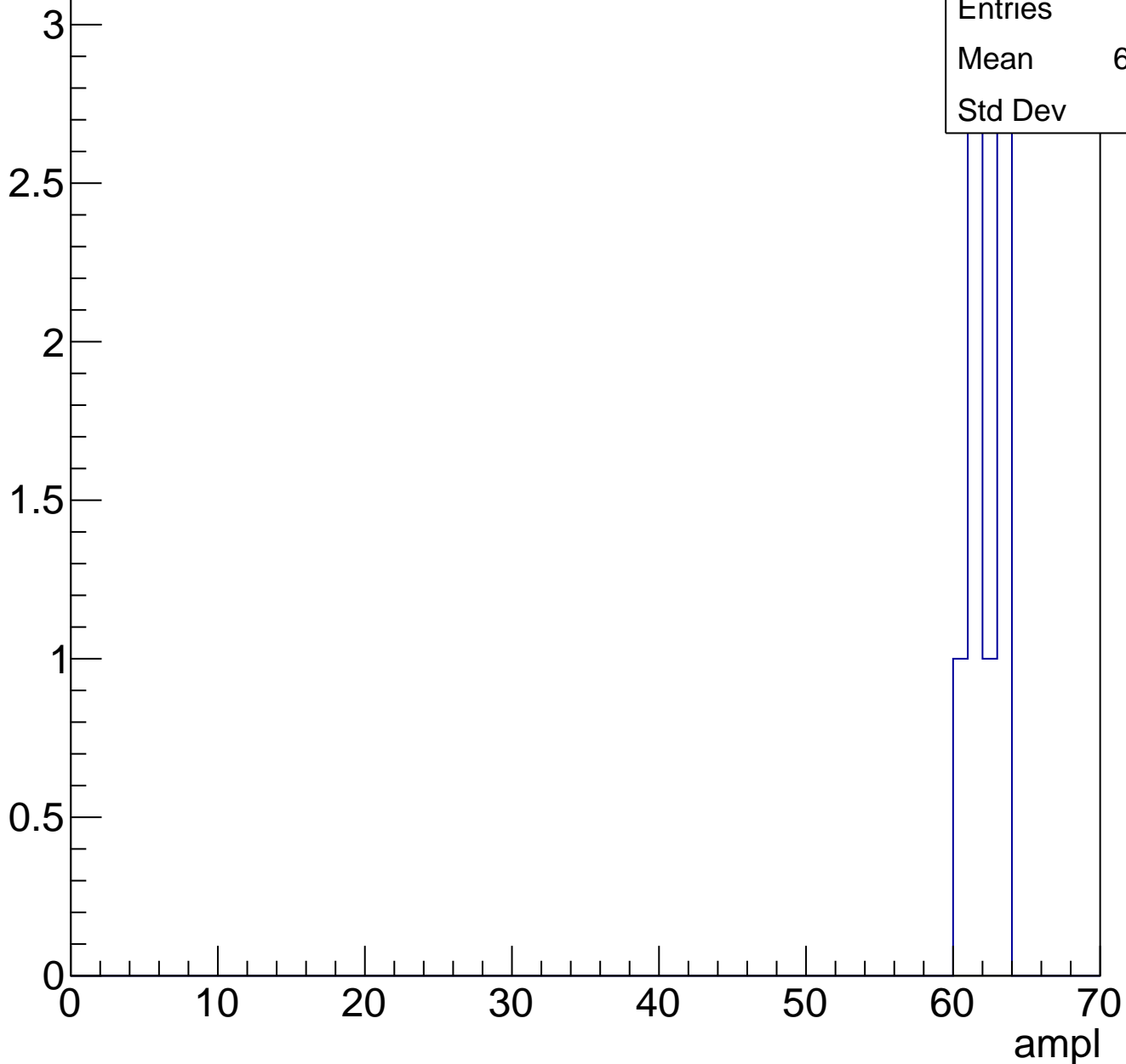
Entries	48
Mean	58.73
Std Dev	8.822



B1L103S, U5-ch4, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch4, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	0
Std Dev	0



B1L103S, U5-ch5, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	25.07
Std Dev	10.42

Entry

10

8

6

4

2

0

0

10

20

30

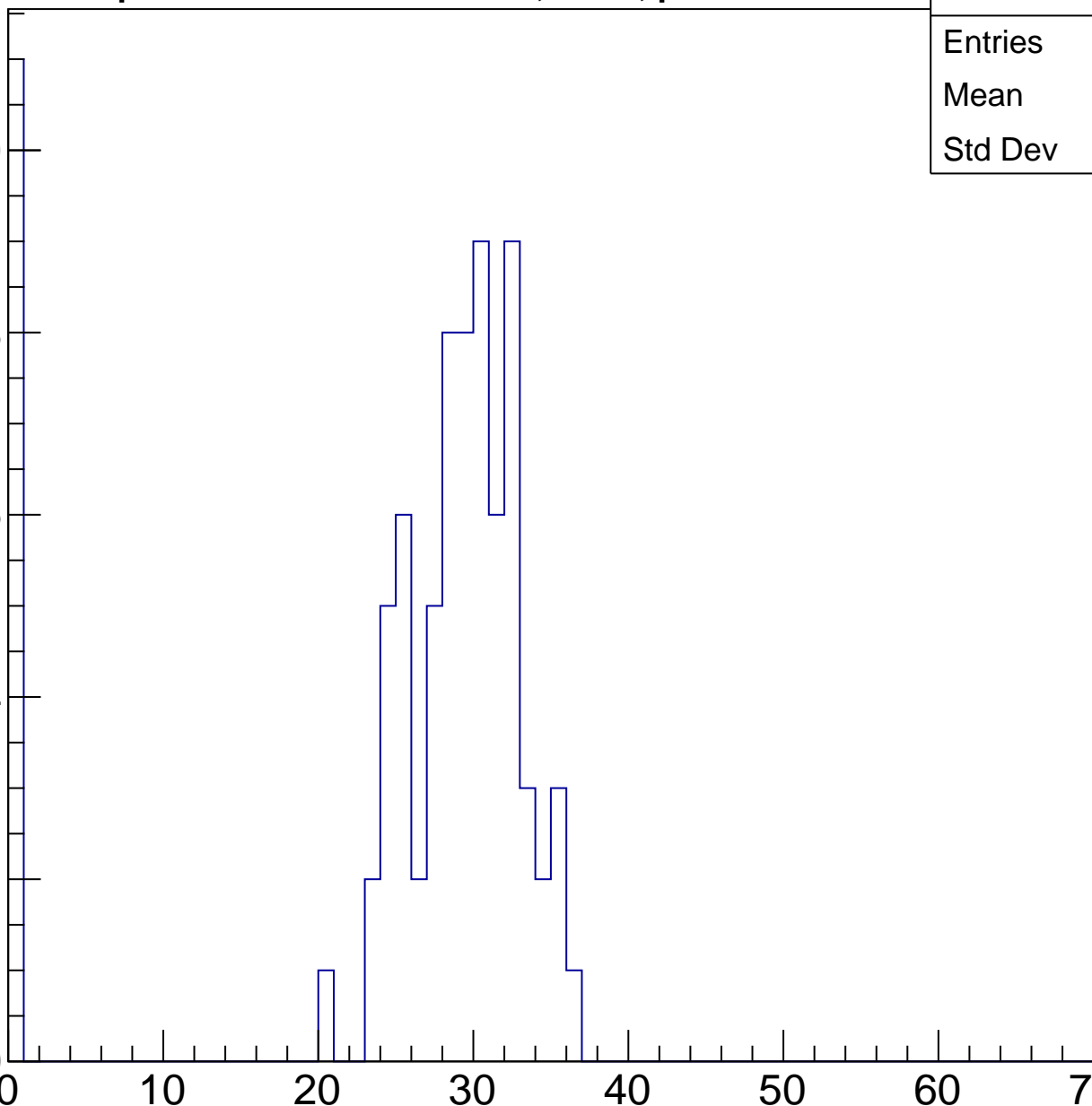
40

50

60

70

ampl

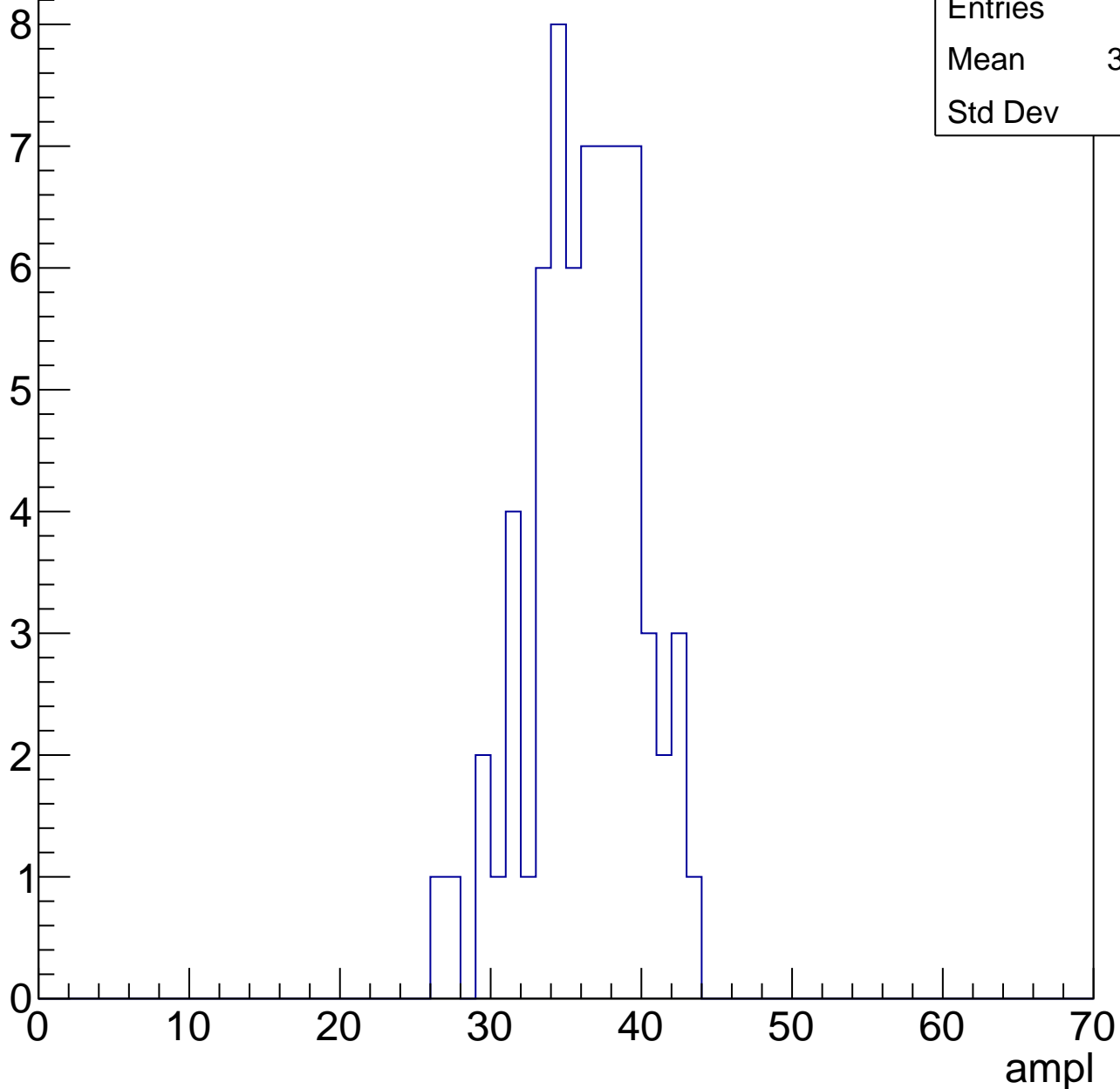


B1L103S, U5-ch5, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

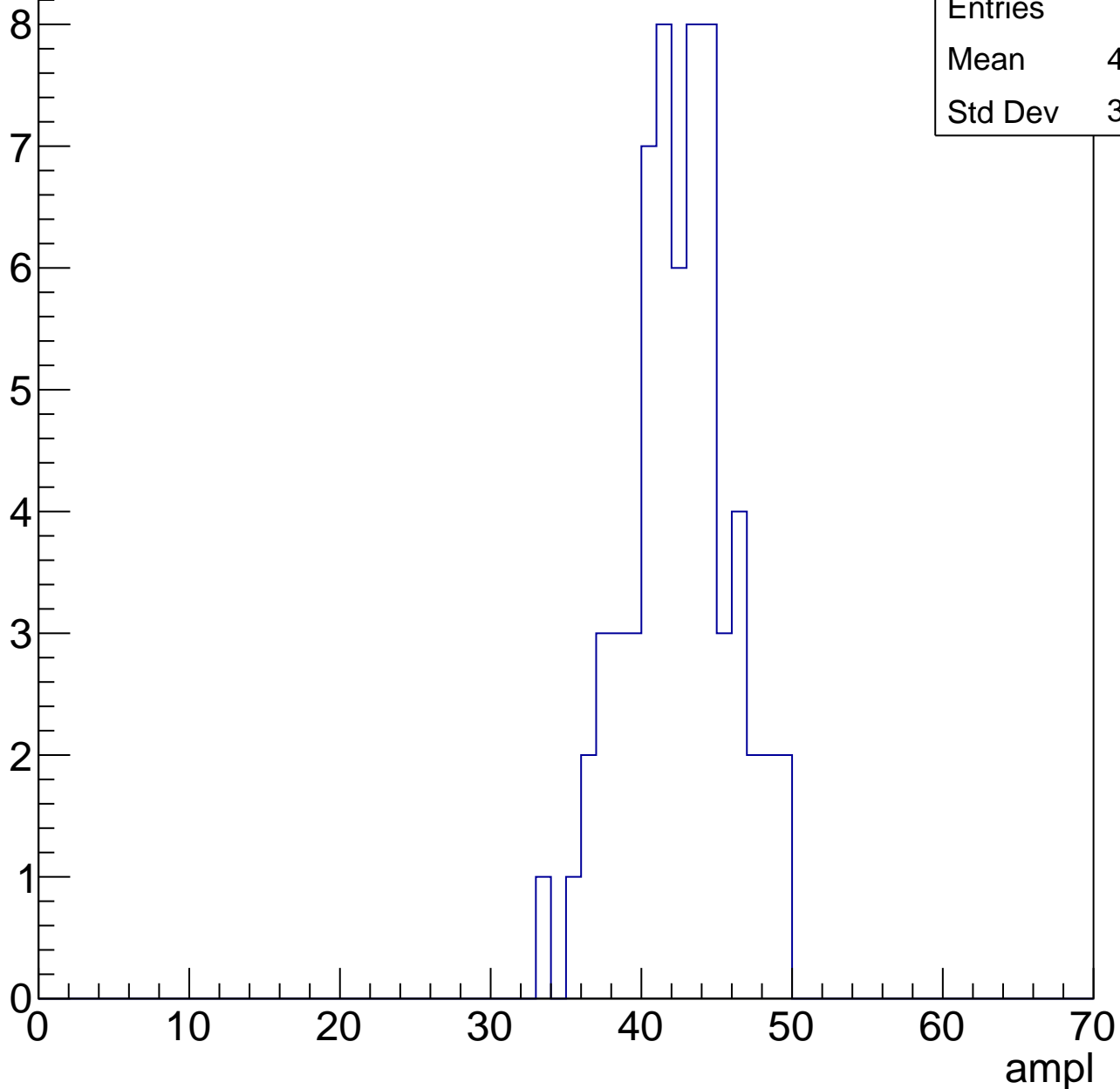
Entries	67
Mean	35.79
Std Dev	3.61



B1L103S, U5-ch5, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry



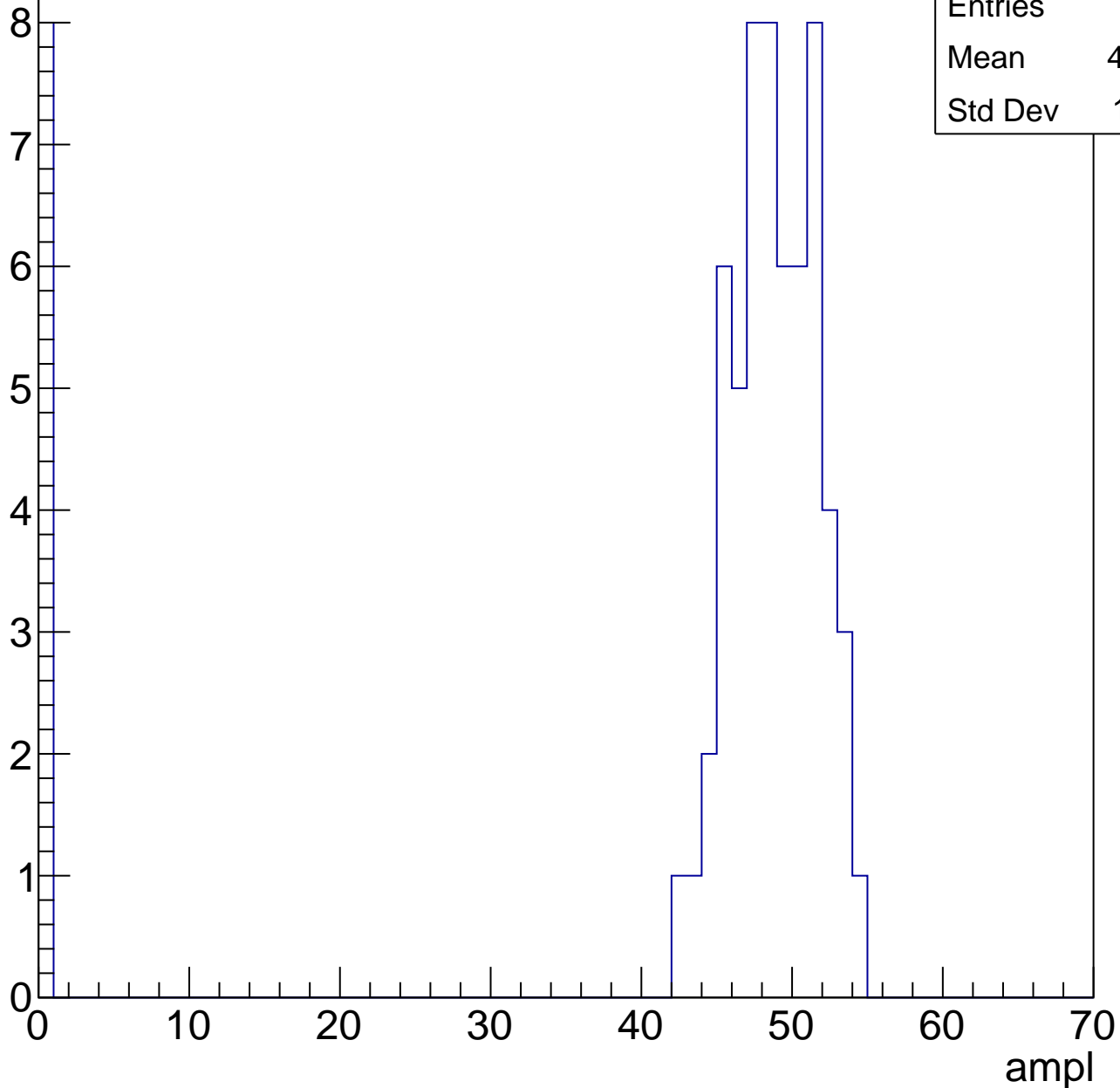
Entries	63
Mean	41.98
Std Dev	3.425

B1L103S, U5-ch5, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	42.63
Std Dev	15.91



B1L103S, U5-ch5, adc4

calib_packv5_041523_1651.root, FC#0, port C2

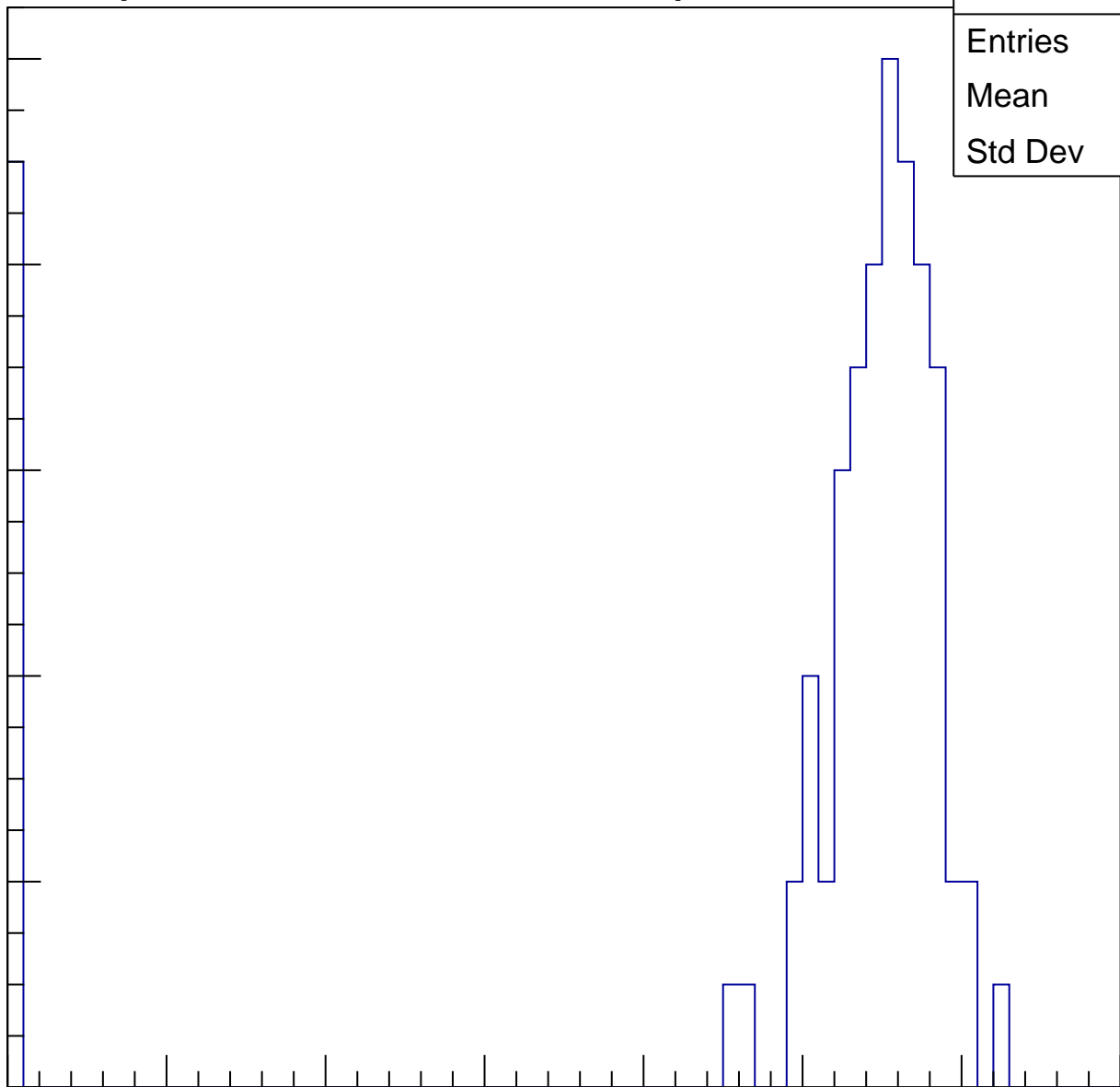
Entries	79
Mean	48.38
Std Dev	17.6

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

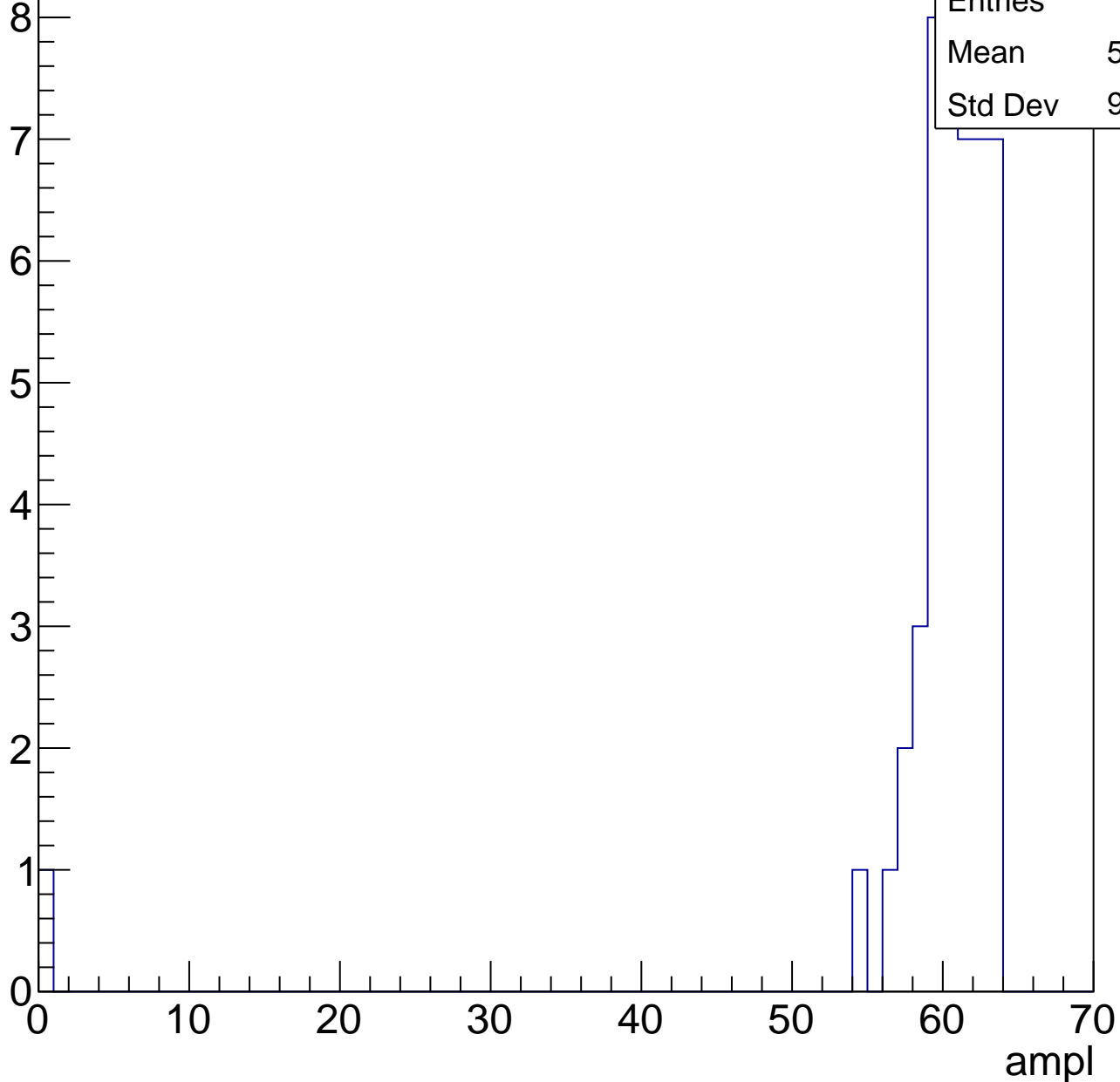


B1L103S, U5-ch5, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

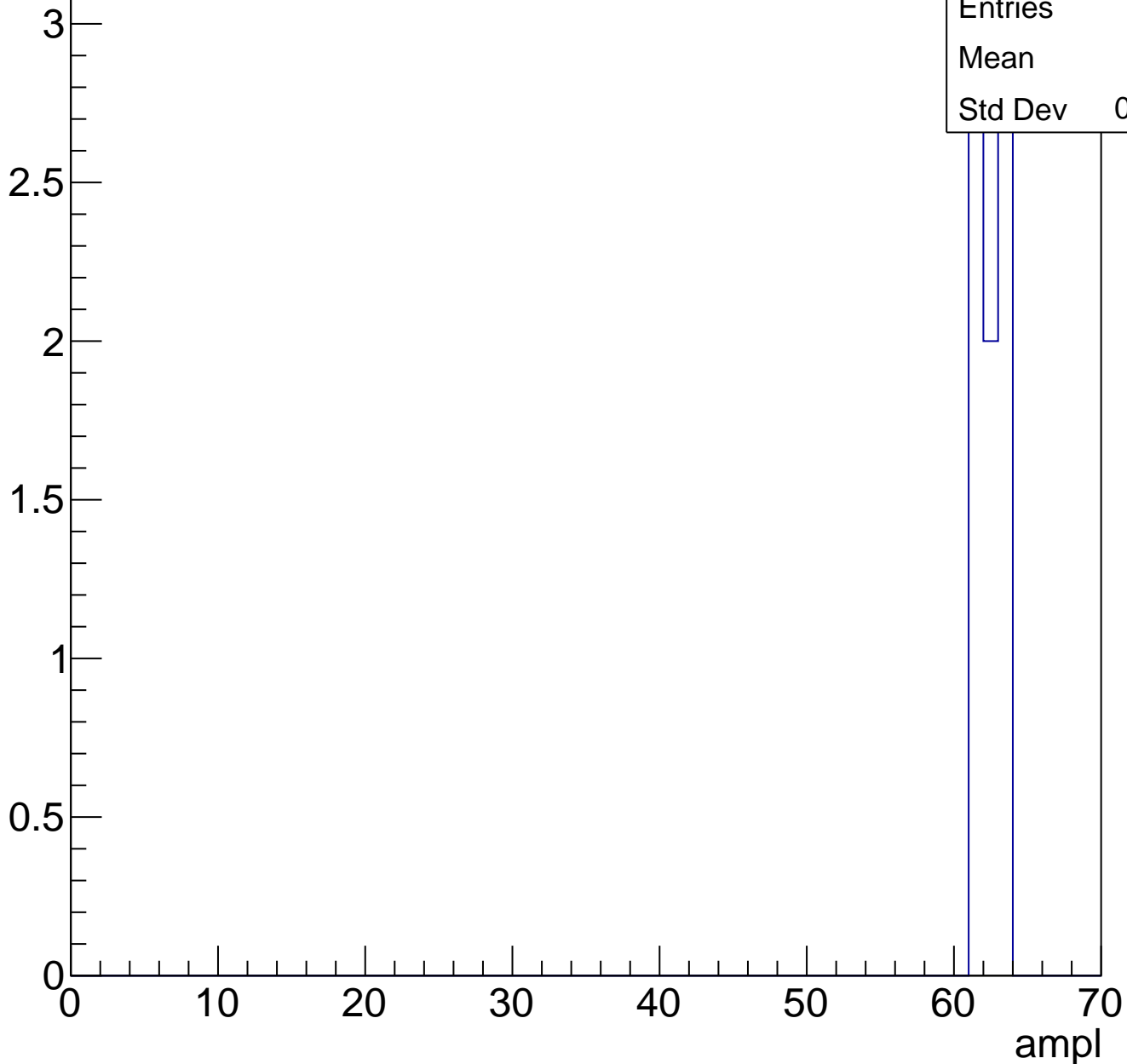
Entries	45
Mean	58.93
Std Dev	9.113



B1L103S, U5-ch5, adc6

calib_packv5_041523_1651.root, FC#0, port C2

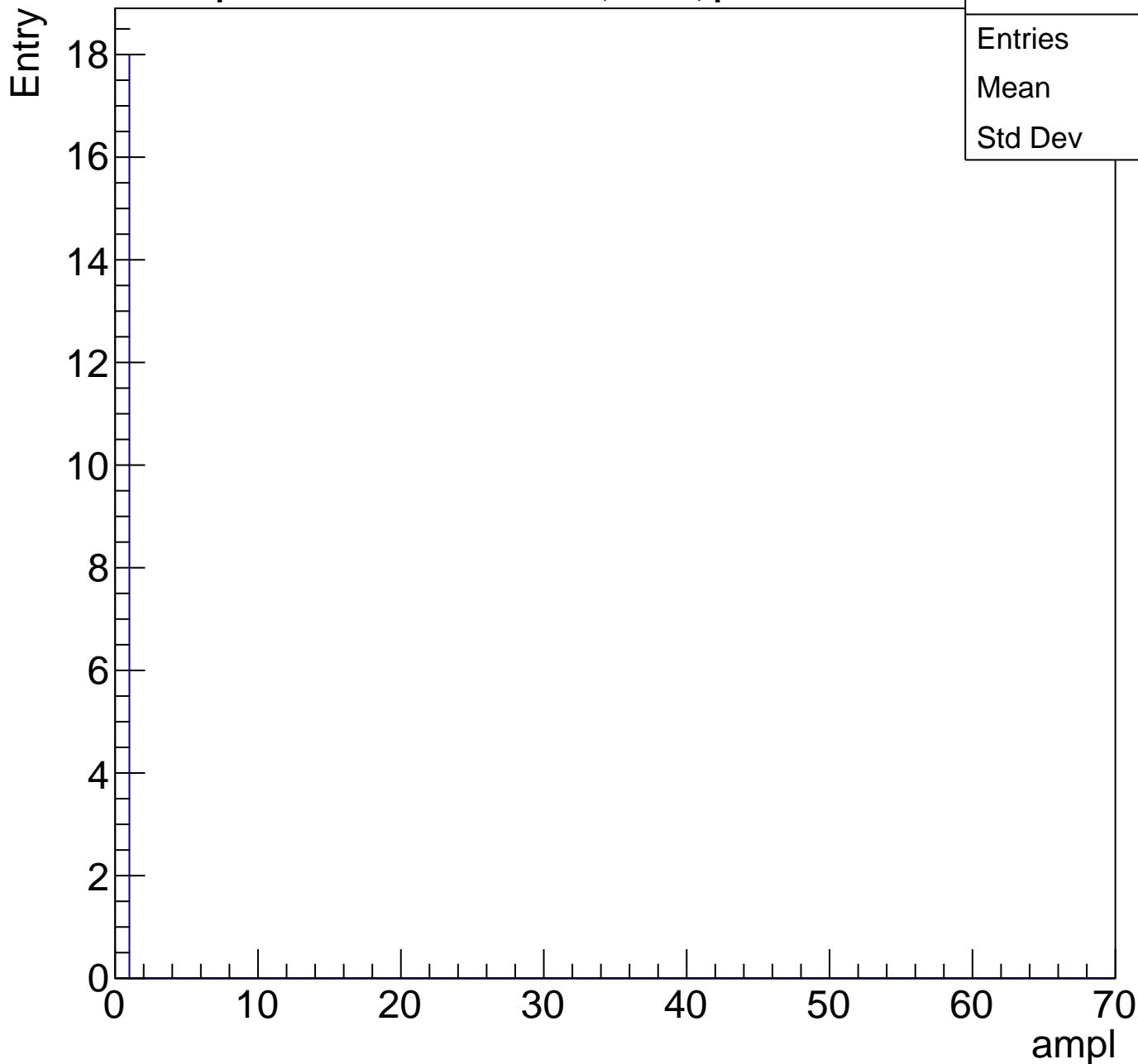
Entry



B1L103S, U5-ch5, adc7

calib_packv5_041523_1651.root, FC#0, port C2

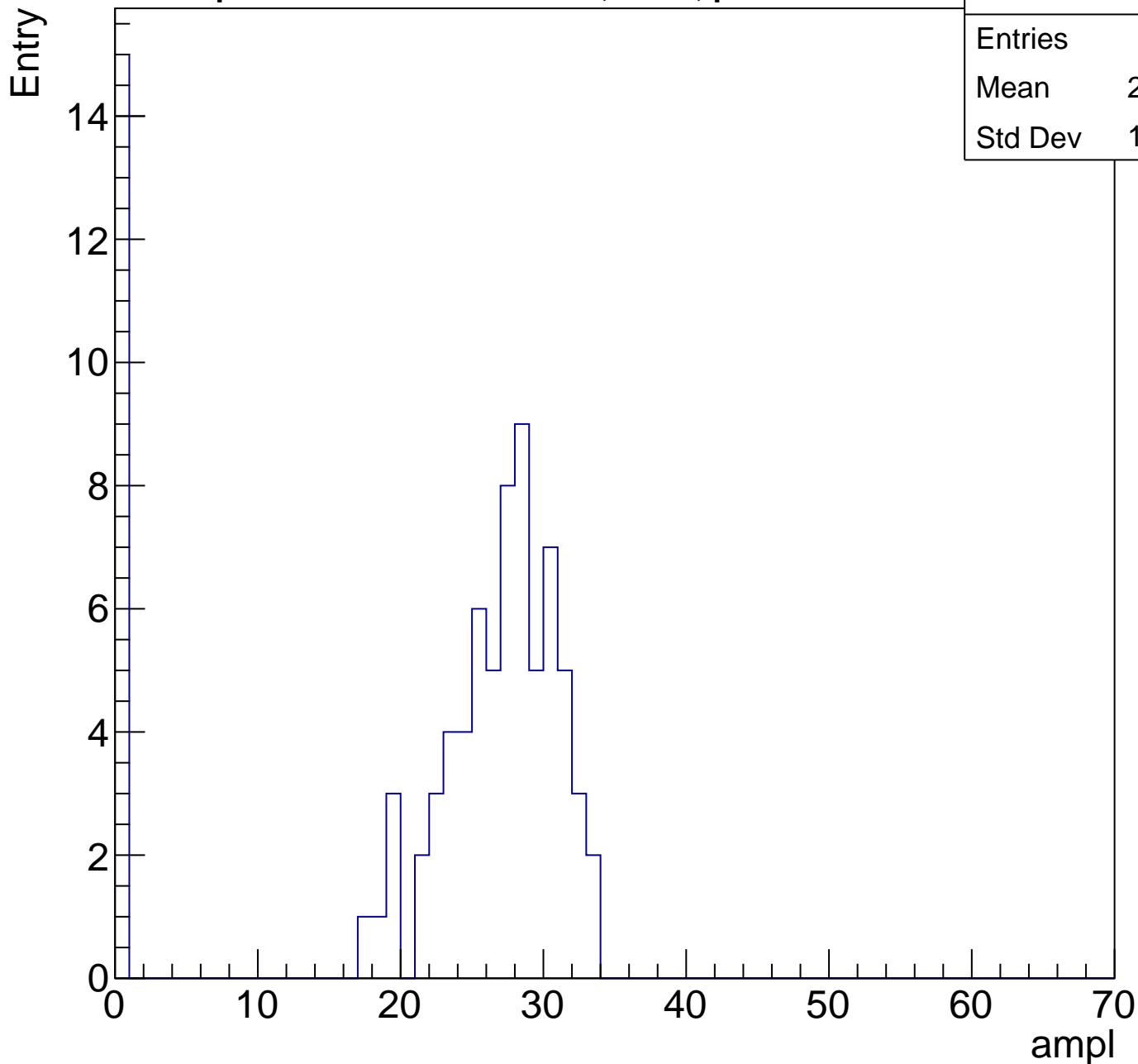
Entries	18
Mean	0
Std Dev	0



B1L103S, U5-ch6, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	83
Mean	21.78
Std Dev	10.78

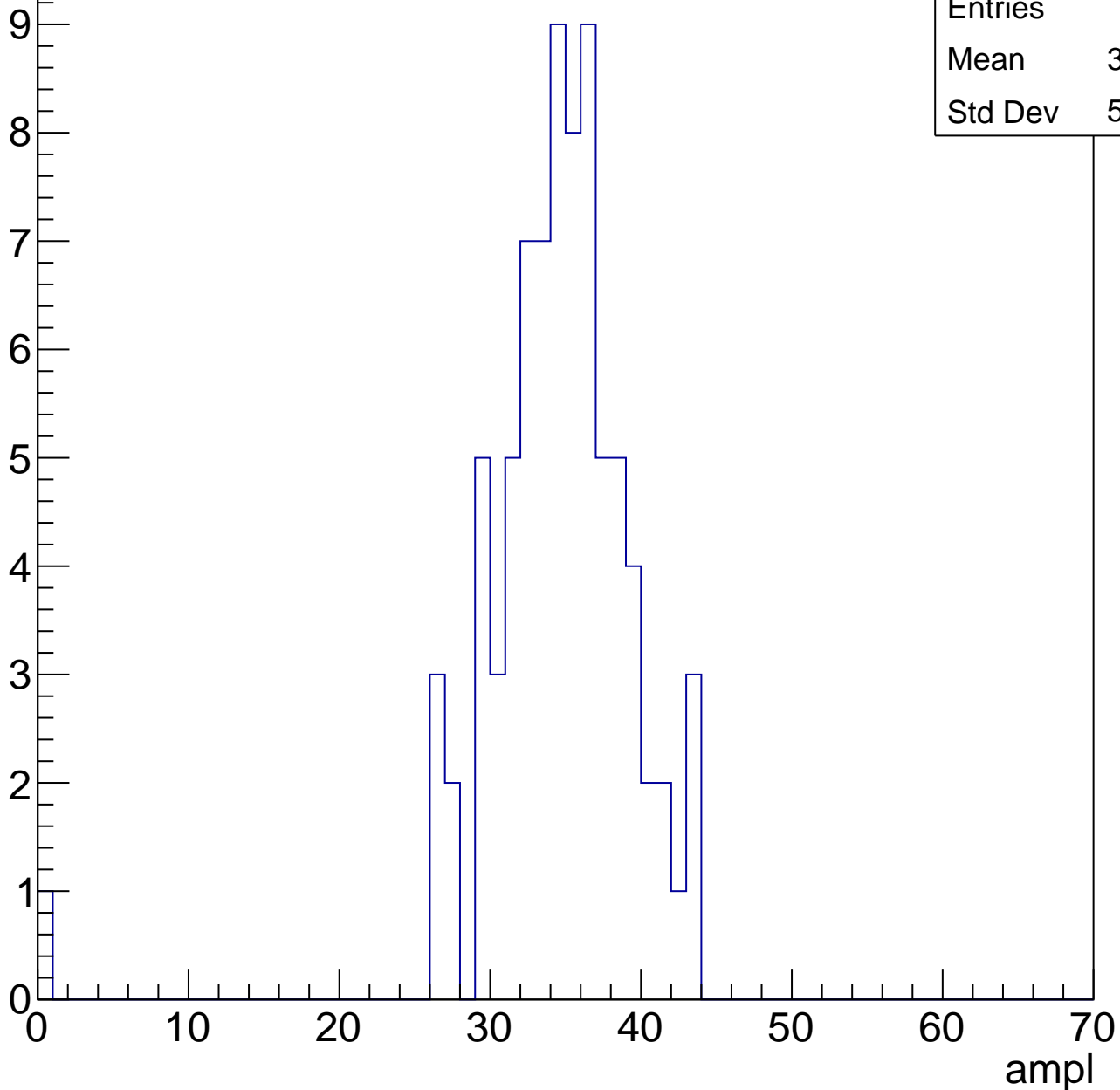


B1L103S, U5-ch6, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	81
Mean	33.96
Std Dev	5.494



B1L103S, U5-ch6, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	68
Mean	32.85
Std Dev	16.25

Entry

12

10

8

6

4

2

0

0

10

20

30

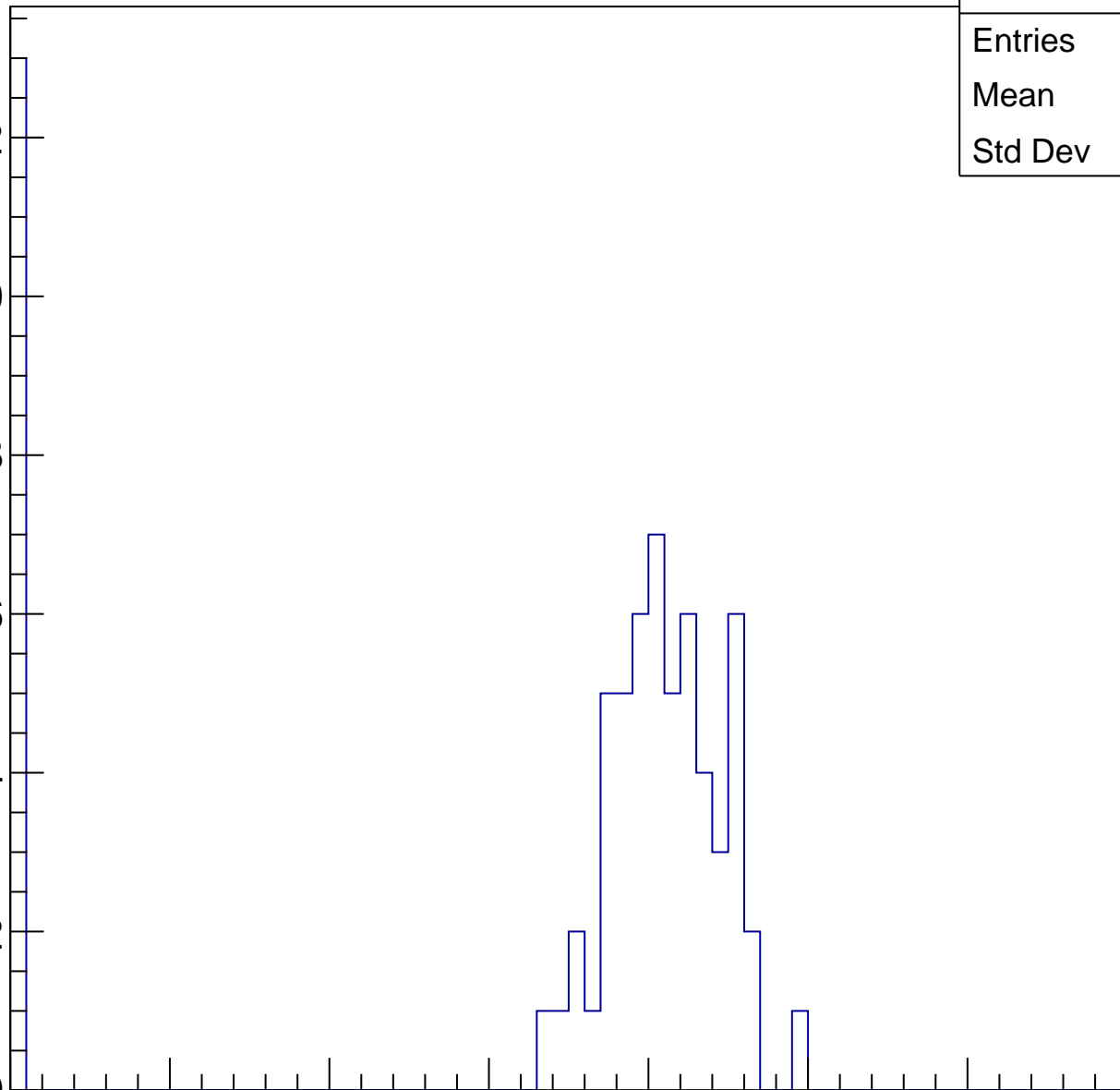
40

50

60

70

ampl

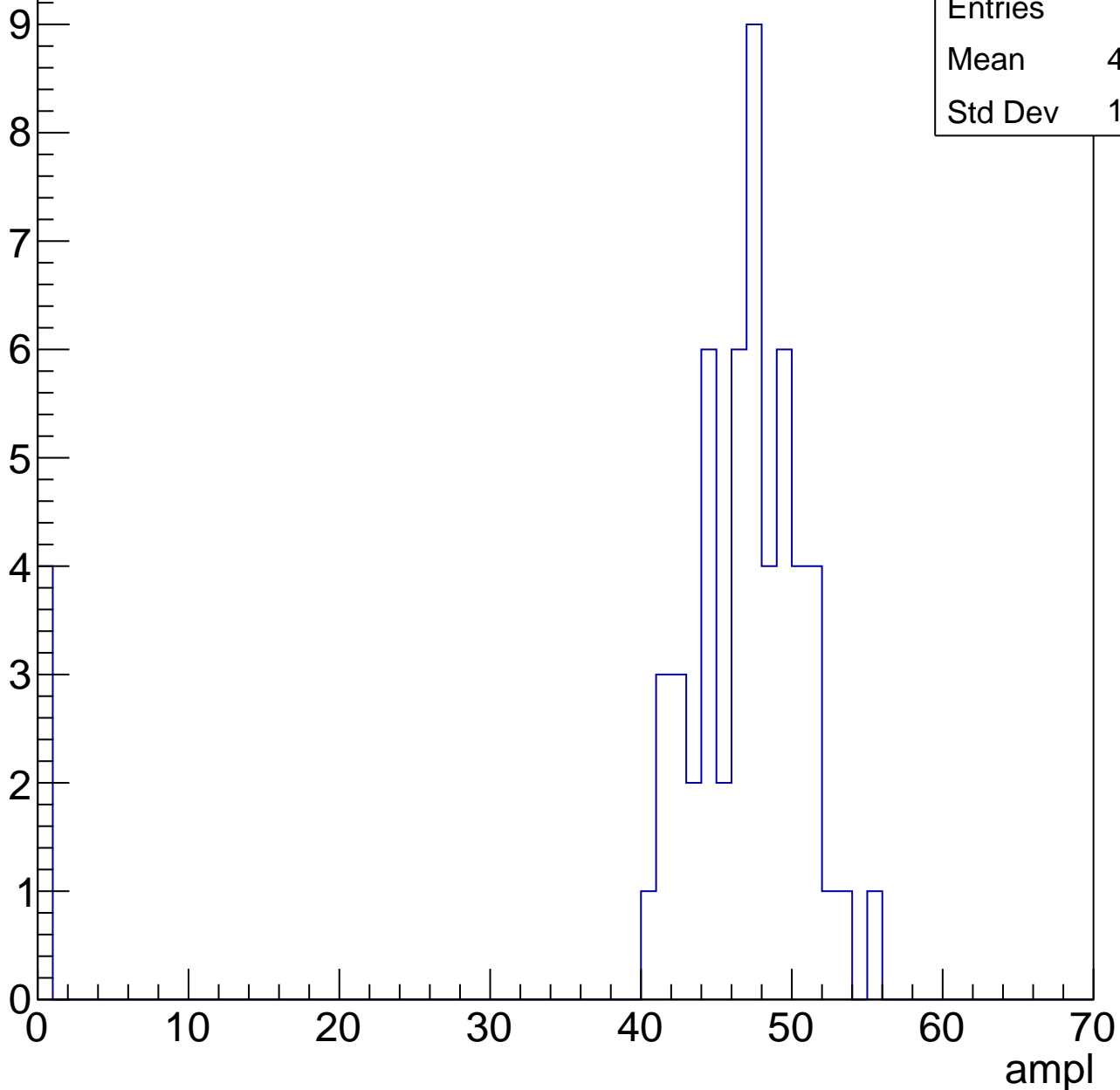


B1L103S, U5-ch6, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	43.47
Std Dev	12.36

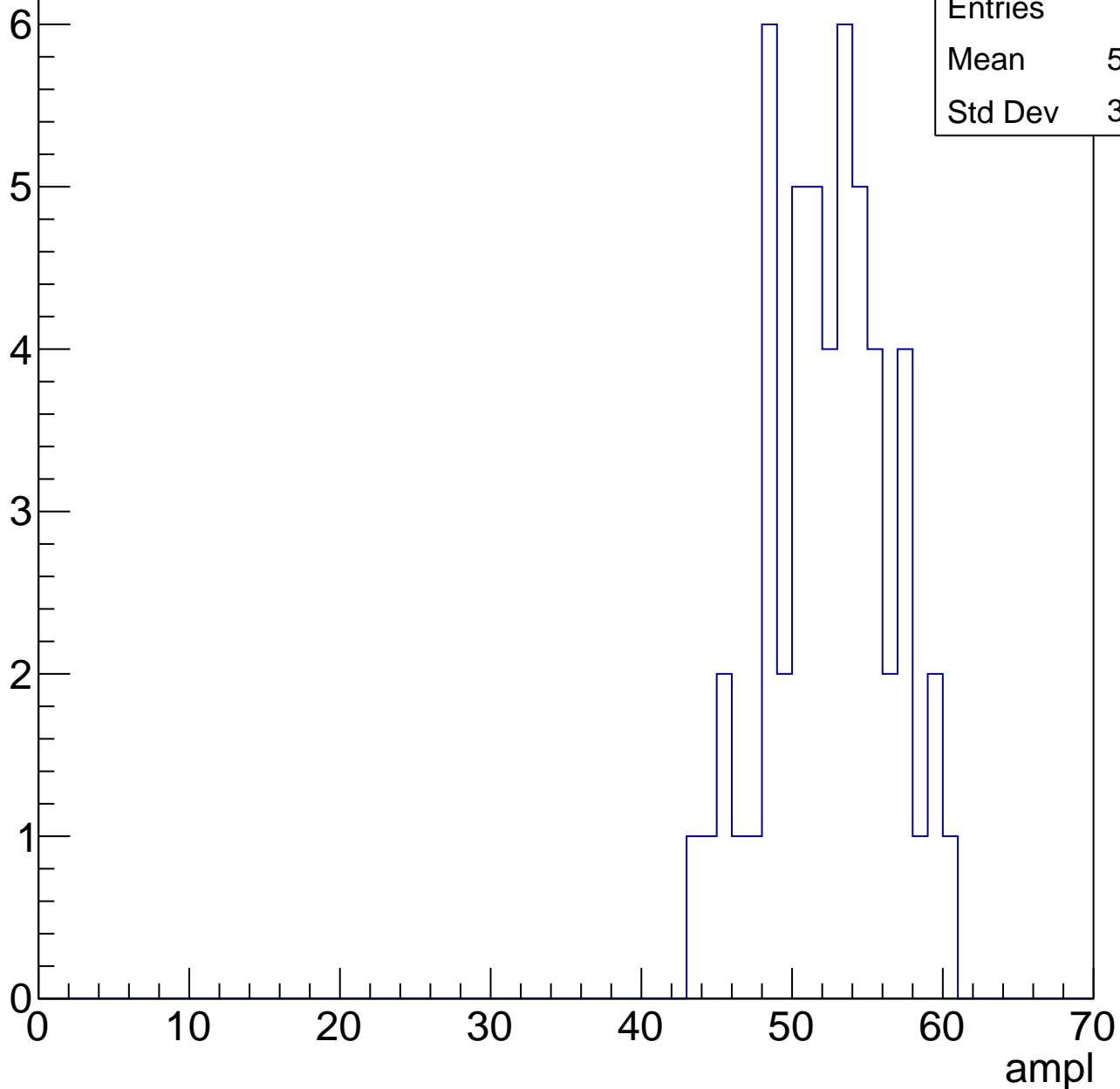


B1L103S, U5-ch6, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	51.94
Std Dev	3.969

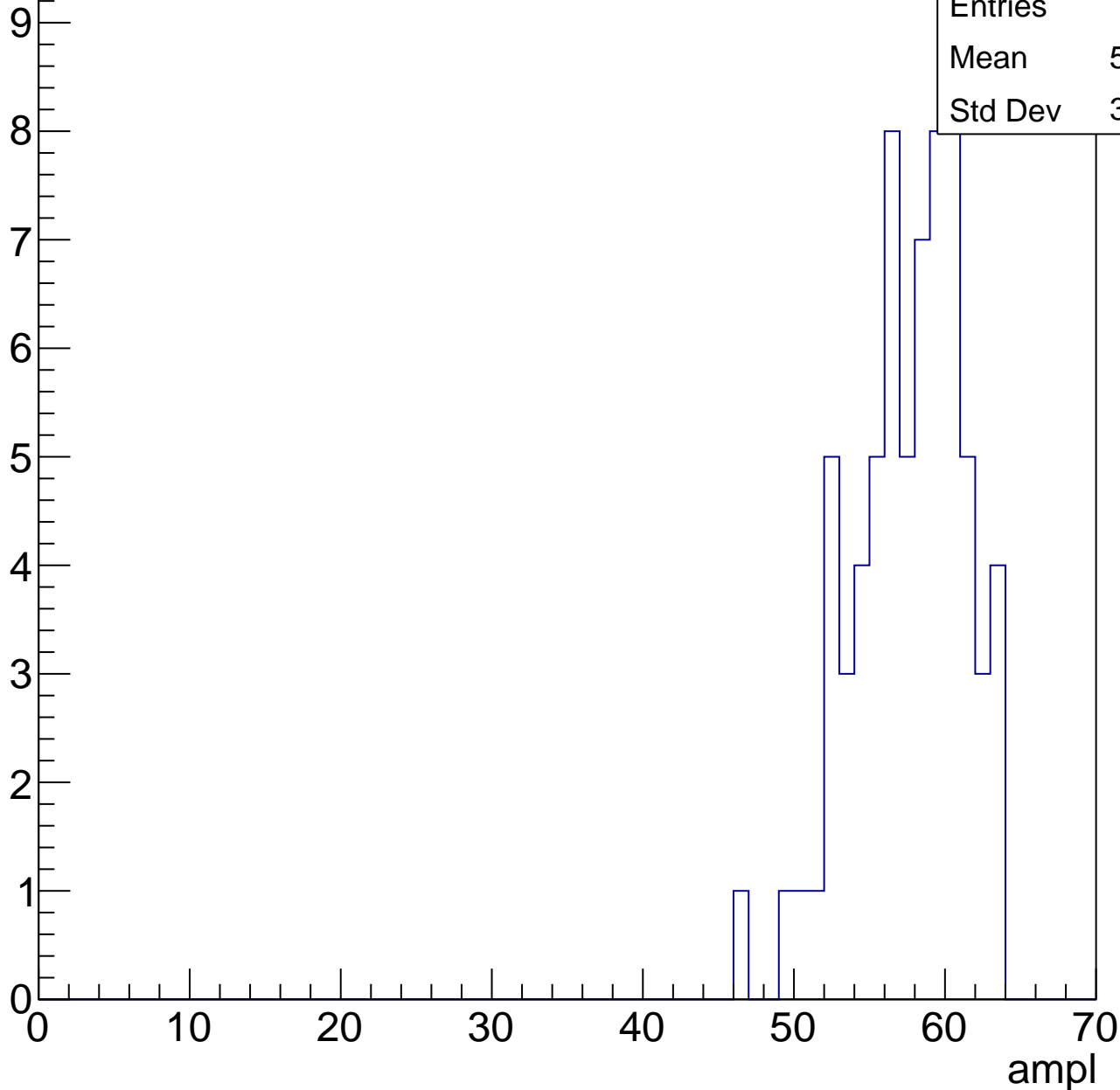


B1L103S, U5-ch6, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	57.14
Std Dev	3.634

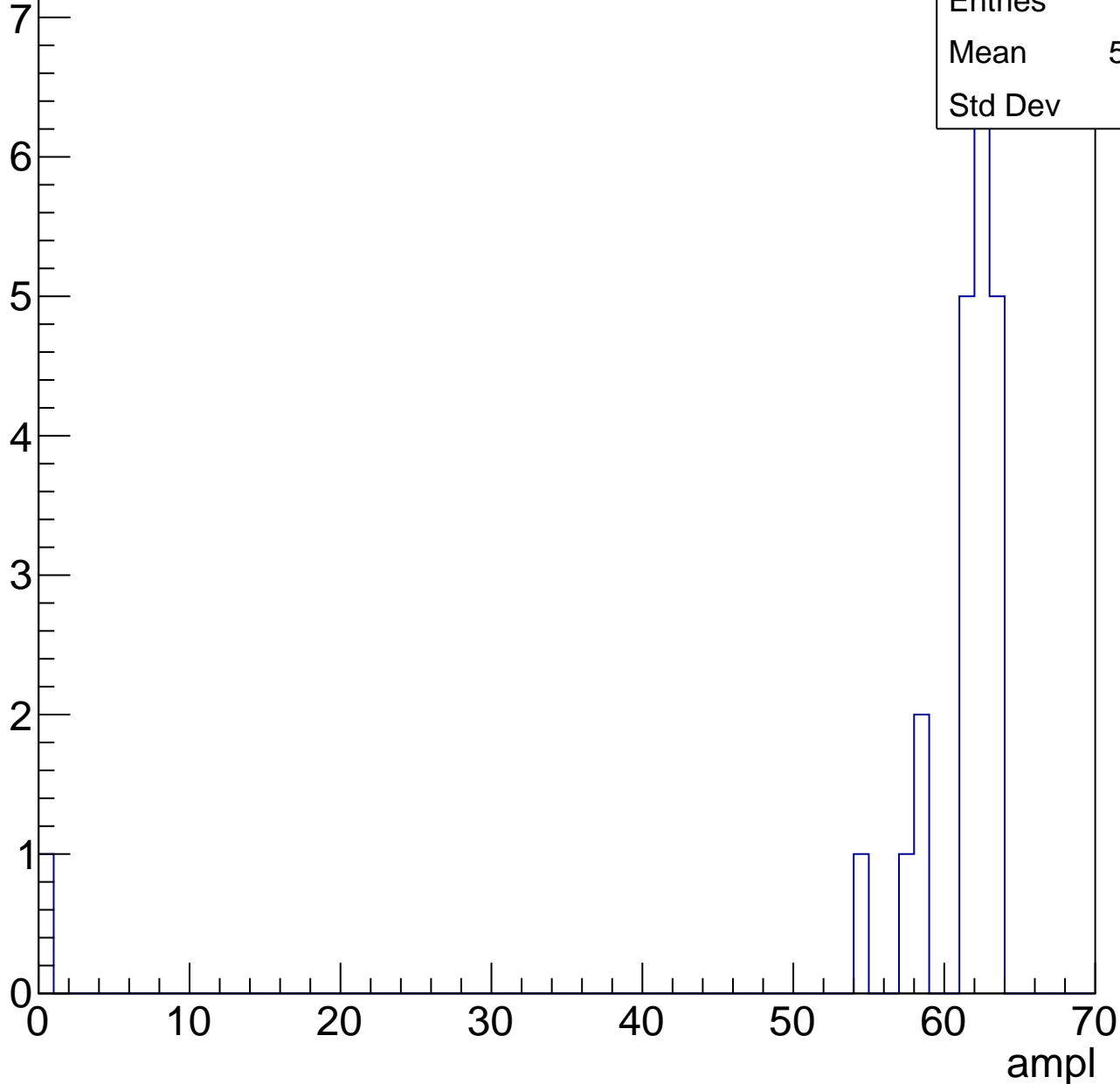


B1L103S, U5-ch6, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	22
Mean	58.23
Std Dev	12.9



B1L103S, U5-ch6, adc7

calib_packv5_041523_1651.root, FC#0, port C2

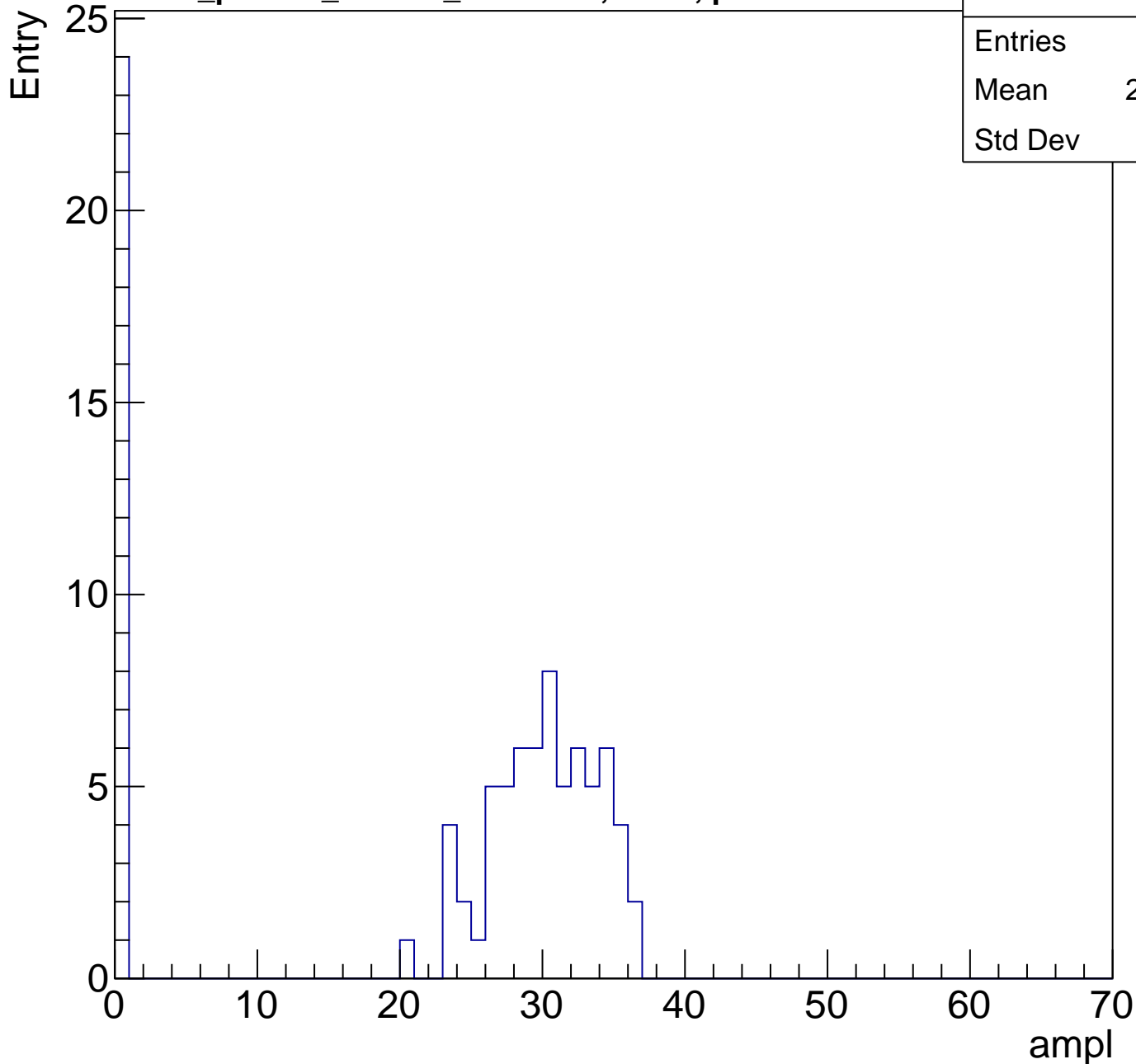
Entries	20
Mean	3.15
Std Dev	13.73



B1L103S, U5-ch7, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	90
Mean	21.78
Std Dev	13.5



B1L103S, U5-ch7, adc1

calib_packv5_041523_1651.root, FC#0, port C2

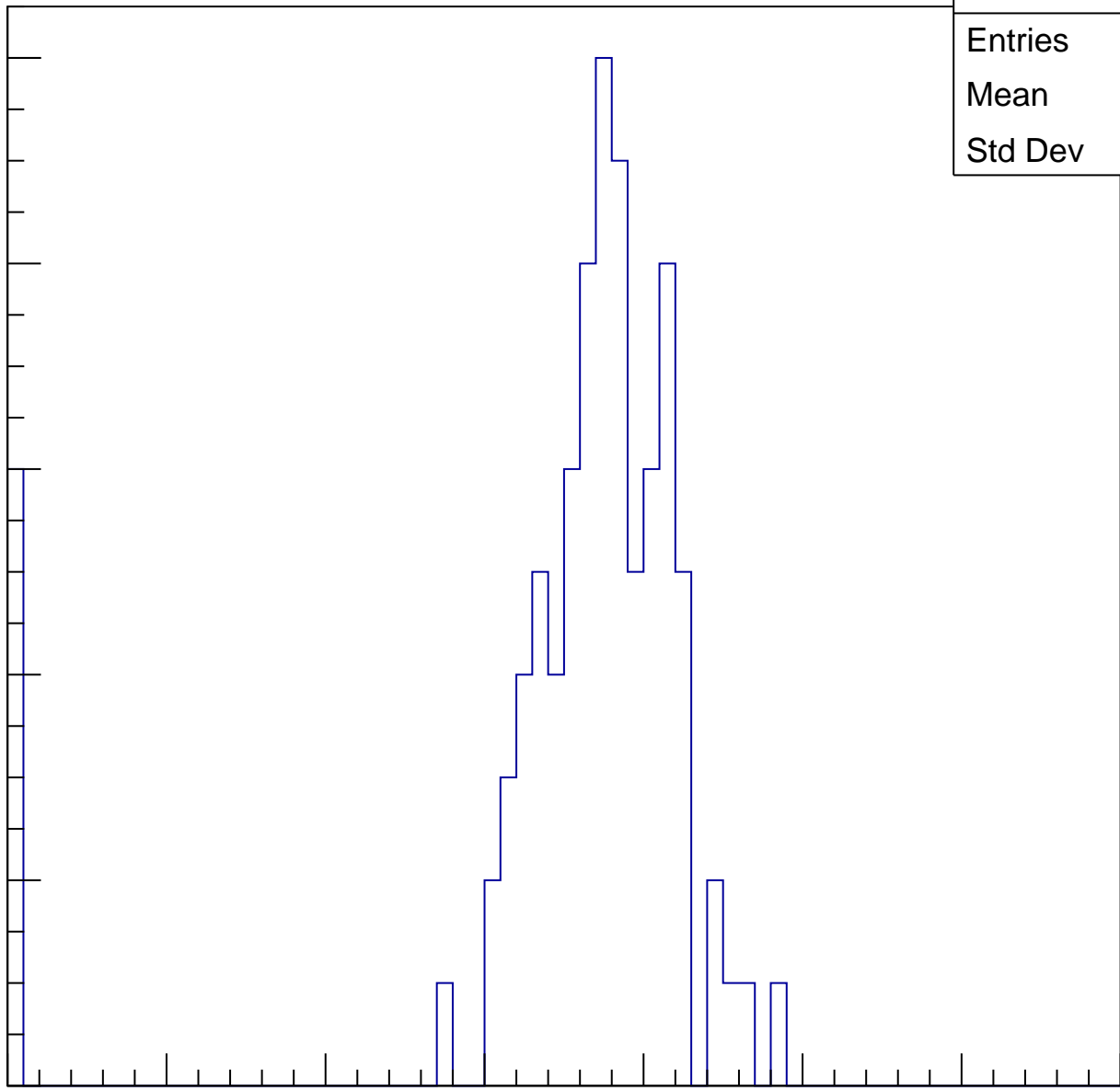
Entries	87
Mean	34.7
Std Dev	10.18

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

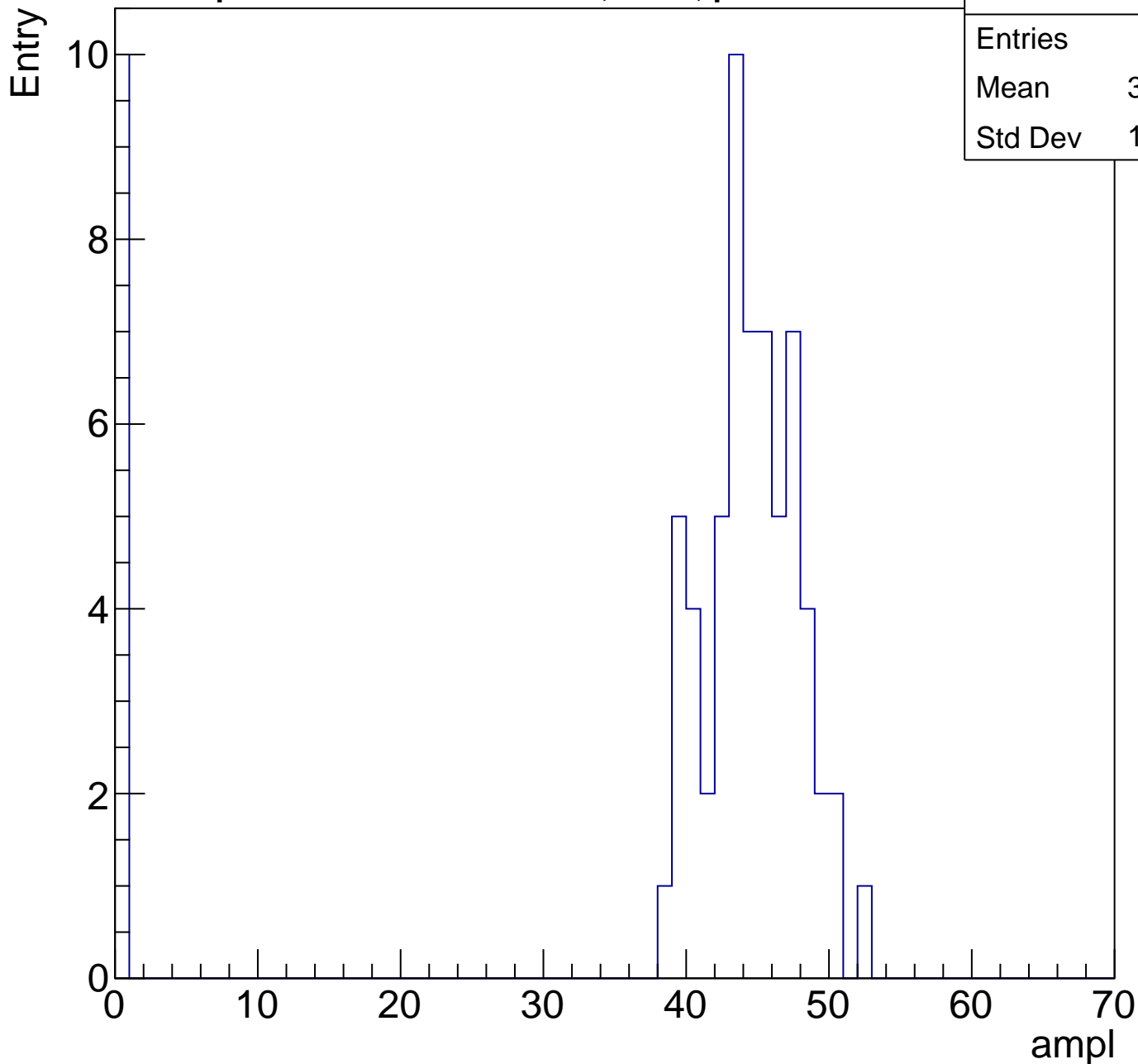
ampl



B1L103S, U5-ch7, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	72
Mean	38.04
Std Dev	15.55

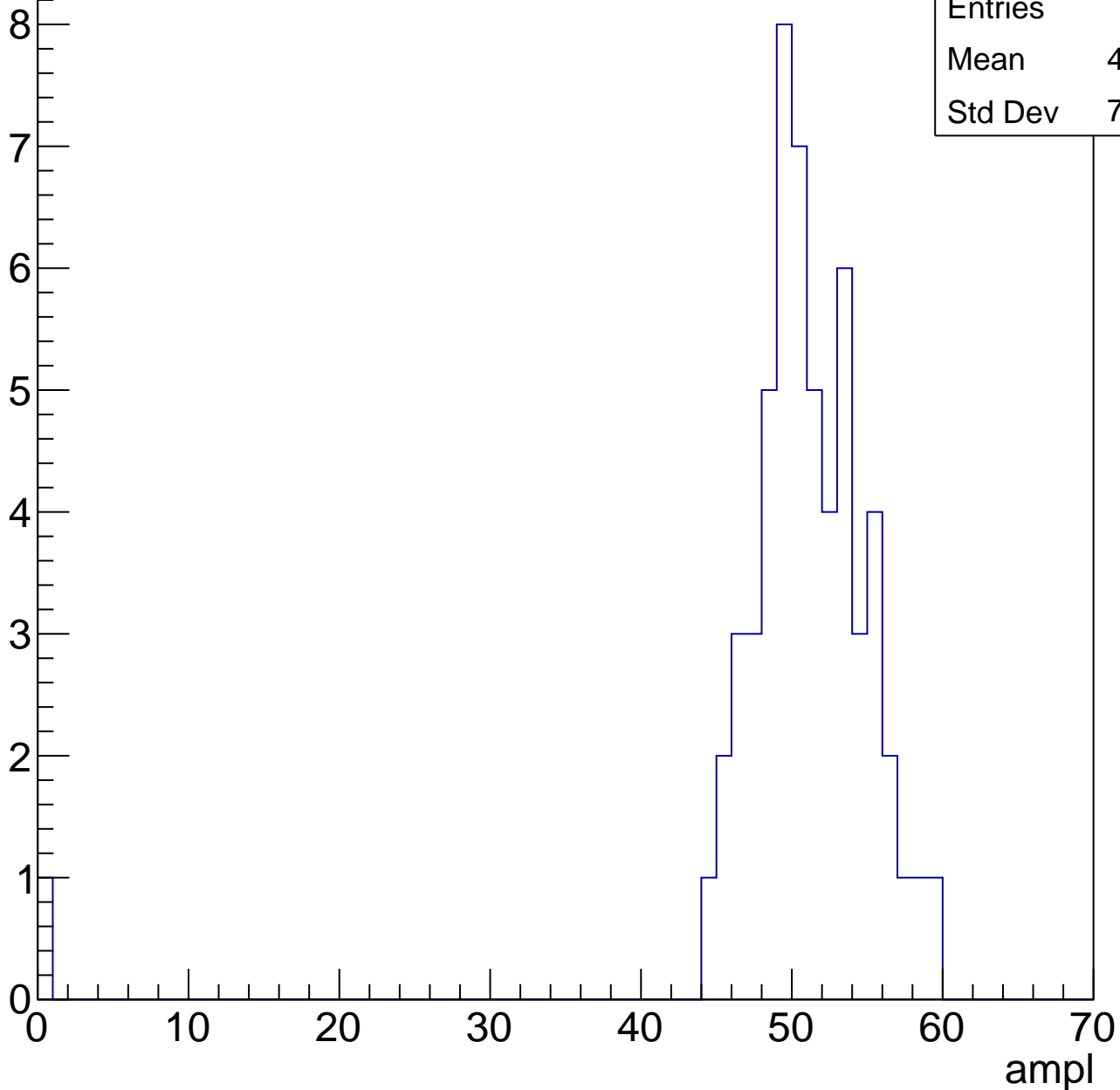


B1L103S, U5-ch7, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	49.89
Std Dev	7.466

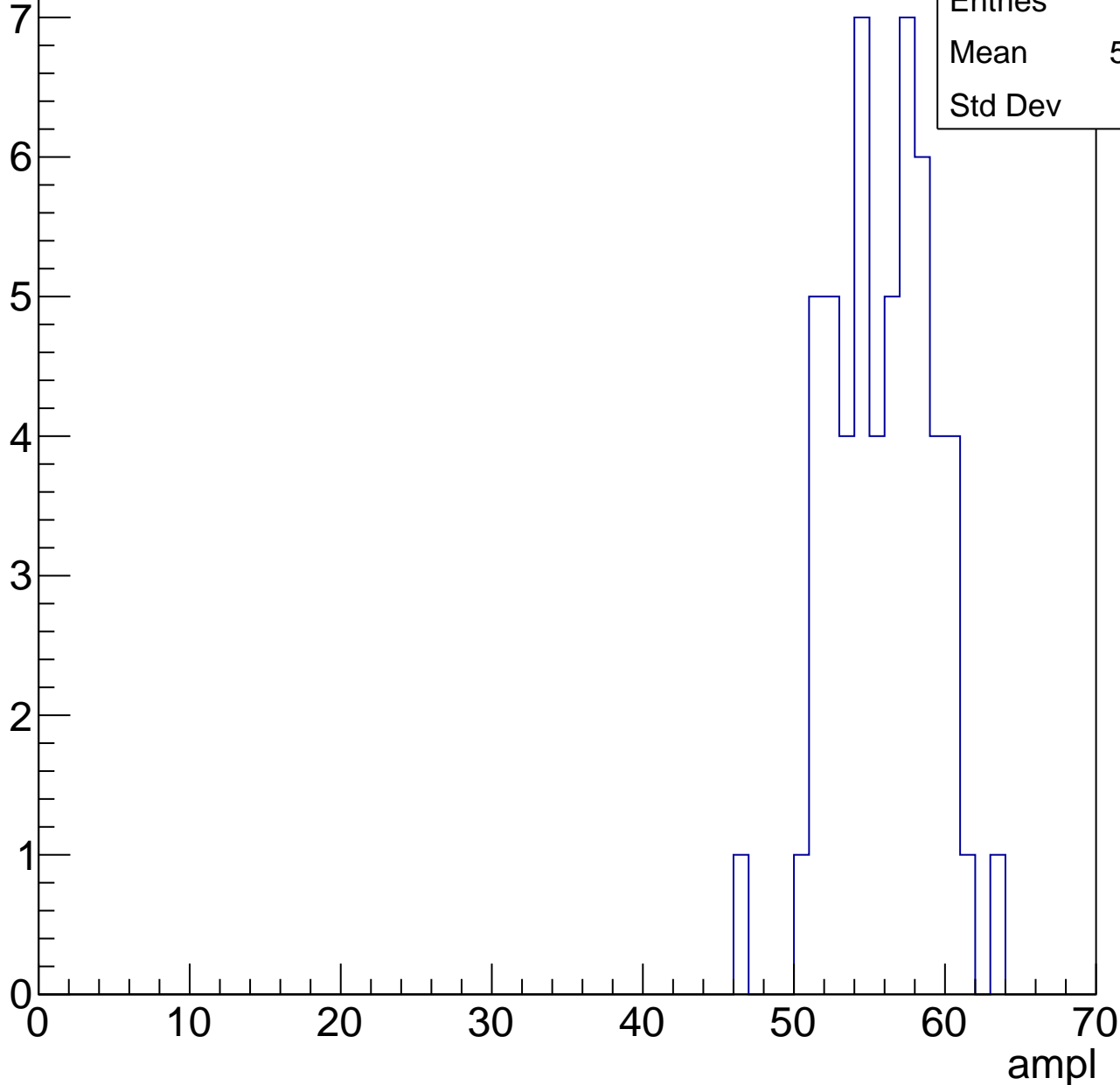


B1L103S, U5-ch7, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	55.42
Std Dev	3.29



B1L103S, U5-ch7, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

8
7
6
5
4
3
2
1
0

Entries	43
Mean	58.81
Std Dev	9.379

ampl

0

10

20

30

40

50

60

70

B1L103S, U5-ch7, adc6

calib_packv5_041523_1651.root, FC#0, port C2

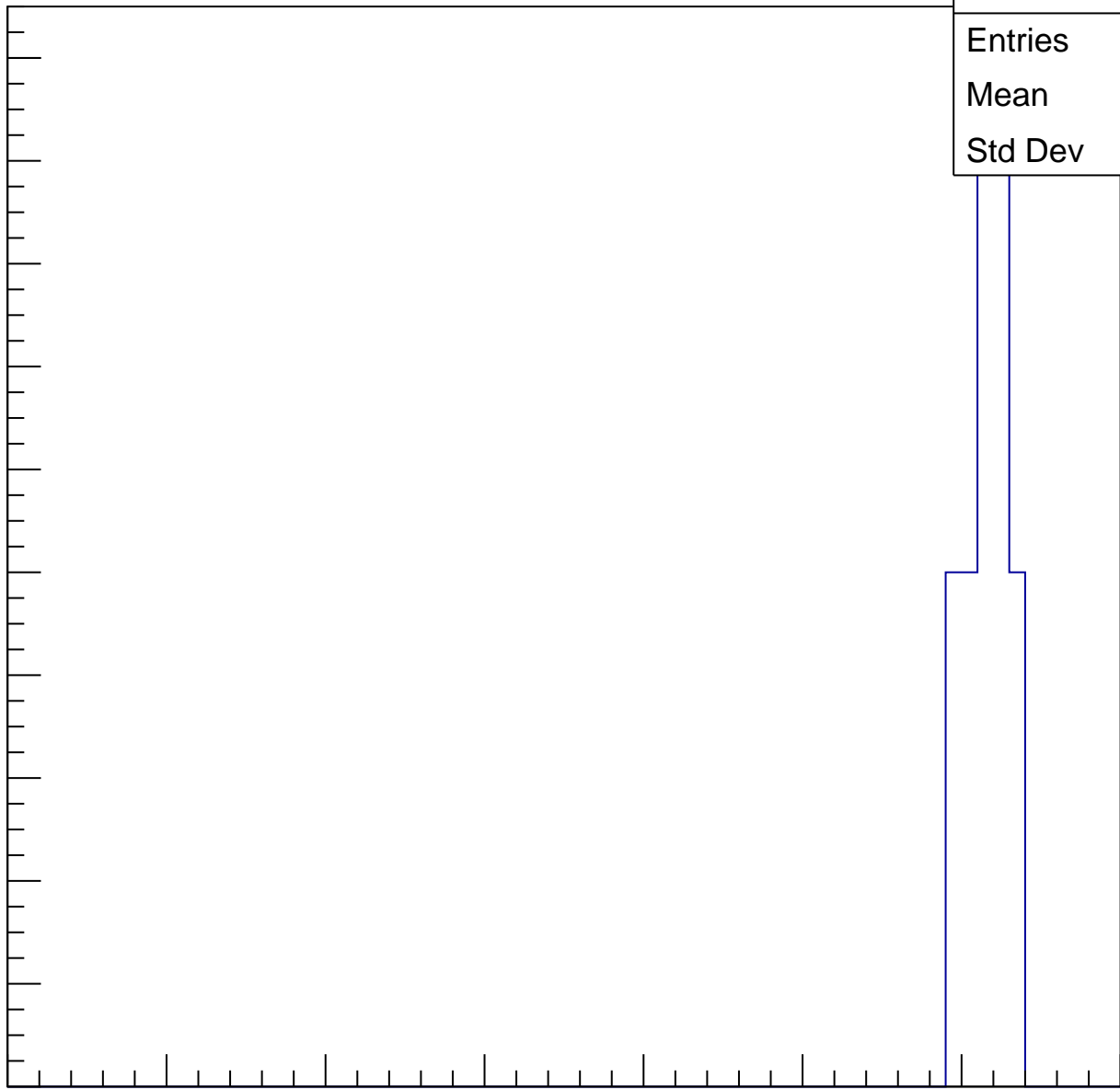
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	7
Mean	61.14
Std Dev	1.245

ampl

0 10 20 30 40 50 60 70



B1L103S, U5-ch7, adc7

calib_packv5_041523_1651.root, FC#0, port C2

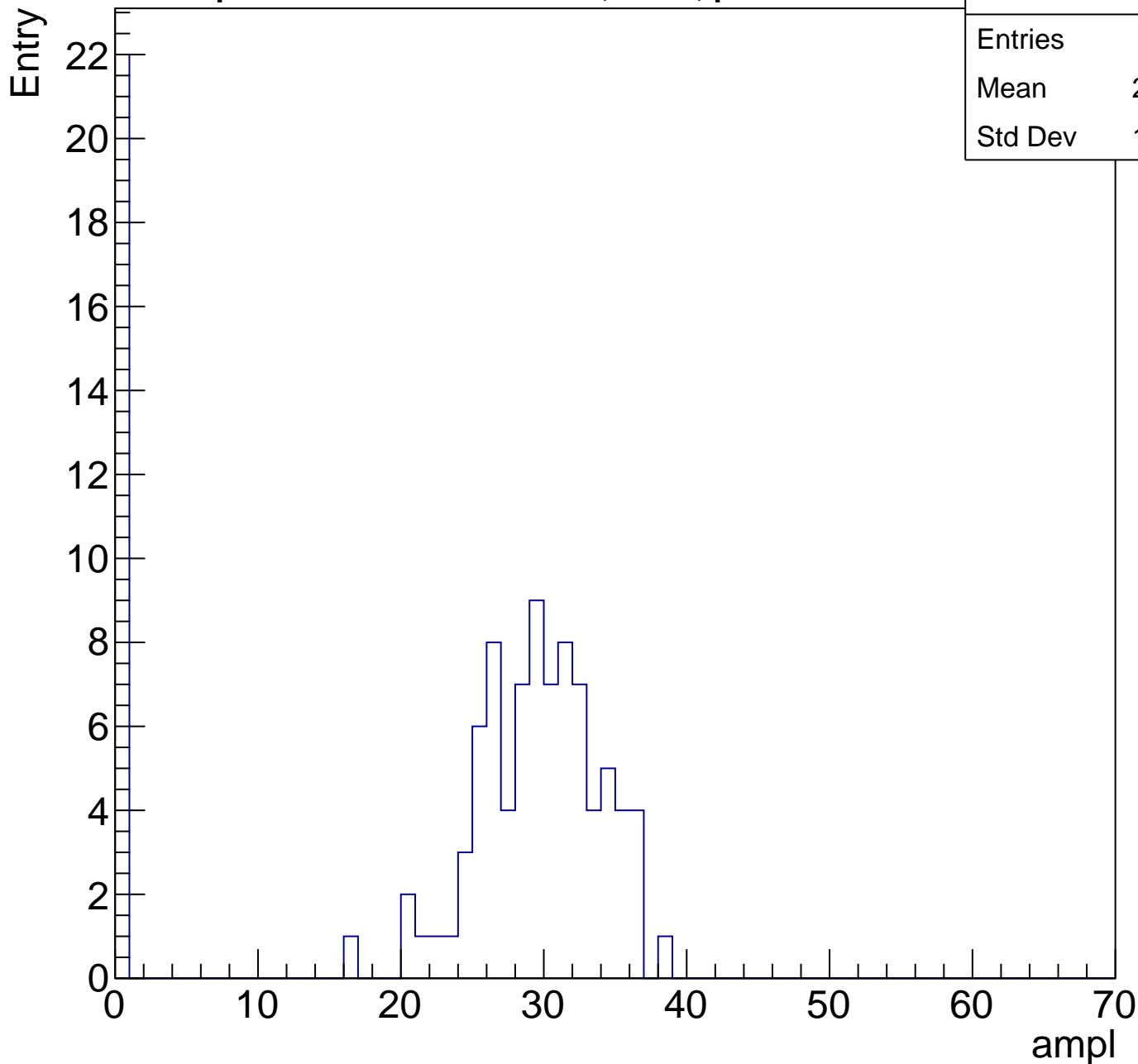
Entries	19
Mean	0
Std Dev	0



B1L103S, U5-ch8, adc0

calib_packv5_041523_1651.root, FC#0, port C2

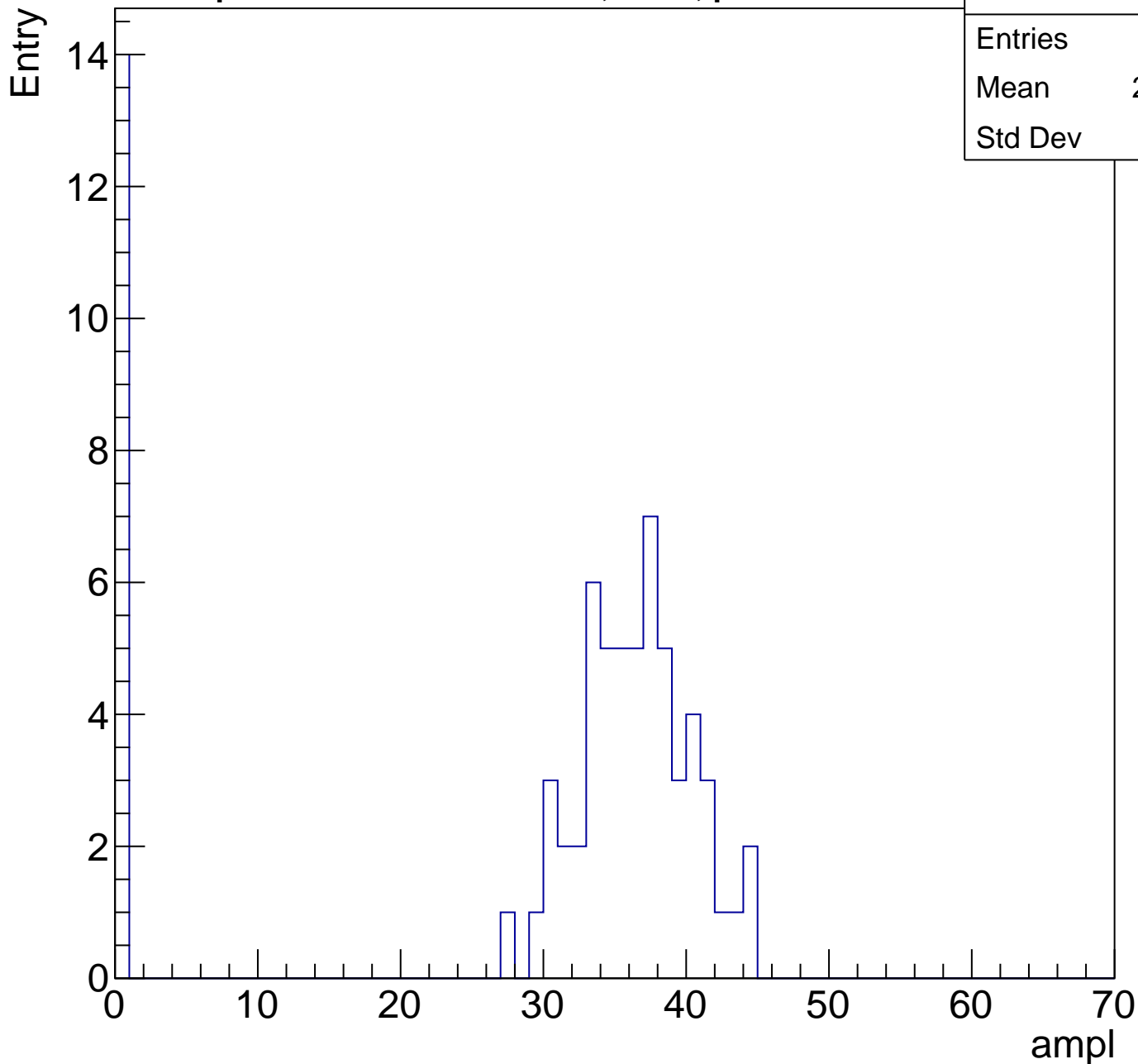
Entries	105
Mean	23.08
Std Dev	12.45



B1L103S, U5-ch8, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	70
Mean	28.81
Std Dev	14.8

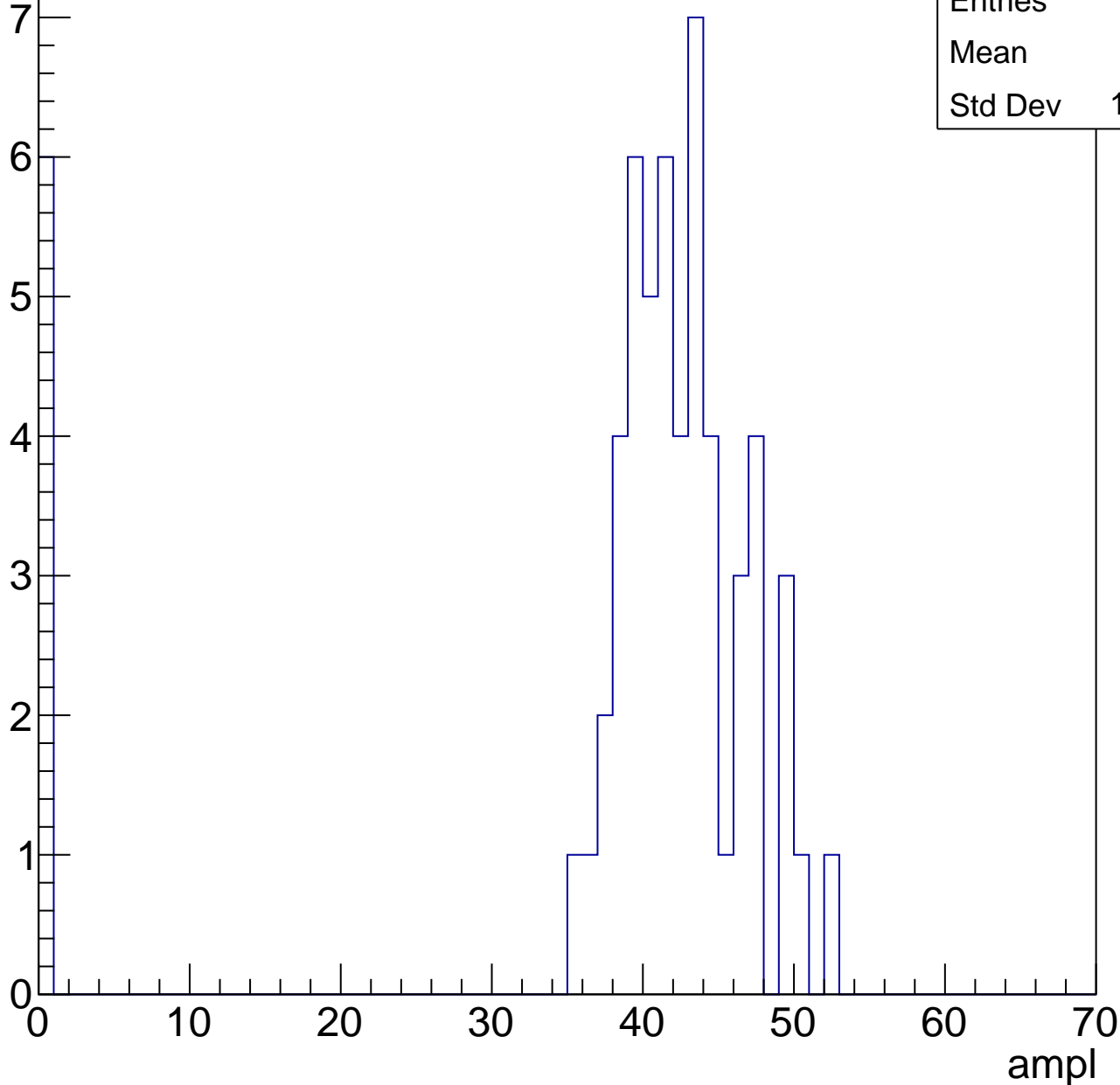


B1L103S, U5-ch8, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

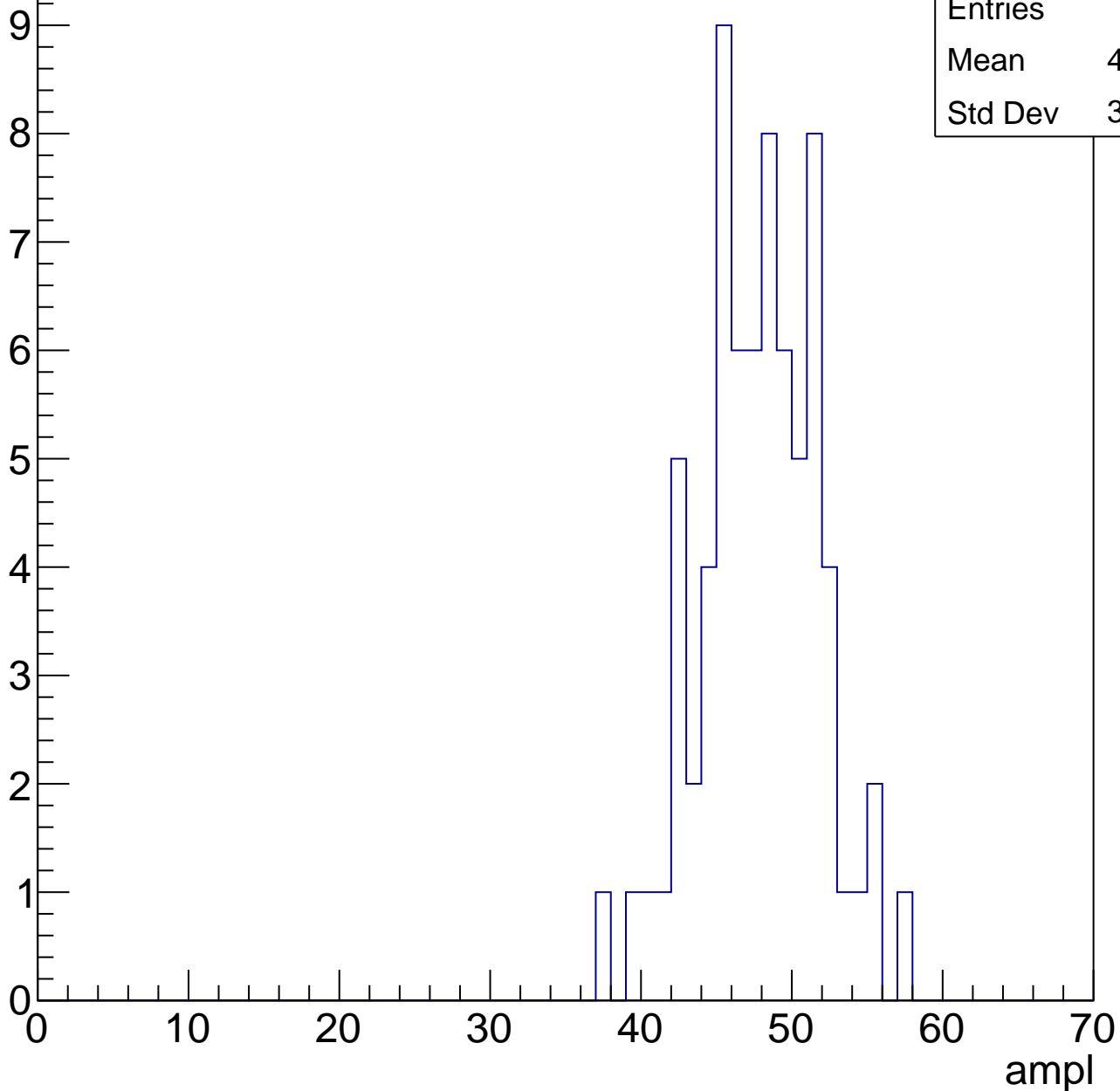
Entries	59
Mean	38
Std Dev	13.28



B1L103S, U5-ch8, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry



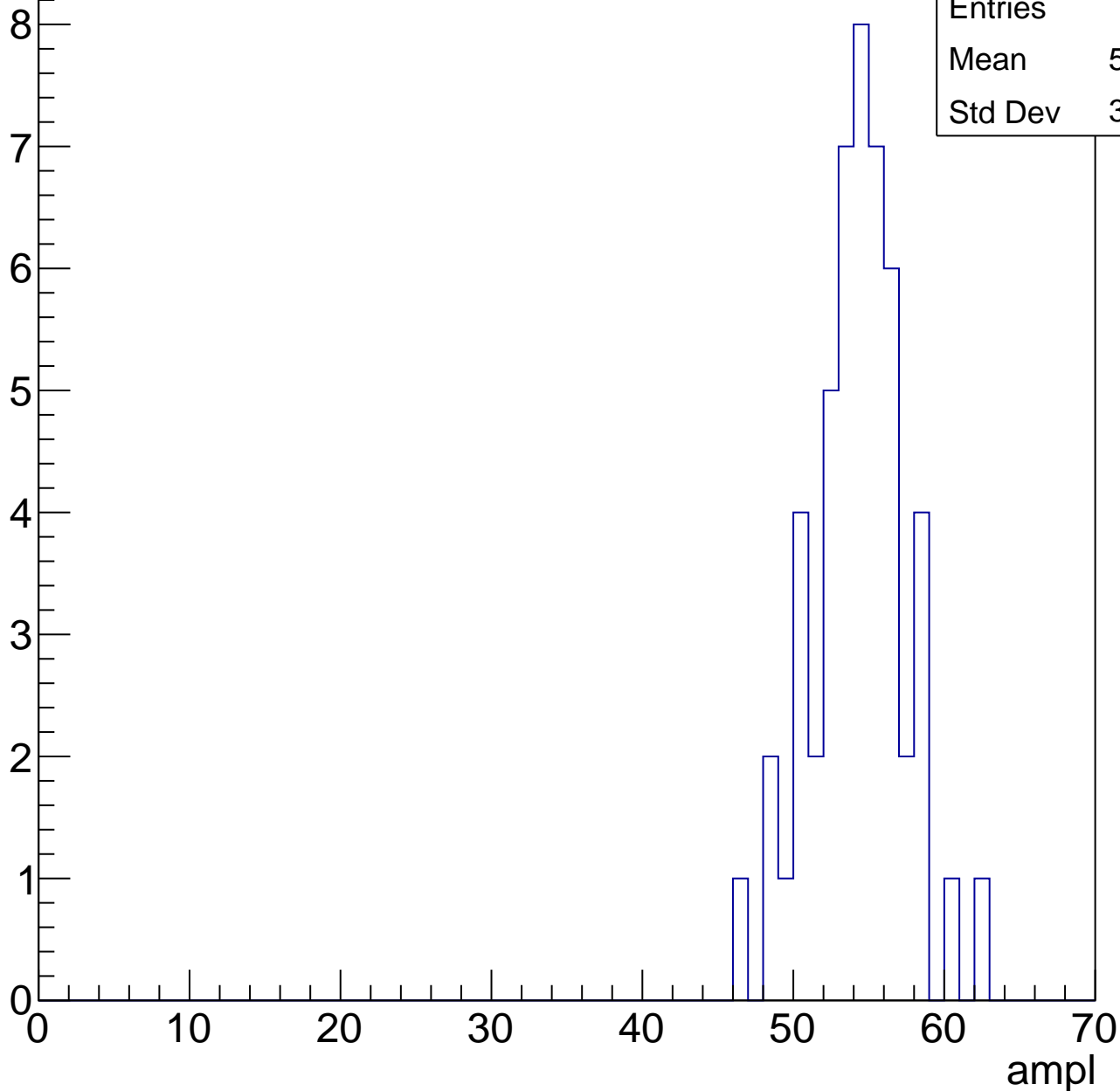
Entries	72
Mean	47.36
Std Dev	3.896

B1L103S, U5-ch8, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	53.82
Std Dev	3.072



B1L103S, U5-ch8, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entries	53
Mean	57.89
Std Dev	8.386

Entry

10

8

6

4

2

0

0

10

20

30

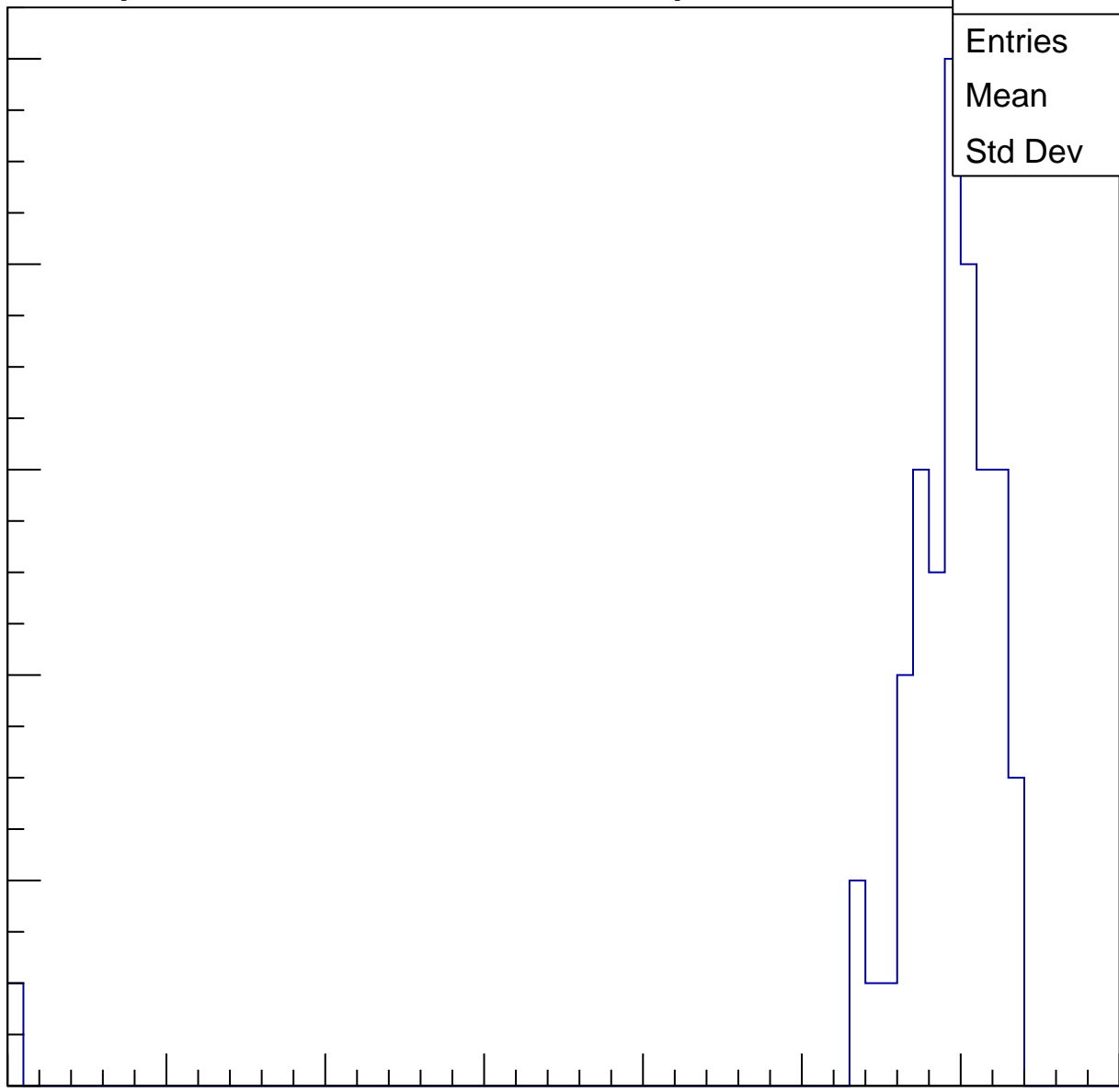
40

50

60

70

ampl

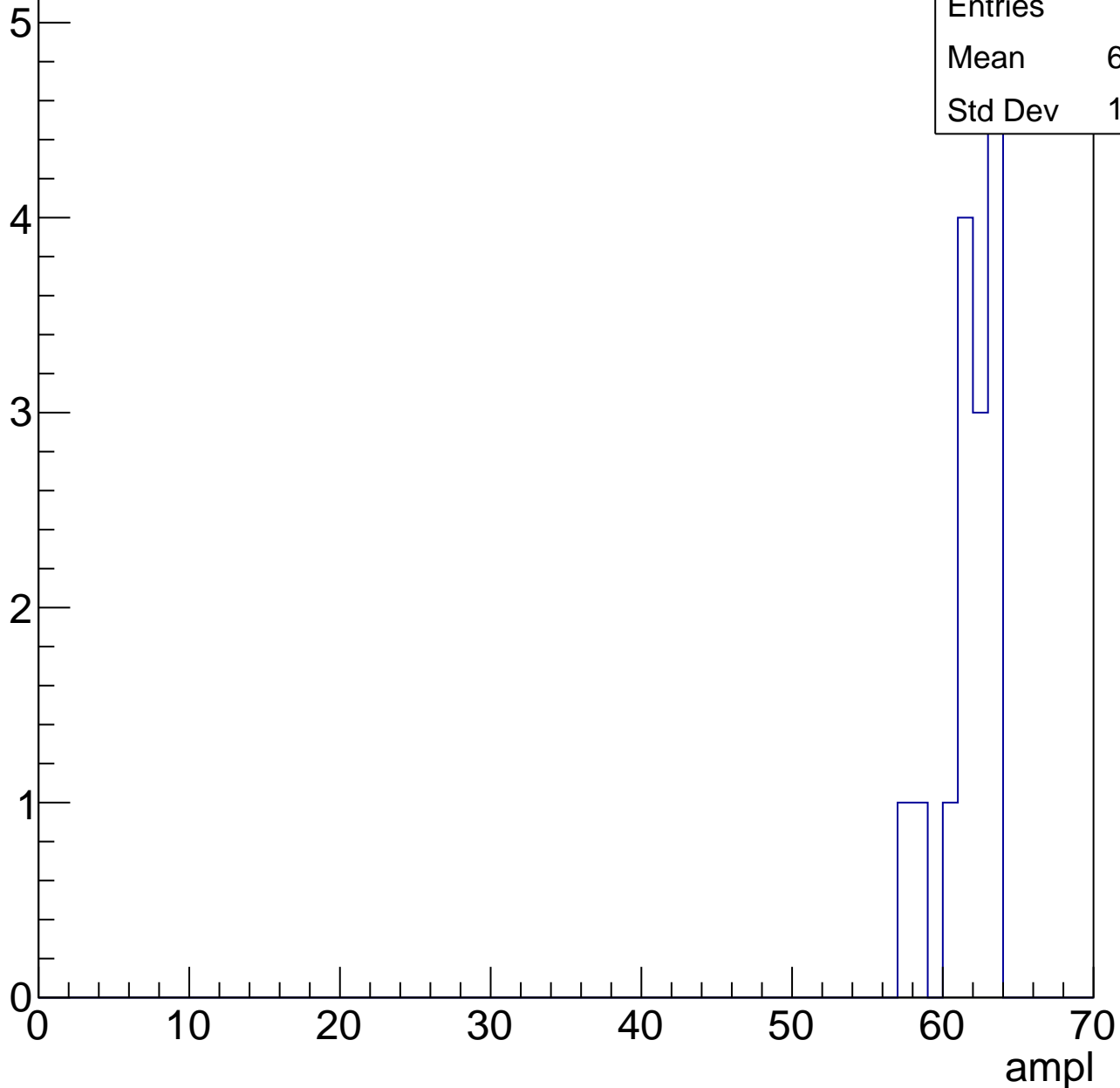


B1L103S, U5-ch8, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	15
Mean	61.33
Std Dev	1.776

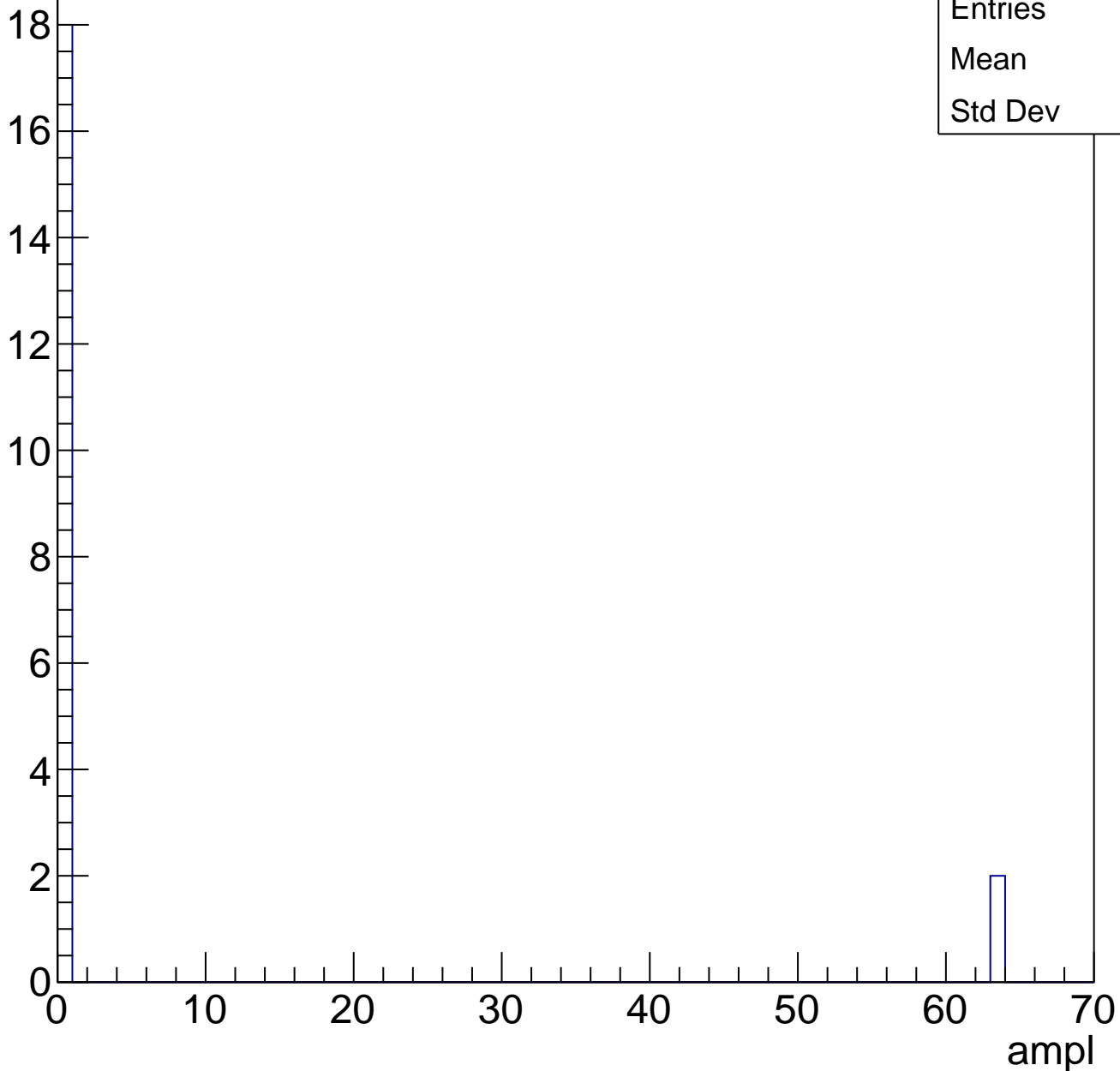


B1L103S, U5-ch8, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	6.3
Std Dev	18.9

Entry

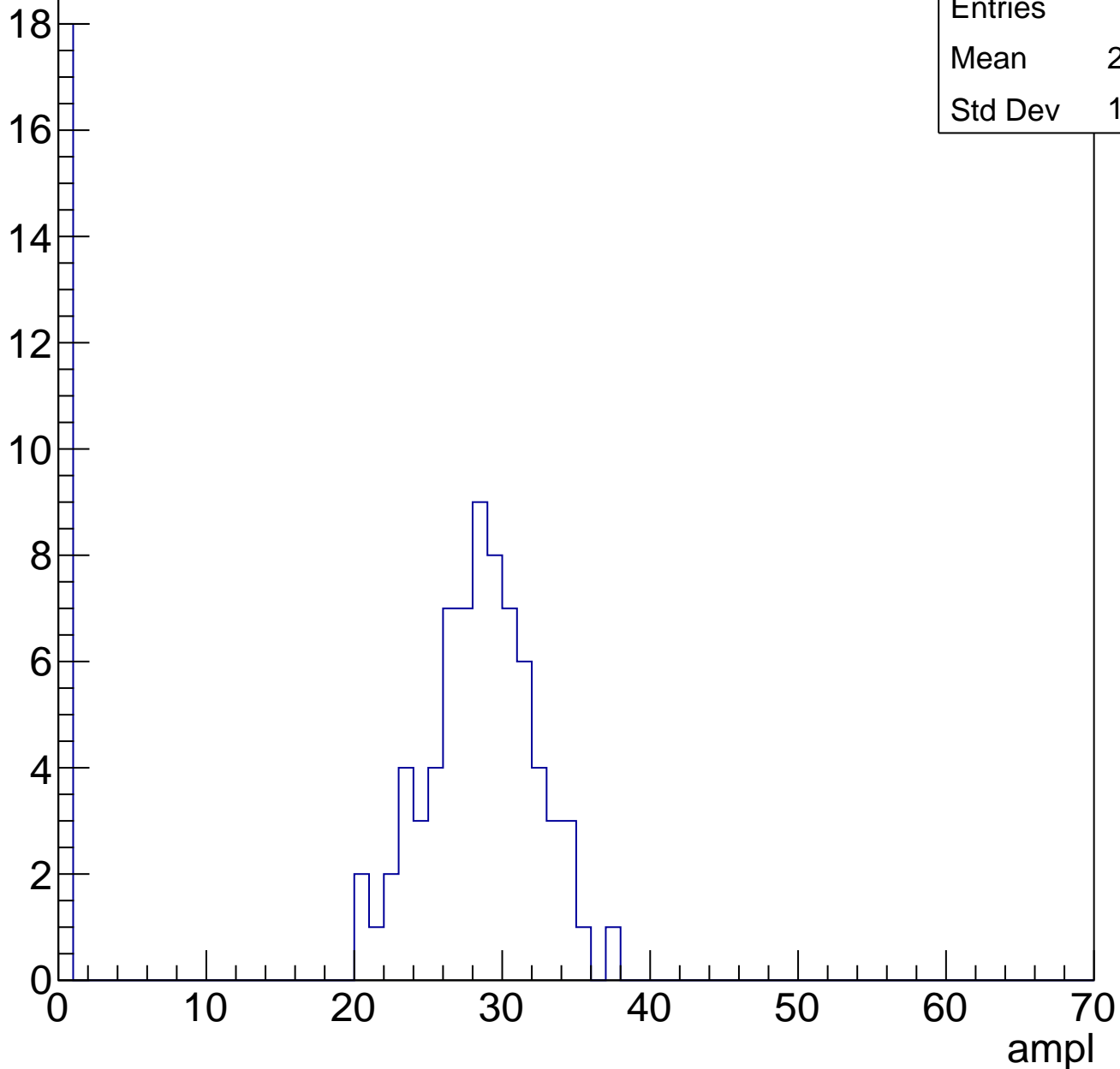


B1L103S, U5-ch9, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	90
Mean	22.46
Std Dev	11.68

Entry

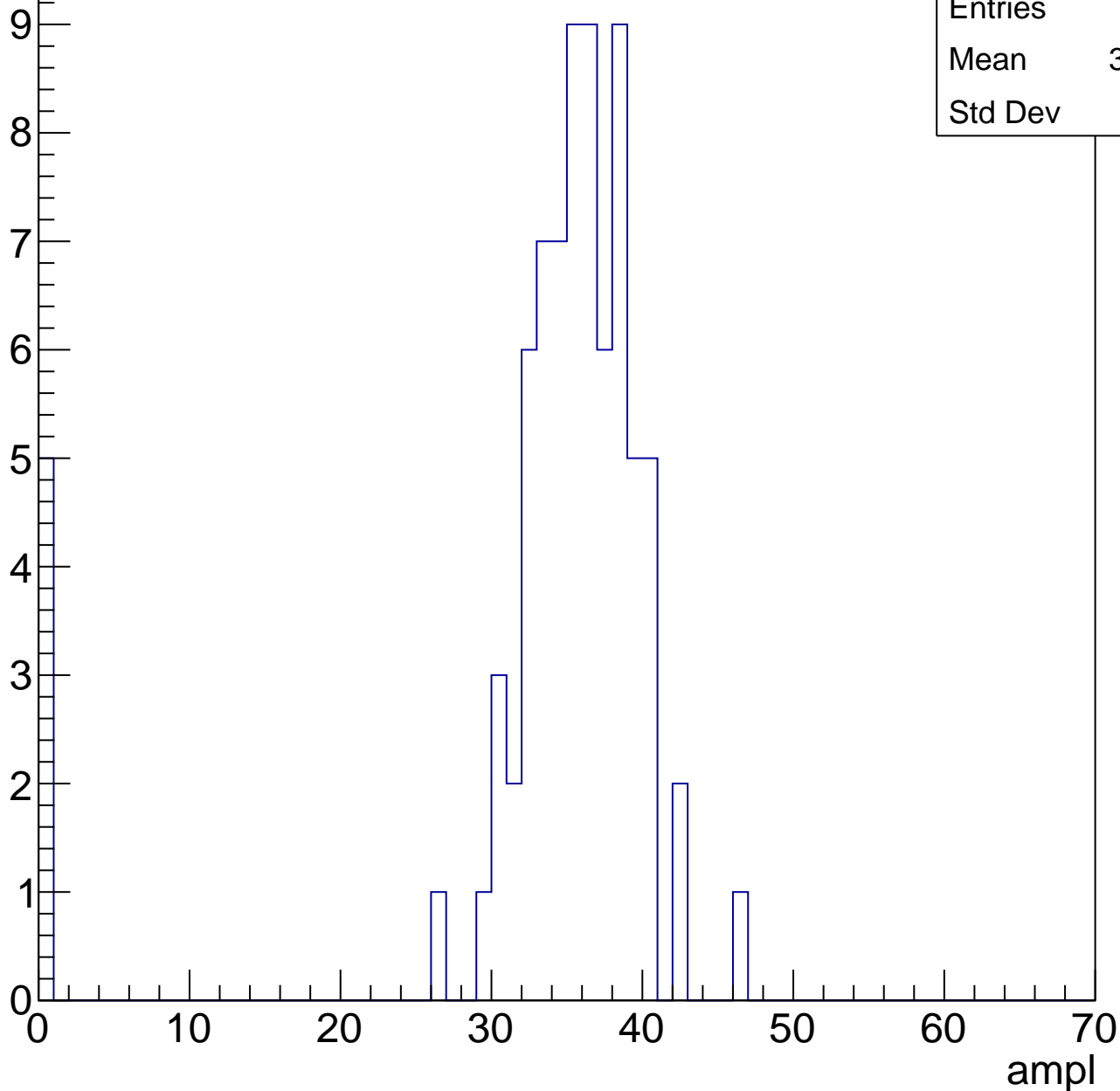


B1L103S, U5-ch9, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	33.28
Std Dev	9.3



B1L103S, U5-ch9, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	37.26
Std Dev	15.09

Entry

10

8

6

4

2

0

0

10

20

30

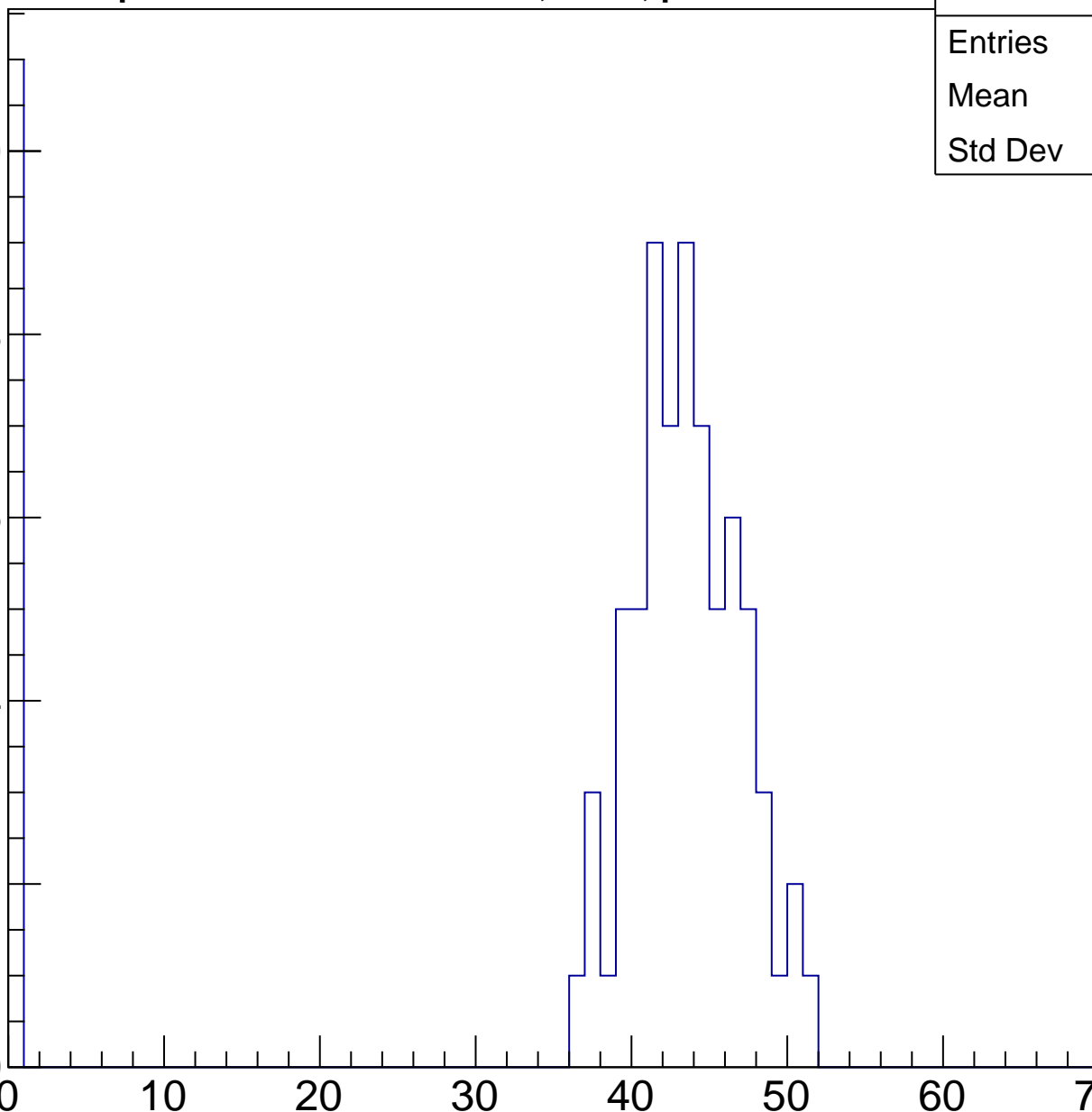
40

50

60

70

ampl

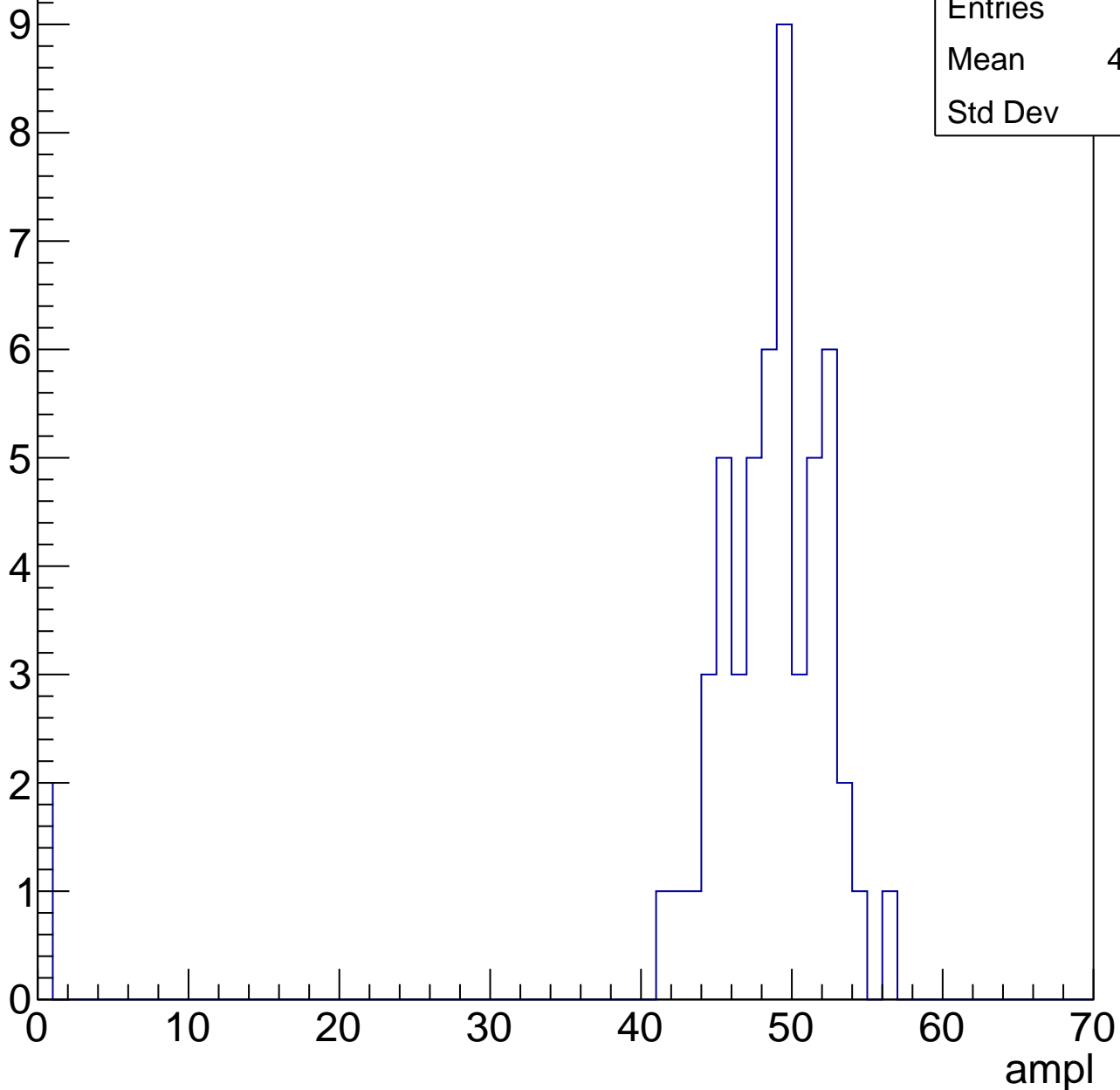


B1L103S, U5-ch9, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	46.63
Std Dev	9.66

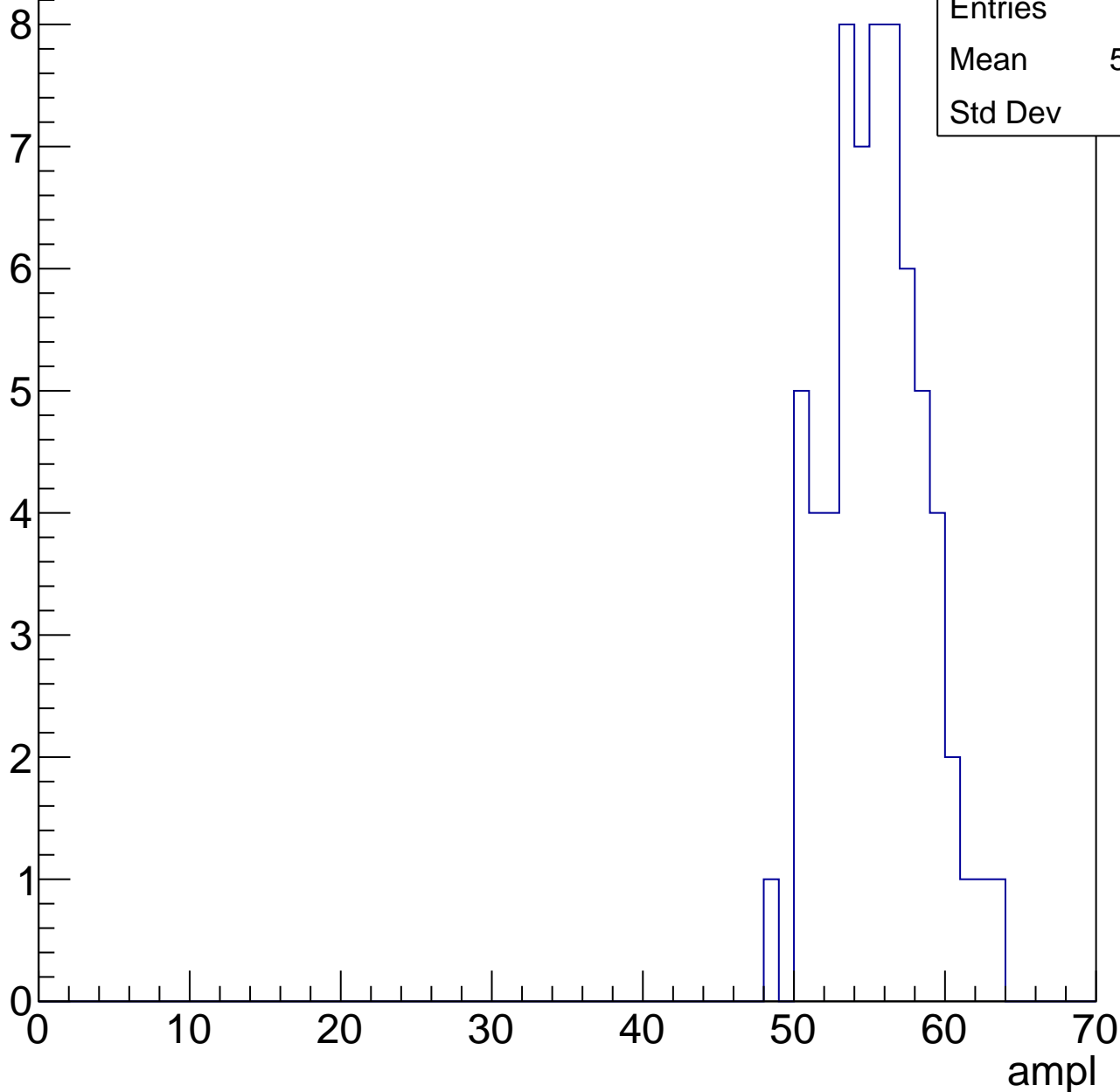


B1L103S, U5-ch9, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	54.98
Std Dev	3.17



B1L103S, U5-ch9, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

8
7
6
5
4
3
2
1
0

Entries	47
Mean	58.3
Std Dev	8.915

ampl

0

10

20

30

40

50

60

70

B1L103S, U5-ch9, adc6

calib_packv5_041523_1651.root, FC#0, port C2

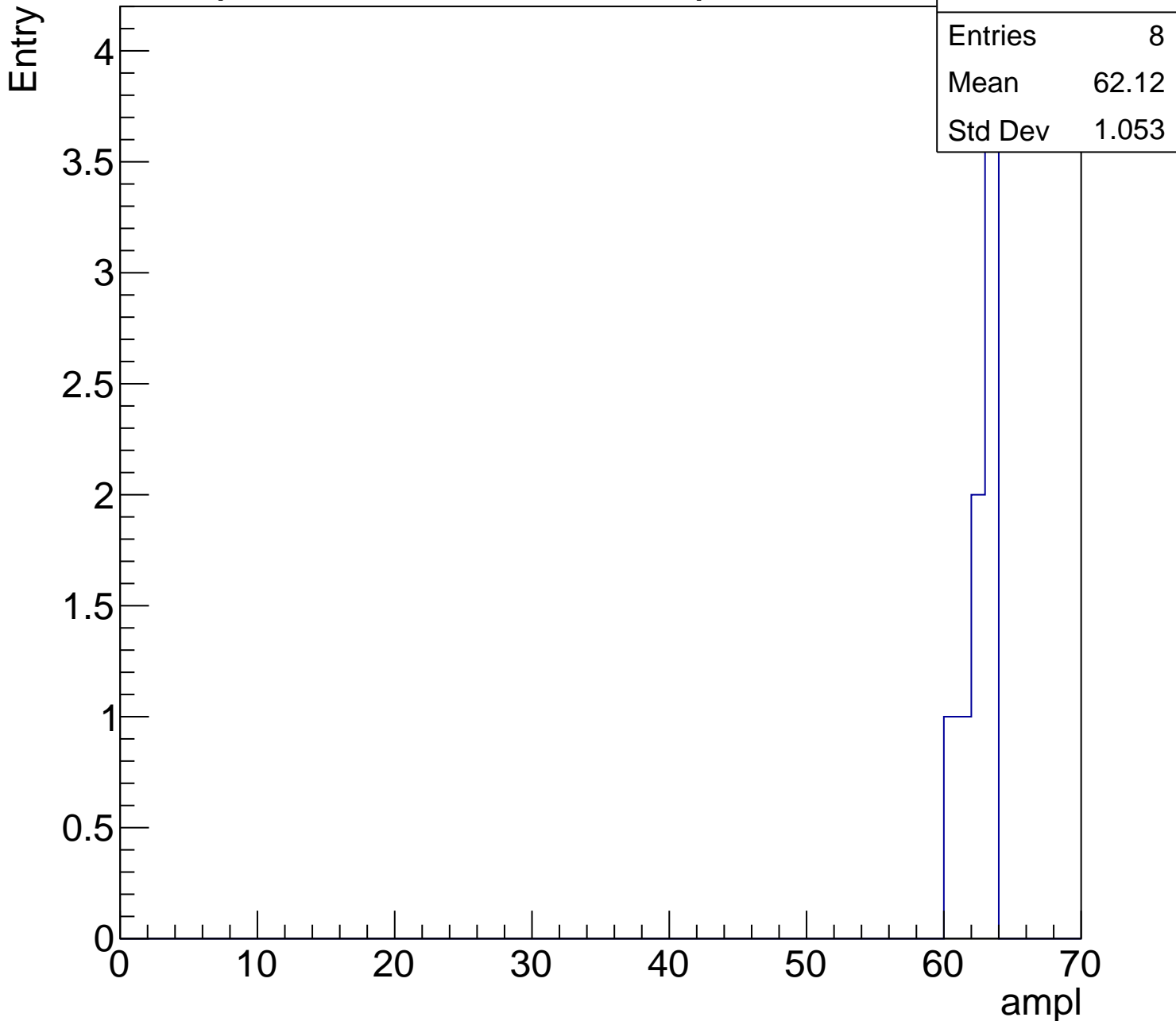
Entry

4
3.5
3
2.5
2
1.5
1
0.5
0

Entries	8
Mean	62.12
Std Dev	1.053

0 10 20 30 40 50 60 70

ampl

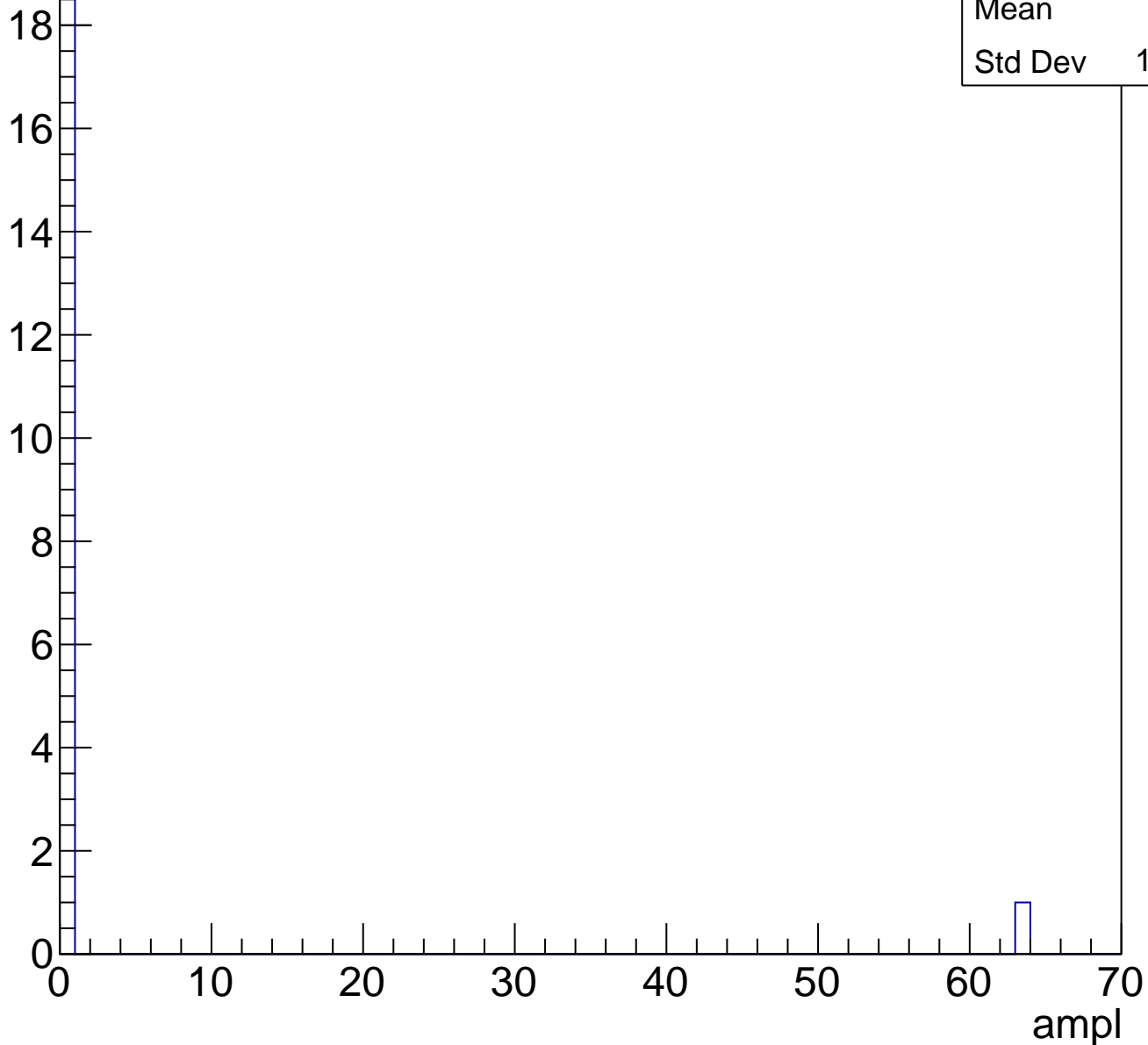


B1L103S, U5-ch9, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry

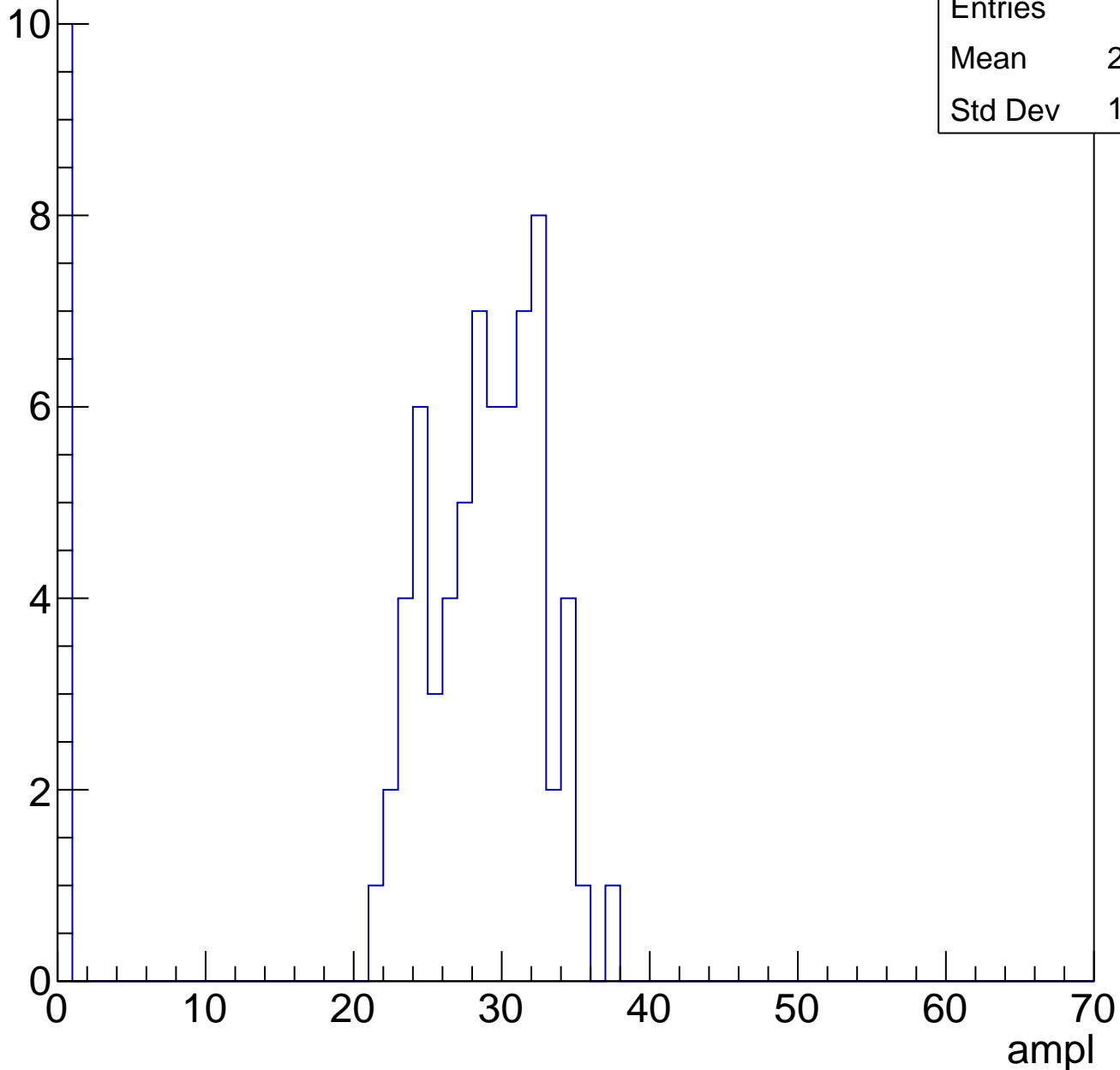


B1L103S, U5-ch10, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	77
Mean	24.83
Std Dev	10.18

Entry

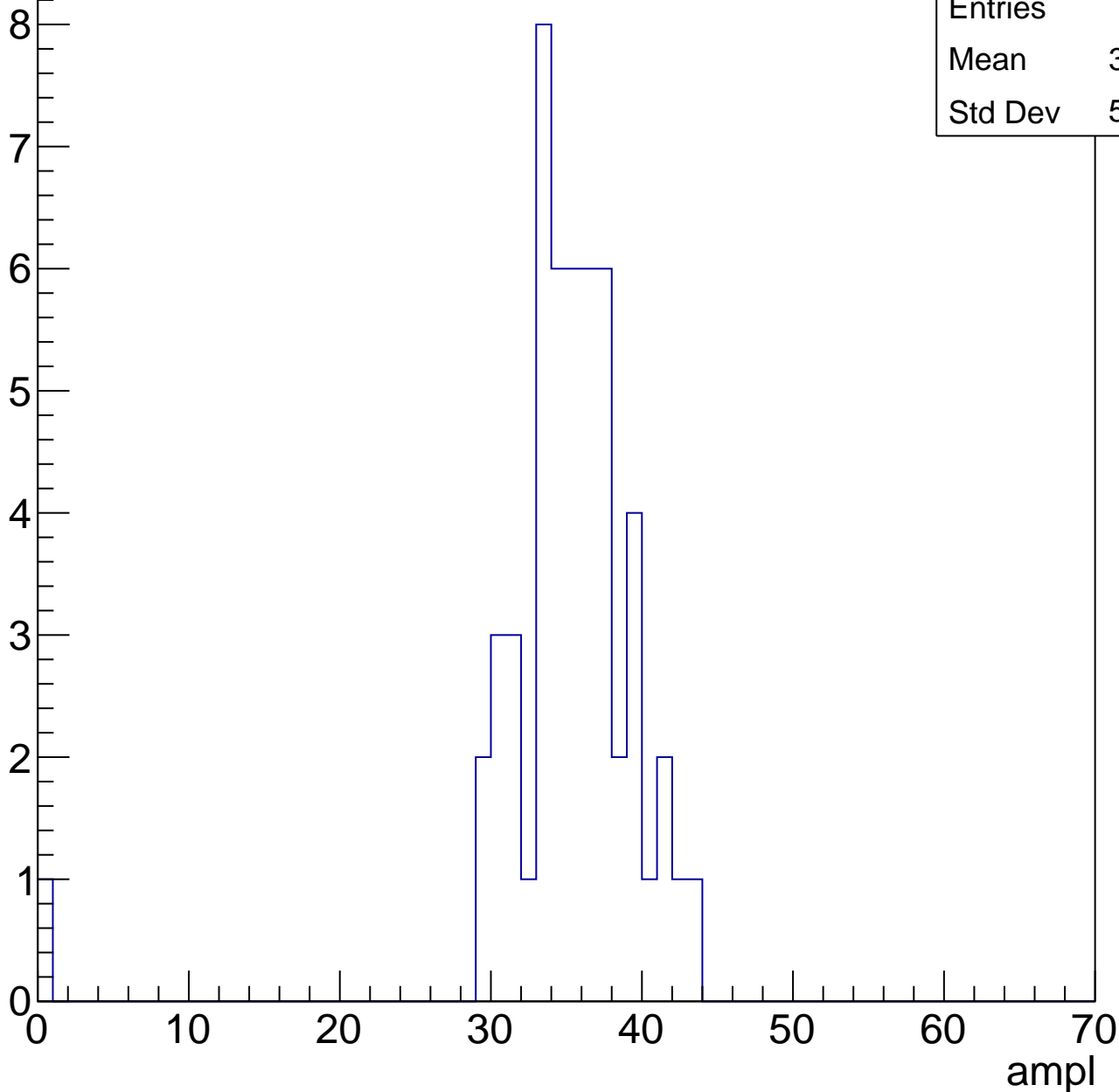


B1L103S, U5-ch10, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	34.49
Std Dev	5.788

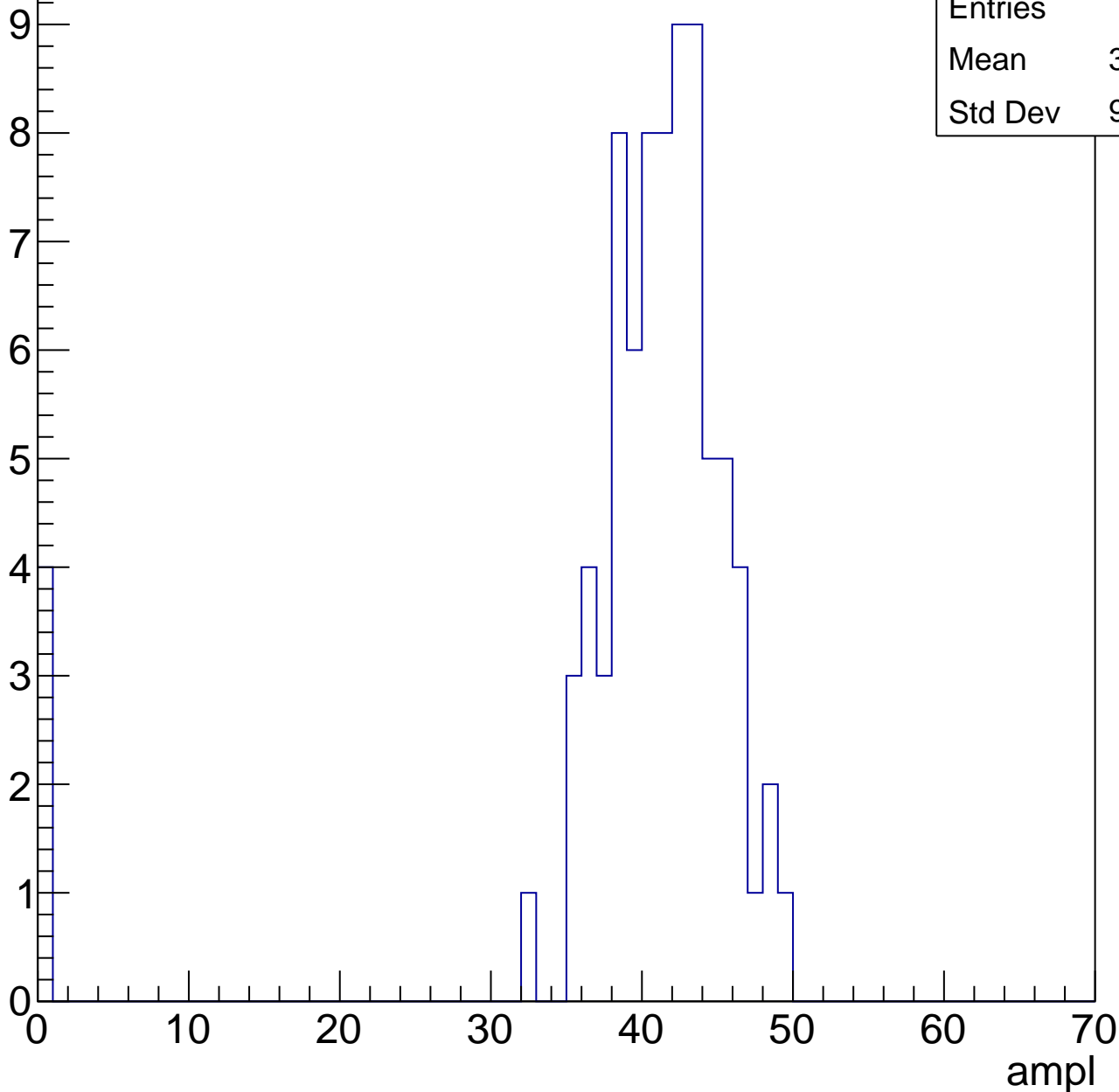


B1L103S, U5-ch10, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	81
Mean	39.06
Std Dev	9.512

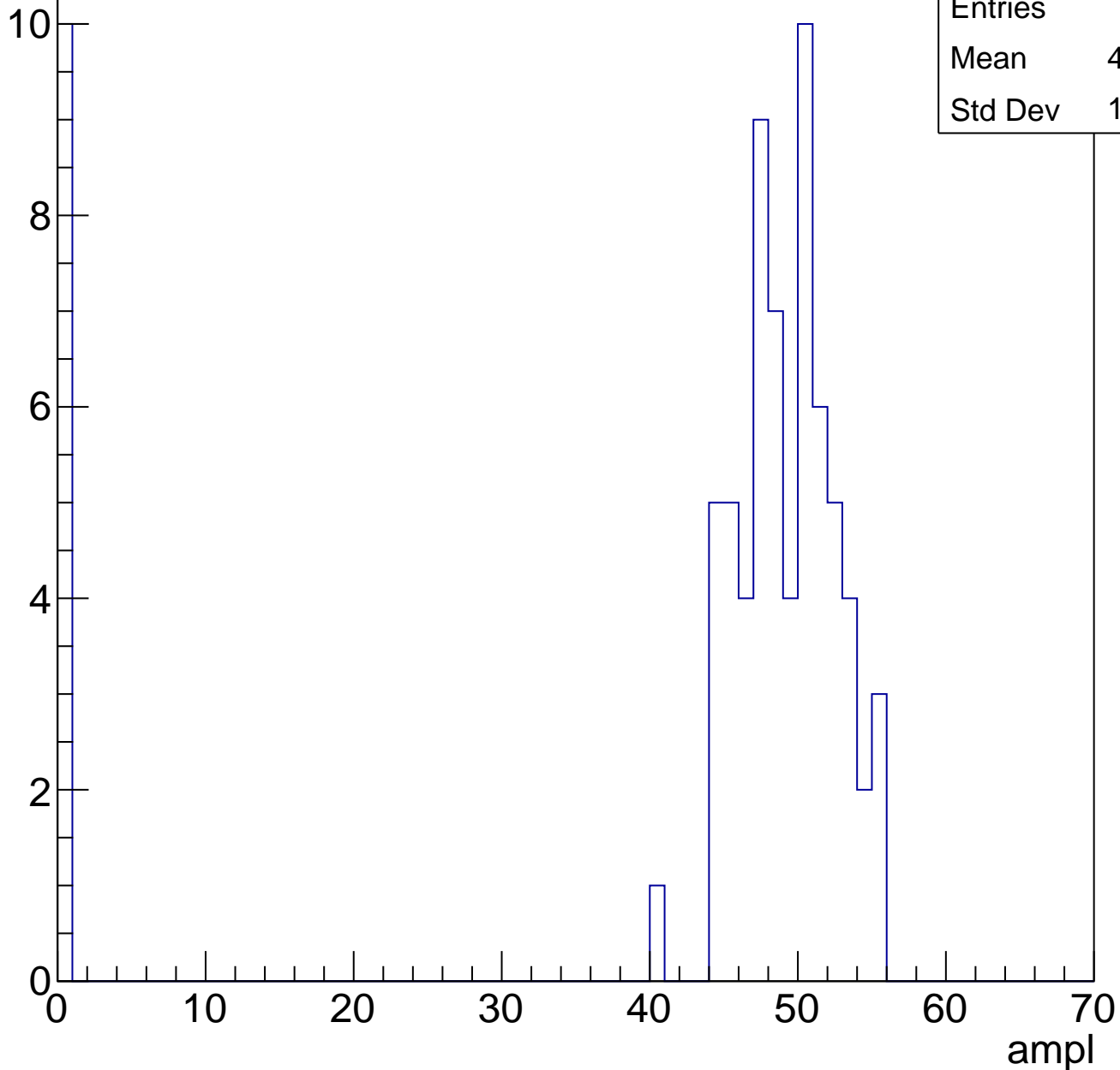


B1L103S, U5-ch10, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	42.33
Std Dev	16.87

Entry

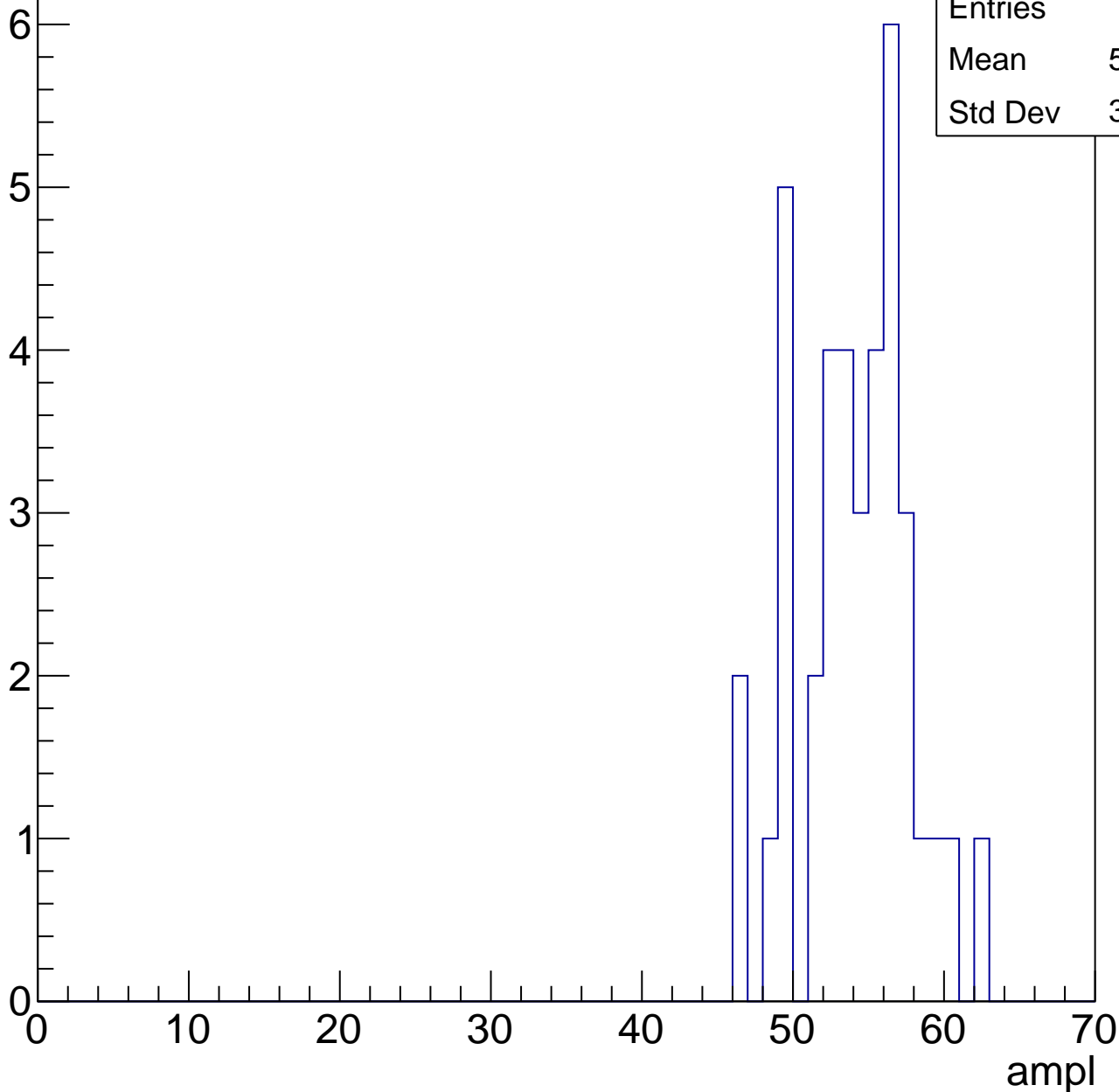


B1L103S, U5-ch10, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	38
Mean	53.55
Std Dev	3.683

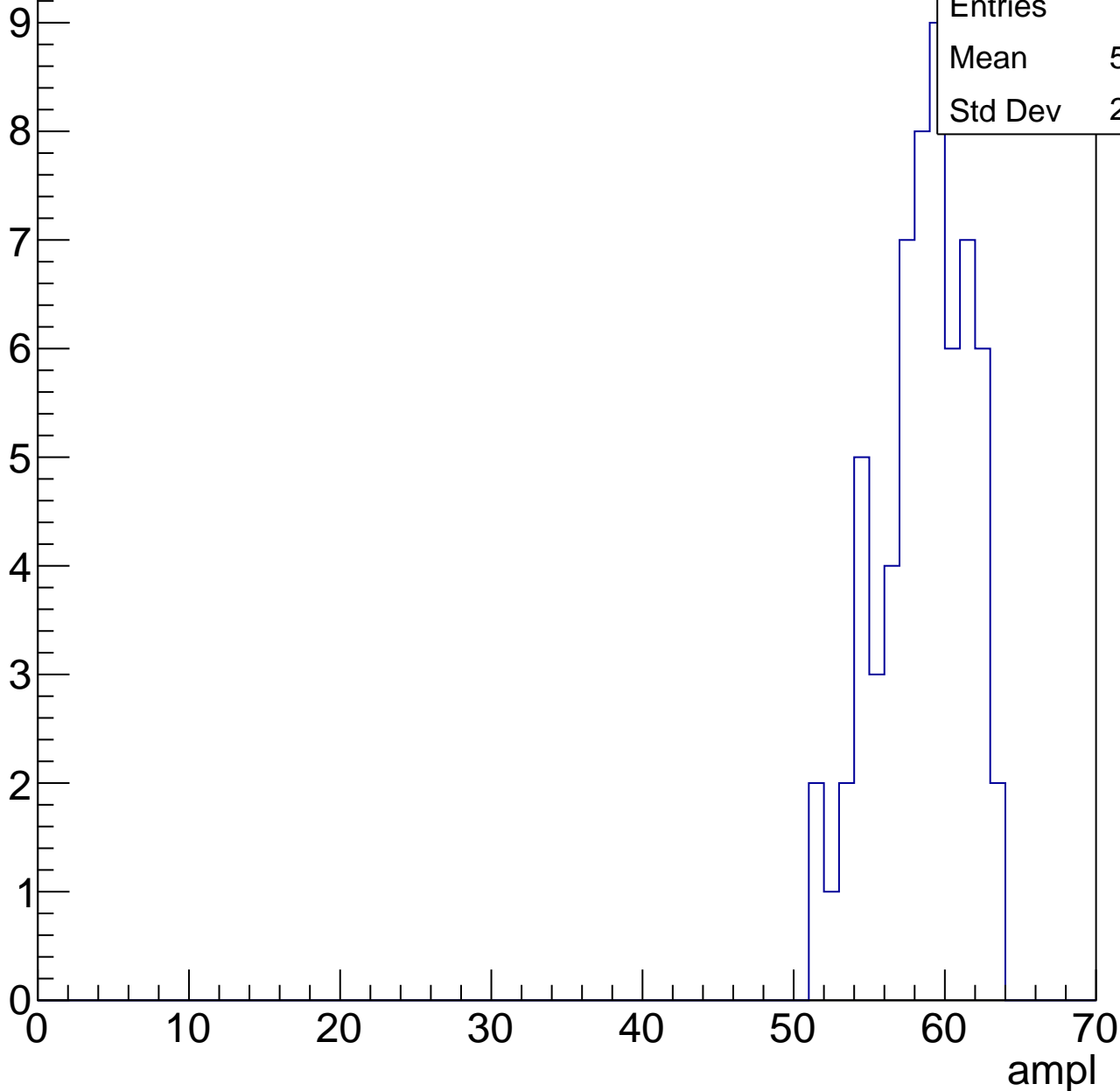


B1L103S, U5-ch10, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	58.03
Std Dev	2.994

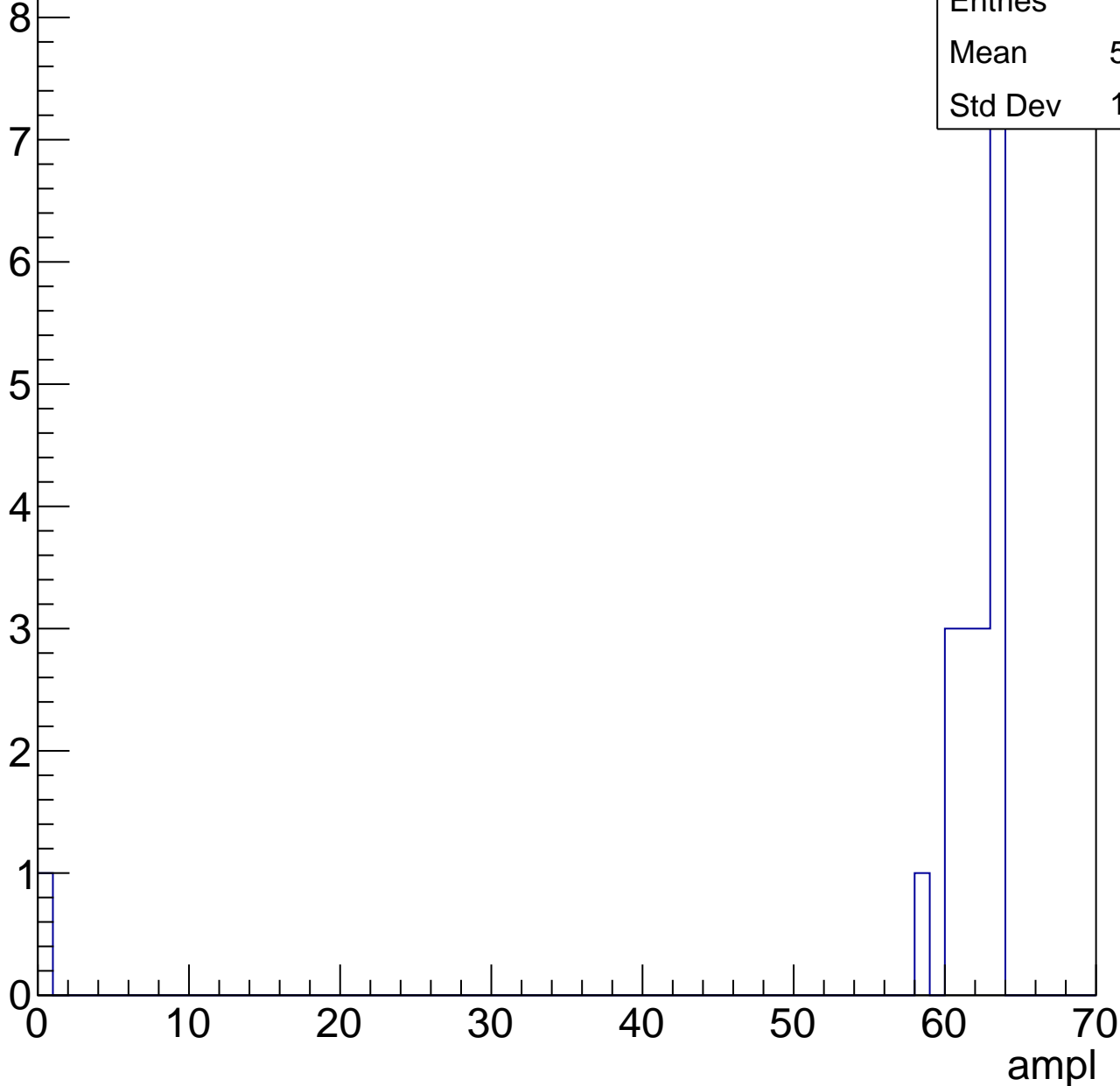


B1L103S, U5-ch10, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	19
Mean	58.47
Std Dev	13.85



B1L103S, U5-ch10, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U5-ch11, adc0

calib_packv5_041523_1651.root, FC#0, port C2

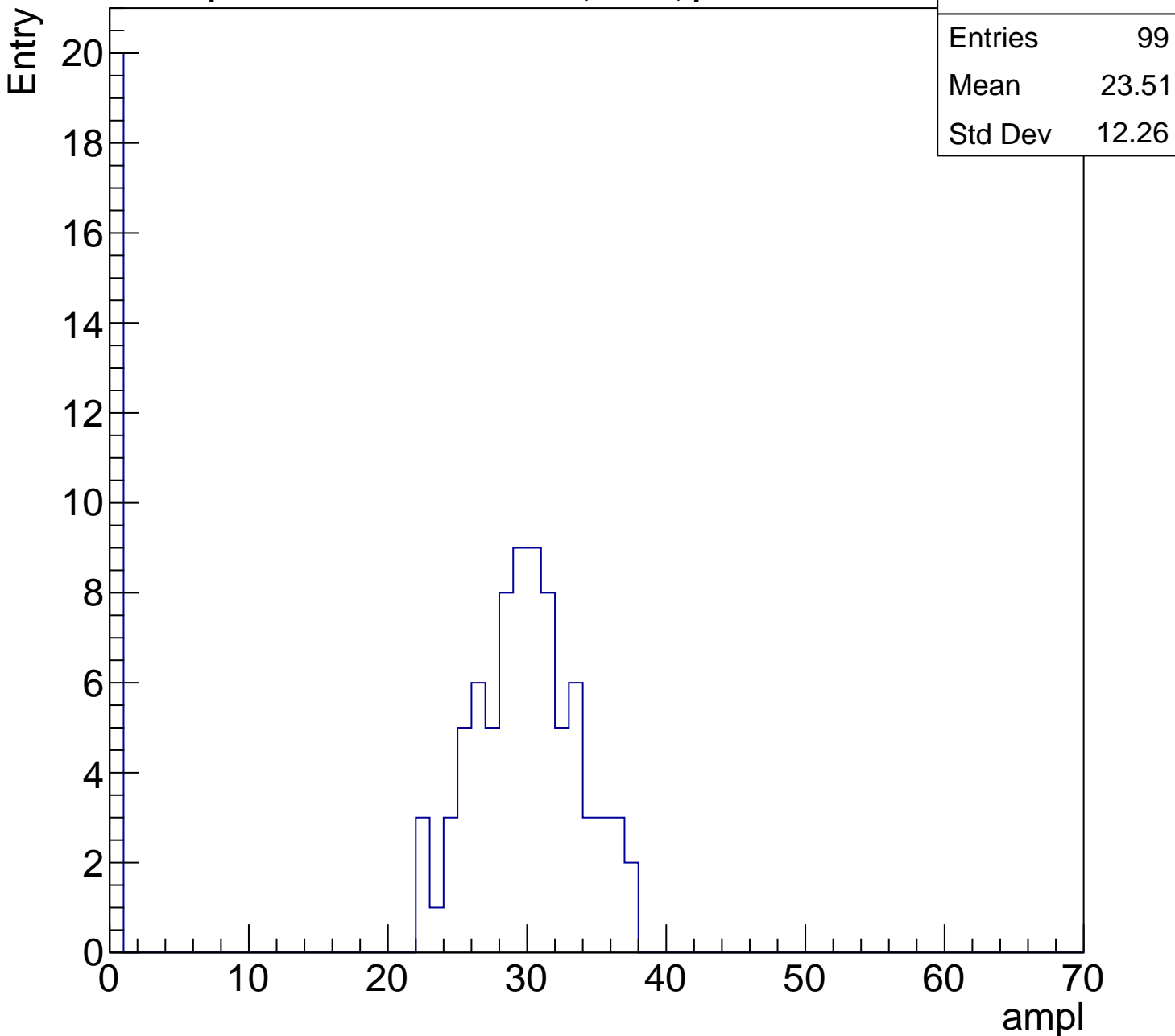
Entries	99
Mean	23.51
Std Dev	12.26

Entry

20
18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

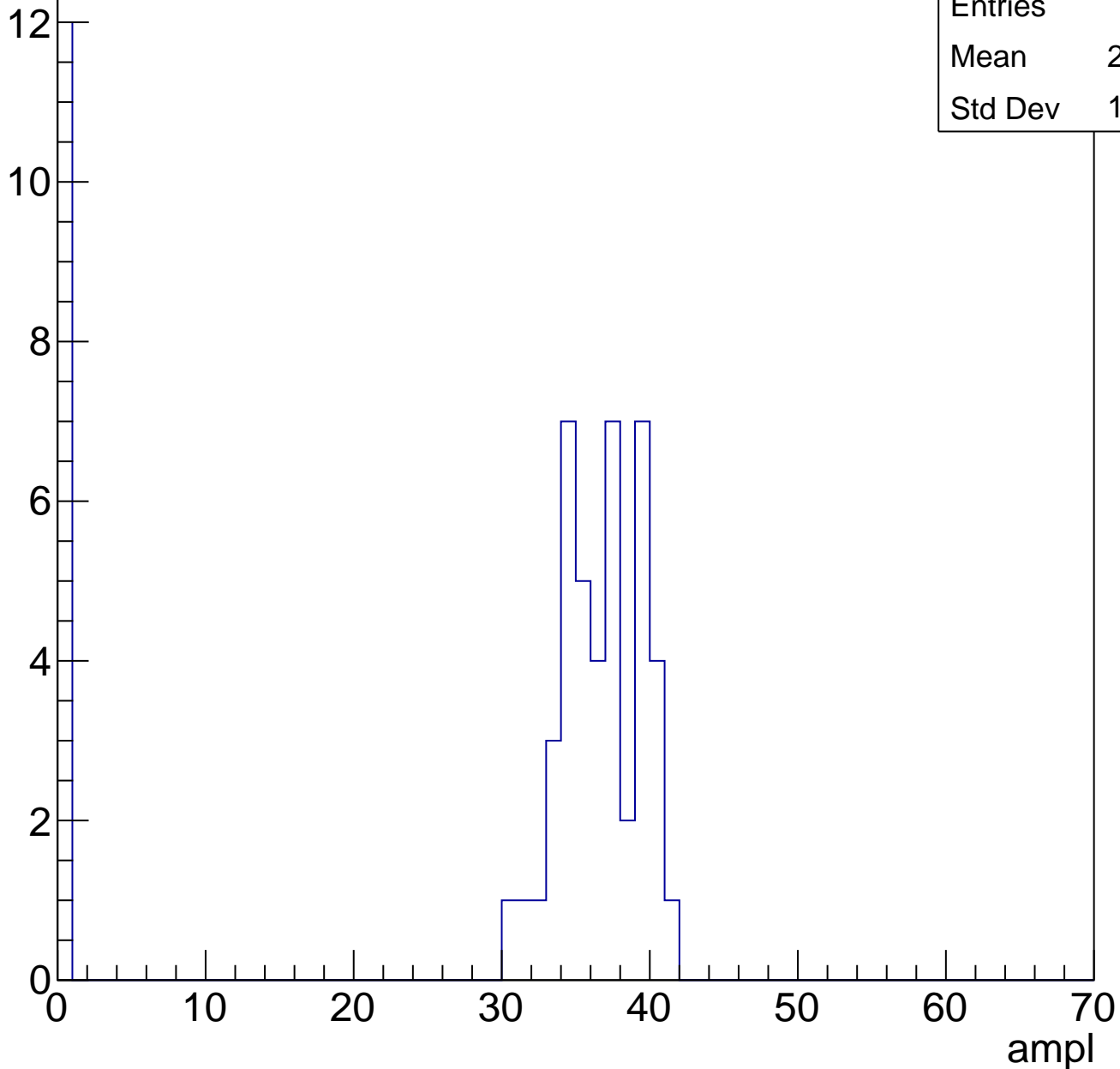


B1L103S, U5-ch11, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	55
Mean	28.33
Std Dev	15.15

Entry

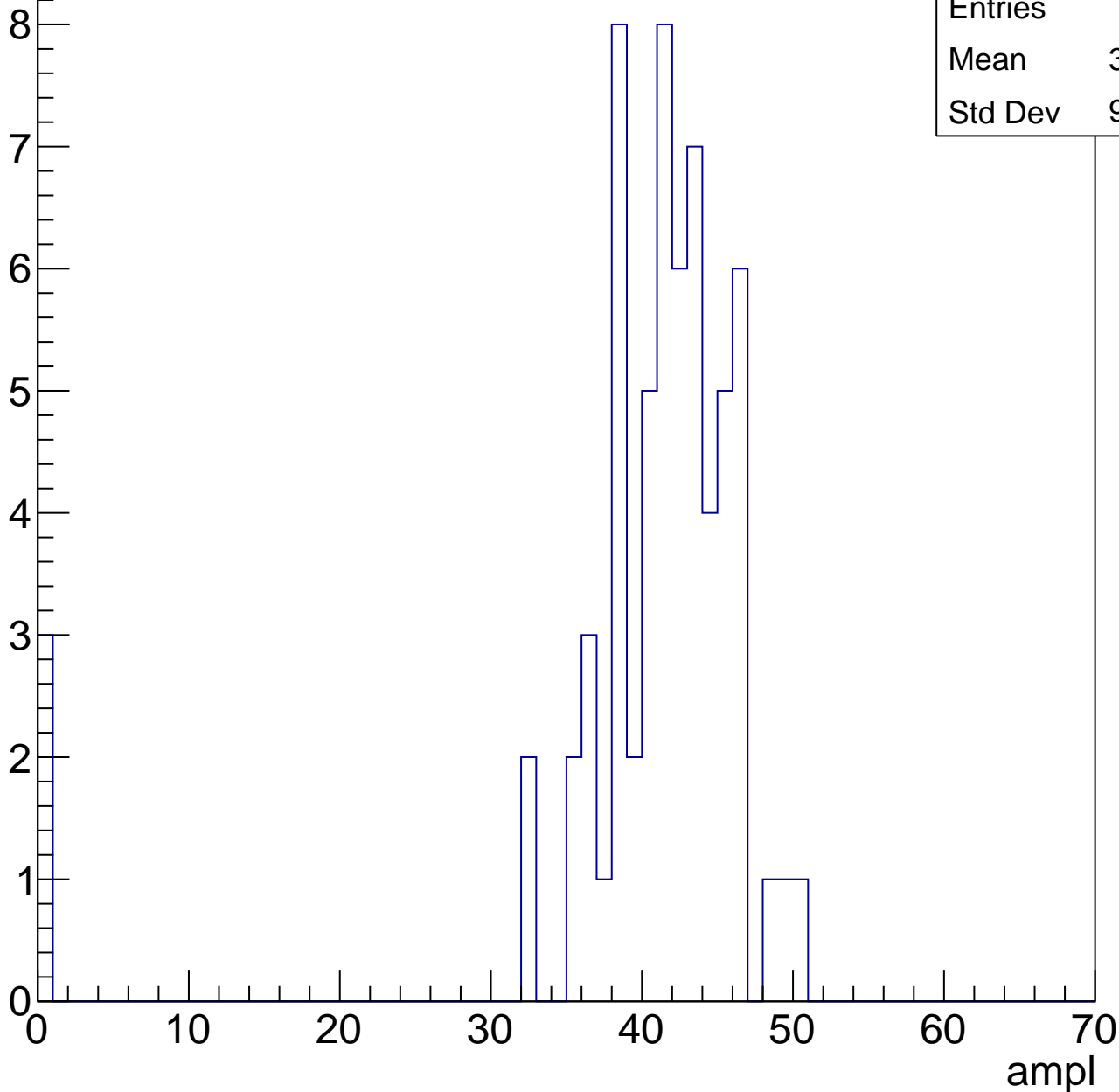


B1L103S, U5-ch11, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	39.48
Std Dev	9.443

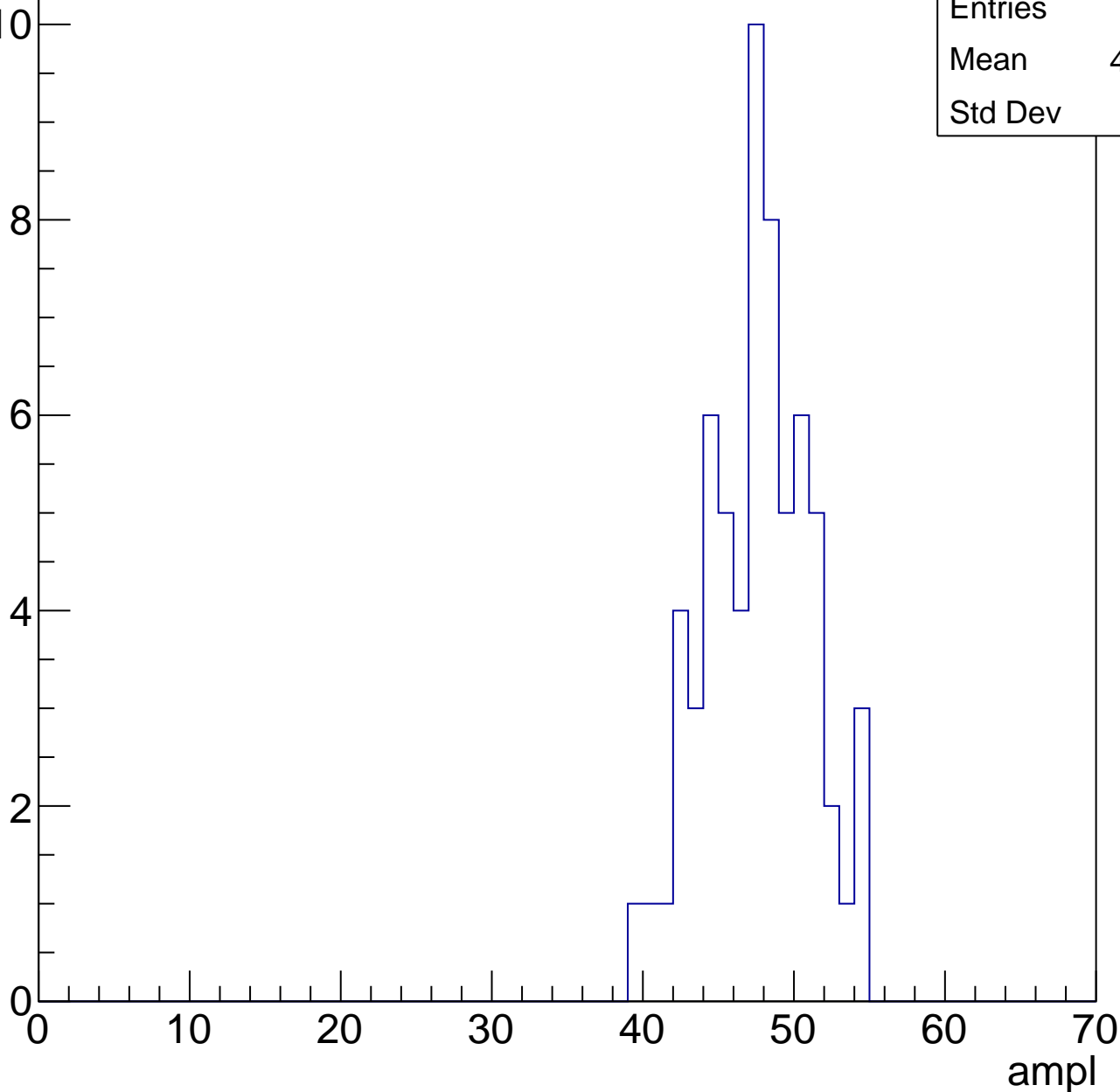


B1L103S, U5-ch11, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	47.12
Std Dev	3.44

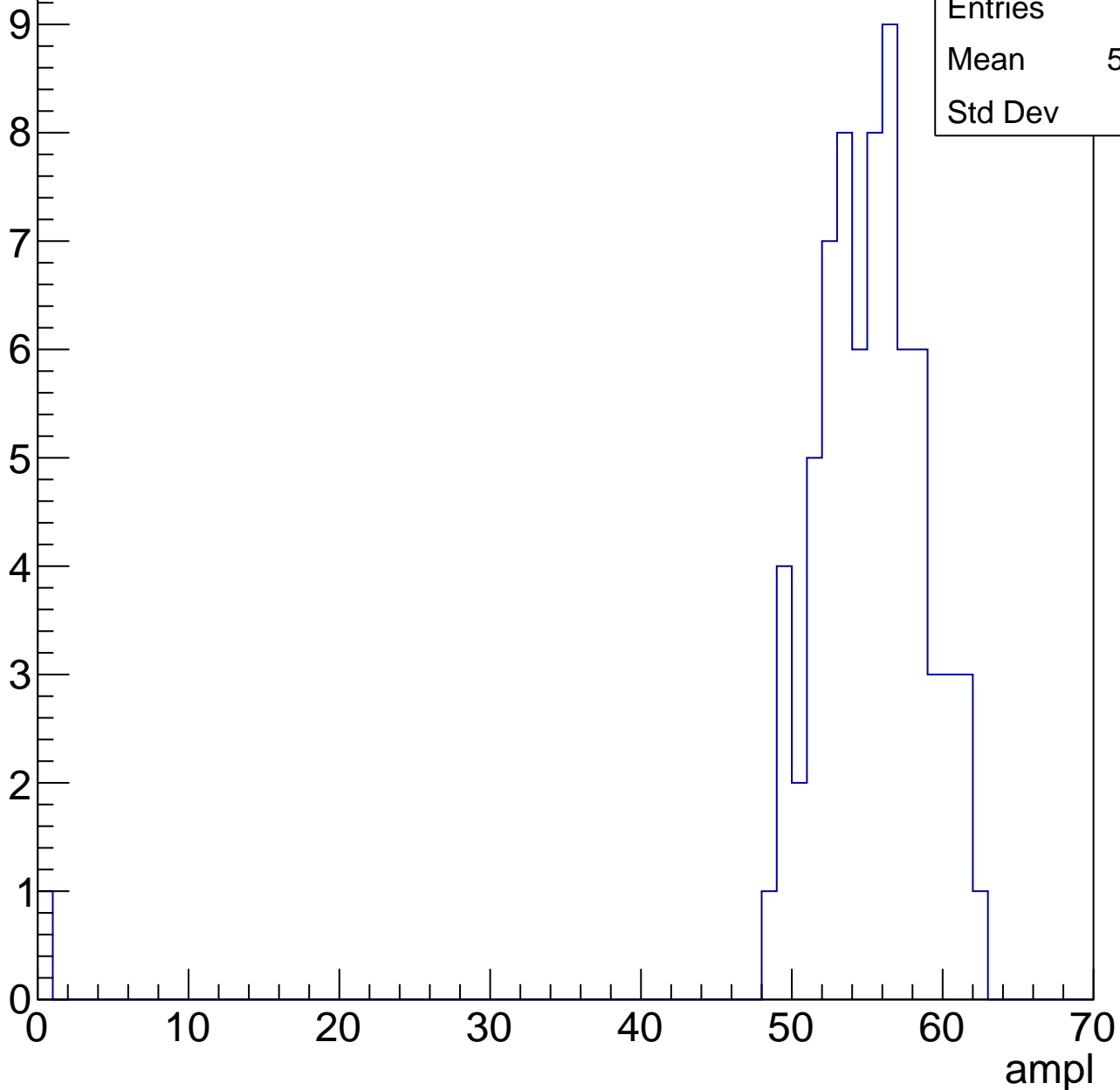


B1L103S, U5-ch11, adc4

calib_packv5_041523_1651.root, FC#0, port C2

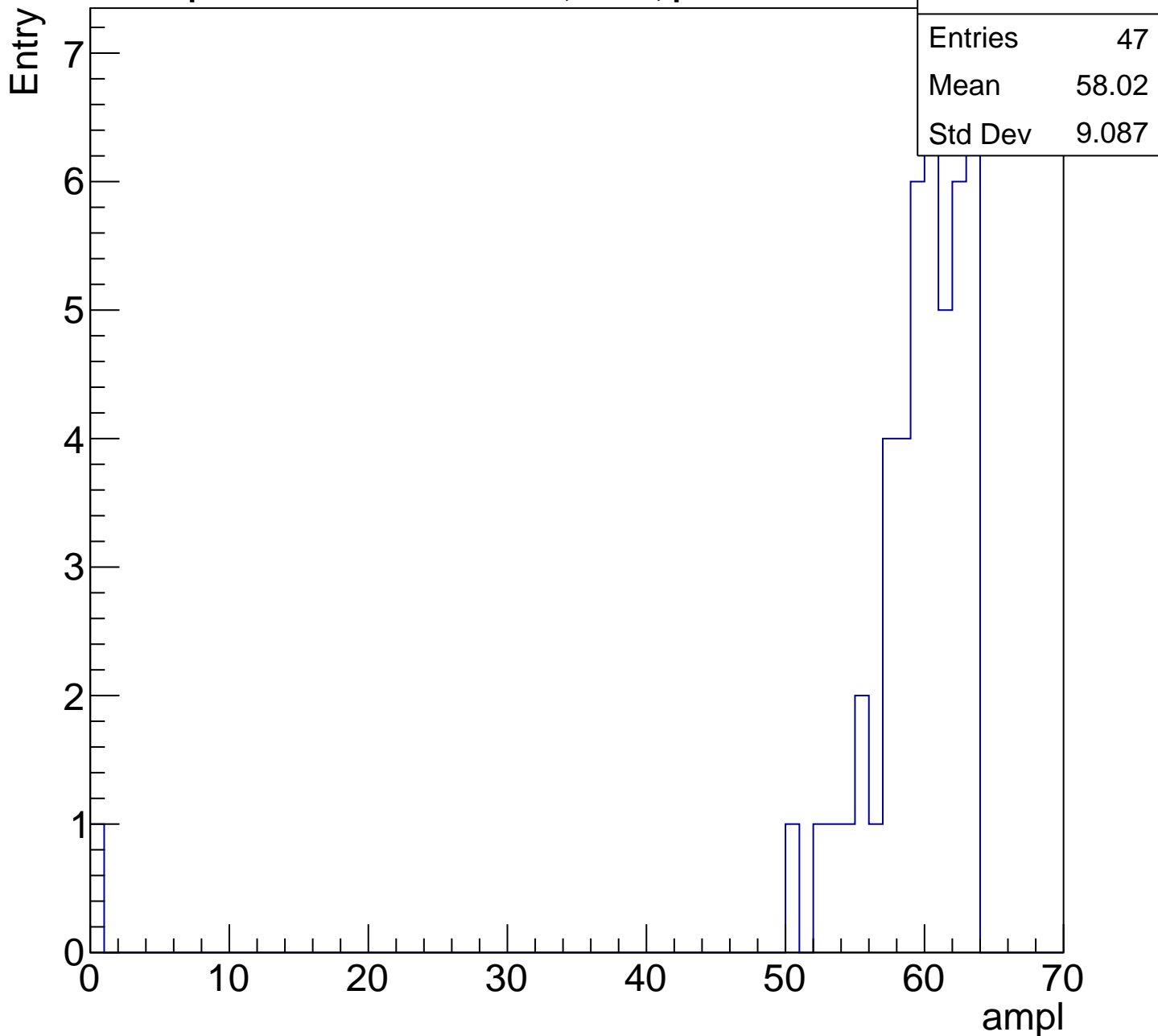
Entry

Entries	73
Mean	54.07
Std Dev	7.17



B1L103S, U5-ch11, adc5

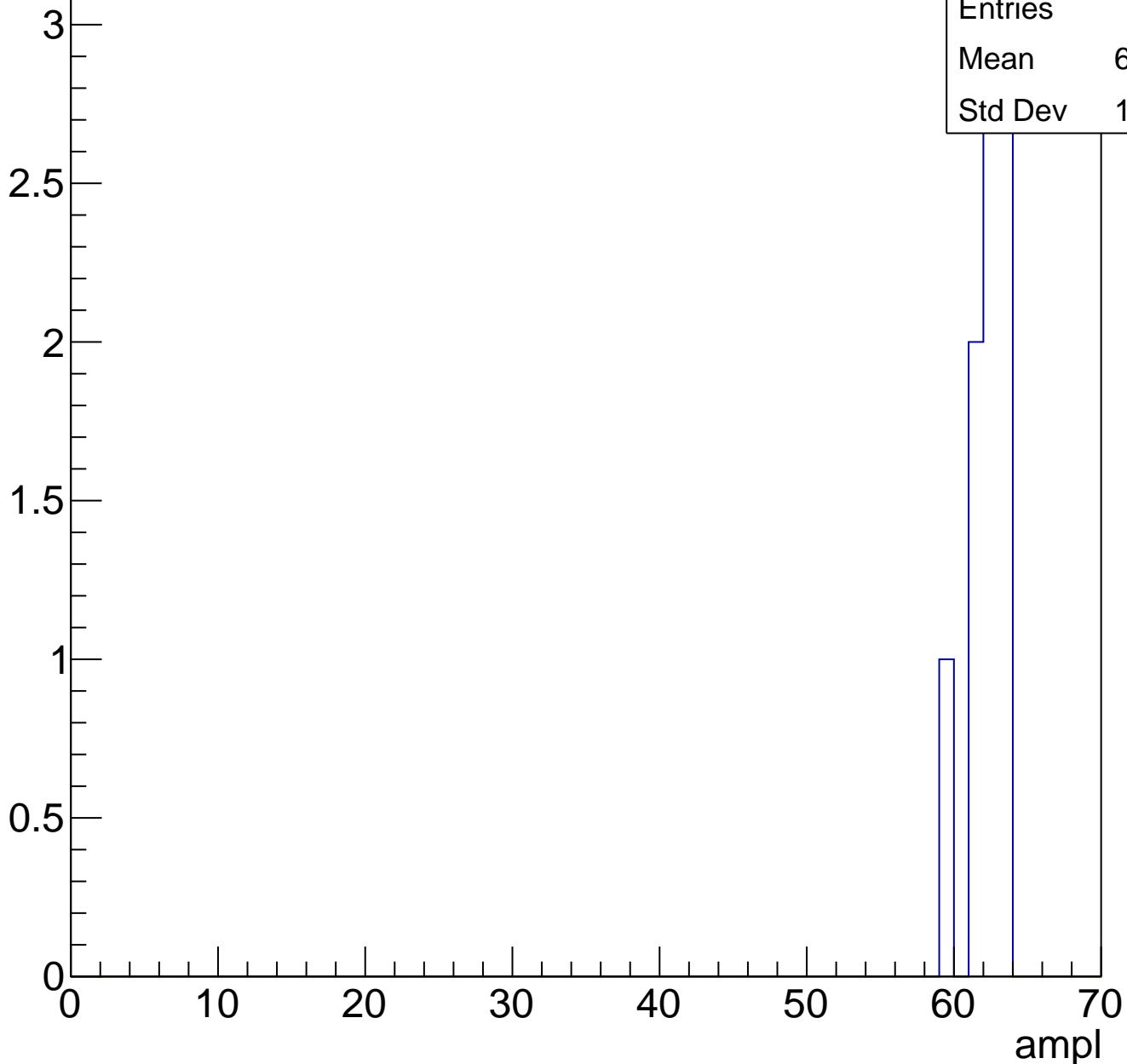
calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U5-ch11, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch11, adc7

calib_packv5_041523_1651.root, FC#0, port C2

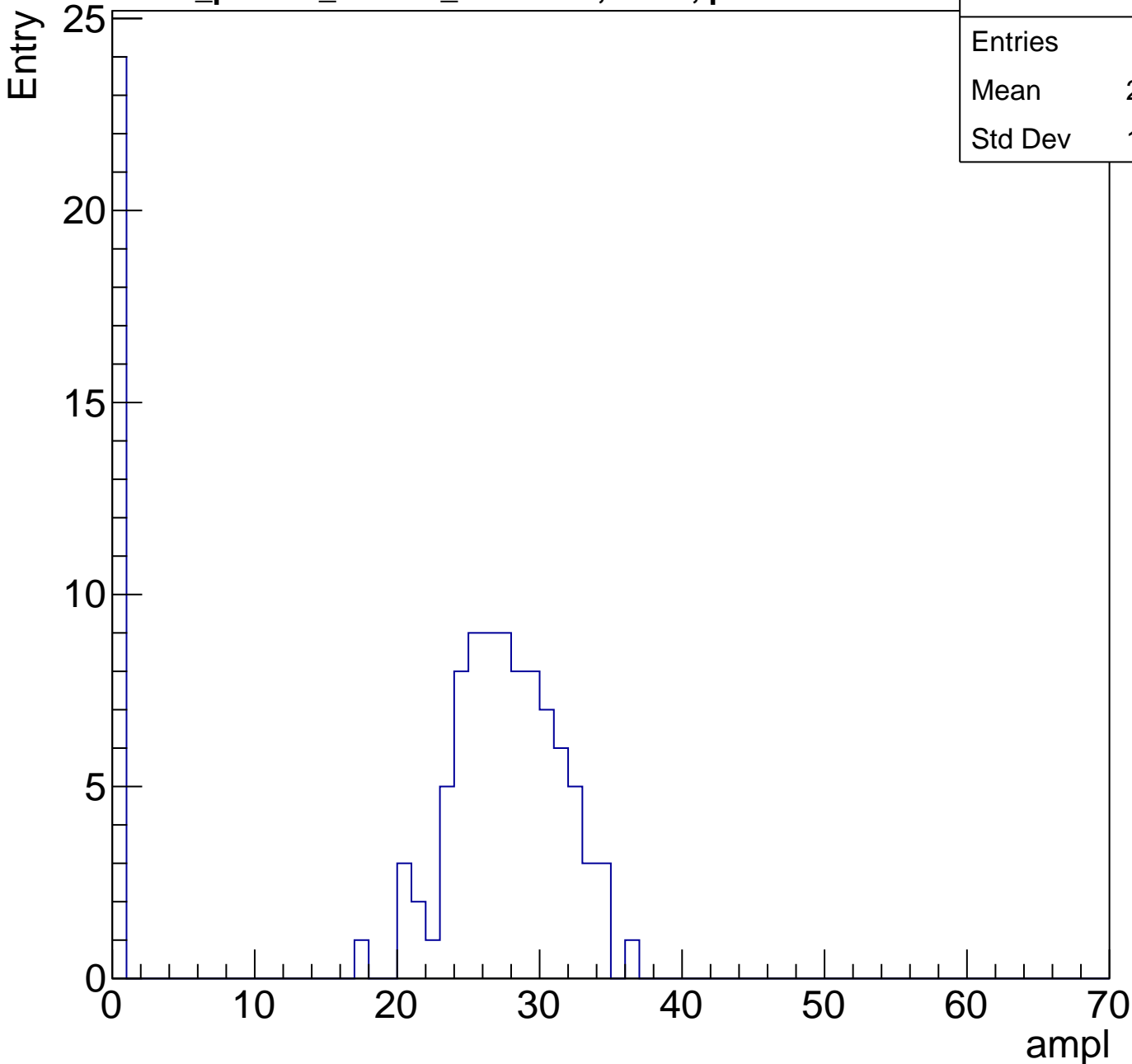
Entry



B1L103S, U5-ch12, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	112
Mean	21.42
Std Dev	11.65

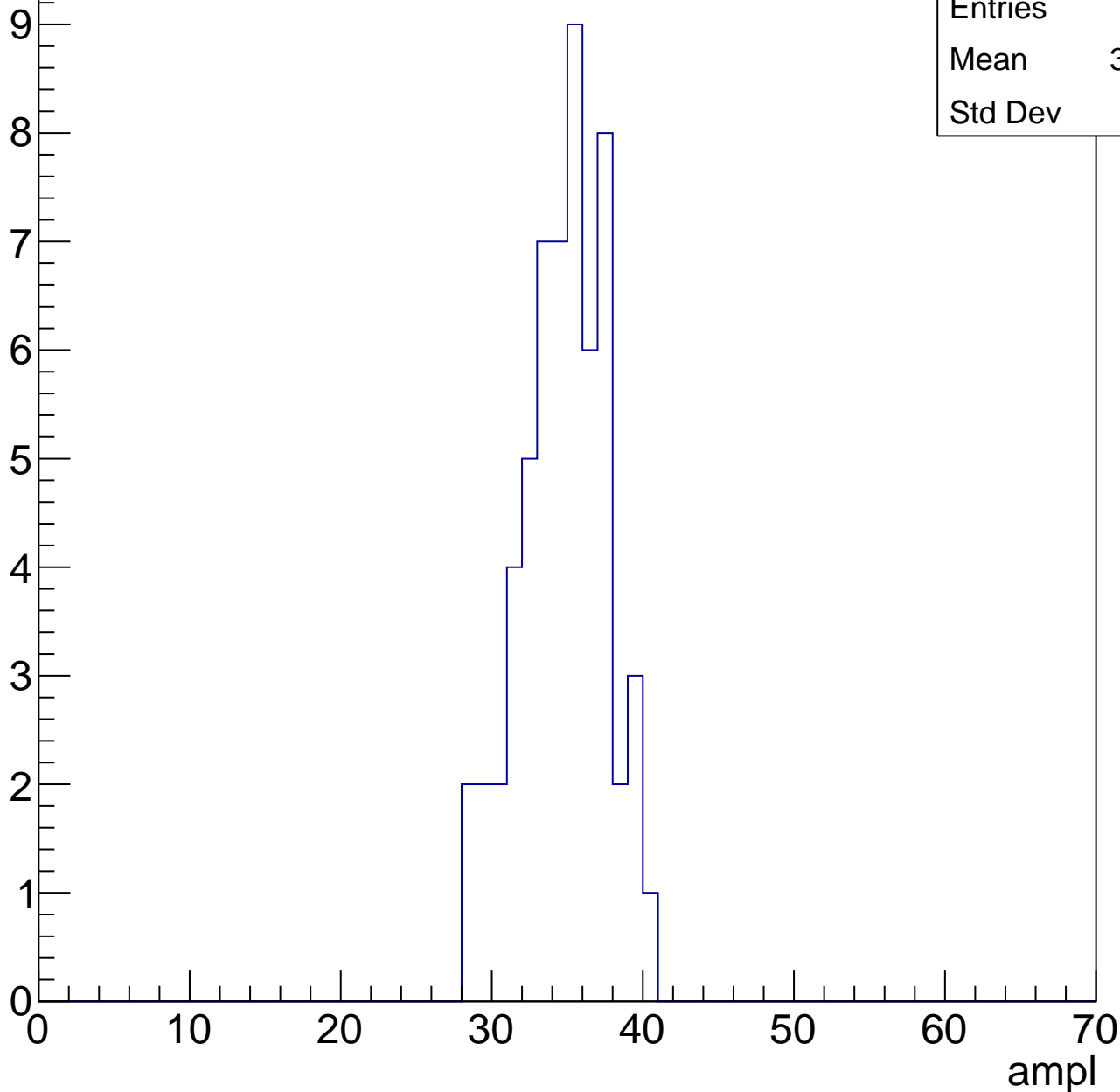


B1L103S, U5-ch12, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	34.26
Std Dev	2.82

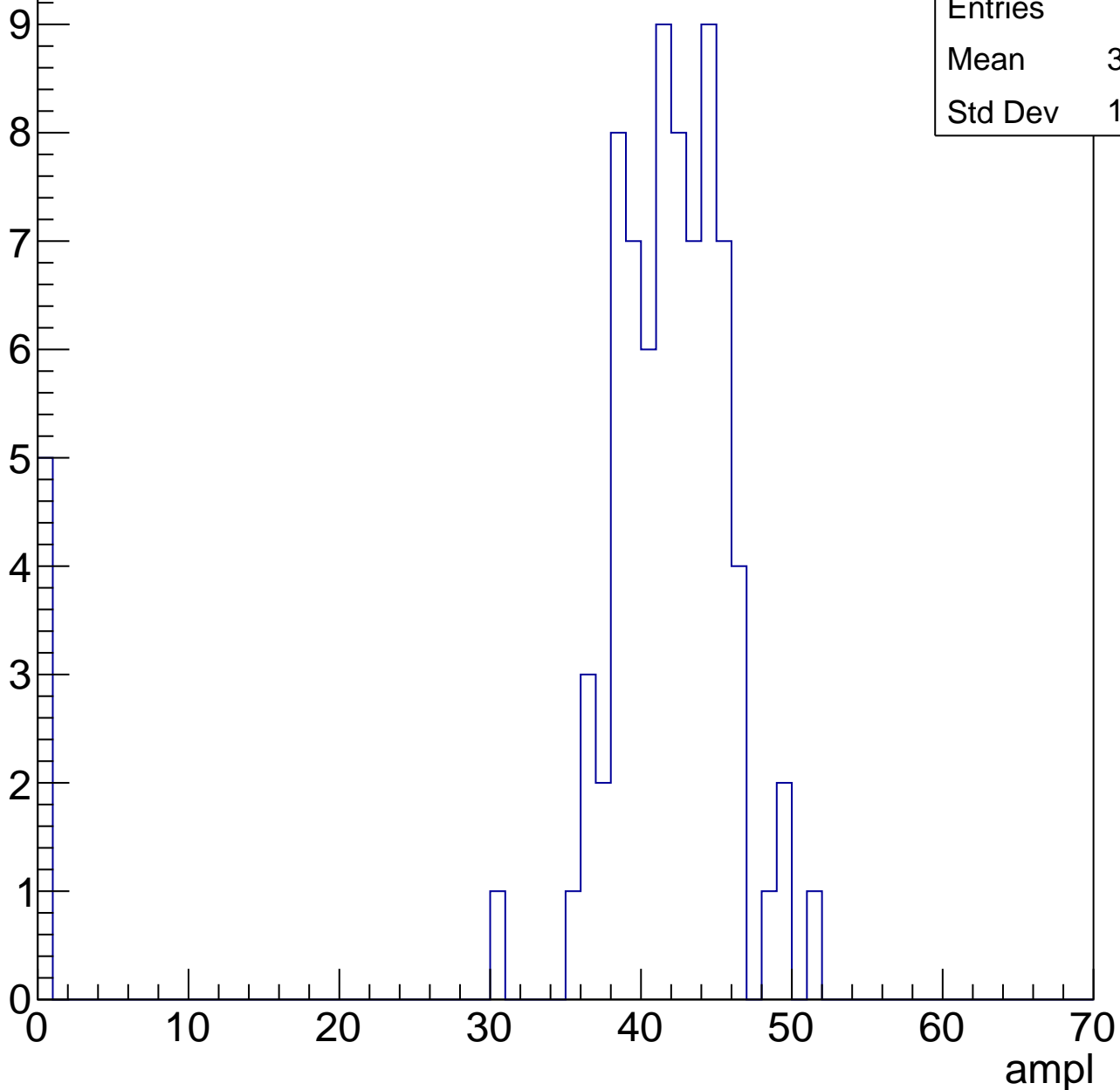


B1L103S, U5-ch12, adc2

calib_packv5_041523_1651.root, FC#0, port C2

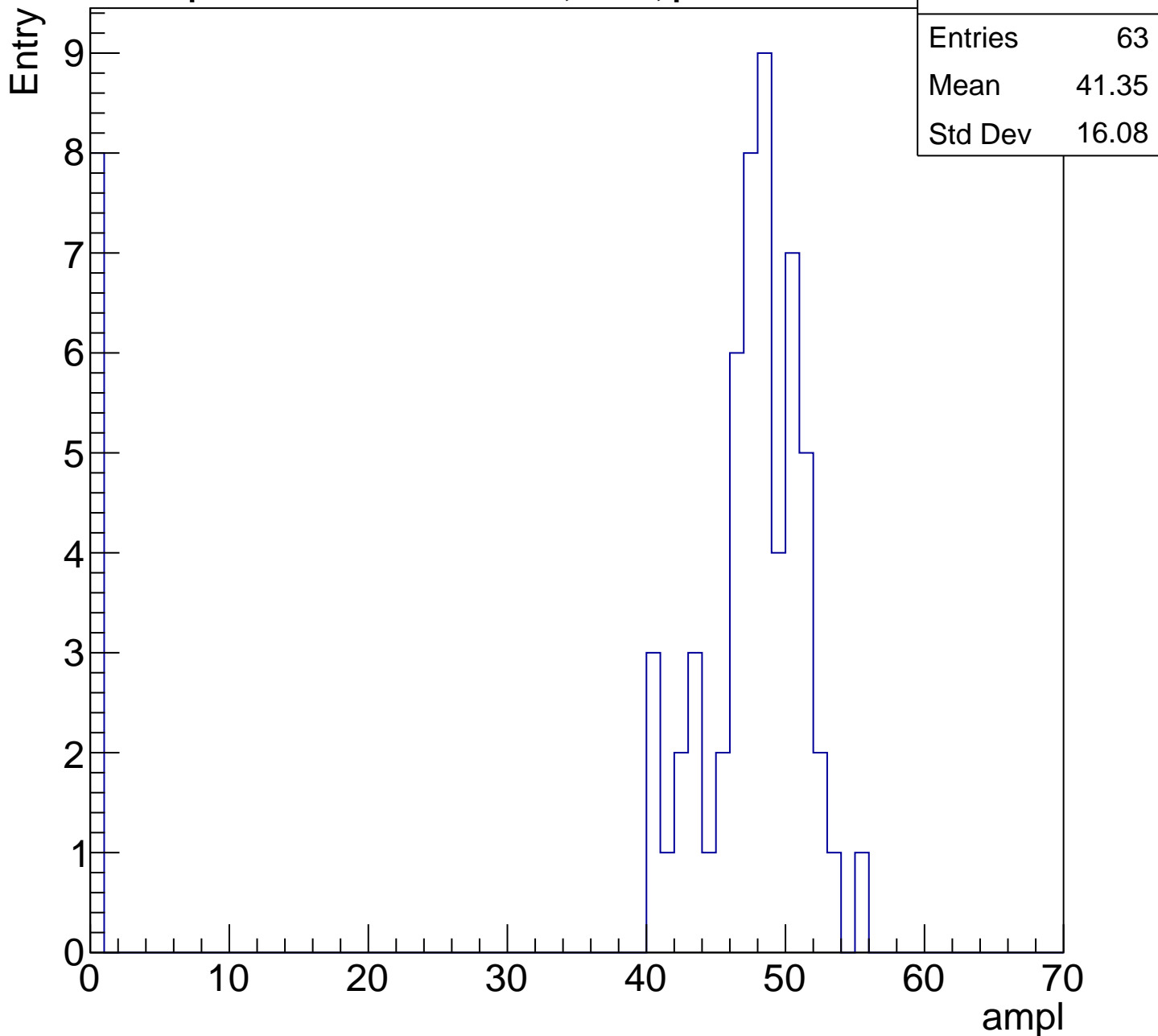
Entry

Entries	81
Mean	39.04
Std Dev	10.58



B1L103S, U5-ch12, adc3

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U5-ch12, adc4

calib_packv5_041523_1651.root, FC#0, port C2

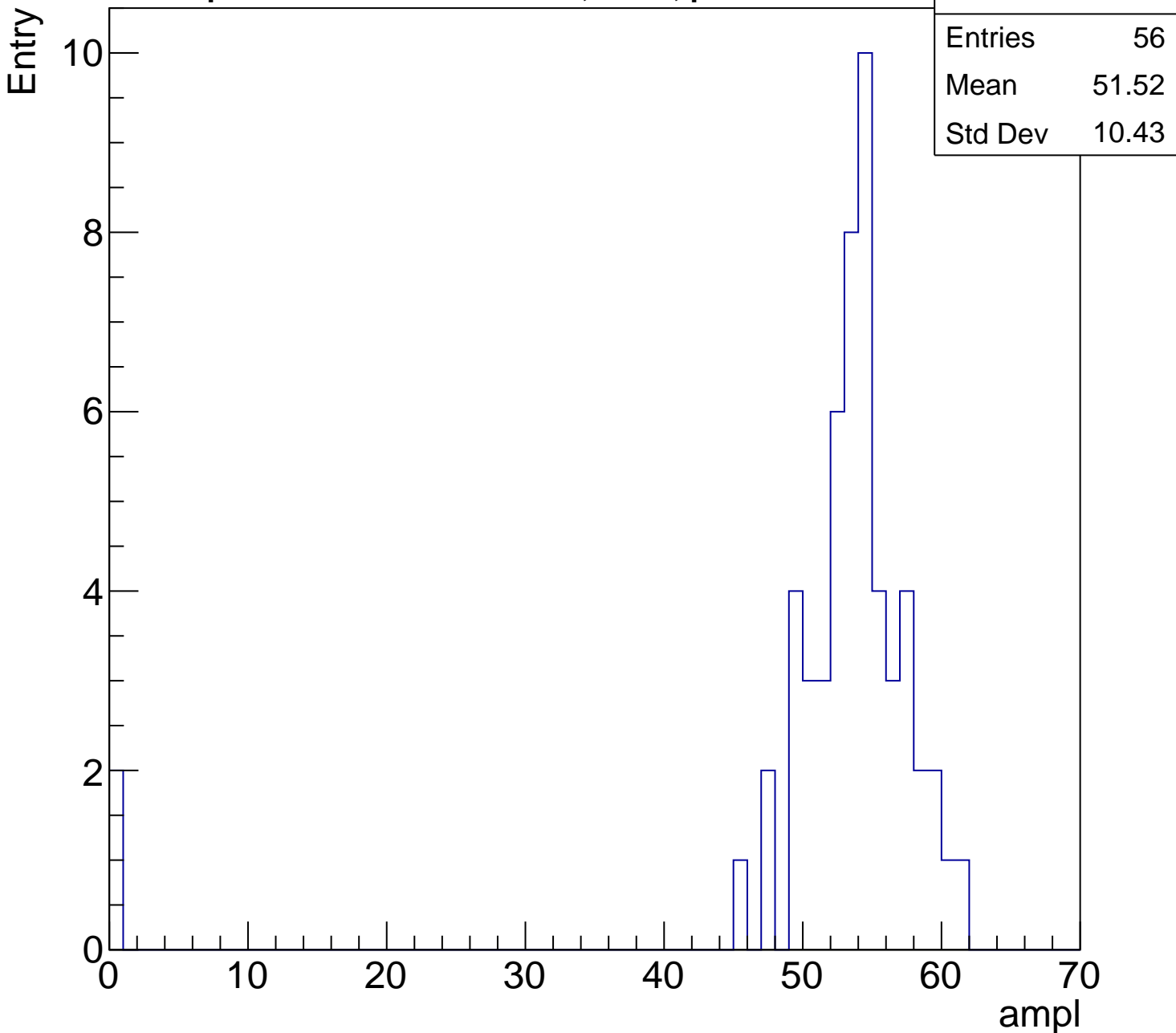
Entries	56
Mean	51.52
Std Dev	10.43

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

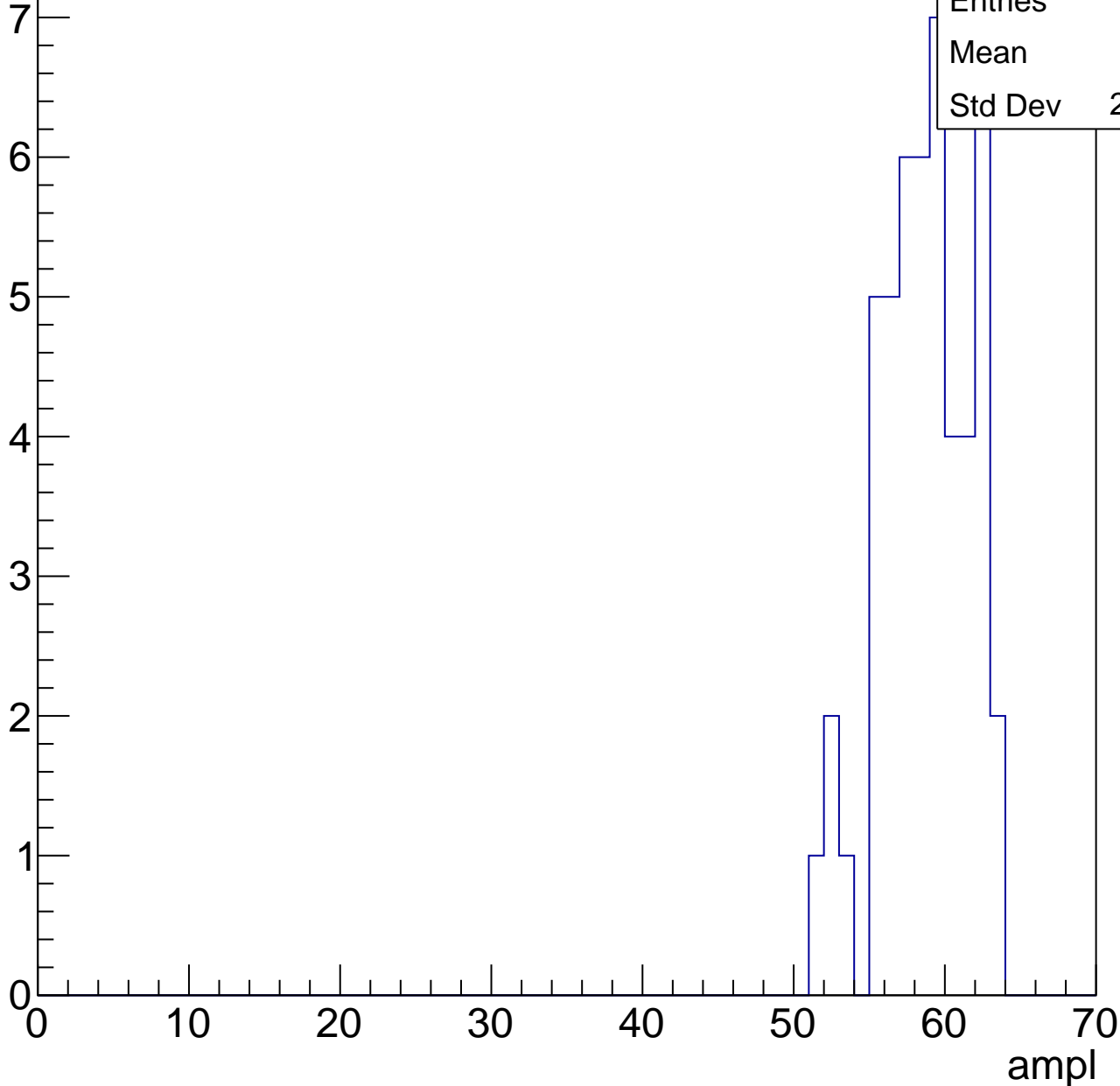


B1L103S, U5-ch12, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	58.2
Std Dev	2.953

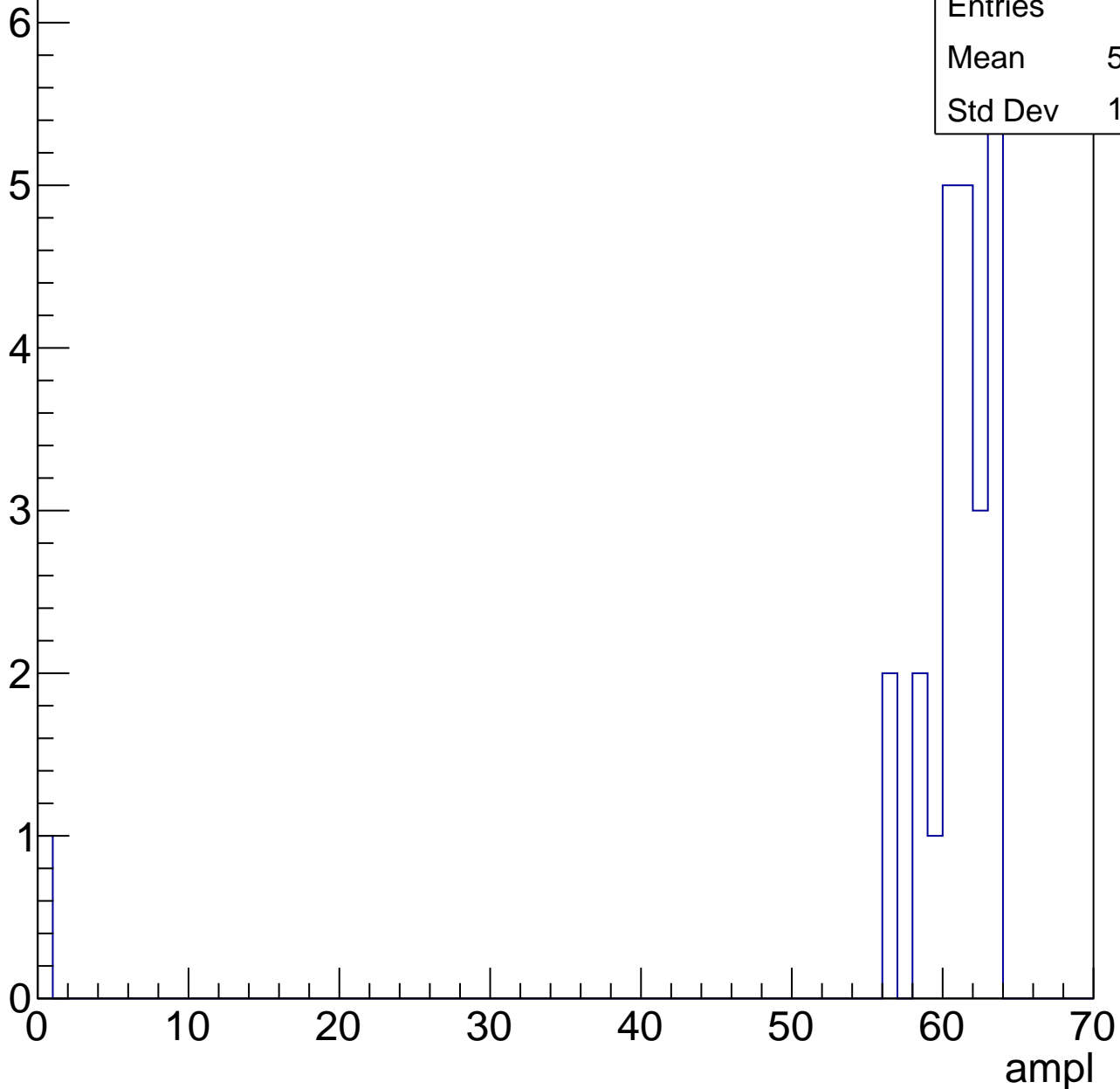


B1L103S, U5-ch12, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	25
Mean	58.24
Std Dev	12.06



B1L103S, U5-ch12, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

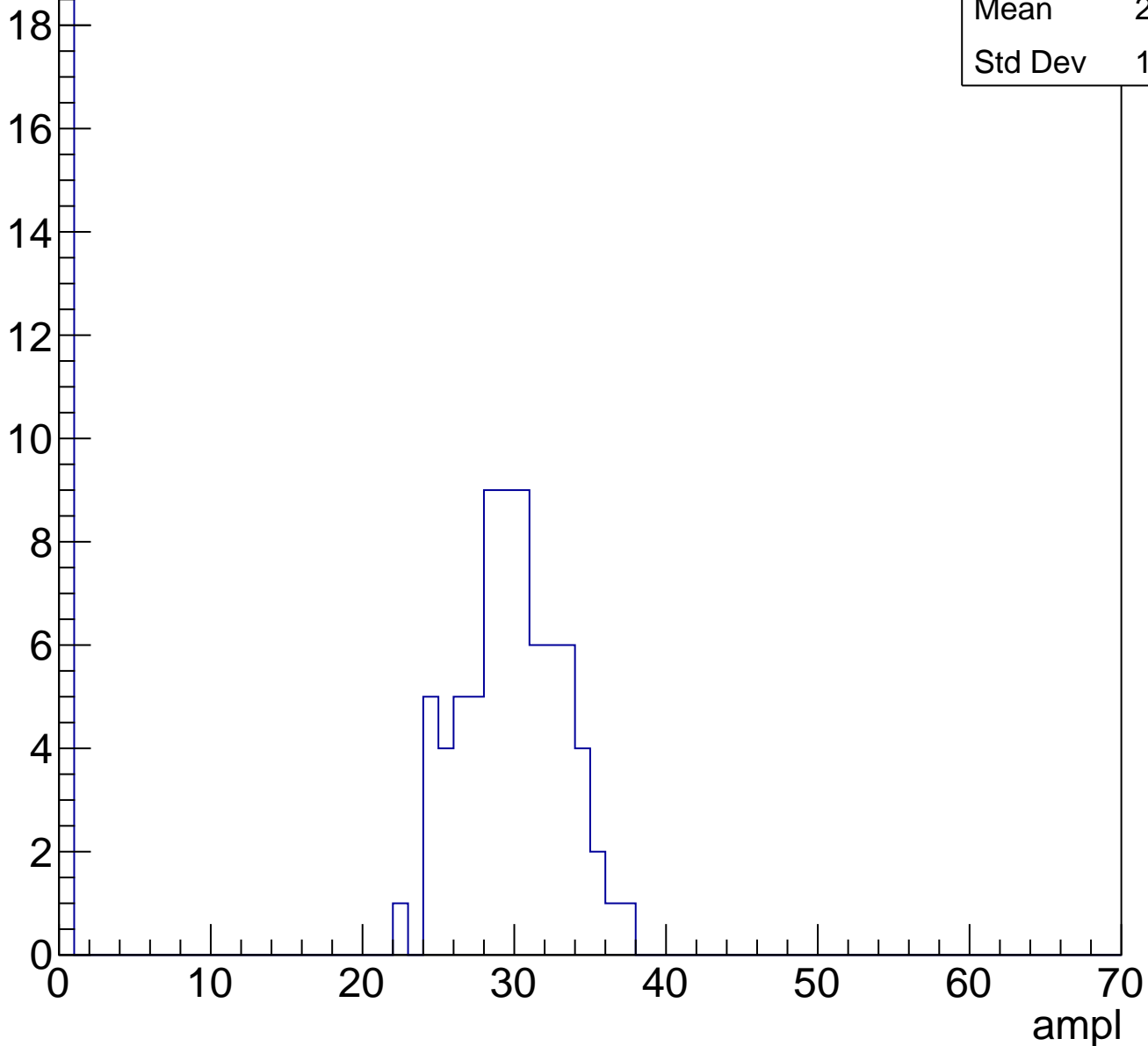


B1L103S, U5-ch13, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	92
Mean	23.32
Std Dev	12.24

Entry

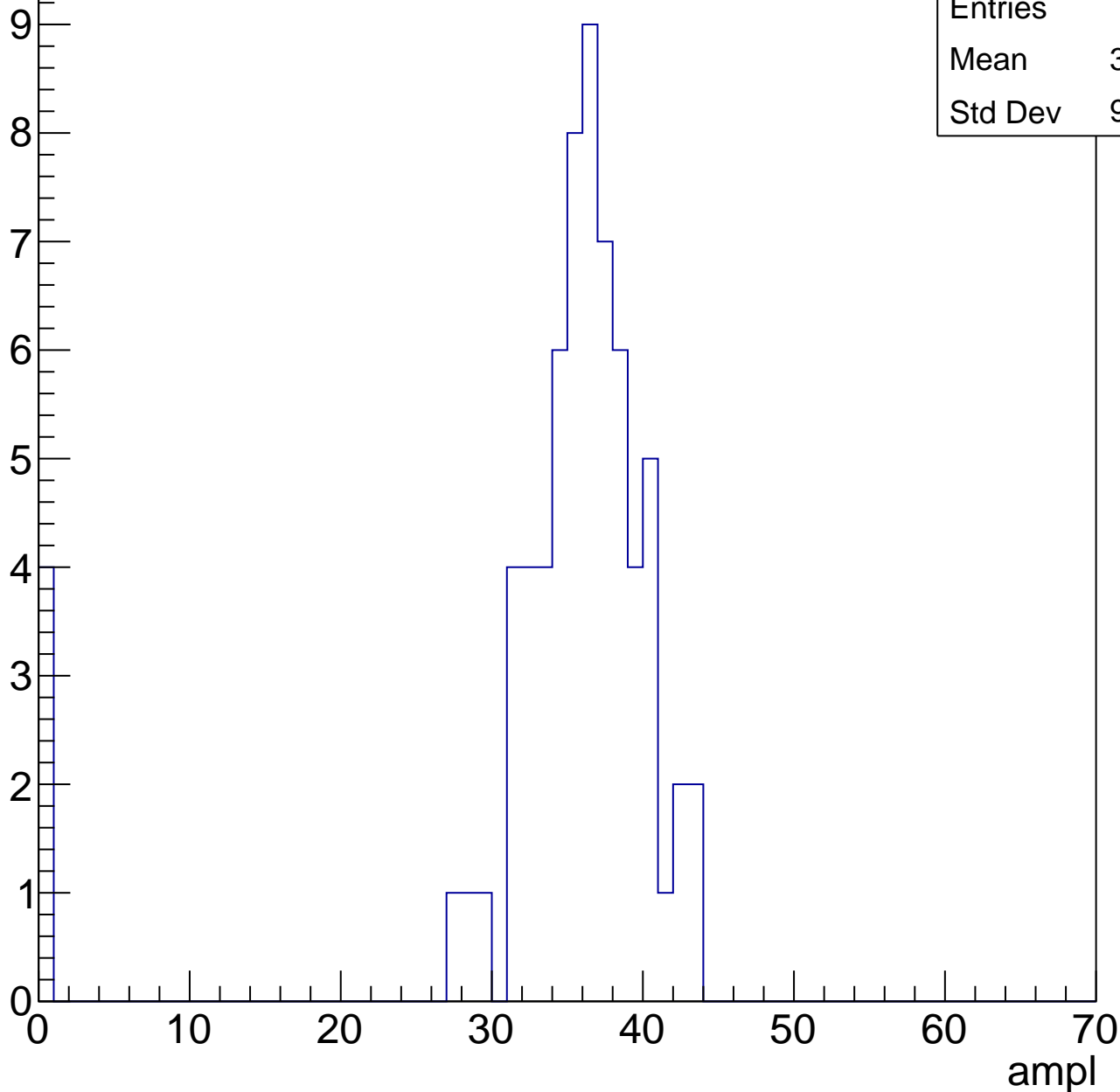


B1L103S, U5-ch13, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	33.77
Std Dev	9.016



B1L103S, U5-ch13, adc2

calib_packv5_041523_1651.root, FC#0, port C2

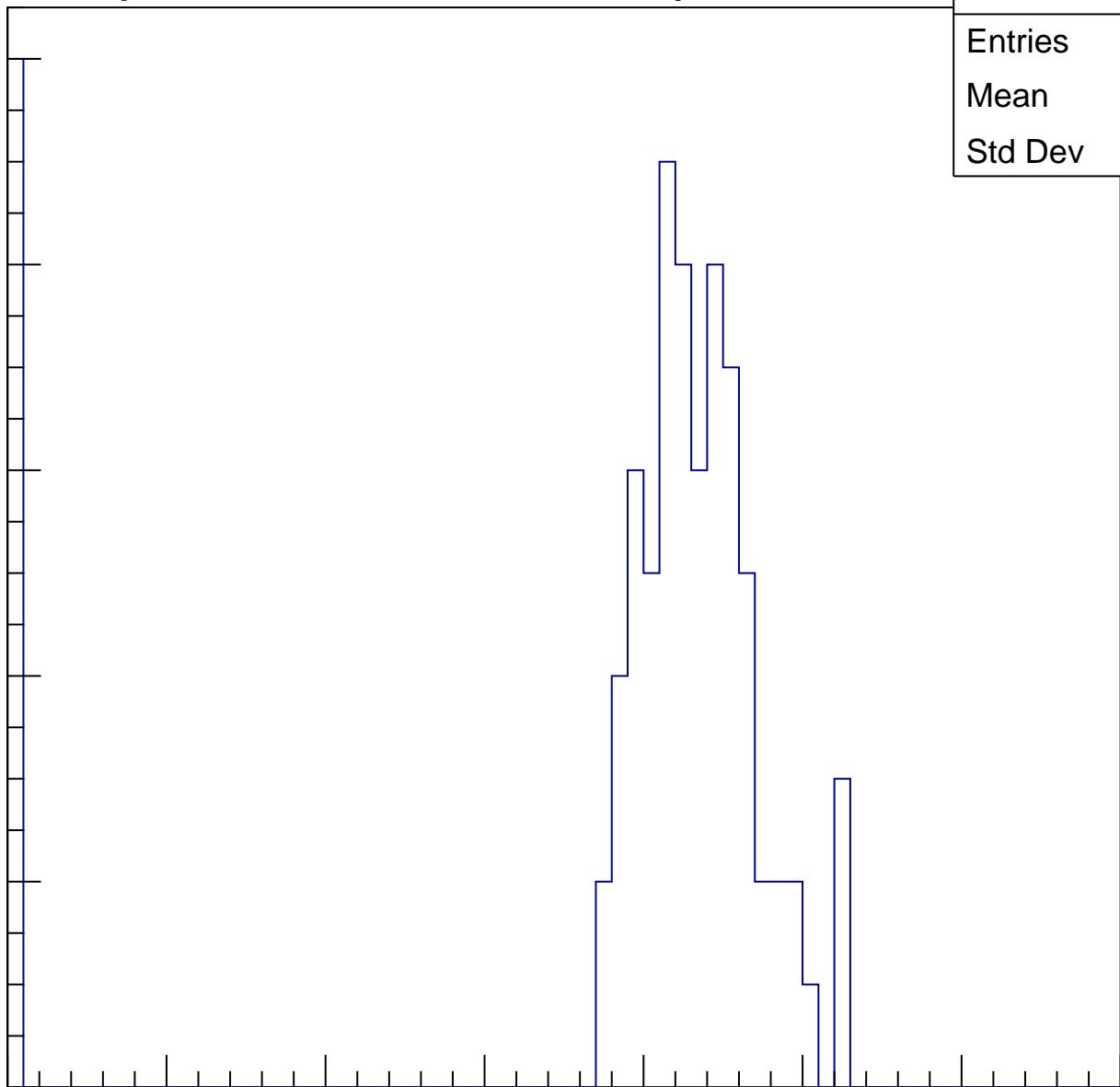
Entries	80
Mean	37.67
Std Dev	14.62

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl



B1L103S, U5-ch13, adc3

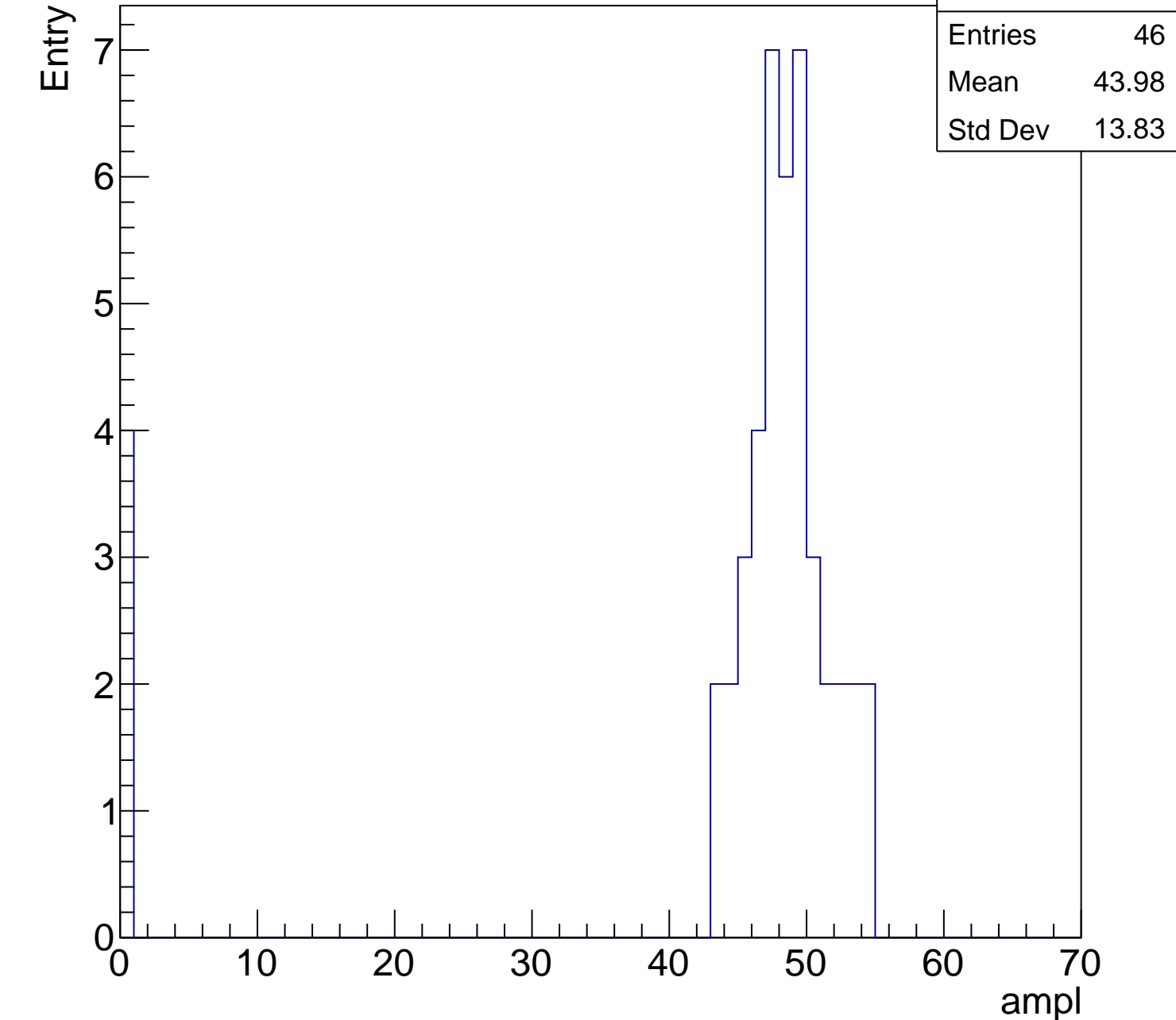
calib_packv5_041523_1651.root, FC#0, port C2

Entry

7
6
5
4
3
2
1
0

Entries	46
Mean	43.98
Std Dev	13.83

ampl

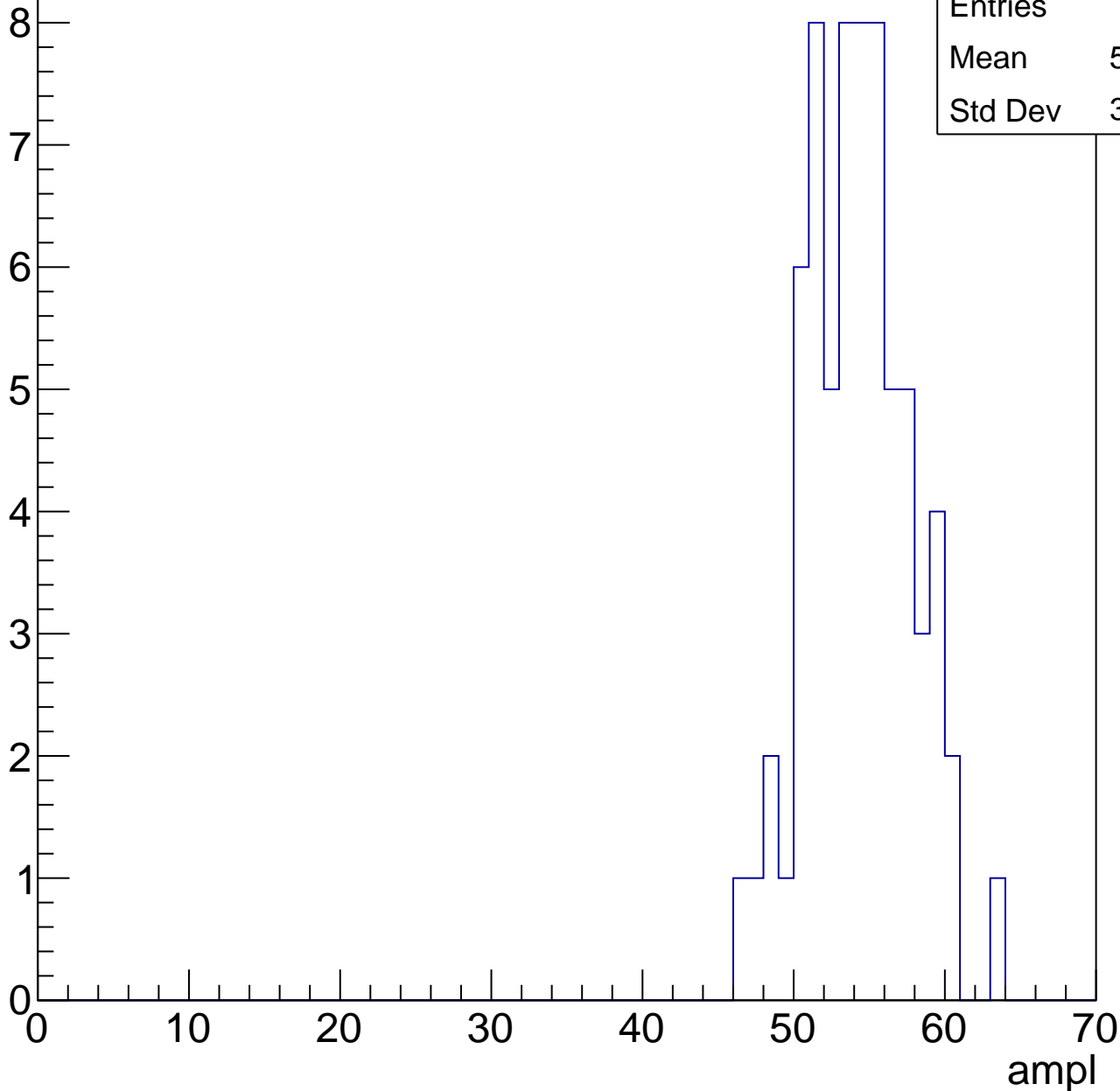


B1L103S, U5-ch13, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	53.82
Std Dev	3.382

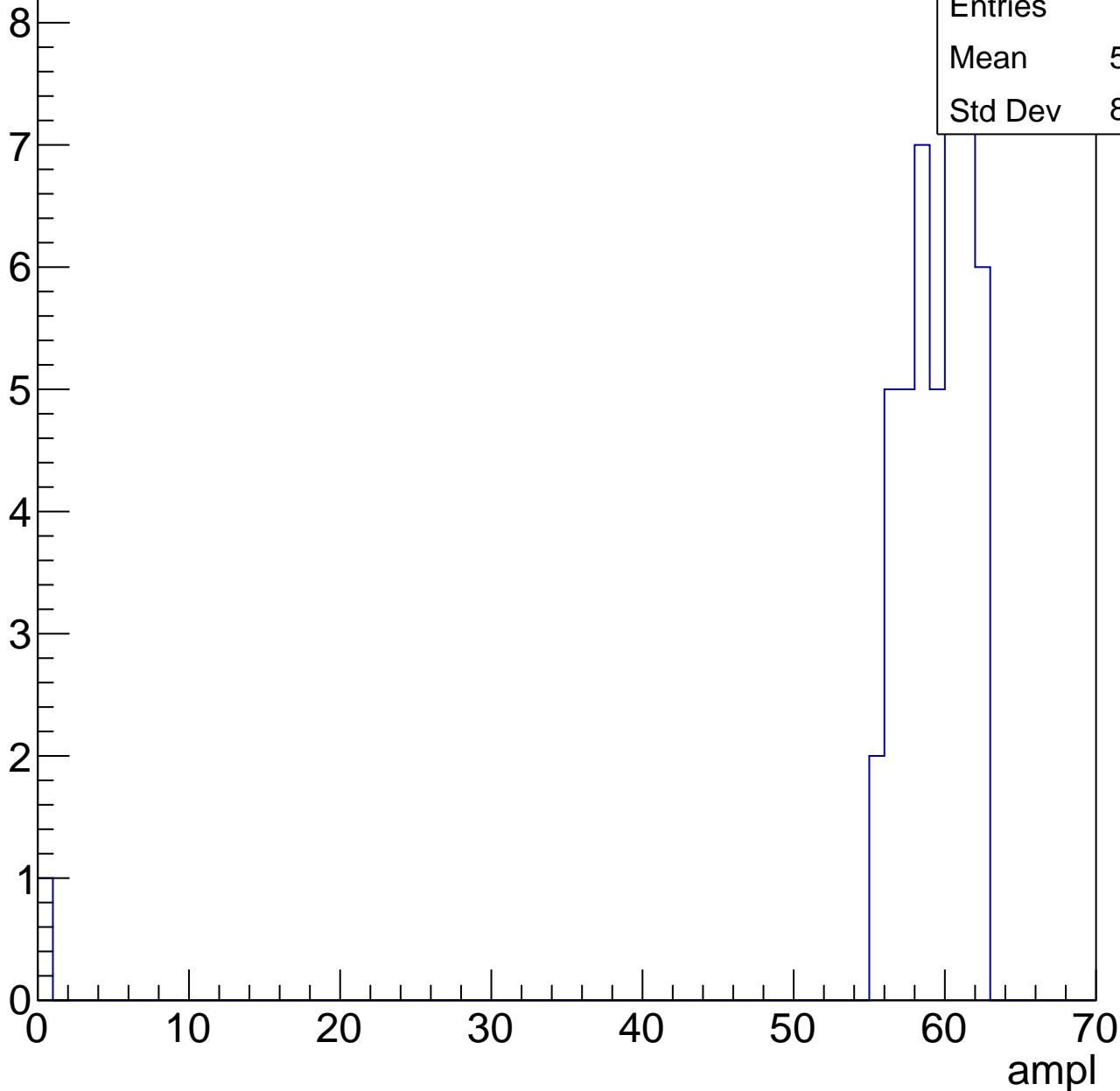


B1L103S, U5-ch13, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	47
Mean	57.79
Std Dev	8.764

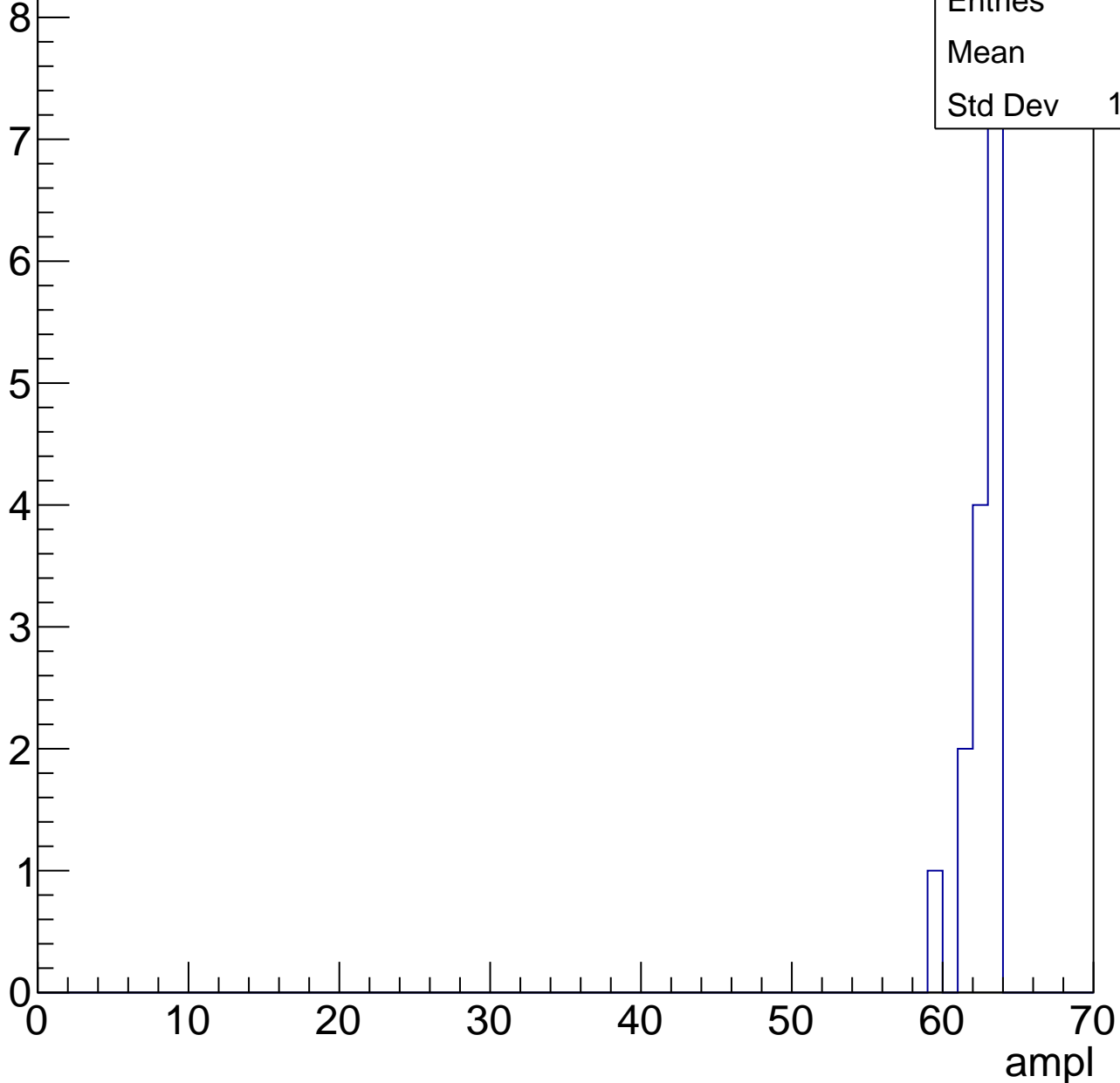


B1L103S, U5-ch13, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	15
Mean	62.2
Std Dev	1.108



B1L103S, U5-ch13, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry



B1L103S, U5-ch14, adc0

calib_packv5_041523_1651.root, FC#0, port C2

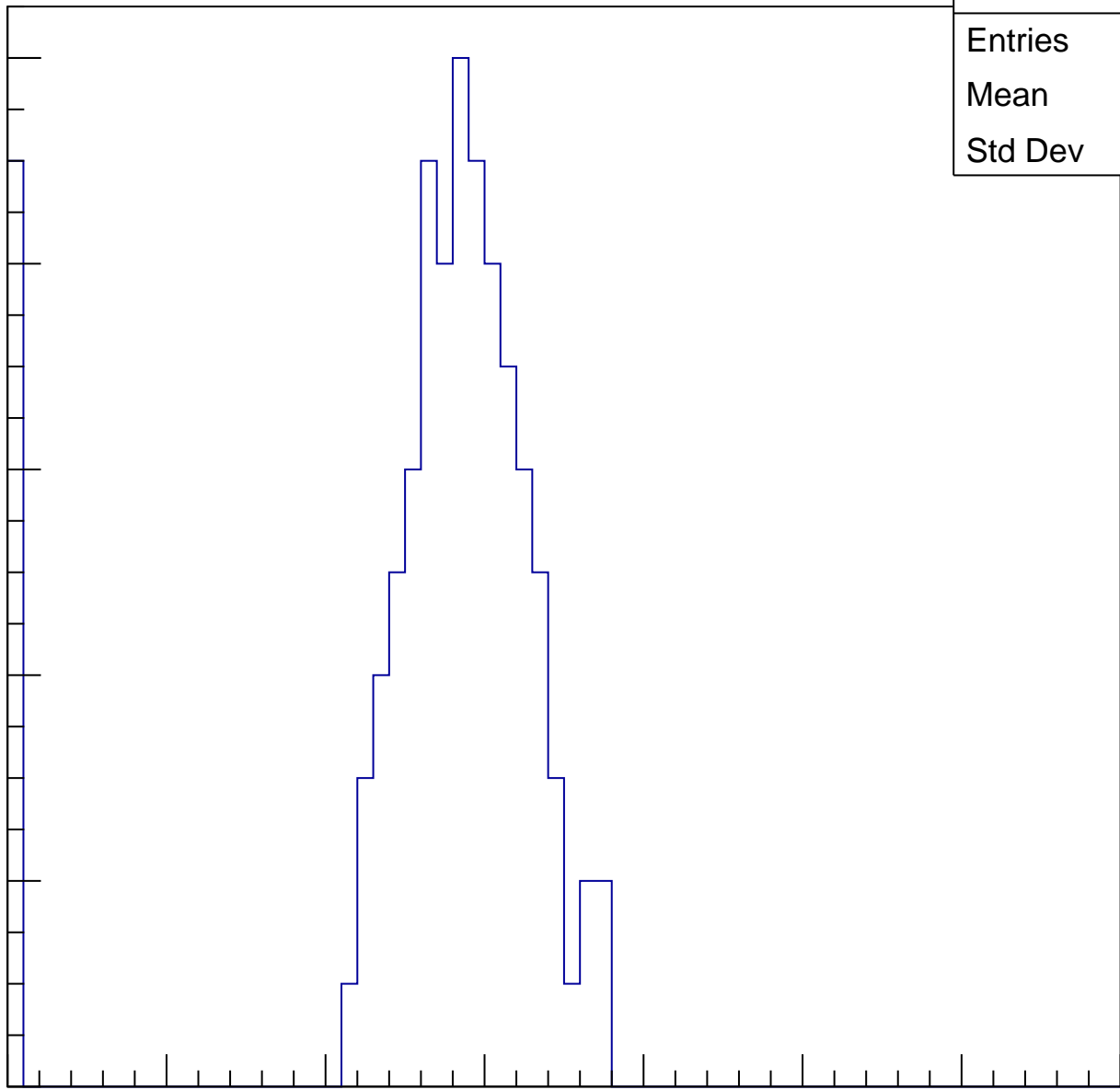
Entries	98
Mean	25.89
Std Dev	8.936

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

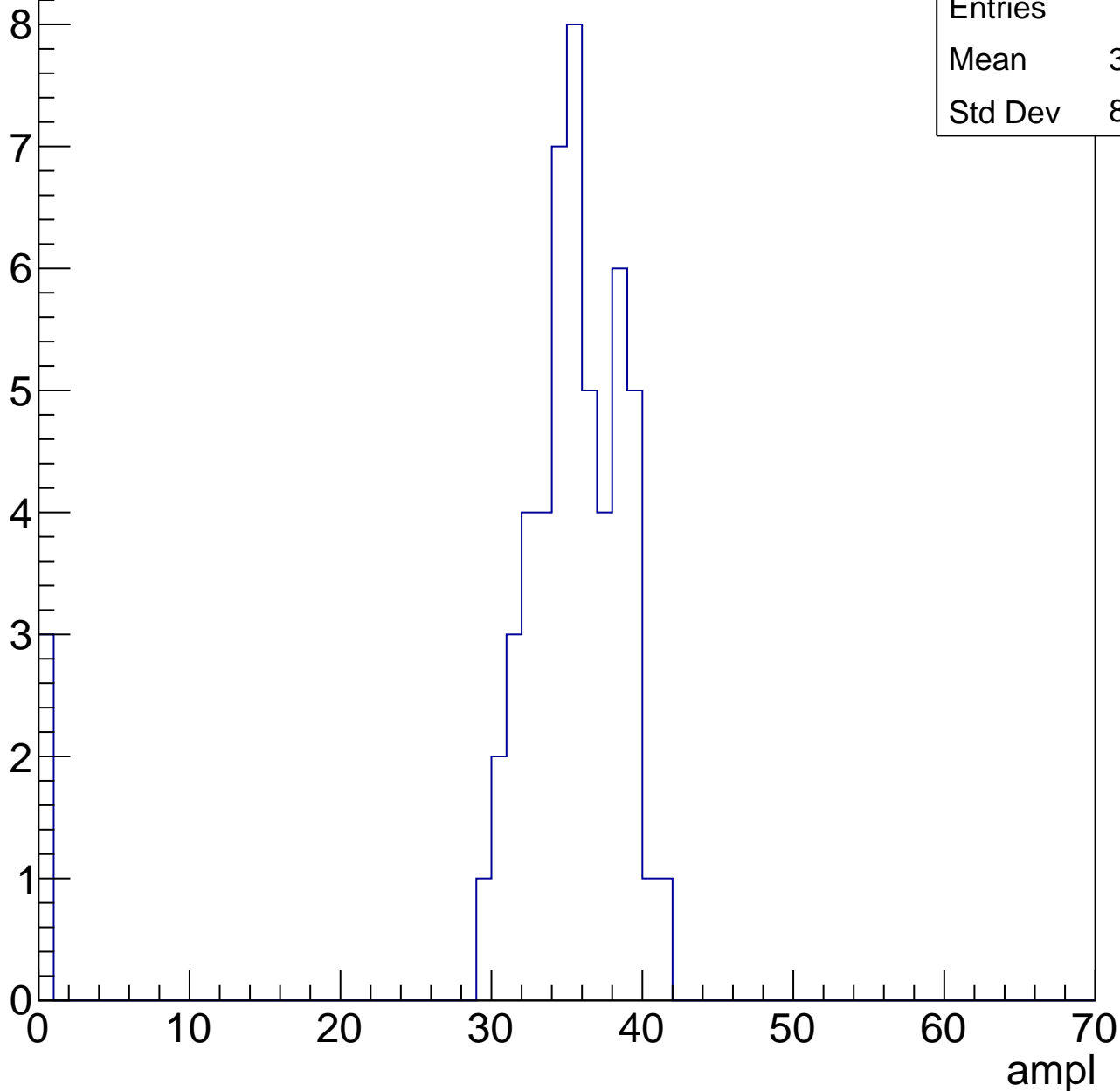


B1L103S, U5-ch14, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	33.19
Std Dev	8.505

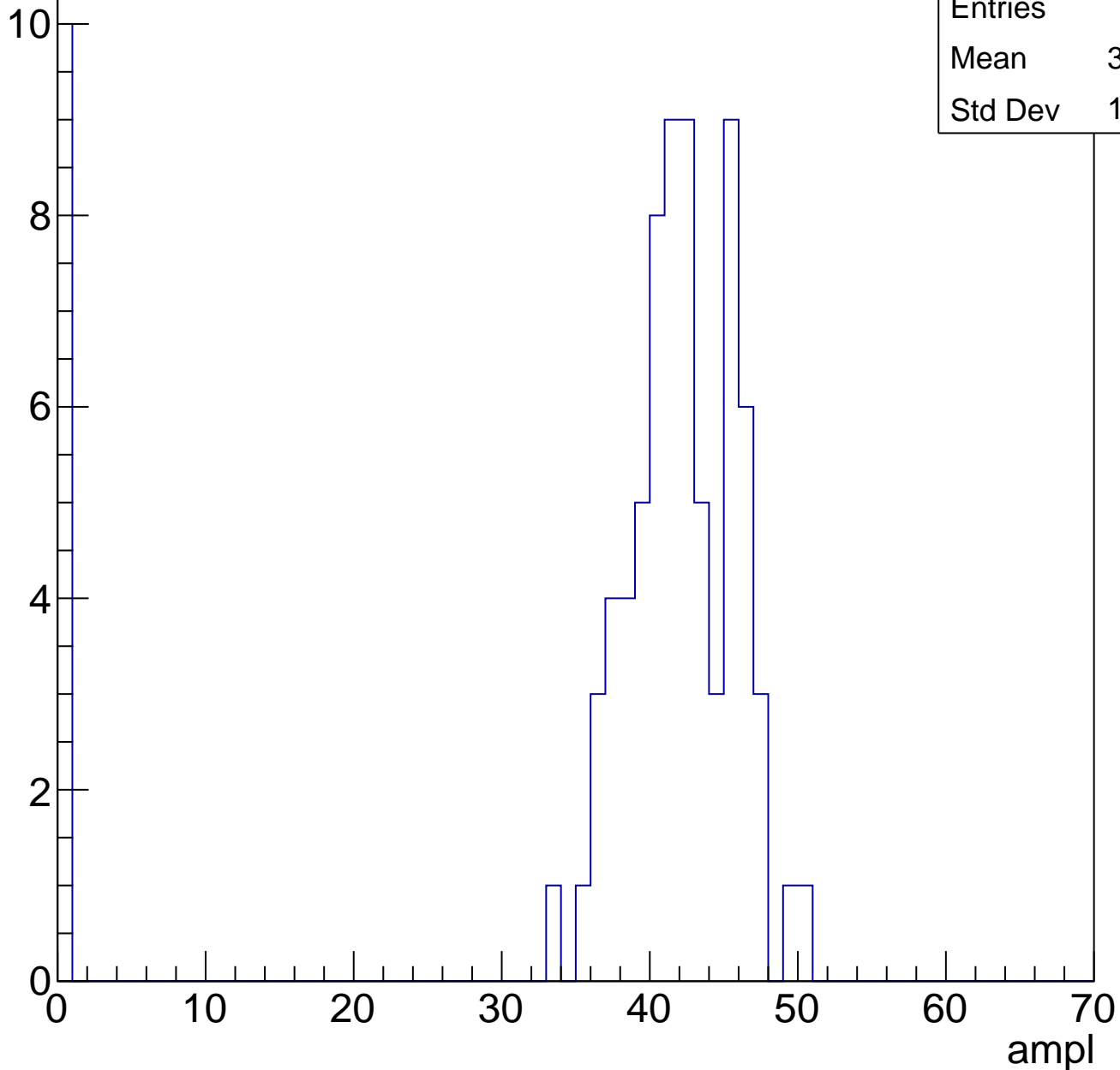


B1L103S, U5-ch14, adc2

calib_packv5_041523_1651.root, FC#0, port C2

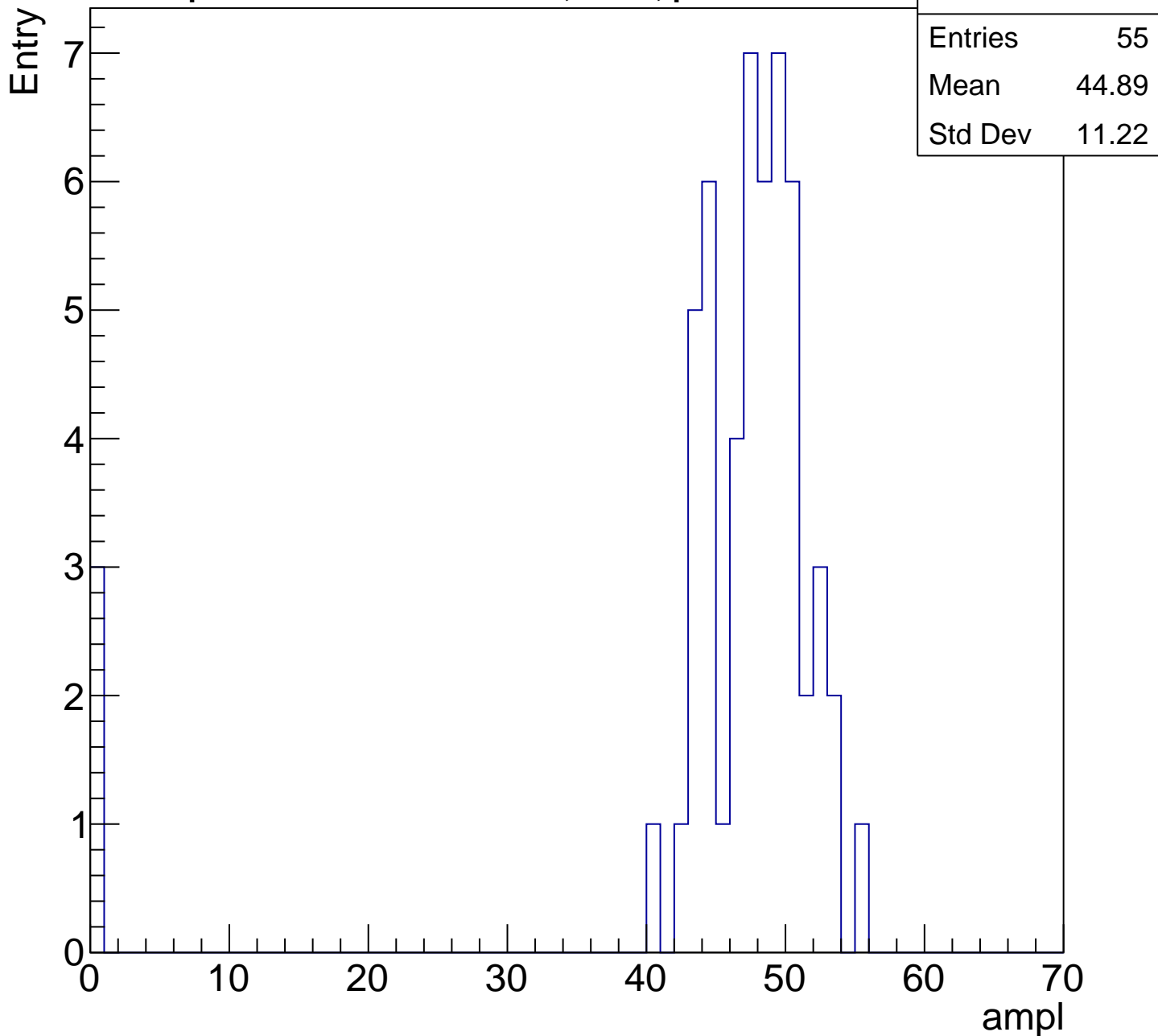
Entries	82
Mean	36.66
Std Dev	14.04

Entry



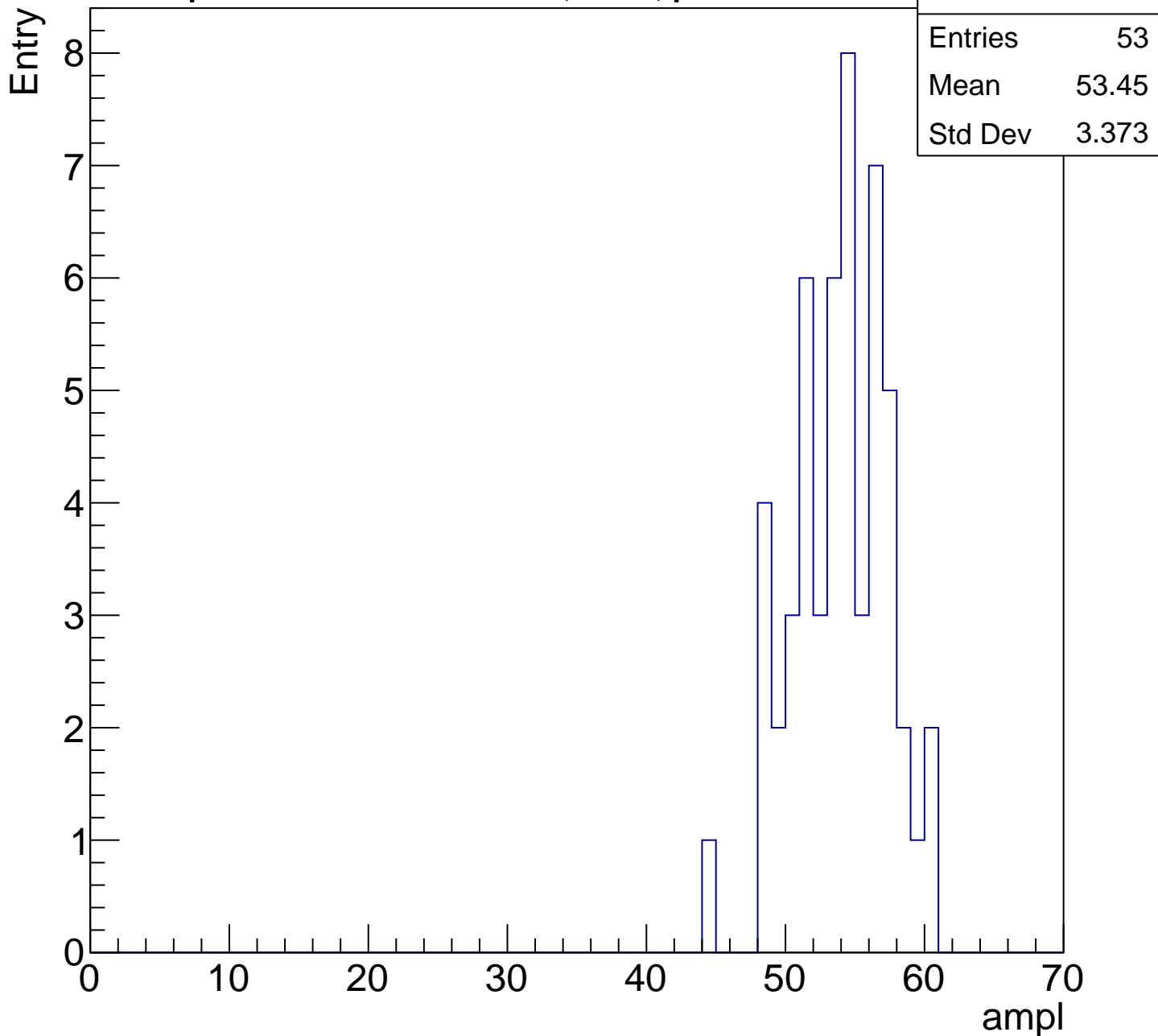
B1L103S, U5-ch14, adc3

calib_packv5_041523_1651.root, FC#0, port C2



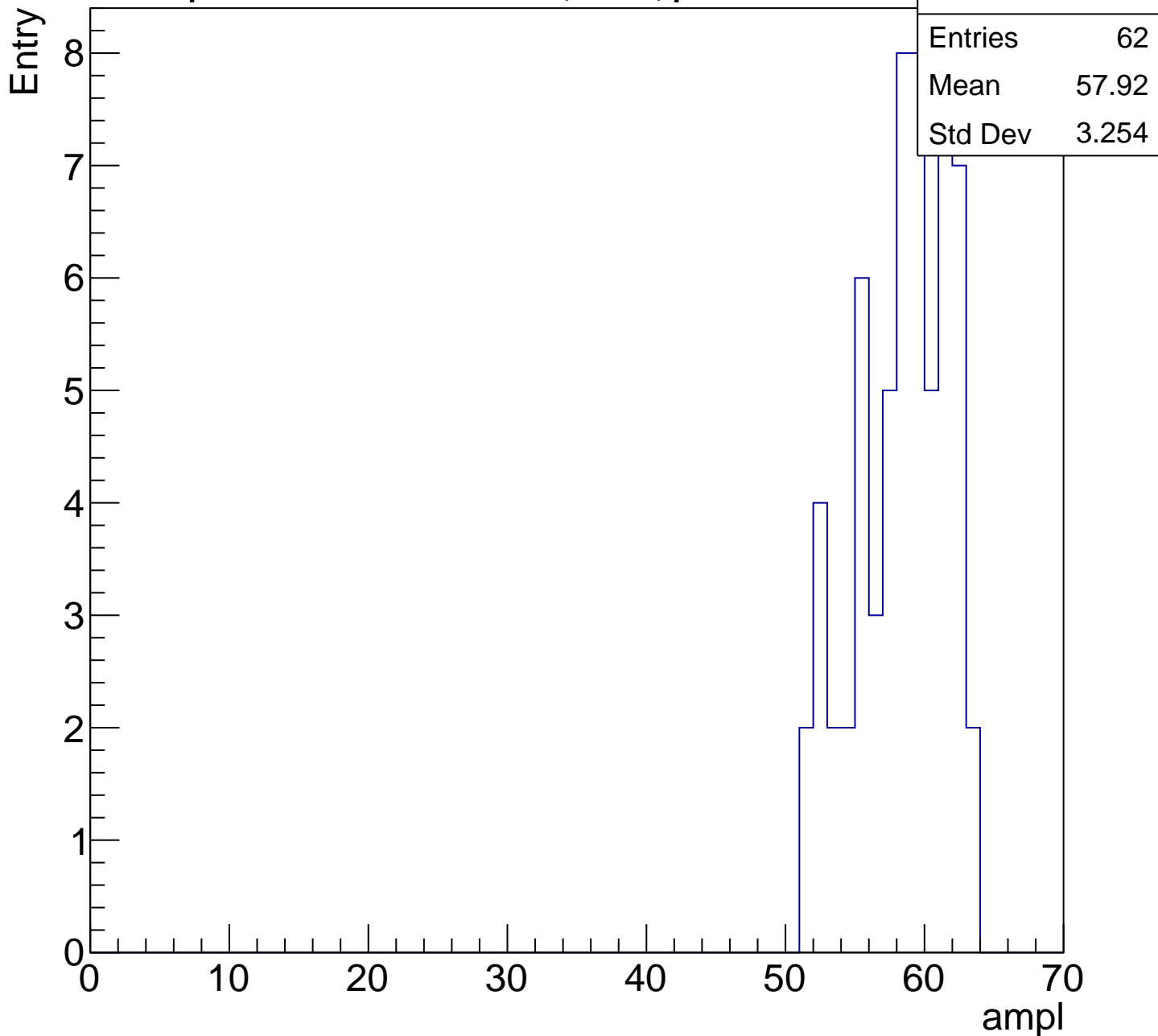
B1L103S, U5-ch14, adc4

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U5-ch14, adc5

calib_packv5_041523_1651.root, FC#0, port C2

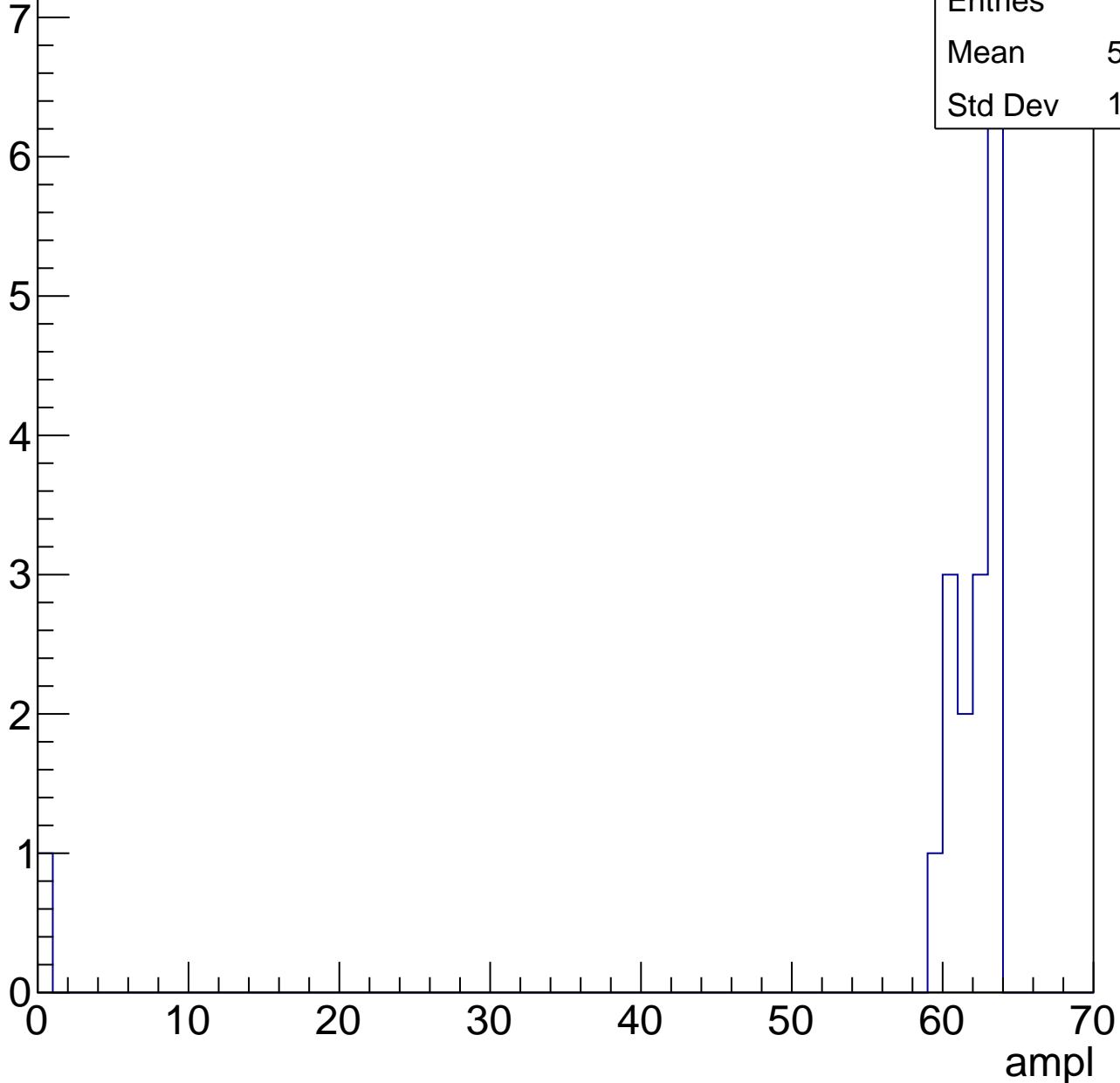


B1L103S, U5-ch14, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	17
Mean	58.12
Std Dev	14.59

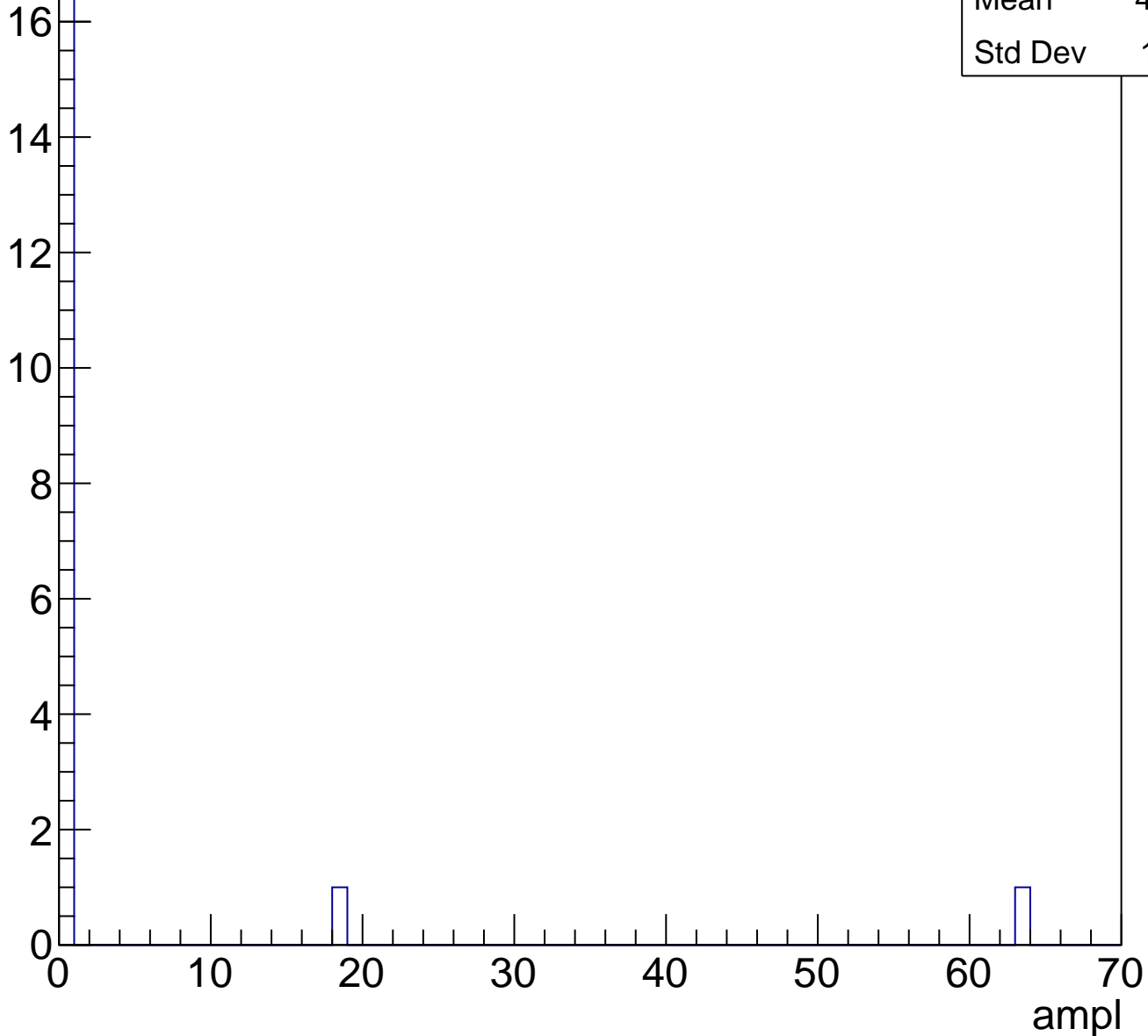


B1L103S, U5-ch14, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	4.263
Std Dev	14.41

Entry

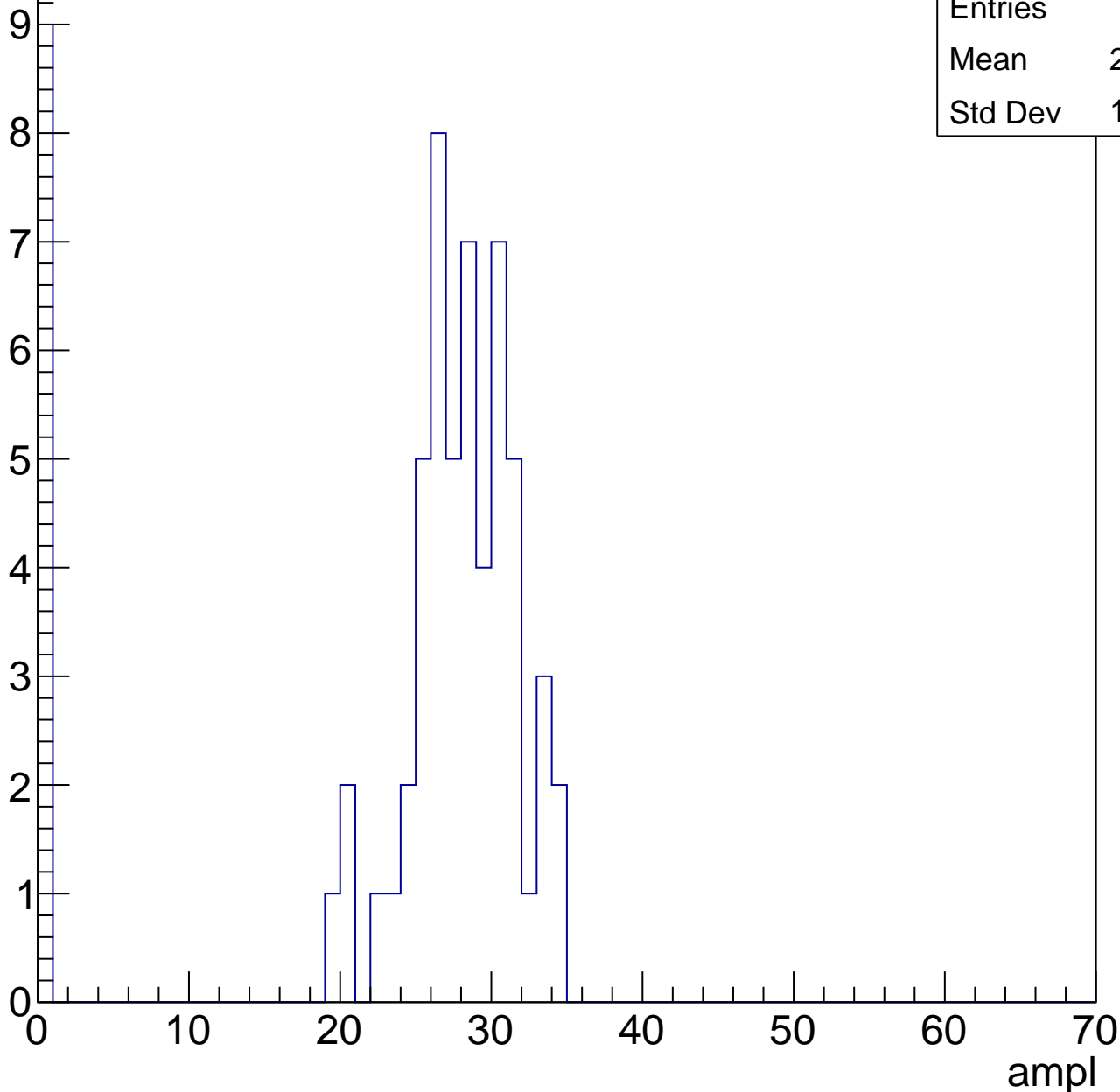


B1L103S, U5-ch15, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

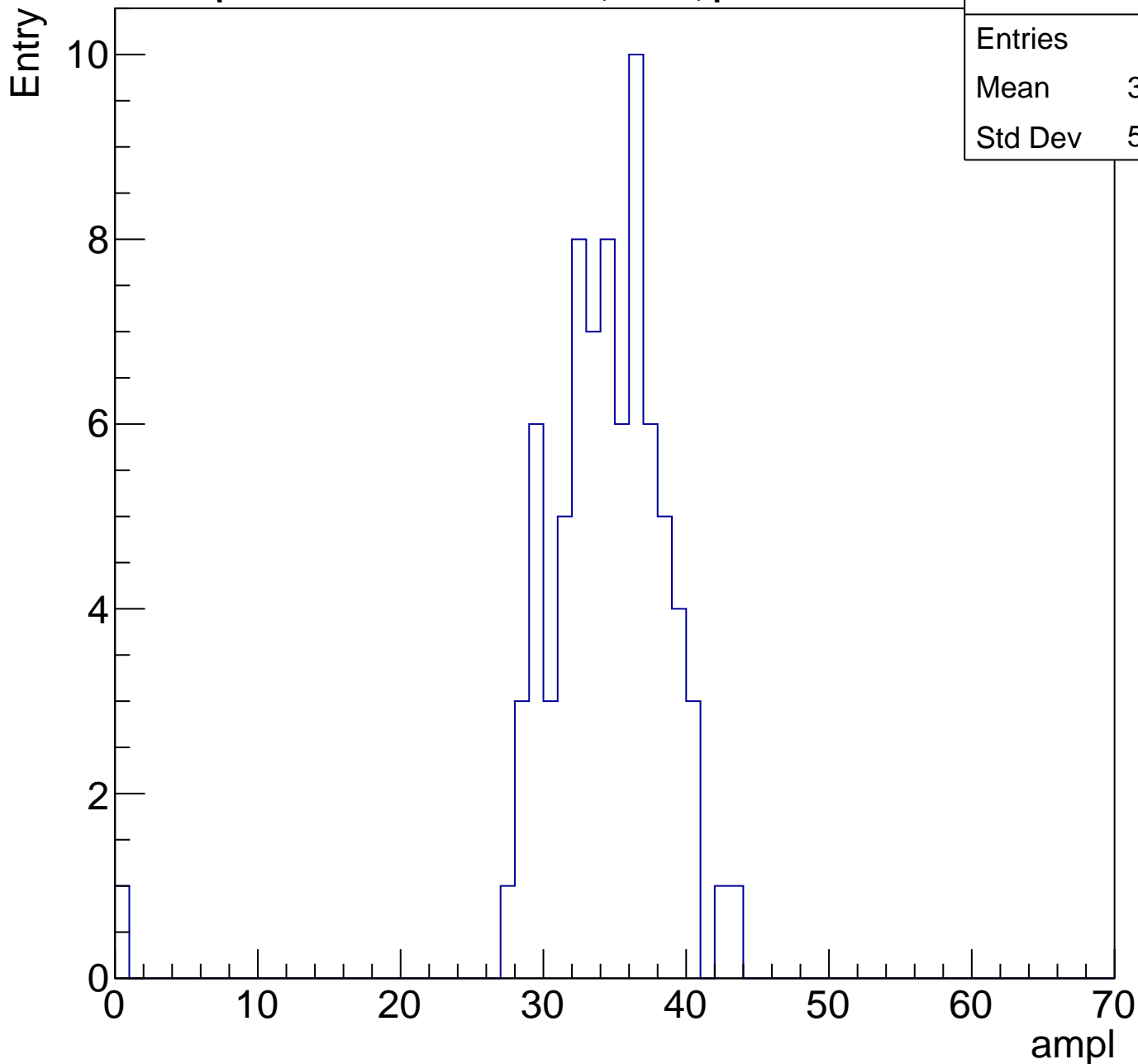
Entries	63
Mean	23.75
Std Dev	10.19



B1L103S, U5-ch15, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	78
Mean	33.74
Std Dev	5.217

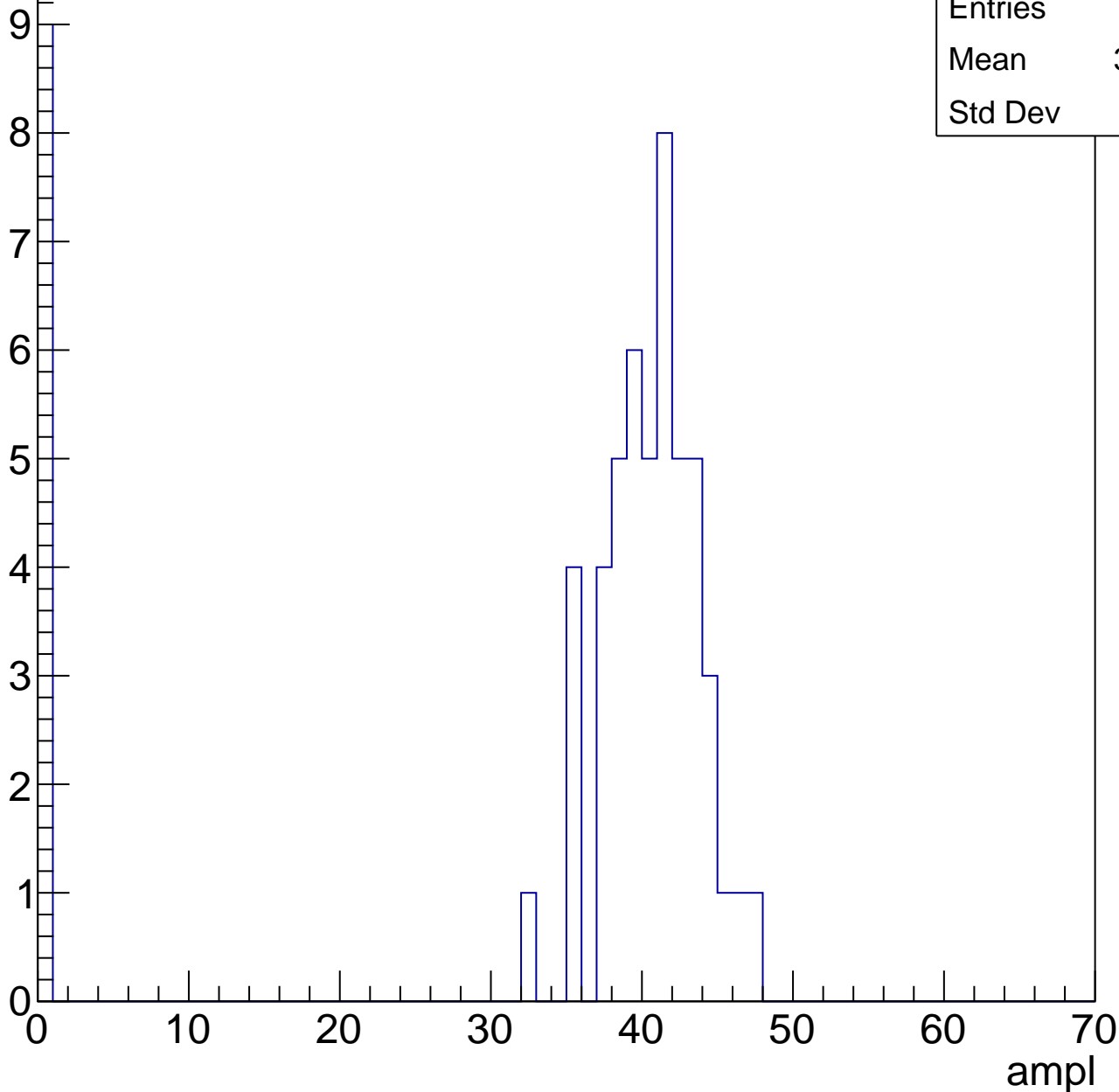


B1L103S, U5-ch15, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	33.91
Std Dev	14.8

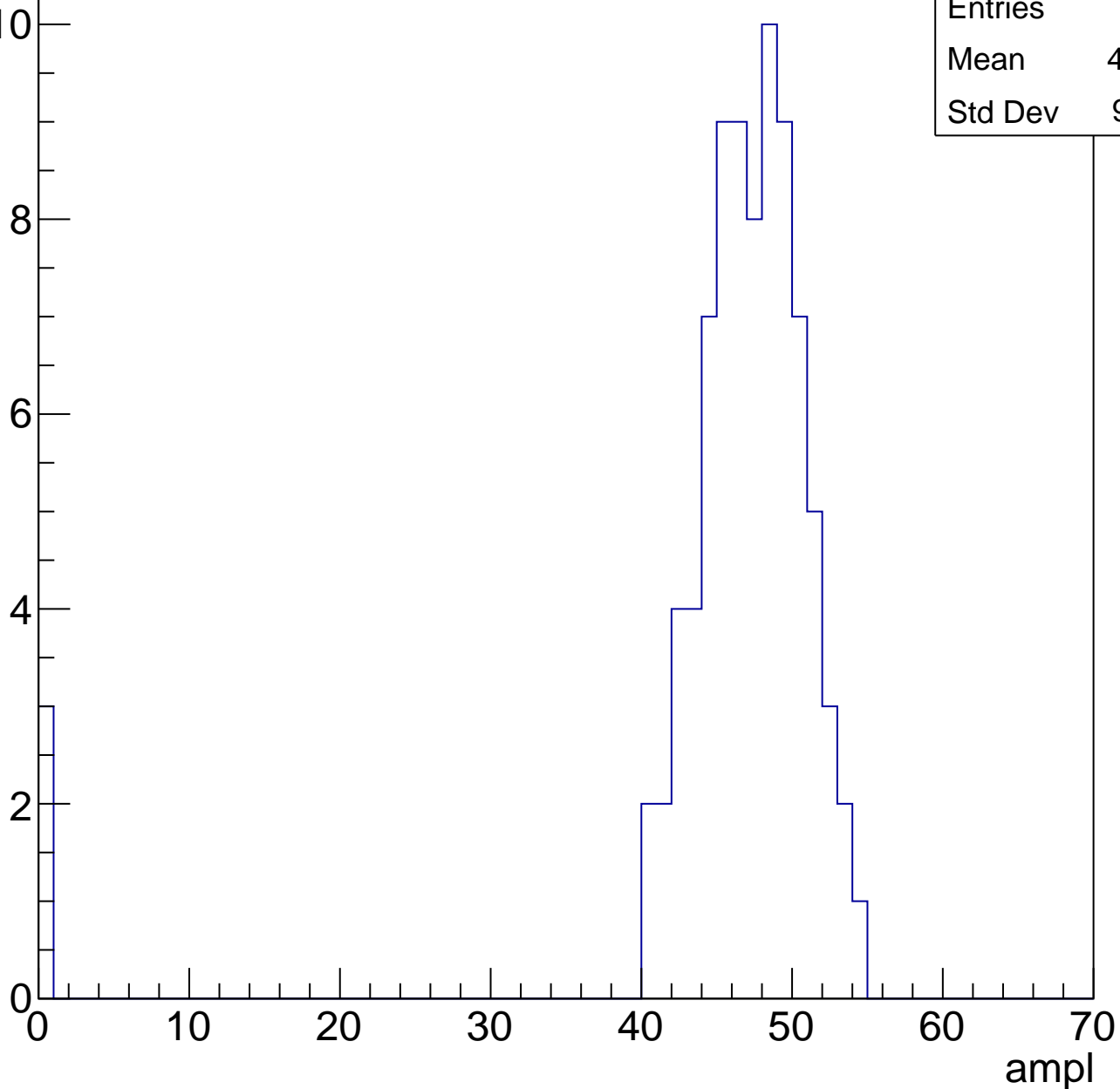


B1L103S, U5-ch15, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	85
Mean	45.26
Std Dev	9.201

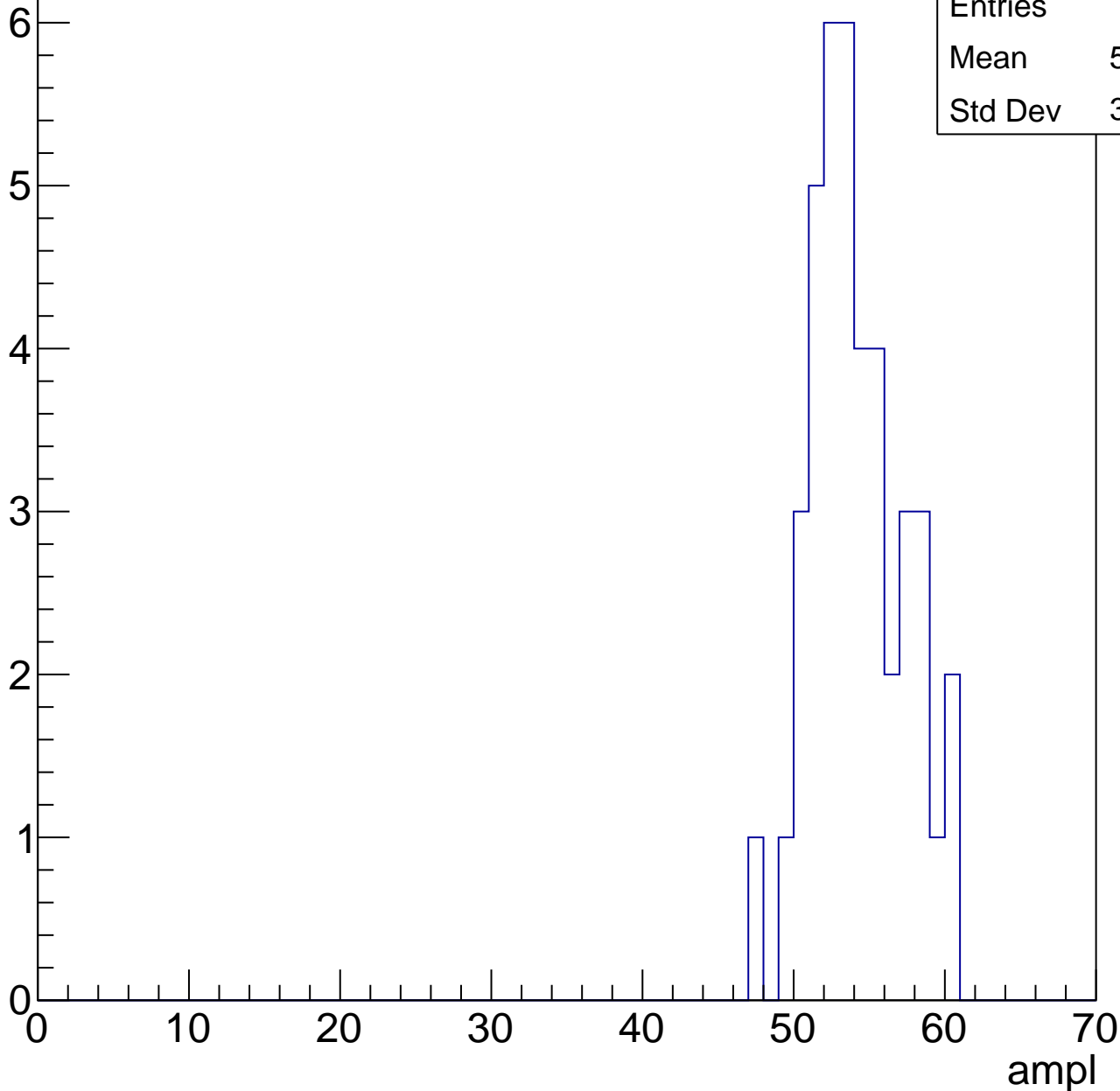


B1L103S, U5-ch15, adc4

calib_packv5_041523_1651.root, FC#0, port C2

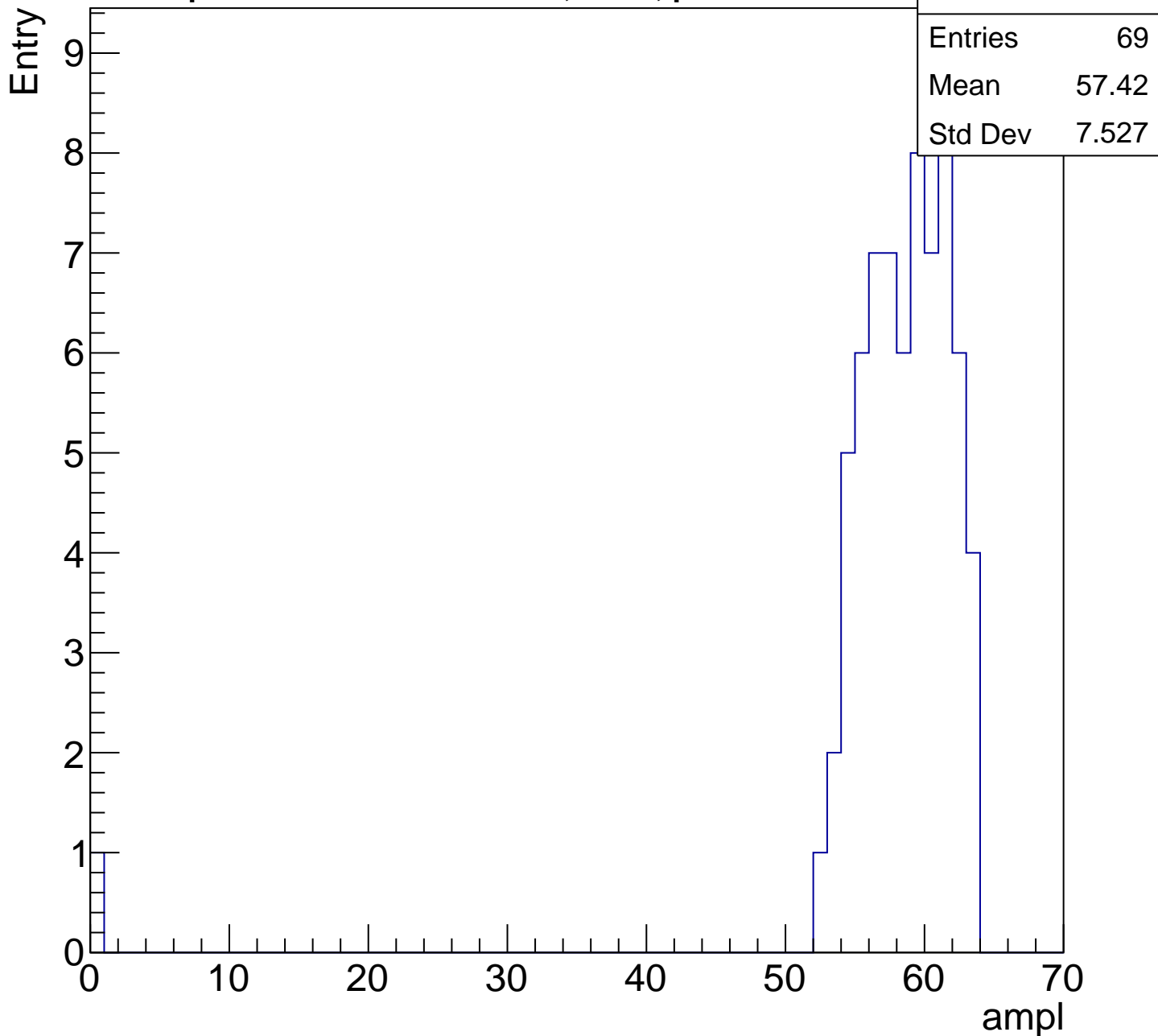
Entry

Entries	41
Mean	53.73
Std Dev	3.037



B1L103S, U5-ch15, adc5

calib_packv5_041523_1651.root, FC#0, port C2

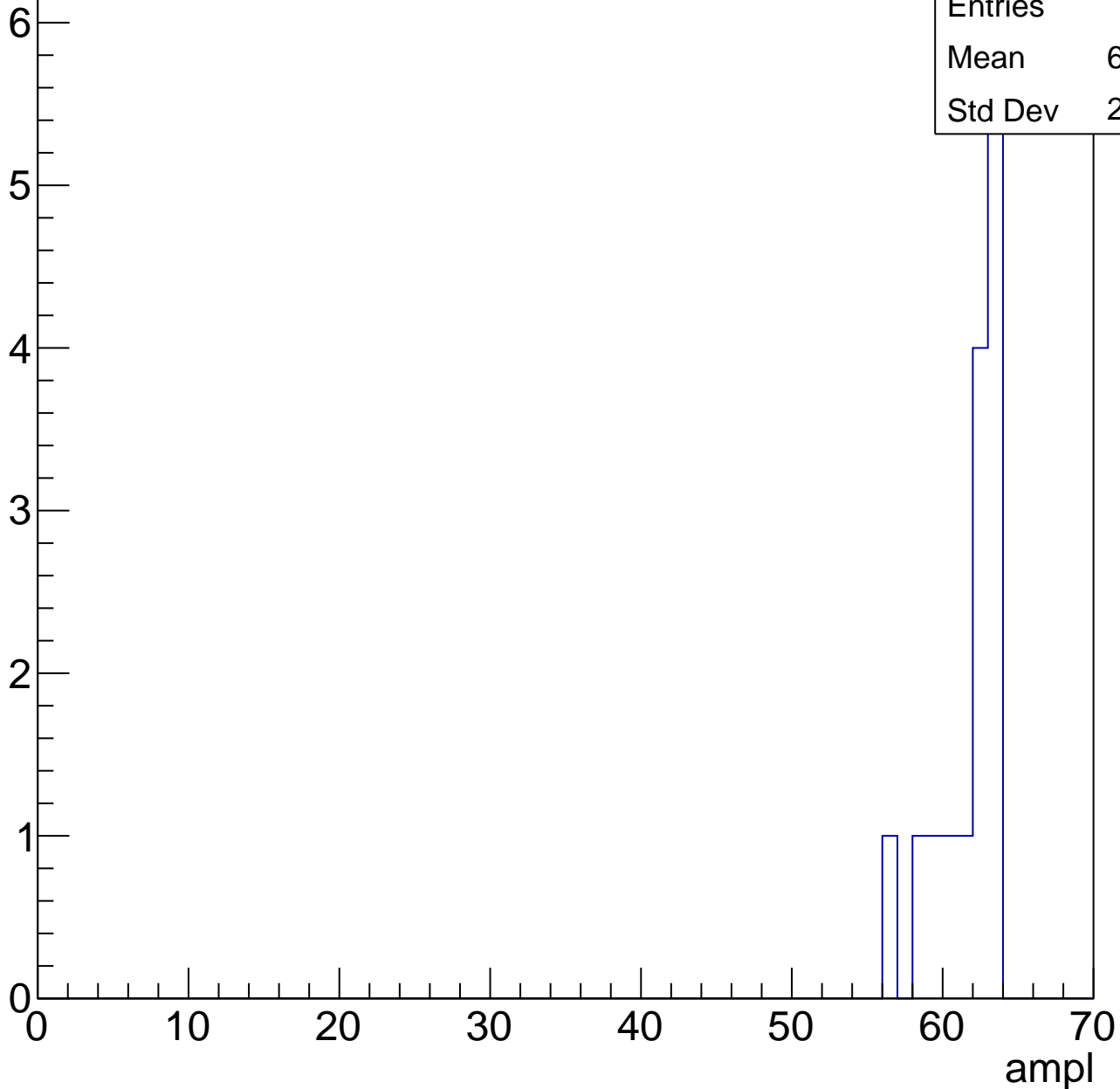


B1L103S, U5-ch15, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	15
Mean	61.33
Std Dev	2.087



B1L103S, U5-ch15, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	18
Mean	0
Std Dev	0

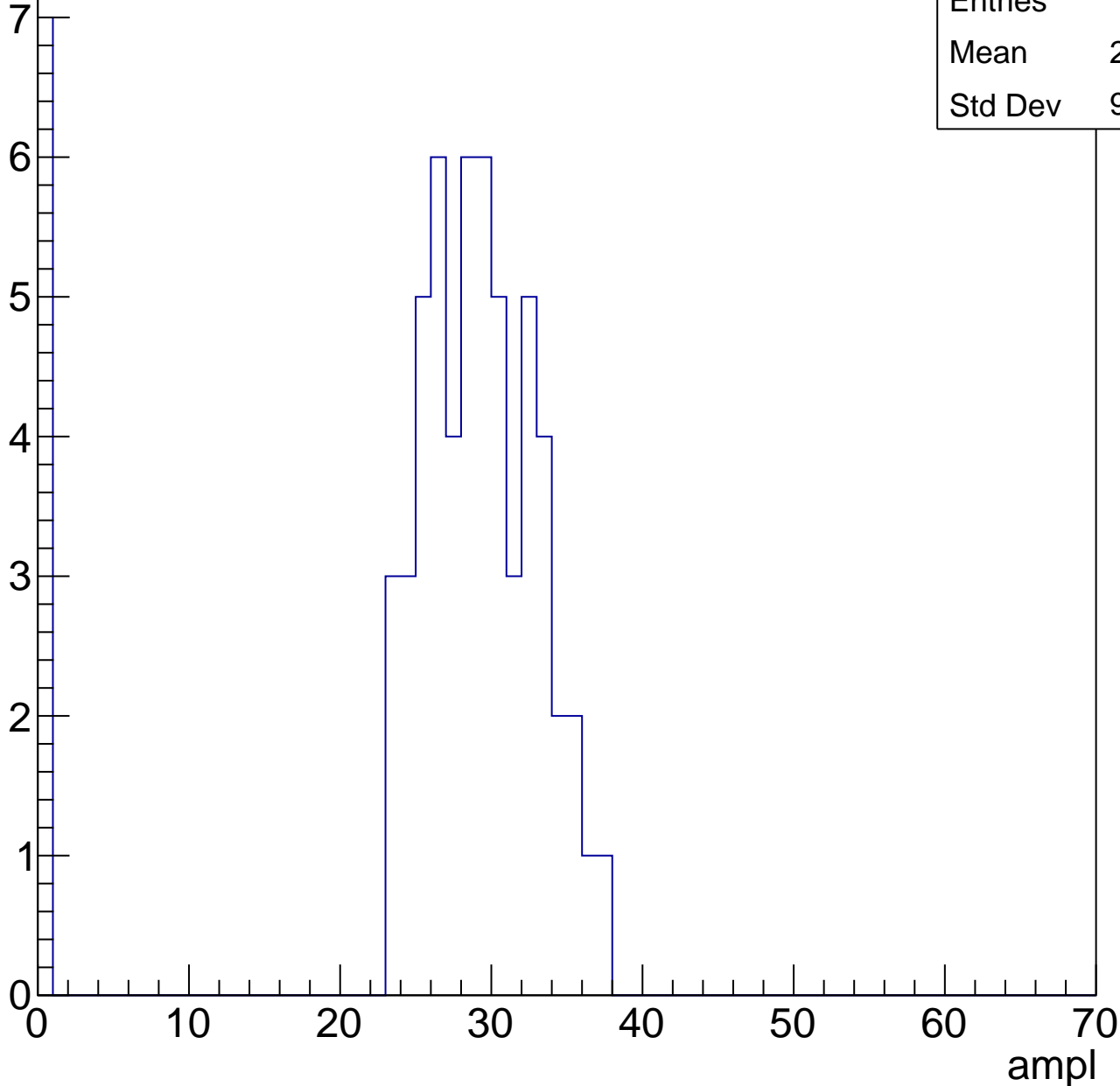
ampl

B1L103S, U5-ch16, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	25.68
Std Dev	9.672

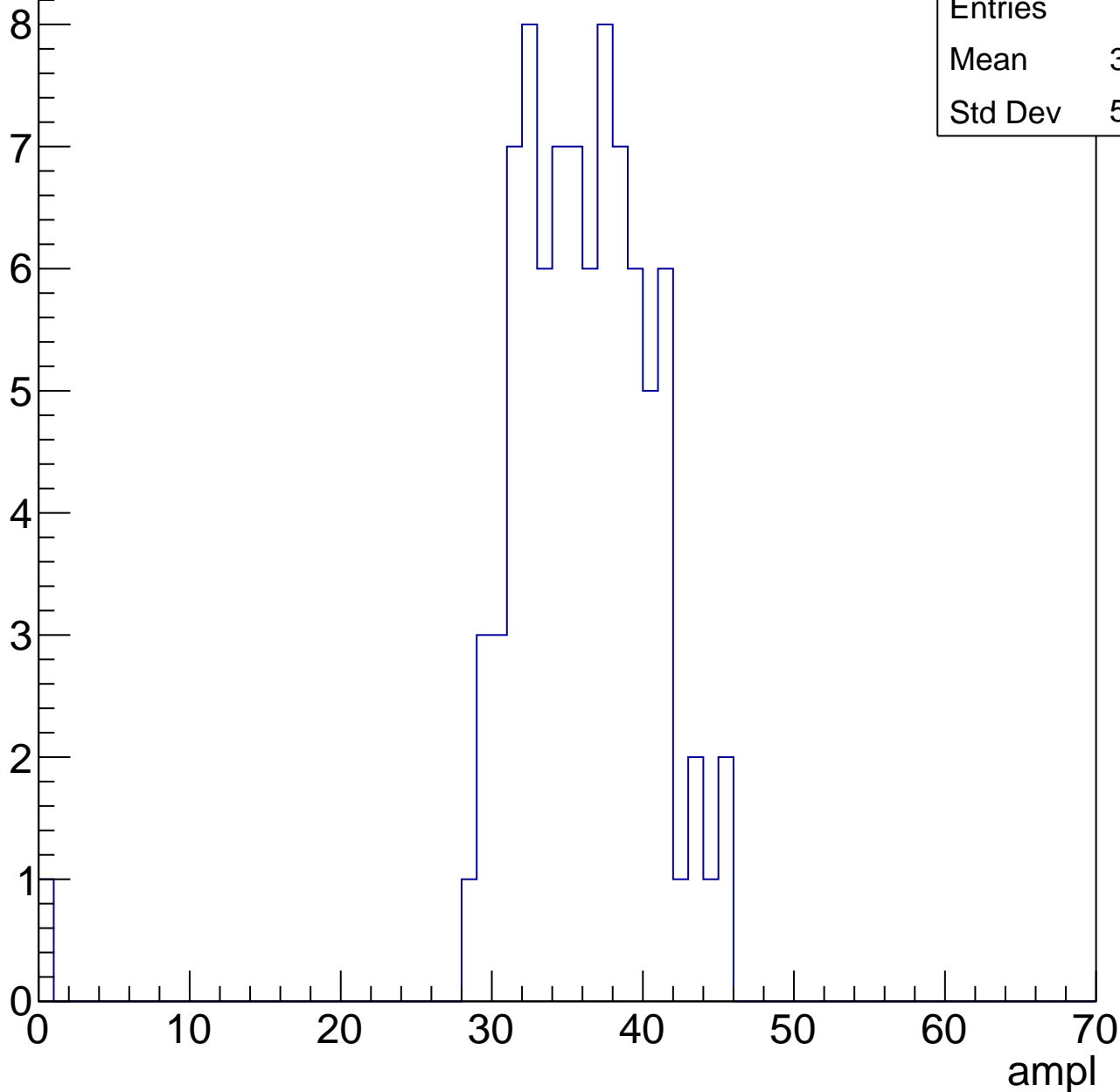


B1L103S, U5-ch16, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	87
Mean	35.39
Std Dev	5.524

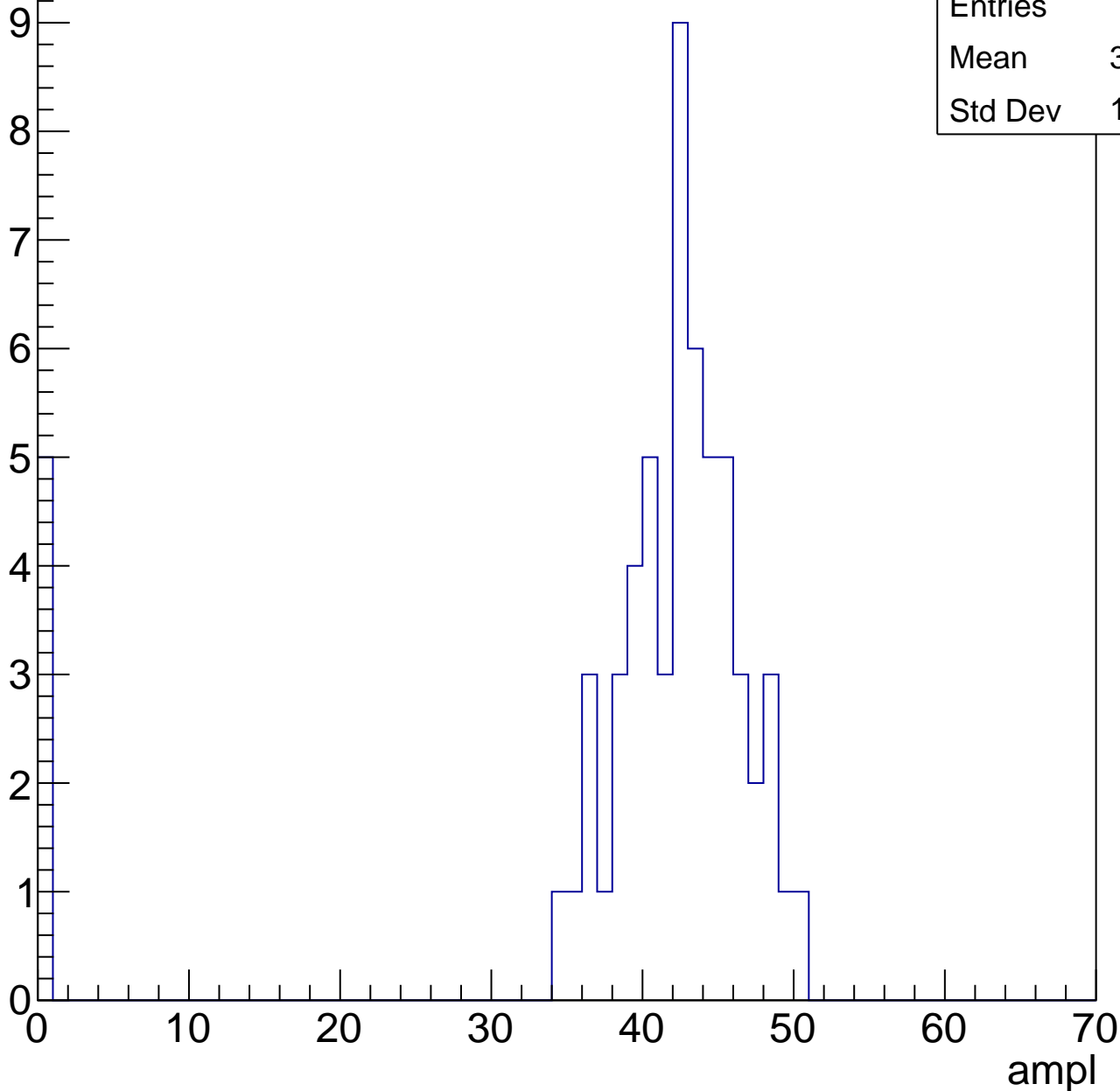


B1L103S, U5-ch16, adc2

calib_packv5_041523_1651.root, FC#0, port C2

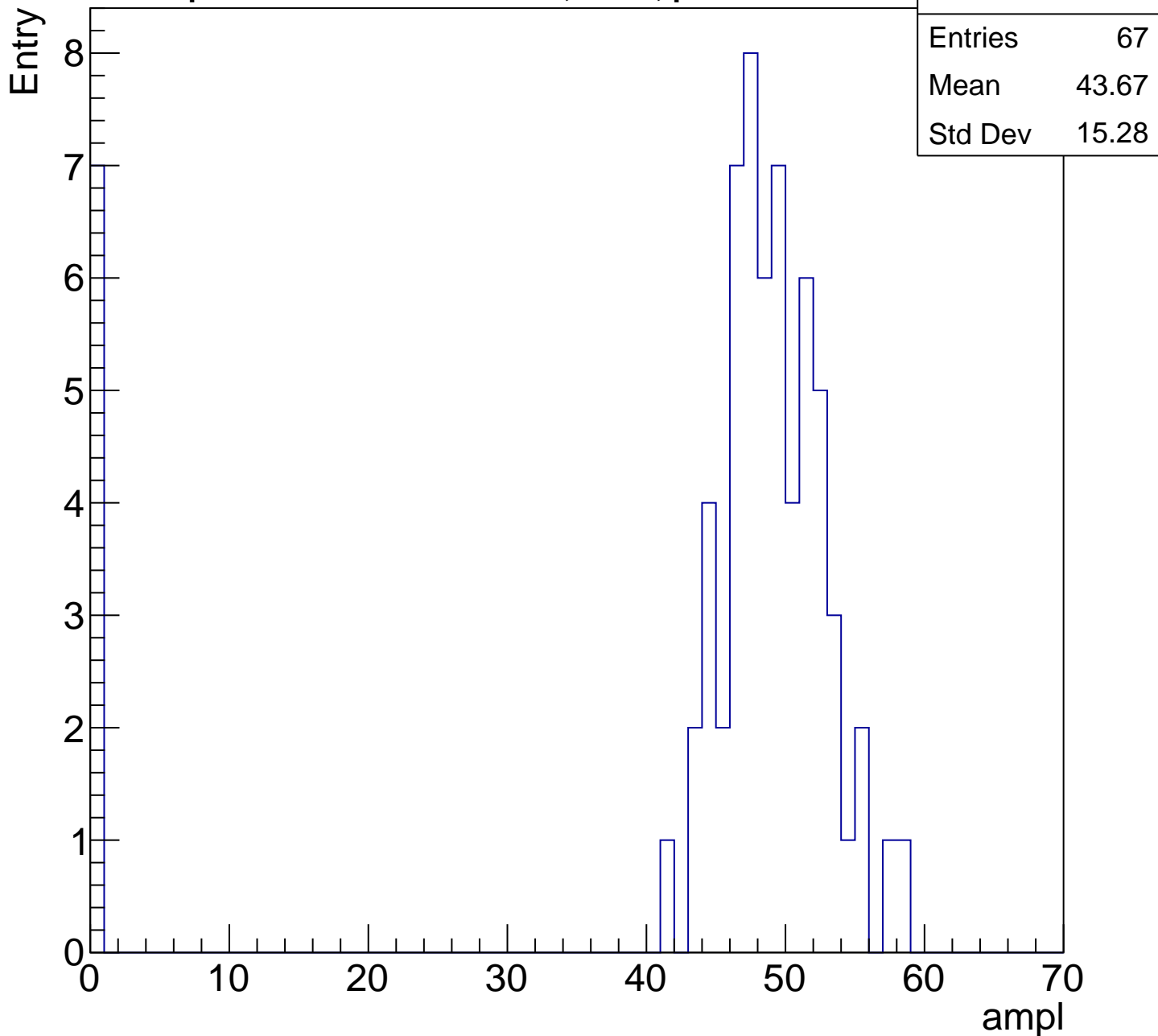
Entry

Entries	61
Mean	38.74
Std Dev	12.09



B1L103S, U5-ch16, adc3

calib_packv5_041523_1651.root, FC#0, port C2

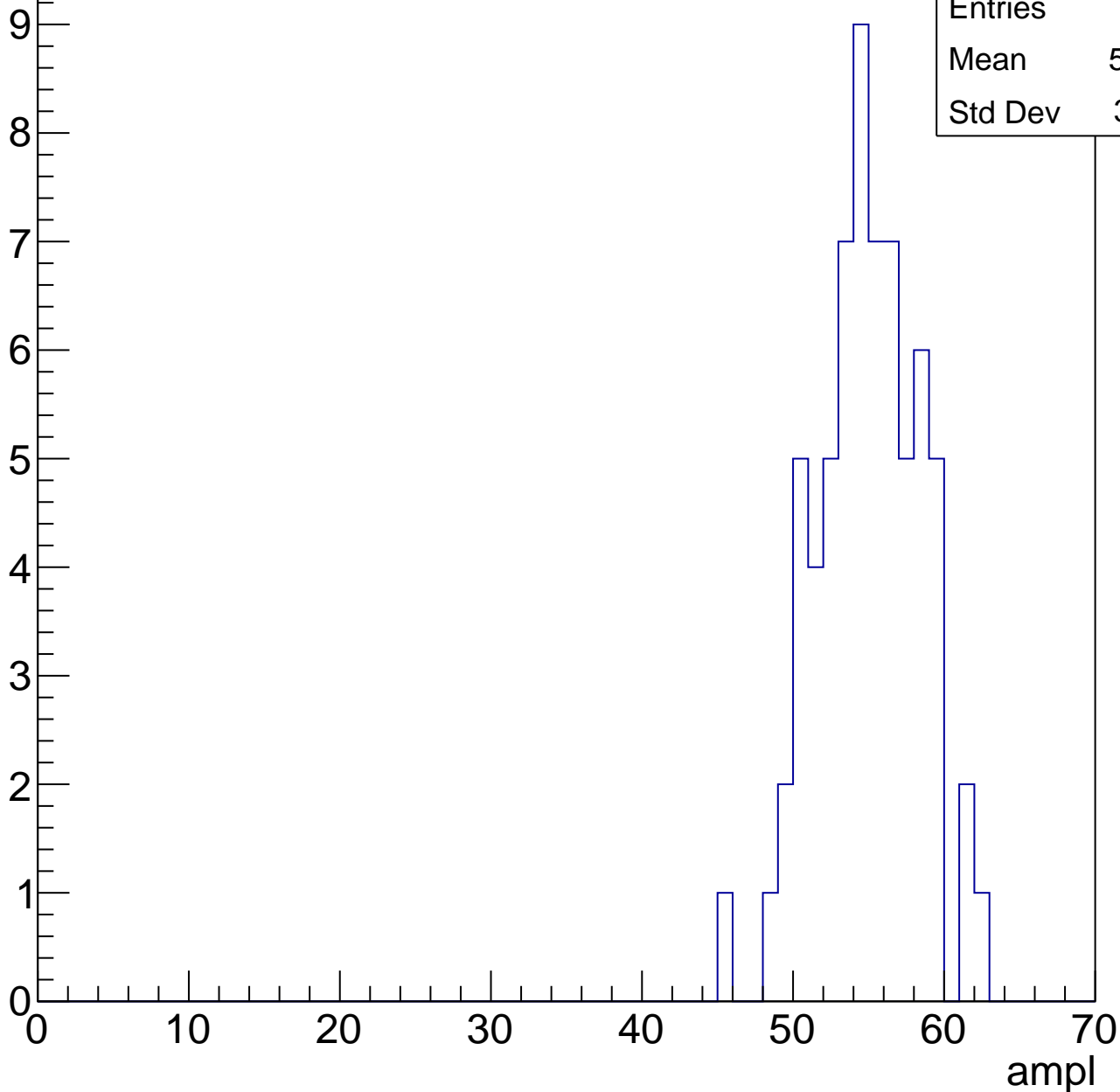


B1L103S, U5-ch16, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	54.49
Std Dev	3.361



B1L103S, U5-ch16, adc5

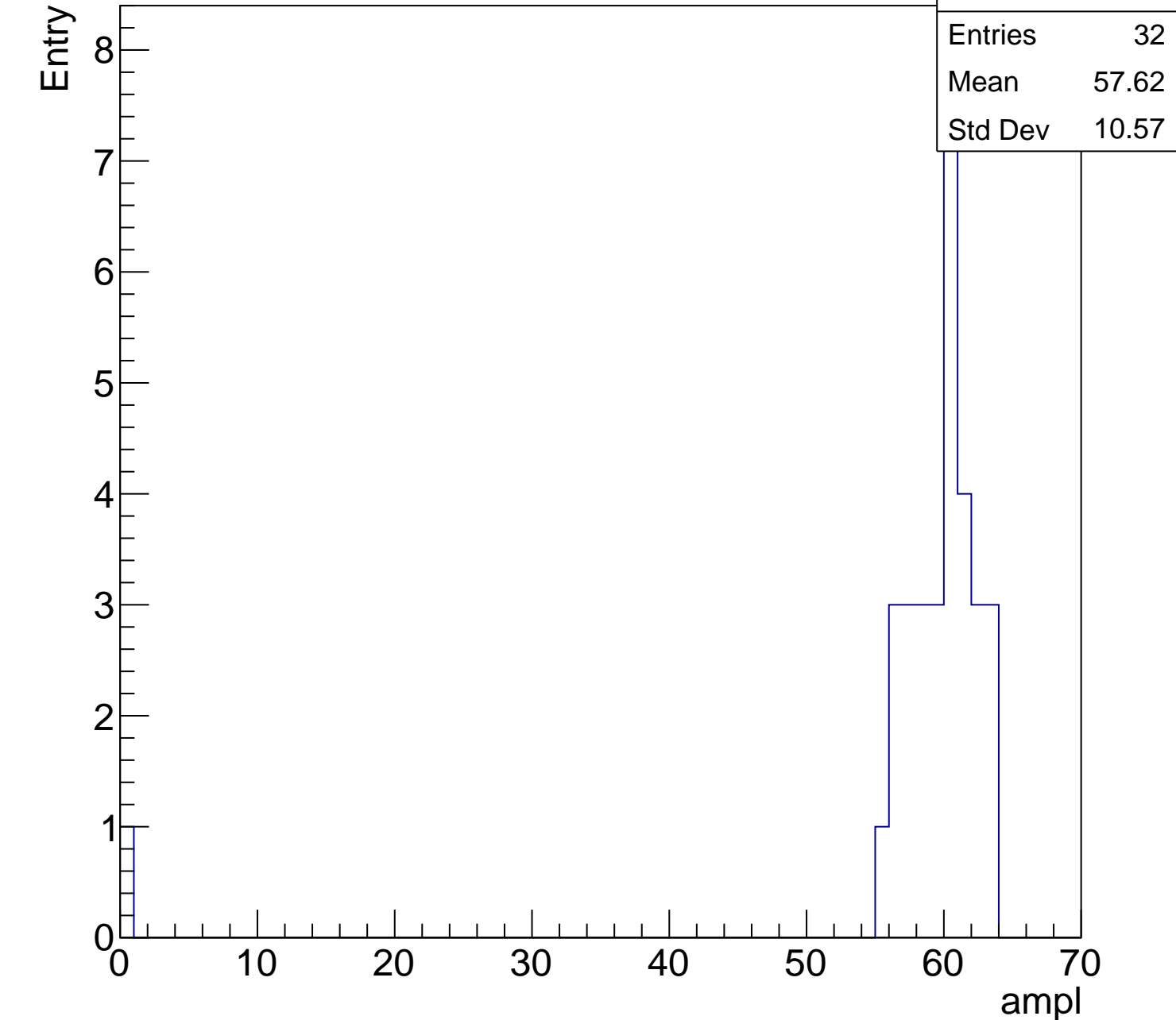
calib_packv5_041523_1651.root, FC#0, port C2

Entry

8
7
6
5
4
3
2
1
0

Entries	32
Mean	57.62
Std Dev	10.57

ampl

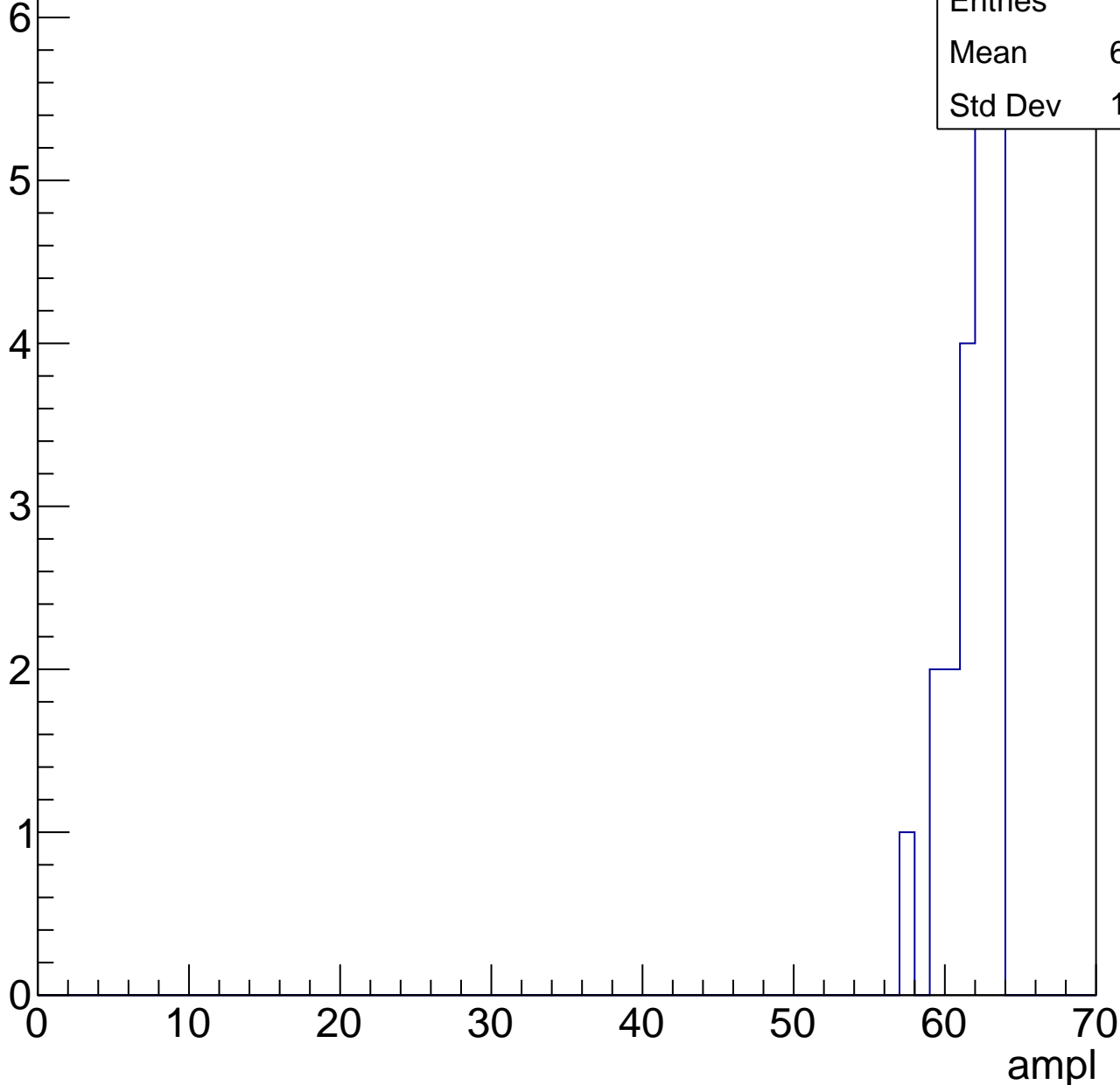


B1L103S, U5-ch16, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	21
Mean	61.38
Std Dev	1.588



B1L103S, U5-ch16, adc7

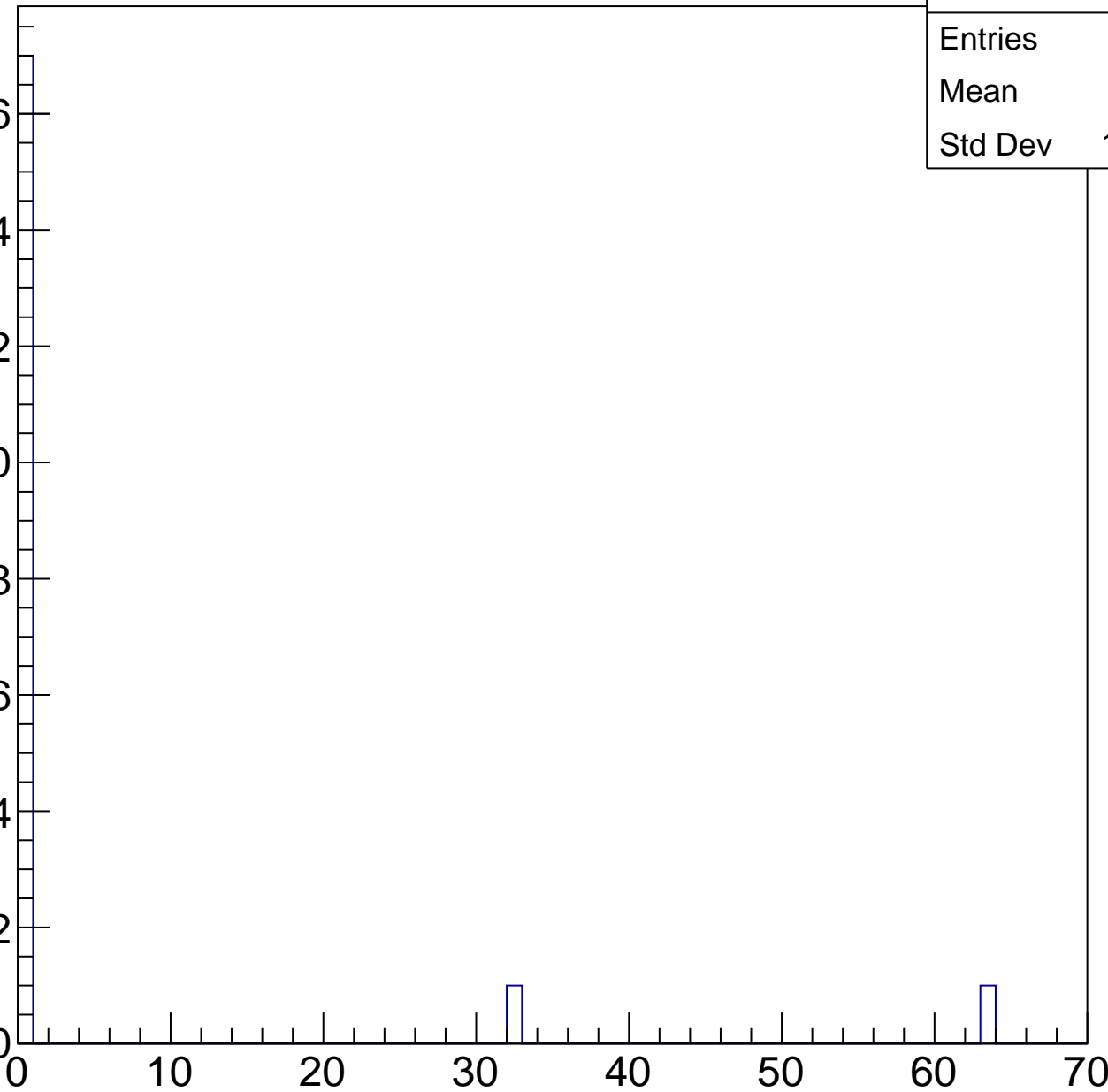
calib_packv5_041523_1651.root, FC#0, port C2

Entry

16
14
12
10
8
6
4
2
0

Entries	19
Mean	5
Std Dev	15.42

ampl

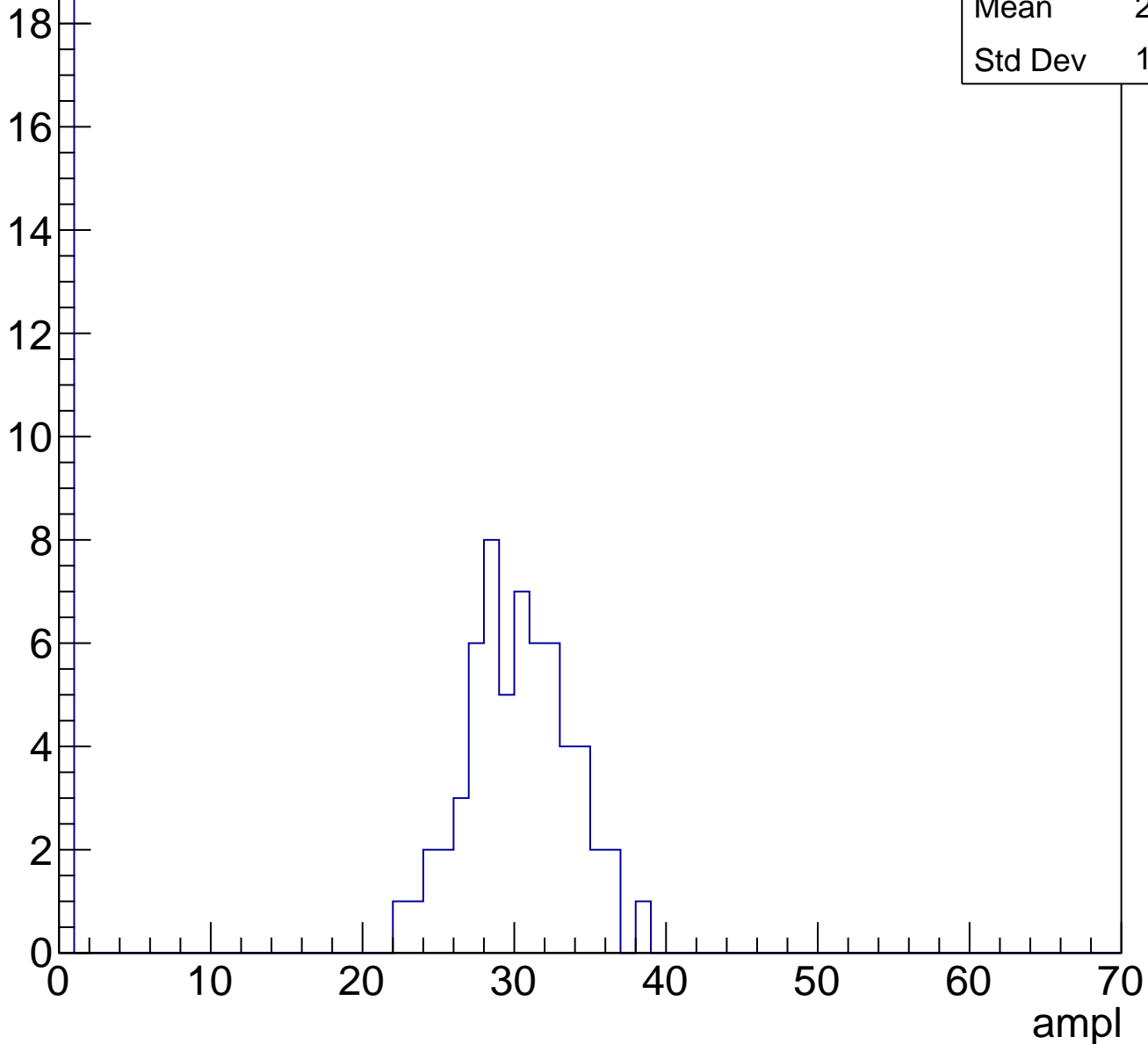


B1L103S, U5-ch17, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	79
Mean	22.63
Std Dev	13.07

Entry

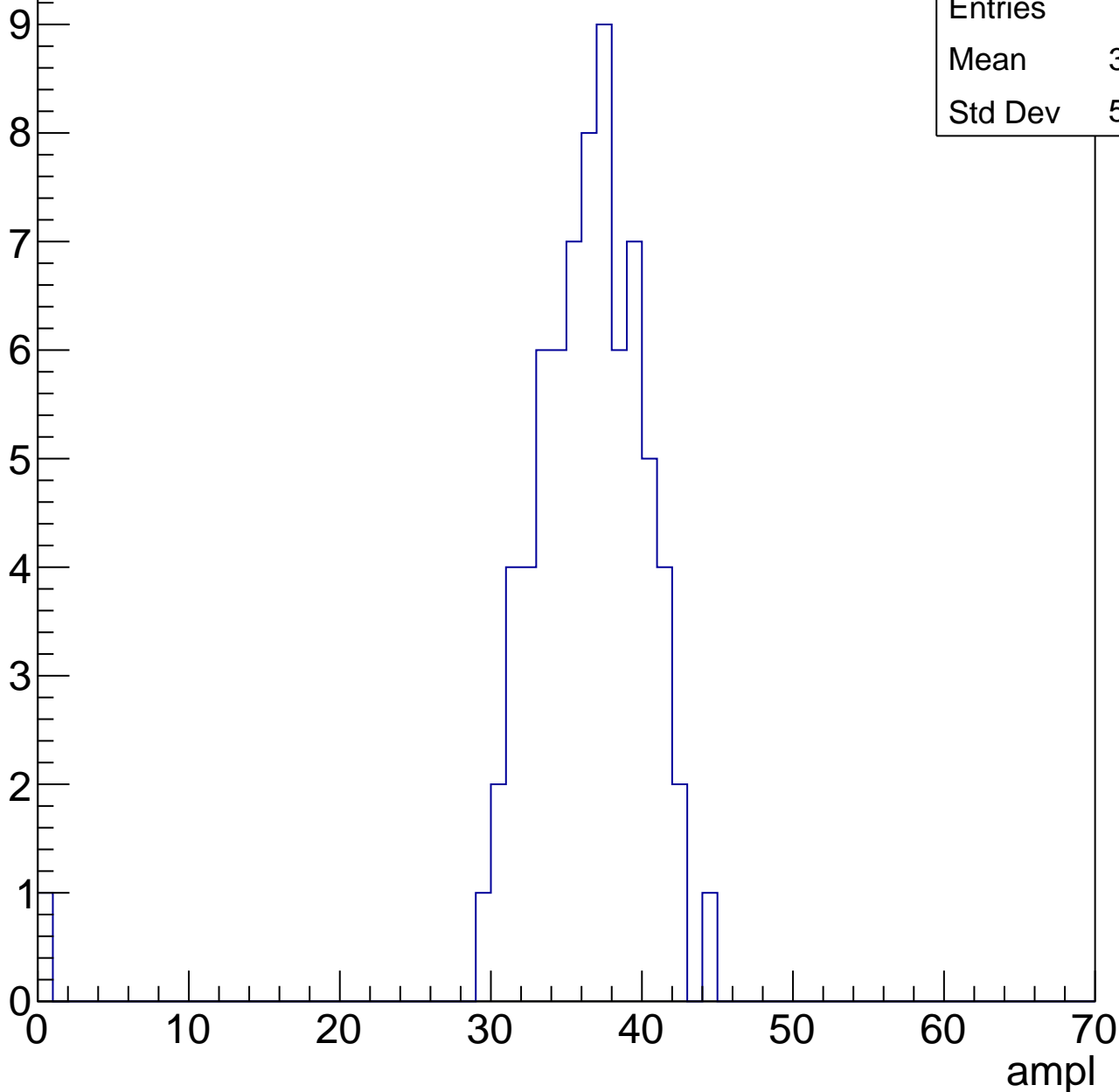


B1L103S, U5-ch17, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	35.64
Std Dev	5.323

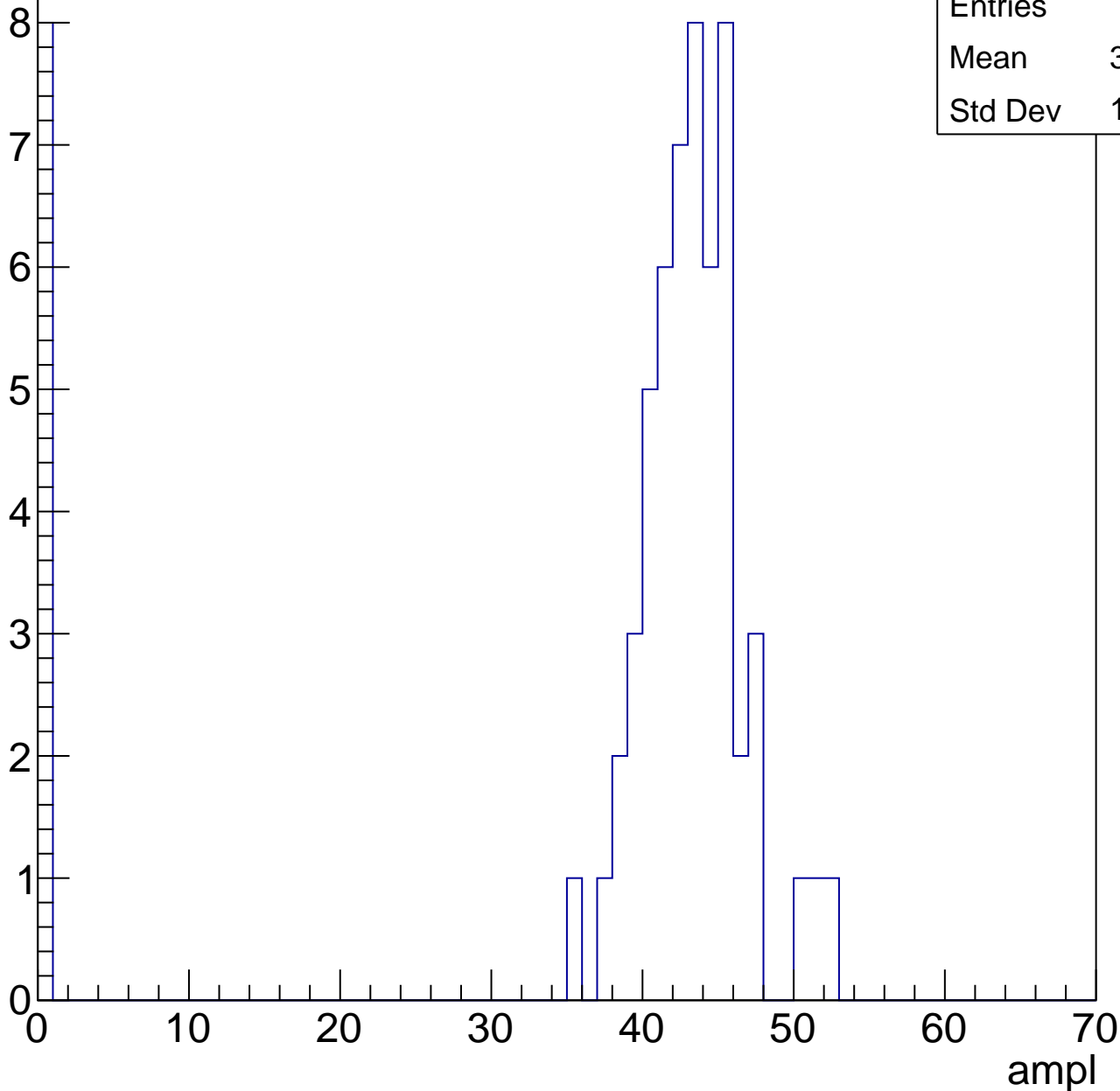


B1L103S, U5-ch17, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	37.44
Std Dev	14.59



B1L103S, U5-ch17, adc3

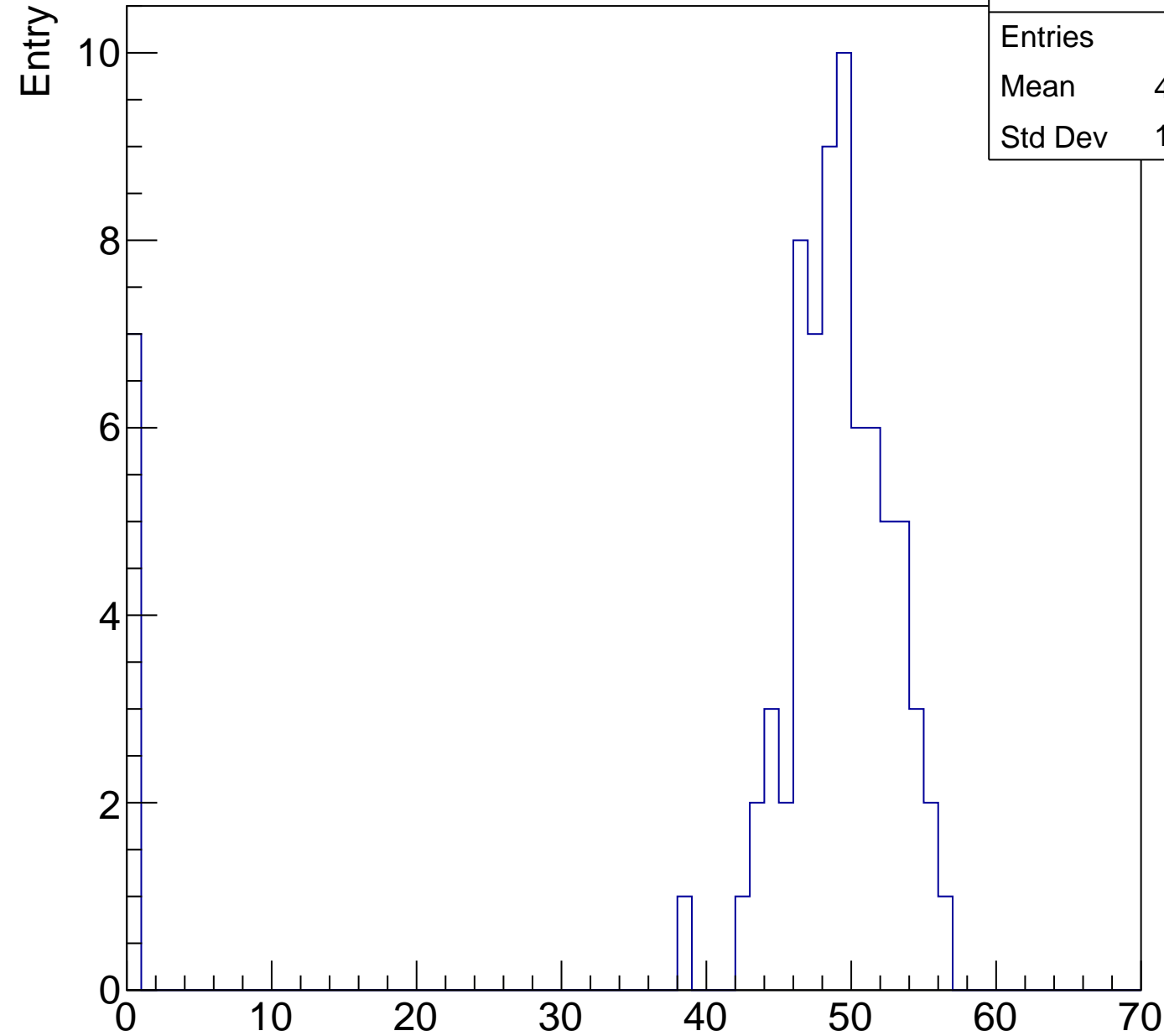
calib_packv5_041523_1651.root, FC#0, port C2

Entries	78
Mean	44.44
Std Dev	14.32

Entry

10
8
6
4
2
0

ampl

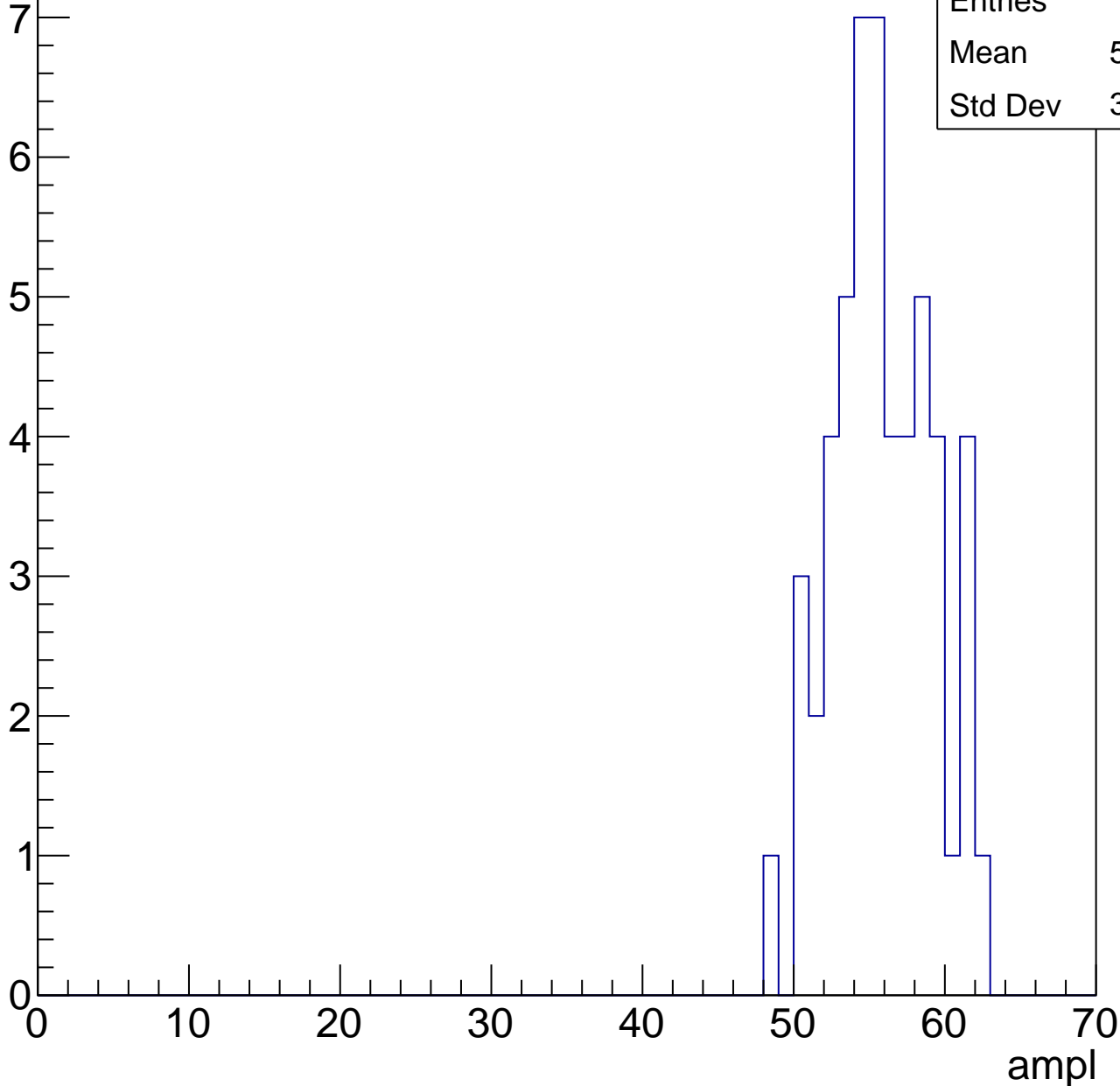


B1L103S, U5-ch17, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	55.38
Std Dev	3.277

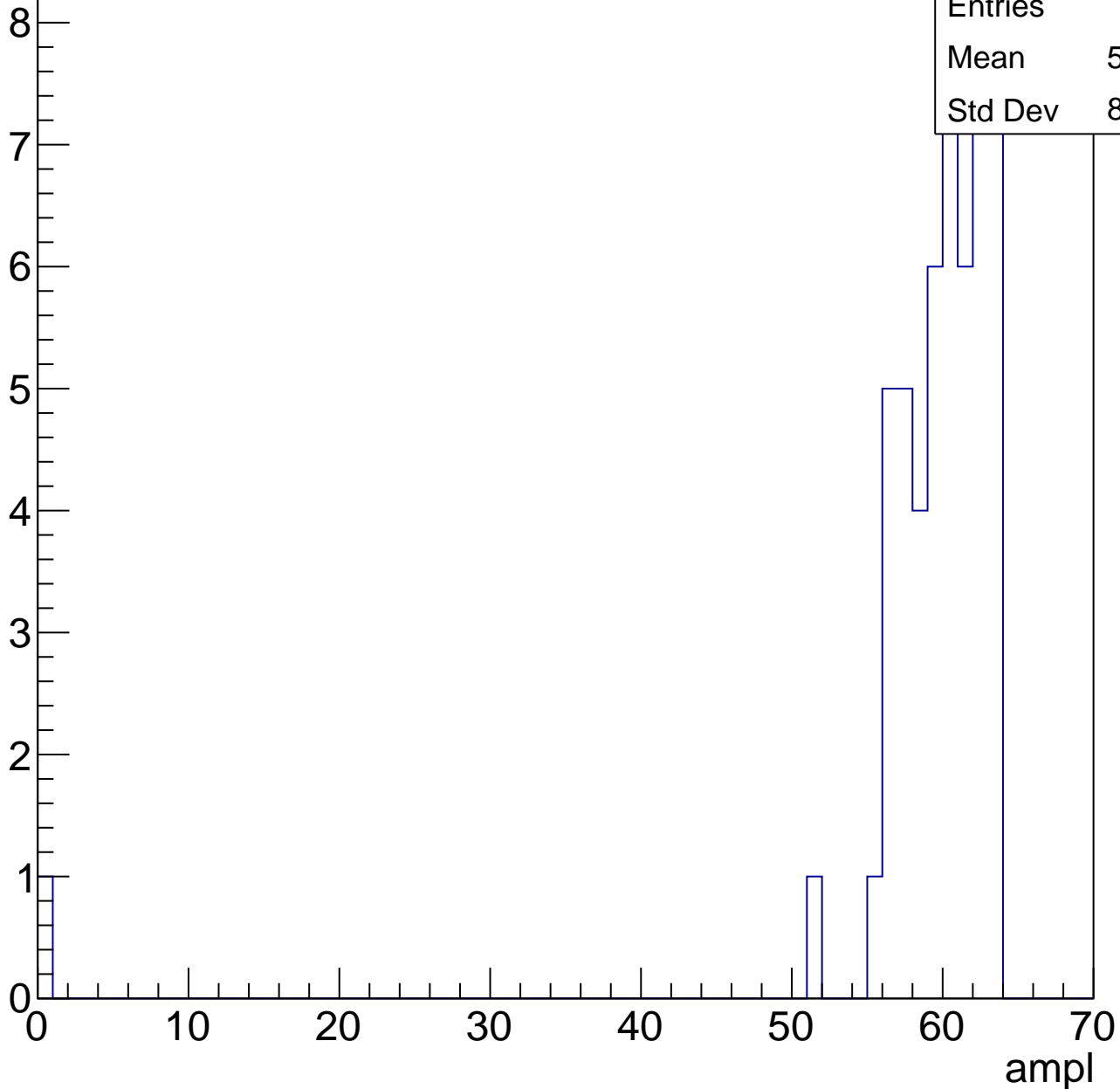


B1L103S, U5-ch17, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	58.55
Std Dev	8.524



B1L103S, U5-ch17, adc6

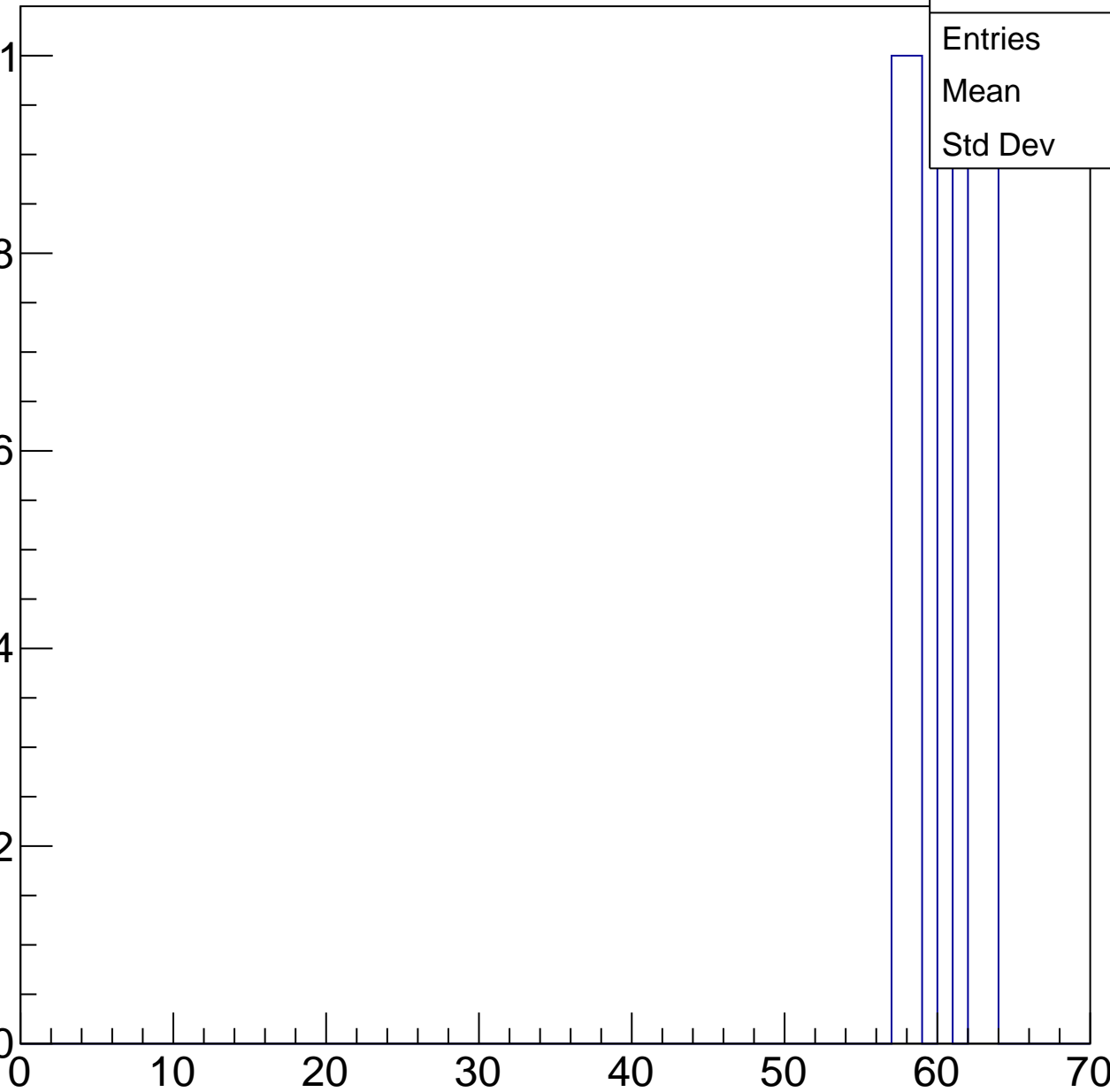
calib_packv5_041523_1651.root, FC#0, port C2

Entry

1
0.8
0.6
0.4
0.2
0

Entries	5
Mean	60
Std Dev	2.28

ampl



B1L103S, U5-ch17, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry



B1L103S, U5-ch18, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	69
Mean	22.91
Std Dev	11.84

Entry

14
12
10
8
6
4
2
0

0

10

20

30

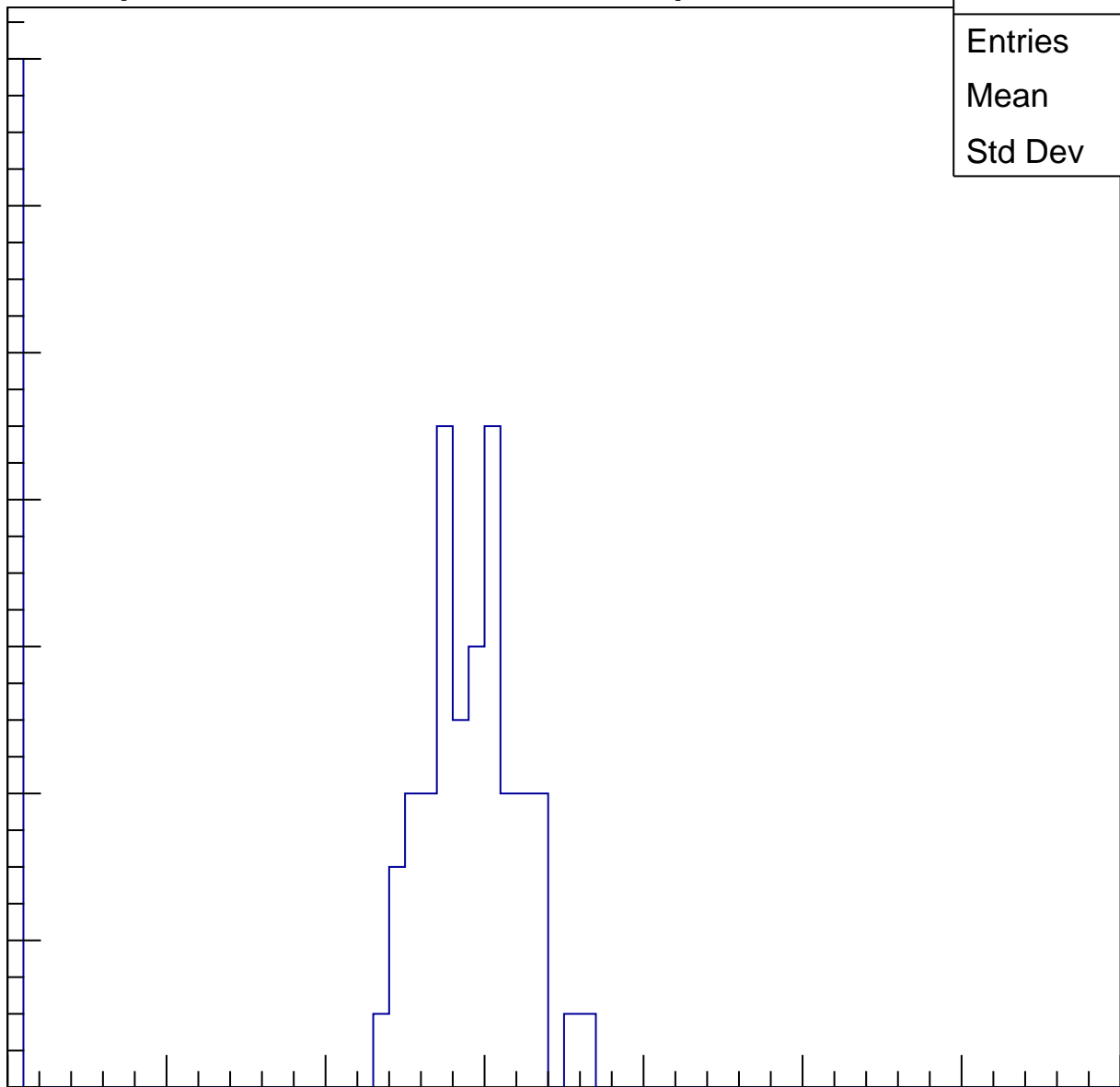
40

50

60

70

ampl

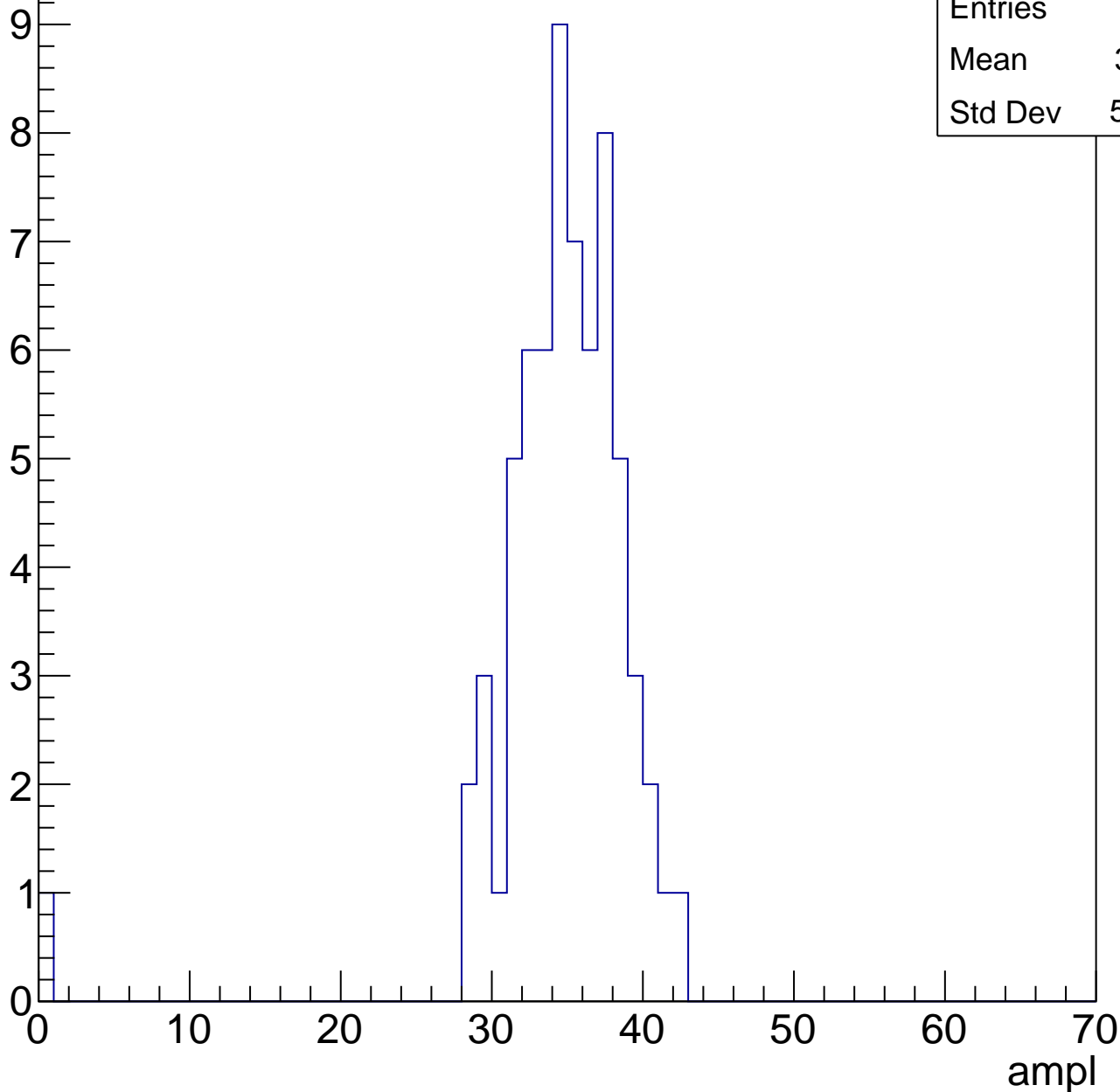


B1L103S, U5-ch18, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	34.11
Std Dev	5.275



B1L103S, U5-ch18, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	72
Mean	33.56
Std Dev	16.01

Entry

12

10

8

6

4

2

0

0

10

20

30

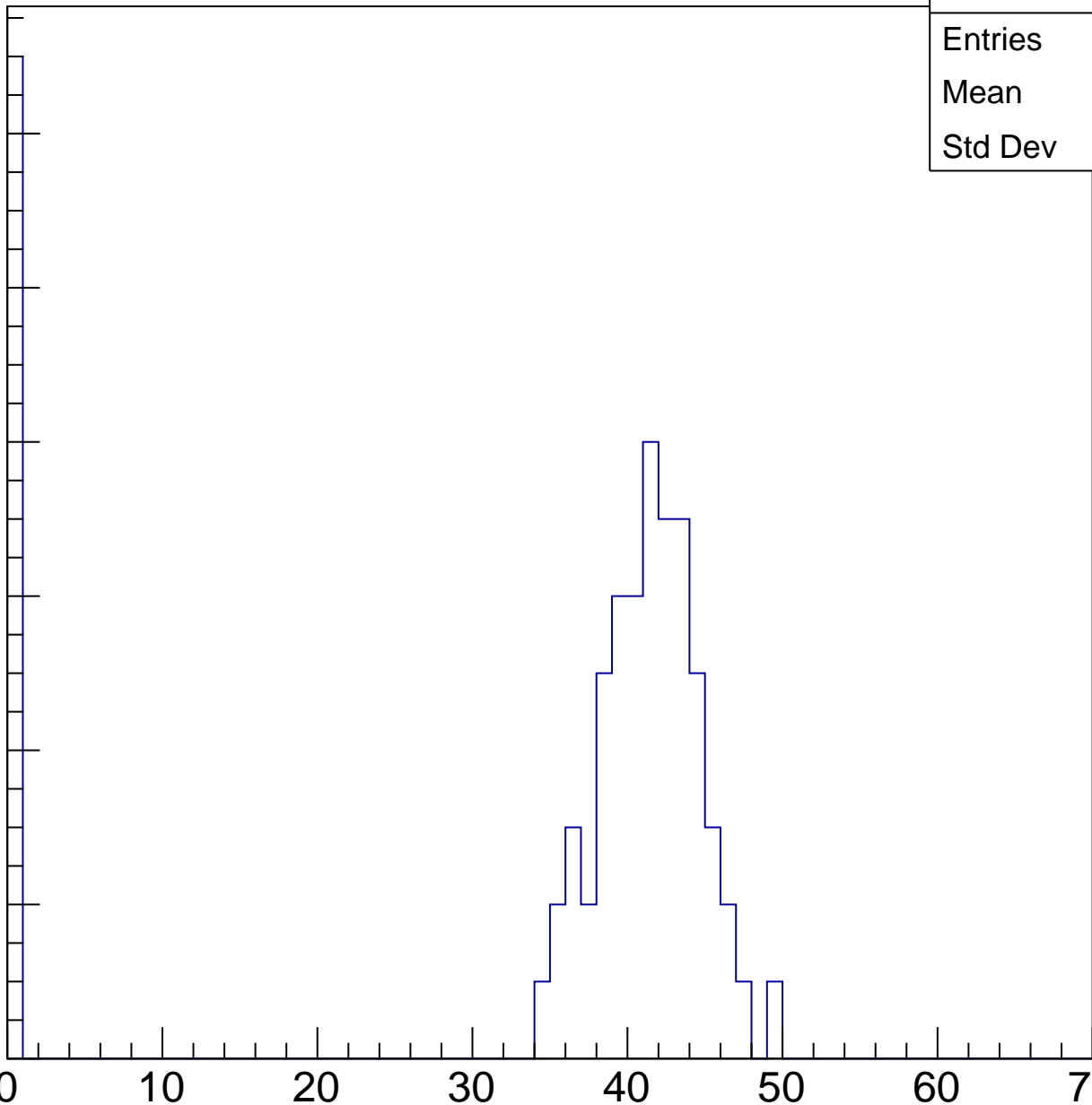
40

50

60

70

ampl

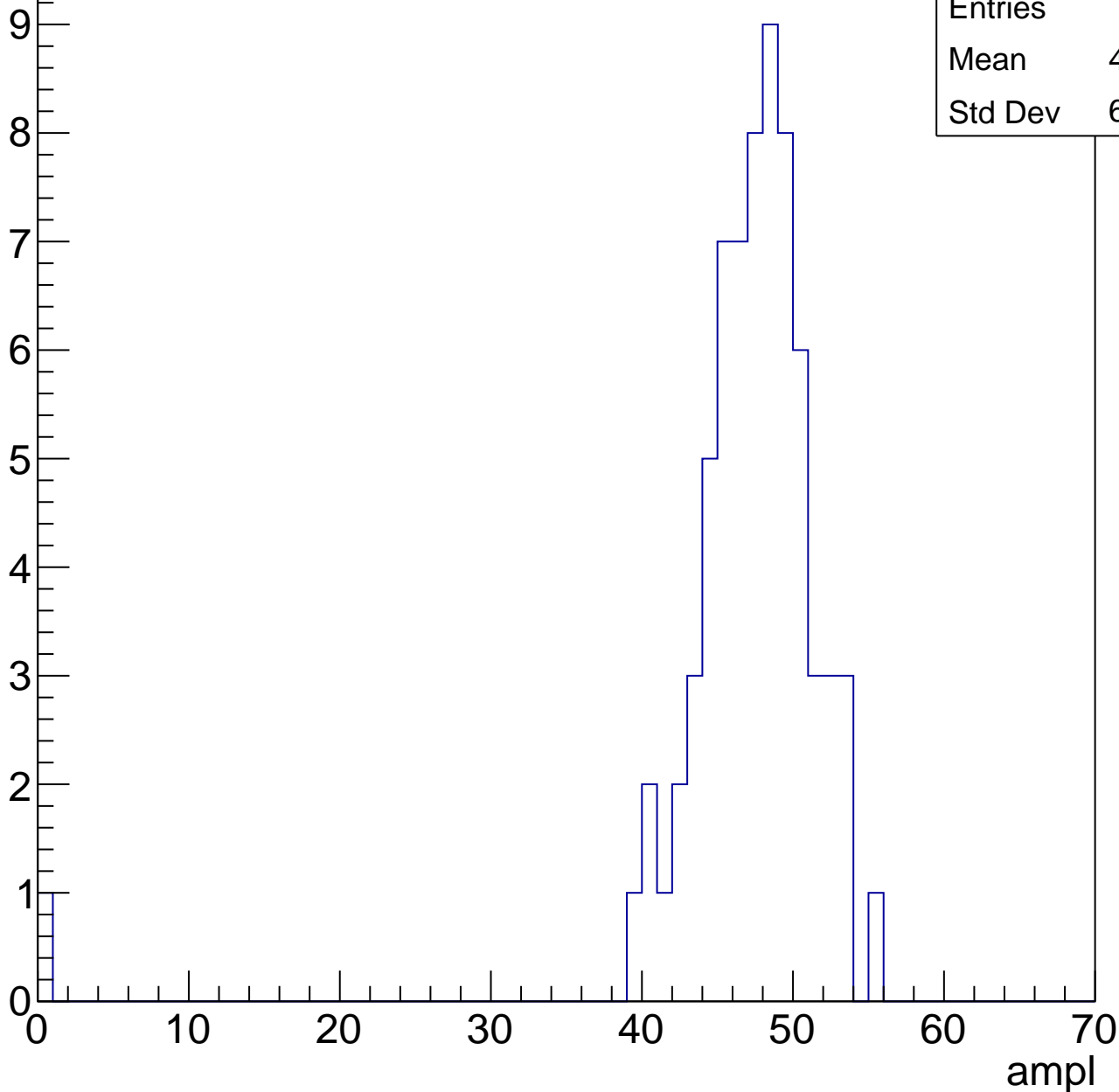


B1L103S, U5-ch18, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	46.47
Std Dev	6.498

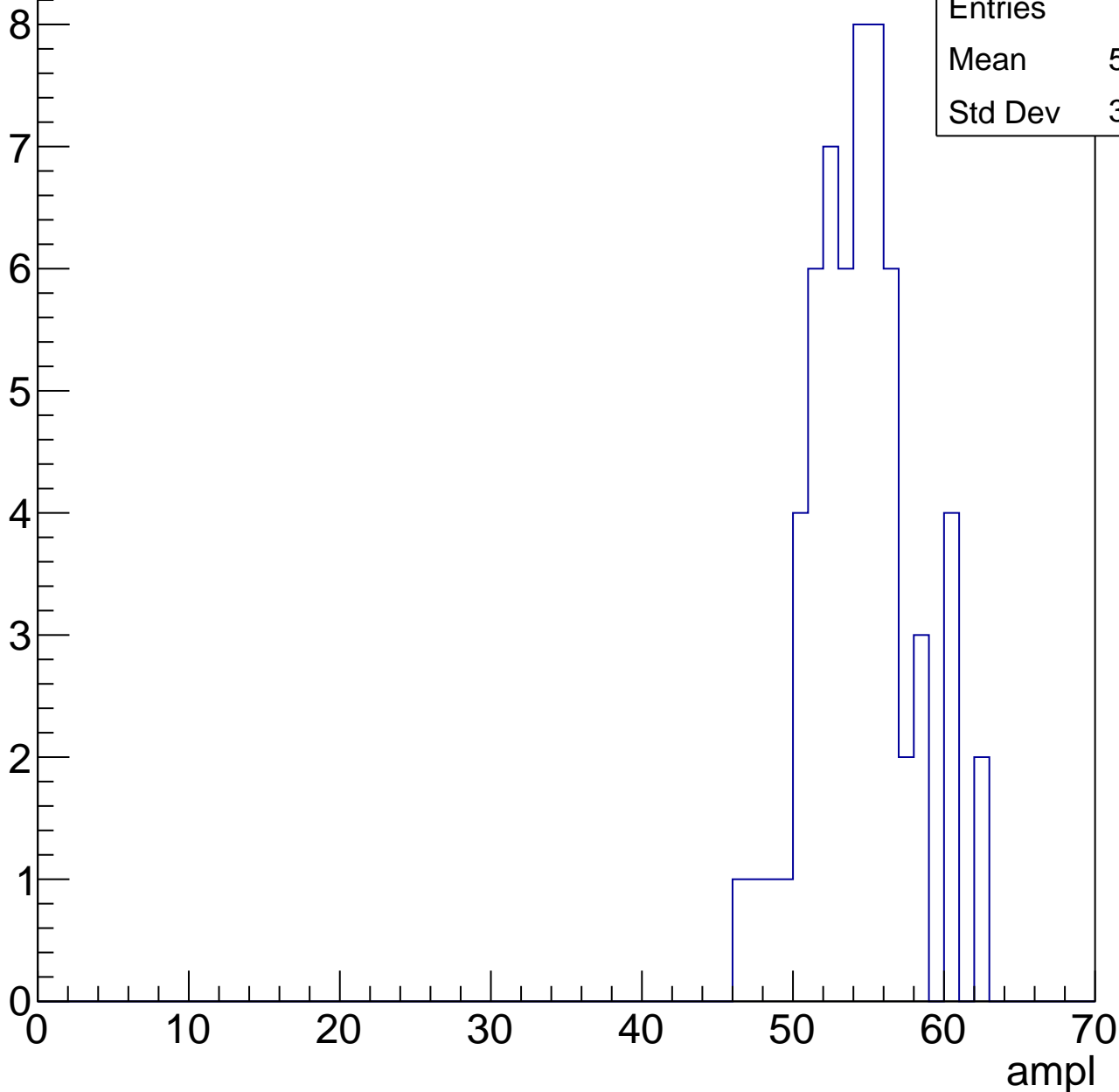


B1L103S, U5-ch18, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	53.97
Std Dev	3.406



B1L103S, U5-ch18, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entries	46
Mean	57.07
Std Dev	8.872

Entry

10

8

6

4

2

0

0

10

20

30

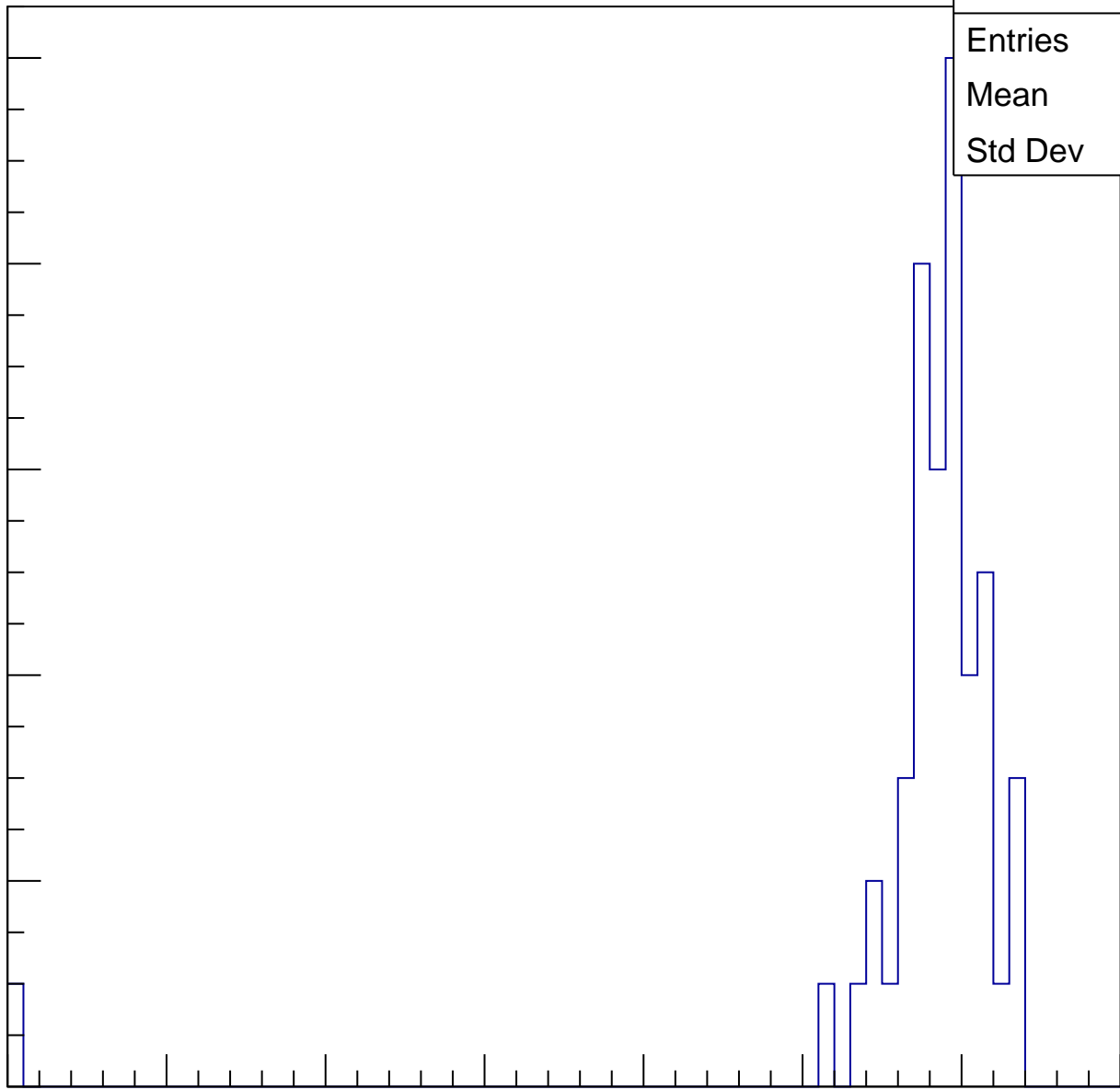
40

50

60

70

ampl

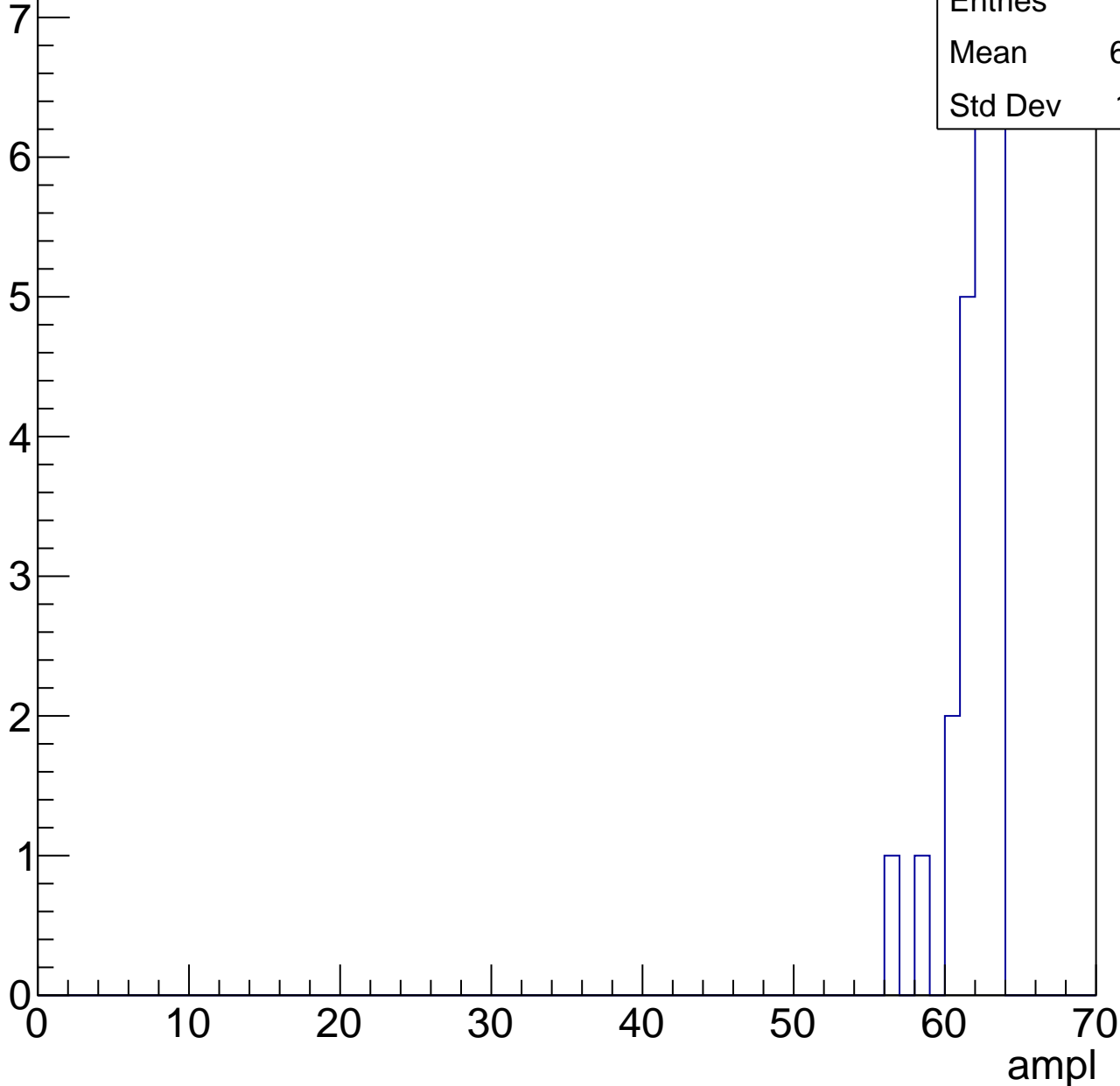


B1L103S, U5-ch18, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	23
Mean	61.48
Std Dev	1.691

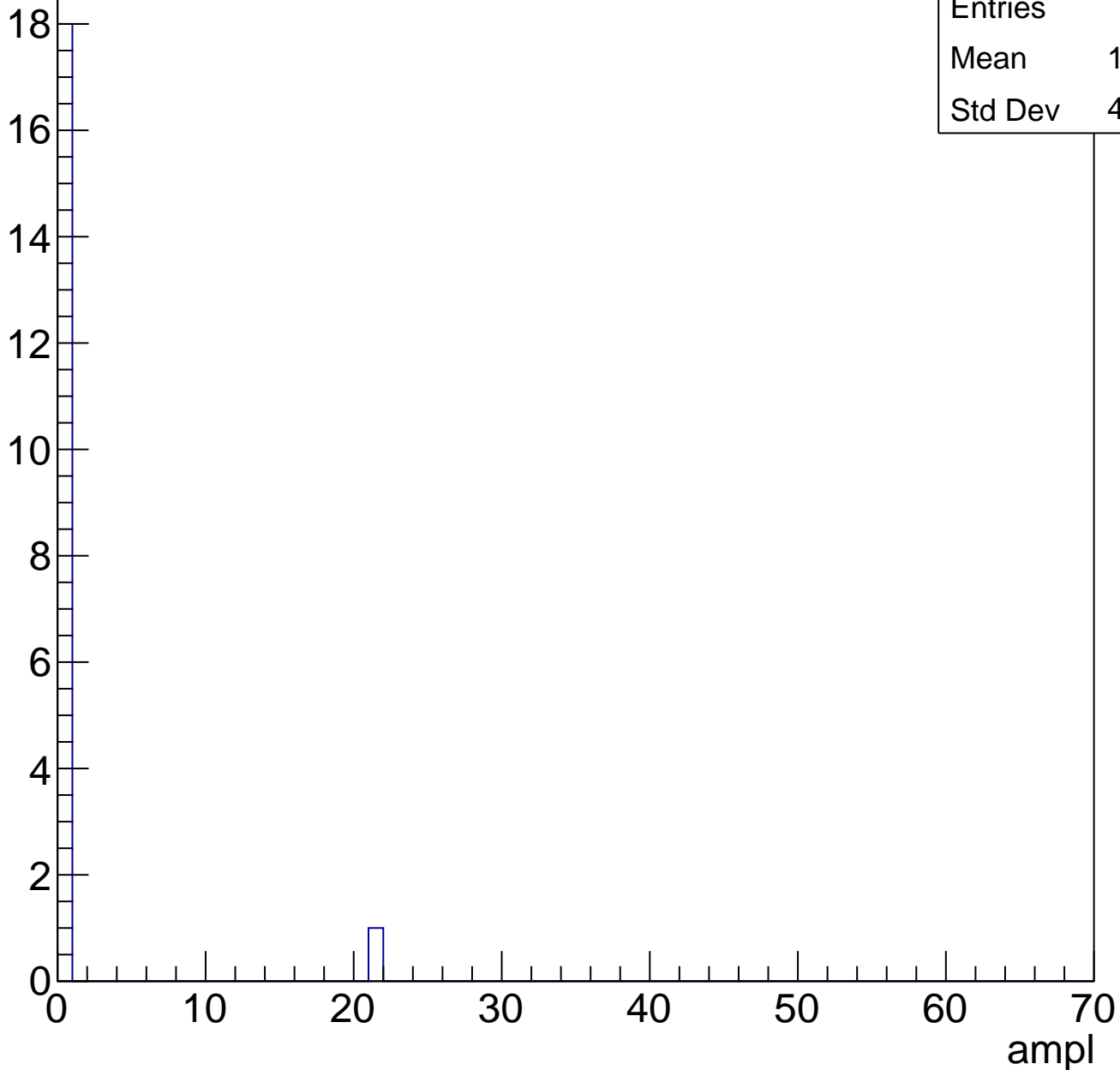


B1L103S, U5-ch18, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.105
Std Dev	4.689

Entry

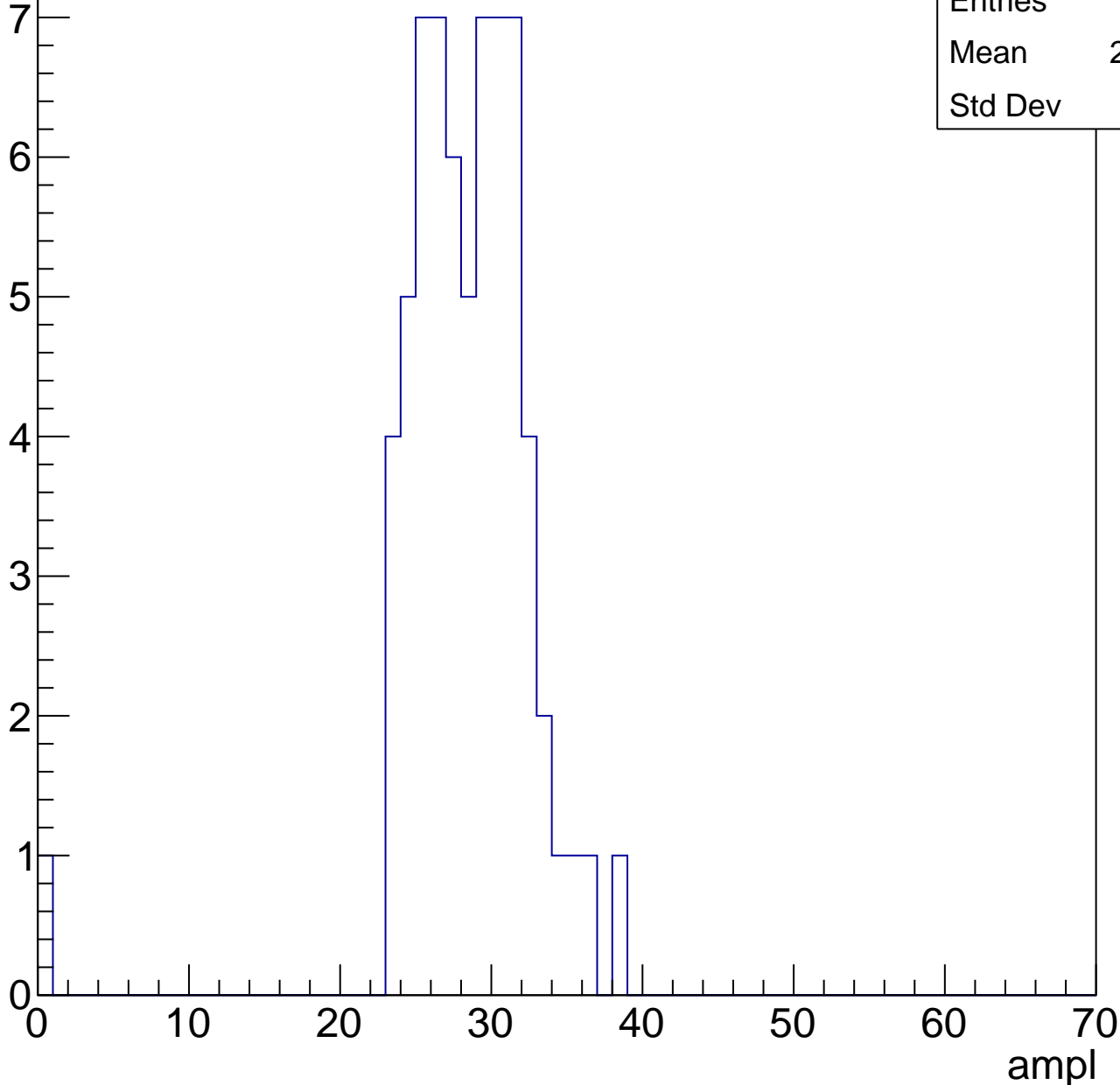


B1L103S, U5-ch19, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	27.85
Std Dev	4.8

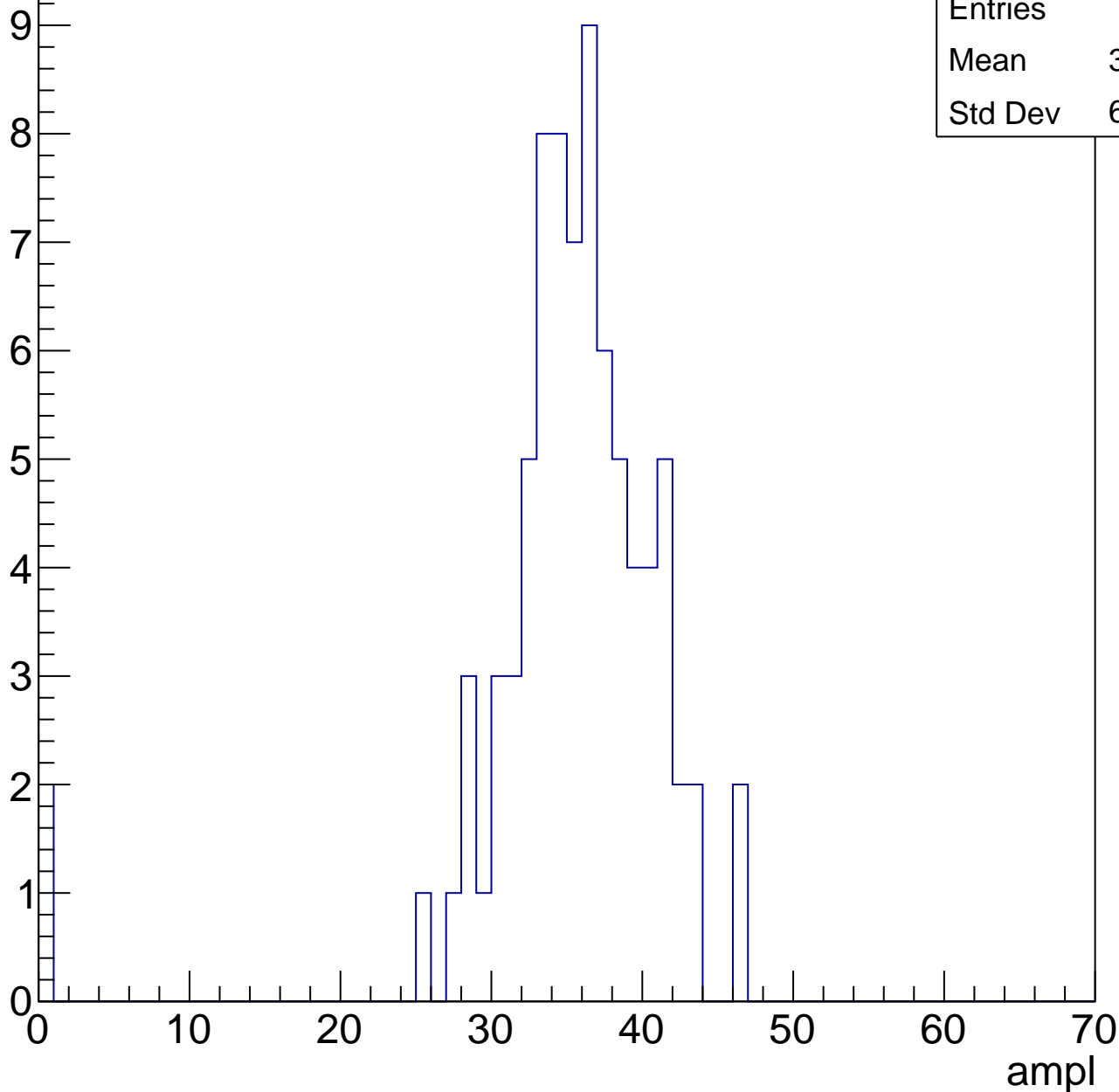


B1L103S, U5-ch19, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	81
Mean	34.67
Std Dev	6.926

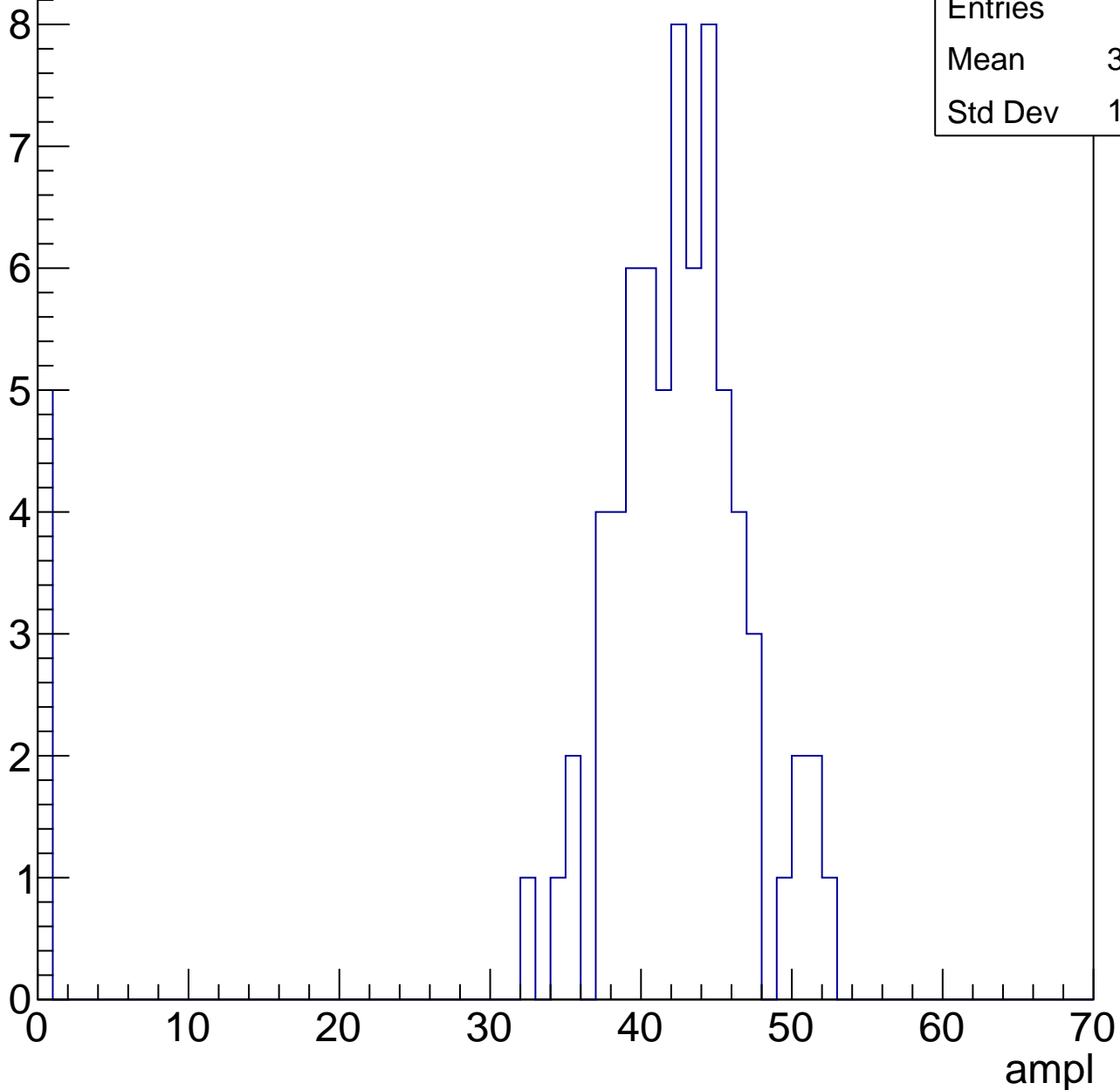


B1L103S, U5-ch19, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	39.38
Std Dev	11.32

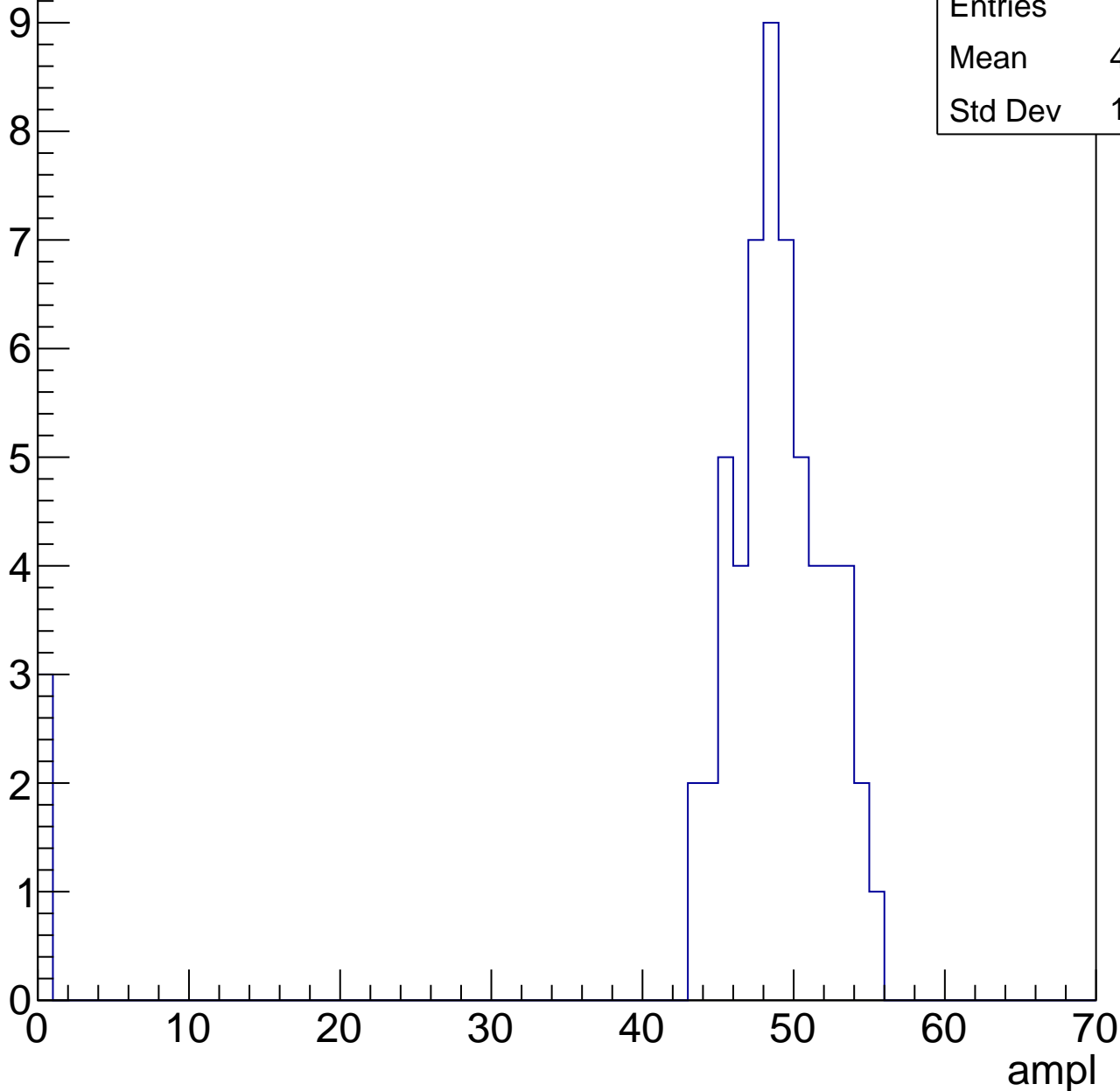


B1L103S, U5-ch19, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	46.17
Std Dev	11.06

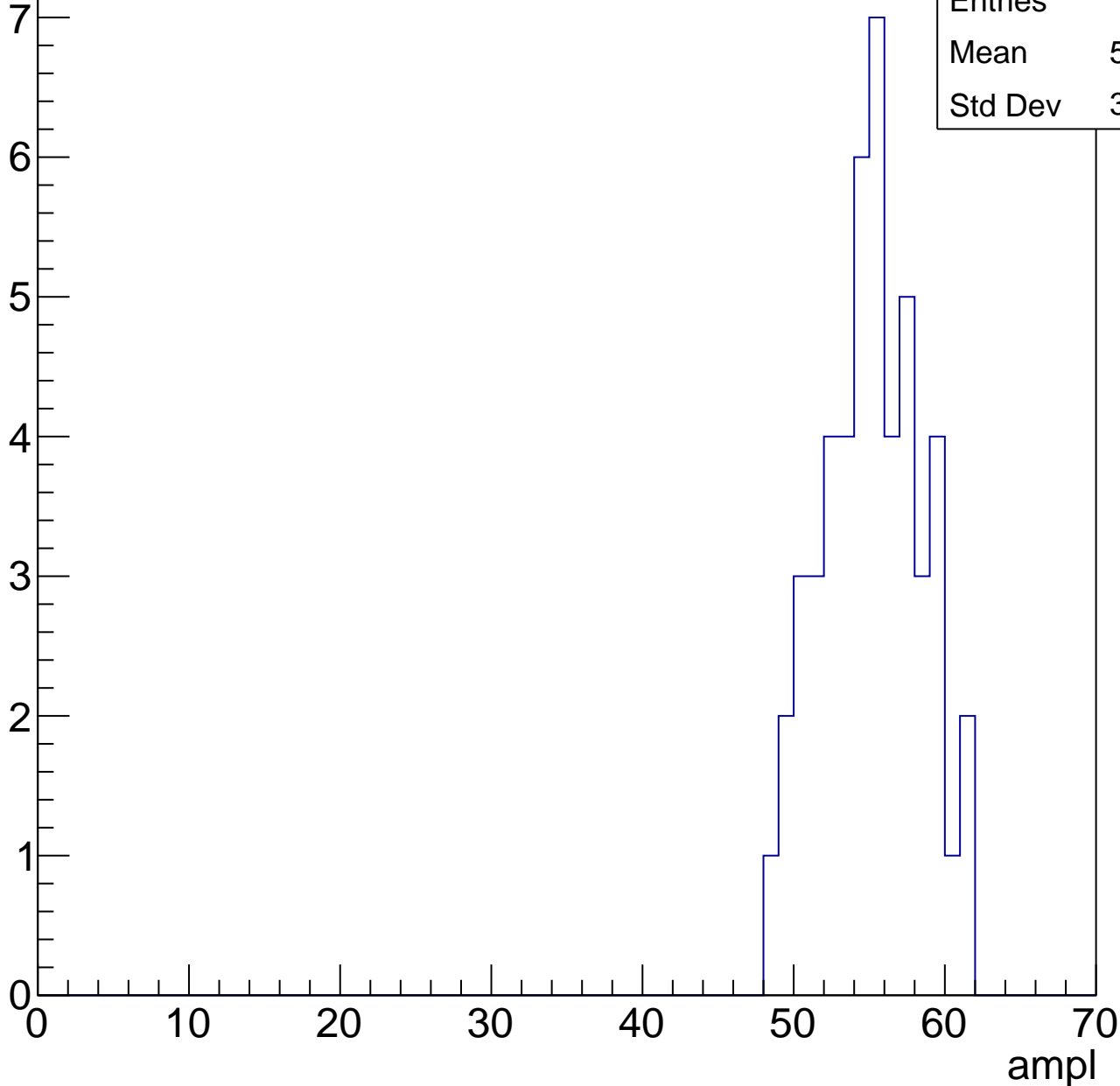


B1L103S, U5-ch19, adc4

calib_packv5_041523_1651.root, FC#0, port C2

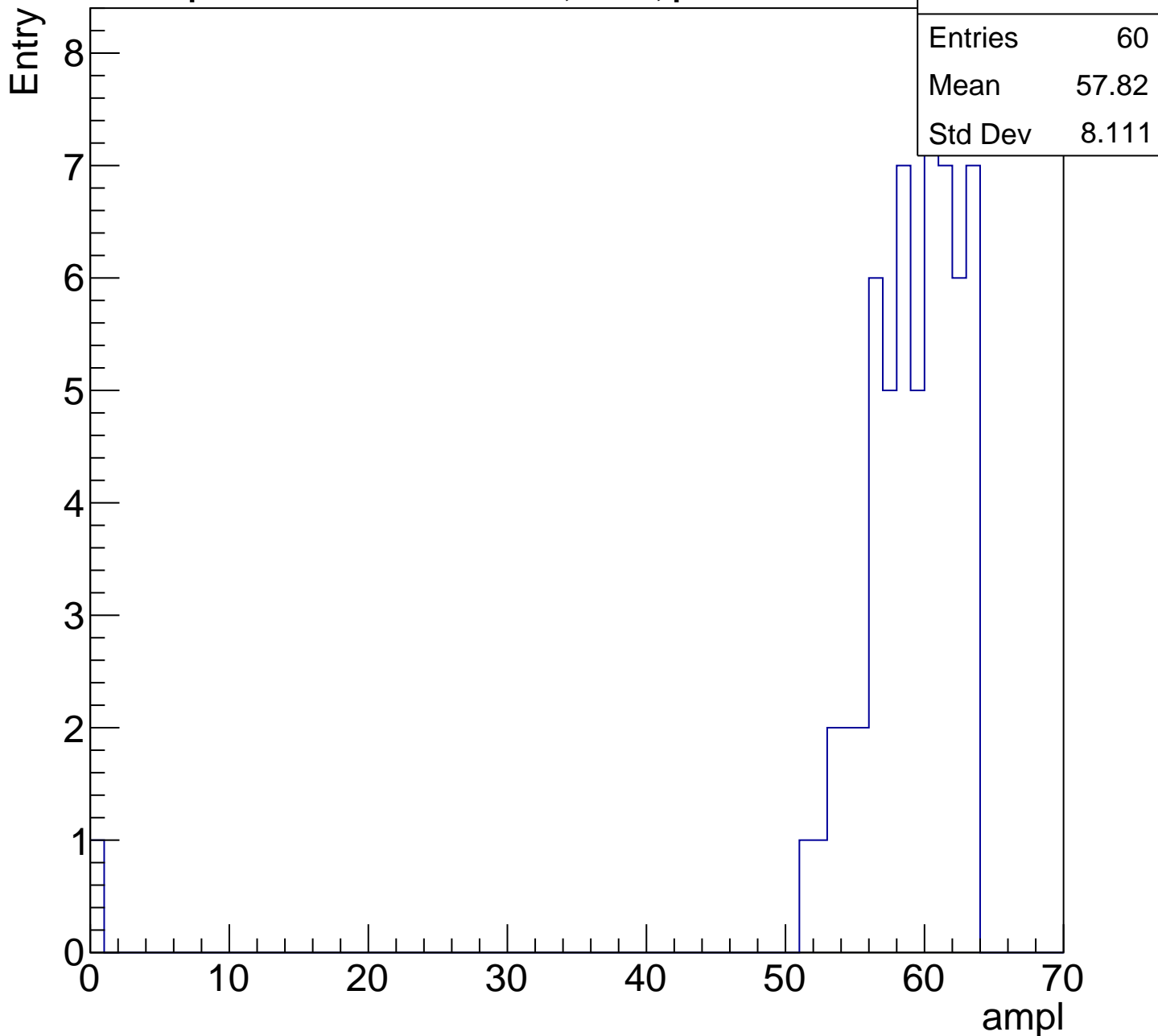
Entry

Entries	49
Mean	54.67
Std Dev	3.222



B1L103S, U5-ch19, adc5

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U5-ch19, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

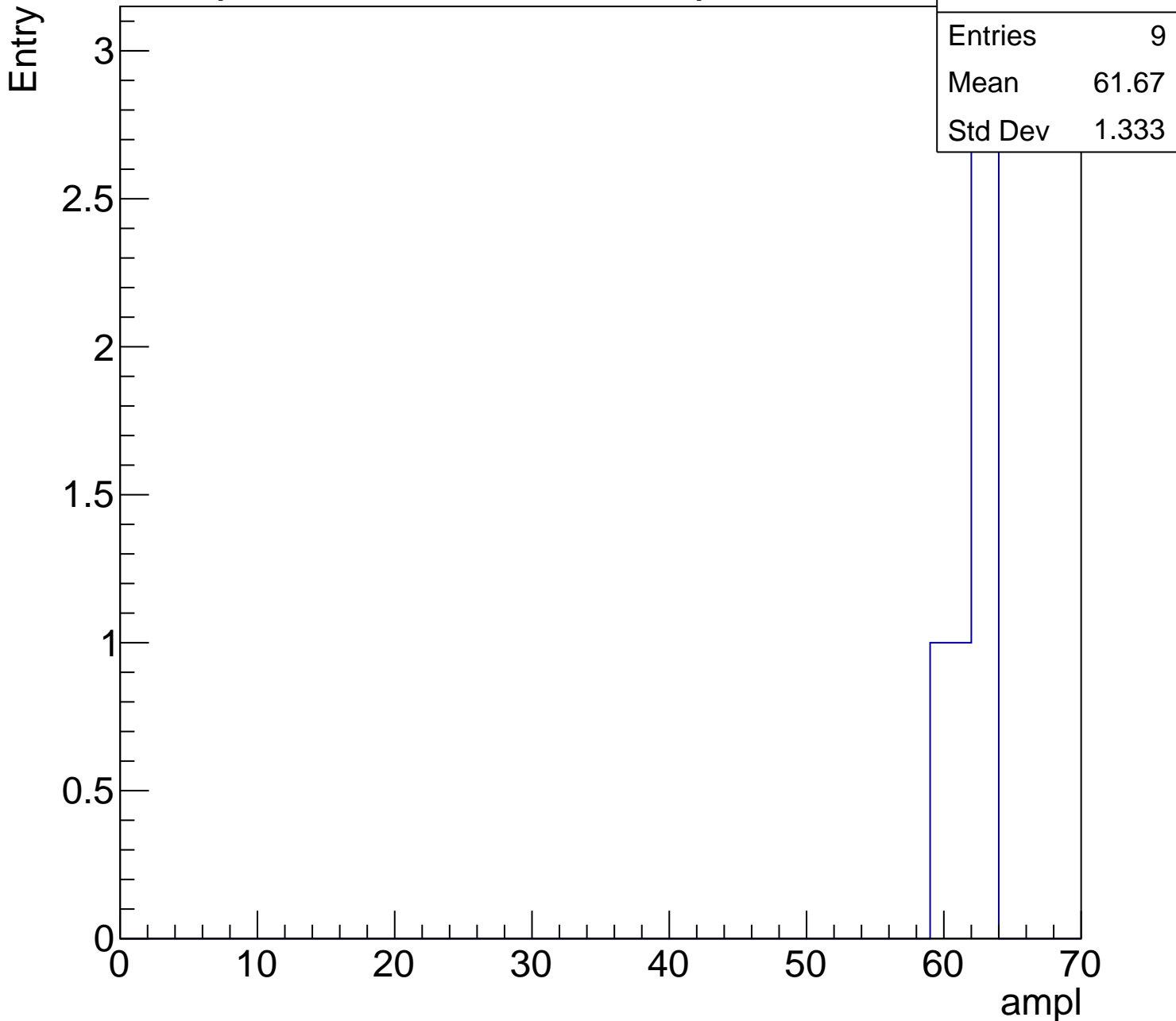
9

Mean

61.67

Std Dev

1.333

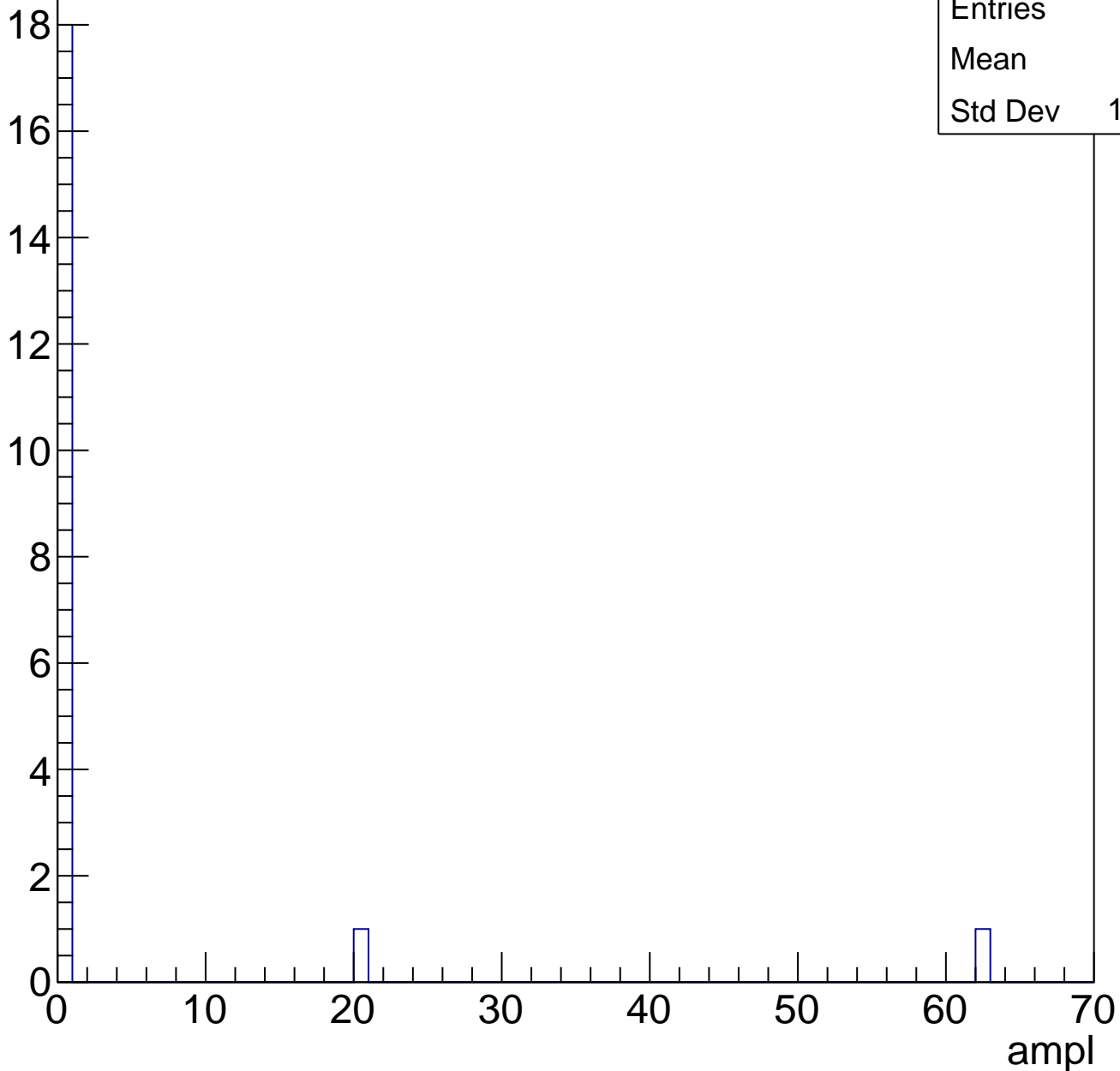


B1L103S, U5-ch19, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	4.1
Std Dev	13.98

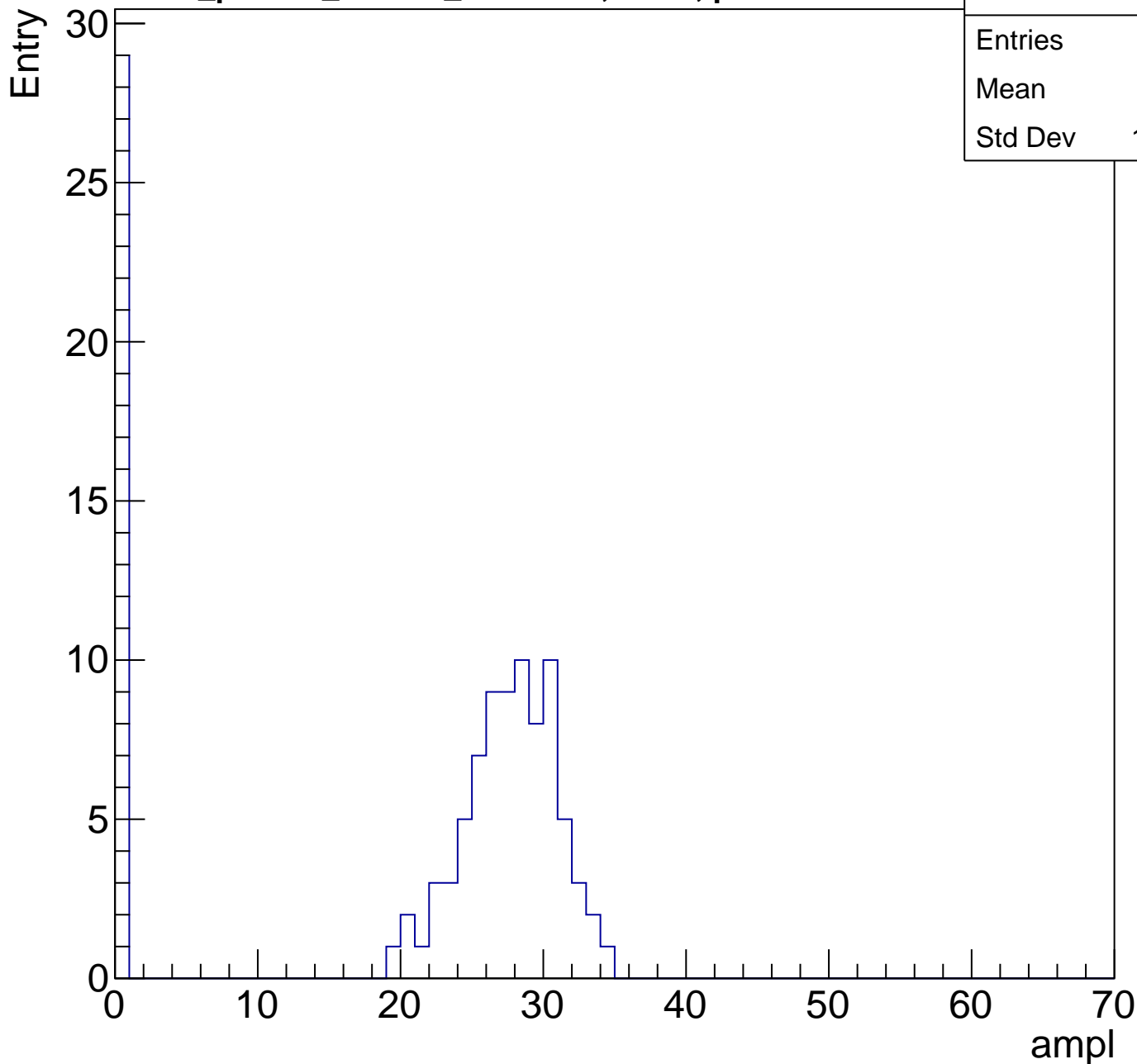
Entry



B1L103S, U5-ch20, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	108
Mean	19.91
Std Dev	12.37

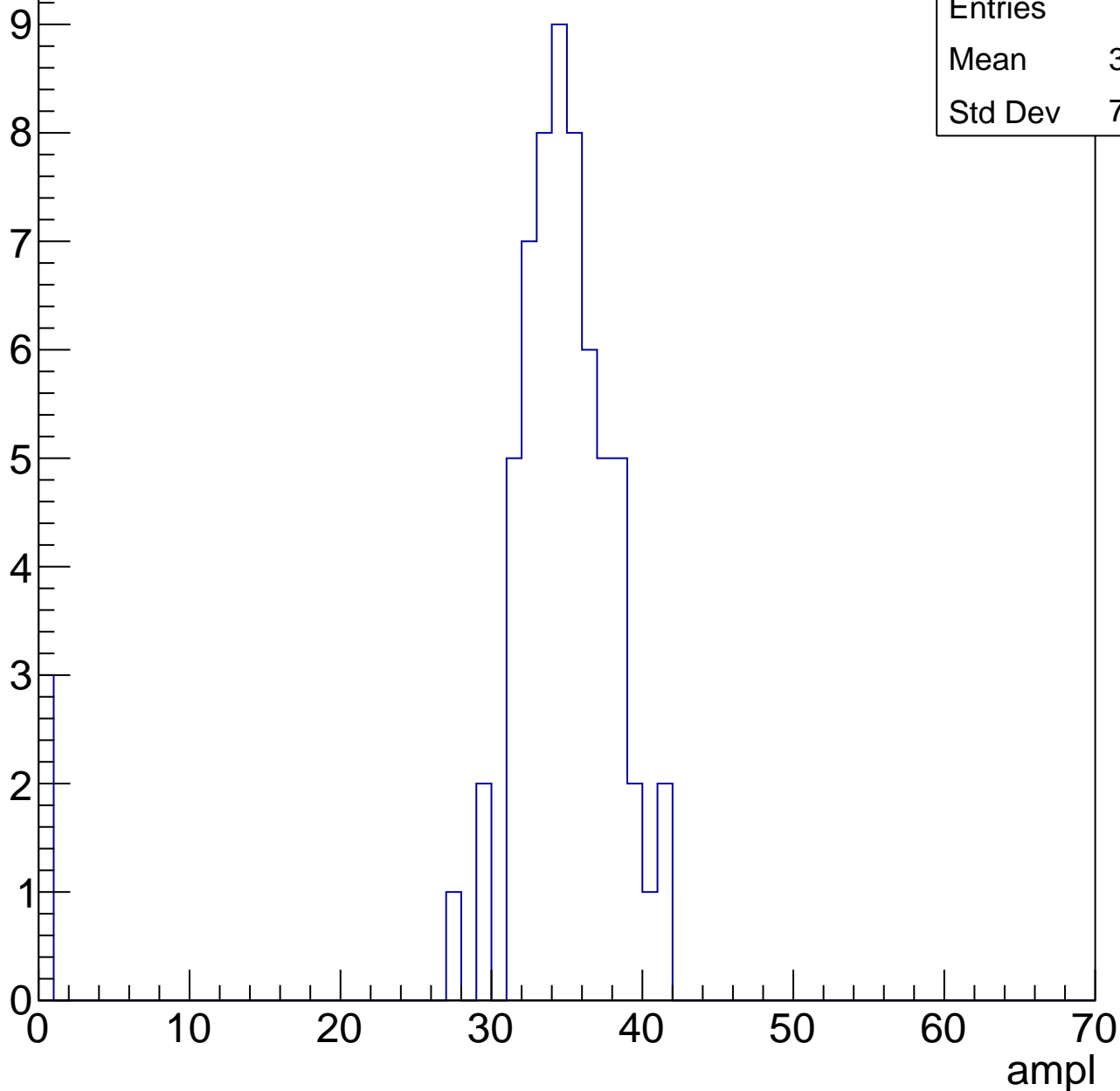


B1L103S, U5-ch20, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	32.89
Std Dev	7.816



B1L103S, U5-ch20, adc2

calib_packv5_041523_1651.root, FC#0, port C2

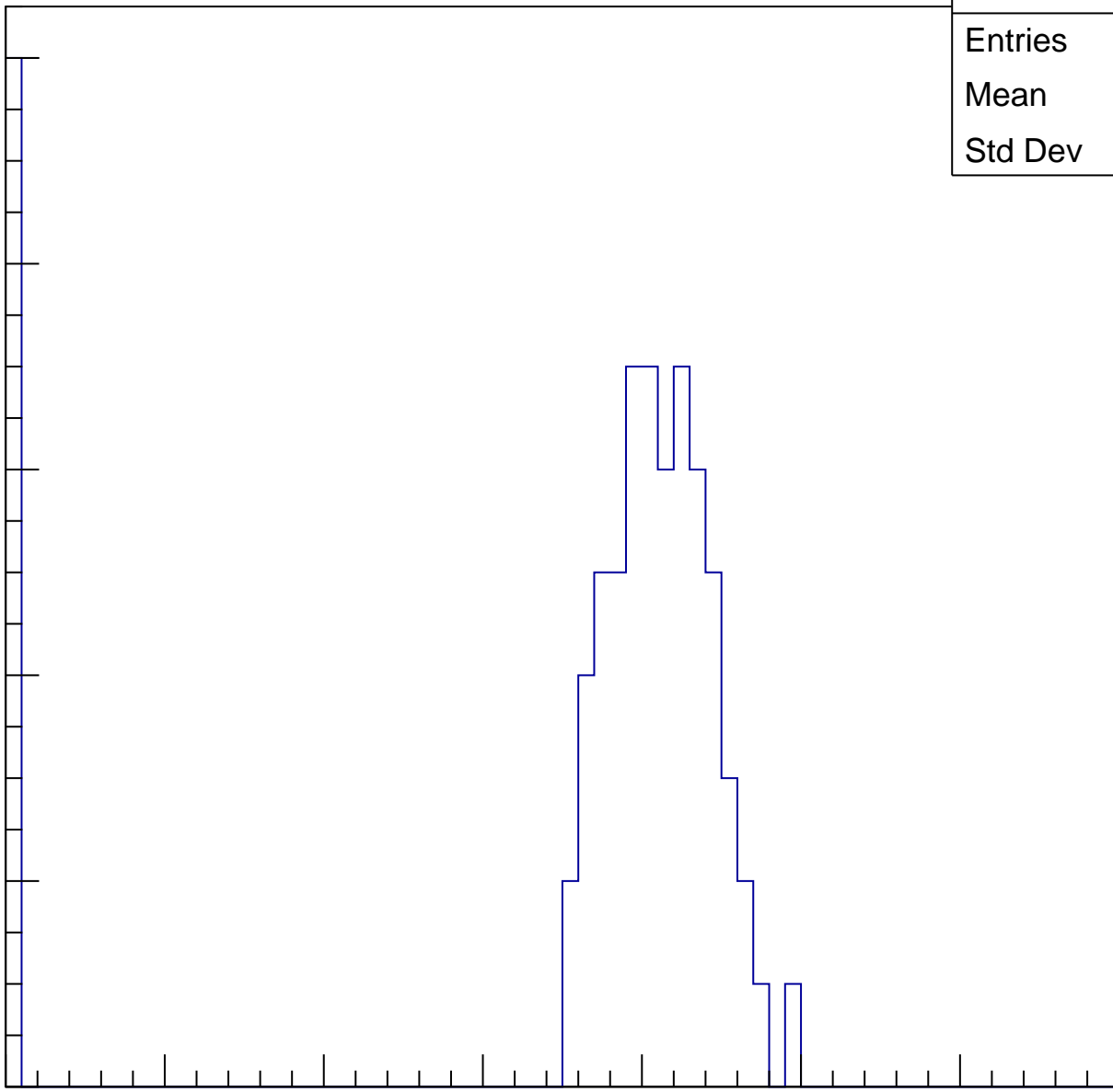
Entries	71
Mean	34.97
Std Dev	14.46

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

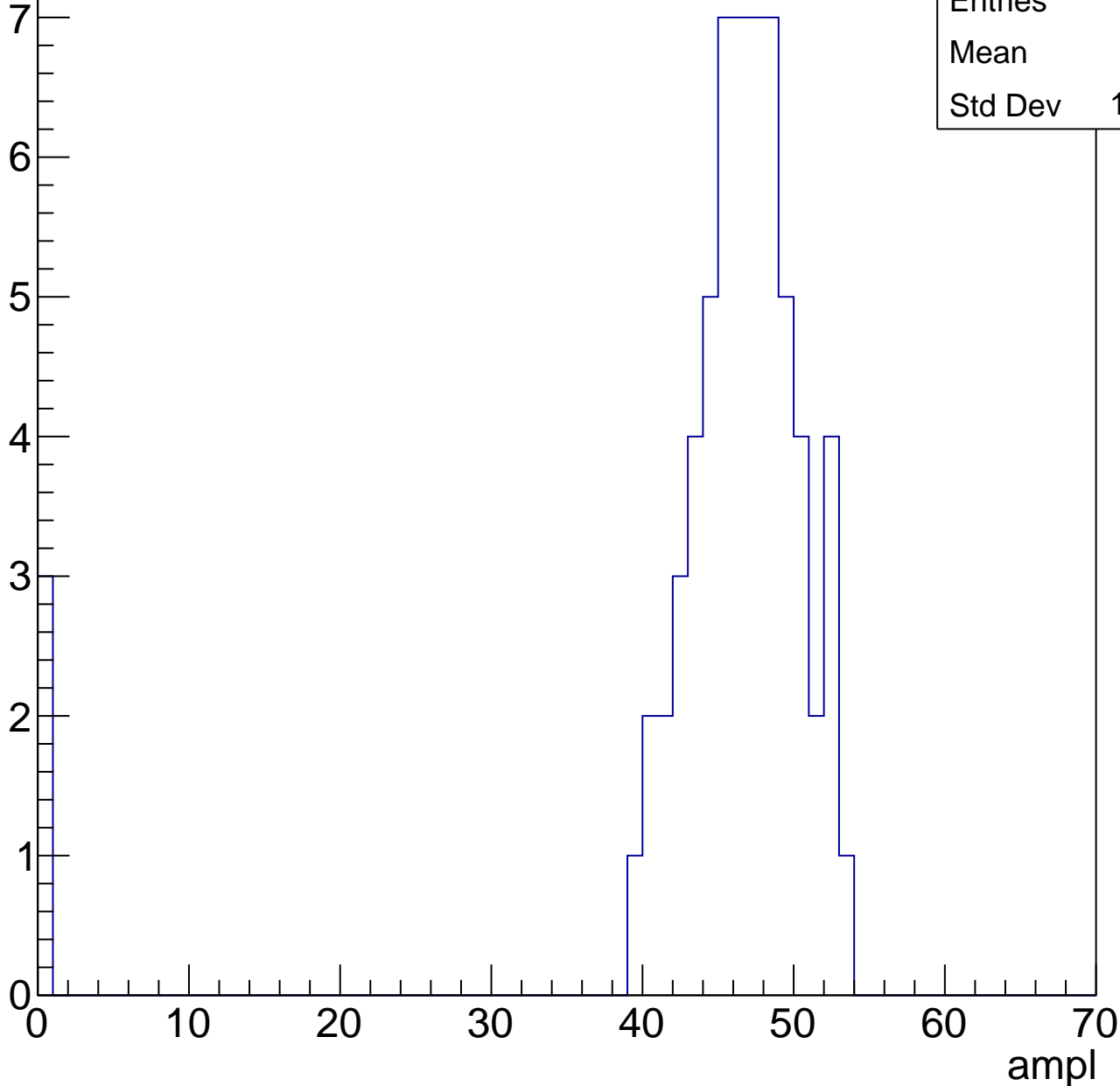


B1L103S, U5-ch20, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	44.2
Std Dev	10.32

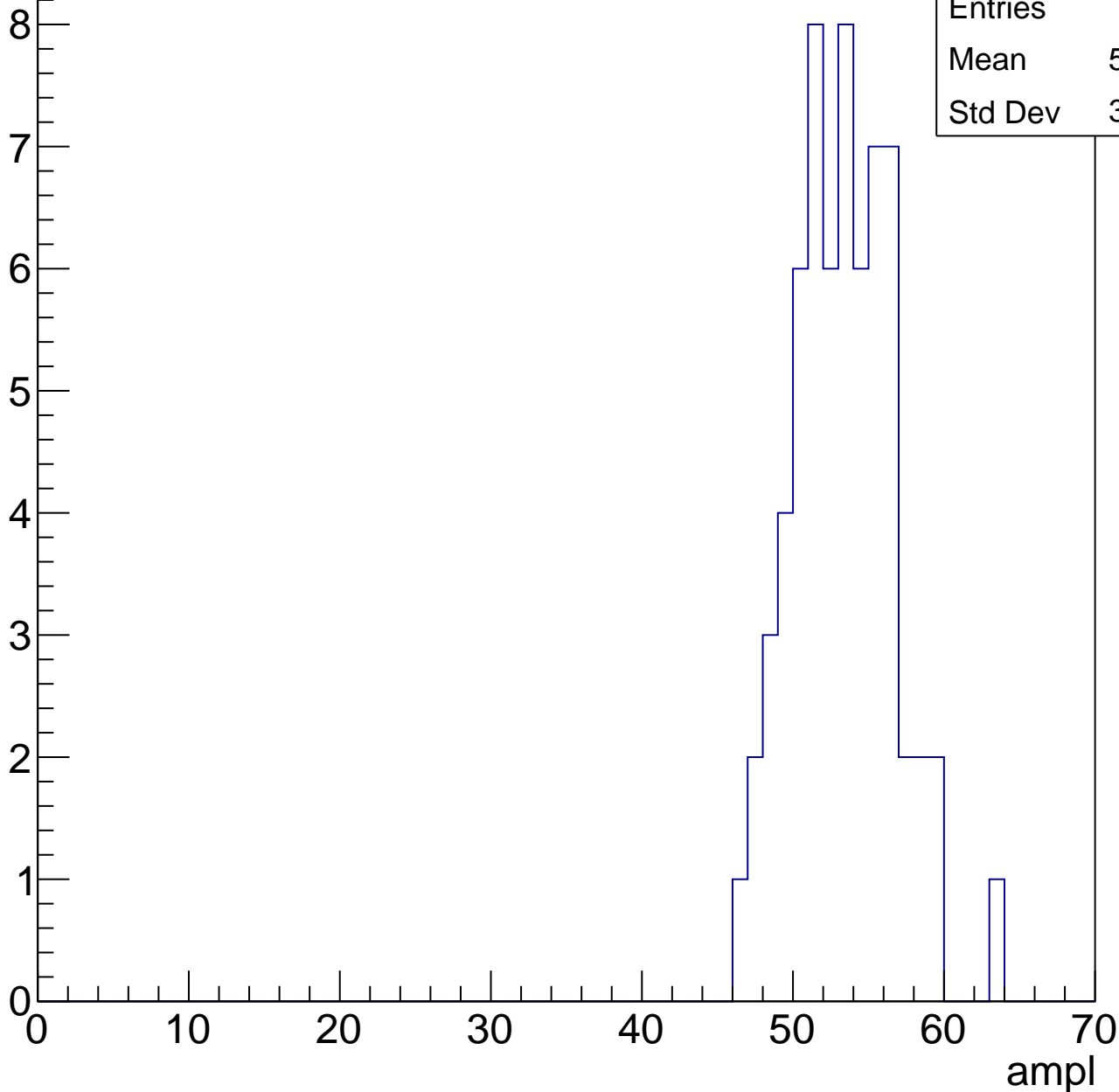


B1L103S, U5-ch20, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	52.86
Std Dev	3.286

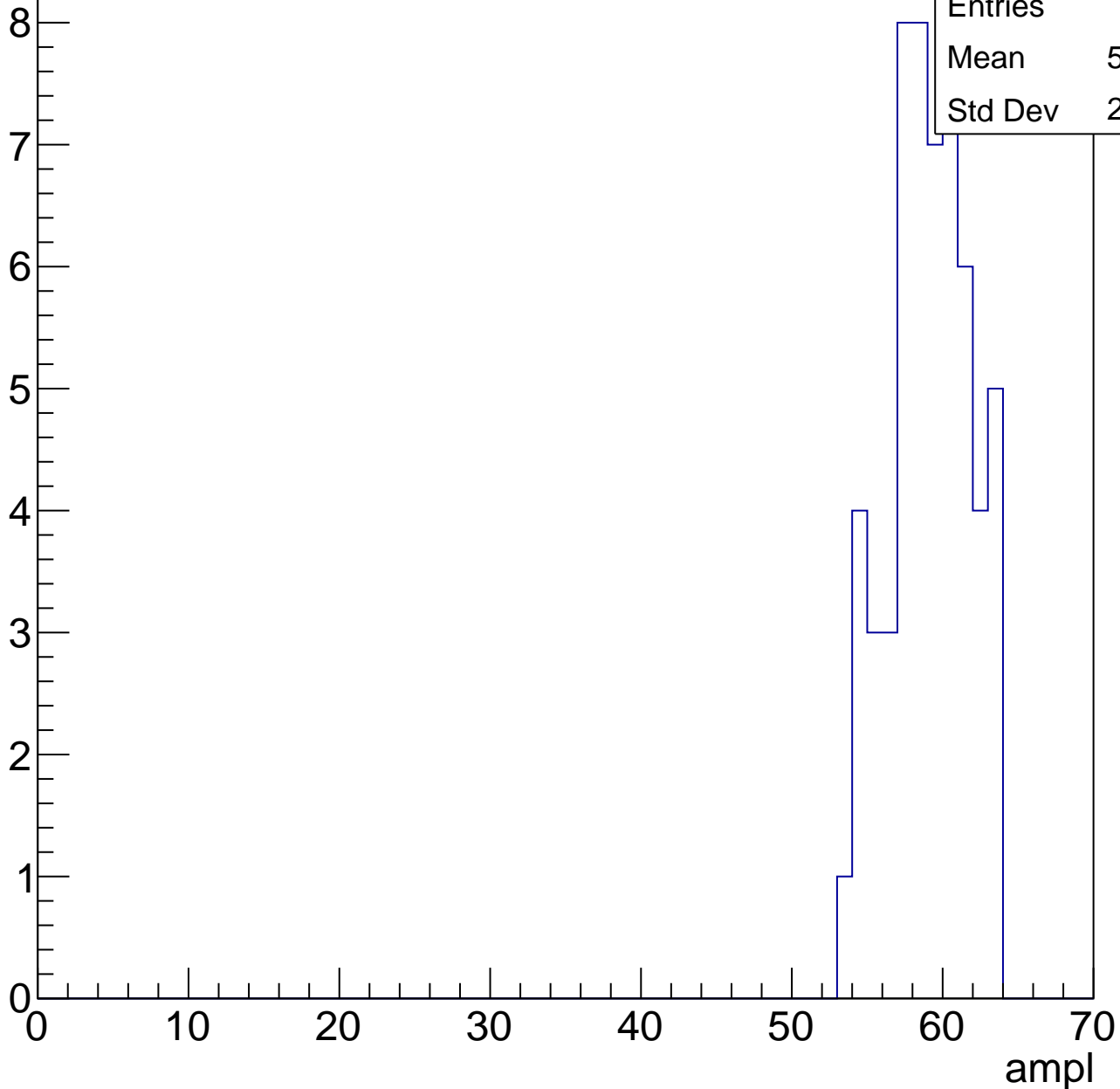


B1L103S, U5-ch20, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	58.67
Std Dev	2.625

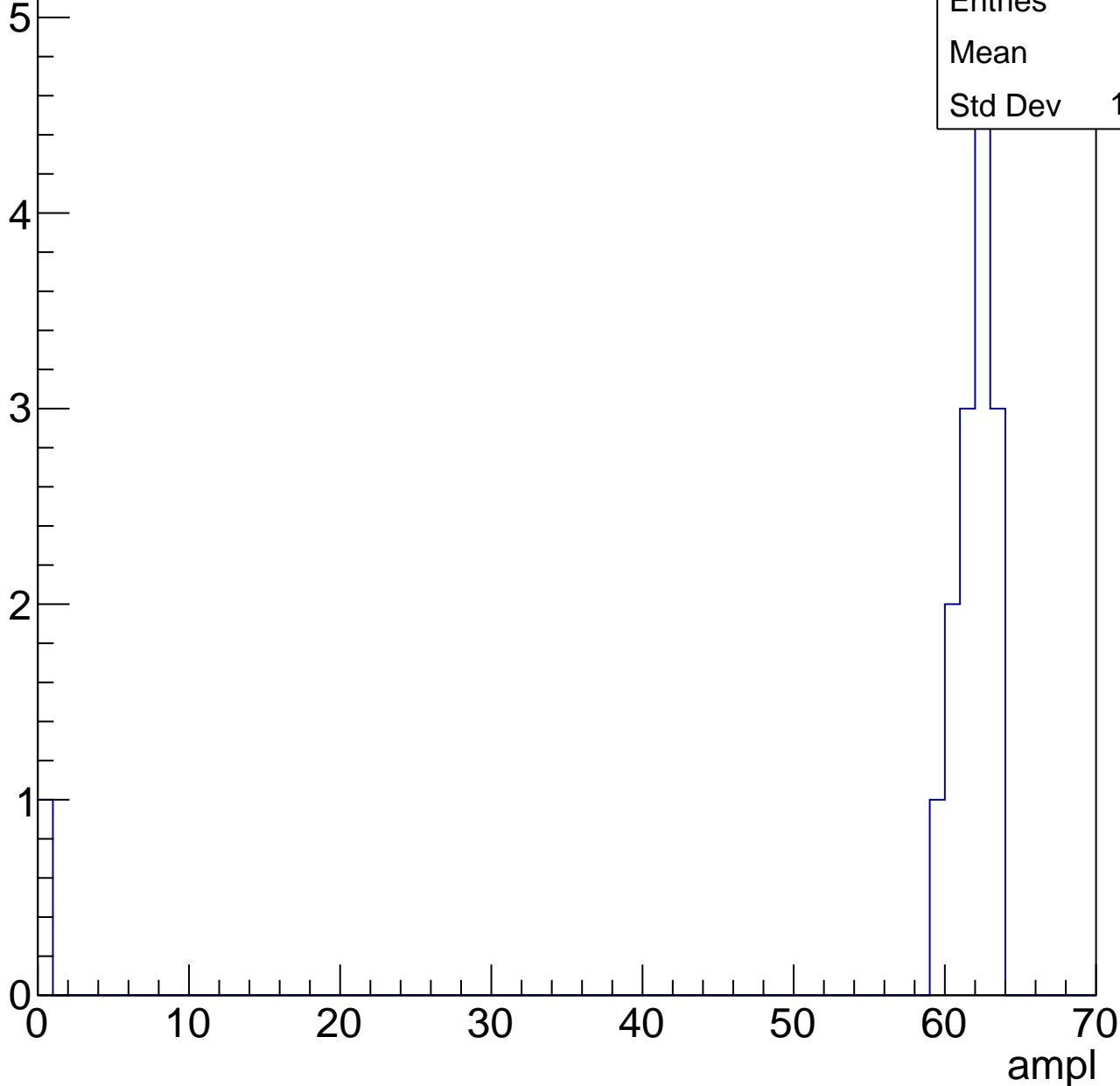


B1L103S, U5-ch20, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	15
Mean	57.4
Std Dev	15.38

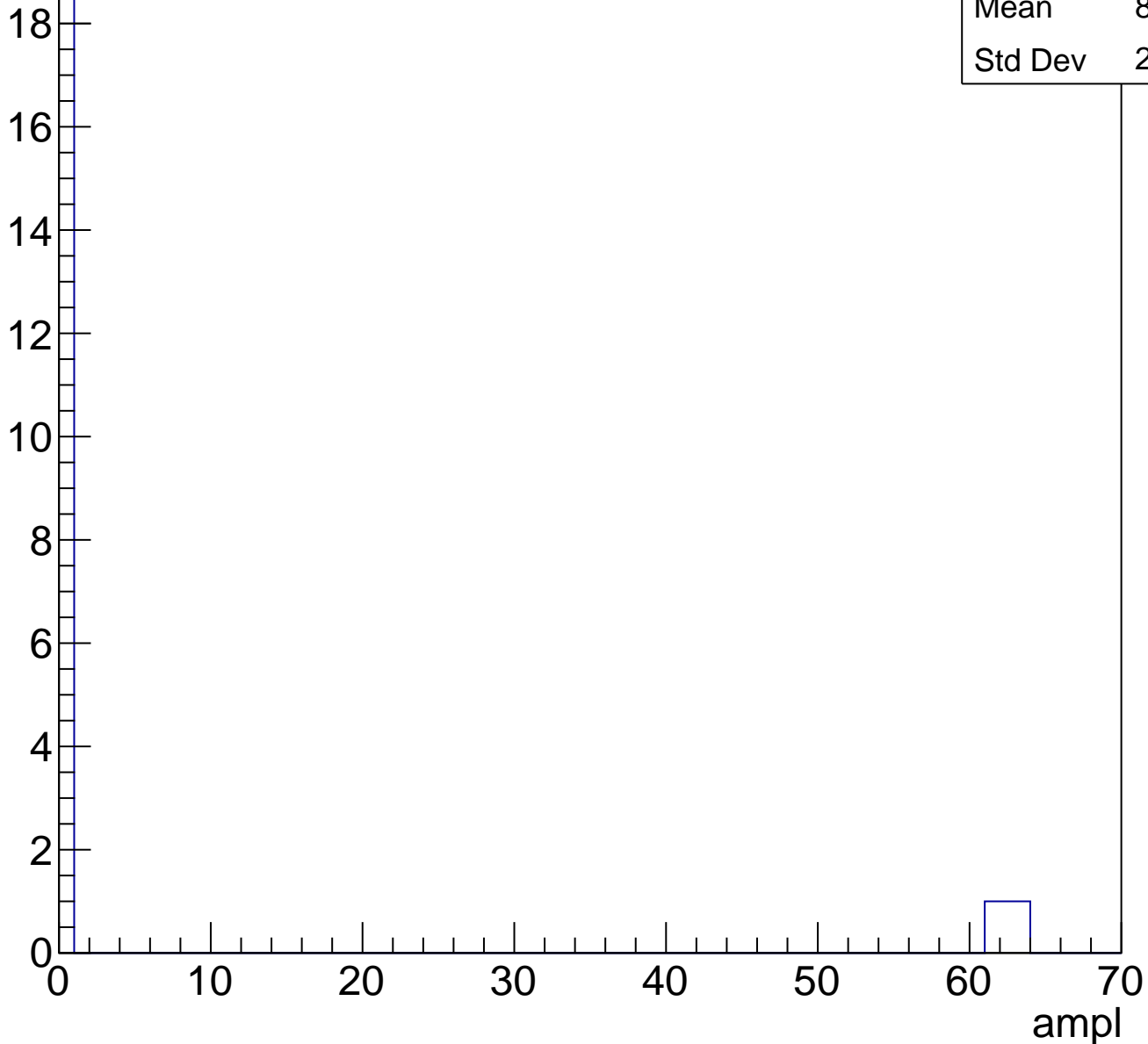


B1L103S, U5-ch20, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	22
Mean	8.455
Std Dev	21.28

Entry

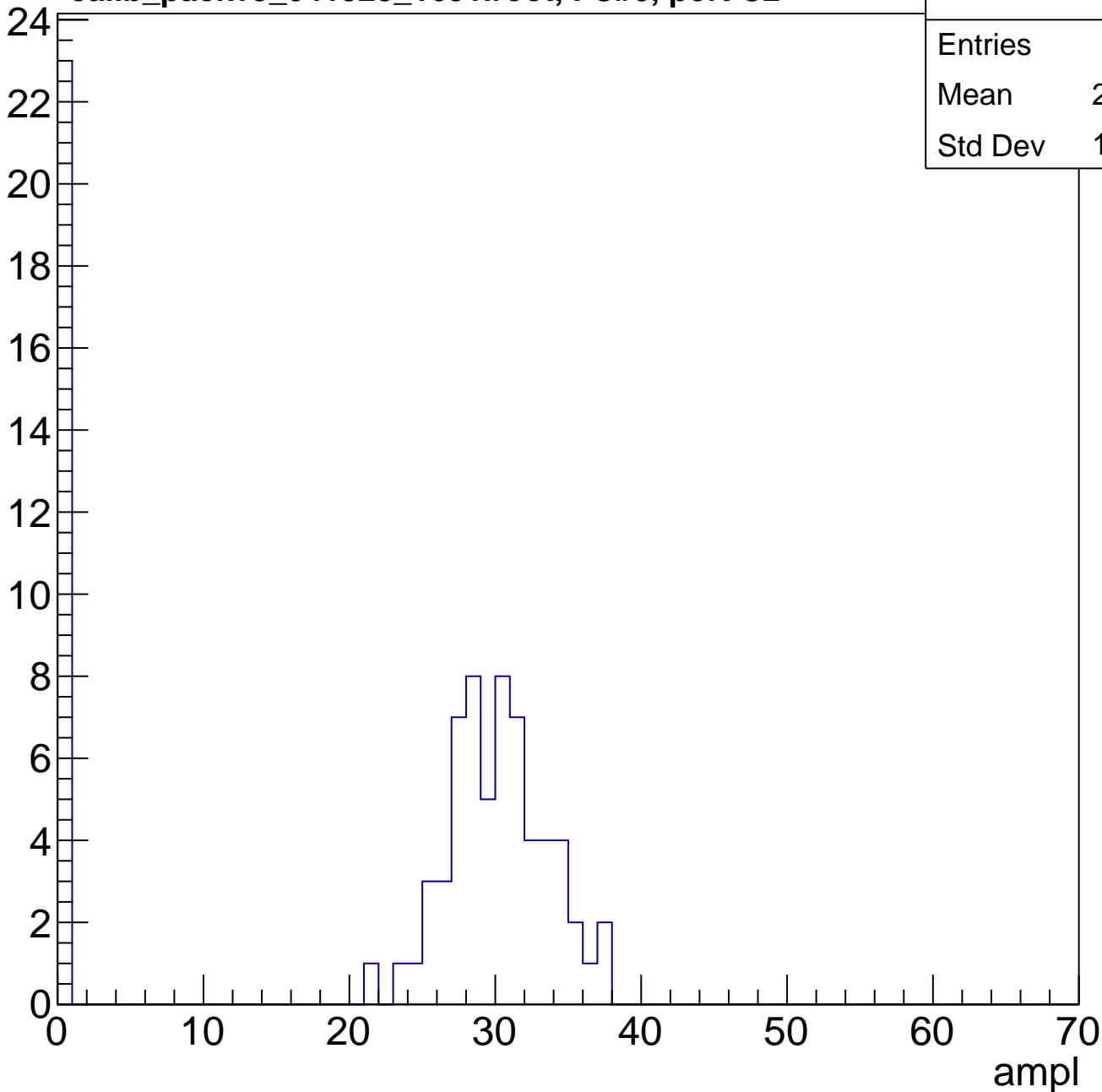


B1L103S, U5-ch21, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	84
Mean	21.57
Std Dev	13.55

Entry



B1L103S, U5-ch21, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	88
Mean	32.03
Std Dev	12.67

Entry

10

8

6

4

2

0

0

10

20

30

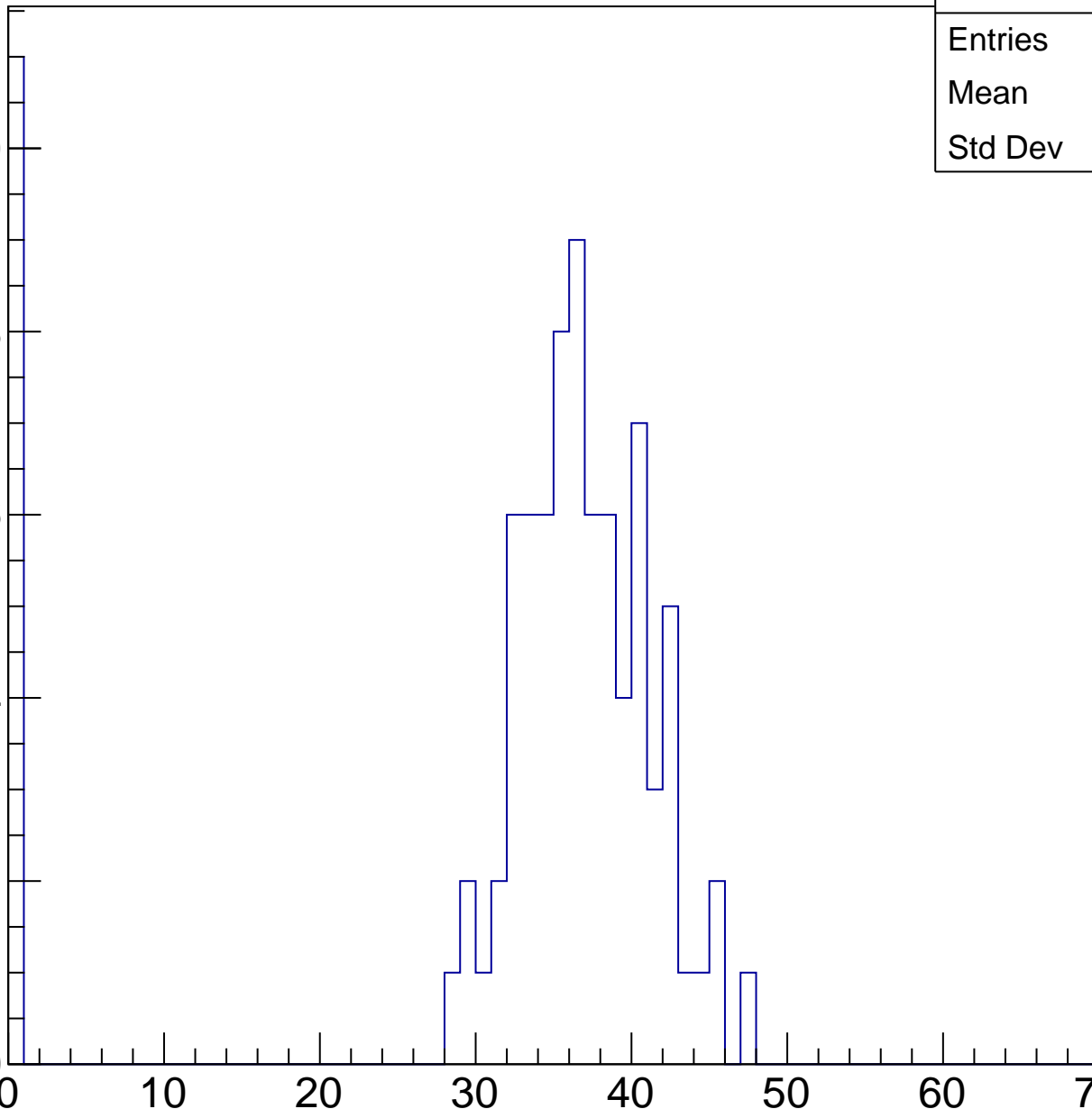
40

50

60

70

ampl

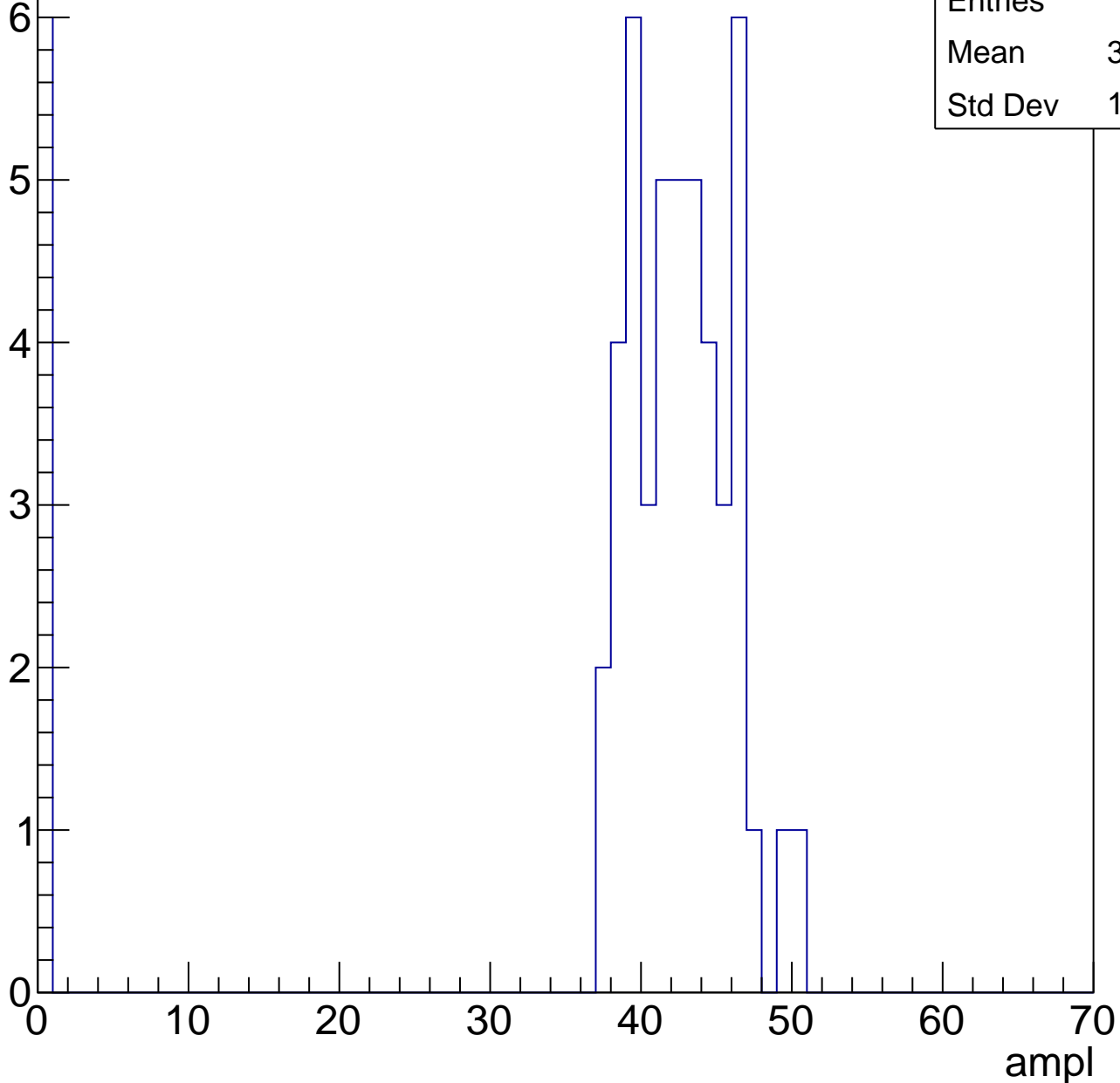


B1L103S, U5-ch21, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	37.37
Std Dev	13.82

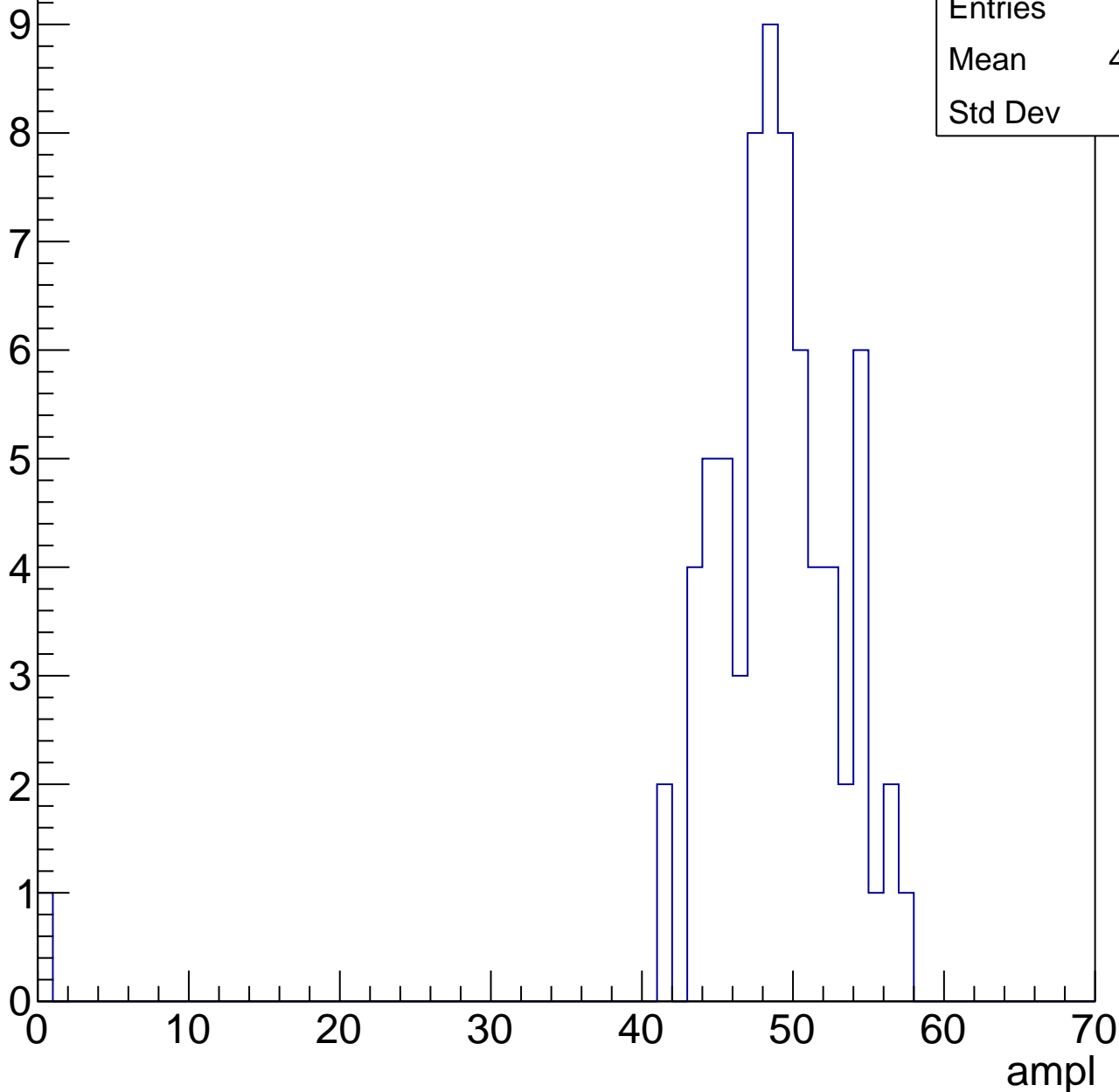


B1L103S, U5-ch21, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

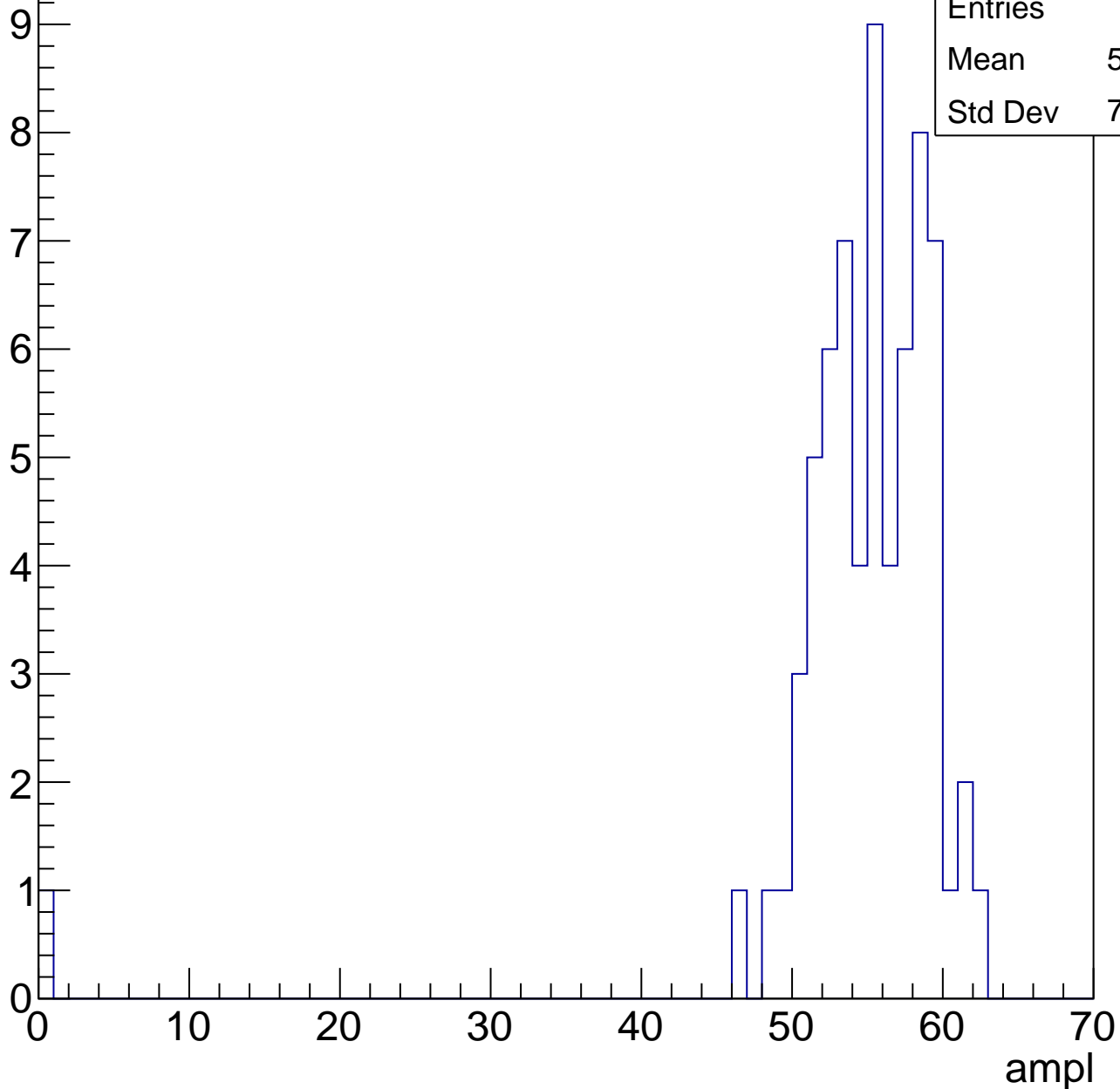
Entries	71
Mean	47.93
Std Dev	6.82



B1L103S, U5-ch21, adc4

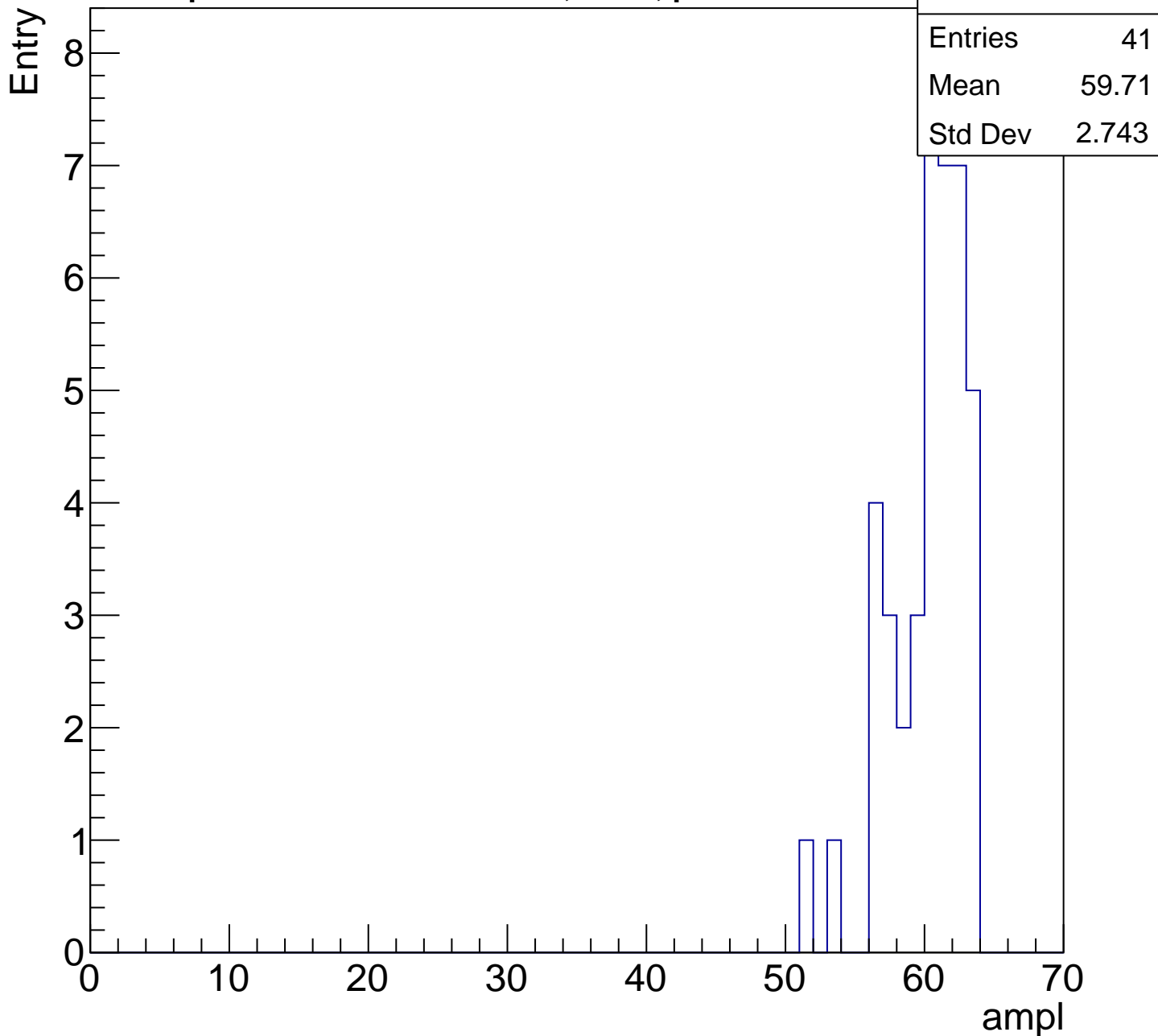
calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch21, adc5

calib_packv5_041523_1651.root, FC#0, port C2

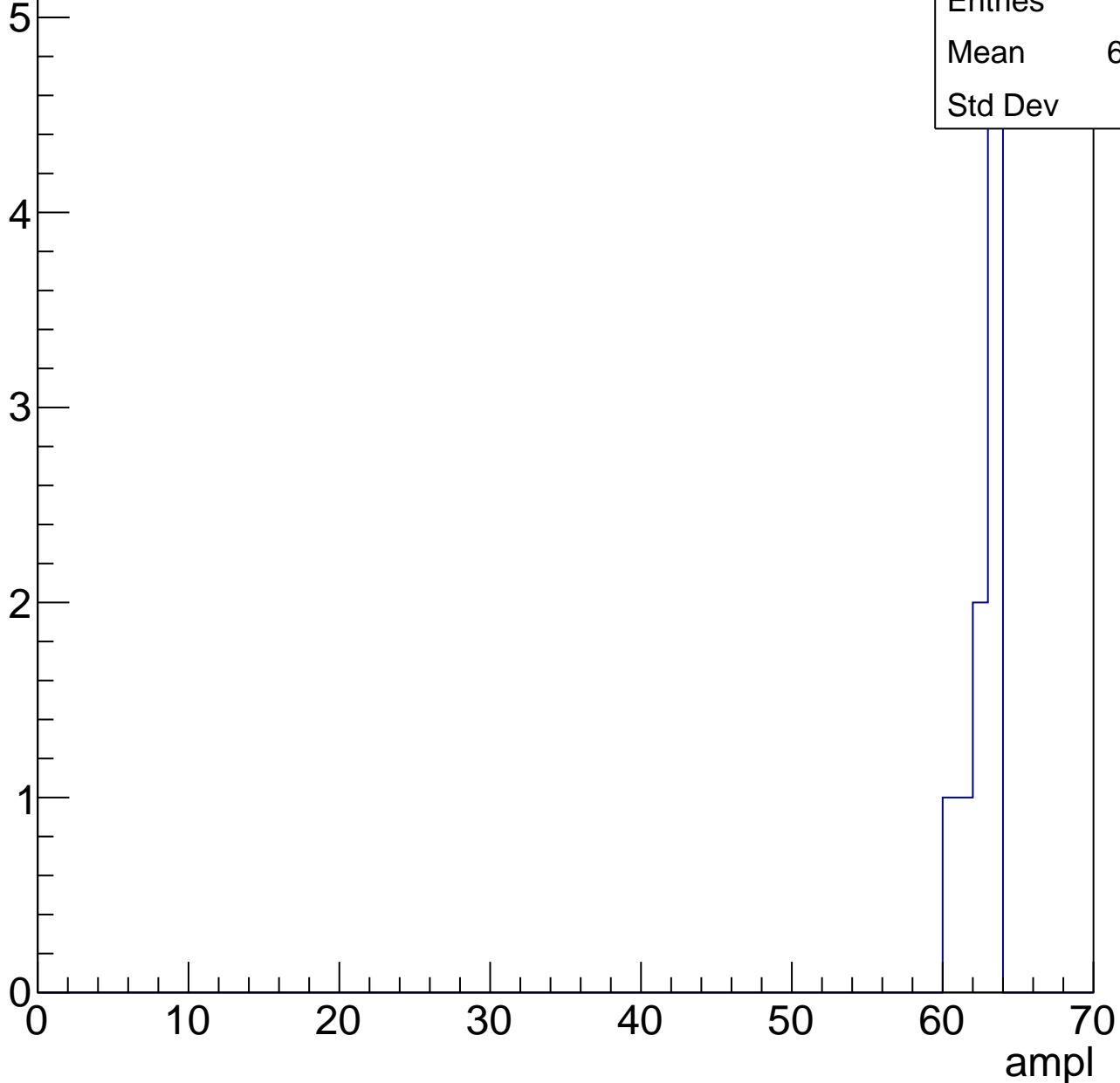


B1L103S, U5-ch21, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	9
Mean	62.22
Std Dev	1.03



B1L103S, U5-ch21, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

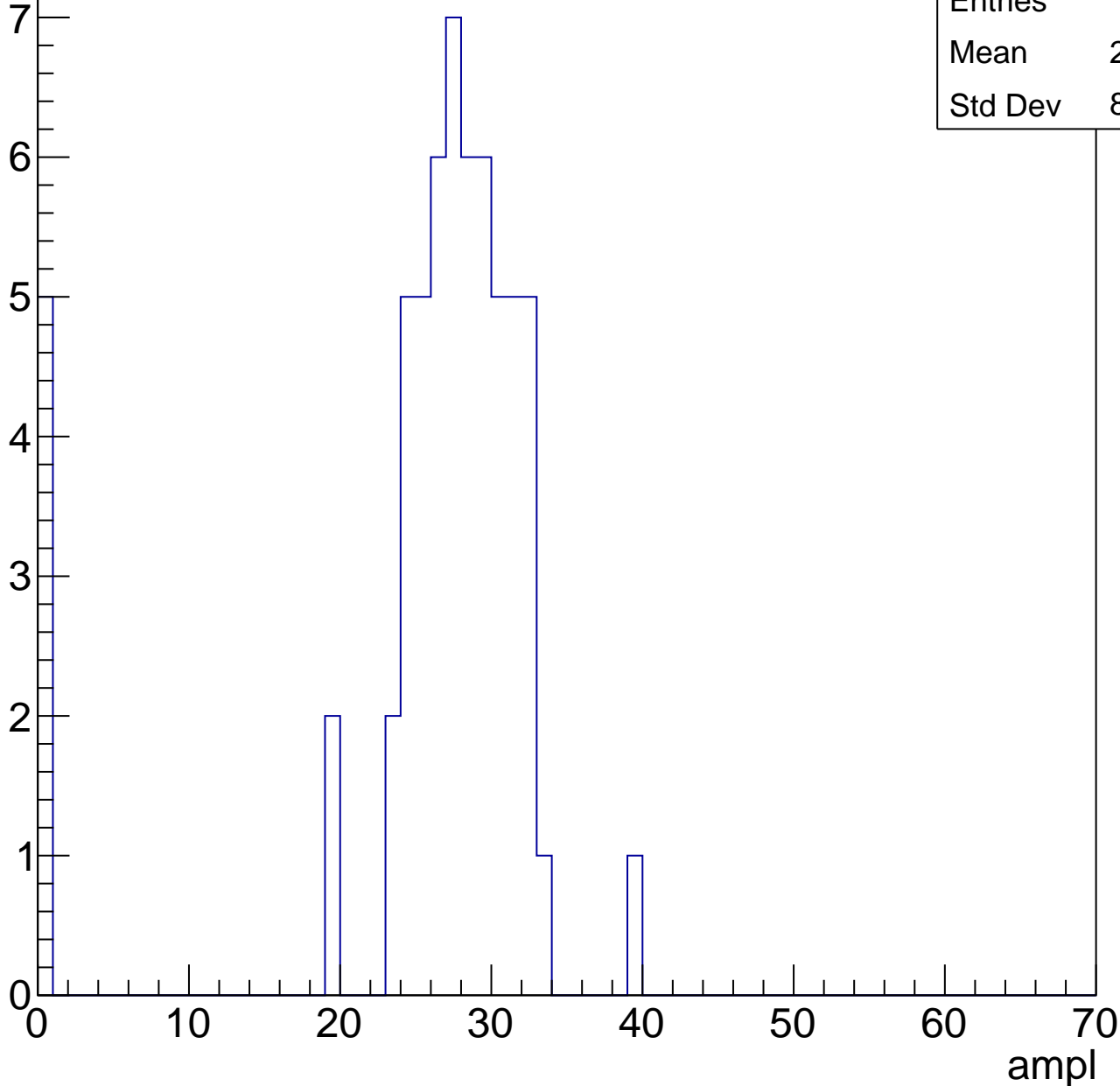
ampl

B1L103S, U5-ch22, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	25.46
Std Dev	8.289

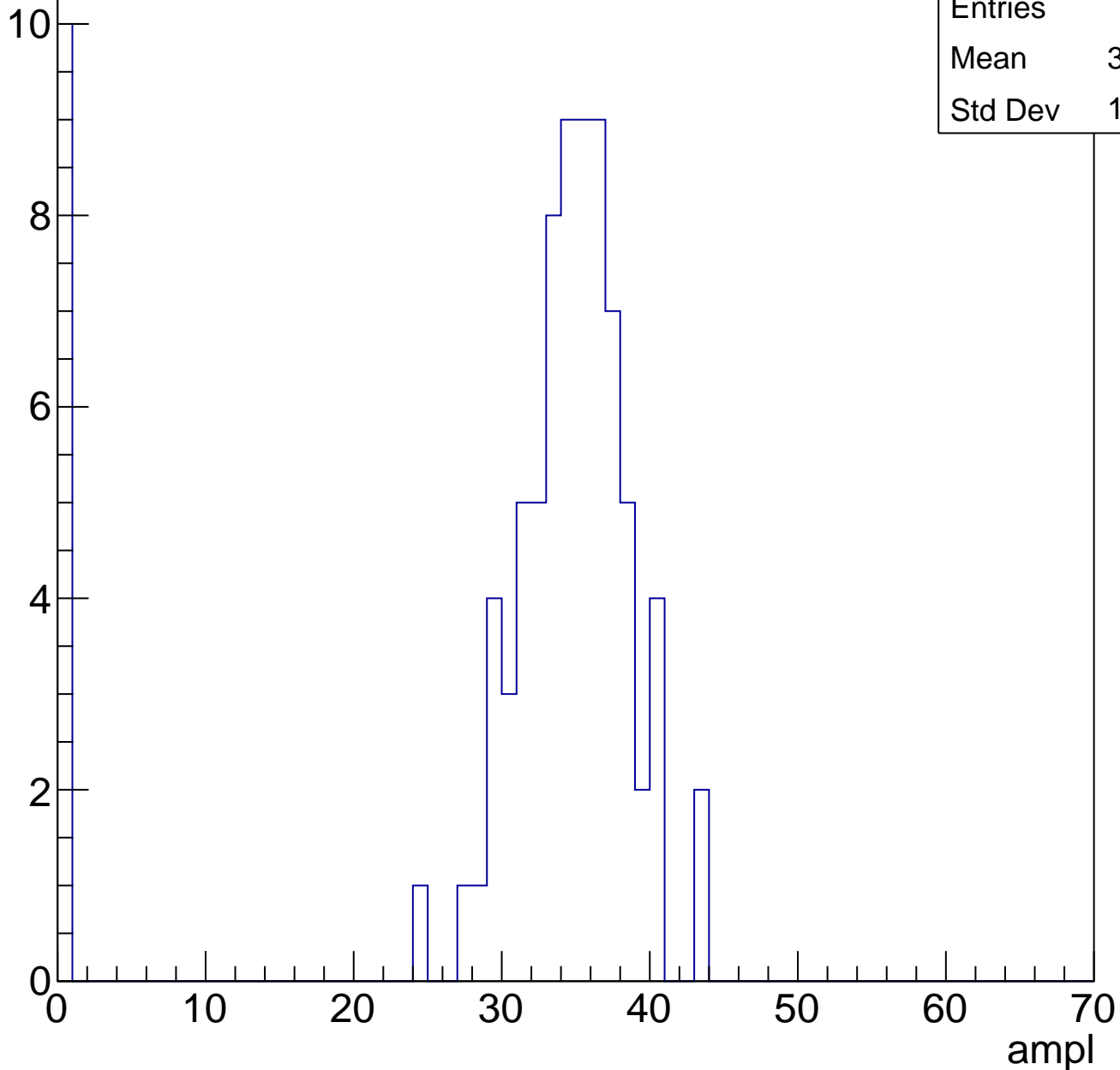


B1L103S, U5-ch22, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	85
Mean	30.38
Std Dev	11.58

Entry

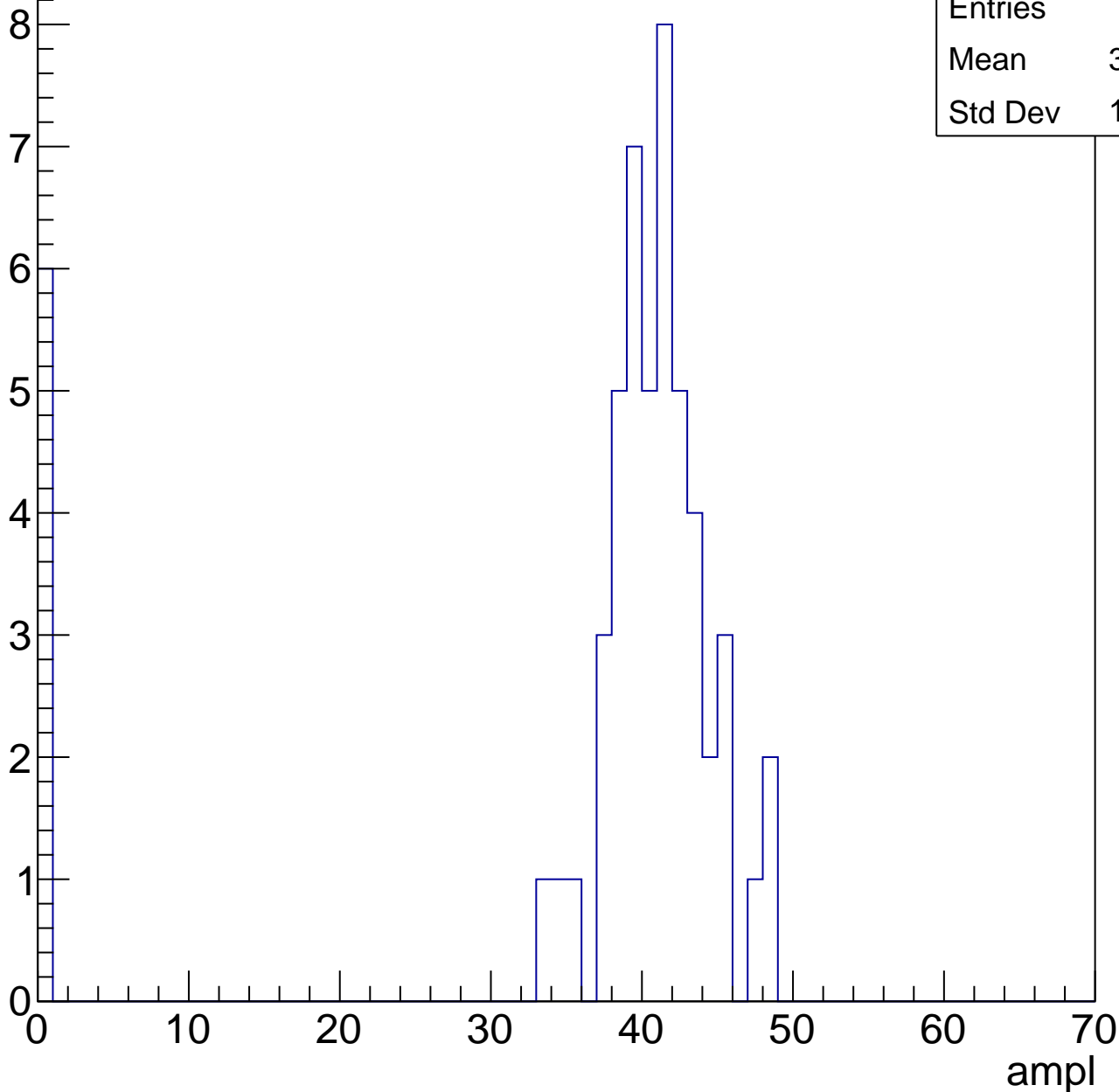


B1L103S, U5-ch22, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	36.15
Std Dev	13.13



B1L103S, U5-ch22, adc3

calib_packv5_041523_1651.root, FC#0, port C2

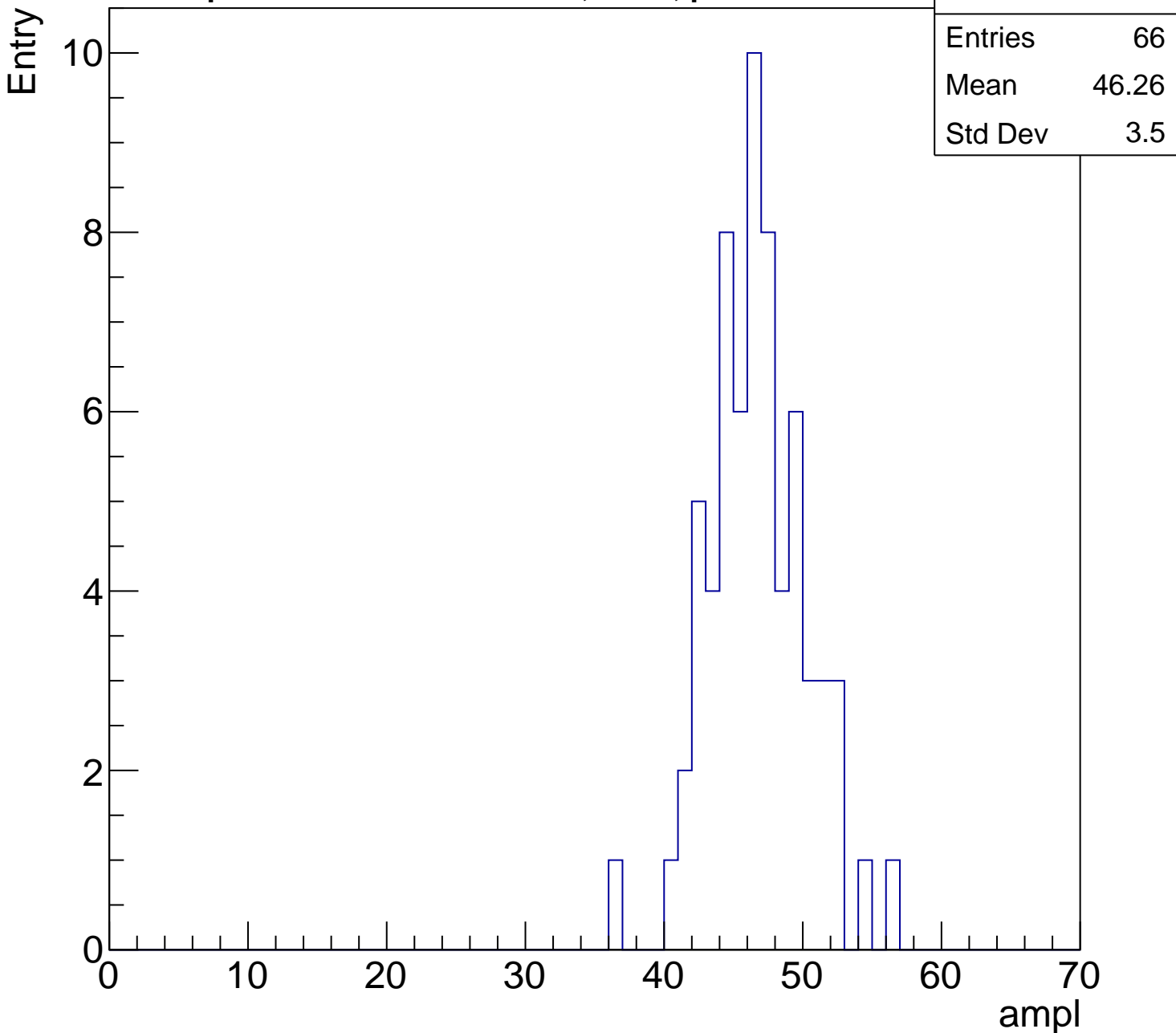
Entries	66
Mean	46.26
Std Dev	3.5

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

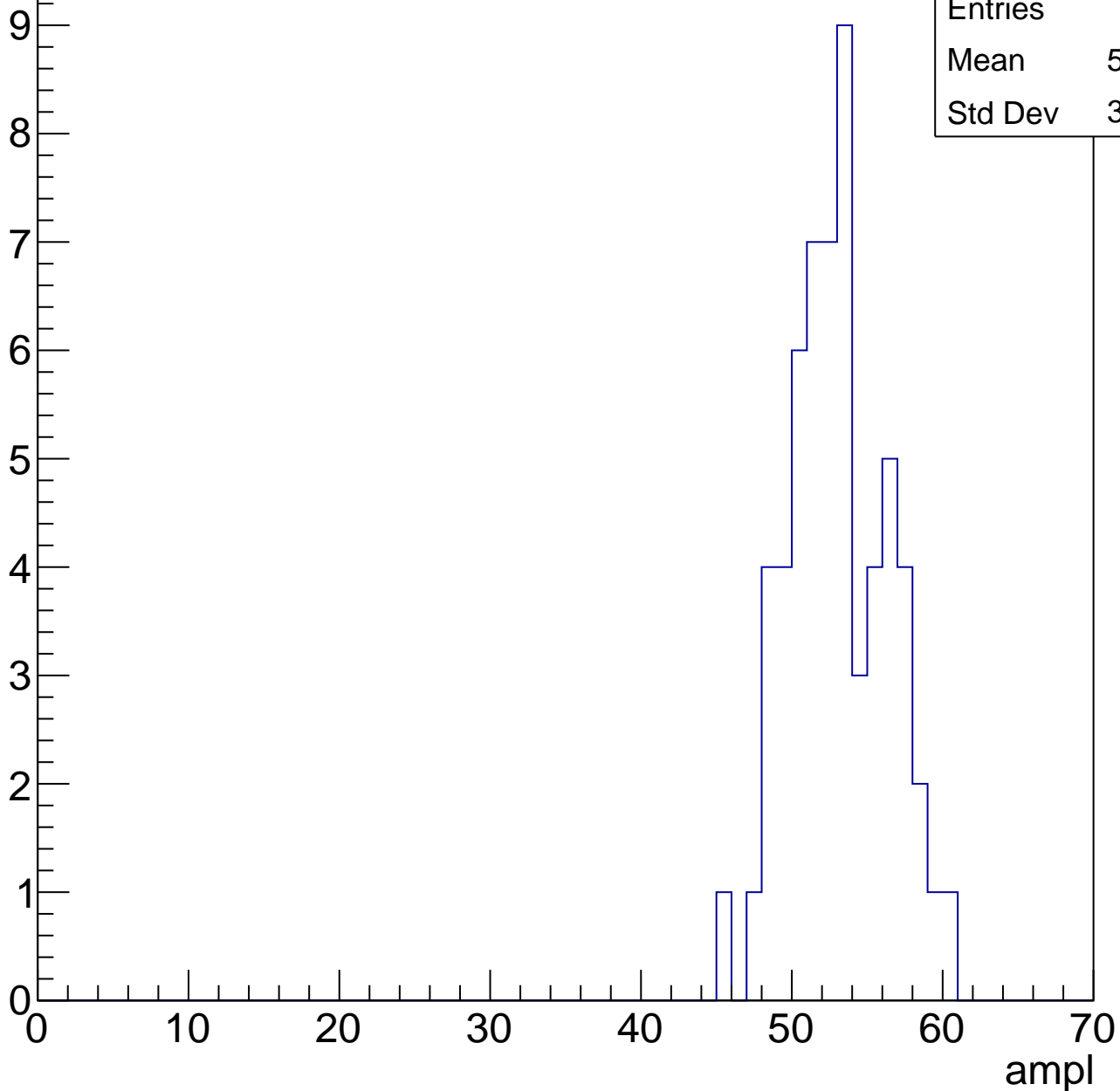


B1L103S, U5-ch22, adc4

calib_packv5_041523_1651.root, FC#0, port C2

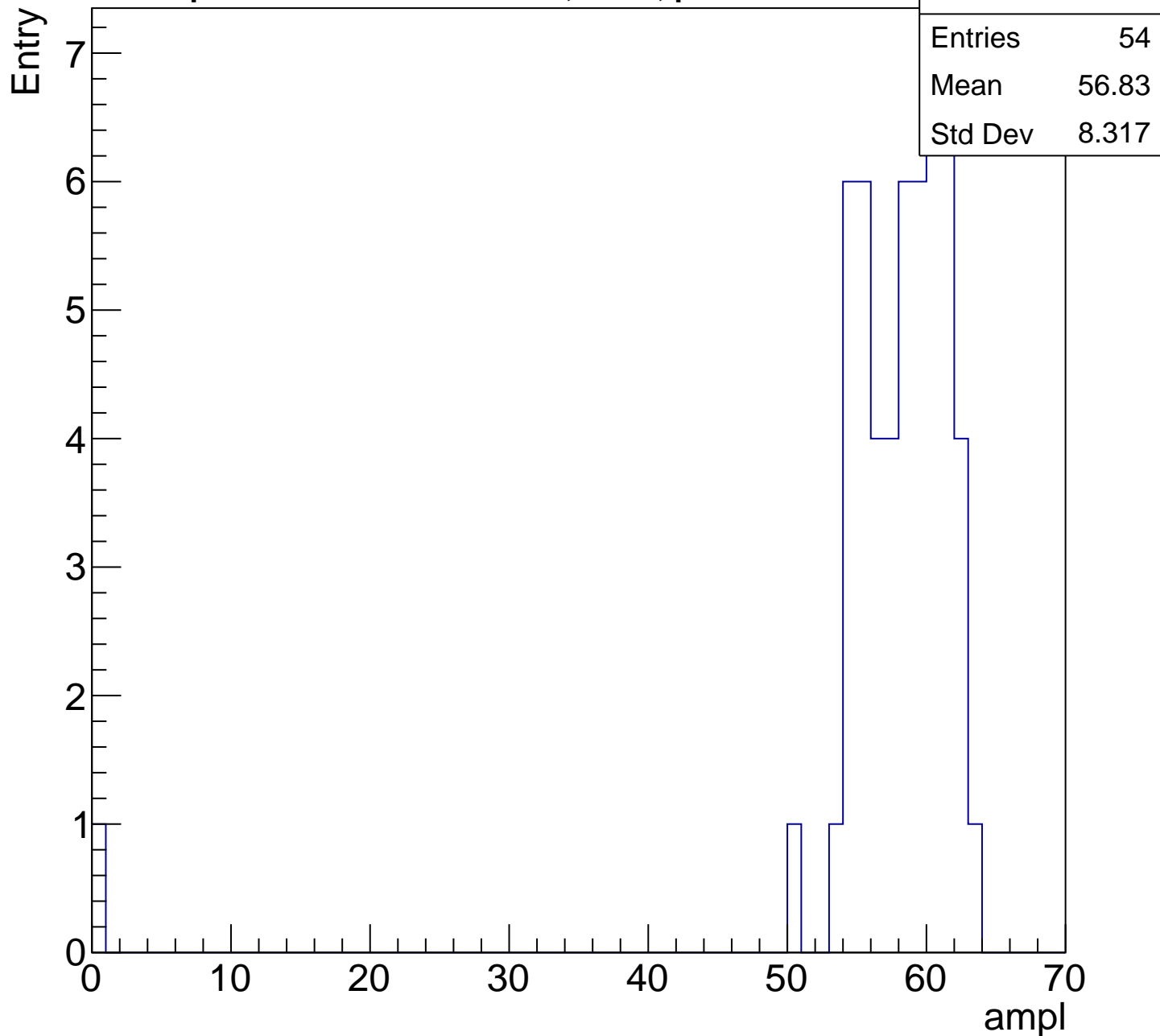
Entry

Entries	59
Mean	52.59
Std Dev	3.205



B1L103S, U5-ch22, adc5

calib_packv5_041523_1651.root, FC#0, port C2

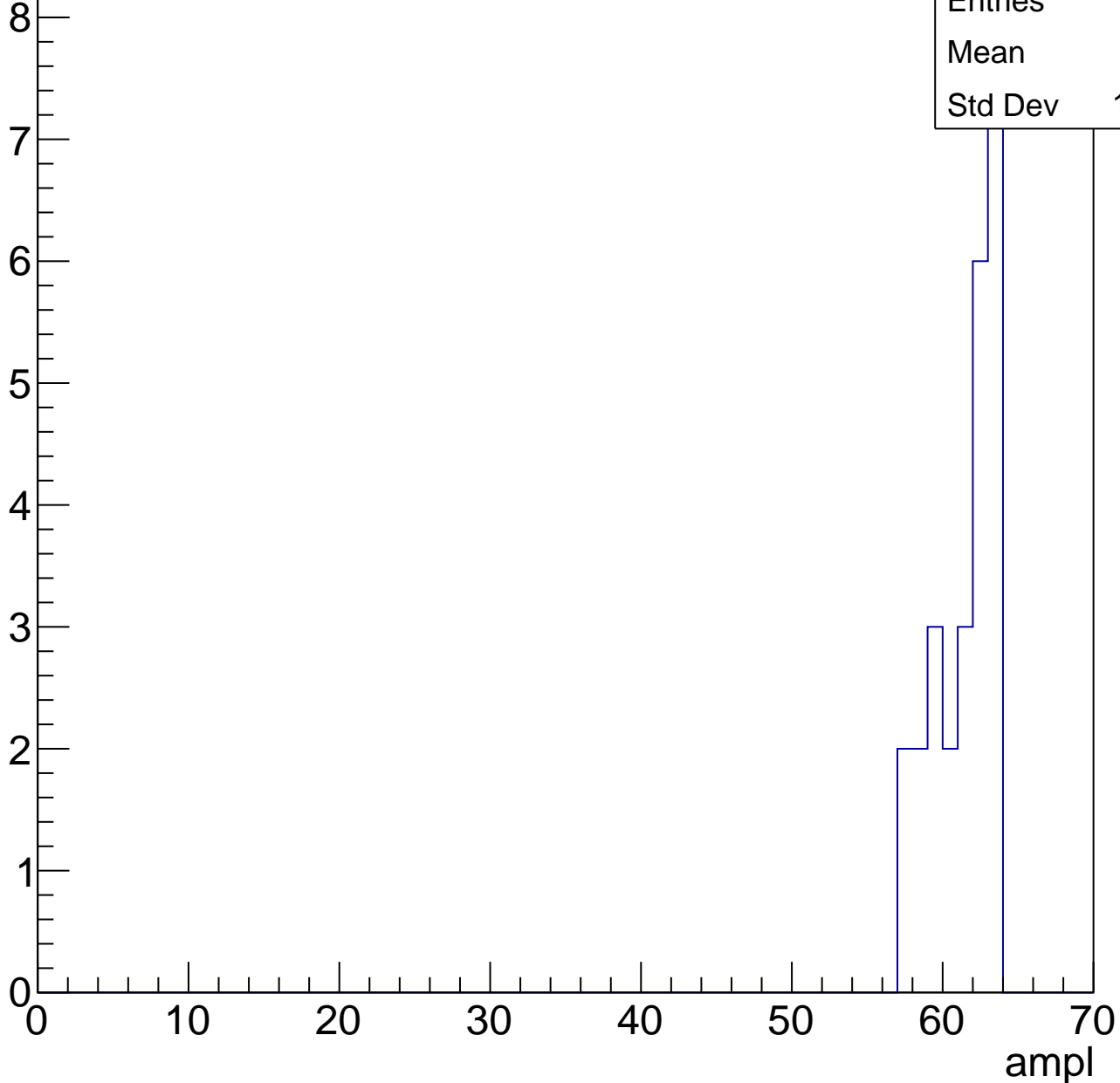


B1L103S, U5-ch22, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	26
Mean	61
Std Dev	1.981



B1L103S, U5-ch22, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry



B1L103S, U5-ch23, adc0

calib_packv5_041523_1651.root, FC#0, port C2

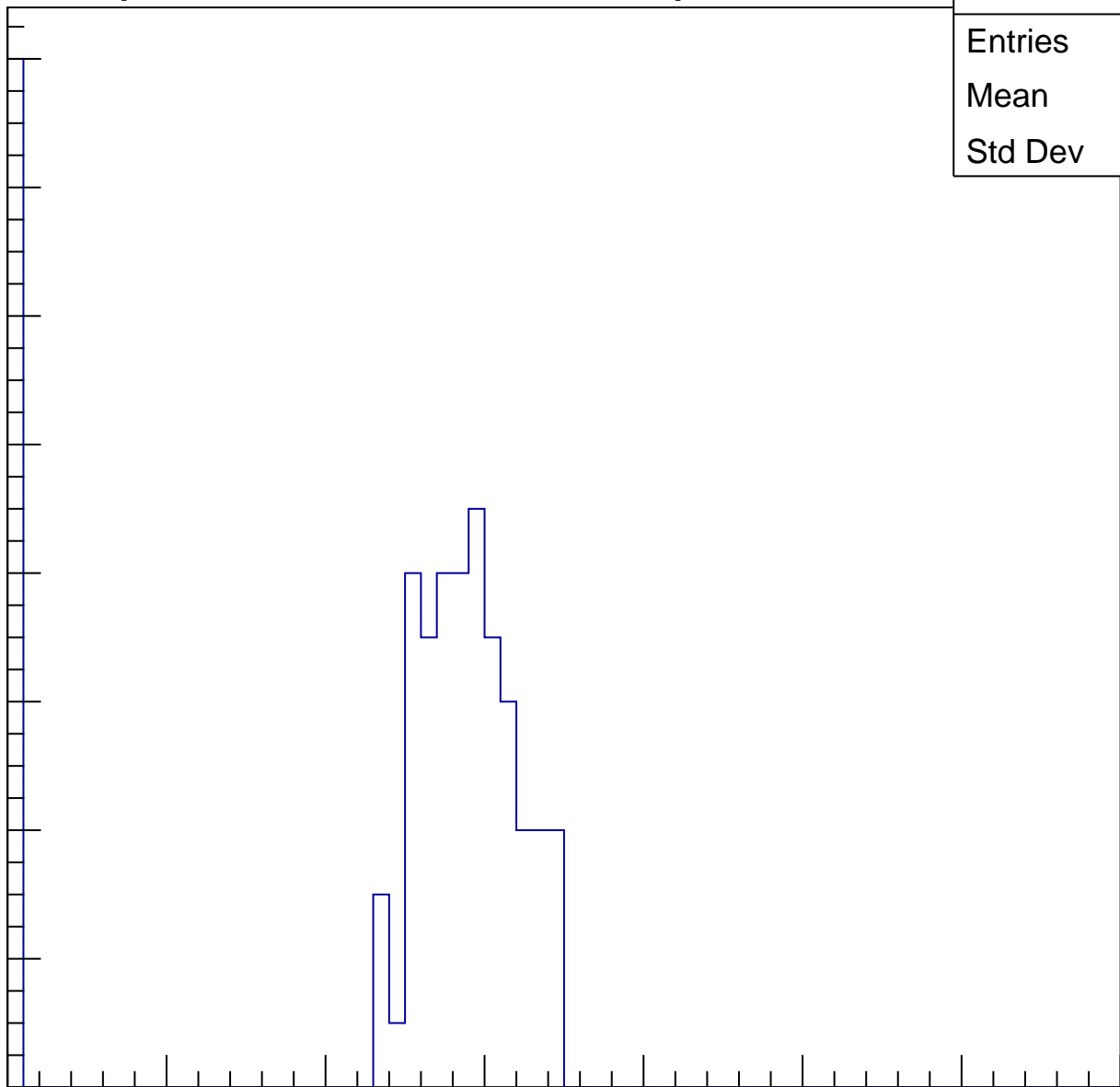
Entries	85
Mean	23.15
Std Dev	11.45

Entry

16
14
12
10
8
6
4
2
0

ampl

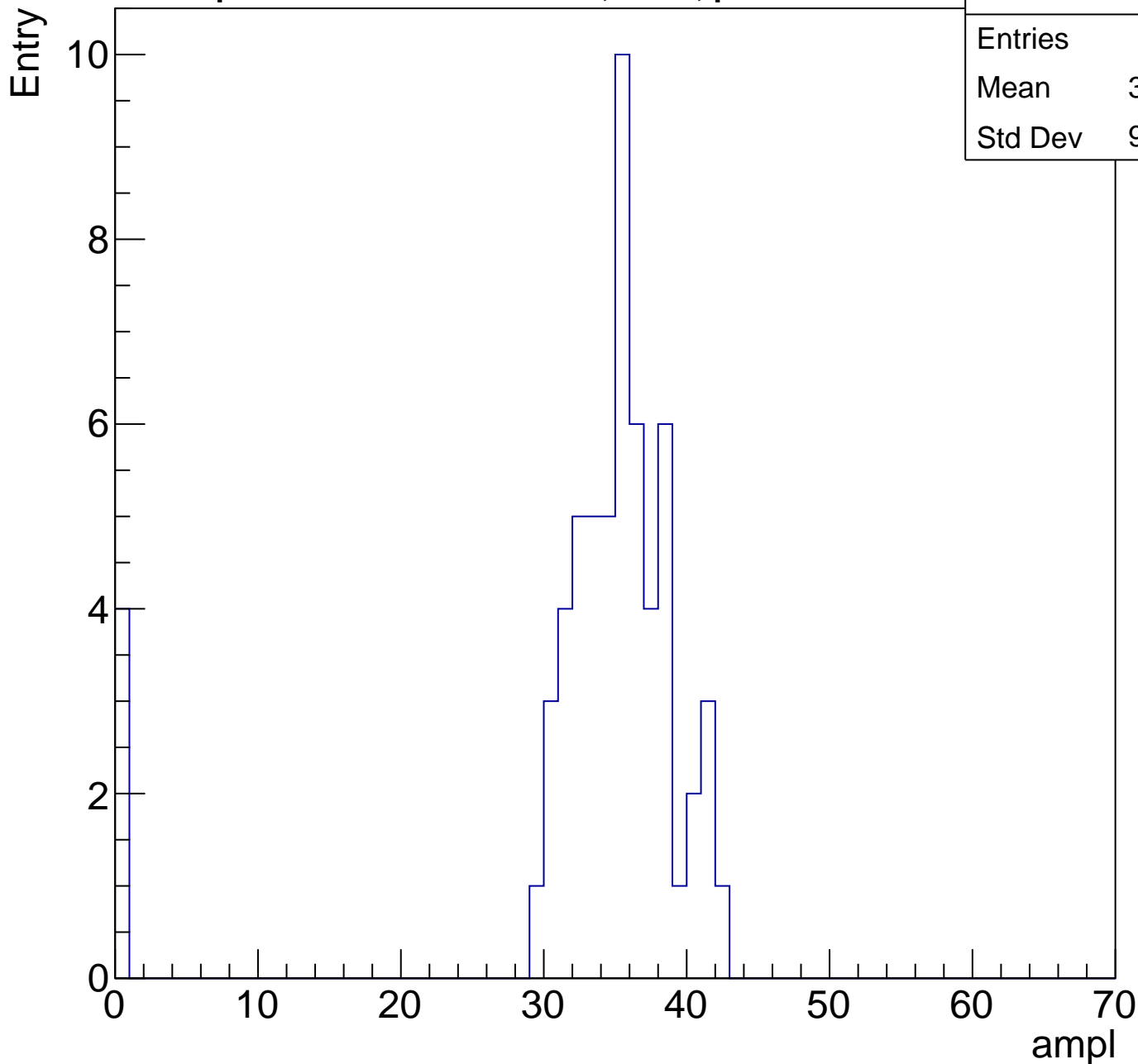
0 10 20 30 40 50 60 70



B1L103S, U5-ch23, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	60
Mean	32.73
Std Dev	9.252



B1L103S, U5-ch23, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	76
Mean	34.87
Std Dev	14.67

Entry

10

8

6

4

2

0

0

10

20

30

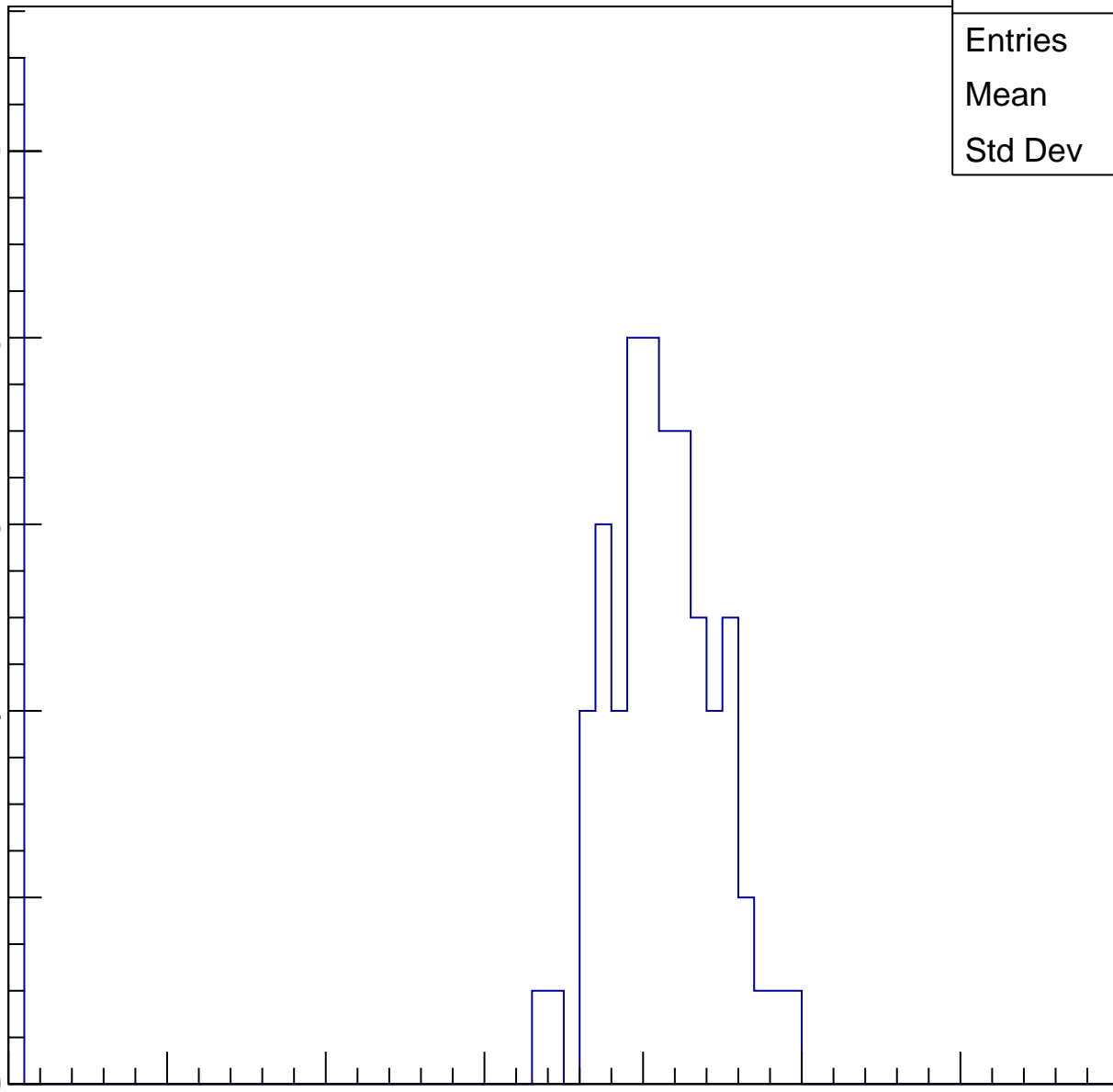
40

50

60

70

ampl

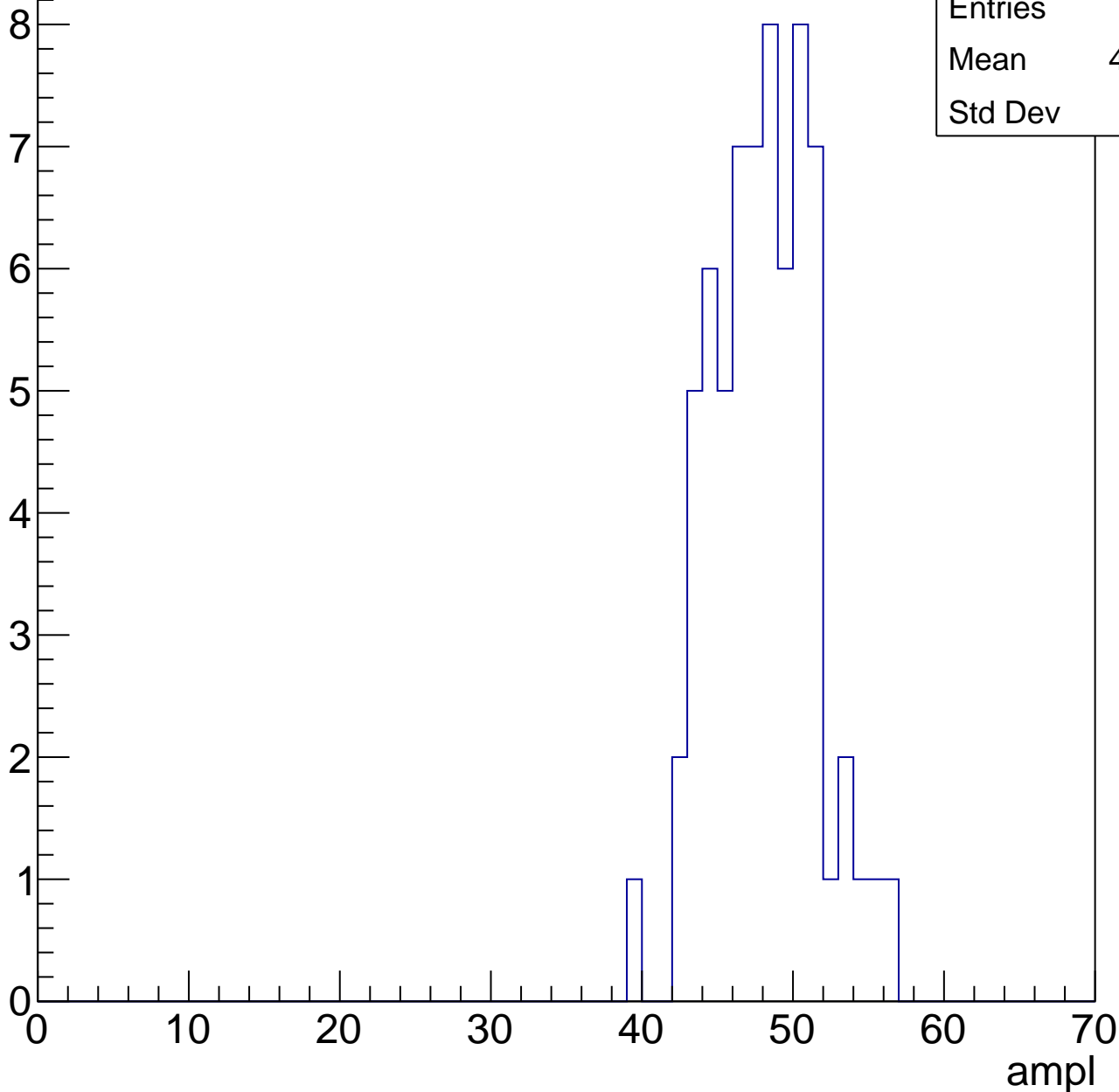


B1L103S, U5-ch23, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	47.59
Std Dev	3.34

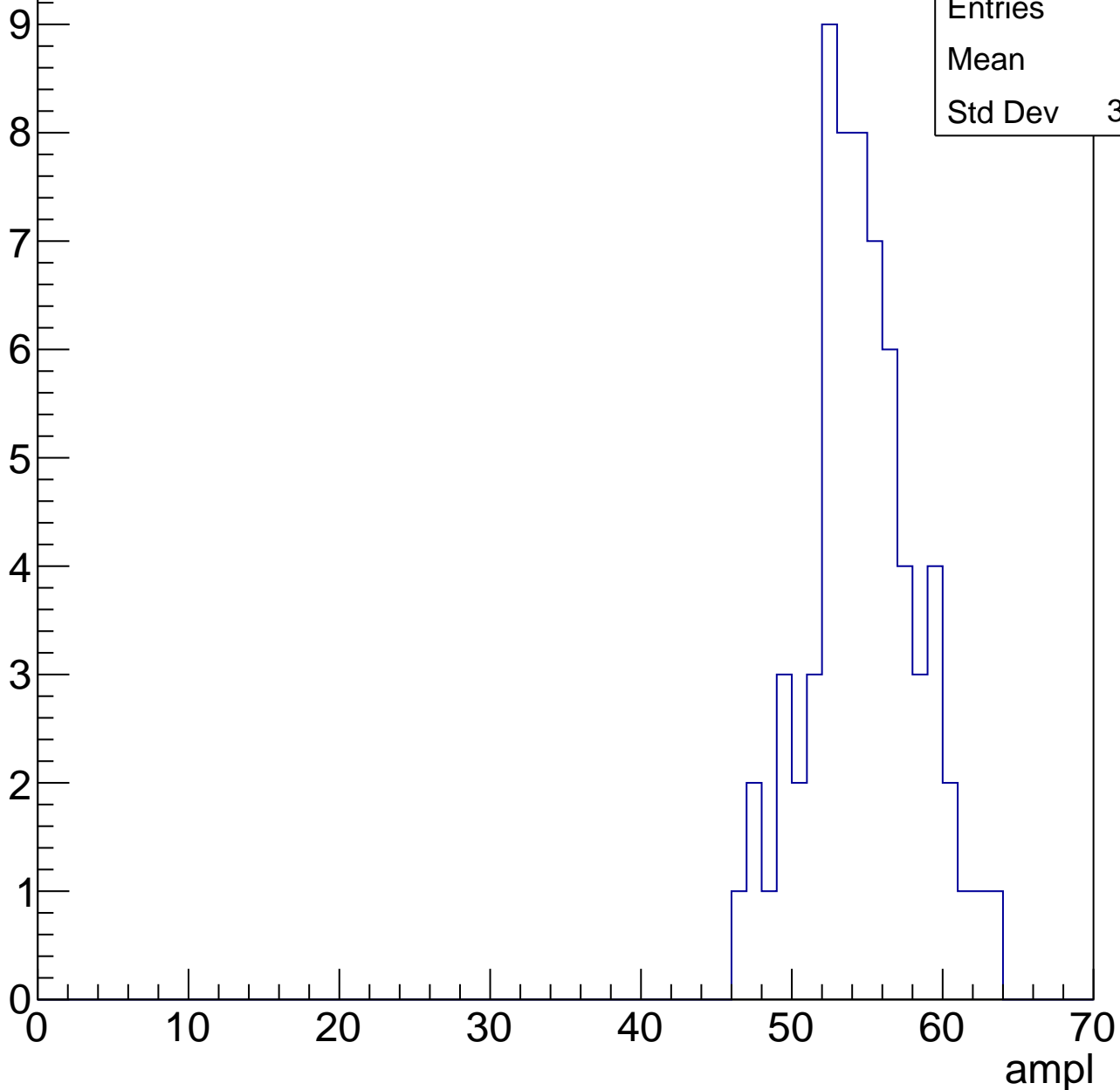


B1L103S, U5-ch23, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	54.2
Std Dev	3.598

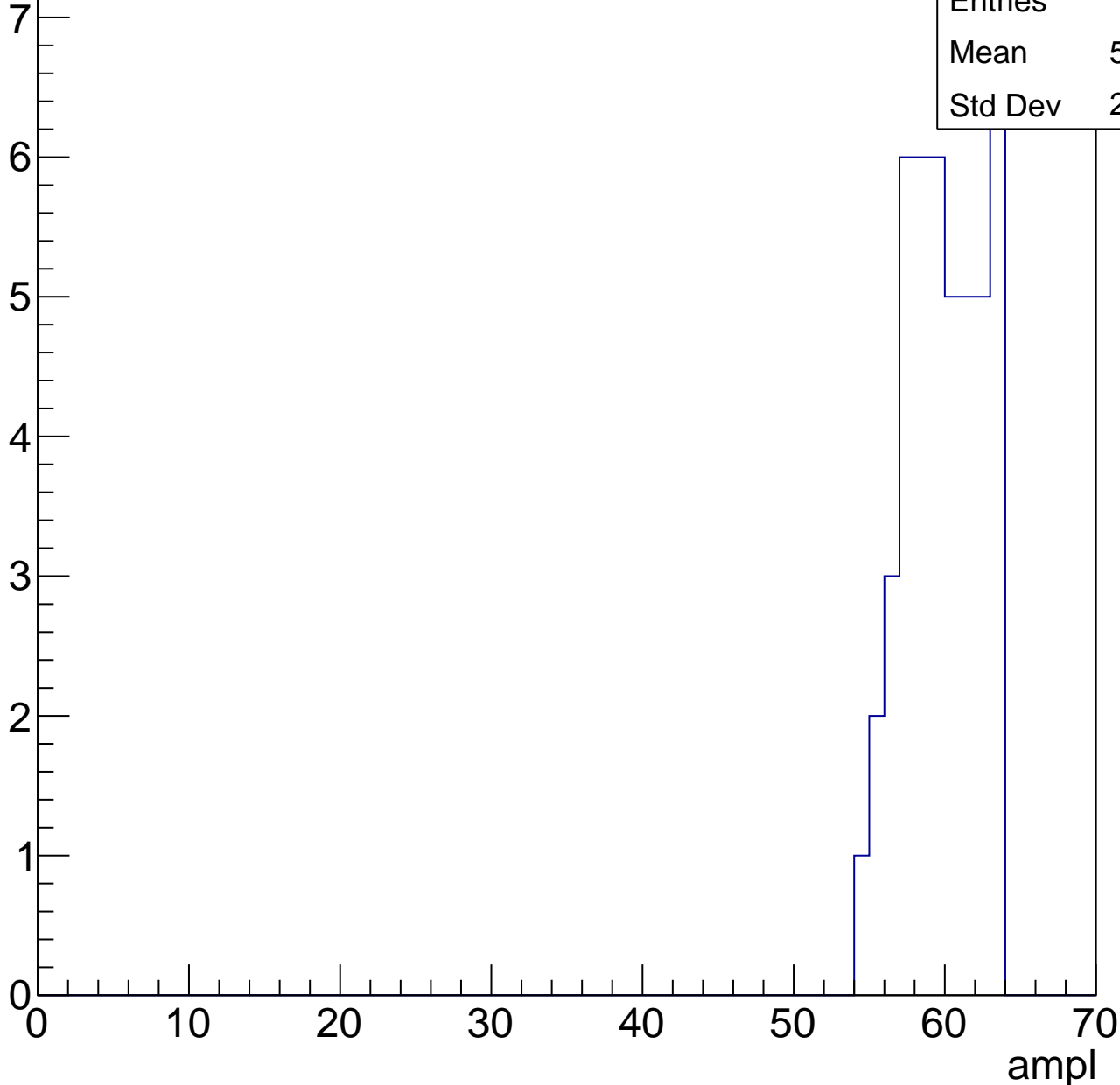


B1L103S, U5-ch23, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

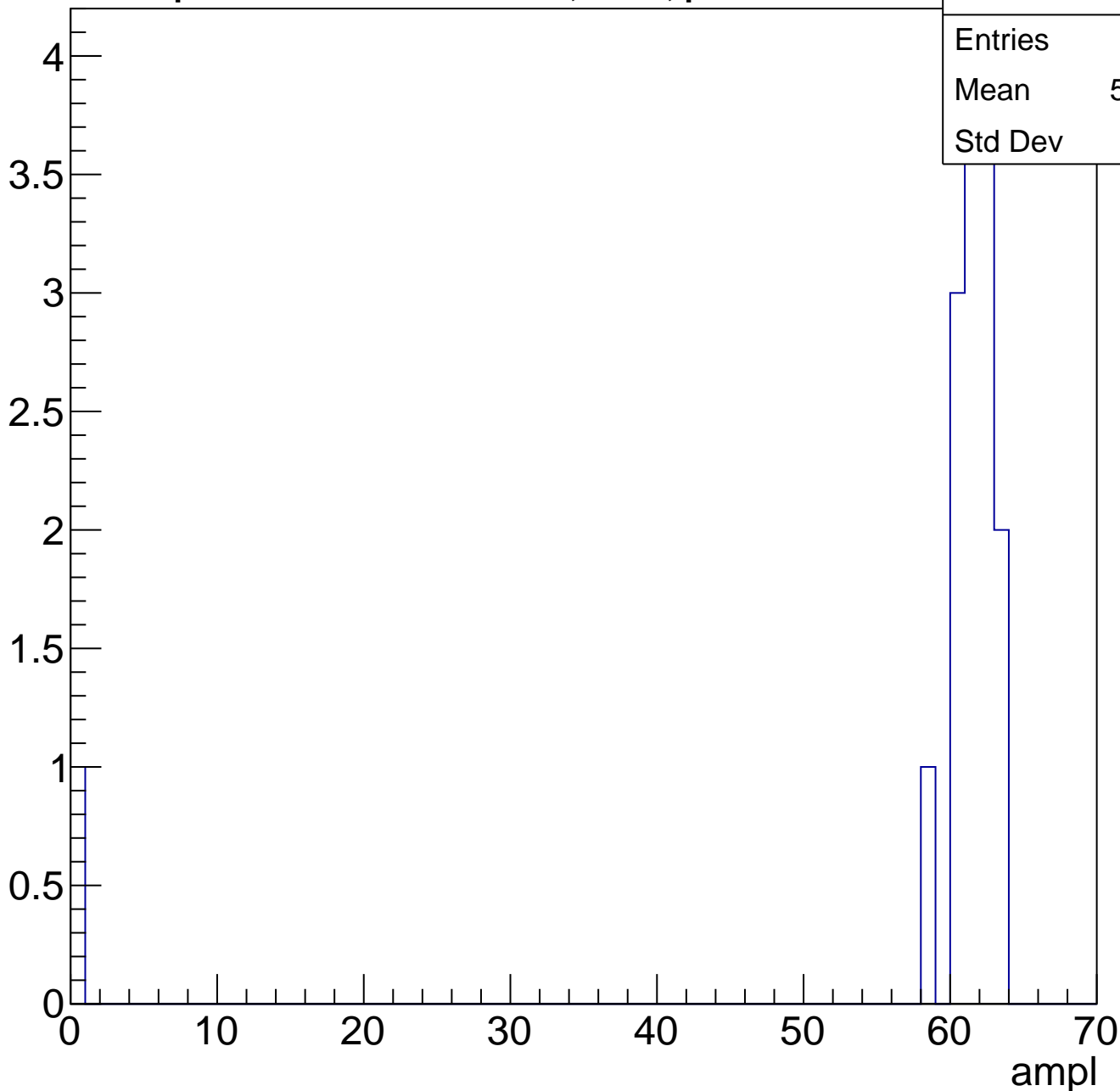
Entries	46
Mean	59.39
Std Dev	2.506



B1L103S, U5-ch23, adc6

calib_packv5_041523_1651.root, FC#0, port C2

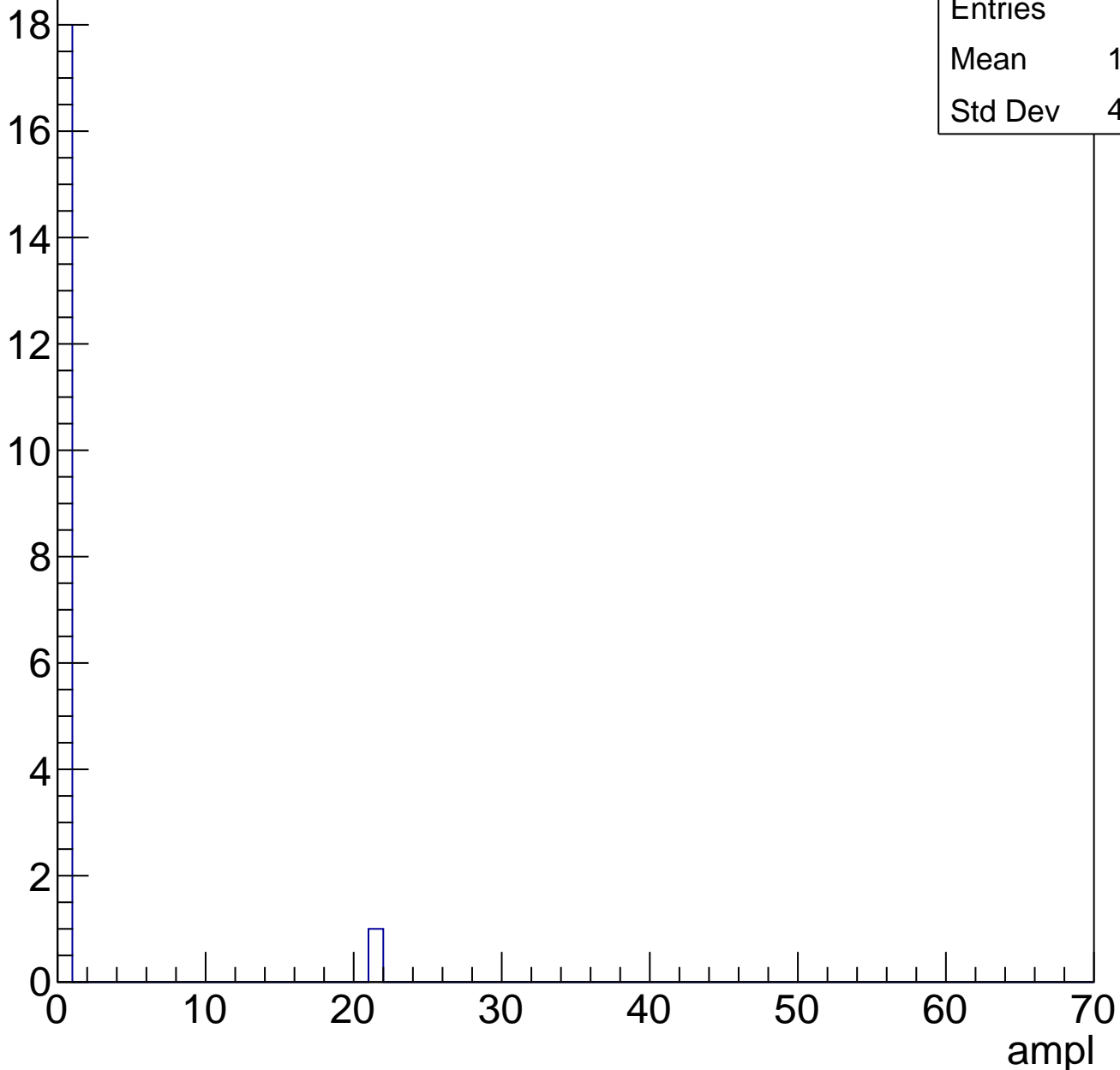
Entry



B1L103S, U5-ch23, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

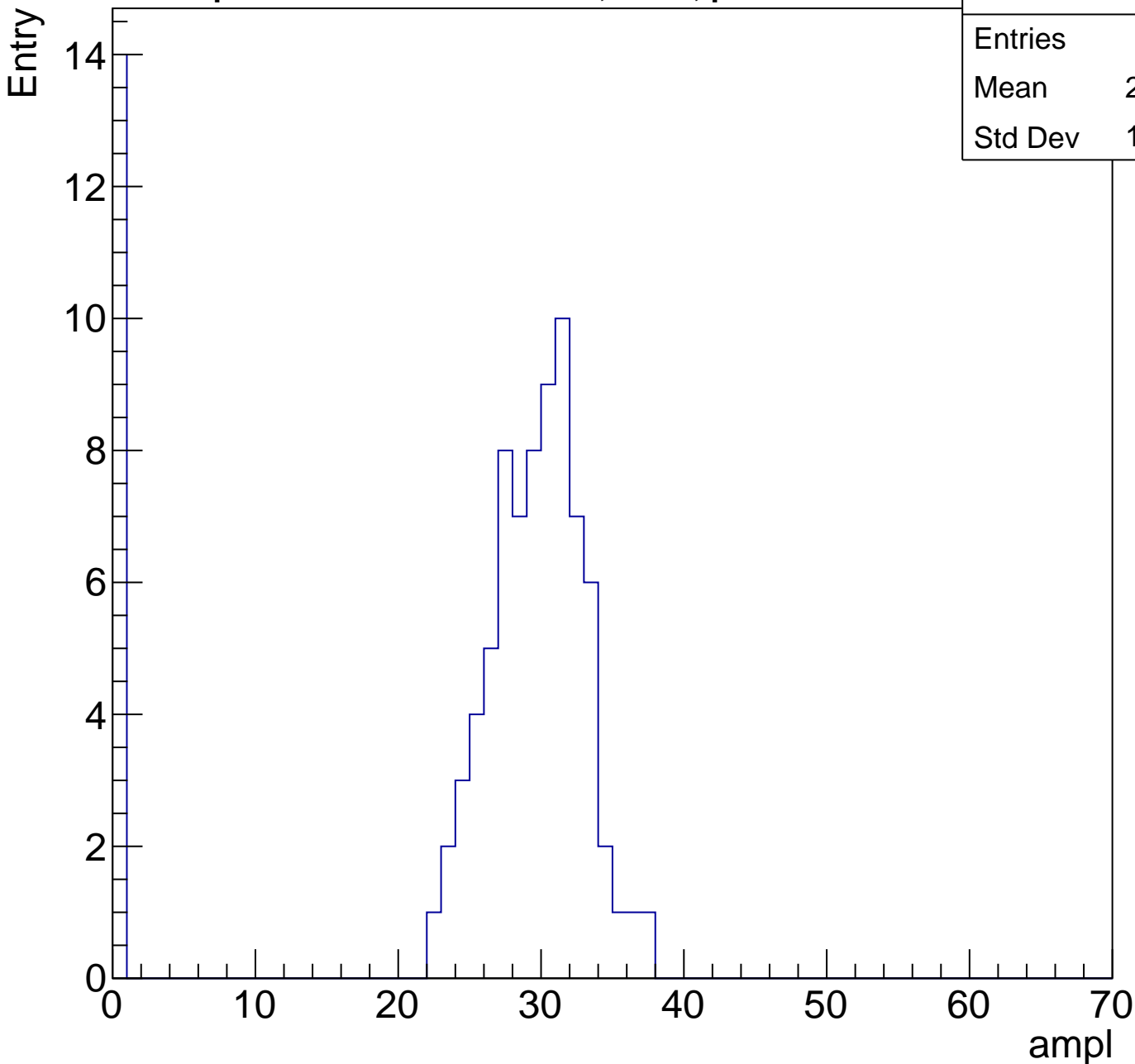


Entries	19
Mean	1.105
Std Dev	4.689

B1L103S, U5-ch24, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	24.63
Std Dev	11.03

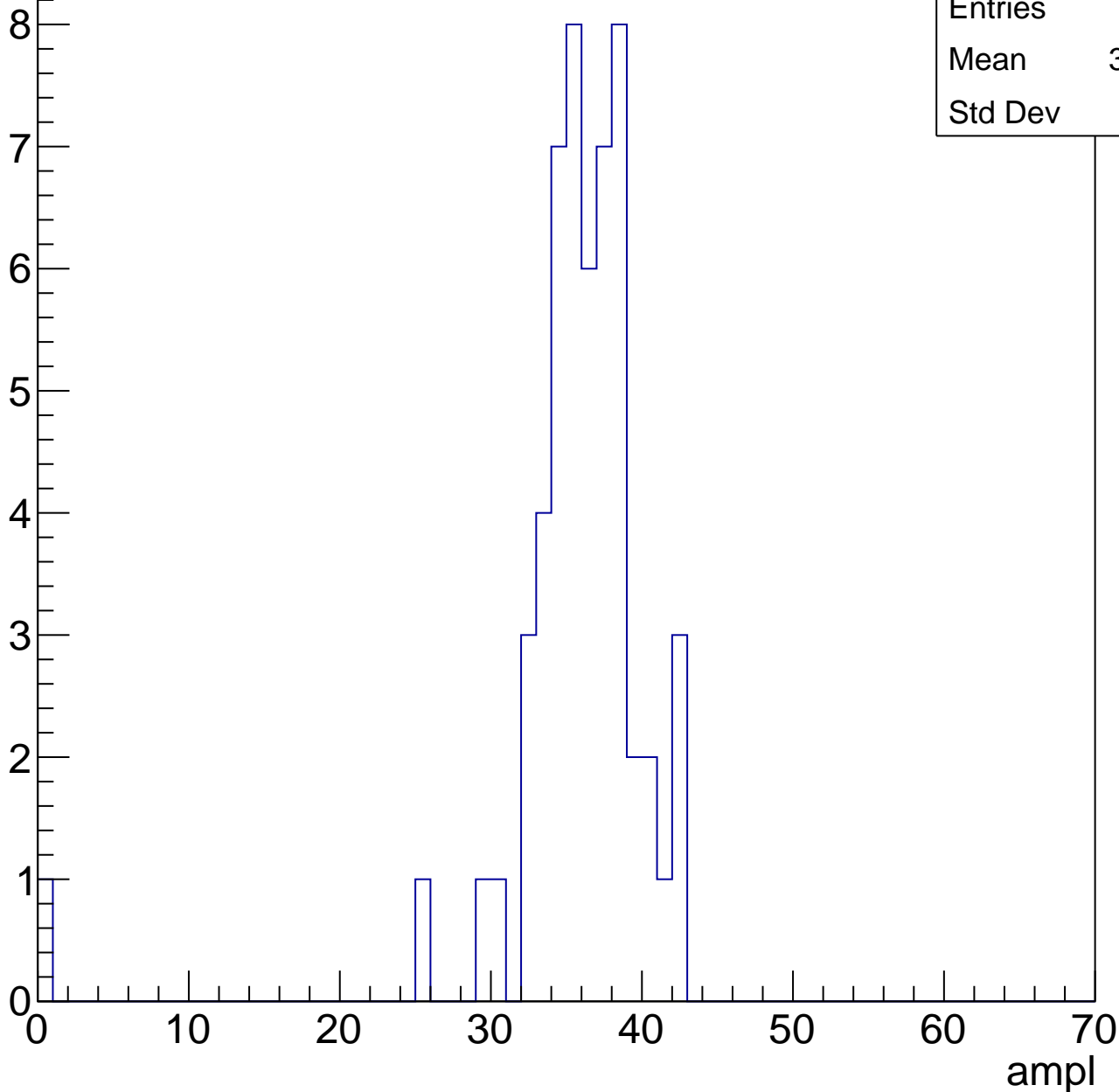


B1L103S, U5-ch24, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	35.16
Std Dev	5.73

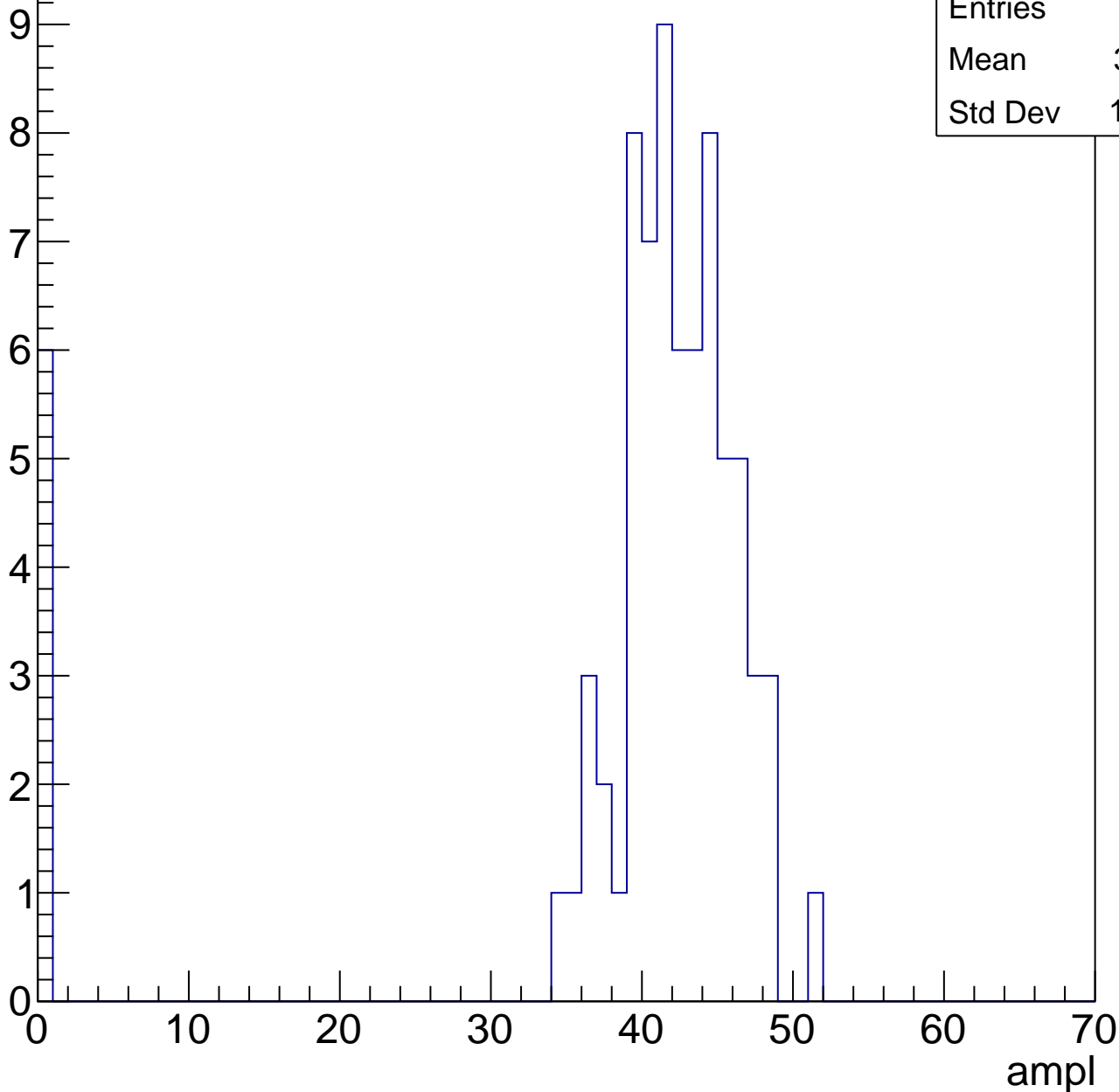


B1L103S, U5-ch24, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	38.71
Std Dev	11.88

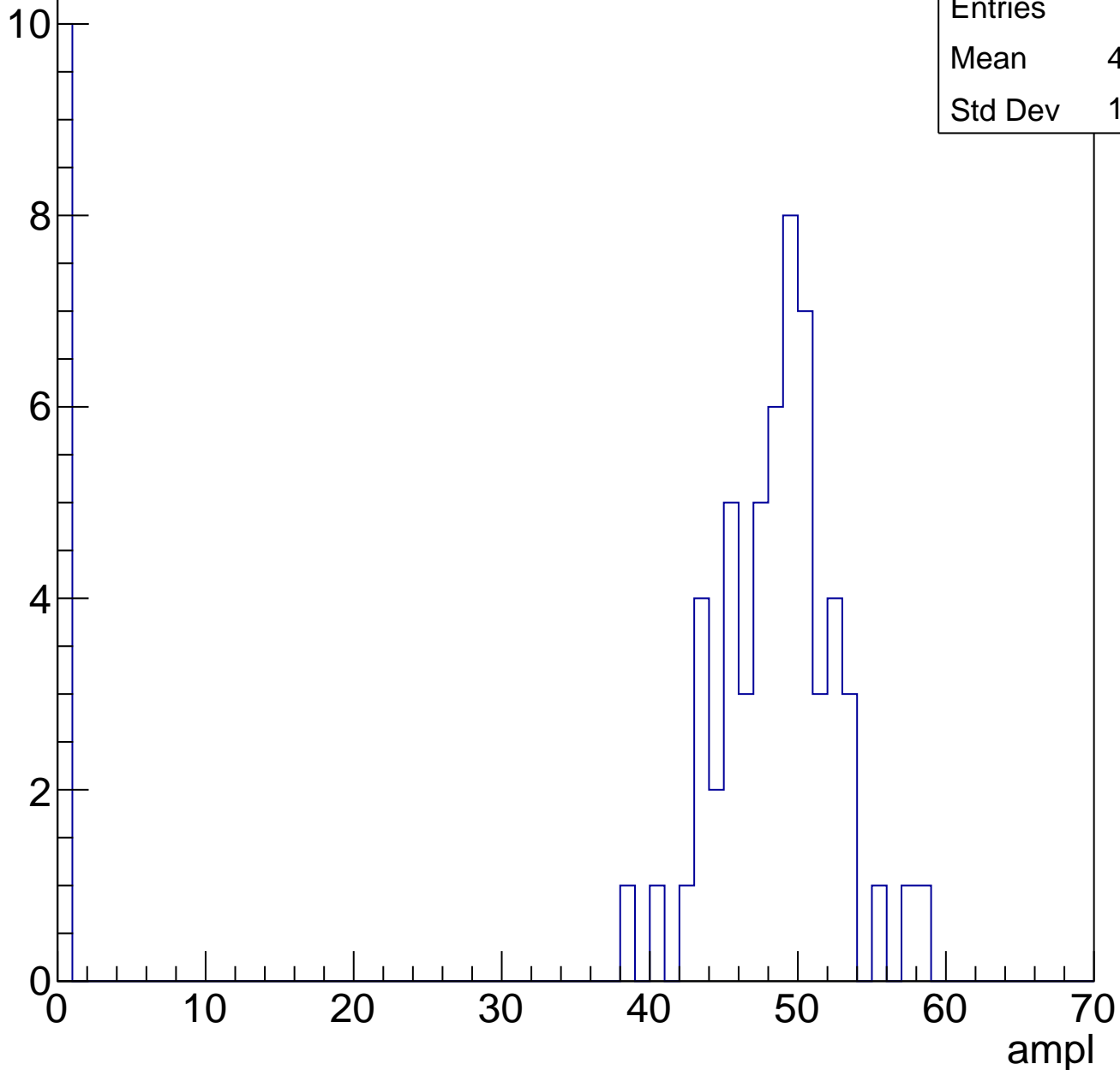


B1L103S, U5-ch24, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	66
Mean	40.88
Std Dev	17.63

Entry

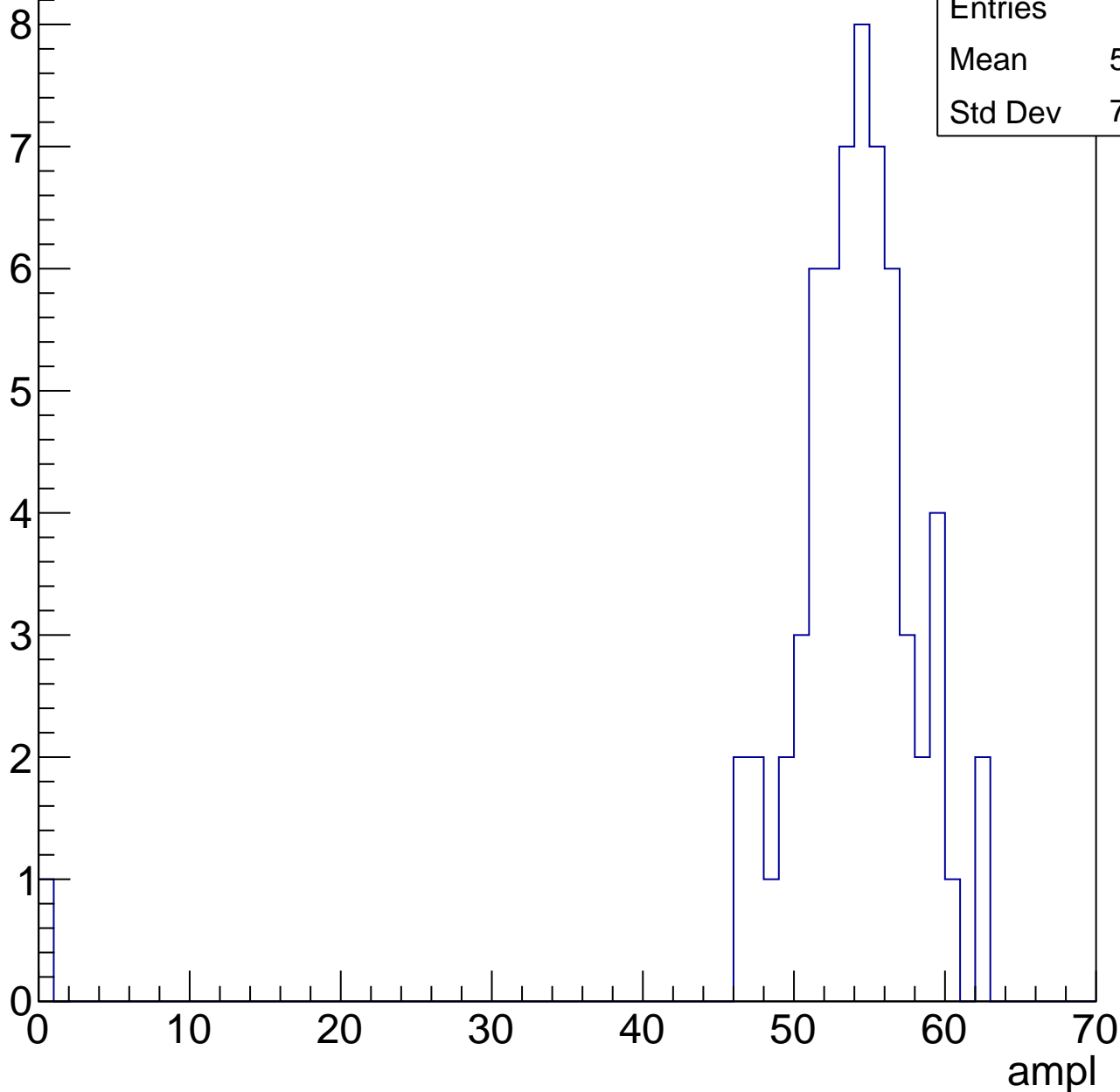


B1L103S, U5-ch24, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	52.87
Std Dev	7.596

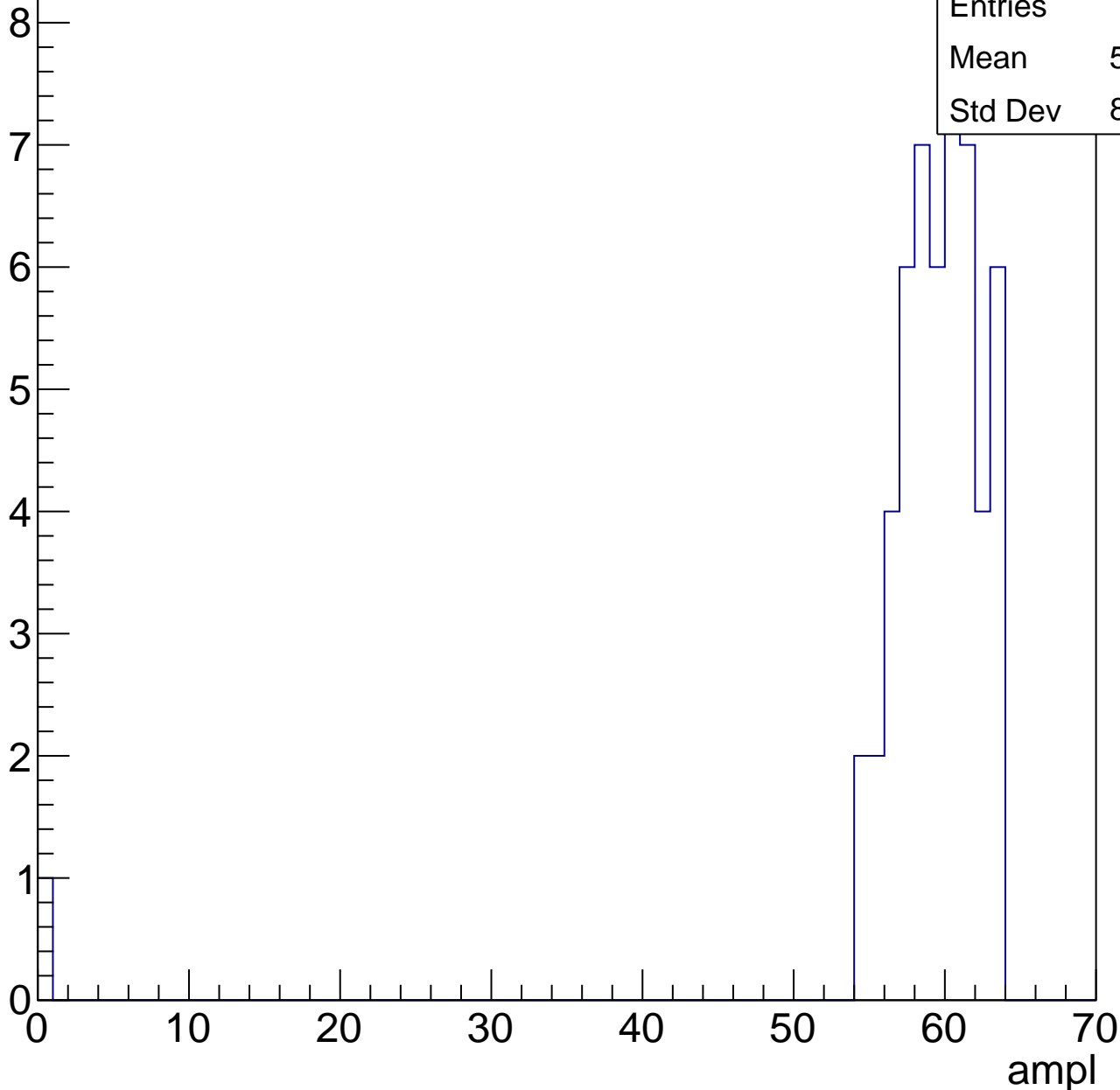


B1L103S, U5-ch24, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

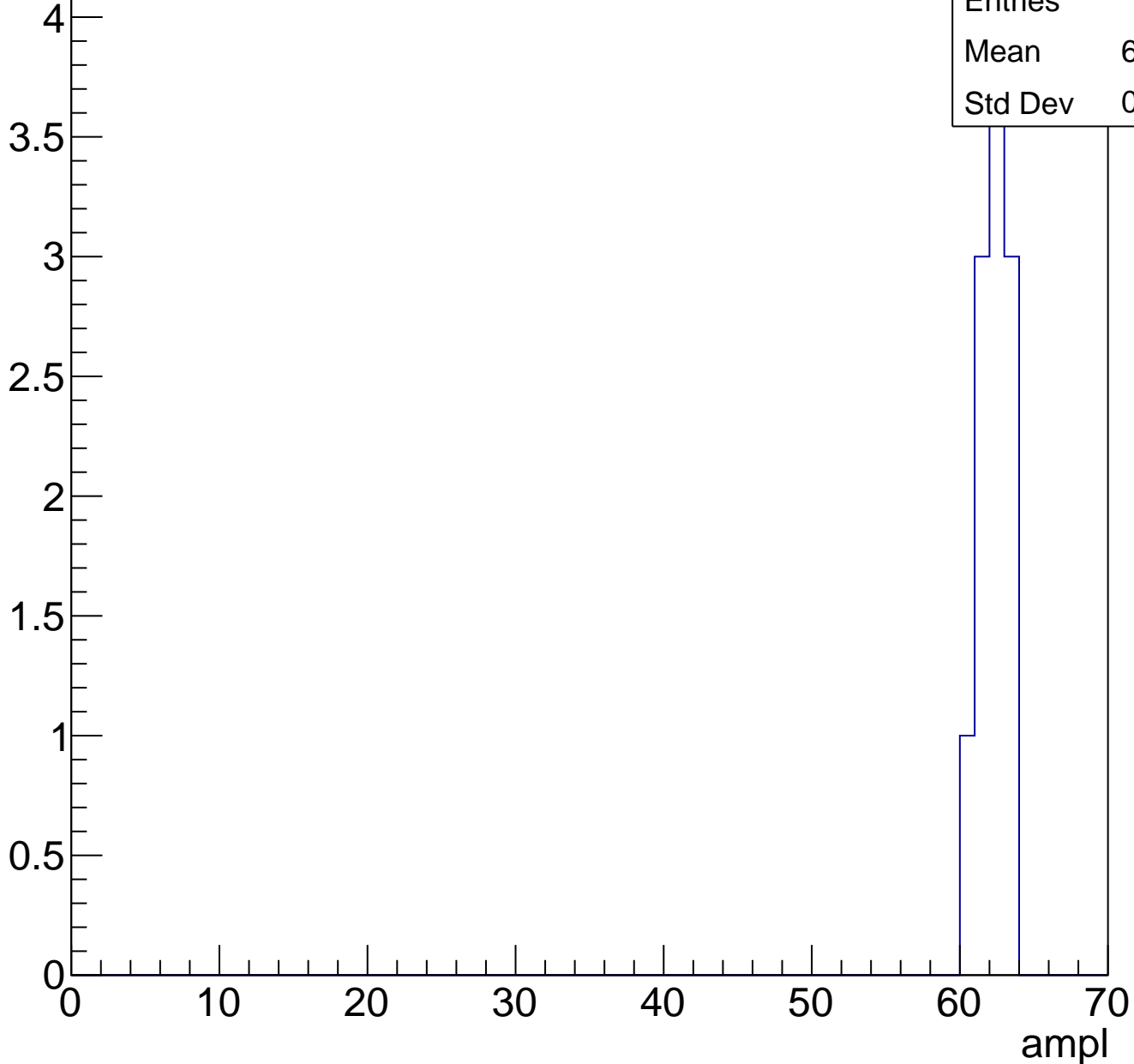
Entries	53
Mean	58.06
Std Dev	8.413



B1L103S, U5-ch24, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch24, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	3.316
Std Dev	14.07

ampl

0 10 20 30 40 50 60 70

B1L103S, U5-ch25, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	74
Mean	24.42
Std Dev	10.6

Entry

10

8

6

4

2

0

0

10

20

30

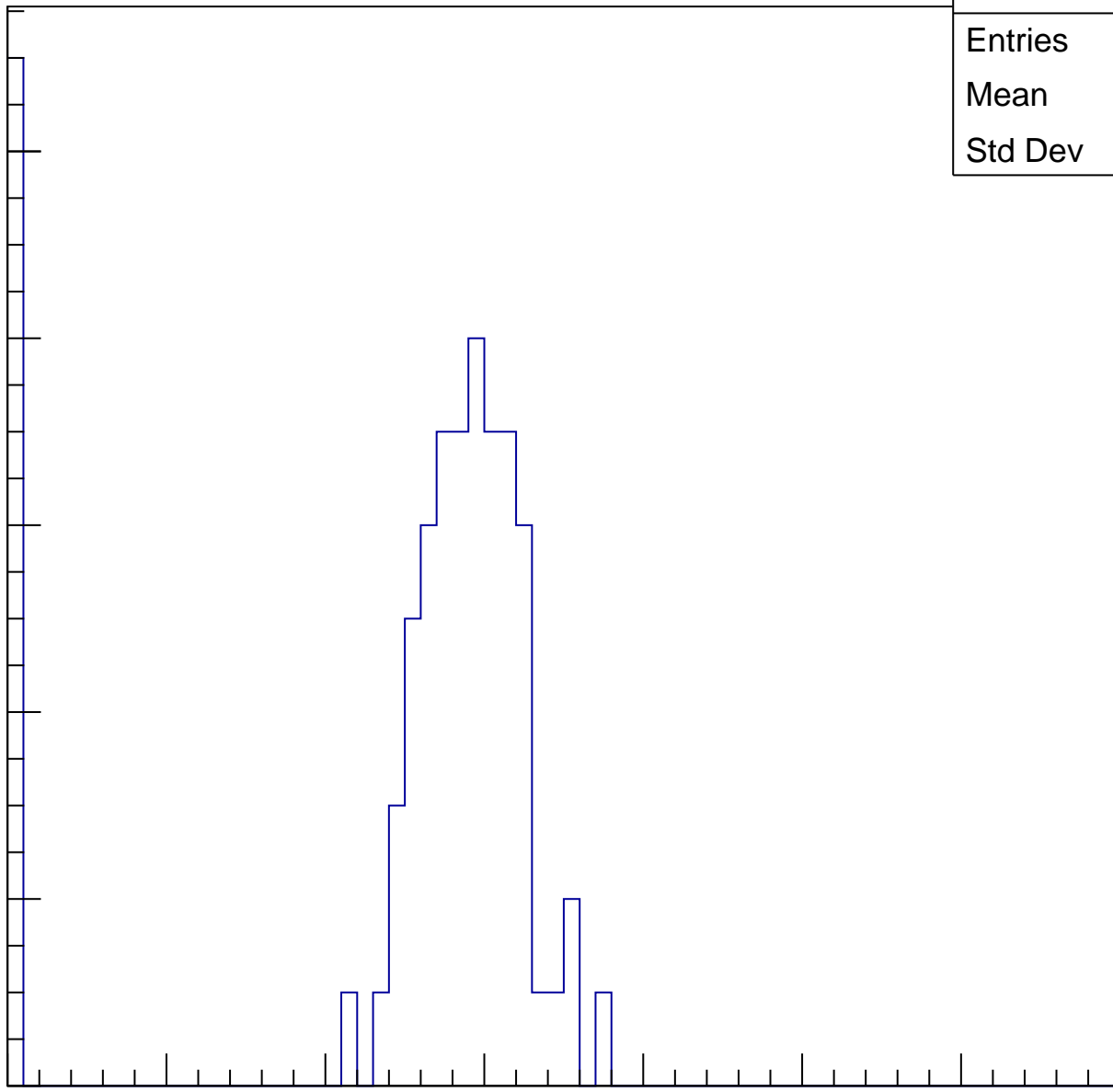
40

50

60

70

ampl



B1L103S, U5-ch25, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	70
Mean	33.73
Std Dev	7.794

Entry

10

8

6

4

2

0

0

10

20

30

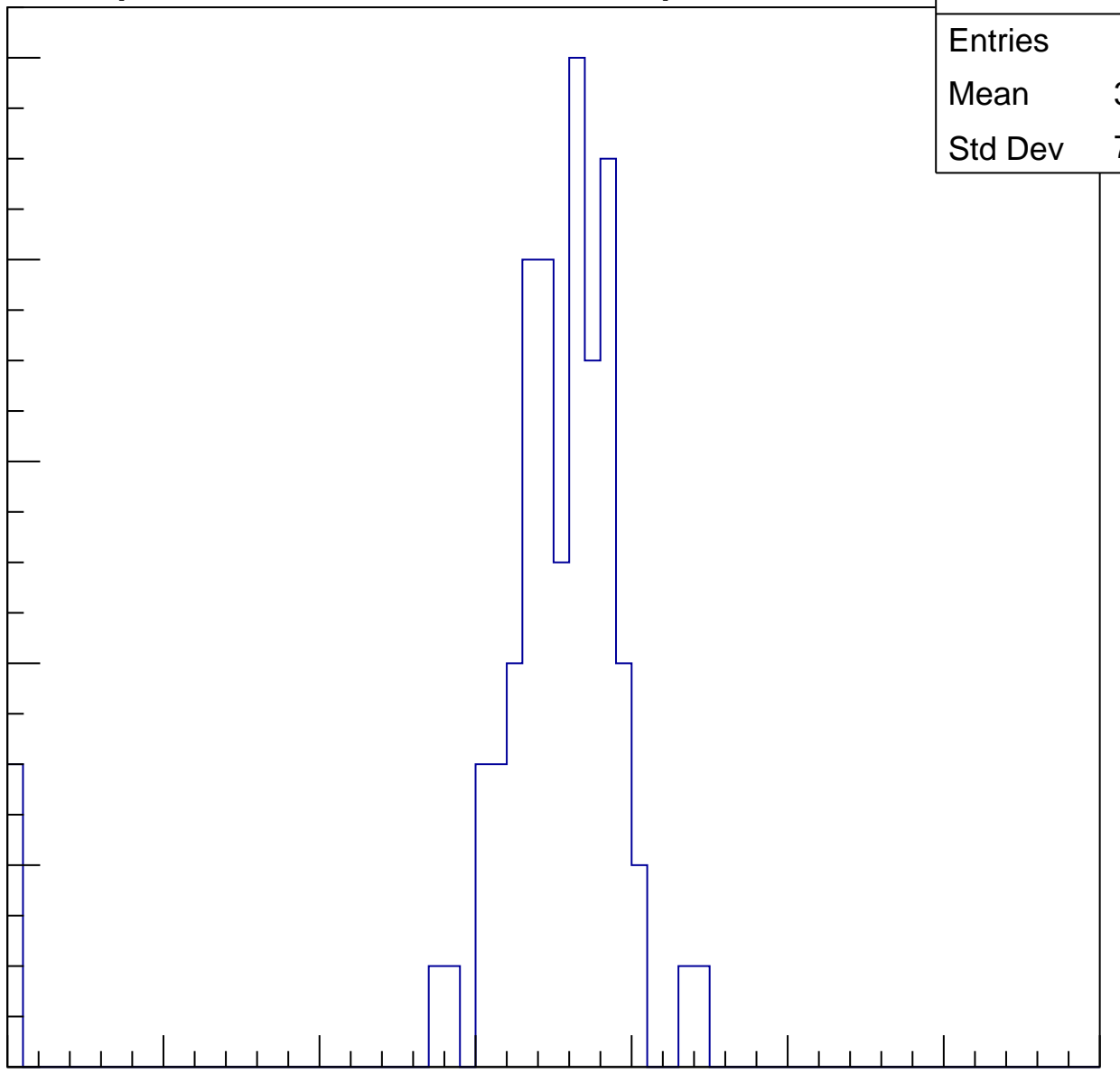
40

50

60

70

ampl

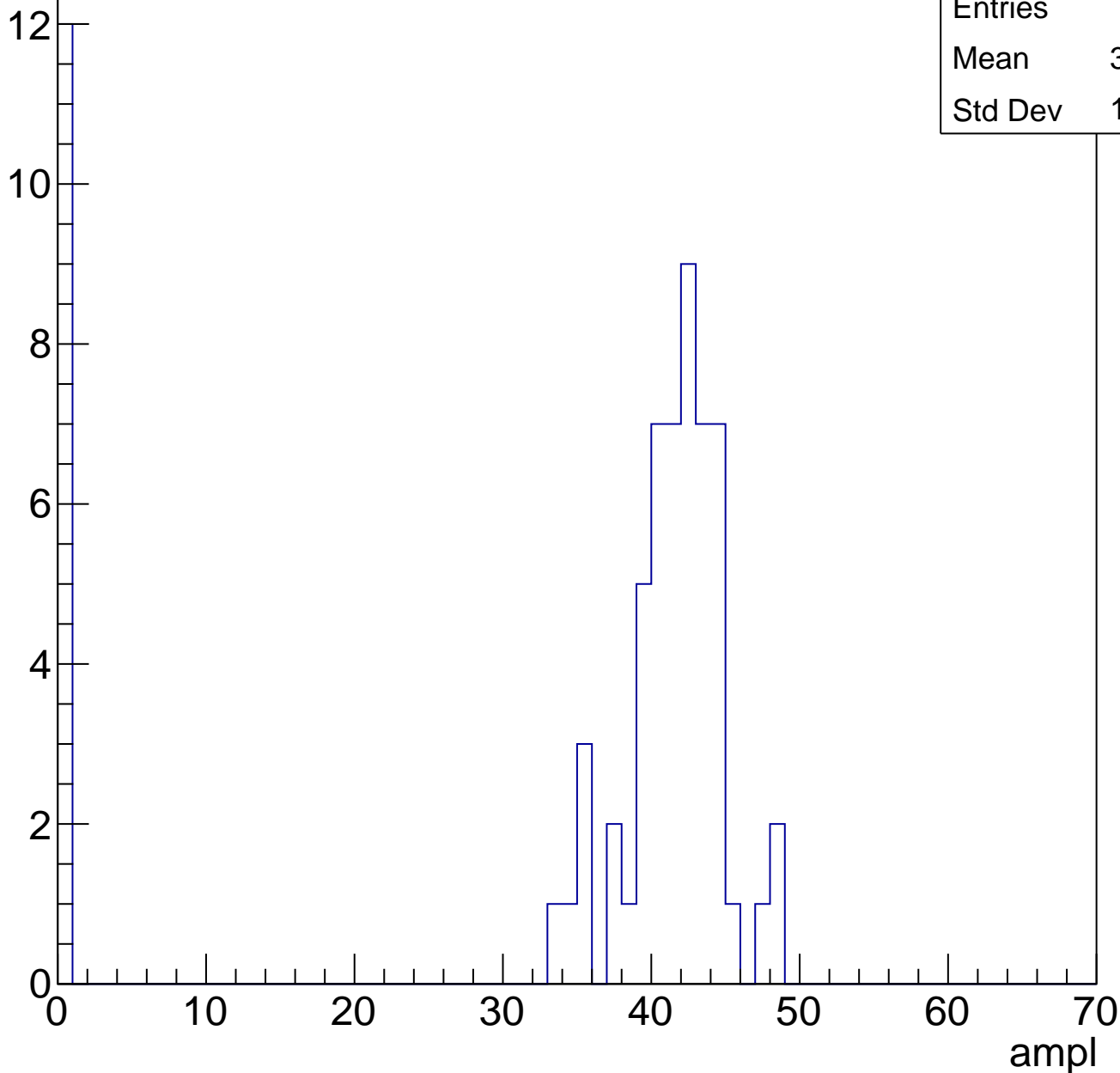


B1L103S, U5-ch25, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	66
Mean	33.65
Std Dev	16.12

Entry

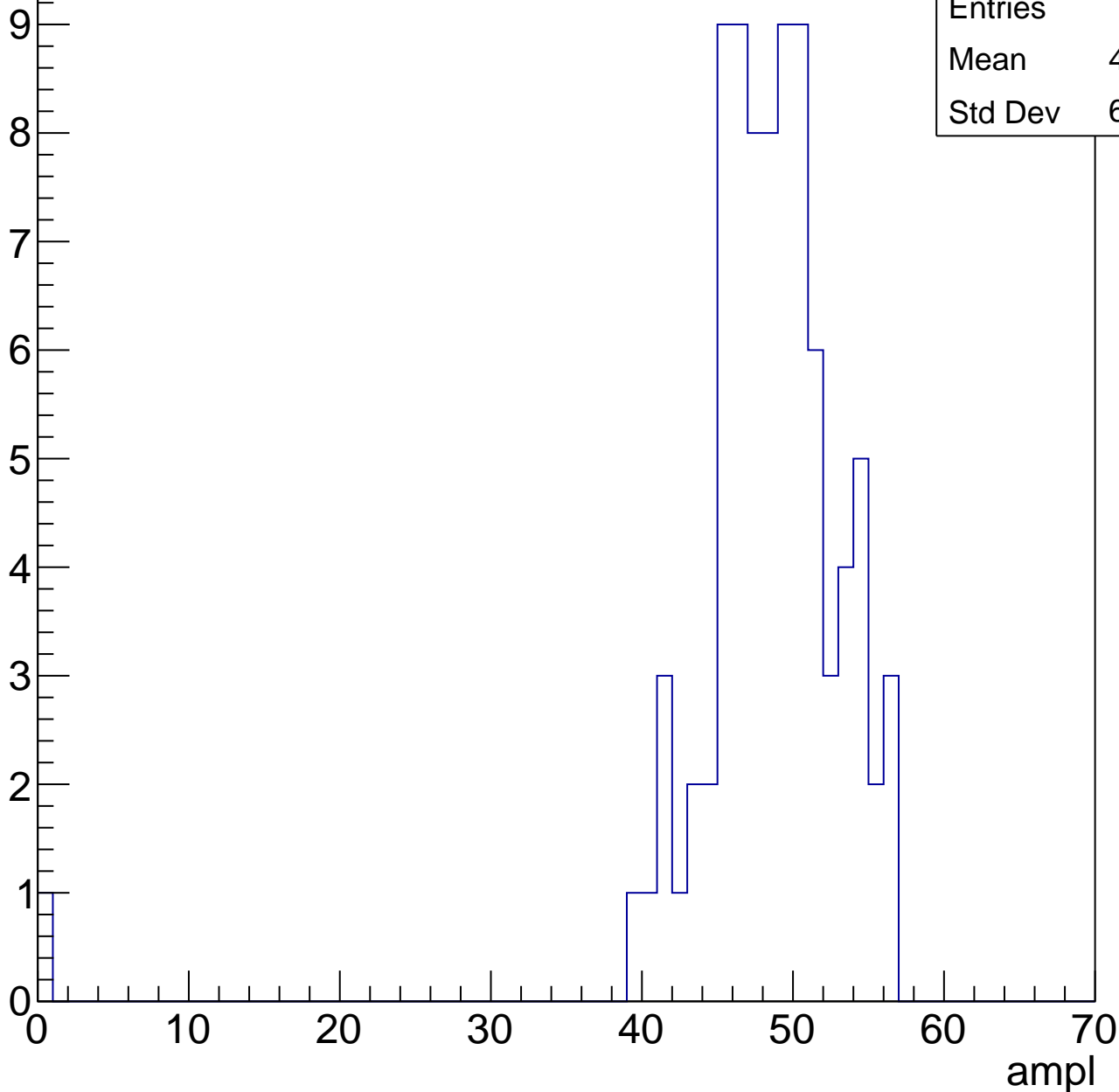


B1L103S, U5-ch25, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	86
Mean	47.79
Std Dev	6.427

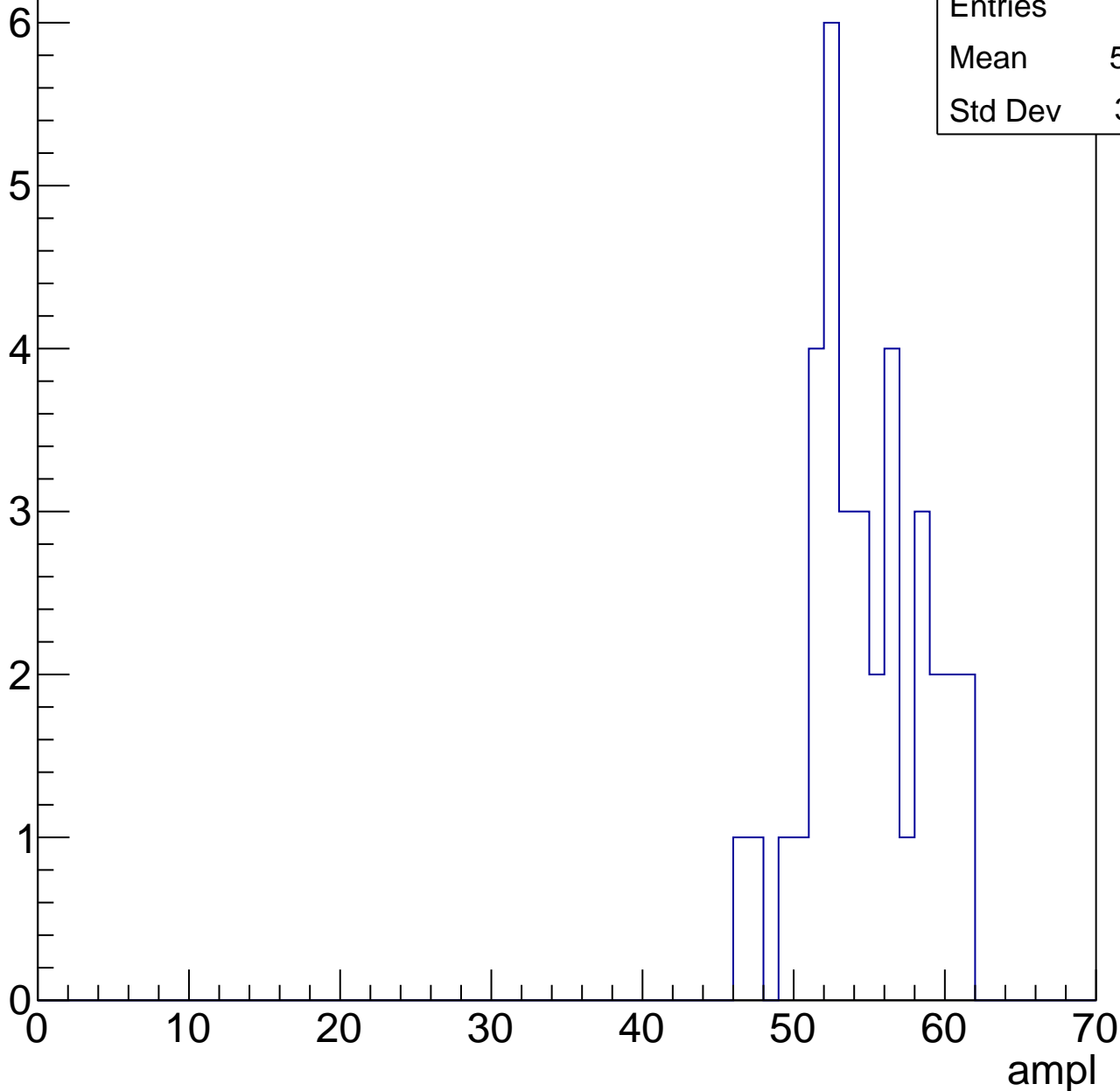


B1L103S, U5-ch25, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

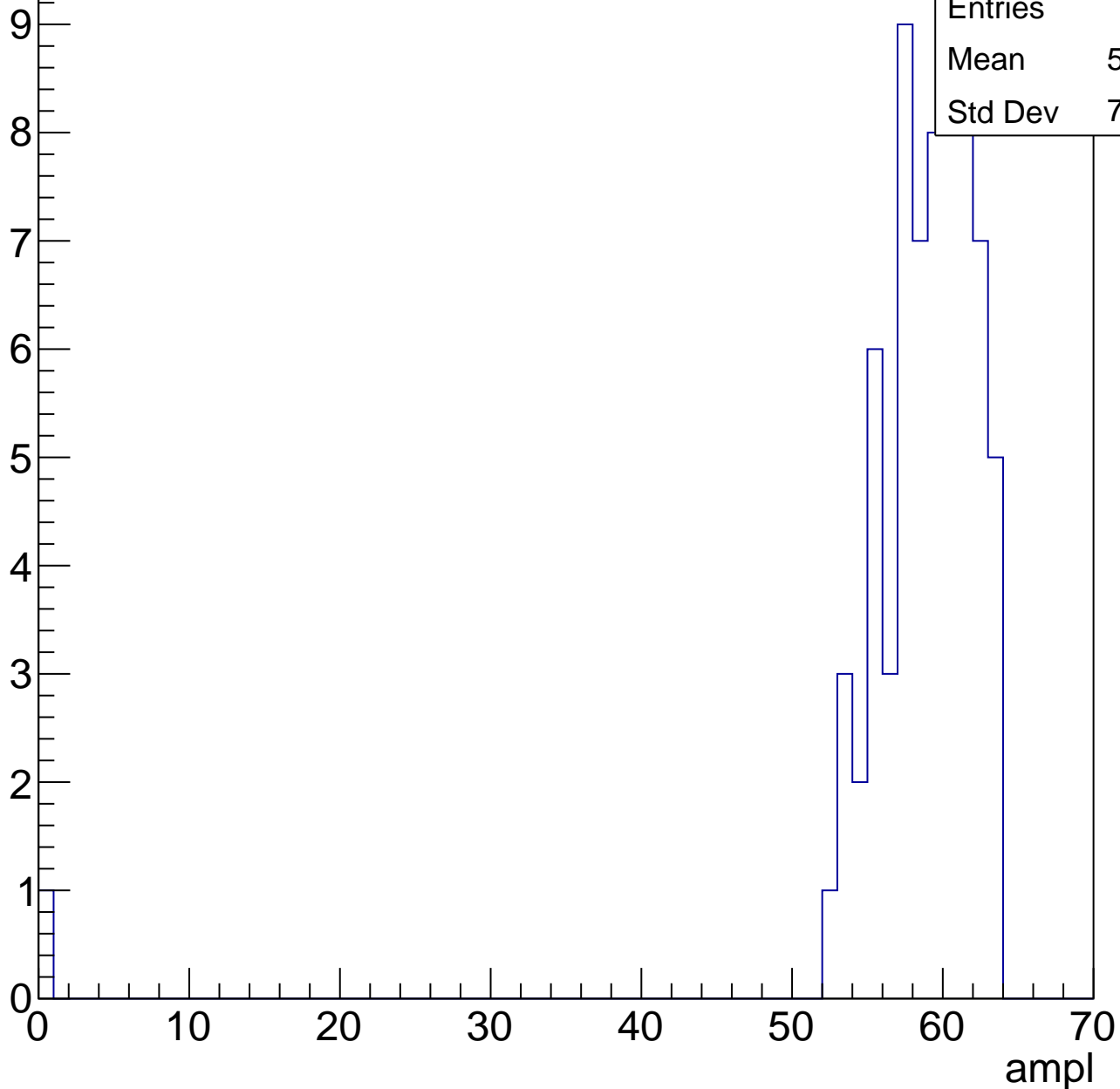
Entries	36
Mean	54.28
Std Dev	3.761



B1L103S, U5-ch25, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

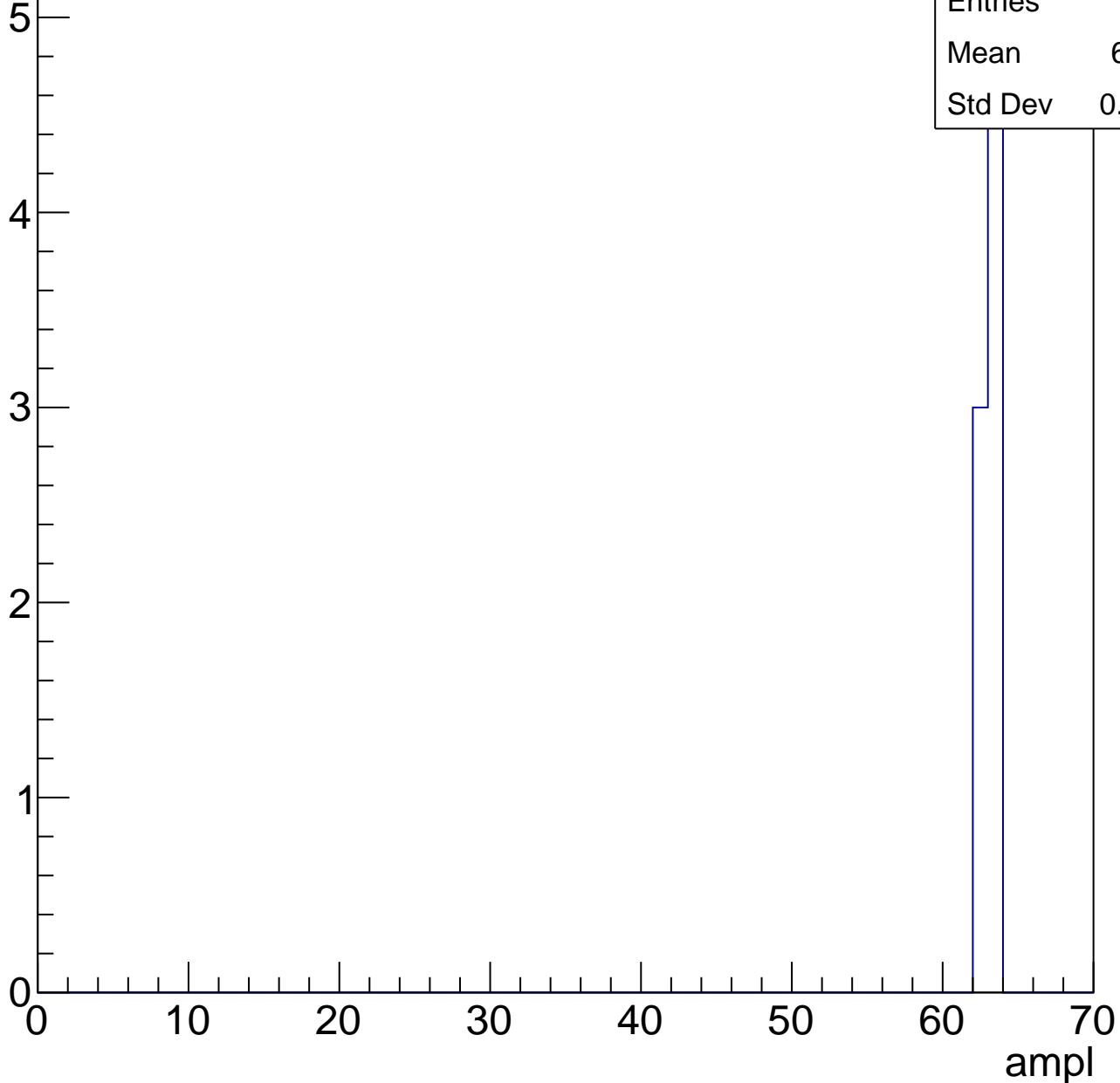


B1L103S, U5-ch25, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	8
Mean	62.62
Std Dev	0.4841



B1L103S, U5-ch25, adc7

calib_packv5_041523_1651.root, FC#0, port C2

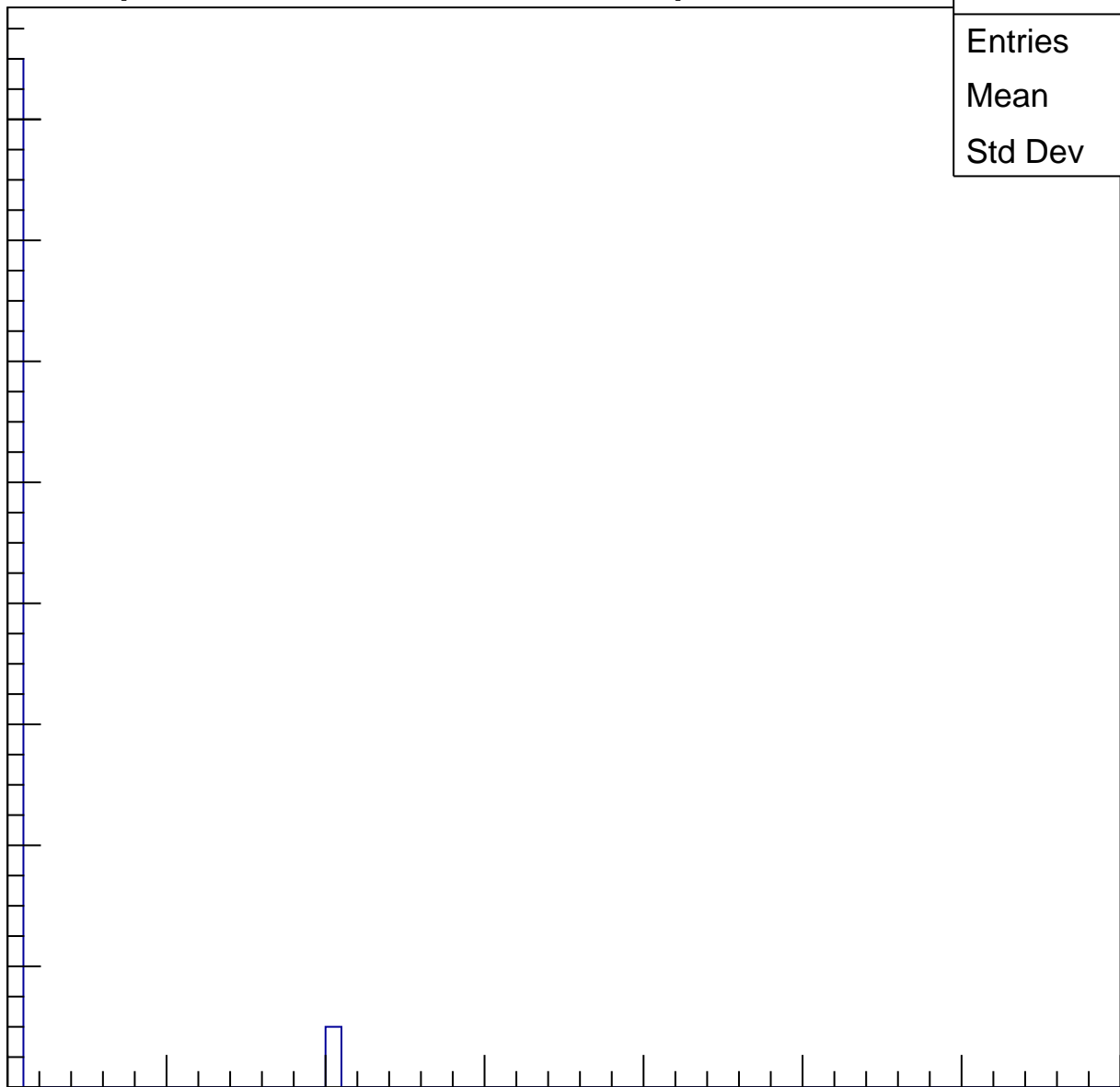
Entries	18
Mean	1.111
Std Dev	4.581

Entry

16
14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

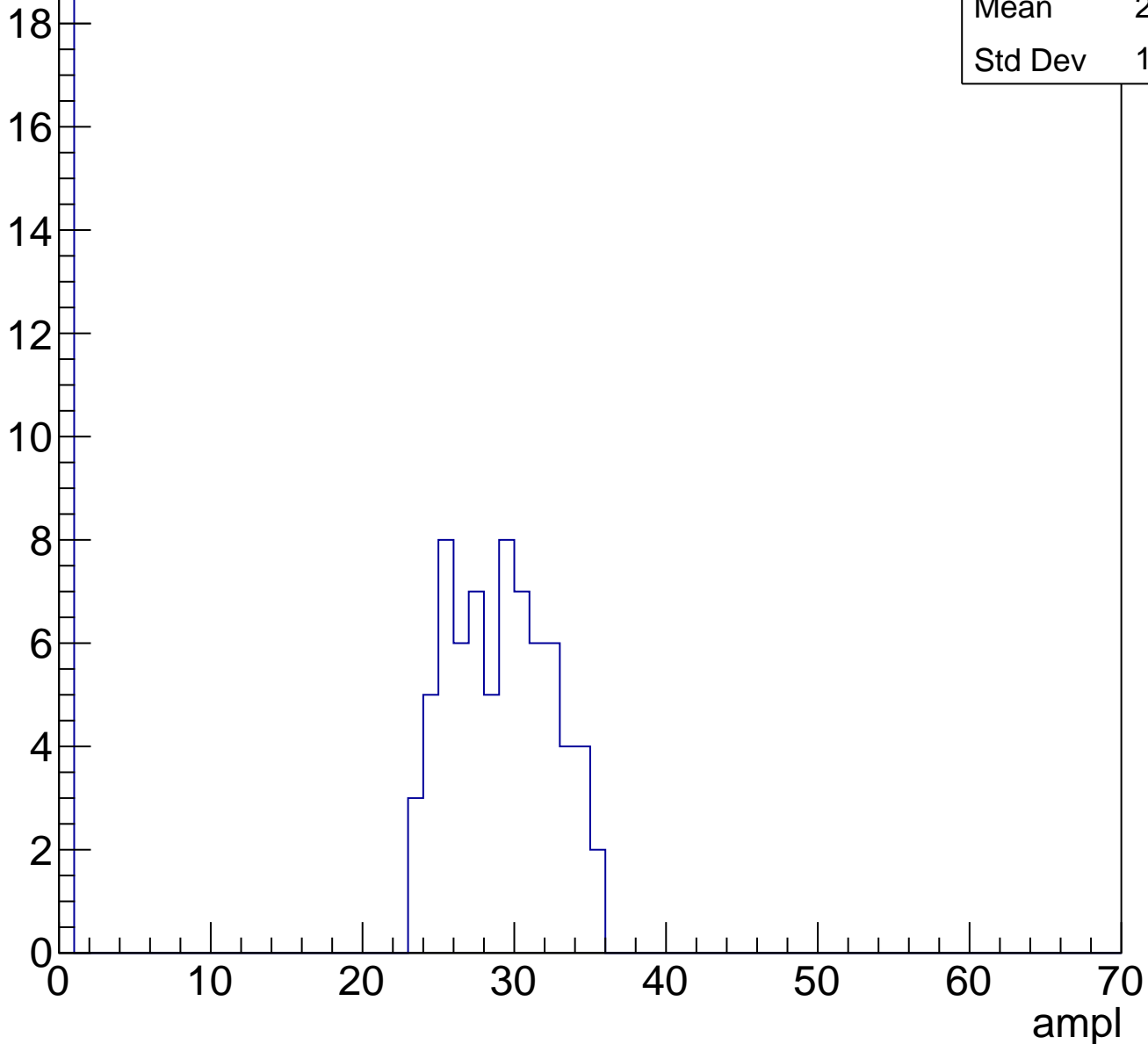


B1L103S, U5-ch26, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	90
Mean	22.58
Std Dev	12.04

Entry

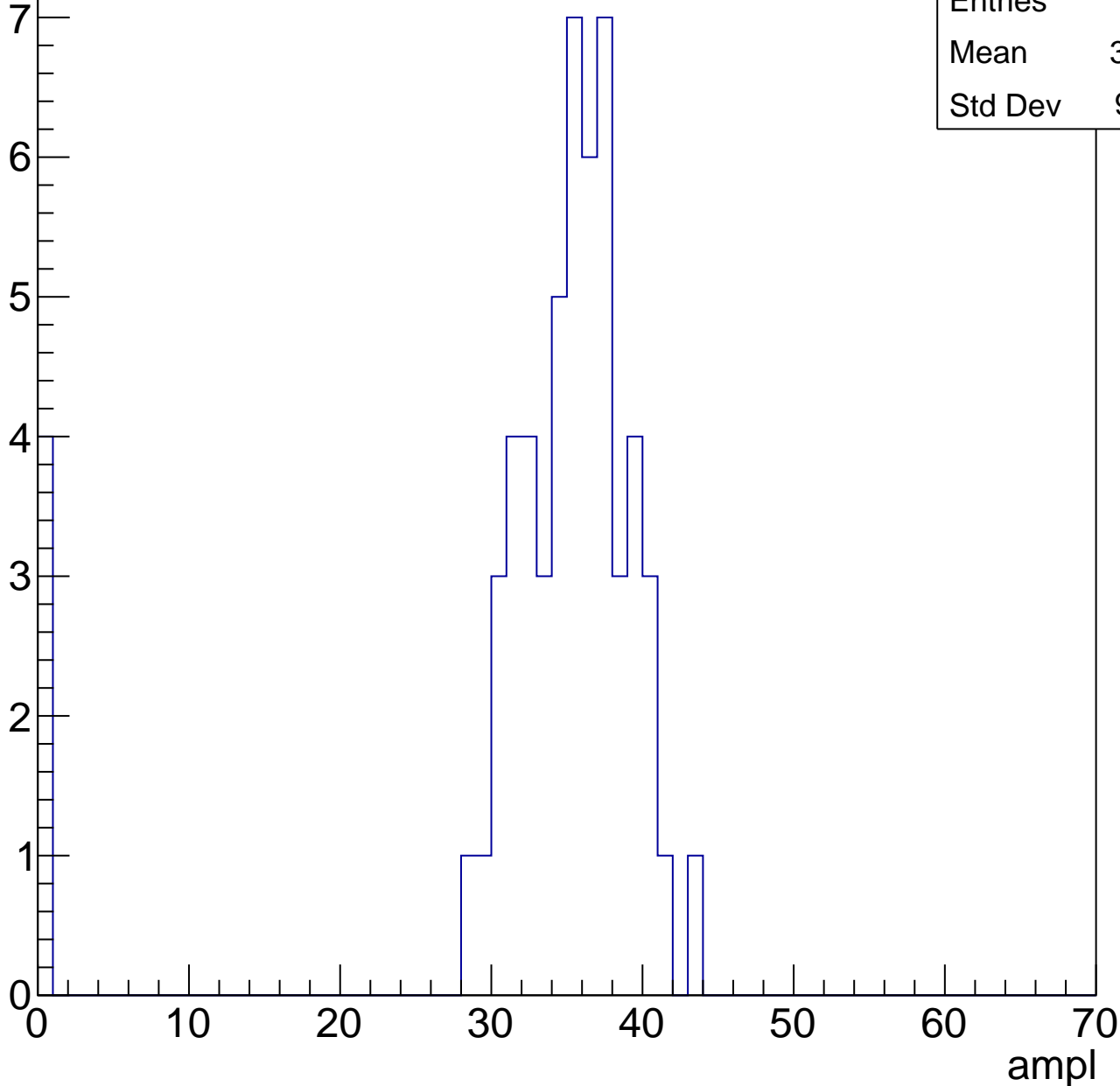


B1L103S, U5-ch26, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	32.67
Std Dev	9.521

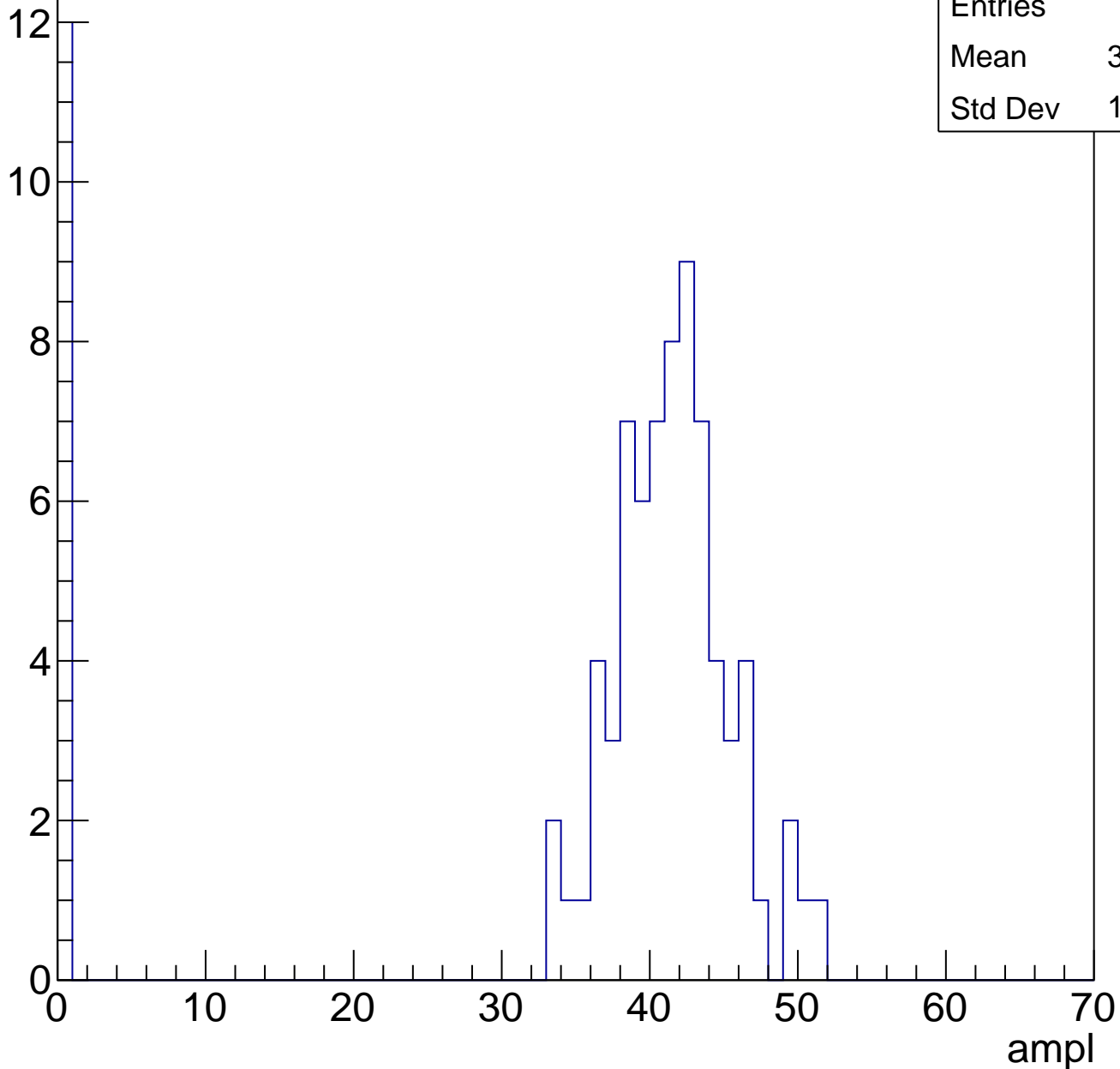


B1L103S, U5-ch26, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	83
Mean	35.16
Std Dev	14.87

Entry

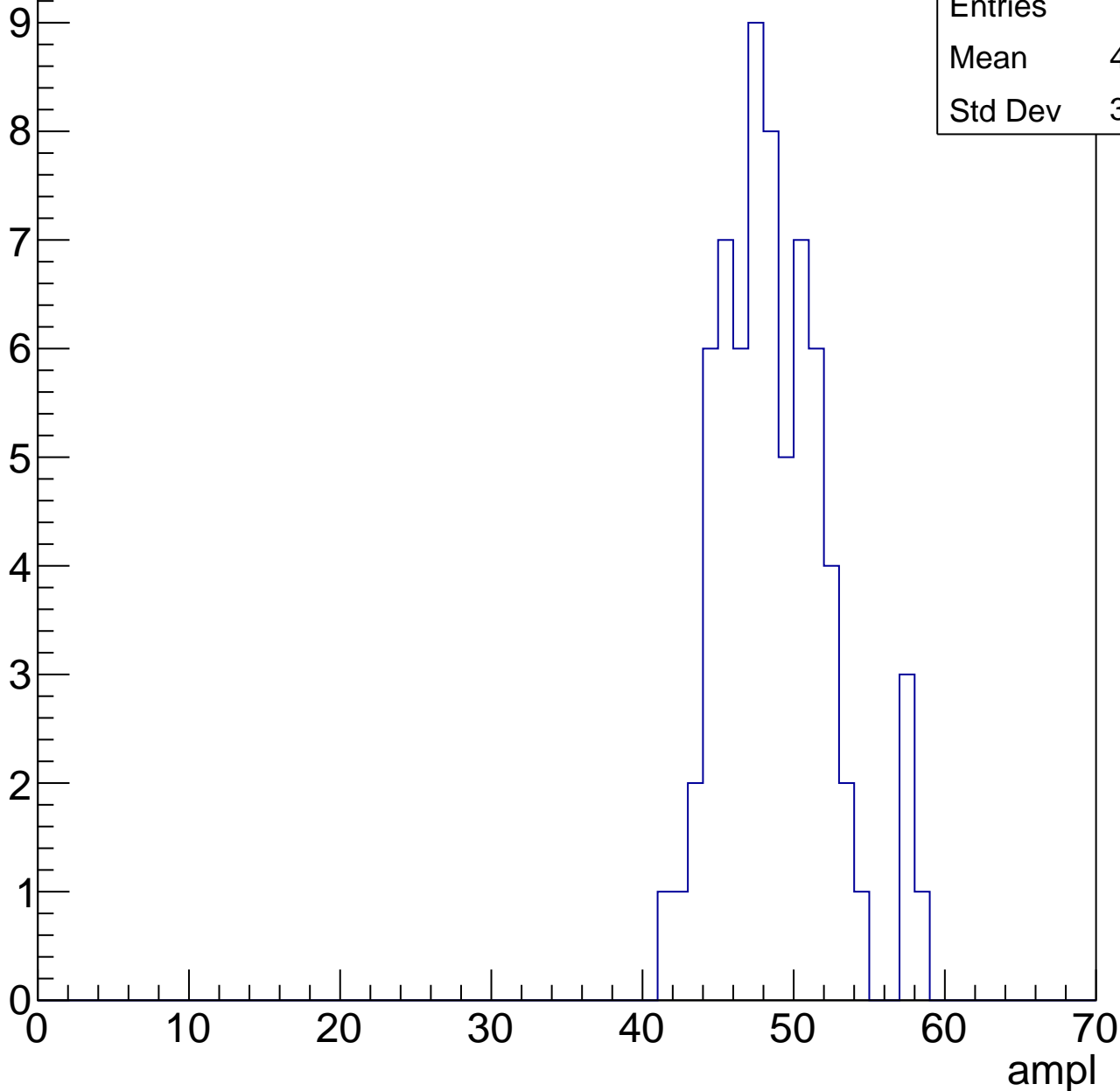


B1L103S, U5-ch26, adc3

calib_packv5_041523_1651.root, FC#0, port C2

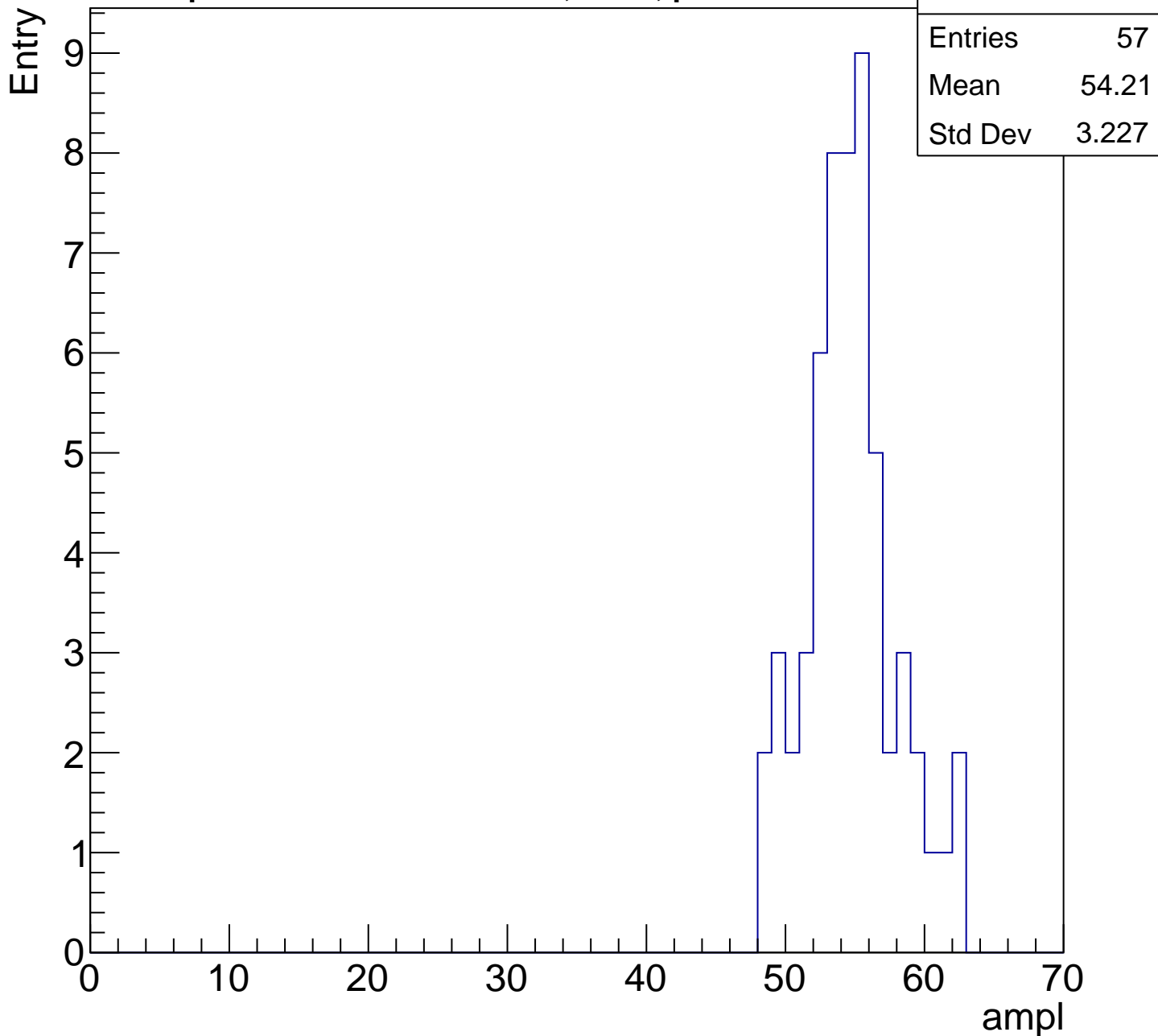
Entry

Entries	69
Mean	48.25
Std Dev	3.617



B1L103S, U5-ch26, adc4

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U5-ch26, adc5

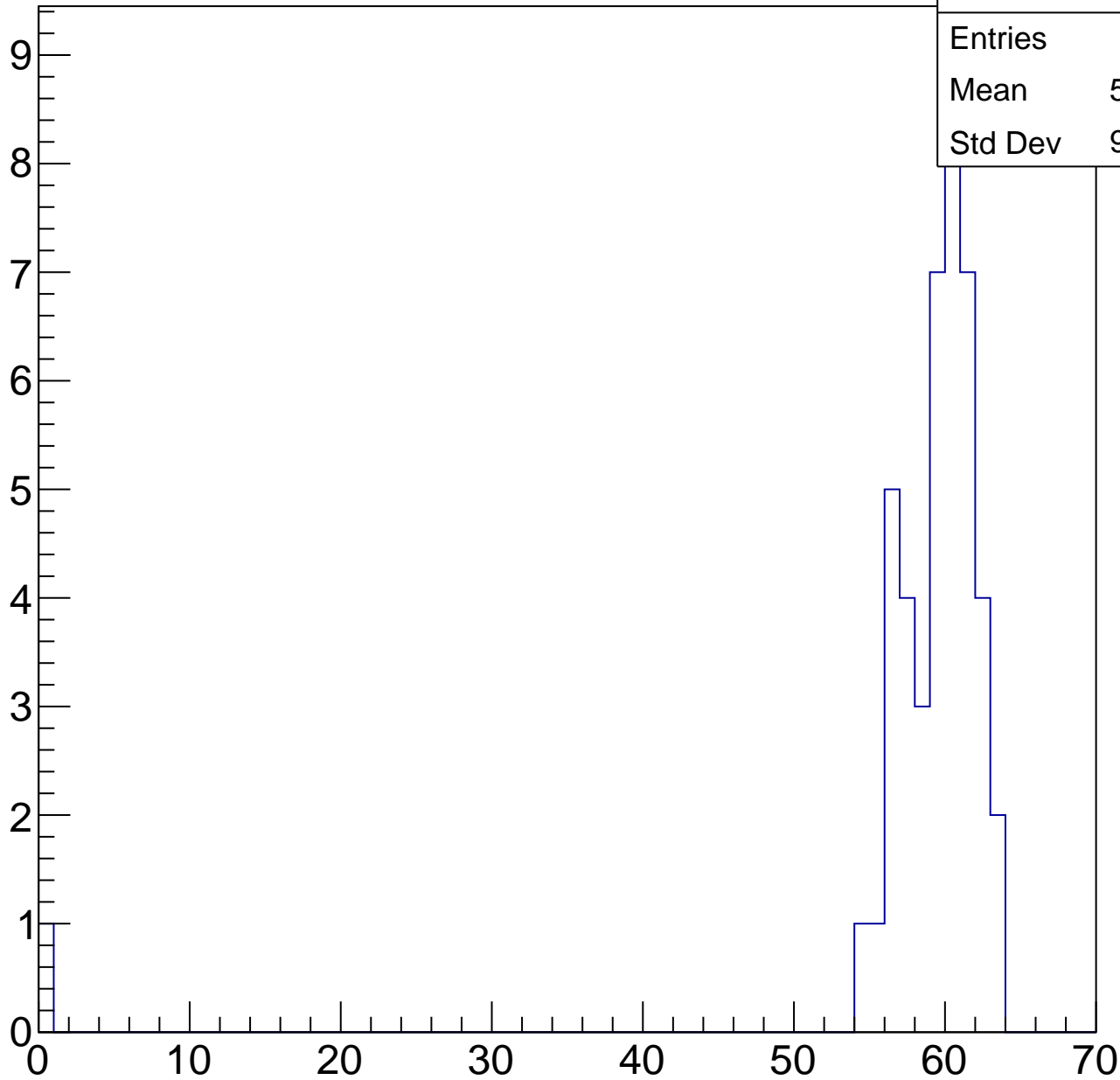
calib_packv5_041523_1651.root, FC#0, port C2

Entry

9
8
7
6
5
4
3
2
1
0

Entries	44
Mean	57.84
Std Dev	9.085

ampl

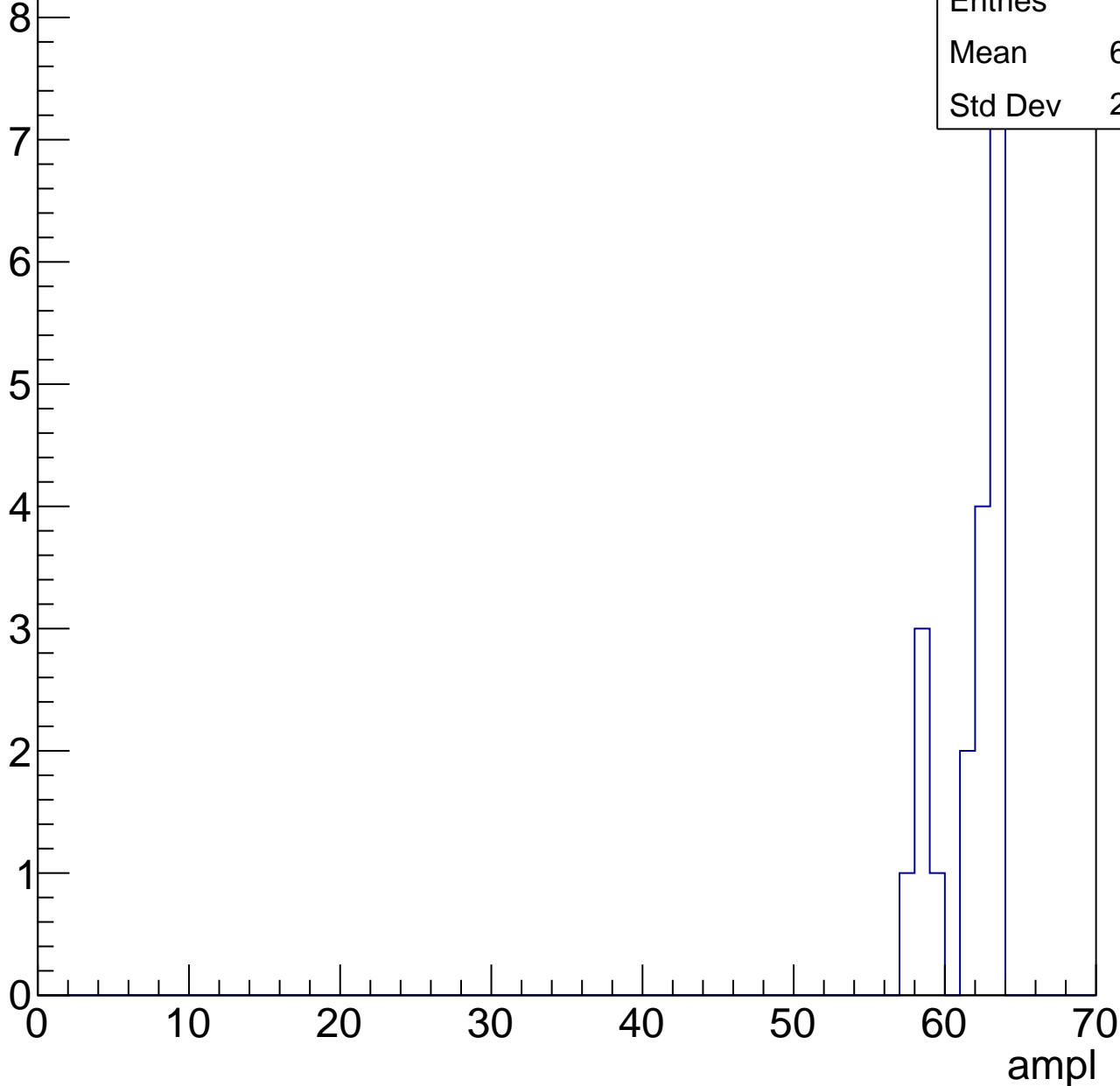


B1L103S, U5-ch26, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

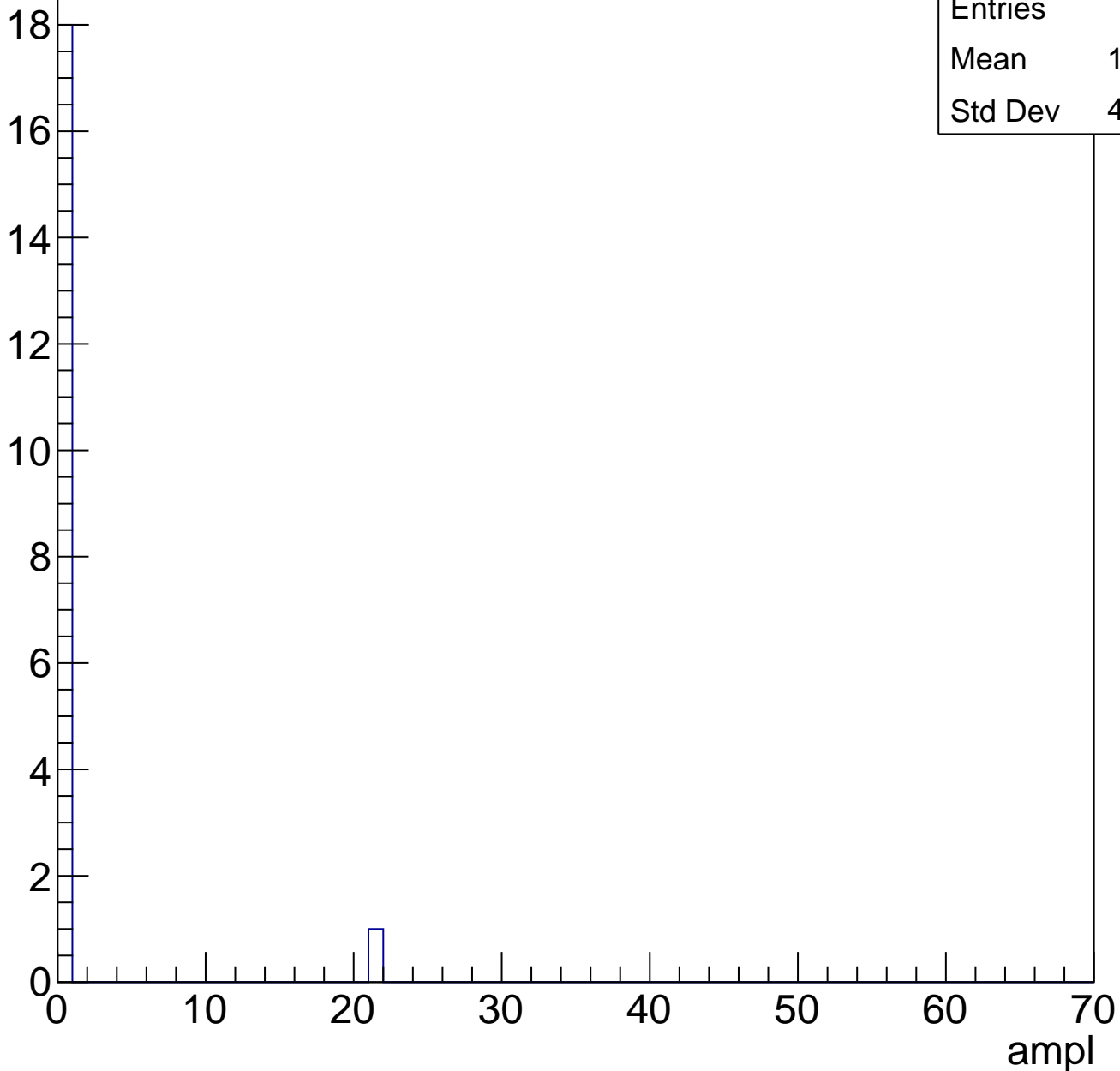
Entries	19
Mean	61.26
Std Dev	2.073



B1L103S, U5-ch26, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

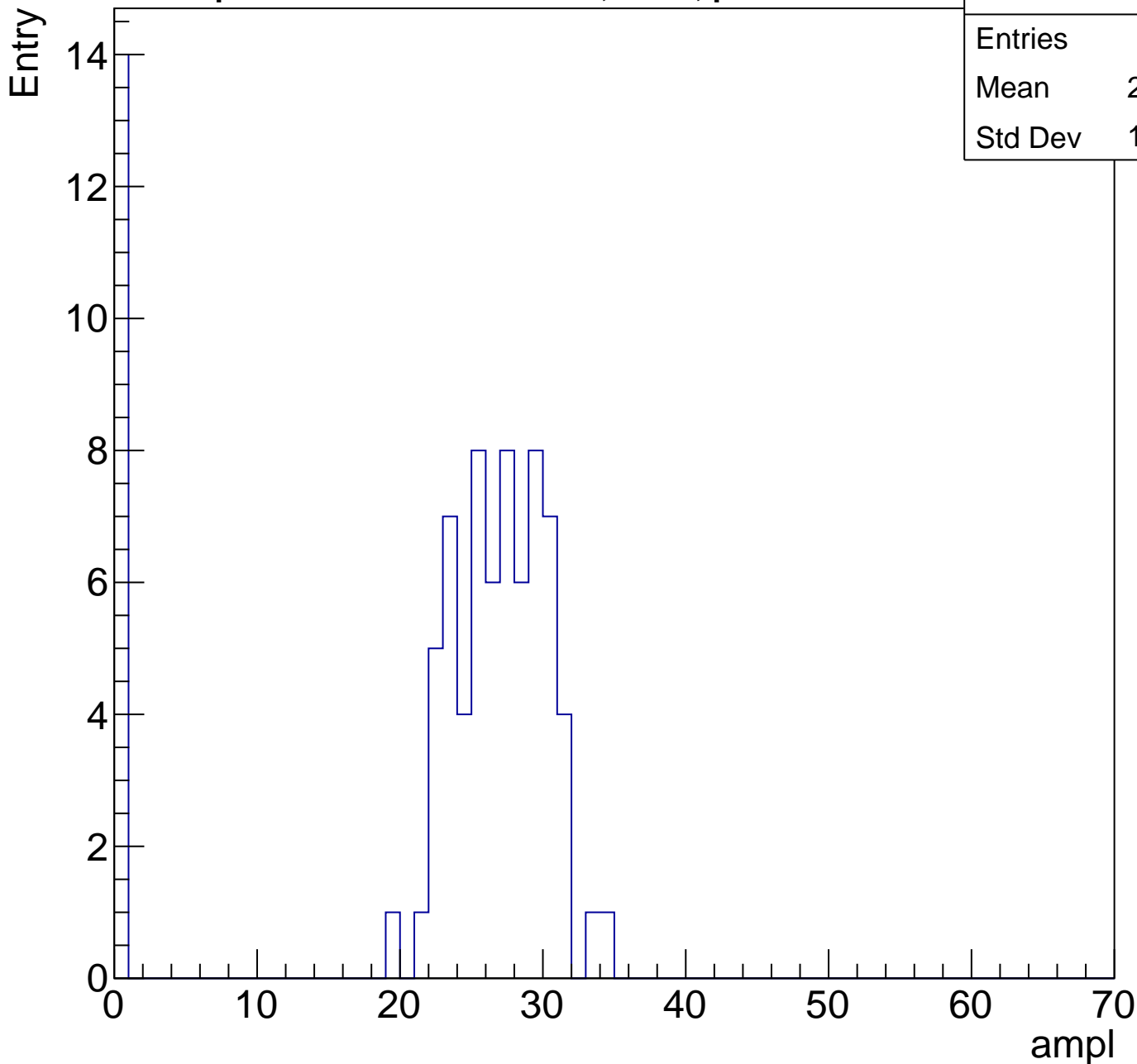


Entries	19
Mean	1.105
Std Dev	4.689

B1L103S, U5-ch27, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	21.98
Std Dev	10.44

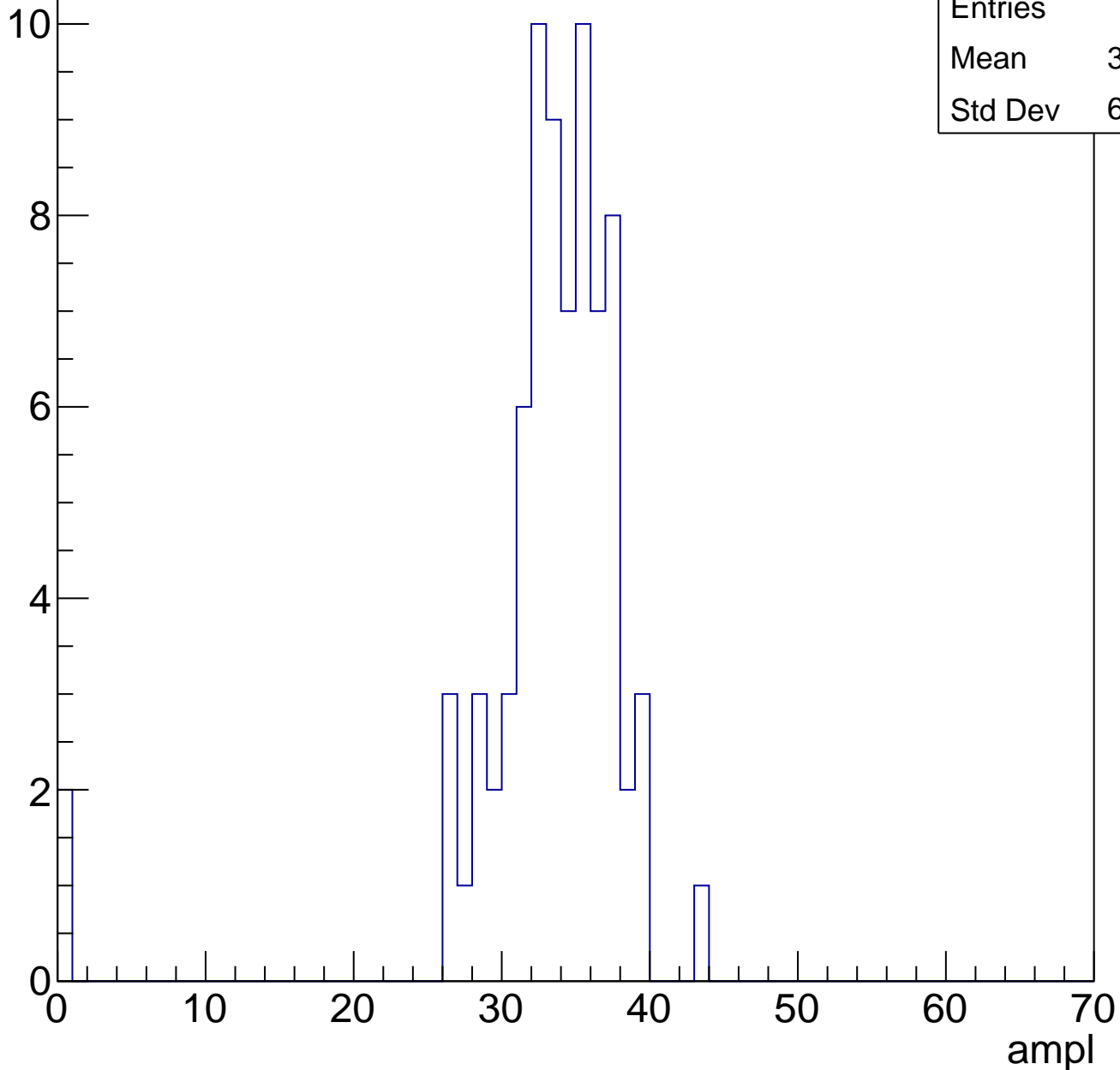


B1L103S, U5-ch27, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	77
Mean	32.62
Std Dev	6.257

Entry



B1L103S, U5-ch27, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

12

10

8

6

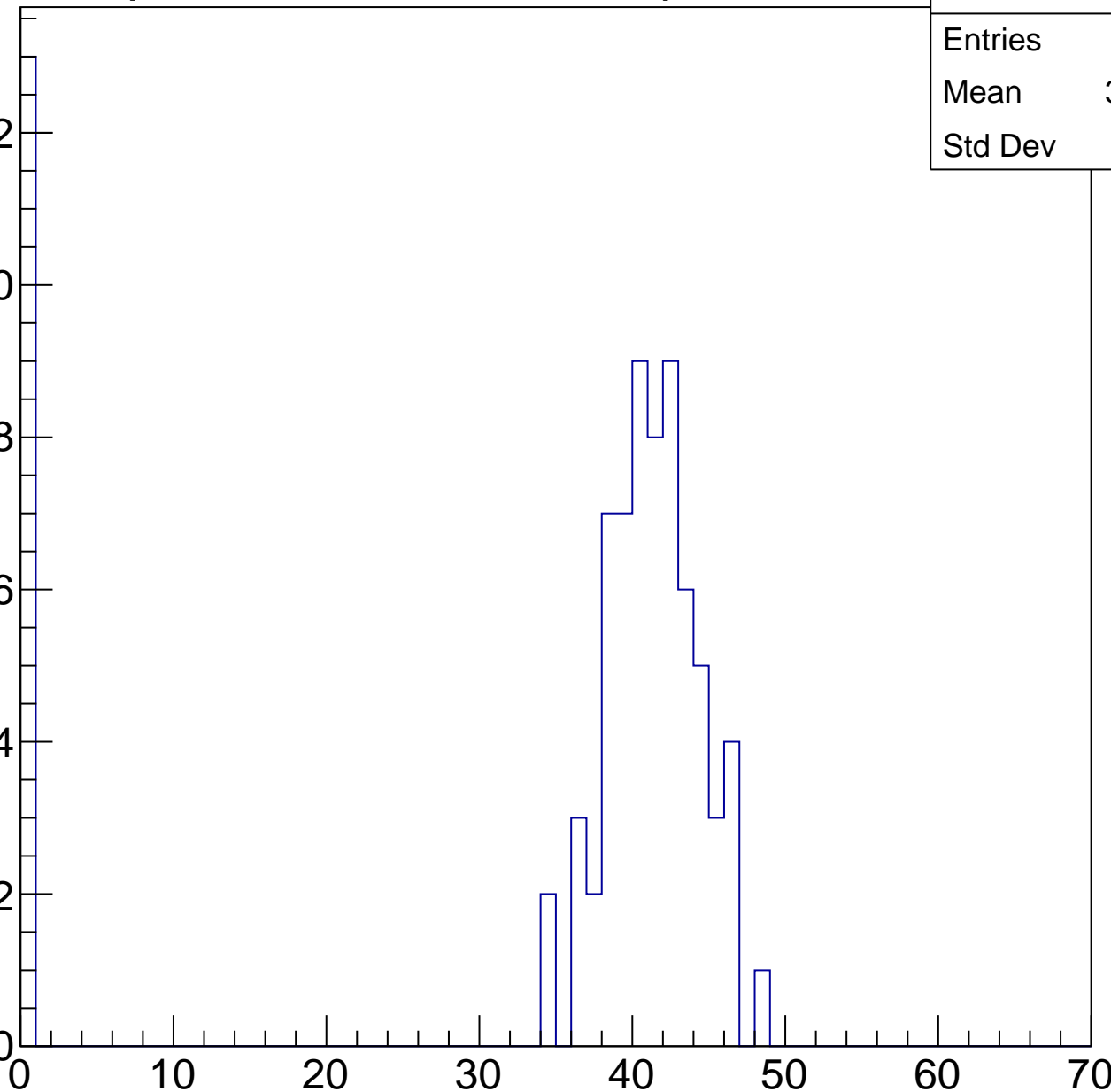
4

2

0

Entries	79
Mean	34.18
Std Dev	15.41

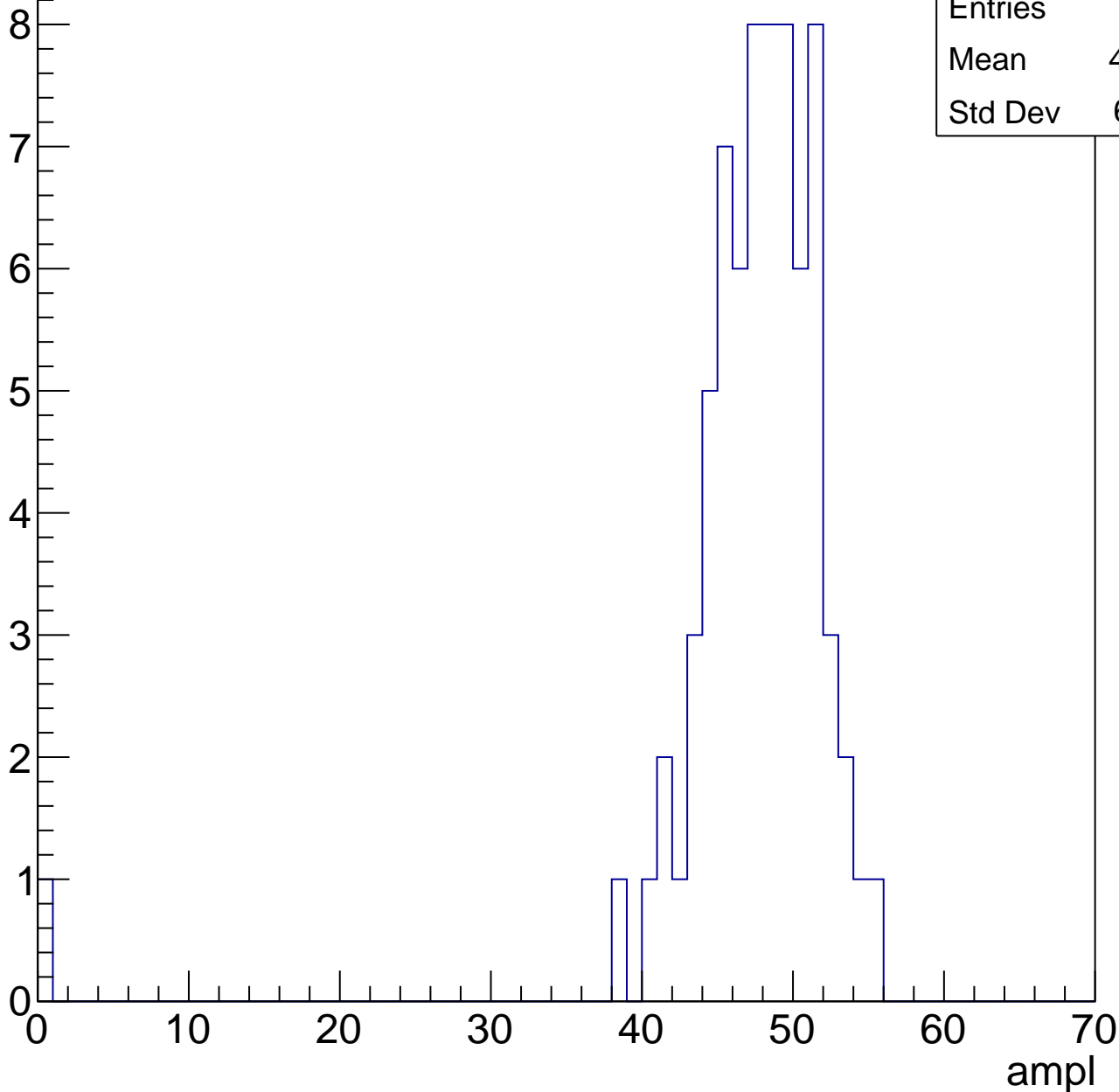
ampl



B1L103S, U5-ch27, adc3

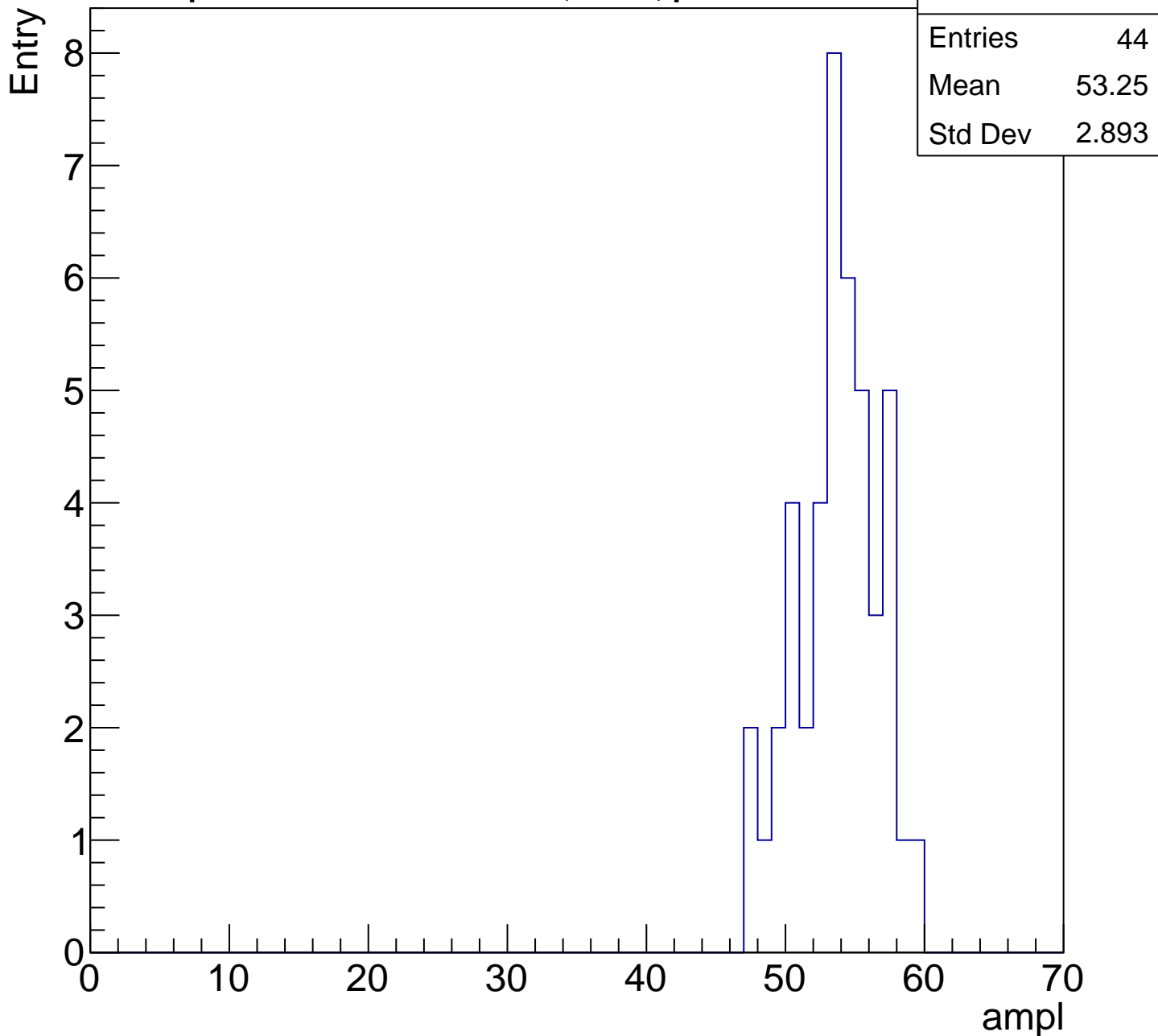
calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch27, adc4

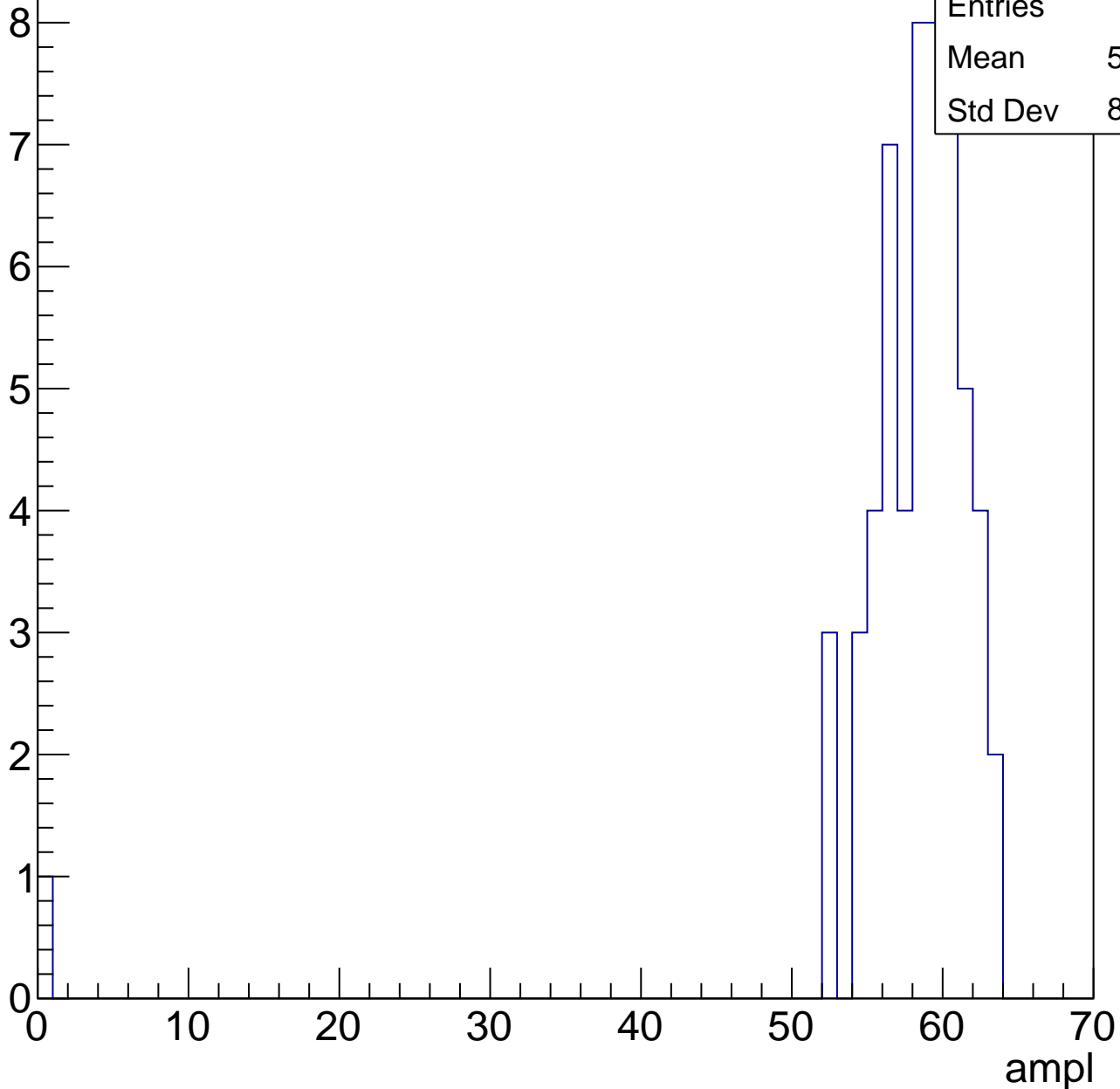
calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U5-ch27, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

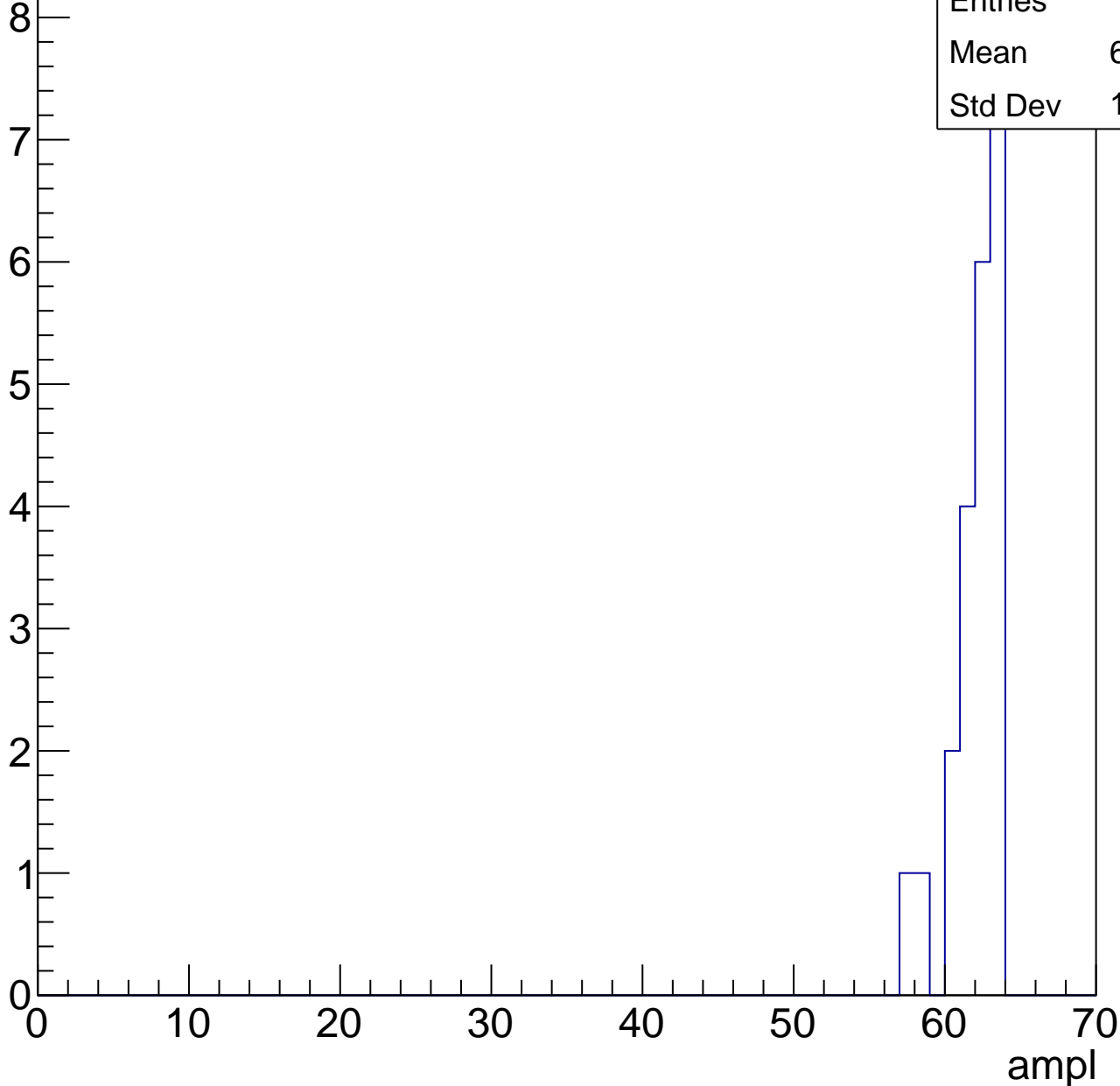


B1L103S, U5-ch27, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

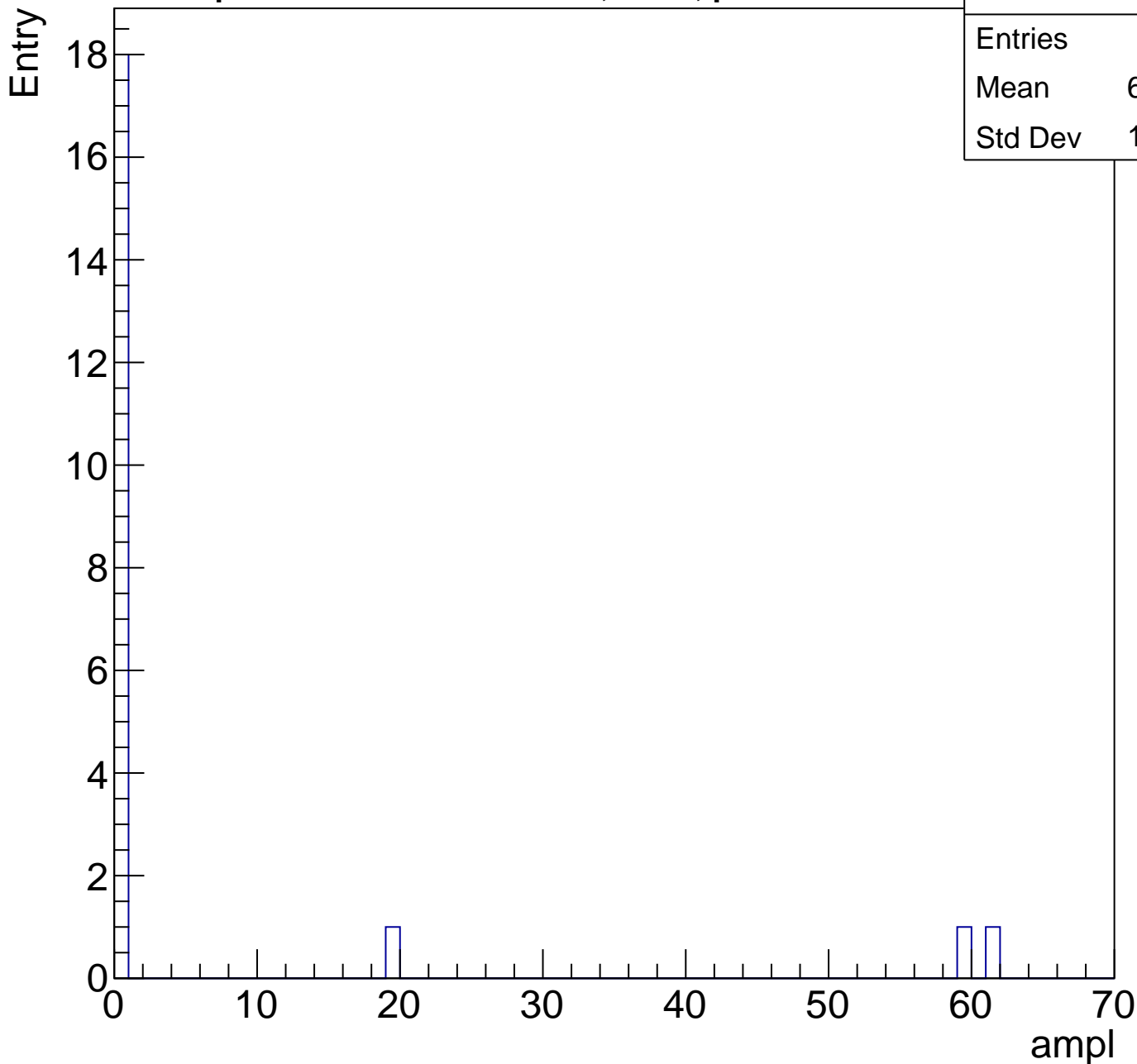
Entries	22
Mean	61.59
Std Dev	1.614



B1L103S, U5-ch27, adc7

calib_packv5_041523_1651.root, FC#0, port C2

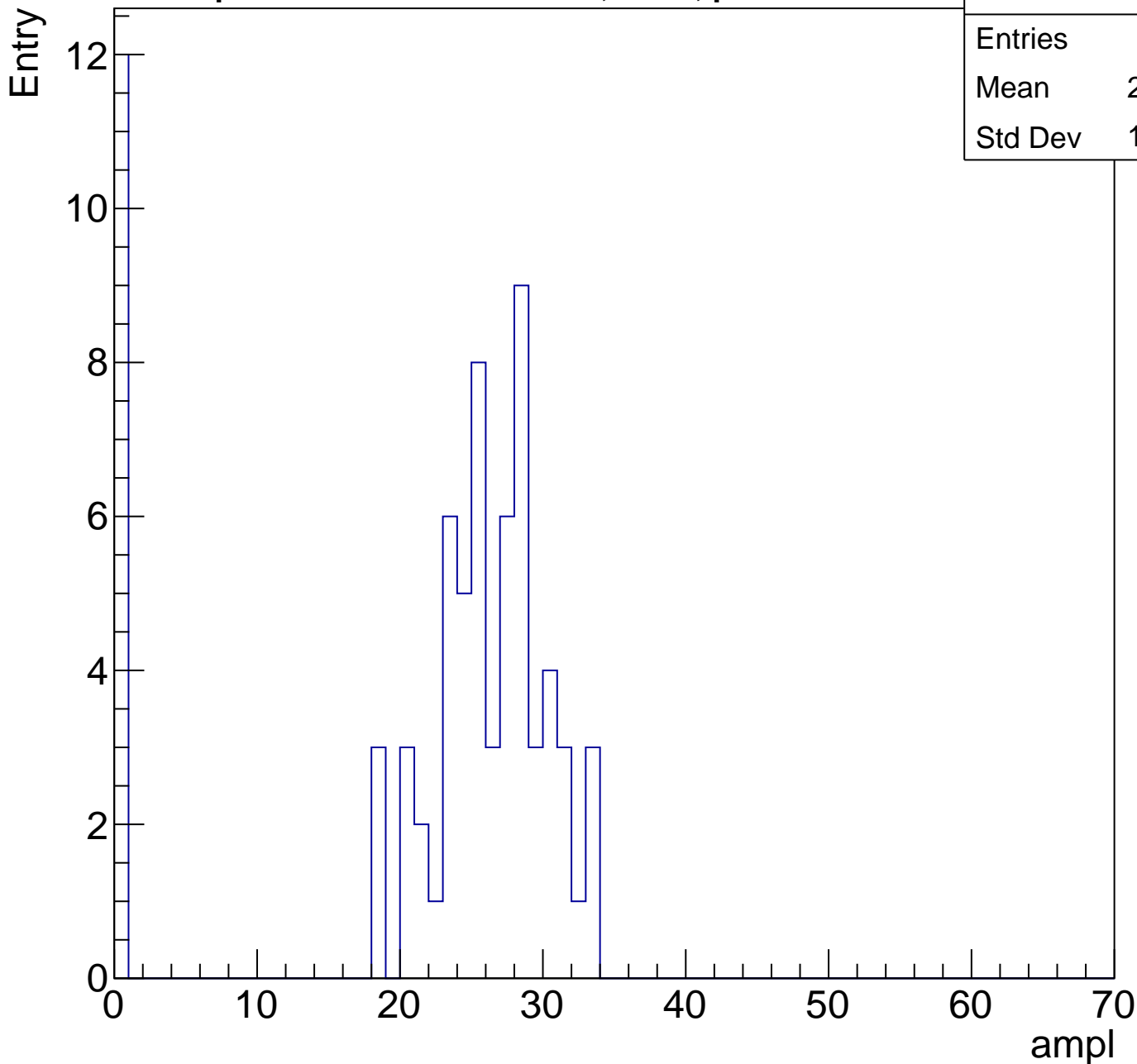
Entries	21
Mean	6.619
Std Dev	17.79



B1L103S, U5-ch28, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	72
Mean	21.65
Std Dev	10.27

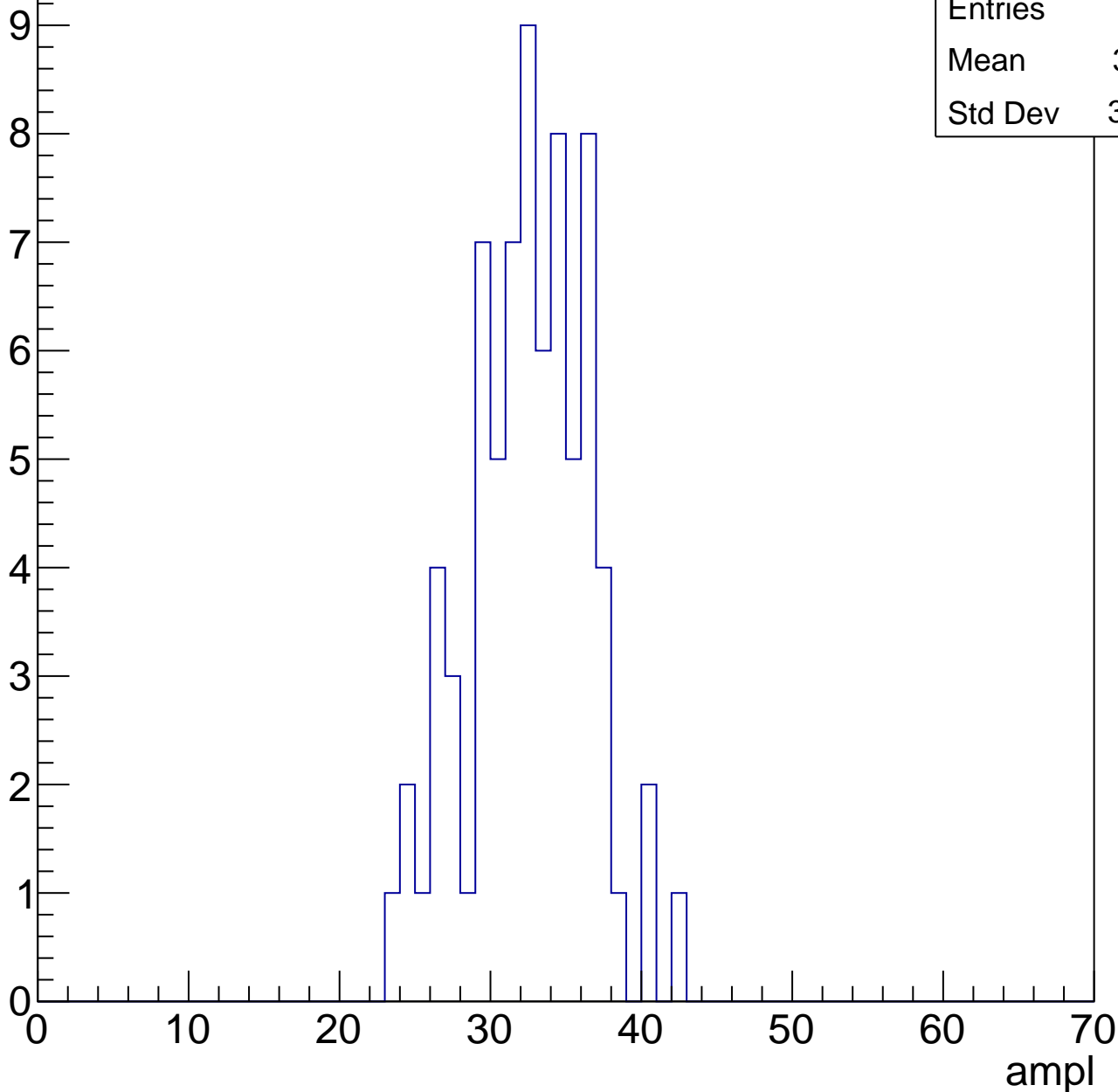


B1L103S, U5-ch28, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	32.11
Std Dev	3.928

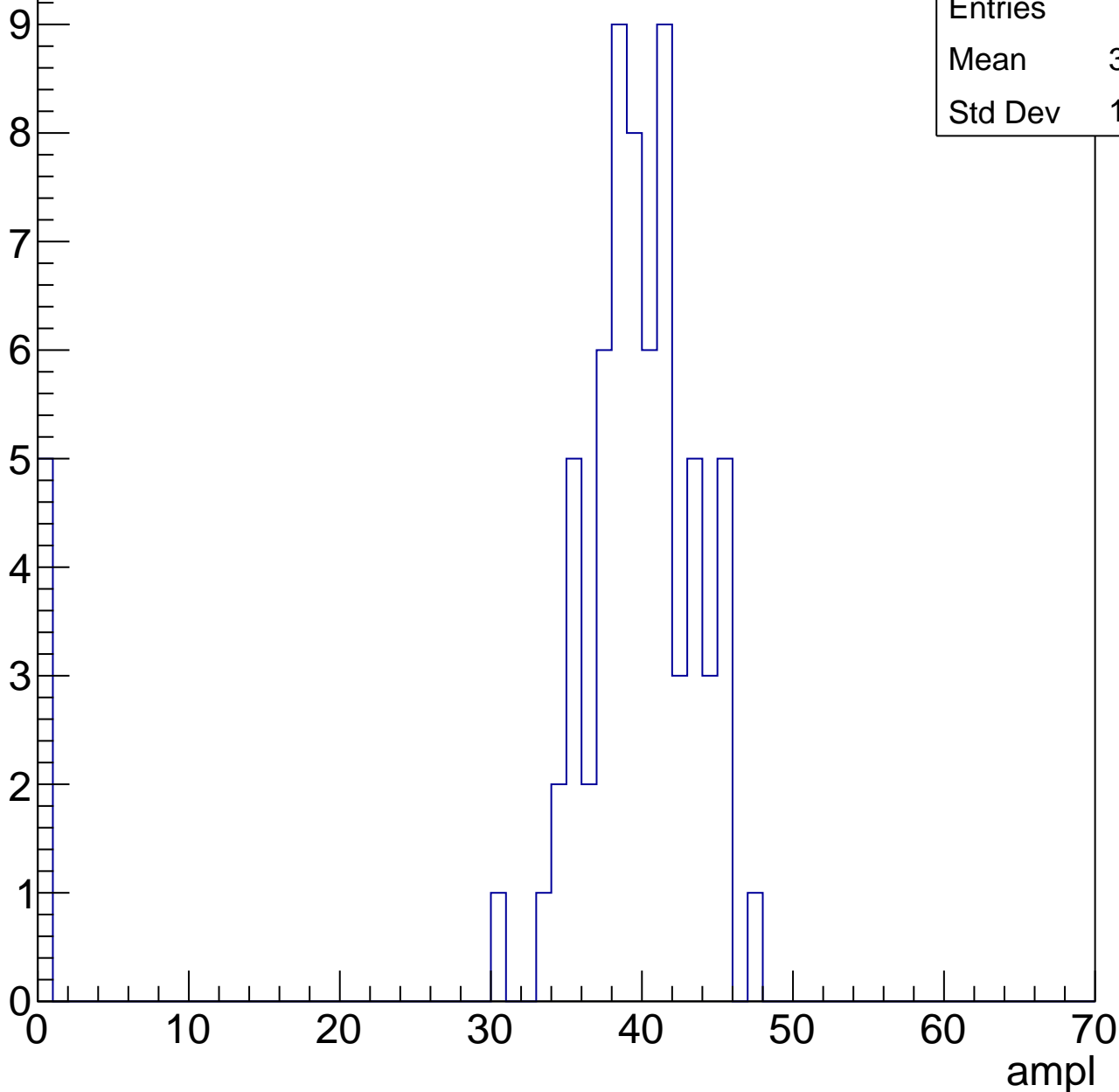


B1L103S, U5-ch28, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

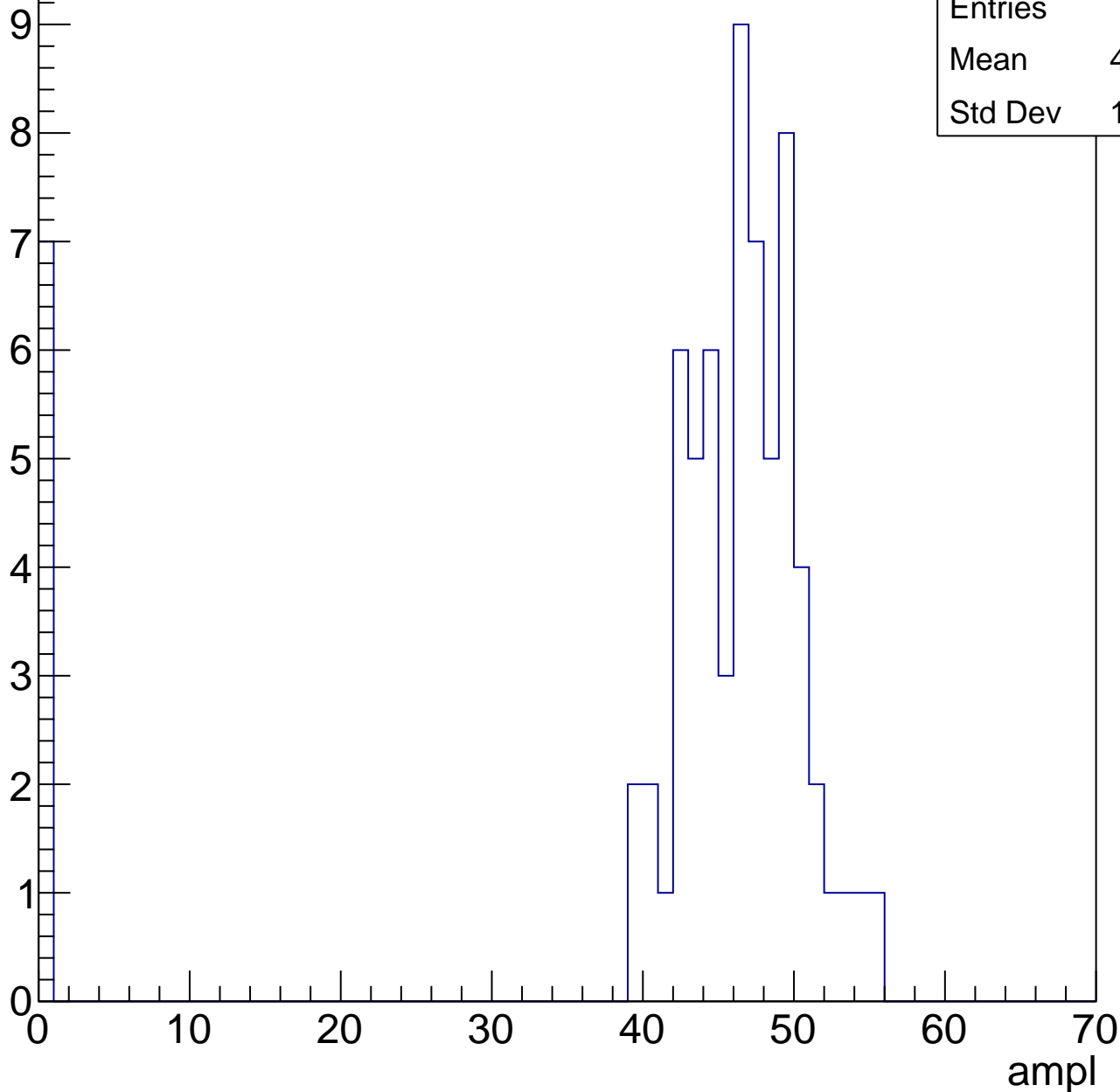
Entries	71
Mean	36.73
Std Dev	10.62



B1L103S, U5-ch28, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

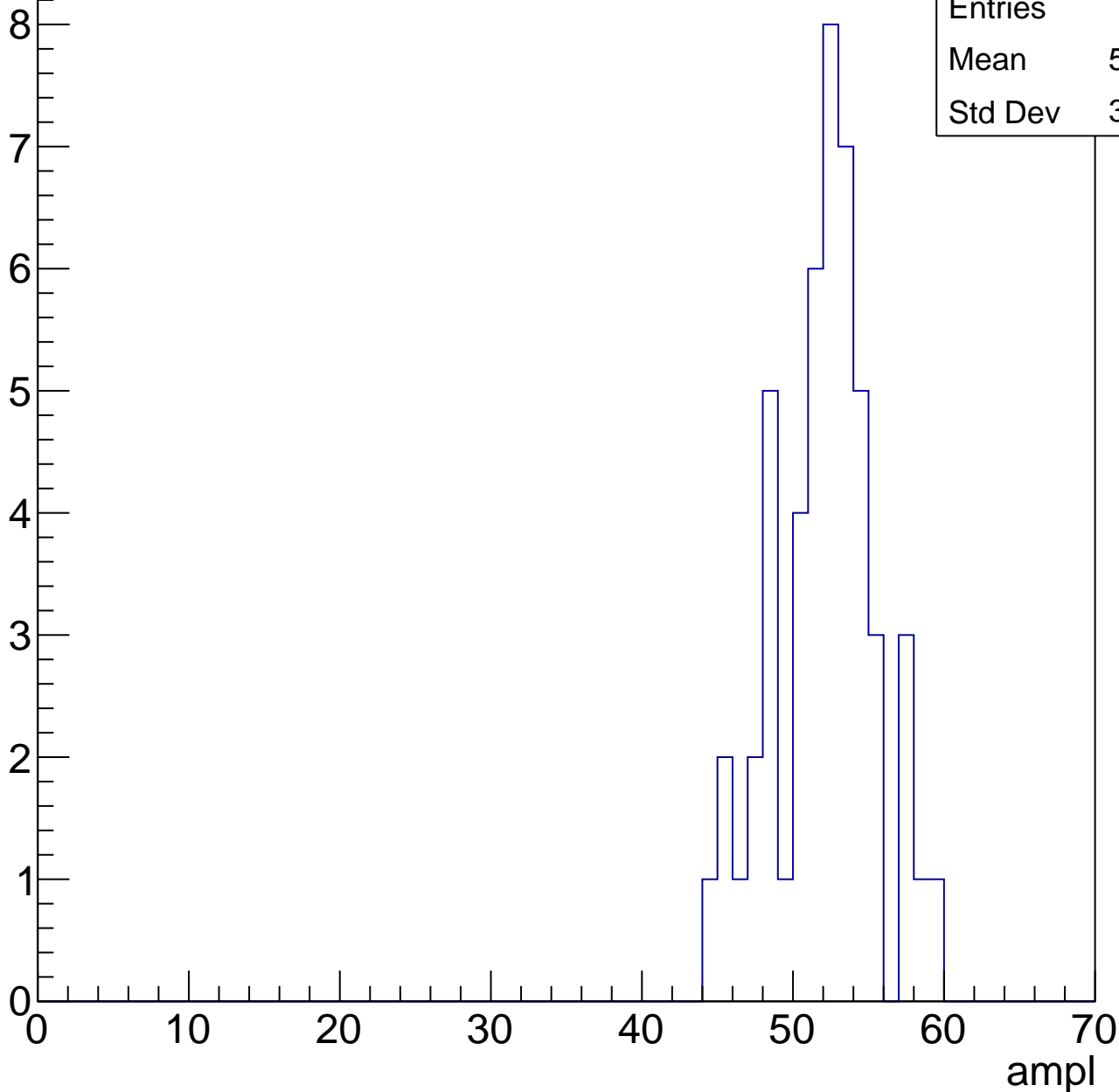


B1L103S, U5-ch28, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

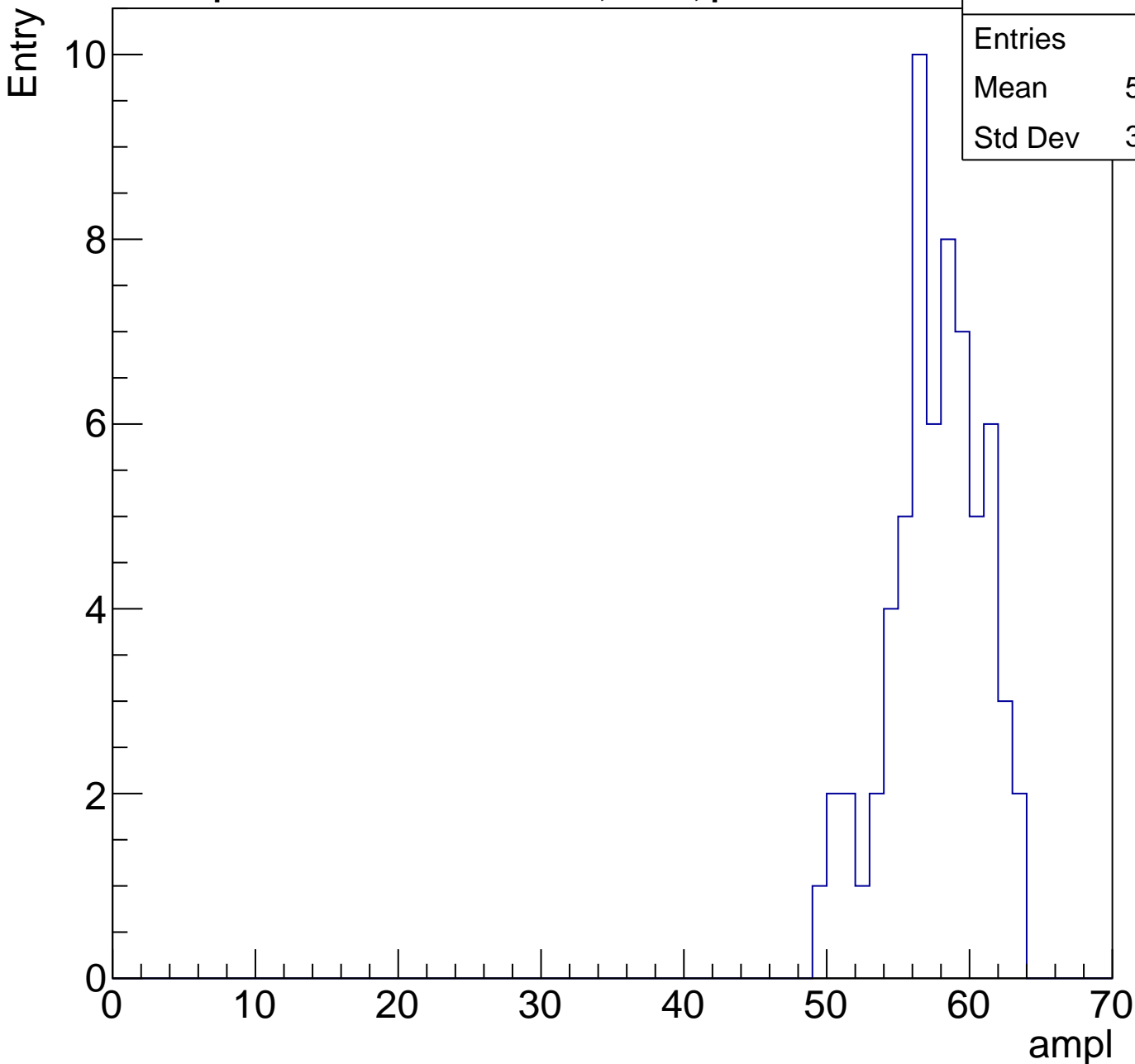
Entries	50
Mean	51.58
Std Dev	3.359



B1L103S, U5-ch28, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entries	64
Mean	57.14
Std Dev	3.259

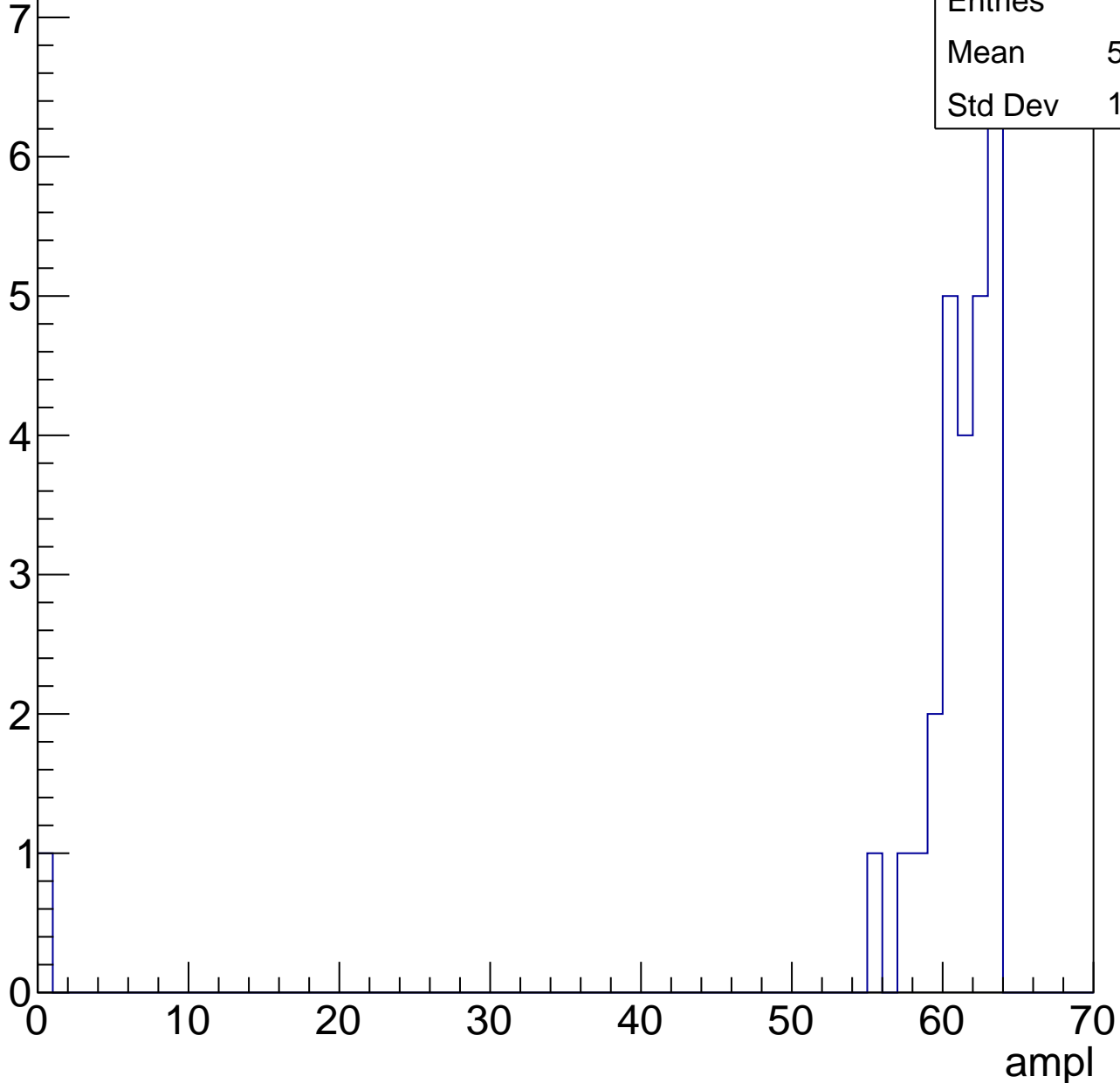


B1L103S, U5-ch28, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	27
Mean	58.63
Std Dev	11.67

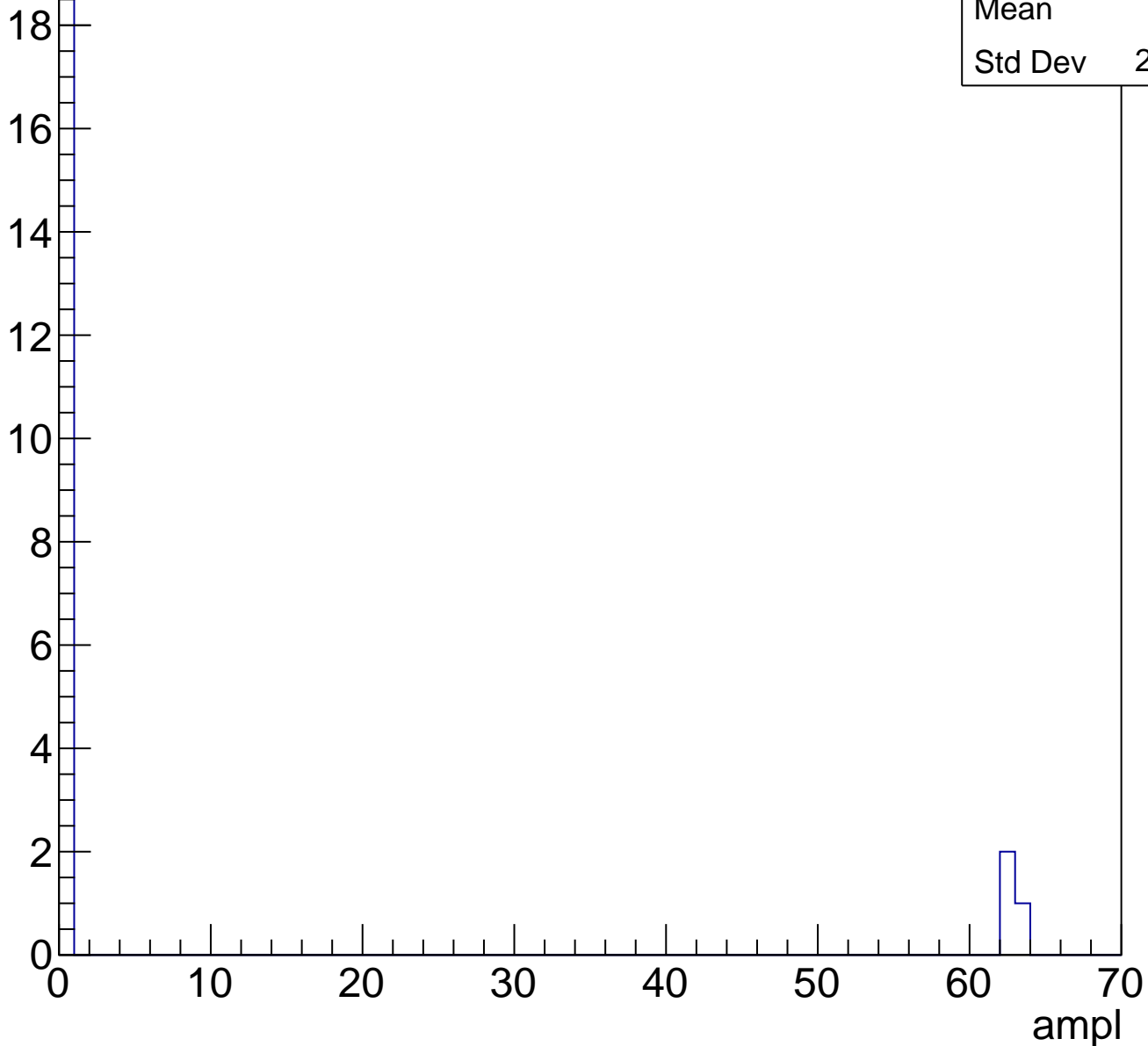


B1L103S, U5-ch28, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	22
Mean	8.5
Std Dev	21.39

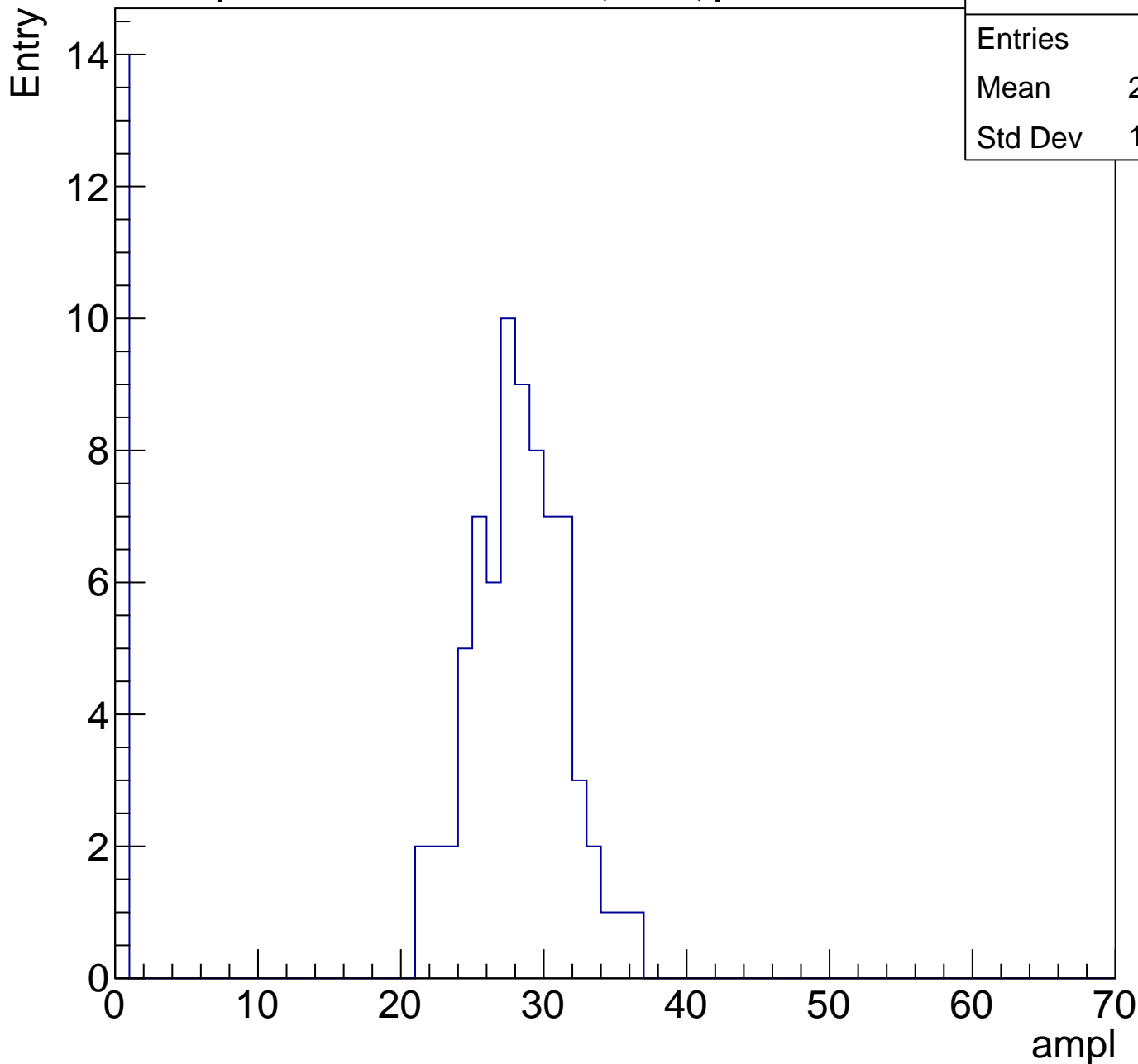
Entry



B1L103S, U5-ch29, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	87
Mean	23.34
Std Dev	10.63

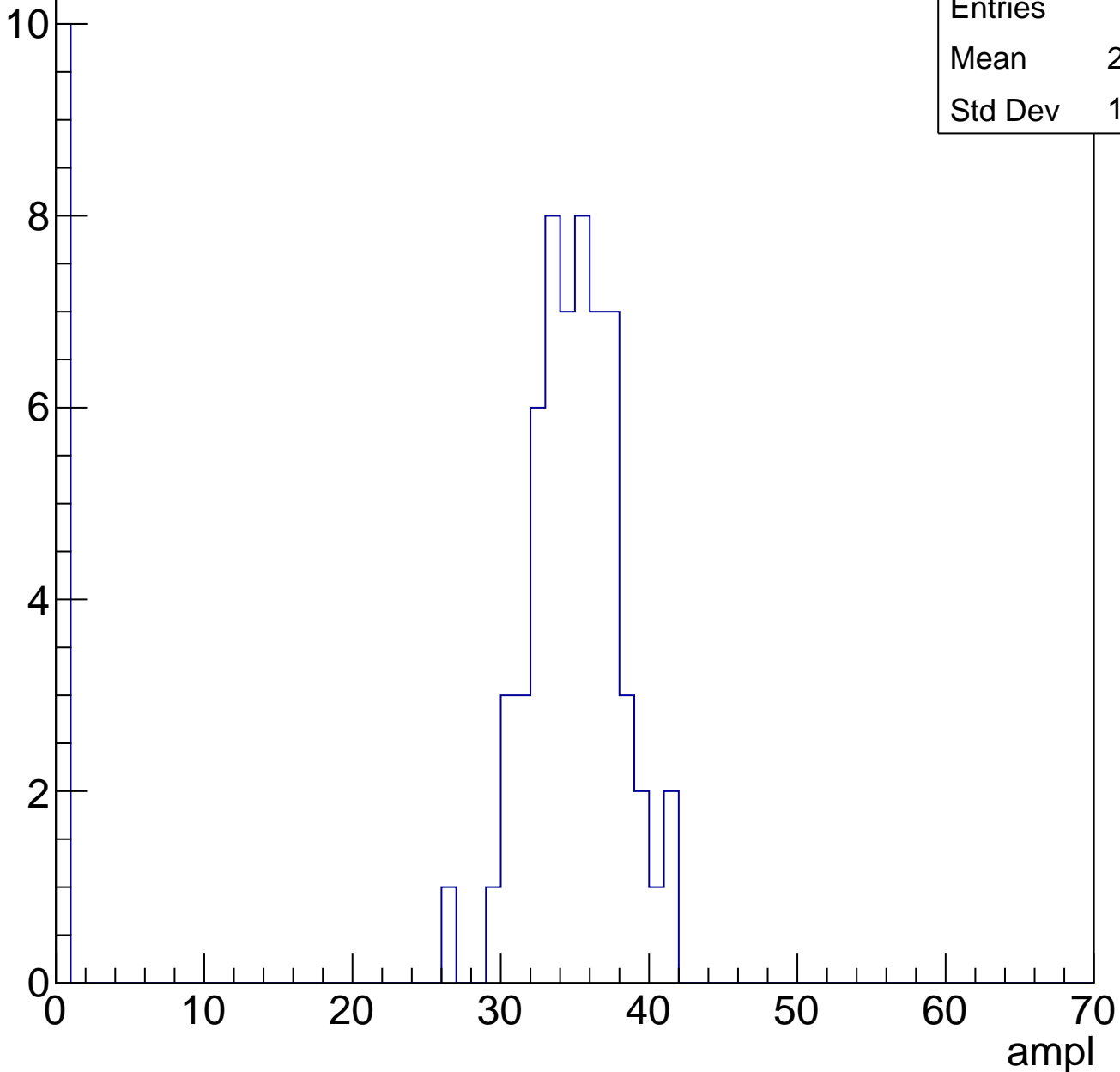


B1L103S, U5-ch29, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	69
Mean	29.52
Std Dev	12.45

Entry

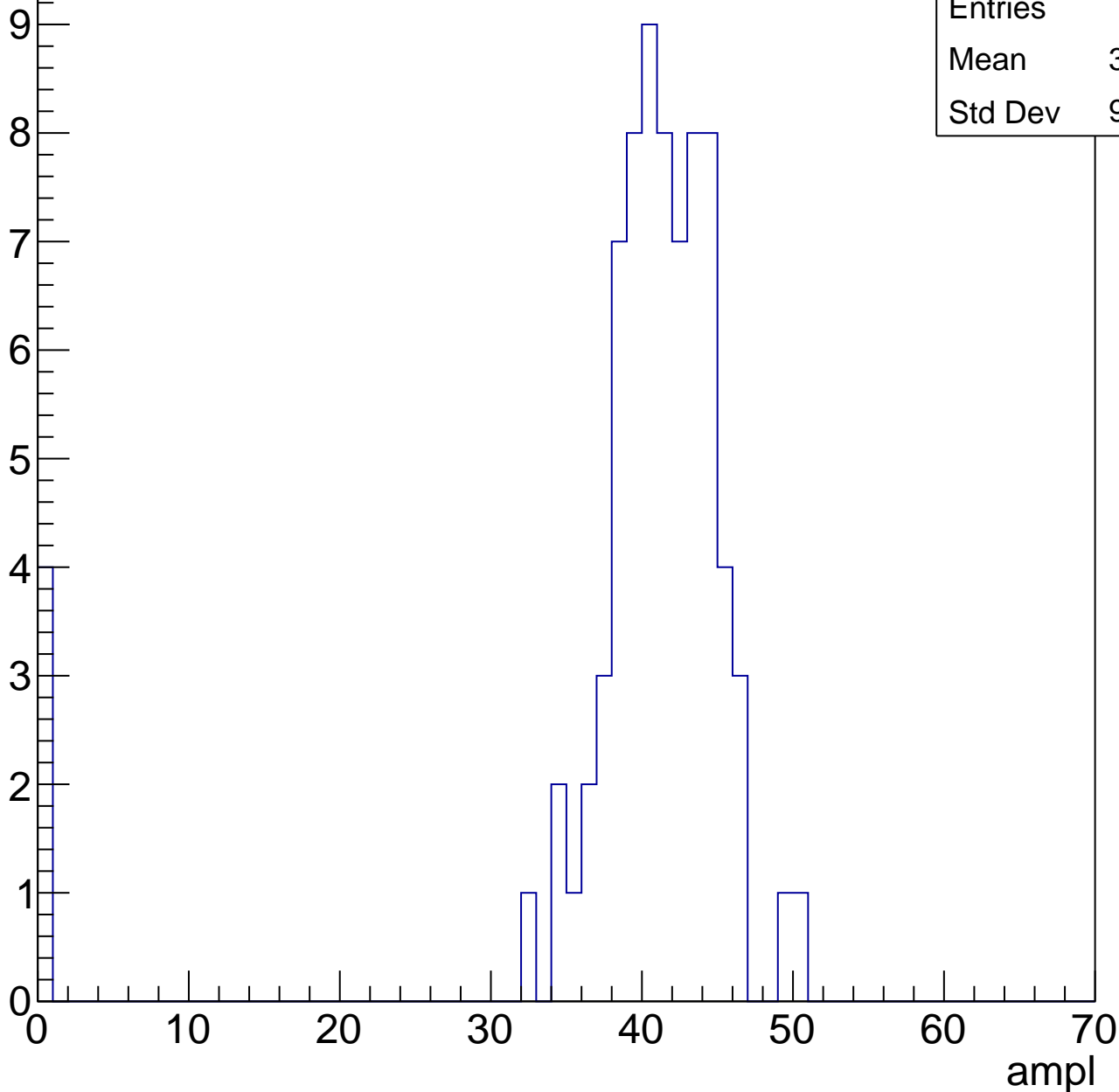


B1L103S, U5-ch29, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	38.84
Std Dev	9.655

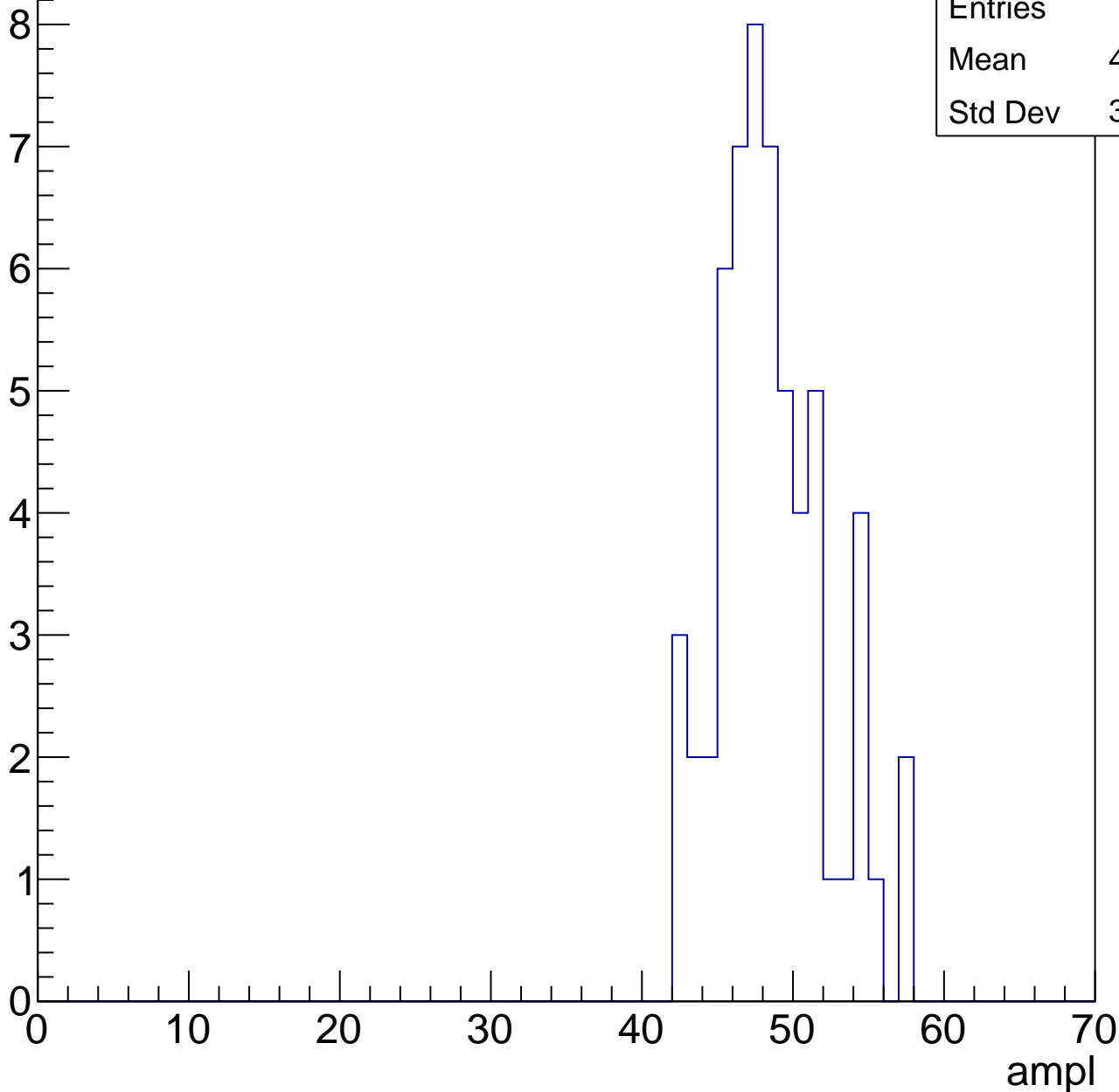


B1L103S, U5-ch29, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	48.17
Std Dev	3.573

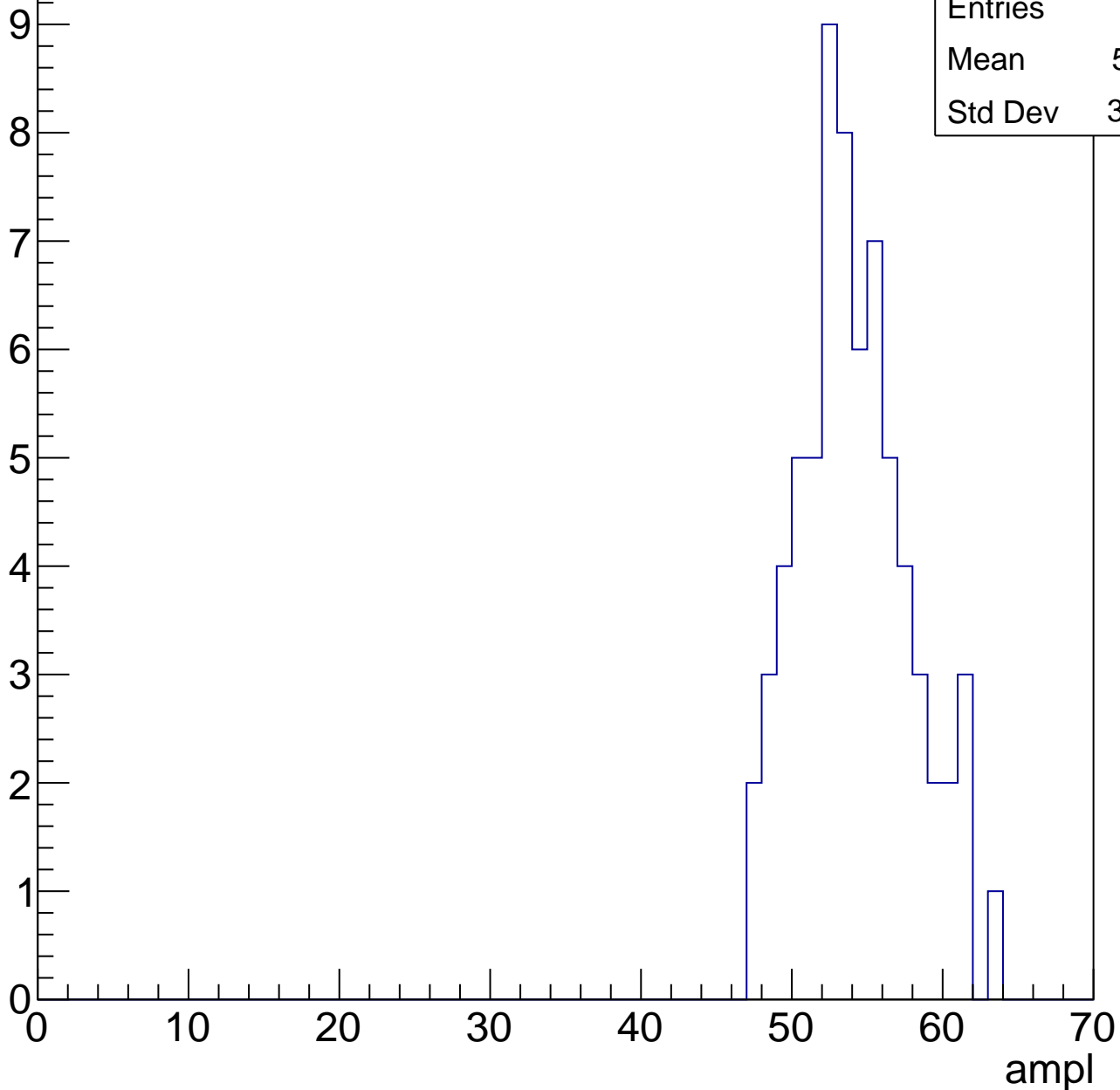


B1L103S, U5-ch29, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	53.71
Std Dev	3.672

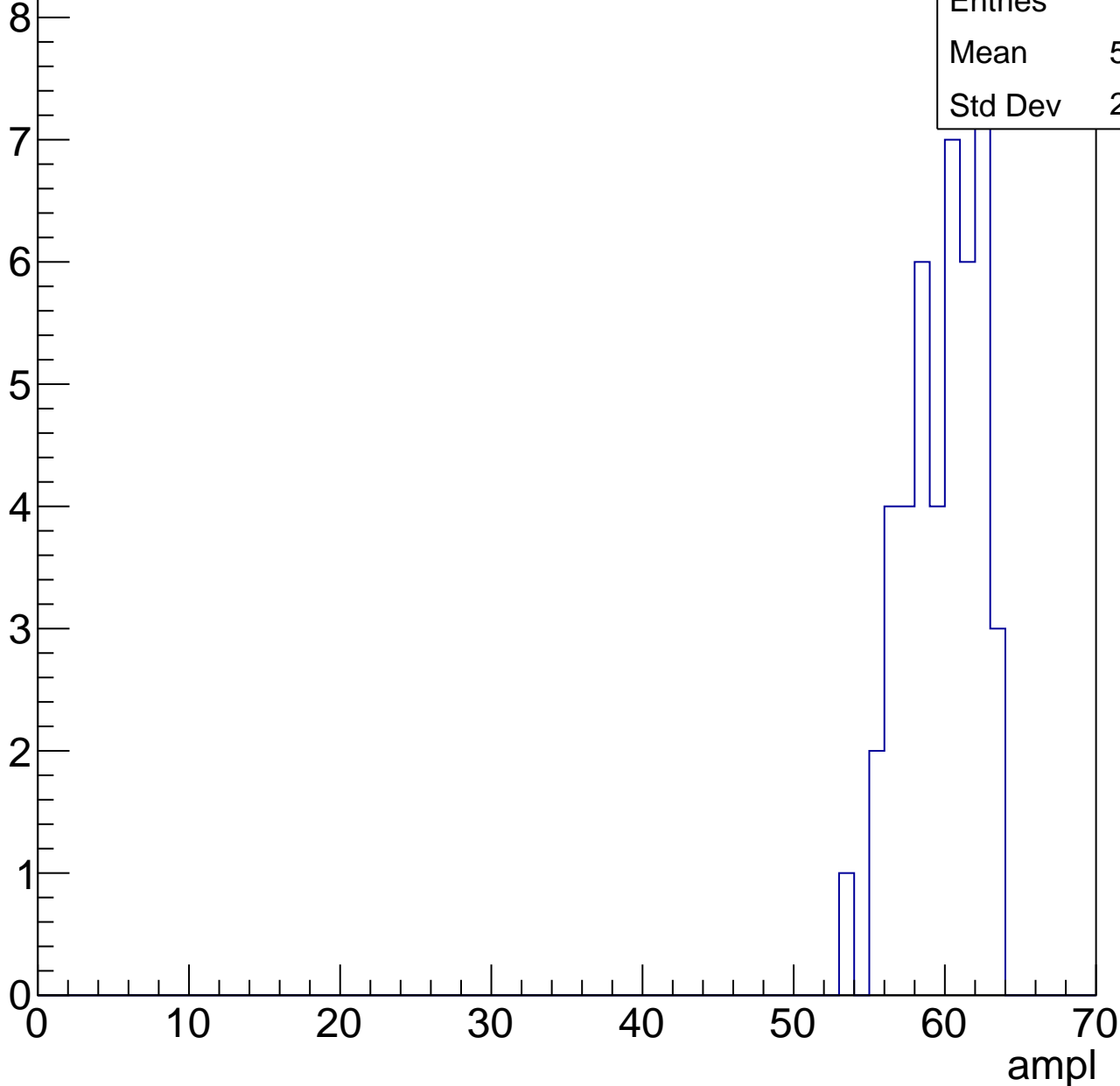


B1L103S, U5-ch29, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	45
Mean	59.33
Std Dev	2.459

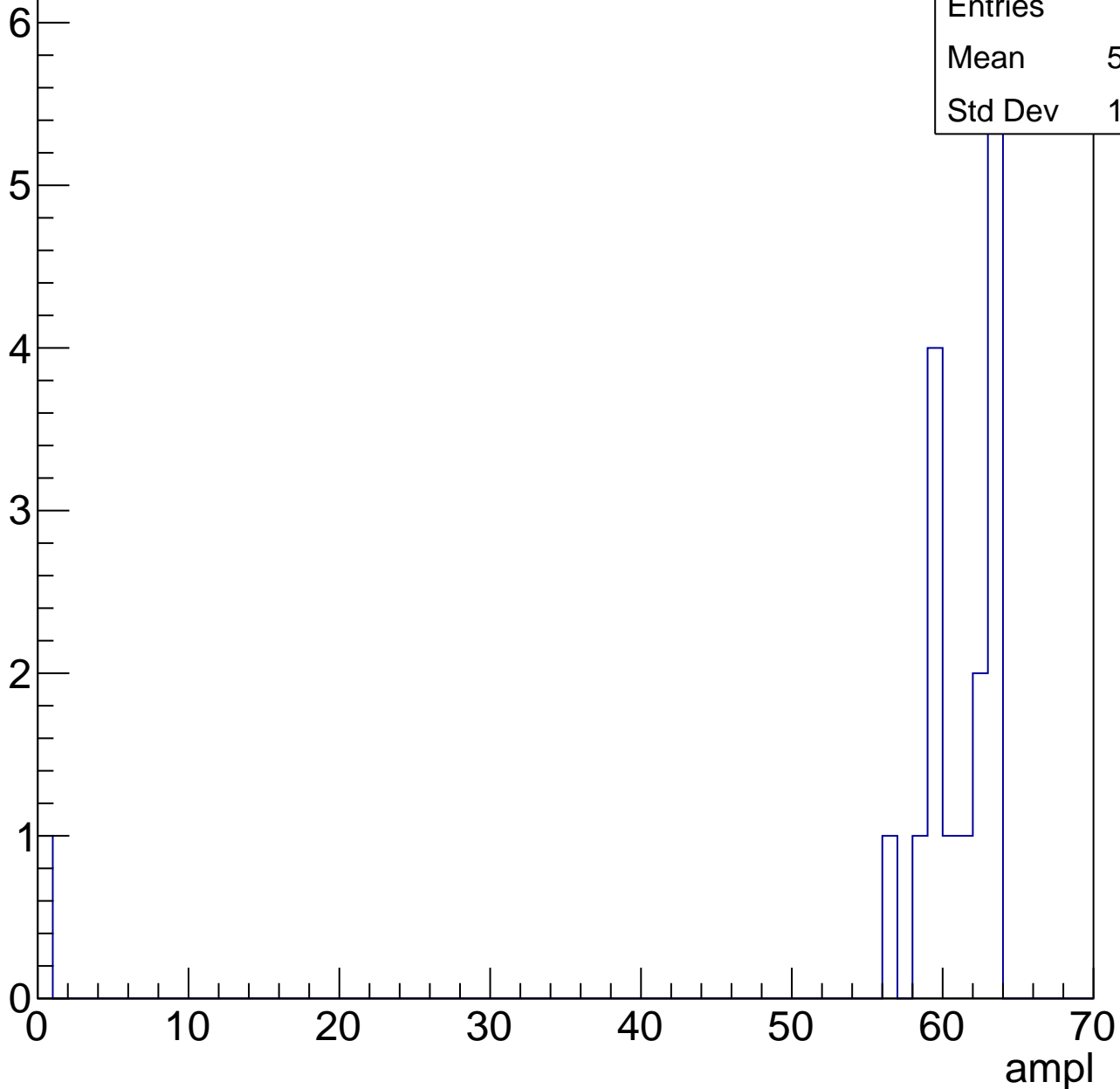


B1L103S, U5-ch29, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	17
Mean	57.24
Std Dev	14.47



B1L103S, U5-ch29, adc7

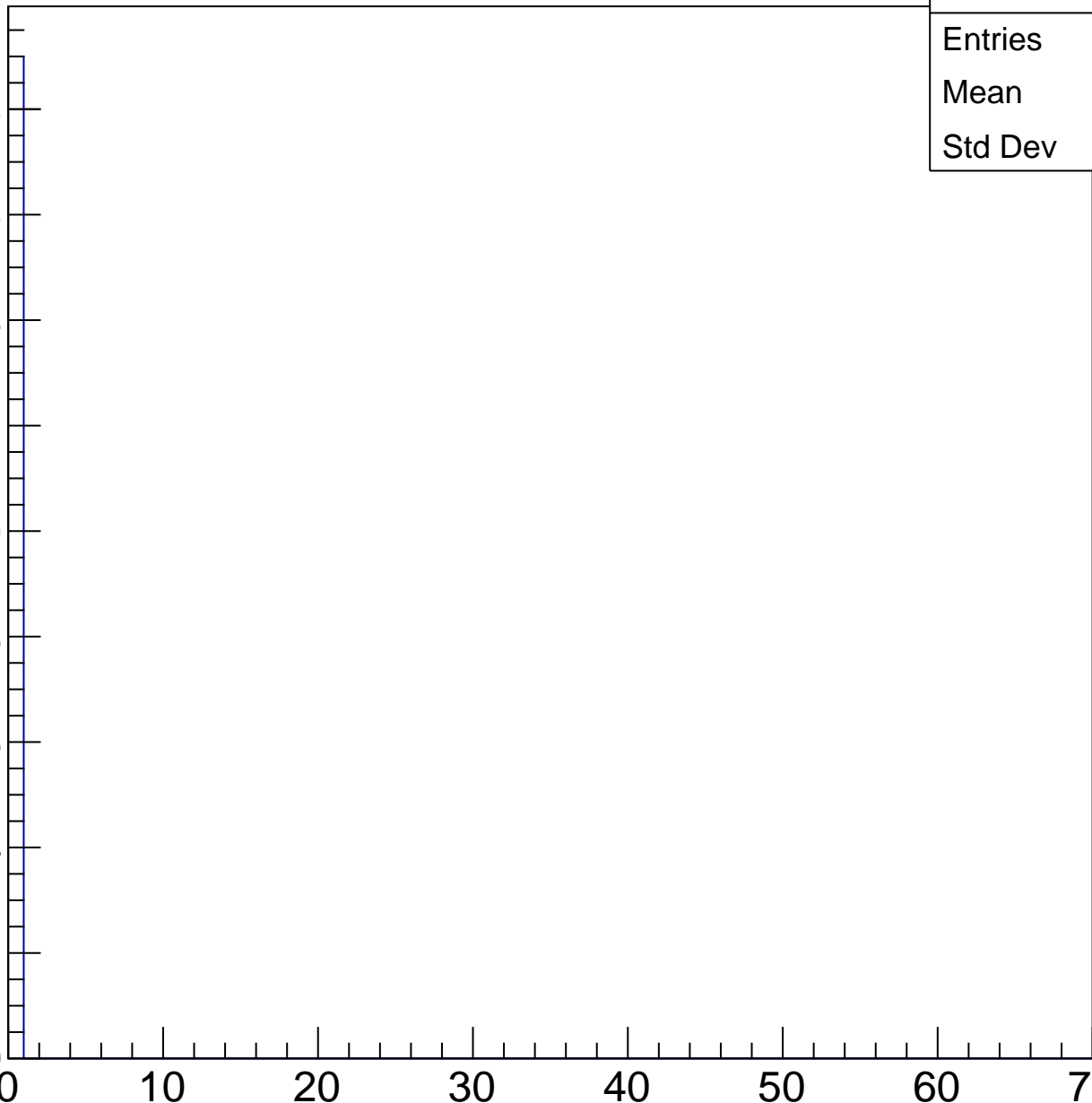
calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

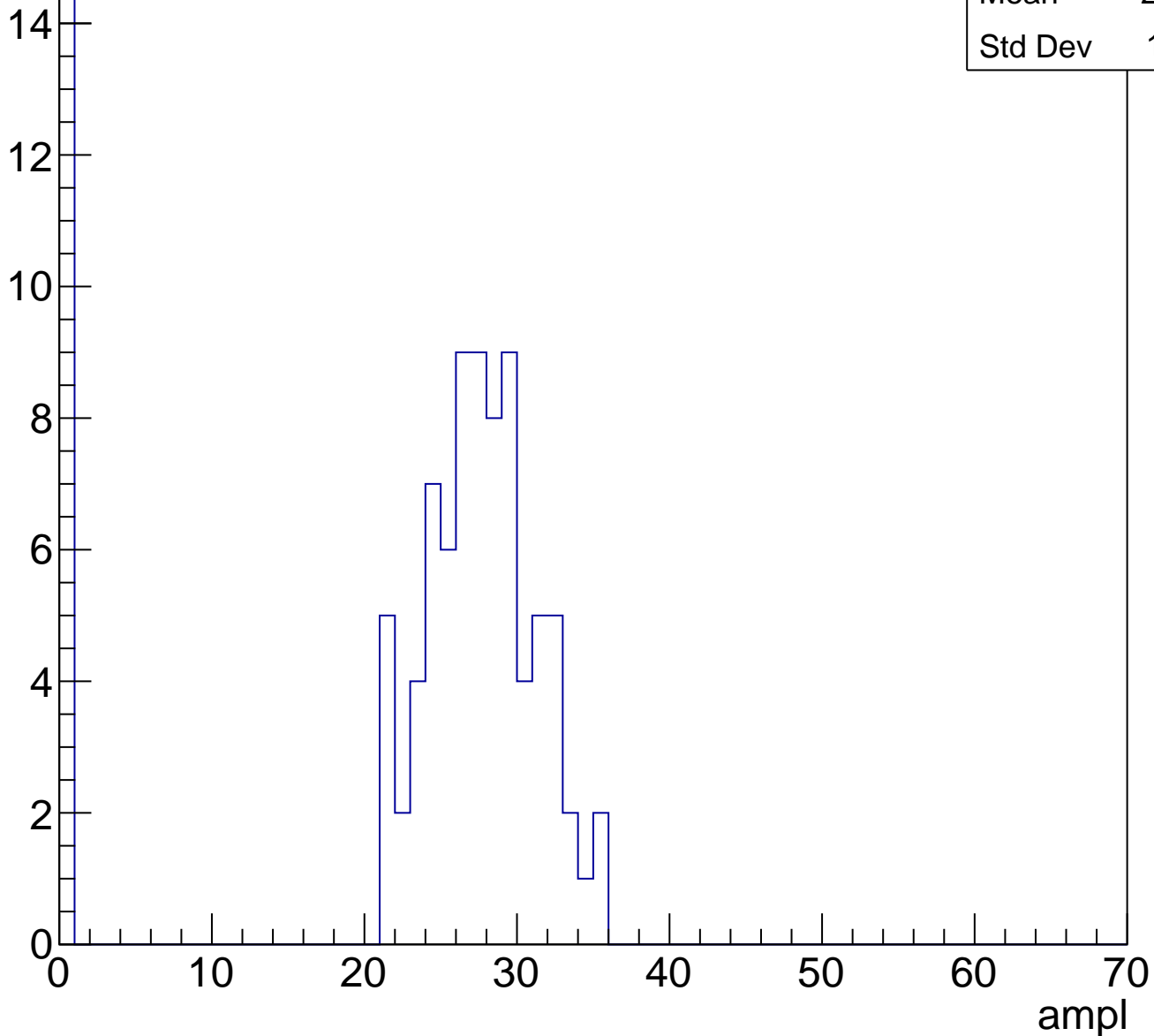


B1L103S, U5-ch30, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	93
Mean	22.86
Std Dev	10.51

Entry



B1L103S, U5-ch30, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	76
Mean	28.55
Std Dev	13.29

Entry

12

10

8

6

4

2

0

0

10

20

30

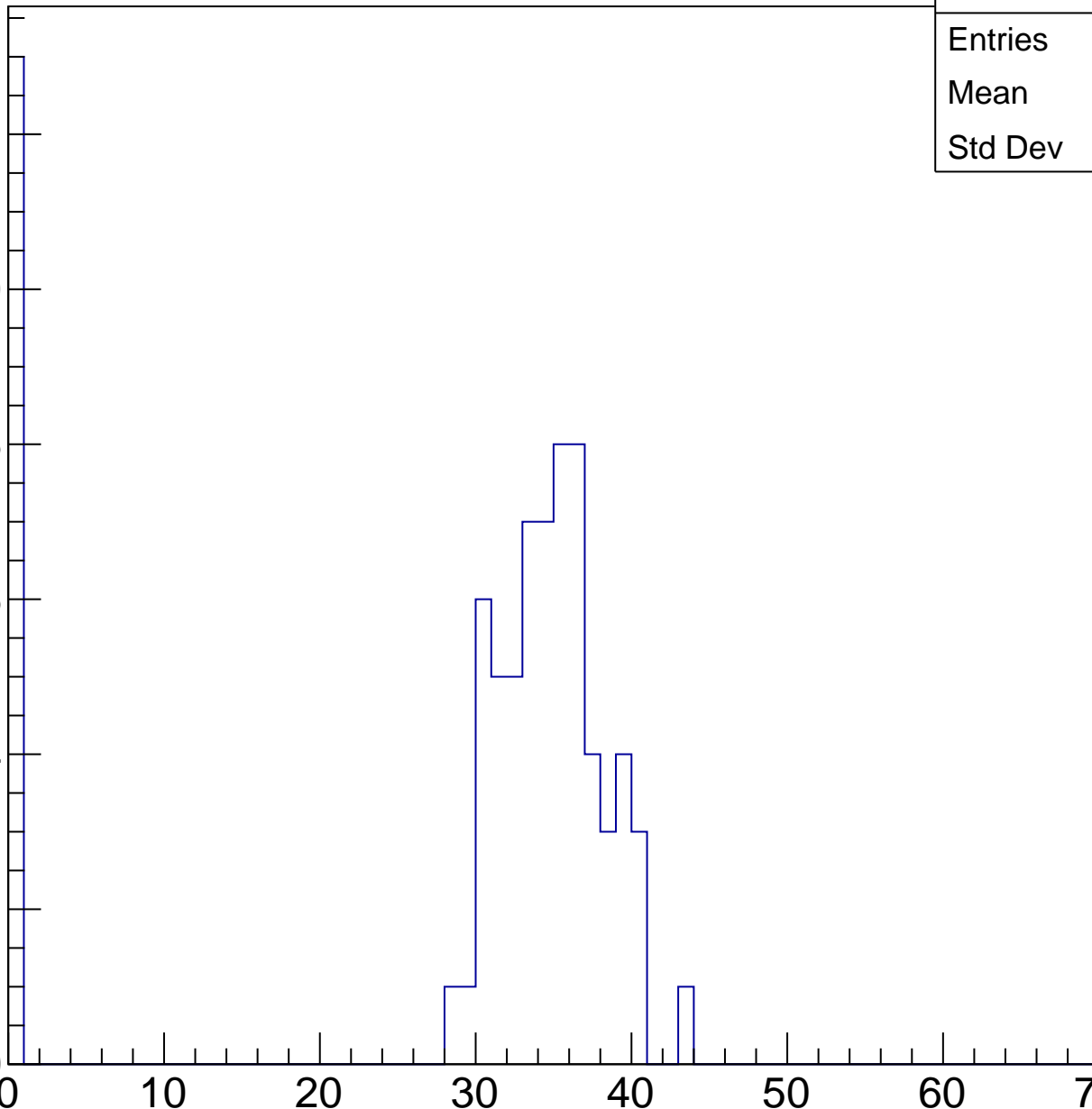
40

50

60

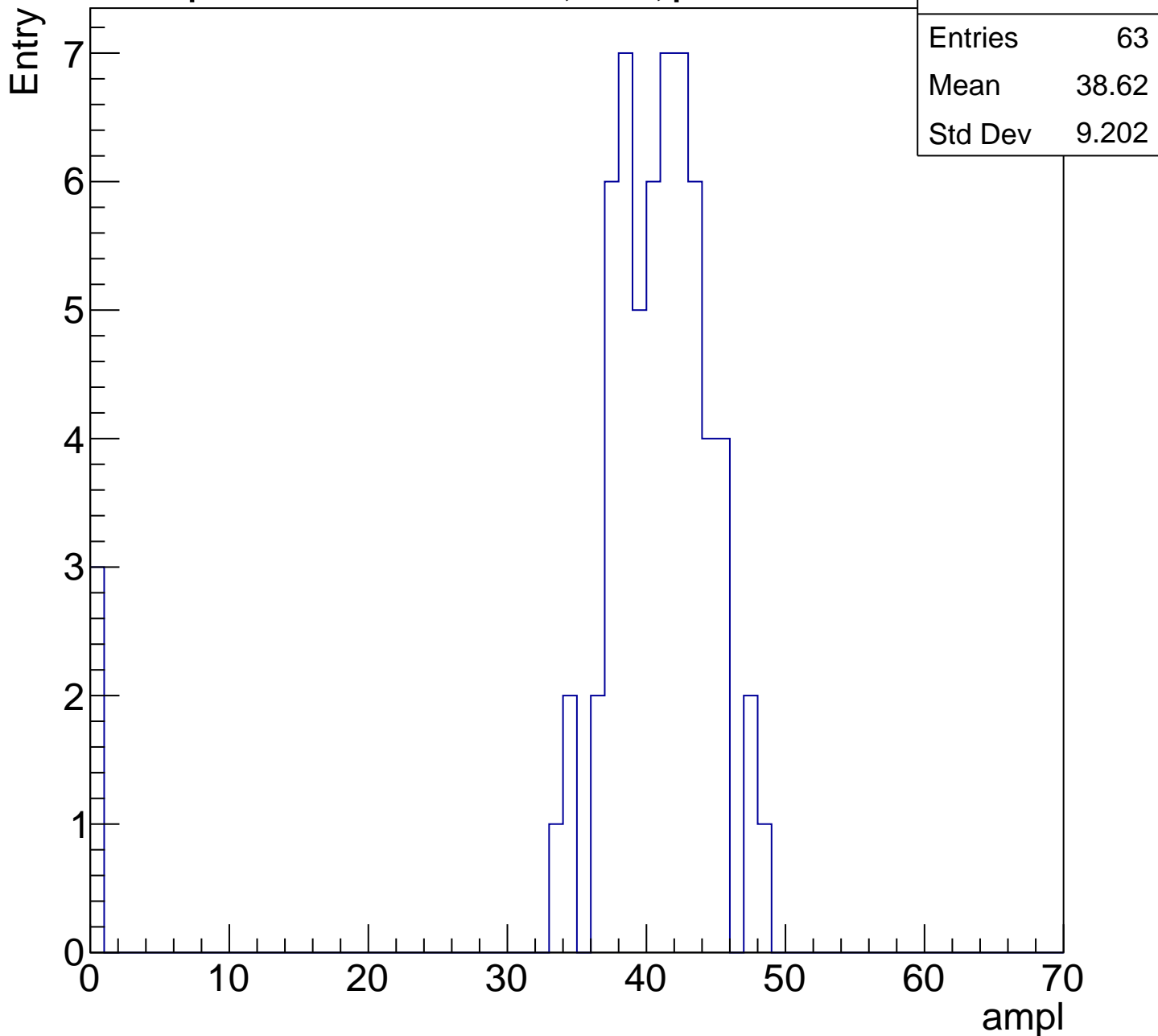
70

ampl



B1L103S, U5-ch30, adc2

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U5-ch30, adc3

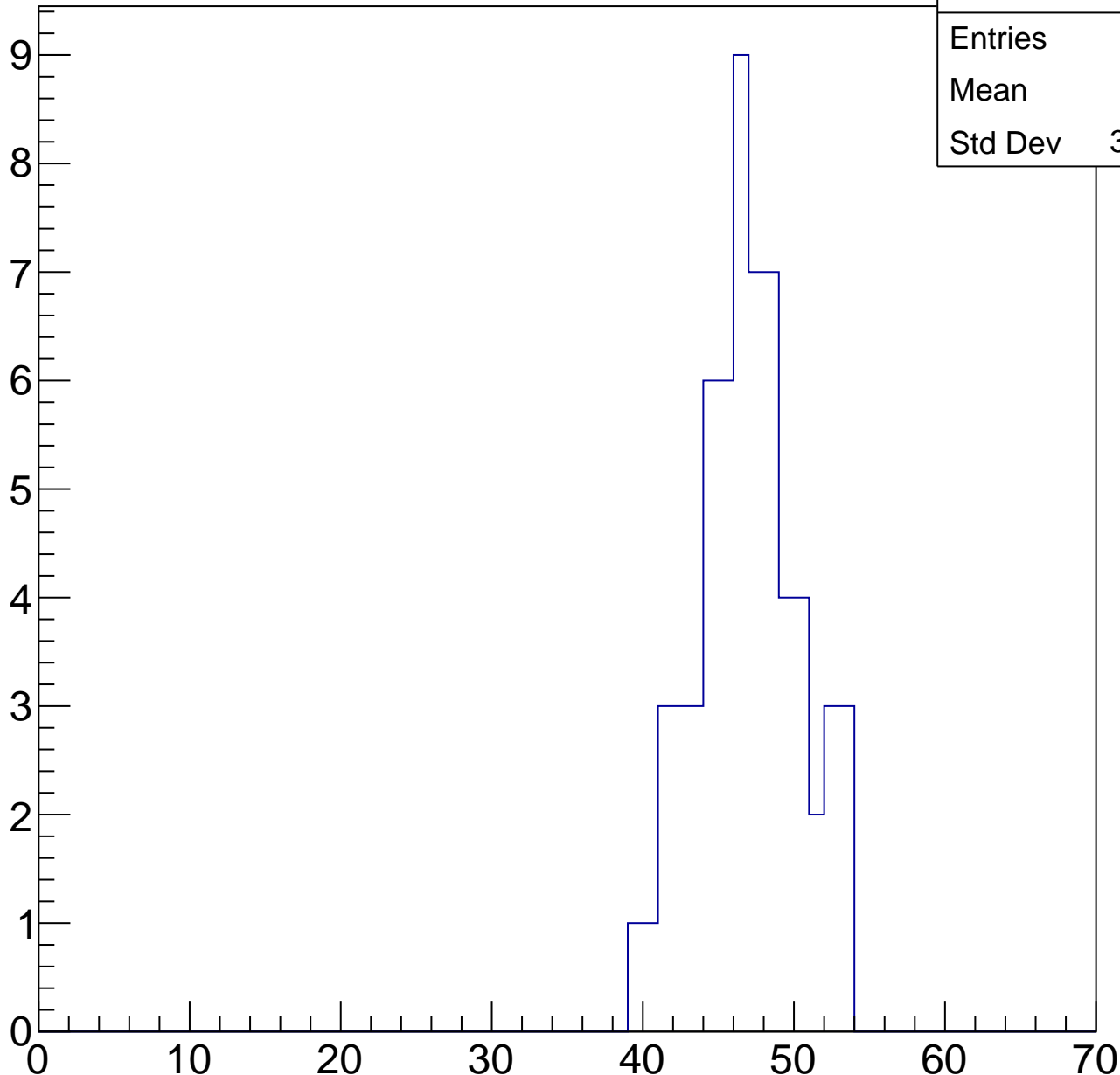
calib_packv5_041523_1651.root, FC#0, port C2

Entry

9
8
7
6
5
4
3
2
1
0

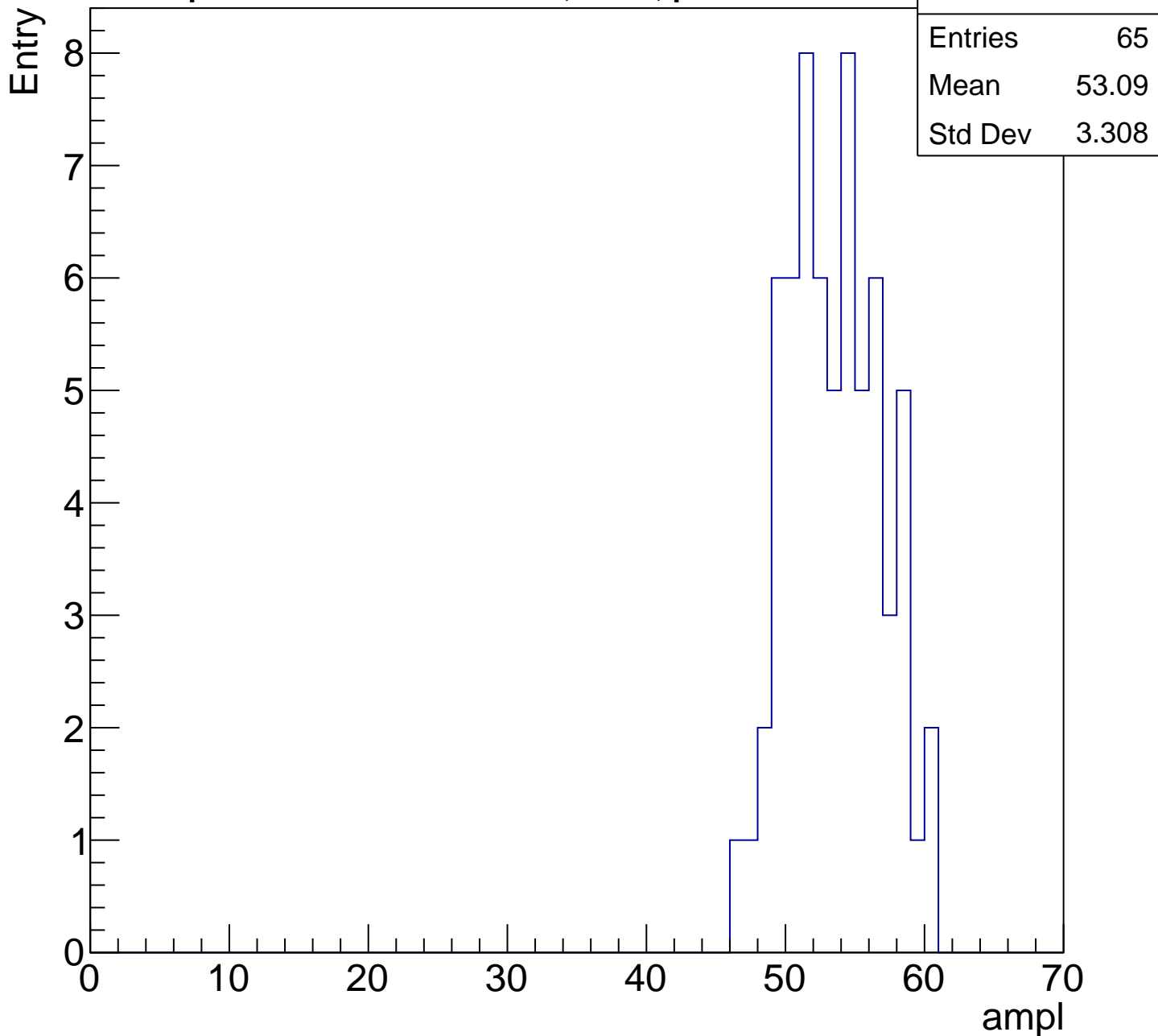
Entries	62
Mean	46.5
Std Dev	3.335

ampl



B1L103S, U5-ch30, adc4

calib_packv5_041523_1651.root, FC#0, port C2

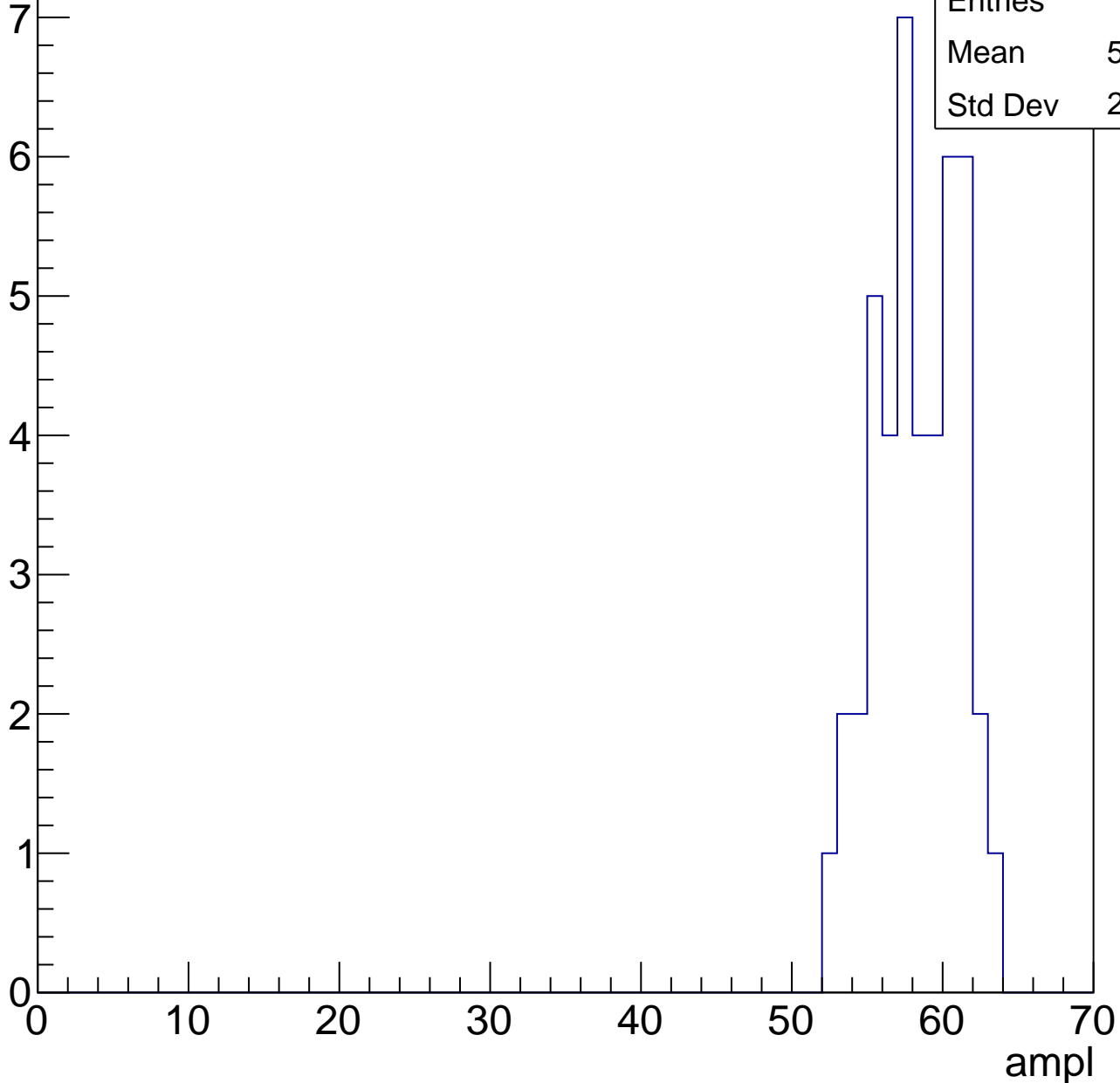


B1L103S, U5-ch30, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	44
Mean	57.84
Std Dev	2.713

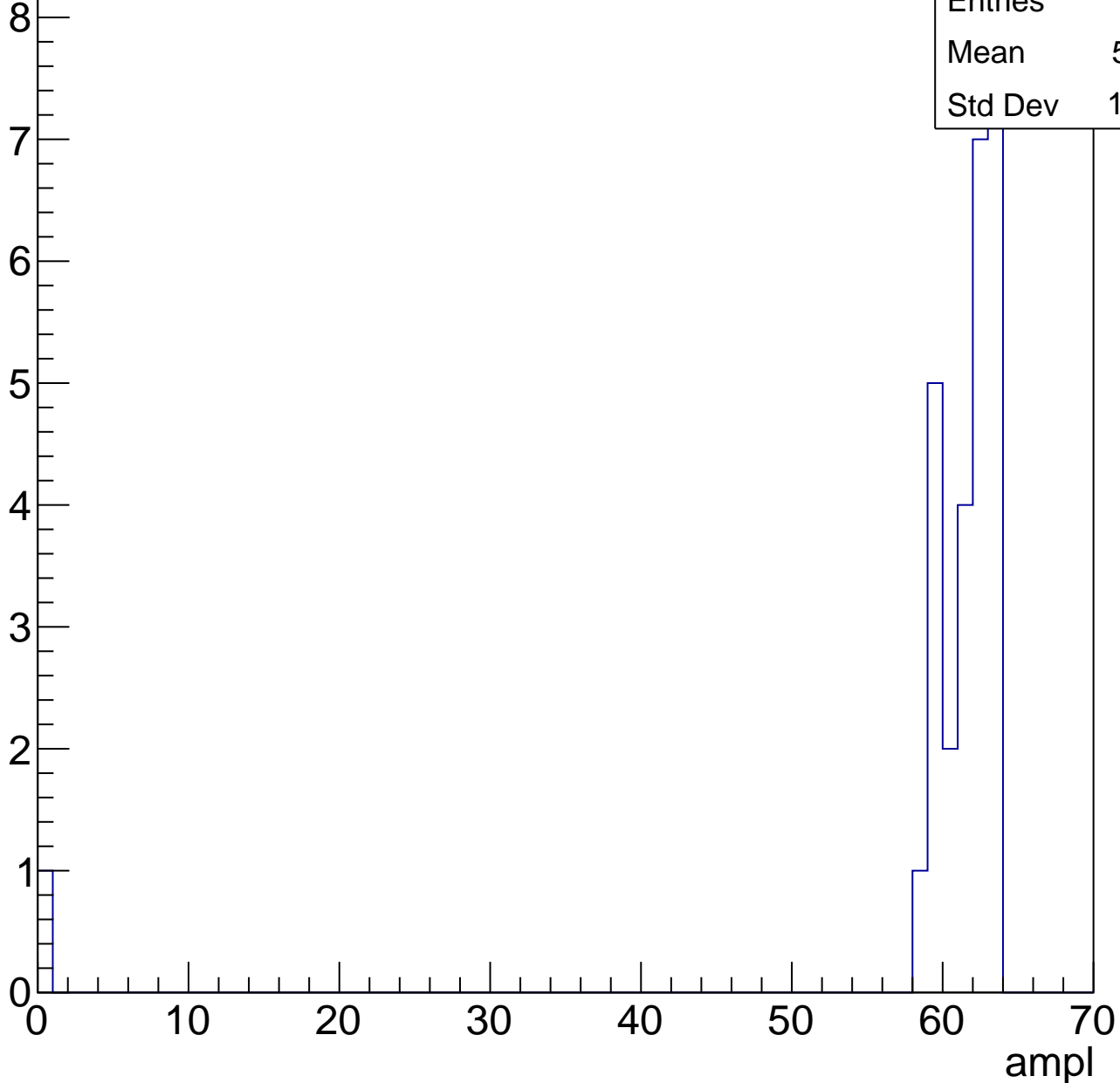


B1L103S, U5-ch30, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

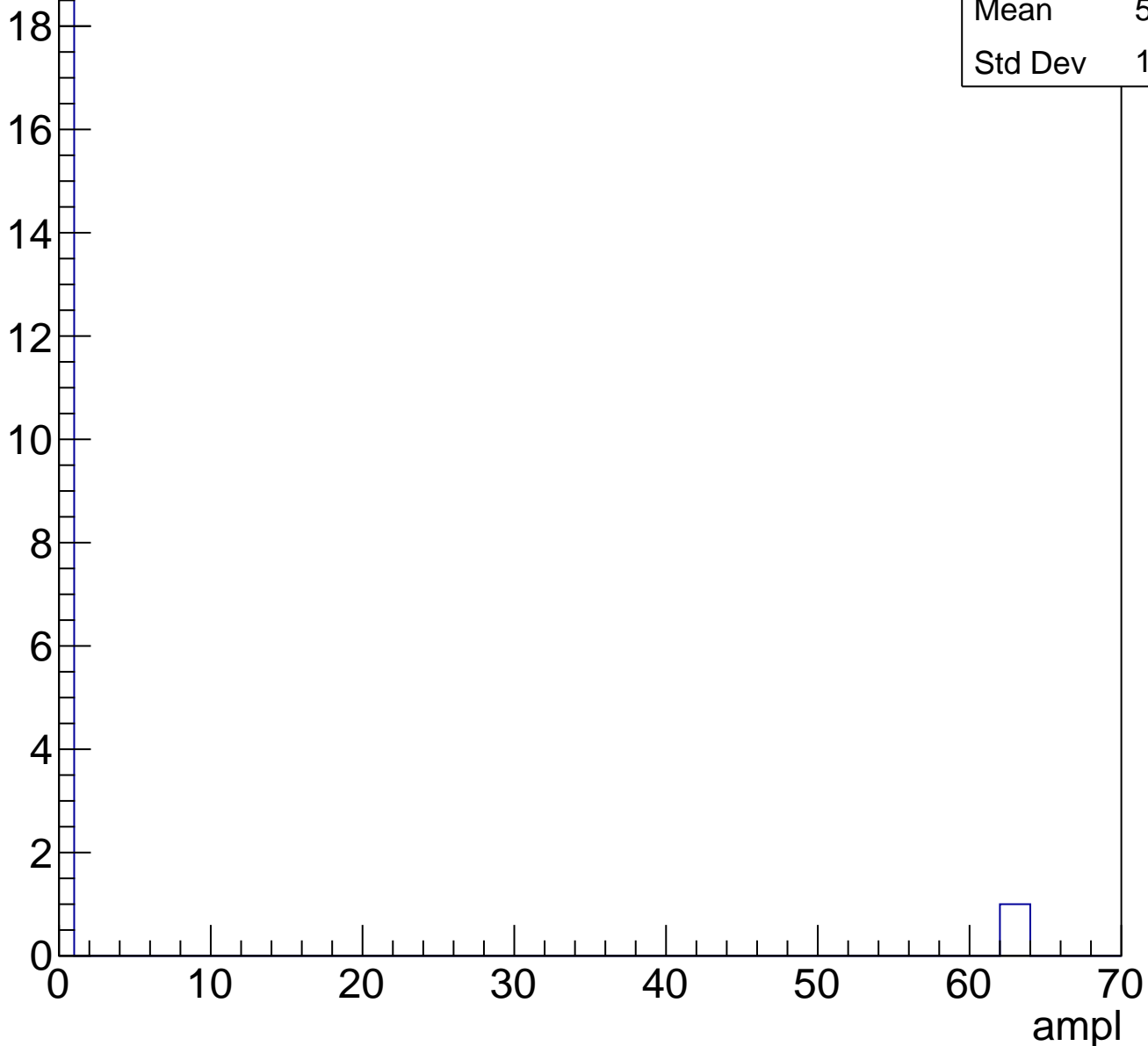
Entries	28
Mean	59.11
Std Dev	11.48



B1L103S, U5-ch30, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



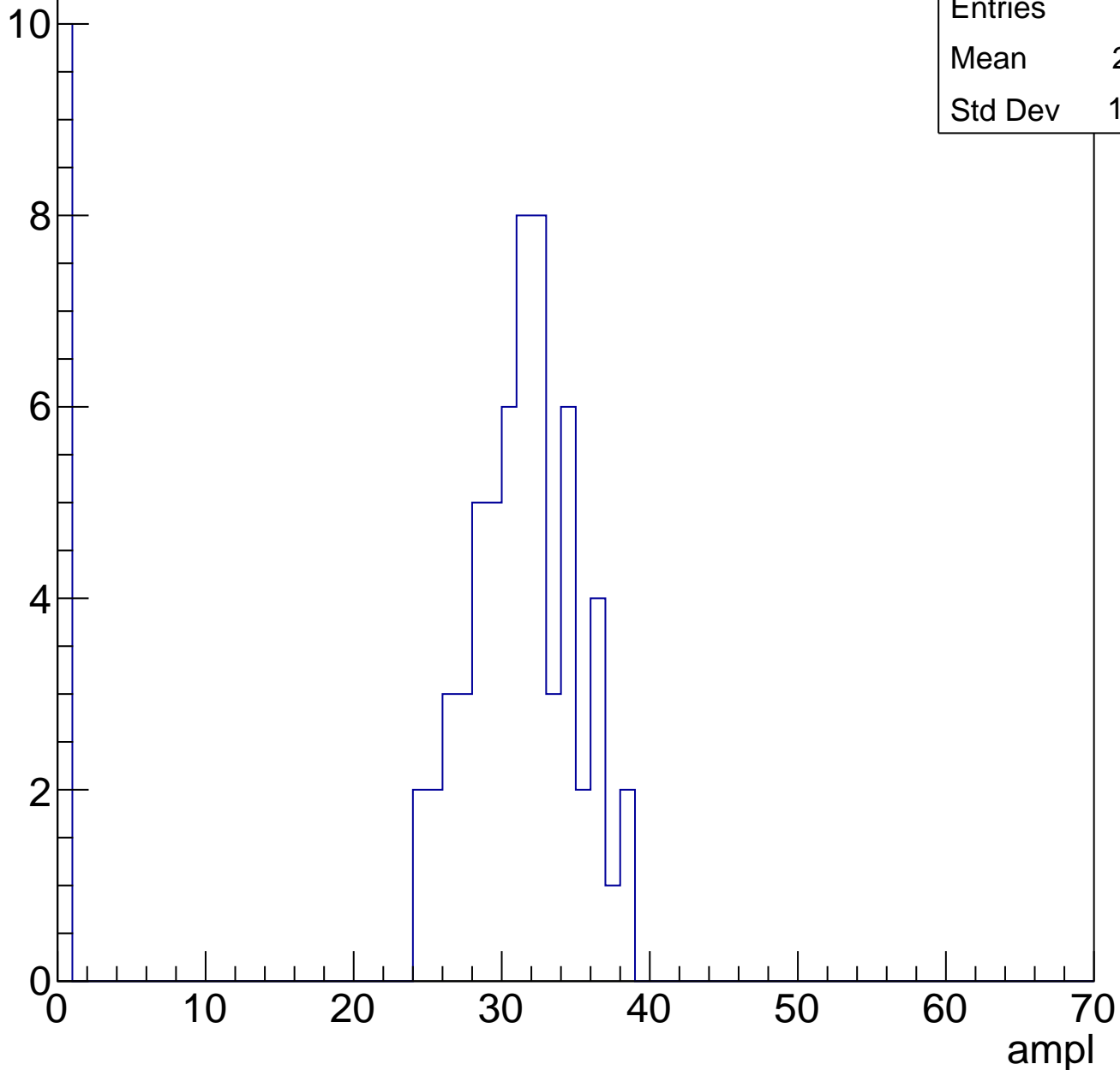
Entries	21
Mean	5.952
Std Dev	18.35

B1L103S, U5-ch31, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	70
Mean	26.51
Std Dev	11.28

Entry

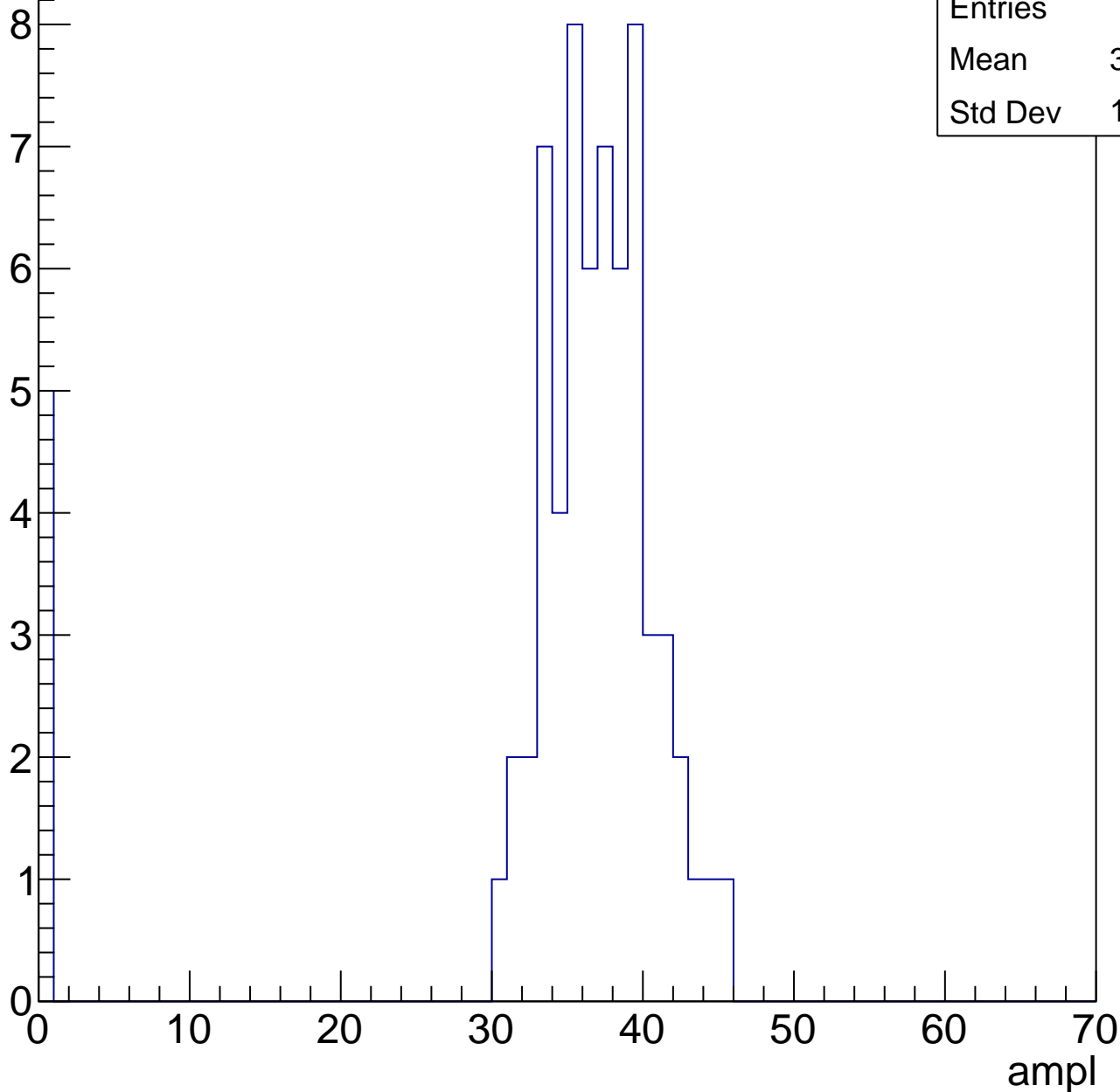


B1L103S, U5-ch31, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	33.99
Std Dev	10.15

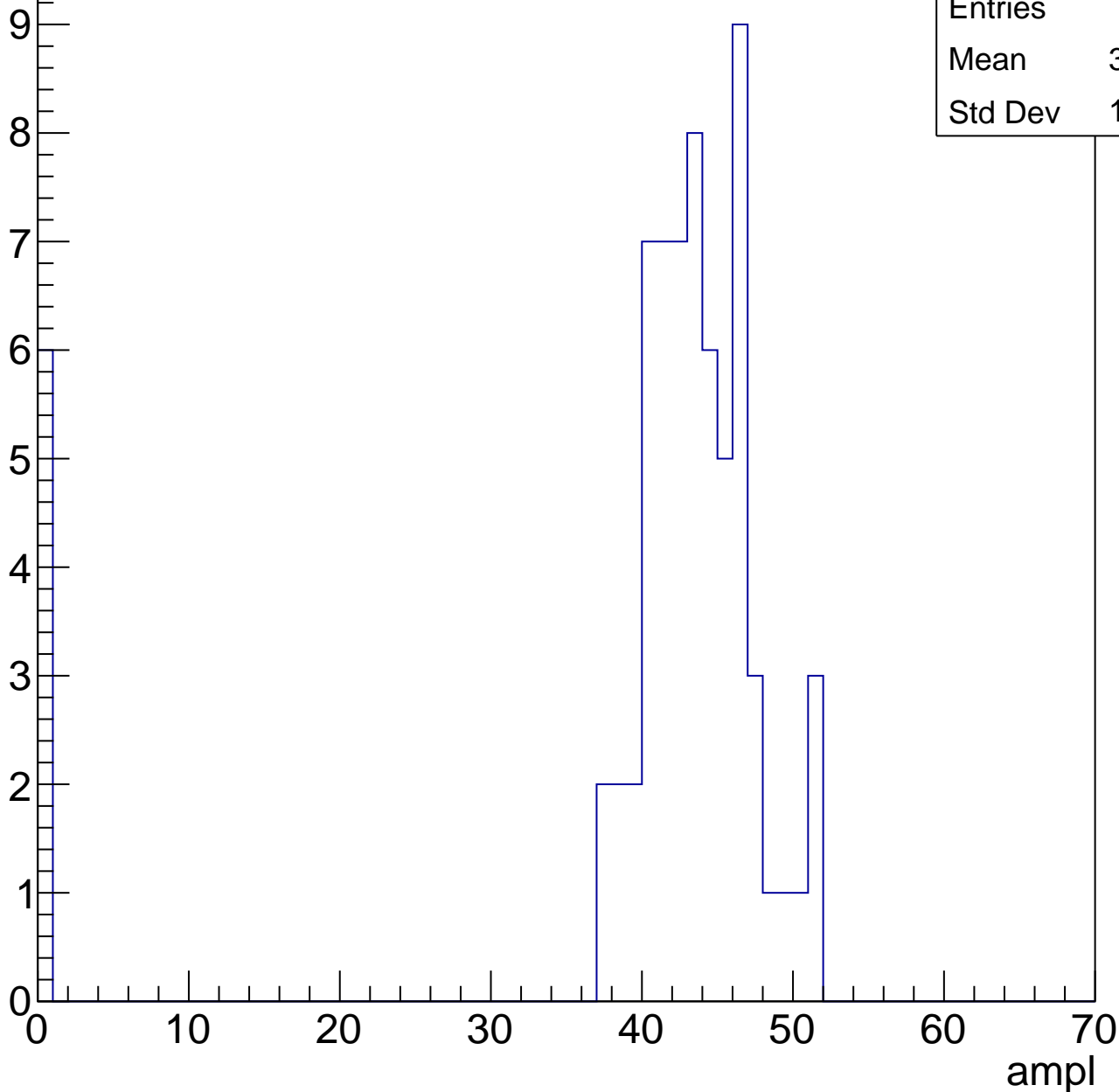


B1L103S, U5-ch31, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	39.67
Std Dev	12.55

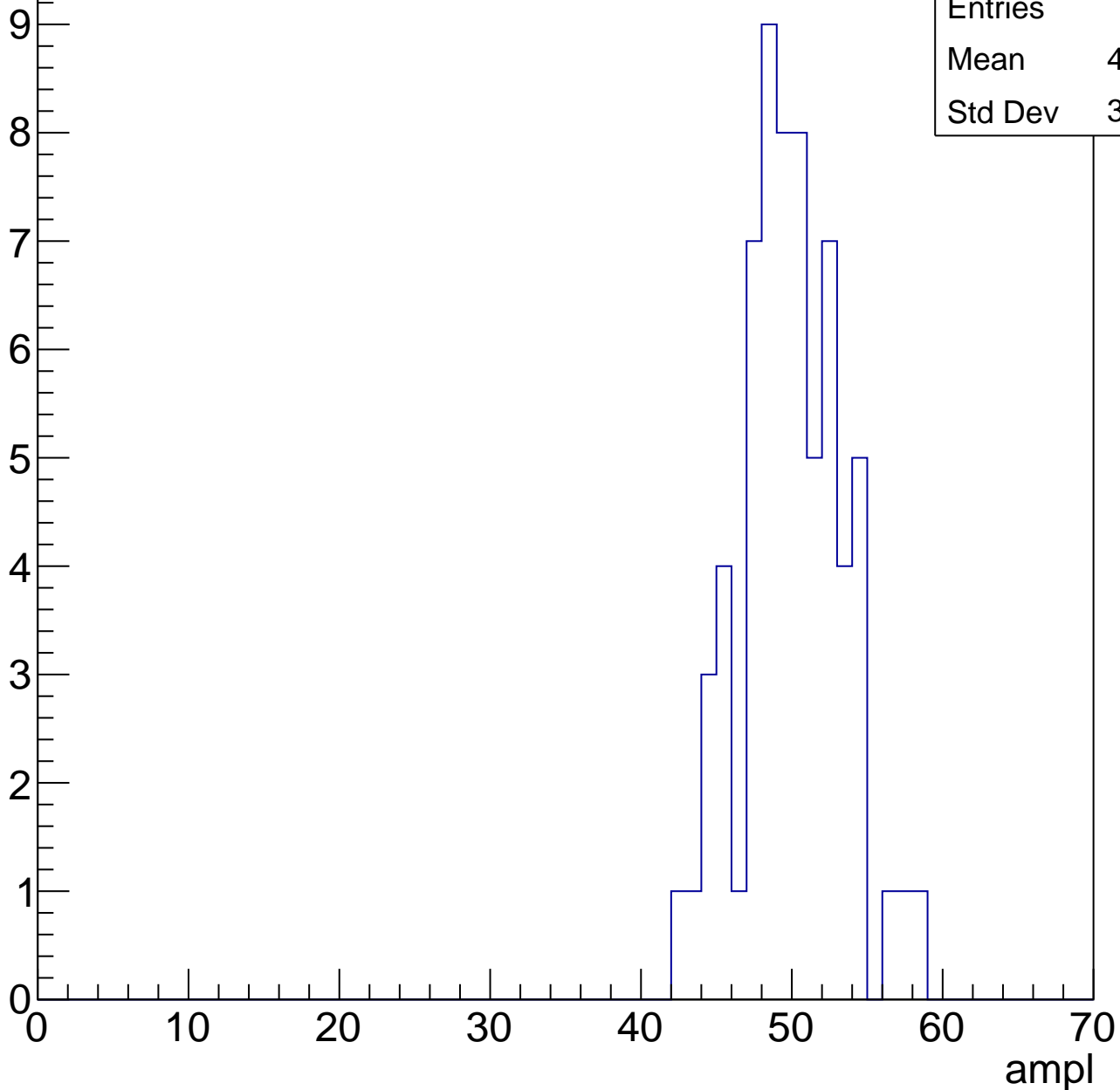


B1L103S, U5-ch31, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	49.52
Std Dev	3.318

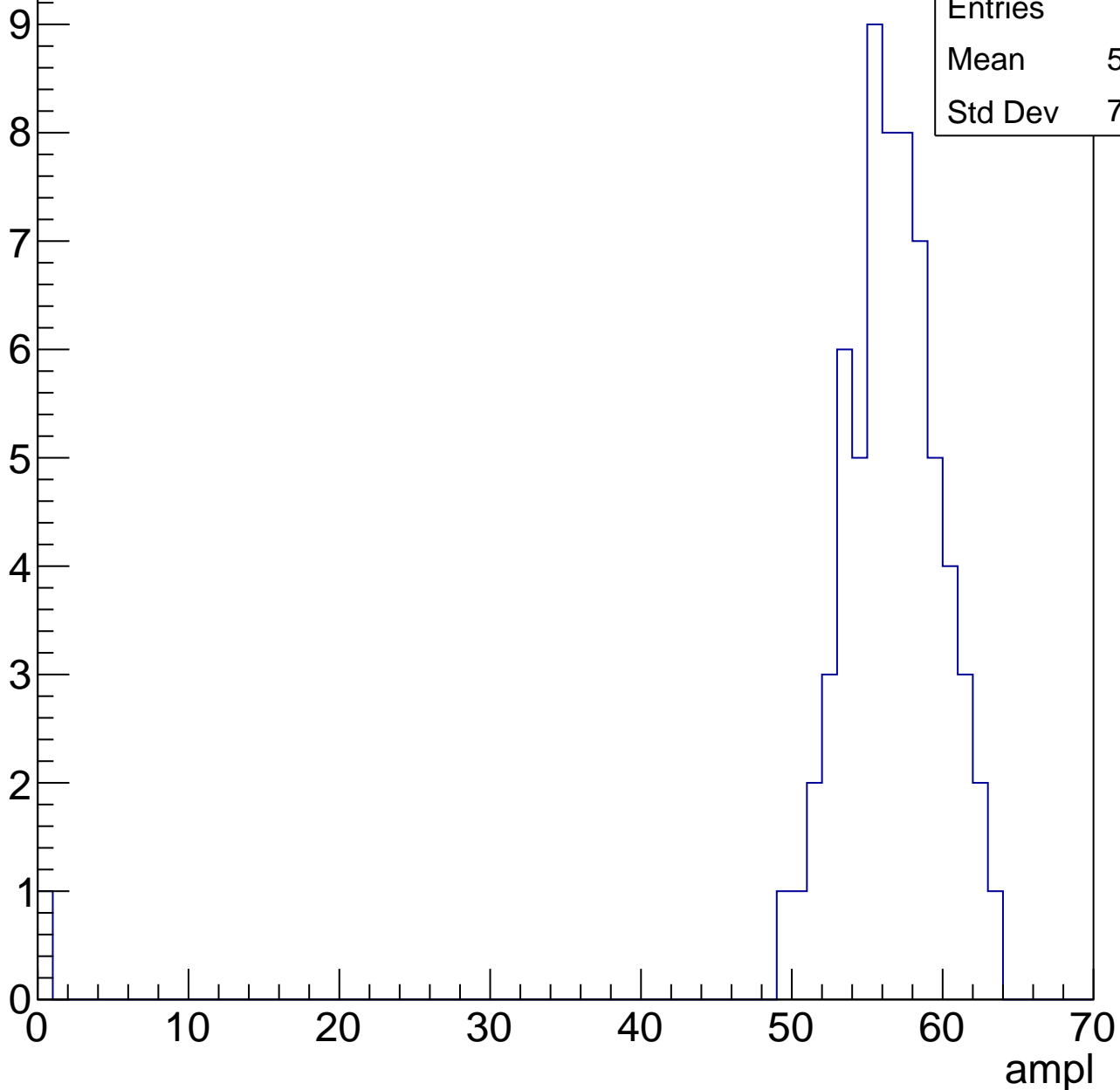


B1L103S, U5-ch31, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	55.38
Std Dev	7.505



B1L103S, U5-ch31, adc5

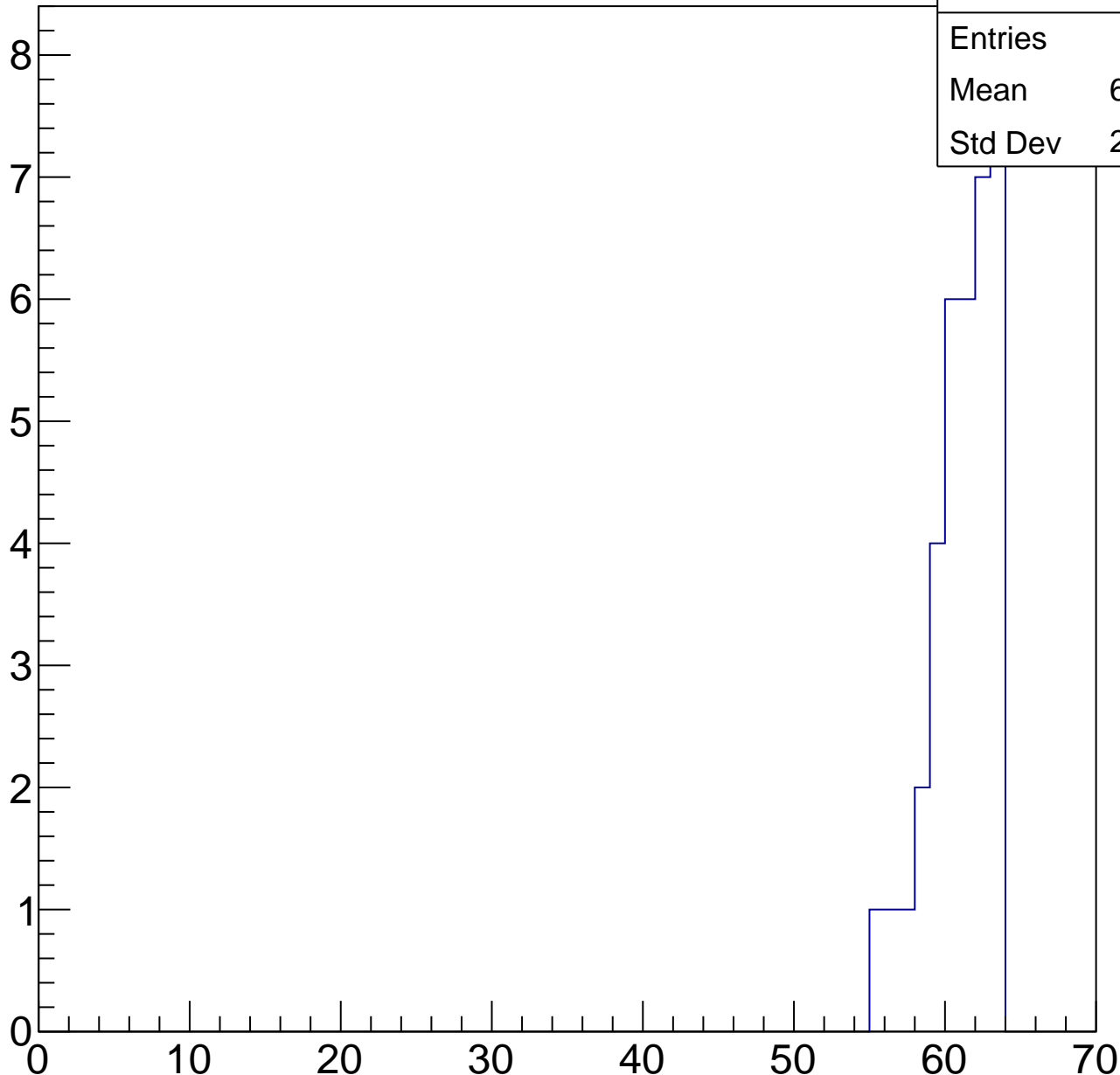
calib_packv5_041523_1651.root, FC#0, port C2

Entry

8
7
6
5
4
3
2
1
0

Entries	36
Mean	60.67
Std Dev	2.055

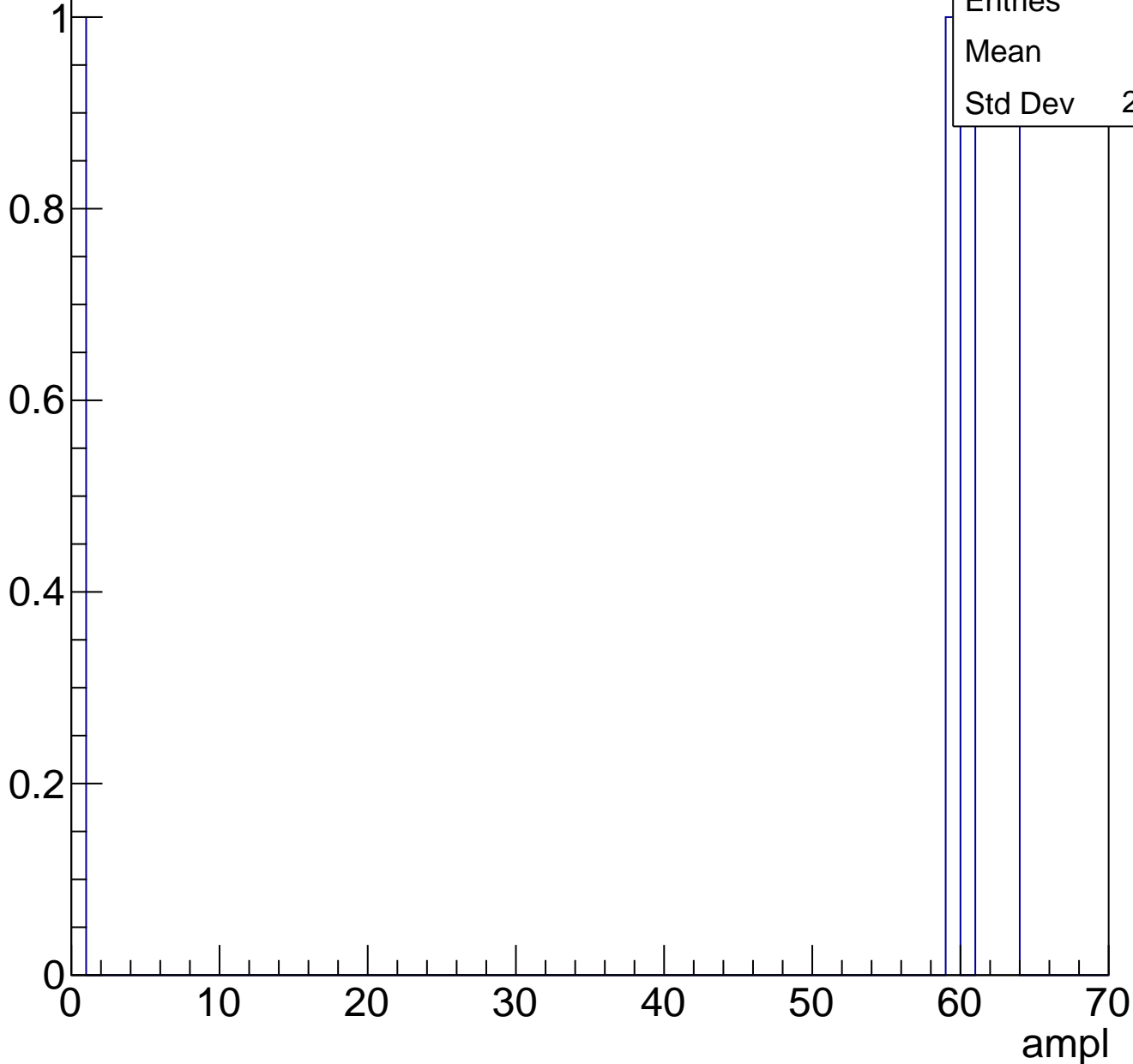
ampl



B1L103S, U5-ch31, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch31, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	18
Mean	0
Std Dev	0

ampl

B1L103S, U5-ch32, adc0

calib_packv5_041523_1651.root, FC#0, port C2

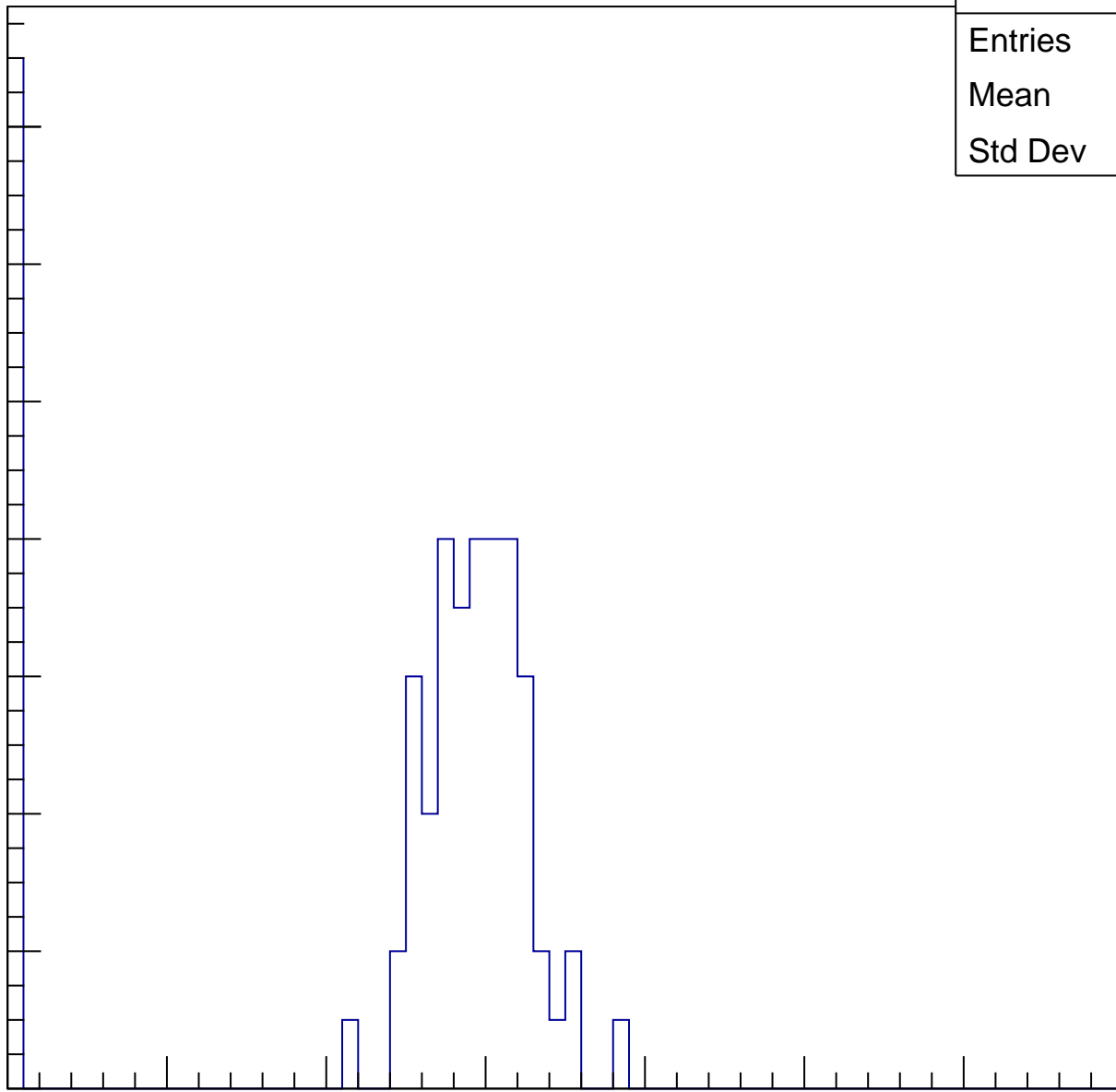
Entries	79
Mean	23.48
Std Dev	11.69

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

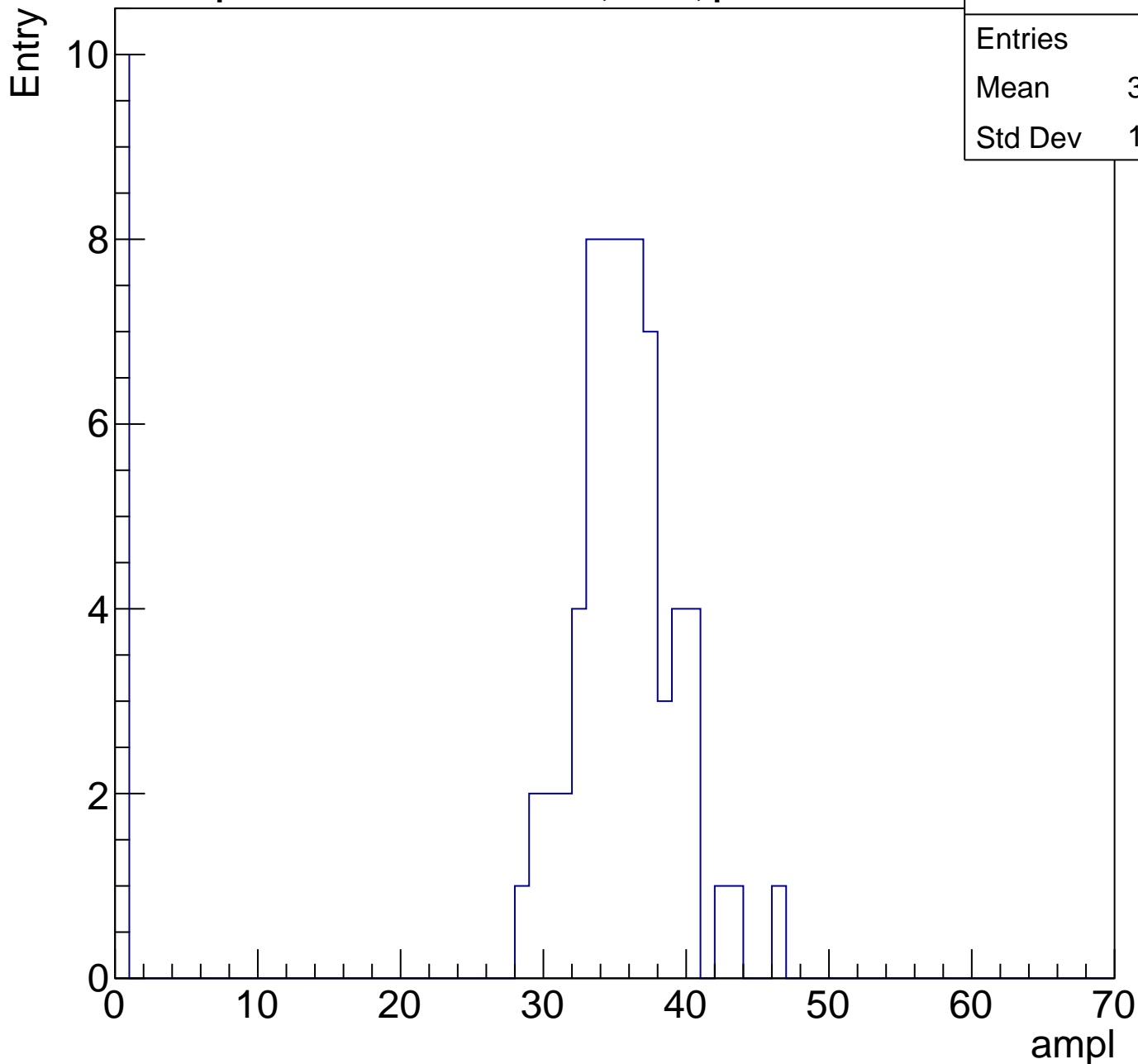
ampl



B1L103S, U5-ch32, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	74
Mean	30.54
Std Dev	12.48



B1L103S, U5-ch32, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	83
Mean	40.81
Std Dev	8.574

Entry

10

8

6

4

2

0

0

10

20

30

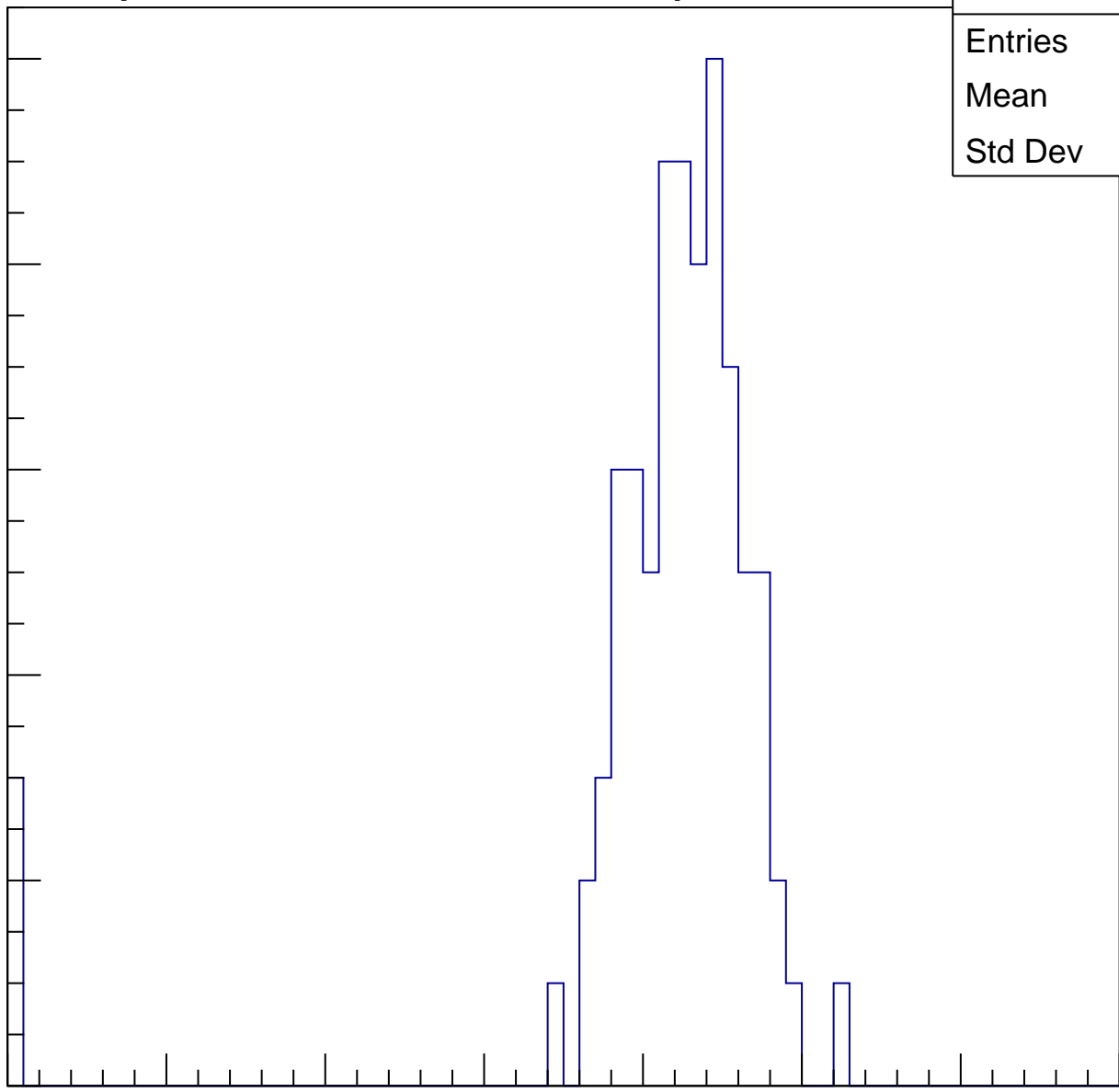
40

50

60

70

ampl

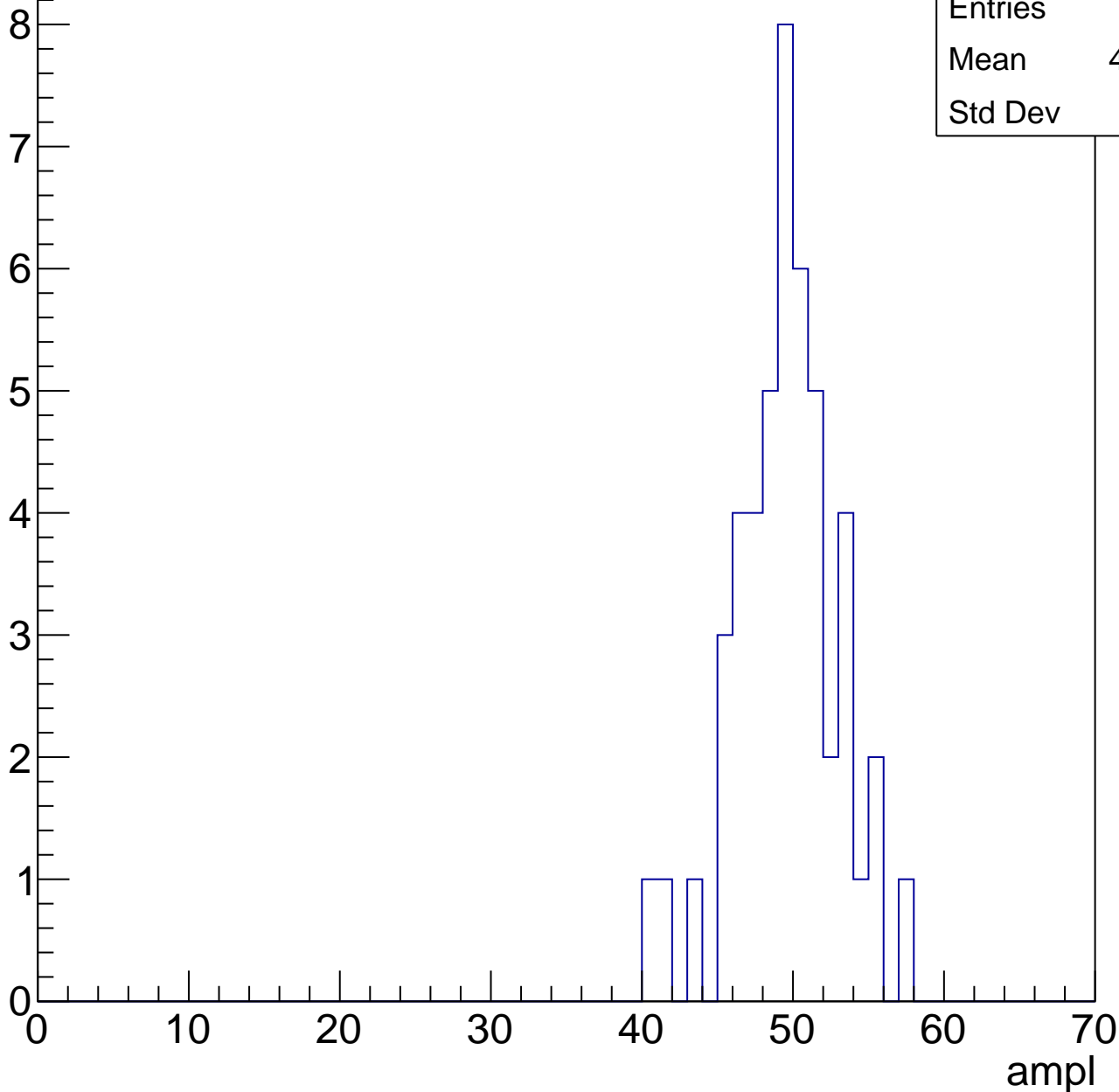


B1L103S, U5-ch32, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	48
Mean	49.06
Std Dev	3.4

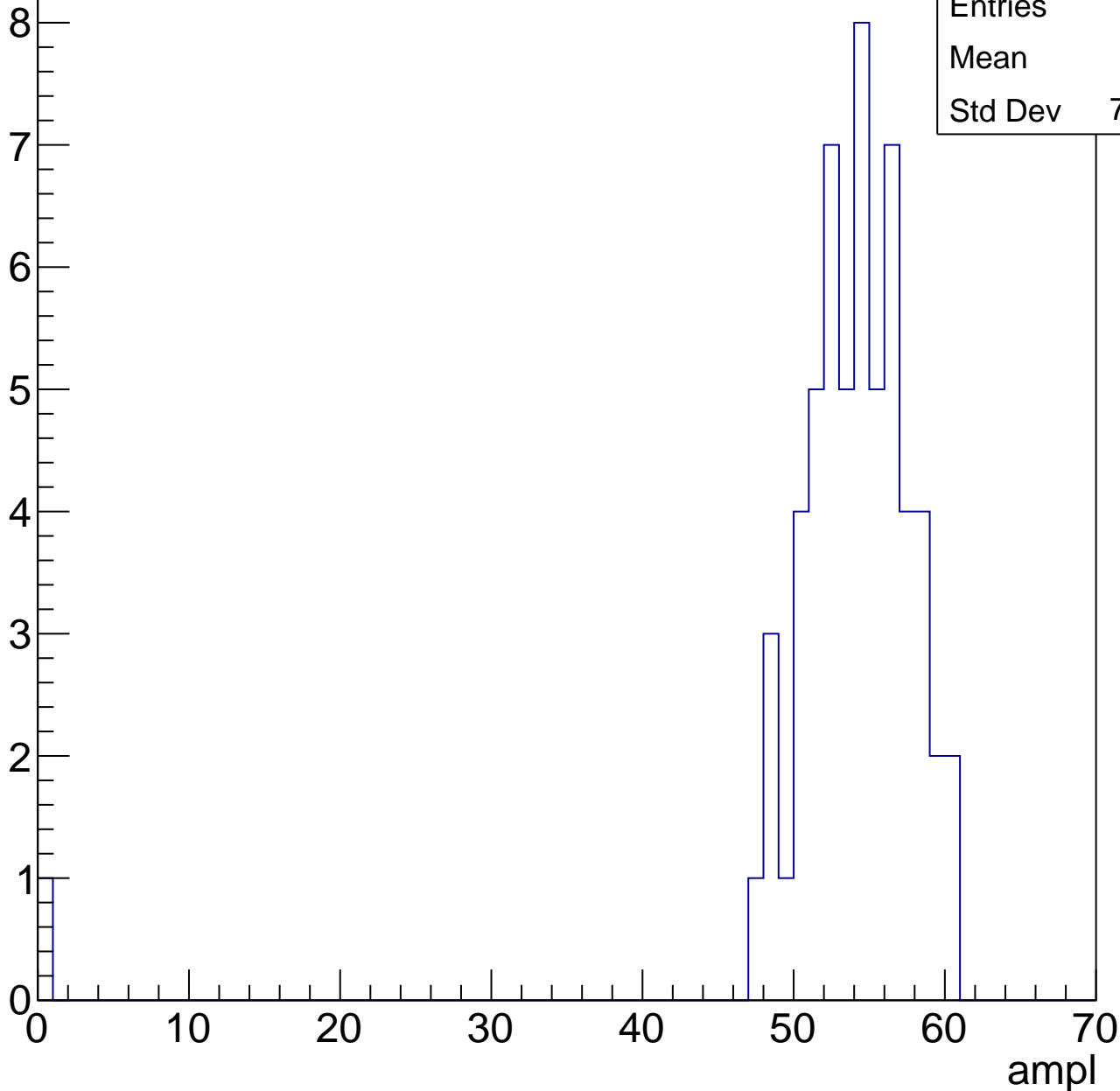


B1L103S, U5-ch32, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	52.9
Std Dev	7.617



B1L103S, U5-ch32, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

8
7
6
5
4
3
2
1
0

Entries	52
Mean	58.1
Std Dev	8.509

ampl

0

10

20

30

40

50

60

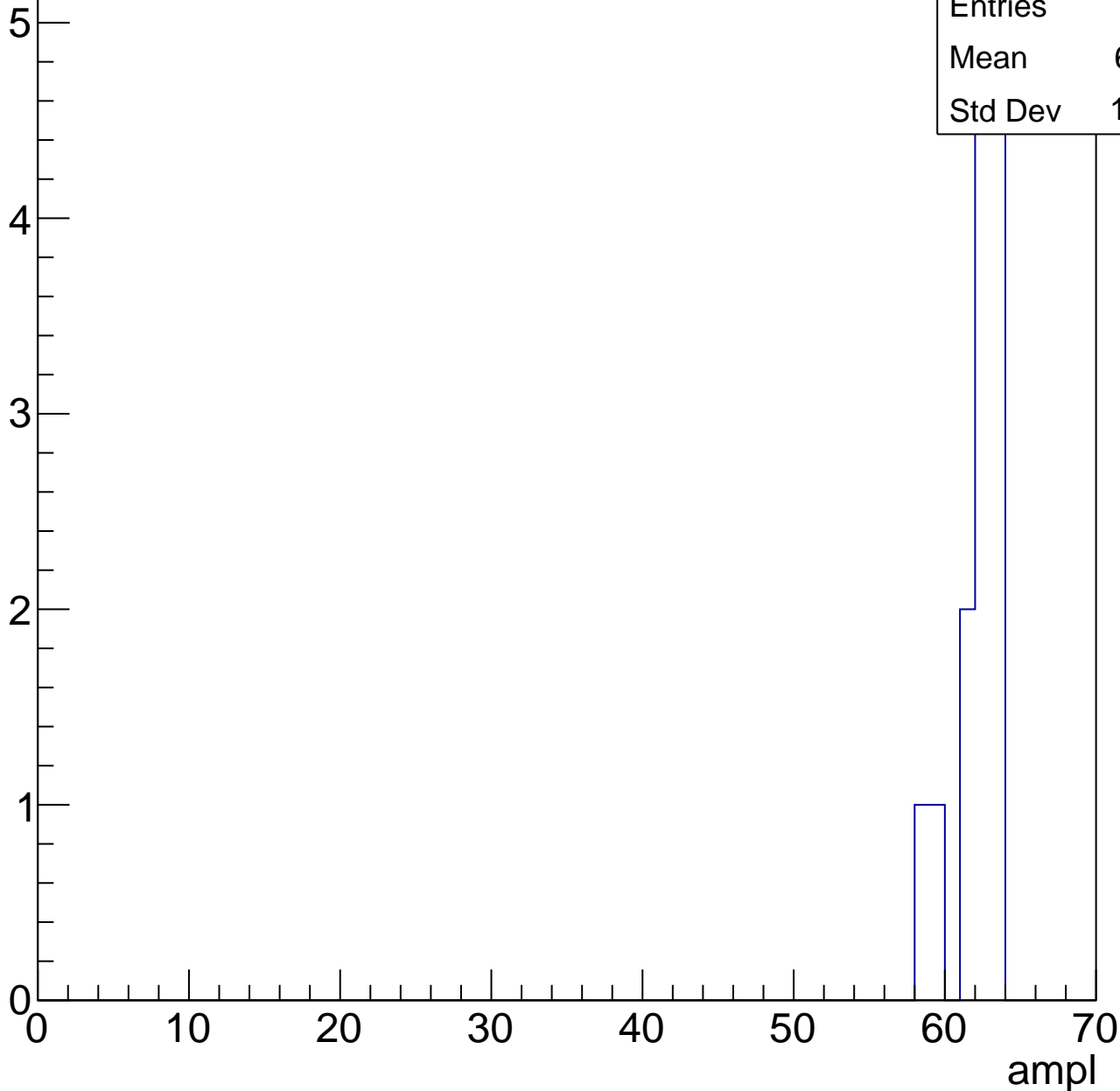
70

B1L103S, U5-ch32, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	14
Mean	61.71
Std Dev	1.485



B1L103S, U5-ch32, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch33, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	116
Mean	21.38
Std Dev	13.83

Entry

30

25

20

15

10

5

0

0

10

20

30

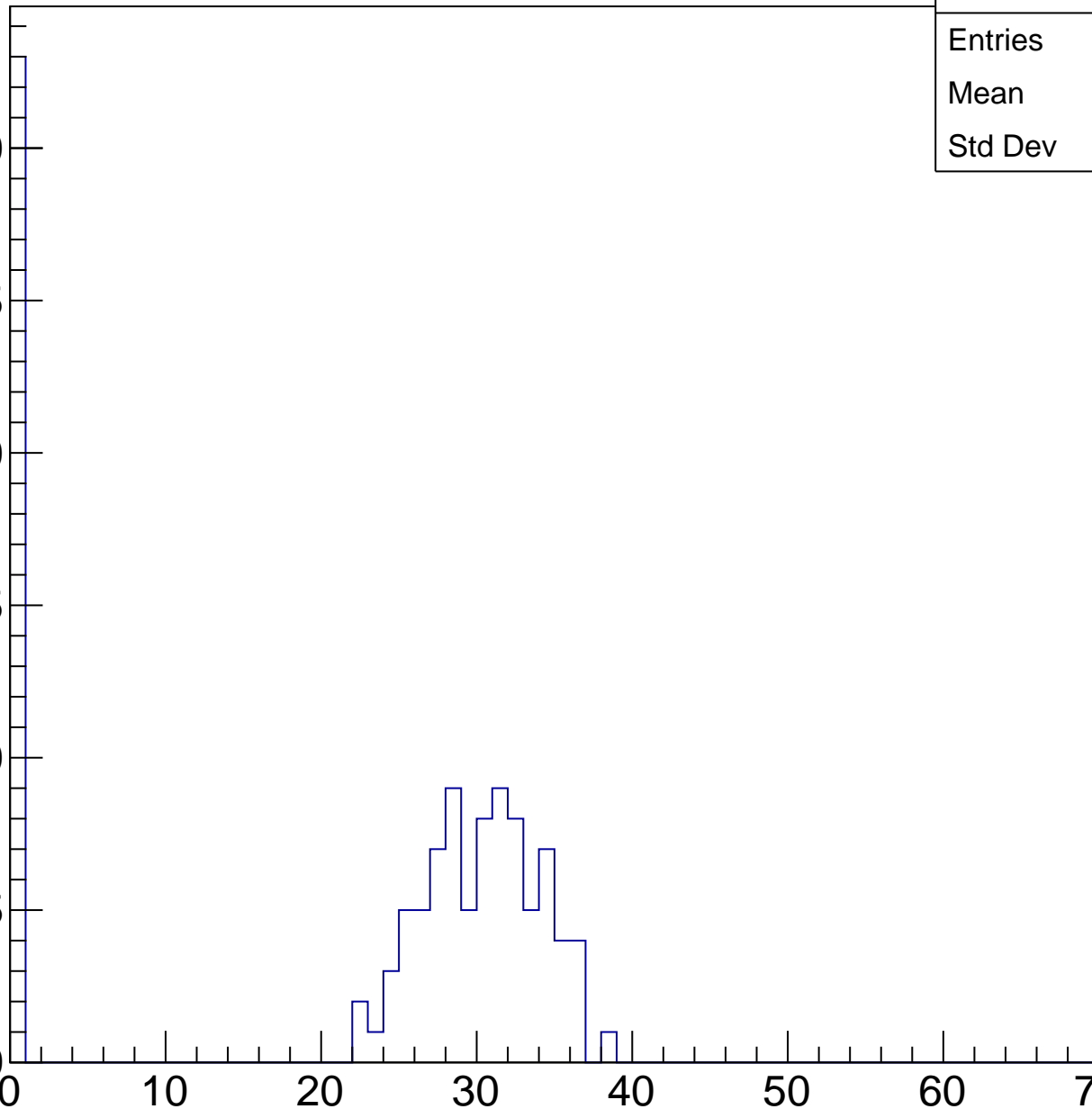
40

50

60

70

ampl

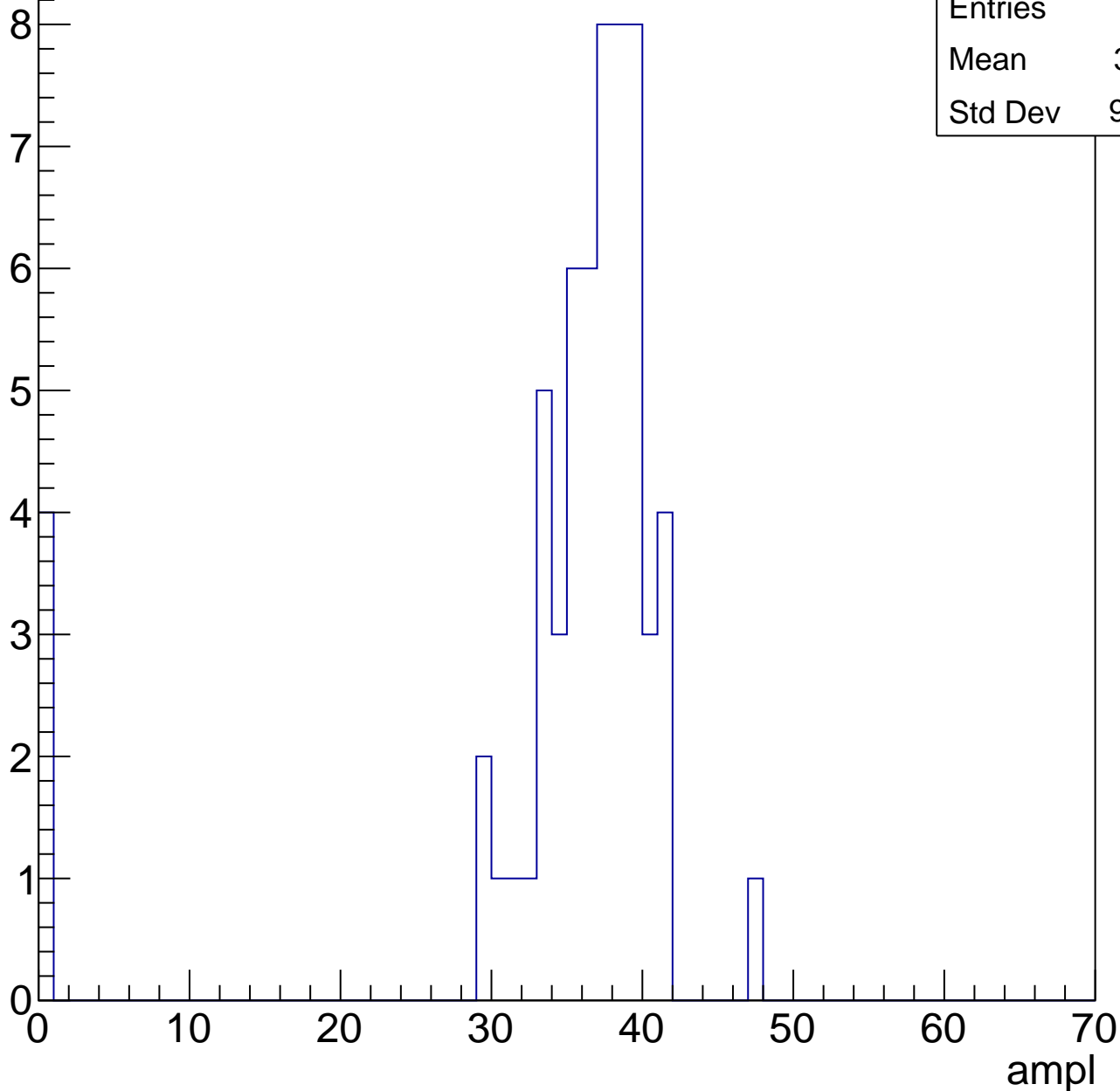


B1L103S, U5-ch33, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

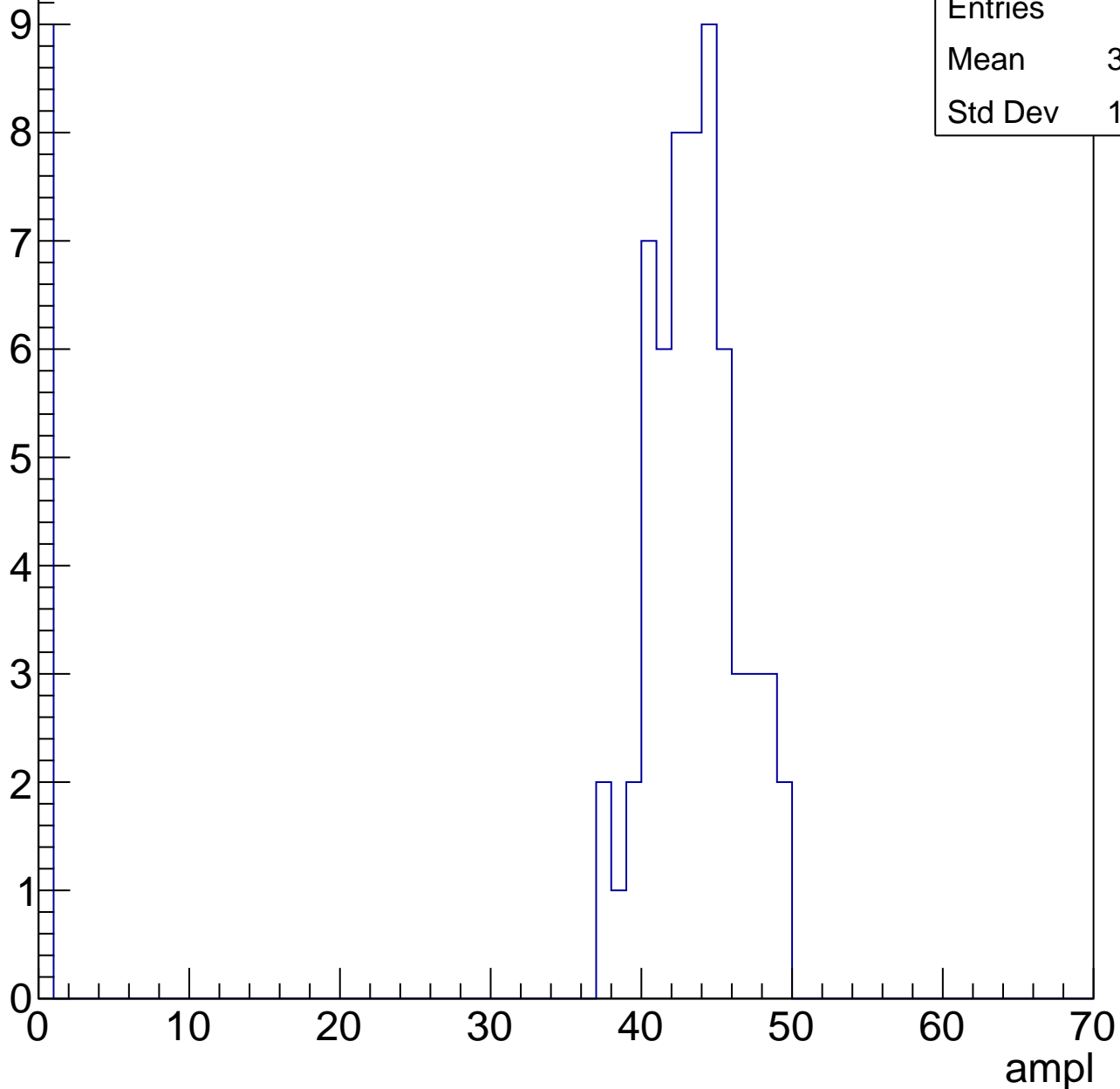
Entries	61
Mean	34.21
Std Dev	9.588



B1L103S, U5-ch33, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch33, adc3

calib_packv5_041523_1651.root, FC#0, port C2

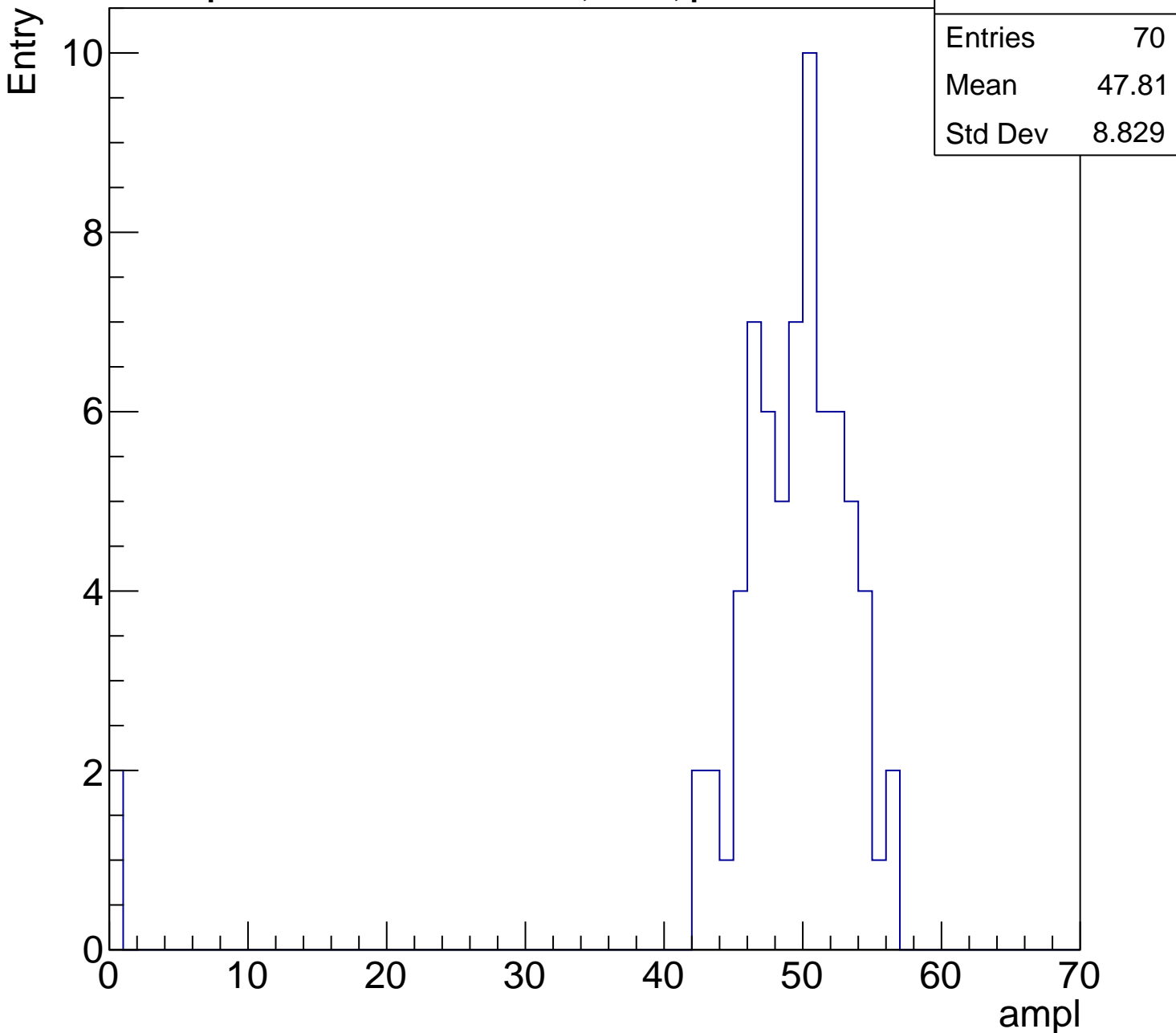
Entries	70
Mean	47.81
Std Dev	8.829

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

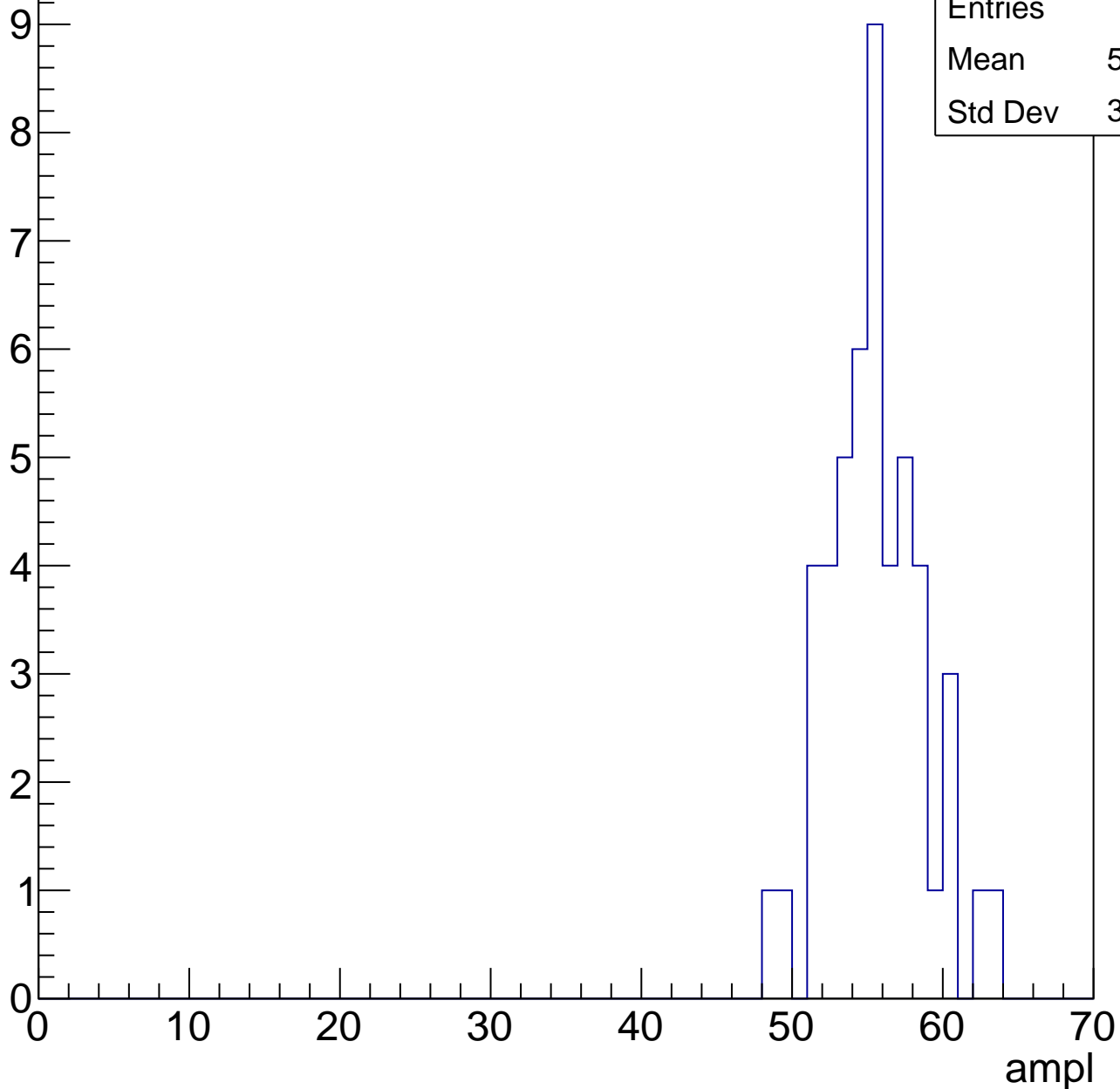
ampl



B1L103S, U5-ch33, adc4

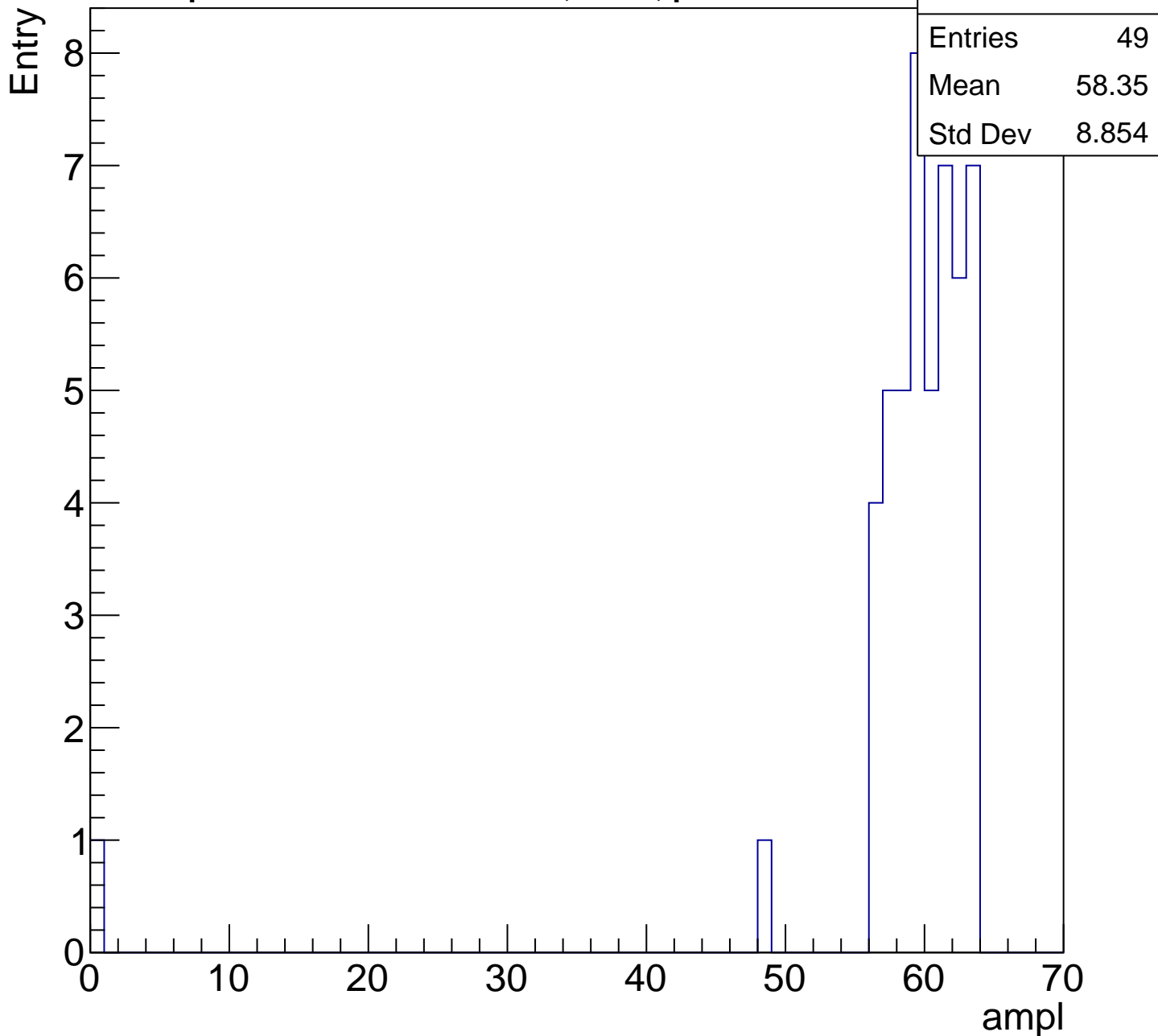
calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch33, adc5

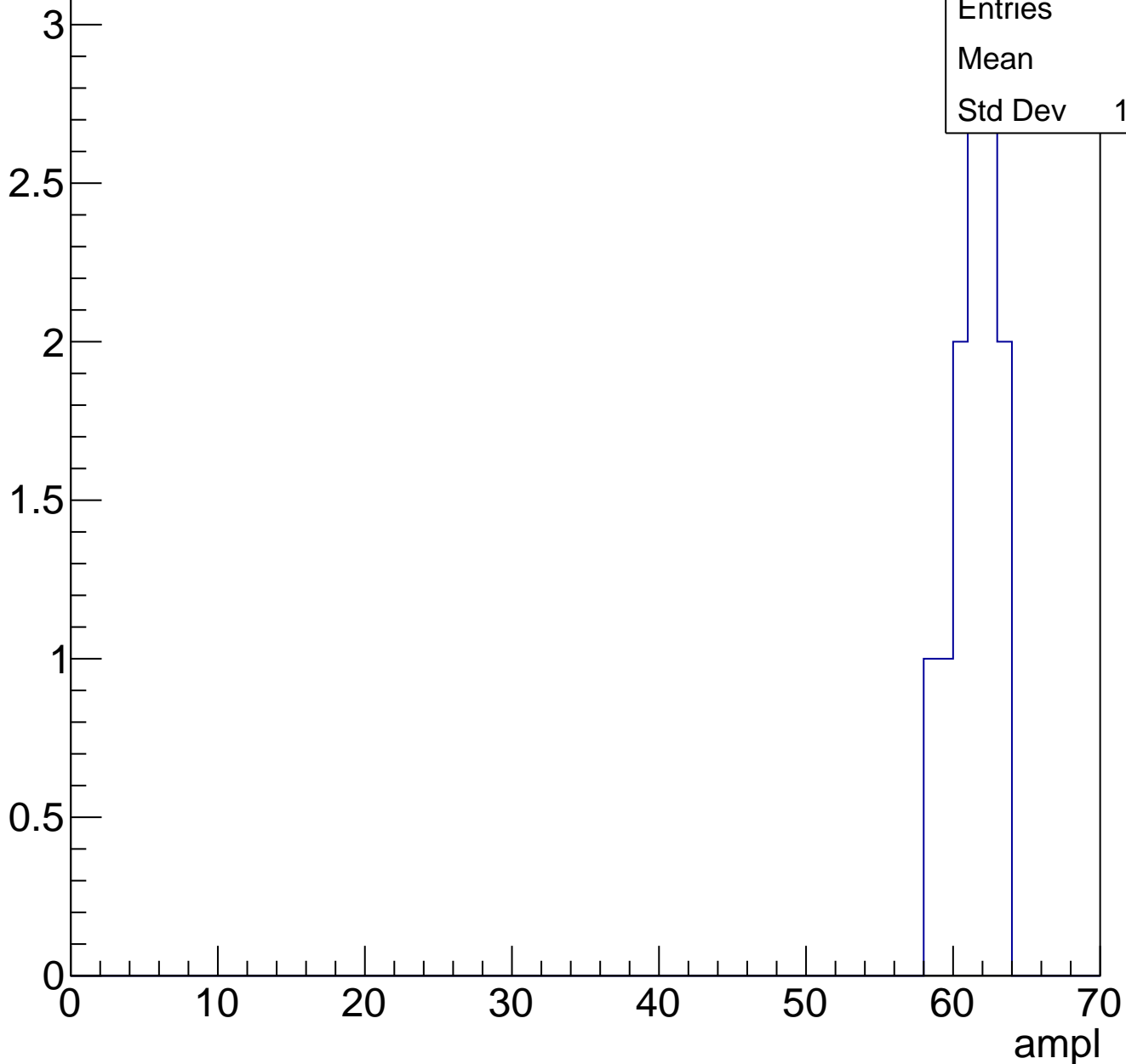
calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U5-ch33, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch33, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

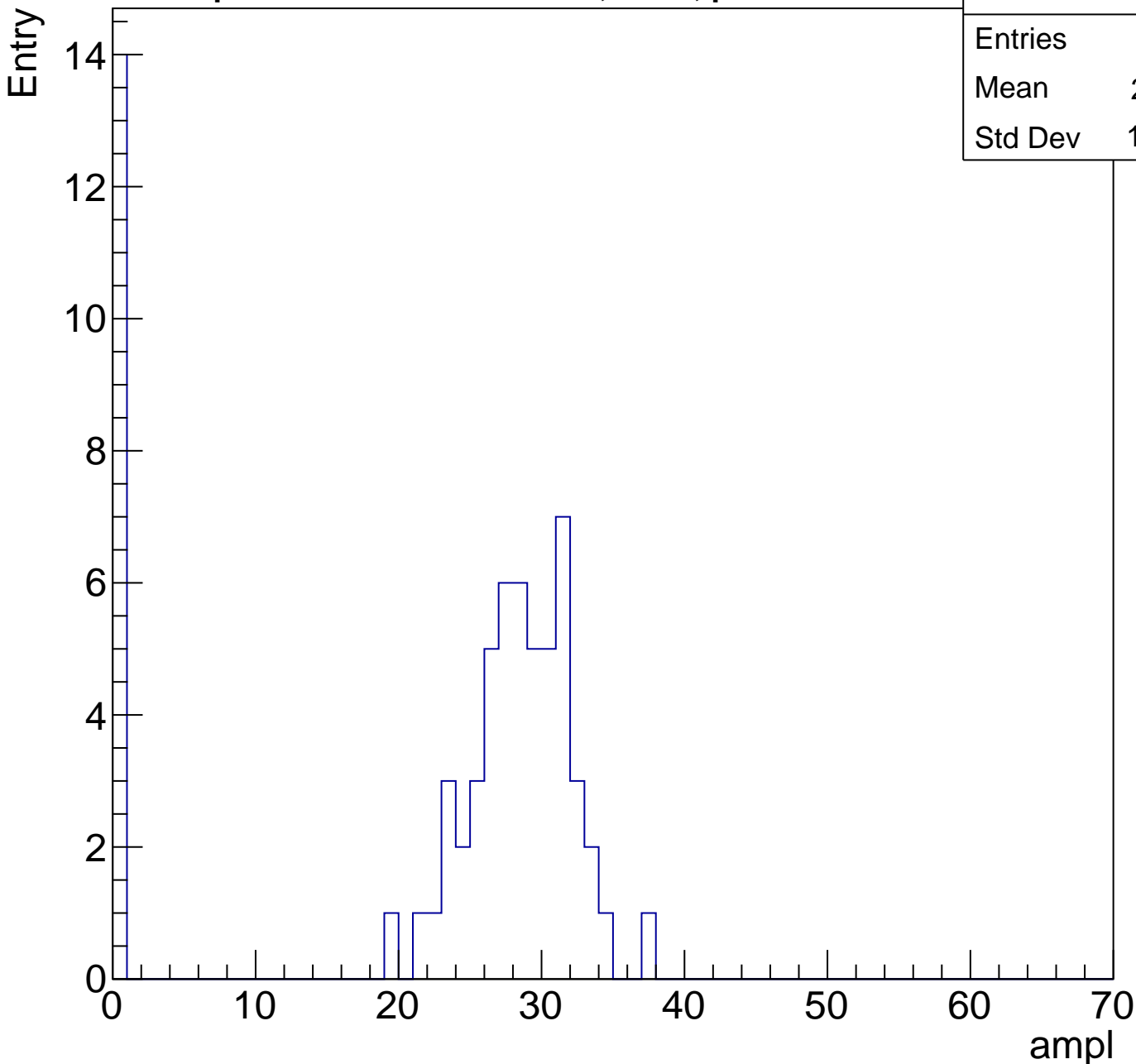
ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U5-ch34, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	66
Mean	22.11
Std Dev	11.88

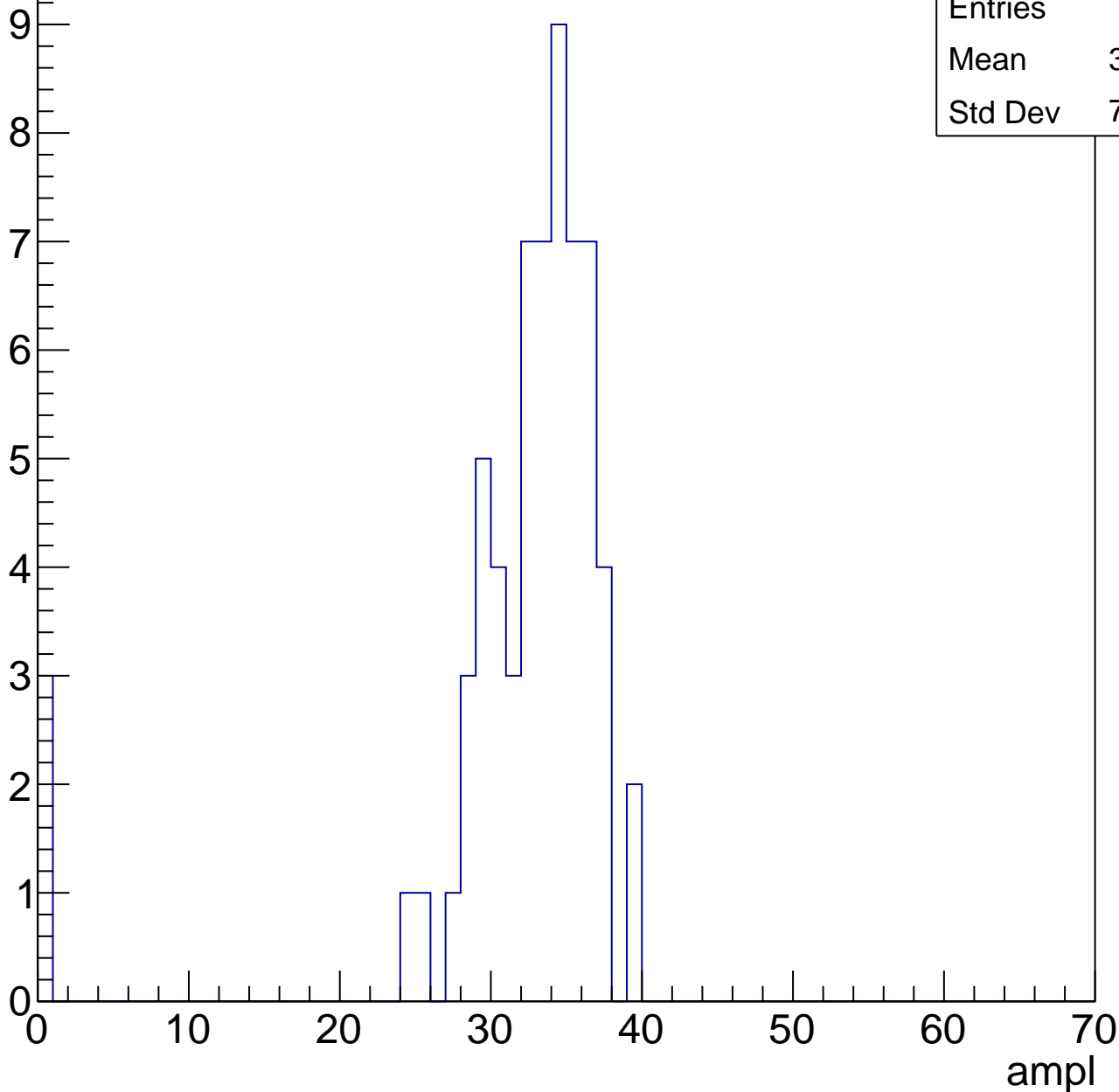


B1L103S, U5-ch34, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	31.28
Std Dev	7.609



B1L103S, U5-ch34, adc2

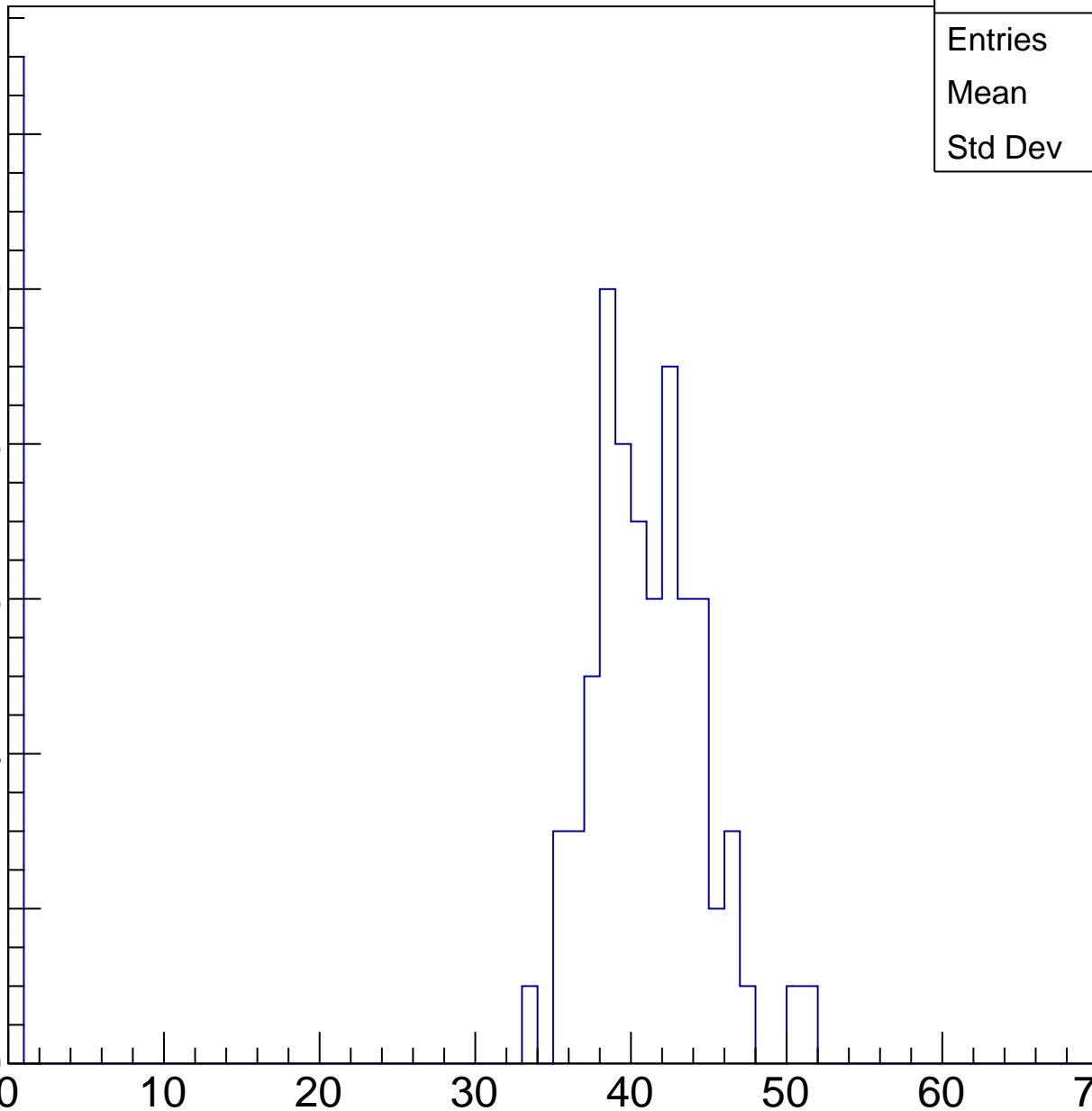
calib_packv5_041523_1651.root, FC#0, port C2

Entry

12
10
8
6
4
2
0

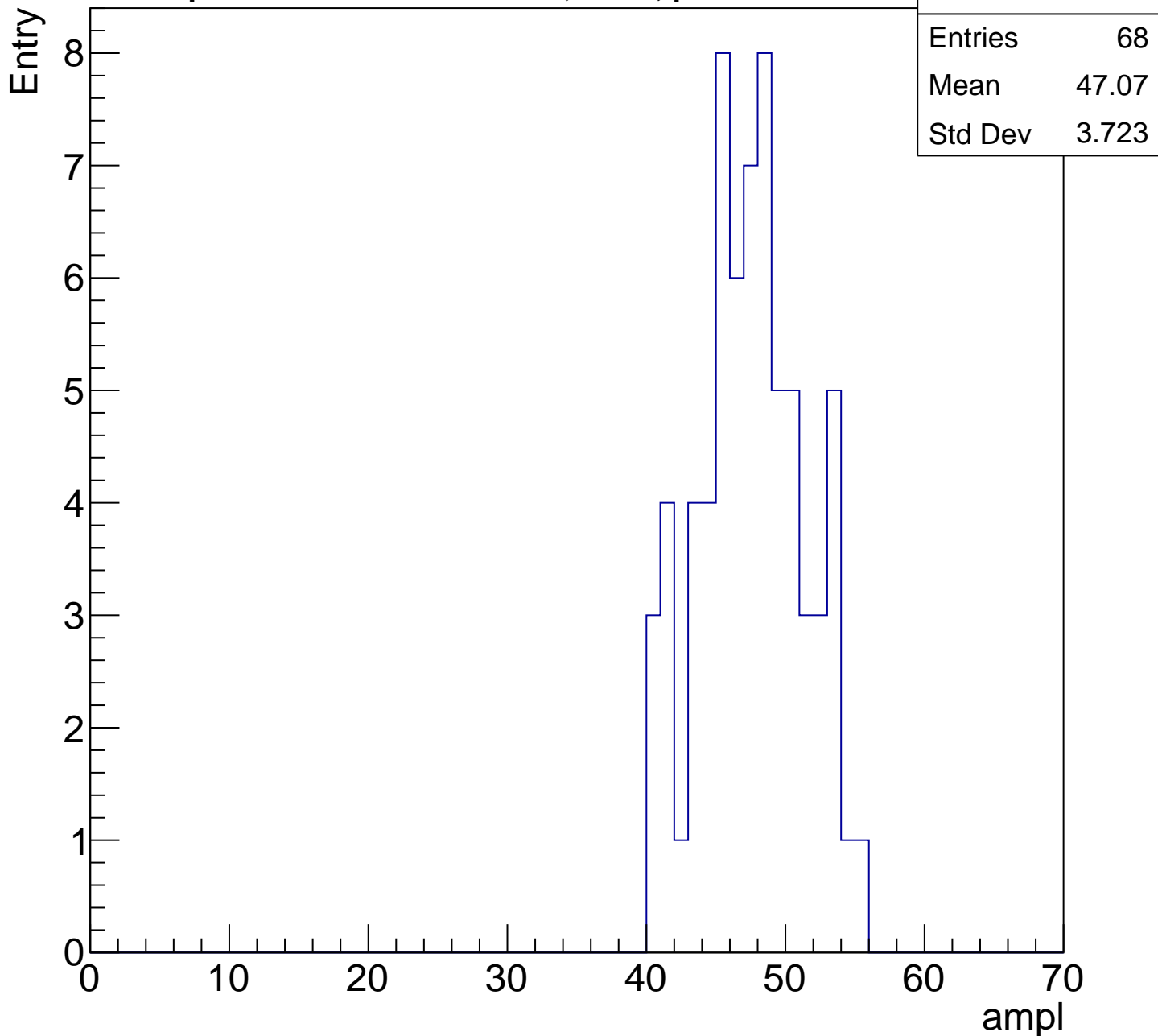
Entries	85
Mean	34.41
Std Dev	14.96

ampl



B1L103S, U5-ch34, adc3

calib_packv5_041523_1651.root, FC#0, port C2

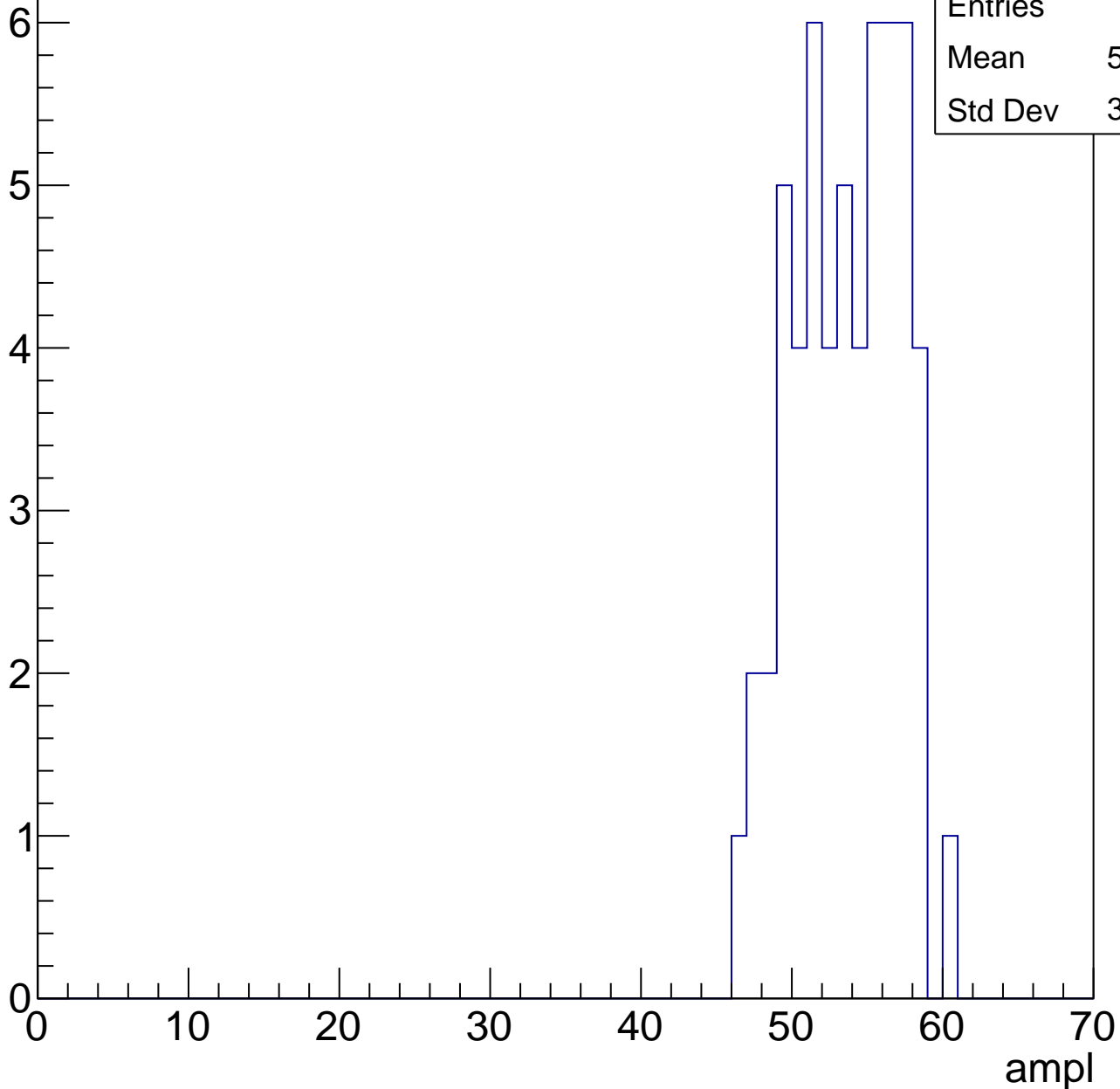


B1L103S, U5-ch34, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	53.14
Std Dev	3.383

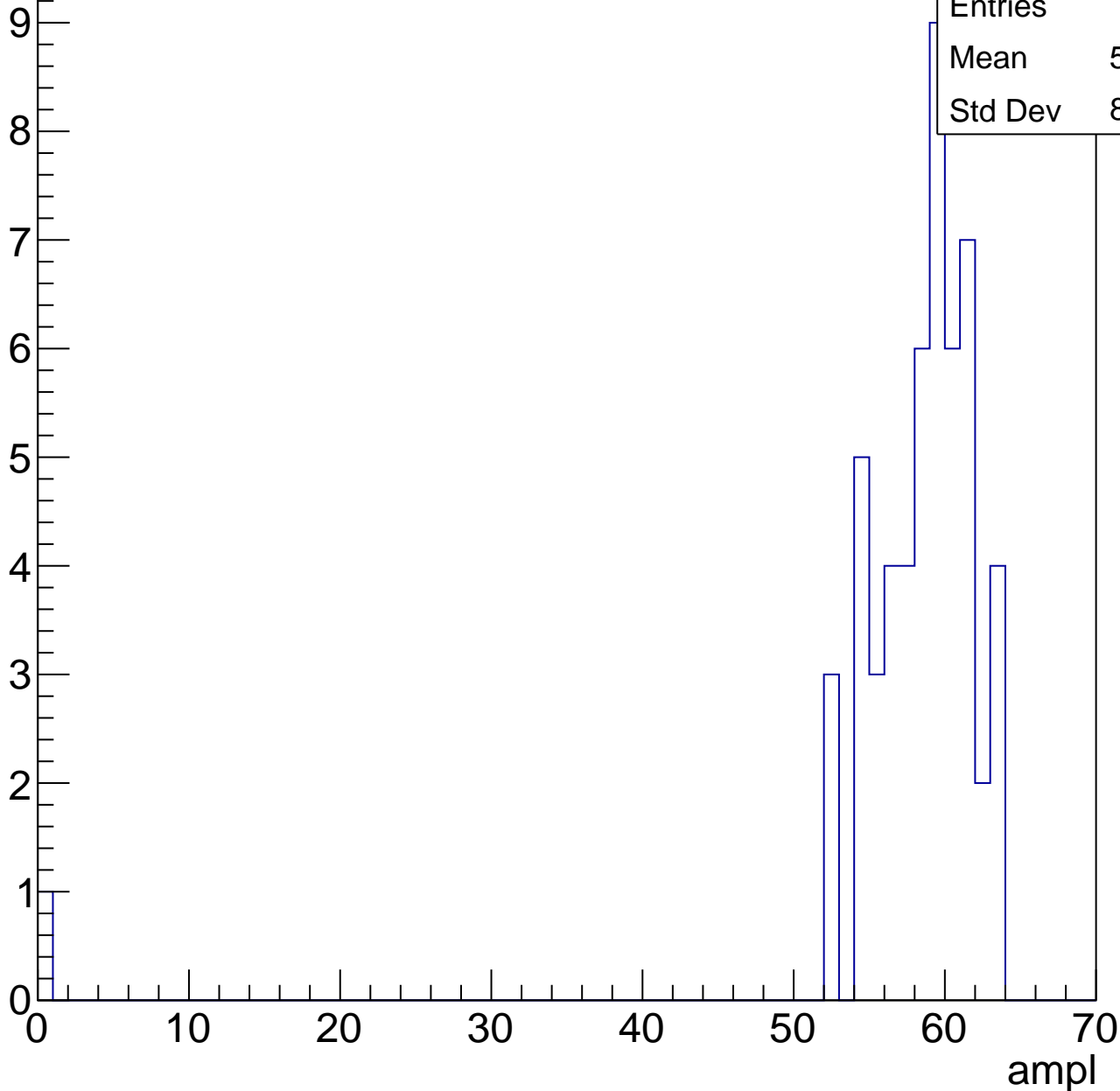


B1L103S, U5-ch34, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	57.13
Std Dev	8.373

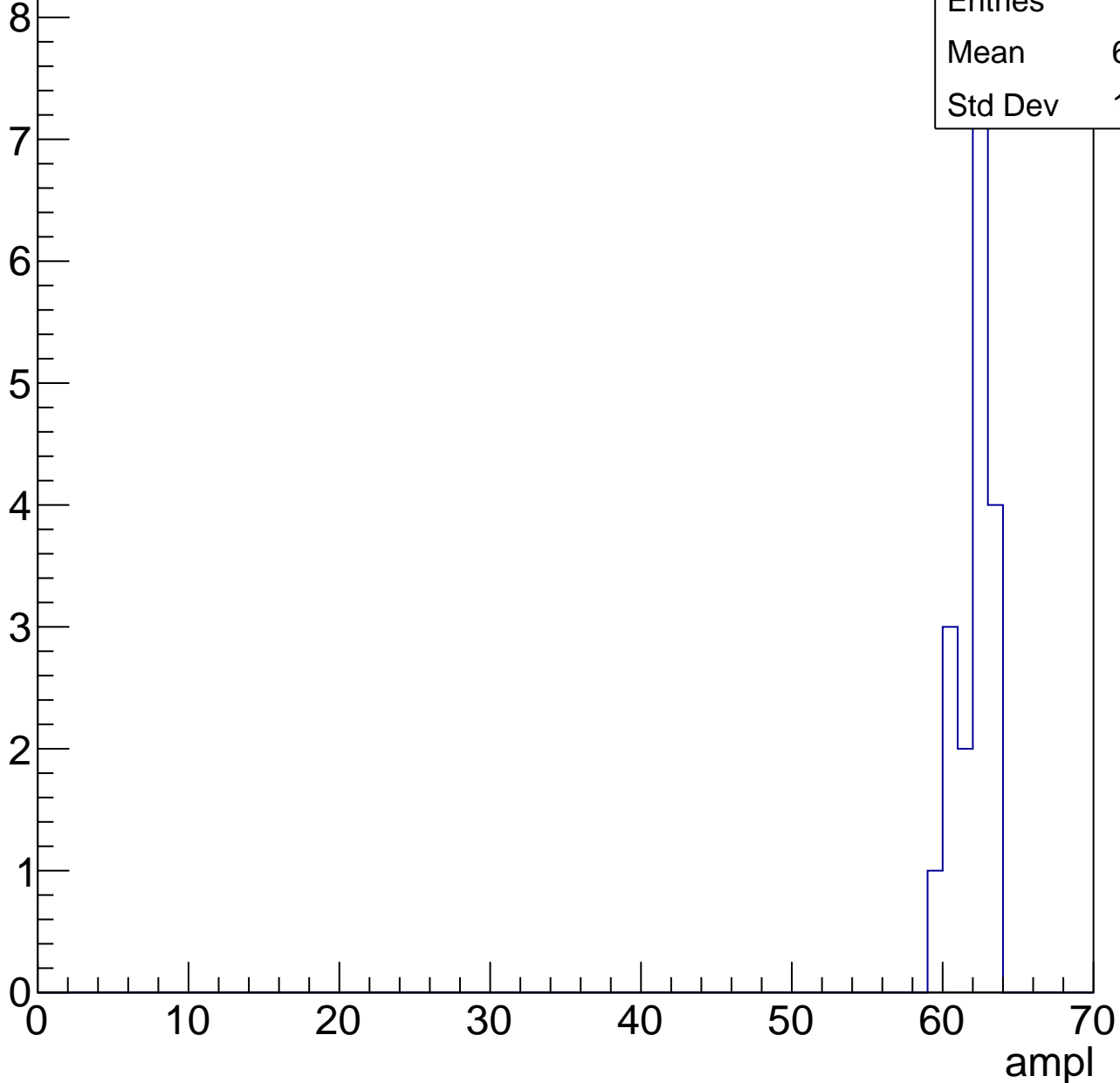


B1L103S, U5-ch34, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	18
Mean	61.61
Std Dev	1.161

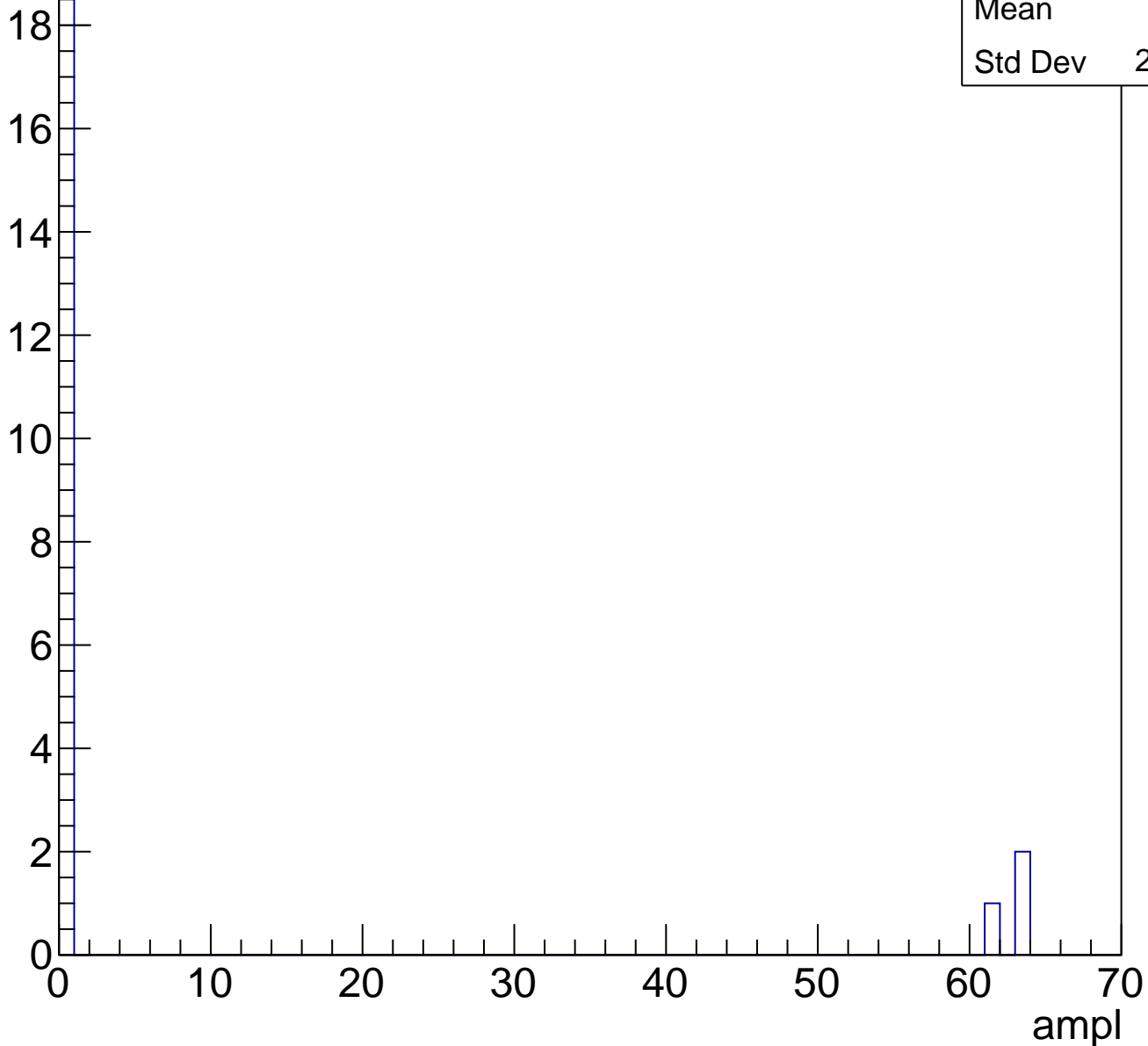


B1L103S, U5-ch34, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	22
Mean	8.5
Std Dev	21.39

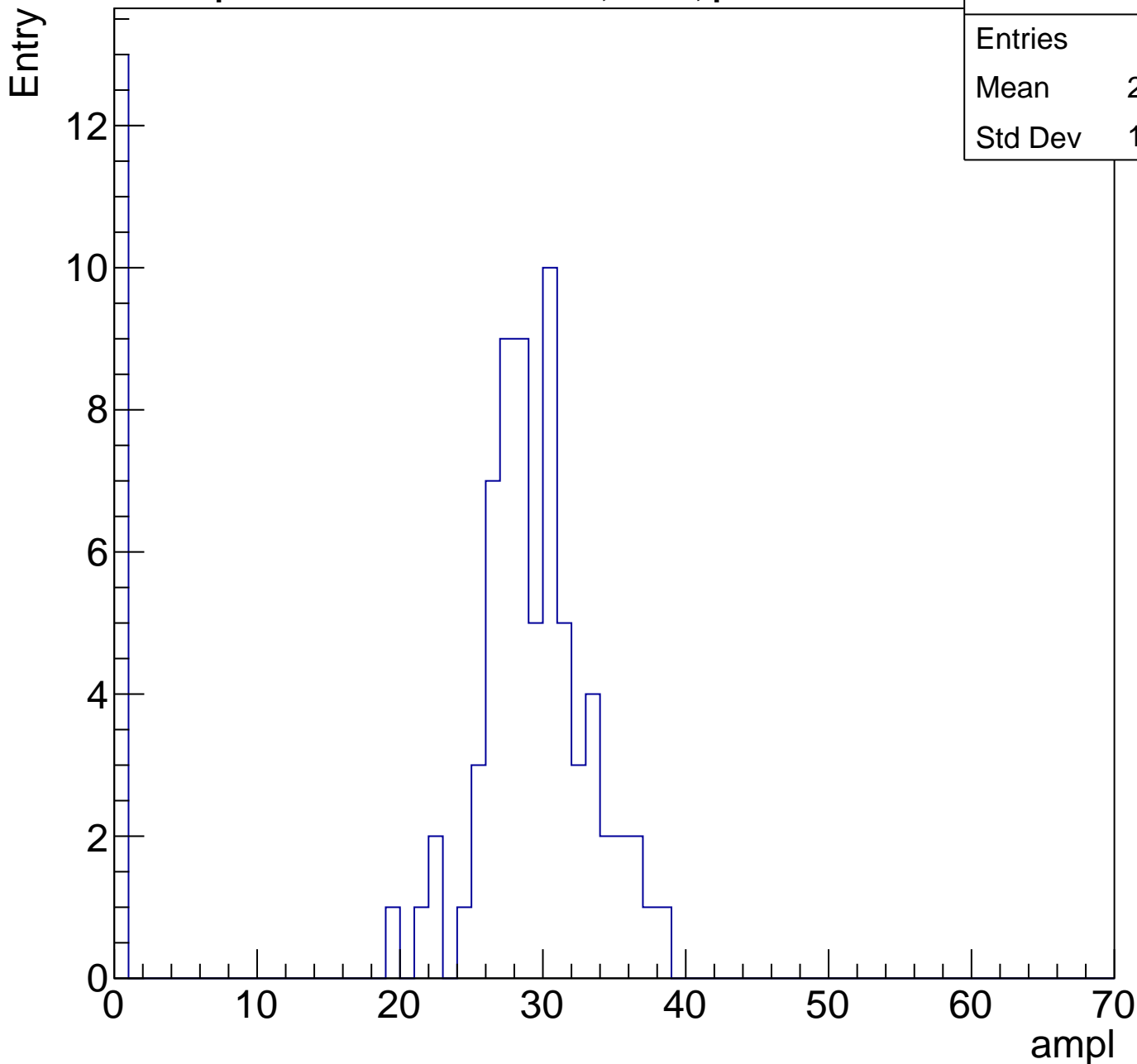
Entry



B1L103S, U5-ch35, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	24.36
Std Dev	11.18

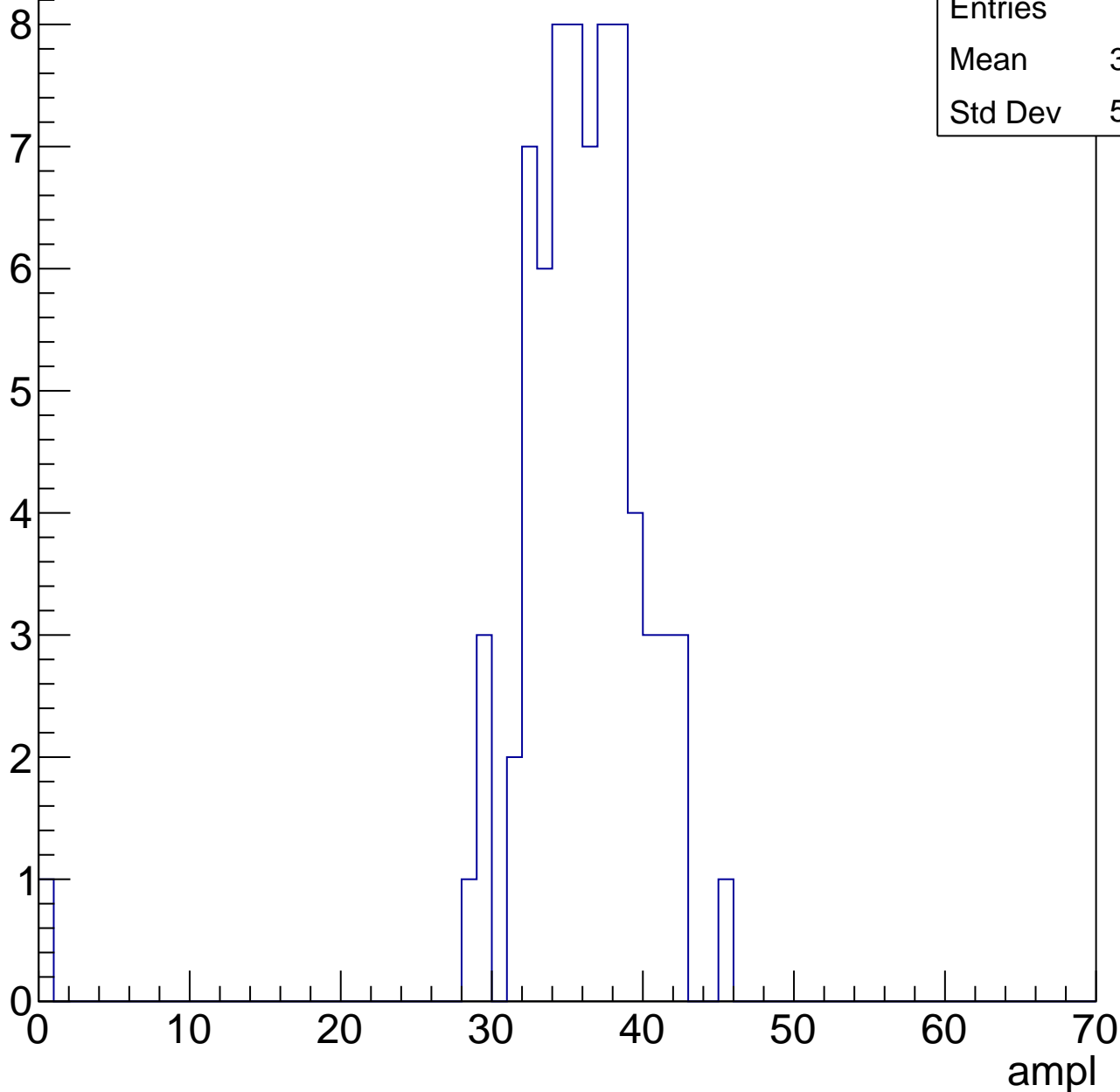


B1L103S, U5-ch35, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	35.25
Std Dev	5.376

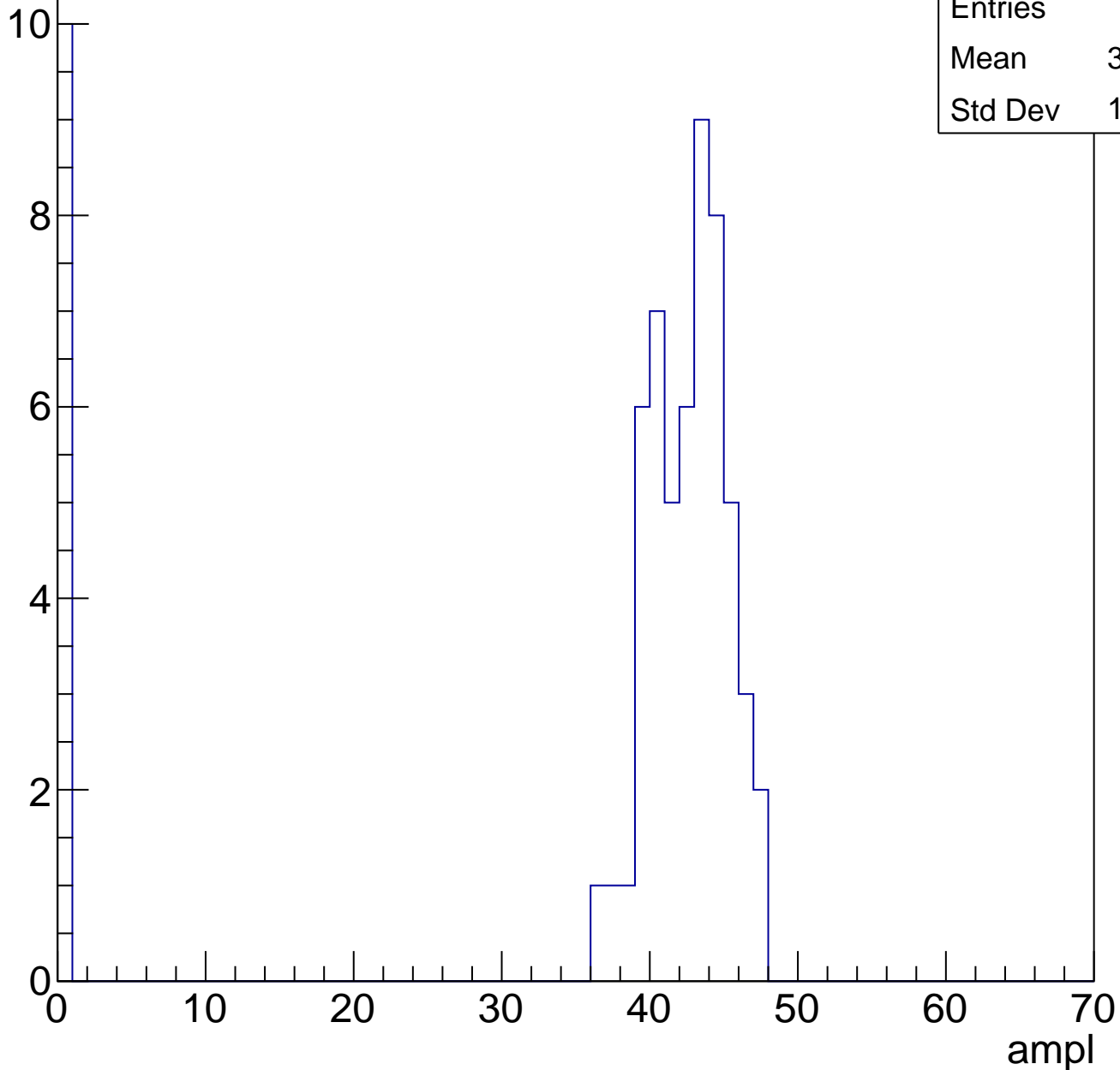


B1L103S, U5-ch35, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	64
Mean	35.59
Std Dev	15.49

Entry

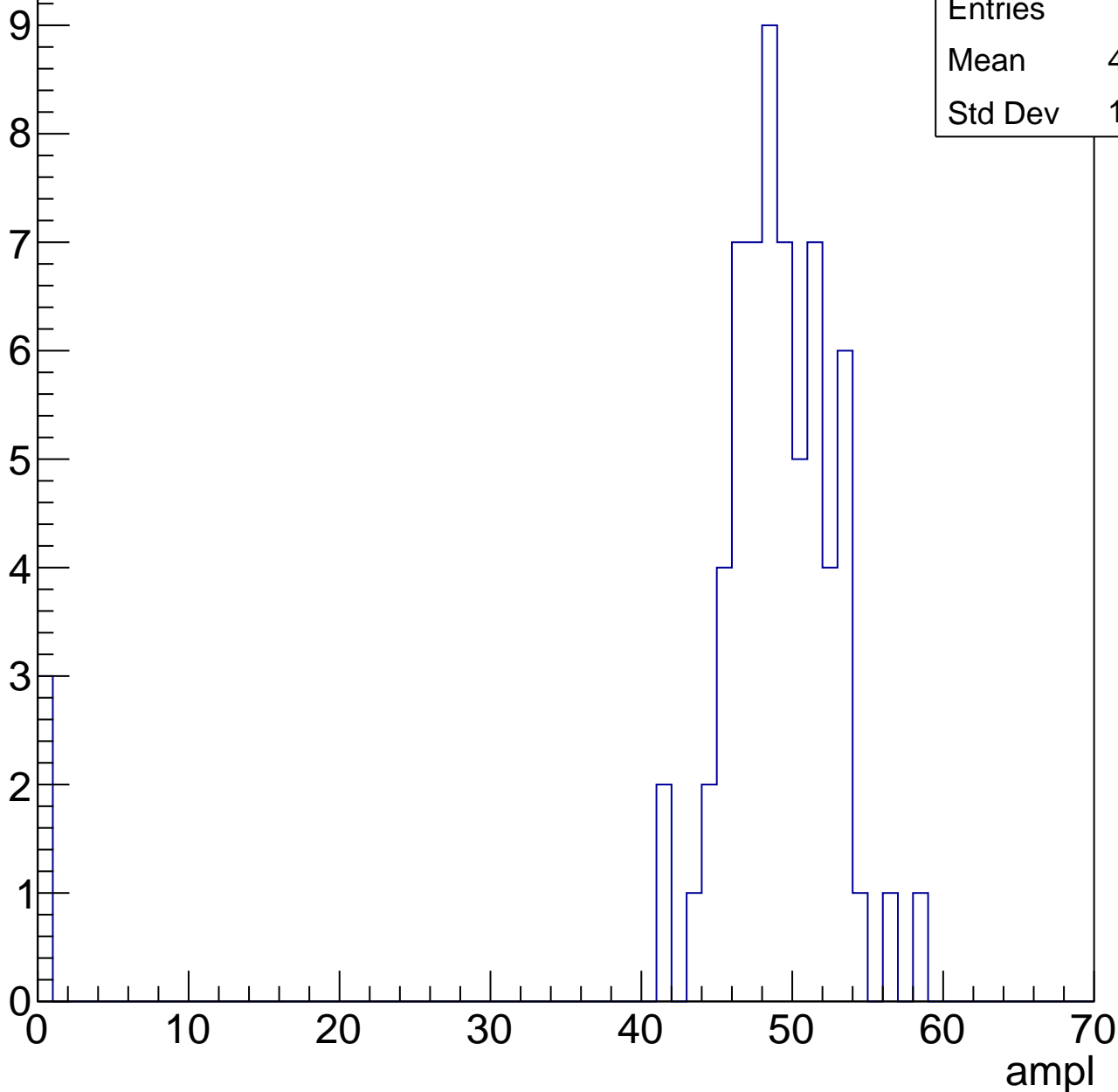


B1L103S, U5-ch35, adc3

calib_packv5_041523_1651.root, FC#0, port C2

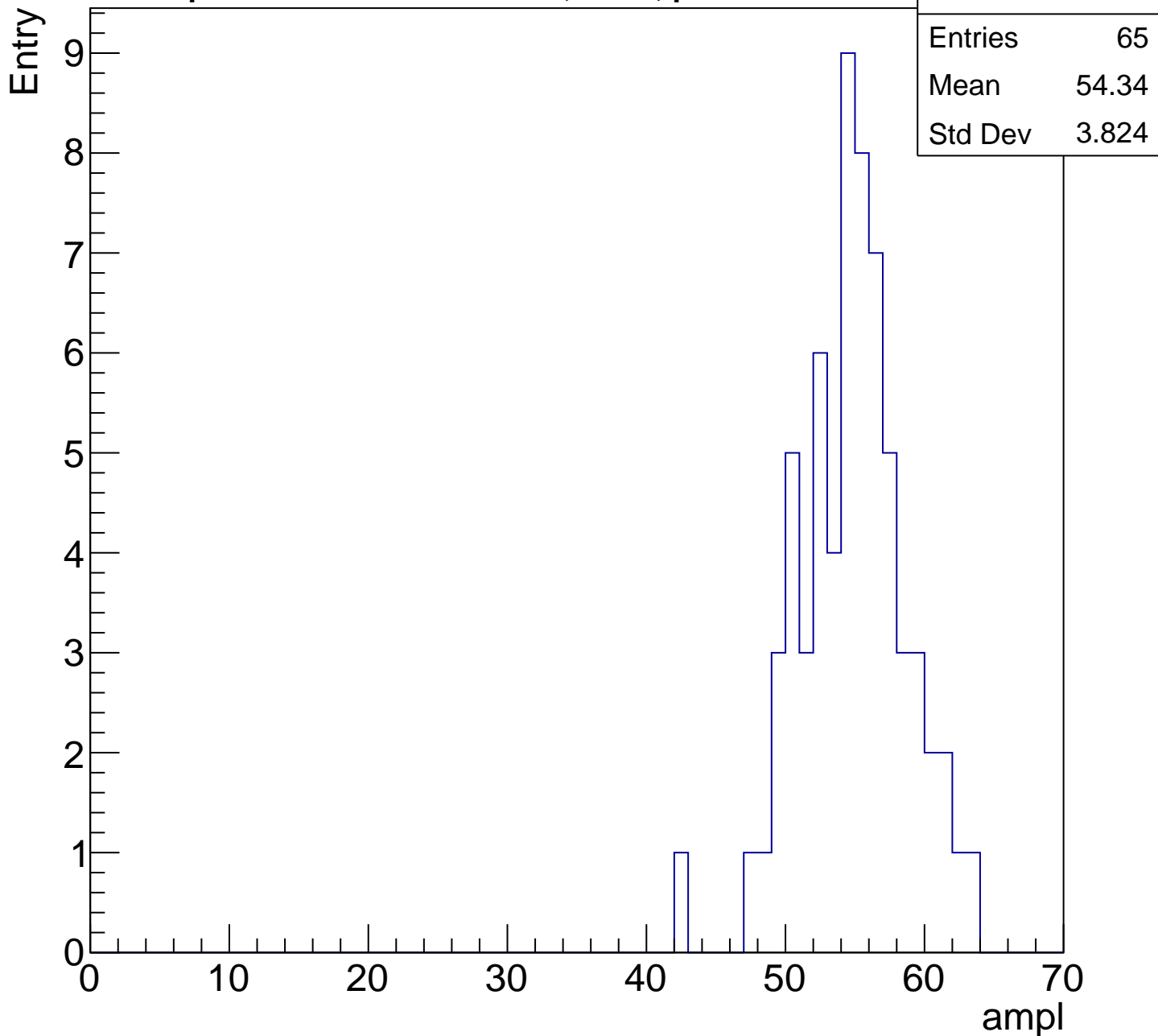
Entry

Entries	67
Mean	46.57
Std Dev	10.58



B1L103S, U5-ch35, adc4

calib_packv5_041523_1651.root, FC#0, port C2

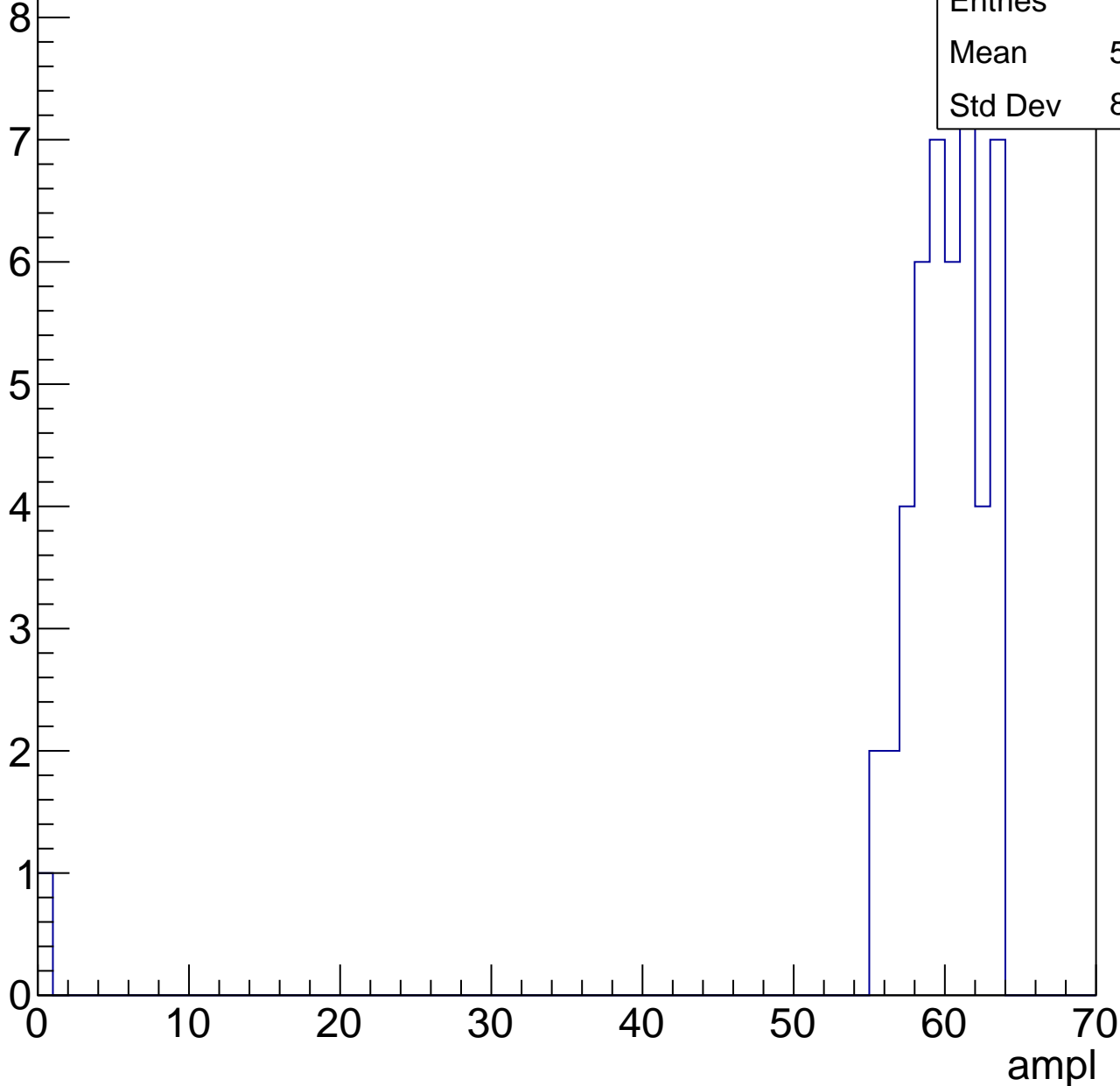


B1L103S, U5-ch35, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	47
Mean	58.47
Std Dev	8.903

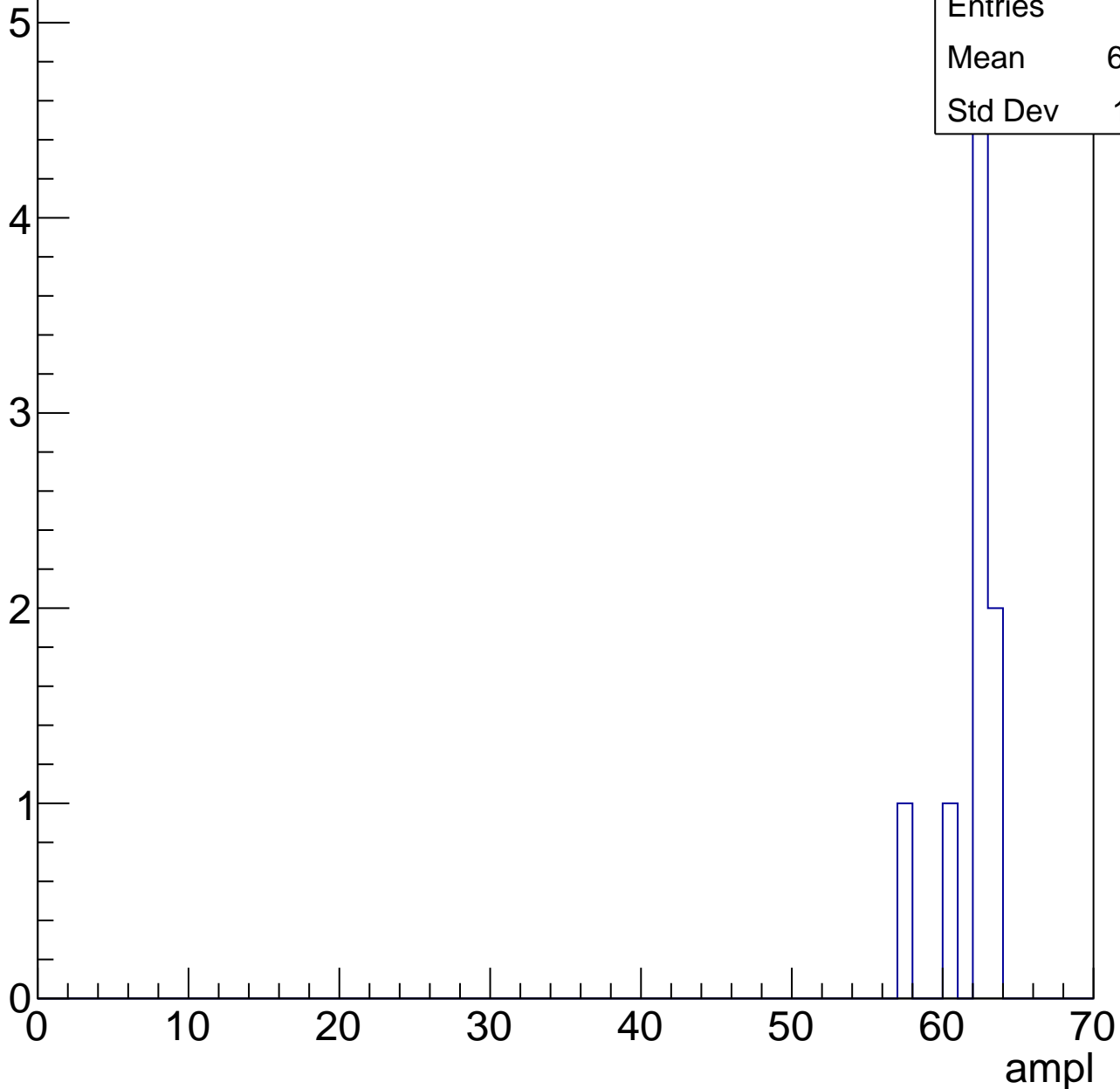


B1L103S, U5-ch35, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	9
Mean	61.44
Std Dev	1.771

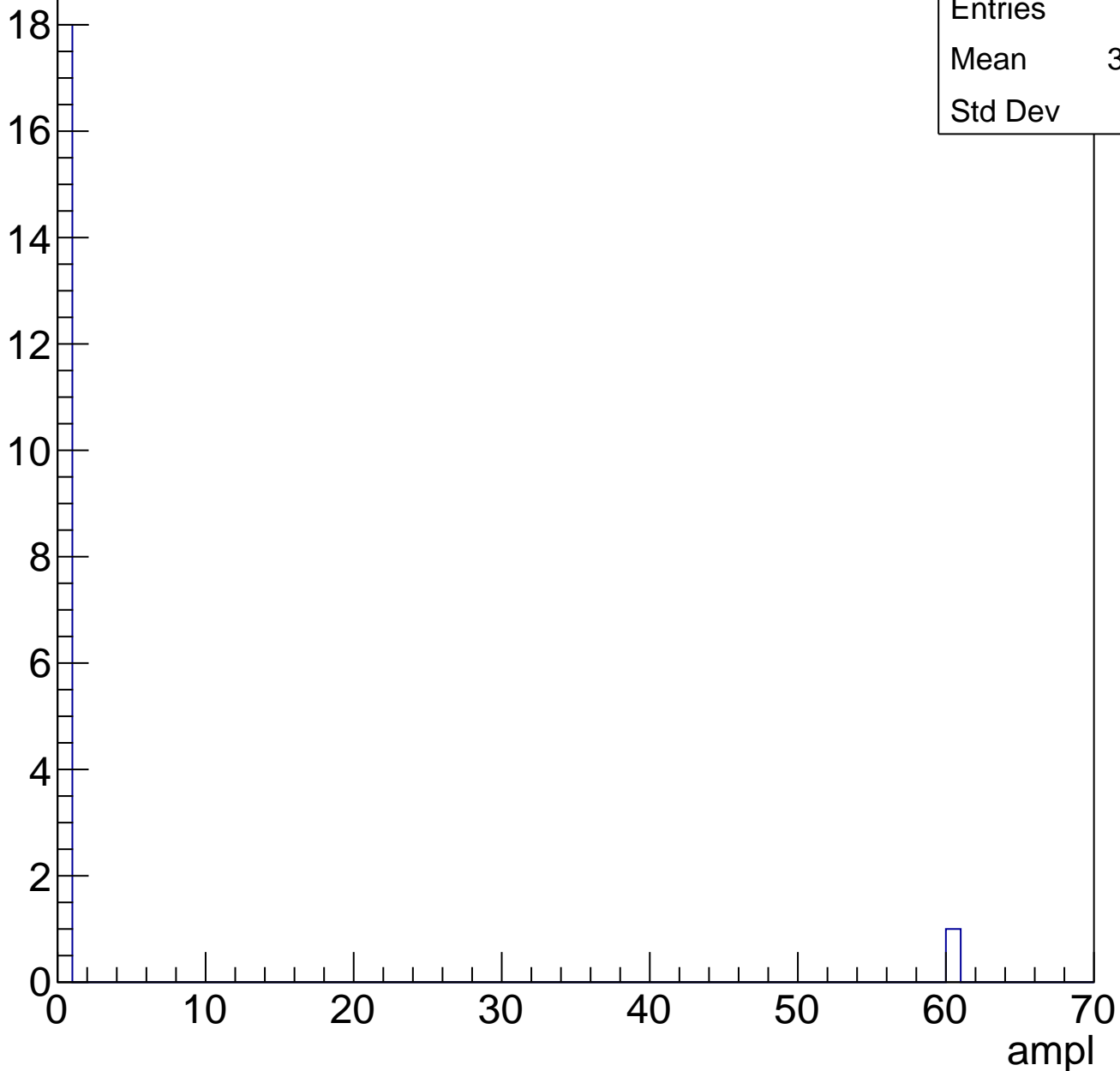


B1L103S, U5-ch35, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	3.158
Std Dev	13.4

Entry

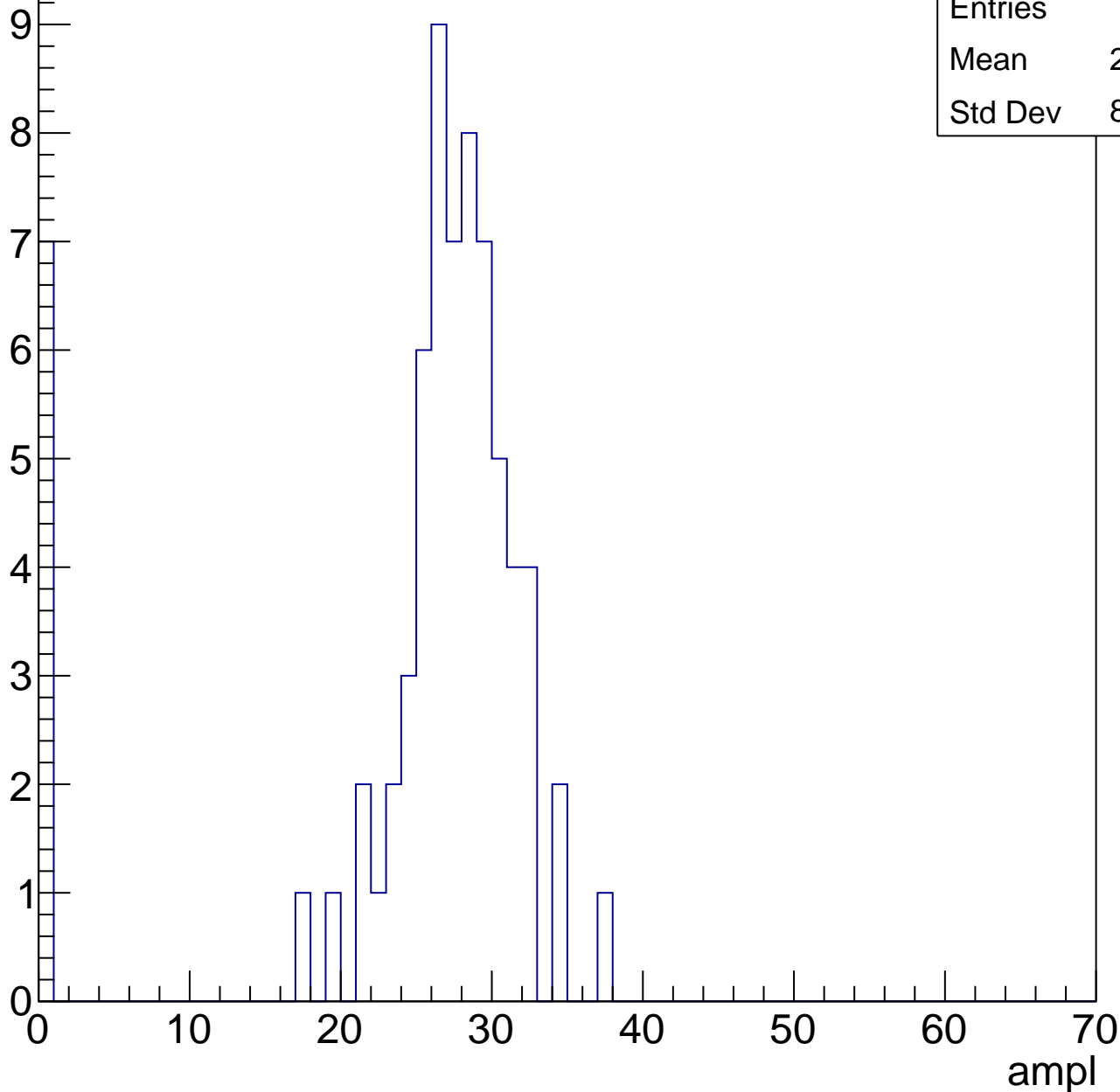


B1L103S, U5-ch36, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	24.64
Std Dev	8.872

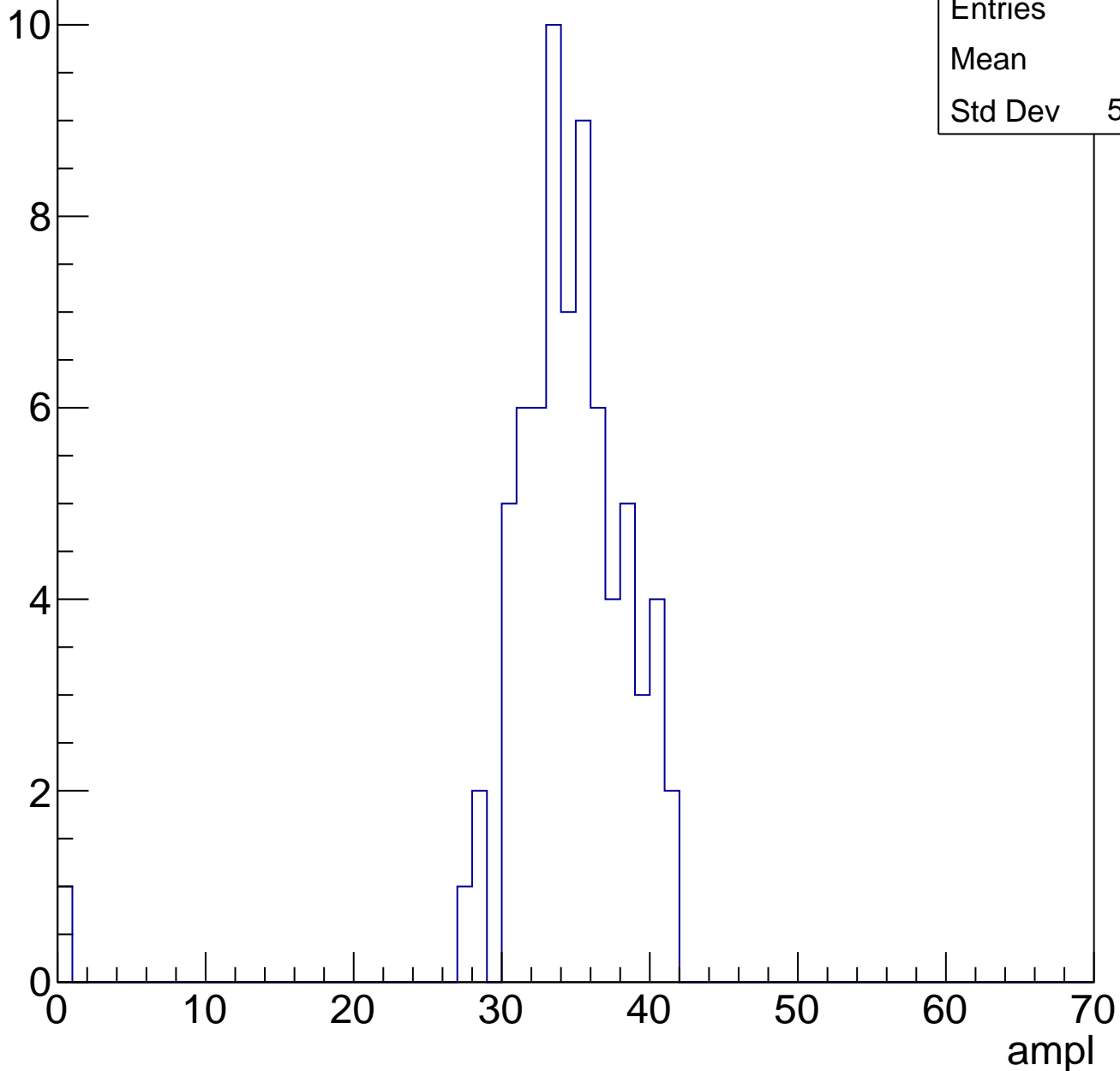


B1L103S, U5-ch36, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	33.9
Std Dev	5.187

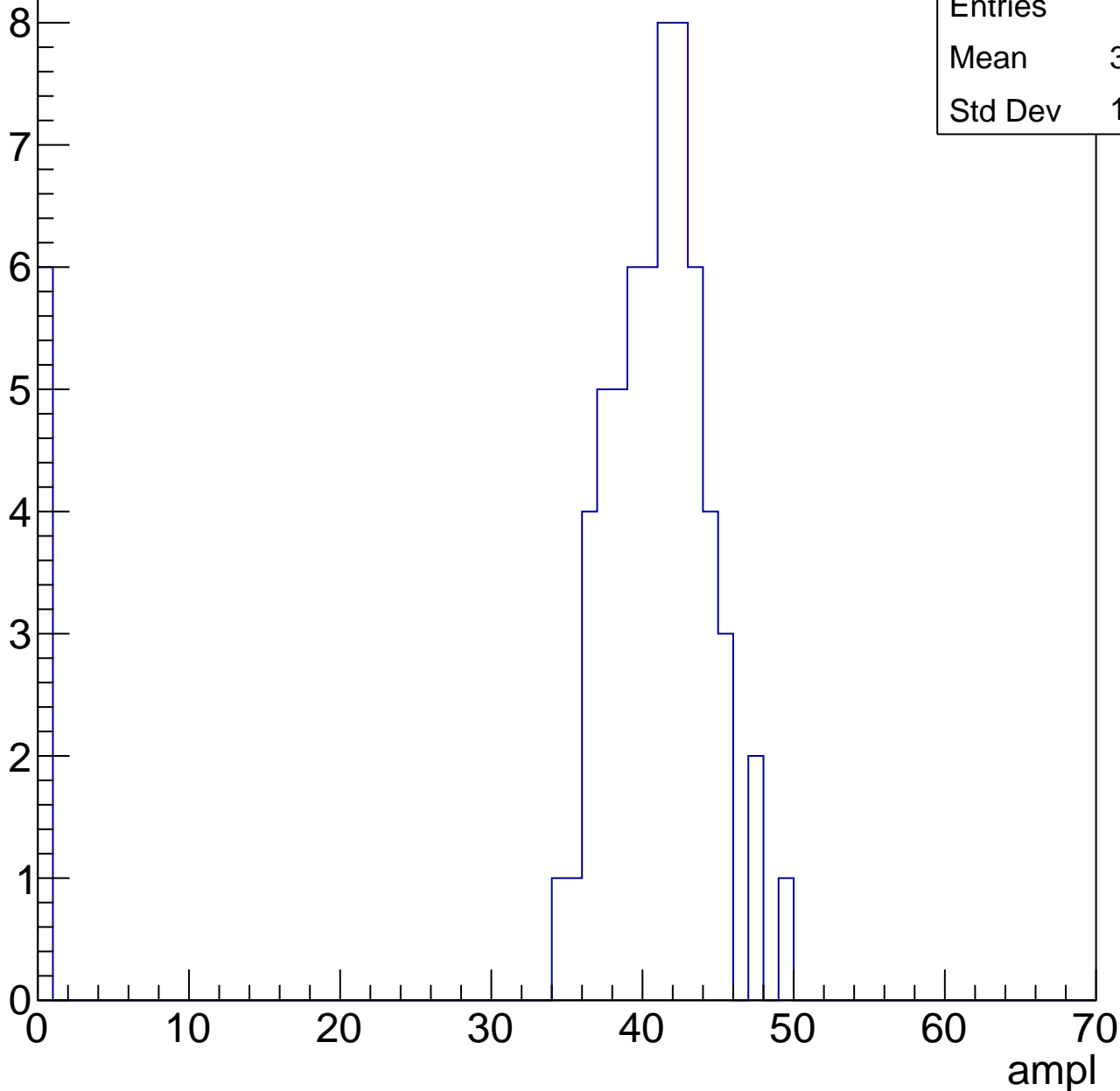


B1L103S, U5-ch36, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

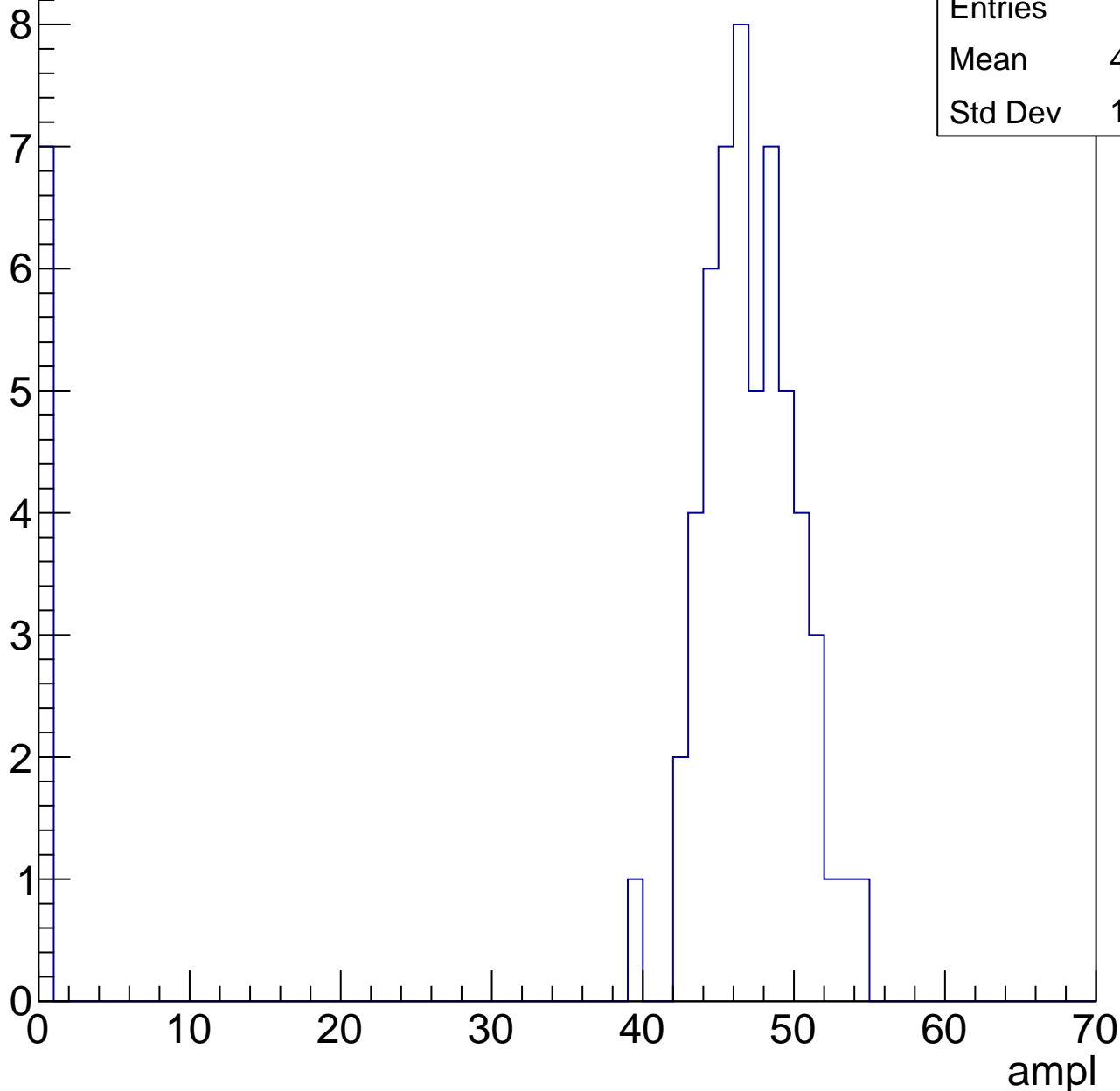
Entries	66
Mean	36.94
Std Dev	12.05



B1L103S, U5-ch36, adc3

calib_packv5_041523_1651.root, FC#0, port C2

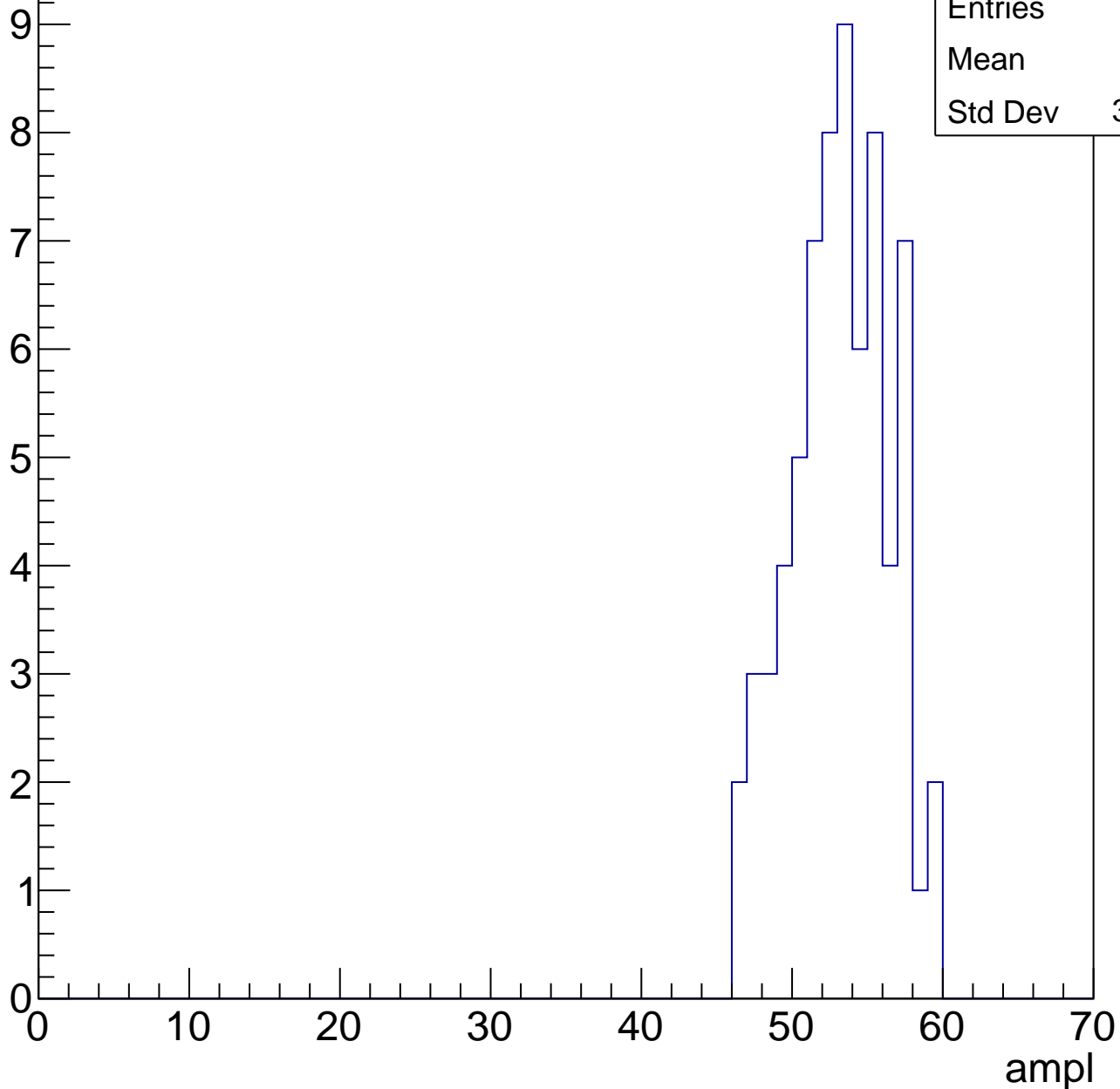
Entry



B1L103S, U5-ch36, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

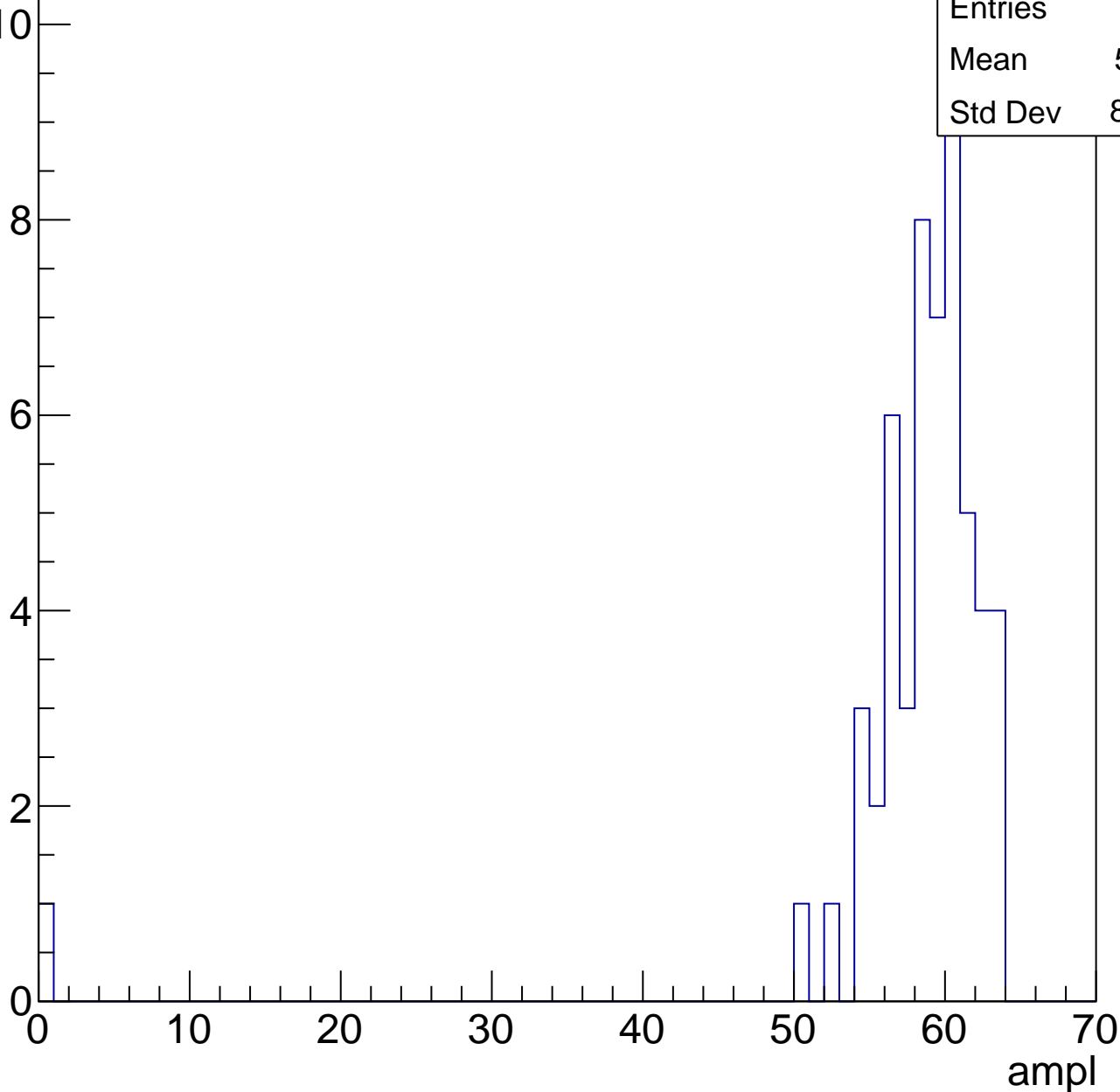


B1L103S, U5-ch36, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	57.51
Std Dev	8.312

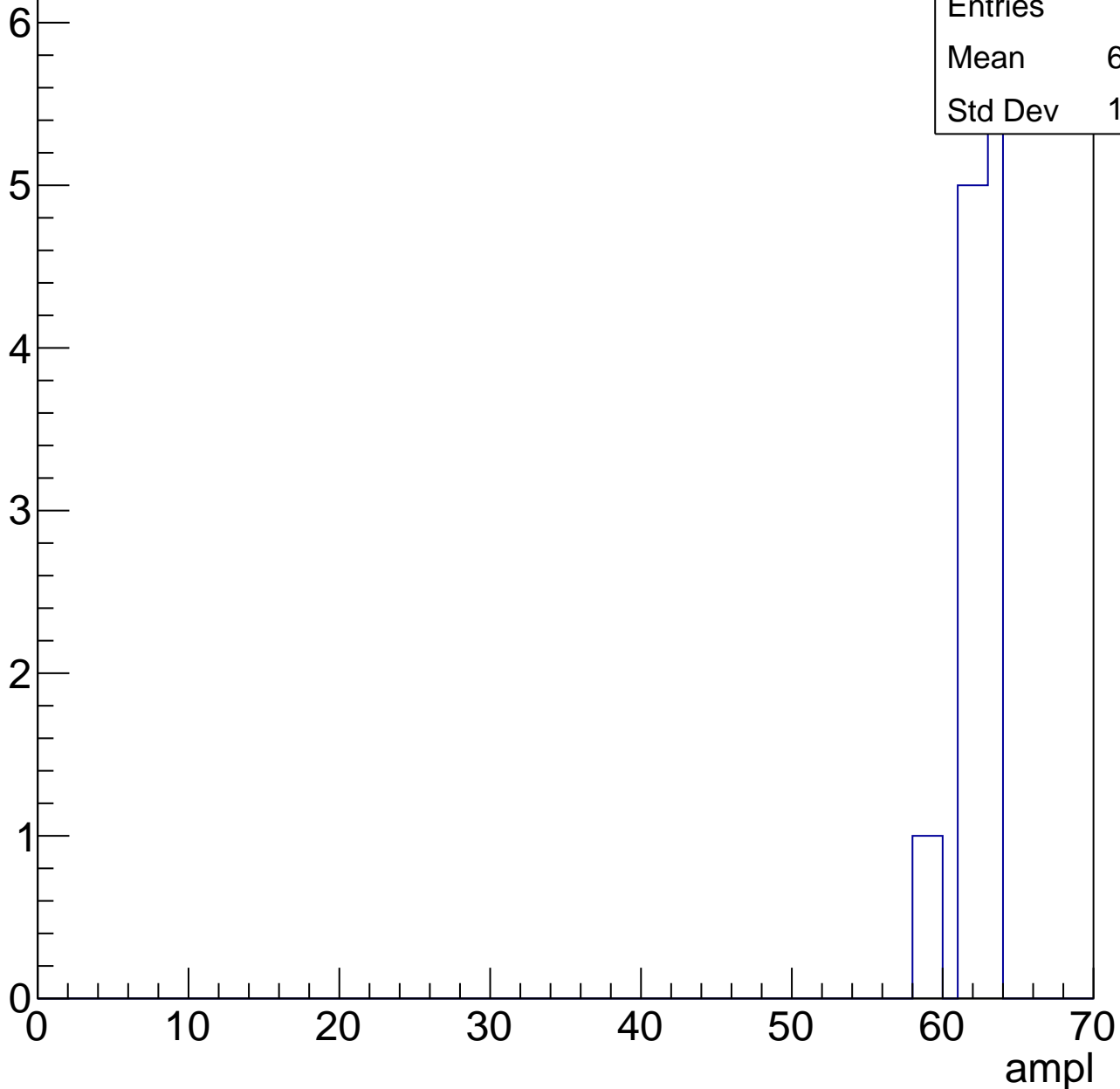


B1L103S, U5-ch36, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	18
Mean	61.67
Std Dev	1.374

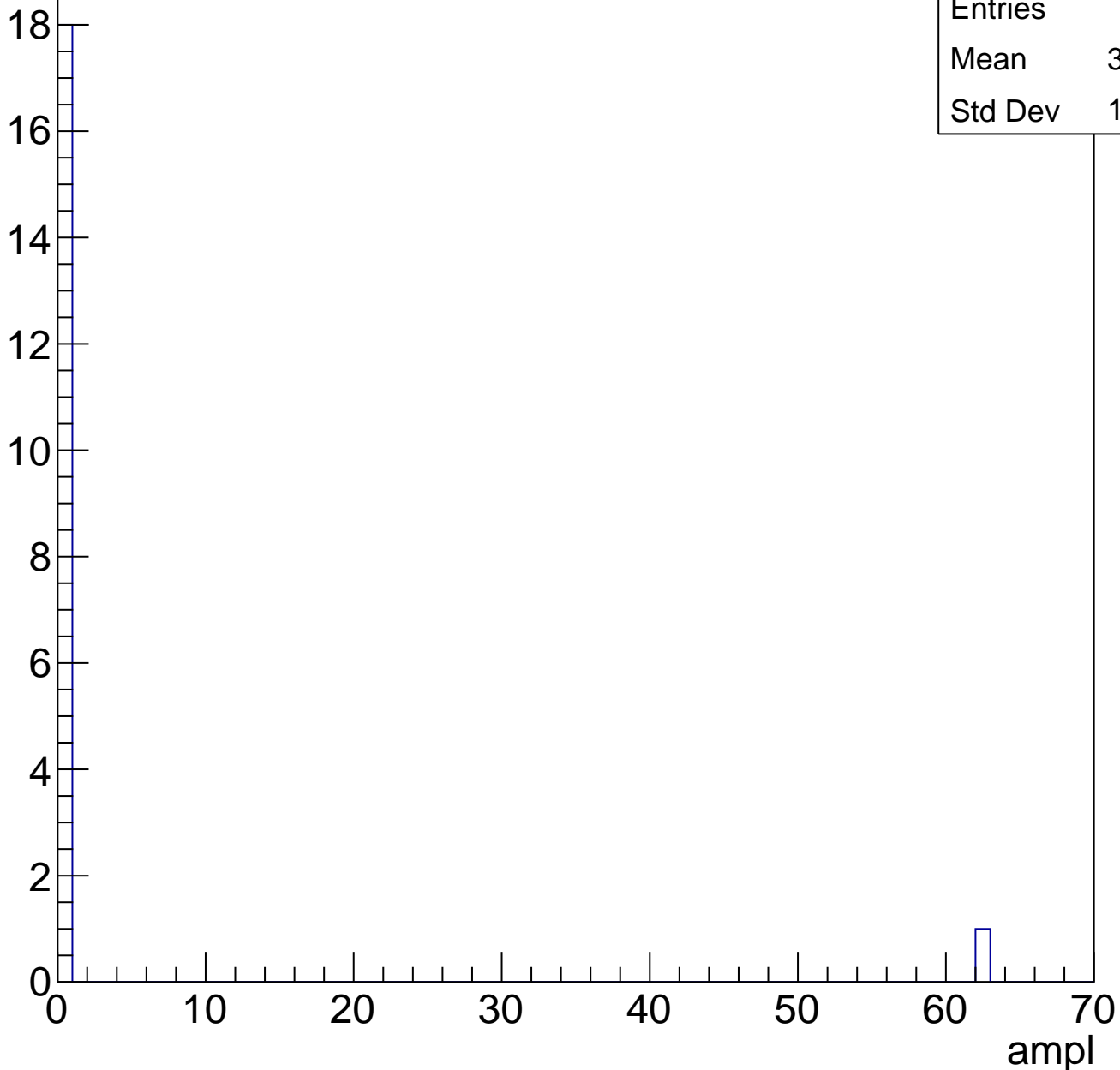


B1L103S, U5-ch36, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	3.263
Std Dev	13.84

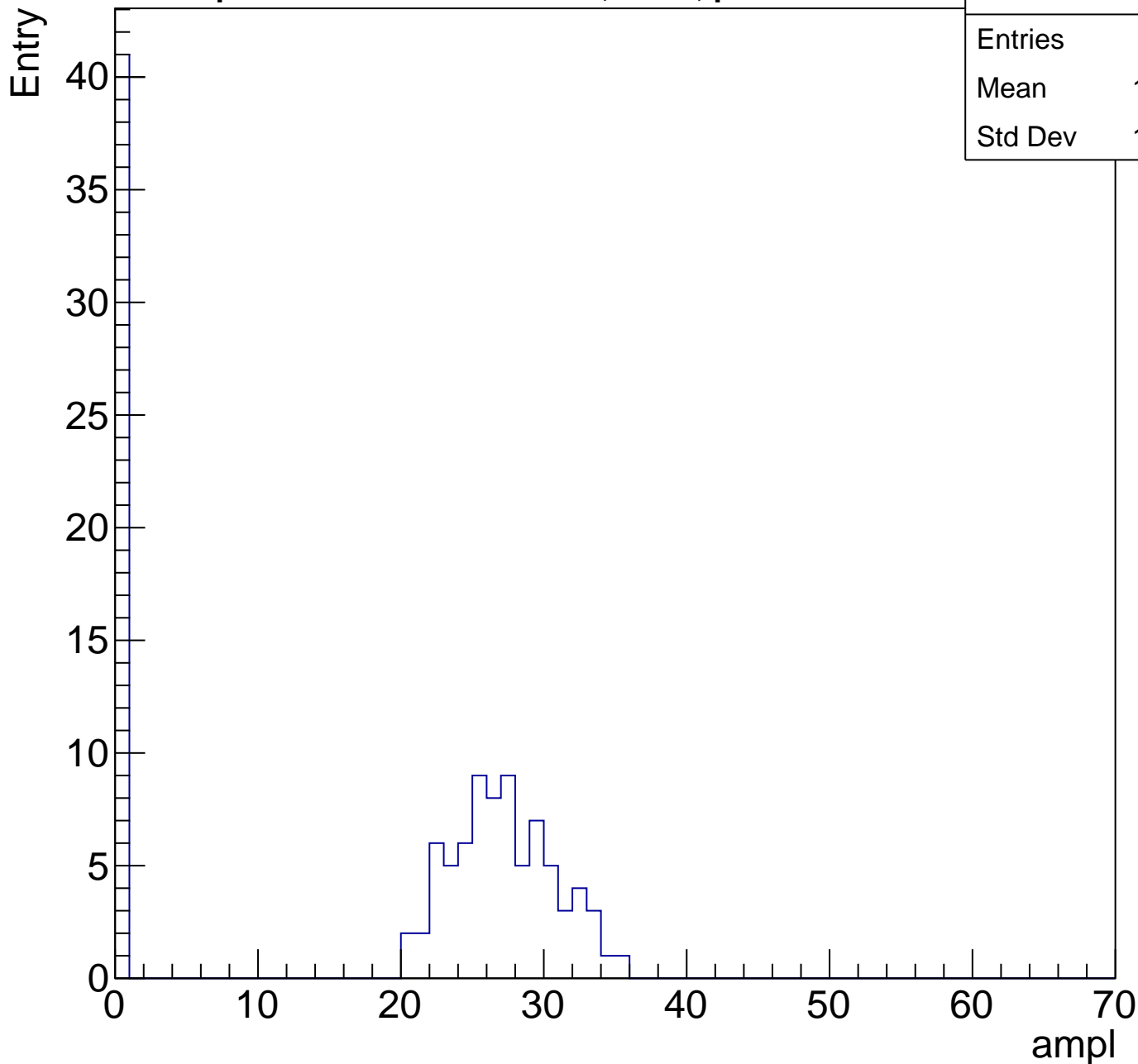
Entry



B1L103S, U5-ch37, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	117
Mean	17.36
Std Dev	13.06



B1L103S, U5-ch37, adc1

calib_packv5_041523_1651.root, FC#0, port C2

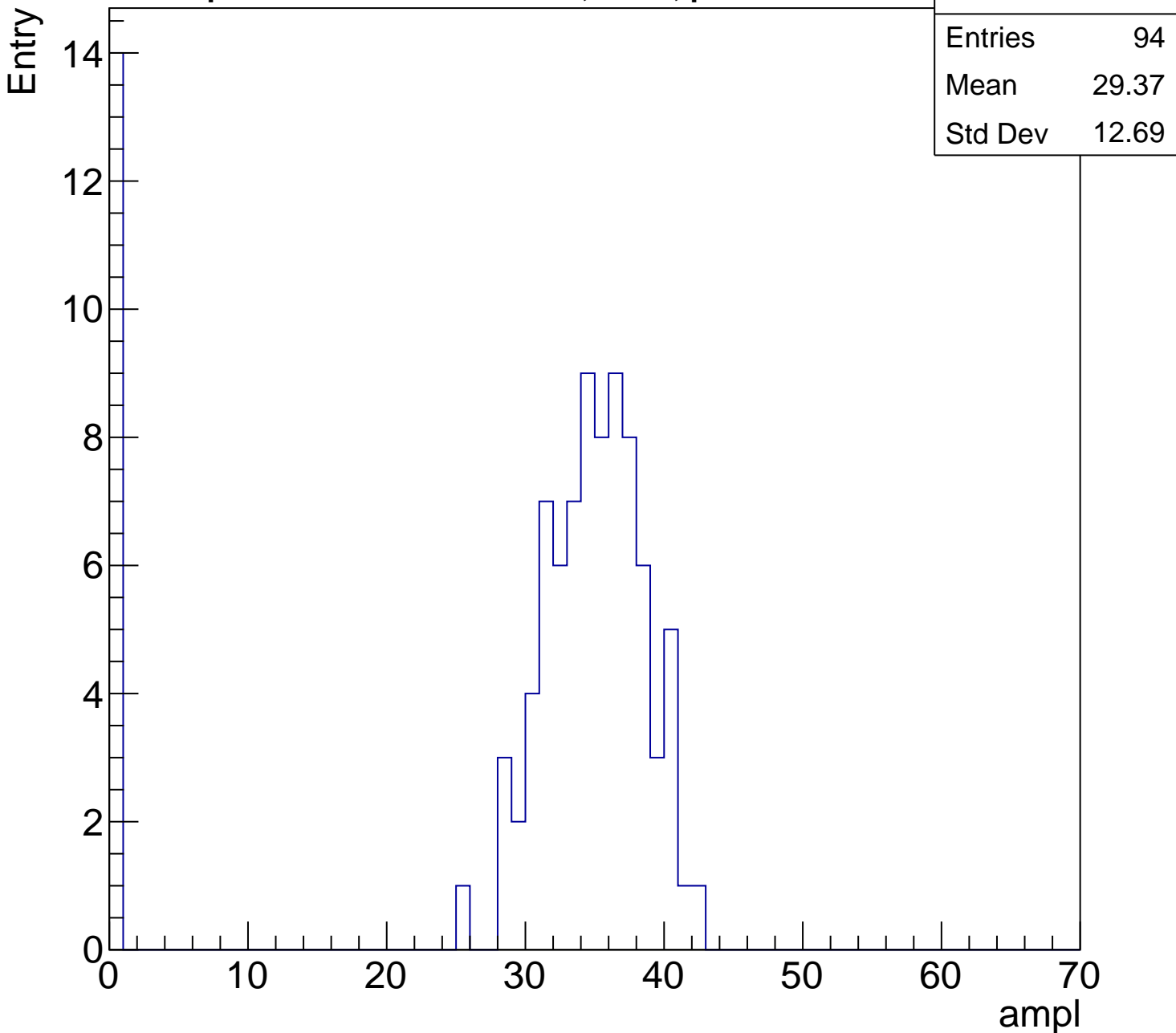
Entries	94
Mean	29.37
Std Dev	12.69

Entry

14
12
10
8
6
4
2
0

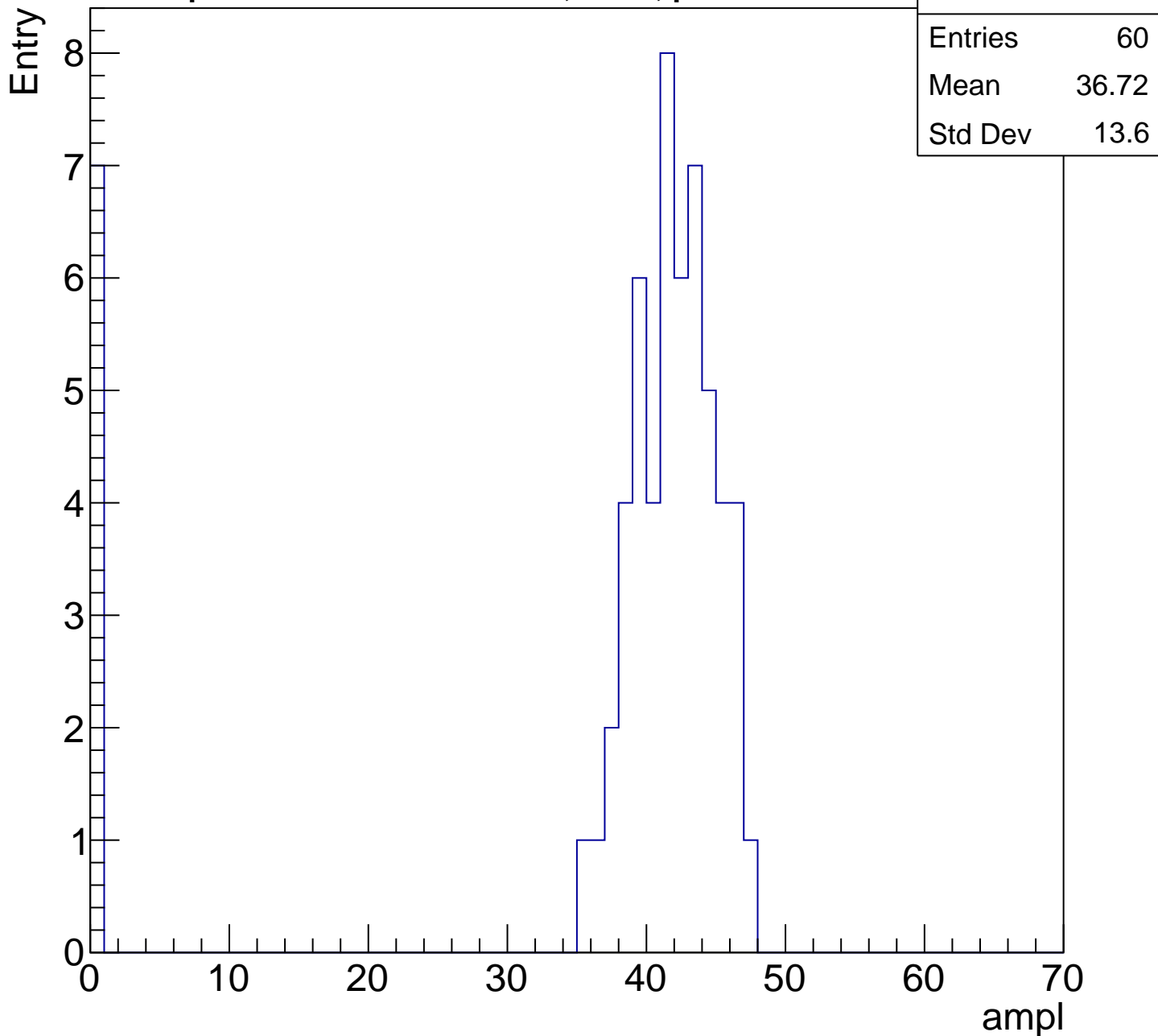
0 10 20 30 40 50 60 70

ampl



B1L103S, U5-ch37, adc2

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U5-ch37, adc3

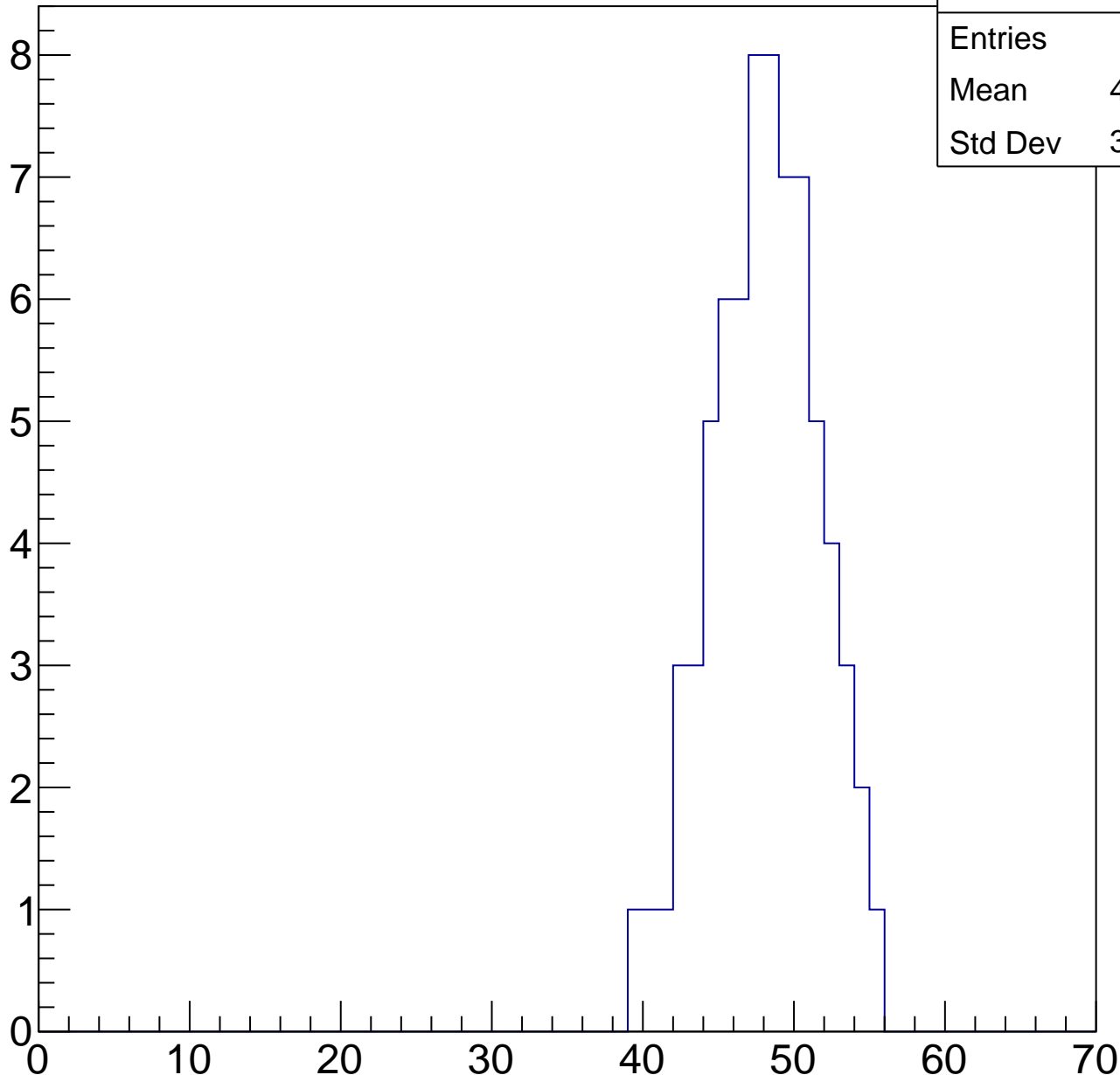
calib_packv5_041523_1651.root, FC#0, port C2

Entry

8
7
6
5
4
3
2
1
0

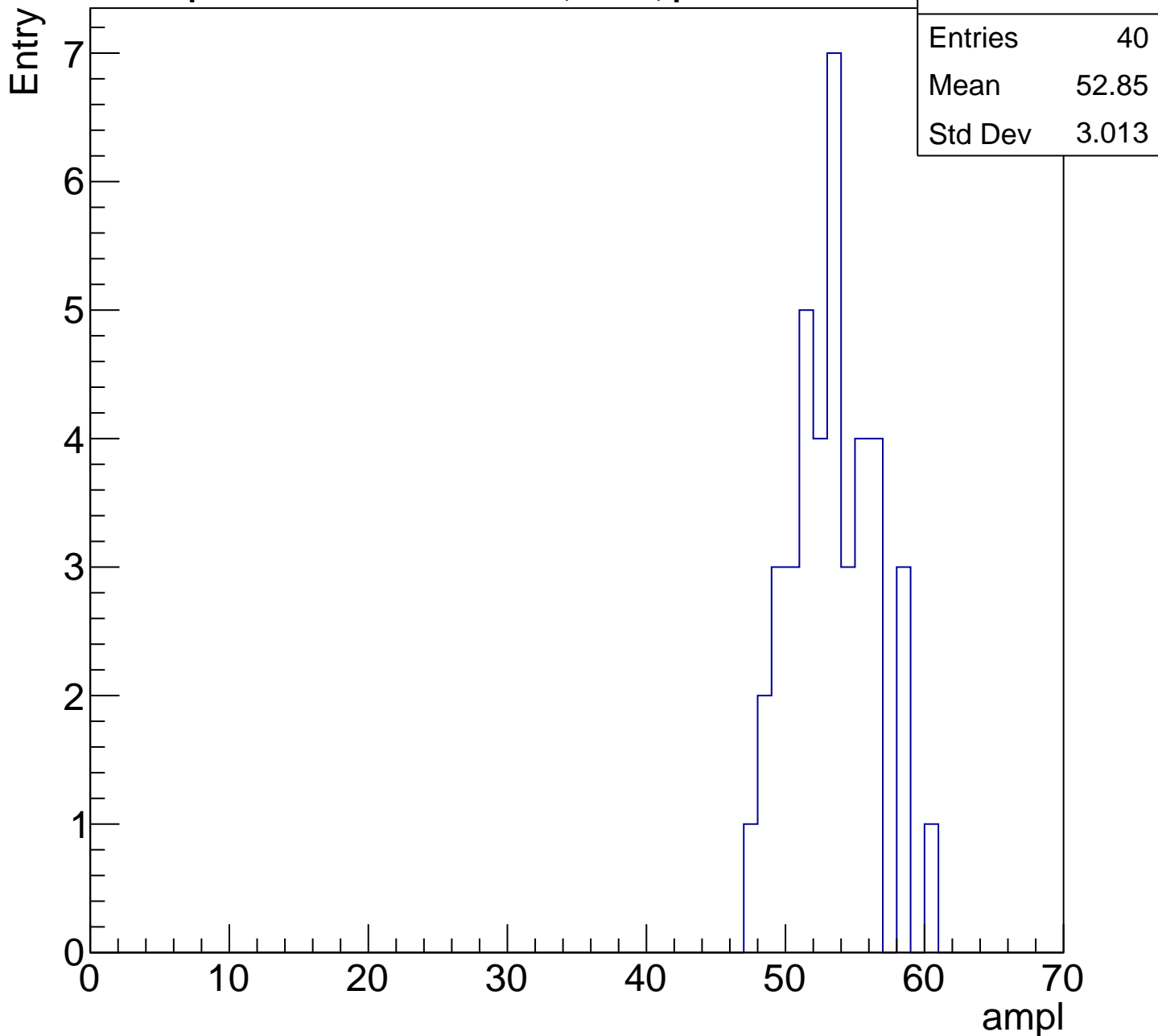
Entries	71
Mean	47.59
Std Dev	3.503

ampl



B1L103S, U5-ch37, adc4

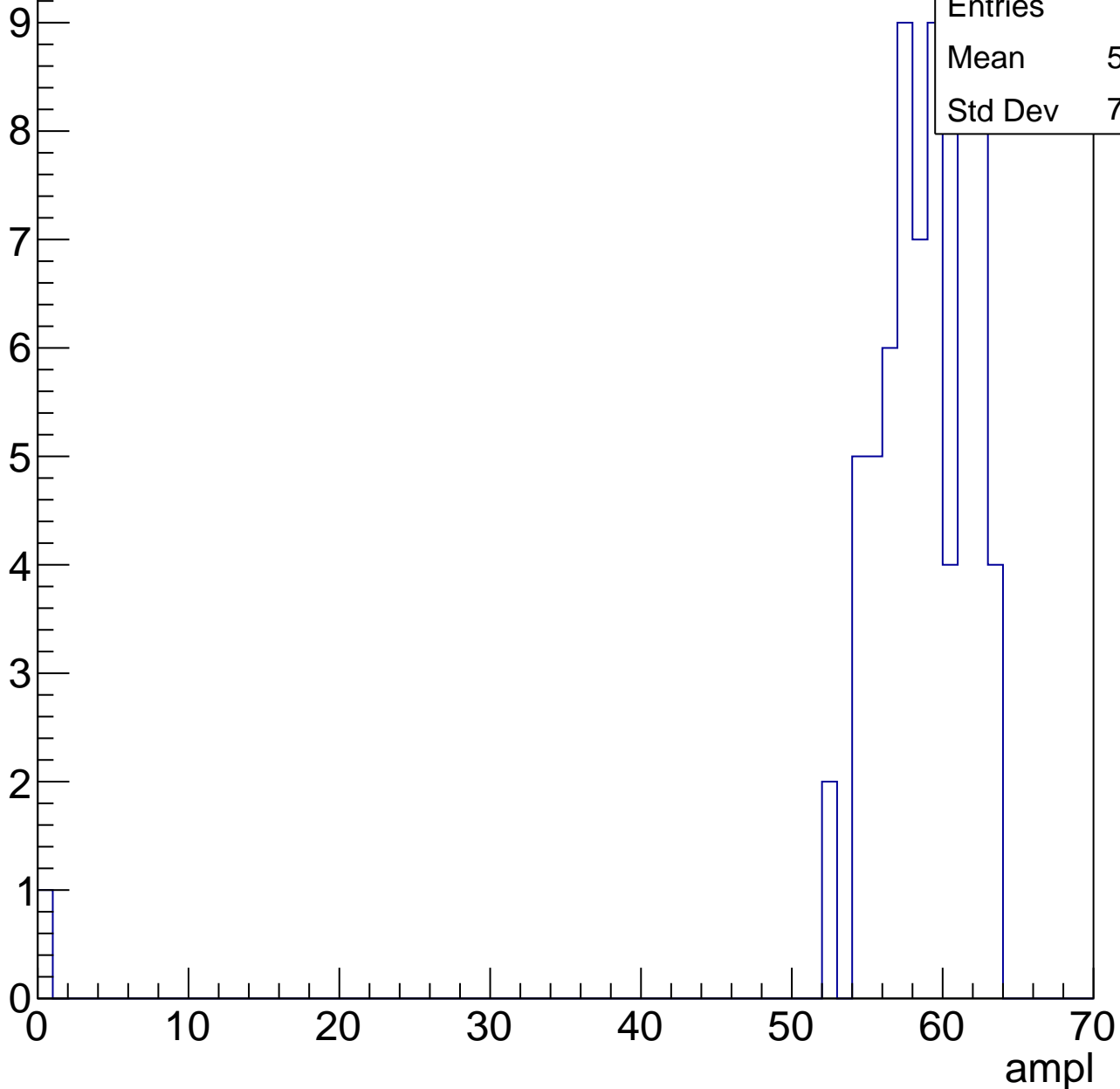
calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U5-ch37, adc5

calib_packv5_041523_1651.root, FC#0, port C2

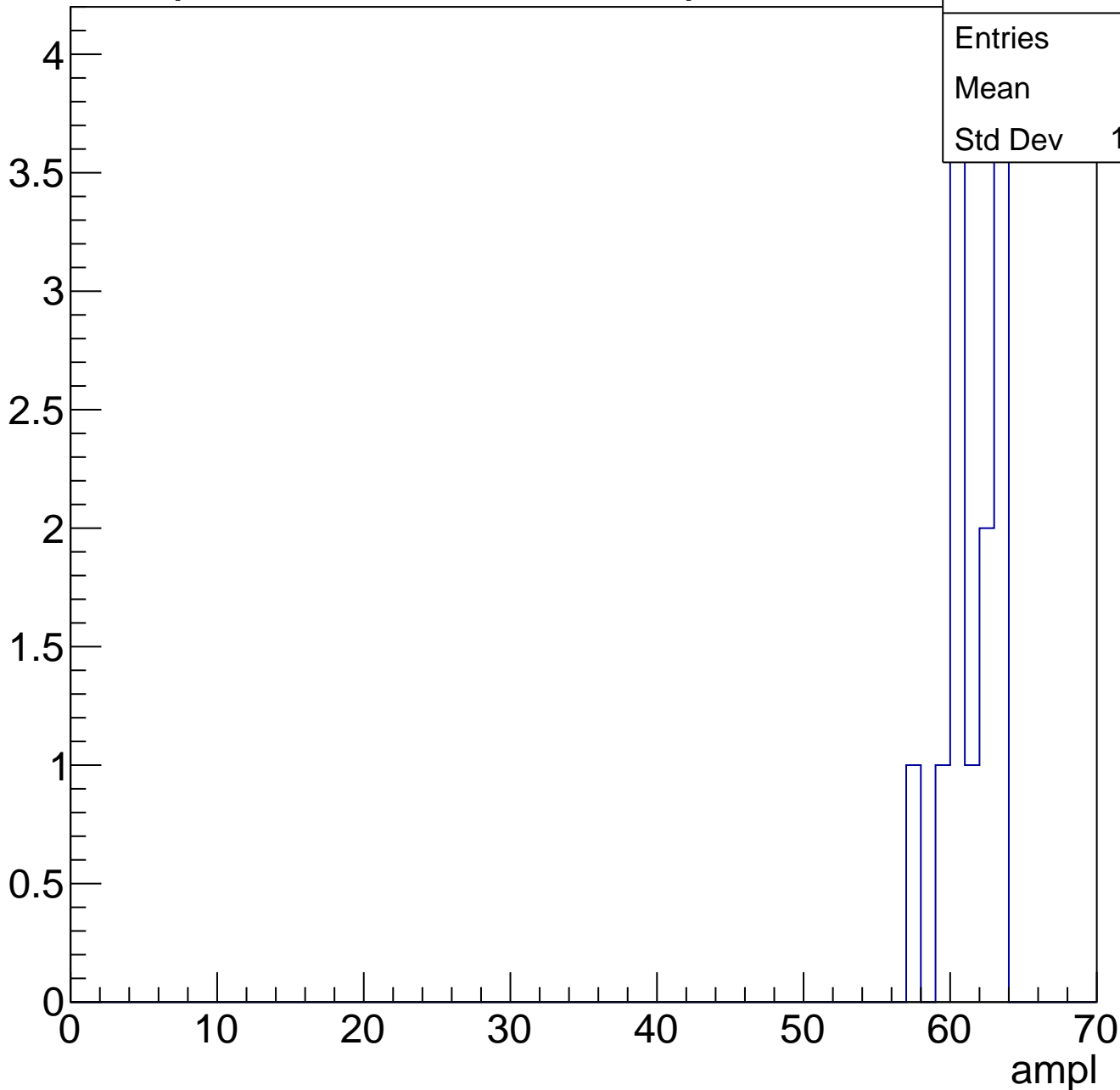
Entry



B1L103S, U5-ch37, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

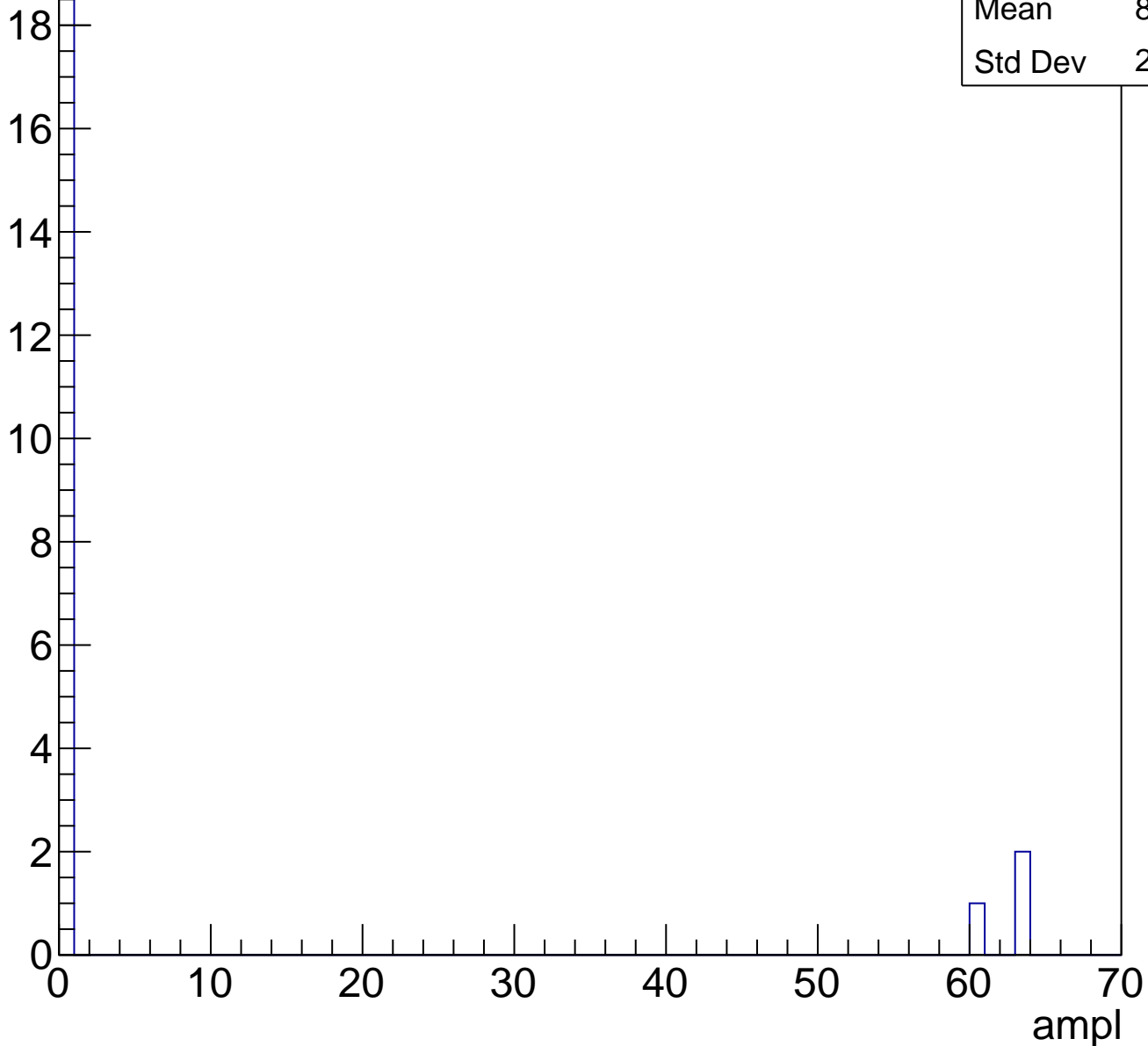


B1L103S, U5-ch37, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	22
Mean	8.455
Std Dev	21.28

Entry

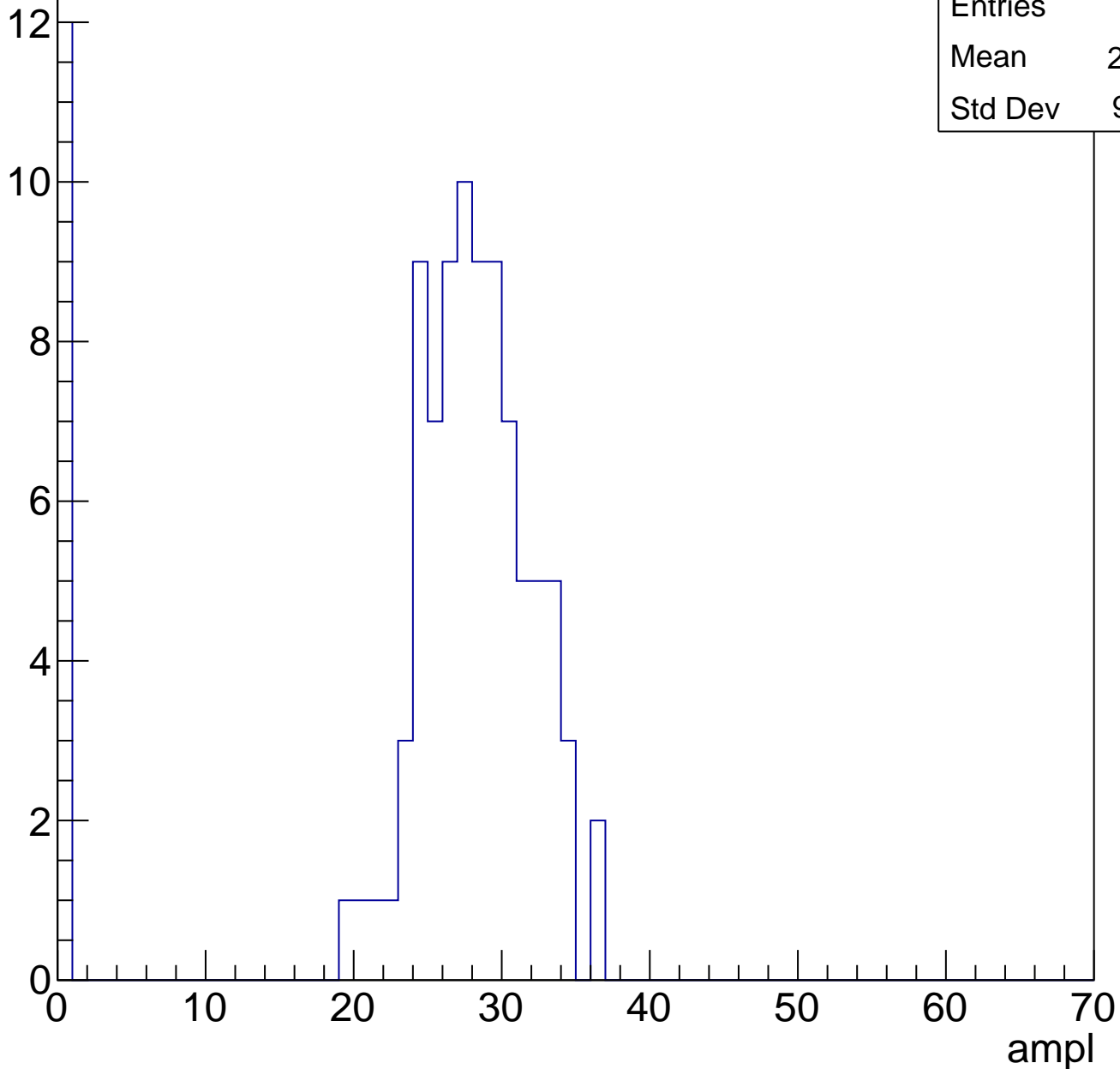


B1L103S, U5-ch38, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	99
Mean	24.47
Std Dev	9.671

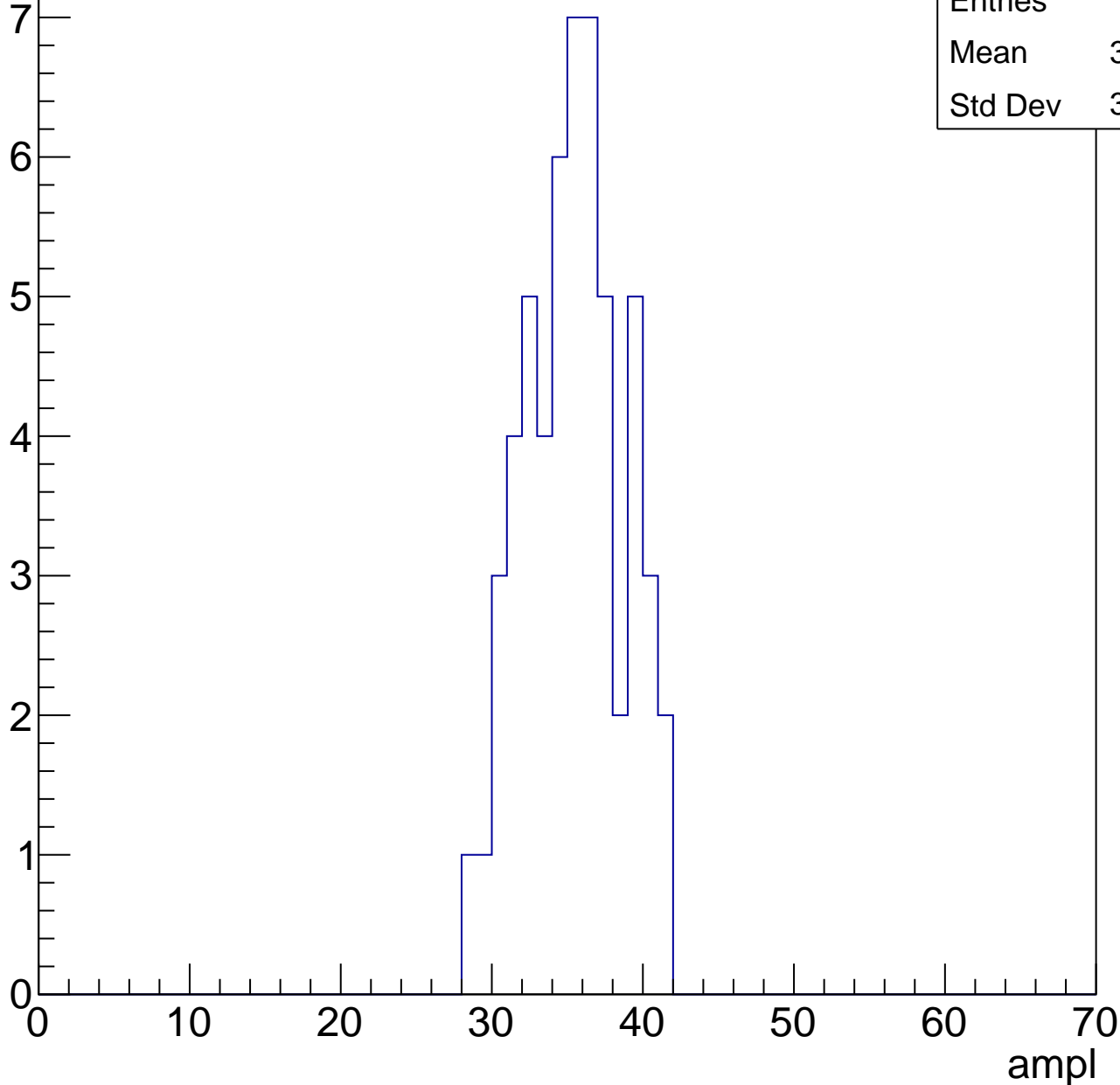
Entry



B1L103S, U5-ch38, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

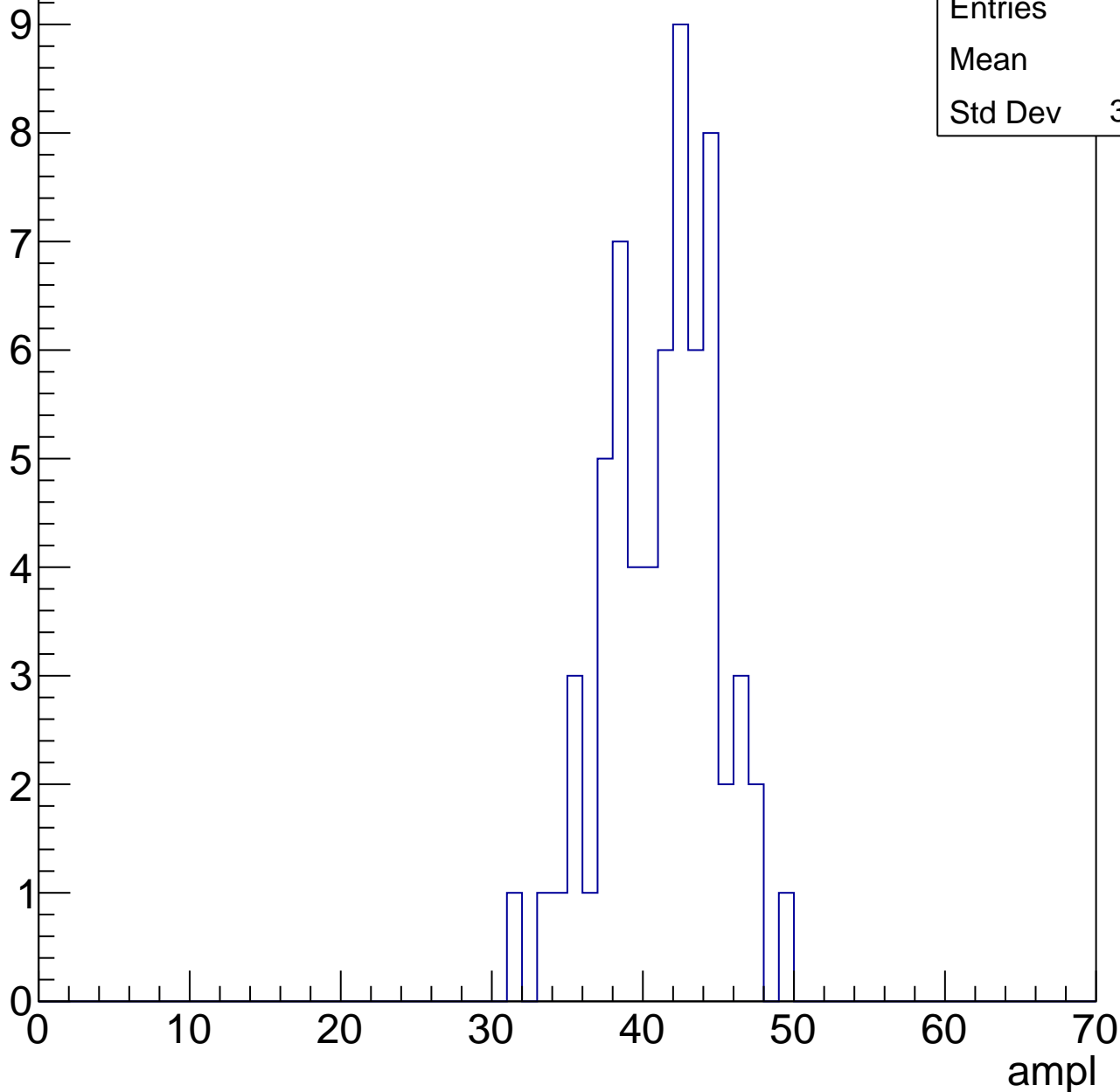


B1L103S, U5-ch38, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	40.8
Std Dev	3.654

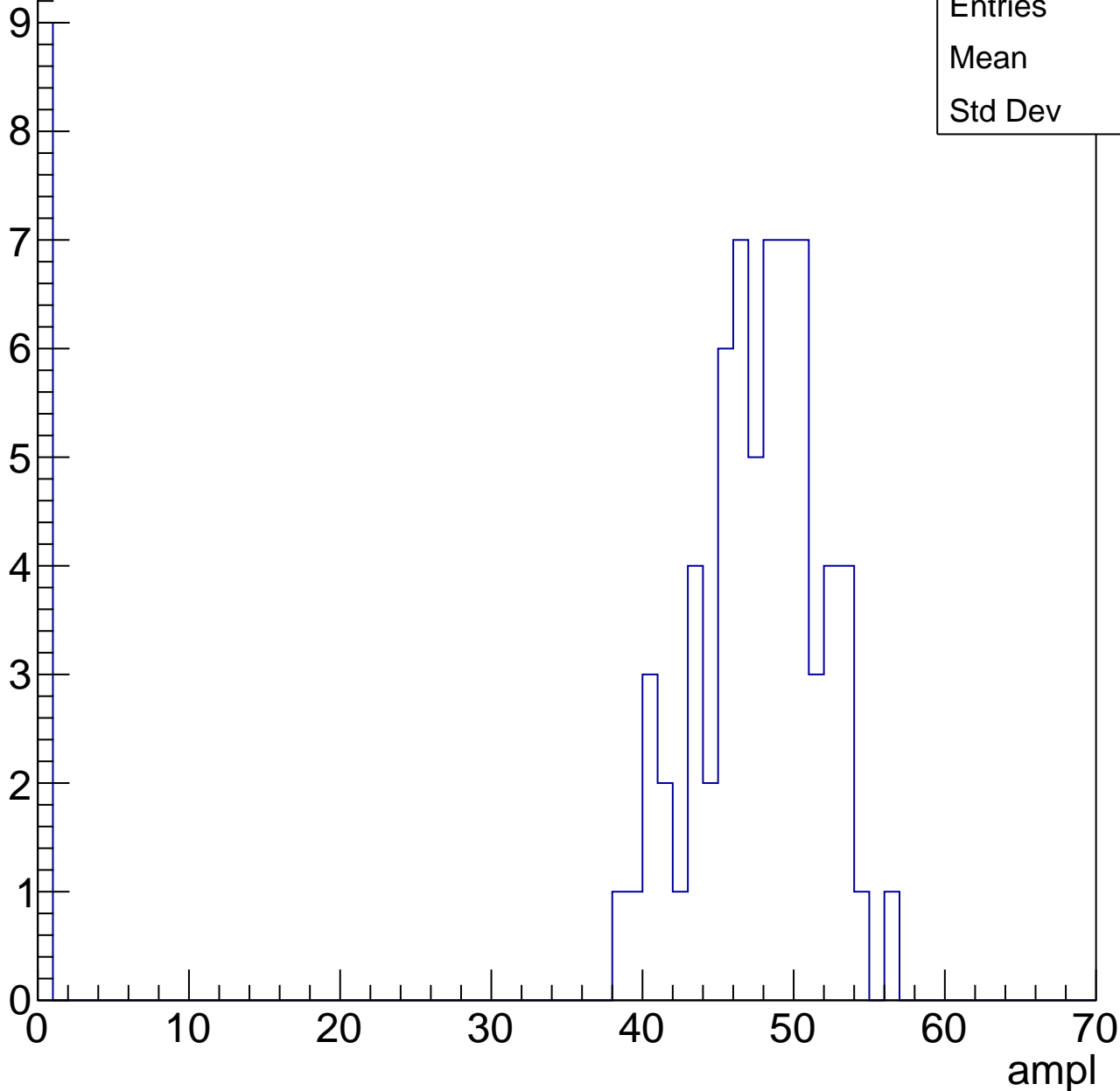


B1L103S, U5-ch38, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	41.6
Std Dev	15.8

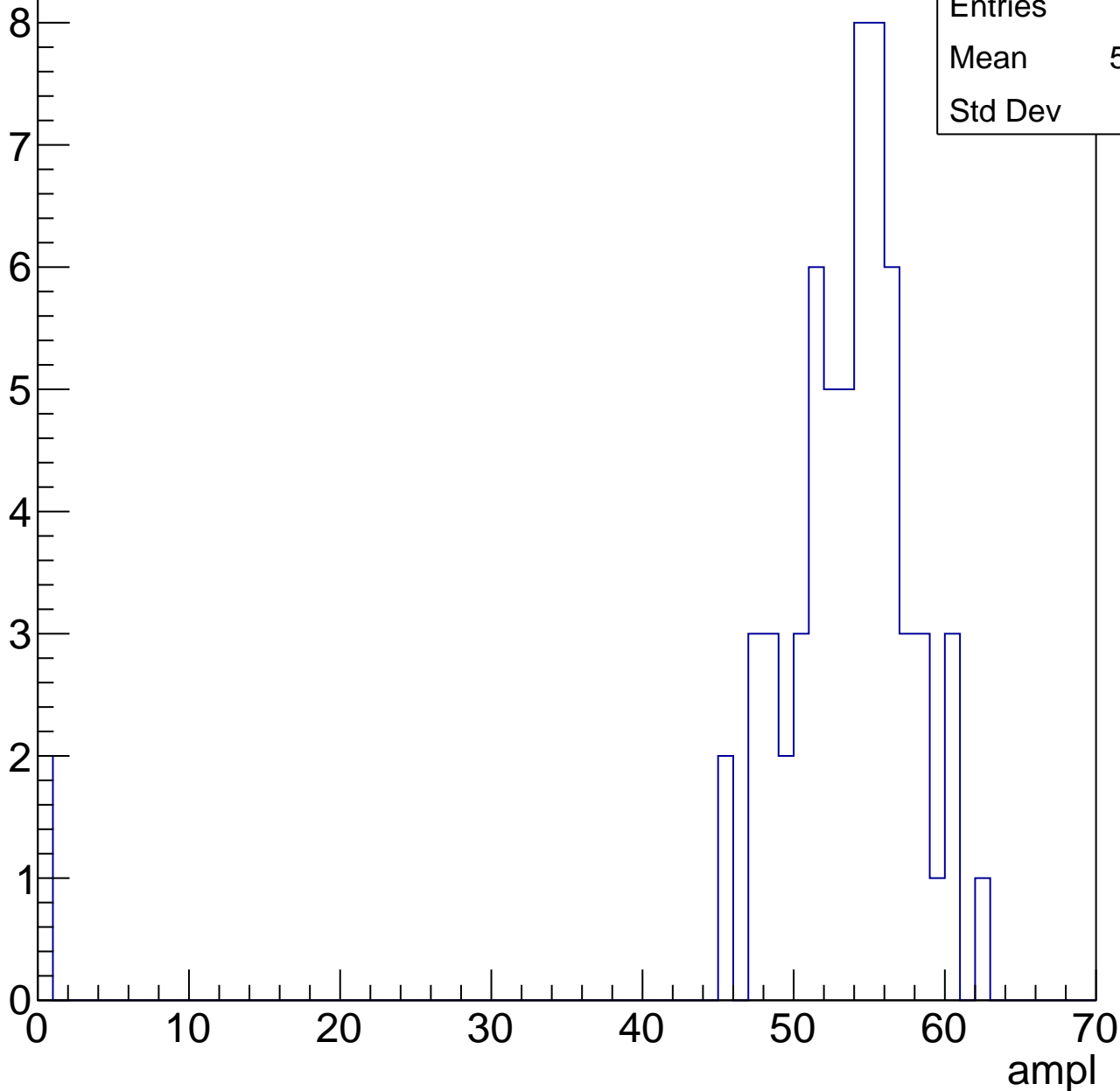


B1L103S, U5-ch38, adc4

calib_packv5_041523_1651.root, FC#0, port C2

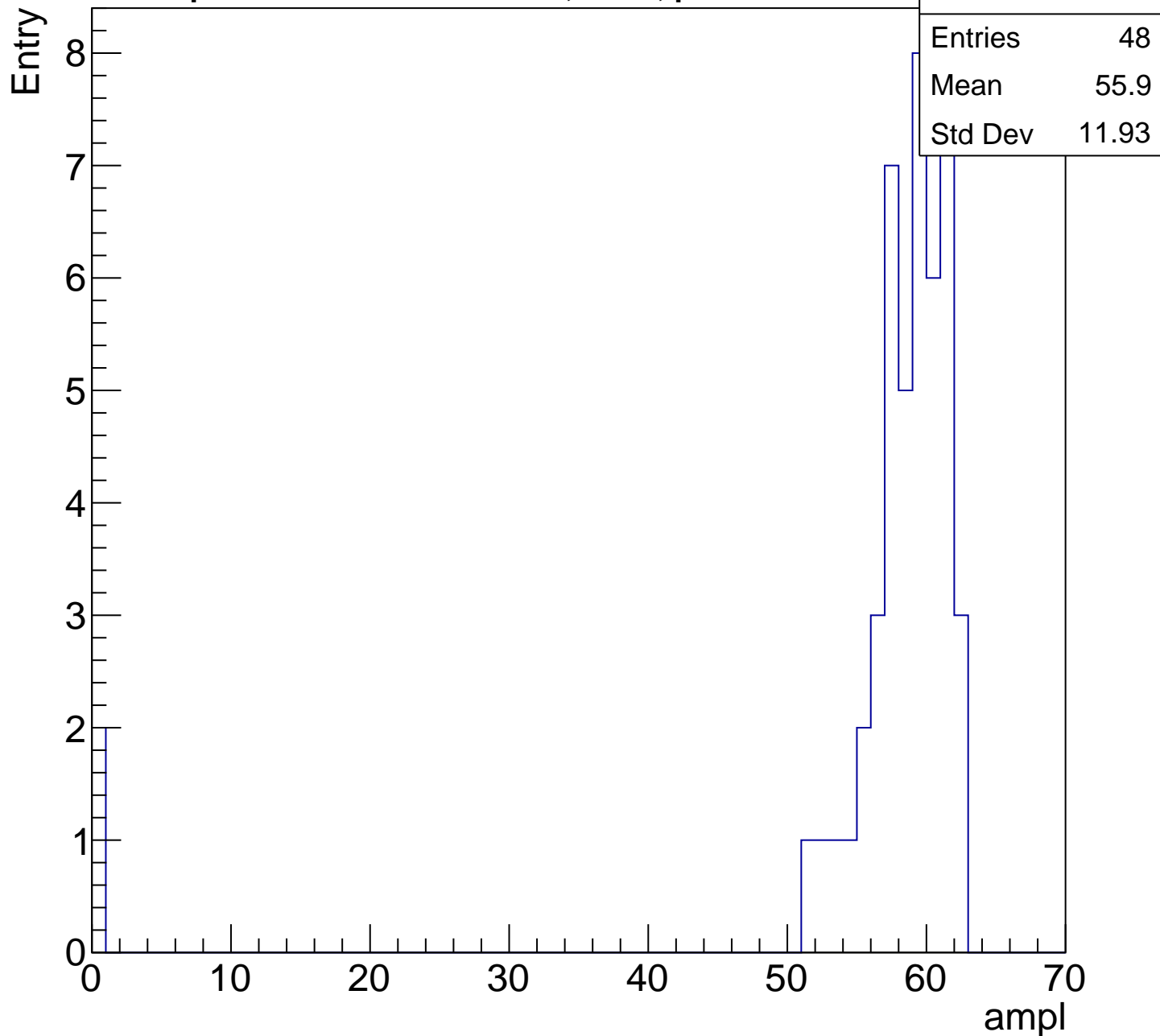
Entry

Entries	64
Mean	51.69
Std Dev	9.99



B1L103S, U5-ch38, adc5

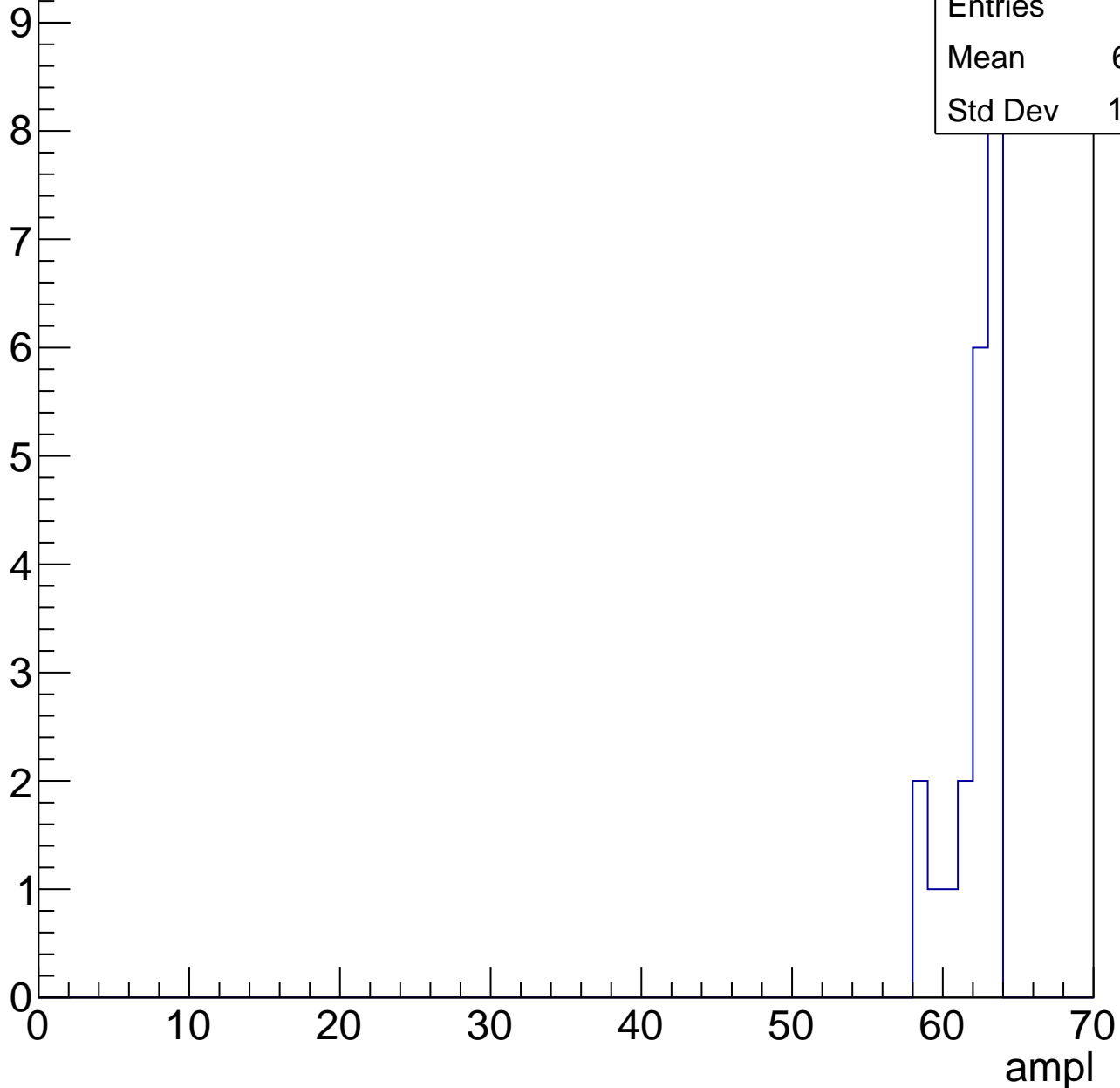
calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U5-ch38, adc6

calib_packv5_041523_1651.root, FC#0, port C2

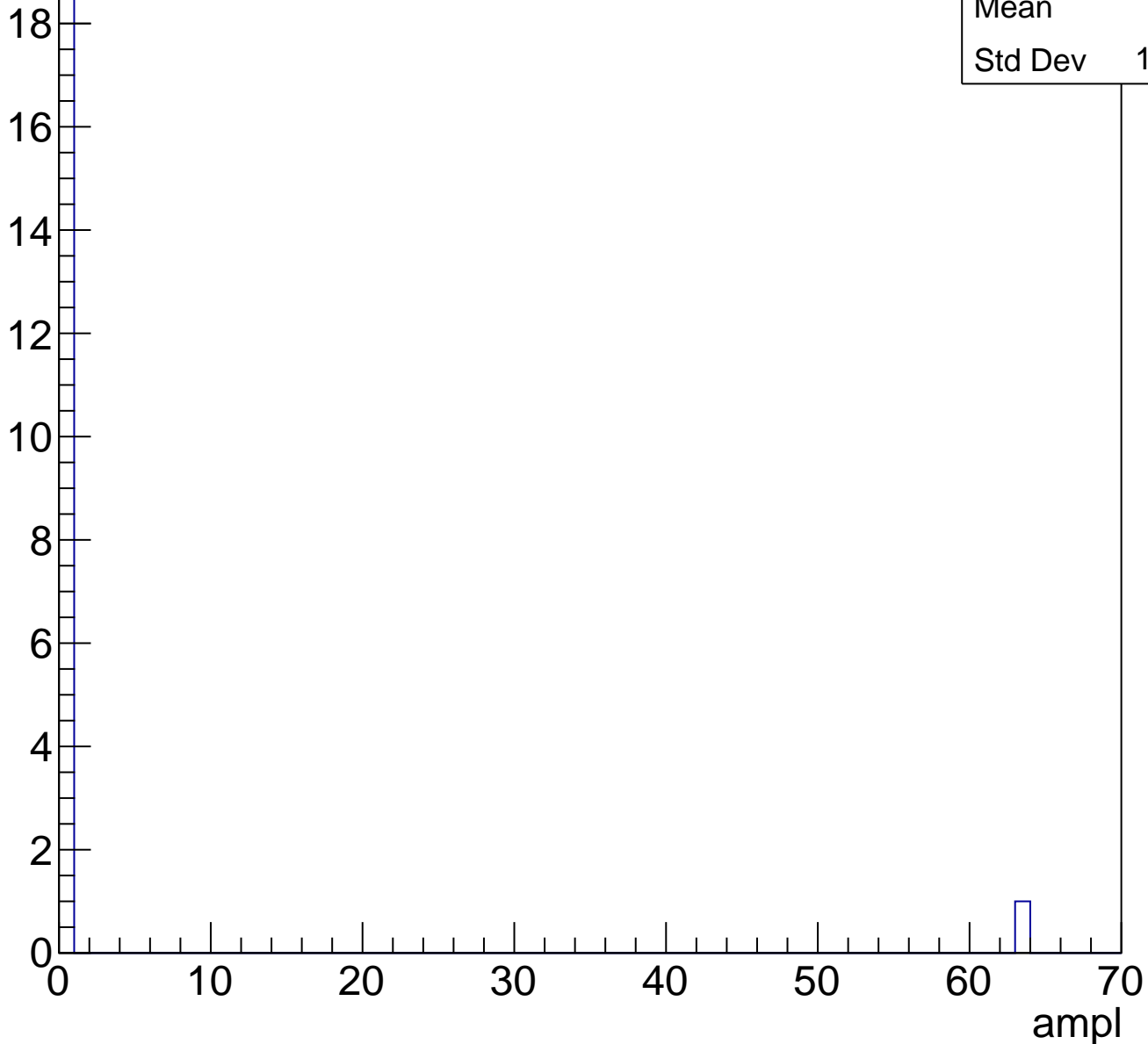
Entry



B1L103S, U5-ch38, adc7

calib_packv5_041523_1651.root, FC#0, port C2

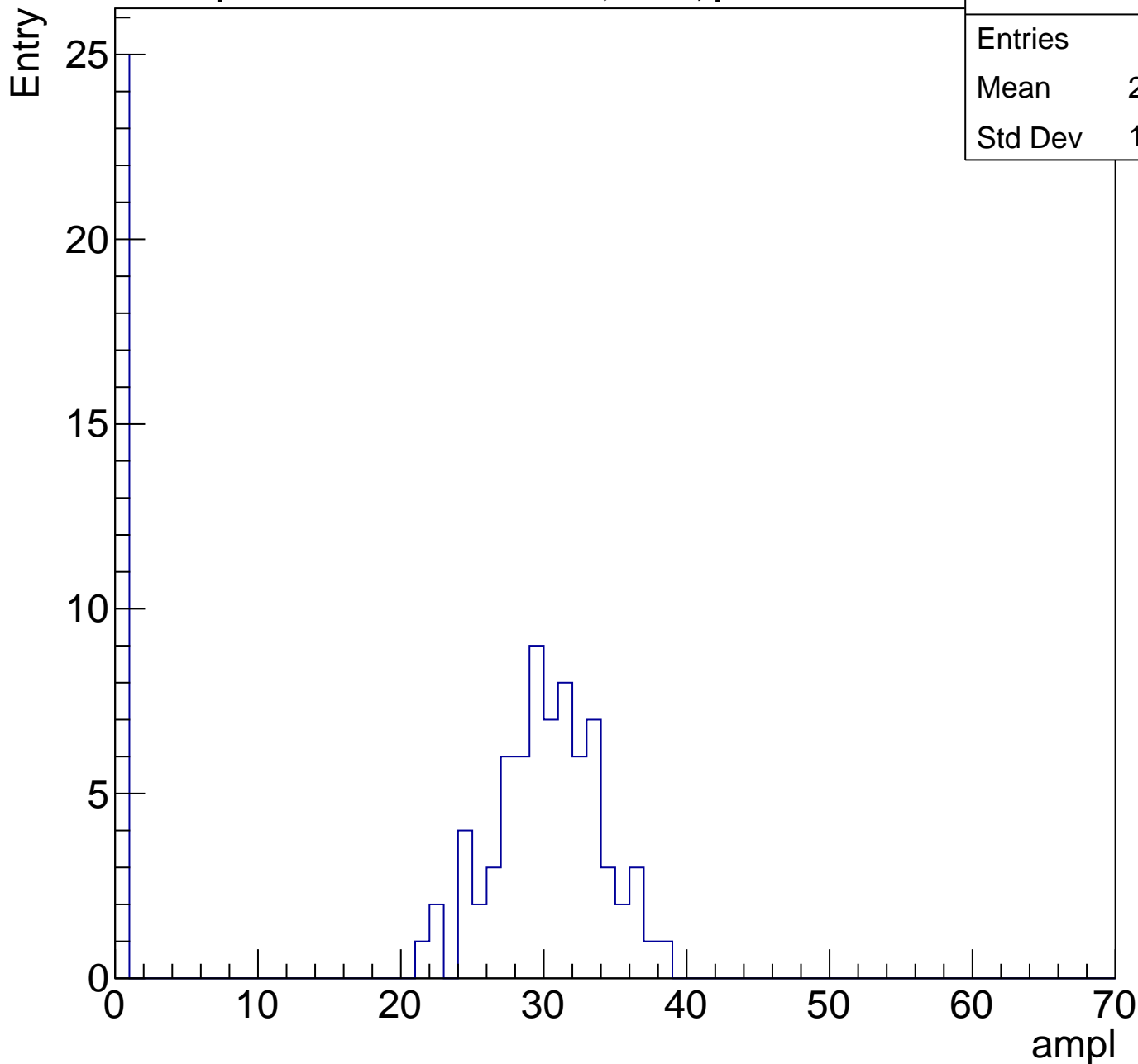
Entry



B1L103S, U5-ch39, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	96
Mean	22.04
Std Dev	13.45

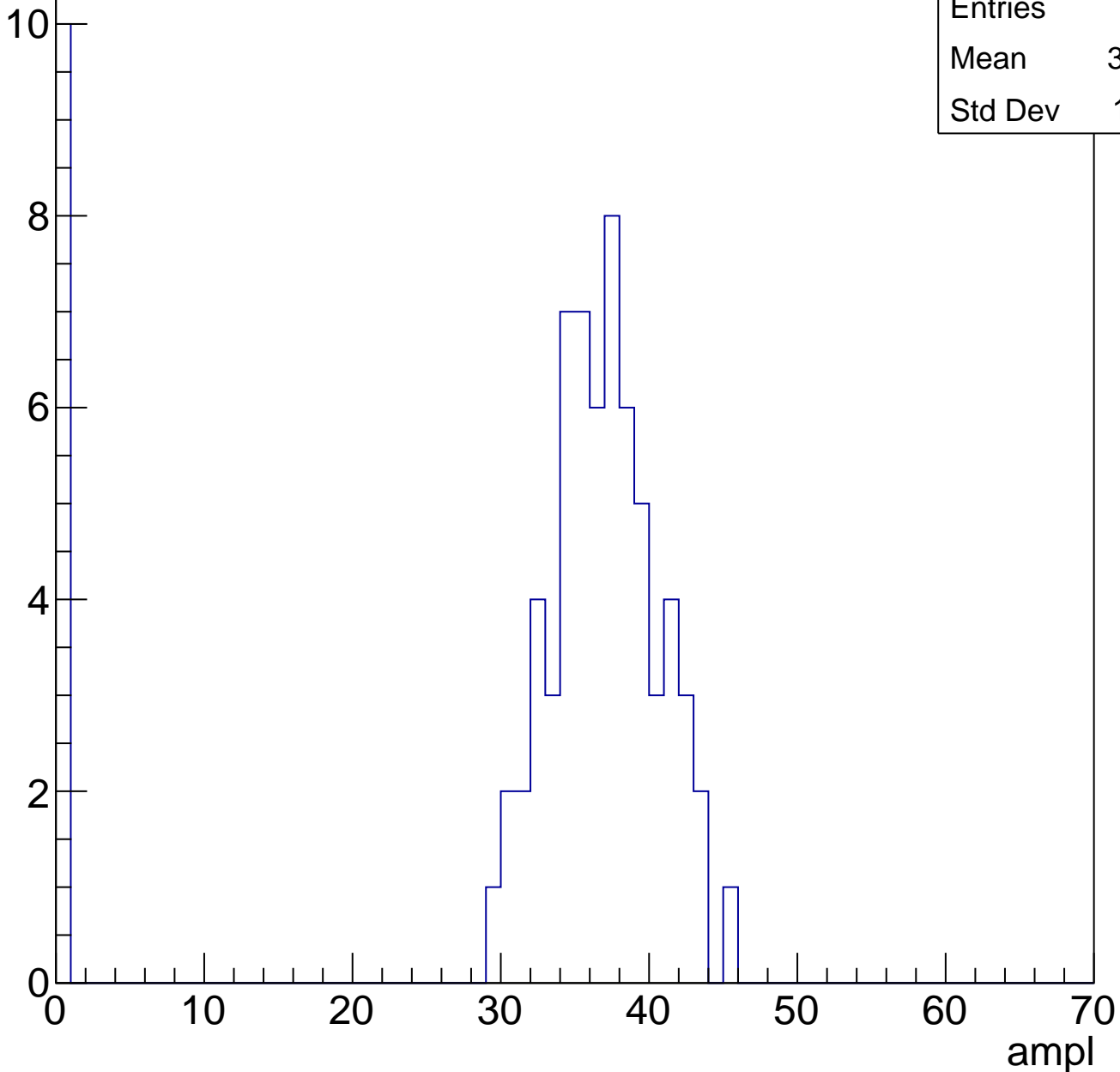


B1L103S, U5-ch39, adc1

calib_packv5_041523_1651.root, FC#0, port C2

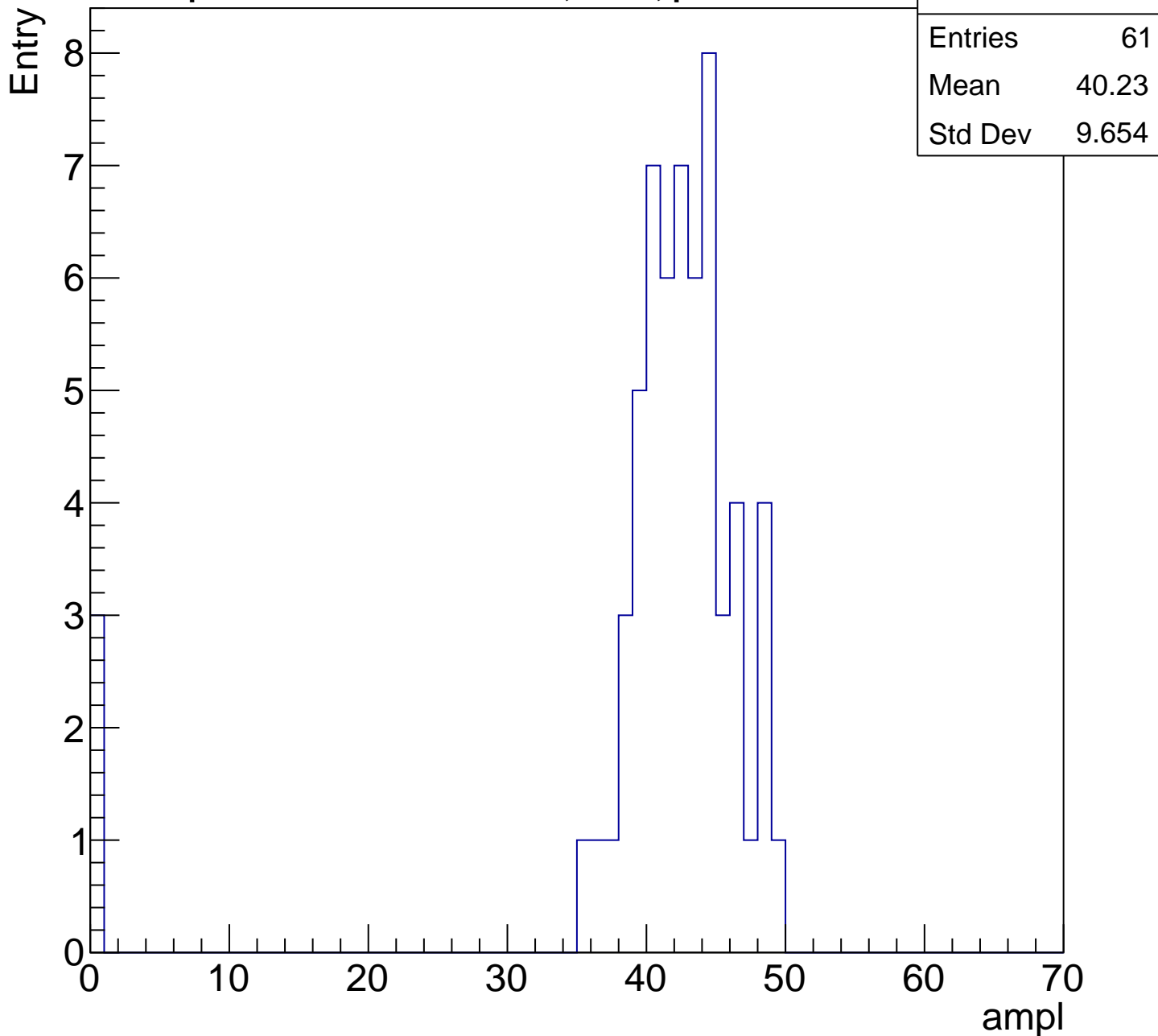
Entries	74
Mean	31.58
Std Dev	12.91

Entry



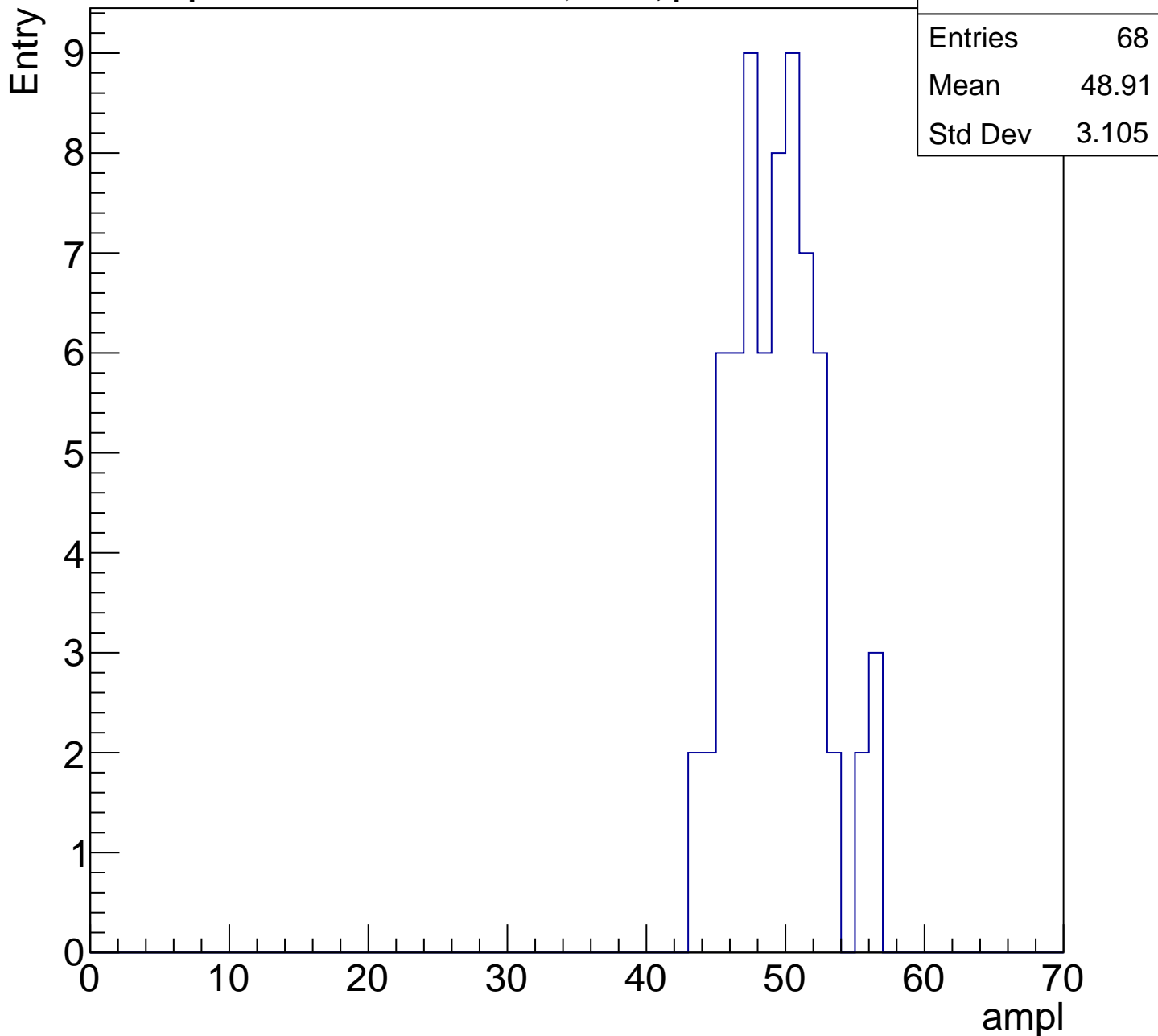
B1L103S, U5-ch39, adc2

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U5-ch39, adc3

calib_packv5_041523_1651.root, FC#0, port C2

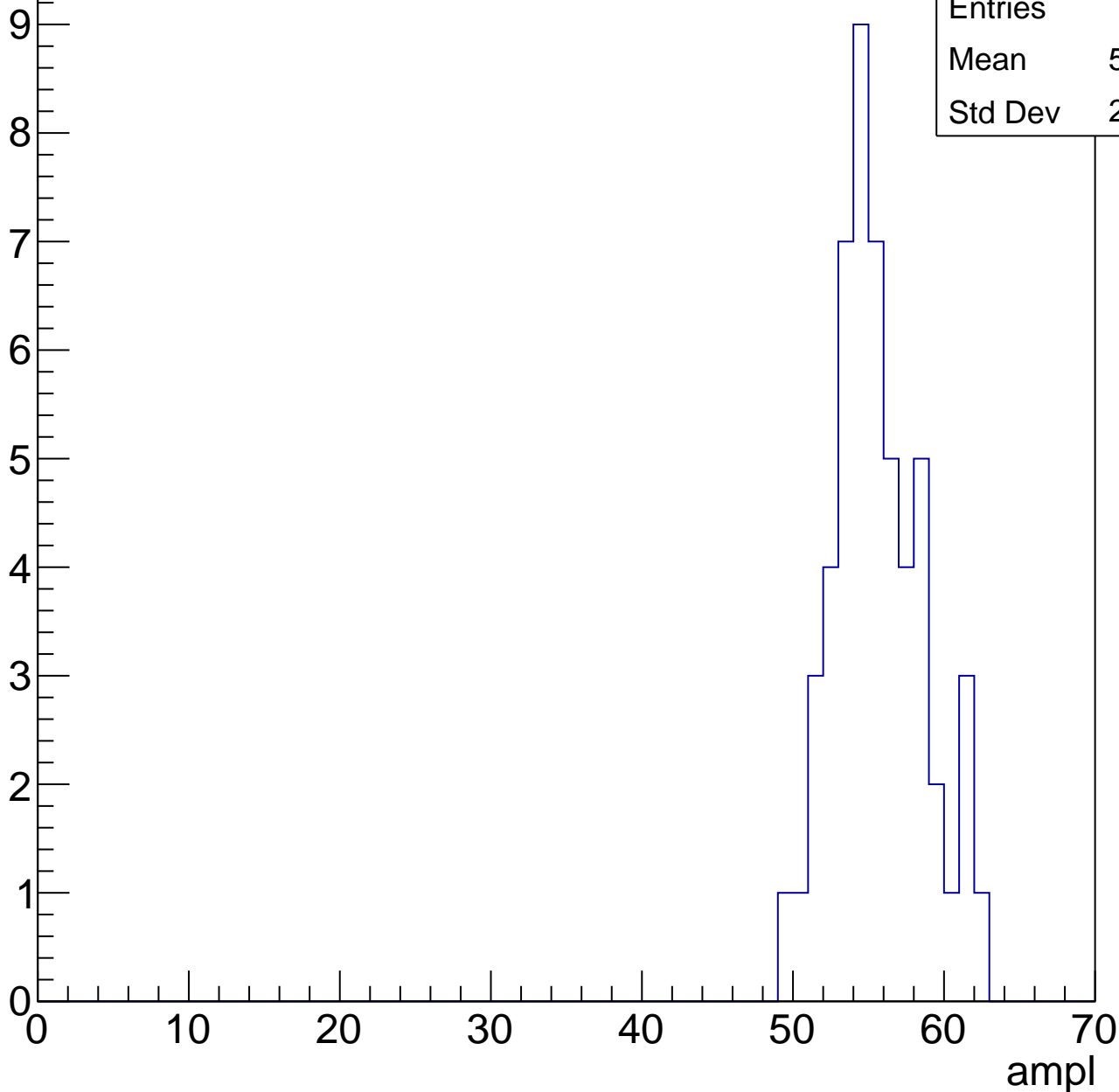


B1L103S, U5-ch39, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

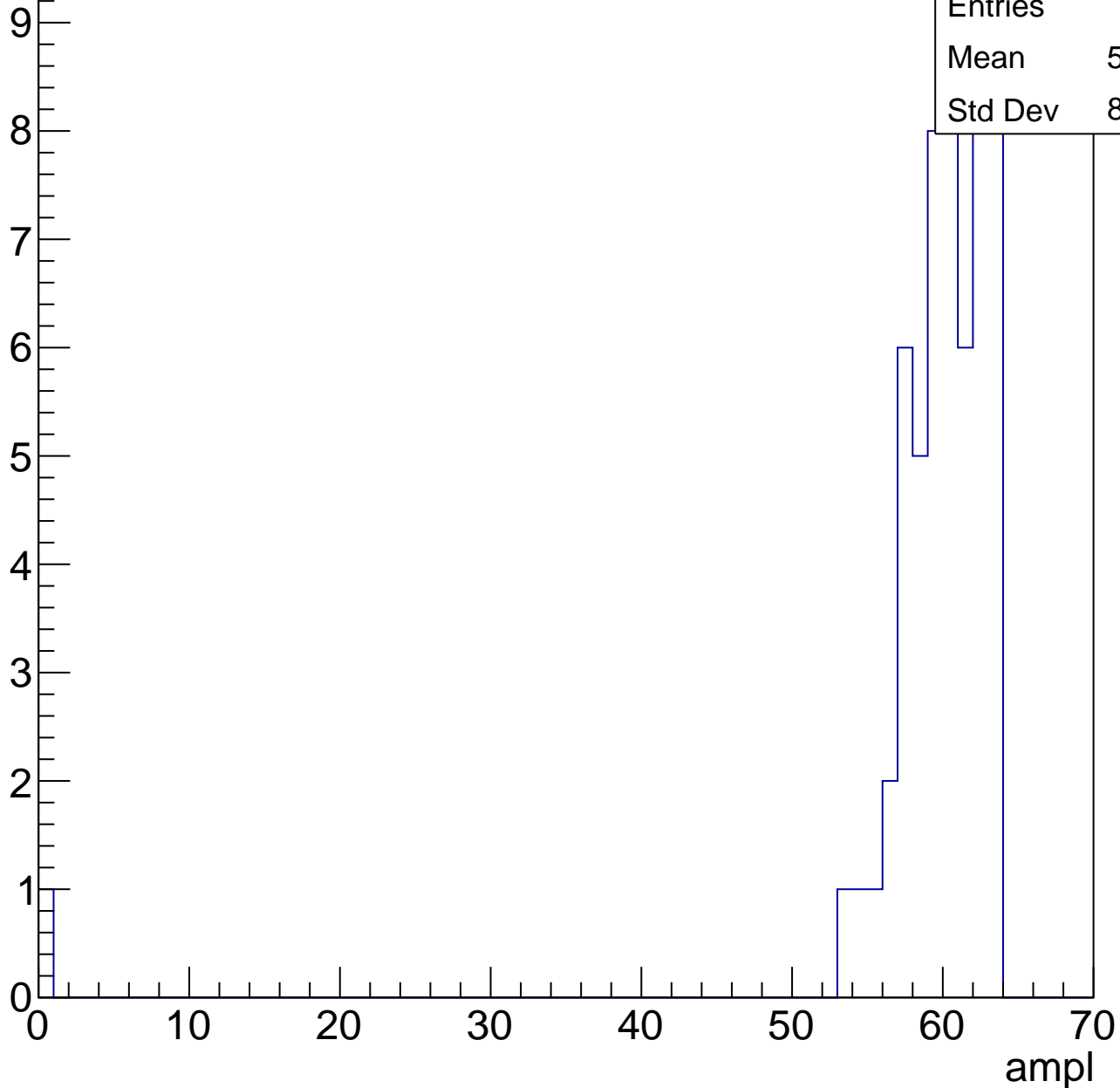
Entries	53
Mean	55.15
Std Dev	2.949



B1L103S, U5-ch39, adc5

calib_packv5_041523_1651.root, FC#0, port C2

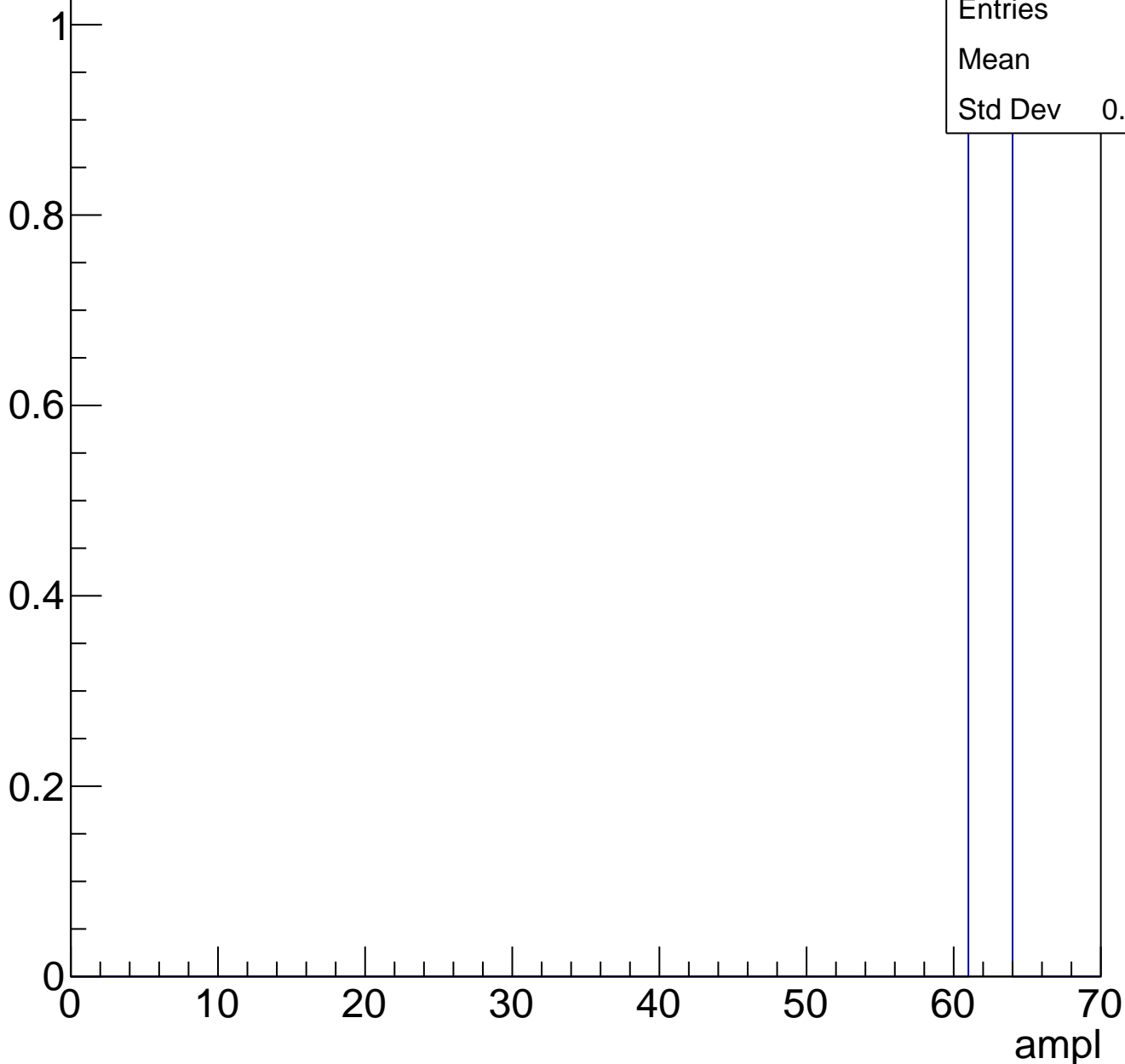
Entry



B1L103S, U5-ch39, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch39, adc7

calib_packv5_041523_1651.root, FC#0, port C2

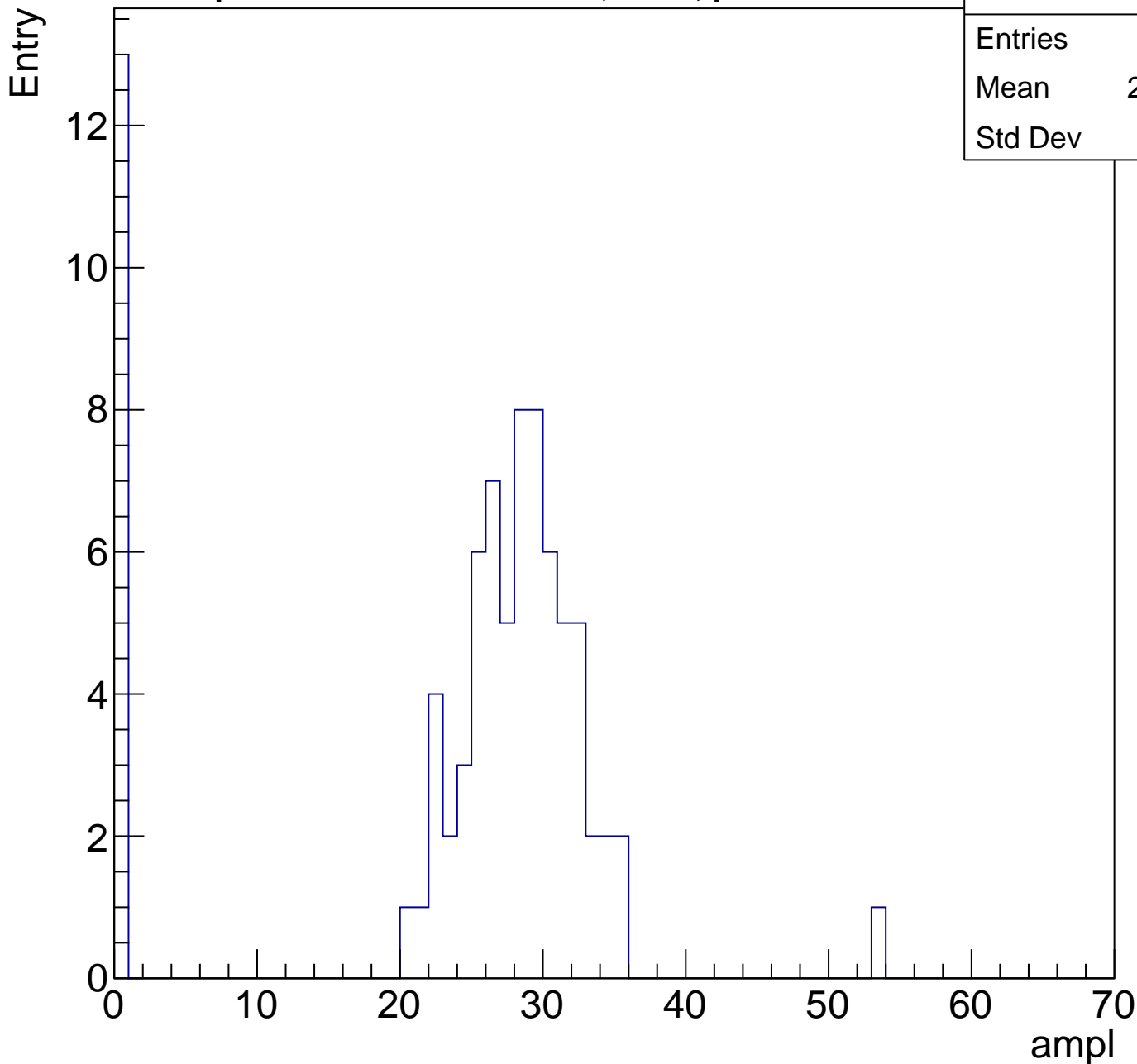
Entry



B1L103S, U5-ch40, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	23.73
Std Dev	11.2

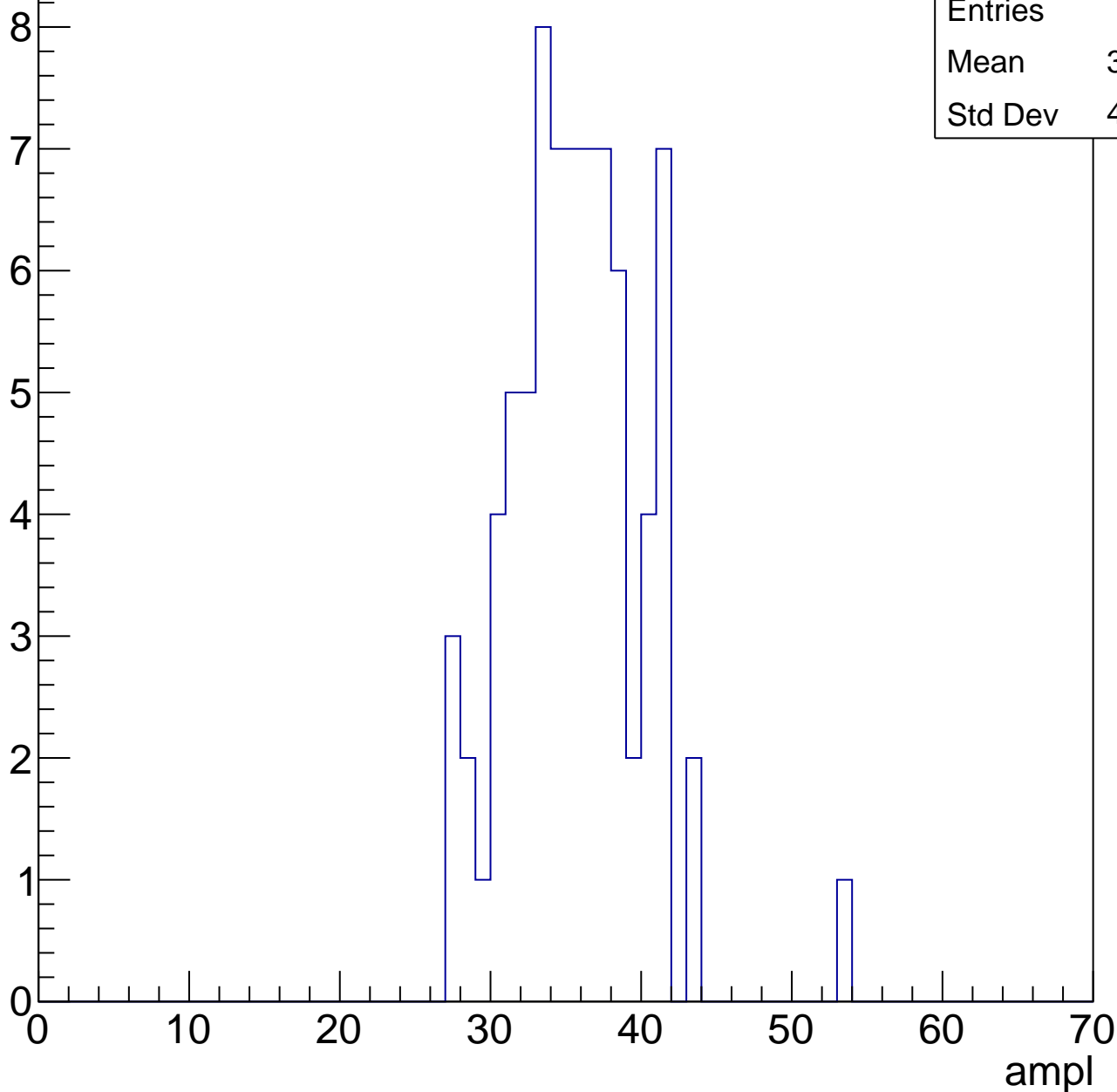


B1L103S, U5-ch40, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	35.27
Std Dev	4.399

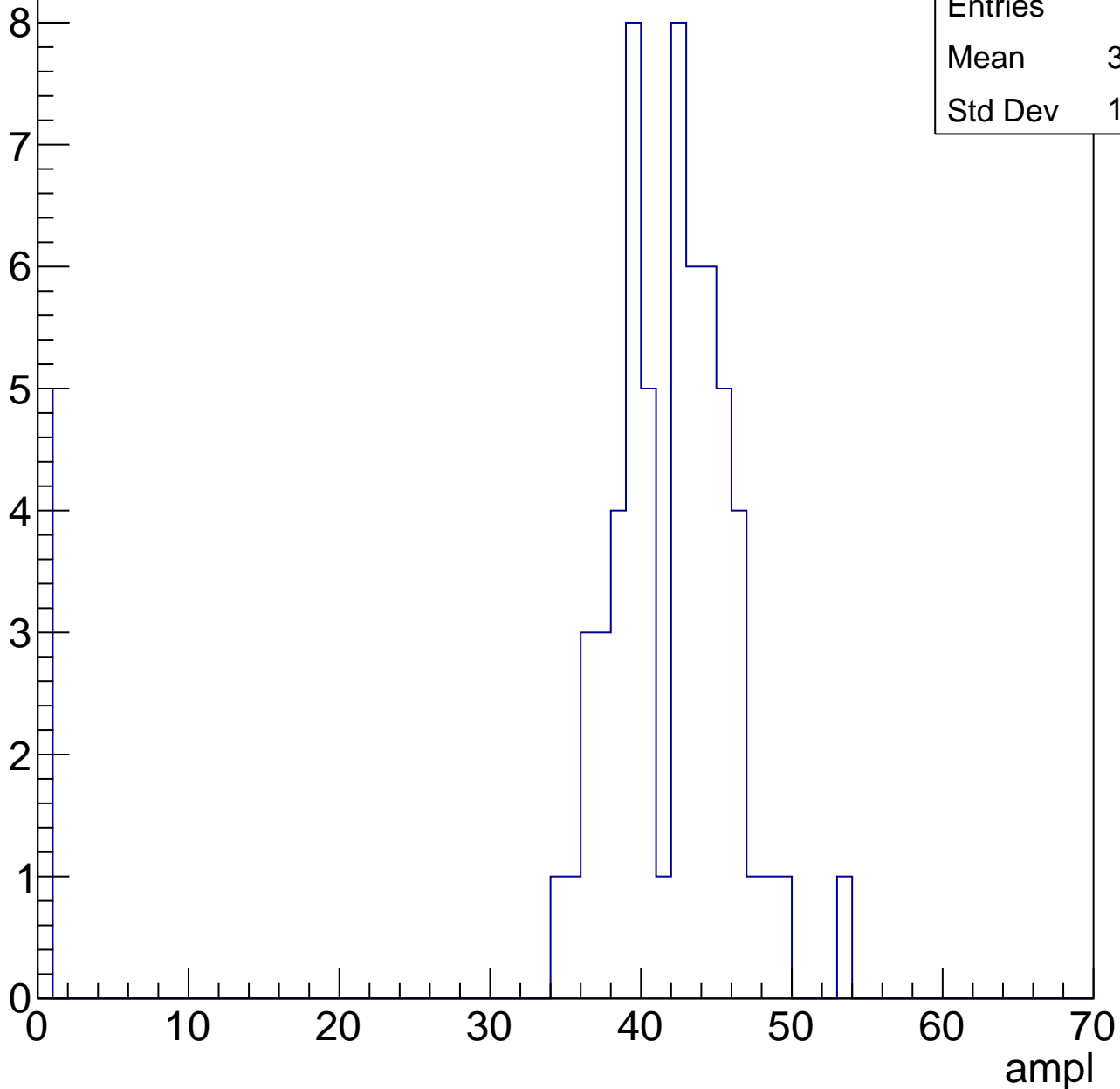


B1L103S, U5-ch40, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	38.39
Std Dev	11.73

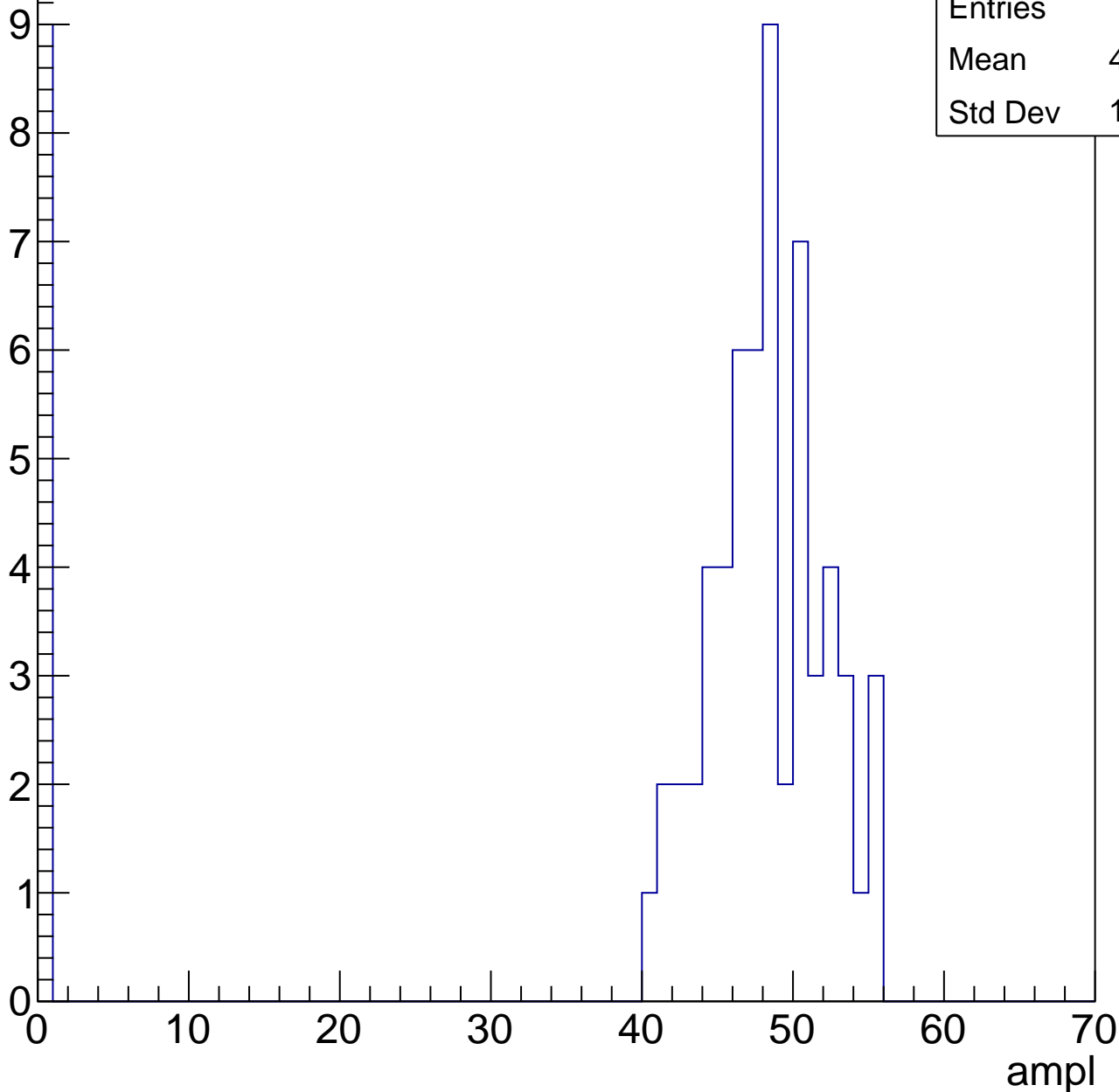


B1L103S, U5-ch40, adc3

calib_packv5_041523_1651.root, FC#0, port C2

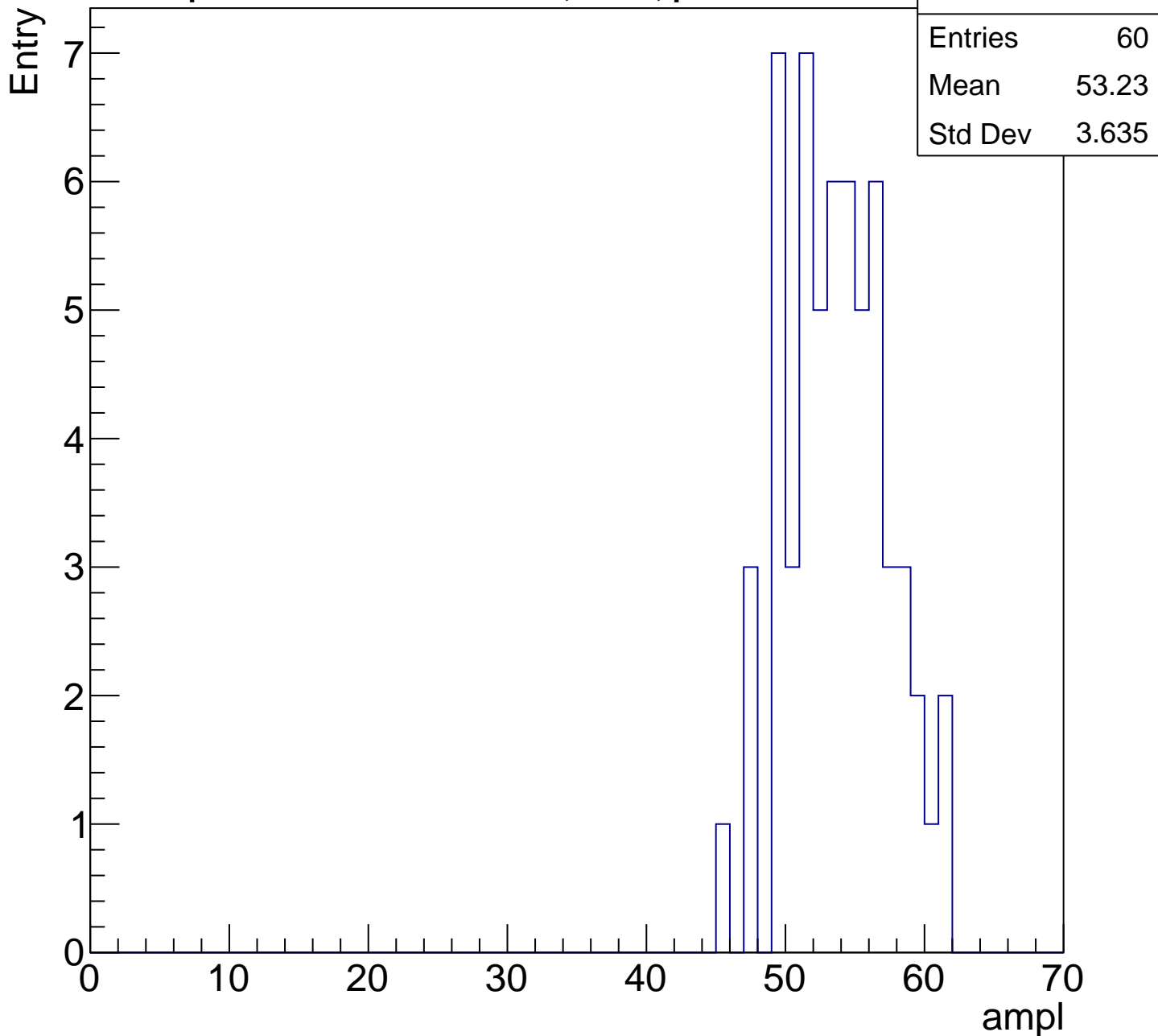
Entry

Entries	68
Mean	41.54
Std Dev	16.58



B1L103S, U5-ch40, adc4

calib_packv5_041523_1651.root, FC#0, port C2

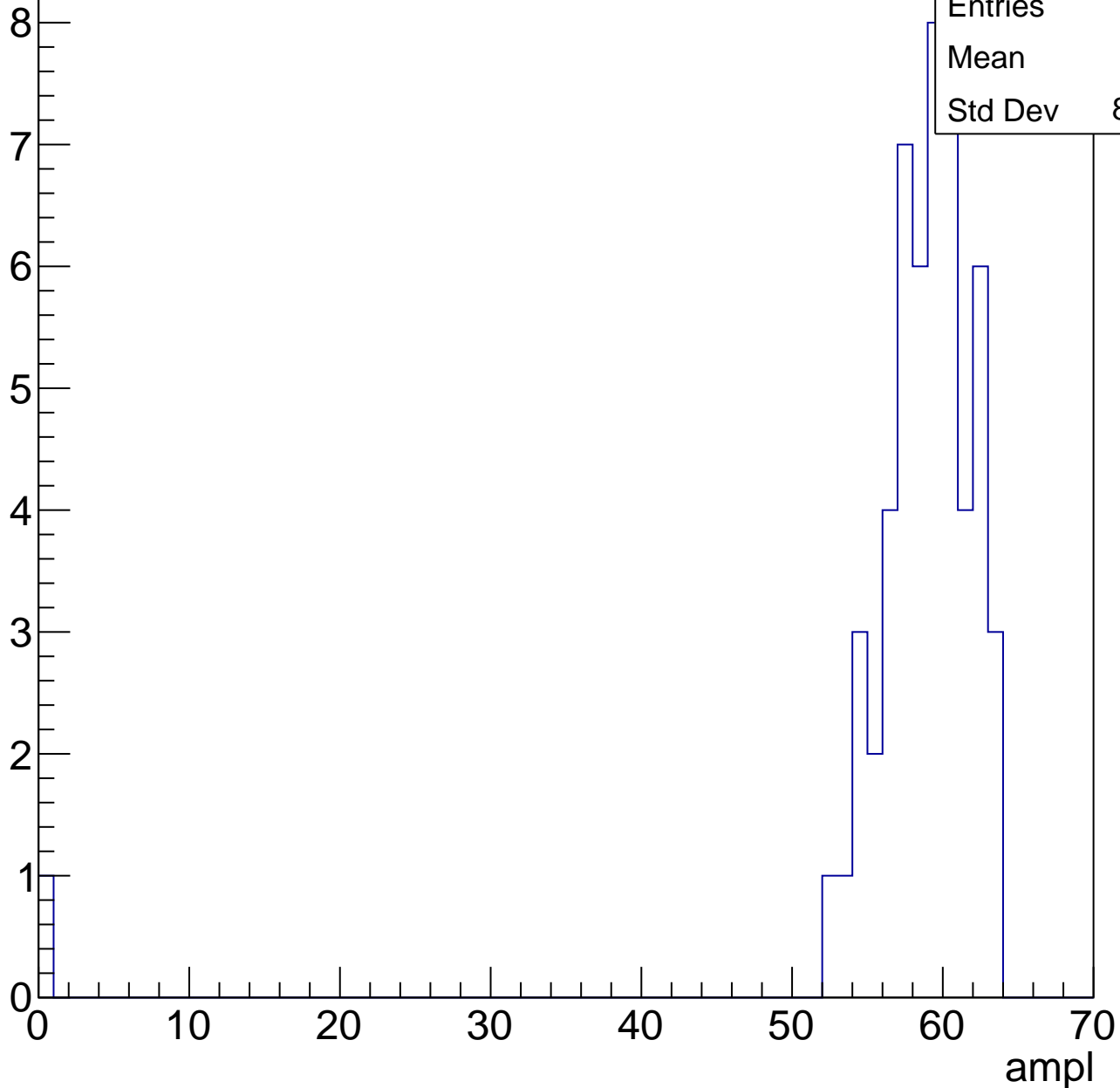


B1L103S, U5-ch40, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	57.5
Std Dev	8.331

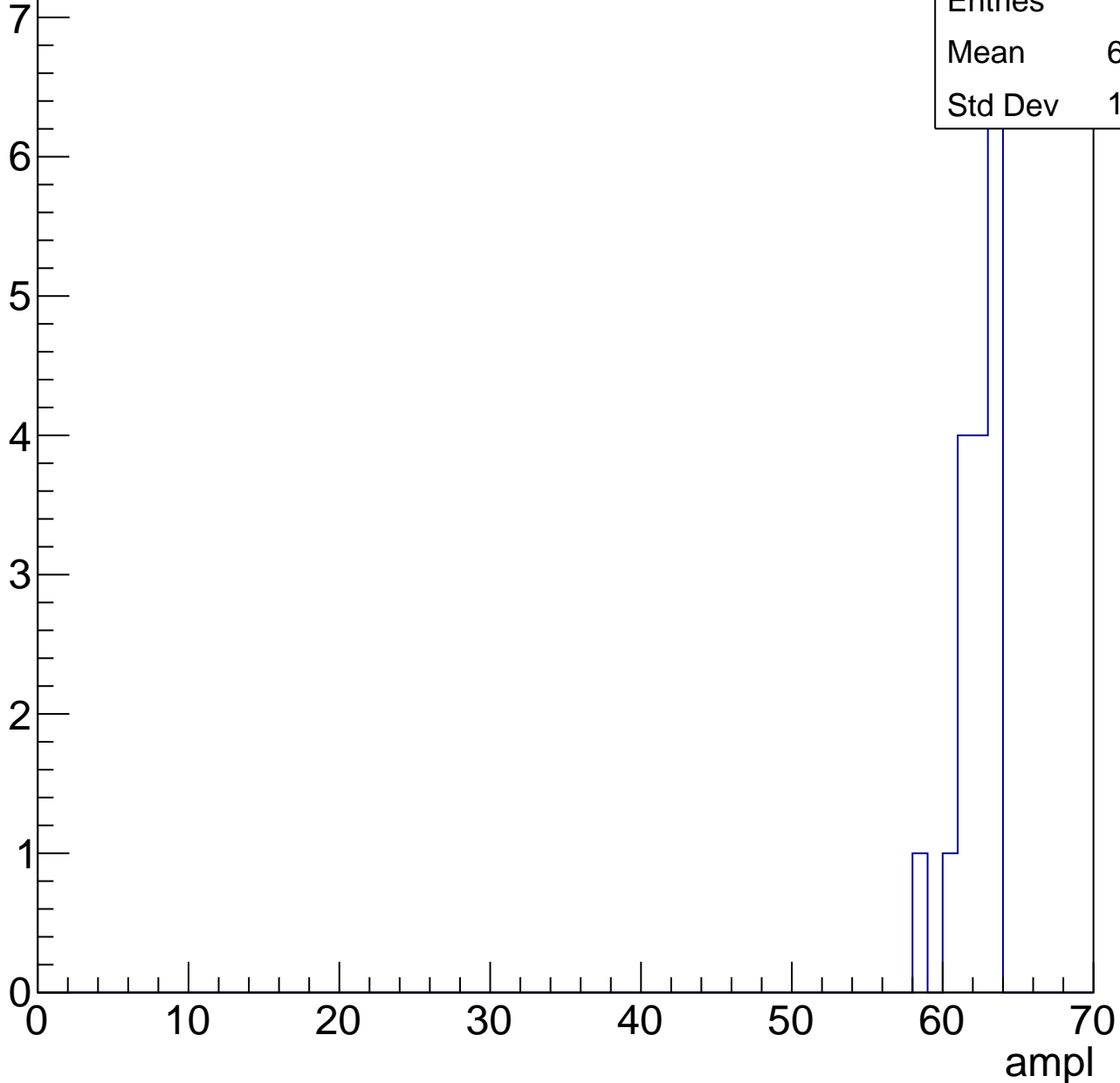


B1L103S, U5-ch40, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	17
Mean	61.82
Std Dev	1.339



B1L103S, U5-ch40, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U5-ch41, adc0

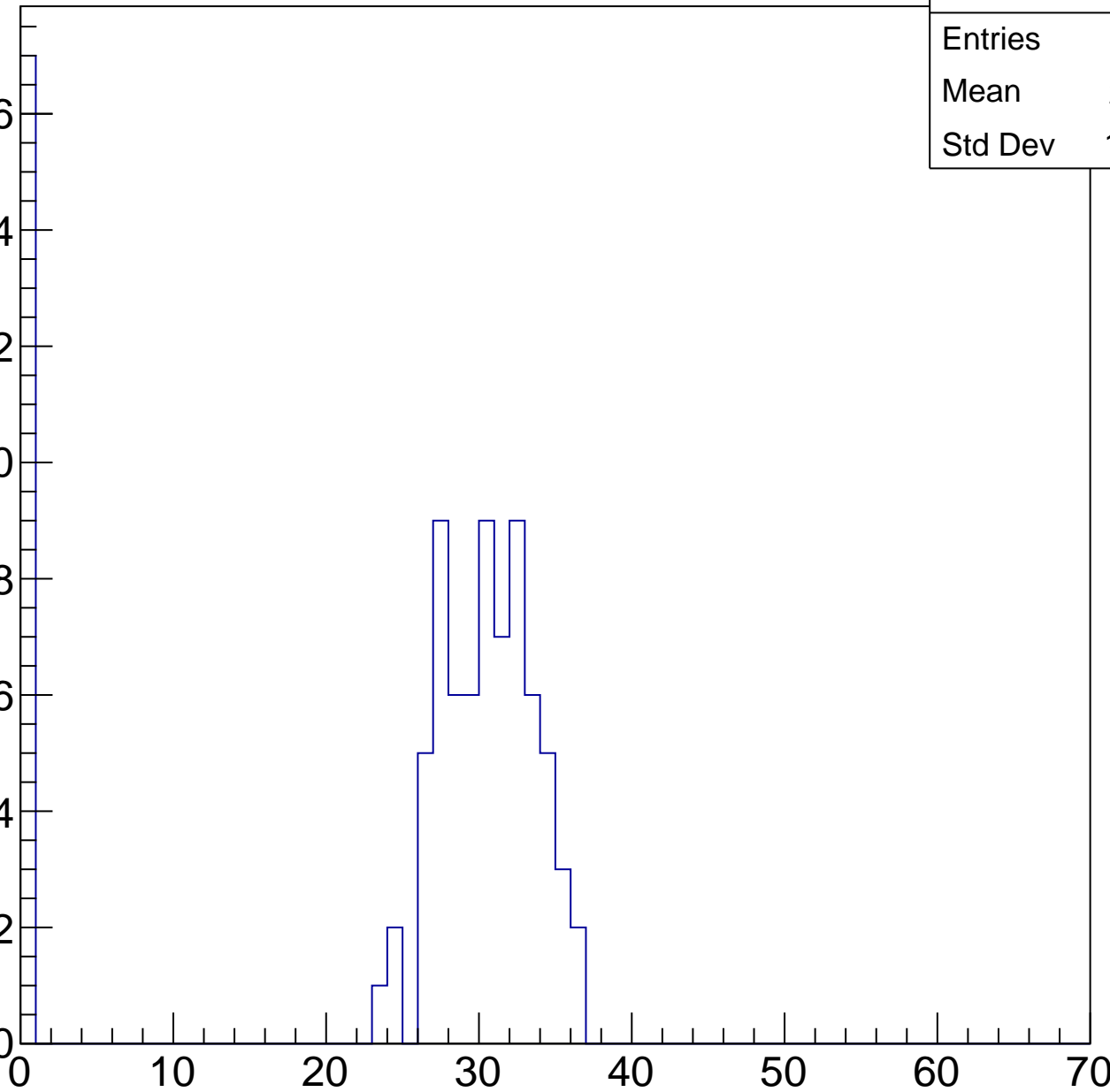
calib_packv5_041523_1651.root, FC#0, port C2

Entries	87
Mean	24.21
Std Dev	12.23

Entry

16
14
12
10
8
6
4
2
0

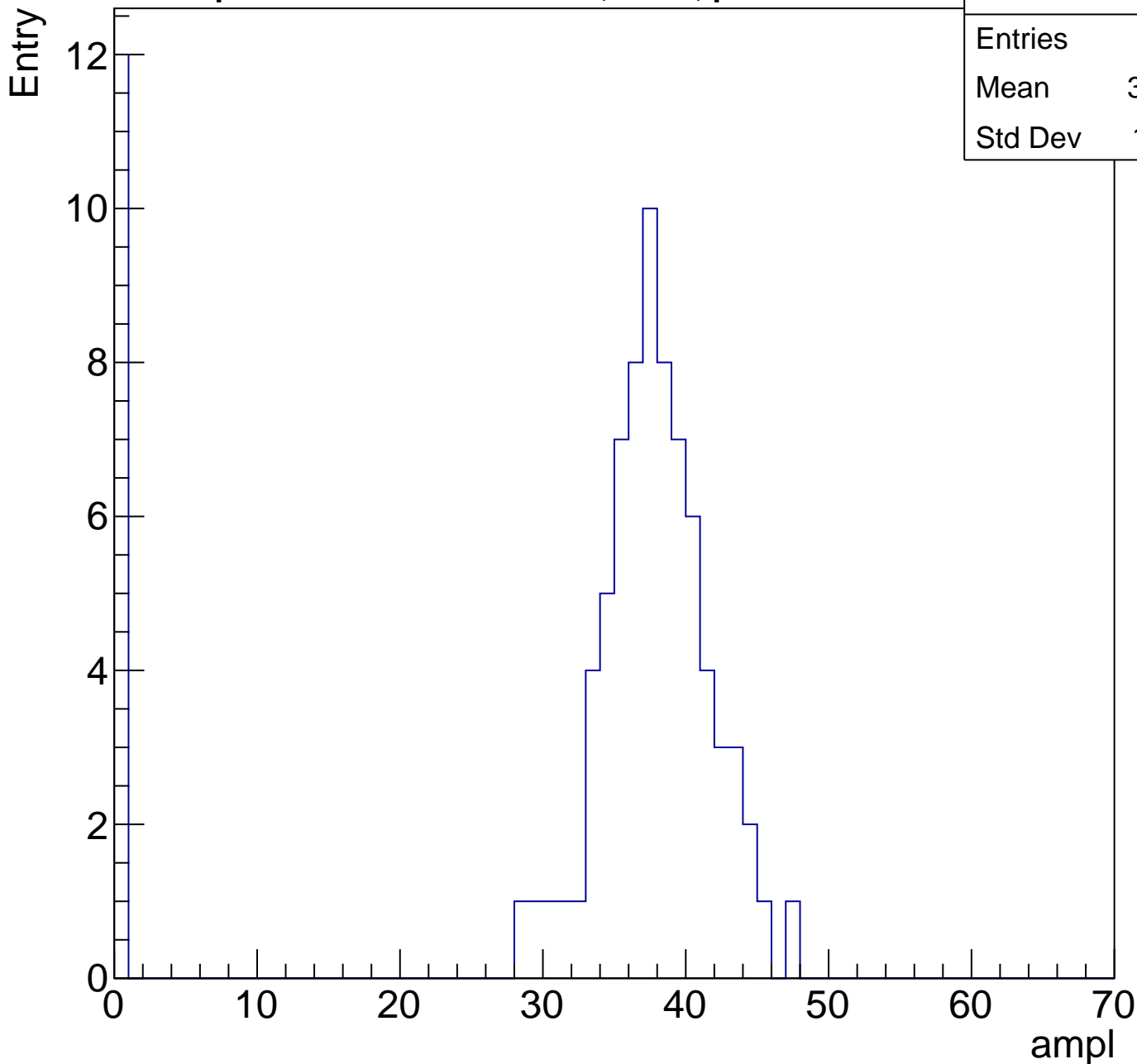
ampl



B1L103S, U5-ch41, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	86
Mean	32.22
Std Dev	13.41

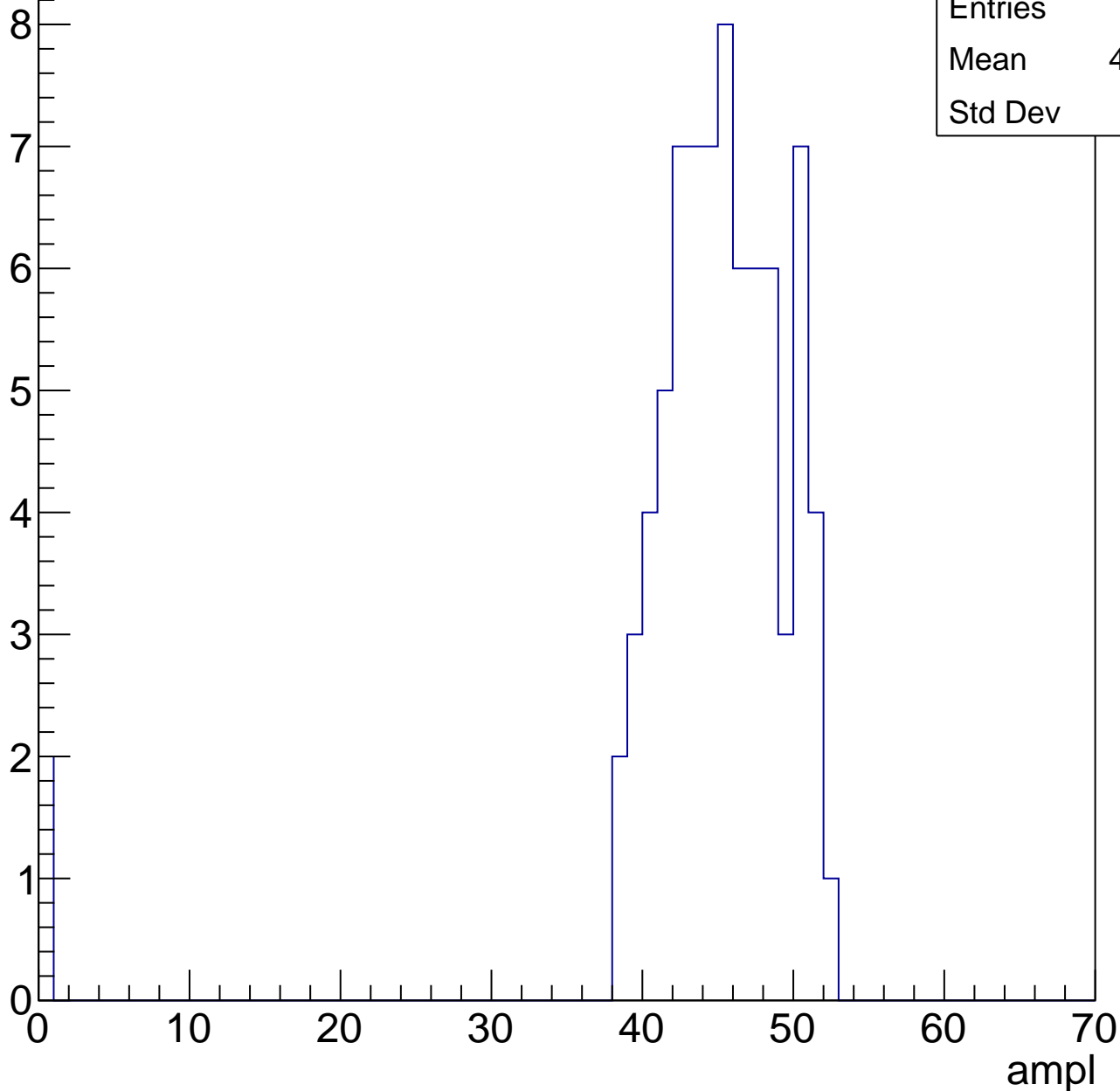


B1L103S, U5-ch41, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	43.85
Std Dev	7.95

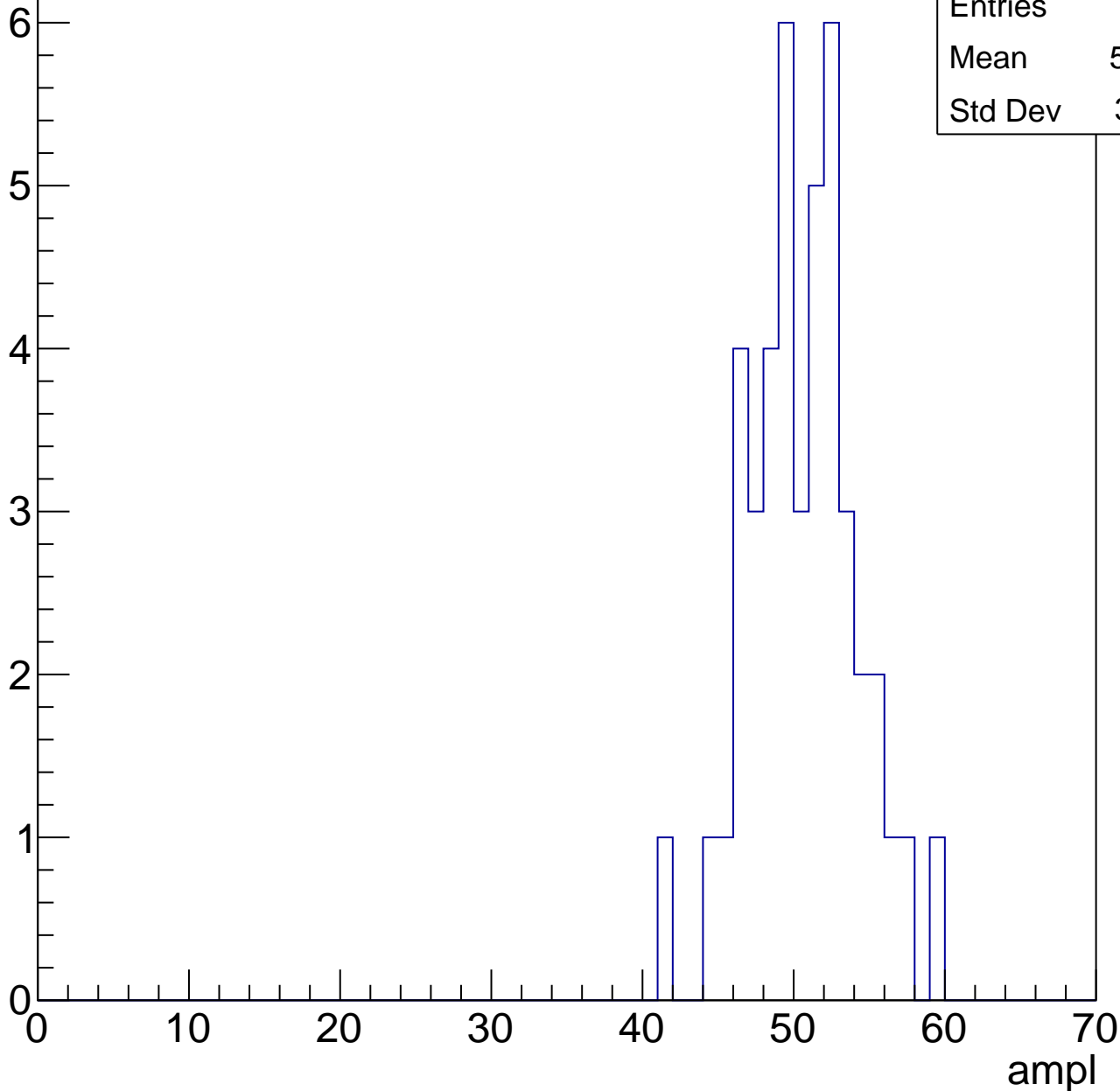


B1L103S, U5-ch41, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	44
Mean	50.16
Std Dev	3.561

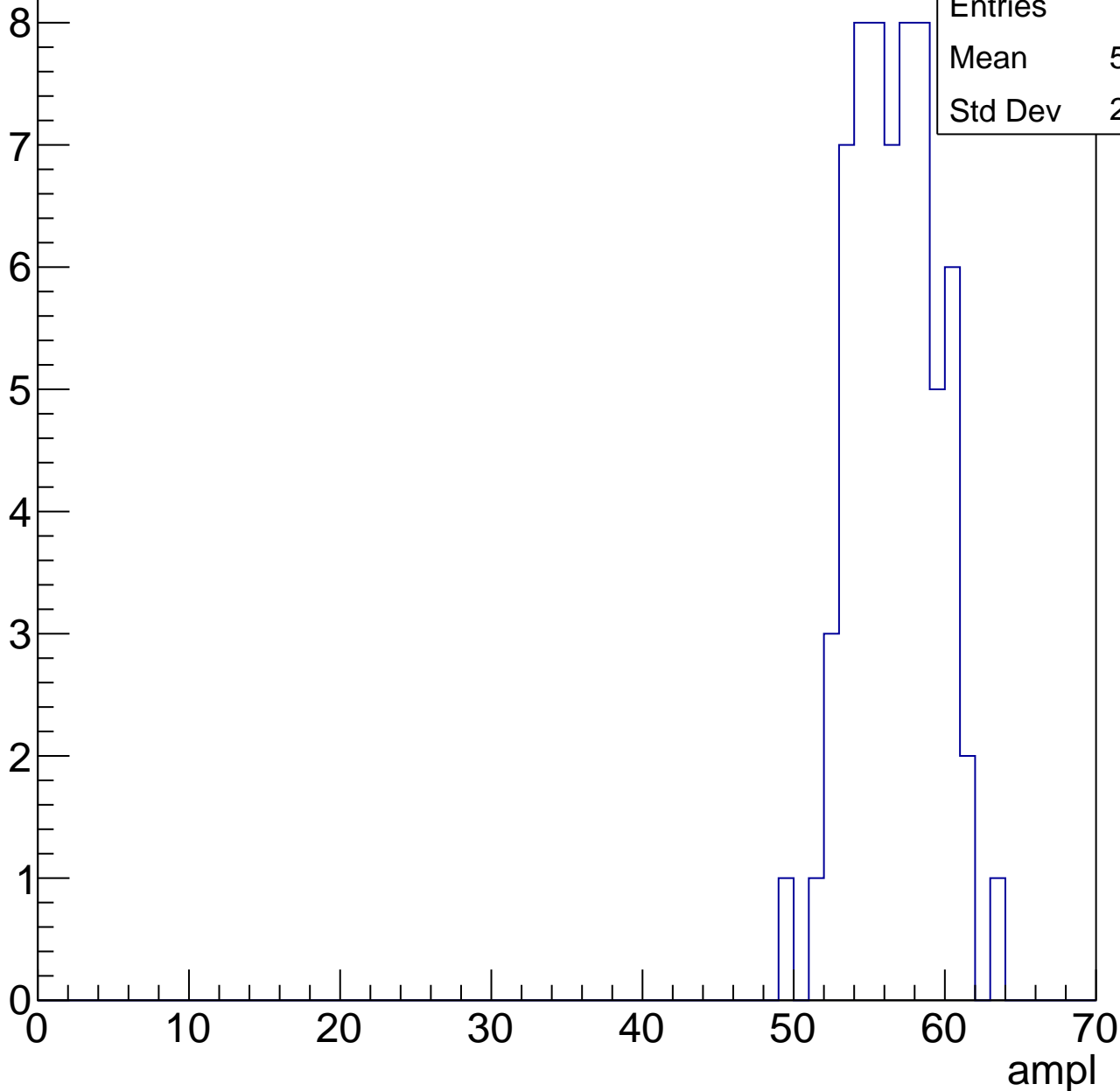


B1L103S, U5-ch41, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	56.17
Std Dev	2.782

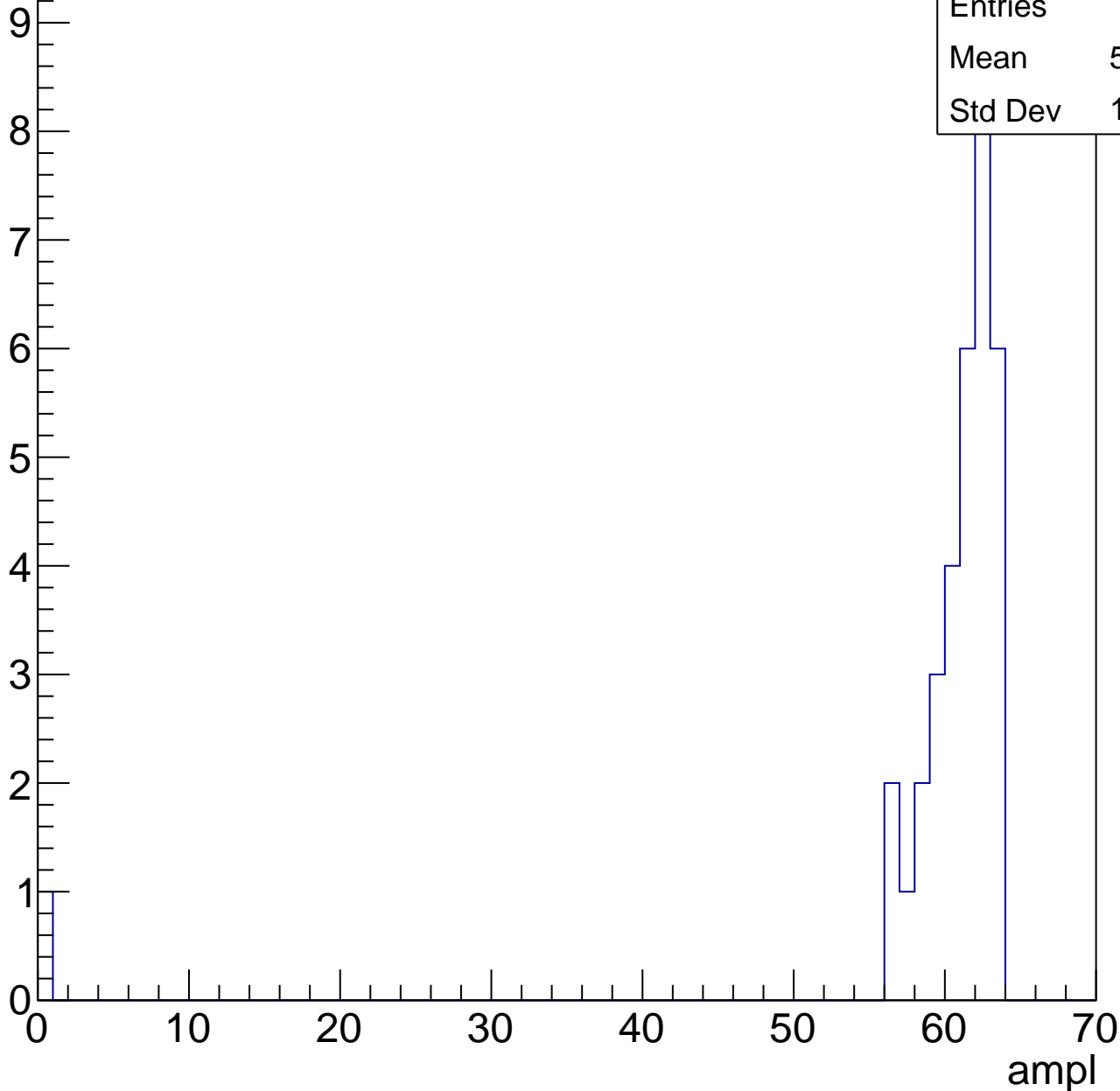


B1L103S, U5-ch41, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

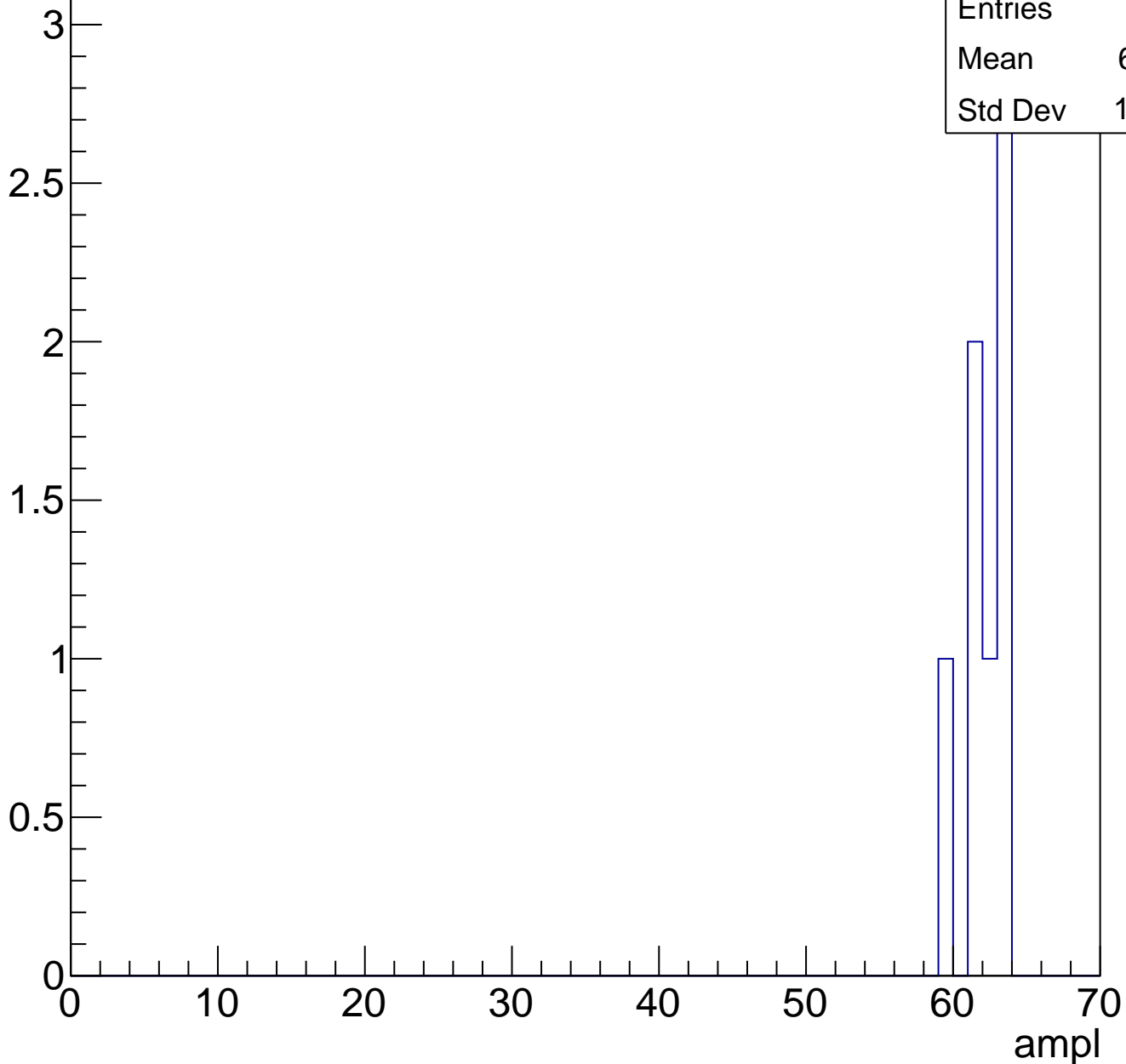
Entries	34
Mean	58.94
Std Dev	10.45



B1L103S, U5-ch41, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch41, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

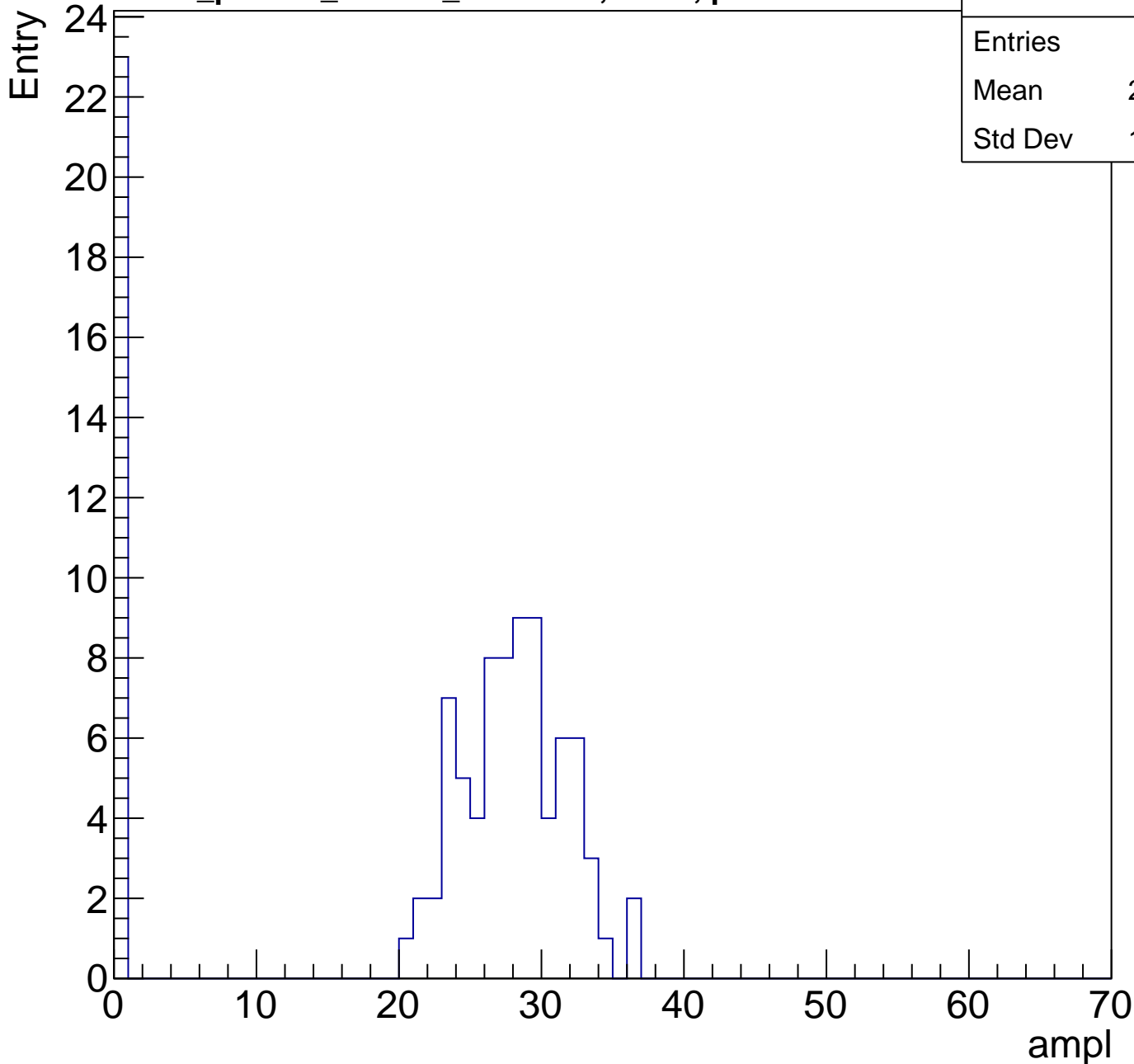
Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U5-ch42, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	100
Mean	21.27
Std Dev	12.03

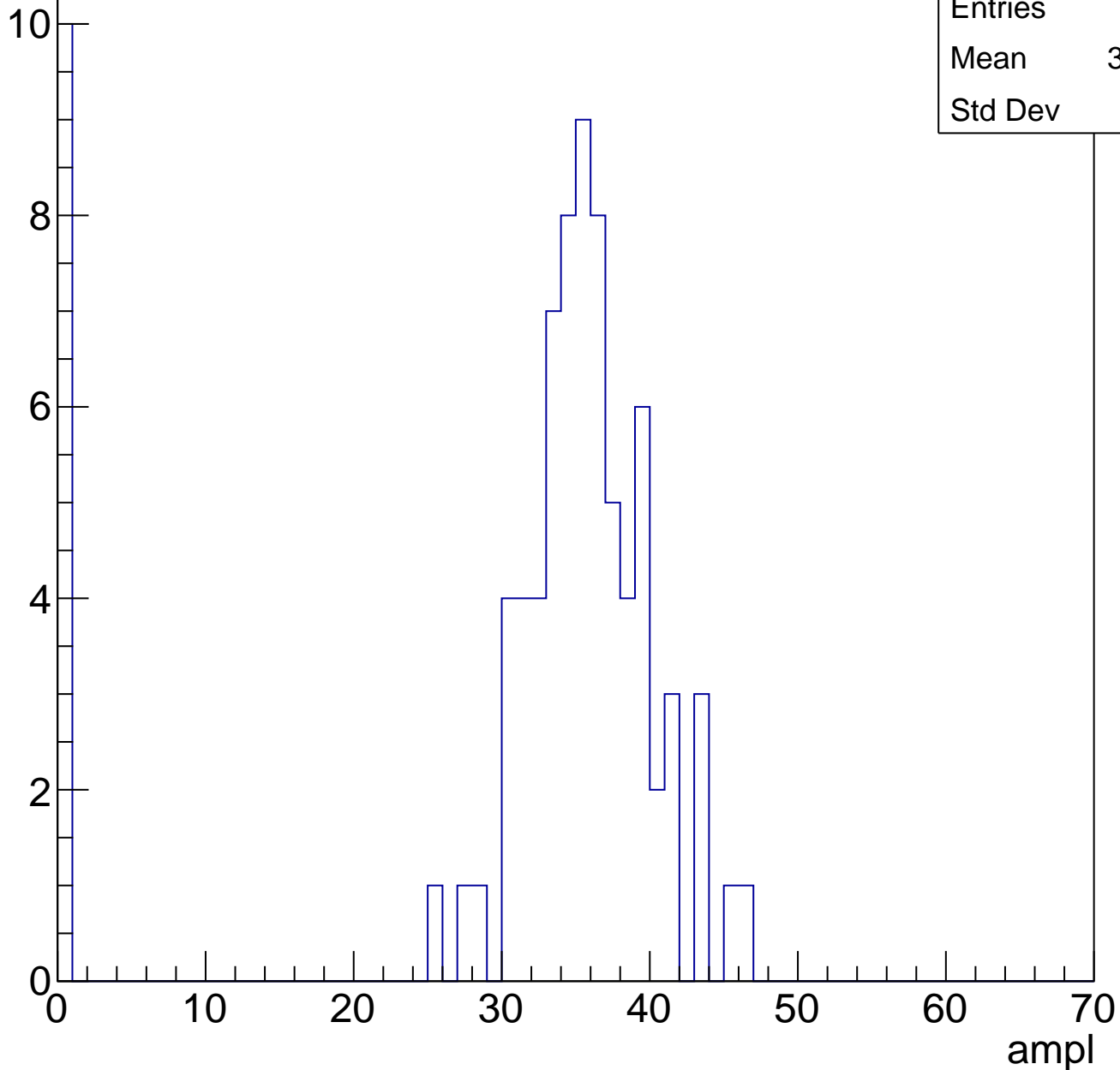


B1L103S, U5-ch42, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	31.12
Std Dev	12.2

Entry

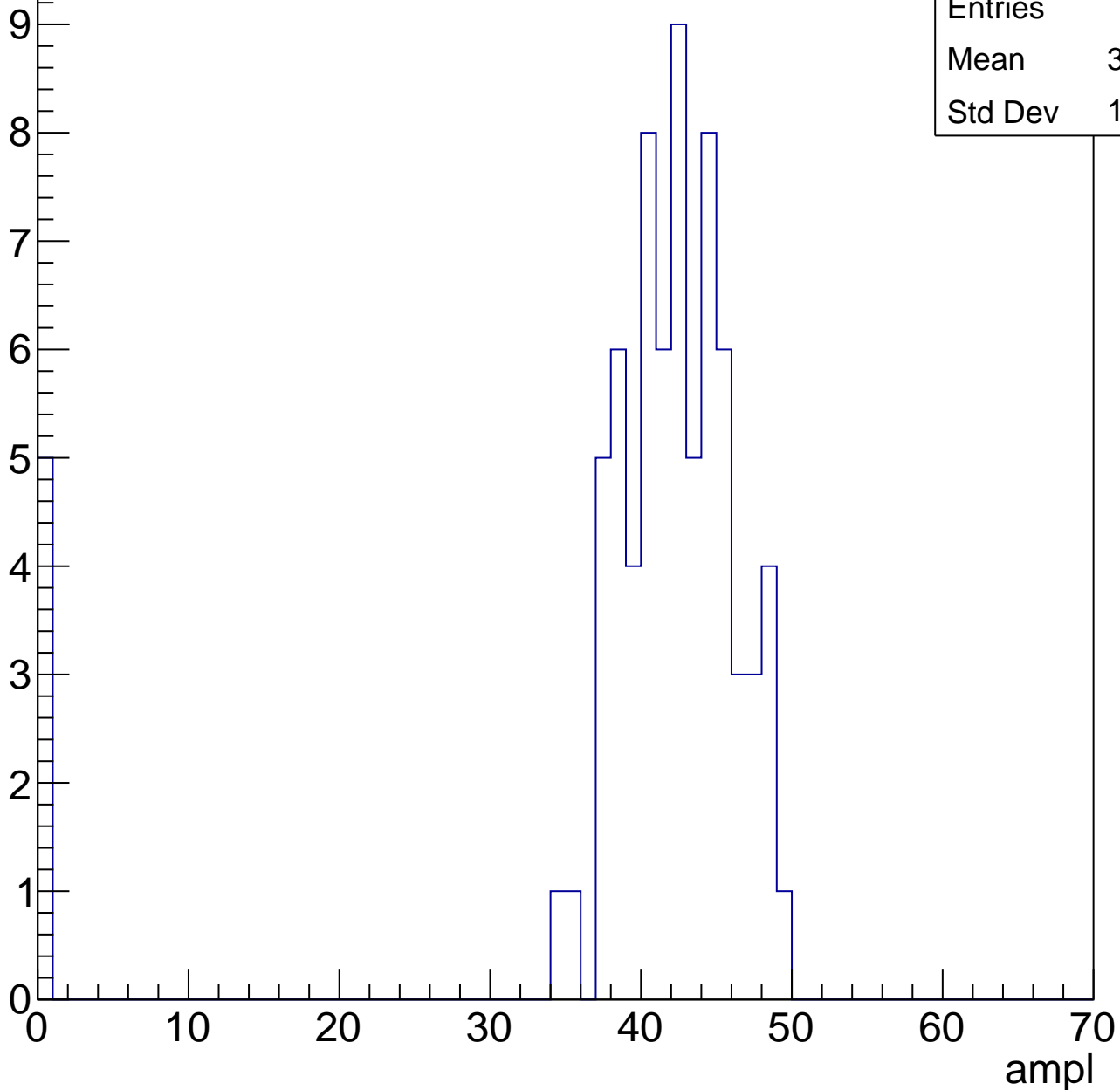


B1L103S, U5-ch42, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	39.19
Std Dev	10.98

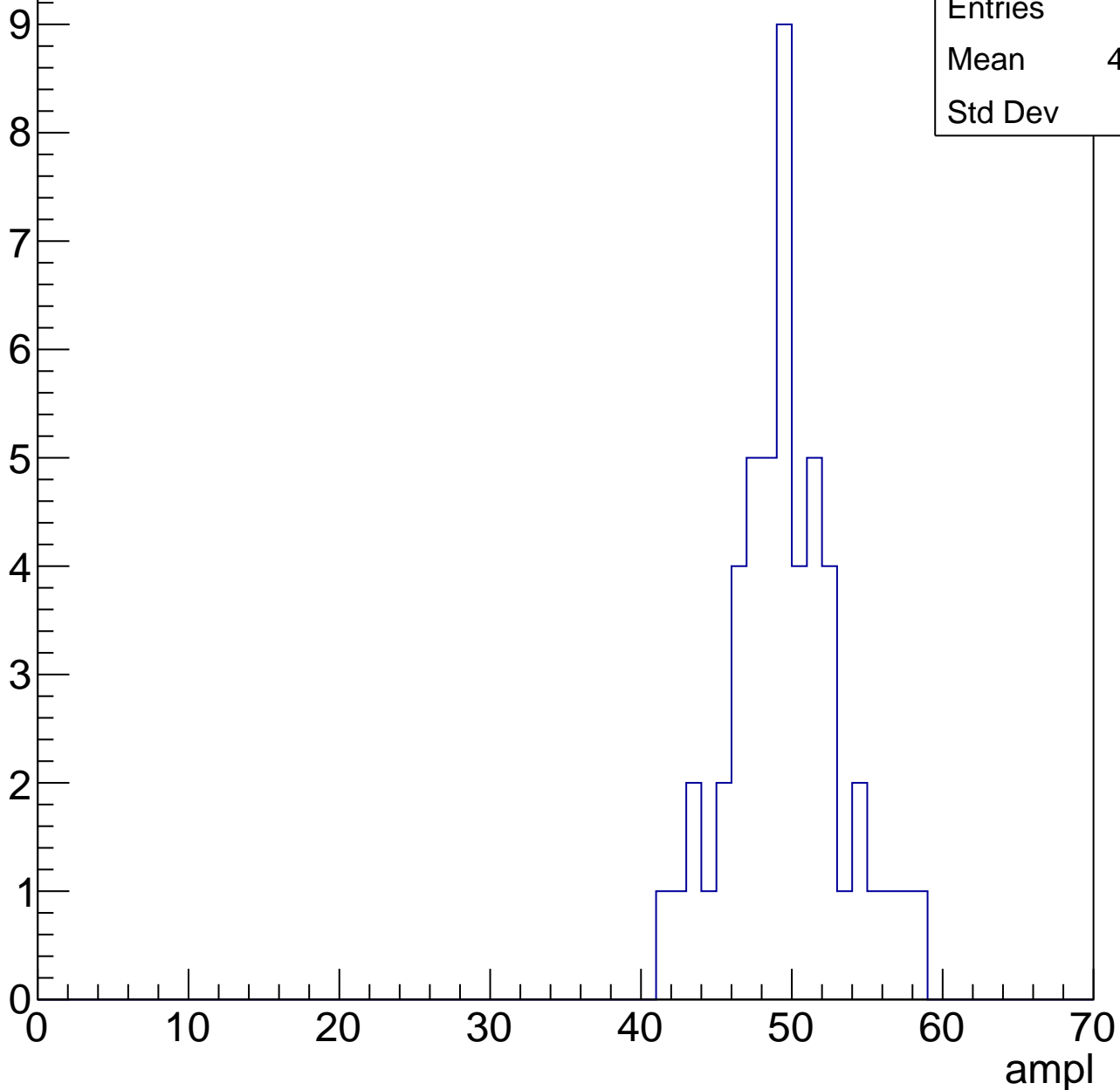


B1L103S, U5-ch42, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	49.06
Std Dev	3.63

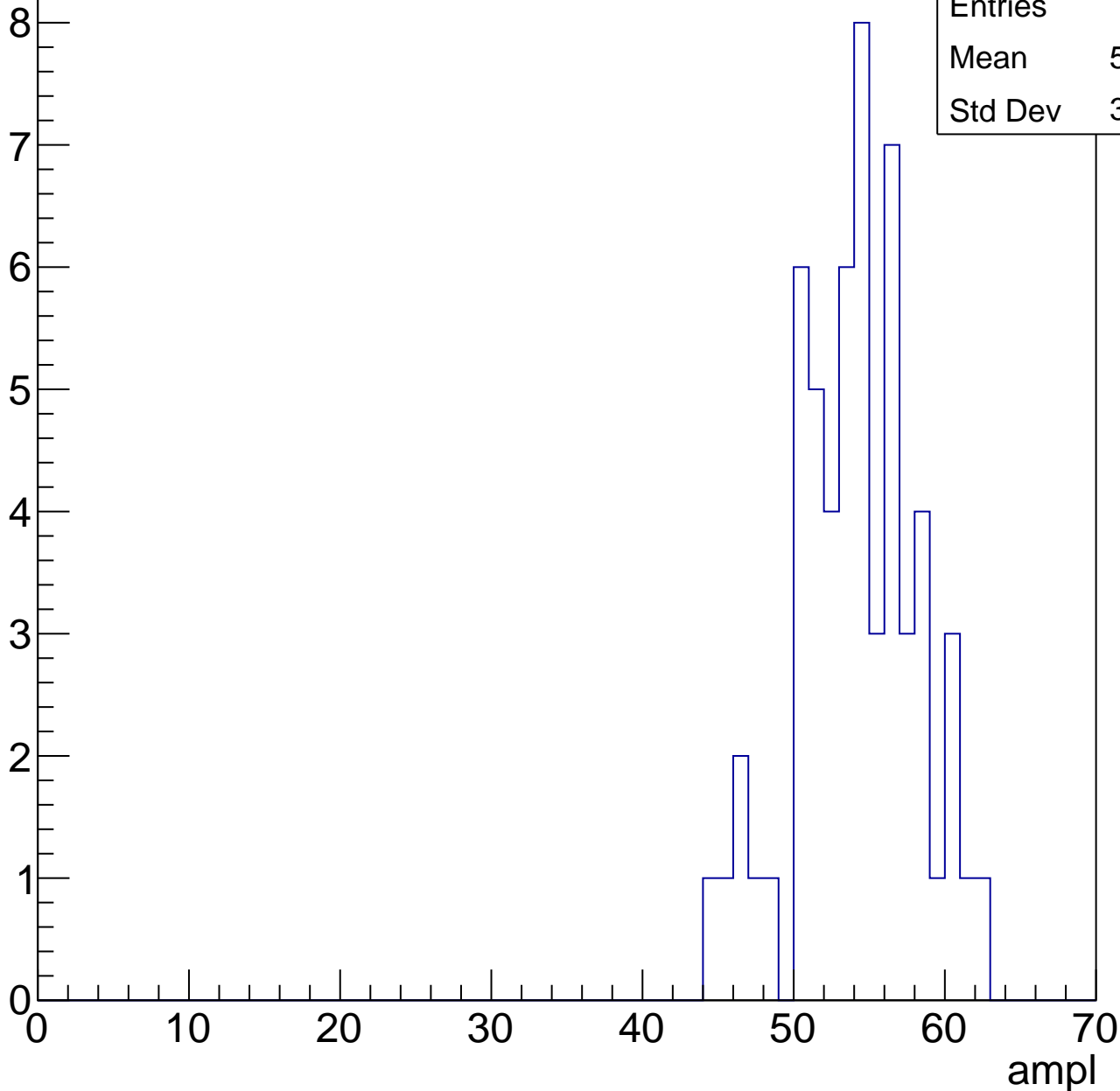


B1L103S, U5-ch42, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	53.64
Std Dev	3.977

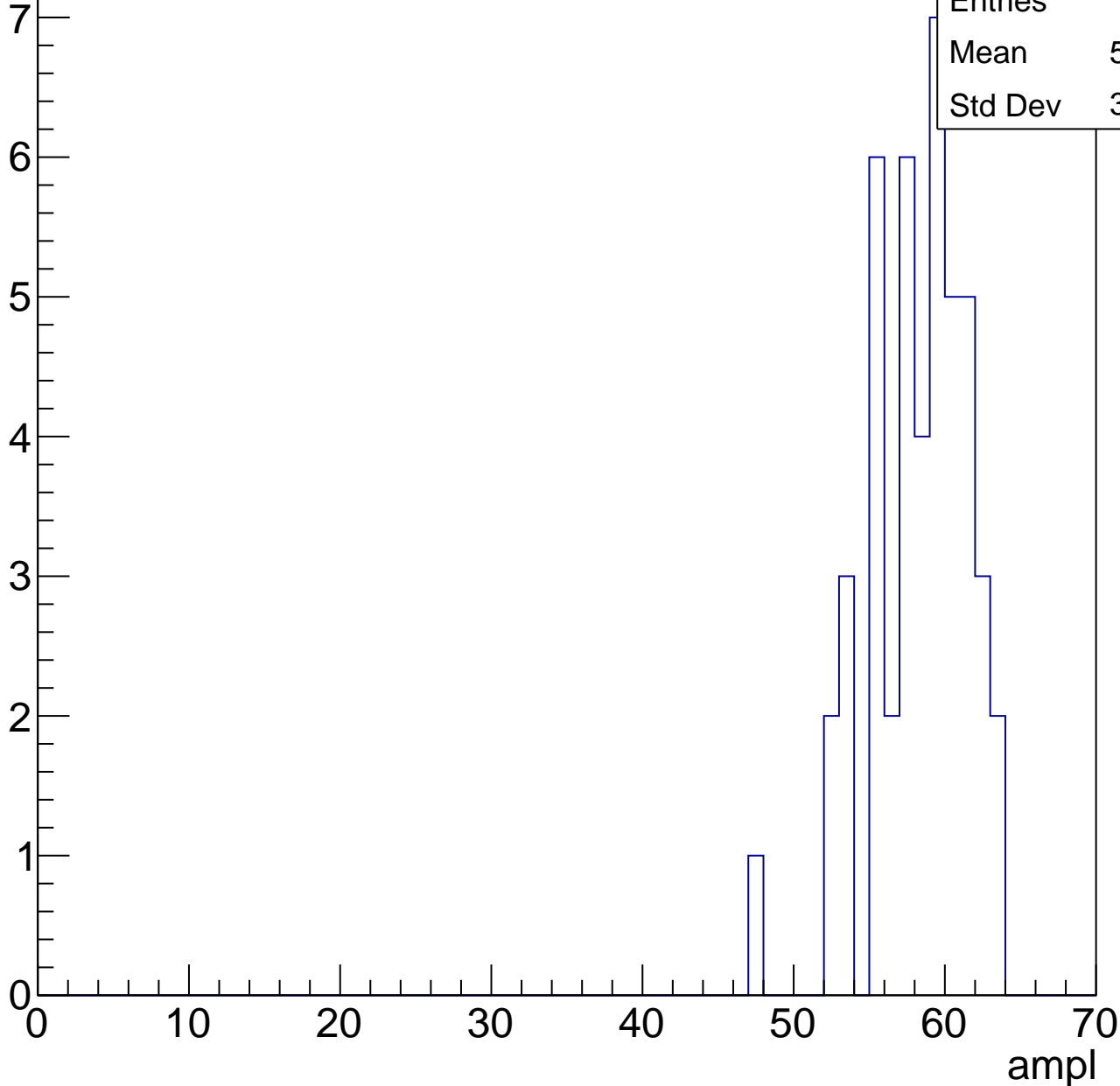


B1L103S, U5-ch42, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	46
Mean	57.74
Std Dev	3.306

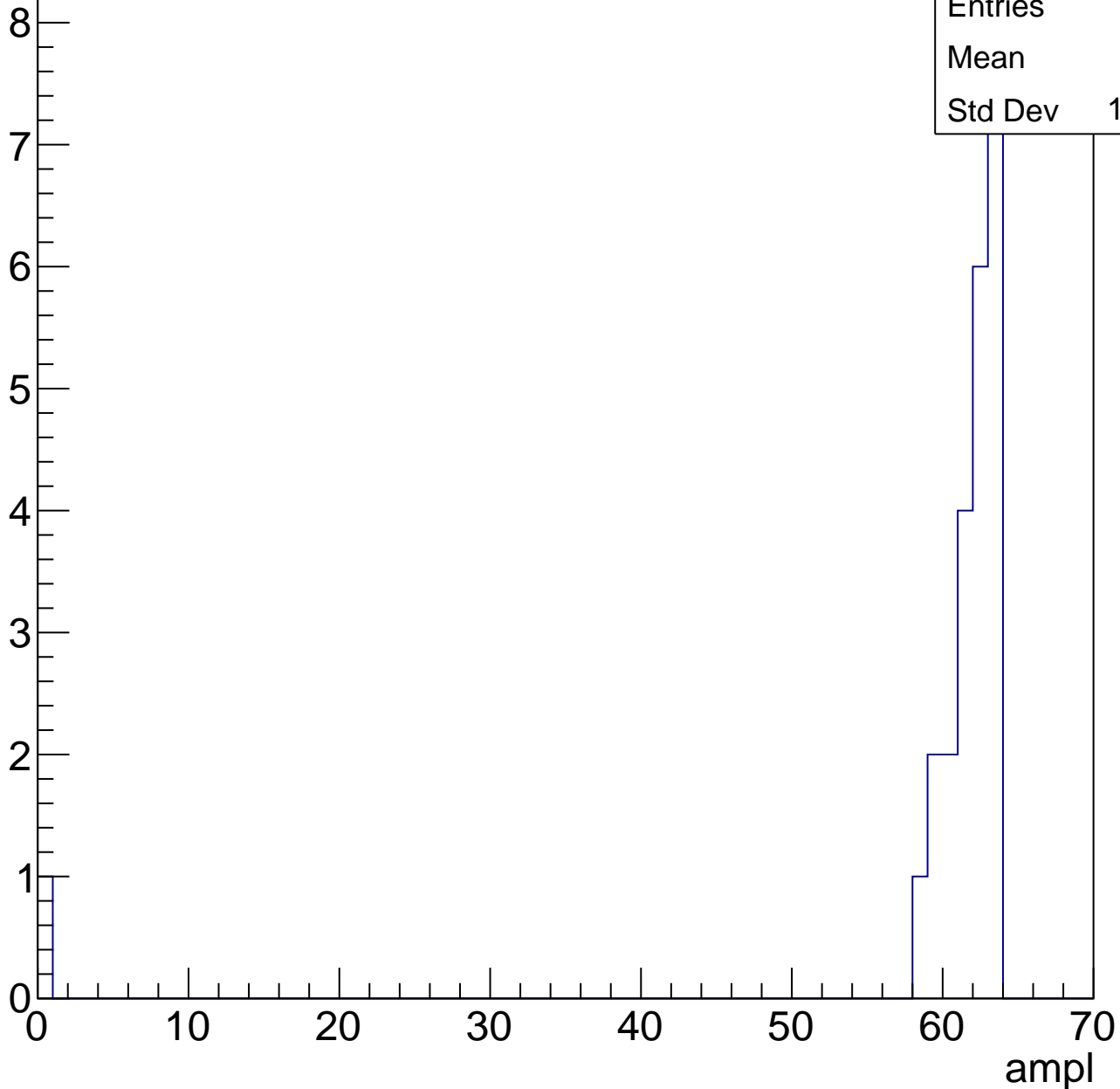


B1L103S, U5-ch42, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	24
Mean	59
Std Dev	12.39



B1L103S, U5-ch42, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U5-ch43, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	92
Mean	24.16
Std Dev	12.03

Entry

16
14
12
10
8
6
4
2
0

0

10

20

30

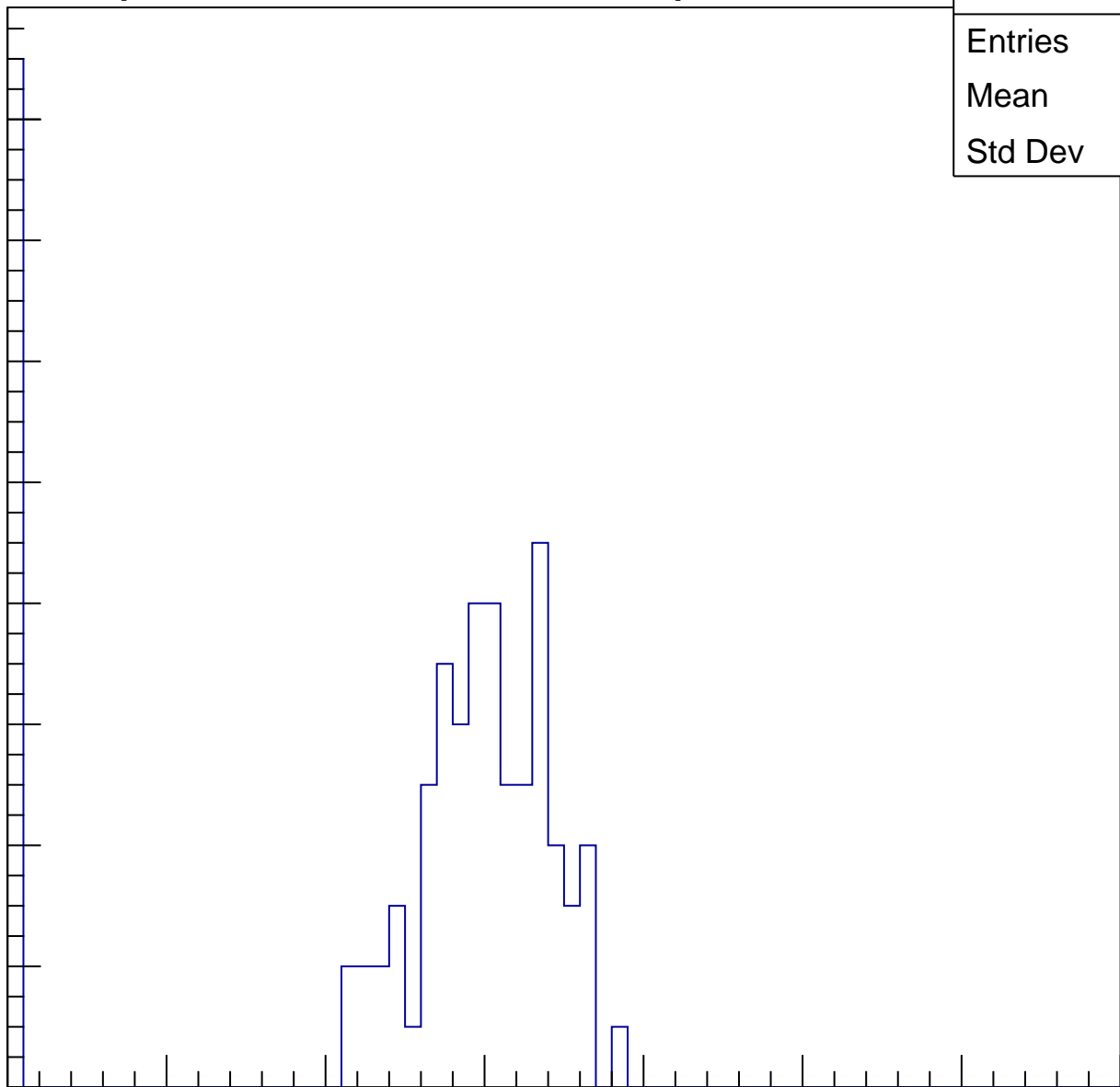
40

50

60

70

ampl

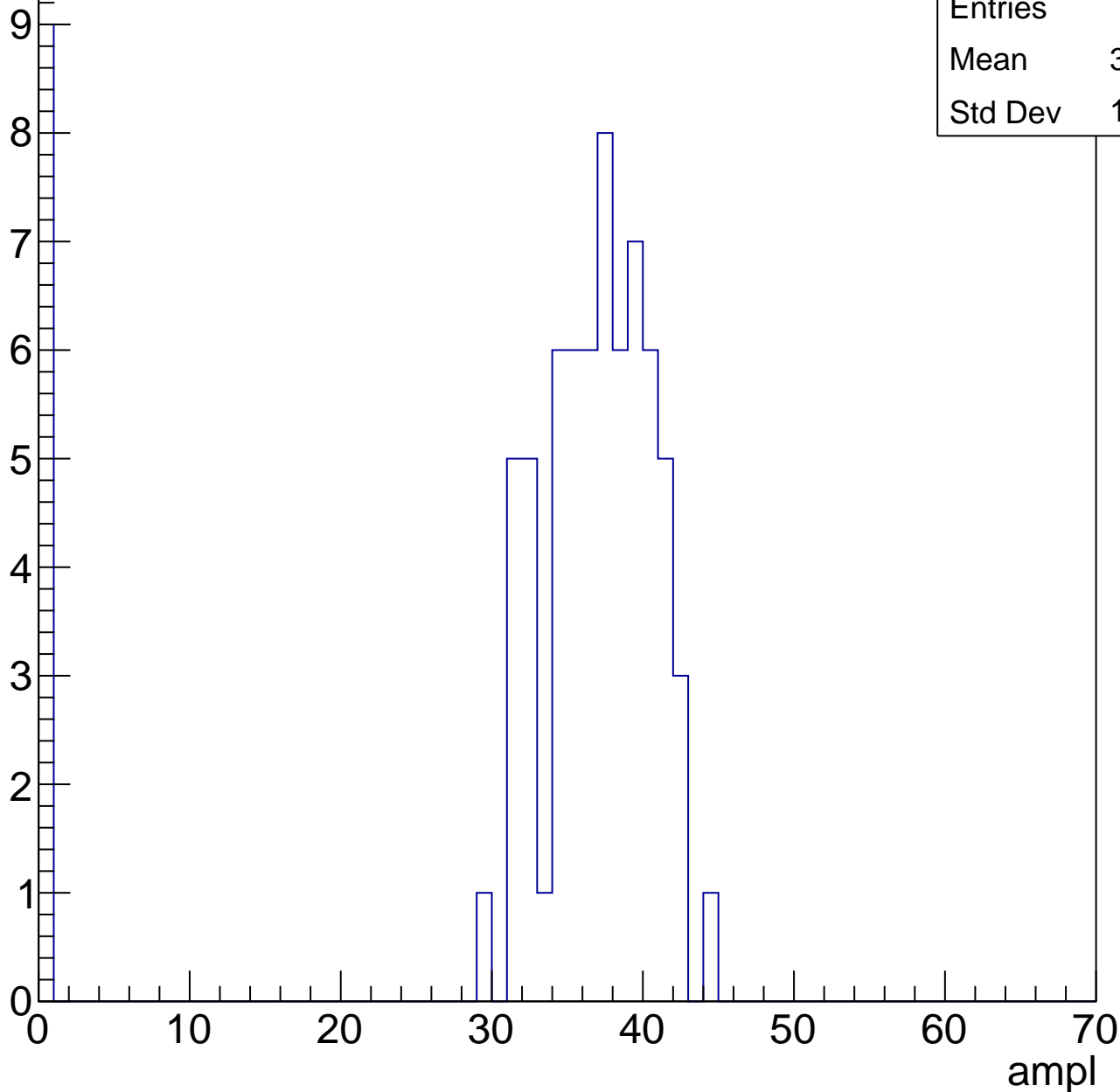


B1L103S, U5-ch43, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	32.25
Std Dev	12.32

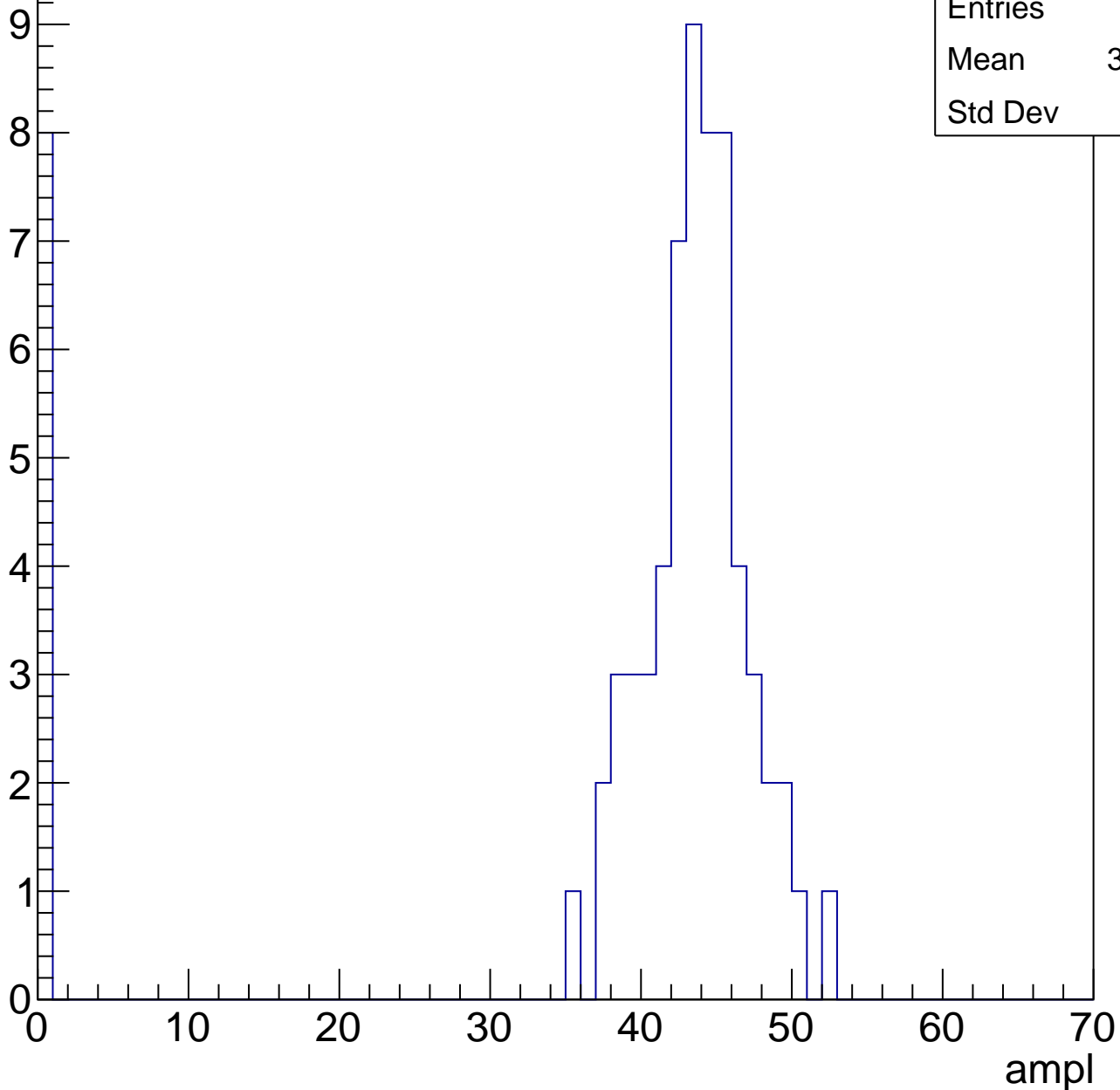


B1L103S, U5-ch43, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	38.23
Std Dev	14.2

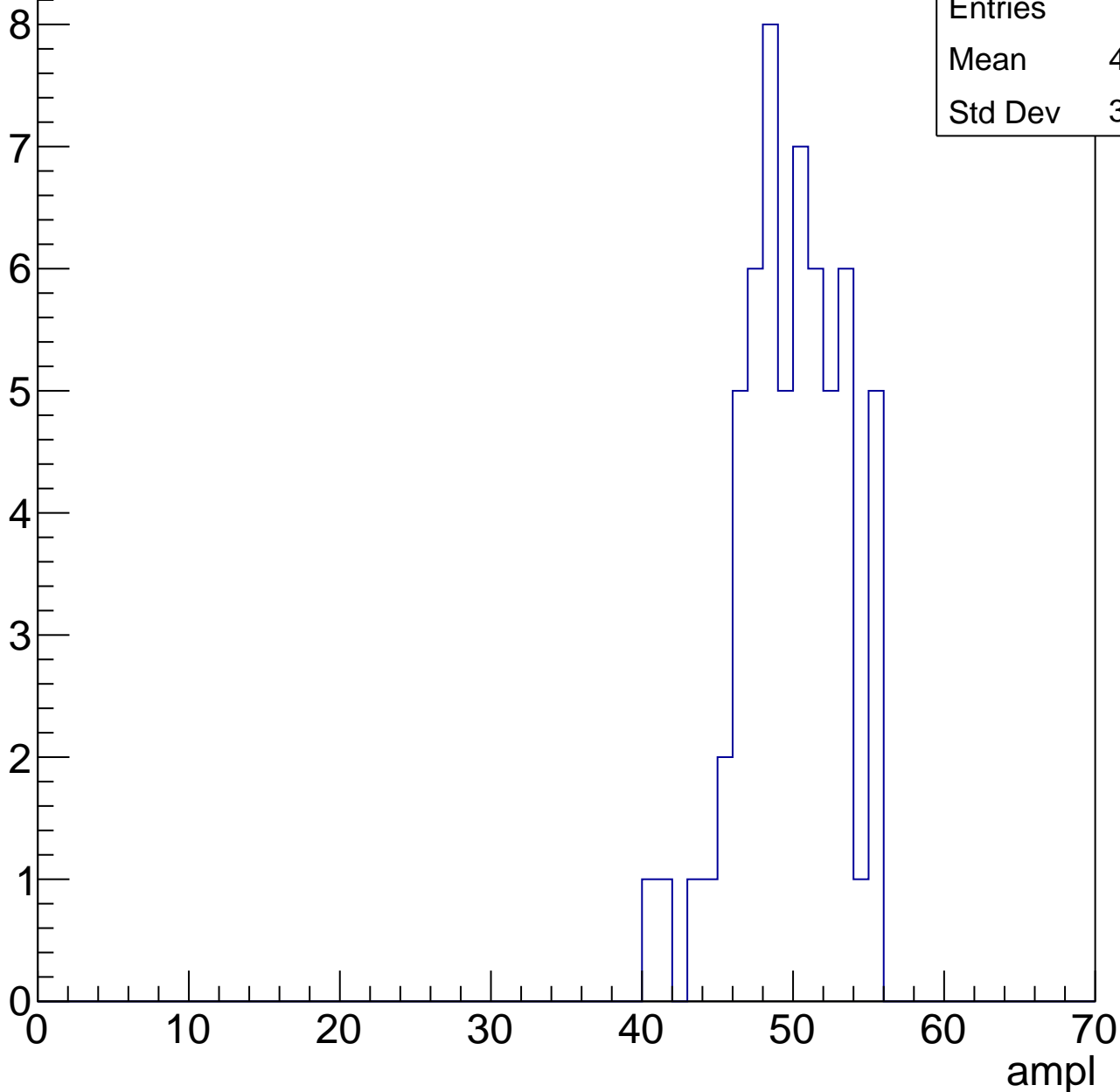


B1L103S, U5-ch43, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	49.37
Std Dev	3.376

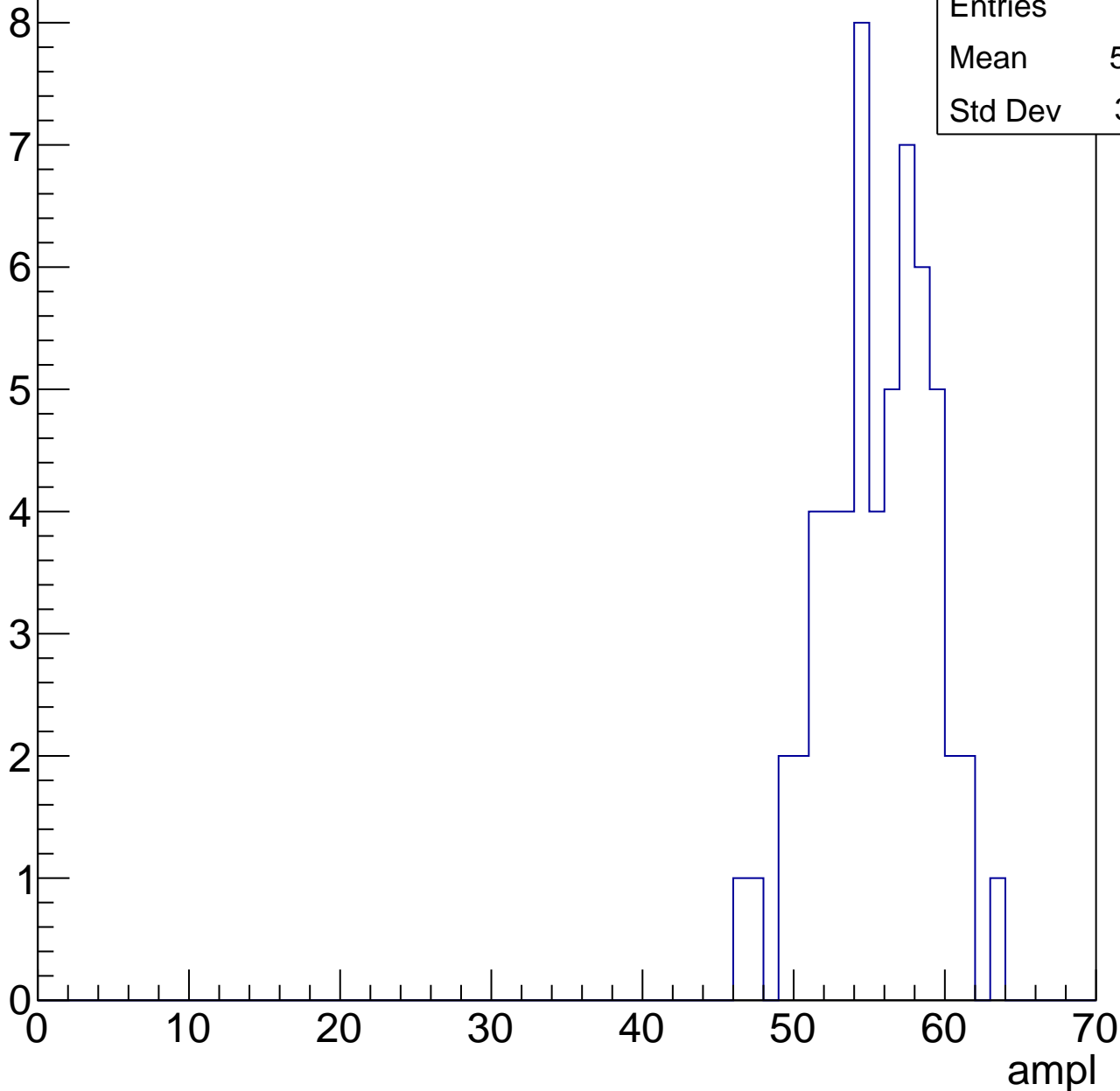


B1L103S, U5-ch43, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	55.07
Std Dev	3.581

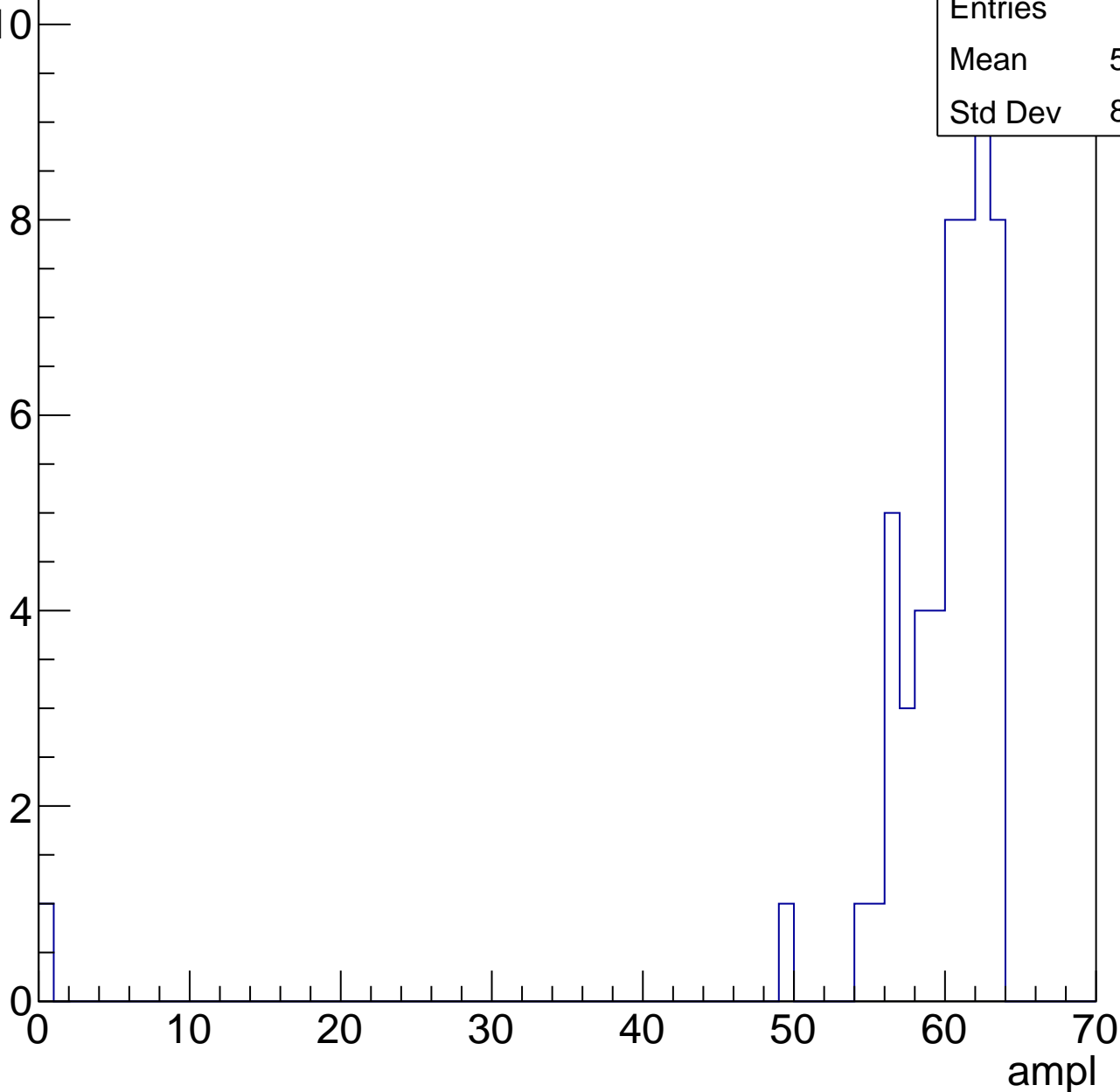


B1L103S, U5-ch43, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	58.69
Std Dev	8.537



B1L103S, U5-ch43, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

2

Mean

61

Std Dev

2

B1L103S, U5-ch43, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

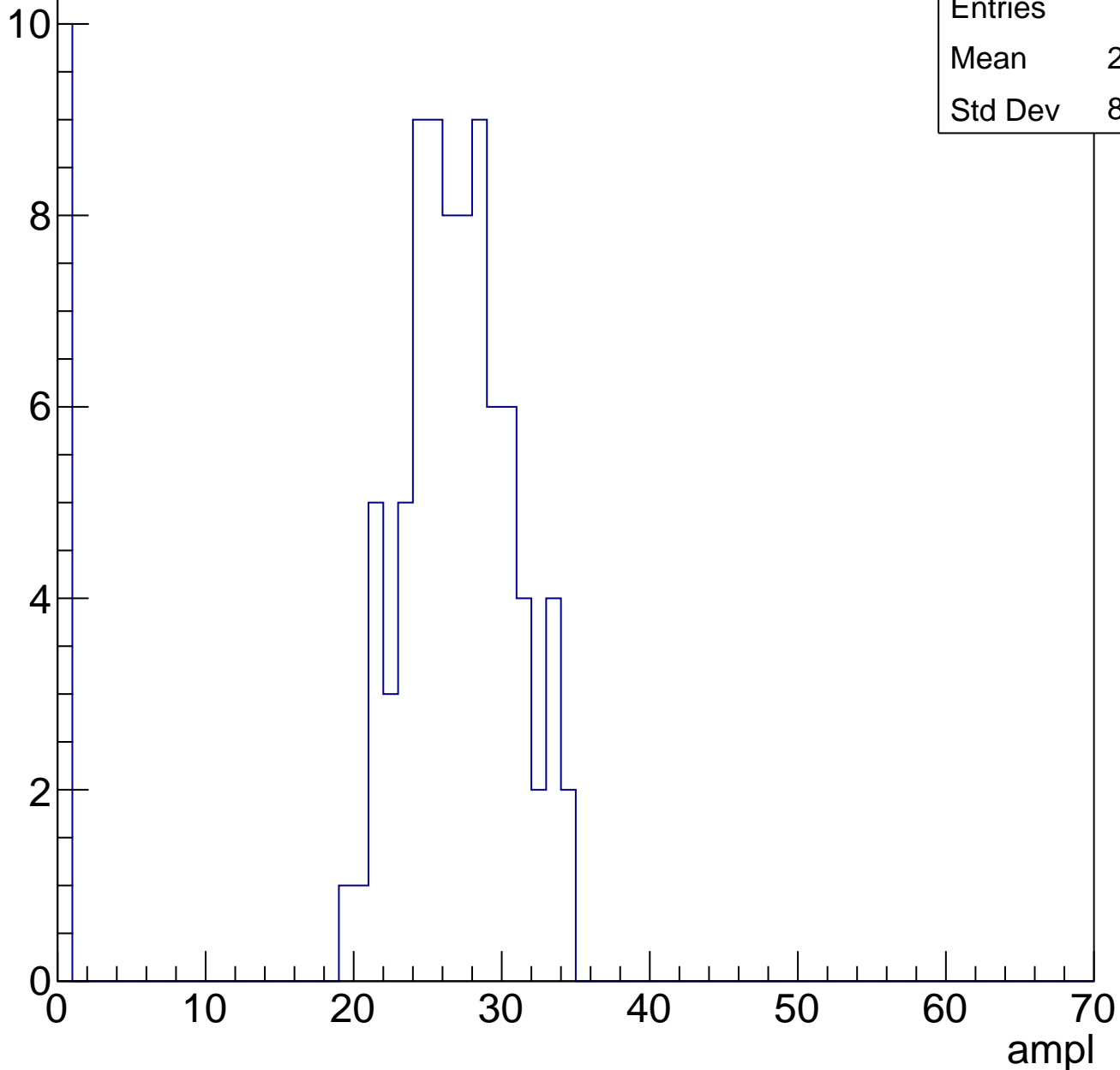


B1L103S, U5-ch44, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	92
Mean	23.74
Std Dev	8.925

Entry

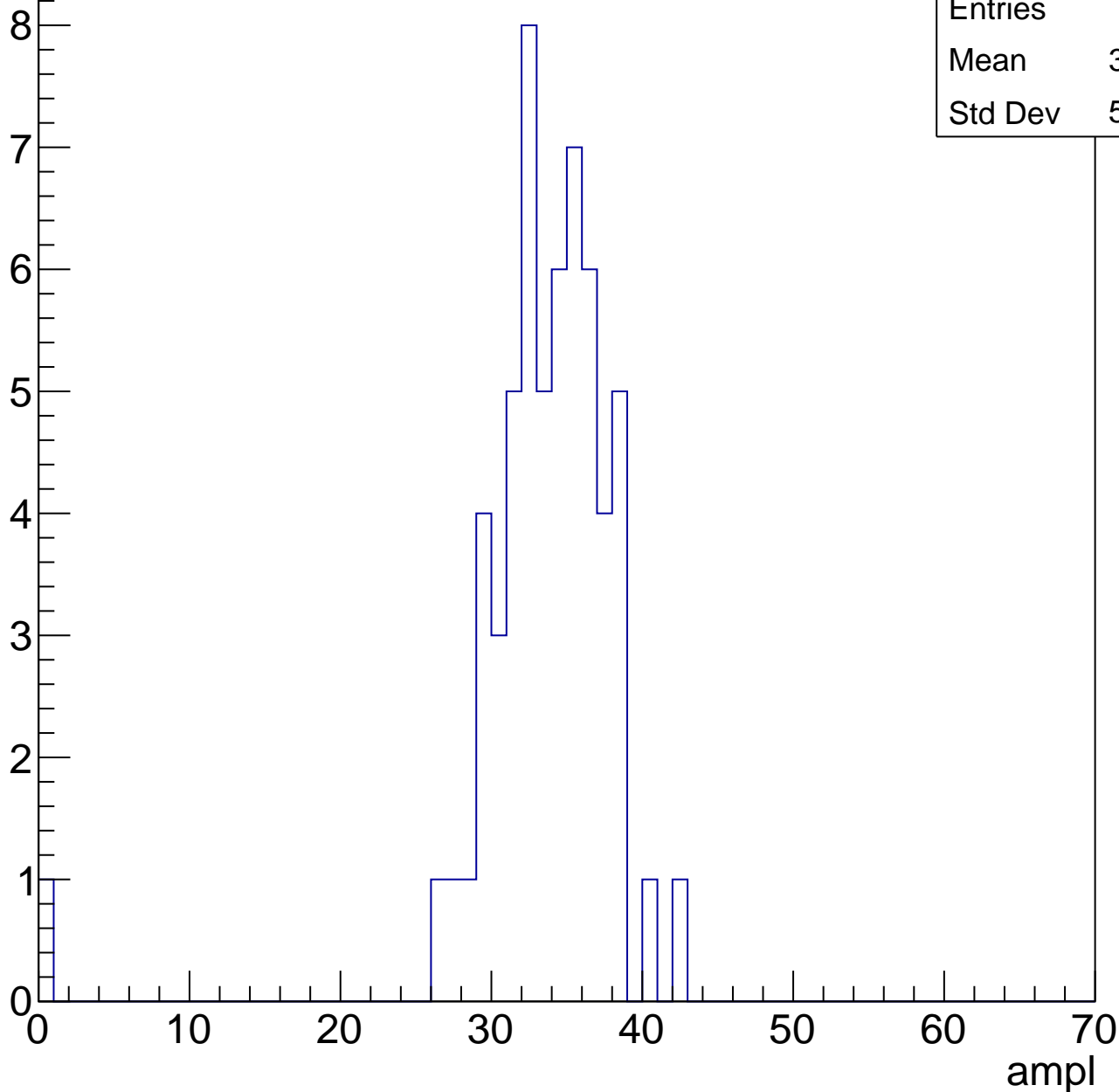


B1L103S, U5-ch44, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	33.02
Std Dev	5.407

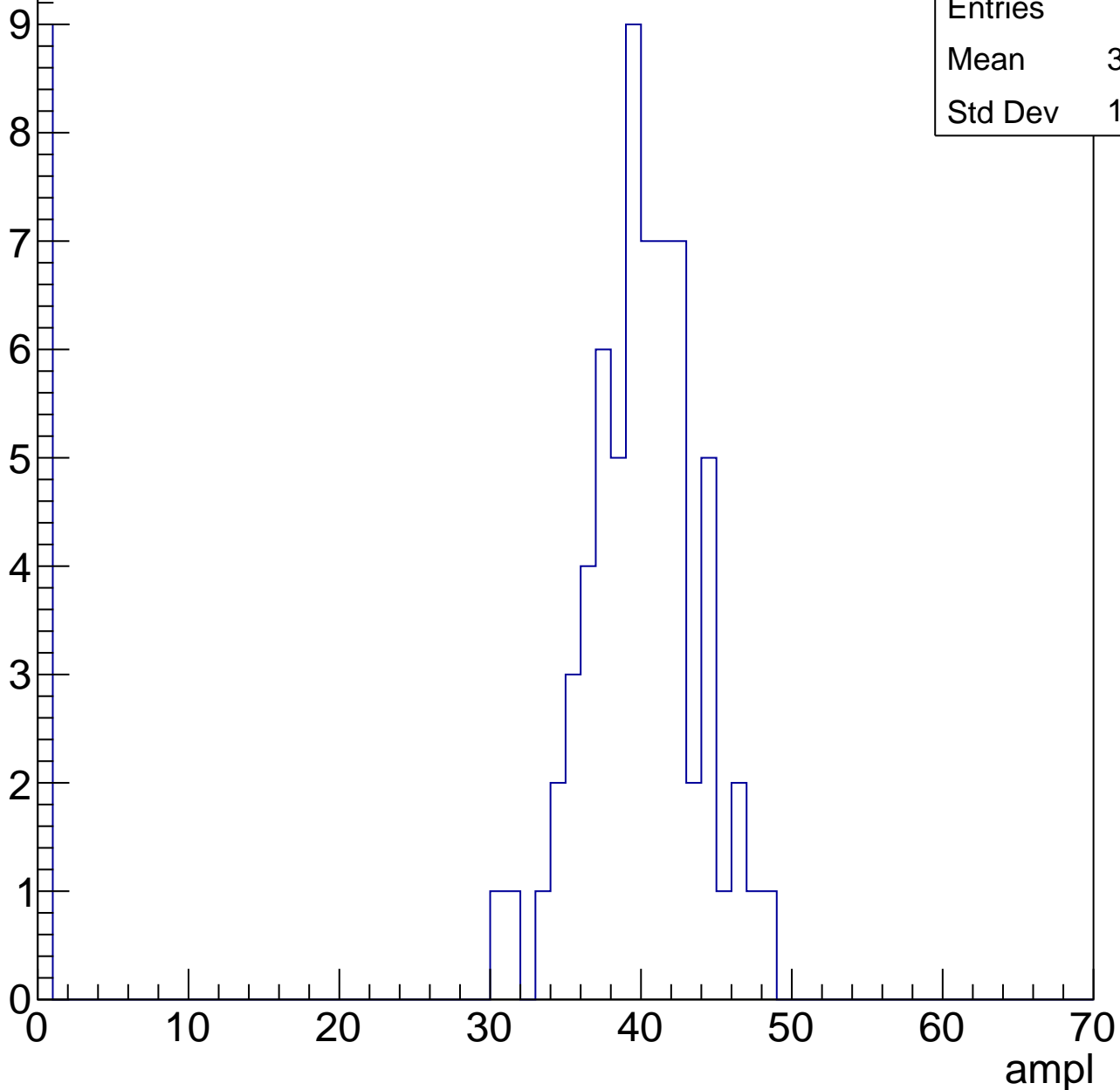


B1L103S, U5-ch44, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	34.77
Std Dev	13.38

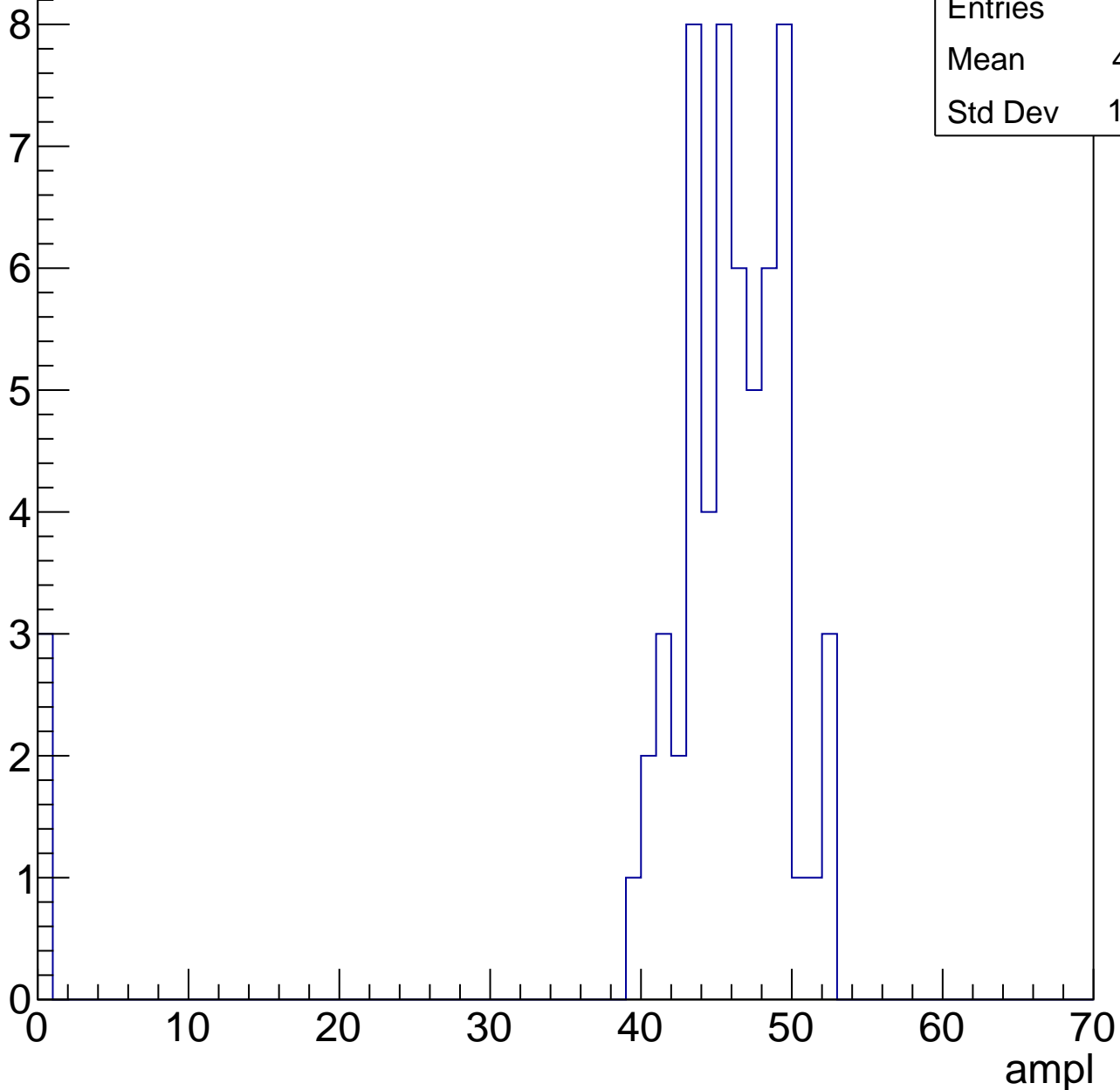


B1L103S, U5-ch44, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	43.51
Std Dev	10.36

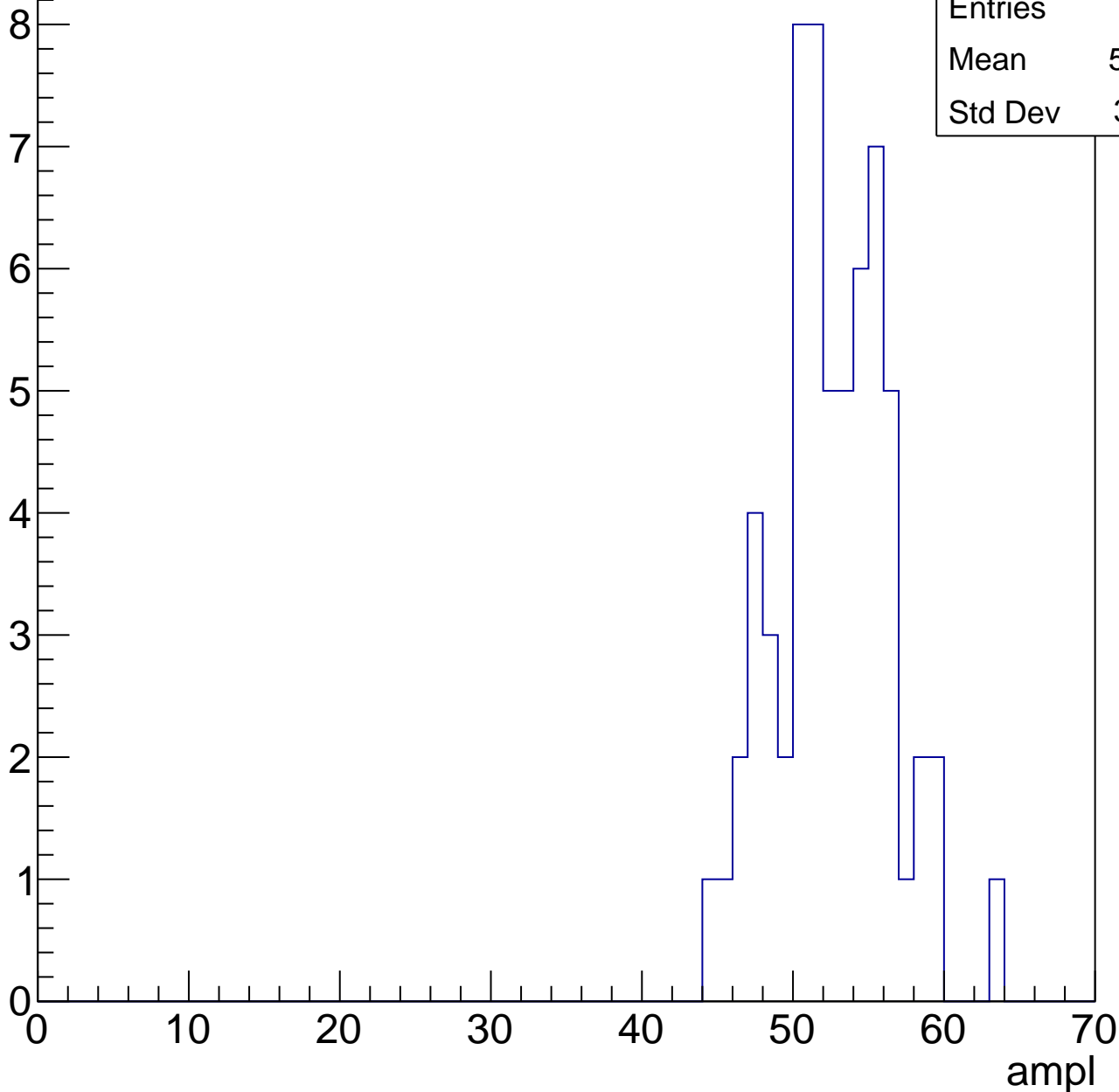


B1L103S, U5-ch44, adc4

calib_packv5_041523_1651.root, FC#0, port C2

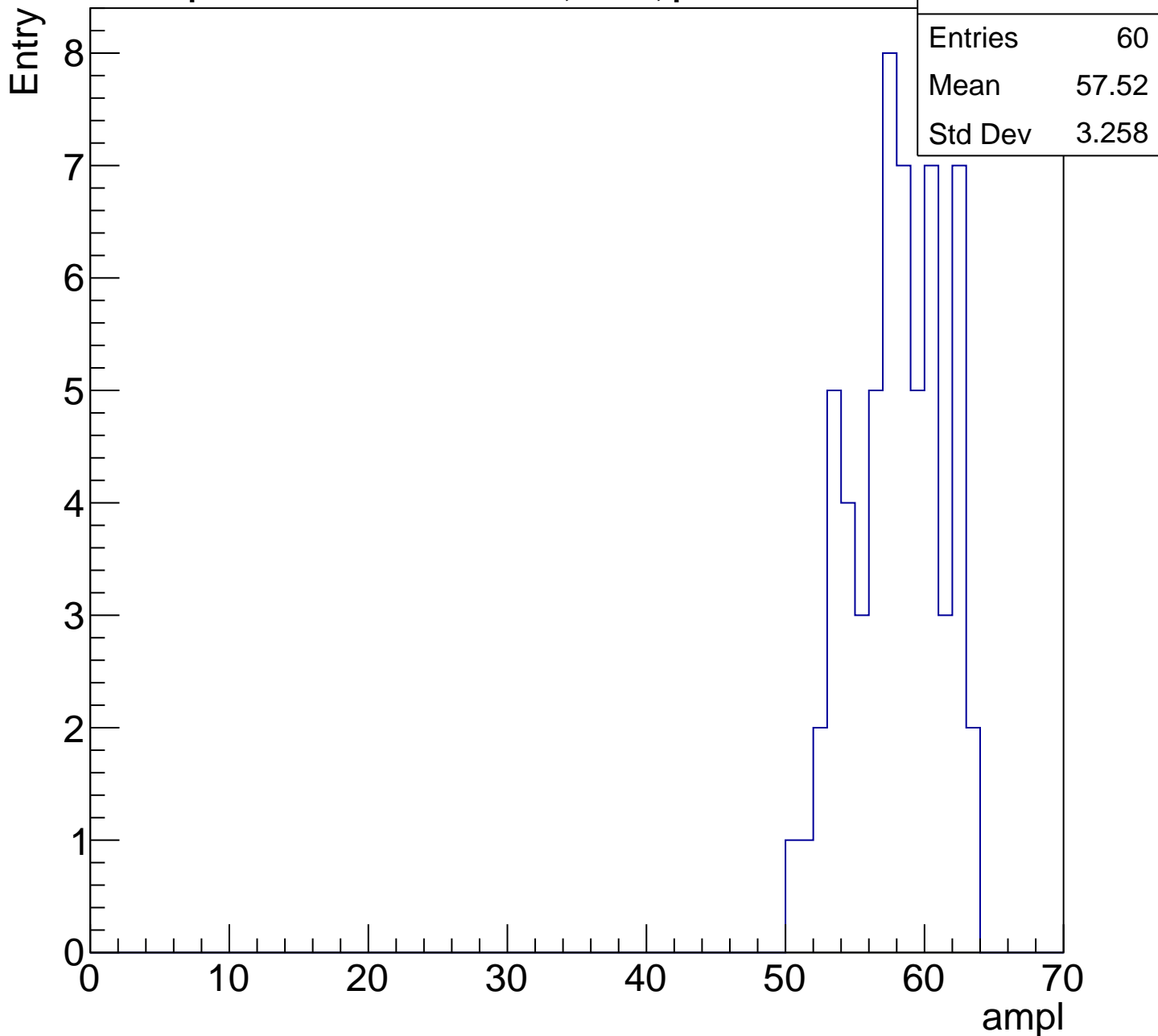
Entry

Entries	63
Mean	52.17
Std Dev	3.731



B1L103S, U5-ch44, adc5

calib_packv5_041523_1651.root, FC#0, port C2

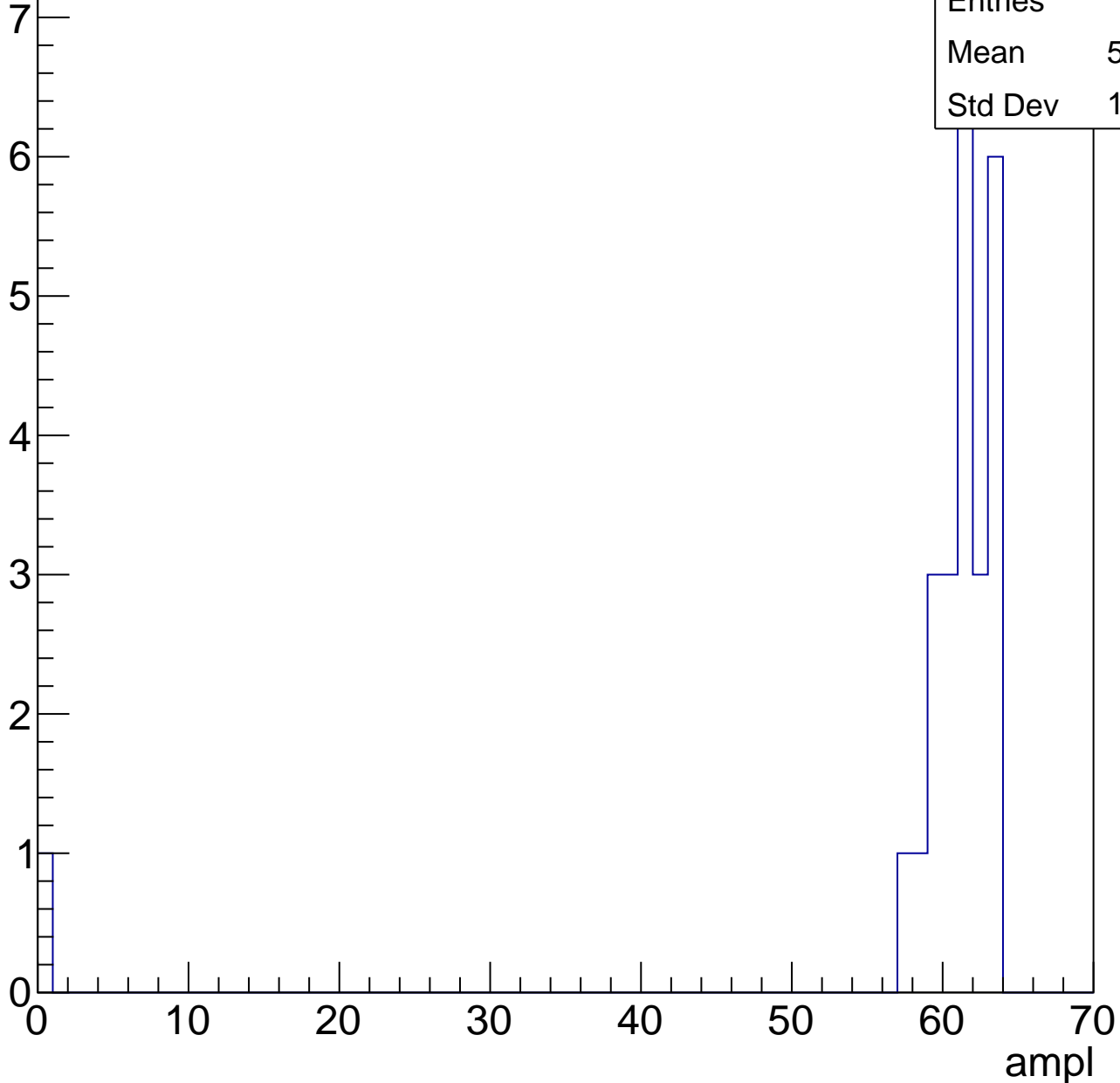


B1L103S, U5-ch44, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

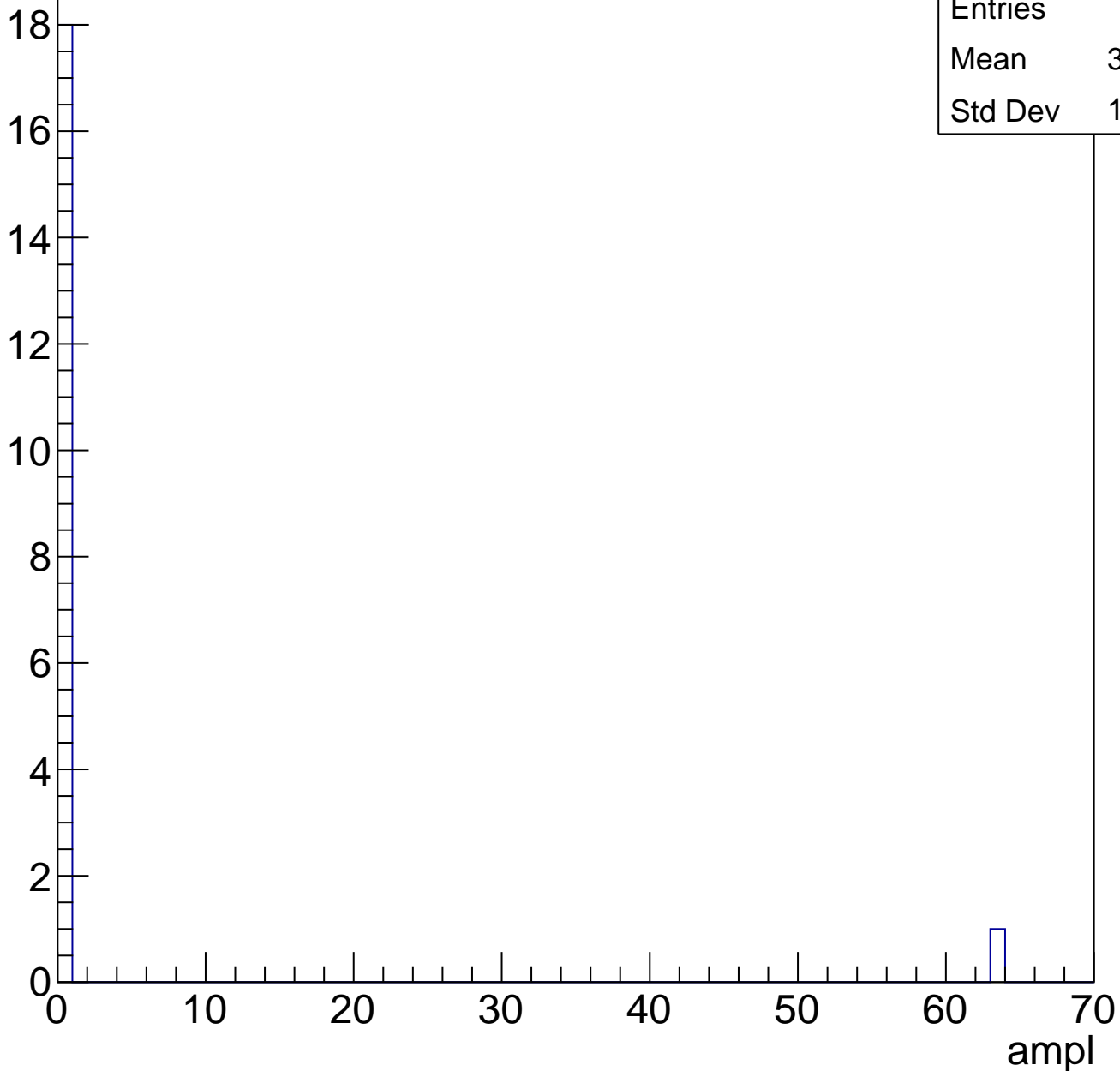
Entries	25
Mean	58.52
Std Dev	12.06



B1L103S, U5-ch44, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch45, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	66
Mean	25.11
Std Dev	11.58

Entry

10

8

6

4

2

0

0

10

20

30

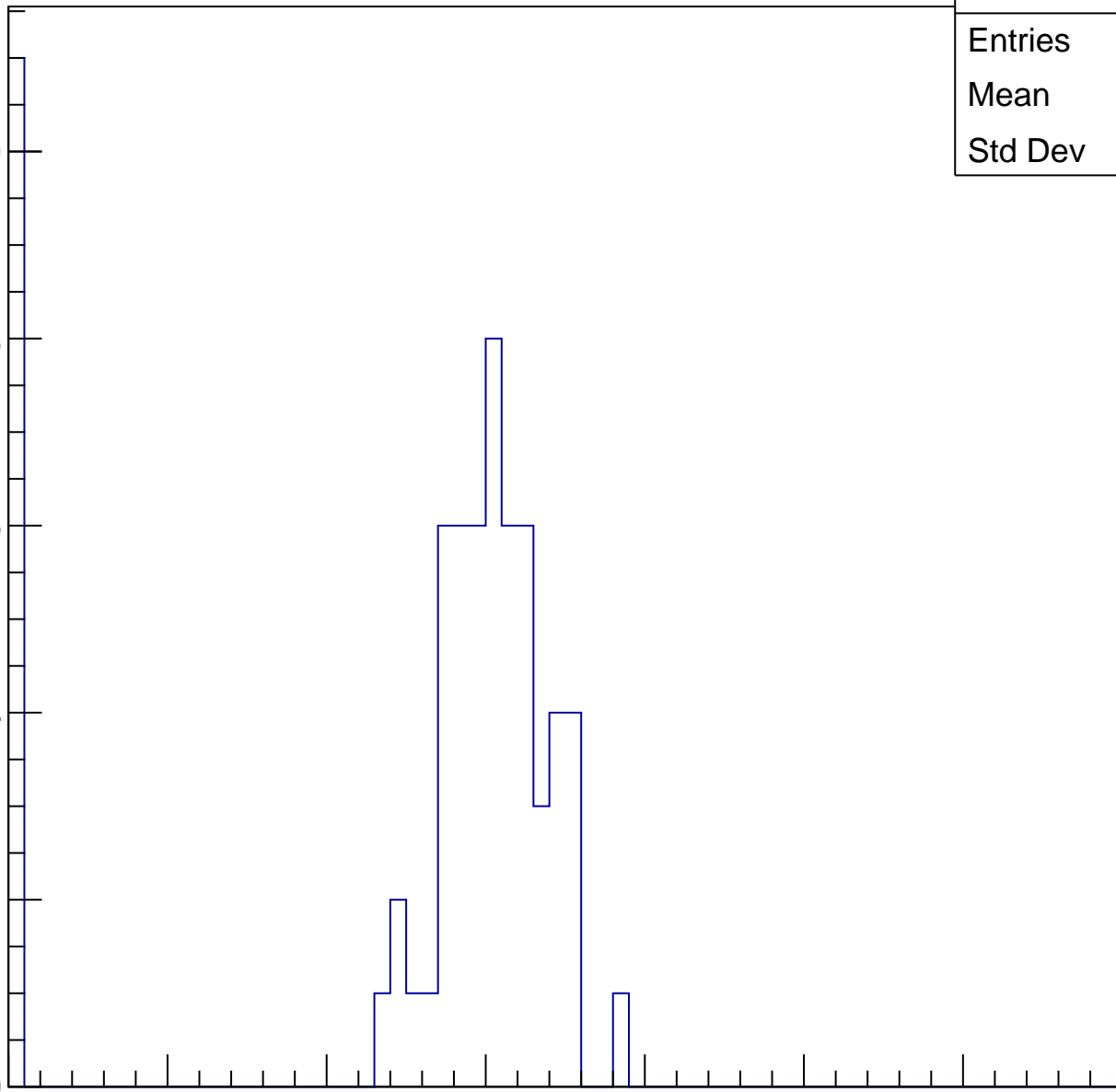
40

50

60

70

ampl

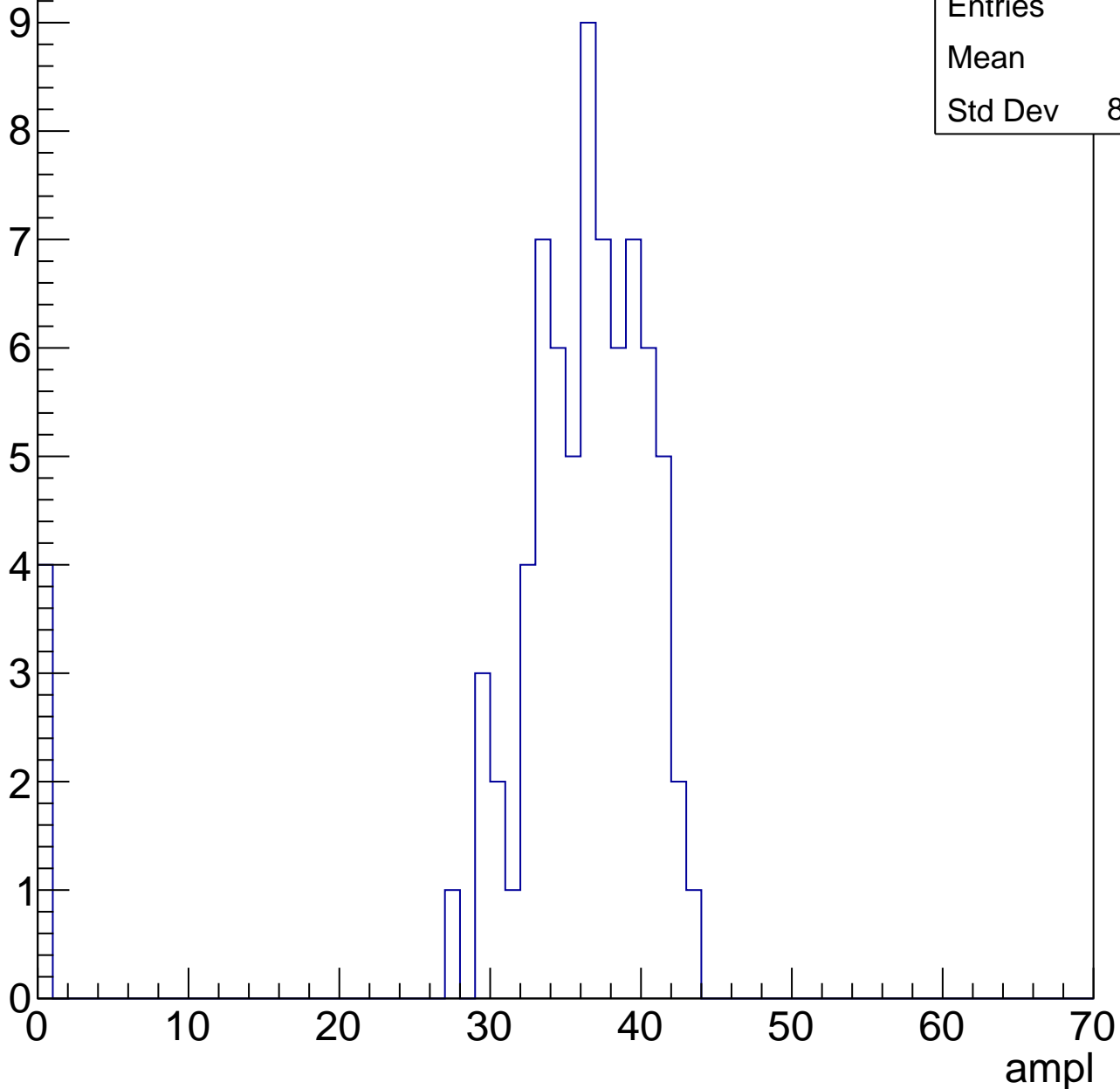


B1L103S, U5-ch45, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	34.2
Std Dev	8.776

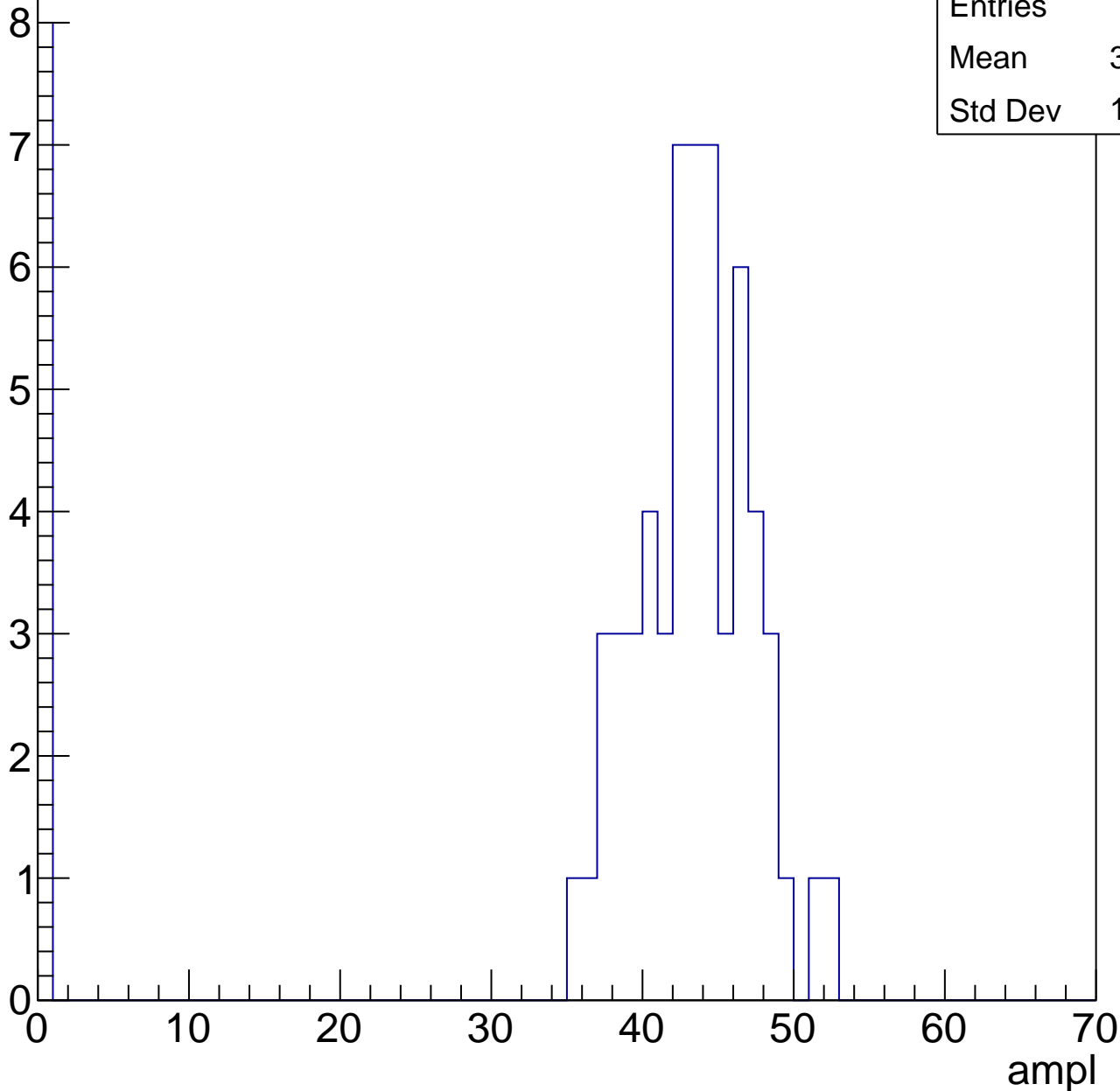


B1L103S, U5-ch45, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	37.79
Std Dev	14.46

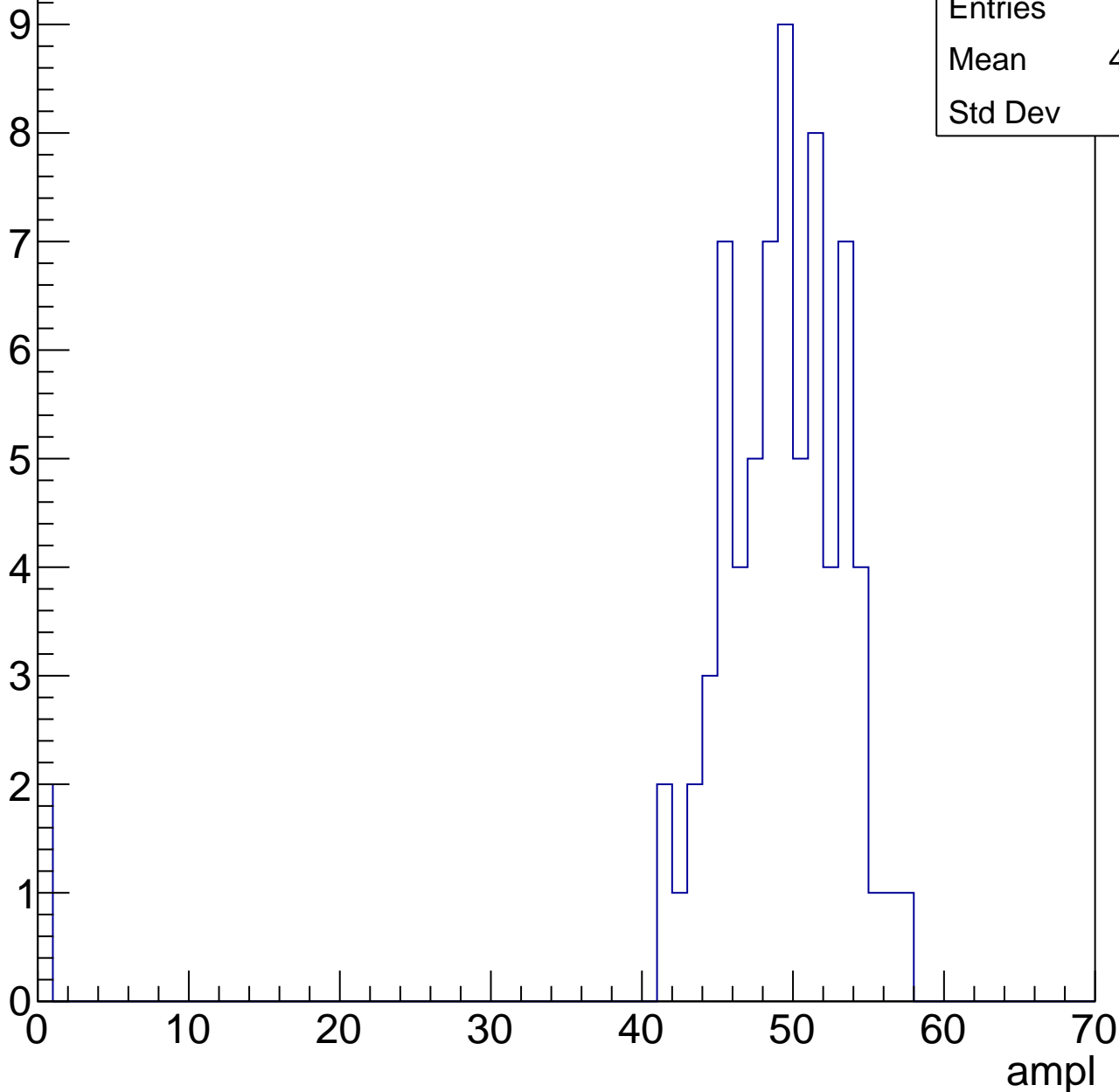


B1L103S, U5-ch45, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	47.59
Std Dev	8.75

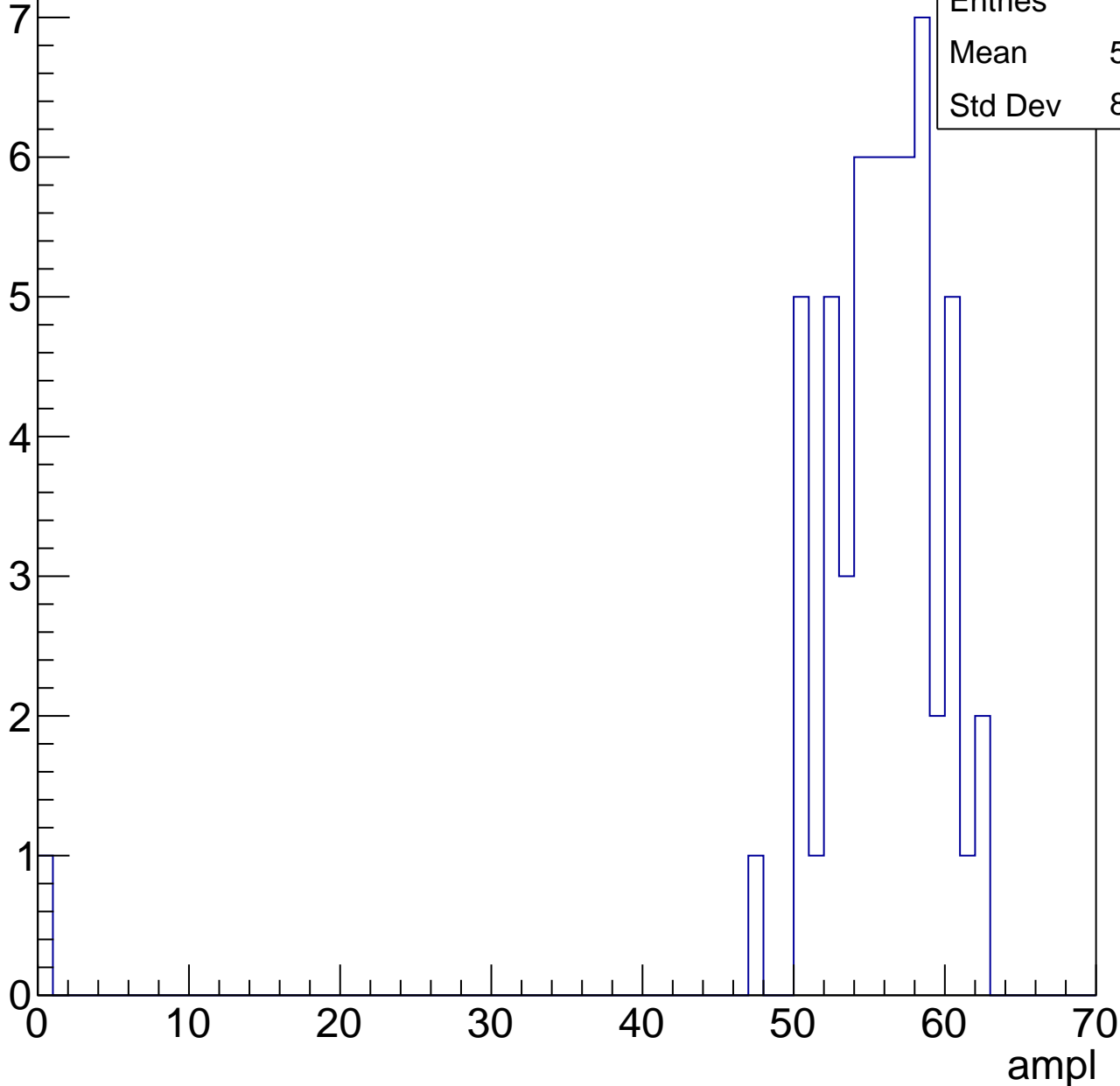


B1L103S, U5-ch45, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	54.53
Std Dev	8.018



B1L103S, U5-ch45, adc5

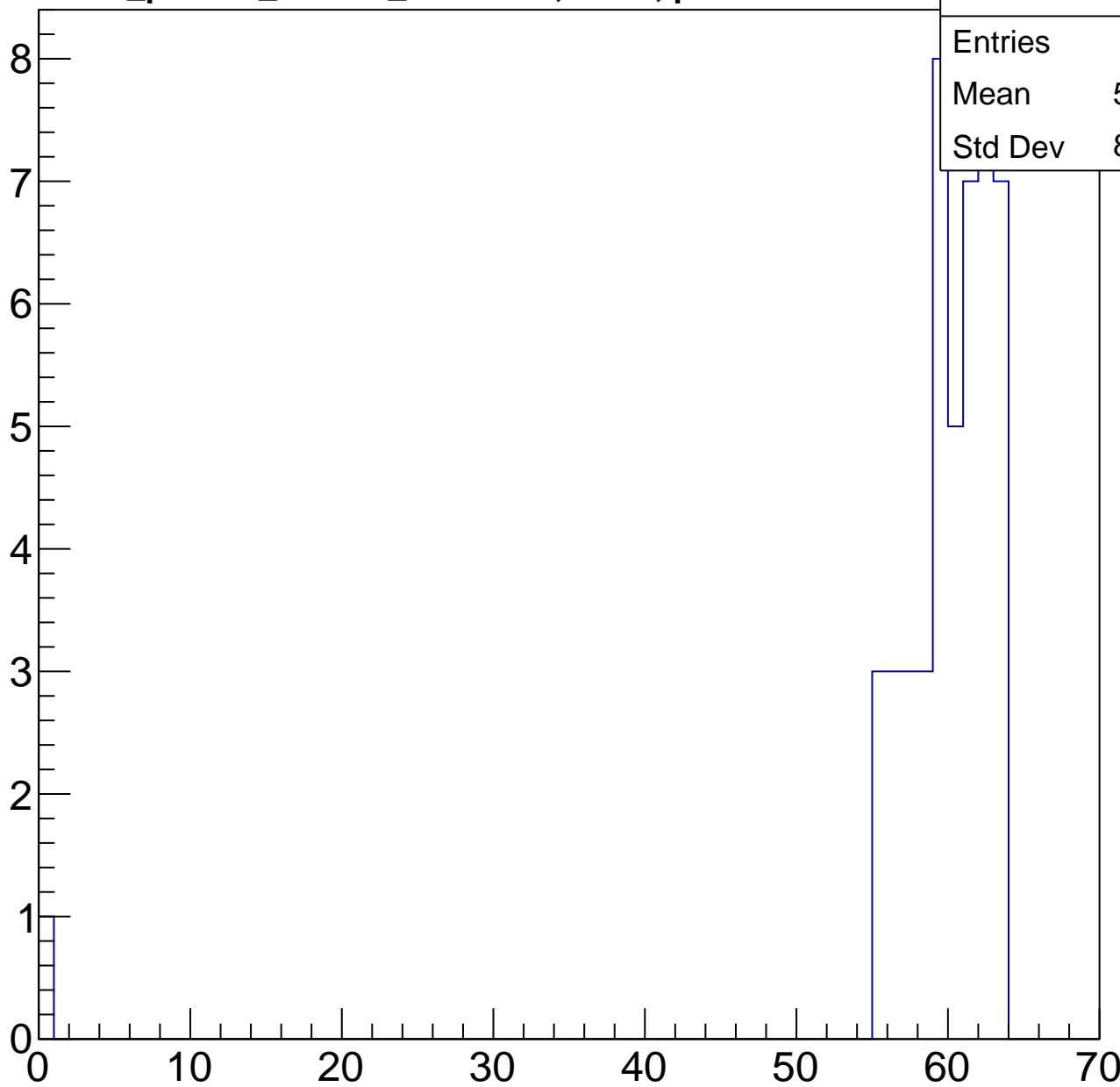
calib_packv5_041523_1651.root, FC#0, port C2

Entry

8
7
6
5
4
3
2
1
0

Entries	48
Mean	58.62
Std Dev	8.876

ampl



B1L103S, U5-ch45, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	4
Mean	62
Std Dev	1

ampl

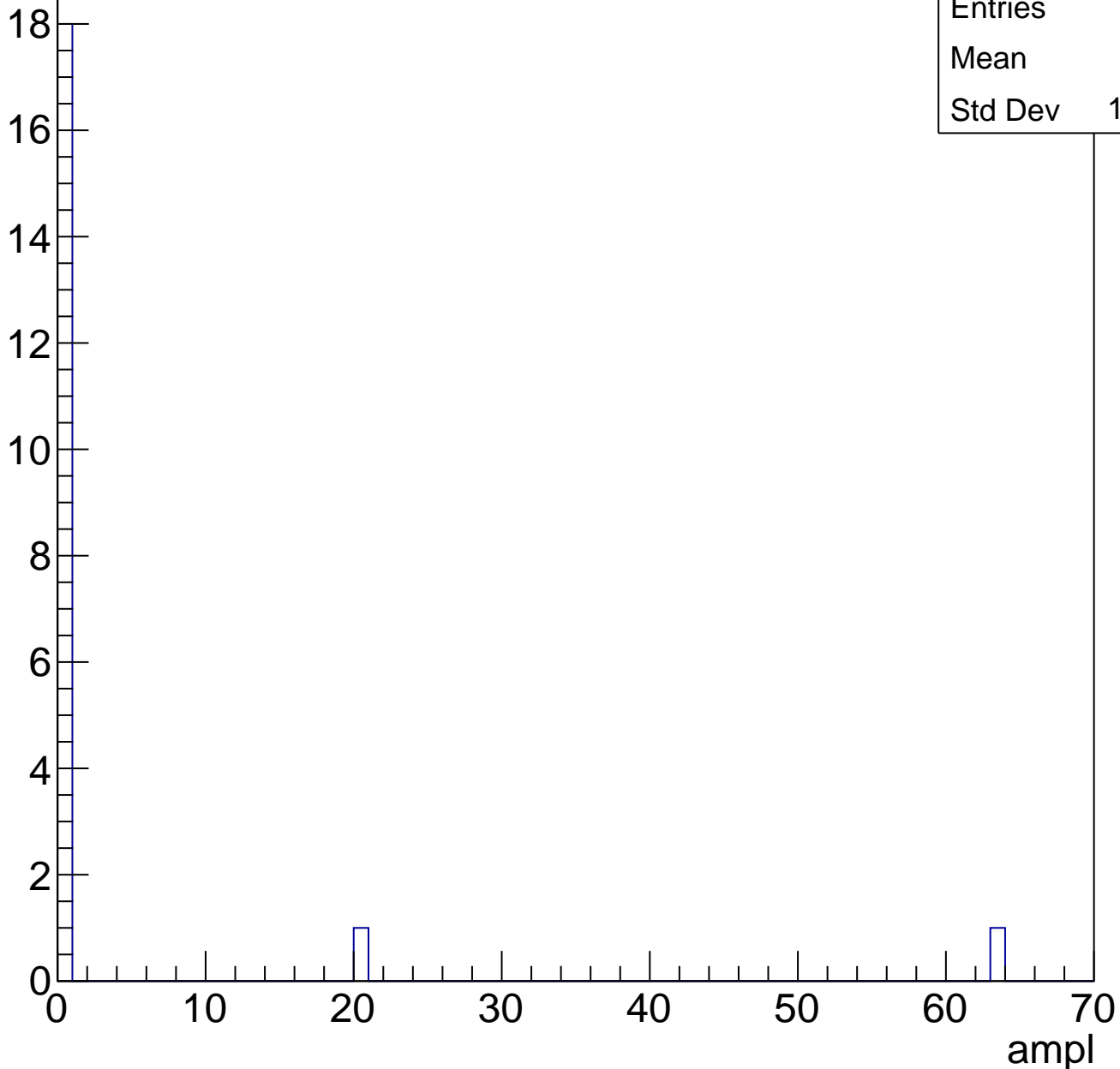
0 10 20 30 40 50 60 70

B1L103S, U5-ch45, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	4.15
Std Dev	14.19

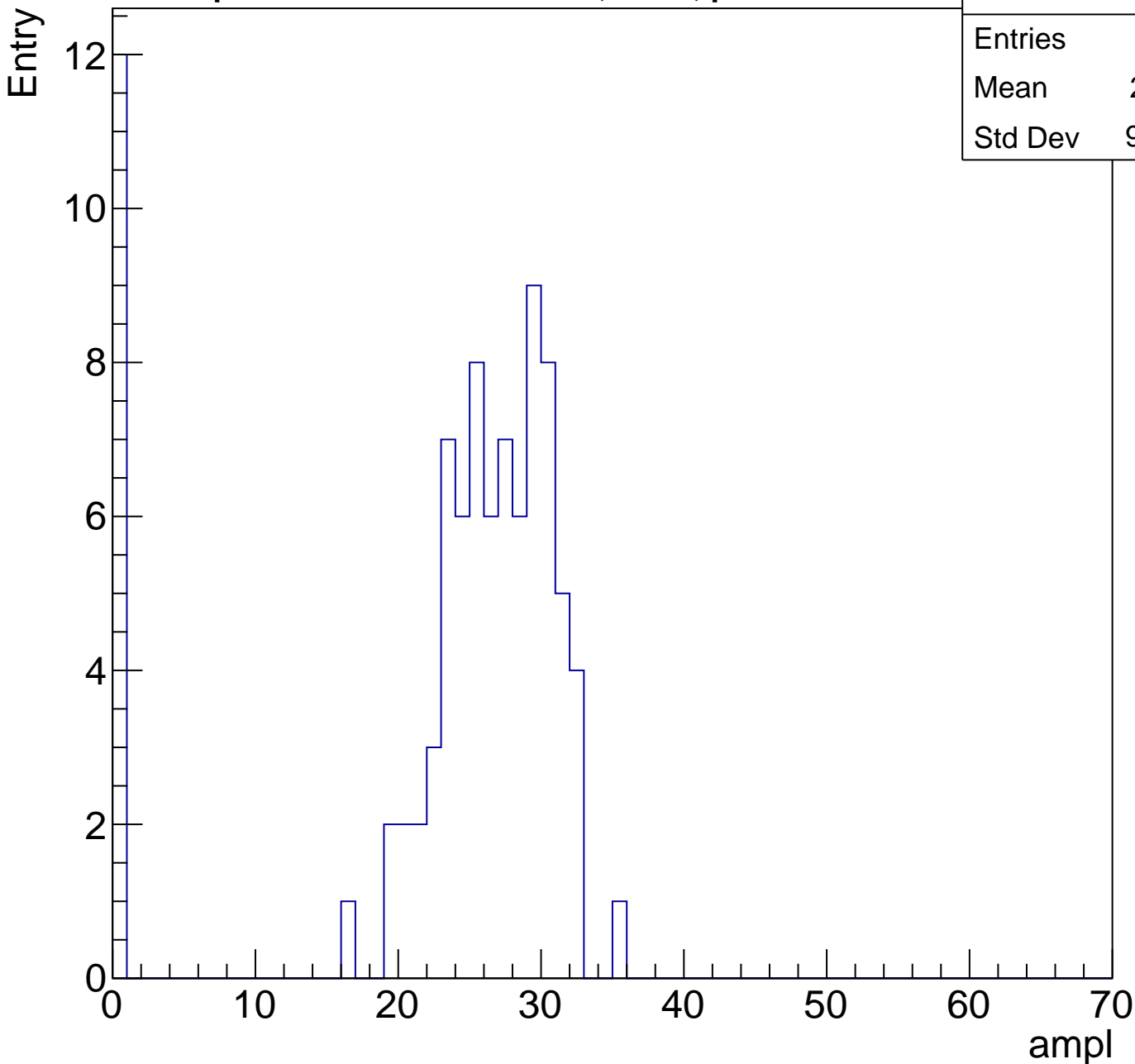
Entry



B1L103S, U5-ch46, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	22.91
Std Dev	9.666



B1L103S, U5-ch46, adc1

calib_packv5_041523_1651.root, FC#0, port C2

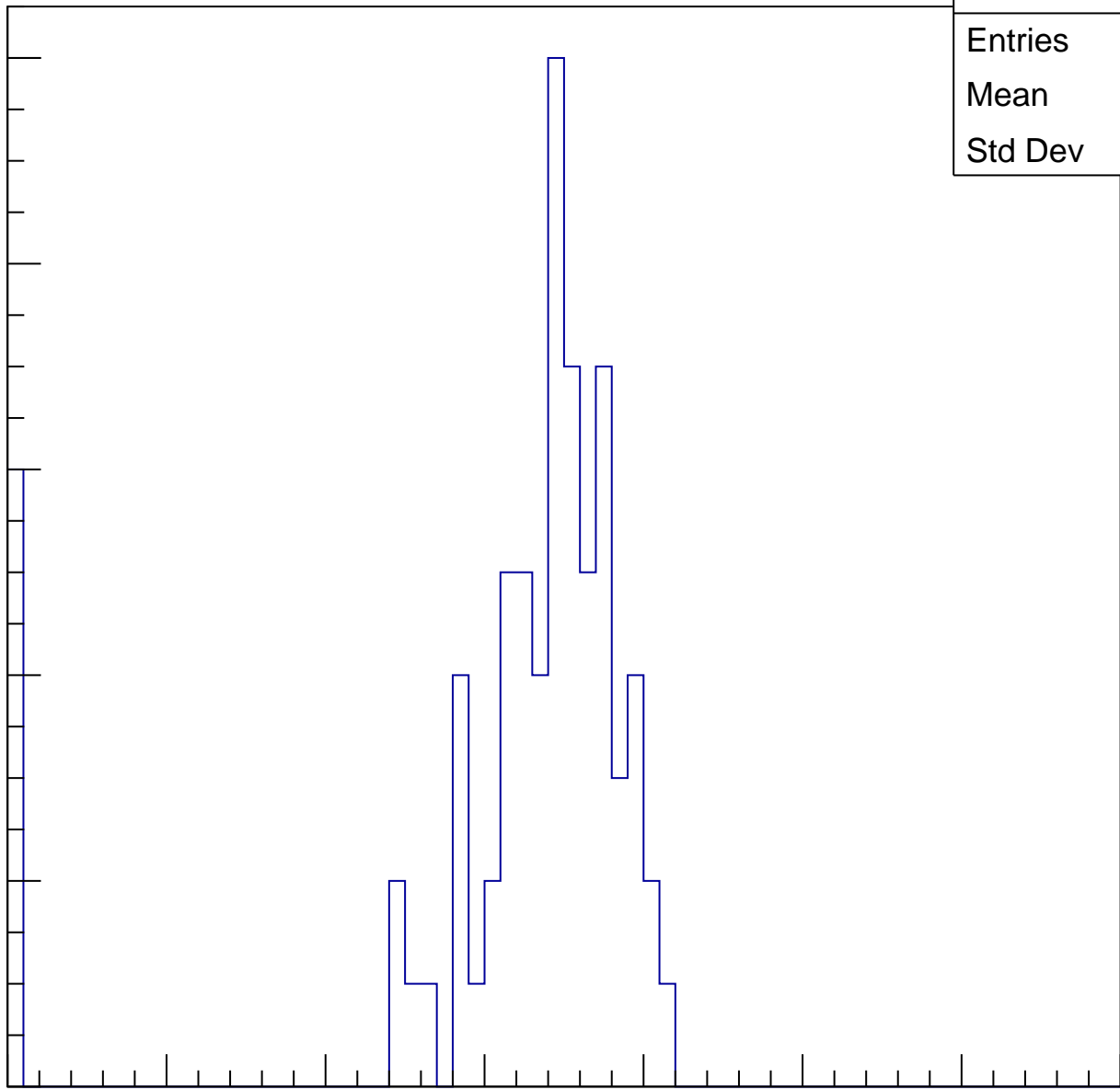
Entries	70
Mean	30.89
Std Dev	10.16

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

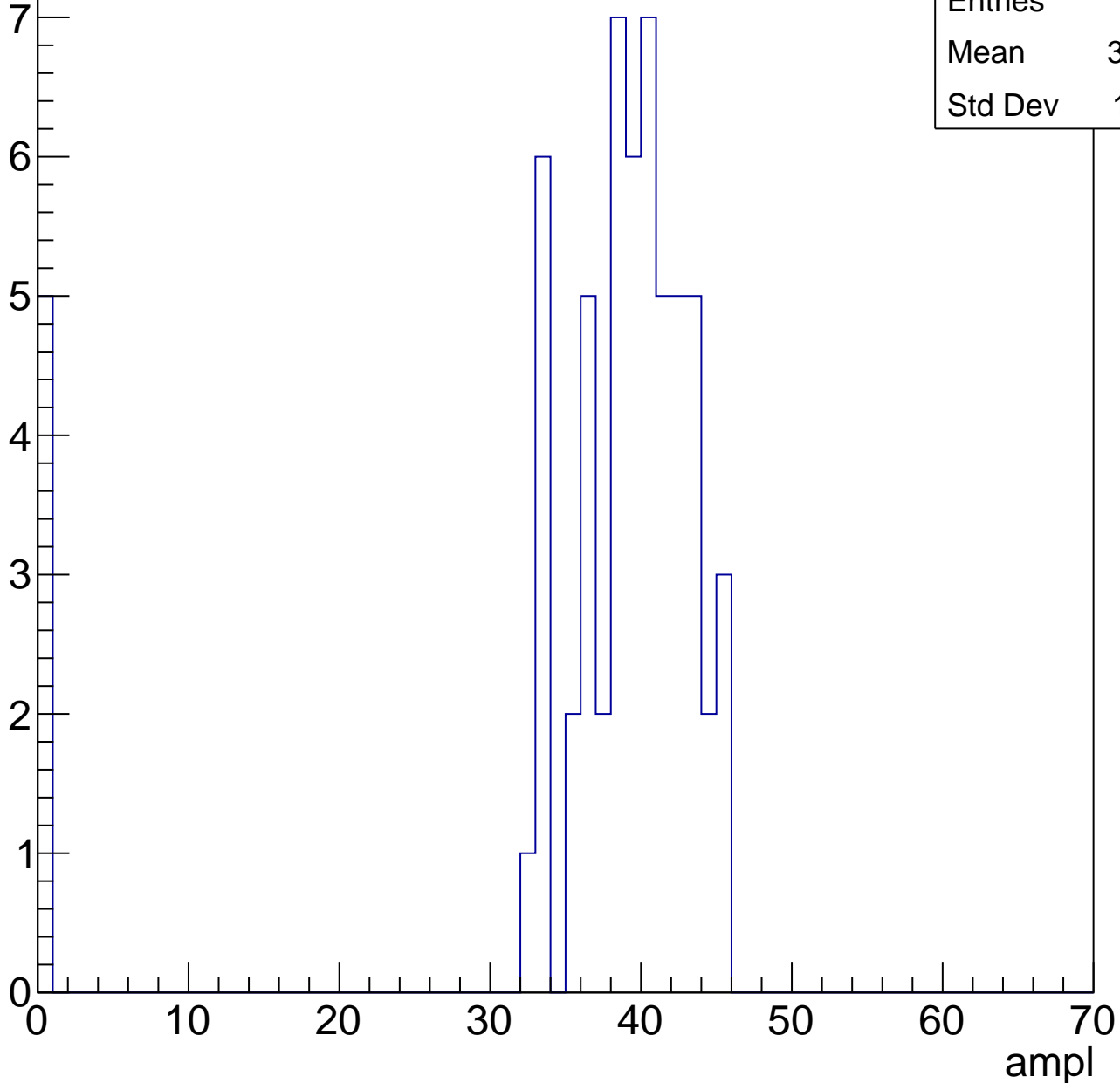


B1L103S, U5-ch46, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	35.85
Std Dev	11.21



B1L103S, U5-ch46, adc3

calib_packv5_041523_1651.root, FC#0, port C2

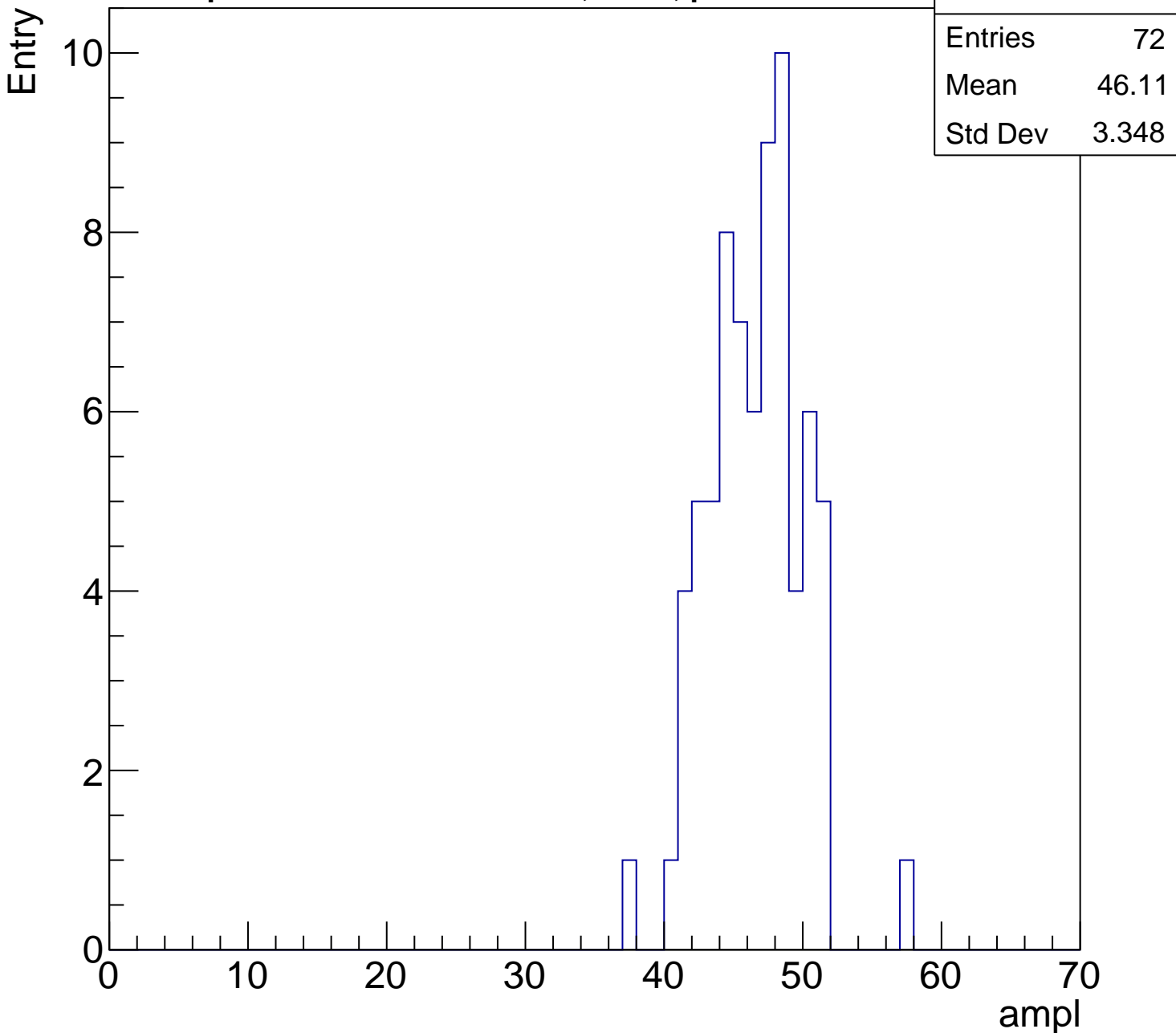
Entries	72
Mean	46.11
Std Dev	3.348

Entry

10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

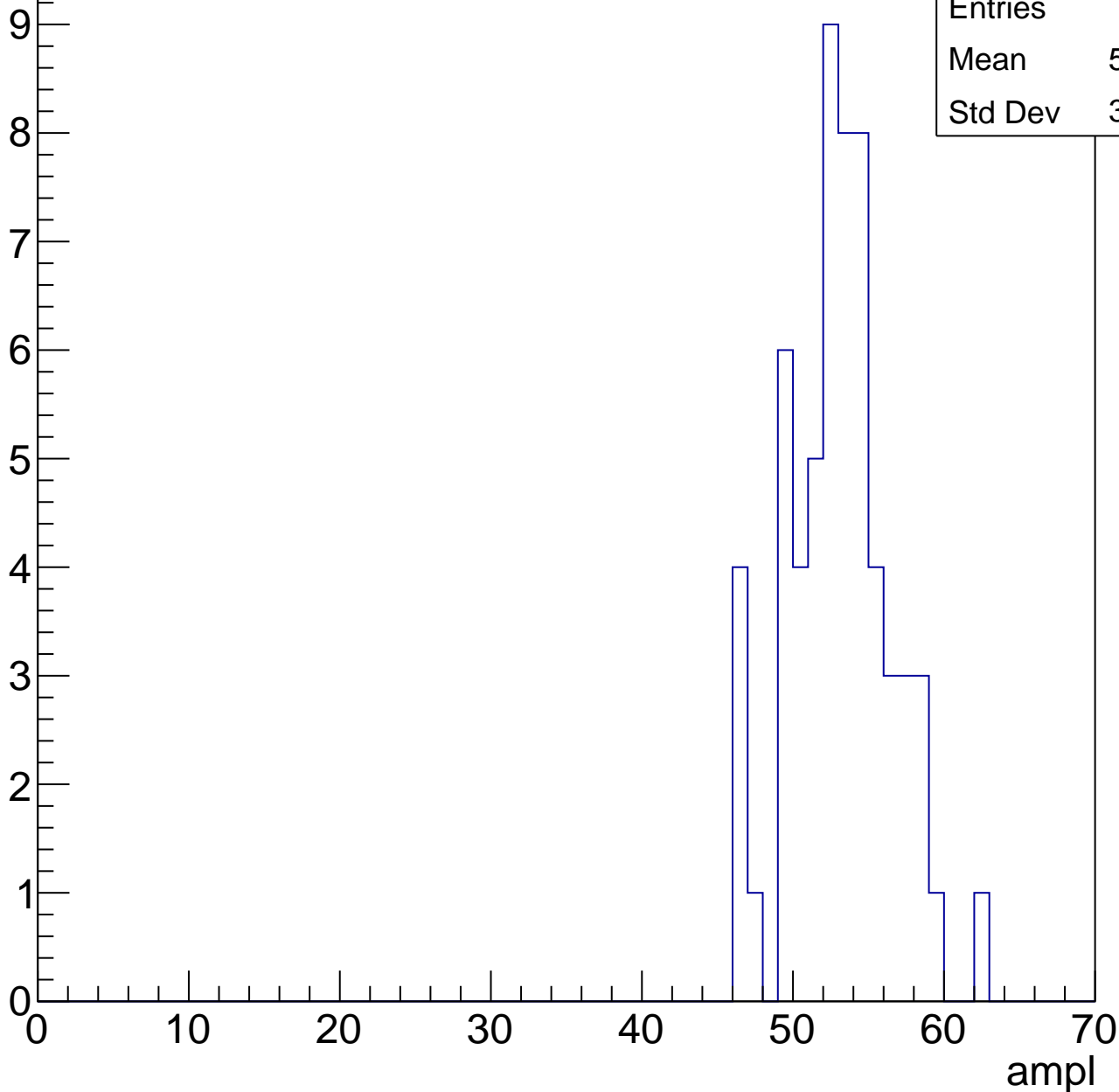


B1L103S, U5-ch46, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	52.63
Std Dev	3.356



B1L103S, U5-ch46, adc5

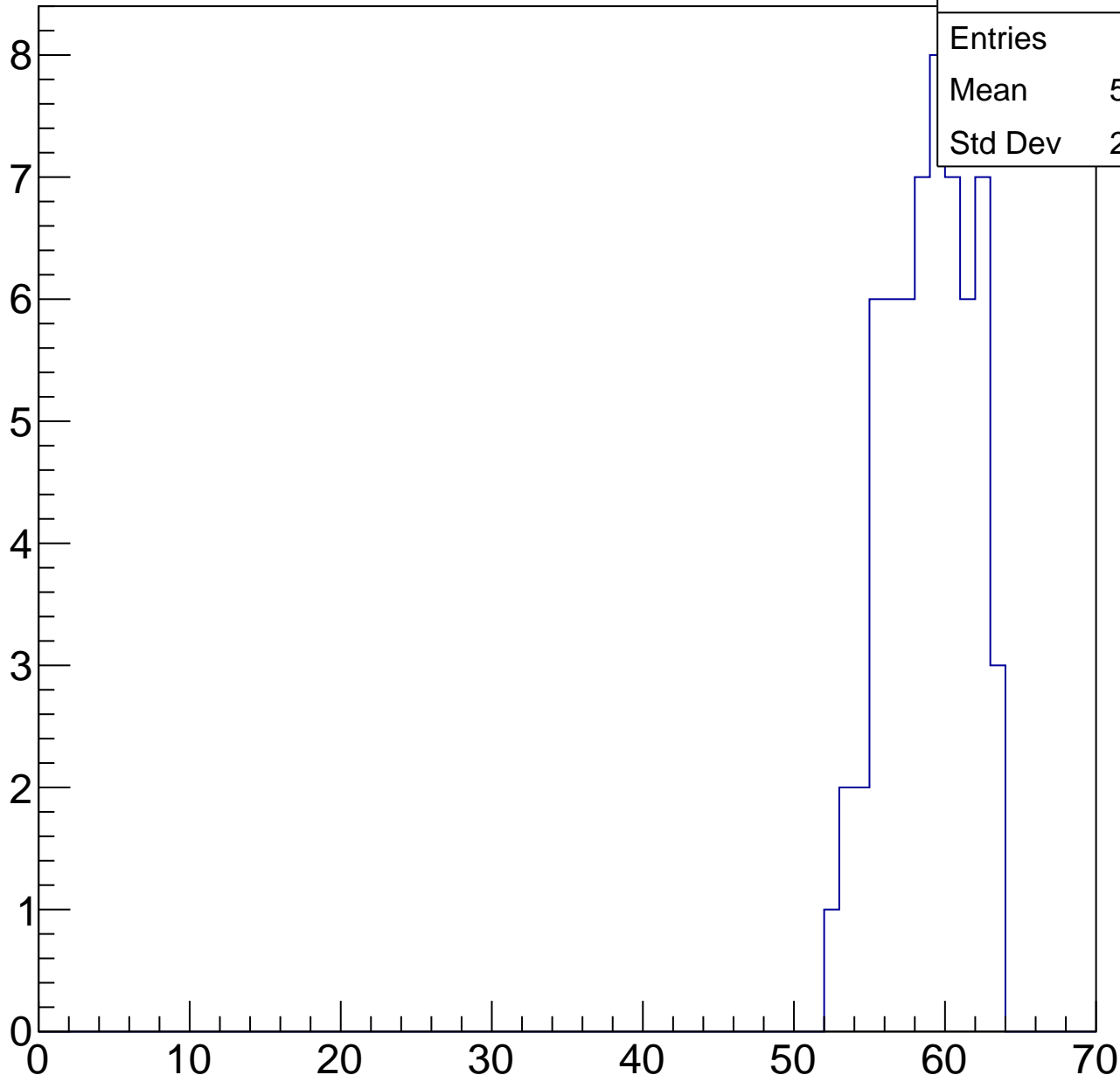
calib_packv5_041523_1651.root, FC#0, port C2

Entry

8
7
6
5
4
3
2
1
0

Entries	61
Mean	58.38
Std Dev	2.777

ampl

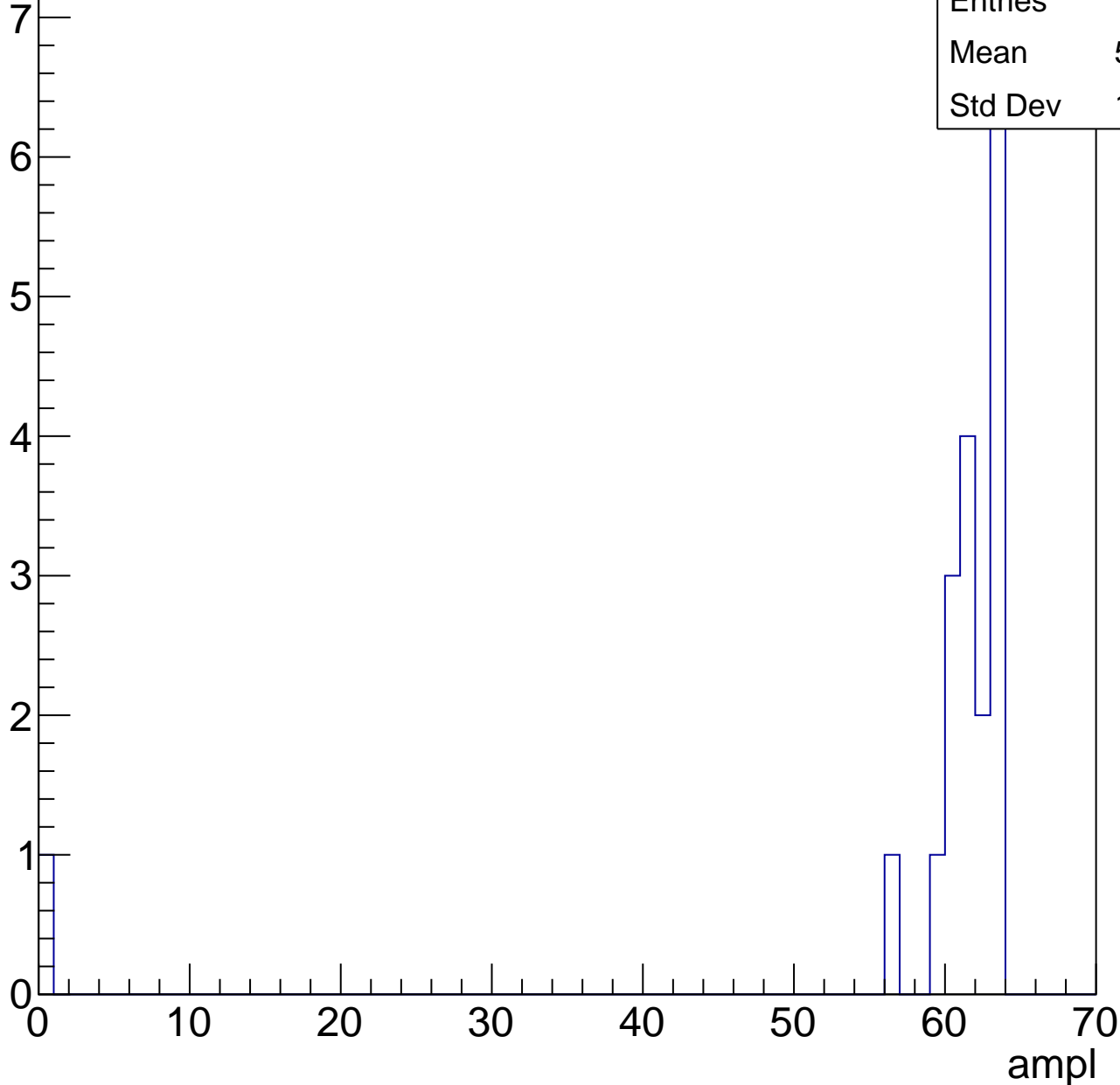


B1L103S, U5-ch46, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	19
Mean	58.11
Std Dev	13.81



B1L103S, U5-ch46, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



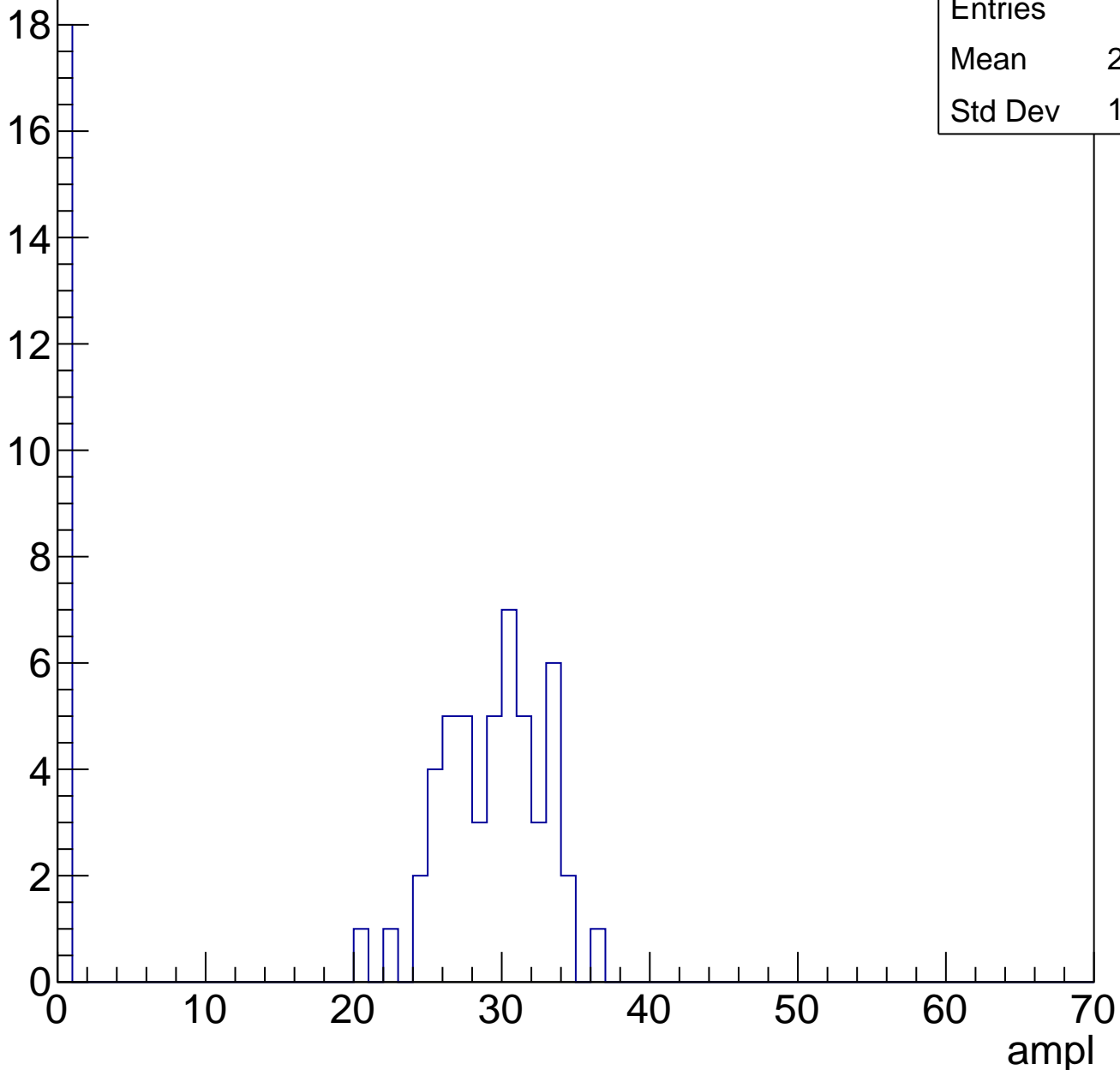
Entries	19
Mean	0
Std Dev	0

B1L103S, U5-ch47, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	68
Mean	21.28
Std Dev	13.09

Entry



B1L103S, U5-ch47, adc1

calib_packv5_041523_1651.root, FC#0, port C2

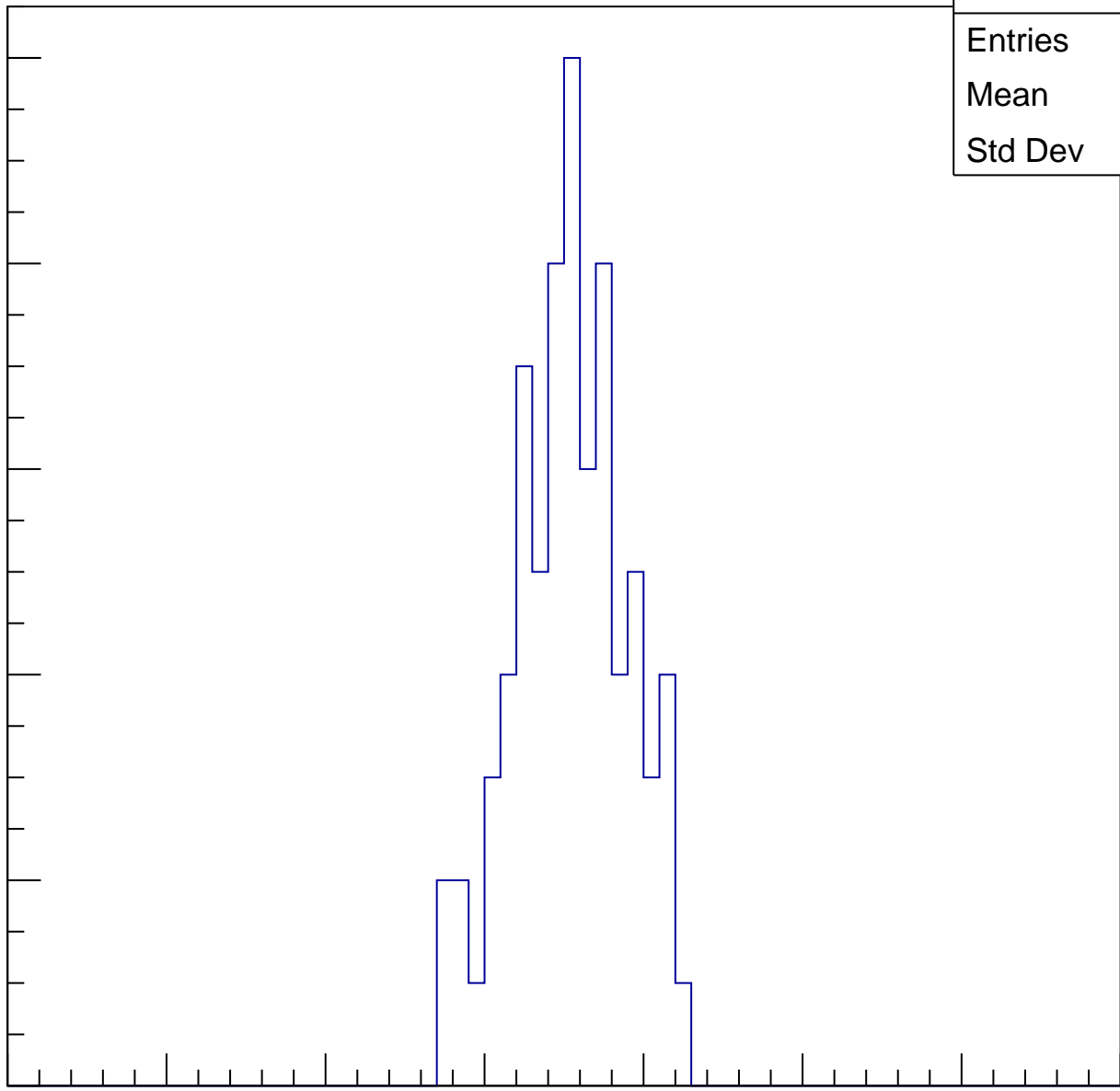
Entries	73
Mean	34.92
Std Dev	3.537

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl



B1L103S, U5-ch47, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	83
Mean	36.46
Std Dev	14.6

Entry

10

8

6

4

2

0

ampl

0

10

20

30

40

50

60

70

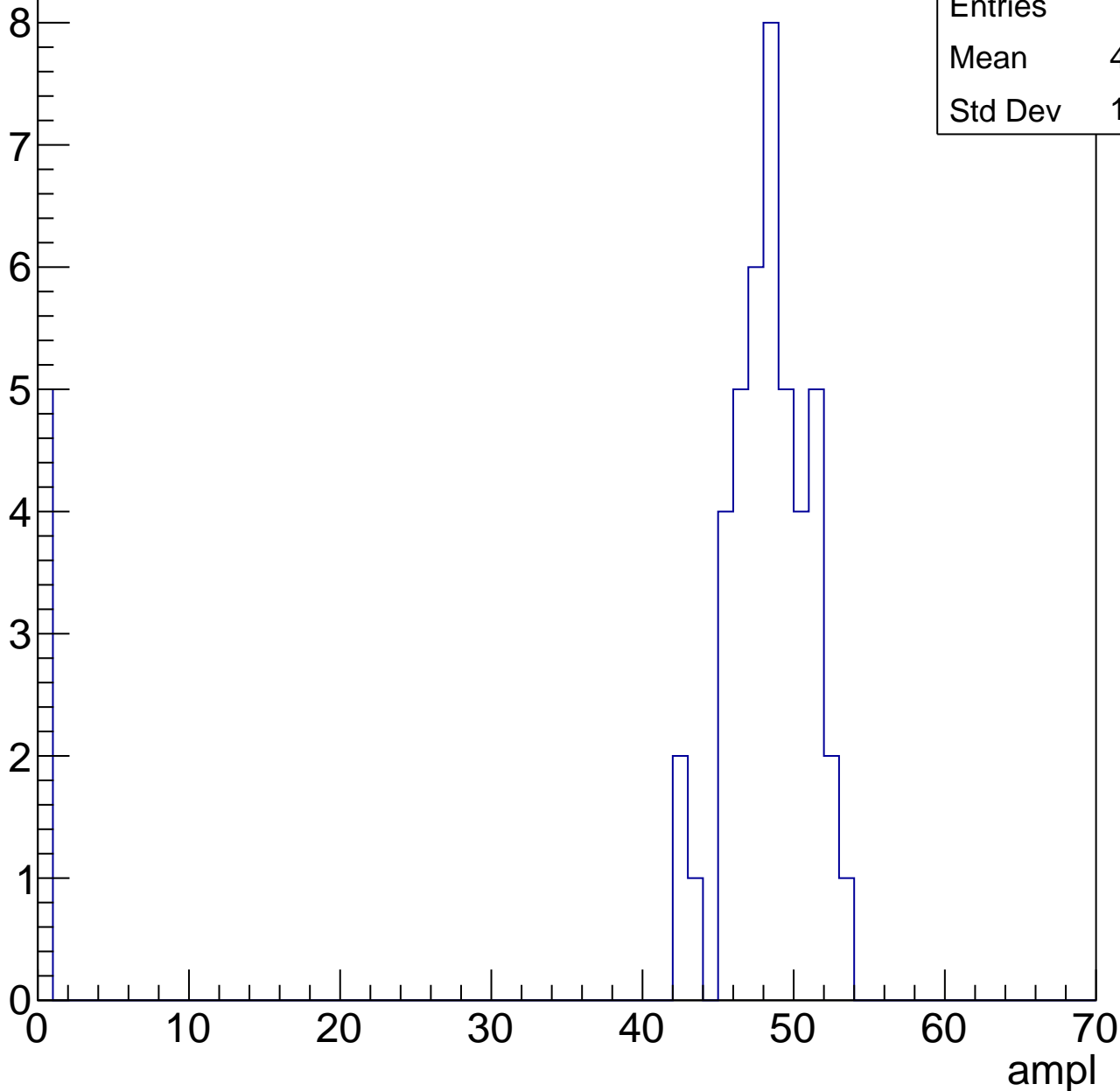
36.46

B1L103S, U5-ch47, adc3

calib_packv5_041523_1651.root, FC#0, port C2

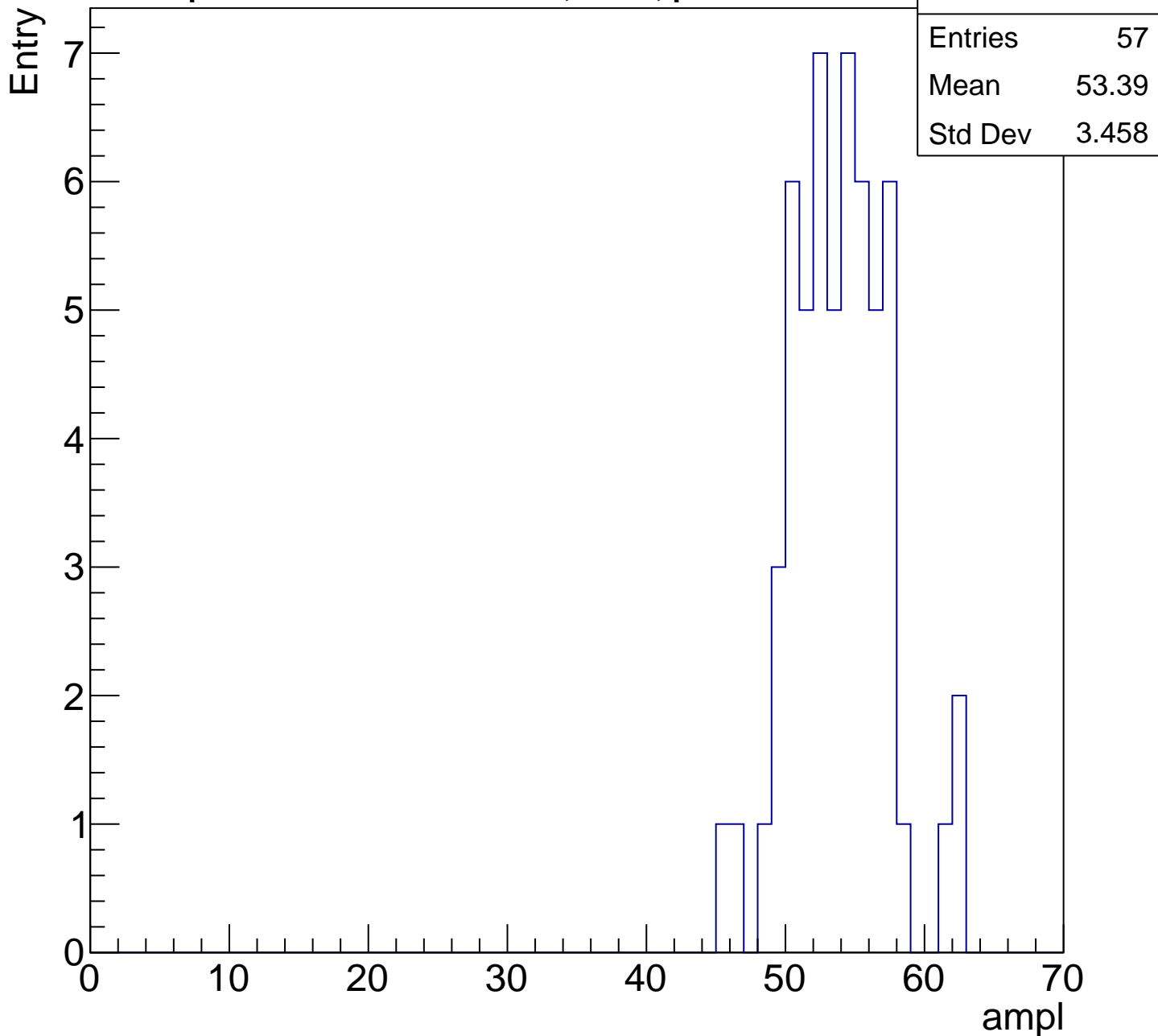
Entry

Entries	48
Mean	42.92
Std Dev	14.83



B1L103S, U5-ch47, adc4

calib_packv5_041523_1651.root, FC#0, port C2

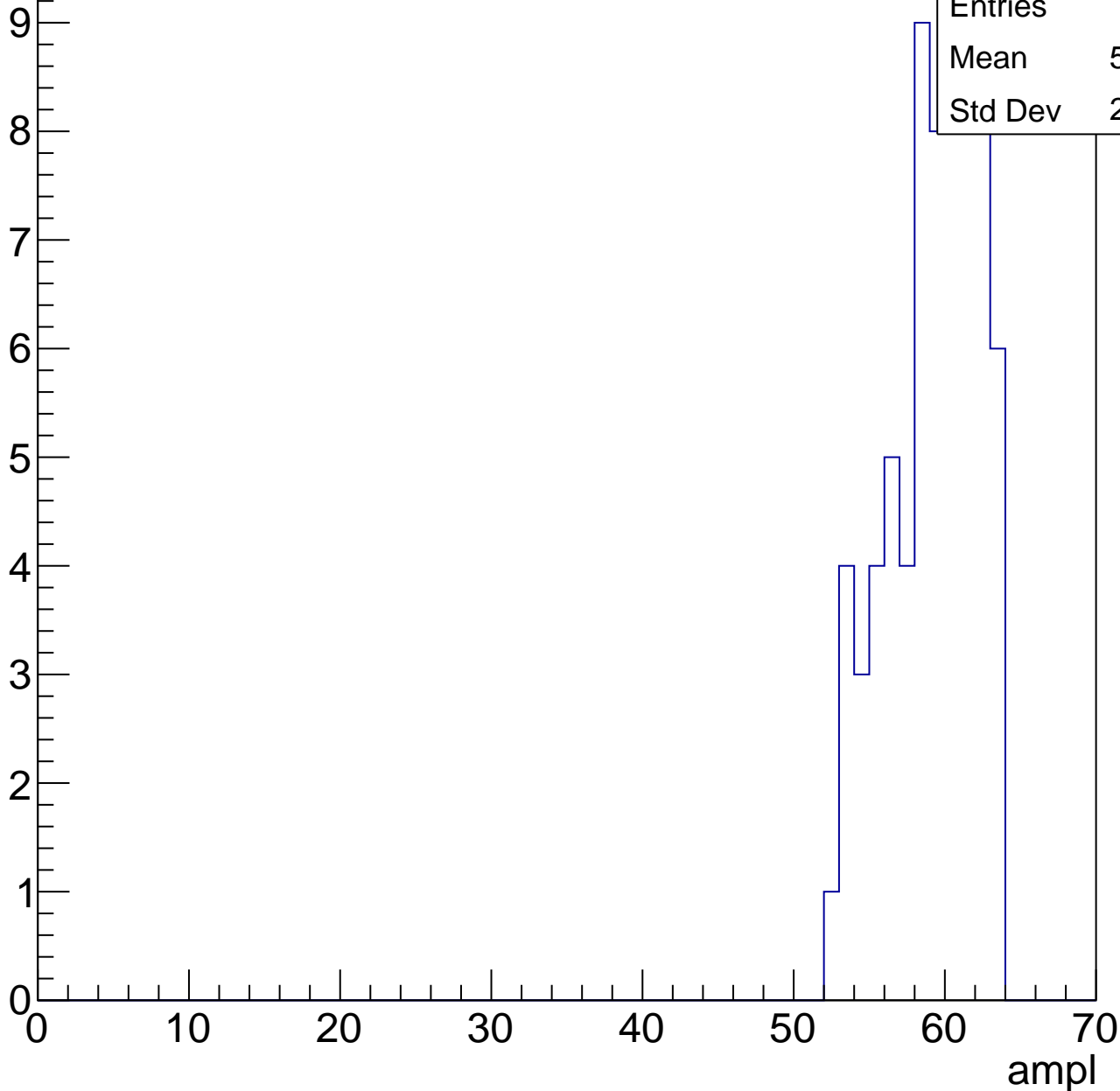


B1L103S, U5-ch47, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

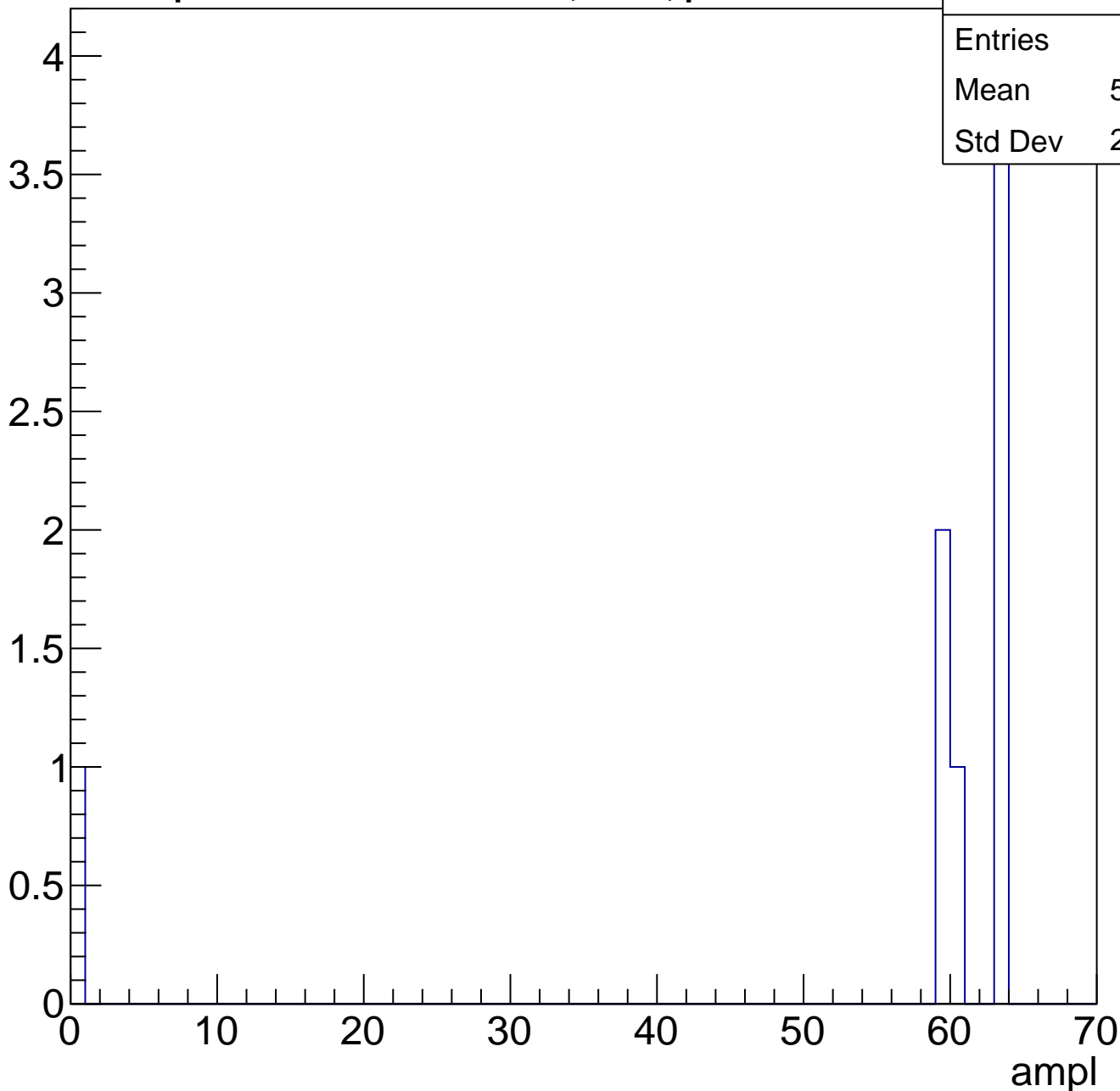
Entries	70
Mean	58.73
Std Dev	2.952



B1L103S, U5-ch47, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch47, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

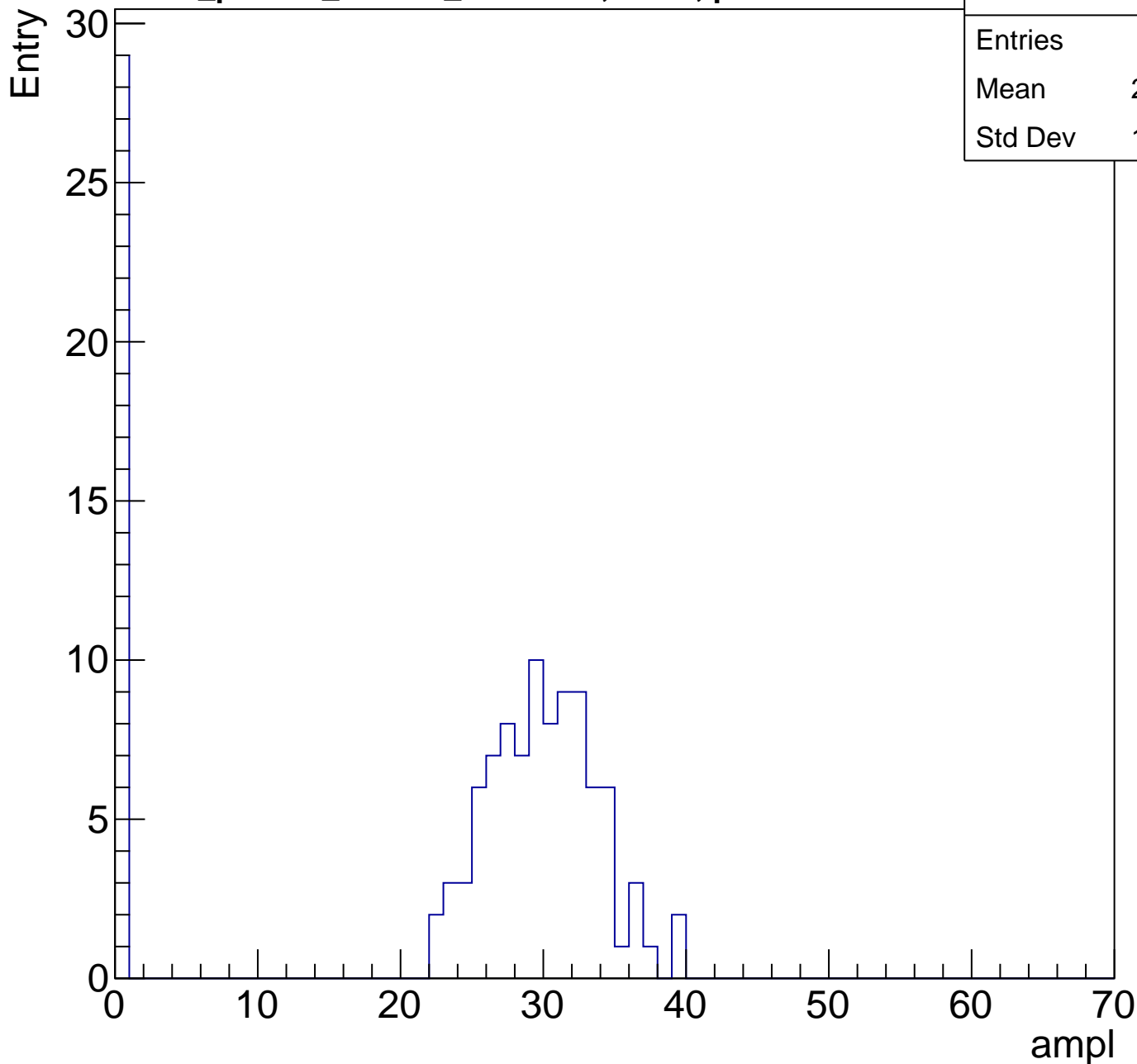
ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U5-ch48, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	120
Mean	22.38
Std Dev	13.05

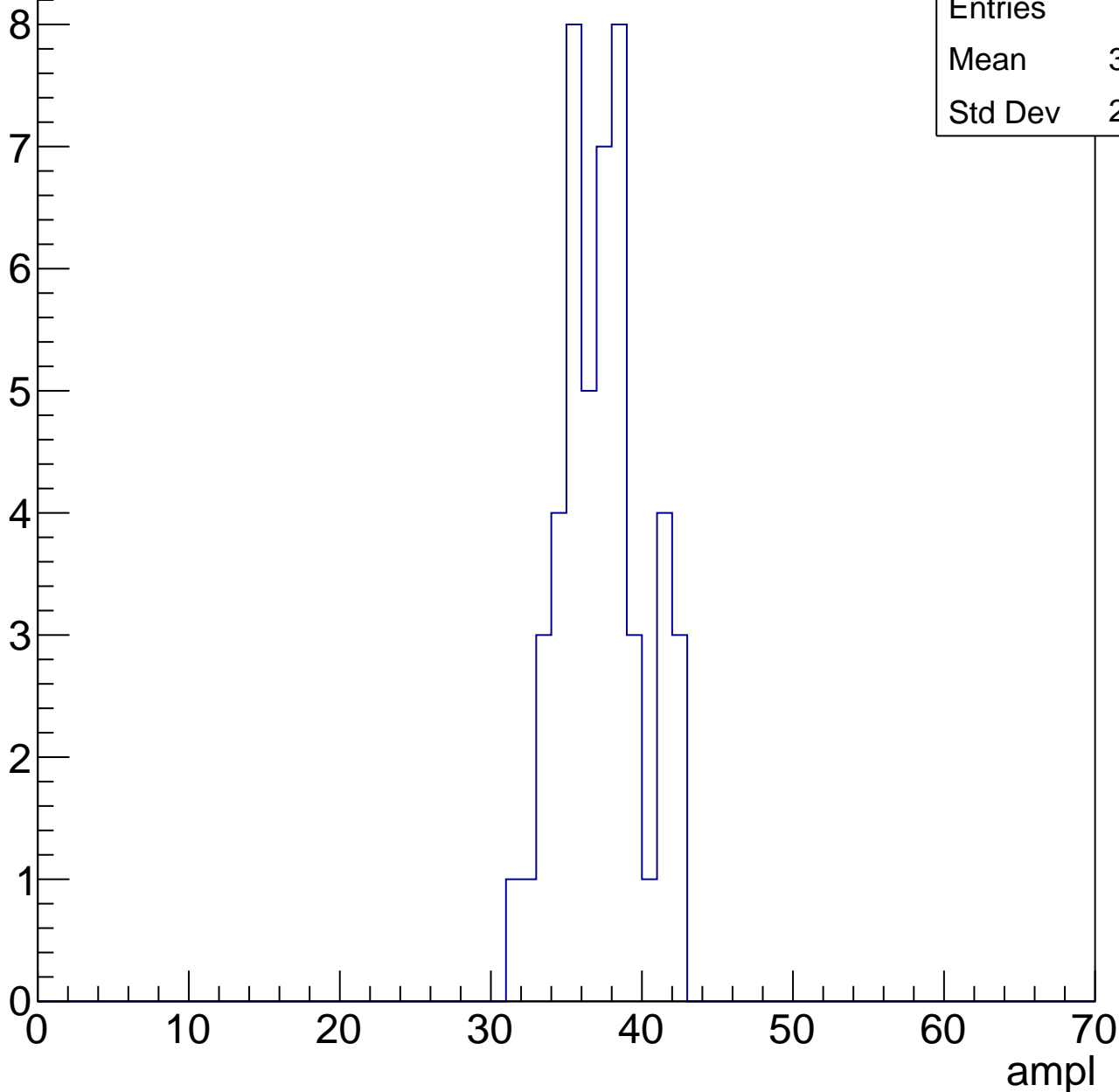


B1L103S, U5-ch48, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	48
Mean	36.83
Std Dev	2.695

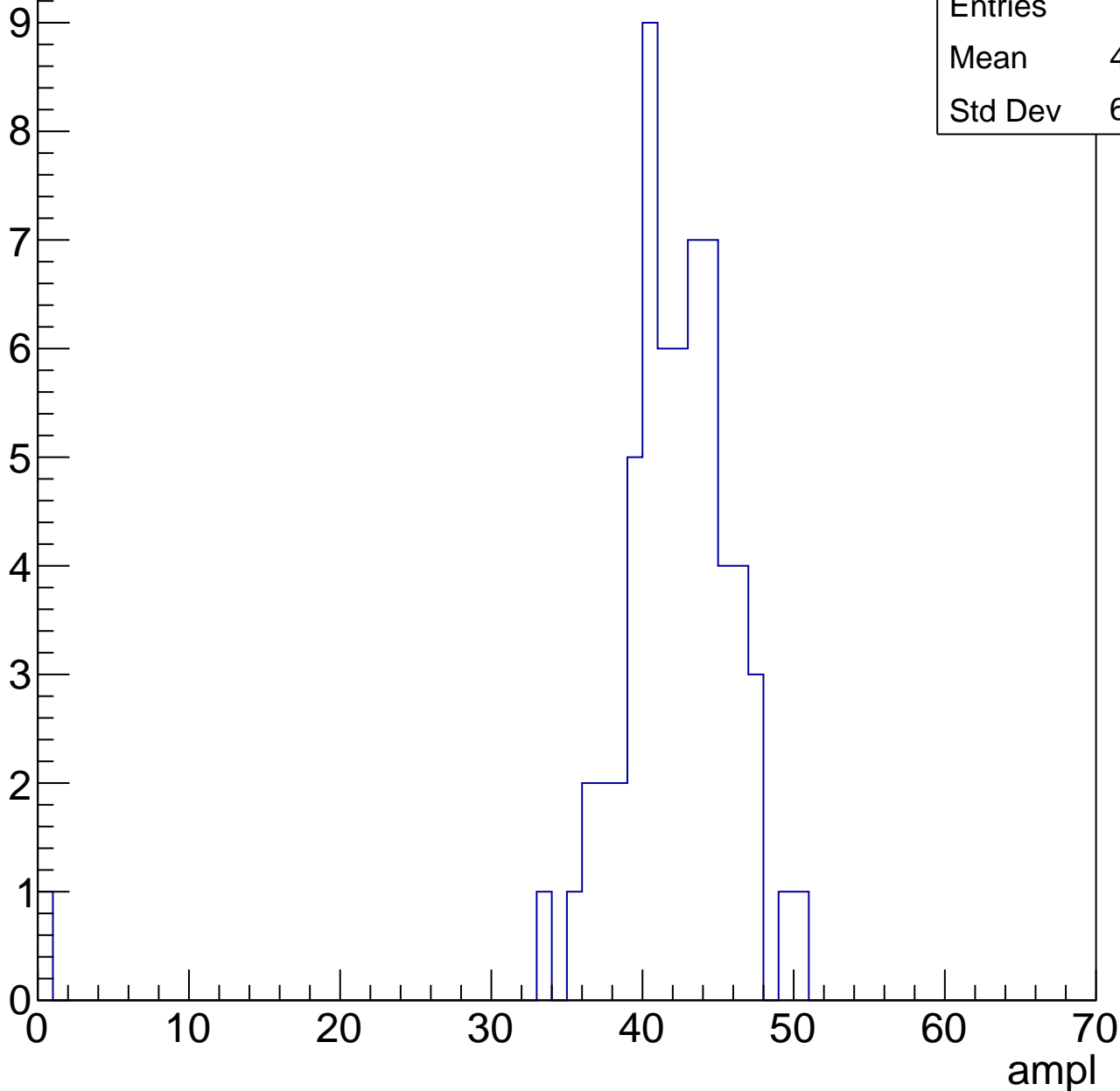


B1L103S, U5-ch48, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	41.23
Std Dev	6.249

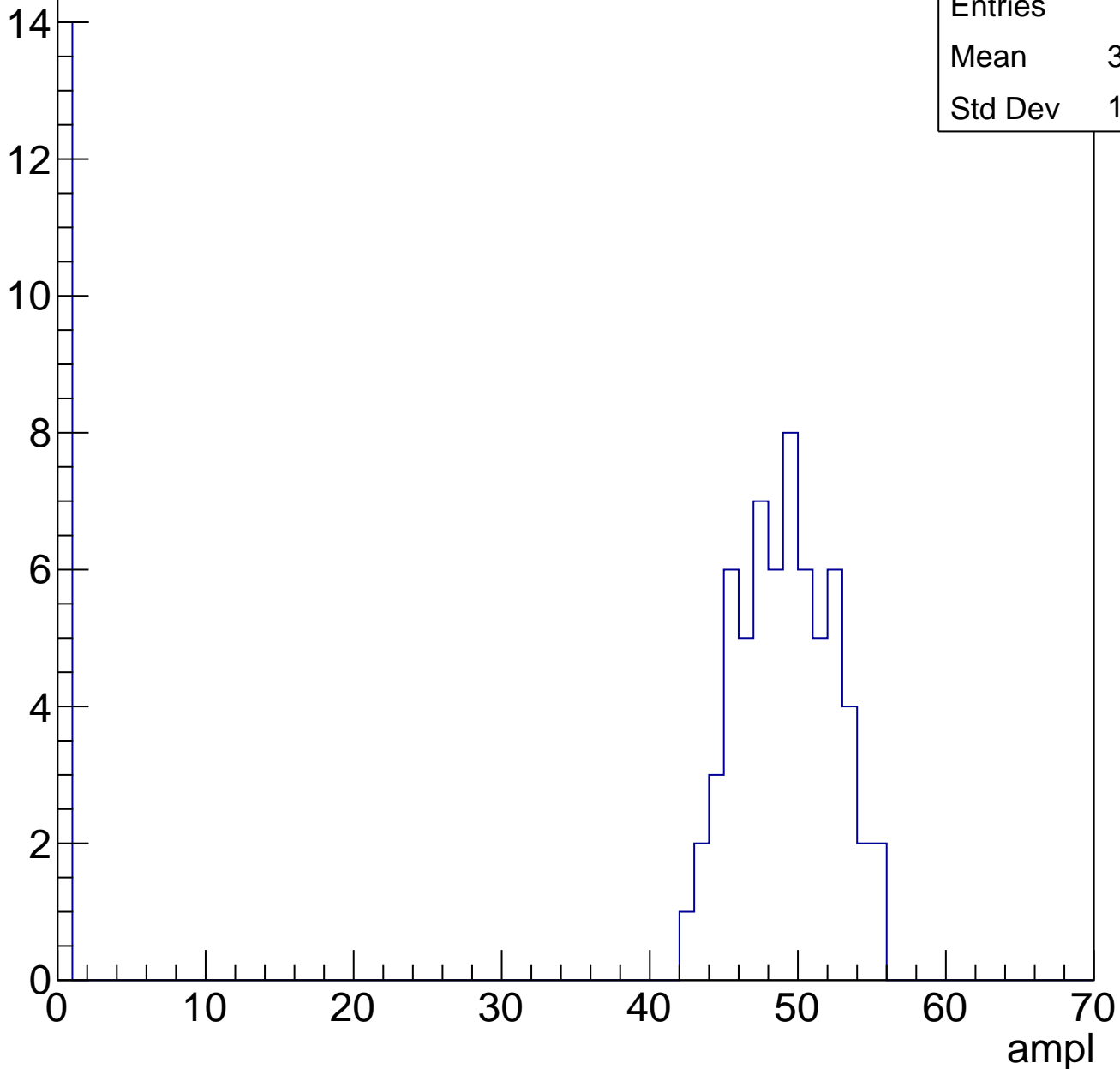


B1L103S, U5-ch48, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	77
Mean	39.82
Std Dev	18.99

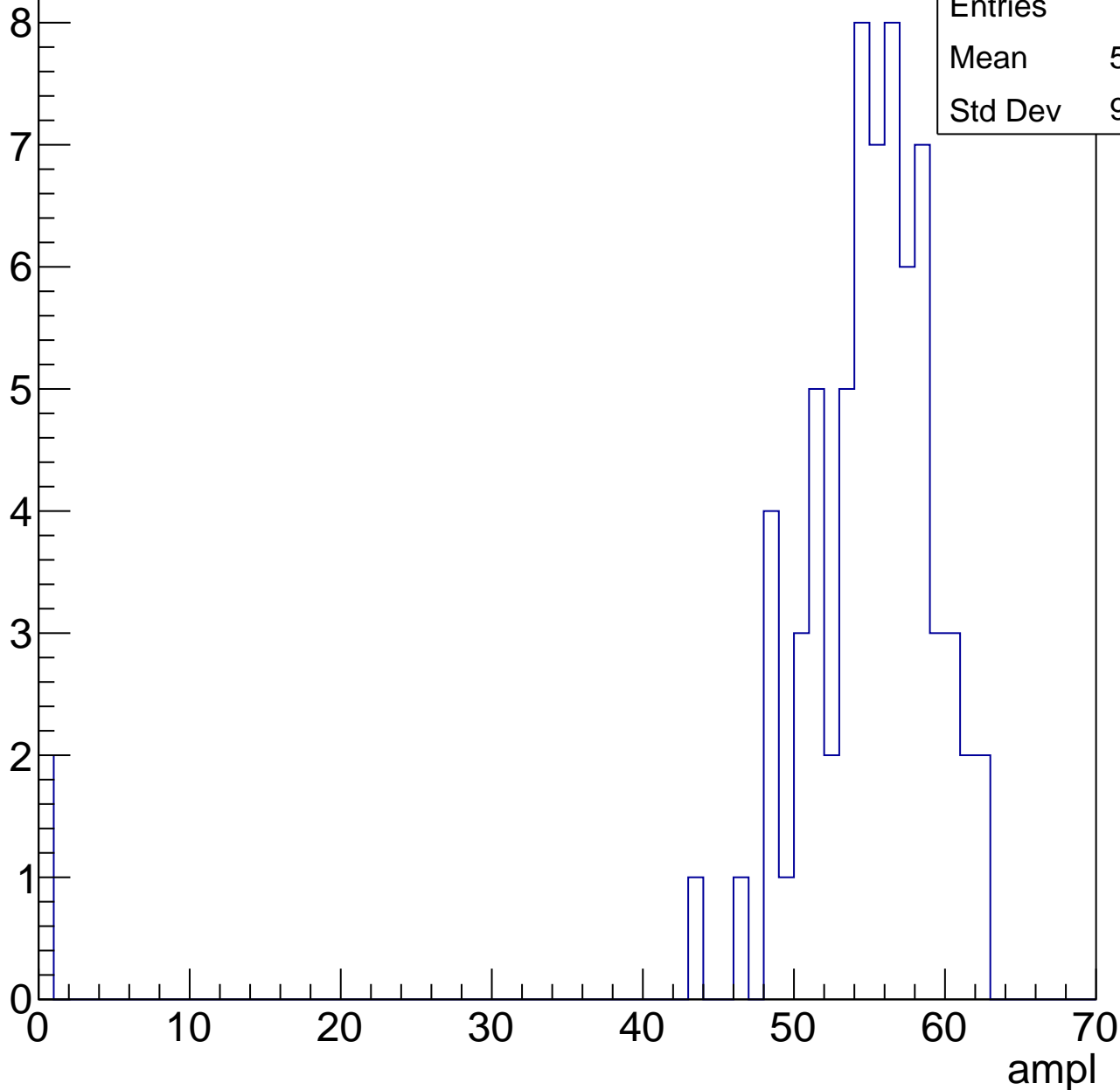
Entry



B1L103S, U5-ch48, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch48, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

7

6

5

4

3

2

1

0

0

10

20

30

40

50

60

70

ampl

Entries	43
Mean	58.02
Std Dev	9.38

0

1

2

3

4

5

6

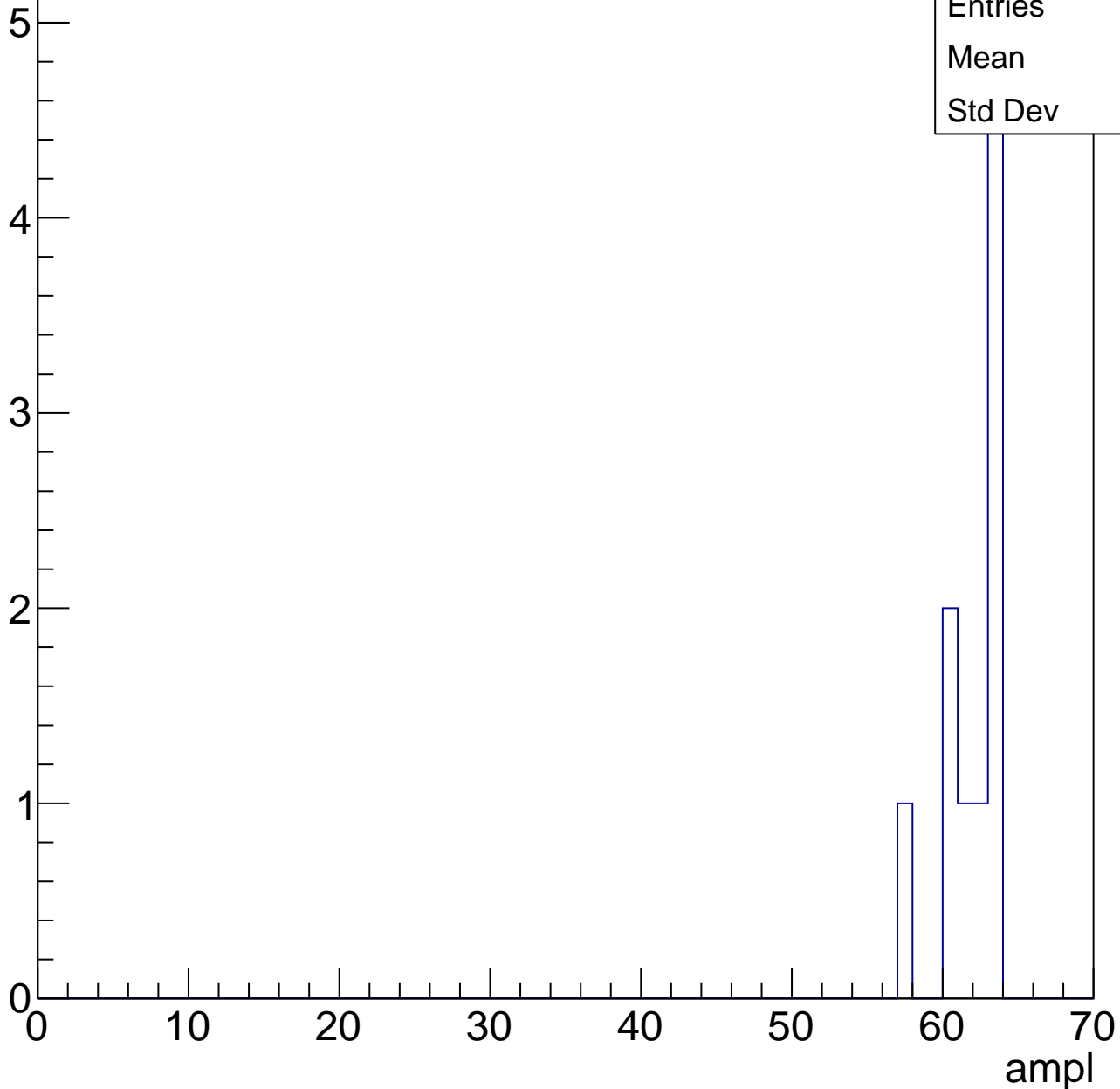
7

B1L103S, U5-ch48, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	10
Mean	61.5
Std Dev	1.91



B1L103S, U5-ch48, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry



B1L103S, U5-ch49, adc0

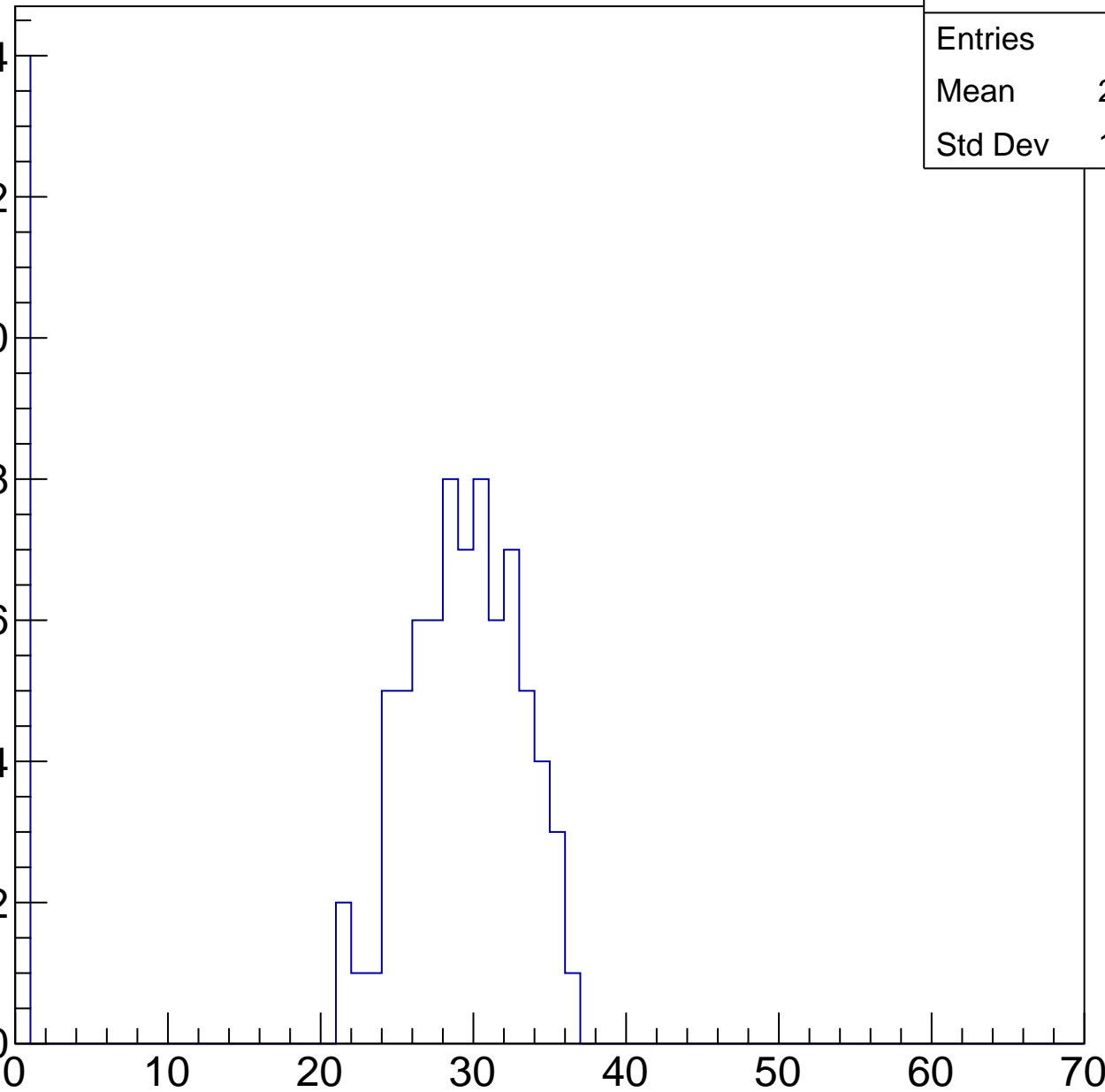
calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	24.37
Std Dev	11.02

Entry

14
12
10
8
6
4
2
0

ampl

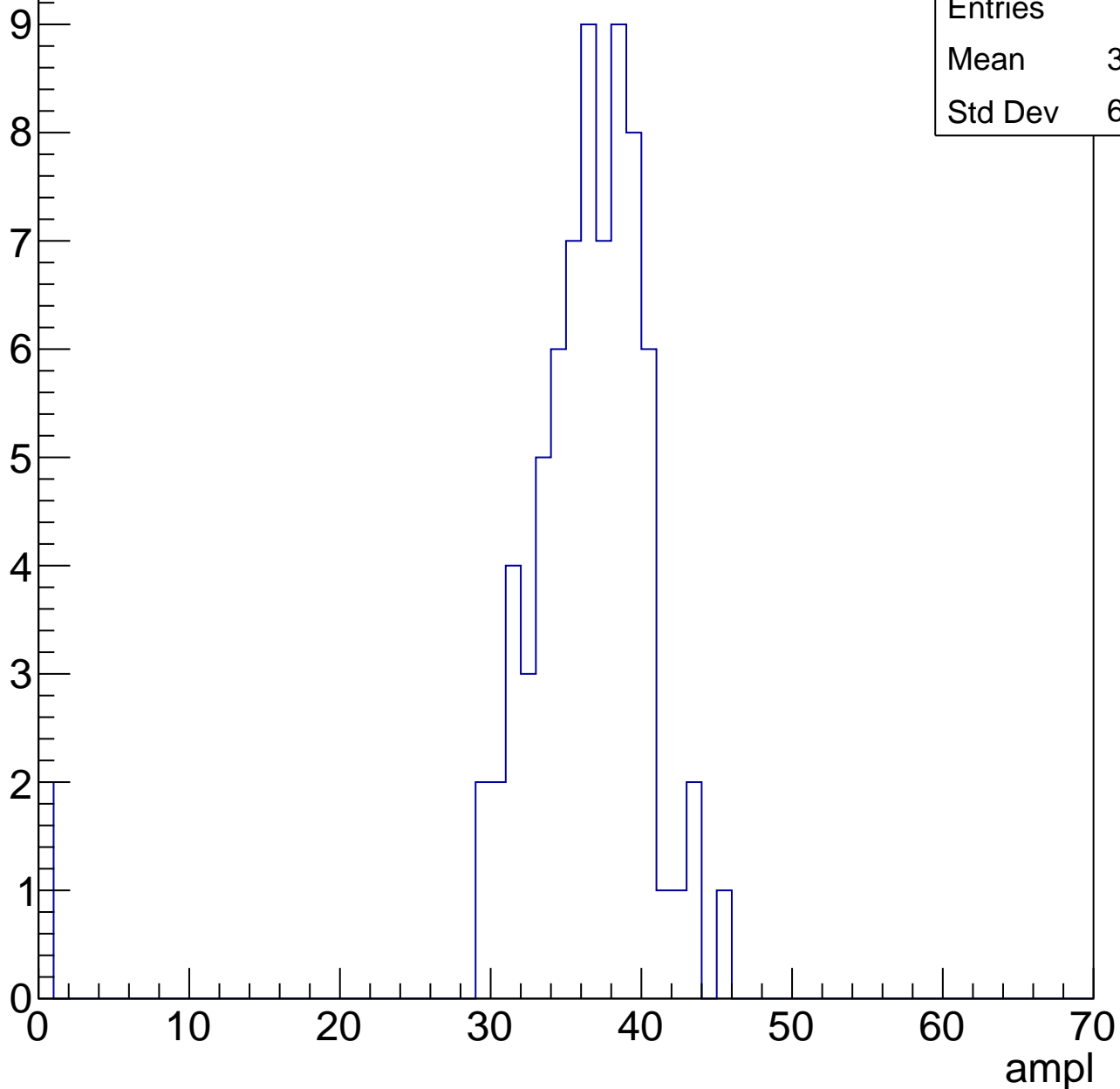


B1L103S, U5-ch49, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

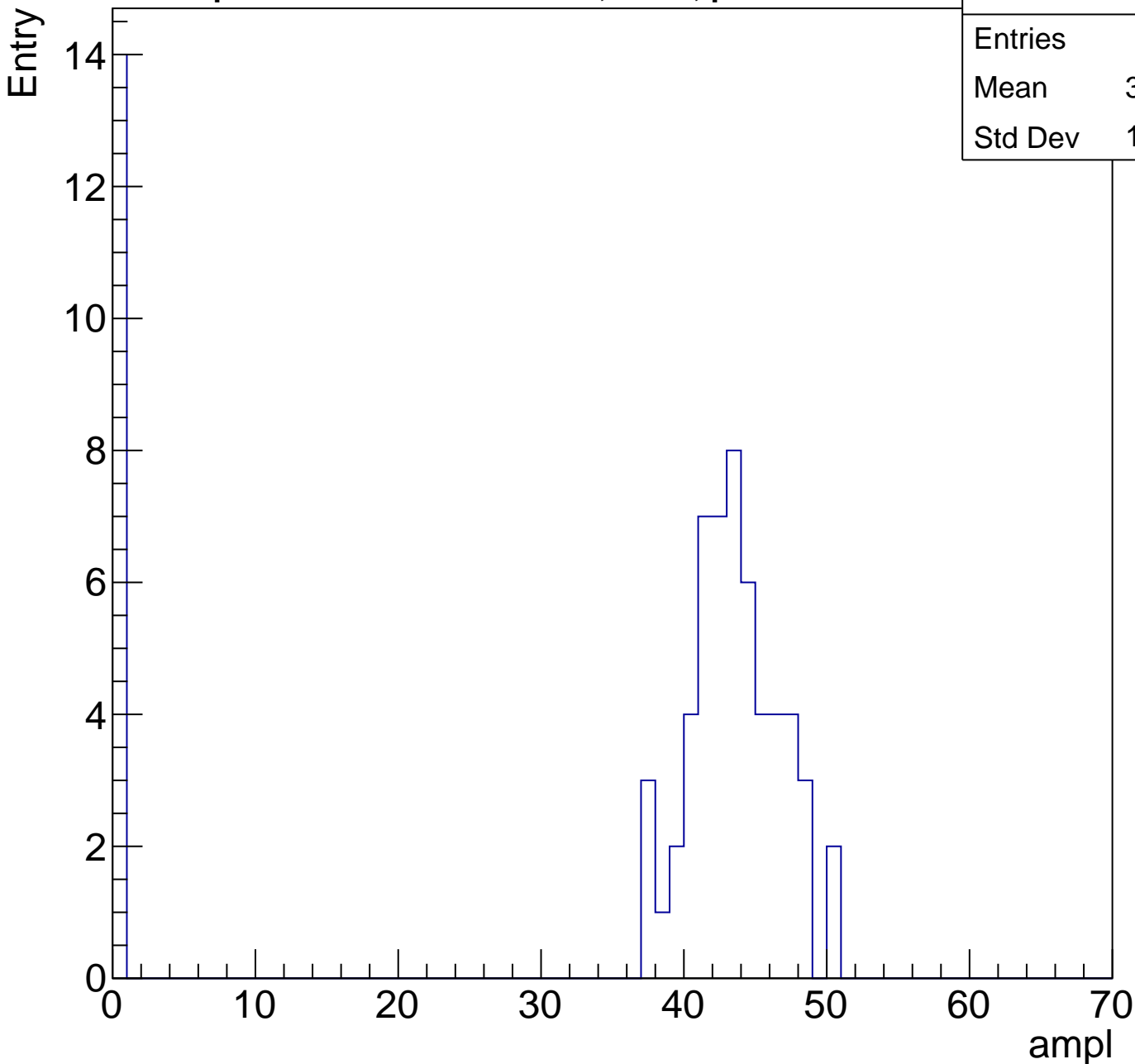
Entries	75
Mean	35.24
Std Dev	6.727



B1L103S, U5-ch49, adc2

calib_packv5_041523_1651.root, FC#0, port C2

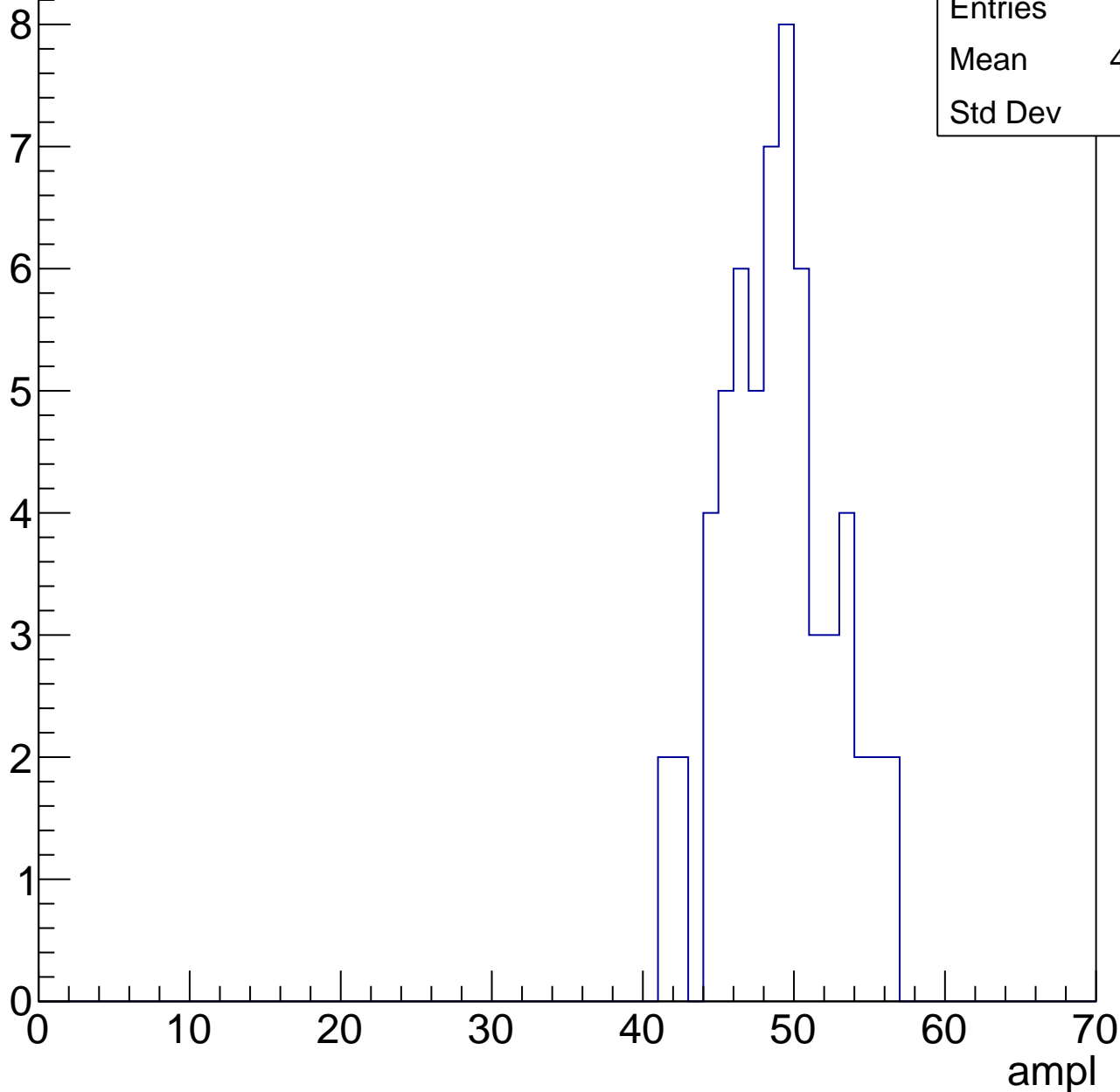
Entries	69
Mean	34.38
Std Dev	17.56



B1L103S, U5-ch49, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

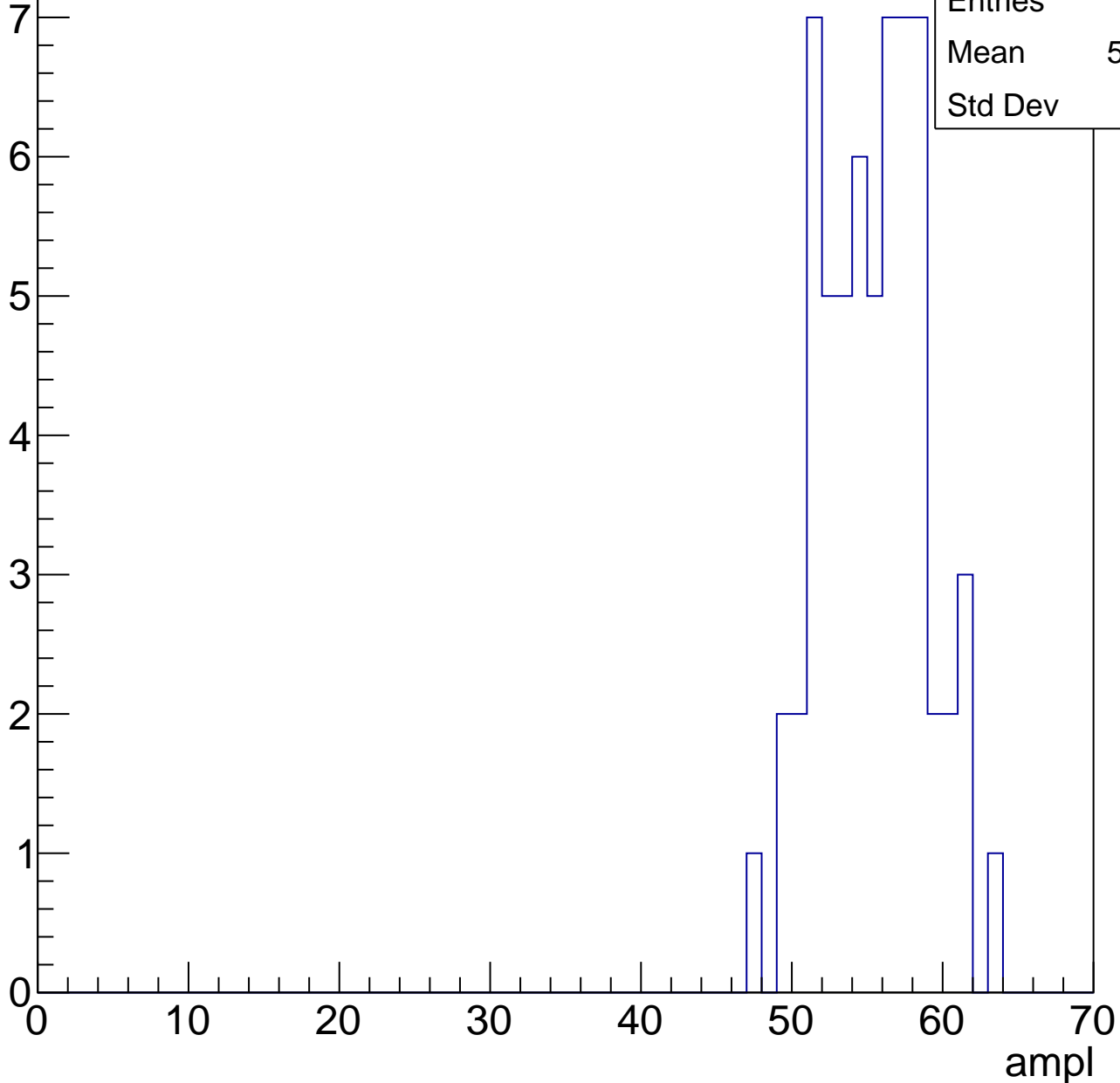


B1L103S, U5-ch49, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	54.95
Std Dev	3.41



B1L103S, U5-ch49, adc5

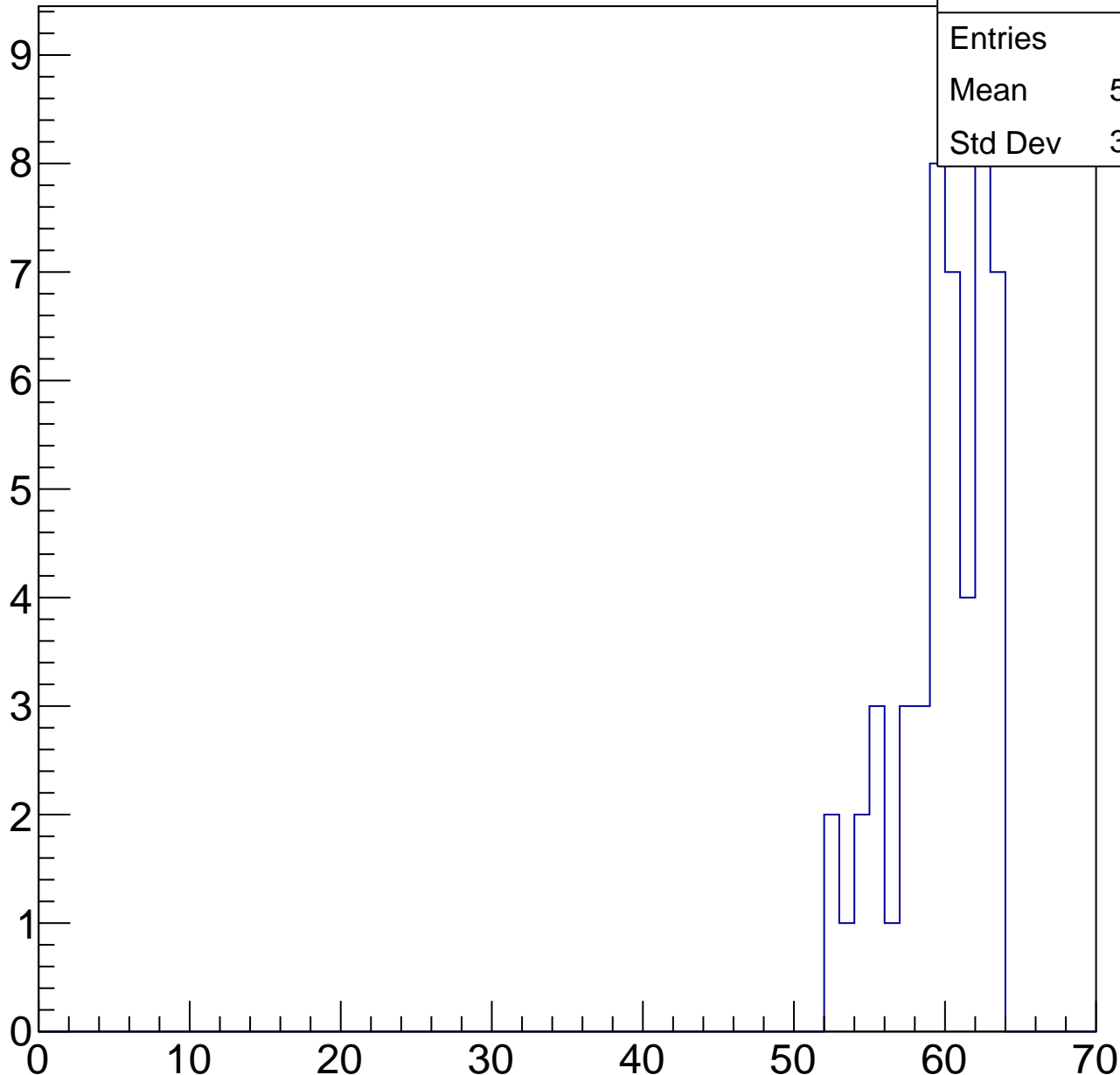
calib_packv5_041523_1651.root, FC#0, port C2

Entry

9
8
7
6
5
4
3
2
1
0

Entries	50
Mean	59.32
Std Dev	3.056

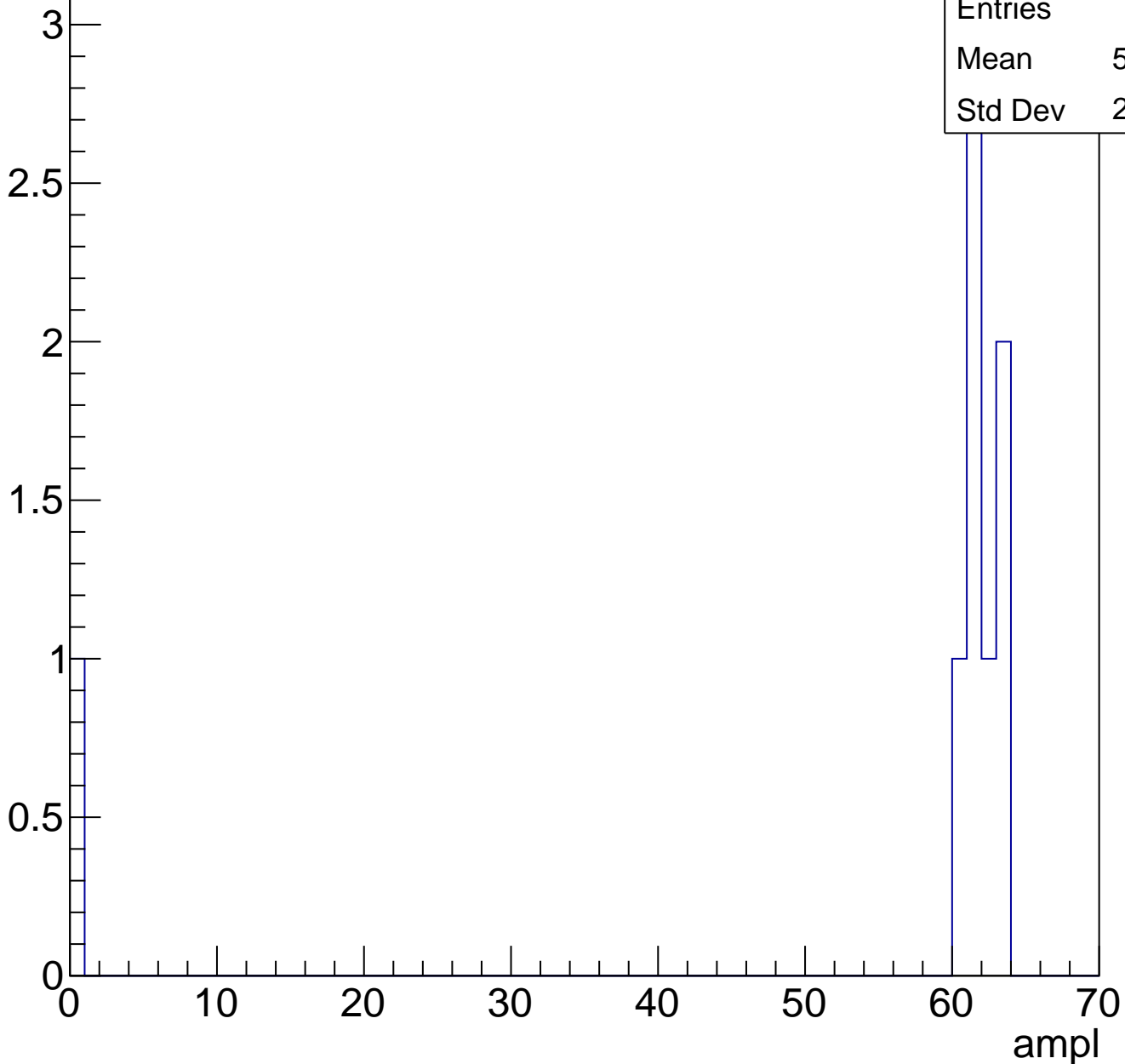
ampl



B1L103S, U5-ch49, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	8
Mean	53.88
Std Dev	20.39

B1L103S, U5-ch49, adc7

calib_packv5_041523_1651.root, FC#0, port C2

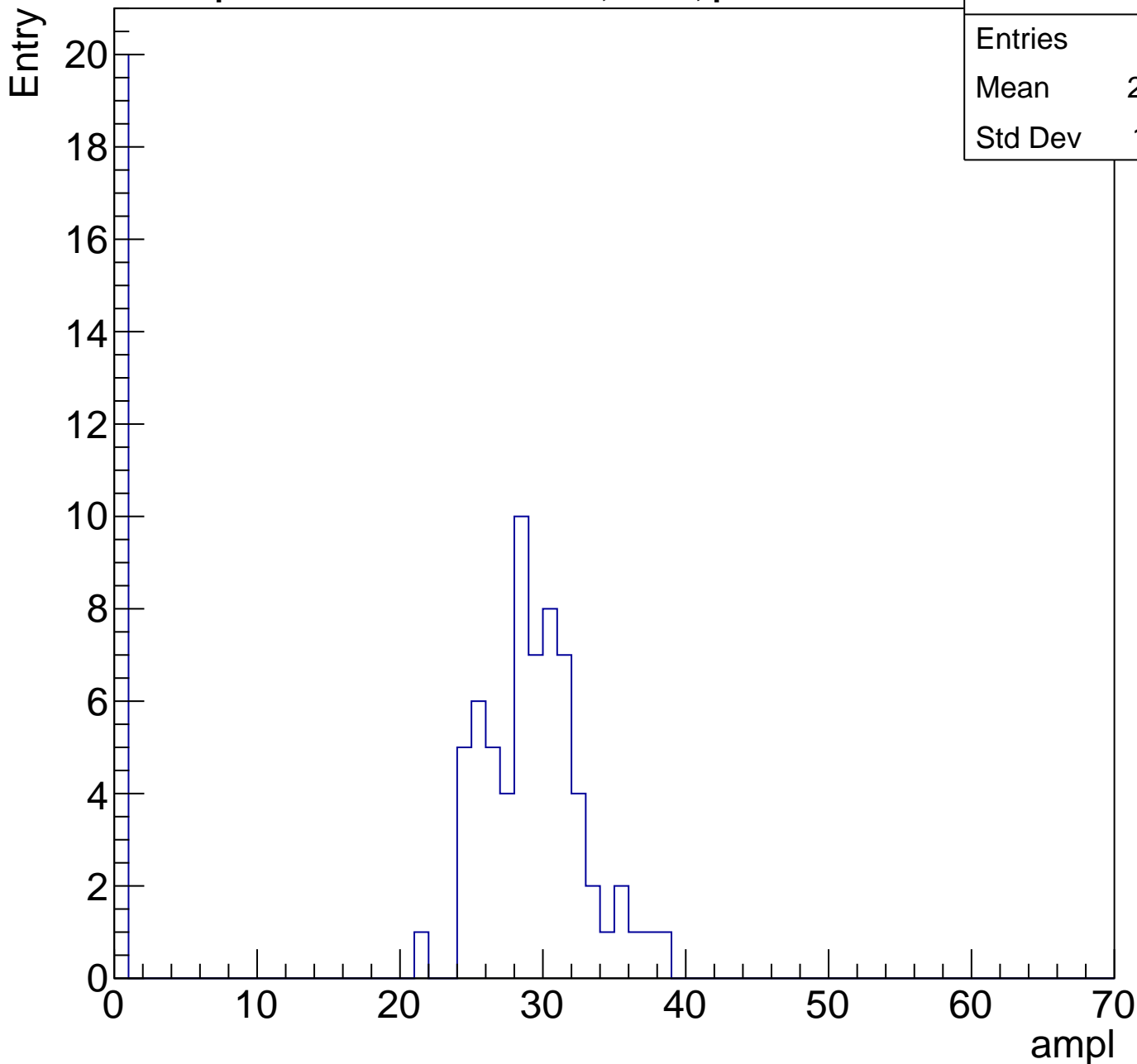
Entry



B1L103S, U5-ch50, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	85
Mean	22.09
Std Dev	12.61

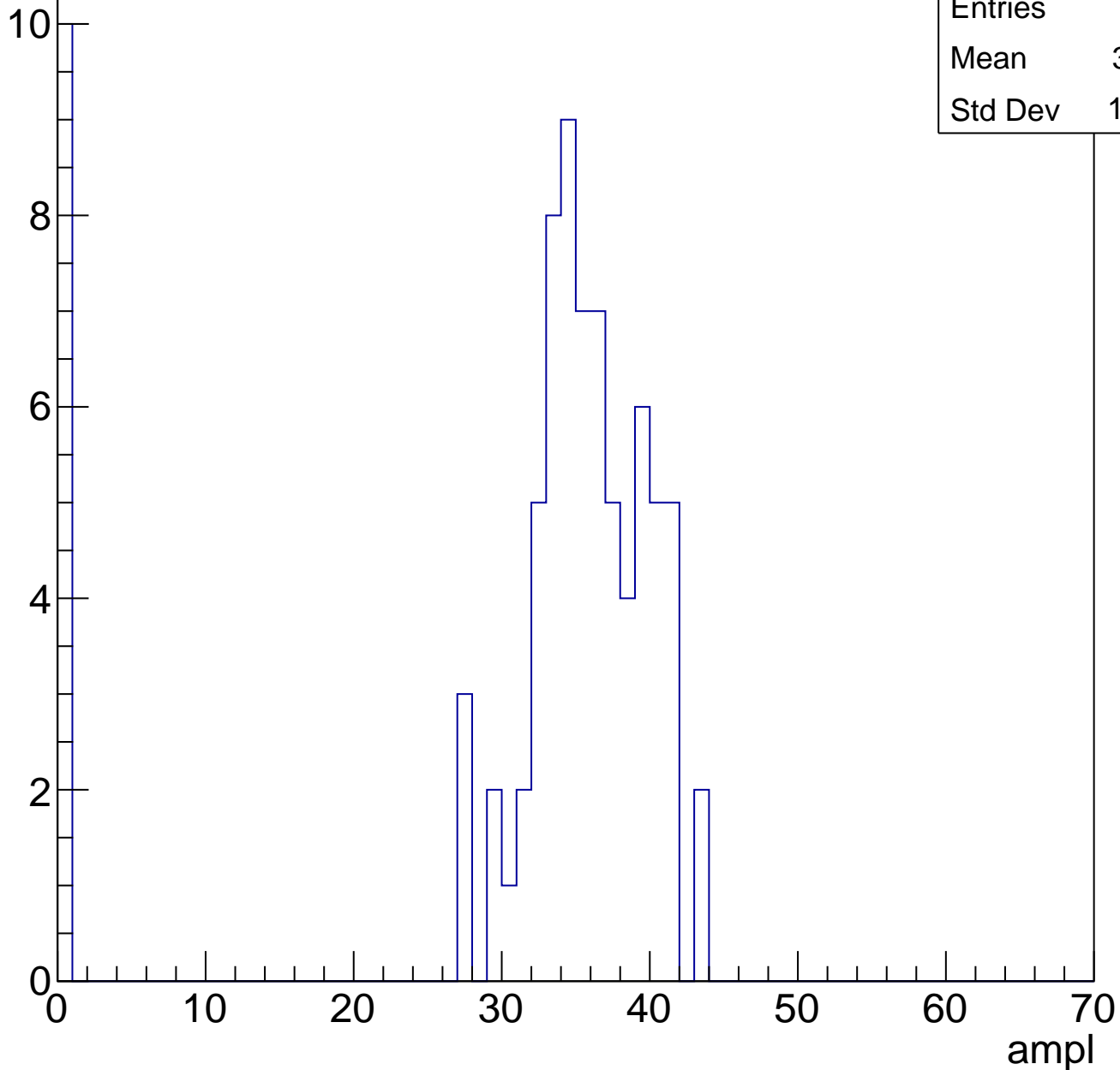


B1L103S, U5-ch50, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	31.11
Std Dev	12.18

Entry

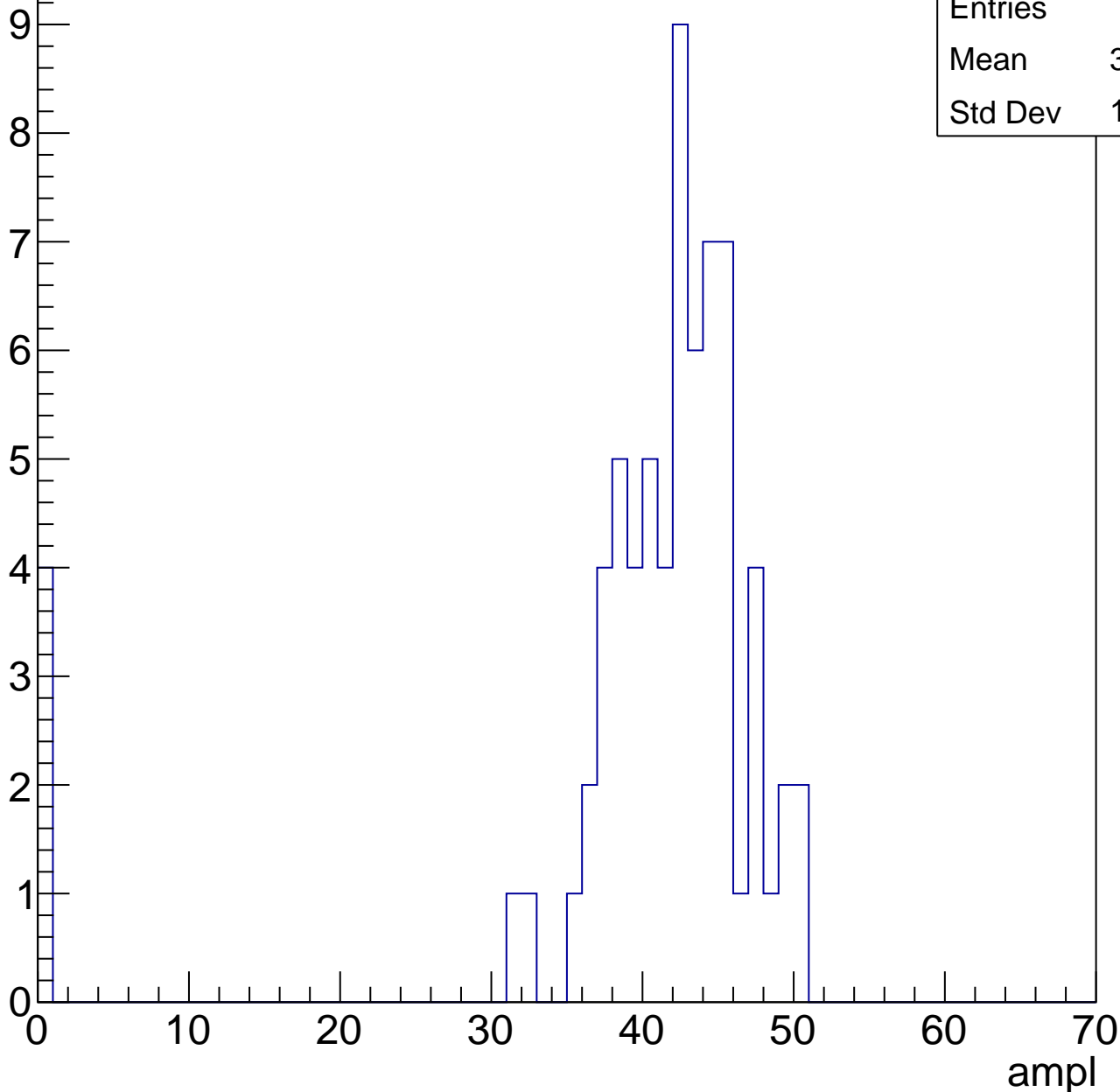


B1L103S, U5-ch50, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	39.53
Std Dev	10.48

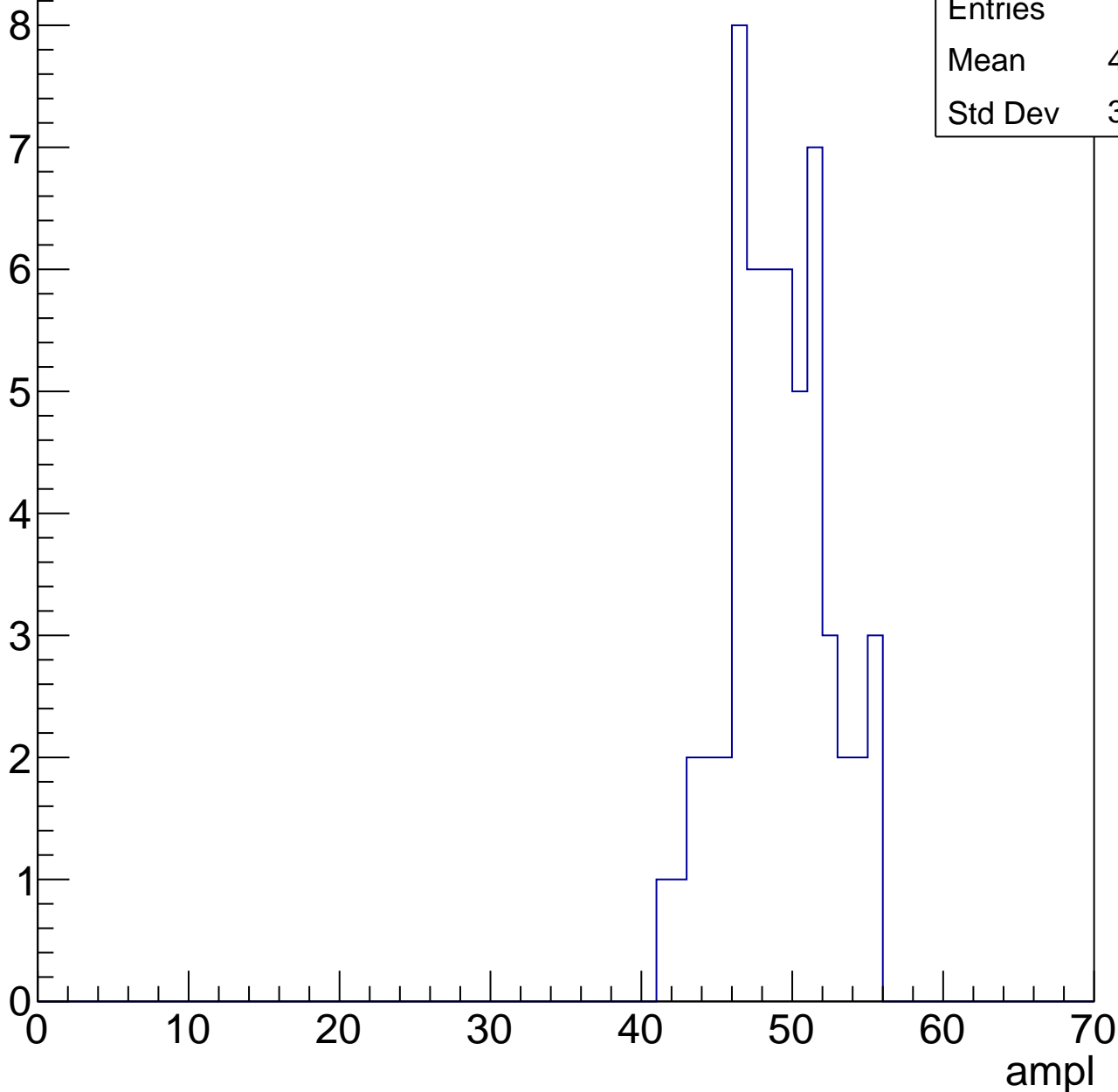


B1L103S, U5-ch50, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	48.59
Std Dev	3.299

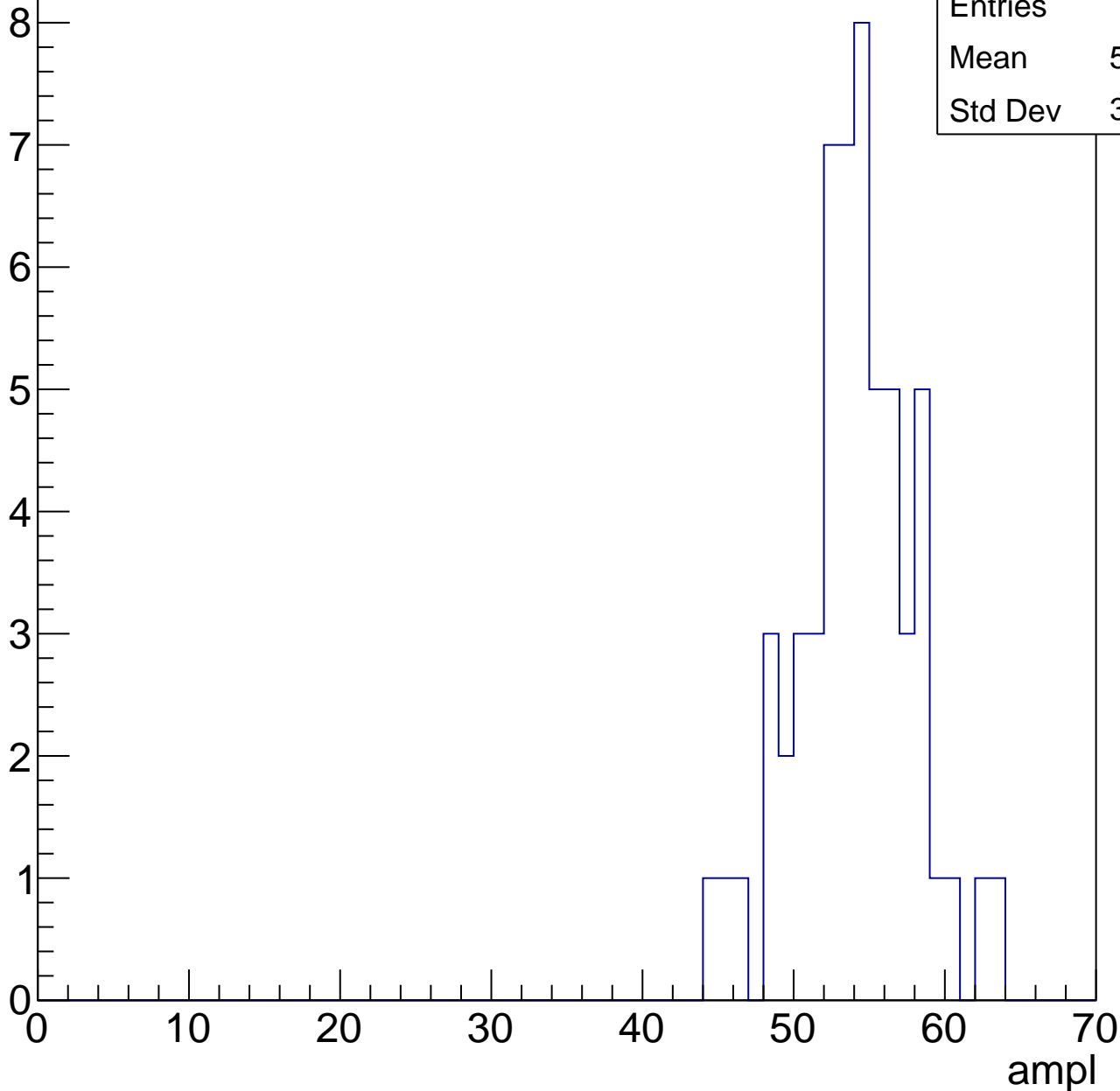


B1L103S, U5-ch50, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	53.57
Std Dev	3.806

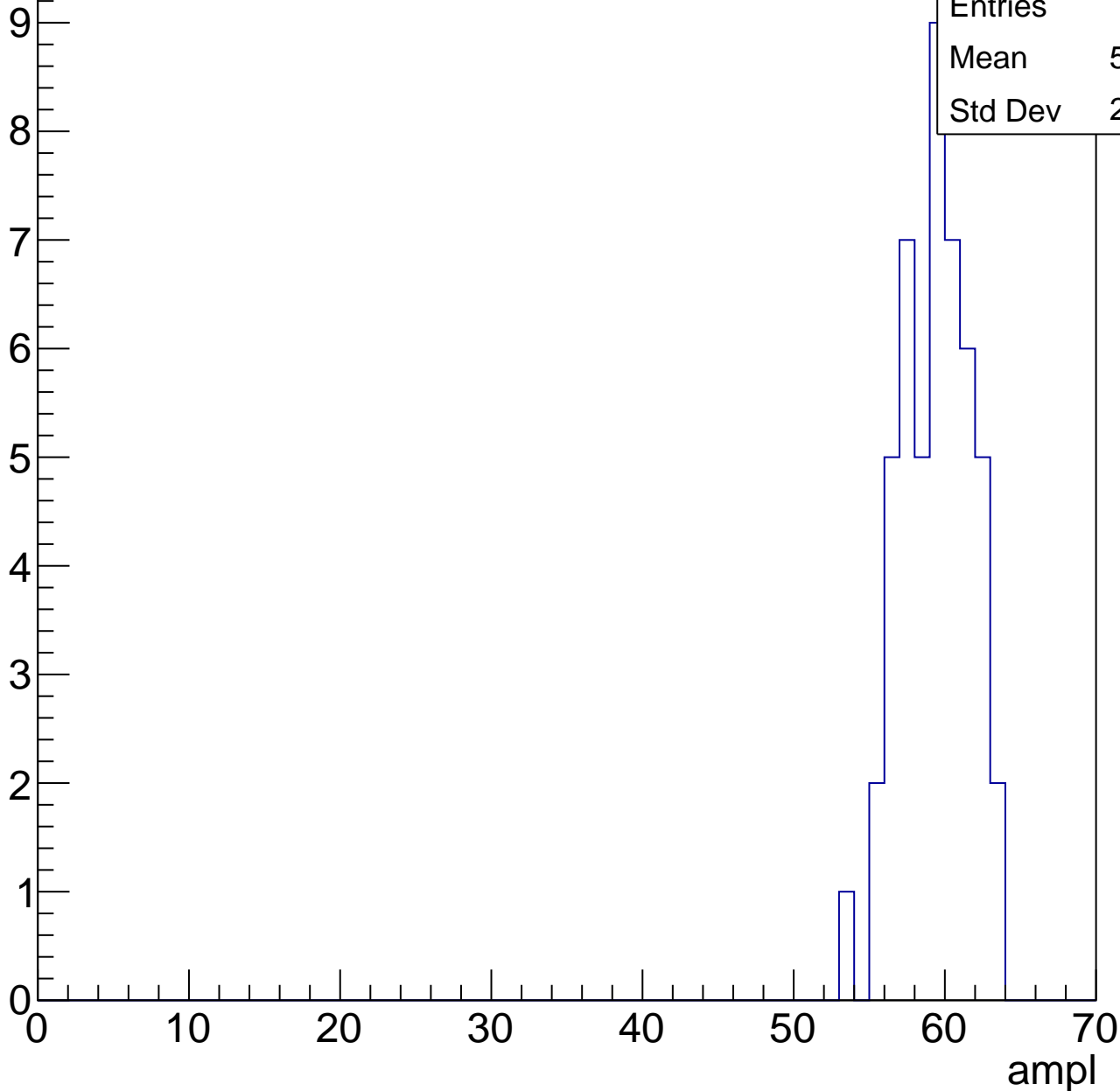


B1L103S, U5-ch50, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	58.88
Std Dev	2.273

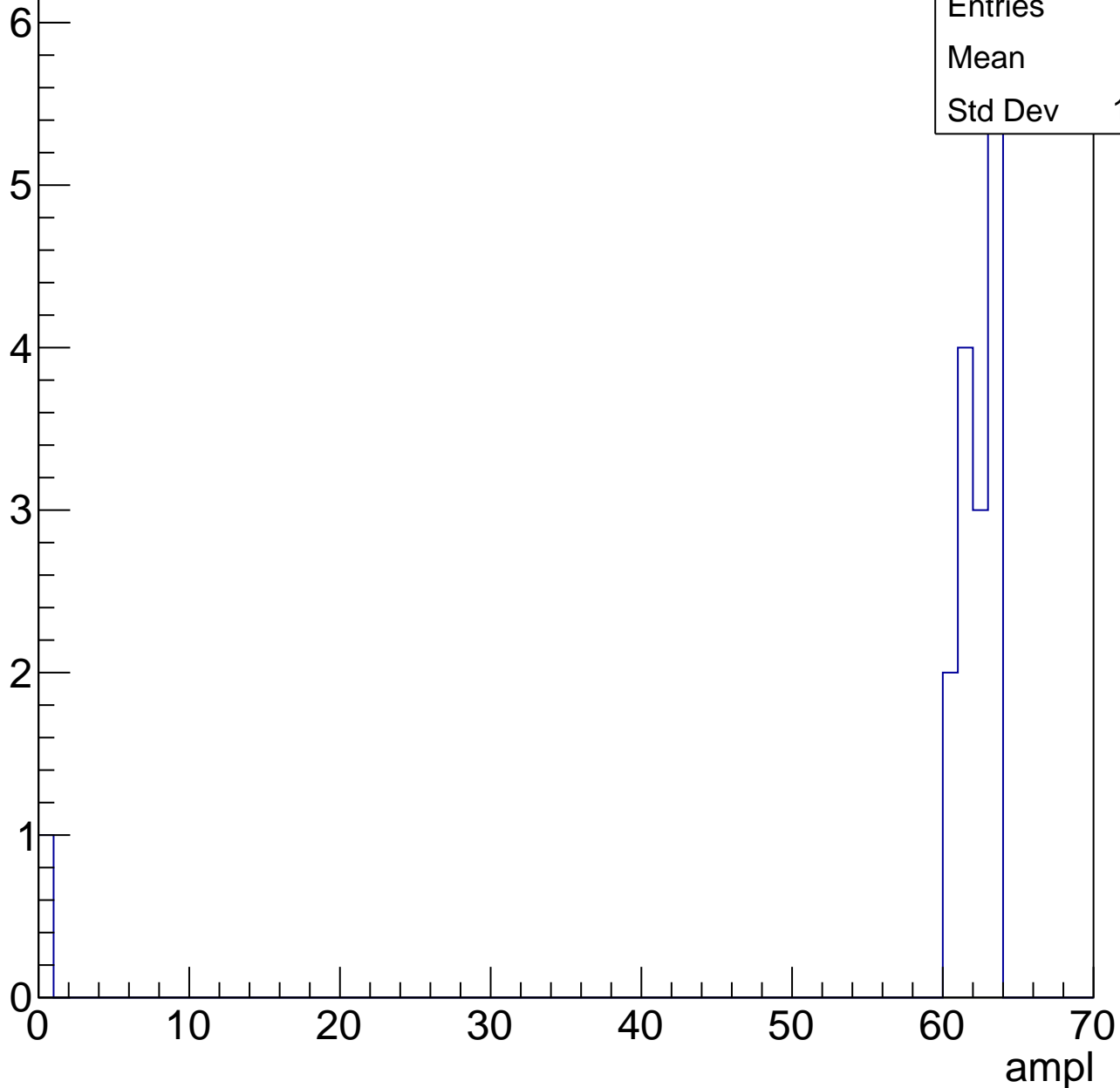


B1L103S, U5-ch50, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

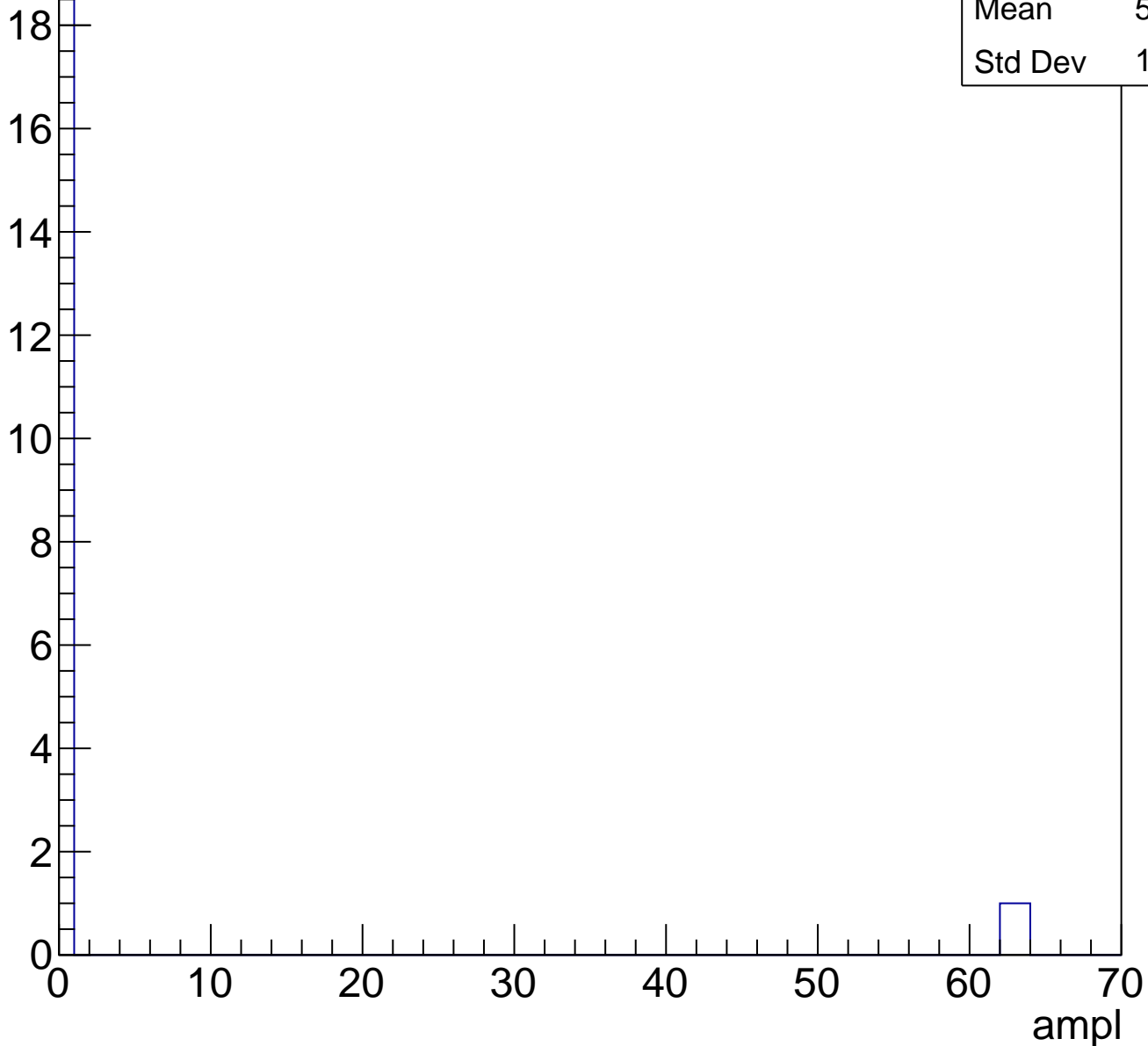
Entries	16
Mean	58
Std Dev	15.01



B1L103S, U5-ch50, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



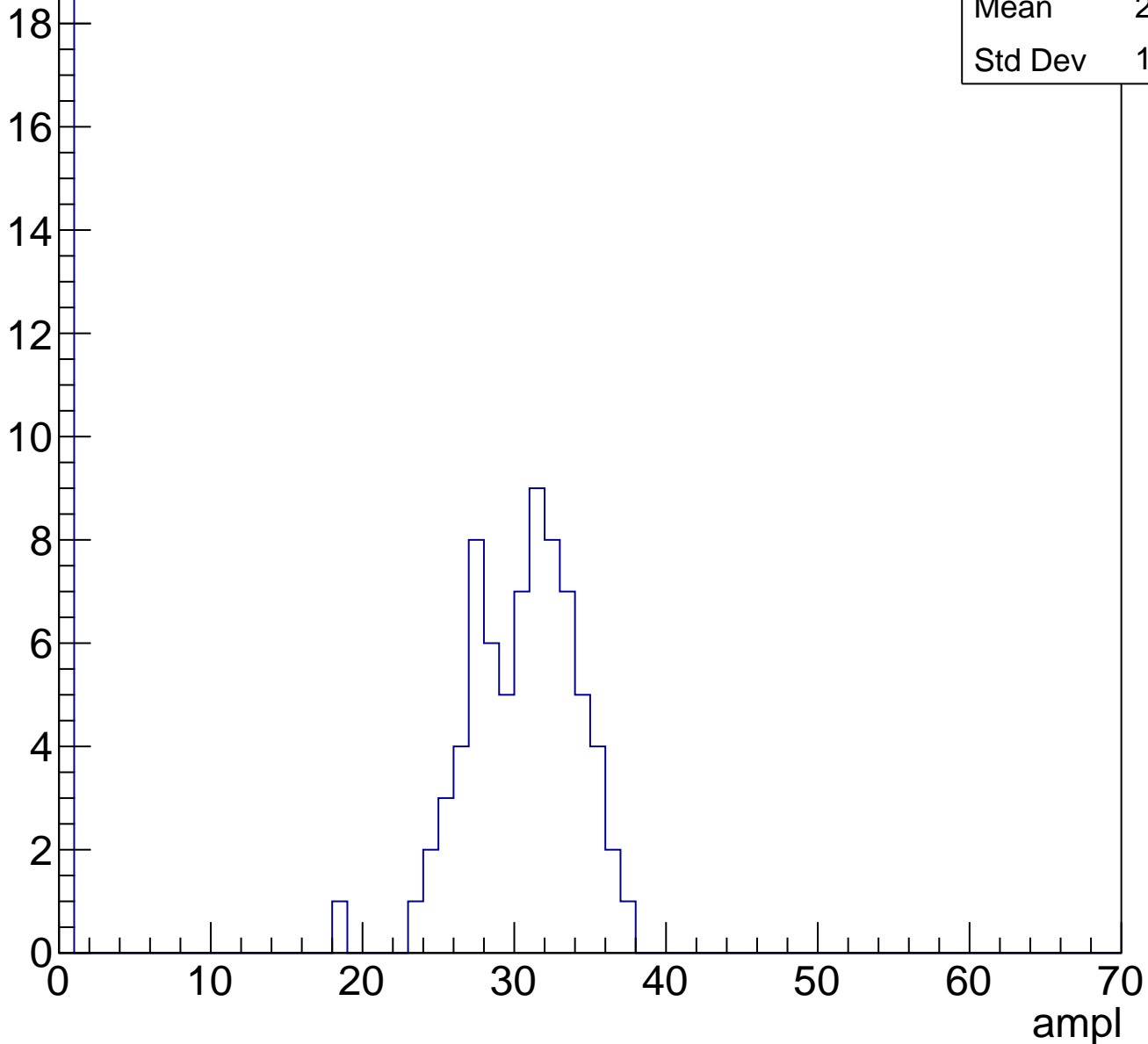
Entries	21
Mean	5.952
Std Dev	18.35

B1L103S, U5-ch51, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	92
Mean	23.83
Std Dev	12.56

Entry

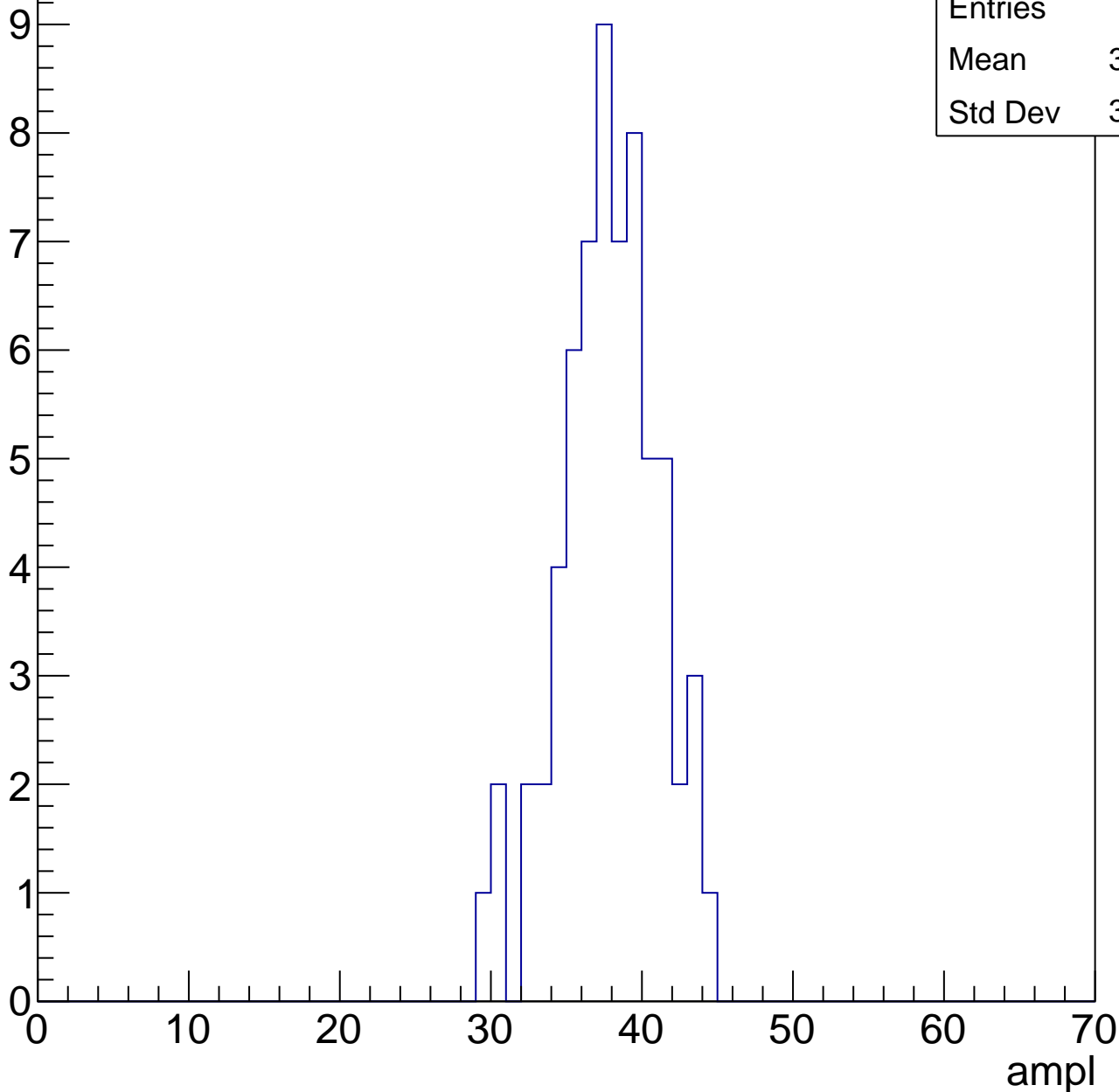


B1L103S, U5-ch51, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	37.34
Std Dev	3.246



B1L103S, U5-ch51, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	39.01
Std Dev	15.11

Entry

10

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ampl

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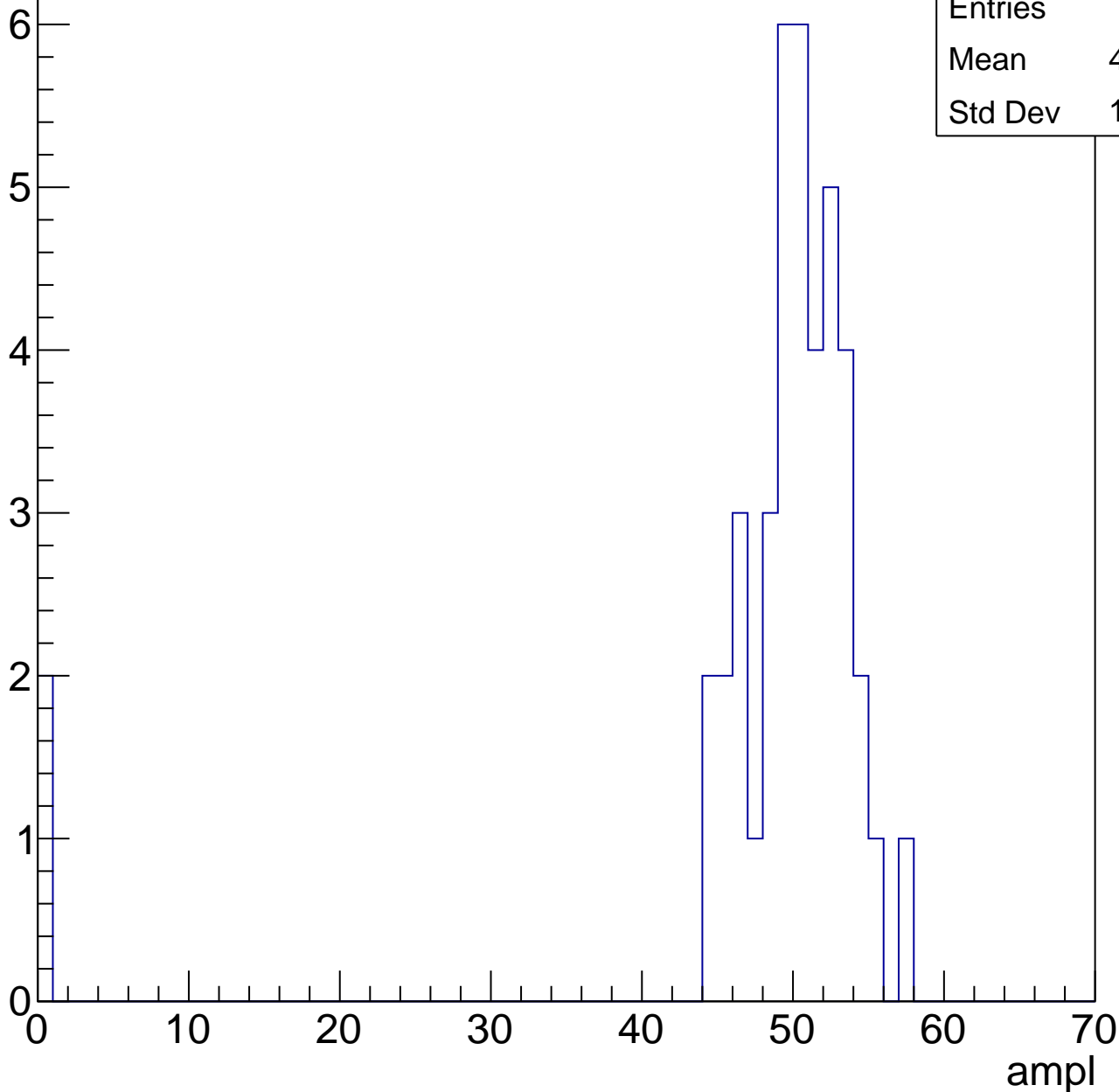
325

B1L103S, U5-ch51, adc3

calib_packv5_041523_1651.root, FC#0, port C2

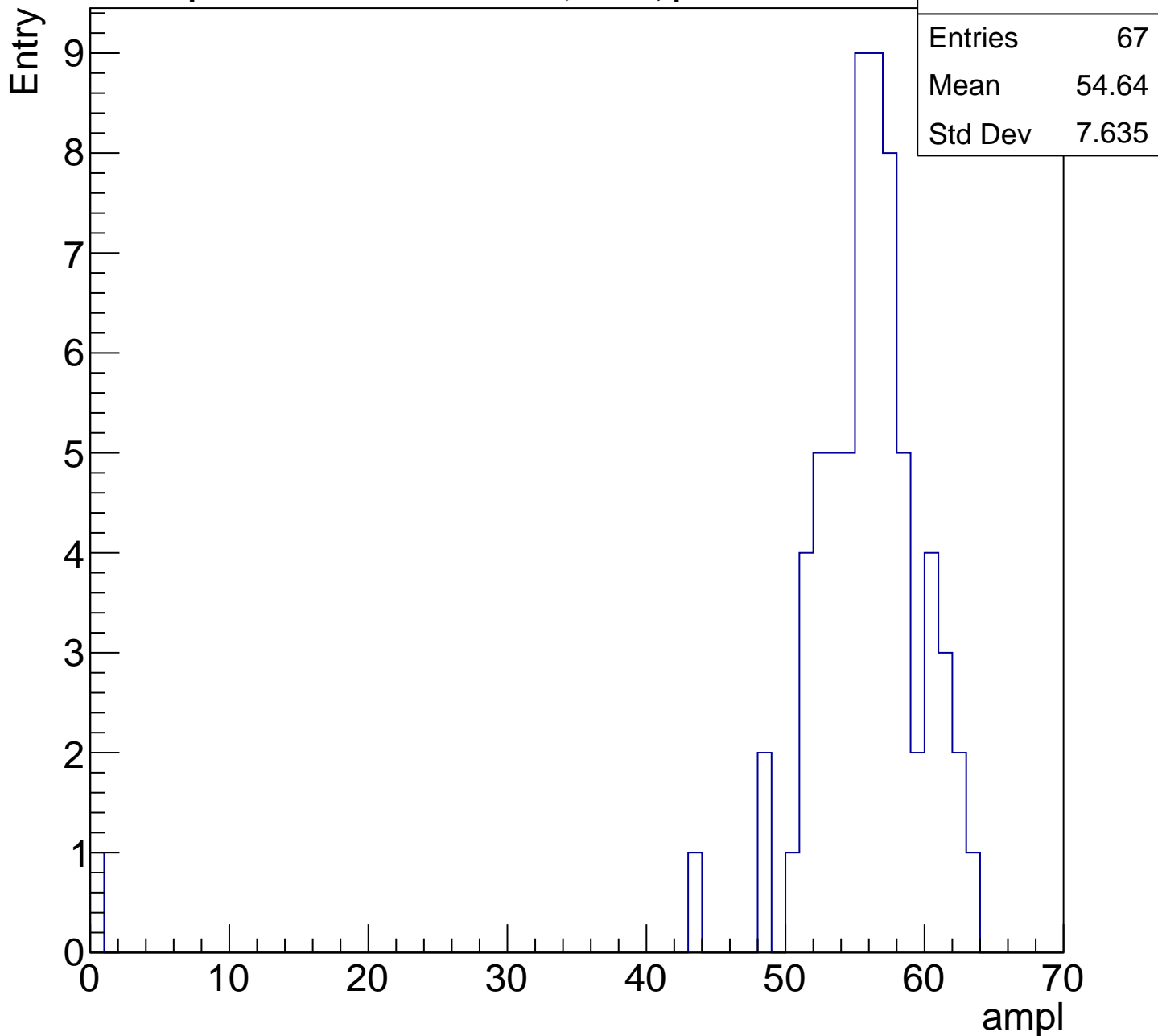
Entry

Entries	42
Mean	47.55
Std Dev	11.03



B1L103S, U5-ch51, adc4

calib_packv5_041523_1651.root, FC#0, port C2

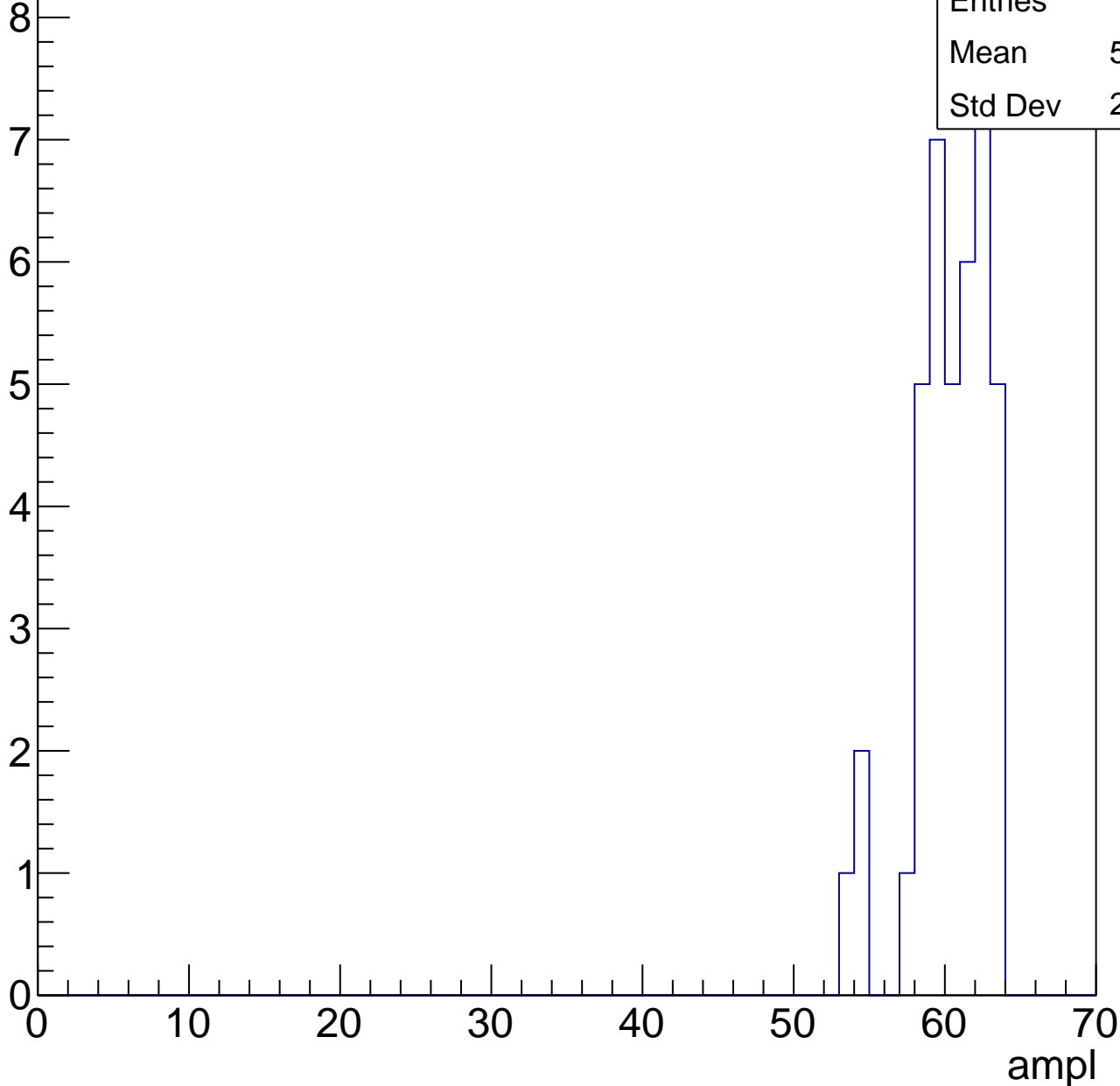


B1L103S, U5-ch51, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

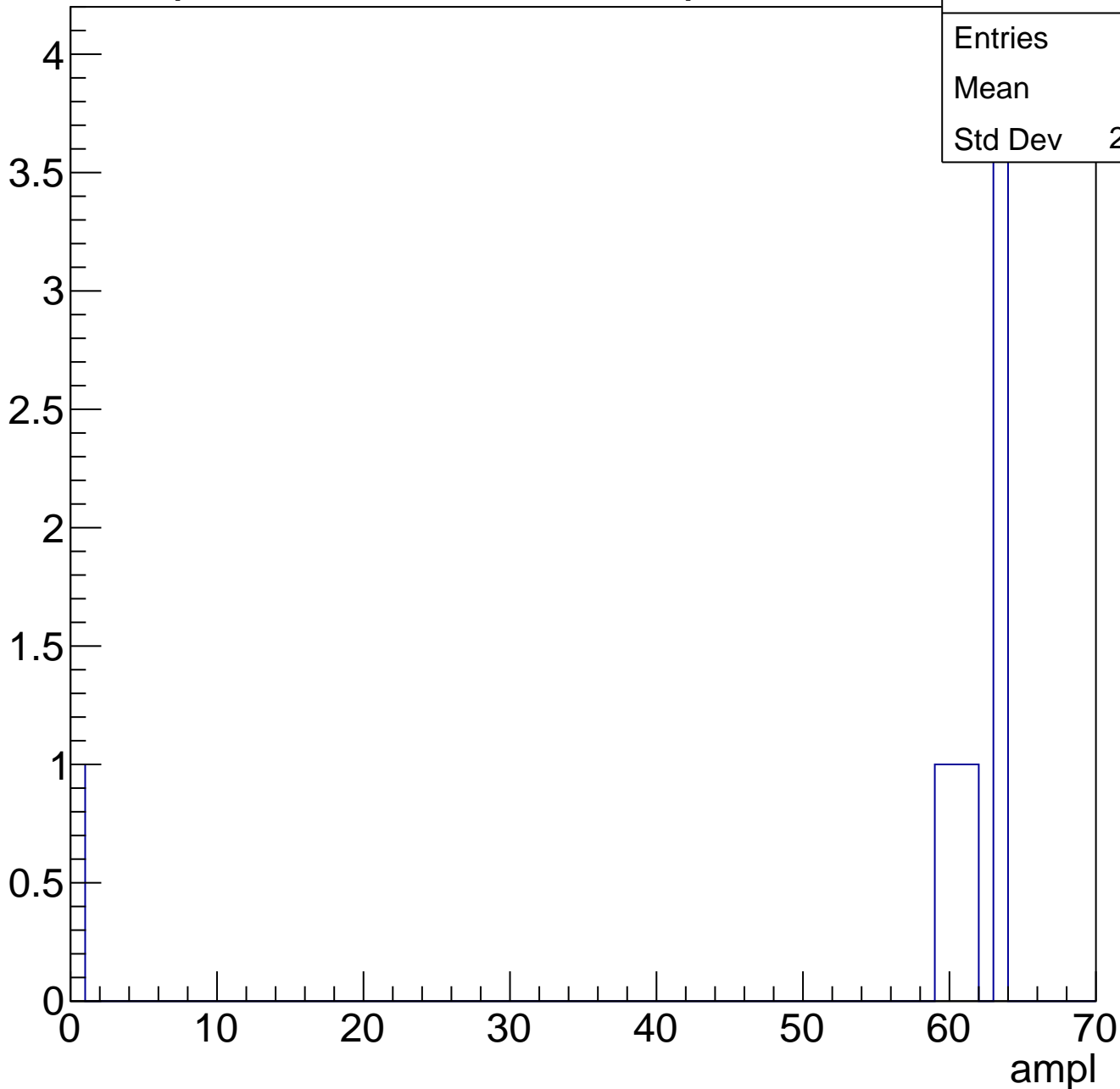
Entries	40
Mean	59.95
Std Dev	2.449



B1L103S, U5-ch51, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch51, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

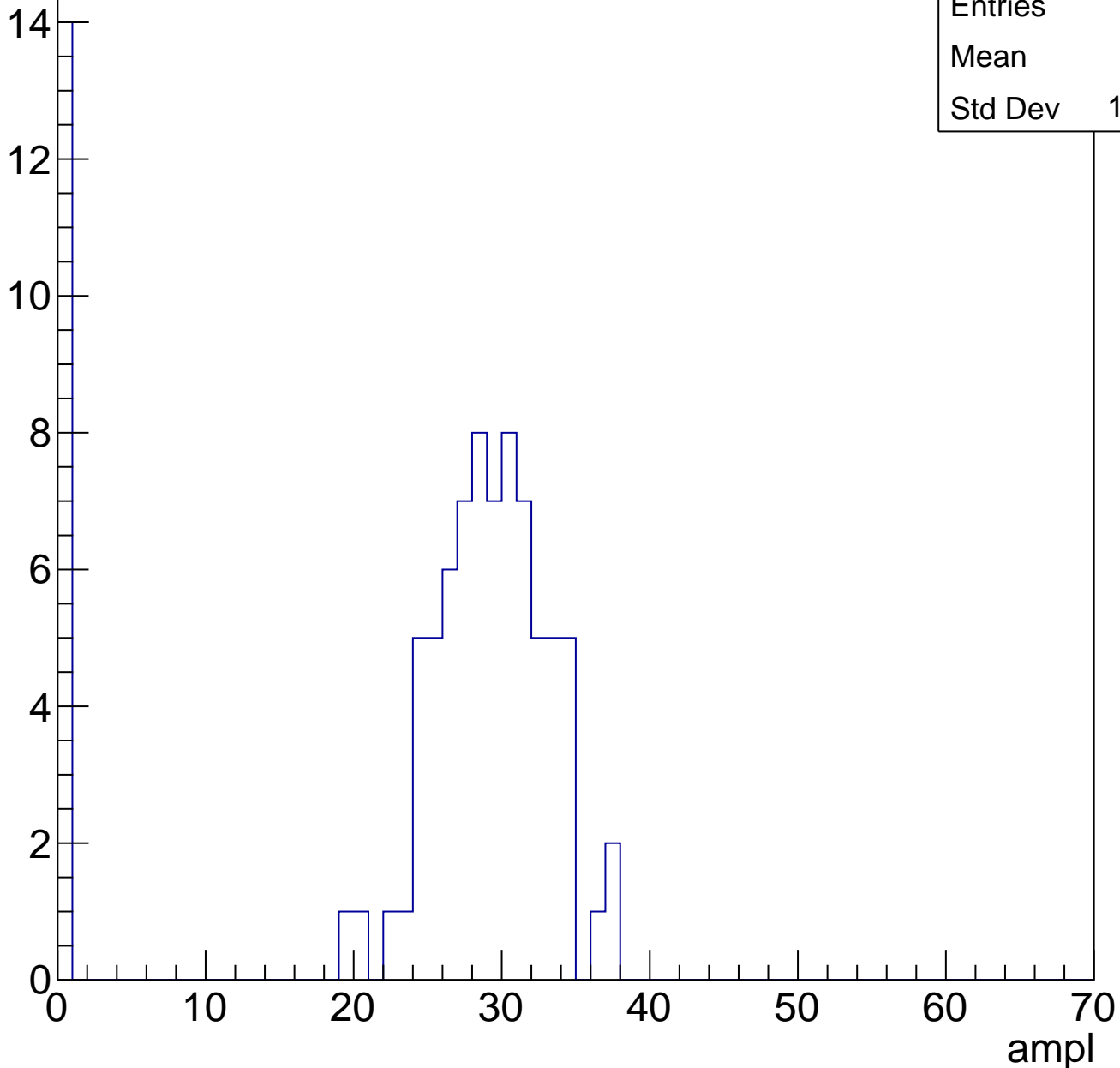
ampl

B1L103S, U5-ch52, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	24.3
Std Dev	11.03

Entry

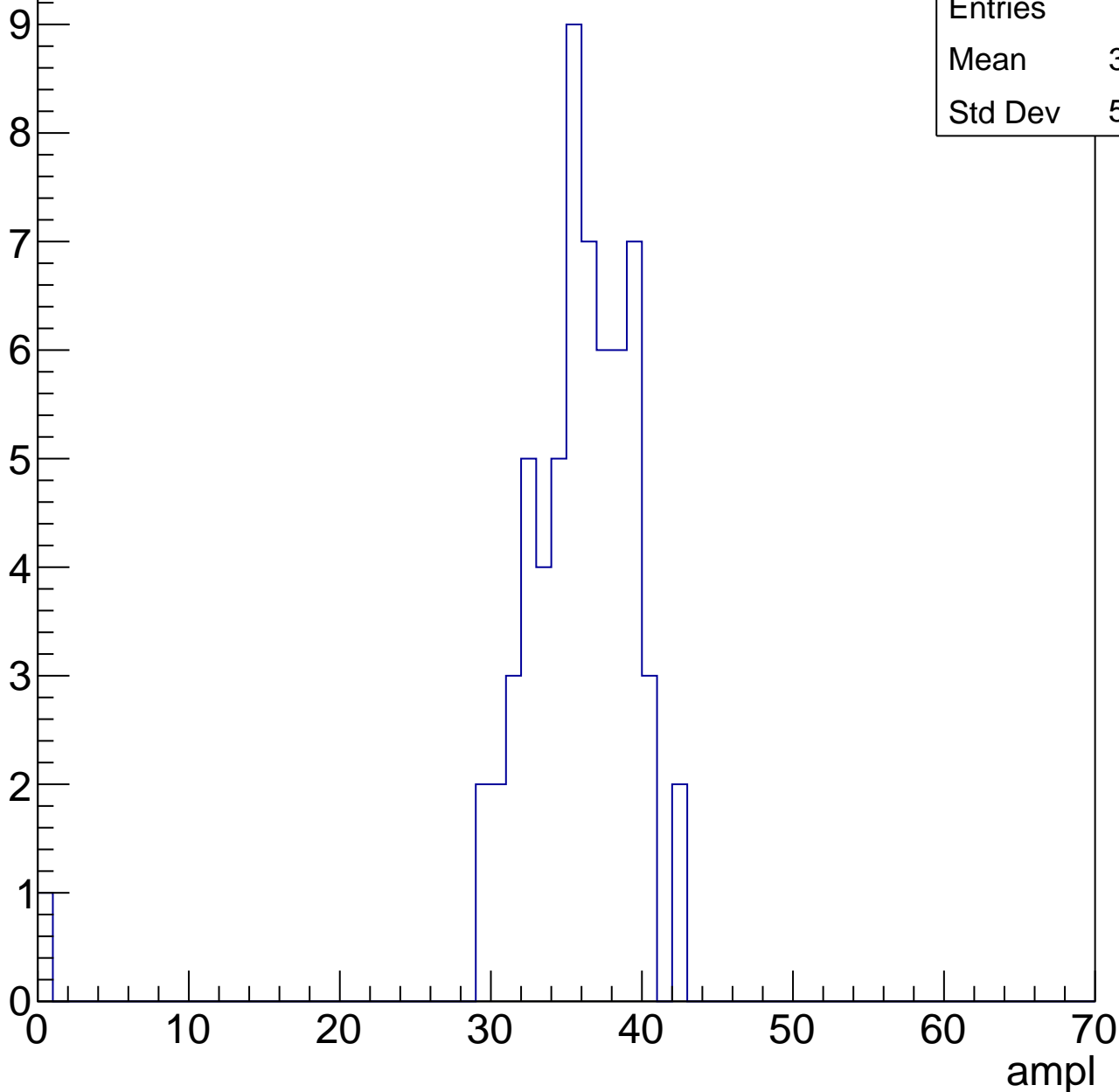


B1L103S, U5-ch52, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	34.95
Std Dev	5.434

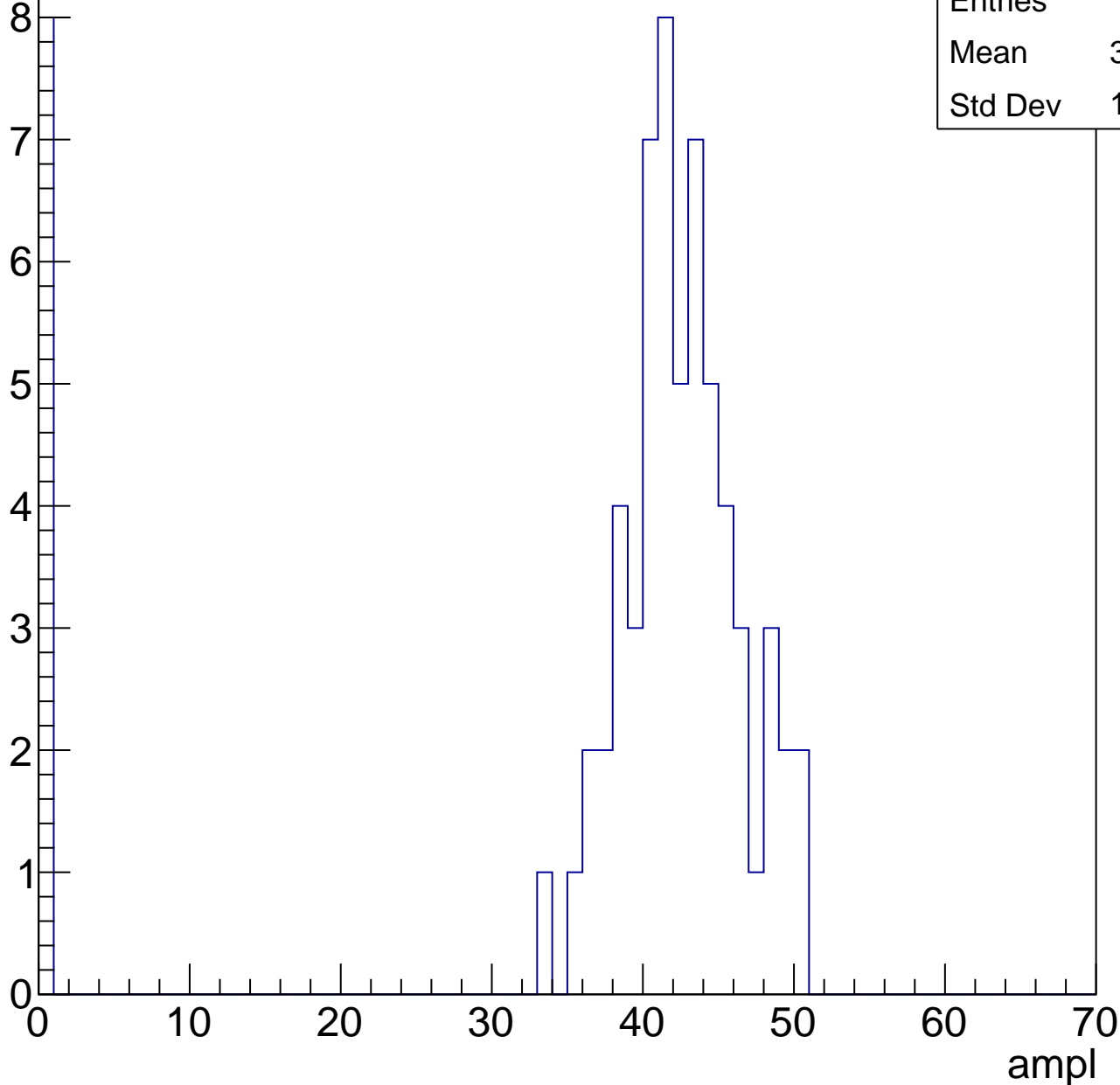


B1L103S, U5-ch52, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	37.19
Std Dev	14.03

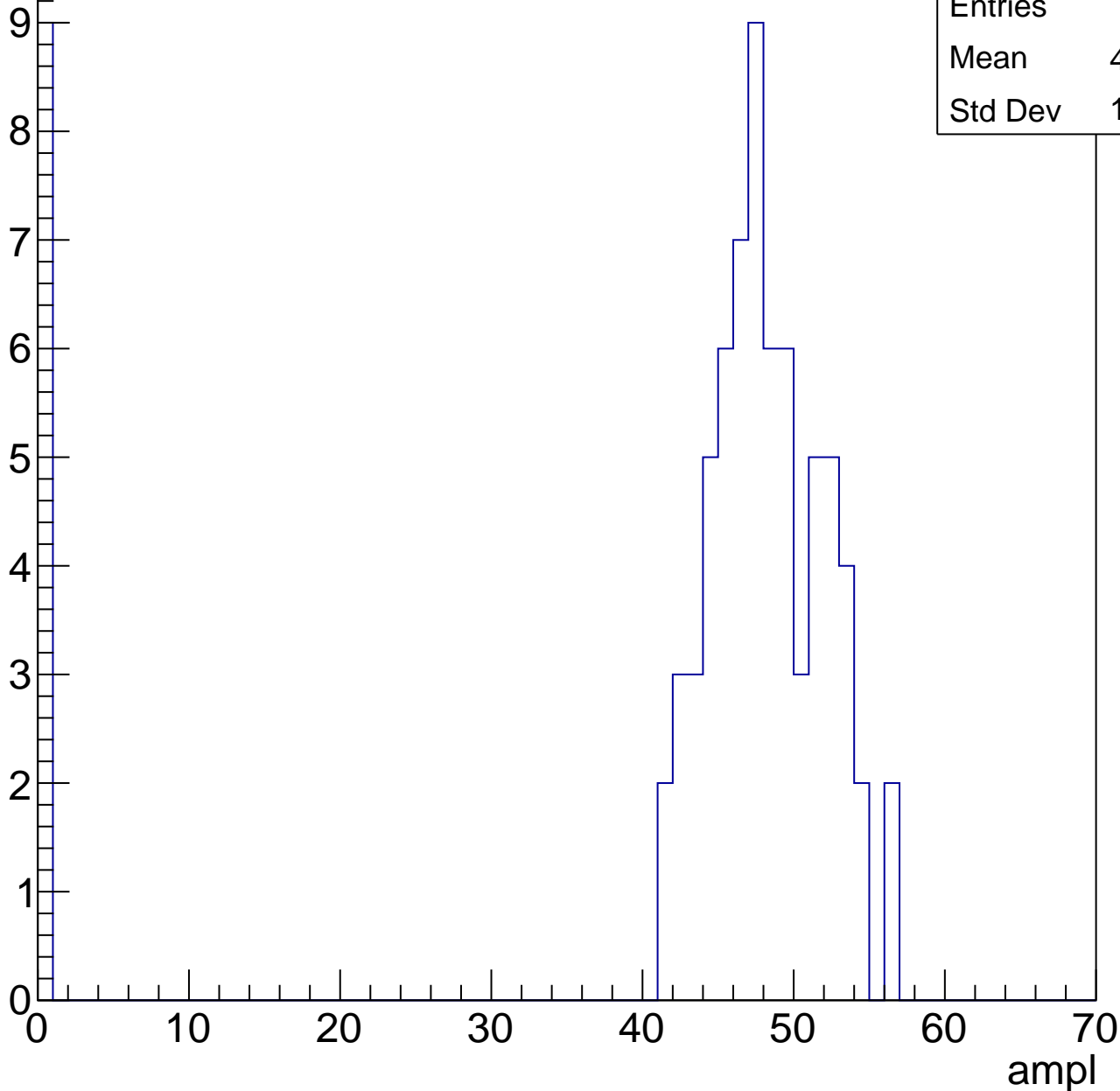


B1L103S, U5-ch52, adc3

calib_packv5_041523_1651.root, FC#0, port C2

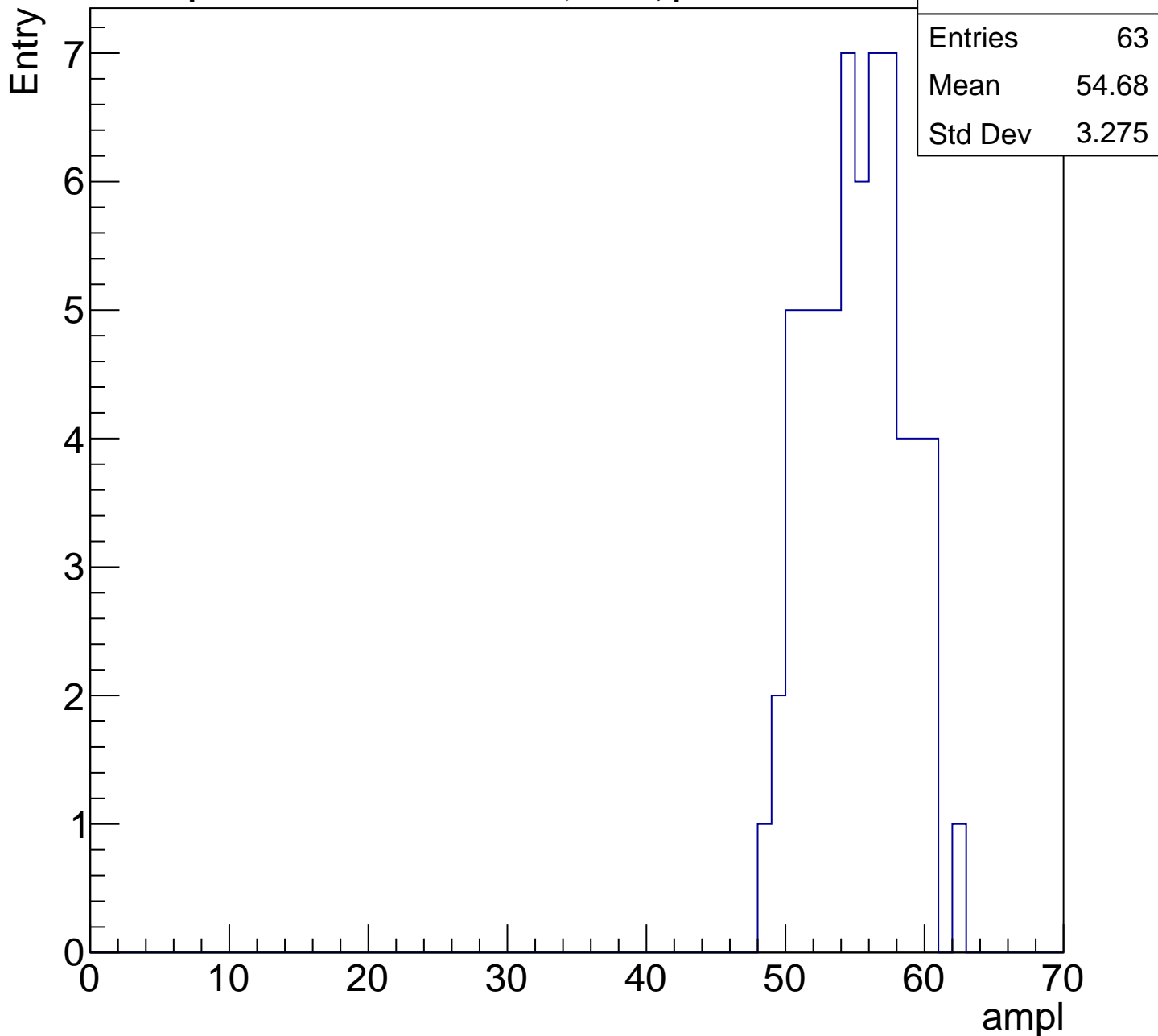
Entry

Entries	77
Mean	42.22
Std Dev	15.73



B1L103S, U5-ch52, adc4

calib_packv5_041523_1651.root, FC#0, port C2

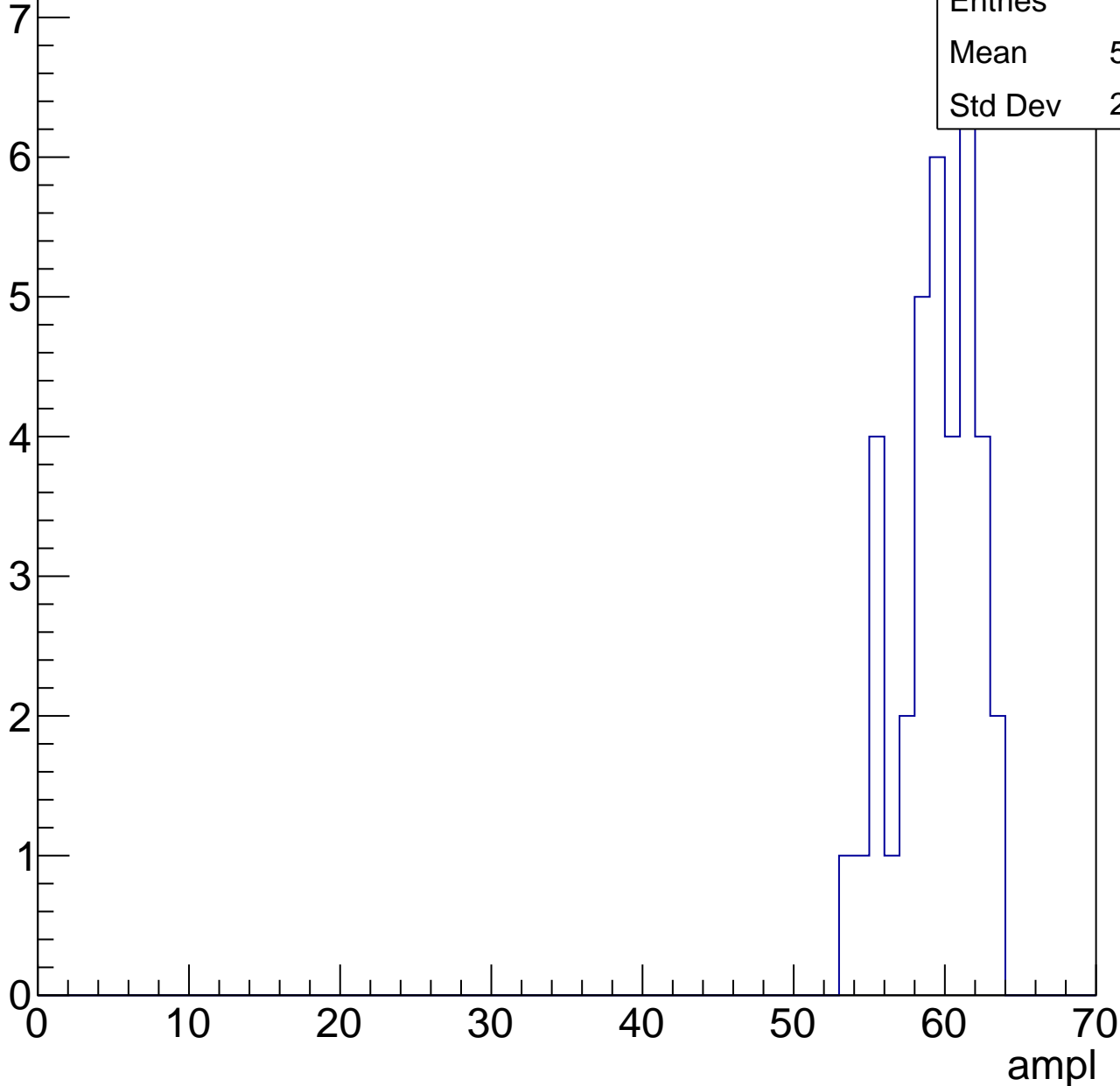


B1L103S, U5-ch52, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	37
Mean	58.97
Std Dev	2.584

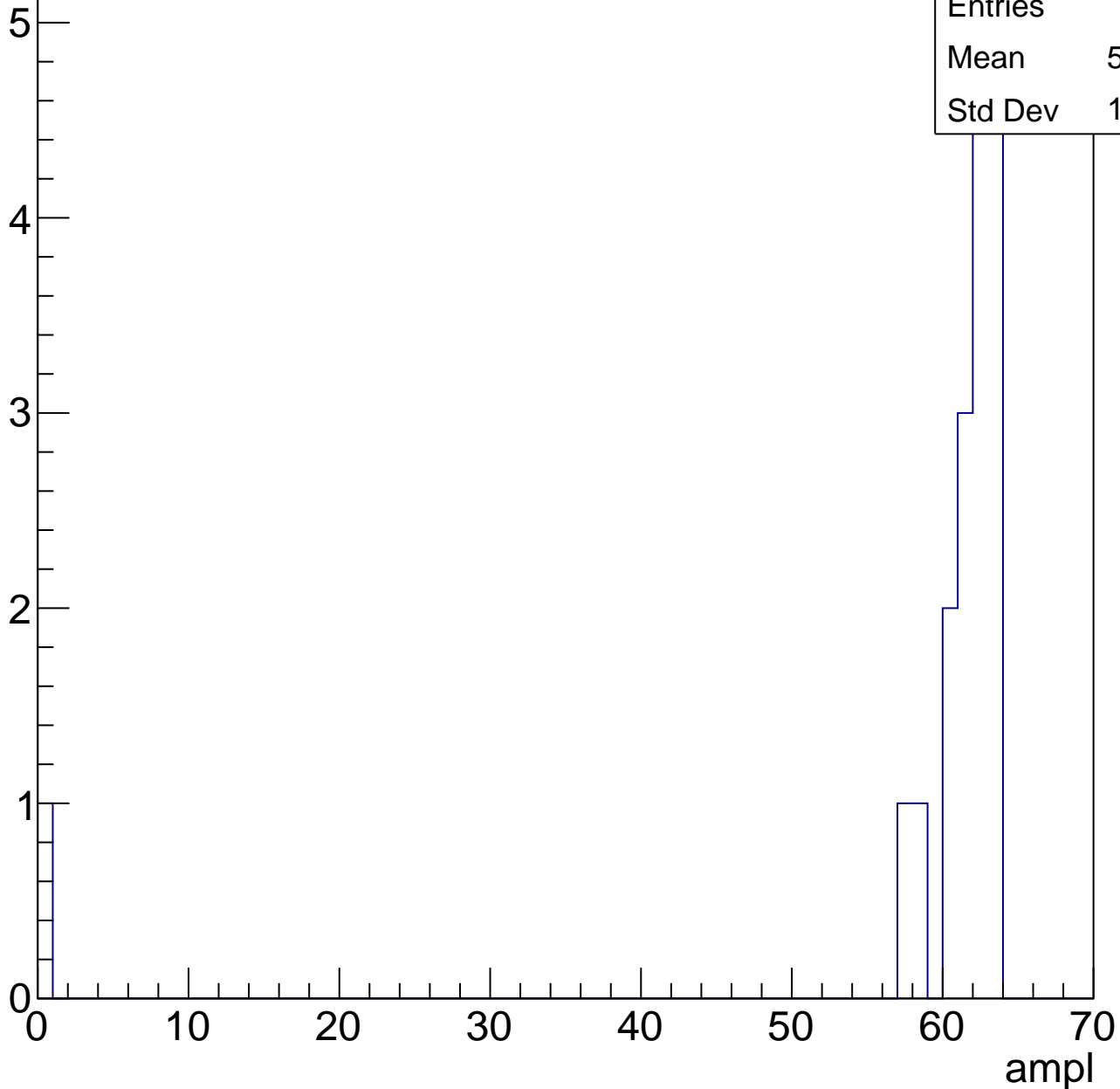


B1L103S, U5-ch52, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	18
Mean	57.94
Std Dev	14.15

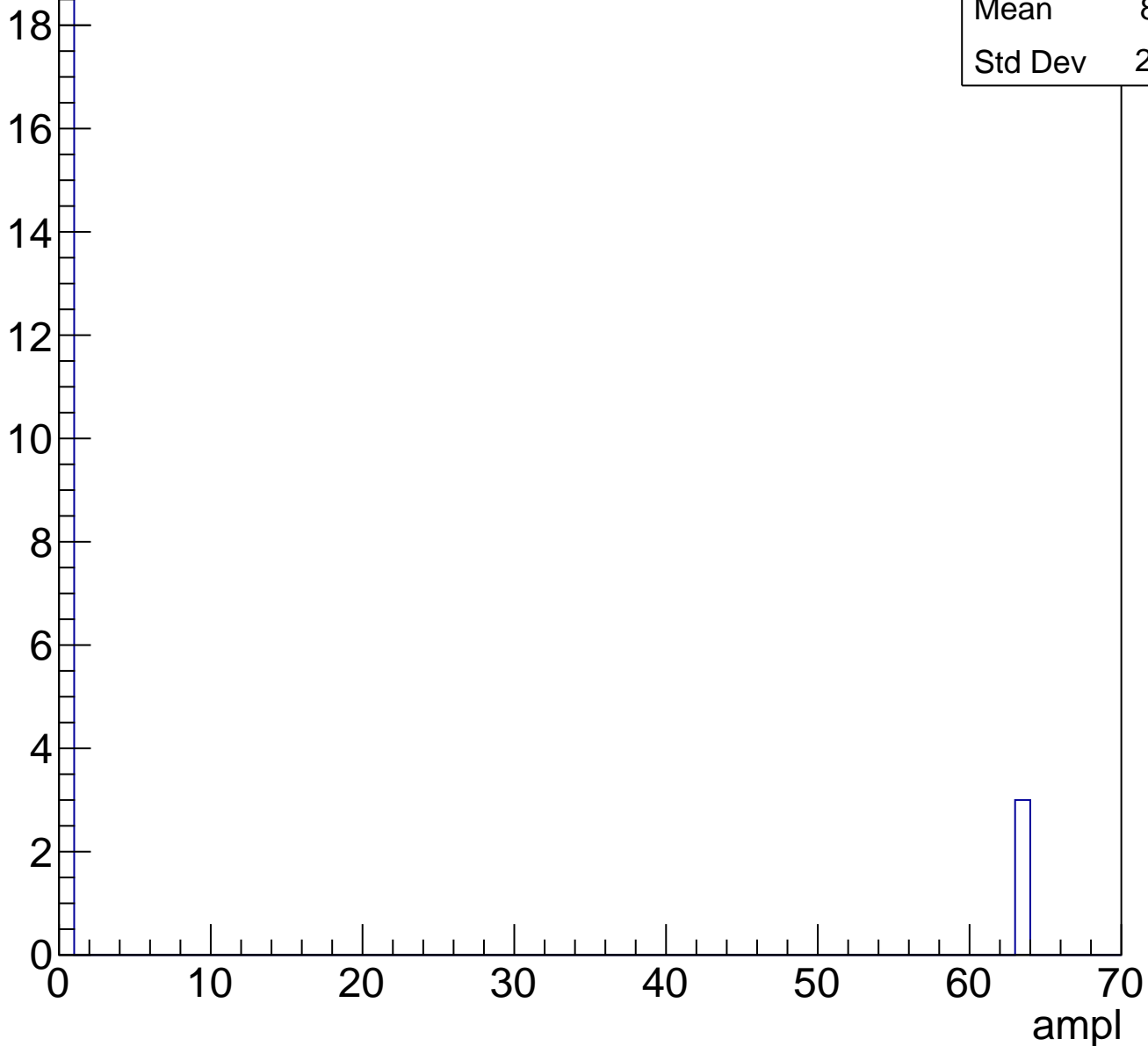


B1L103S, U5-ch52, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	22
Mean	8.591
Std Dev	21.62

Entry

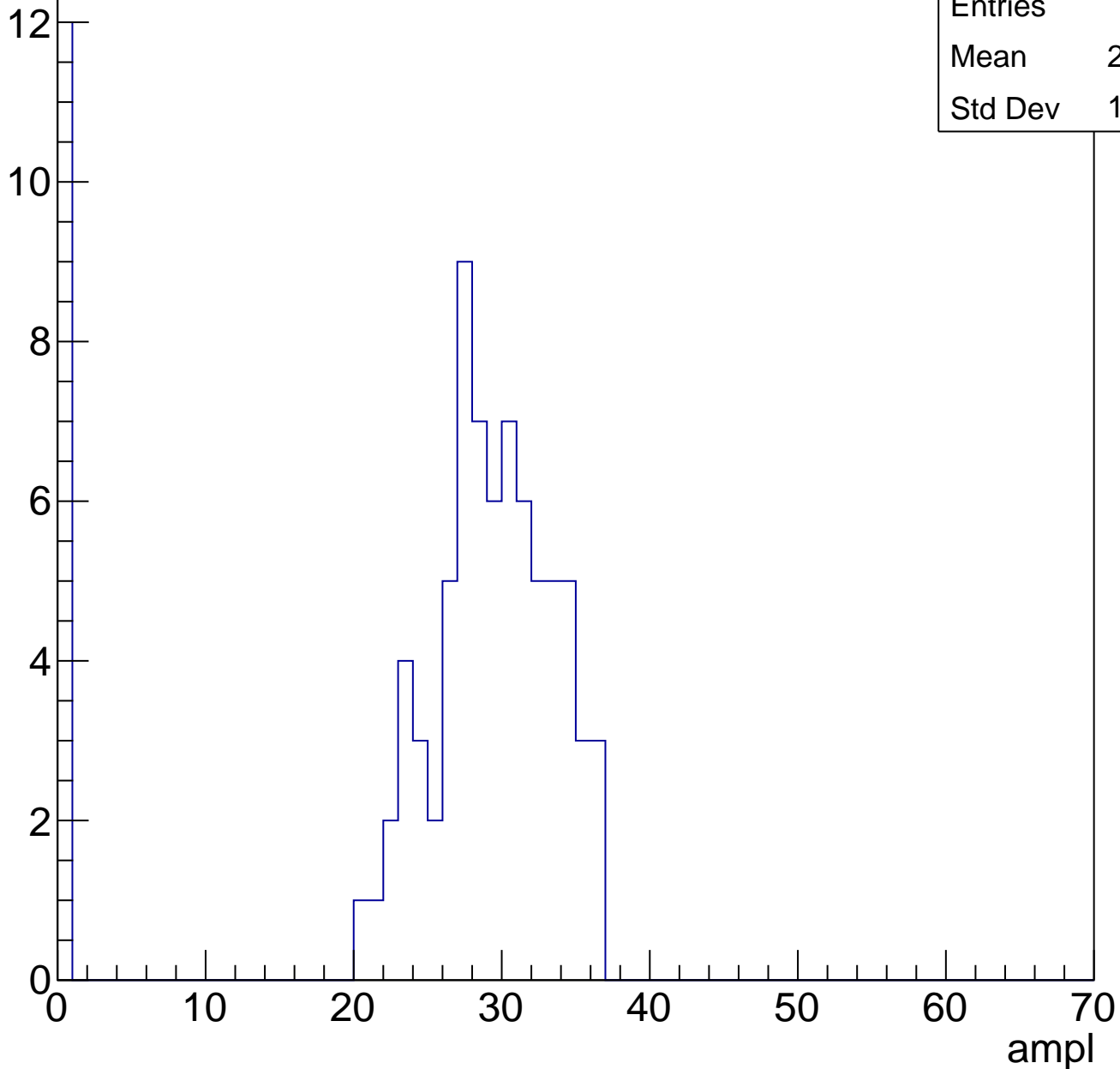


B1L103S, U5-ch53, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	86
Mean	24.95
Std Dev	10.68

Entry

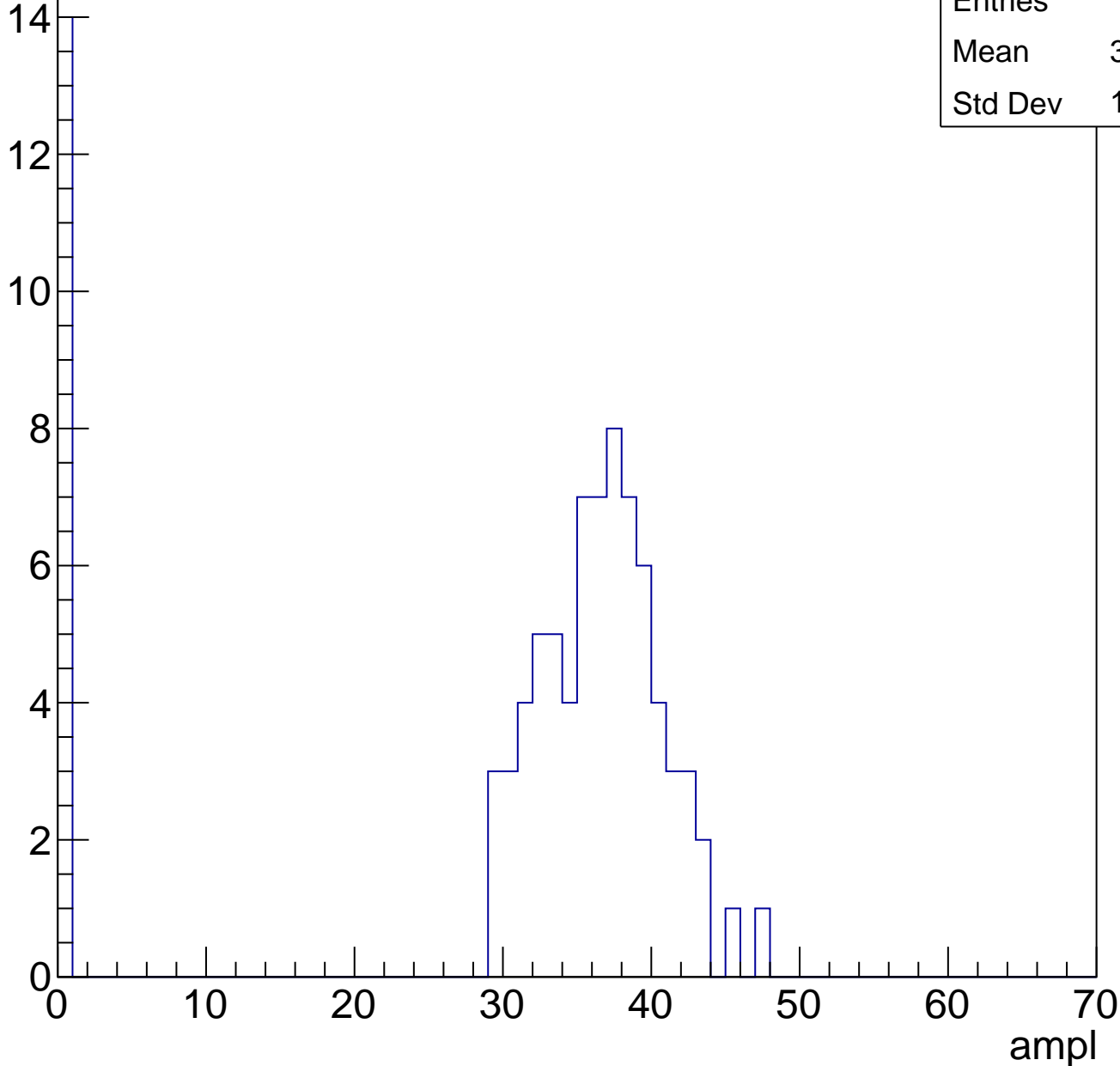


B1L103S, U5-ch53, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	87
Mean	30.37
Std Dev	13.78

Entry

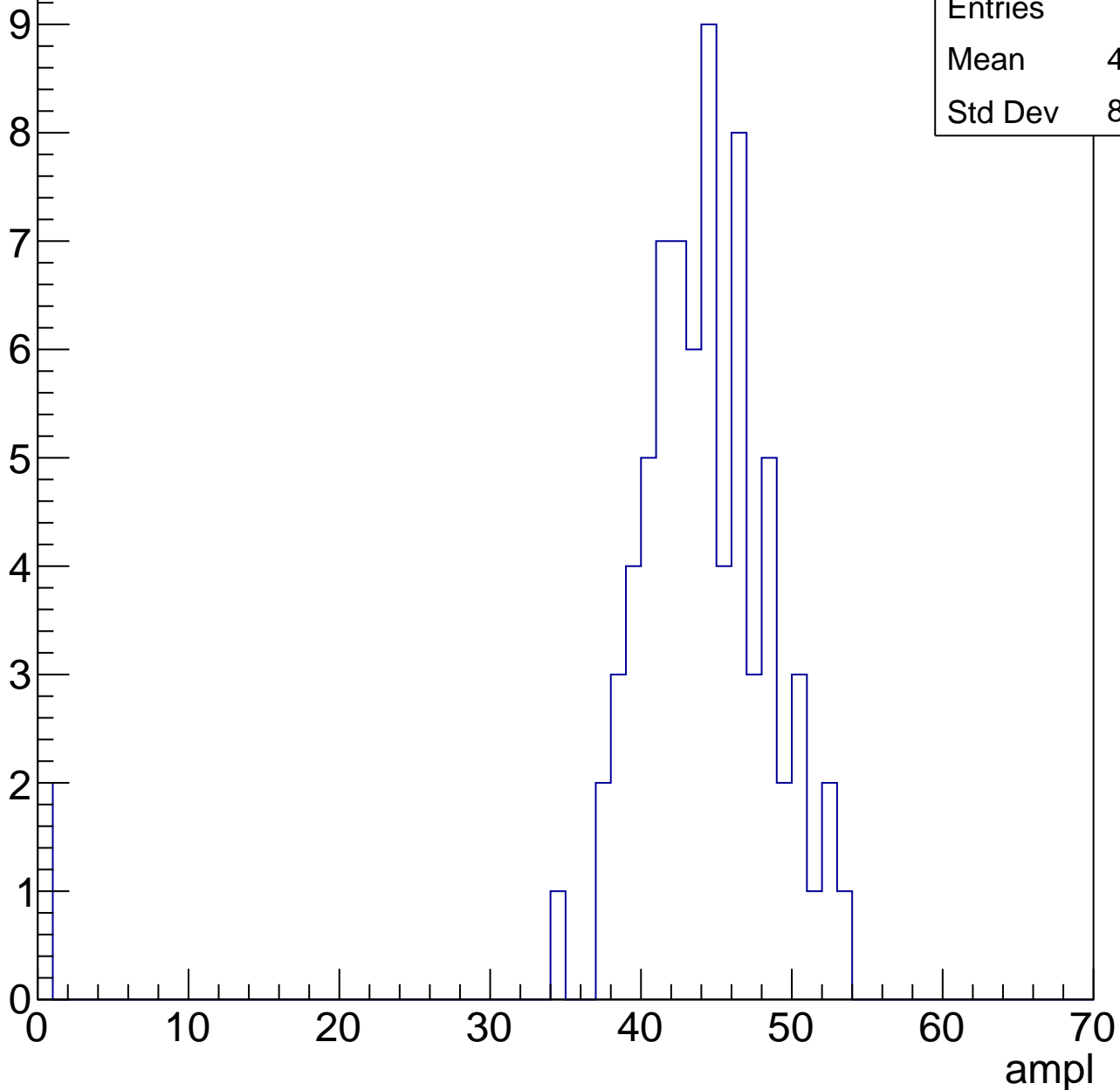


B1L103S, U5-ch53, adc2

calib_packv5_041523_1651.root, FC#0, port C2

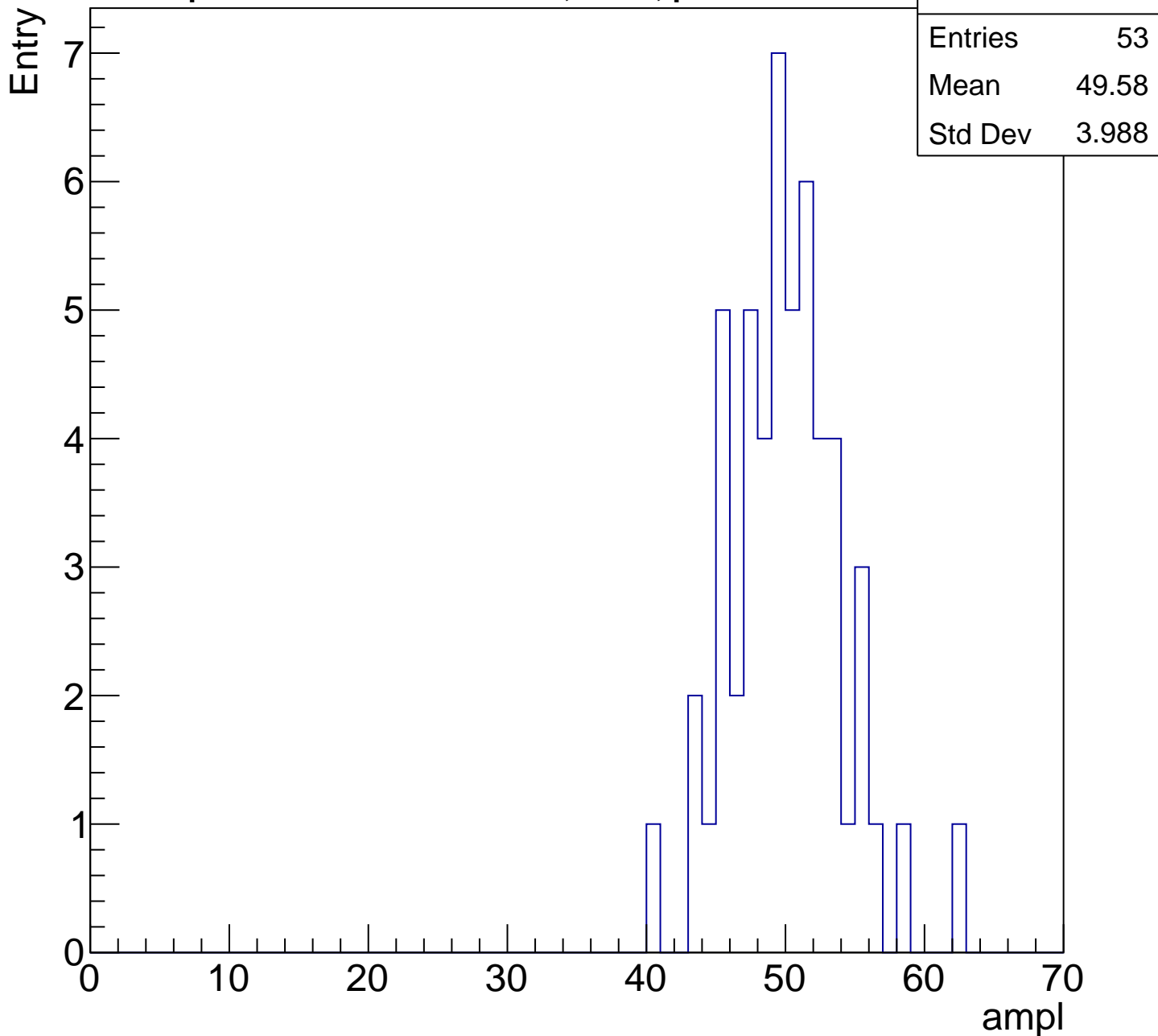
Entry

Entries	75
Mean	42.64
Std Dev	8.062



B1L103S, U5-ch53, adc3

calib_packv5_041523_1651.root, FC#0, port C2

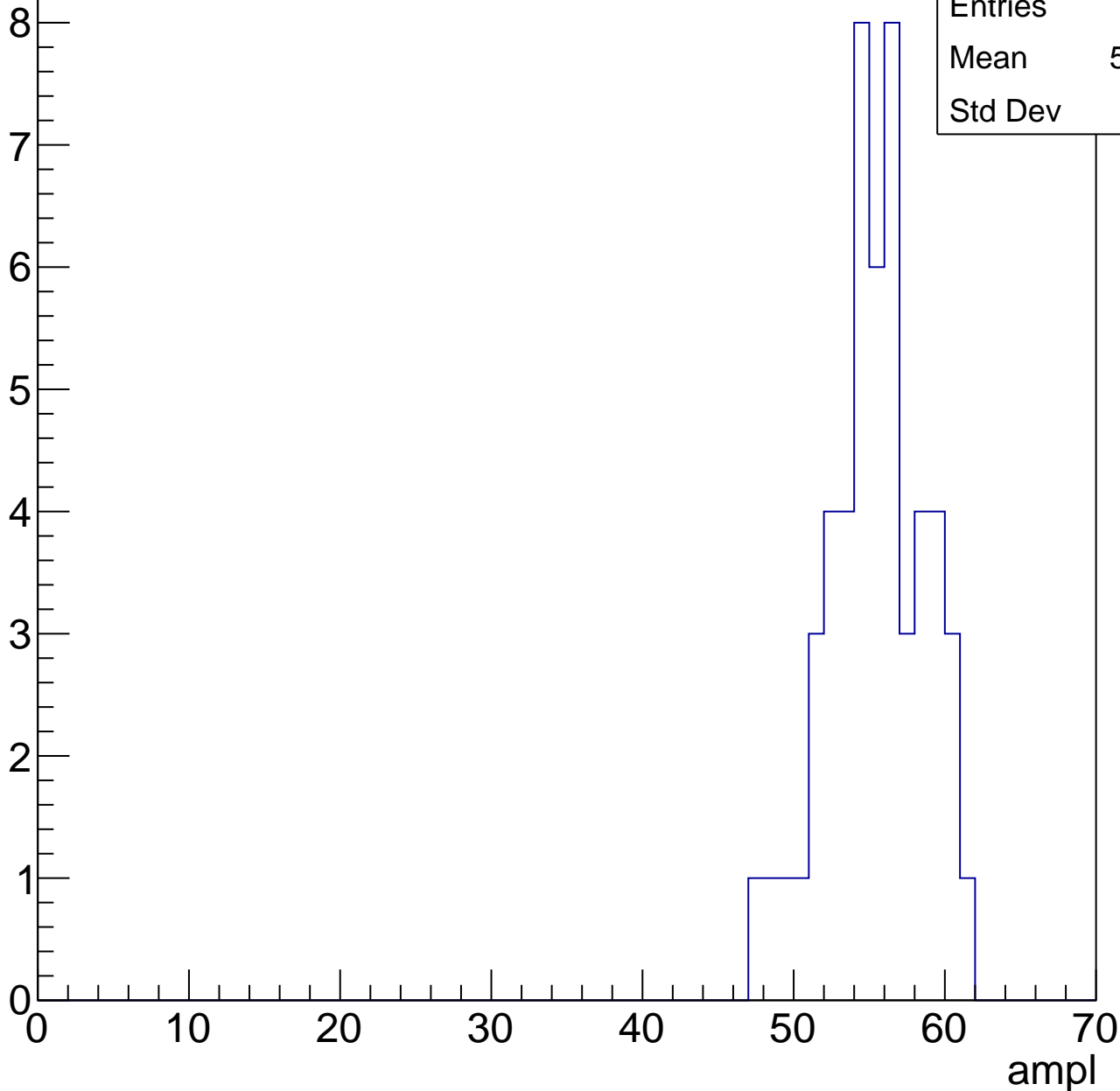


B1L103S, U5-ch53, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	54.94
Std Dev	3.14

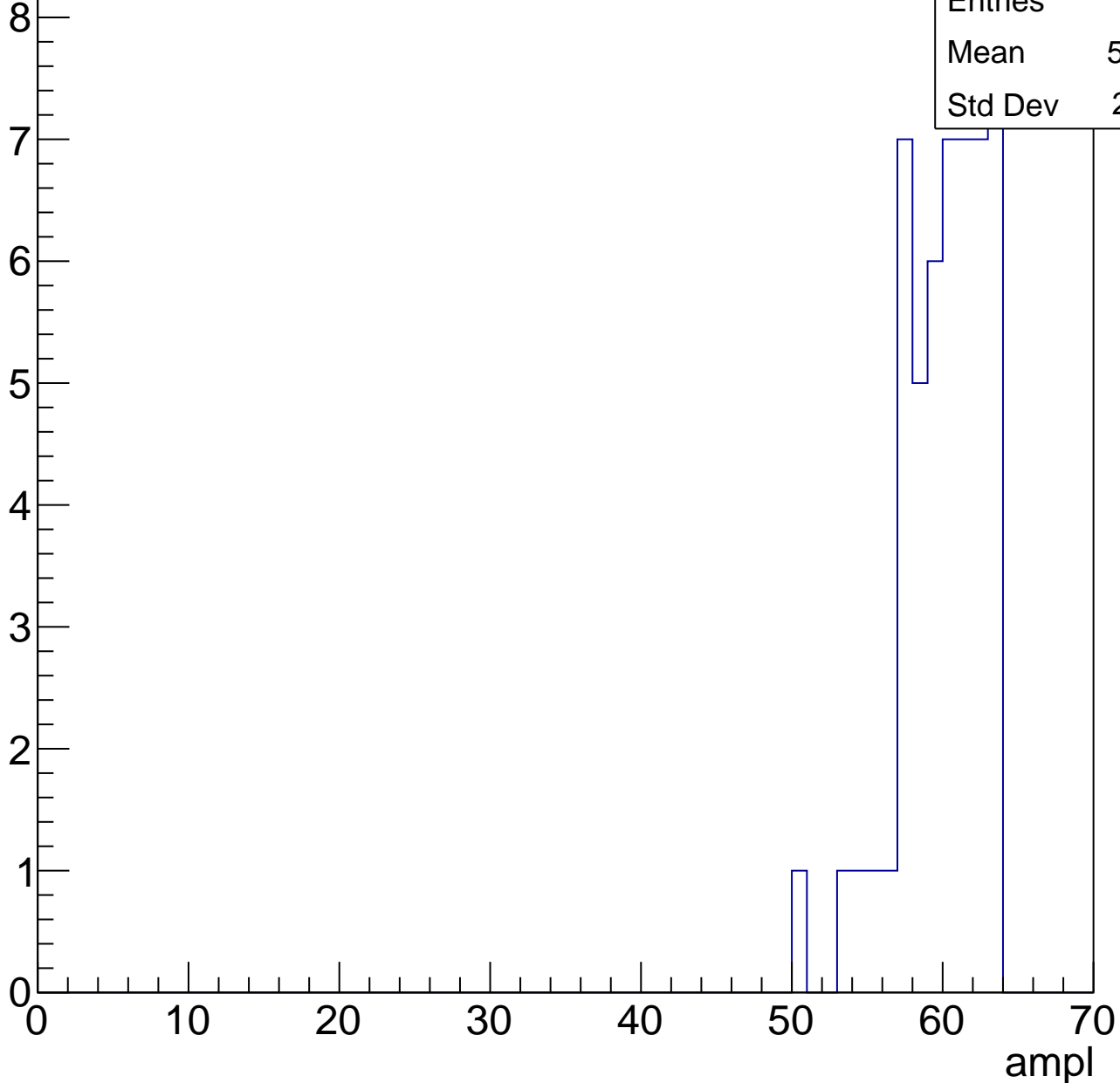


B1L103S, U5-ch53, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

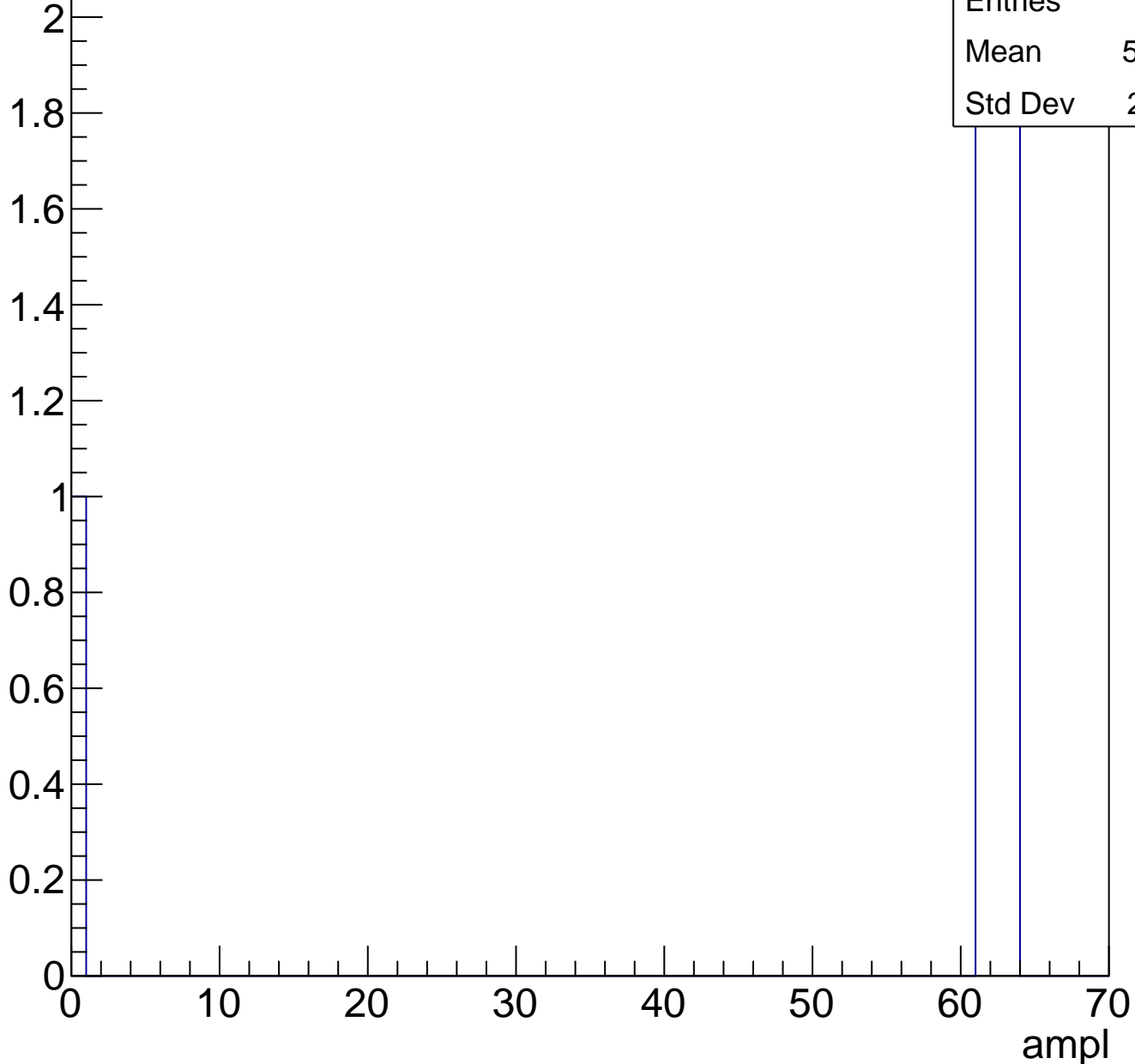
Entries	52
Mean	59.54
Std Dev	2.811



B1L103S, U5-ch53, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch53, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch54, adc0

calib_packv5_041523_1651.root, FC#0, port C2

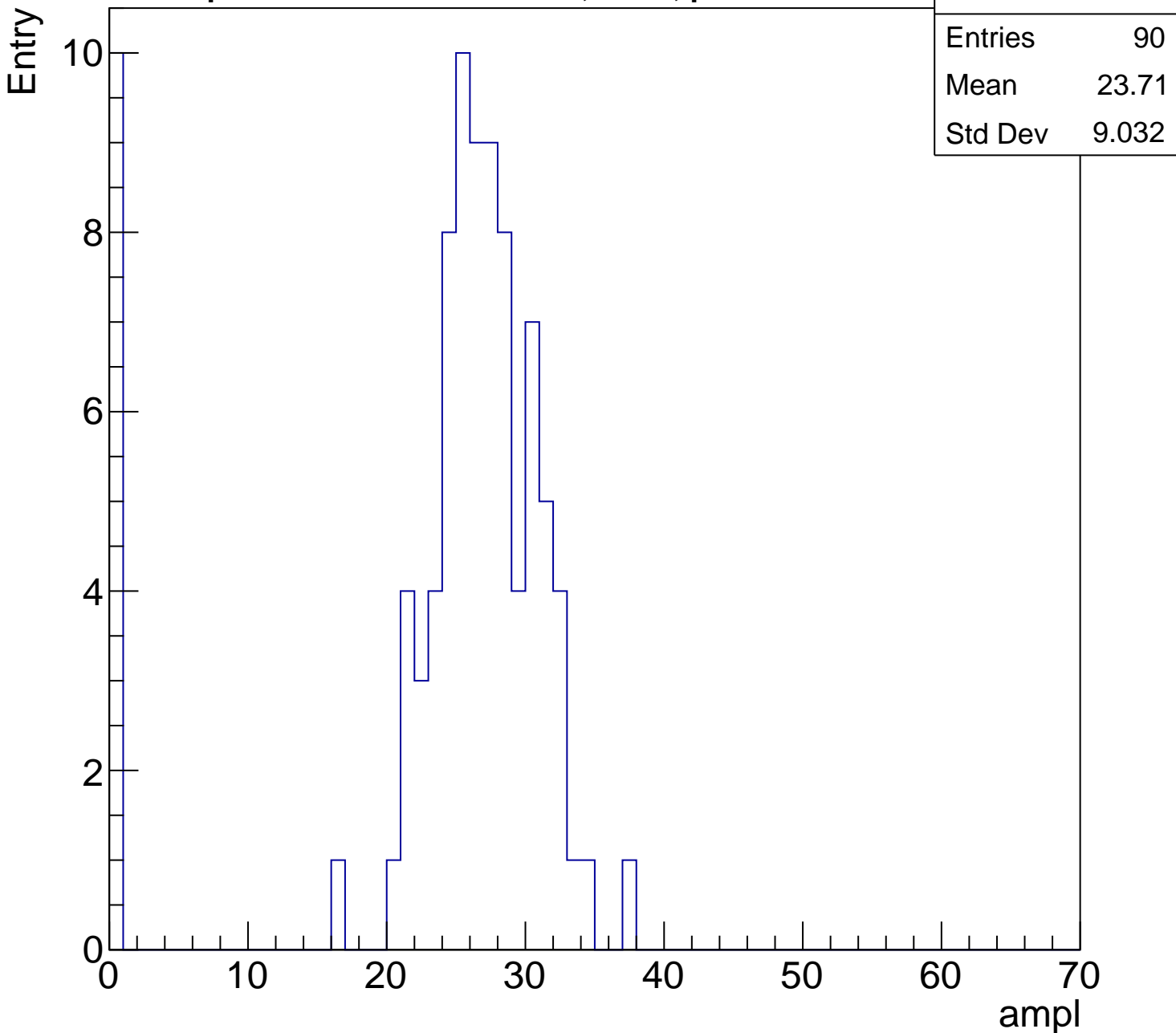
Entries	90
Mean	23.71
Std Dev	9.032

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

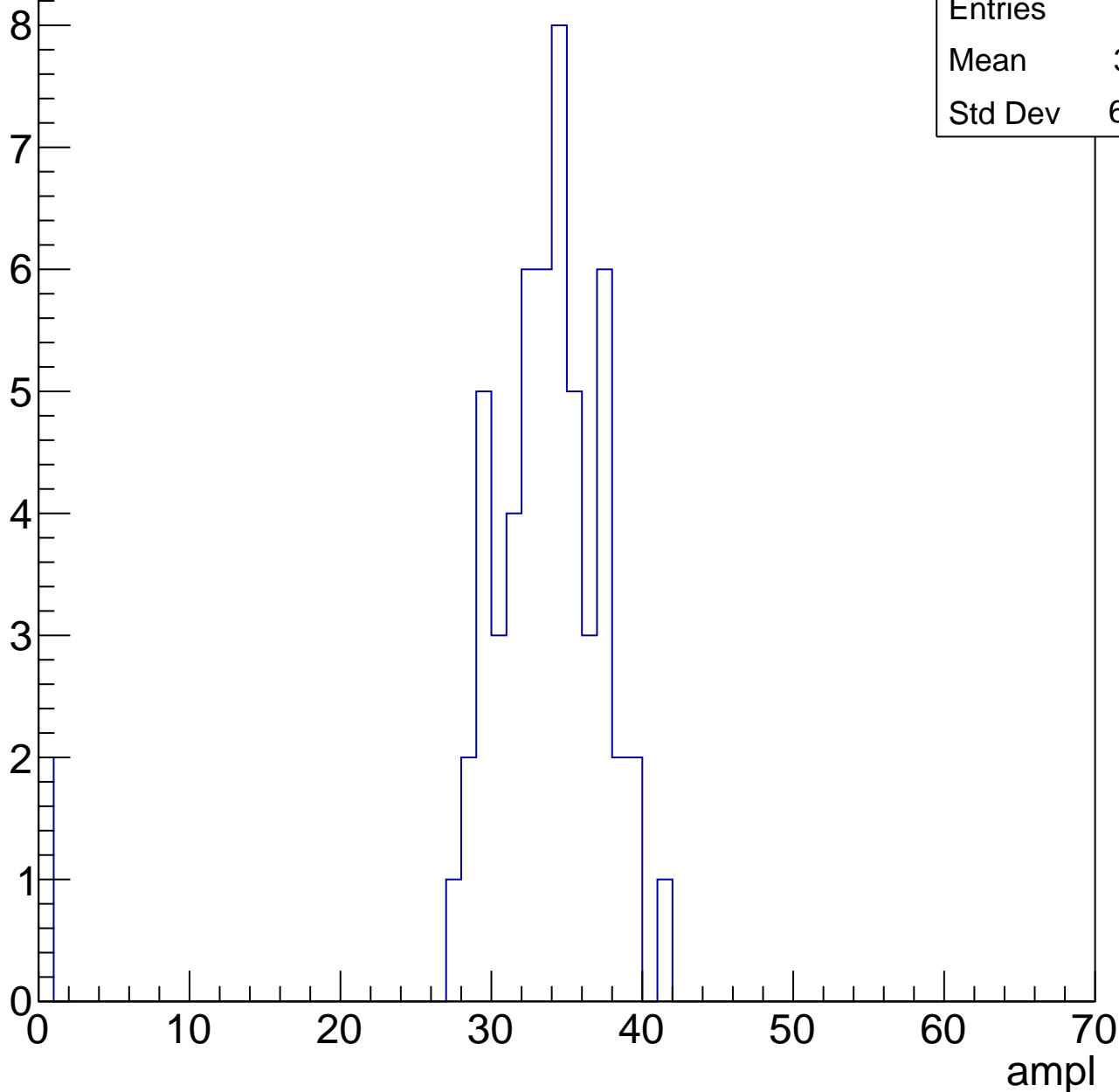


B1L103S, U5-ch54, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	32.21
Std Dev	6.938



B1L103S, U5-ch54, adc2

calib_packv5_041523_1651.root, FC#0, port C2

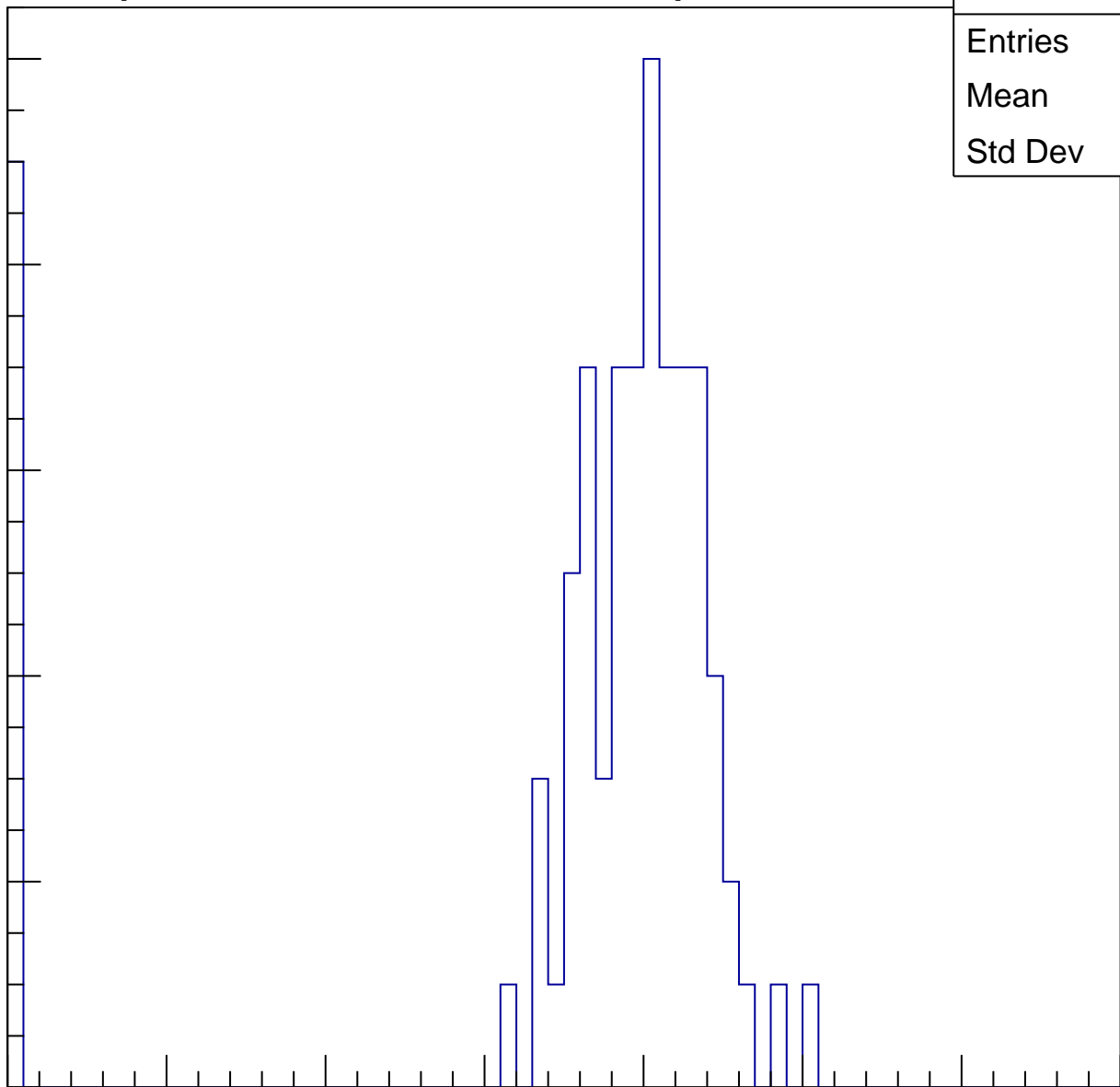
Entries	83
Mean	35.34
Std Dev	12.79

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

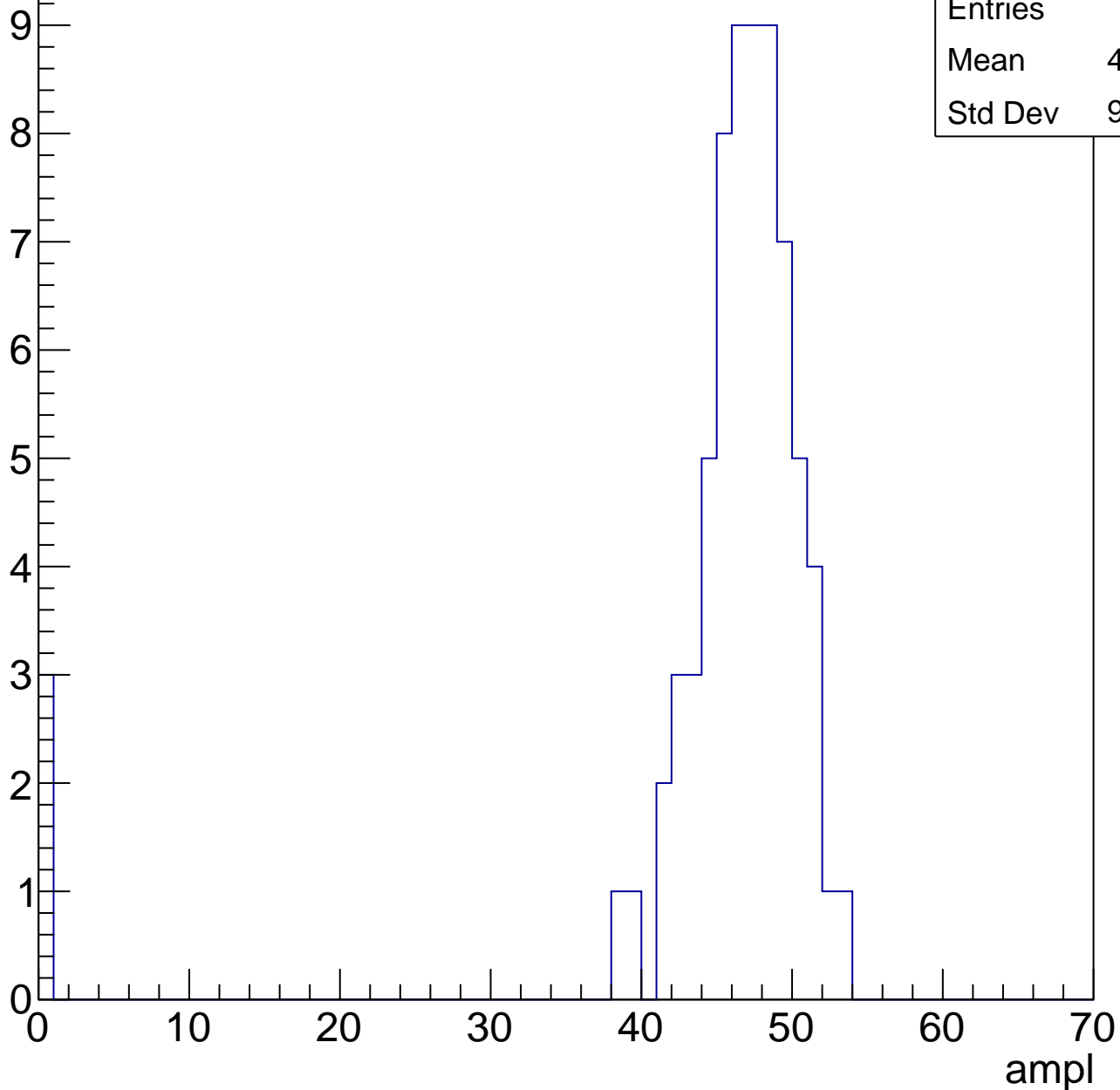
ampl



B1L103S, U5-ch54, adc3

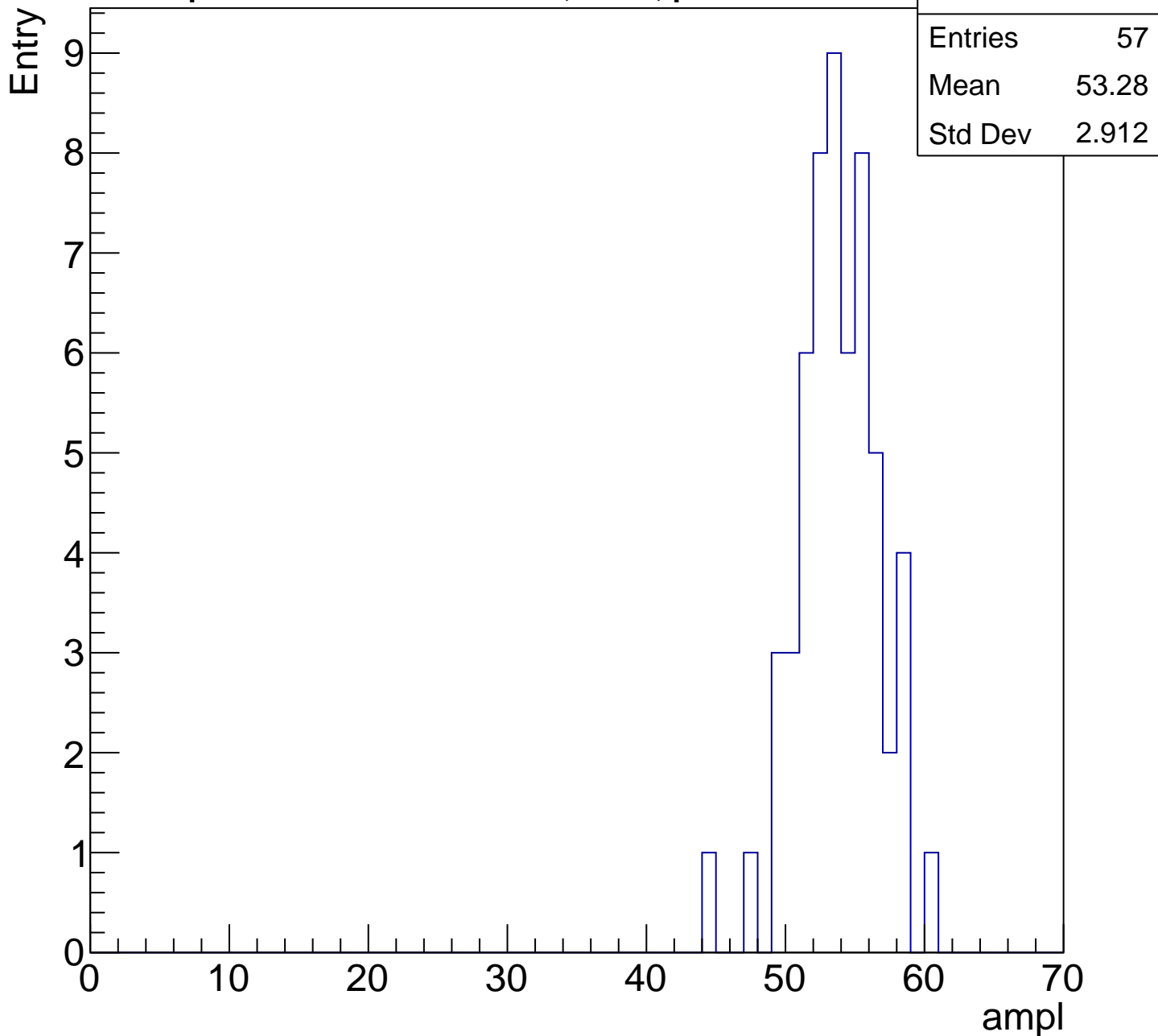
calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch54, adc4

calib_packv5_041523_1651.root, FC#0, port C2

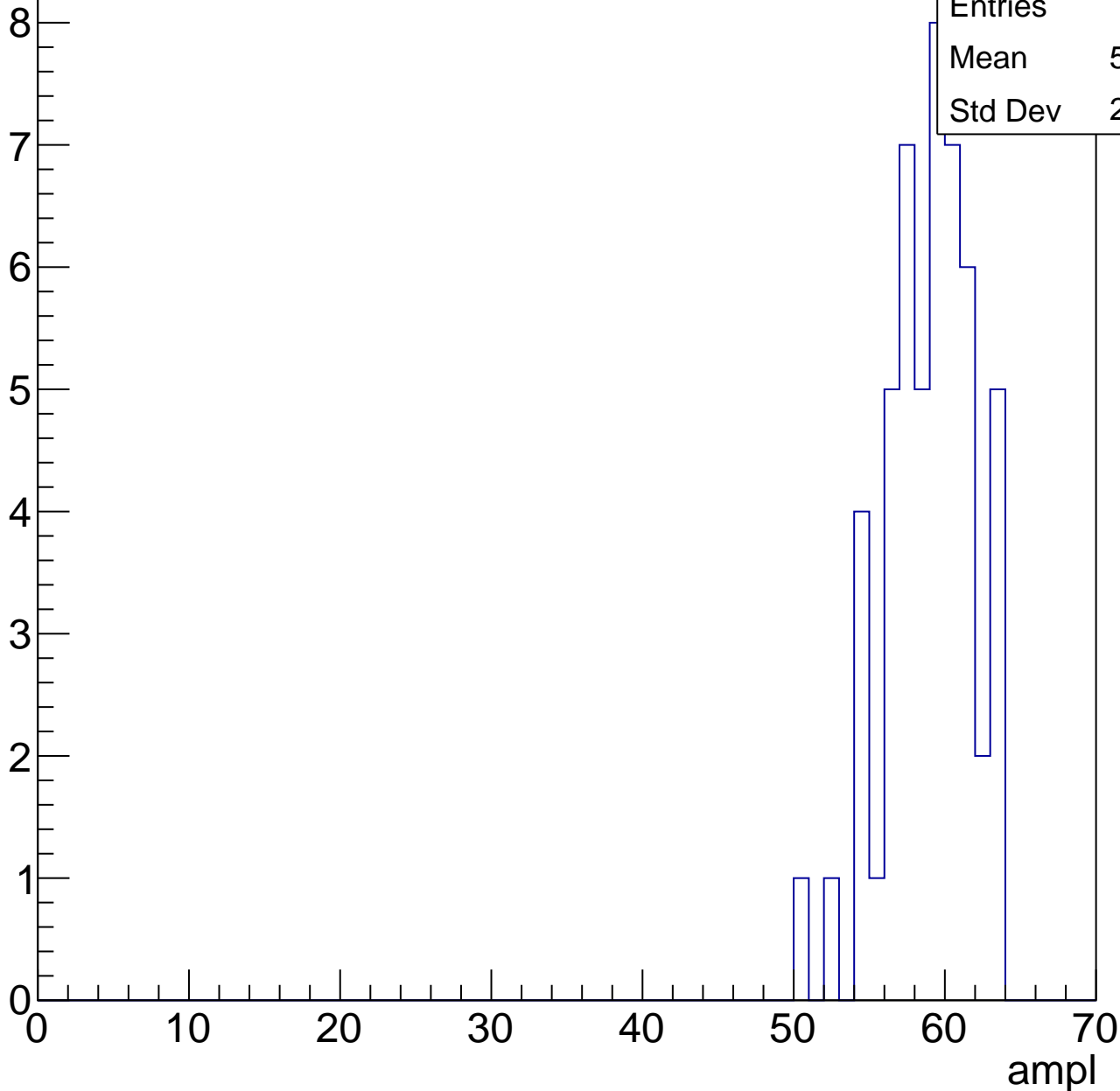


B1L103S, U5-ch54, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	58.44
Std Dev	2.898

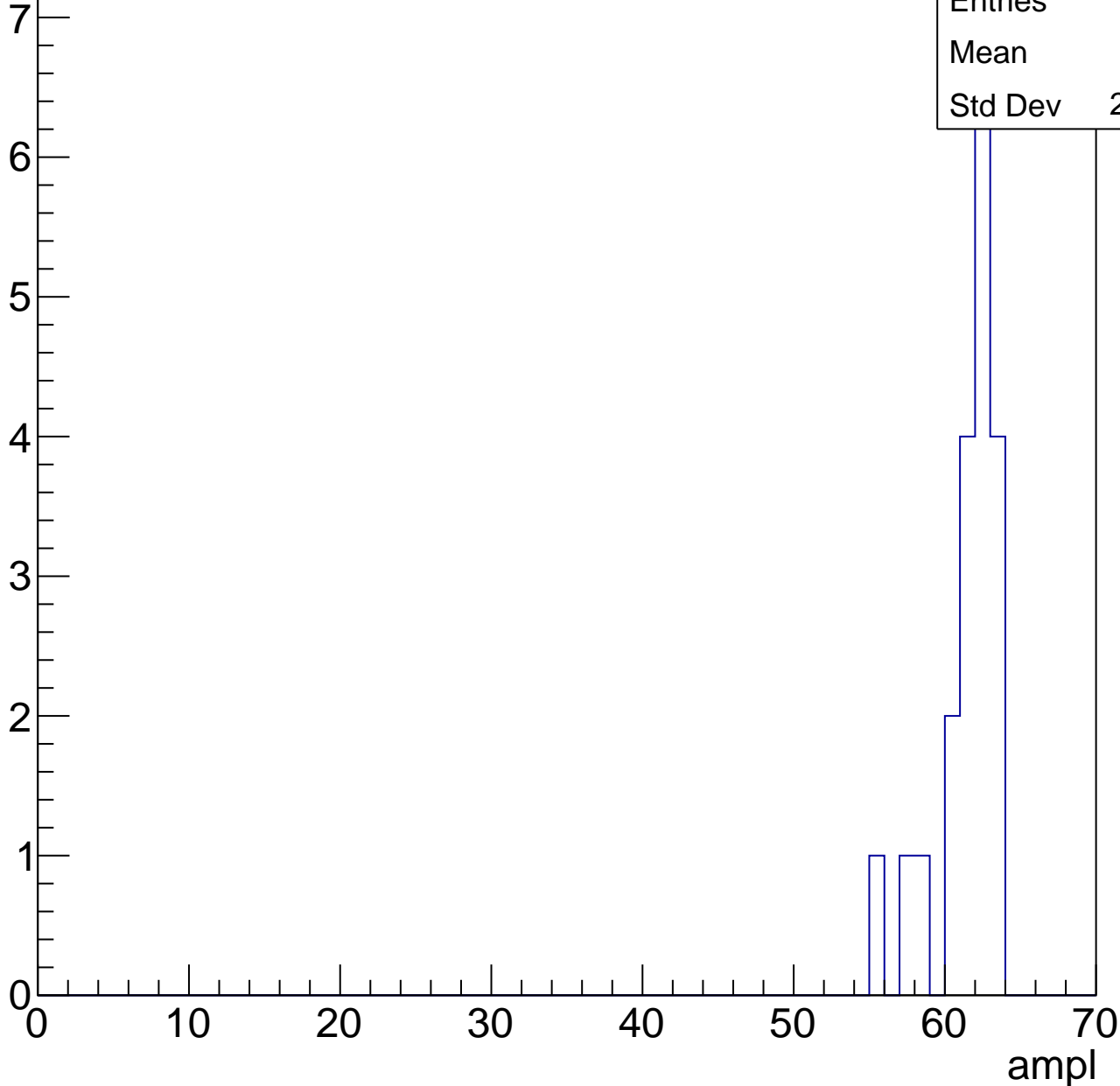


B1L103S, U5-ch54, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	20
Mean	61
Std Dev	2.074



B1L103S, U5-ch54, adc7

calib_packv5_041523_1651.root, FC#0, port C2

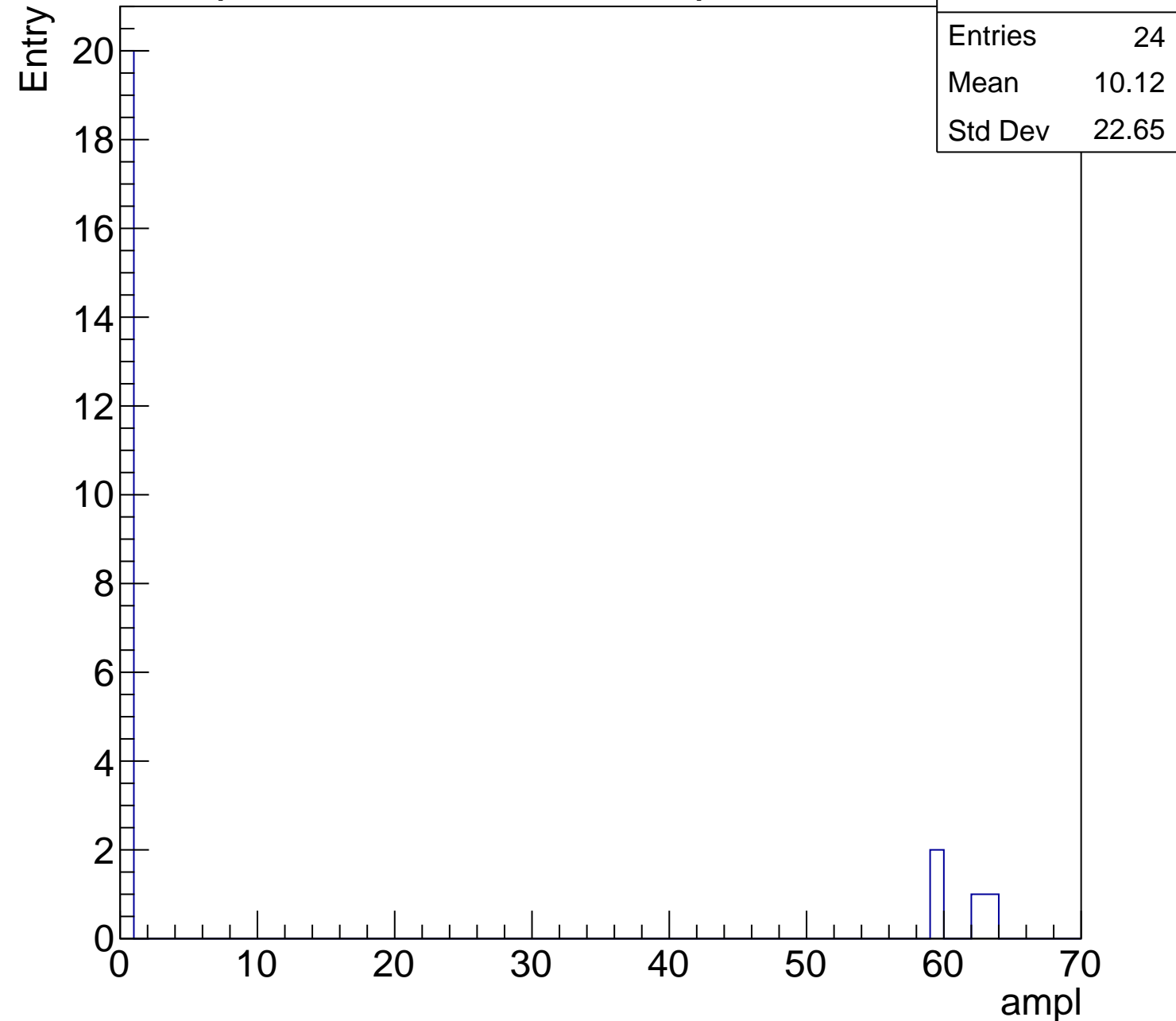
Entry

20
18
16
14
12
10
8
6
4
2
0

Entries	24
Mean	10.12
Std Dev	22.65

0 10 20 30 40 50 60 70

ampl

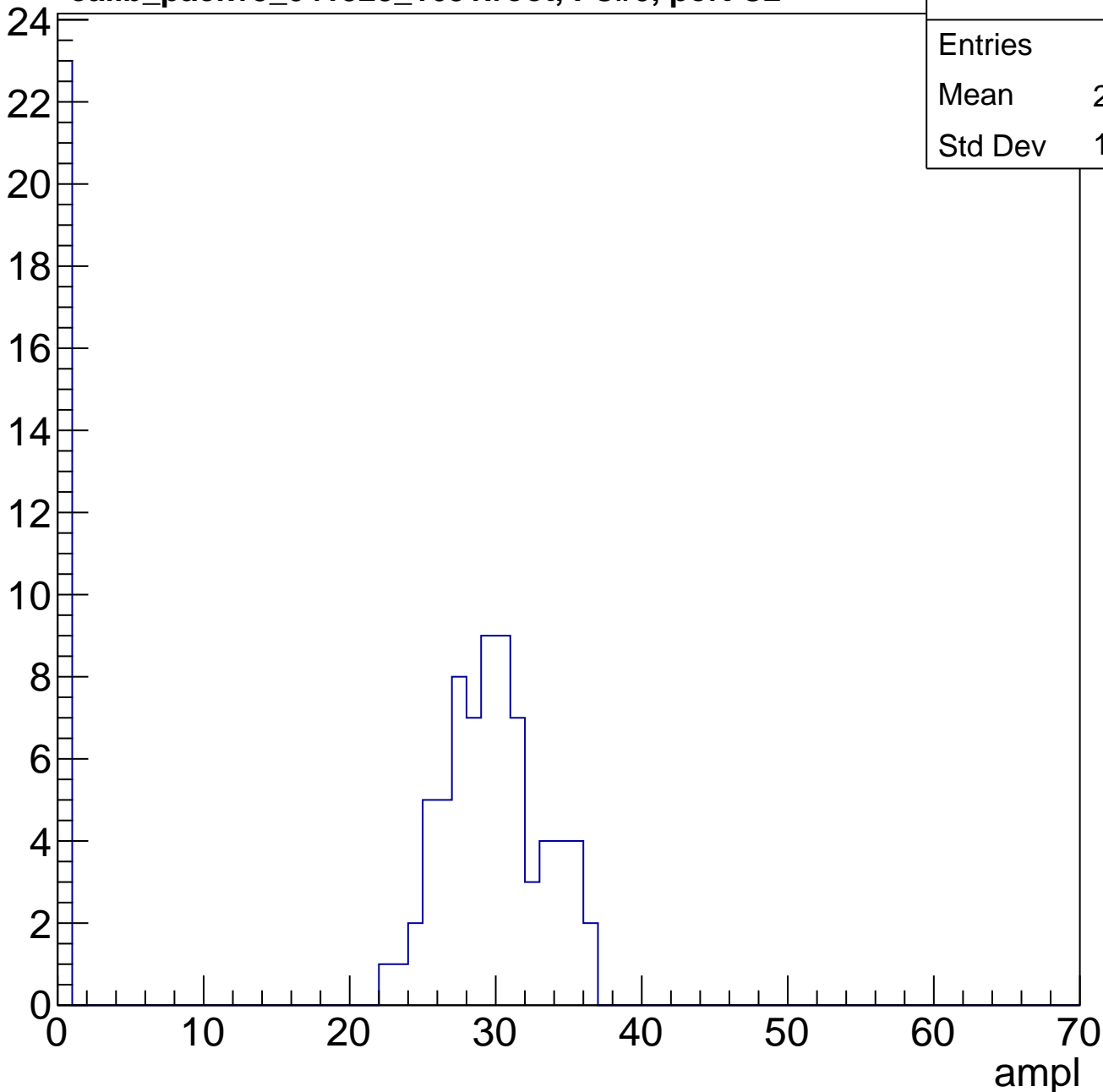


B1L103S, U5-ch55, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	94
Mean	22.17
Std Dev	12.93

Entry

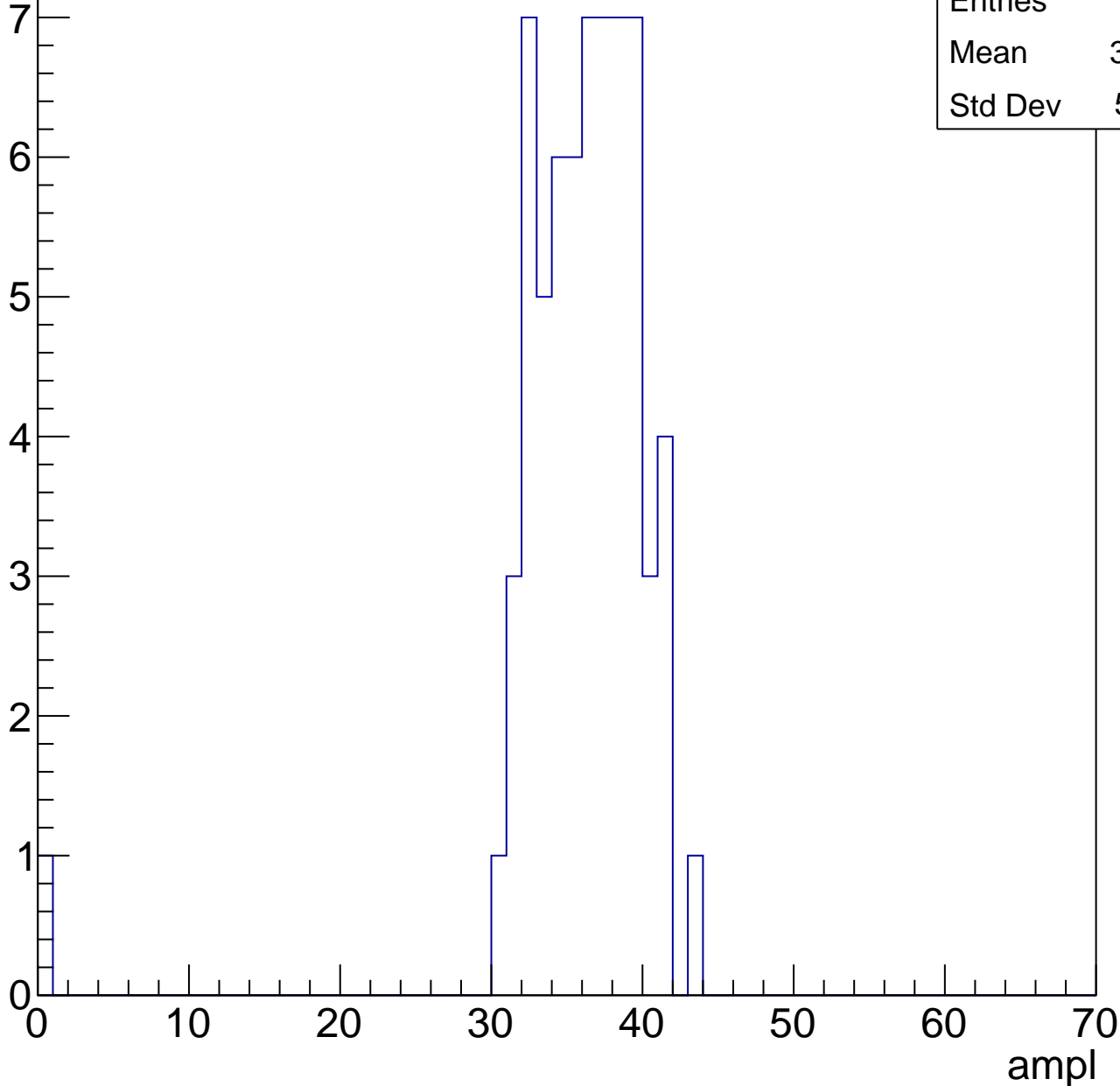


B1L103S, U5-ch55, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	35.43
Std Dev	5.361

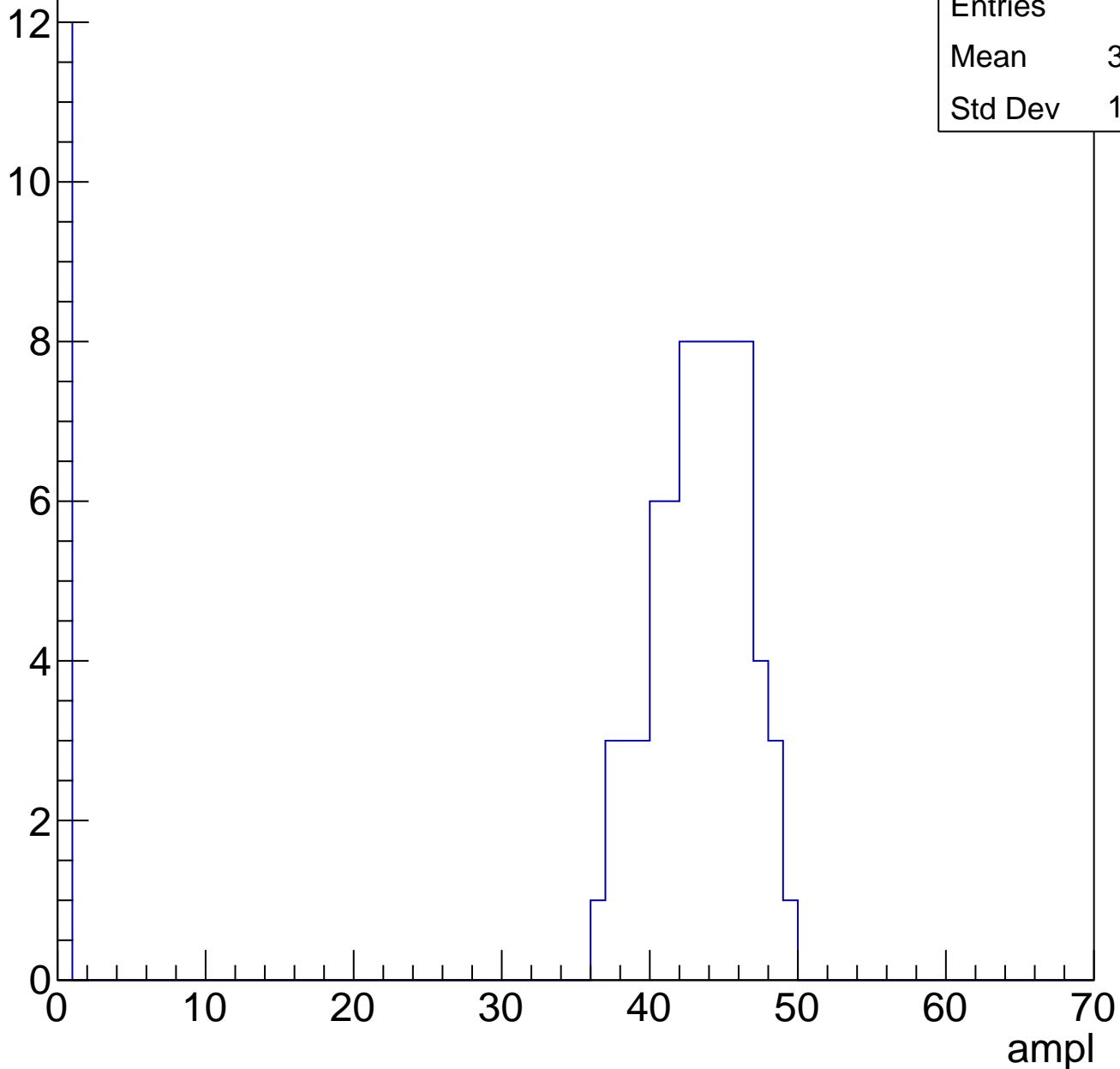


B1L103S, U5-ch55, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	36.65
Std Dev	15.43

Entry

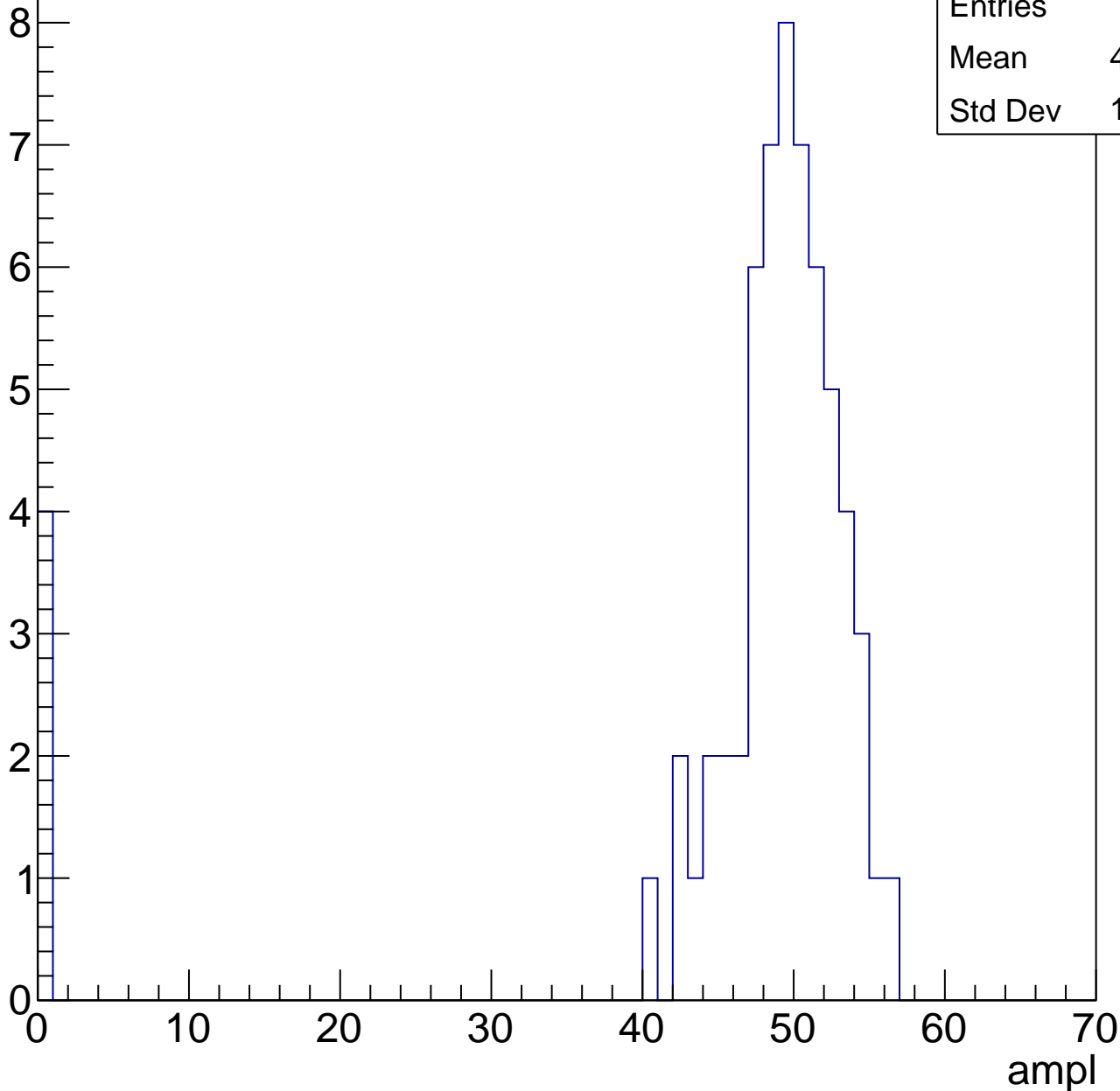


B1L103S, U5-ch55, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	45.94
Std Dev	12.49

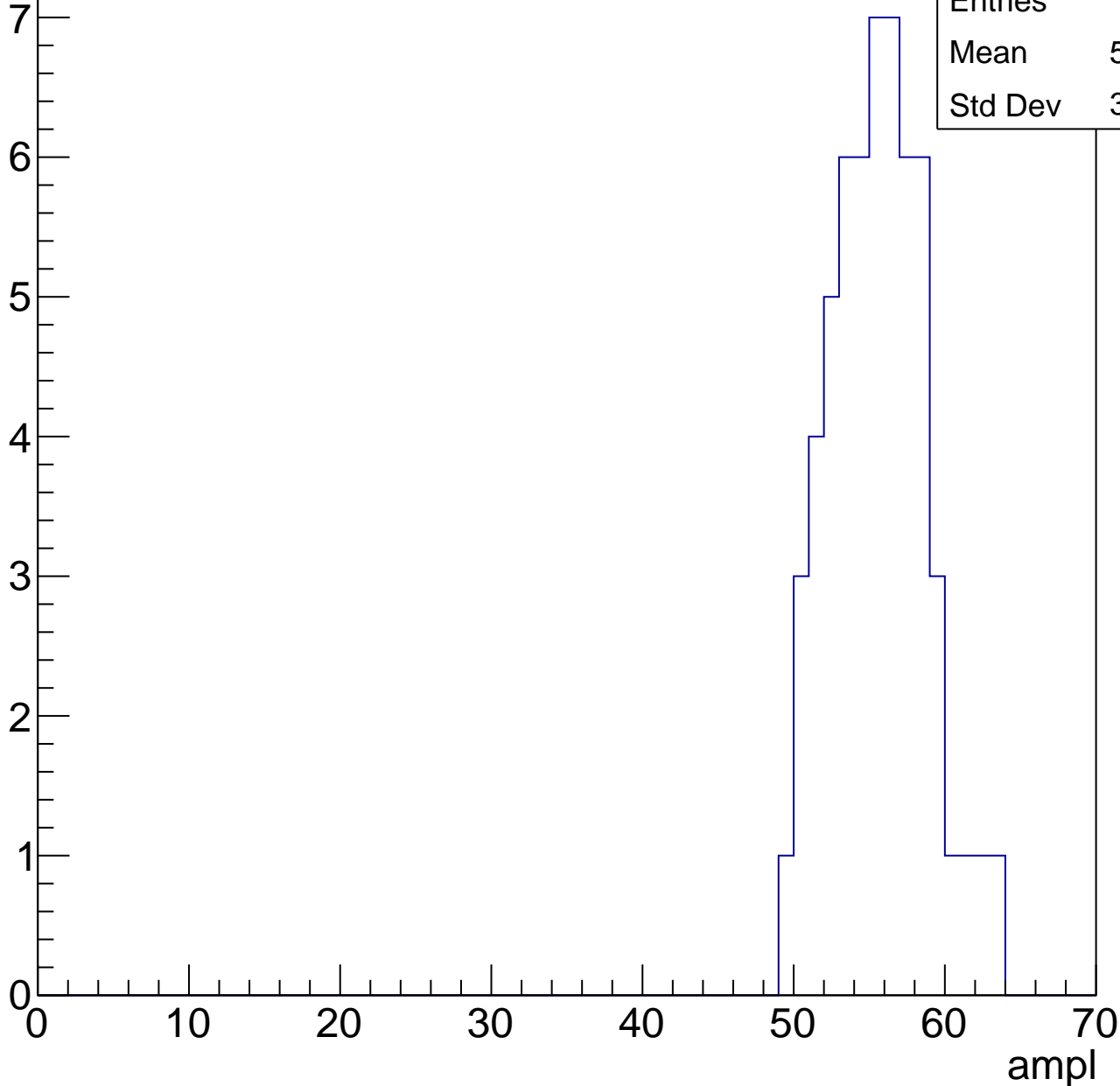


B1L103S, U5-ch55, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	55.09
Std Dev	3.098



B1L103S, U5-ch55, adc5

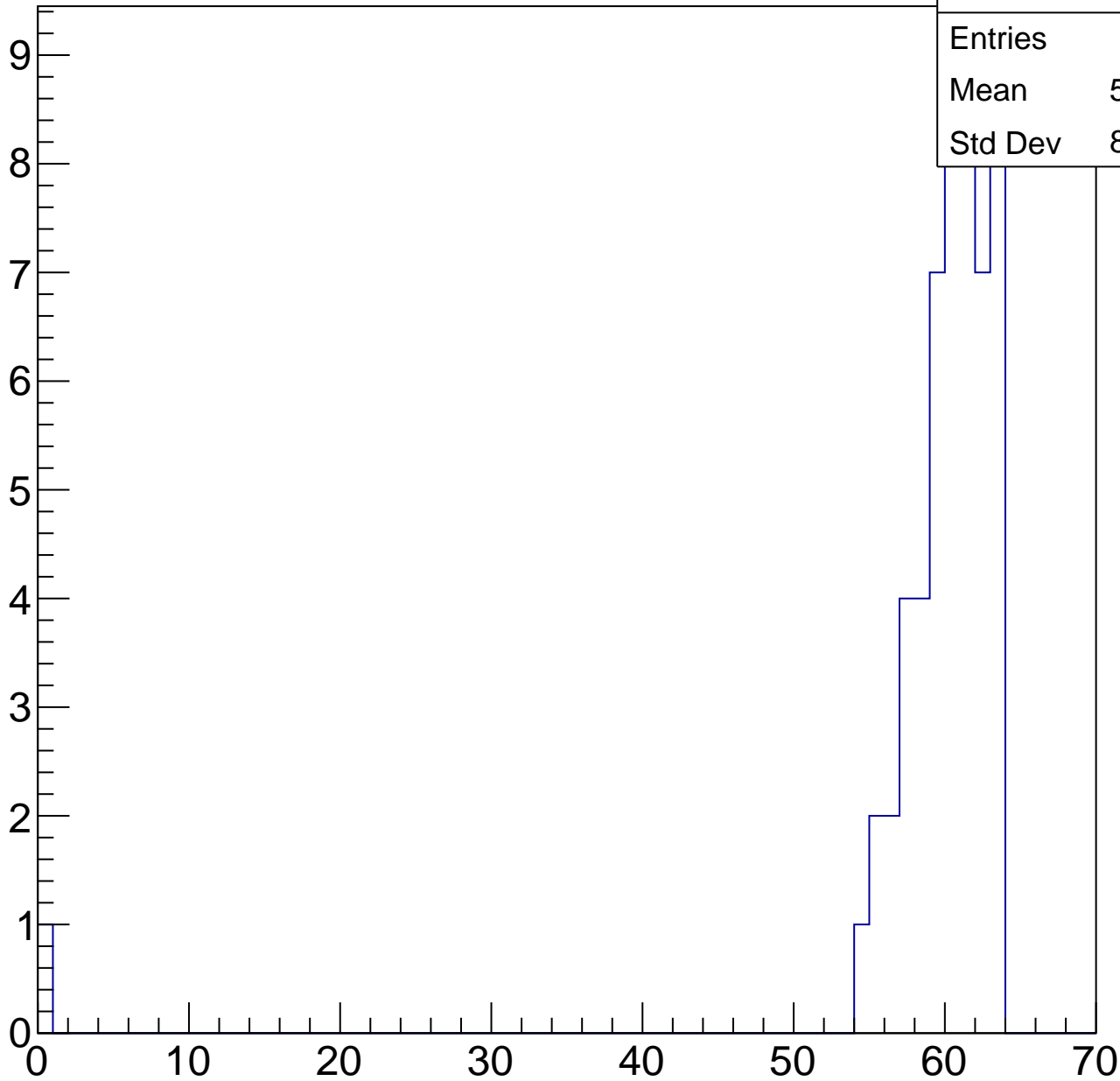
calib_packv5_041523_1651.root, FC#0, port C2

Entry

9
8
7
6
5
4
3
2
1
0

Entries	53
Mean	58.77
Std Dev	8.473

ampl



B1L103S, U5-ch55, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch55, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	19
Mean	0
Std Dev	0

B1L103S, U5-ch56, adc0

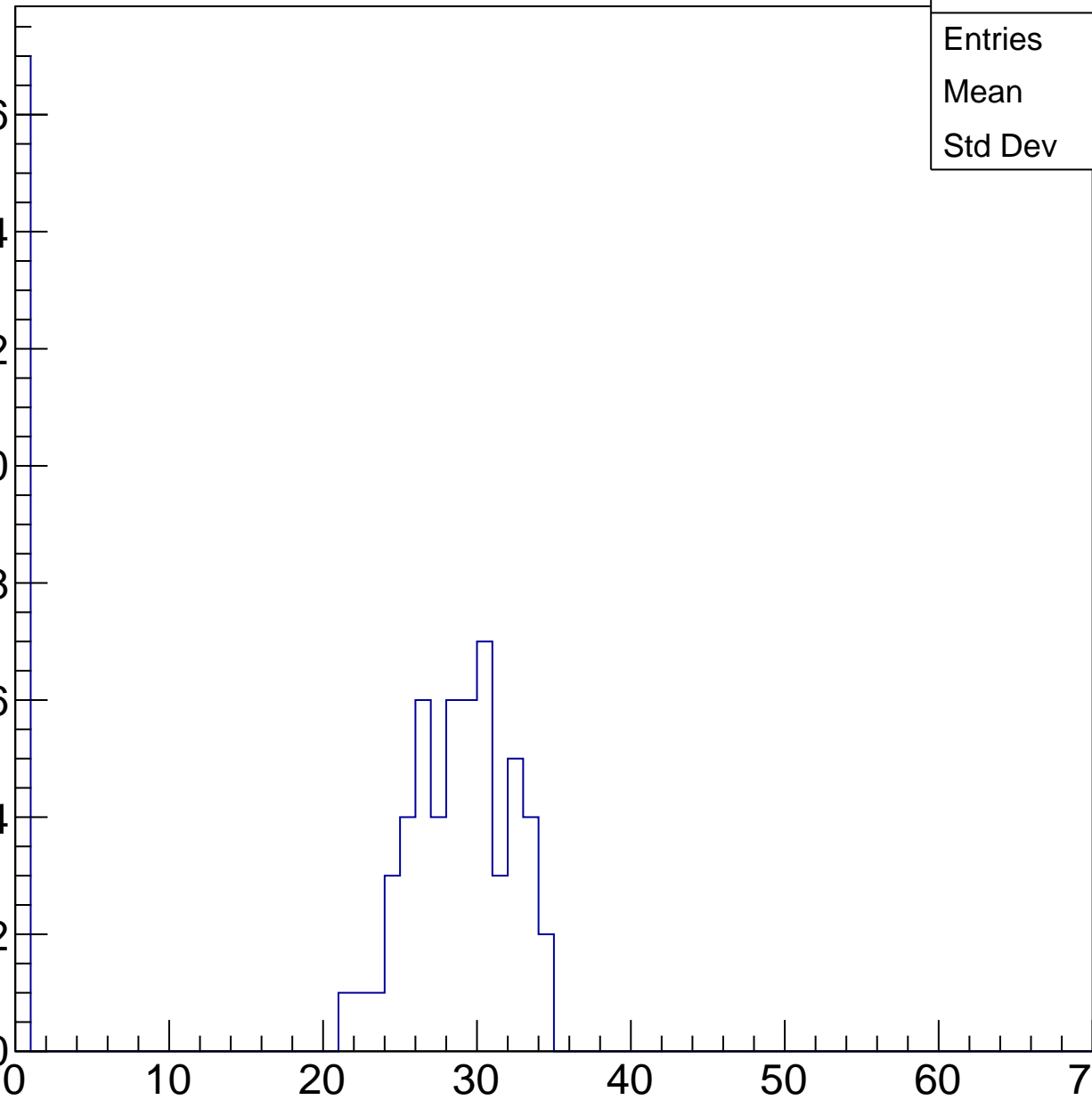
calib_packv5_041523_1651.root, FC#0, port C2

Entries	70
Mean	21.53
Std Dev	12.5

Entry

16
14
12
10
8
6
4
2
0

ampl

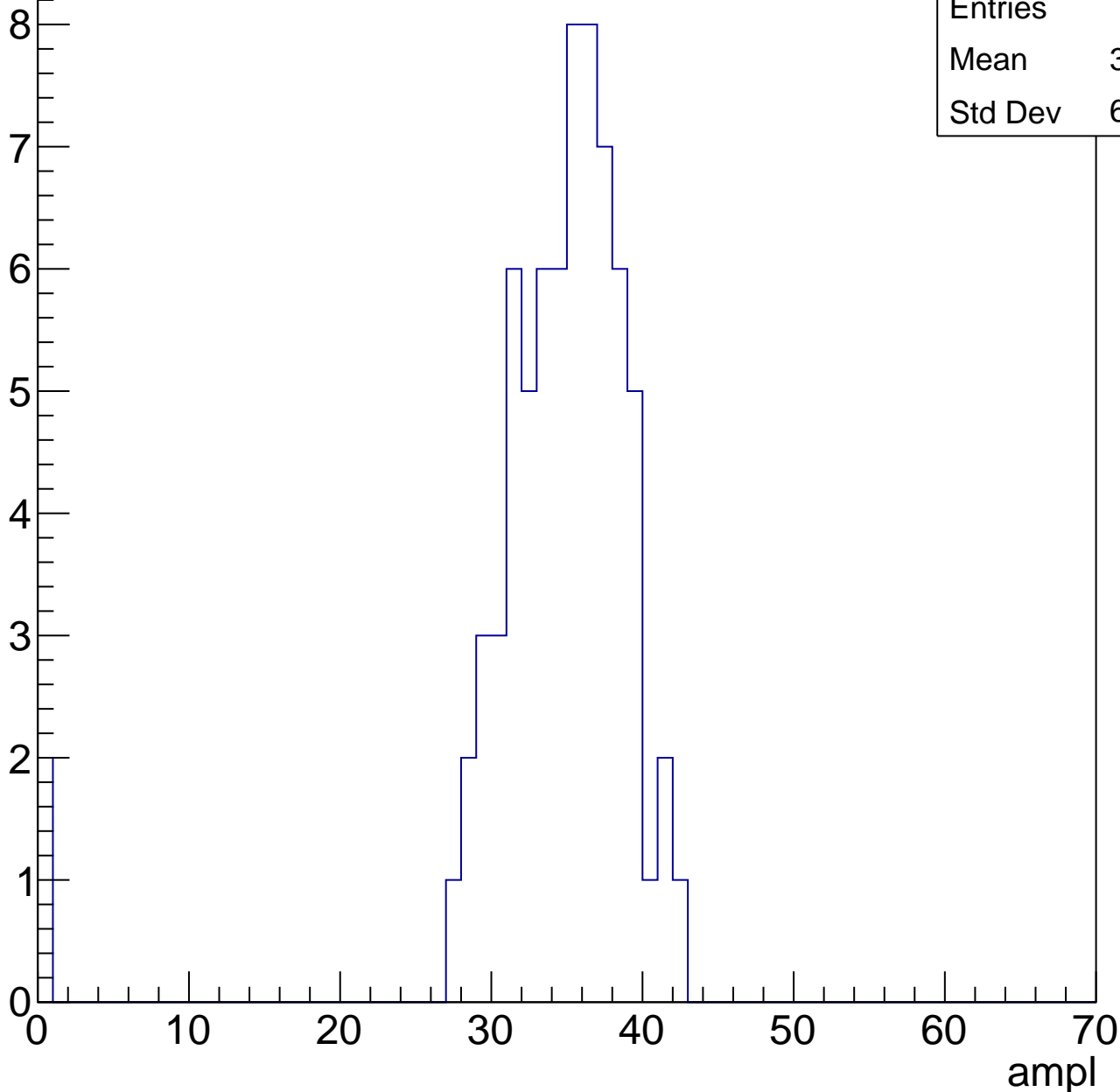


B1L103S, U5-ch56, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	33.64
Std Dev	6.613



B1L103S, U5-ch56, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	83
Mean	40.8
Std Dev	8.735

Entry

10

8

6

4

2

0

0

10

20

30

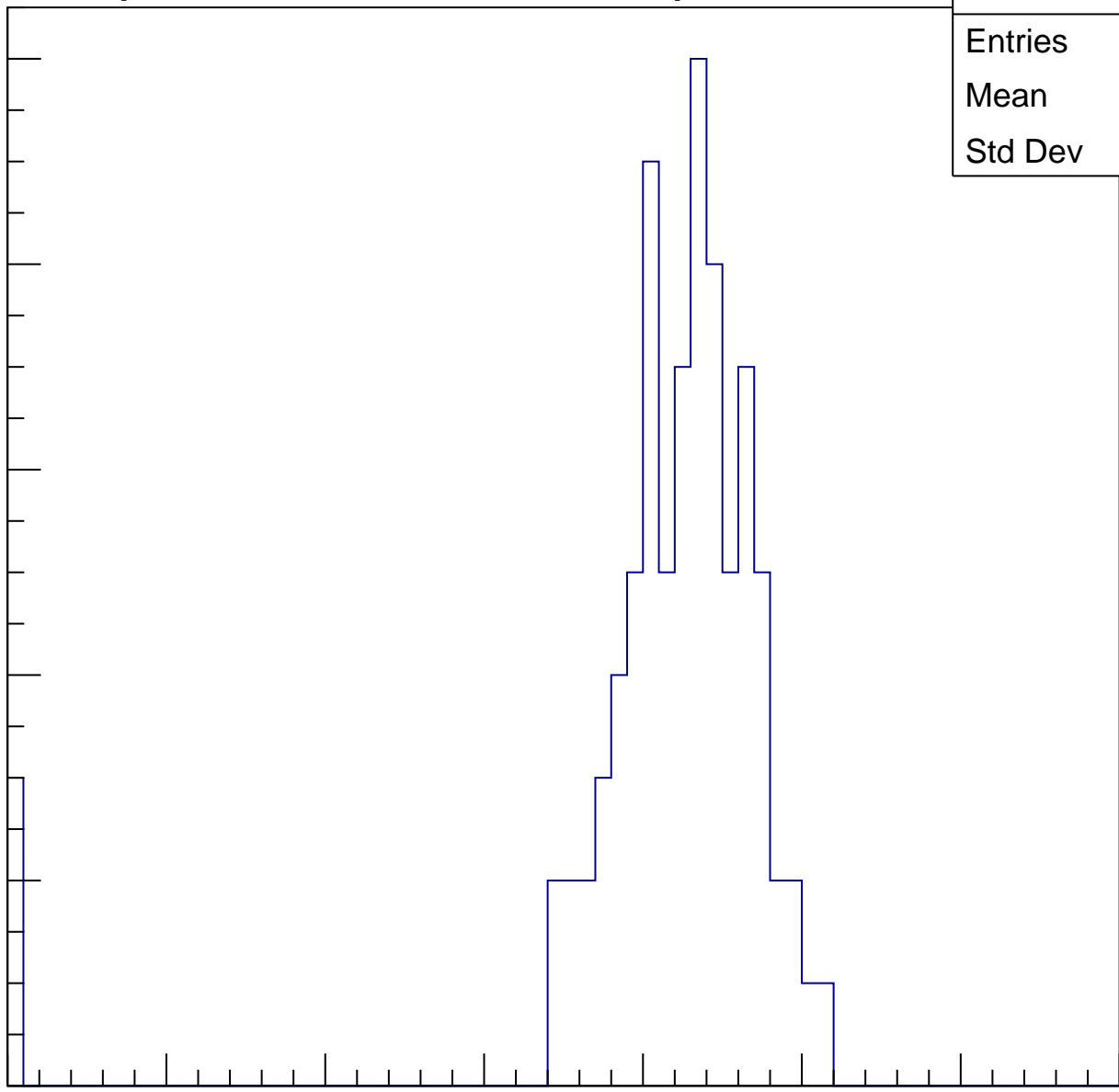
40

50

60

70

ampl



B1L103S, U5-ch56, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	53
Mean	37.75
Std Dev	19.54

Entry

10

8

6

4

2

0

0

10

20

30

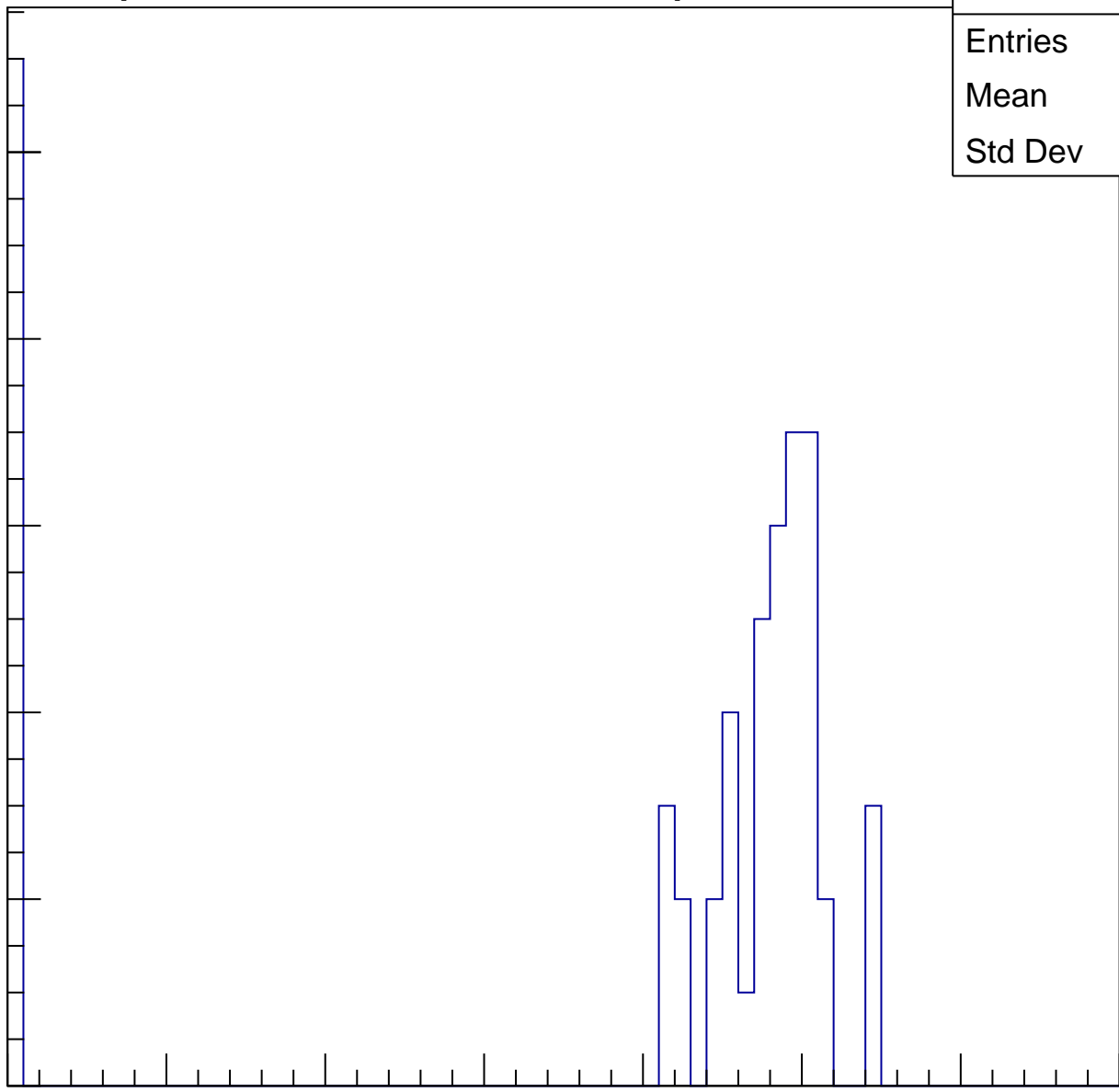
40

50

60

70

ampl

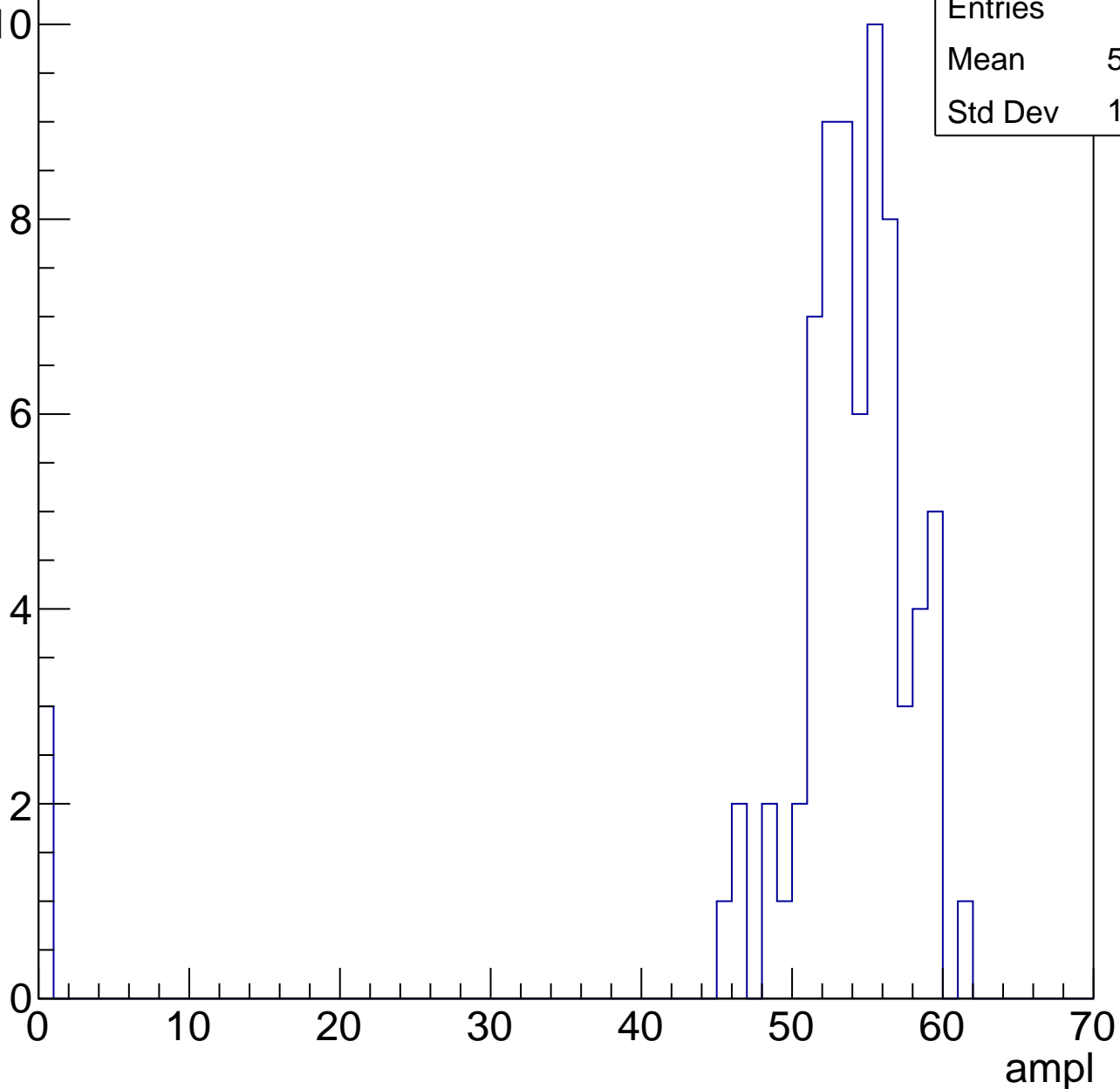


B1L103S, U5-ch56, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	51.58
Std Dev	11.15

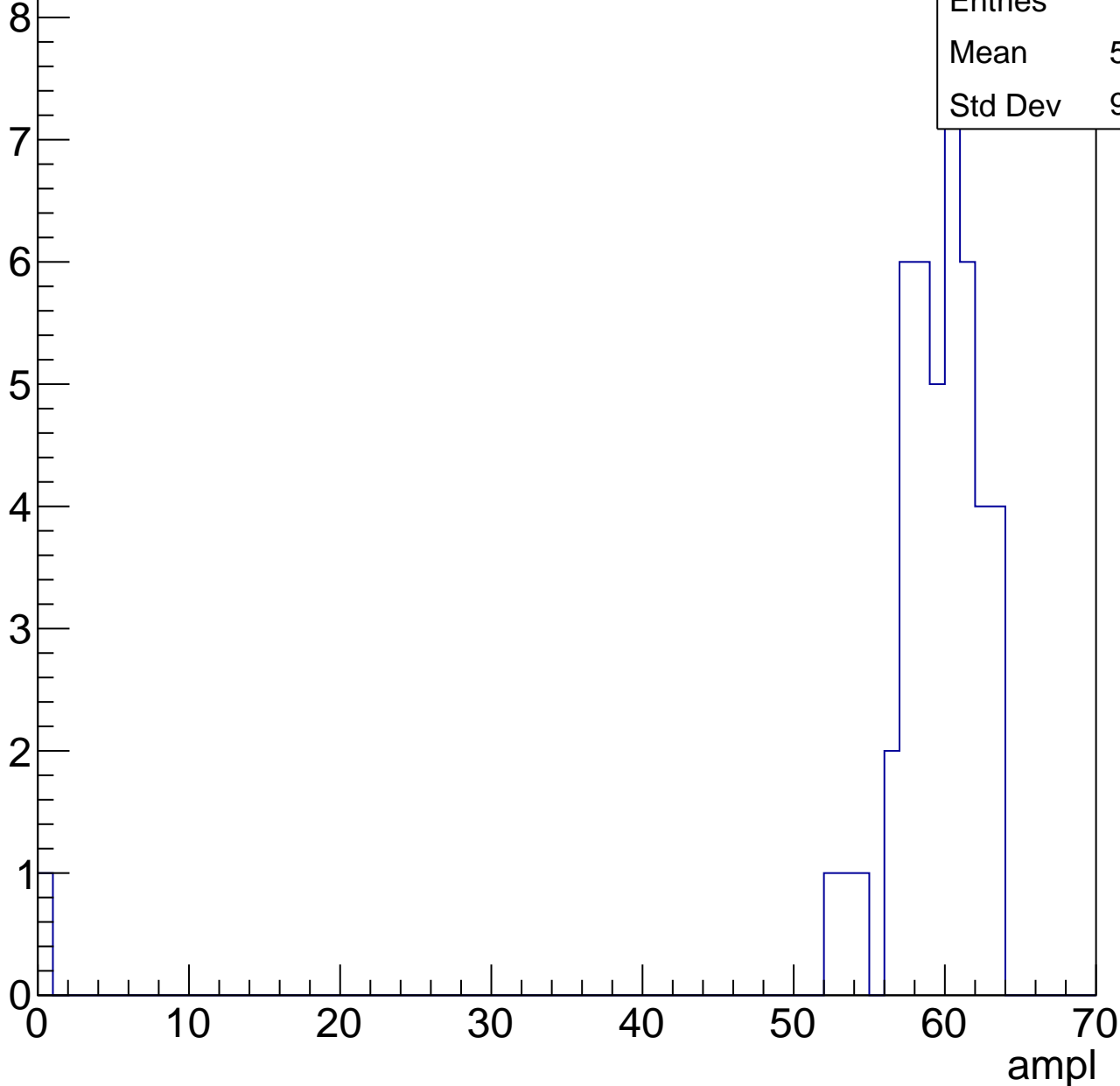


B1L103S, U5-ch56, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	45
Mean	57.82
Std Dev	9.078

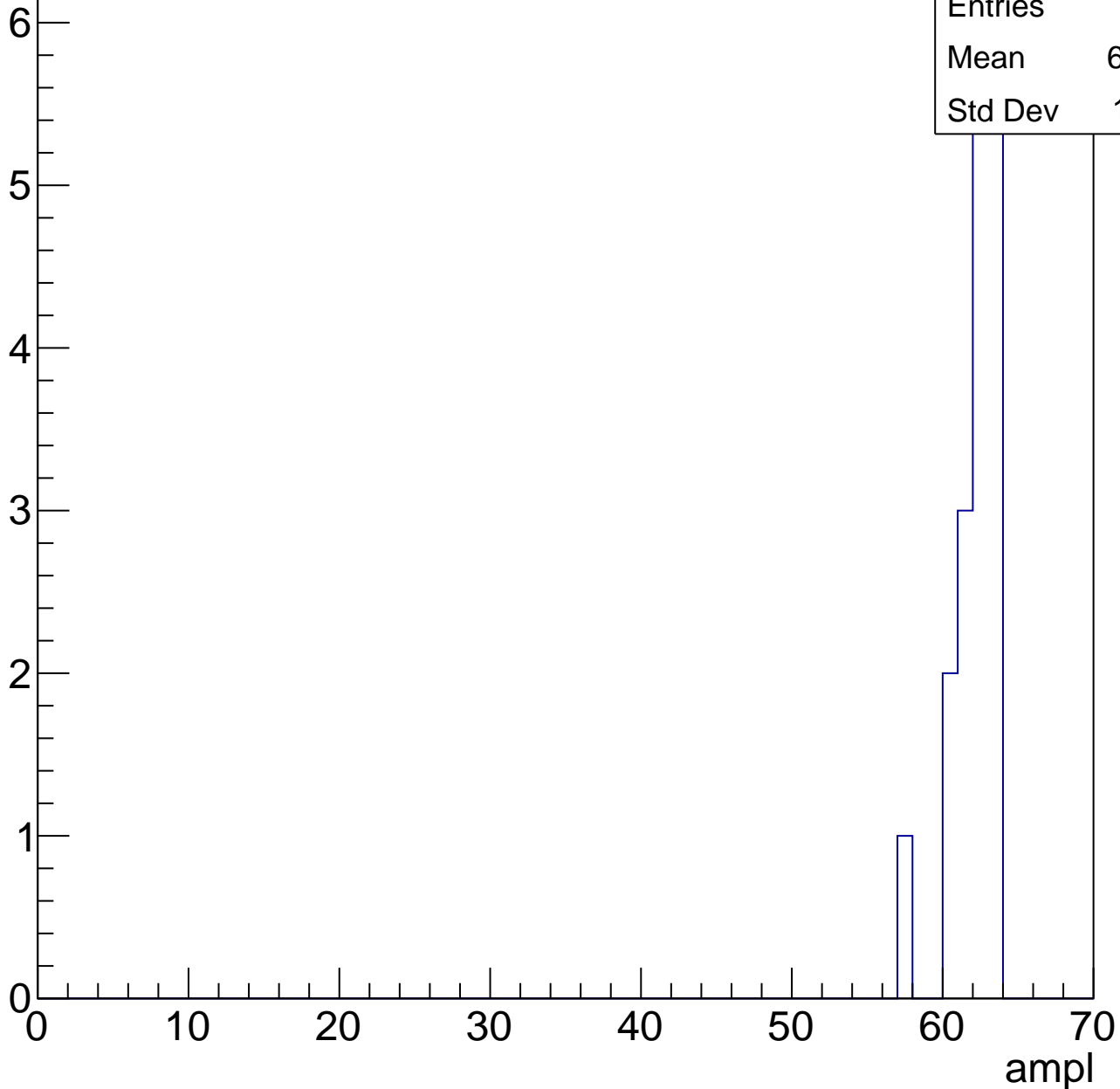


B1L103S, U5-ch56, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	18
Mean	61.67
Std Dev	1.491



B1L103S, U5-ch56, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

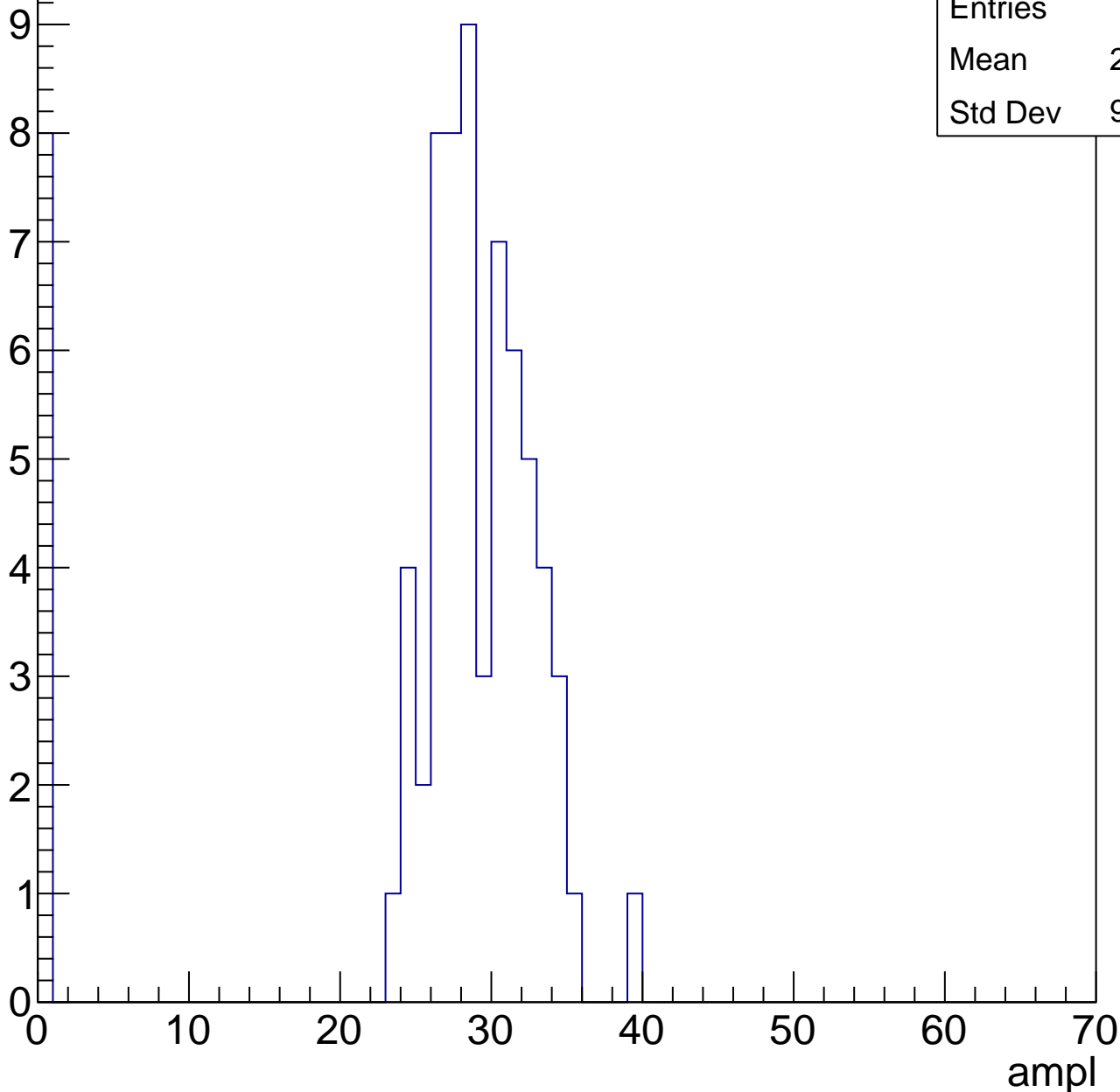


B1L103S, U5-ch57, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	25.66
Std Dev	9.694

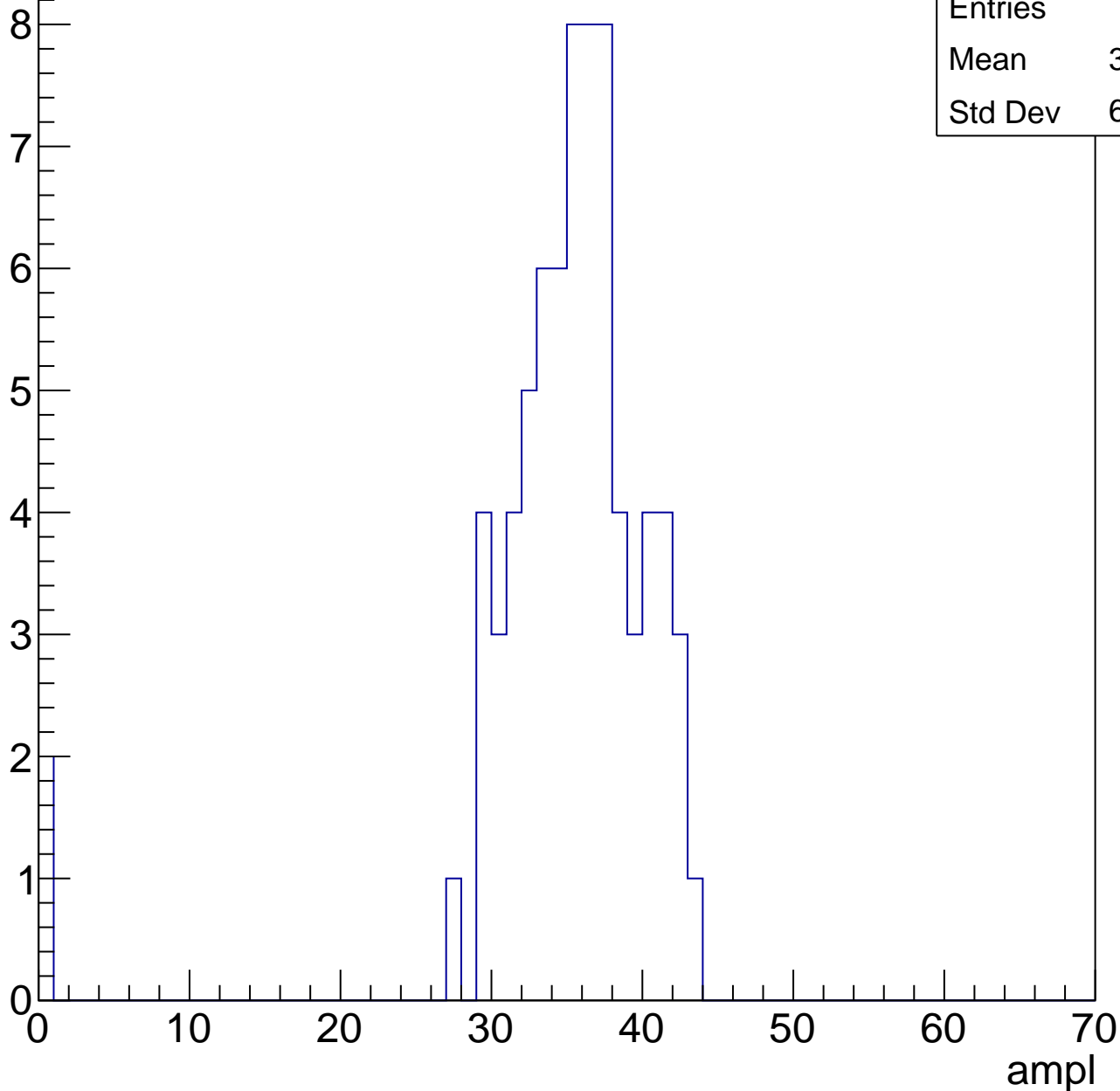


B1L103S, U5-ch57, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	34.39
Std Dev	6.802

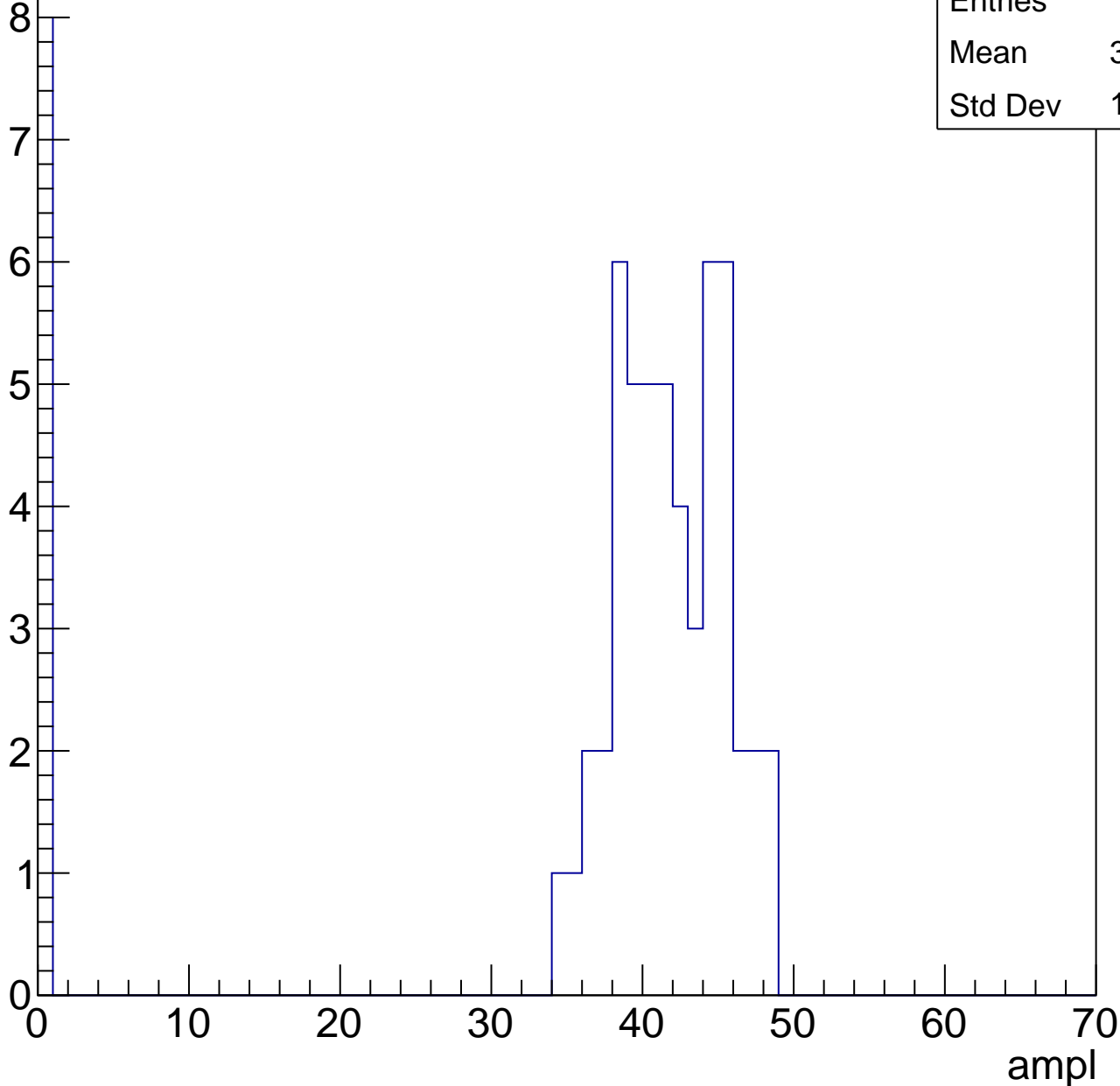


B1L103S, U5-ch57, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

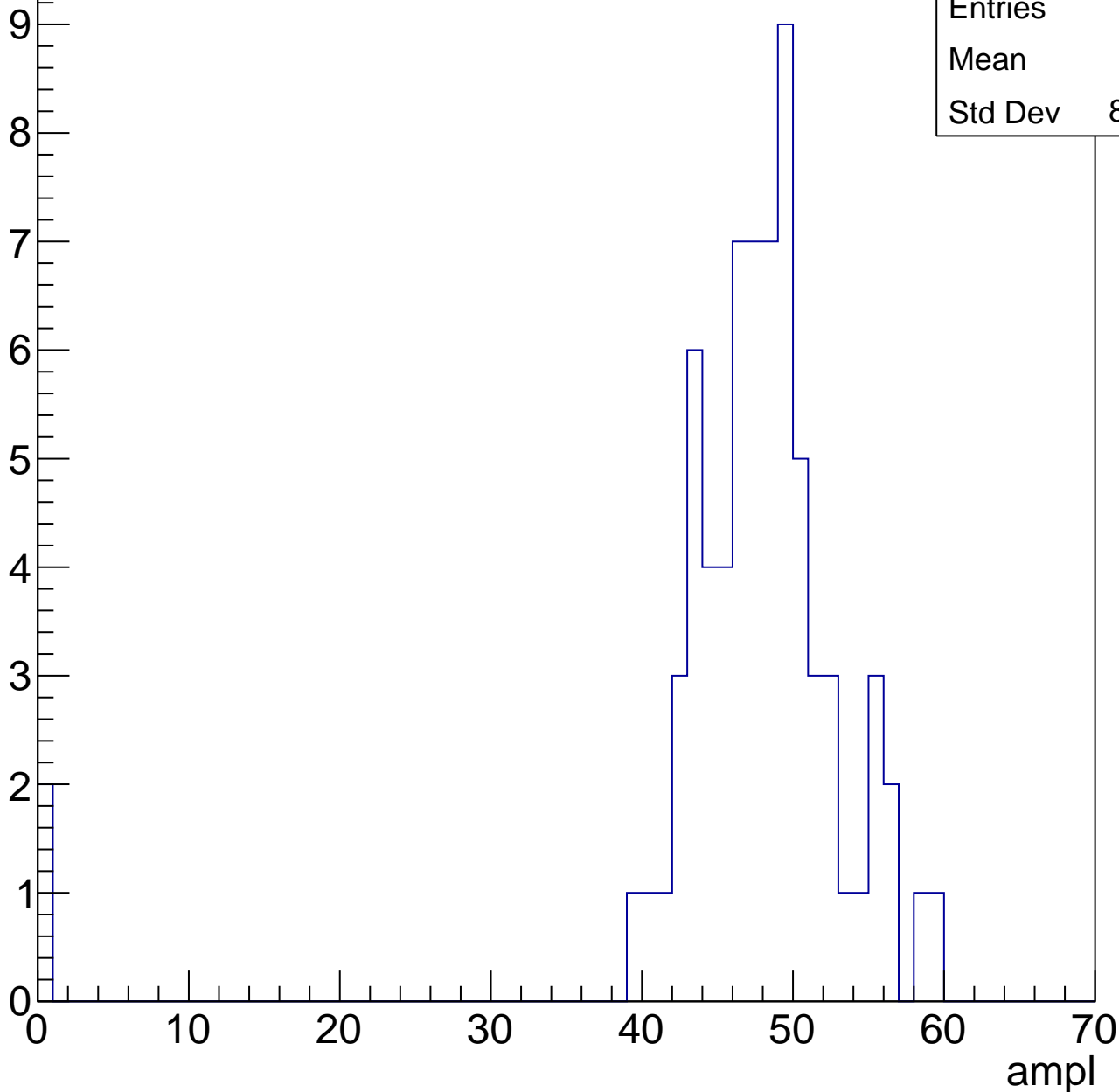
Entries	60
Mean	35.93
Std Dev	14.46



B1L103S, U5-ch57, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

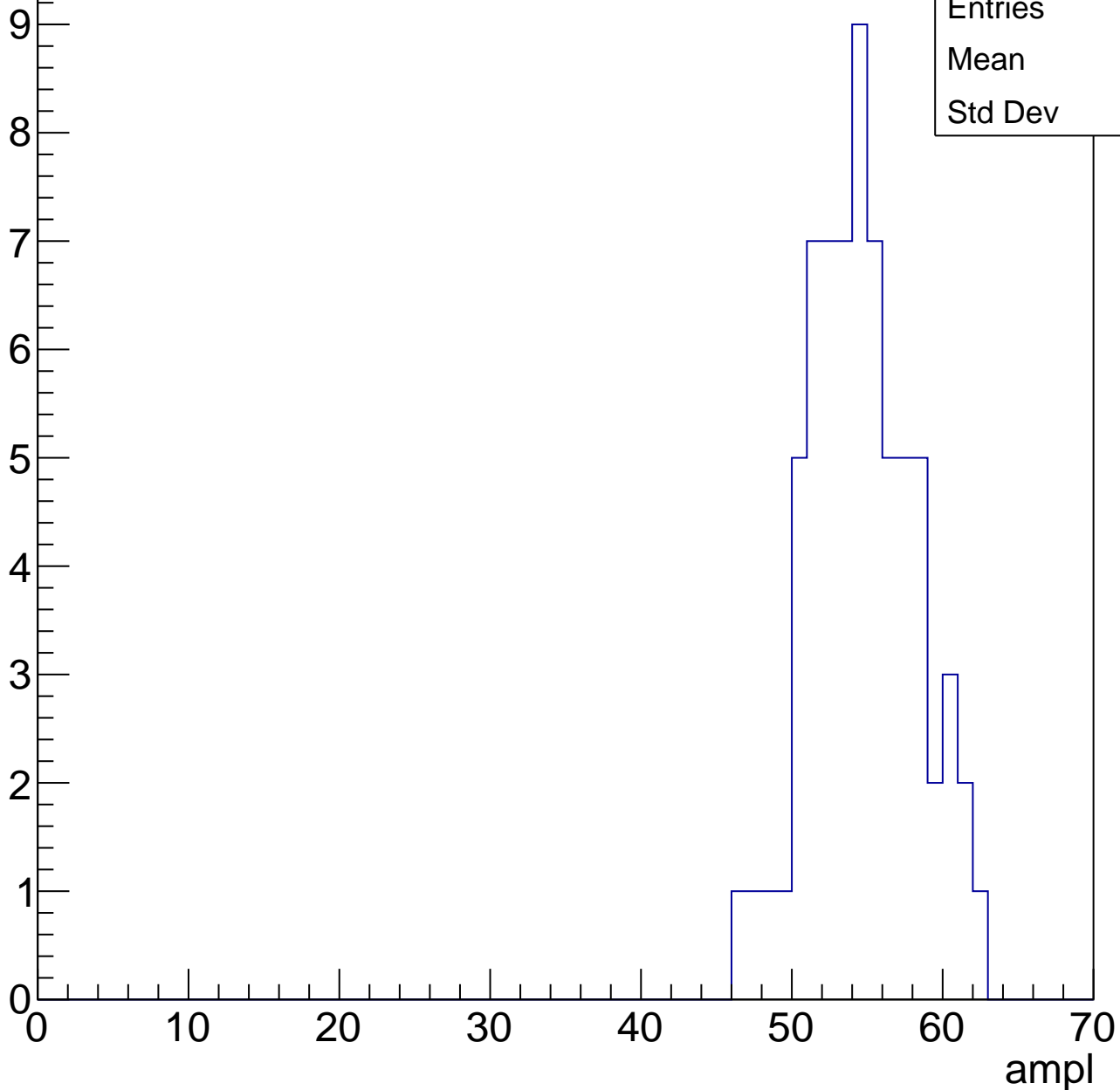


B1L103S, U5-ch57, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	54.2
Std Dev	3.45

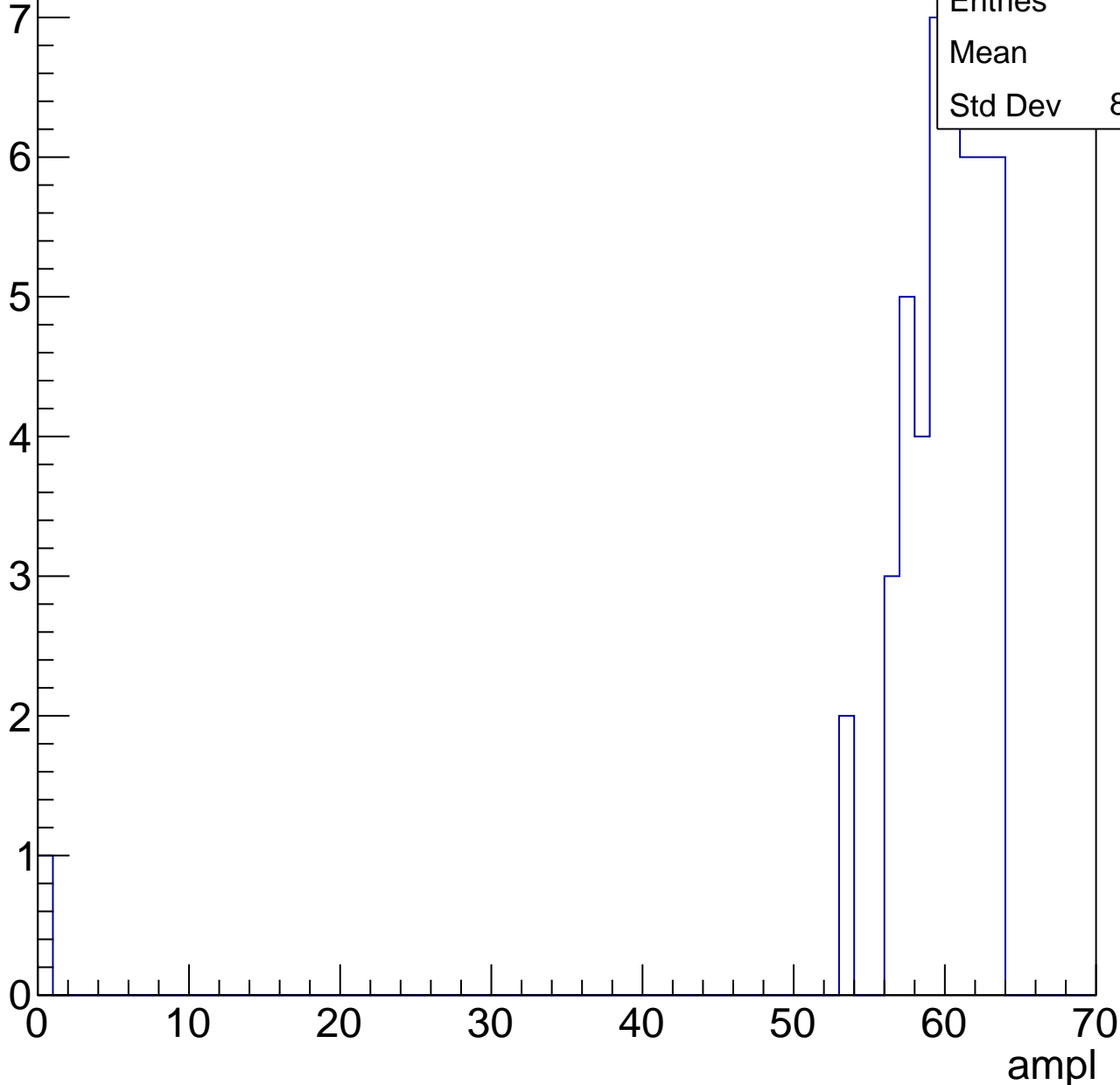


B1L103S, U5-ch57, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

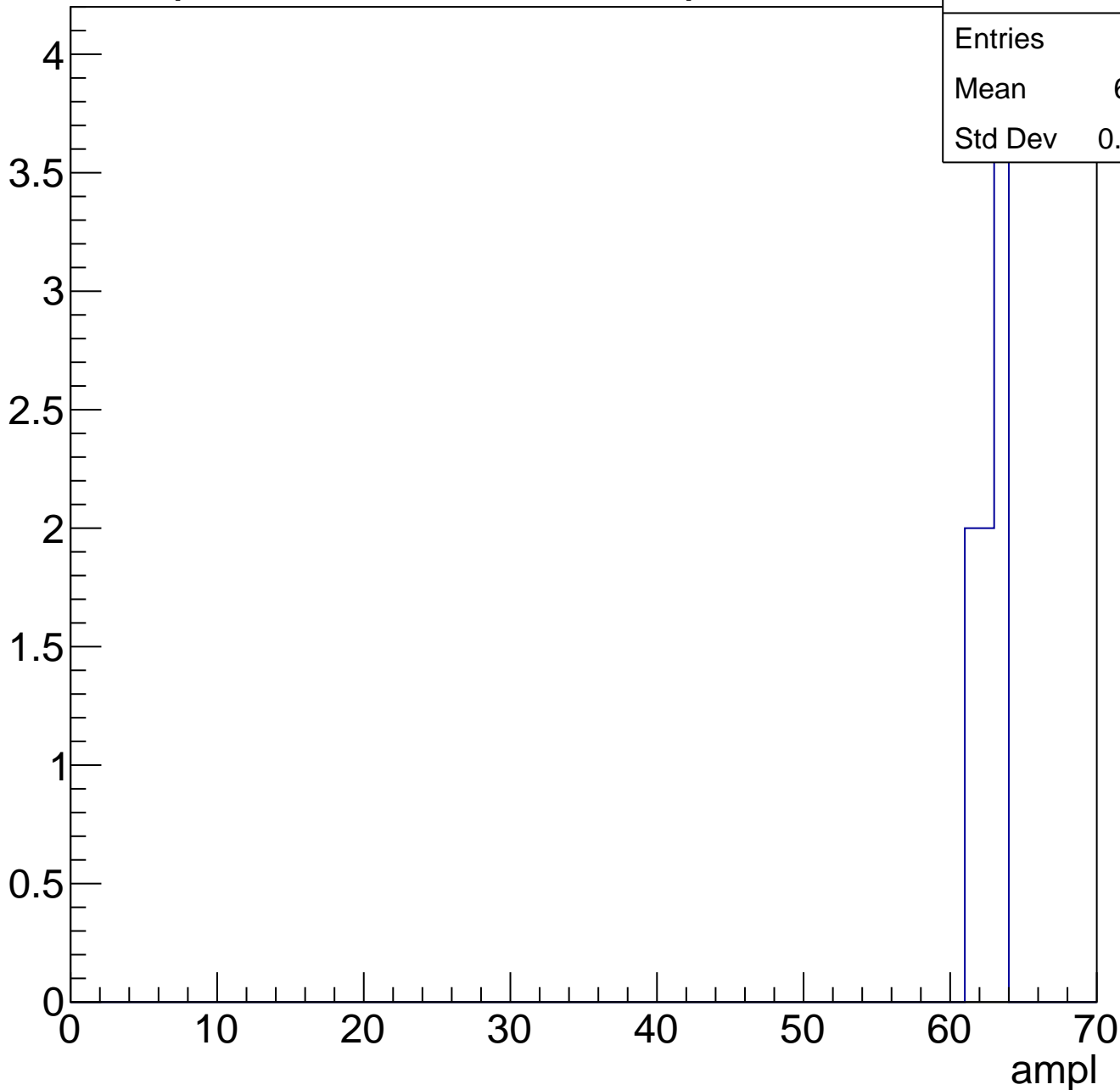
Entries	47
Mean	58.3
Std Dev	8.946



B1L103S, U5-ch57, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

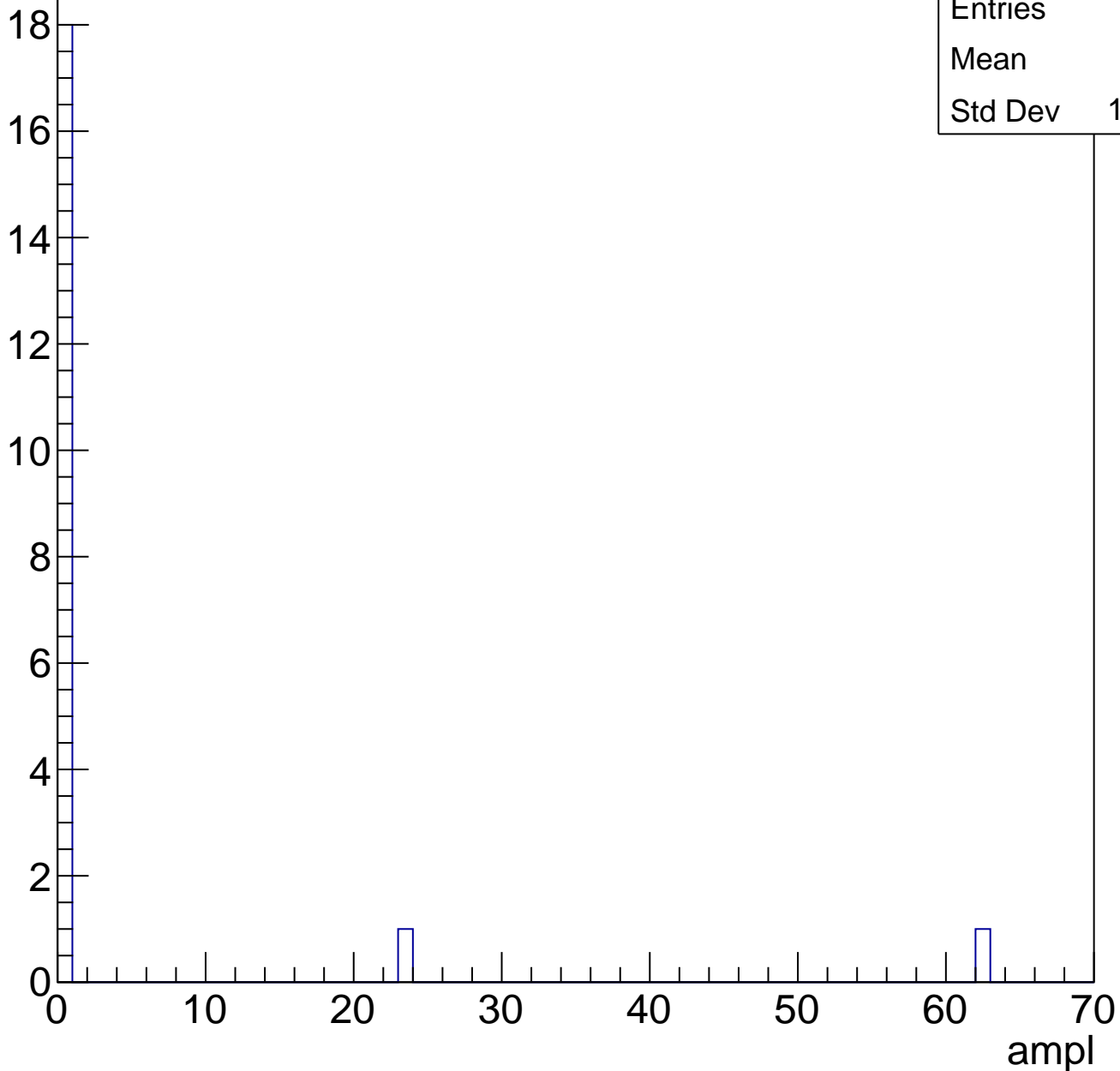


B1L103S, U5-ch57, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	4.25
Std Dev	14.16

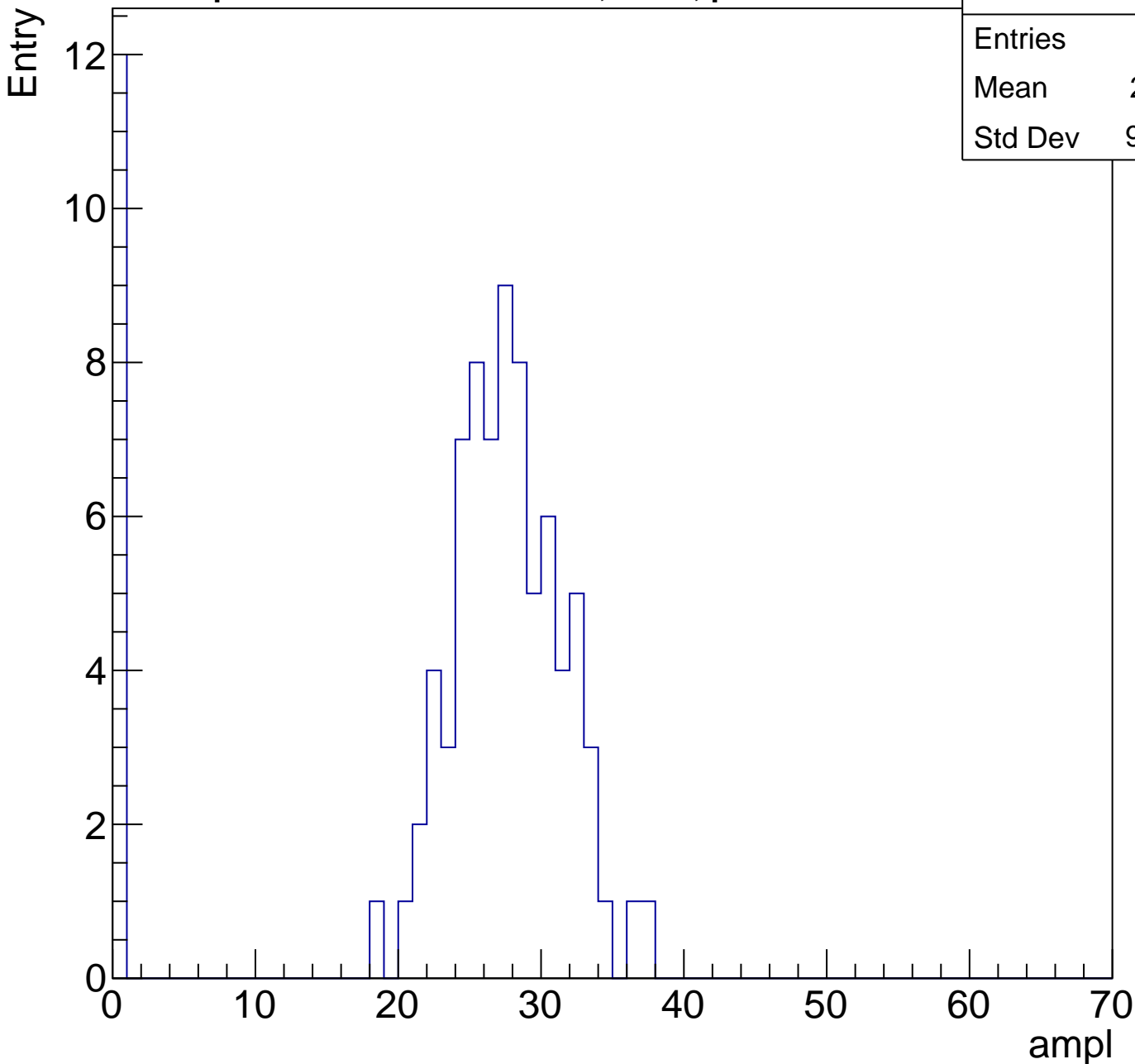
Entry



B1L103S, U5-ch58, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	88
Mean	23.51
Std Dev	9.965

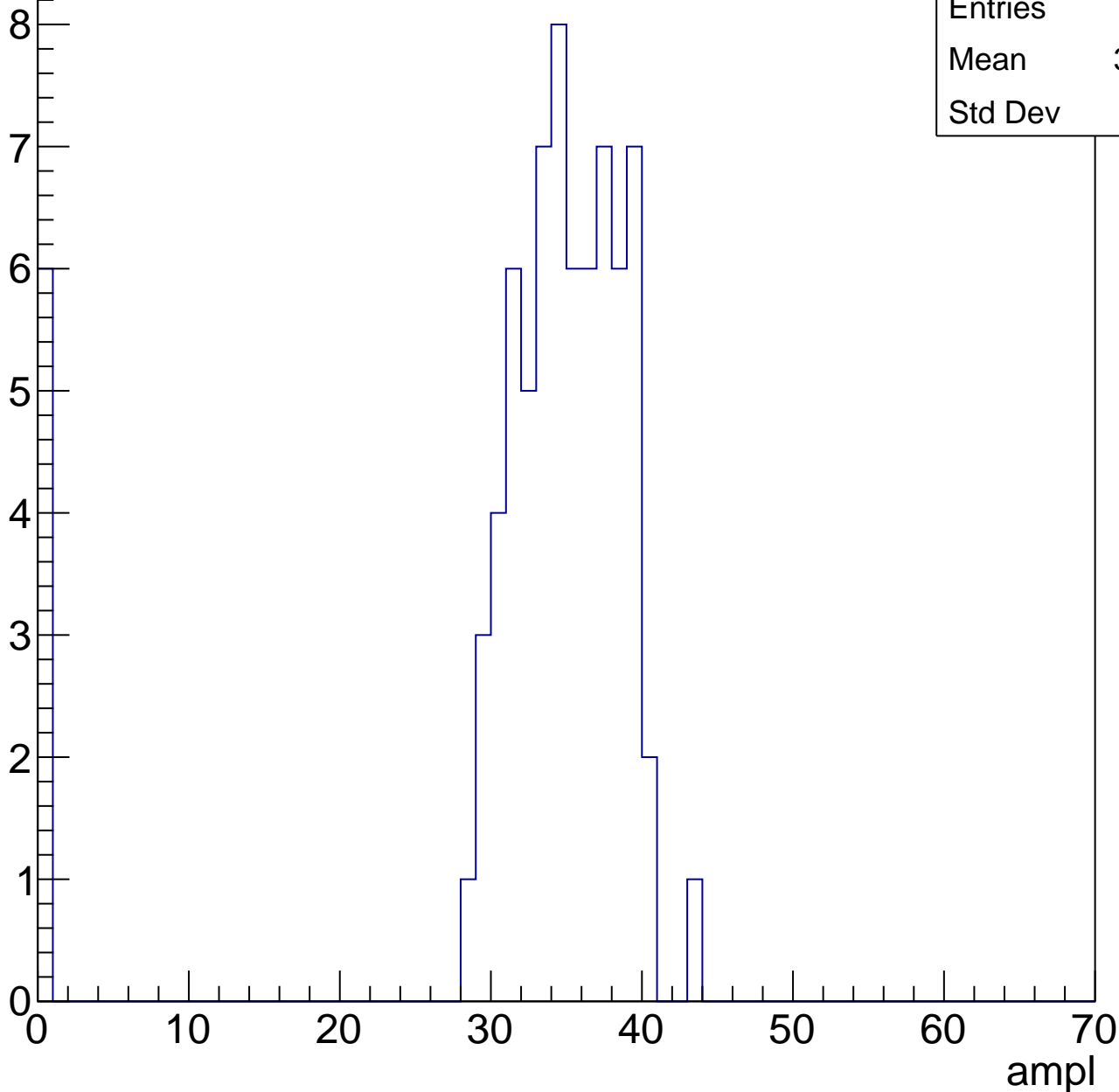


B1L103S, U5-ch58, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	31.91
Std Dev	9.92

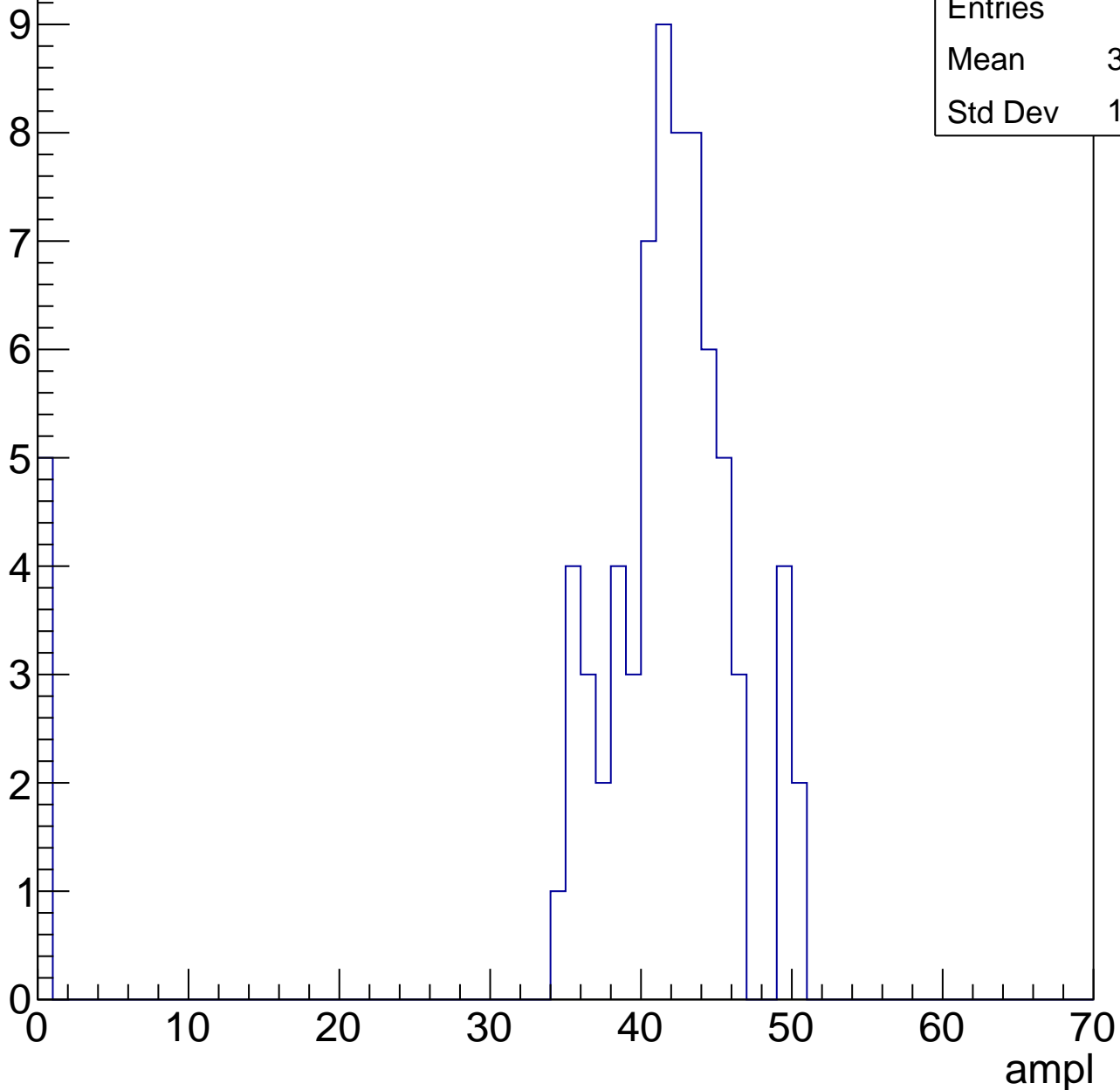


B1L103S, U5-ch58, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	38.88
Std Dev	11.09

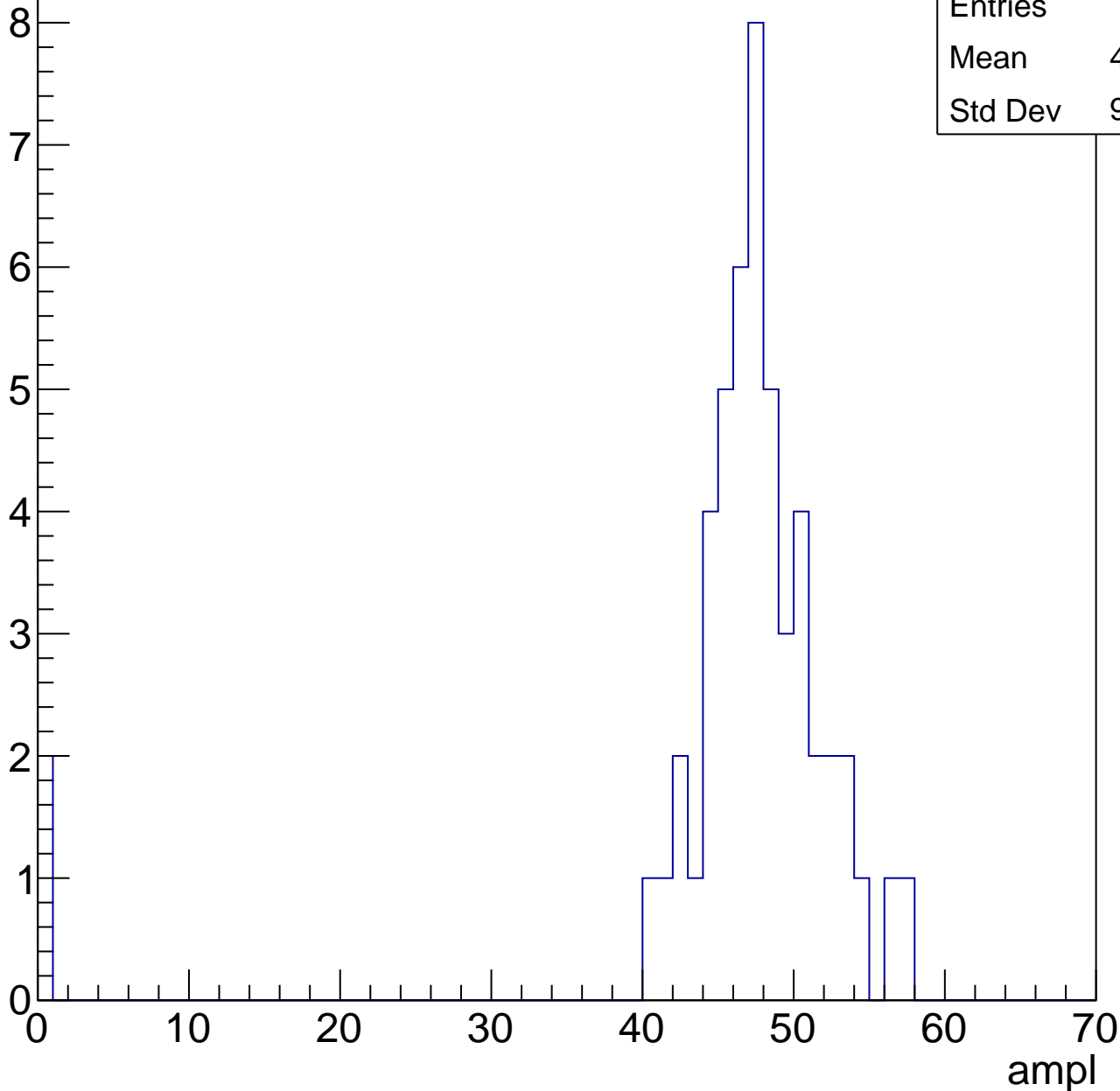


B1L103S, U5-ch58, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	45.63
Std Dev	9.874

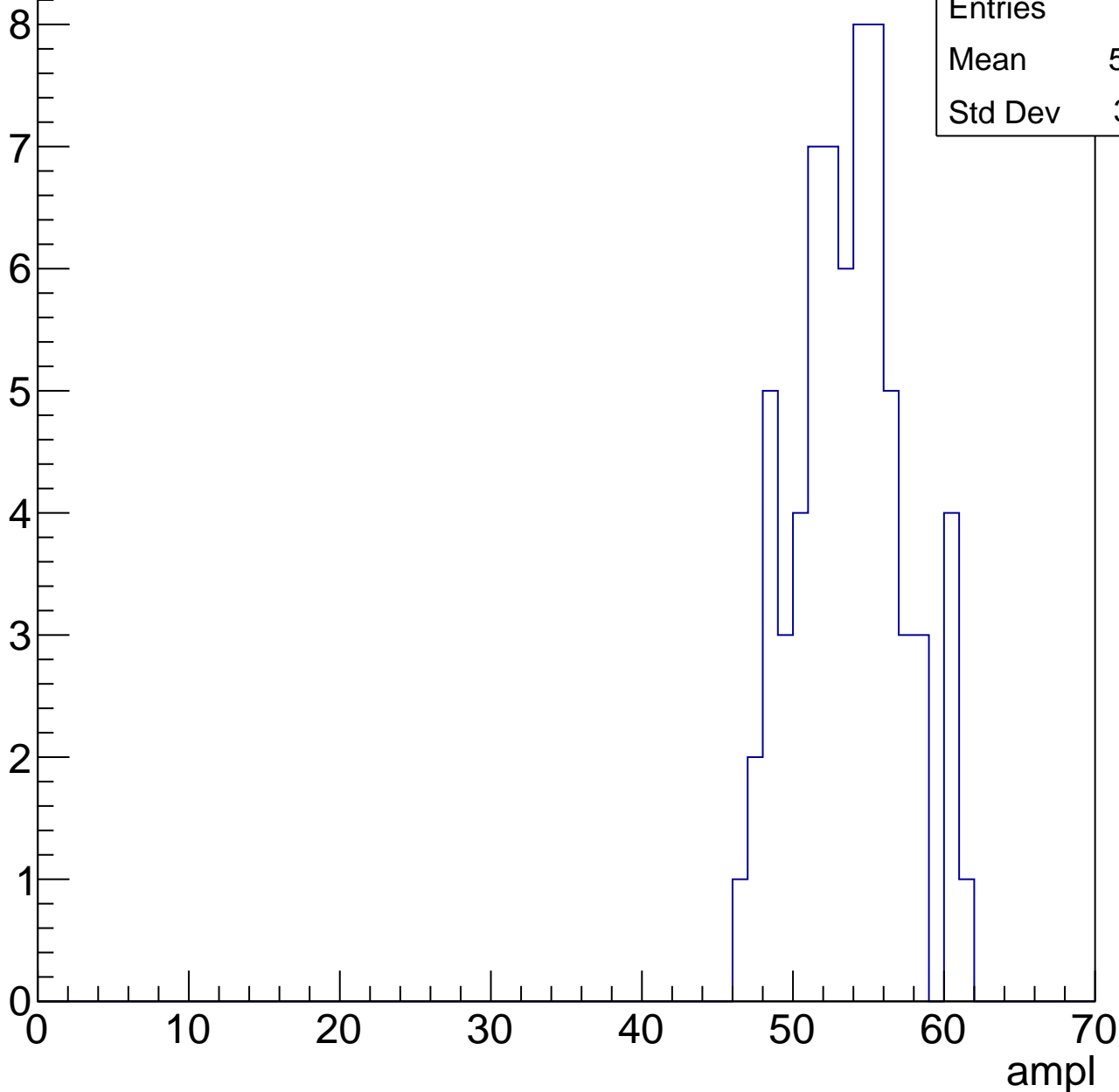


B1L103S, U5-ch58, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	53.19
Std Dev	3.521

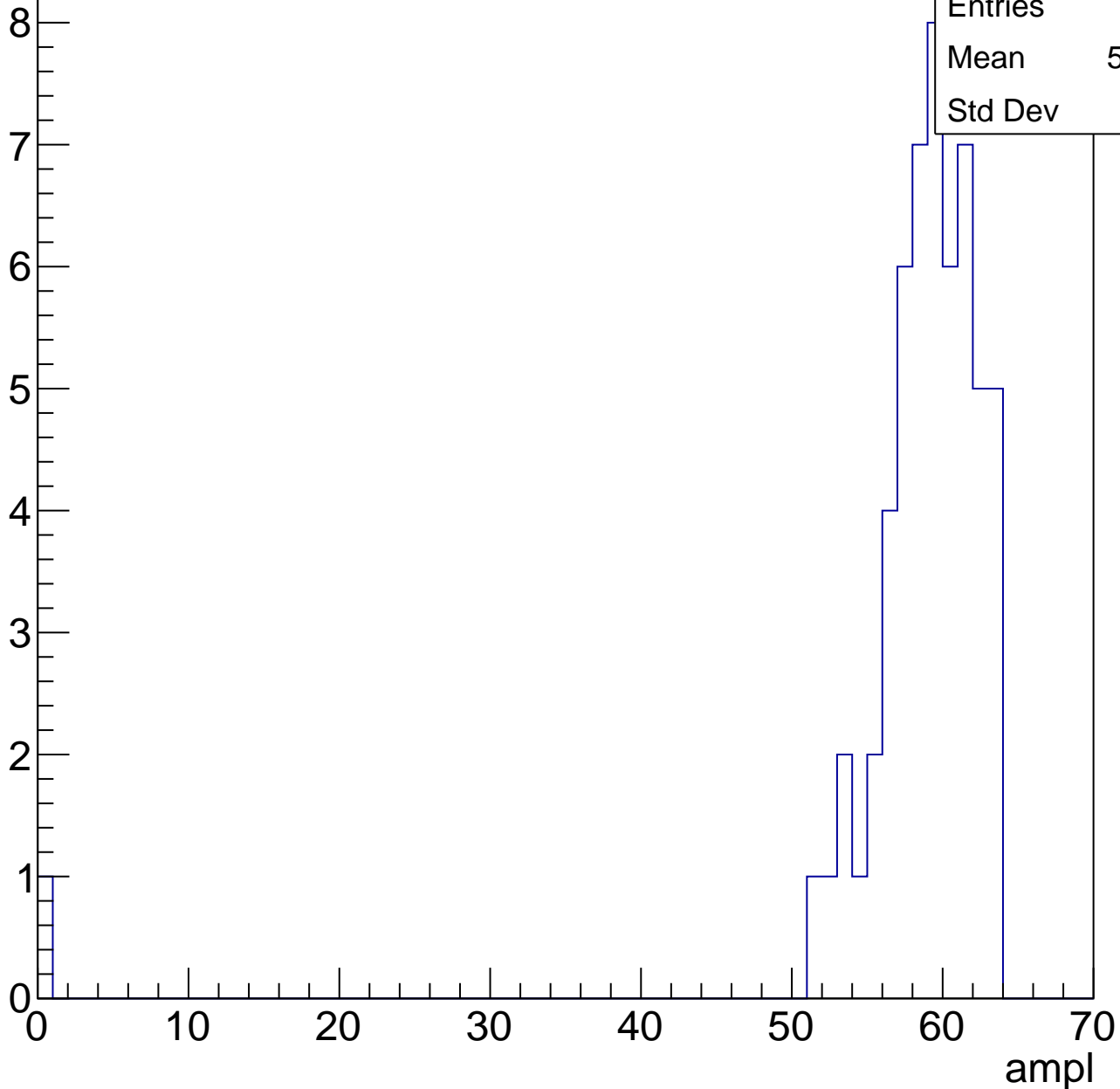


B1L103S, U5-ch58, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	57.66
Std Dev	8.29

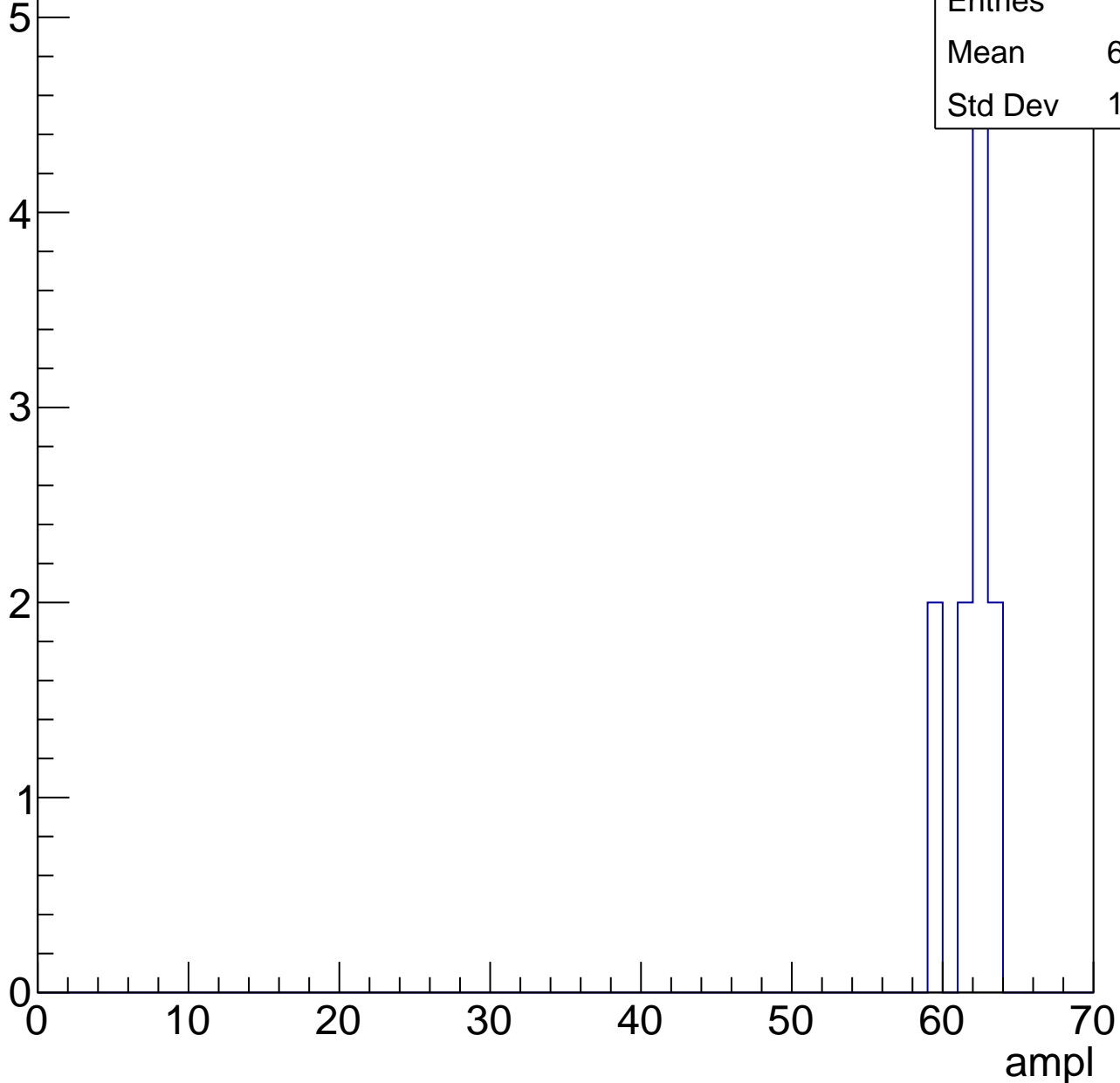


B1L103S, U5-ch58, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	11
Mean	61.45
Std Dev	1.305

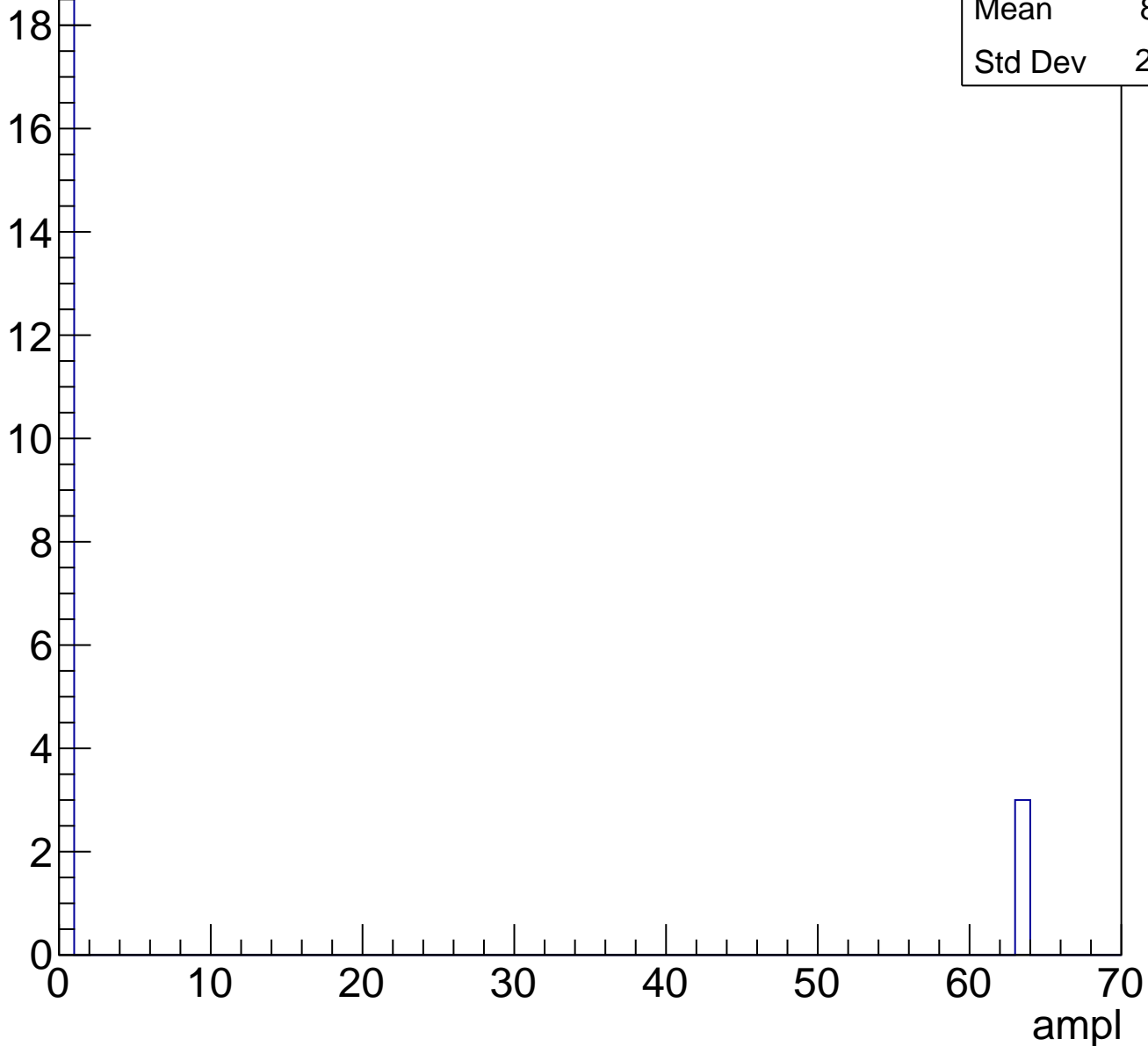


B1L103S, U5-ch58, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	22
Mean	8.591
Std Dev	21.62

Entry

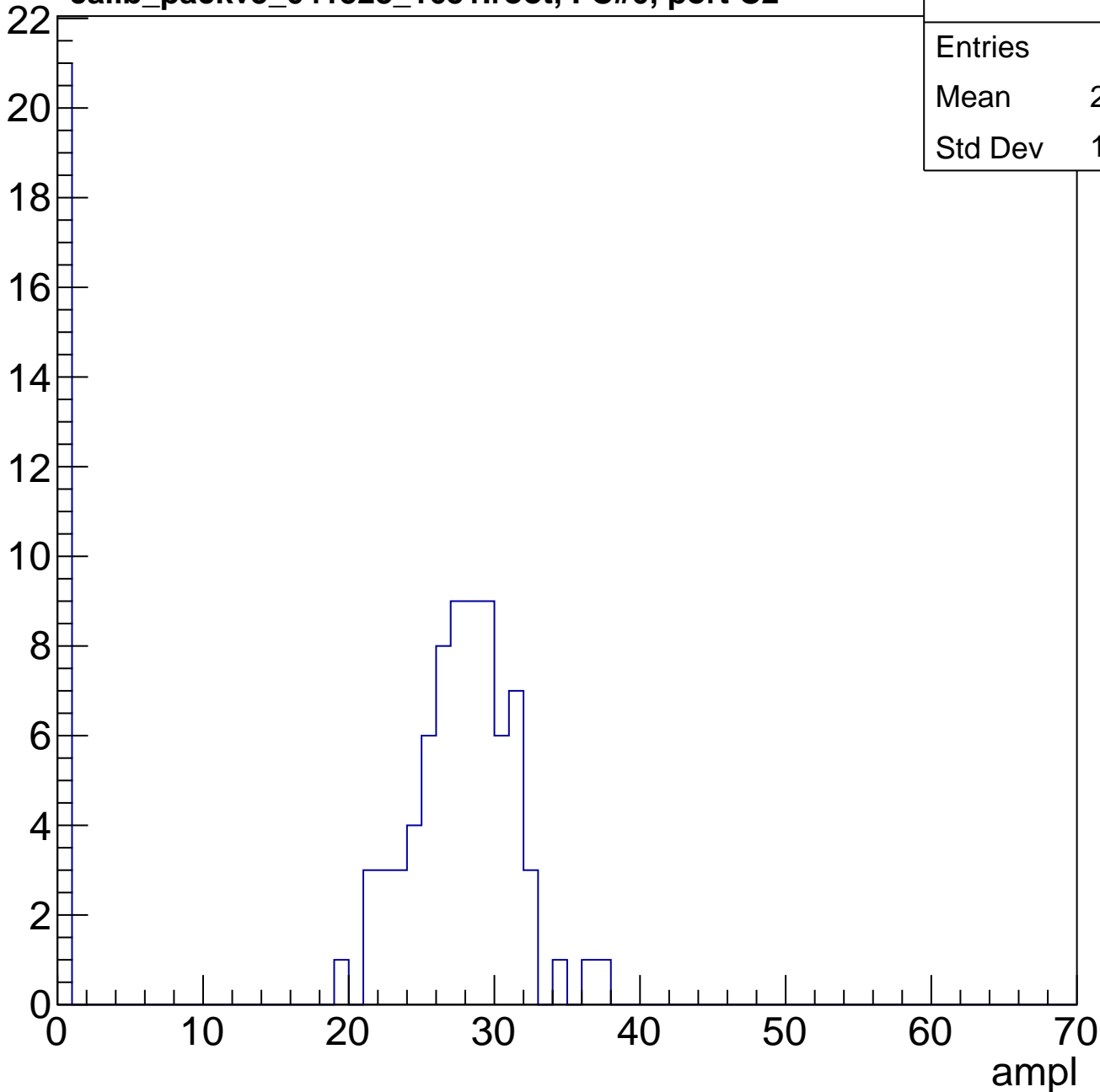


B1L103S, U5-ch59, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	95
Mean	21.34
Std Dev	11.76

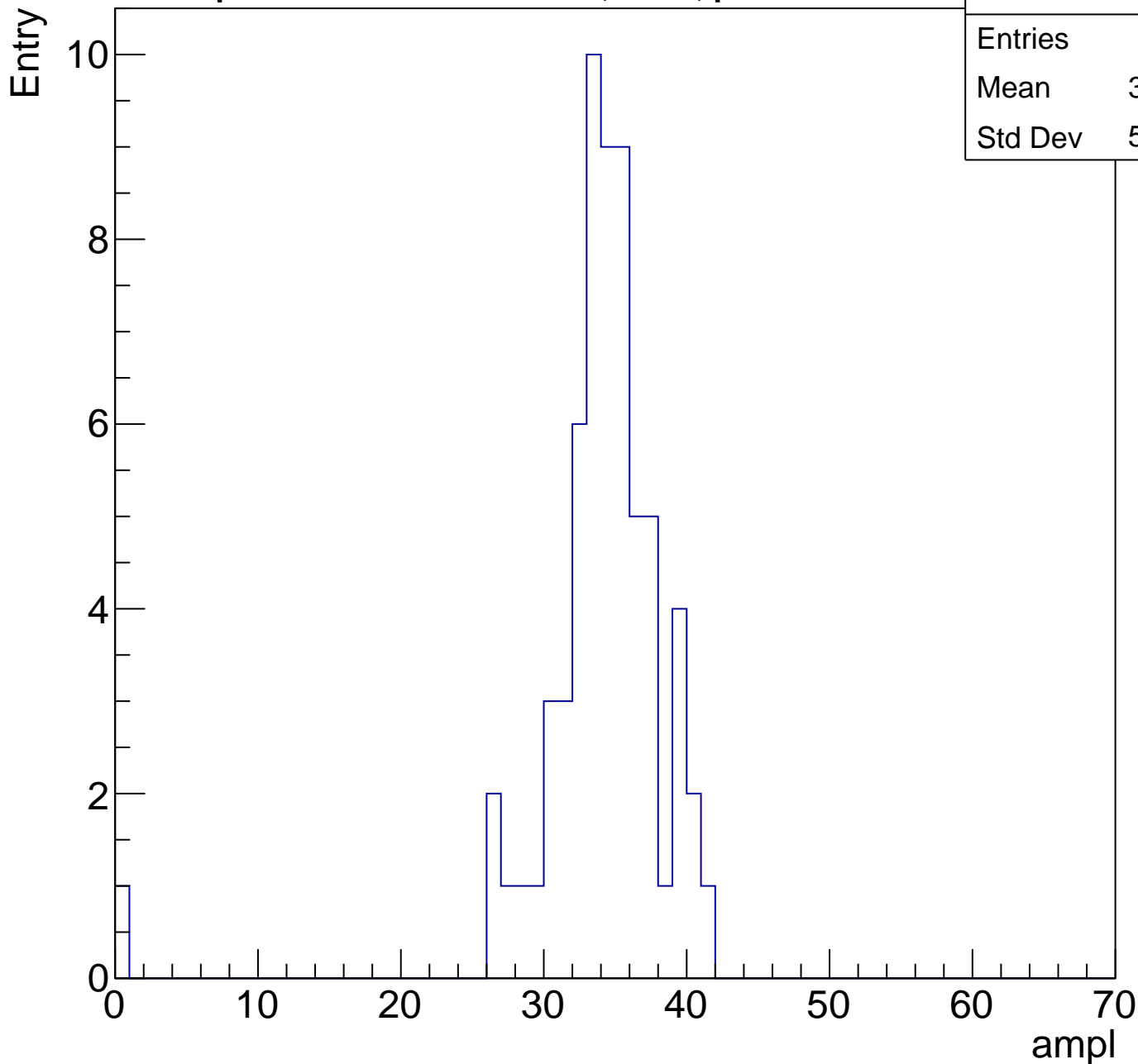
Entry



B1L103S, U5-ch59, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	64
Mean	33.47
Std Dev	5.297

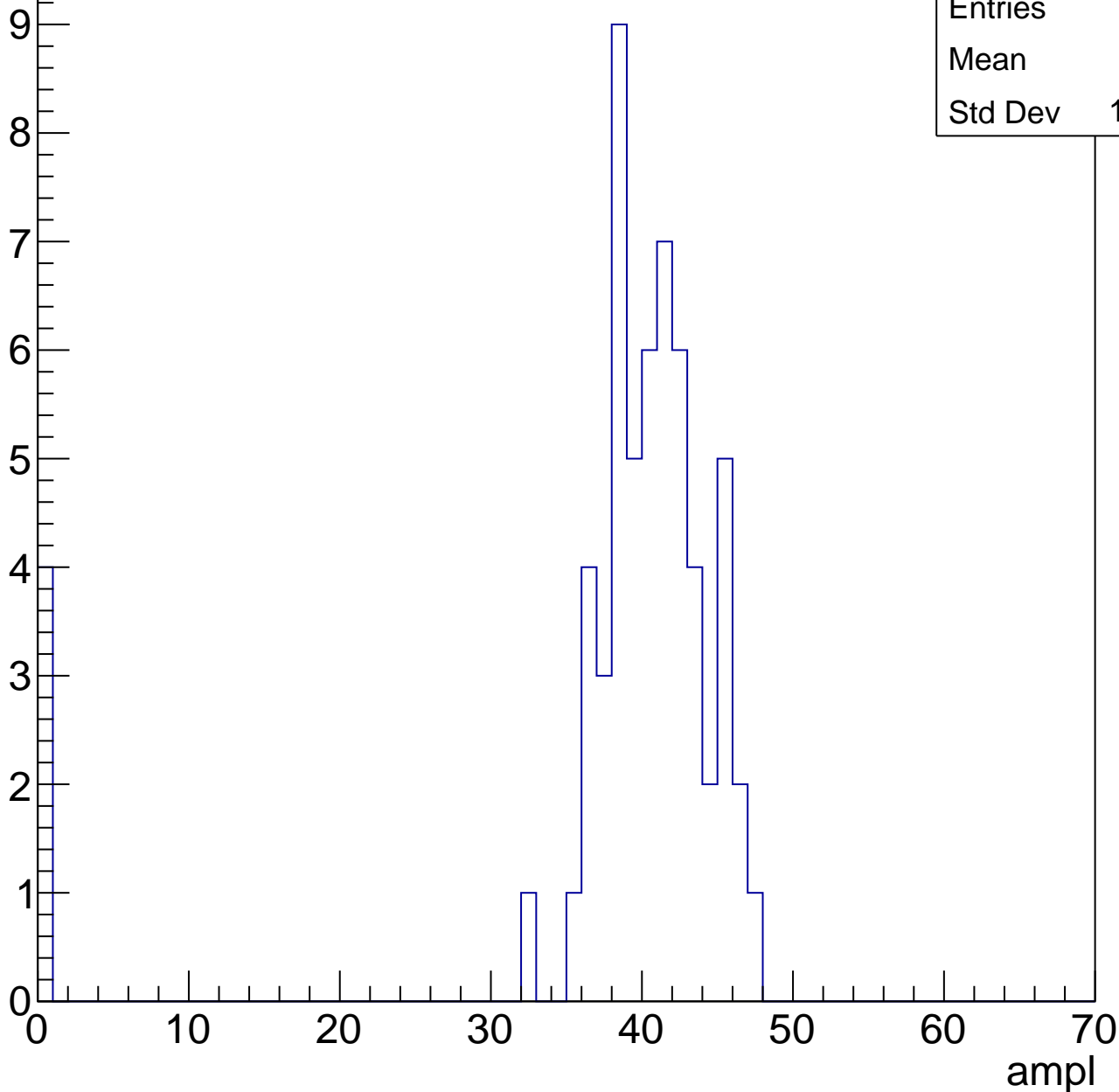


B1L103S, U5-ch59, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

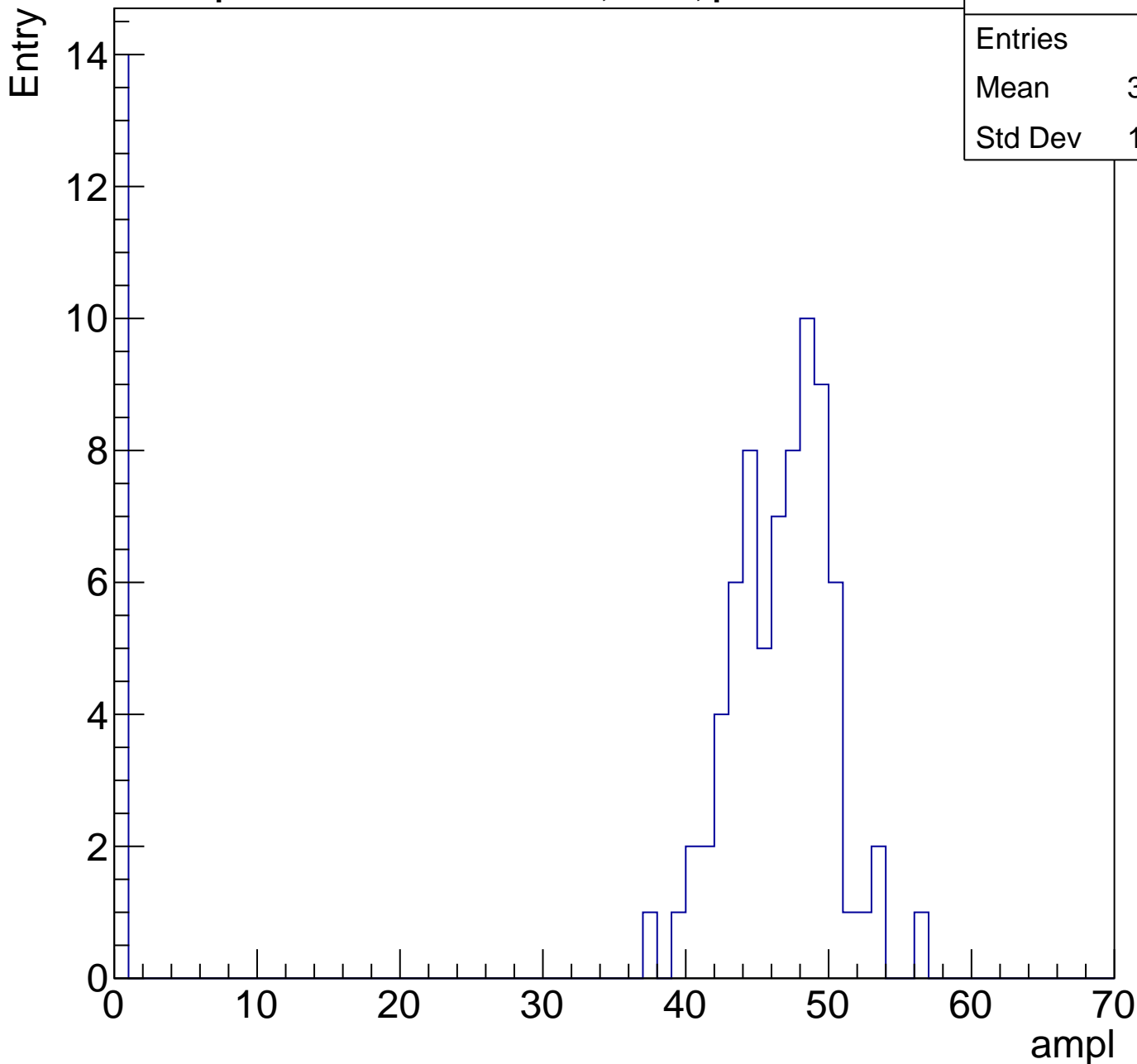
Entries	60
Mean	37.7
Std Dev	10.53



B1L103S, U5-ch59, adc3

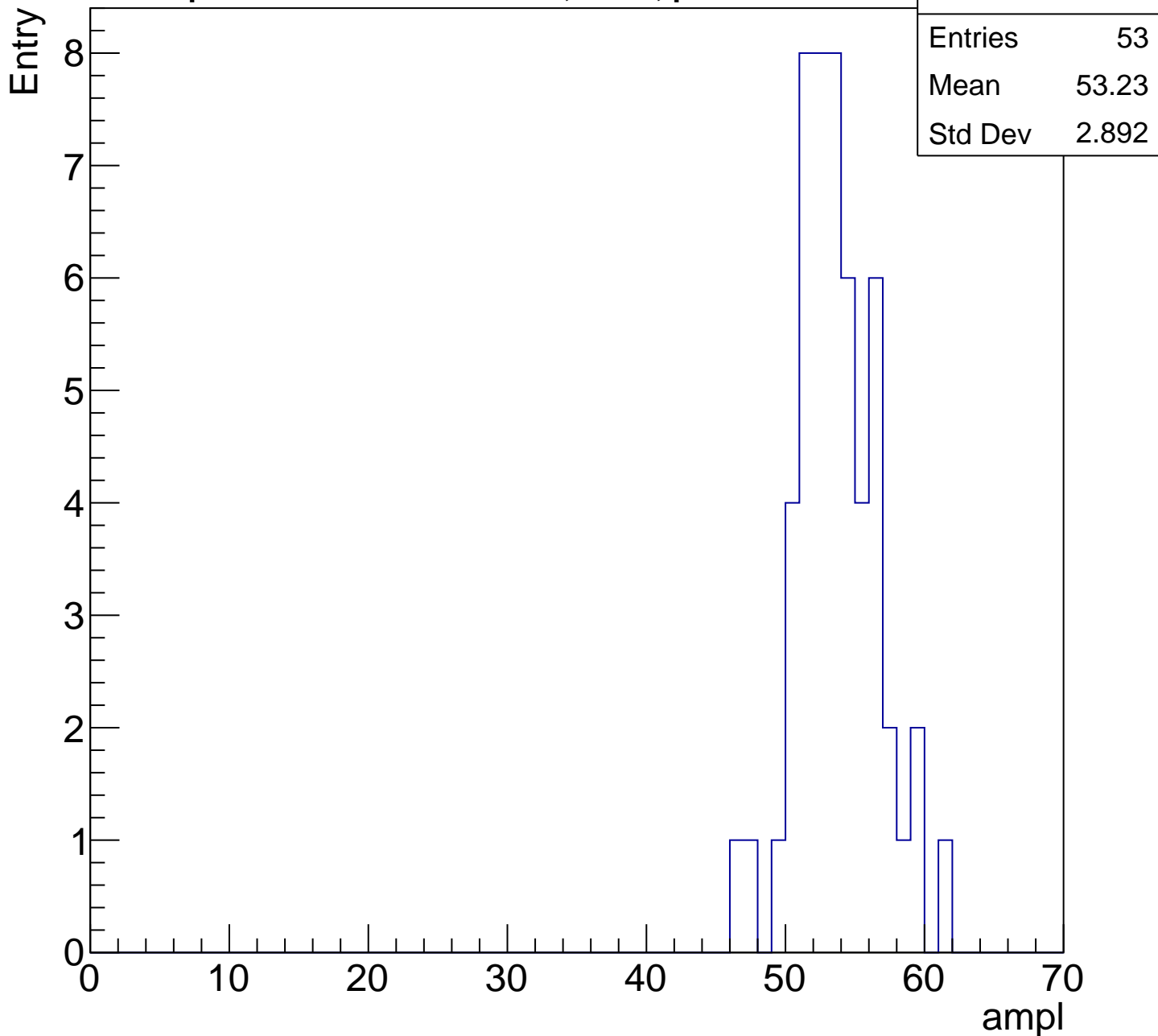
calib_packv5_041523_1651.root, FC#0, port C2

Entries	88
Mean	38.92
Std Dev	17.22



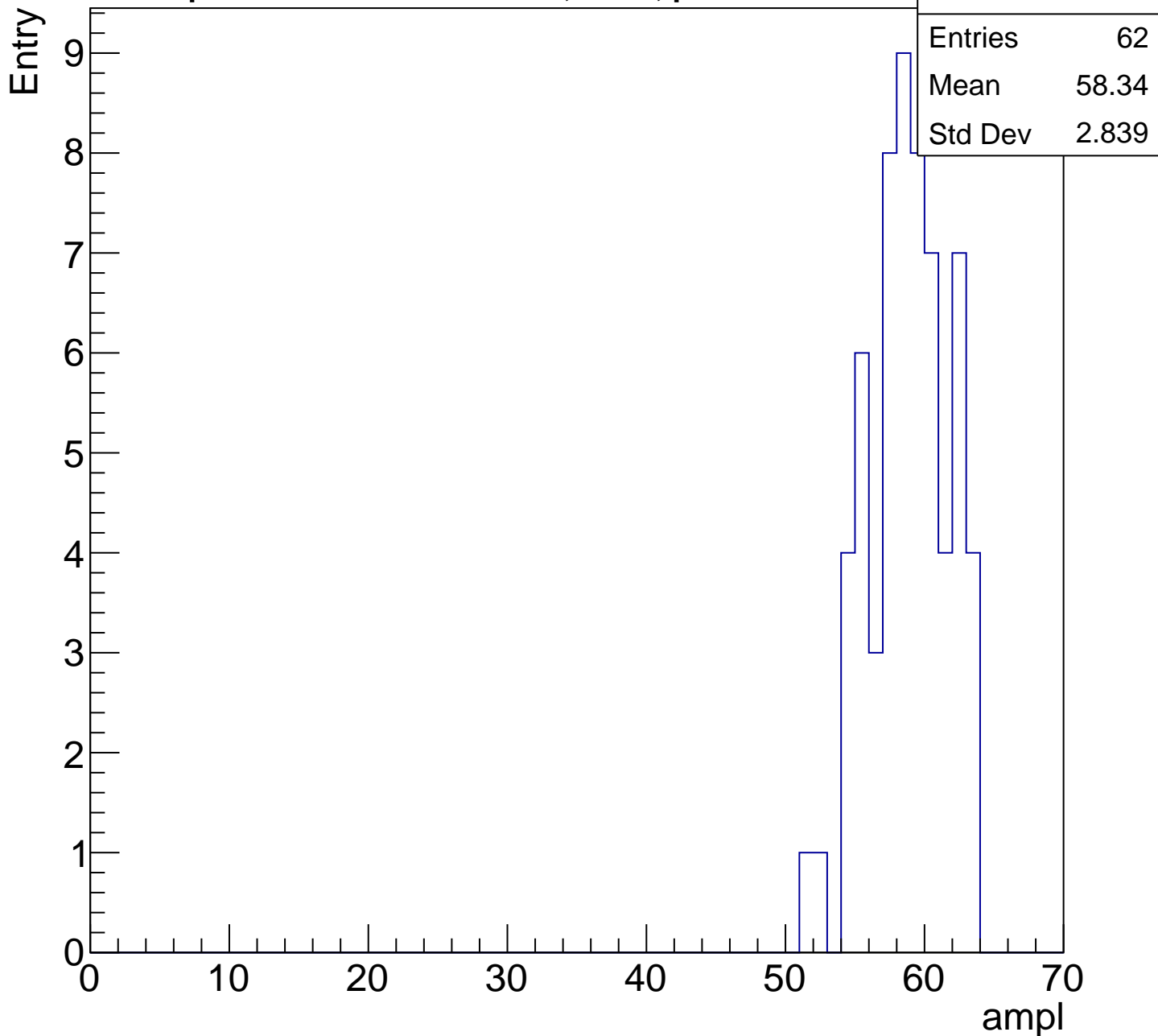
B1L103S, U5-ch59, adc4

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U5-ch59, adc5

calib_packv5_041523_1651.root, FC#0, port C2

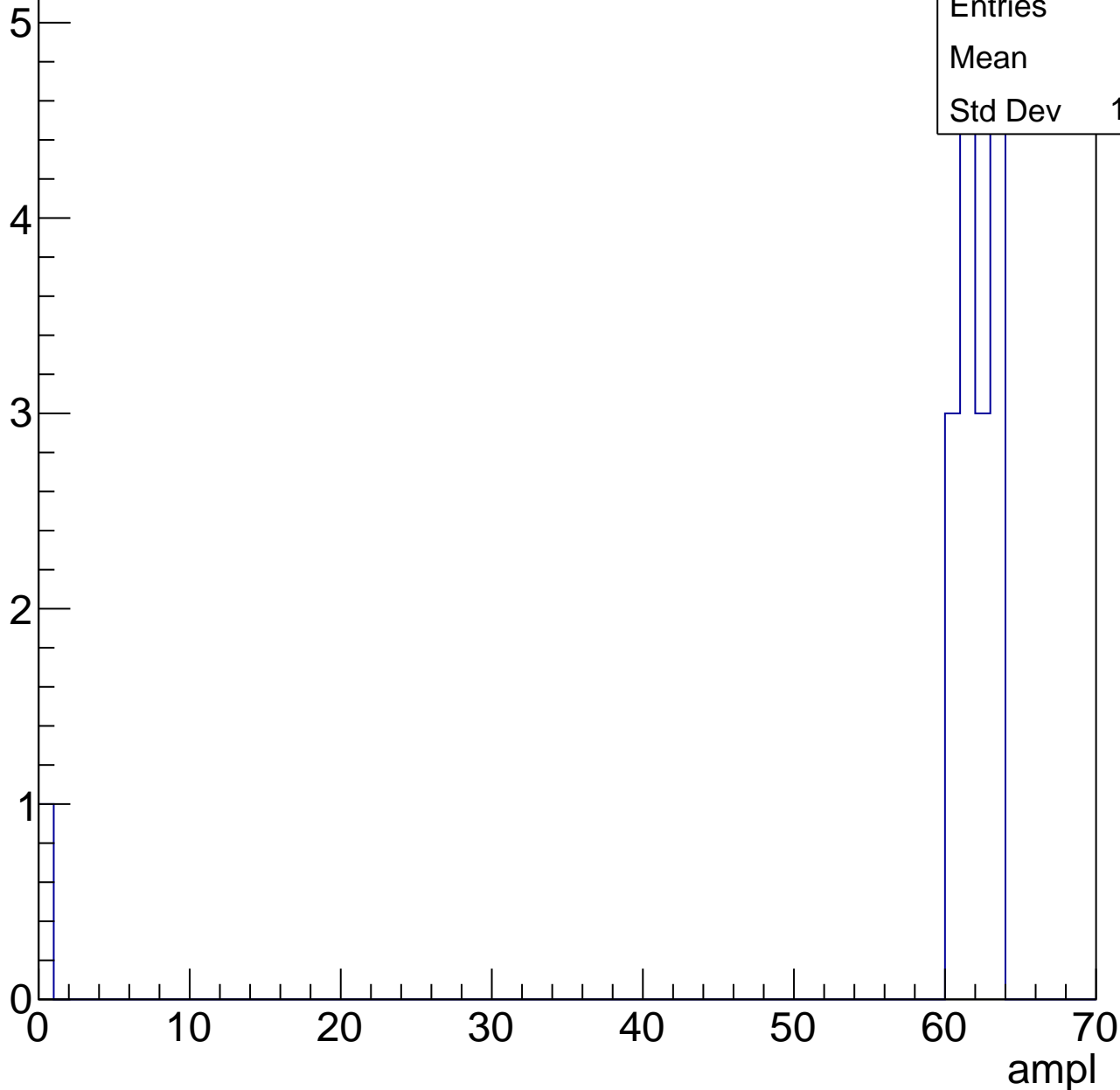


B1L103S, U5-ch59, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	17
Mean	58
Std Dev	14.54



B1L103S, U5-ch59, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry

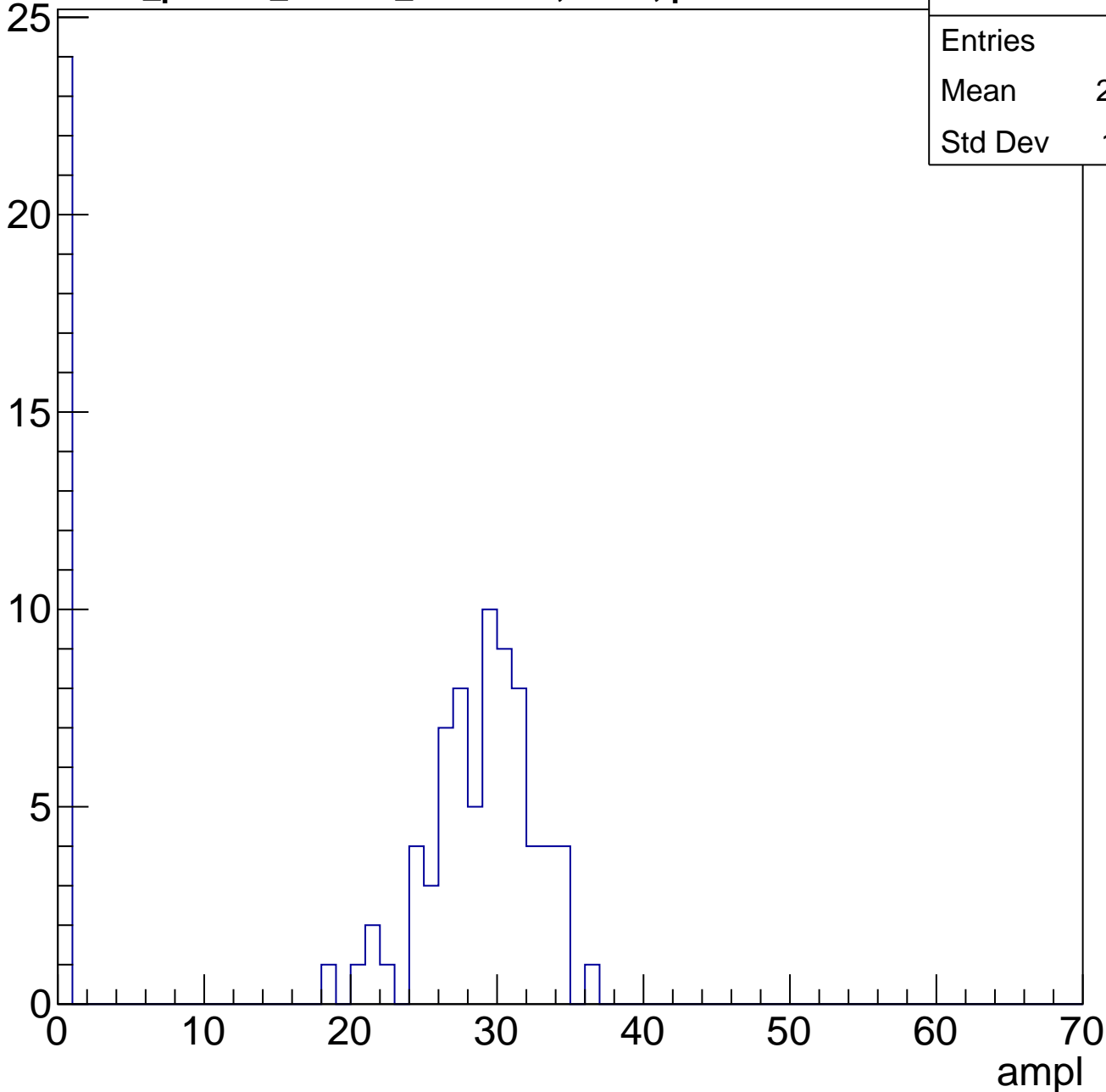


B1L103S, U5-ch60, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	96
Mean	21.36
Std Dev	12.71

Entry

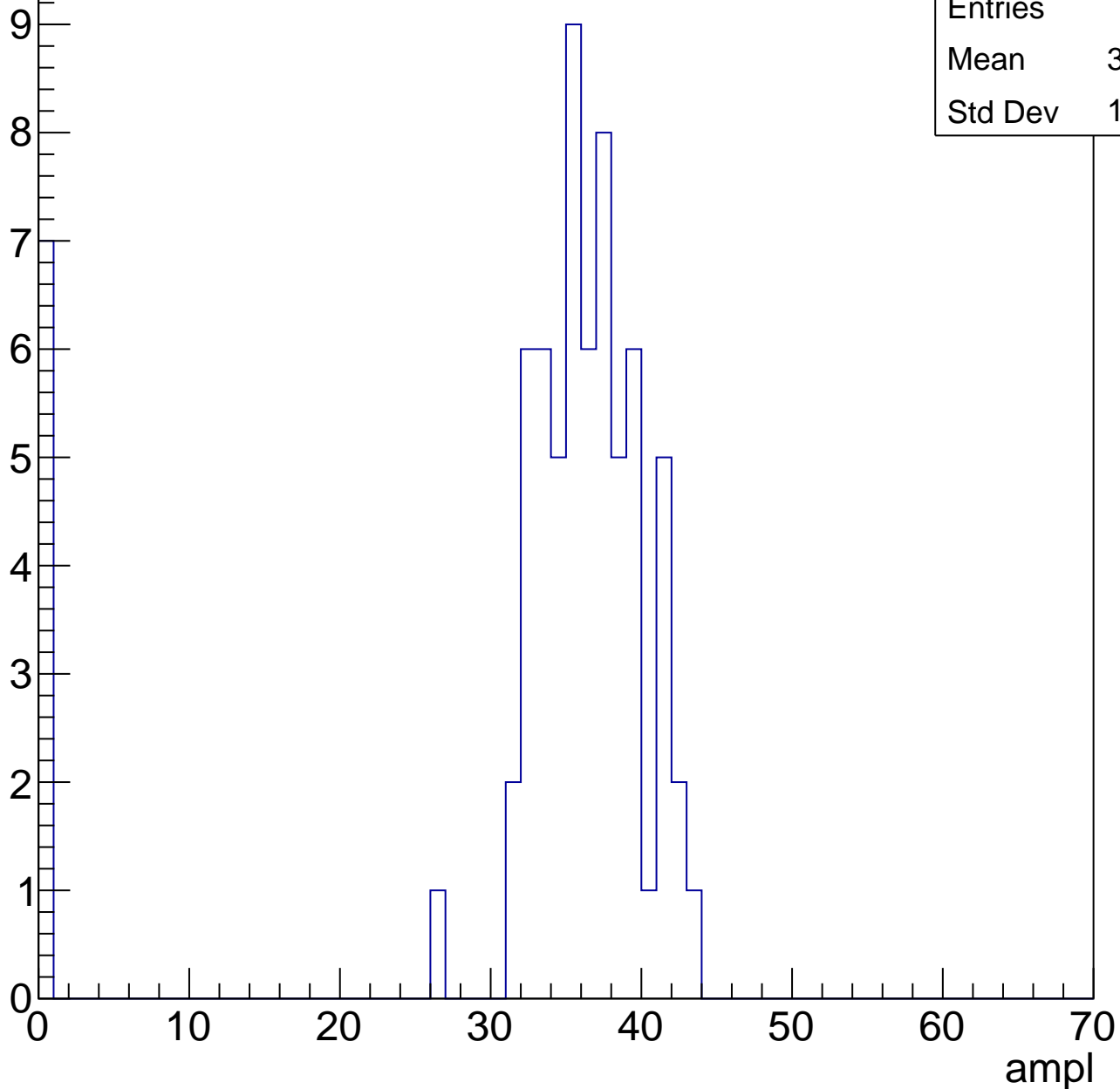


B1L103S, U5-ch60, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	32.44
Std Dev	11.25



B1L103S, U5-ch60, adc2

calib_packv5_041523_1651.root, FC#0, port C2

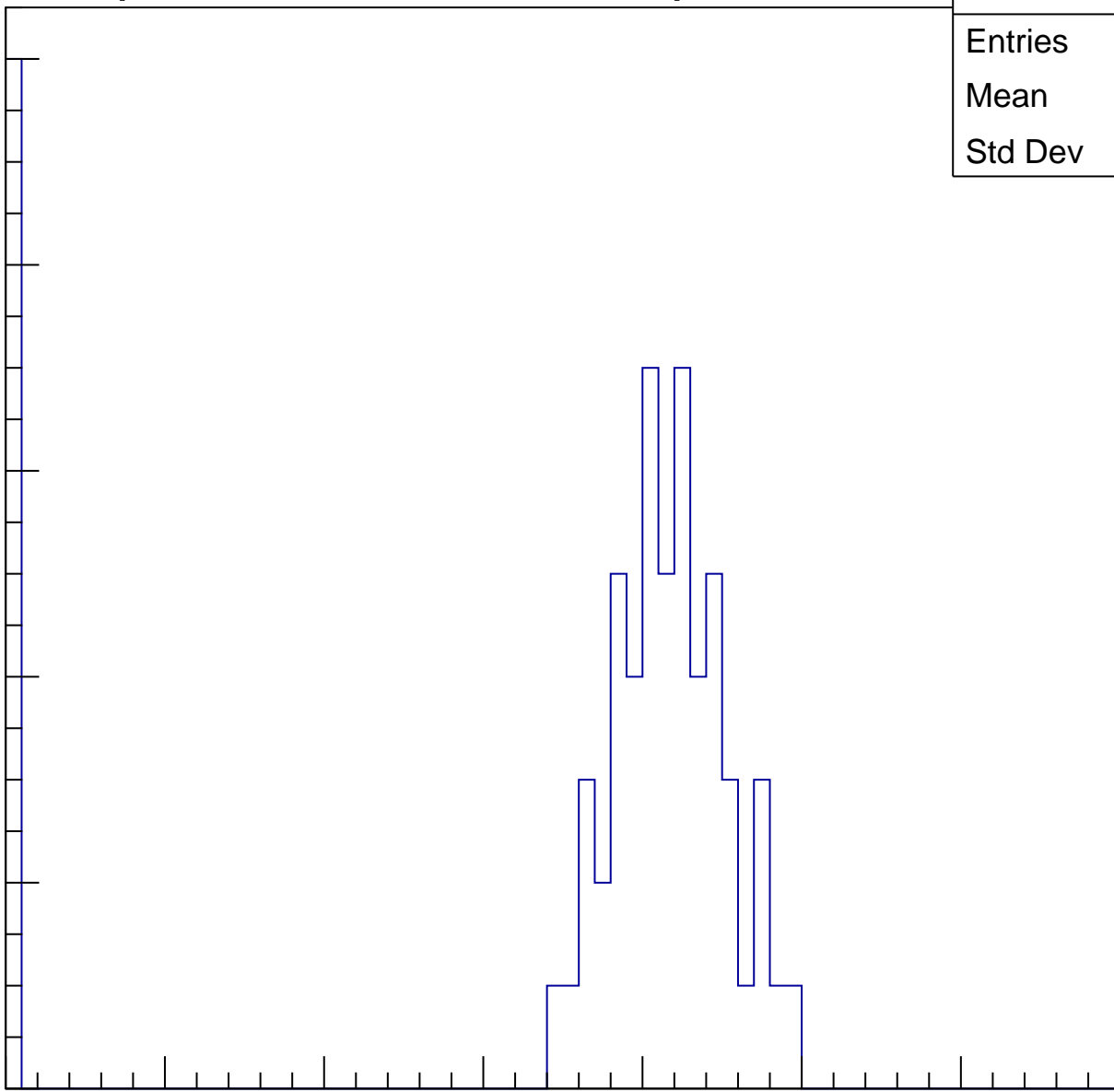
Entries	63
Mean	34.71
Std Dev	15.4

Entry

10
8
6
4
2
0

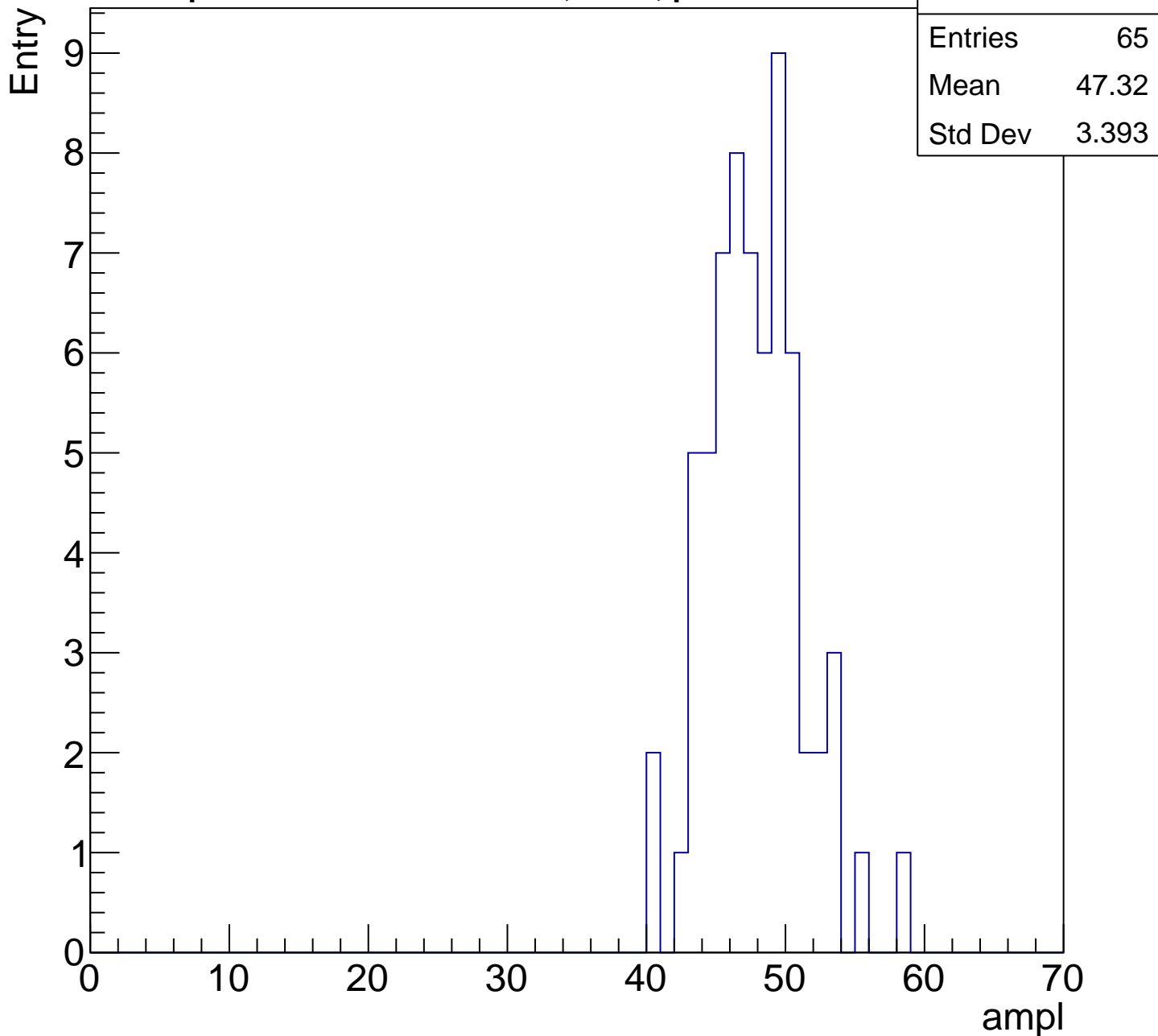
0 10 20 30 40 50 60 70

ampl



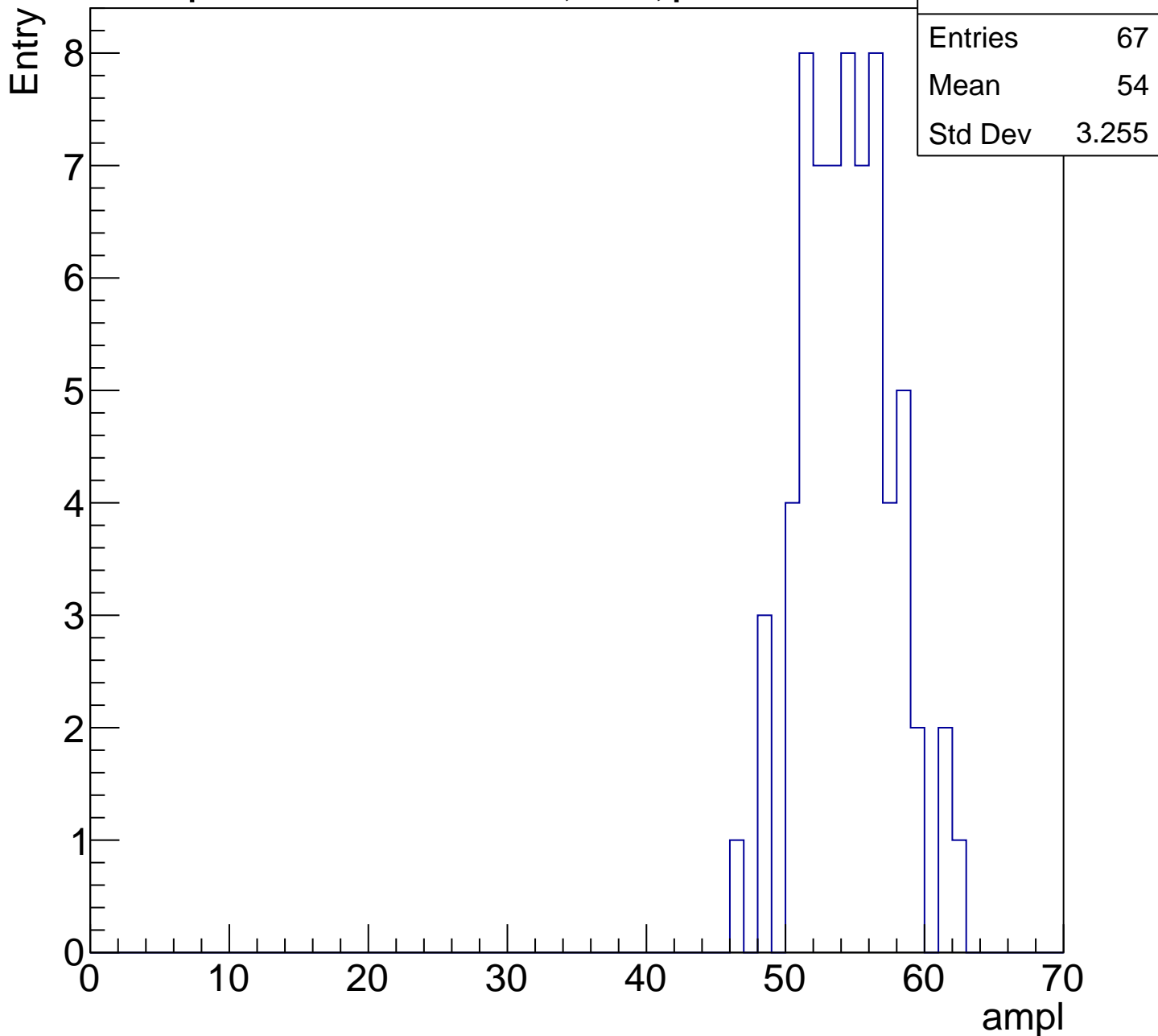
B1L103S, U5-ch60, adc3

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U5-ch60, adc4

calib_packv5_041523_1651.root, FC#0, port C2

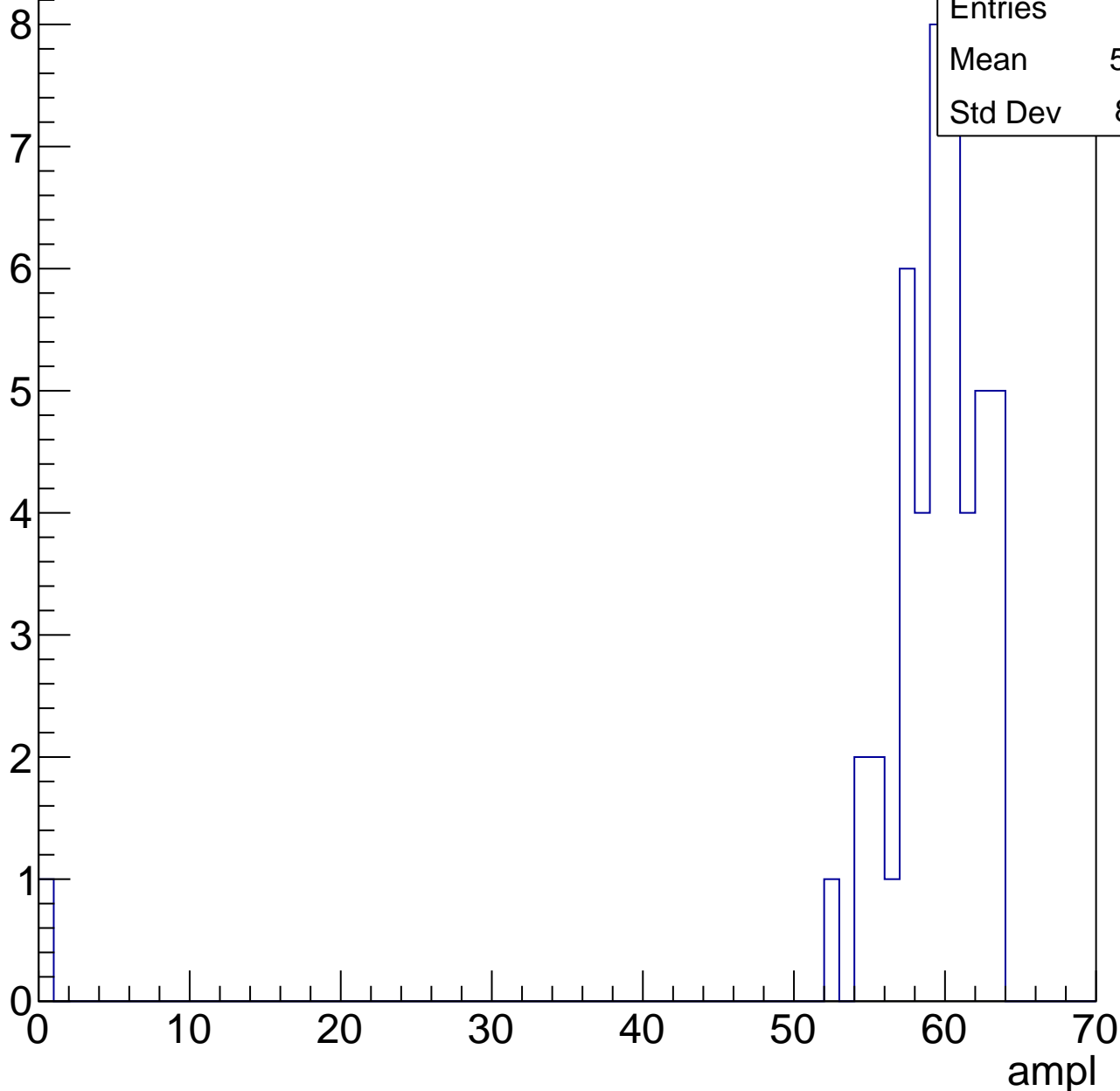


B1L103S, U5-ch60, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

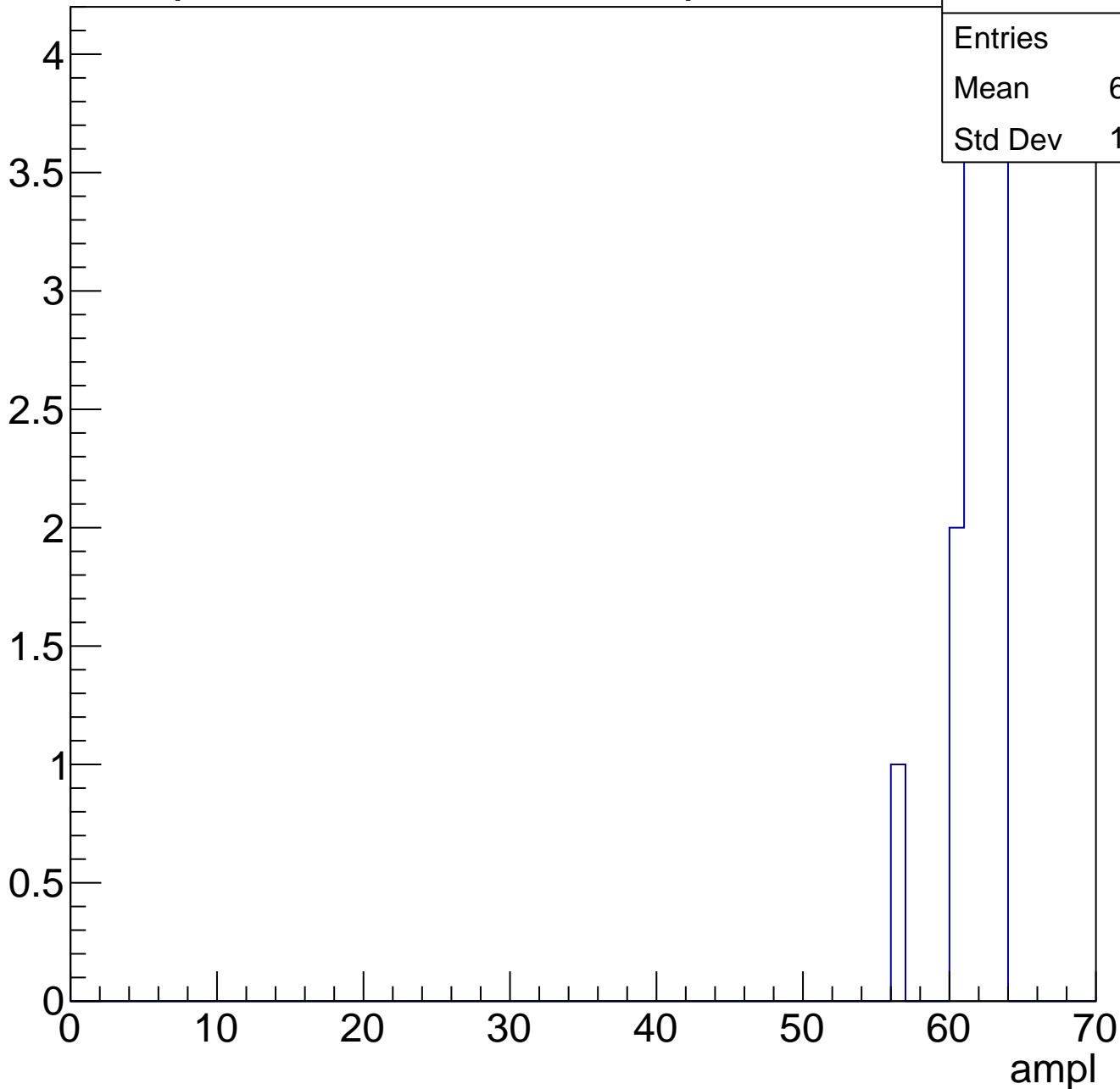
Entries	47
Mean	57.89
Std Dev	8.921



B1L103S, U5-ch60, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch60, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

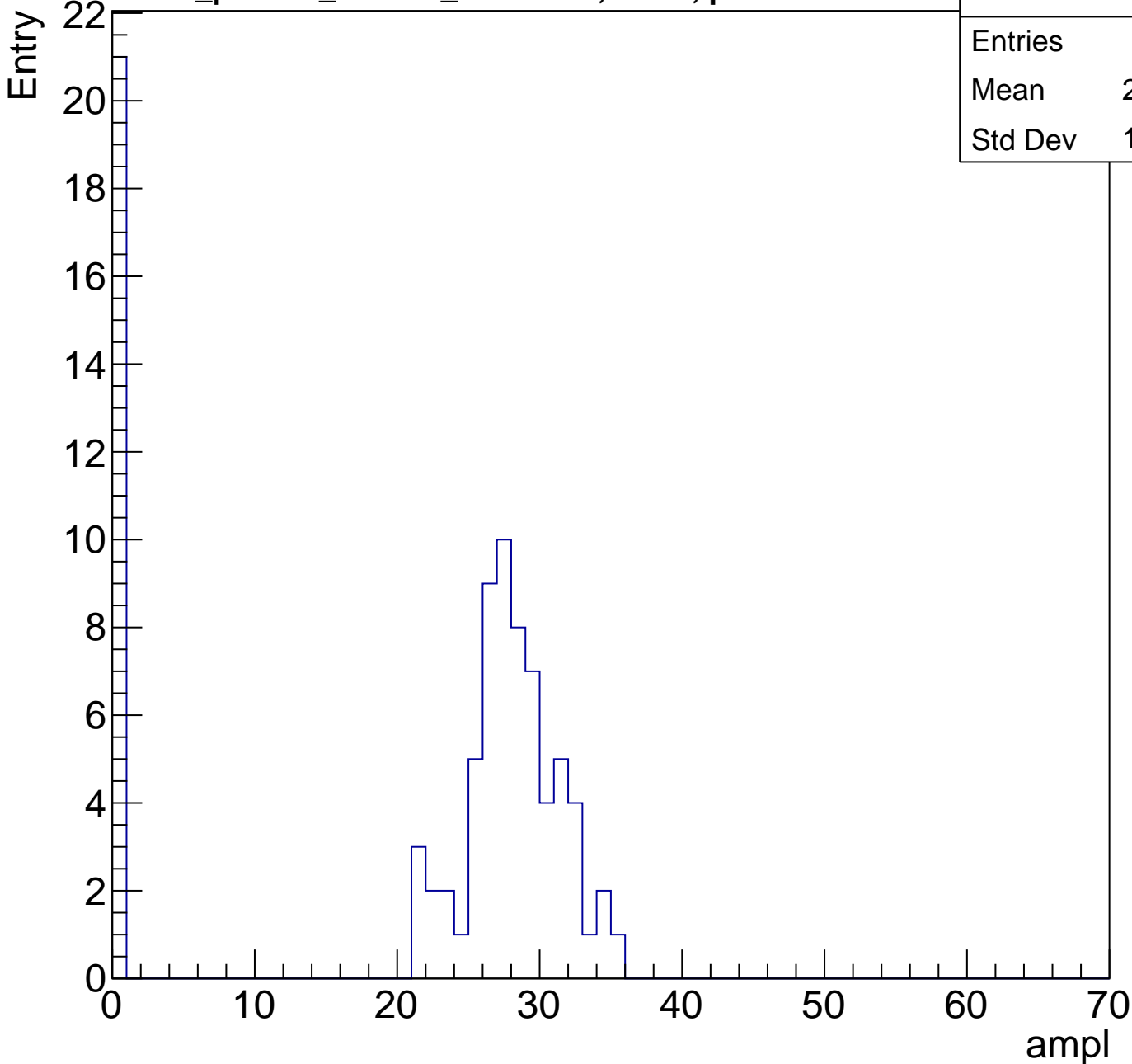
Entry



B1L103S, U5-ch61, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	85
Mean	20.85
Std Dev	12.26

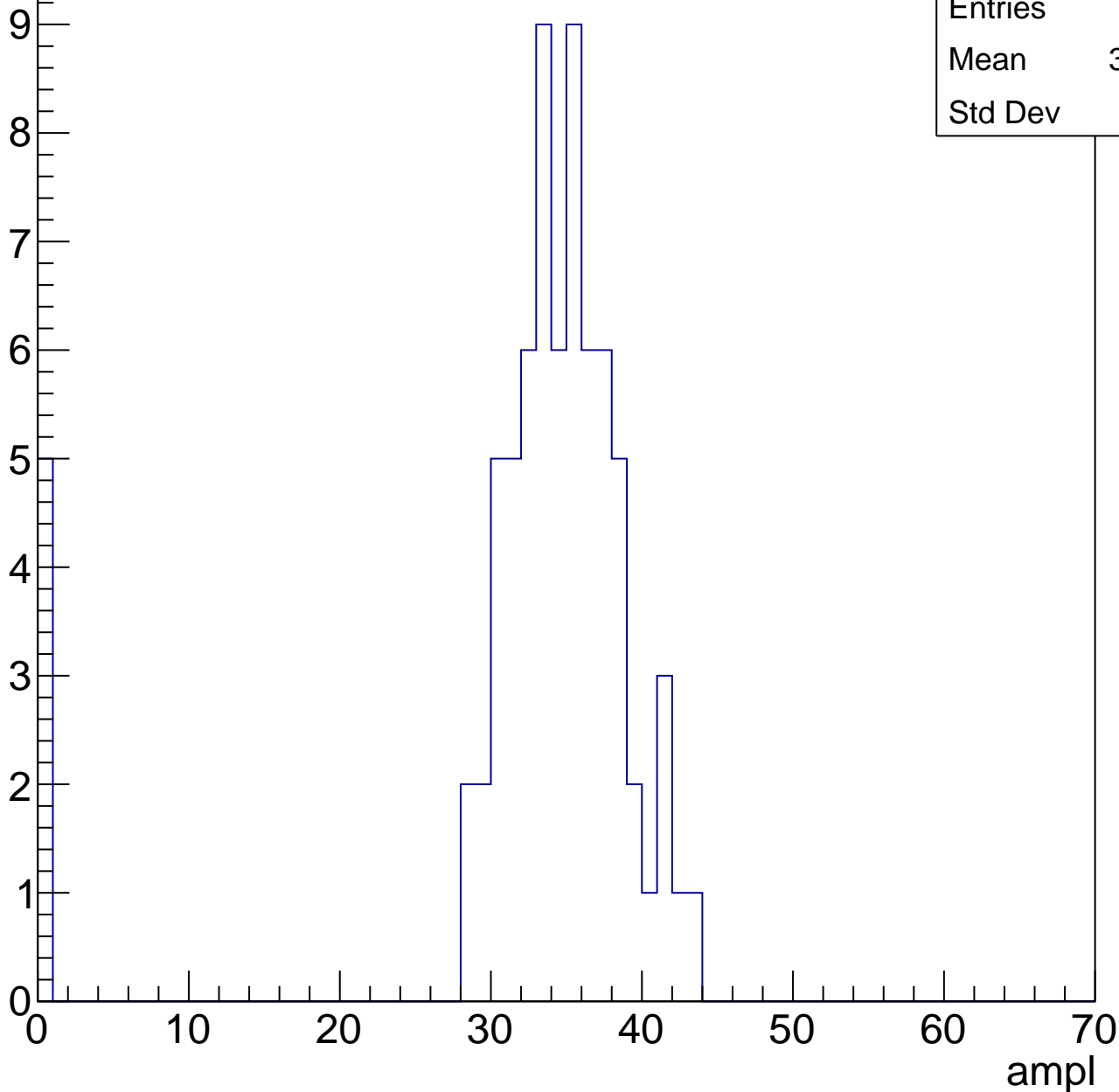


B1L103S, U5-ch61, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	32.18
Std Dev	9.27

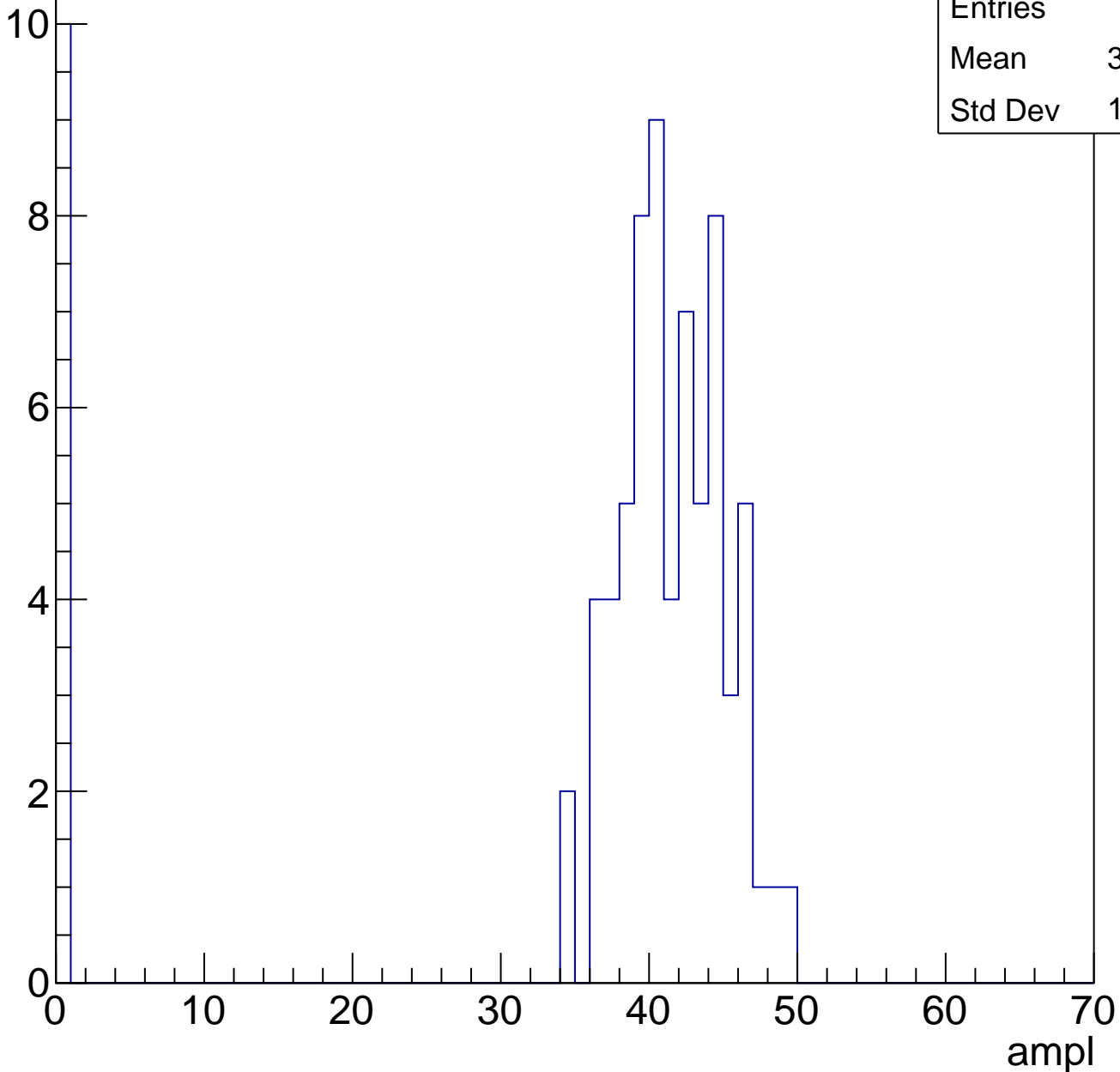


B1L103S, U5-ch61, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	77
Mean	35.79
Std Dev	14.18

Entry

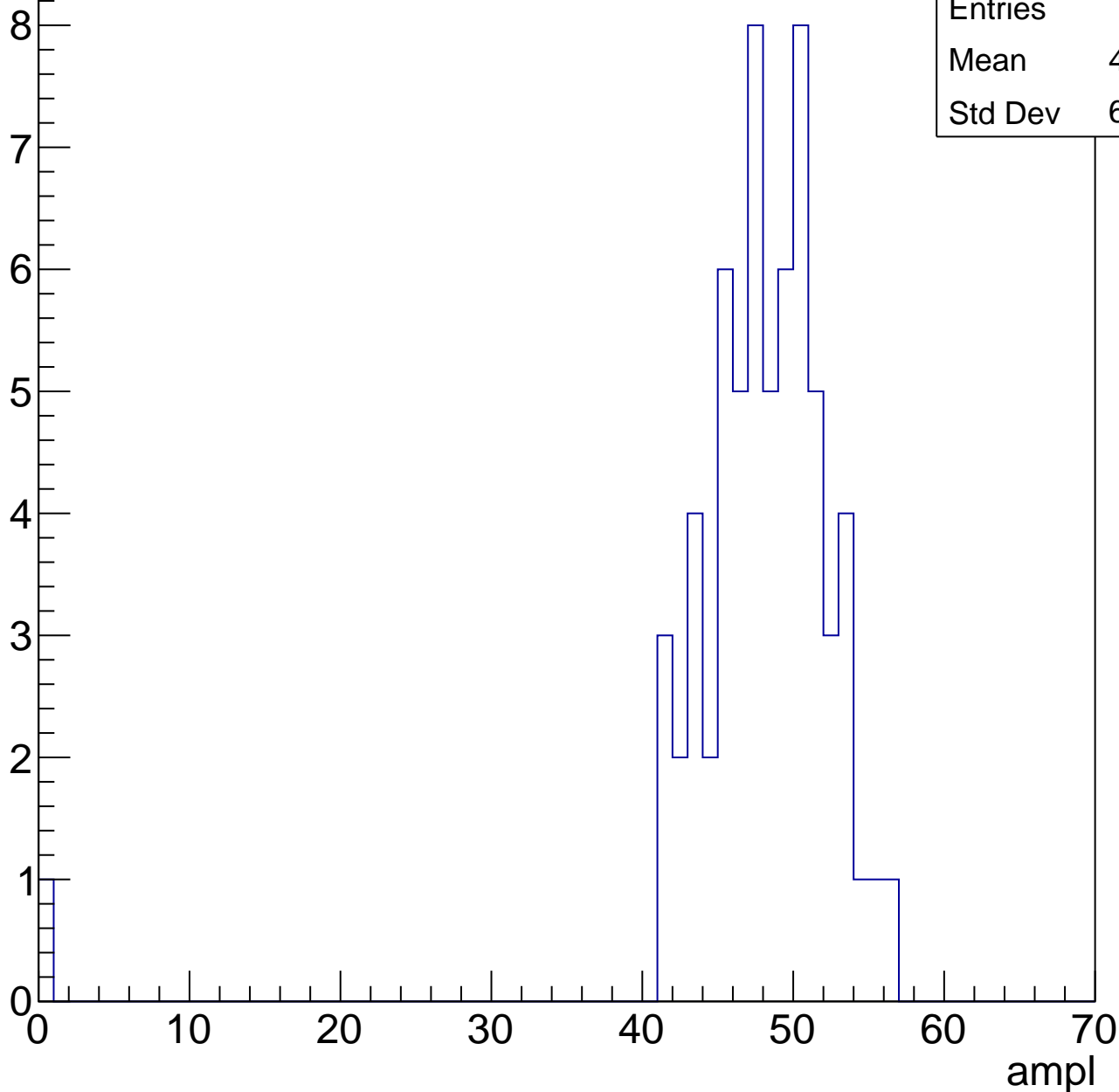


B1L103S, U5-ch61, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	47.15
Std Dev	6.873

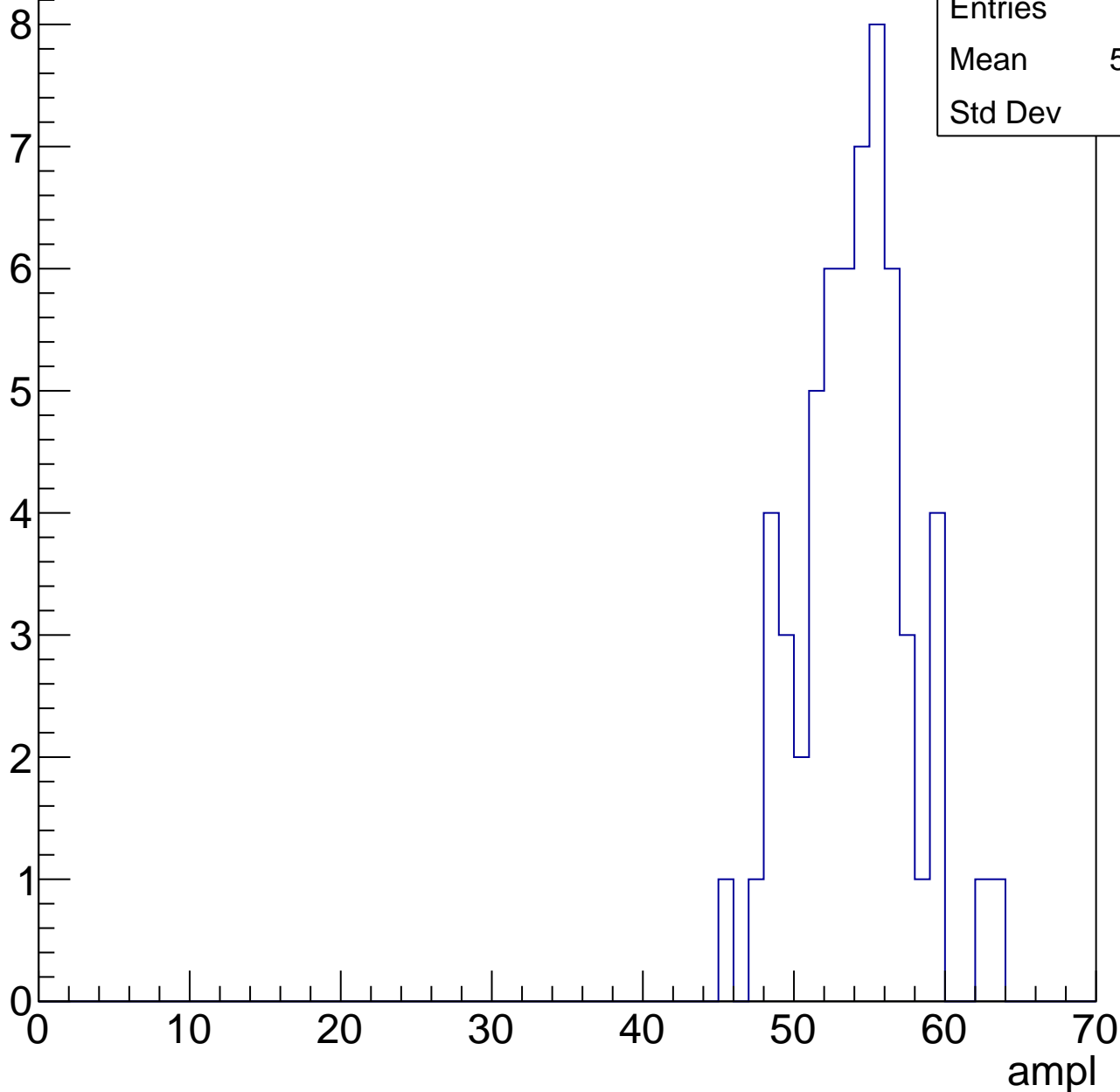


B1L103S, U5-ch61, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	53.56
Std Dev	3.6



B1L103S, U5-ch61, adc5

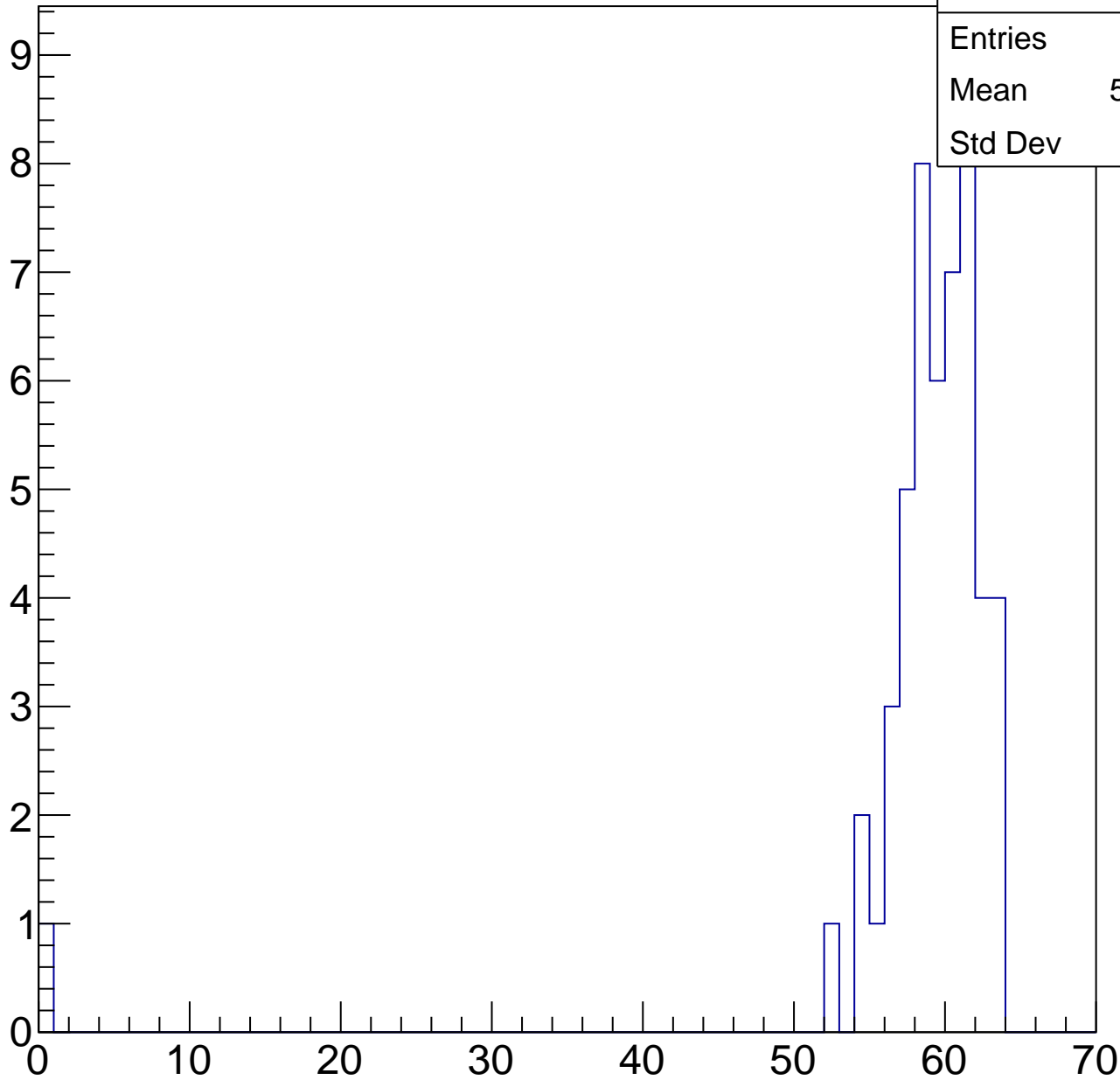
calib_packv5_041523_1651.root, FC#0, port C2

Entry

9
8
7
6
5
4
3
2
1
0

Entries	51
Mean	57.94
Std Dev	8.56

ampl

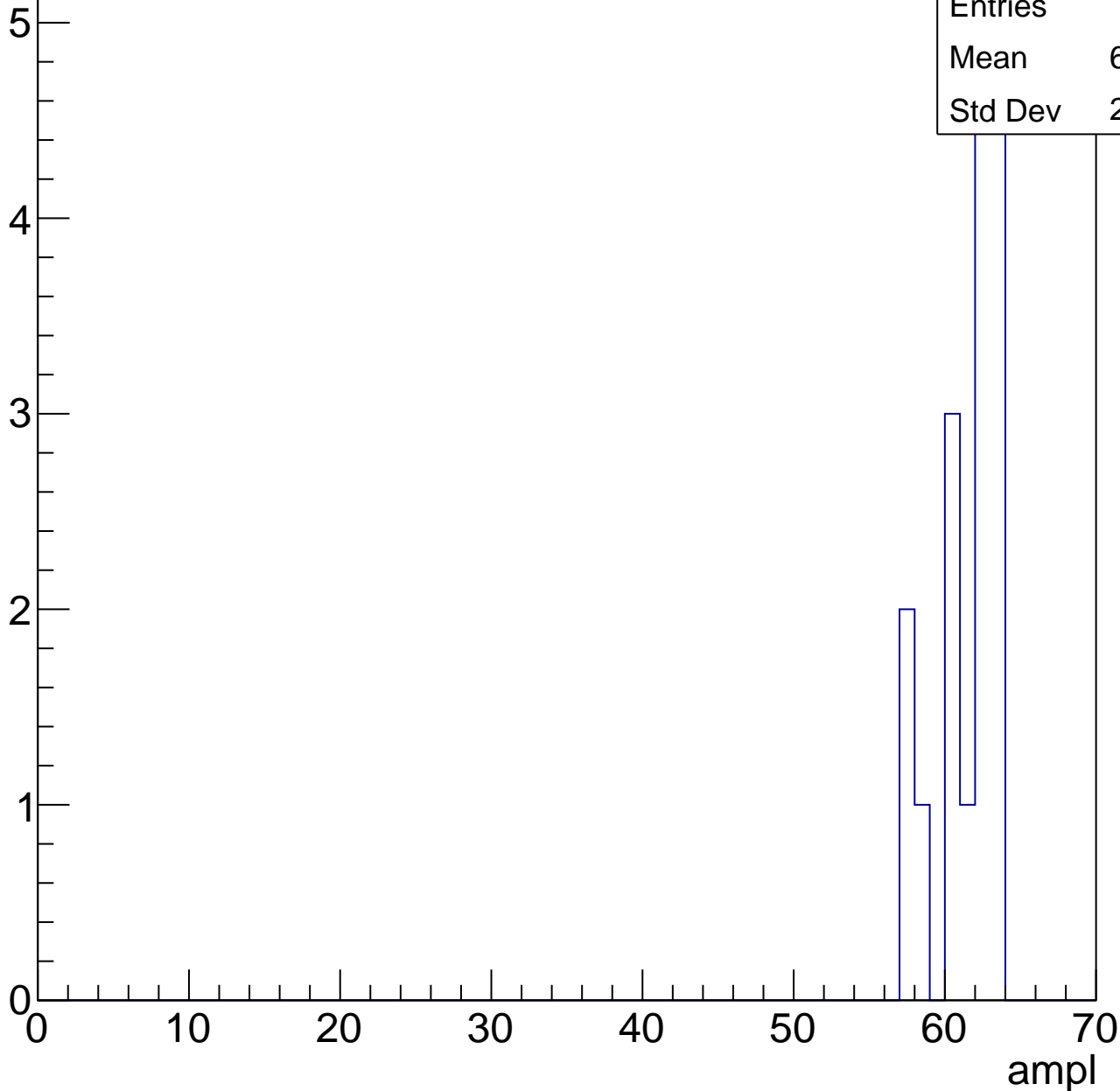


B1L103S, U5-ch61, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	17
Mean	61.06
Std Dev	2.014



B1L103S, U5-ch61, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

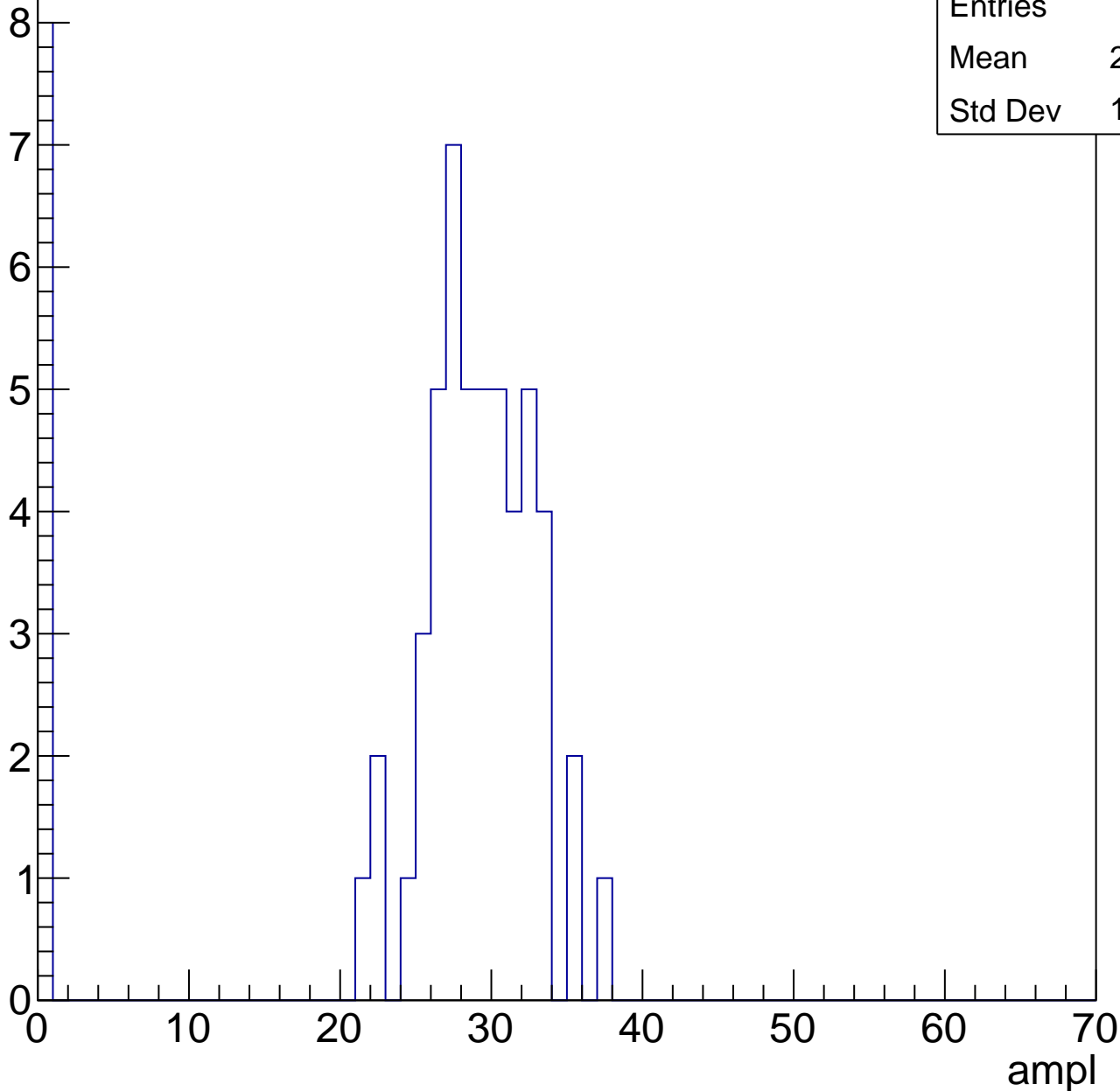
ampl

B1L103S, U5-ch62, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	24.84
Std Dev	10.43

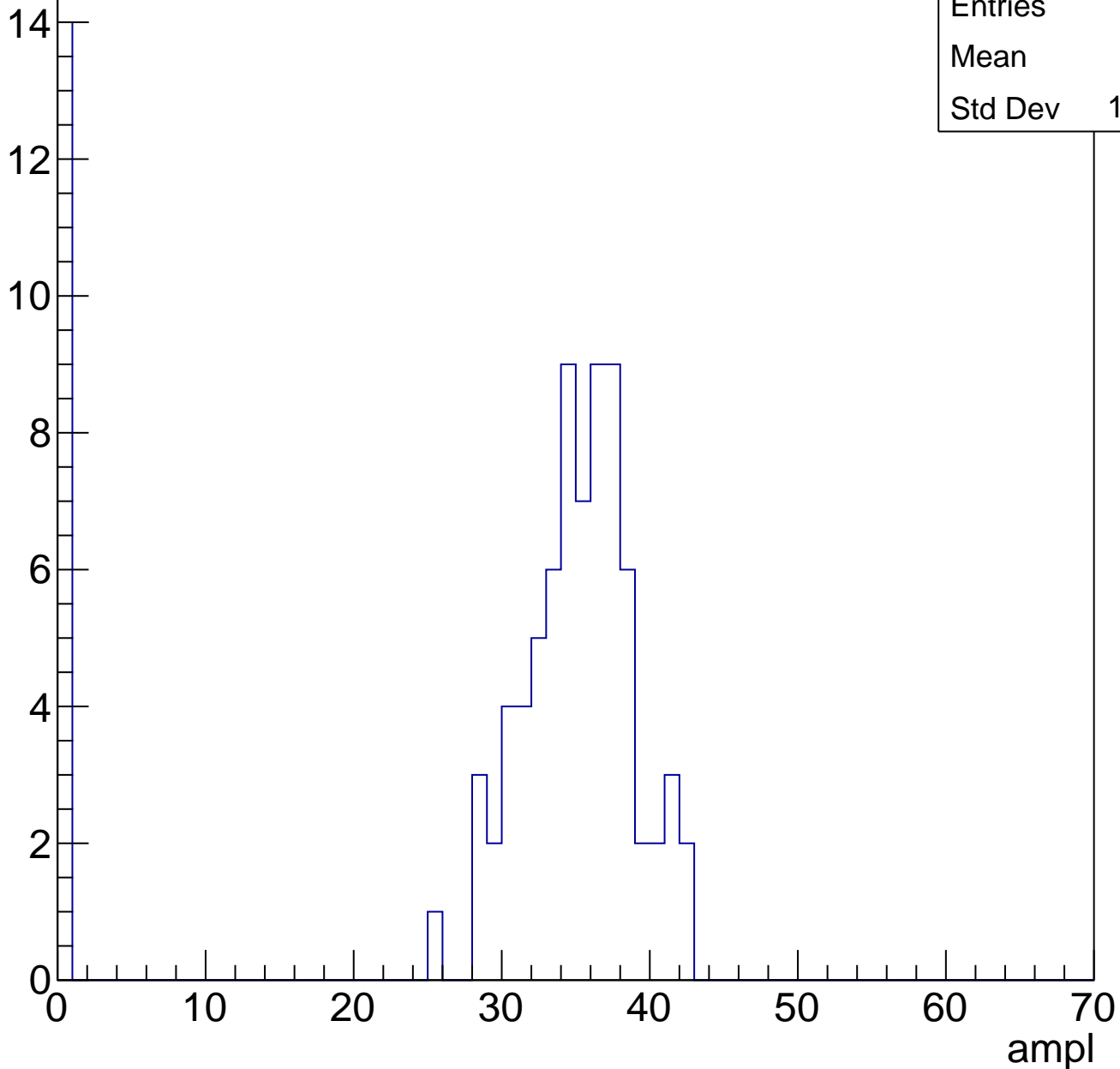


B1L103S, U5-ch62, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	88
Mean	29.2
Std Dev	13.12

Entry

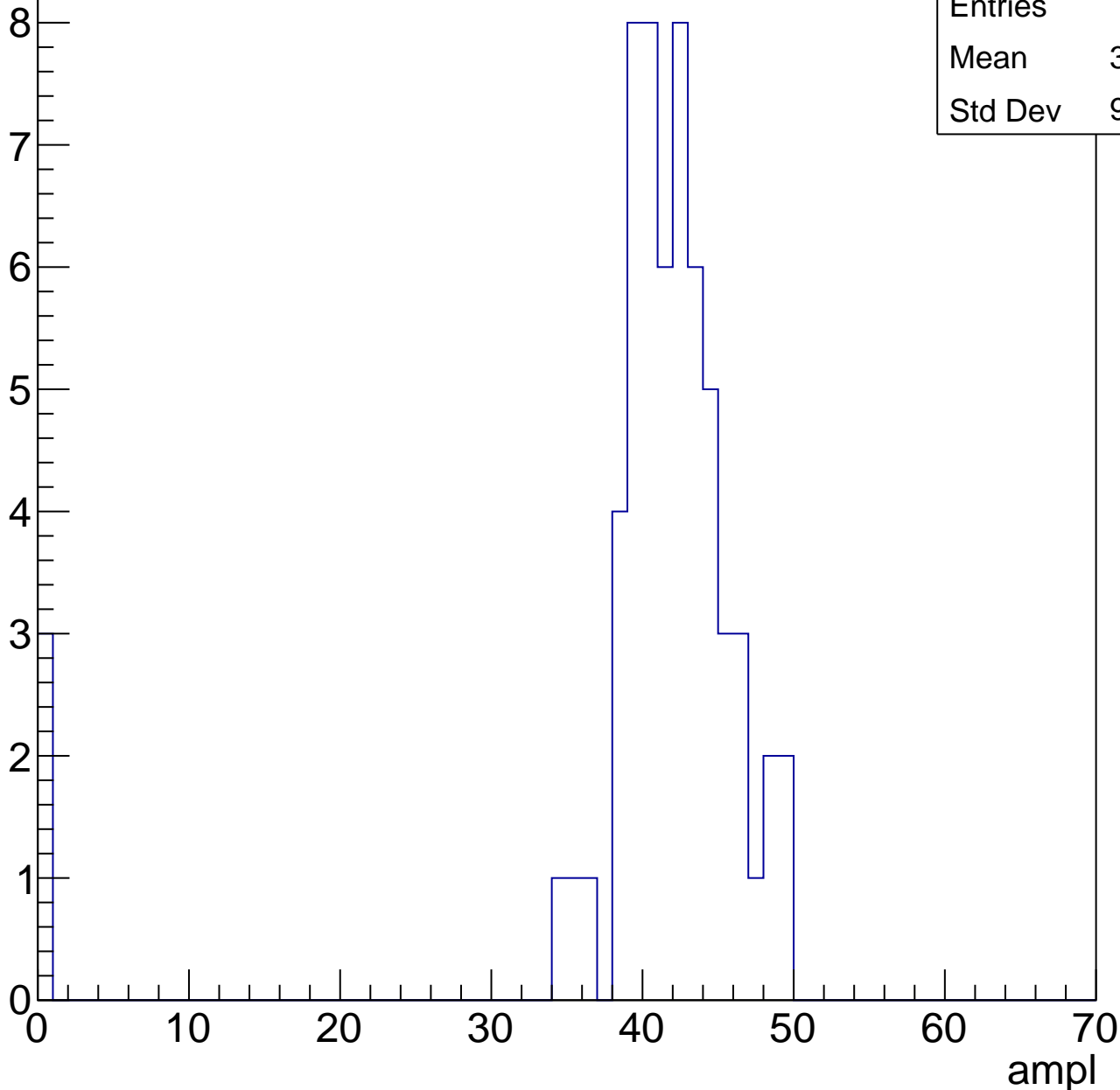


B1L103S, U5-ch62, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	39.73
Std Dev	9.496

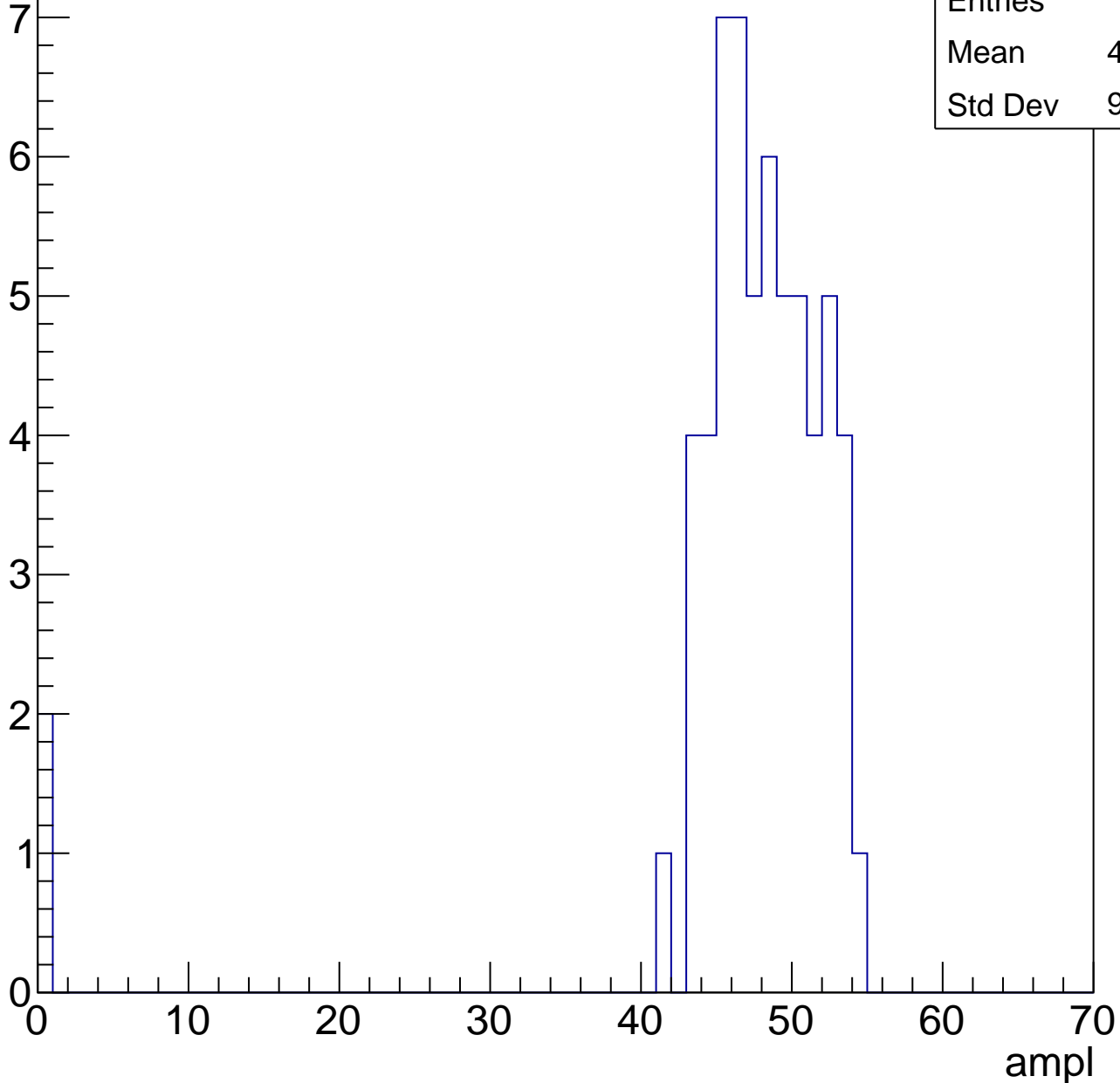


B1L103S, U5-ch62, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	46.23
Std Dev	9.135

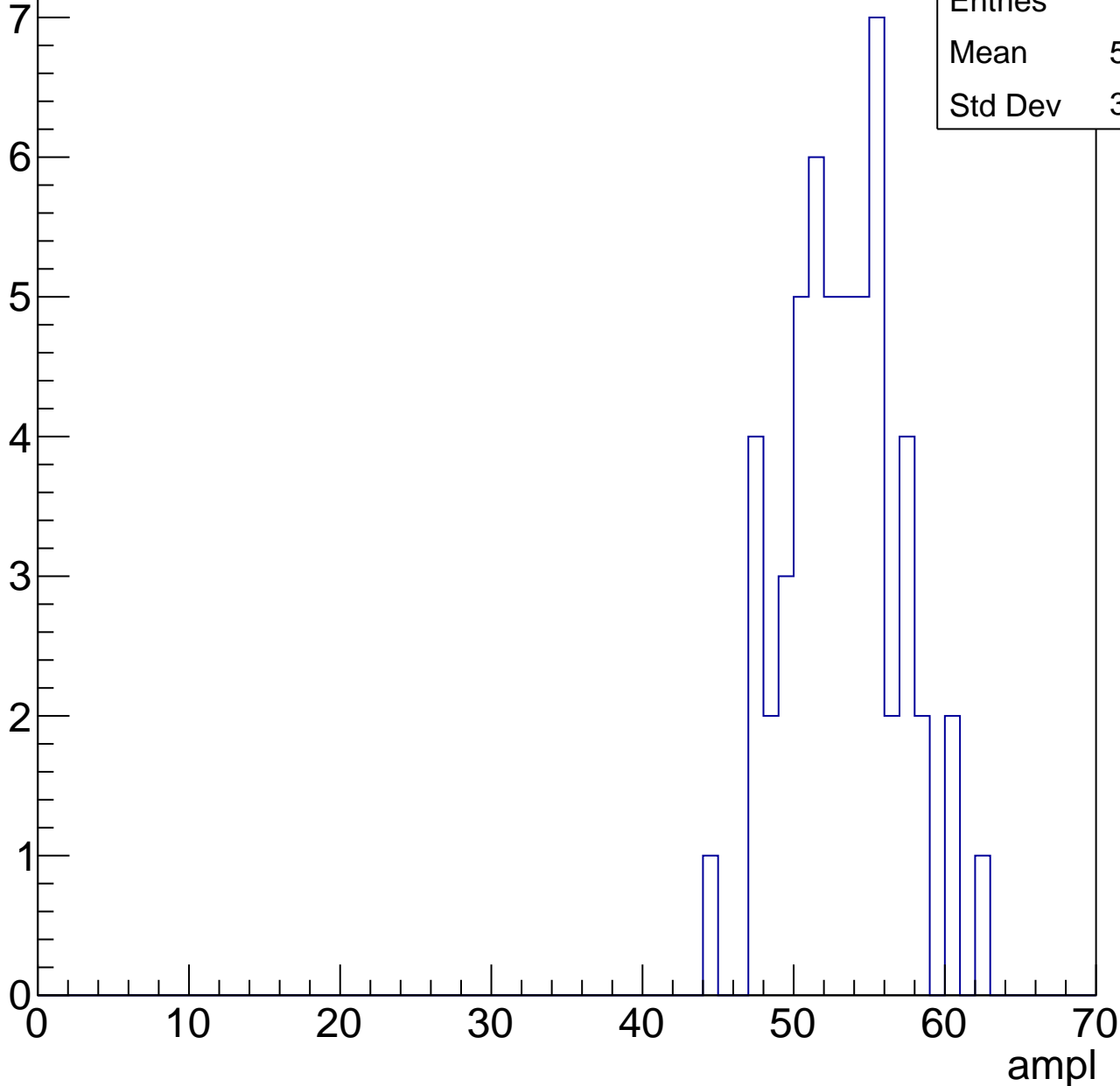


B1L103S, U5-ch62, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

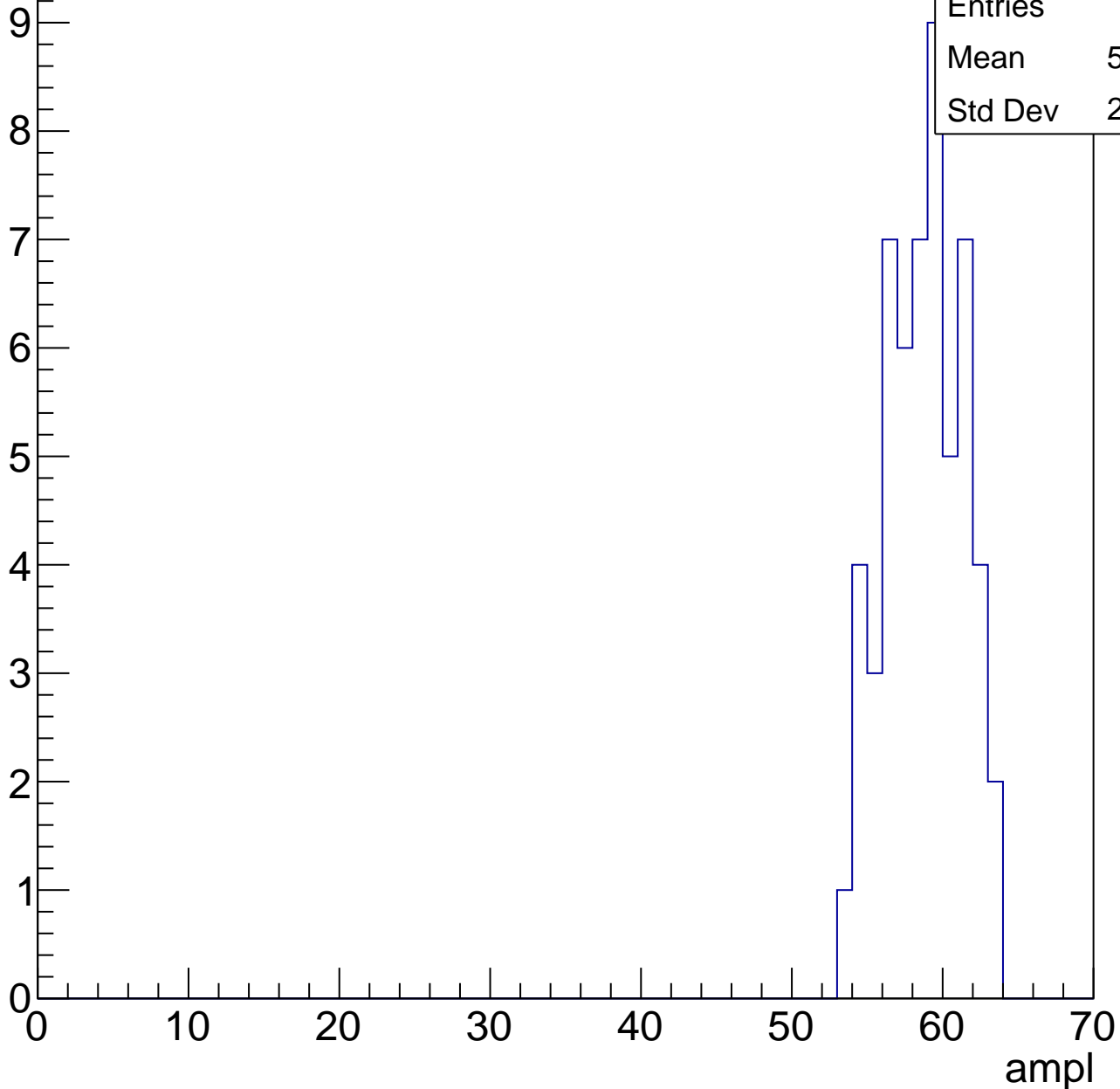
Entries	54
Mean	52.76
Std Dev	3.697



B1L103S, U5-ch62, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



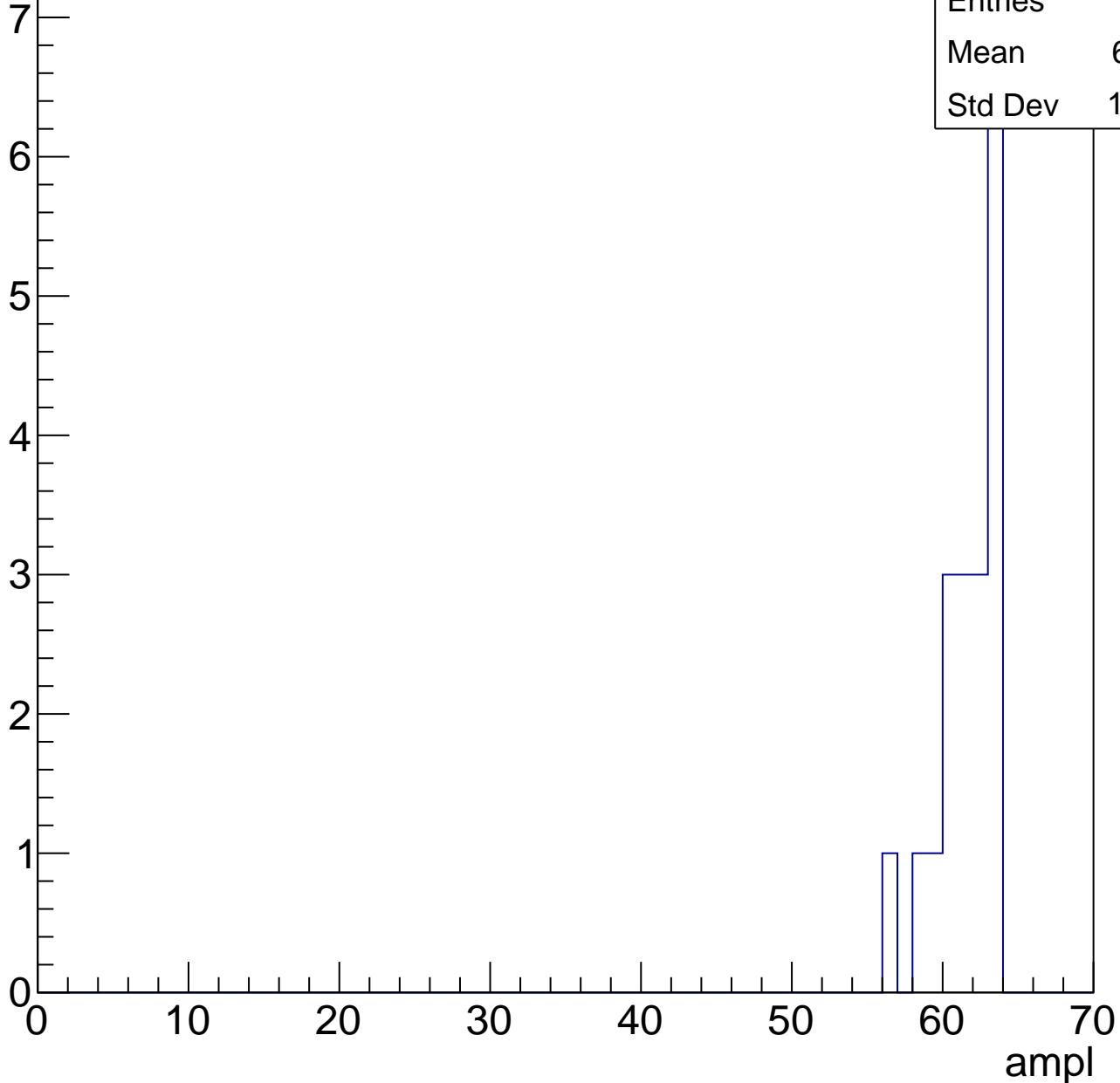
Entries	55
Mean	58.29
Std Dev	2.527

B1L103S, U5-ch62, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	19
Mean	61.21
Std Dev	1.935



B1L103S, U5-ch62, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

20
18
16
14
12
10
8
6
4
2
0

Entries	23
Mean	8.13
Std Dev	20.99

0 10 20 30 40 50 60 70

ampl

2

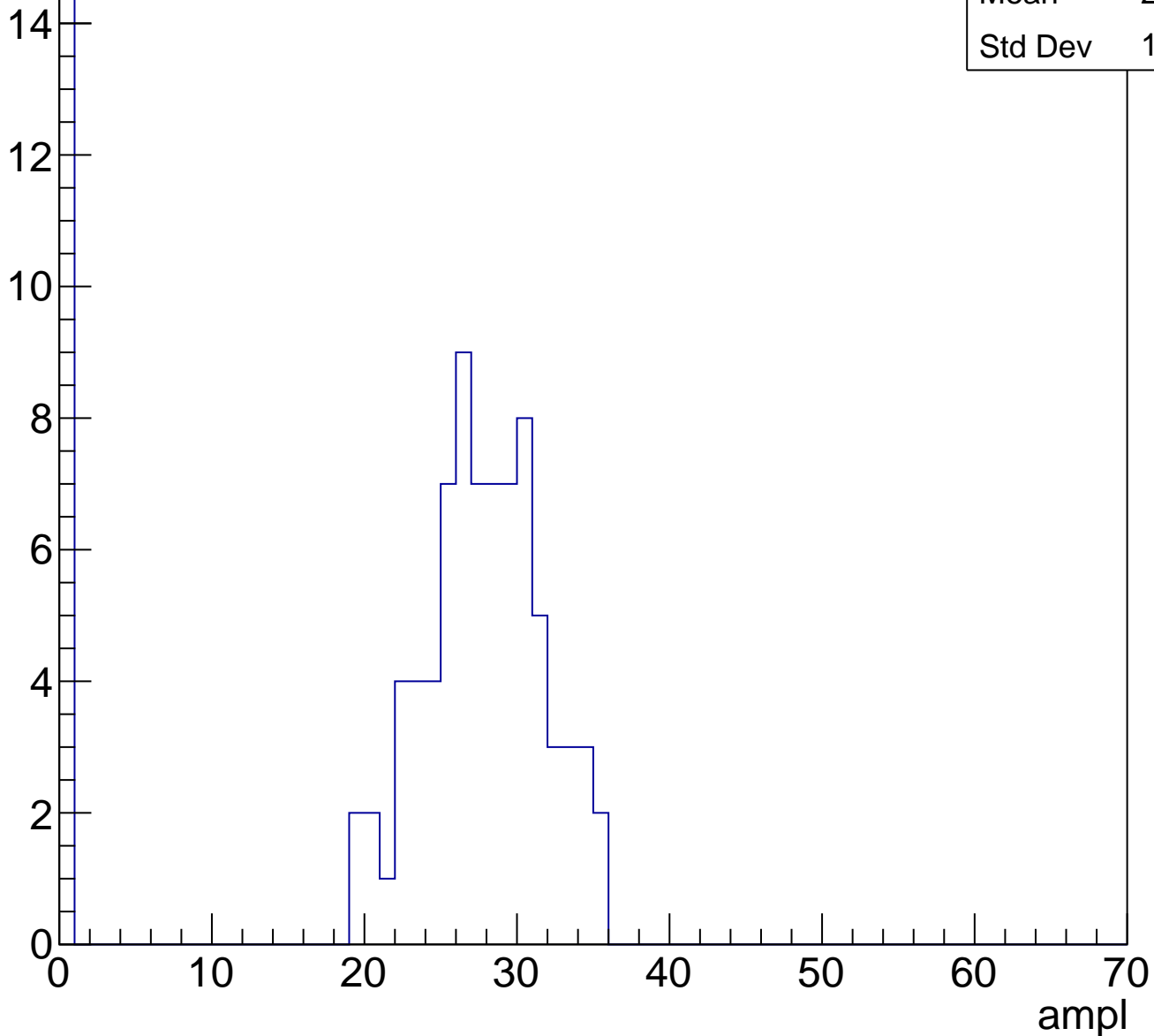
1

B1L103S, U5-ch63, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	93
Mean	22.95
Std Dev	10.65

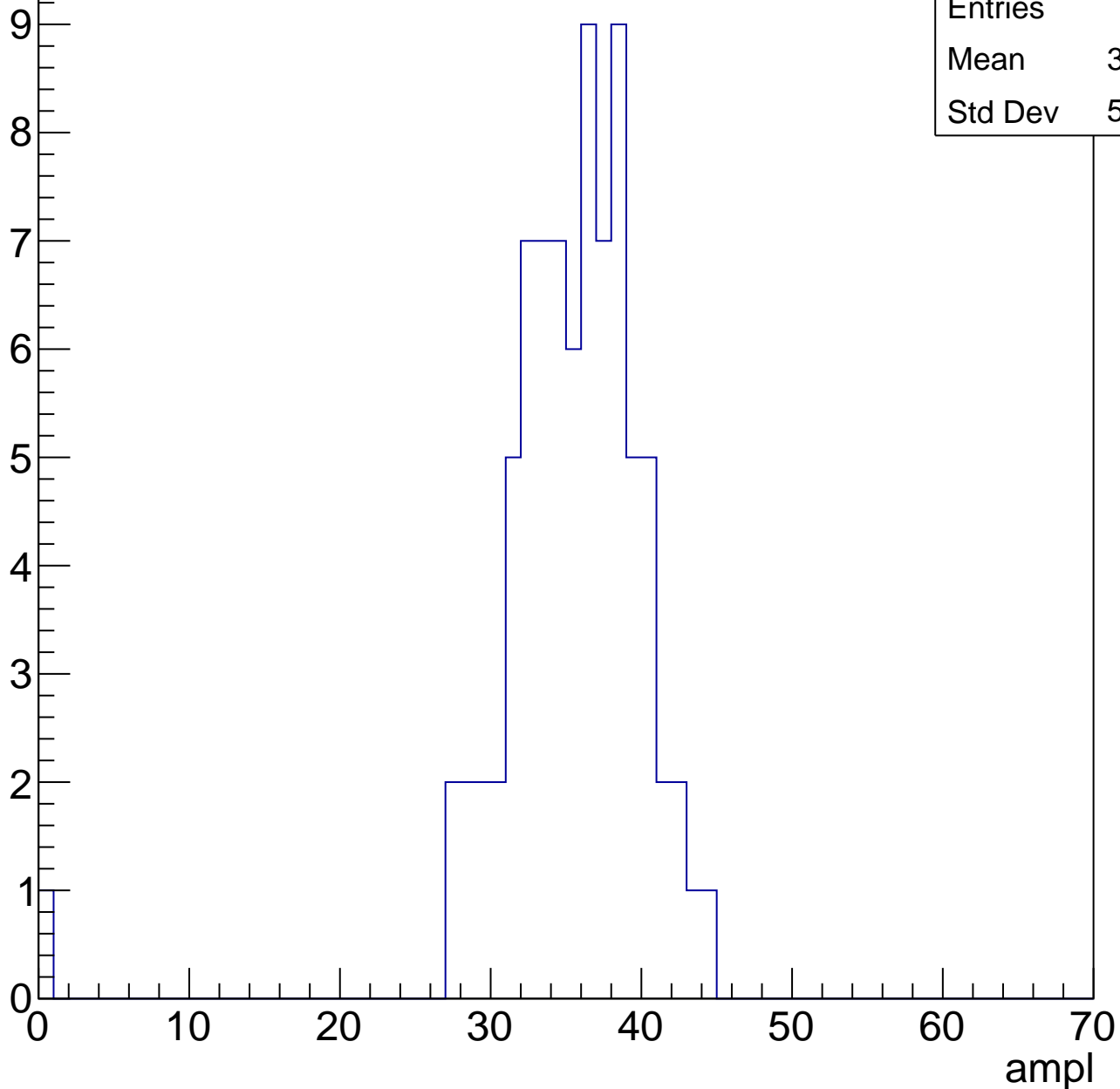
Entry



B1L103S, U5-ch63, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry



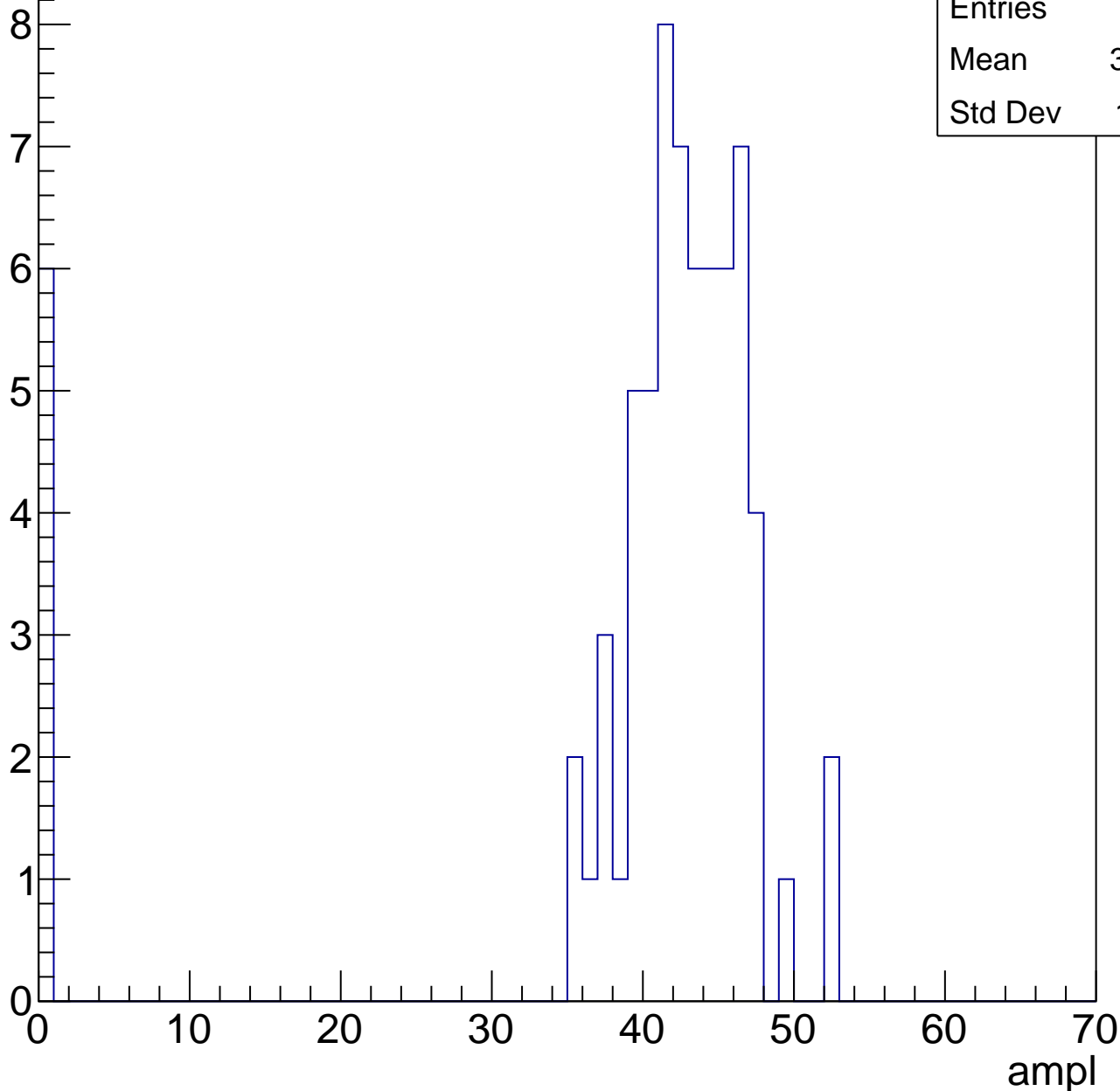
Entries	82
Mean	34.87
Std Dev	5.396

B1L103S, U5-ch63, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	38.96
Std Dev	12.41

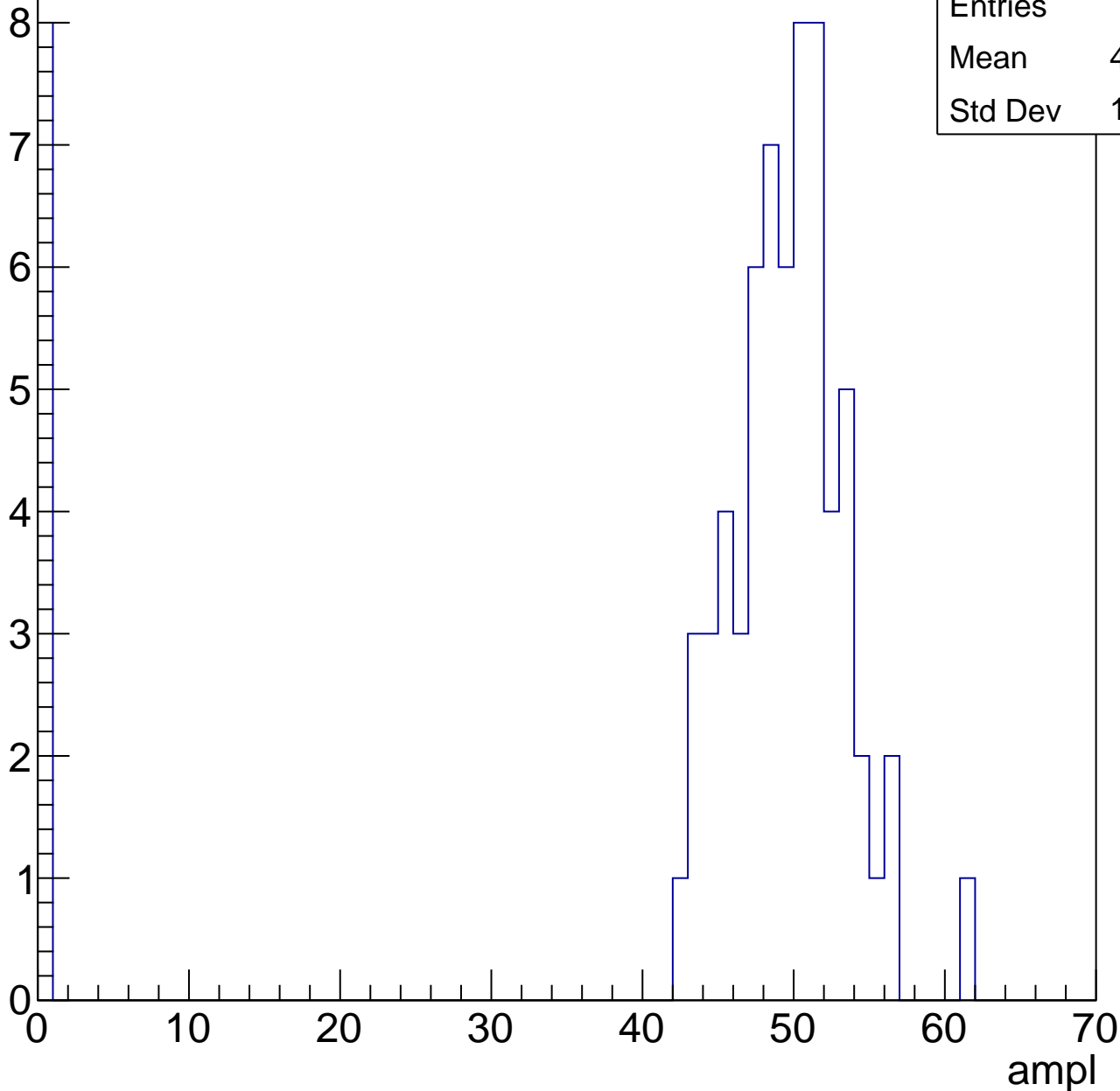


B1L103S, U5-ch63, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	43.75
Std Dev	15.84

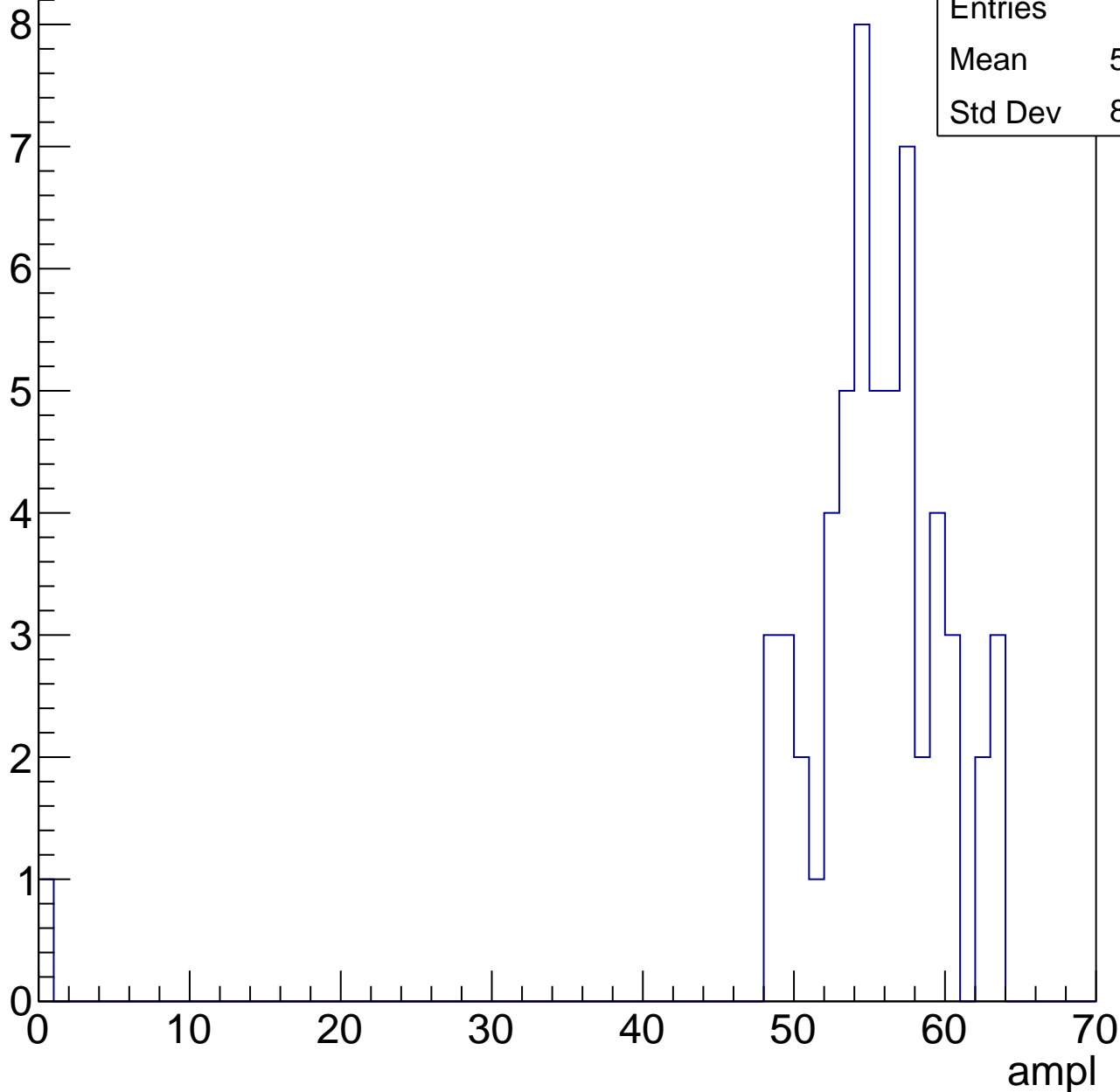


B1L103S, U5-ch63, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	54.24
Std Dev	8.154

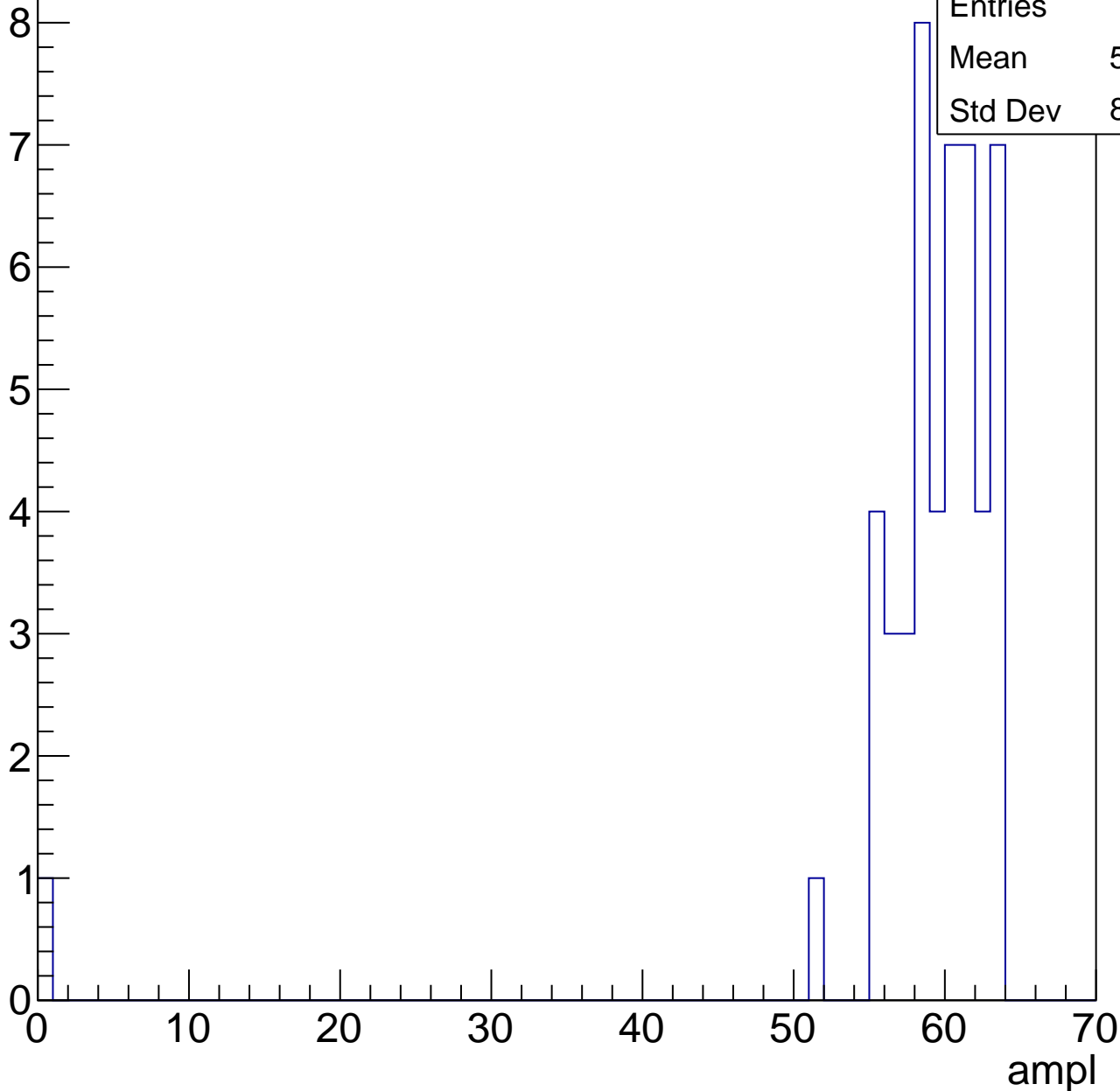


B1L103S, U5-ch63, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

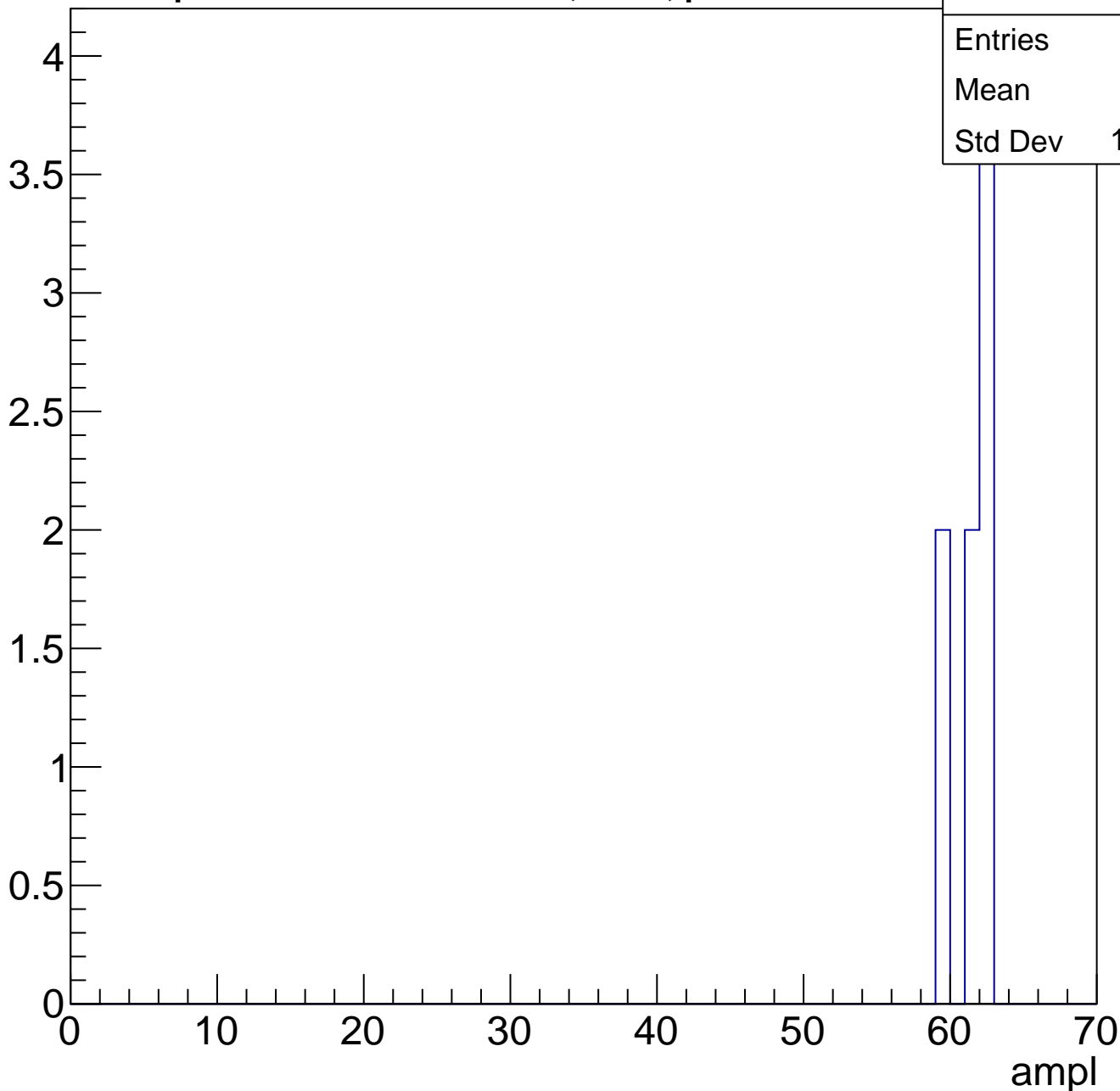
Entries	49
Mean	58.08
Std Dev	8.804



B1L103S, U5-ch63, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch63, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

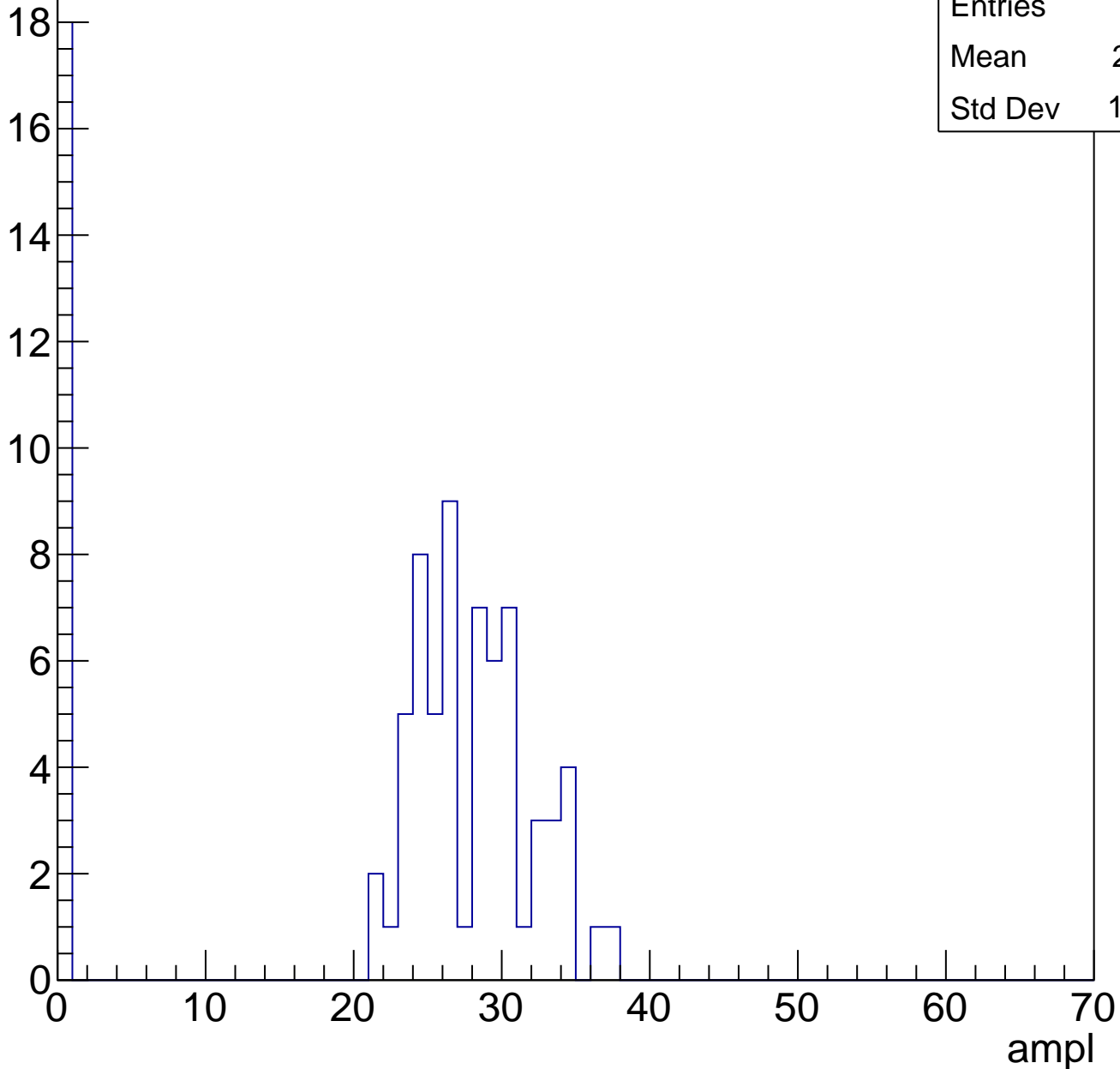


B1L103S, U5-ch64, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	21.61
Std Dev	11.94

Entry

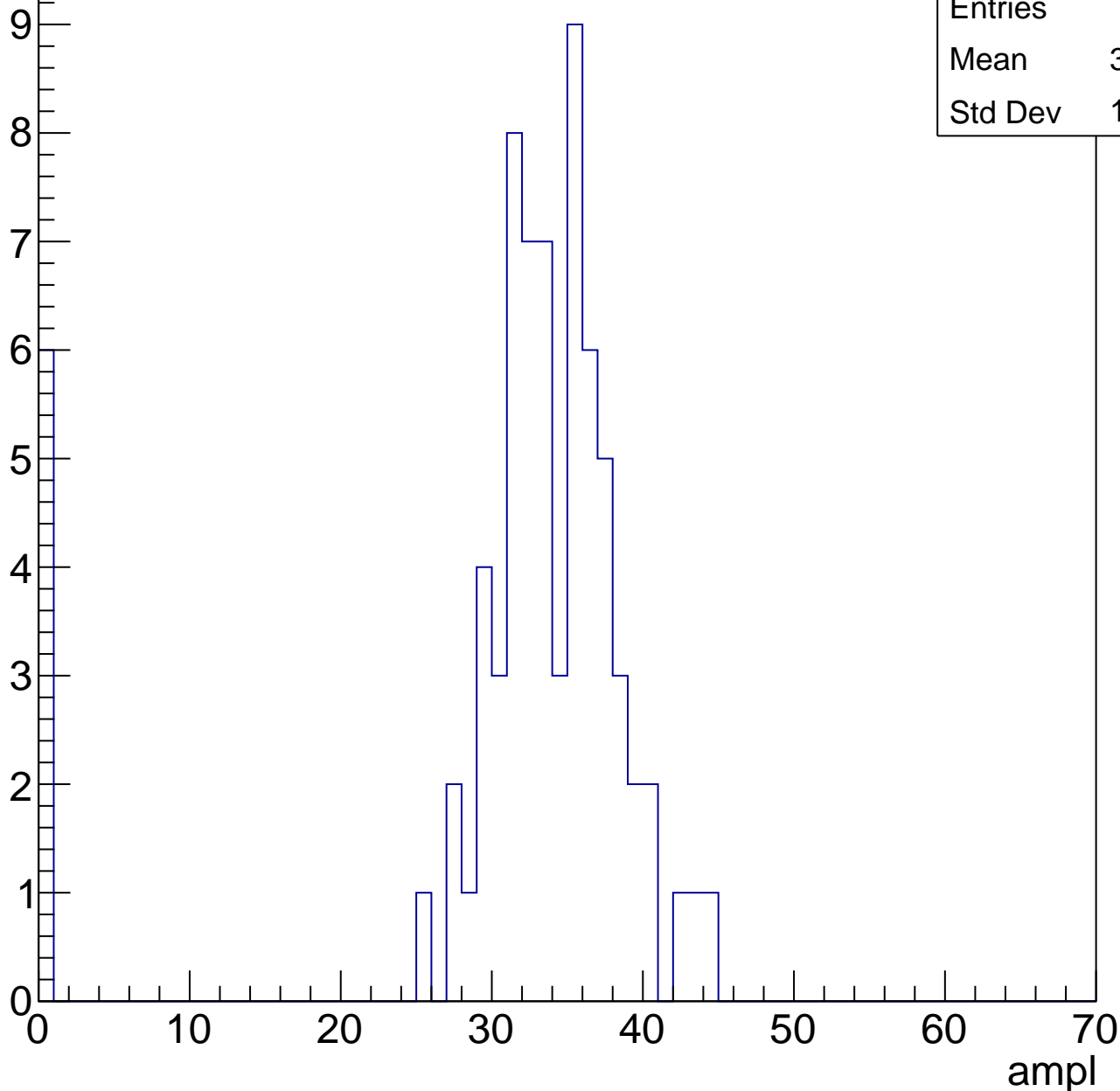


B1L103S, U5-ch64, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	31.04
Std Dev	10.05

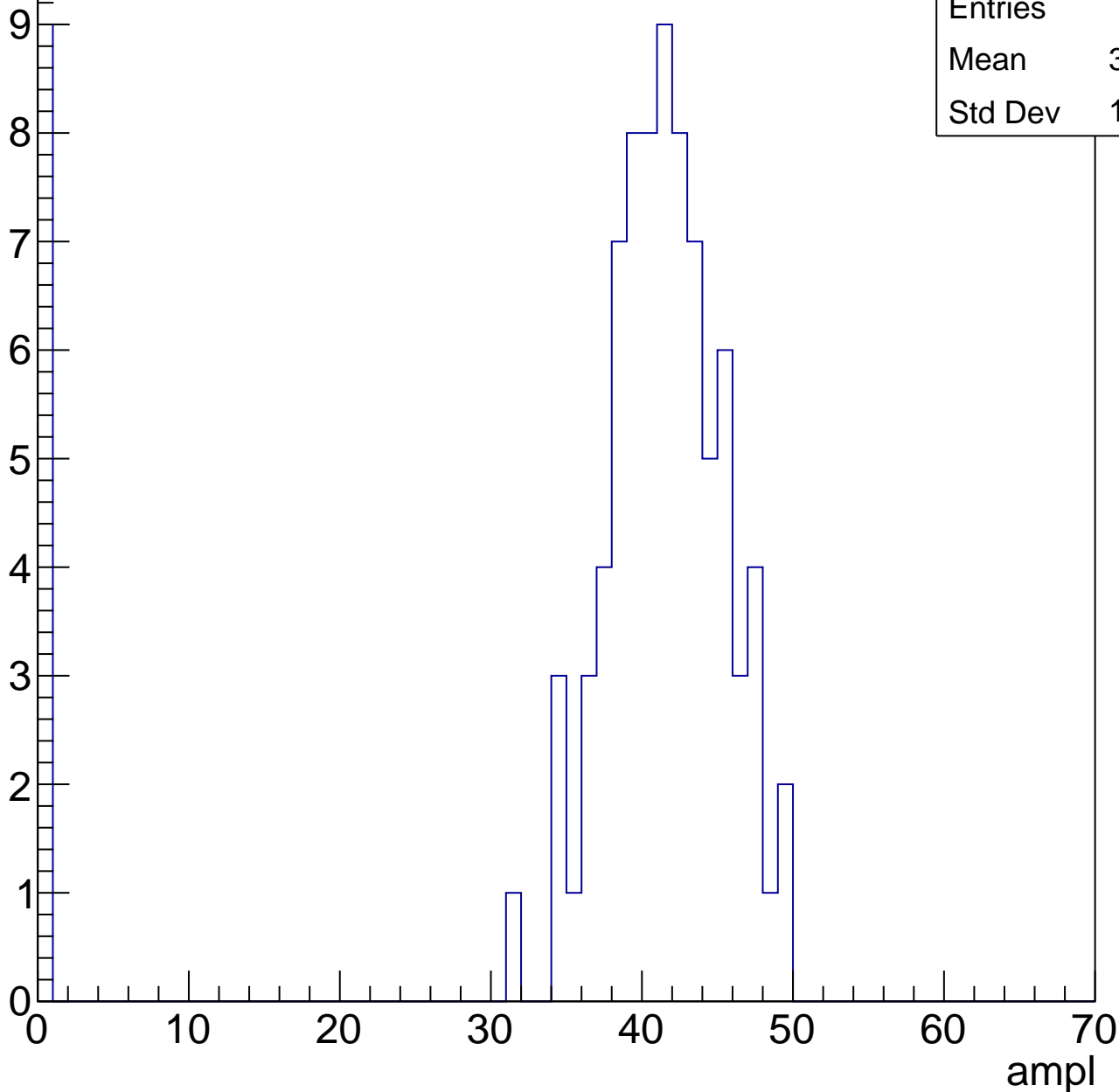


B1L103S, U5-ch64, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	89
Mean	36.97
Std Dev	12.89

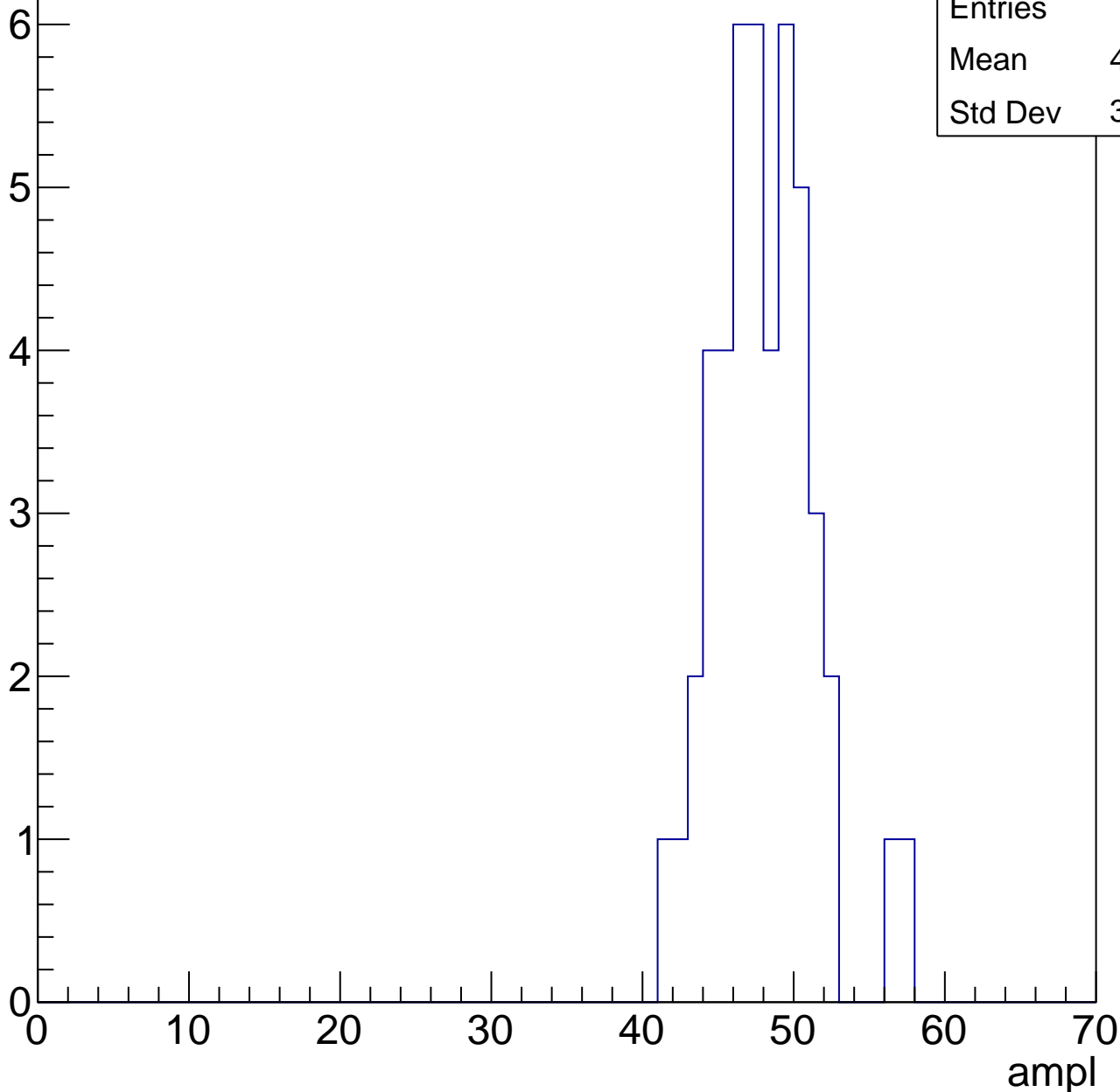


B1L103S, U5-ch64, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	46
Mean	47.59
Std Dev	3.254



B1L103S, U5-ch64, adc4

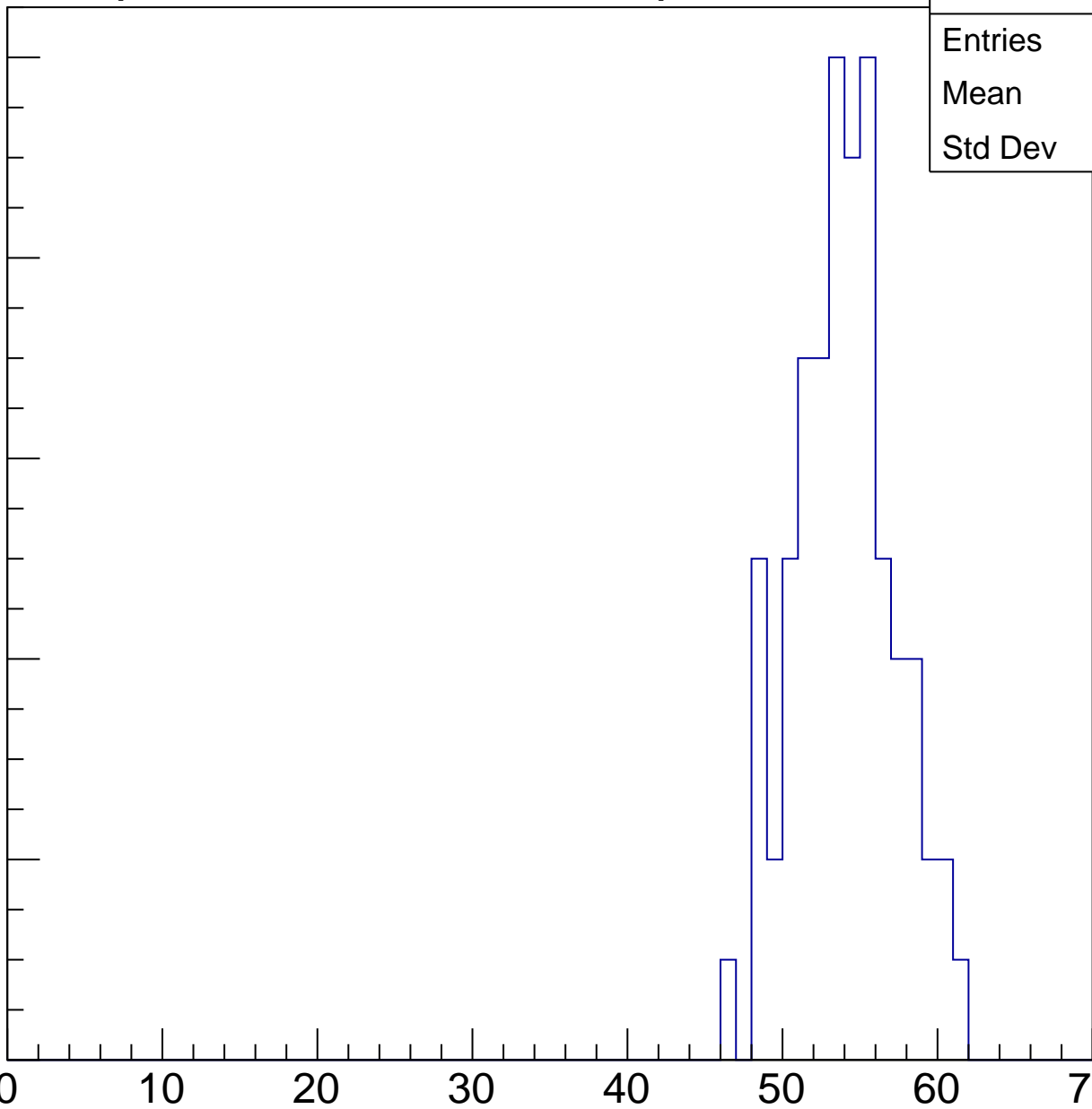
calib_packv5_041523_1651.root, FC#0, port C2

Entry

10
8
6
4
2
0

Entries	74
Mean	53.51
Std Dev	3.202

ampl



B1L103S, U5-ch64, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

7

6

5

4

3

2

1

0

Entries

42

Mean

59.1

Std Dev

2.438

ampl

0

10

20

30

40

50

60

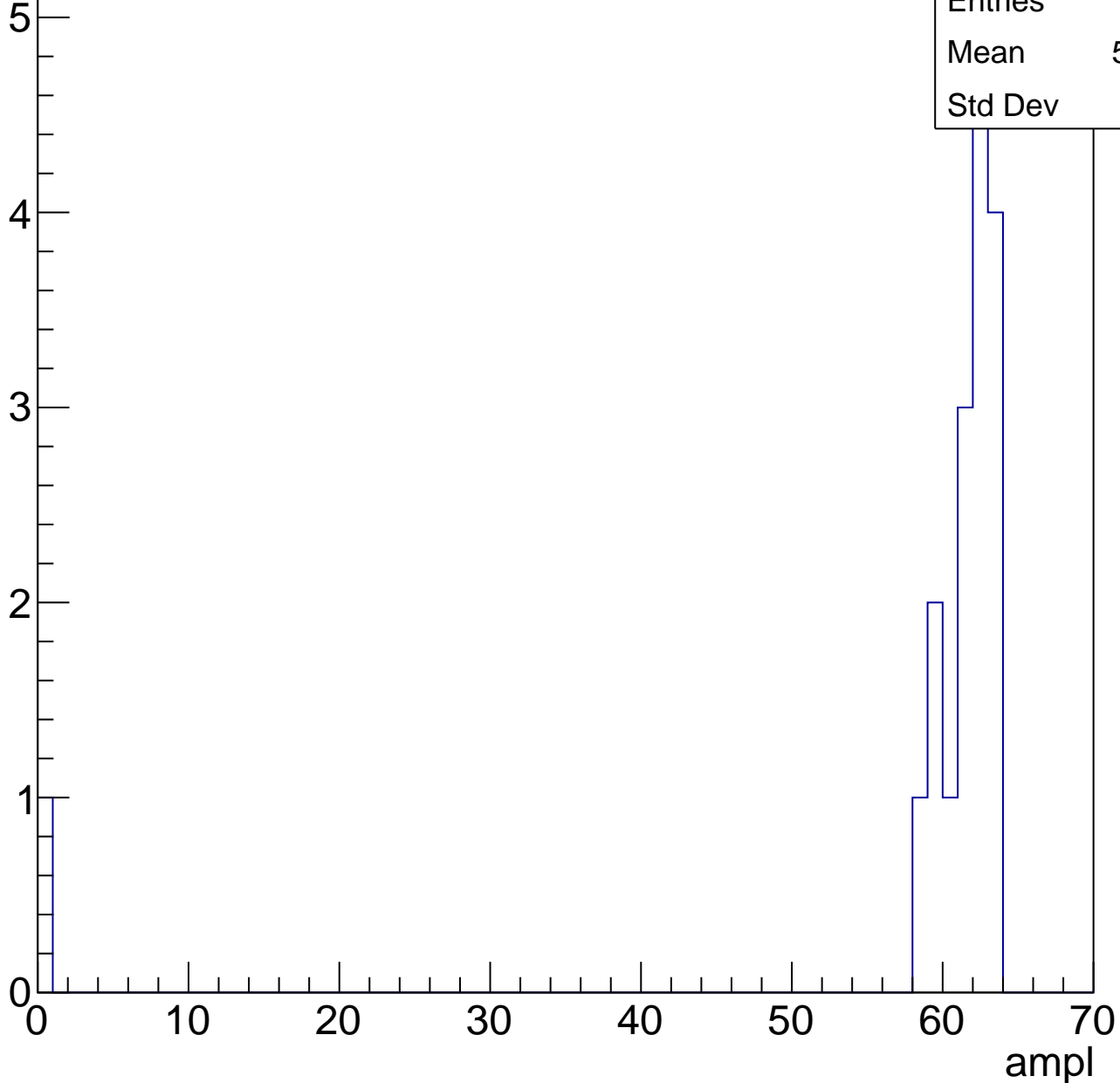
70

B1L103S, U5-ch64, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	17
Mean	57.71
Std Dev	14.5

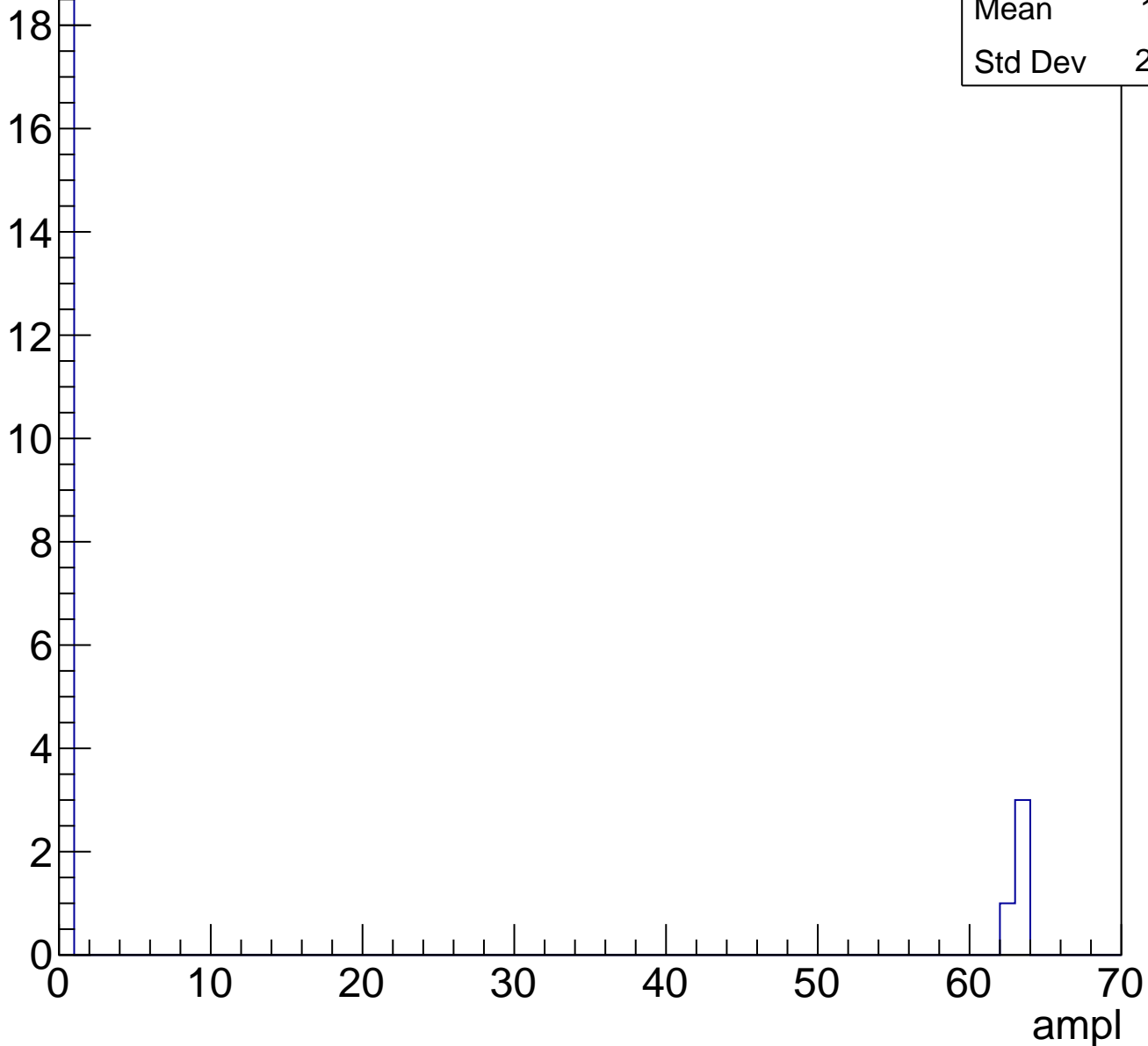


B1L103S, U5-ch64, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	23
Mean	10.91
Std Dev	23.79

Entry

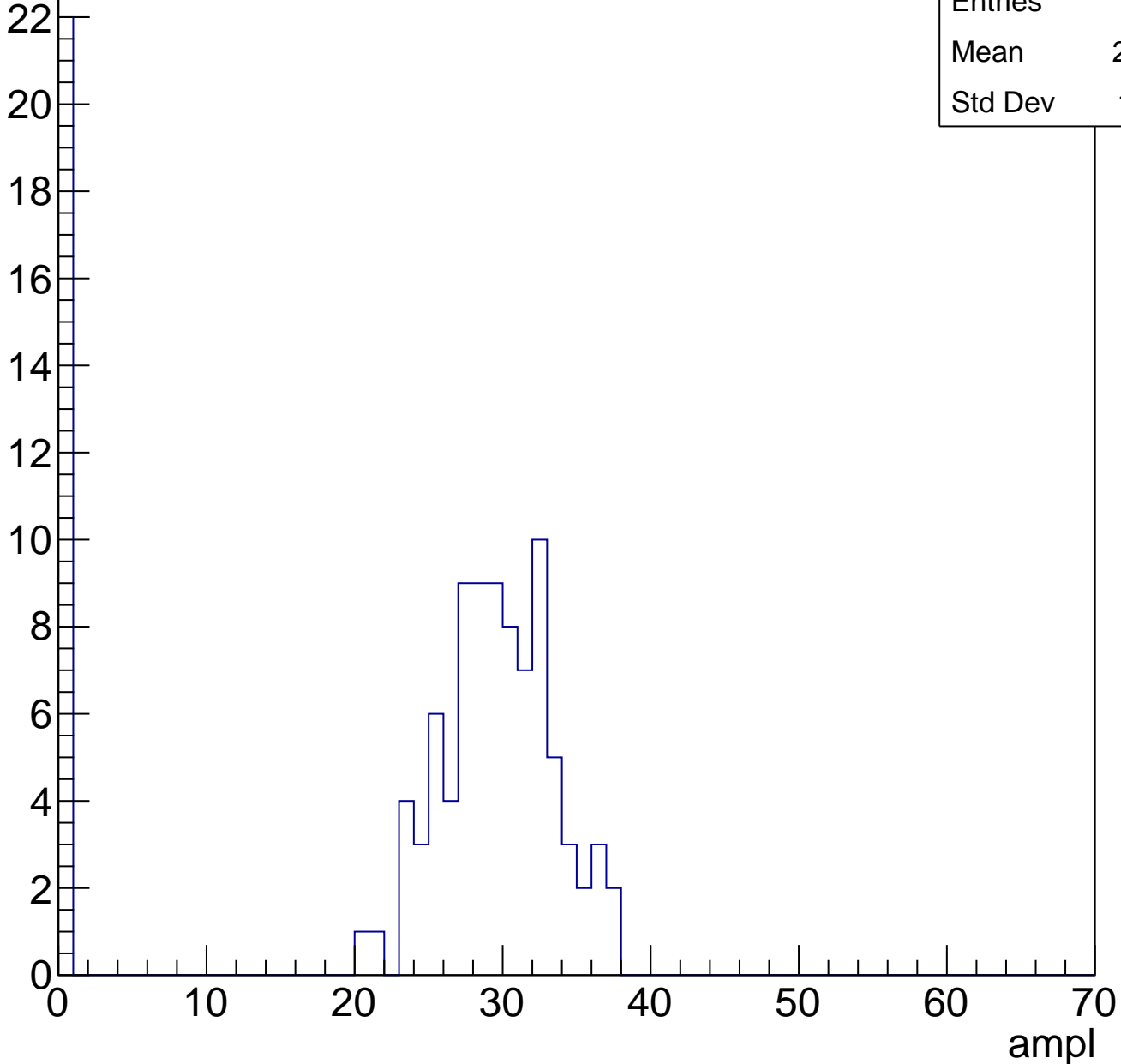


B1L103S, U5-ch65, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	108
Mean	23.25
Std Dev	12.21

Entry

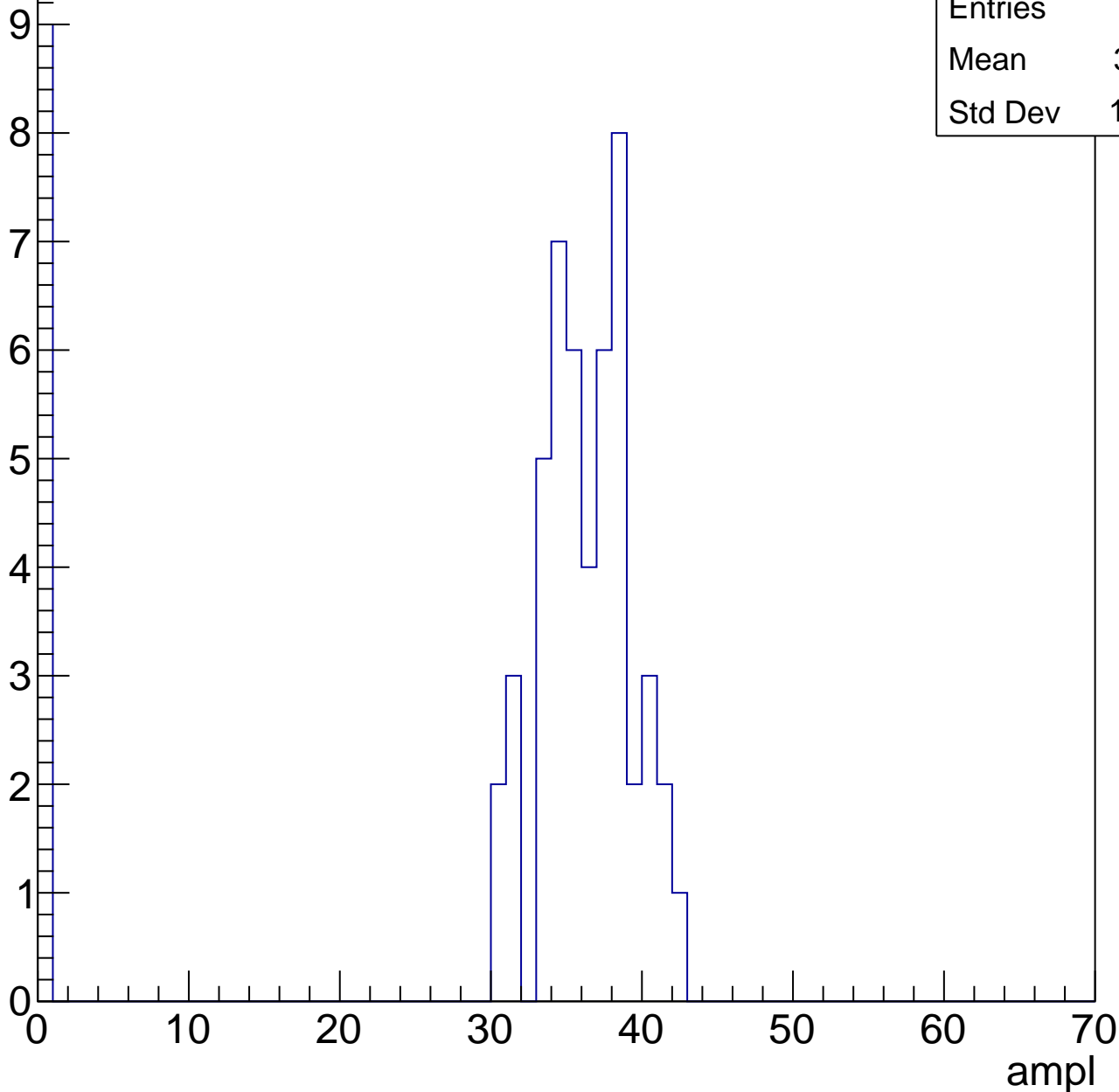


B1L103S, U5-ch65, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	30.31
Std Dev	13.26

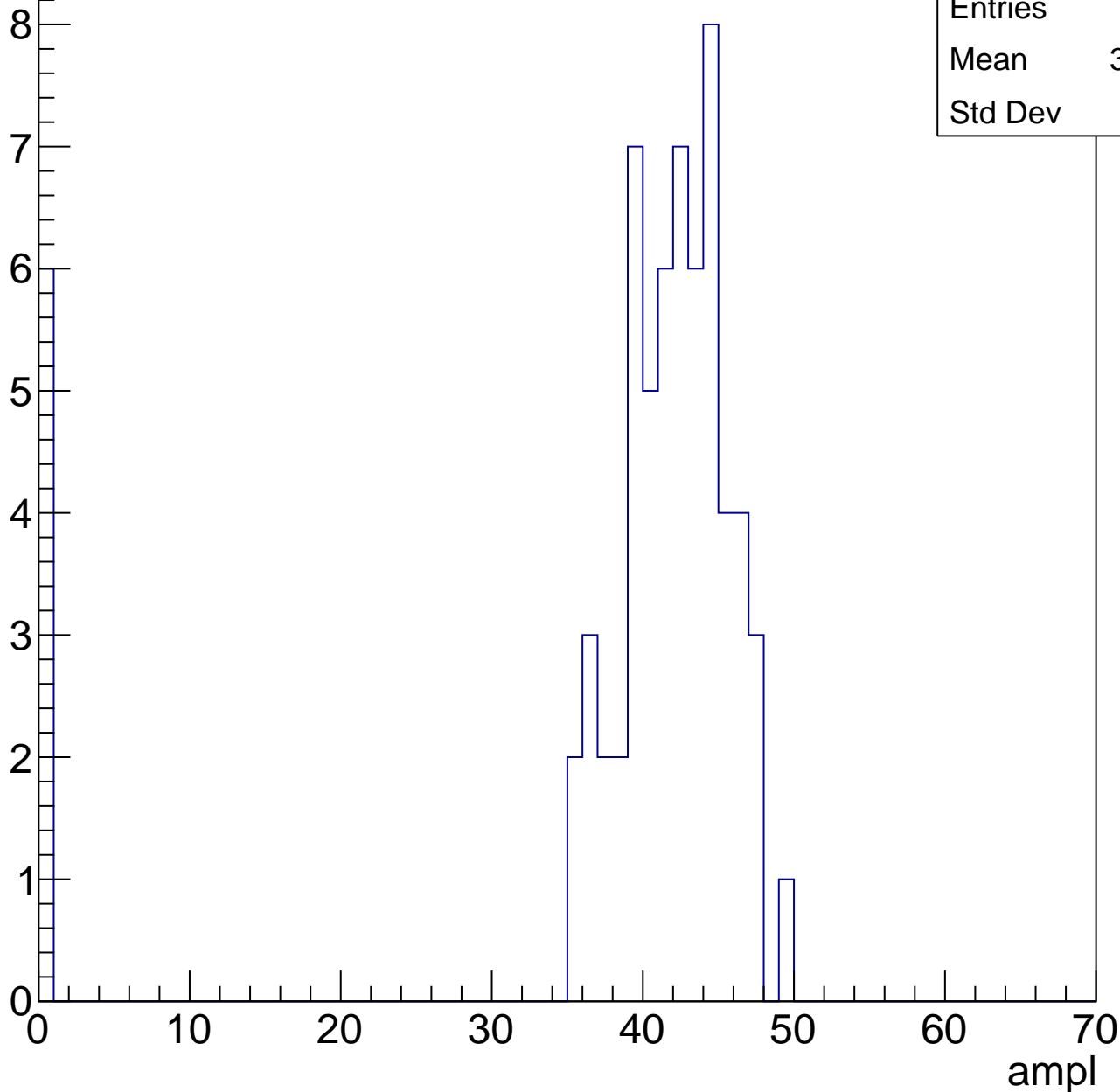


B1L103S, U5-ch65, adc2

calib_packv5_041523_1651.root, FC#0, port C2

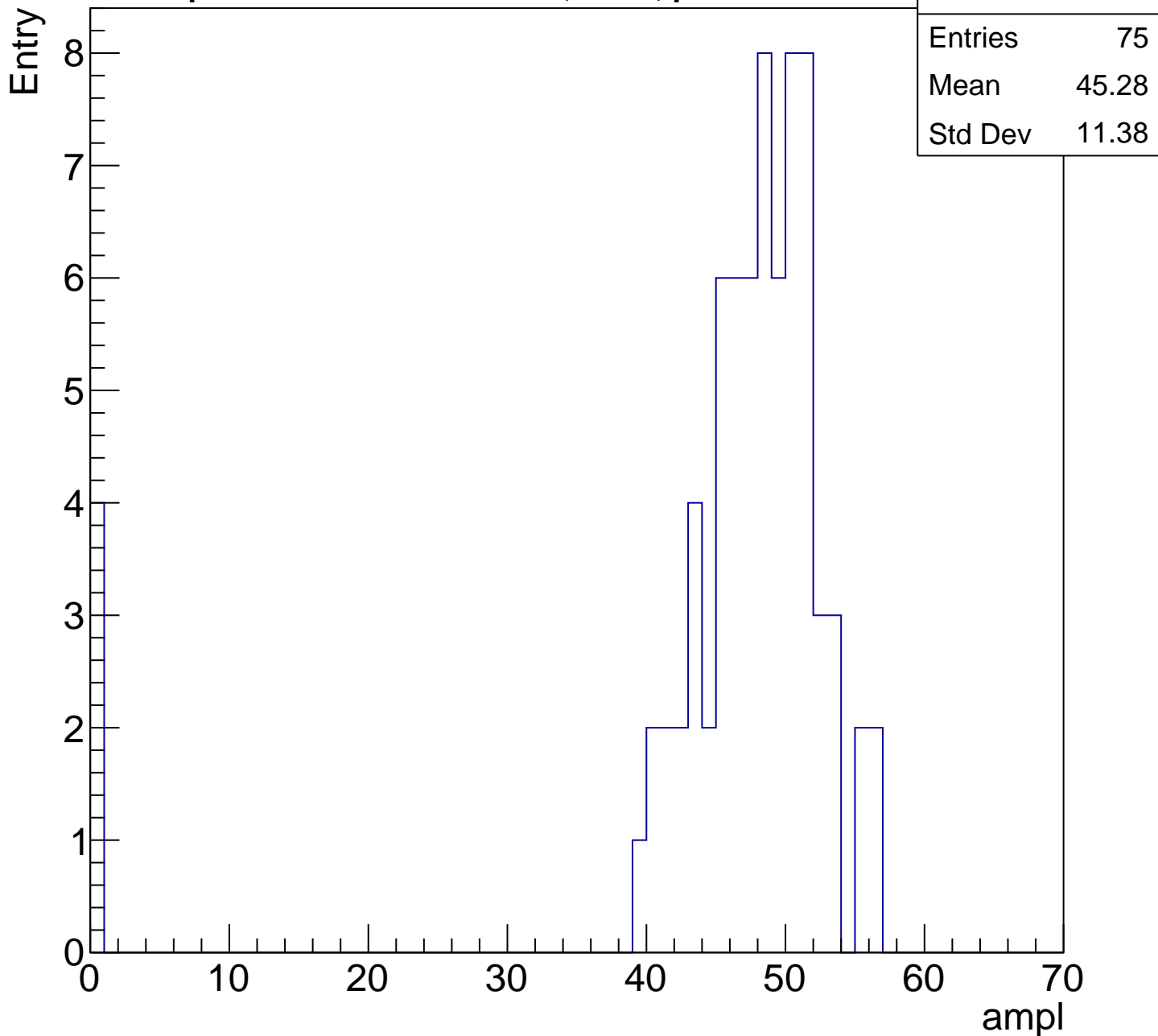
Entry

Entries	66
Mean	37.95
Std Dev	12.4



B1L103S, U5-ch65, adc3

calib_packv5_041523_1651.root, FC#0, port C2

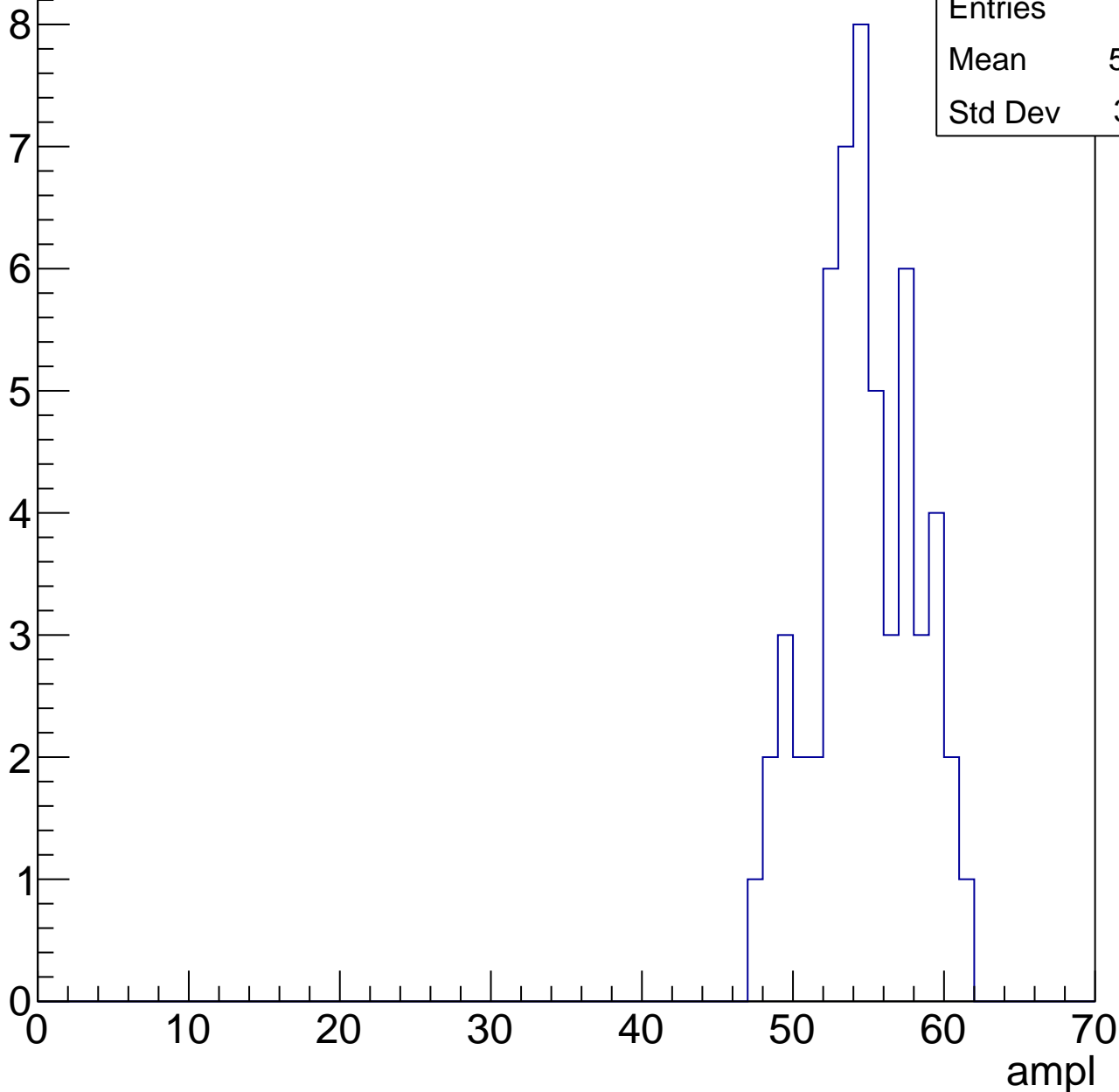


B1L103S, U5-ch65, adc4

calib_packv5_041523_1651.root, FC#0, port C2

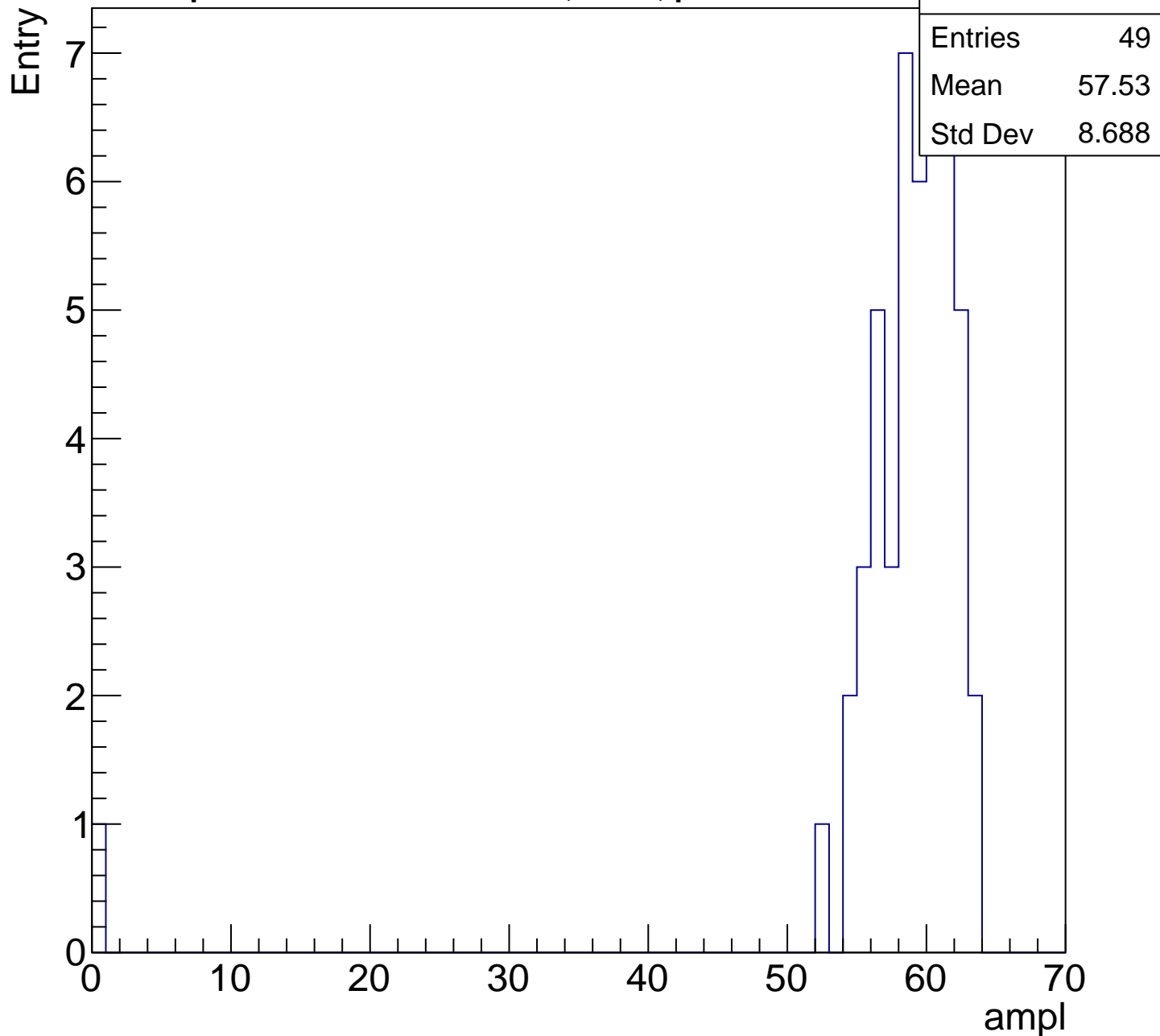
Entry

Entries	55
Mean	54.24
Std Dev	3.341



B1L103S, U5-ch65, adc5

calib_packv5_041523_1651.root, FC#0, port C2

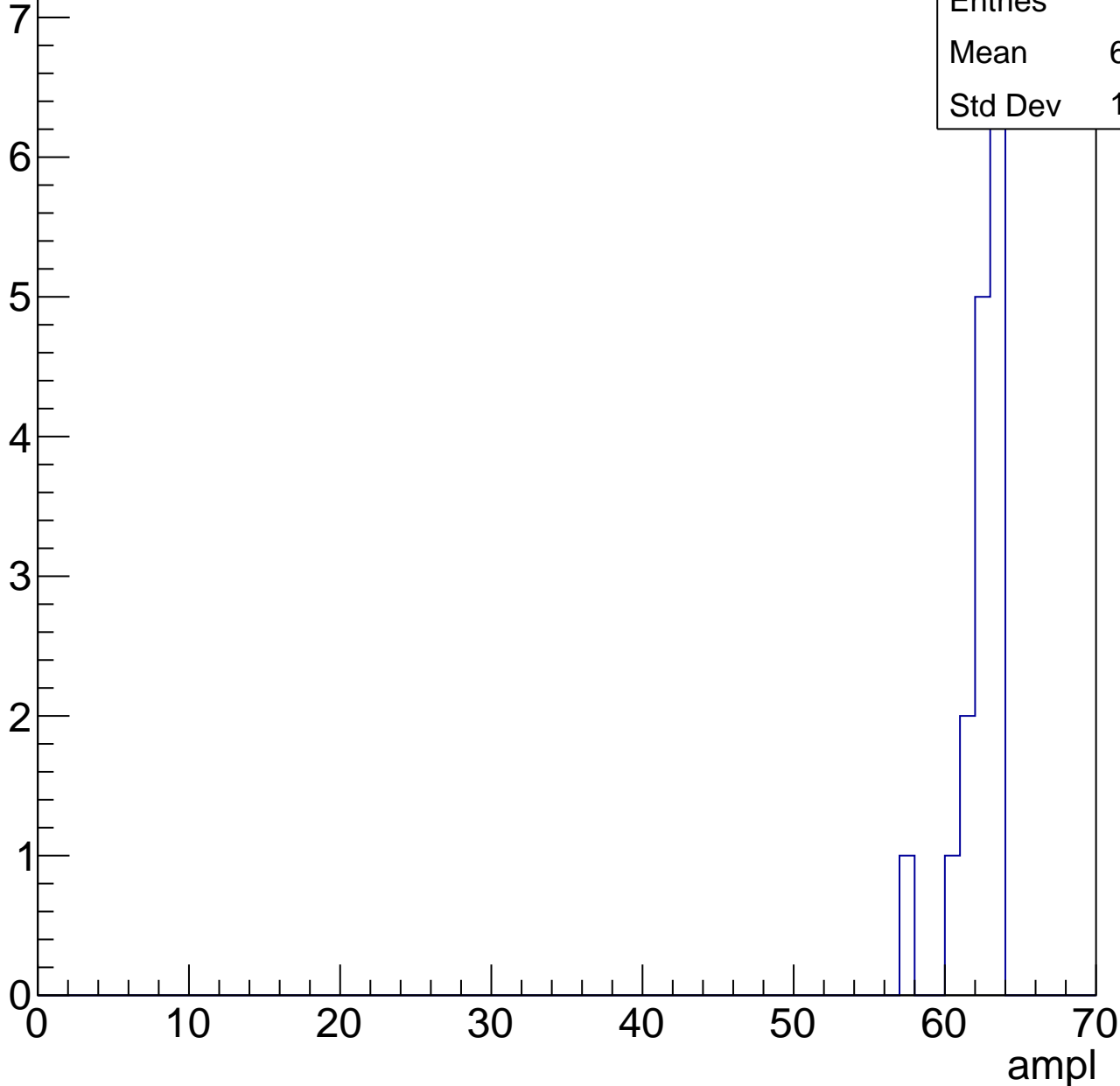


B1L103S, U5-ch65, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	16
Mean	61.88
Std Dev	1.536



B1L103S, U5-ch65, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	20
Mean	3.15
Std Dev	13.73

B1L103S, U5-ch66, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	22.91
Std Dev	9.243

Entry

10

8

6

4

2

0

0

10

20

30

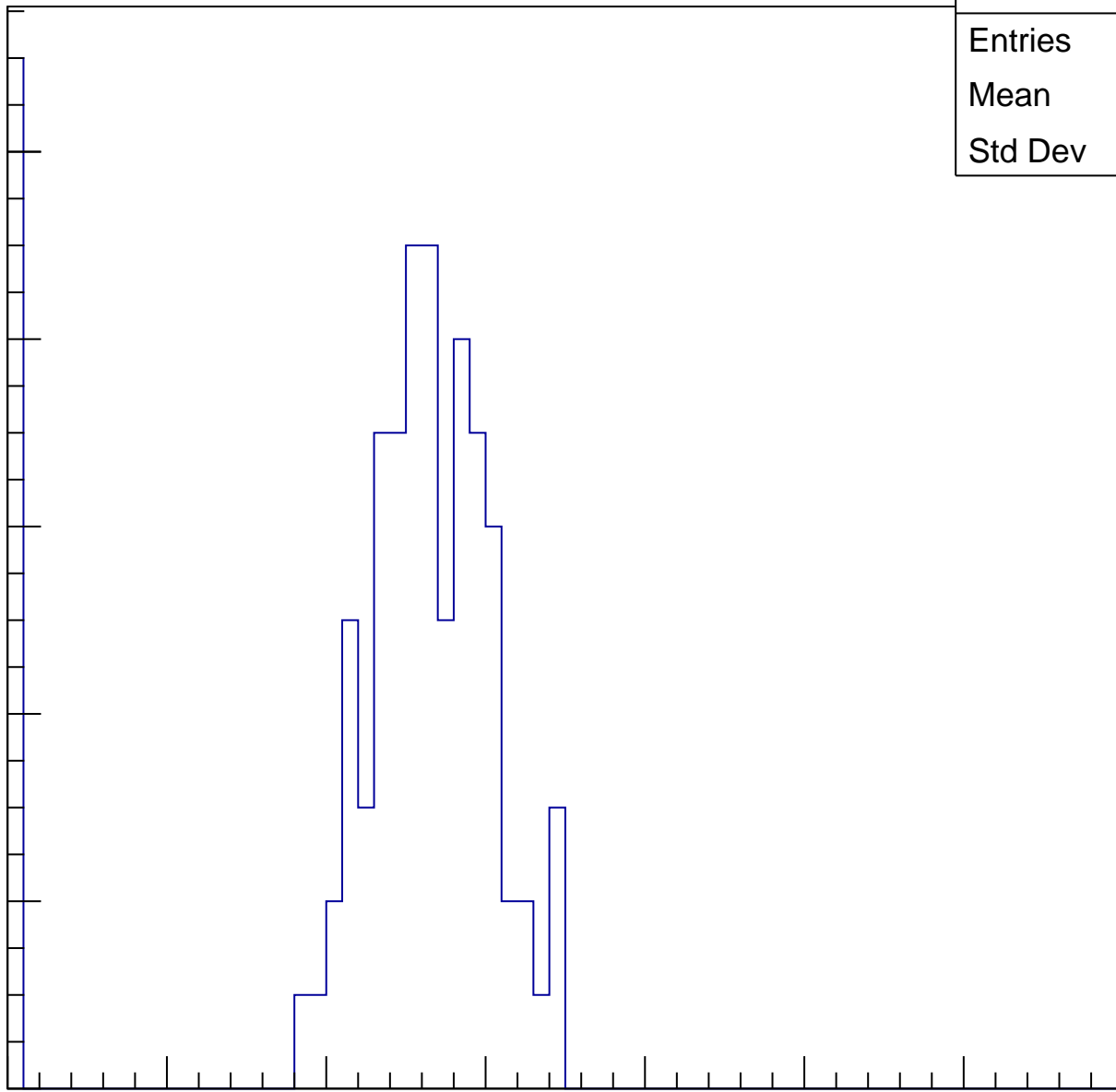
40

50

60

70

ampl

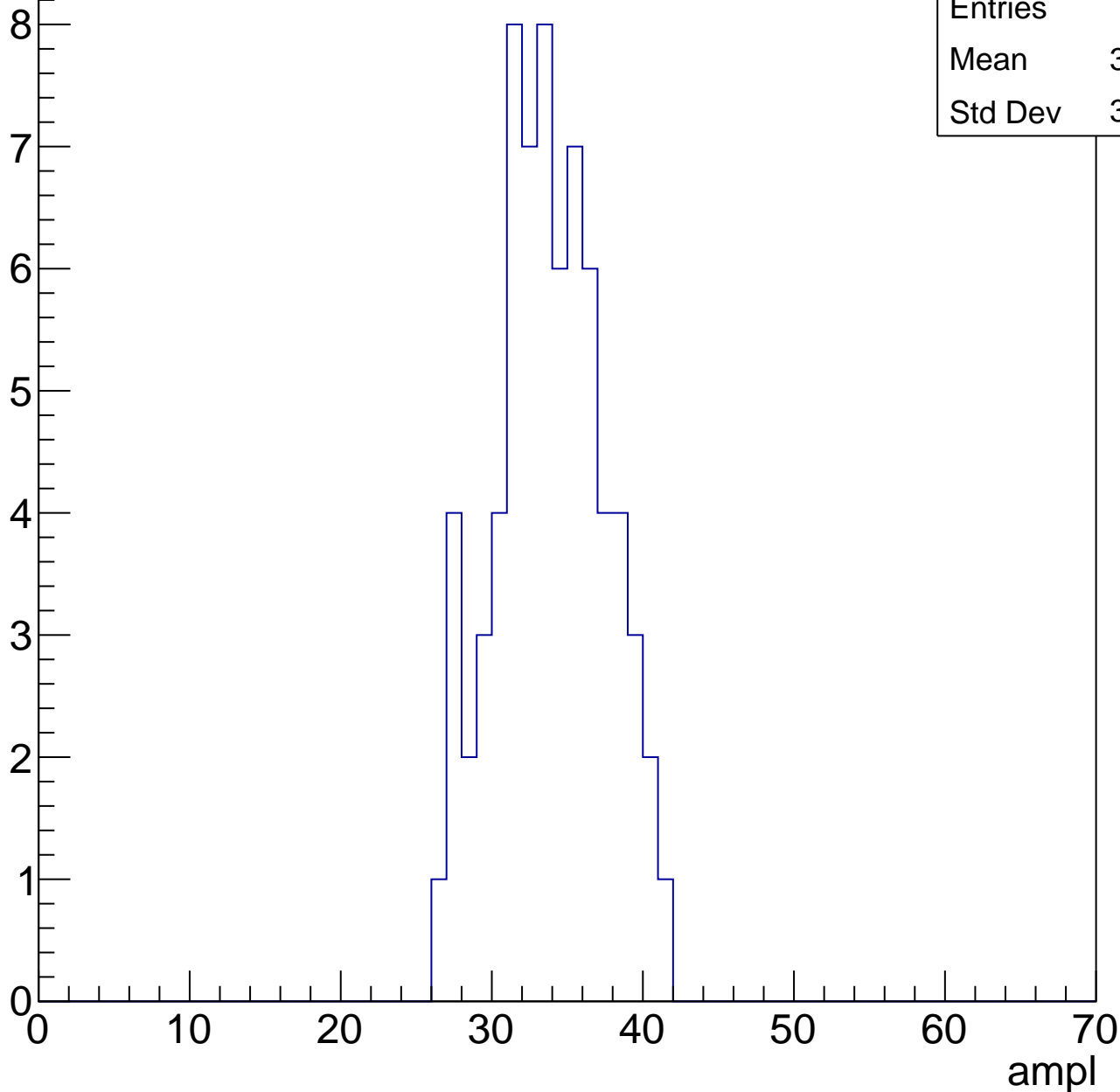


B1L103S, U5-ch66, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	33.37
Std Dev	3.542

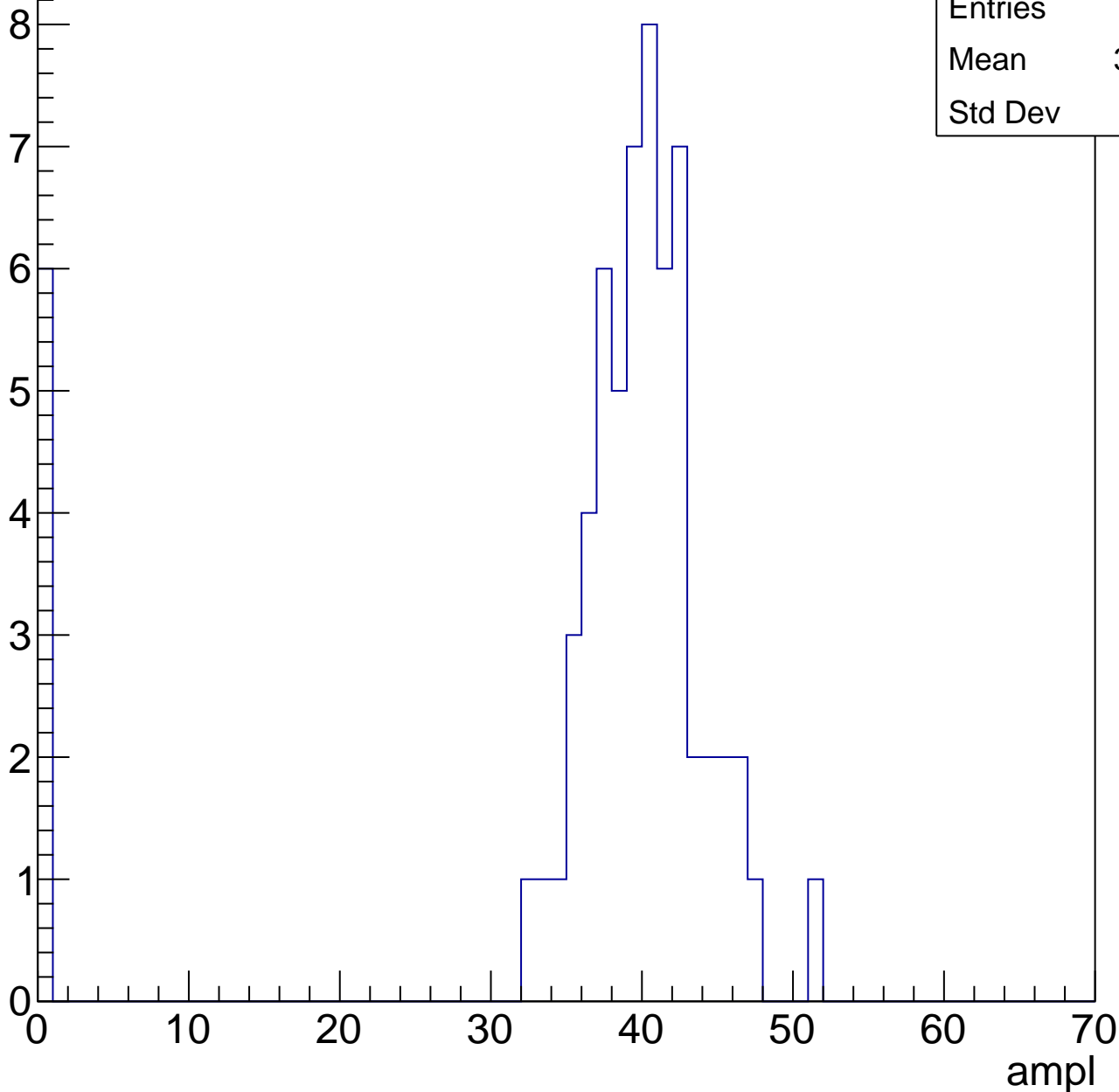


B1L103S, U5-ch66, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	36.11
Std Dev	12

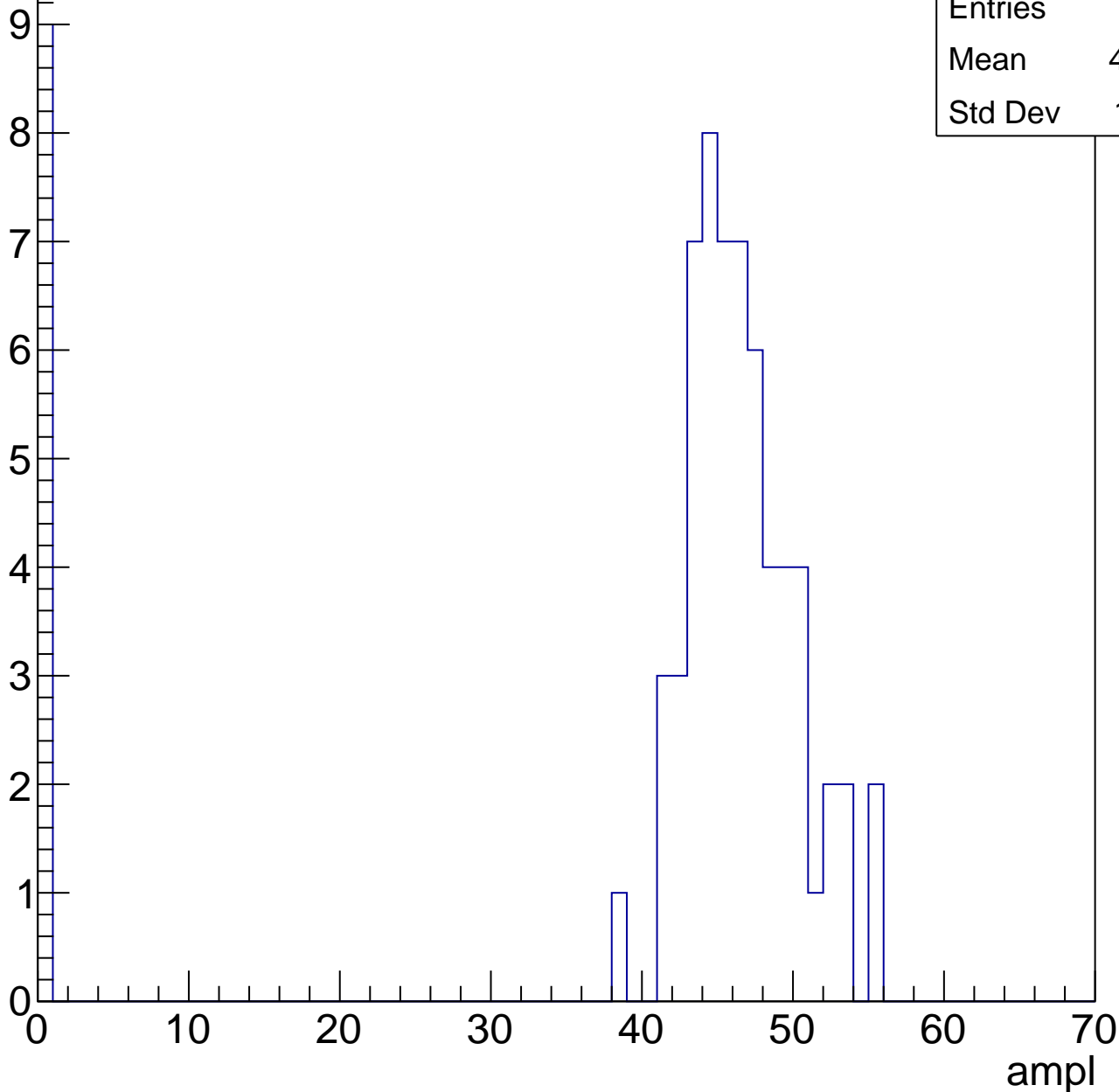


B1L103S, U5-ch66, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	40.26
Std Dev	15.81

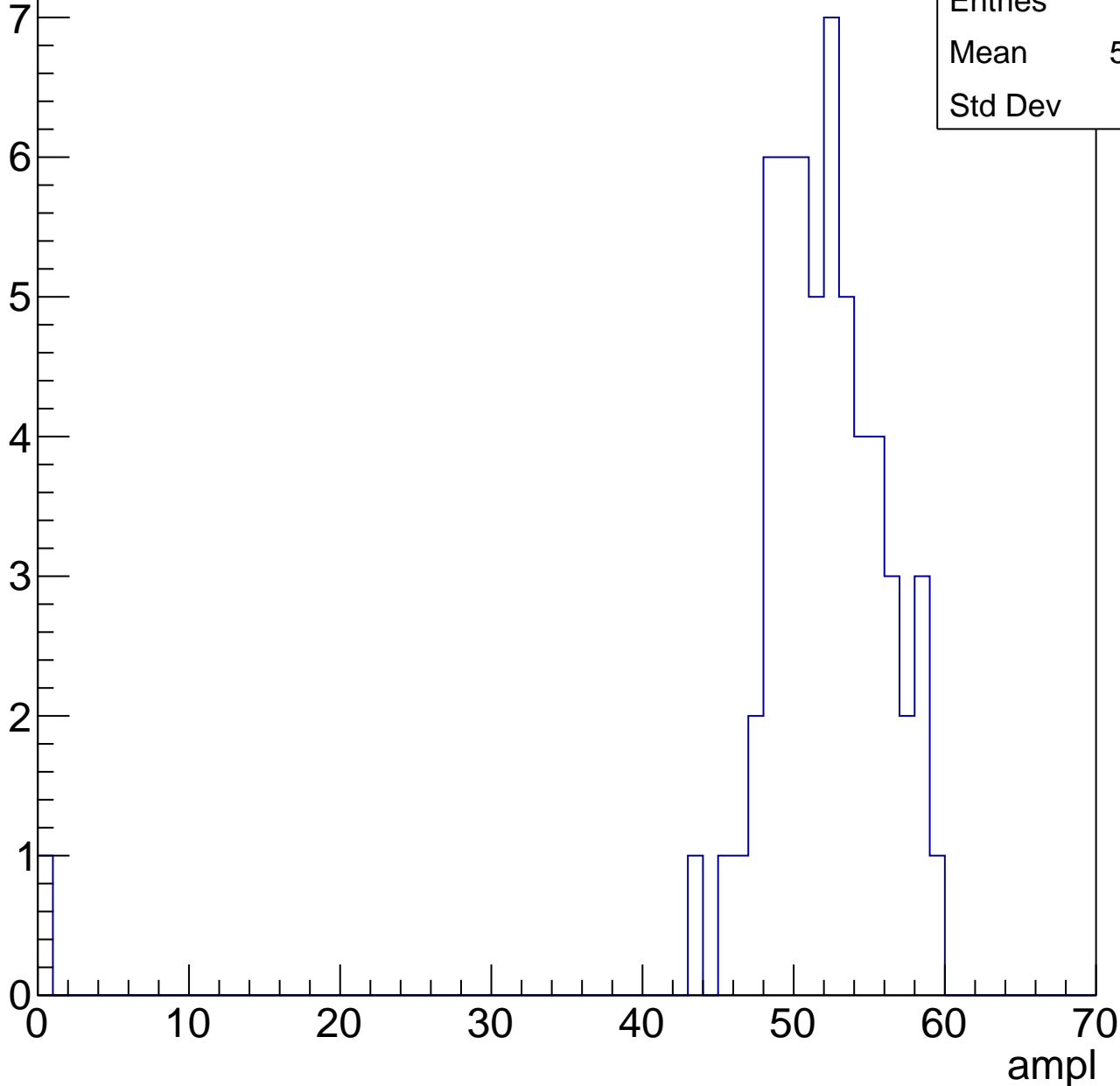


B1L103S, U5-ch66, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	50.78
Std Dev	7.57

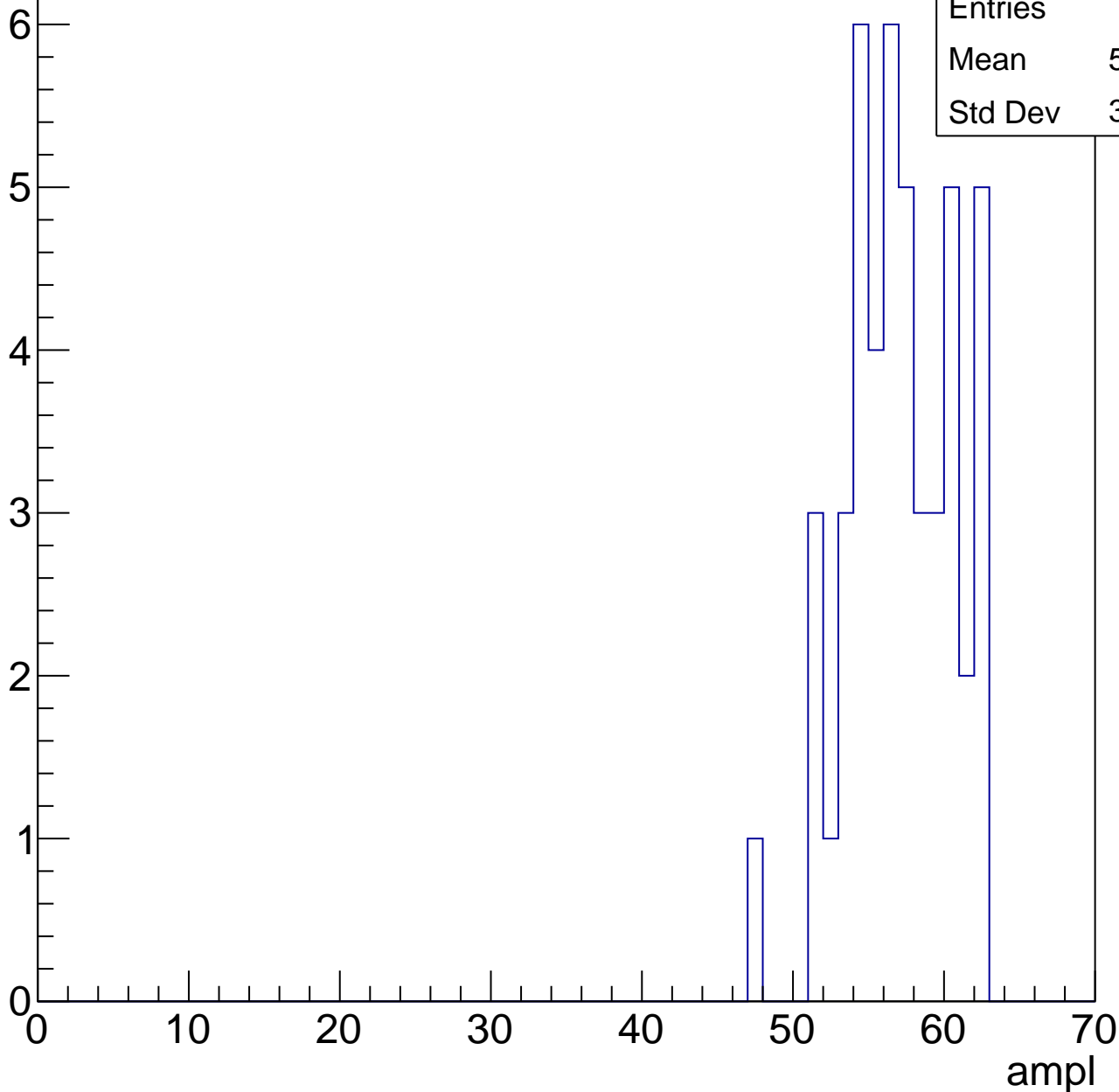


B1L103S, U5-ch66, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	47
Mean	56.57
Std Dev	3.469

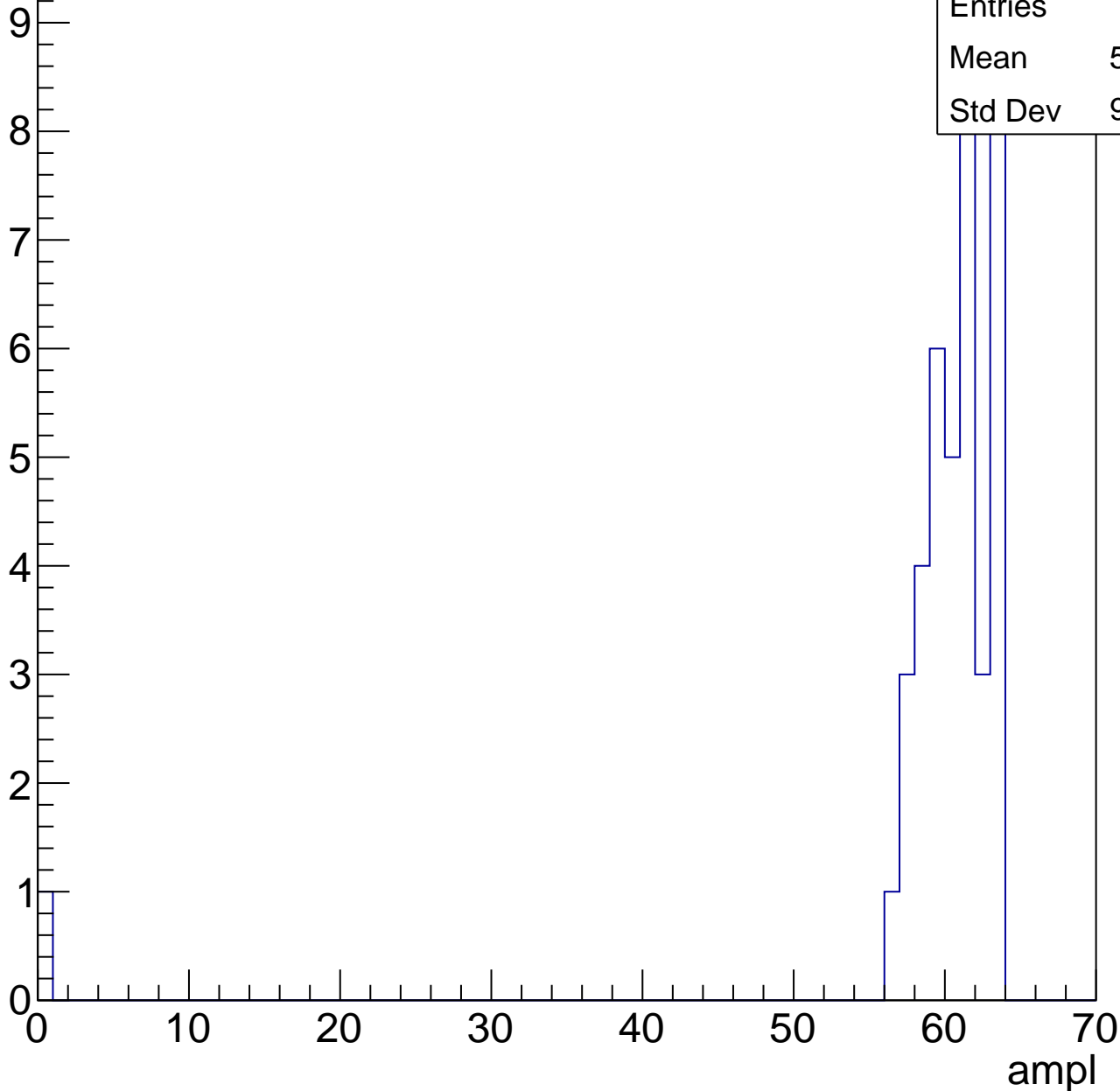


B1L103S, U5-ch66, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	58.85
Std Dev	9.635

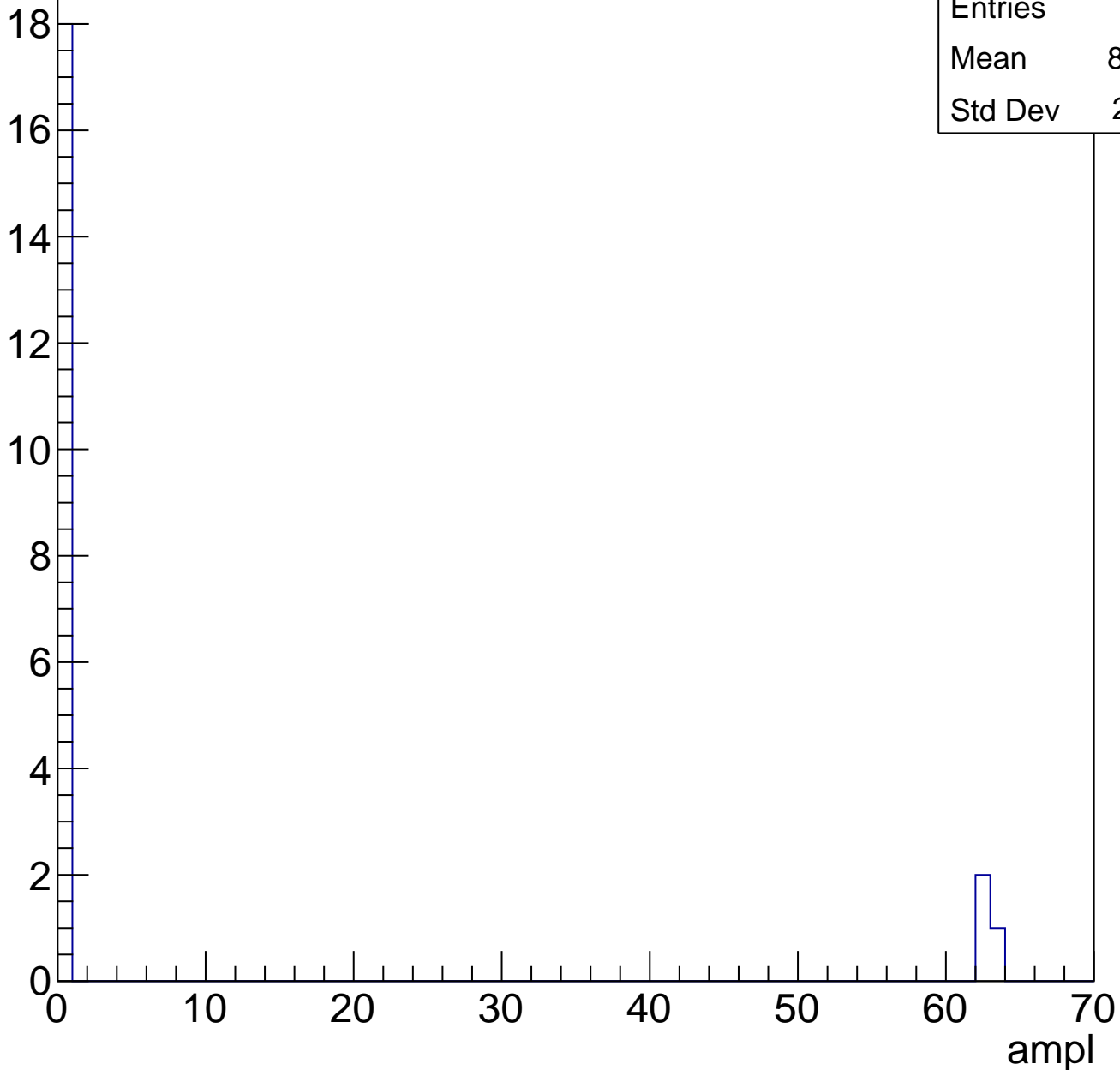


B1L103S, U5-ch66, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	8.905
Std Dev	21.81

Entry

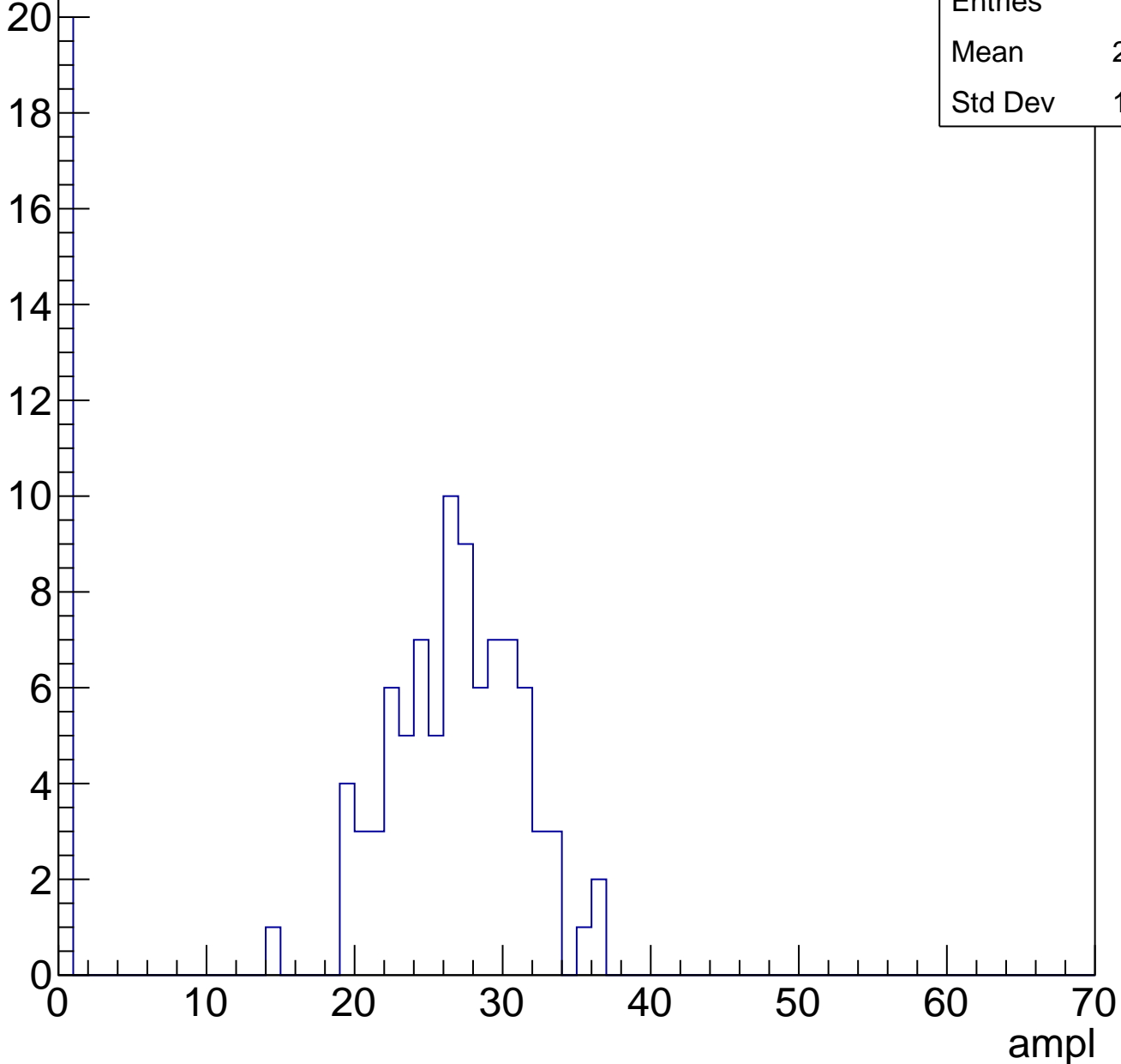


B1L103S, U5-ch67, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	108
Mean	21.53
Std Dev	10.95

Entry

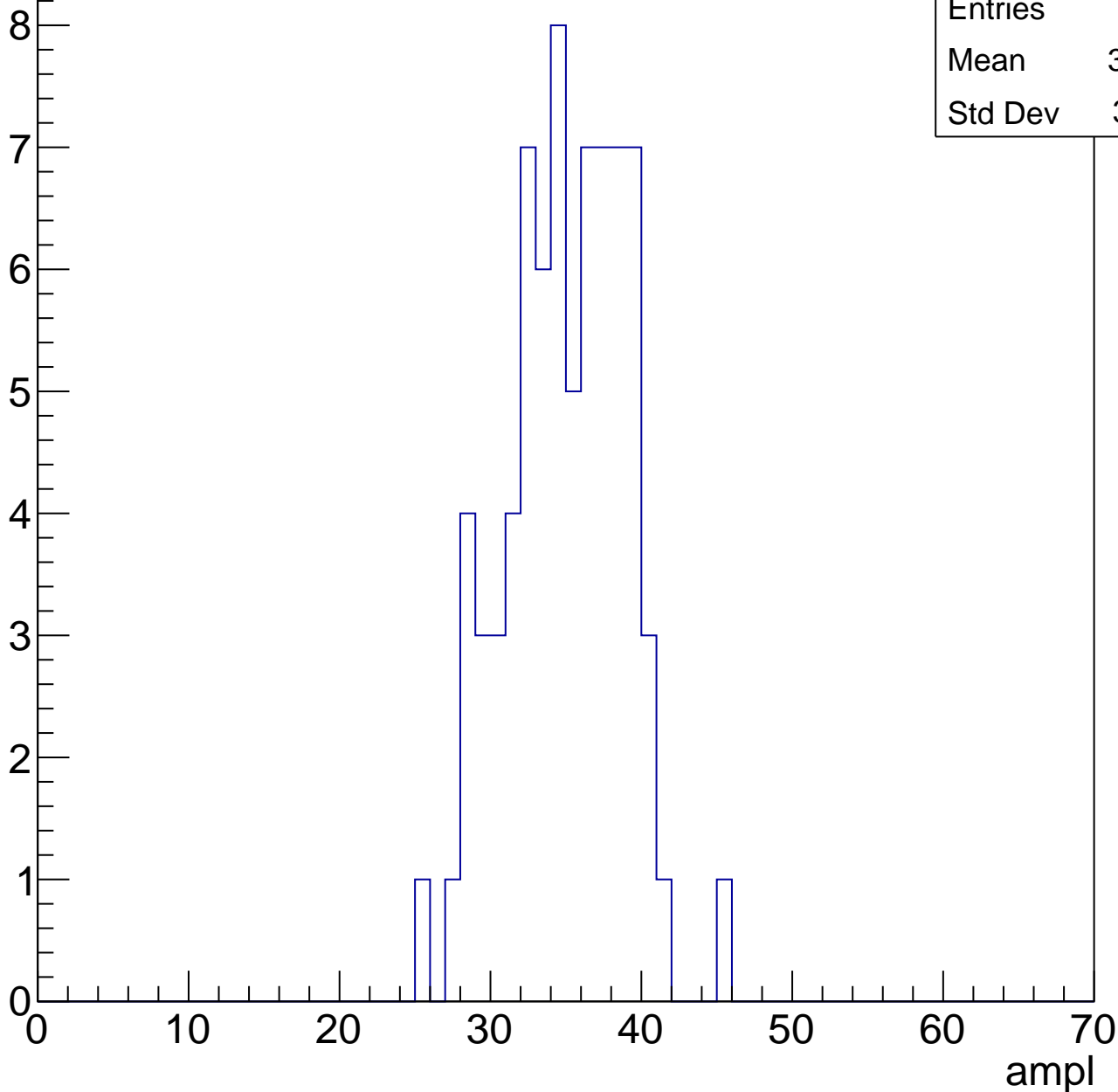


B1L103S, U5-ch67, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	34.53
Std Dev	3.841

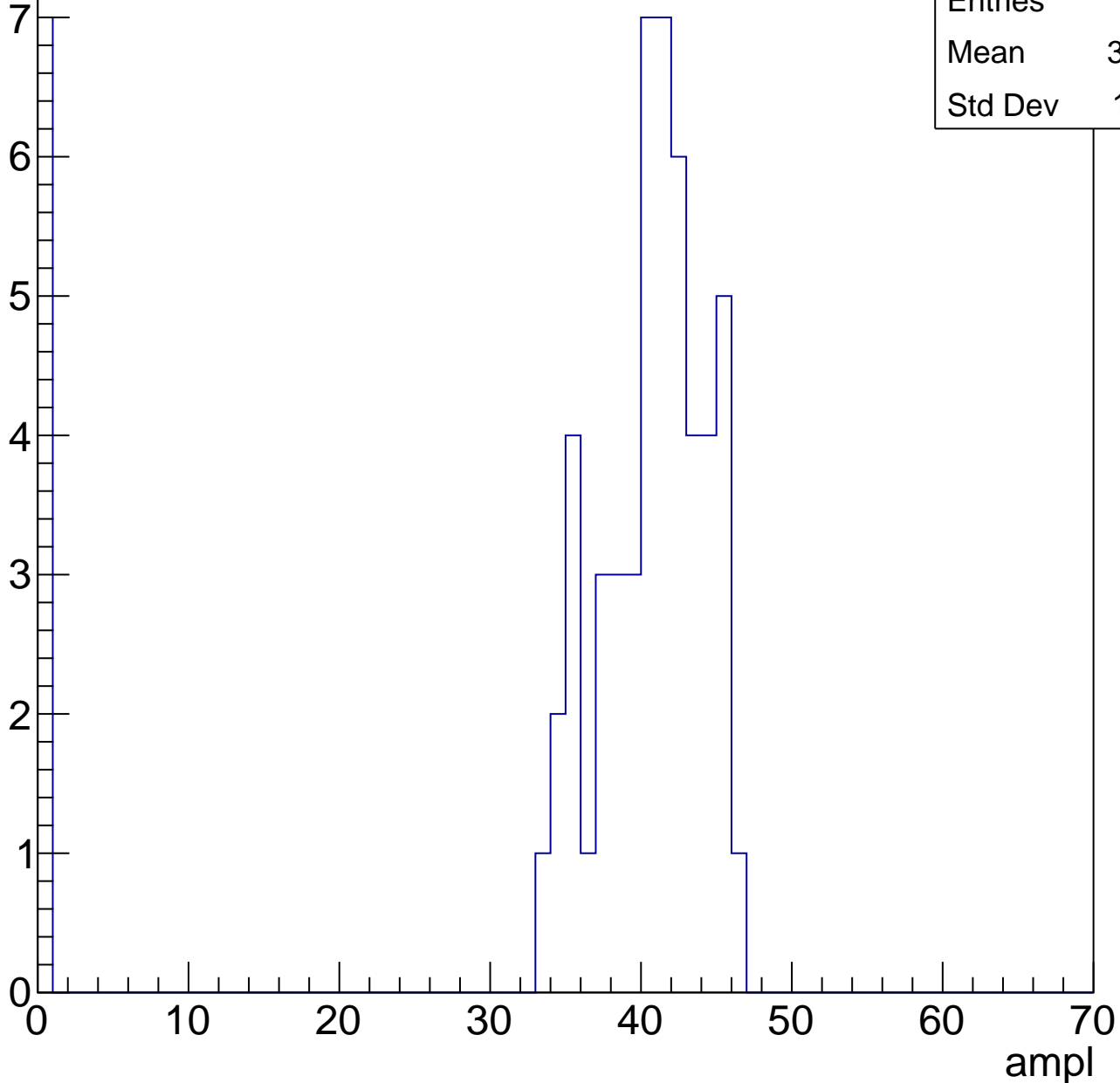


B1L103S, U5-ch67, adc2

calib_packv5_041523_1651.root, FC#0, port C2

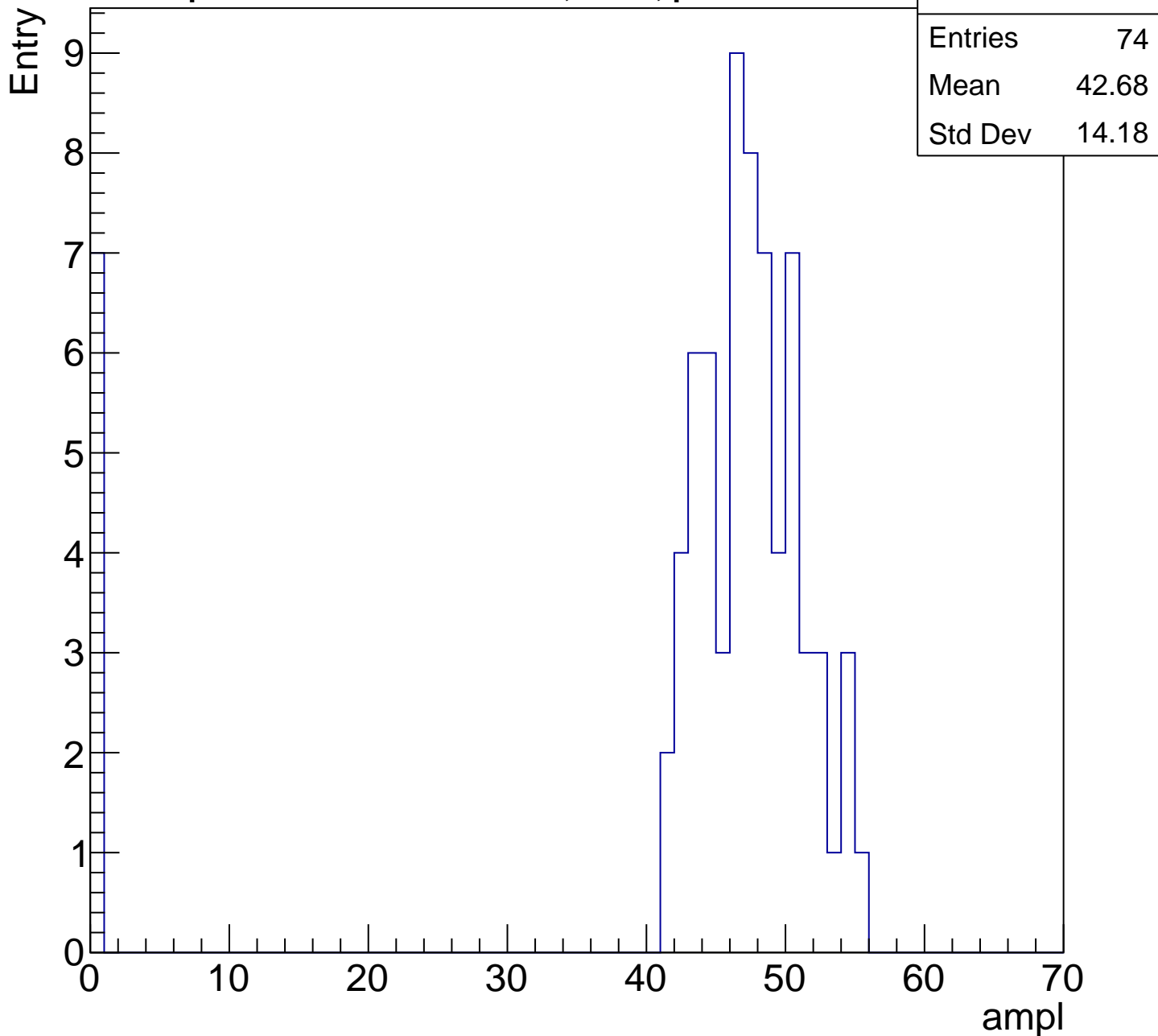
Entry

Entries	58
Mean	35.47
Std Dev	13.51



B1L103S, U5-ch67, adc3

calib_packv5_041523_1651.root, FC#0, port C2

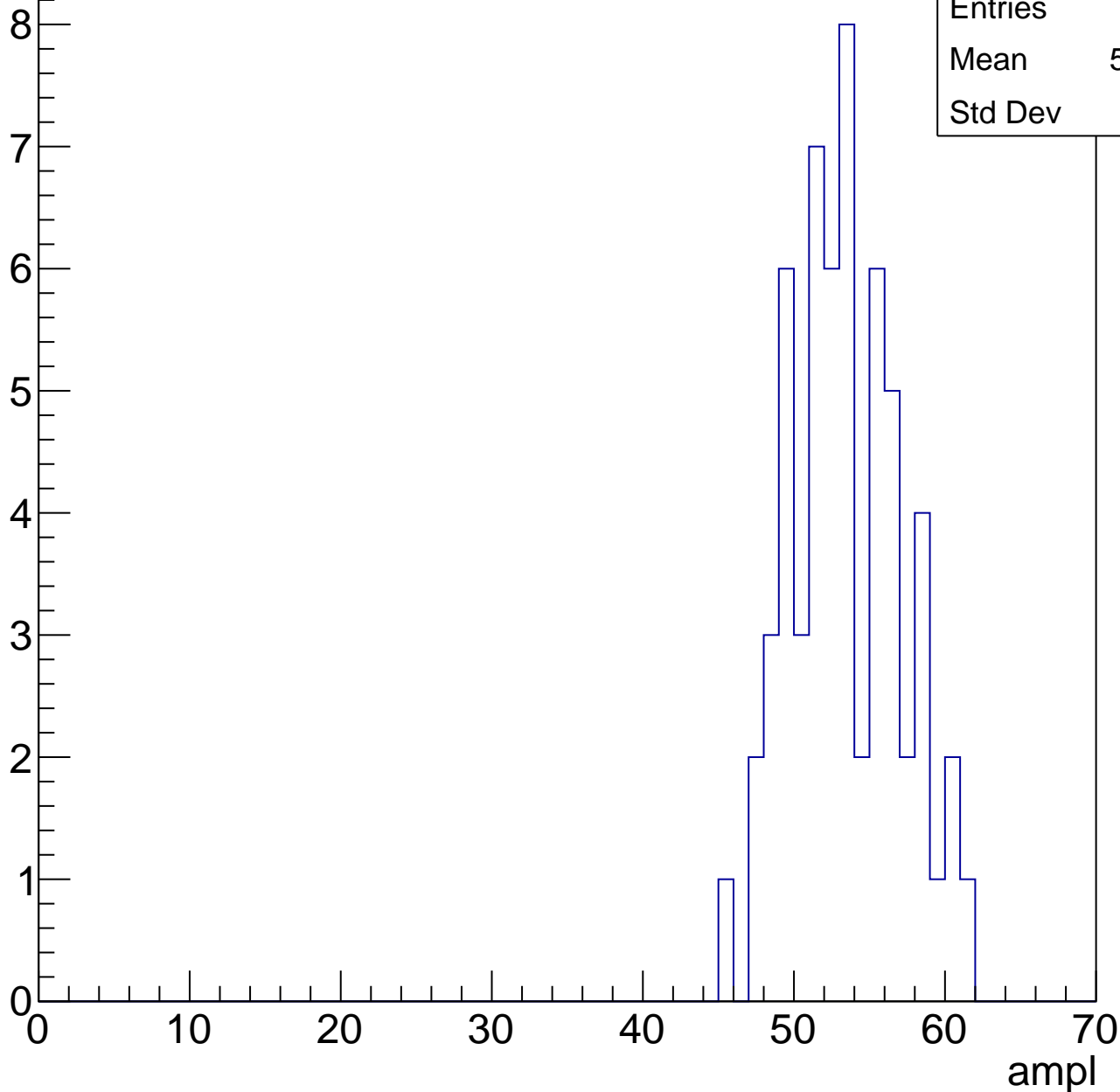


B1L103S, U5-ch67, adc4

calib_packv5_041523_1651.root, FC#0, port C2

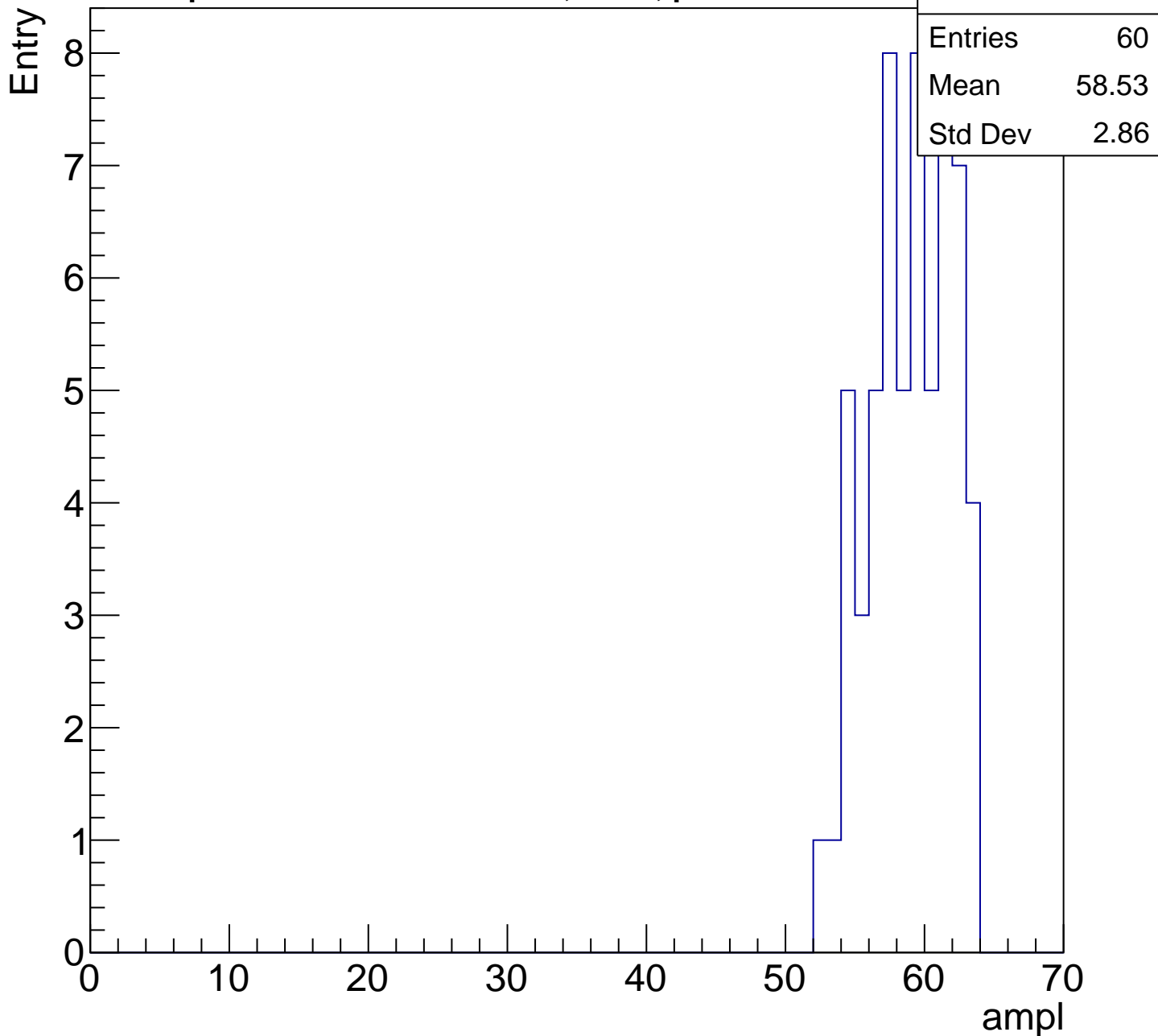
Entry

Entries	59
Mean	52.95
Std Dev	3.61



B1L103S, U5-ch67, adc5

calib_packv5_041523_1651.root, FC#0, port C2

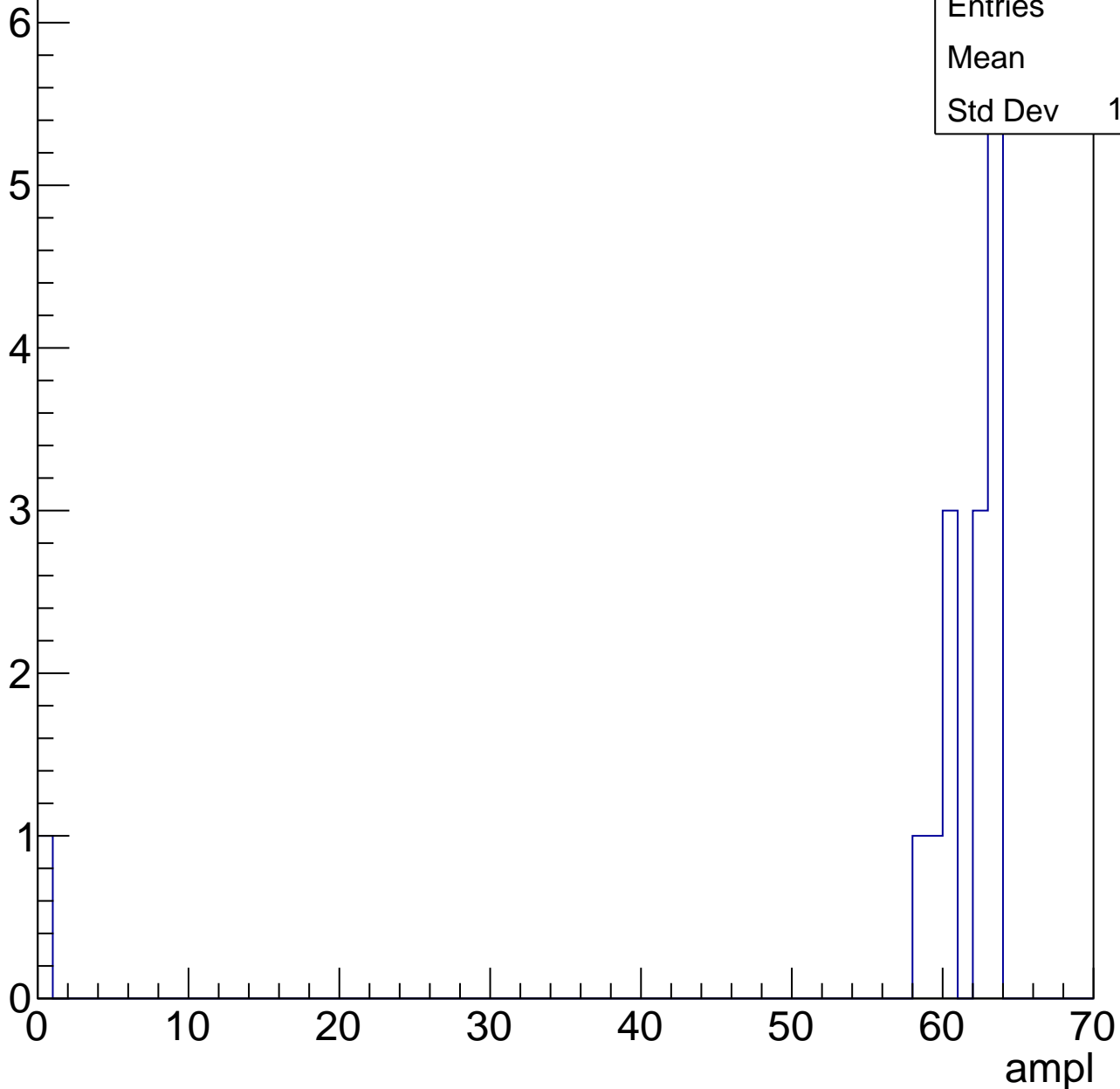


B1L103S, U5-ch67, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	15
Mean	57.4
Std Dev	15.43

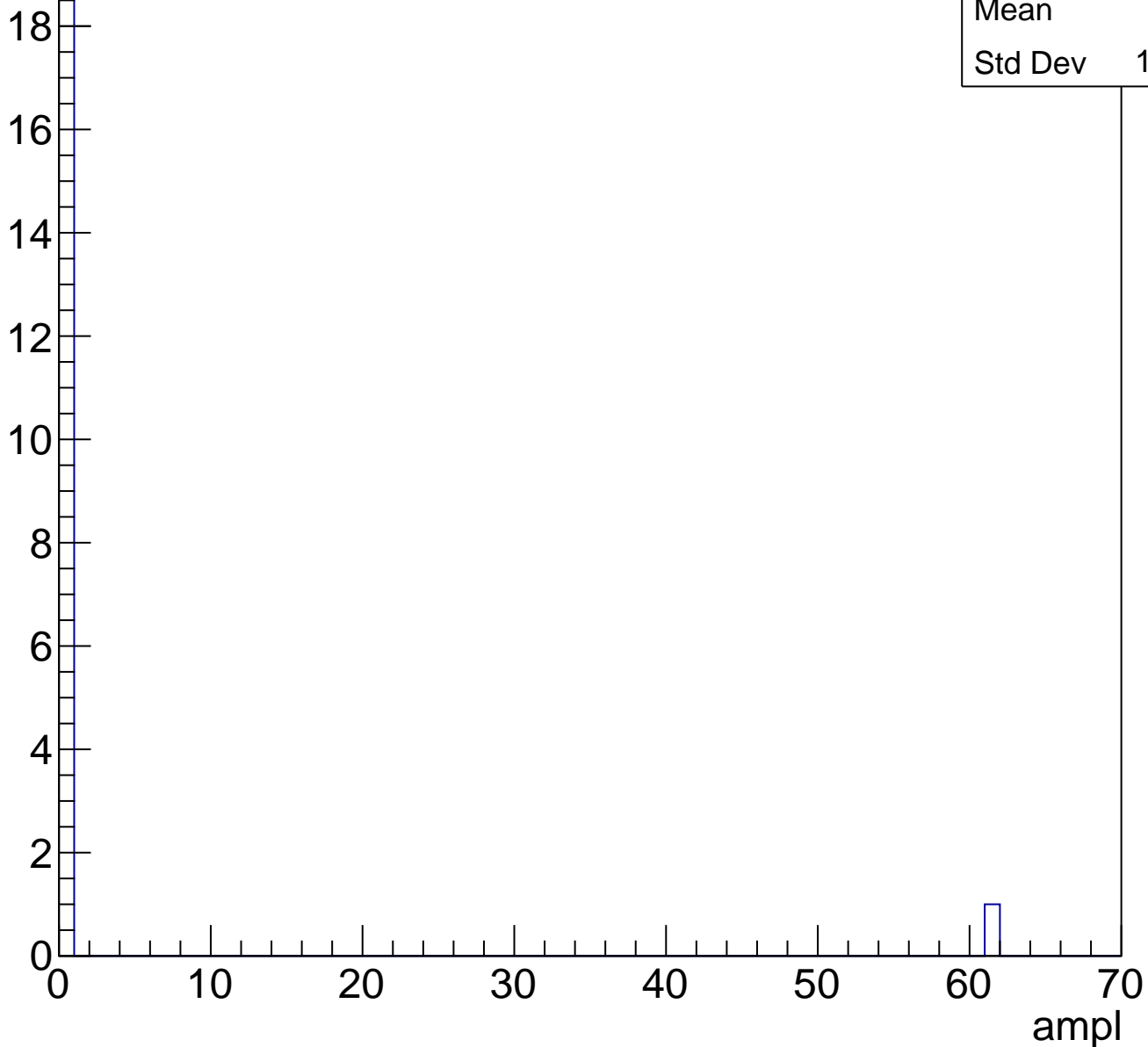


B1L103S, U5-ch67, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.05
Std Dev	13.29

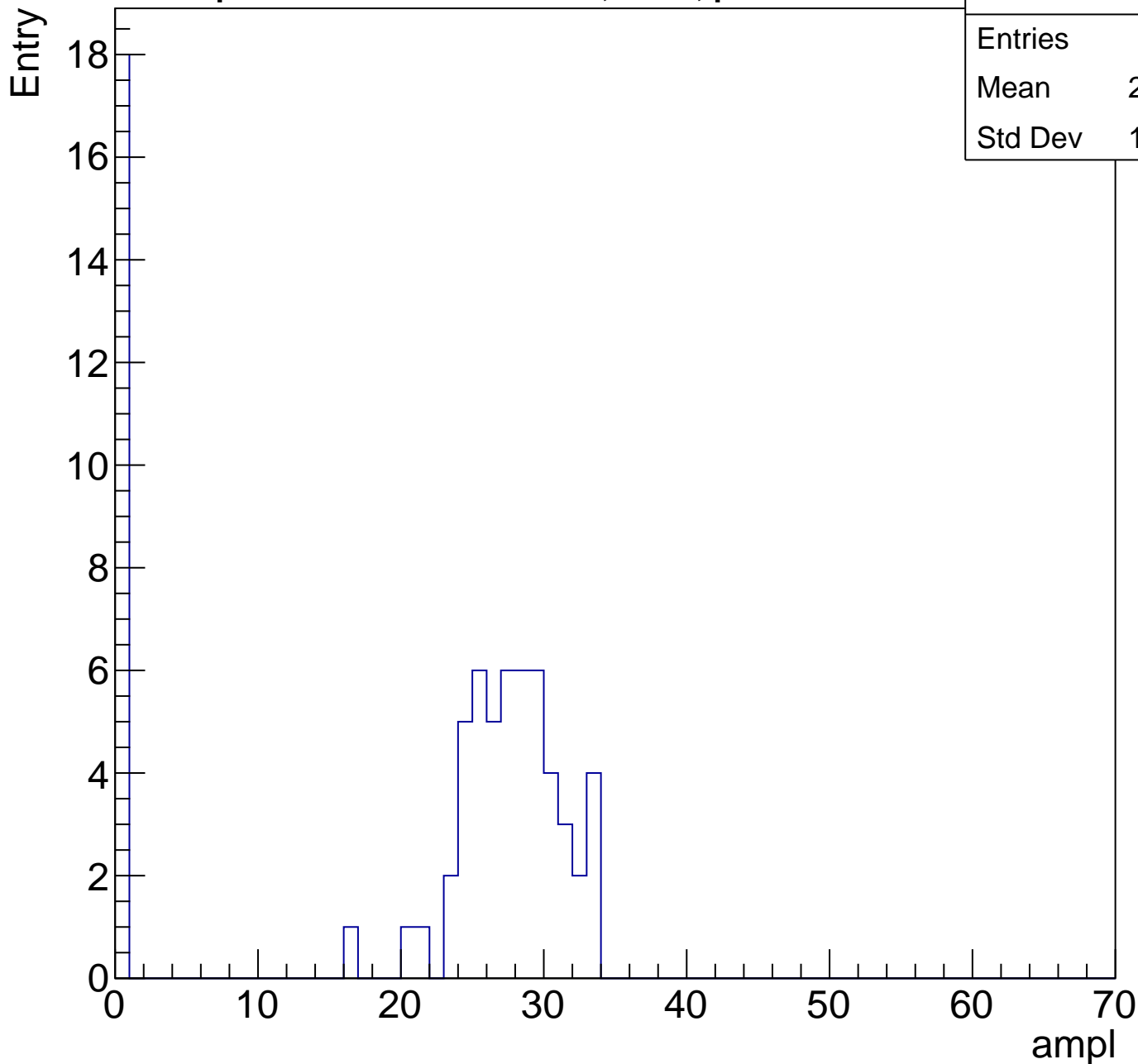
Entry



B1L103S, U5-ch68, adc0

calib_packv5_041523_1651.root, FC#0, port C2

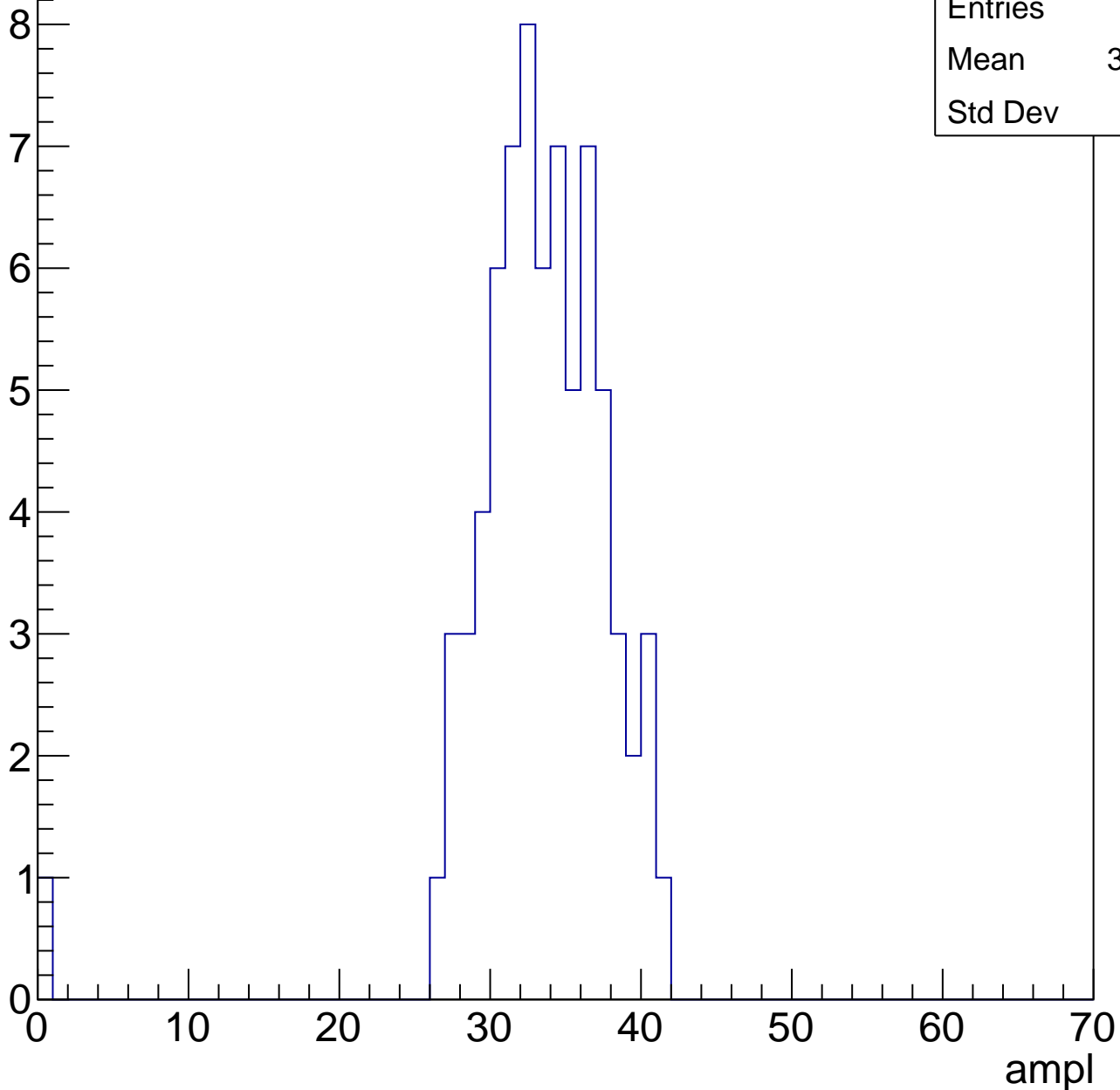
Entries	70
Mean	20.23
Std Dev	12.27



B1L103S, U5-ch68, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry



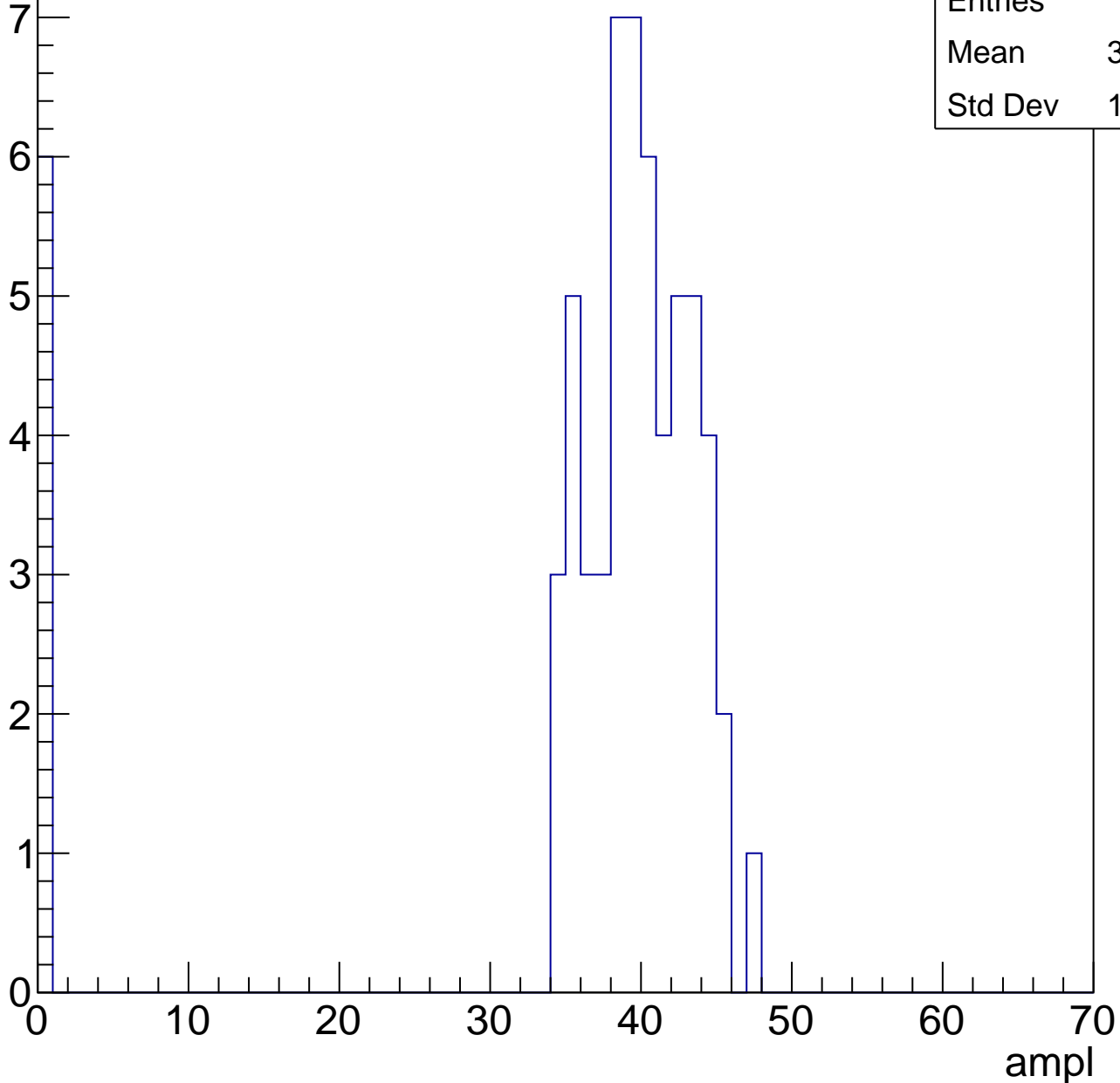
Entries	72
Mean	32.79
Std Dev	5.27

B1L103S, U5-ch68, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	35.69
Std Dev	12.17

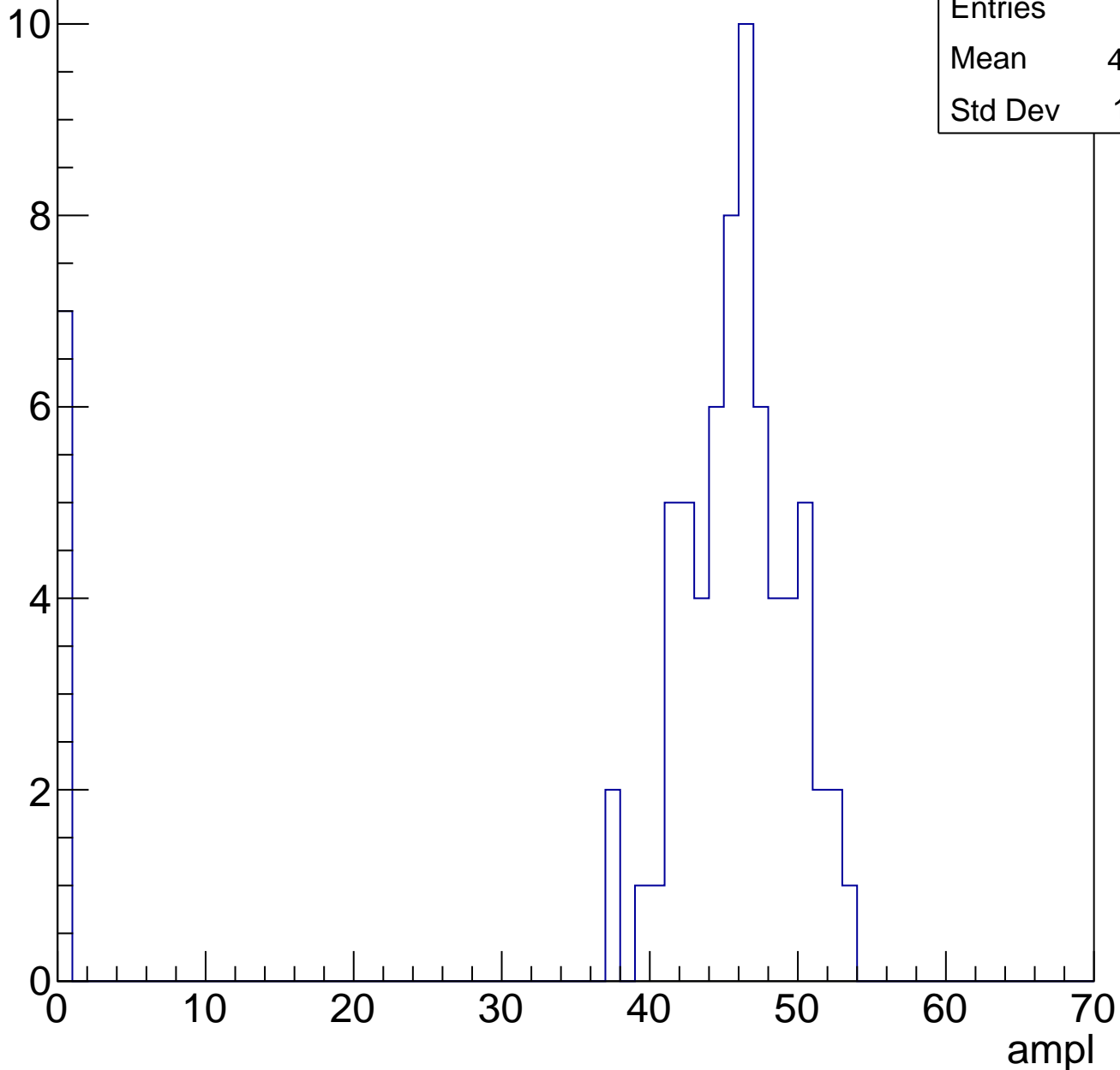


B1L103S, U5-ch68, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	73
Mean	41.14
Std Dev	13.81

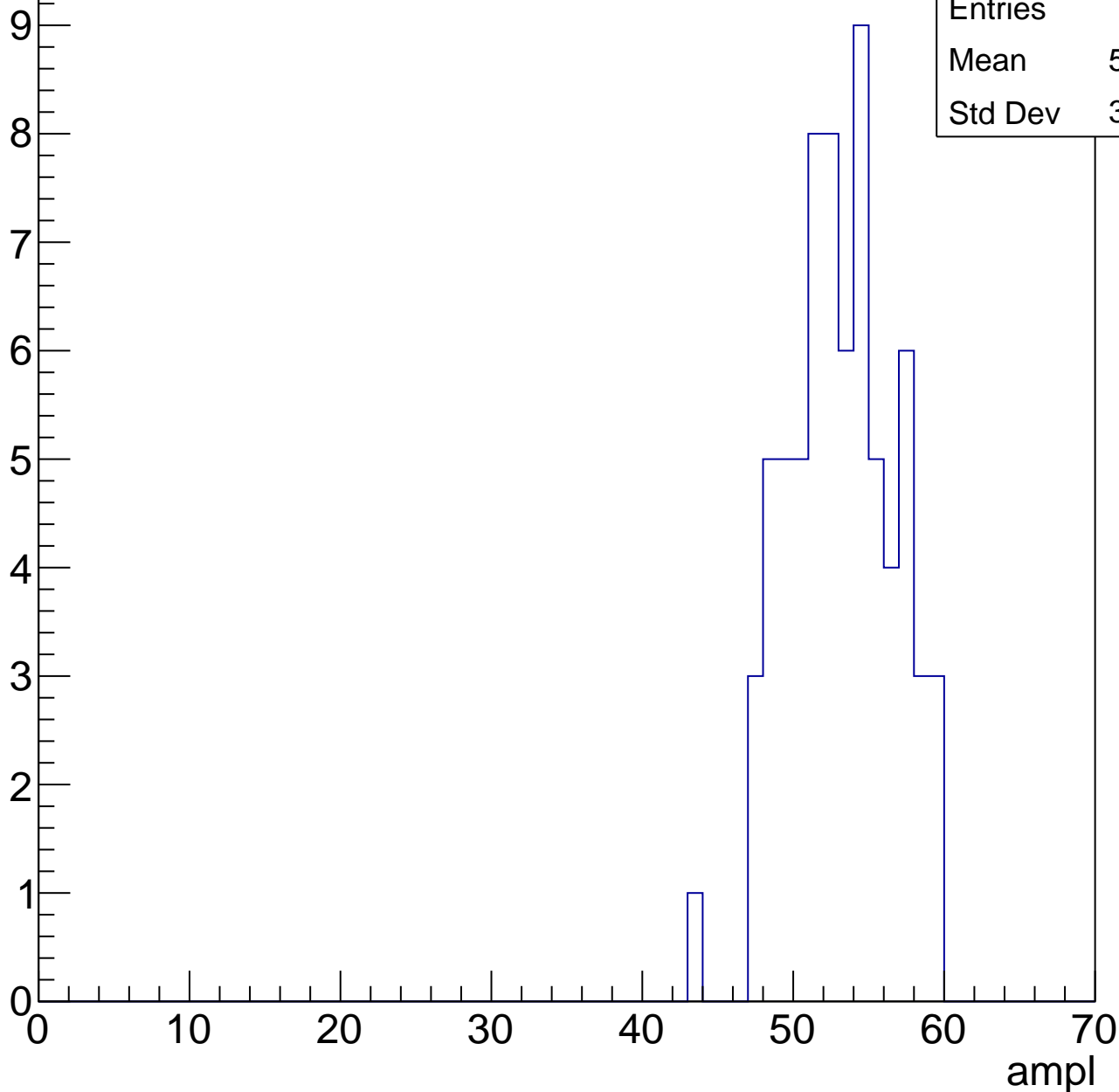
Entry



B1L103S, U5-ch68, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

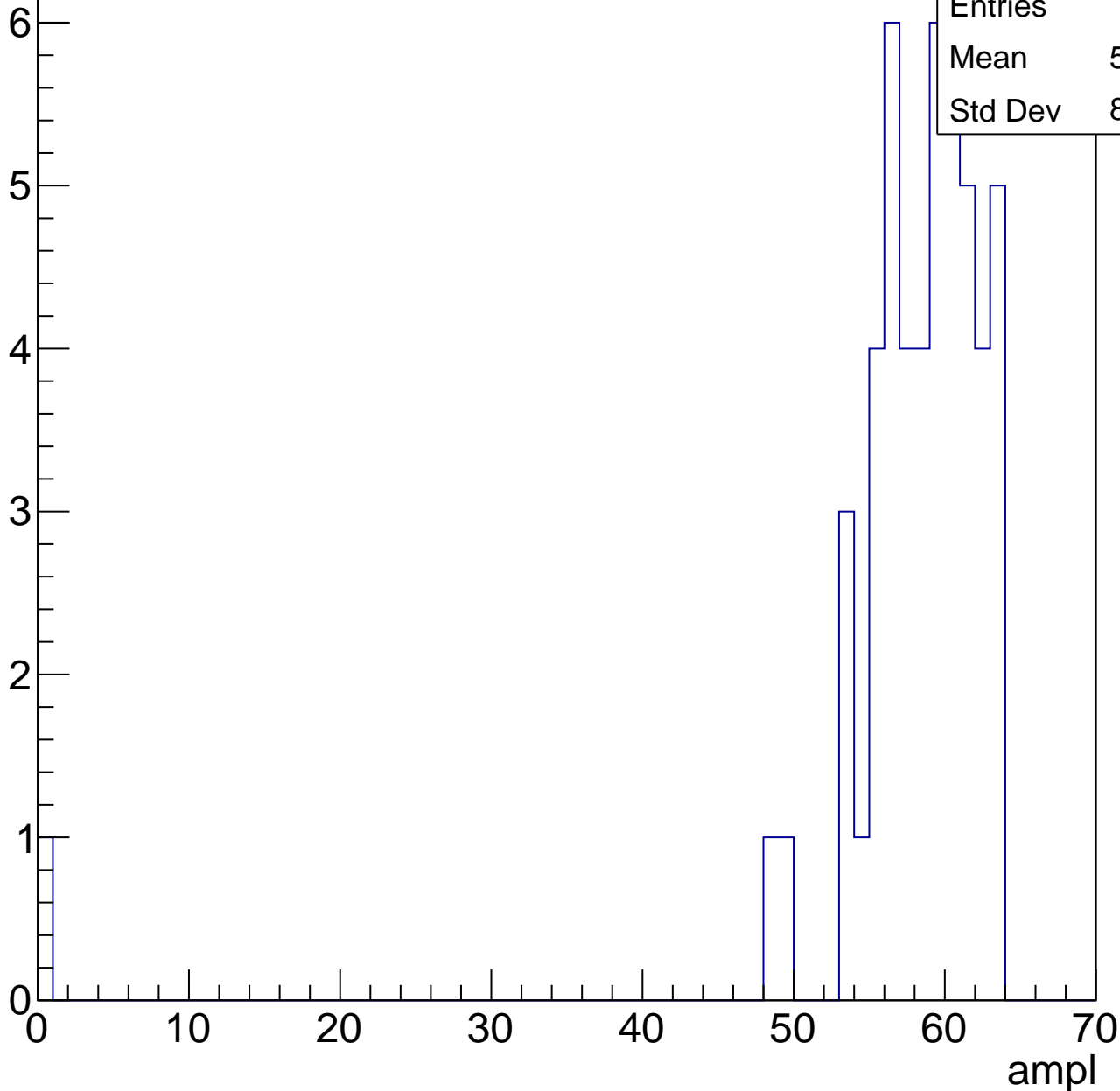


B1L103S, U5-ch68, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	57.02
Std Dev	8.762

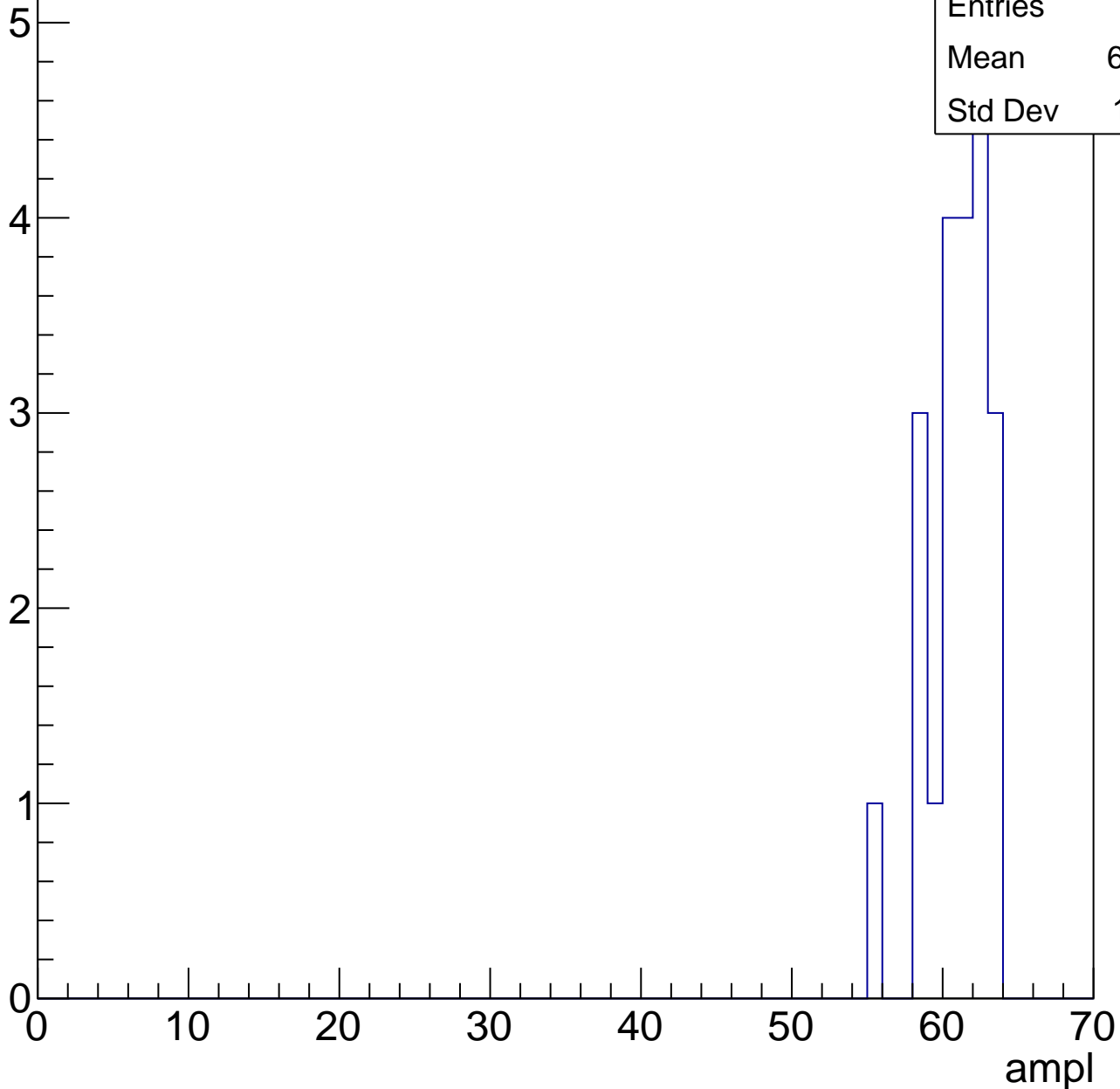


B1L103S, U5-ch68, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	21
Mean	60.52
Std Dev	1.991

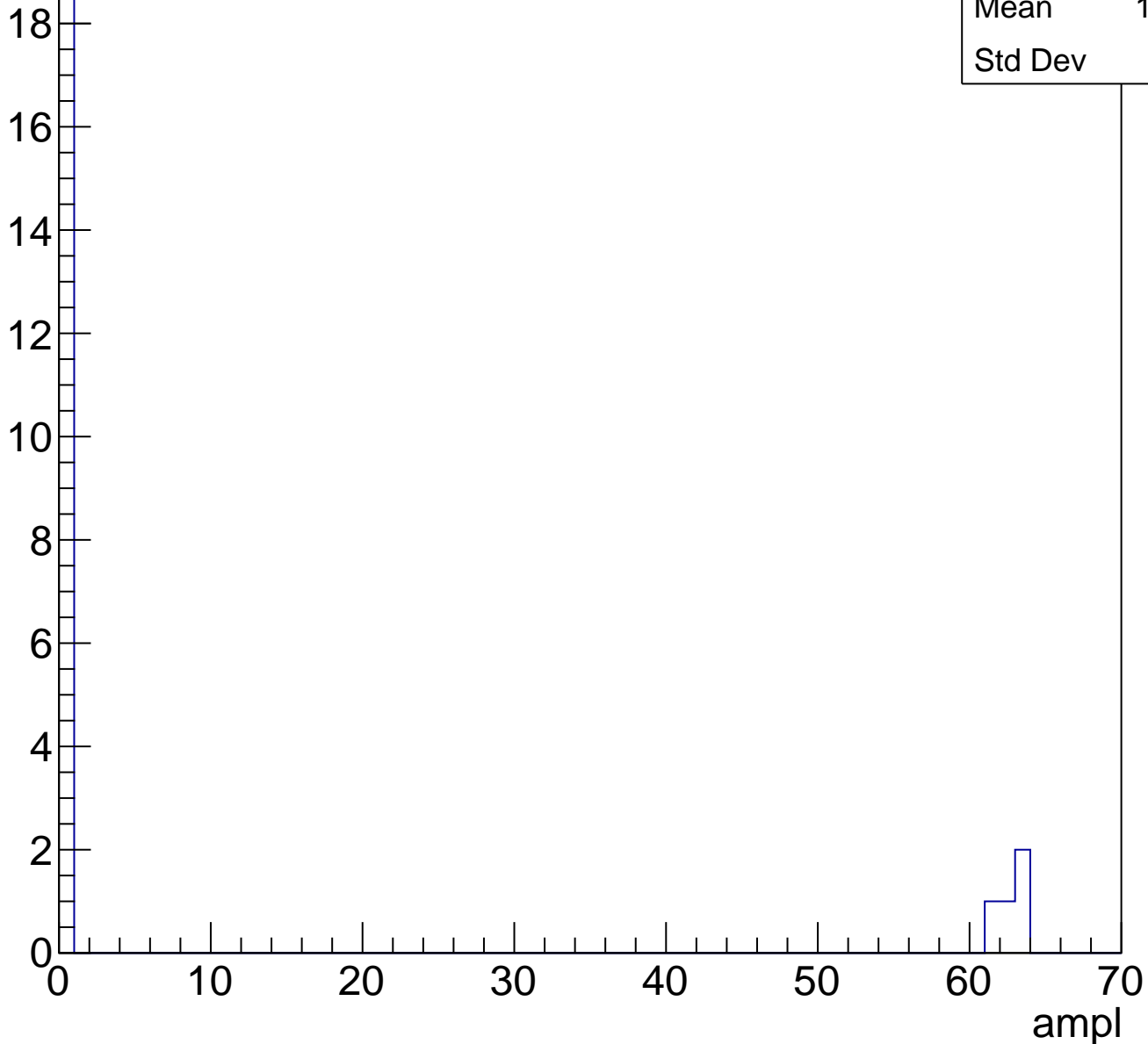


B1L103S, U5-ch68, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	23
Mean	10.83
Std Dev	23.6

Entry



B1L103S, U5-ch69, adc0

calib_packv5_041523_1651.root, FC#0, port C2

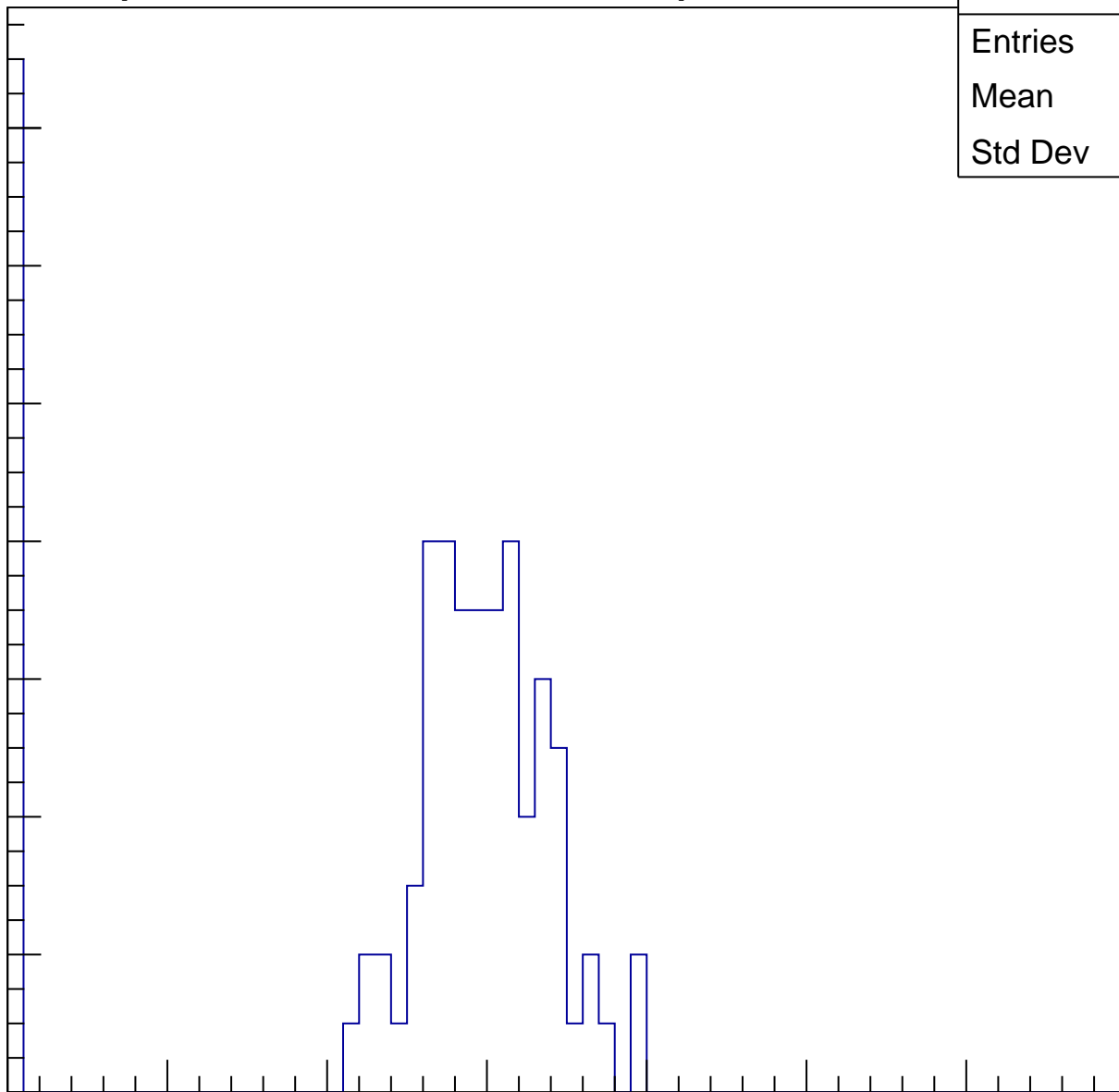
Entries	90
Mean	24.54
Std Dev	11.52

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

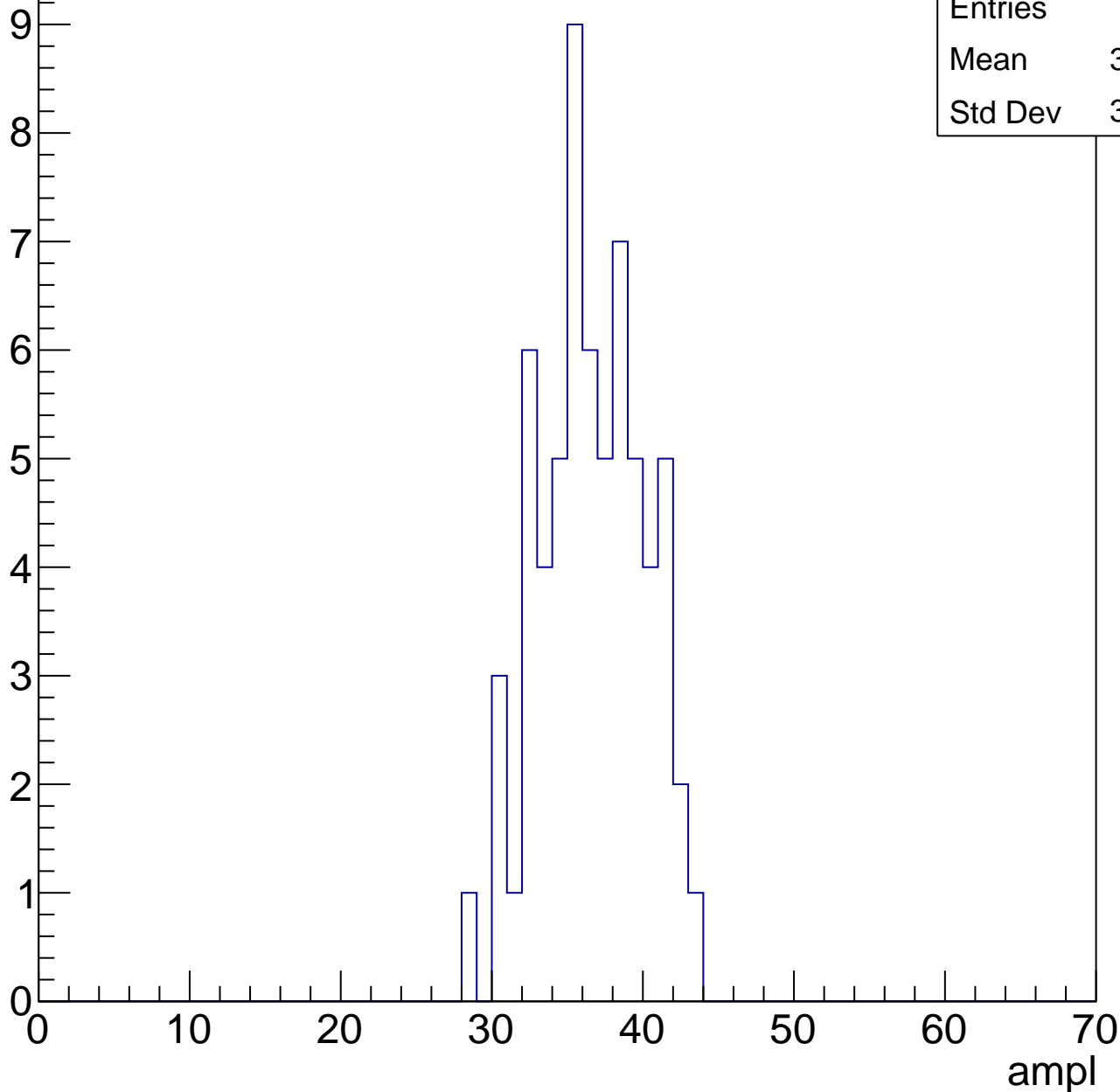


B1L103S, U5-ch69, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	36.12
Std Dev	3.412

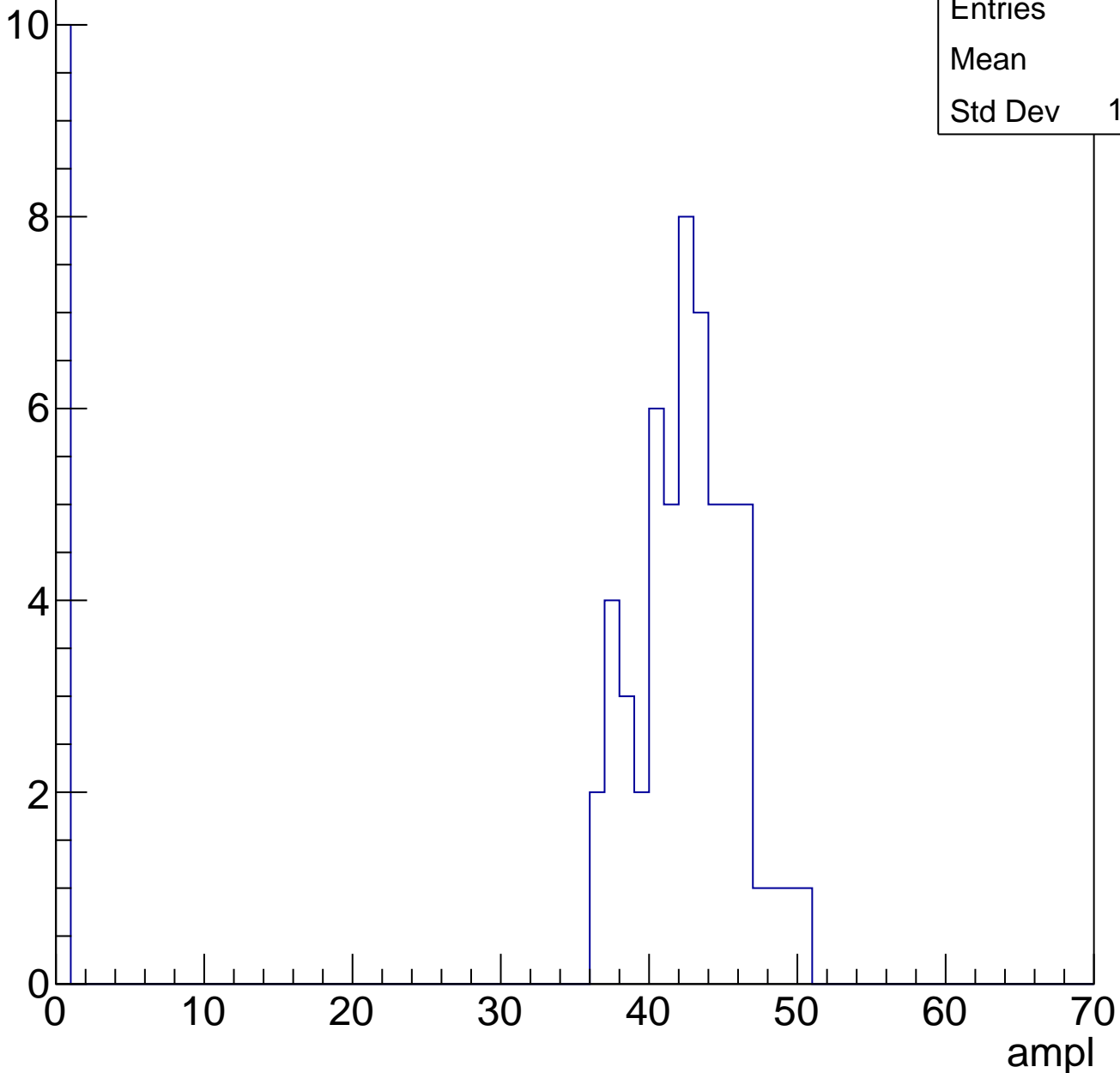


B1L103S, U5-ch69, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	66
Mean	35.8
Std Dev	15.42

Entry

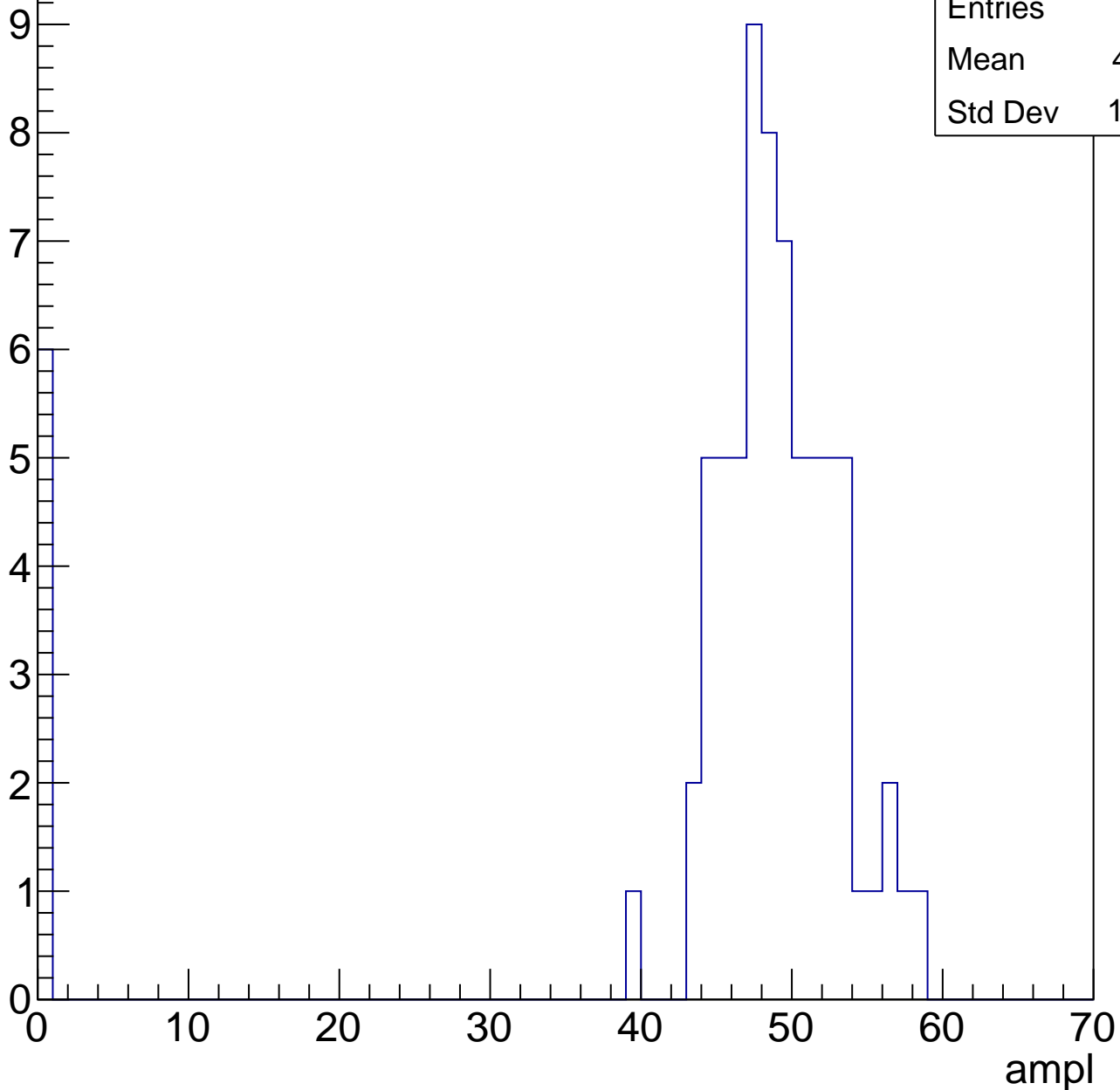


B1L103S, U5-ch69, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	44.81
Std Dev	13.77

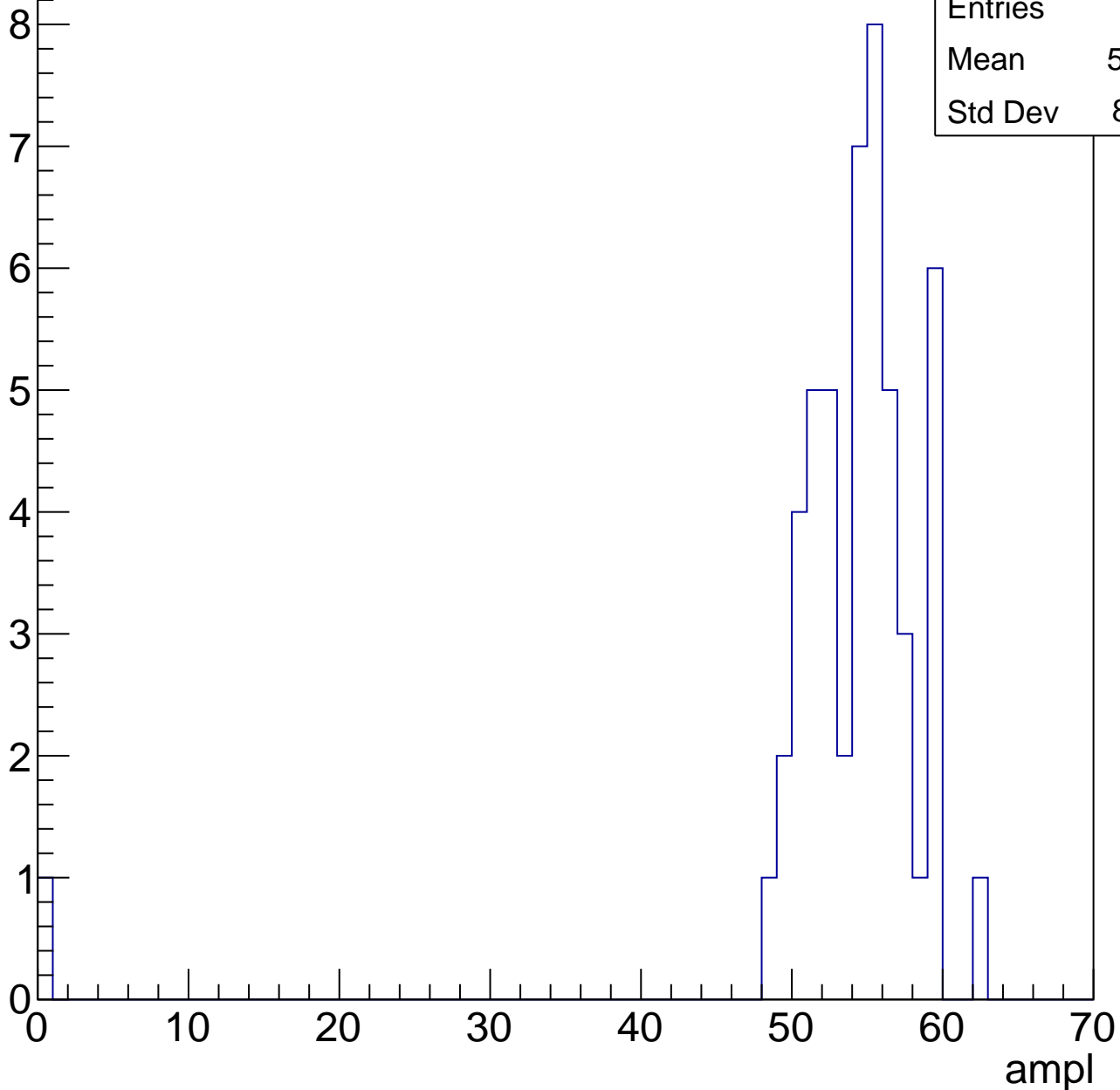


B1L103S, U5-ch69, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	53.14
Std Dev	8.141

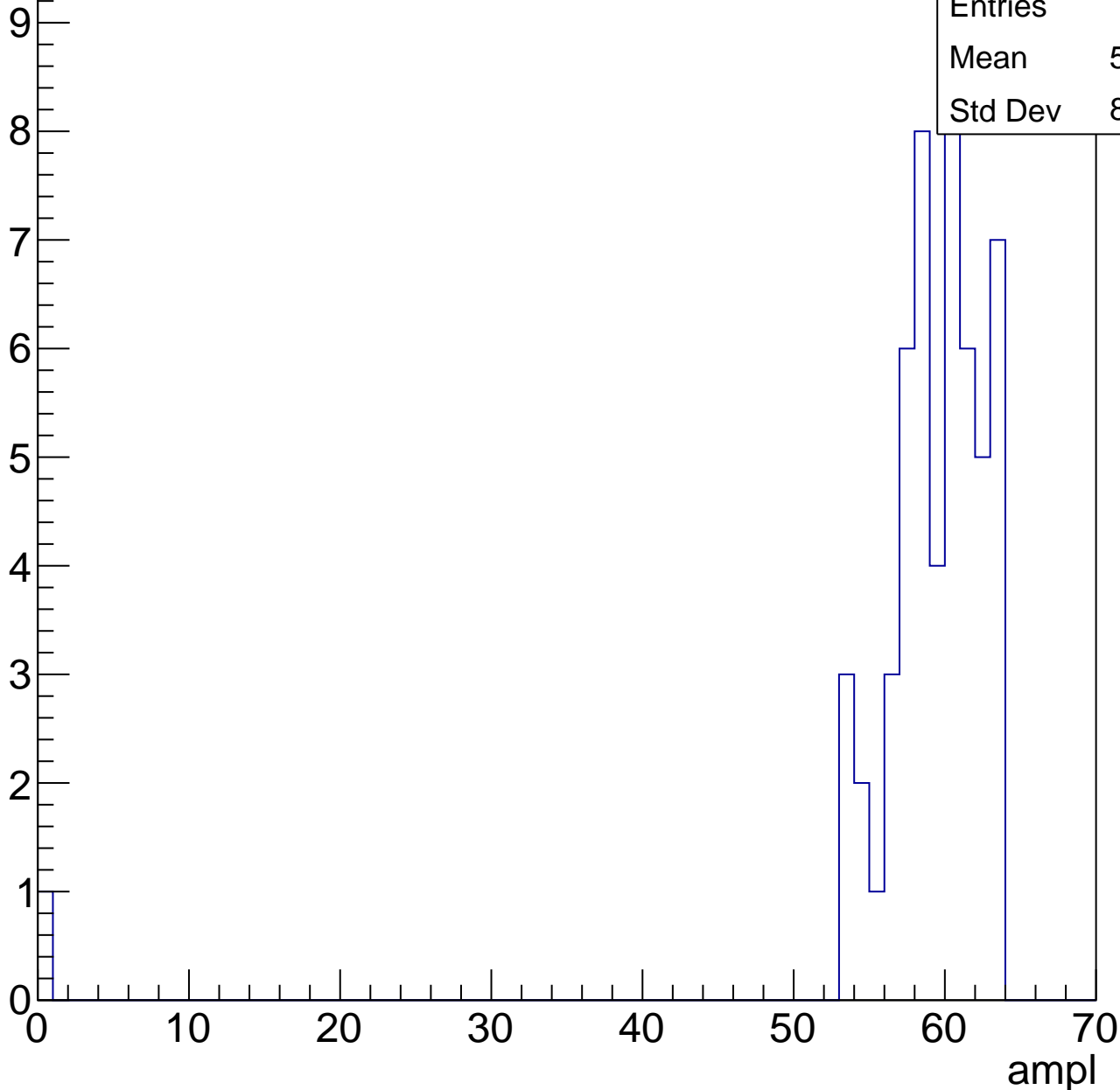


B1L103S, U5-ch69, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

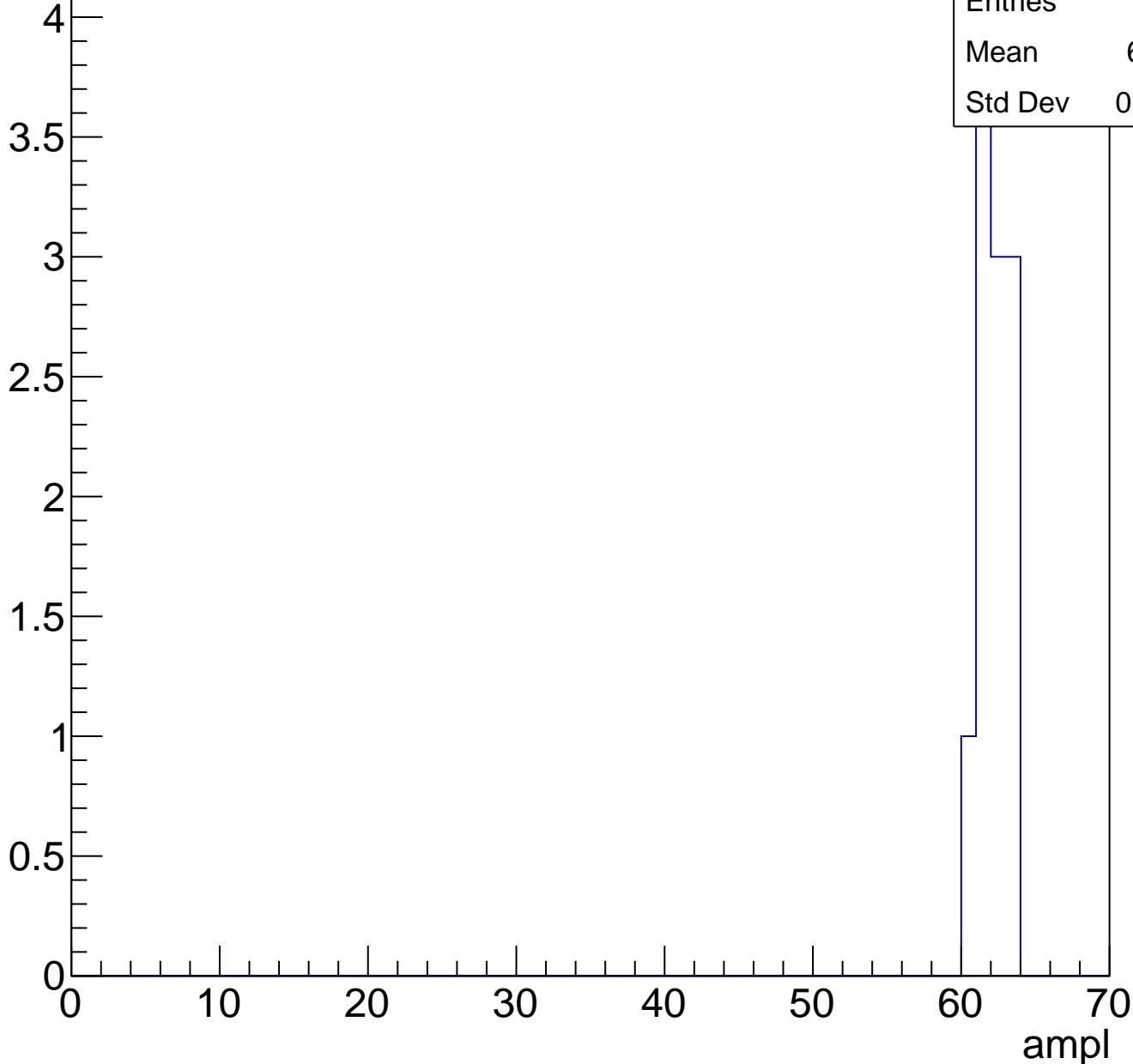
Entries	55
Mean	57.98
Std Dev	8.363



B1L103S, U5-ch69, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch69, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51

Entry



B1L103S, U5-ch70, adc0

calib_packv5_041523_1651.root, FC#0, port C2

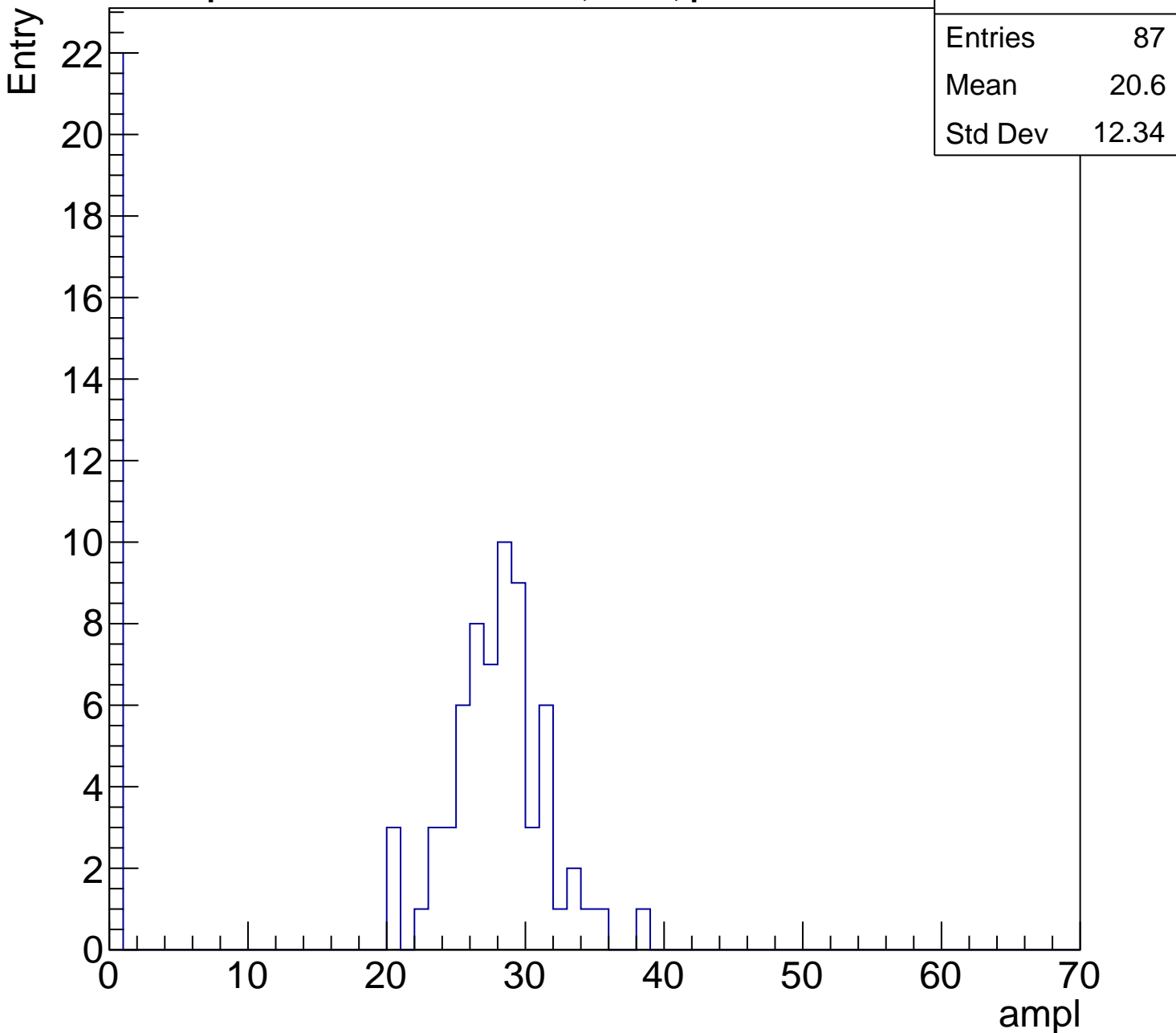
Entry

22
20
18
16
14
12
10
8
6
4
2
0

Entries	87
Mean	20.6
Std Dev	12.34

0 10 20 30 40 50 60 70

ampl

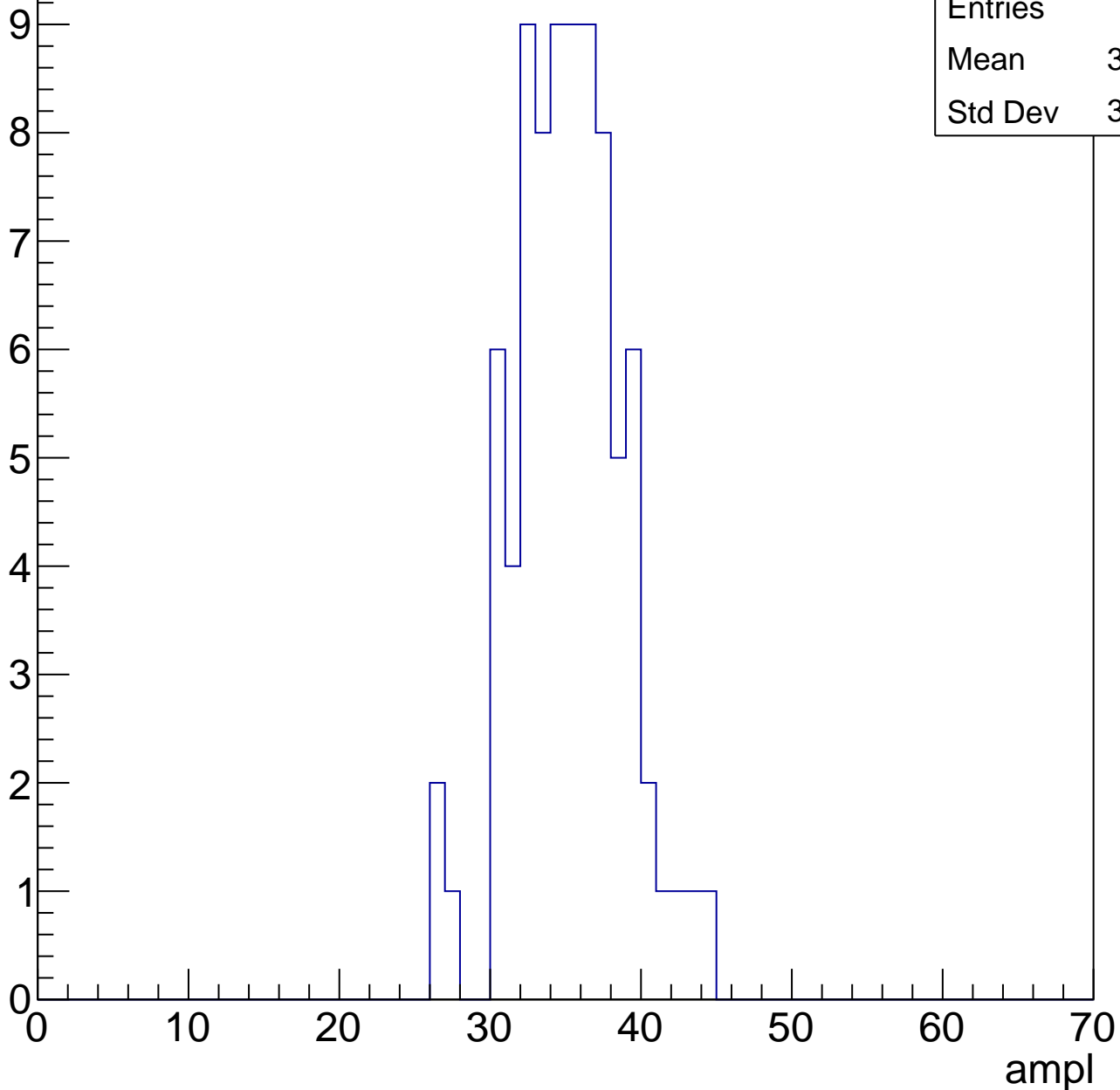


B1L103S, U5-ch70, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	82
Mean	34.76
Std Dev	3.525

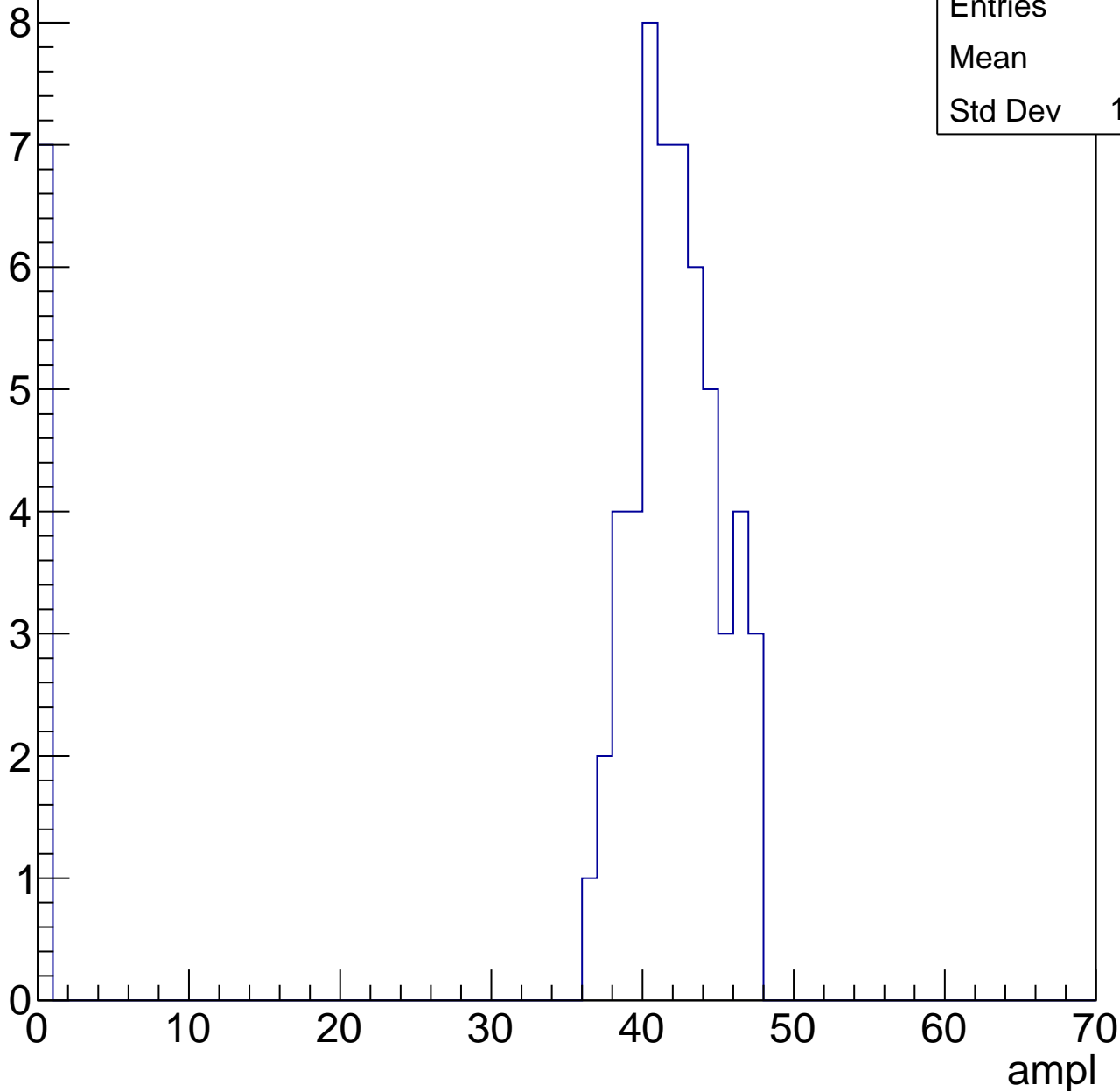


B1L103S, U5-ch70, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	37
Std Dev	13.57

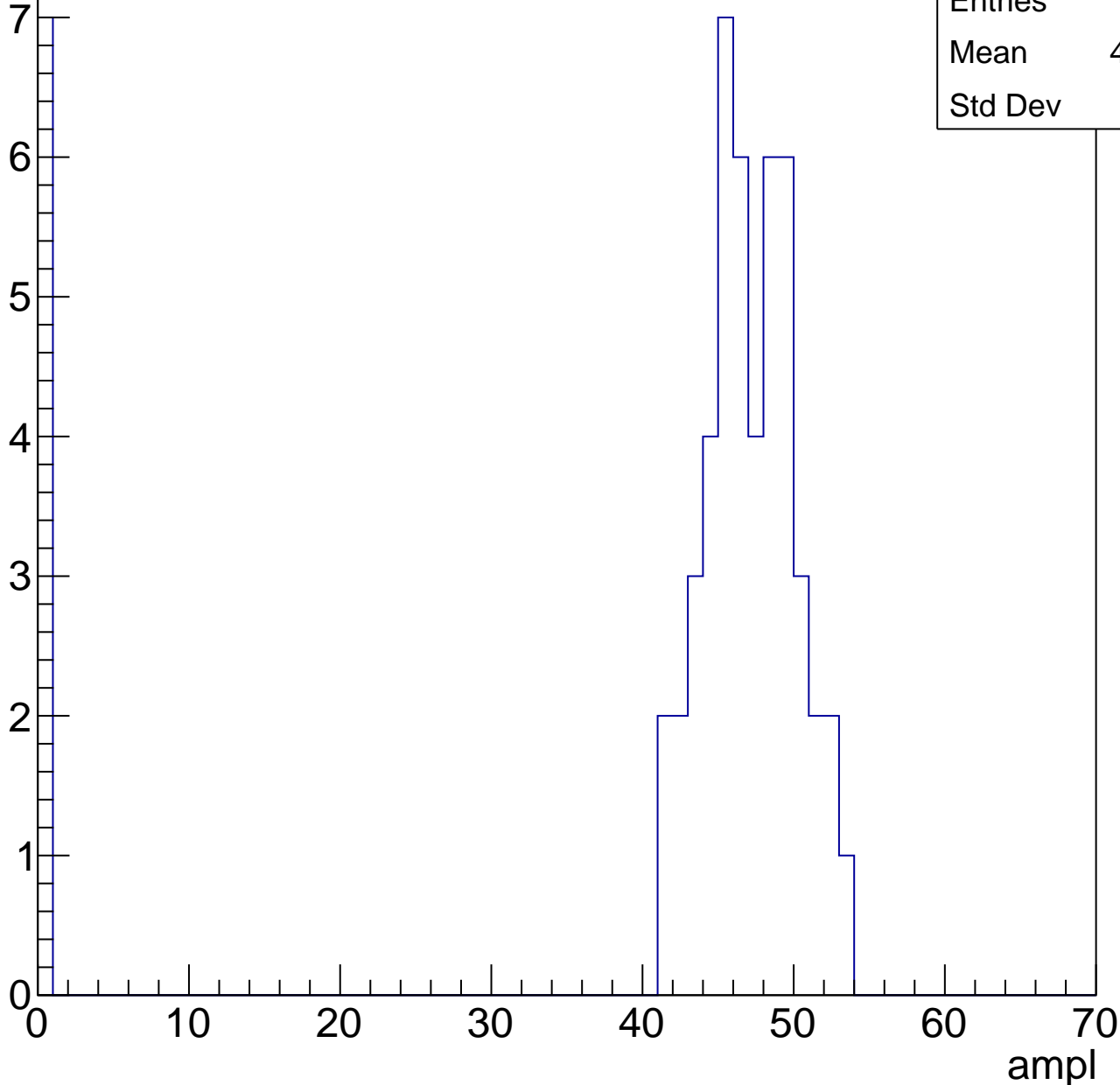


B1L103S, U5-ch70, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	40.75
Std Dev	15.8

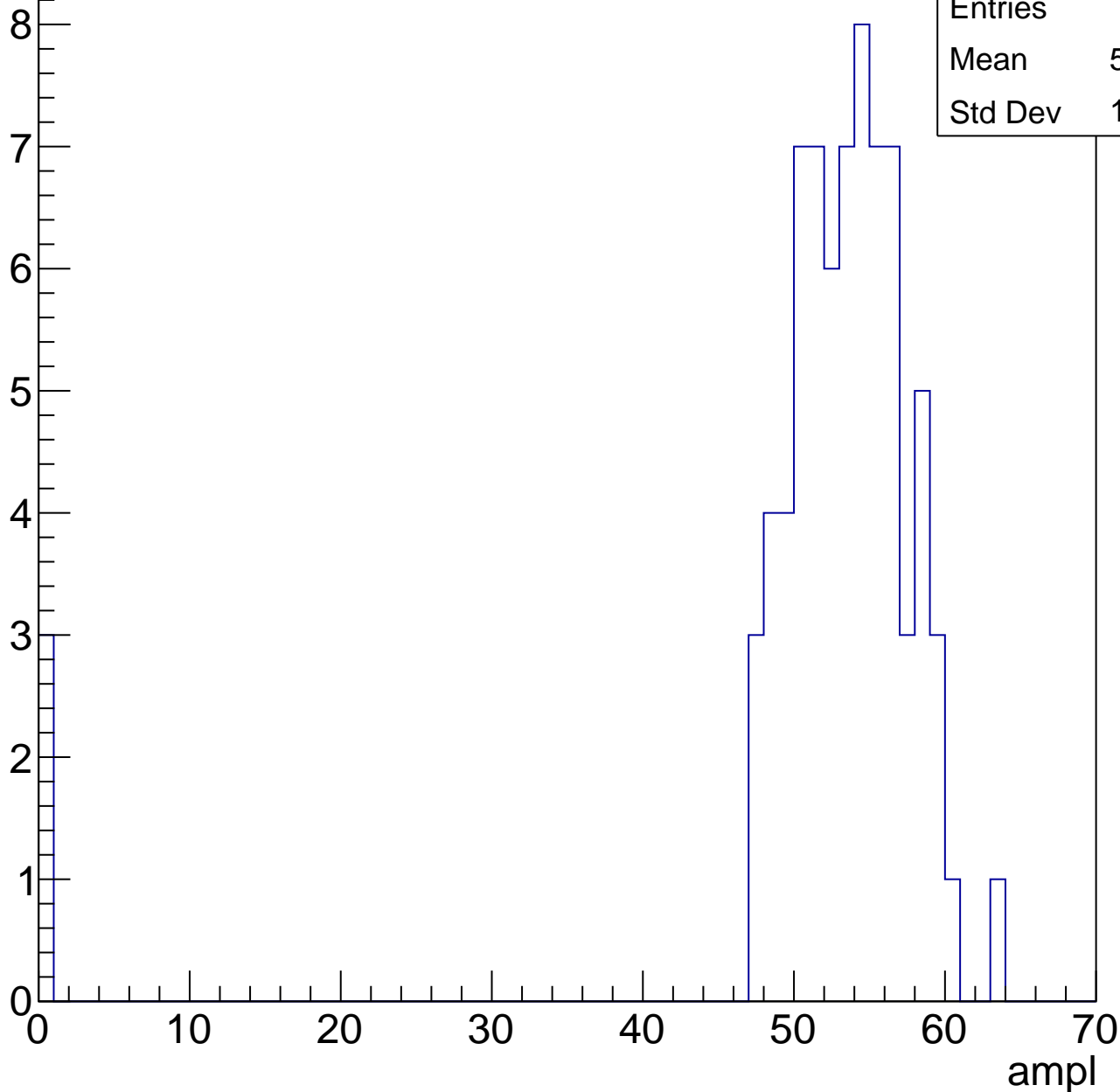


B1L103S, U5-ch70, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	51.17
Std Dev	10.92

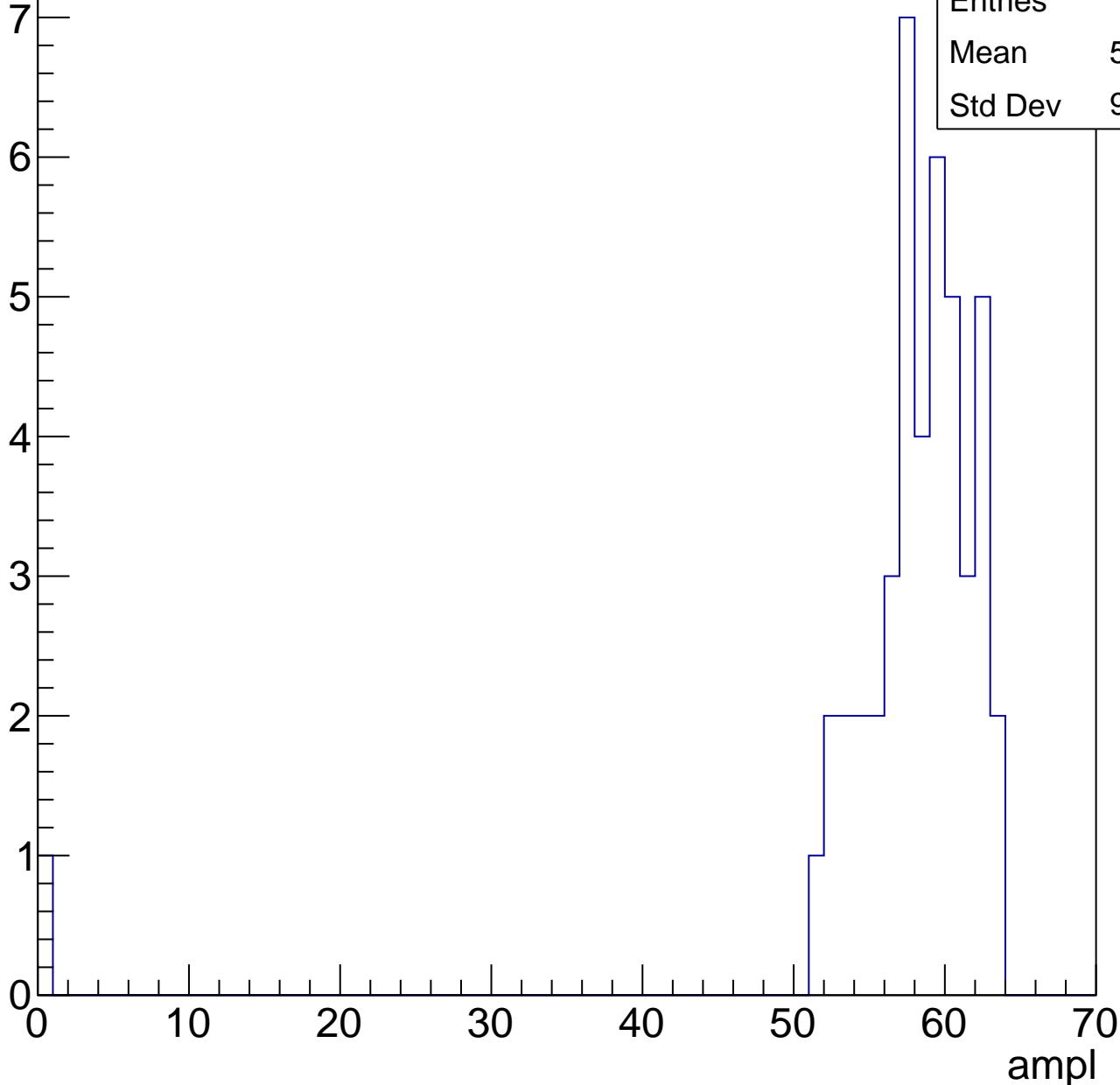


B1L103S, U5-ch70, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	45
Mean	56.69
Std Dev	9.079

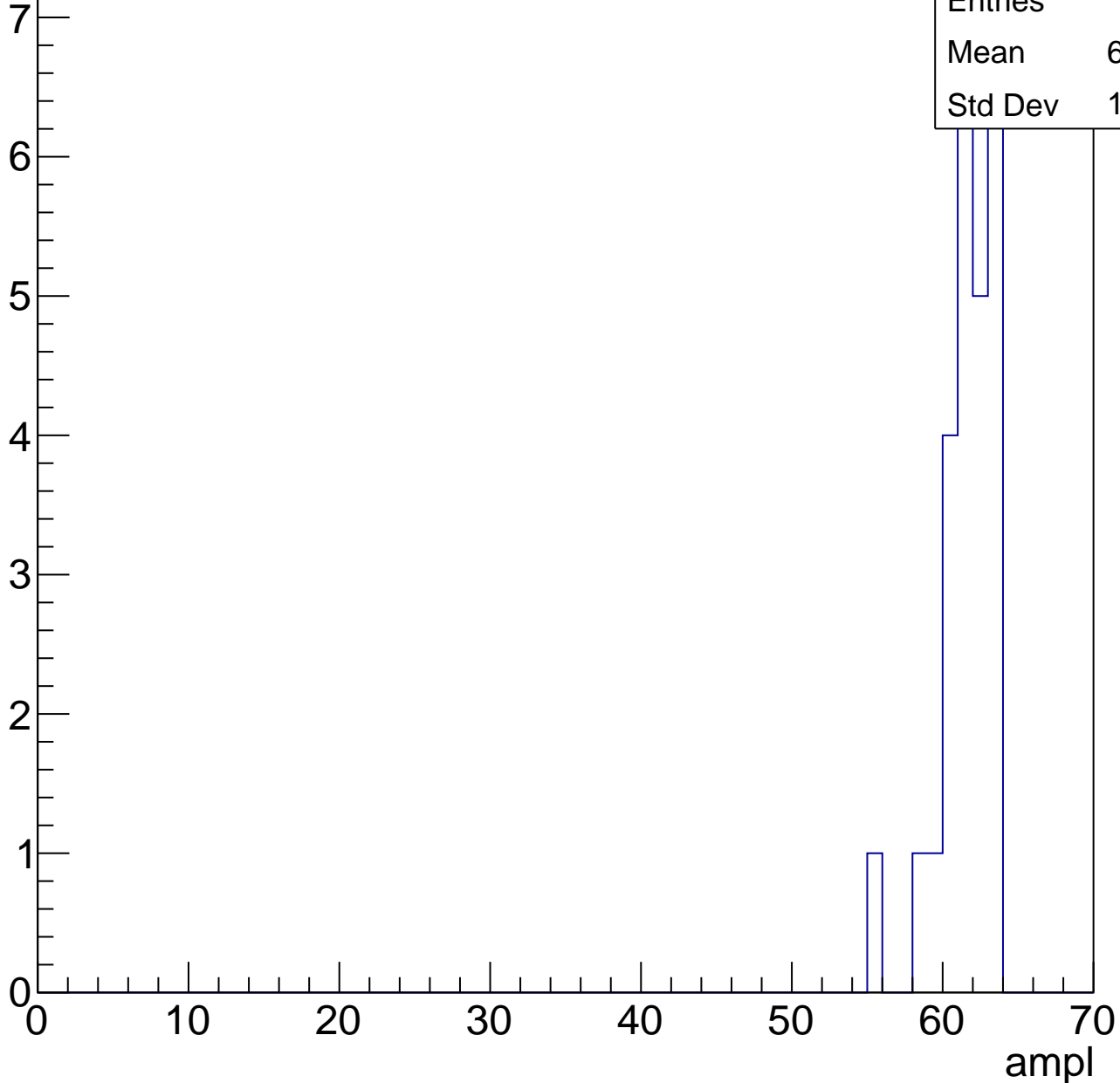


B1L103S, U5-ch70, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	26
Mean	61.15
Std Dev	1.812



B1L103S, U5-ch70, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

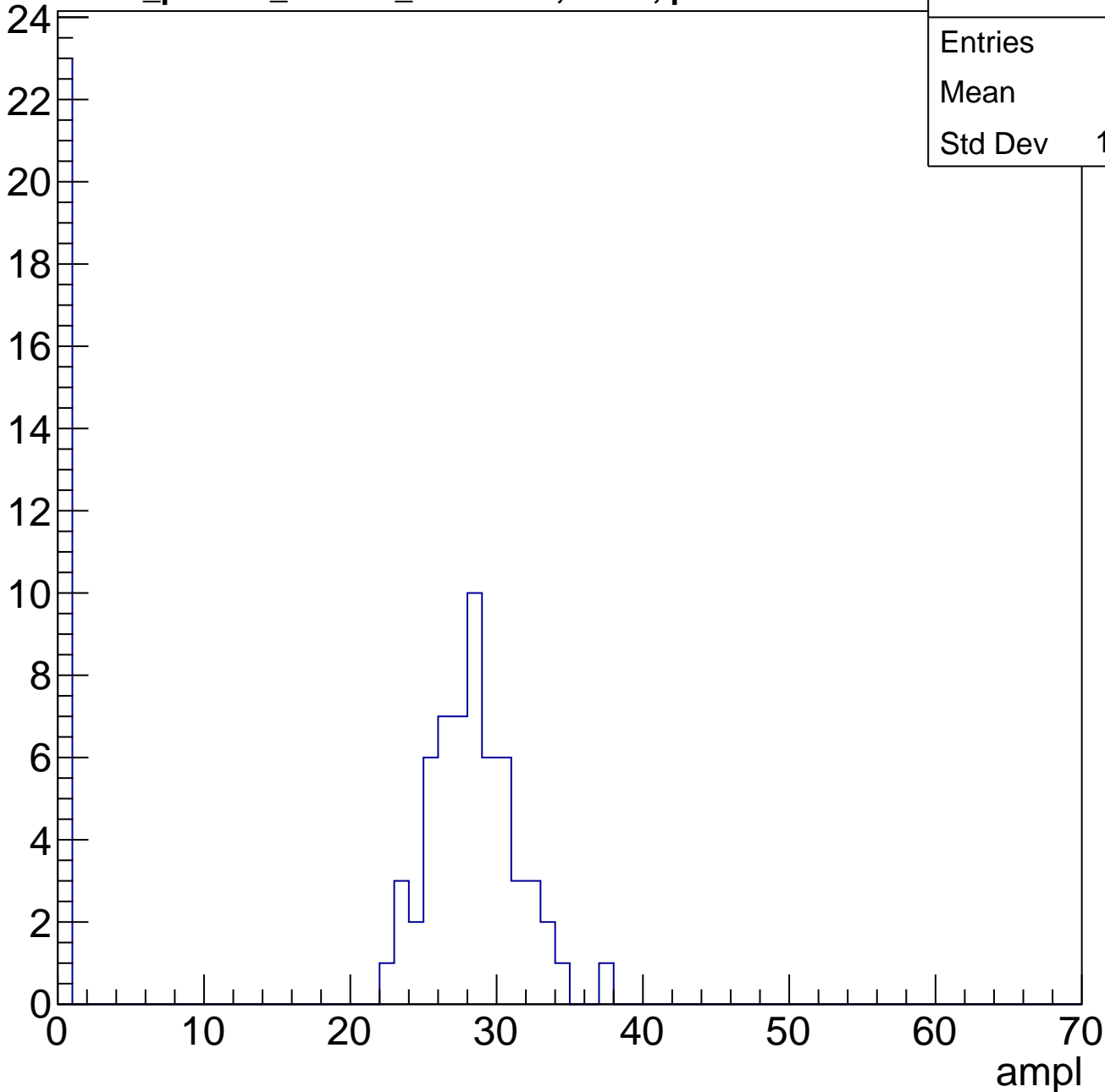


B1L103S, U5-ch71, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	20
Std Dev	12.84

Entry



B1L103S, U5-ch71, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	97
Mean	30.3
Std Dev	12.44

Entry

12

10

8

6

4

2

0

0

10

20

30

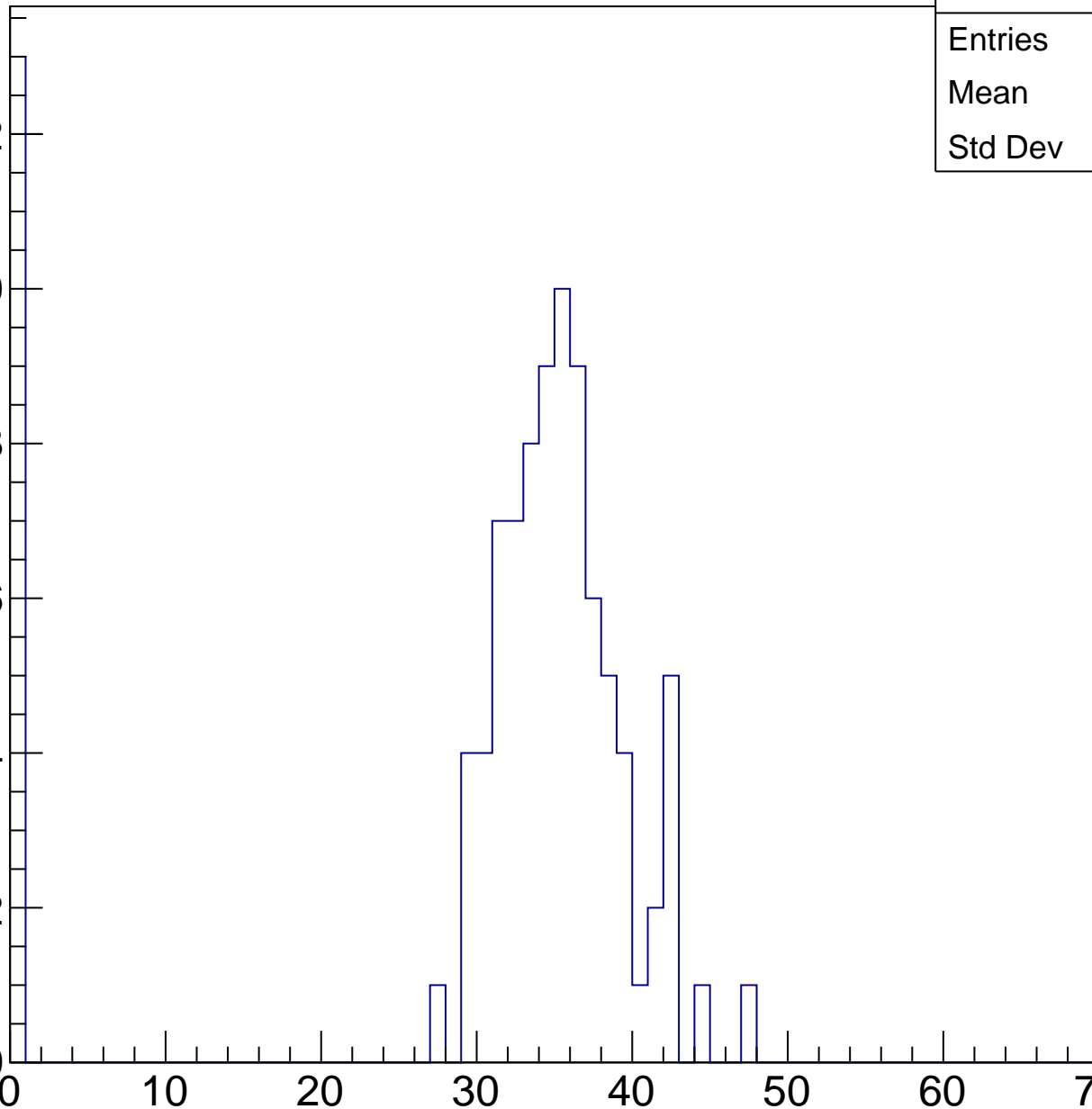
40

50

60

70

ampl

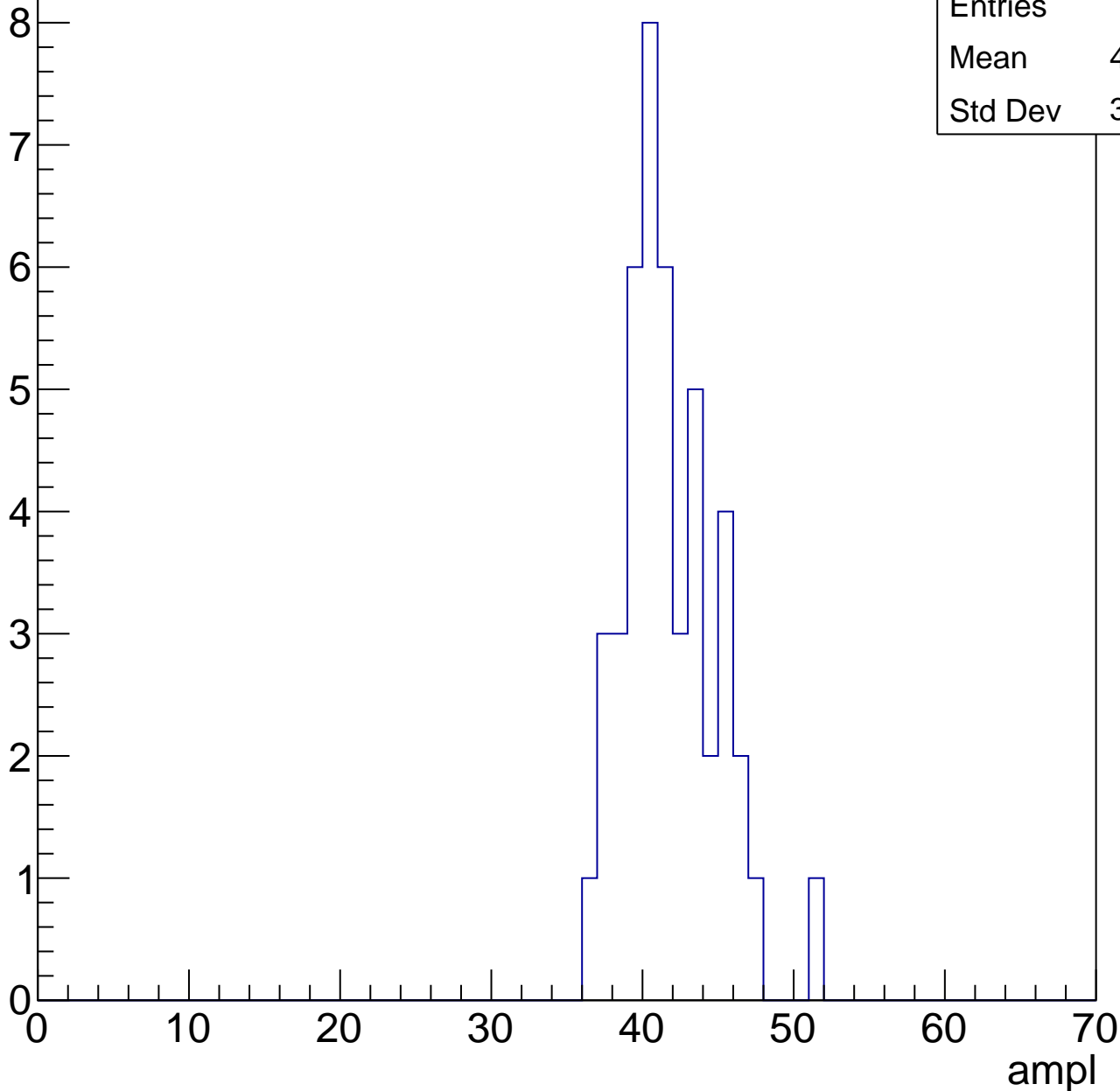


B1L103S, U5-ch71, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	45
Mean	41.33
Std Dev	3.048

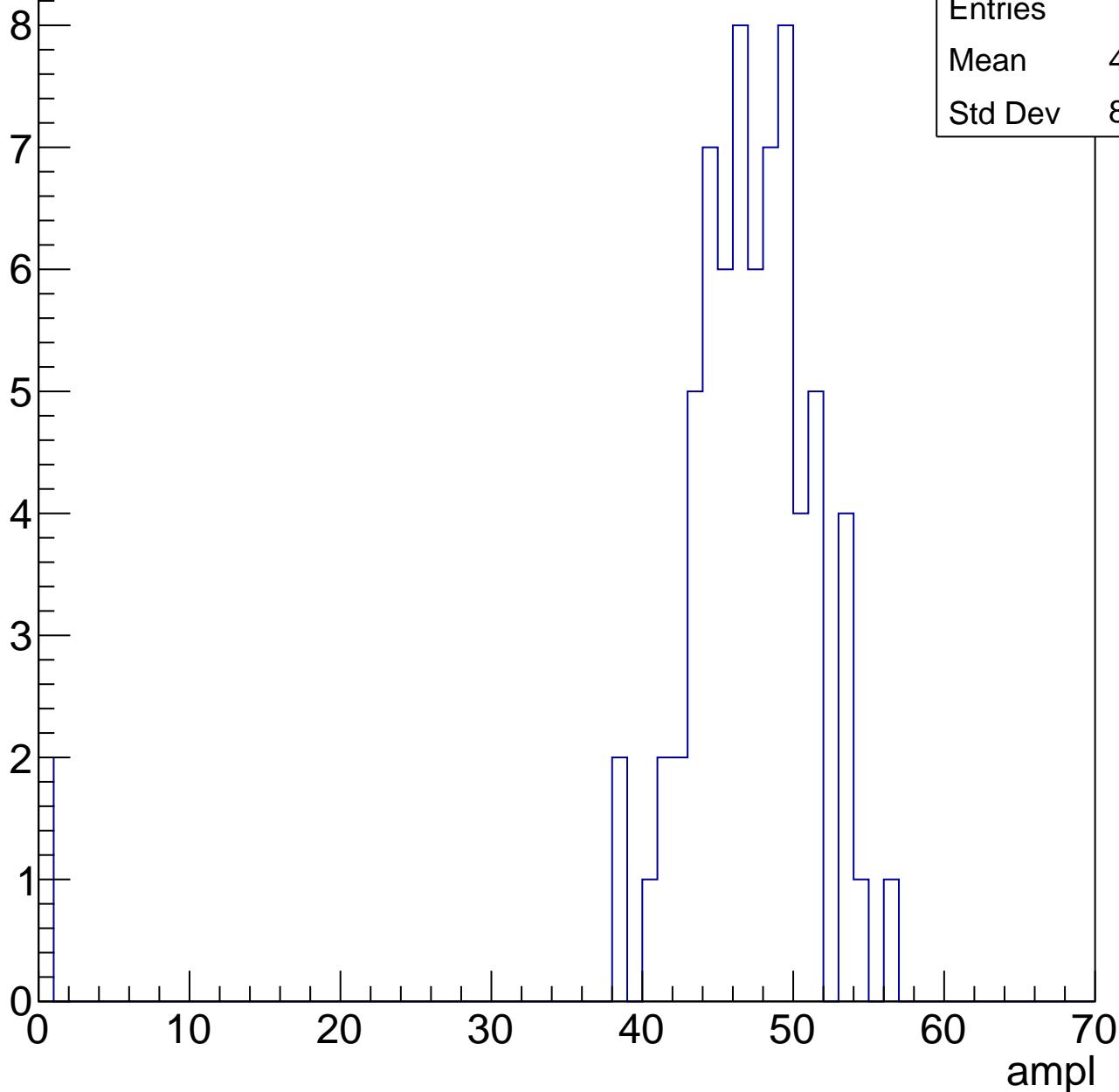


B1L103S, U5-ch71, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	45.49
Std Dev	8.553

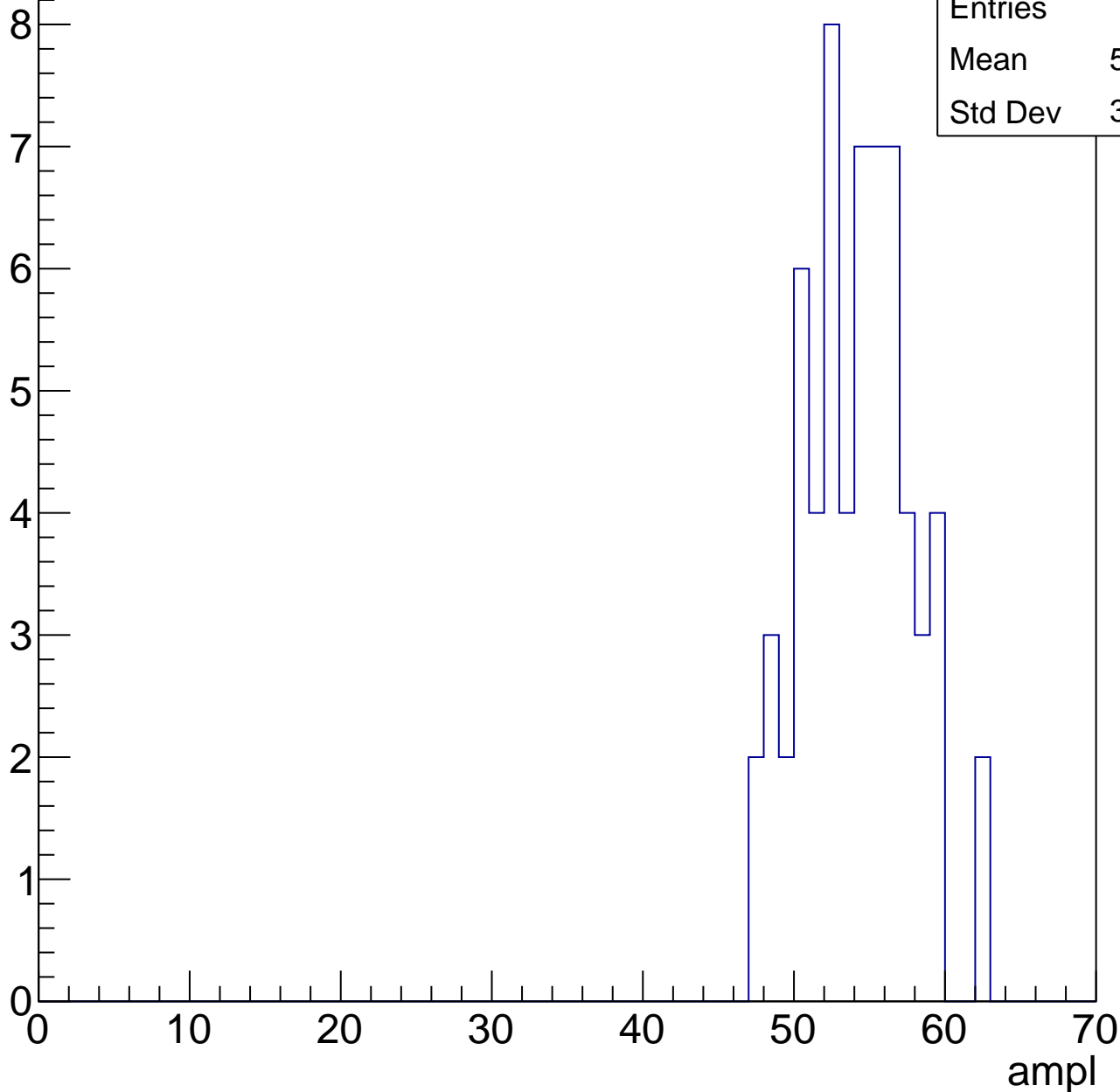


B1L103S, U5-ch71, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

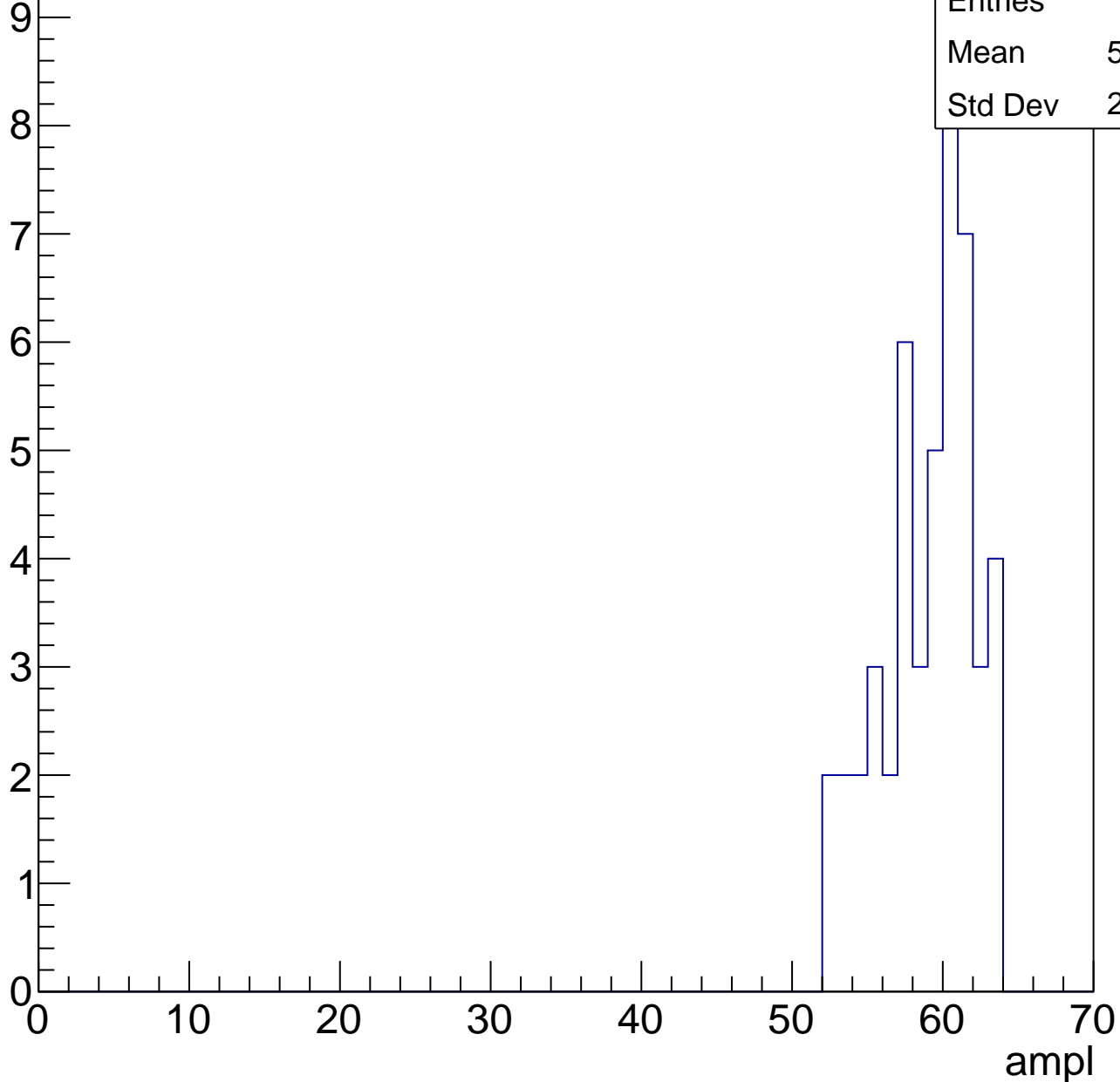
Entries	63
Mean	53.73
Std Dev	3.488



B1L103S, U5-ch71, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



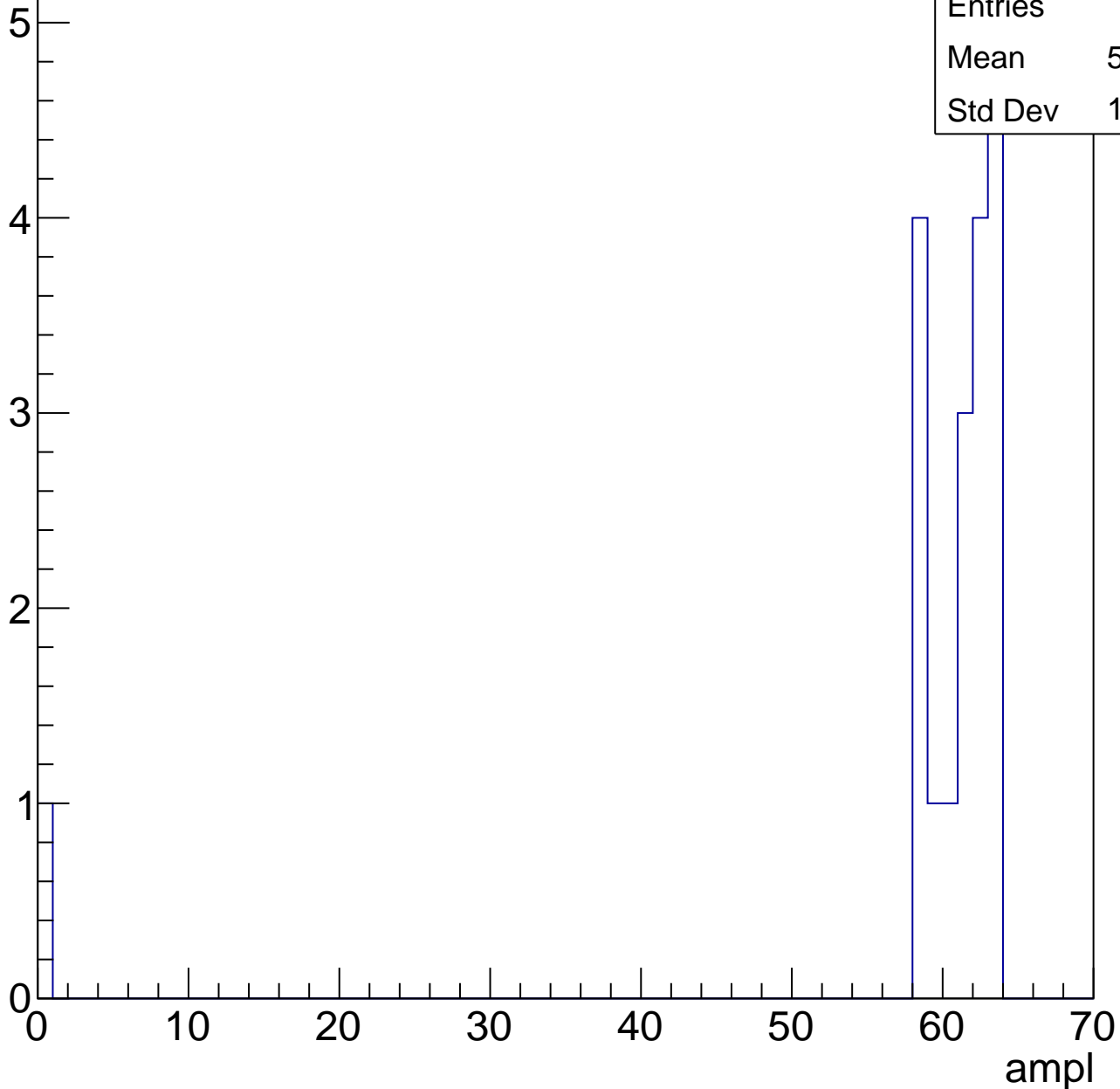
Entries	48
Mean	58.56
Std Dev	2.999

B1L103S, U5-ch71, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	19
Mean	57.74
Std Dev	13.73

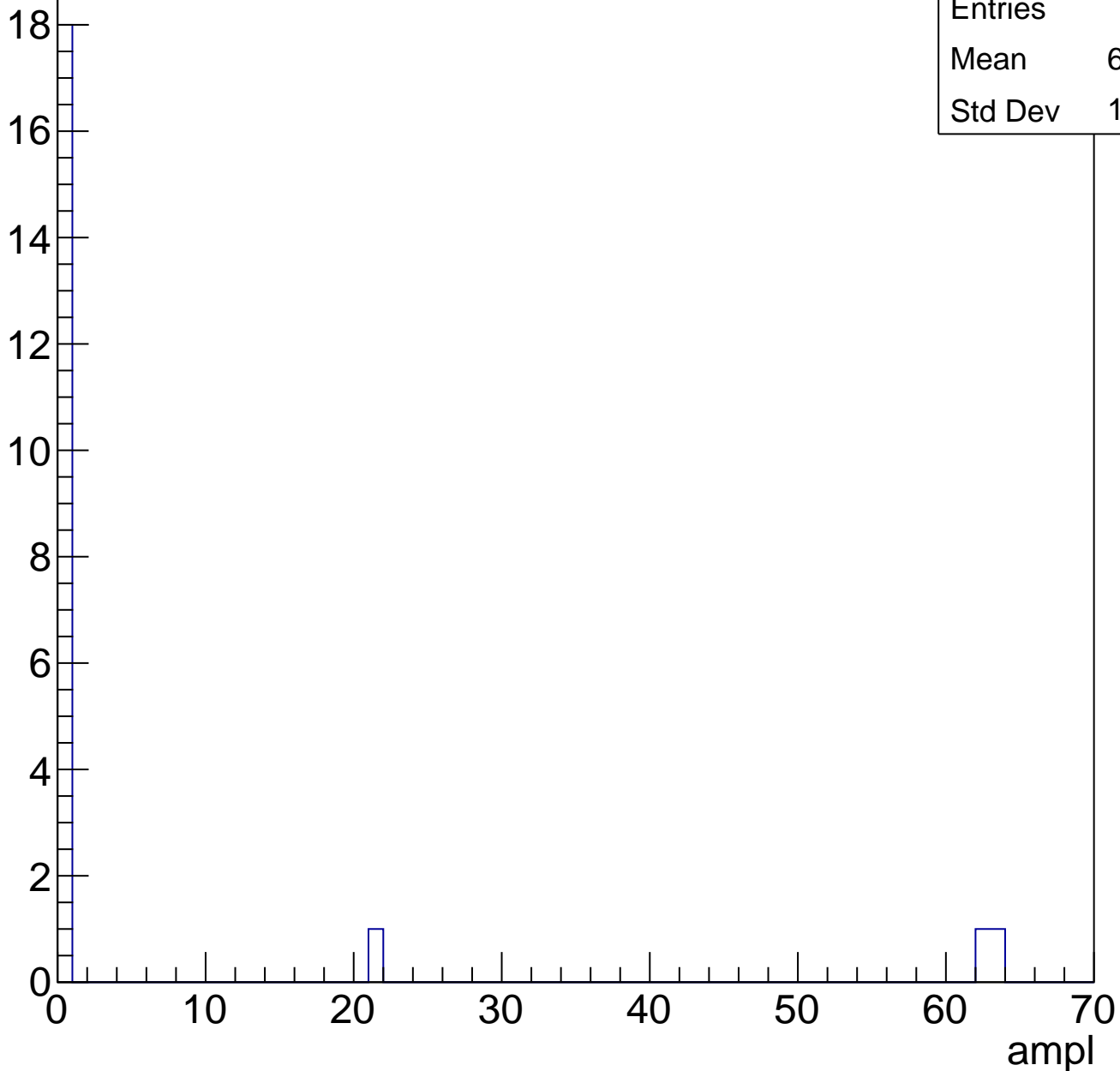


B1L103S, U5-ch71, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	6.952
Std Dev	18.57

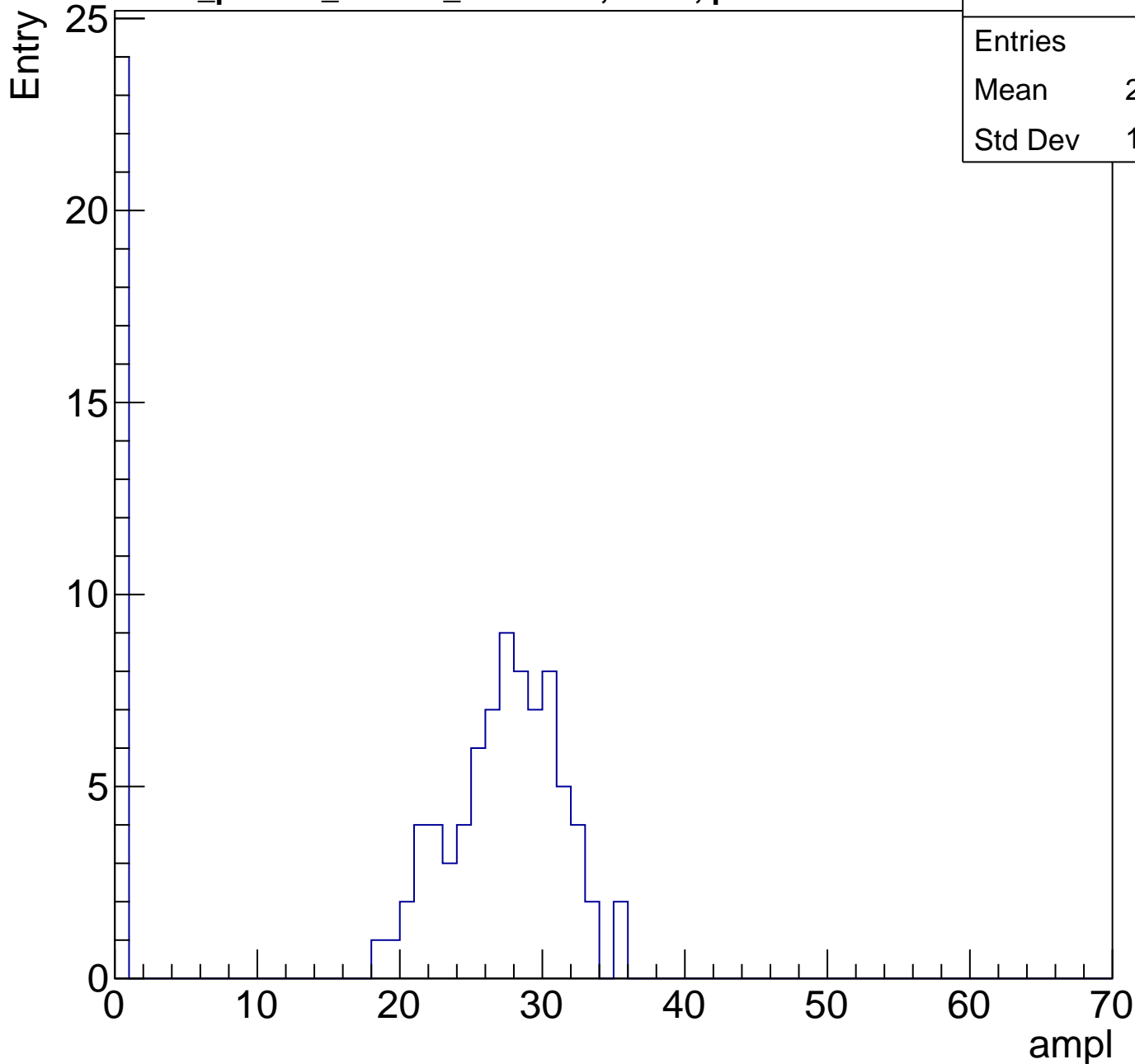
Entry



B1L103S, U5-ch72, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	101
Mean	20.54
Std Dev	11.93

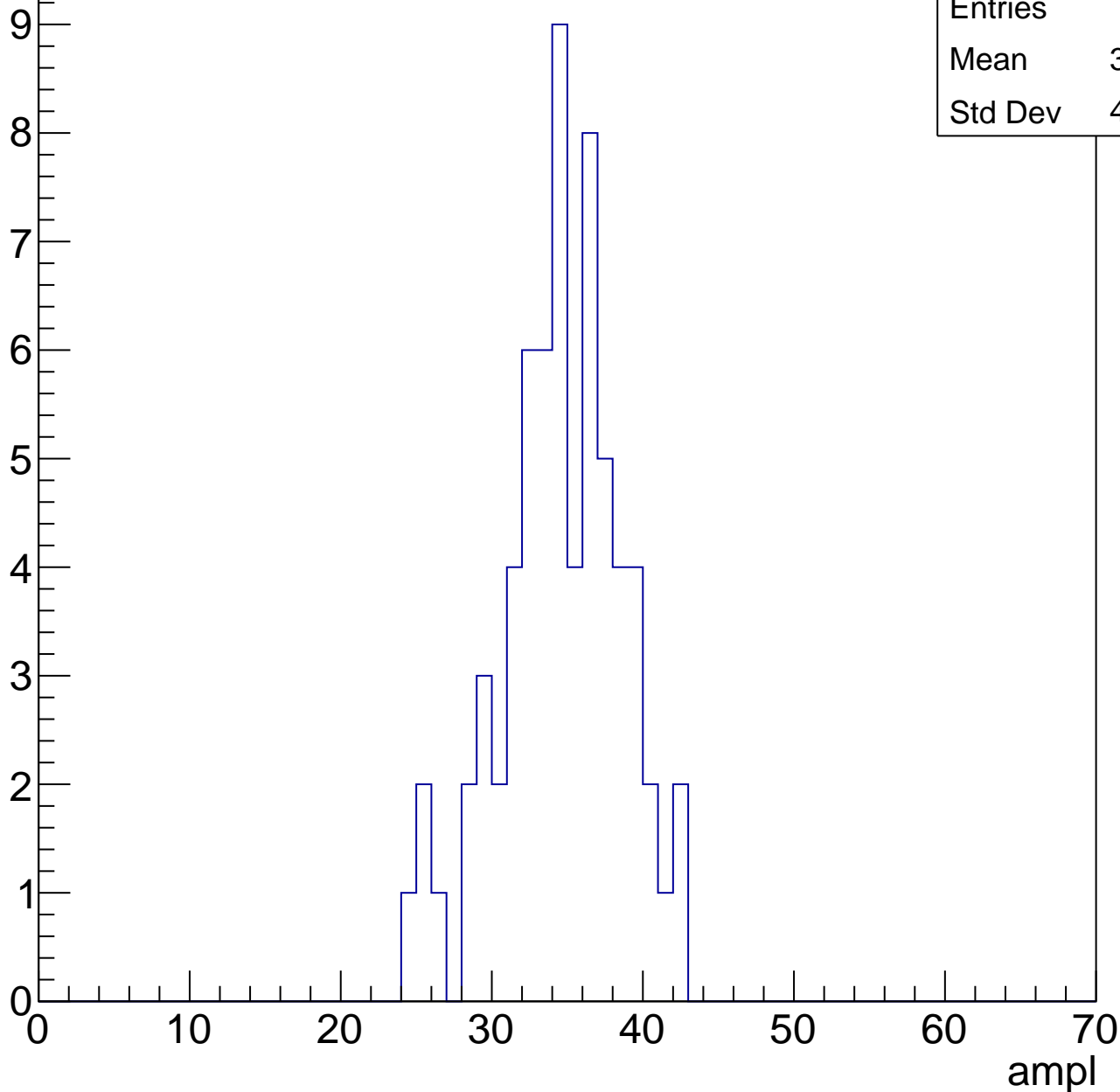


B1L103S, U5-ch72, adc1

calib_packv5_041523_1651.root, FC#0, port C2

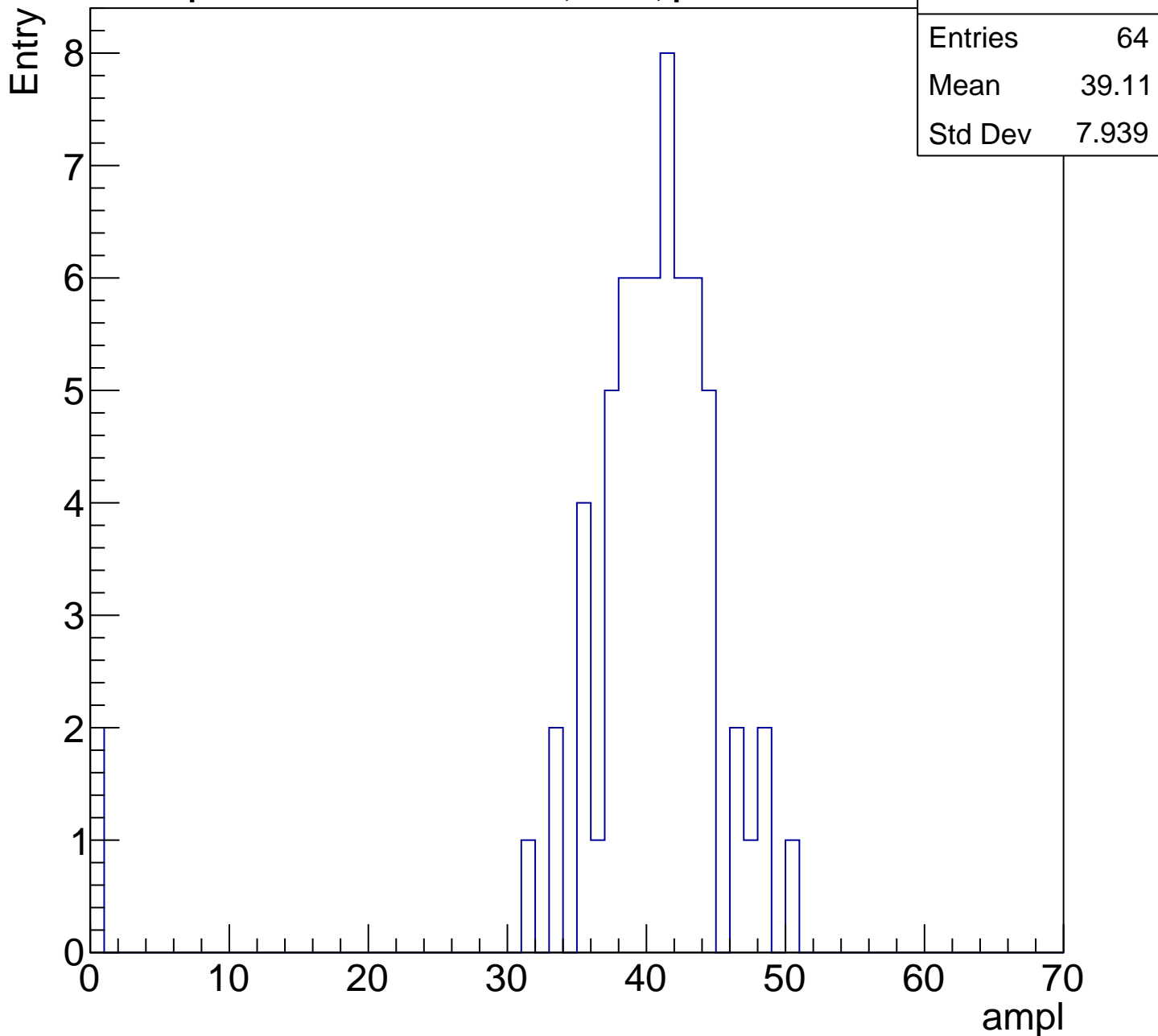
Entry

Entries	66
Mean	34.08
Std Dev	4.016



B1L103S, U5-ch72, adc2

calib_packv5_041523_1651.root, FC#0, port C2

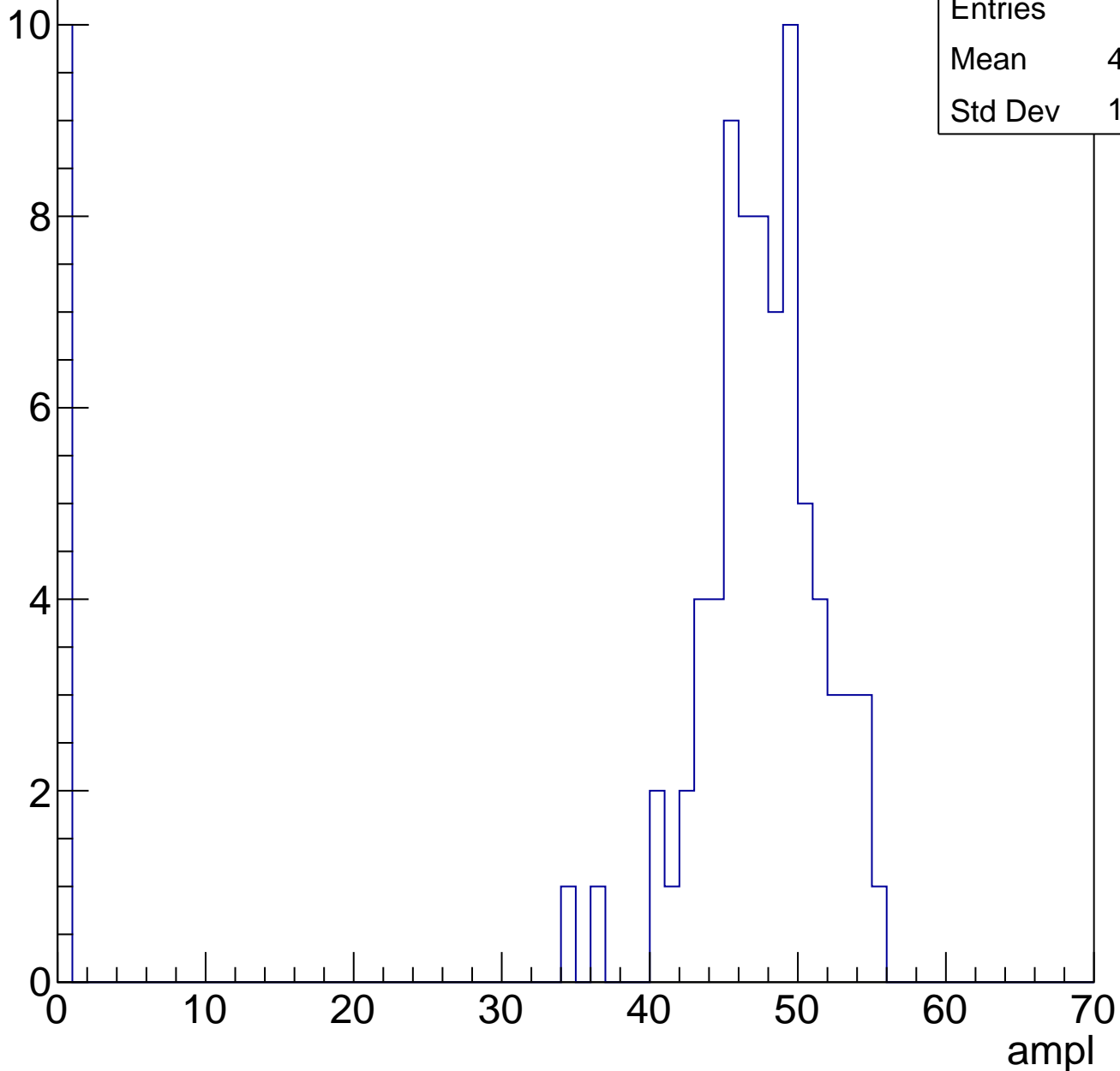


B1L103S, U5-ch72, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	86
Mean	41.67
Std Dev	15.56

Entry

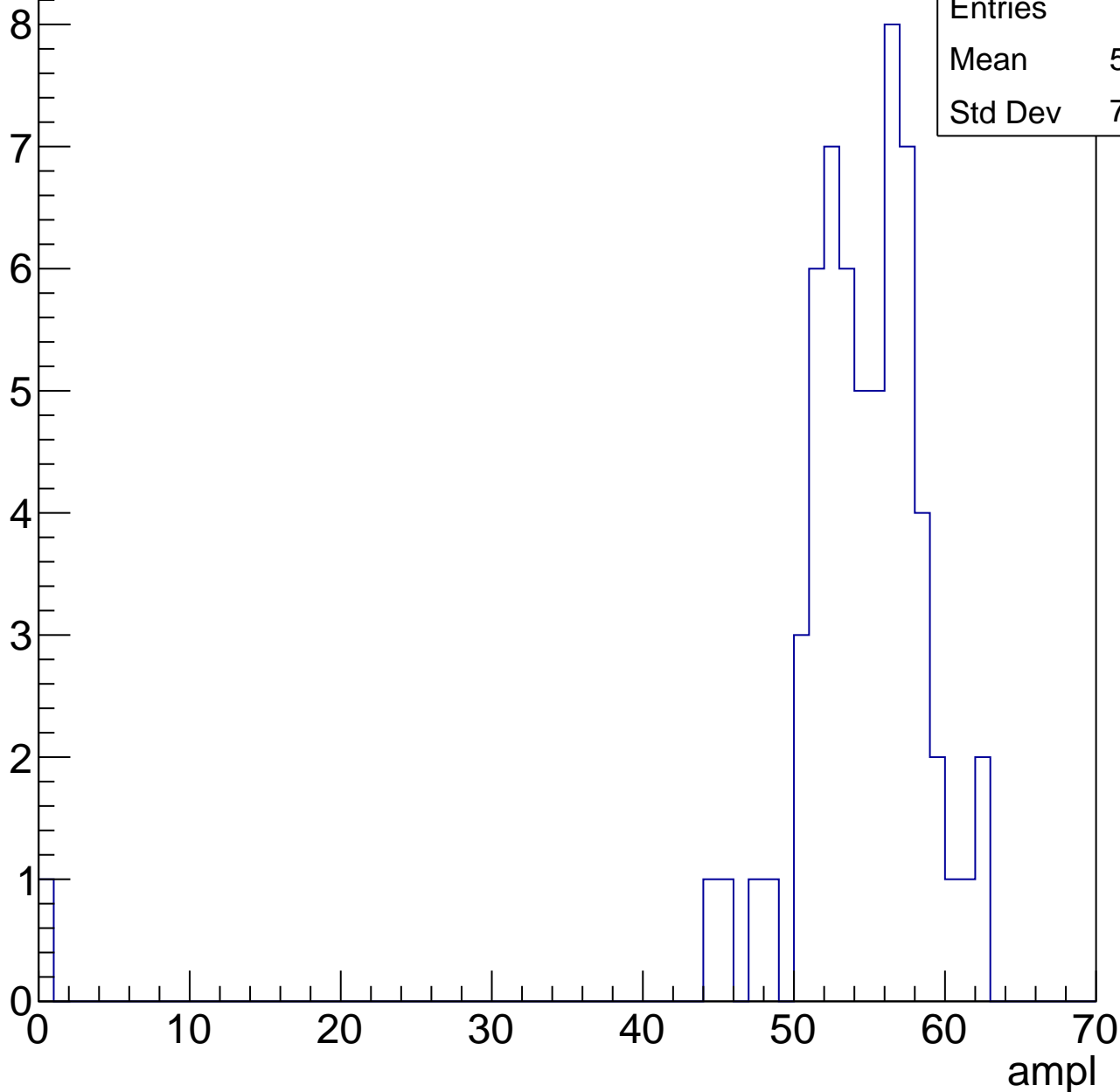


B1L103S, U5-ch72, adc4

calib_packv5_041523_1651.root, FC#0, port C2

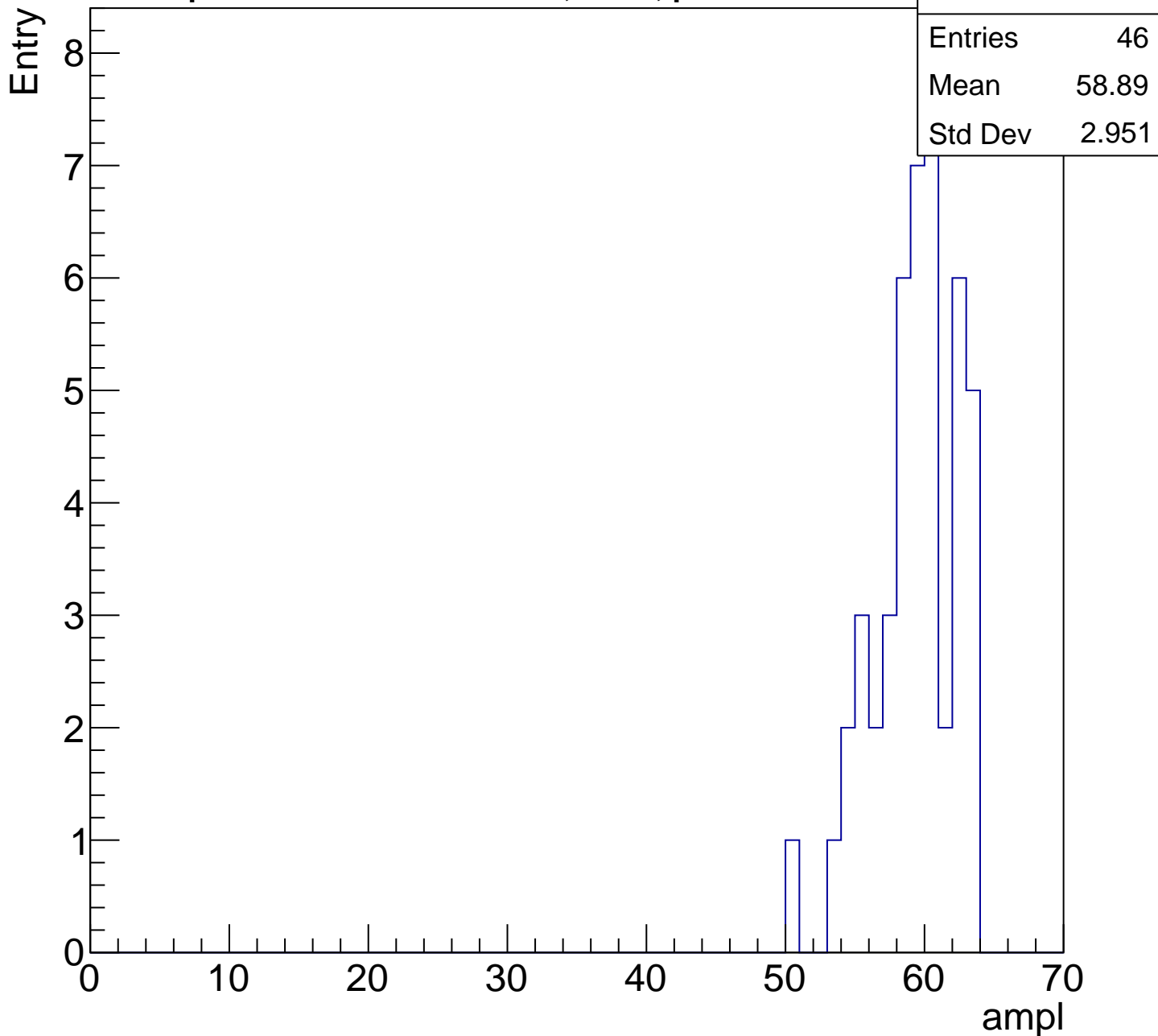
Entry

Entries	62
Mean	53.37
Std Dev	7.746



B1L103S, U5-ch72, adc5

calib_packv5_041523_1651.root, FC#0, port C2

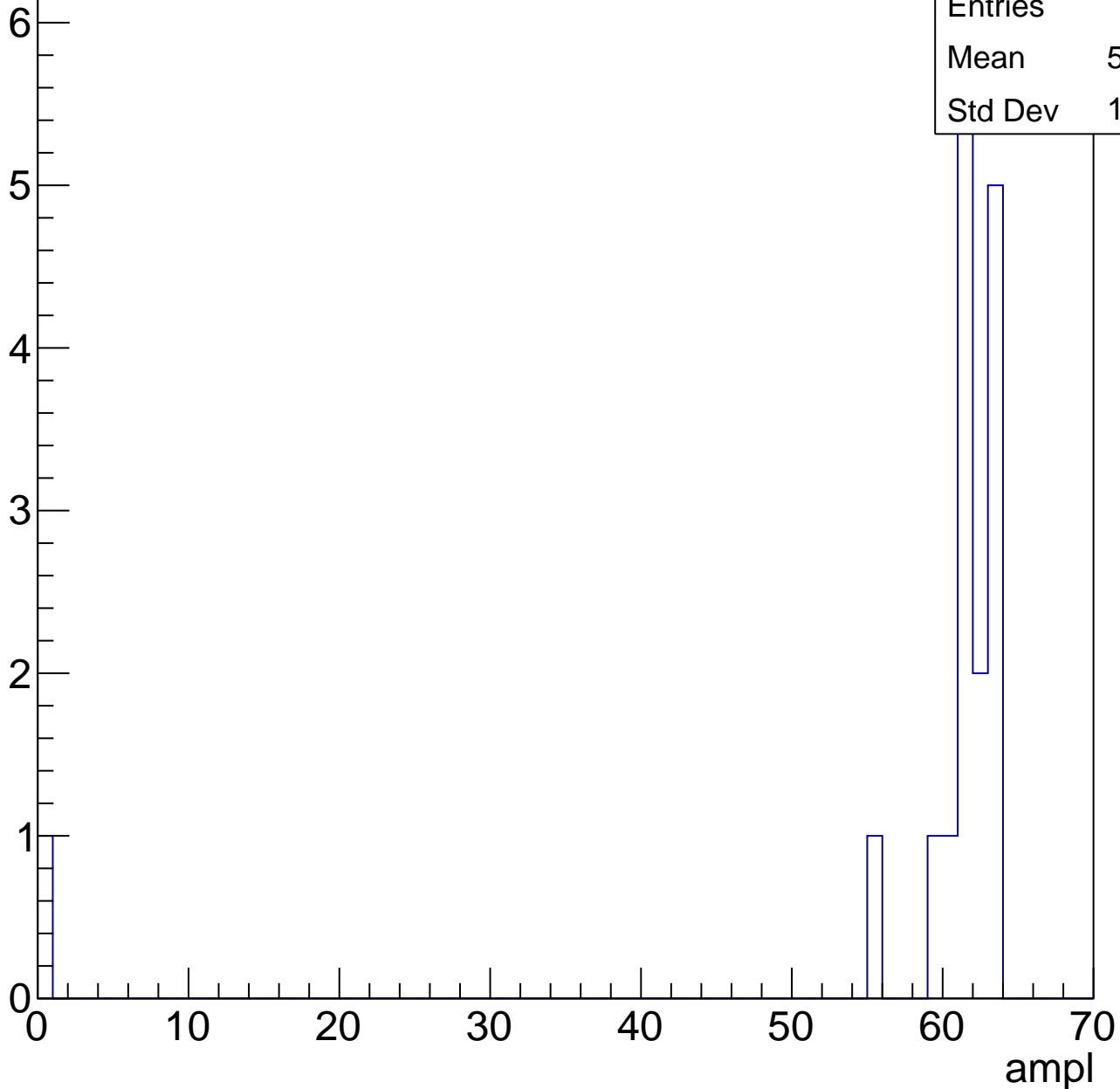


B1L103S, U5-ch72, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	17
Mean	57.59
Std Dev	14.52



B1L103S, U5-ch72, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.05
Std Dev	13.29

Entry



B1L103S, U5-ch73, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	23.27
Std Dev	11.85

Entry

16
14
12
10
8
6
4
2
0

0

10

20

30

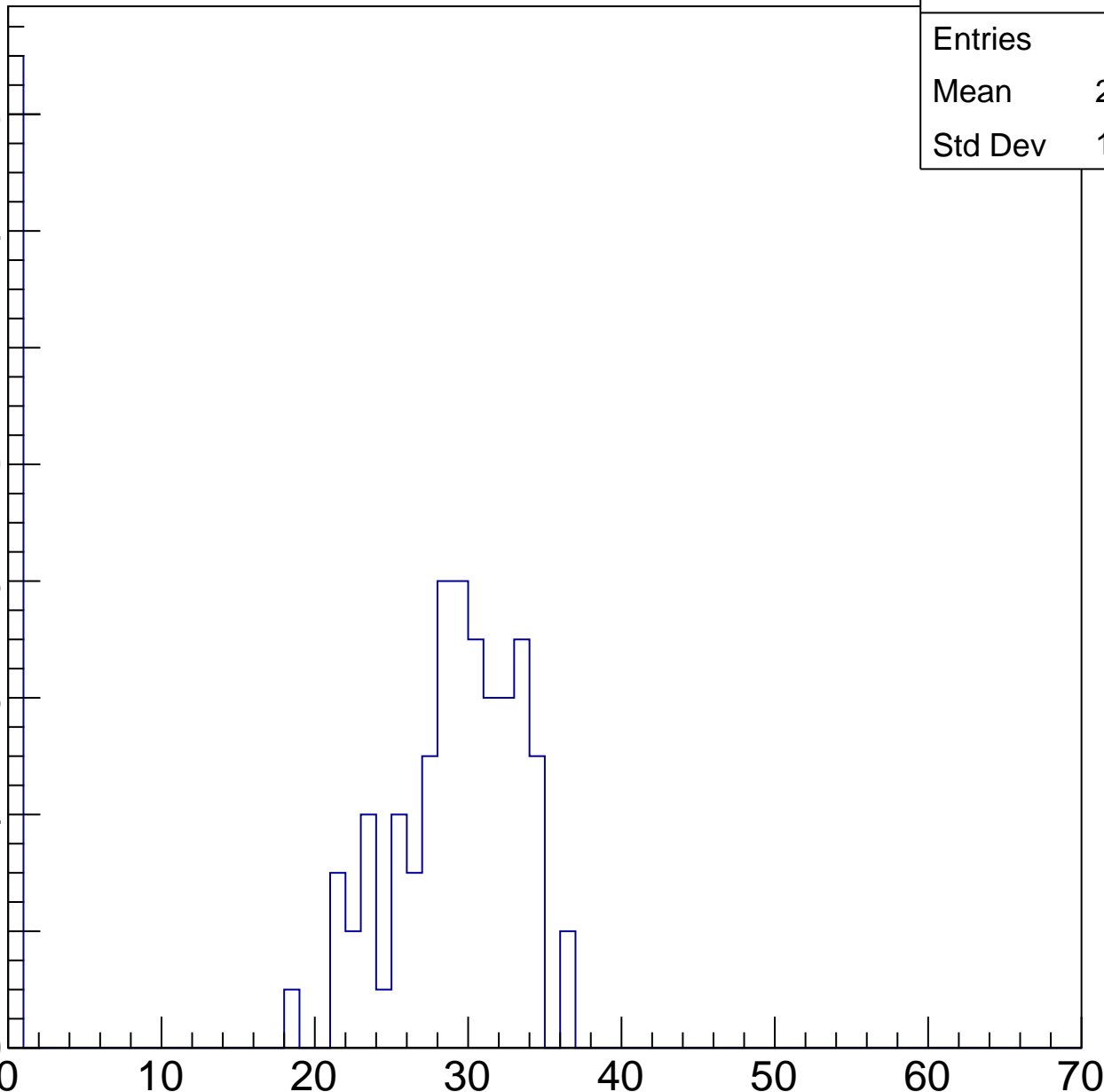
40

50

60

70

ampl

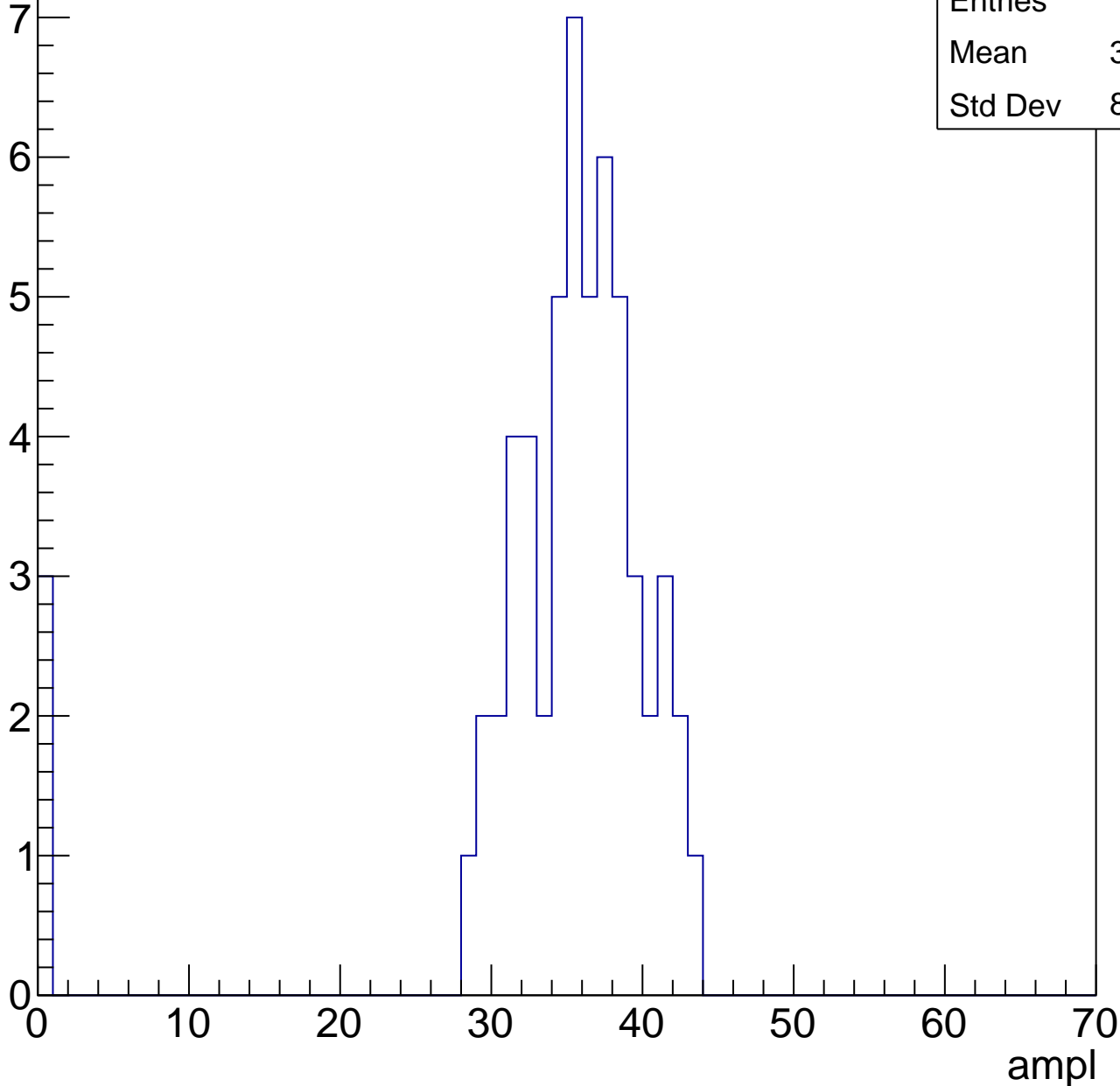


B1L103S, U5-ch73, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	33.65
Std Dev	8.682

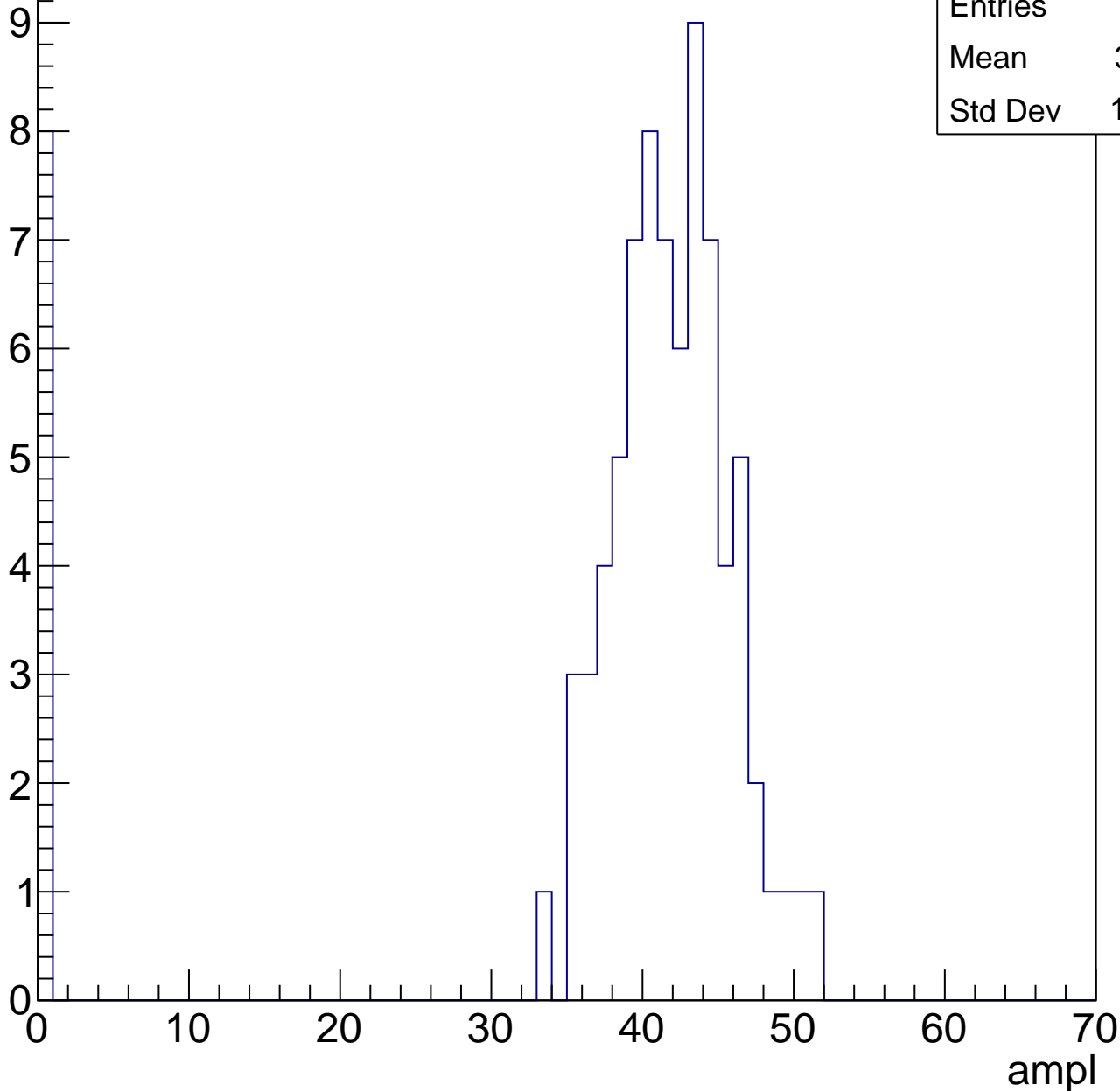


B1L103S, U5-ch73, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	83
Mean	37.51
Std Dev	12.75

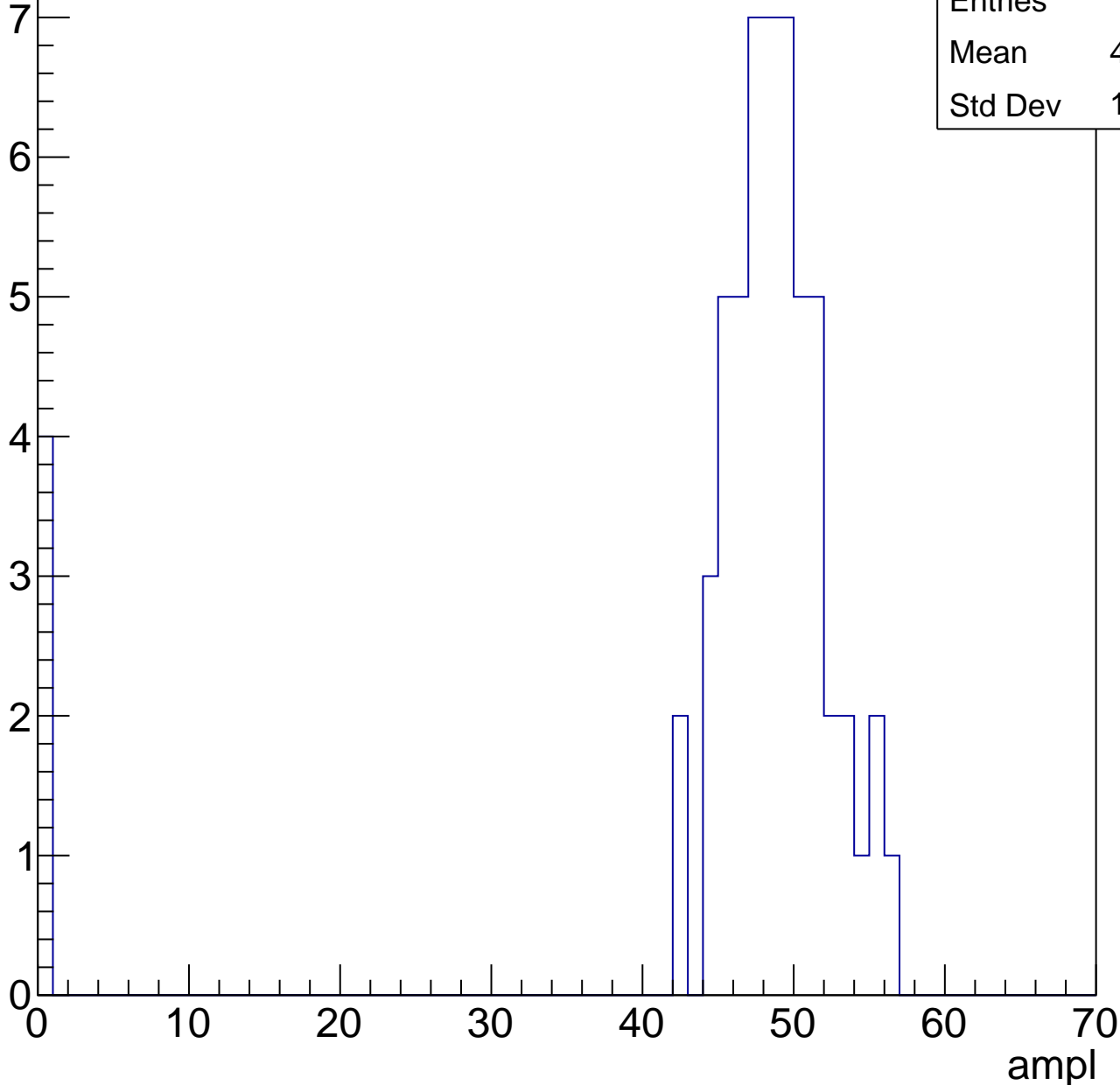


B1L103S, U5-ch73, adc3

calib_packv5_041523_1651.root, FC#0, port C2

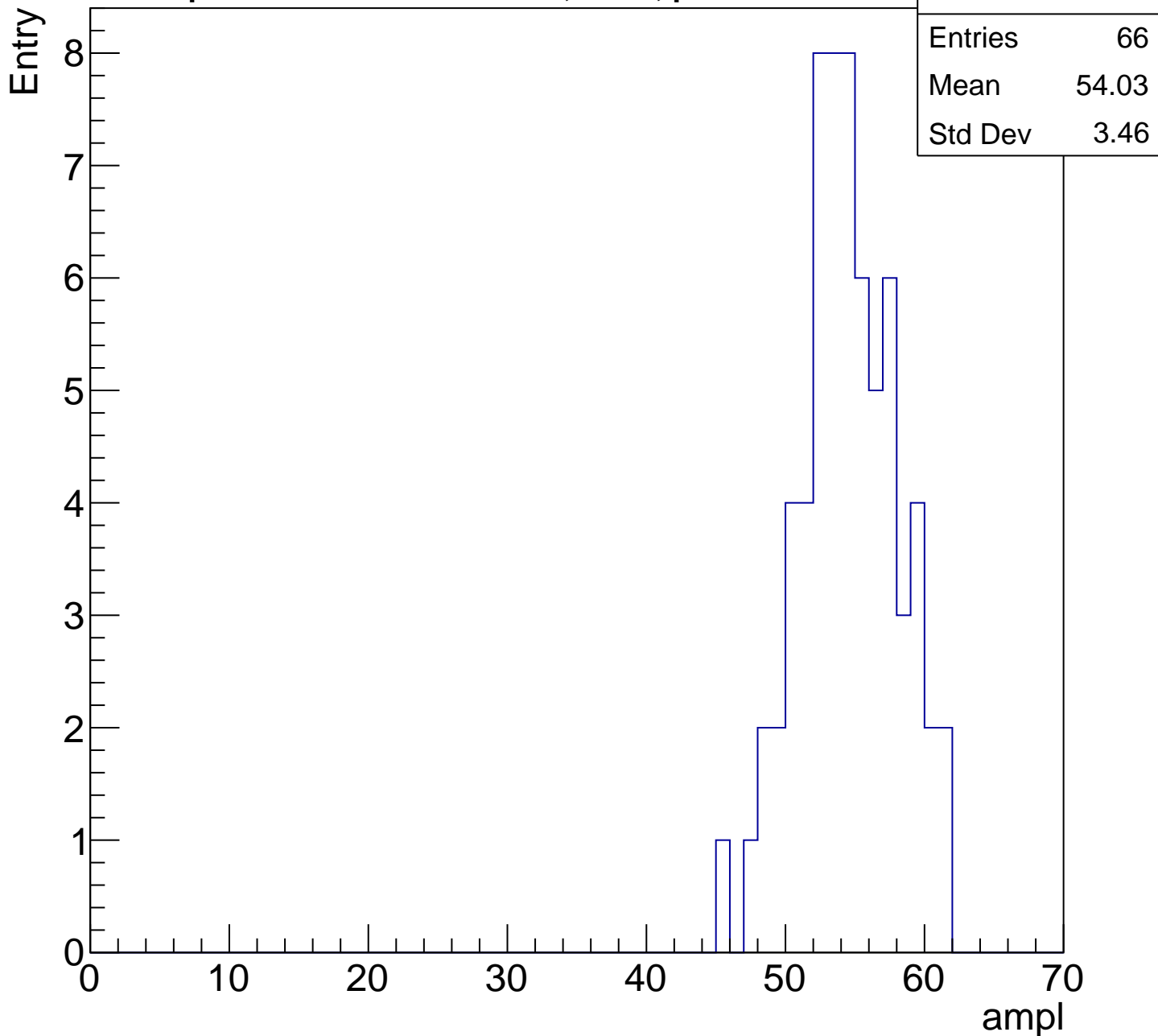
Entry

Entries	58
Mean	45.07
Std Dev	12.64



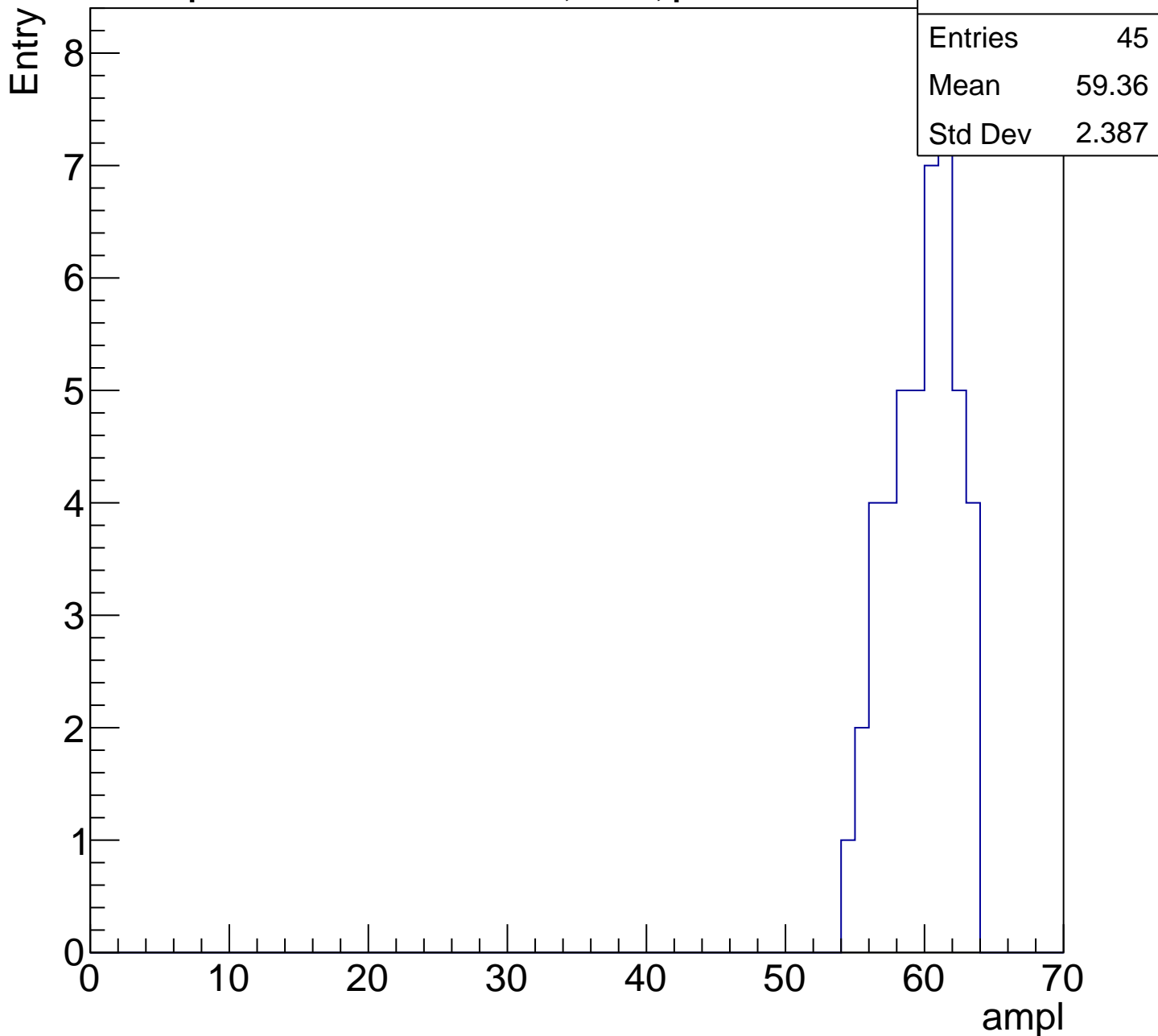
B1L103S, U5-ch73, adc4

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U5-ch73, adc5

calib_packv5_041523_1651.root, FC#0, port C2

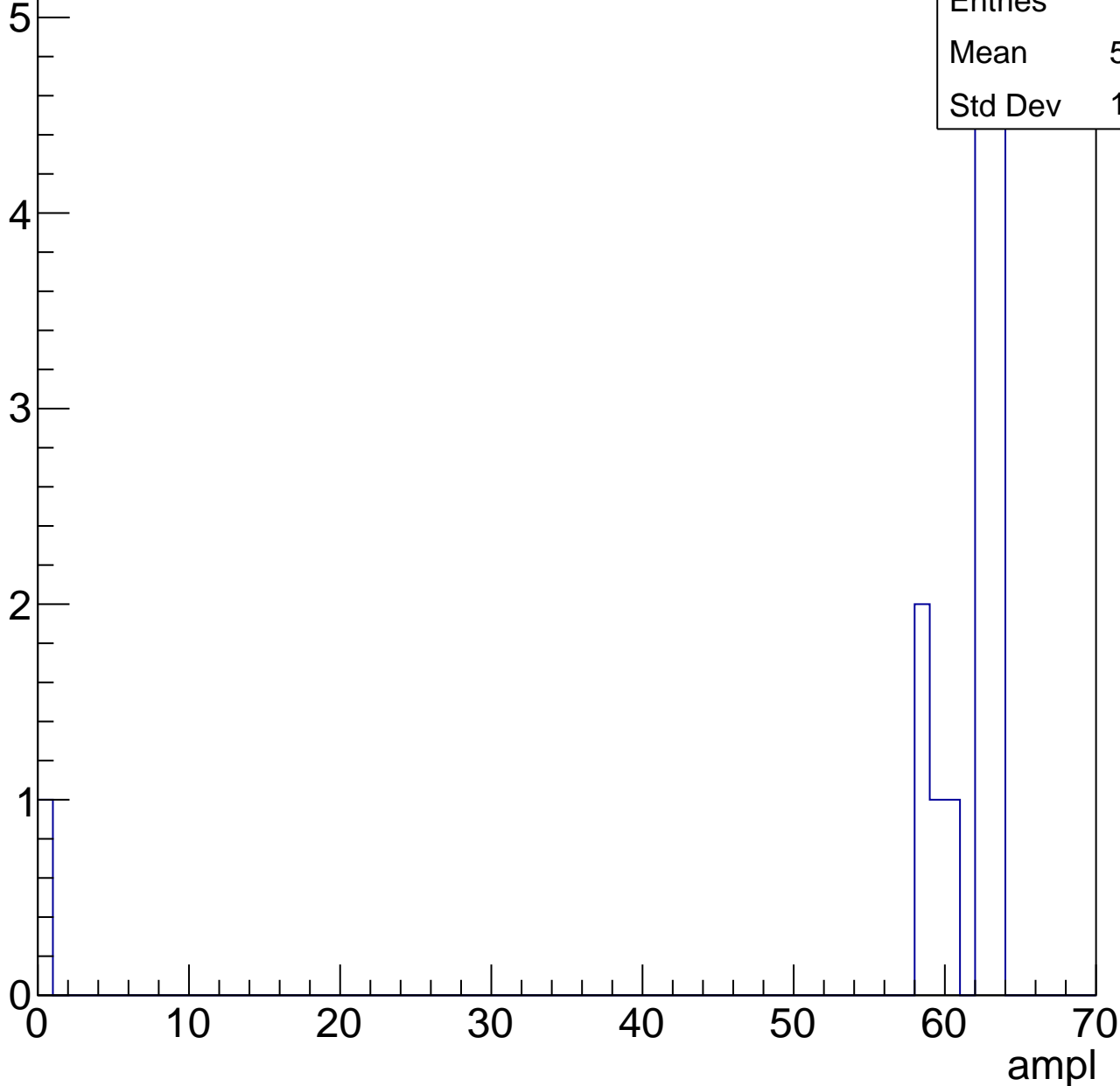


B1L103S, U5-ch73, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	15
Mean	57.33
Std Dev	15.42



B1L103S, U5-ch73, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	20
Mean	3.15
Std Dev	13.73

ampl

0 10 20 30 40 50 60 70

B1L103S, U5-ch74, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

25
20
15
10
5
0

Entries	95
Mean	21.36
Std Dev	12.87

ampl

0

10

20

30

40

50

60

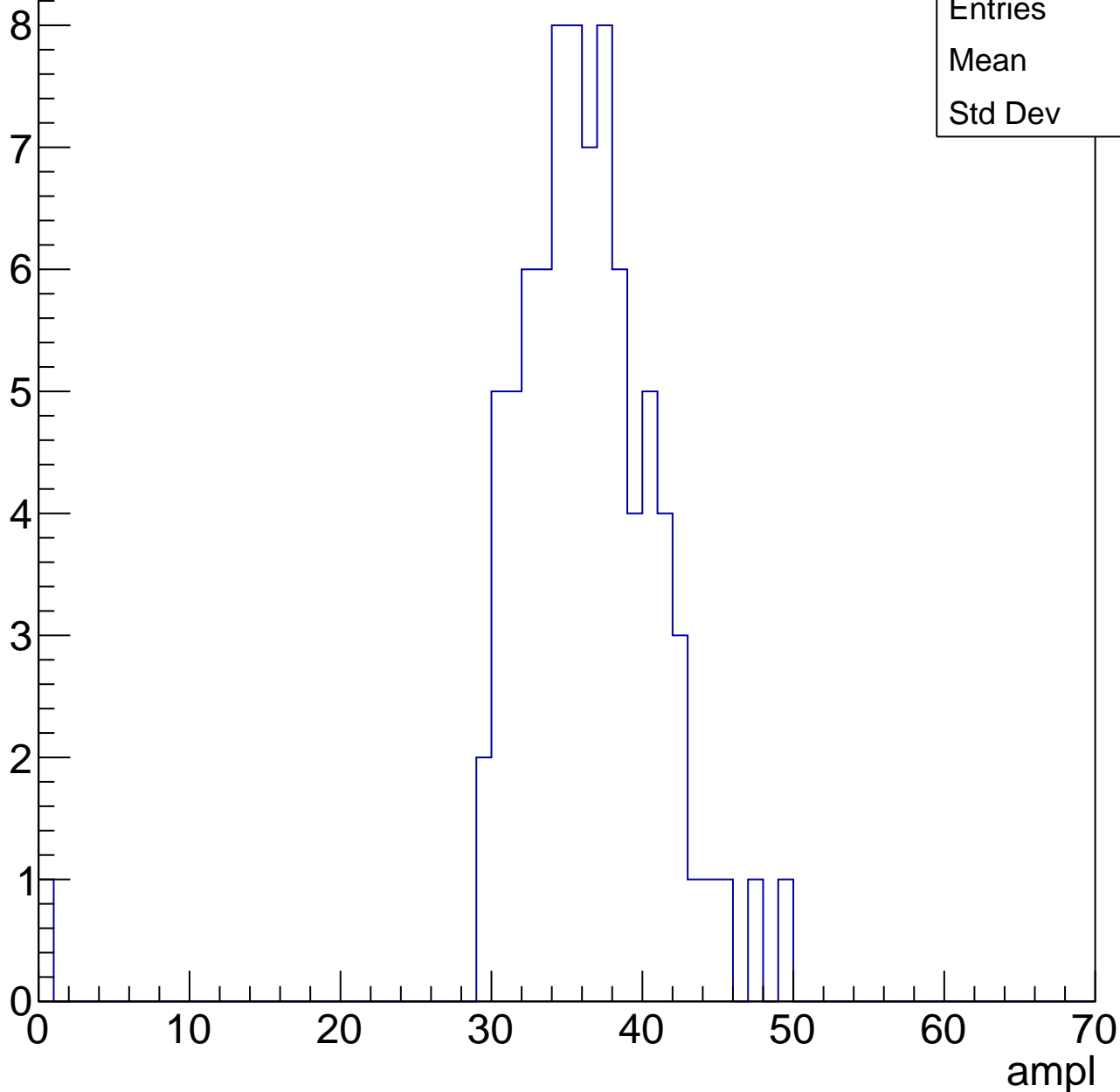
70

B1L103S, U5-ch74, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	83
Mean	35.6
Std Dev	5.72

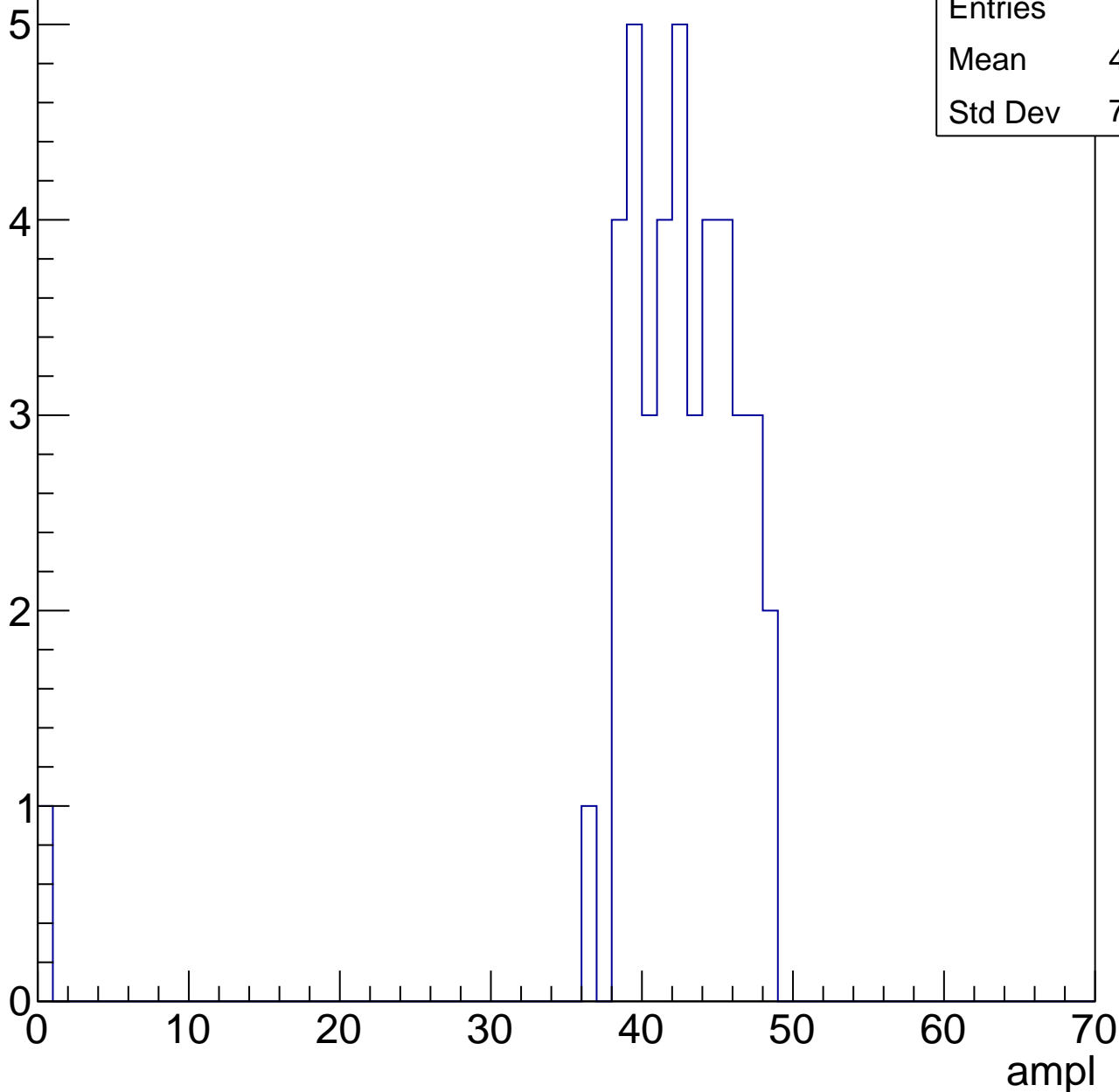


B1L103S, U5-ch74, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	42
Mean	41.36
Std Dev	7.167



B1L103S, U5-ch74, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	69
Mean	38.14
Std Dev	18.68

Entry

12

10

8

6

4

2

0

0

10

20

30

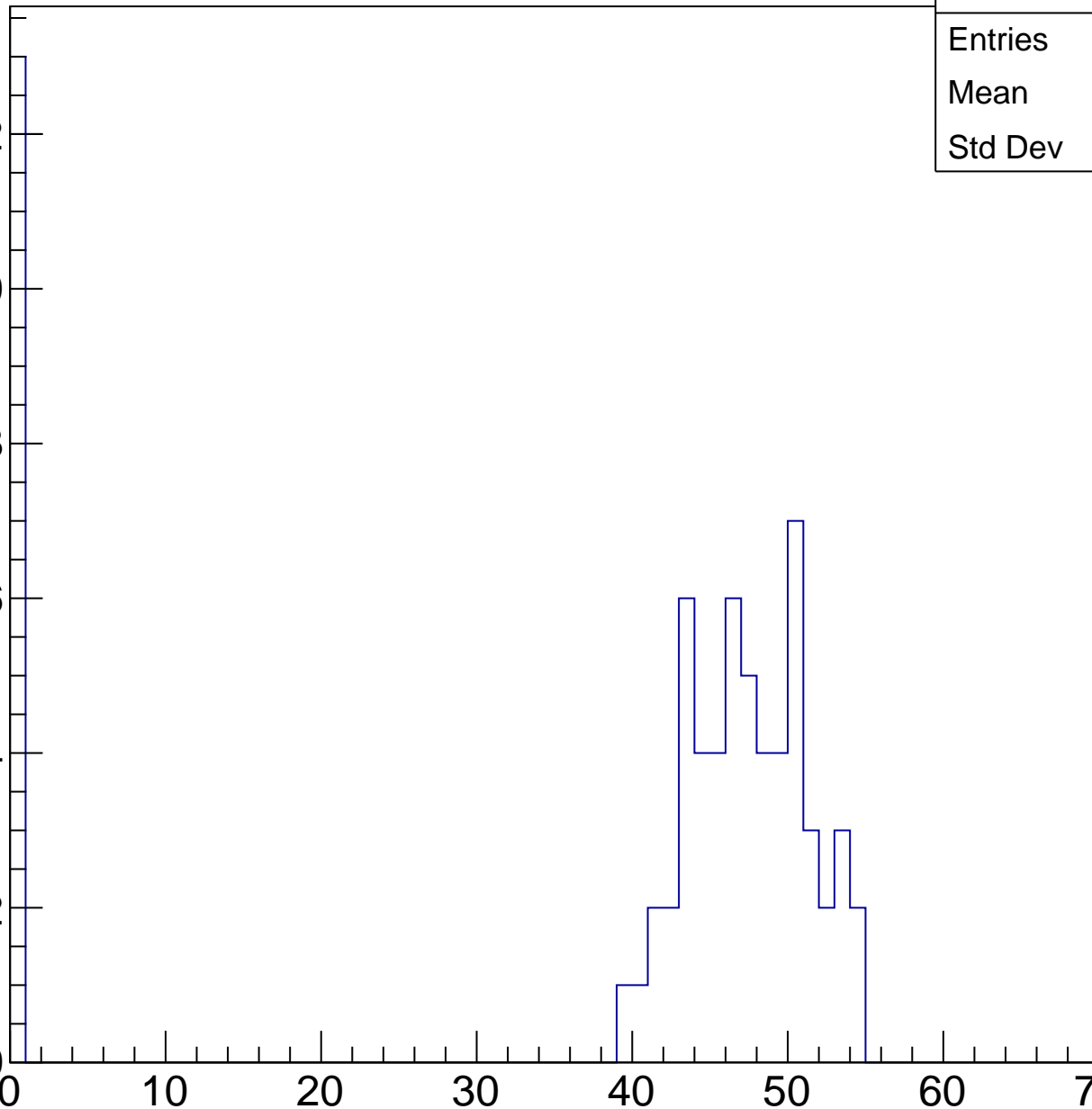
40

50

60

70

ampl

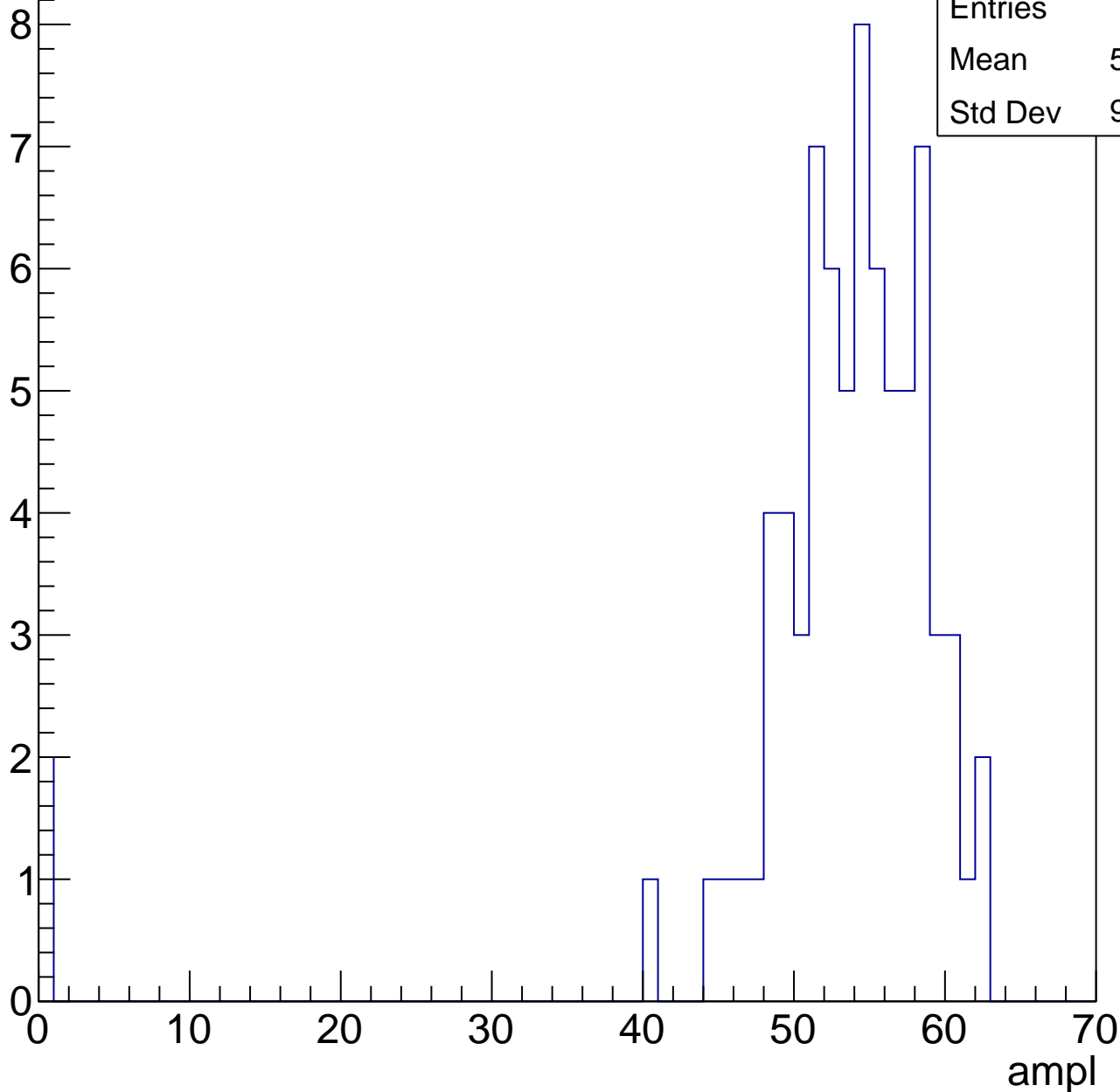


B1L103S, U5-ch74, adc4

calib_packv5_041523_1651.root, FC#0, port C2

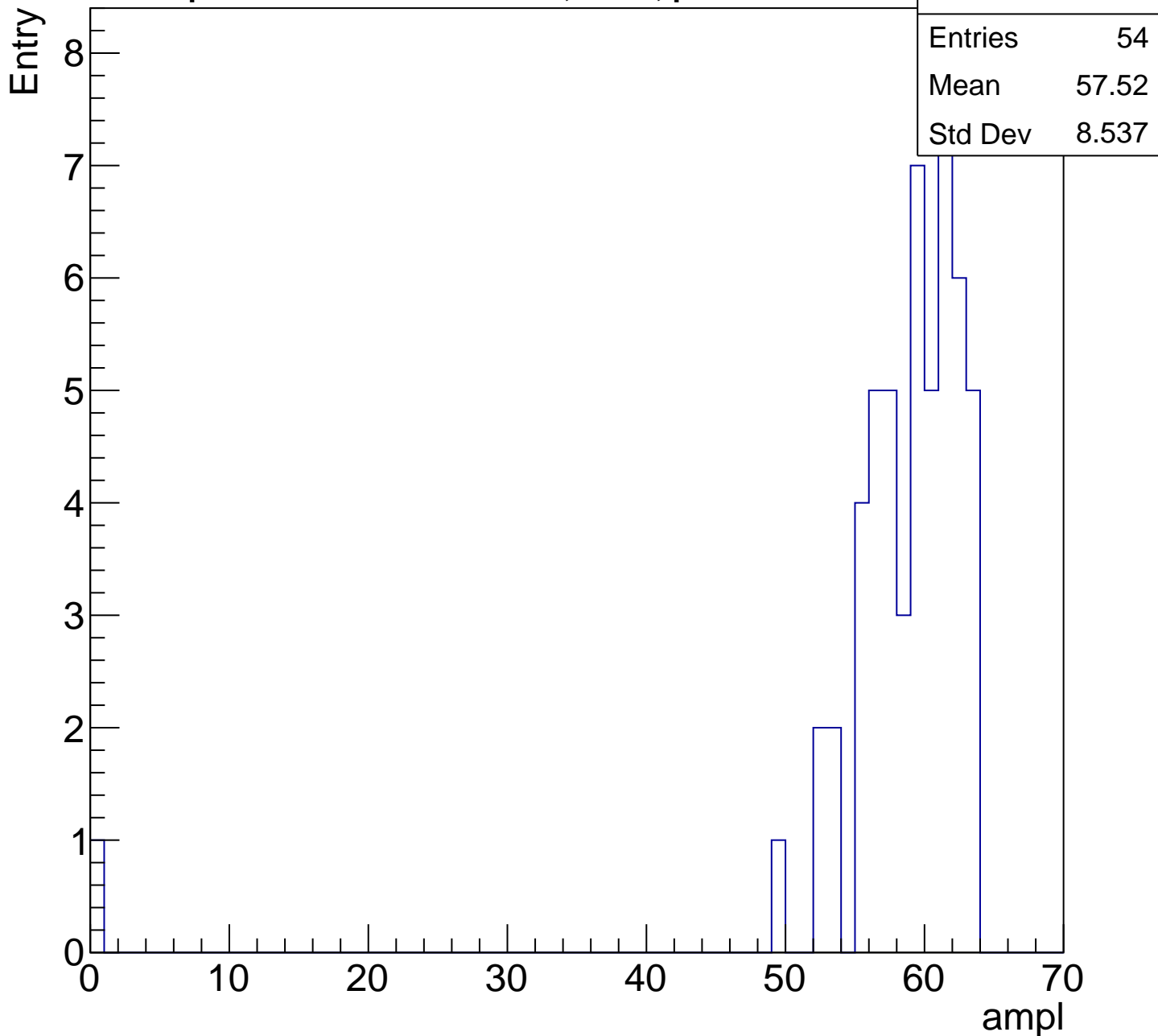
Entry

Entries	76
Mean	52.22
Std Dev	9.603



B1L103S, U5-ch74, adc5

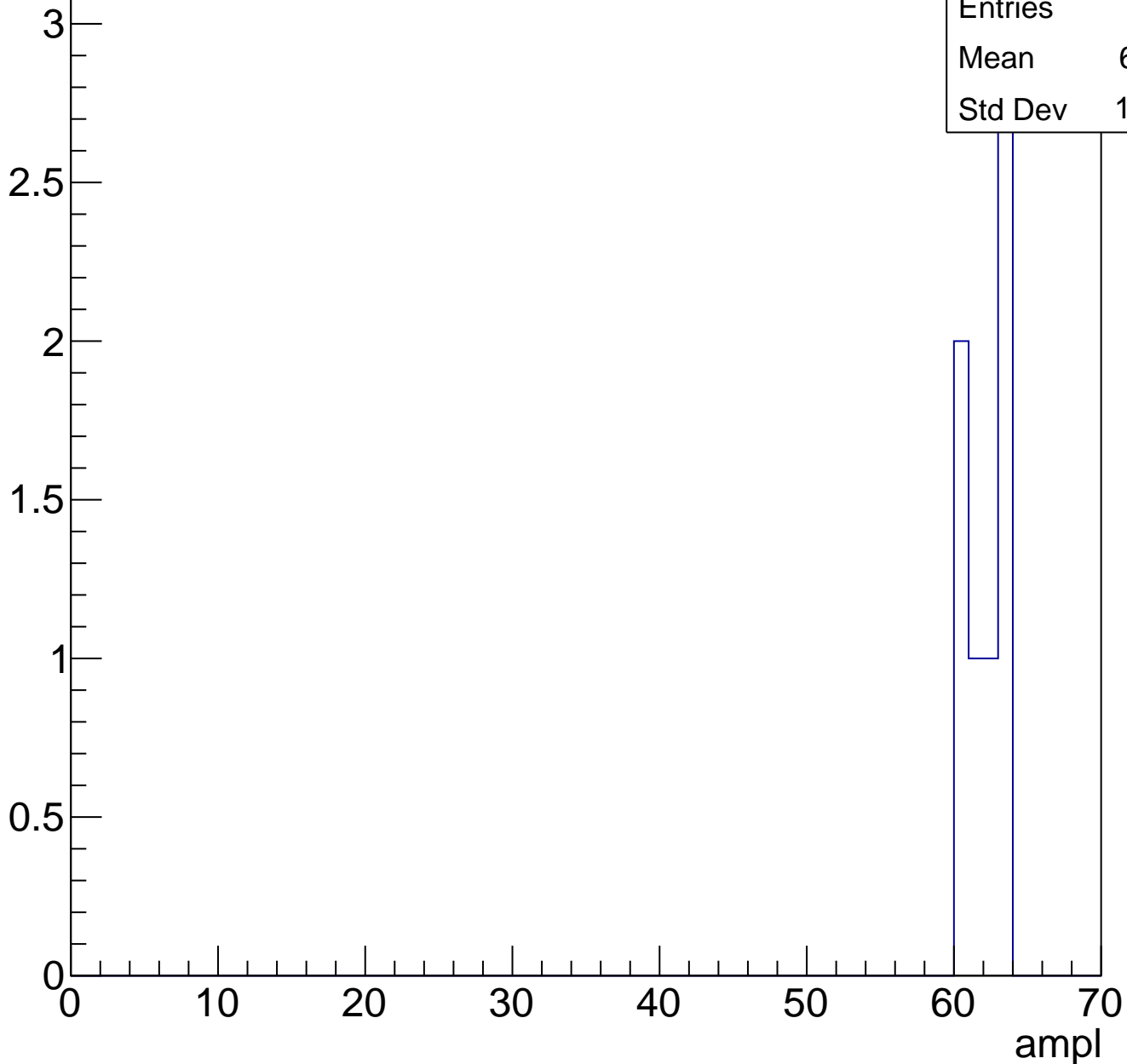
calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U5-ch74, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch74, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	22
Mean	8.545
Std Dev	21.51

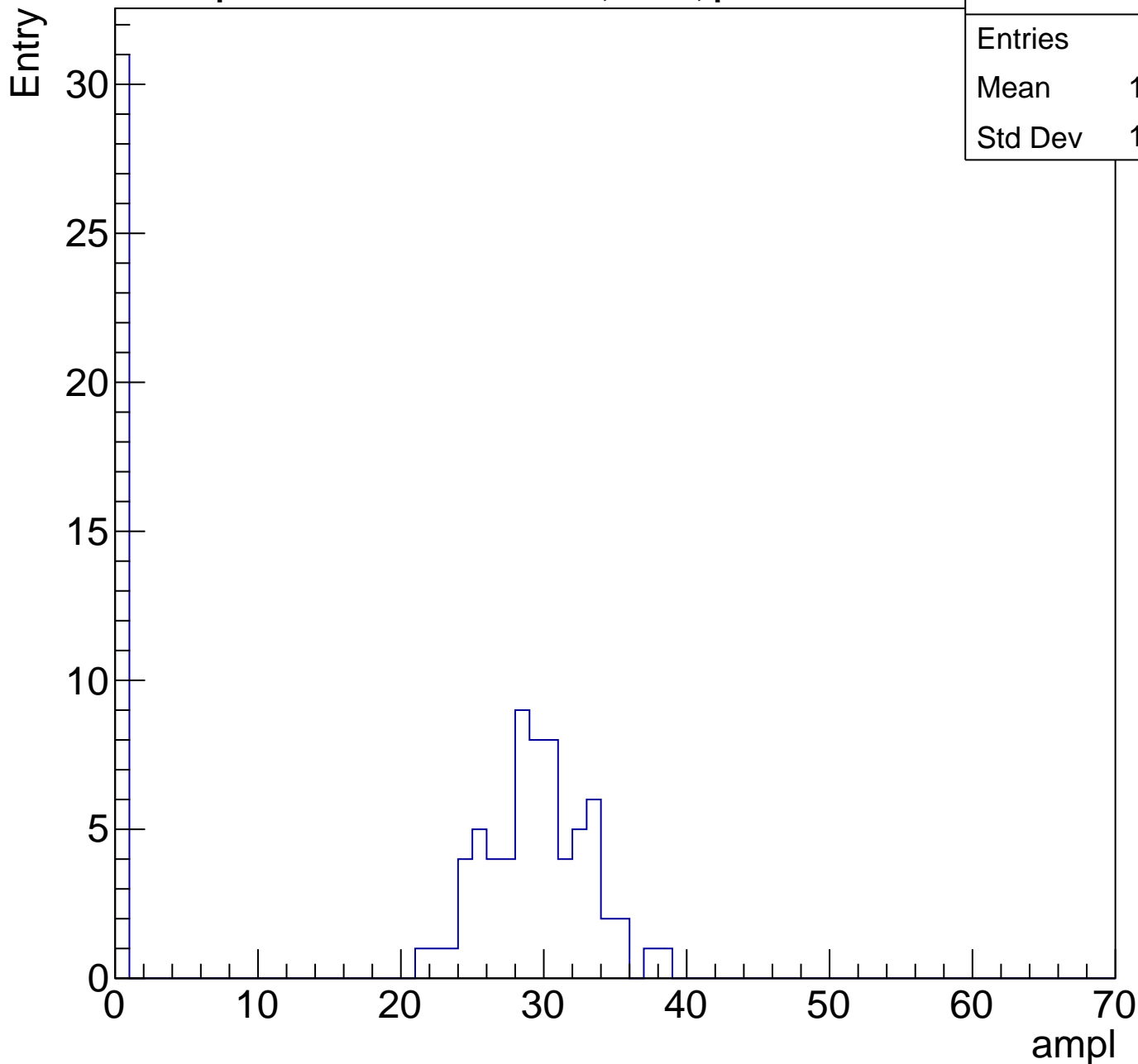
Entry



B1L103S, U5-ch75, adc0

calib_packv5_041523_1651.root, FC#0, port C2

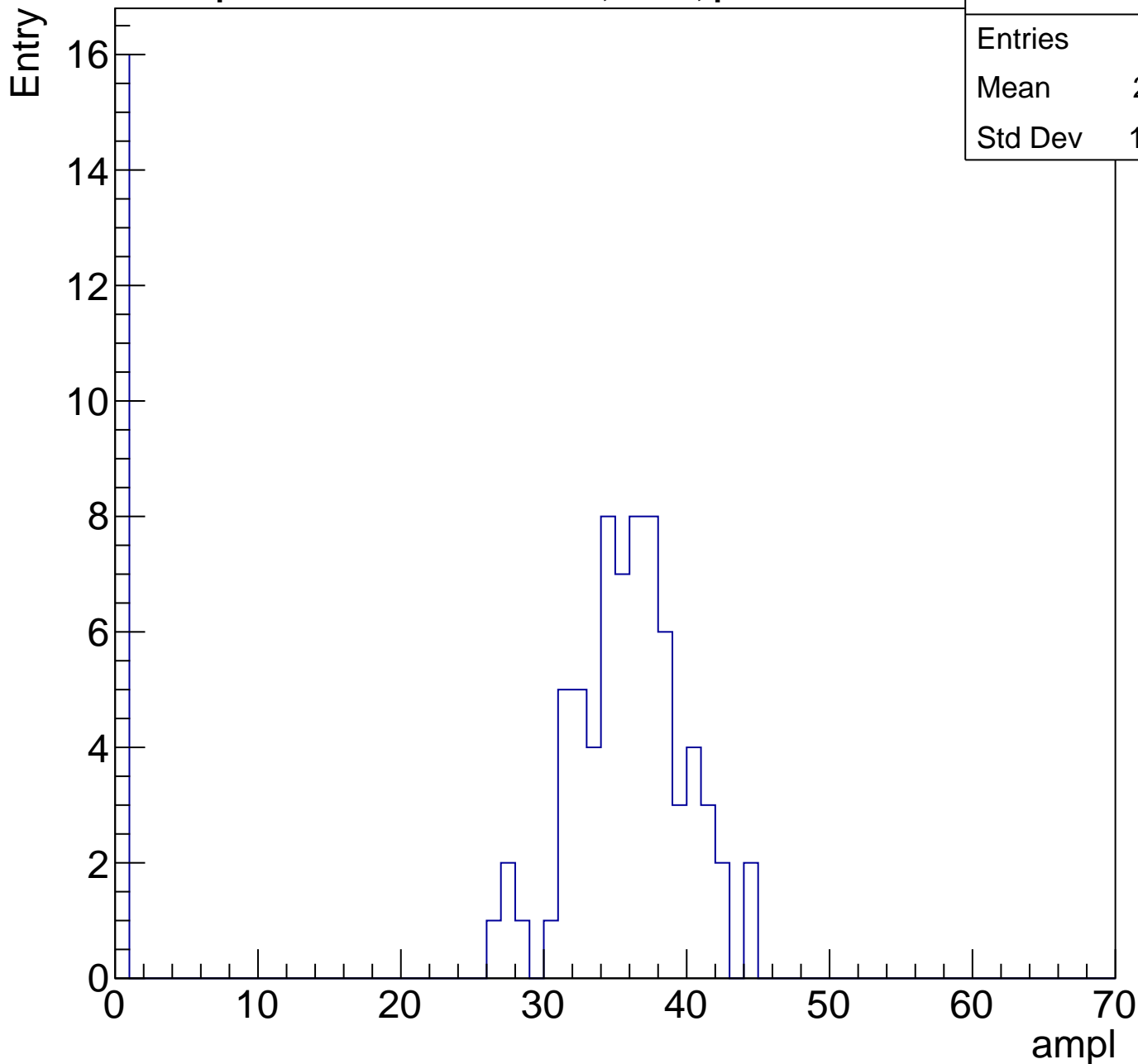
Entries	97
Mean	19.77
Std Dev	13.86



B1L103S, U5-ch75, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	86
Mean	28.91
Std Dev	14.24

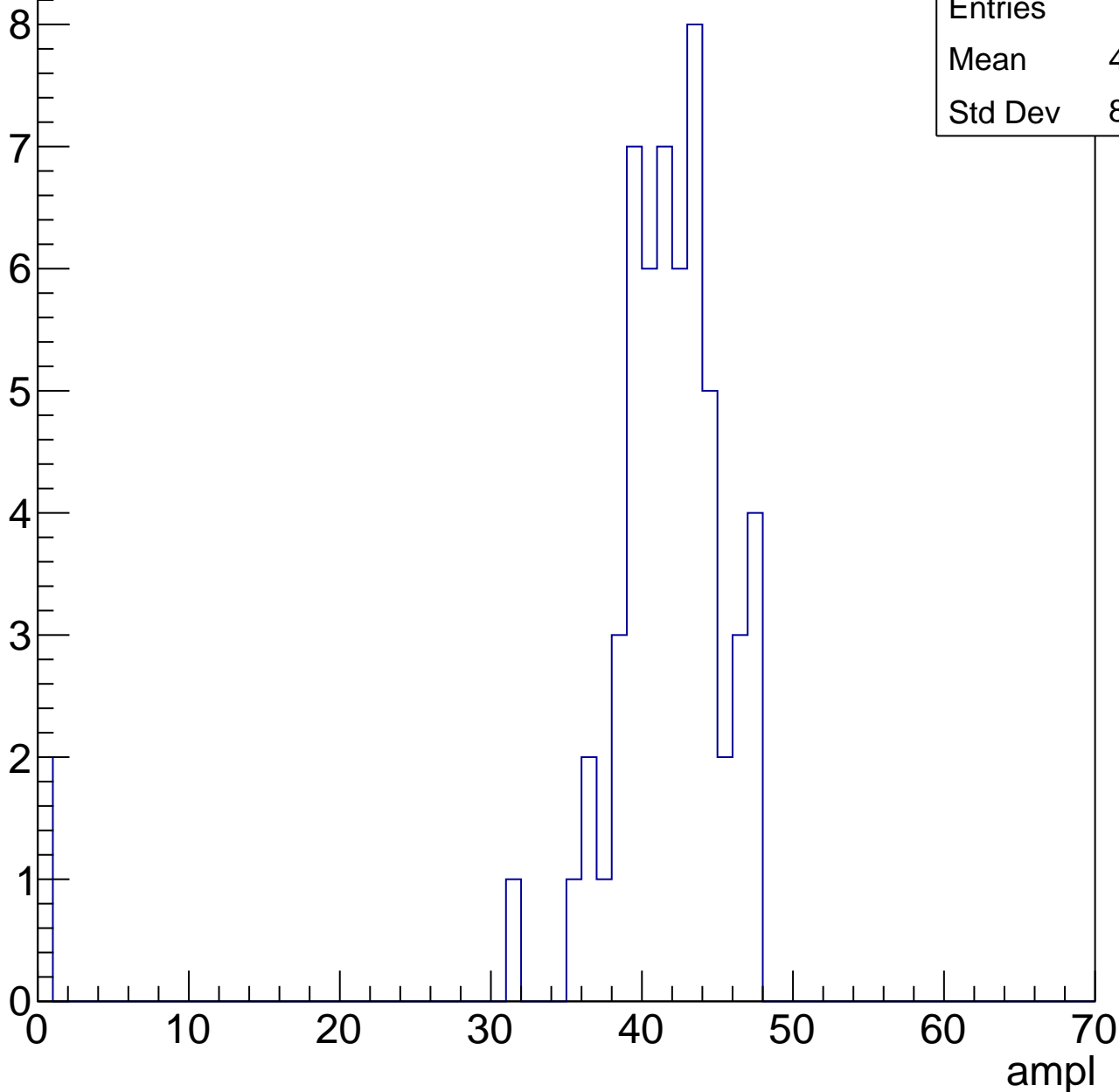


B1L103S, U5-ch75, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	40.02
Std Dev	8.203



B1L103S, U5-ch75, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	48.89
Std Dev	3.381

Entry

10

8

6

4

2

0

0

10

20

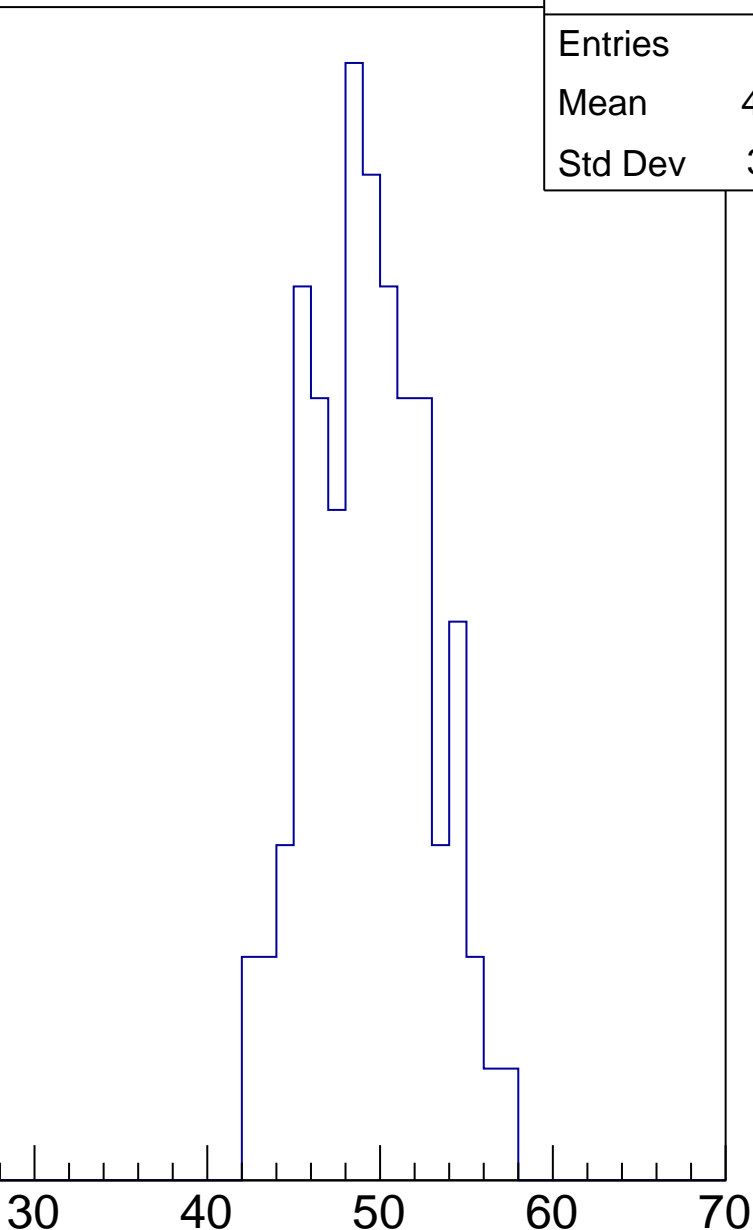
30

40

50

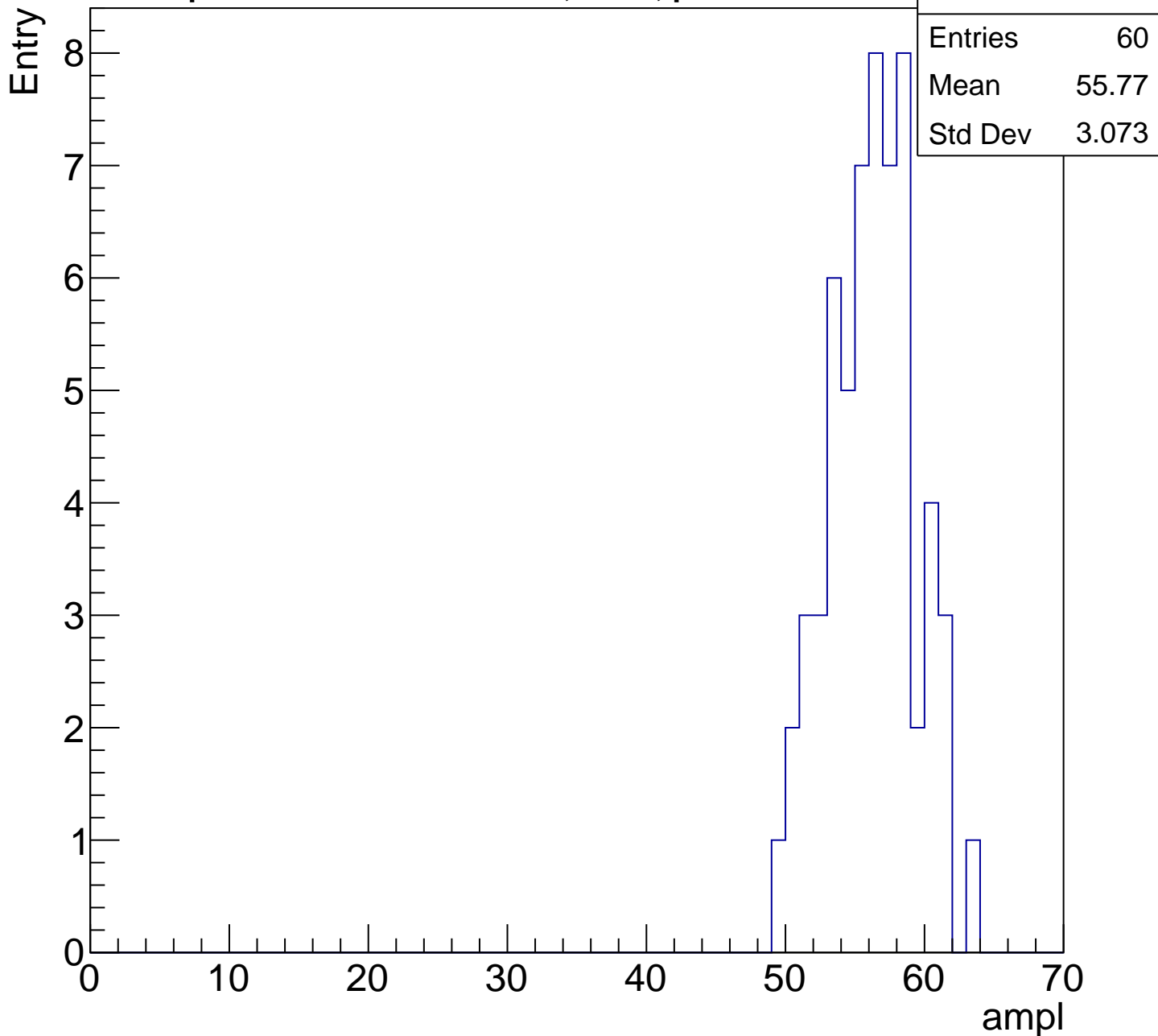
60

ampl



B1L103S, U5-ch75, adc4

calib_packv5_041523_1651.root, FC#0, port C2

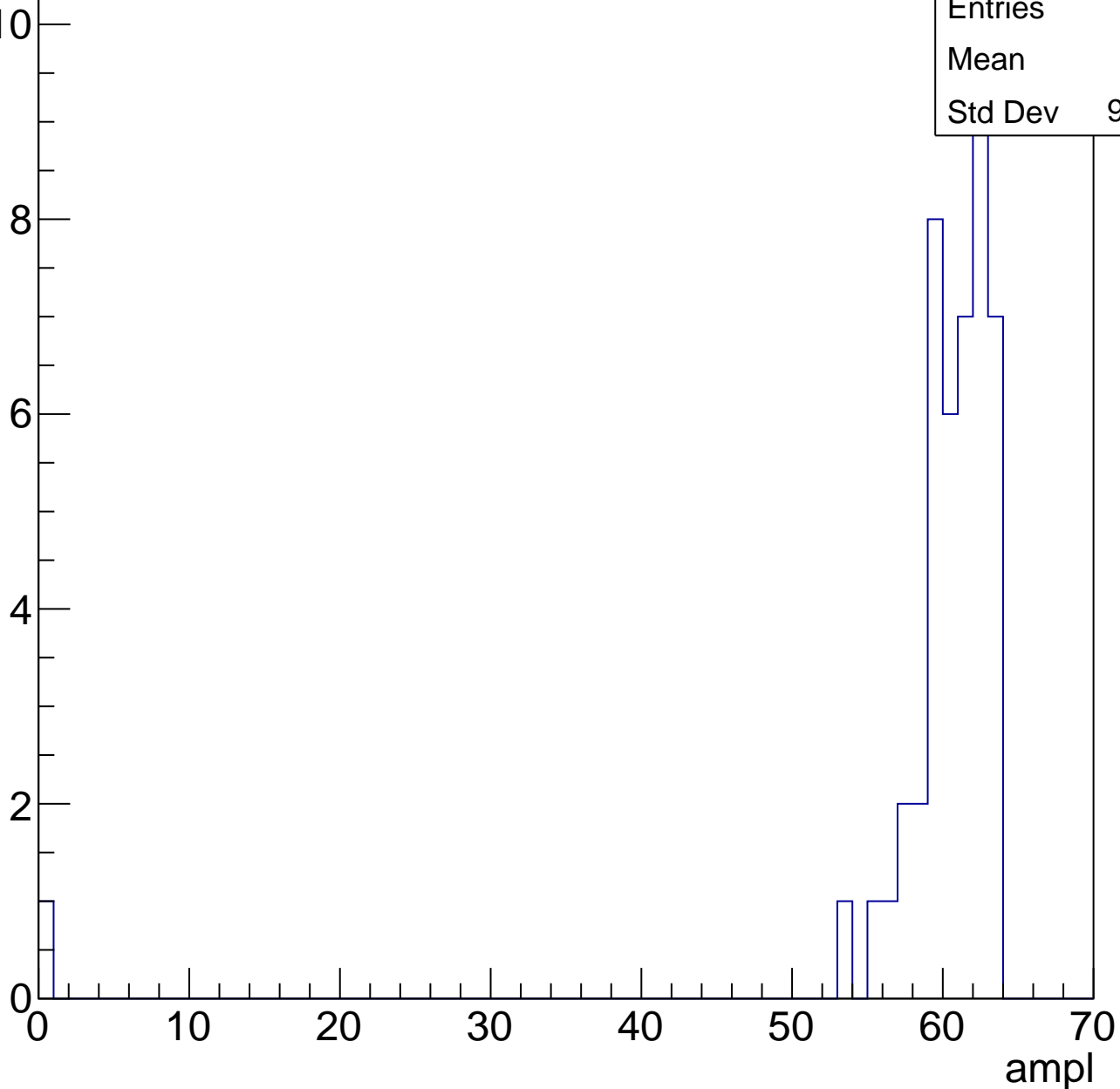


B1L103S, U5-ch75, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	46
Mean	59
Std Dev	9.075



B1L103S, U5-ch75, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch75, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch76, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	86
Mean	23.08
Std Dev	10.23

Entry

12

10

8

6

4

2

0

0

10

20

30

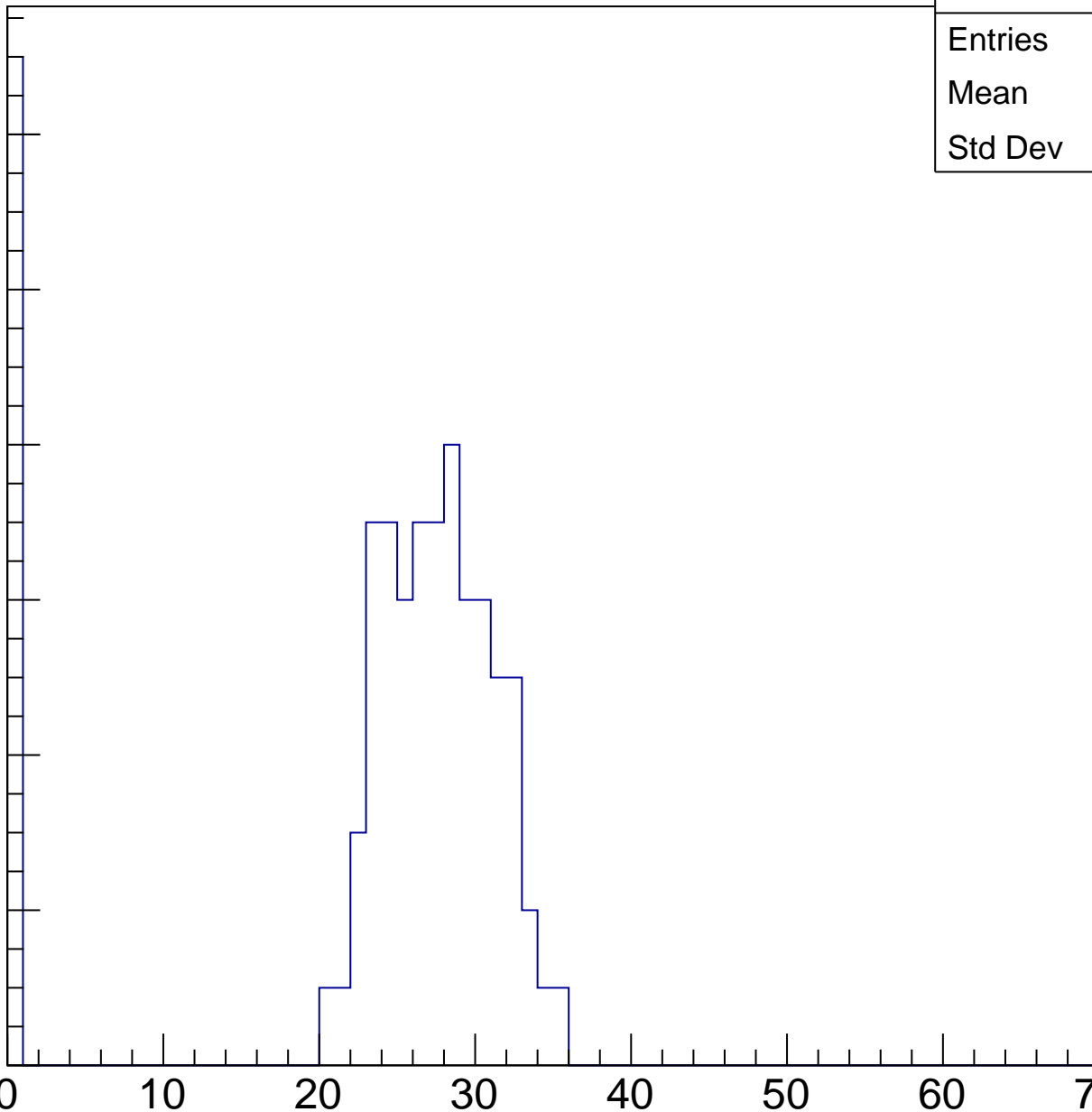
40

50

60

70

ampl

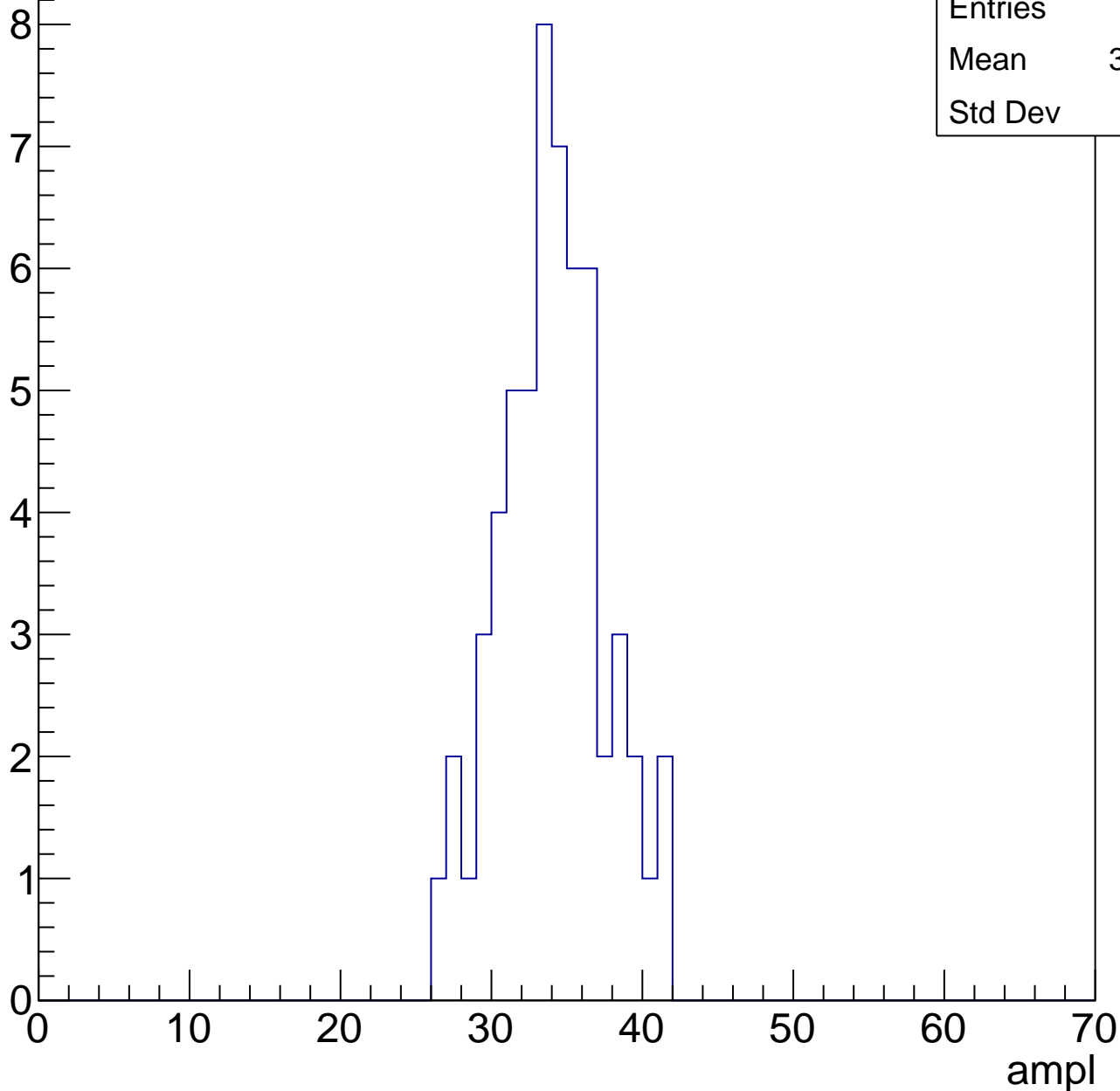


B1L103S, U5-ch76, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	33.55
Std Dev	3.42



B1L103S, U5-ch76, adc2

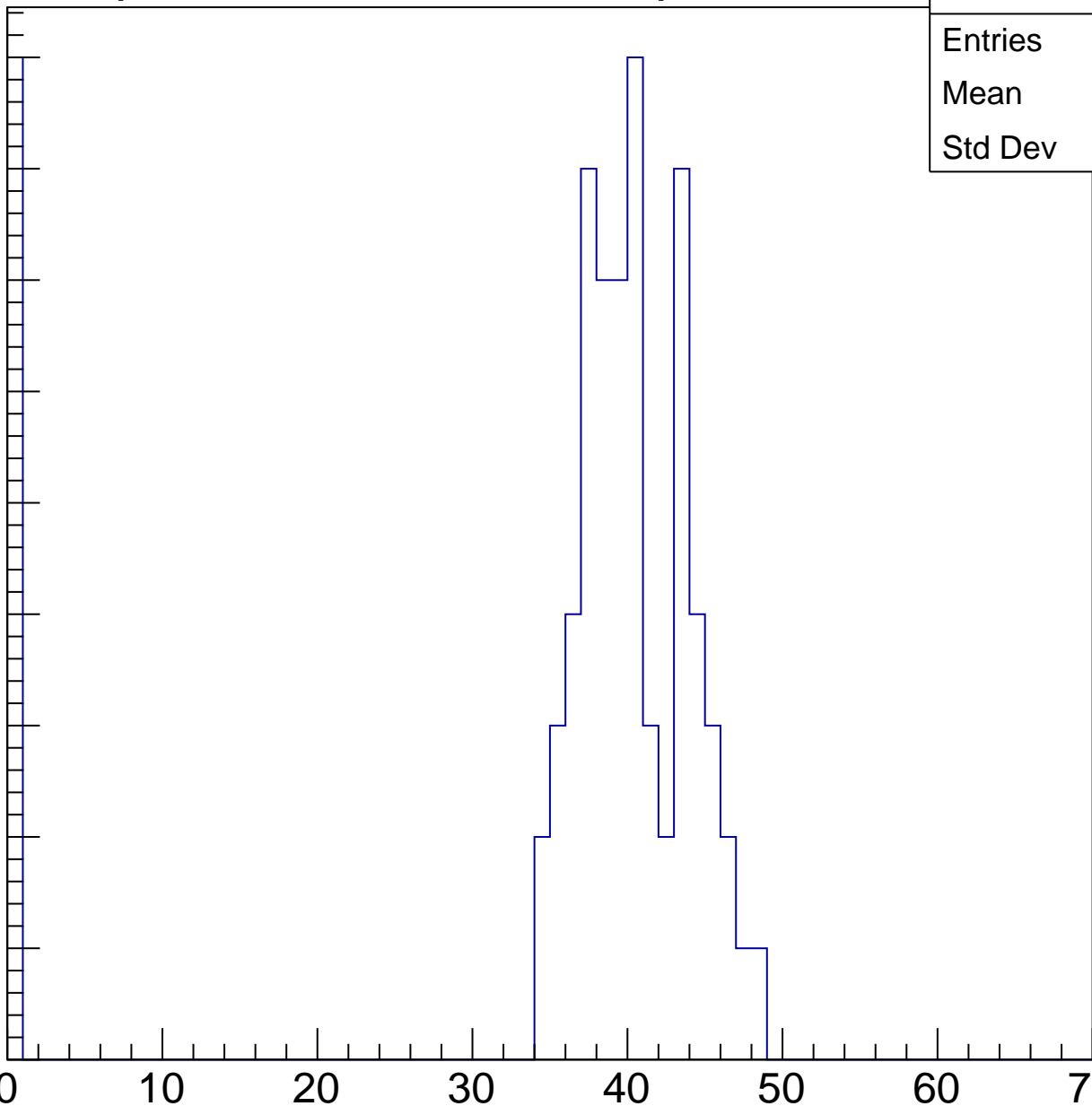
calib_packv5_041523_1651.root, FC#0, port C2

Entry

9
8
7
6
5
4
3
2
1
0

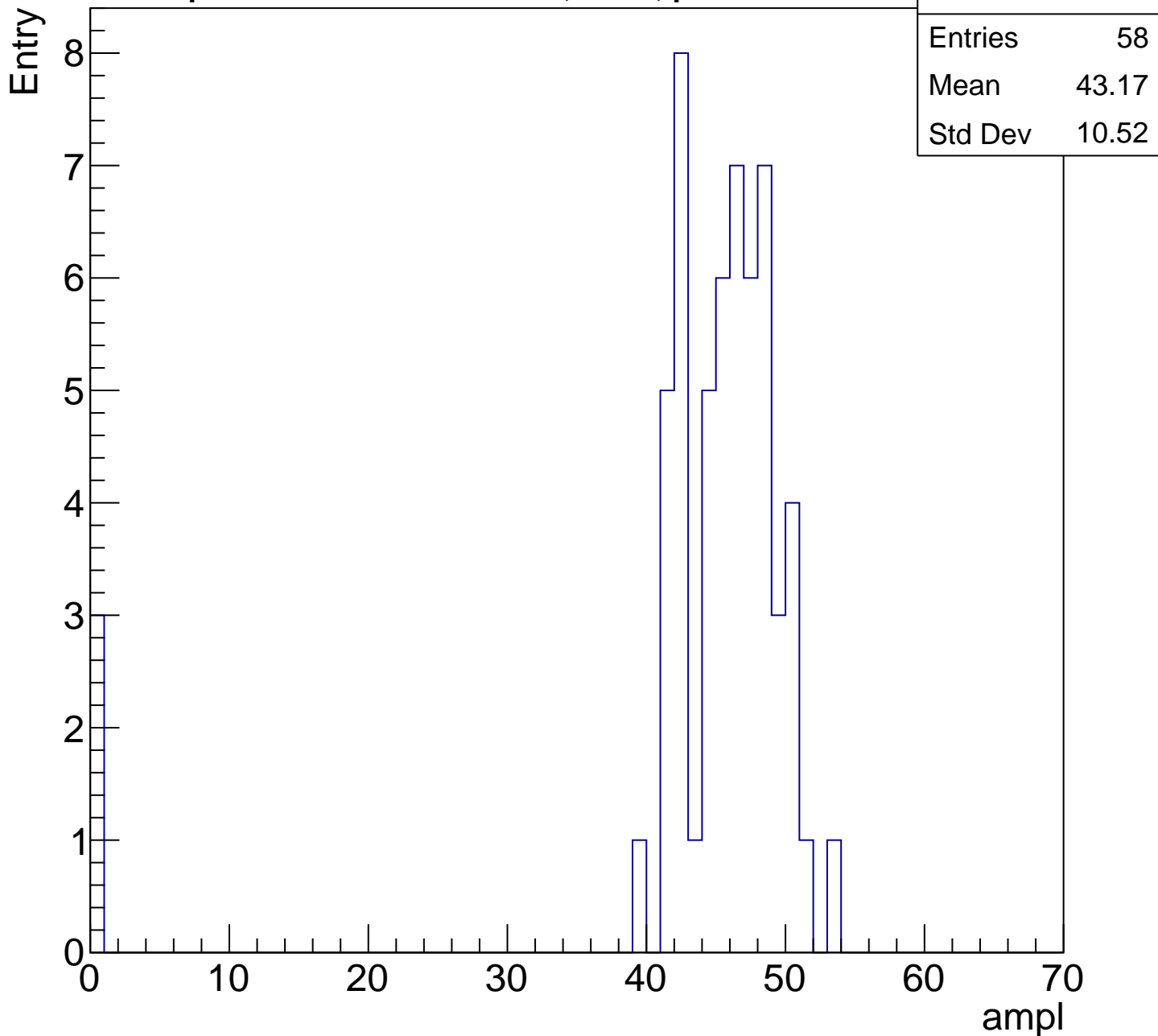
Entries	73
Mean	35.08
Std Dev	13.53

ampl



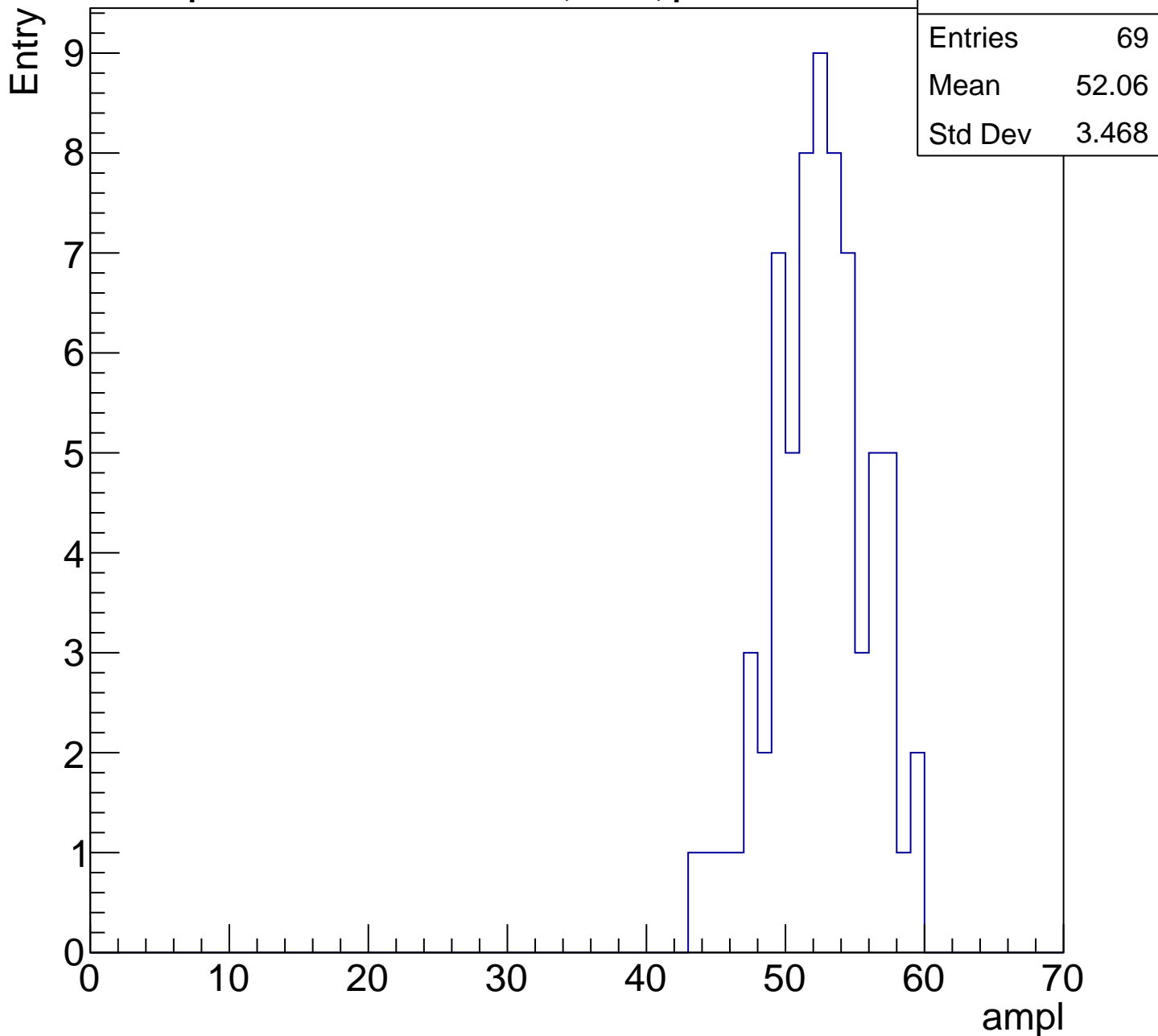
B1L103S, U5-ch76, adc3

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U5-ch76, adc4

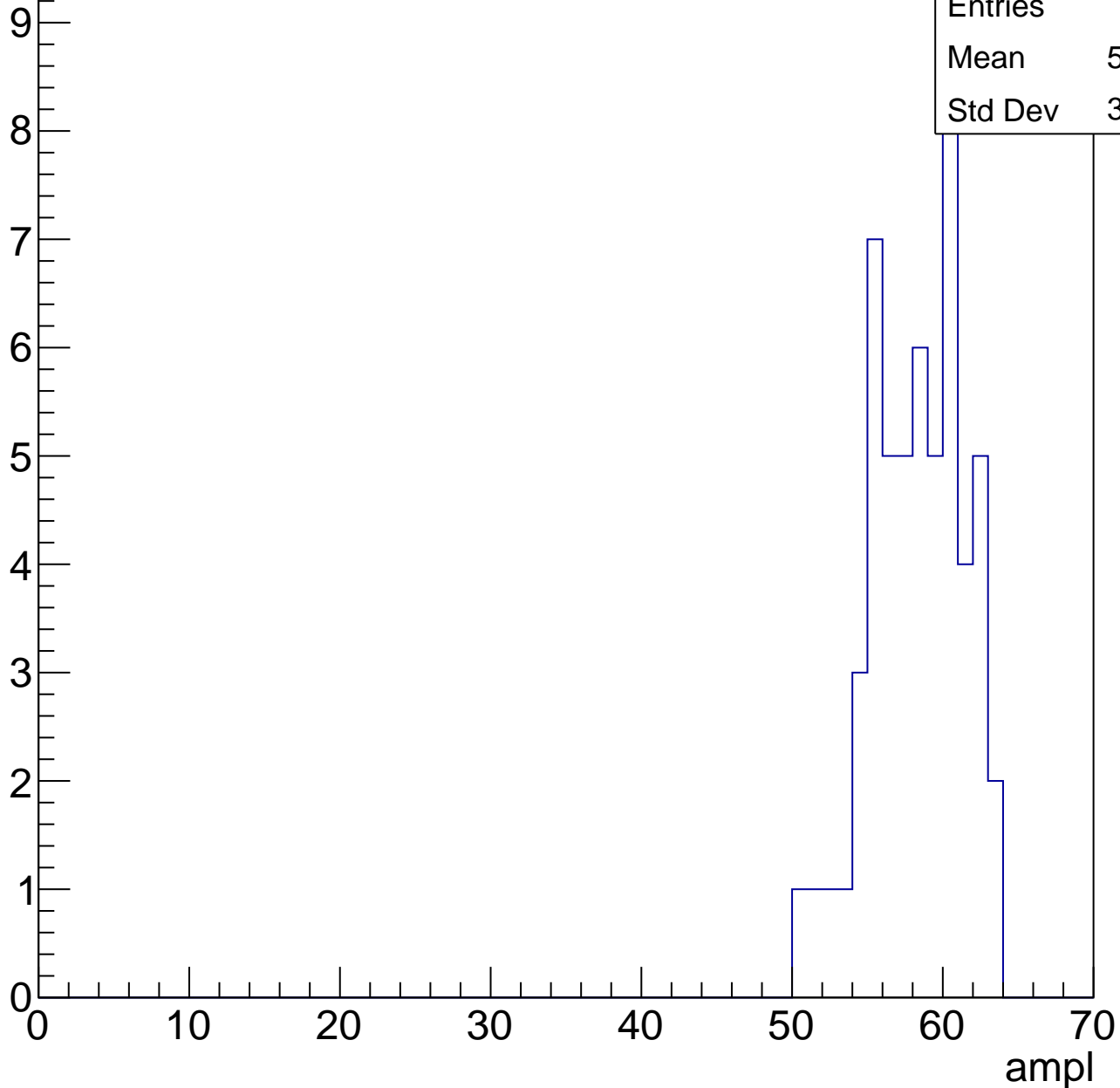
calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U5-ch76, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



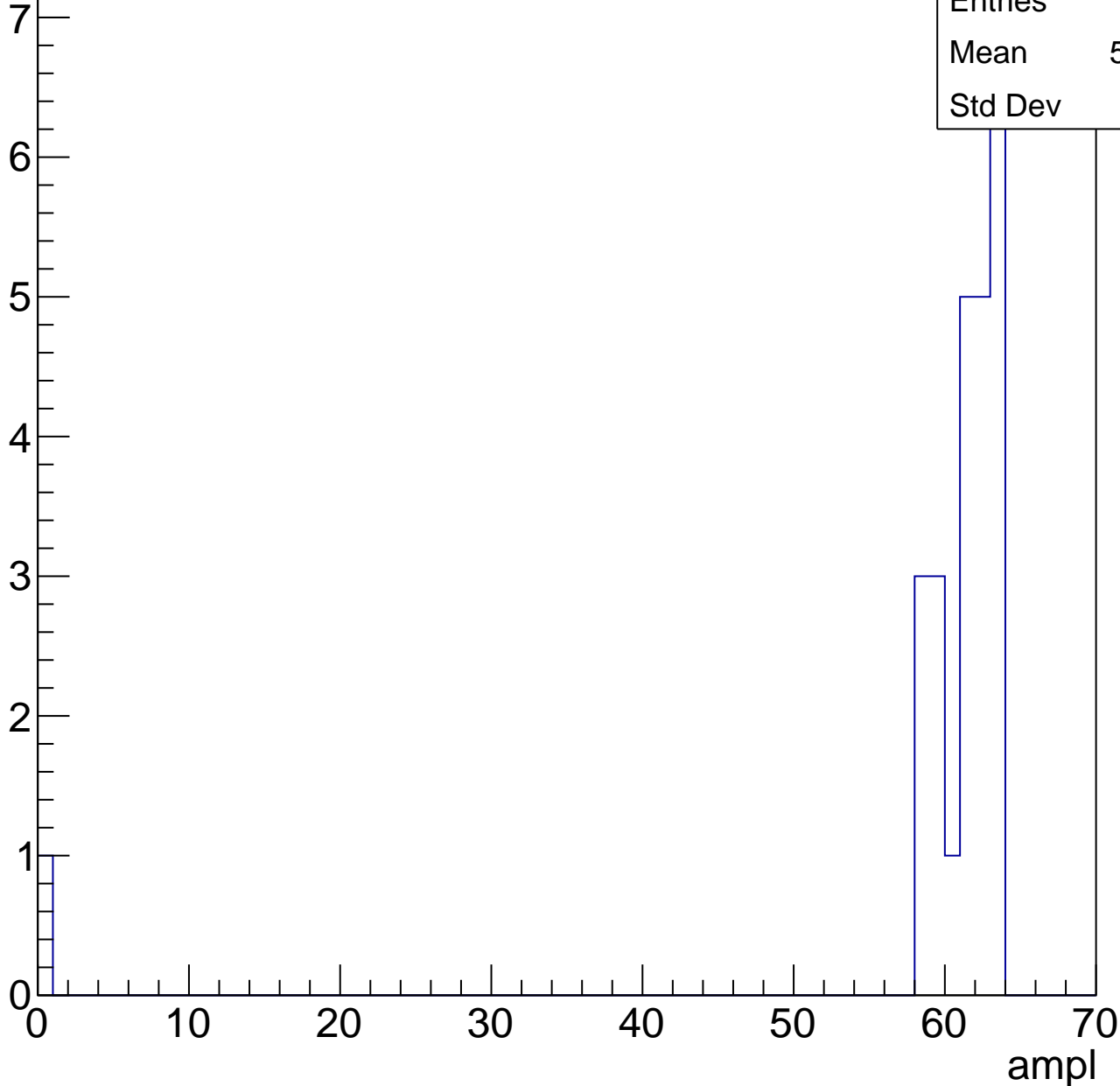
Entries	55
Mean	57.84
Std Dev	3.062

B1L103S, U5-ch76, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	25
Mean	58.68
Std Dev	12.1

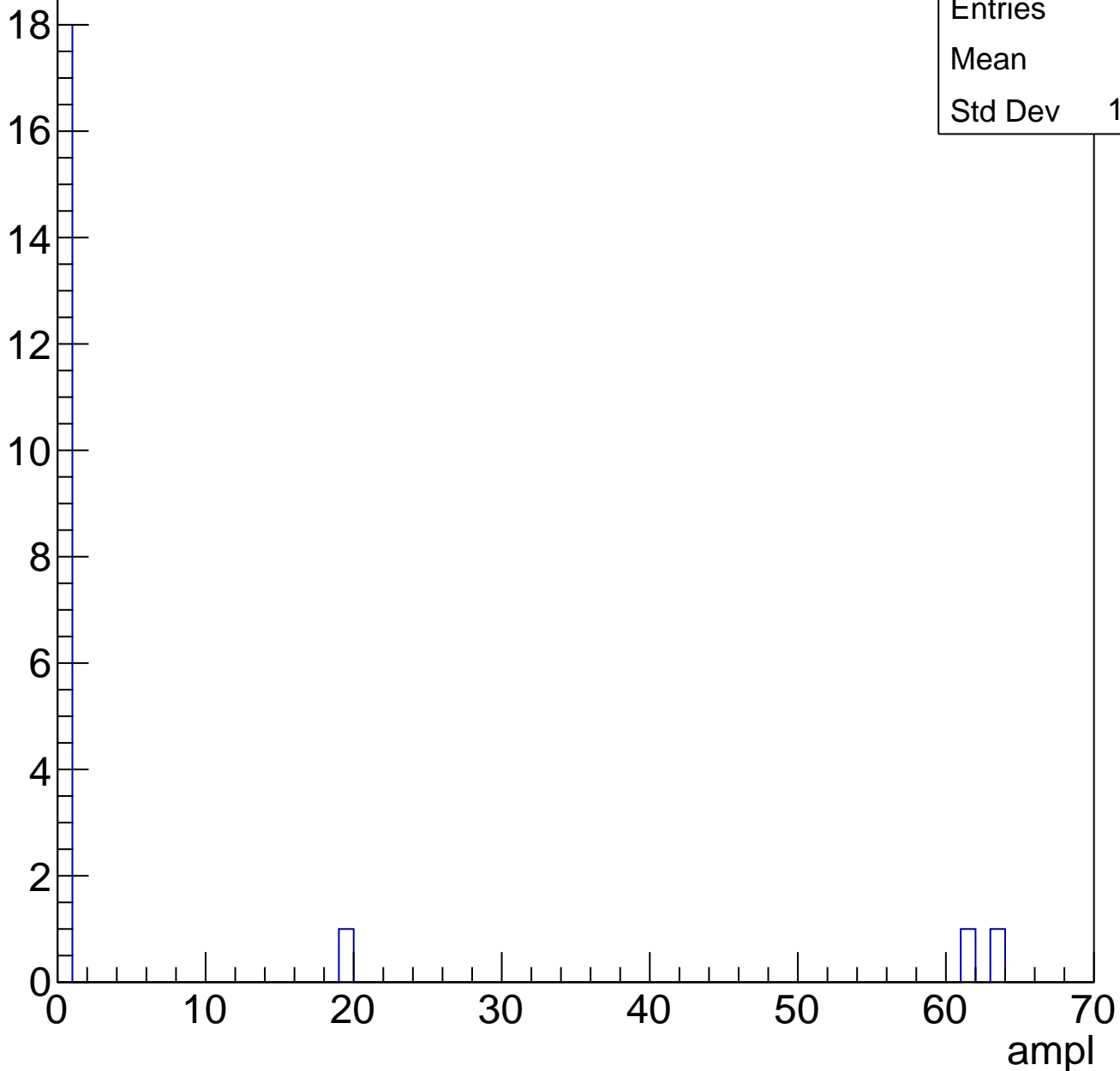


B1L103S, U5-ch76, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	6.81
Std Dev	18.36

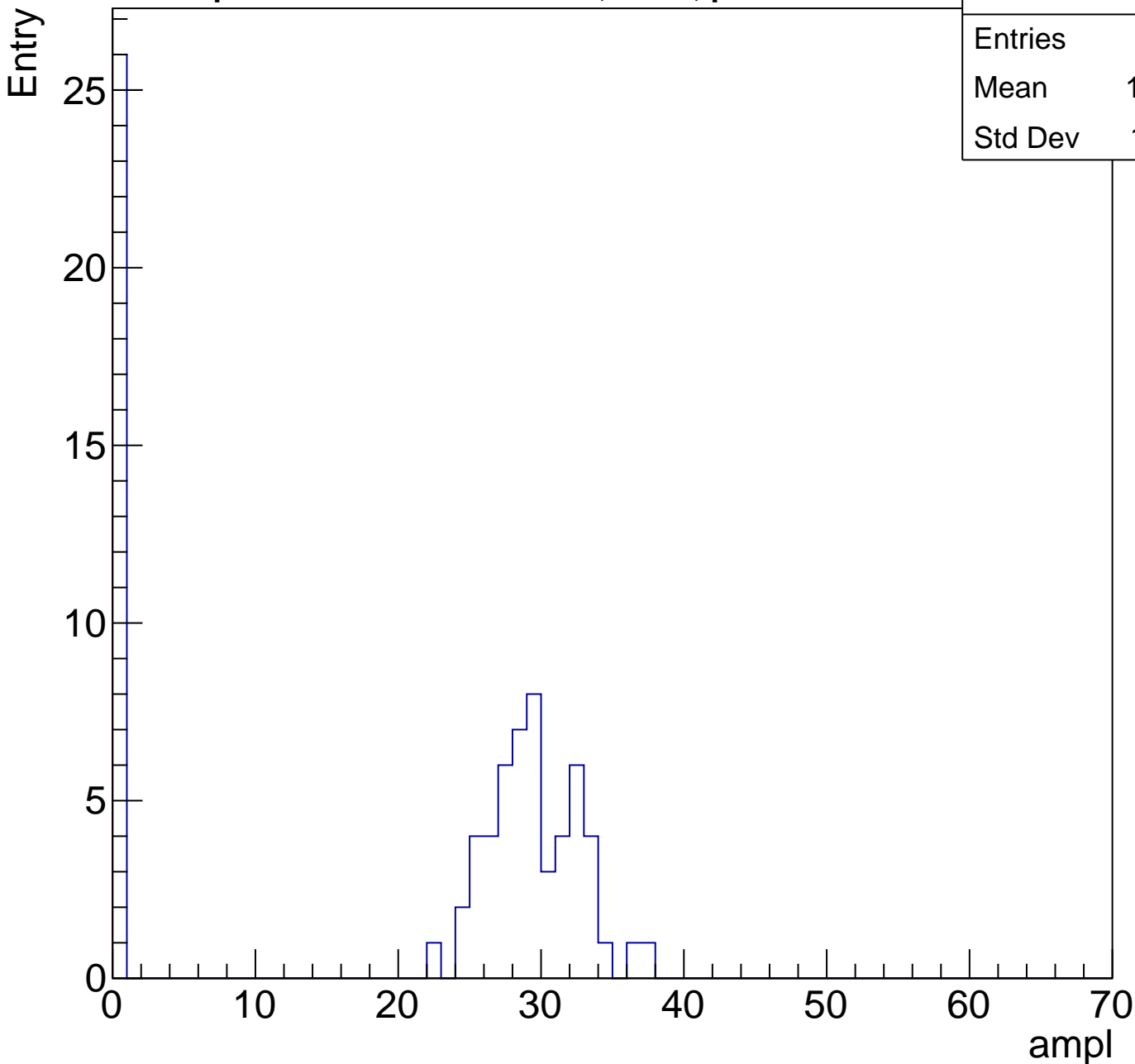
Entry



B1L103S, U5-ch77, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	78
Mean	19.35
Std Dev	13.91

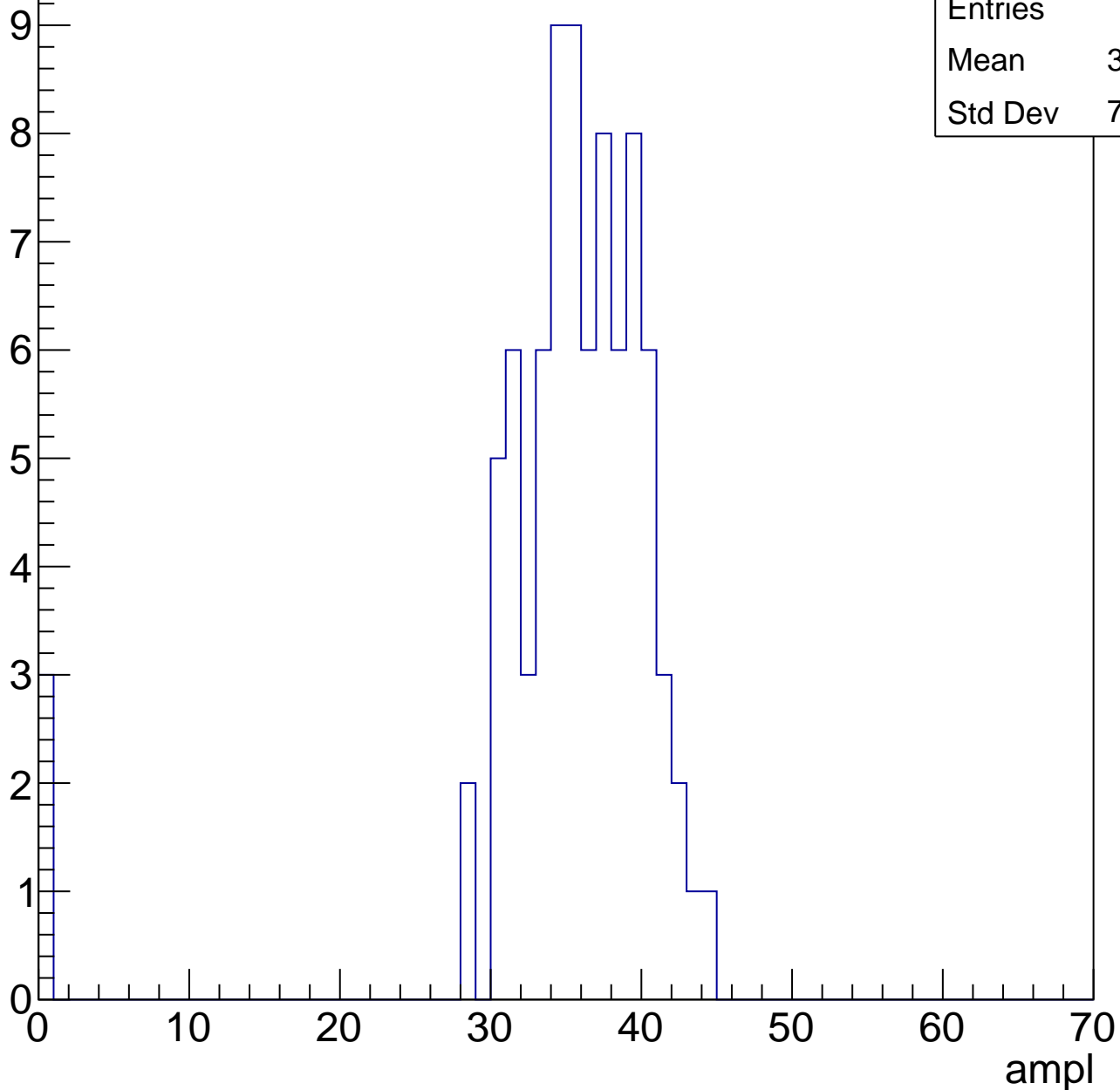


B1L103S, U5-ch77, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	84
Mean	34.44
Std Dev	7.519



B1L103S, U5-ch77, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	63
Mean	34.97
Std Dev	16.39

Entry

10

8

6

4

2

0

0

10

20

30

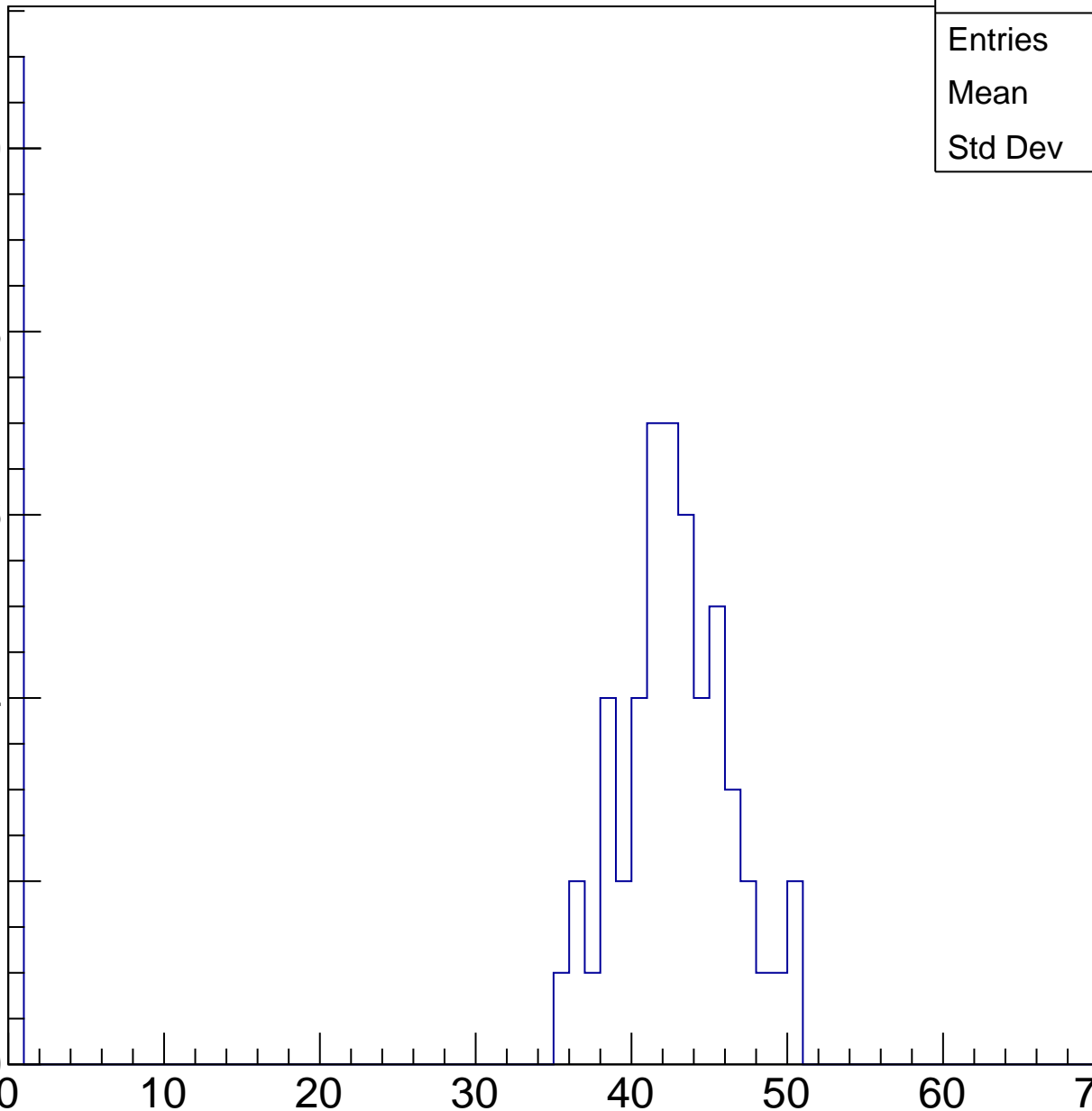
40

50

60

70

ampl

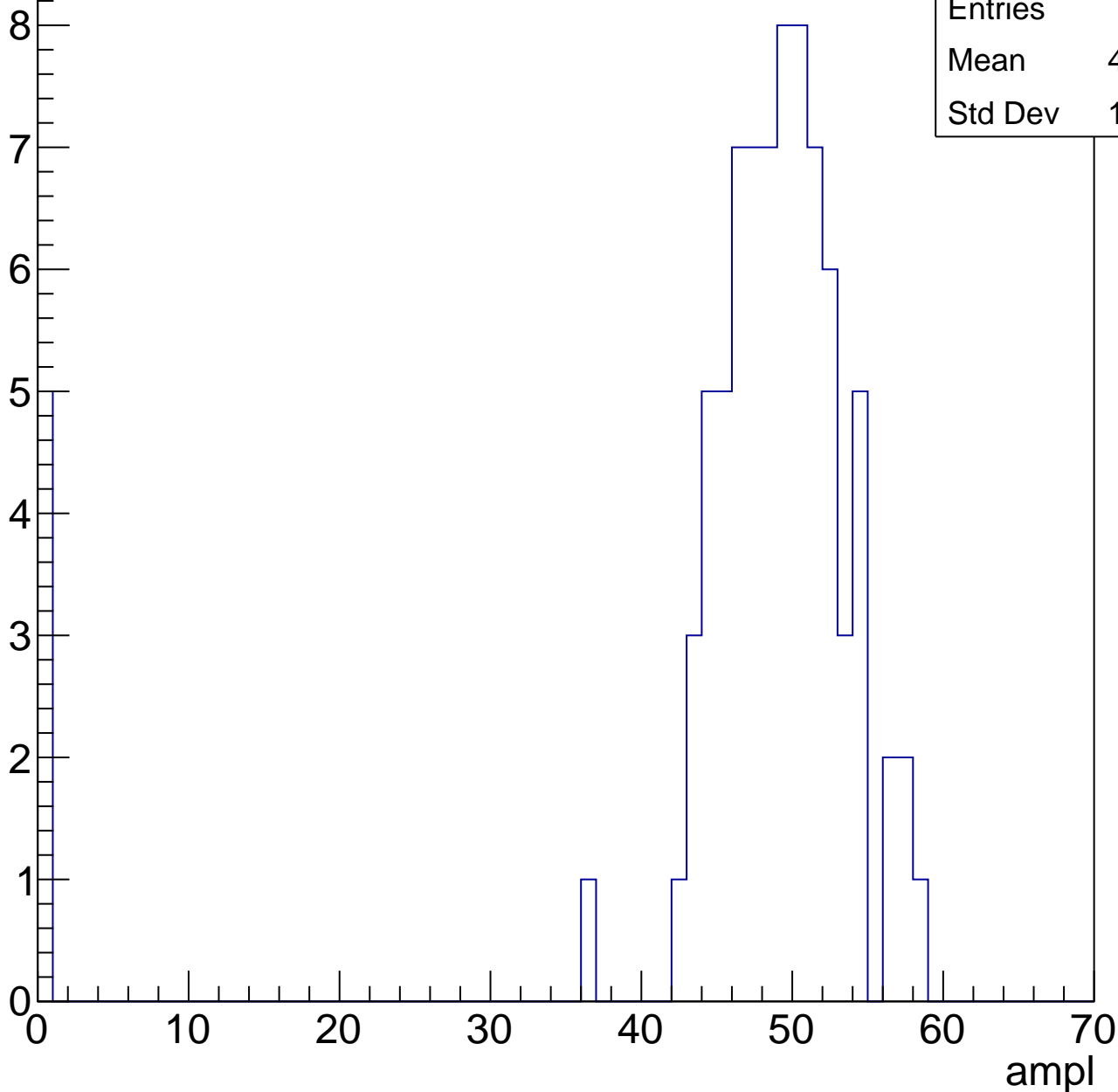


B1L103S, U5-ch77, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	83
Mean	45.94
Std Dev	12.24

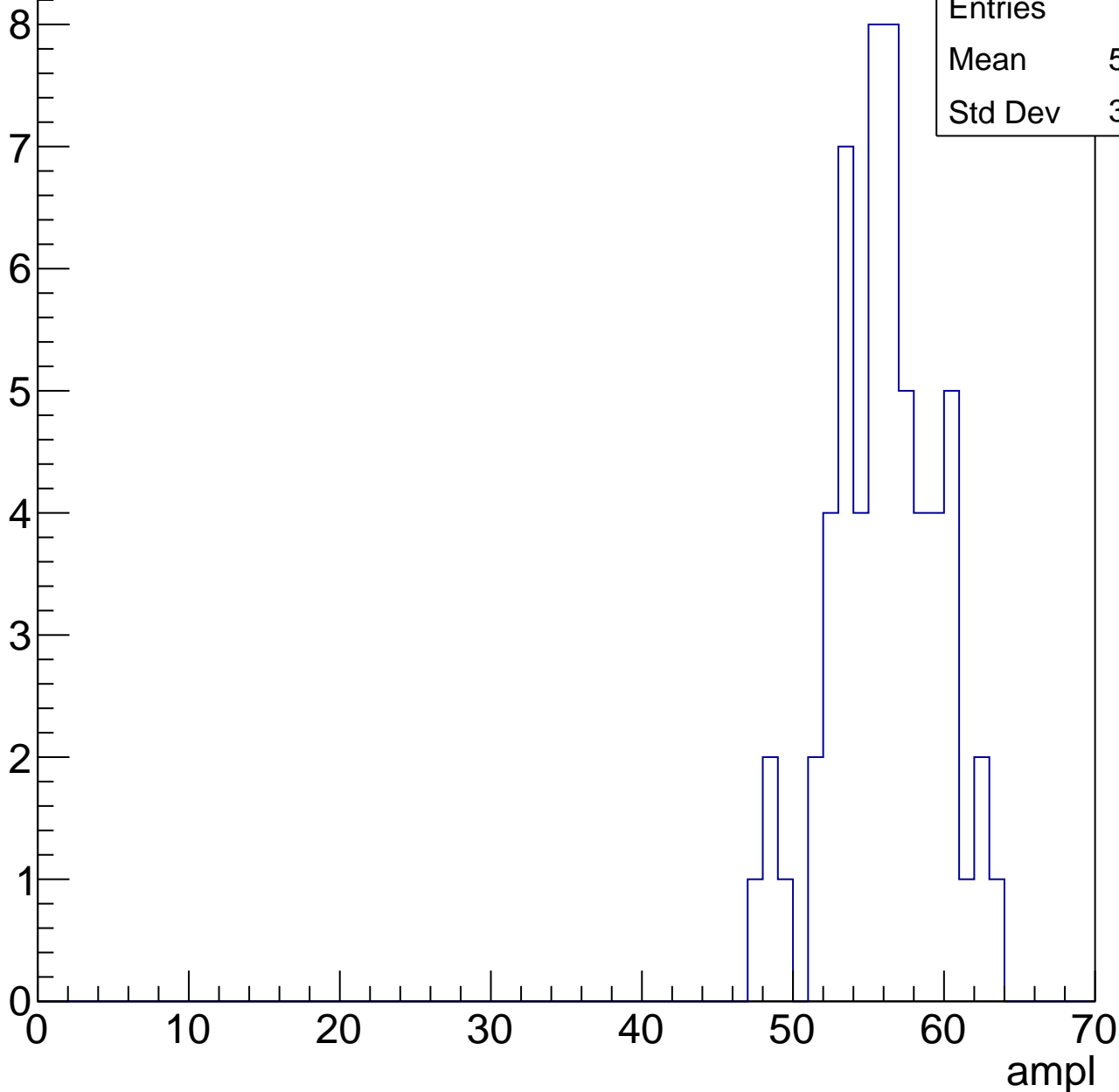


B1L103S, U5-ch77, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

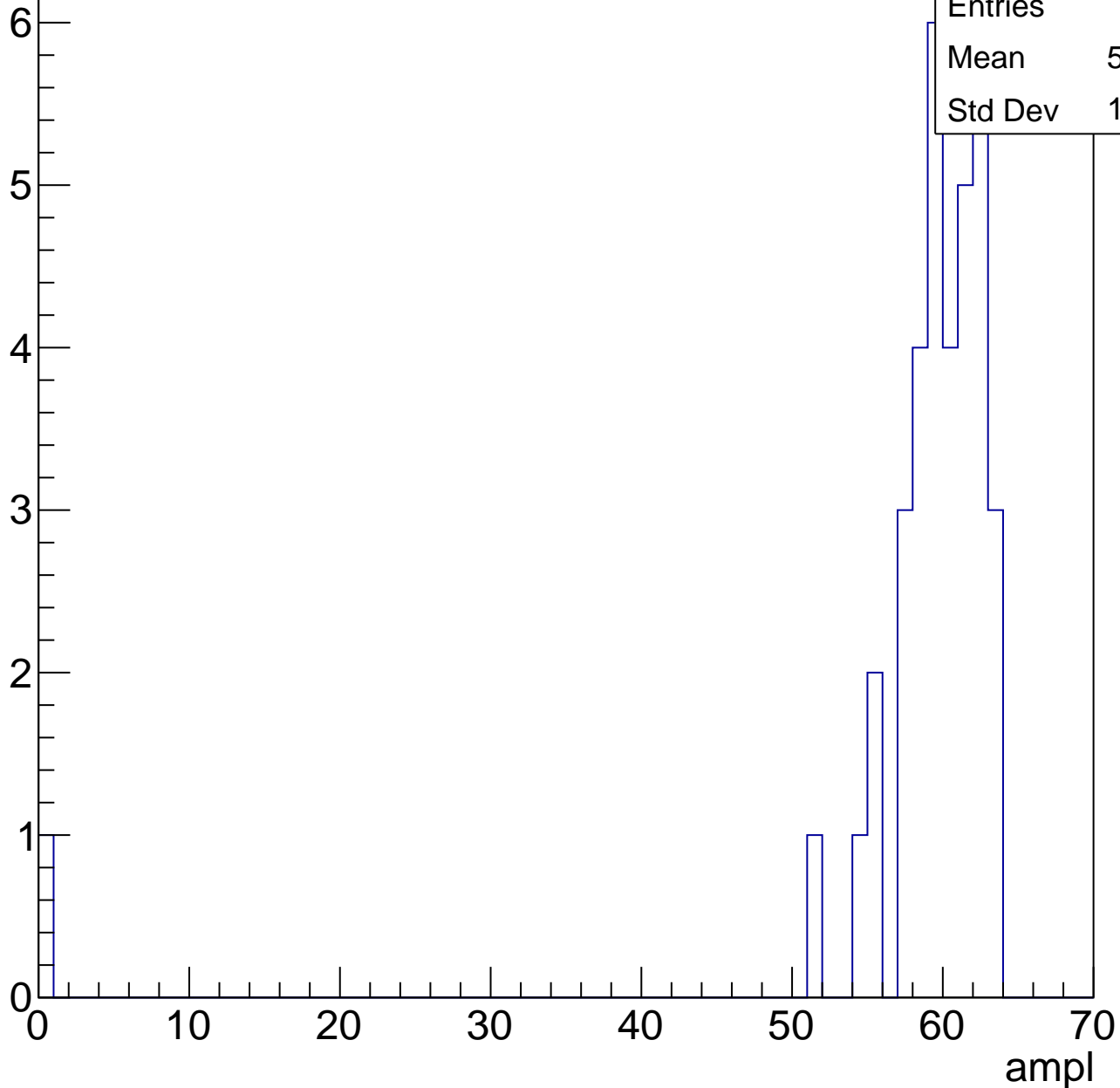
Entries	59
Mean	55.56
Std Dev	3.519



B1L103S, U5-ch77, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

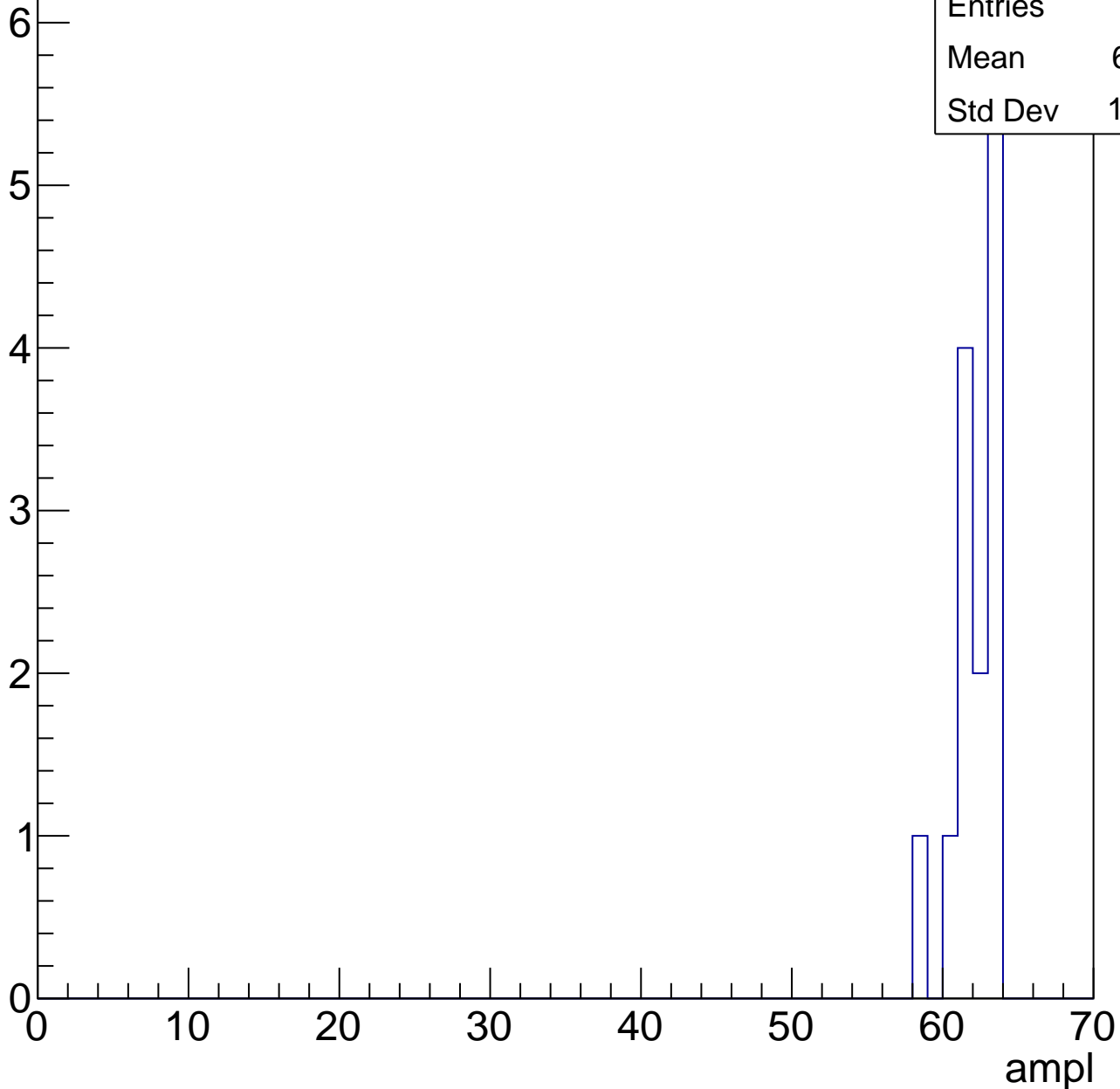


B1L103S, U5-ch77, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	14
Mean	61.71
Std Dev	1.436



B1L103S, U5-ch77, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U5-ch78, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	92
Mean	23.05
Std Dev	10.01

Entry

12

10

8

6

4

2

0

0

10

20

30

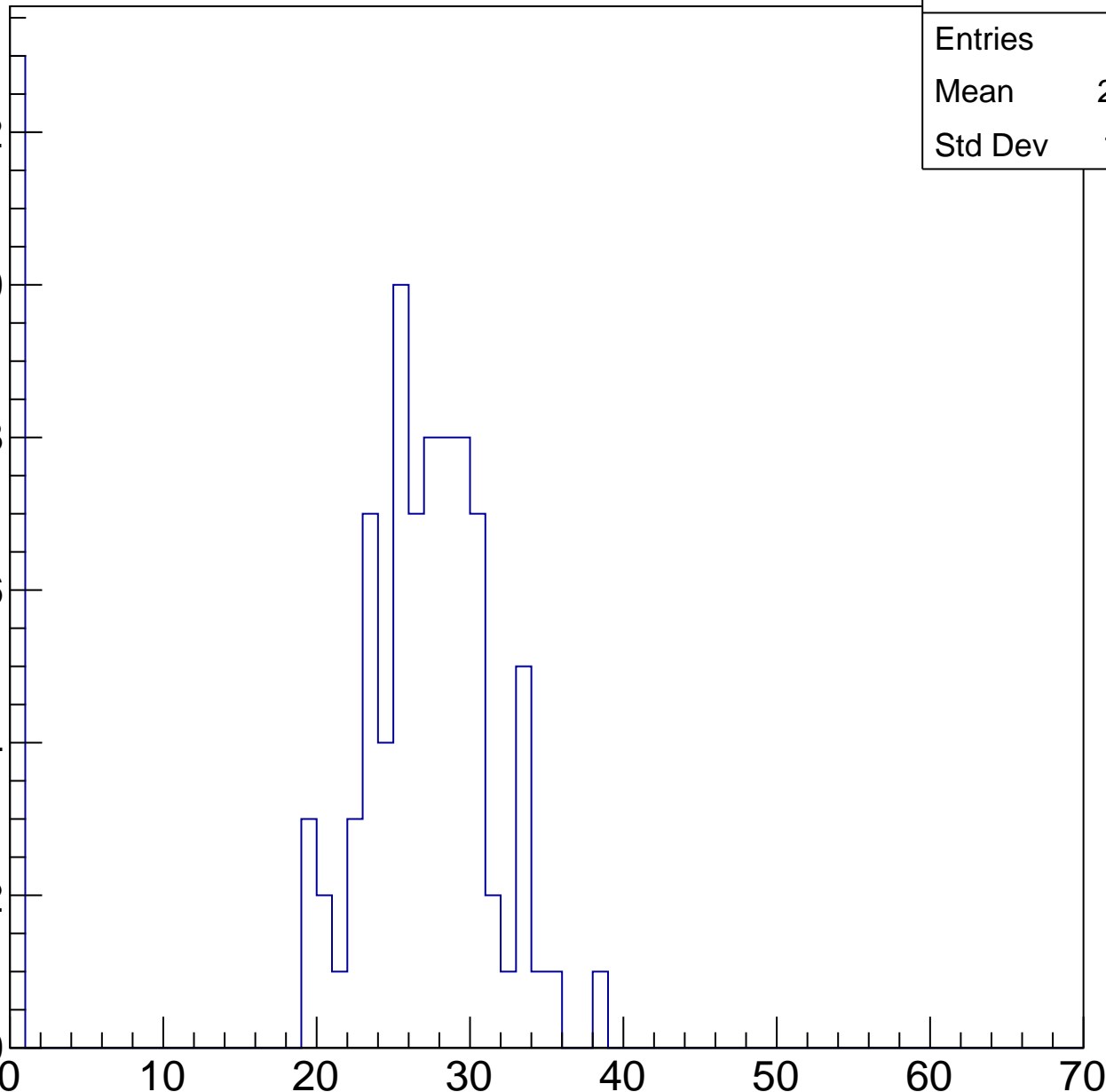
40

50

60

70

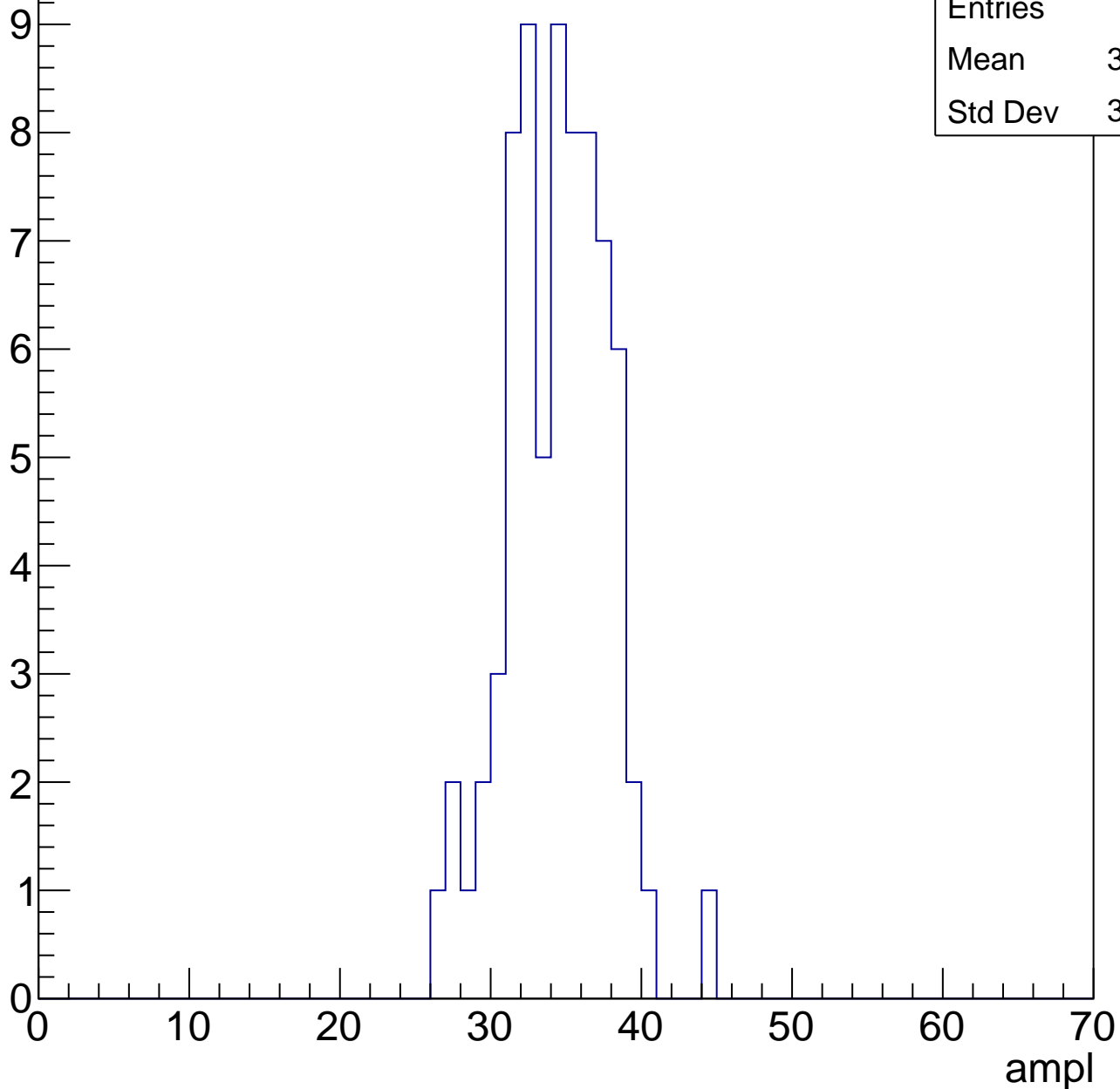
ampl



B1L103S, U5-ch78, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry



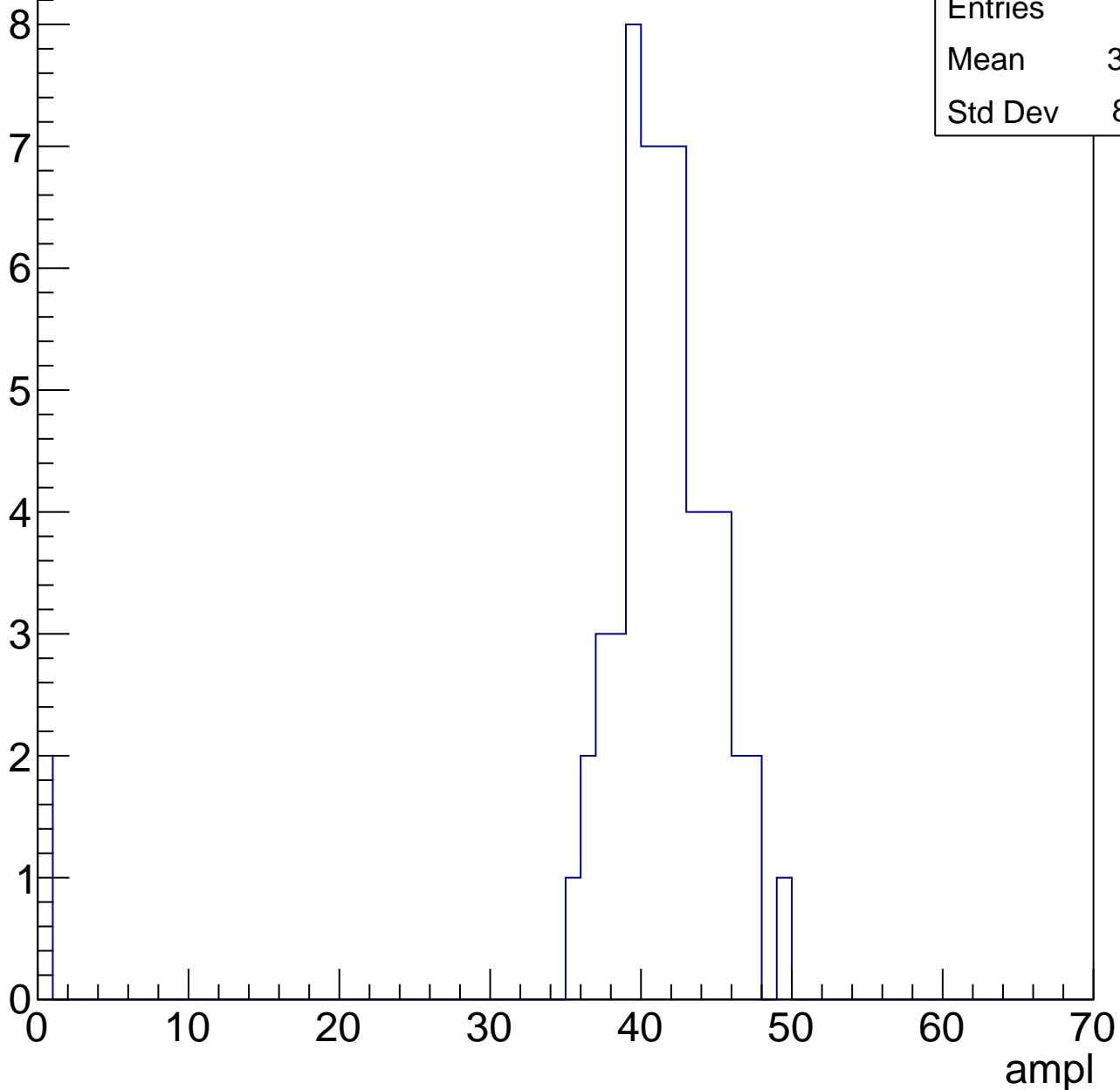
Entries	73
Mean	33.97
Std Dev	3.298

B1L103S, U5-ch78, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	39.79
Std Dev	8.151

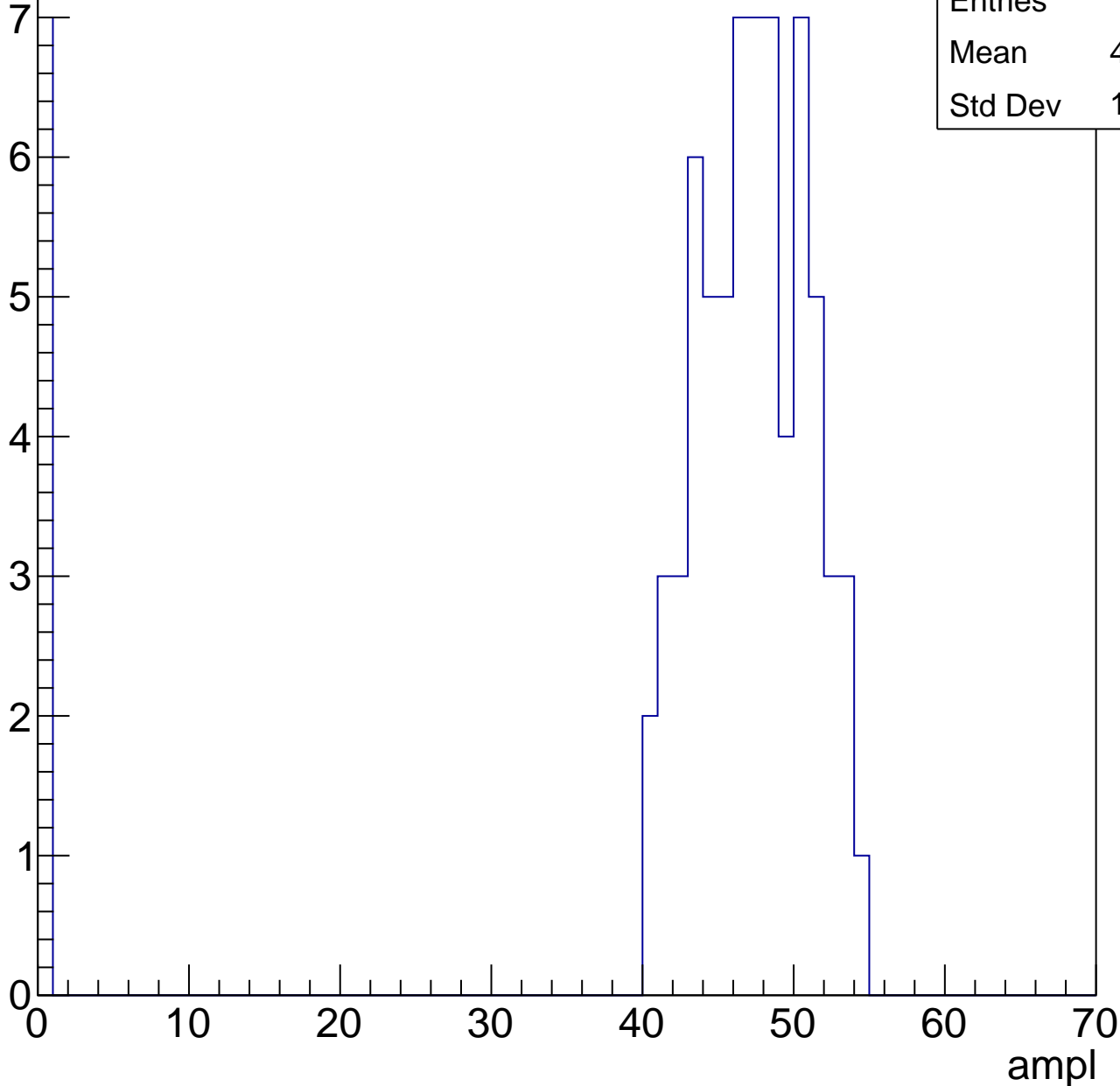


B1L103S, U5-ch78, adc3

calib_packv5_041523_1651.root, FC#0, port C2

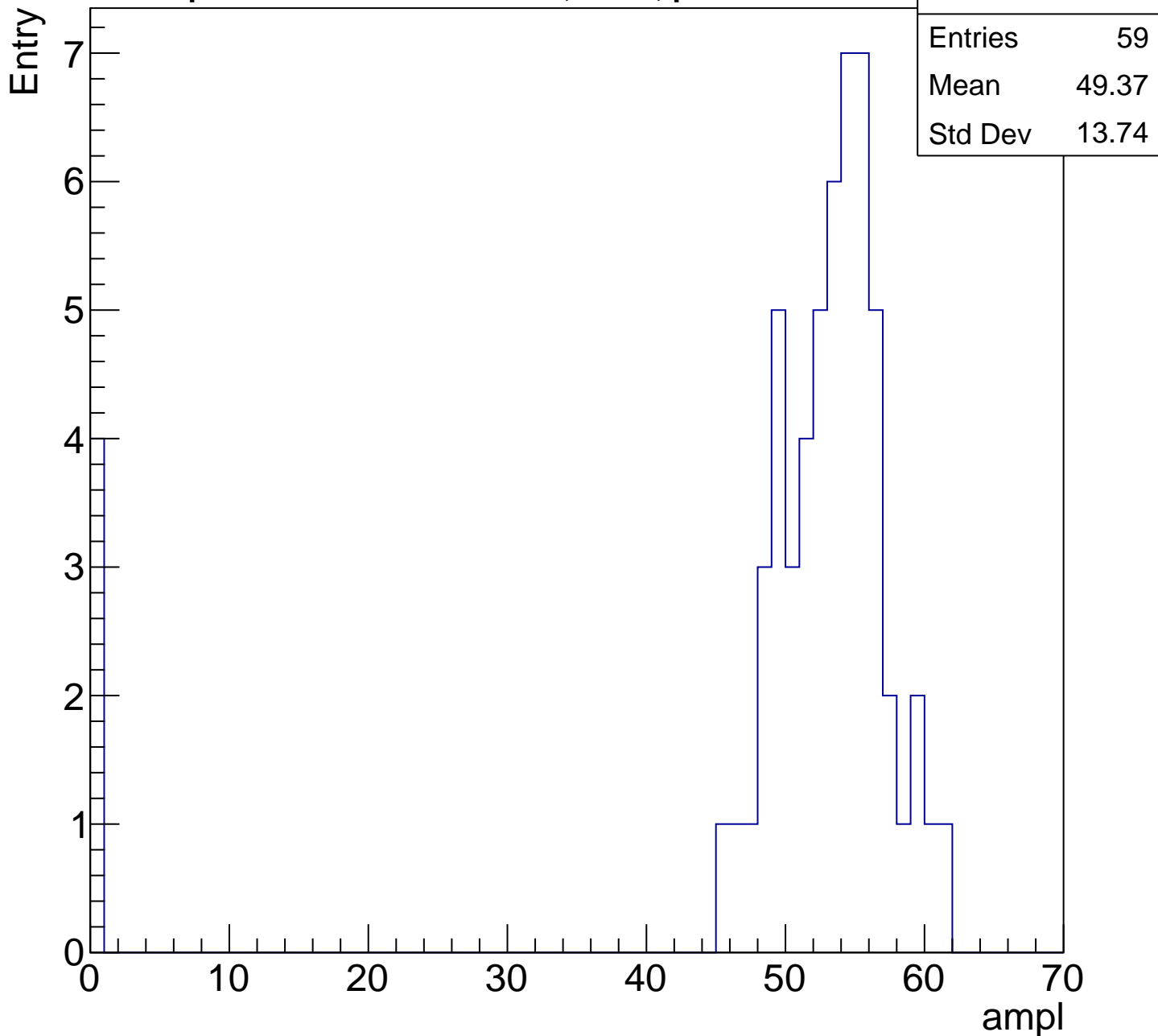
Entry

Entries	75
Mean	42.52
Std Dev	14.05



B1L103S, U5-ch78, adc4

calib_packv5_041523_1651.root, FC#0, port C2

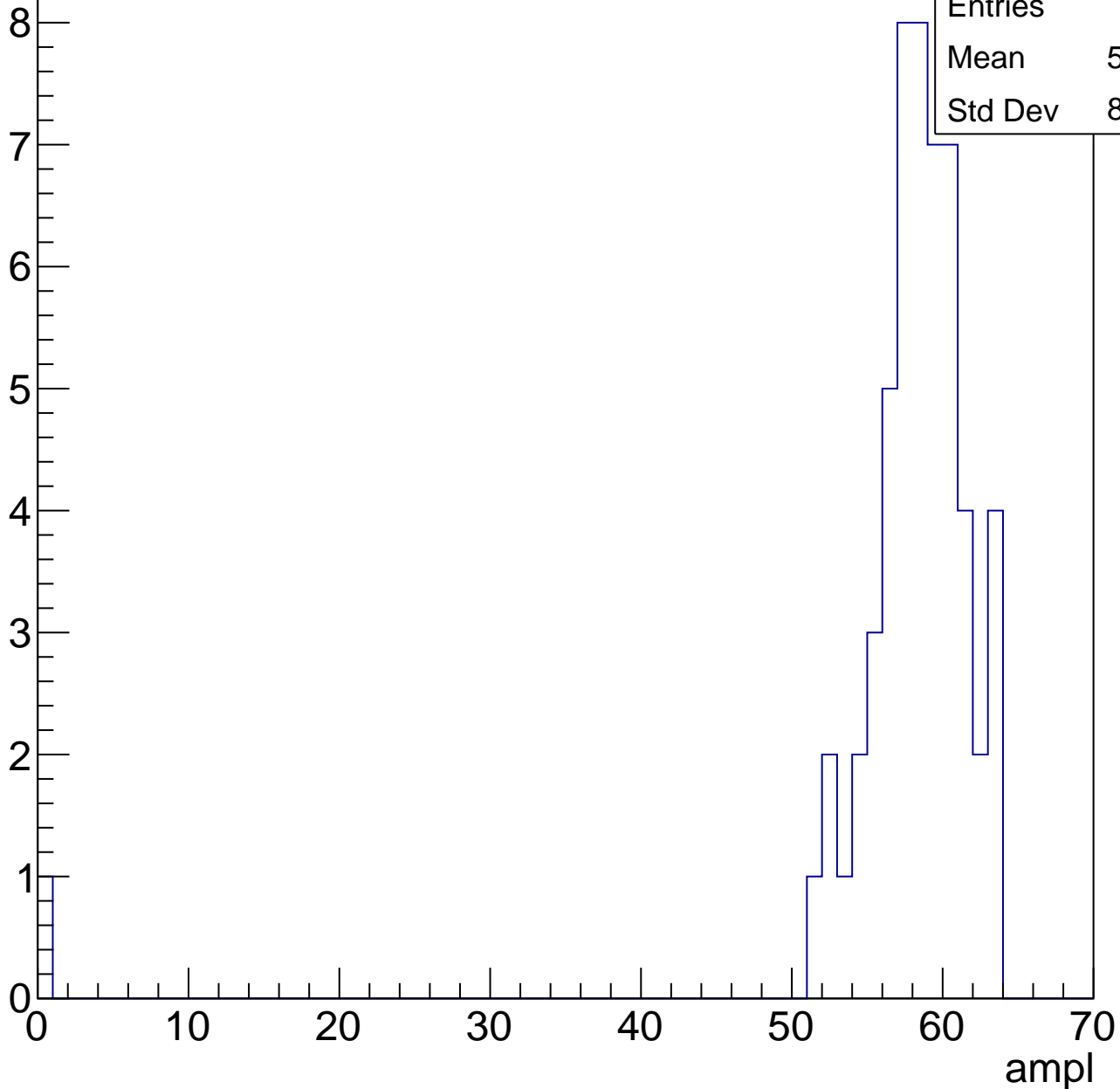


B1L103S, U5-ch78, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	56.98
Std Dev	8.249

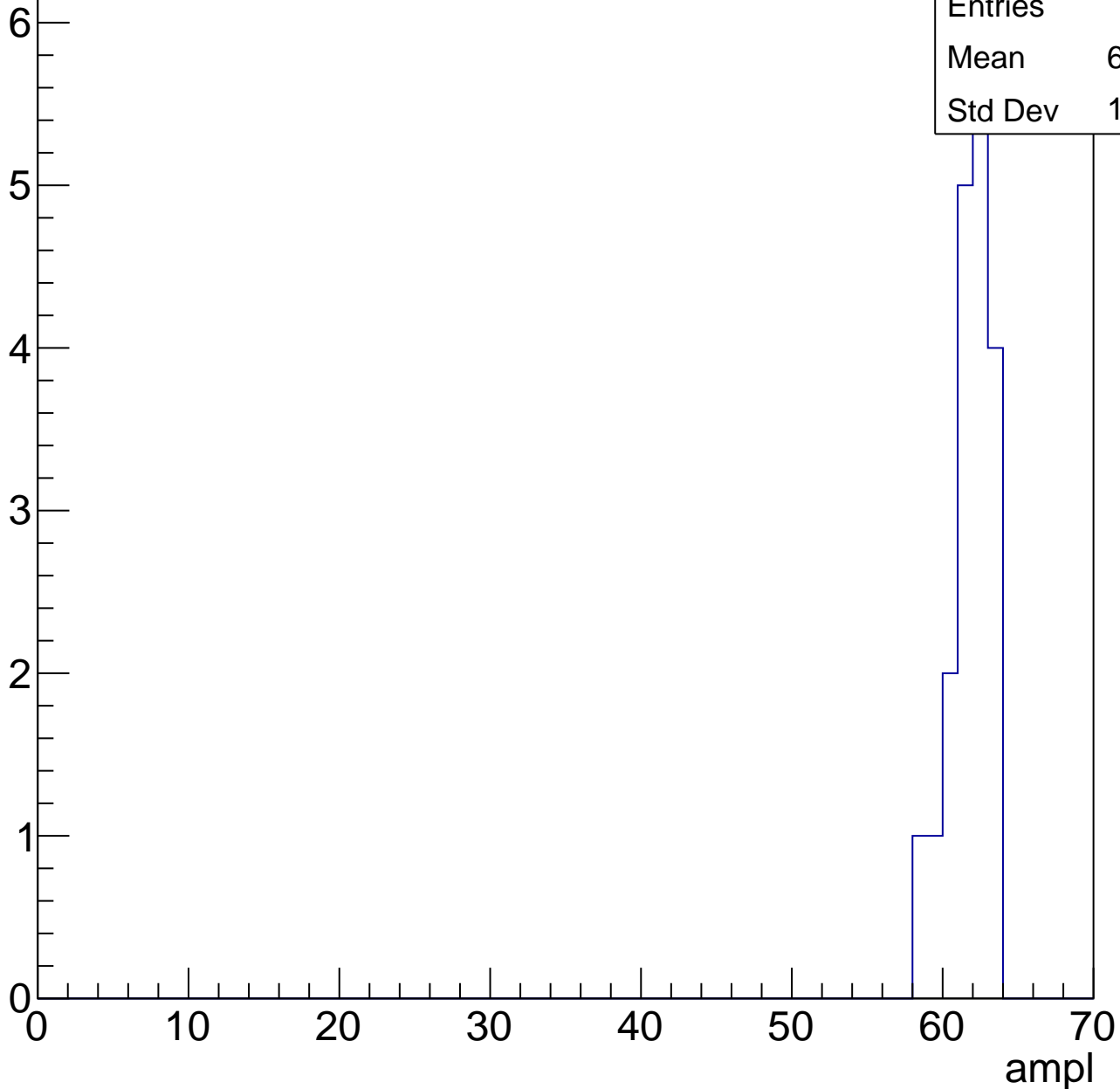


B1L103S, U5-ch78, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	19
Mean	61.37
Std Dev	1.346

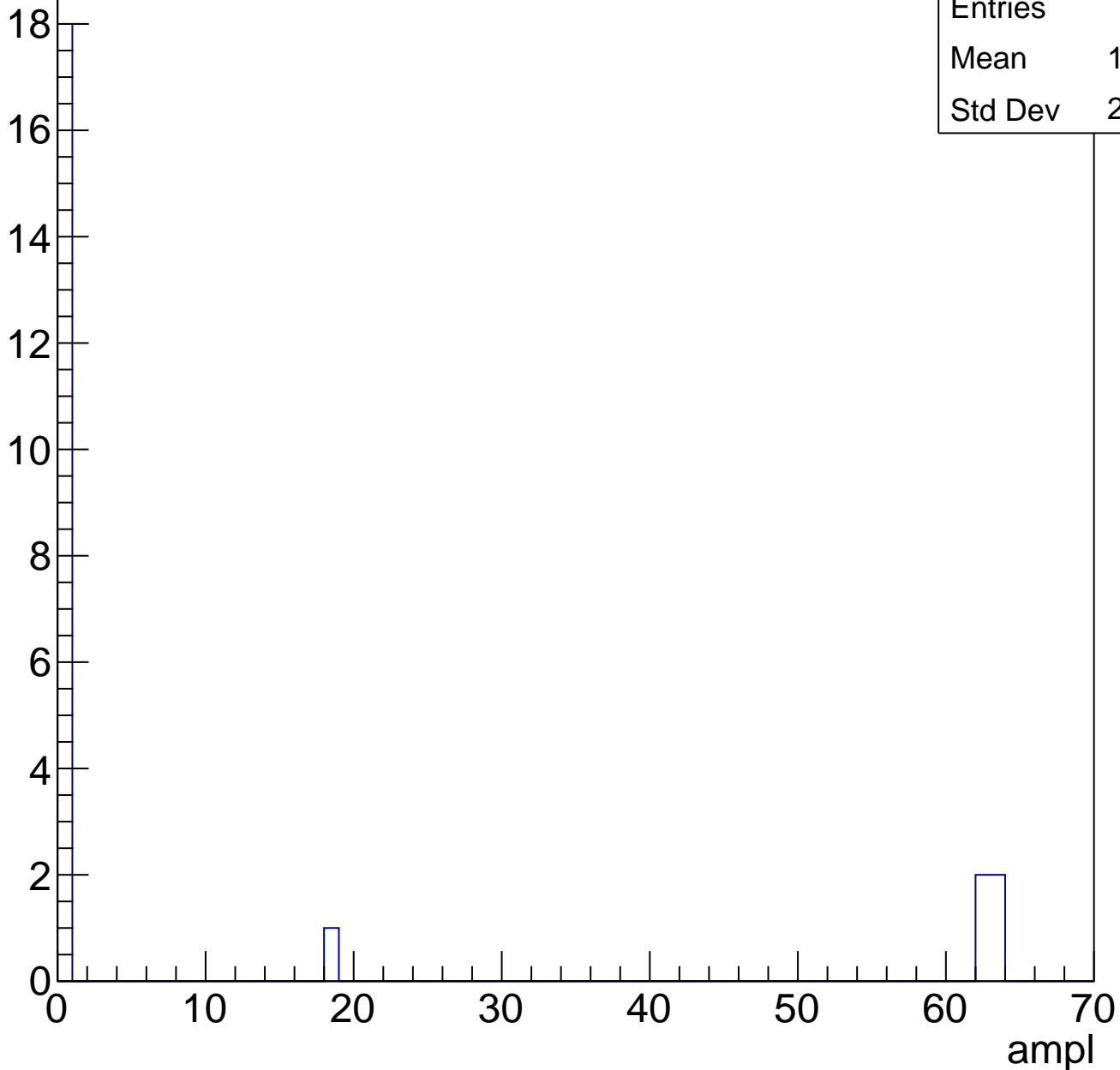


B1L103S, U5-ch78, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	23
Mean	11.65
Std Dev	23.62

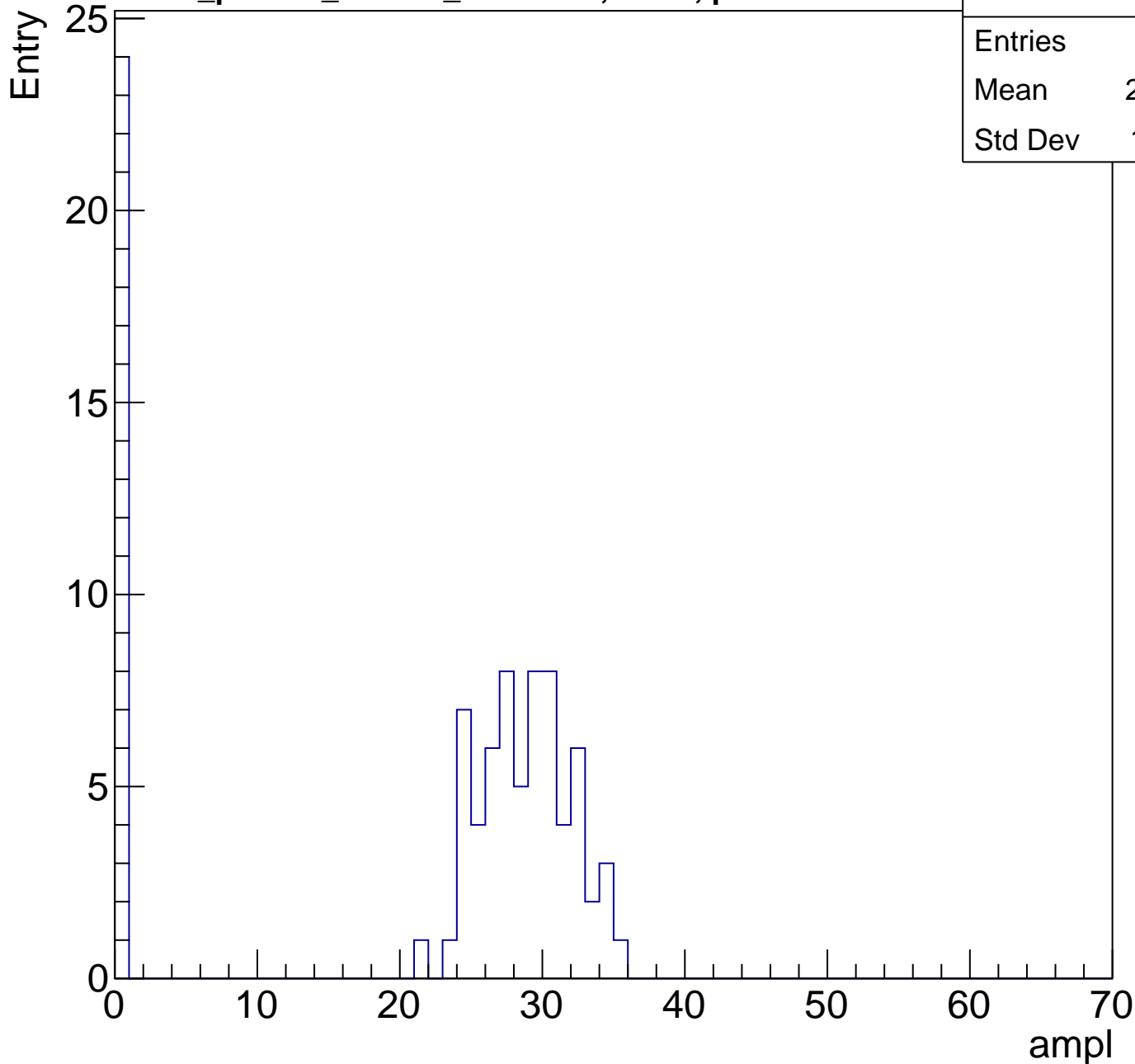
Entry



B1L103S, U5-ch79, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	88
Mean	20.62
Std Dev	12.91

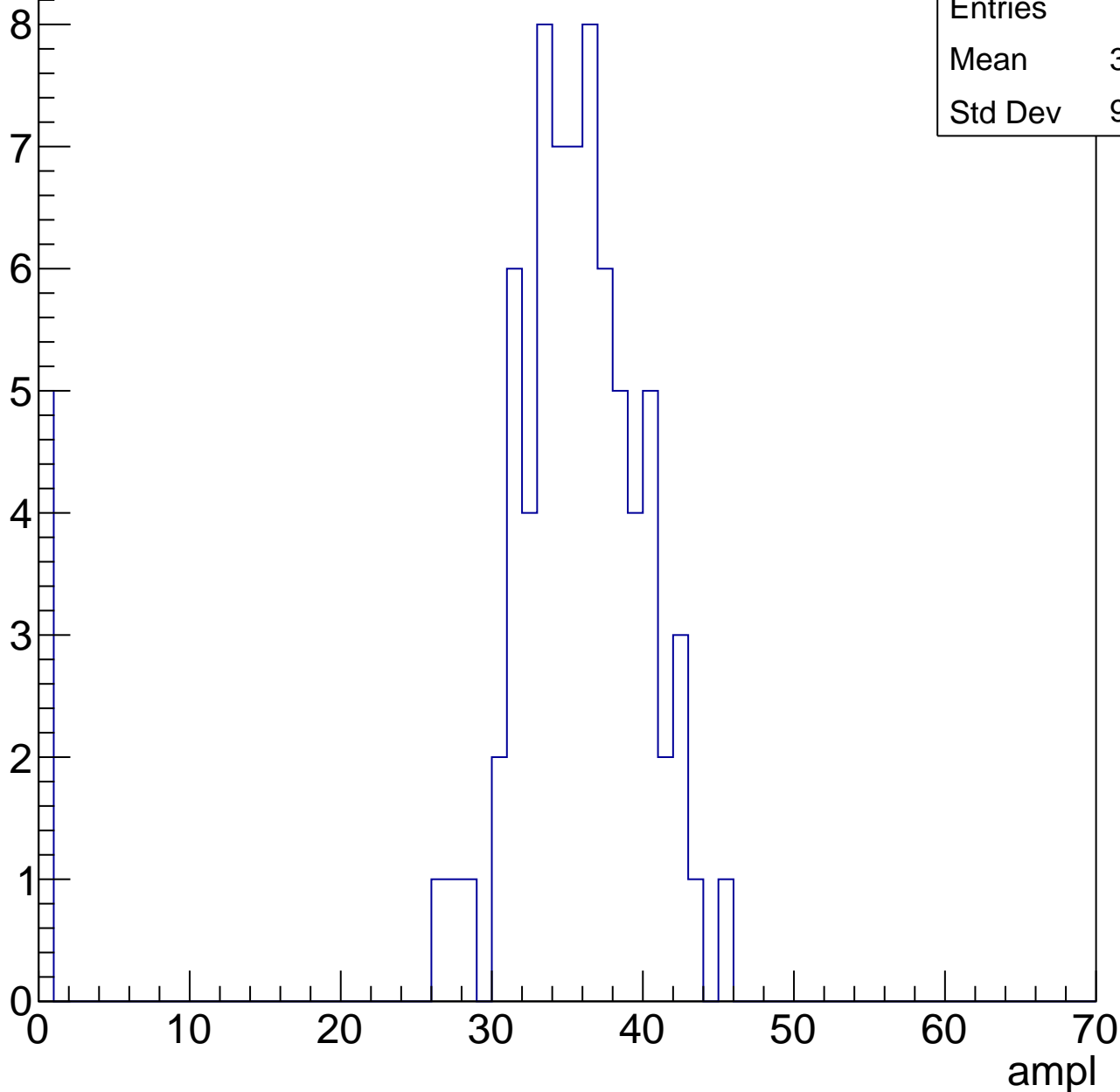


B1L103S, U5-ch79, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	33.17
Std Dev	9.487

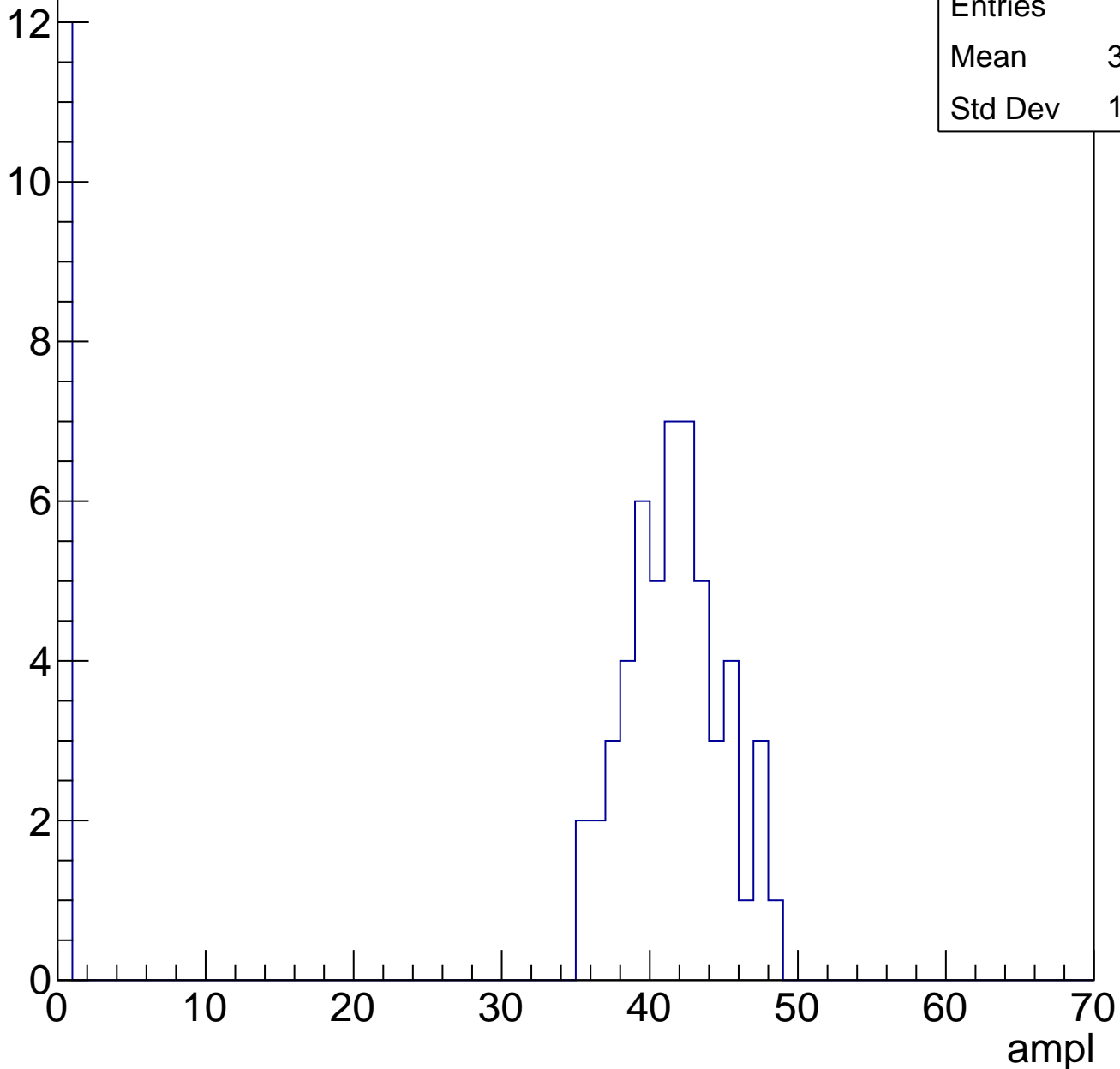


B1L103S, U5-ch79, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	65
Mean	33.57
Std Dev	16.23

Entry



B1L103S, U5-ch79, adc3

calib_packv5_041523_1651.root, FC#0, port C2

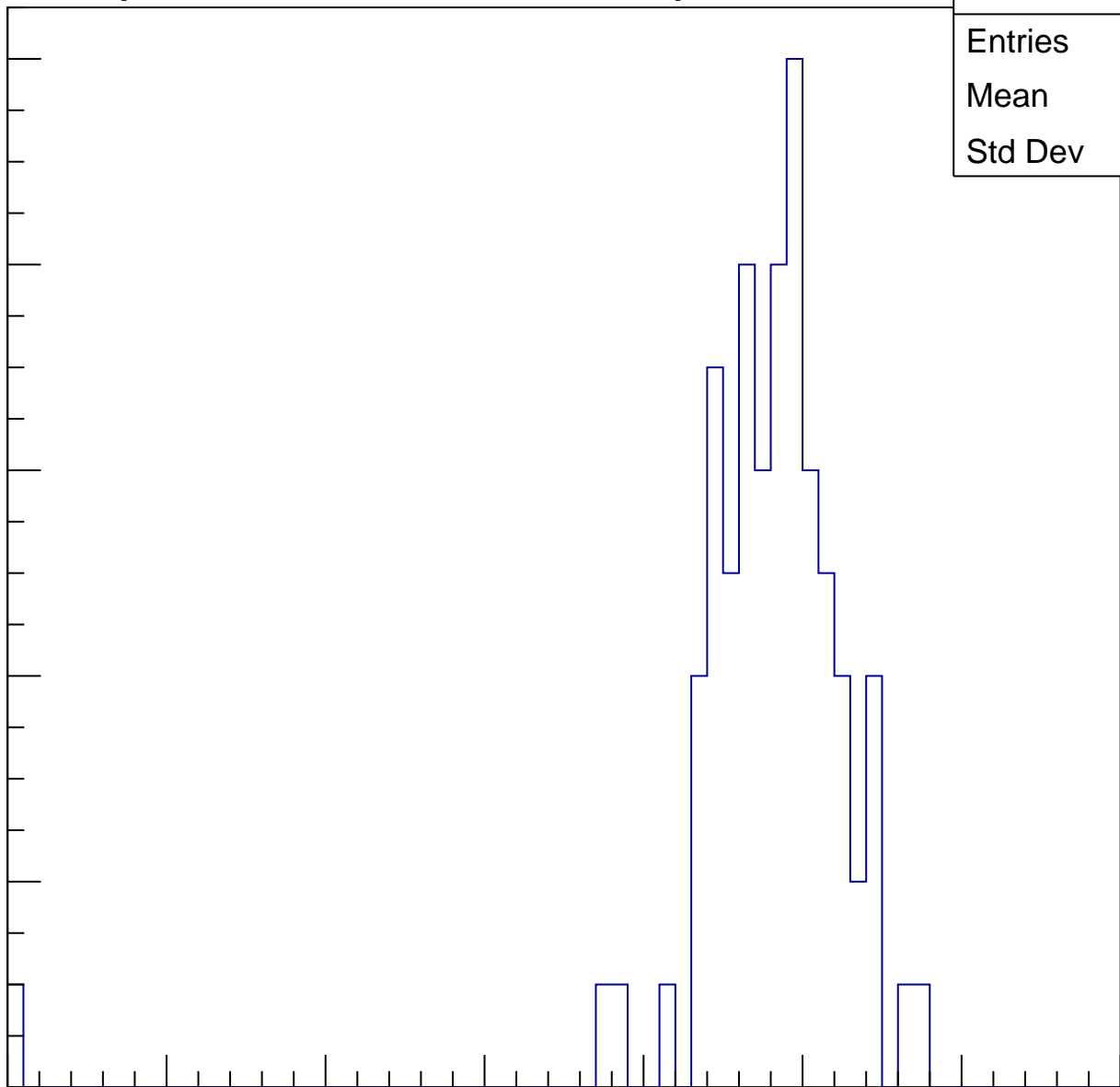
Entries	75
Mean	47.24
Std Dev	6.641

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

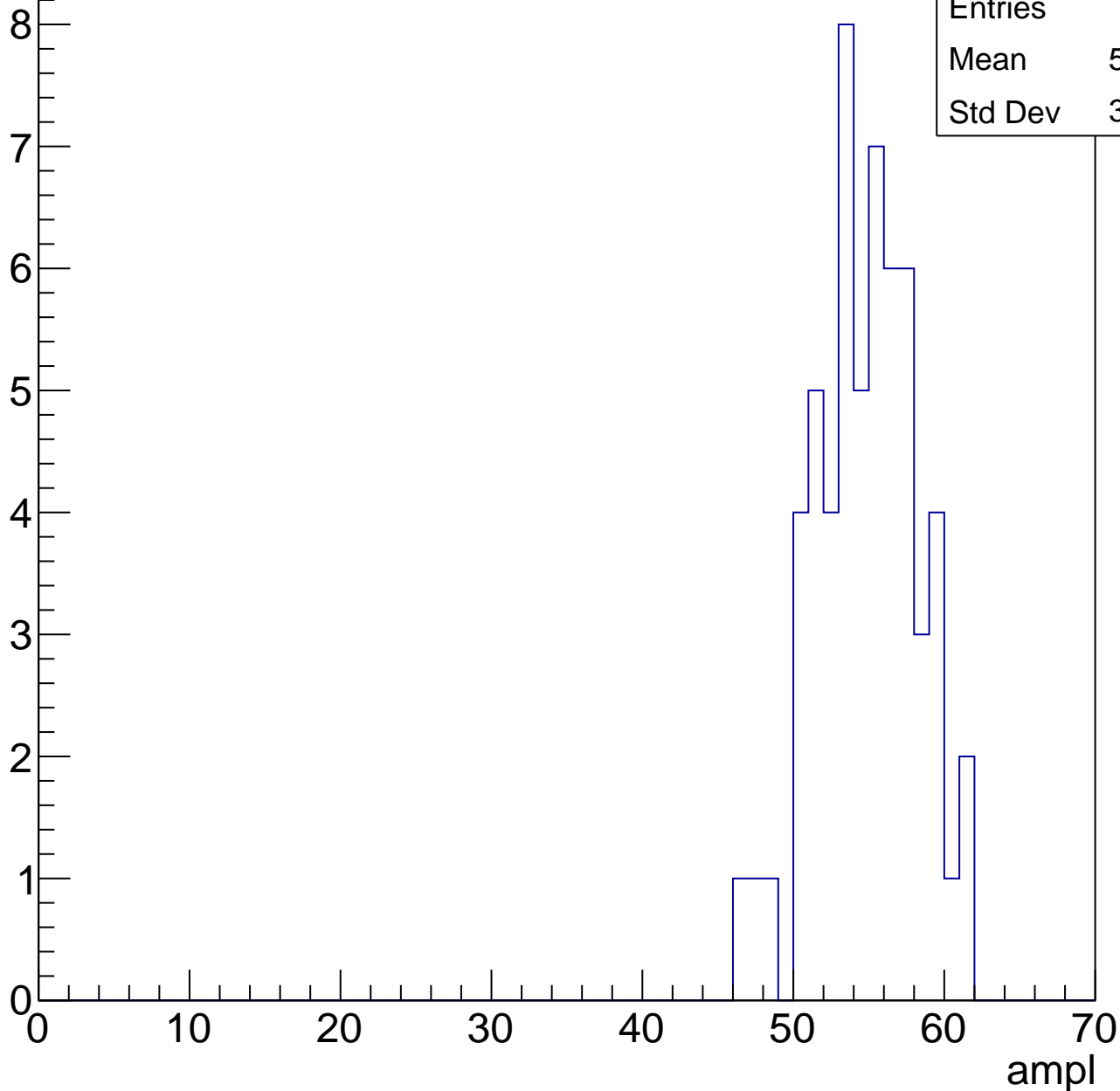


B1L103S, U5-ch79, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	54.36
Std Dev	3.325

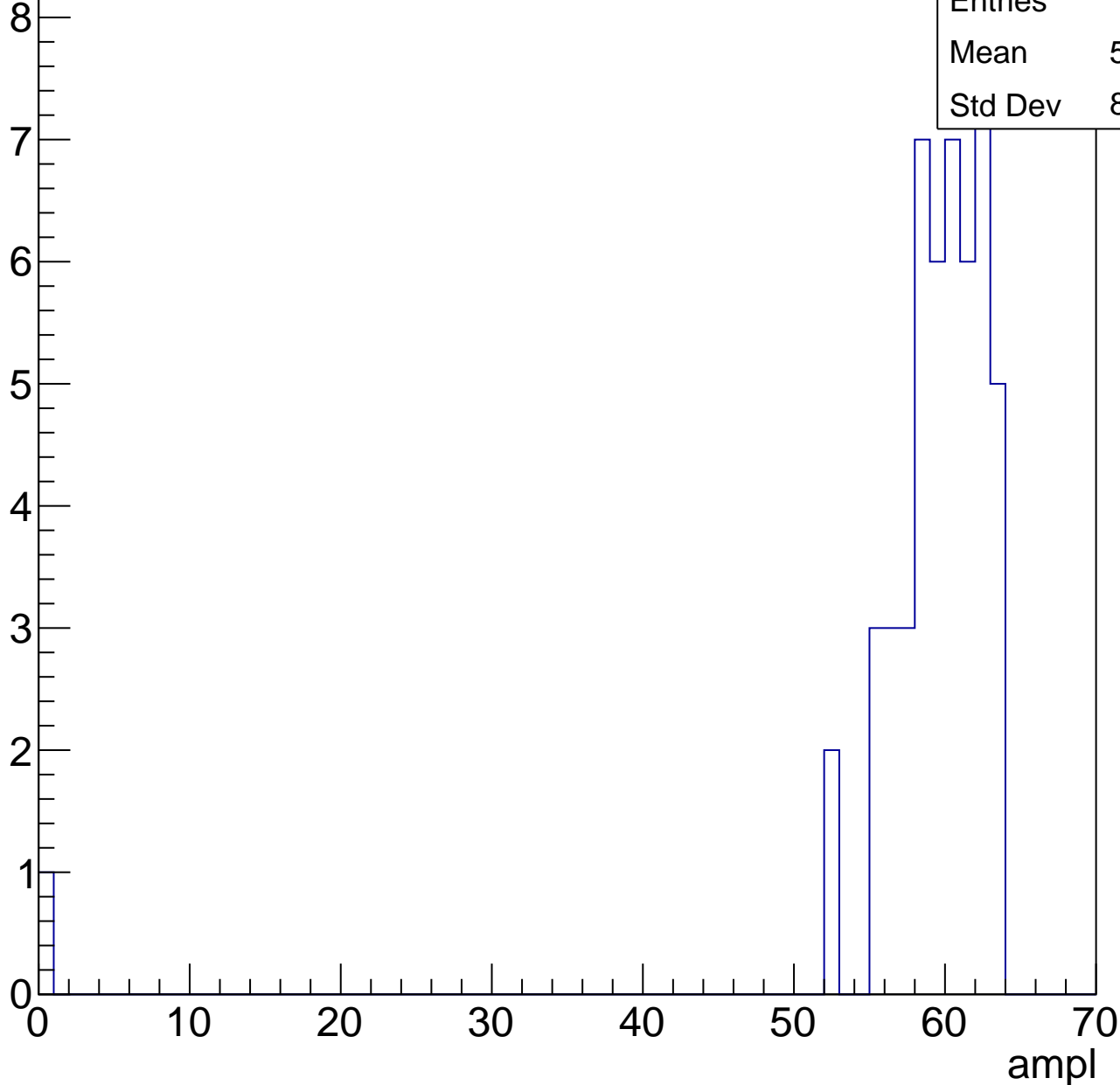


B1L103S, U5-ch79, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

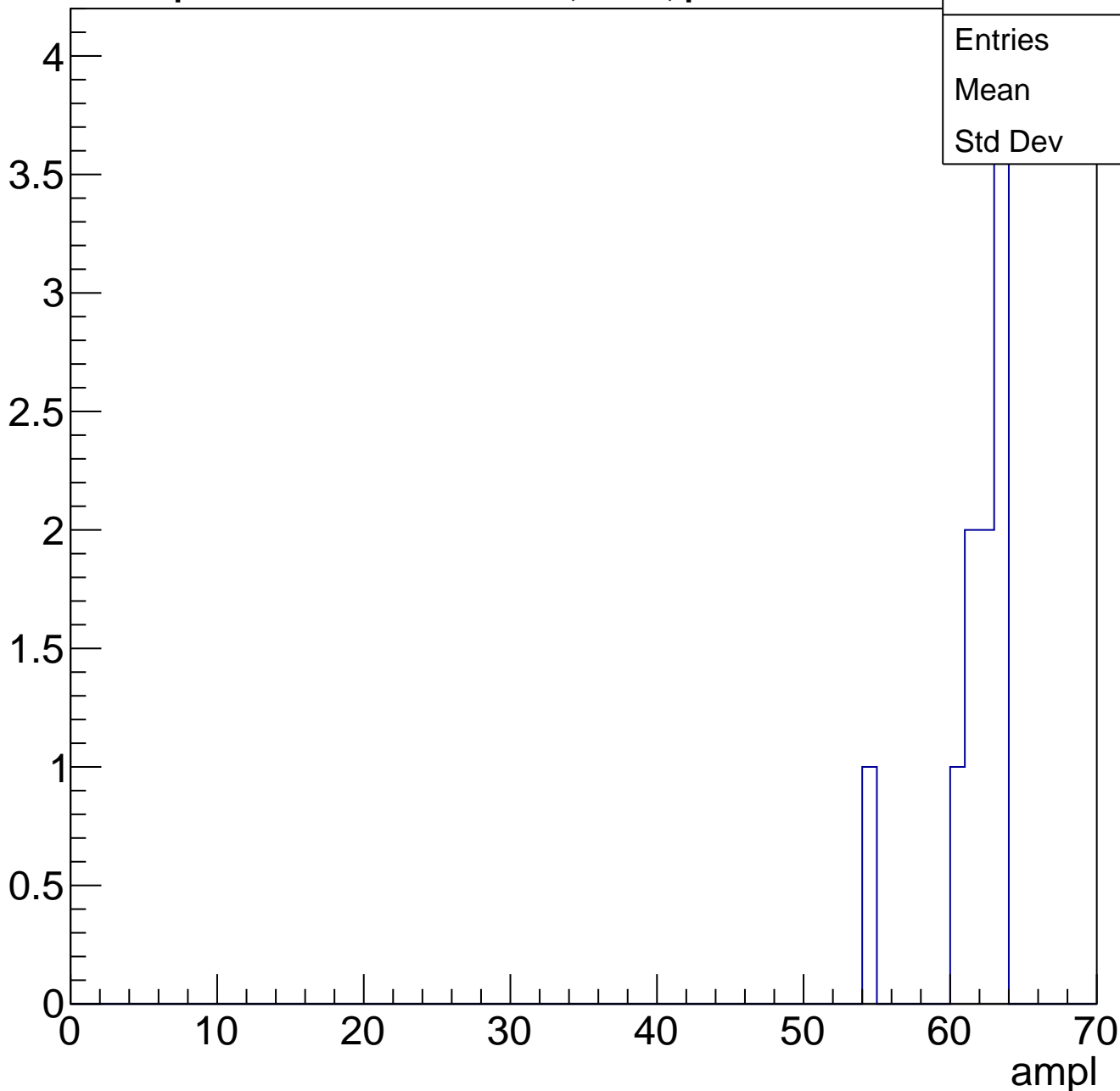
Entries	51
Mean	58.14
Std Dev	8.652



B1L103S, U5-ch79, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

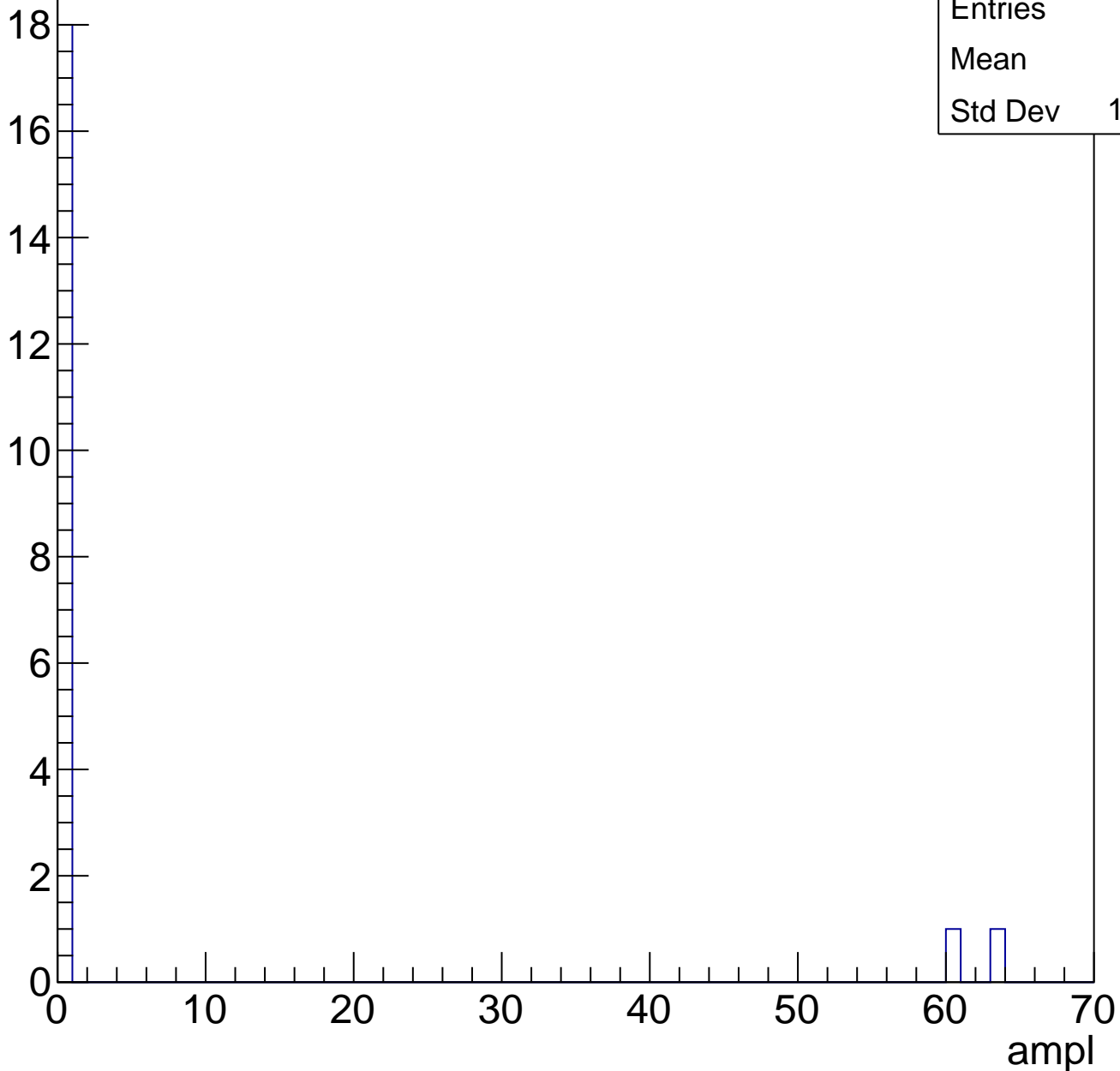


B1L103S, U5-ch79, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	6.15
Std Dev	18.46

Entry

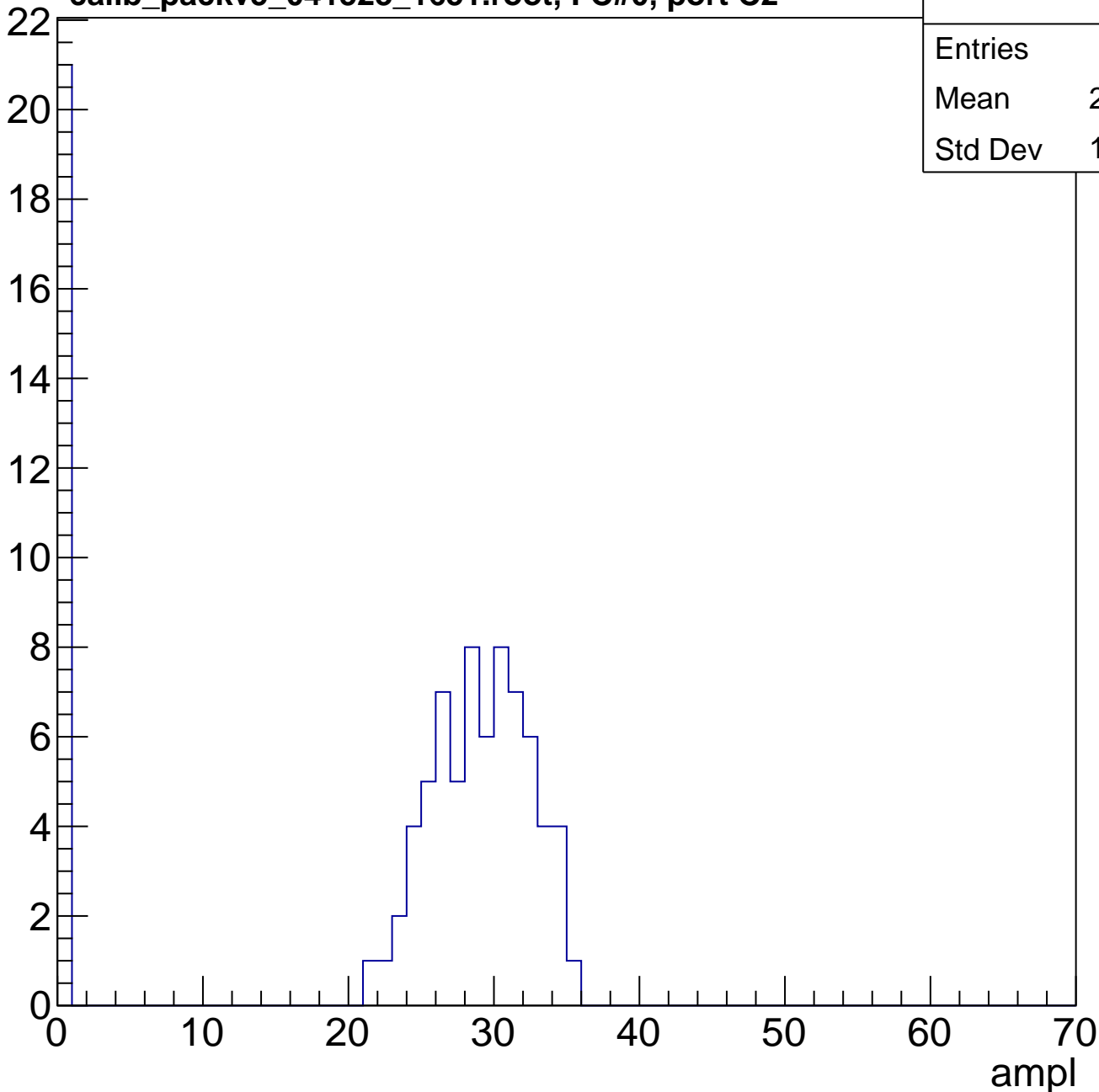


B1L103S, U5-ch80, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	90
Mean	21.97
Std Dev	12.45

Entry

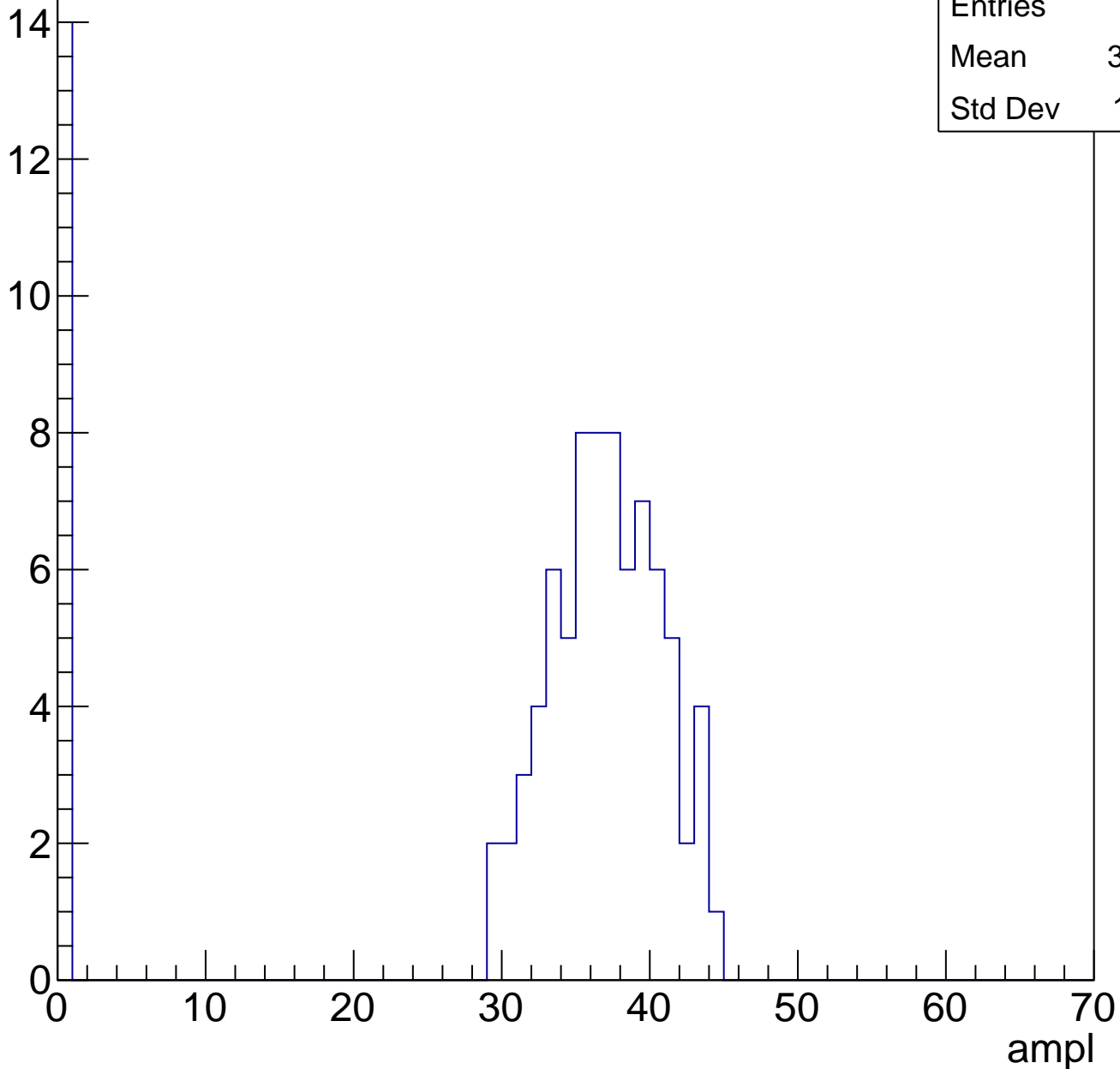


B1L103S, U5-ch80, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	91
Mean	30.96
Std Dev	13.61

Entry

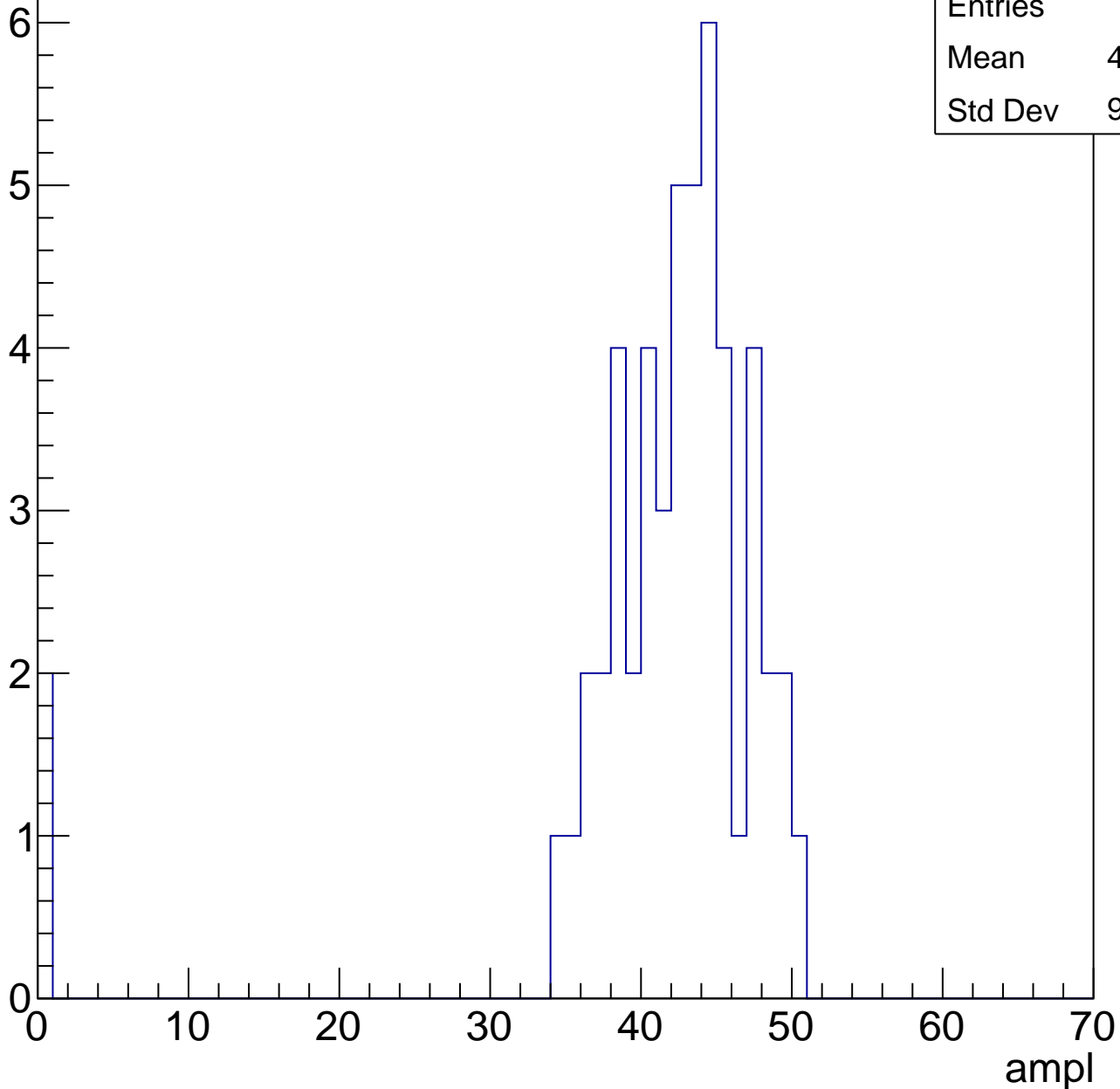


B1L103S, U5-ch80, adc2

calib_packv5_041523_1651.root, FC#0, port C2

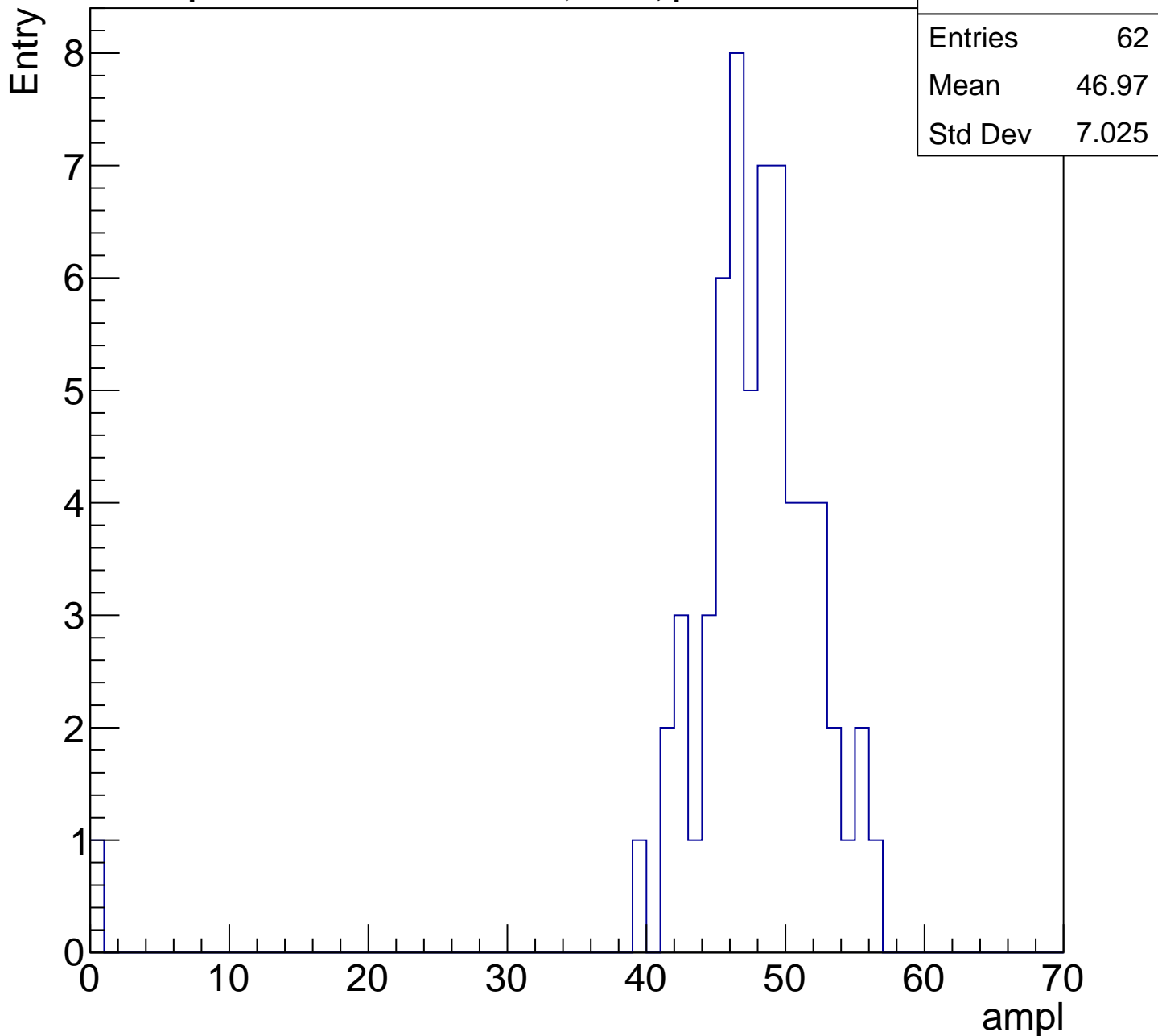
Entry

Entries	51
Mean	40.69
Std Dev	9.065



B1L103S, U5-ch80, adc3

calib_packv5_041523_1651.root, FC#0, port C2

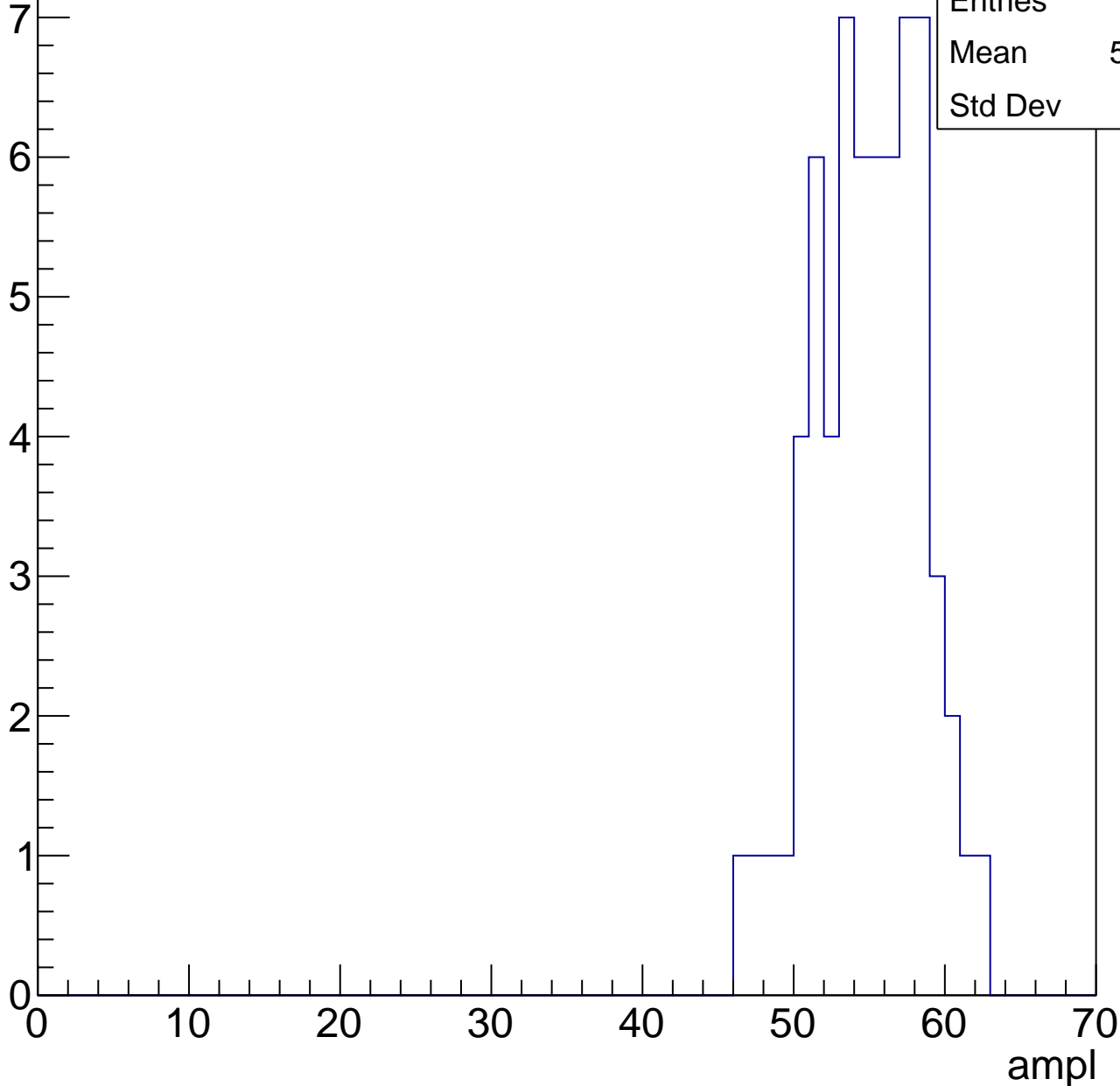


B1L103S, U5-ch80, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	54.53
Std Dev	3.45

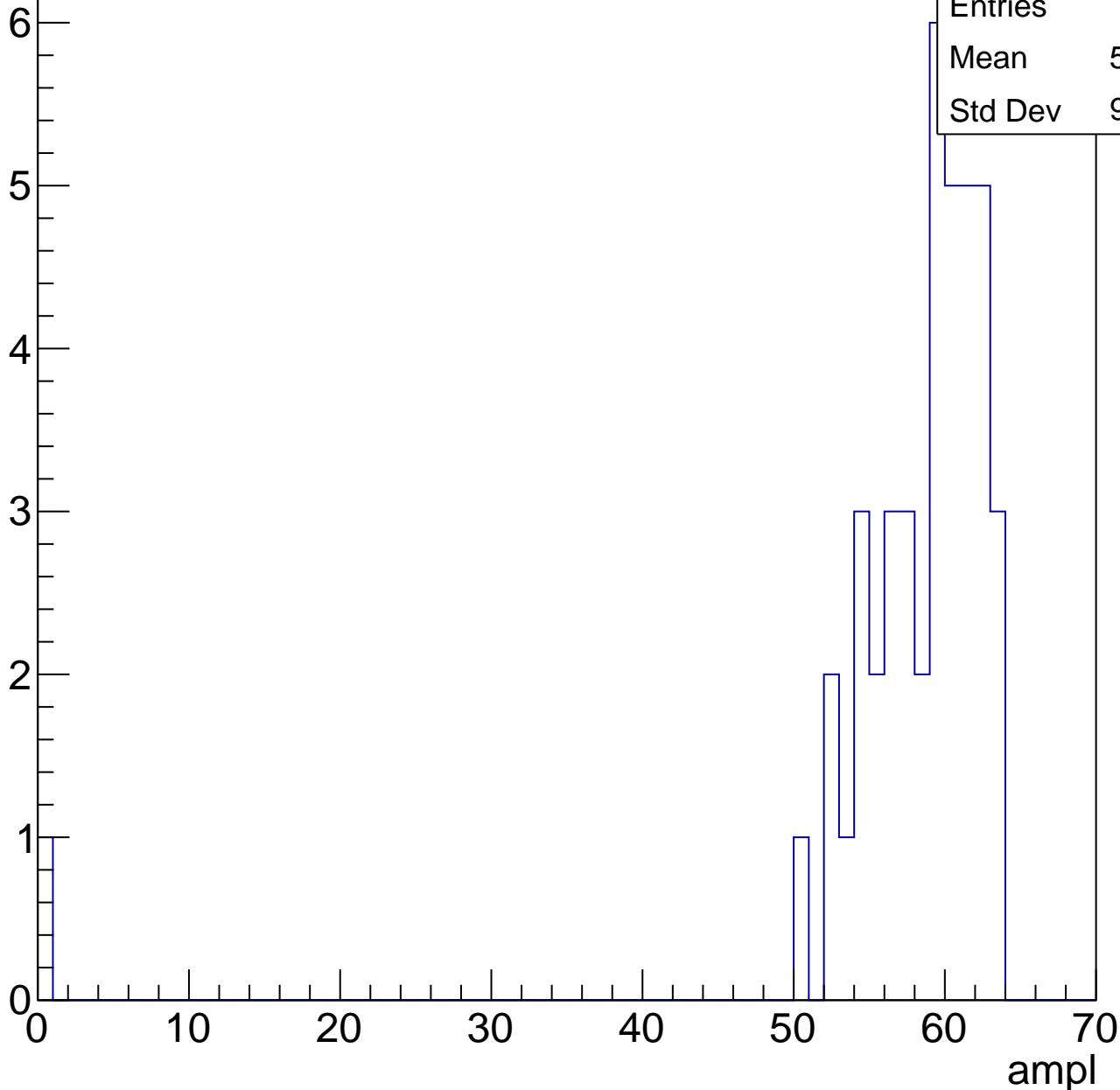


B1L103S, U5-ch80, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	42
Mean	56.95
Std Dev	9.494

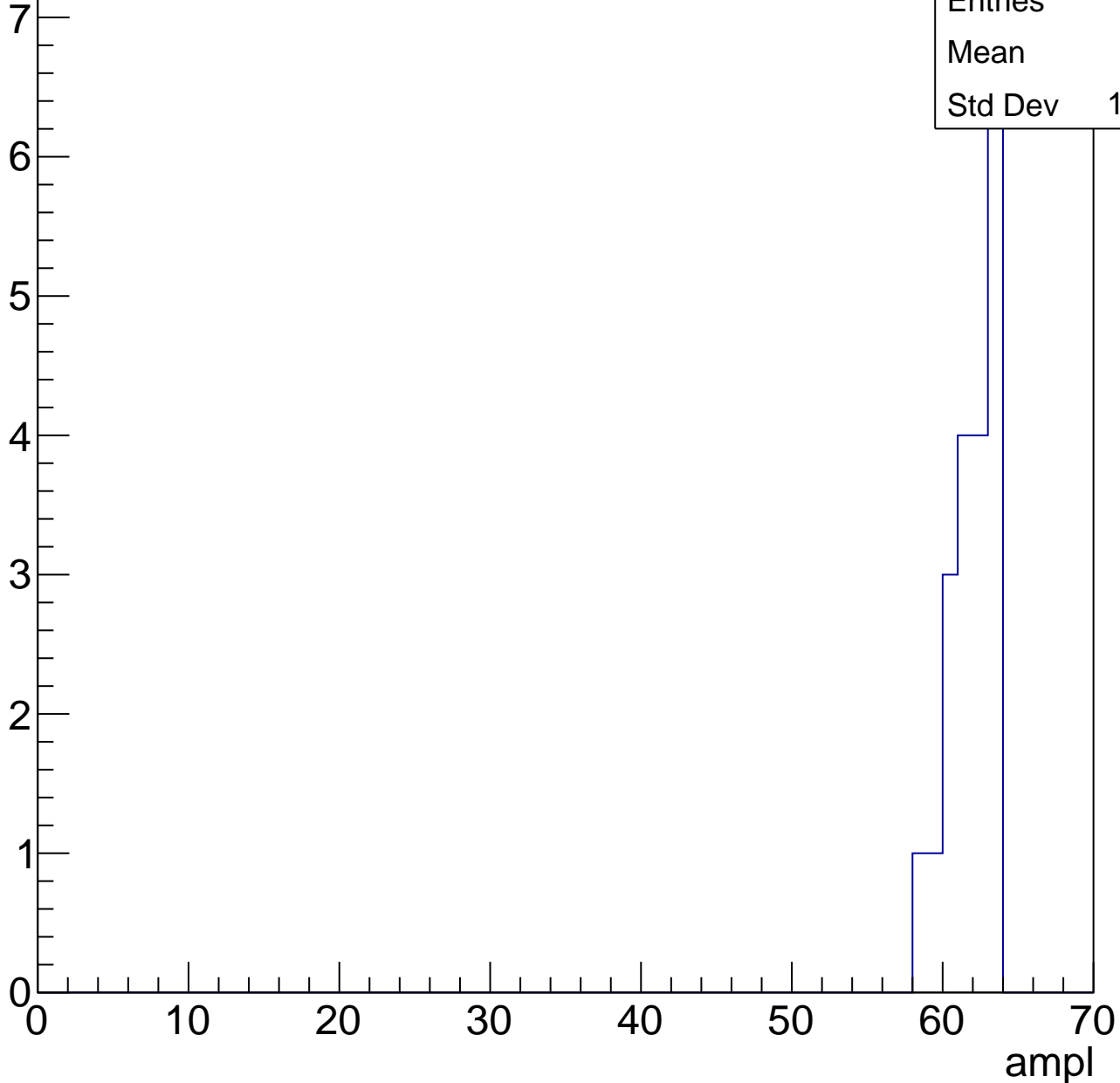


B1L103S, U5-ch80, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	20
Mean	61.5
Std Dev	1.466



B1L103S, U5-ch80, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

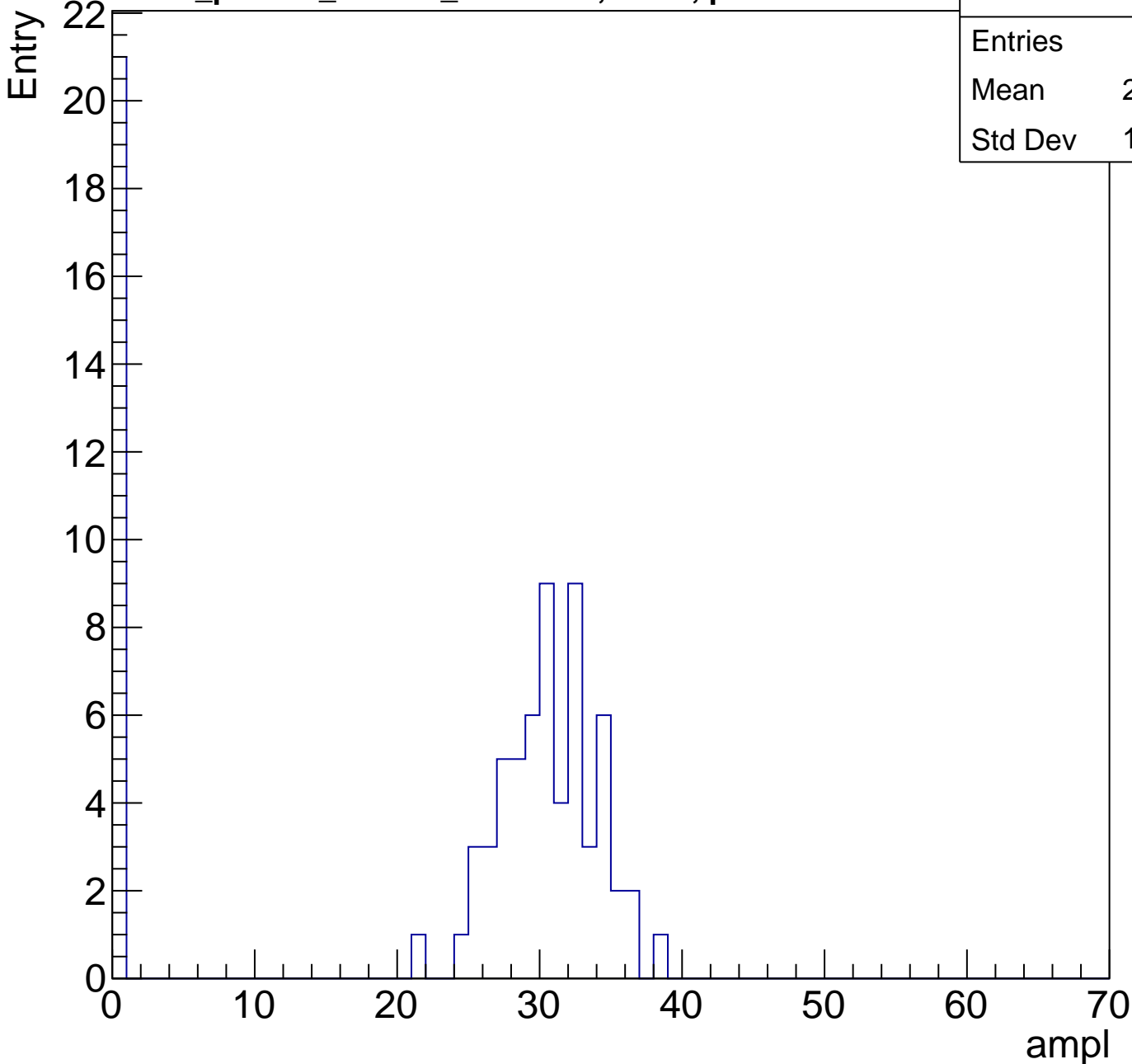
Entries	18
Mean	0
Std Dev	0

ampl

B1L103S, U5-ch81, adc0

calib_packv5_041523_1651.root, FC#0, port C2

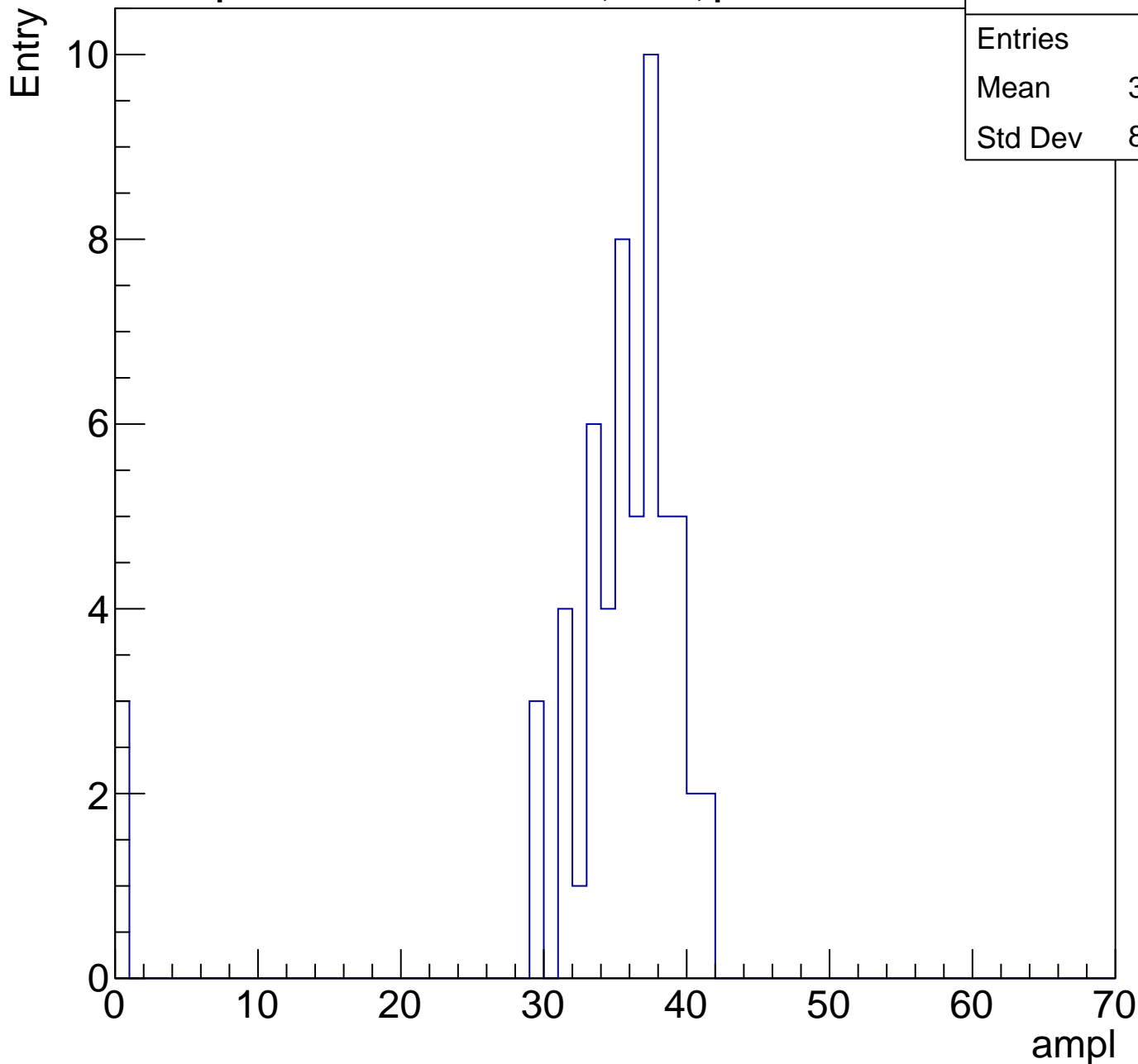
Entries	81
Mean	22.37
Std Dev	13.54



B1L103S, U5-ch81, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	58
Mean	33.69
Std Dev	8.383



B1L103S, U5-ch81, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	74
Mean	35.65
Std Dev	15.1

Entry

10

8

6

4

2

0

0

10

20

30

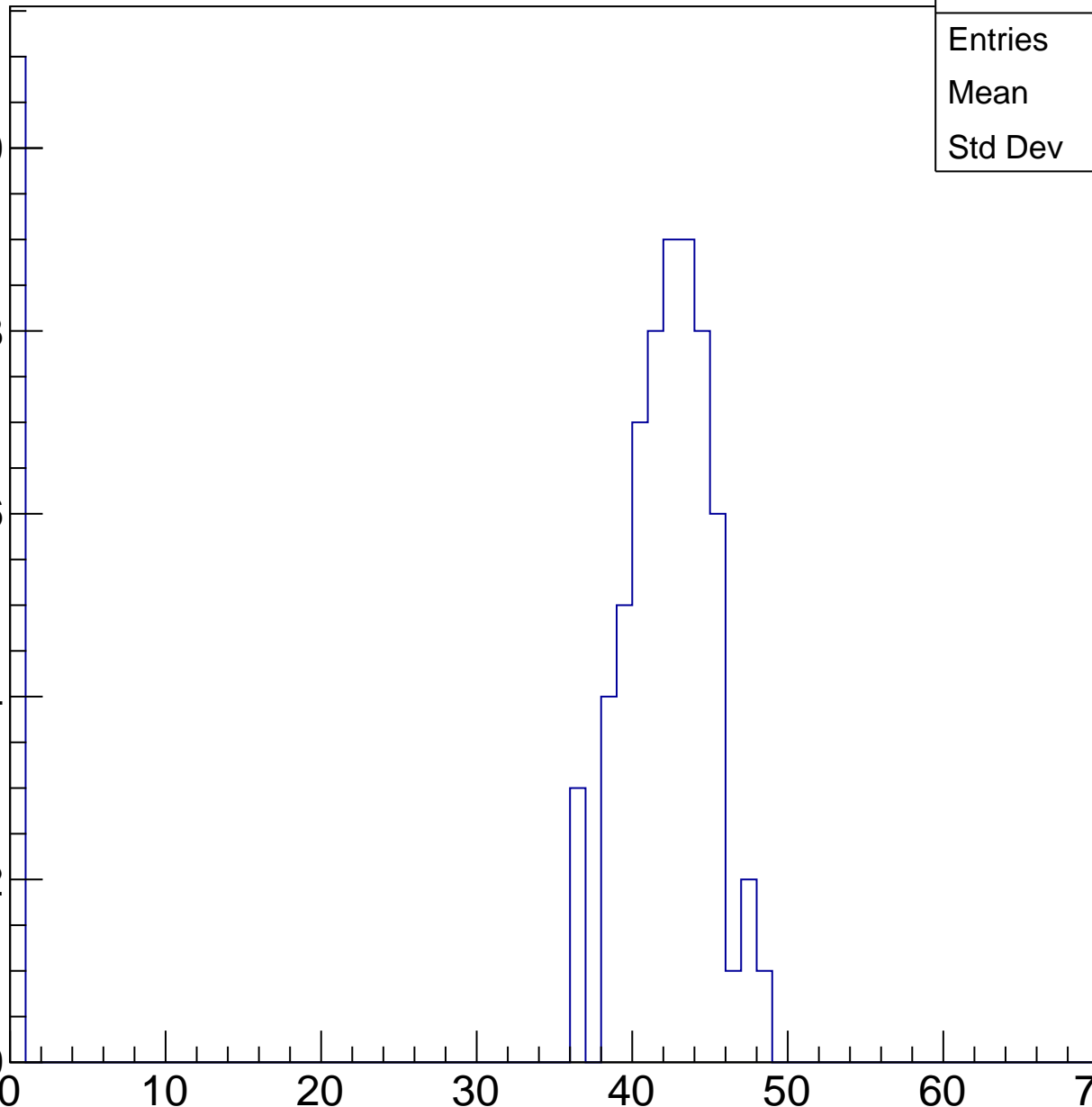
40

50

60

70

ampl

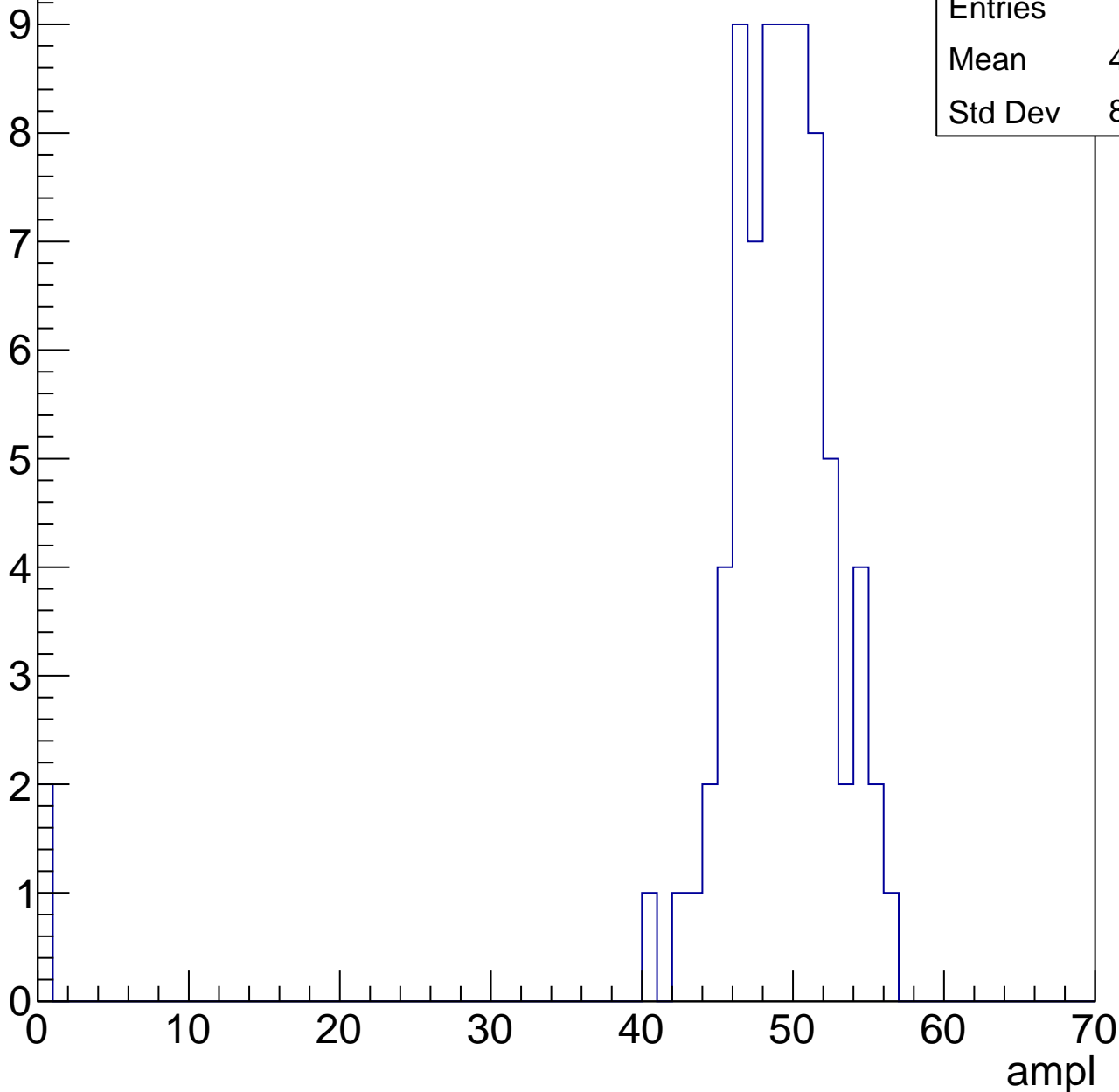


B1L103S, U5-ch81, adc3

calib_packv5_041523_1651.root, FC#0, port C2

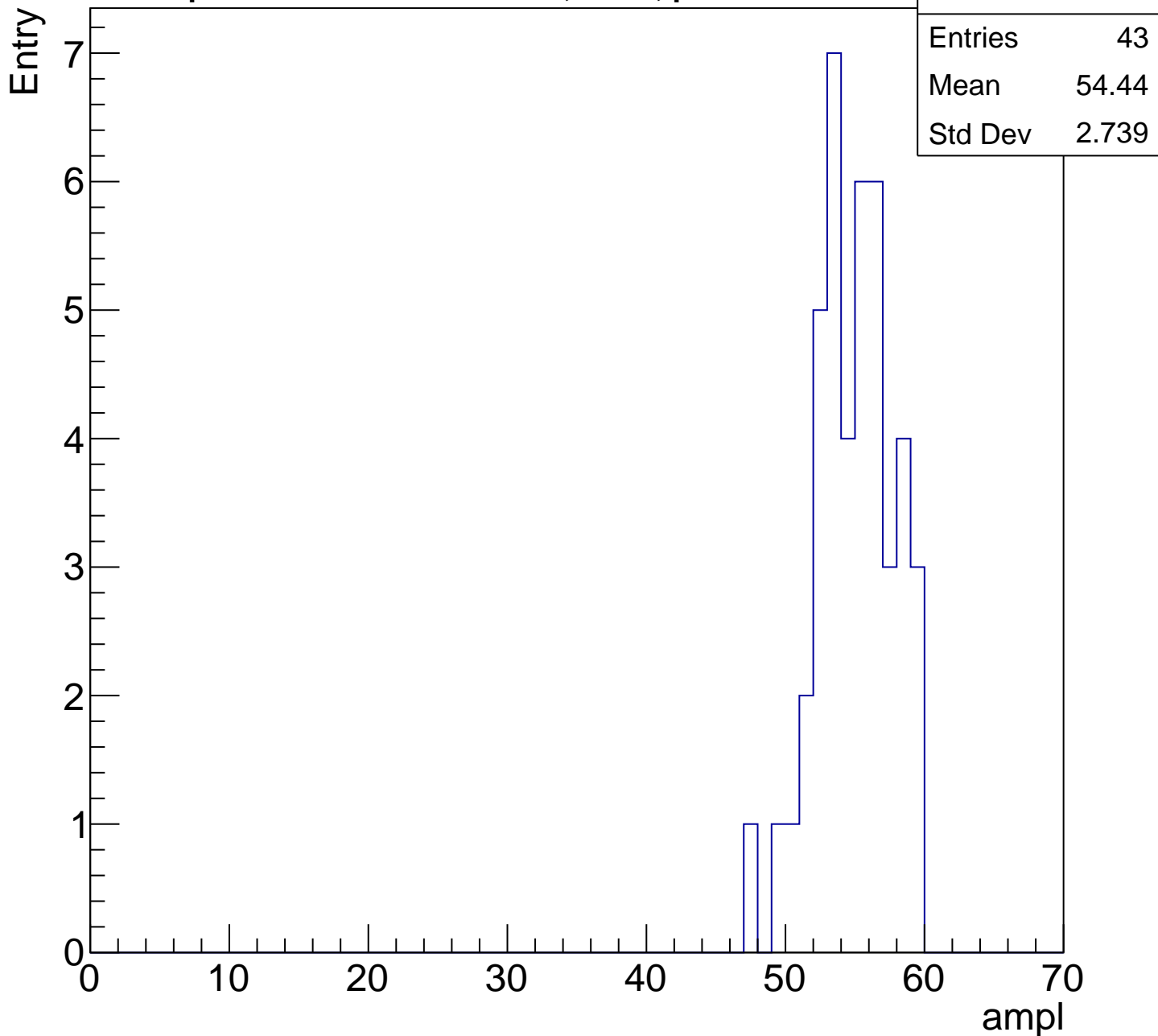
Entry

Entries	76
Mean	47.57
Std Dev	8.416



B1L103S, U5-ch81, adc4

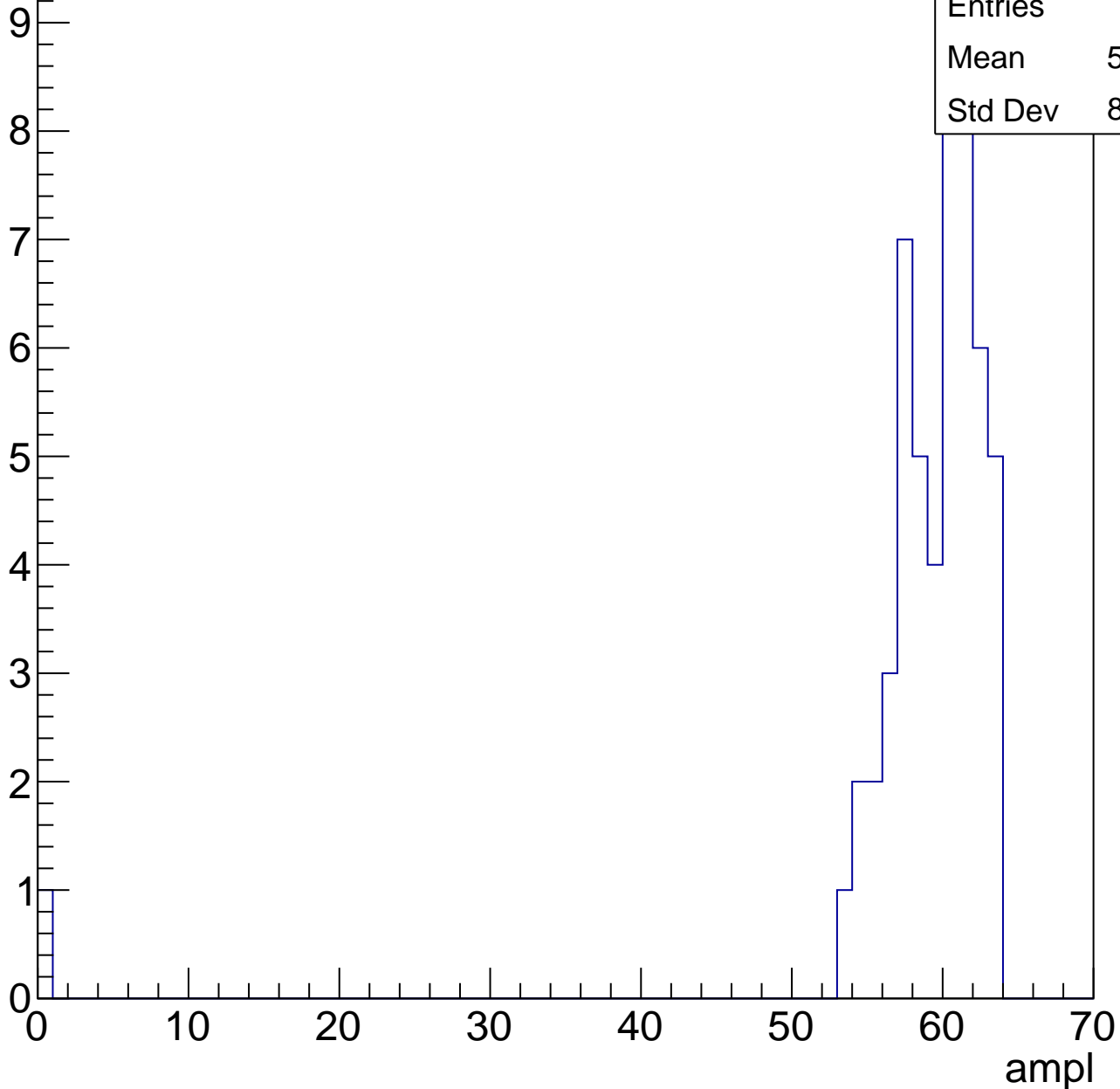
calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U5-ch81, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

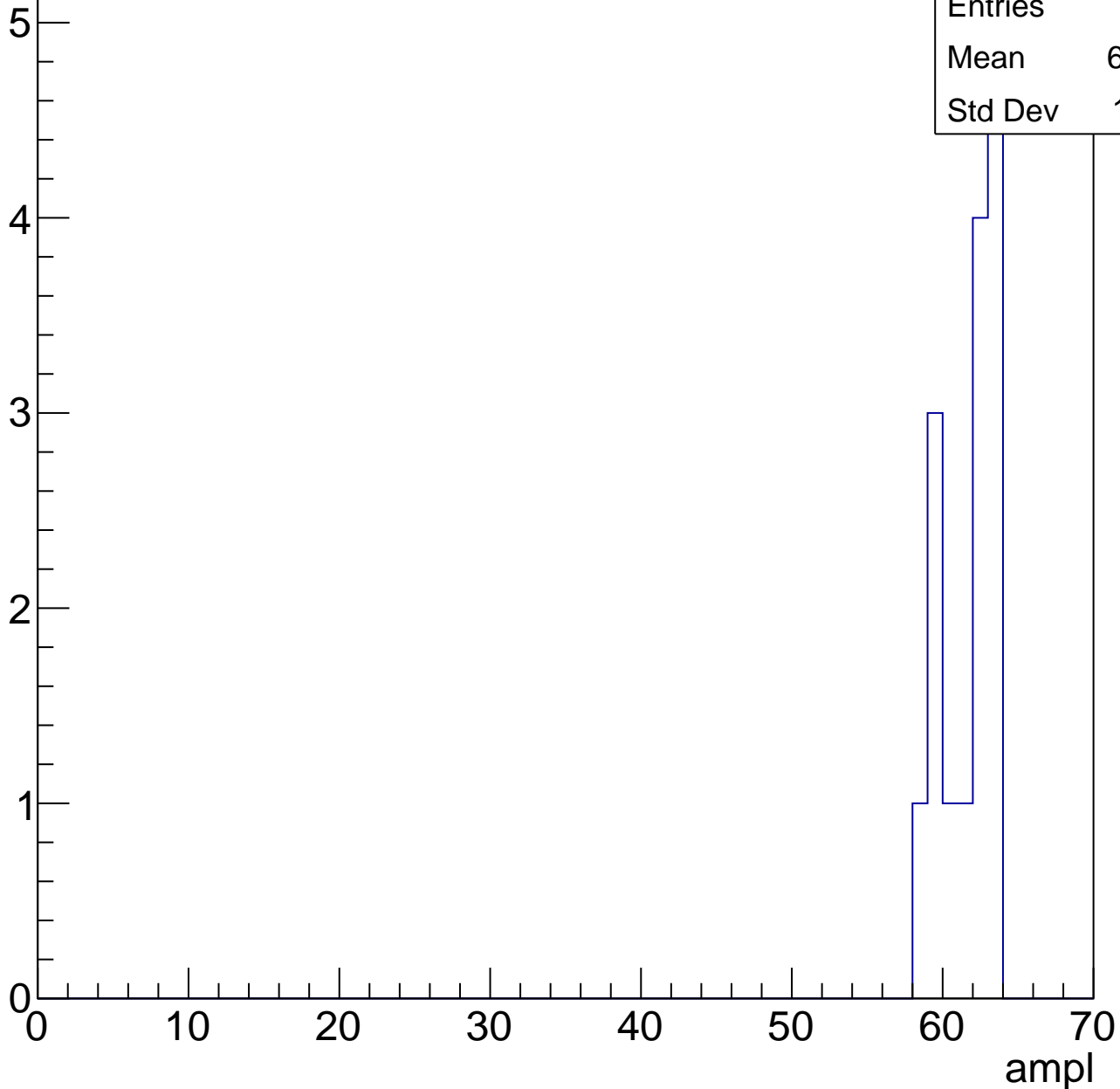


B1L103S, U5-ch81, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	15
Mean	61.27
Std Dev	1.731



B1L103S, U5-ch81, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U5-ch82, adc0

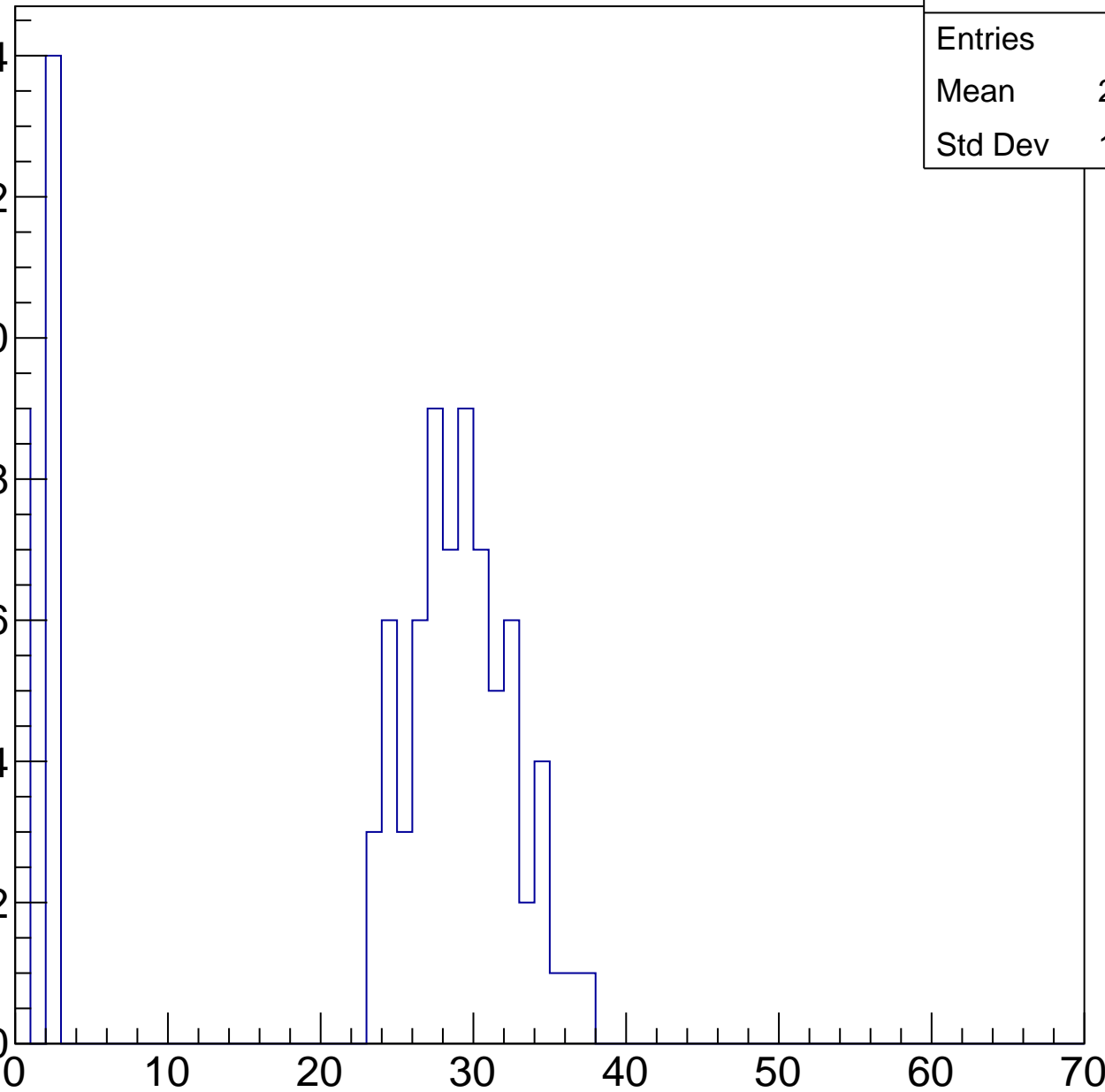
calib_packv5_041523_1651.root, FC#0, port C2

Entries	93
Mean	21.92
Std Dev	12.22

Entry

14
12
10
8
6
4
2
0

ampl

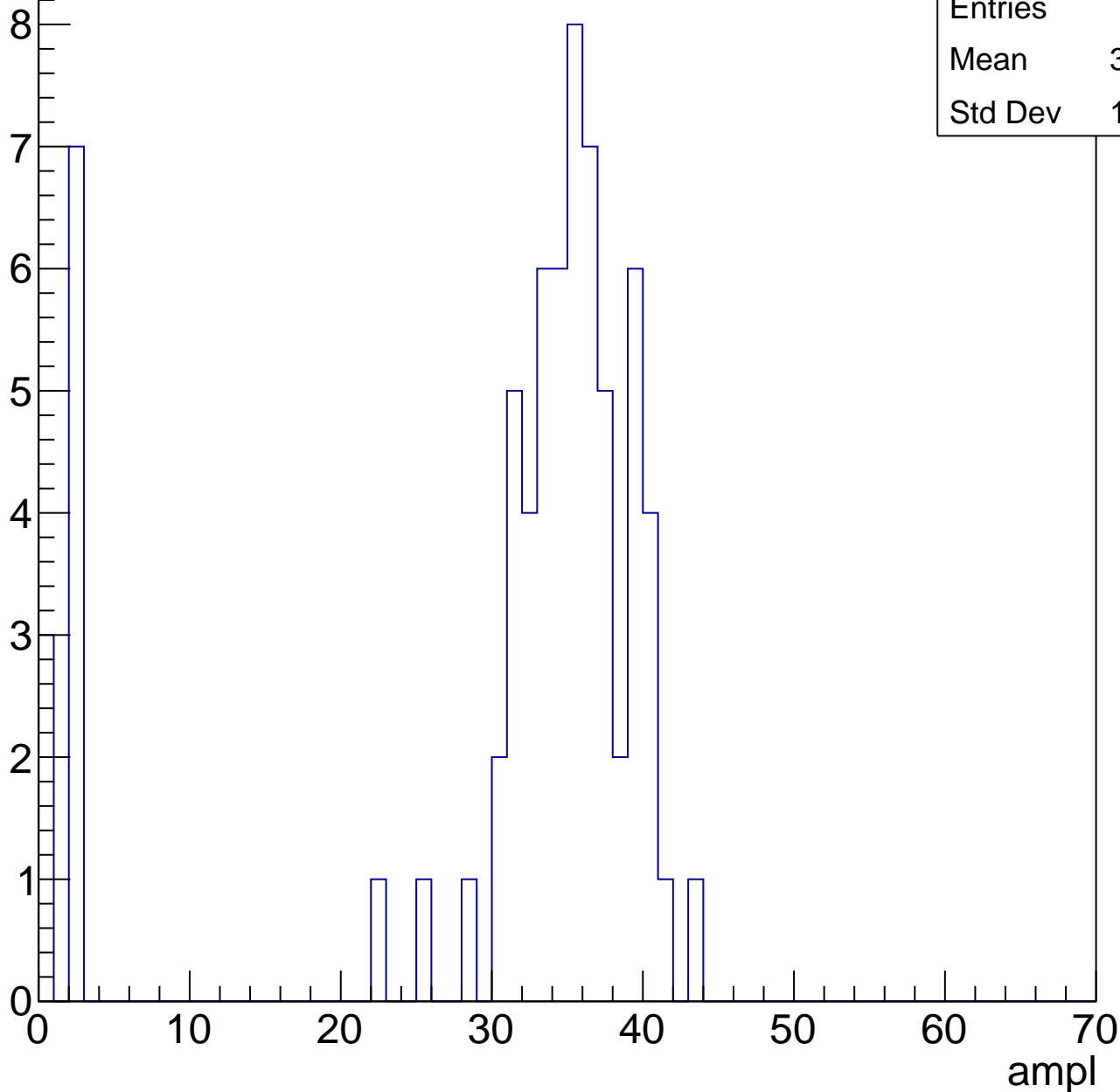


B1L103S, U5-ch82, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	30.07
Std Dev	12.22



B1L103S, U5-ch82, adc2

calib_packv5_041523_1651.root, FC#0, port C2

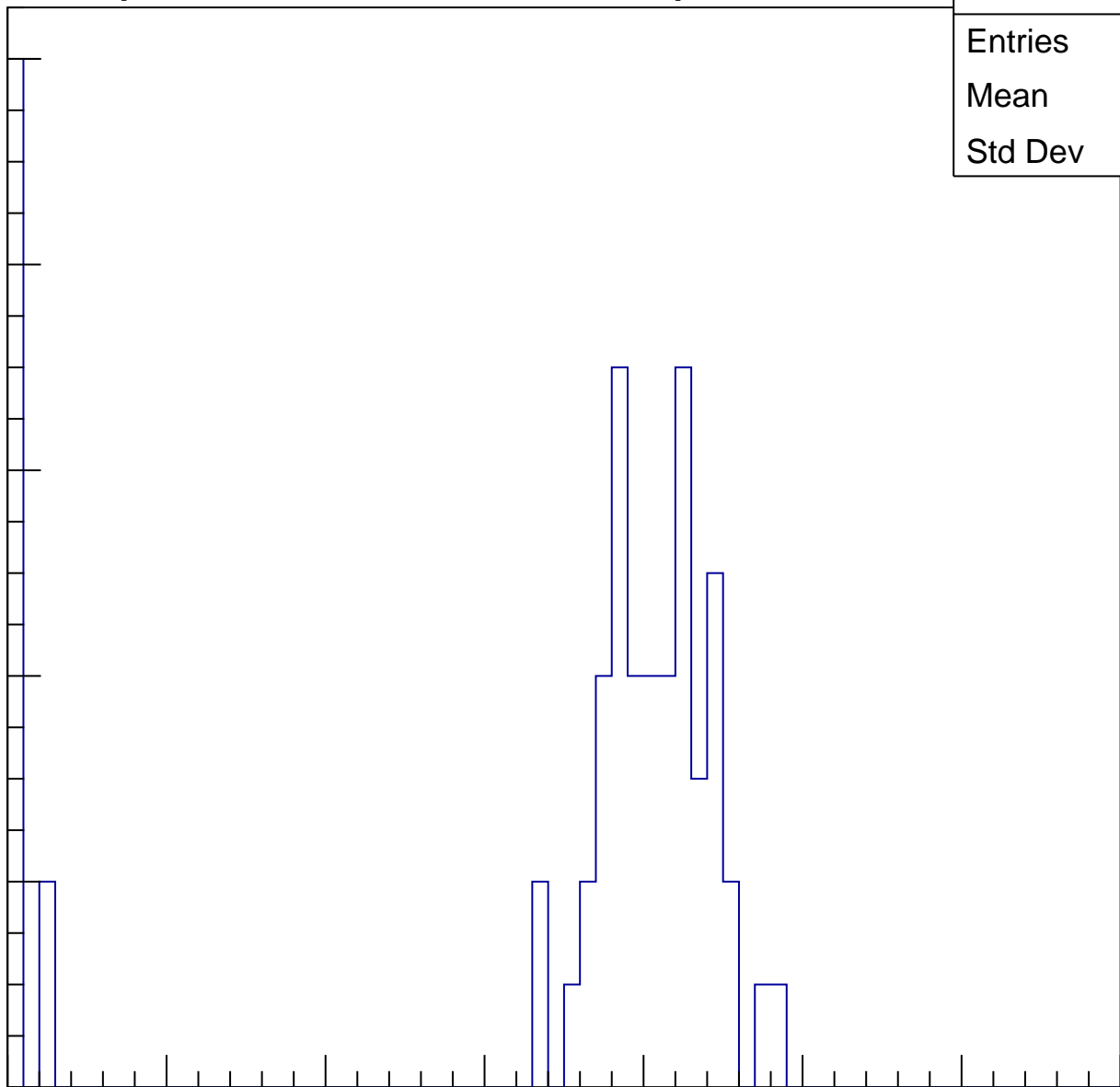
Entries	59
Mean	32.19
Std Dev	16.37

Entry

10
8
6
4
2
0

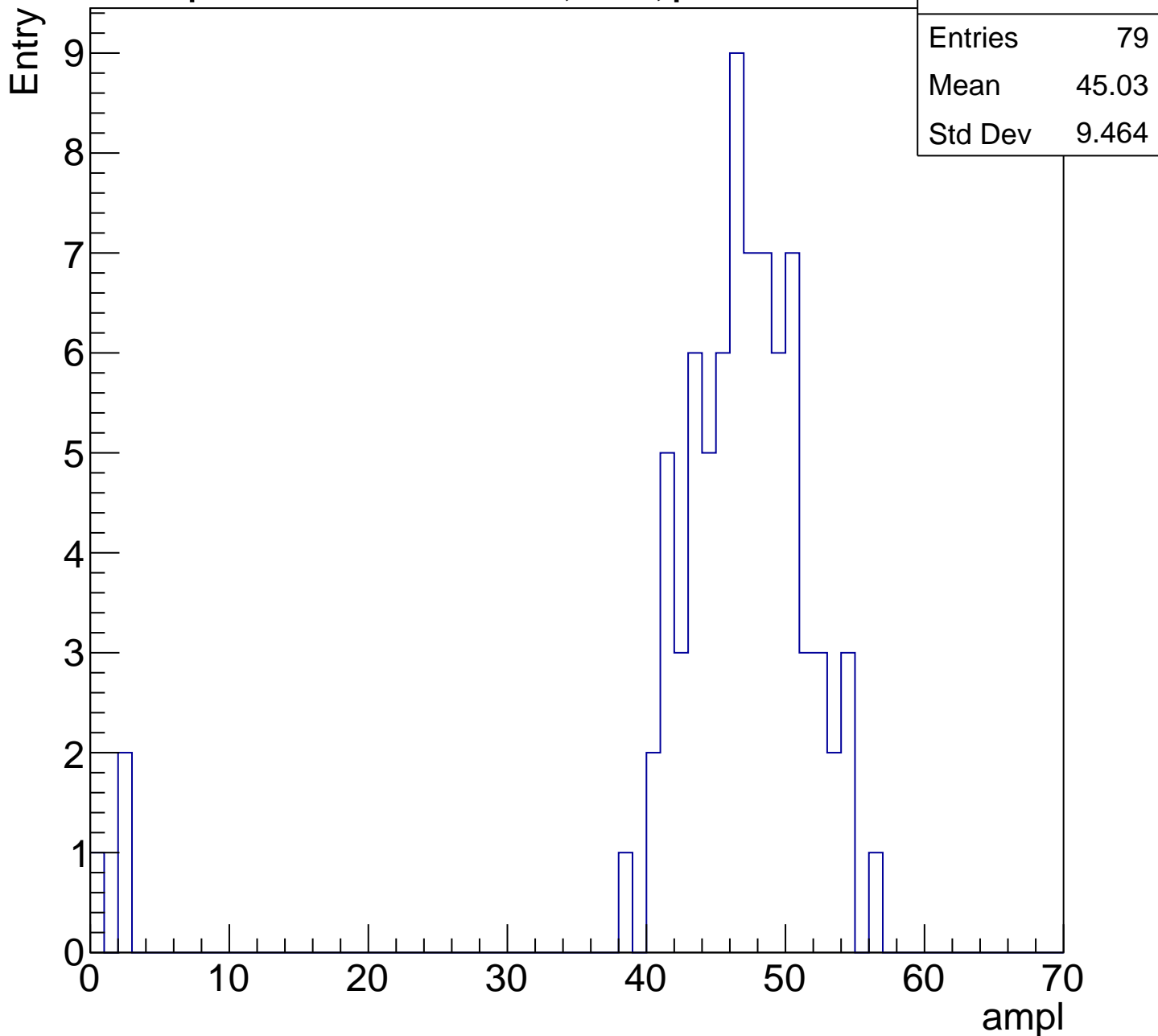
ampl

0 10 20 30 40 50 60 70



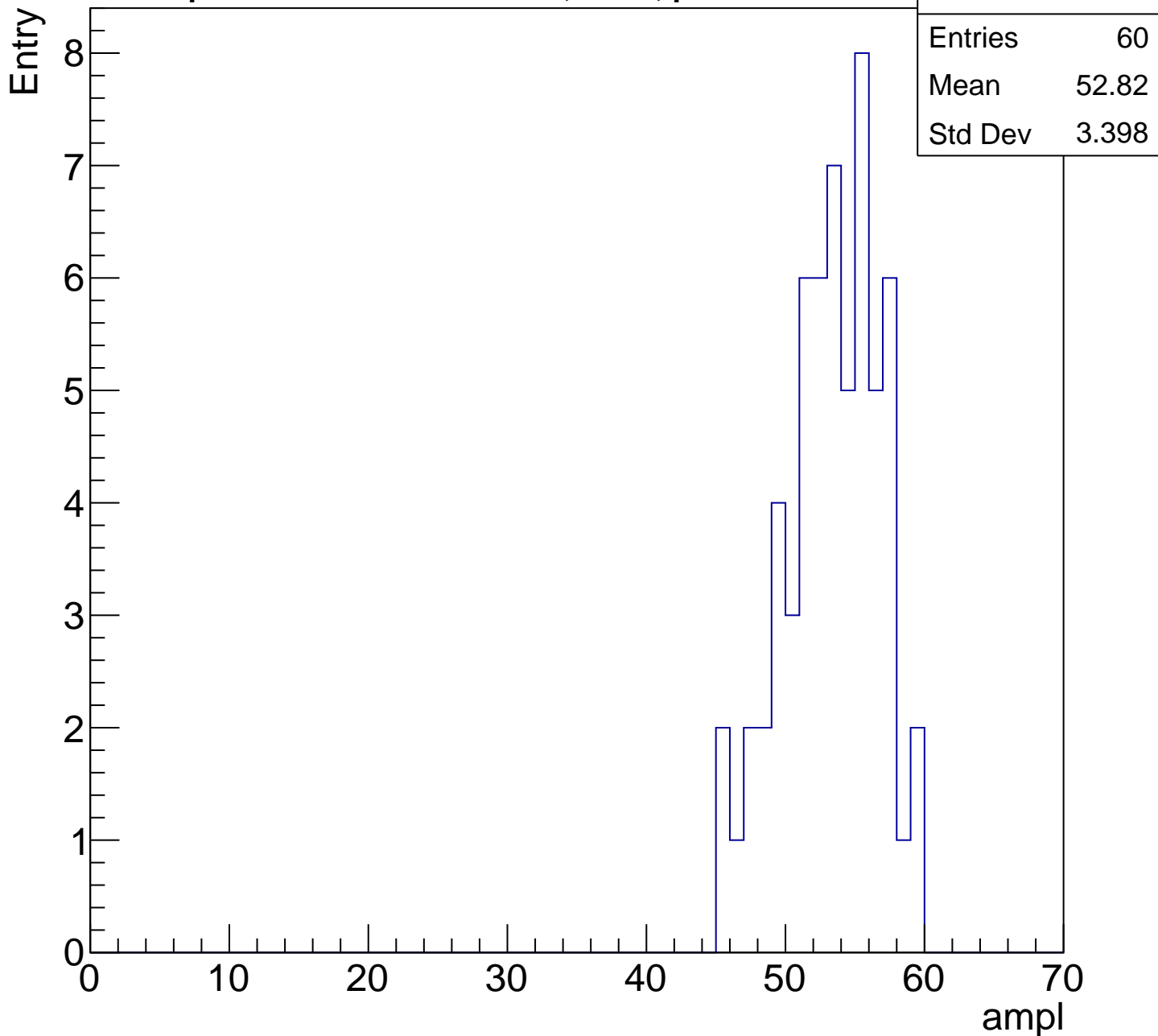
B1L103S, U5-ch82, adc3

calib_packv5_041523_1651.root, FC#0, port C2



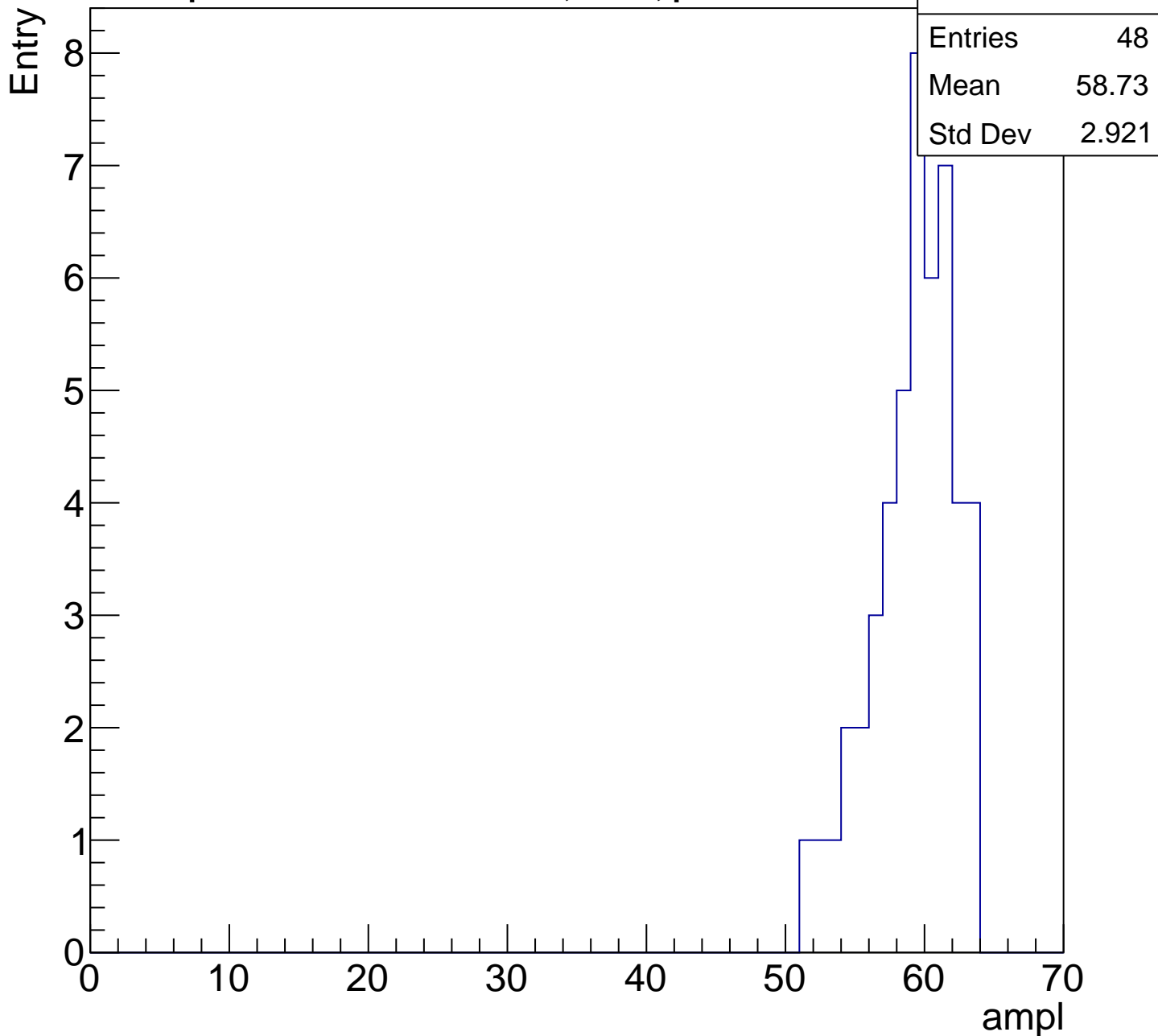
B1L103S, U5-ch82, adc4

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U5-ch82, adc5

calib_packv5_041523_1651.root, FC#0, port C2

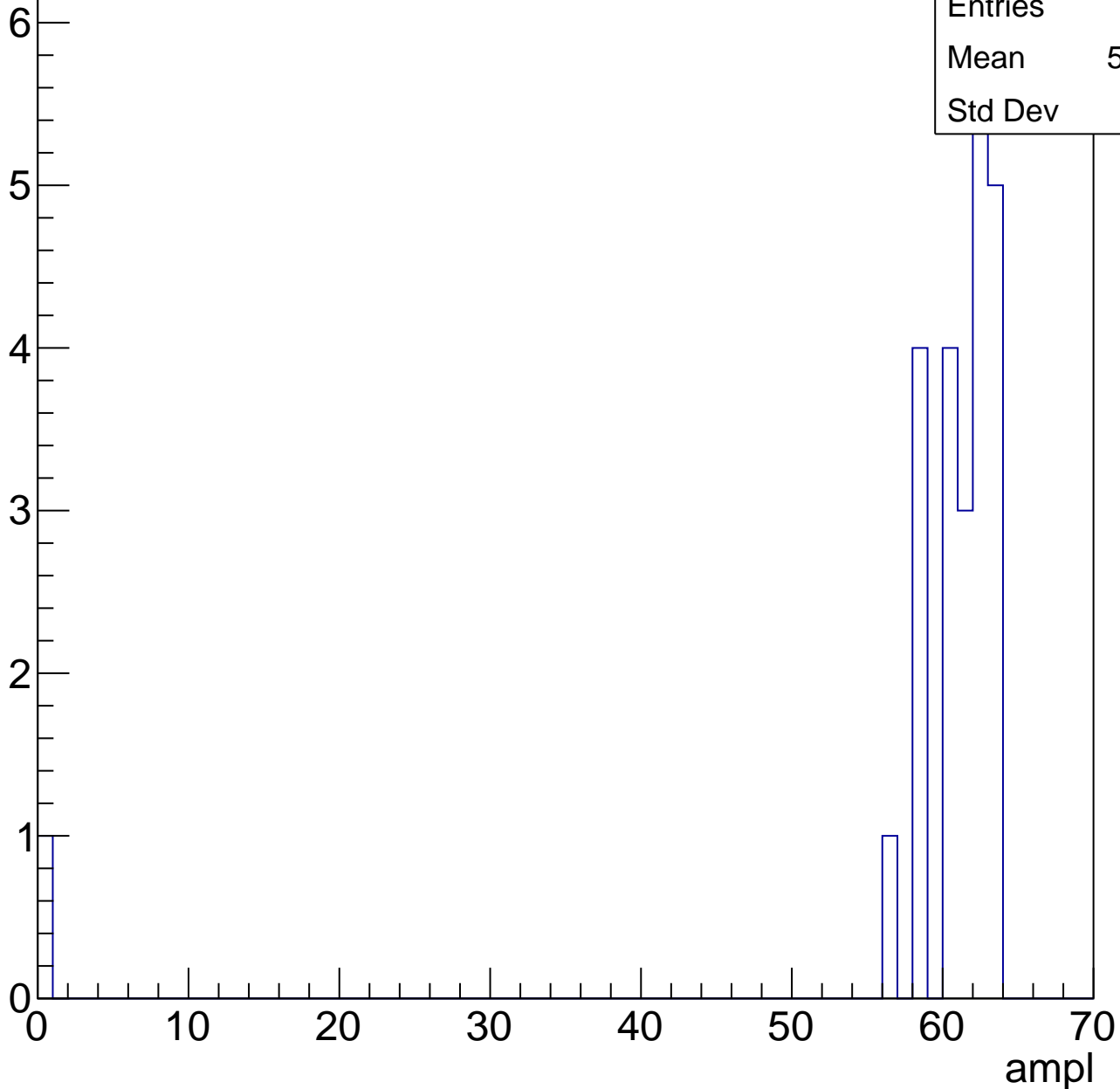


B1L103S, U5-ch82, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	24
Mean	58.25
Std Dev	12.3

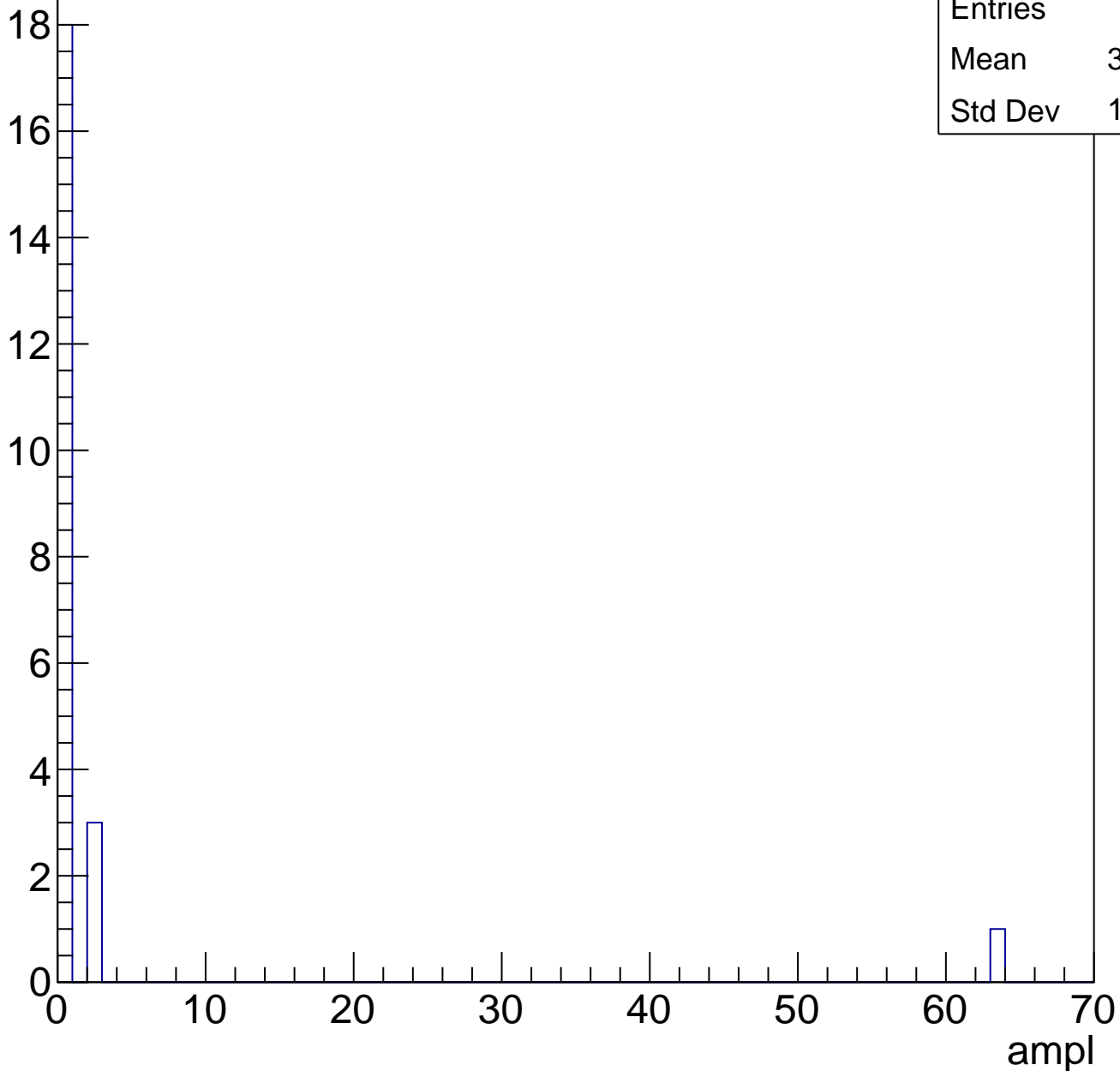


B1L103S, U5-ch82, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	22
Mean	3.136
Std Dev	13.08

Entry



B1L103S, U5-ch83, adc0

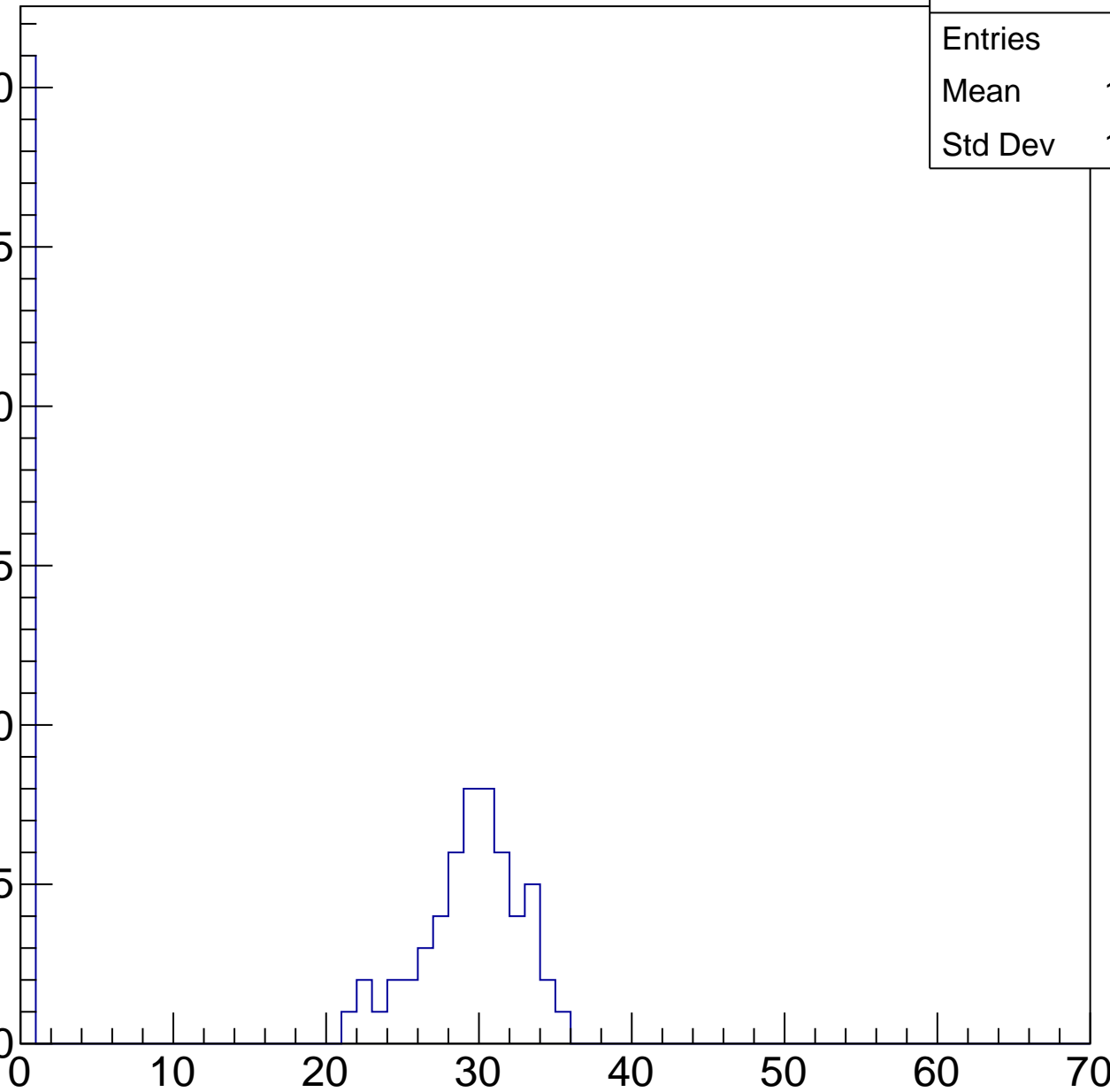
calib_packv5_041523_1651.root, FC#0, port C2

Entries	86
Mean	18.53
Std Dev	14.15

Entry

30
25
20
15
10
5
0

ampl

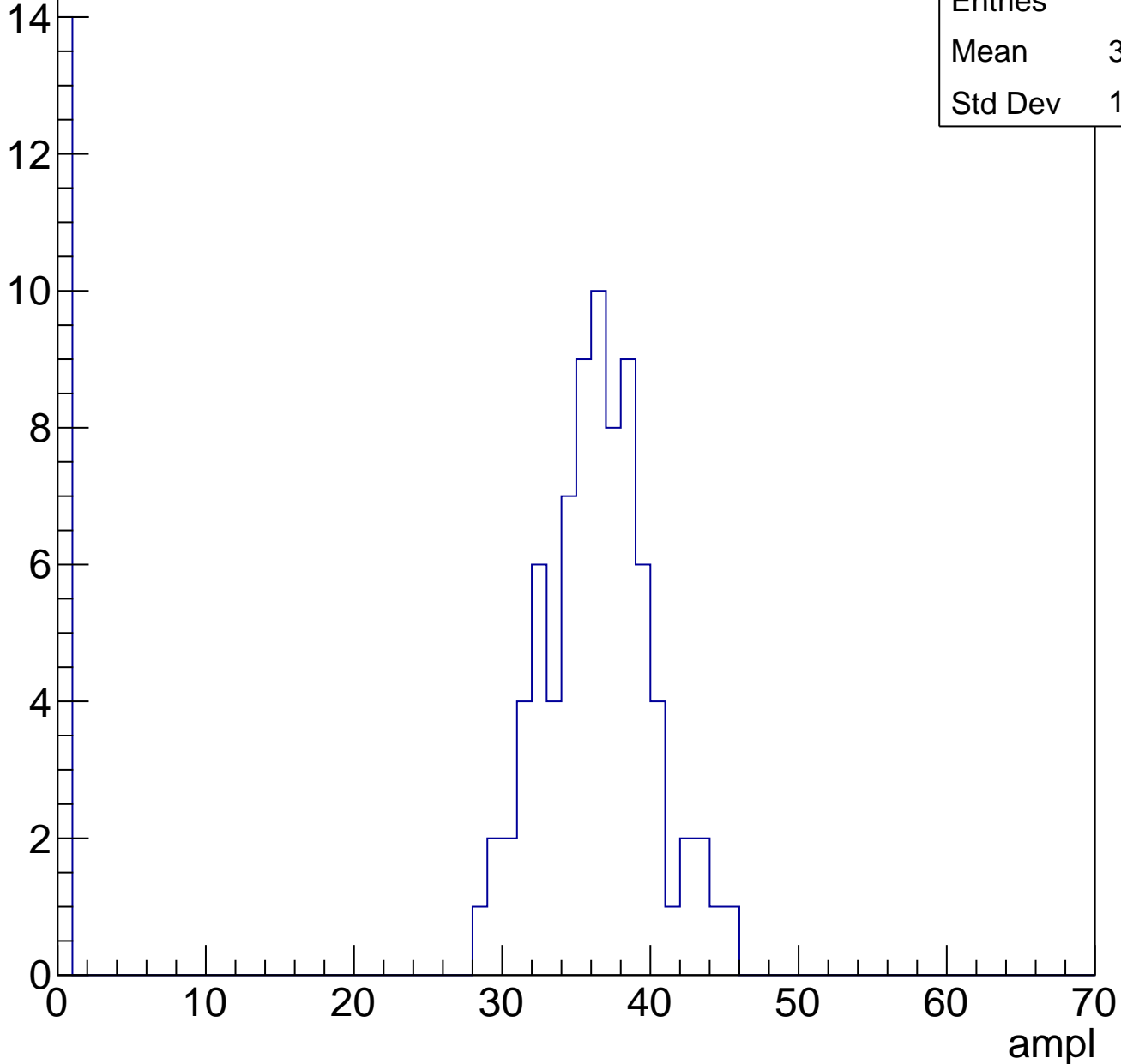


B1L103S, U5-ch83, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	93
Mean	30.53
Std Dev	13.26

Entry

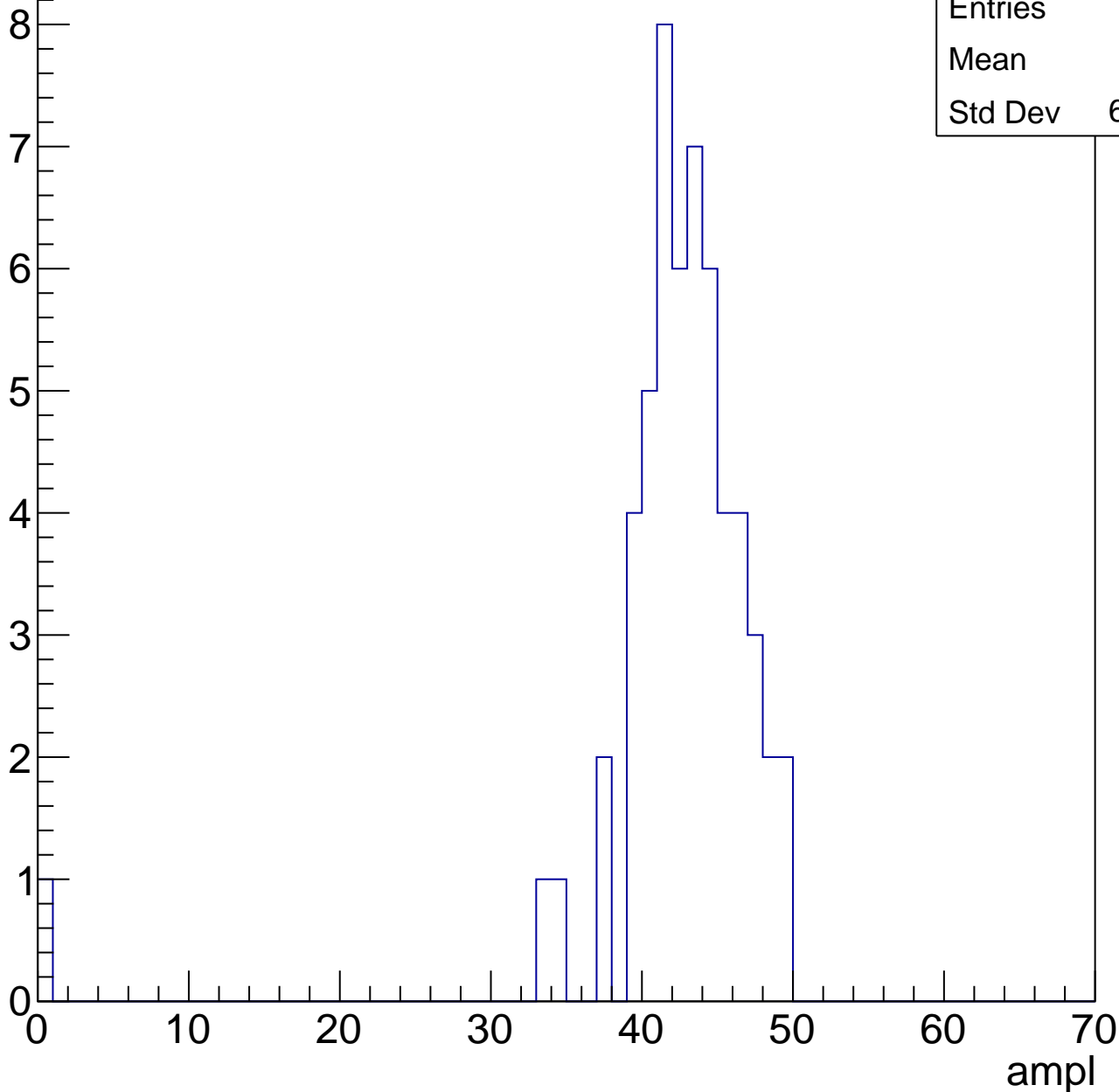


B1L103S, U5-ch83, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	41.8
Std Dev	6.542

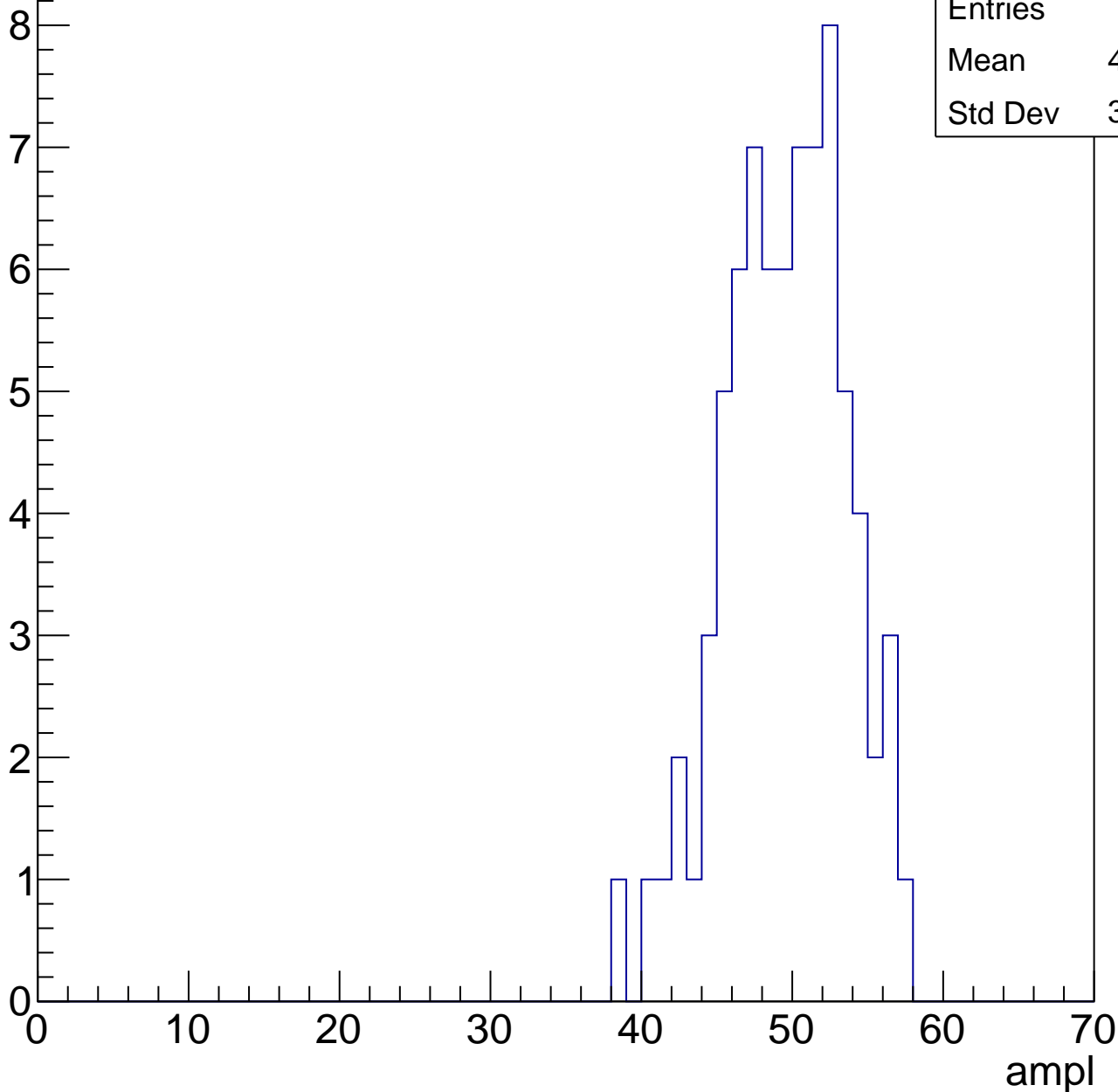


B1L103S, U5-ch83, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	49.07
Std Dev	3.995

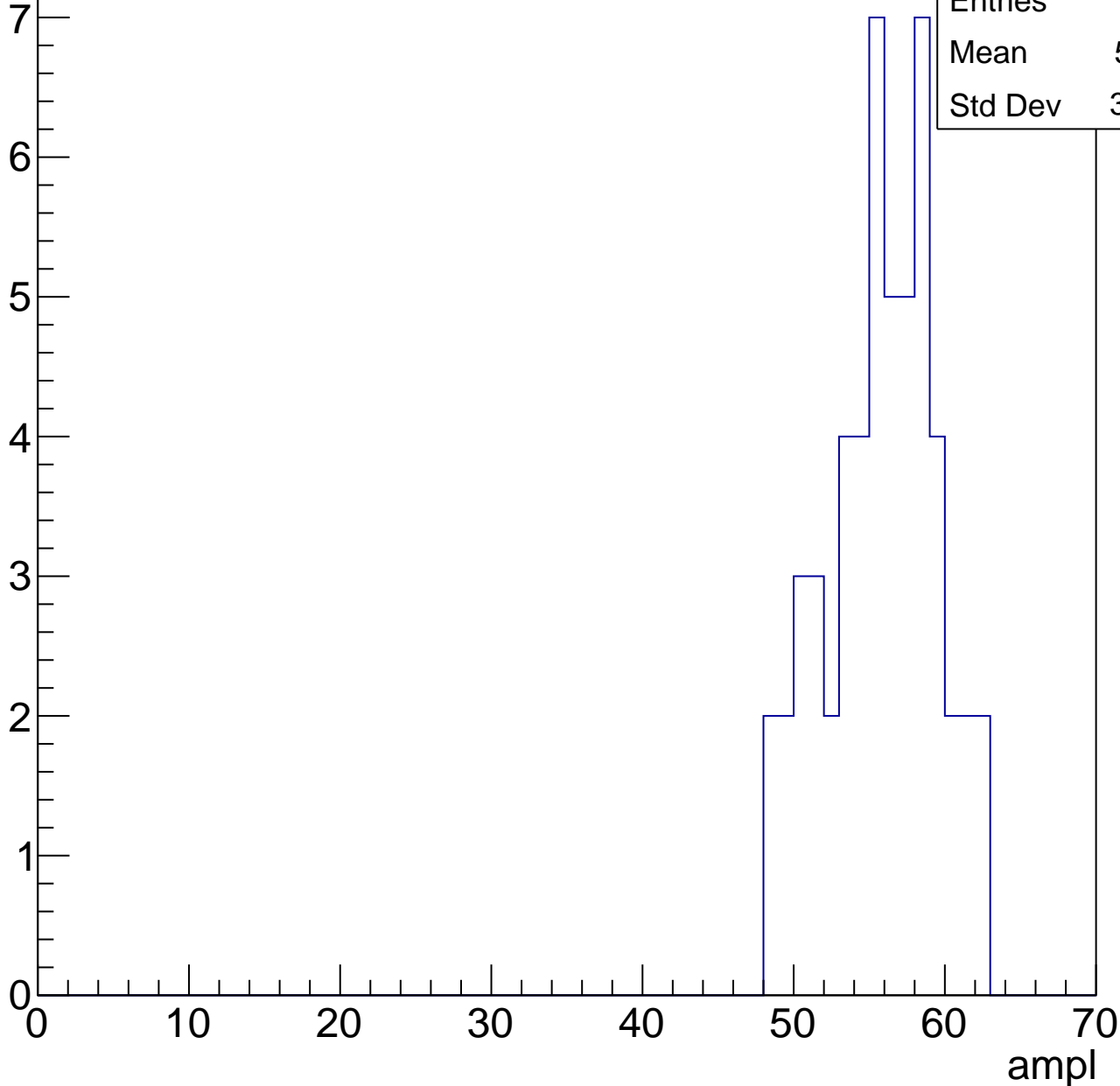


B1L103S, U5-ch83, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	55.31
Std Dev	3.594



B1L103S, U5-ch83, adc5

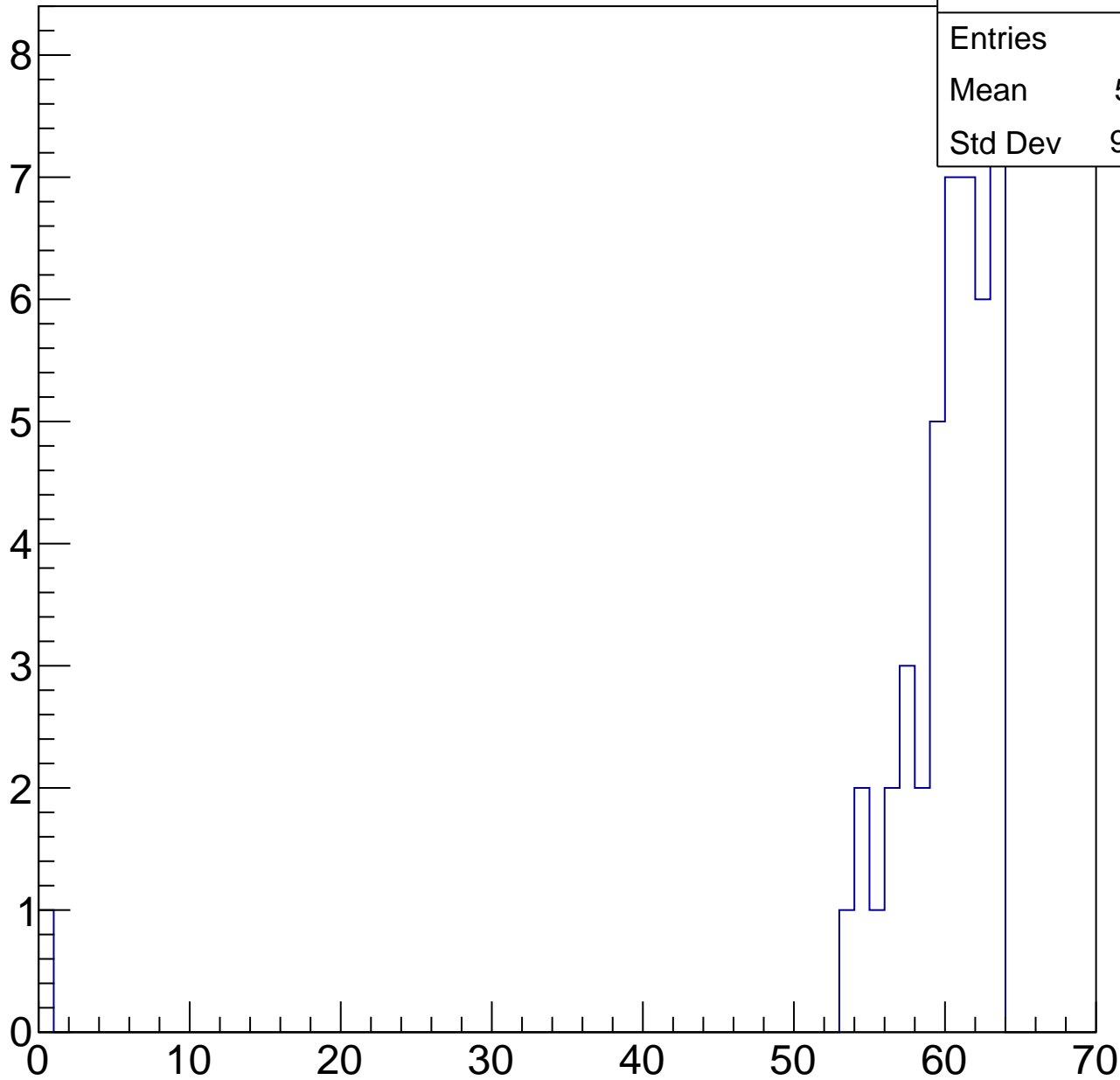
calib_packv5_041523_1651.root, FC#0, port C2

Entry

8
7
6
5
4
3
2
1
0

Entries	45
Mean	58.51
Std Dev	9.215

ampl



B1L103S, U5-ch83, adc6

calib_packv5_041523_1651.root, FC#0, port C2

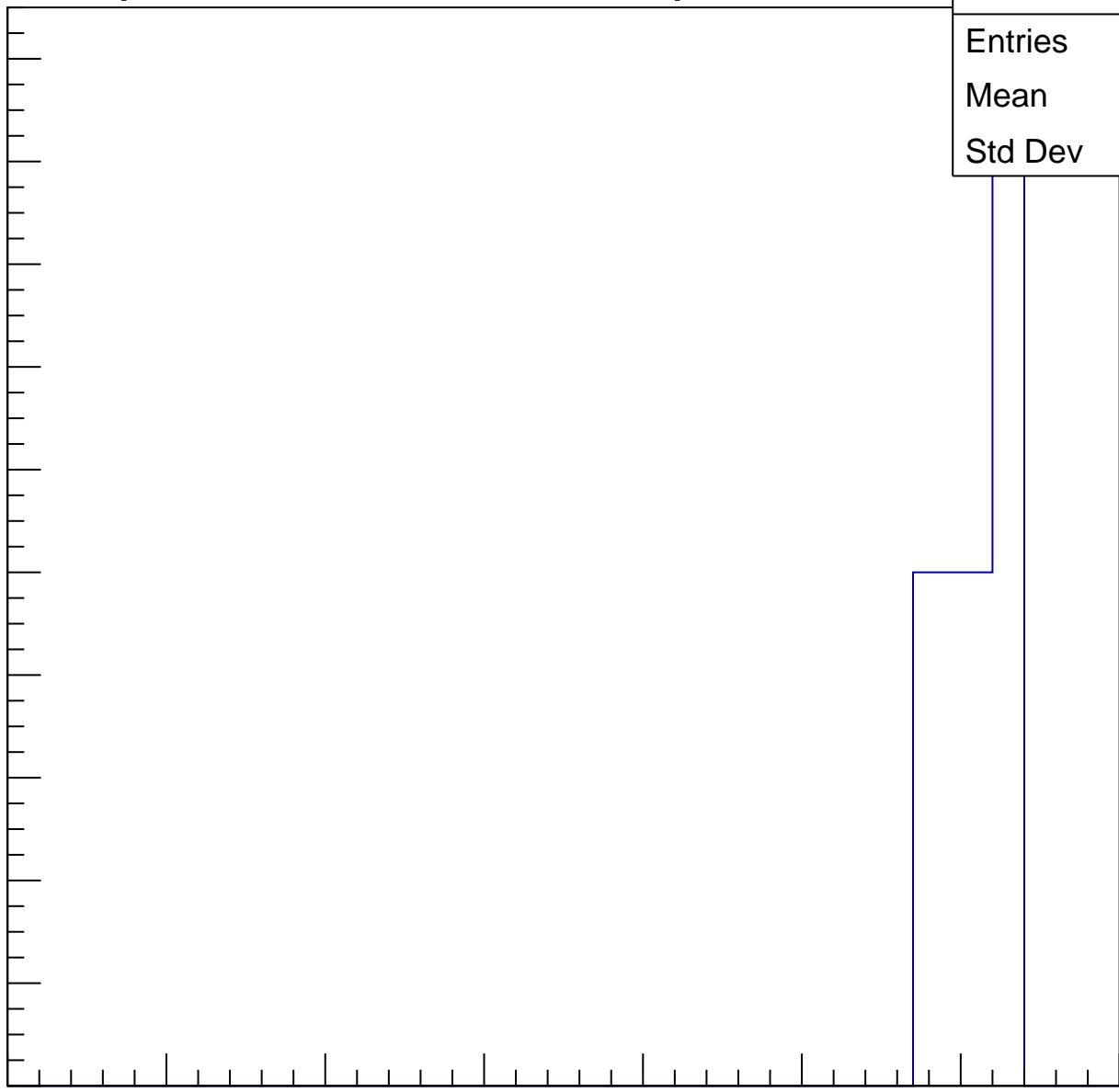
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	9
Mean	60.56
Std Dev	2.061

ampl

0 10 20 30 40 50 60 70



B1L103S, U5-ch83, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U5-ch84, adc0

calib_packv5_041523_1651.root, FC#0, port C2

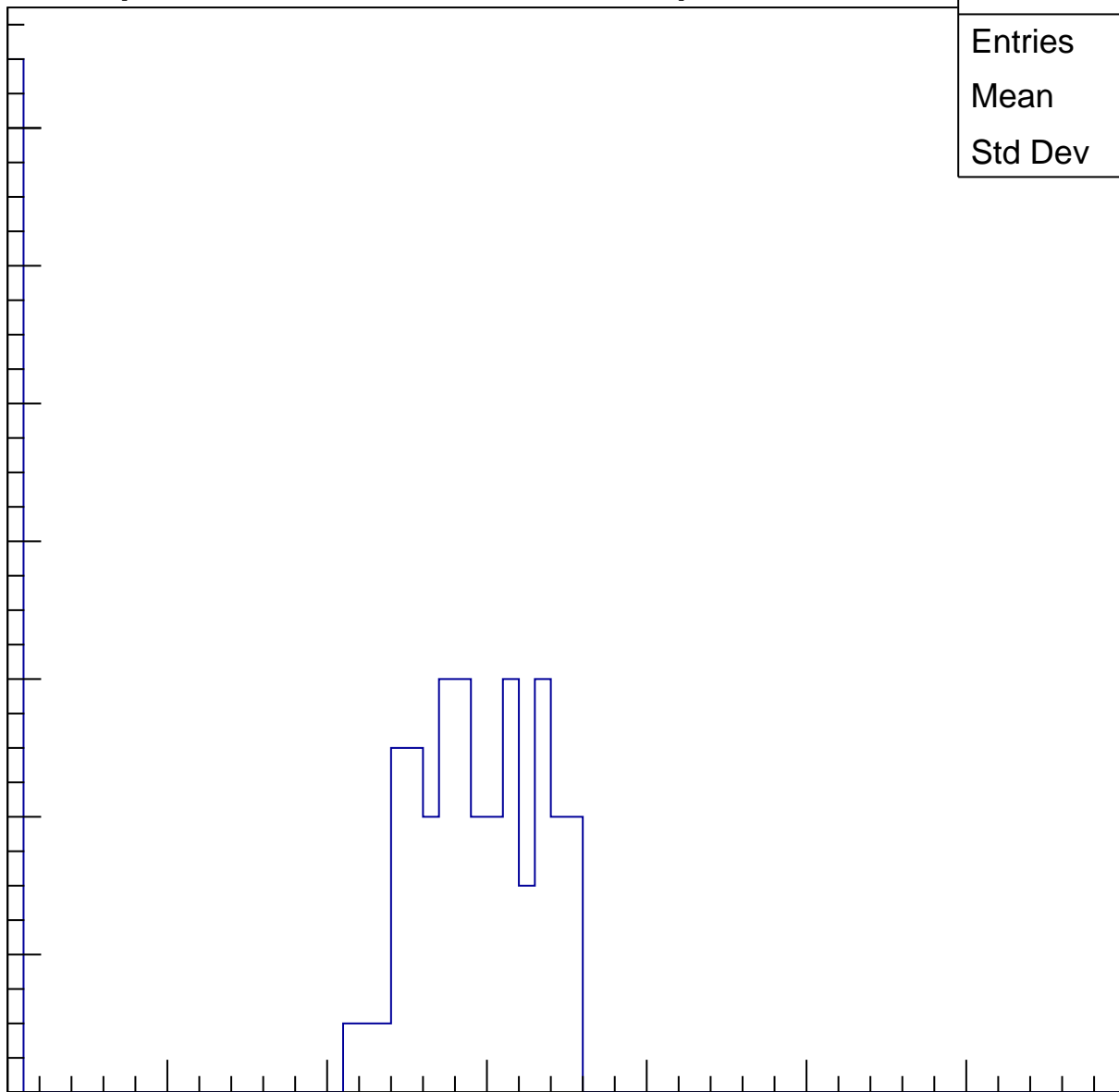
Entries	75
Mean	23.16
Std Dev	12.04

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

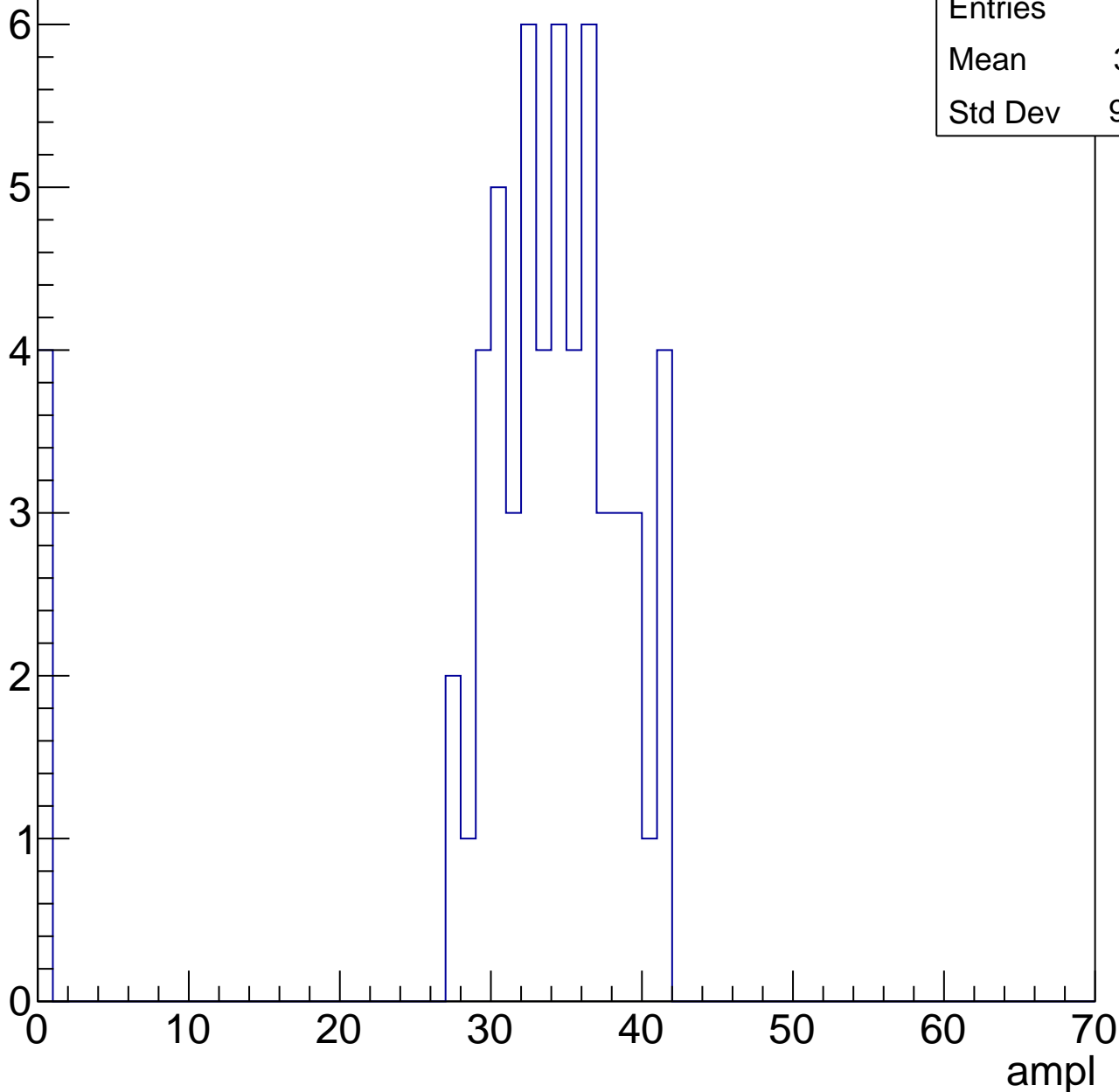


B1L103S, U5-ch84, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	31.71
Std Dev	9.292

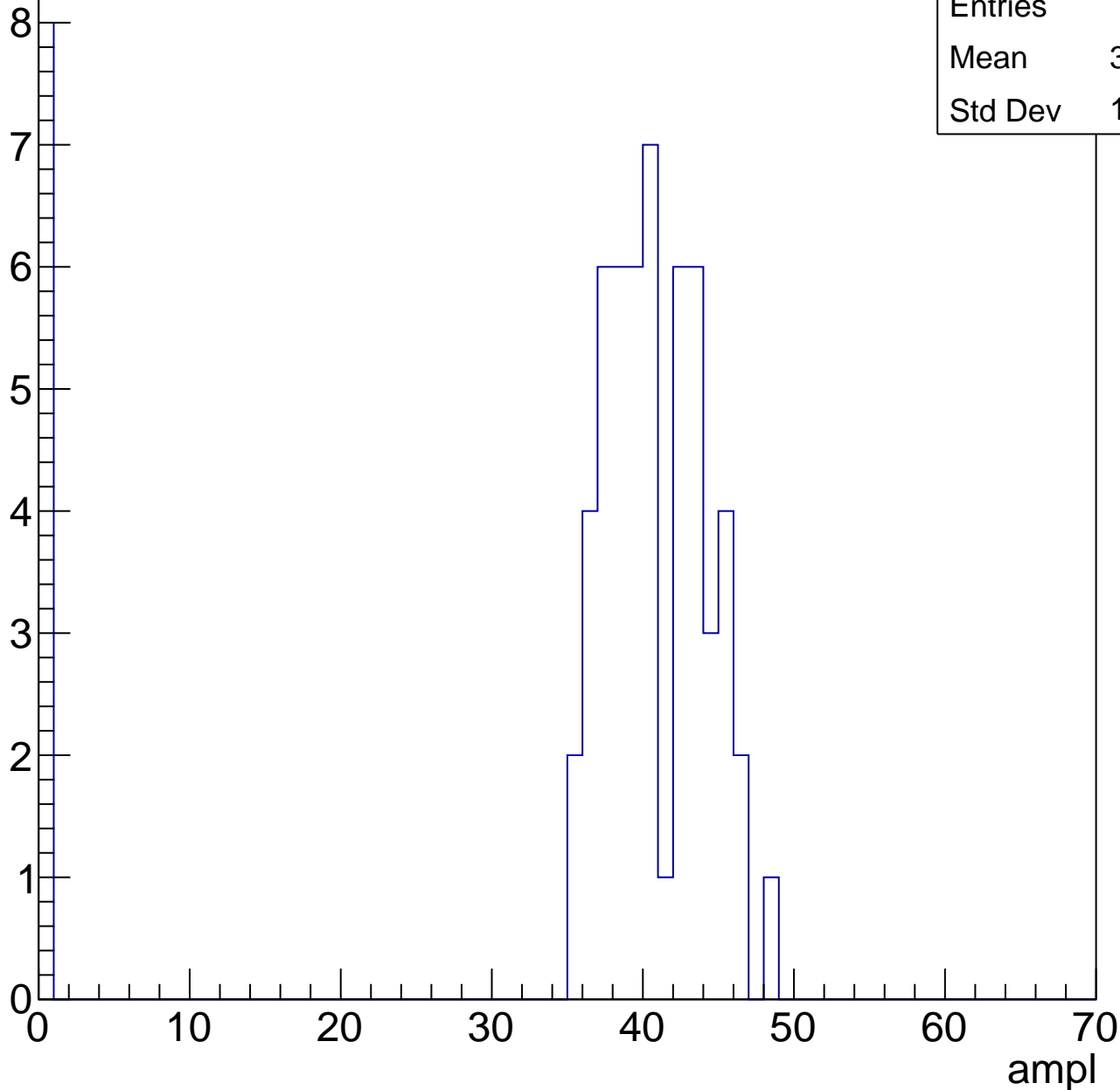


B1L103S, U5-ch84, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	35.18
Std Dev	13.87

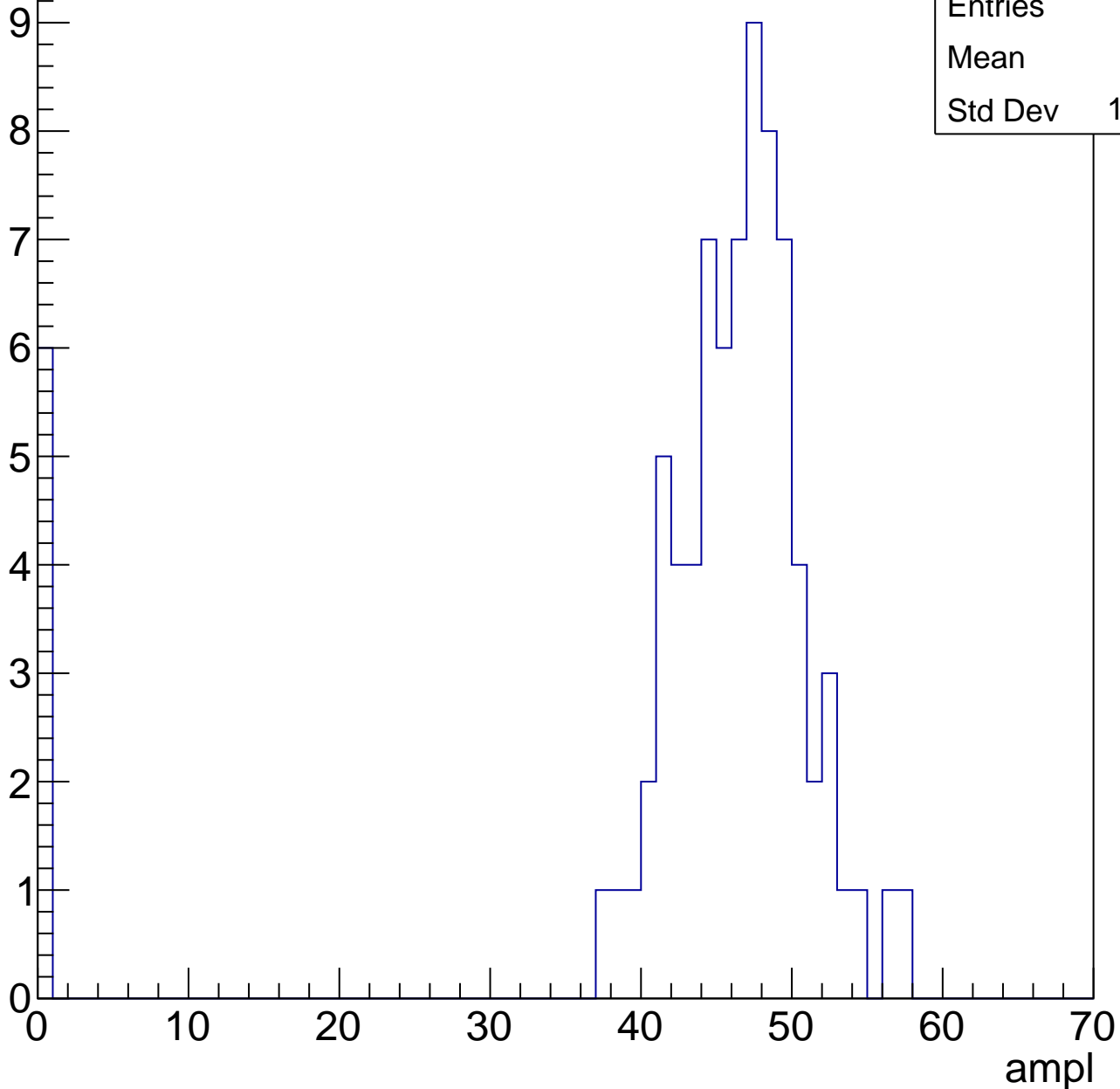


B1L103S, U5-ch84, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	81
Mean	42.8
Std Dev	12.69

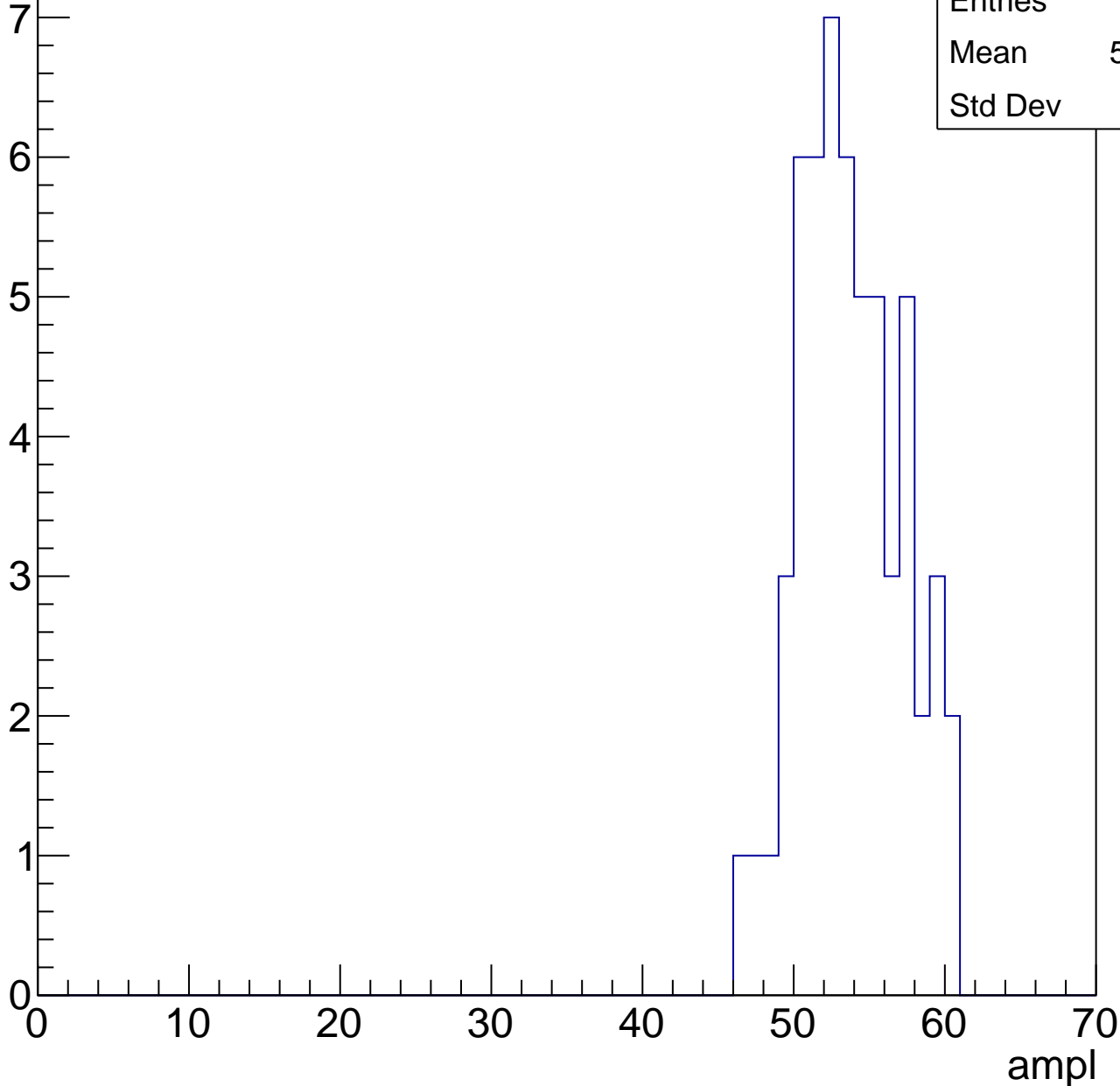


B1L103S, U5-ch84, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	53.34
Std Dev	3.34

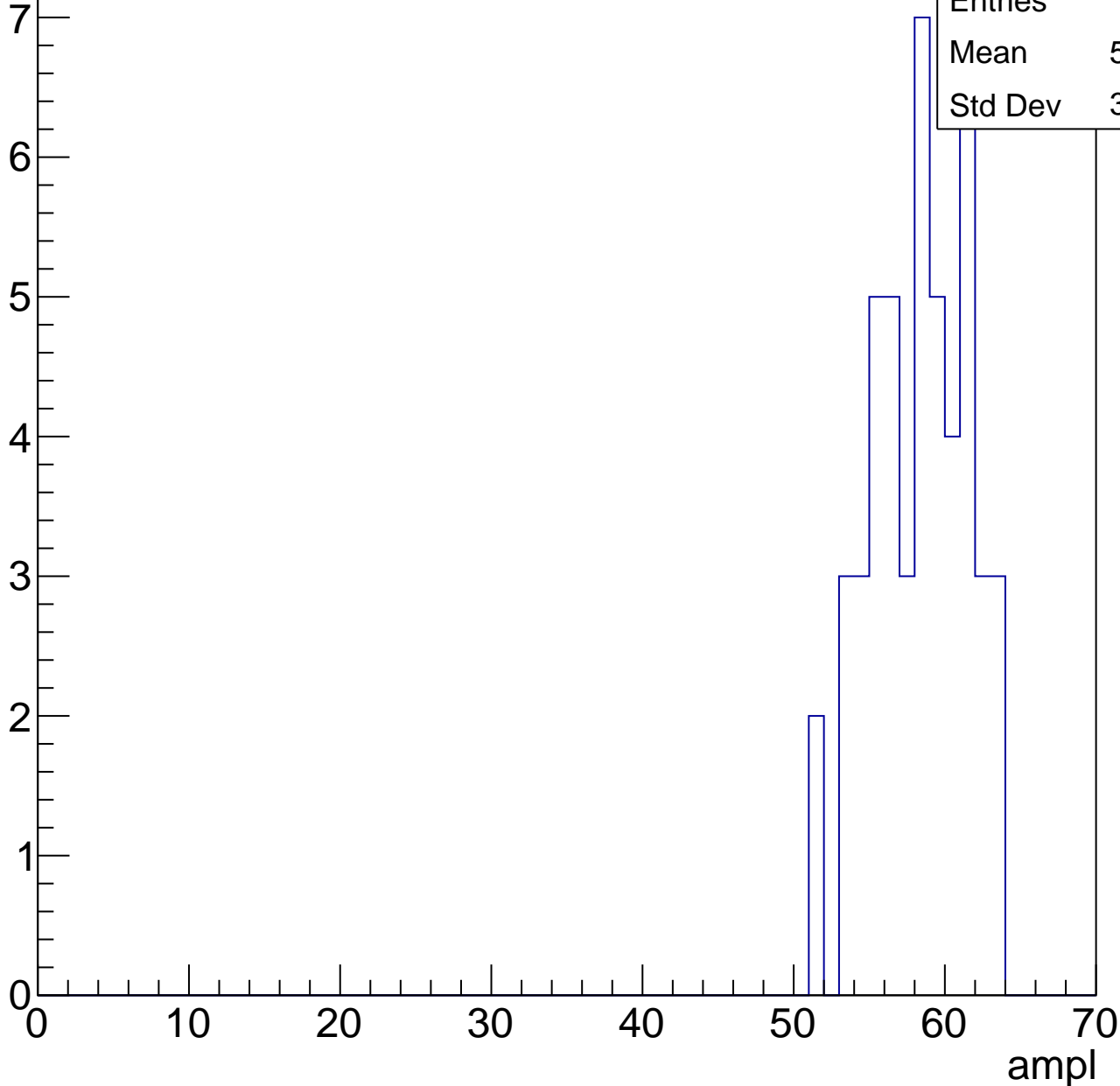


B1L103S, U5-ch84, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	57.84
Std Dev	3.146

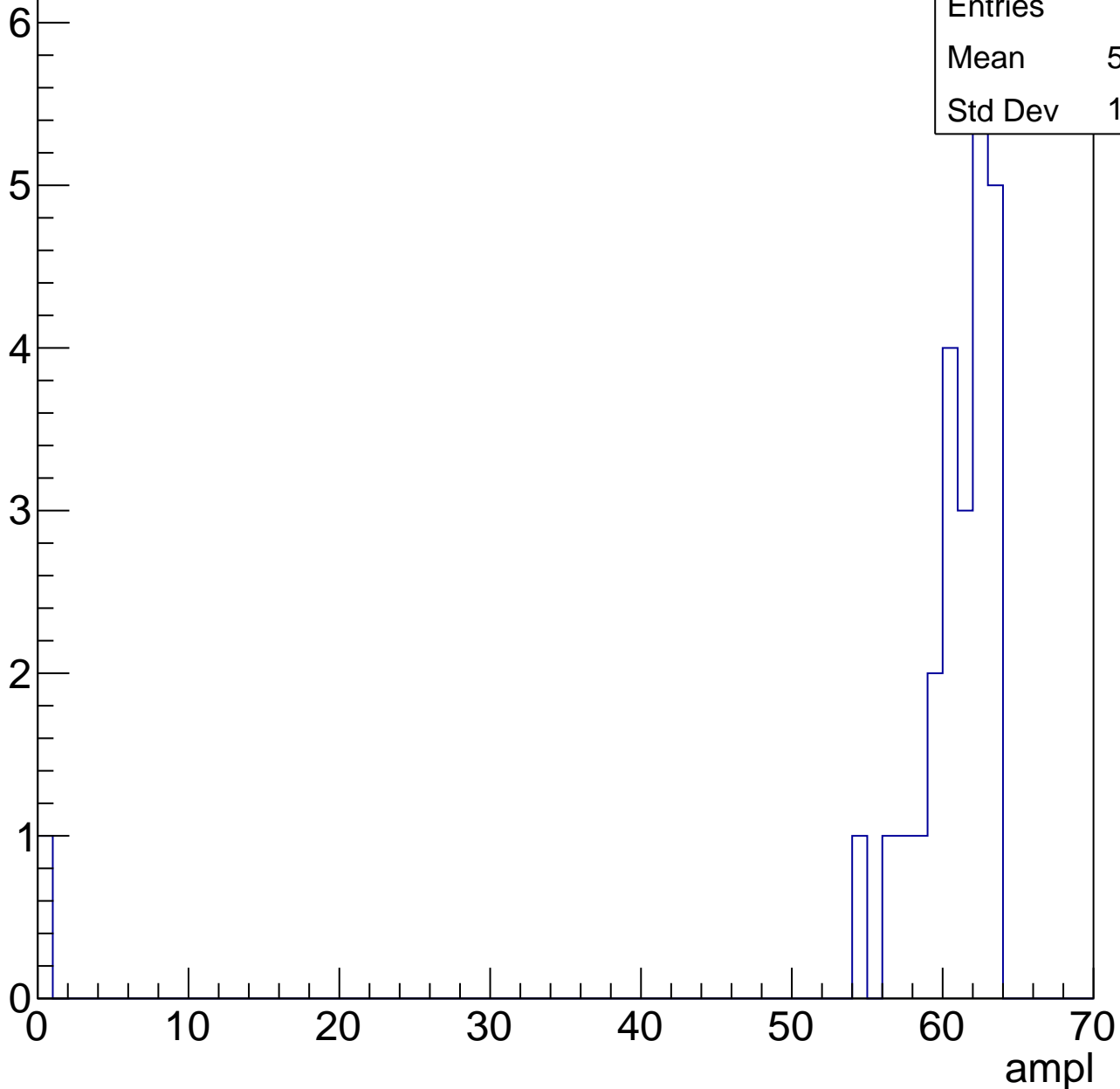


B1L103S, U5-ch84, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	25
Mean	58.12
Std Dev	12.08



B1L103S, U5-ch84, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	22
Mean	8.545
Std Dev	21.51

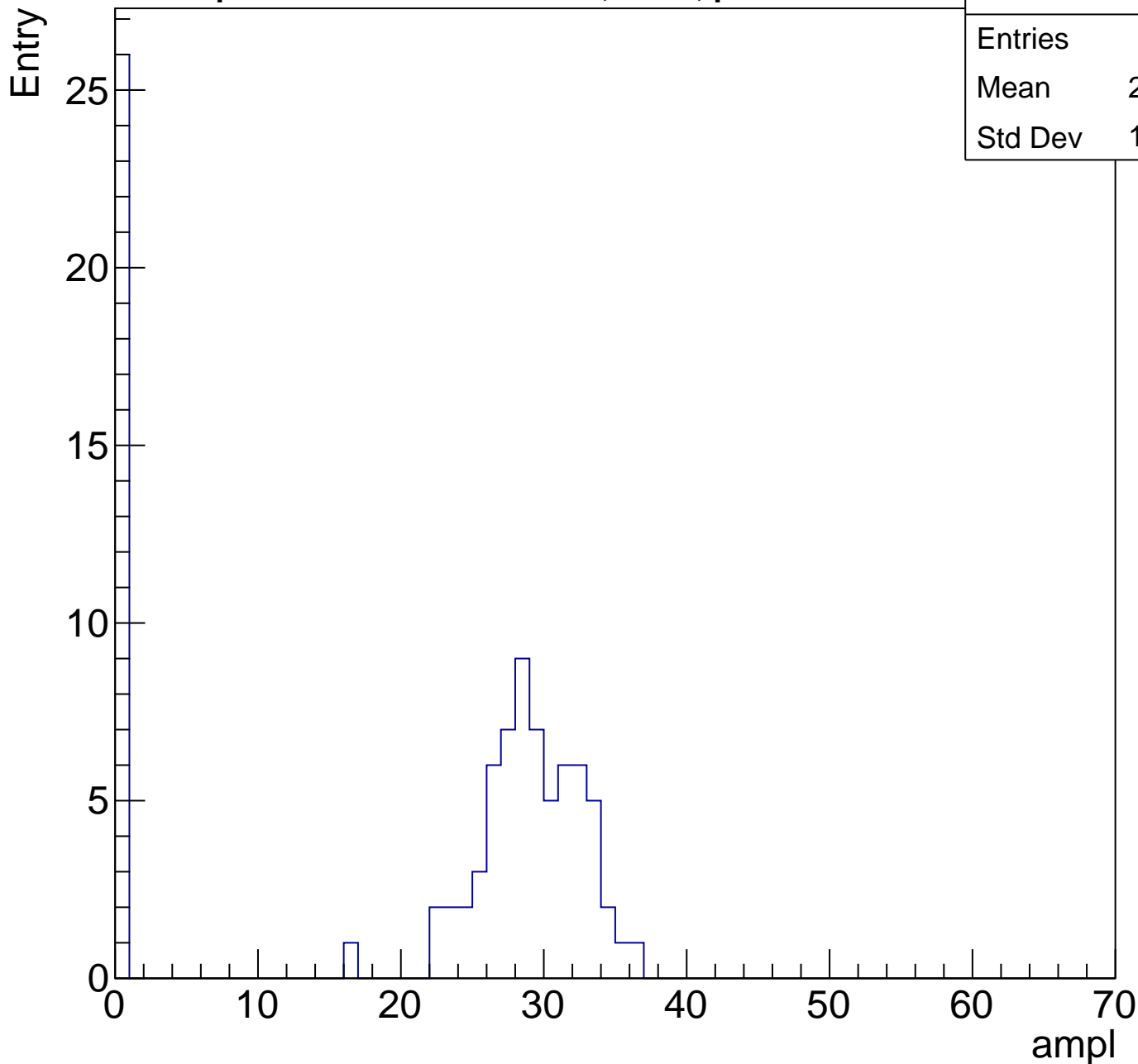
Entry



B1L103S, U5-ch85, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	91
Mean	20.45
Std Dev	13.28

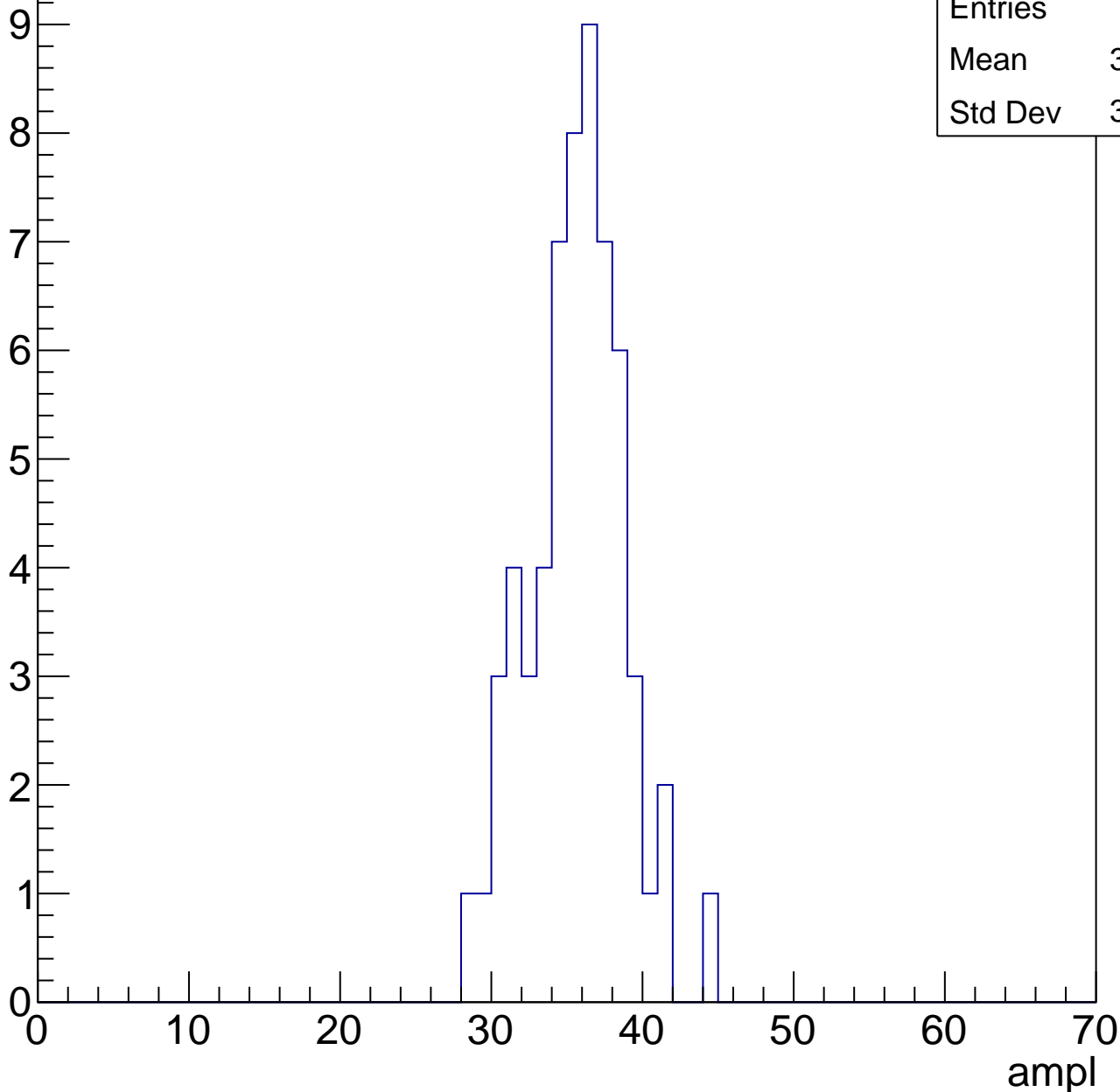


B1L103S, U5-ch85, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	35.18
Std Dev	3.133

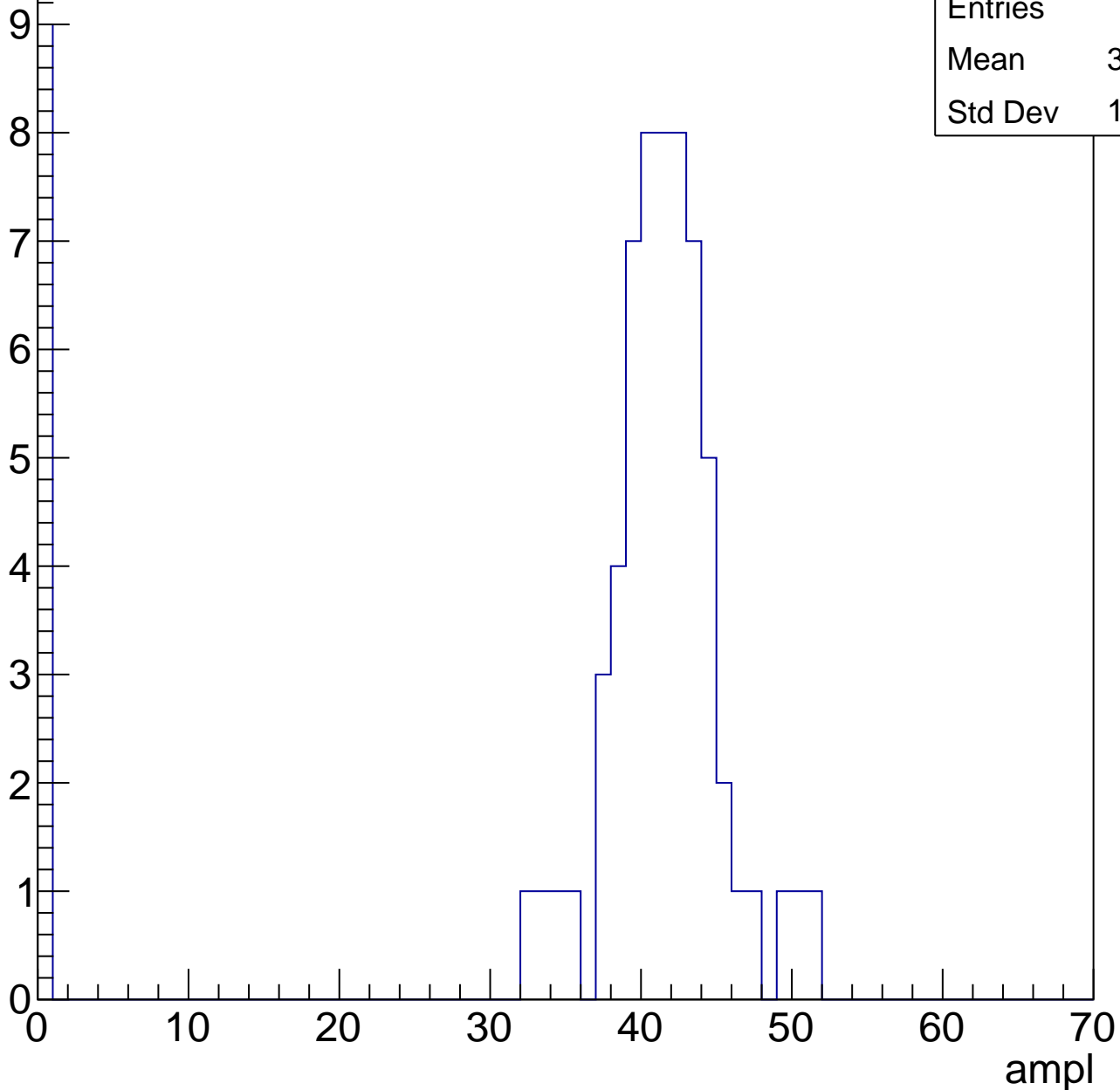


B1L103S, U5-ch85, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

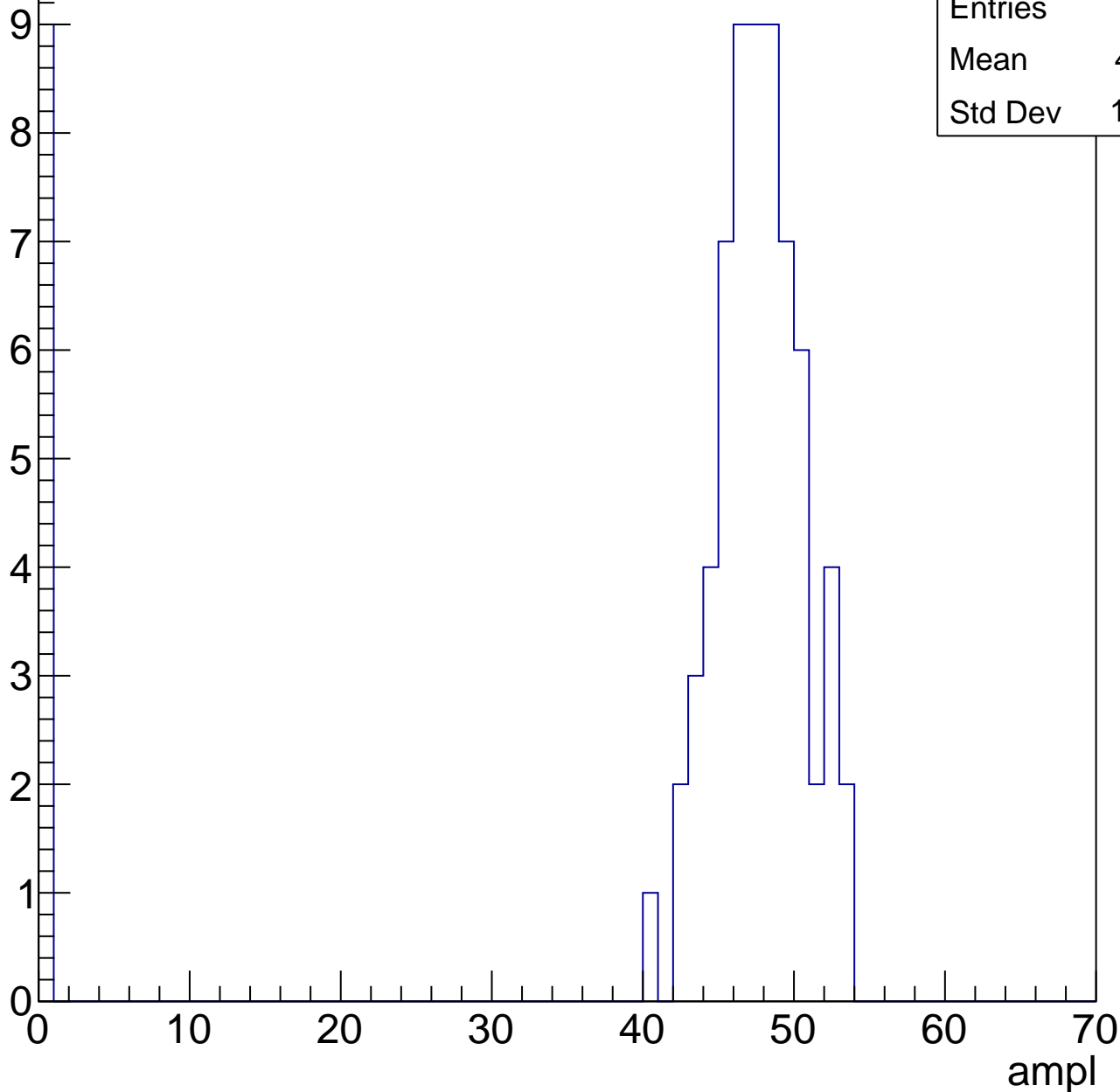
Entries	70
Mean	35.83
Std Dev	14.16



B1L103S, U5-ch85, adc3

calib_packv5_041523_1651.root, FC#0, port C2

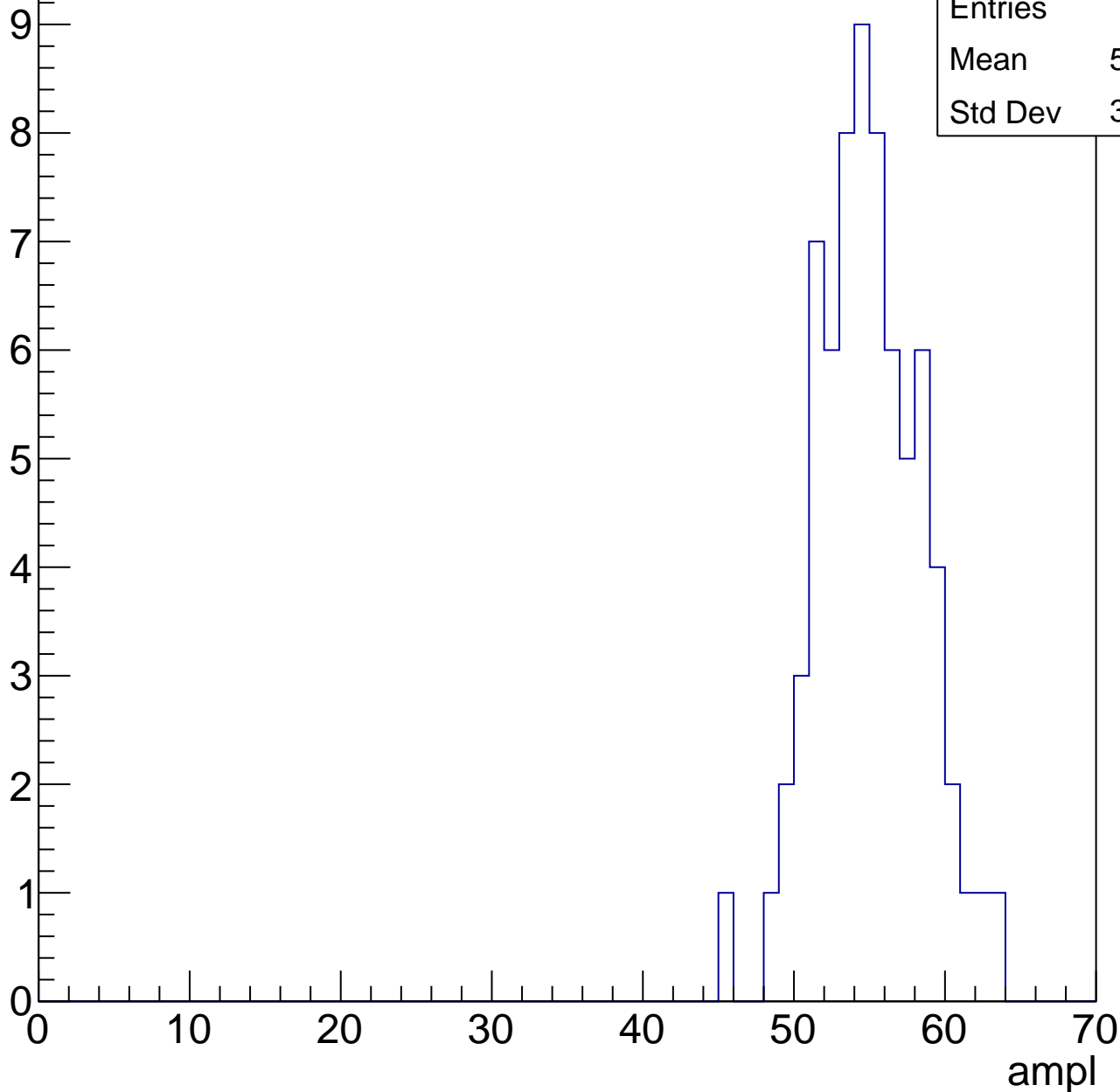
Entry



B1L103S, U5-ch85, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



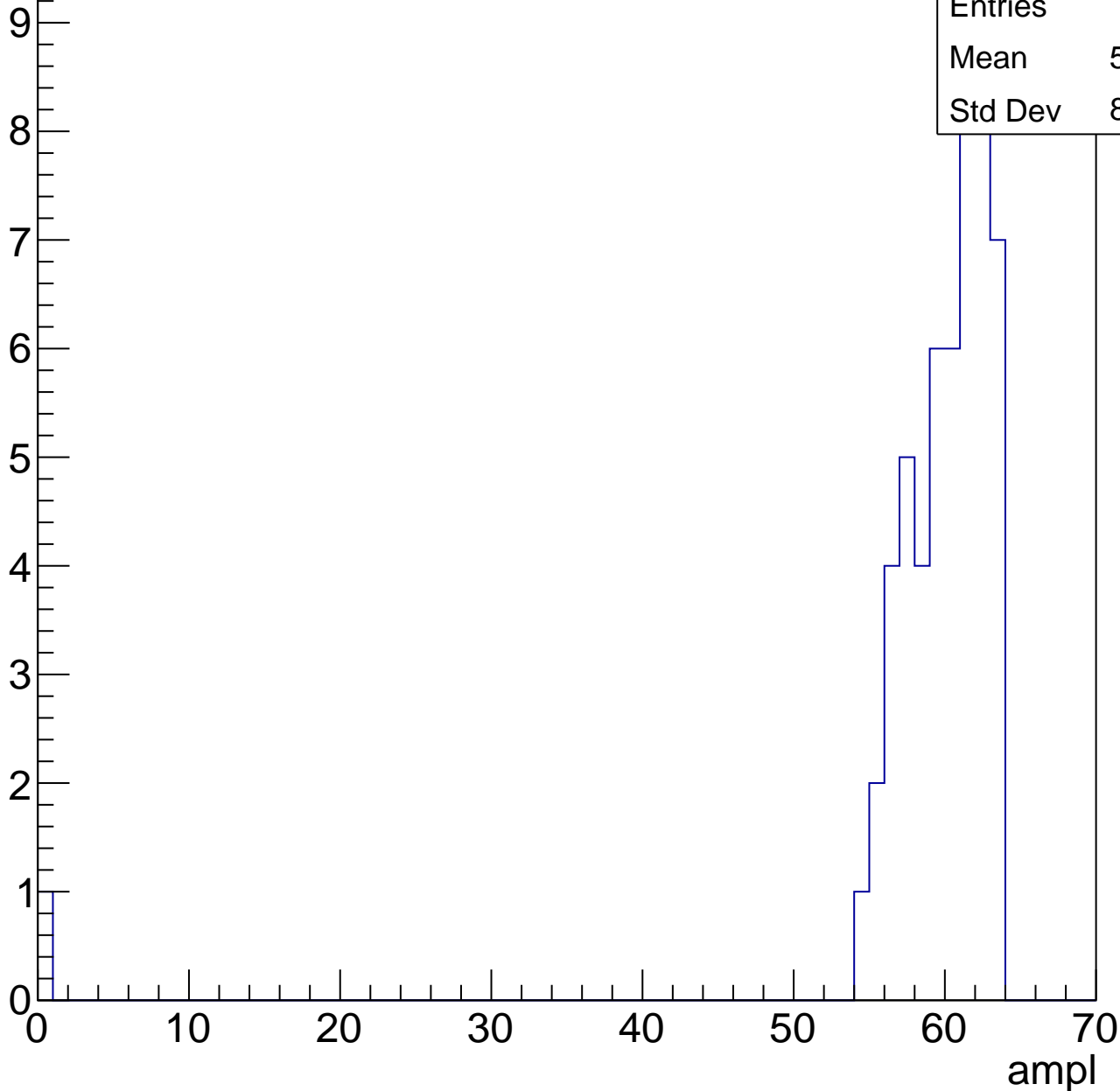
Entries	71
Mean	54.52
Std Dev	3.419

B1L103S, U5-ch85, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	58.58
Std Dev	8.484



B1L103S, U5-ch85, adc6

calib_packv5_041523_1651.root, FC#0, port C2

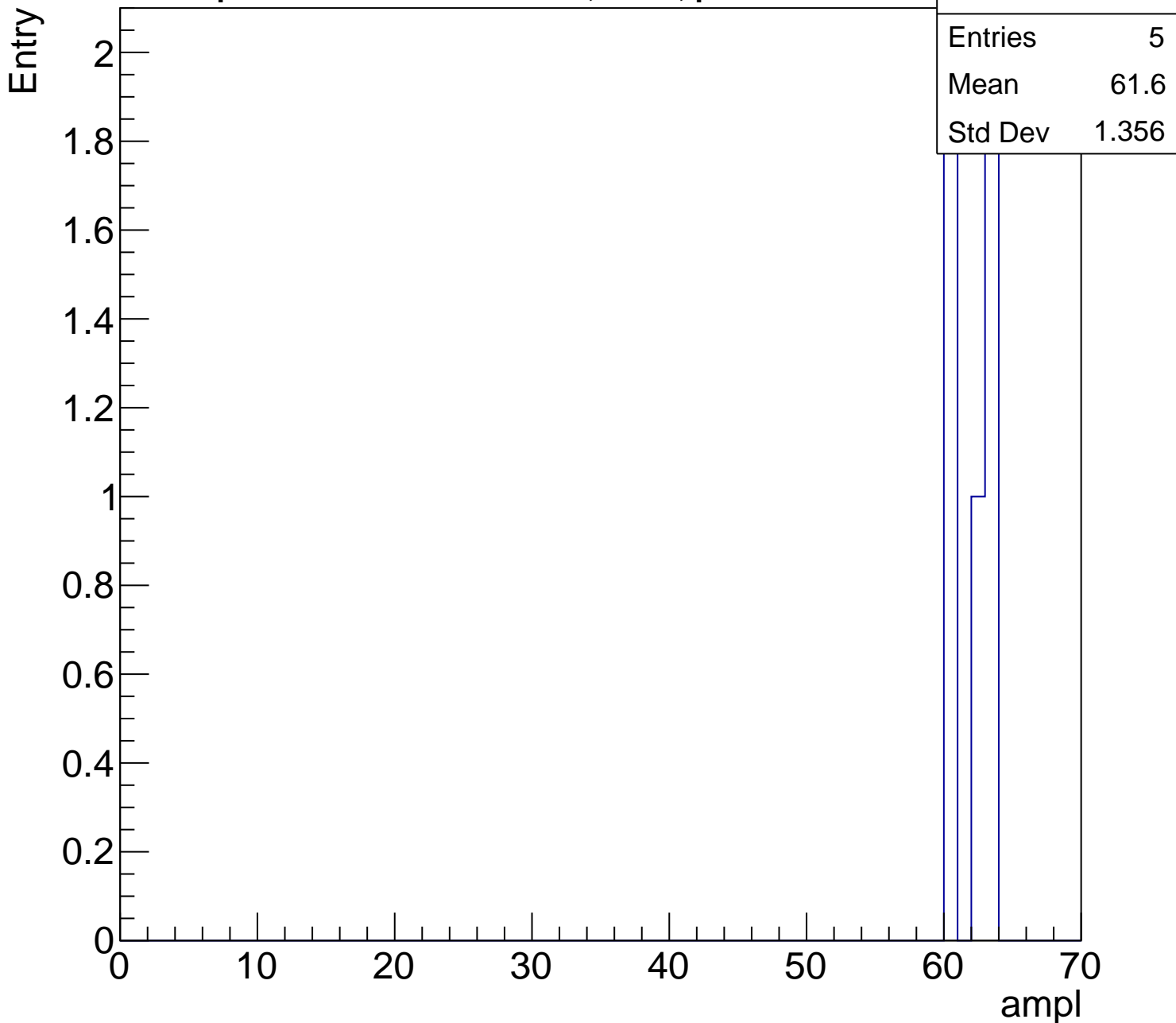
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	5
Mean	61.6
Std Dev	1.356

0 10 20 30 40 50 60 70

ampl



B1L103S, U5-ch85, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch86, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	66
Mean	23.98
Std Dev	11.28

Entry

10

8

6

4

2

0

0

10

20

30

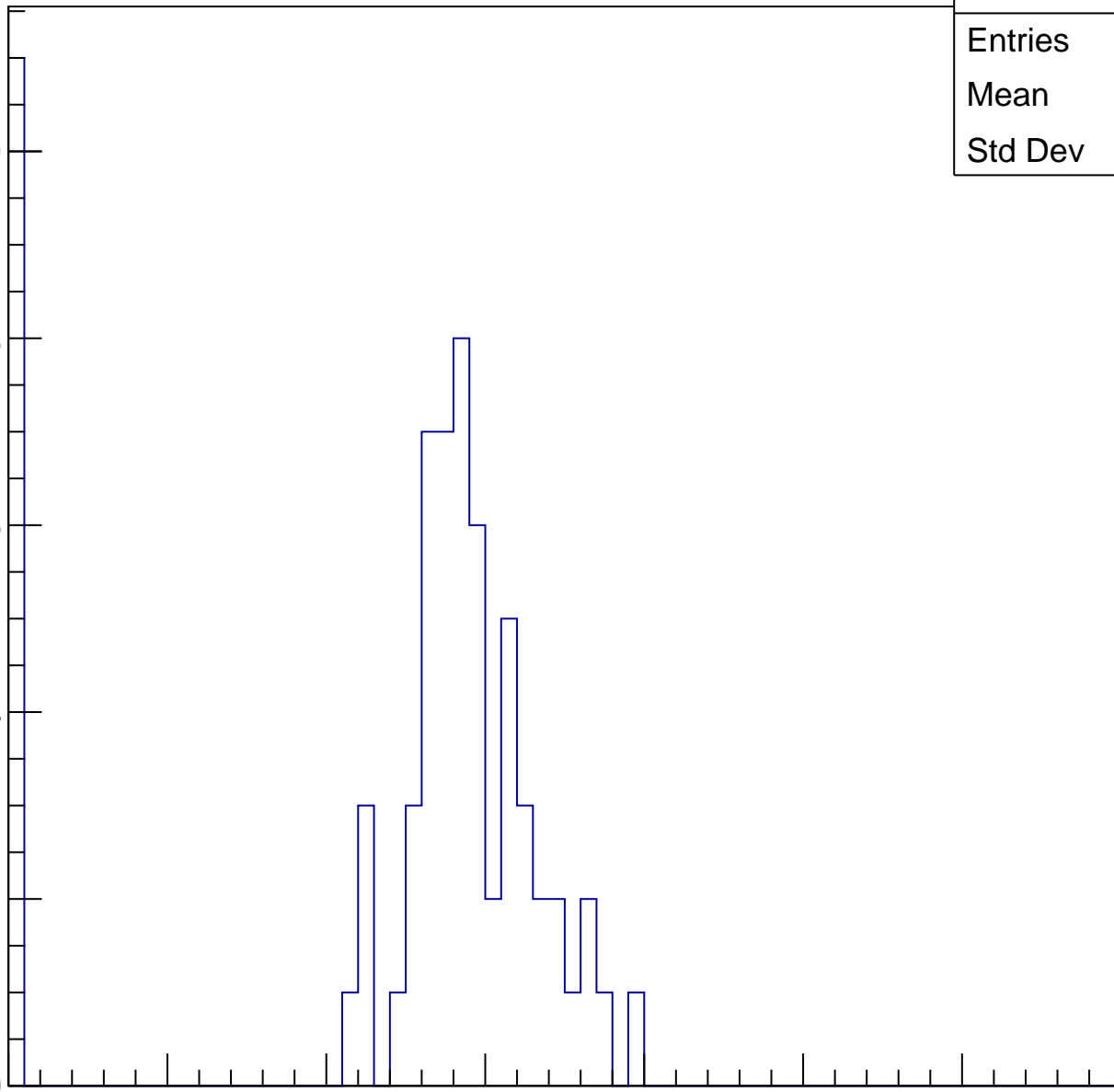
40

50

60

70

ampl

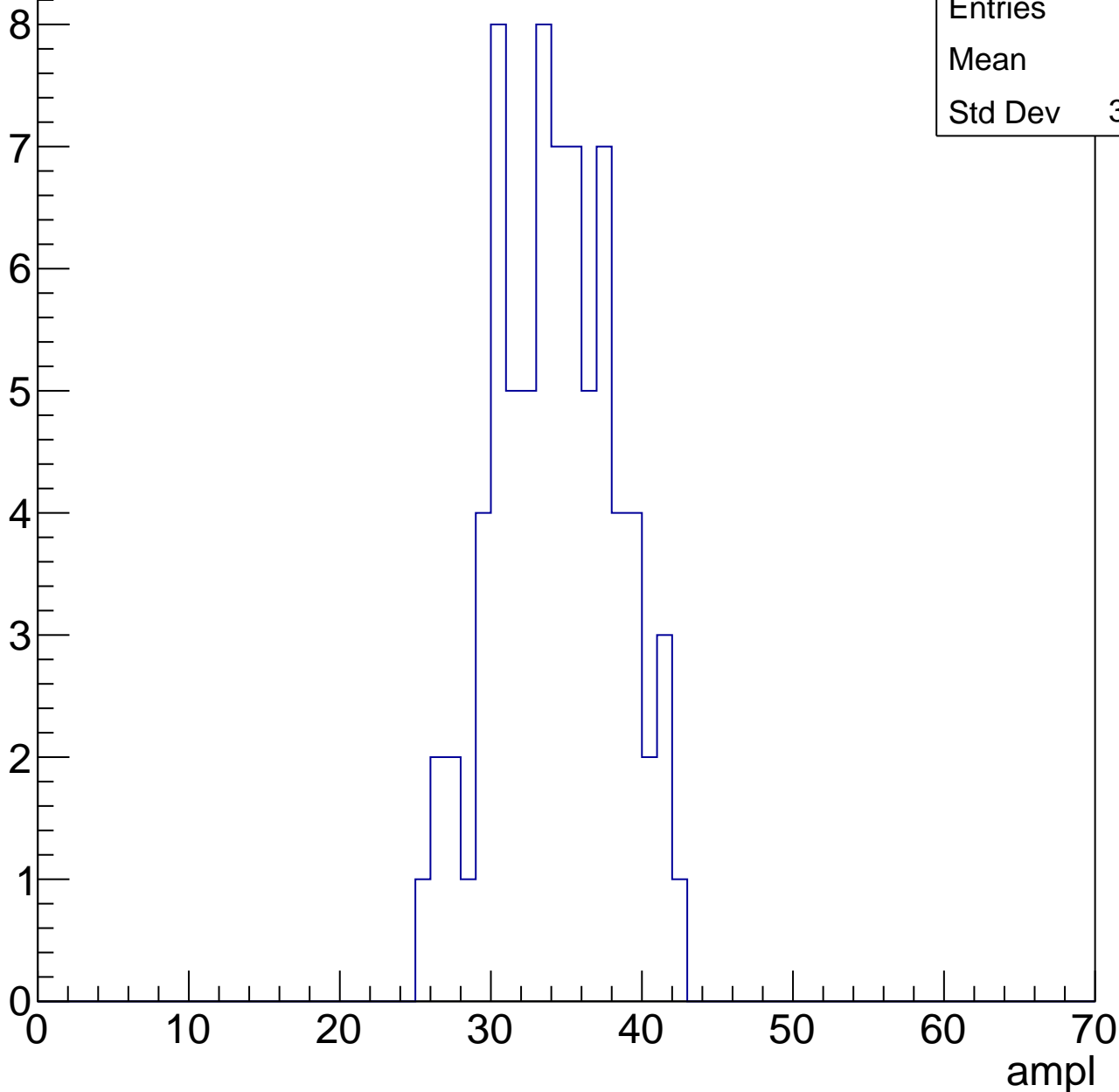


B1L103S, U5-ch86, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	33.8
Std Dev	3.937

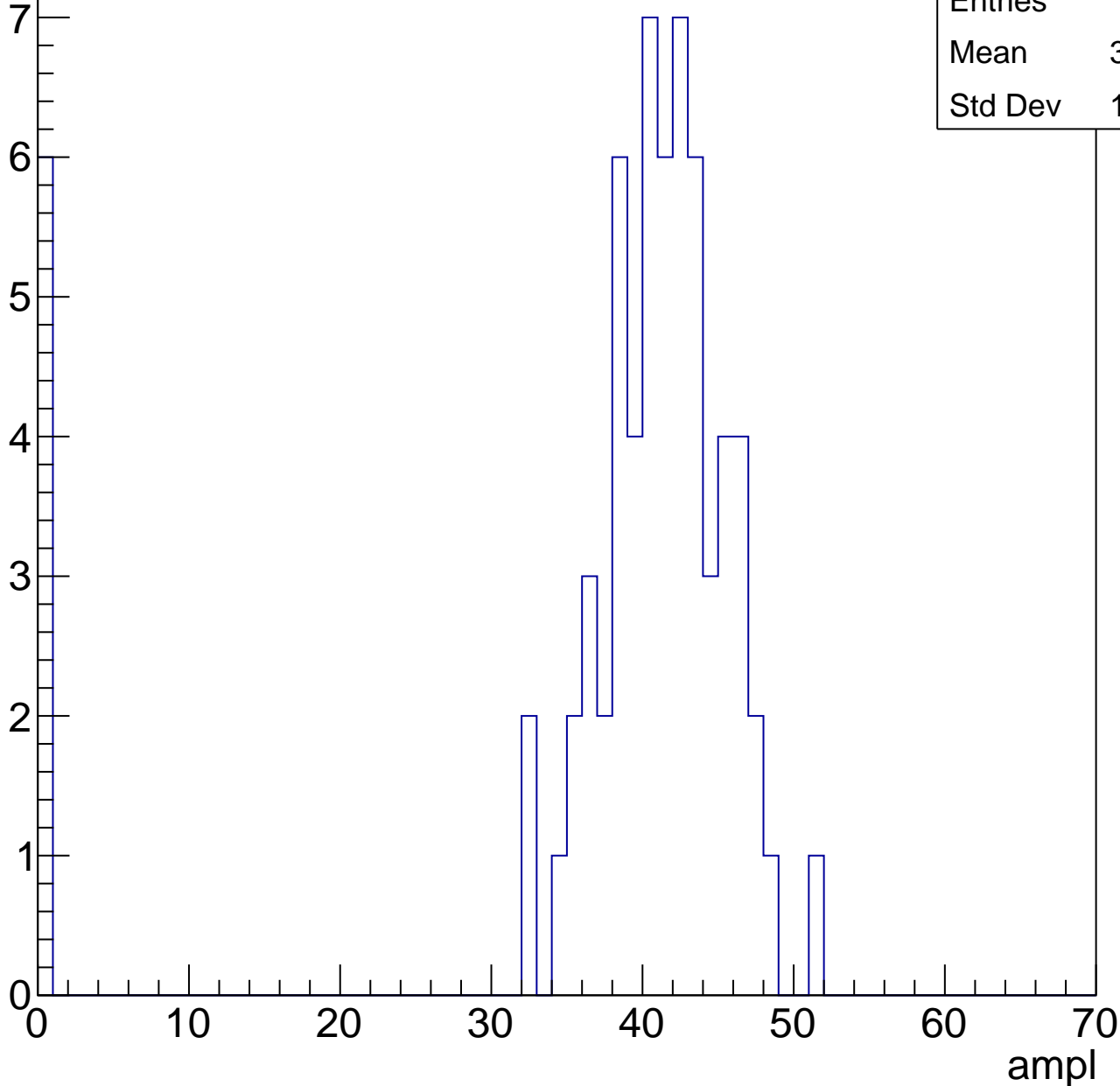


B1L103S, U5-ch86, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

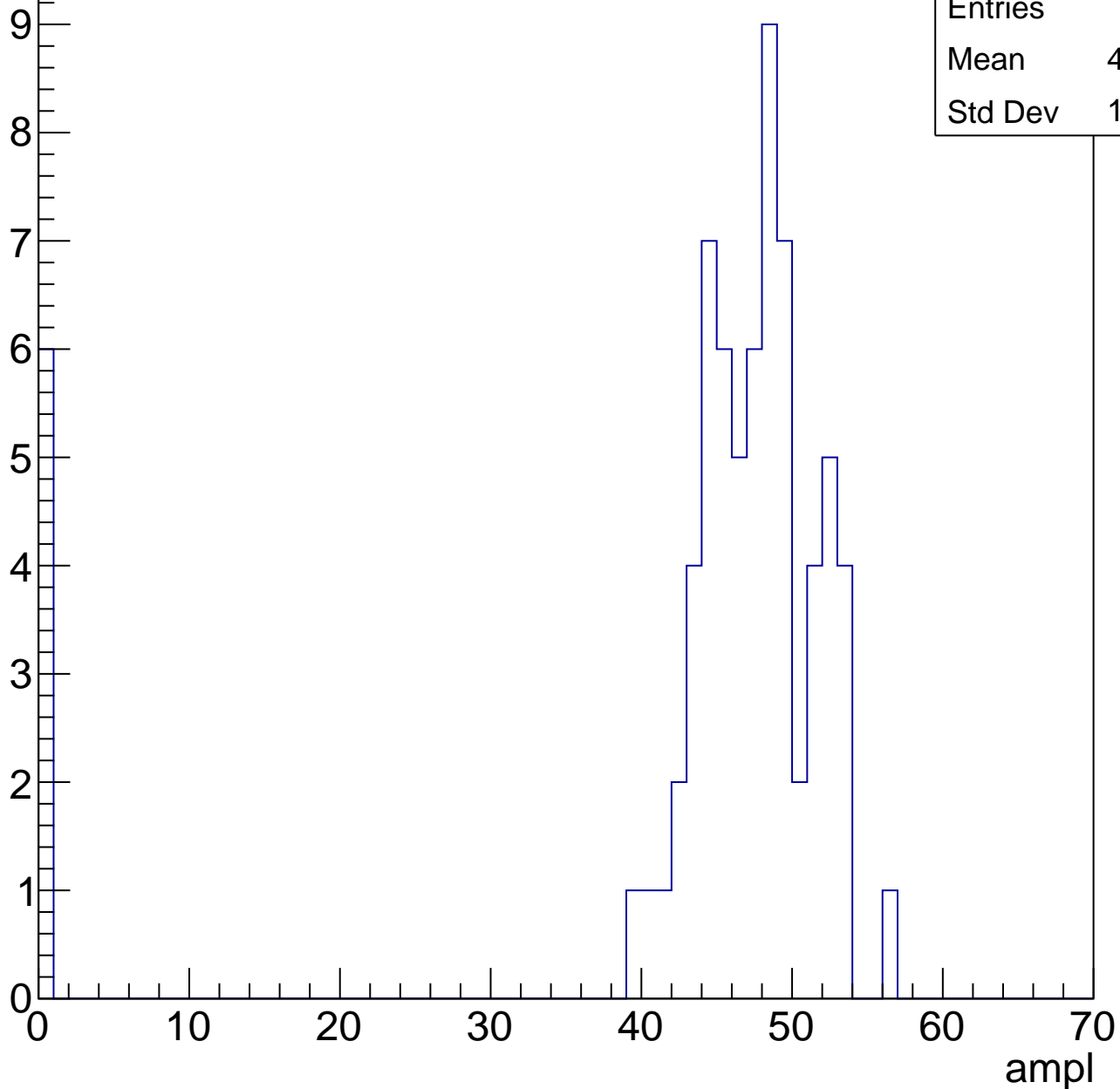
Entries	67
Mean	37.33
Std Dev	12.27



B1L103S, U5-ch86, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

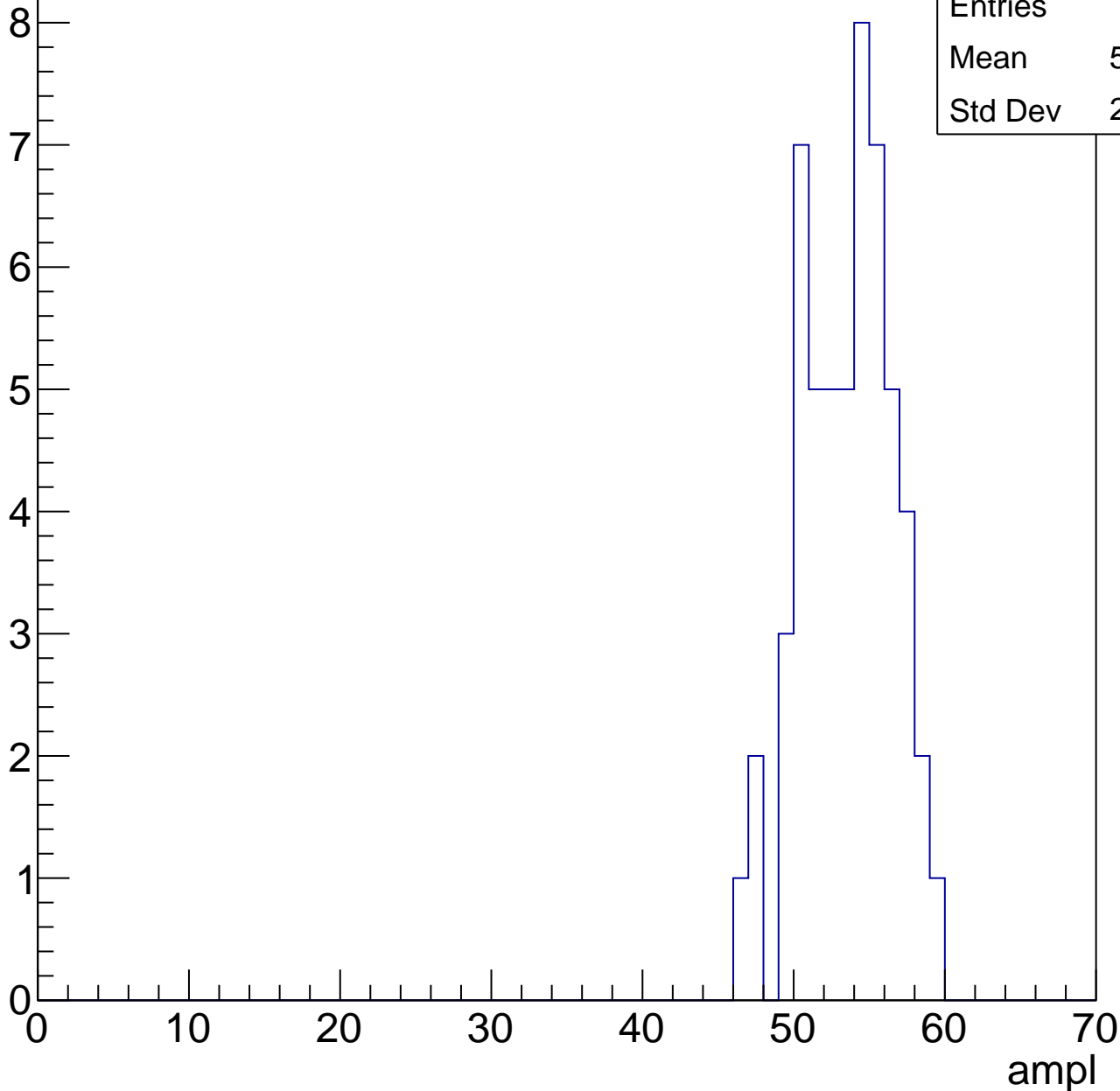


B1L103S, U5-ch86, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

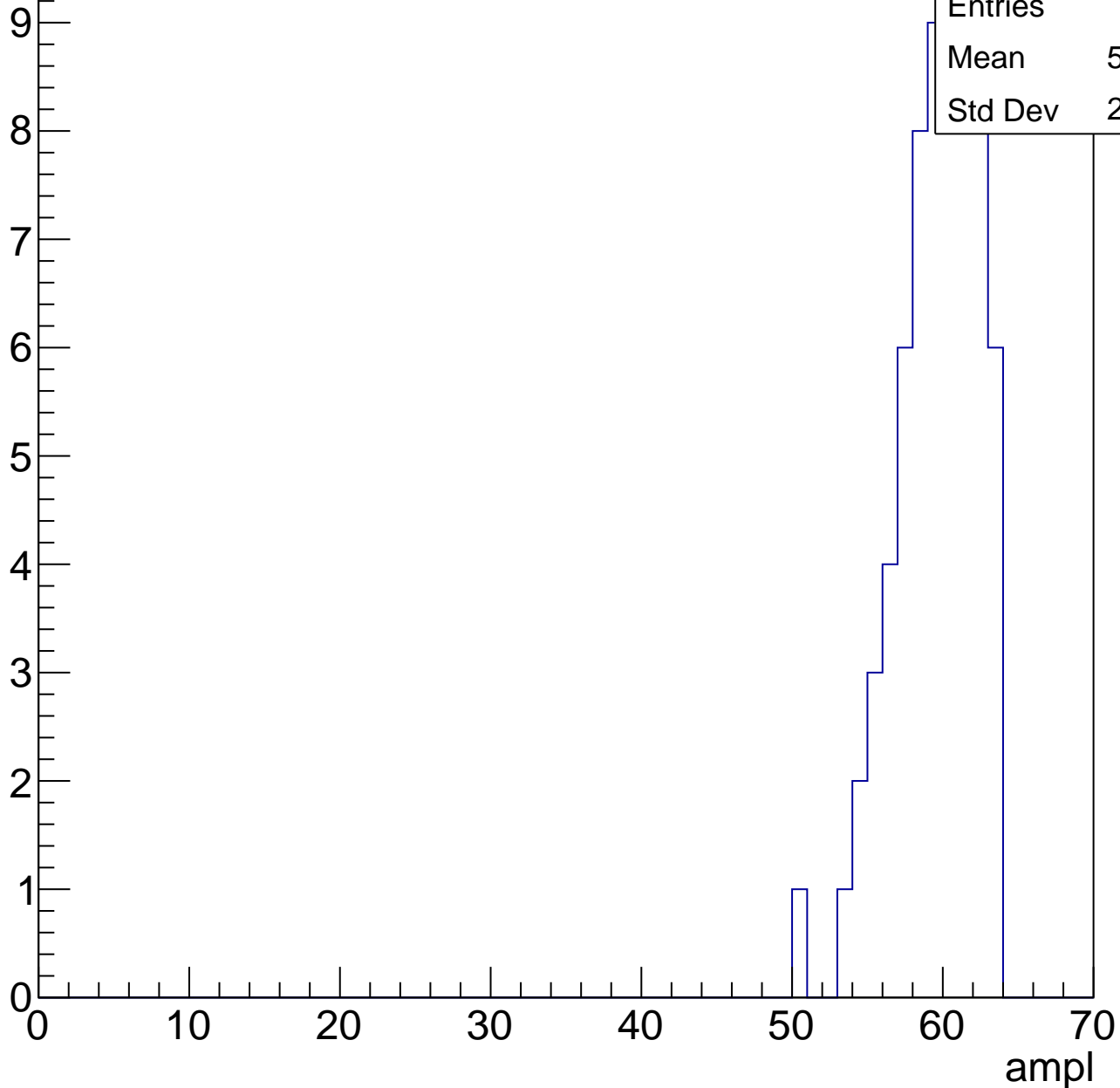
Entries	55
Mean	53.04
Std Dev	2.978



B1L103S, U5-ch86, adc5

calib_packv5_041523_1651.root, FC#0, port C2

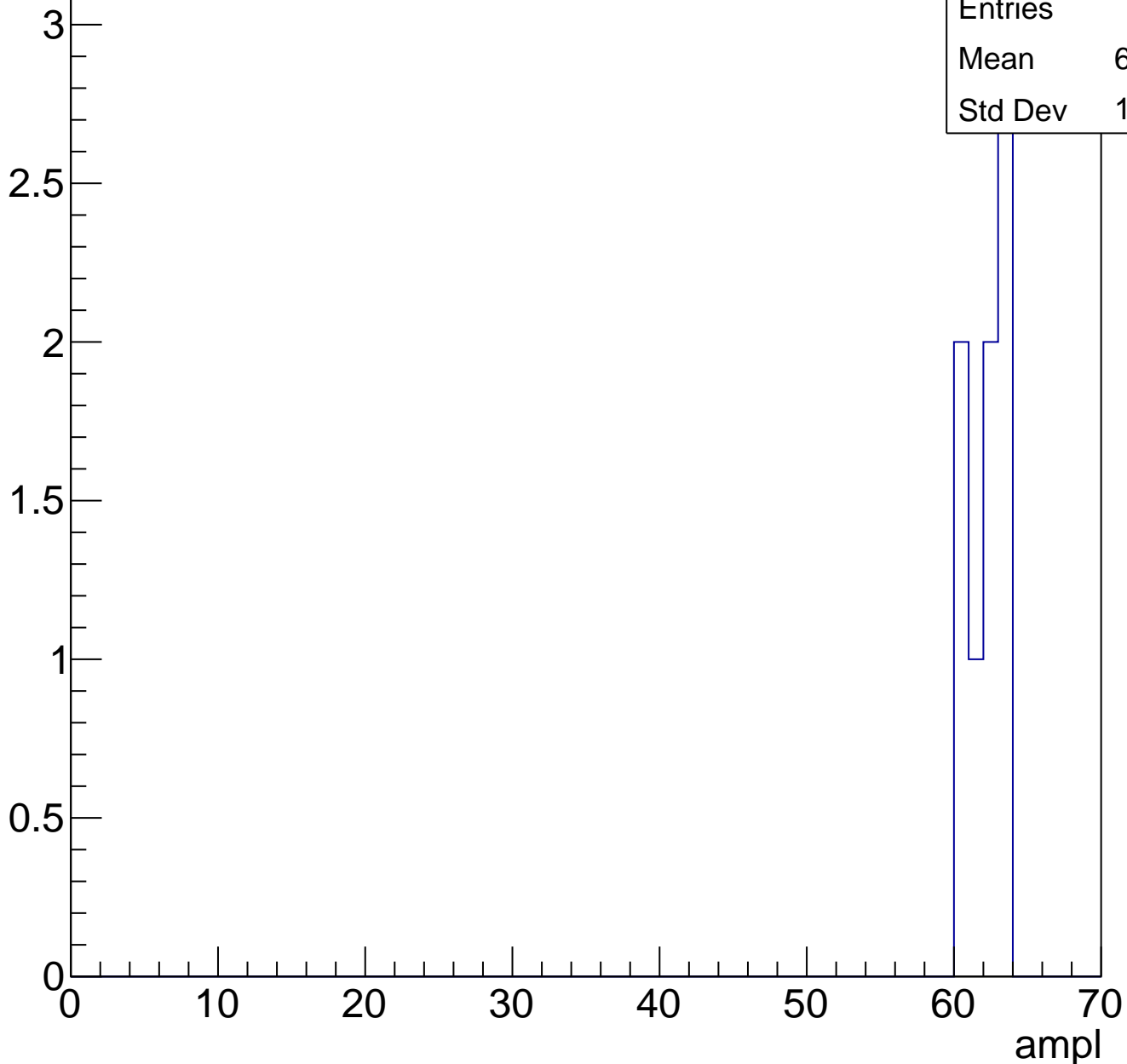
Entry



B1L103S, U5-ch86, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch86, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry

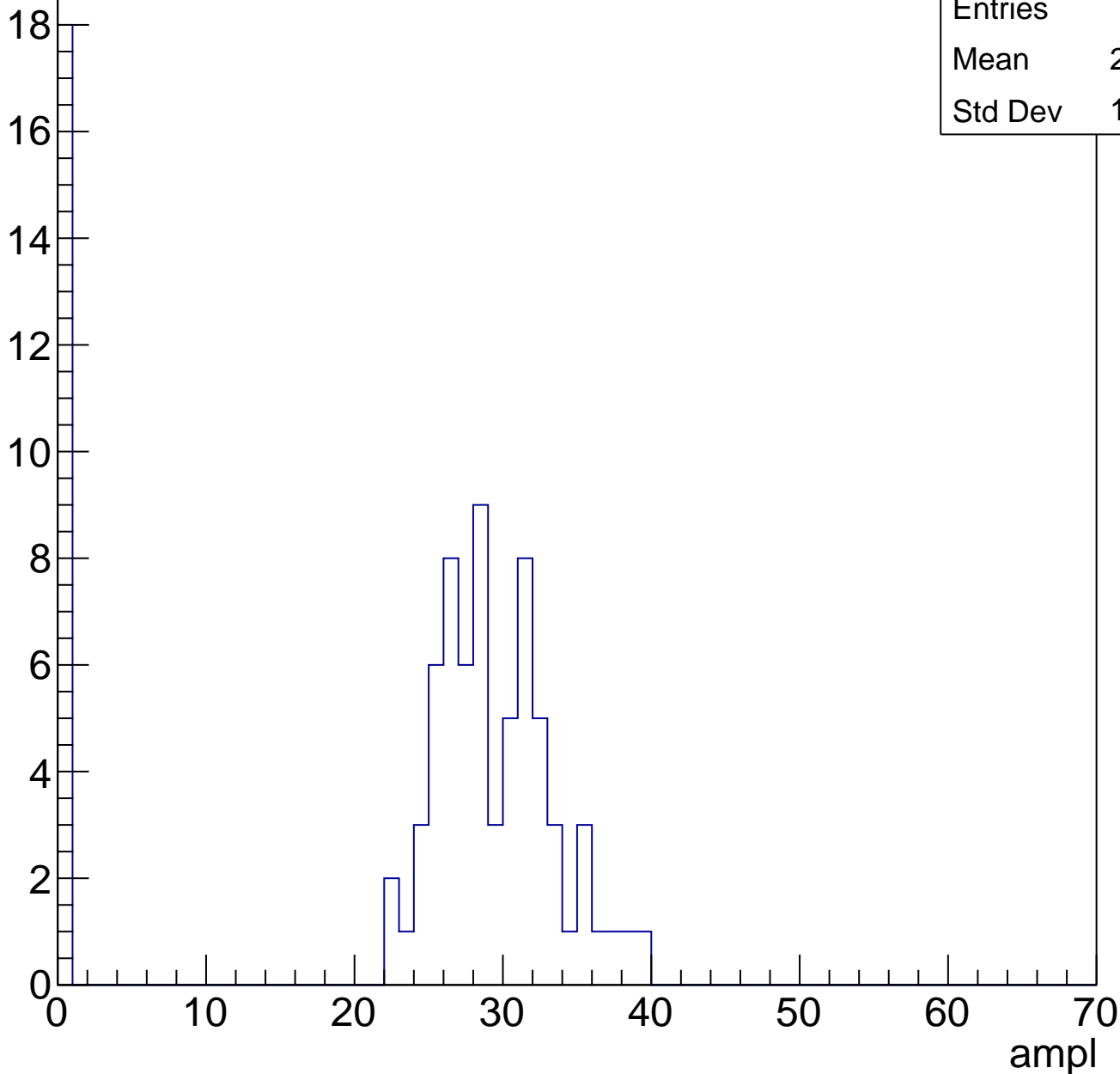


B1L103S, U5-ch87, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	85
Mean	22.87
Std Dev	12.32

Entry

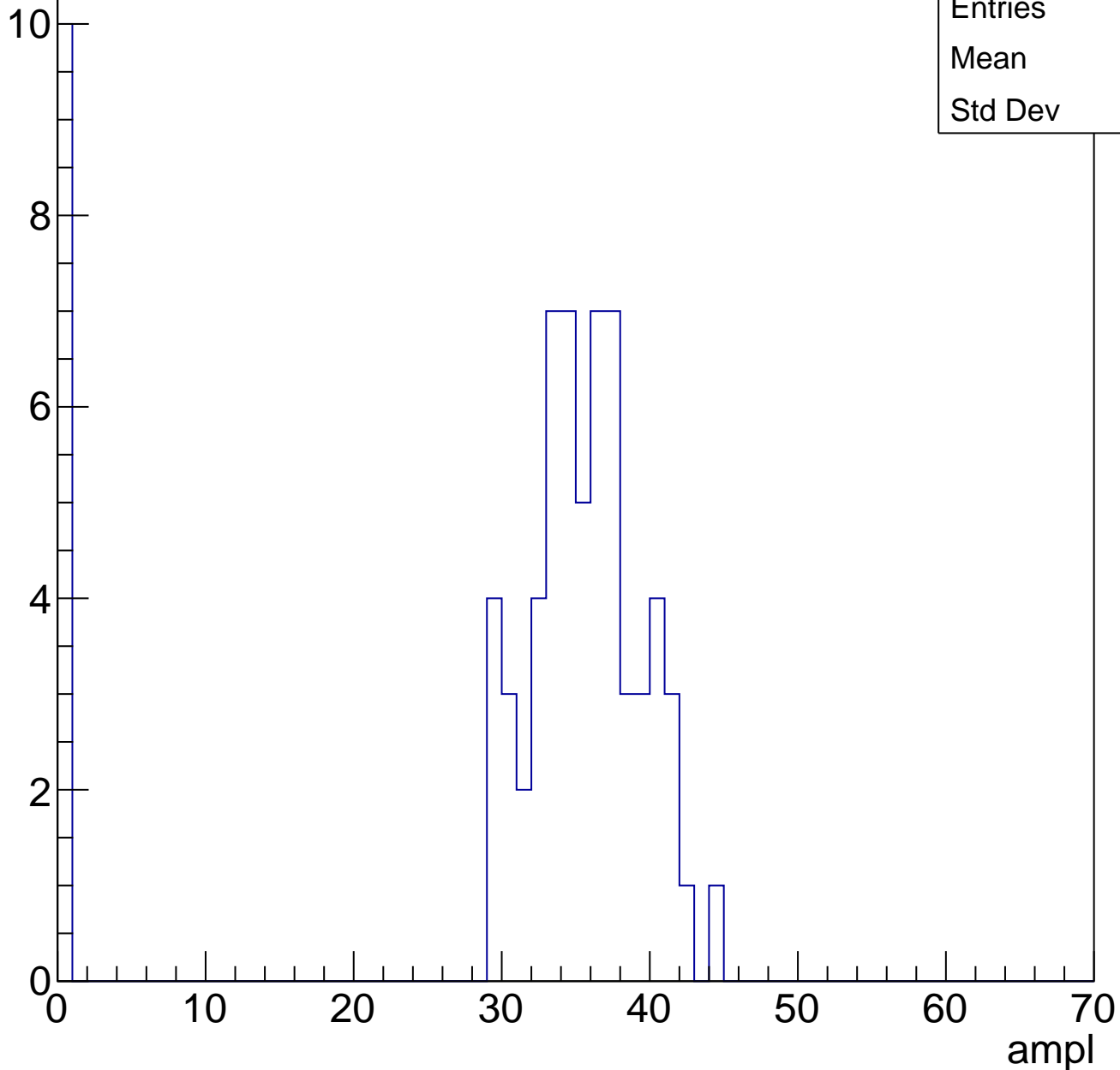


B1L103S, U5-ch87, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	71
Mean	30.3
Std Dev	12.7

Entry

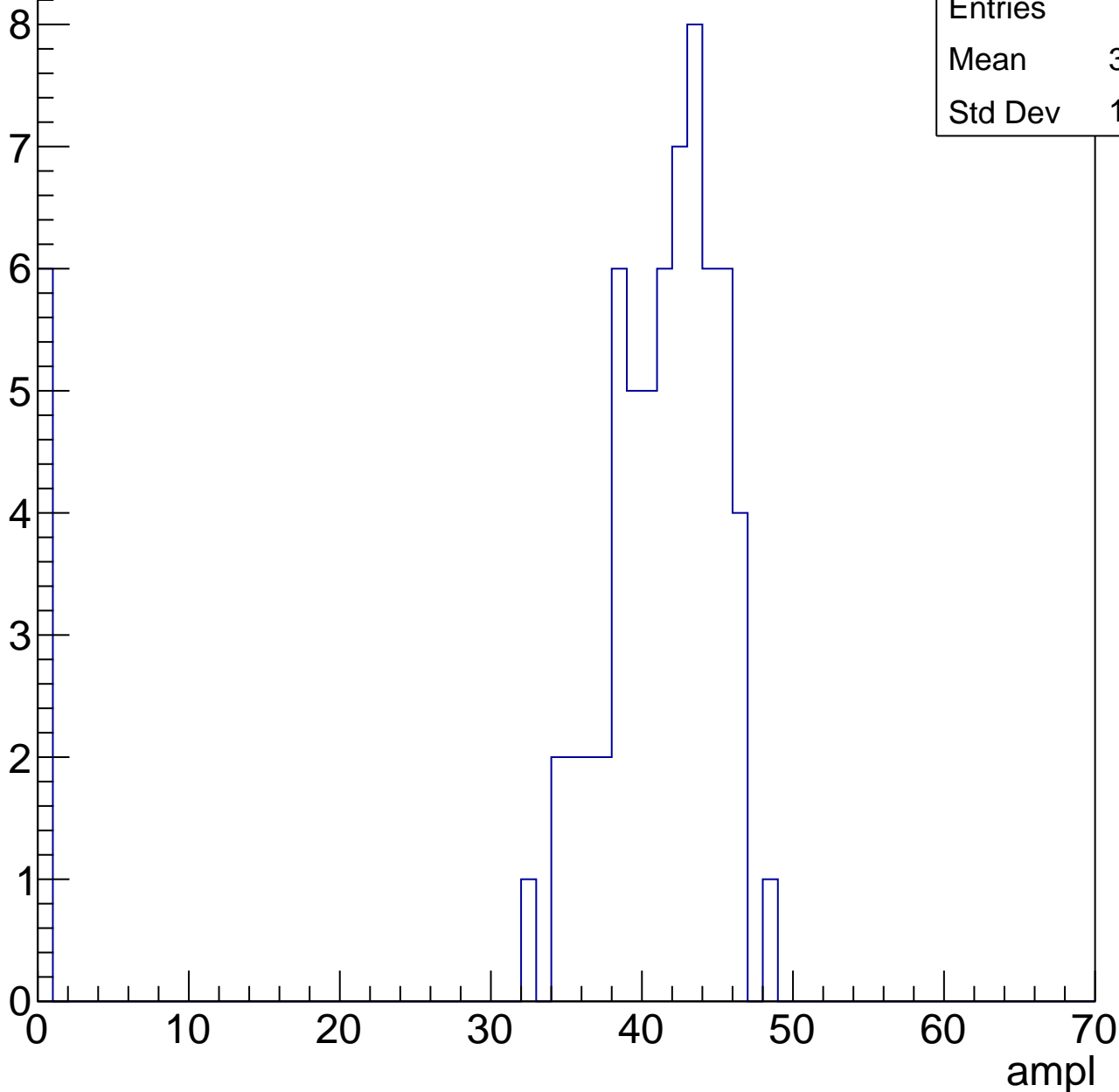


B1L103S, U5-ch87, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

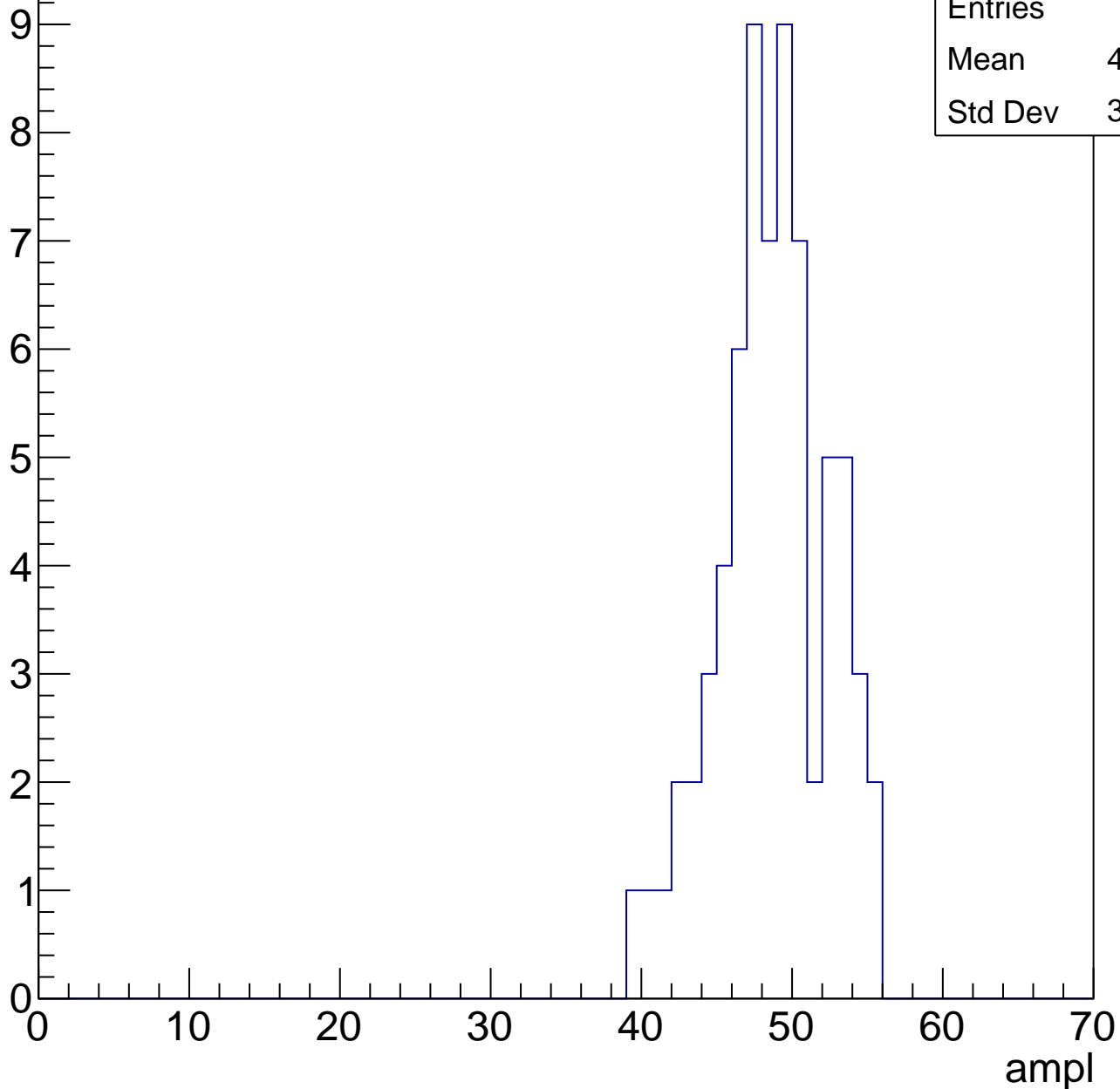
Entries	69
Mean	37.52
Std Dev	12.04



B1L103S, U5-ch87, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry



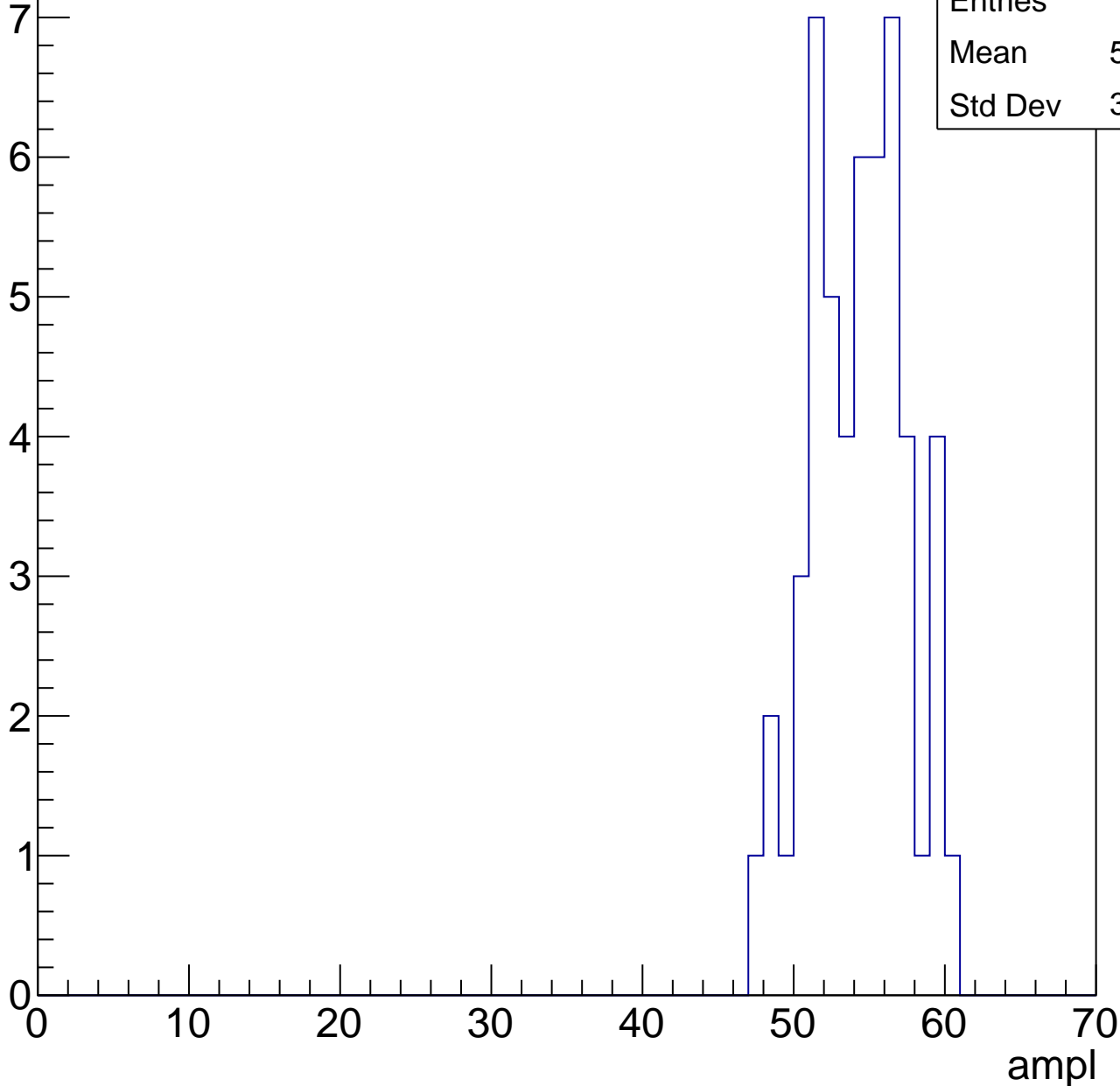
Entries	69
Mean	48.22
Std Dev	3.603

B1L103S, U5-ch87, adc4

calib_packv5_041523_1651.root, FC#0, port C2

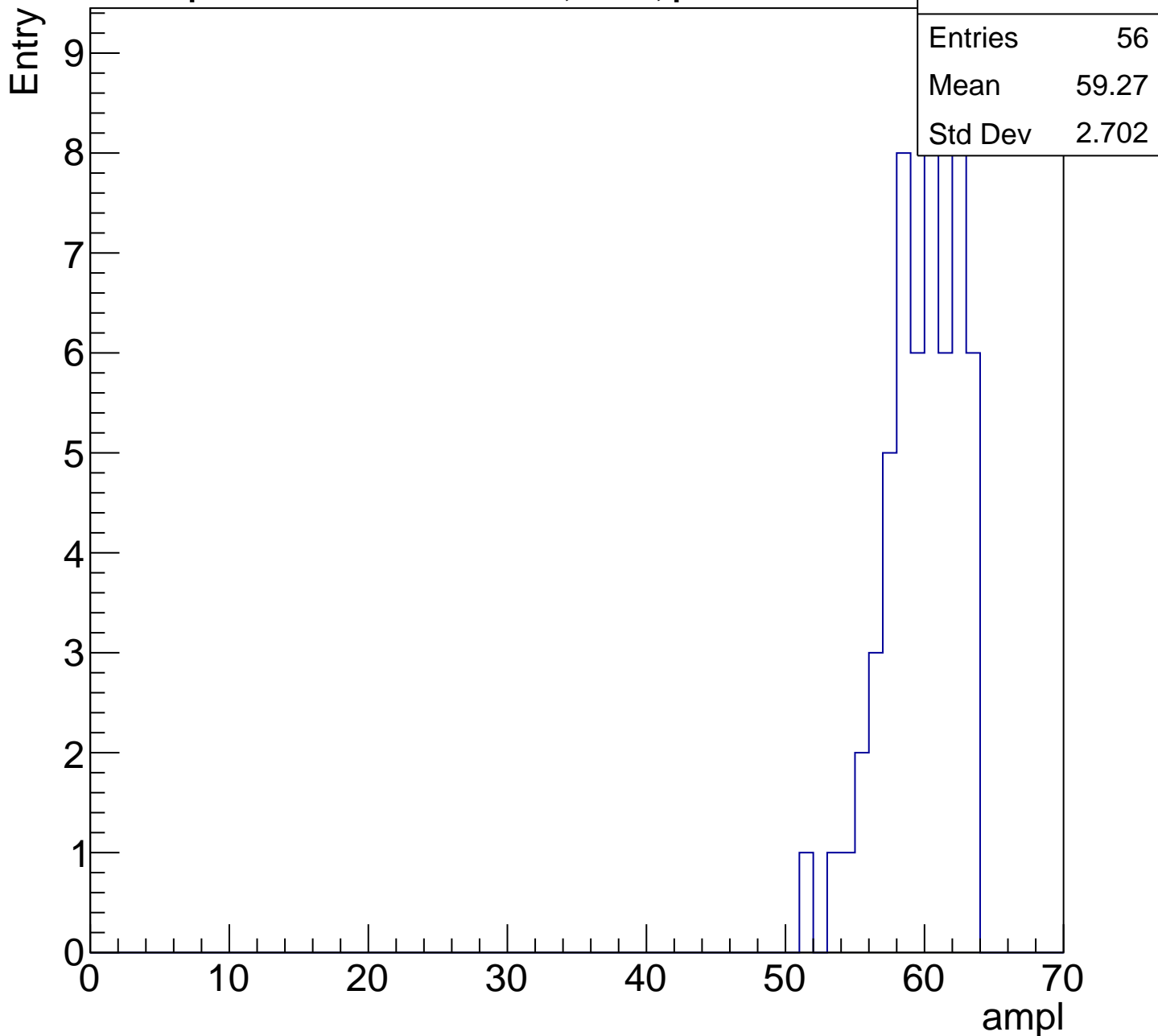
Entry

Entries	52
Mean	53.83
Std Dev	3.105



B1L103S, U5-ch87, adc5

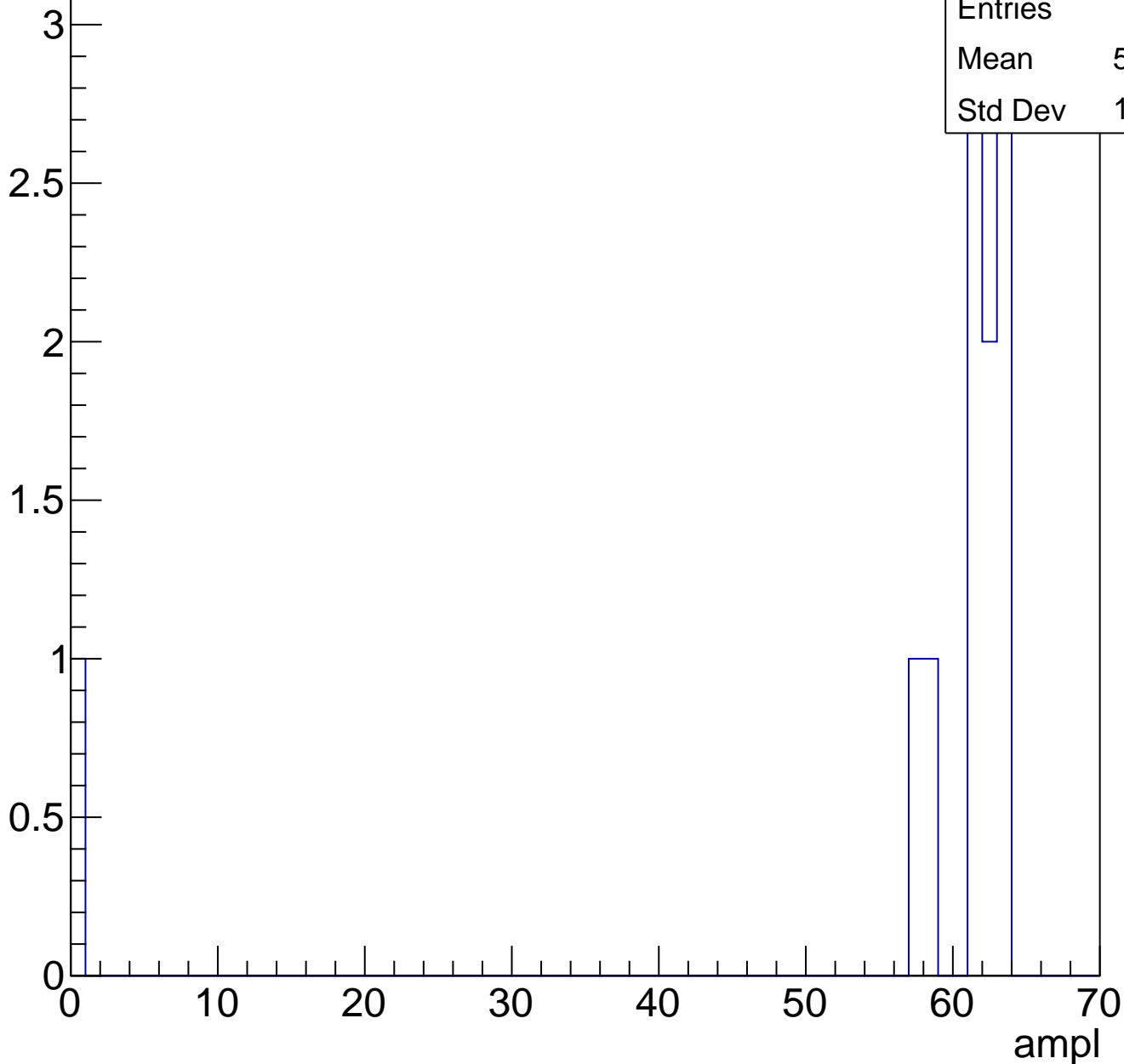
calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U5-ch87, adc6

calib_packv5_041523_1651.root, FC#0, port C2

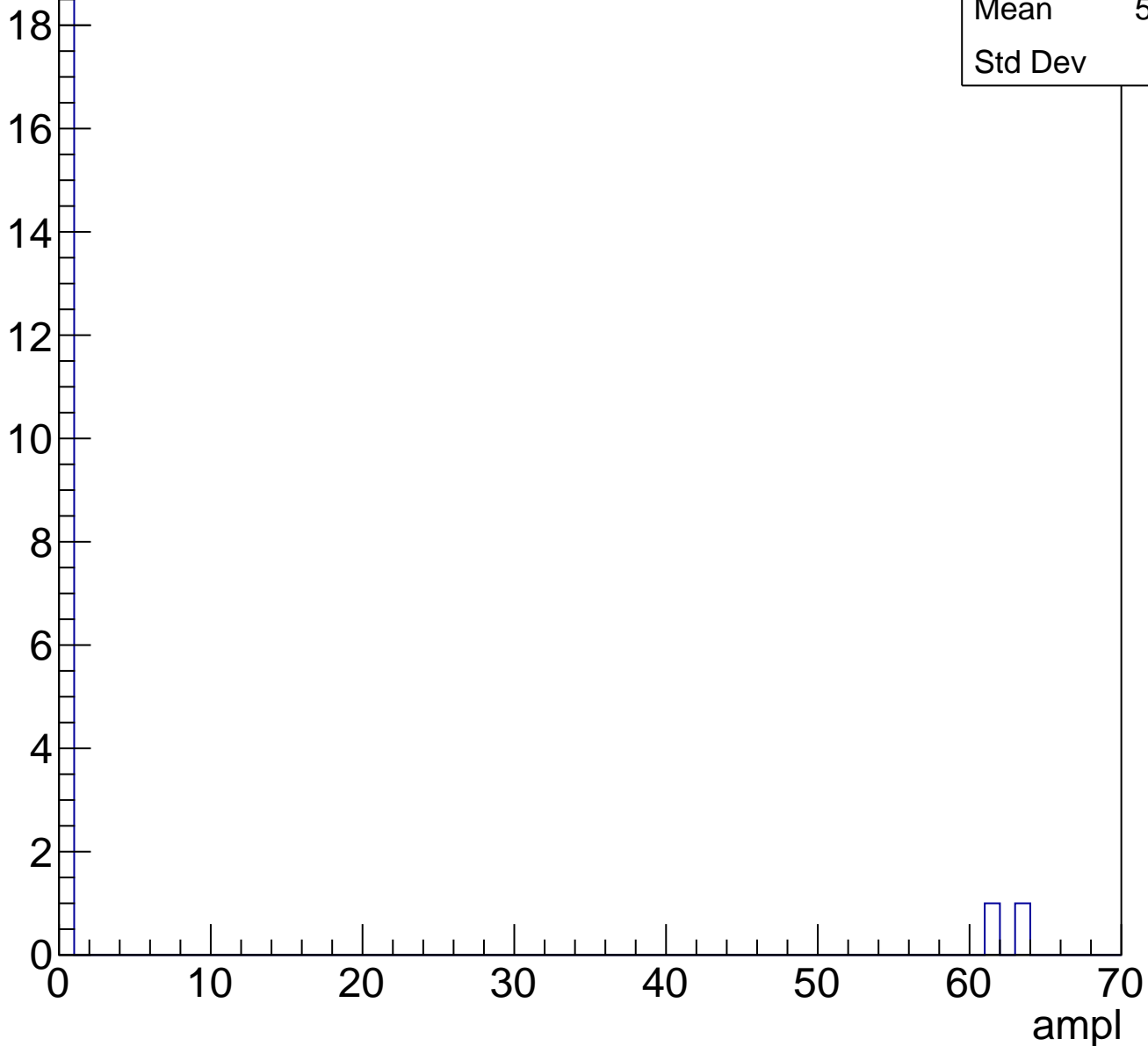
Entry



B1L103S, U5-ch87, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

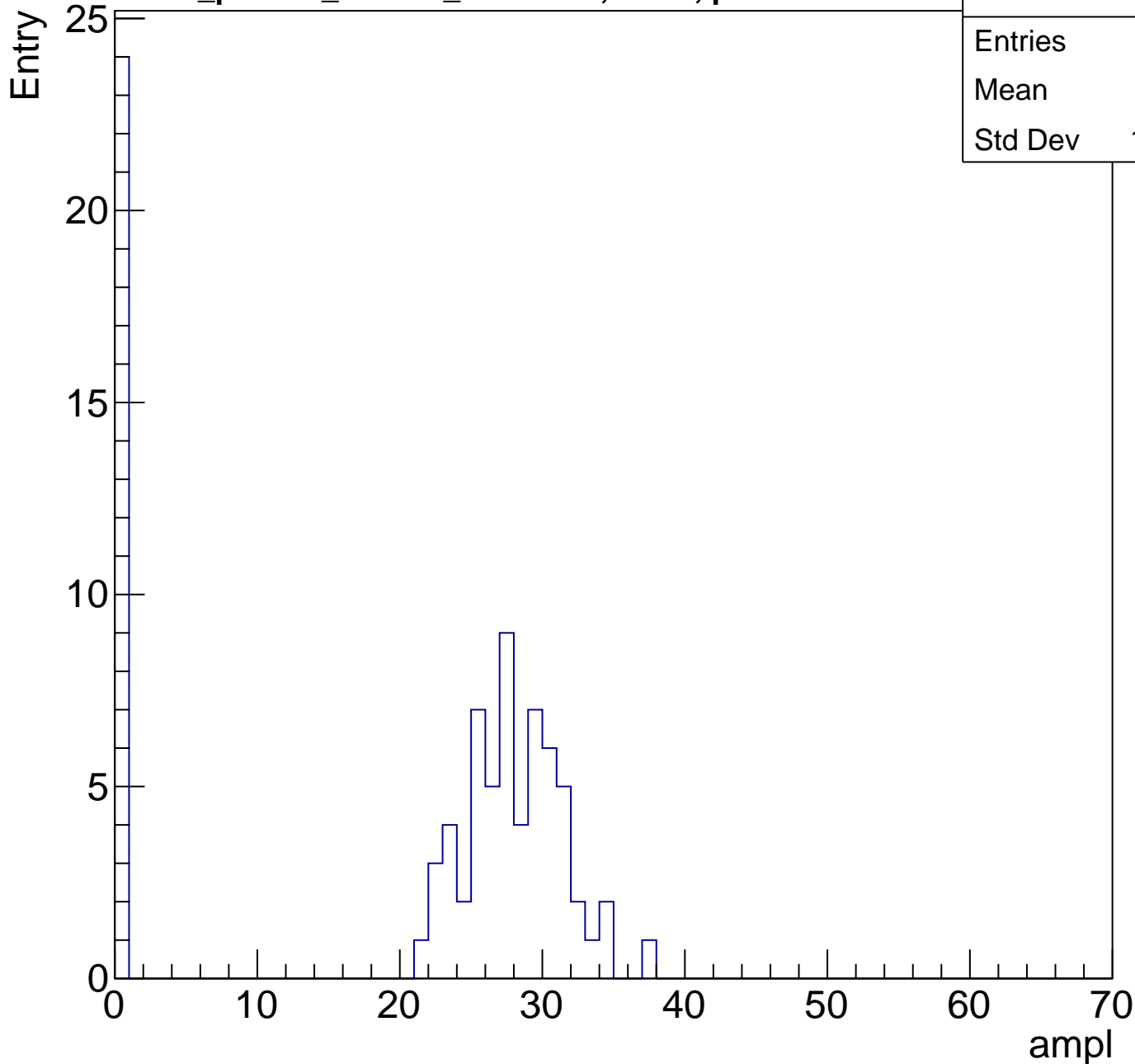


Entries	21
Mean	5.905
Std Dev	18.2

B1L103S, U5-ch88, adc0

calib_packv5_041523_1651.root, FC#0, port C2

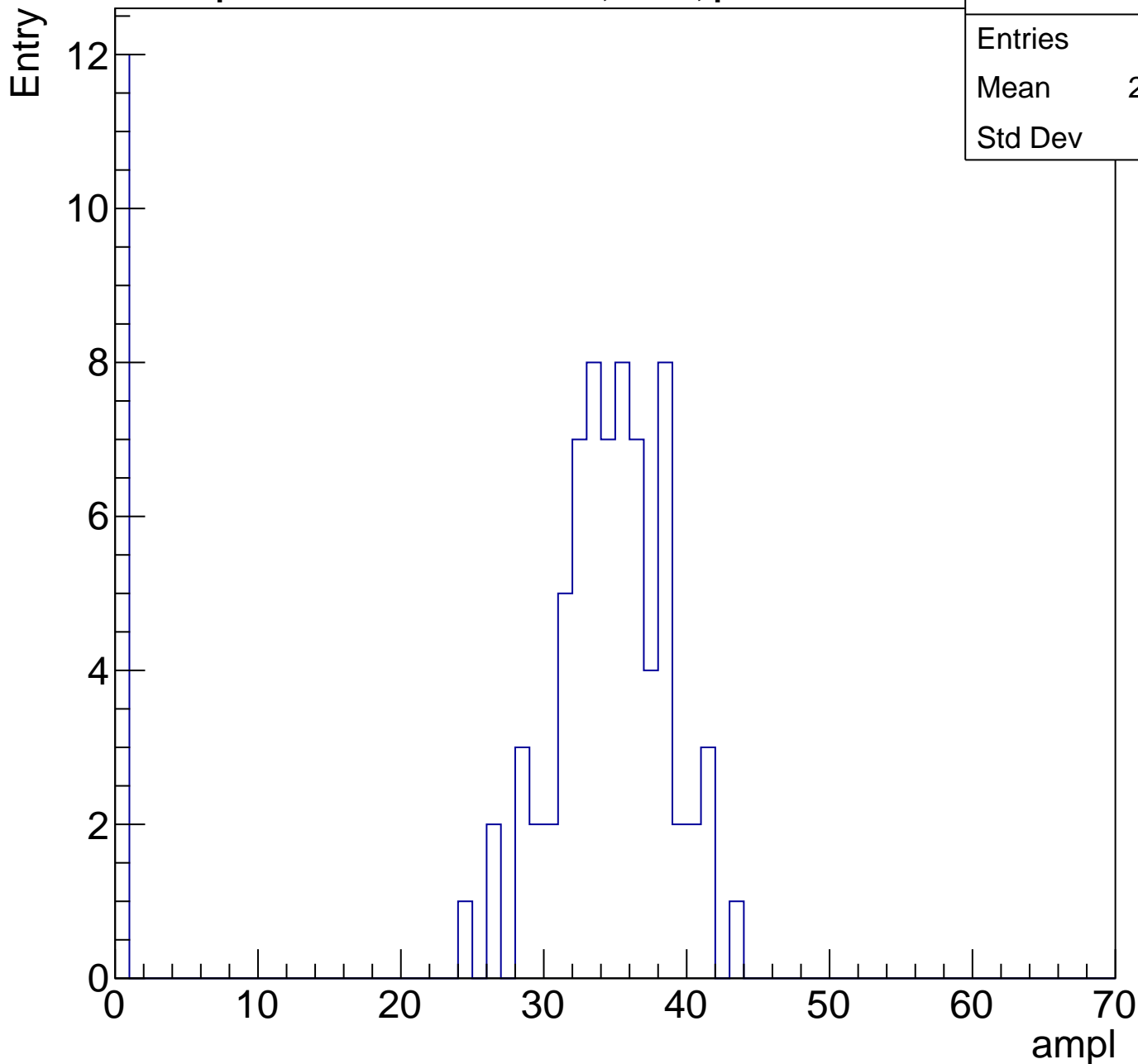
Entries	83
Mean	19.6
Std Dev	12.81



B1L103S, U5-ch88, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	84
Mean	29.37
Std Dev	12.5

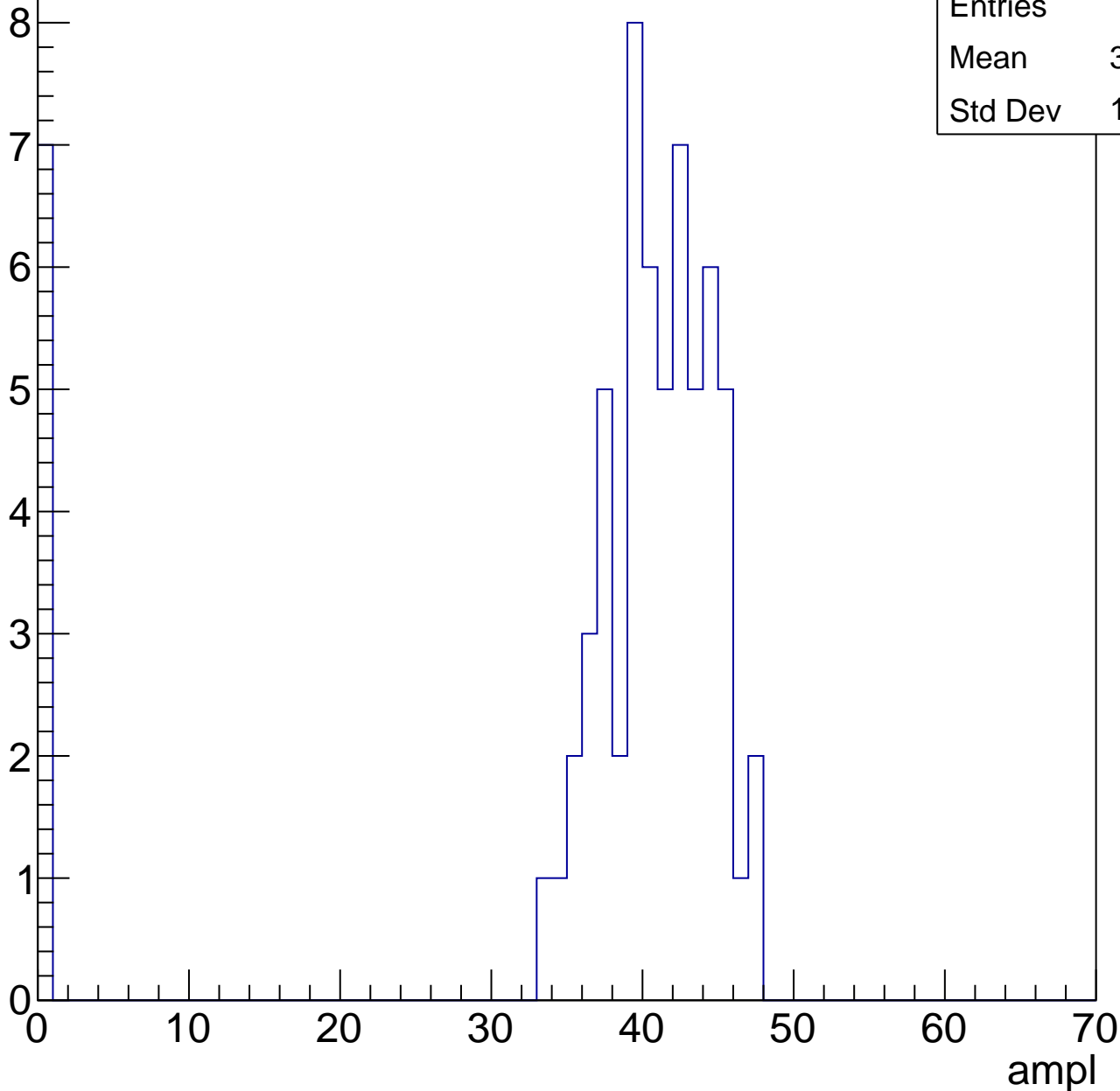


B1L103S, U5-ch88, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

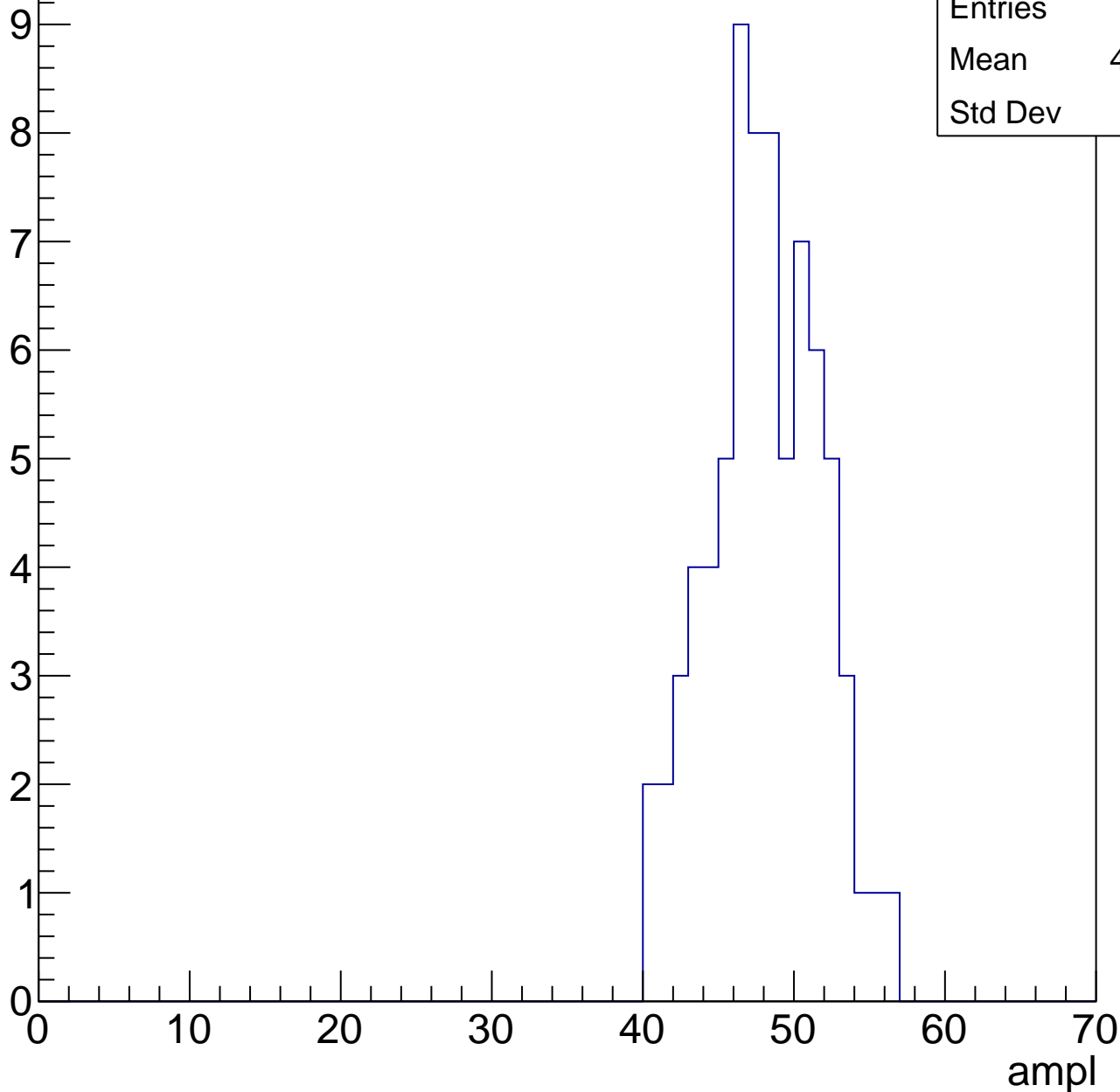
Entries	66
Mean	36.38
Std Dev	12.92



B1L103S, U5-ch88, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

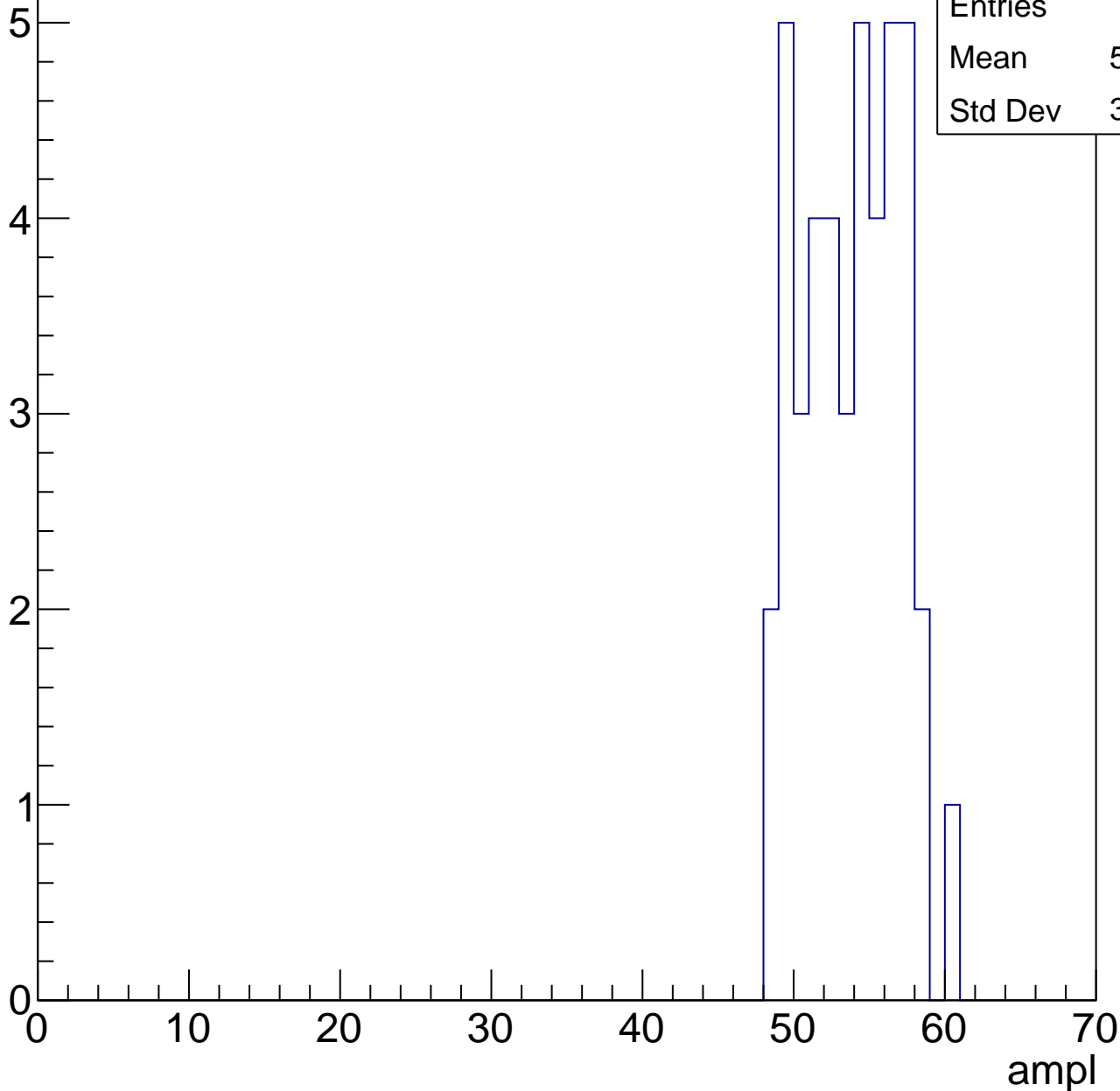


B1L103S, U5-ch88, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	43
Mean	53.33
Std Dev	3.116

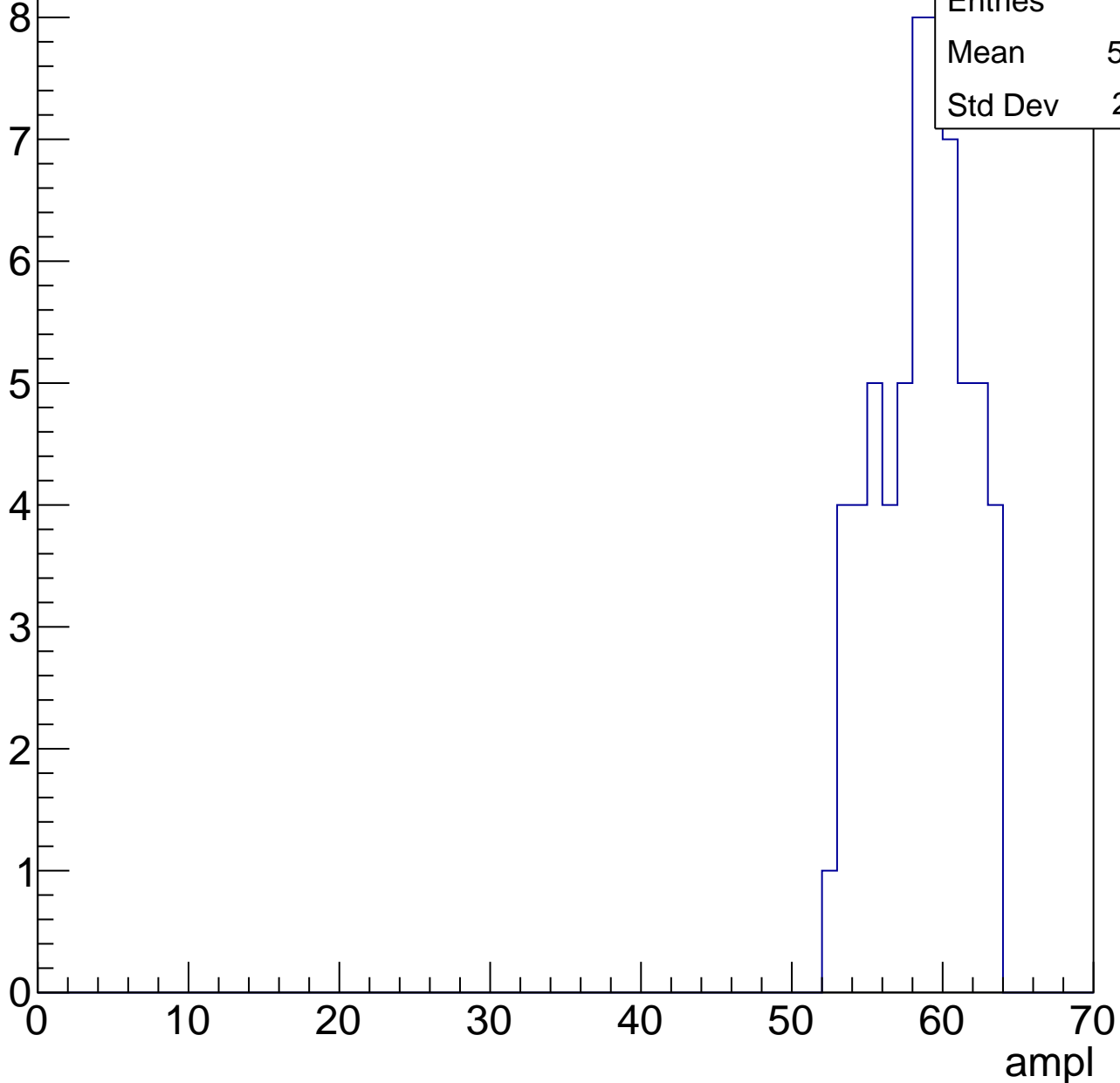


B1L103S, U5-ch88, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	58.12
Std Dev	2.961

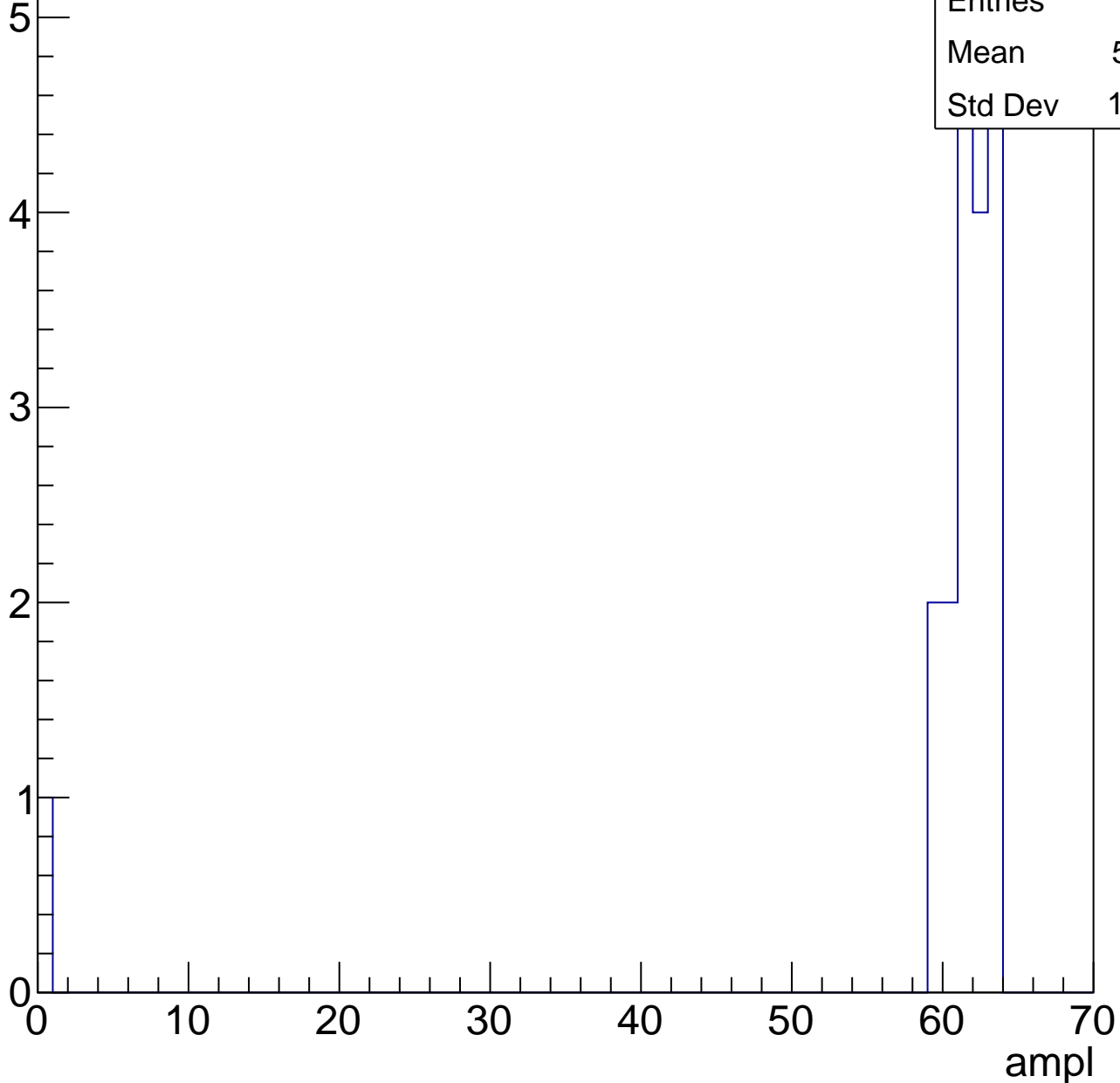


B1L103S, U5-ch88, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	19
Mean	58.21
Std Dev	13.78



B1L103S, U5-ch88, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	5.952
Std Dev	18.35

Entry

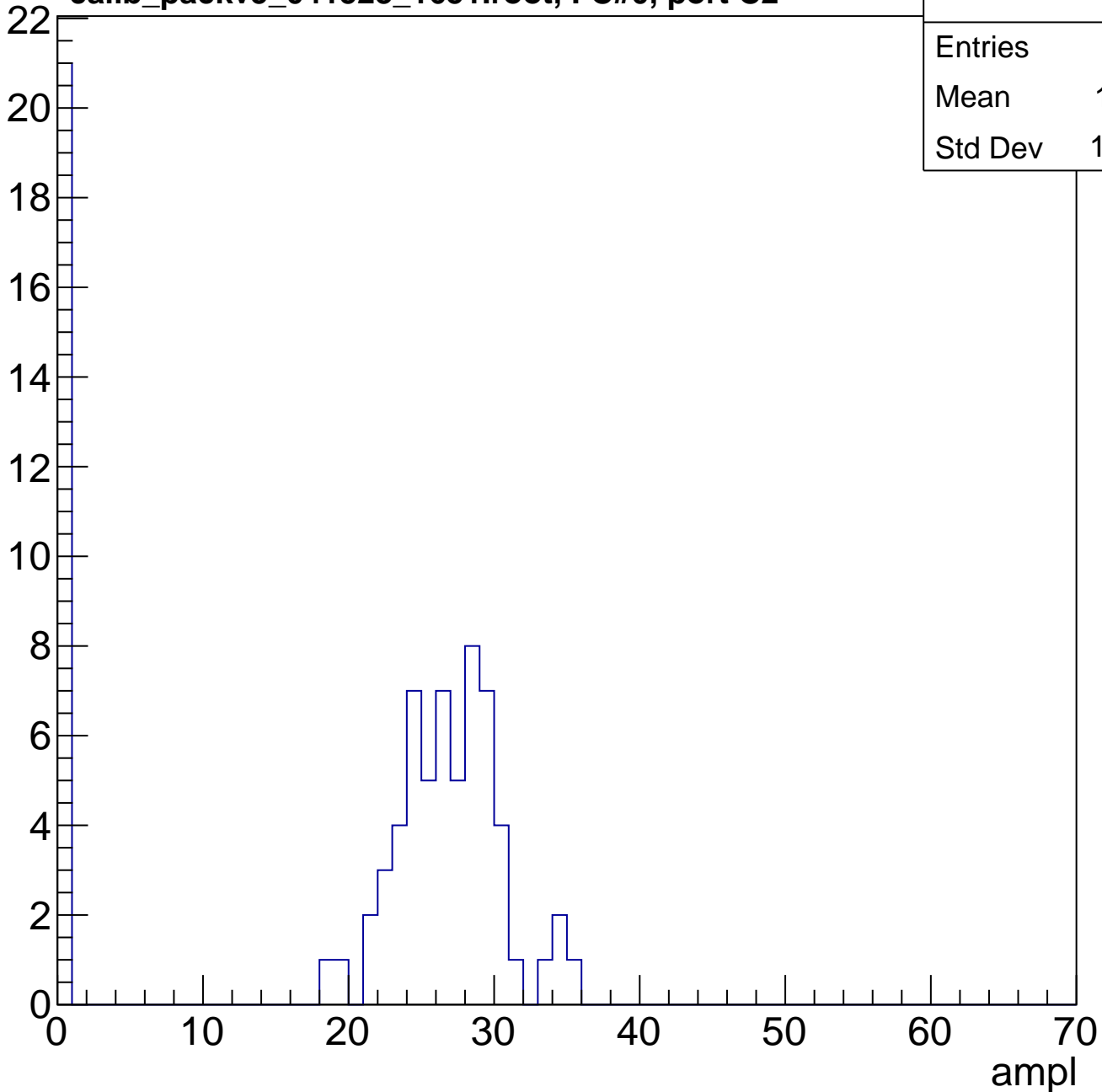


B1L103S, U5-ch89, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	19.51
Std Dev	12.02

Entry

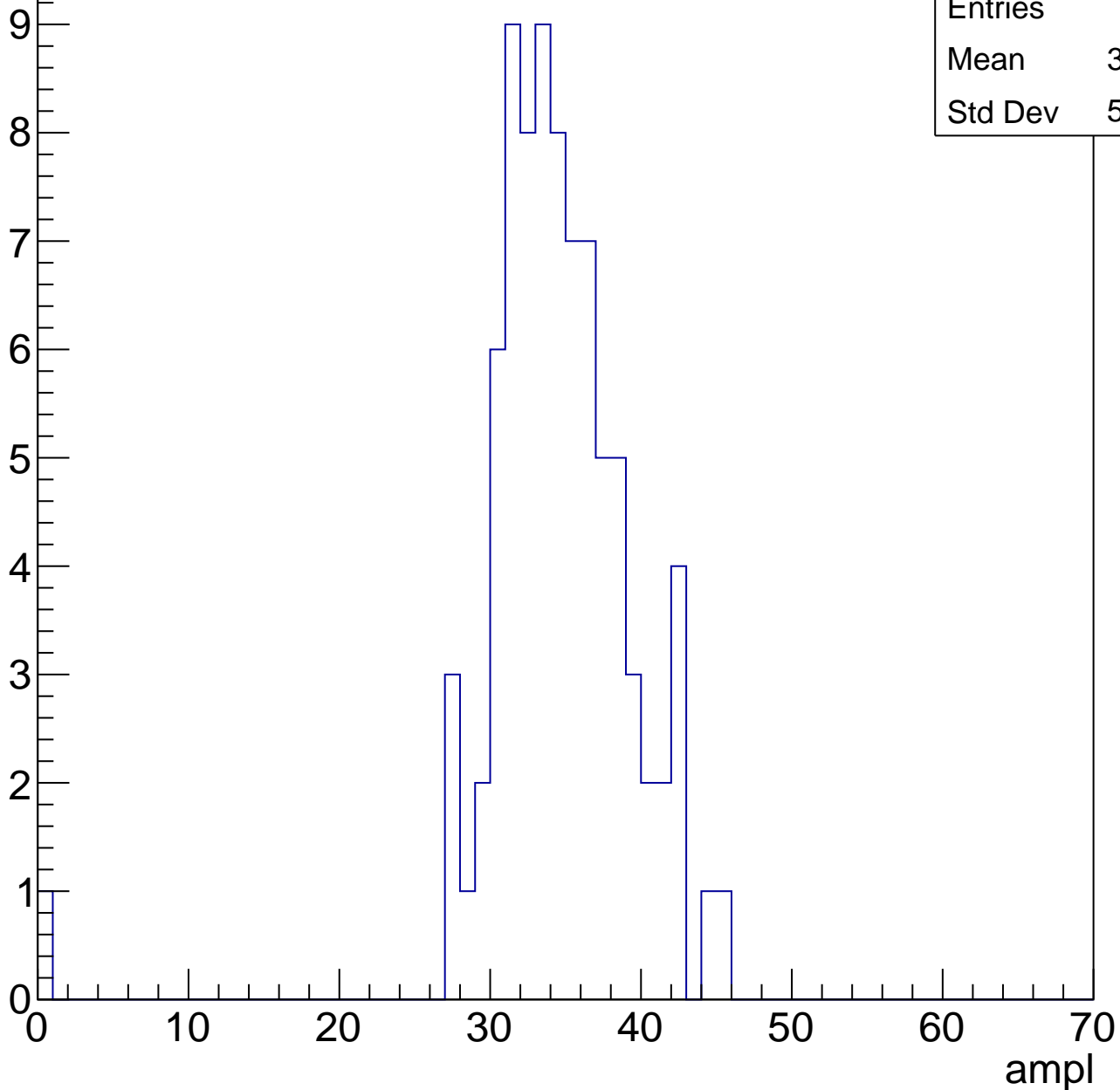


B1L103S, U5-ch89, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	84
Mean	34.04
Std Dev	5.443

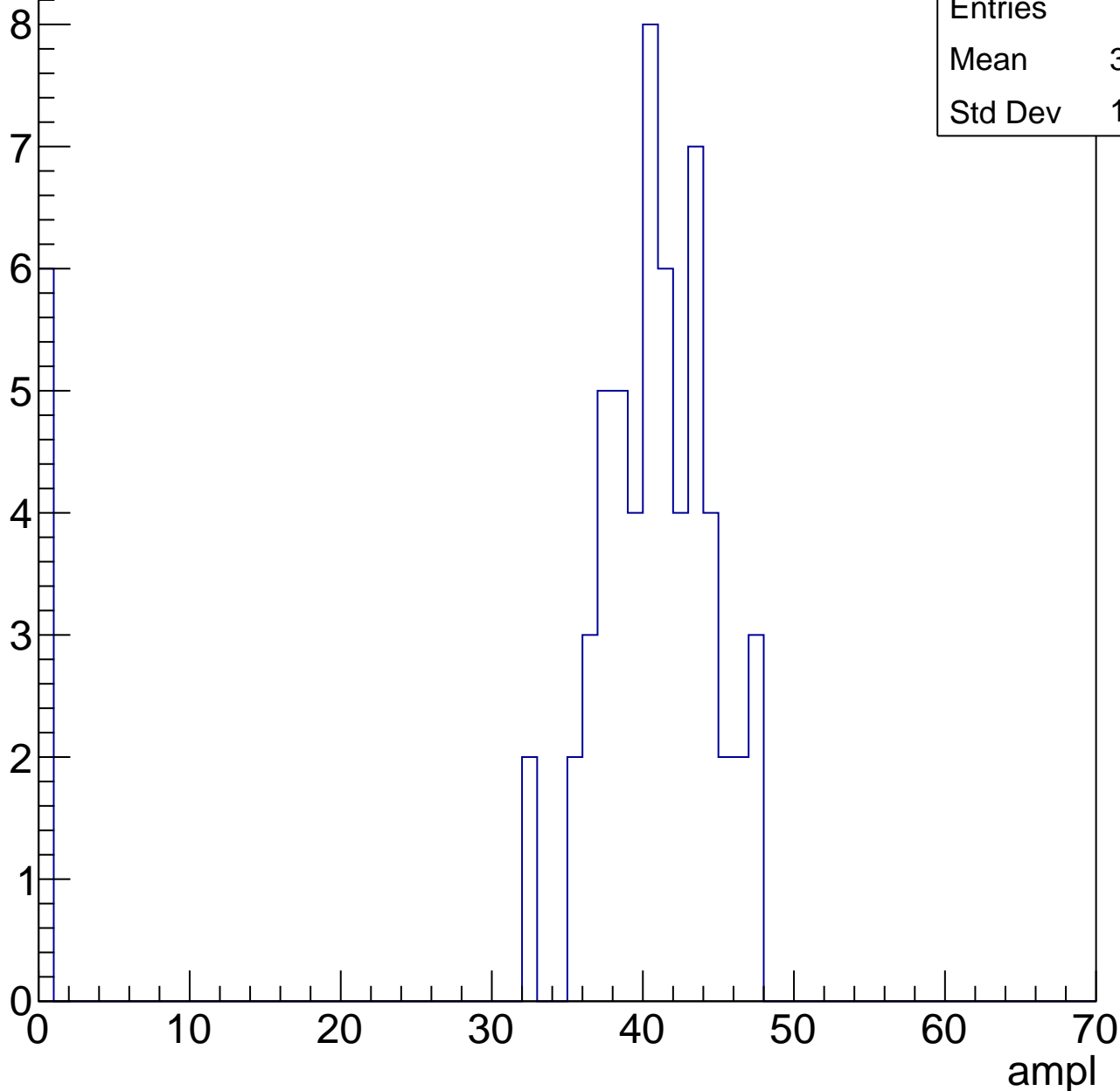


B1L103S, U5-ch89, adc2

calib_packv5_041523_1651.root, FC#0, port C2

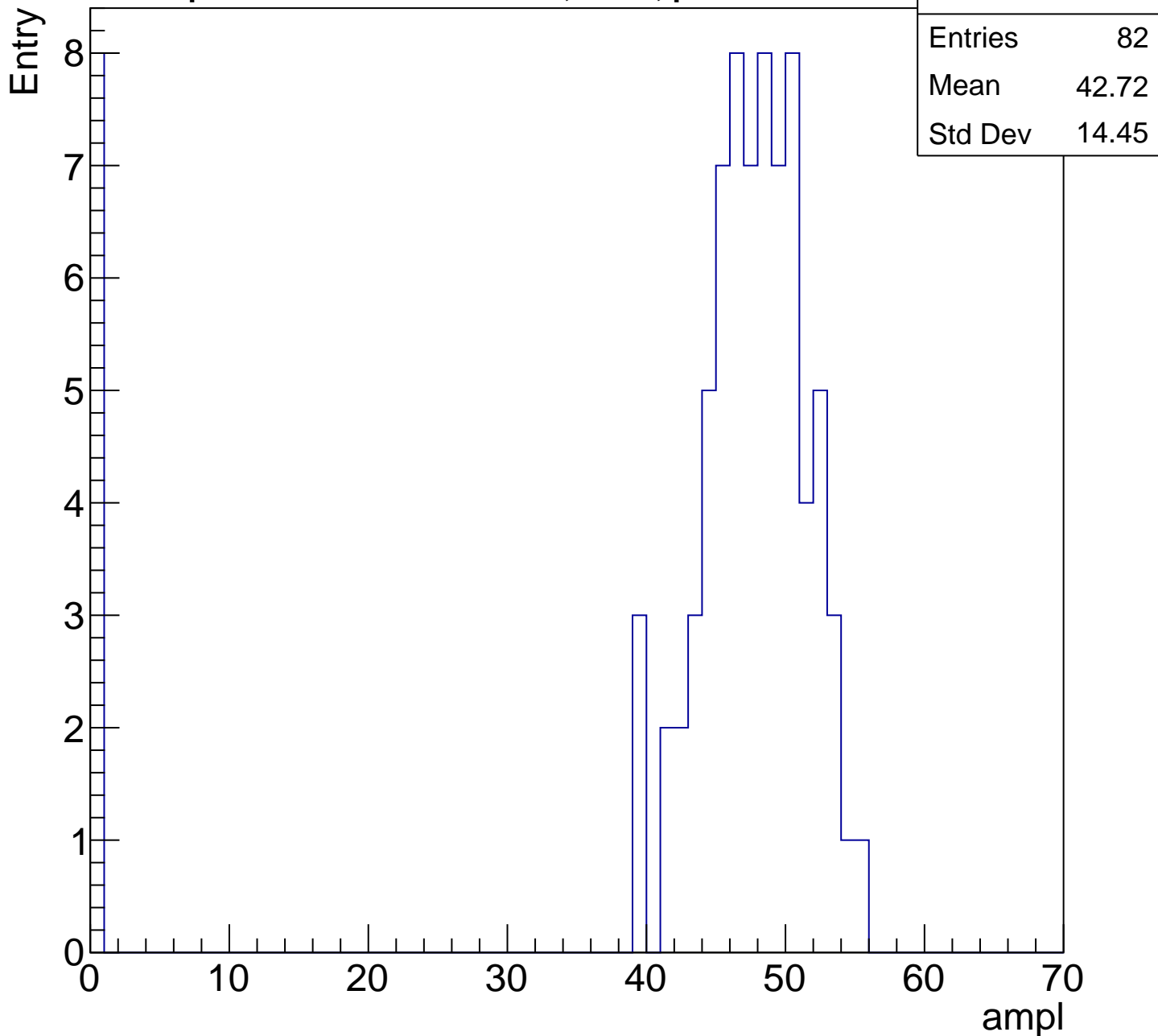
Entry

Entries	63
Mean	36.62
Std Dev	12.34



B1L103S, U5-ch89, adc3

calib_packv5_041523_1651.root, FC#0, port C2

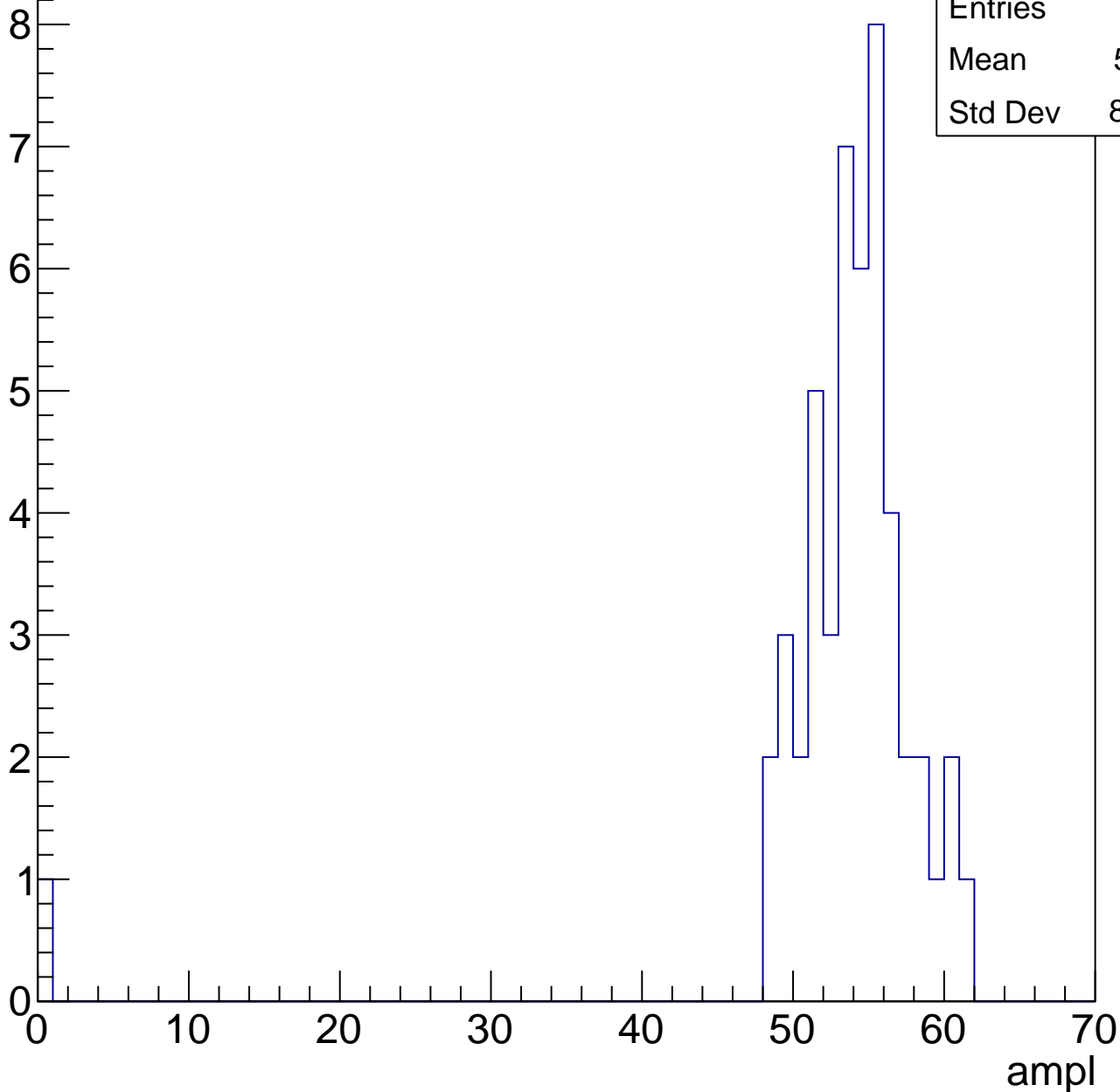


B1L103S, U5-ch89, adc4

calib_packv5_041523_1651.root, FC#0, port C2

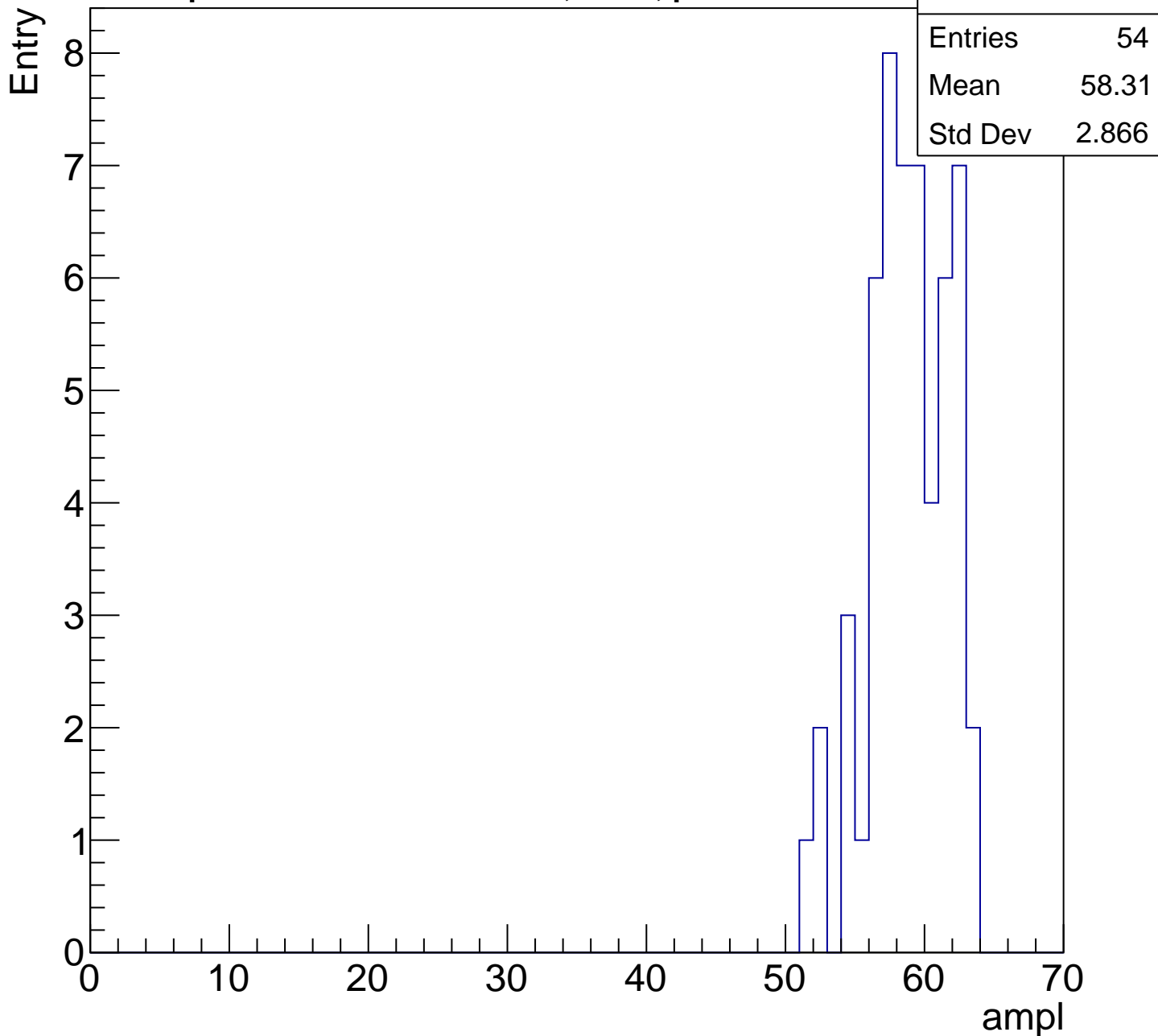
Entry

Entries	49
Mean	52.71
Std Dev	8.204



B1L103S, U5-ch89, adc5

calib_packv5_041523_1651.root, FC#0, port C2

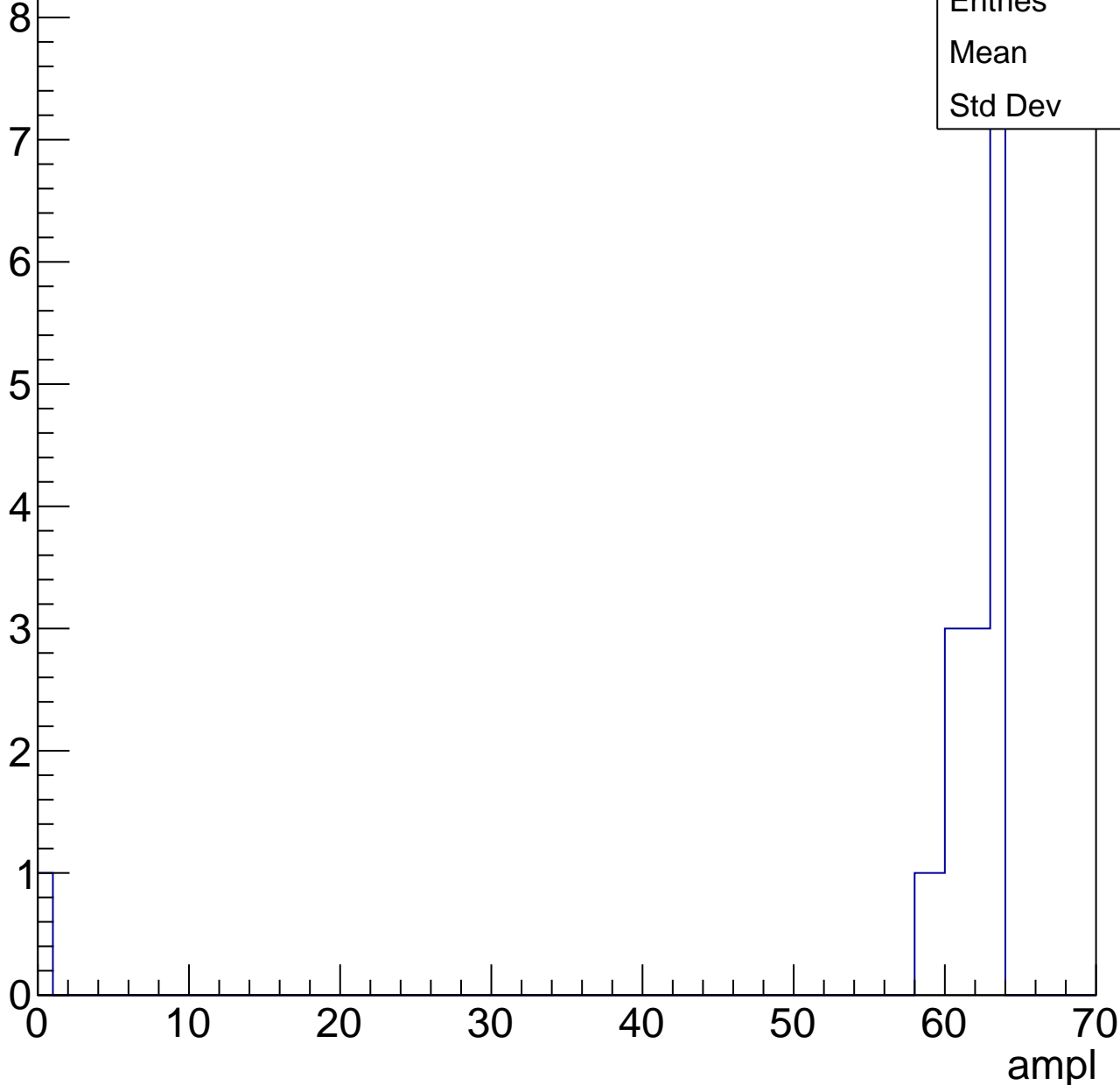


B1L103S, U5-ch89, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	20
Mean	58.5
Std Dev	13.5

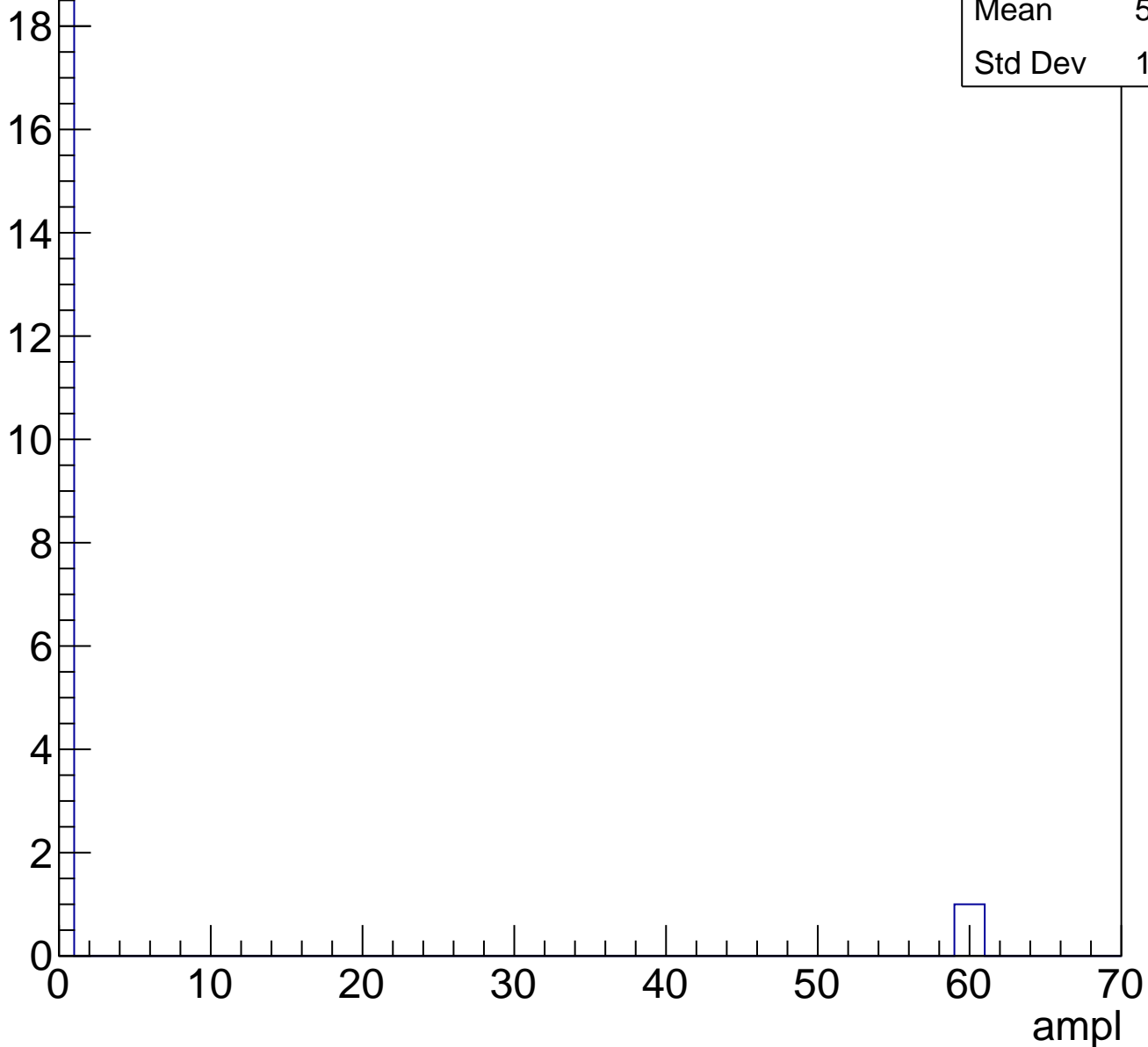


B1L103S, U5-ch89, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	5.667
Std Dev	17.47

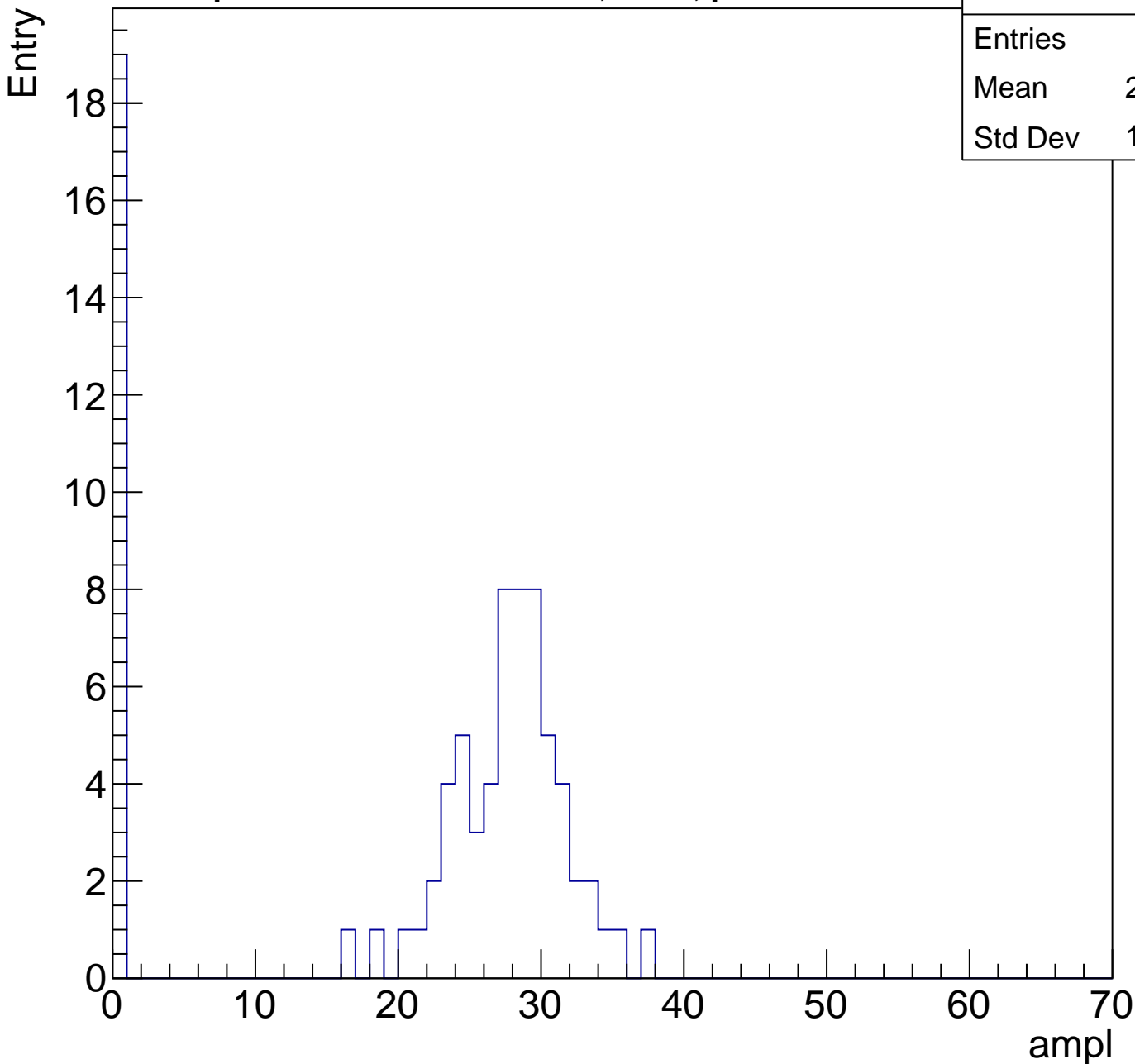
Entry



B1L103S, U5-ch90, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	20.89
Std Dev	12.06

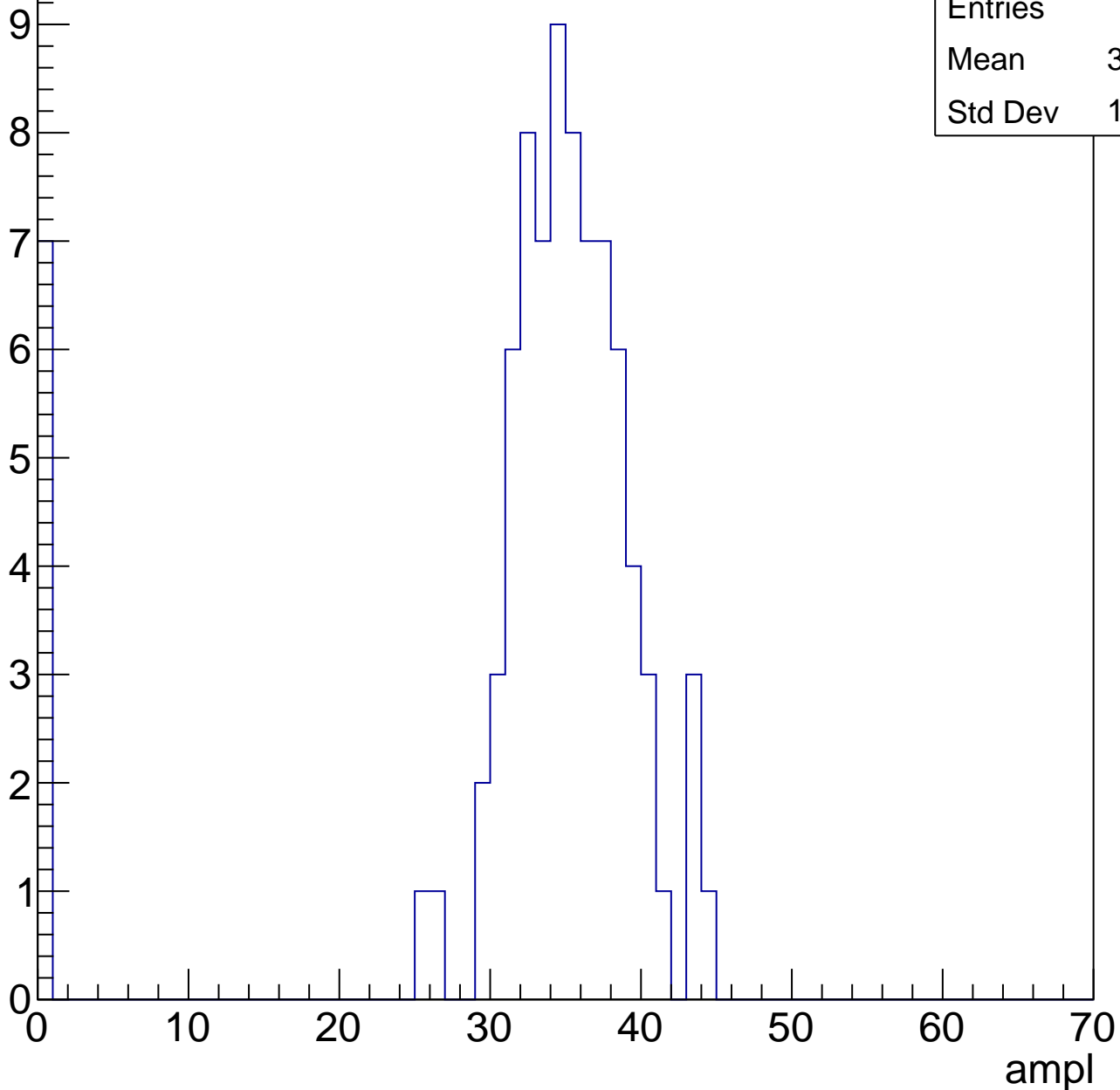


B1L103S, U5-ch90, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	84
Mean	31.99
Std Dev	10.28

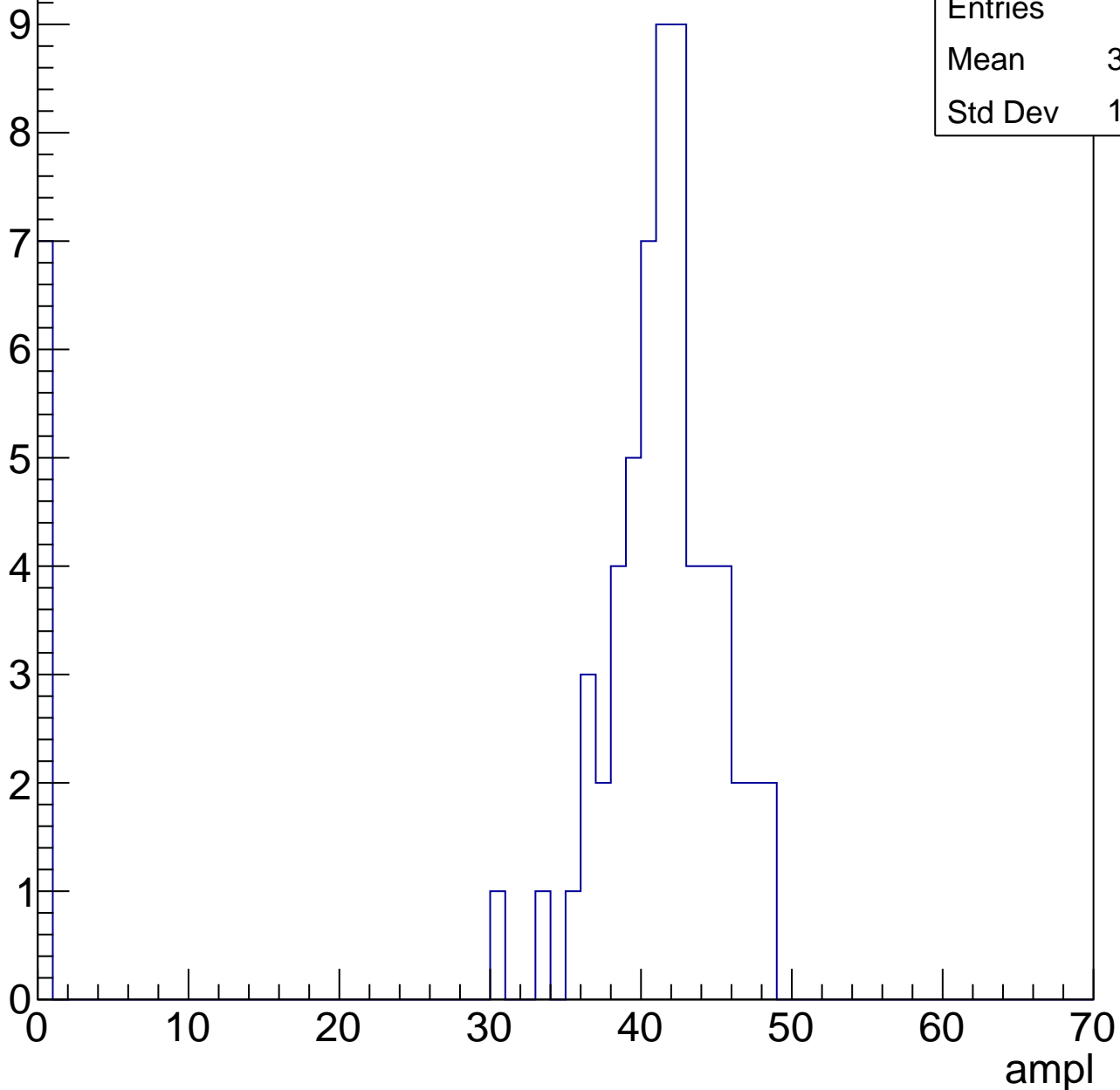


B1L103S, U5-ch90, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	36.78
Std Dev	12.99

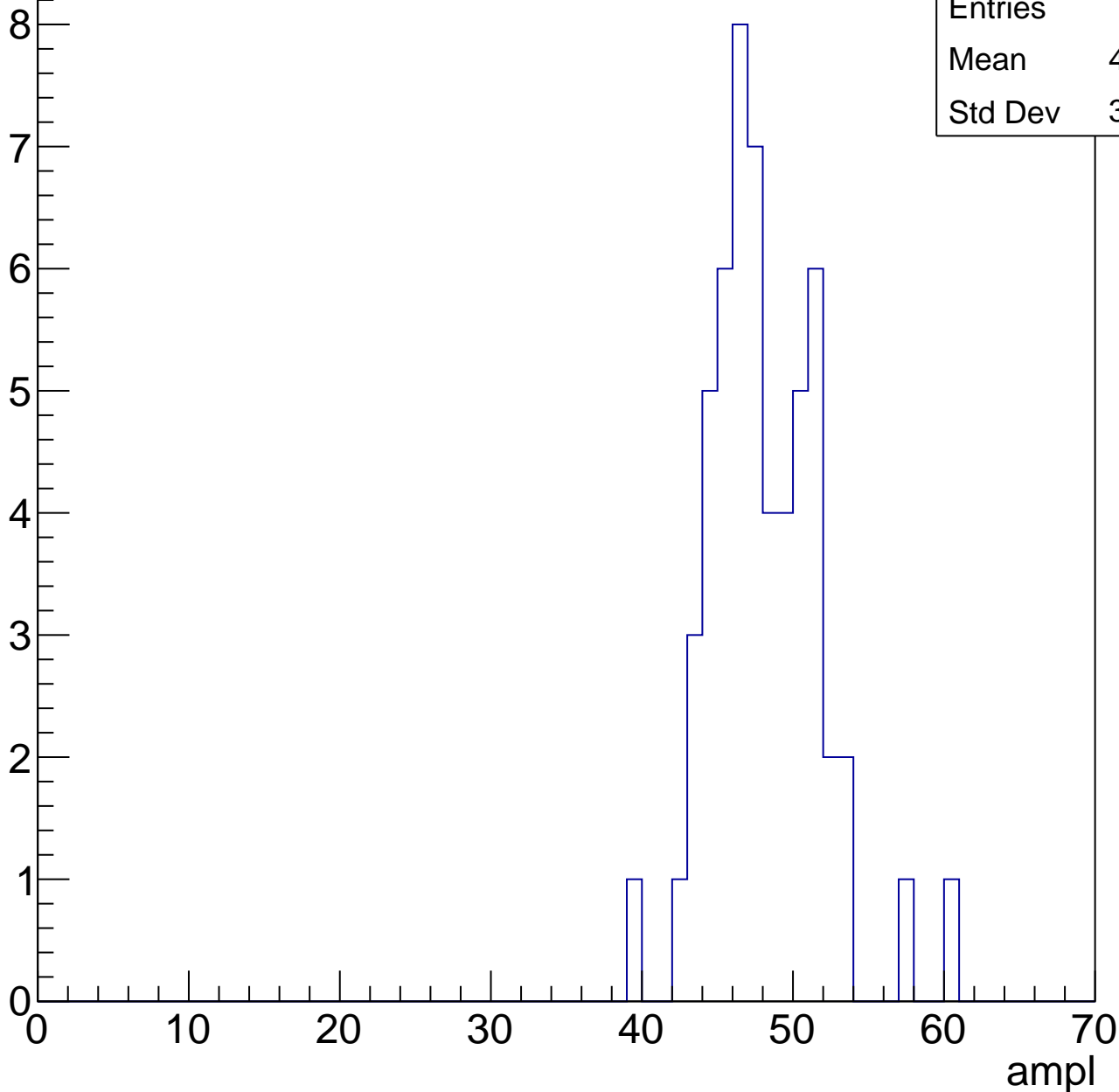


B1L103S, U5-ch90, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	47.64
Std Dev	3.642

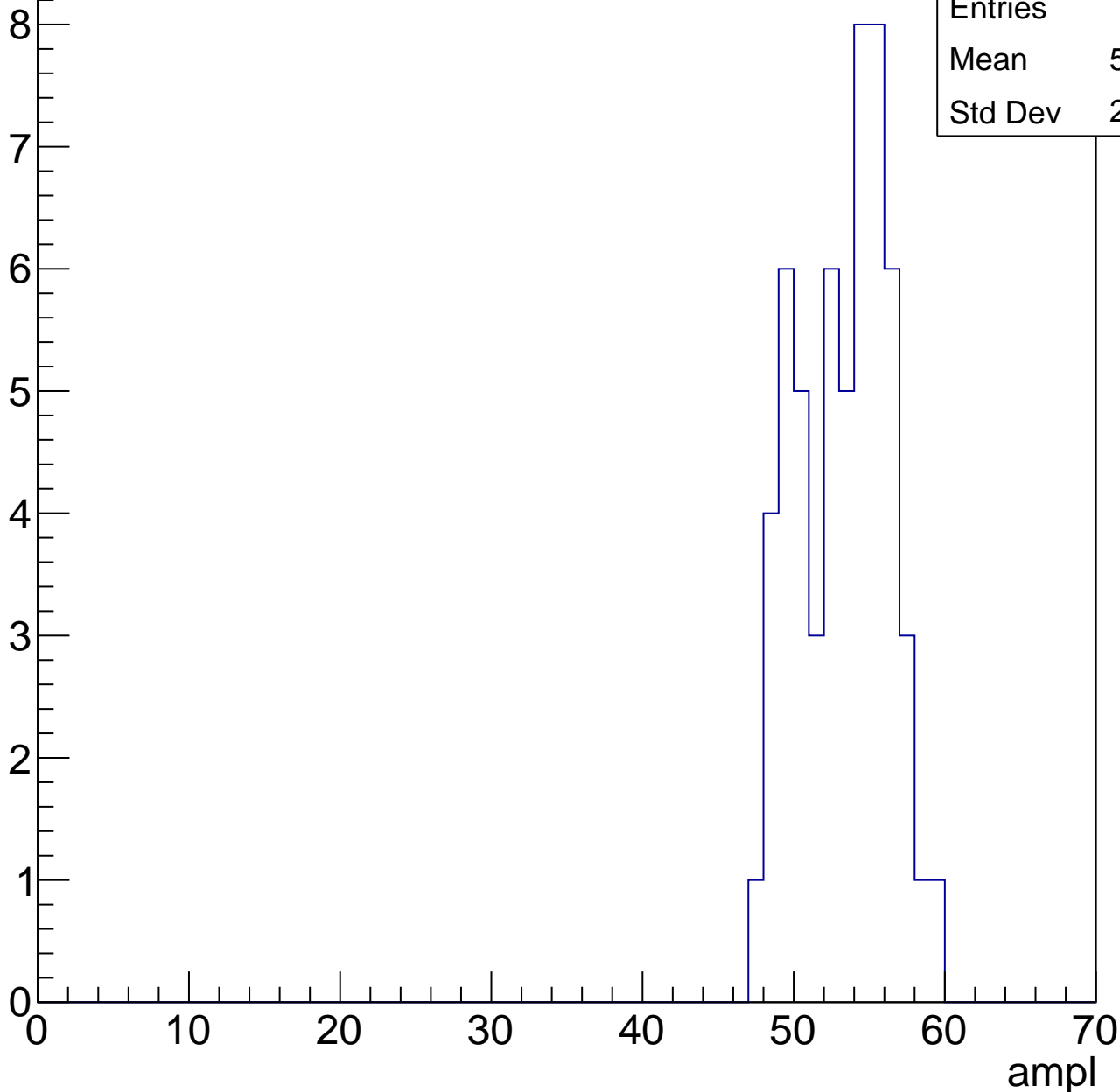


B1L103S, U5-ch90, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	52.79
Std Dev	2.948

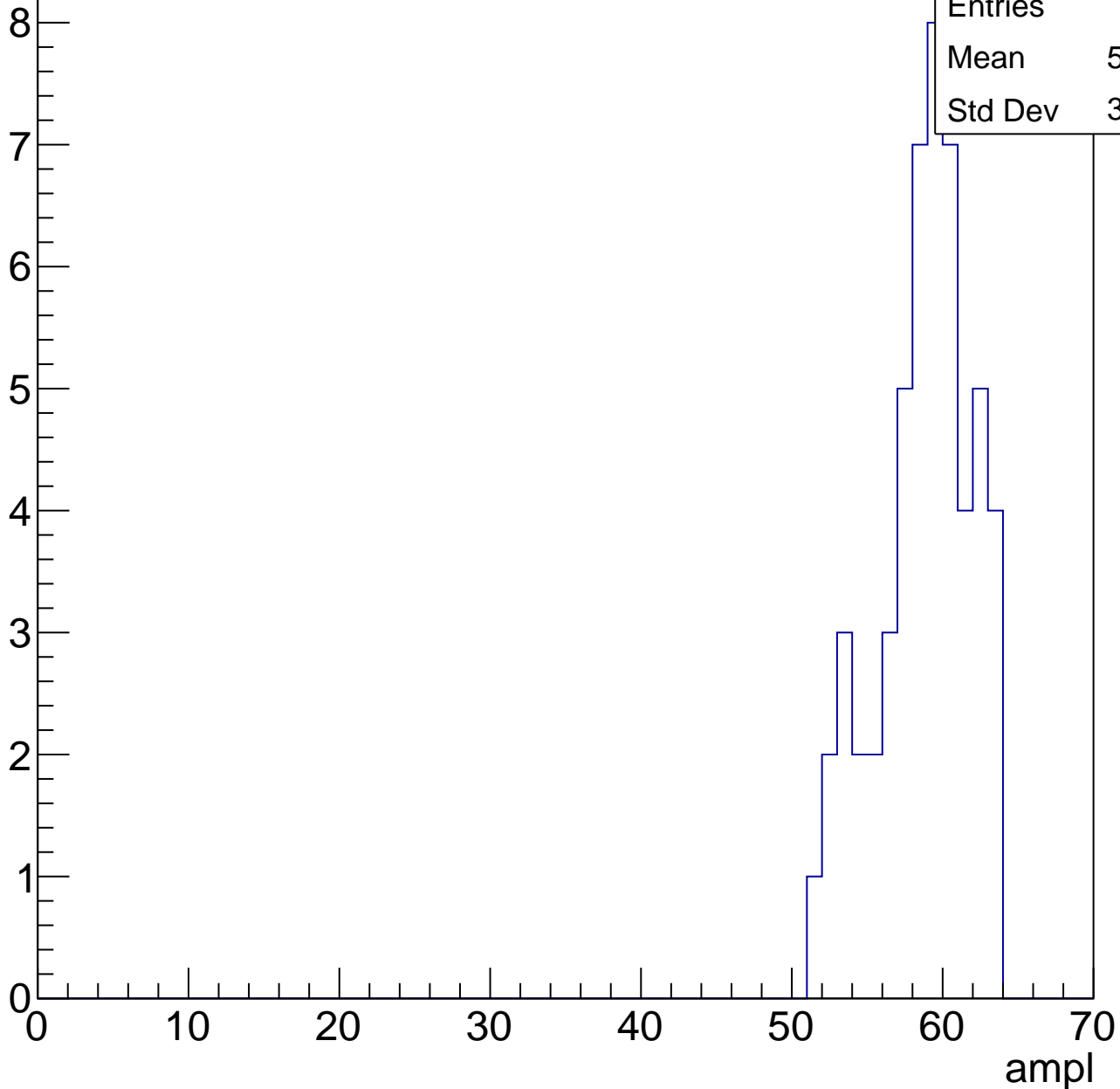


B1L103S, U5-ch90, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	58.28
Std Dev	3.104

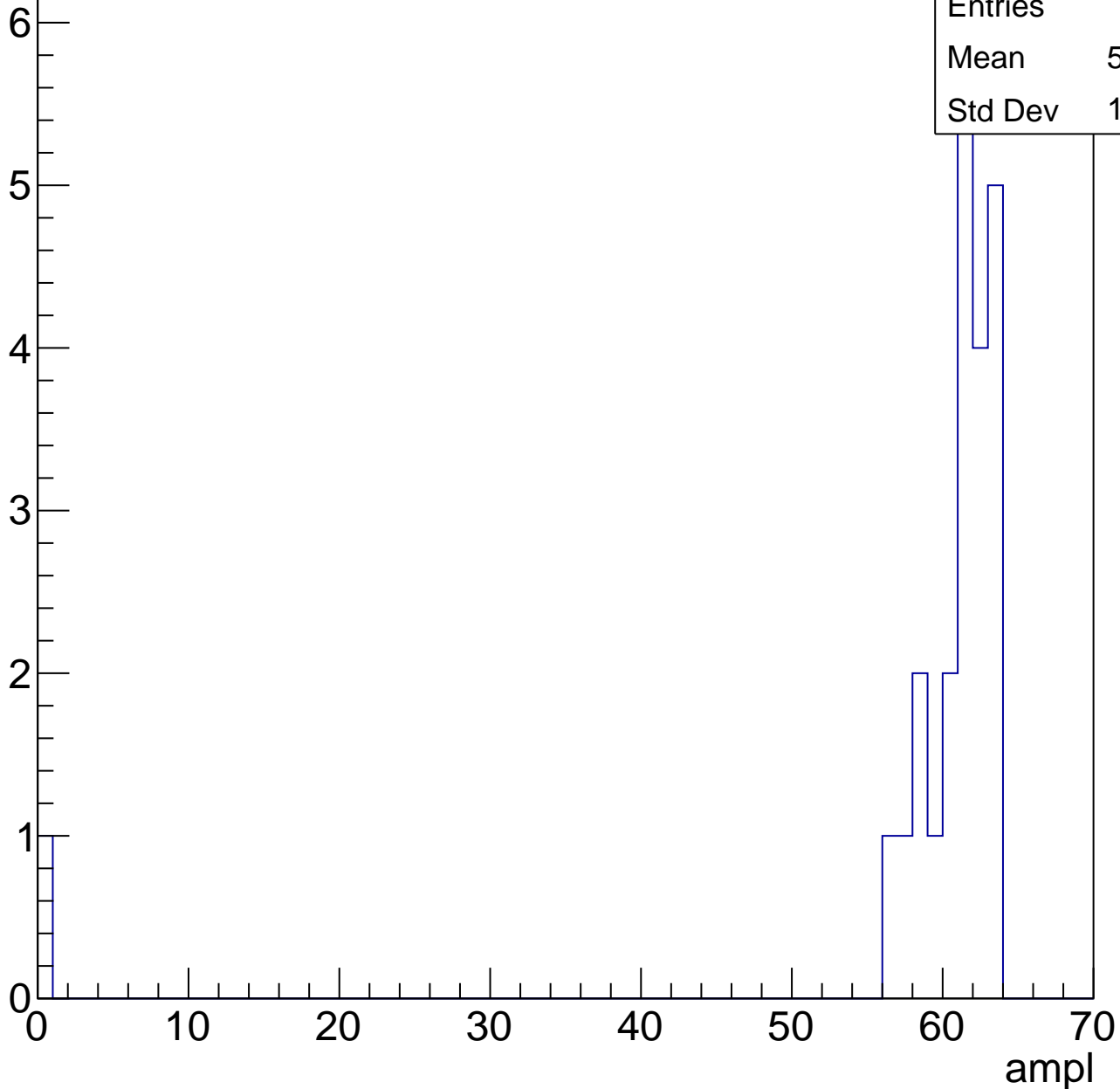


B1L103S, U5-ch90, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	23
Mean	58.13
Std Dev	12.55

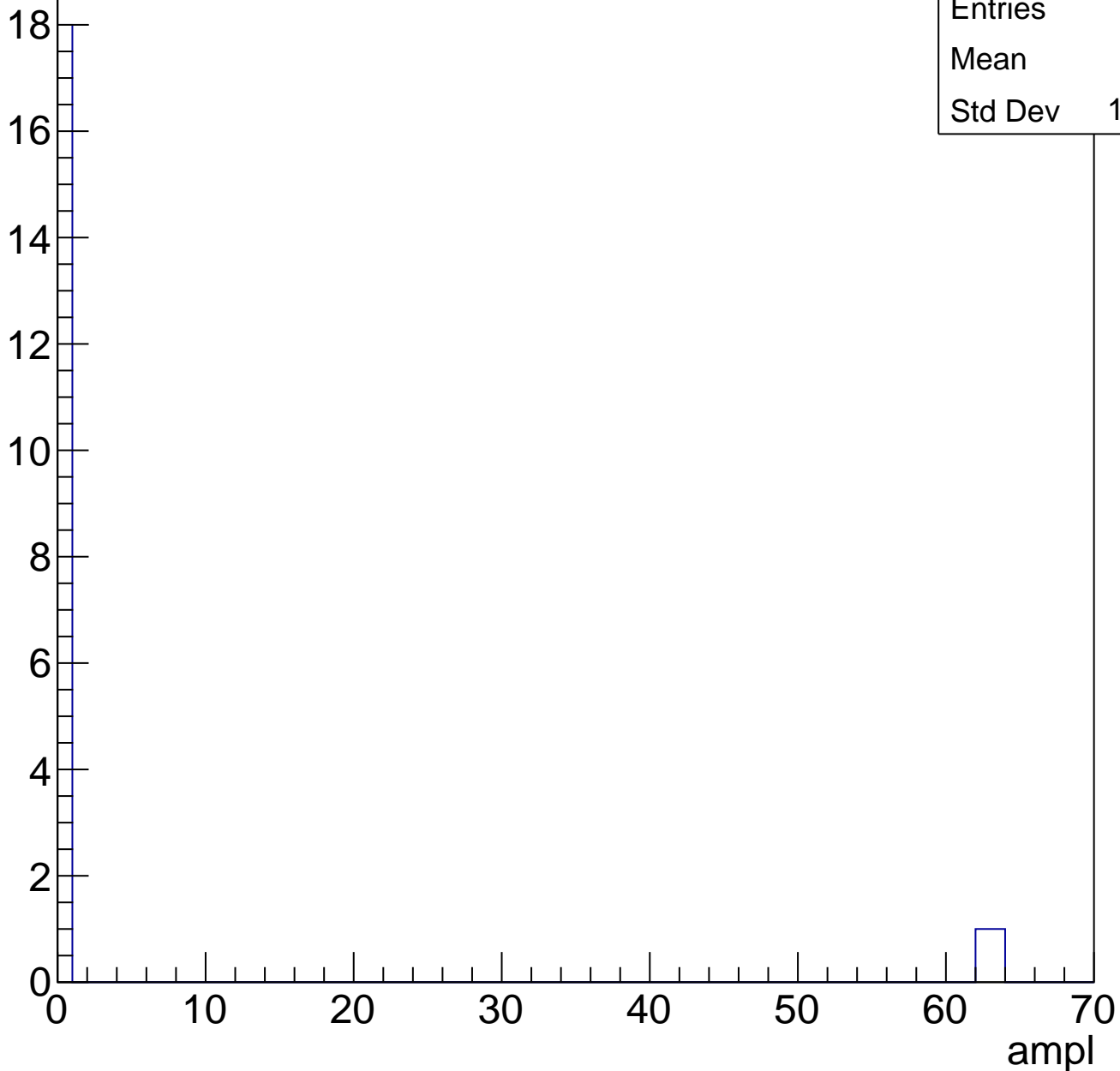


B1L103S, U5-ch90, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	6.25
Std Dev	18.75

Entry



B1L103S, U5-ch91, adc0

calib_packv5_041523_1651.root, FC#0, port C2

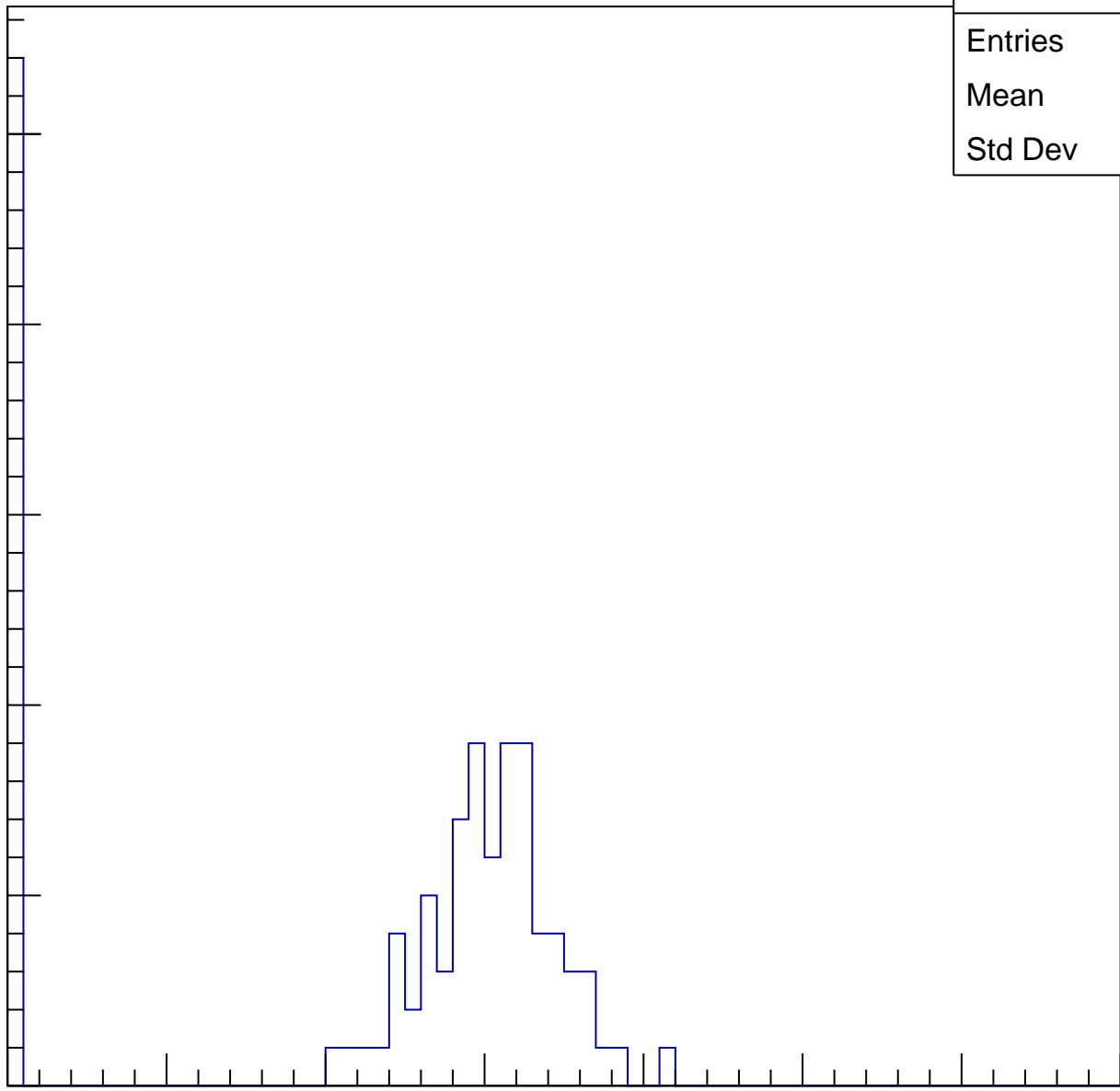
Entries	102
Mean	22
Std Dev	13.64

Entry

25
20
15
10
5
0

0 10 20 30 40 50 60 70

ampl

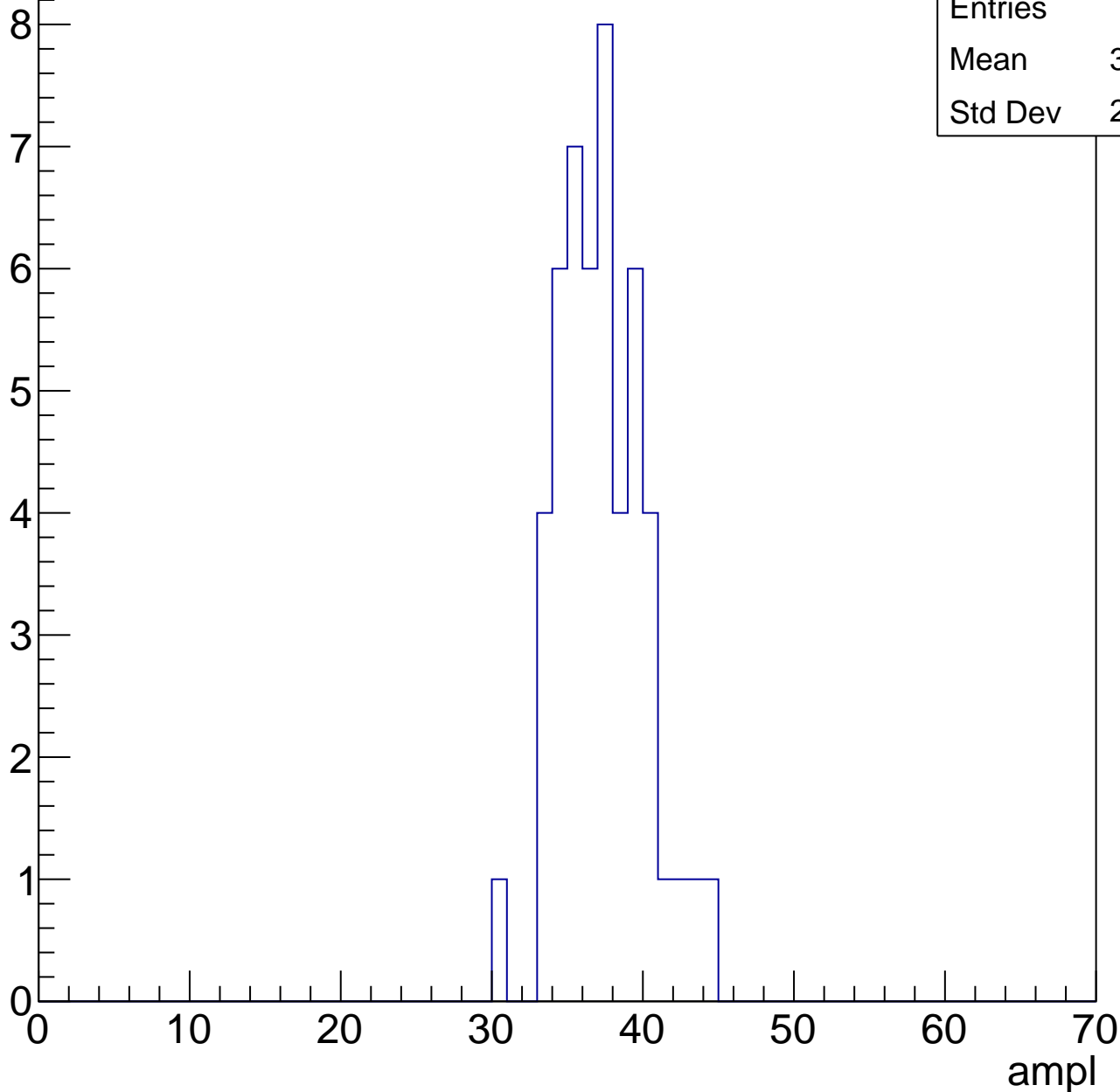


B1L103S, U5-ch91, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	36.78
Std Dev	2.788

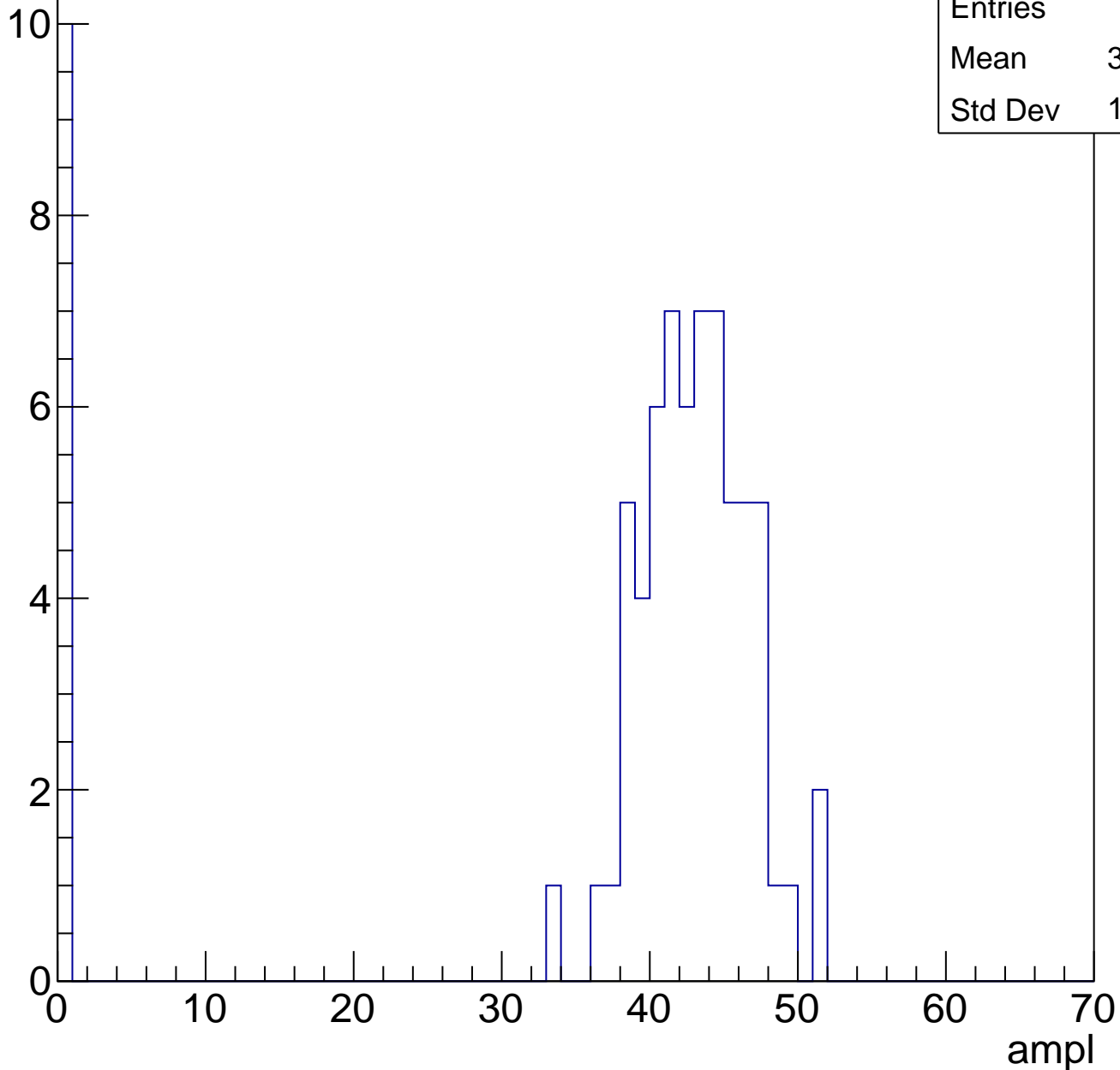


B1L103S, U5-ch91, adc2

calib_packv5_041523_1651.root, FC#0, port C2

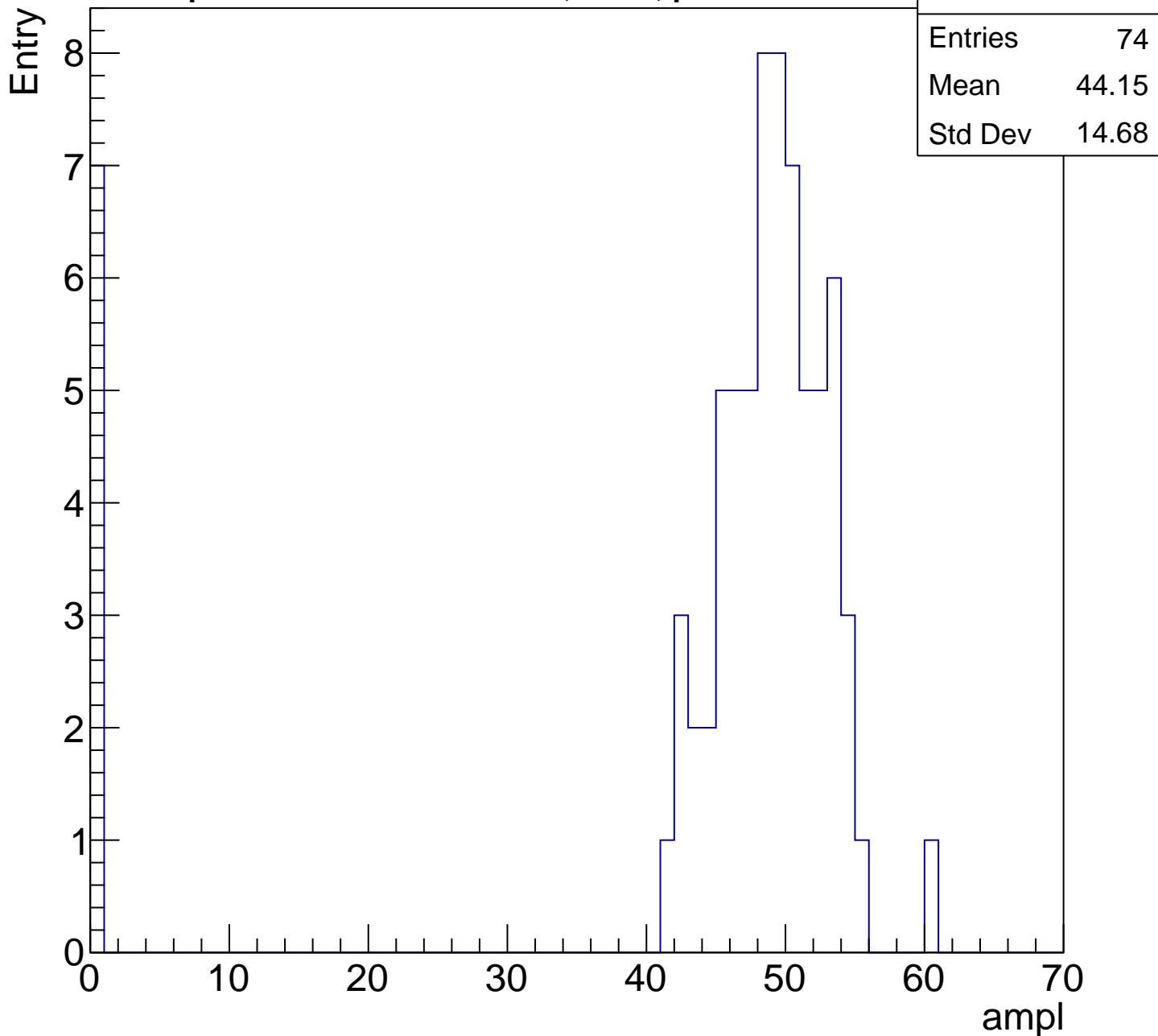
Entries	74
Mean	36.88
Std Dev	14.94

Entry



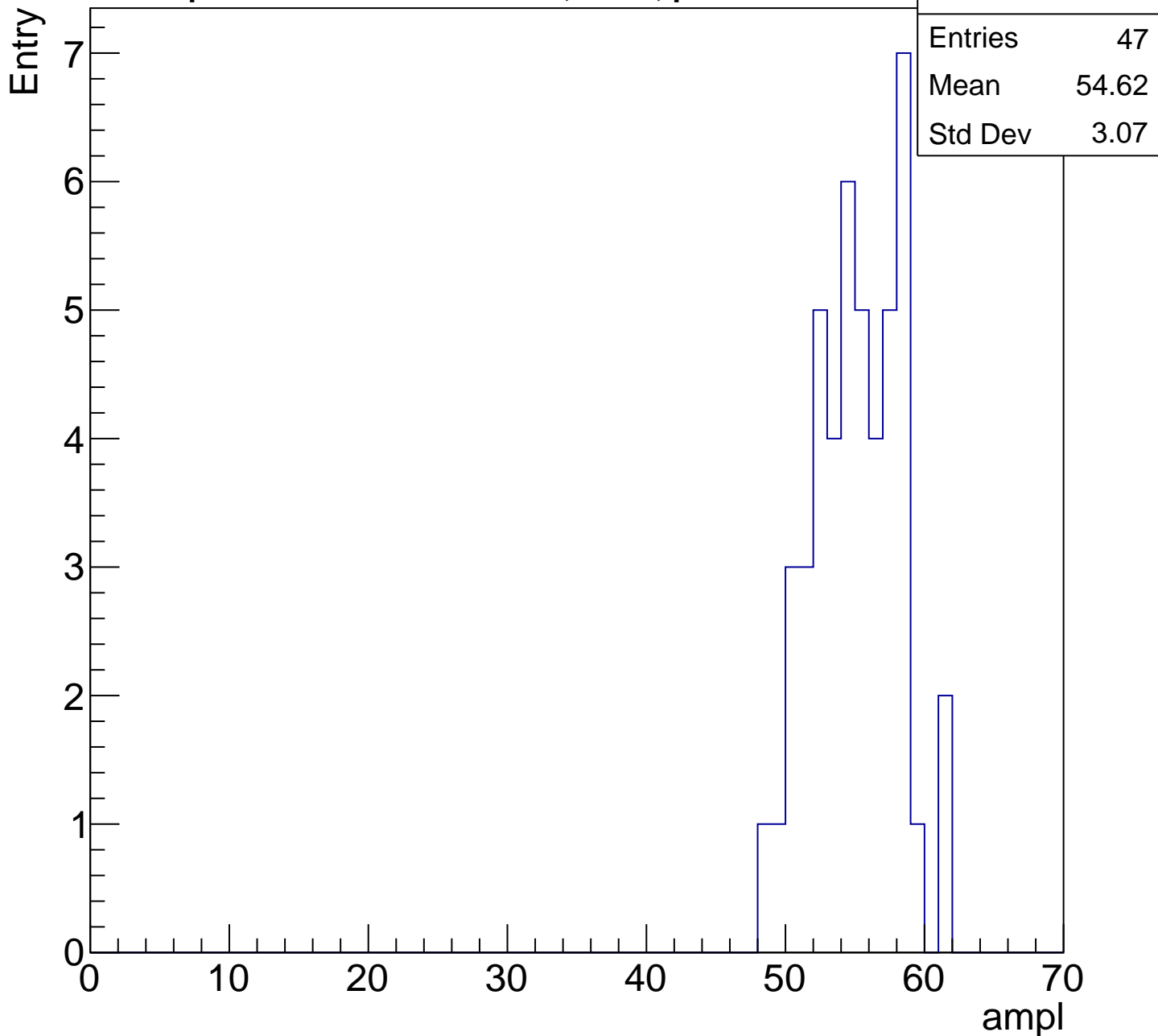
B1L103S, U5-ch91, adc3

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U5-ch91, adc4

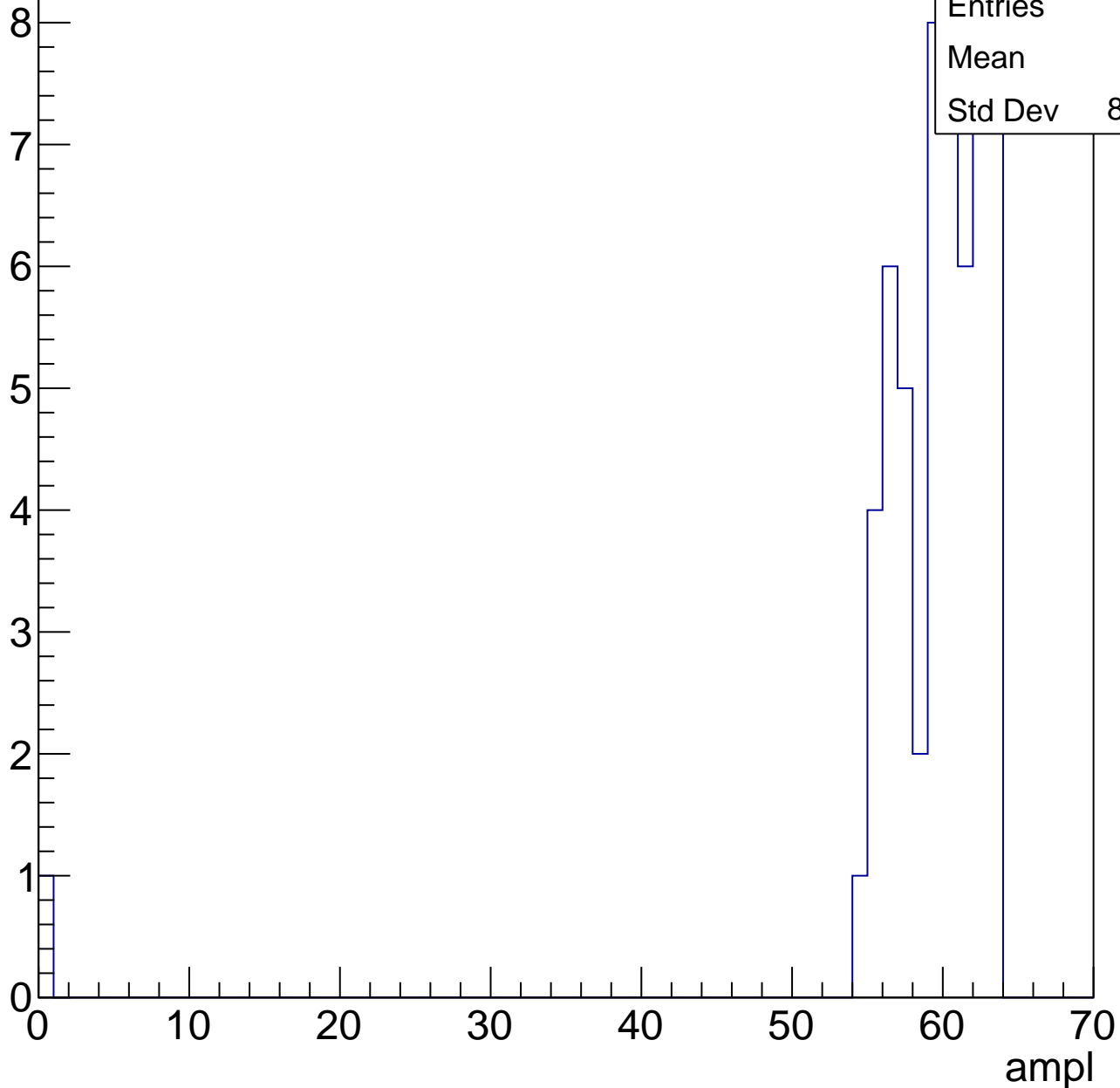
calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U5-ch91, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch91, adc6

calib_packv5_041523_1651.root, FC#0, port C2

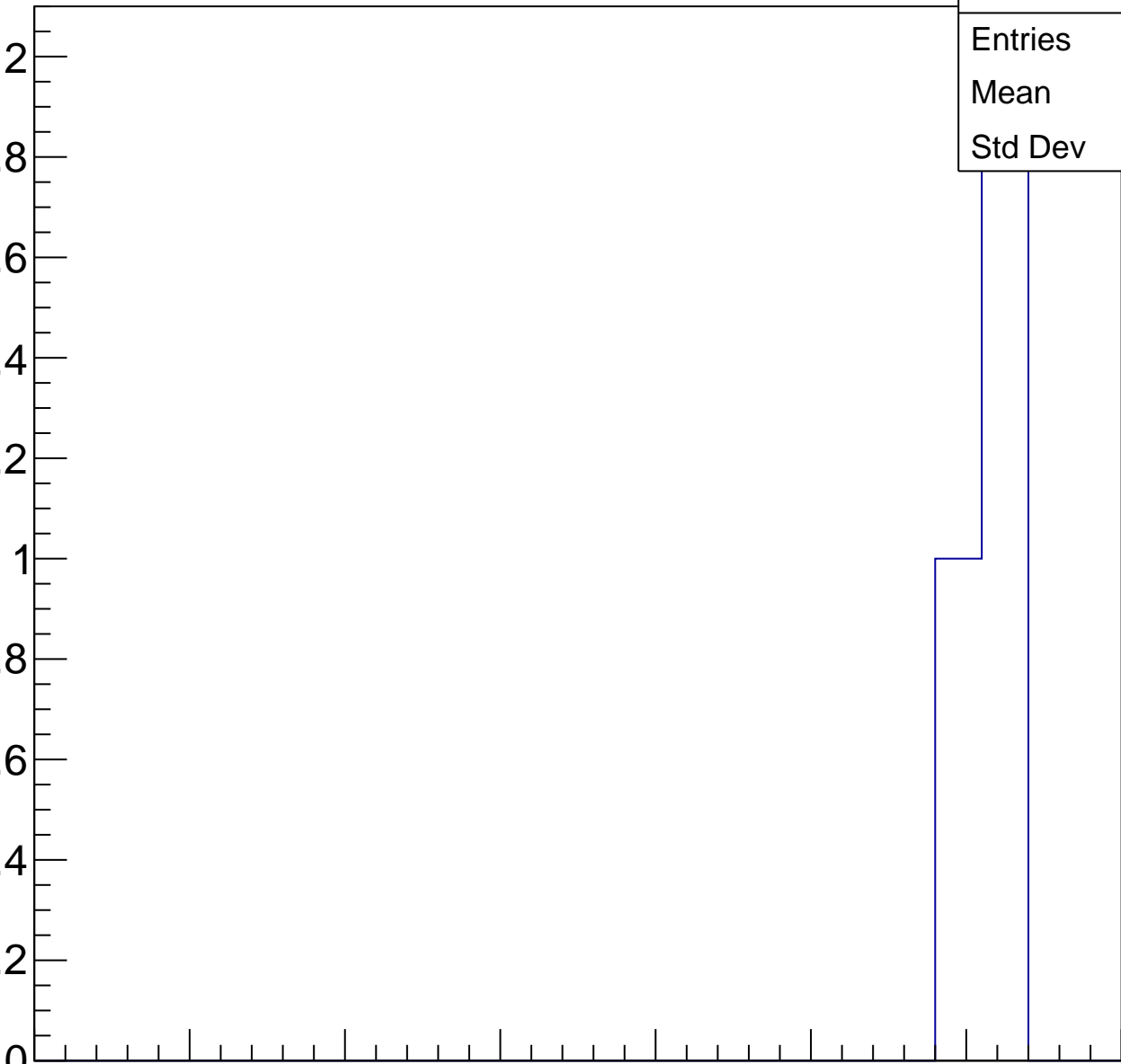
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	9
Mean	61
Std Dev	1.633

ampl

0 10 20 30 40 50 60 70



B1L103S, U5-ch91, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U5-ch92, adc0

calib_packv5_041523_1651.root, FC#0, port C2

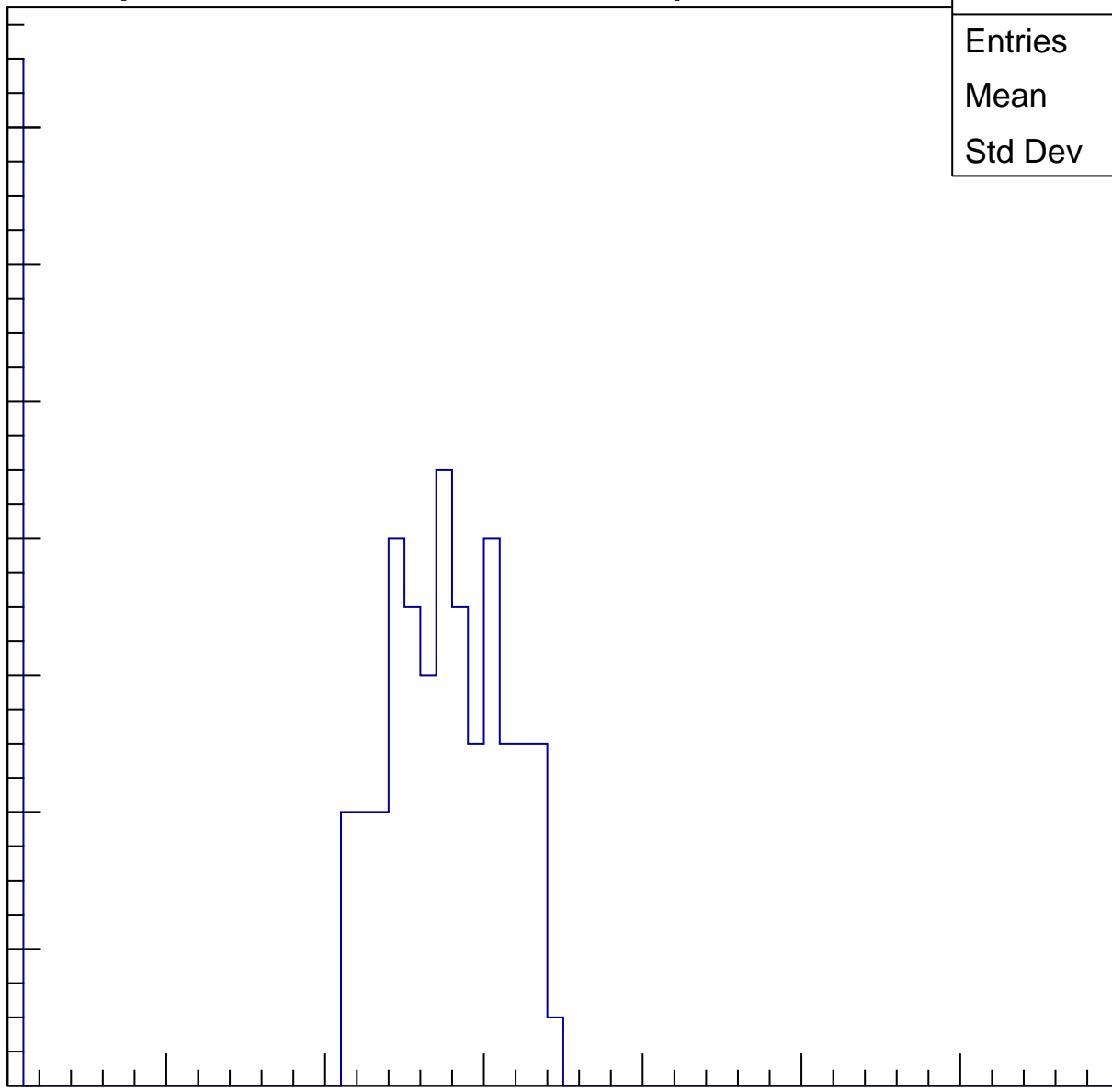
Entries	93
Mean	22.85
Std Dev	10.51

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl



B1L103S, U5-ch92, adc1

calib_packv5_041523_1651.root, FC#0, port C2

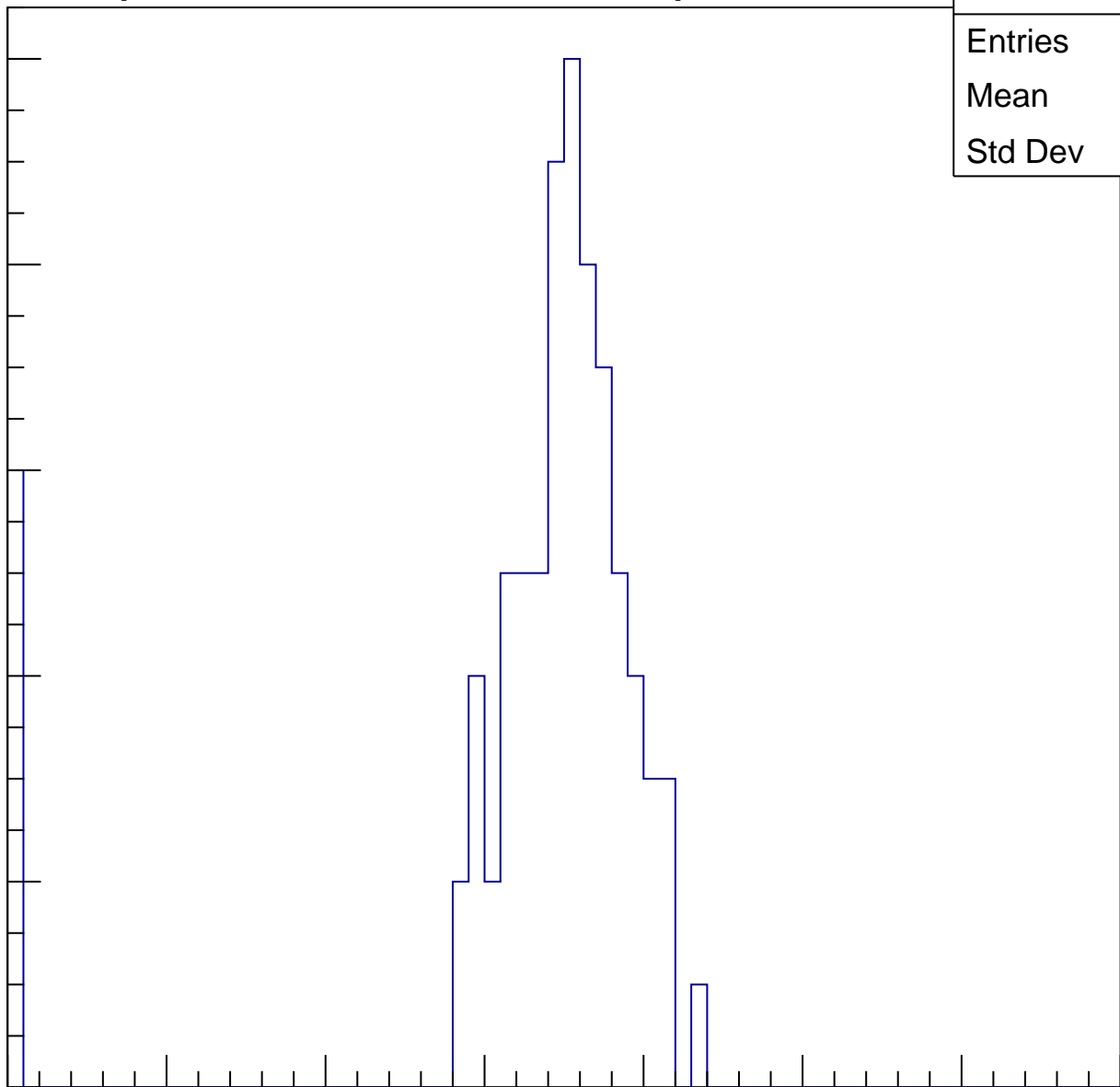
Entries	79
Mean	32.24
Std Dev	9.8

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

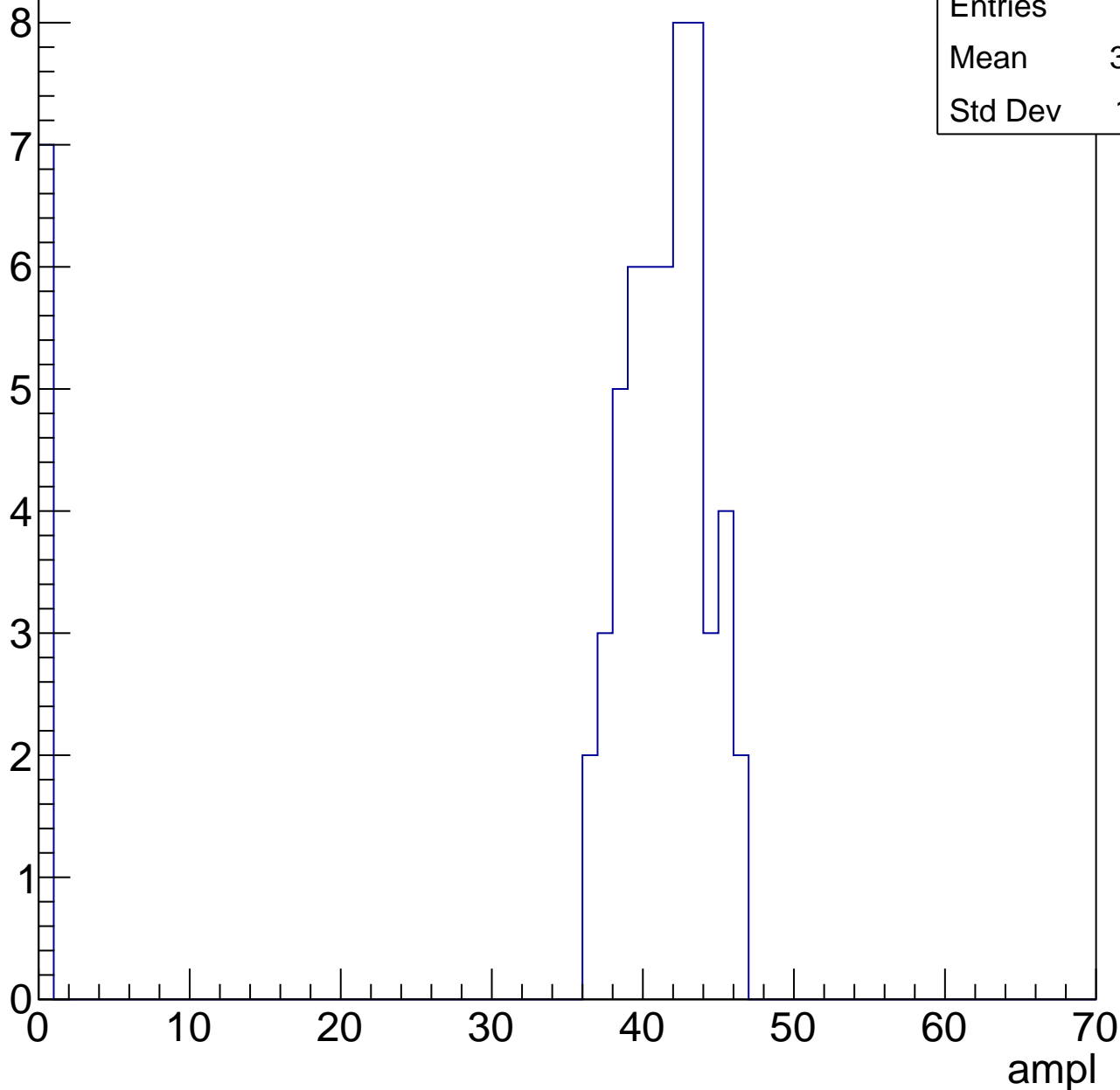


B1L103S, U5-ch92, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	36.28
Std Dev	13.41

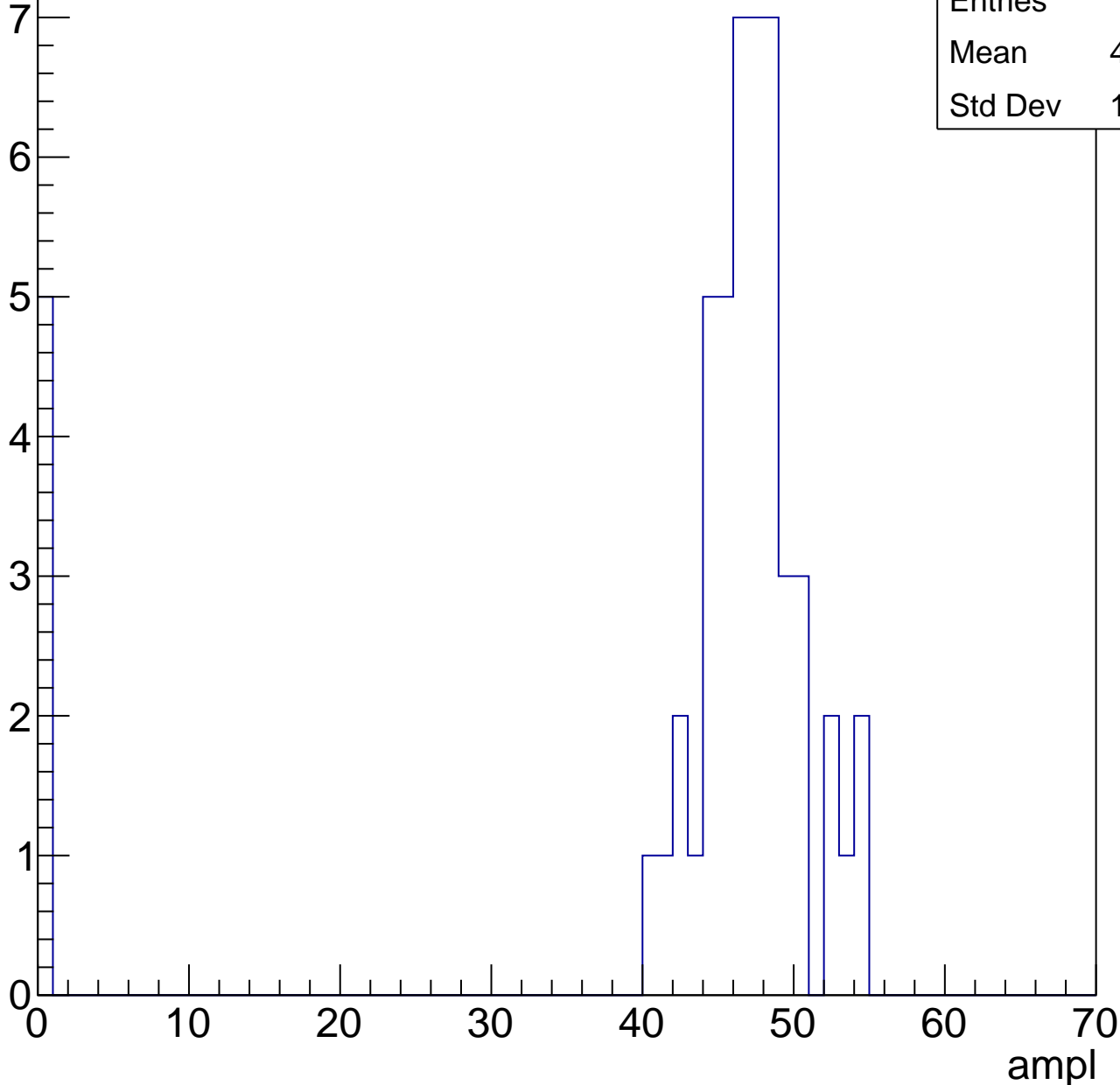


B1L103S, U5-ch92, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	42.35
Std Dev	14.12

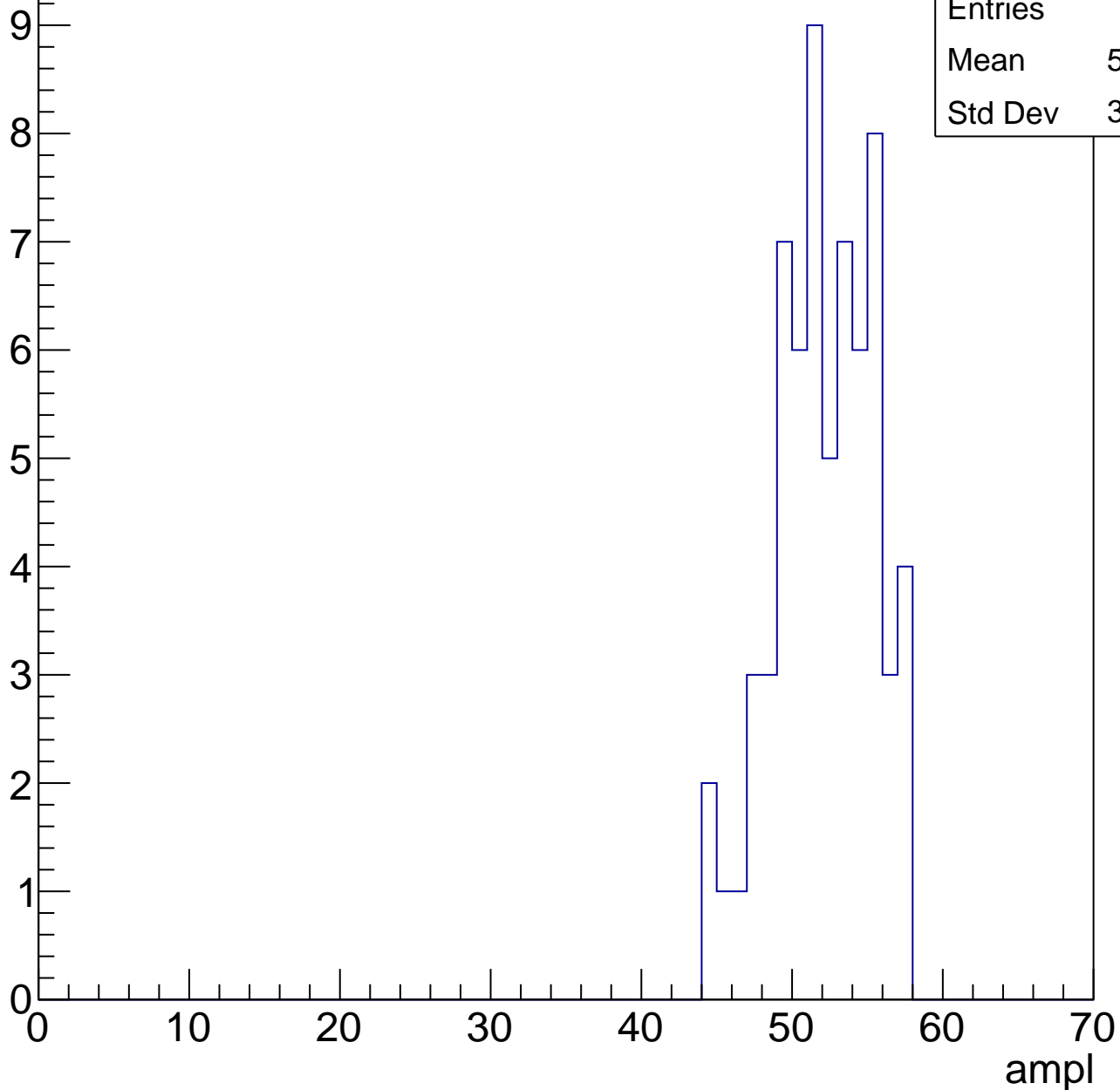


B1L103S, U5-ch92, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	51.65
Std Dev	3.222



B1L103S, U5-ch92, adc5

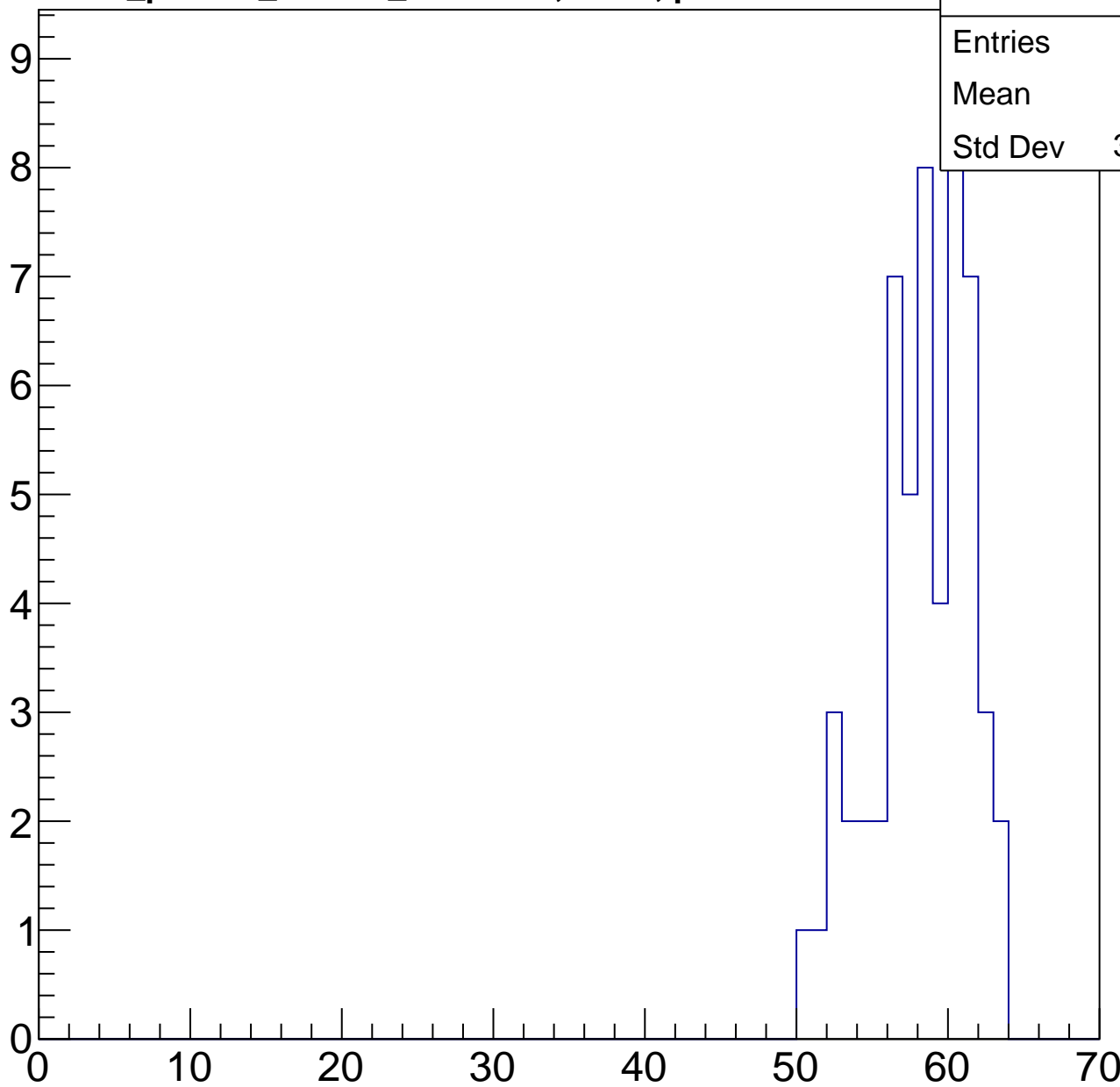
calib_packv5_041523_1651.root, FC#0, port C2

Entry

9
8
7
6
5
4
3
2
1
0

Entries	56
Mean	57.8
Std Dev	3.142

ampl

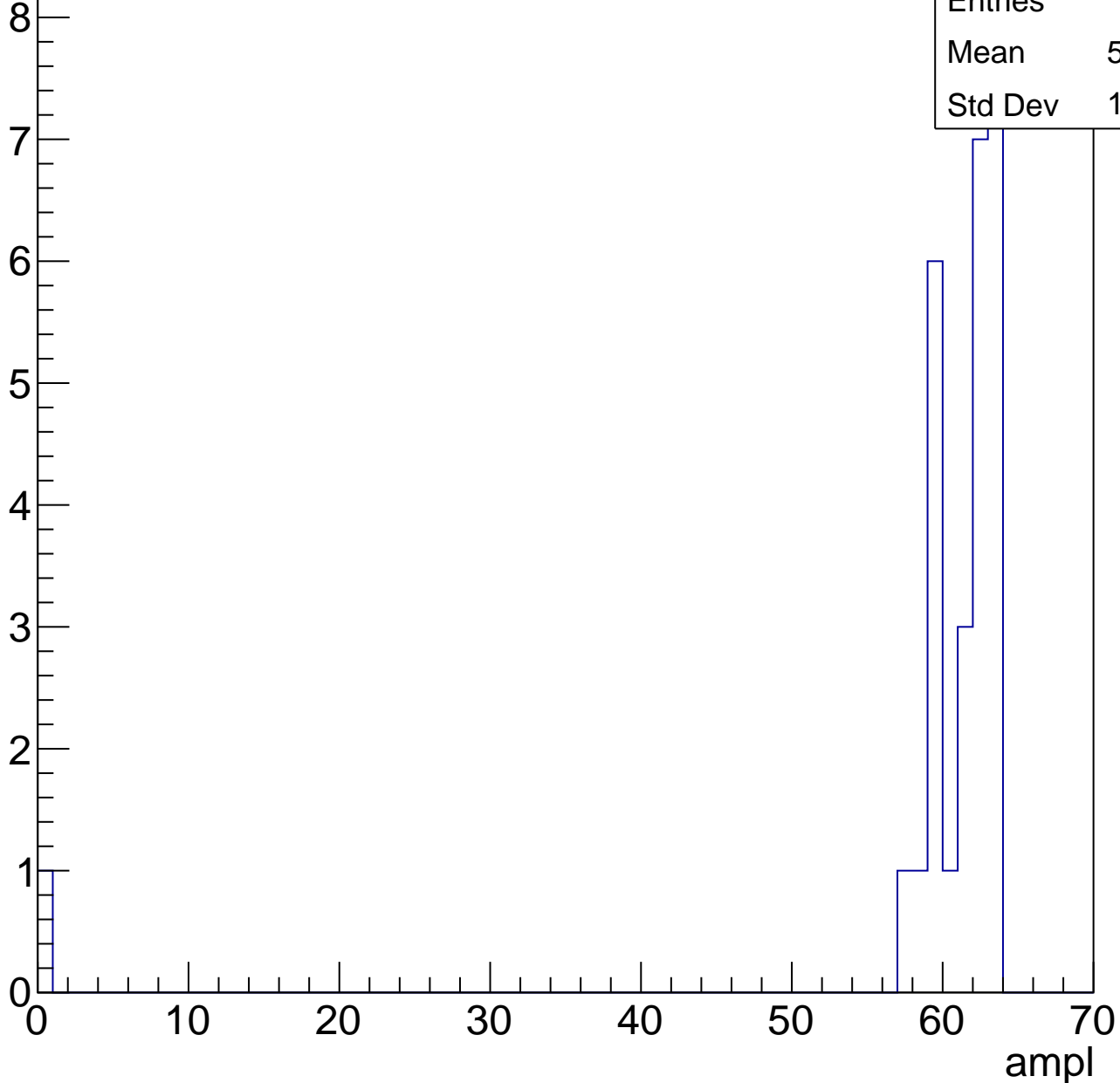


B1L103S, U5-ch92, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

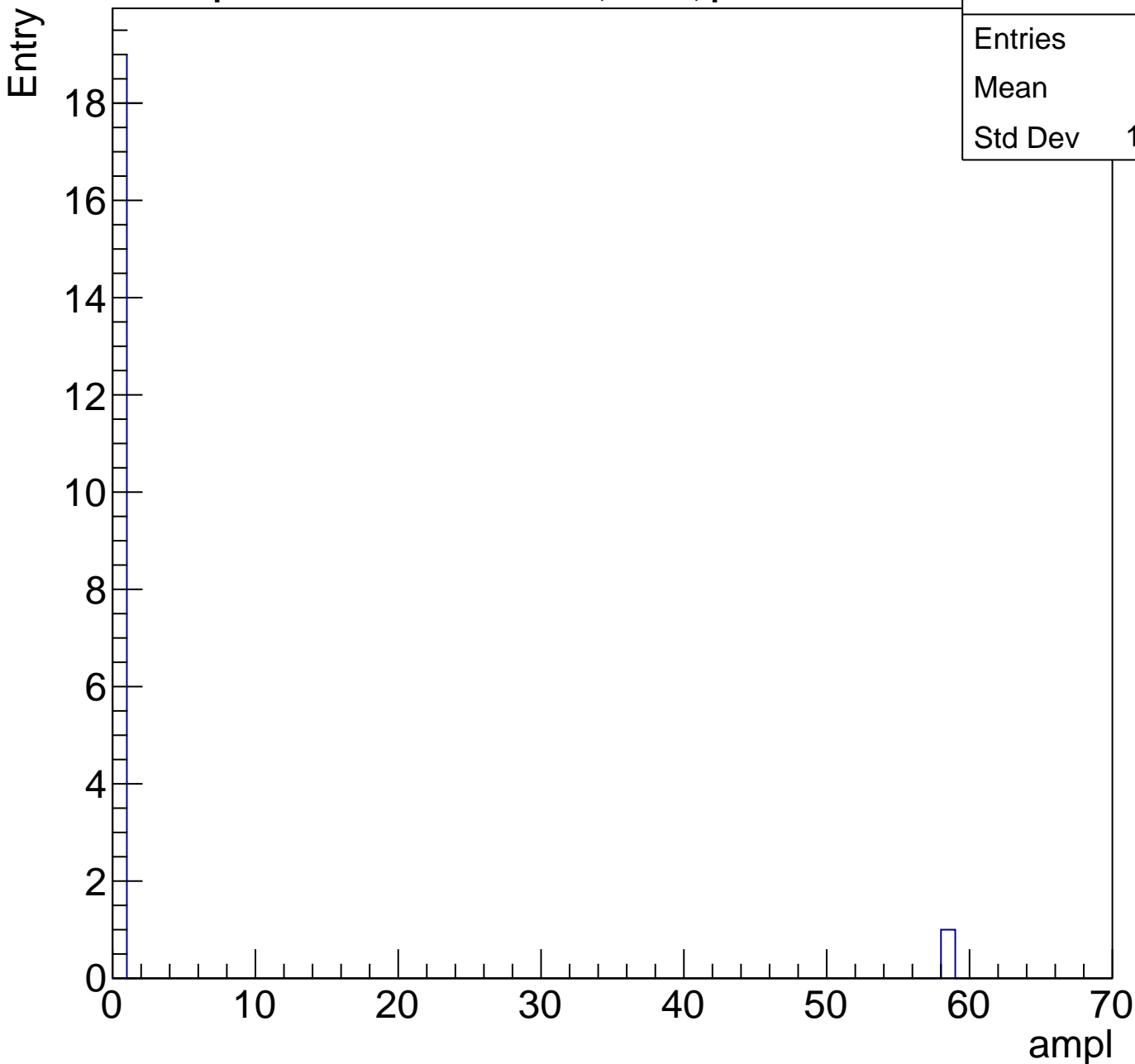
Entries	28
Mean	58.93
Std Dev	11.48



B1L103S, U5-ch92, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	2.9
Std Dev	12.64



B1L103S, U5-ch93, adc0

calib_packv5_041523_1651.root, FC#0, port C2

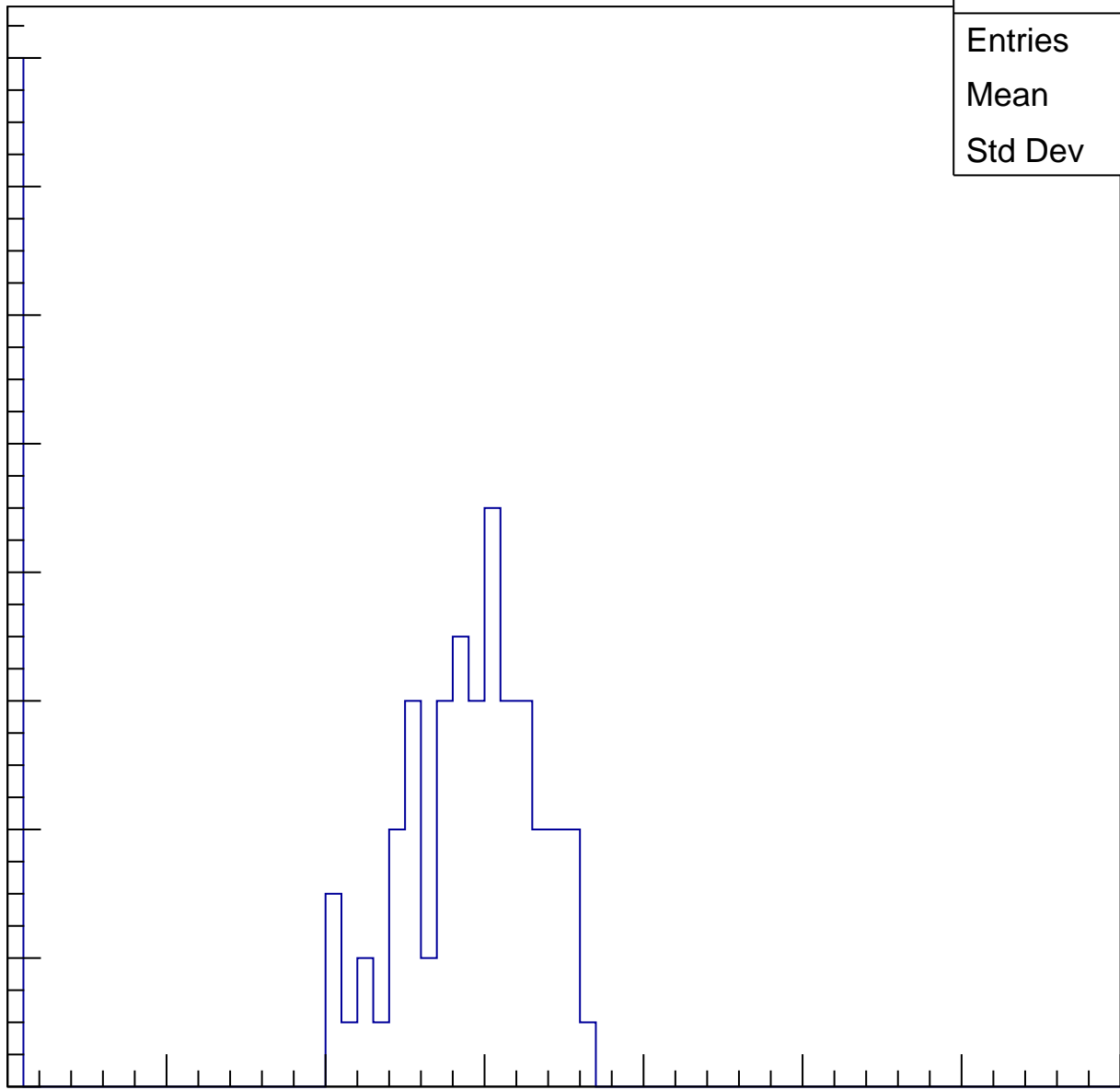
Entries	88
Mean	23.52
Std Dev	11.65

Entry

16
14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

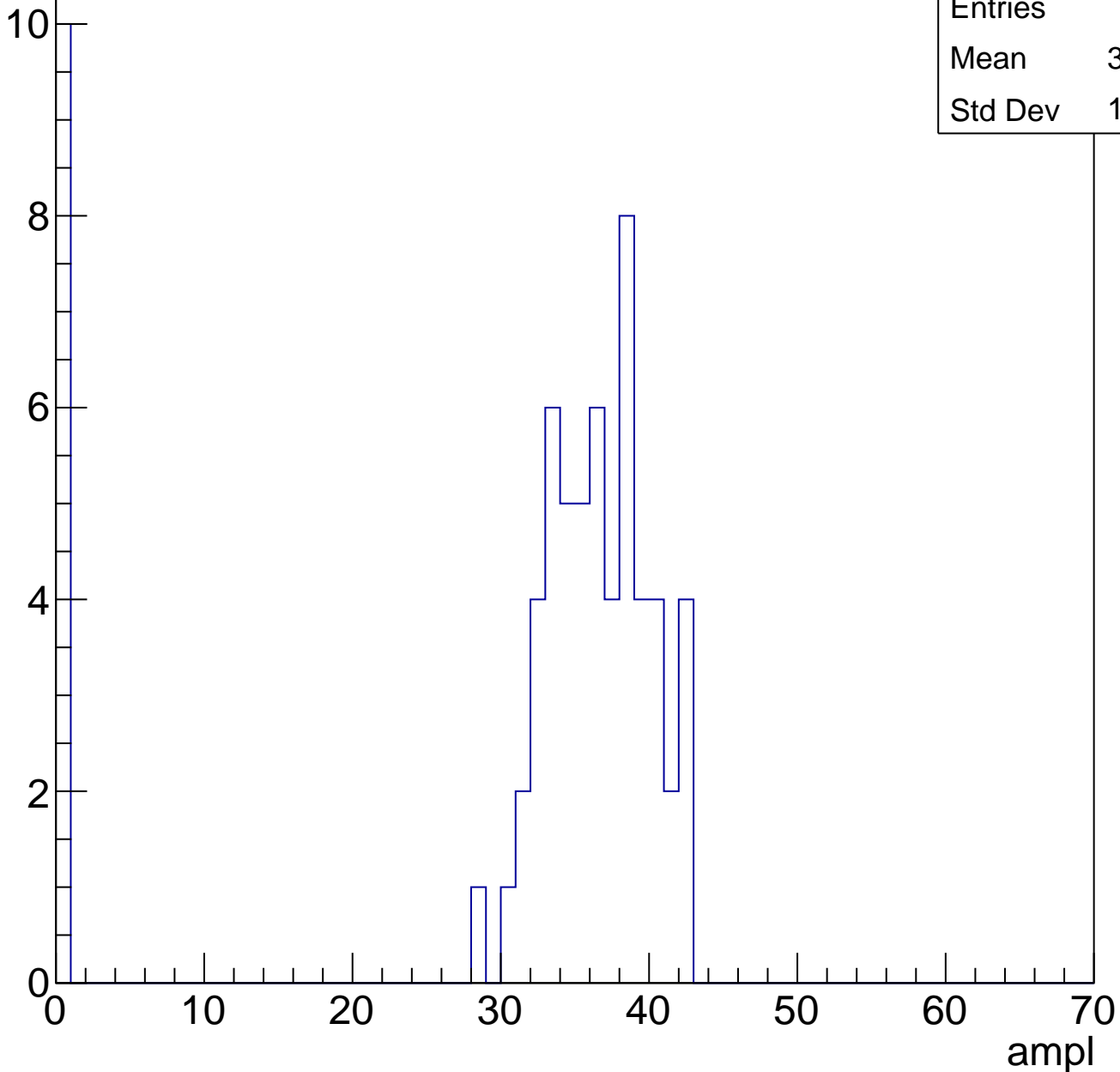


B1L103S, U5-ch93, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	66
Mean	30.68
Std Dev	13.32

Entry

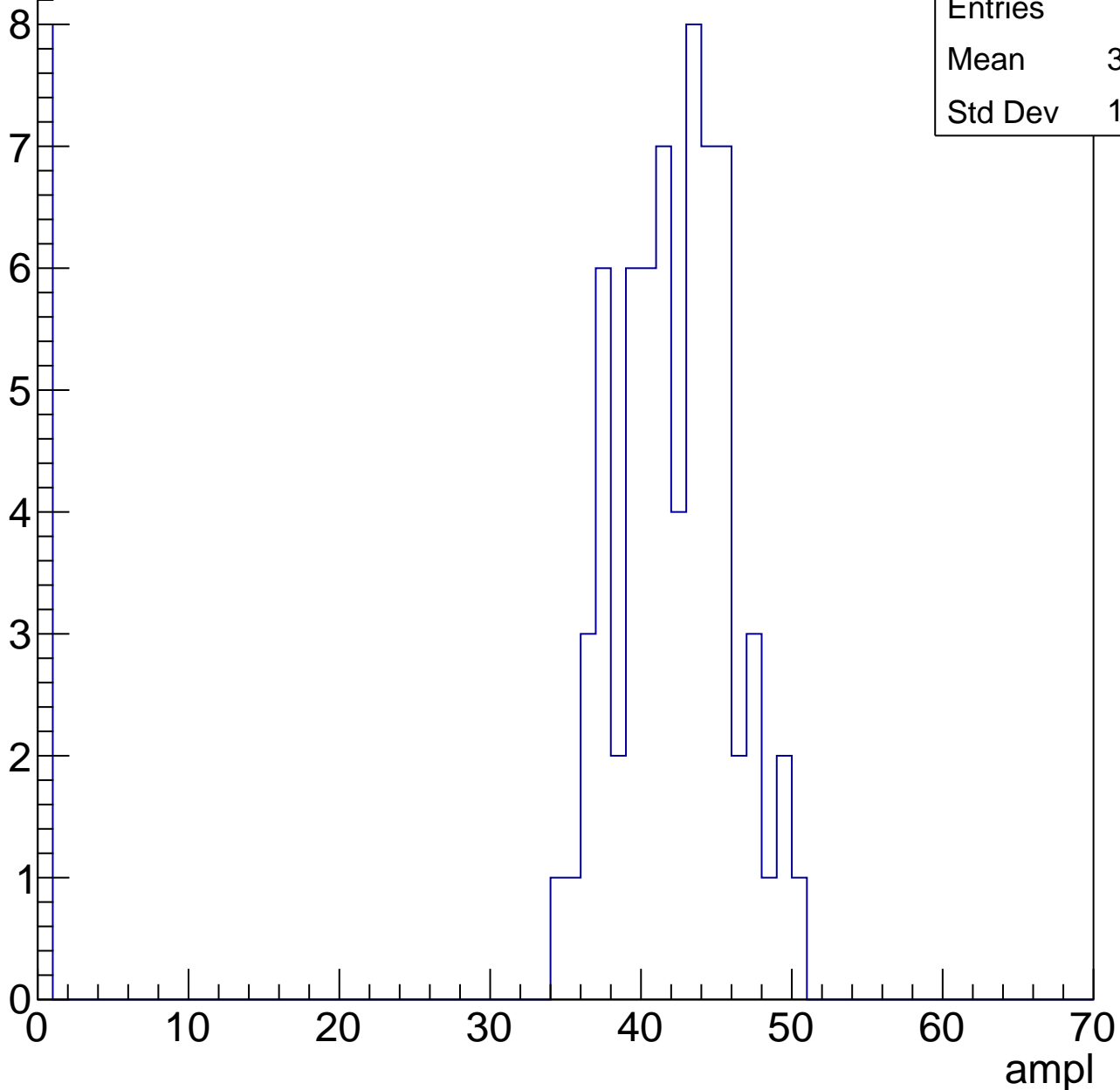


B1L103S, U5-ch93, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

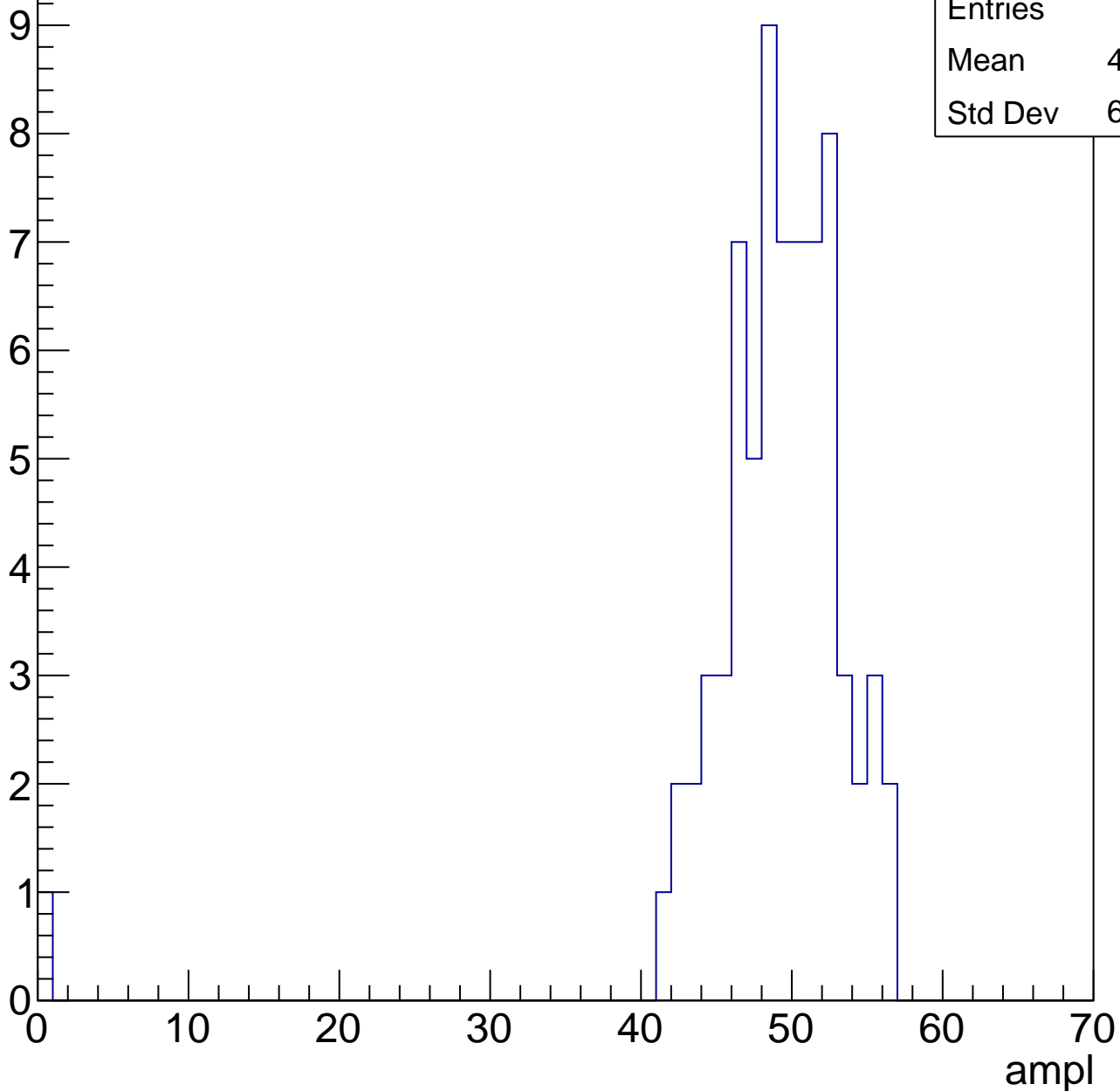
Entries	75
Mean	37.33
Std Dev	13.35



B1L103S, U5-ch93, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry



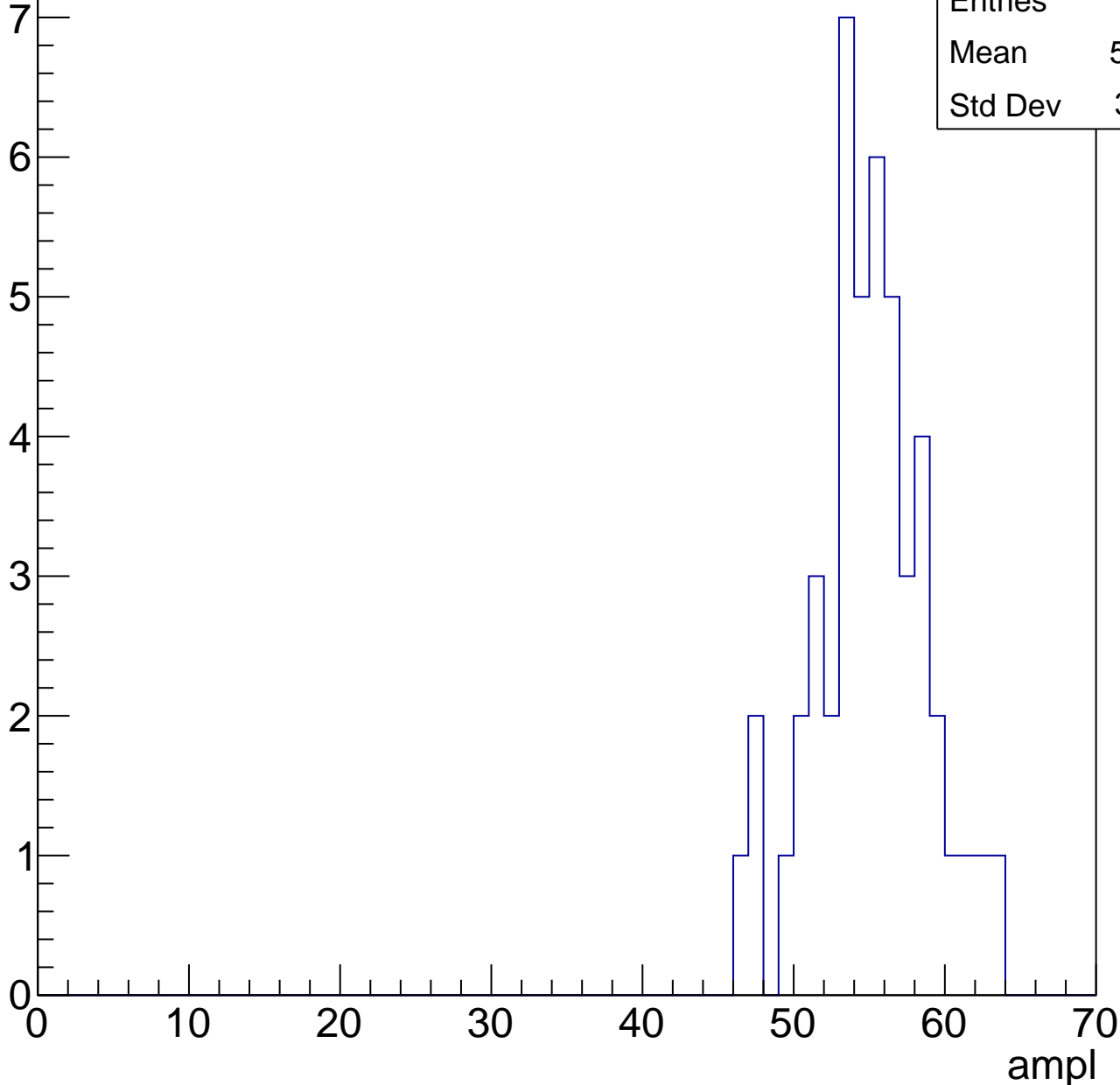
Entries	72
Mean	48.29
Std Dev	6.693

B1L103S, U5-ch93, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	47
Mean	54.55
Std Dev	3.701



B1L103S, U5-ch93, adc5

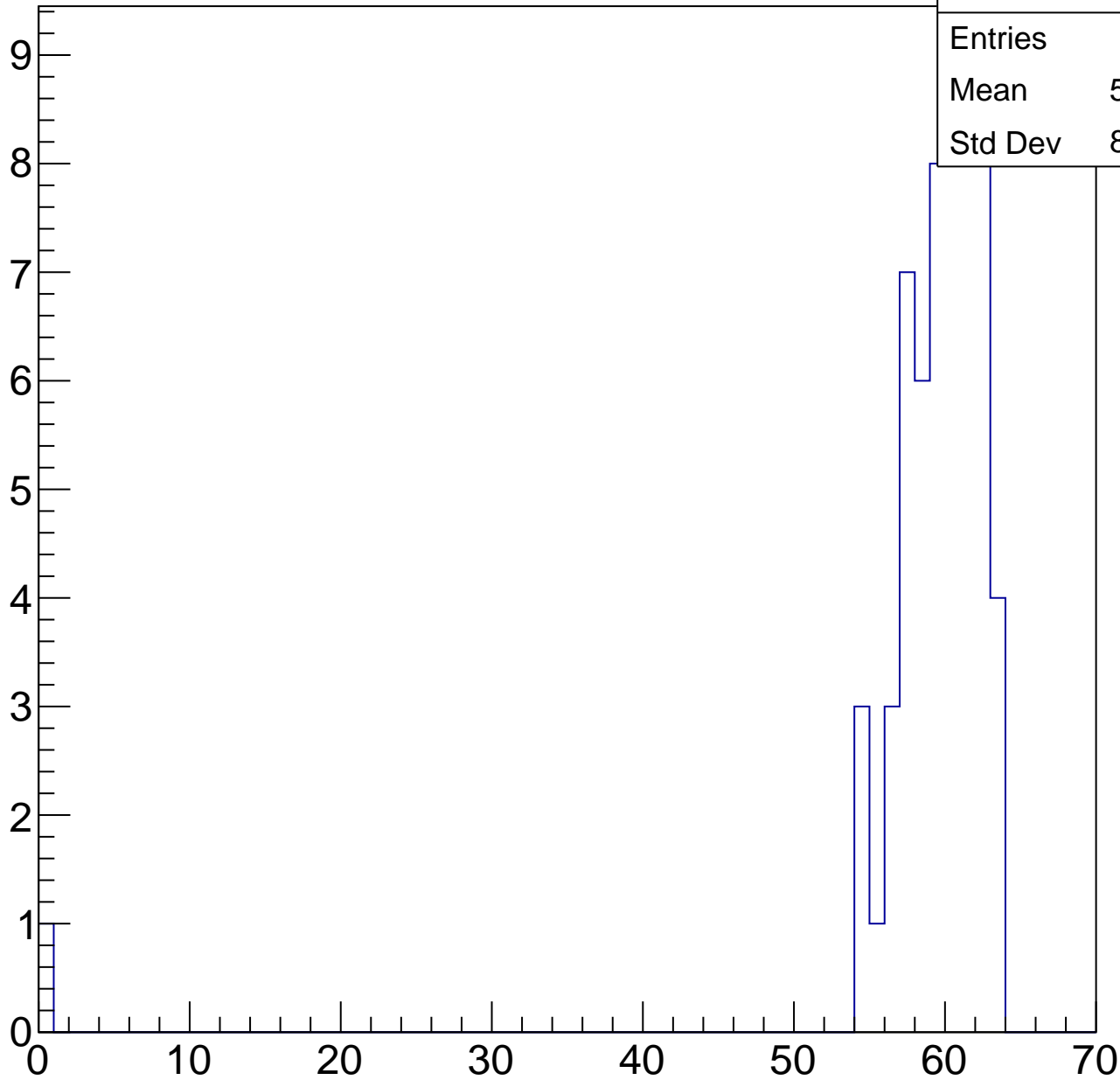
calib_packv5_041523_1651.root, FC#0, port C2

Entry

9
8
7
6
5
4
3
2
1
0

Entries	59
Mean	58.34
Std Dev	8.018

ampl

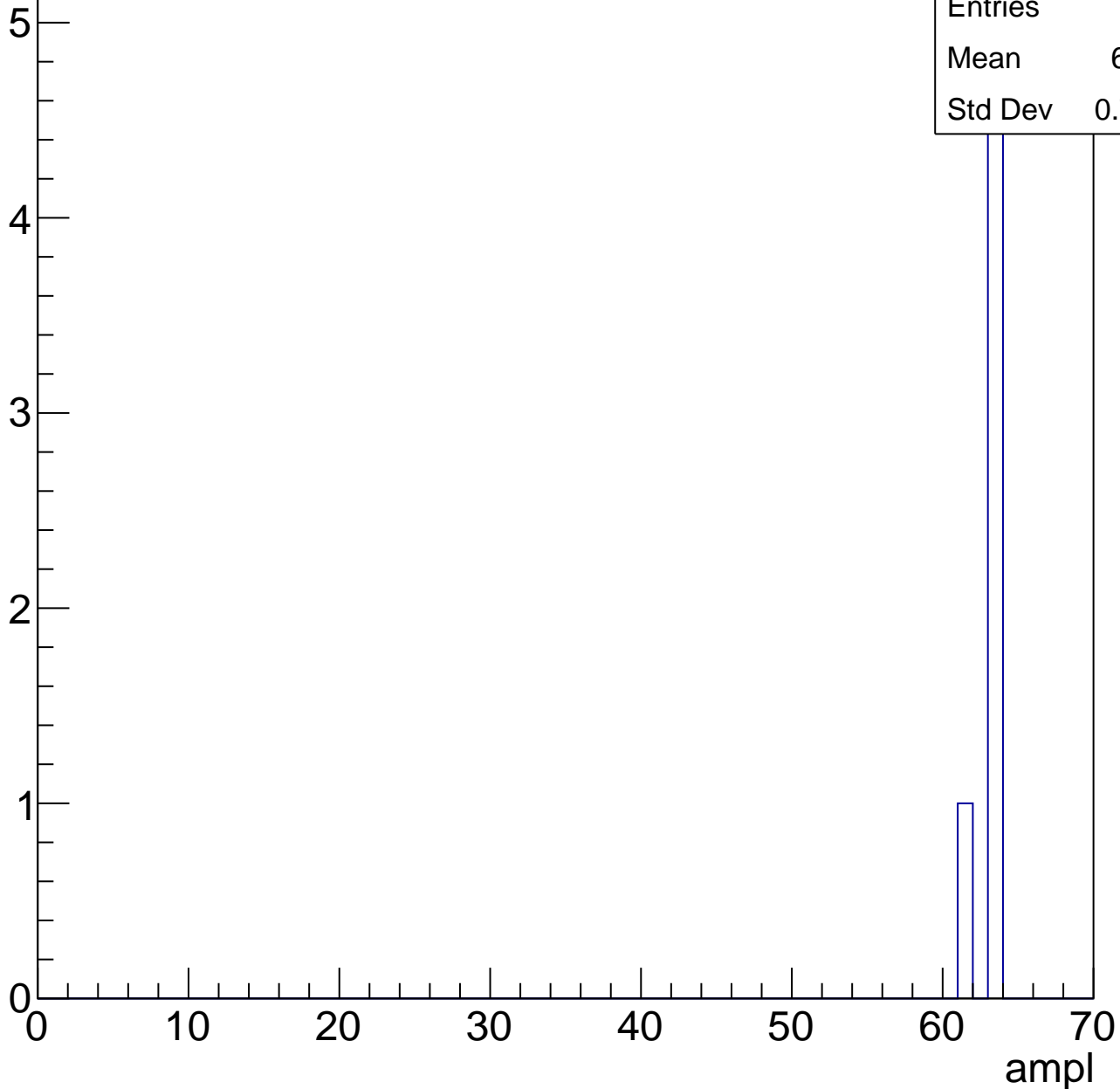


B1L103S, U5-ch93, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	6
Mean	62.67
Std Dev	0.7454



B1L103S, U5-ch93, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

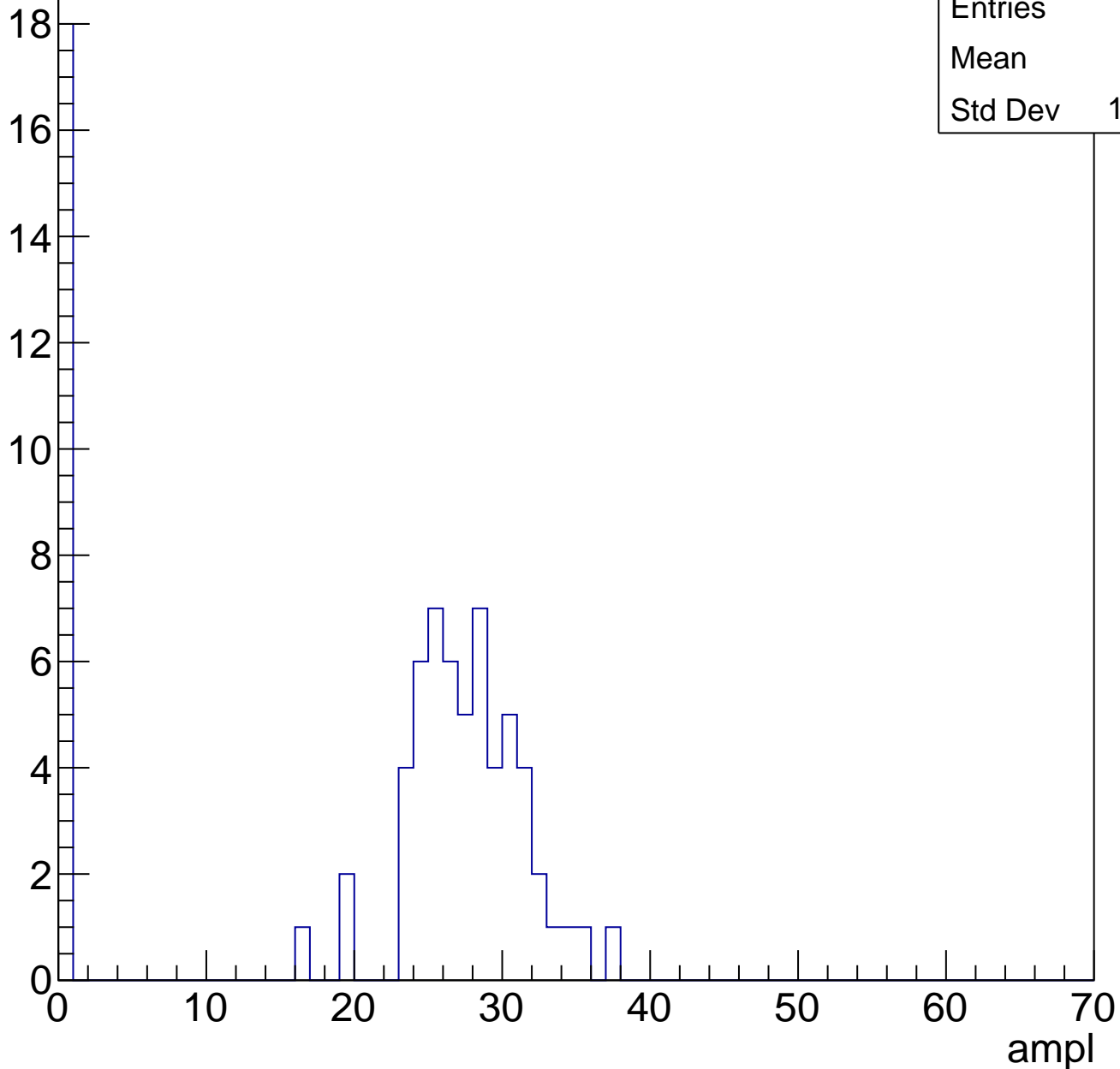


B1L103S, U5-ch94, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	20.6
Std Dev	12.05

Entry

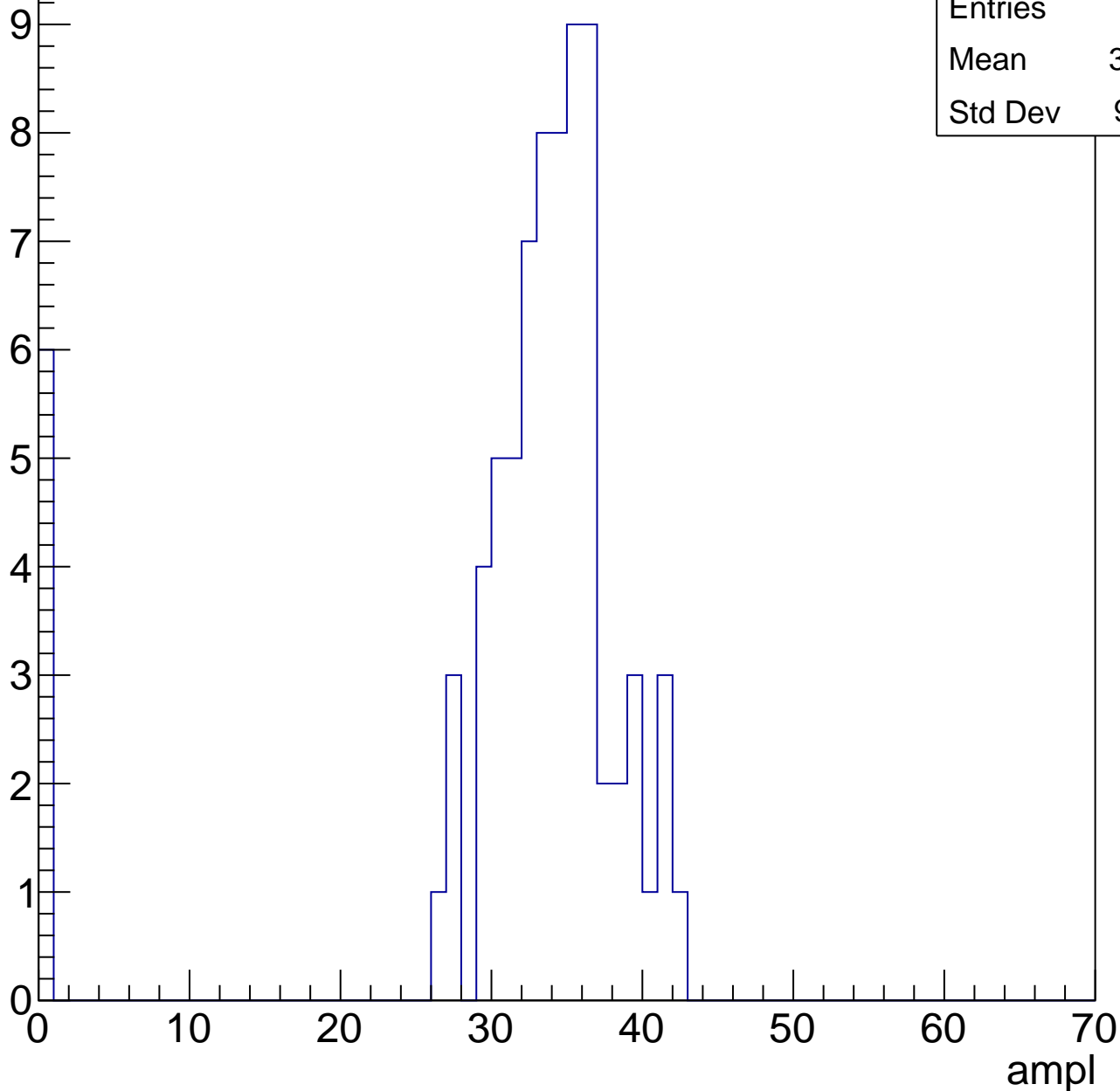


B1L103S, U5-ch94, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	31.16
Std Dev	9.671



B1L103S, U5-ch94, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	73
Mean	34.47
Std Dev	14.93

Entry

10

8

6

4

2

0

0

10

20

30

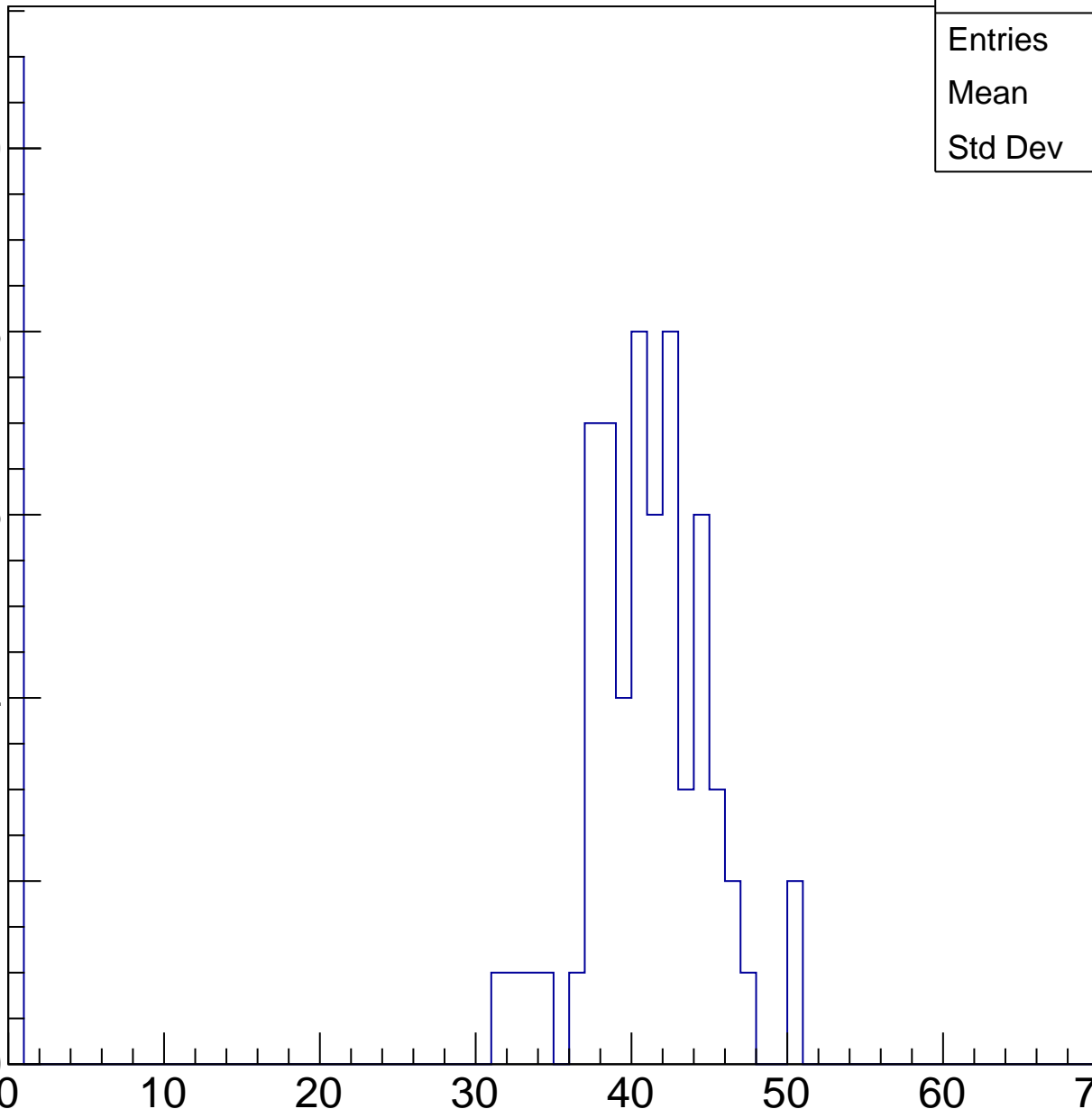
40

50

60

70

ampl

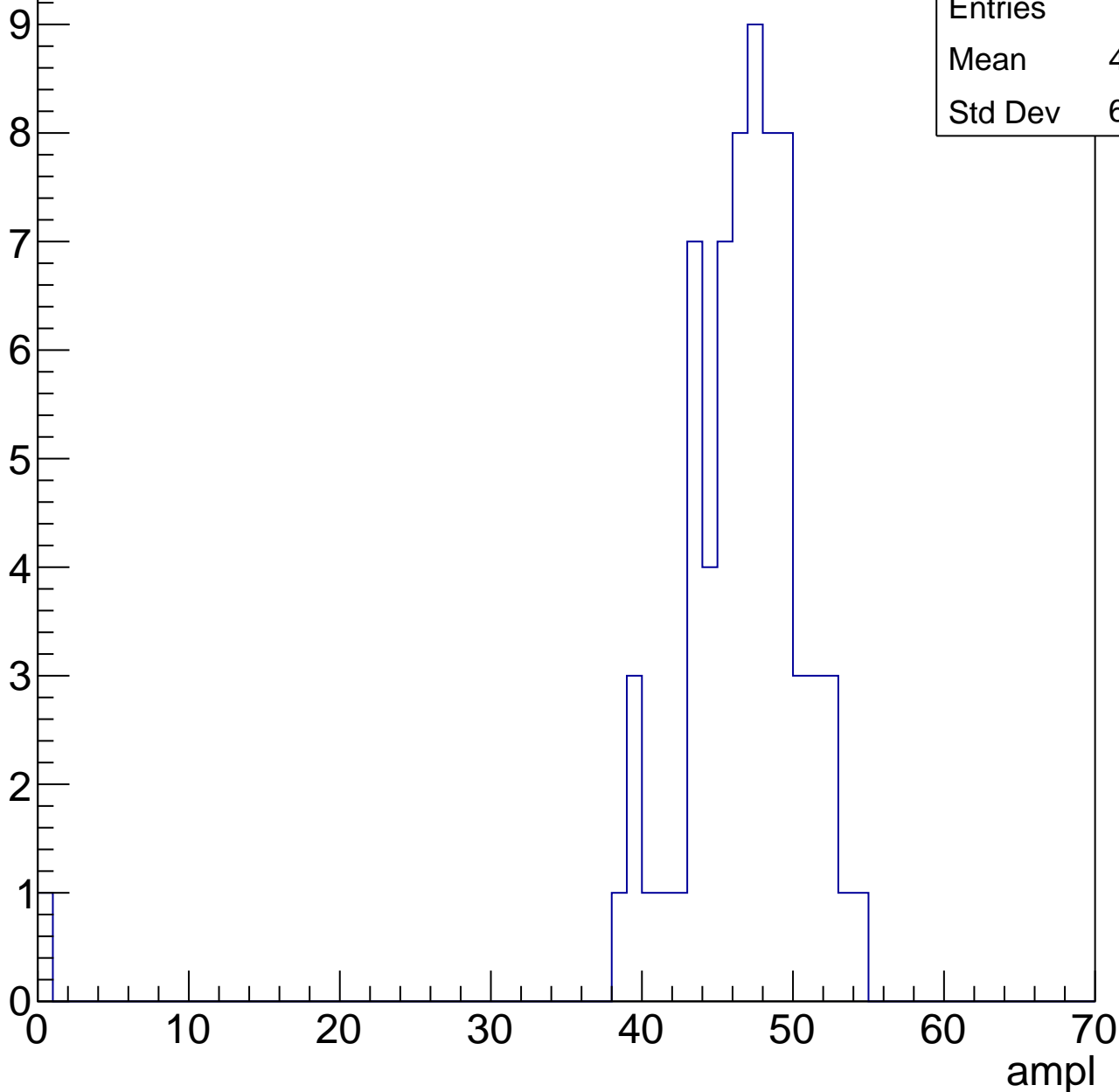


B1L103S, U5-ch94, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	45.76
Std Dev	6.484

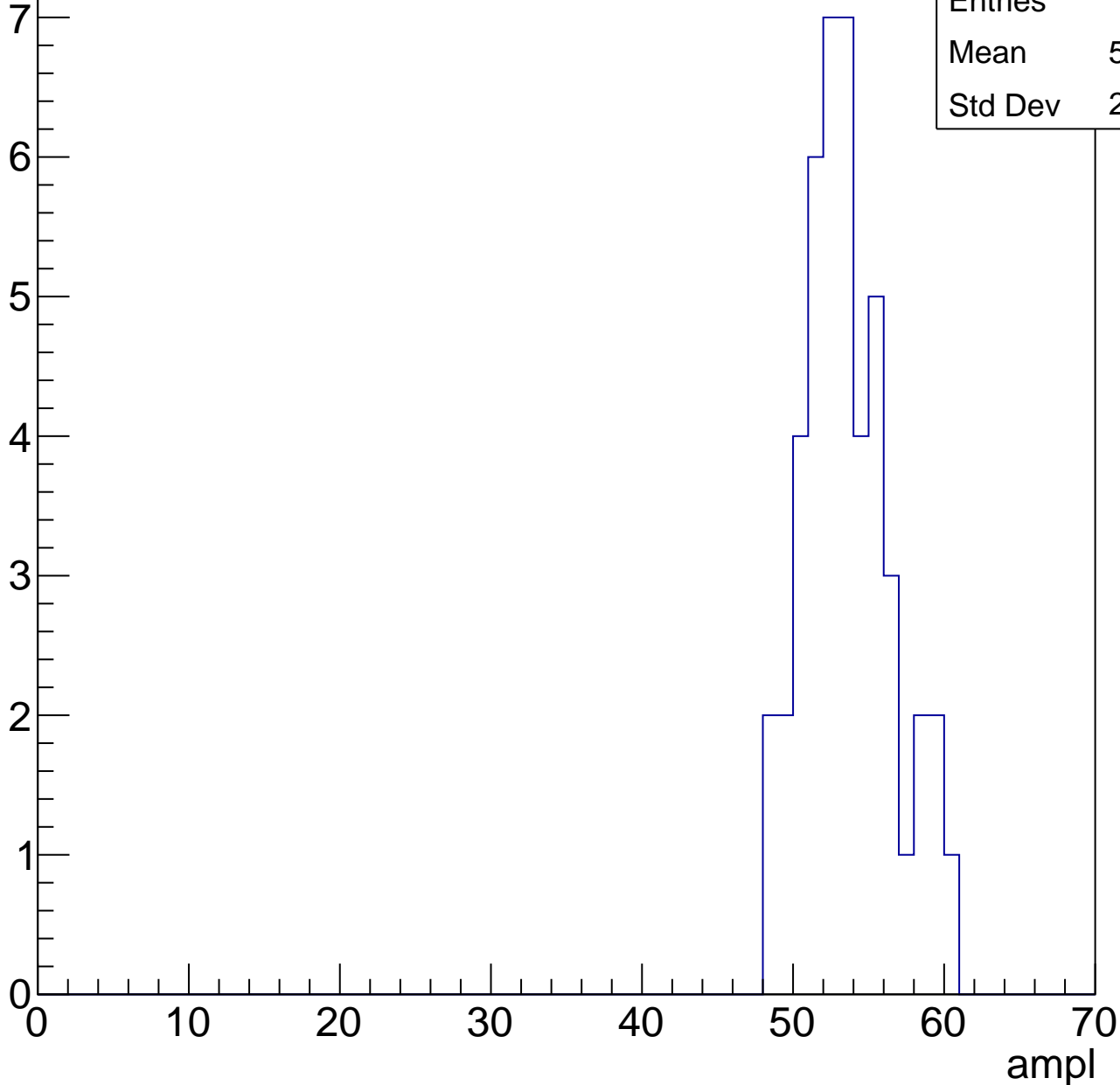


B1L103S, U5-ch94, adc4

calib_packv5_041523_1651.root, FC#0, port C2

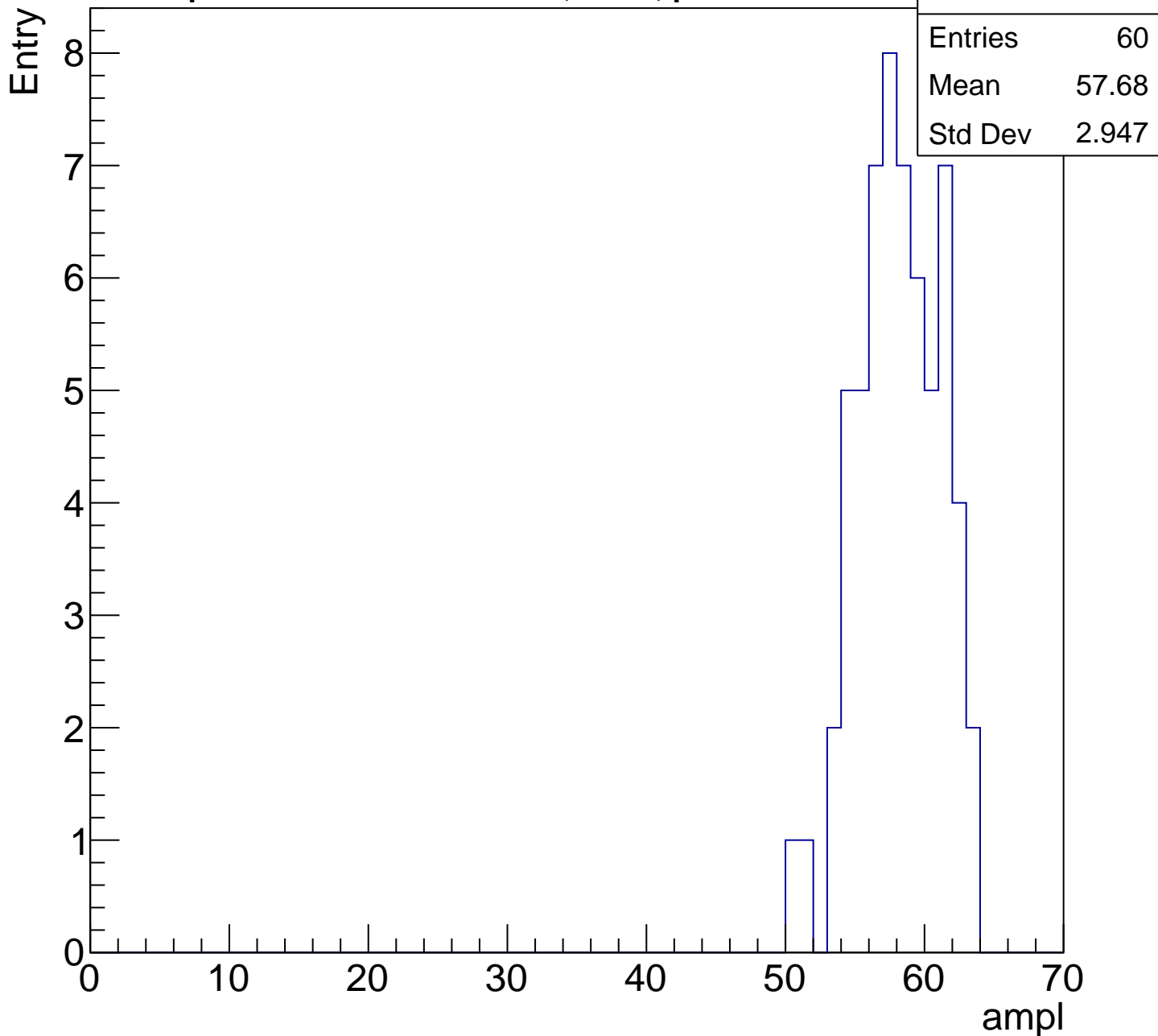
Entry

Entries	46
Mean	53.15
Std Dev	2.897



B1L103S, U5-ch94, adc5

calib_packv5_041523_1651.root, FC#0, port C2

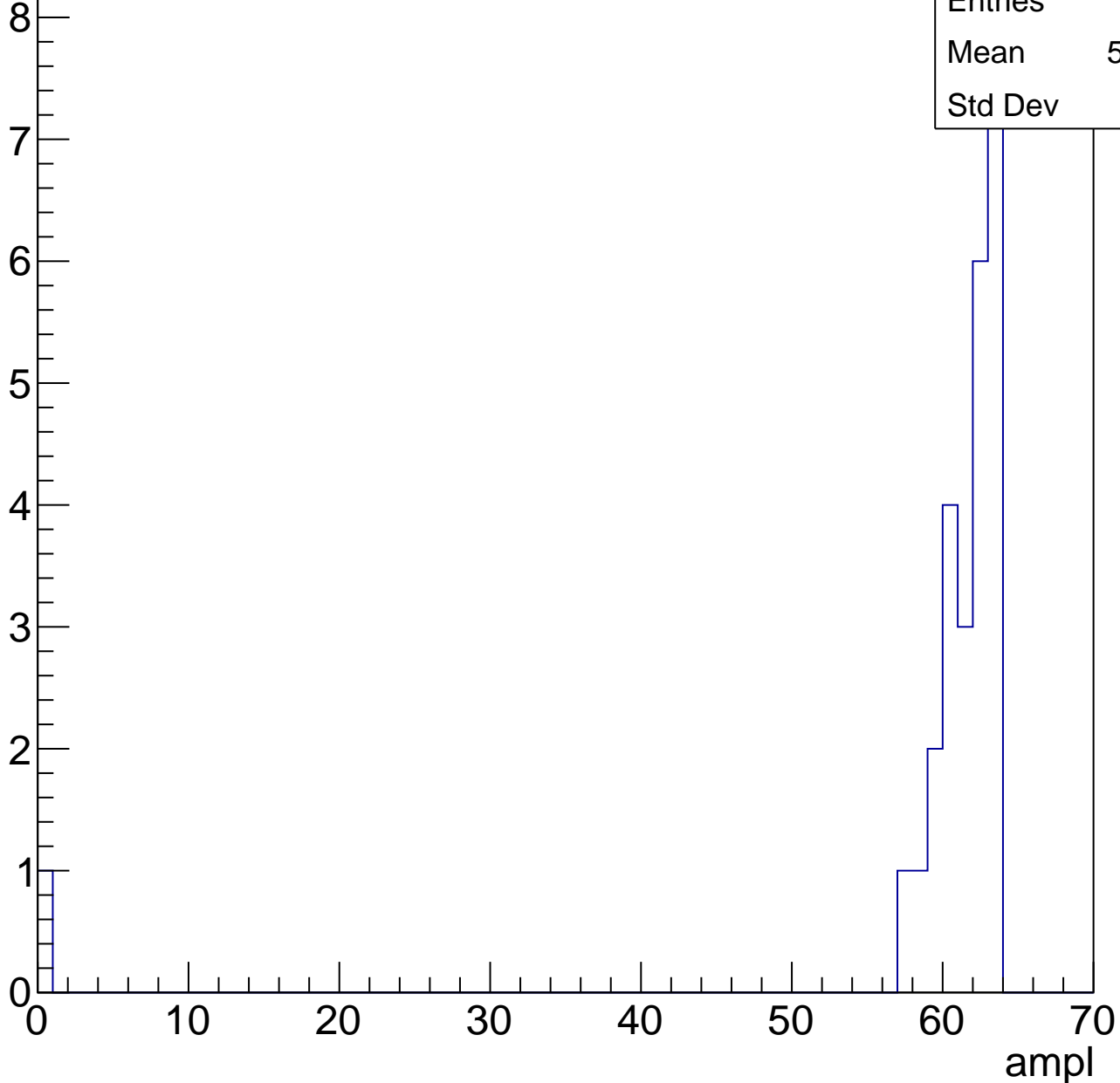


B1L103S, U5-ch94, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	26
Mean	58.92
Std Dev	11.9



B1L103S, U5-ch94, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

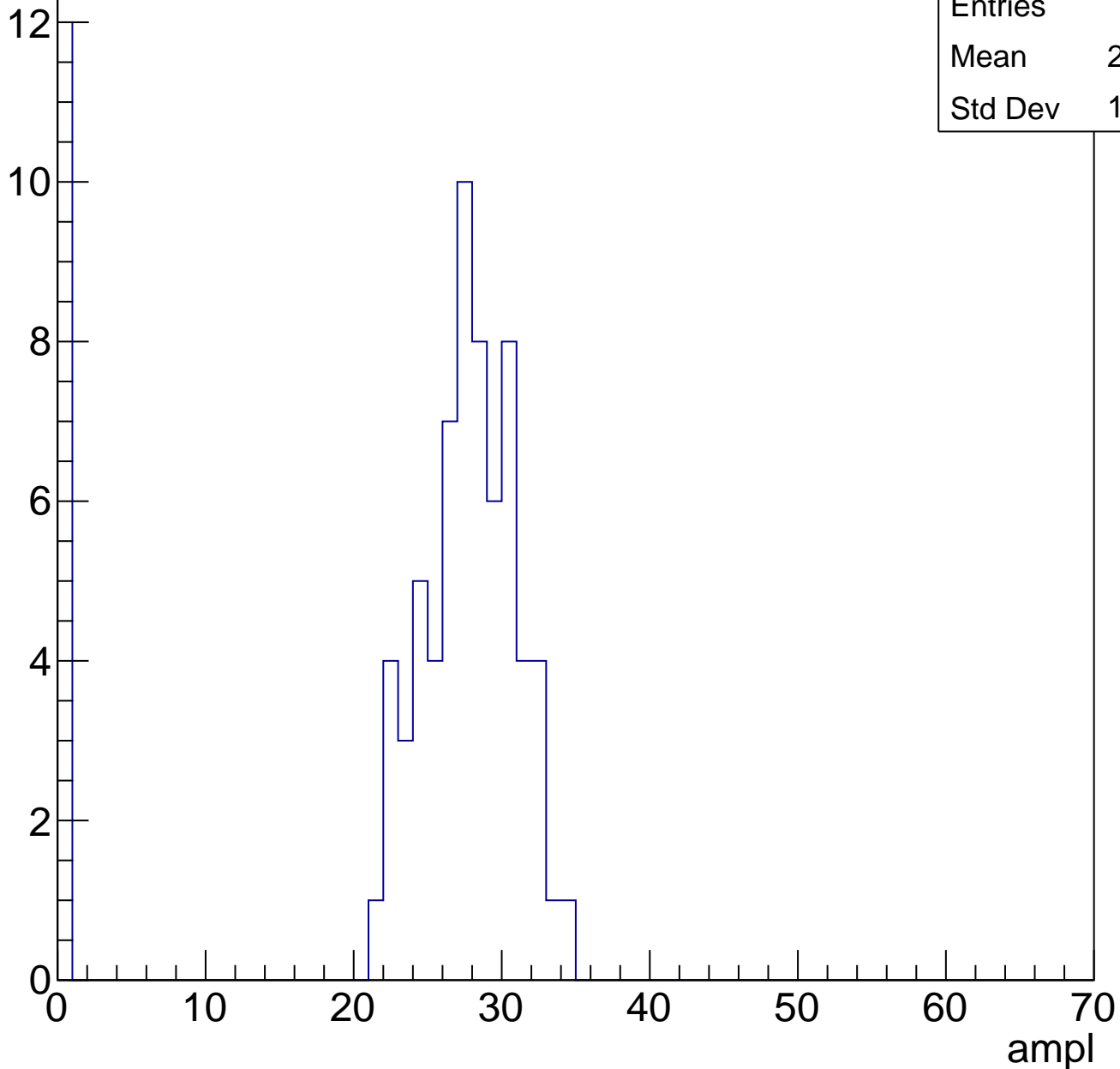


B1L103S, U5-ch95, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	78
Mean	23.17
Std Dev	10.26

Entry

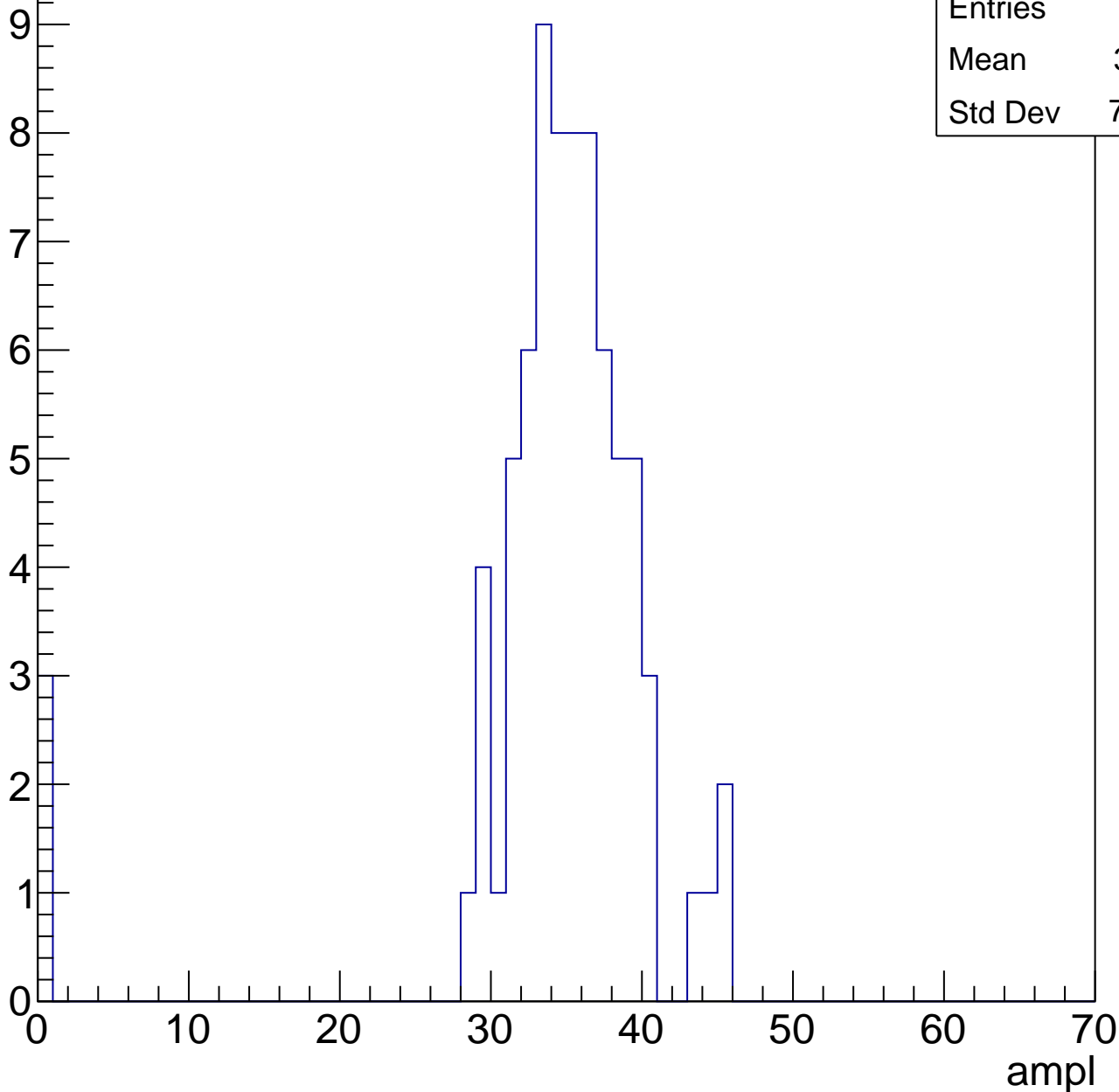


B1L103S, U5-ch95, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	33.71
Std Dev	7.713

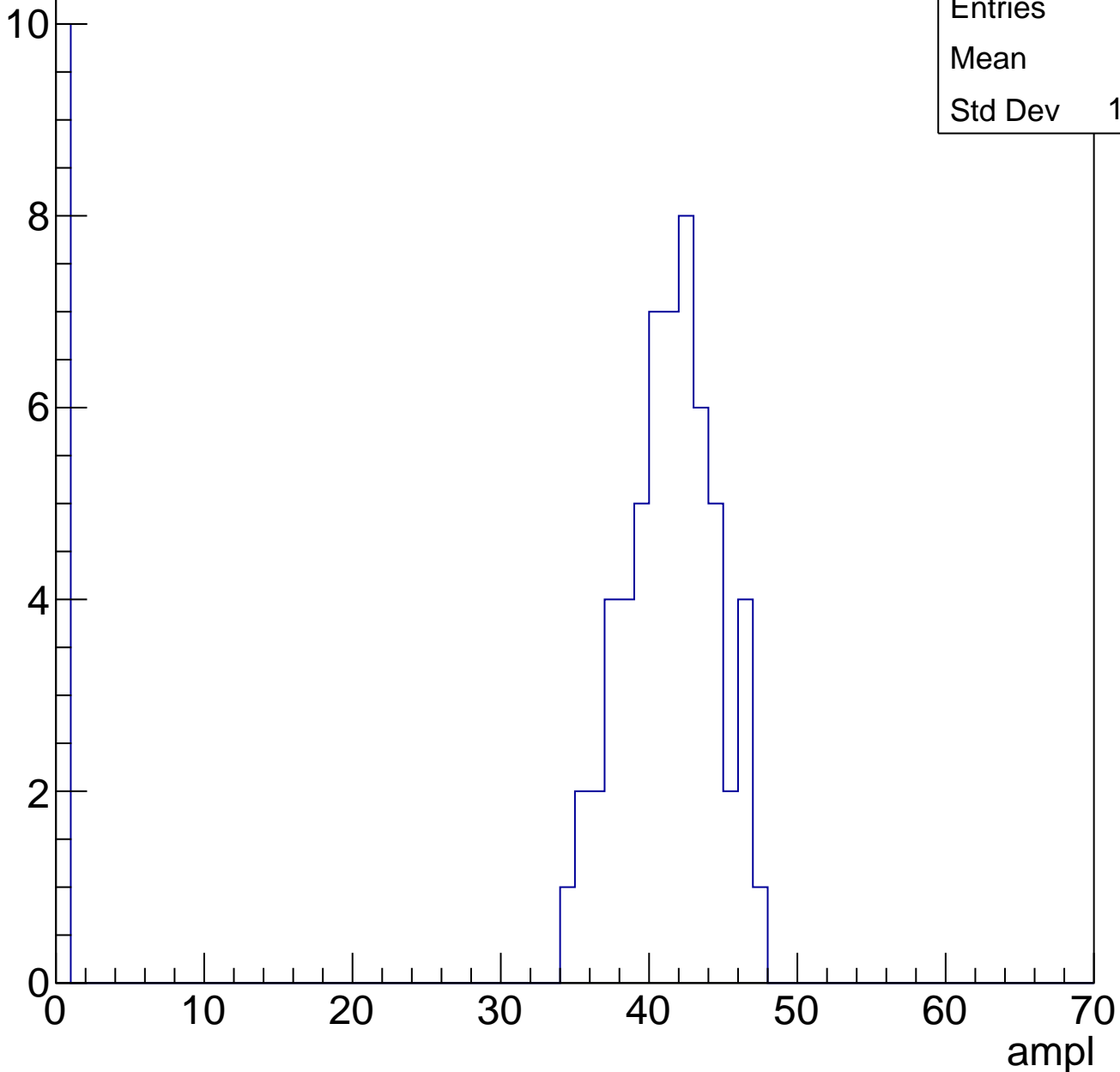


B1L103S, U5-ch95, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	68
Mean	34.9
Std Dev	14.76

Entry

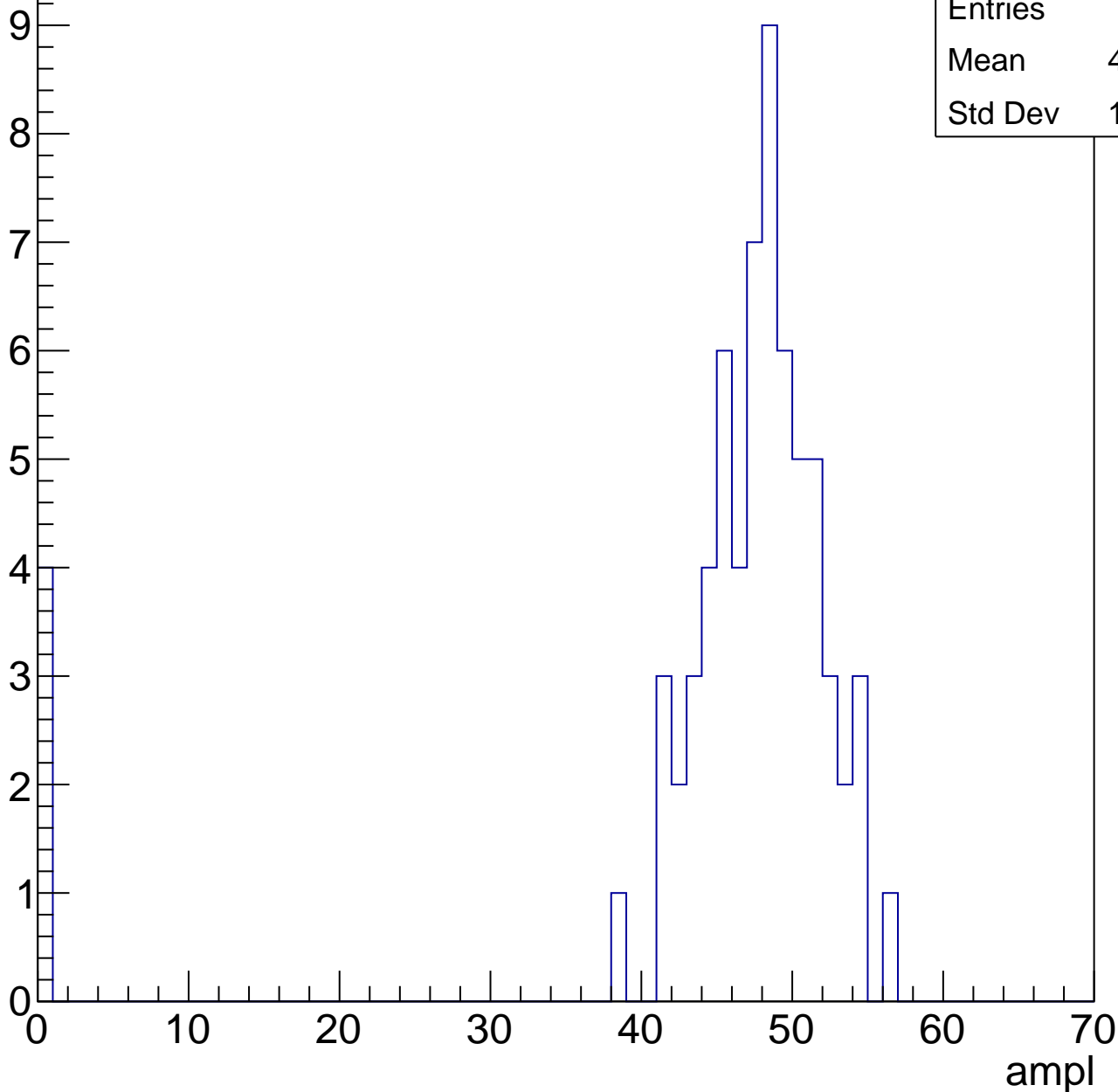


B1L103S, U5-ch95, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	44.76
Std Dev	11.74



B1L103S, U5-ch95, adc4

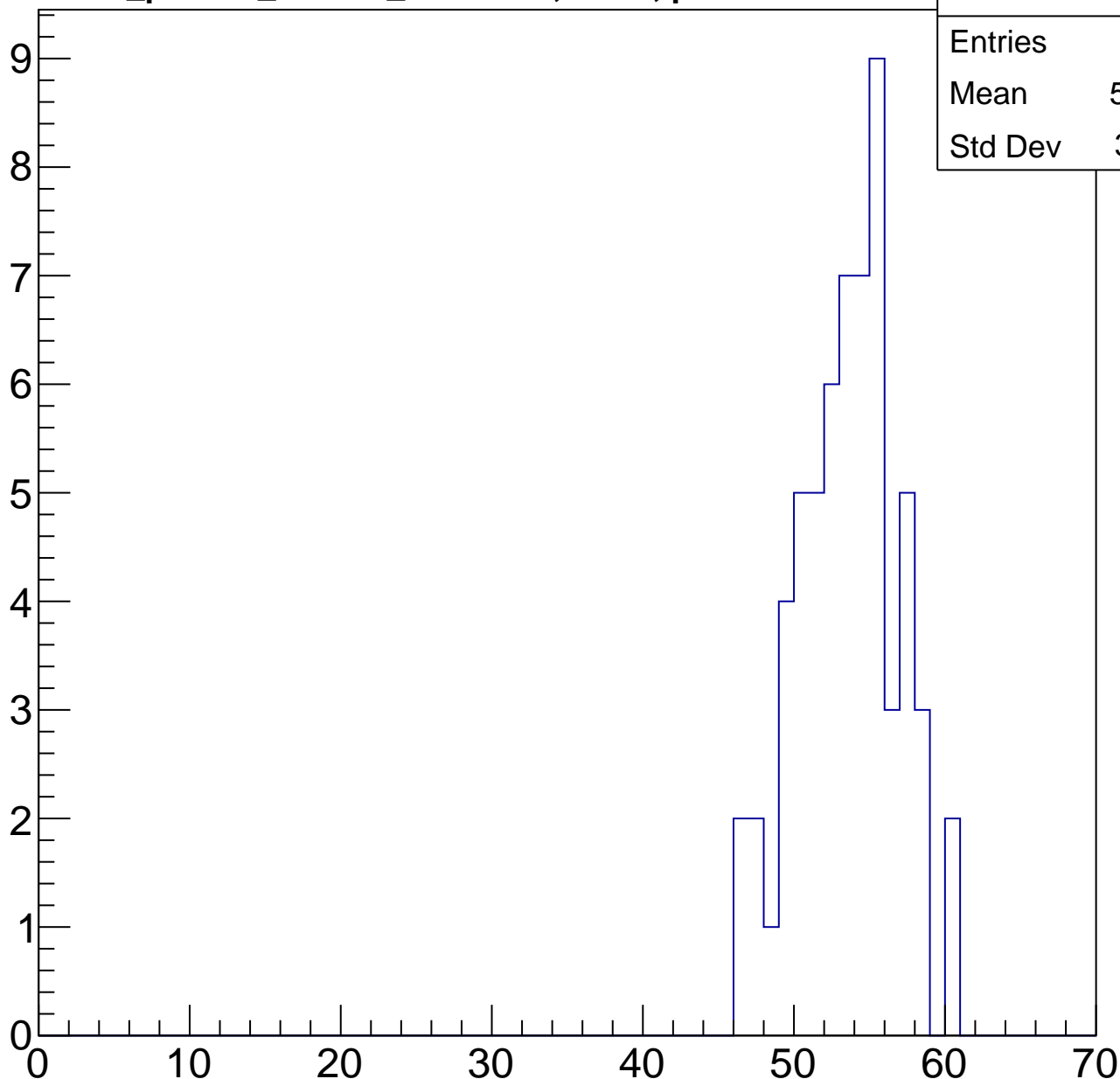
calib_packv5_041523_1651.root, FC#0, port C2

Entry

9
8
7
6
5
4
3
2
1
0

Entries	61
Mean	53.08
Std Dev	3.271

ampl

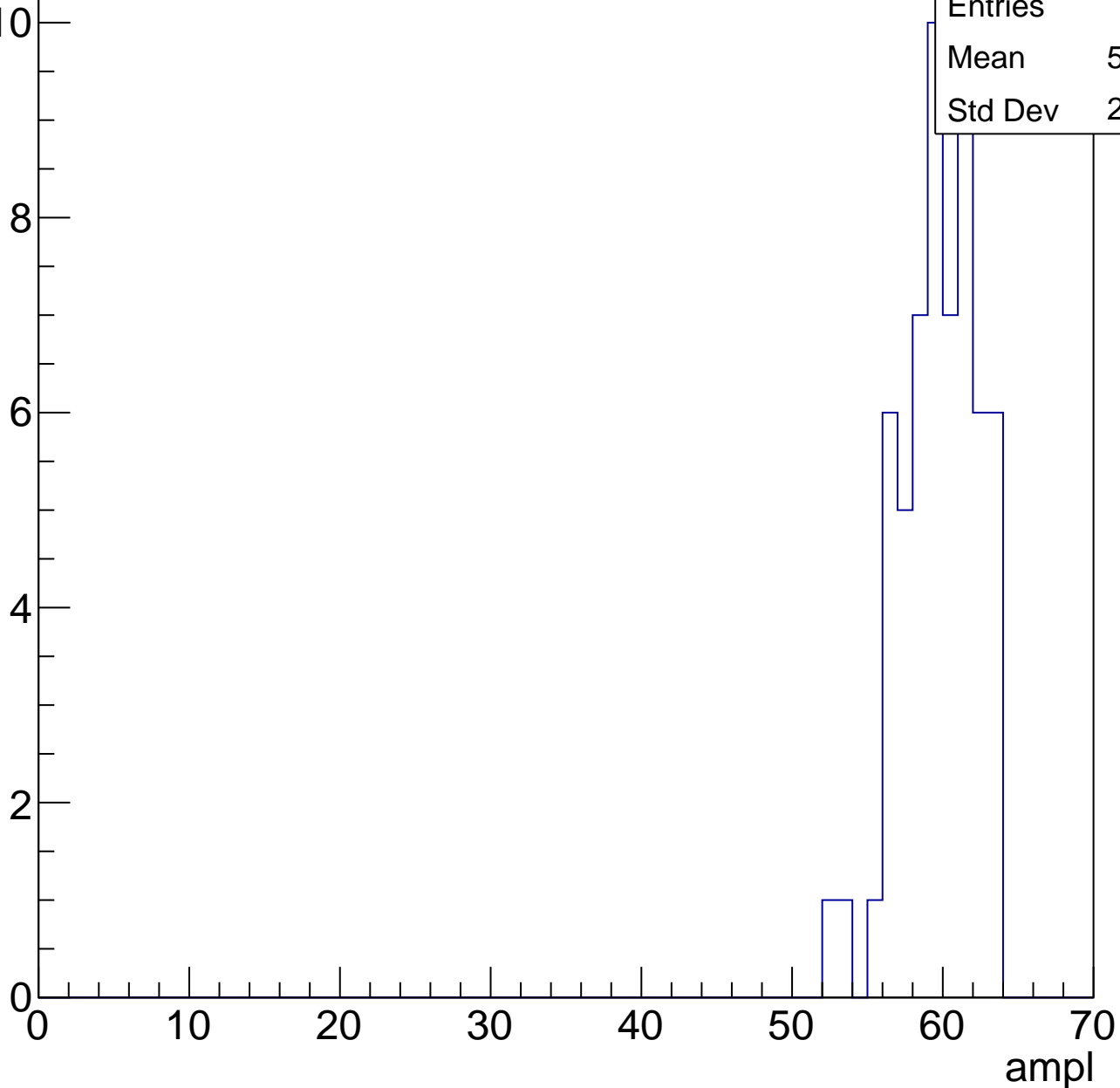


B1L103S, U5-ch95, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

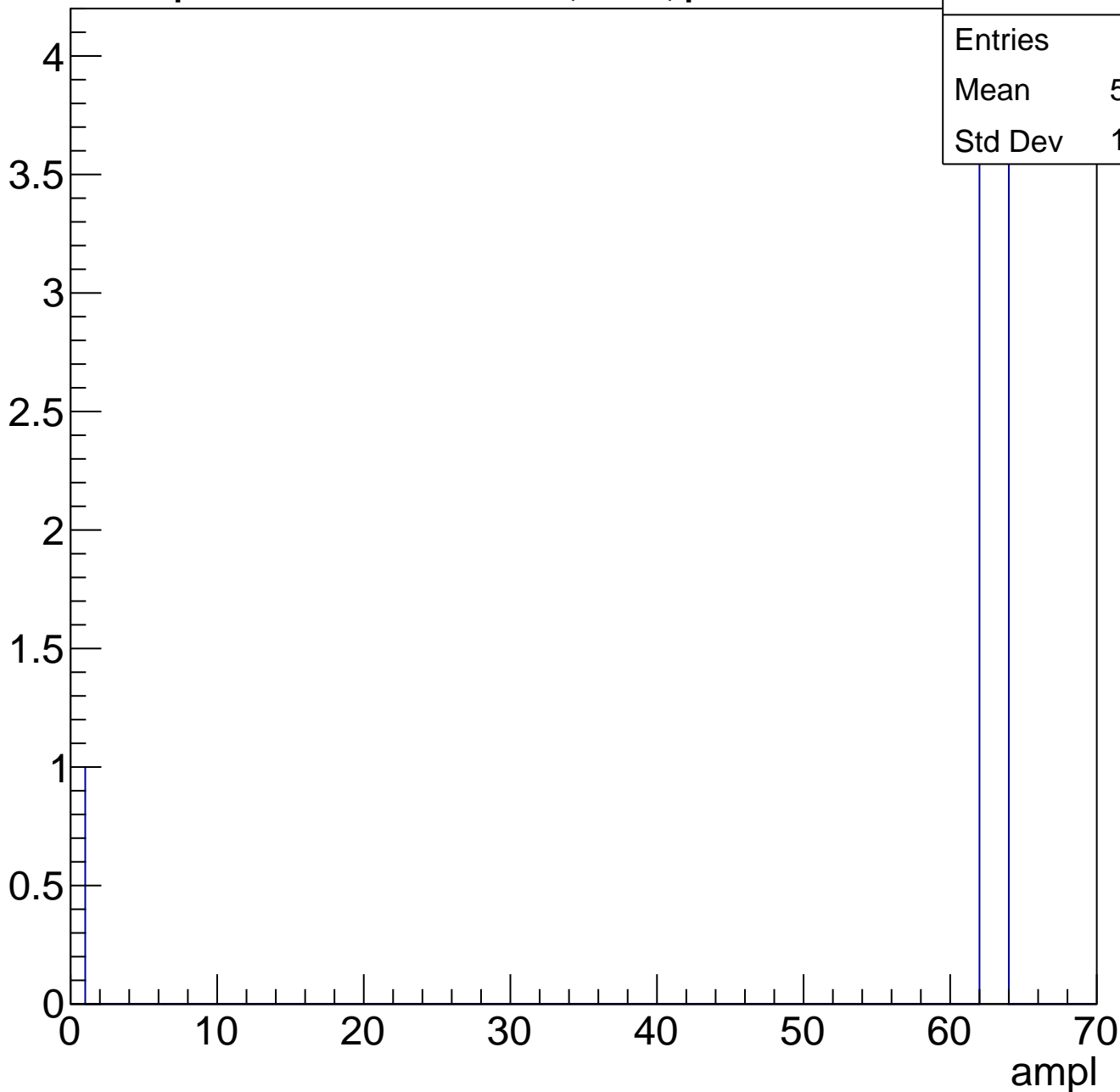
Entries	60
Mean	59.28
Std Dev	2.497



B1L103S, U5-ch95, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

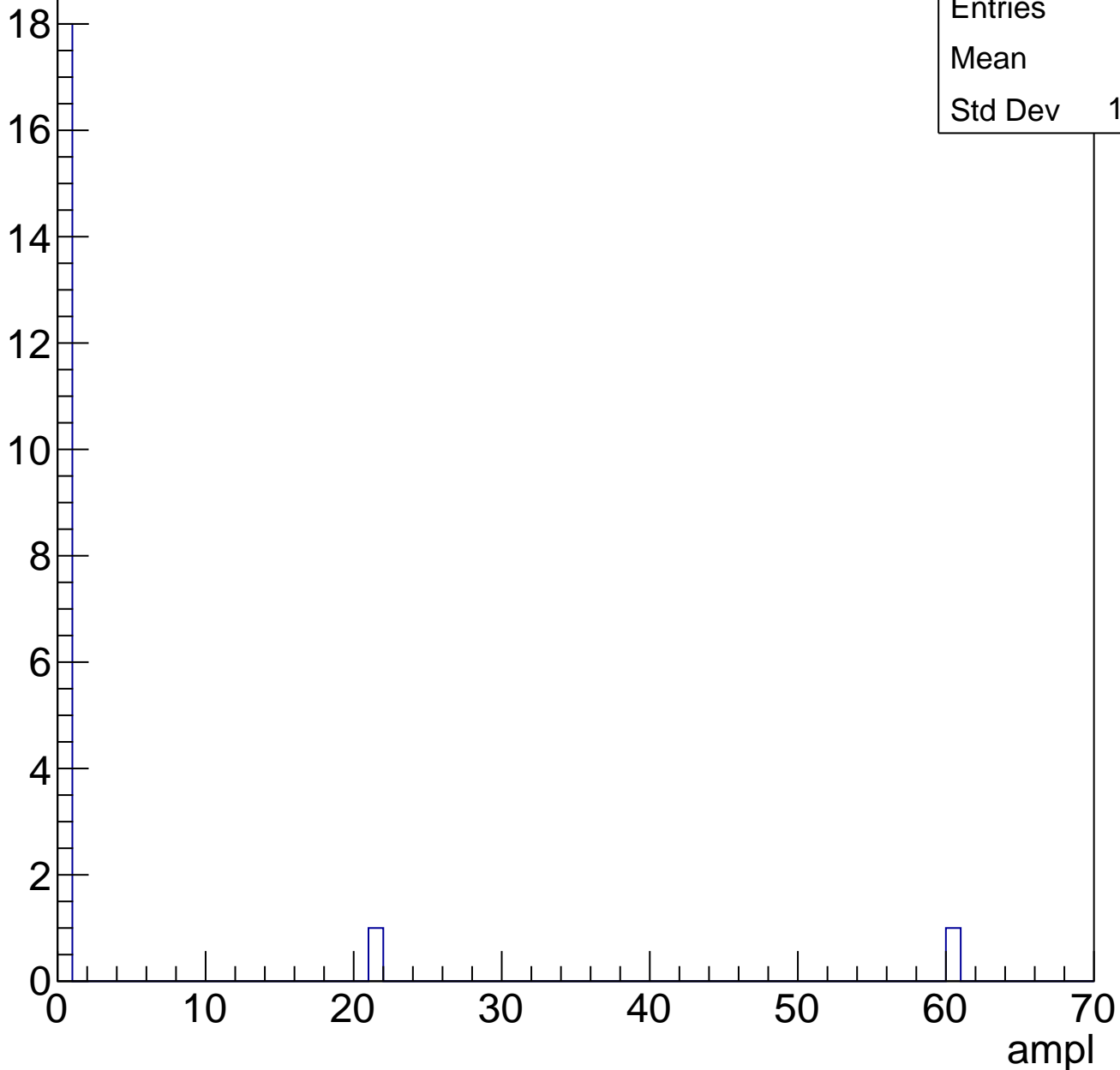


B1L103S, U5-ch95, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	4.05
Std Dev	13.63

Entry

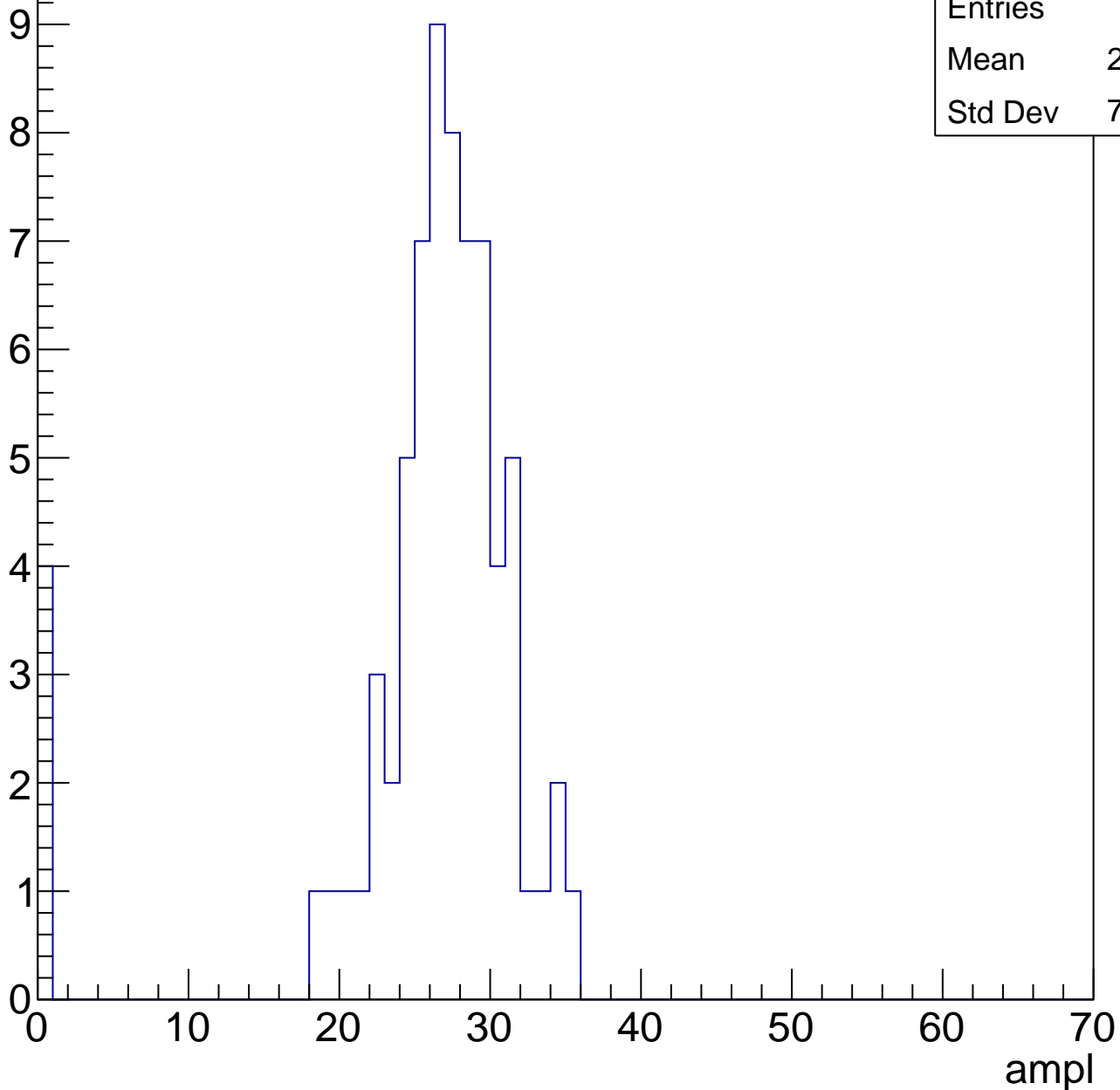


B1L103S, U5-ch96, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	25.39
Std Dev	7.098

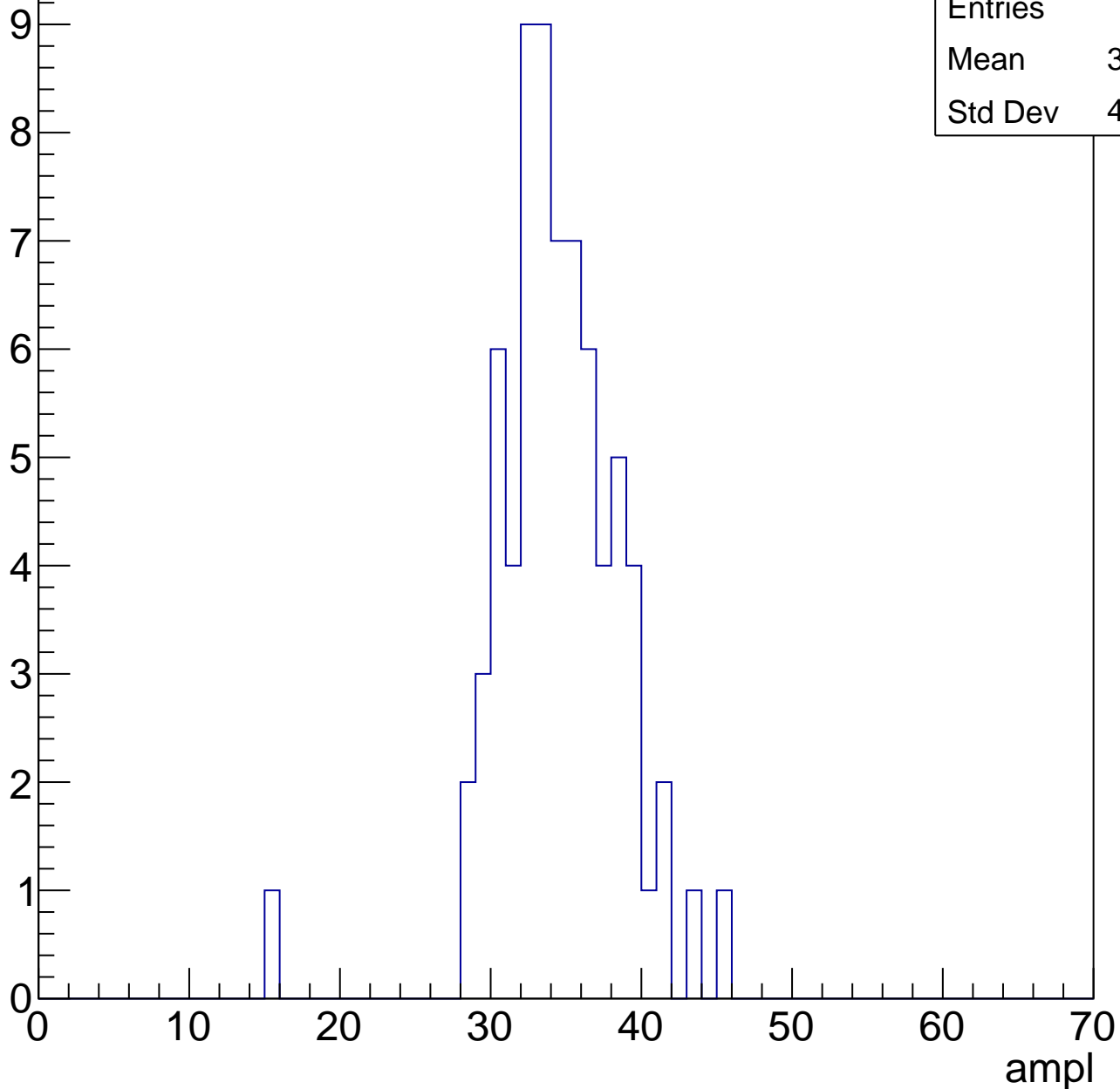


B1L103S, U5-ch96, adc1

calib_packv5_041523_1651.root, FC#0, port C2

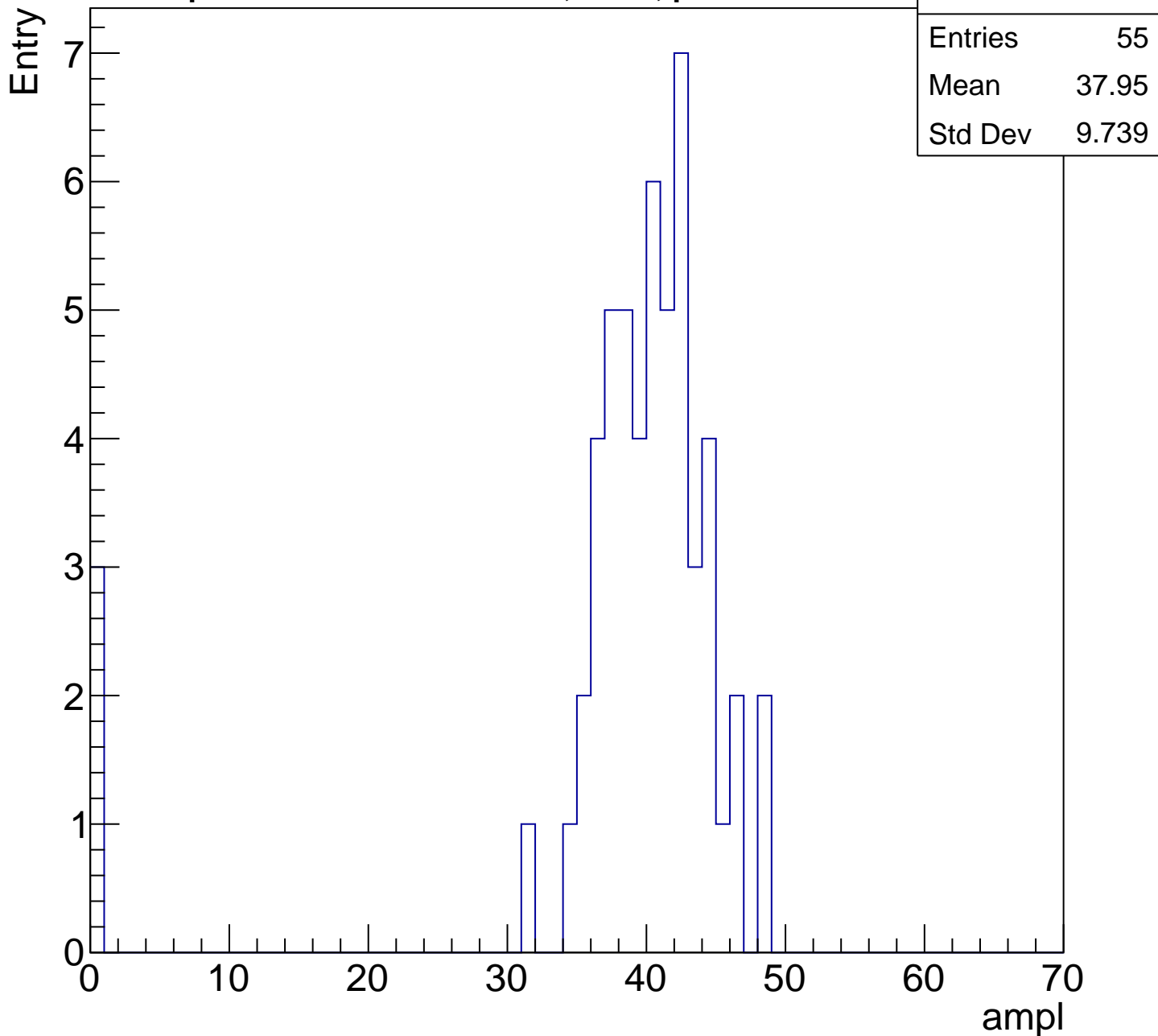
Entry

Entries	72
Mean	34.03
Std Dev	4.196



B1L103S, U5-ch96, adc2

calib_packv5_041523_1651.root, FC#0, port C2

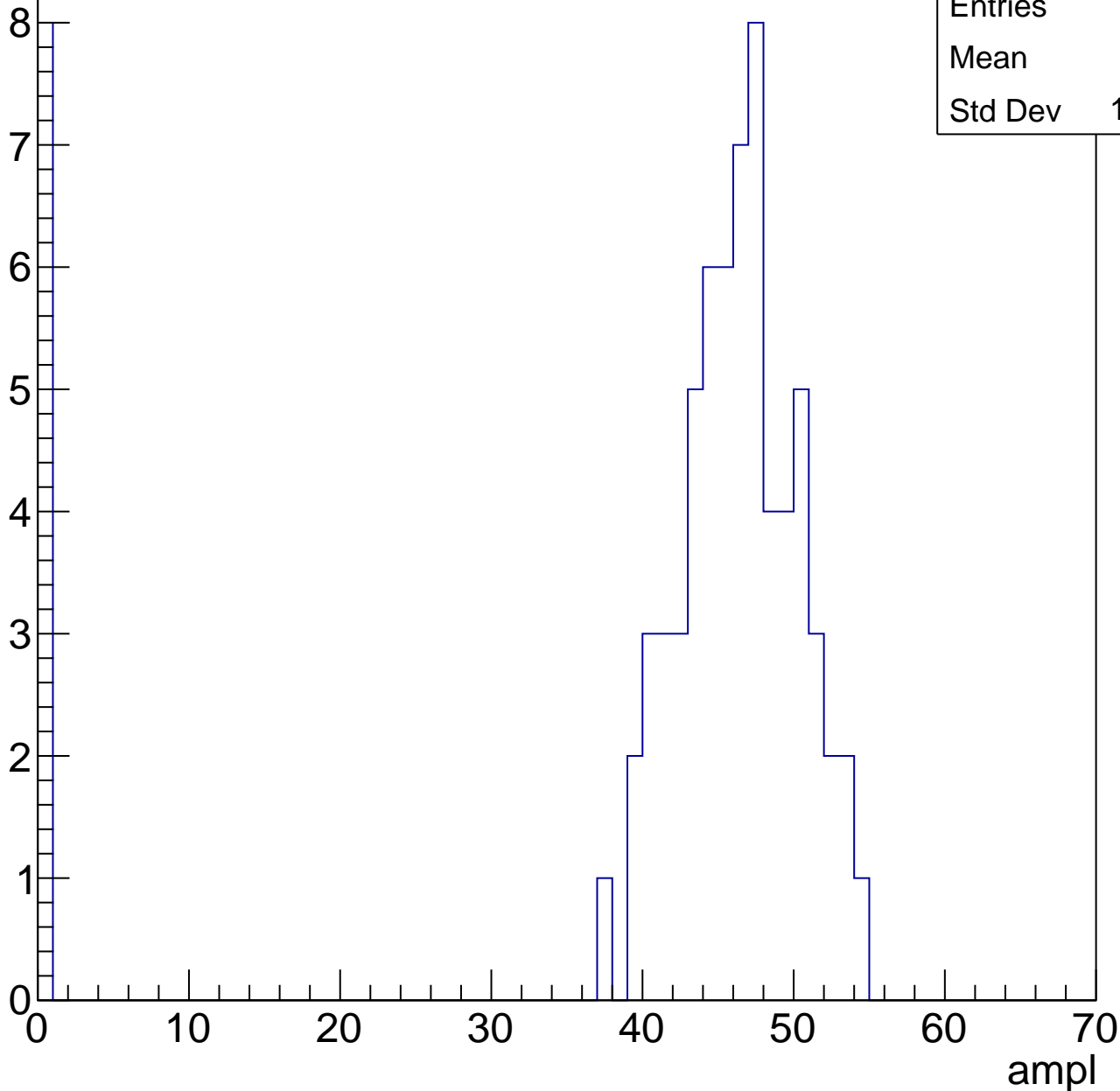


B1L103S, U5-ch96, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	40.9
Std Dev	14.79

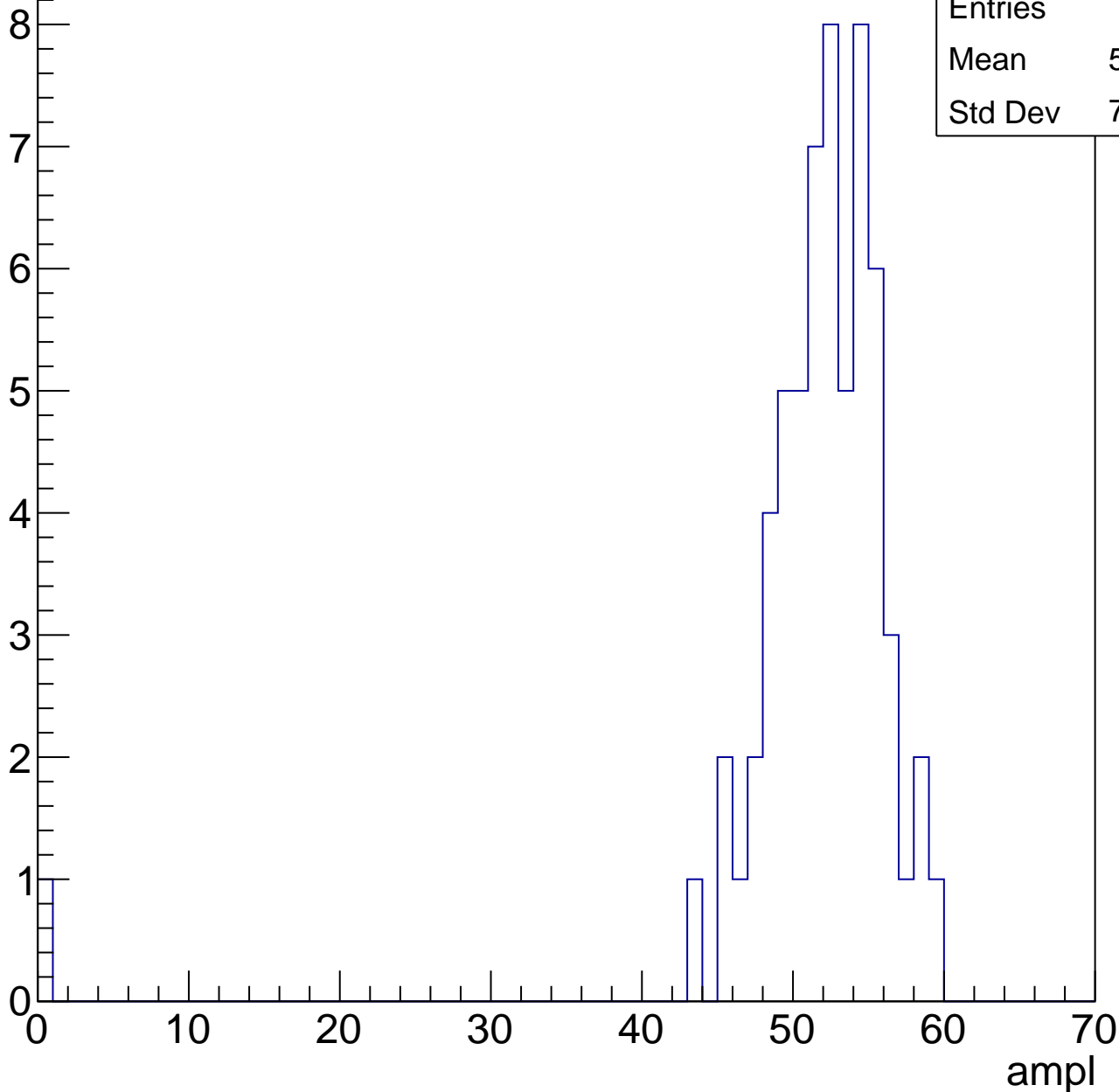


B1L103S, U5-ch96, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	50.97
Std Dev	7.322

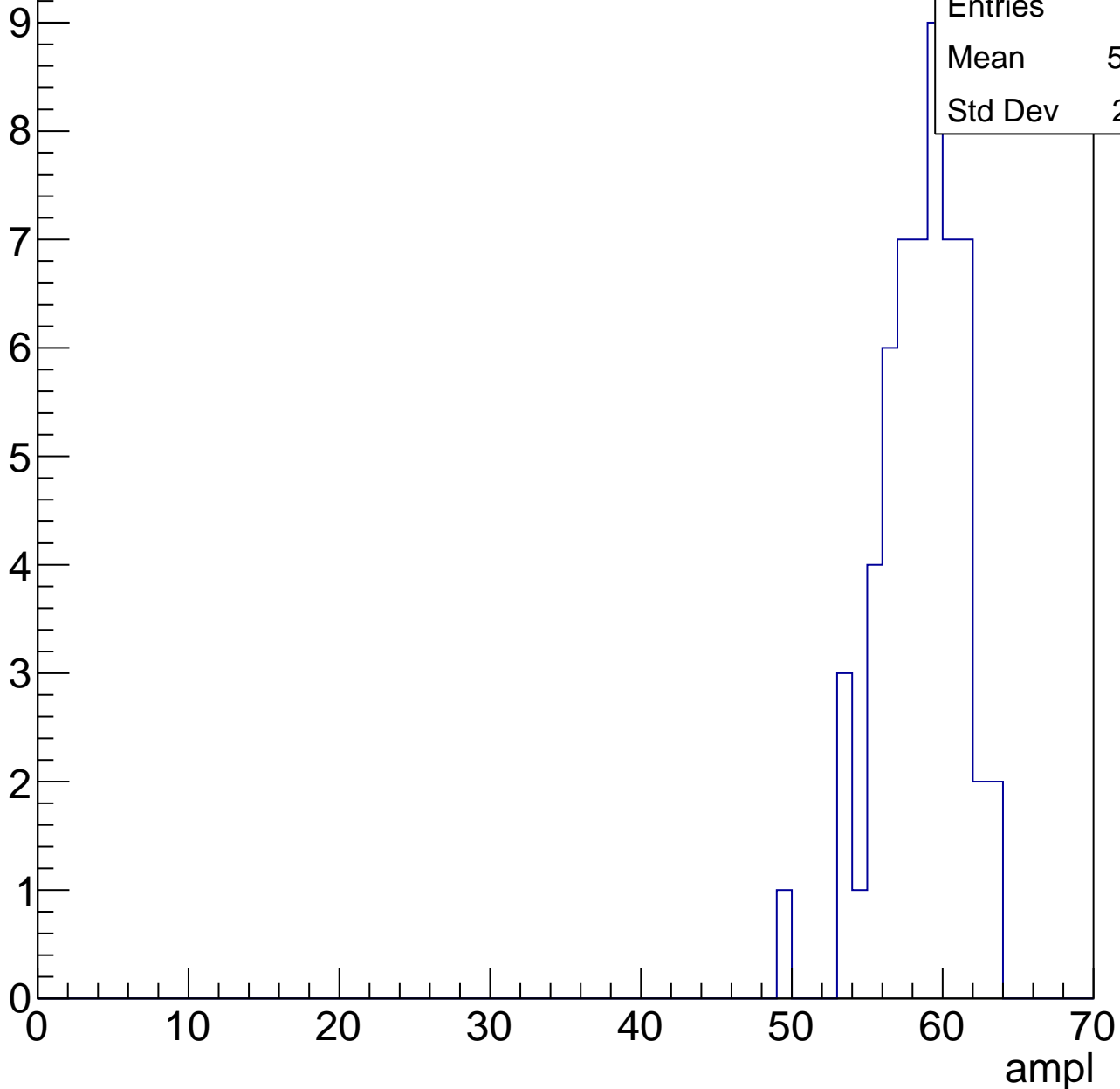


B1L103S, U5-ch96, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	58.05
Std Dev	2.741

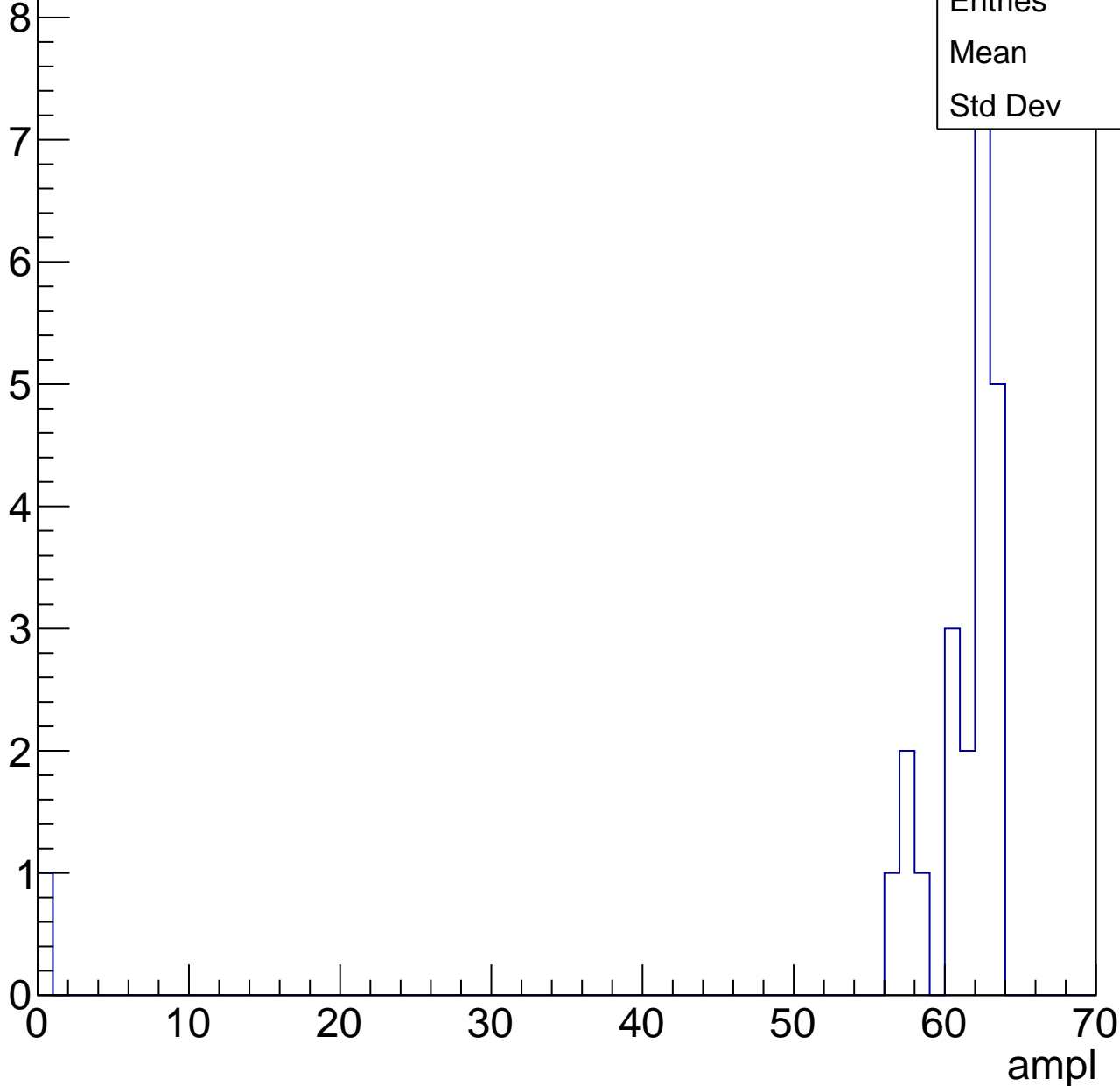


B1L103S, U5-ch96, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	23
Mean	58.3
Std Dev	12.6

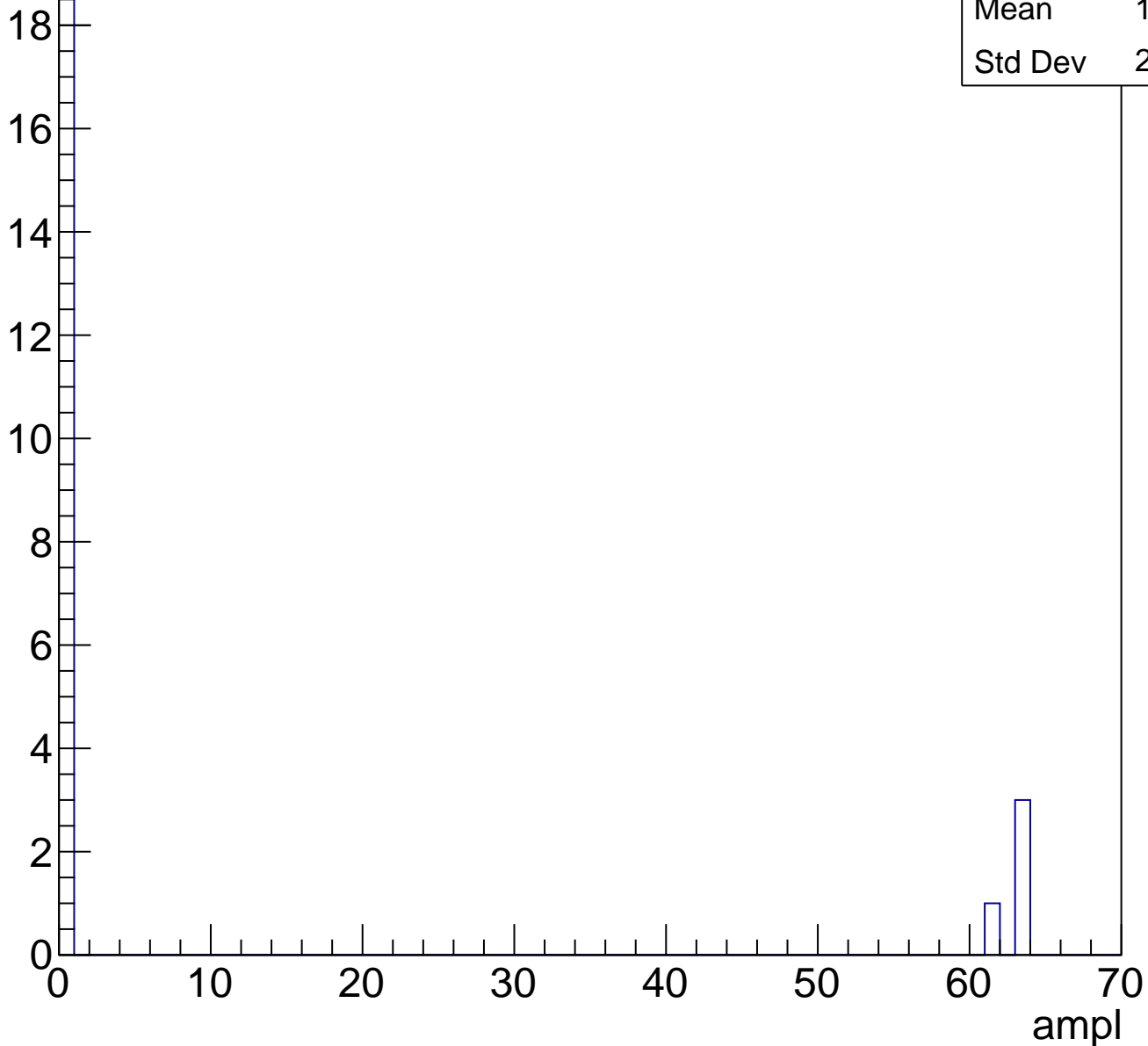


B1L103S, U5-ch96, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	23
Mean	10.87
Std Dev	23.69

Entry



B1L103S, U5-ch97, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	87
Mean	25.13
Std Dev	10.18

Entry

10

8

6

4

2

0

0

10

20

30

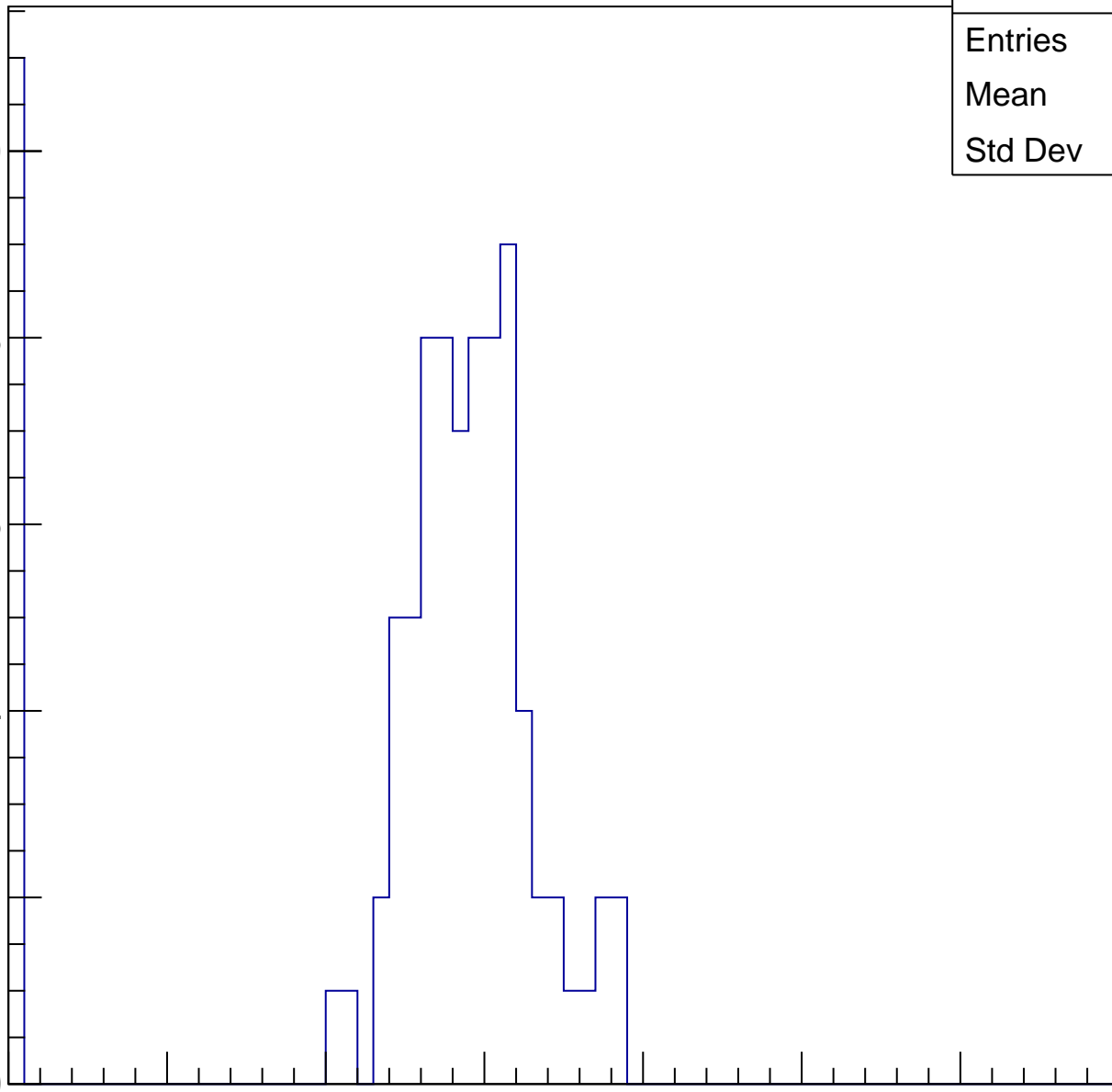
40

50

60

70

ampl

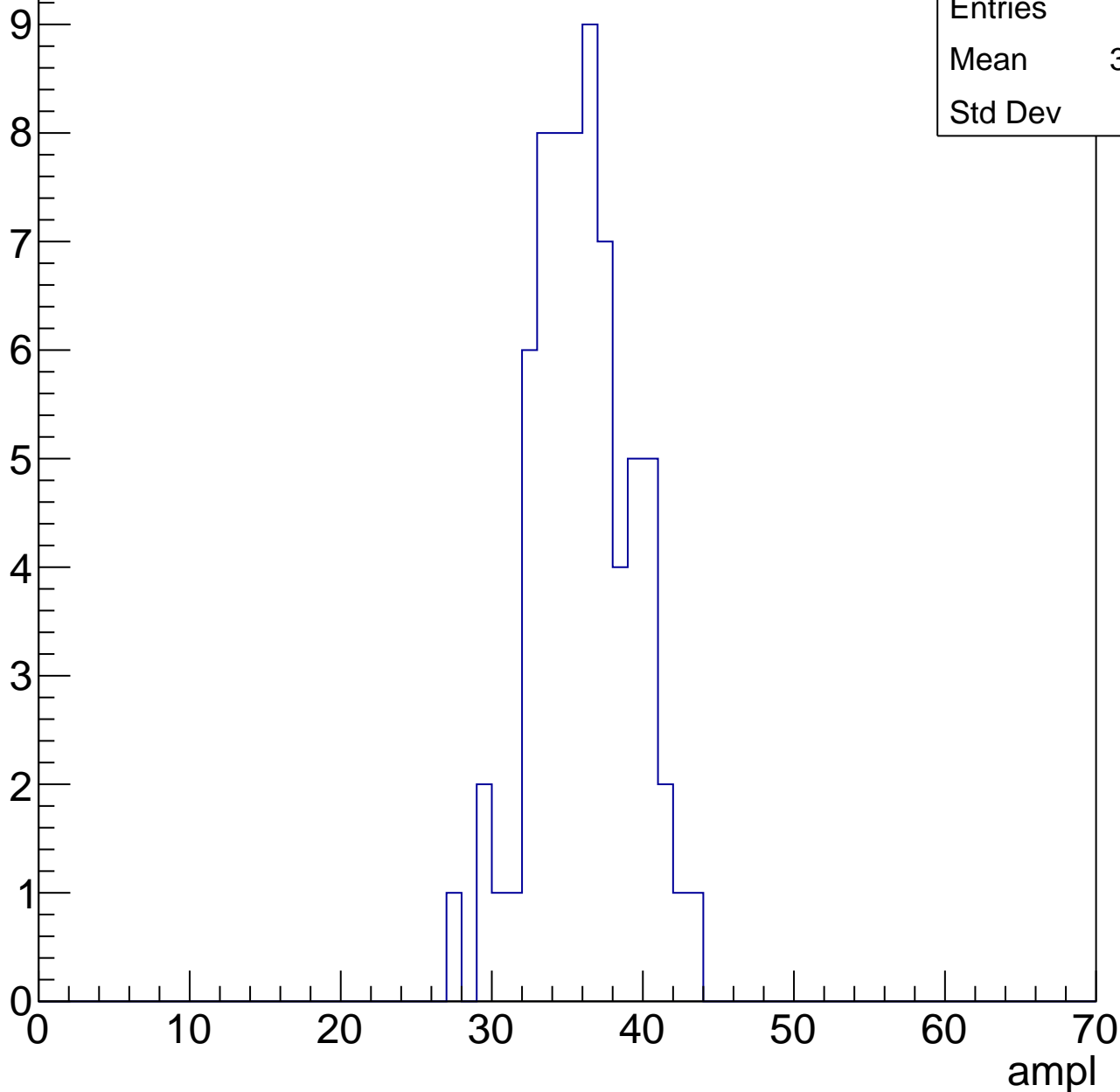


B1L103S, U5-ch97, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	35.52
Std Dev	3.22

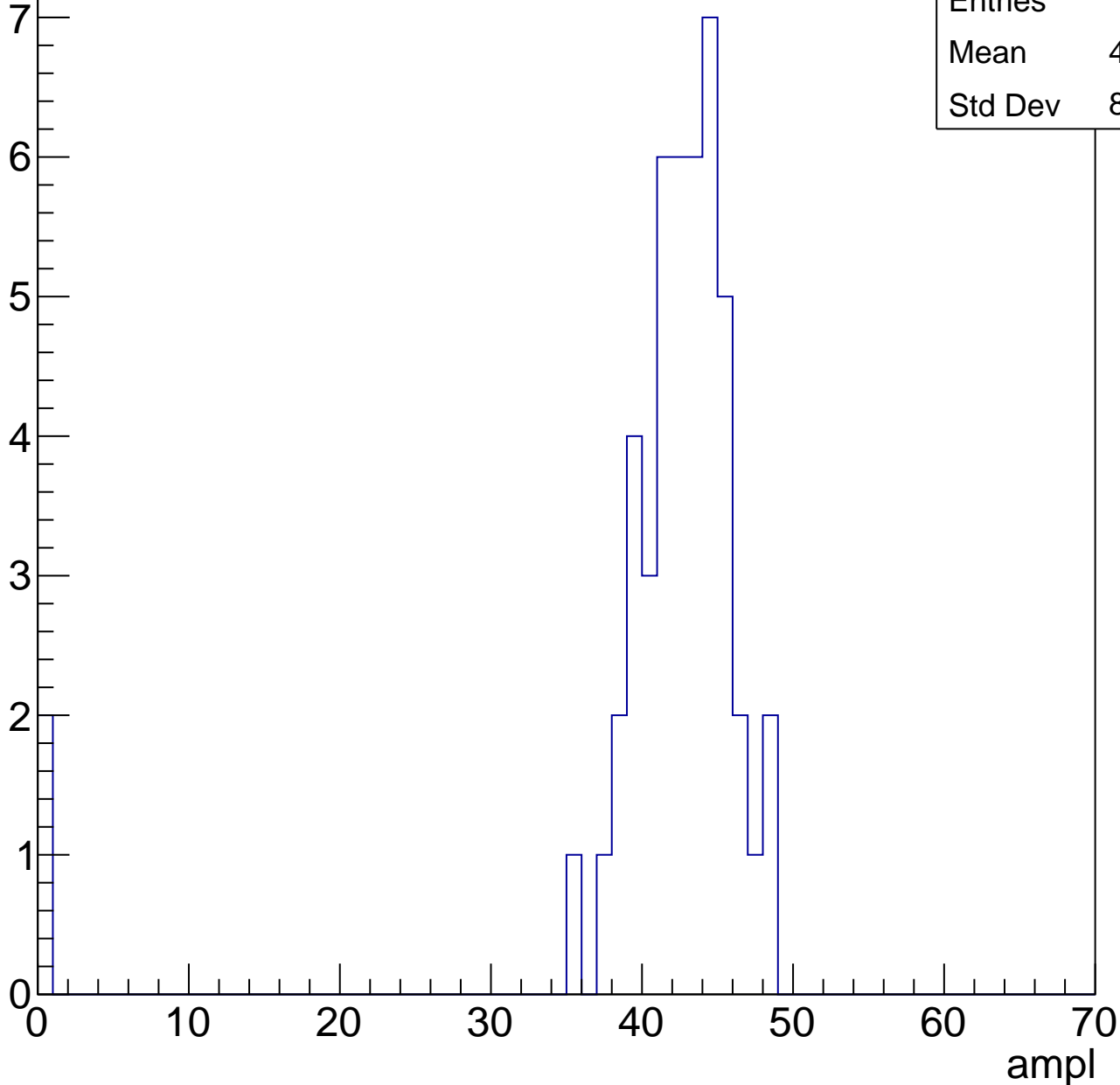


B1L103S, U5-ch97, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

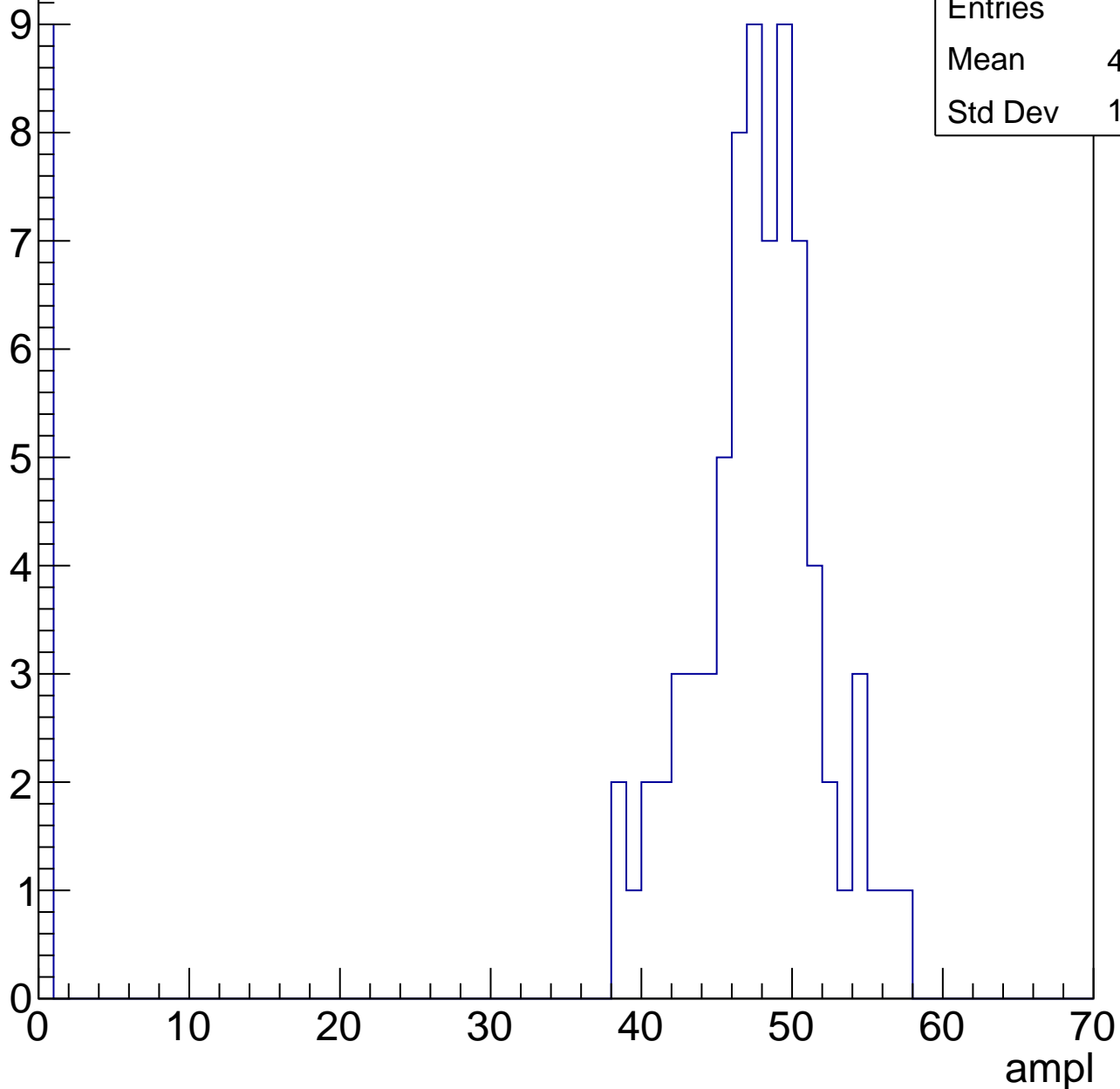
Entries	48
Mean	40.58
Std Dev	8.897



B1L103S, U5-ch97, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

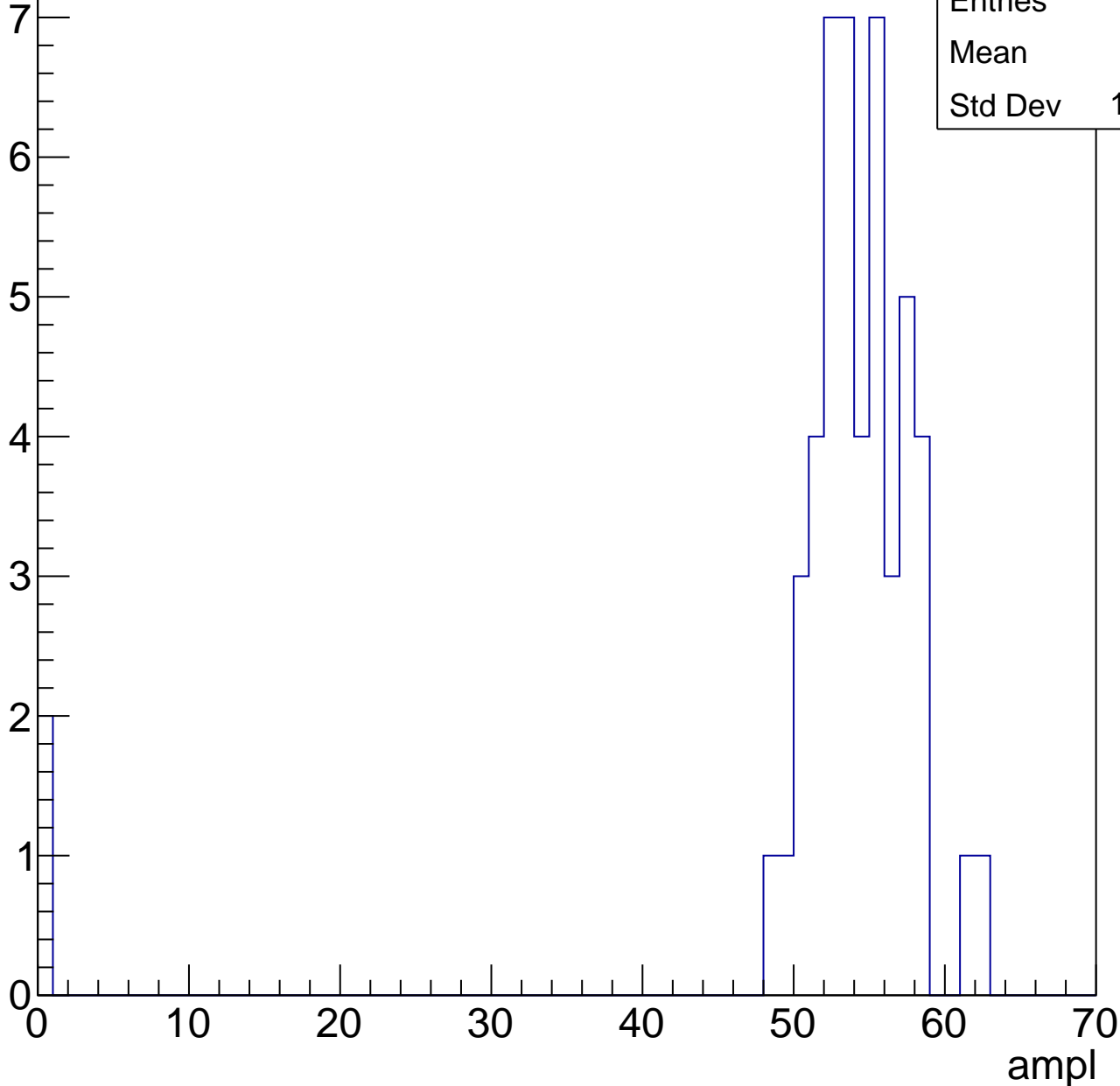


B1L103S, U5-ch97, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	51.9
Std Dev	10.98

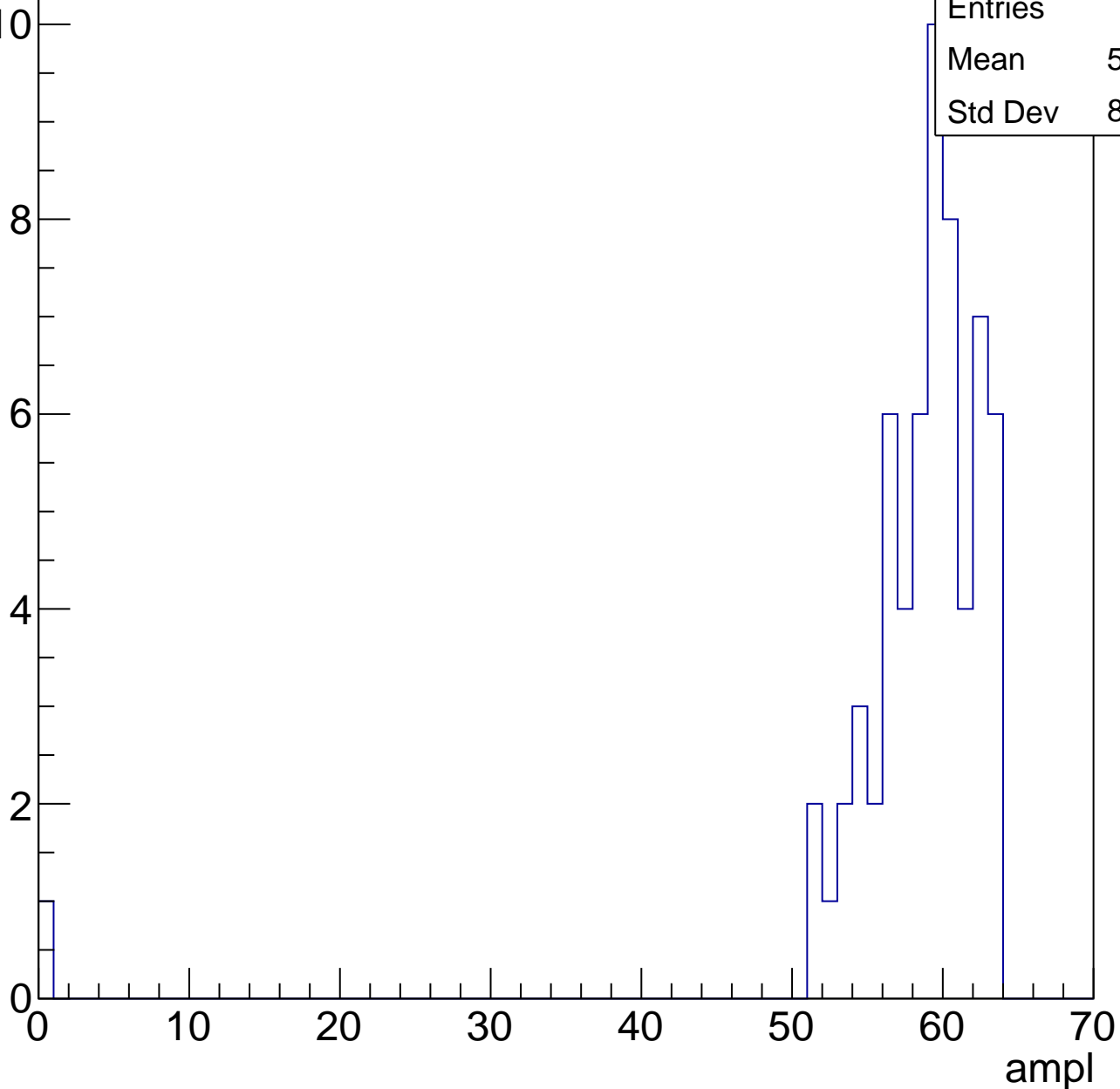


B1L103S, U5-ch97, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	57.58
Std Dev	8.003

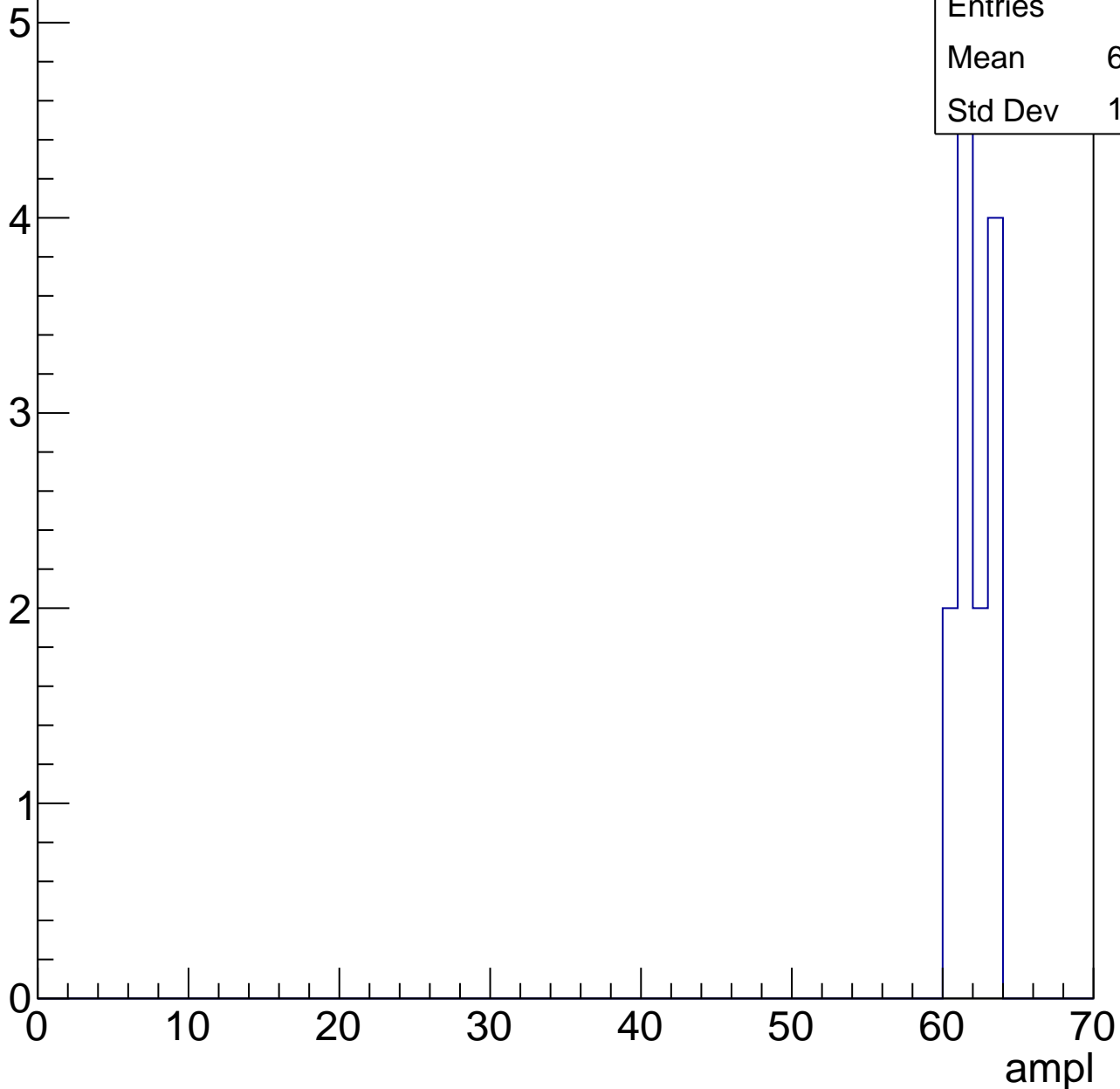


B1L103S, U5-ch97, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

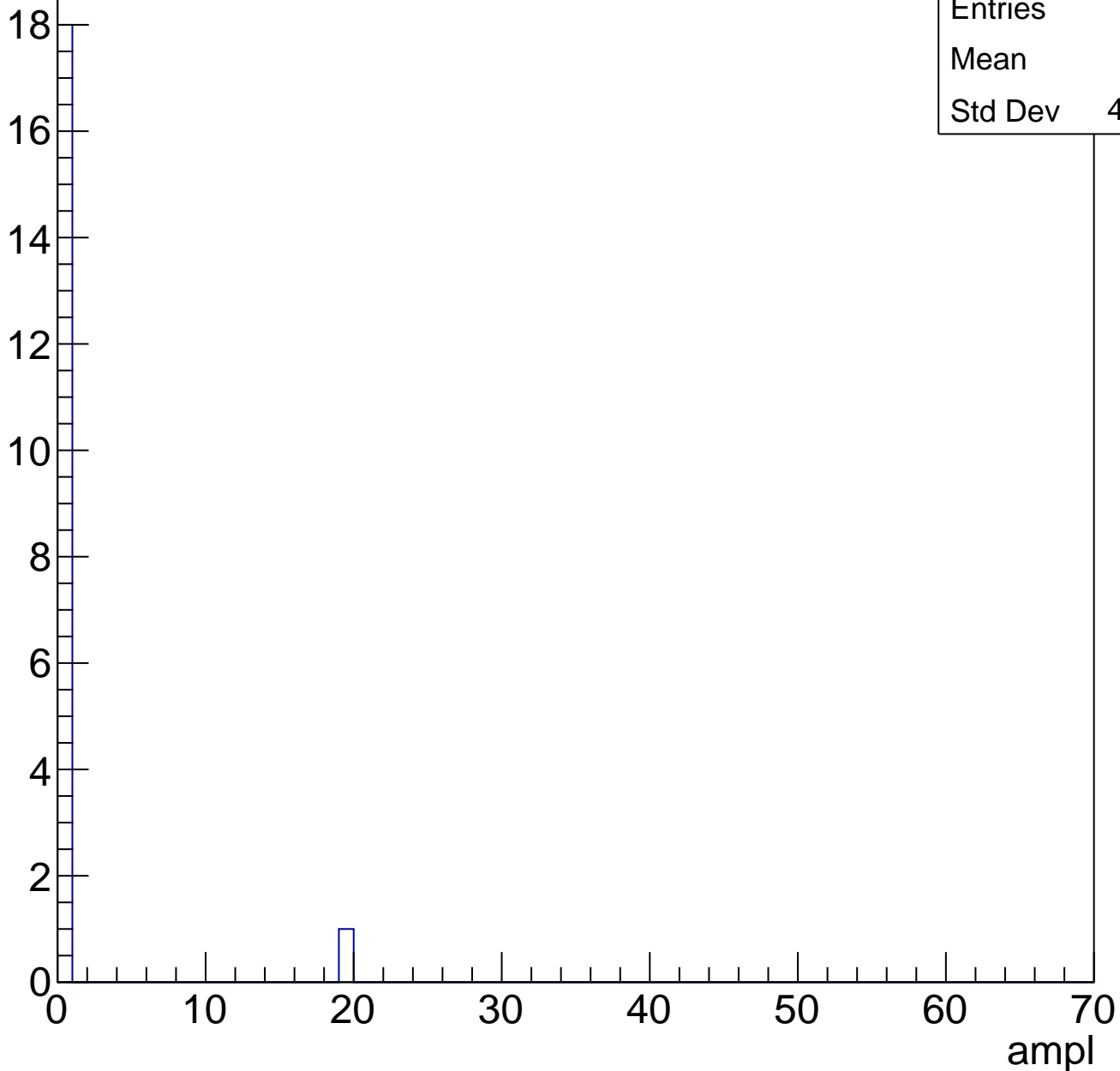
Entries	13
Mean	61.62
Std Dev	1.077



B1L103S, U5-ch97, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

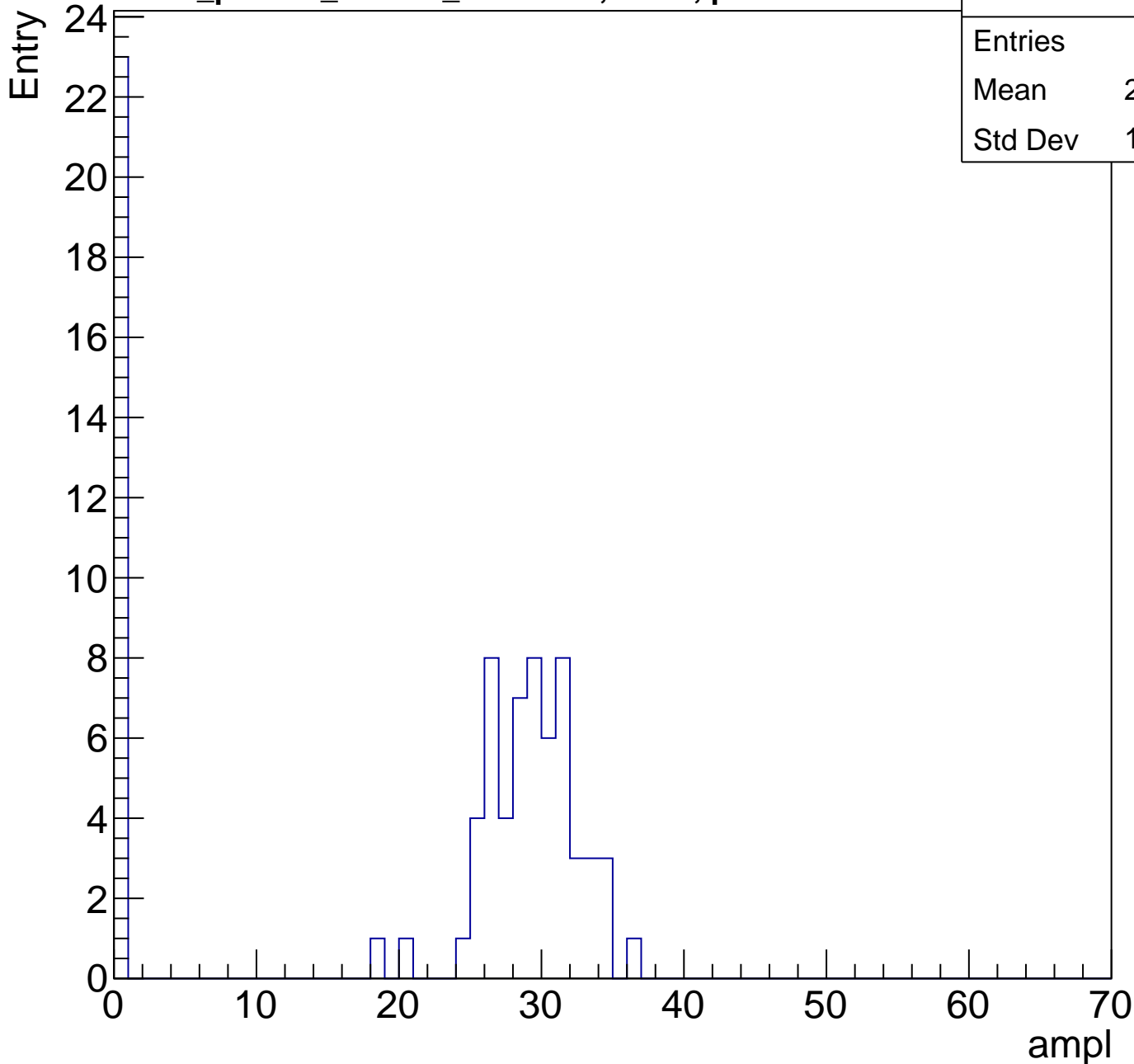


Entries	19
Mean	1
Std Dev	4.243

B1L103S, U5-ch98, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	20.58
Std Dev	13.25

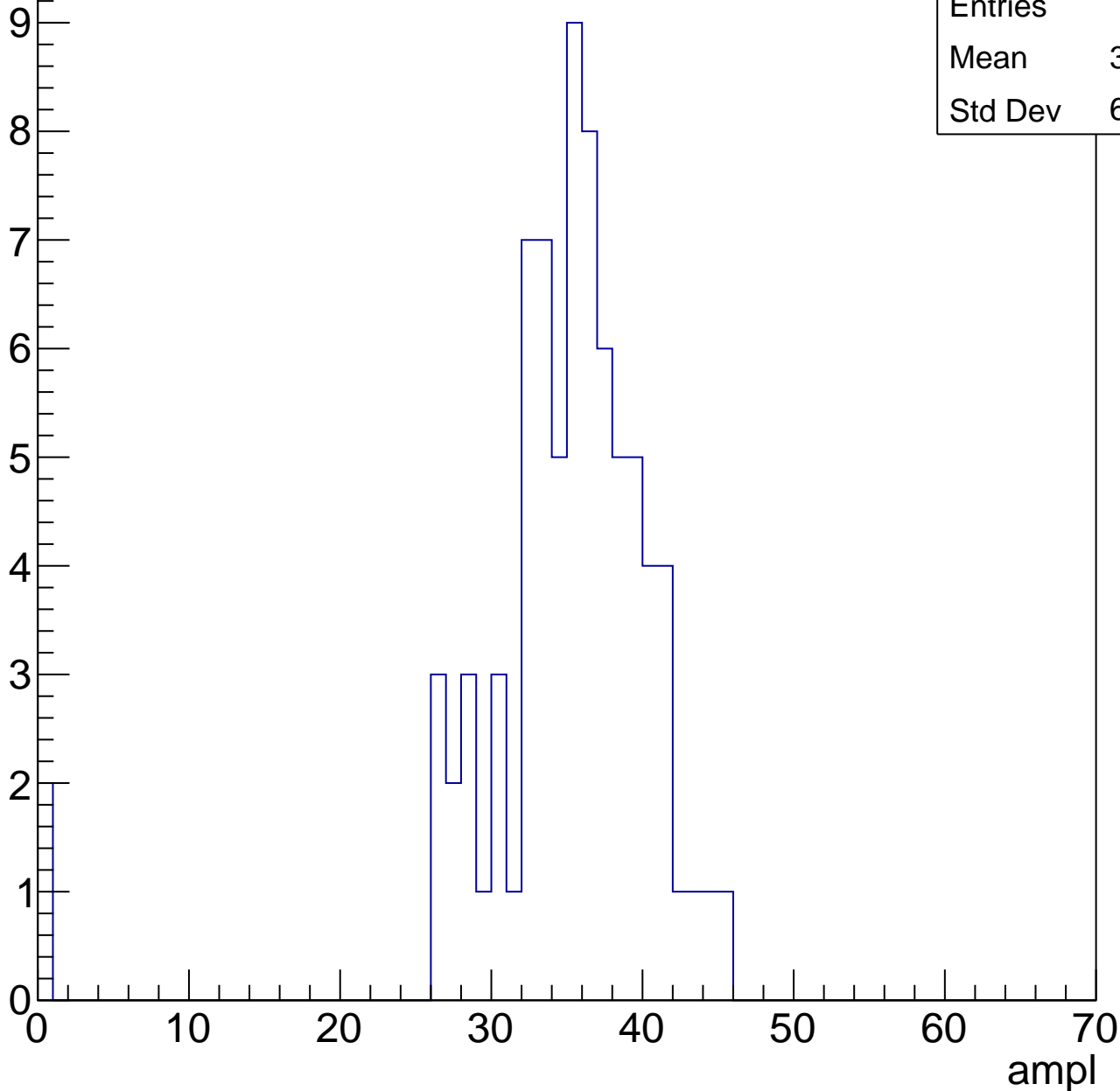


B1L103S, U5-ch98, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	79
Mean	34.16
Std Dev	6.964

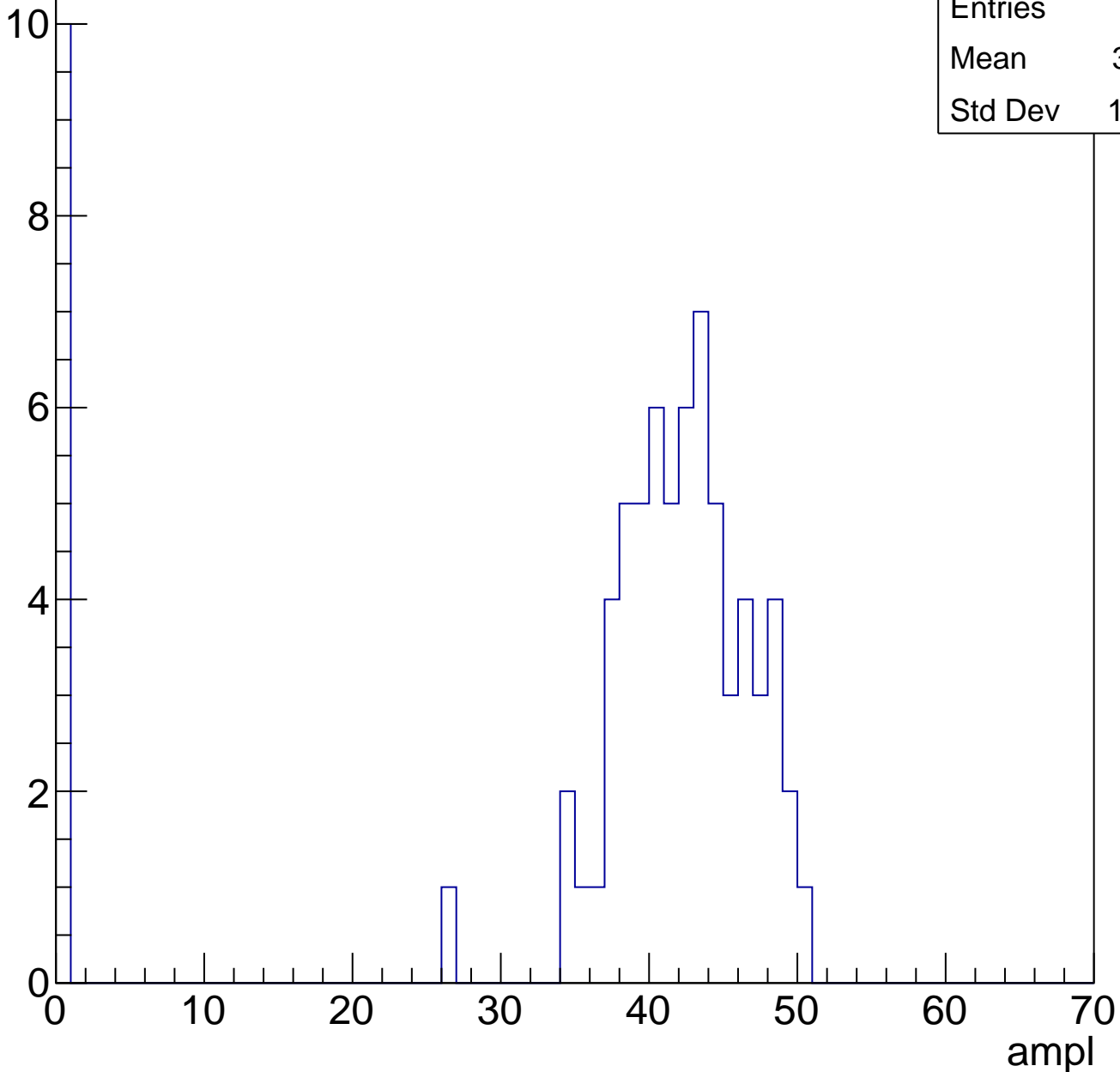


B1L103S, U5-ch98, adc2

calib_packv5_041523_1651.root, FC#0, port C2

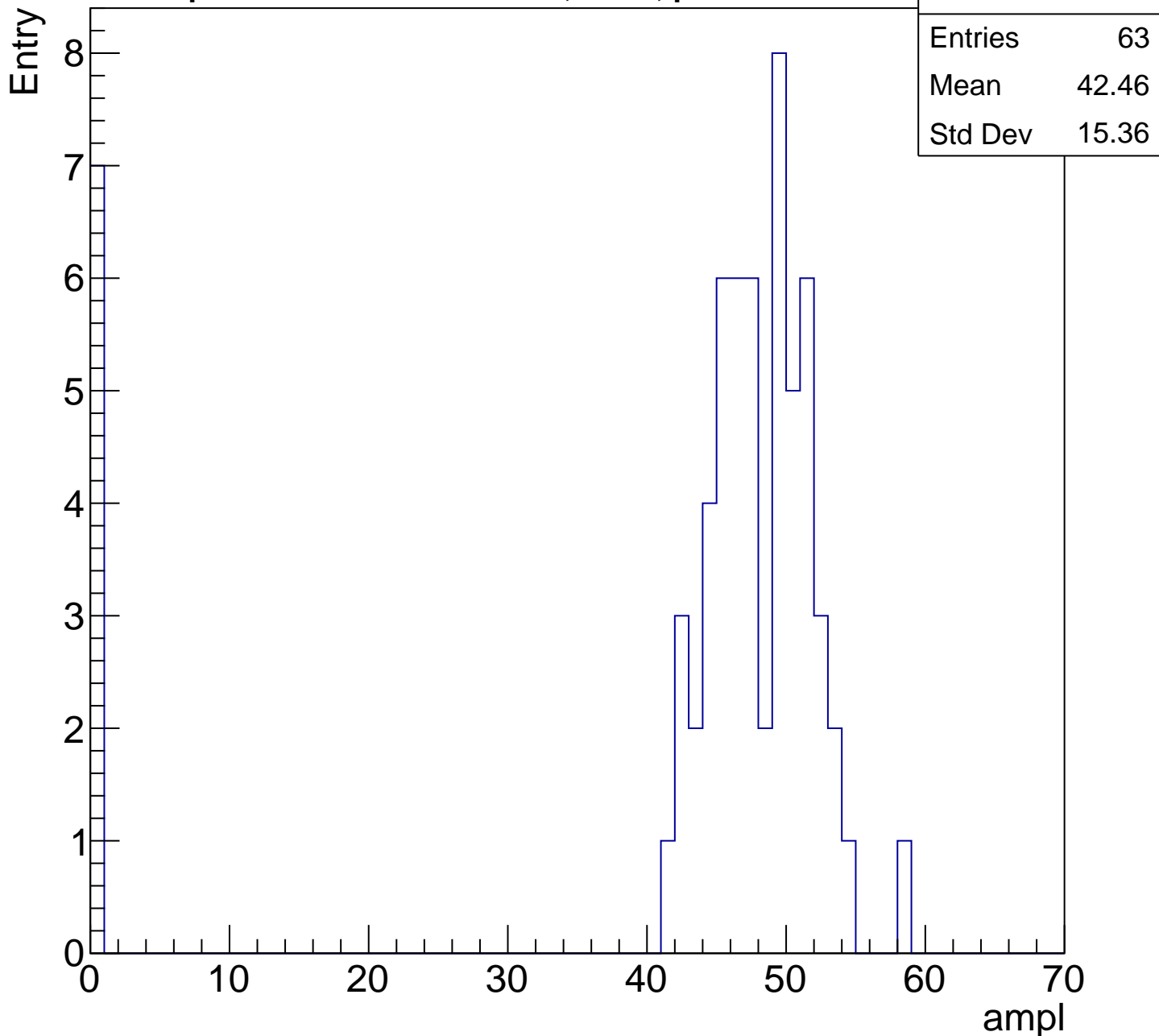
Entries	75
Mean	36.21
Std Dev	14.77

Entry



B1L103S, U5-ch98, adc3

calib_packv5_041523_1651.root, FC#0, port C2

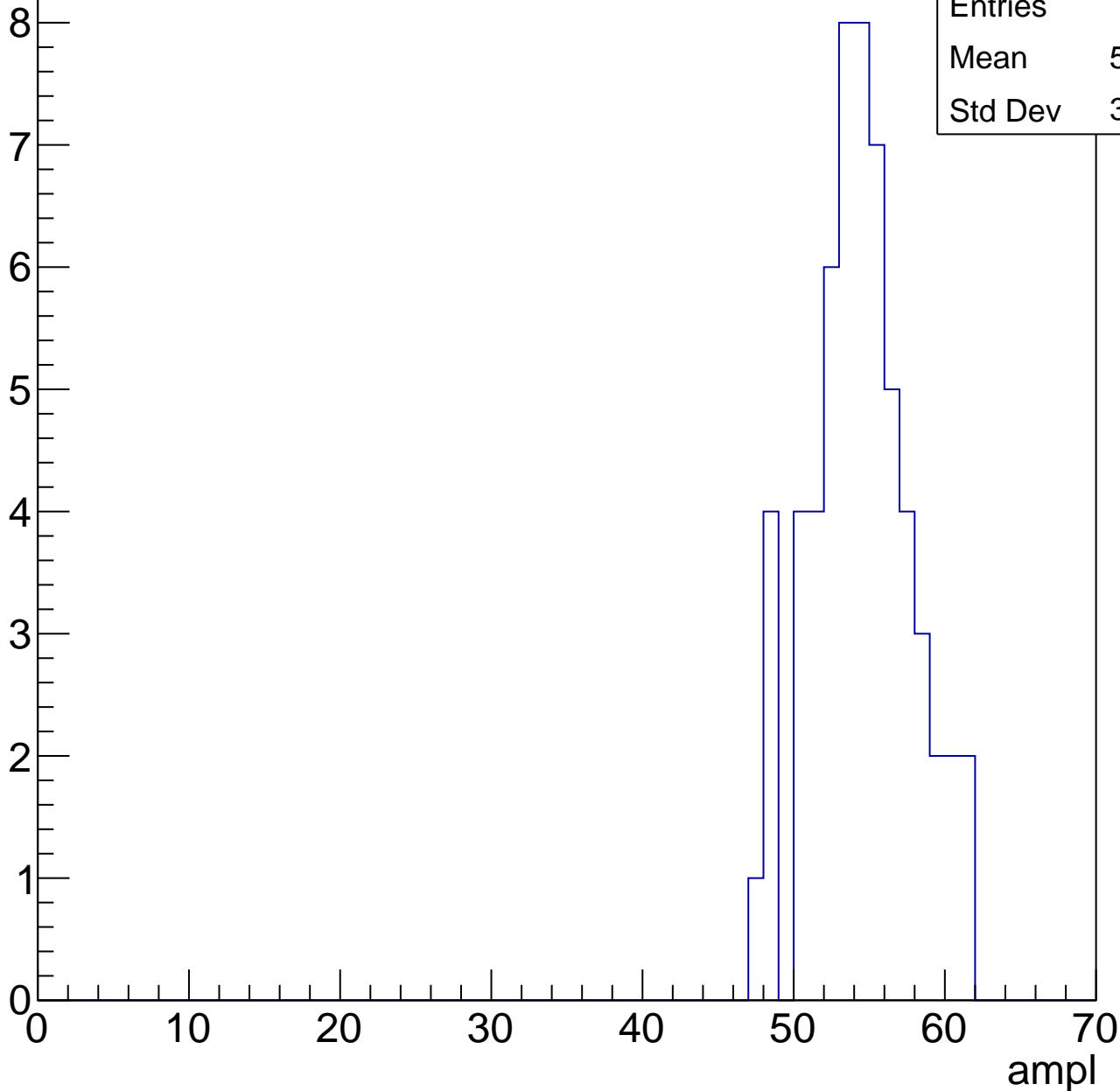


B1L103S, U5-ch98, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	53.97
Std Dev	3.306

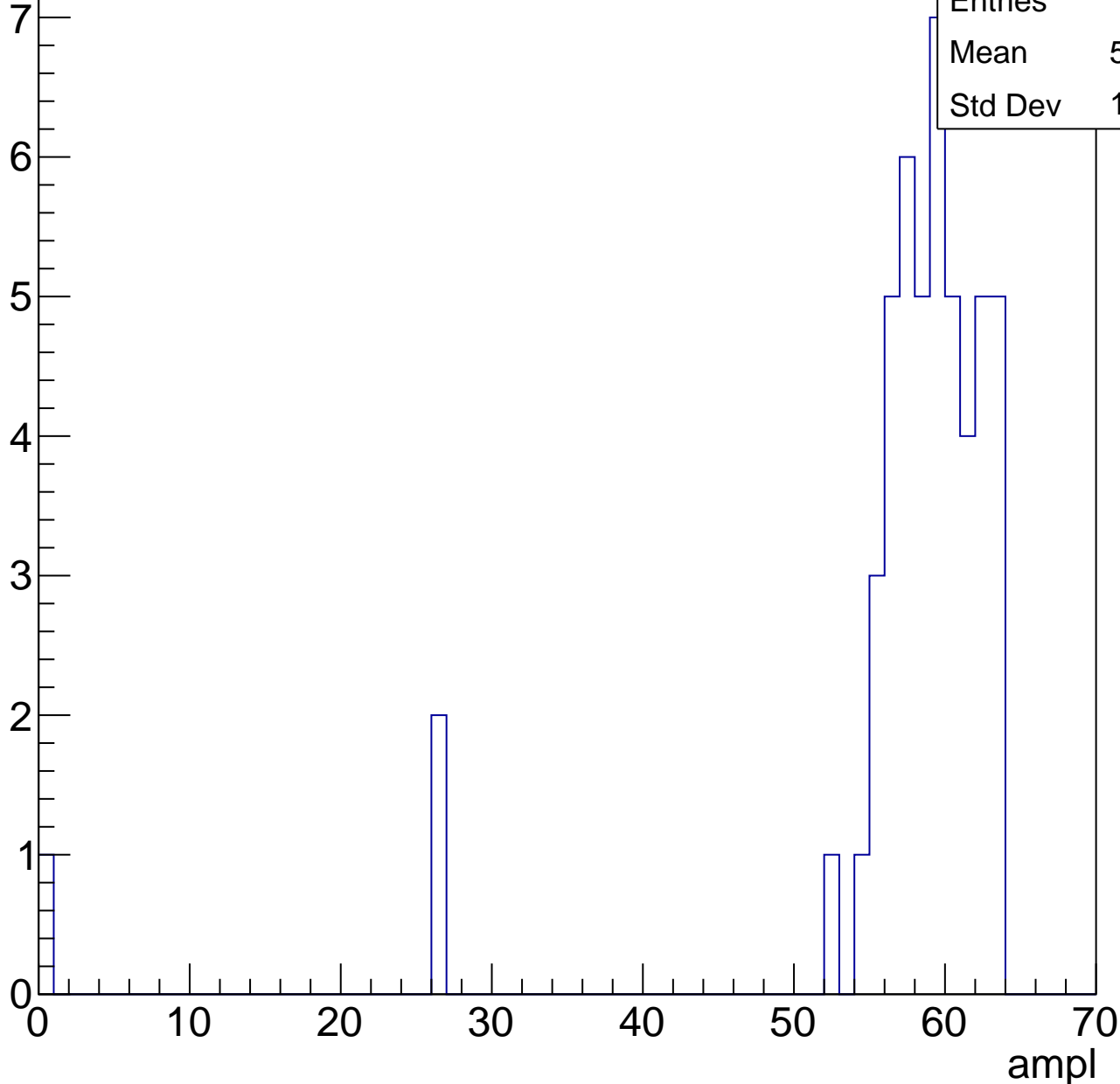


B1L103S, U5-ch98, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

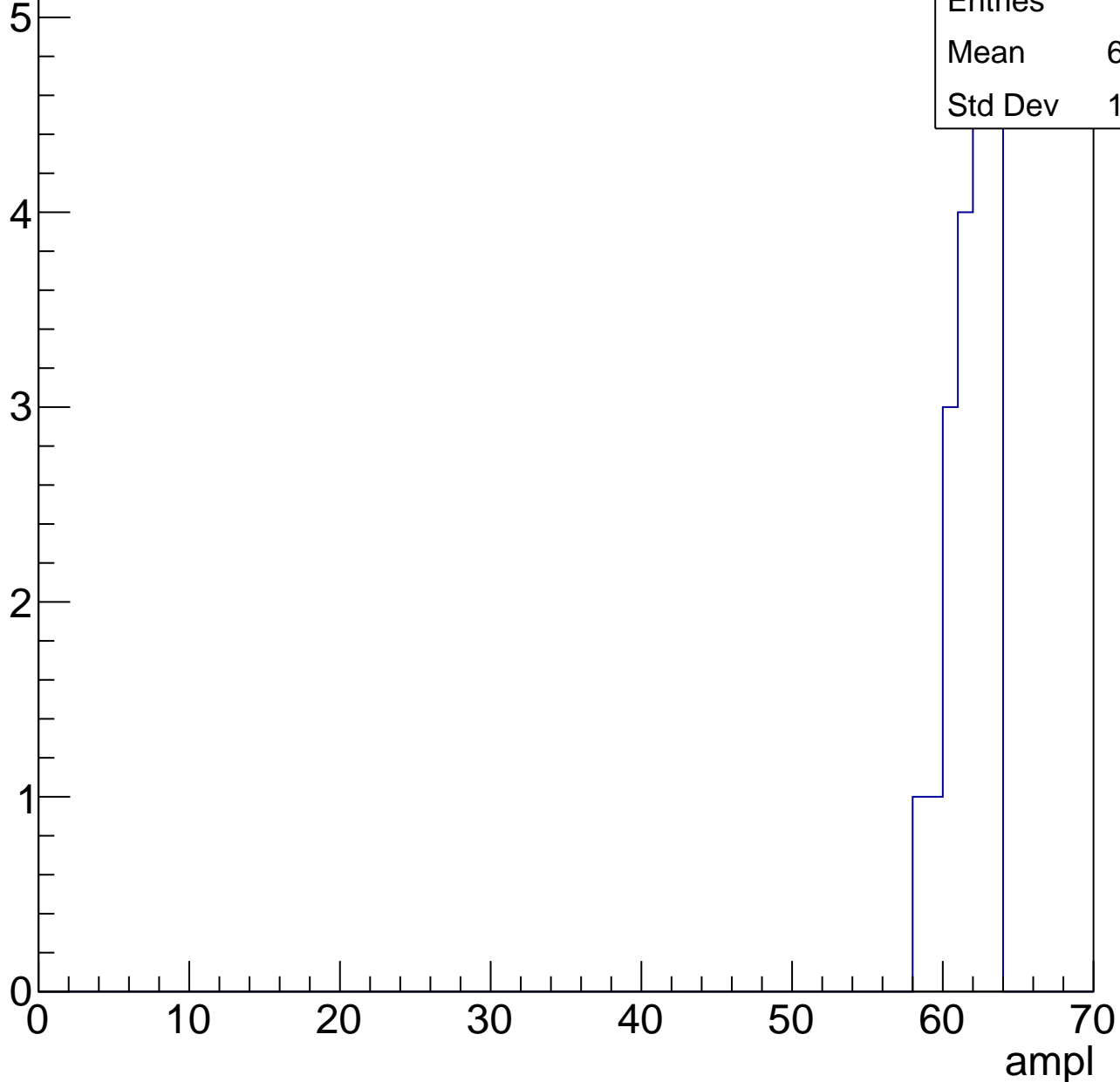
Entries	50
Mean	56.34
Std Dev	10.63



B1L103S, U5-ch98, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch98, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

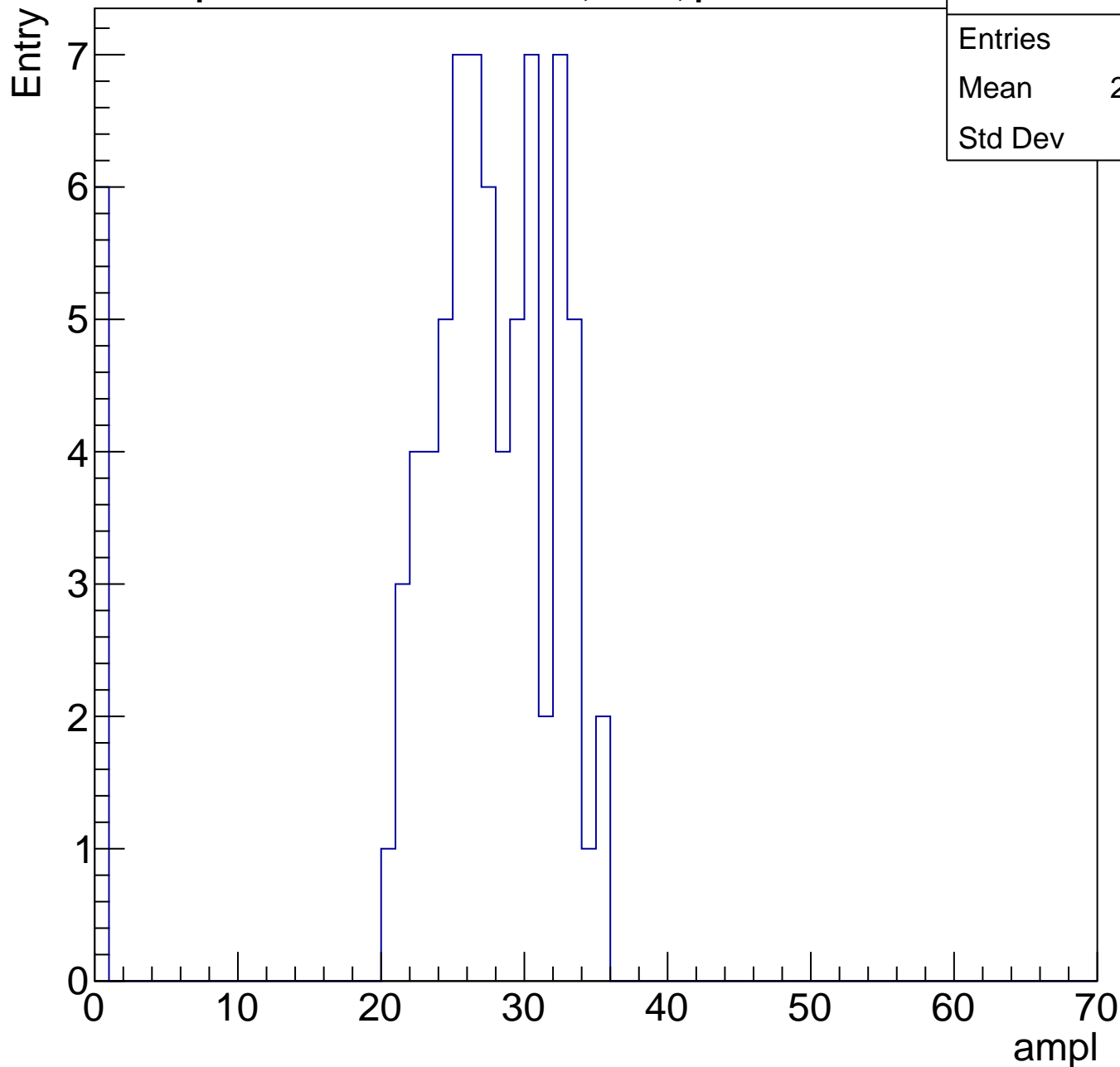
18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U5-ch99, adc0

calib_packv5_041523_1651.root, FC#0, port C2

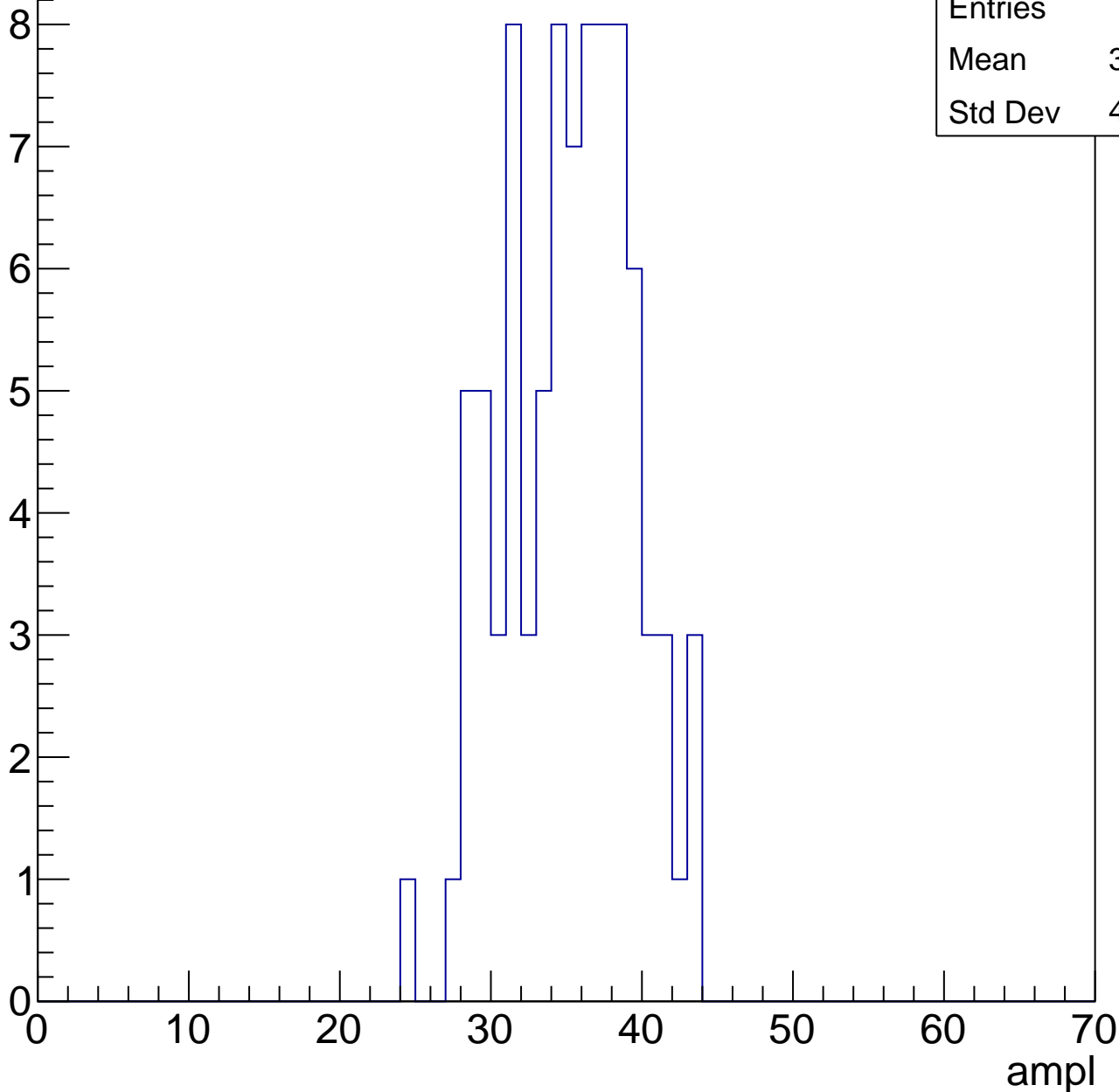


B1L103S, U5-ch99, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	86
Mean	34.74
Std Dev	4.169

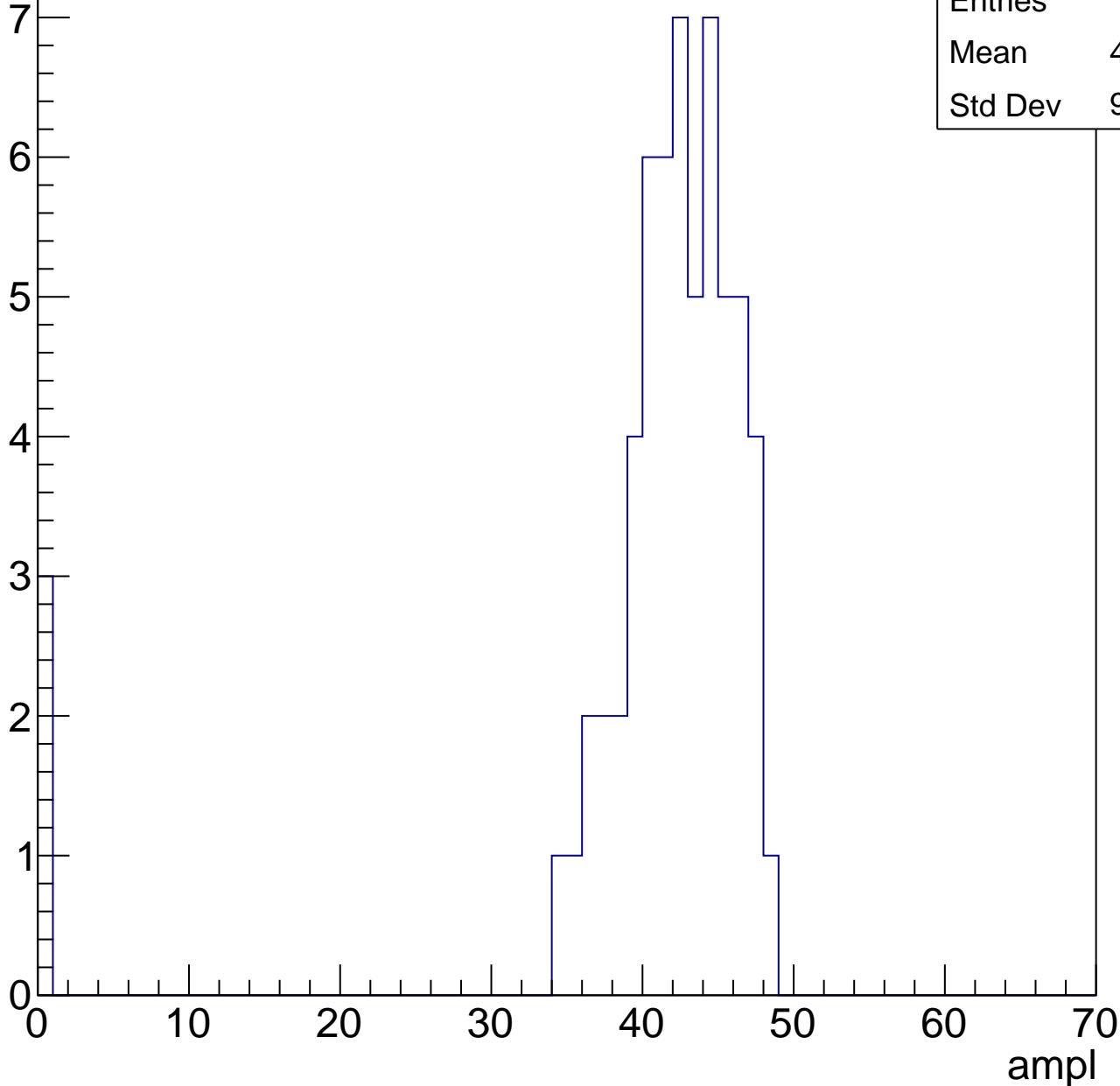


B1L103S, U5-ch99, adc2

calib_packv5_041523_1651.root, FC#0, port C2

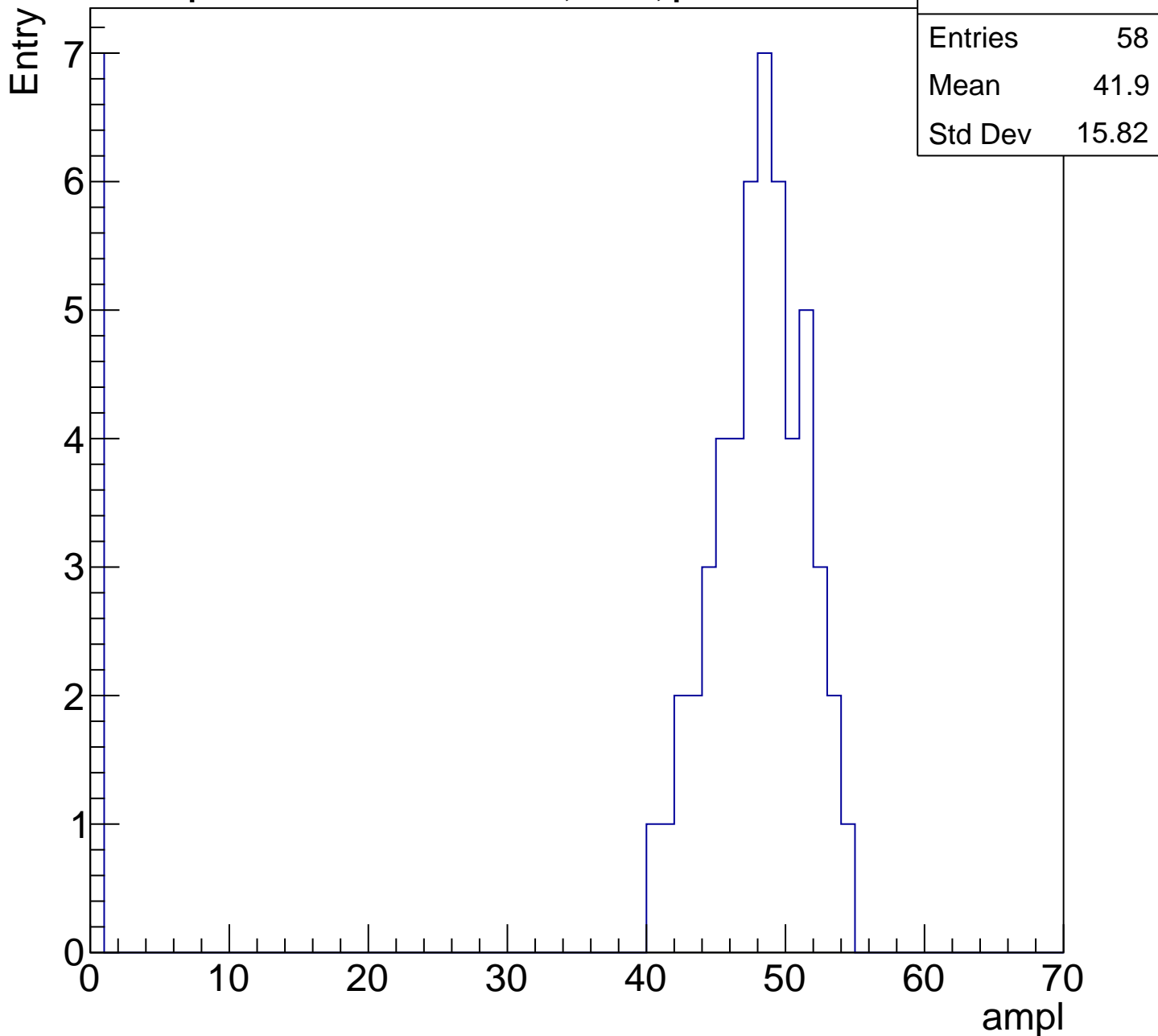
Entry

Entries	61
Mean	40.02
Std Dev	9.649



B1L103S, U5-ch99, adc3

calib_packv5_041523_1651.root, FC#0, port C2

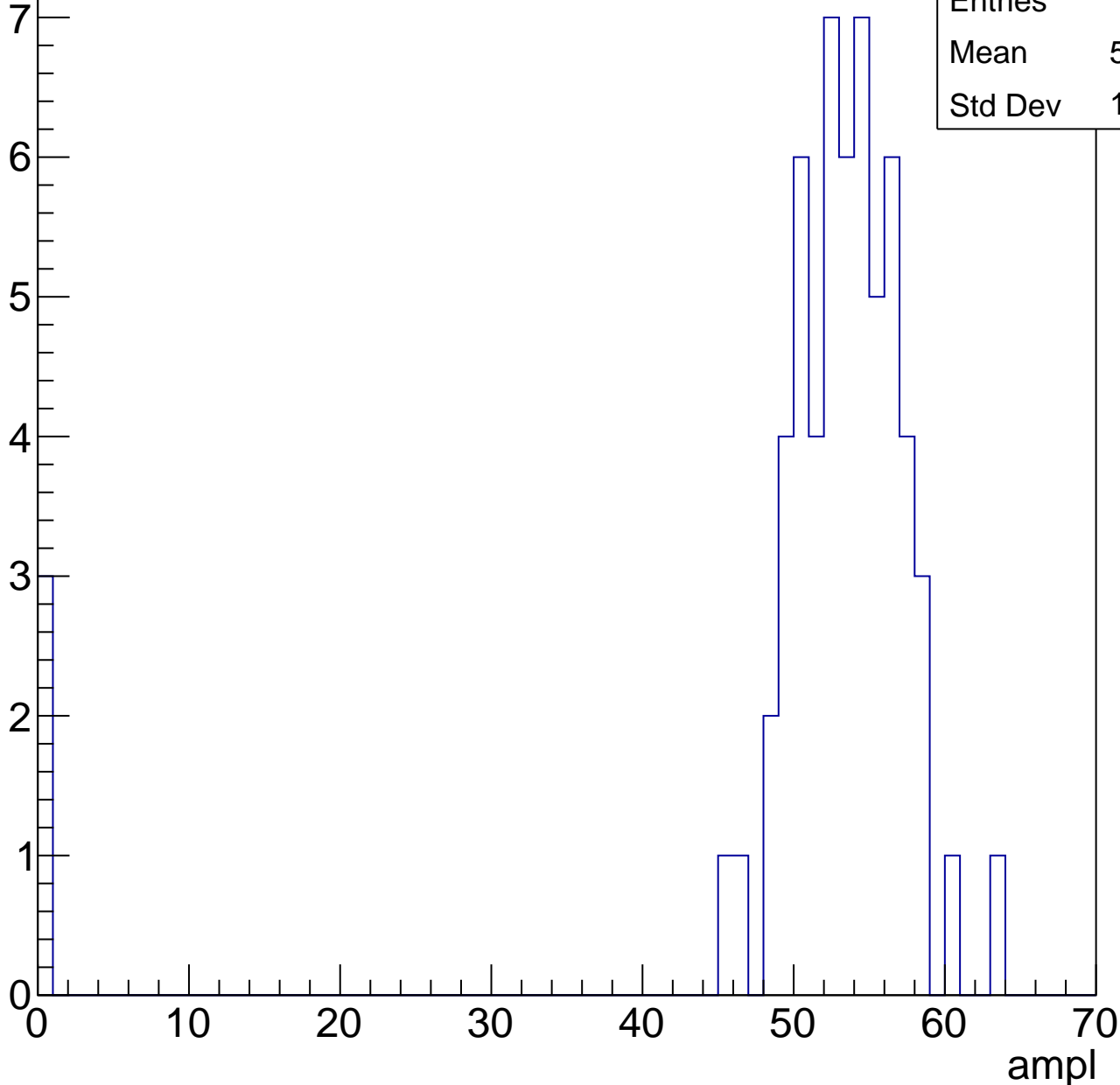


B1L103S, U5-ch99, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	50.54
Std Dev	11.96

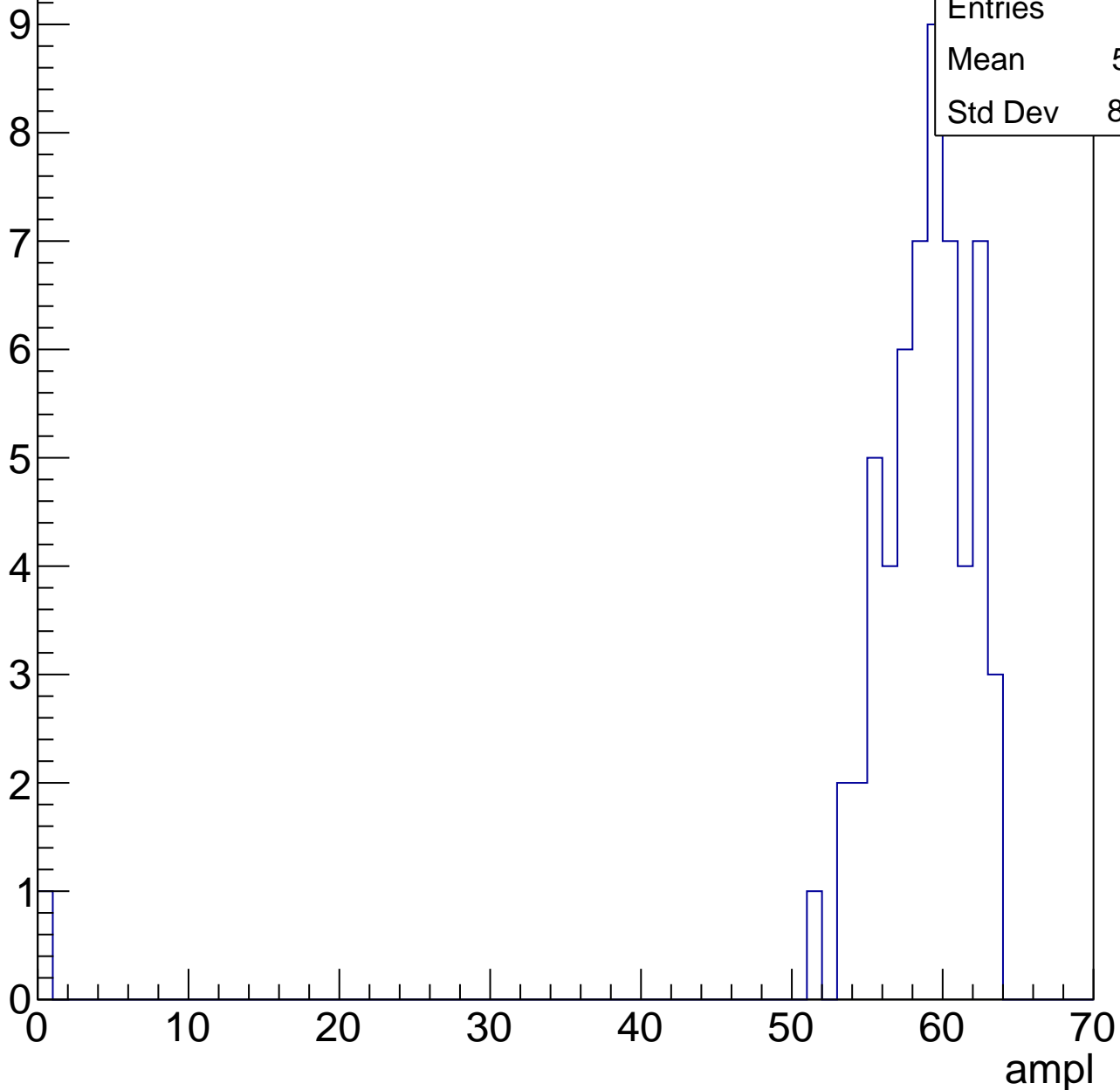


B1L103S, U5-ch99, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	57.41
Std Dev	8.096

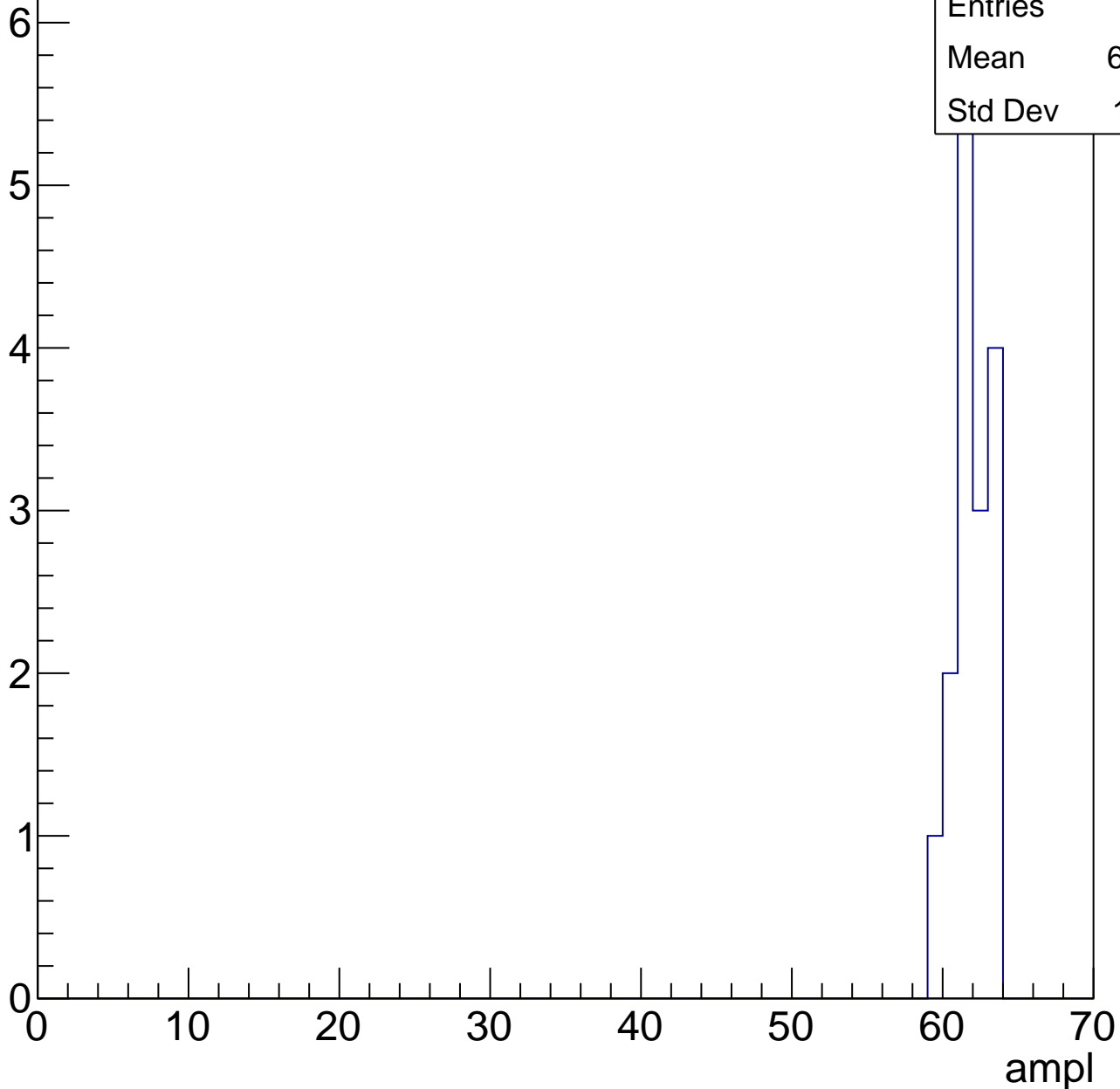


B1L103S, U5-ch99, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	16
Mean	61.44
Std Dev	1.171



B1L103S, U5-ch99, adc7

calib_packv5_041523_1651.root, FC#0, port C2

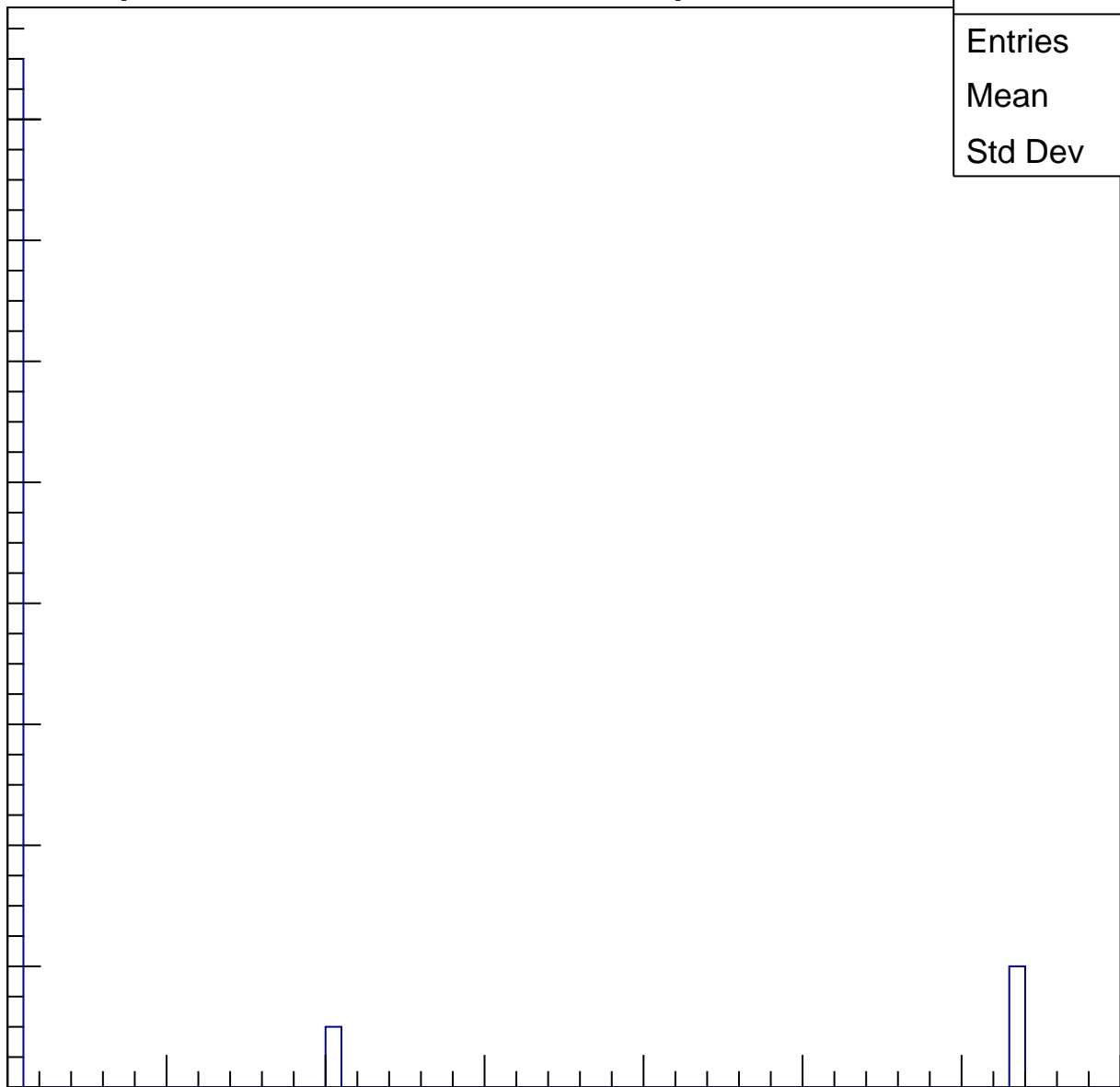
Entries	20
Mean	7.3
Std Dev	19.07

Entry

16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

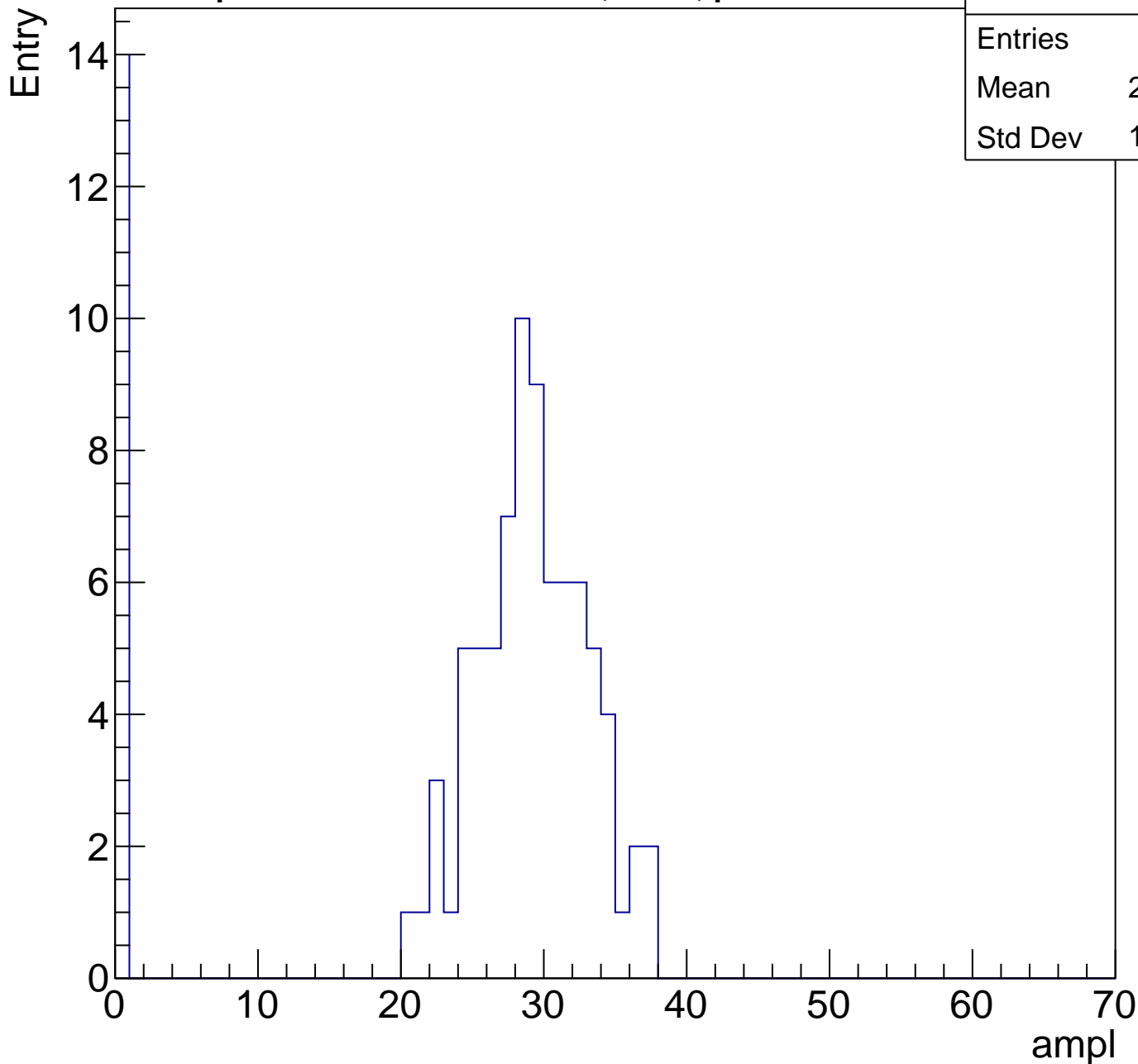
ampl



B1L103S, U5-ch100, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	93
Mean	24.46
Std Dev	10.88

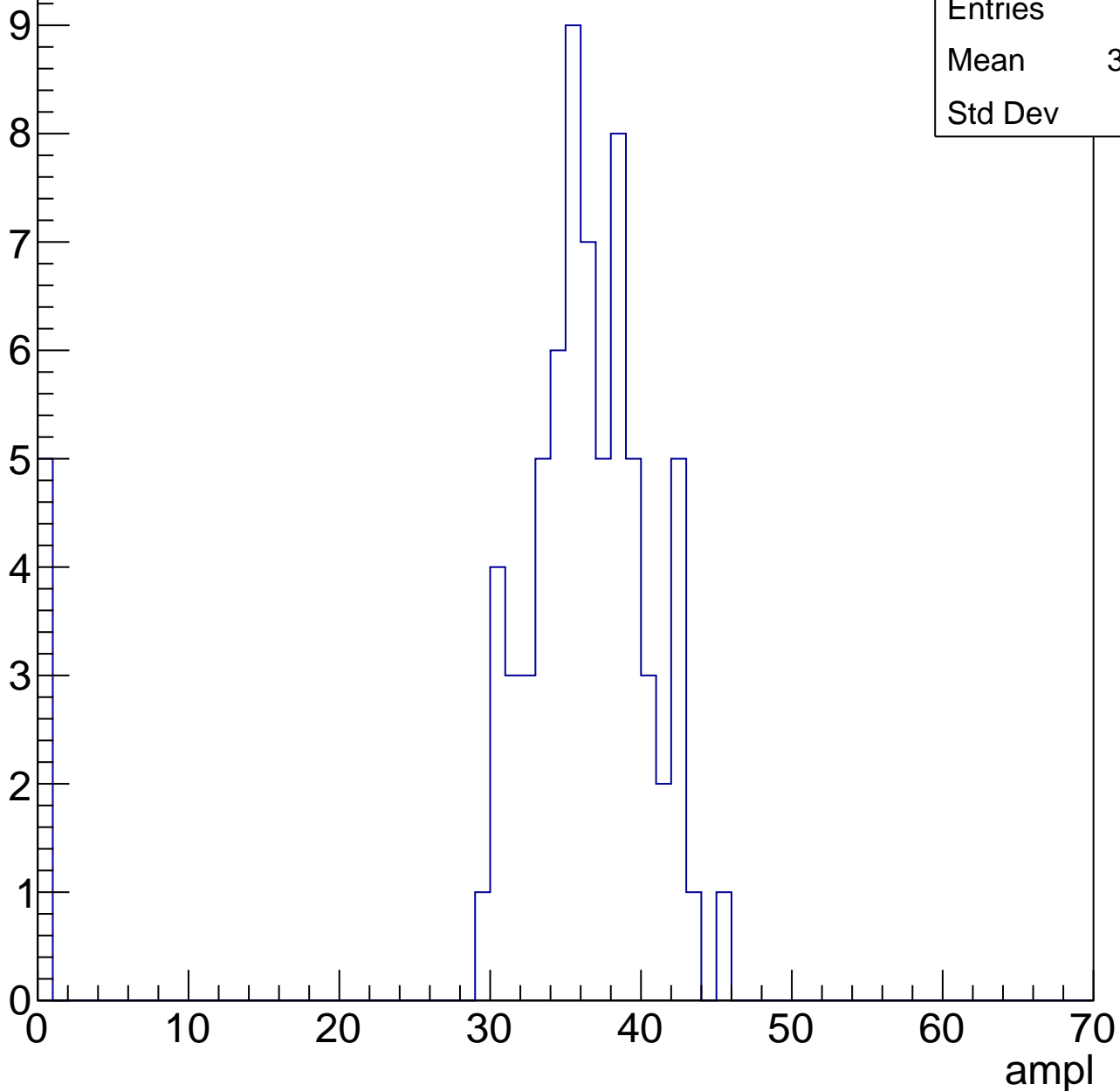


B1L103S, U5-ch100, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	33.67
Std Dev	9.77

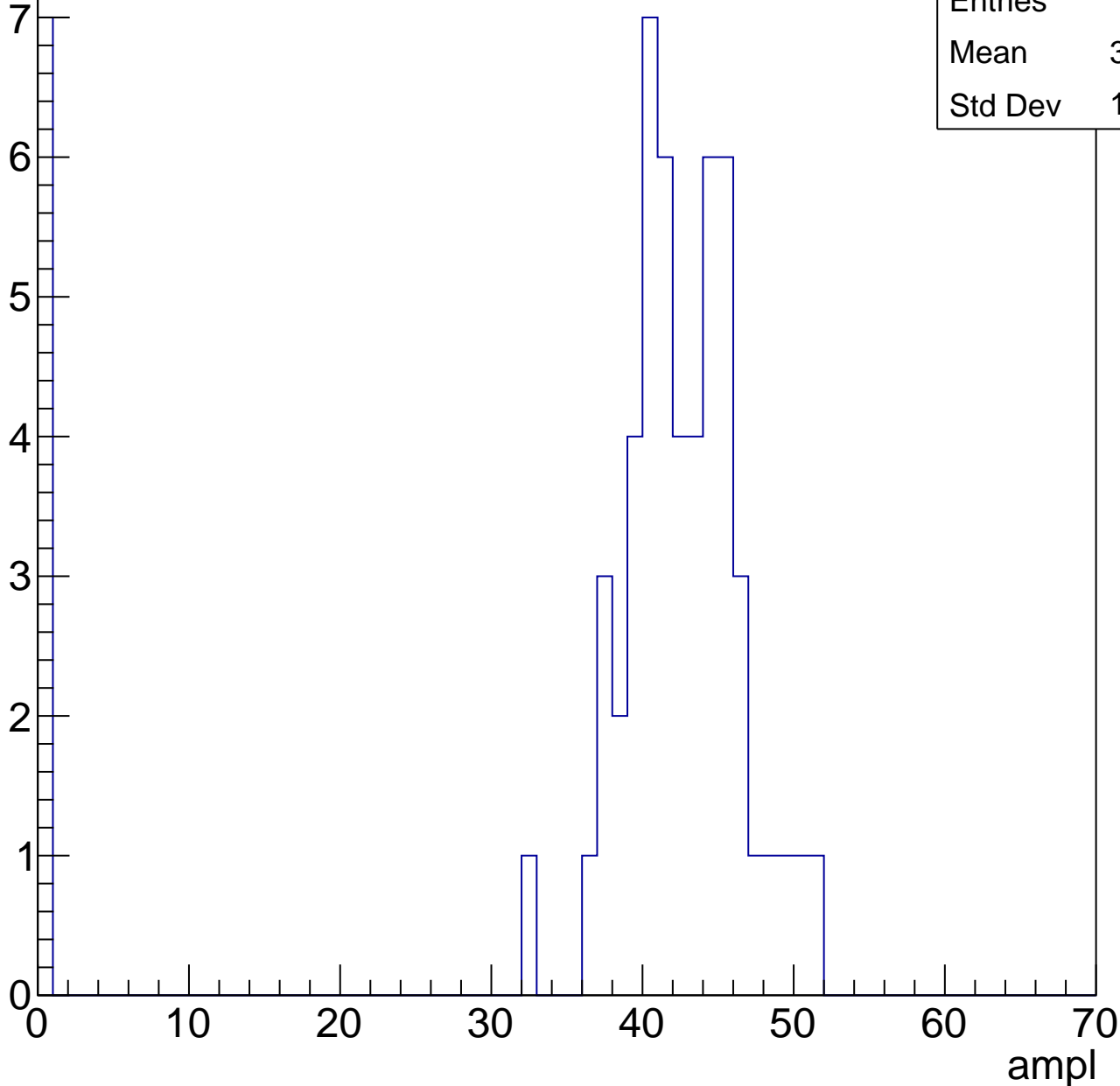


B1L103S, U5-ch100, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	37.19
Std Dev	14.07

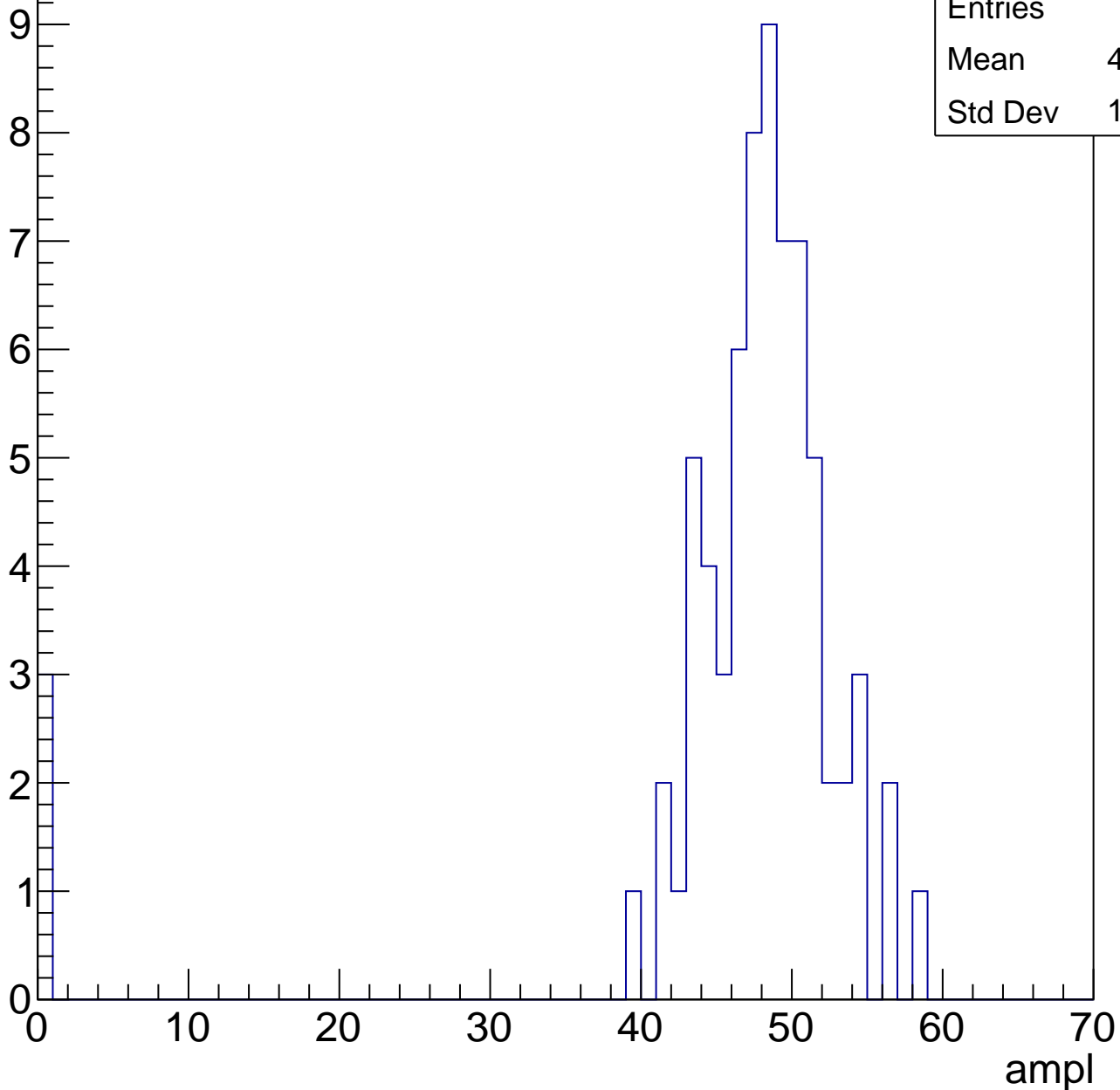


B1L103S, U5-ch100, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	45.96
Std Dev	10.33

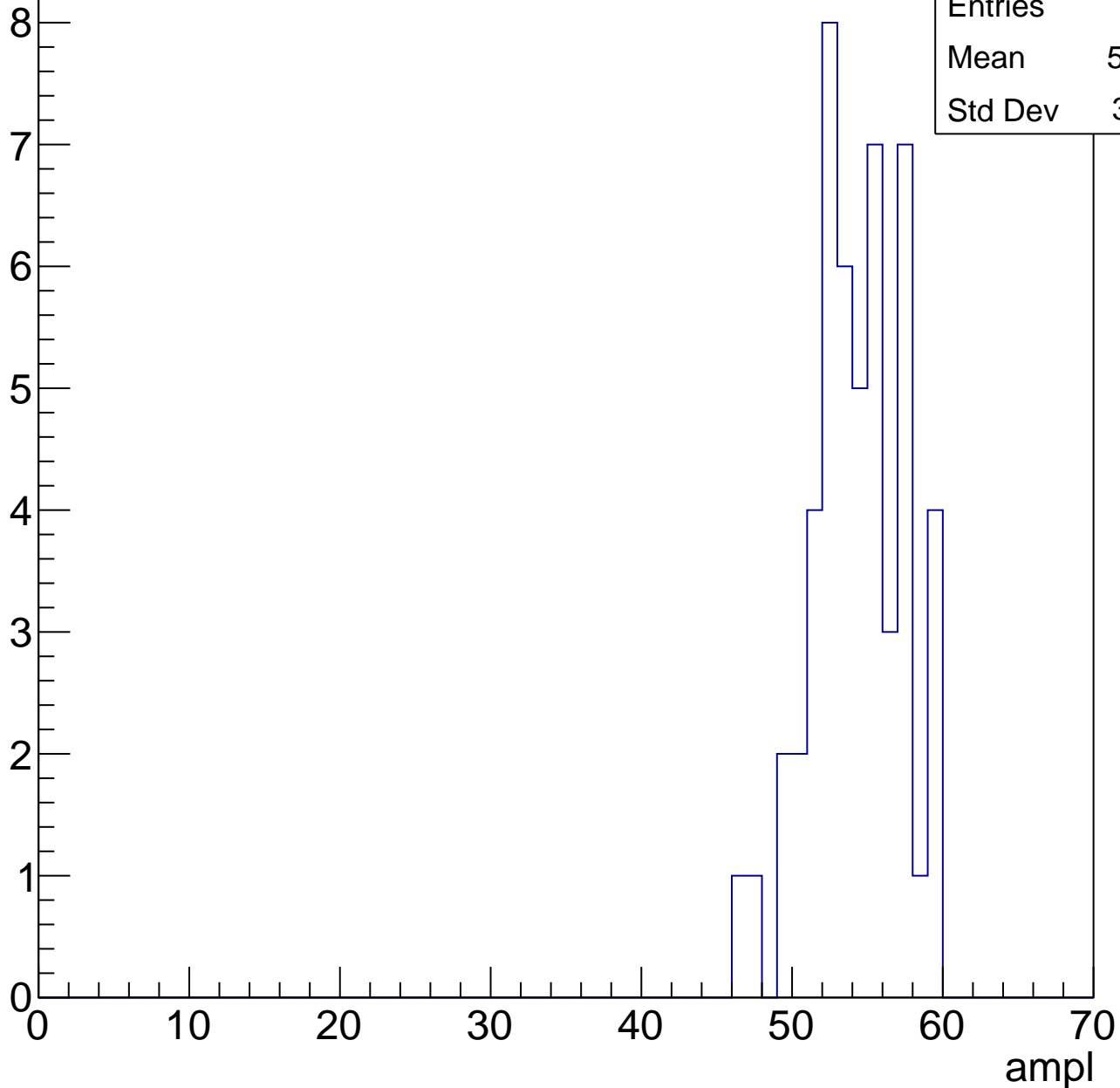


B1L103S, U5-ch100, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

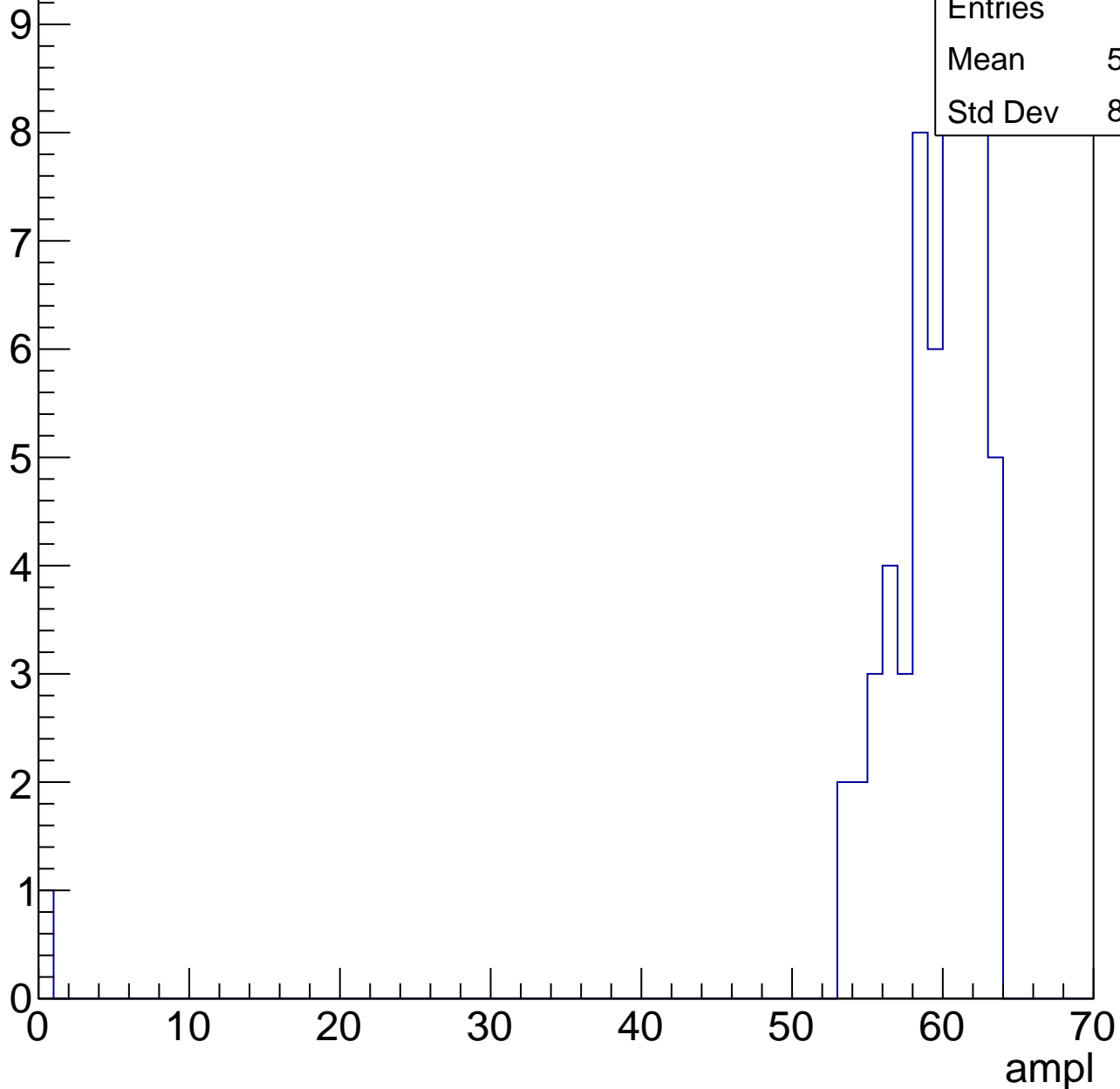
Entries	51
Mean	53.82
Std Dev	3.021



B1L103S, U5-ch100, adc5

calib_packv5_041523_1651.root, FC#0, port C2

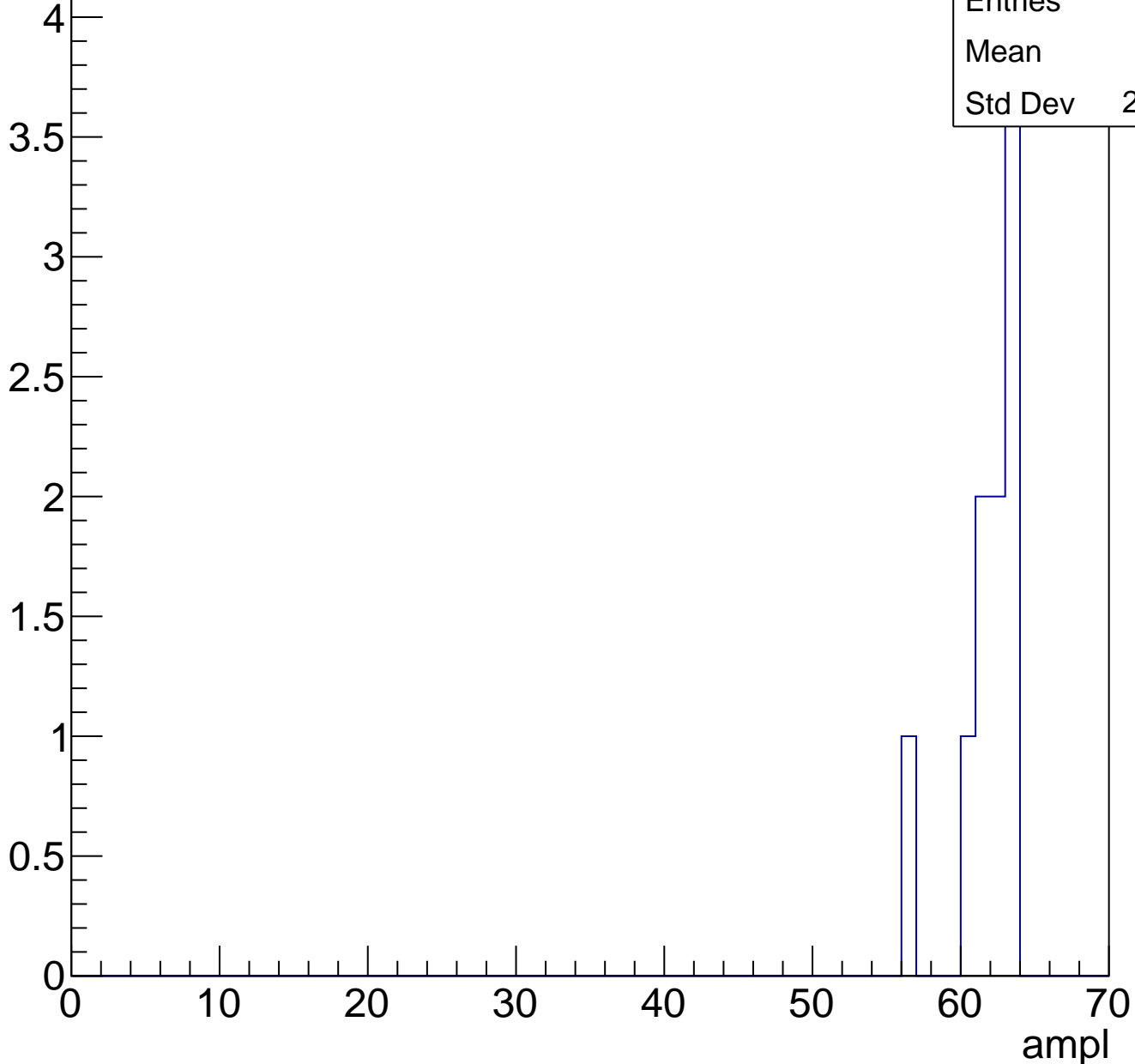
Entry



B1L103S, U5-ch100, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch100, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry



B1L103S, U5-ch101, adc0

calib_packv5_041523_1651.root, FC#0, port C2

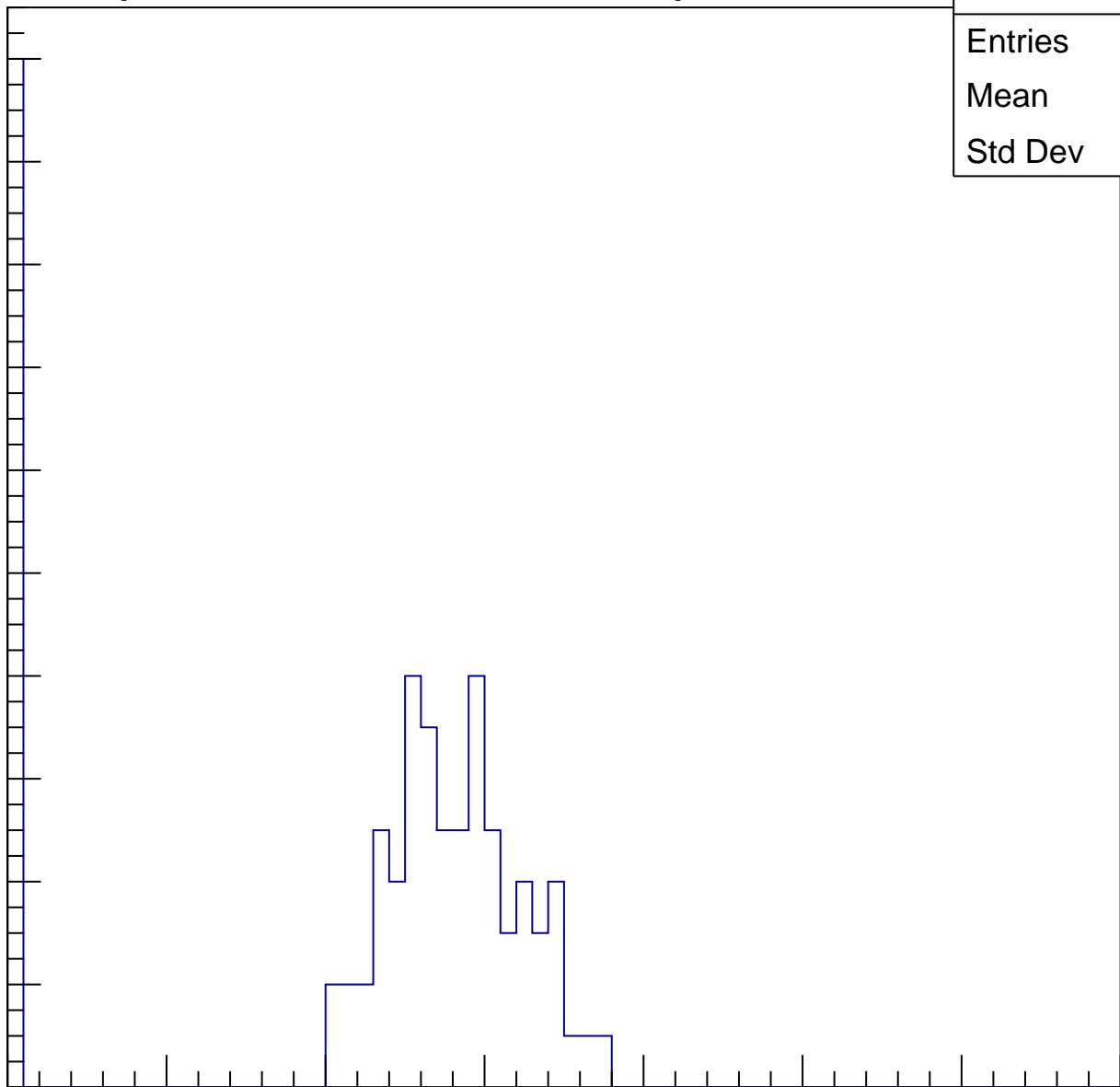
Entries	90
Mean	21.56
Std Dev	12.05

Entry

20
18
16
14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

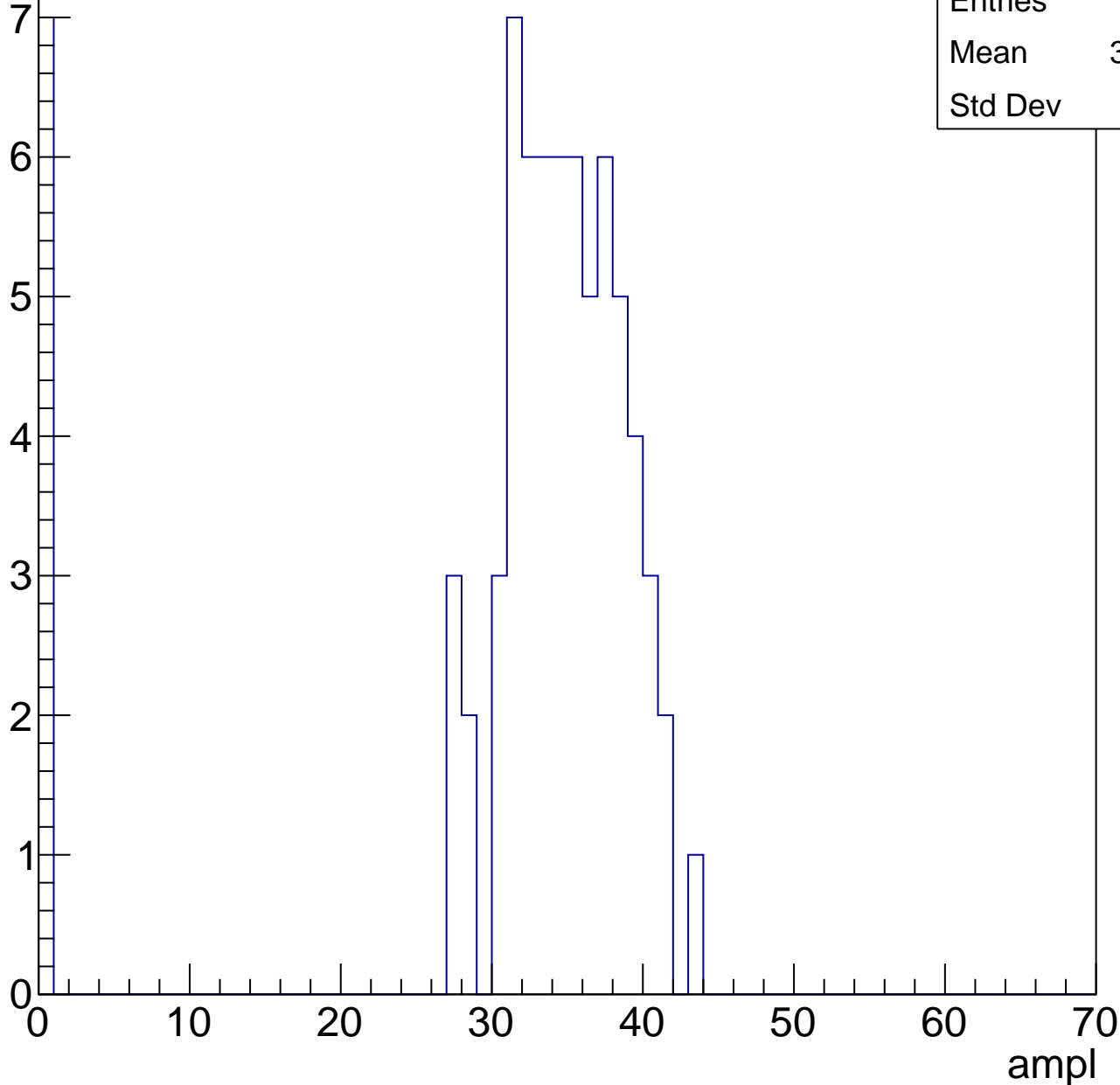


B1L103S, U5-ch101, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	31.12
Std Dev	10.8

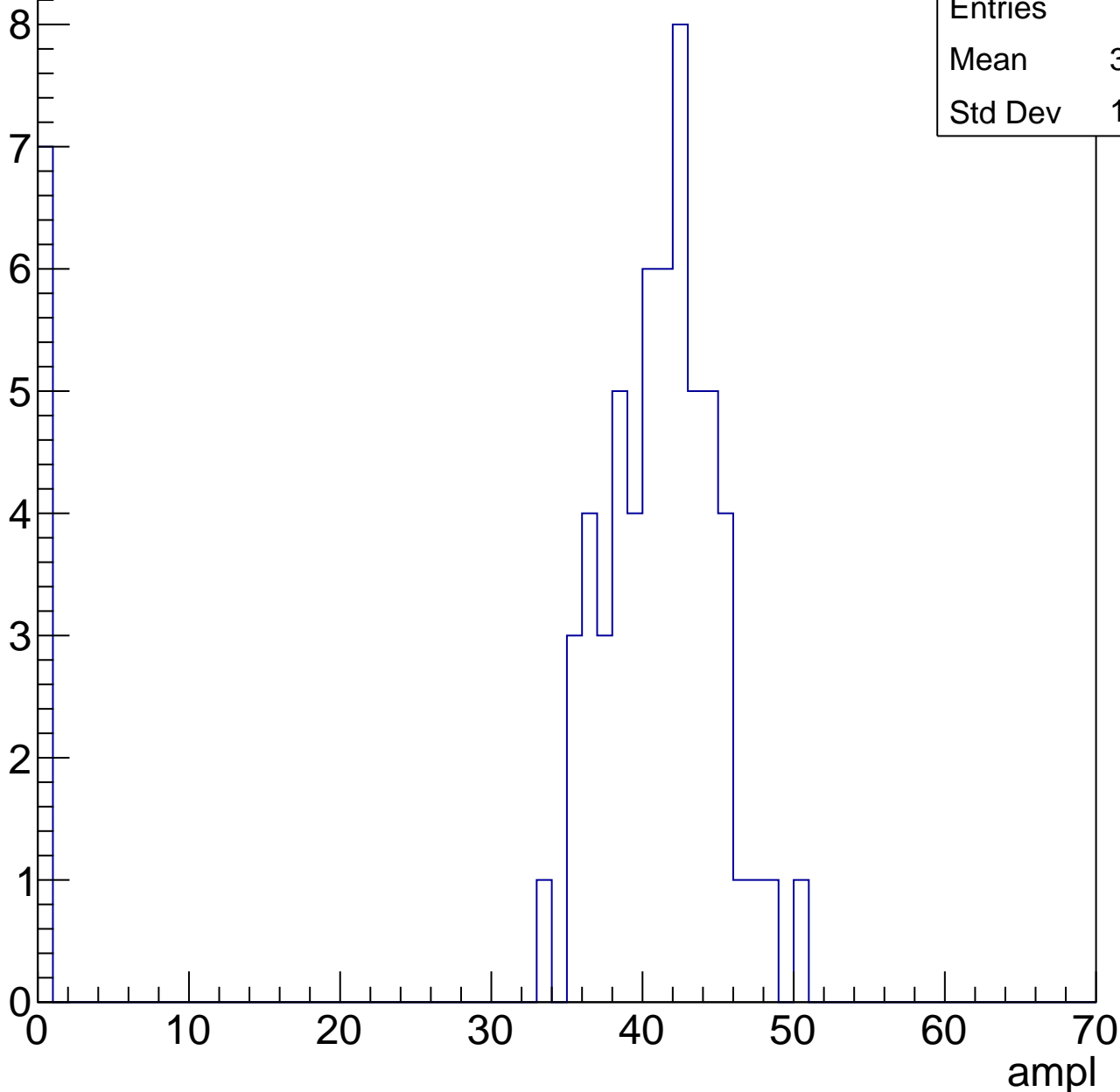


B1L103S, U5-ch101, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

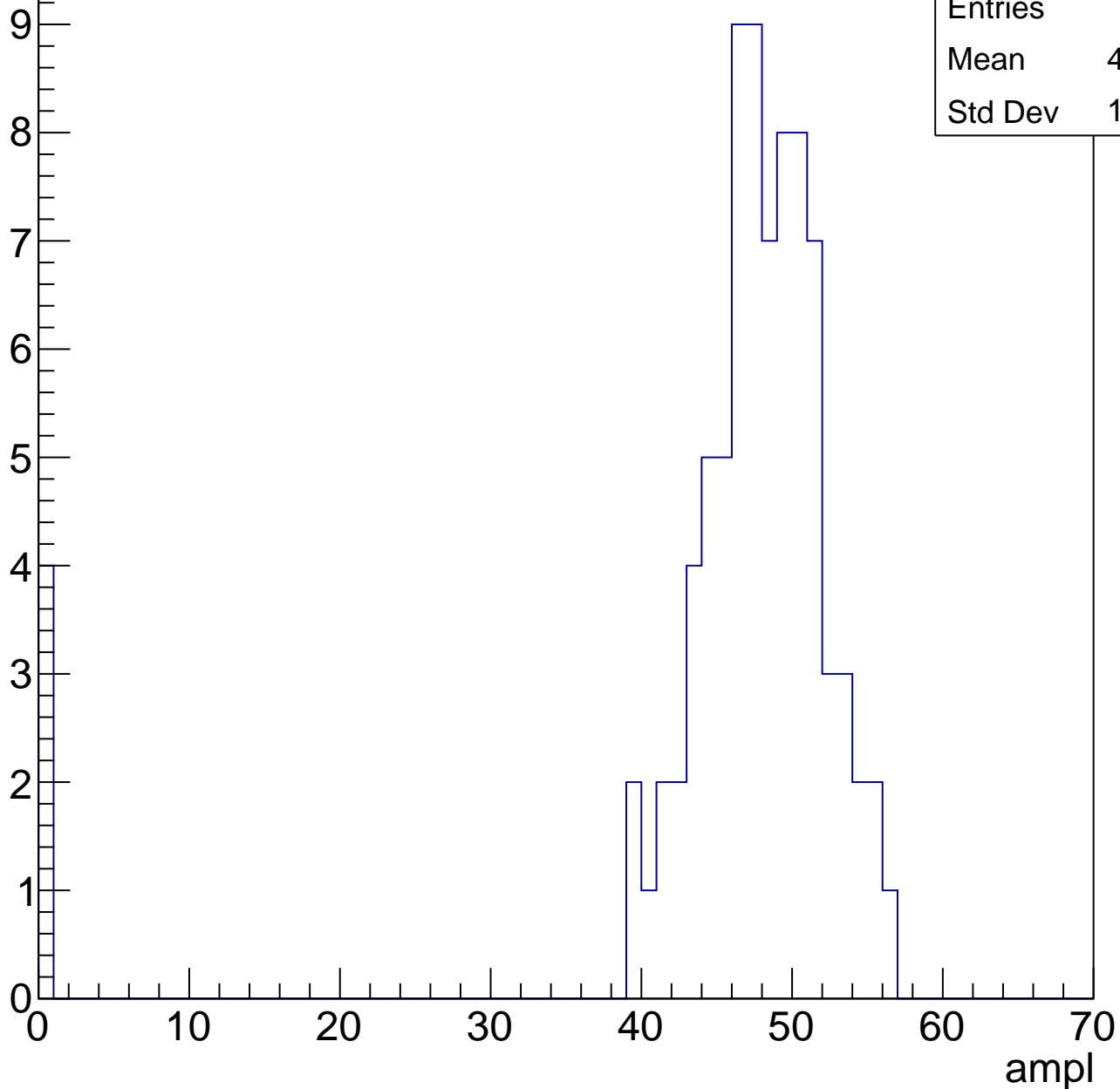
Entries	65
Mean	36.42
Std Dev	13.08



B1L103S, U5-ch101, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

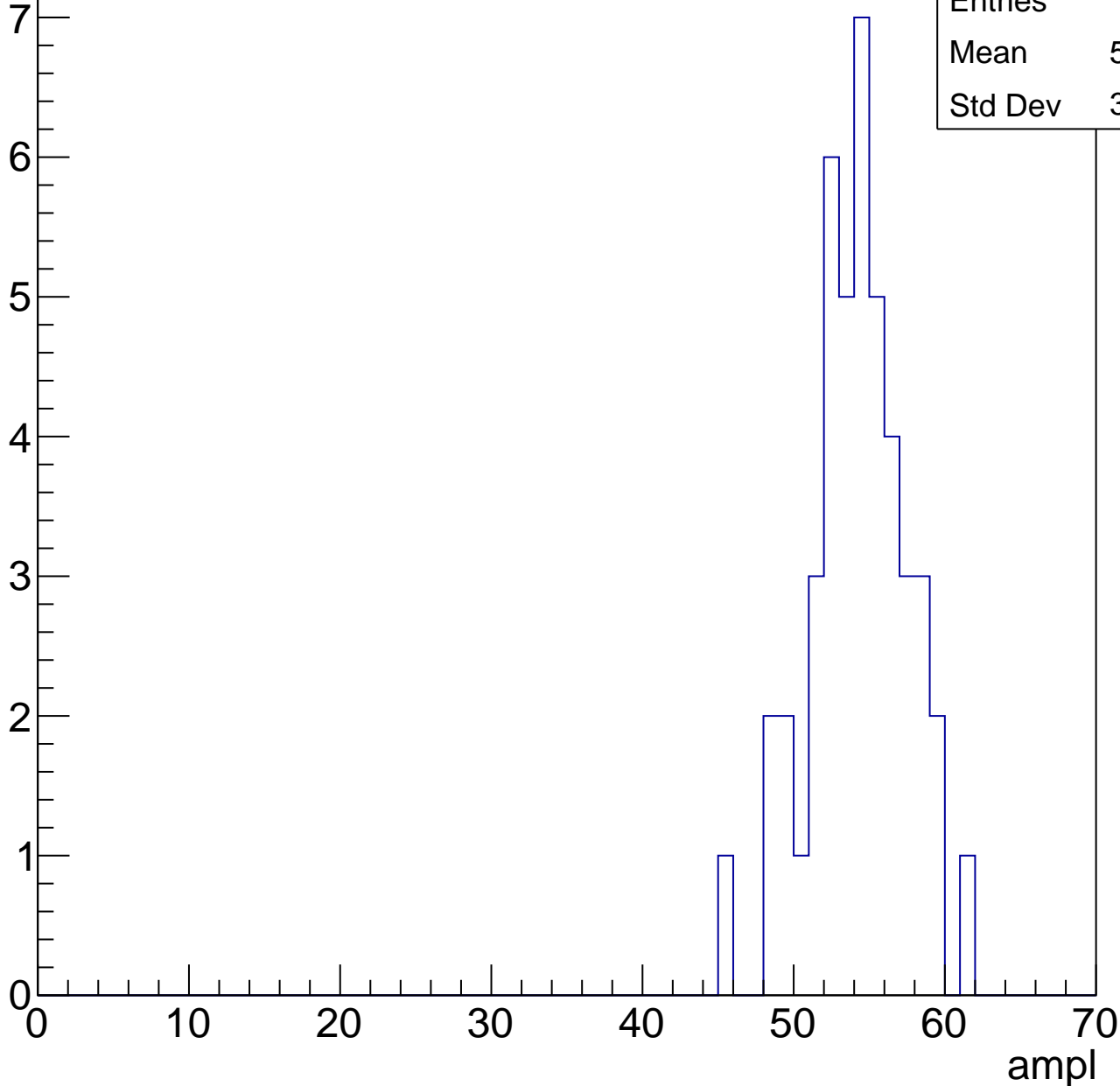


B1L103S, U5-ch101, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	45
Mean	53.78
Std Dev	3.224

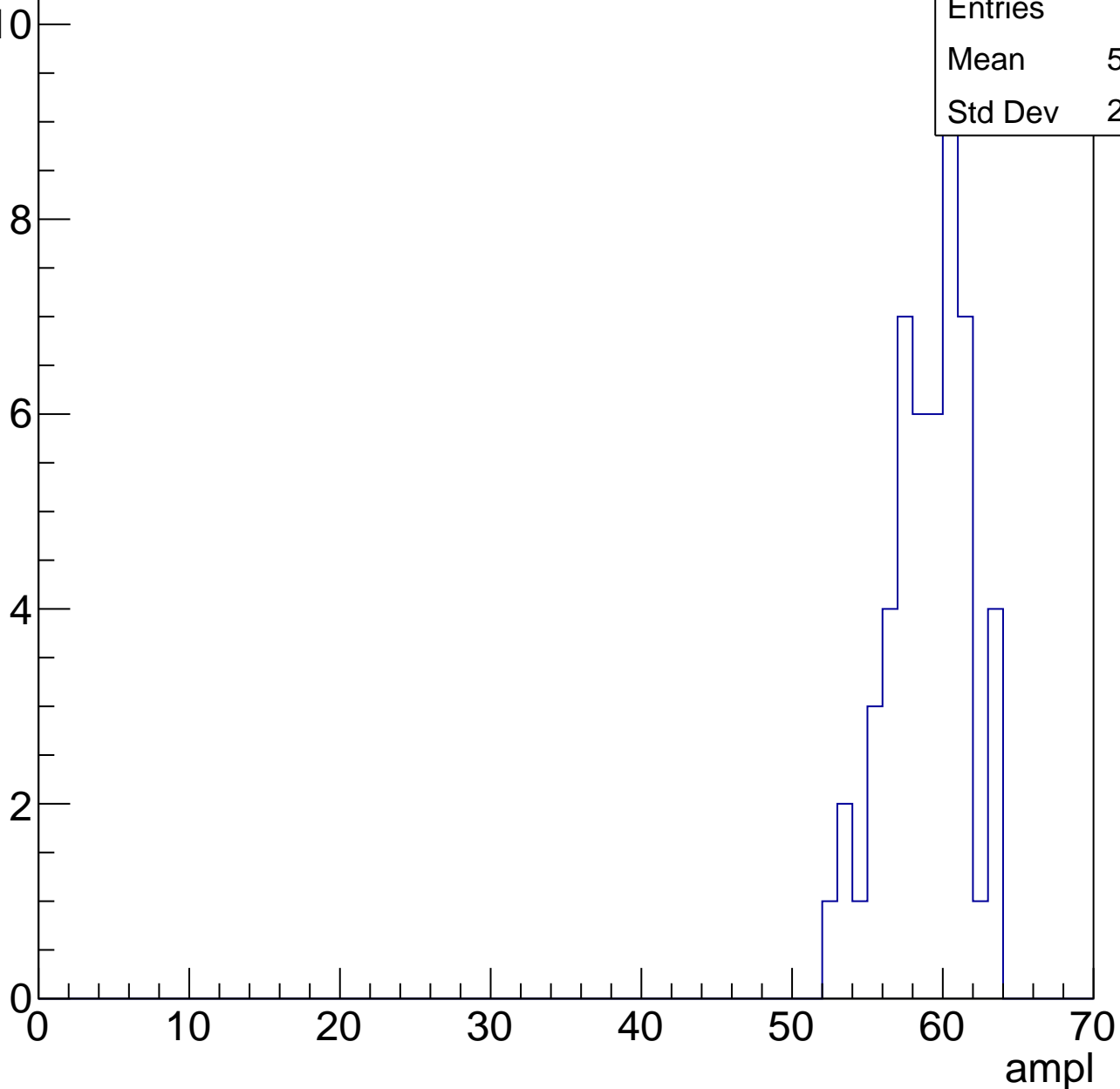


B1L103S, U5-ch101, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	58.52
Std Dev	2.642

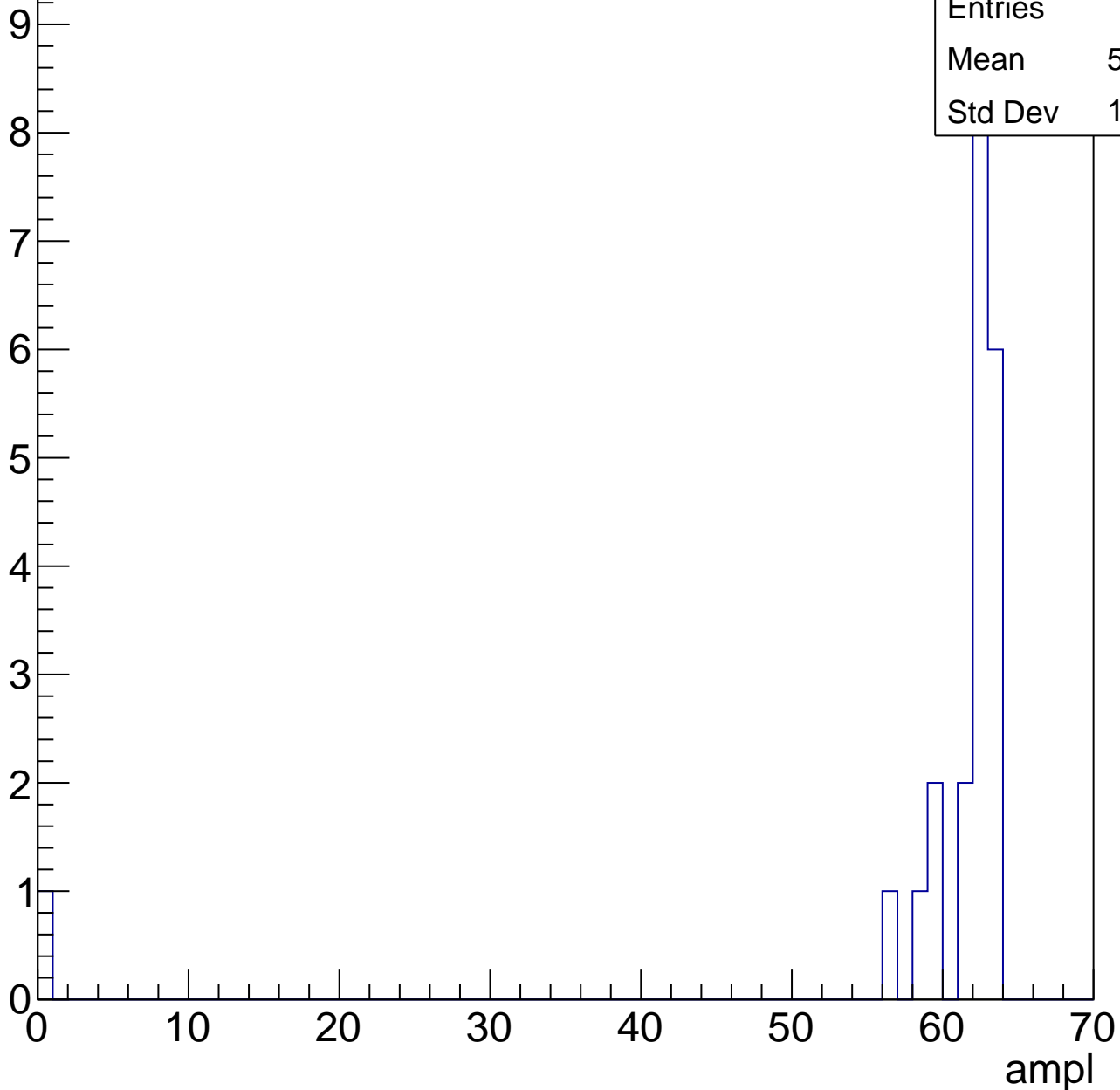


B1L103S, U5-ch101, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	22
Mean	58.64
Std Dev	12.92



B1L103S, U5-ch101, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

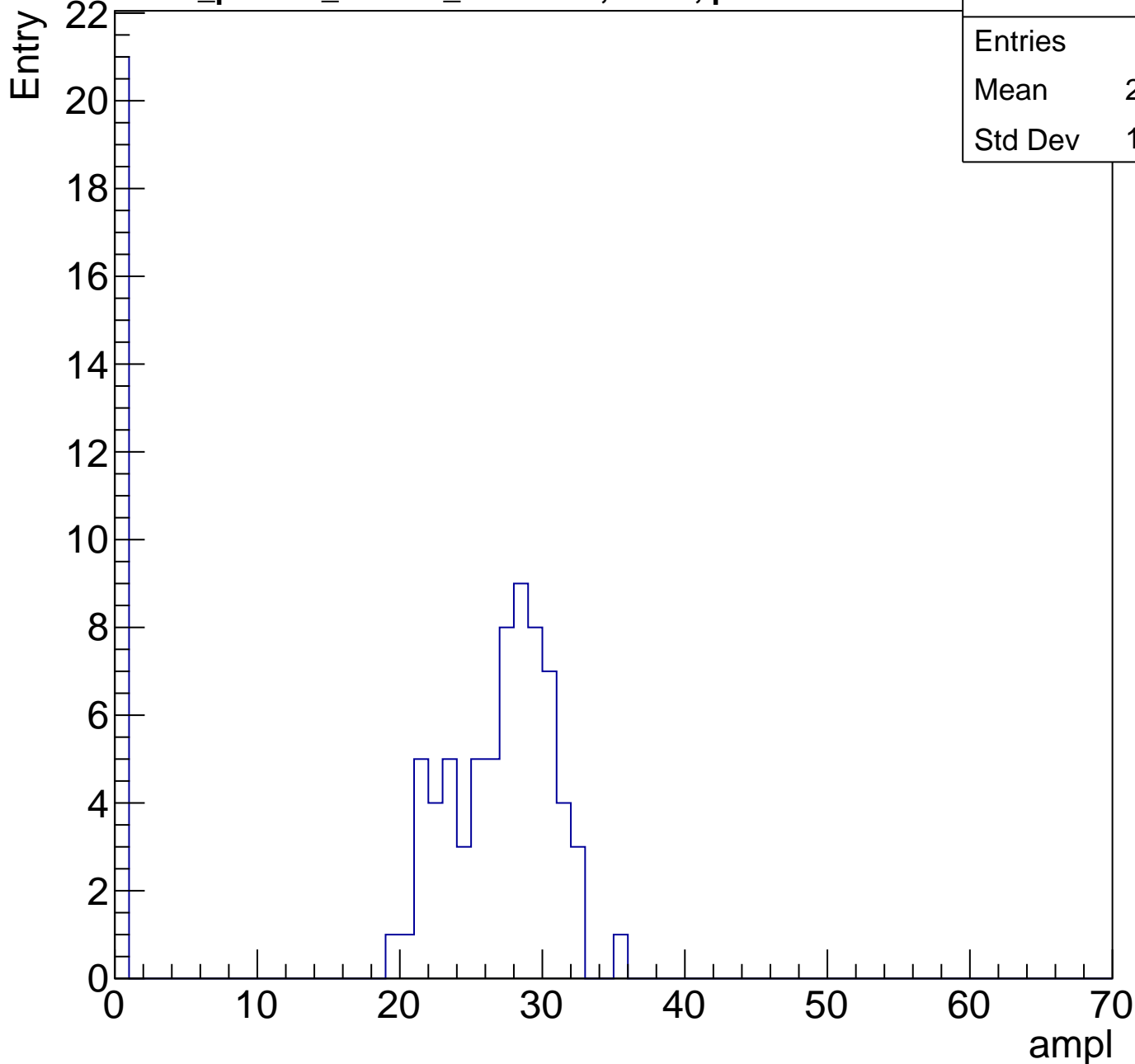
ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U5-ch102, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	90
Mean	20.43
Std Dev	11.67

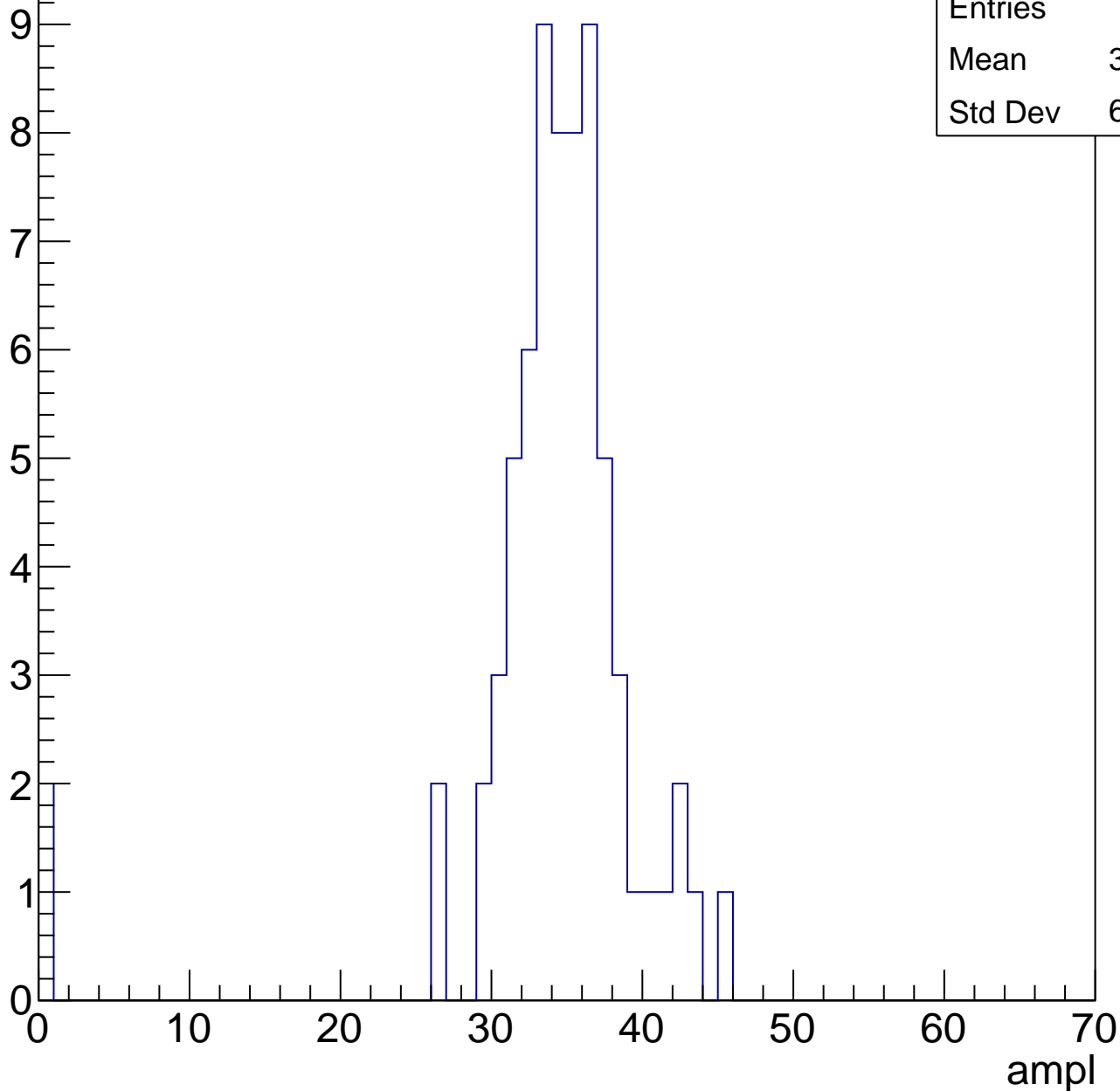


B1L103S, U5-ch102, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	33.49
Std Dev	6.784

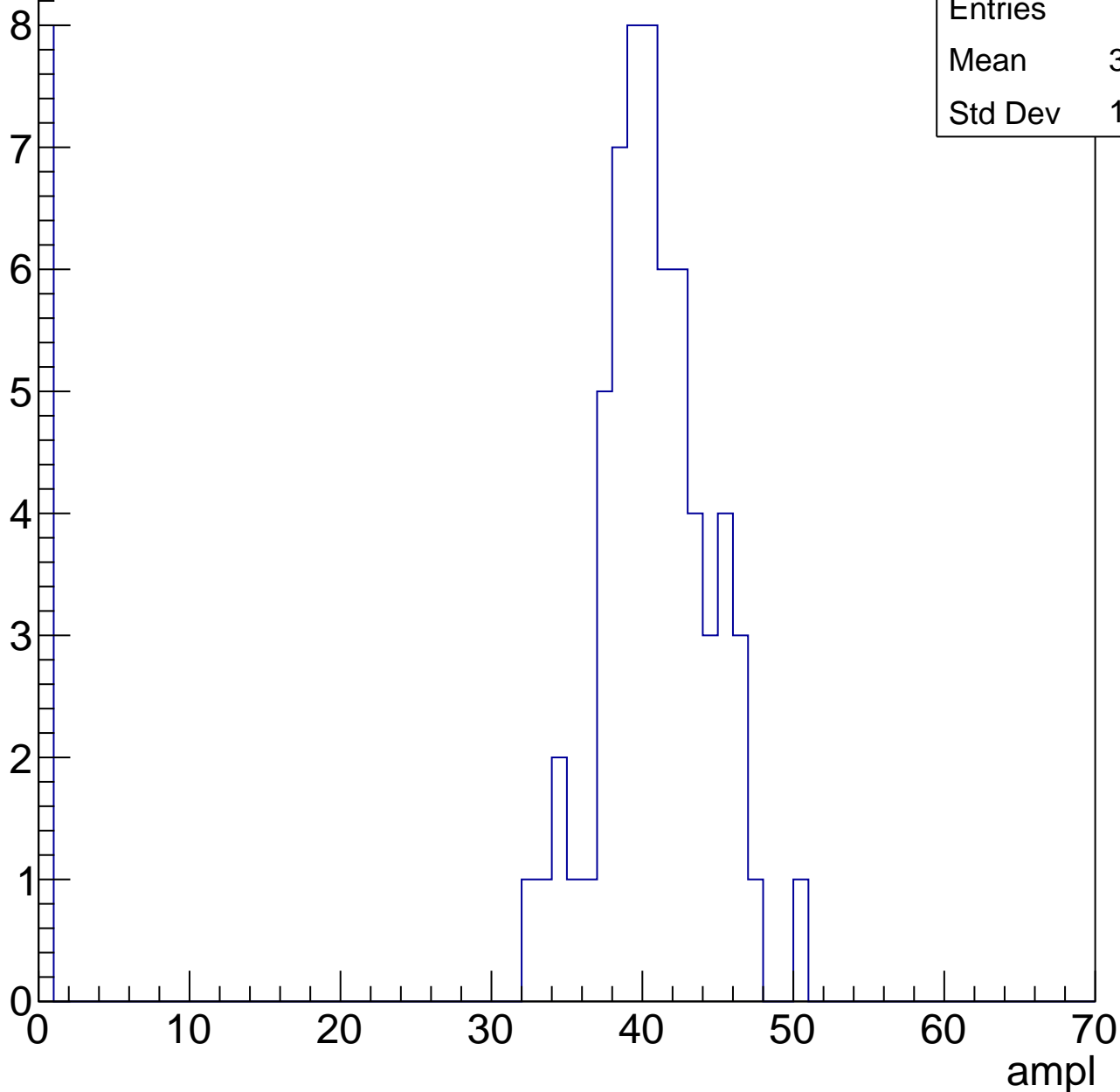


B1L103S, U5-ch102, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	35.77
Std Dev	13.27

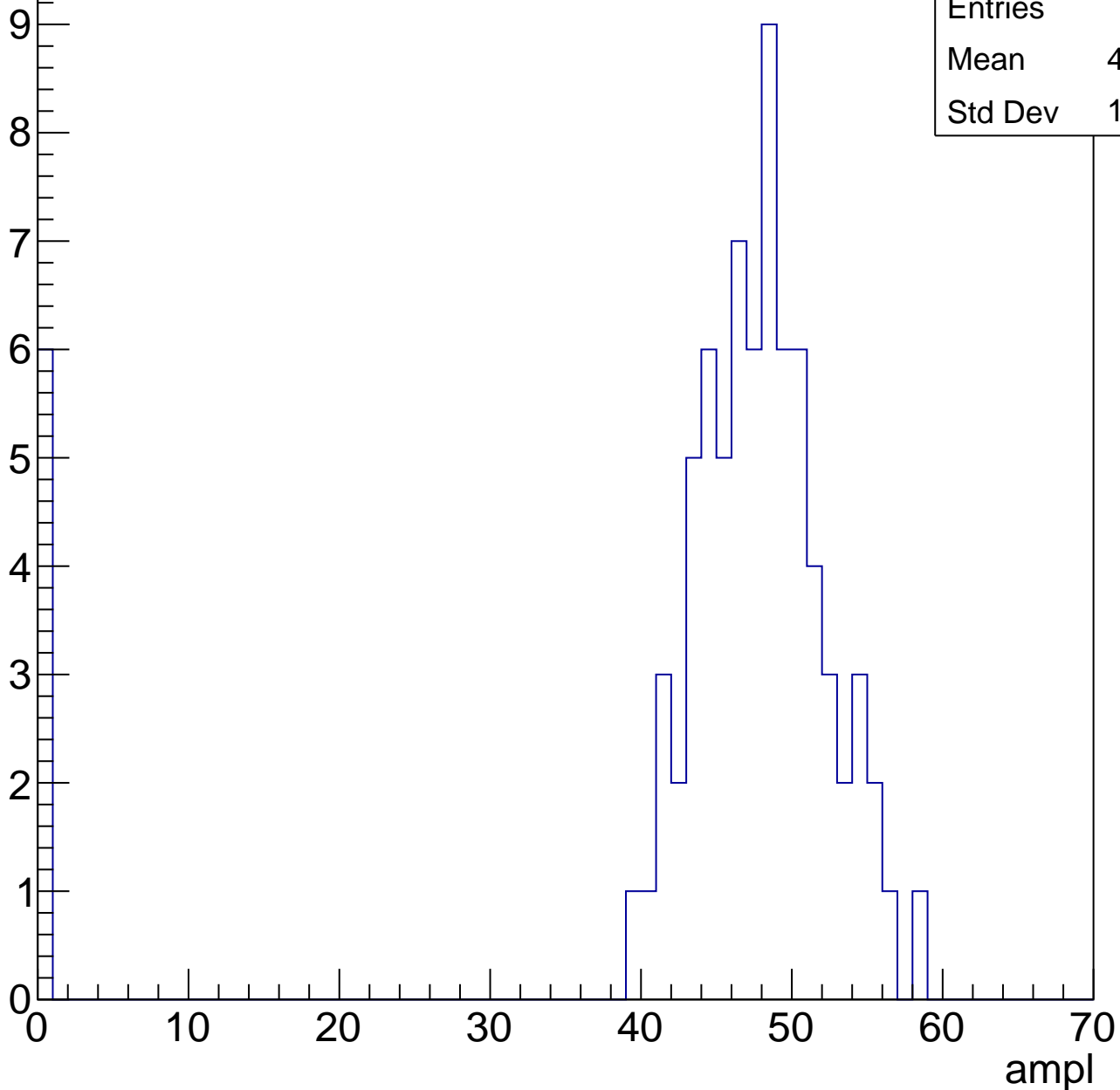


B1L103S, U5-ch102, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	79
Mean	43.95
Std Dev	13.18

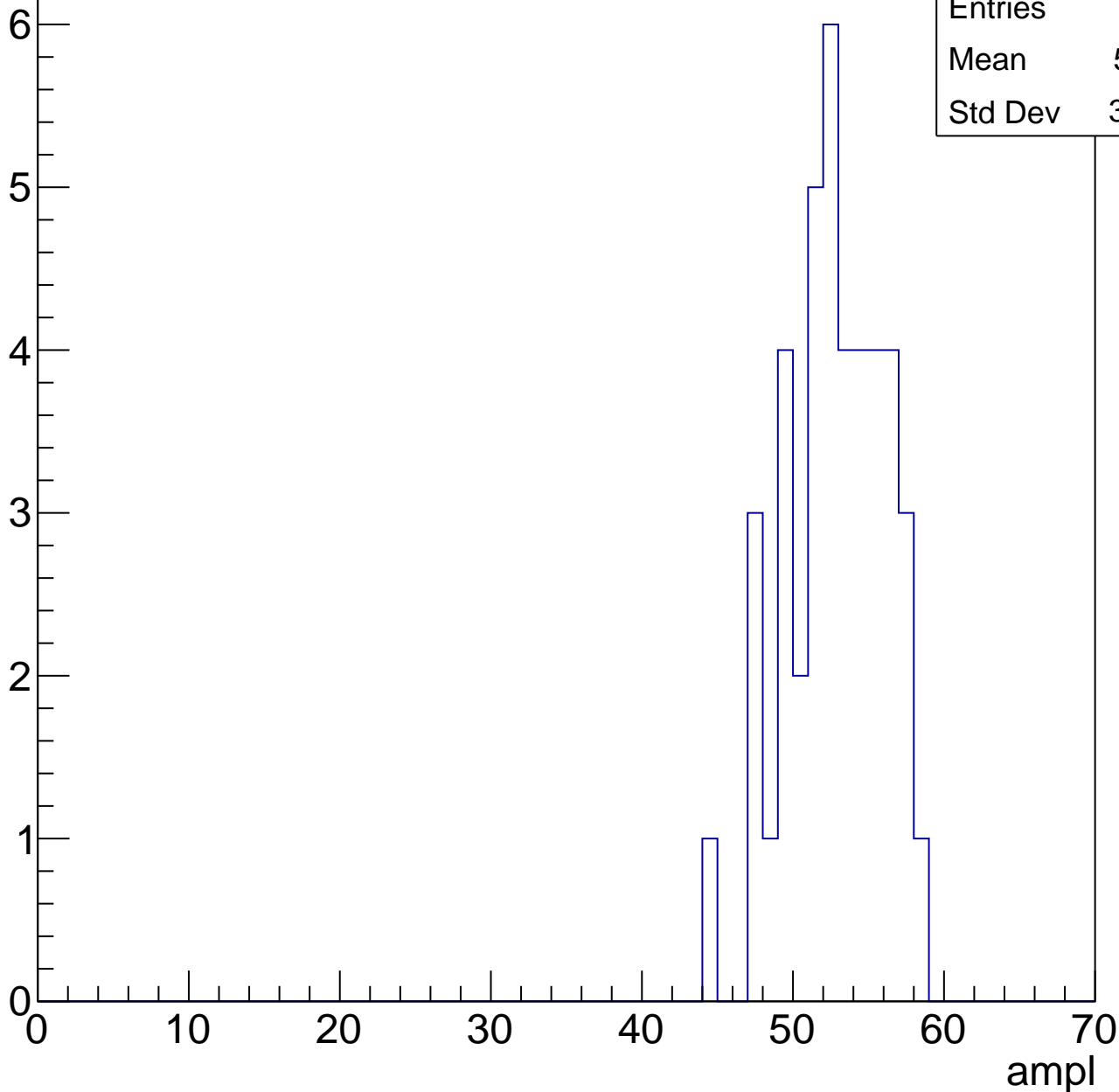


B1L103S, U5-ch102, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	42
Mean	52.31
Std Dev	3.203

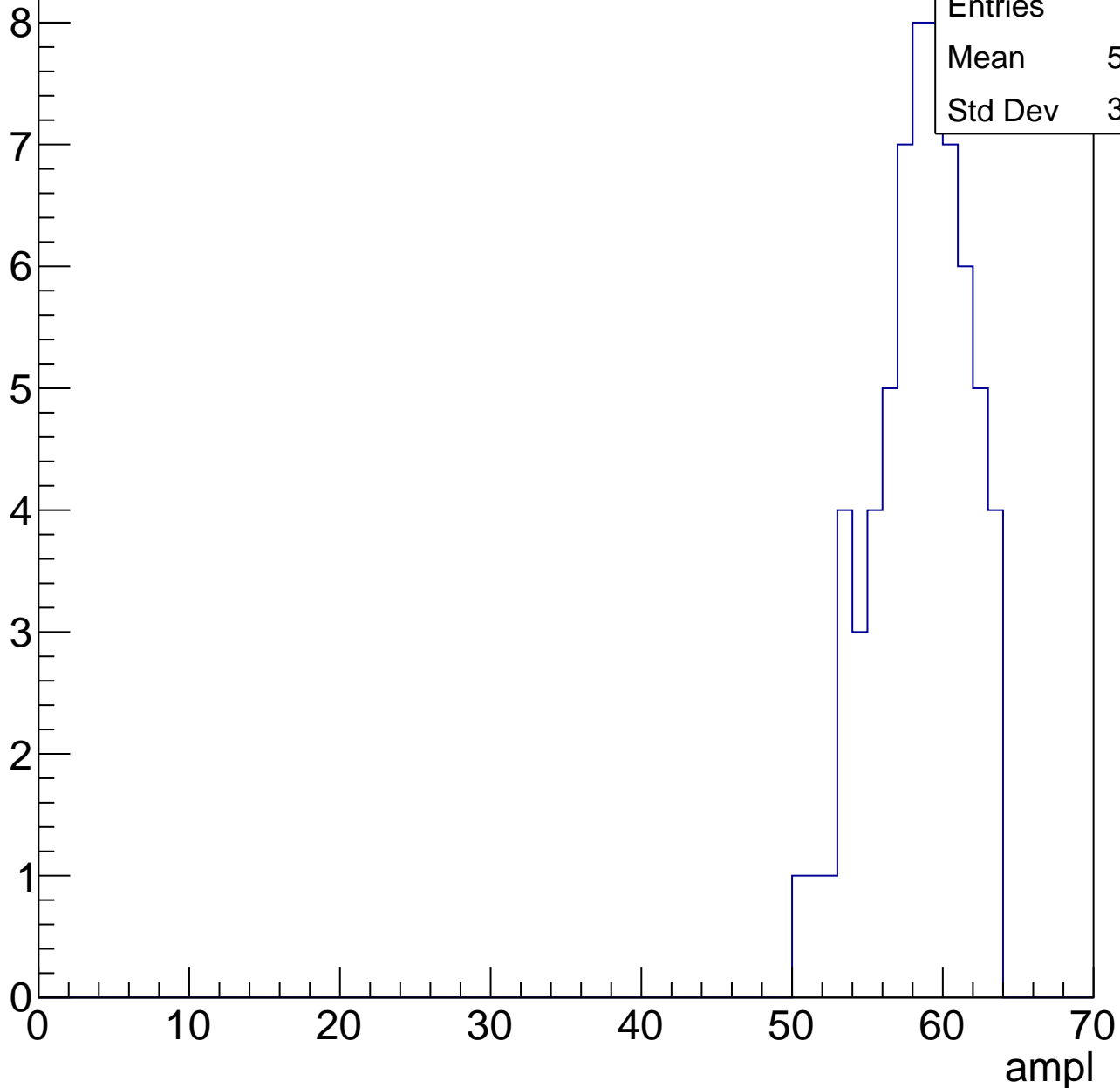


B1L103S, U5-ch102, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

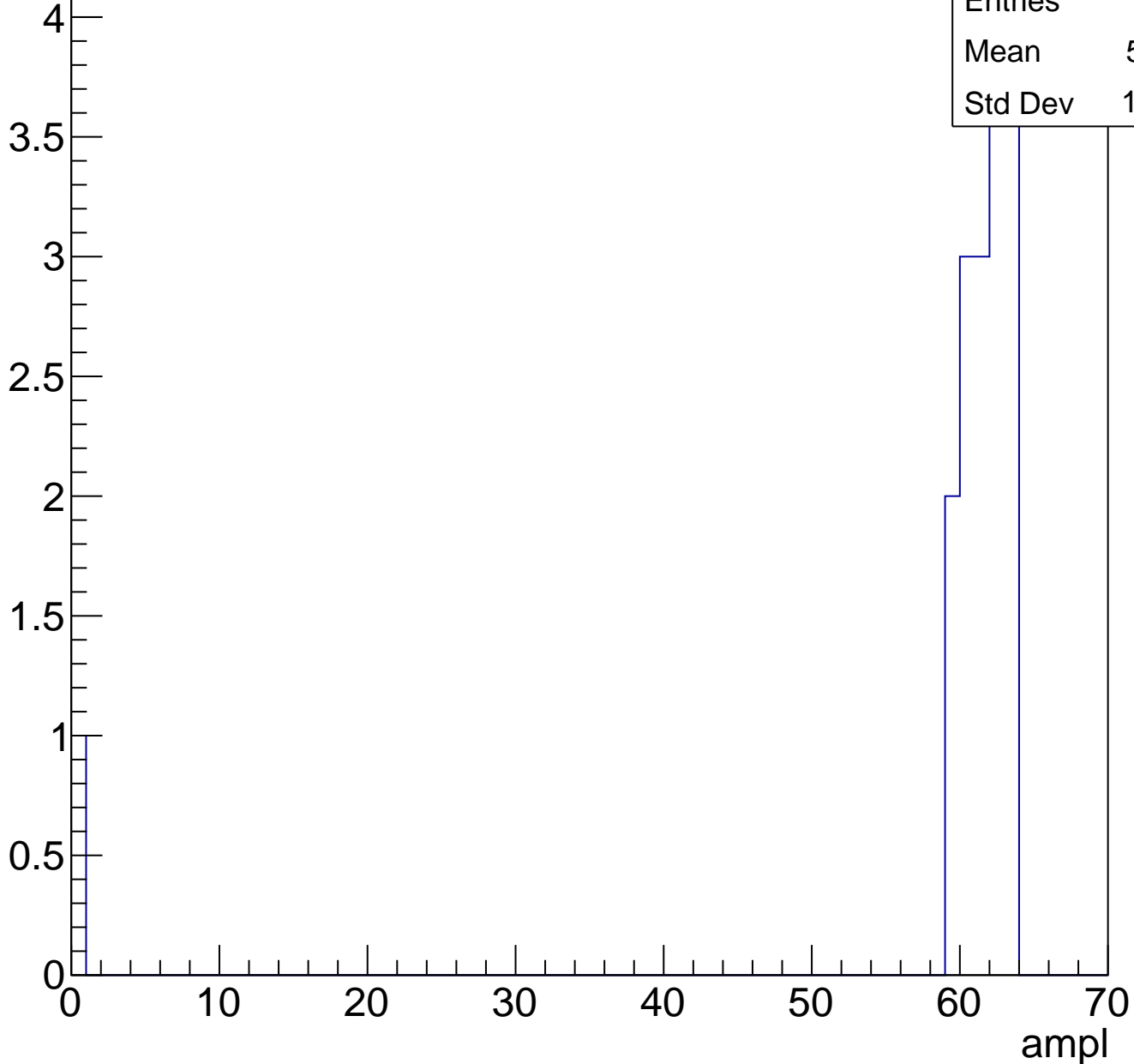
Entries	64
Mean	57.97
Std Dev	3.137



B1L103S, U5-ch102, adc6

calib_packv5_041523_1651.root, FC#0, port C2

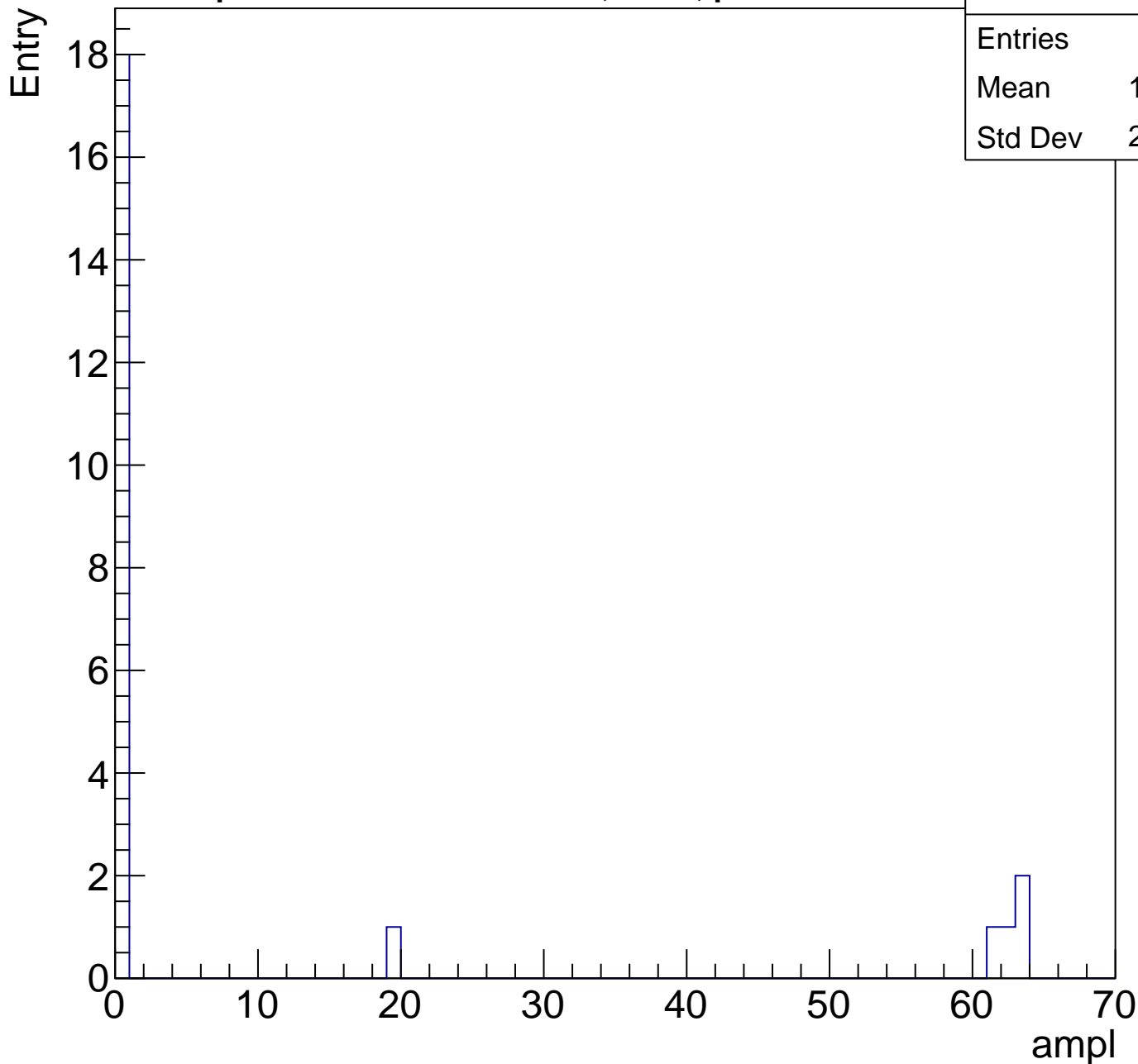
Entry



B1L103S, U5-ch102, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	23
Mean	11.65
Std Dev	23.54



B1L103S, U5-ch103, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	25.12
Std Dev	10.55

Entry

10

8

6

4

2

0

0

10

20

30

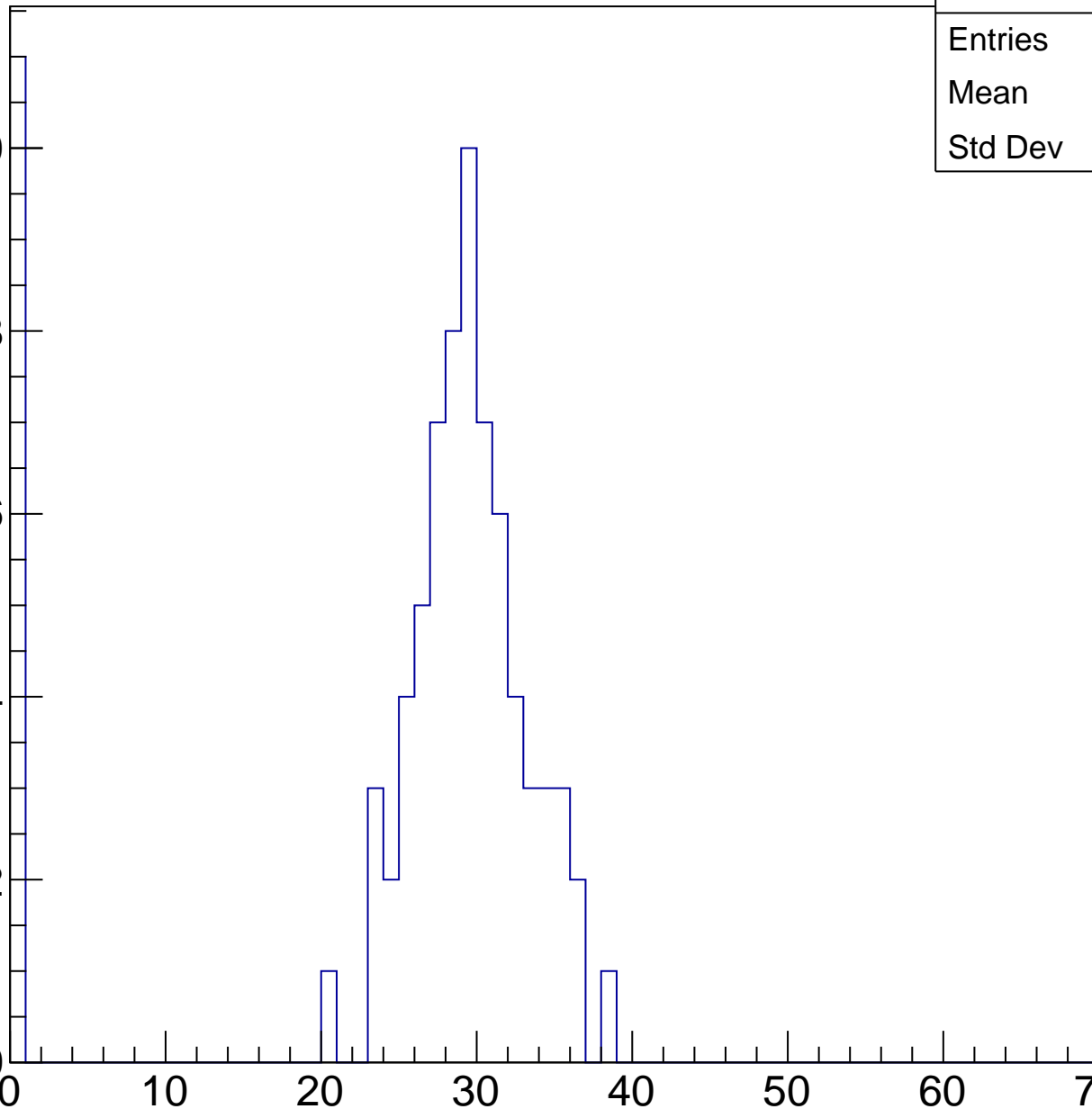
40

50

60

70

ampl

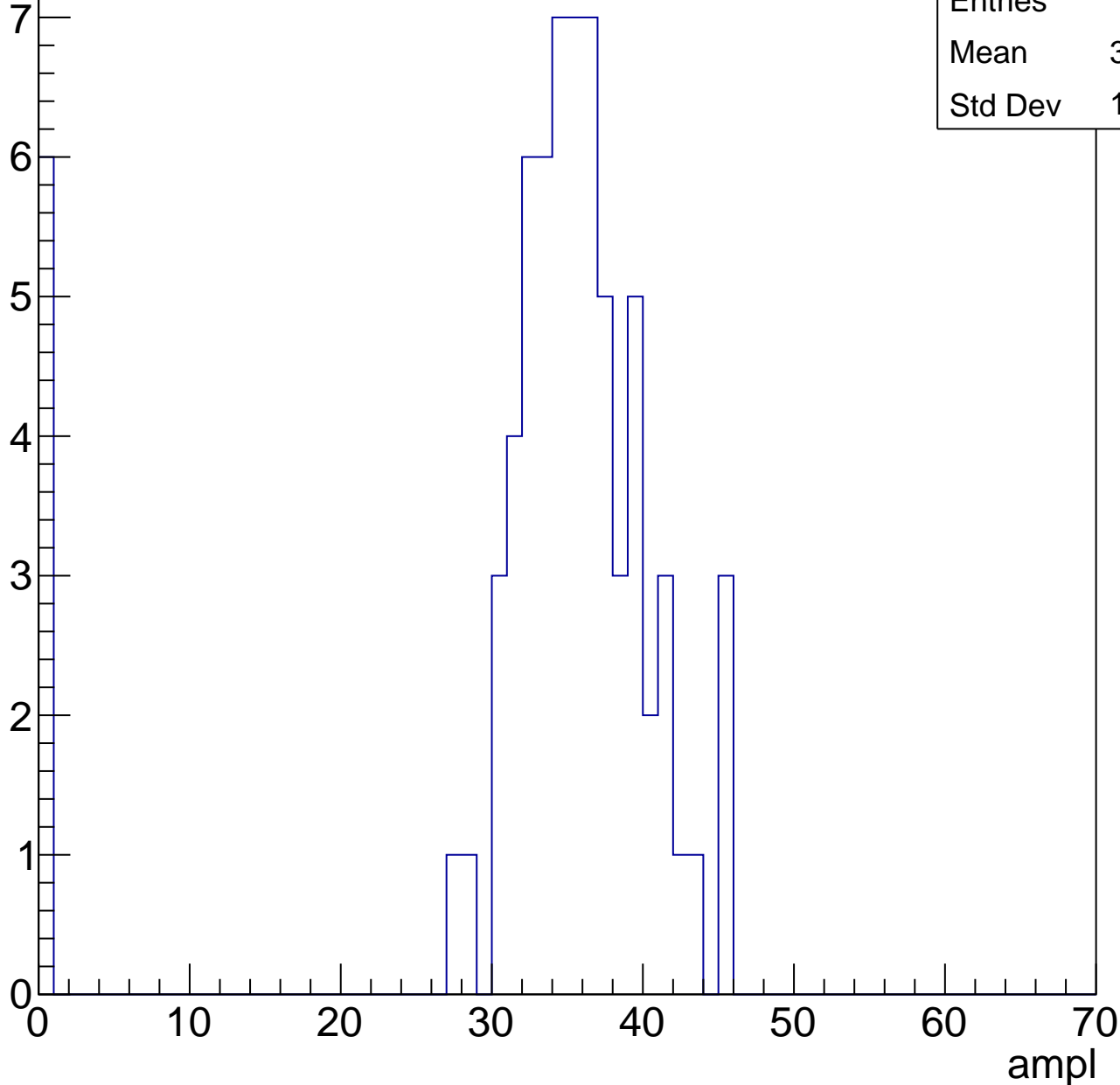


B1L103S, U5-ch103, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	32.55
Std Dev	10.59

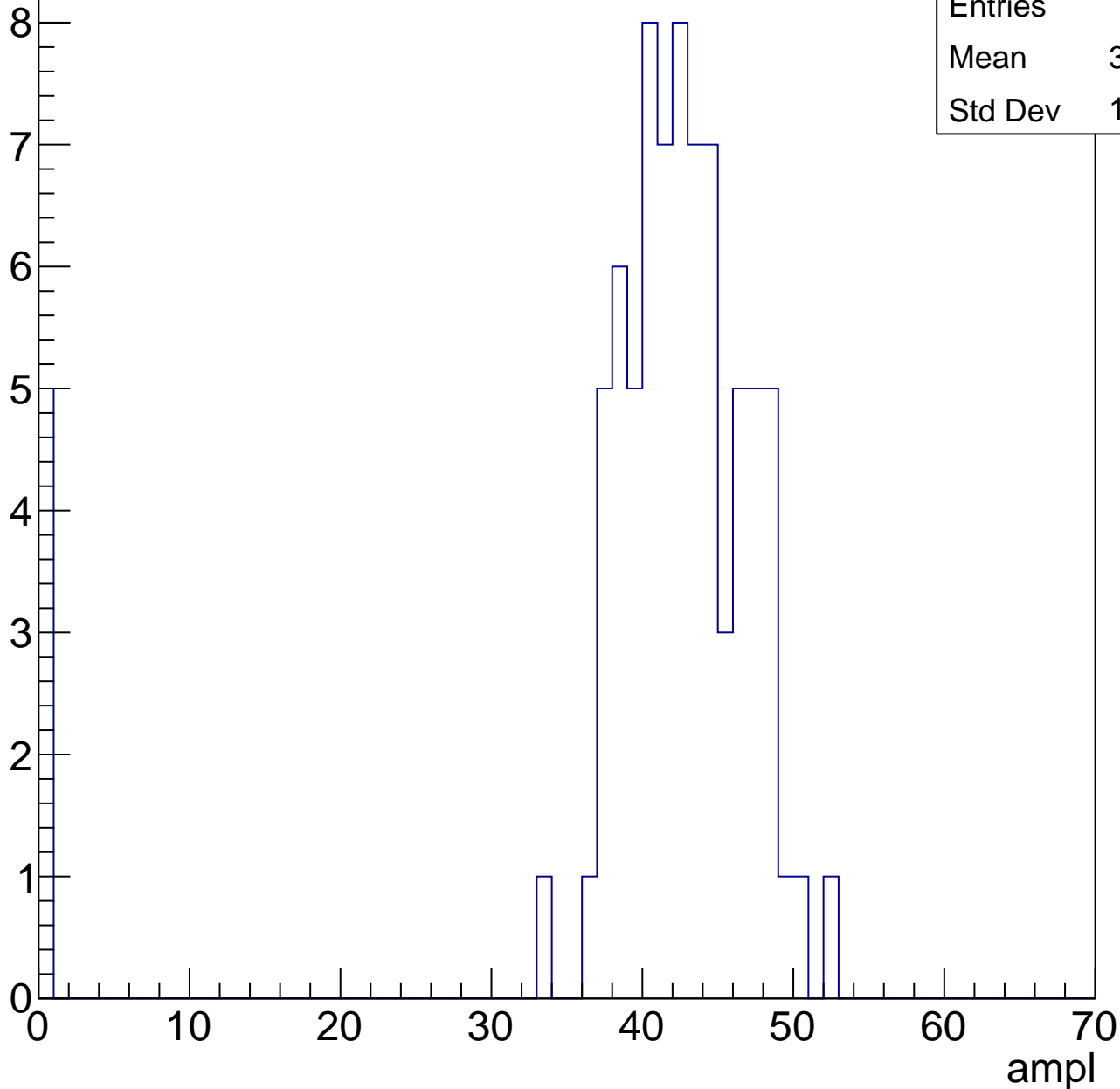


B1L103S, U5-ch103, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	81
Mean	39.75
Std Dev	10.83

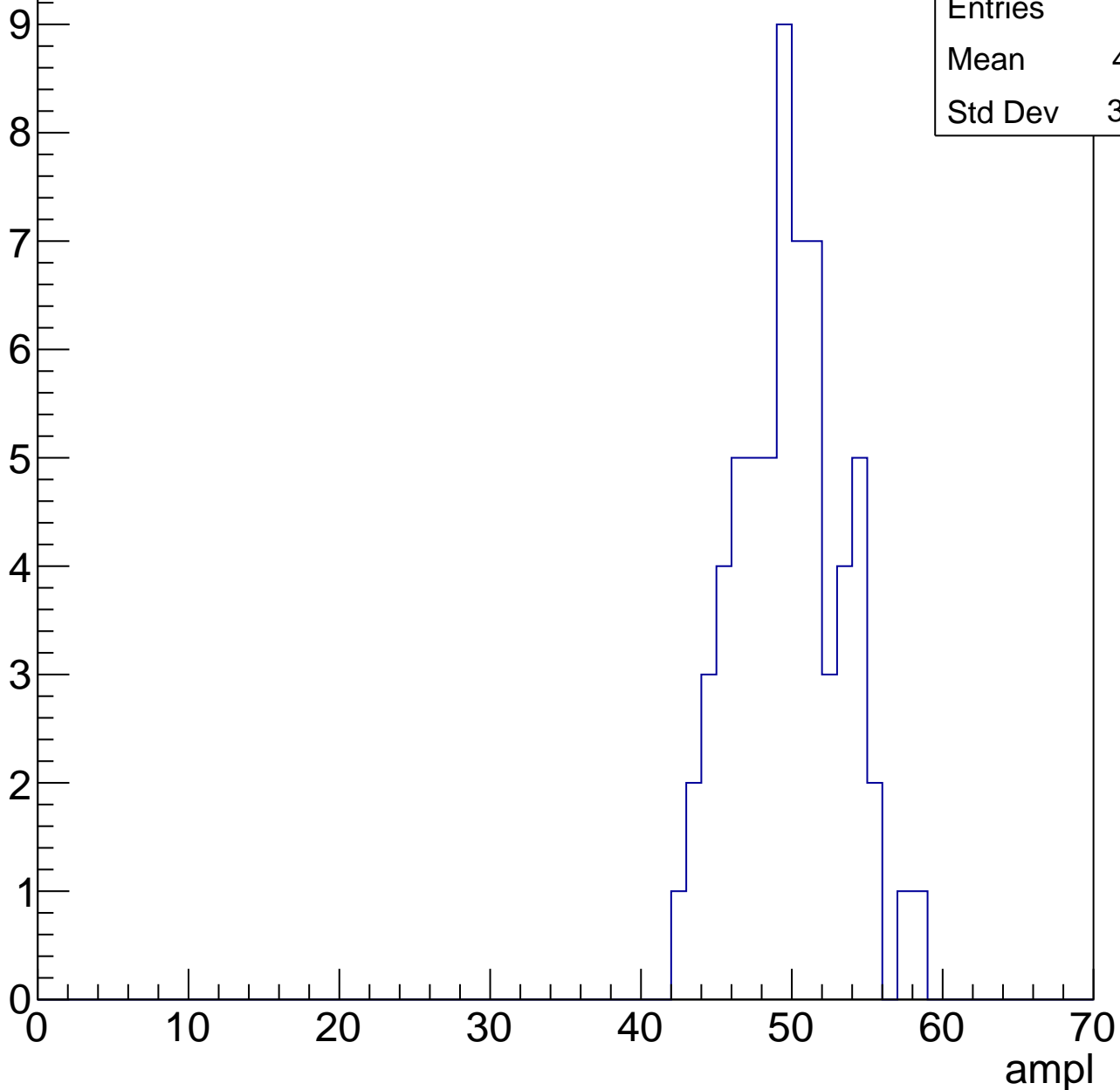


B1L103S, U5-ch103, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	49.31
Std Dev	3.517

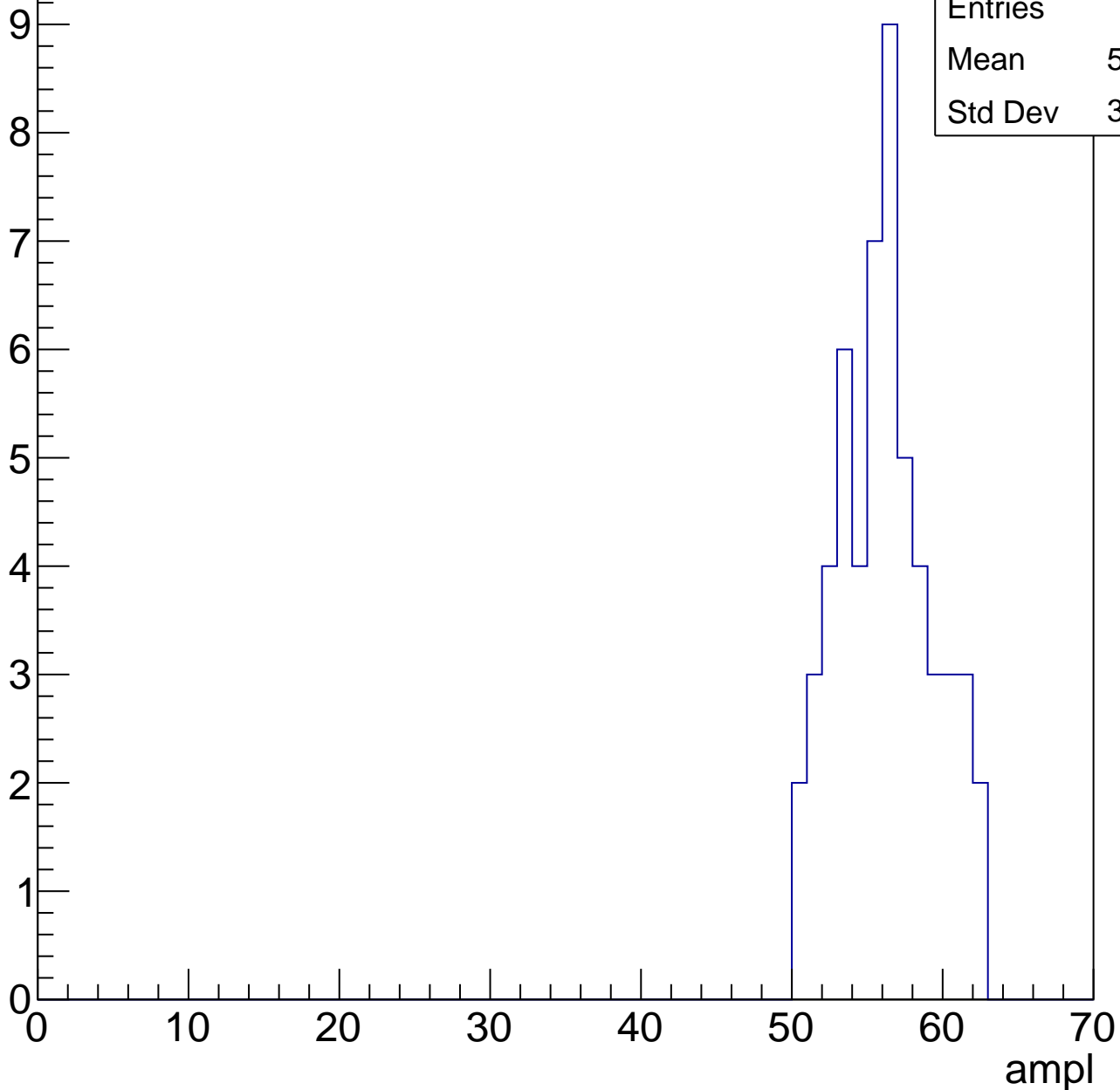


B1L103S, U5-ch103, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	55.73
Std Dev	3.095

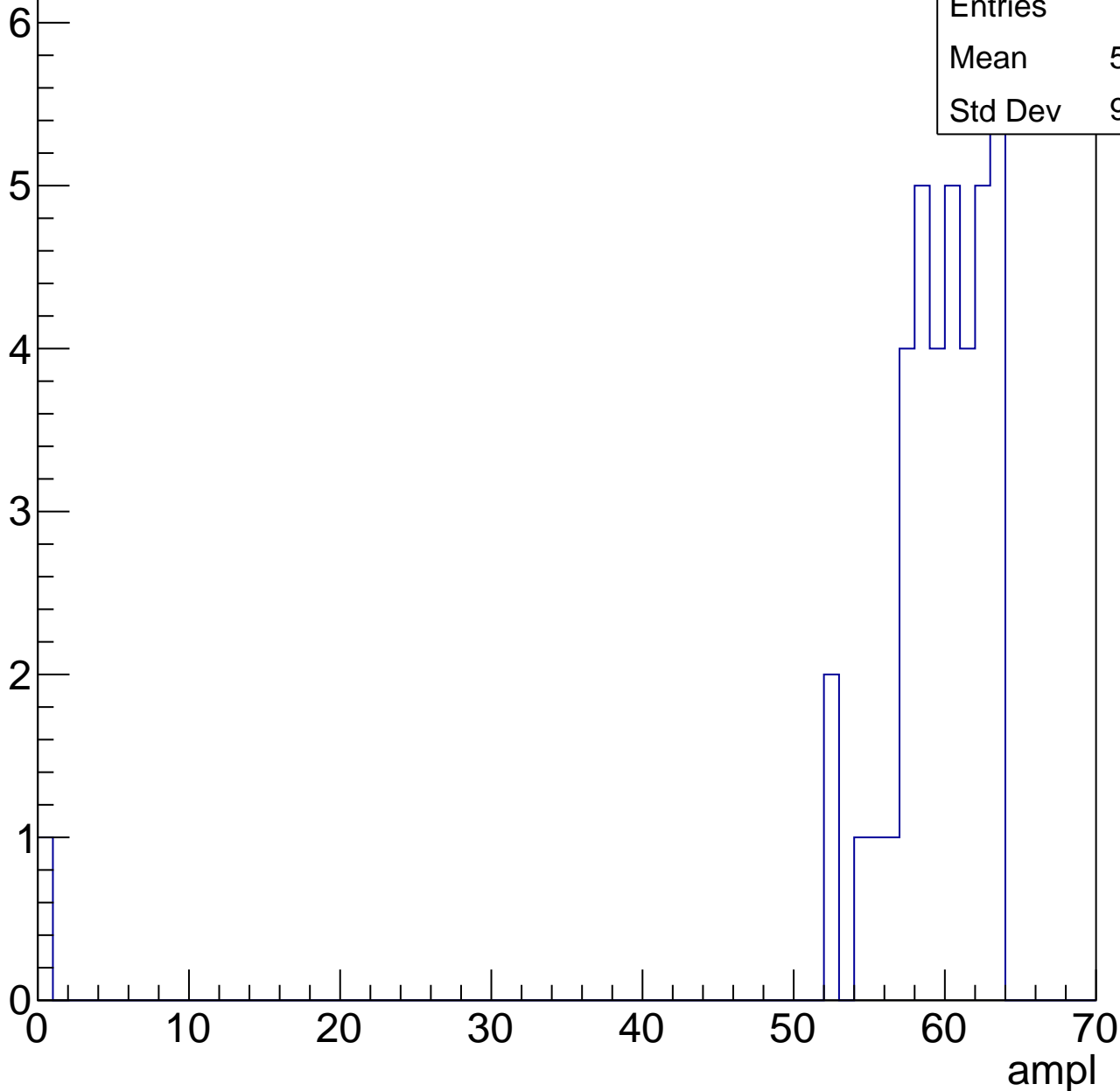


B1L103S, U5-ch103, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	57.82
Std Dev	9.816



B1L103S, U5-ch103, adc6

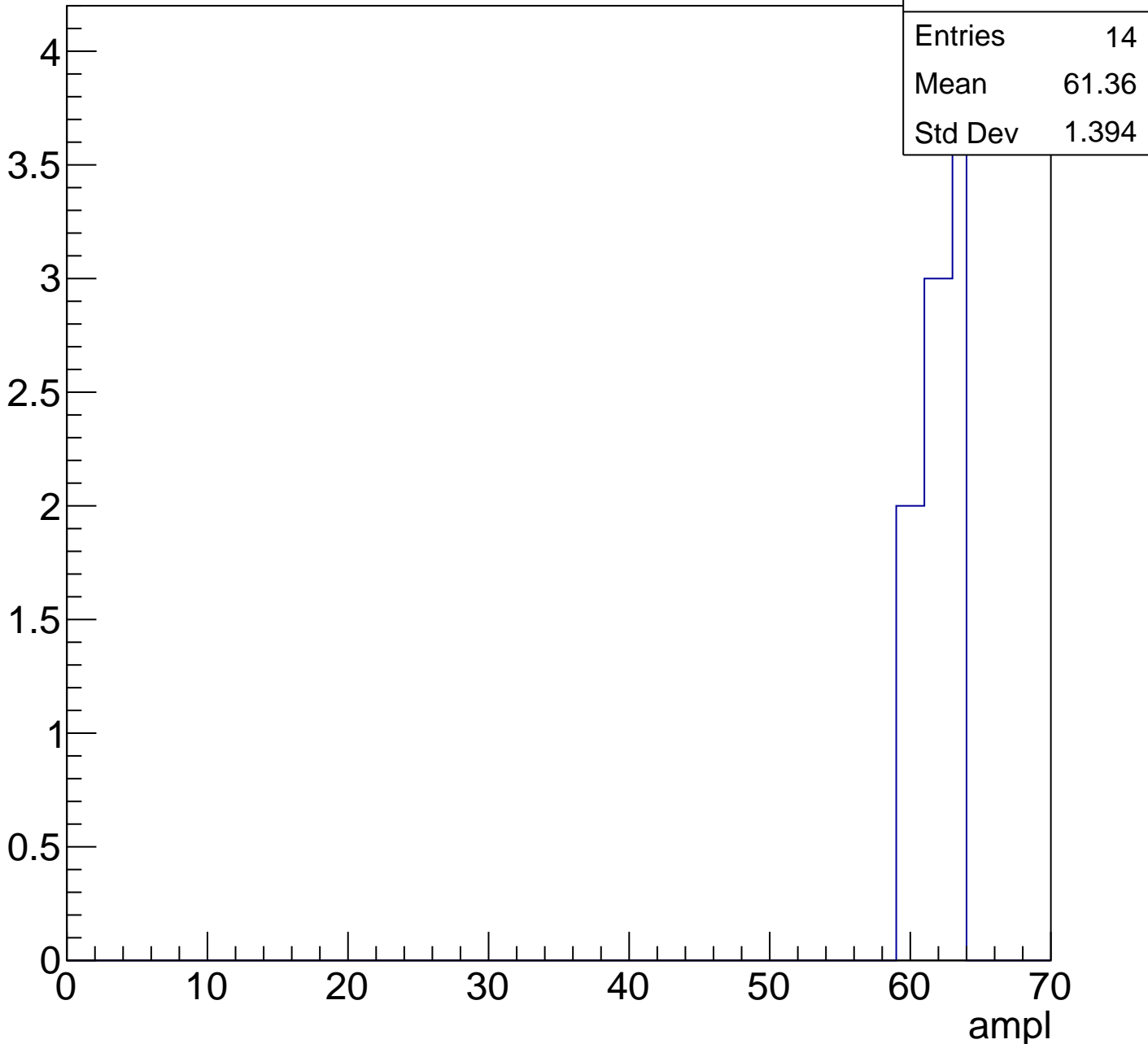
calib_packv5_041523_1651.root, FC#0, port C2

Entry

4
3.5
3
2.5
2
1.5
1
0.5
0

Entries	14
Mean	61.36
Std Dev	1.394

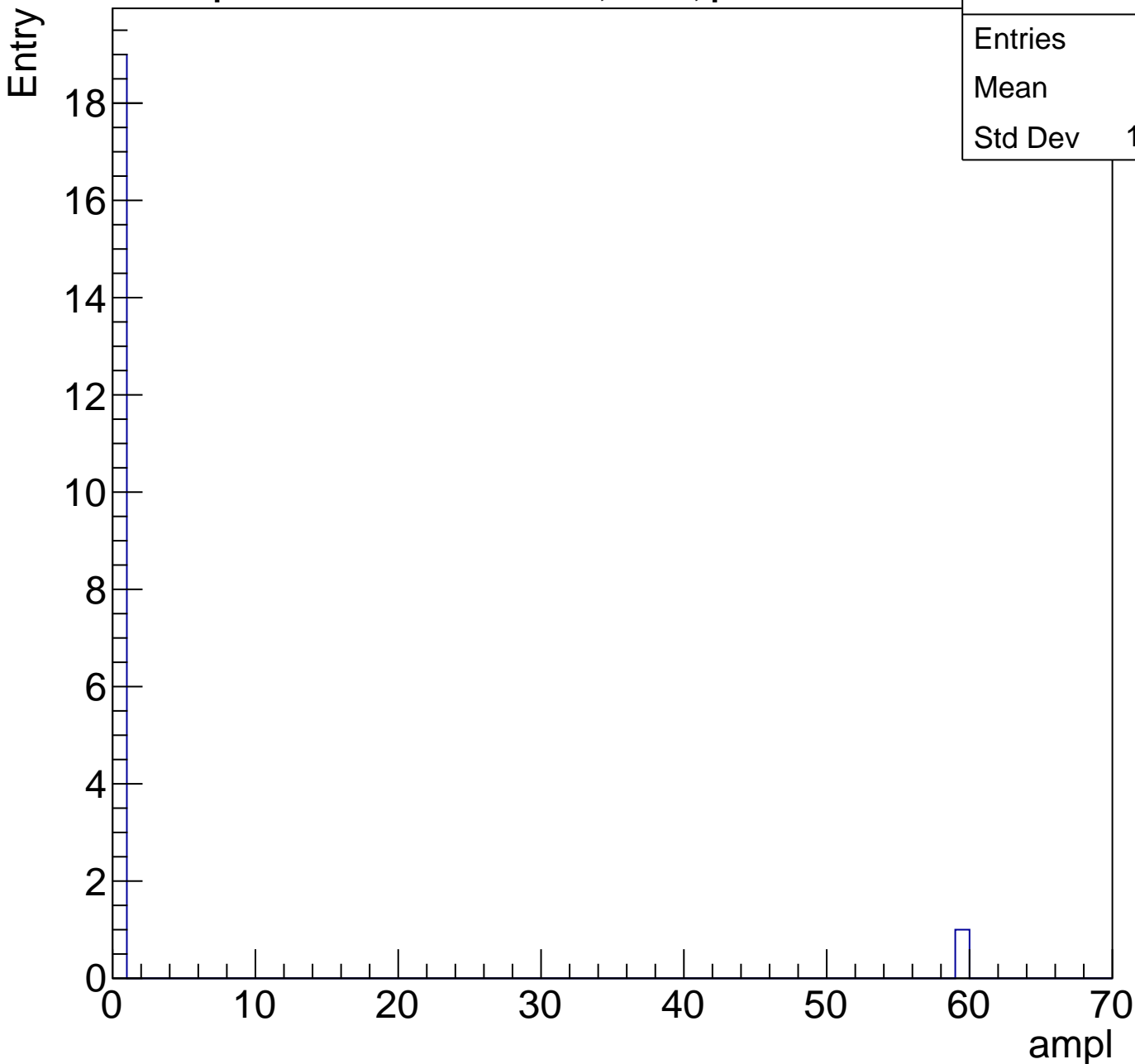
ampl



B1L103S, U5-ch103, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	2.95
Std Dev	12.86



B1L103S, U5-ch104, adc0

calib_packv5_041523_1651.root, FC#0, port C2

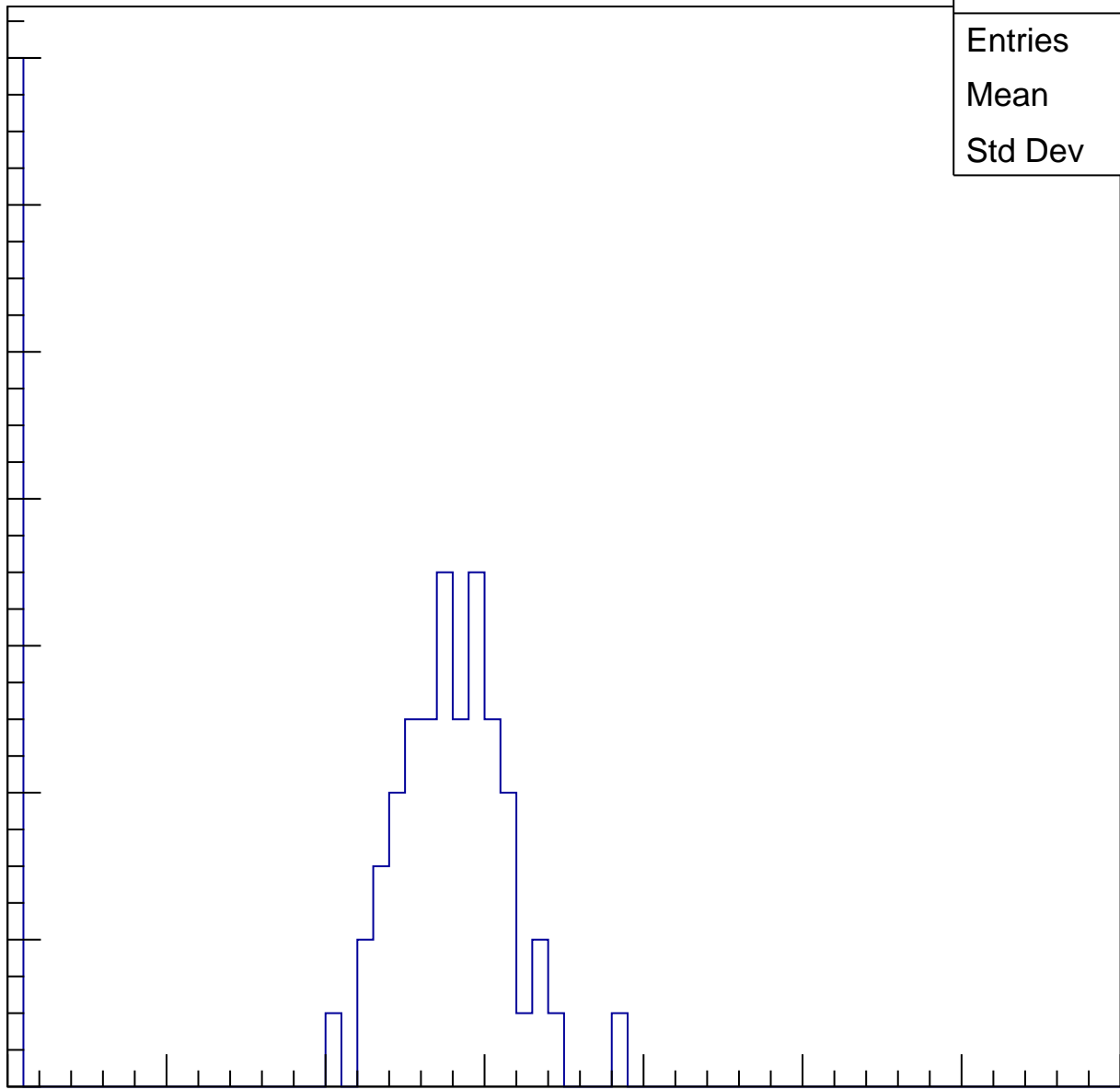
Entries	67
Mean	21.79
Std Dev	11.59

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

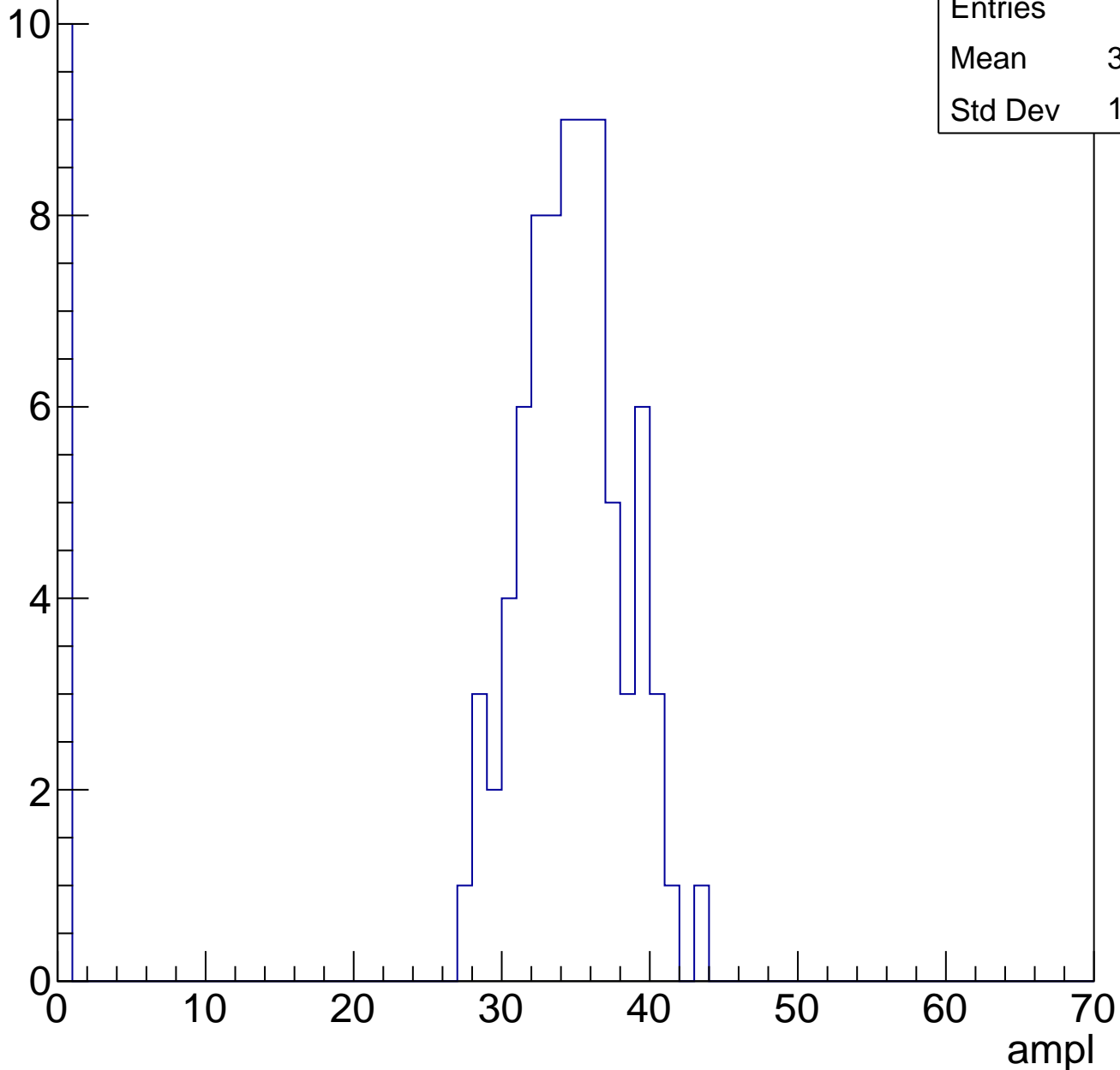


B1L103S, U5-ch104, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	88
Mean	30.42
Std Dev	11.34

Entry

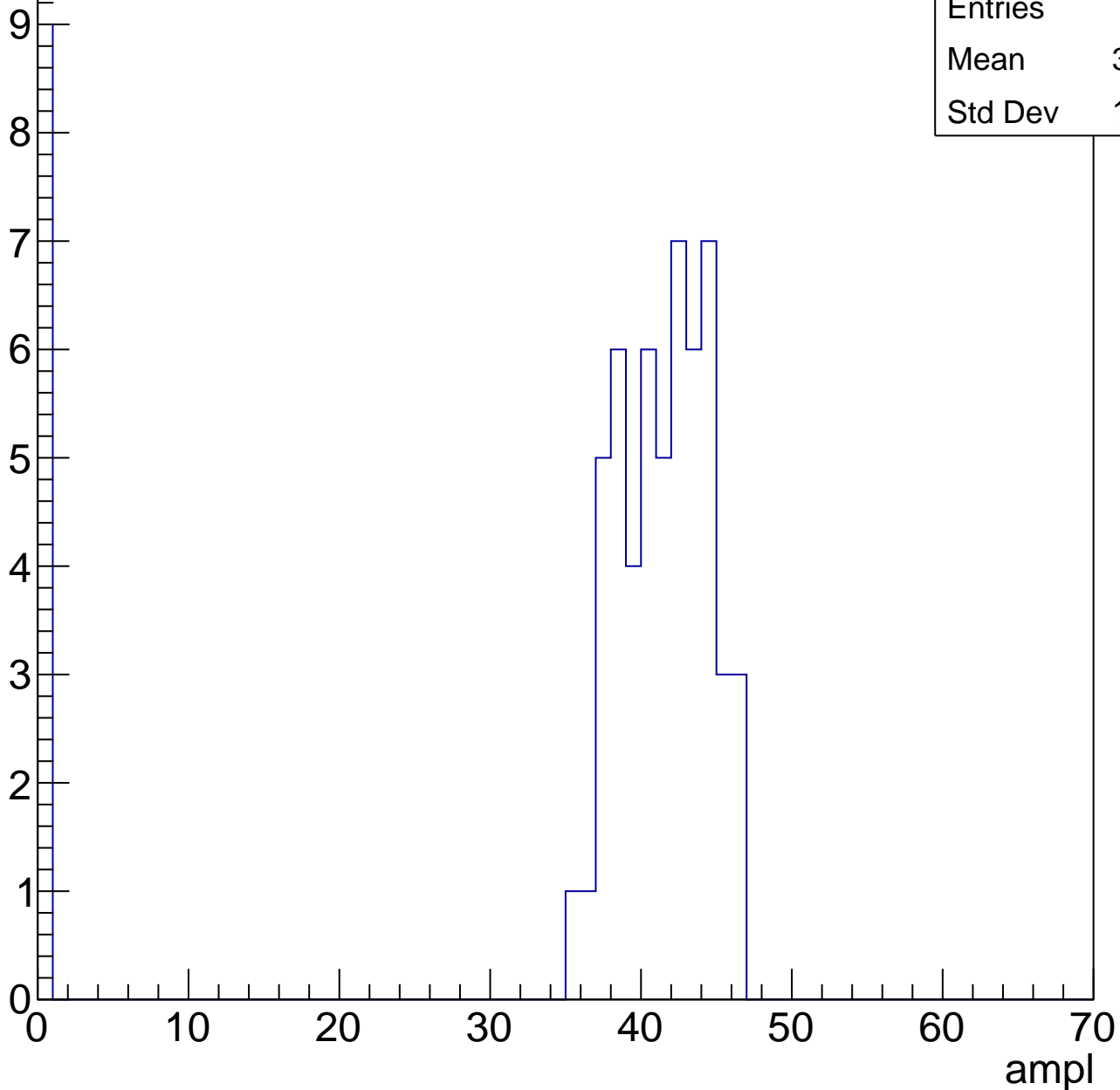


B1L103S, U5-ch104, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	35.21
Std Dev	14.61

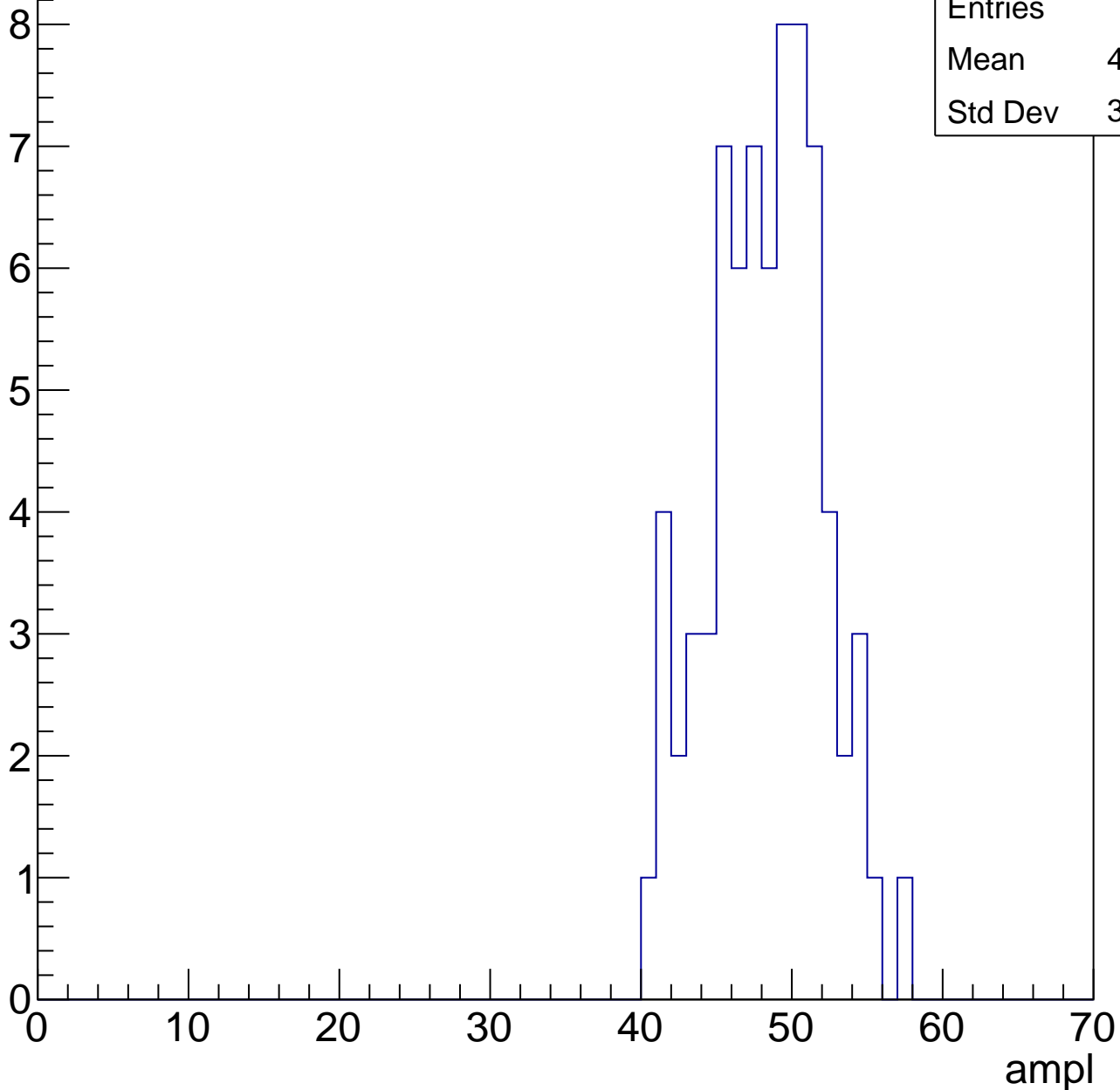


B1L103S, U5-ch104, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	47.86
Std Dev	3.706

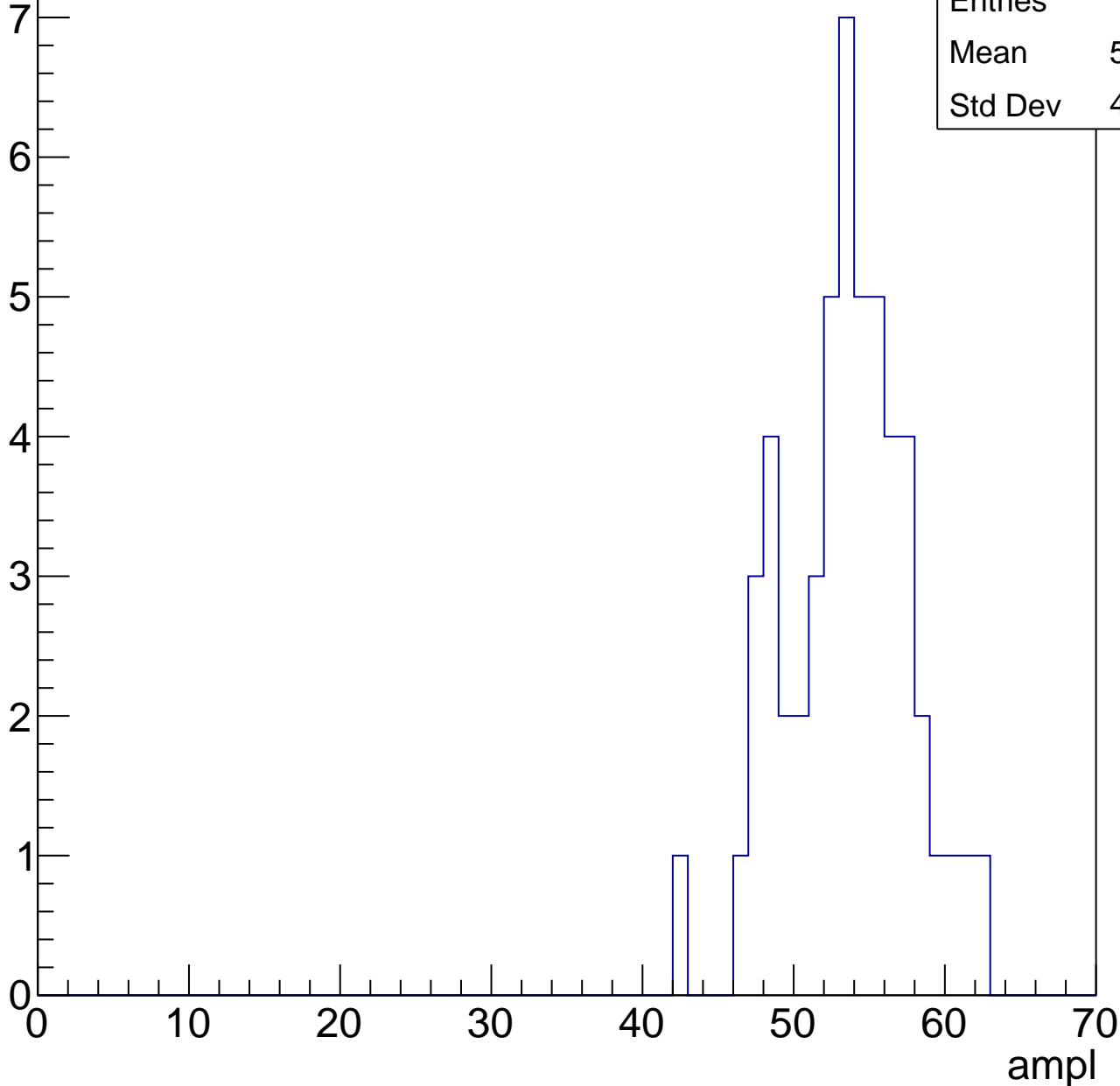


B1L103S, U5-ch104, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

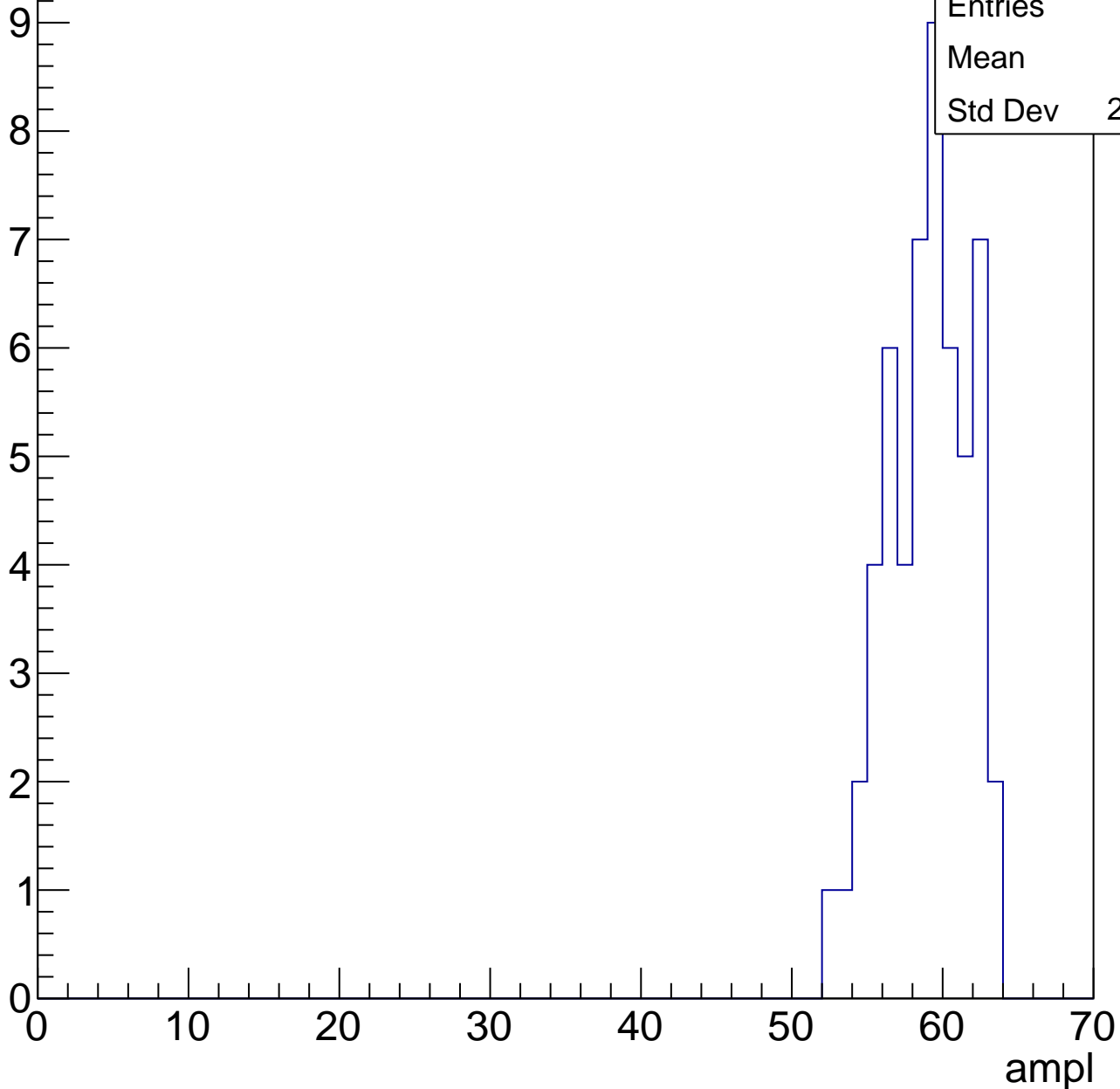
Entries	52
Mean	53.04
Std Dev	4.043



B1L103S, U5-ch104, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

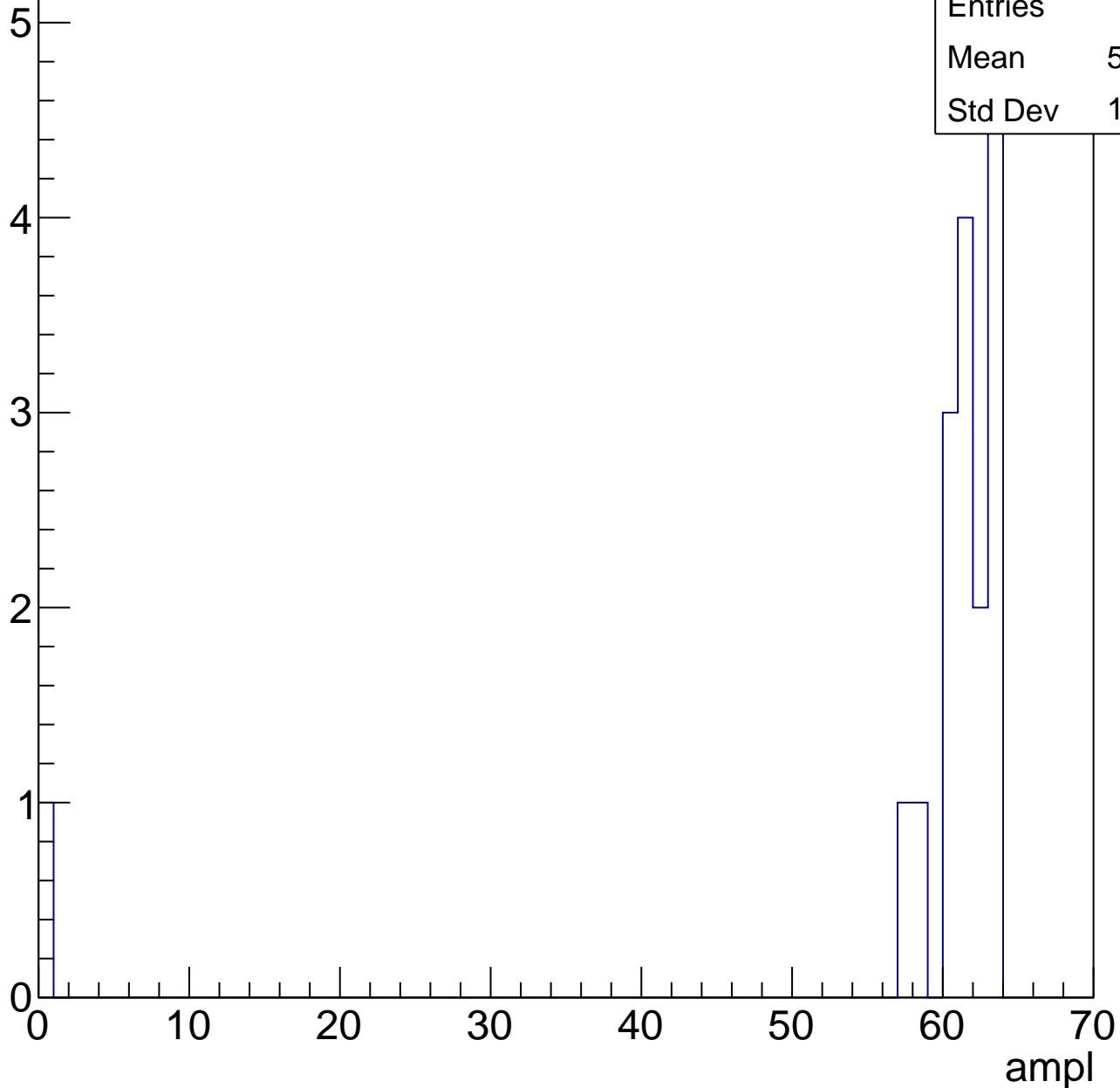


B1L103S, U5-ch104, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	17
Mean	57.53
Std Dev	14.48

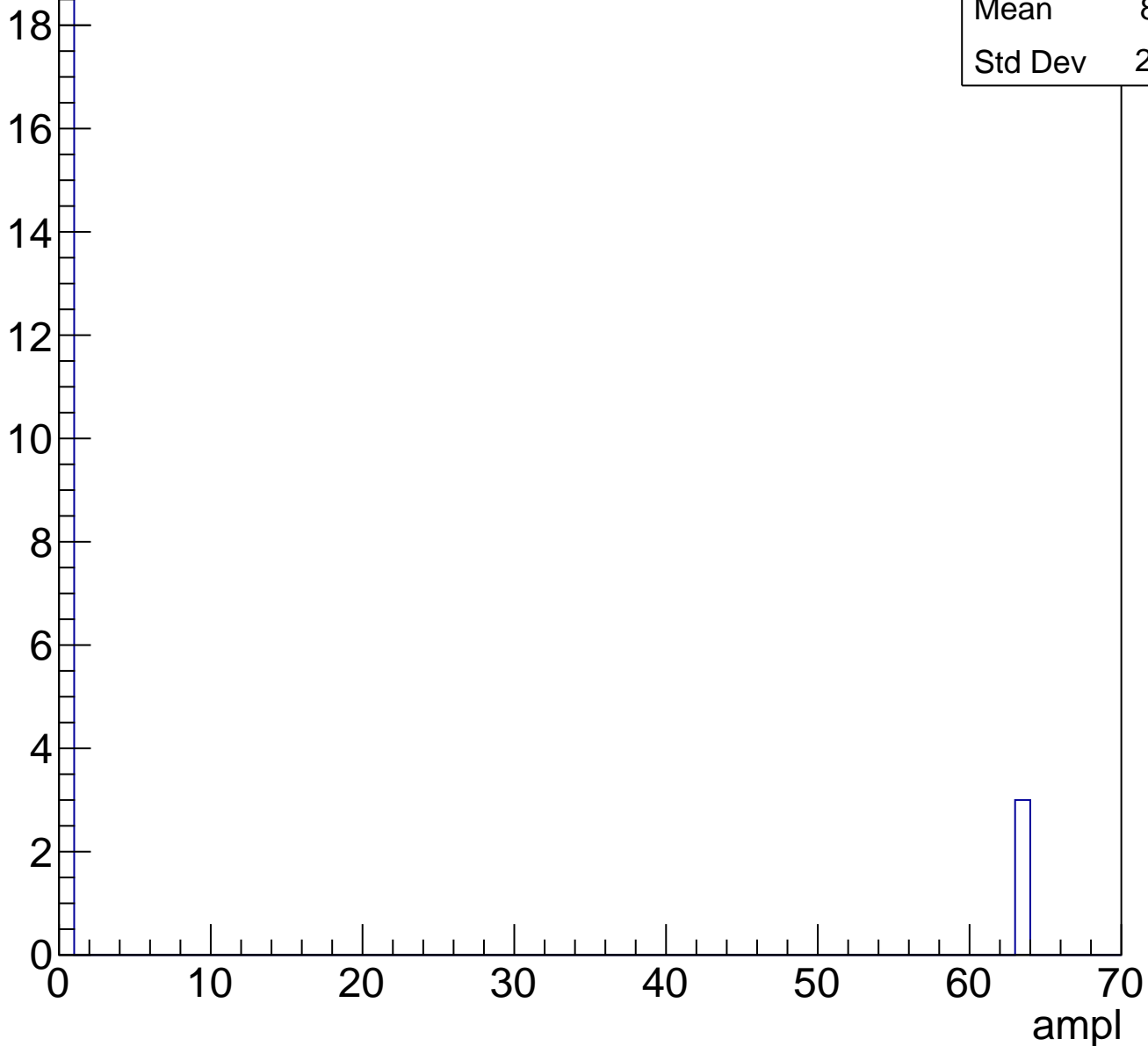


B1L103S, U5-ch104, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	22
Mean	8.591
Std Dev	21.62

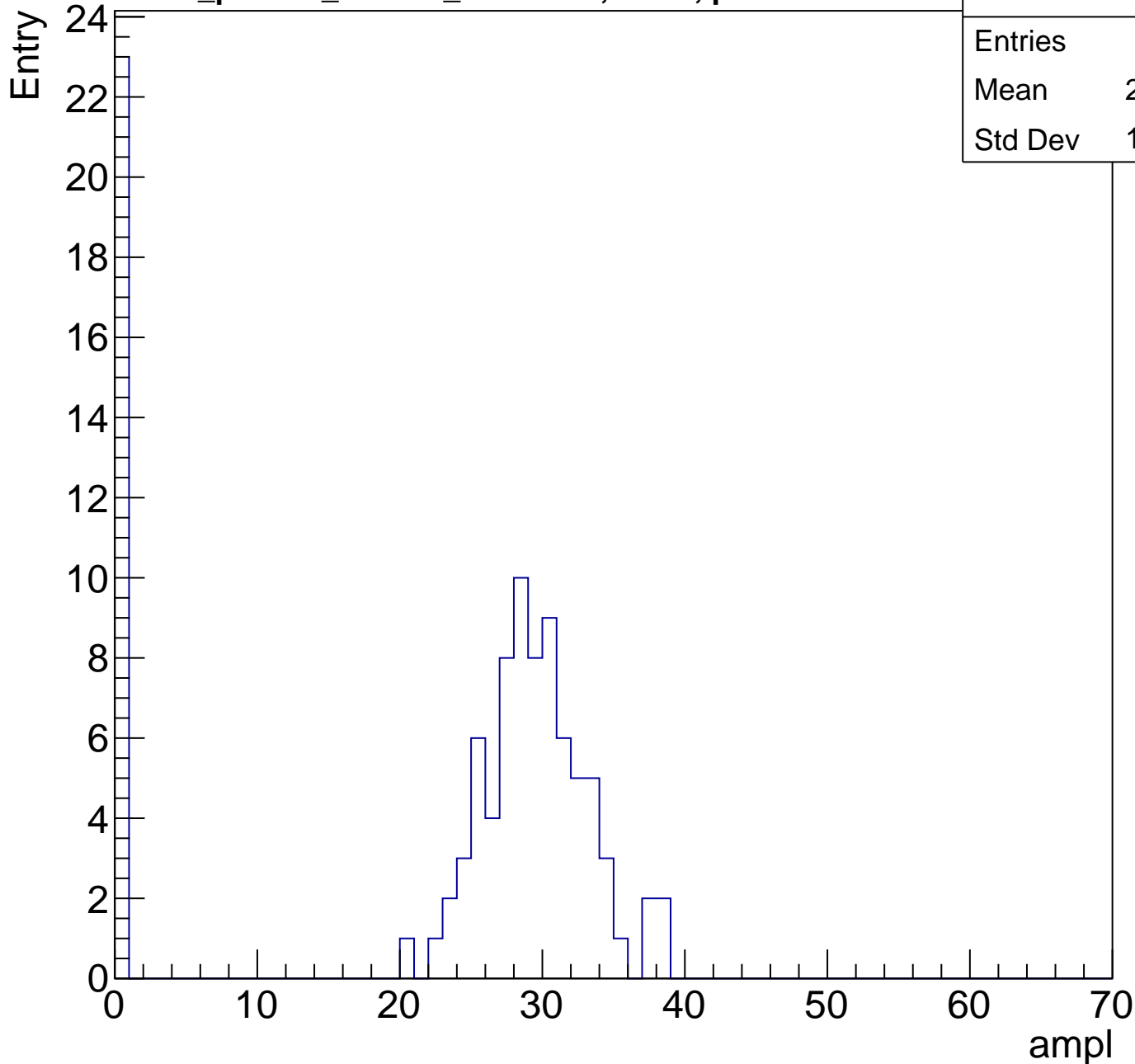
Entry



B1L103S, U5-ch105, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	99
Mean	22.32
Std Dev	12.69

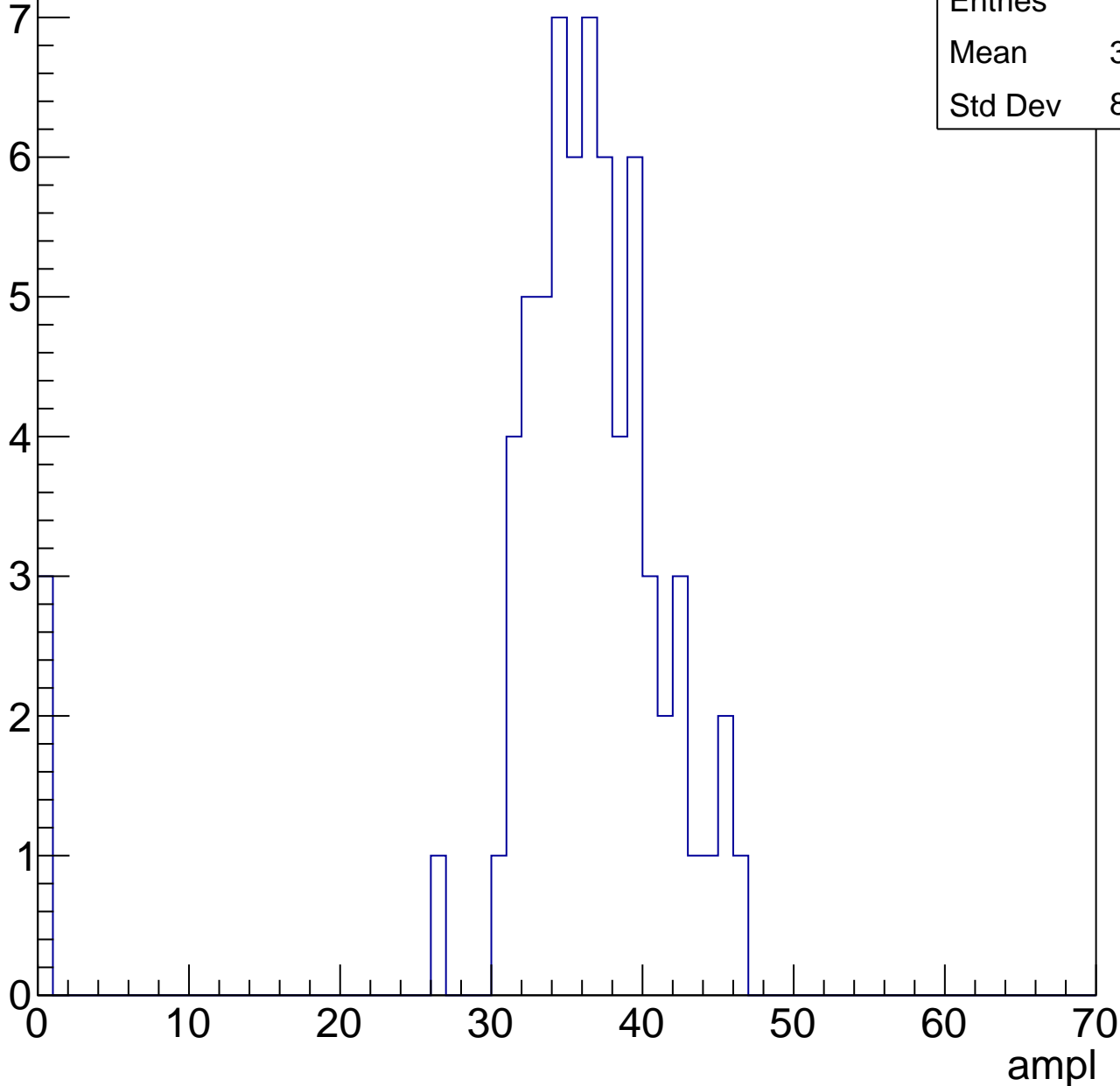


B1L103S, U5-ch105, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	34.76
Std Dev	8.433



B1L103S, U5-ch105, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	78
Mean	34.79
Std Dev	15.88

Entry

12

10

8

6

4

2

0

0

10

20

30

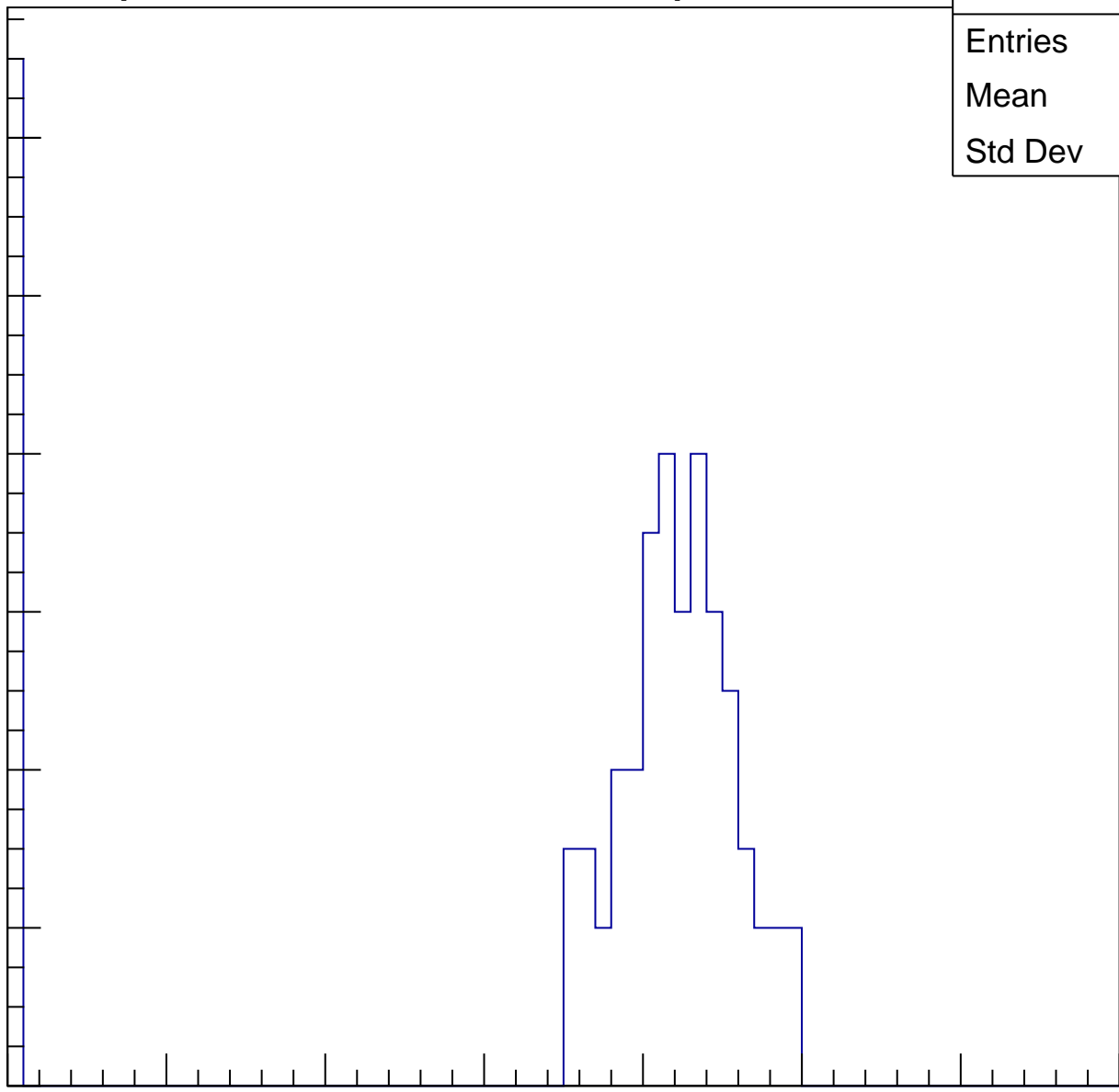
40

50

60

70

ampl

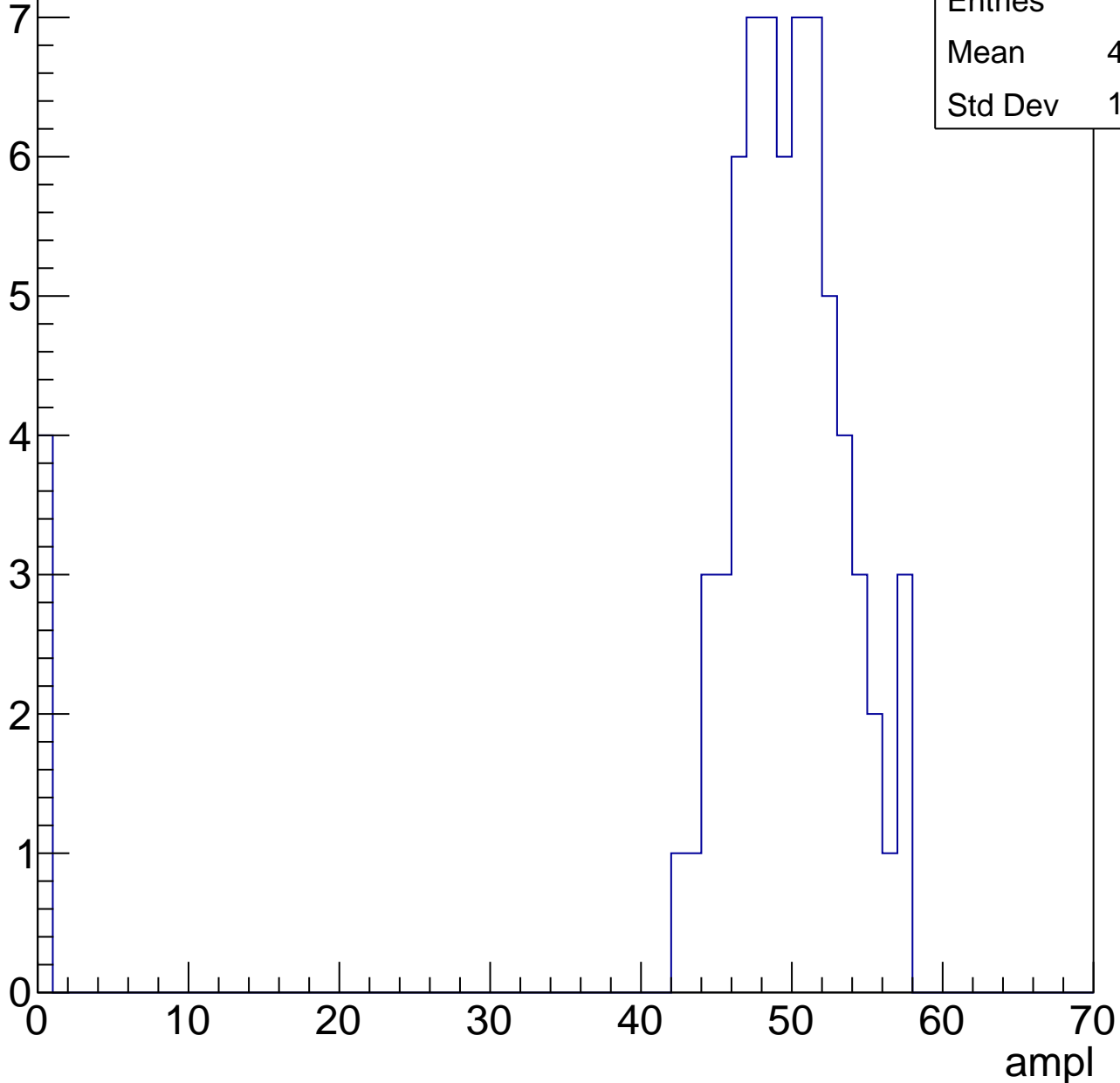


B1L103S, U5-ch105, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	46.64
Std Dev	11.98

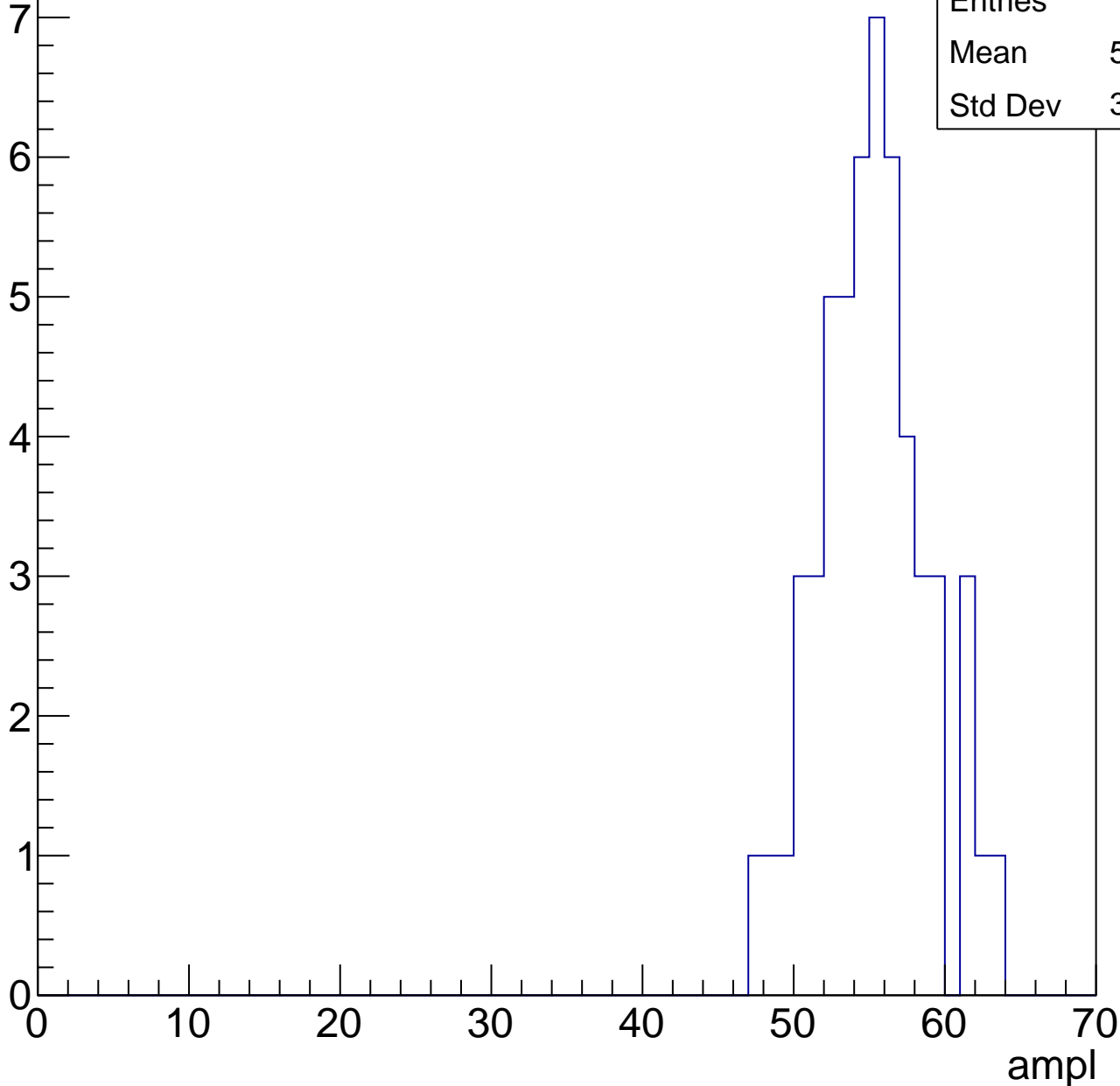


B1L103S, U5-ch105, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

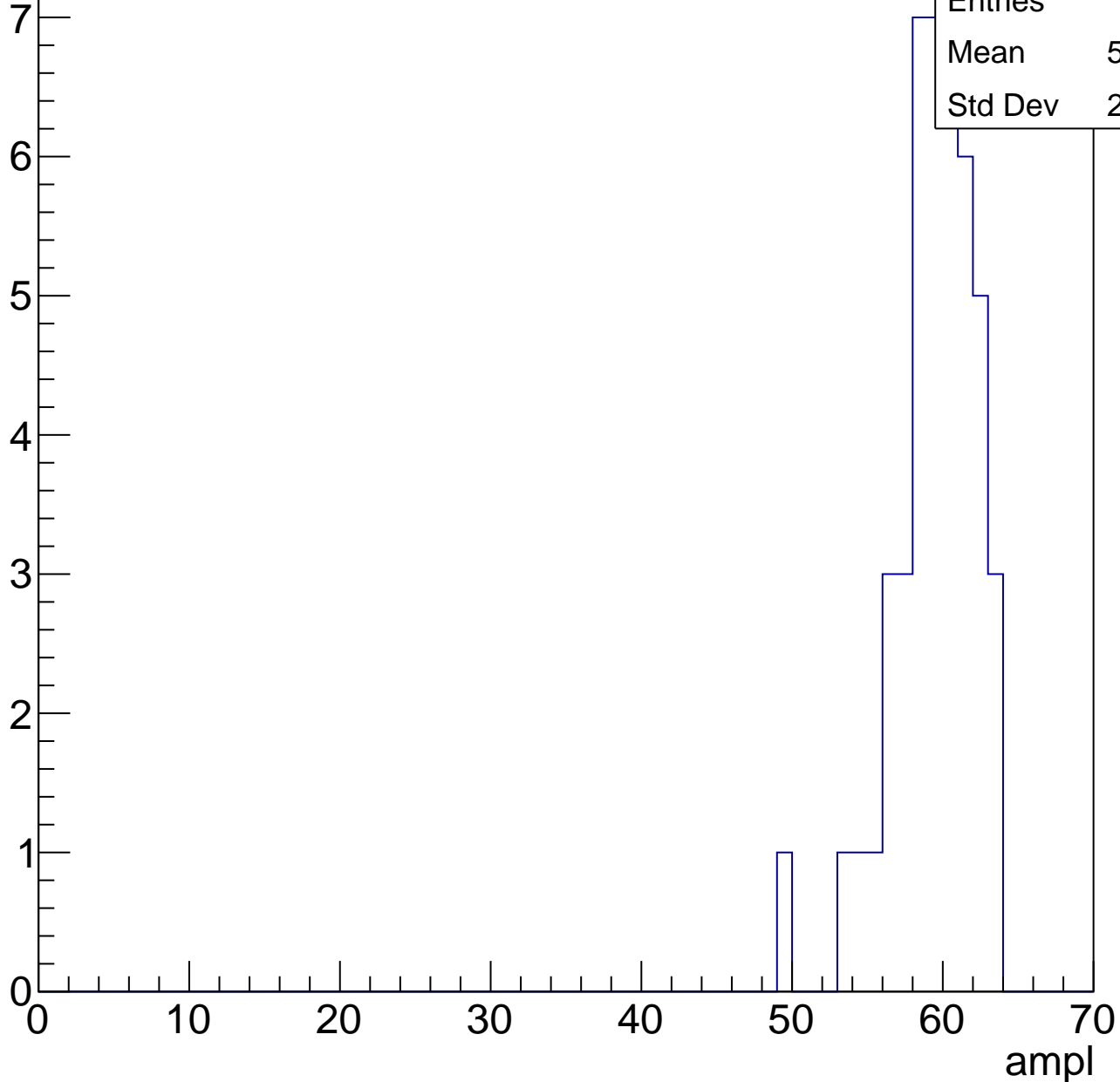
Entries	53
Mean	54.79
Std Dev	3.525



B1L103S, U5-ch105, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

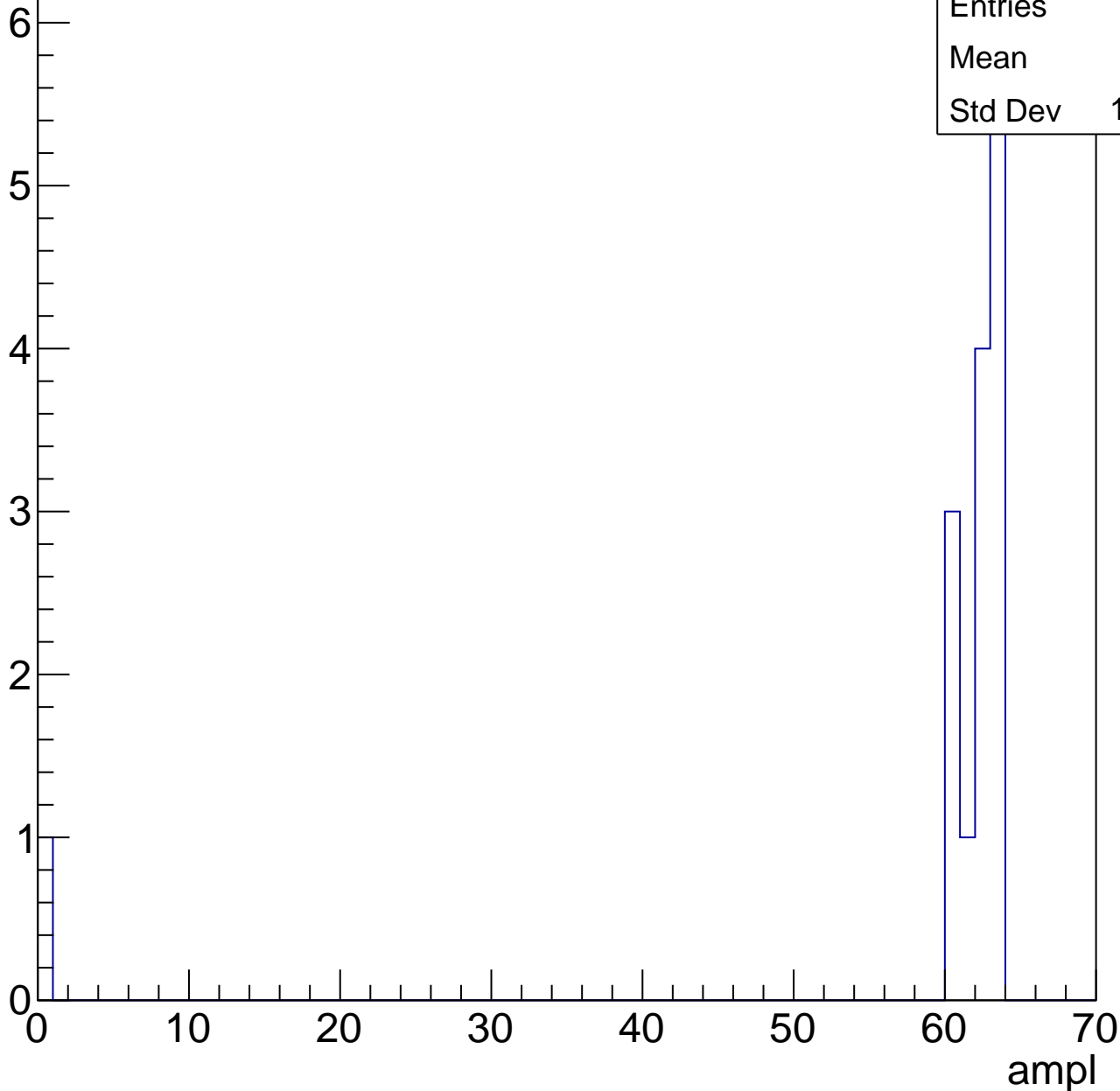


B1L103S, U5-ch105, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	15
Mean	57.8
Std Dev	15.49



B1L103S, U5-ch105, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

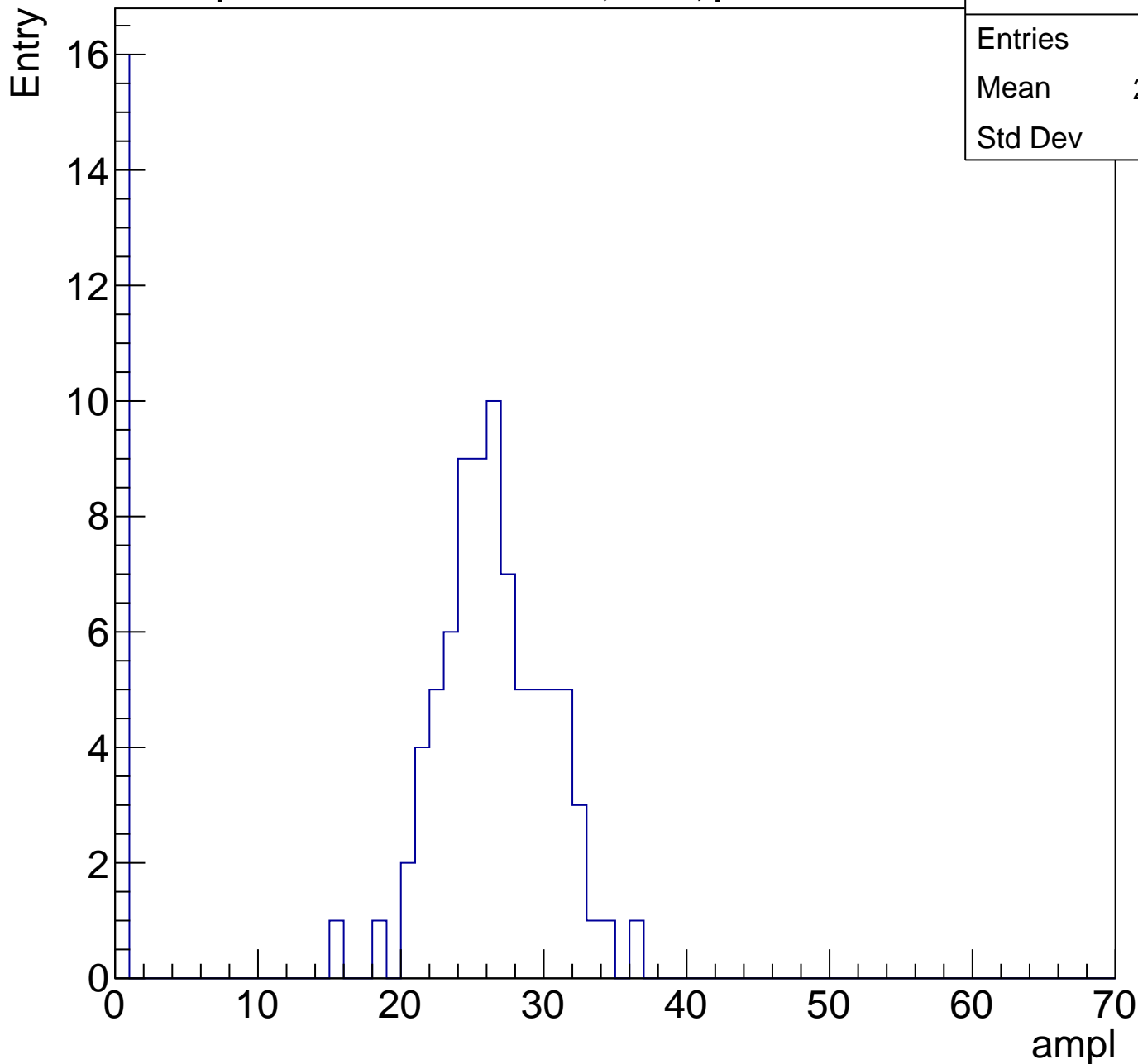
ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U5-ch106, adc0

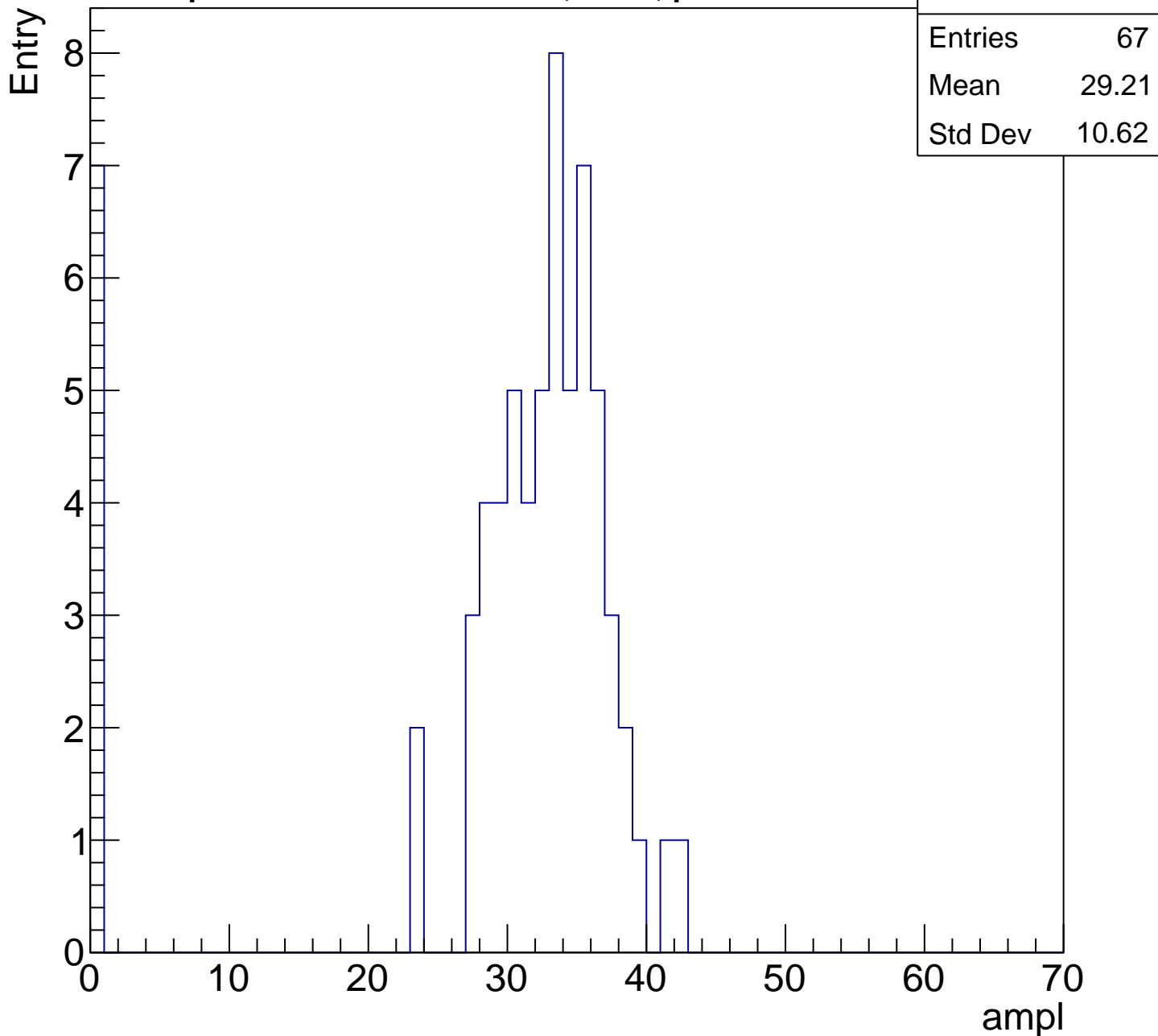
calib_packv5_041523_1651.root, FC#0, port C2

Entries	96
Mean	21.71
Std Dev	10.3



B1L103S, U5-ch106, adc1

calib_packv5_041523_1651.root, FC#0, port C2

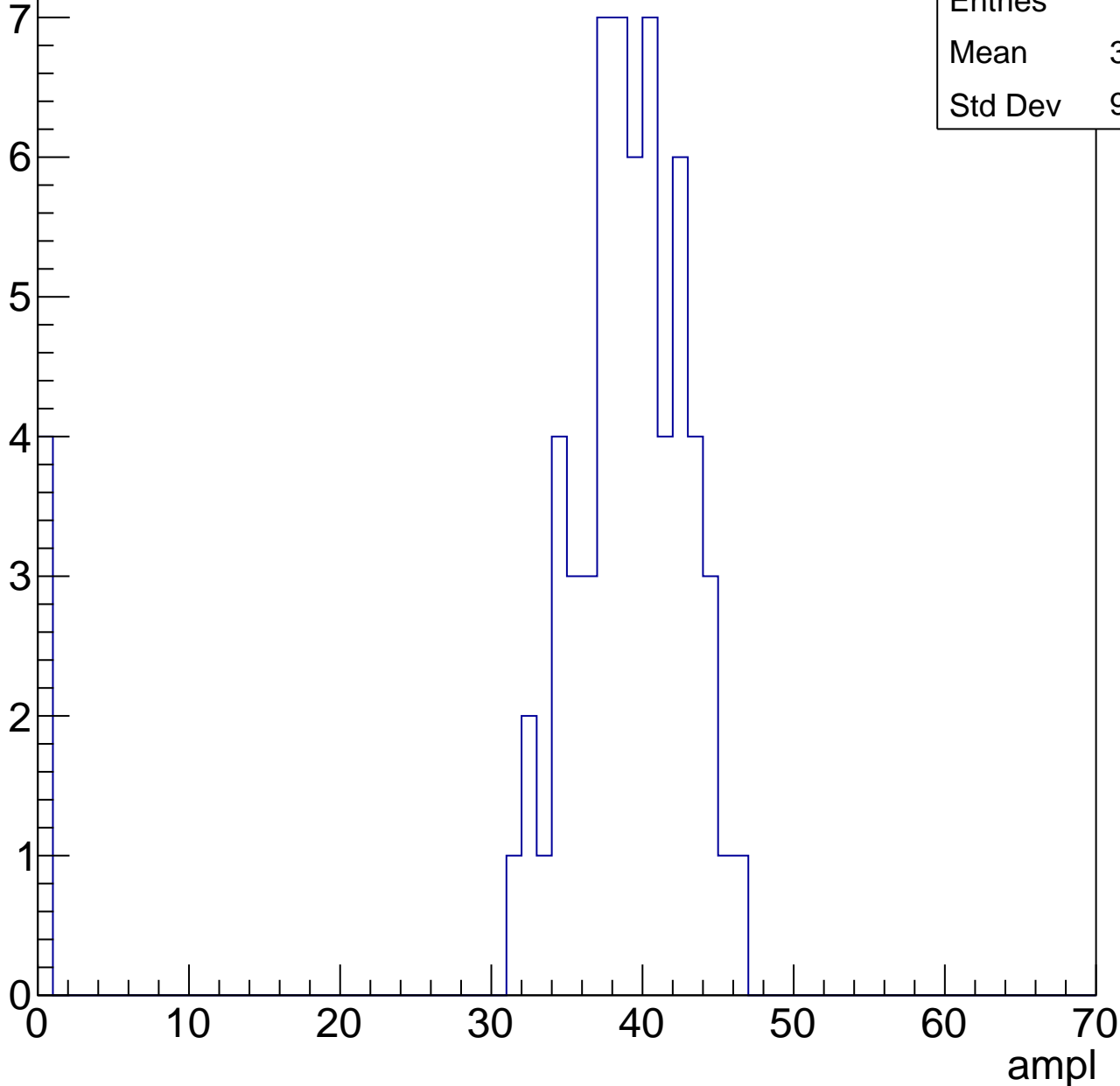


B1L103S, U5-ch106, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	36.36
Std Dev	9.958

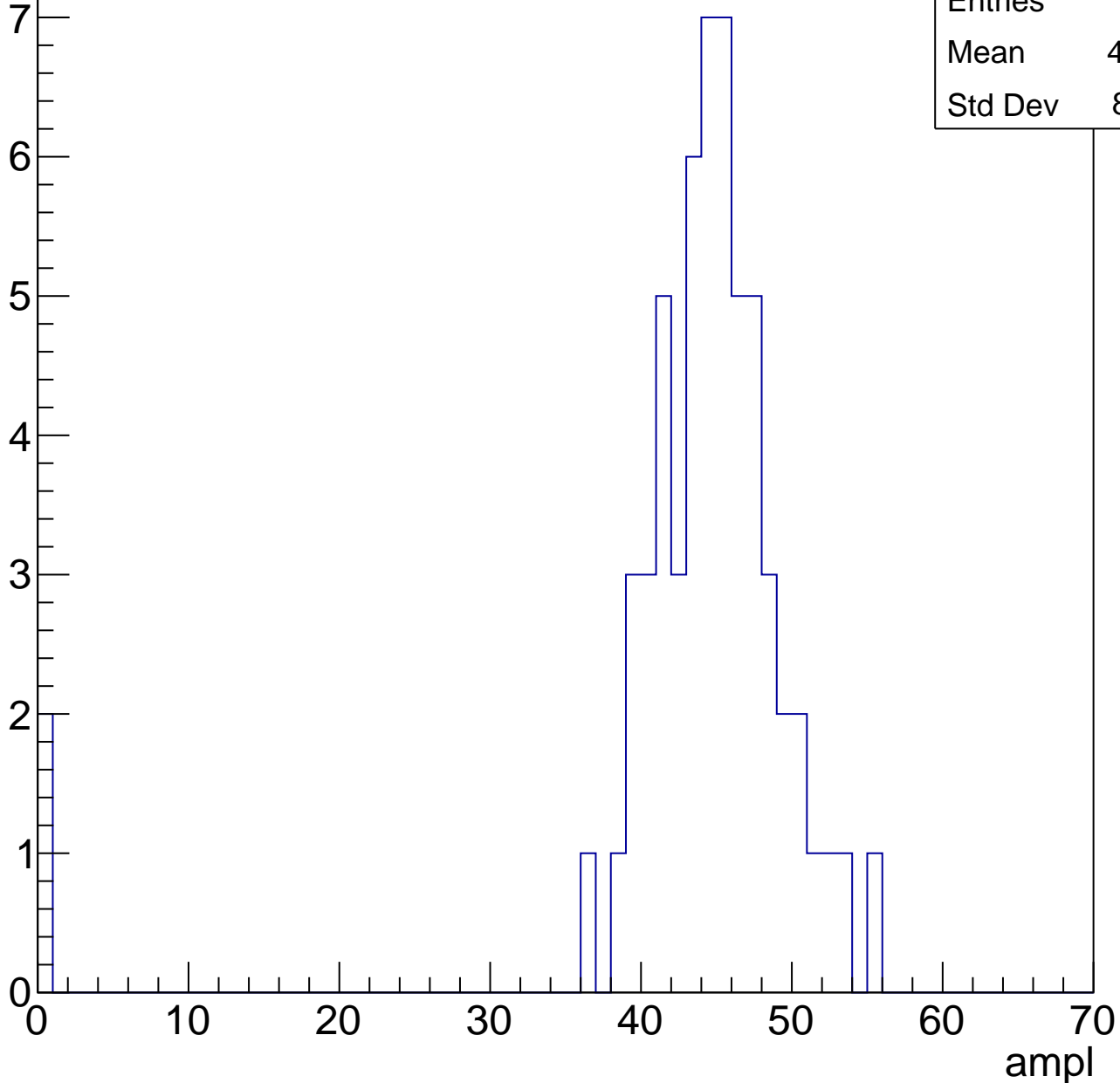


B1L103S, U5-ch106, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	43.07
Std Dev	8.891

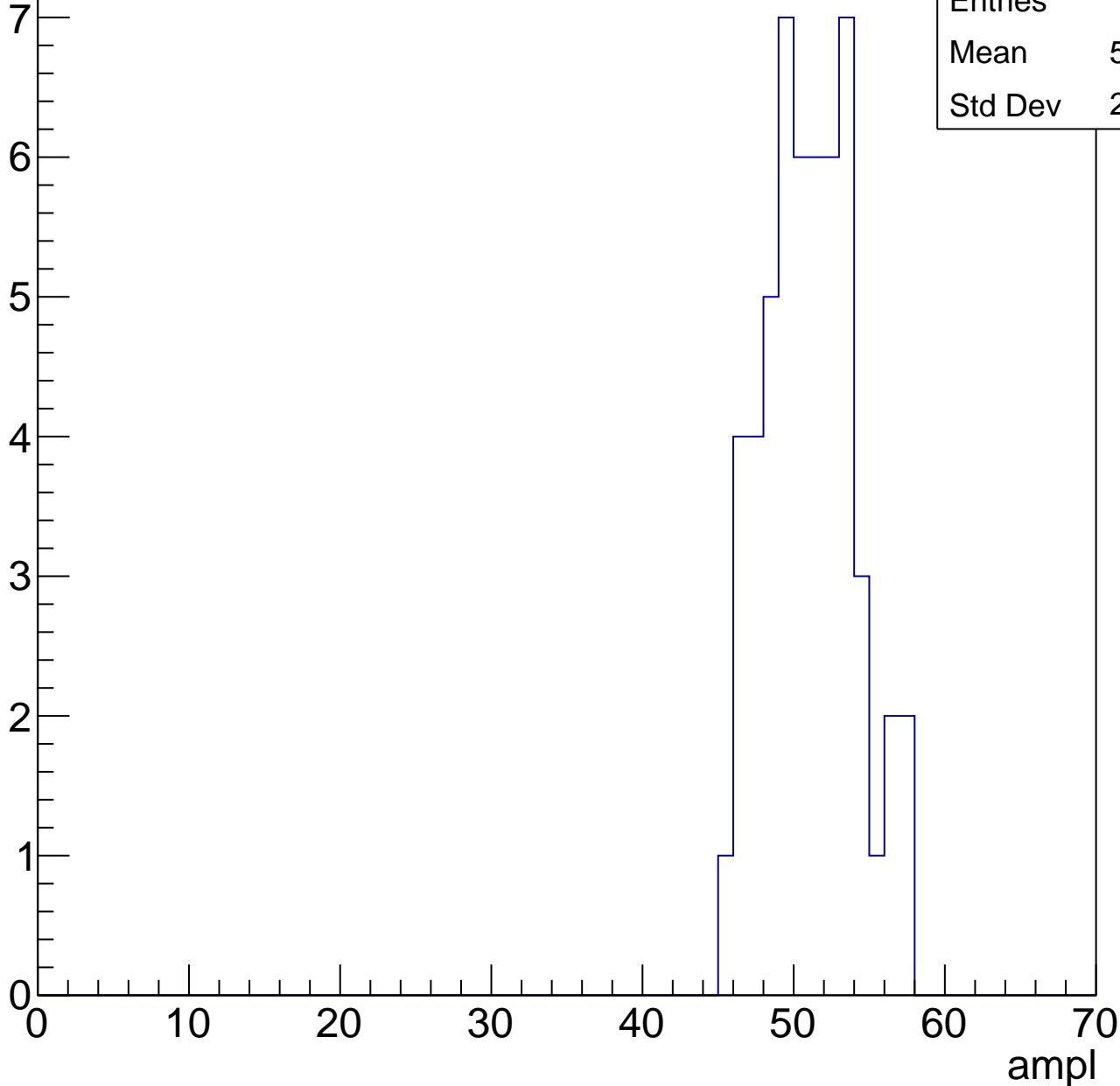


B1L103S, U5-ch106, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

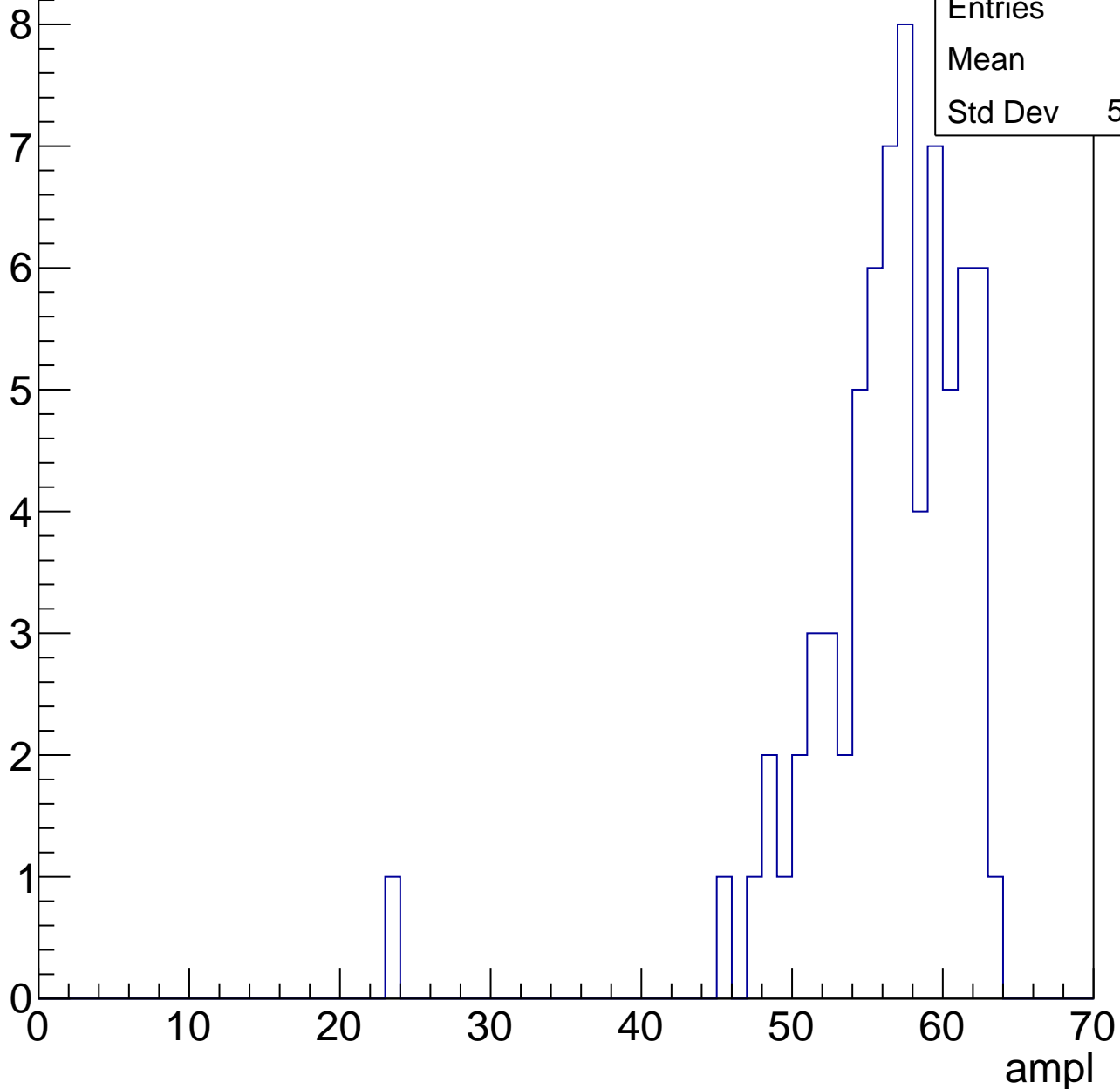
Entries	54
Mean	50.59
Std Dev	2.947



B1L103S, U5-ch106, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

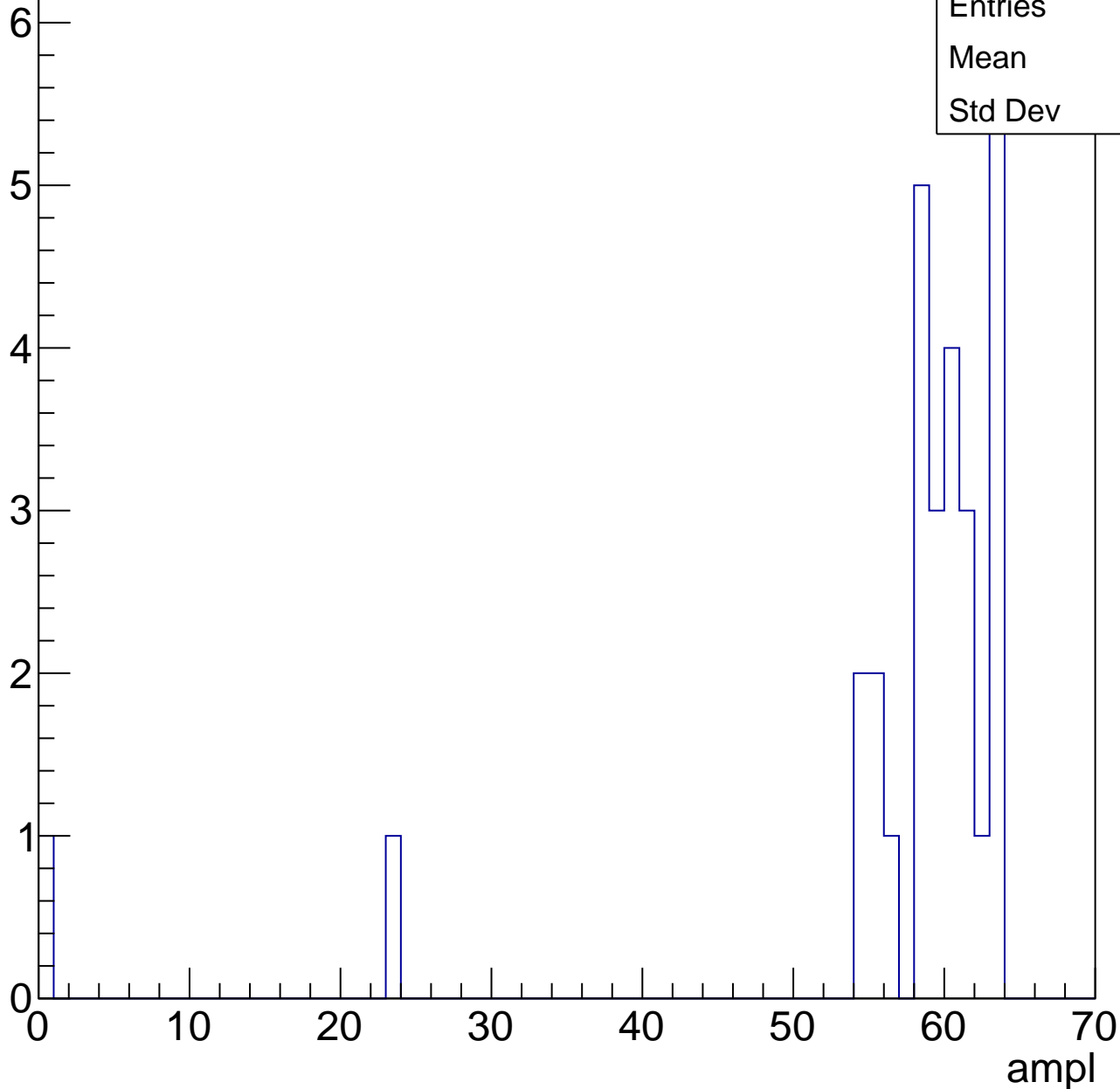


B1L103S, U5-ch106, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	29
Mean	56.1
Std Dev	12.8

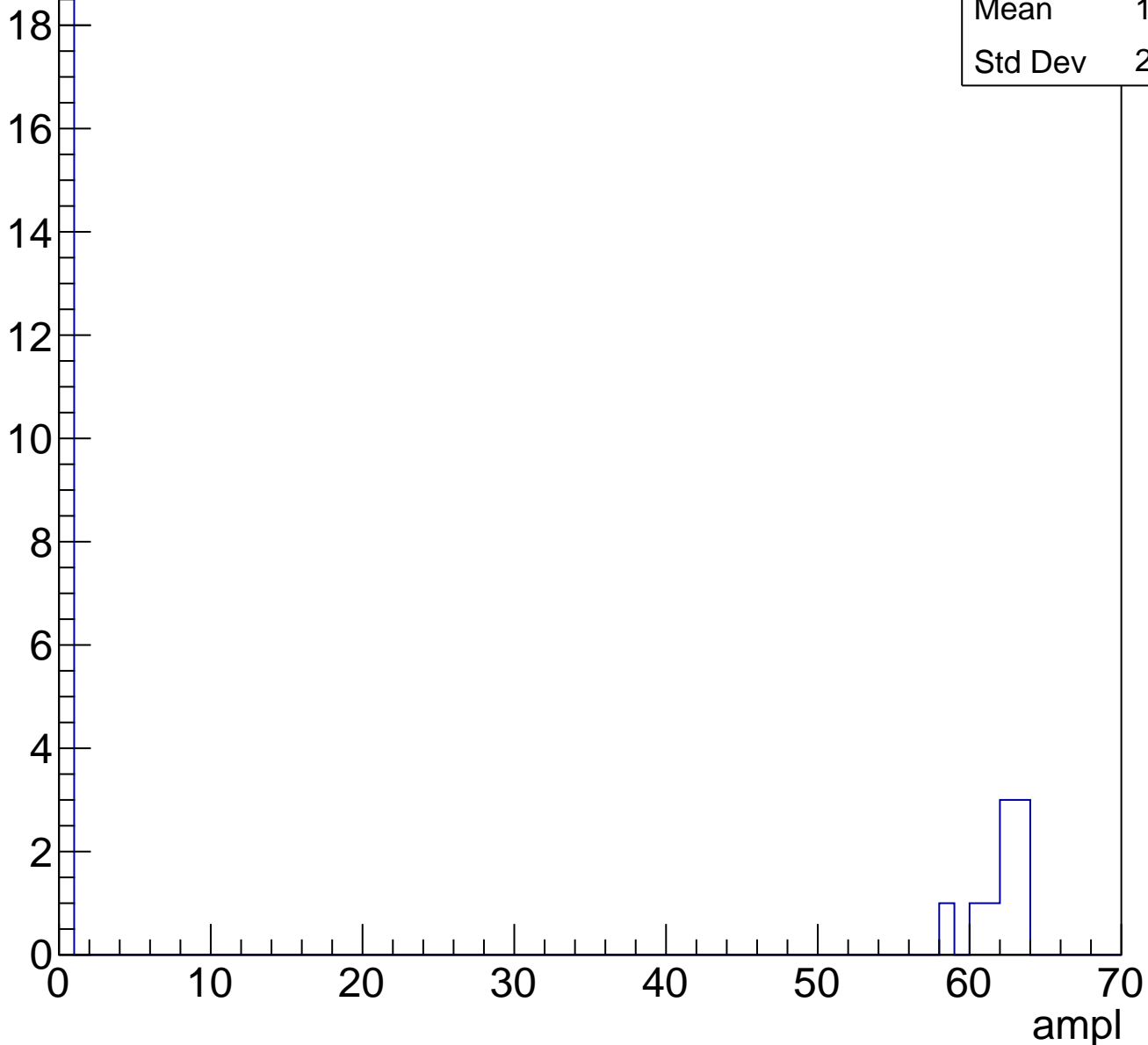


B1L103S, U5-ch106, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	28
Mean	19.79
Std Dev	28.76

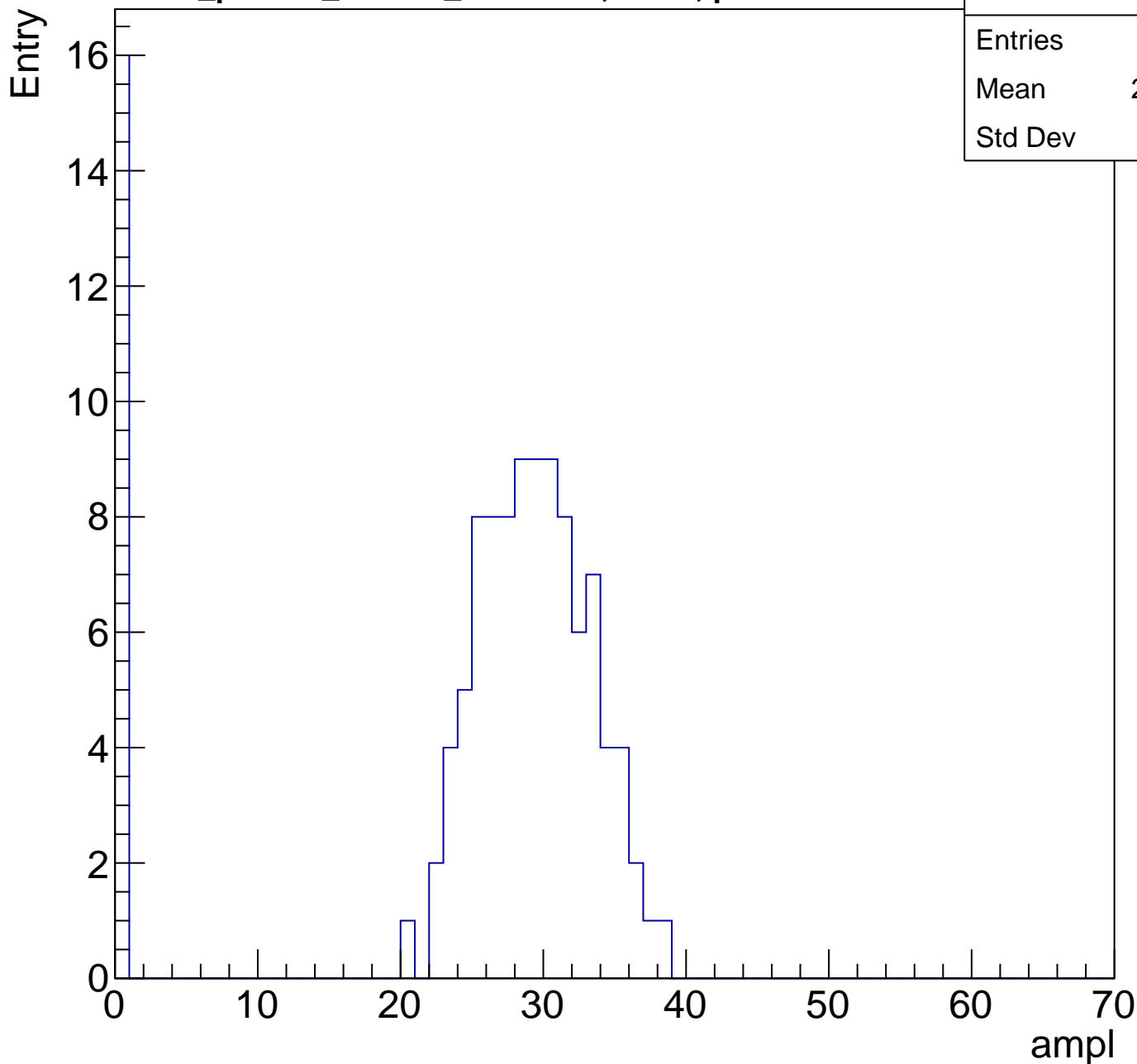
Entry



B1L103S, U5-ch107, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	112
Mean	24.79
Std Dev	10.71

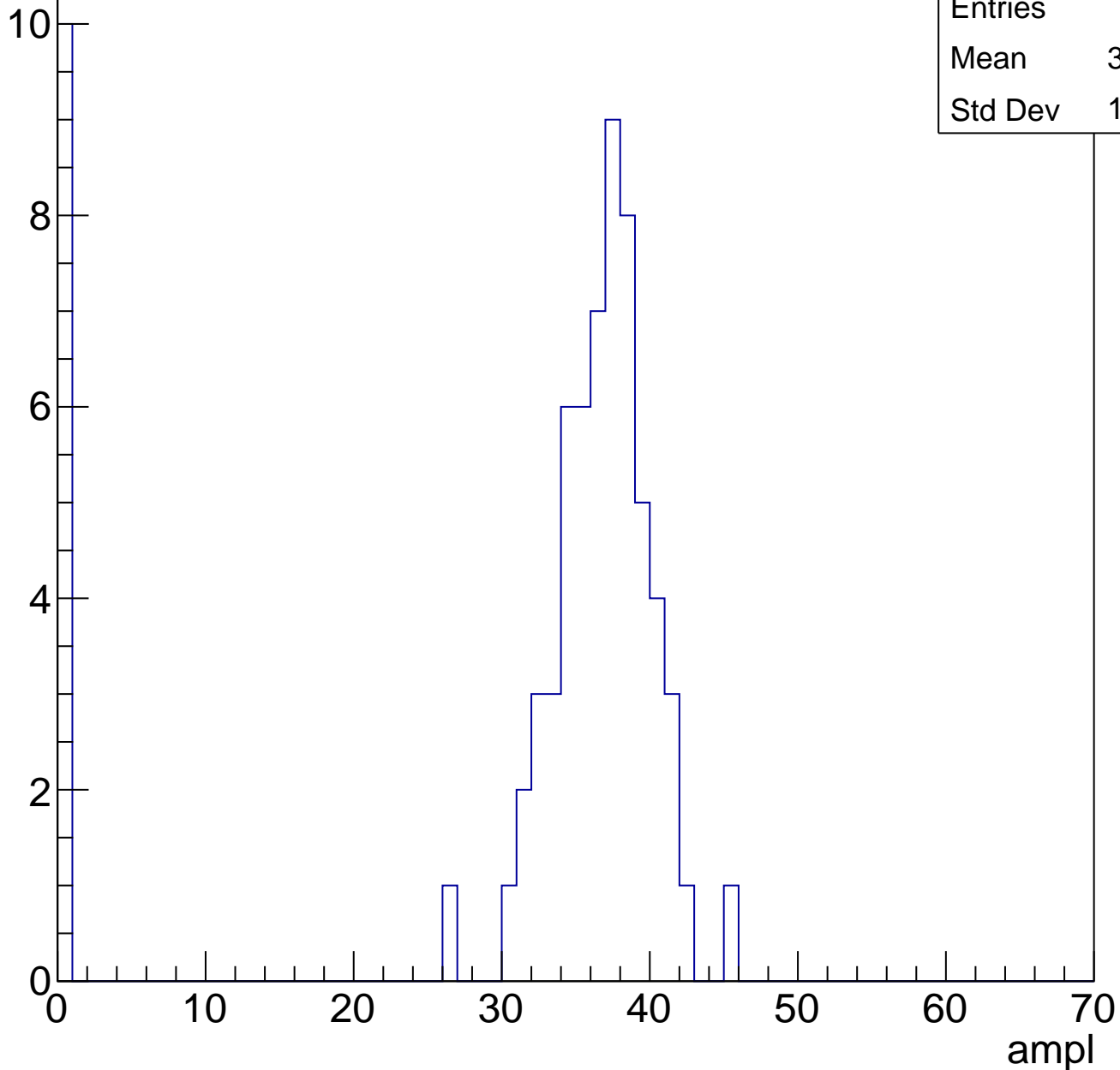


B1L103S, U5-ch107, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	70
Mean	31.16
Std Dev	13.07

Entry

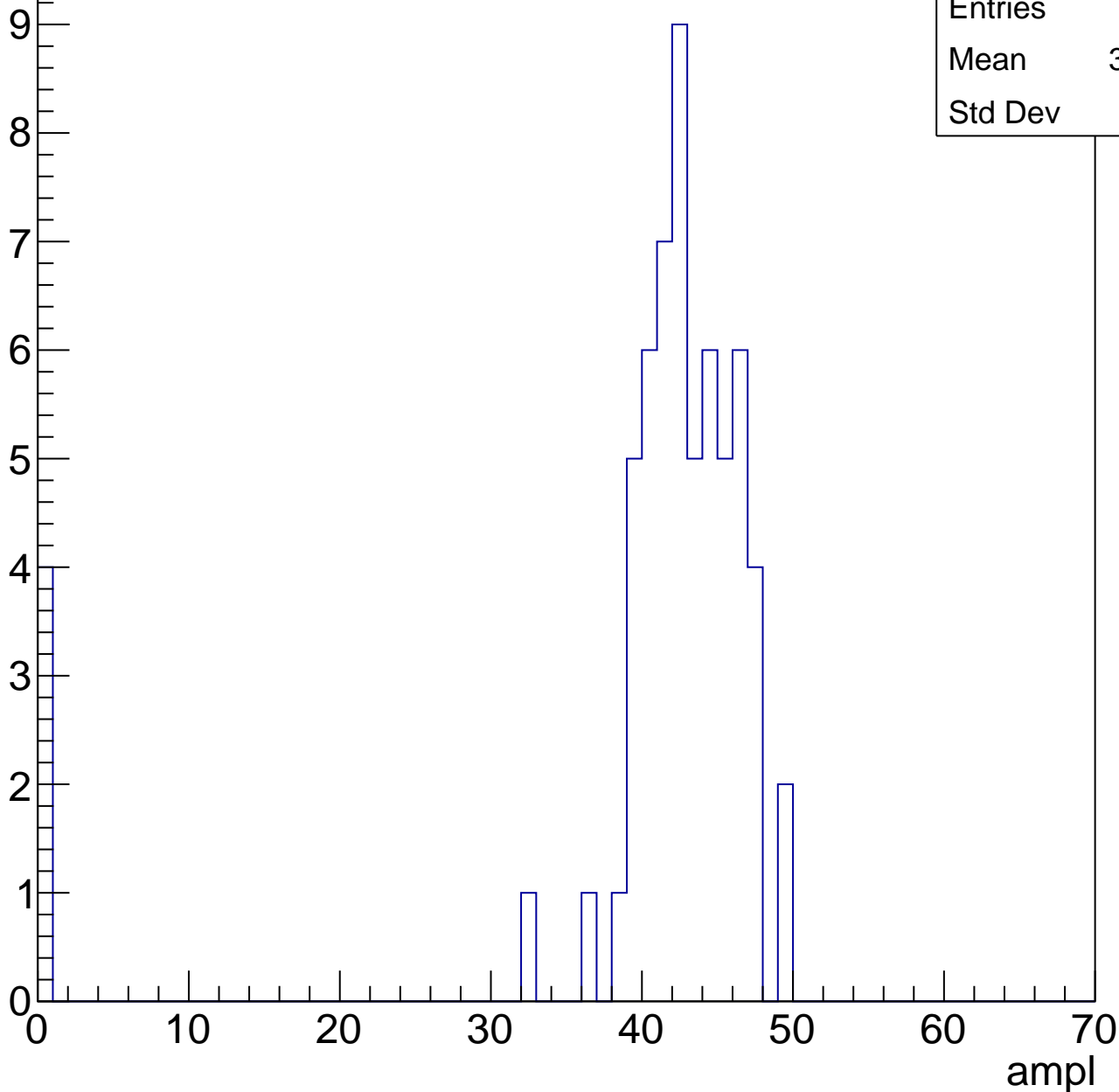


B1L103S, U5-ch107, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

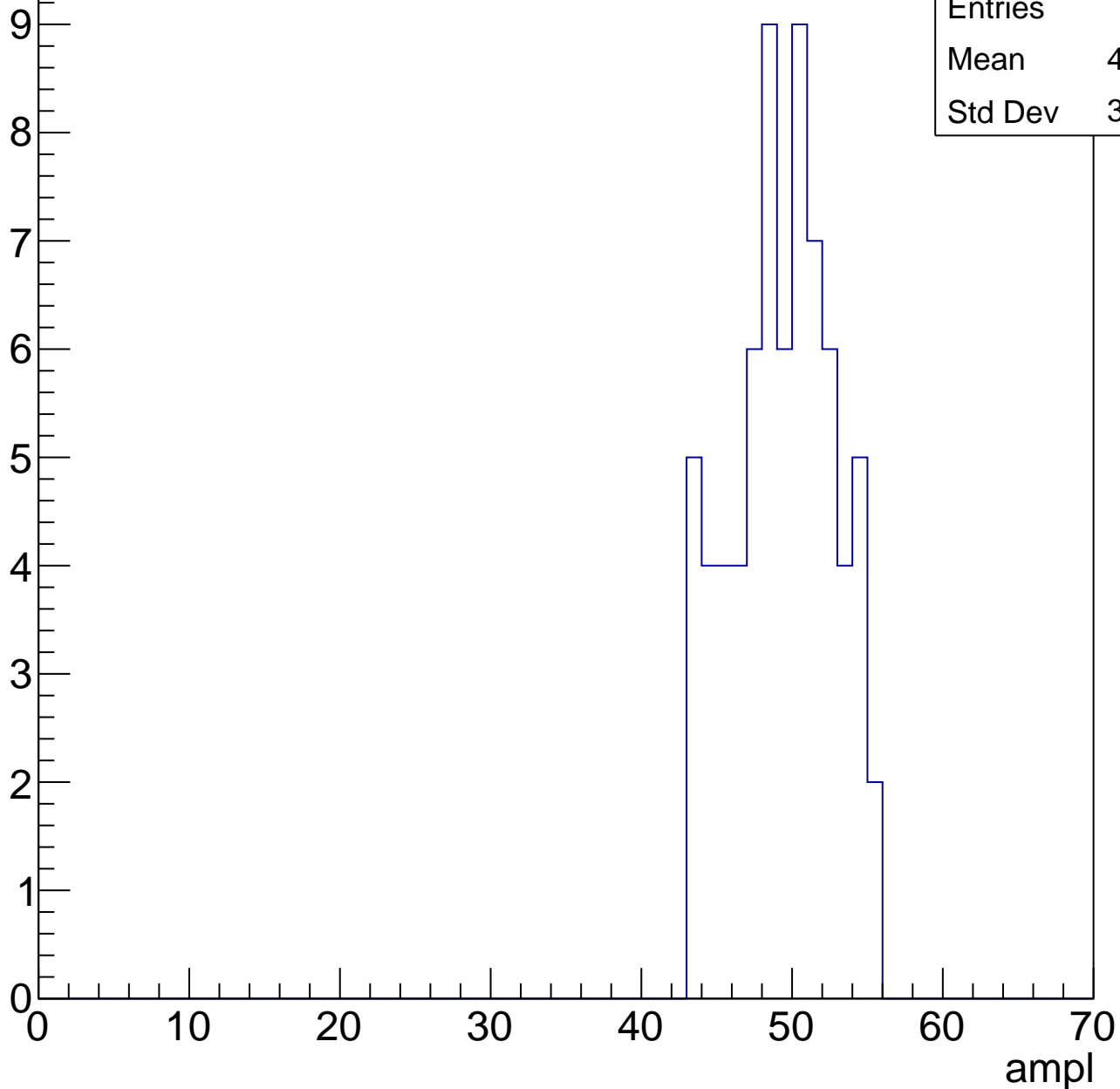
Entries	62
Mean	39.87
Std Dev	10.9



B1L103S, U5-ch107, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

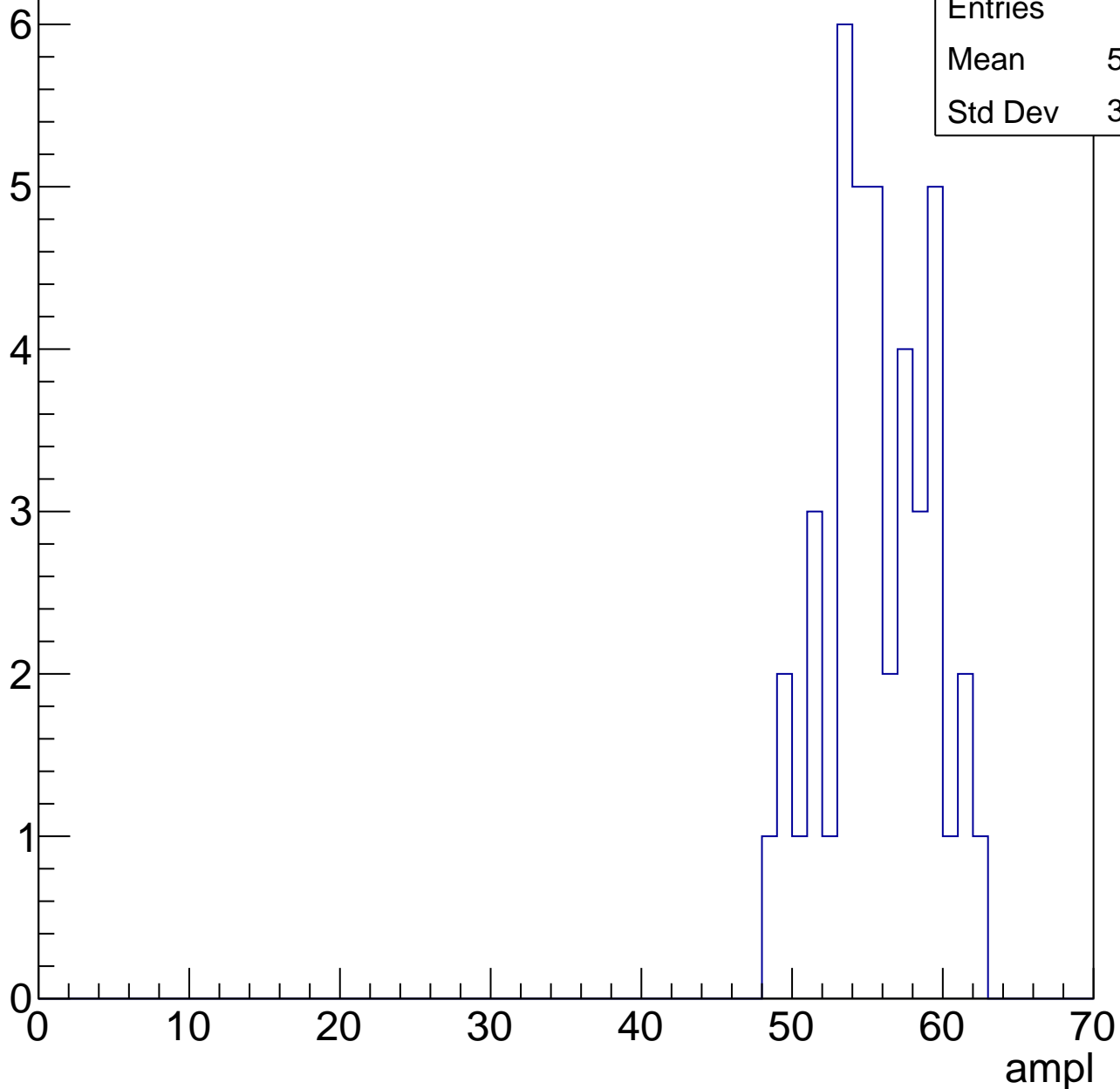


B1L103S, U5-ch107, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	42
Mean	55.17
Std Dev	3.457

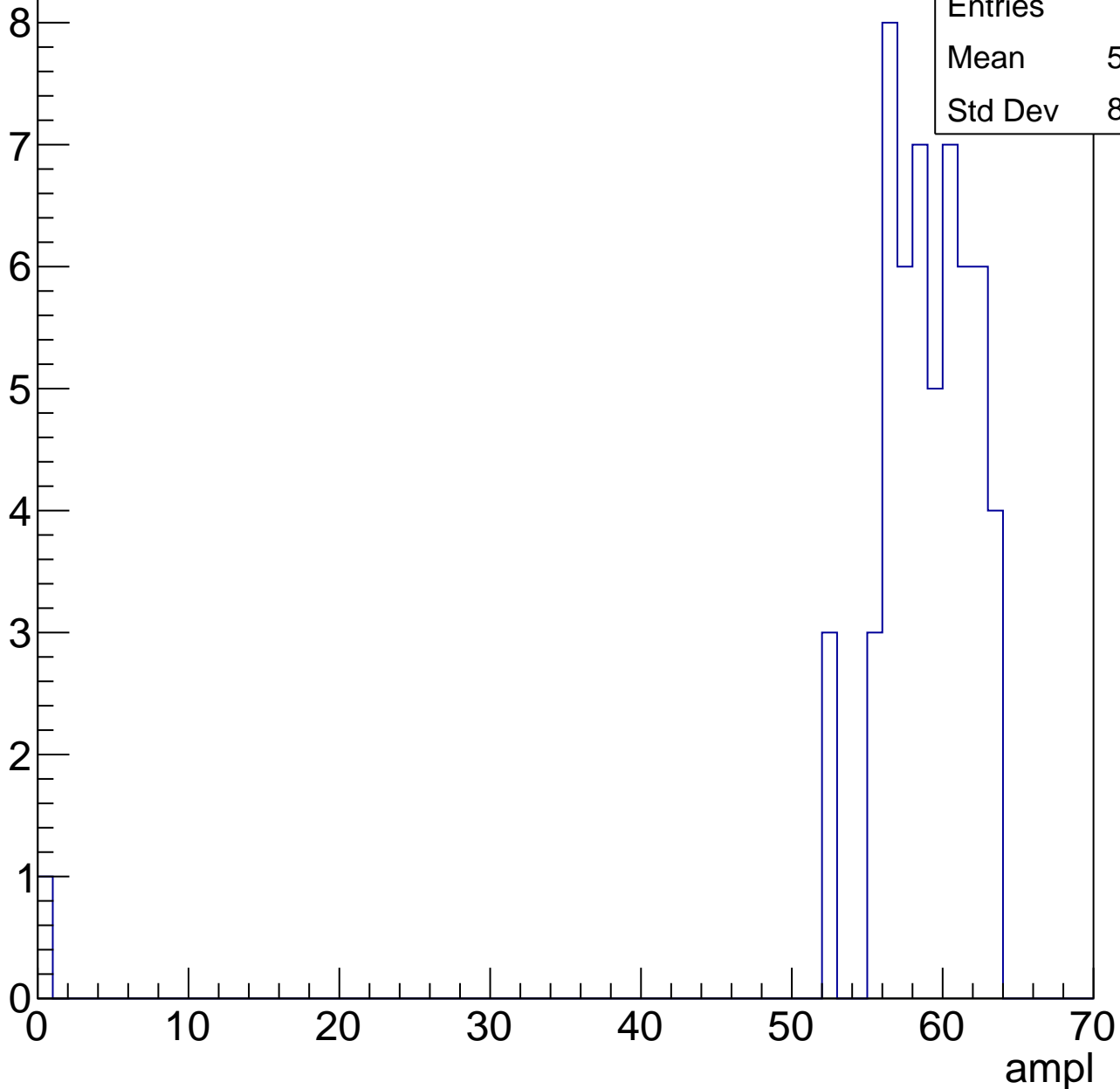


B1L103S, U5-ch107, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	57.54
Std Dev	8.246

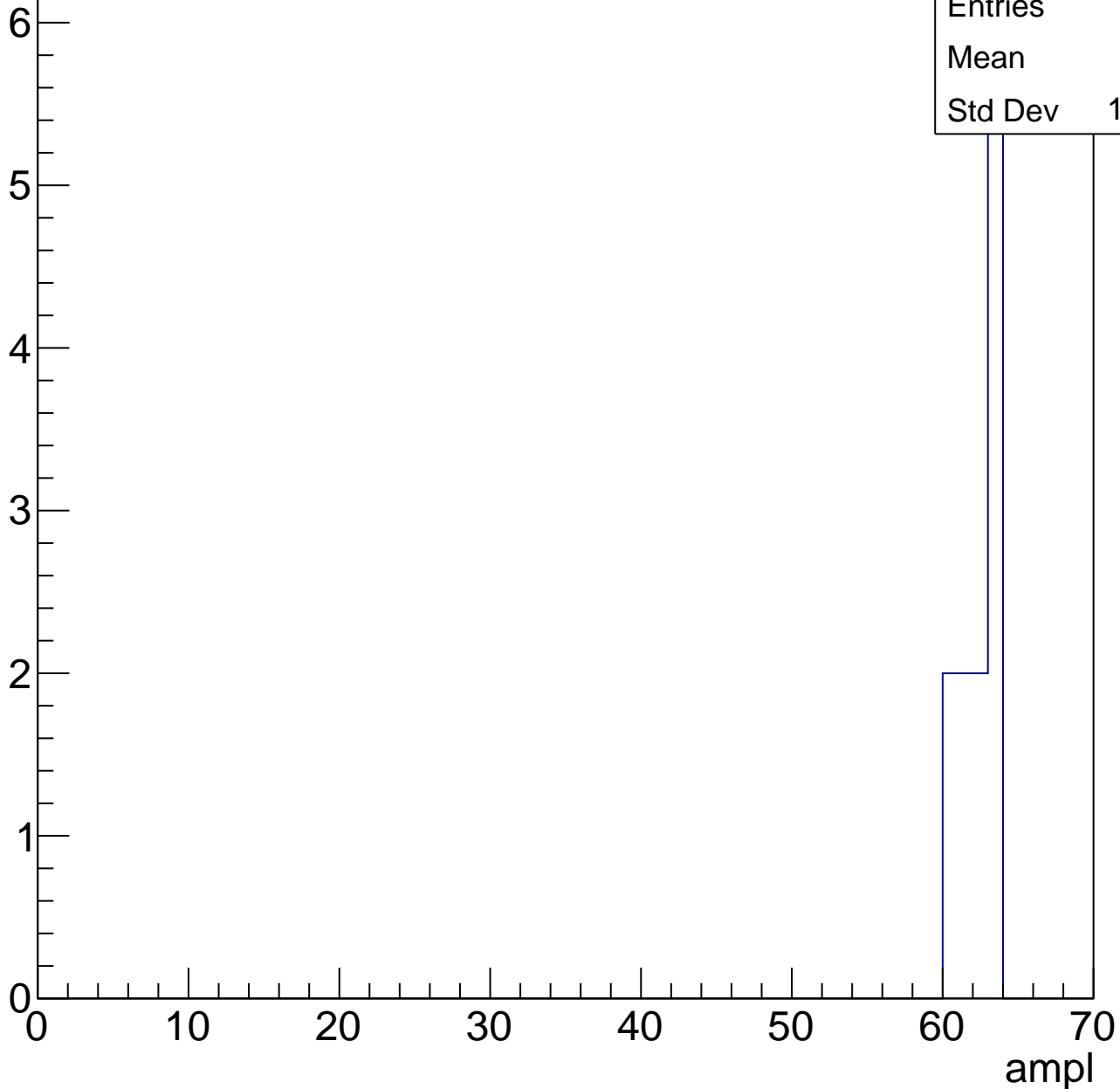


B1L103S, U5-ch107, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	12
Mean	62
Std Dev	1.155

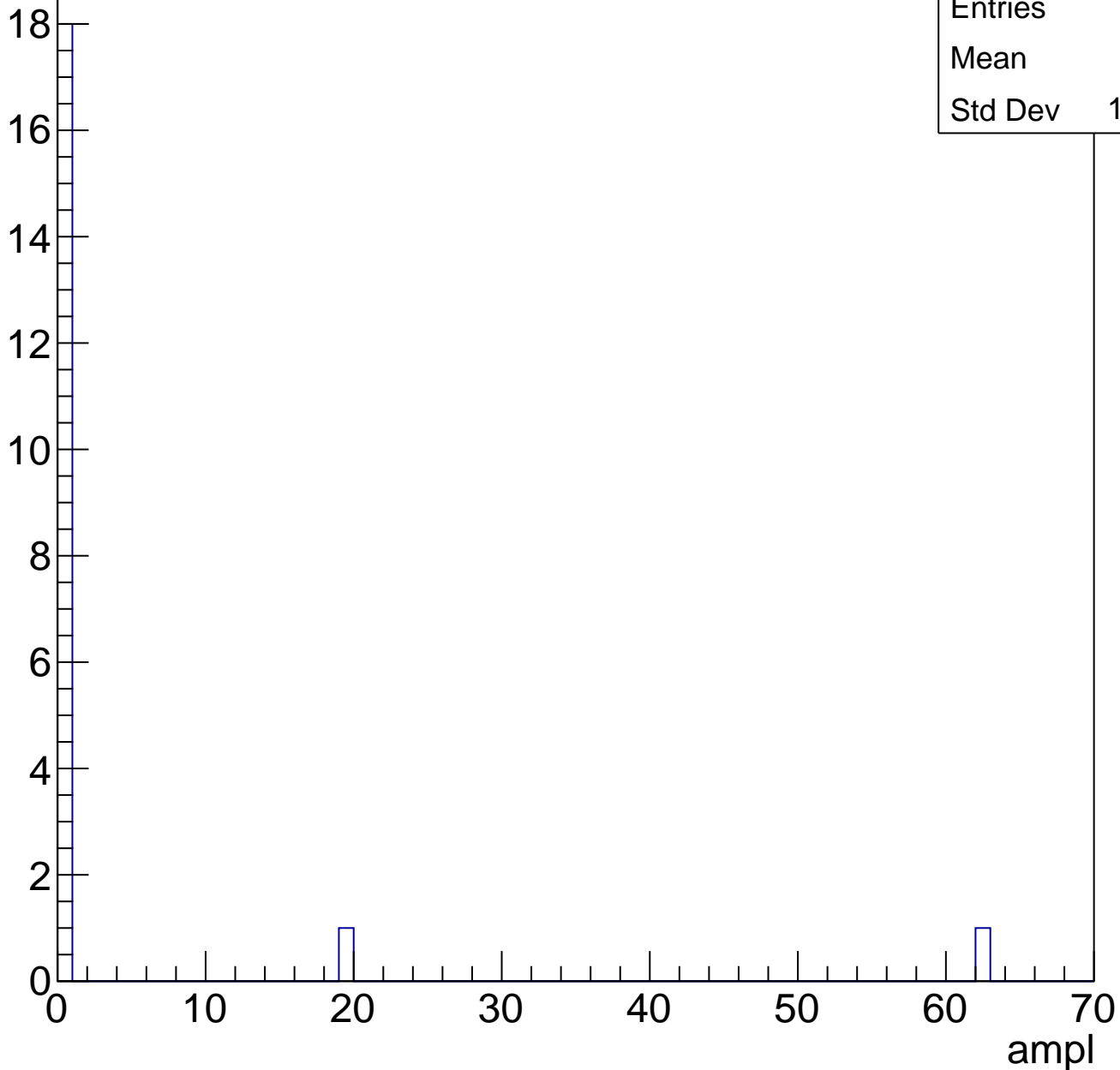


B1L103S, U5-ch107, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	4.05
Std Dev	13.92

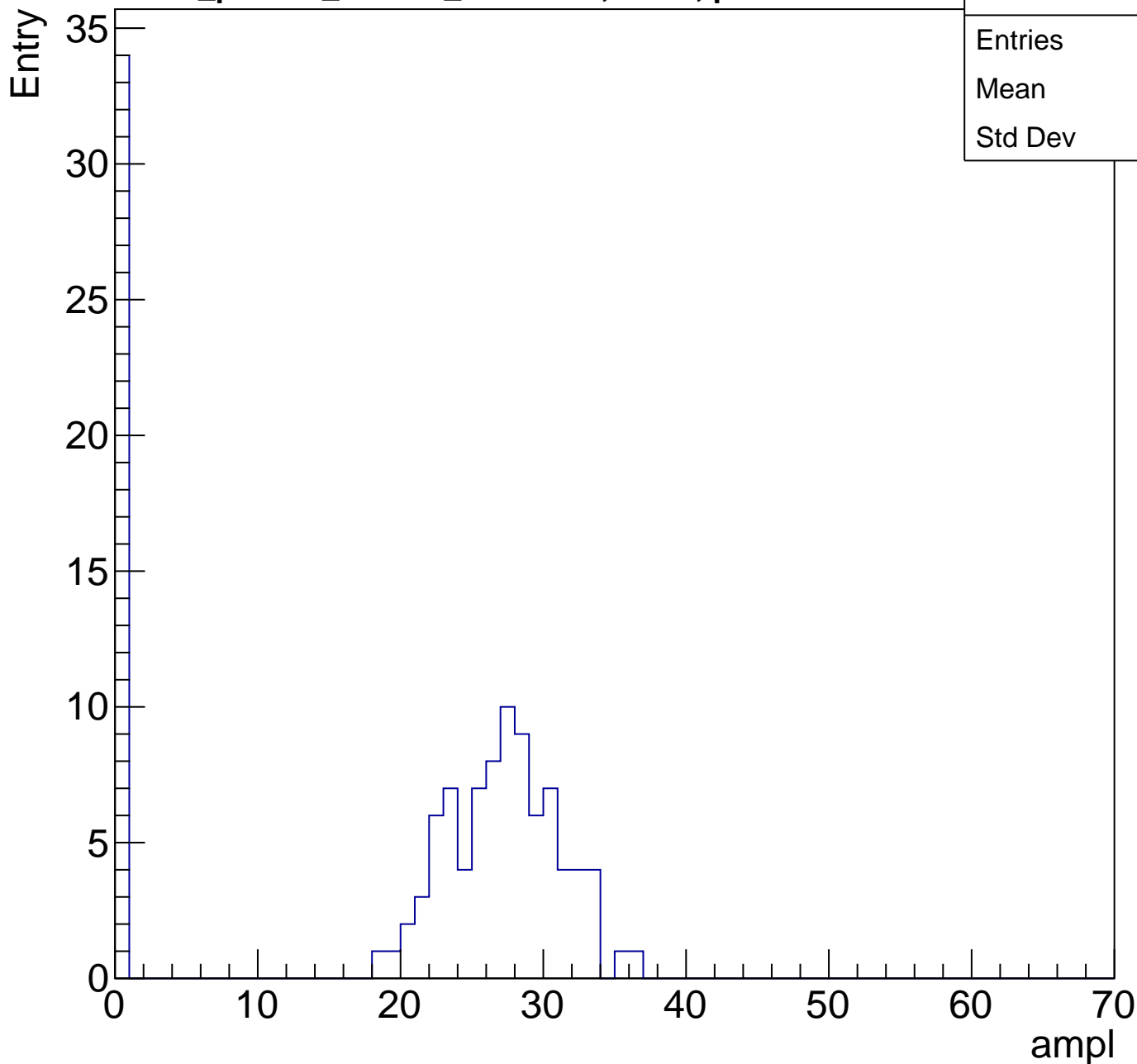
Entry



B1L103S, U5-ch108, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	119
Mean	19.1
Std Dev	12.5

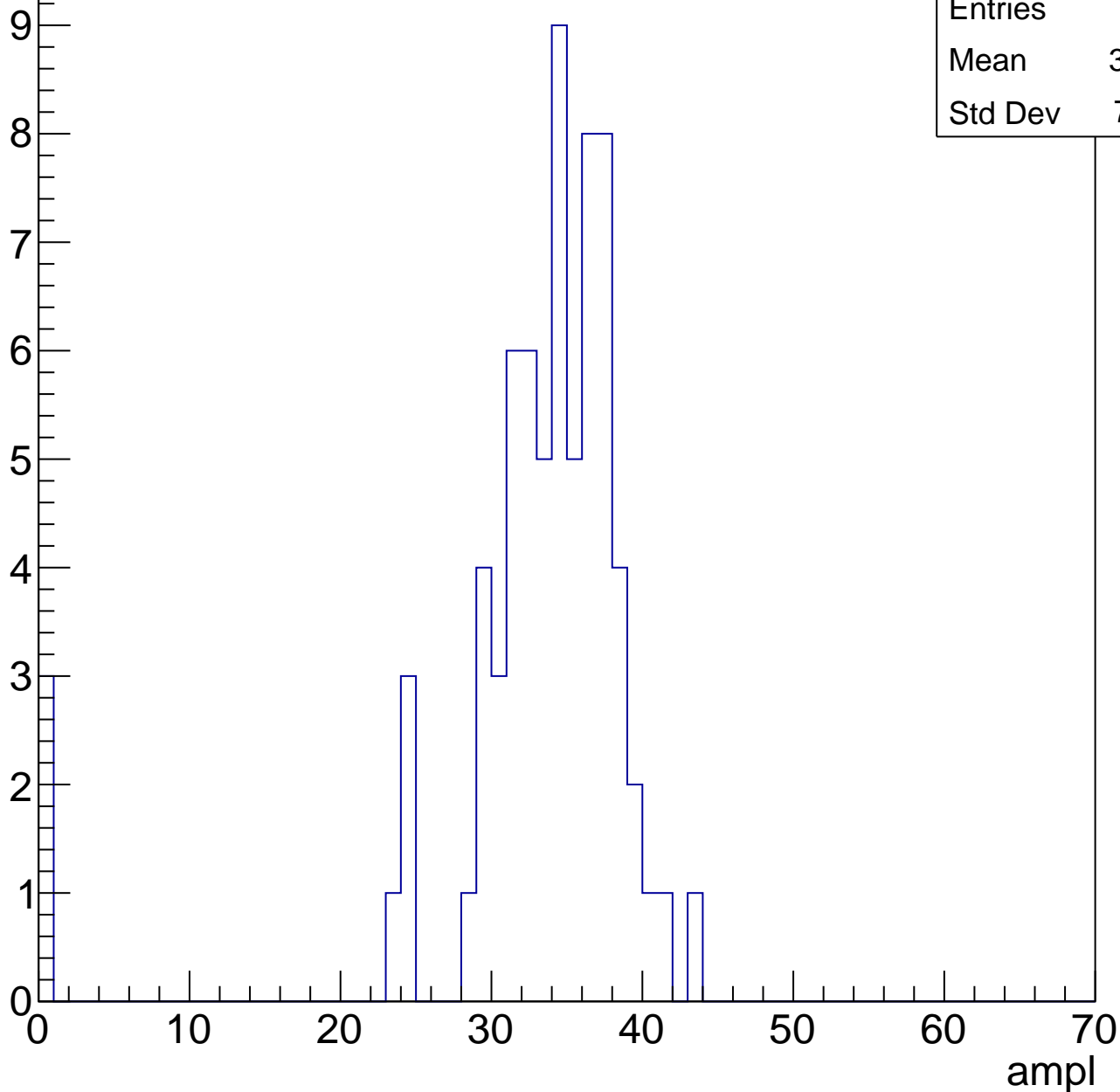


B1L103S, U5-ch108, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	32.27
Std Dev	7.811

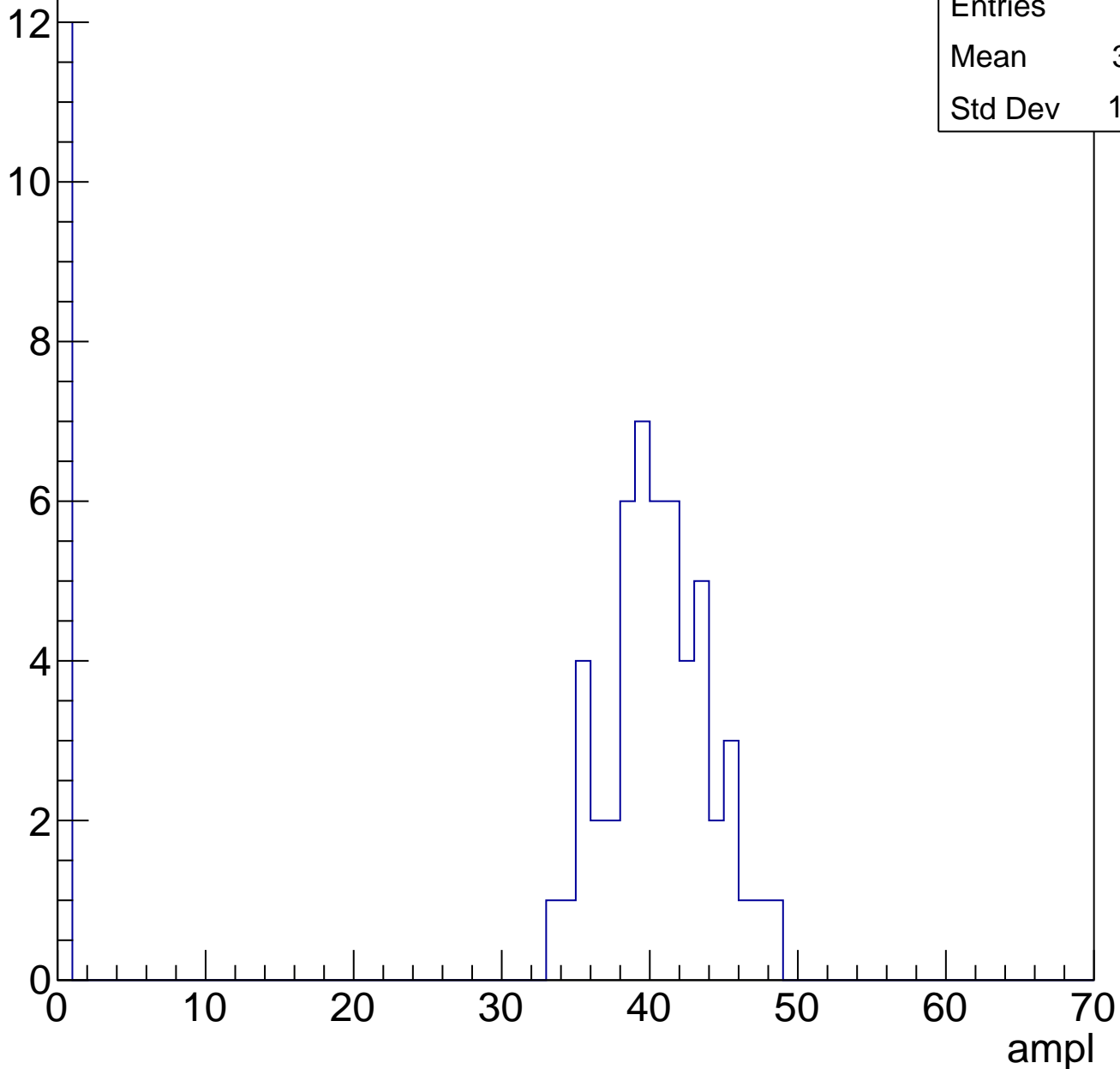


B1L103S, U5-ch108, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	64
Mean	32.61
Std Dev	15.96

Entry

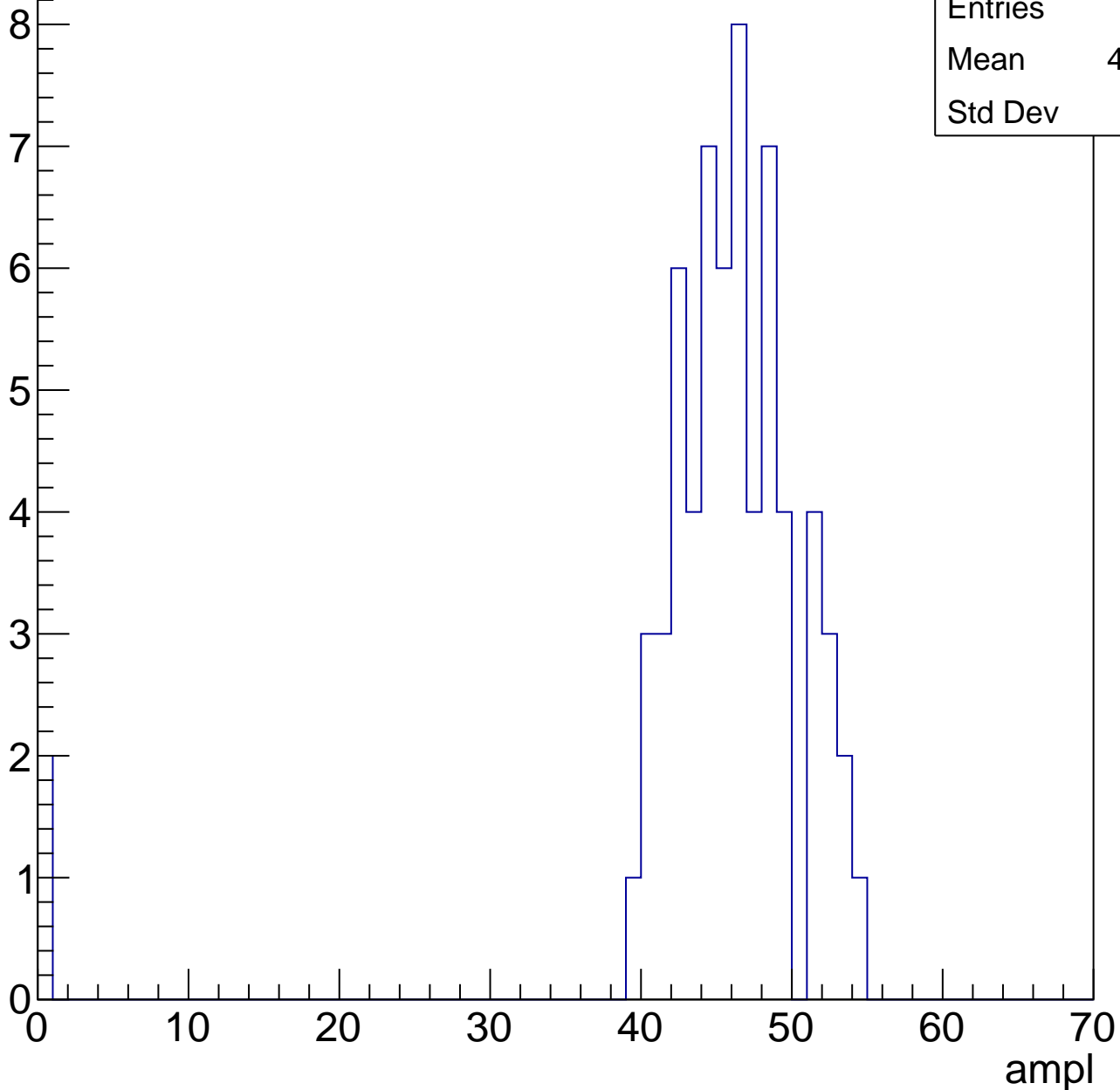


B1L103S, U5-ch108, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	44.49
Std Dev	8.7



B1L103S, U5-ch108, adc4

calib_packv5_041523_1651.root, FC#0, port C2

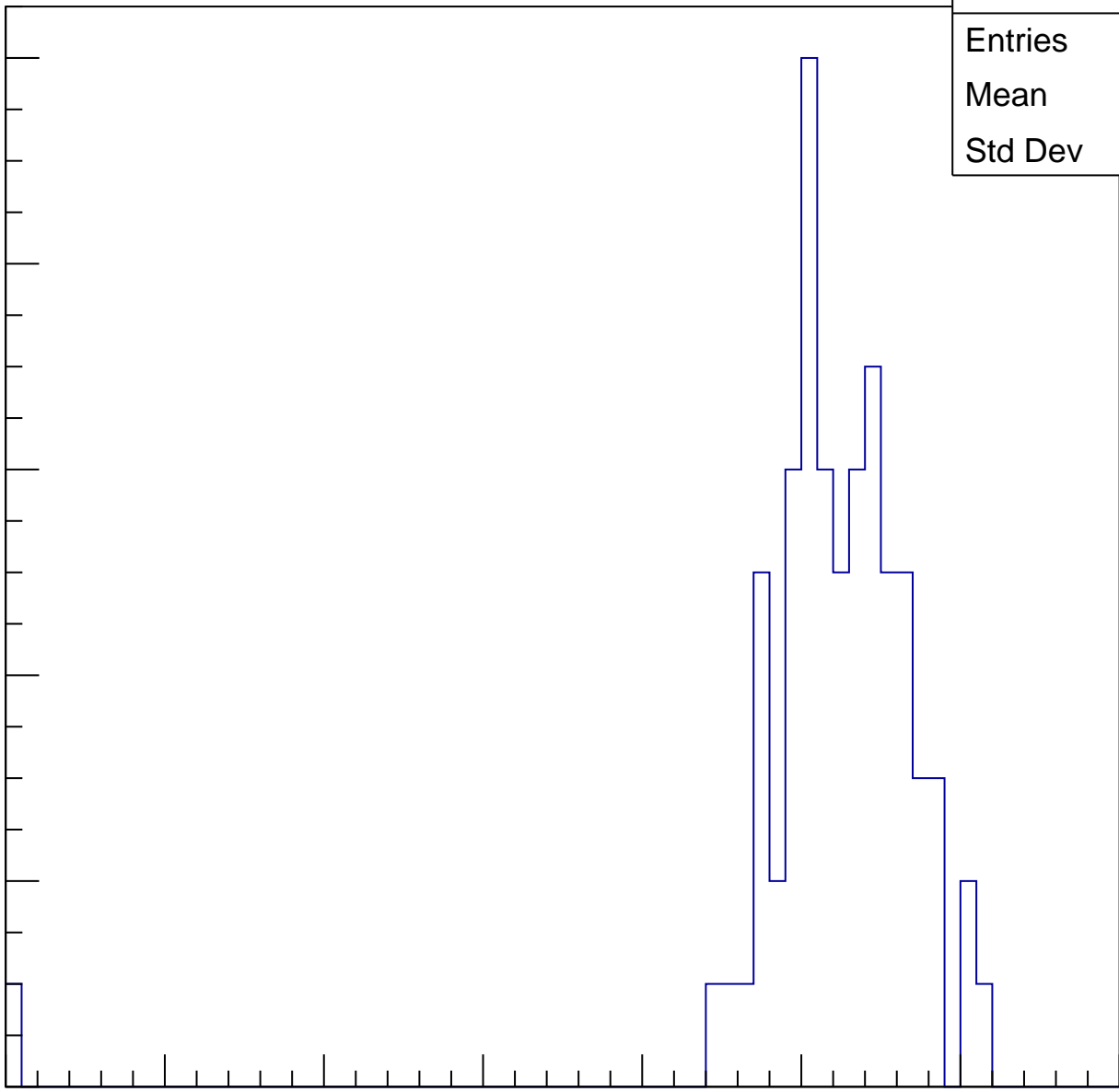
Entries	70
Mean	51.47
Std Dev	7.213

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

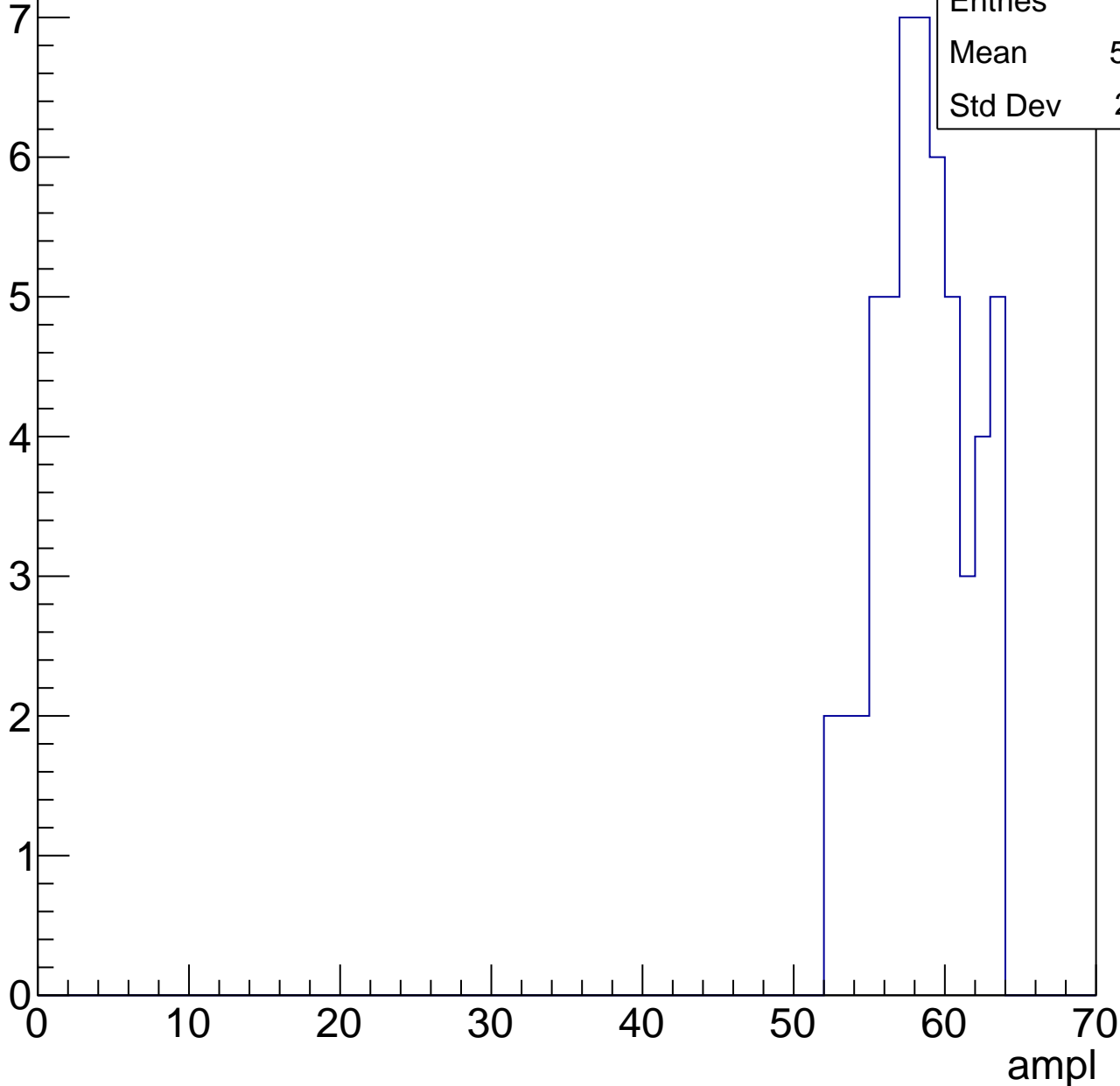


B1L103S, U5-ch108, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	58.08
Std Dev	2.971

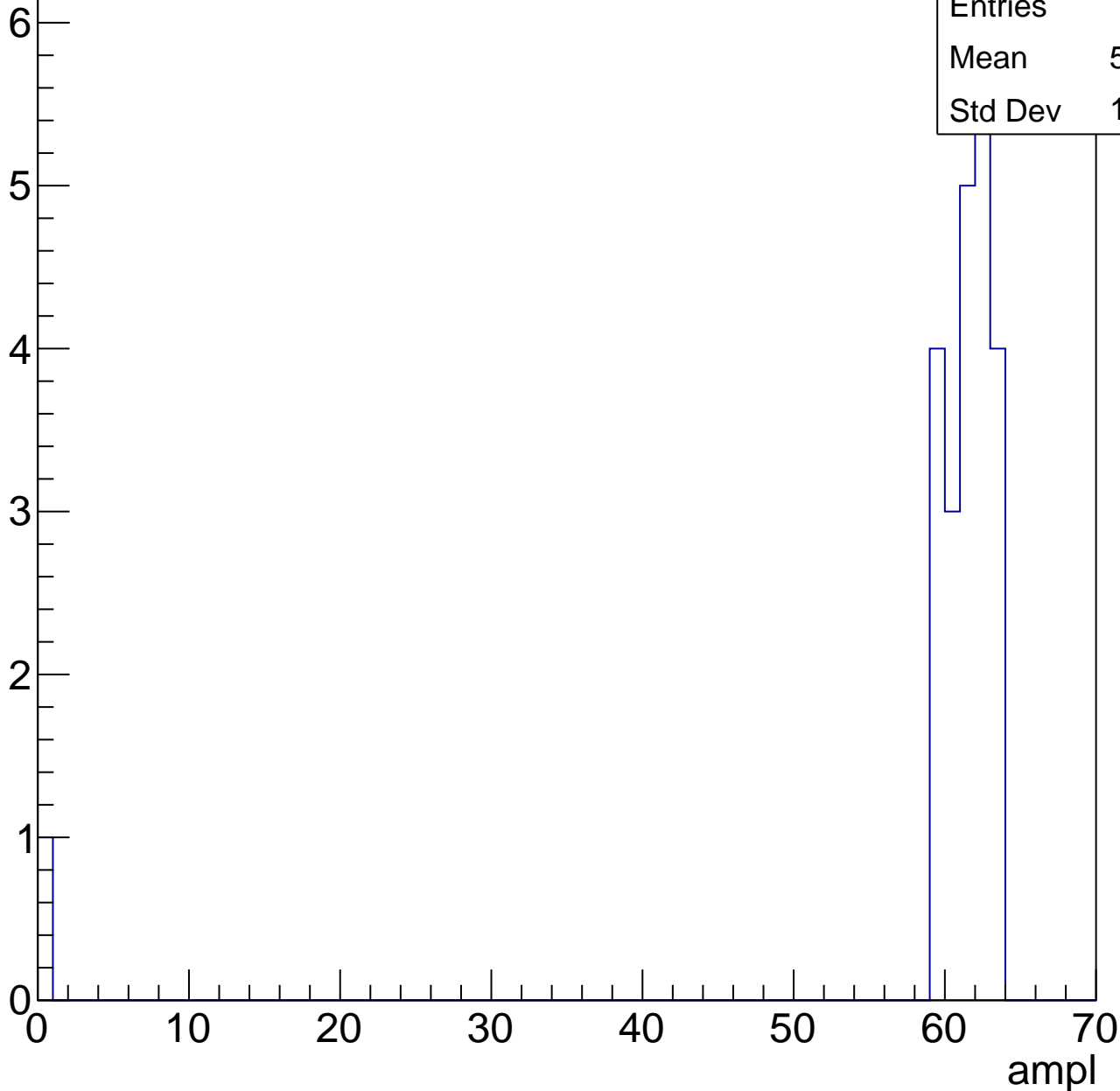


B1L103S, U5-ch108, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	23
Mean	58.48
Std Dev	12.54

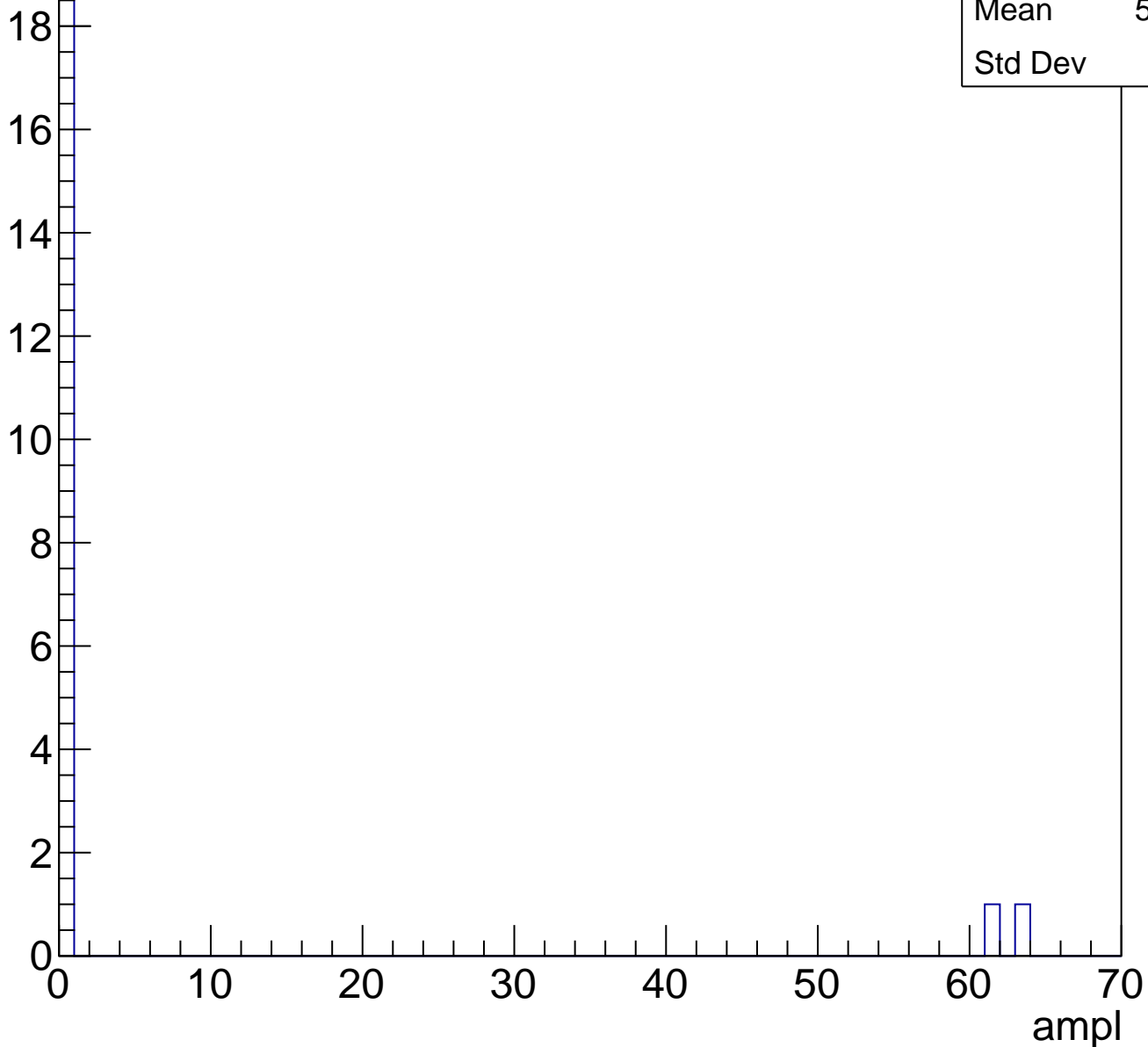


B1L103S, U5-ch108, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	5.905
Std Dev	18.2

Entry

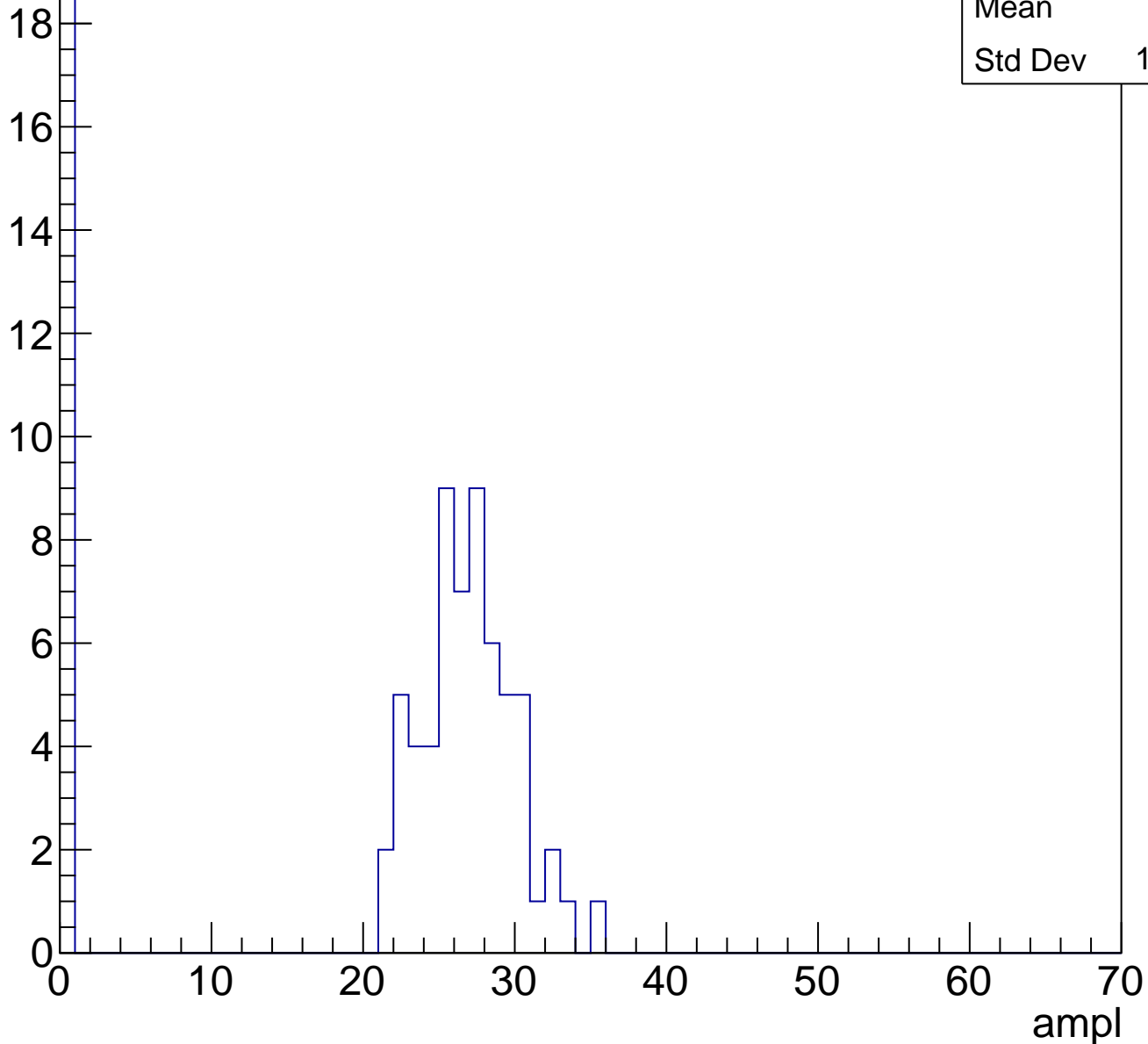


B1L103S, U5-ch109, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	20.2
Std Dev	11.58

Entry

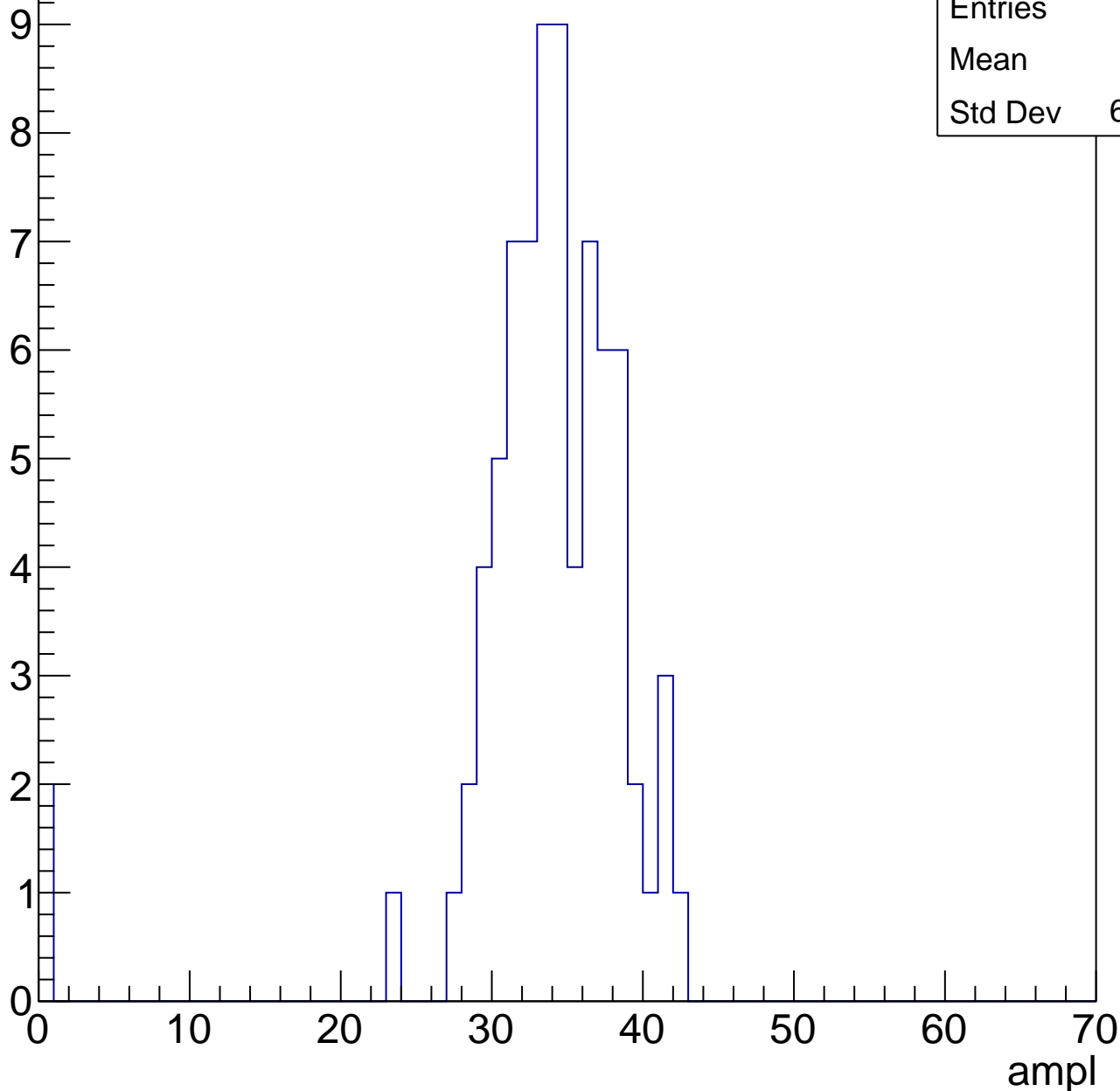


B1L103S, U5-ch109, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	33
Std Dev	6.483



B1L103S, U5-ch109, adc2

calib_packv5_041523_1651.root, FC#0, port C2

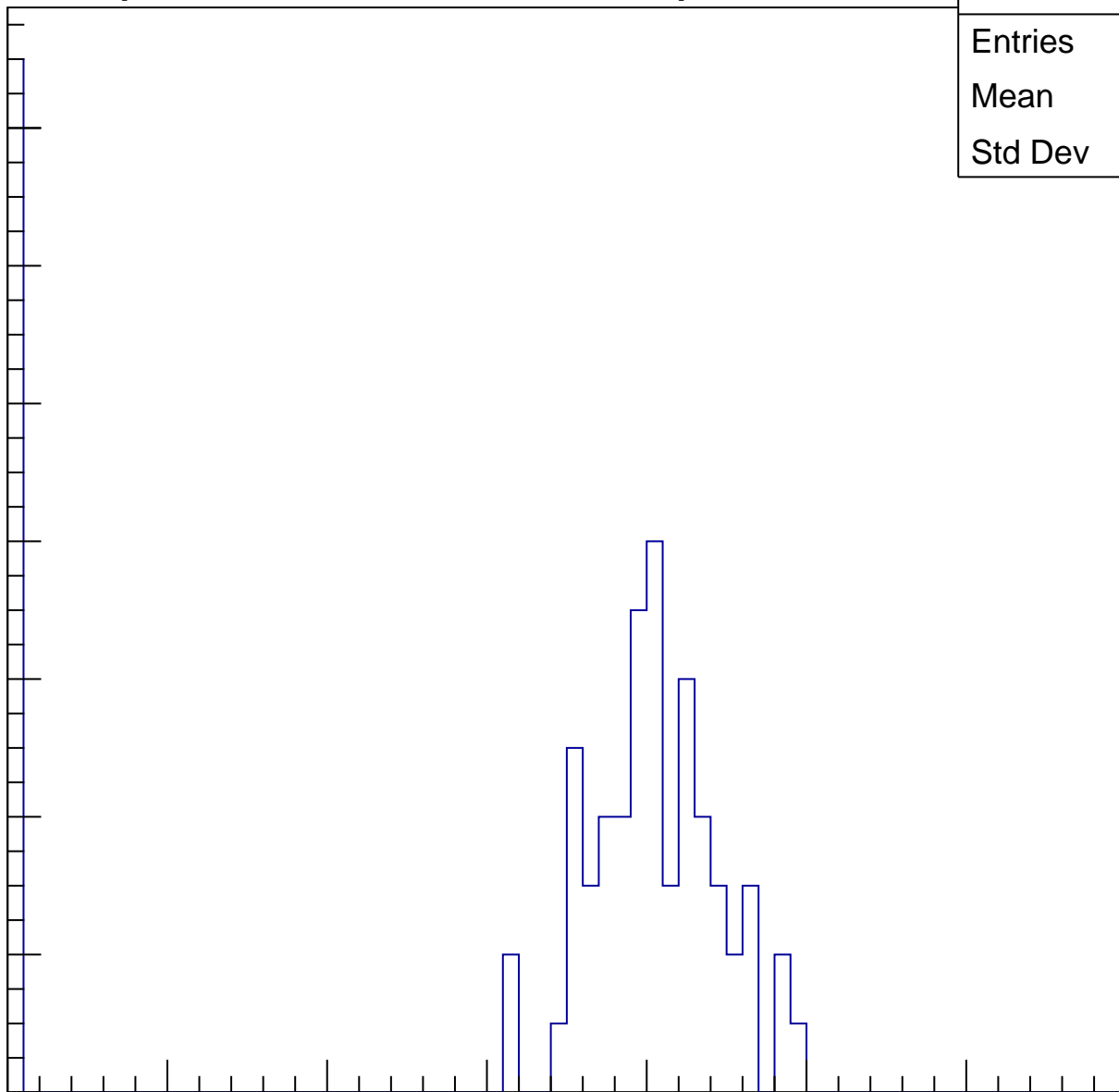
Entries	73
Mean	31.84
Std Dev	16.57

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

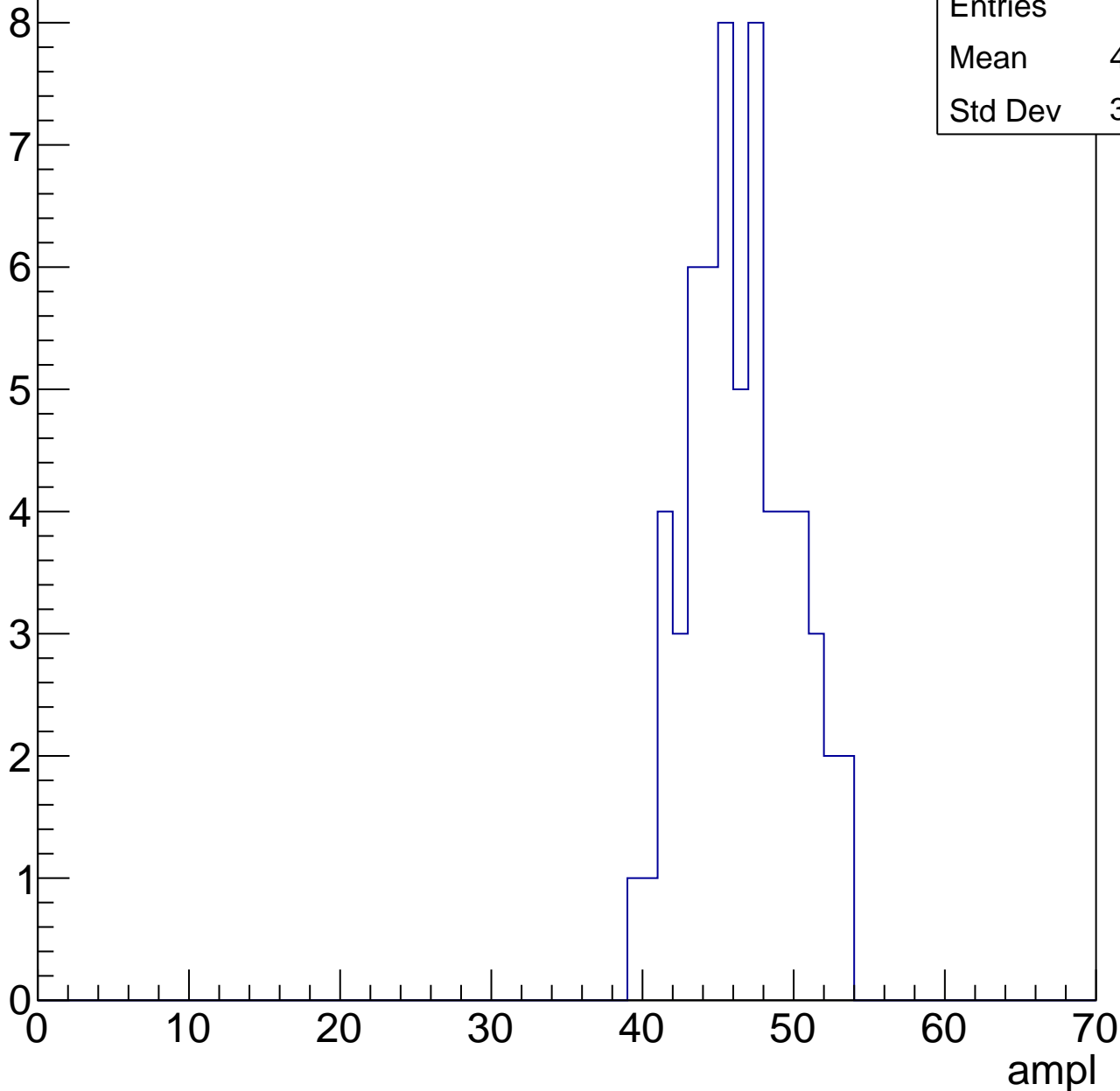


B1L103S, U5-ch109, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	46.03
Std Dev	3.358

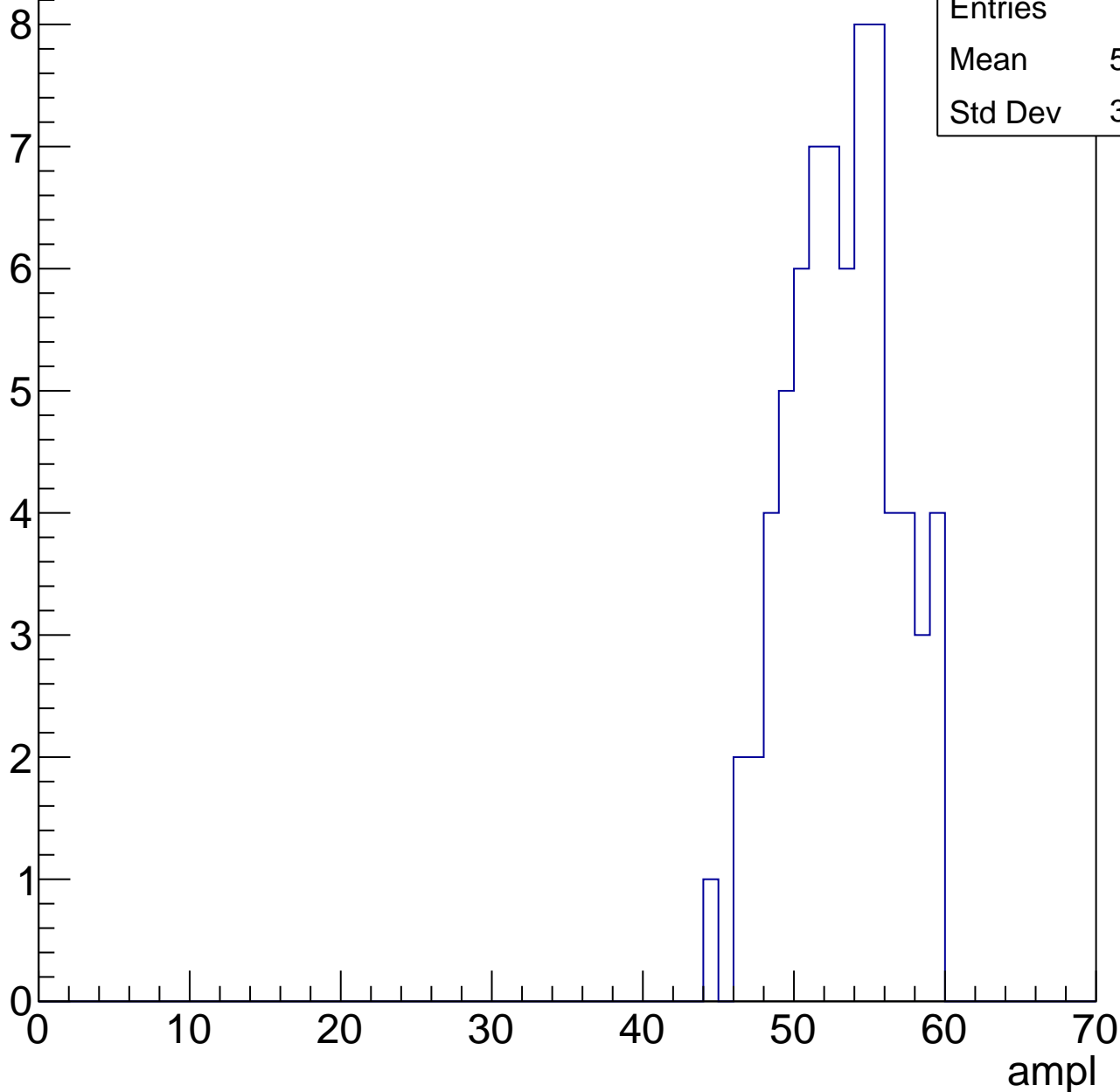


B1L103S, U5-ch109, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	52.68
Std Dev	3.504



B1L103S, U5-ch109, adc5

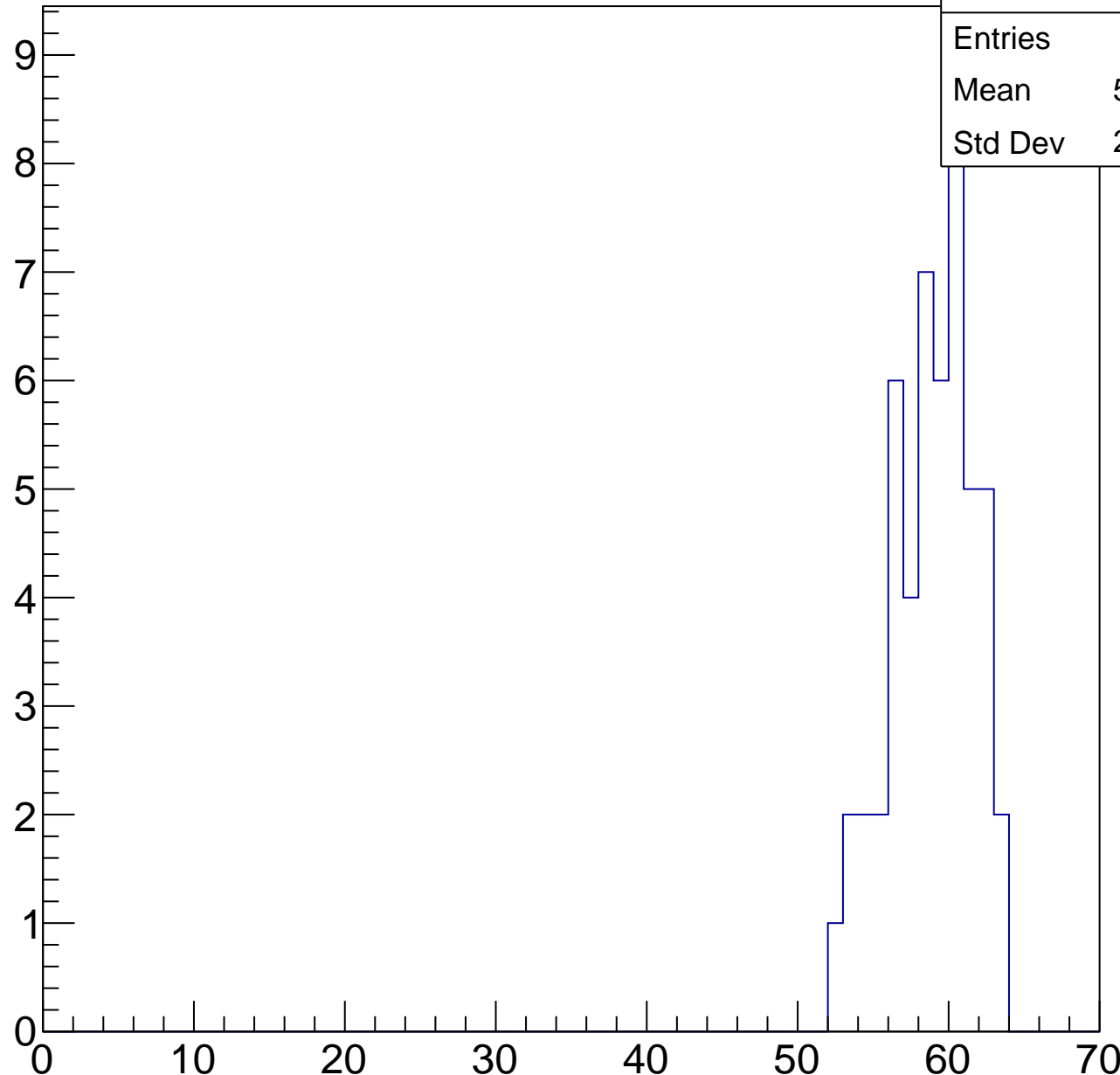
calib_packv5_041523_1651.root, FC#0, port C2

Entry

9
8
7
6
5
4
3
2
1
0

Entries	51
Mean	58.45
Std Dev	2.696

ampl

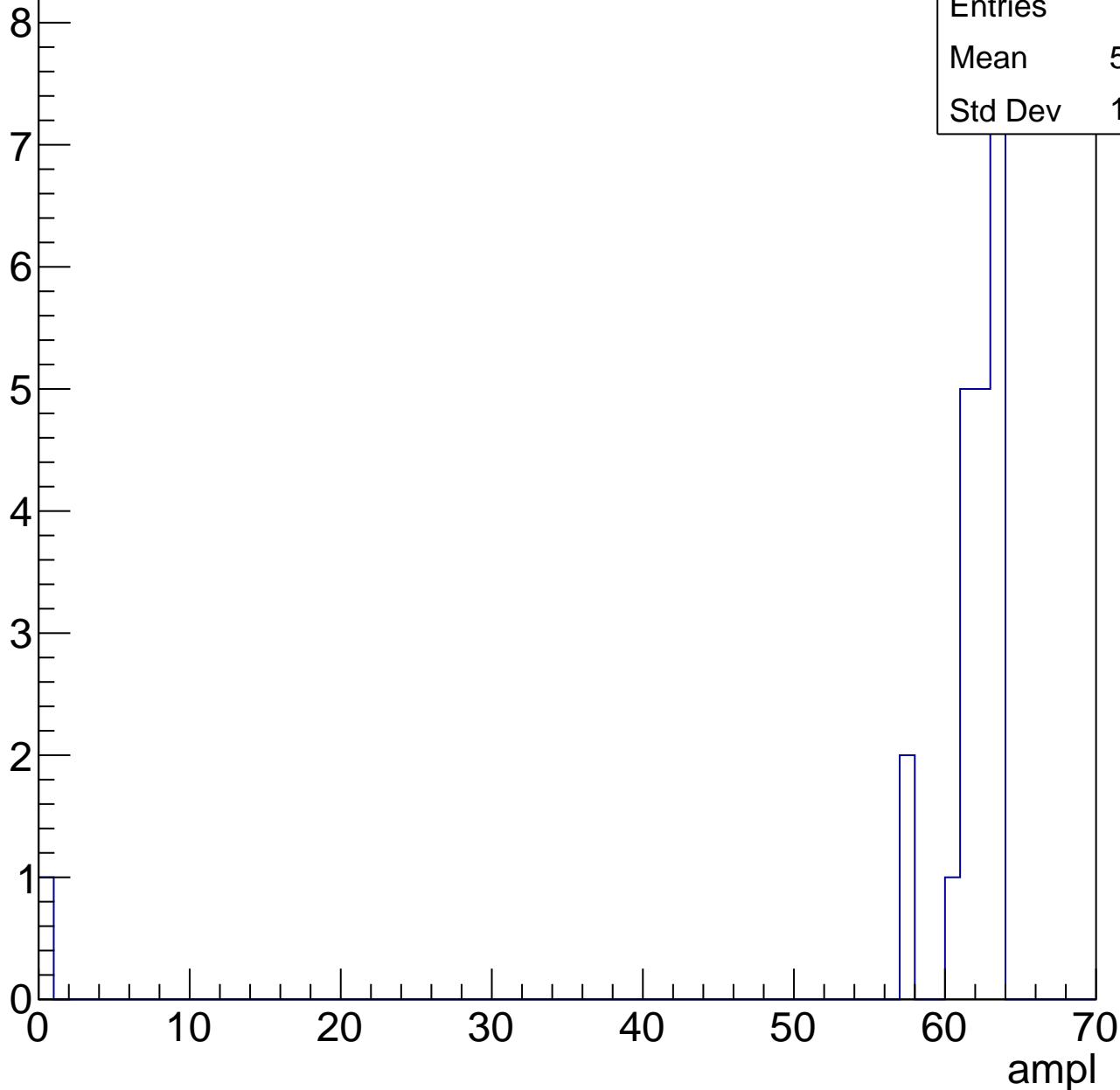


B1L103S, U5-ch109, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	22
Mean	58.77
Std Dev	12.94



B1L103S, U5-ch109, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



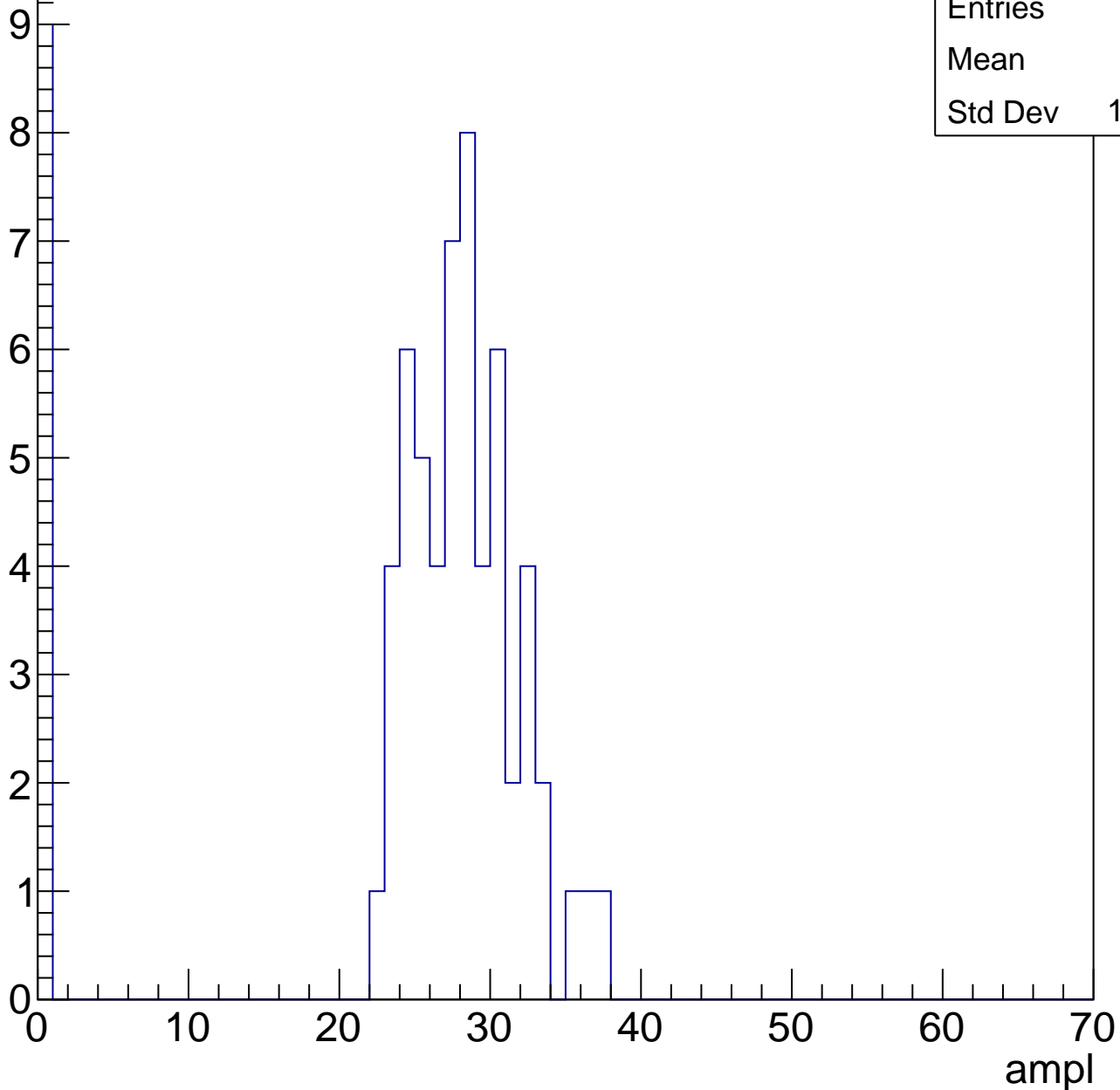
Entries	18
Mean	0
Std Dev	0

B1L103S, U5-ch110, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	24
Std Dev	10.13

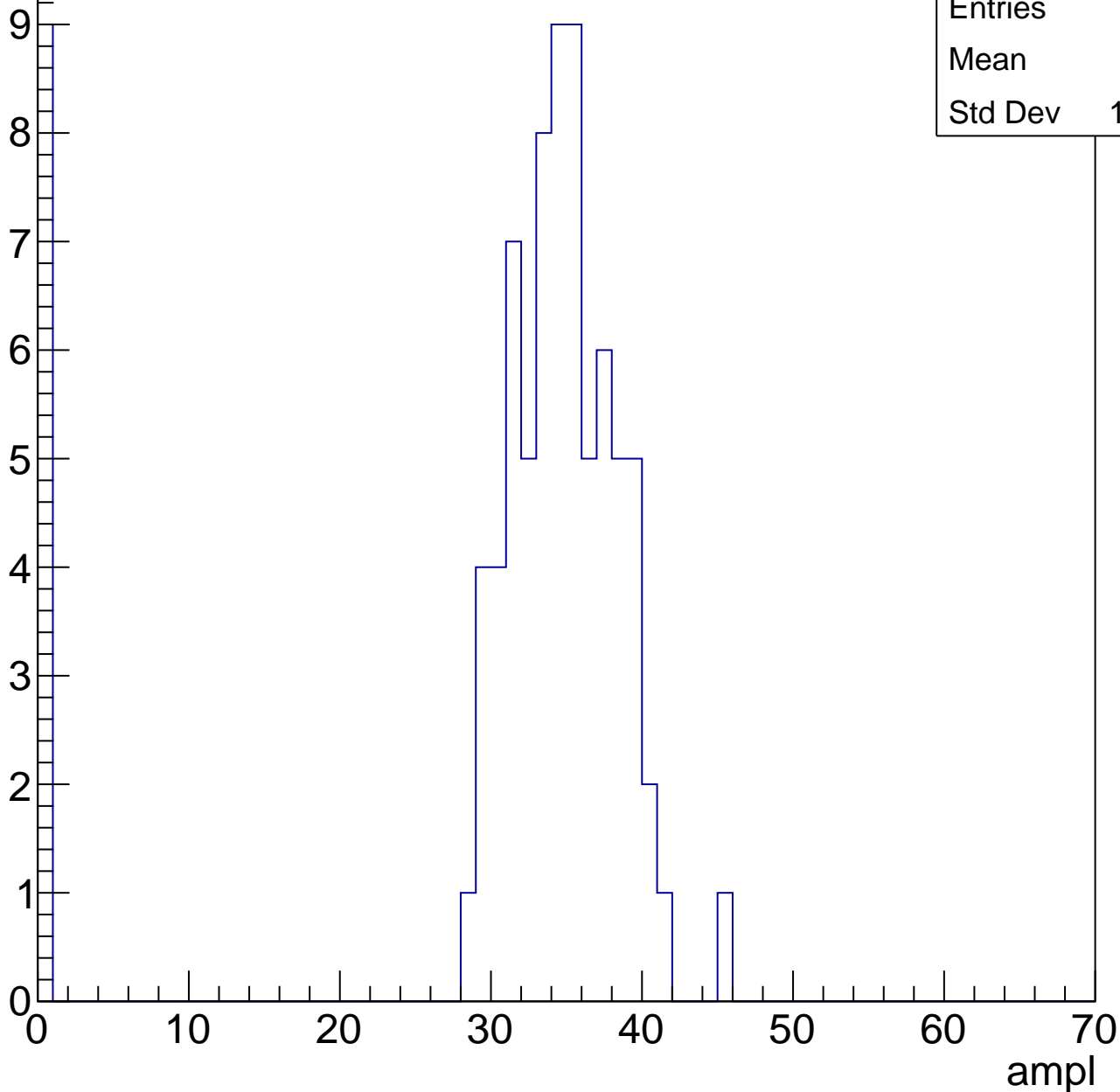


B1L103S, U5-ch110, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	81
Mean	30.6
Std Dev	11.27

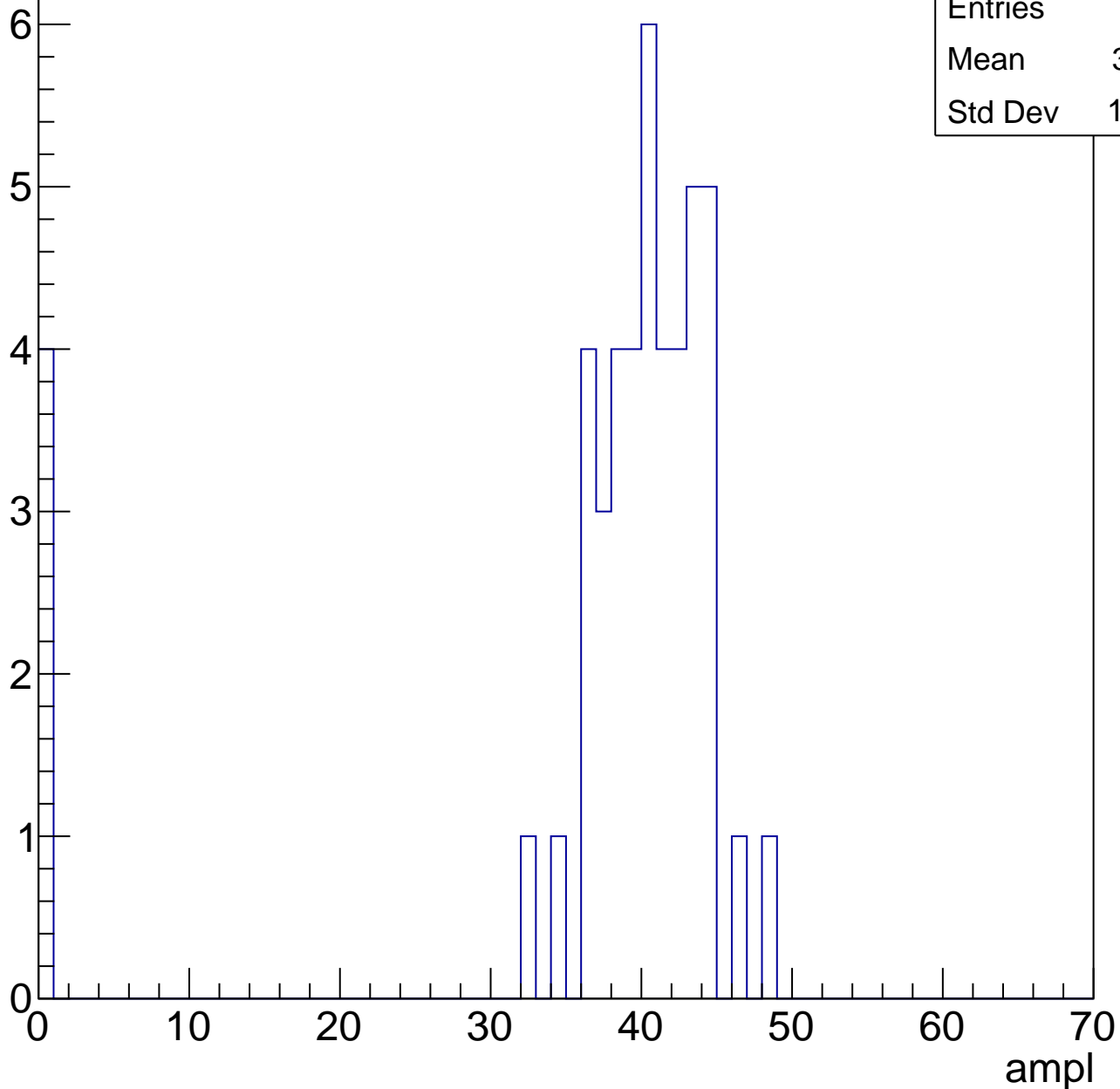


B1L103S, U5-ch110, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

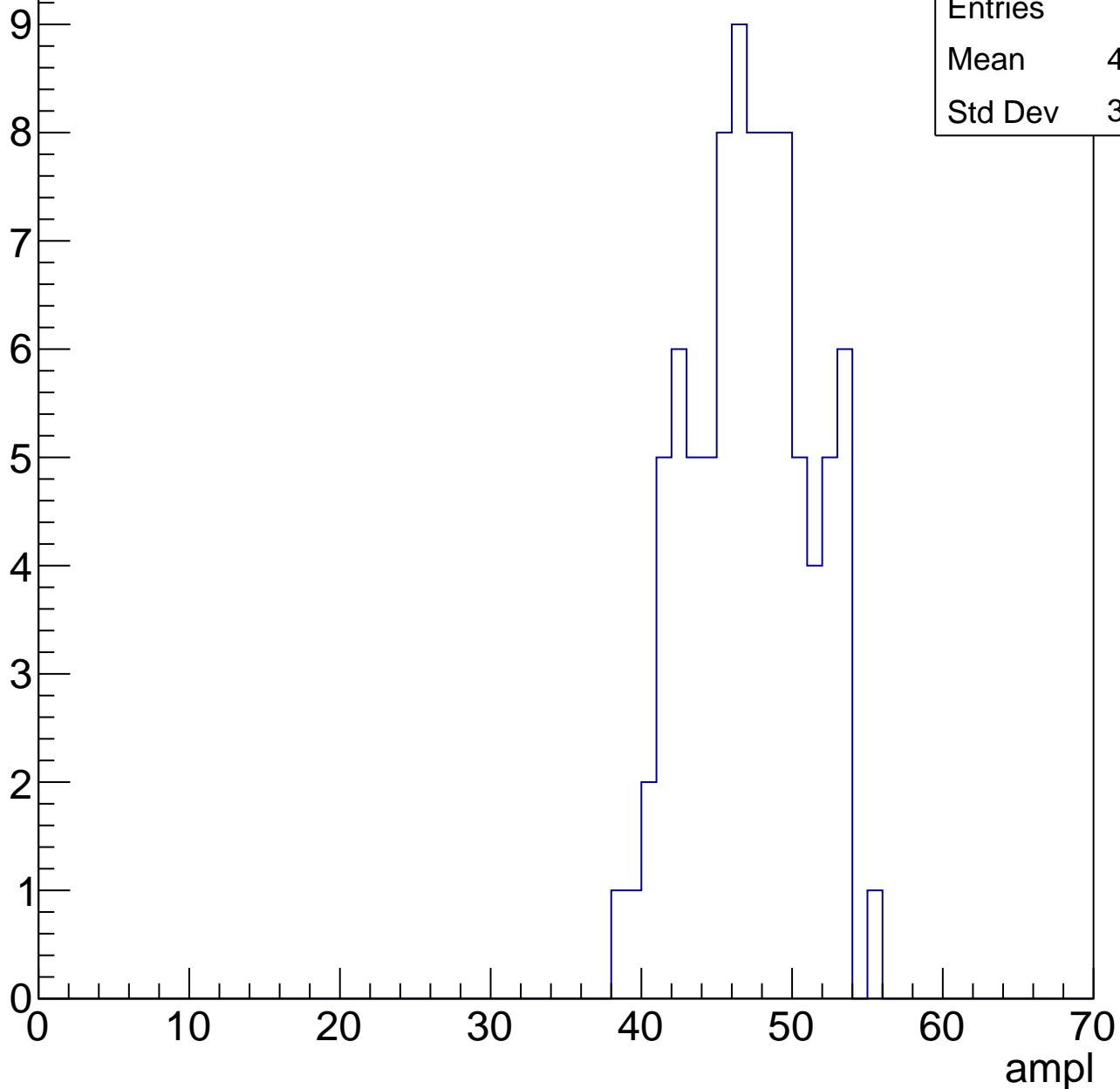
Entries	47
Mean	36.81
Std Dev	11.65



B1L103S, U5-ch110, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry



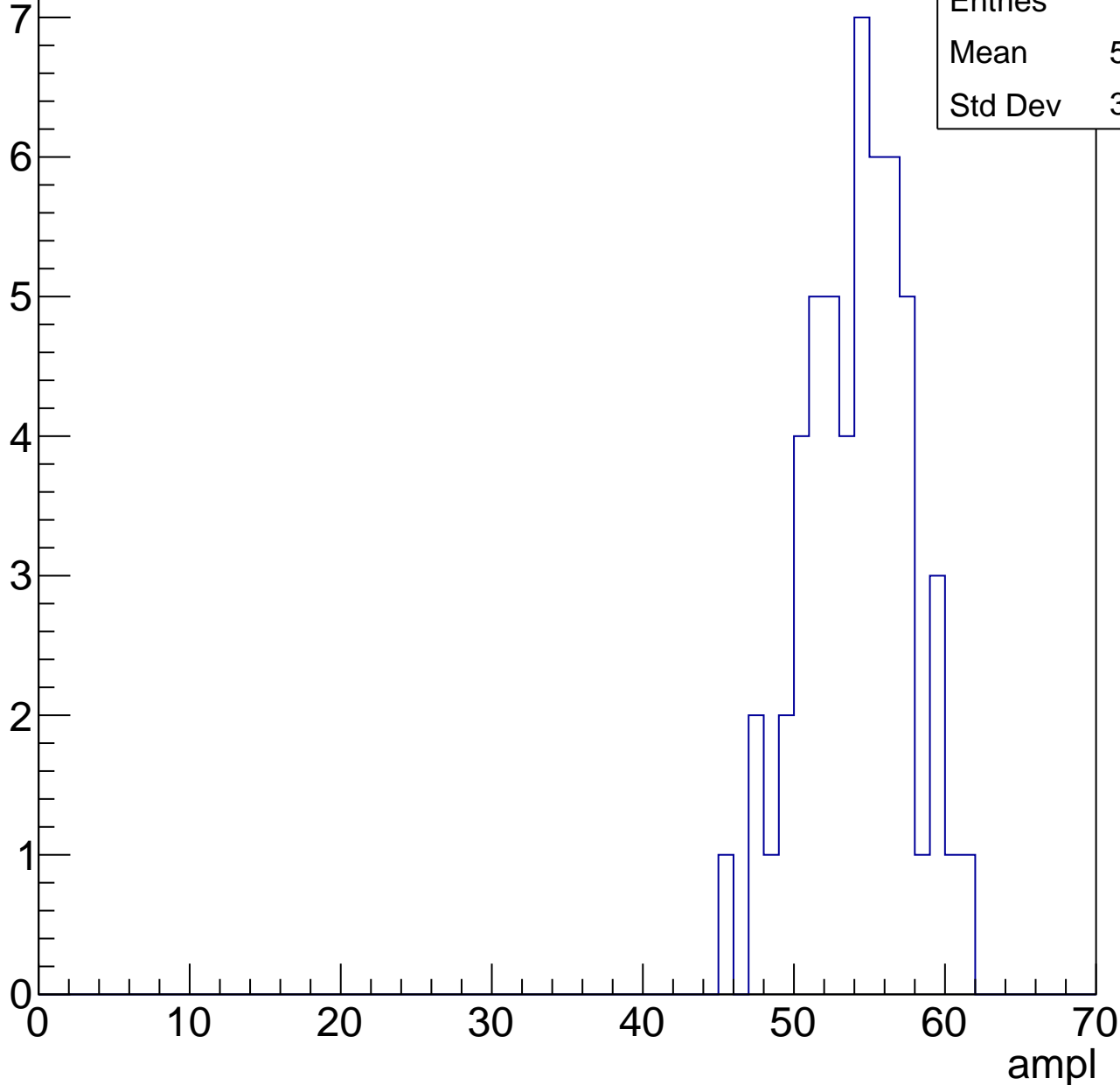
Entries	87
Mean	46.69
Std Dev	3.843

B1L103S, U5-ch110, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	53.65
Std Dev	3.449

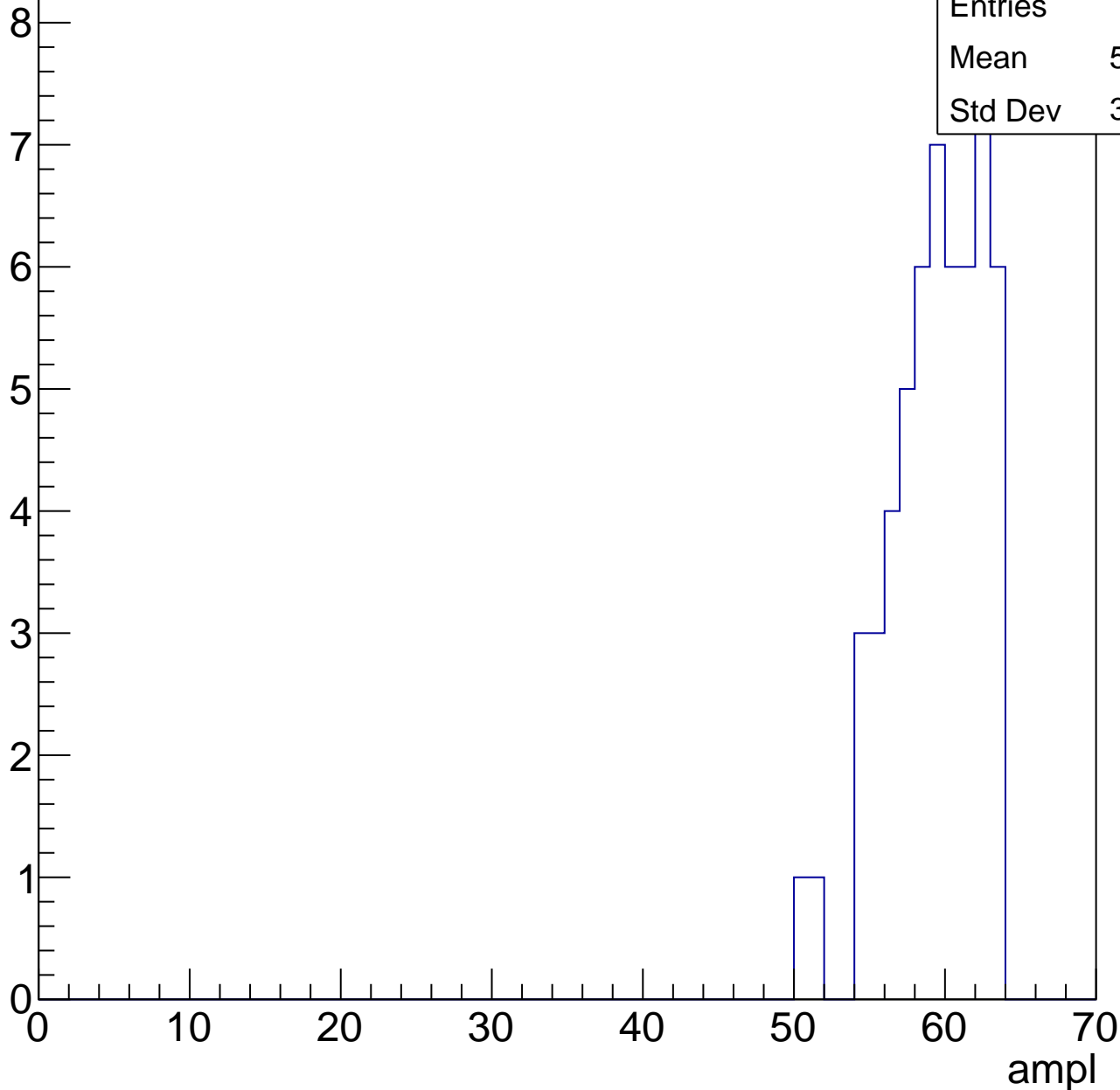


B1L103S, U5-ch110, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

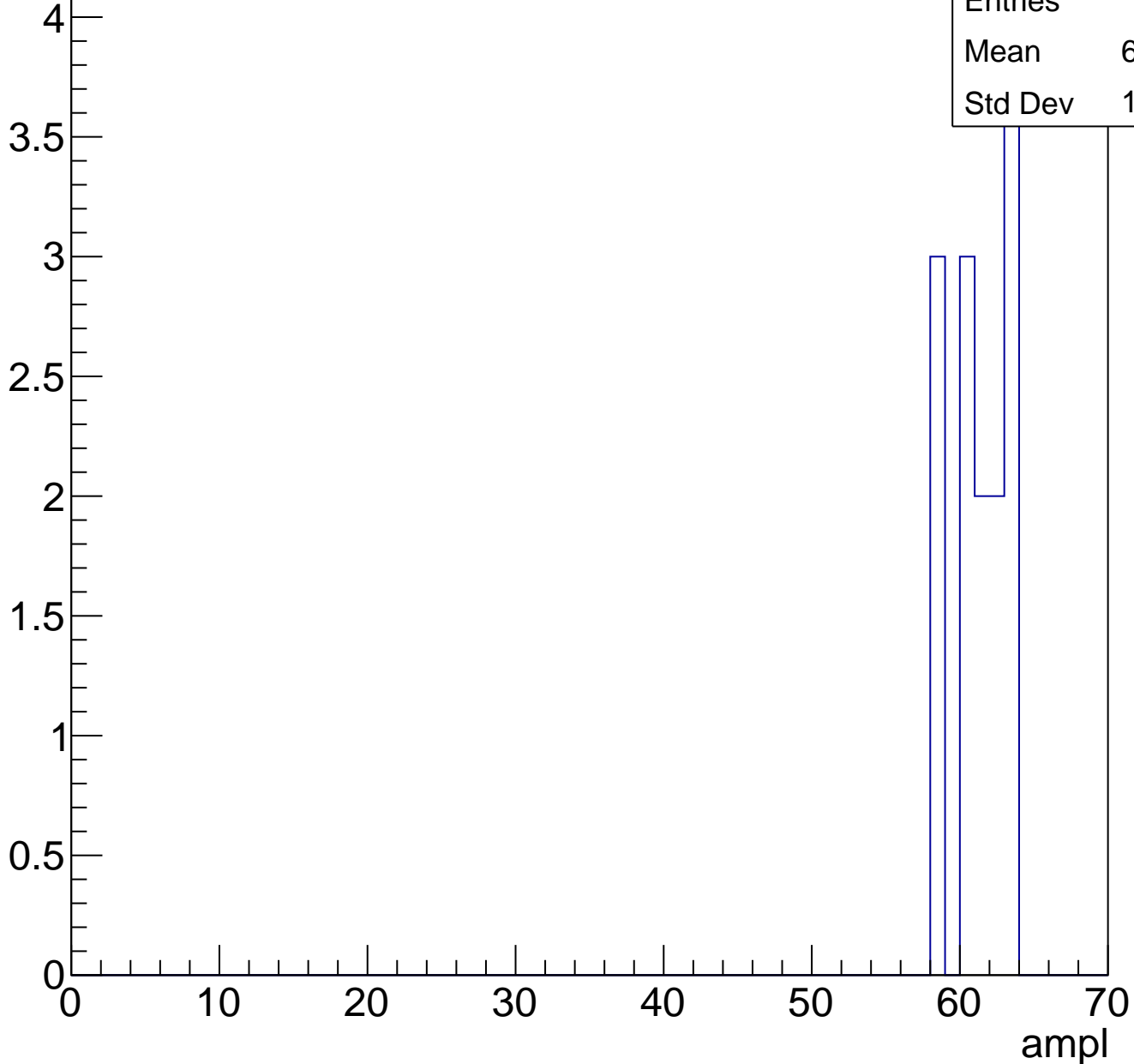
Entries	56
Mean	58.89
Std Dev	3.069



B1L103S, U5-ch110, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	14
Mean	60.86
Std Dev	1.846

B1L103S, U5-ch110, adc7

calib_packv5_041523_1651.root, FC#0, port C2

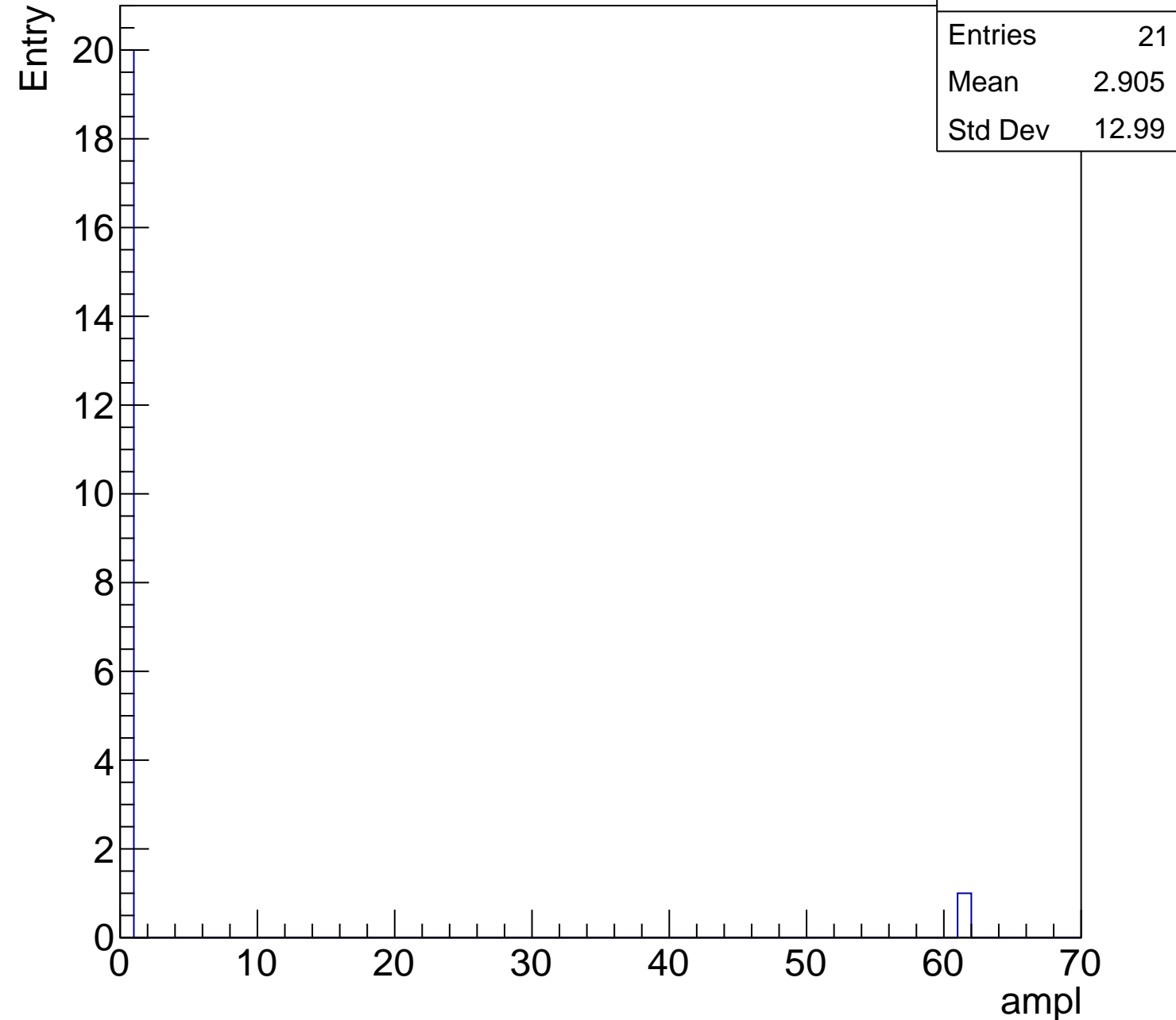
Entries	21
Mean	2.905
Std Dev	12.99

Entry

20
18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

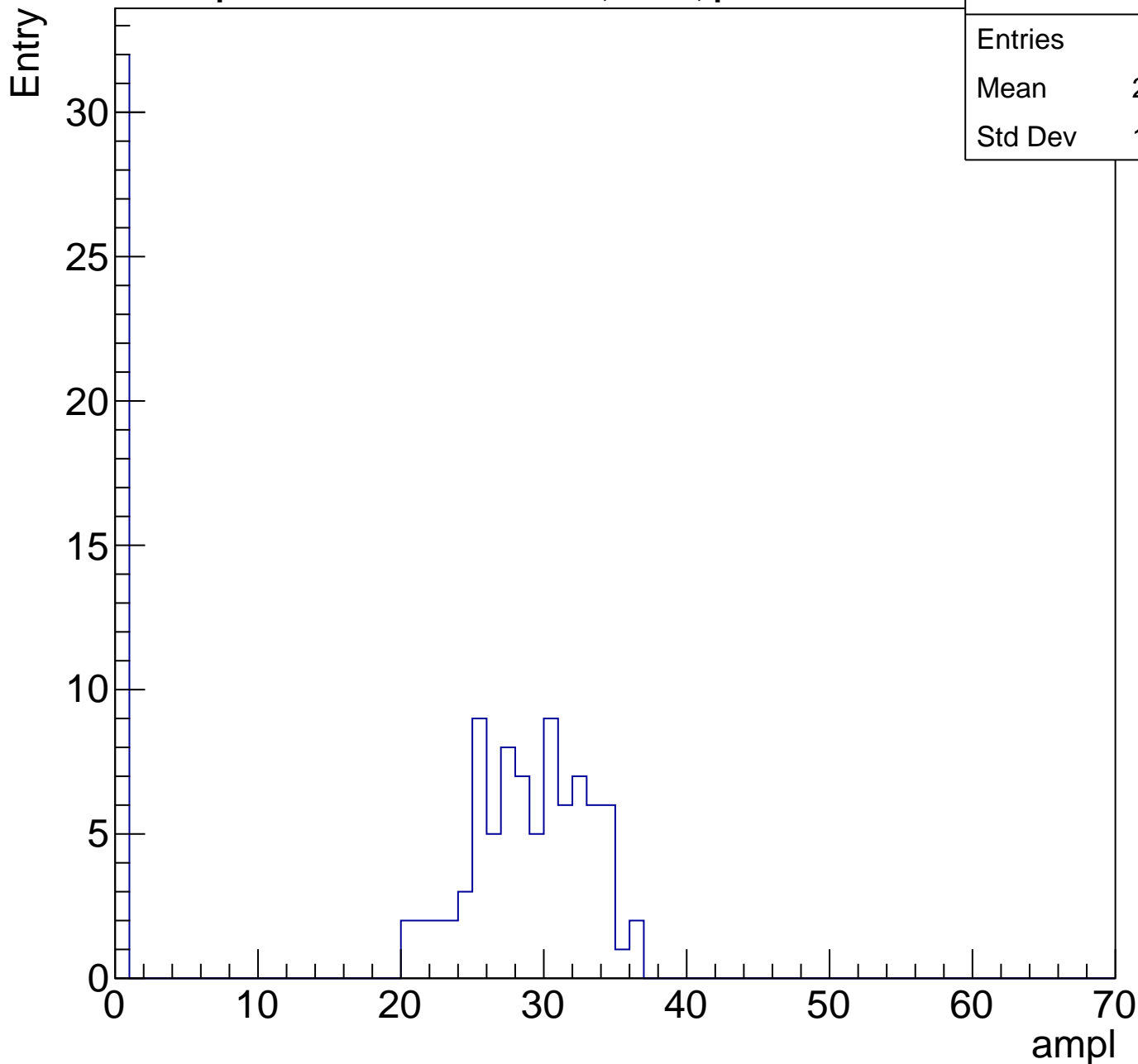
ampl



B1L103S, U5-ch111, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	114
Mean	20.57
Std Dev	13.26

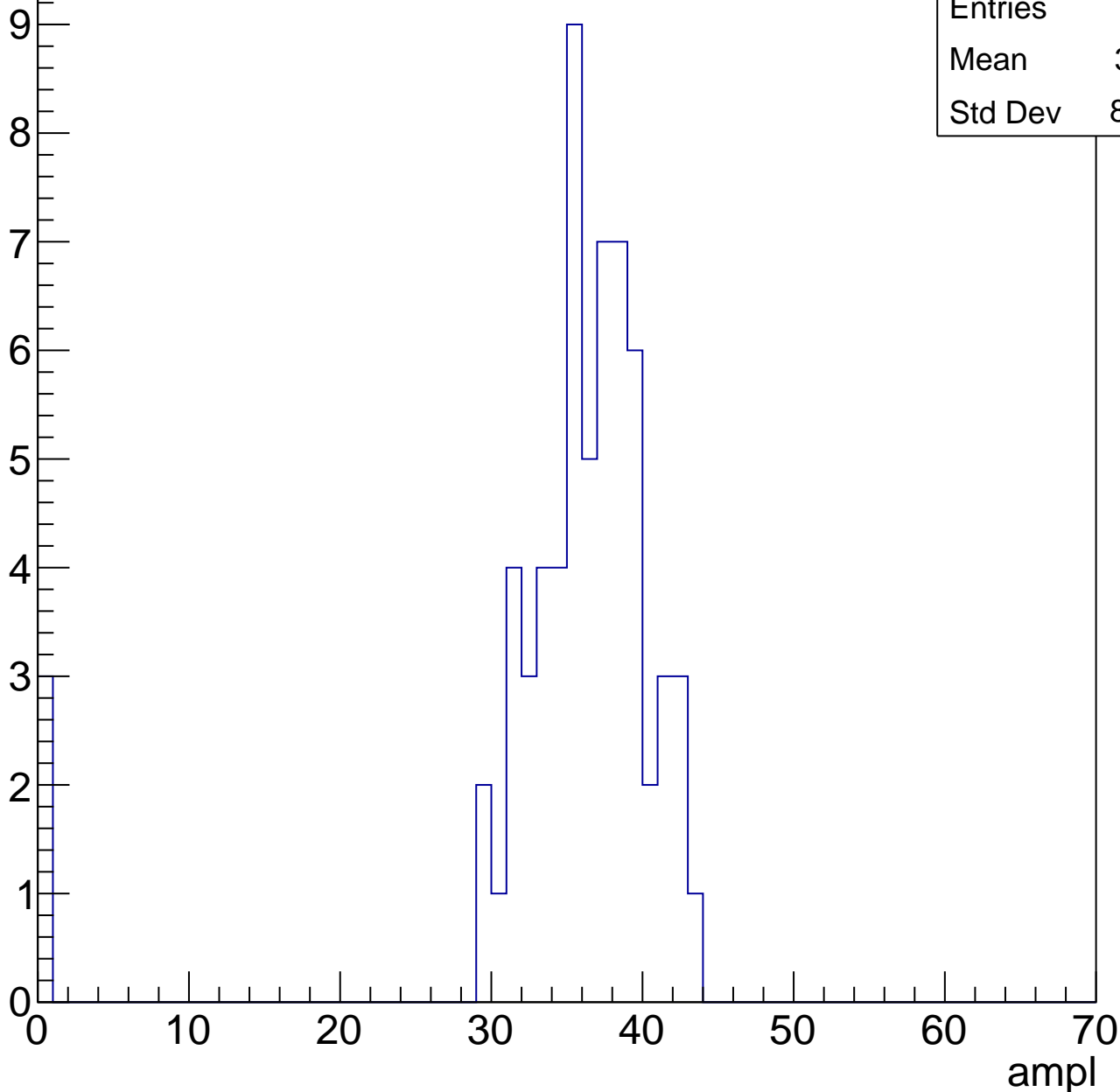


B1L103S, U5-ch111, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	34.41
Std Dev	8.312



B1L103S, U5-ch111, adc2

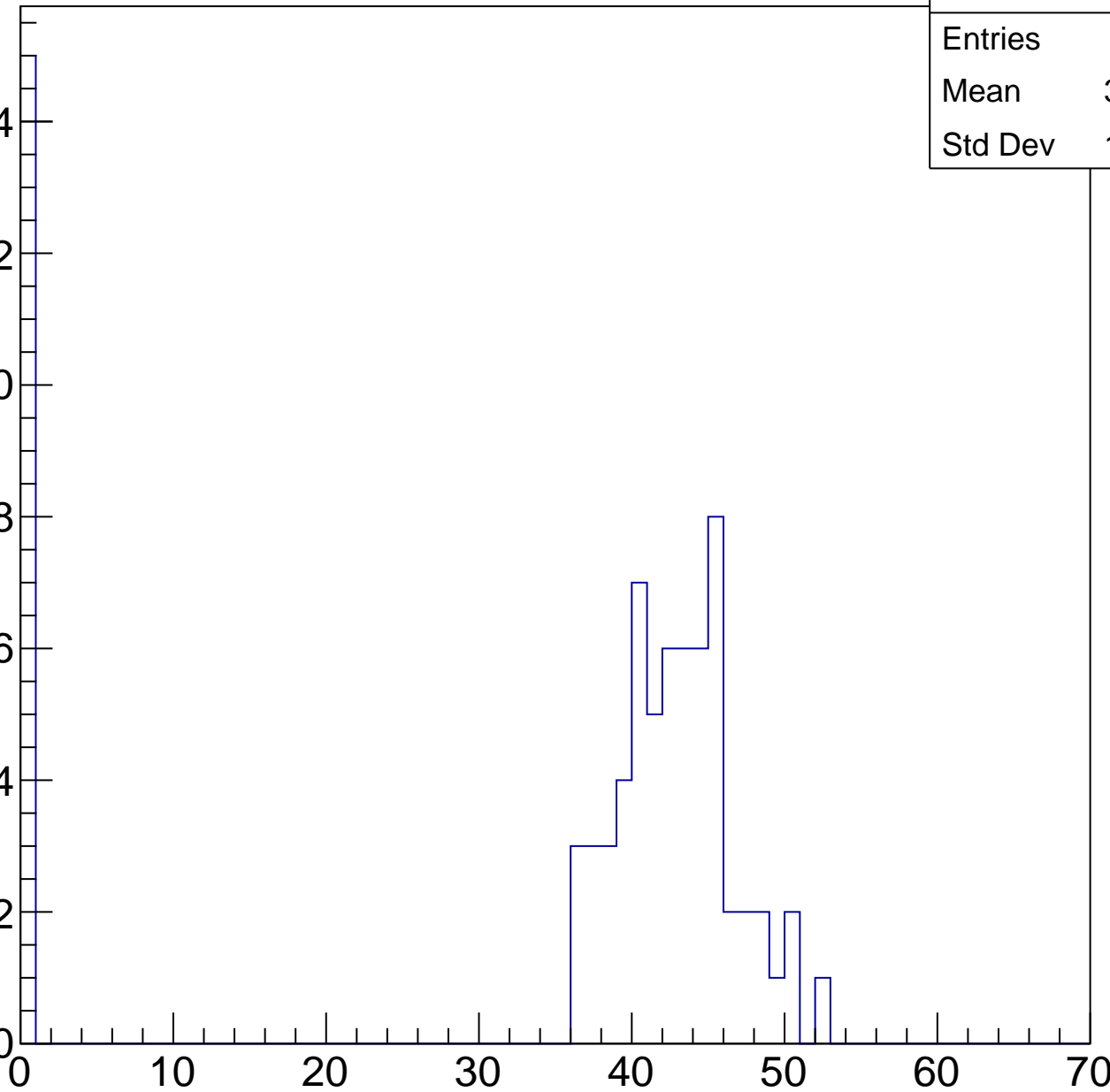
calib_packv5_041523_1651.root, FC#0, port C2

Entries	76
Mean	34.09
Std Dev	17.22

Entry

14
12
10
8
6
4
2
0

ampl

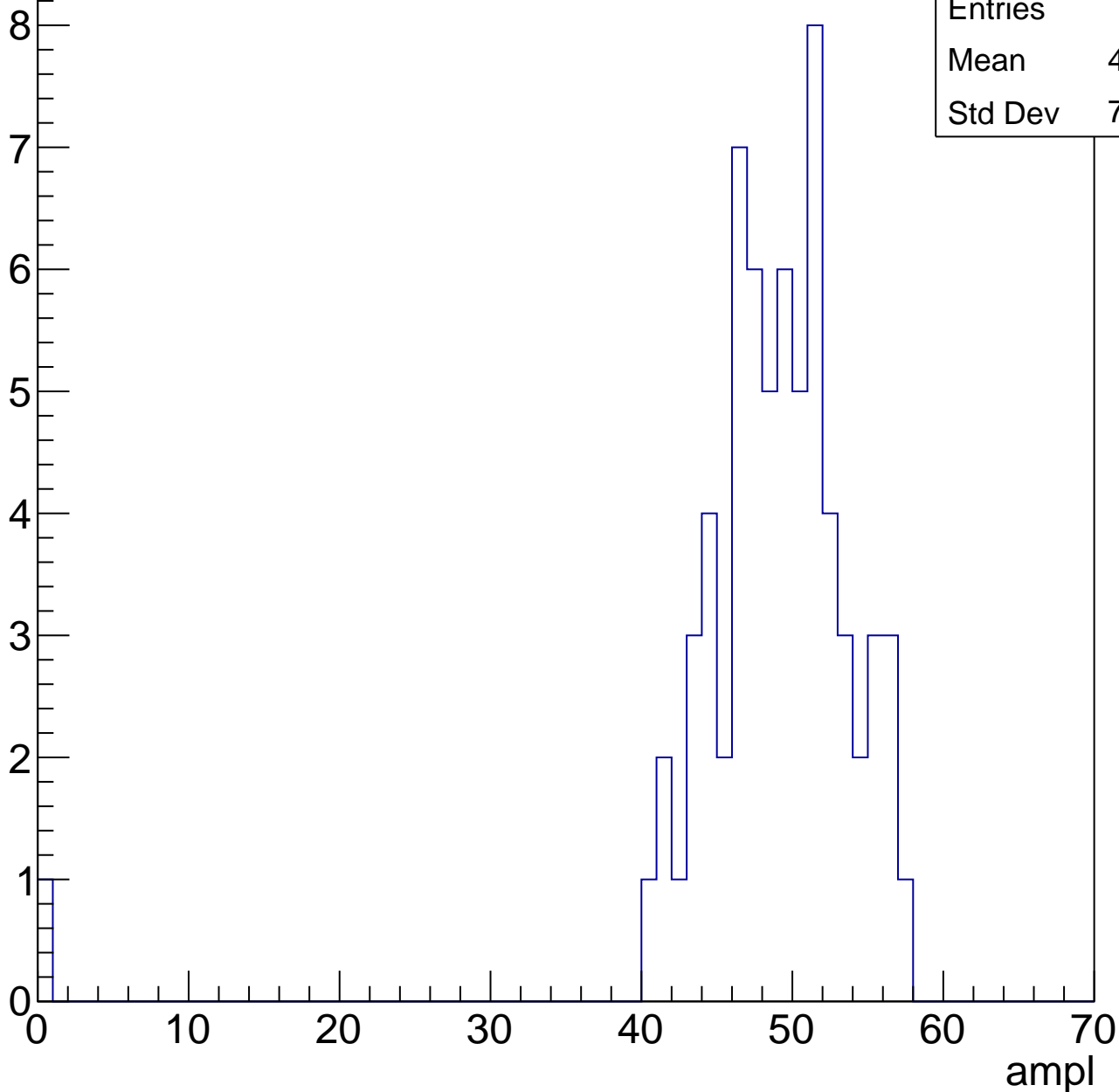


B1L103S, U5-ch111, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	48.06
Std Dev	7.146

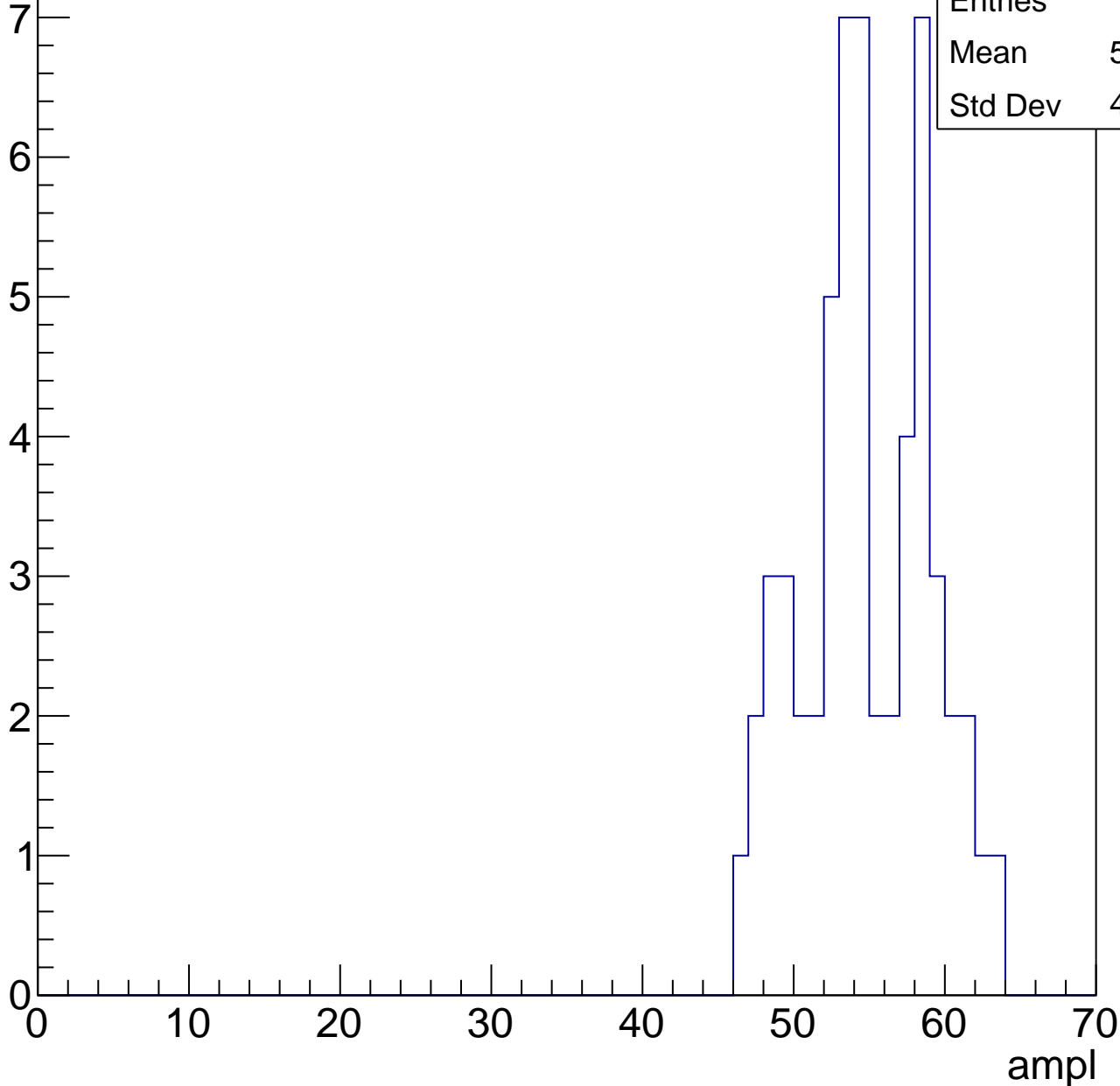


B1L103S, U5-ch111, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	54.32
Std Dev	4.149

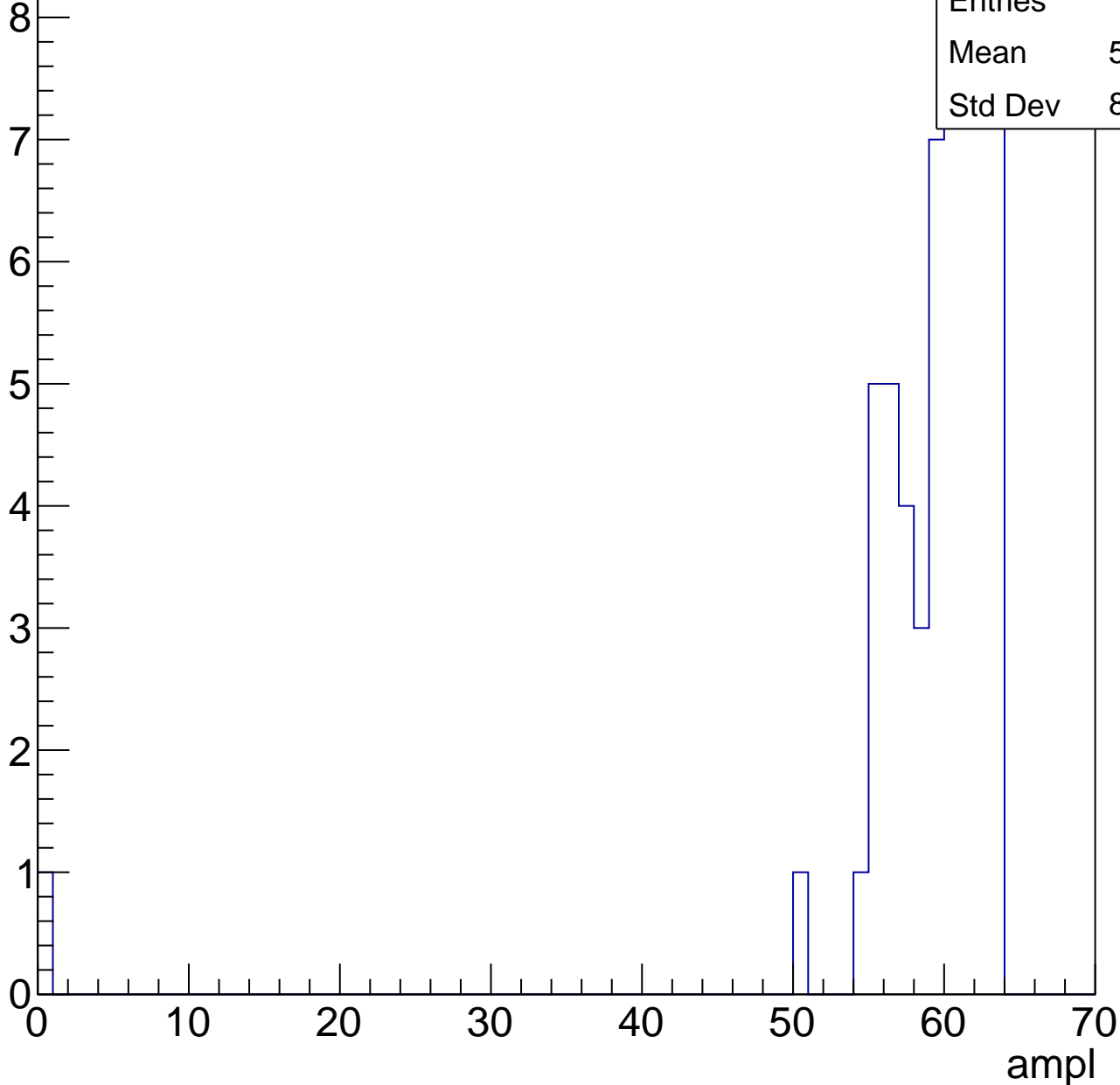


B1L103S, U5-ch111, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

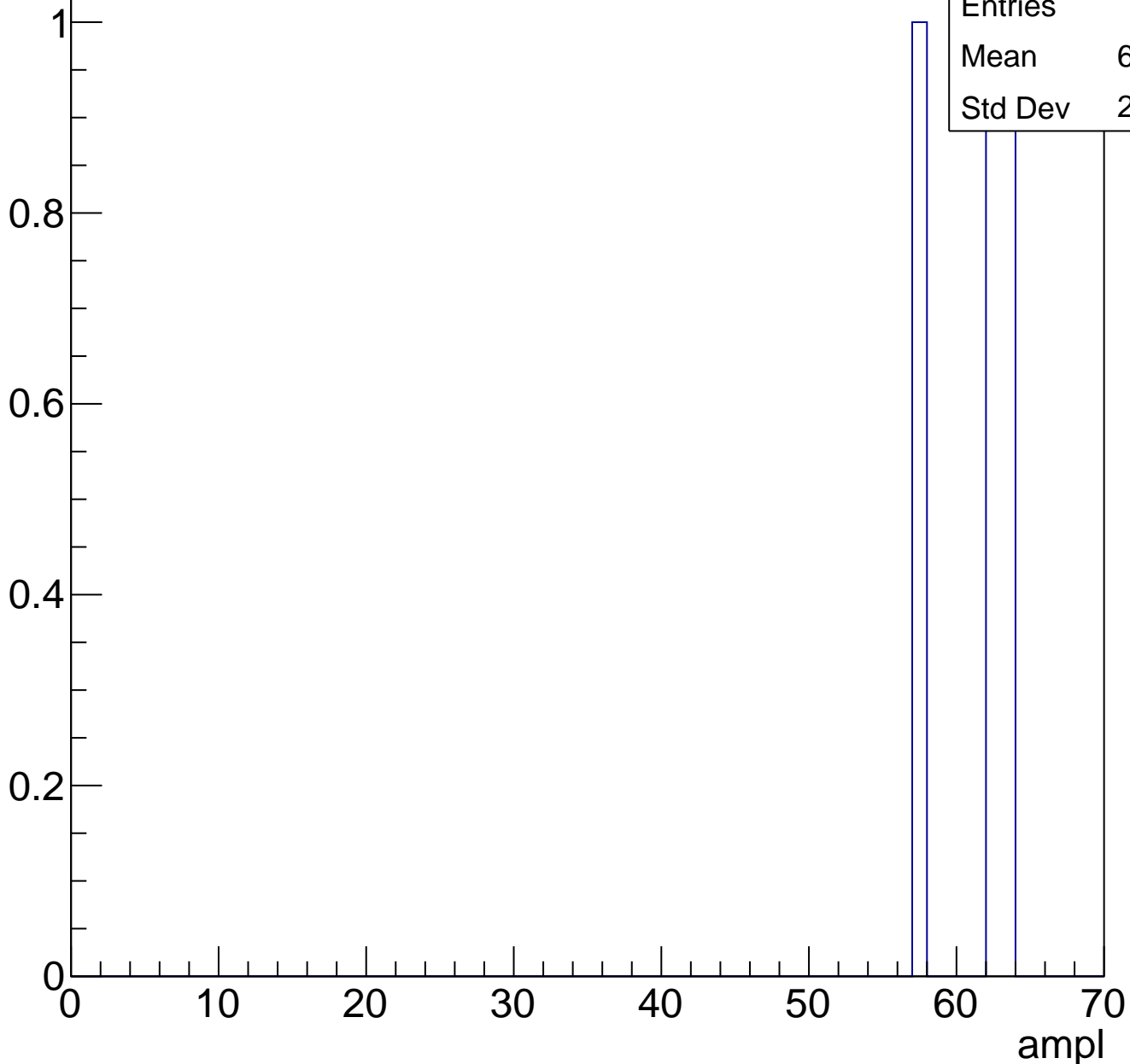
Entries	59
Mean	58.34
Std Dev	8.177



B1L103S, U5-ch111, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch111, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

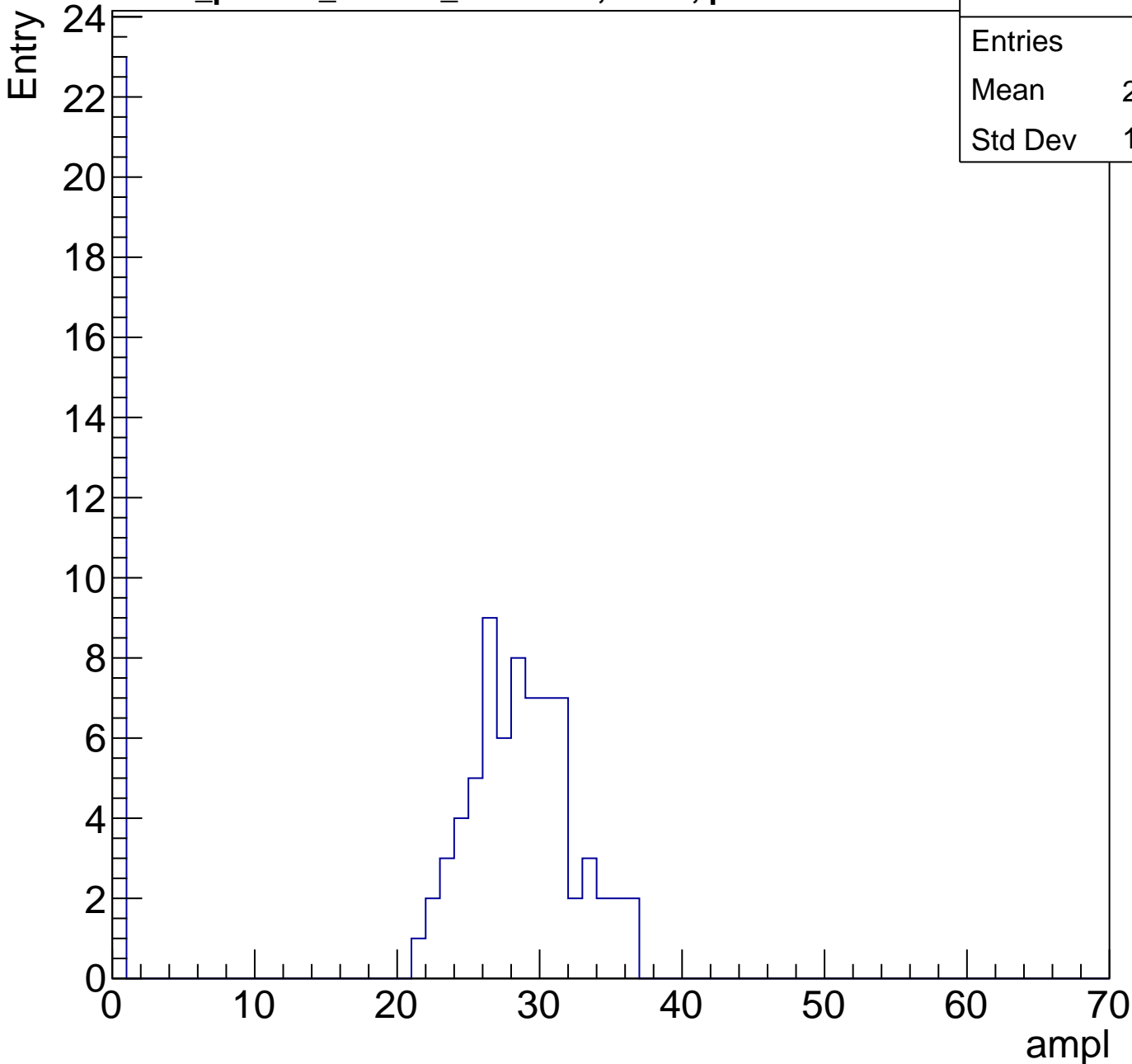
ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U5-ch112, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	93
Mean	21.27
Std Dev	12.56

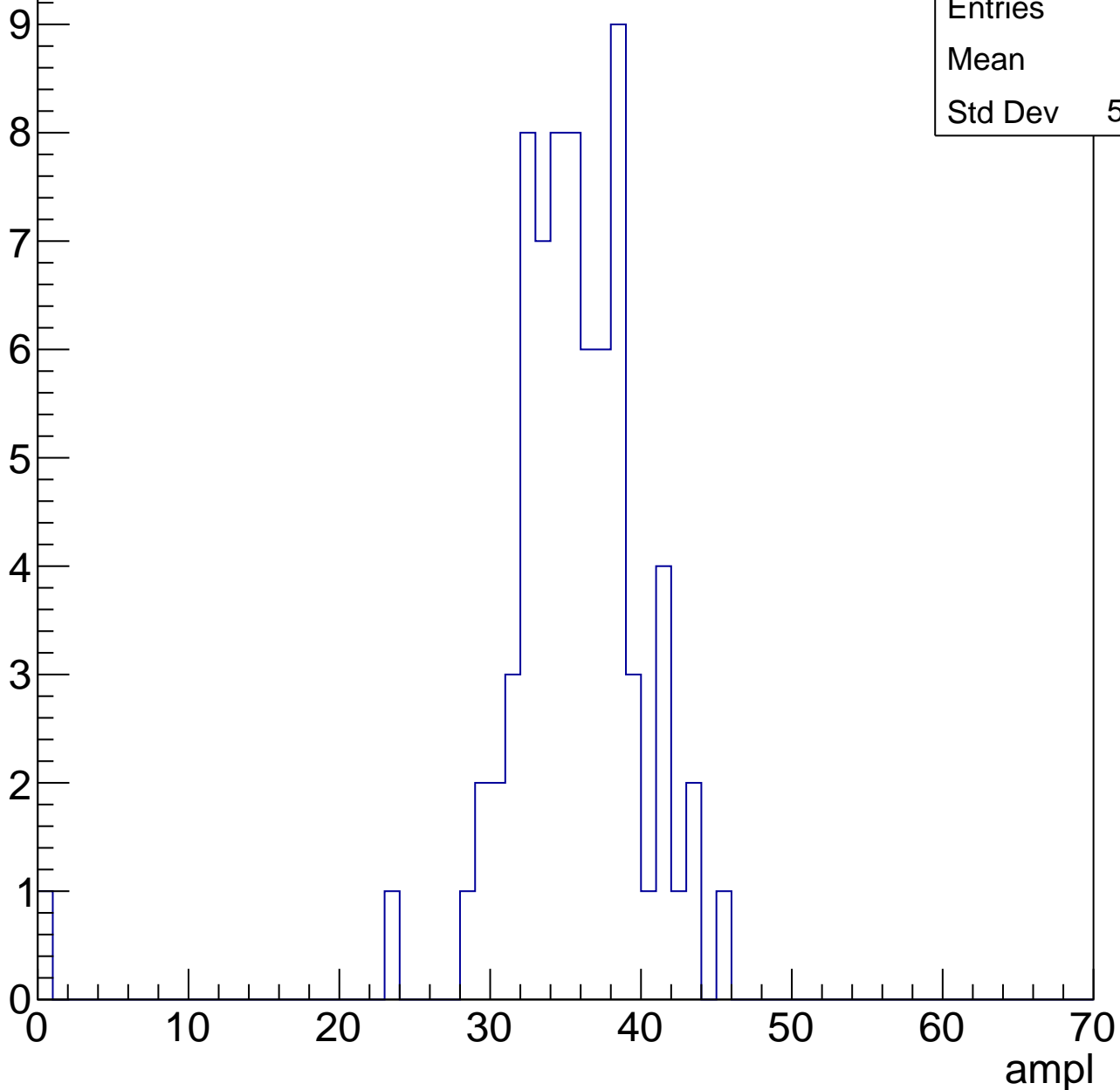


B1L103S, U5-ch112, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	34.8
Std Dev	5.573



B1L103S, U5-ch112, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	62
Mean	33.9
Std Dev	15.92

Entry

10

8

6

4

2

0

0

10

20

30

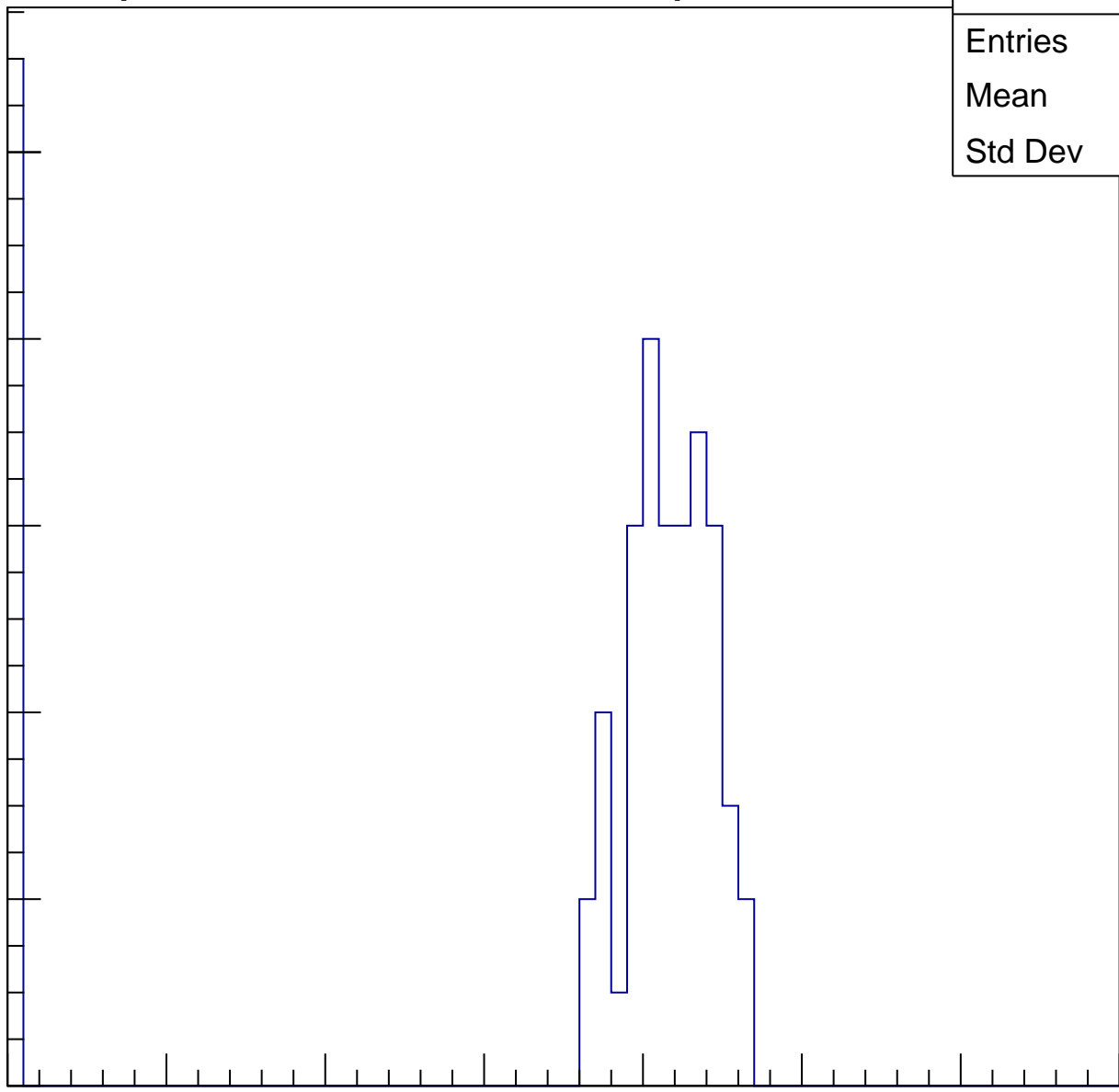
40

50

60

70

ampl



B1L103S, U5-ch112, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	77
Mean	46.75
Std Dev	8.331

Entry

10

8

6

4

2

0

0

10

20

30

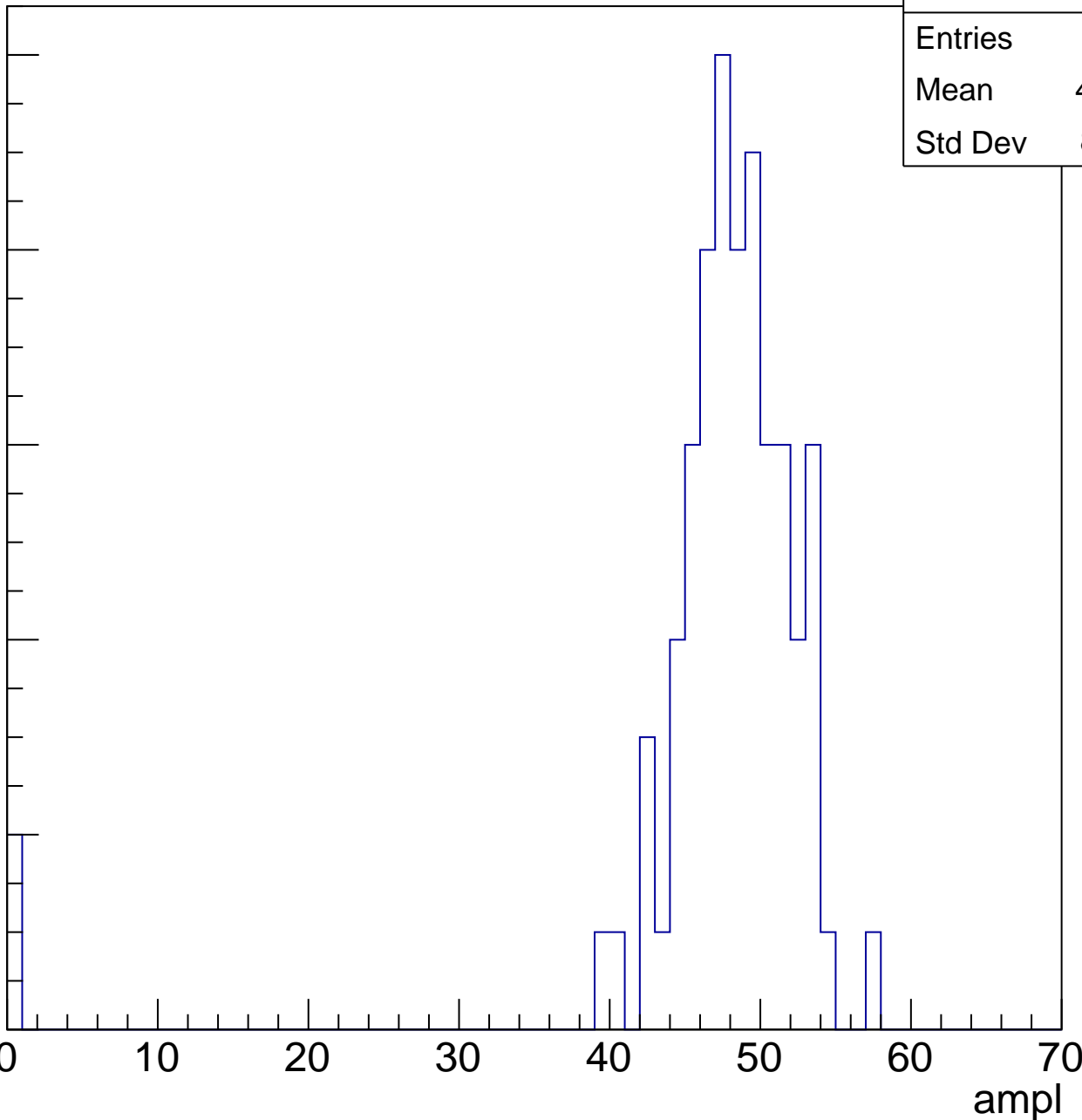
40

50

60

70

ampl

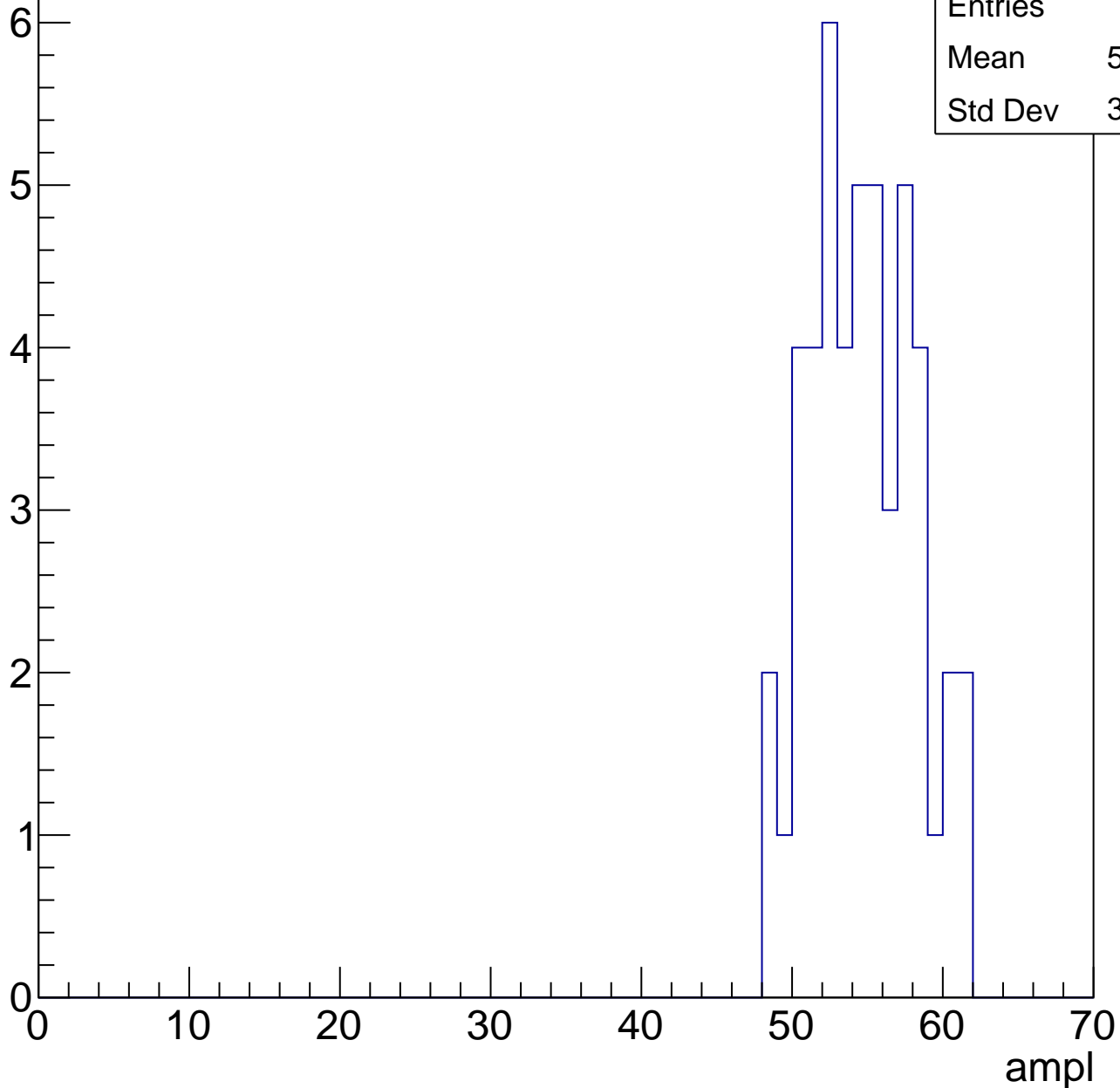


B1L103S, U5-ch112, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	48
Mean	54.25
Std Dev	3.363

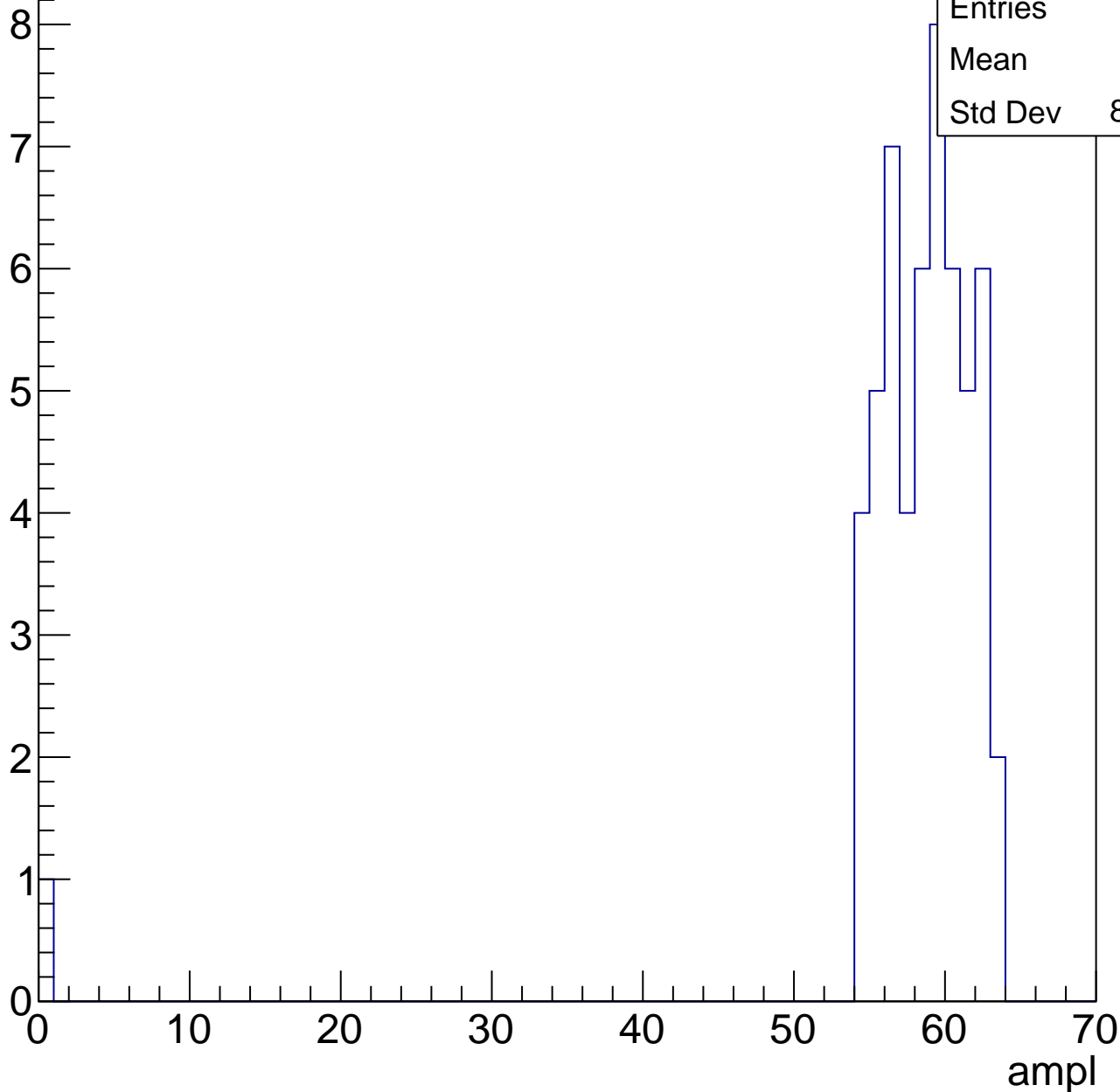


B1L103S, U5-ch112, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	57.3
Std Dev	8.279

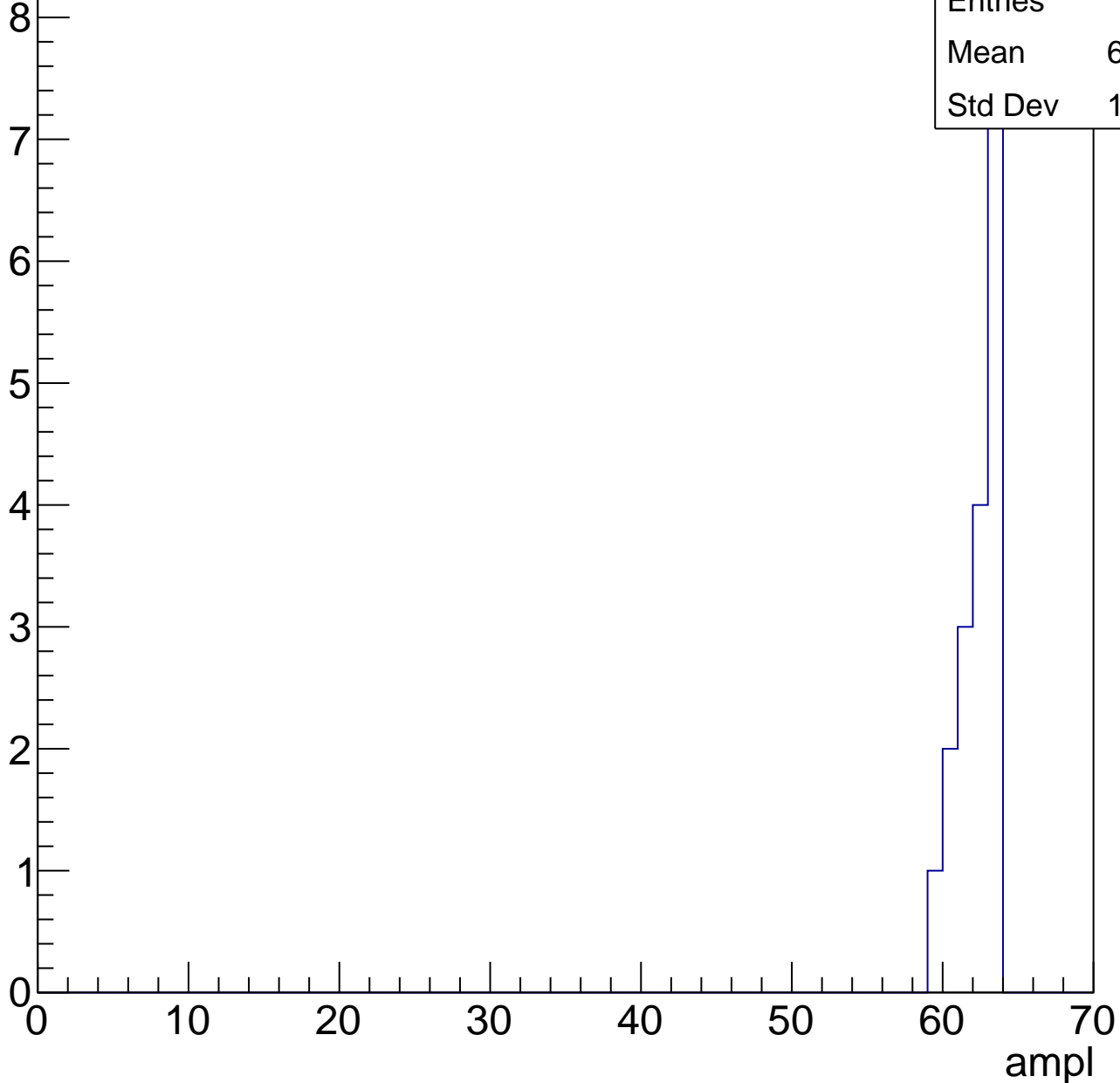


B1L103S, U5-ch112, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	18
Mean	61.89
Std Dev	1.242

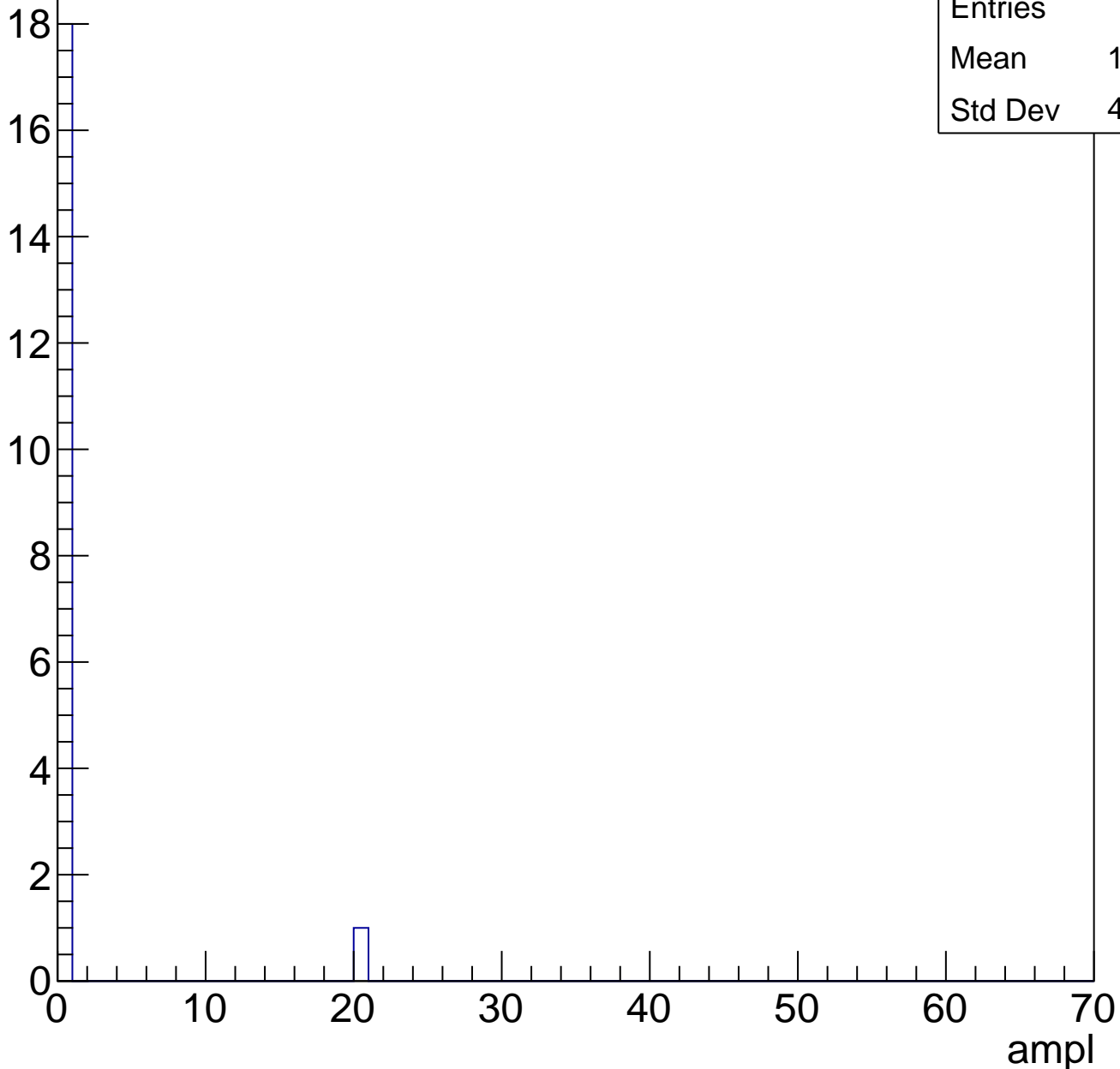


B1L103S, U5-ch112, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.053
Std Dev	4.466

Entry



B1L103S, U5-ch113, adc0

calib_packv5_041523_1651.root, FC#0, port C2

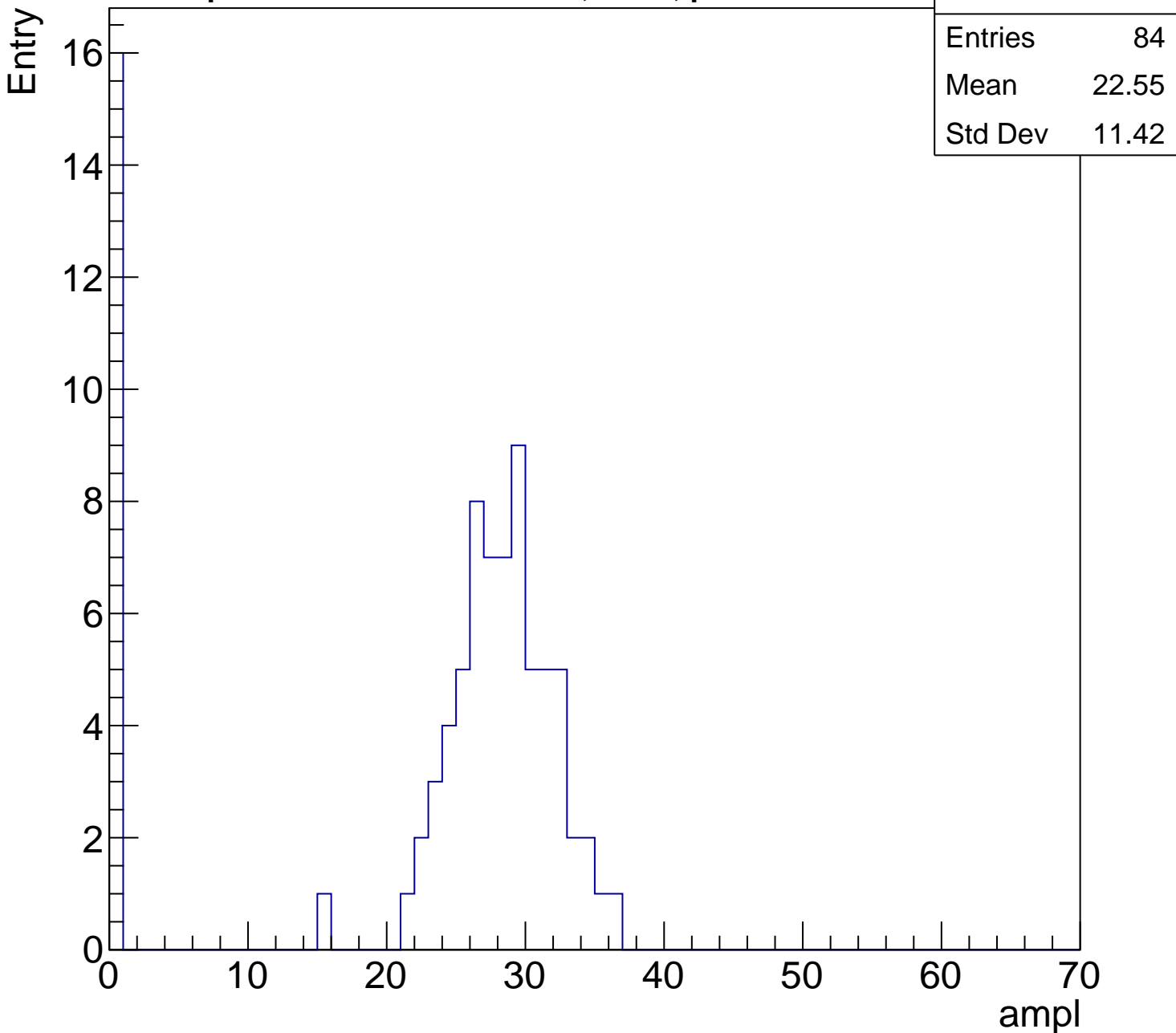
Entries	84
Mean	22.55
Std Dev	11.42

Entry

16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

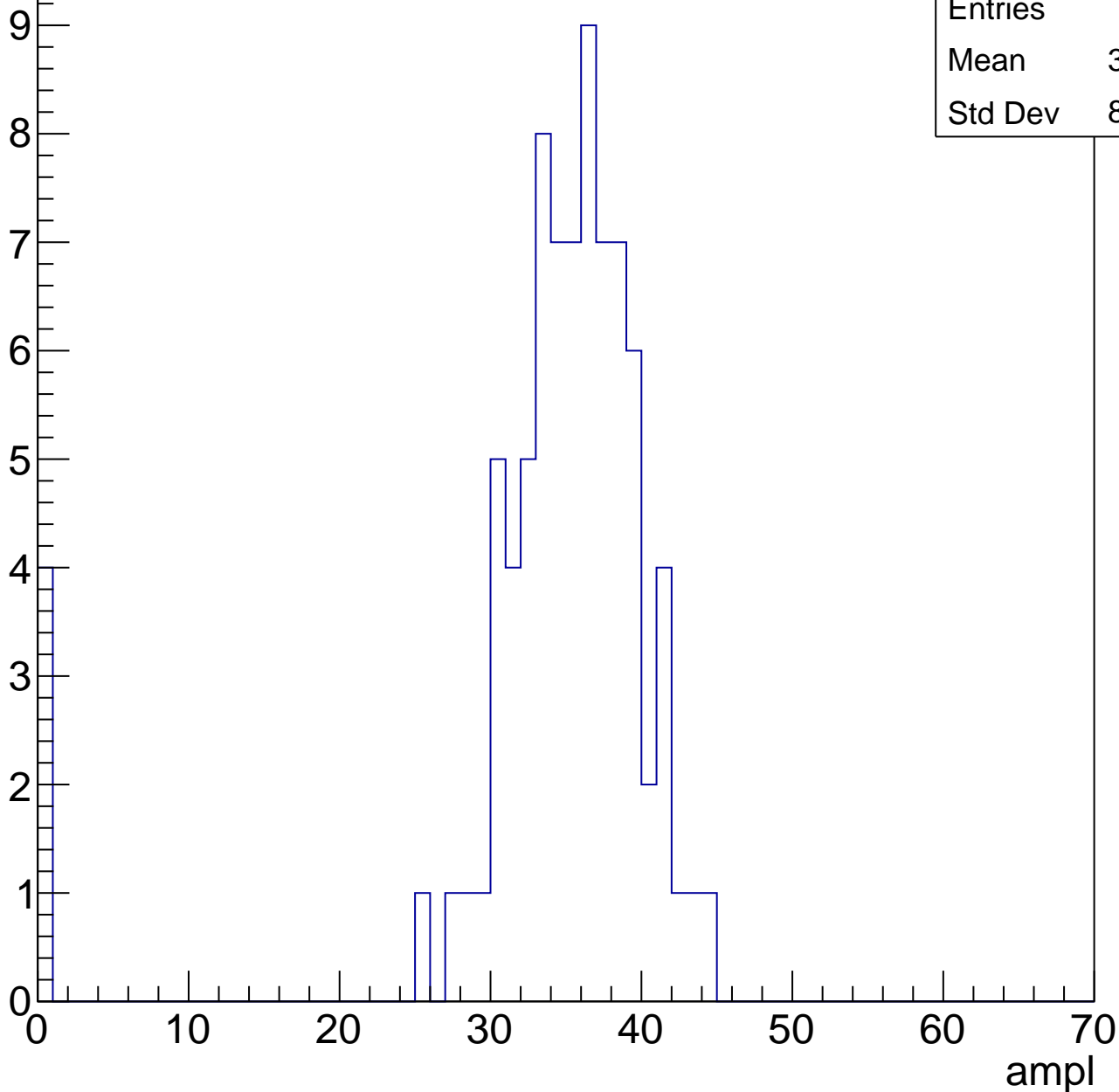


B1L103S, U5-ch113, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	82
Mean	33.49
Std Dev	8.424



B1L103S, U5-ch113, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	71
Mean	34.51
Std Dev	16.71

Entry

12

10

8

6

4

2

0

0

10

20

30

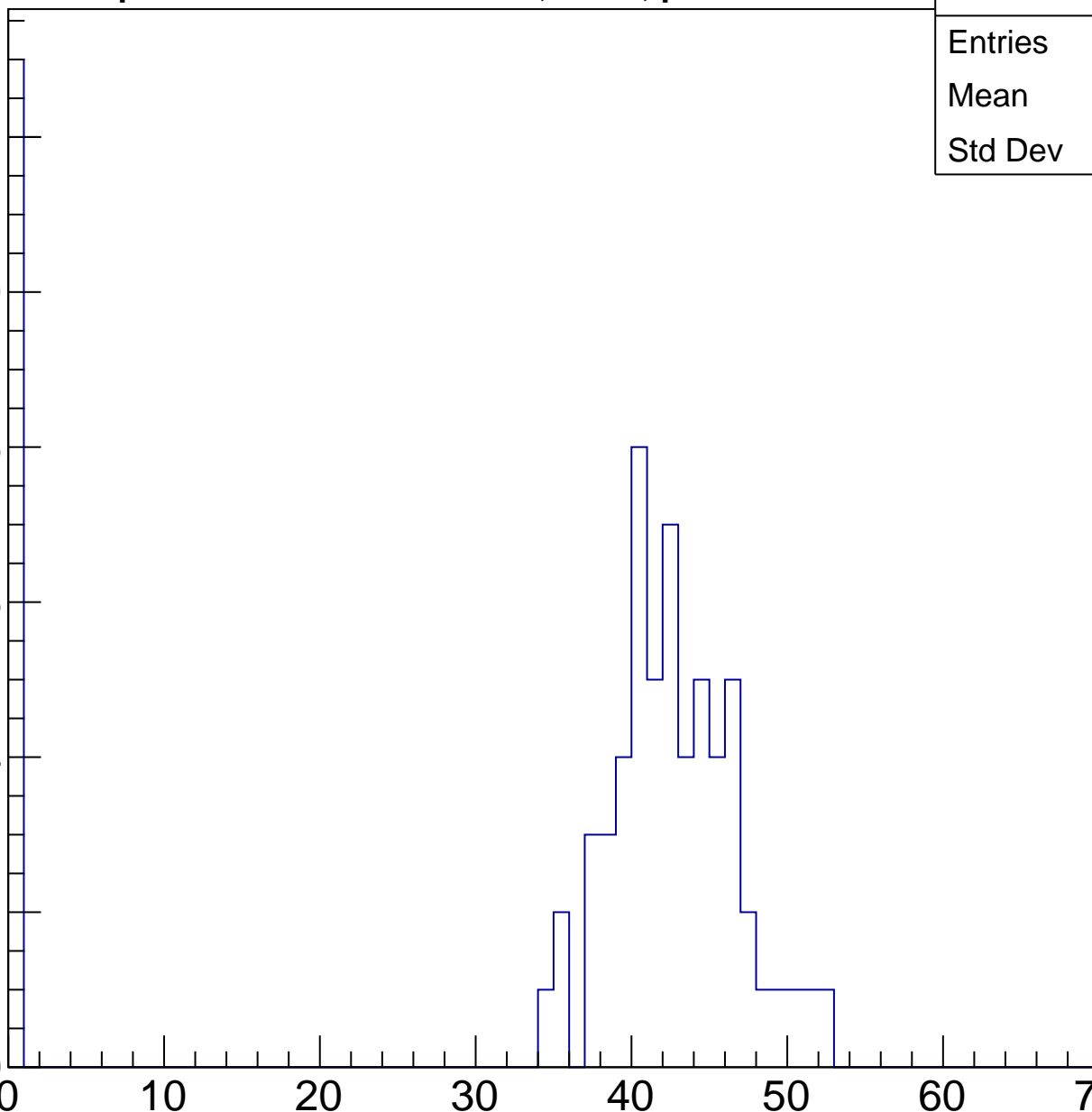
40

50

60

70

ampl

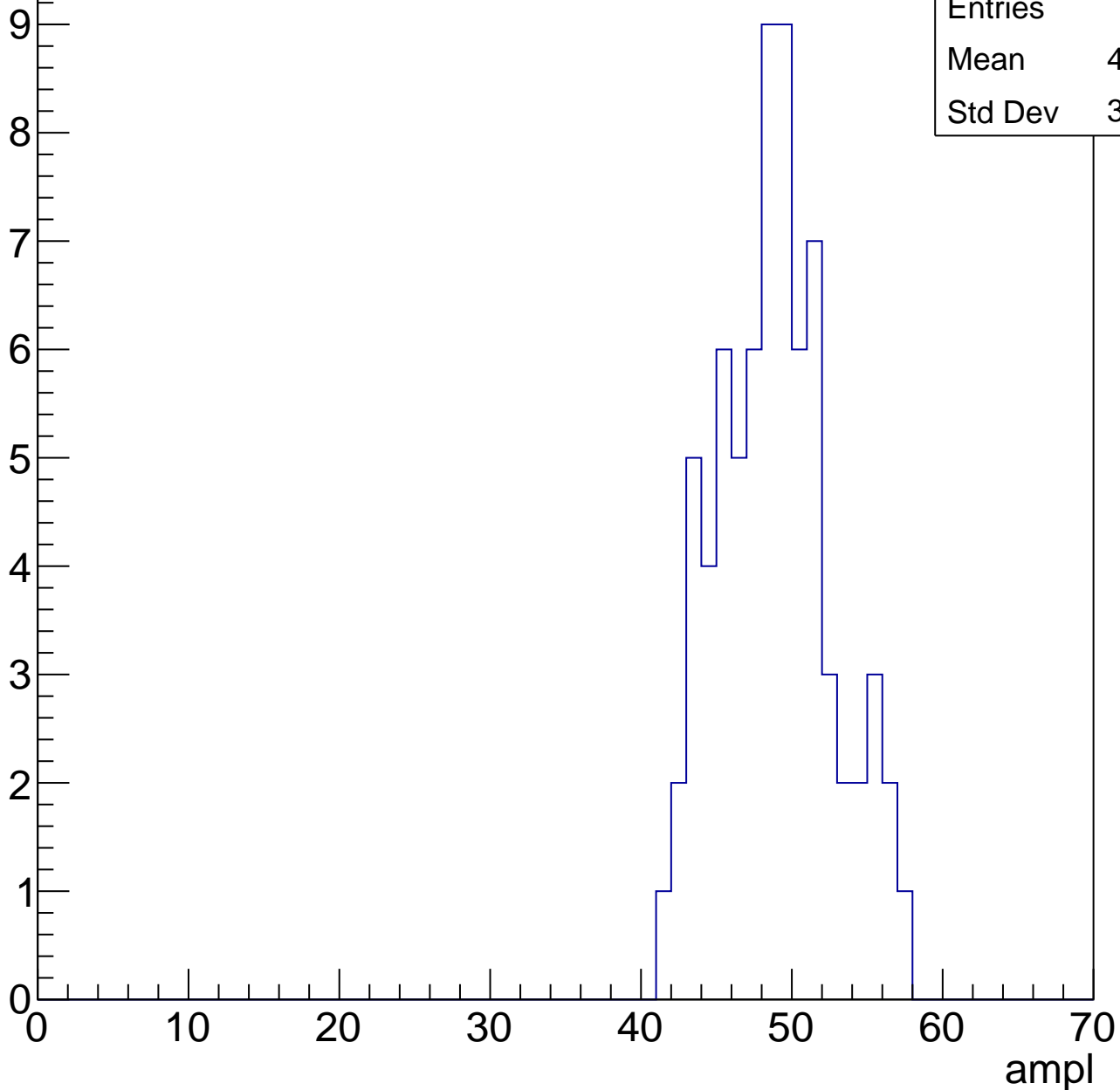


B1L103S, U5-ch113, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	48.38
Std Dev	3.703

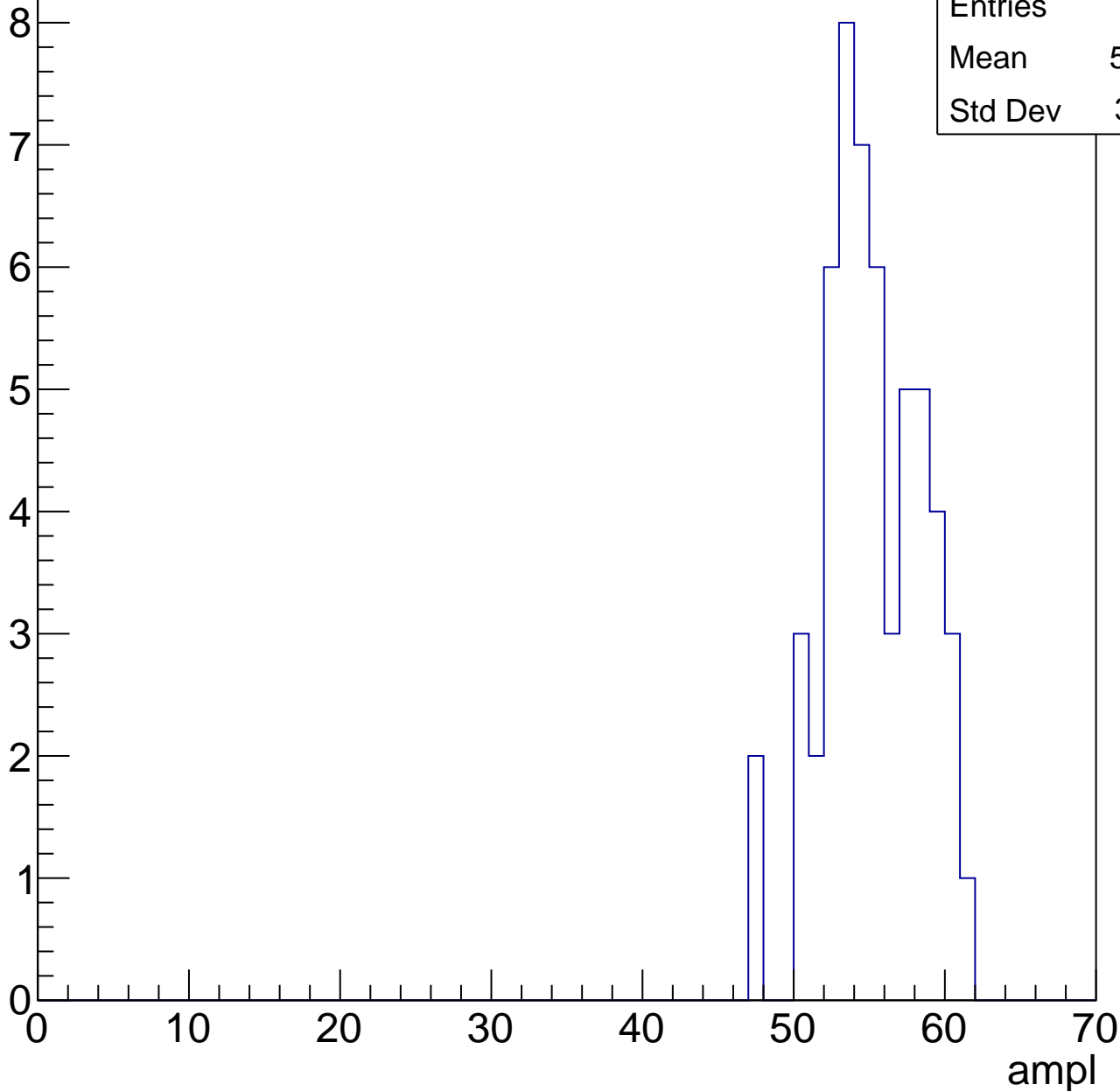


B1L103S, U5-ch113, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	54.73
Std Dev	3.211

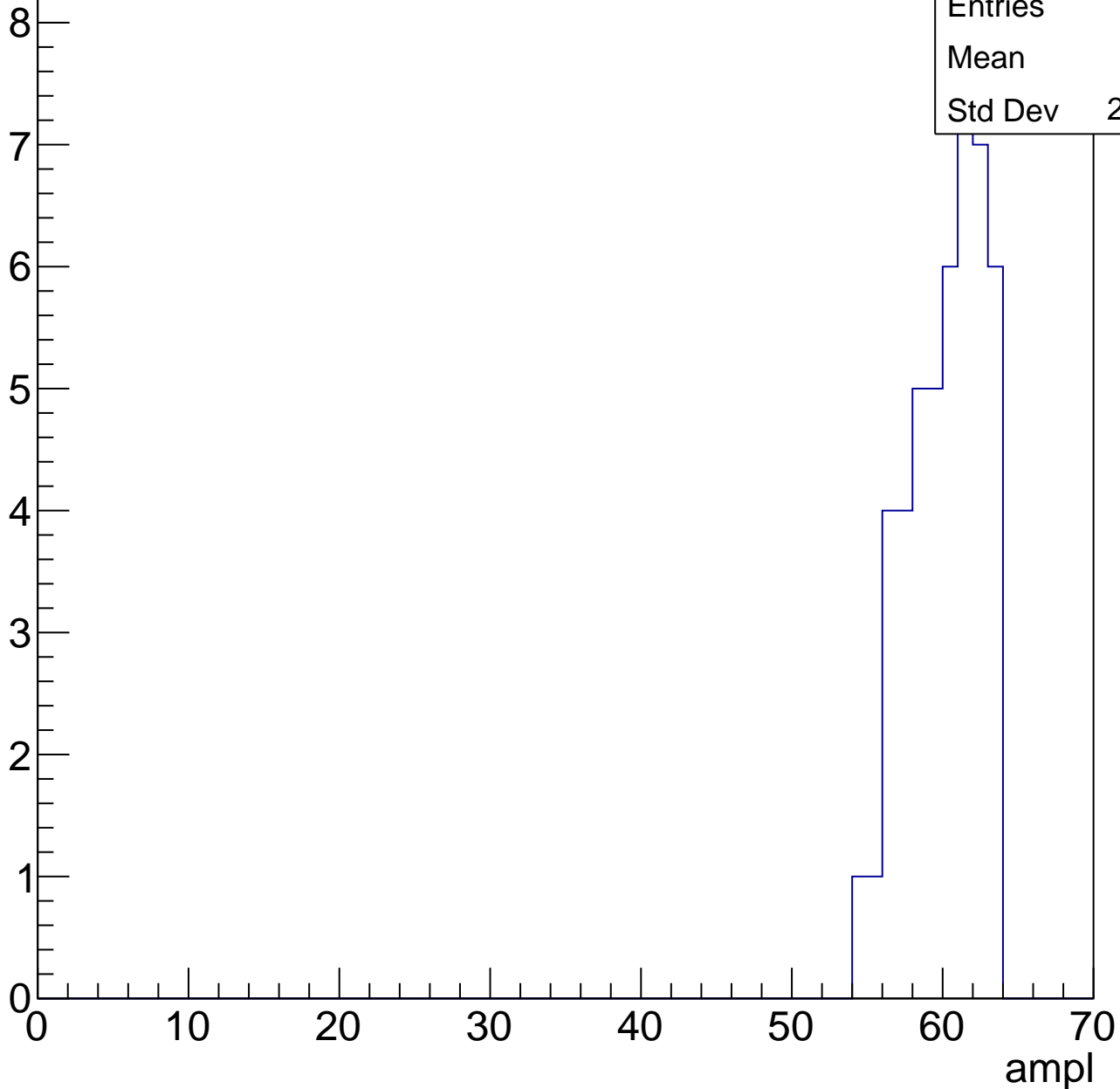


B1L103S, U5-ch113, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

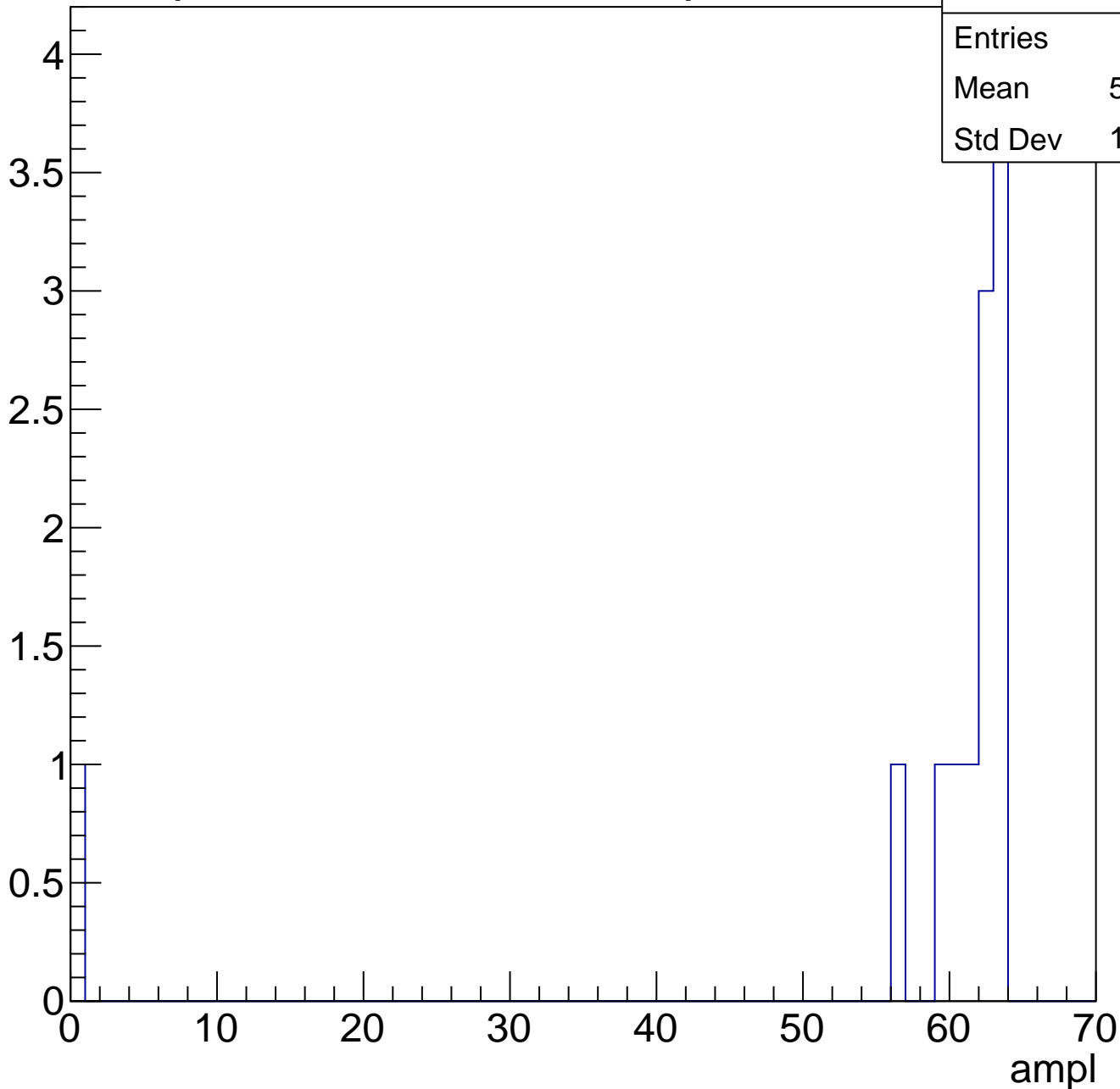
Entries	47
Mean	59.7
Std Dev	2.405



B1L103S, U5-ch113, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch113, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

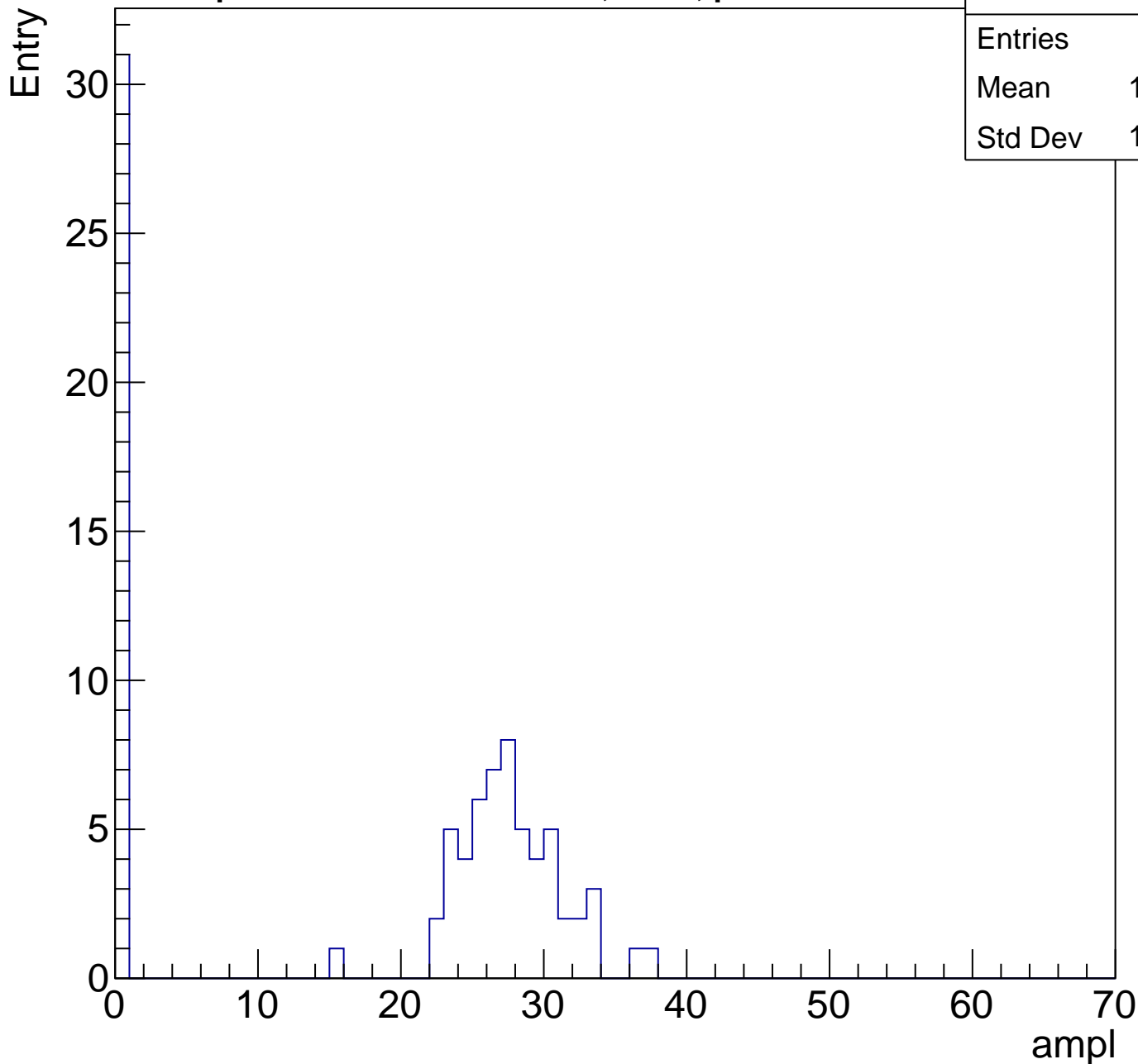
Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U5-ch114, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	87
Mean	17.49
Std Dev	13.35

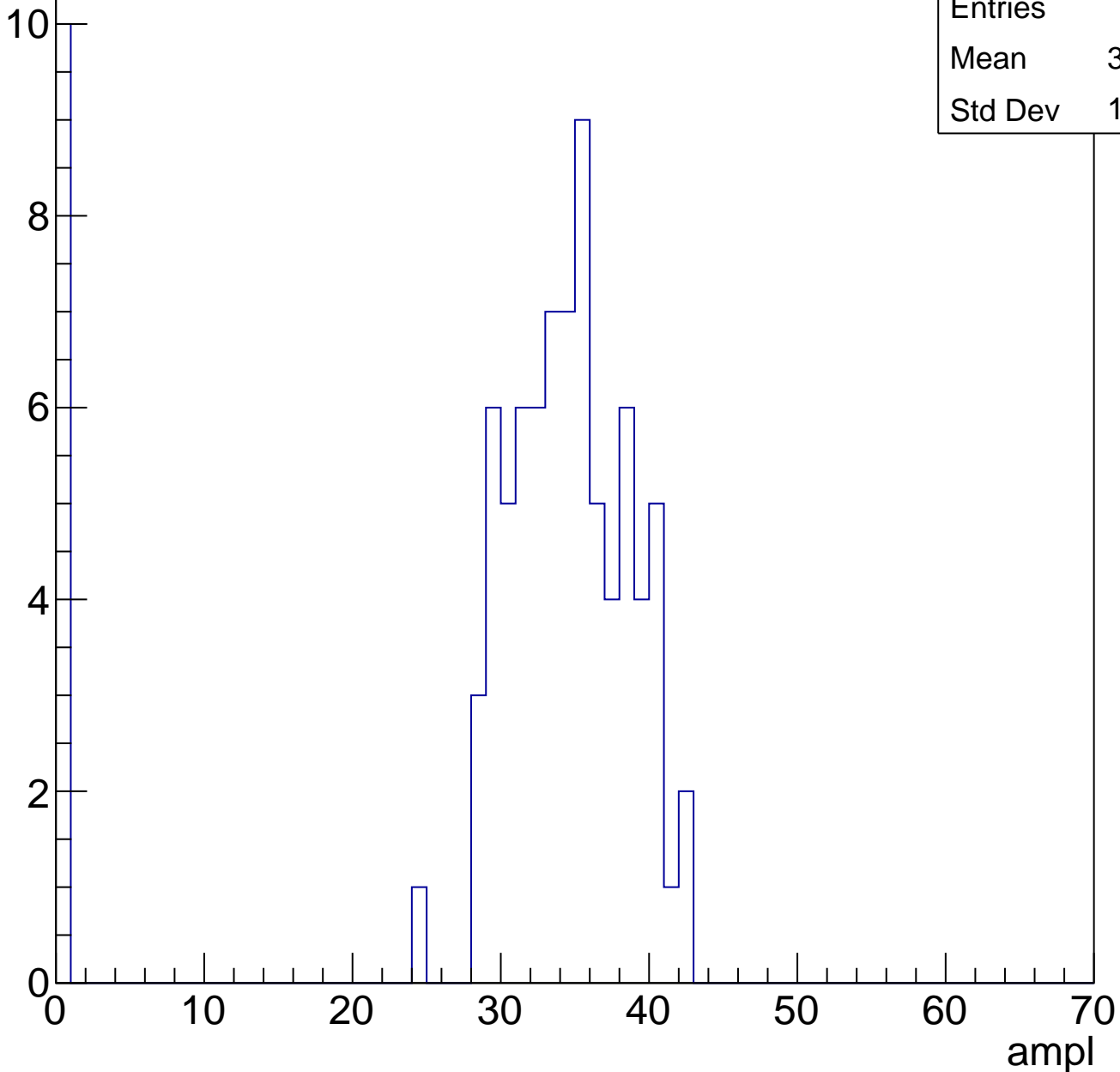


B1L103S, U5-ch114, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	87
Mean	30.24
Std Dev	11.48

Entry

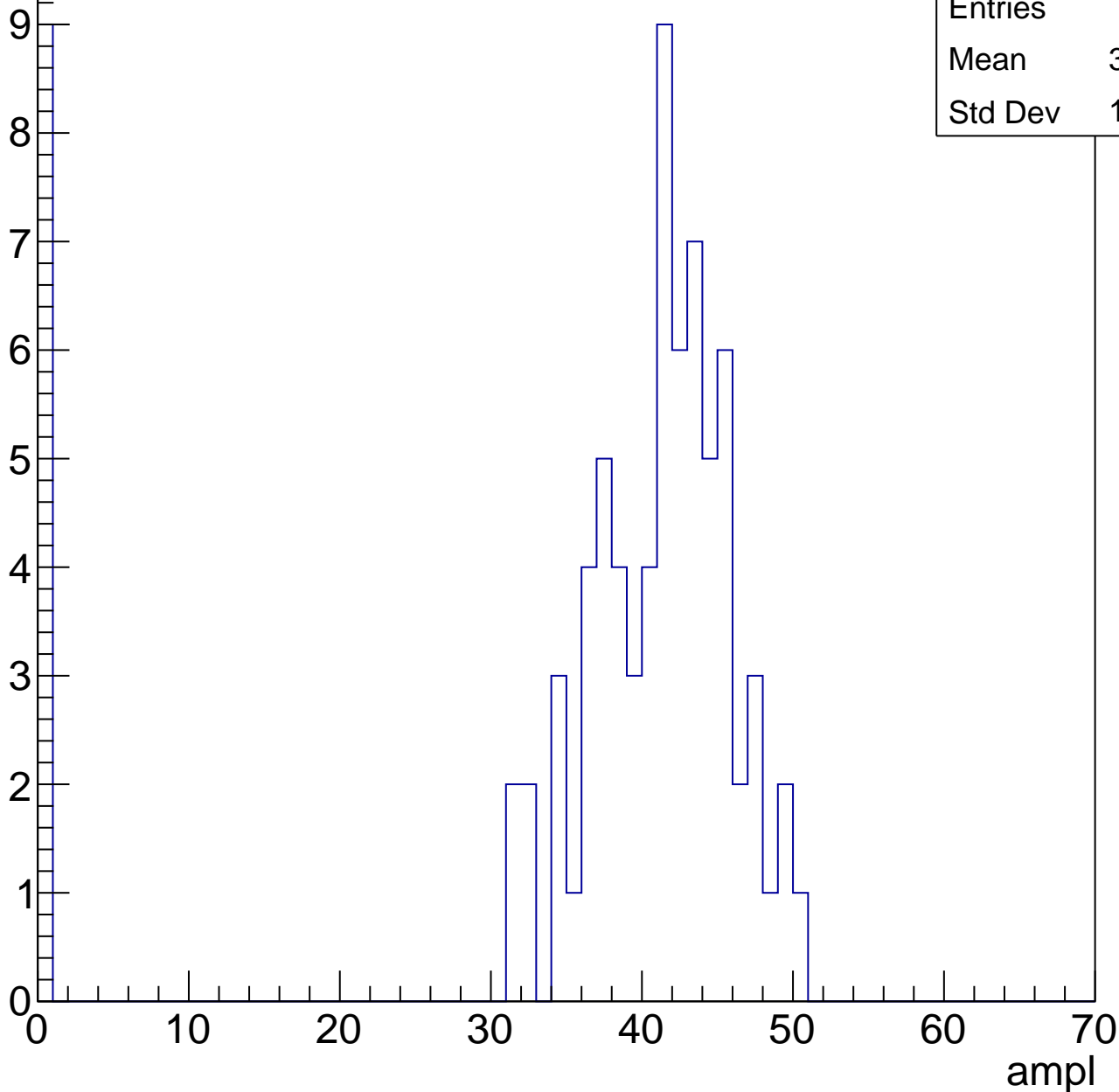


B1L103S, U5-ch114, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	79
Mean	36.23
Std Dev	13.64

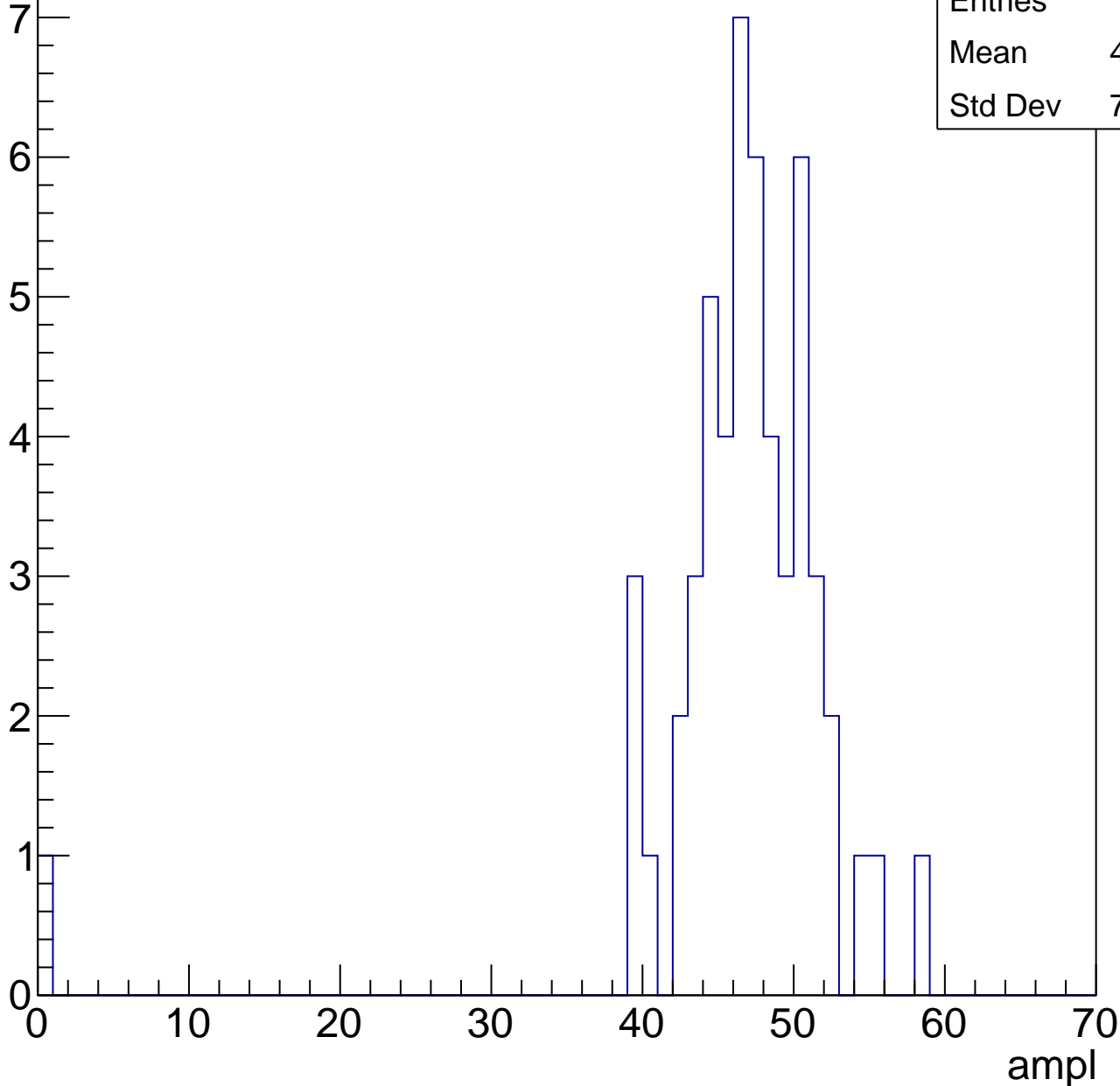


B1L103S, U5-ch114, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	45.98
Std Dev	7.477

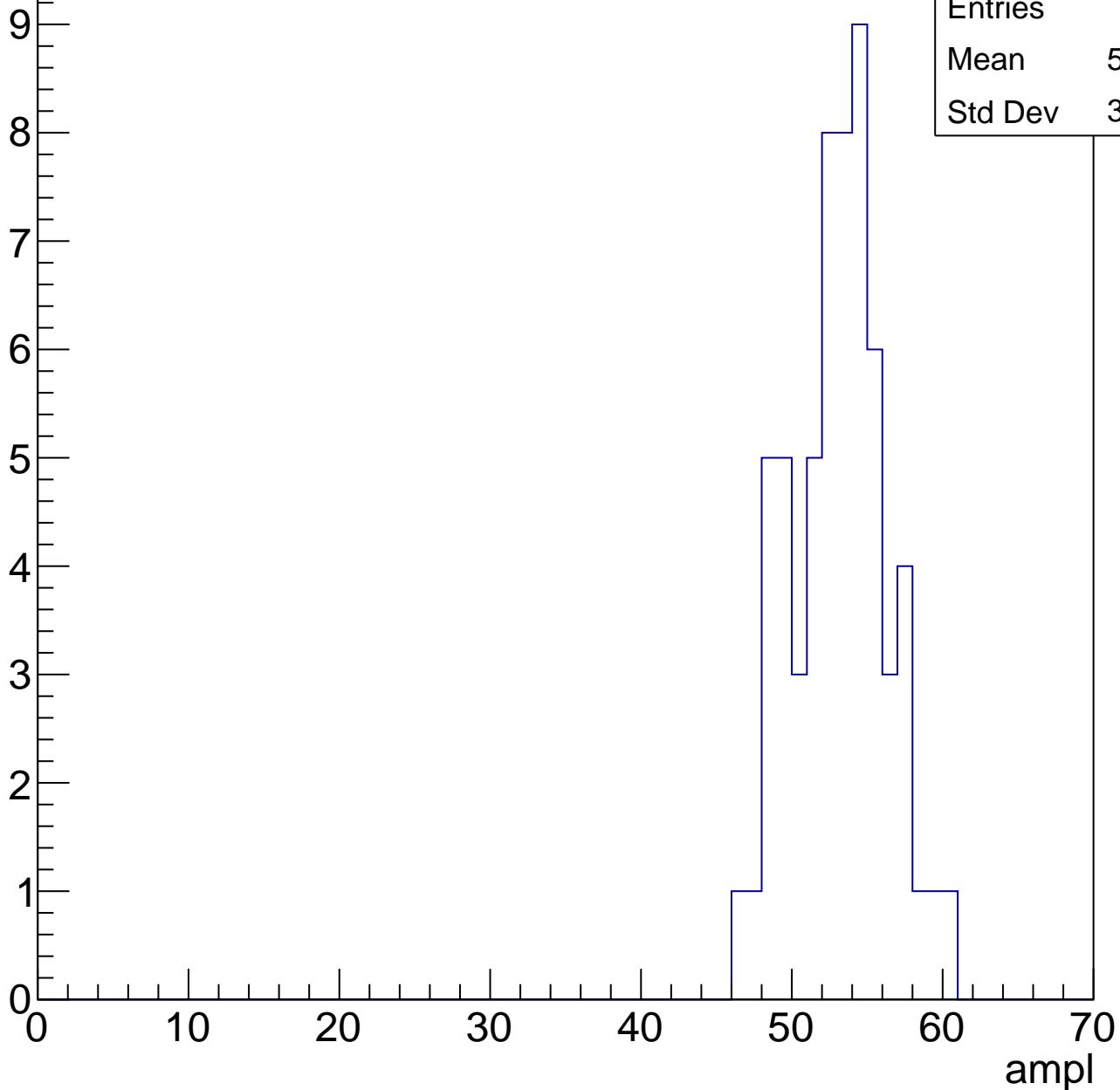


B1L103S, U5-ch114, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

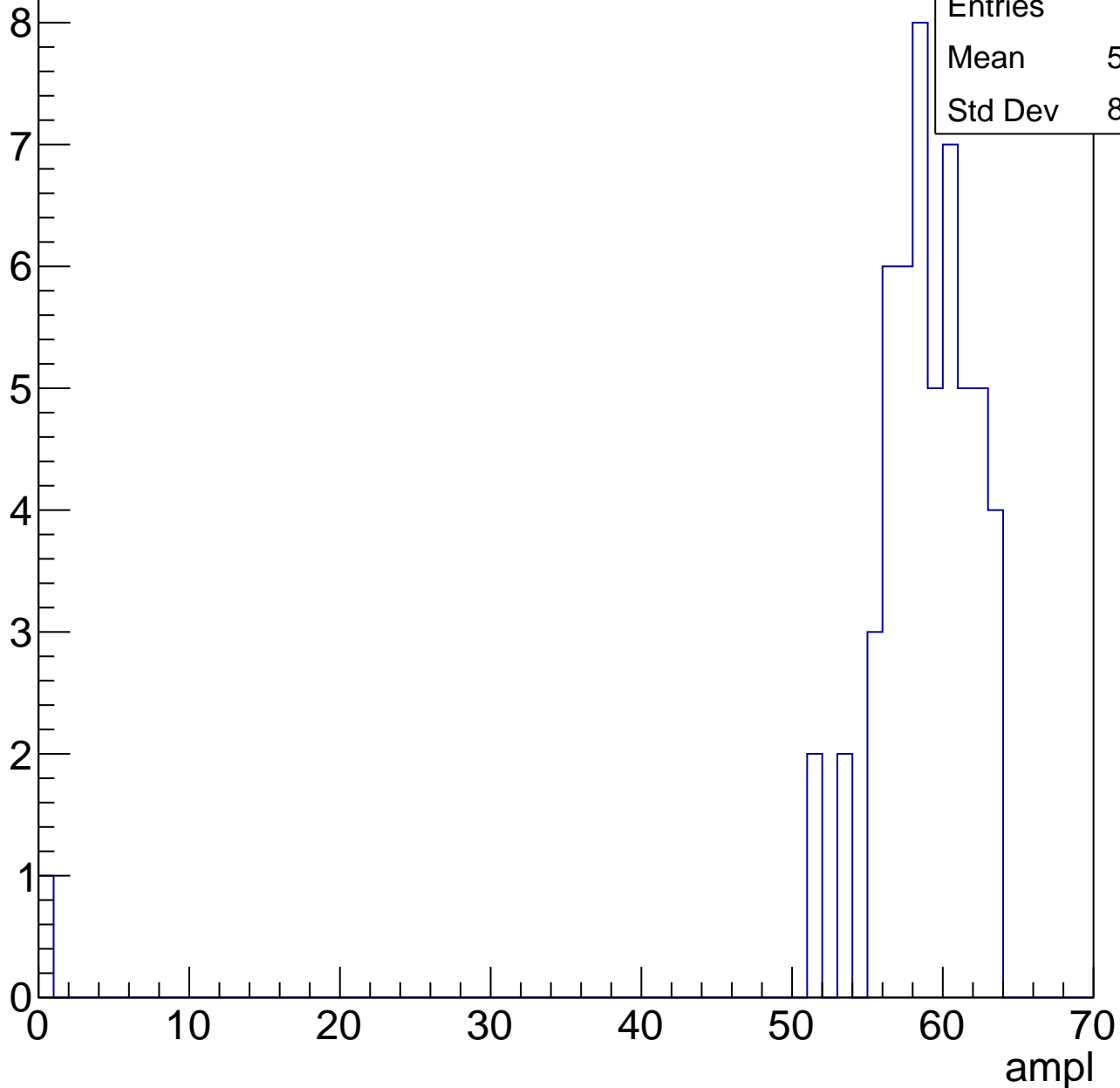
Entries	61
Mean	52.66
Std Dev	3.062



B1L103S, U5-ch114, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

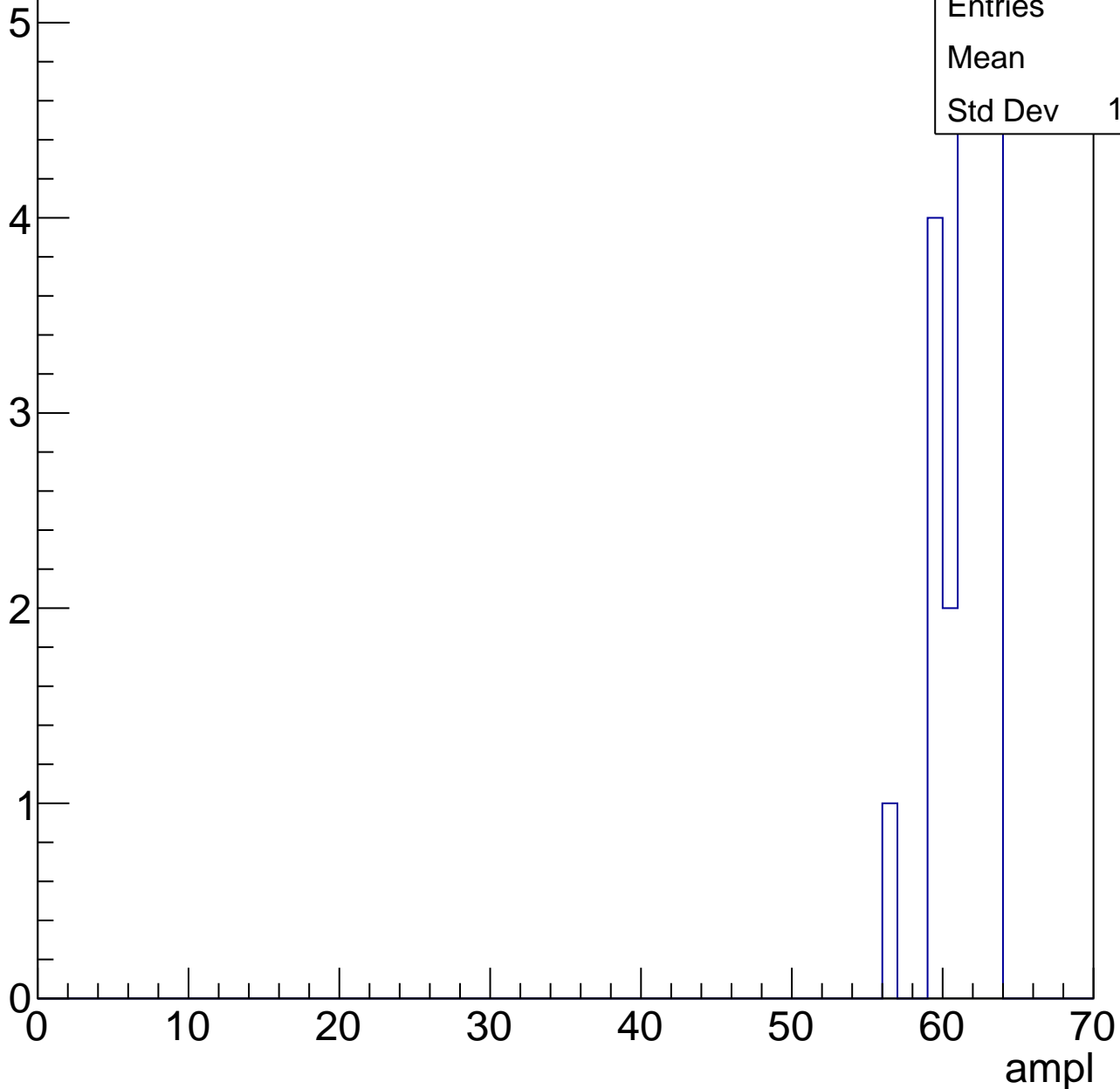


B1L103S, U5-ch114, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	22
Mean	61
Std Dev	1.758



B1L103S, U5-ch114, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

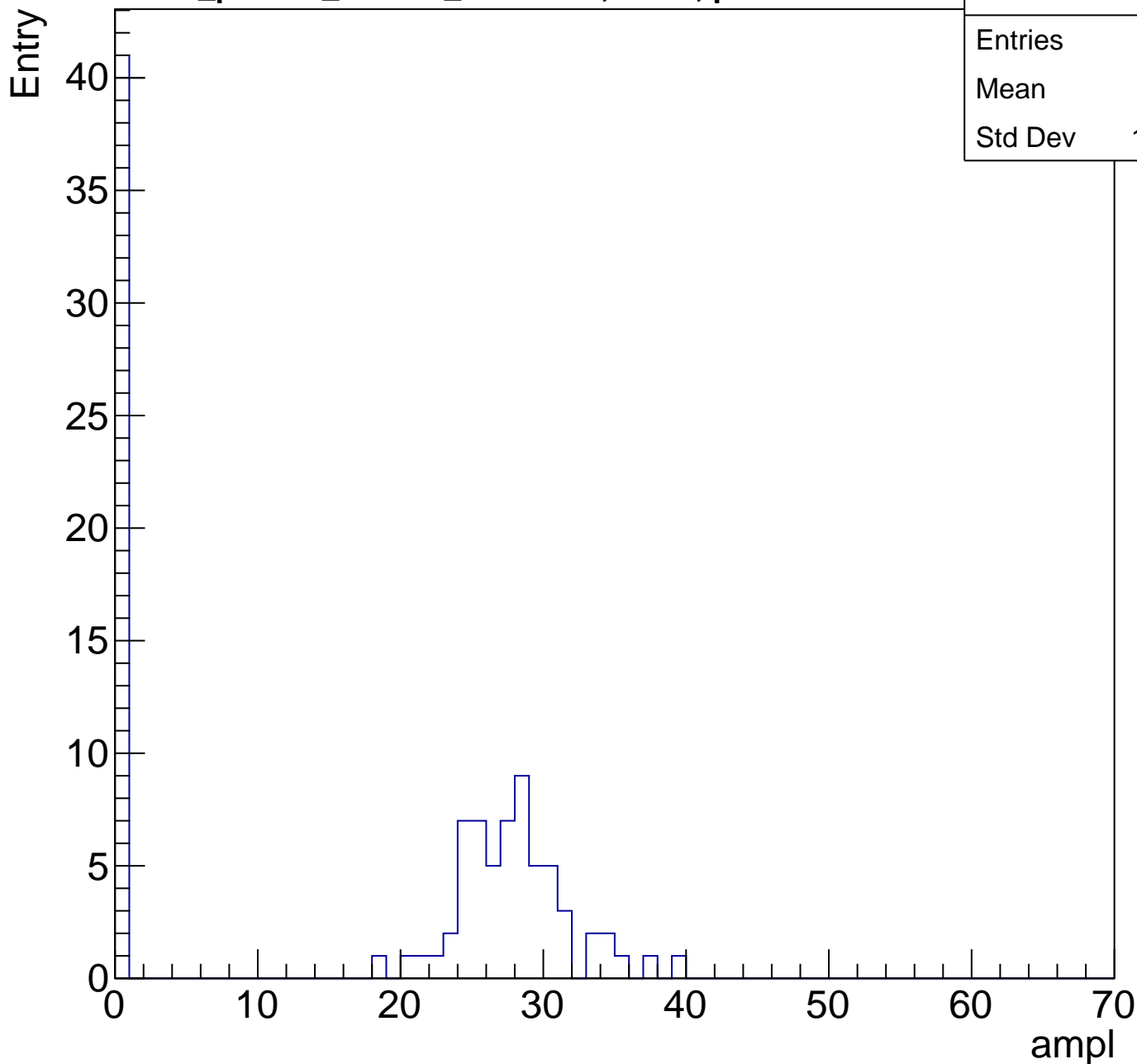
Entry



B1L103S, U5-ch115, adc0

calib_packv5_041523_1651.root, FC#0, port C2

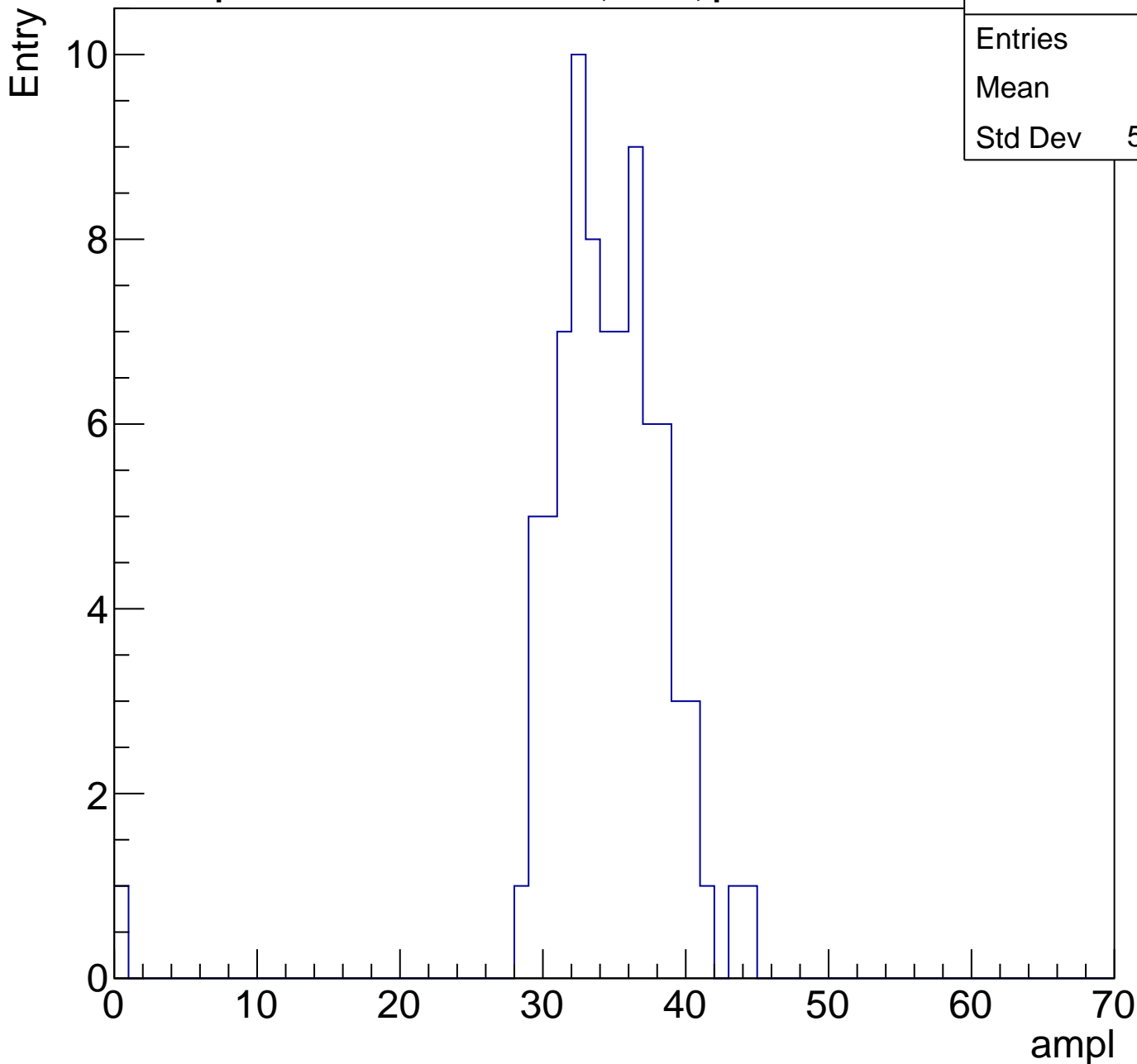
Entries	102
Mean	16.41
Std Dev	13.78



B1L103S, U5-ch115, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	33.9
Std Dev	5.108

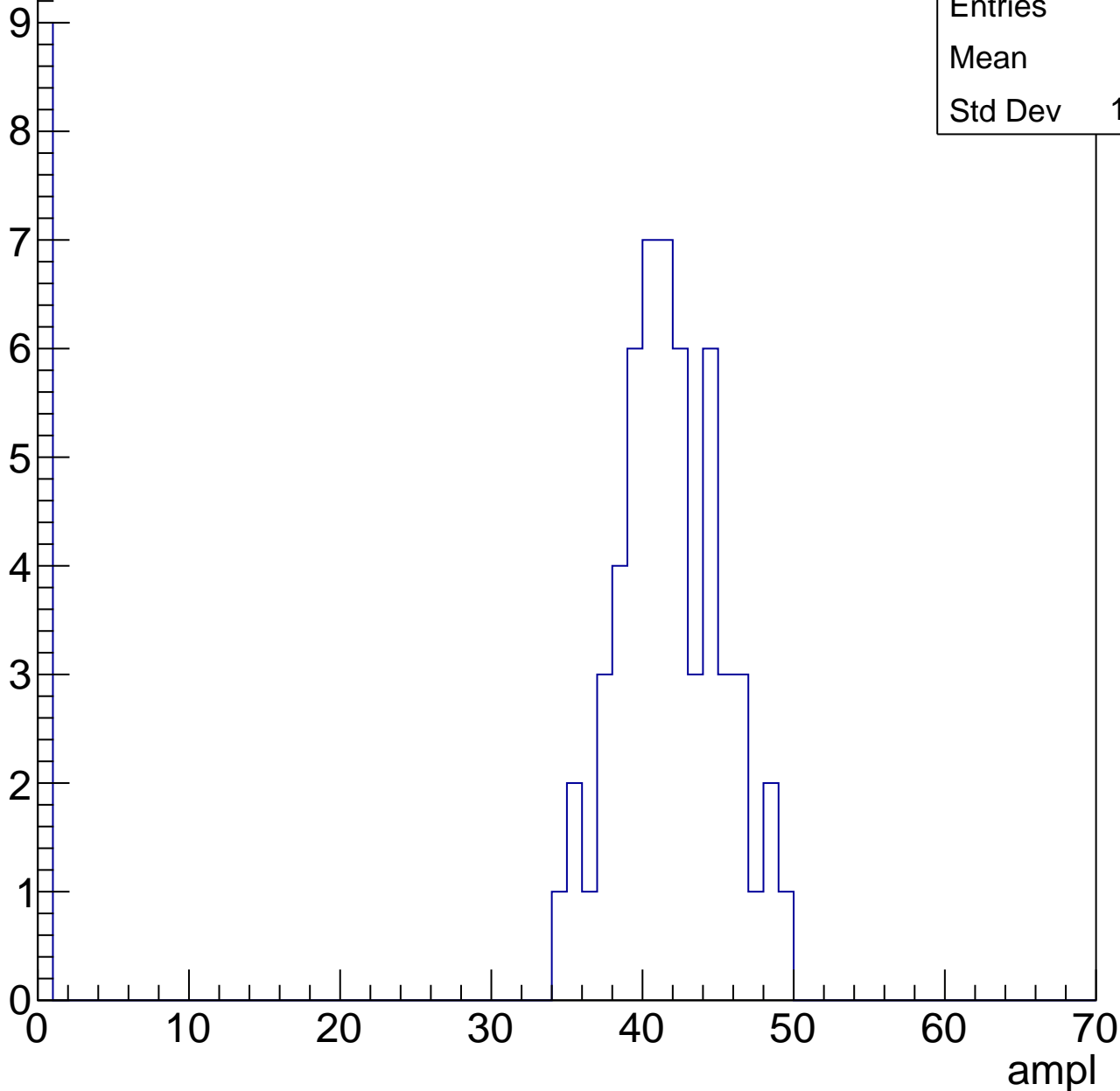


B1L103S, U5-ch115, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	35.6
Std Dev	14.62

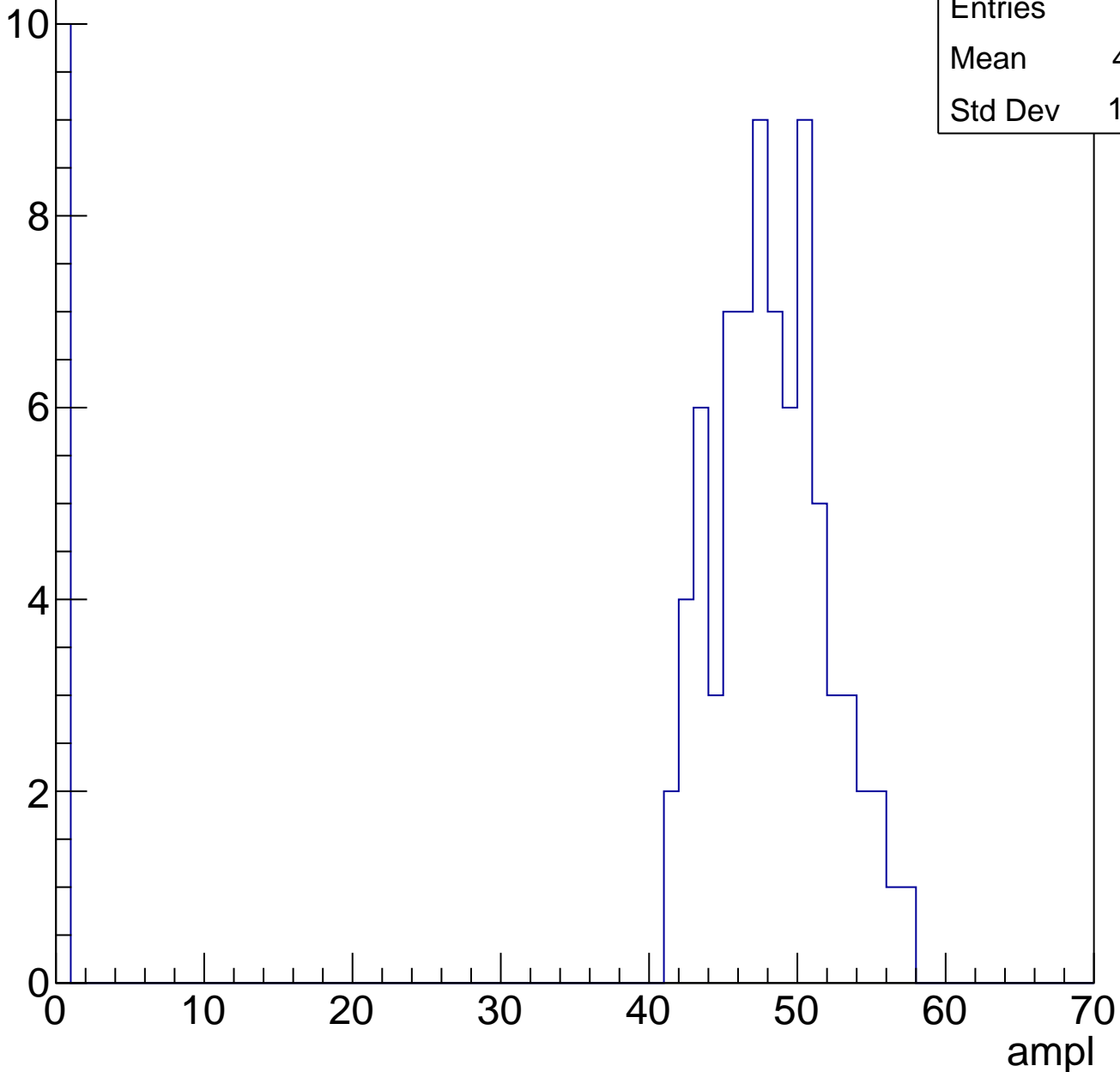


B1L103S, U5-ch115, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	87
Mean	42.31
Std Dev	15.64

Entry

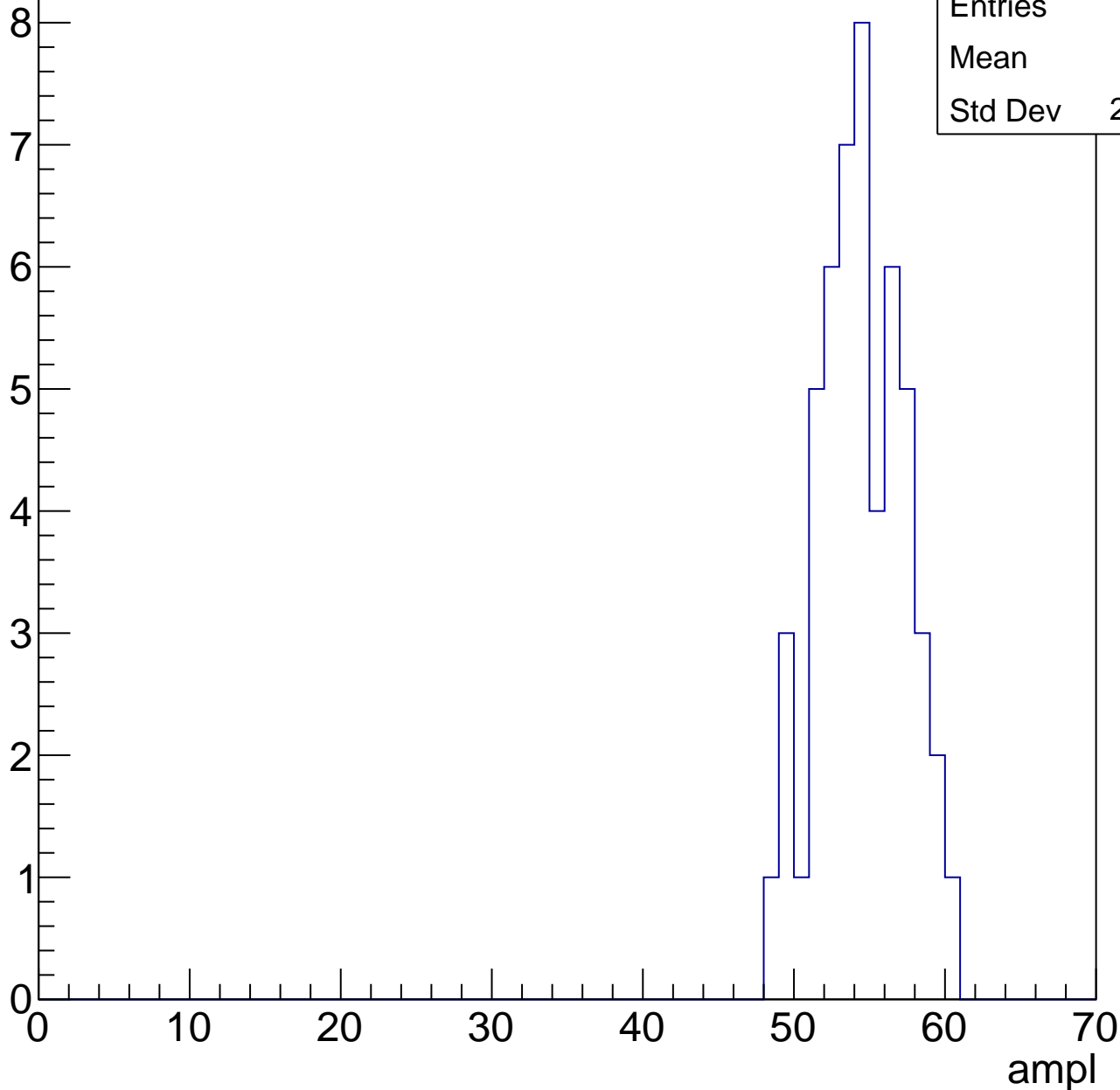


B1L103S, U5-ch115, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	54
Std Dev	2.808

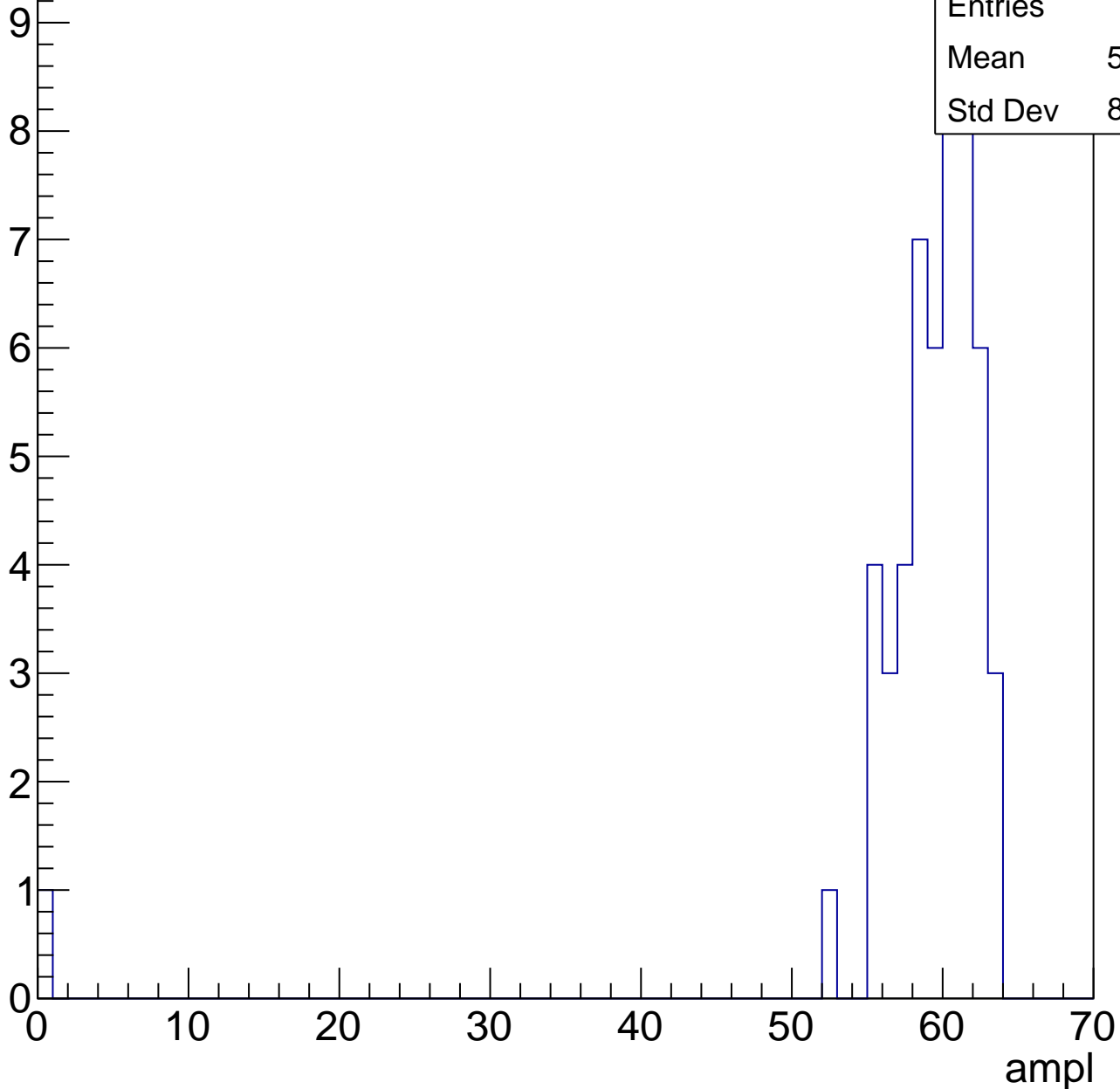


B1L103S, U5-ch115, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	58.08
Std Dev	8.407

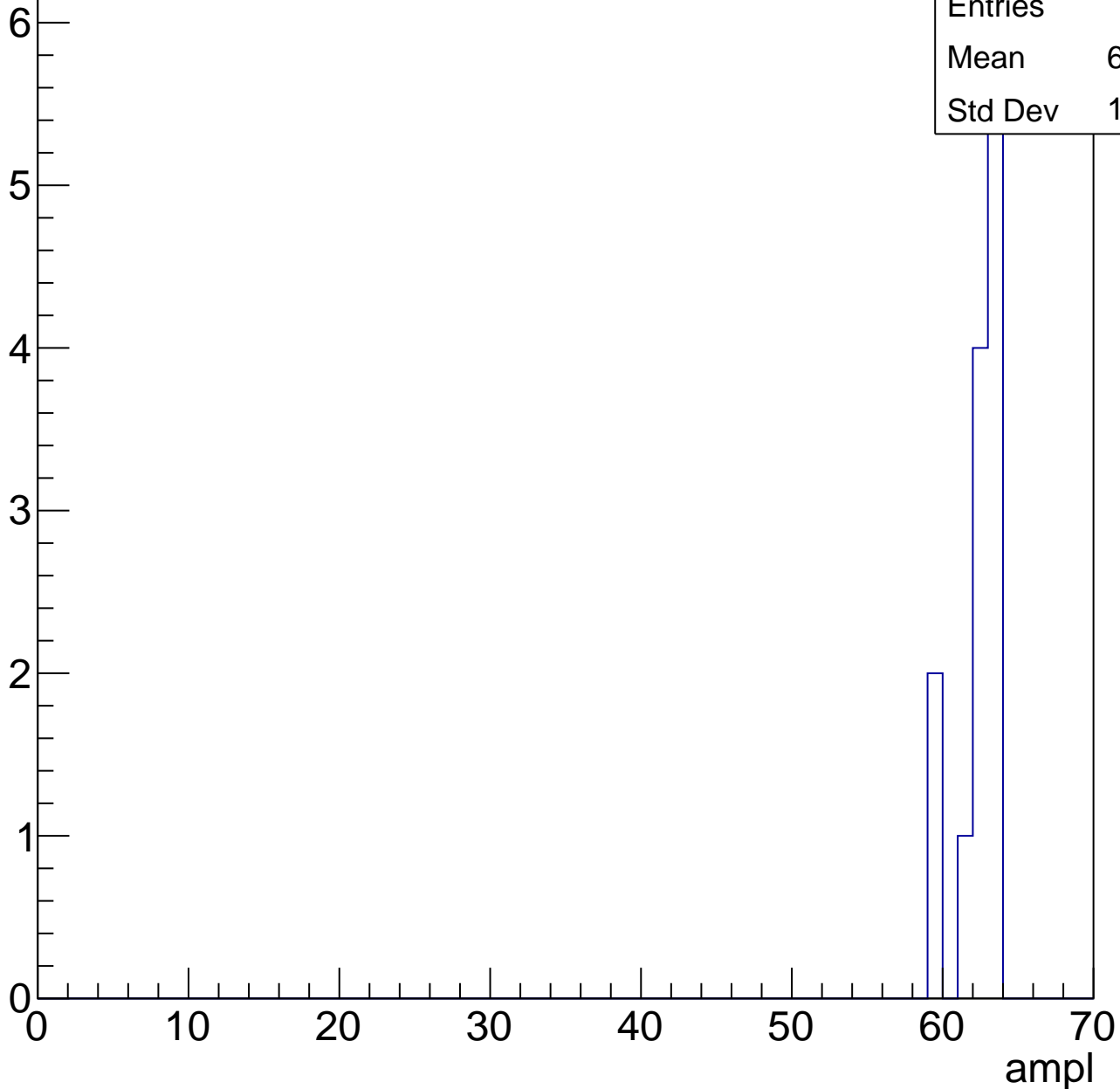


B1L103S, U5-ch115, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	13
Mean	61.92
Std Dev	1.385



B1L103S, U5-ch115, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry



B1L103S, U5-ch116, adc0

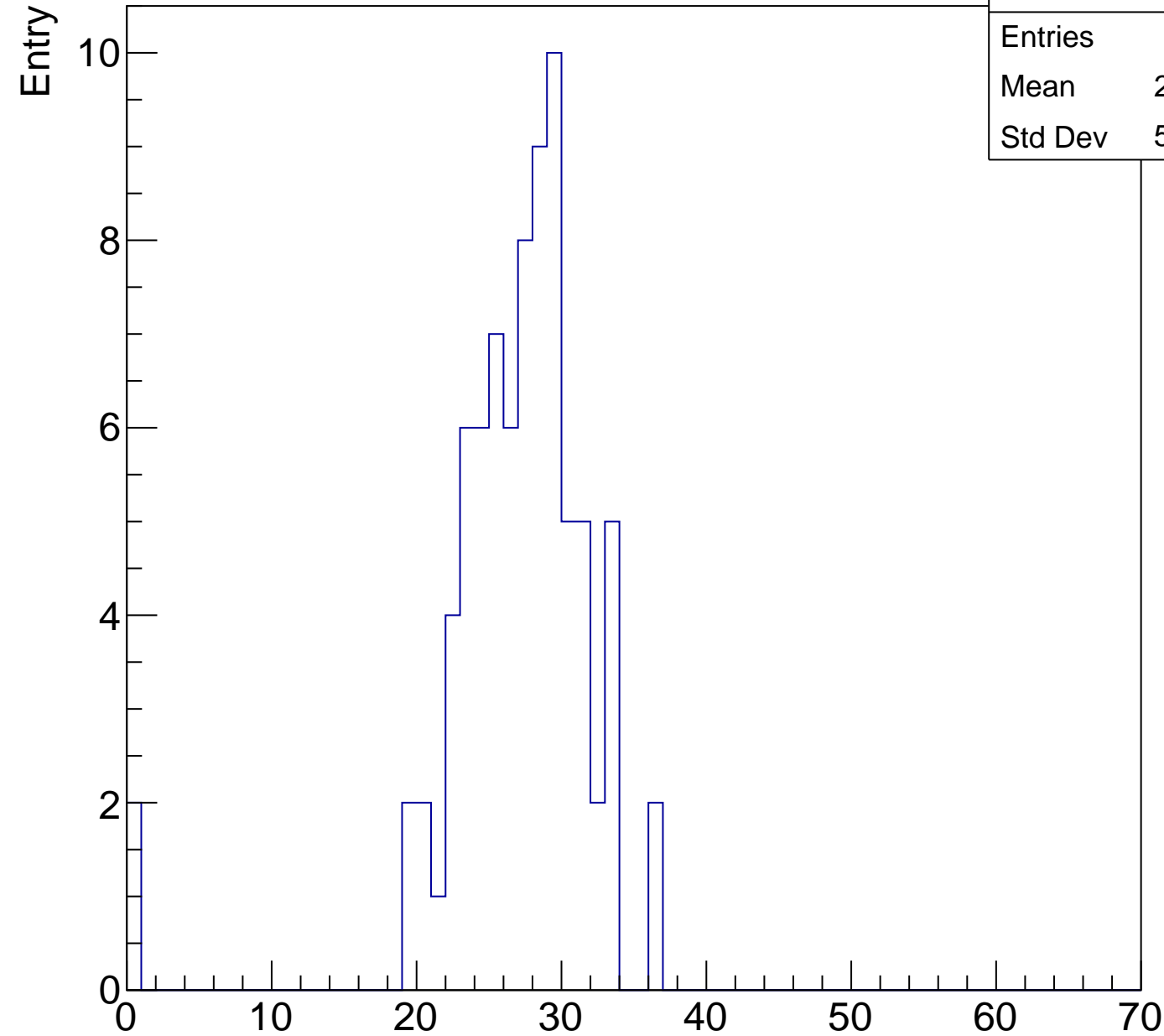
calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	26.39
Std Dev	5.565

Entry

10
8
6
4
2
0

ampl

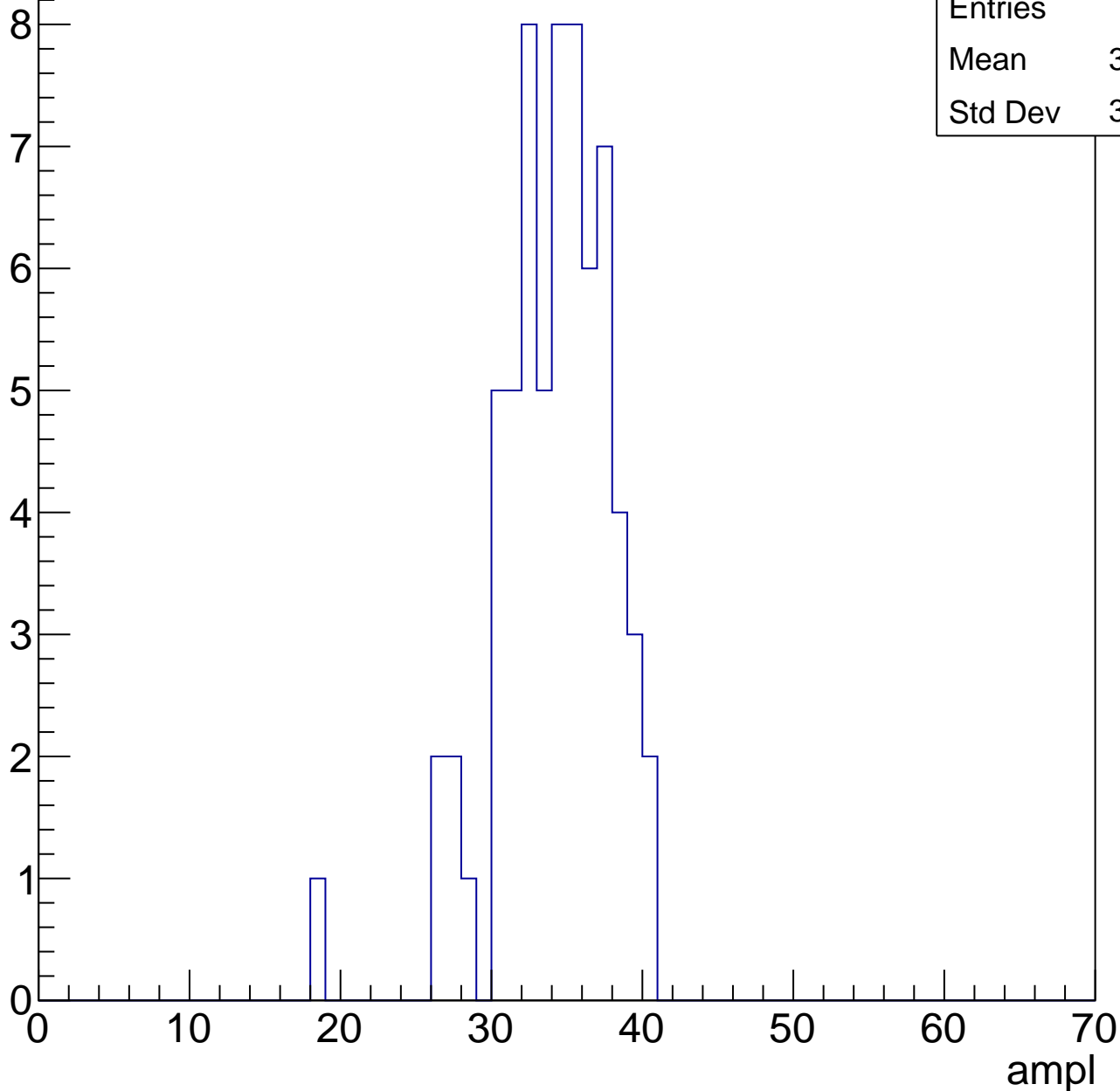


B1L103S, U5-ch116, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	33.64
Std Dev	3.819

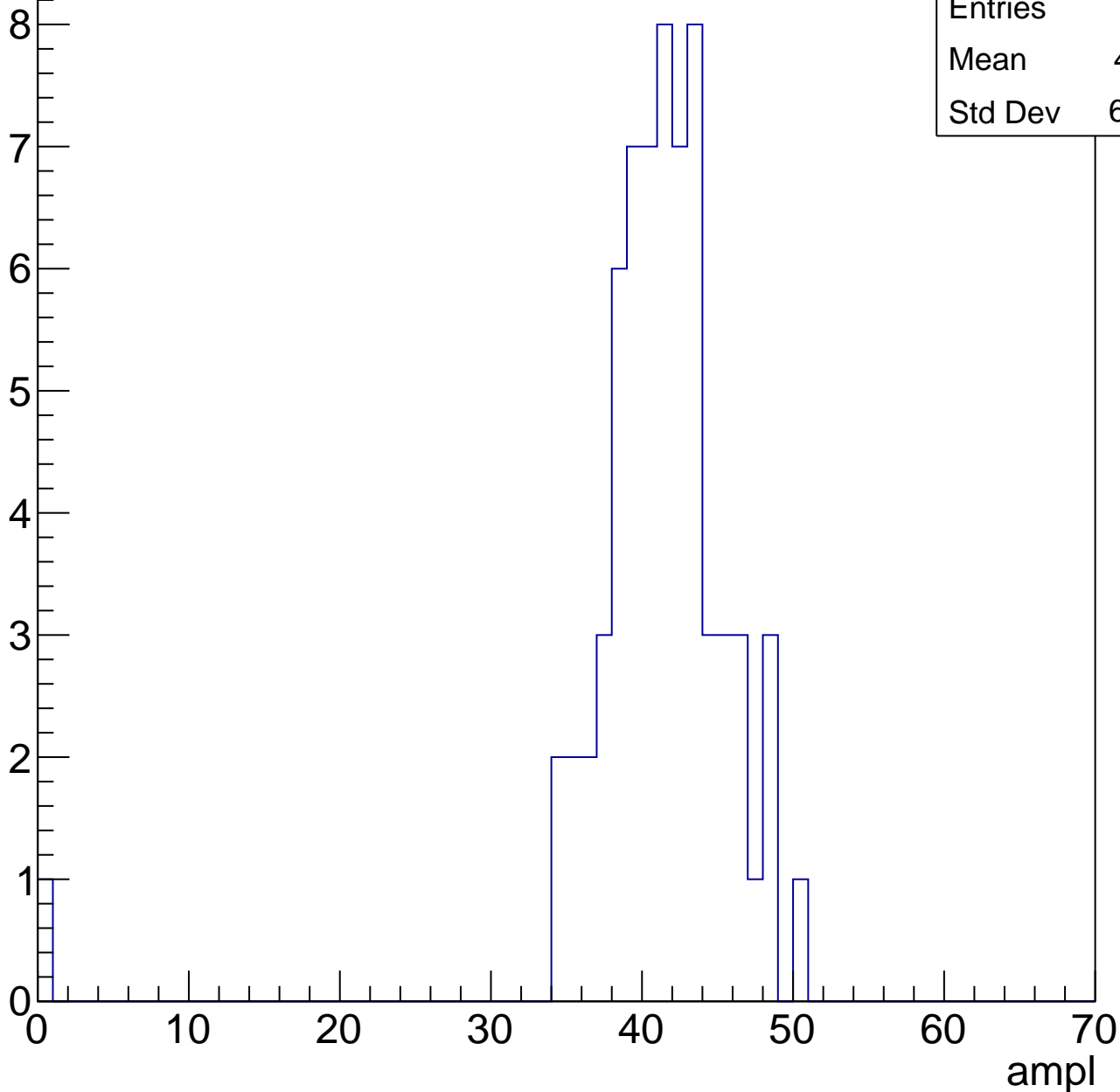


B1L103S, U5-ch116, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	40.51
Std Dev	6.078

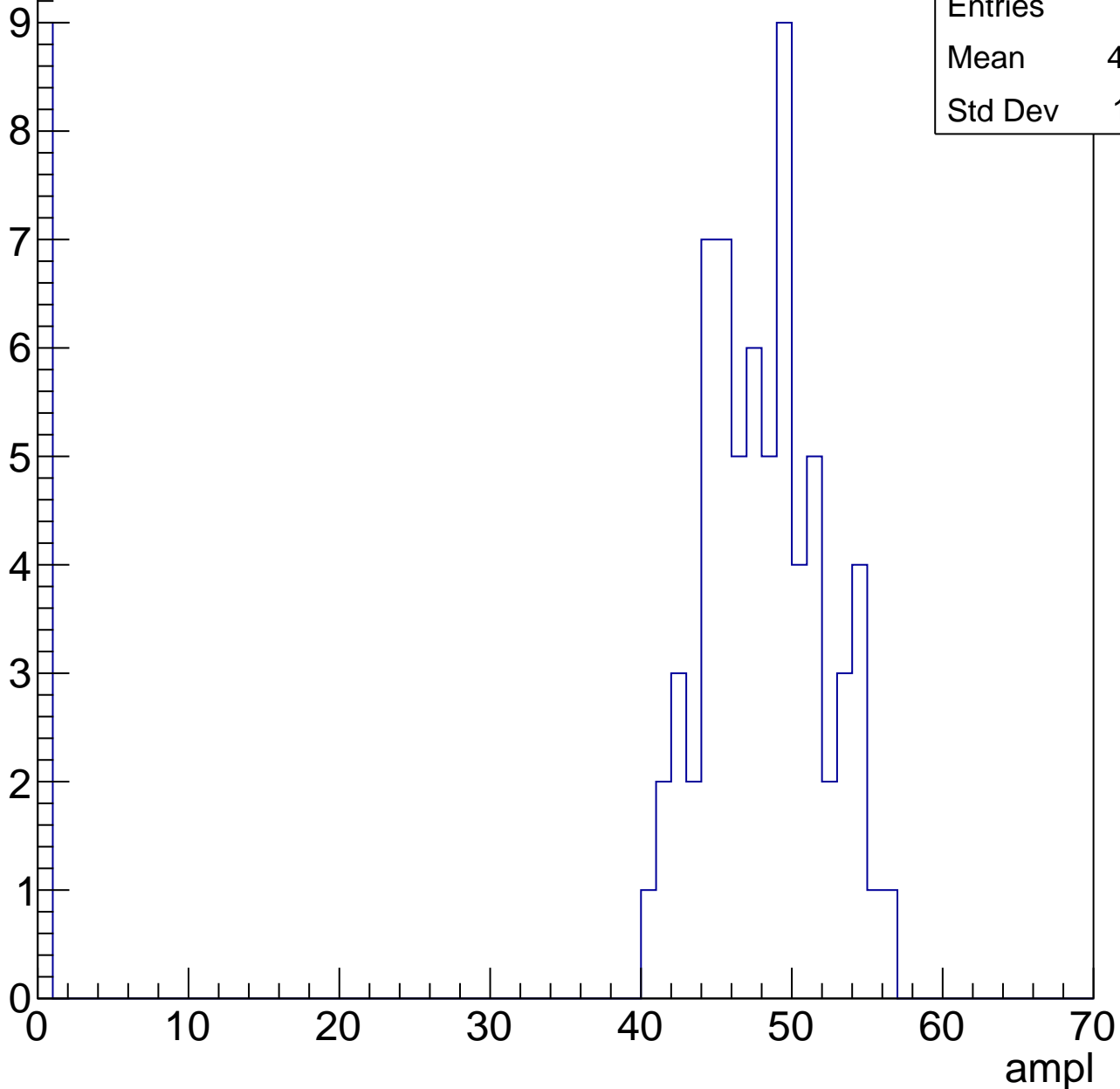


B1L103S, U5-ch116, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	42.04
Std Dev	15.81

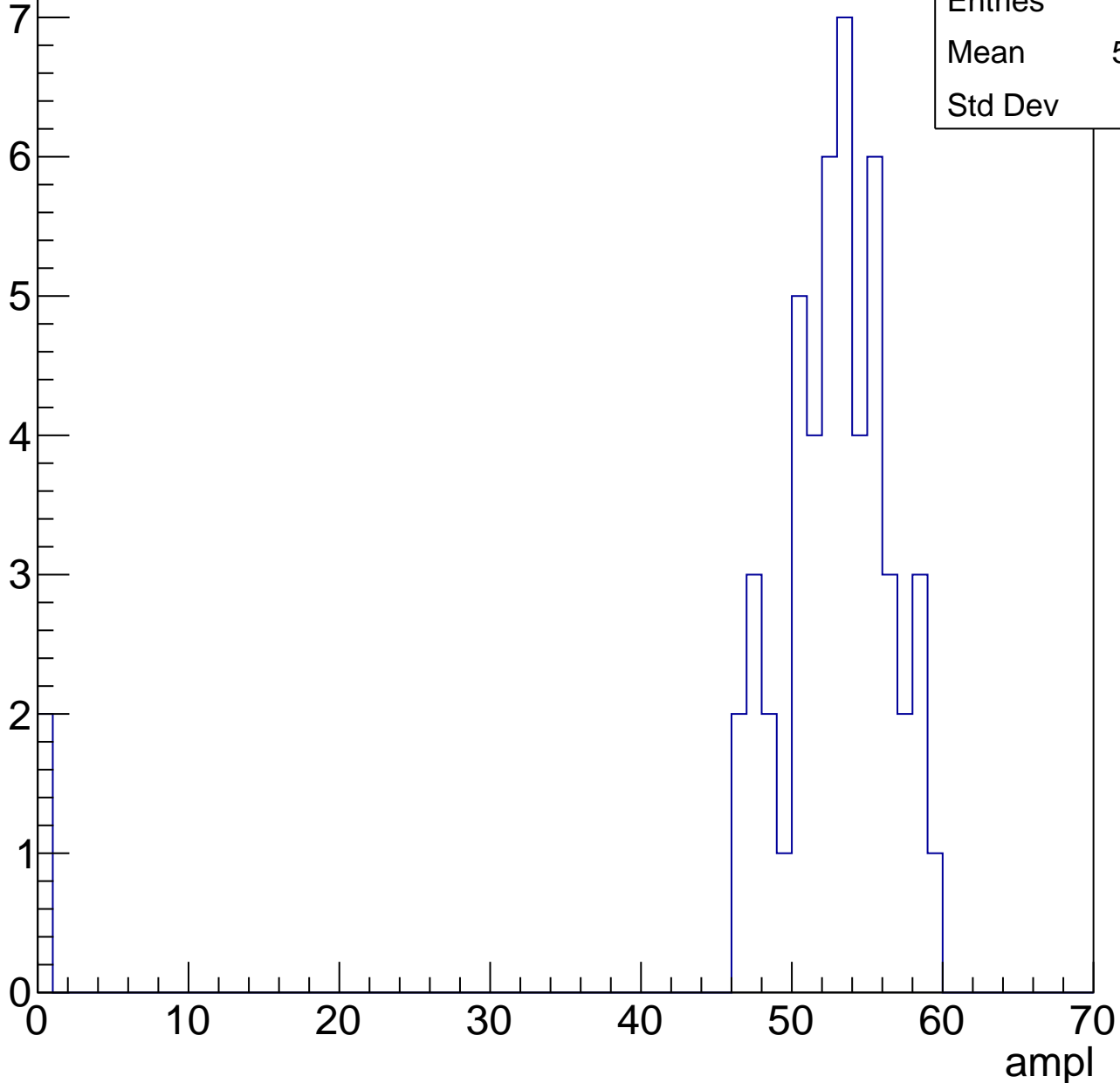


B1L103S, U5-ch116, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	50.51
Std Dev	10.7

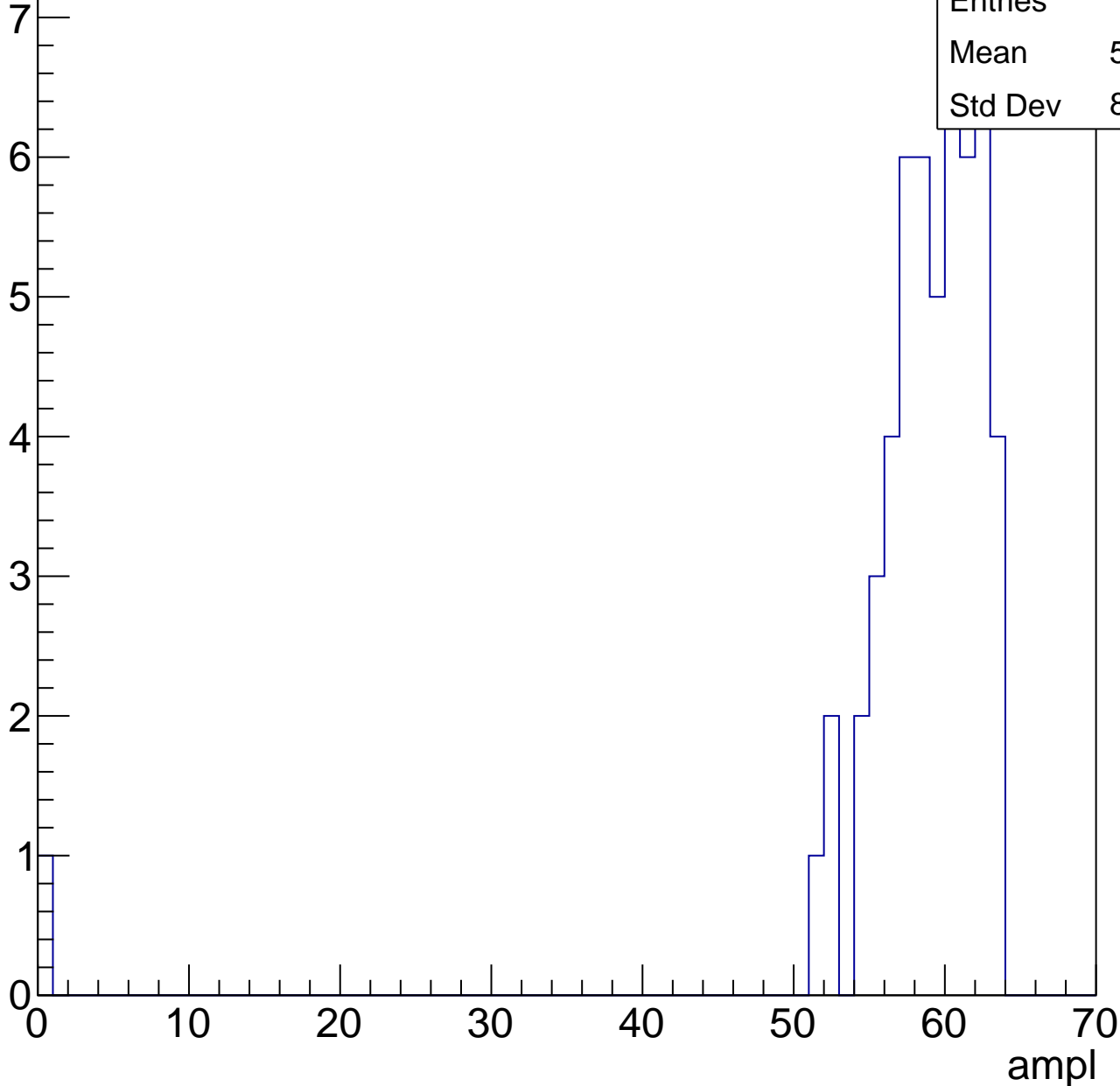


B1L103S, U5-ch116, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	57.57
Std Dev	8.449

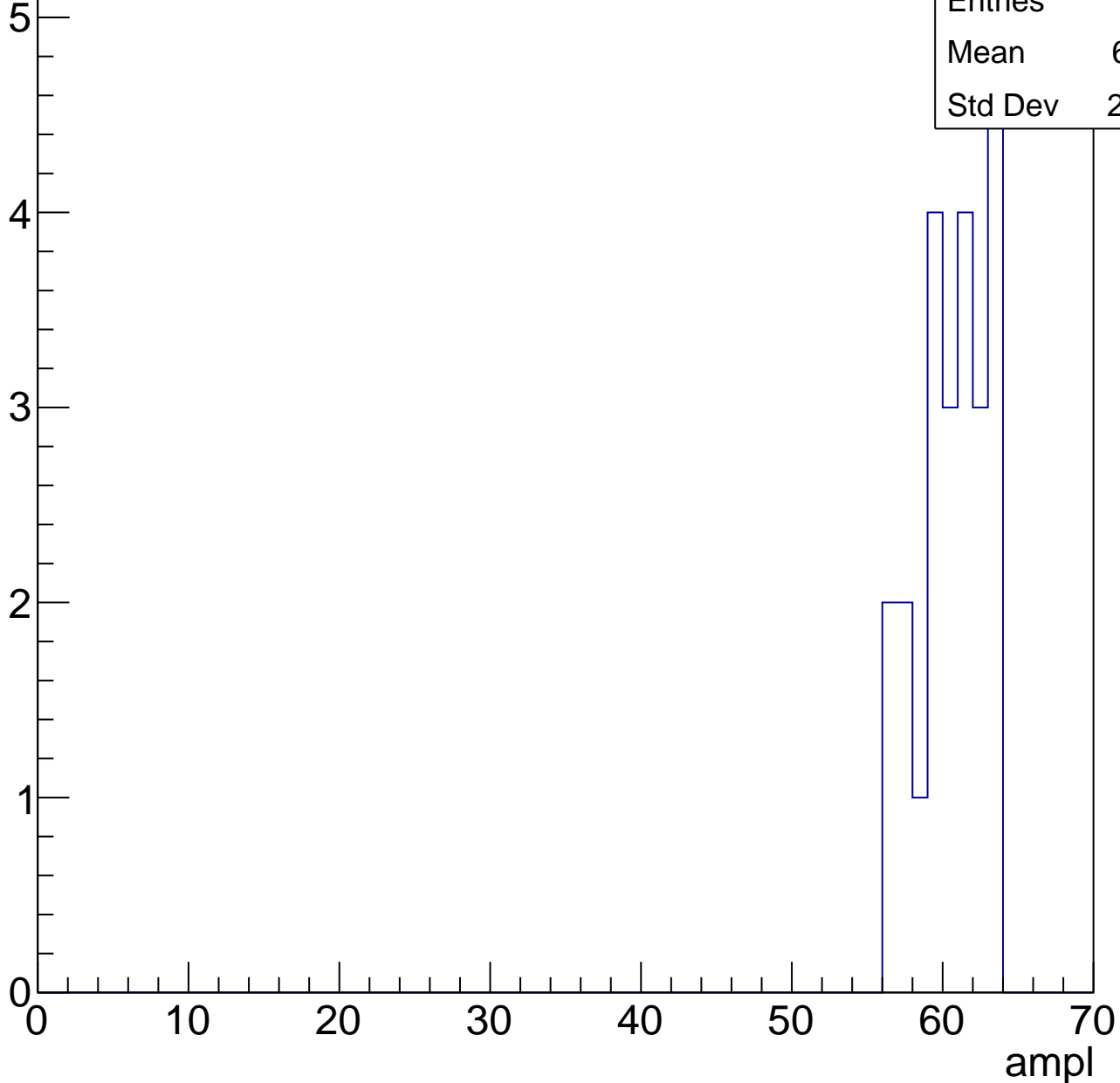


B1L103S, U5-ch116, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	24
Mean	60.21
Std Dev	2.217



B1L103S, U5-ch116, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

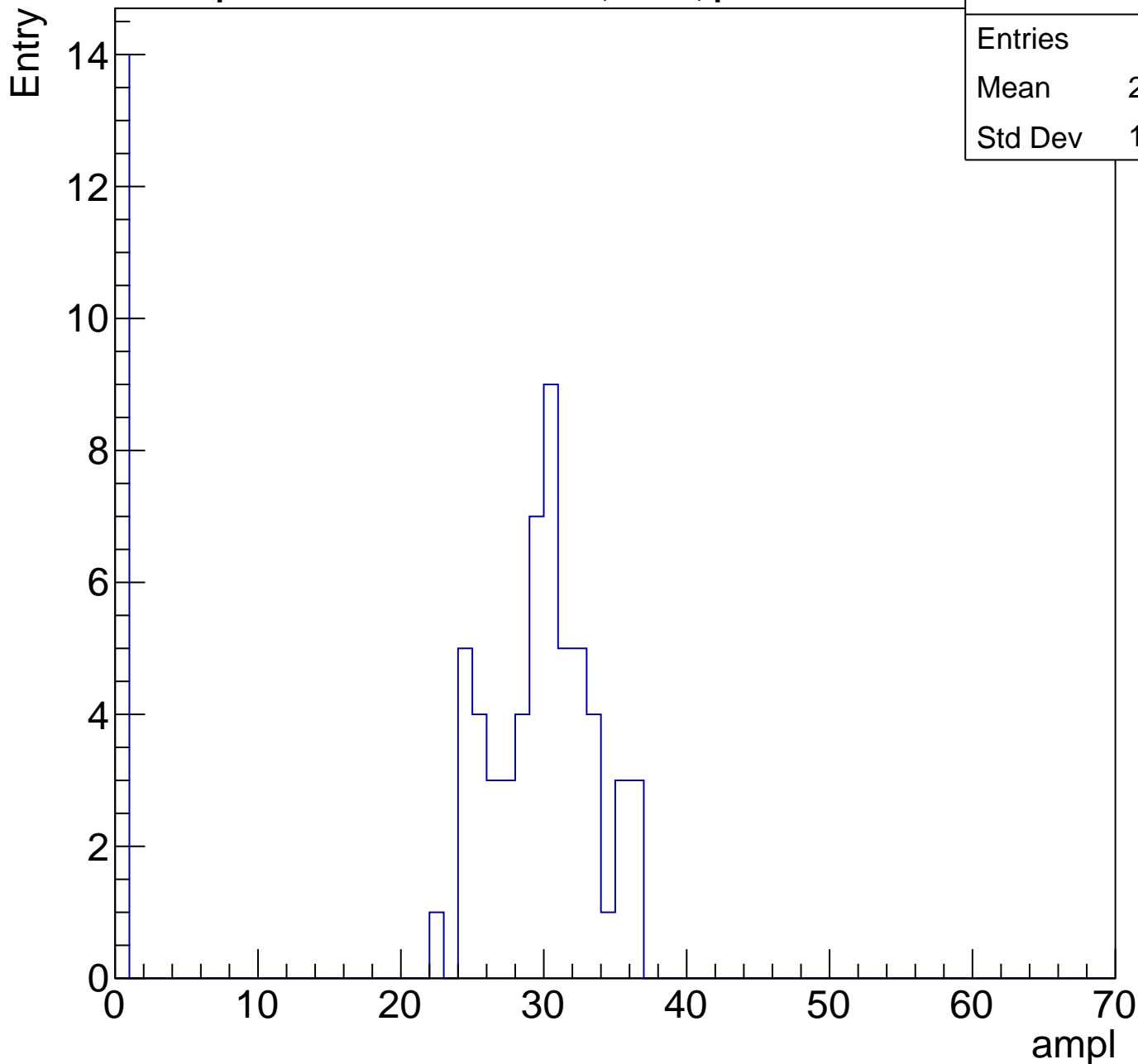
Entry



B1L103S, U5-ch117, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	71
Mean	23.66
Std Dev	12.13

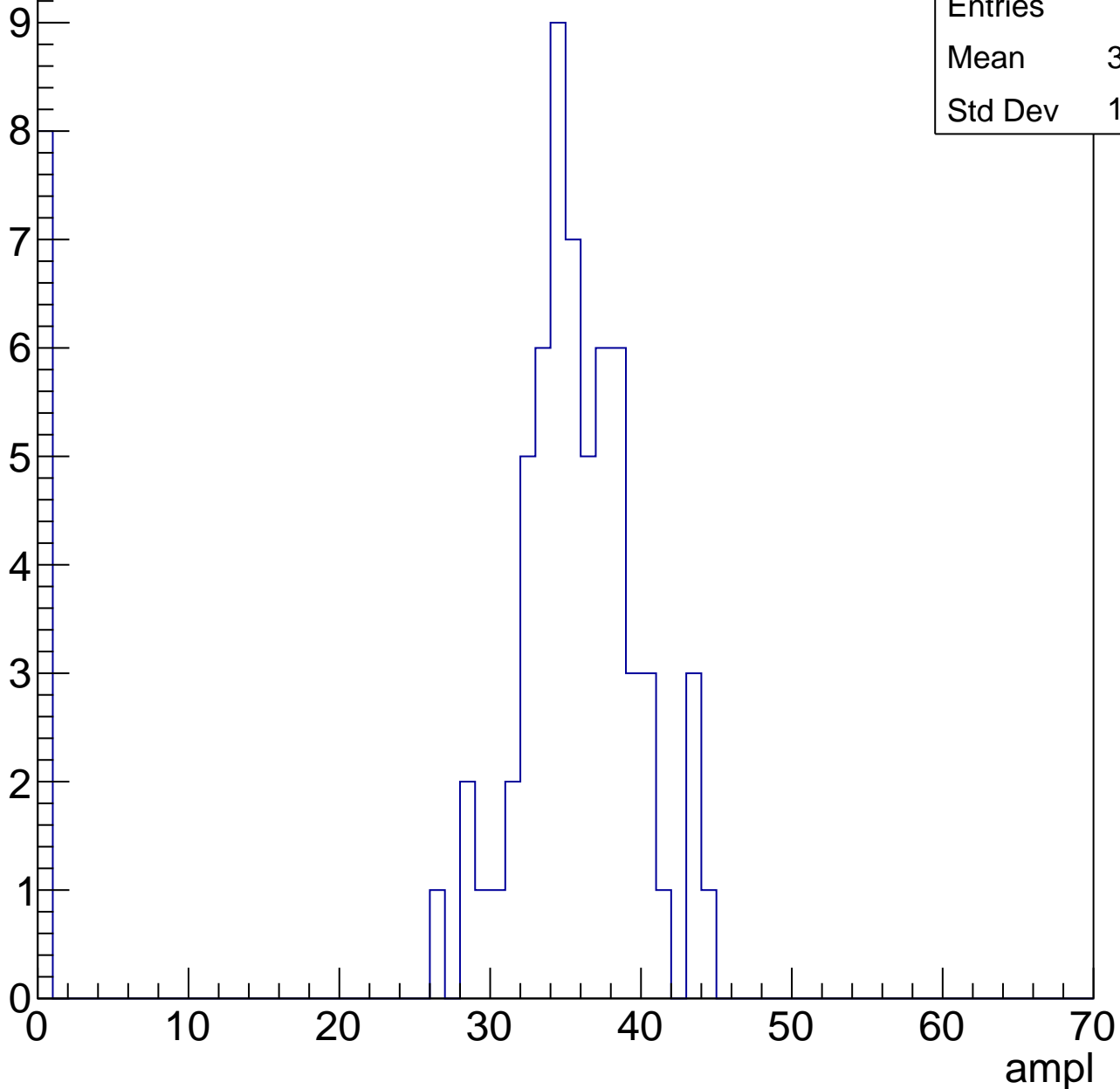


B1L103S, U5-ch117, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	31.33
Std Dev	11.78

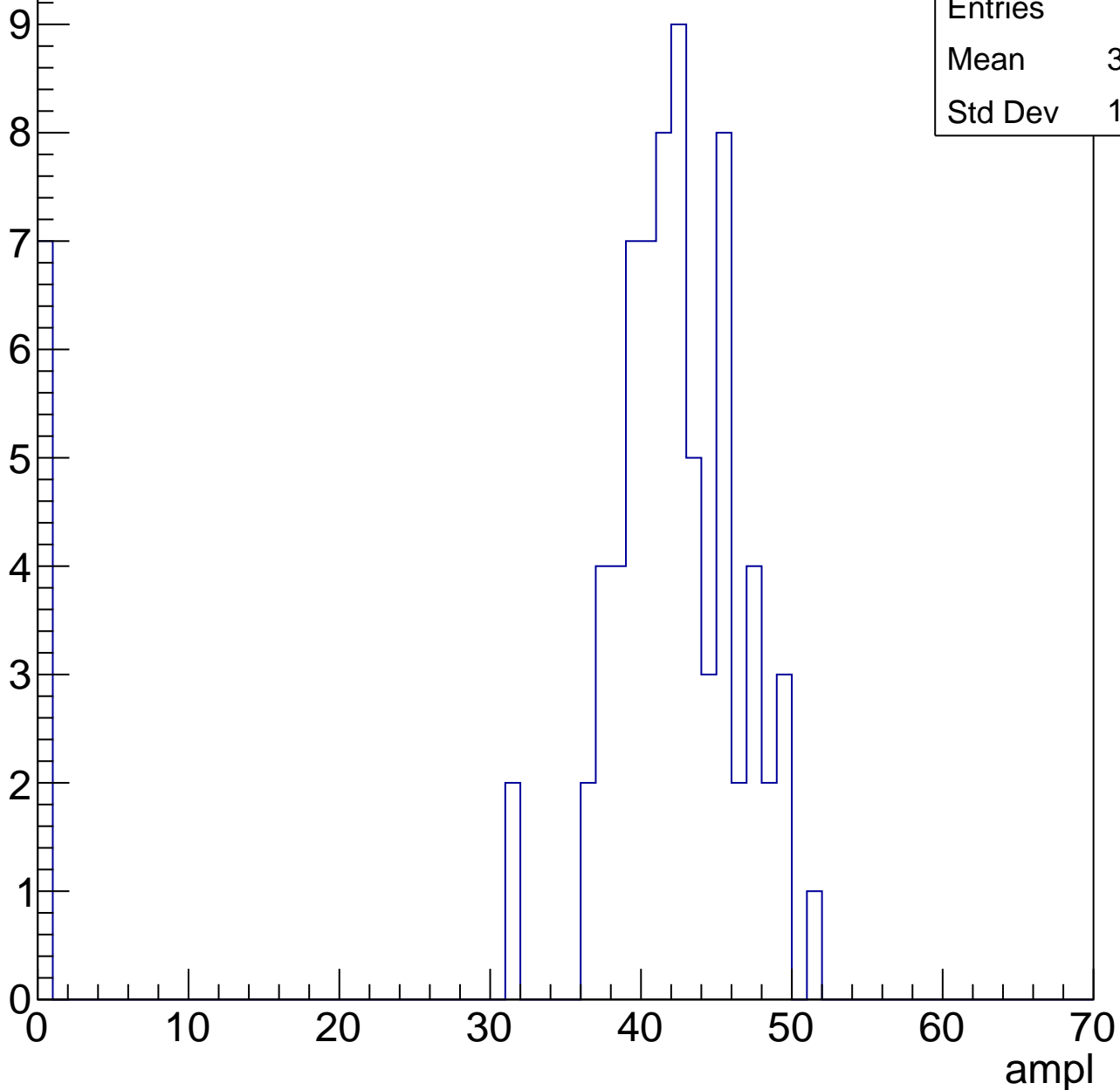


B1L103S, U5-ch117, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	38.13
Std Dev	12.55

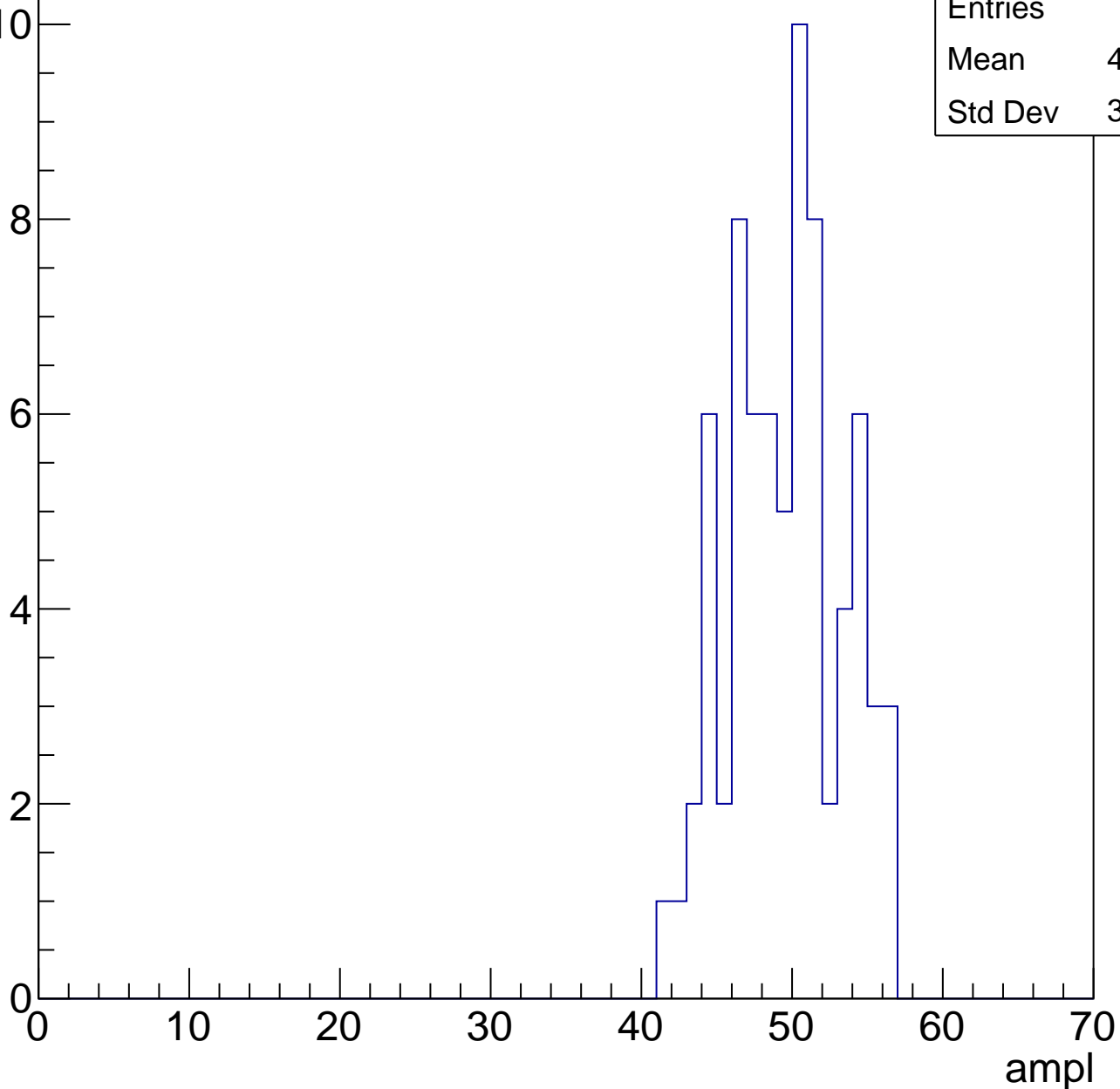


B1L103S, U5-ch117, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	49.14
Std Dev	3.695

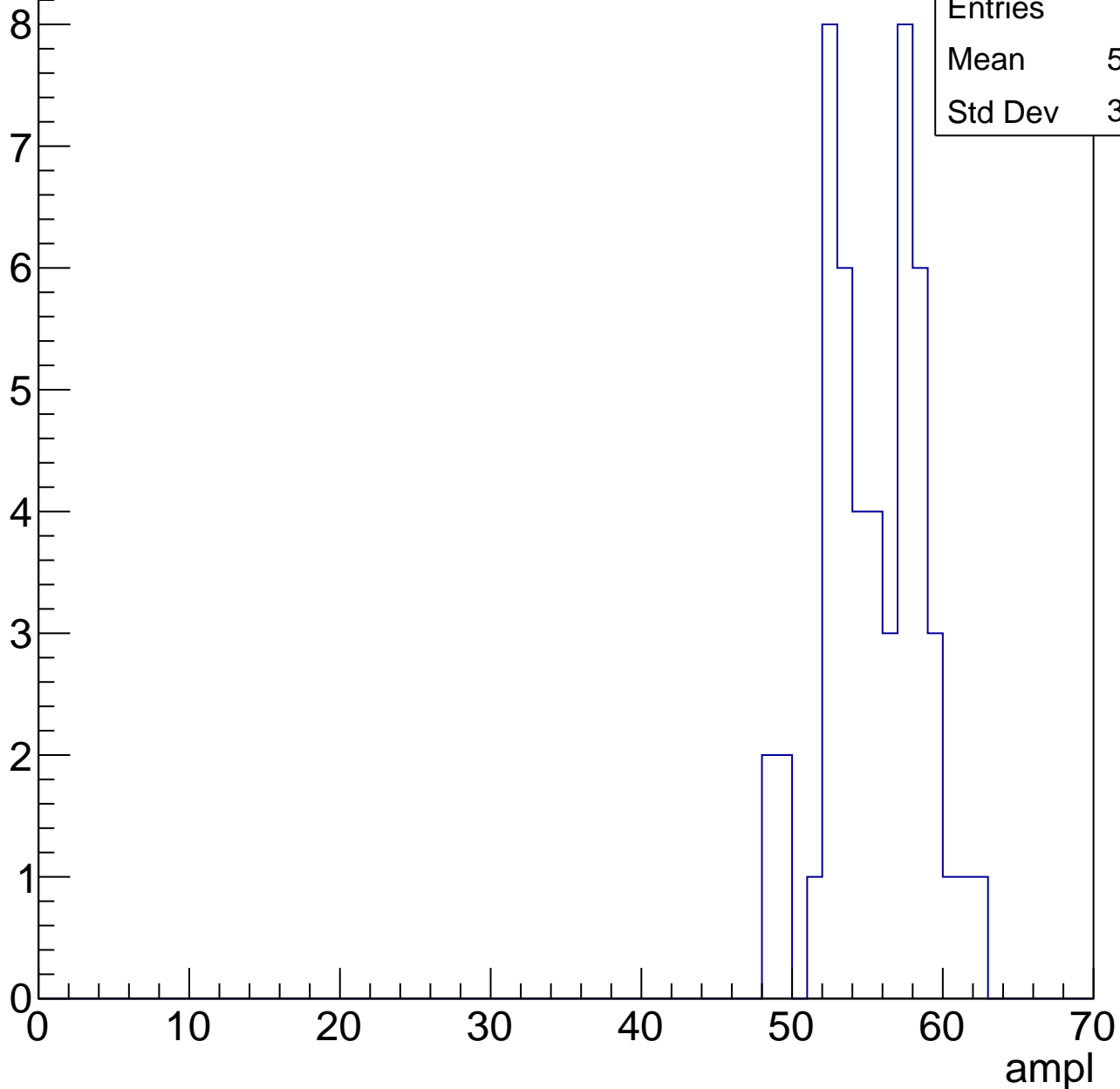


B1L103S, U5-ch117, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

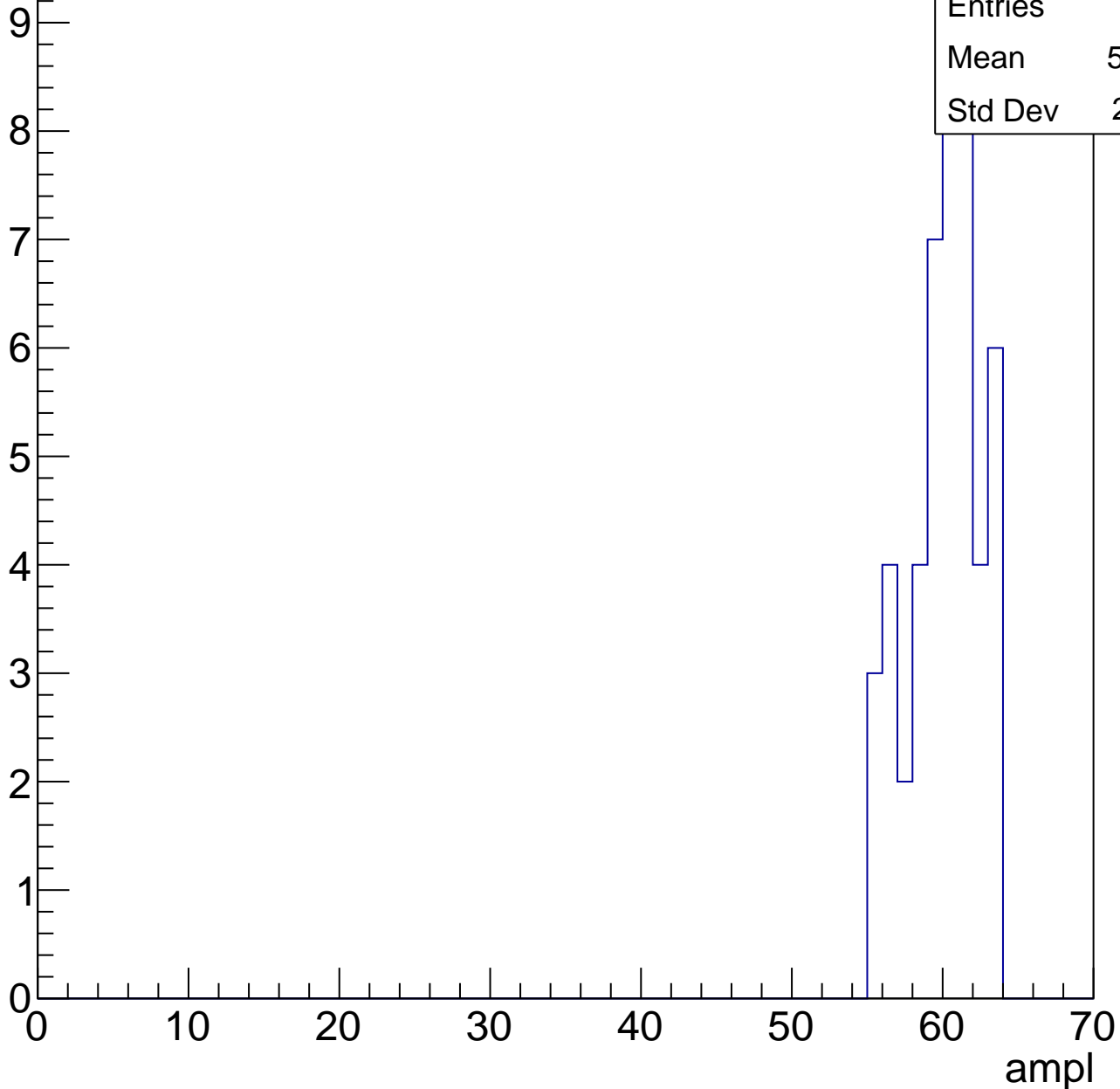
Entries	50
Mean	54.94
Std Dev	3.264



B1L103S, U5-ch117, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

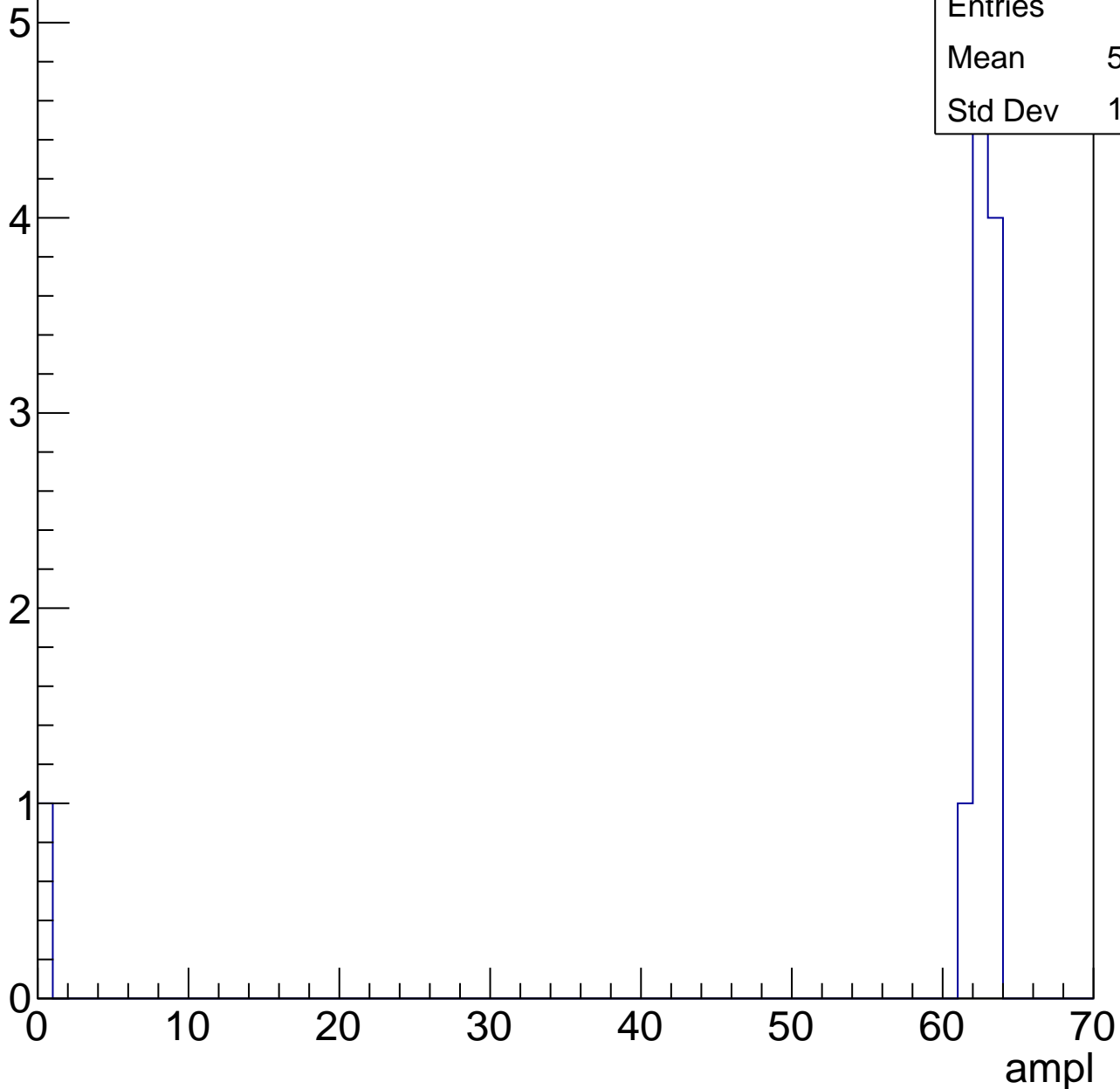


B1L103S, U5-ch117, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	11
Mean	56.64
Std Dev	17.92



B1L103S, U5-ch117, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	18
Mean	0
Std Dev	0

B1L103S, U5-ch118, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	84
Mean	23.51
Std Dev	9.665

Entry

10

8

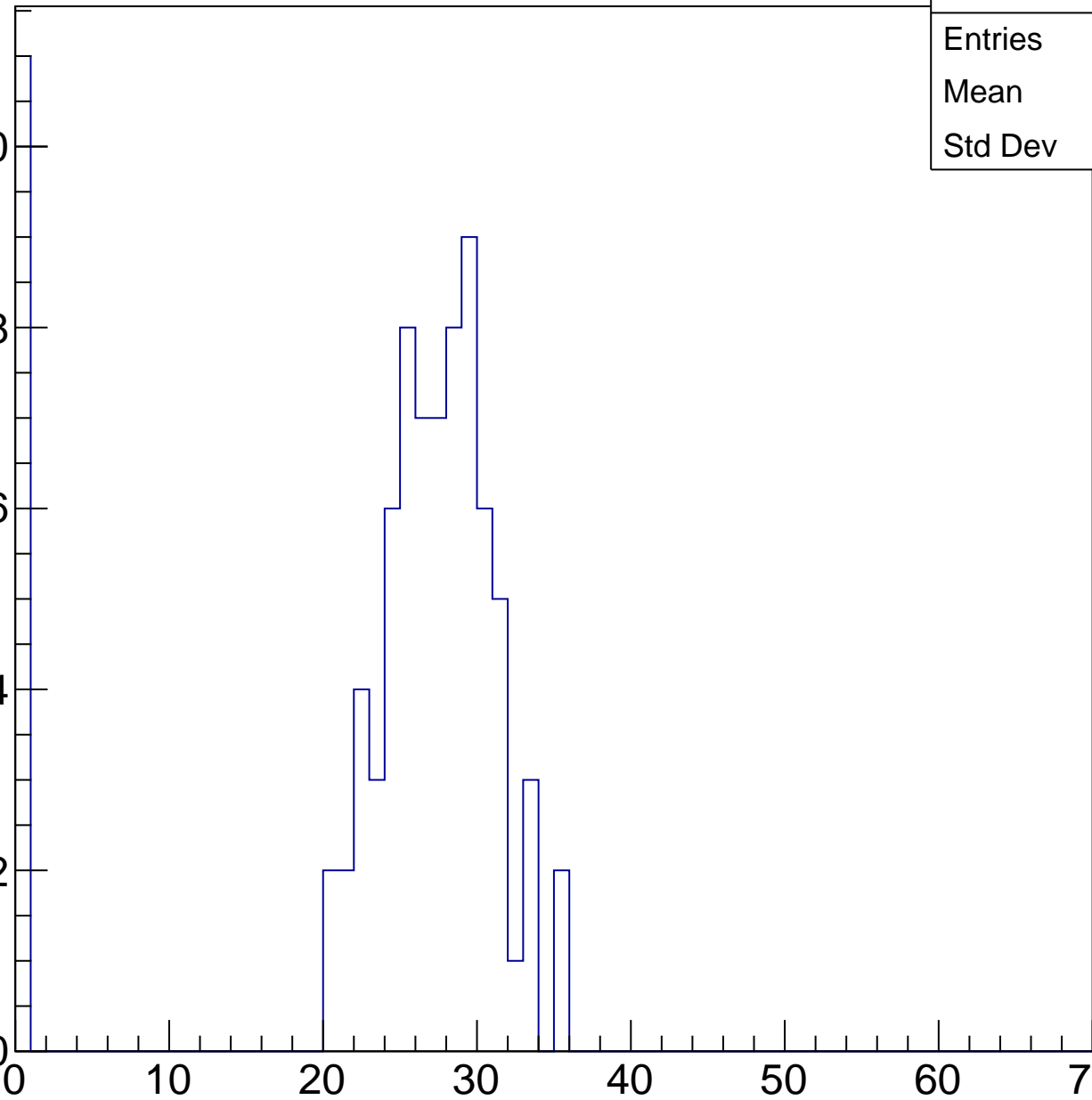
6

4

2

0

ampl

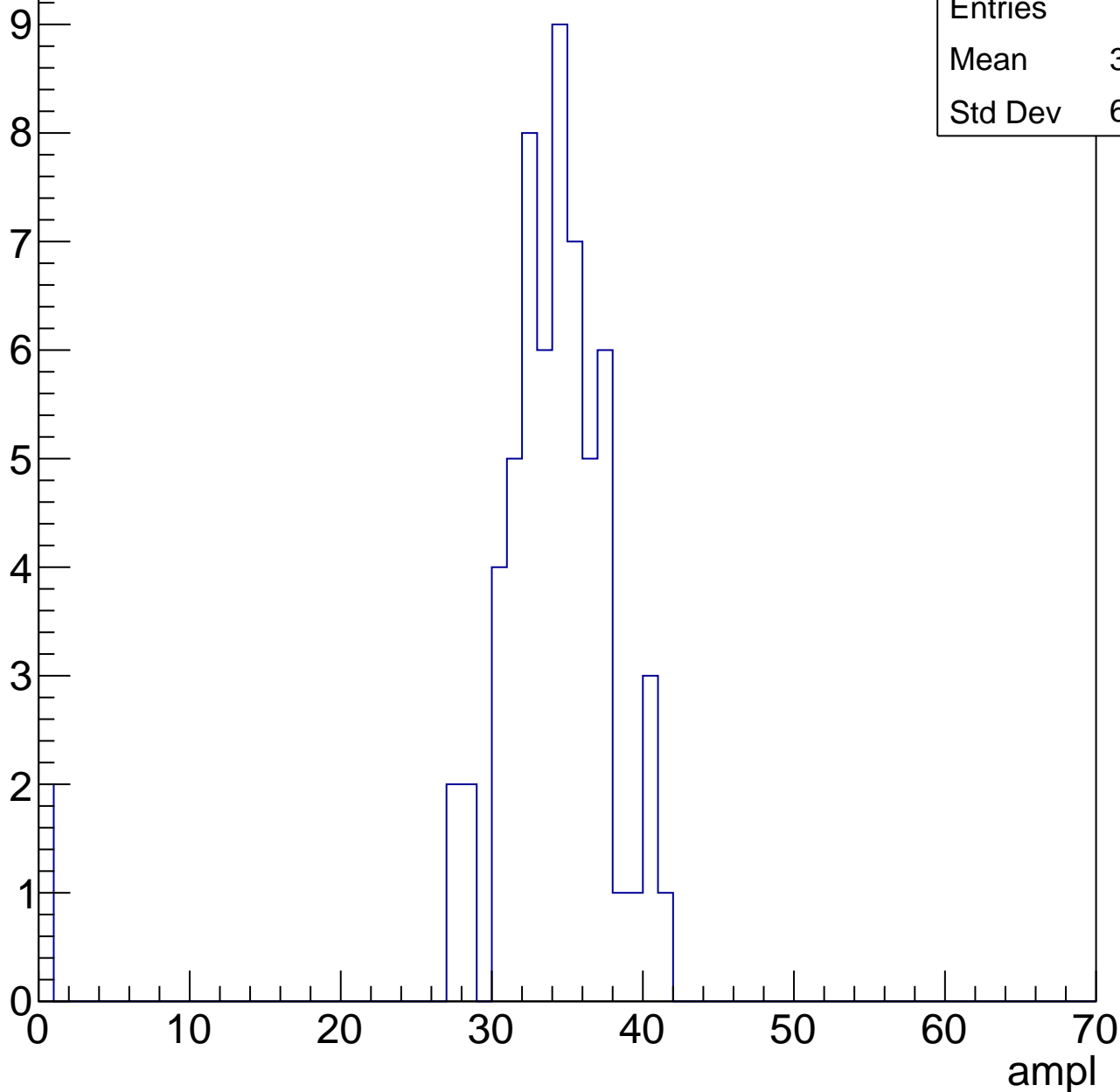


B1L103S, U5-ch118, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	32.74
Std Dev	6.732

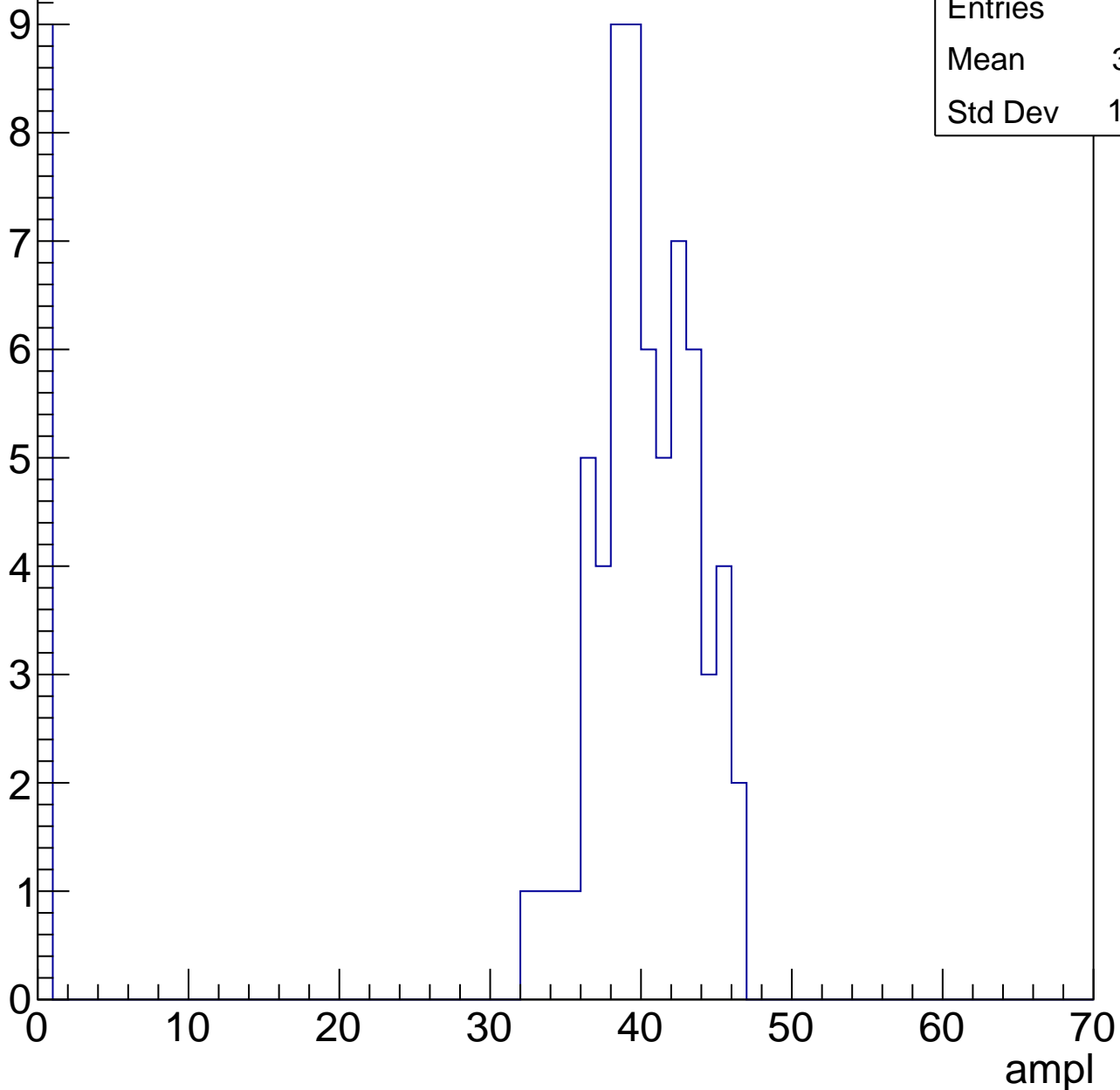


B1L103S, U5-ch118, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	35.01
Std Dev	13.46

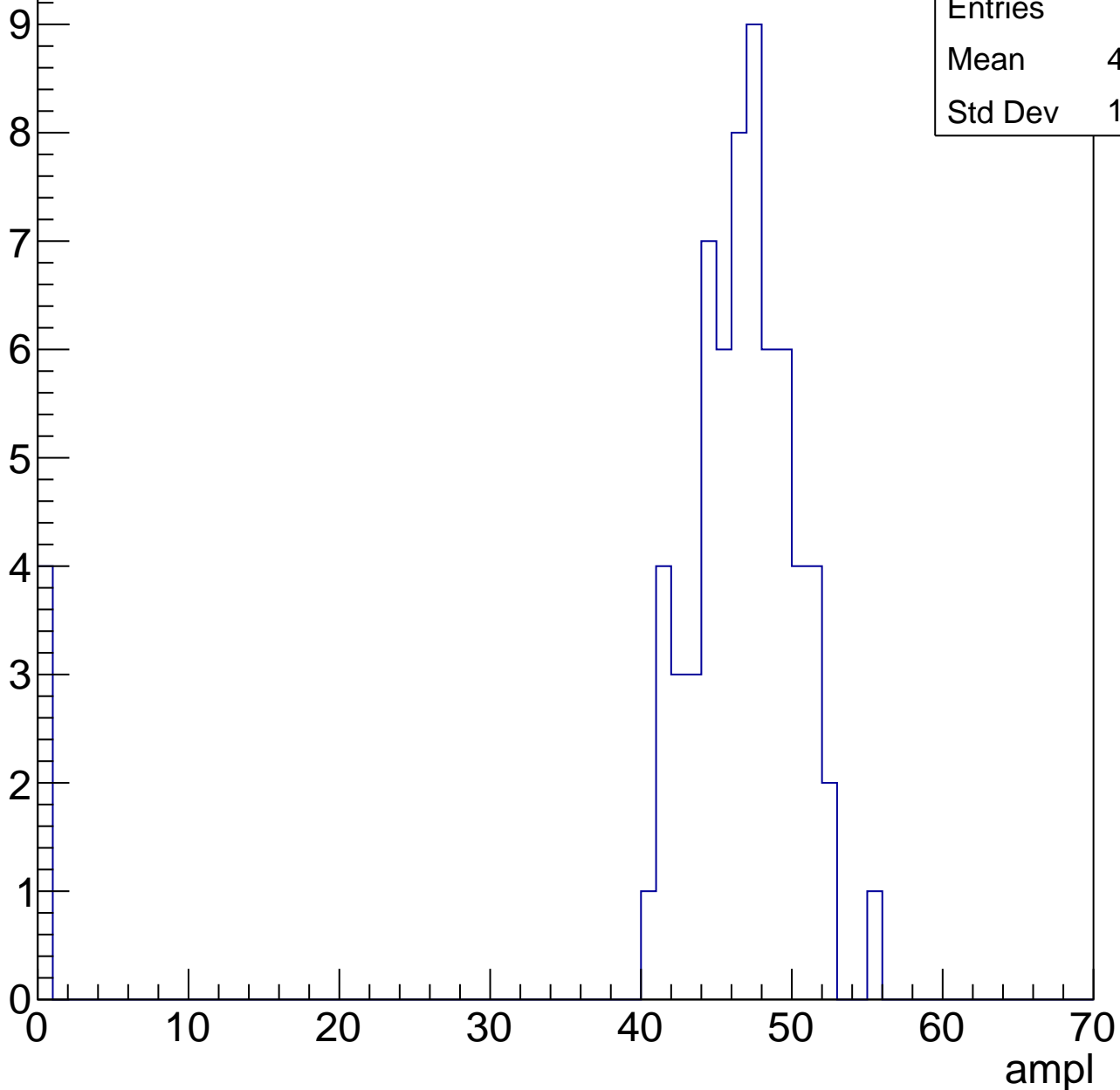


B1L103S, U5-ch118, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	43.72
Std Dev	11.35

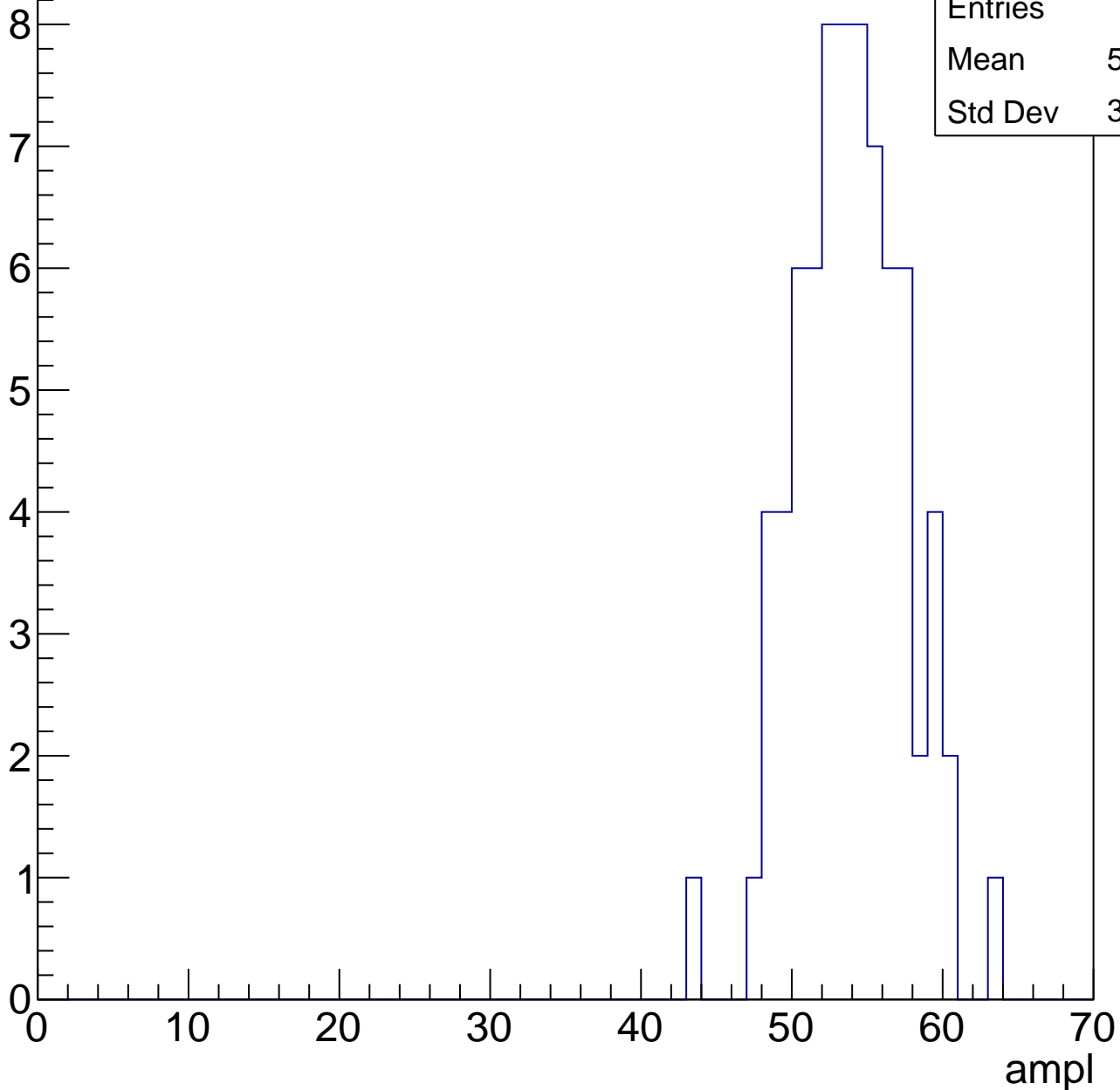


B1L103S, U5-ch118, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	53.43
Std Dev	3.583

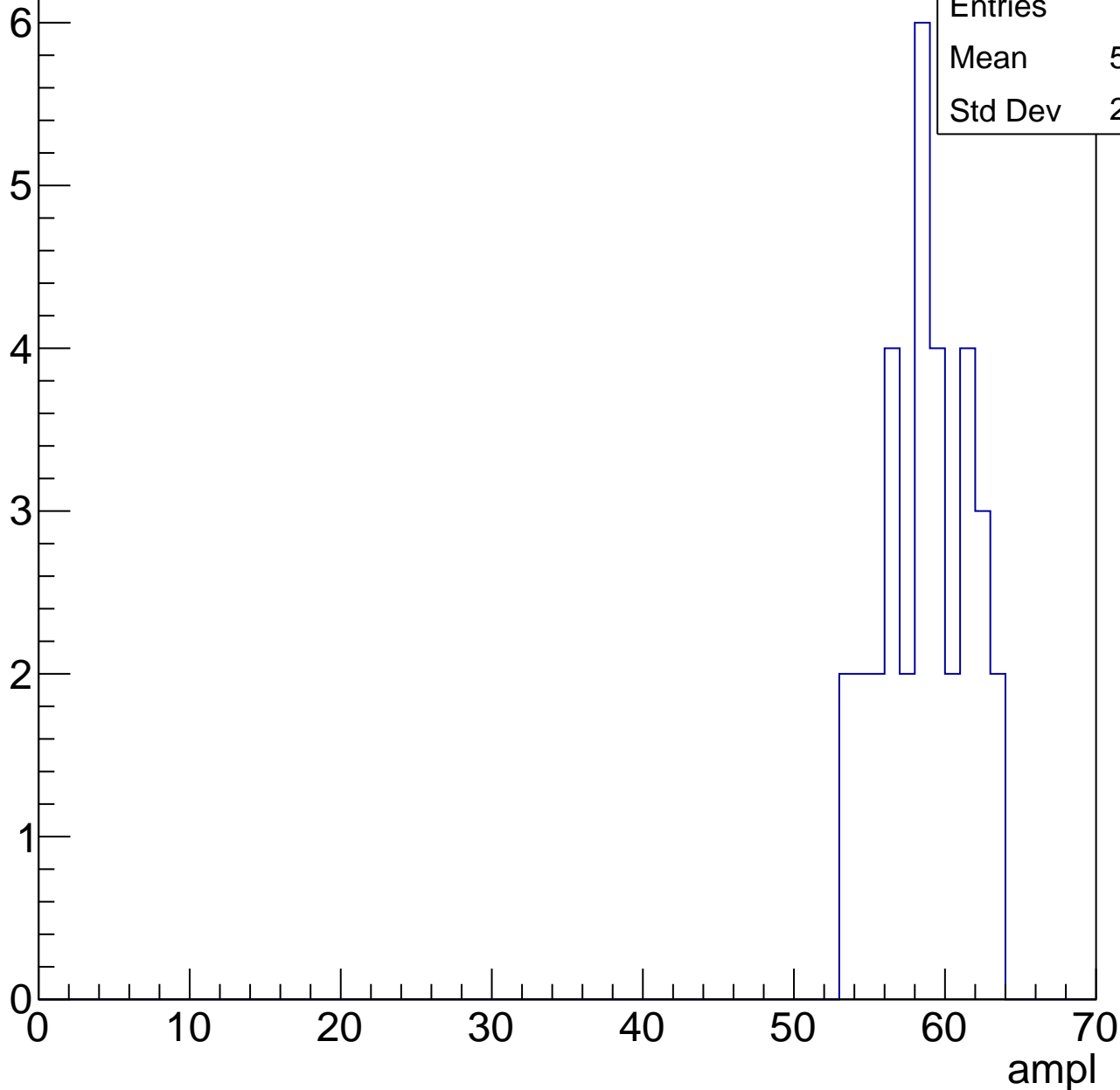


B1L103S, U5-ch118, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	33
Mean	58.24
Std Dev	2.818

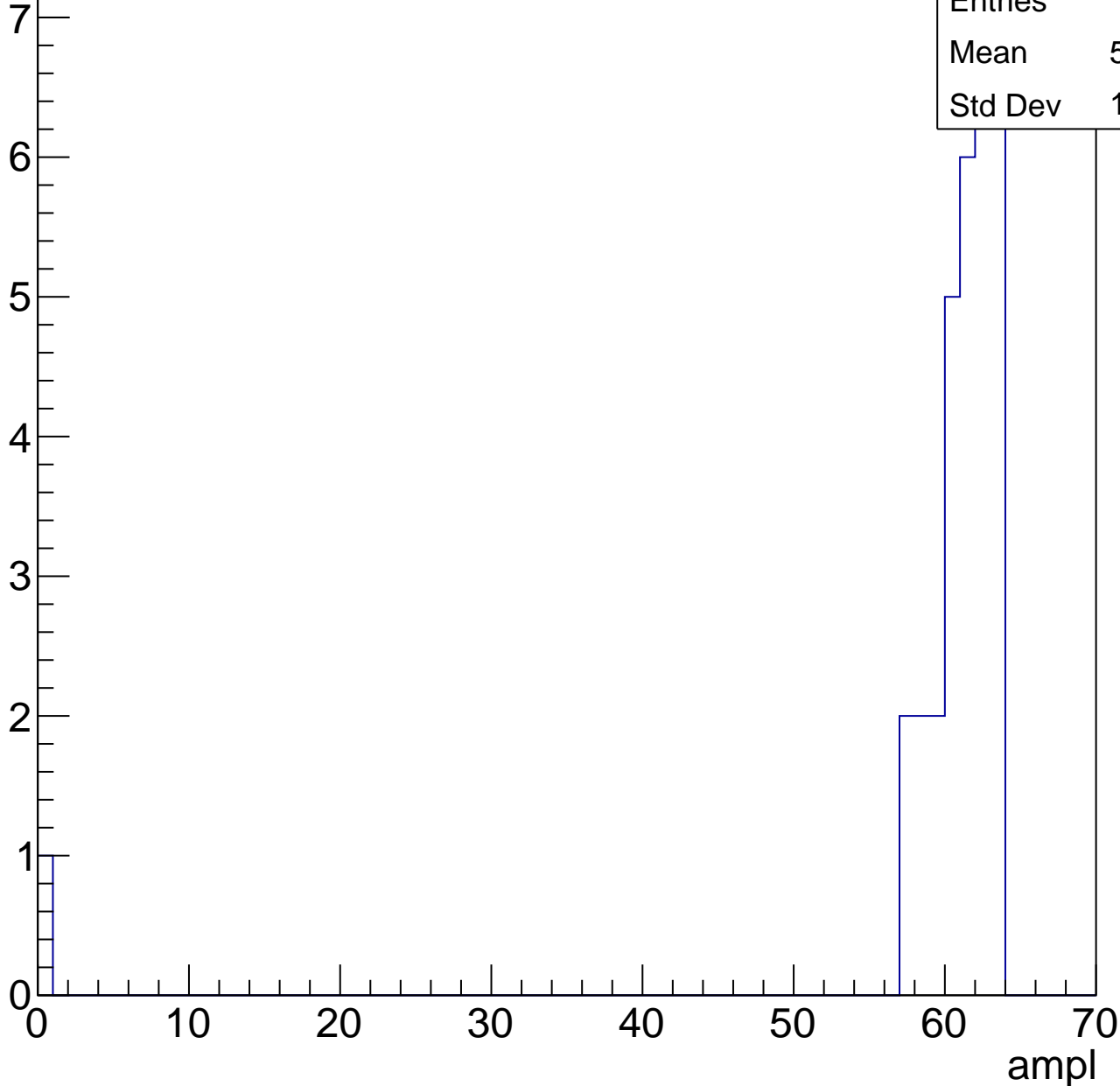


B1L103S, U5-ch118, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	32
Mean	59.03
Std Dev	10.75



B1L103S, U5-ch118, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3
Std Dev	13.08

Entry



B1L103S, U5-ch119, adc0

calib_packv5_041523_1651.root, FC#0, port C2

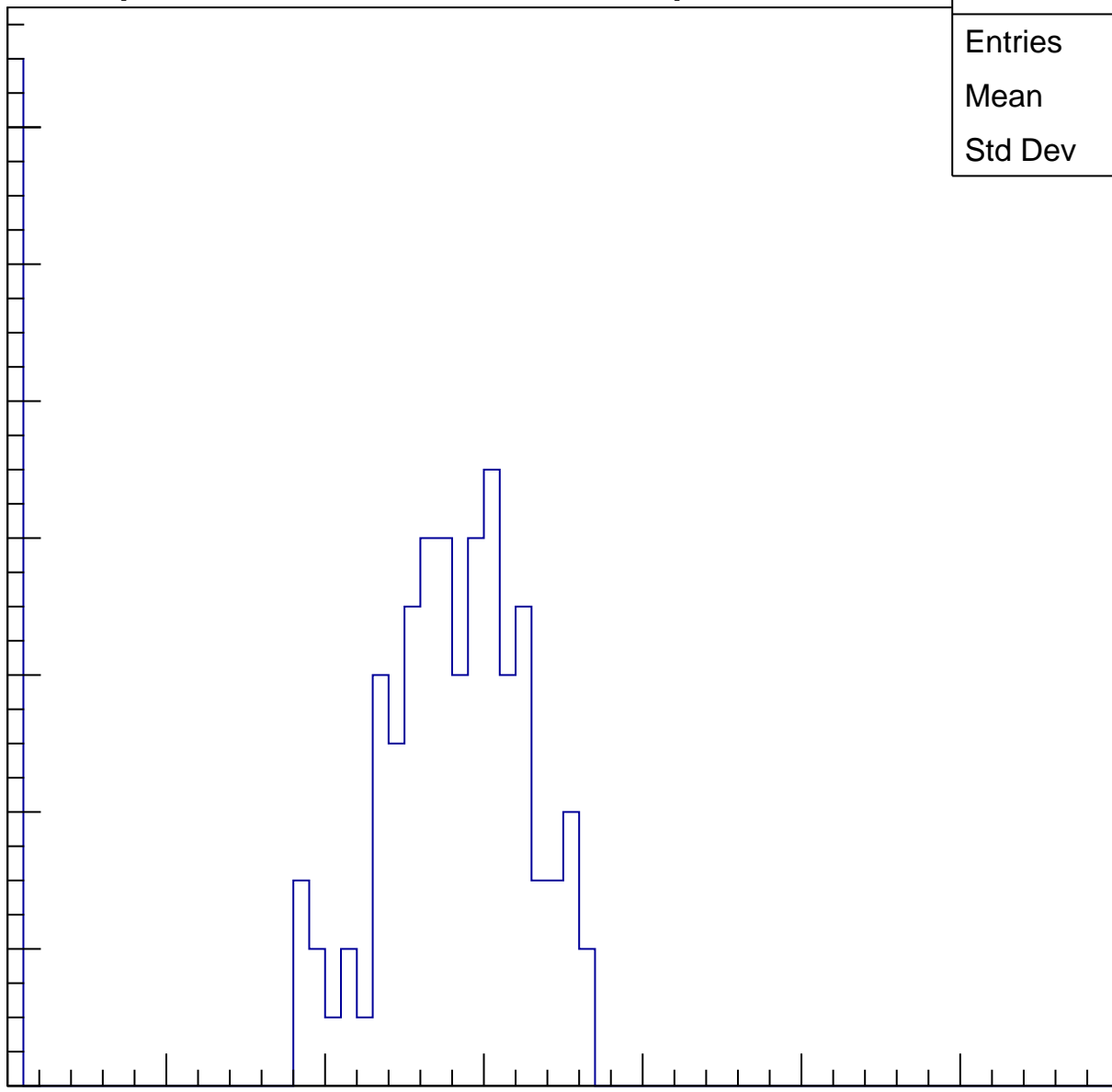
Entries	106
Mean	23.83
Std Dev	10.47

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

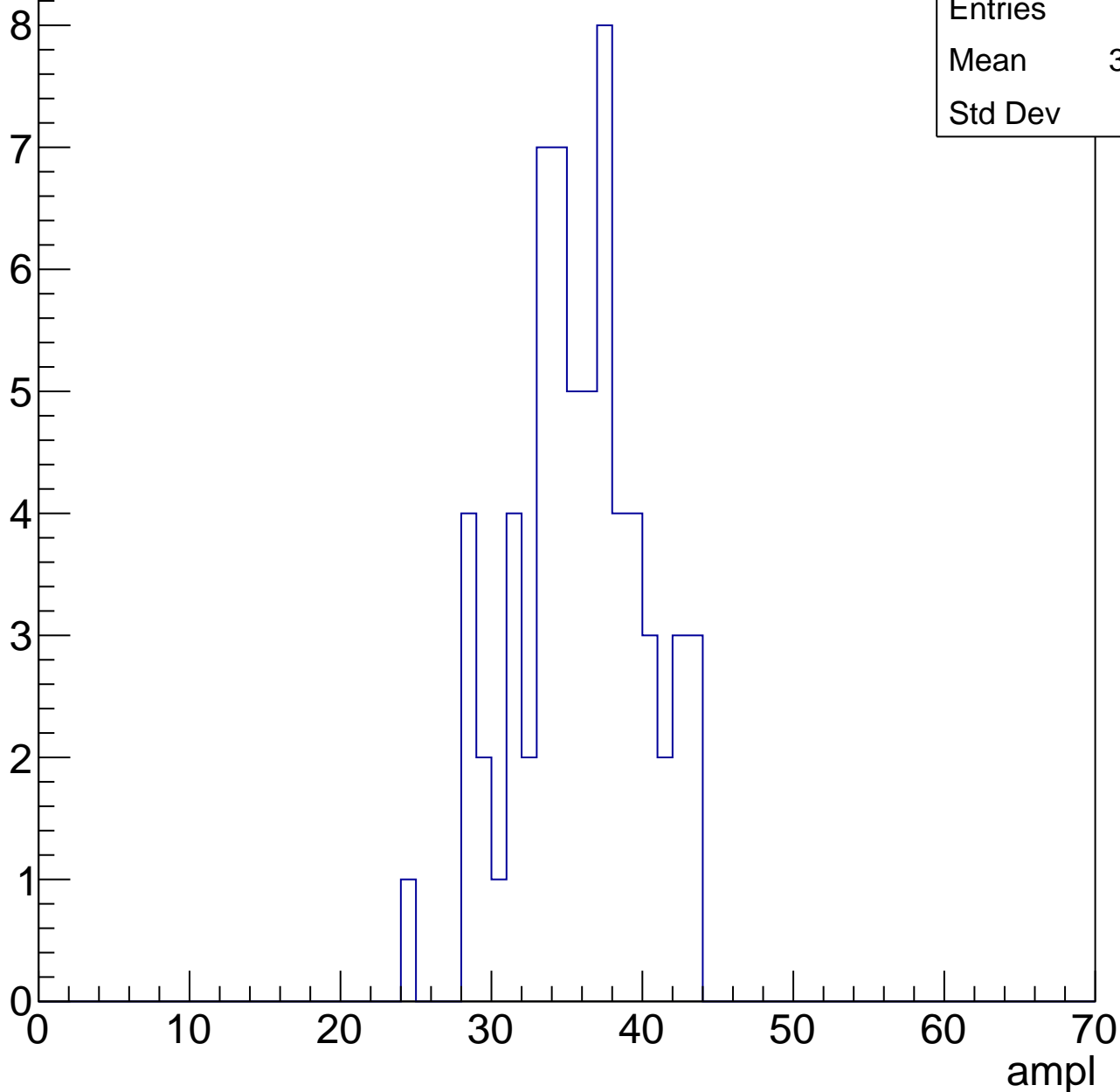


B1L103S, U5-ch119, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	35.34
Std Dev	4.2

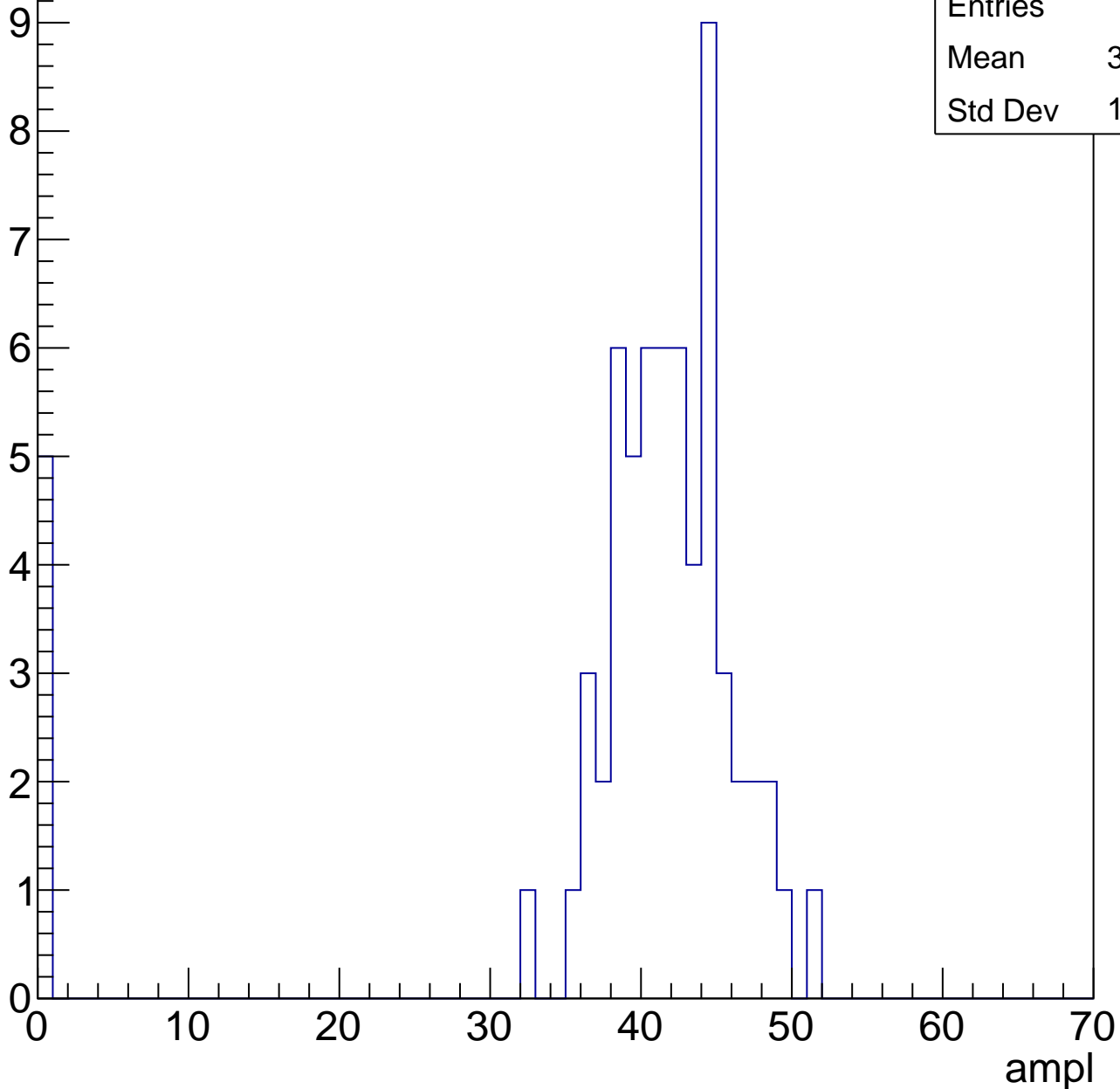


B1L103S, U5-ch119, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	38.38
Std Dev	11.64

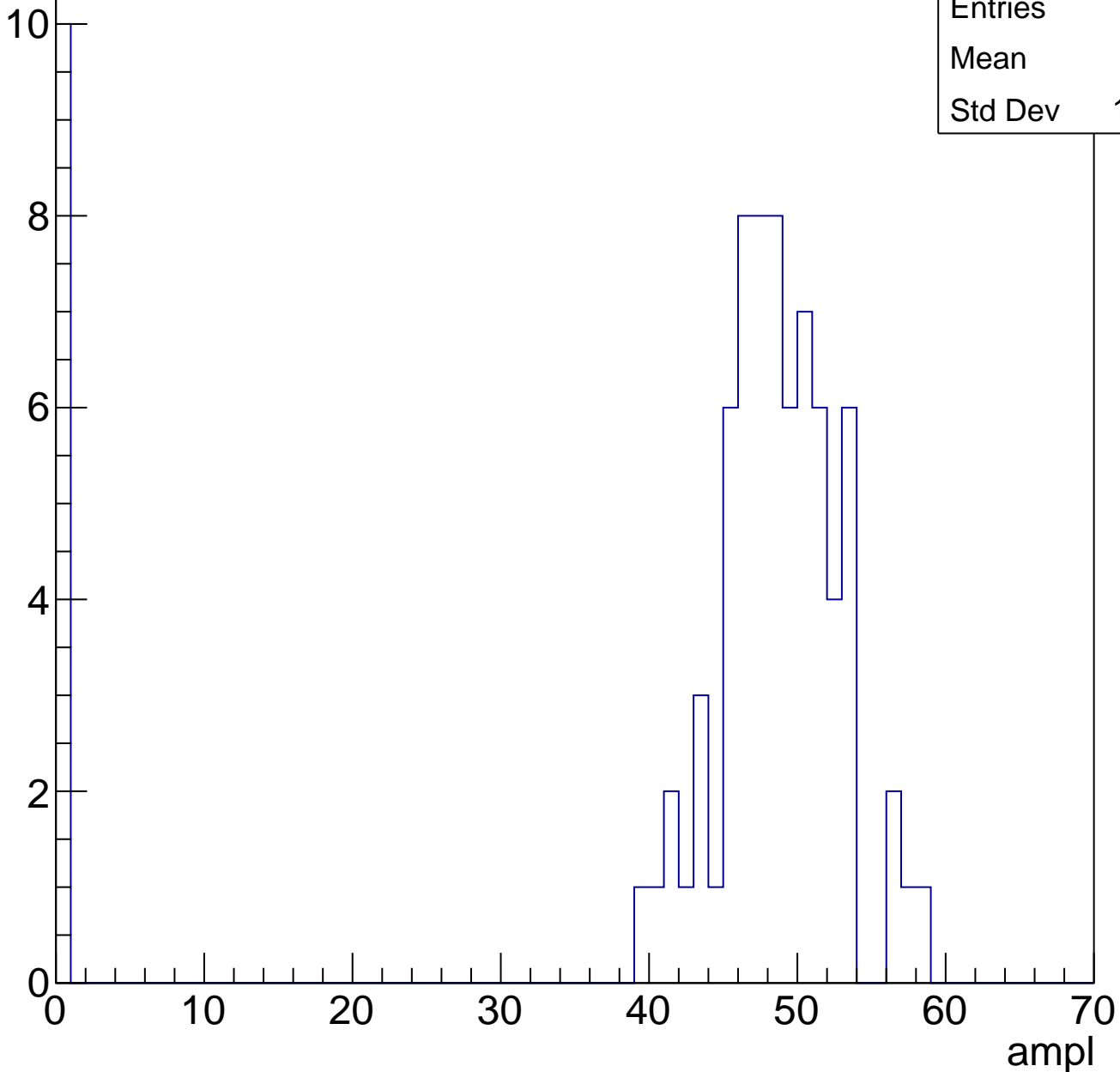


B1L103S, U5-ch119, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	42.4
Std Dev	16.21

Entry

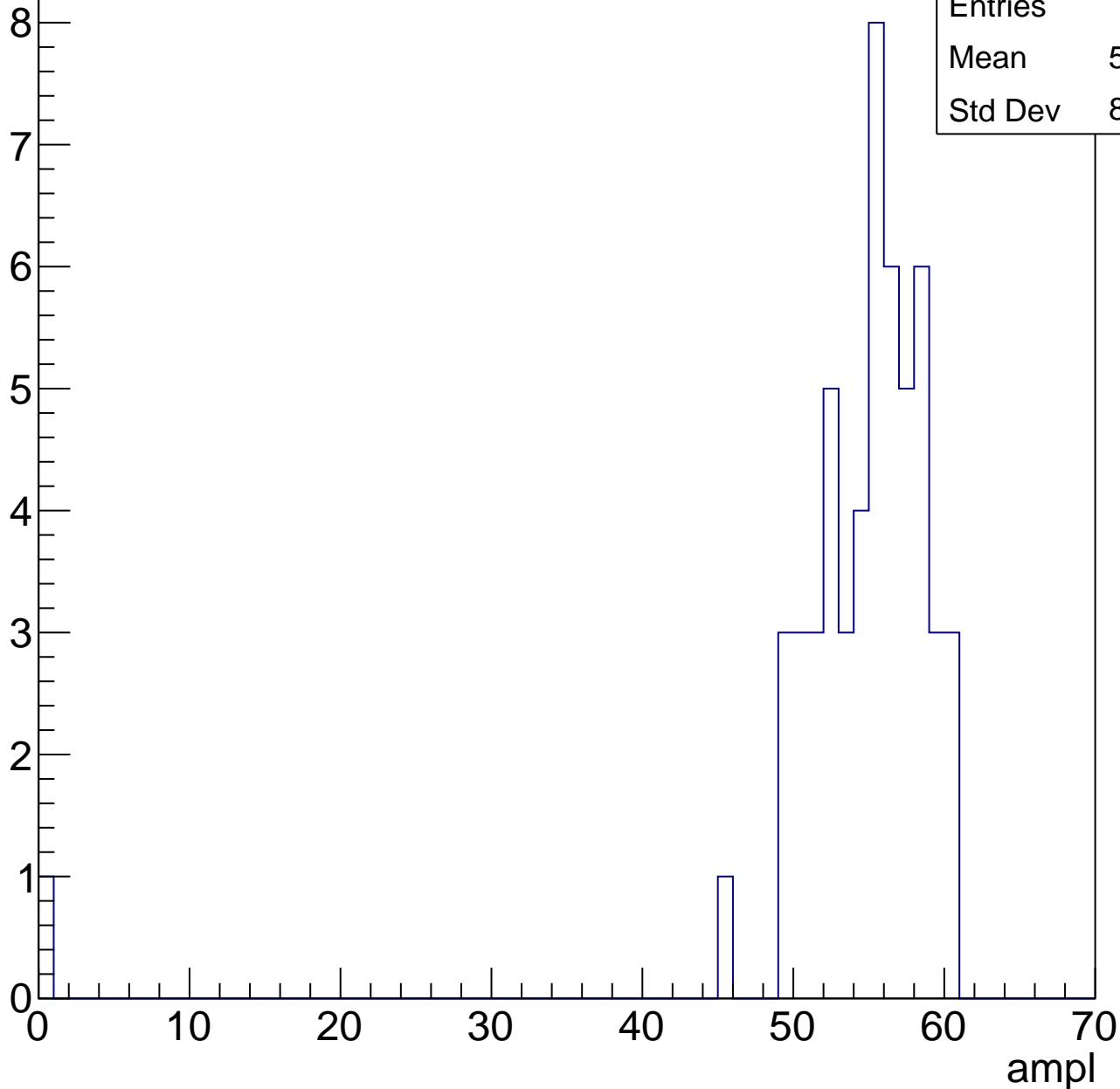


B1L103S, U5-ch119, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	53.63
Std Dev	8.072

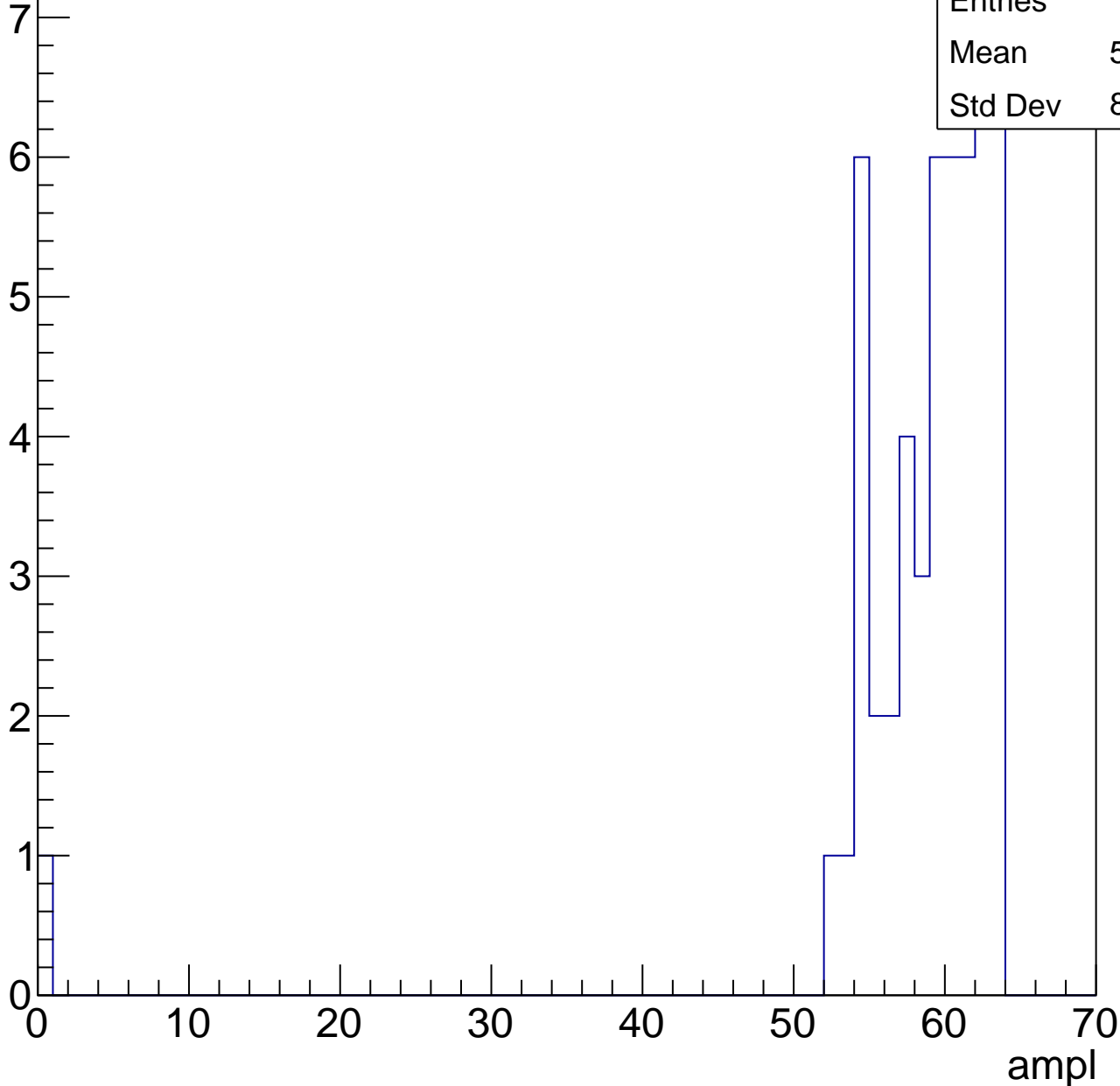


B1L103S, U5-ch119, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

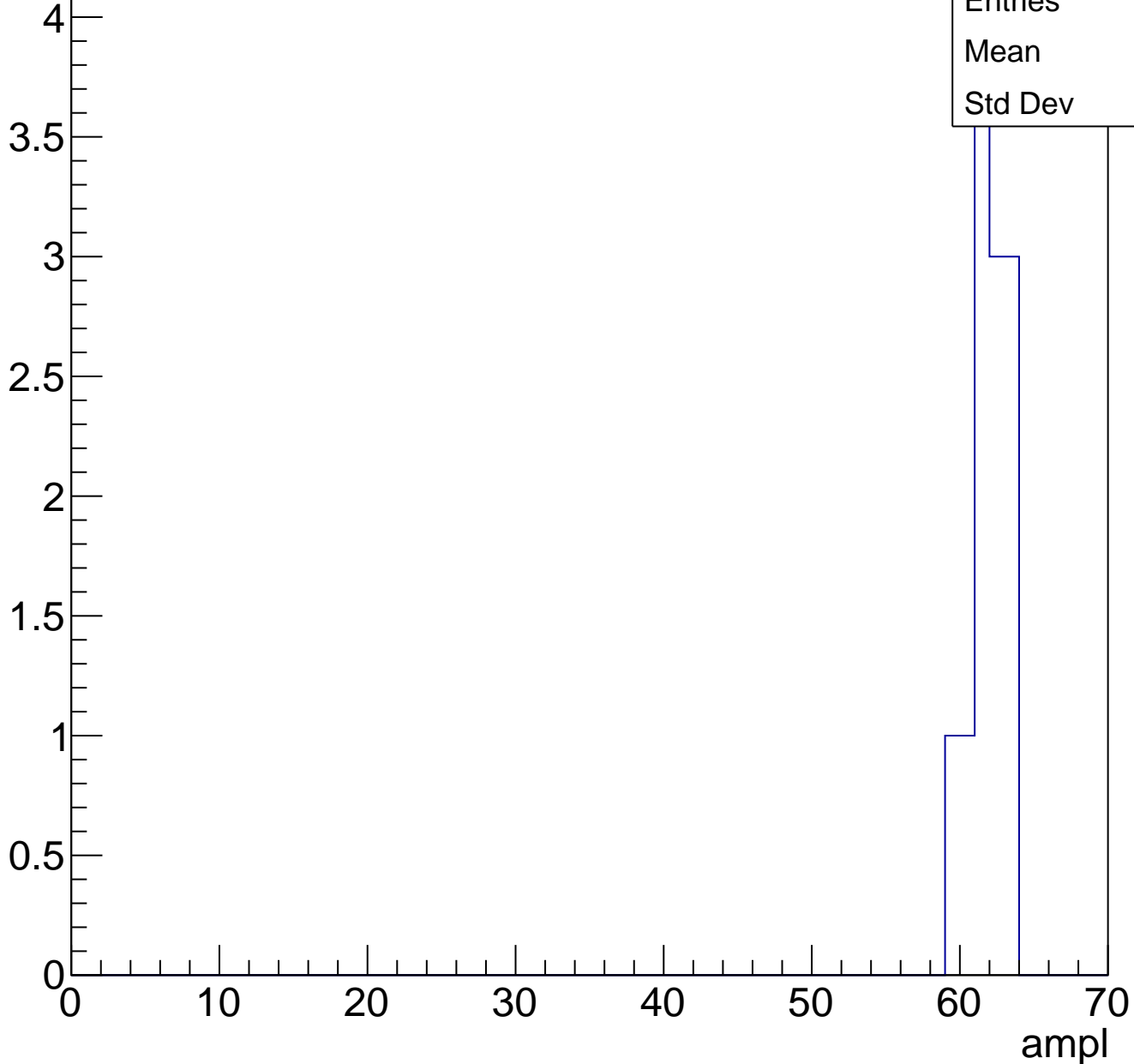
Entries	52
Mean	57.85
Std Dev	8.683



B1L103S, U5-ch119, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch119, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

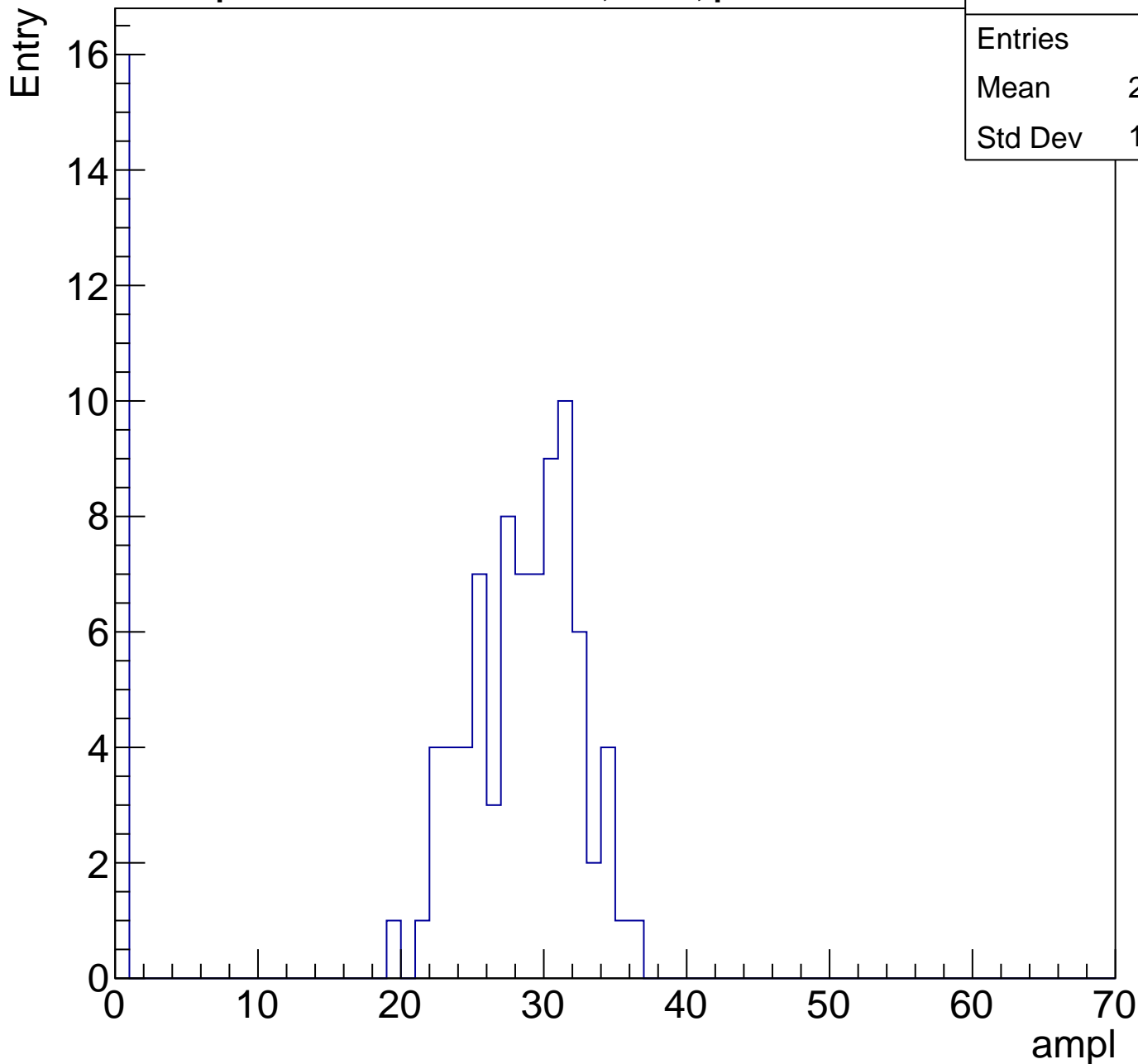


Entries	19
Mean	0
Std Dev	0

B1L103S, U5-ch120, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	95
Mean	23.46
Std Dev	11.07

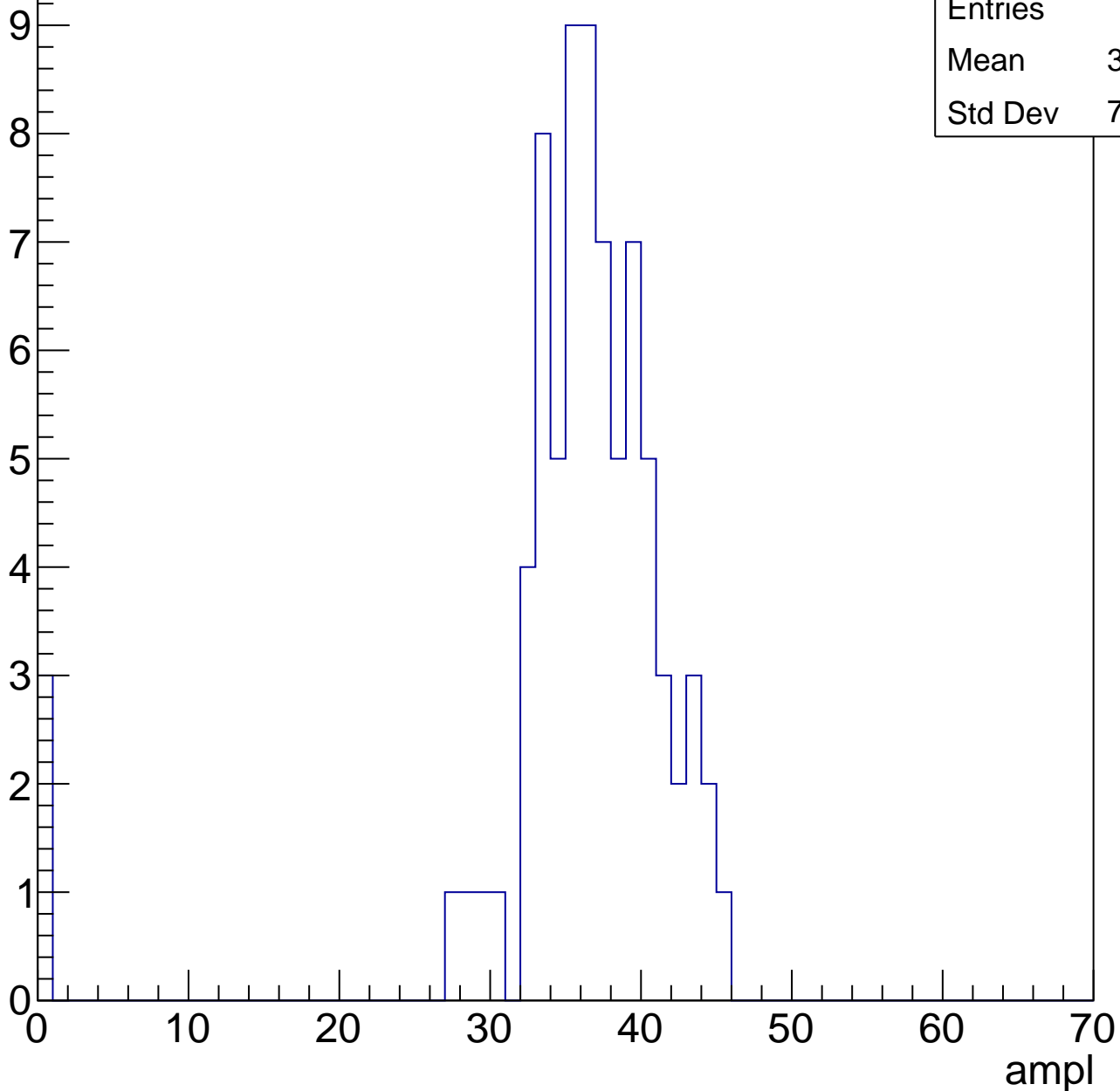


B1L103S, U5-ch120, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	35.14
Std Dev	7.977



B1L103S, U5-ch120, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	52
Mean	32.67
Std Dev	17.14

Entry

10

8

6

4

2

0

0

10

20

30

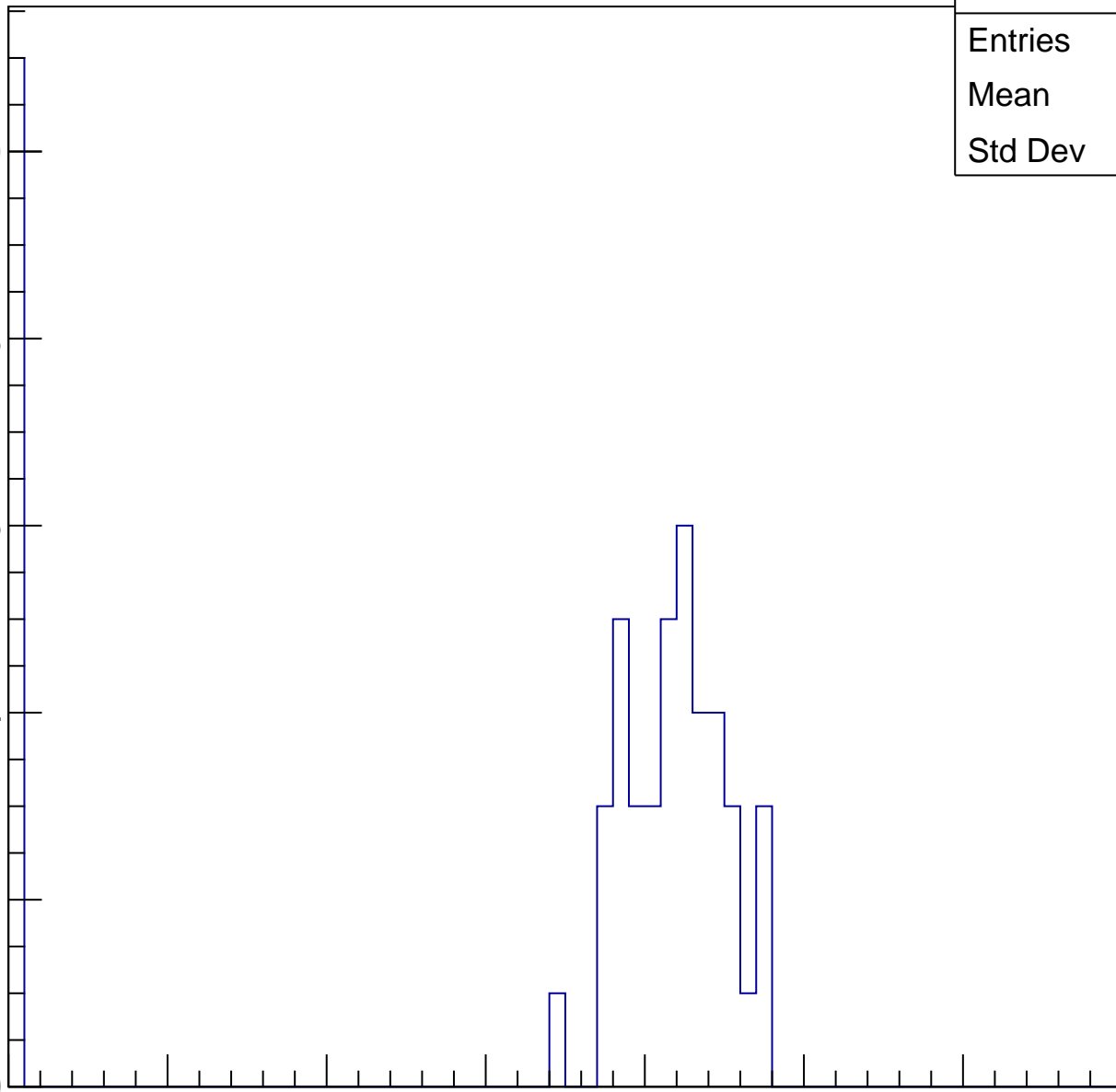
40

50

60

70

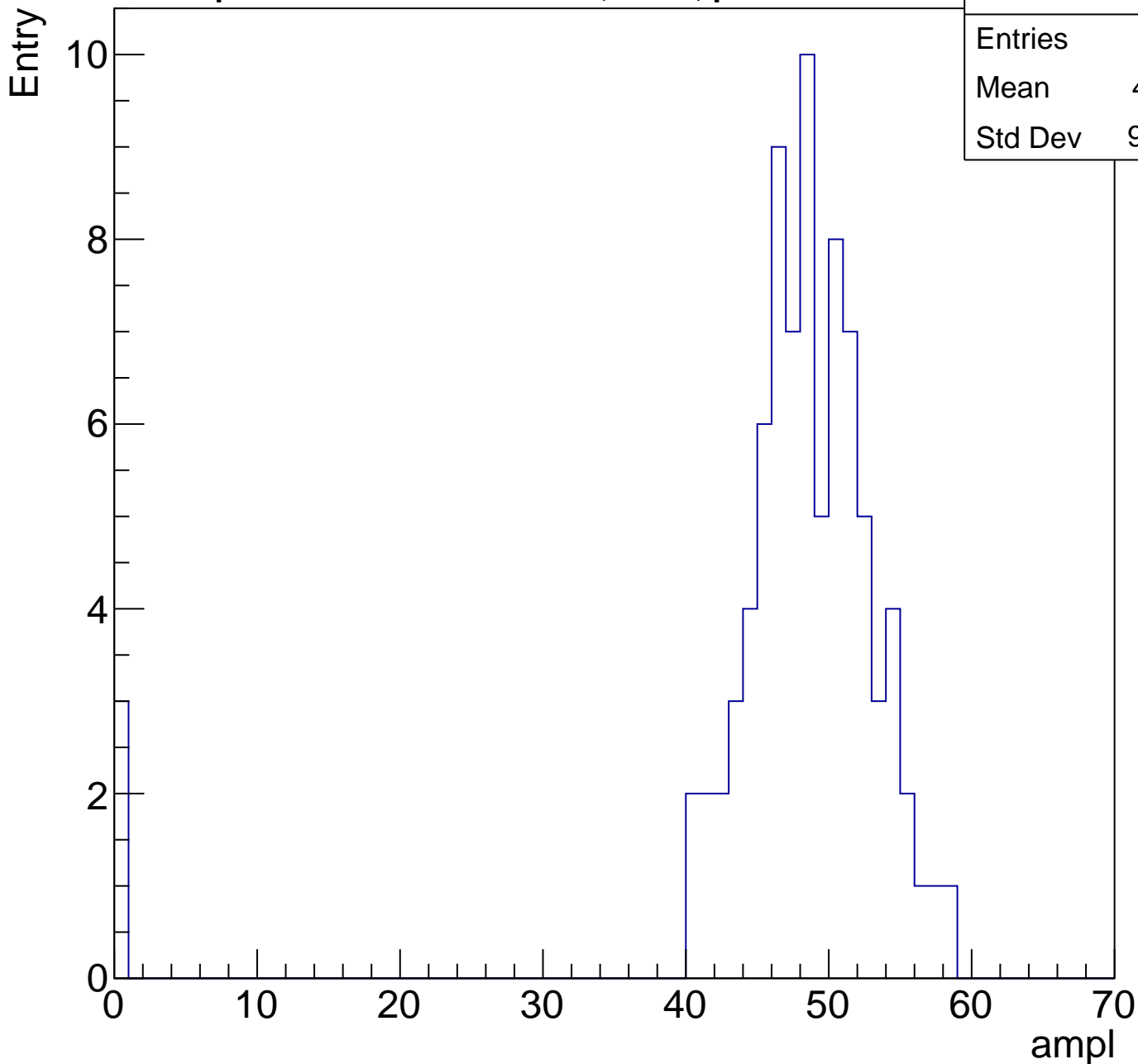
ampl



B1L103S, U5-ch120, adc3

calib_packv5_041523_1651.root, FC#0, port C2

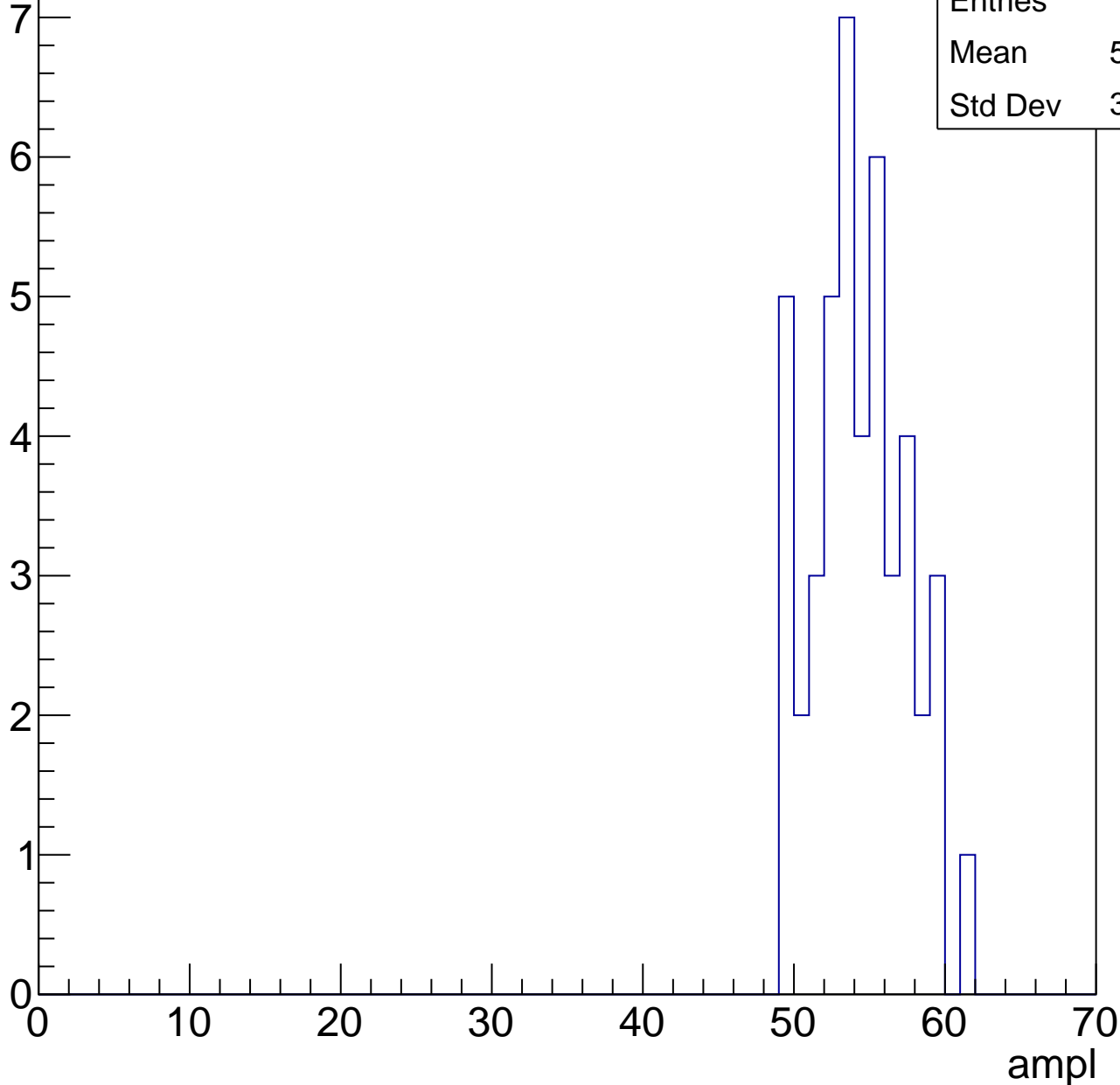
Entries	85
Mean	46.61
Std Dev	9.716



B1L103S, U5-ch120, adc4

calib_packv5_041523_1651.root, FC#0, port C2

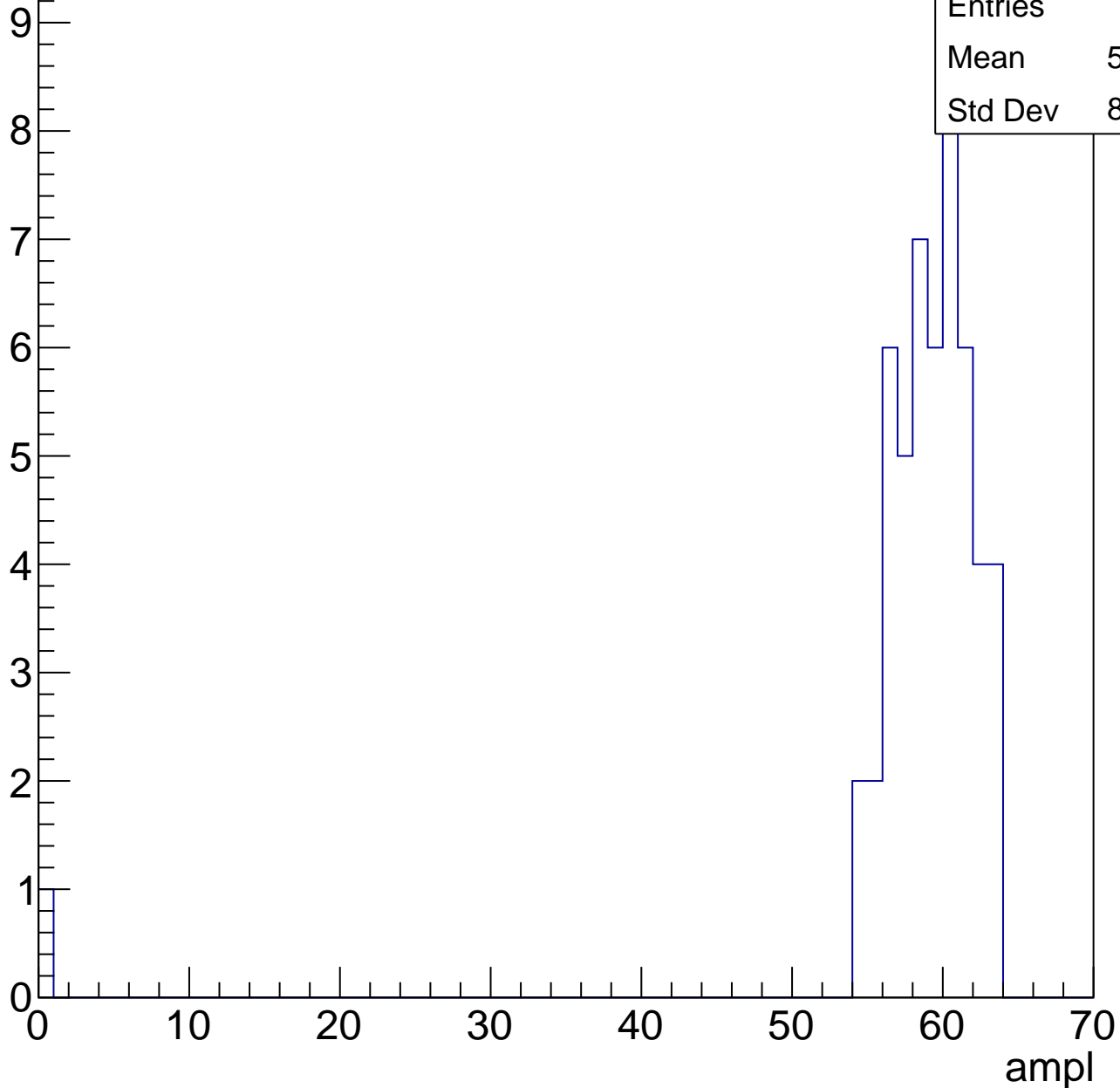
Entry



B1L103S, U5-ch120, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

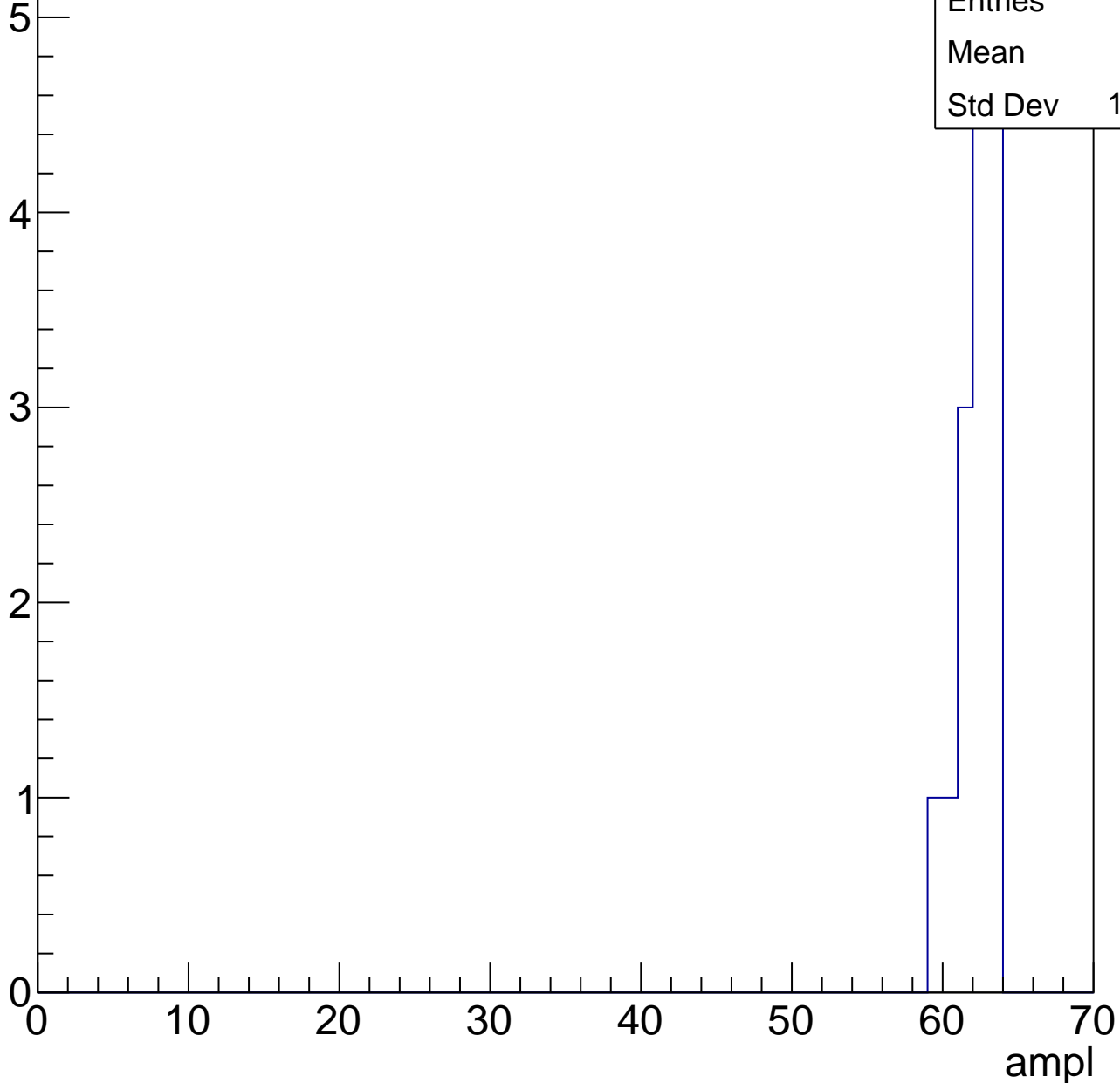


B1L103S, U5-ch120, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	15
Mean	61.8
Std Dev	1.166



B1L103S, U5-ch120, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	5.952
Std Dev	18.35

Entry



B1L103S, U5-ch121, adc0

calib_packv5_041523_1651.root, FC#0, port C2

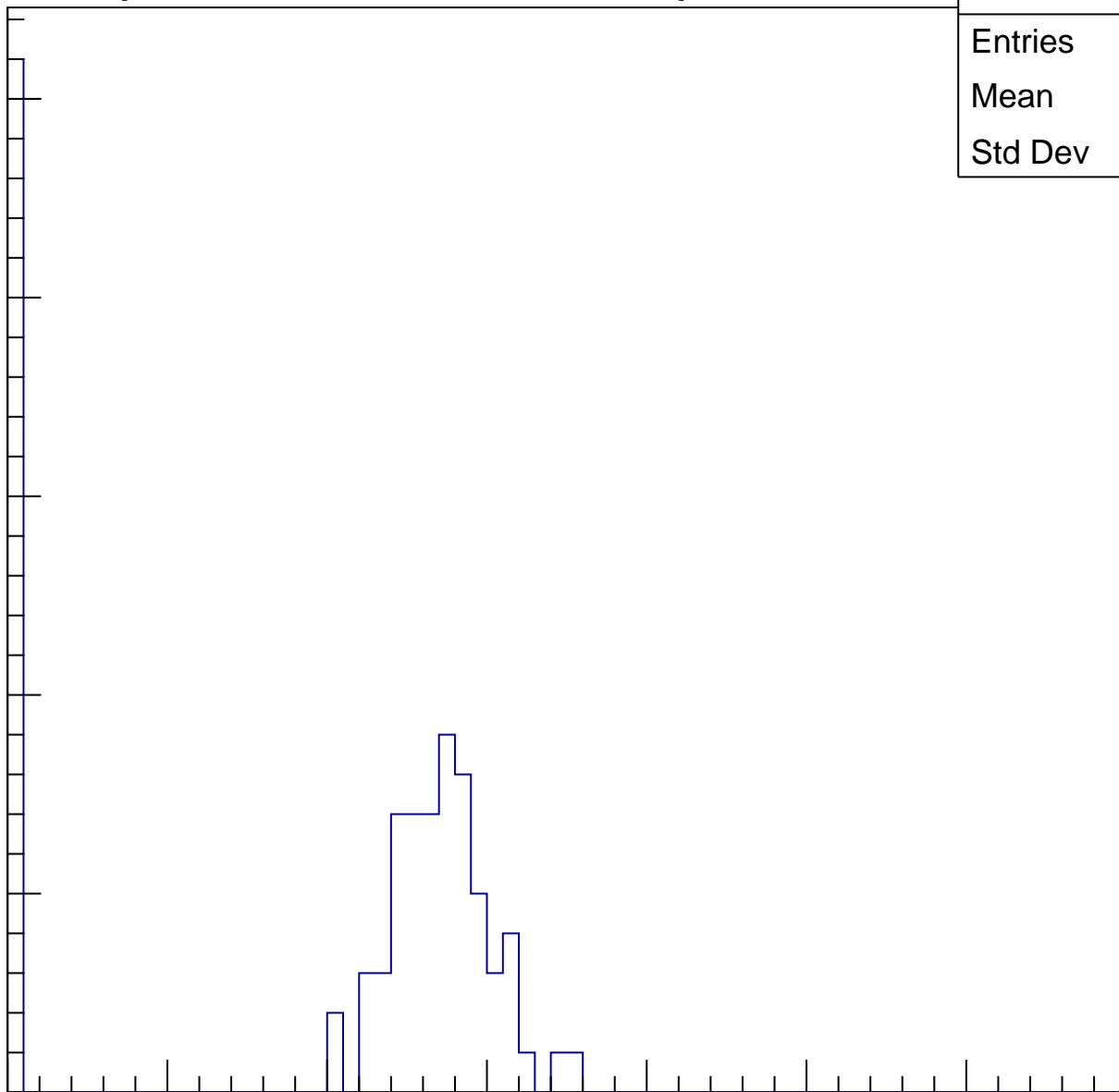
Entries	87
Mean	18.7
Std Dev	12.47

Entry

25
20
15
10
5
0

0 10 20 30 40 50 60 70

ampl



B1L103S, U5-ch121, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	85
Mean	32.71
Std Dev	7.199

Entry

10

8

6

4

2

0

0

10

20

30

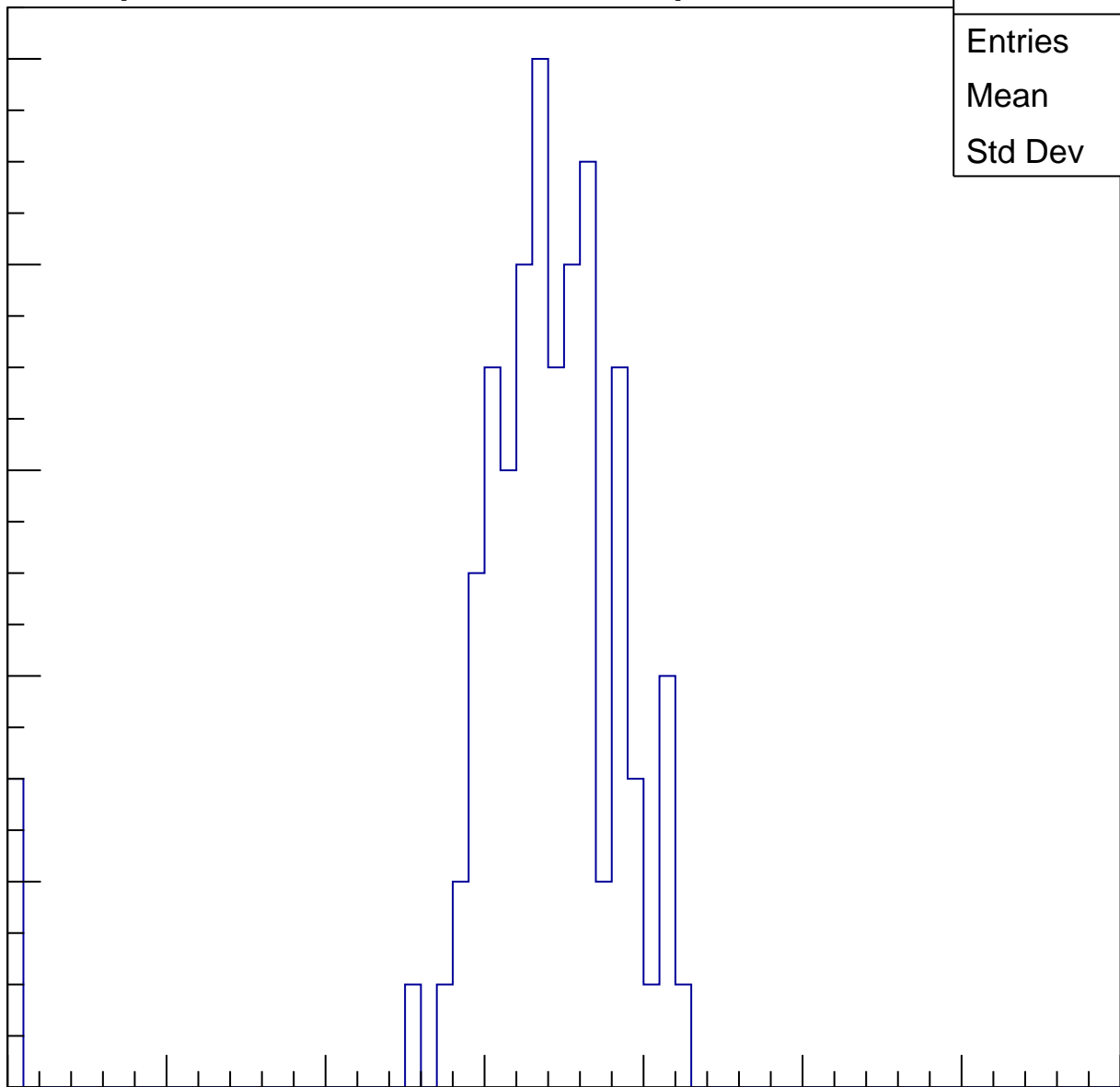
40

50

60

70

ampl



B1L103S, U5-ch121, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	84
Mean	35
Std Dev	15.42

Entry

12

10

8

6

4

2

0

0

10

20

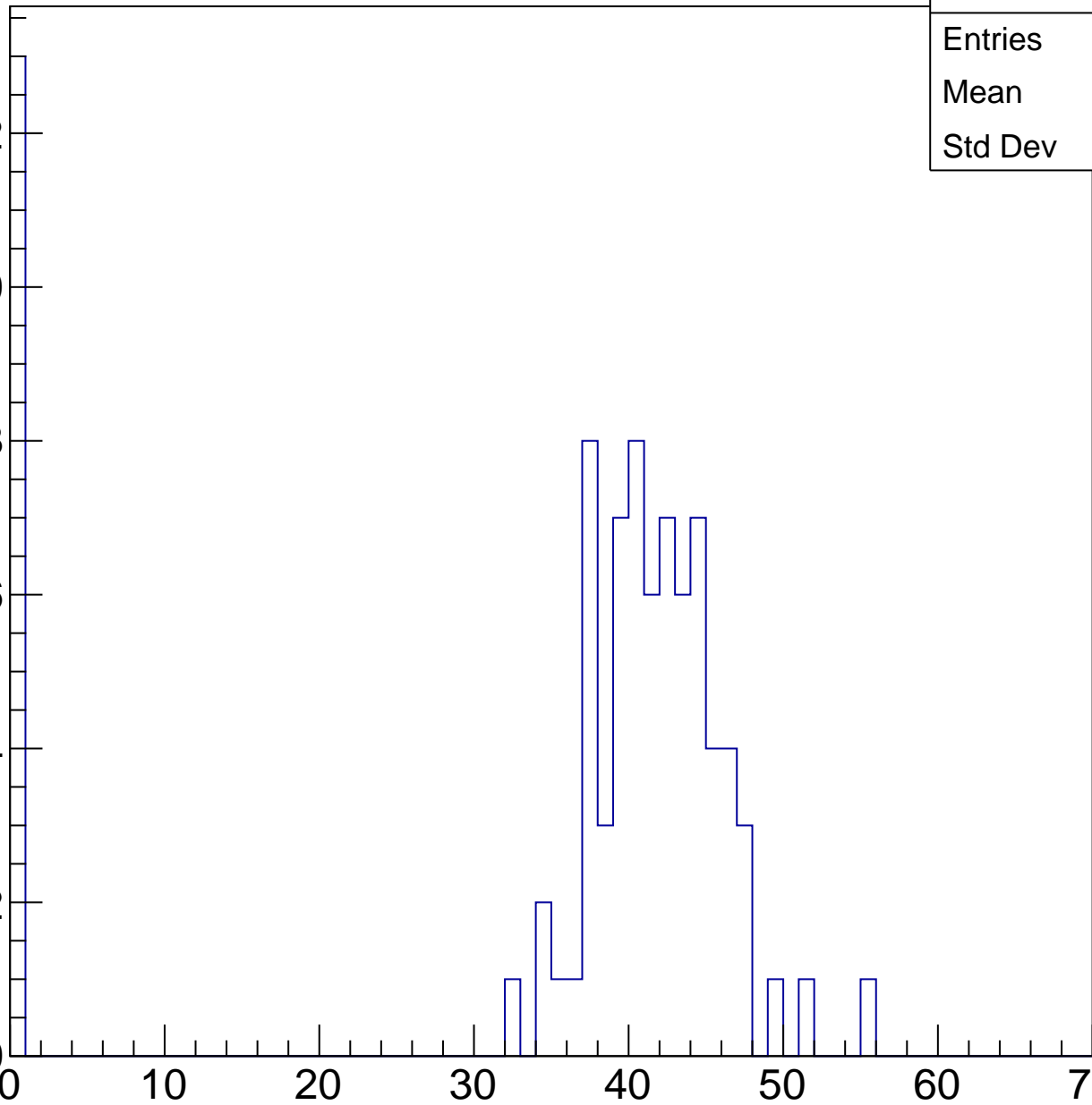
30

40

50

60

ampl

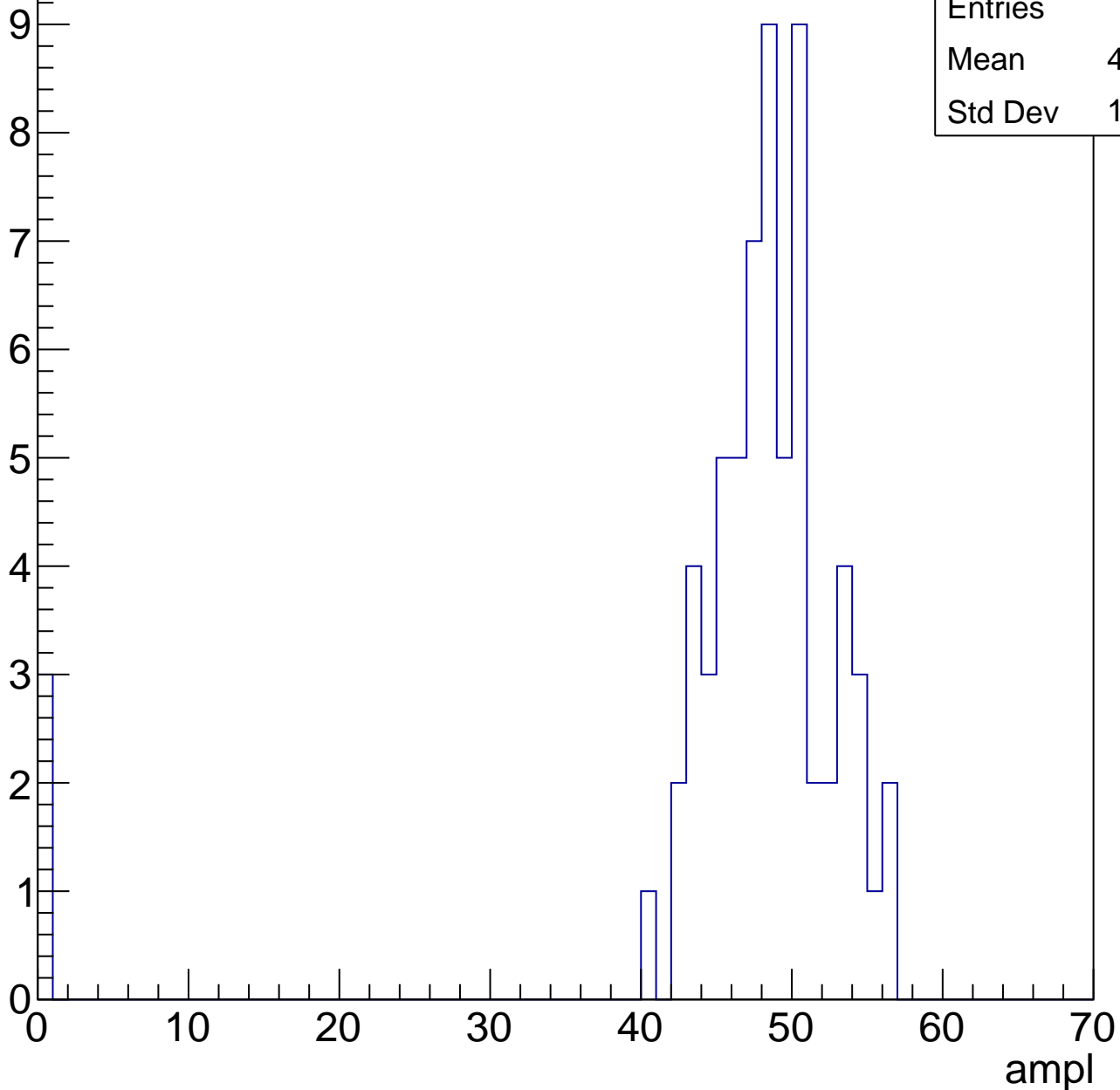


B1L103S, U5-ch121, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	46.06
Std Dev	10.57

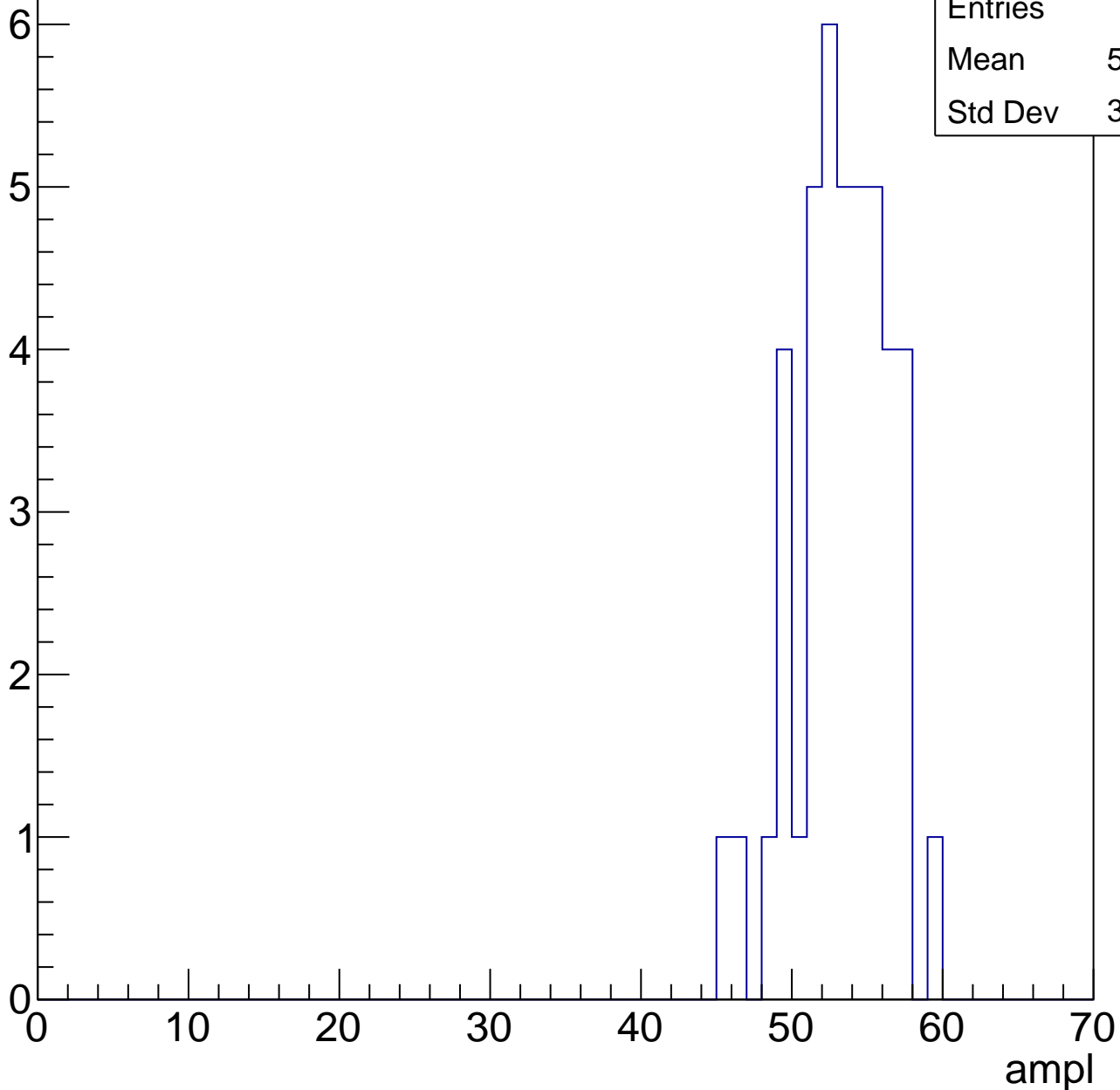


B1L103S, U5-ch121, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

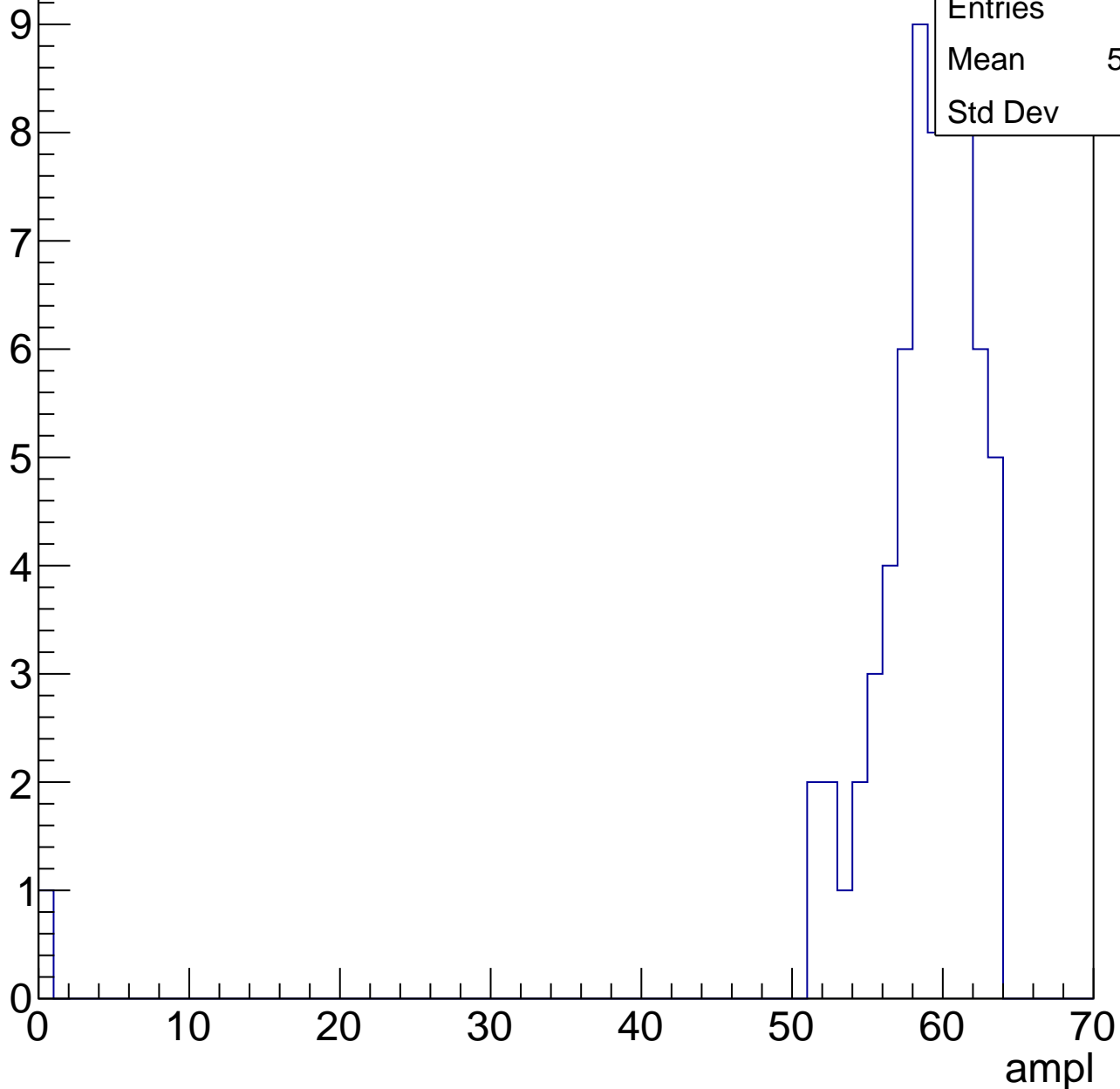
Entries	43
Mean	52.86
Std Dev	3.039



B1L103S, U5-ch121, adc5

calib_packv5_041523_1651.root, FC#0, port C2

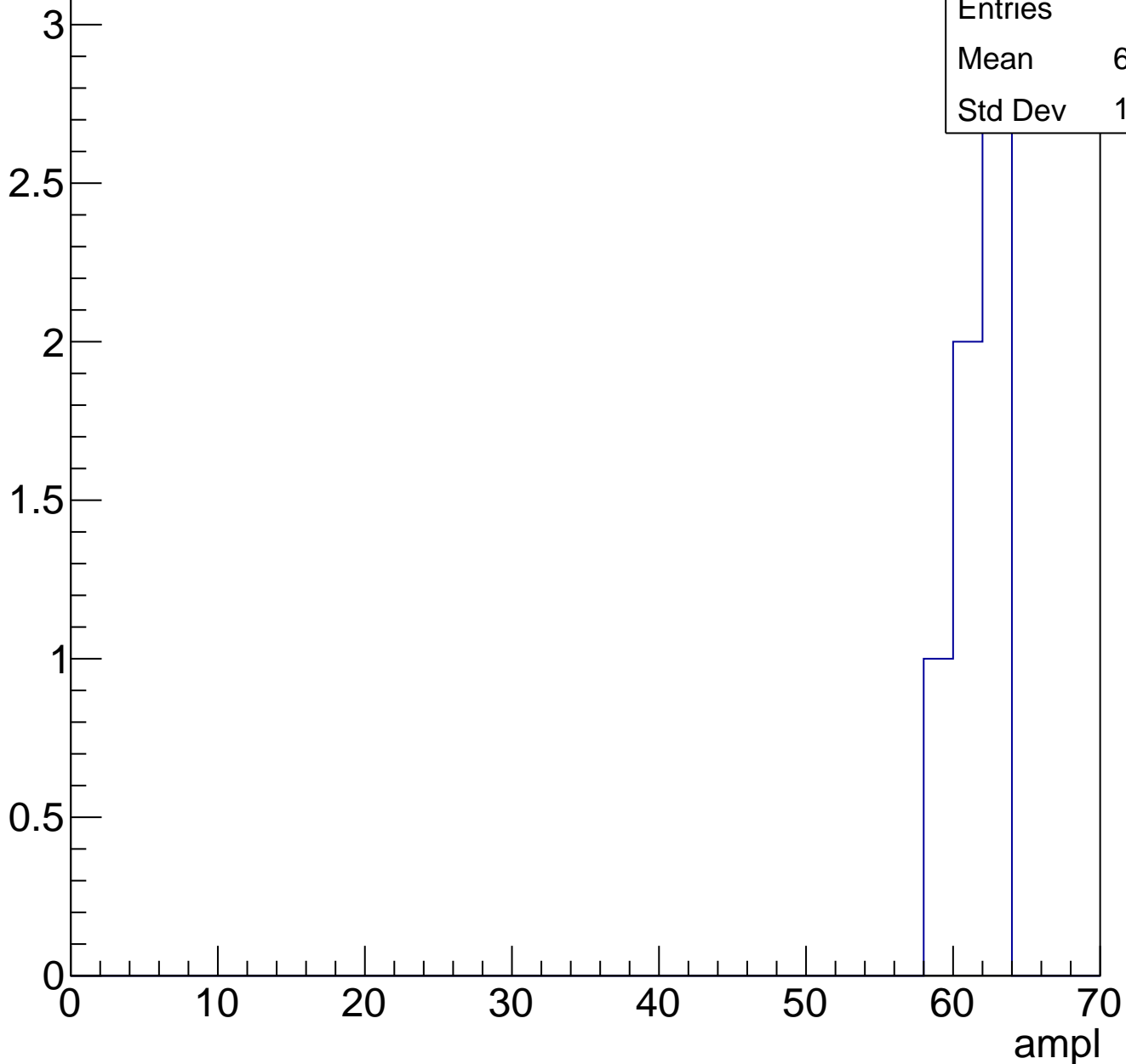
Entry



B1L103S, U5-ch121, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

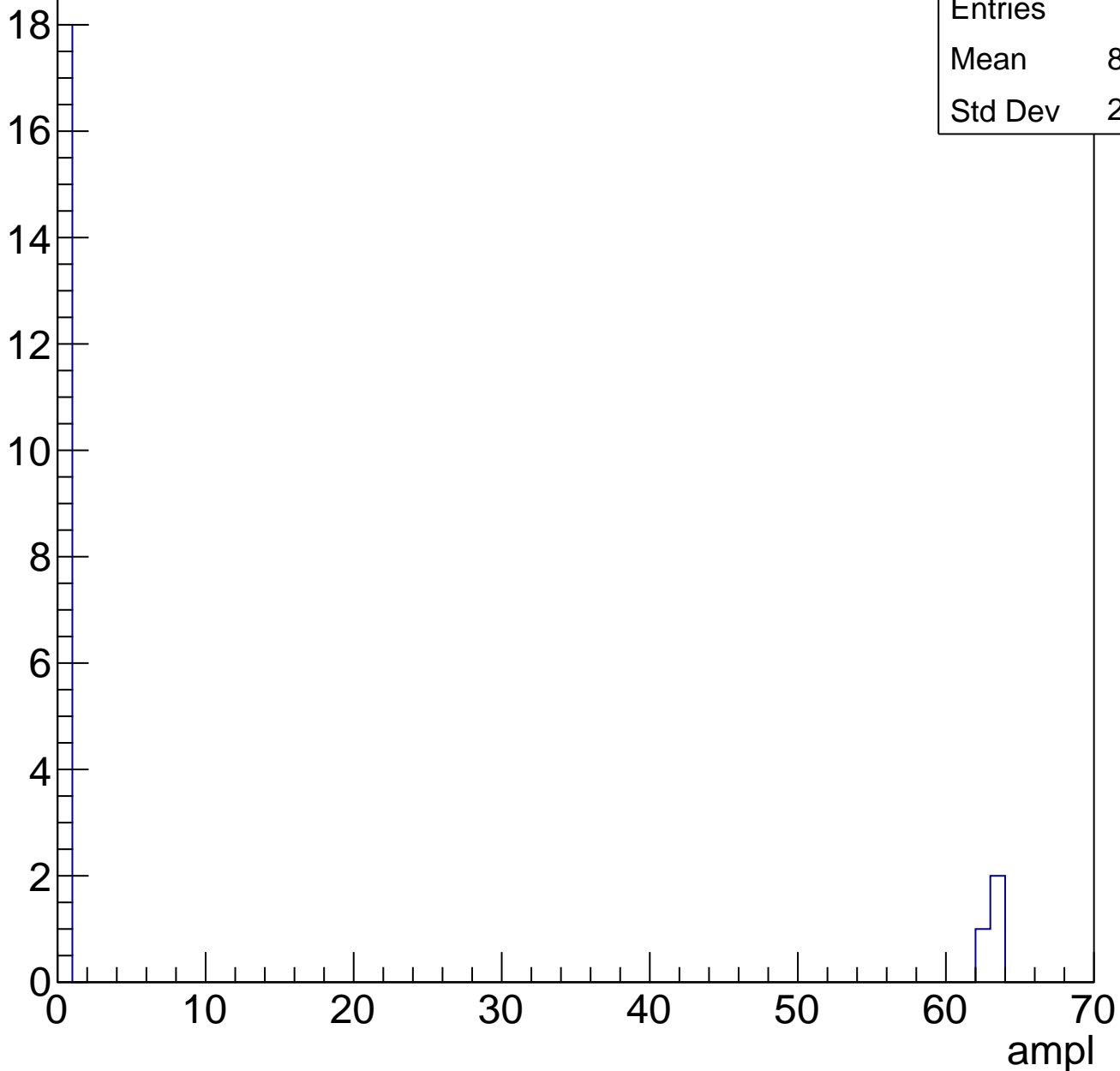


B1L103S, U5-ch121, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	8.952
Std Dev	21.93

Entry

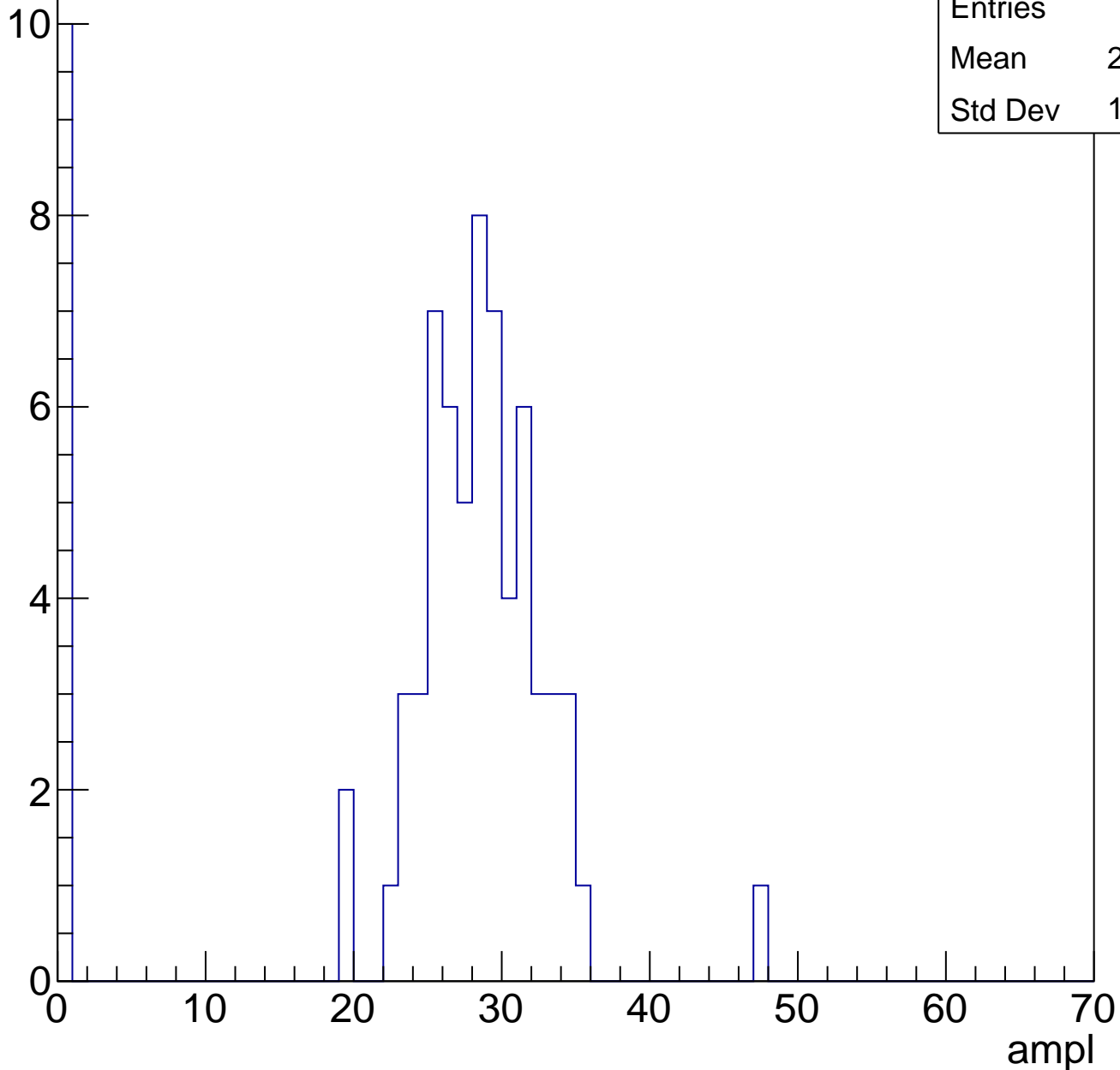


B1L103S, U5-ch122, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	73
Mean	24.37
Std Dev	10.47

Entry

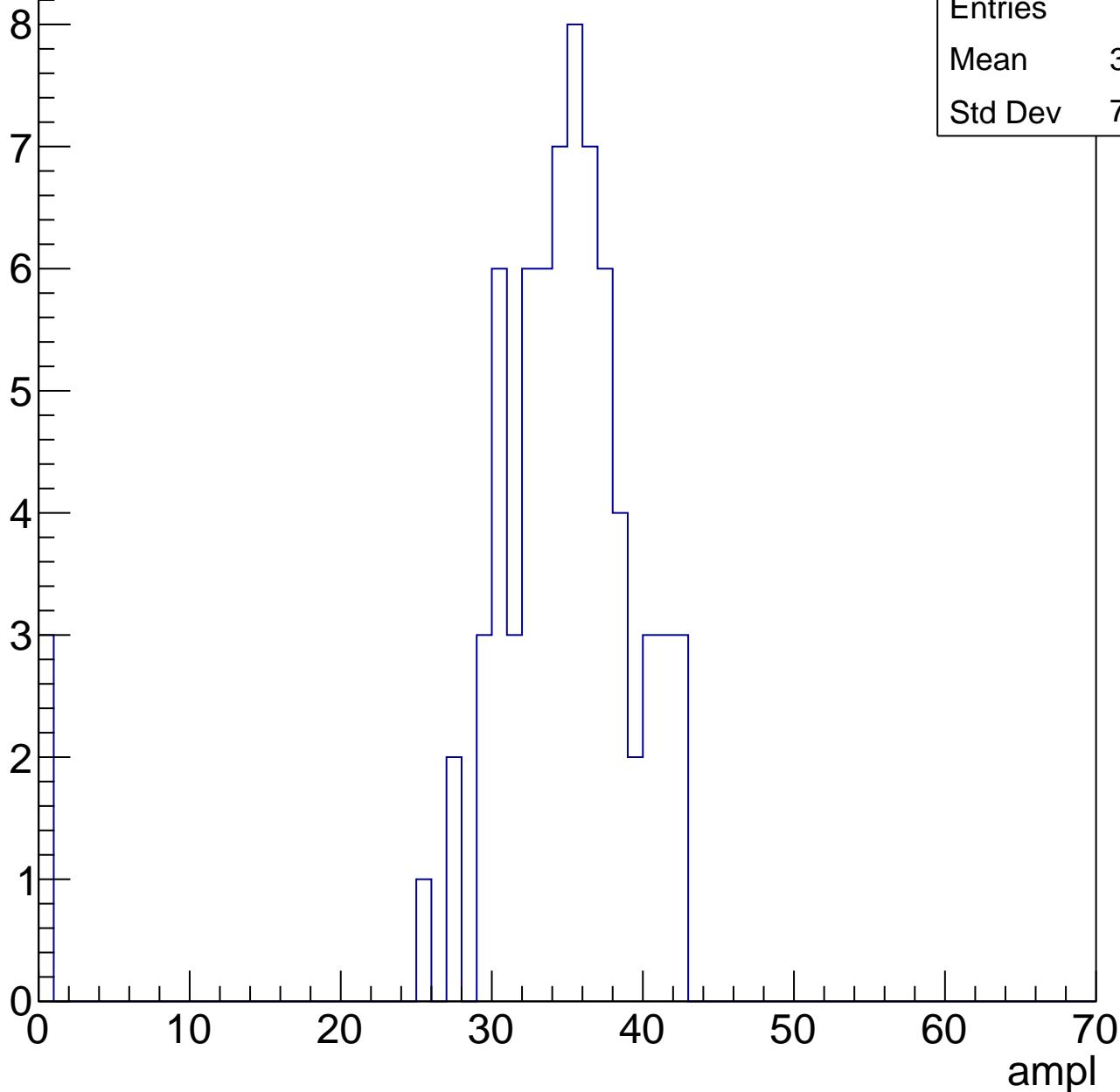


B1L103S, U5-ch122, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	33.15
Std Dev	7.828

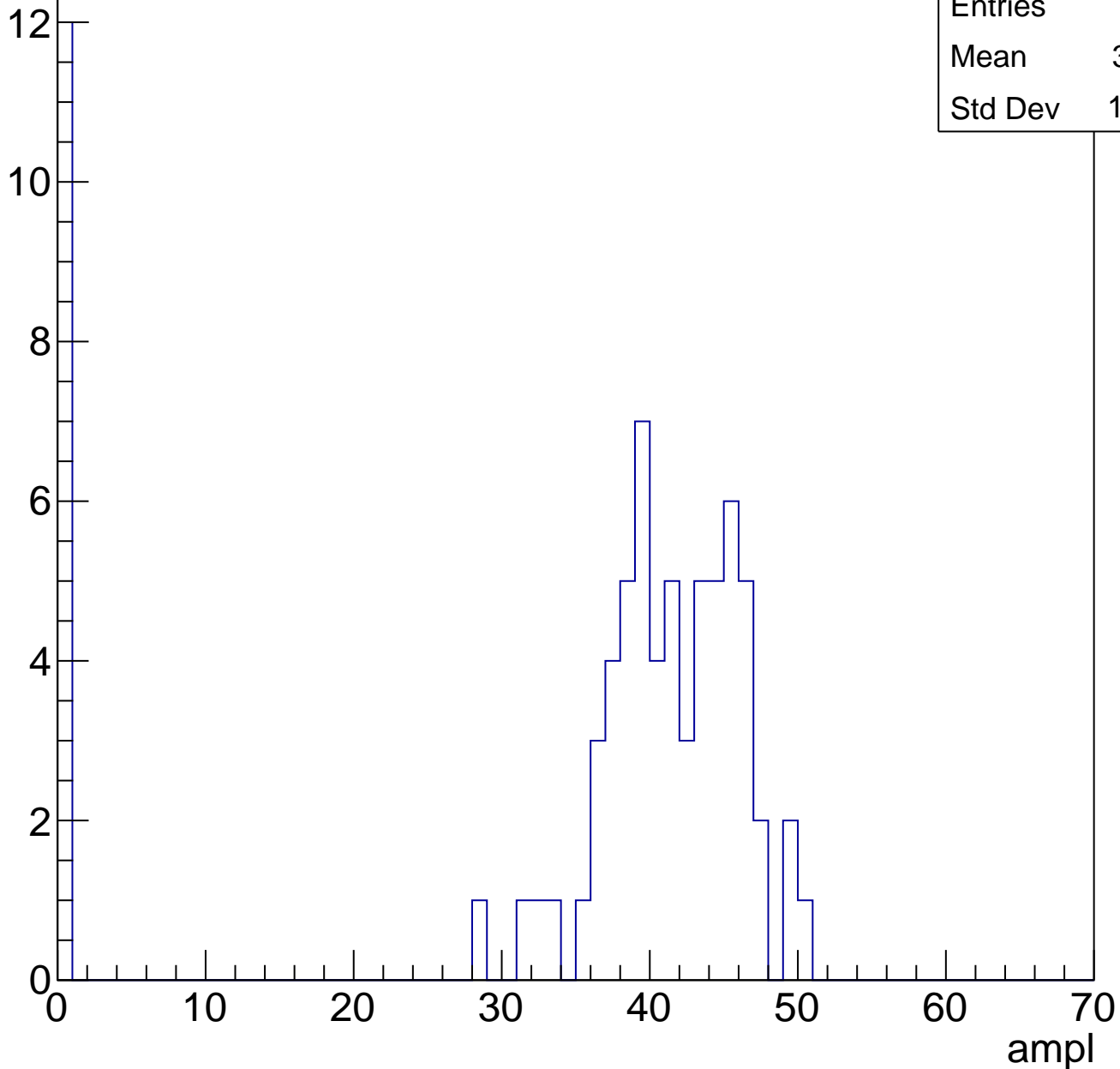


B1L103S, U5-ch122, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	74
Mean	34.41
Std Dev	15.68

Entry

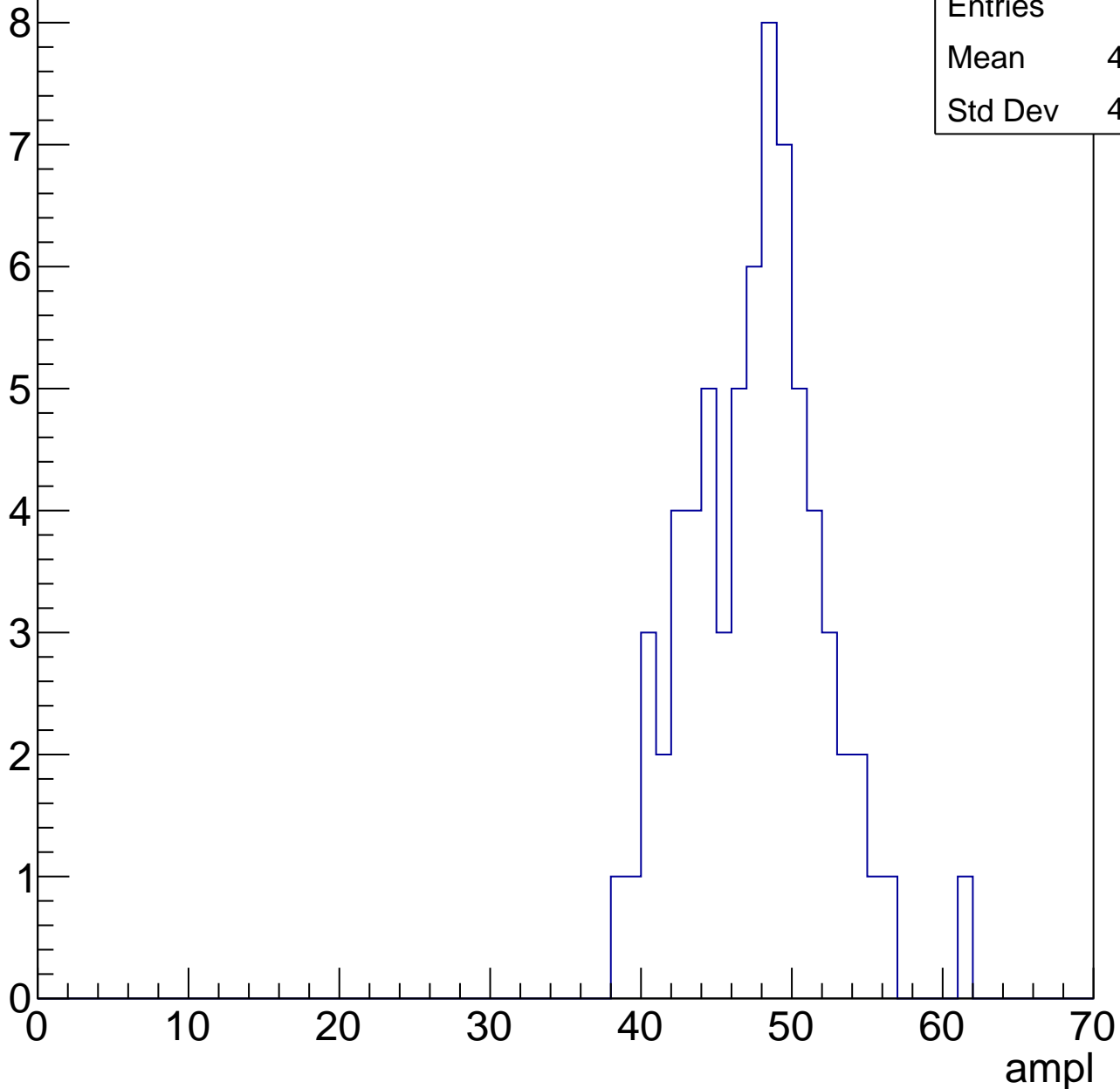


B1L103S, U5-ch122, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	47.19
Std Dev	4.403

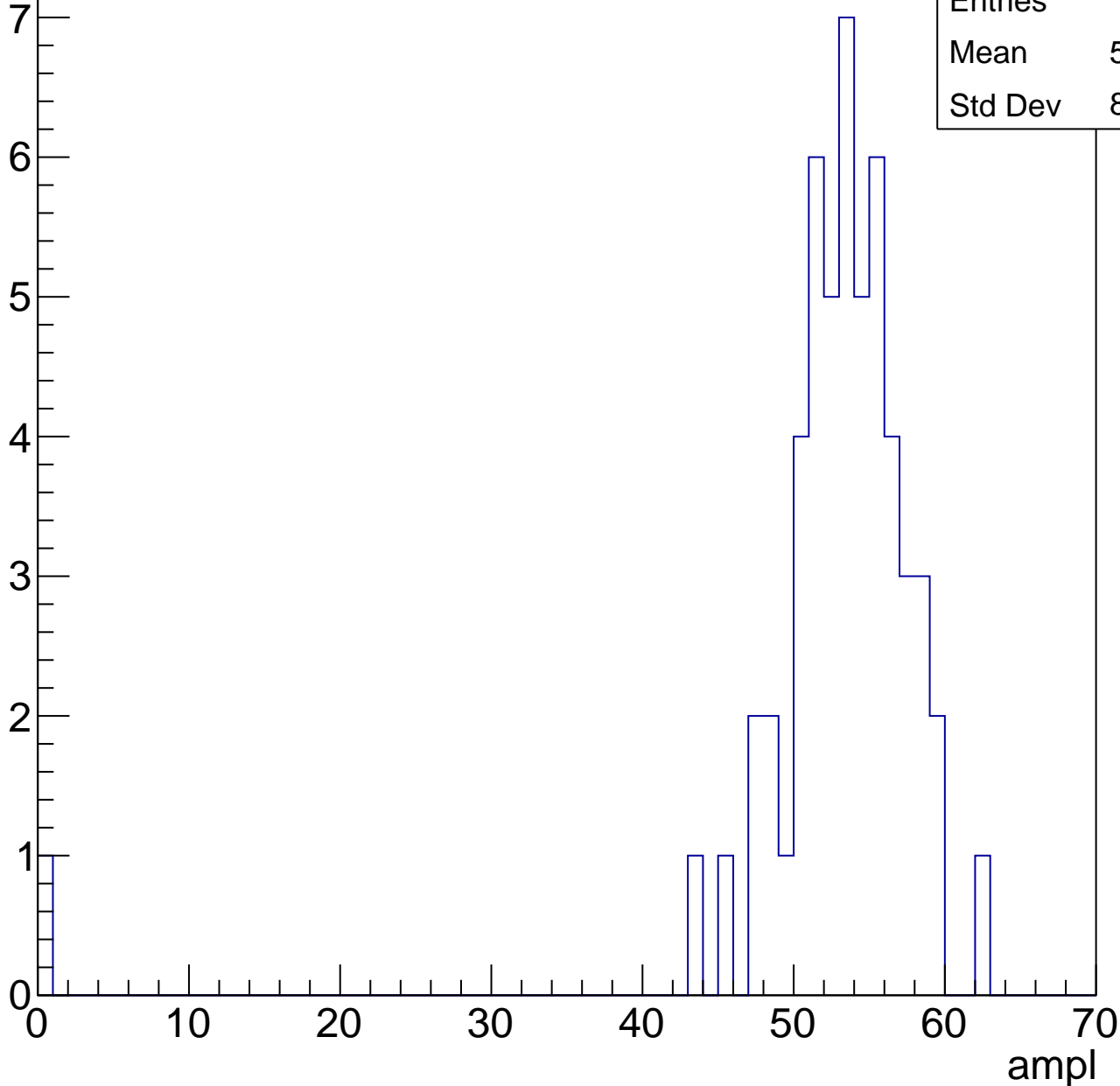


B1L103S, U5-ch122, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

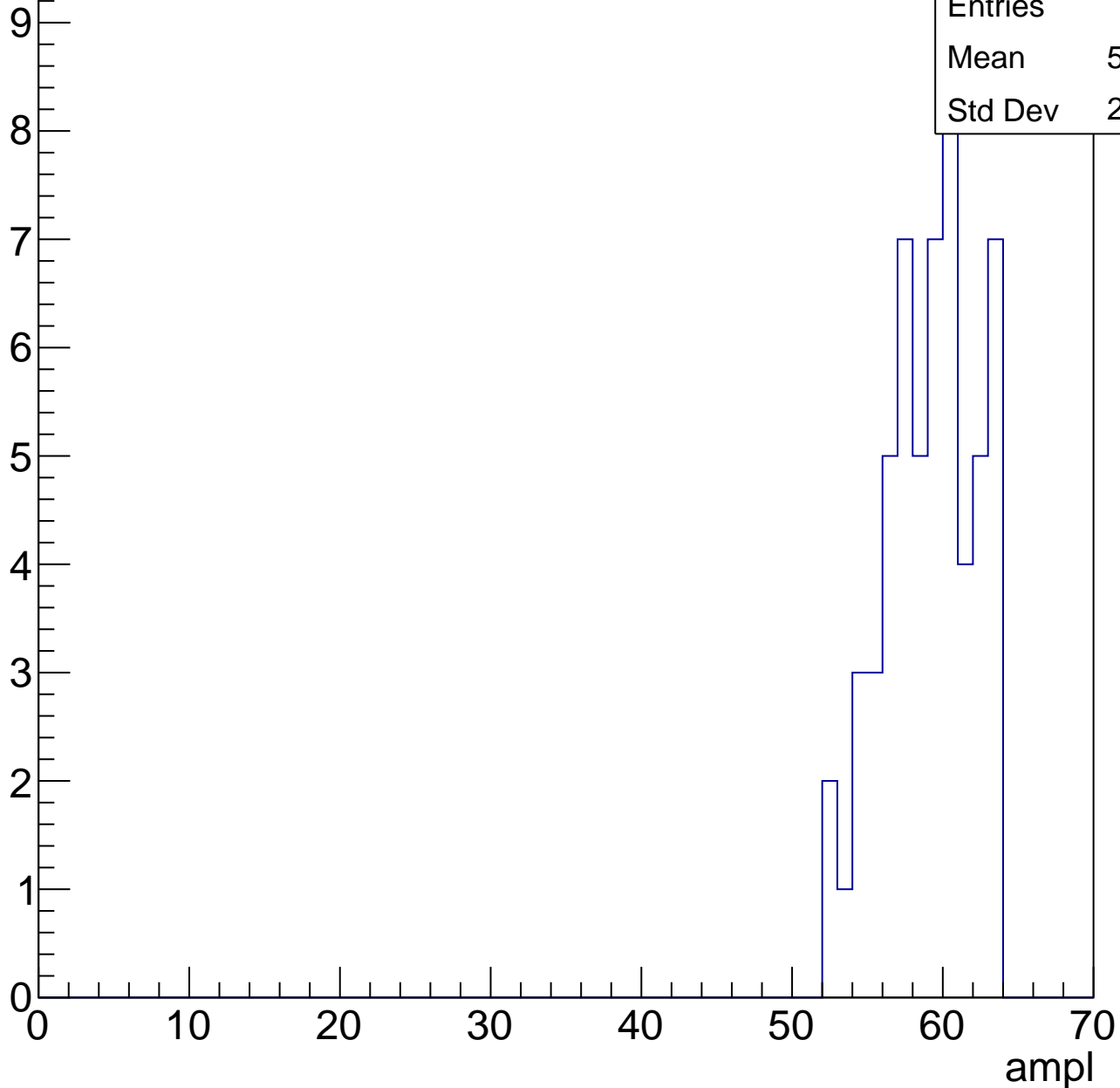
Entries	54
Mean	52.09
Std Dev	8.019



B1L103S, U5-ch122, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

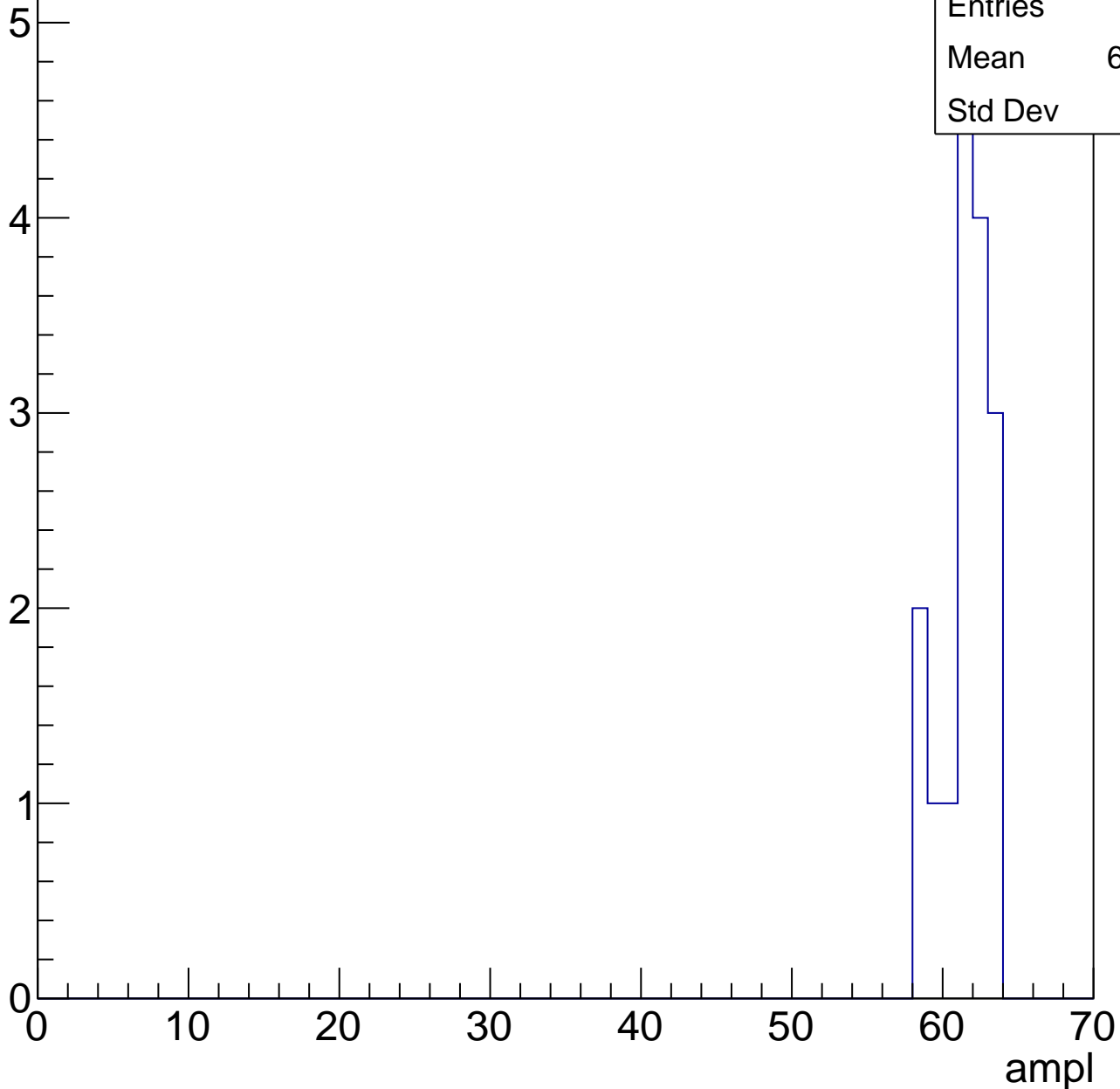


B1L103S, U5-ch122, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	16
Mean	61.06
Std Dev	1.56



B1L103S, U5-ch122, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

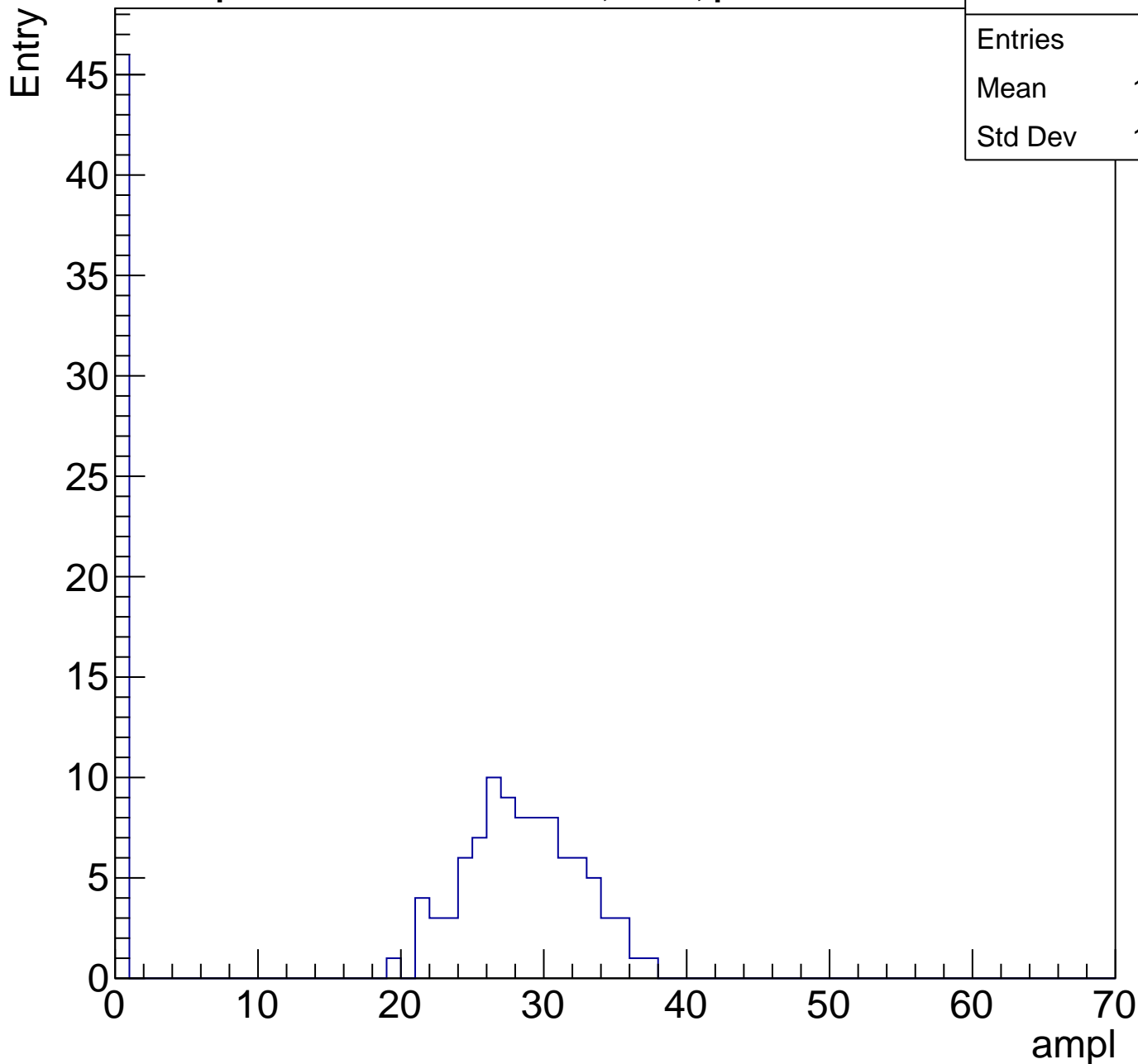
ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U5-ch123, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	138
Mean	18.69
Std Dev	13.59

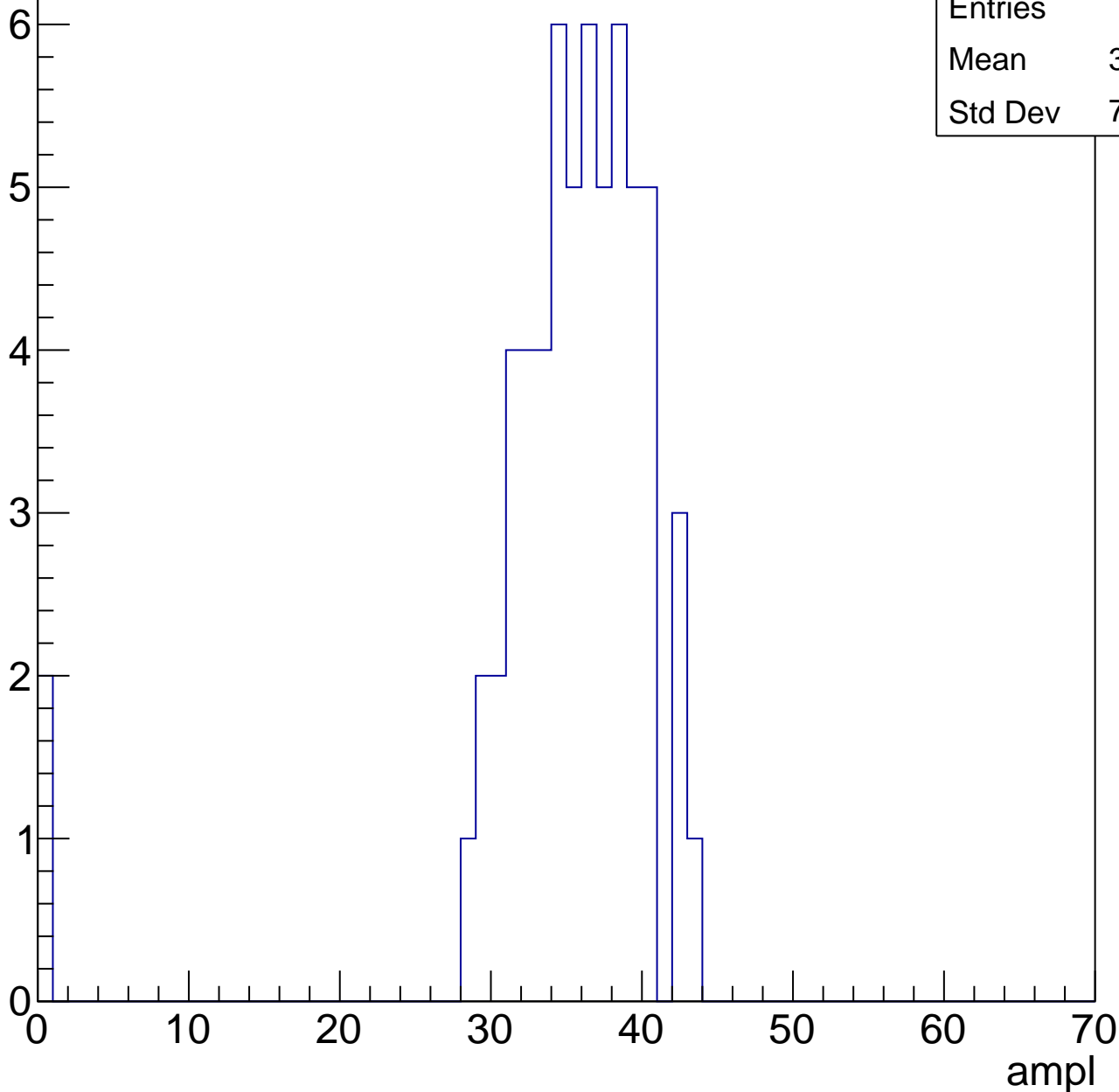


B1L103S, U5-ch123, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	34.46
Std Dev	7.267



B1L103S, U5-ch123, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	76
Mean	34.13
Std Dev	15.86

Entry

12

10

8

6

4

2

0

0

10

20

30

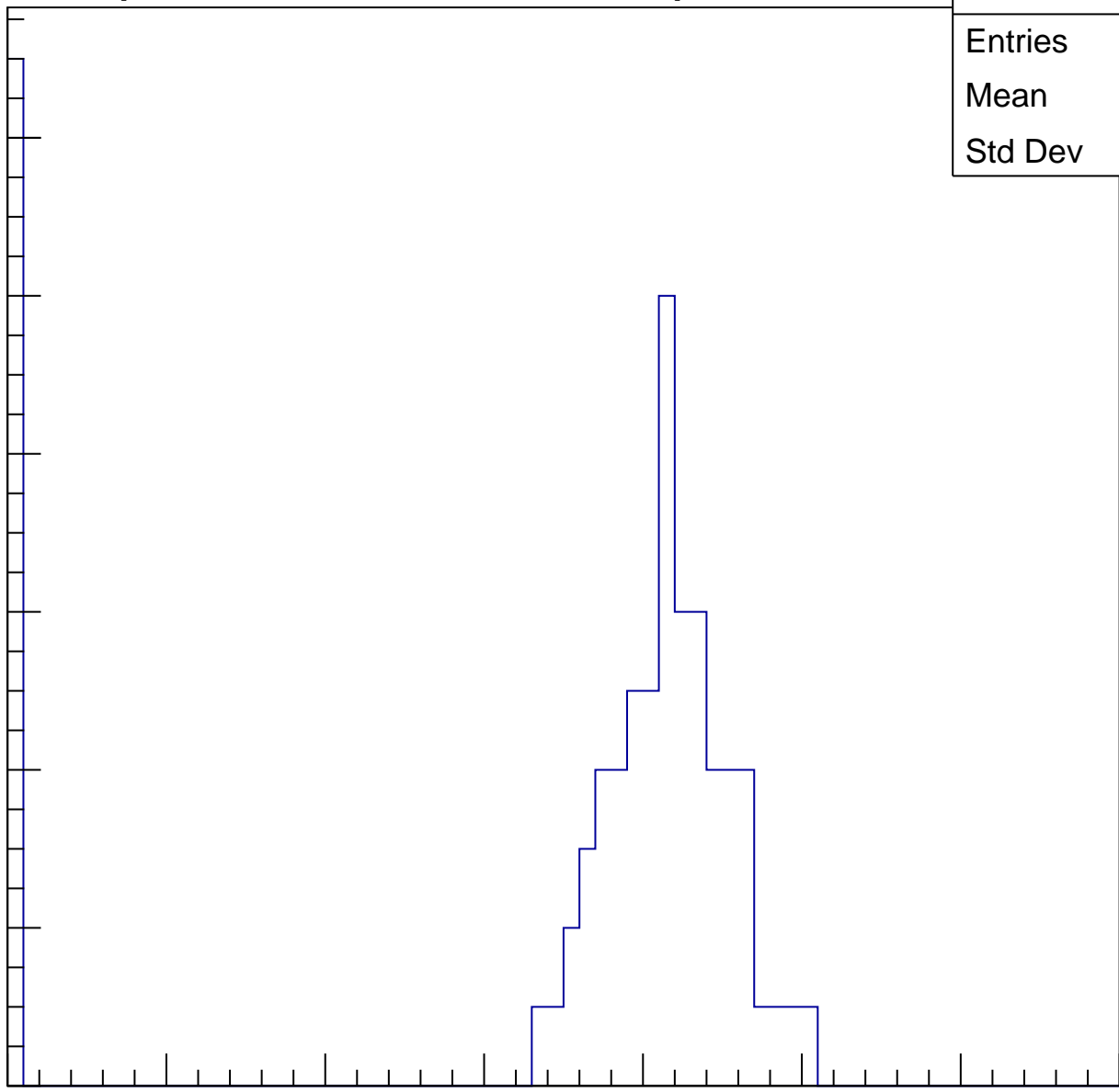
40

50

60

70

ampl

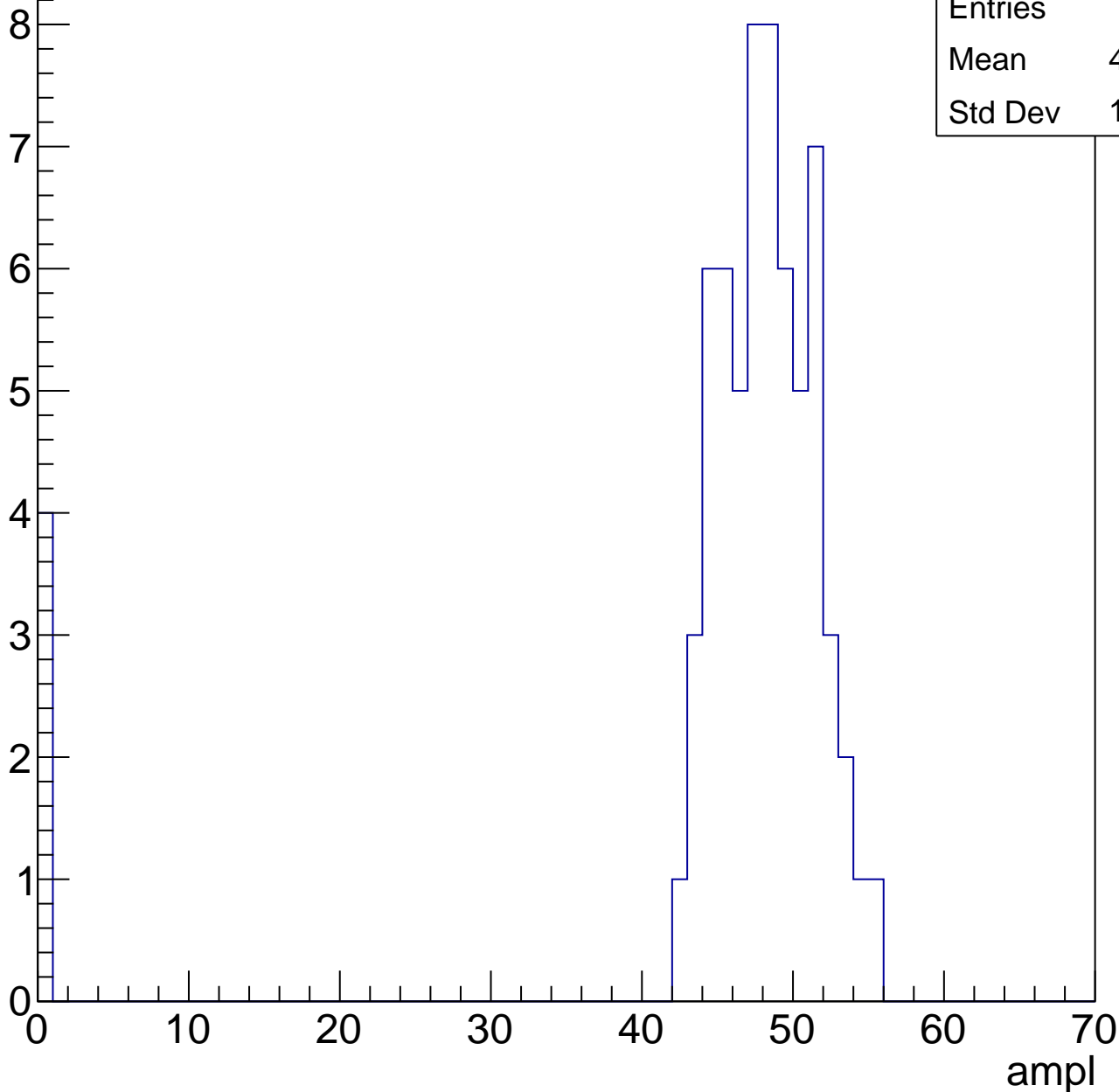


B1L103S, U5-ch123, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	44.95
Std Dev	11.78

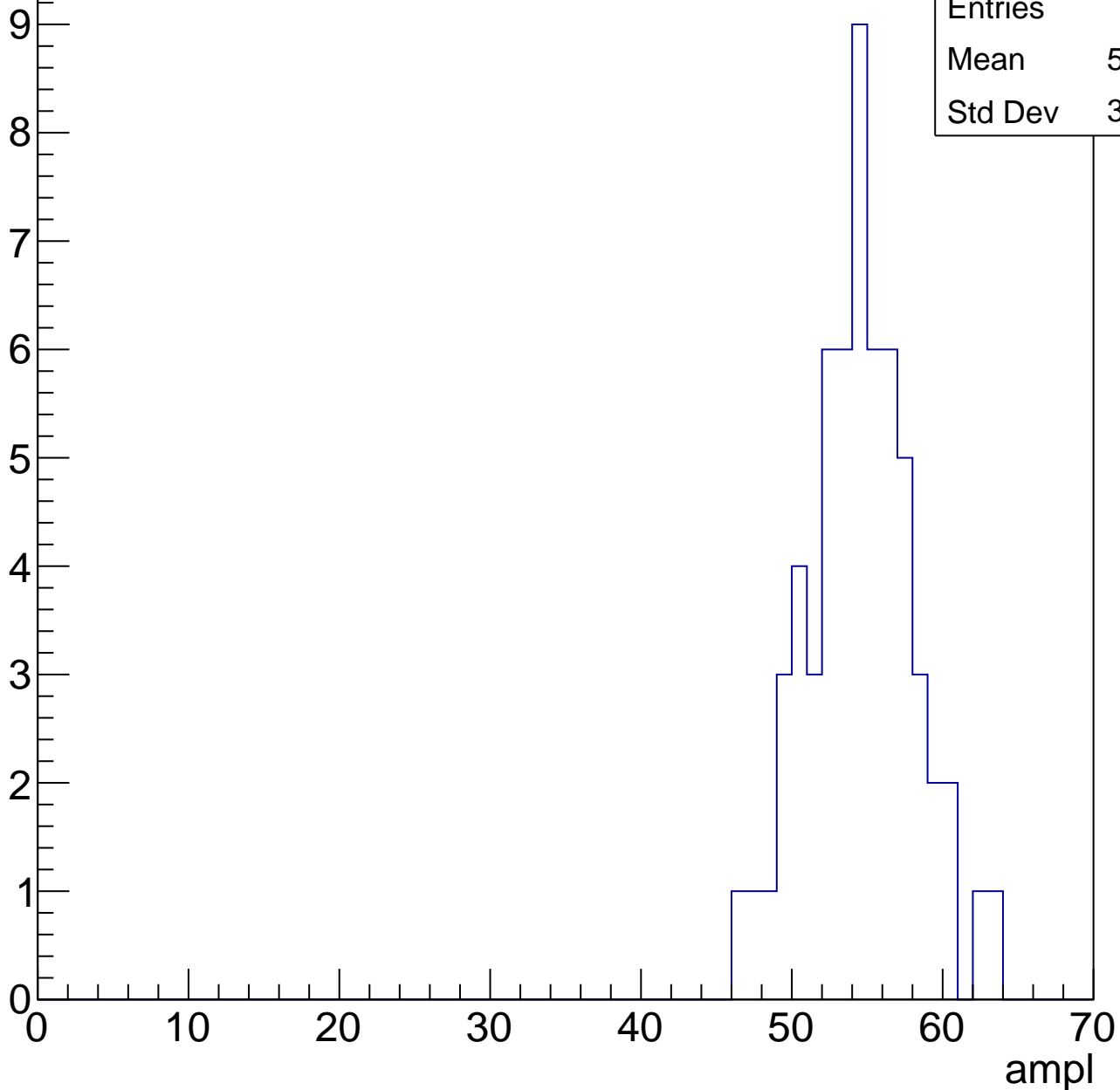


B1L103S, U5-ch123, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	54.08
Std Dev	3.499

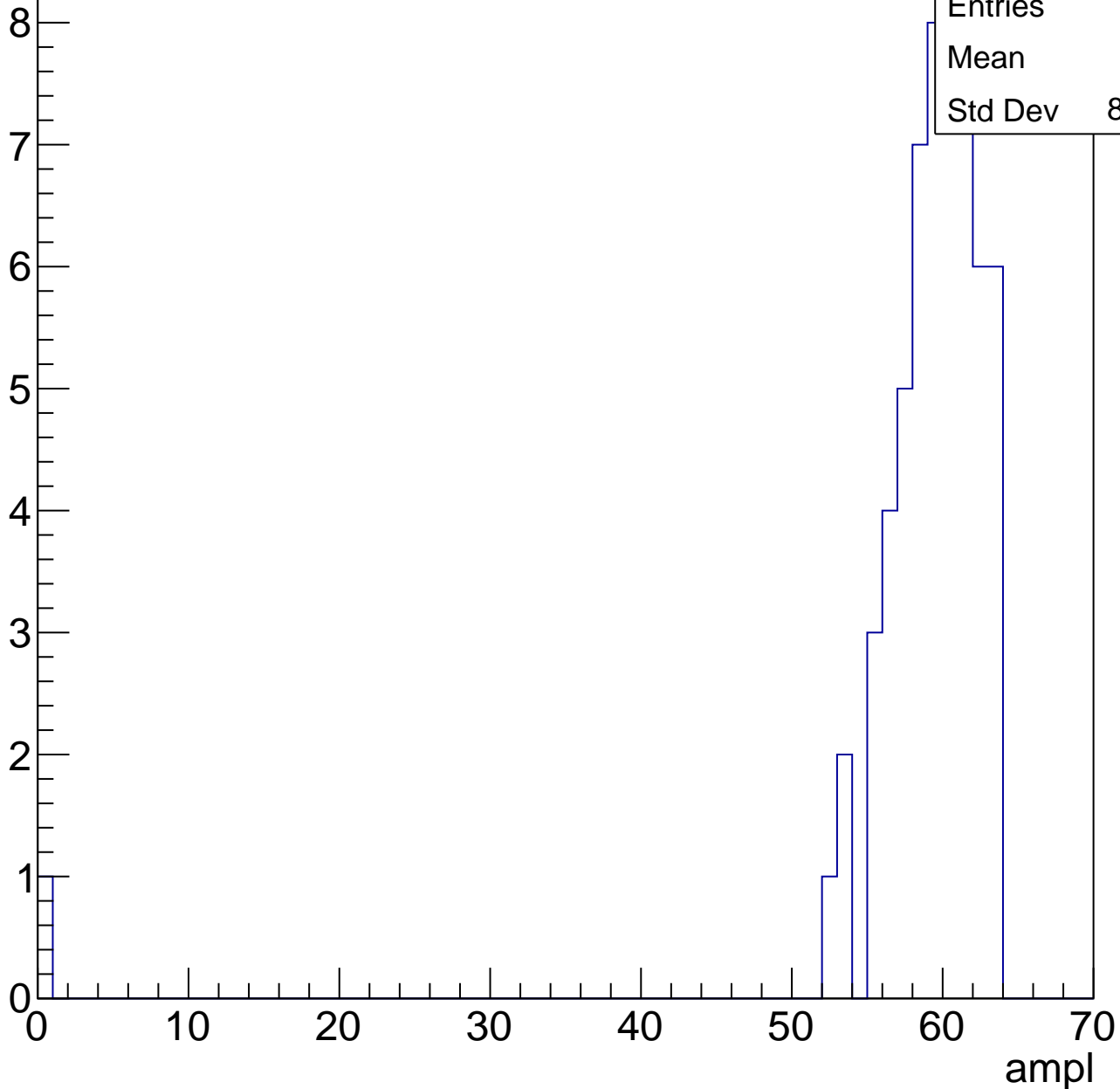


B1L103S, U5-ch123, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

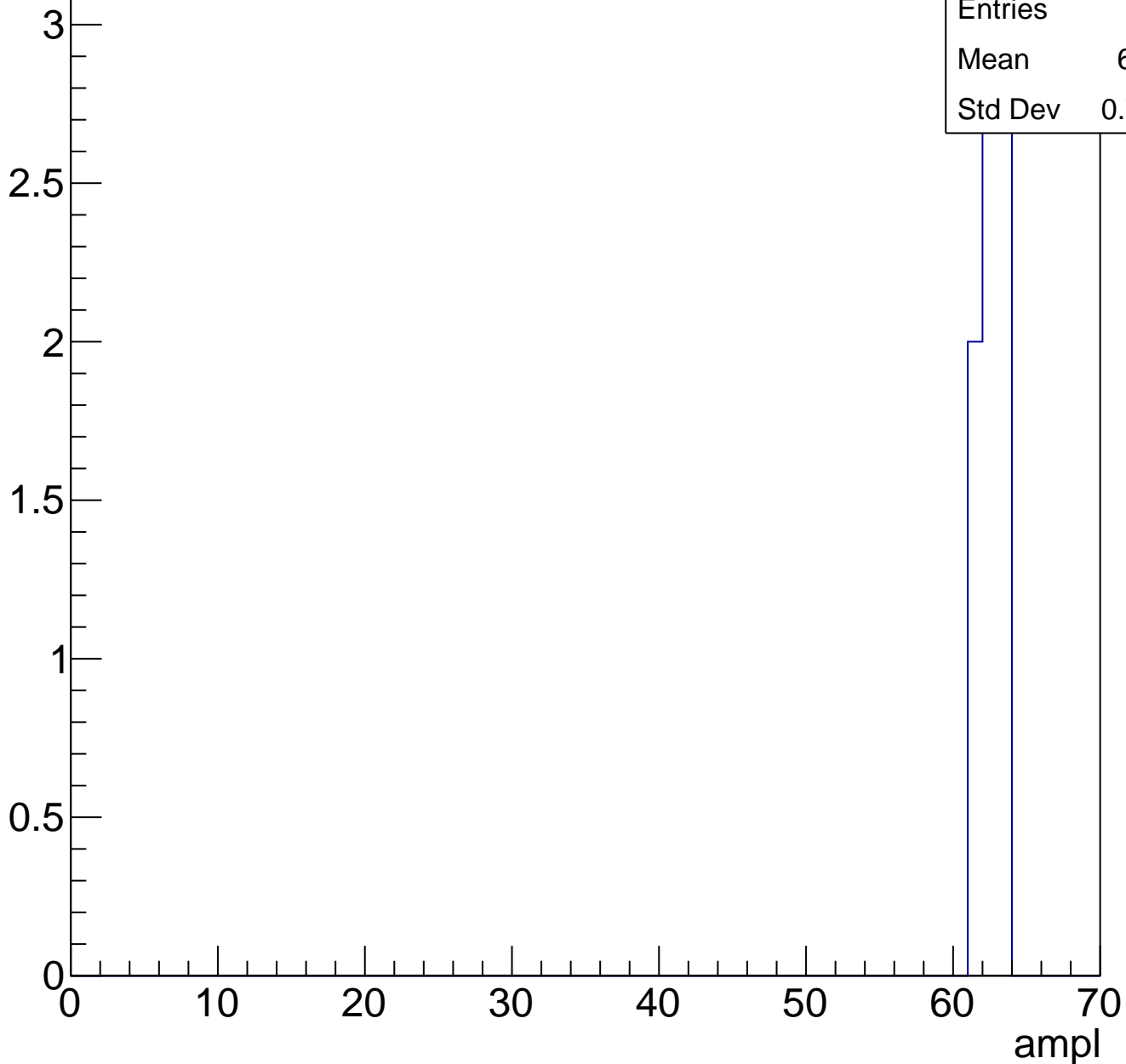
Entries	59
Mean	58.1
Std Dev	8.084



B1L103S, U5-ch123, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U5-ch123, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	18
Mean	0
Std Dev	0

B1L103S, U5-ch124, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	84
Mean	24.12
Std Dev	10.95

Entry

12

10

8

6

4

2

0

0

10

20

30

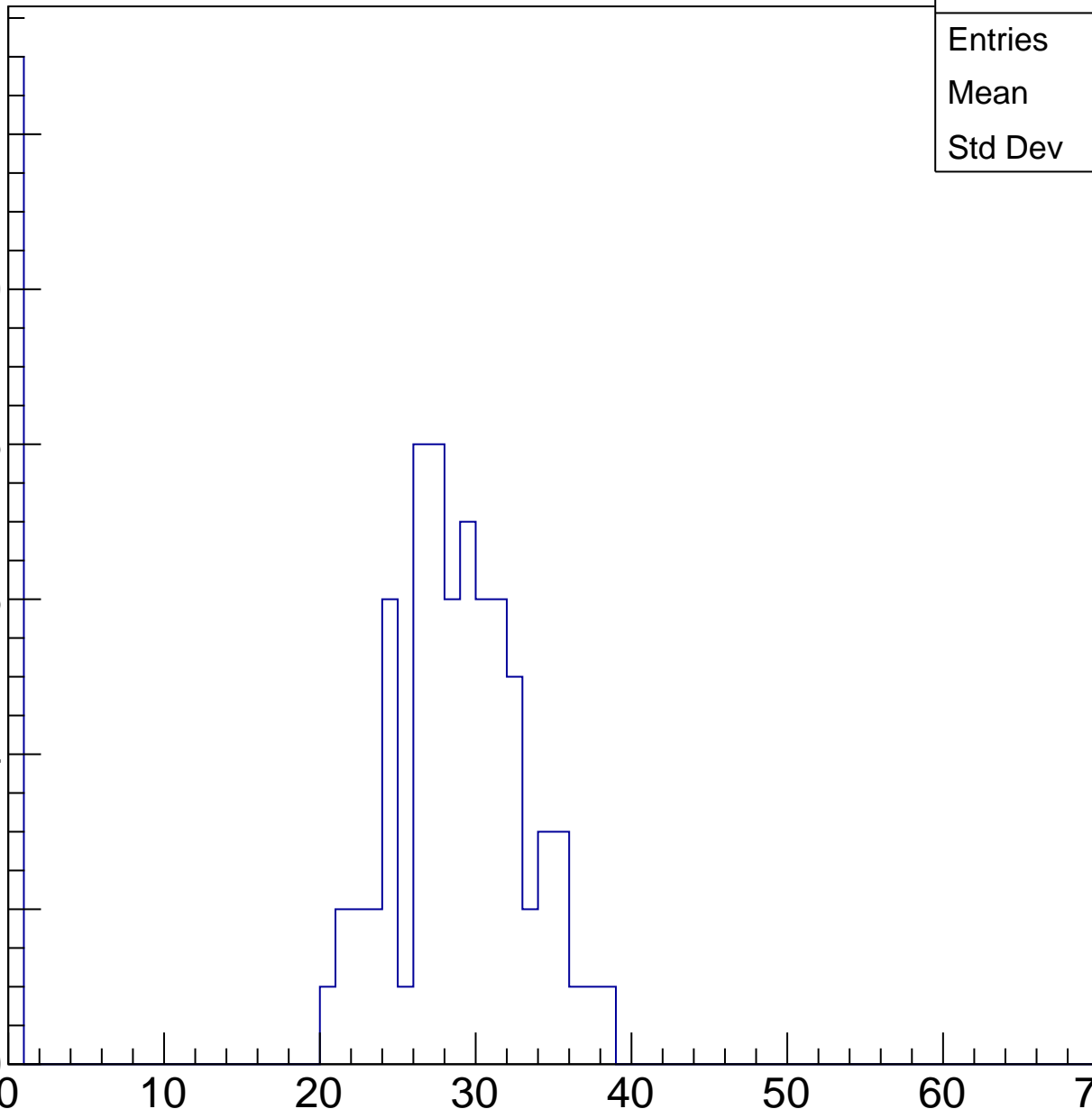
40

50

60

70

ampl

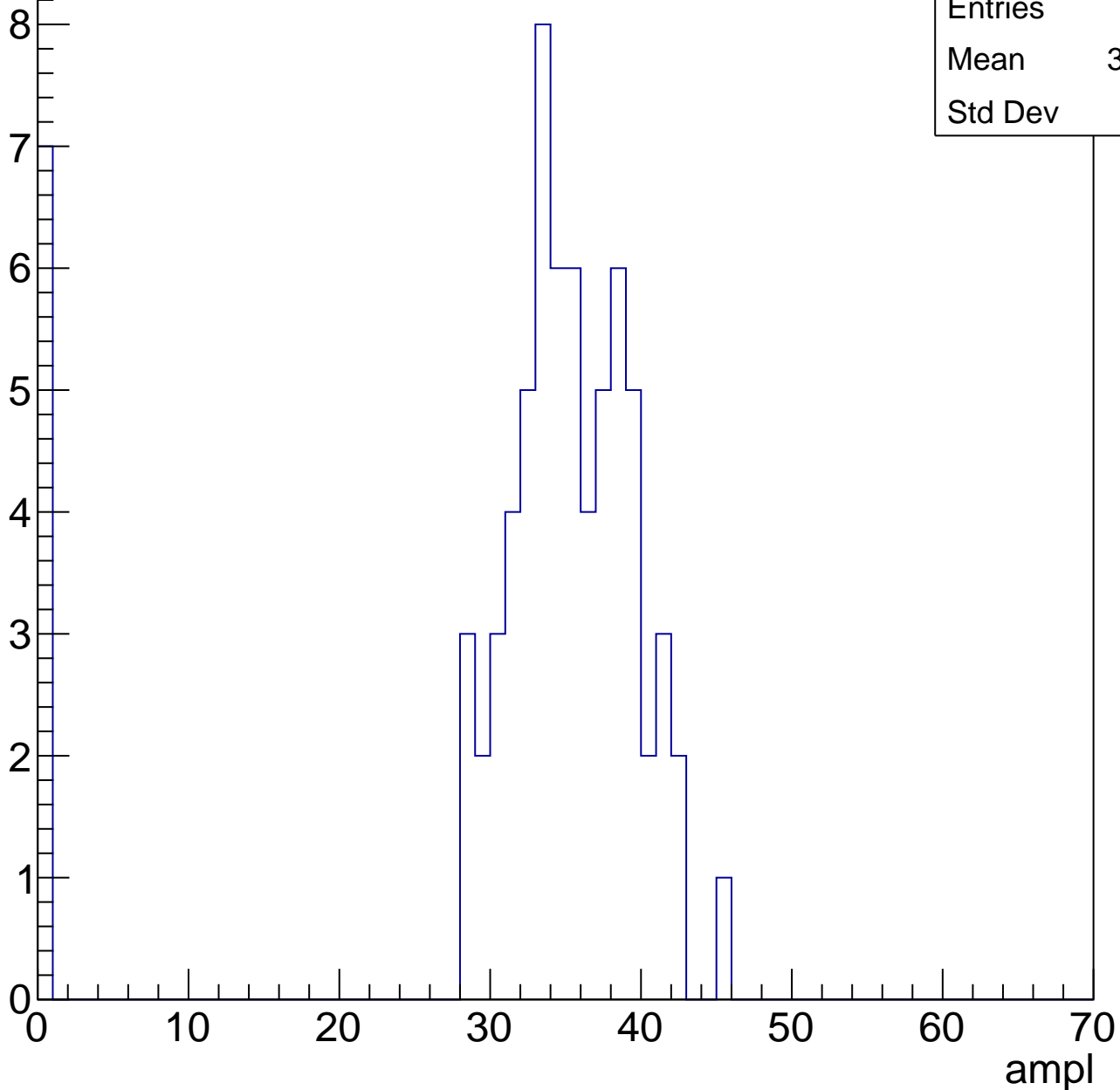


B1L103S, U5-ch124, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	31.64
Std Dev	11

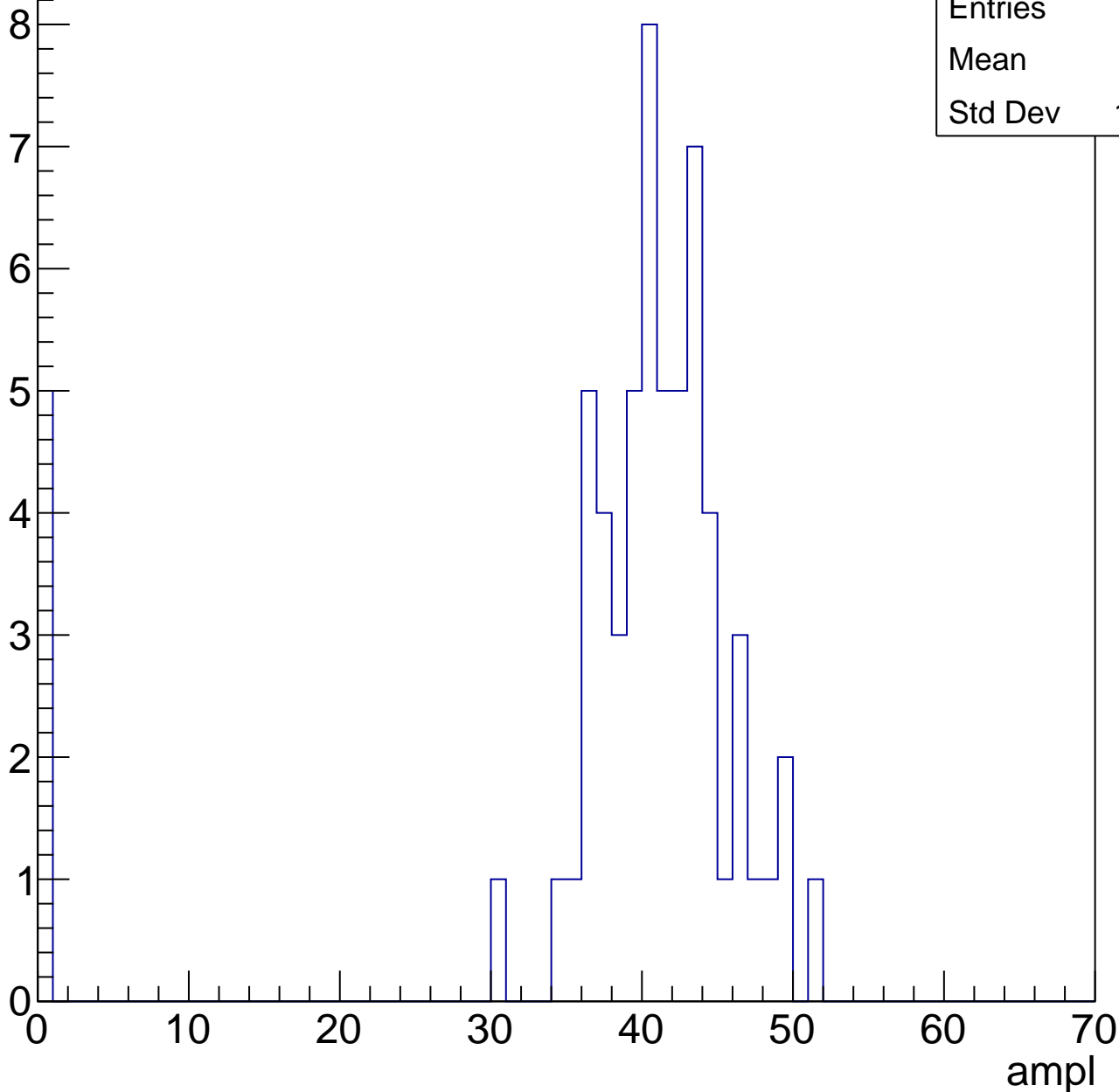


B1L103S, U5-ch124, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	37.7
Std Dev	11.71

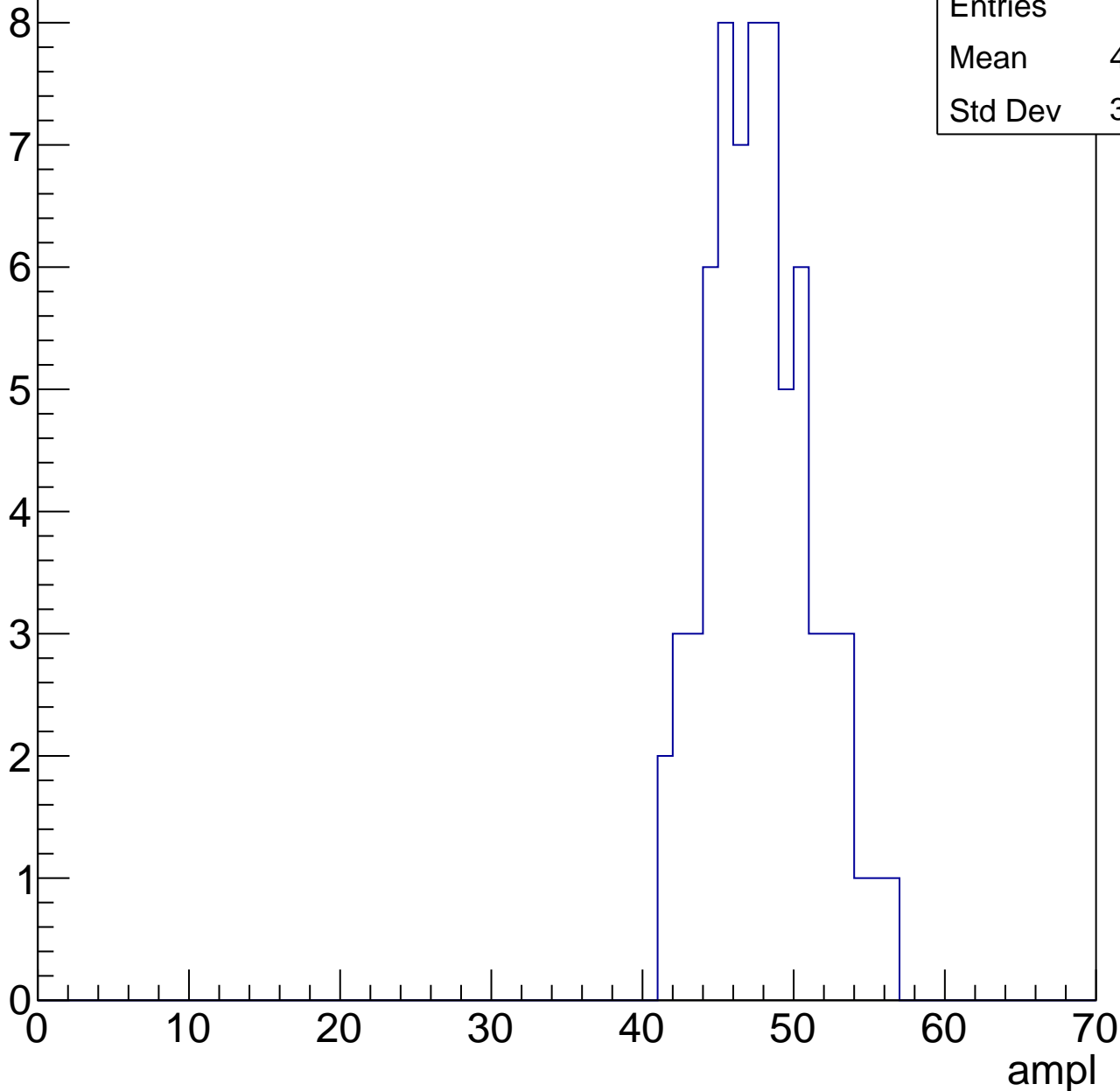


B1L103S, U5-ch124, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	47.37
Std Dev	3.399

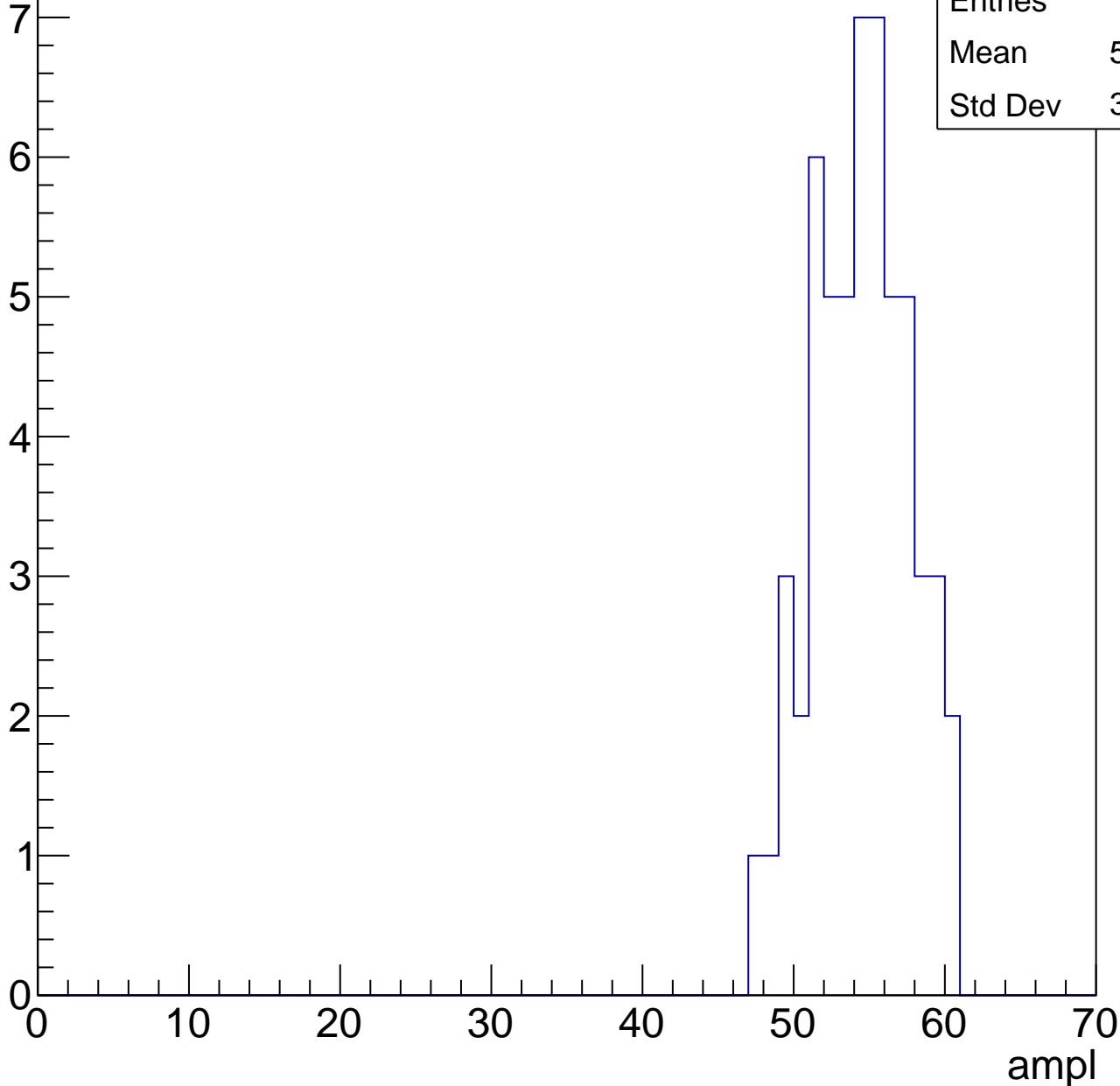


B1L103S, U5-ch124, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	54.04
Std Dev	3.127



B1L103S, U5-ch124, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

7

6

5

4

3

2

1

0

Entries	54
Mean	58.31
Std Dev	3.254

ampl

0

10

20

30

40

50

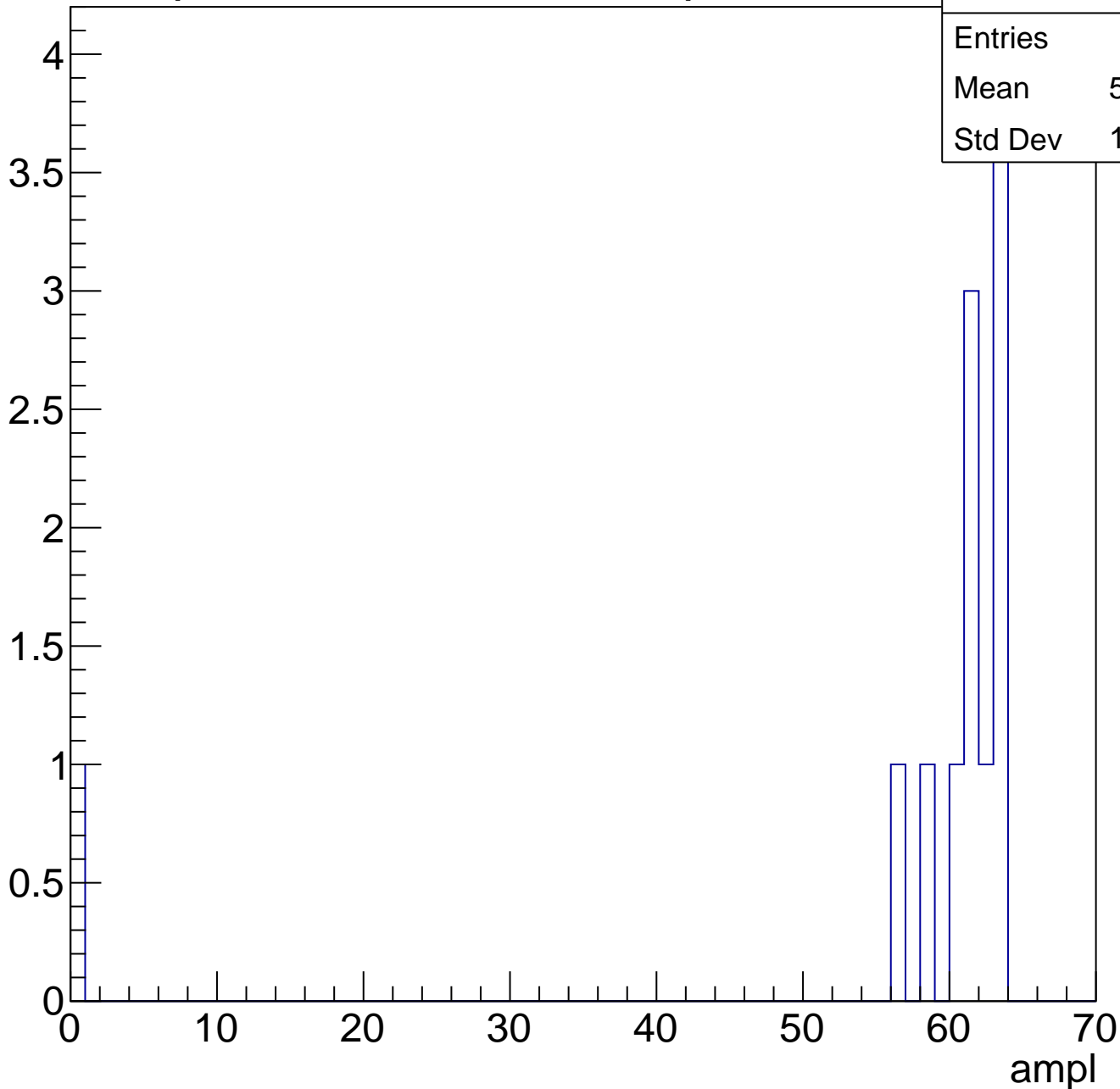
60

70

B1L103S, U5-ch124, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

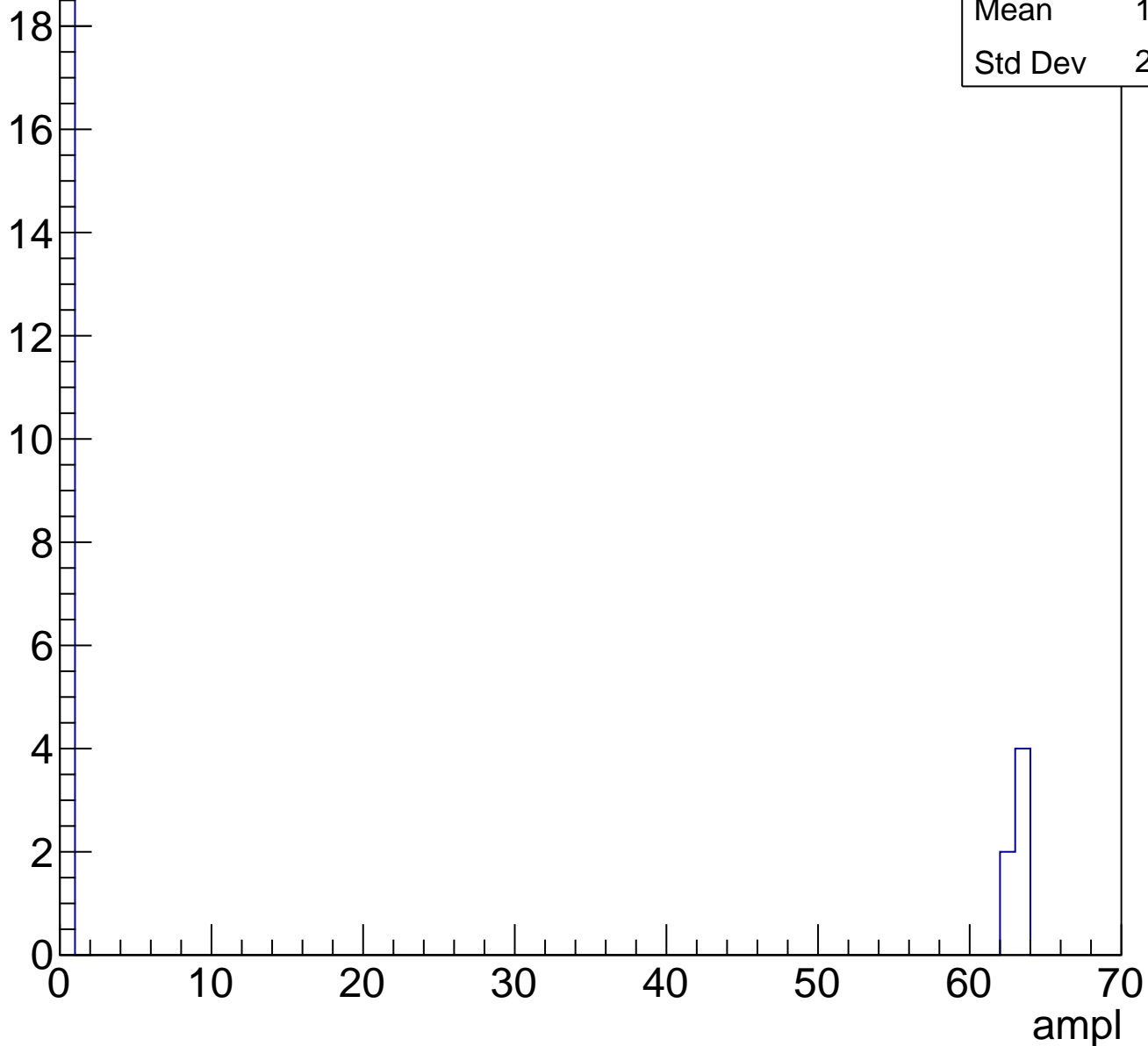


B1L103S, U5-ch124, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	25
Mean	15.04
Std Dev	26.76

Entry



B1L103S, U5-ch125, adc0

calib_packv5_041523_1651.root, FC#0, port C2

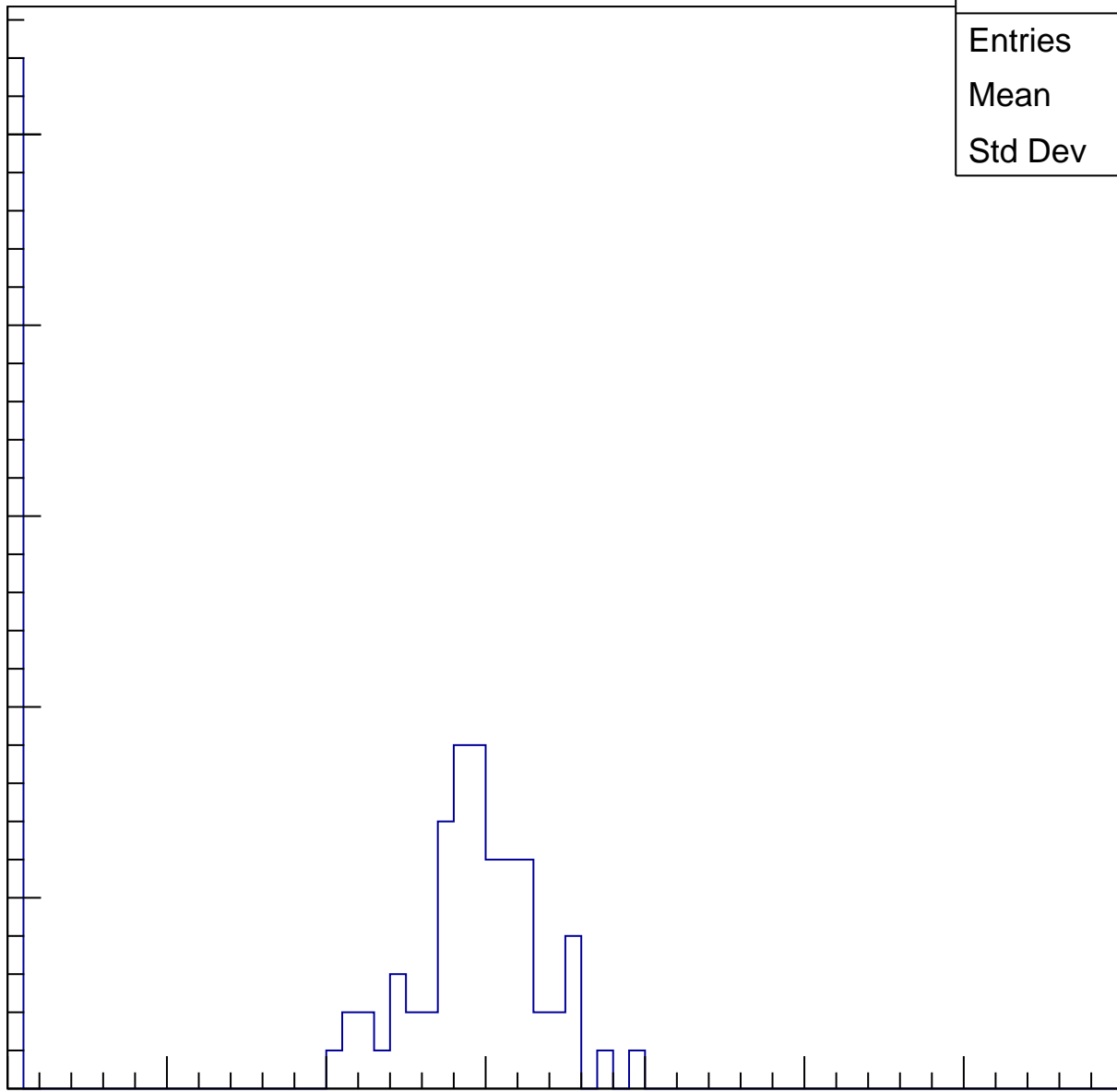
Entries	93
Mean	20.57
Std Dev	13.55

Entry

25
20
15
10
5
0

0 10 20 30 40 50 60 70

ampl

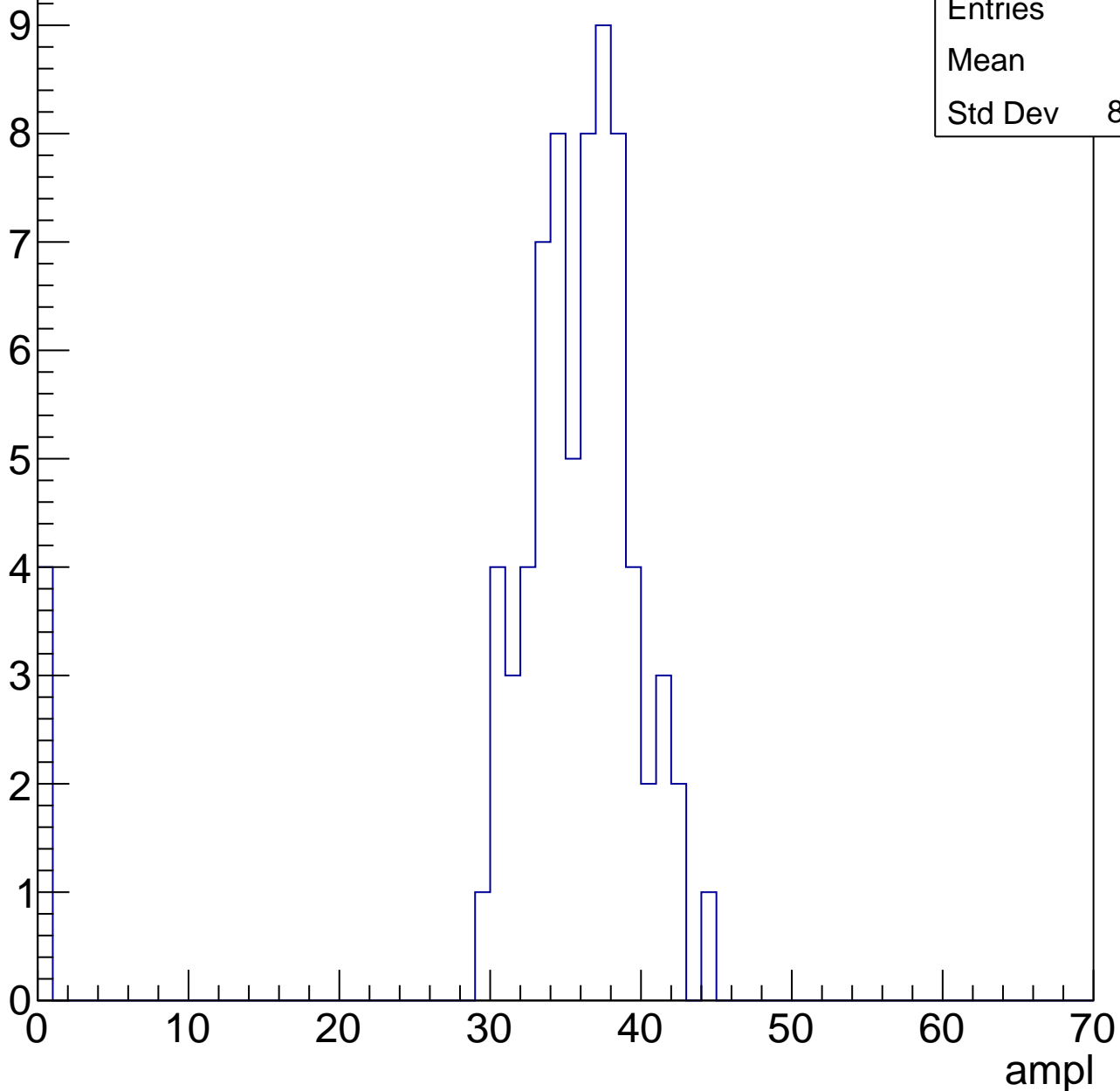


B1L103S, U5-ch125, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	33.7
Std Dev	8.719

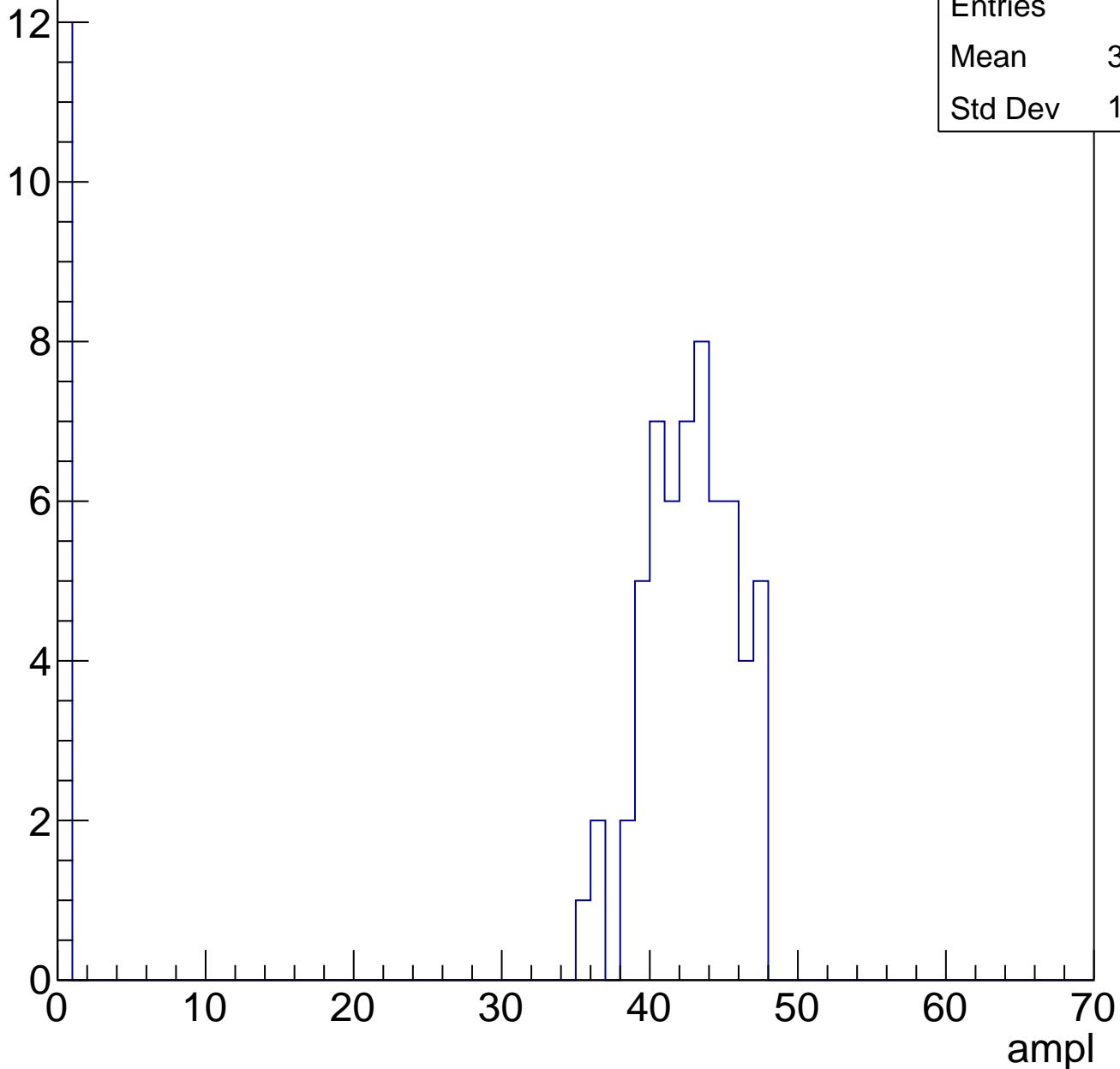


B1L103S, U5-ch125, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	71
Mean	35.14
Std Dev	16.07

Entry



B1L103S, U5-ch125, adc3

calib_packv5_041523_1651.root, FC#0, port C2

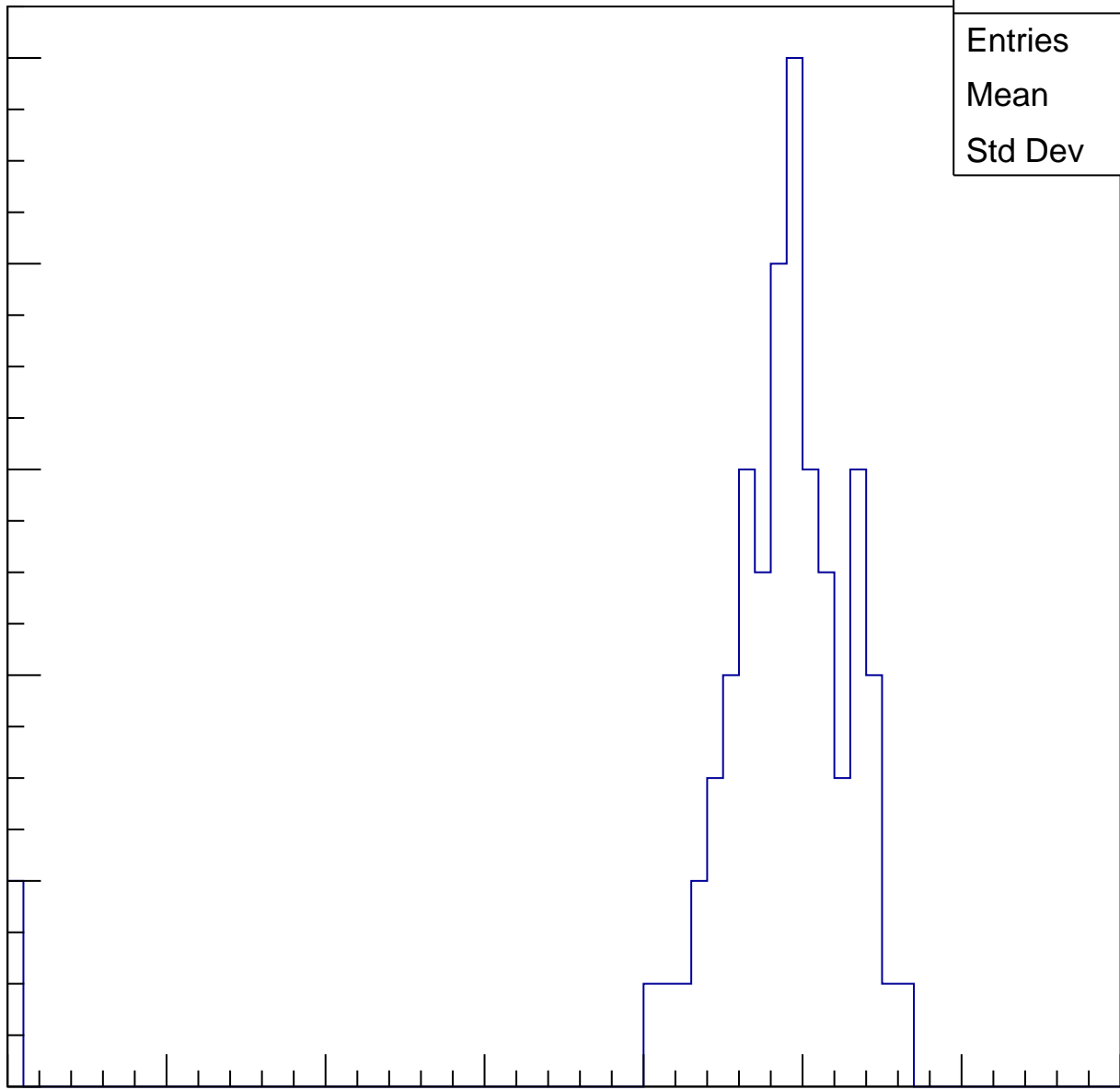
Entries	69
Mean	47.28
Std Dev	8.861

Entry

10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

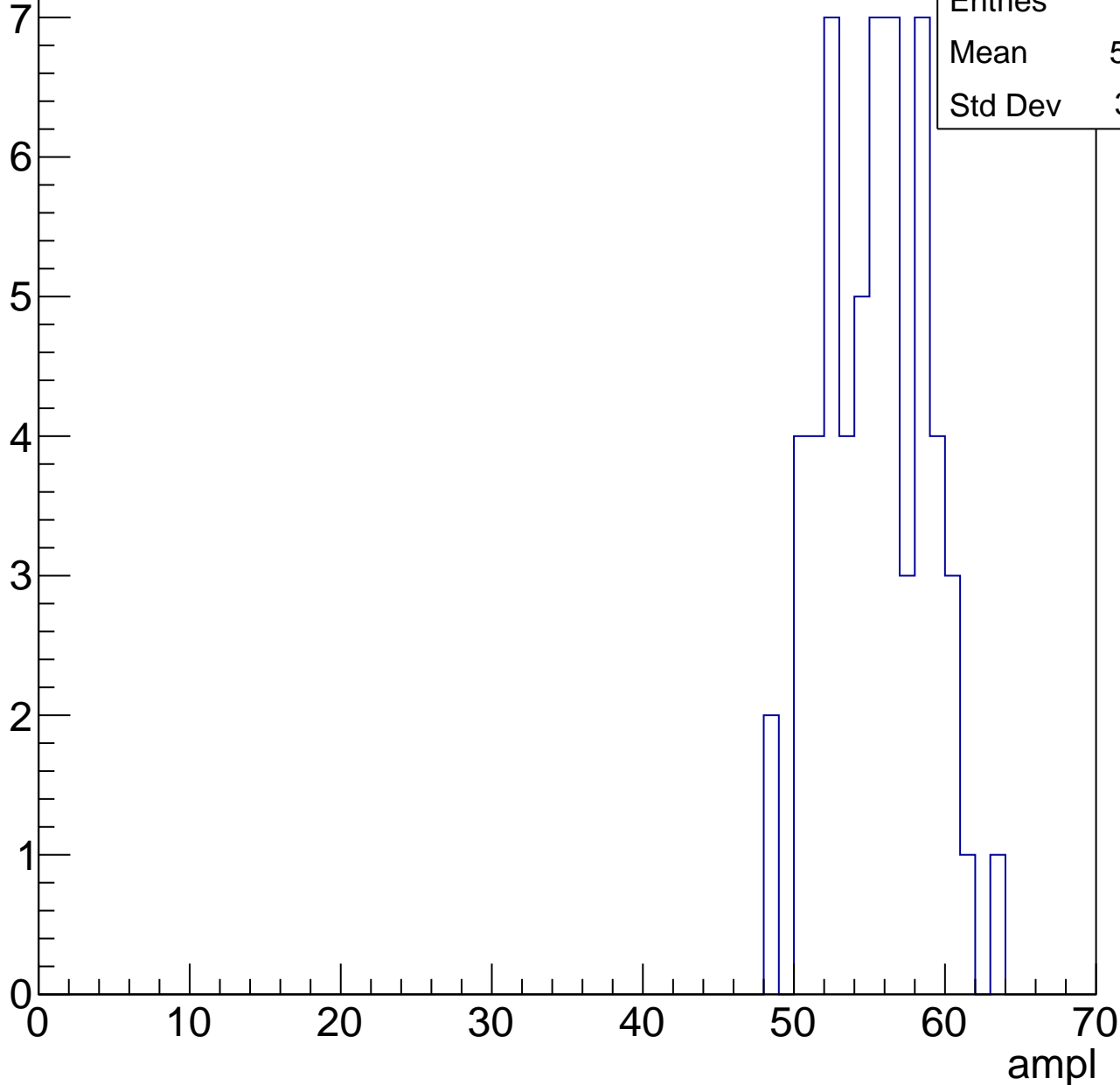


B1L103S, U5-ch125, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	54.92
Std Dev	3.361

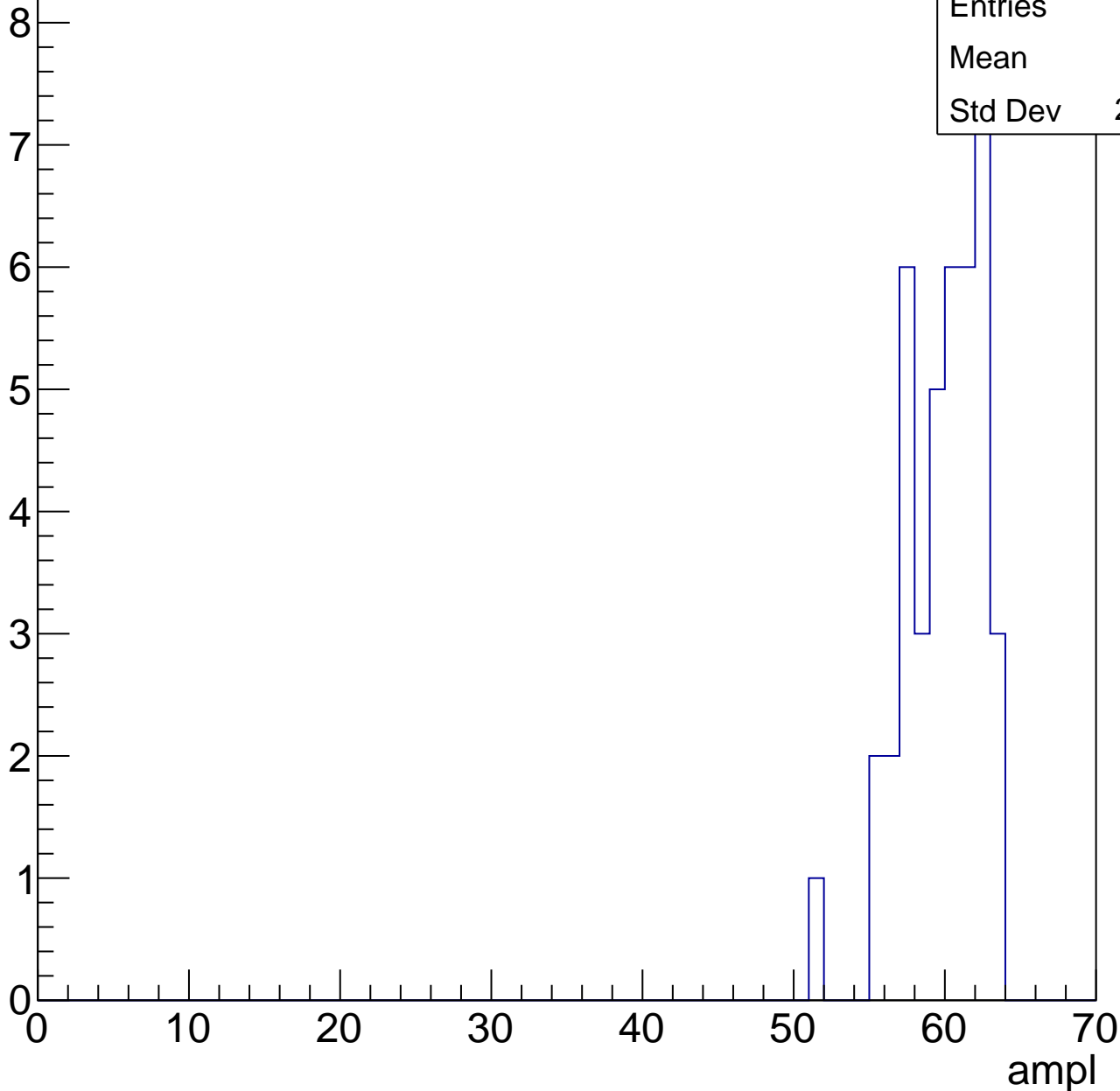


B1L103S, U5-ch125, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	42
Mean	59.4
Std Dev	2.601

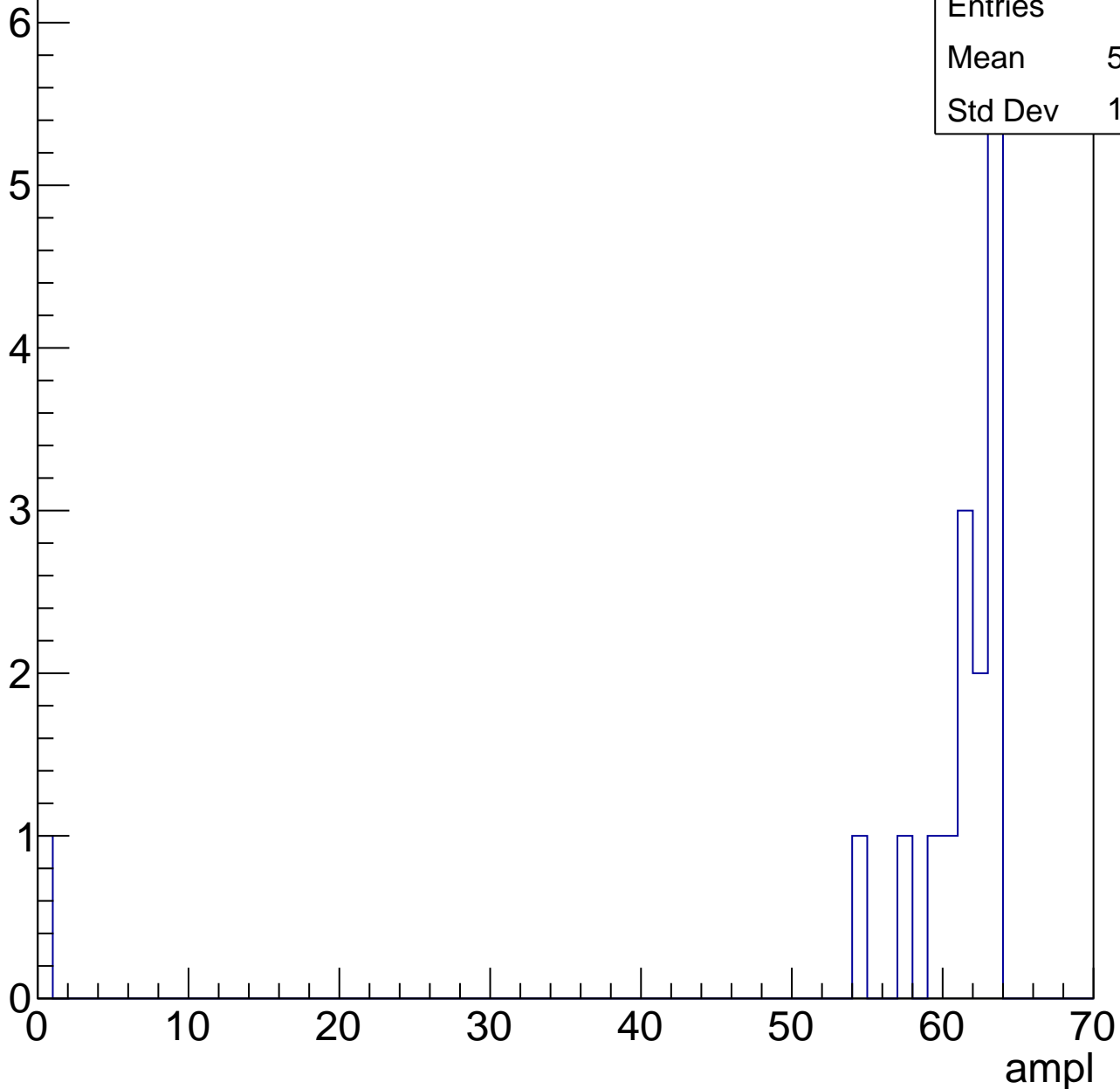


B1L103S, U5-ch125, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	16
Mean	57.19
Std Dev	14.97



B1L103S, U5-ch125, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

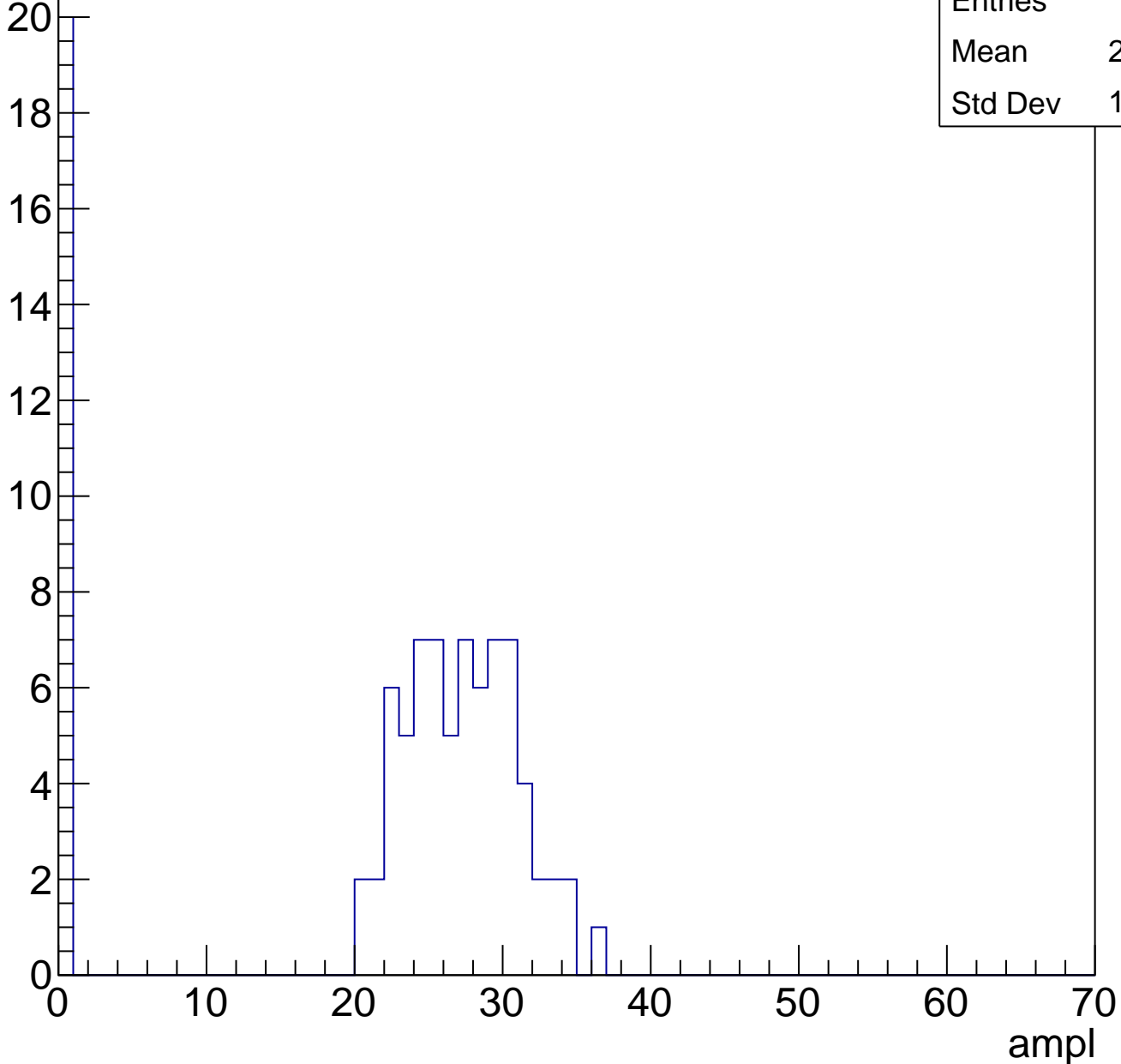
Entries	19
Mean	0
Std Dev	0

B1L103S, U5-ch126, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	92
Mean	20.98
Std Dev	11.52

Entry

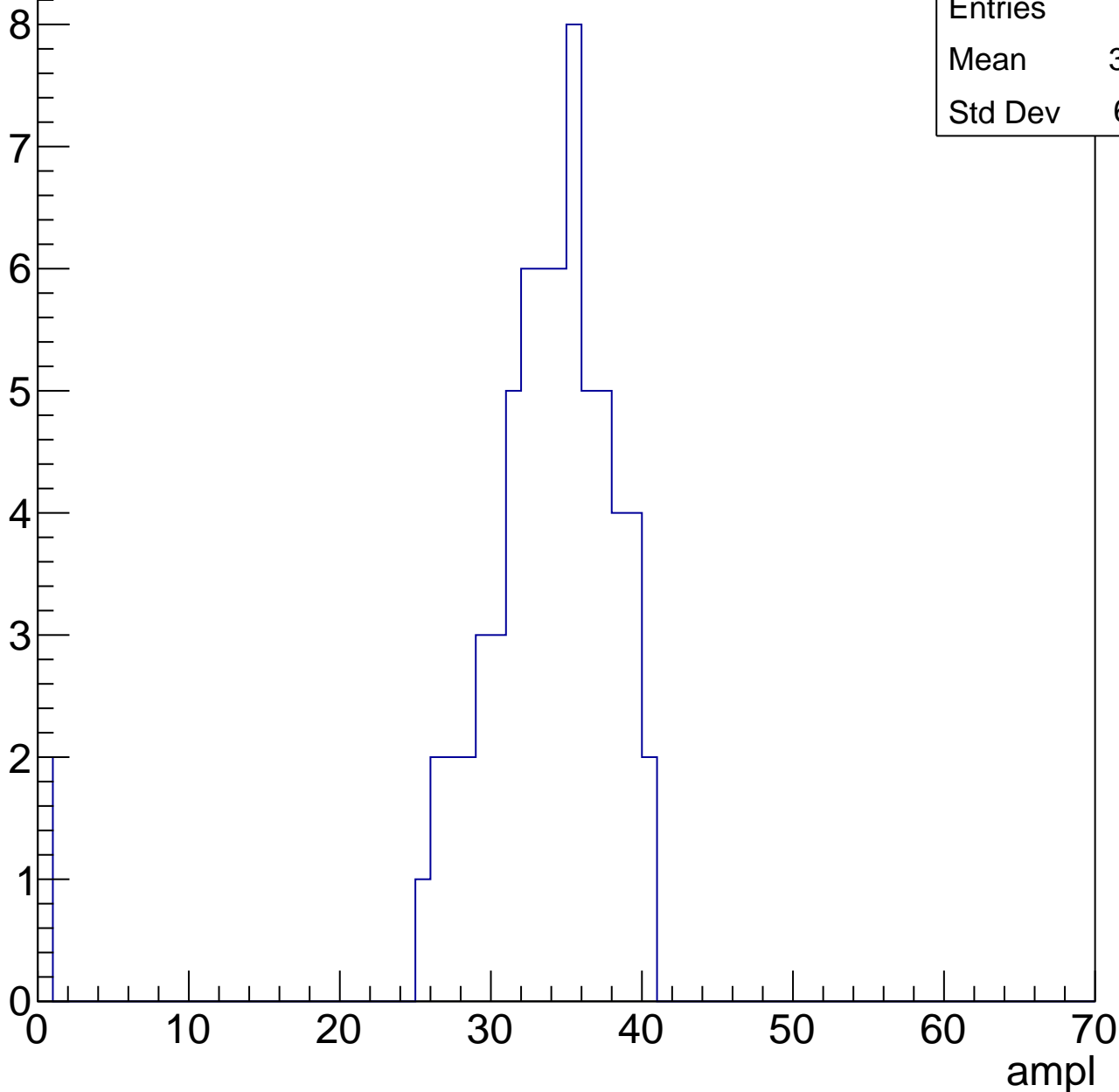


B1L103S, U5-ch126, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	32.52
Std Dev	6.801

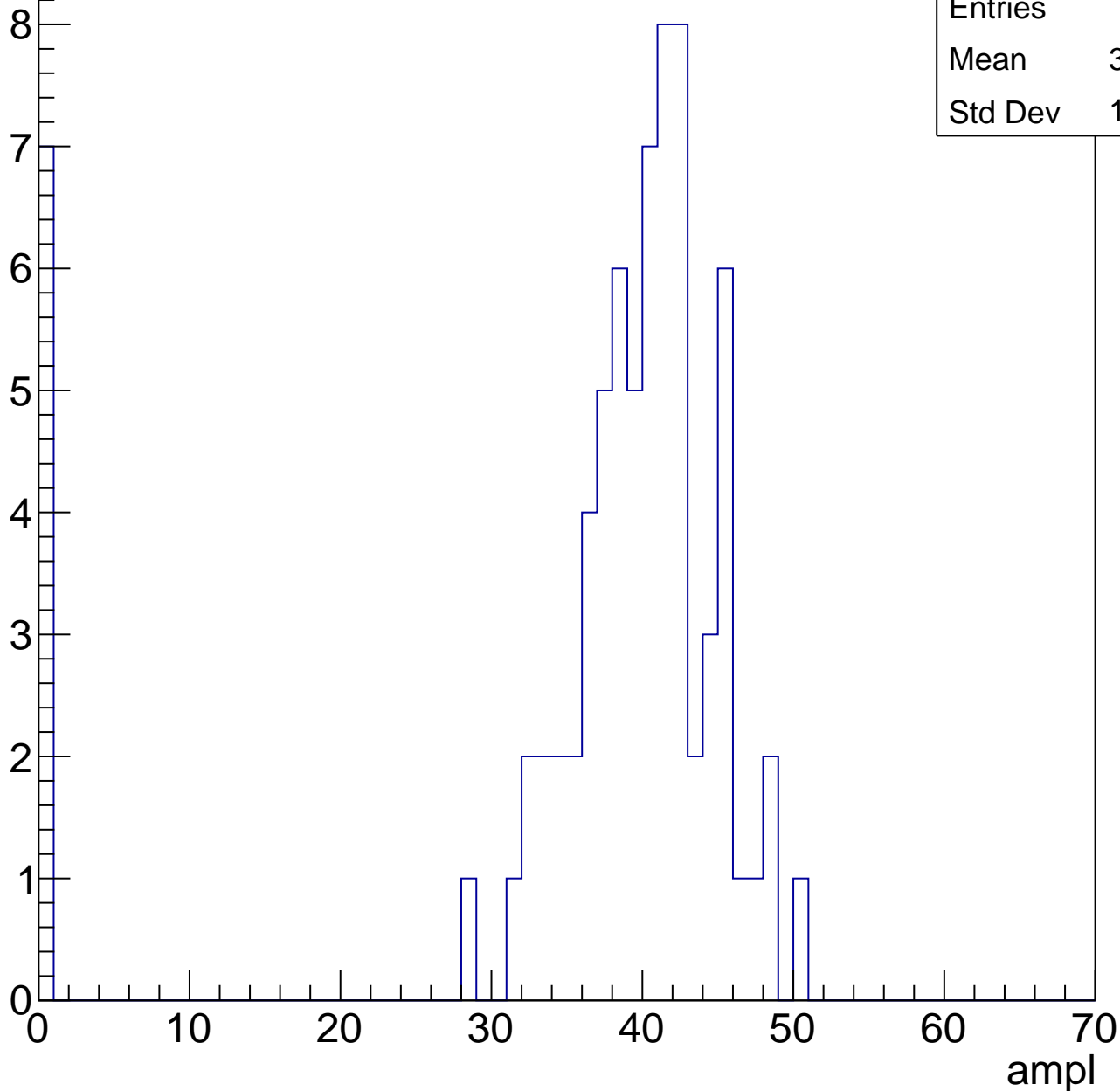


B1L103S, U5-ch126, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	36.18
Std Dev	12.23

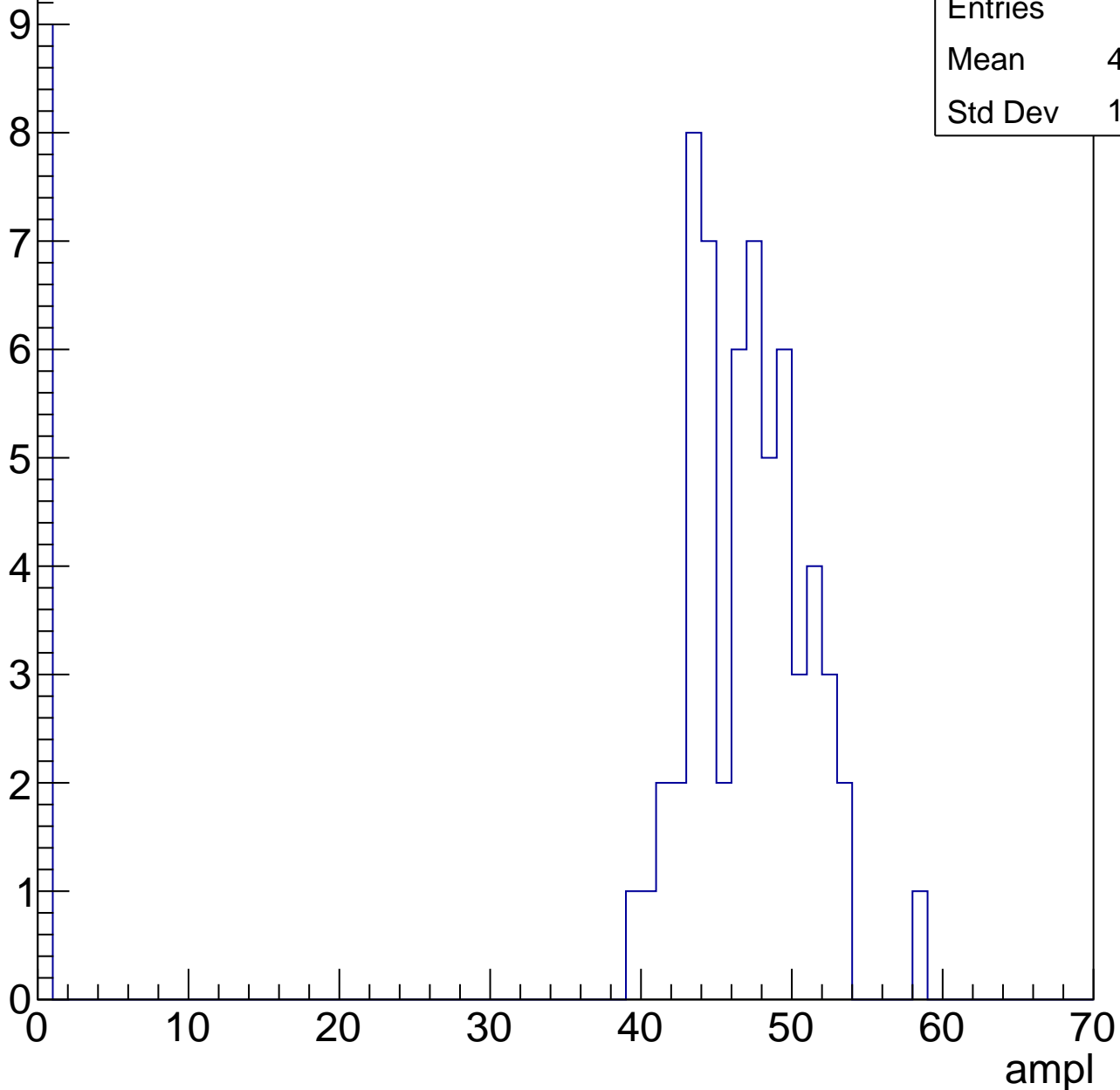


B1L103S, U5-ch126, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	40.58
Std Dev	16.09

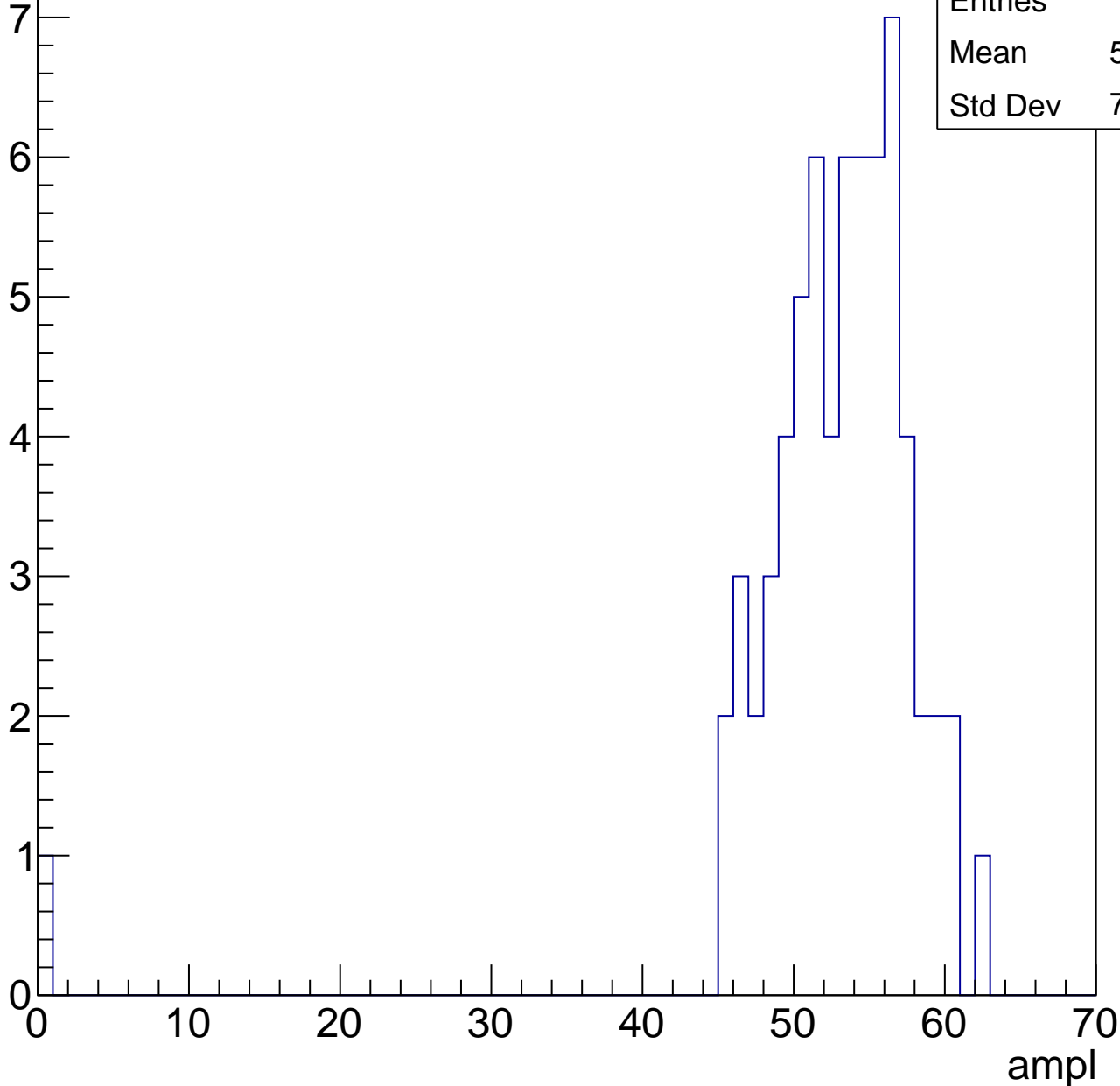


B1L103S, U5-ch126, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	52.03
Std Dev	7.552

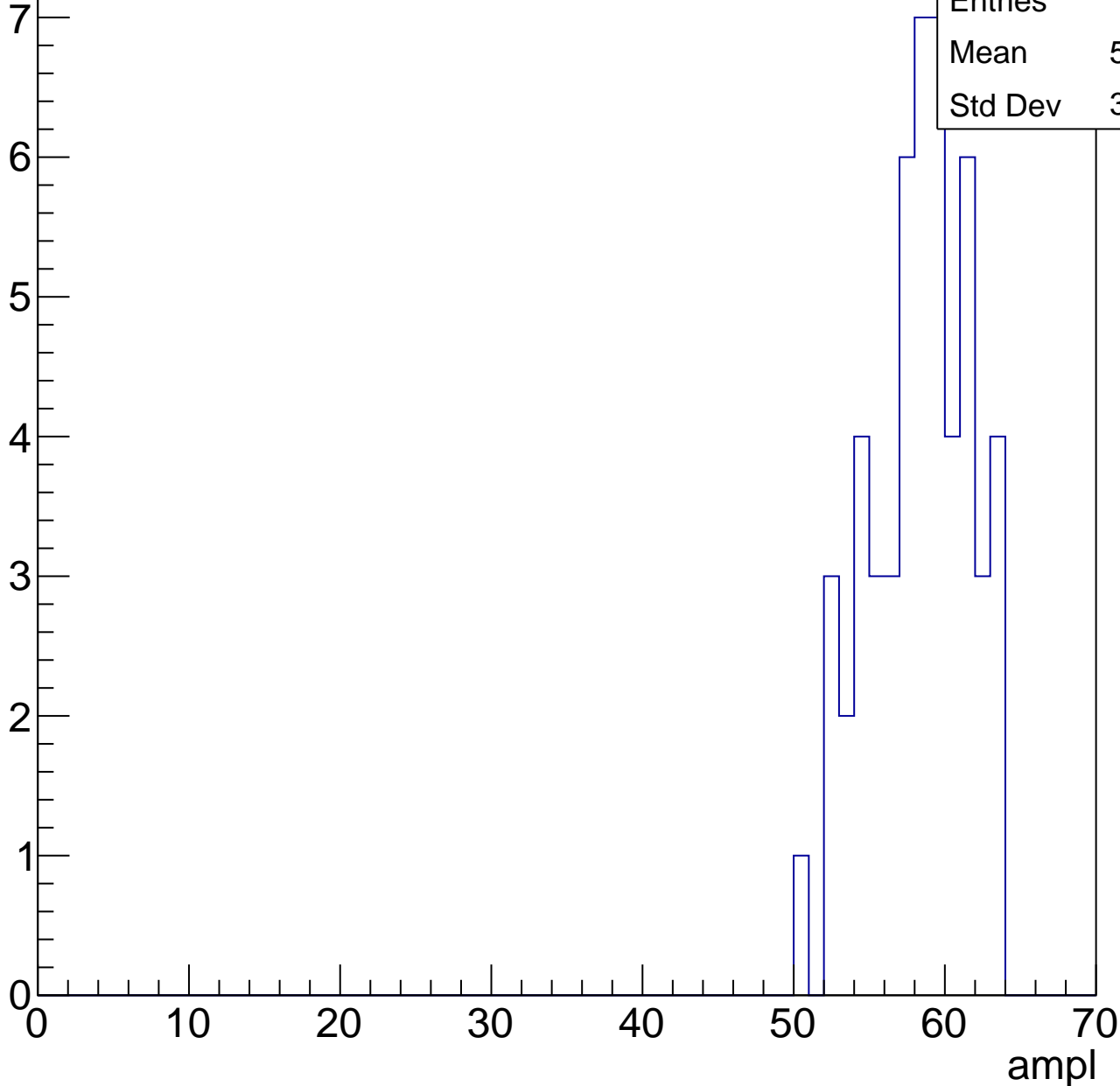


B1L103S, U5-ch126, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	57.85
Std Dev	3.235

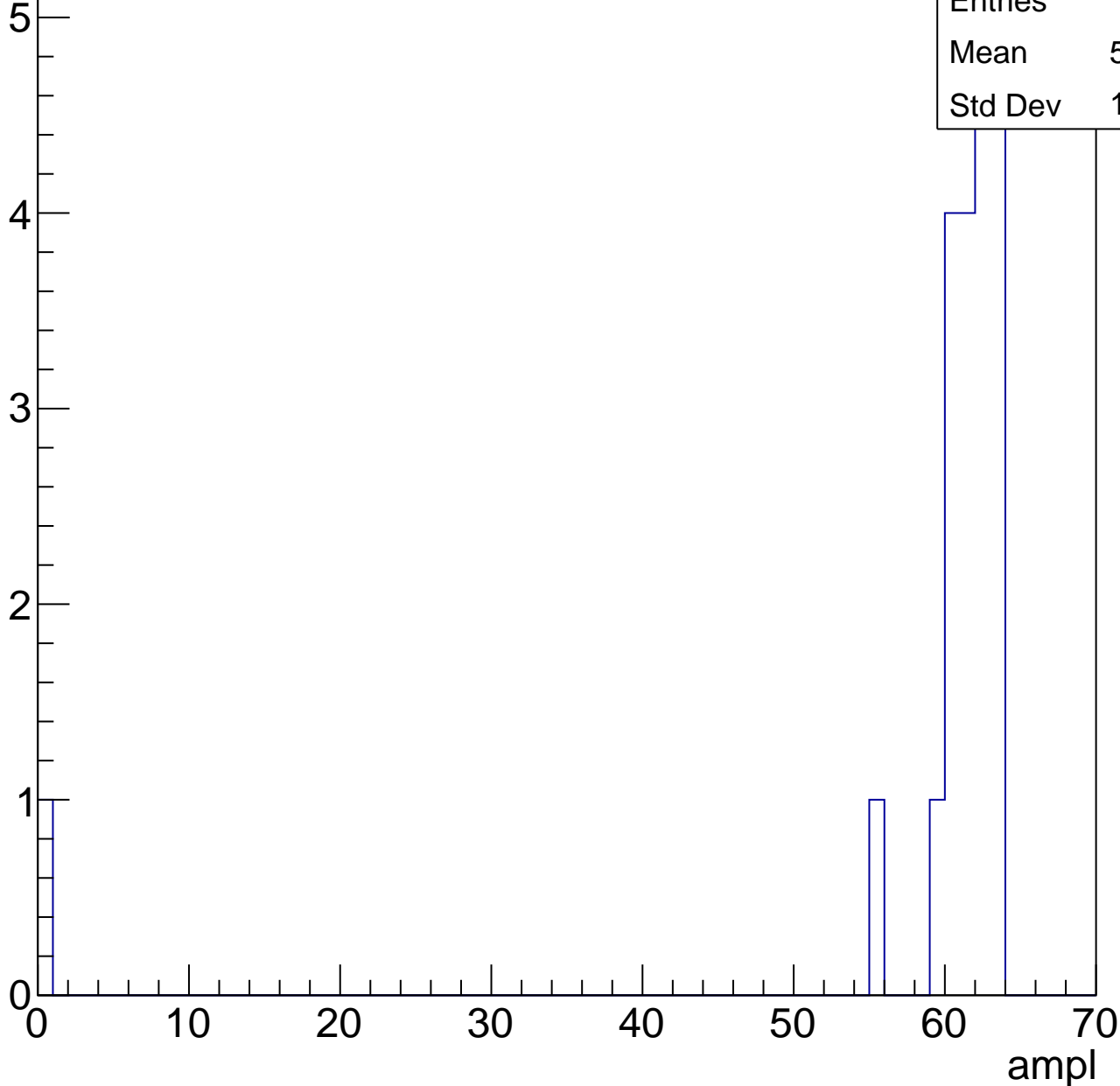


B1L103S, U5-ch126, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	21
Mean	58.24
Std Dev	13.15

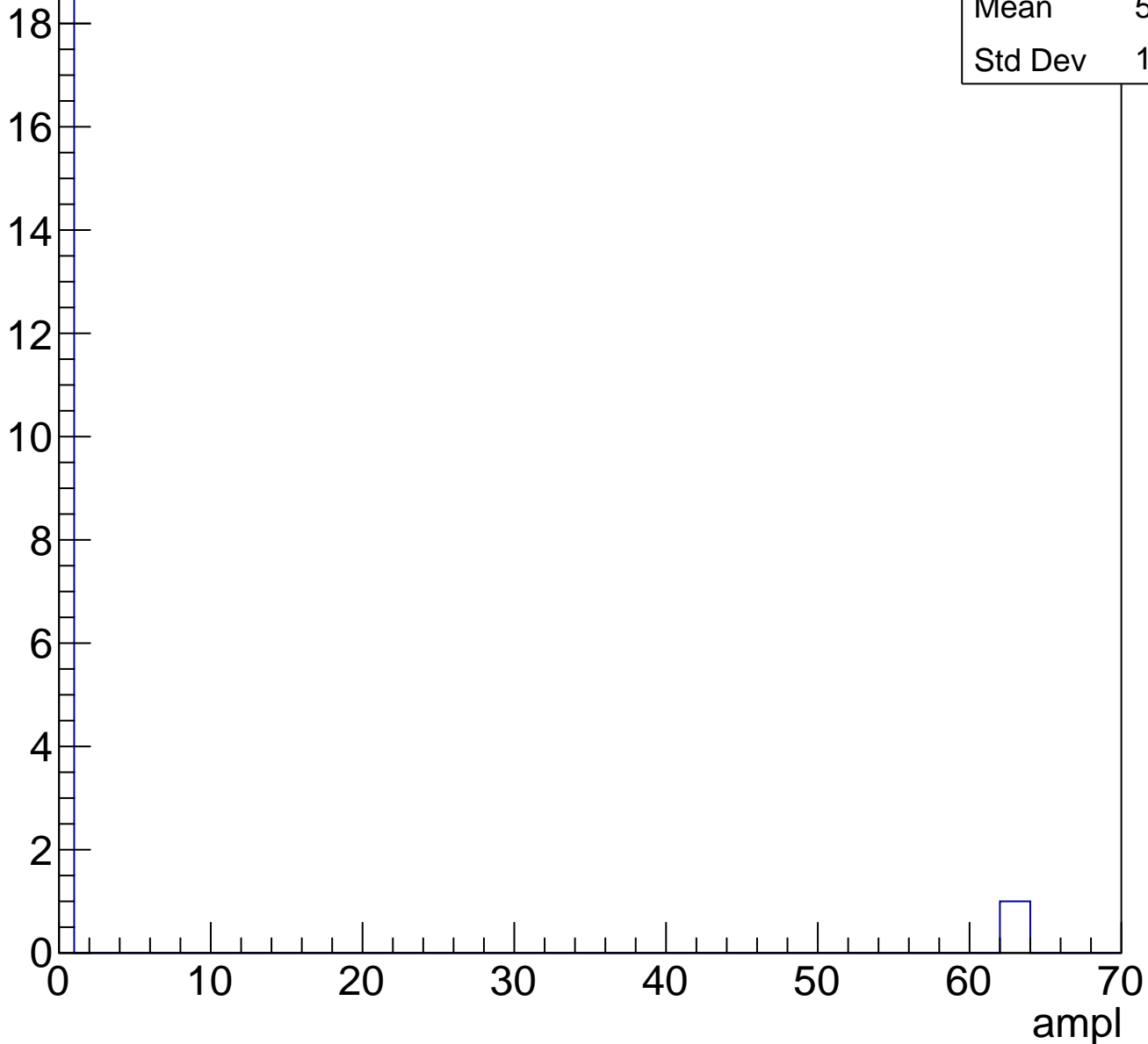


B1L103S, U5-ch126, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	5.952
Std Dev	18.35

Entry



B1L103S, U5-ch127, adc0

calib_packv5_041523_1651.root, FC#0, port C2

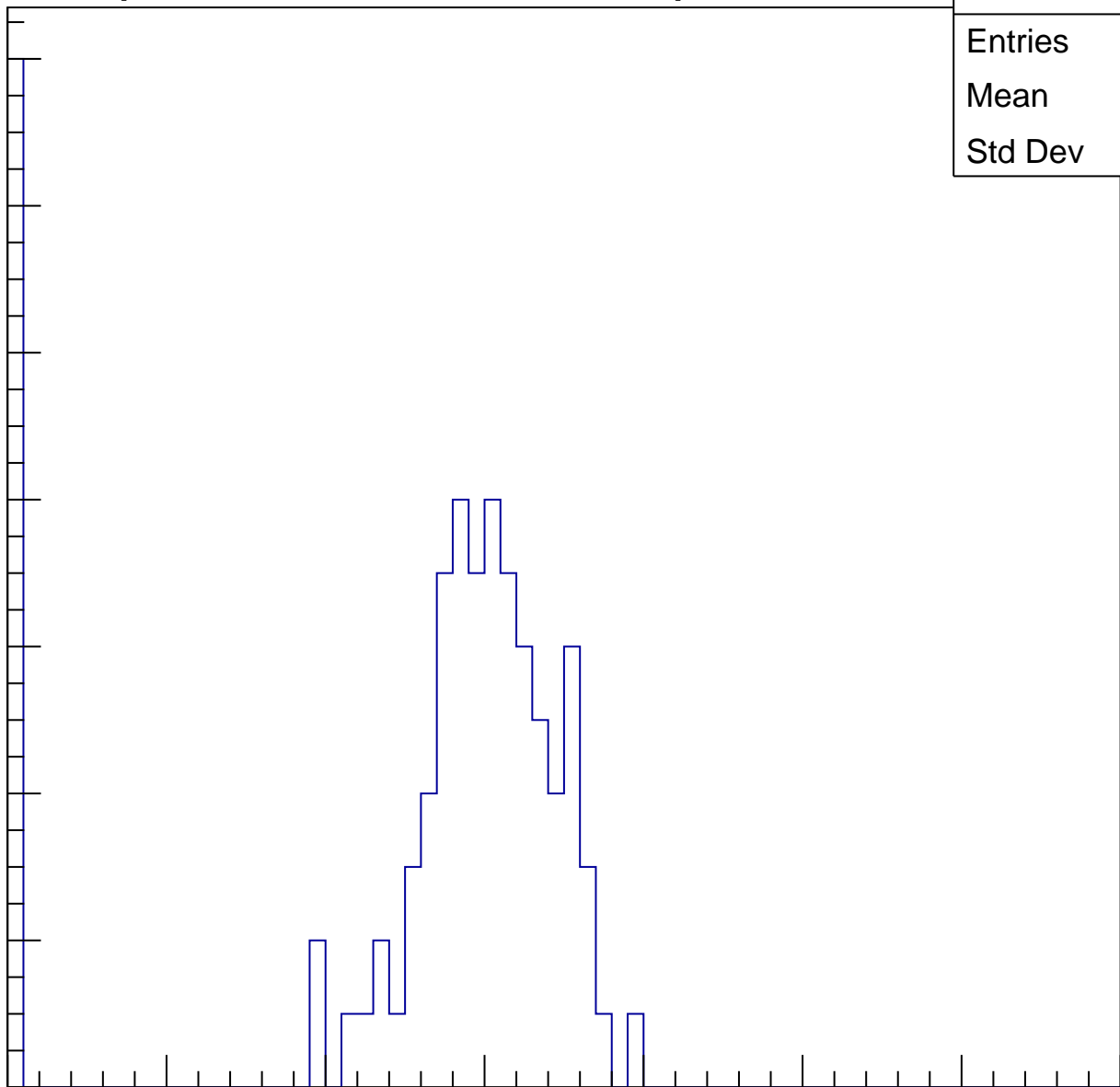
Entries	91
Mean	25.16
Std Dev	11.37

Entry

14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

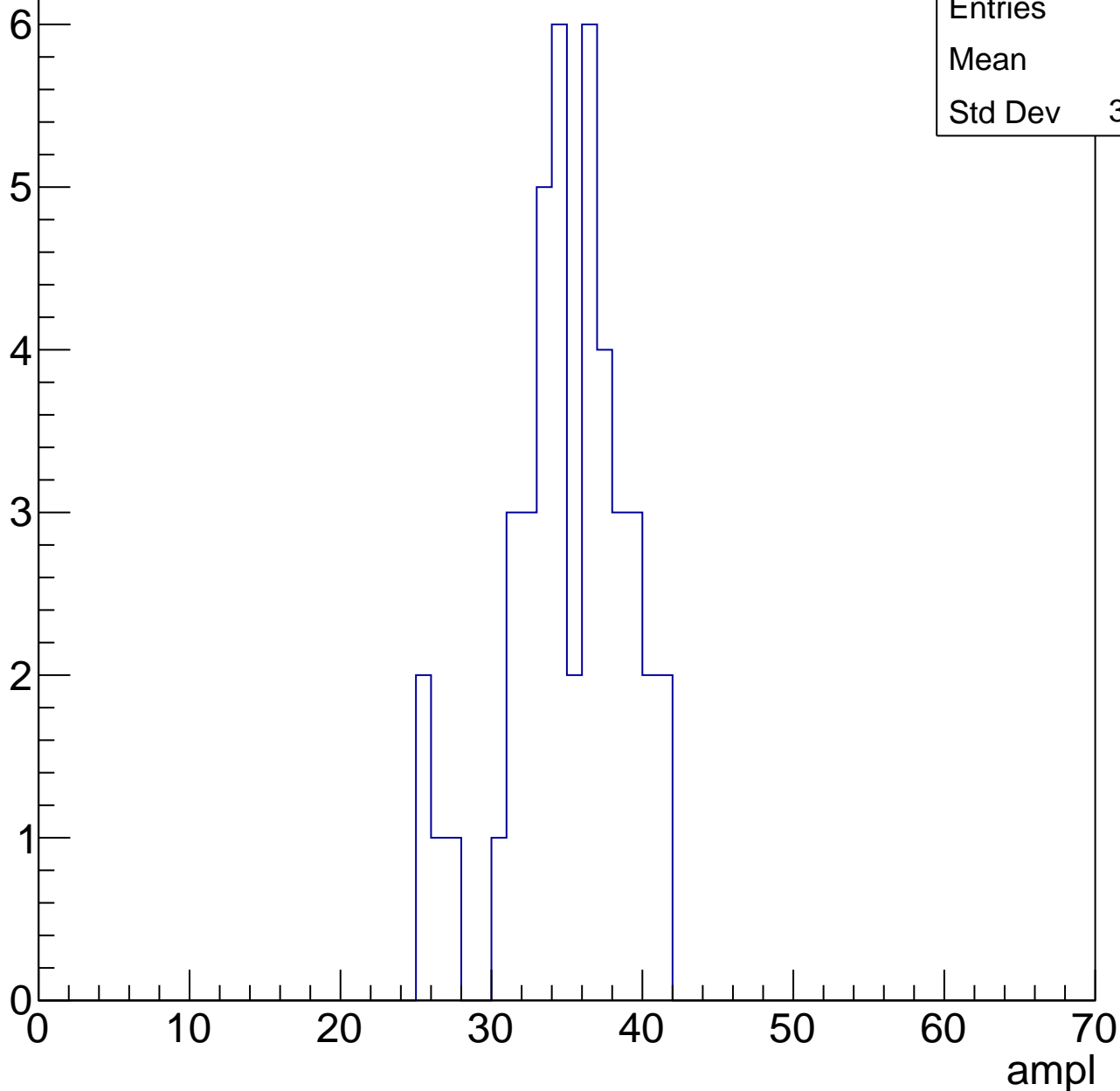


B1L103S, U5-ch127, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	44
Mean	34.5
Std Dev	3.928

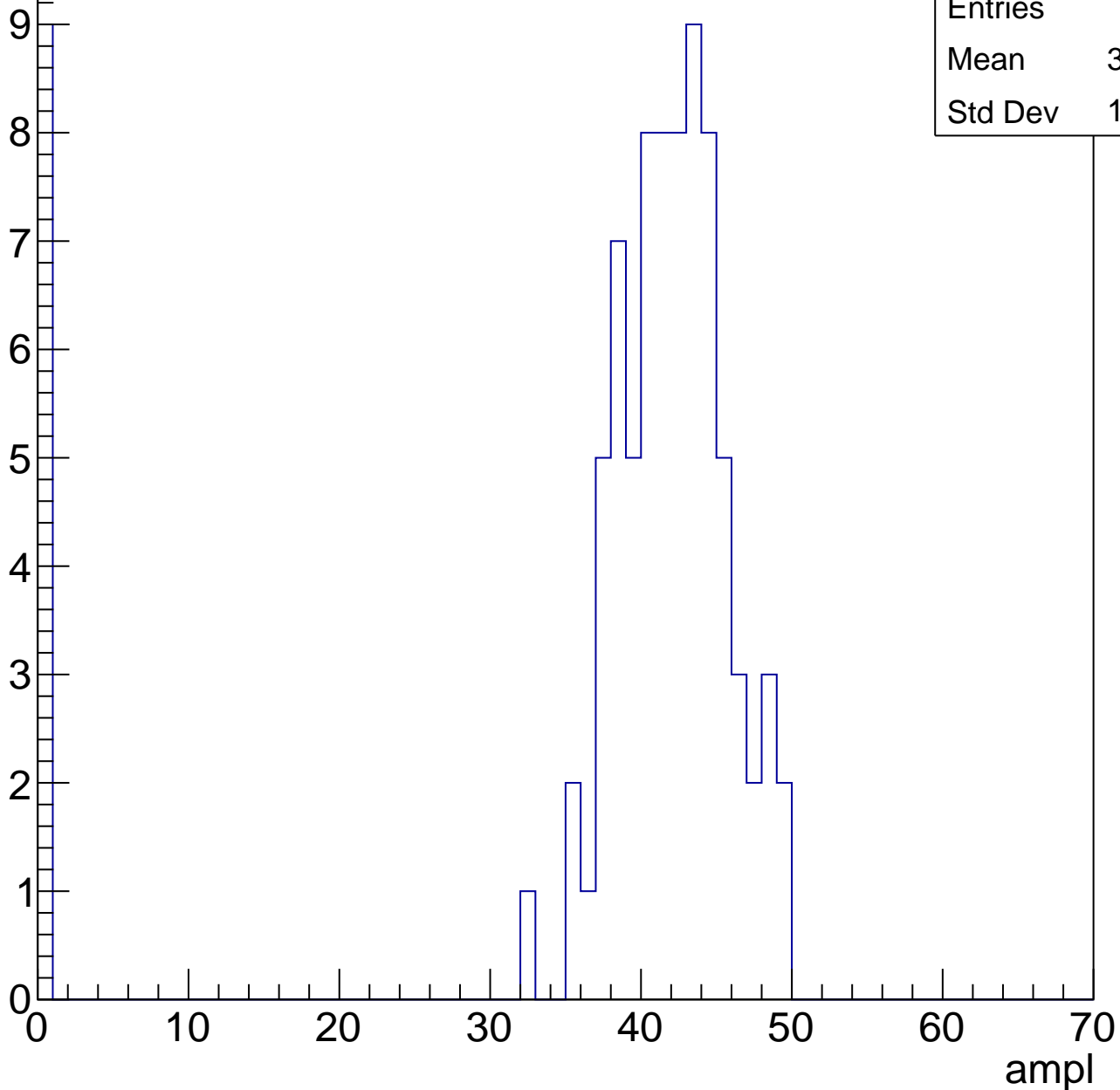


B1L103S, U5-ch127, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	86
Mean	37.28
Std Dev	13.17

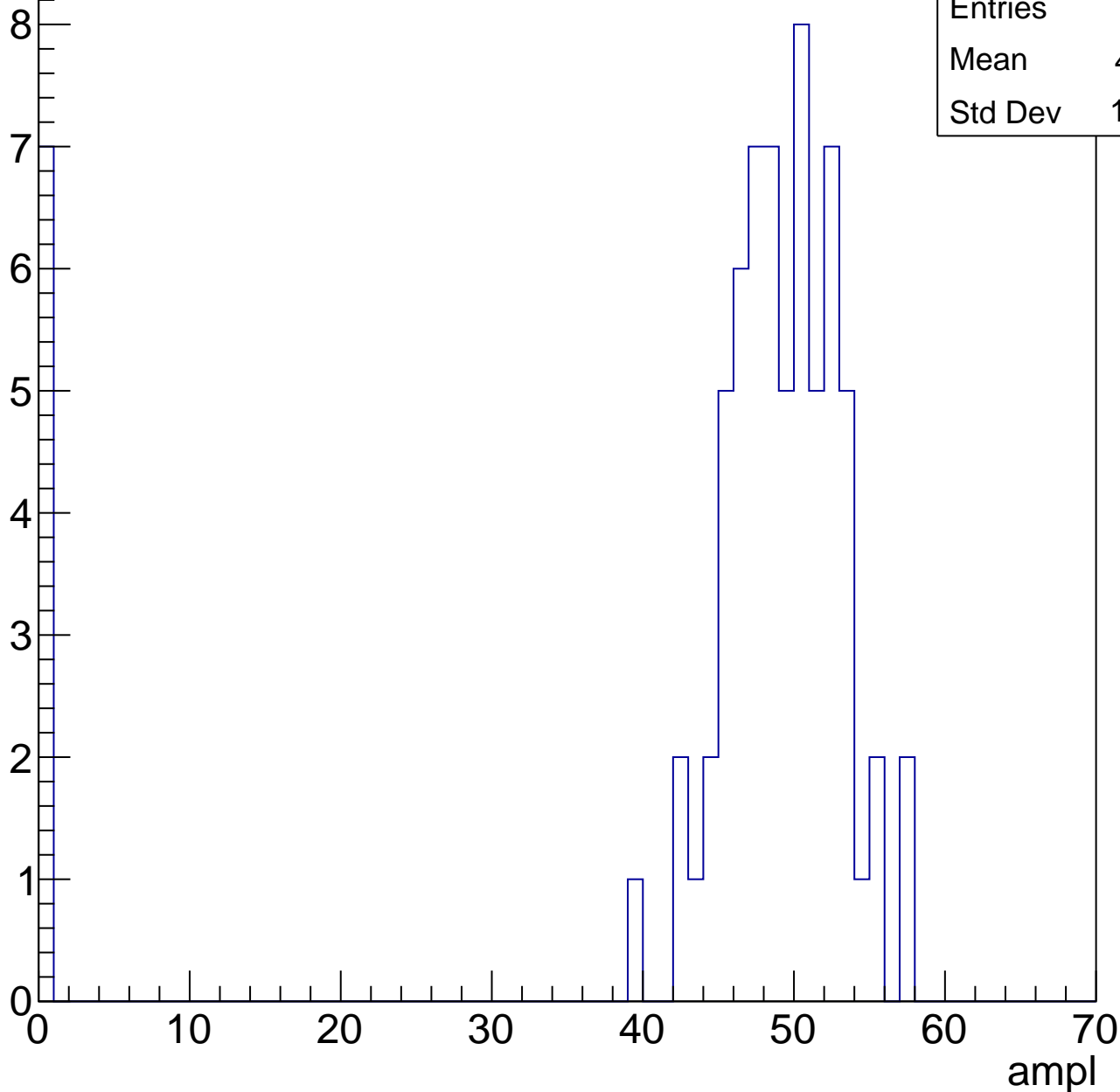


B1L103S, U5-ch127, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	44.21
Std Dev	14.79

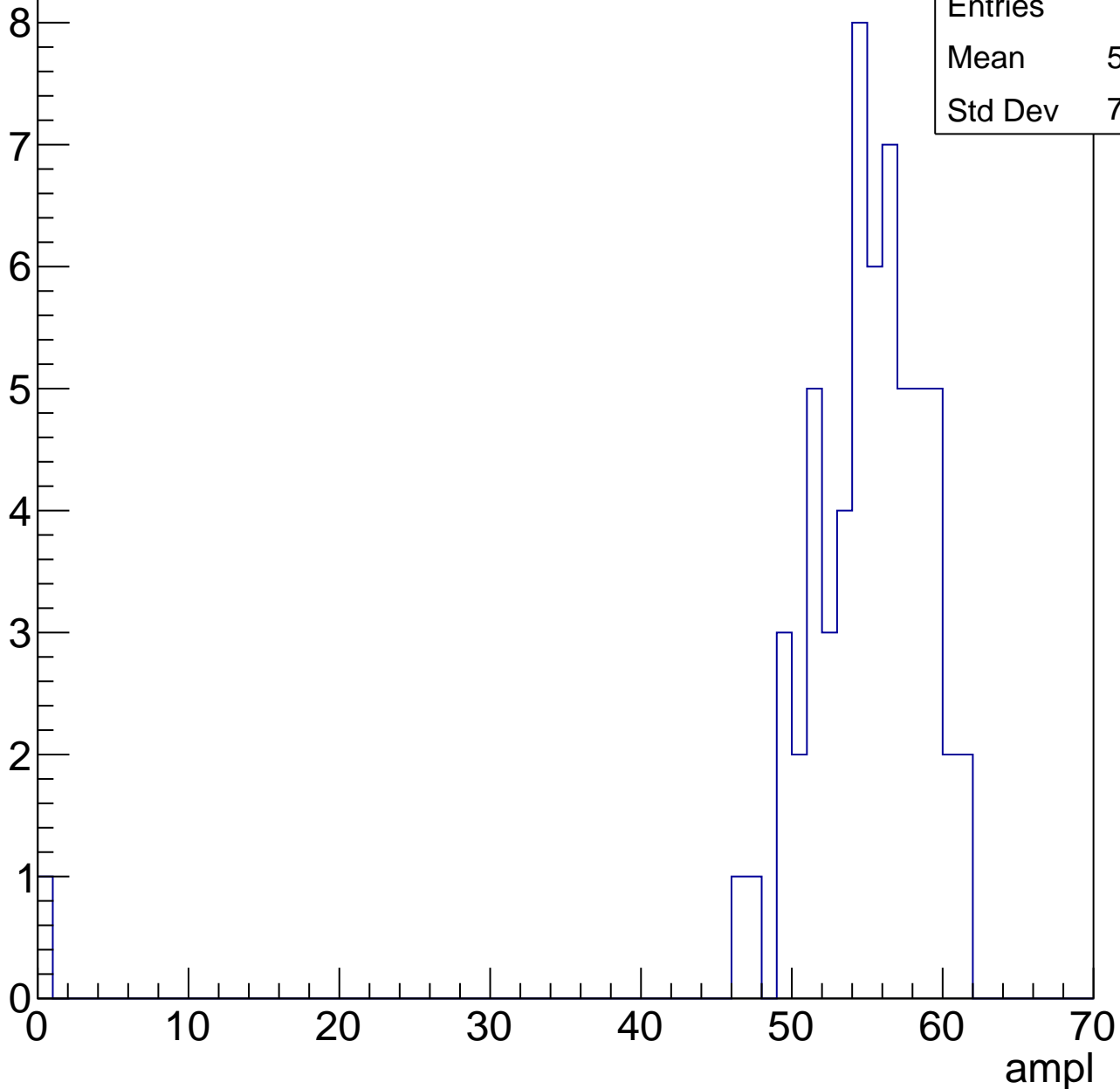


B1L103S, U5-ch127, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	53.82
Std Dev	7.798

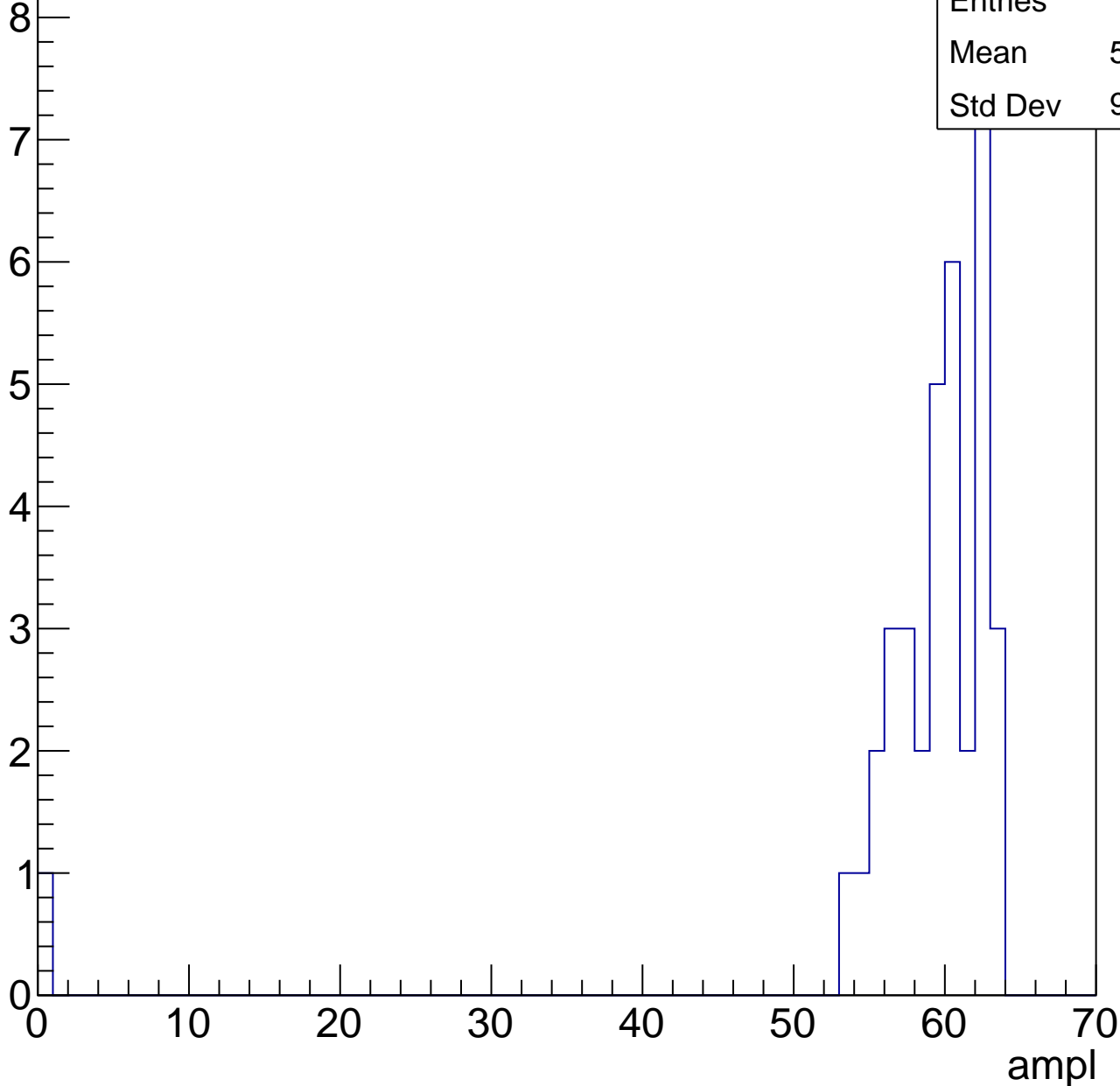


B1L103S, U5-ch127, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	37
Mean	57.68
Std Dev	9.979

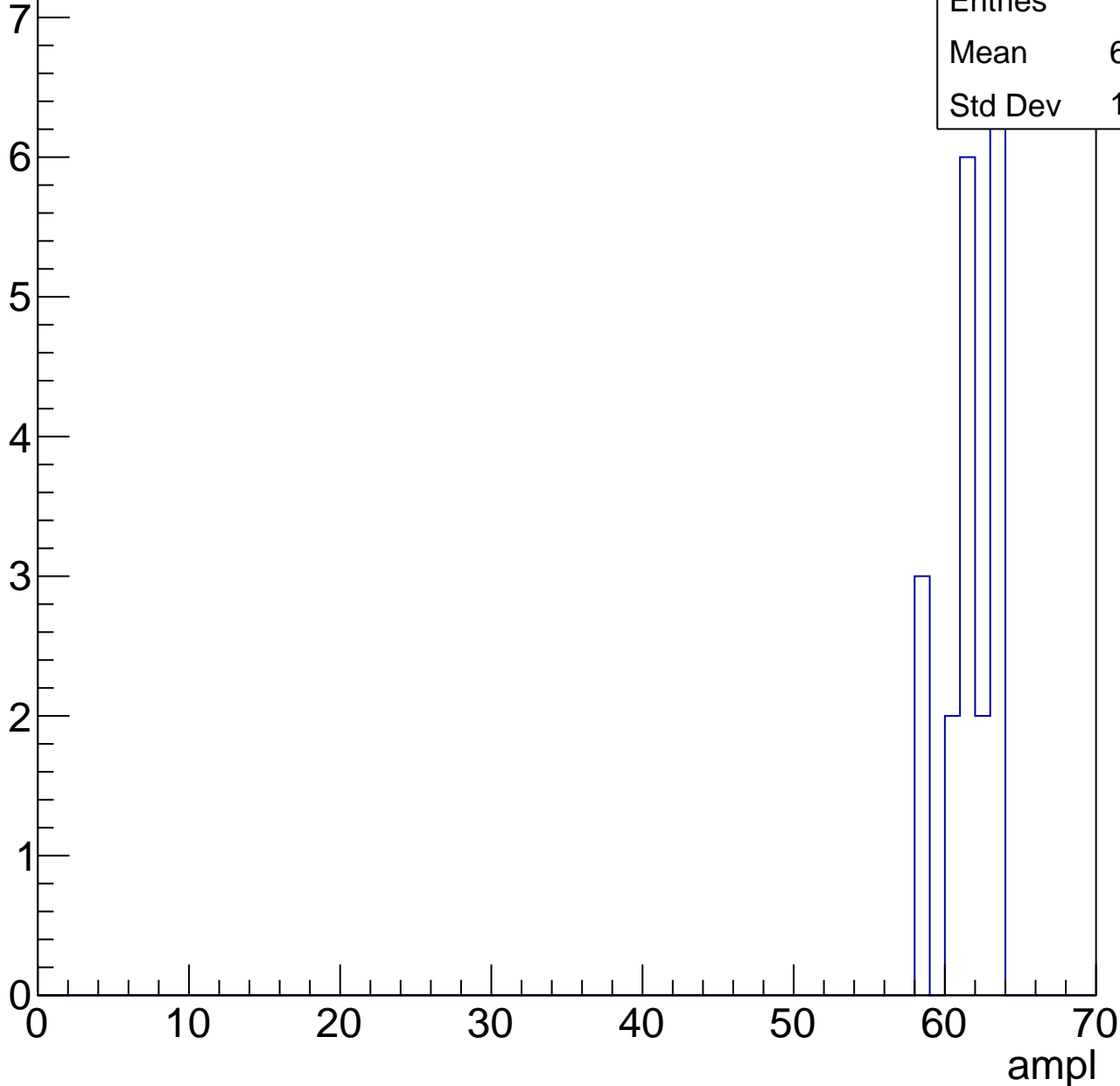


B1L103S, U5-ch127, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	20
Mean	61.25
Std Dev	1.699

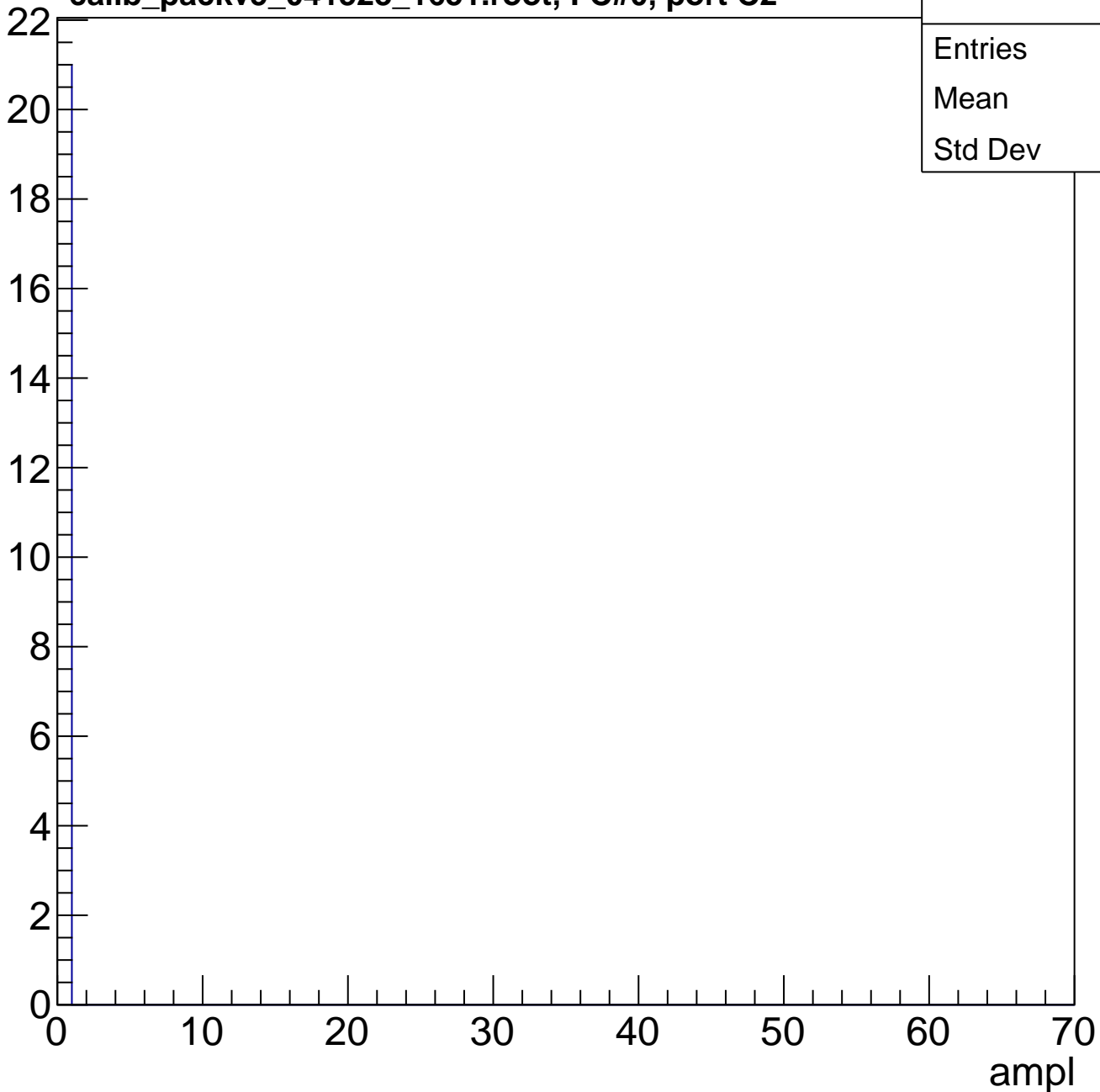


B1L103S, U5-ch127, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	0
Std Dev	0

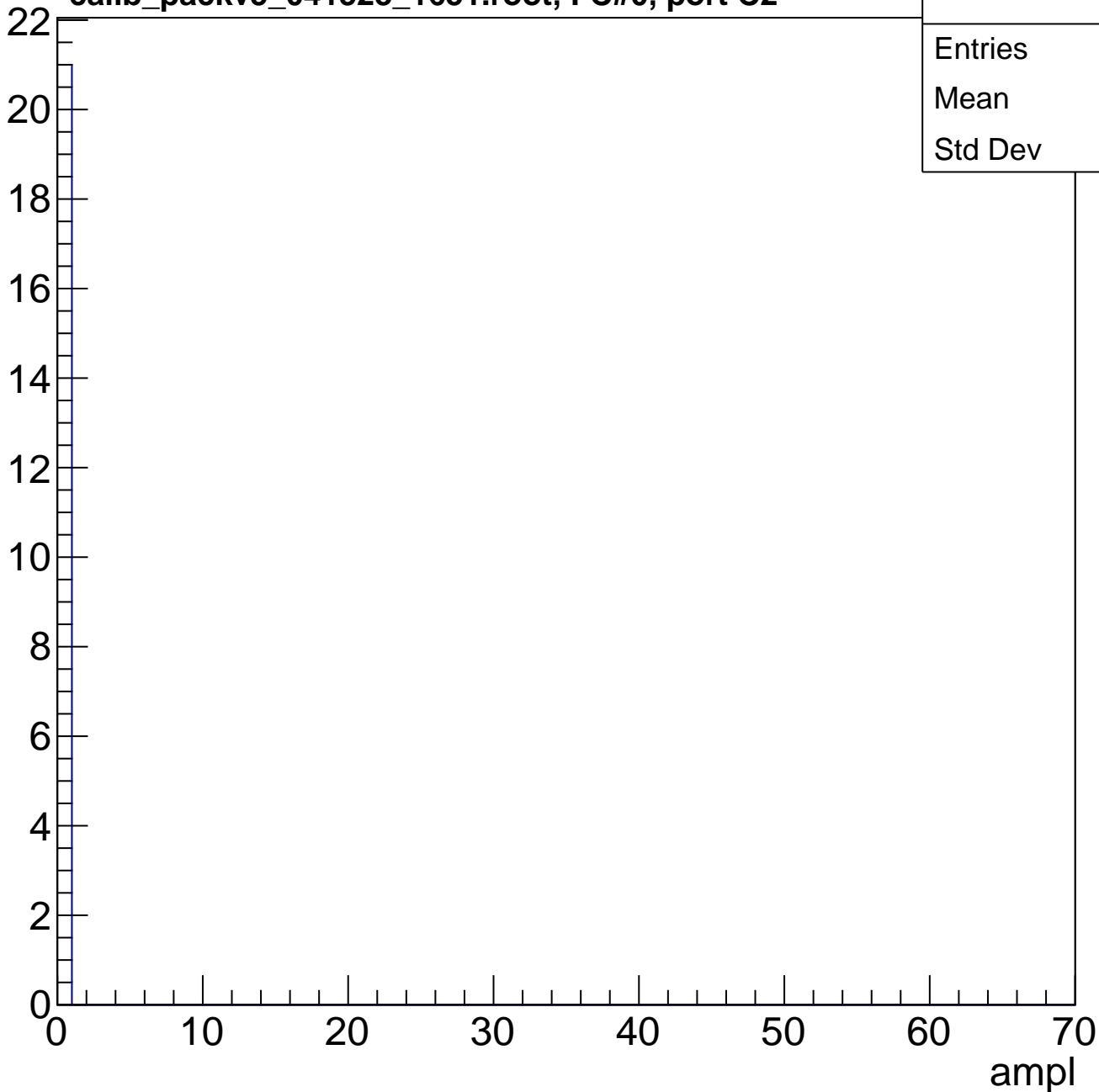
Entry



B1L103S, U5-ch127, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	21
Mean	0
Std Dev	0