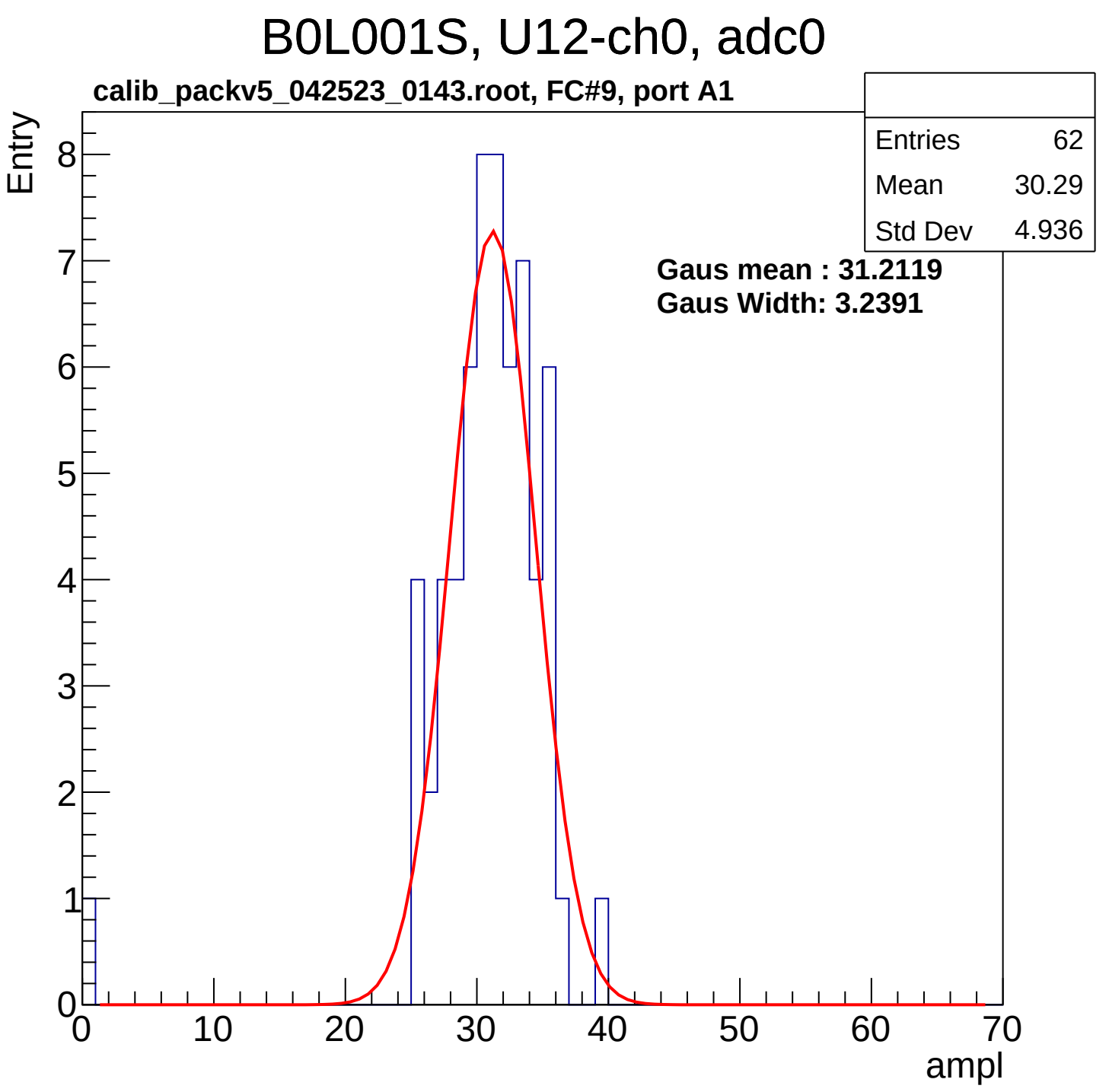
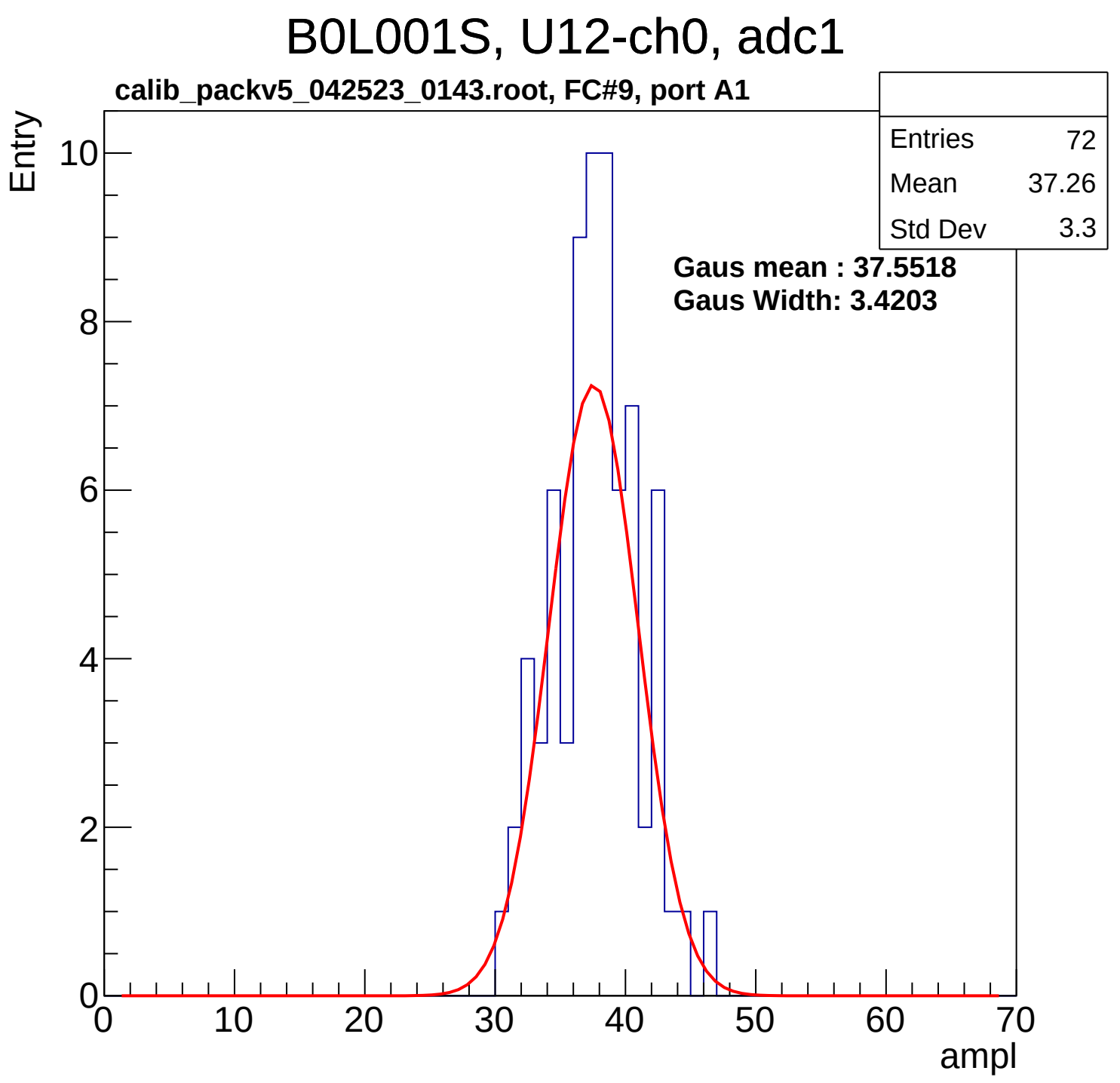
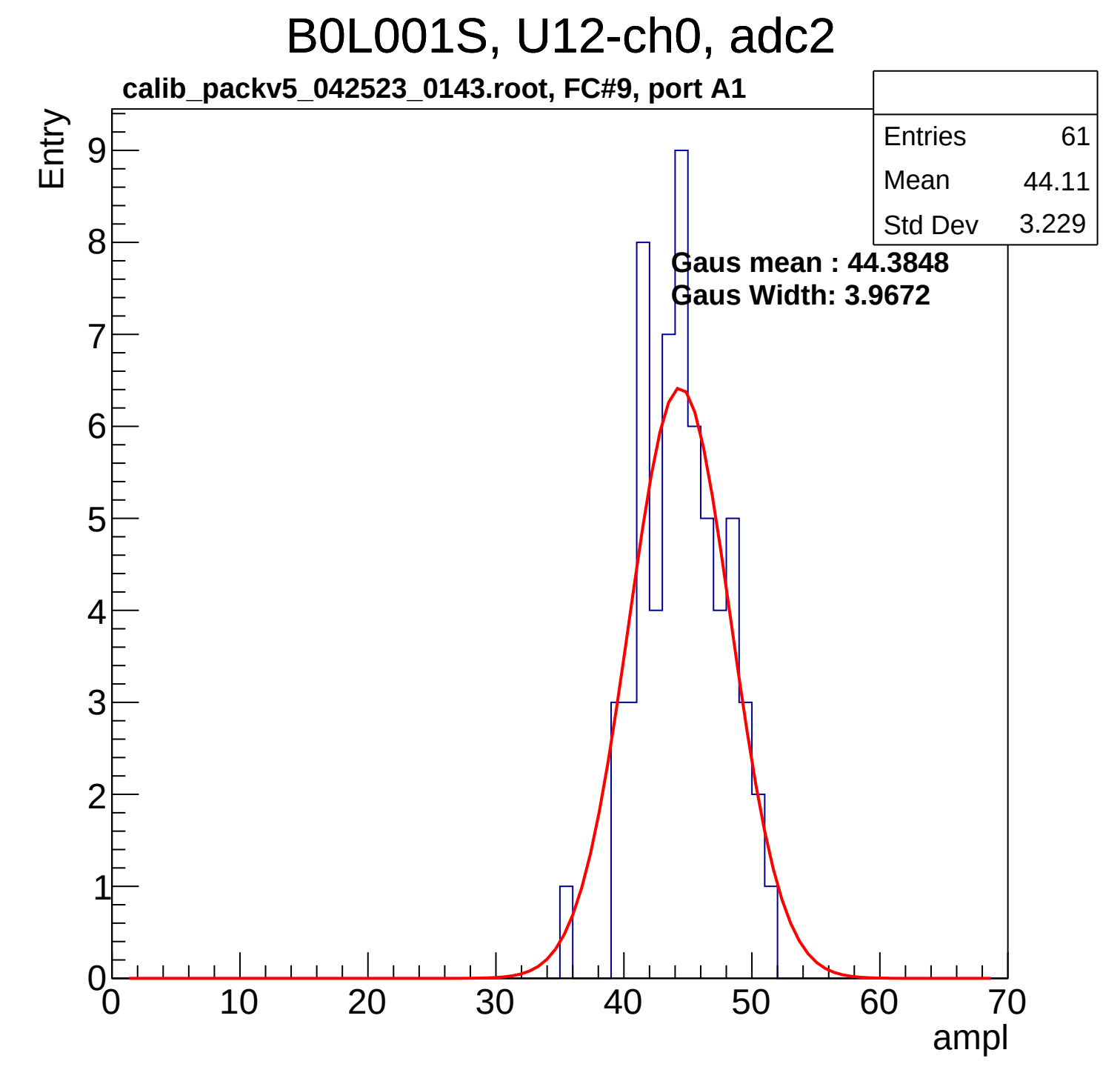

B0L001S, U12-ch0, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 62
Mean 30.29
Std Dev 4.936
Gaus mean : 31.2119
Gaus Width: 3.2391
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch0, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 72
Mean 37.26
Std Dev 3.3
Gaus mean : 37.5518
Gaus Width: 3.4203
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch0, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 61
Mean 44.11
Std Dev 3.229
Gaus mean : 44.3848
Gaus Width: 3.9672
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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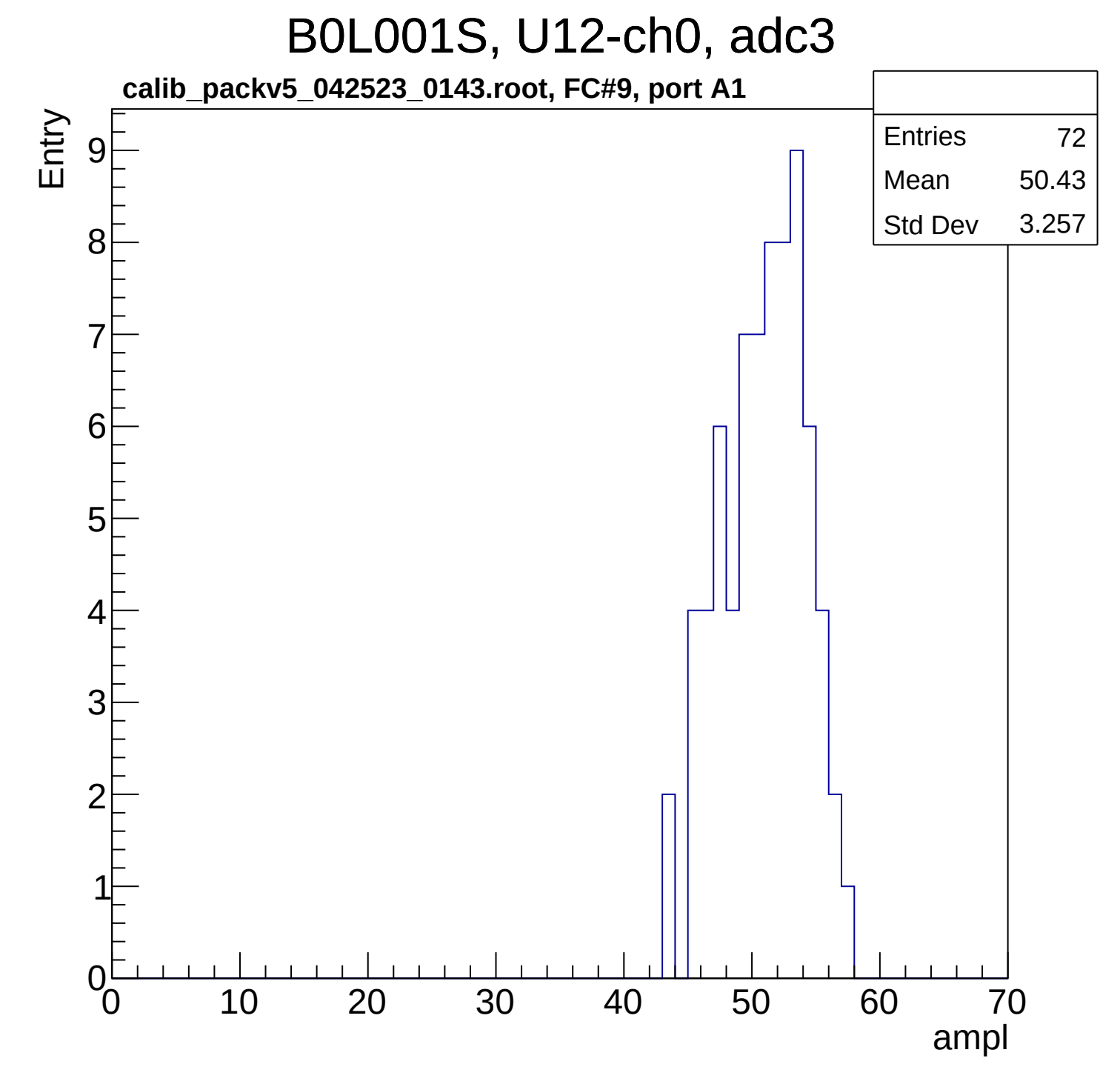
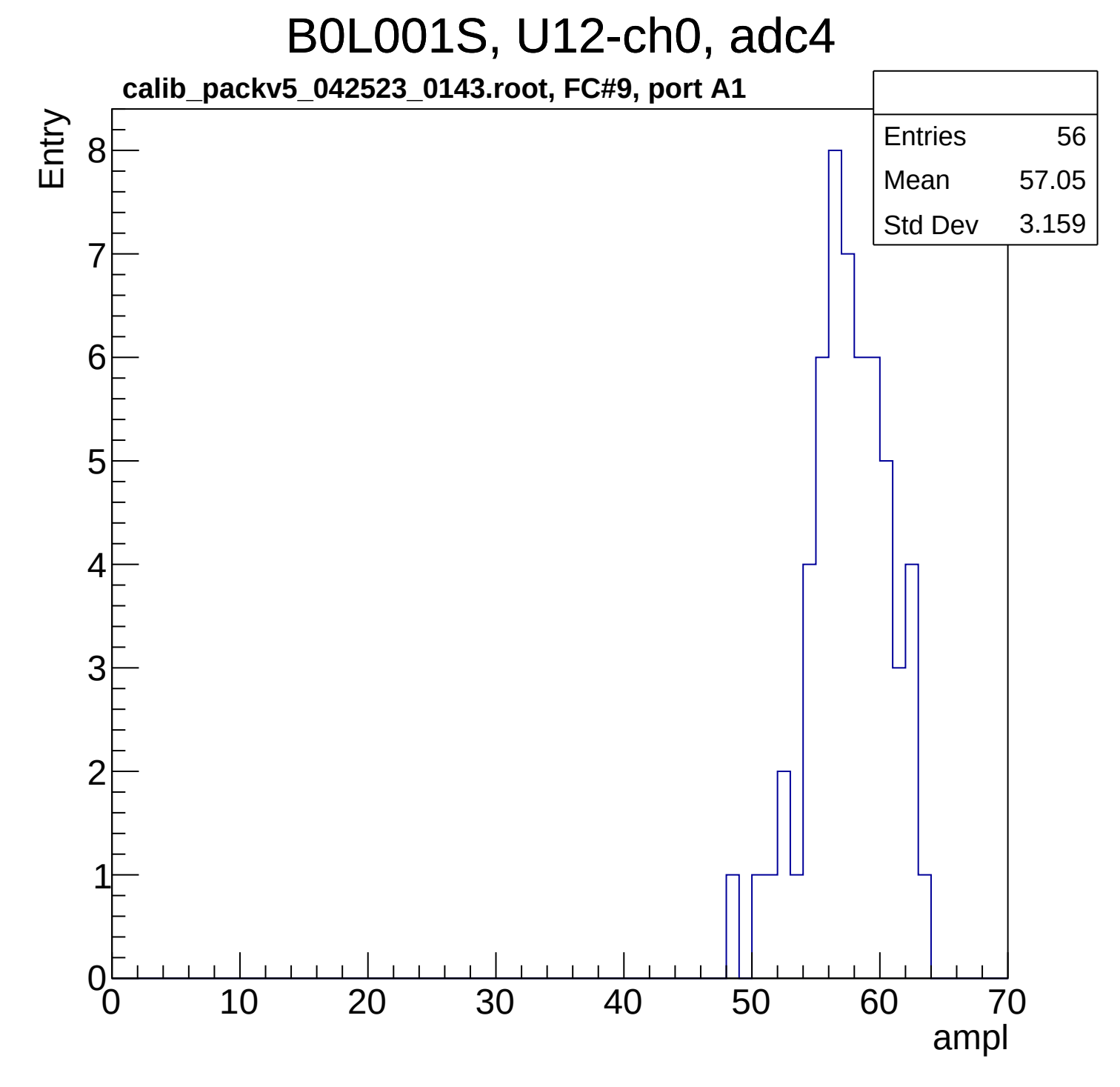

B0L001S, U12-ch0, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 72
Mean 50.43
Std Dev 3.257
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch0, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 56
Mean 57.05
Std Dev 3.159
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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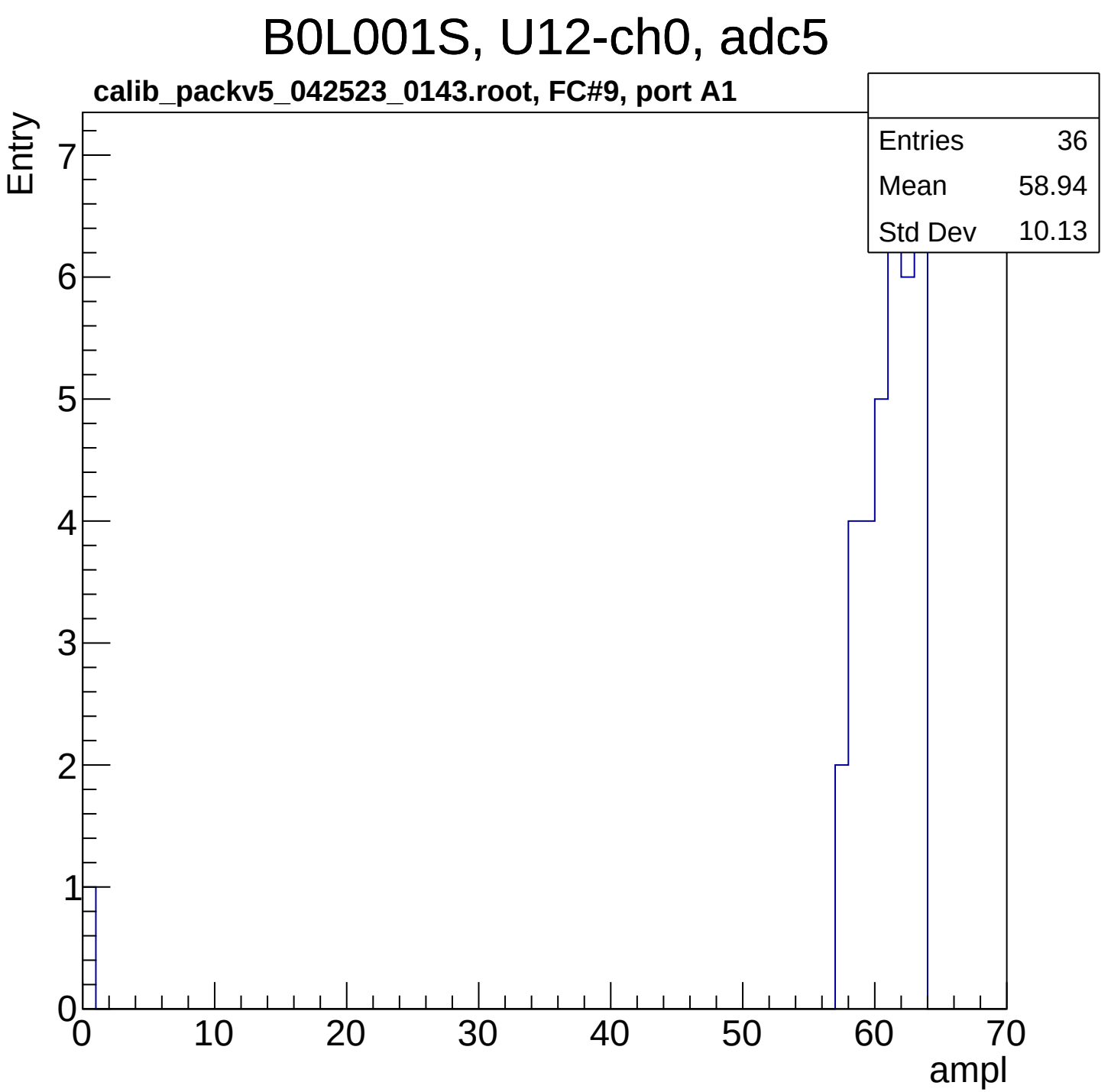
B0L001S, U12-ch0, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 36
Mean 58.94
Std Dev 10.13
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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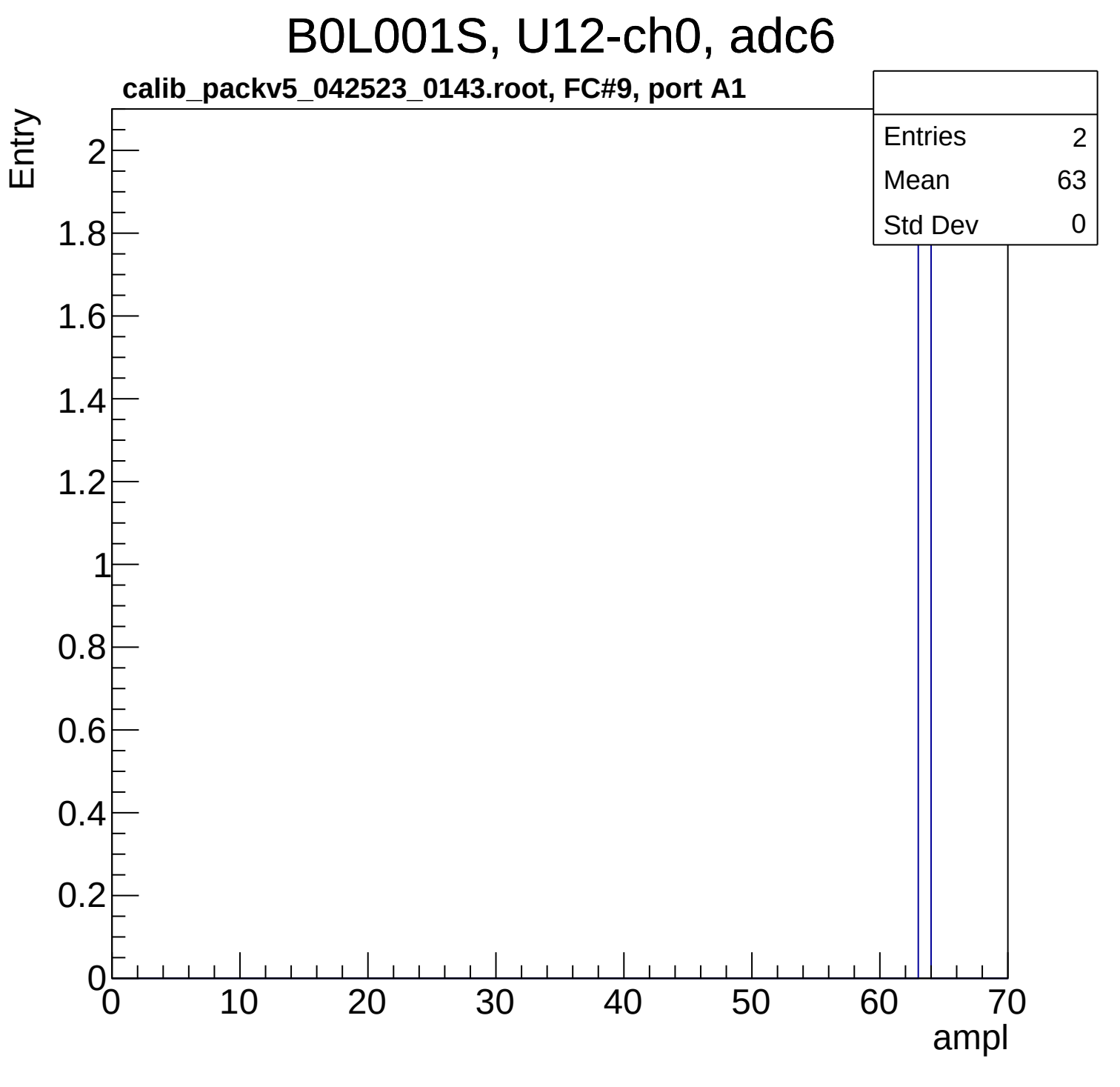
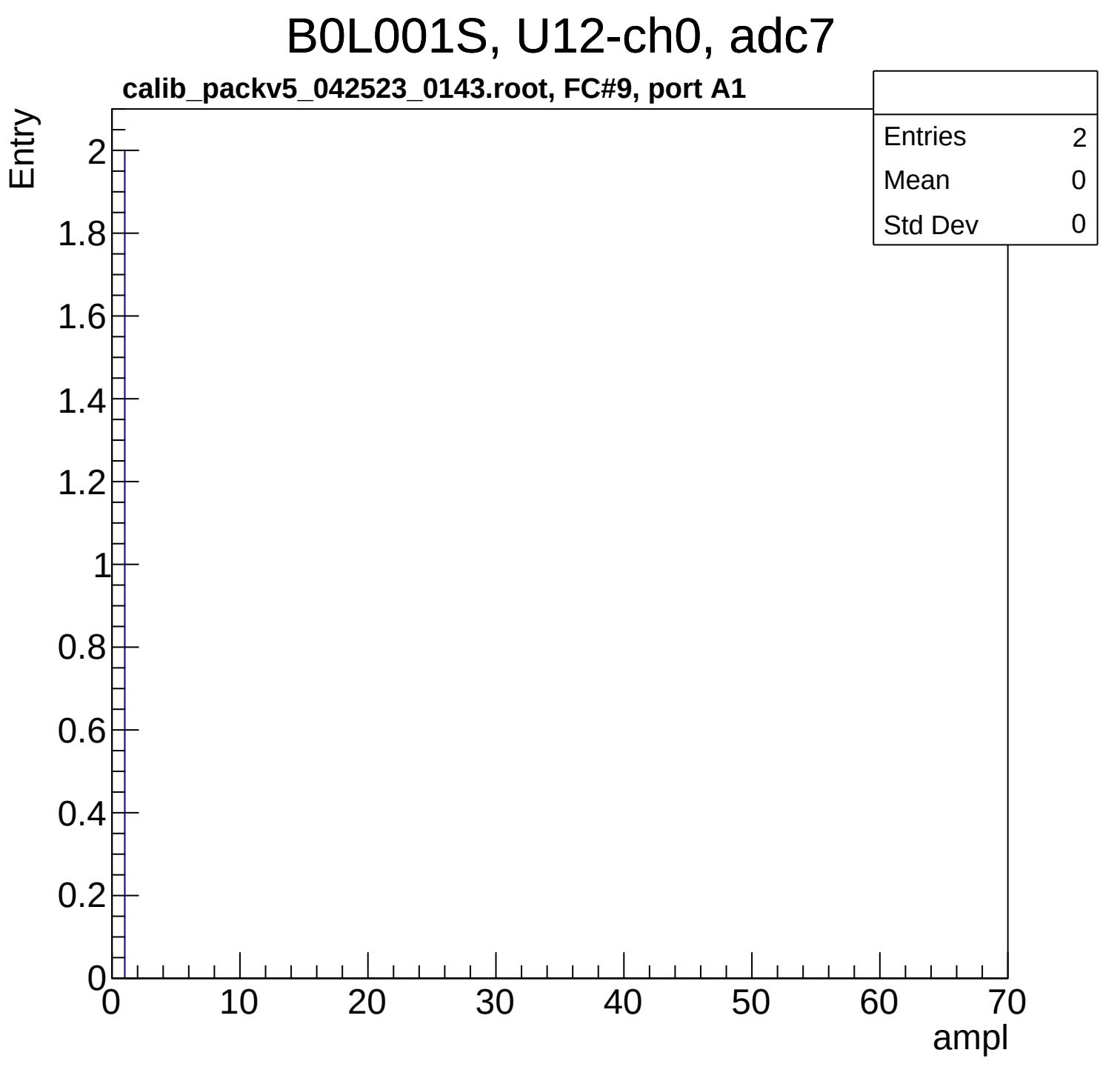
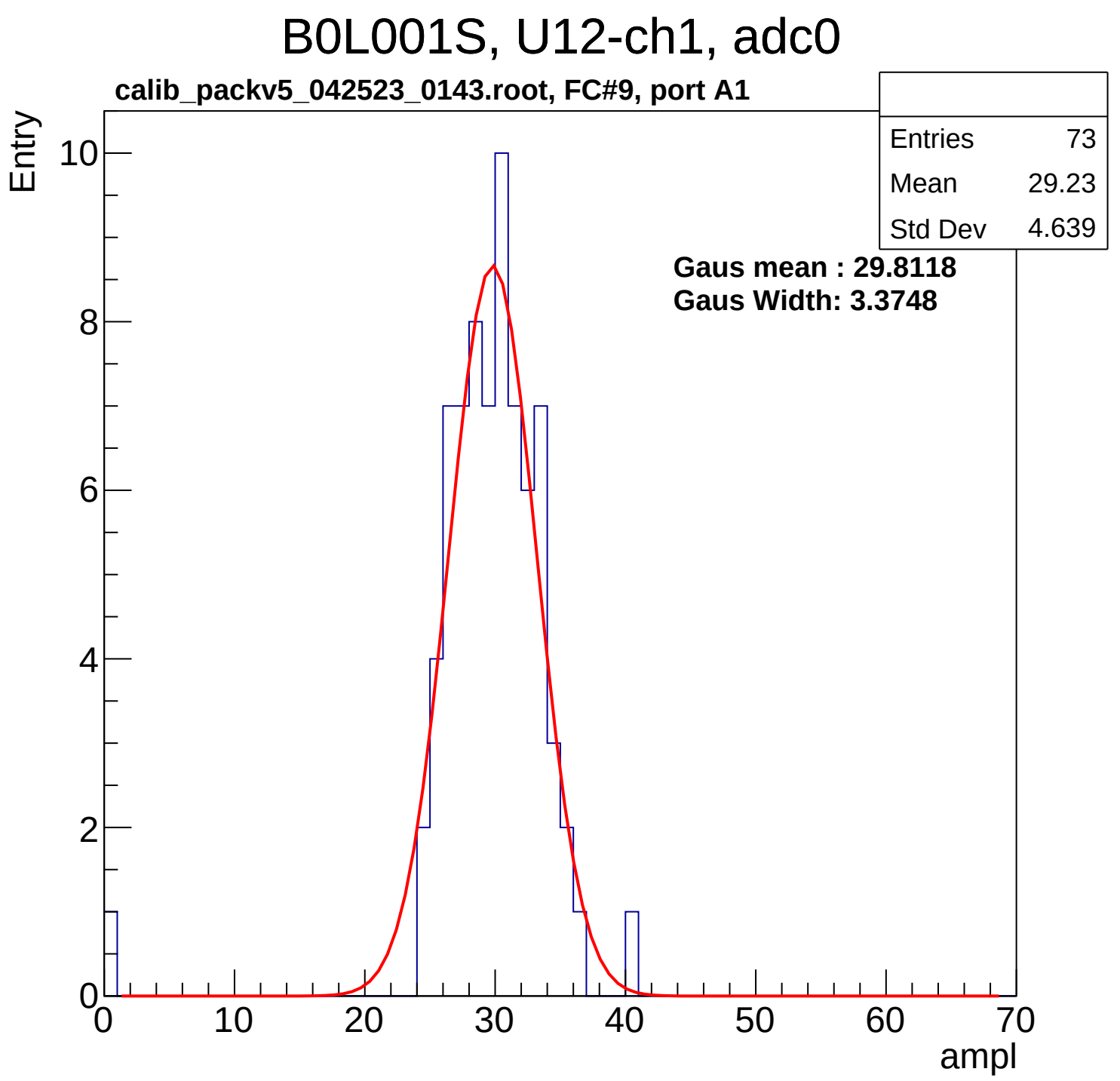
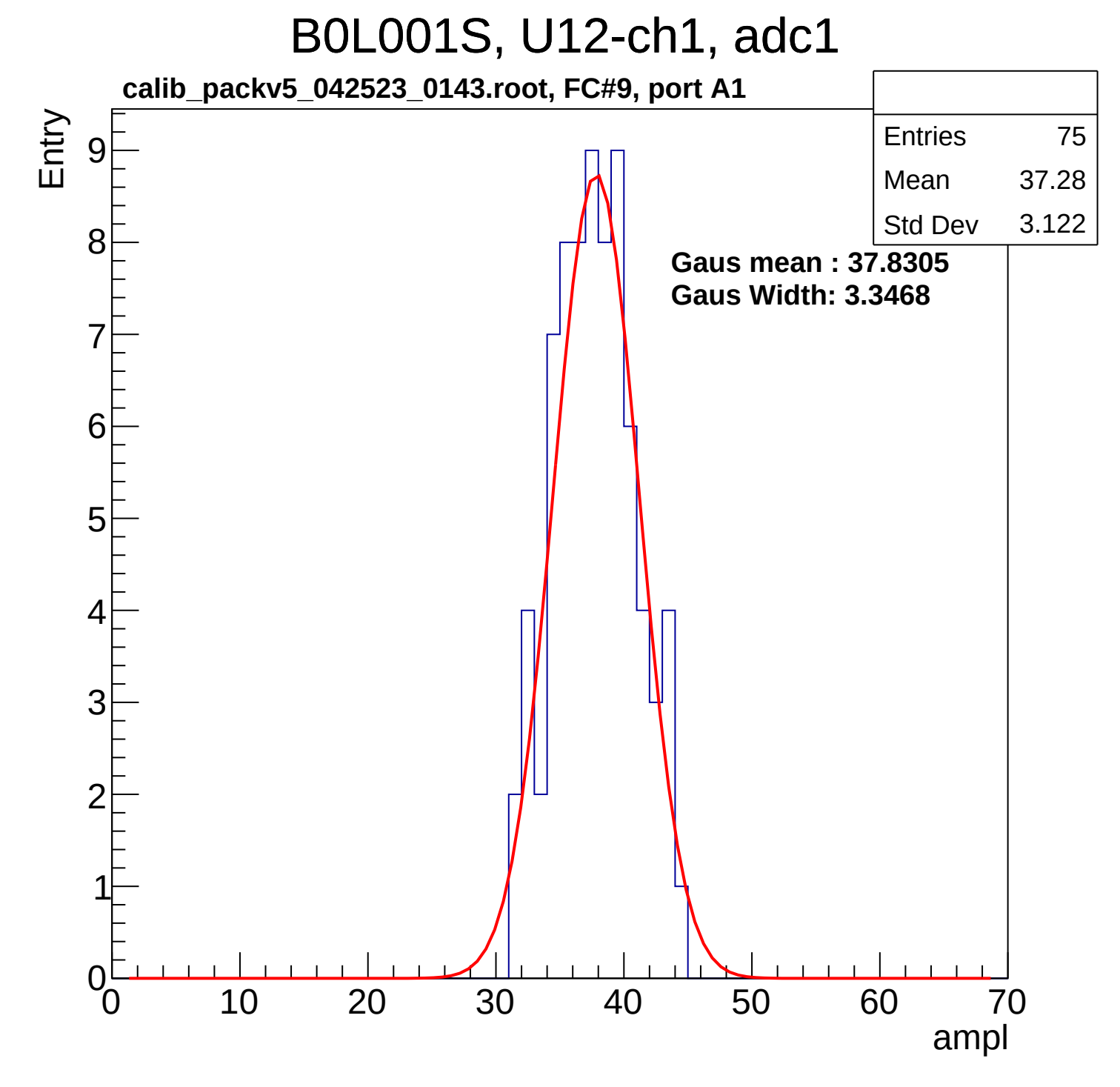

B0L001S, U12-ch0, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L001S, U12-ch0, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch1, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 73
Mean 29.23
Std Dev 4.639
Gaus mean : 29.8118
Gaus Width: 3.3748
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch1, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 75
Mean 37.28
Std Dev 3.122
Gaus mean : 37.8305
Gaus Width: 3.3468
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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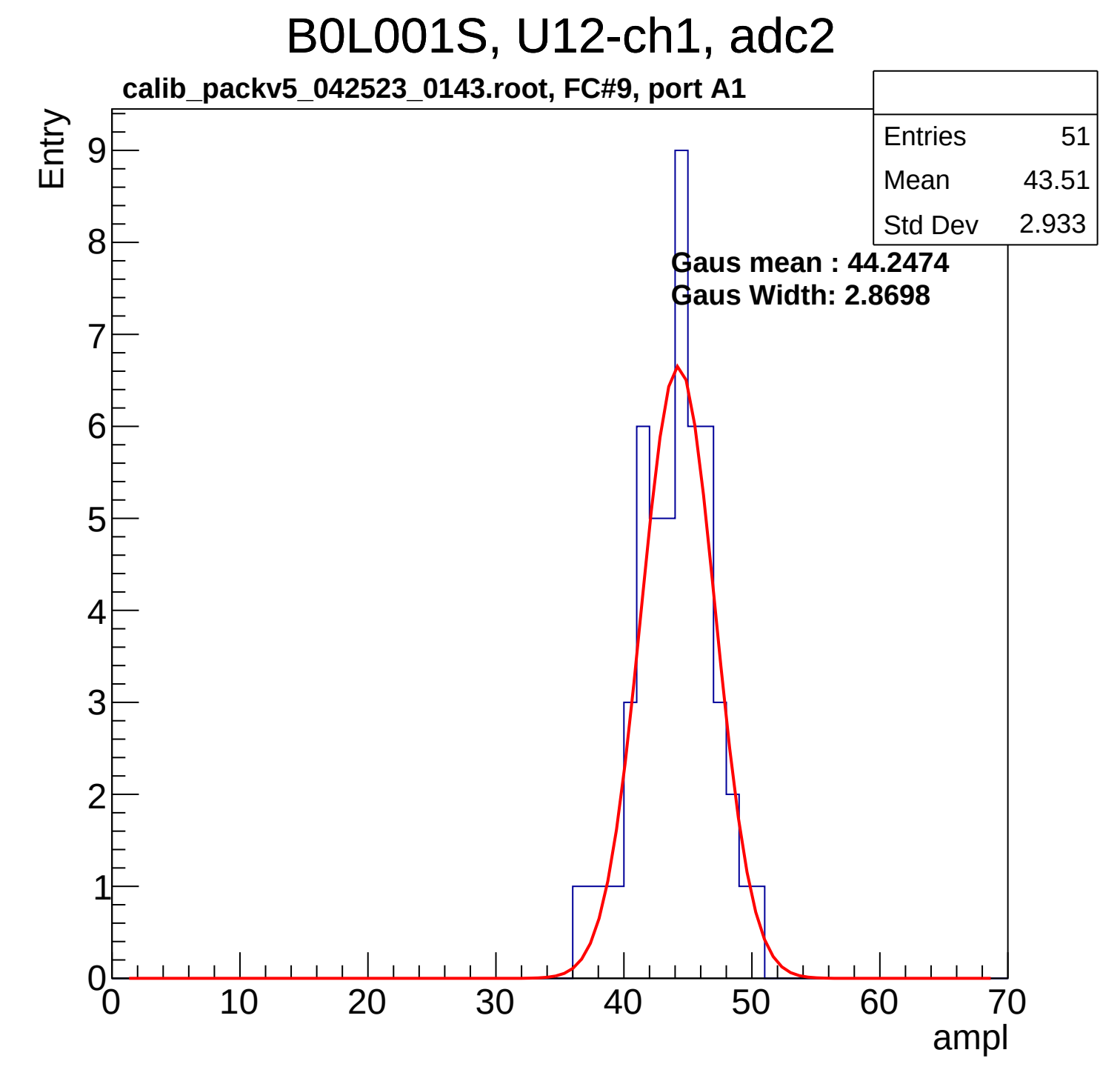
B0L001S, U12-ch1, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 51
Mean 43.51
Std Dev 2.933
Gaus mean : 44.2474
Gaus Width: 2.8698
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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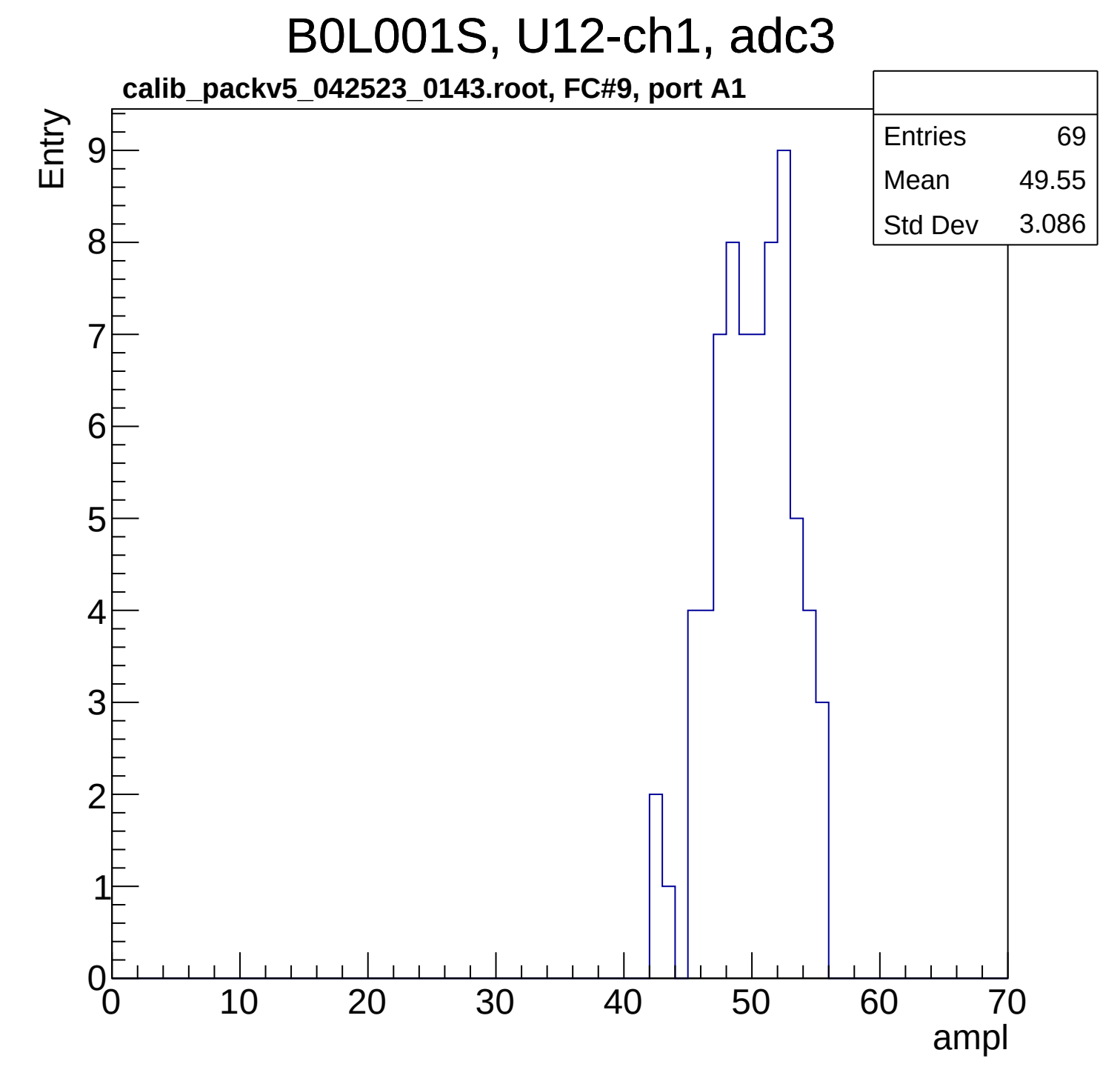
B0L001S, U12-ch1, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 69
Mean 49.55
Std Dev 3.086
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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40
50
60
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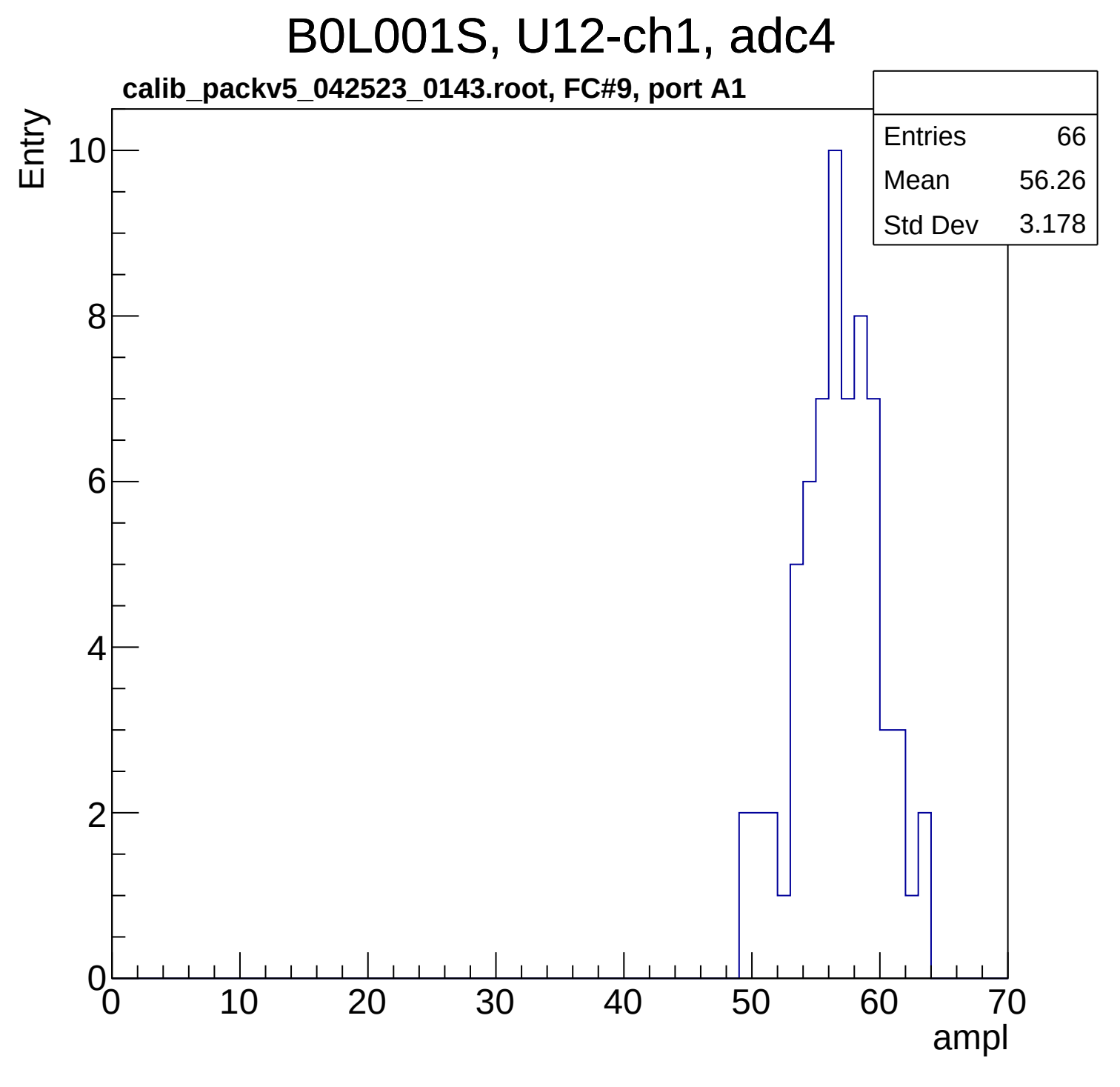
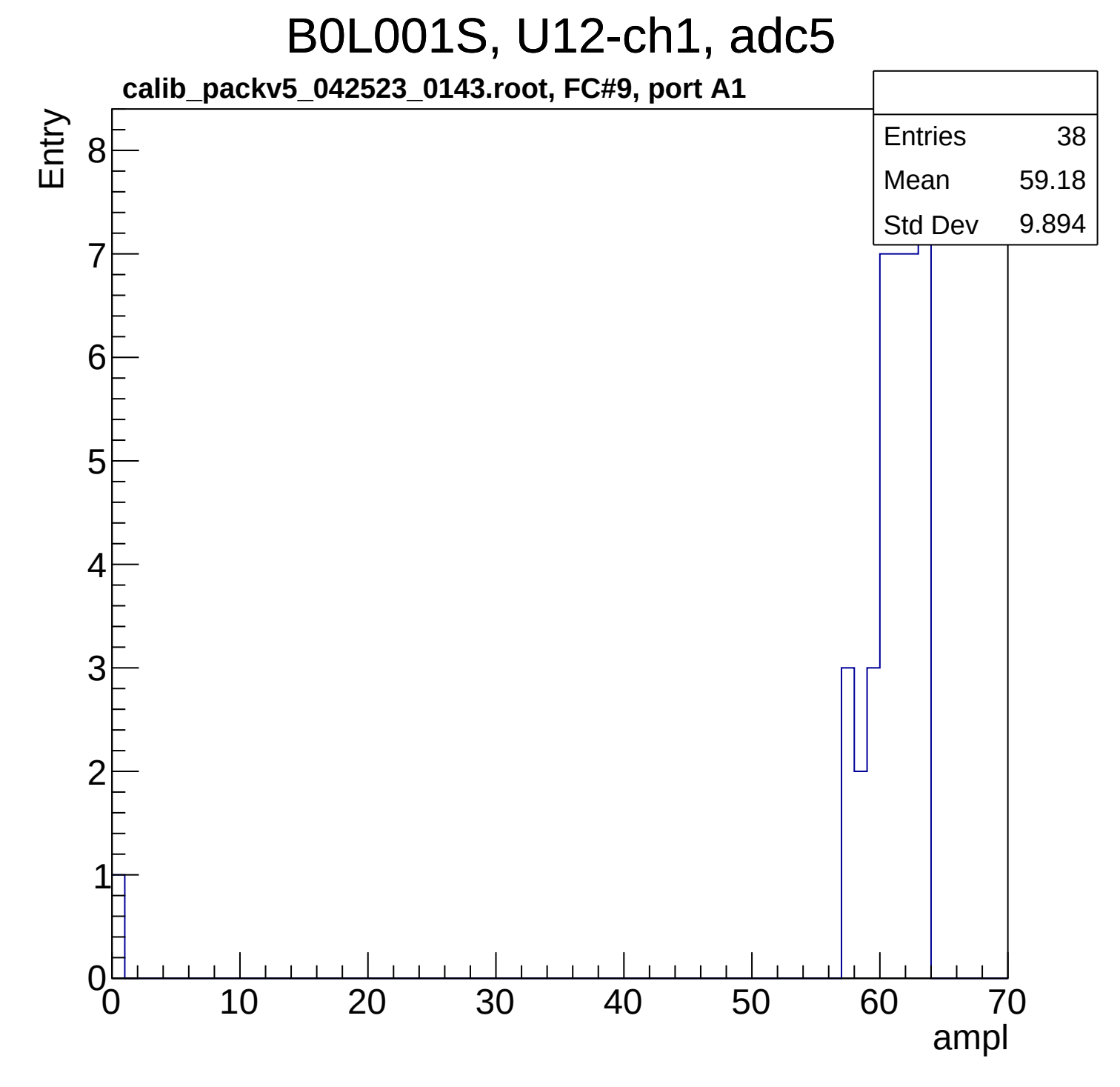

B0L001S, U12-ch1, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 66
Mean 56.26
Std Dev 3.178
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch1, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 38
Mean 59.18
Std Dev 9.894
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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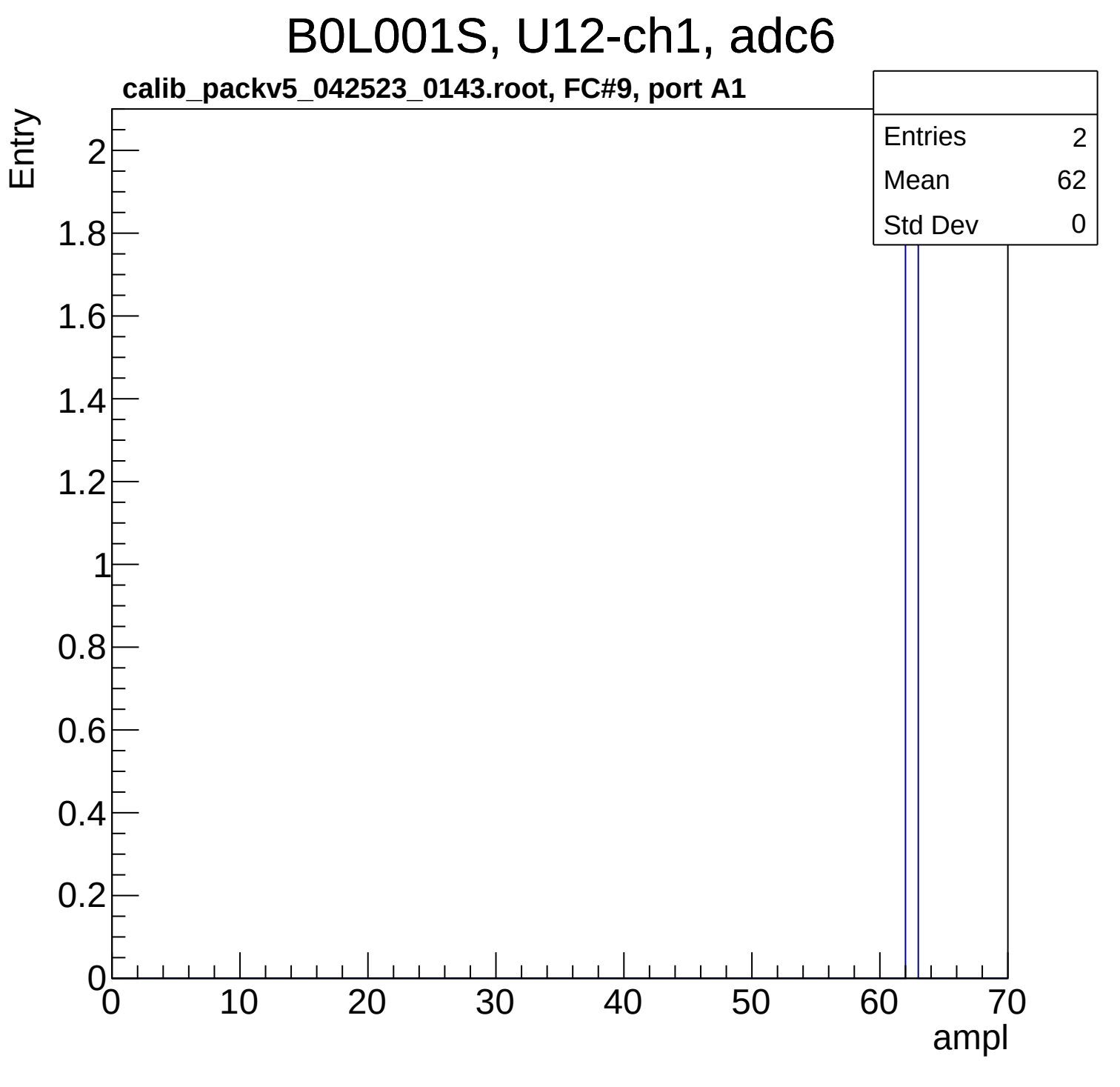
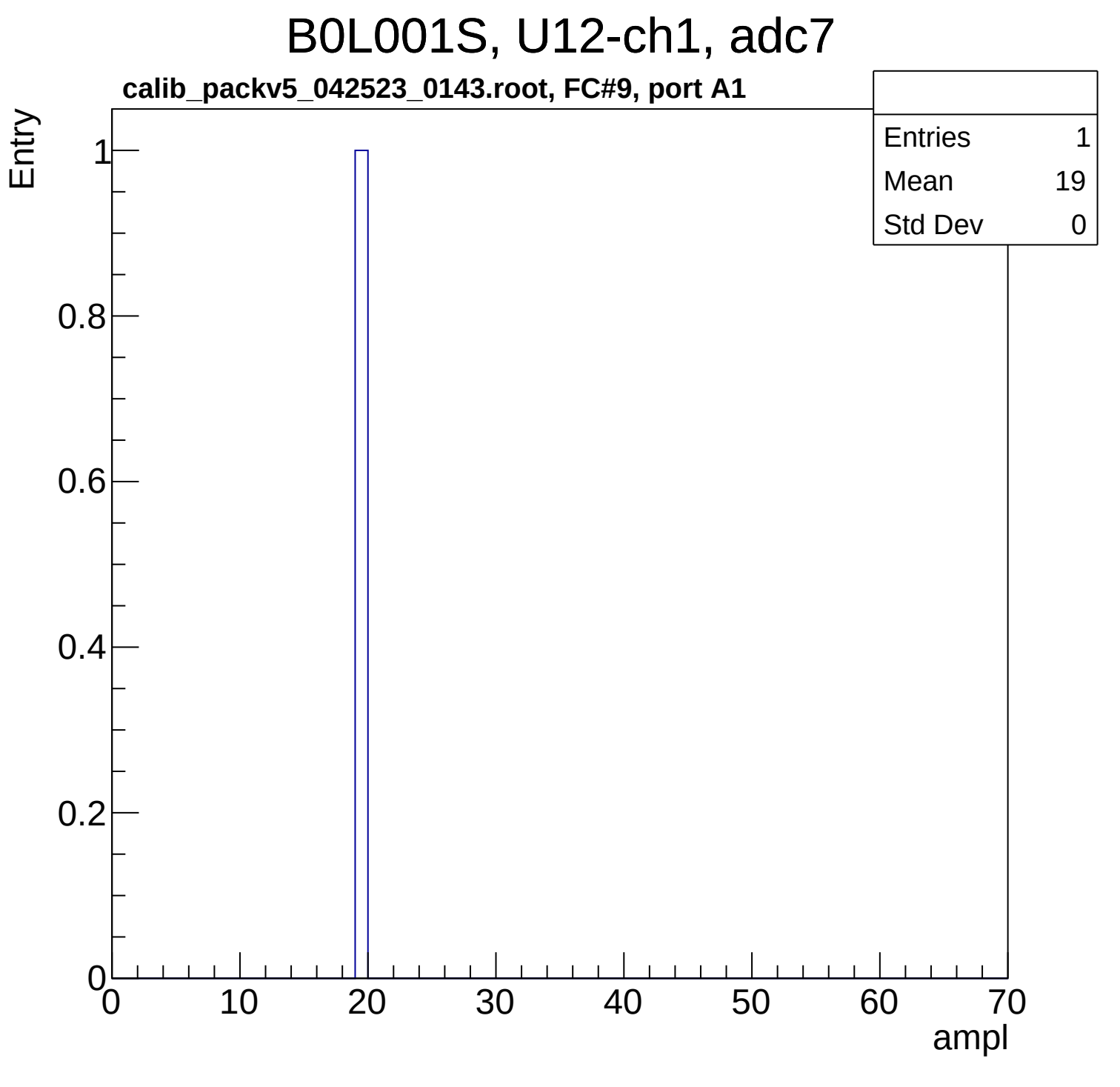

B0L001S, U12-ch1, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 62
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L001S, U12-ch1, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 19
Std Dev 0
Entry
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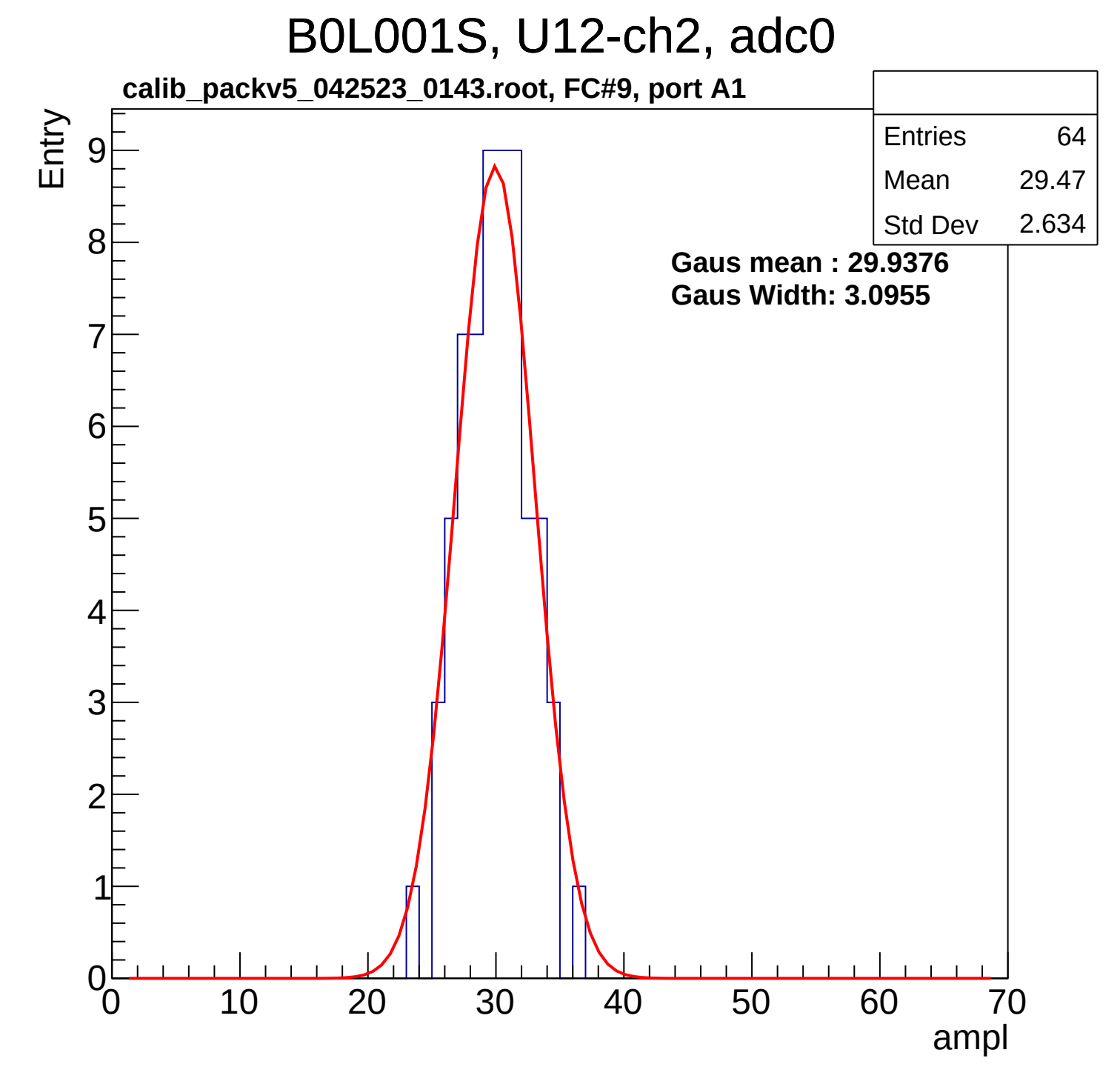
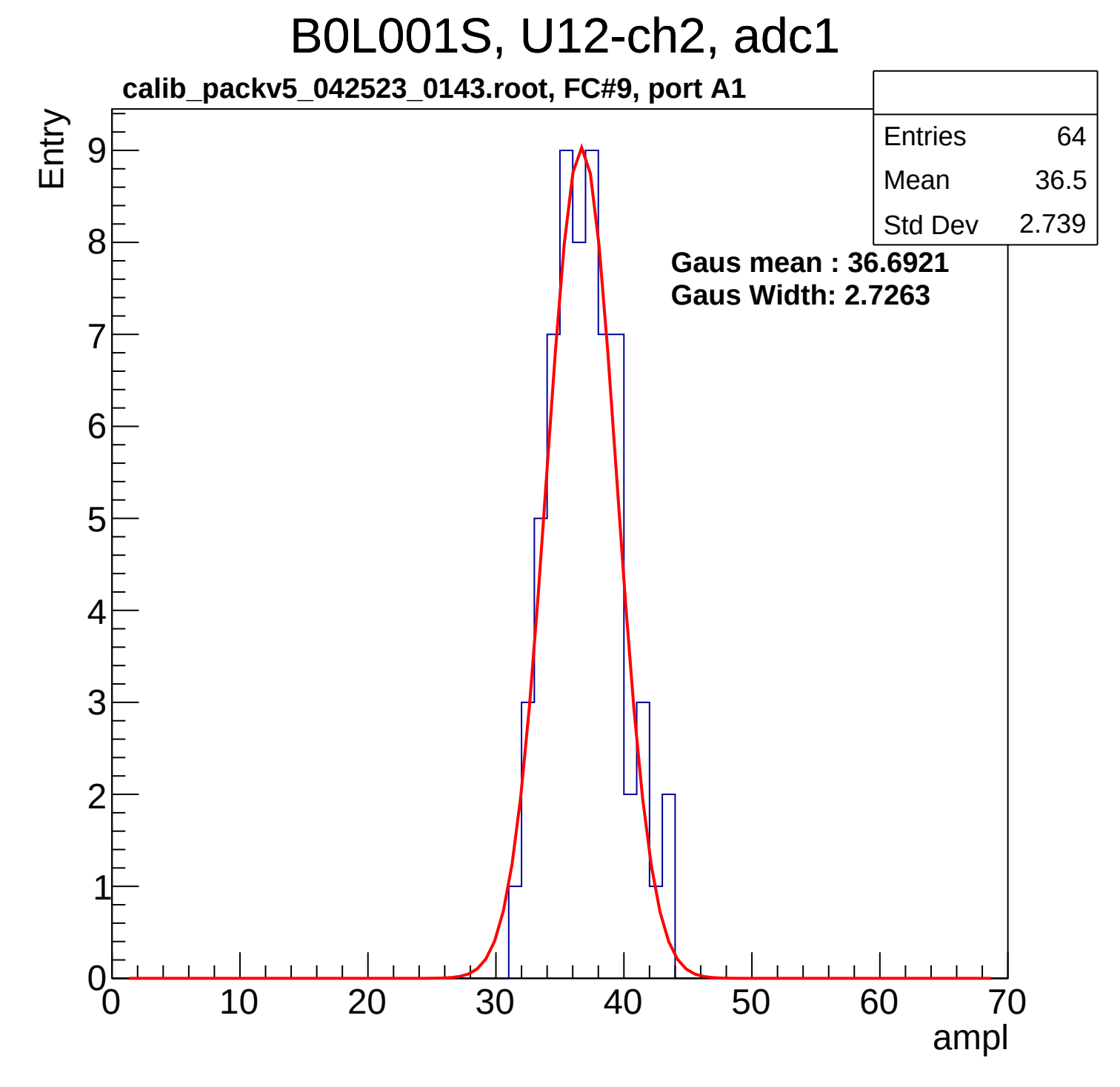
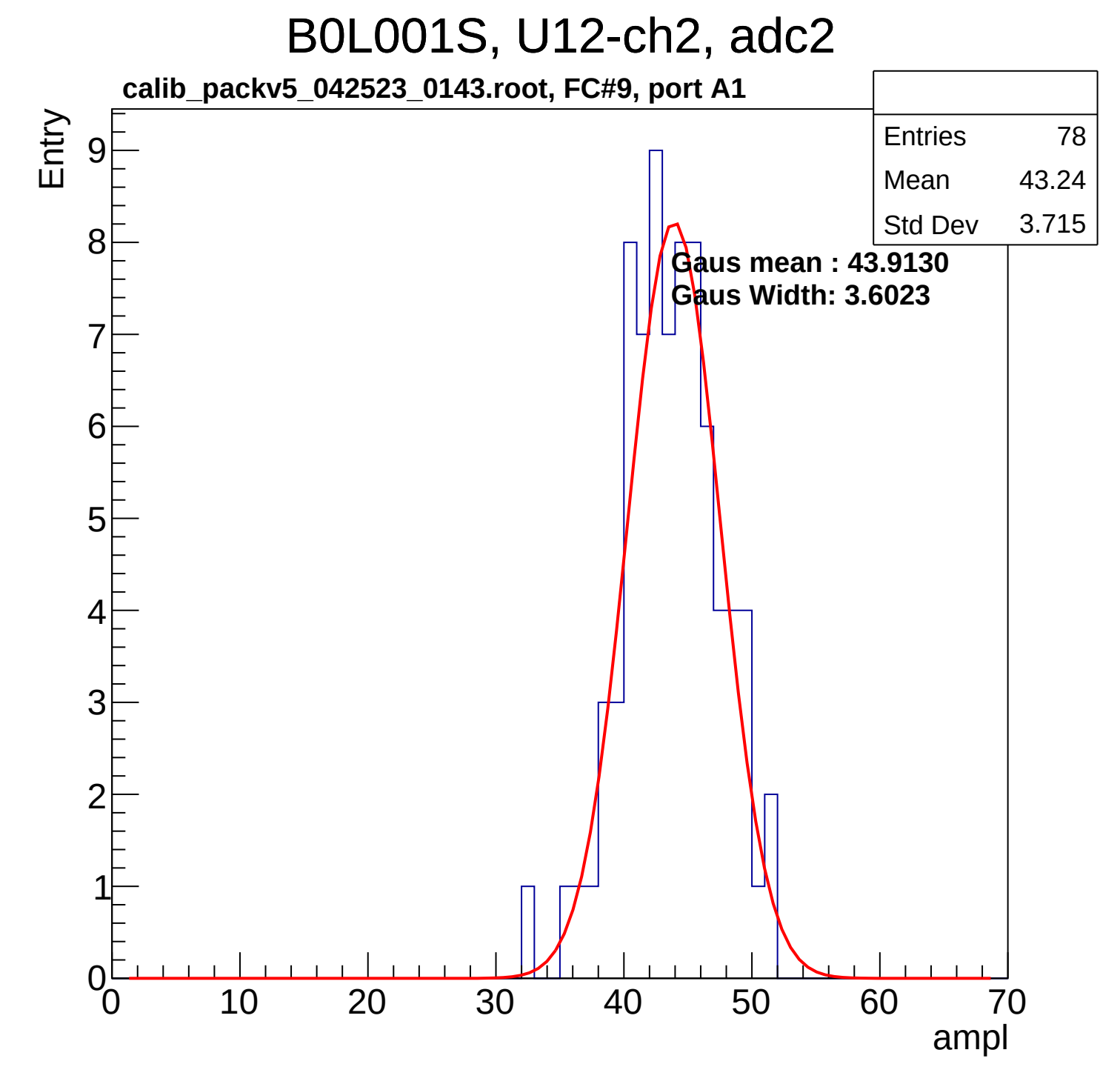
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch2, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 64
Mean 29.47
Std Dev 2.634
Gaus mean : 29.9376
Gaus Width: 3.0955
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch2, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 64
Mean 36.5
Std Dev 2.739
Gaus mean : 36.6921
Gaus Width: 2.7263
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch2, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 78
Mean 43.24
Std Dev 3.715
Gaus mean : 43.9130
Gaus Width: 3.6023
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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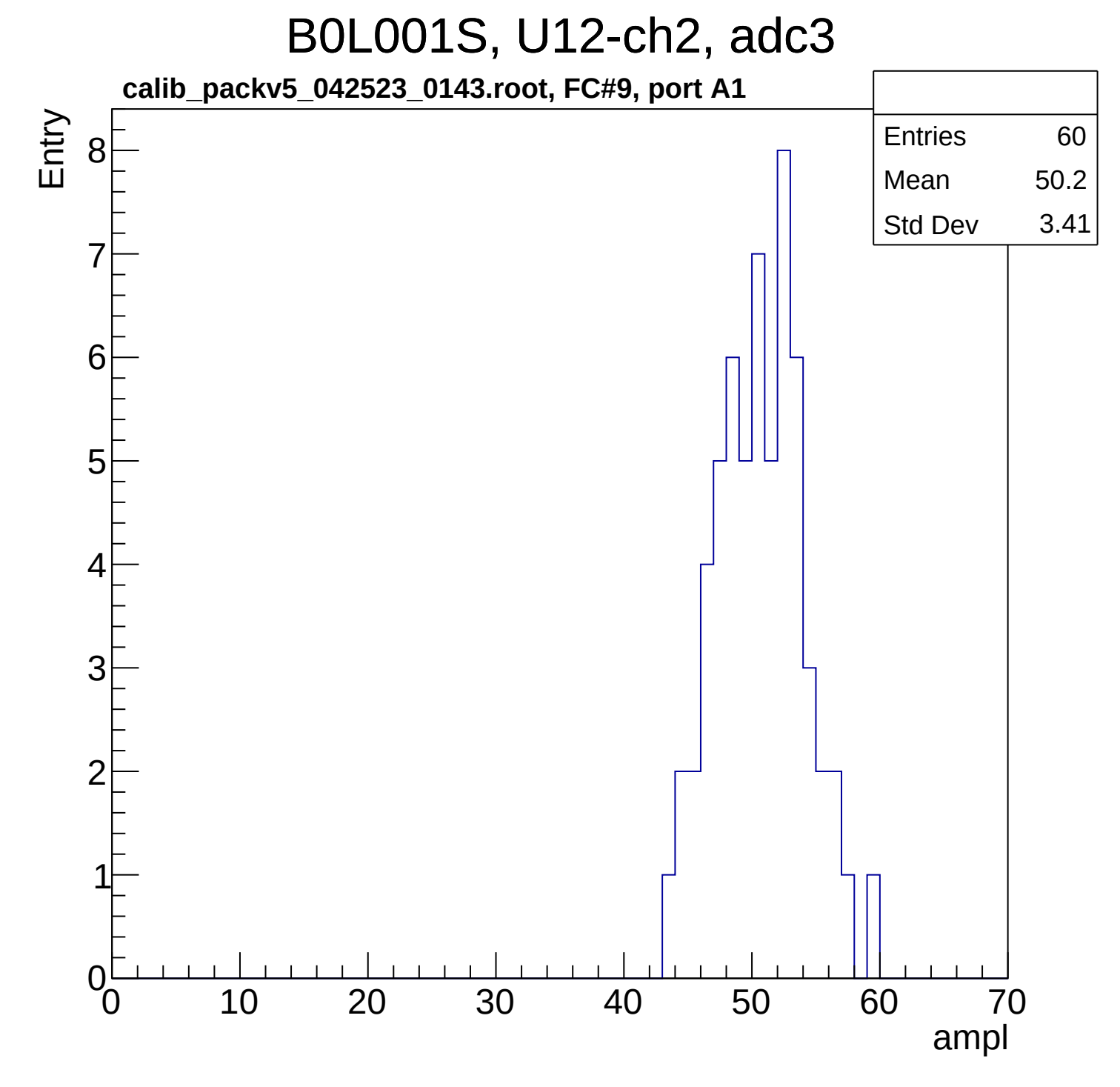
B0L001S, U12-ch2, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 60
Mean 50.2
Std Dev 3.41
Entry
ampl
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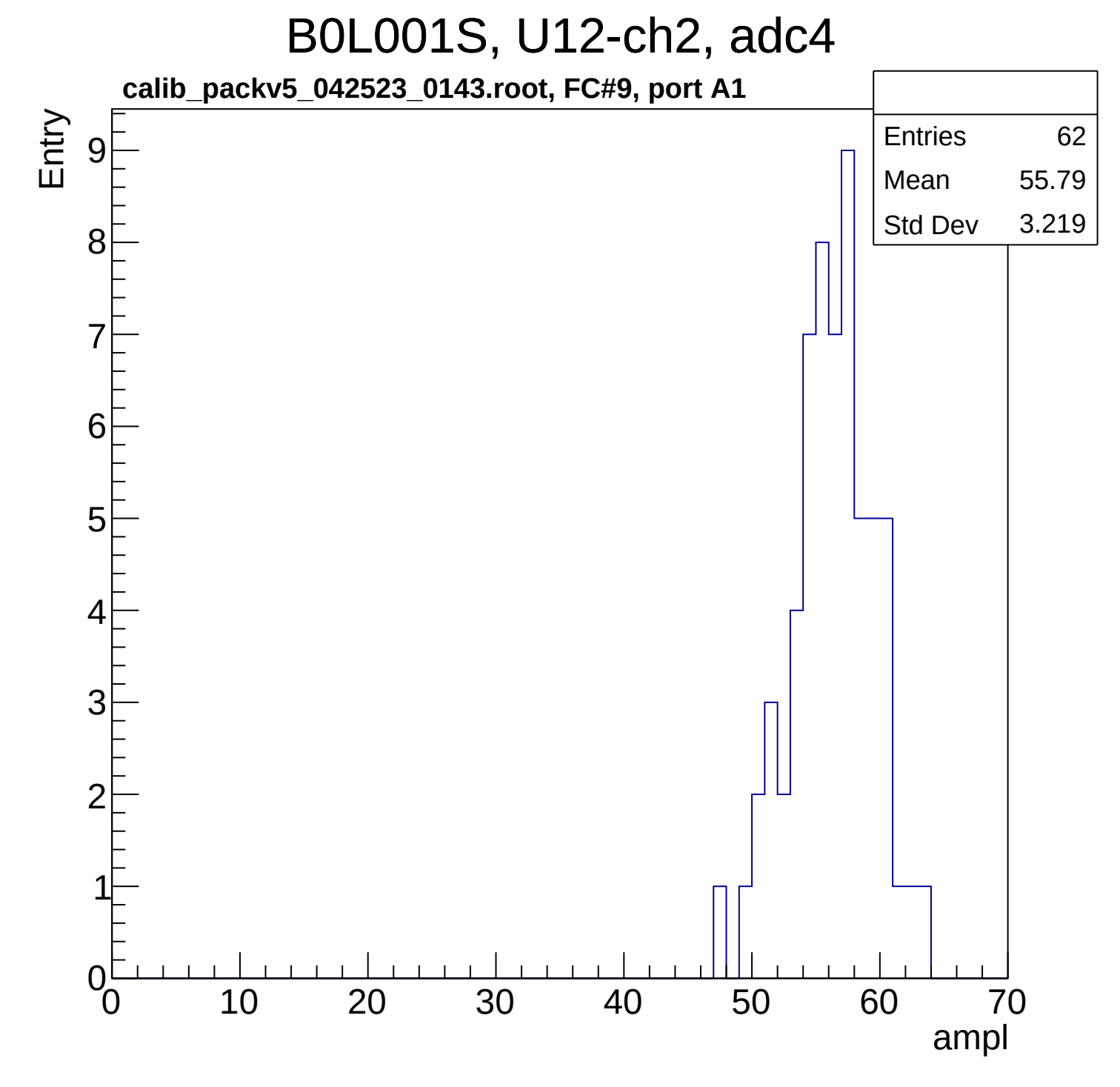
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch2, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 62
Mean 55.79
Std Dev 3.219
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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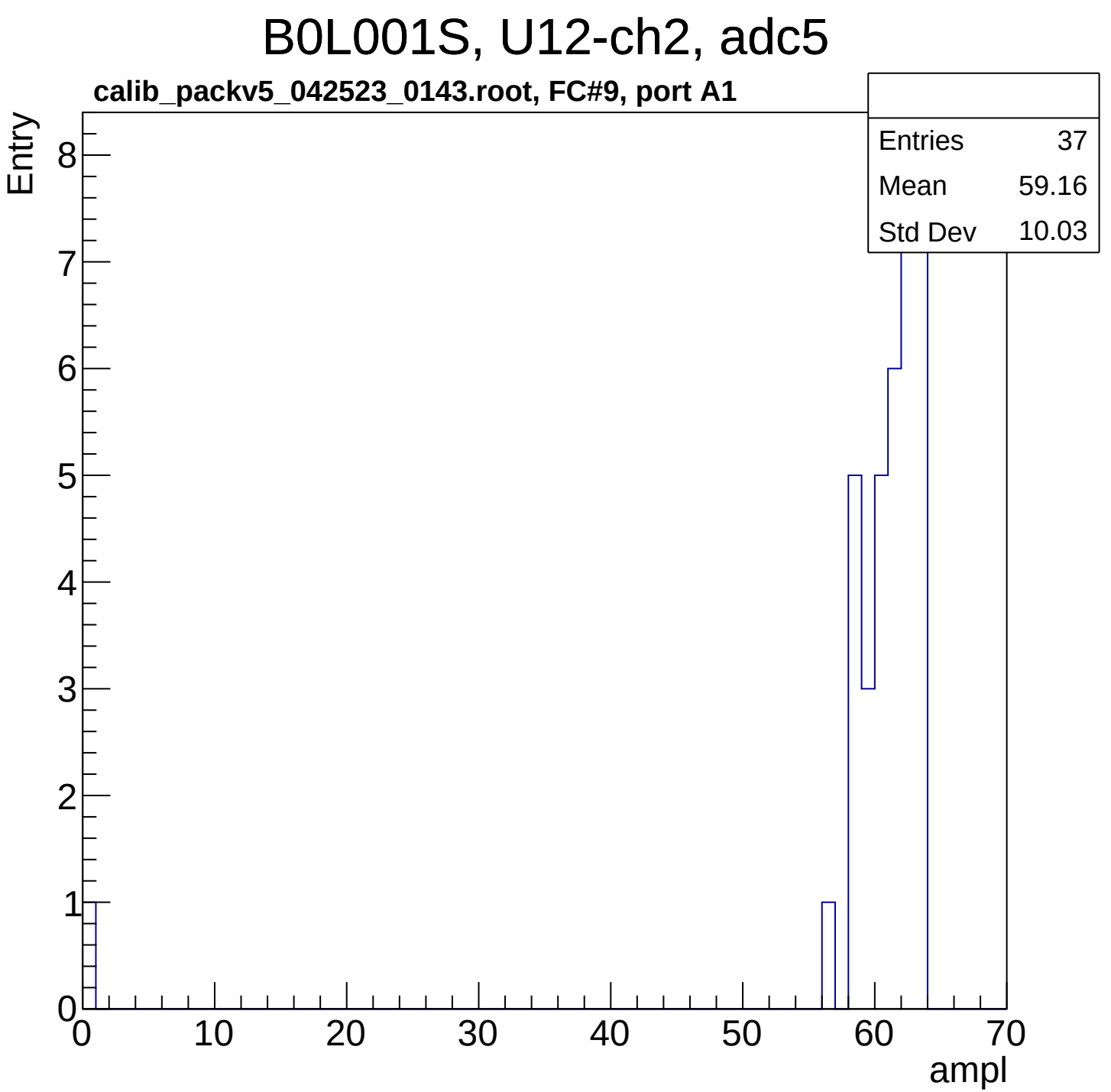
B0L001S, U12-ch2, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 37
Mean 59.16
Std Dev 10.03
Entry
ampl
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1
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3
4
5
6
7
8
0
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20
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40
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60
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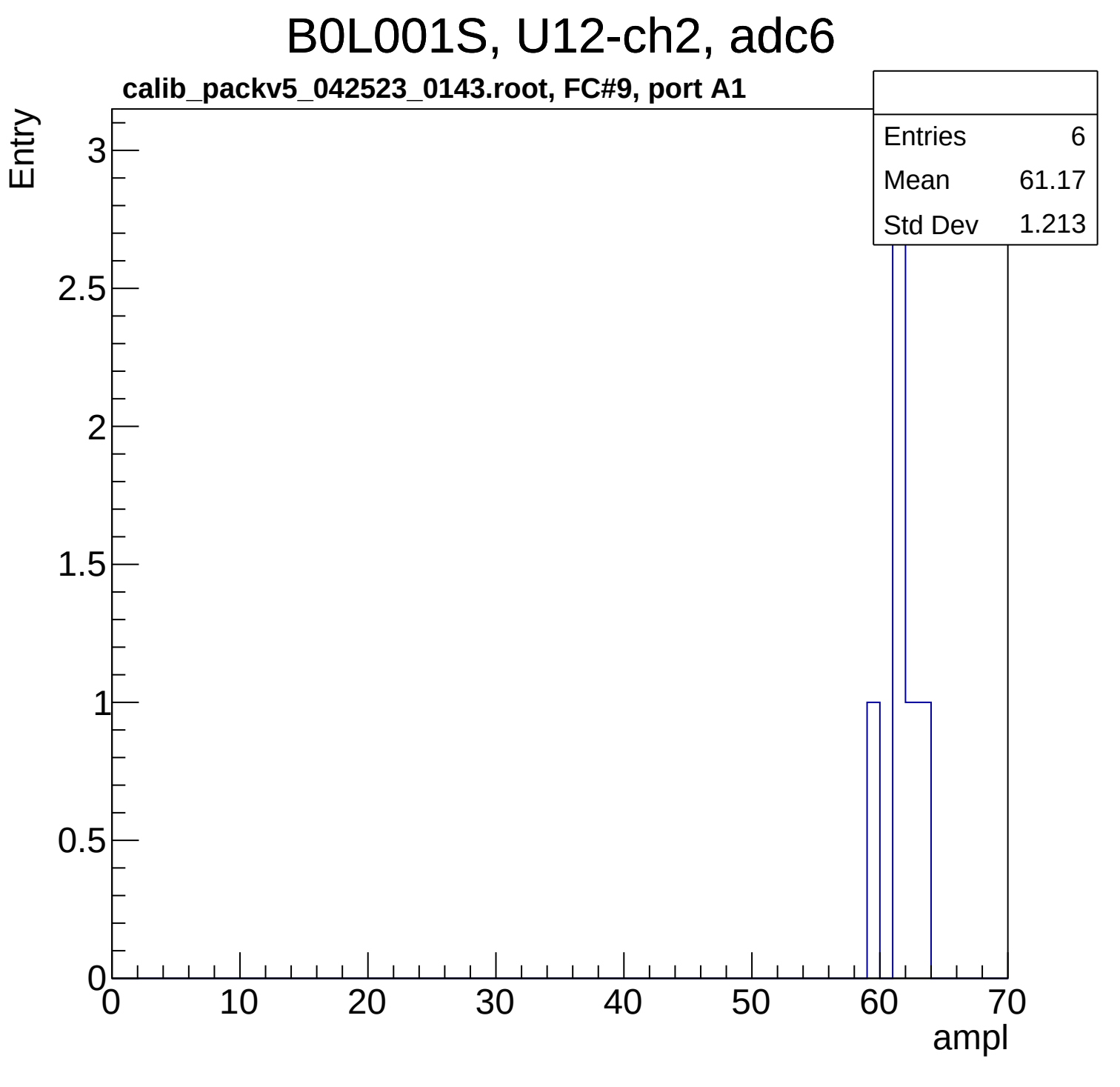
B0L001S, U12-ch2, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 6
Mean 61.17
Std Dev 1.213
Entry
ampl
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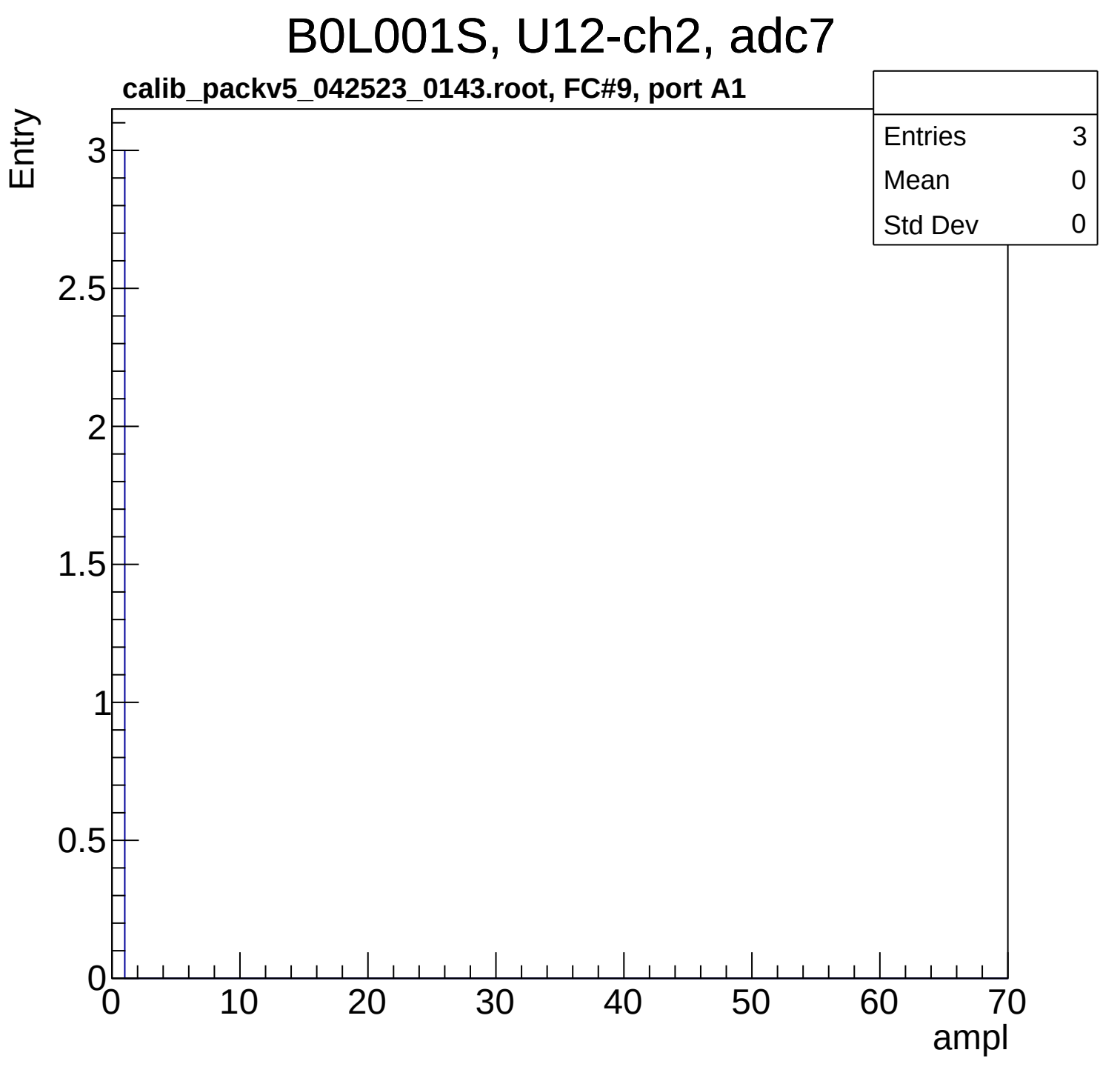
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B0L001S, U12-ch2, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 3
Mean 0
Std Dev 0
Entry
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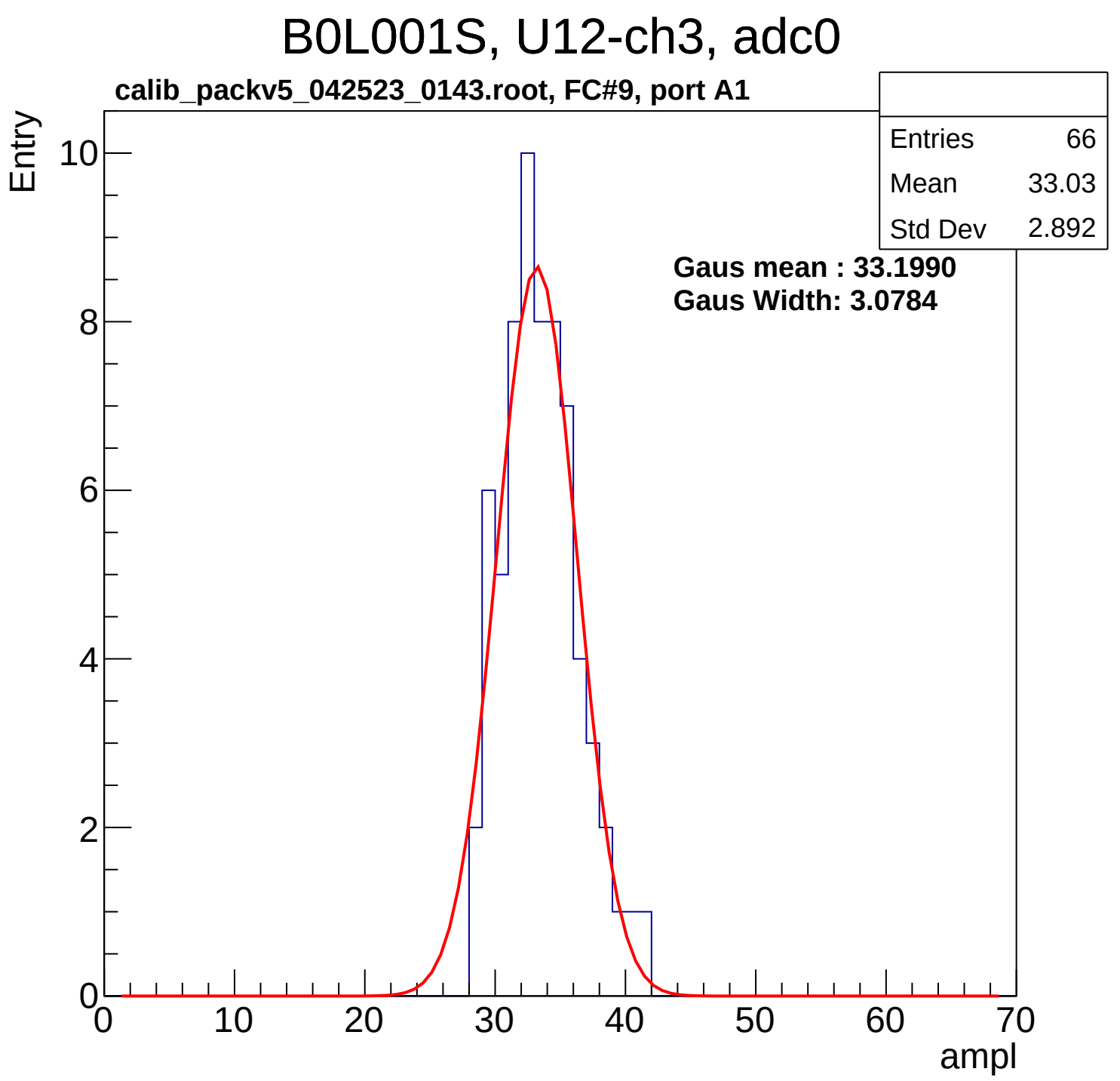
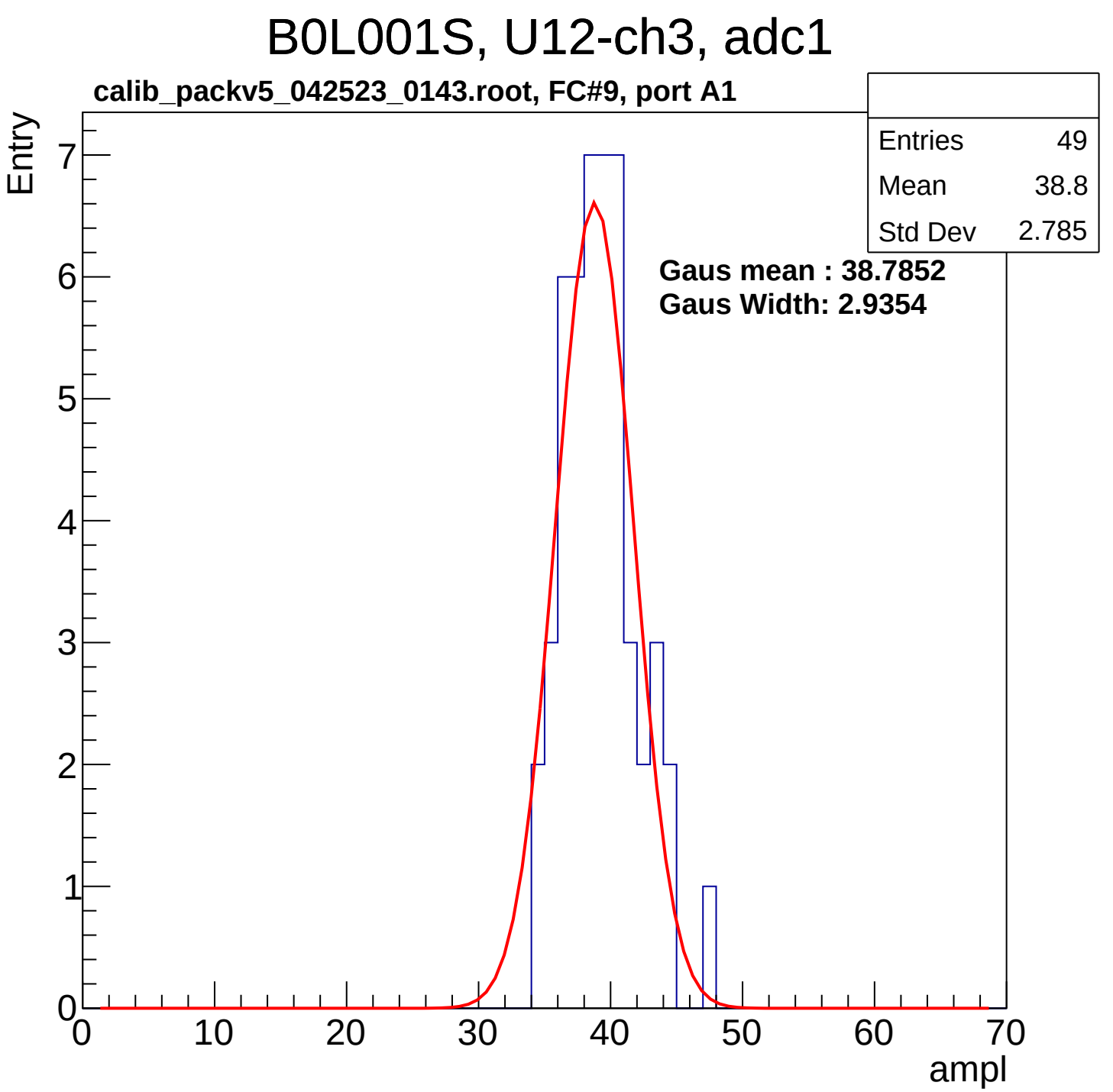
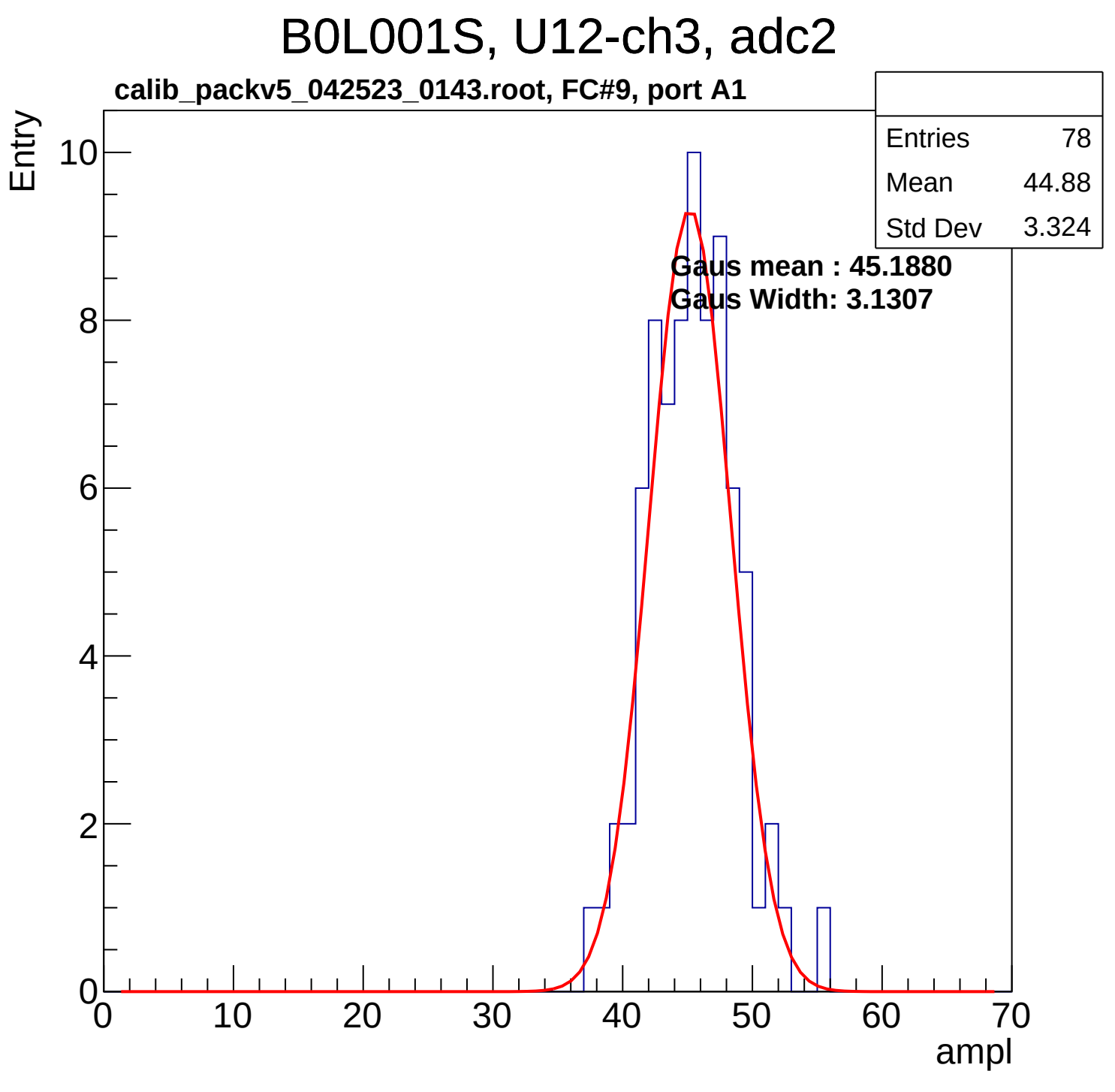
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch3, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 66
Mean 33.03
Std Dev 2.892
Gaus mean : 33.1990
Gaus Width: 3.0784
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch3, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 49
Mean 38.8
Std Dev 2.785
Gaus mean : 38.7852
Gaus Width: 2.9354
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B0L001S, U12-ch3, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 78
Mean 44.88
Std Dev 3.324
Gaus mean : 45.1880
Gaus Width: 3.1307
Entry
ampl
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6
8
10
0
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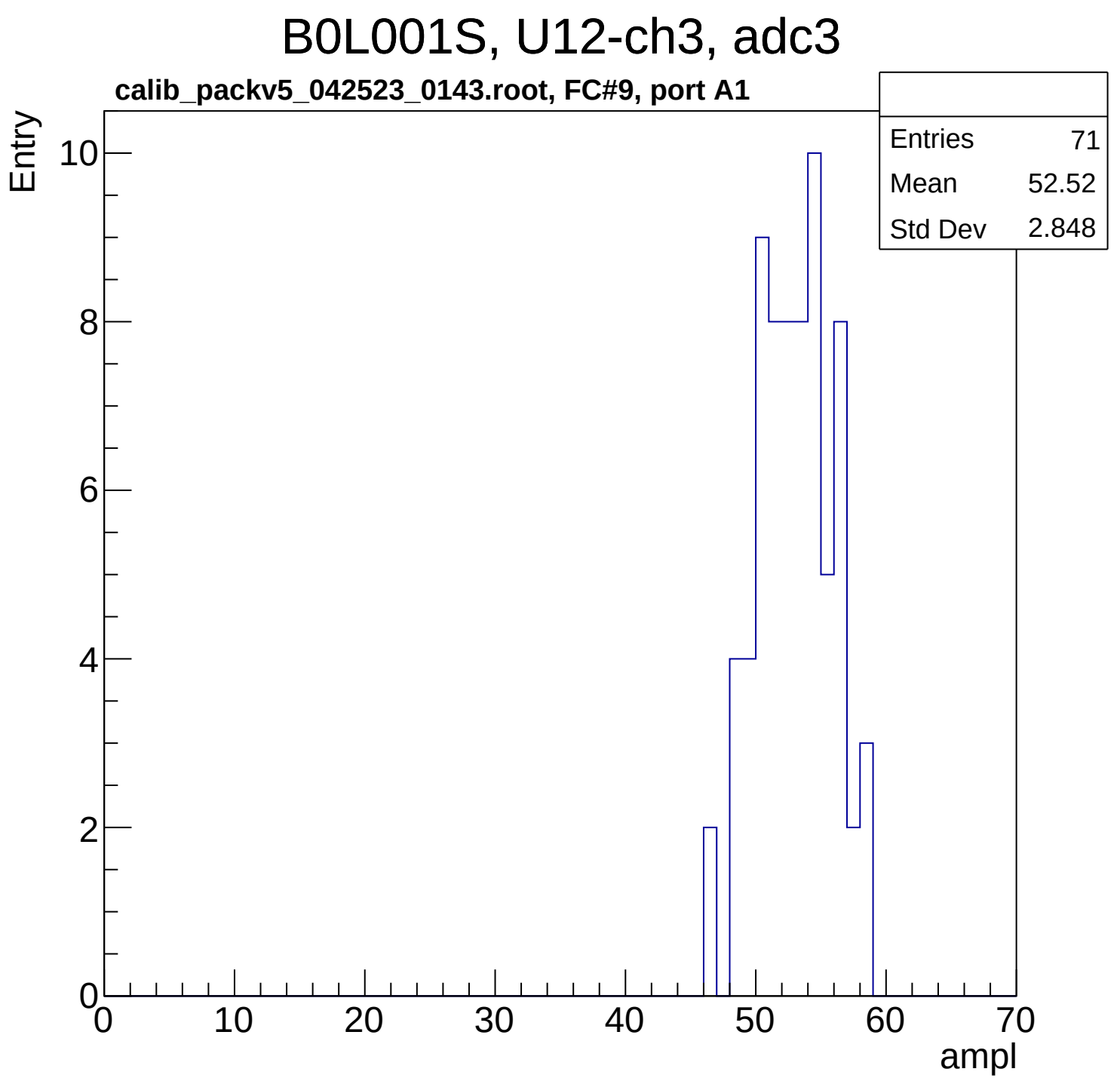
20
30
40
50
60
70


B0L001S, U12-ch3, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 71
Mean 52.52
Std Dev 2.848
Entry
ampl
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0
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60
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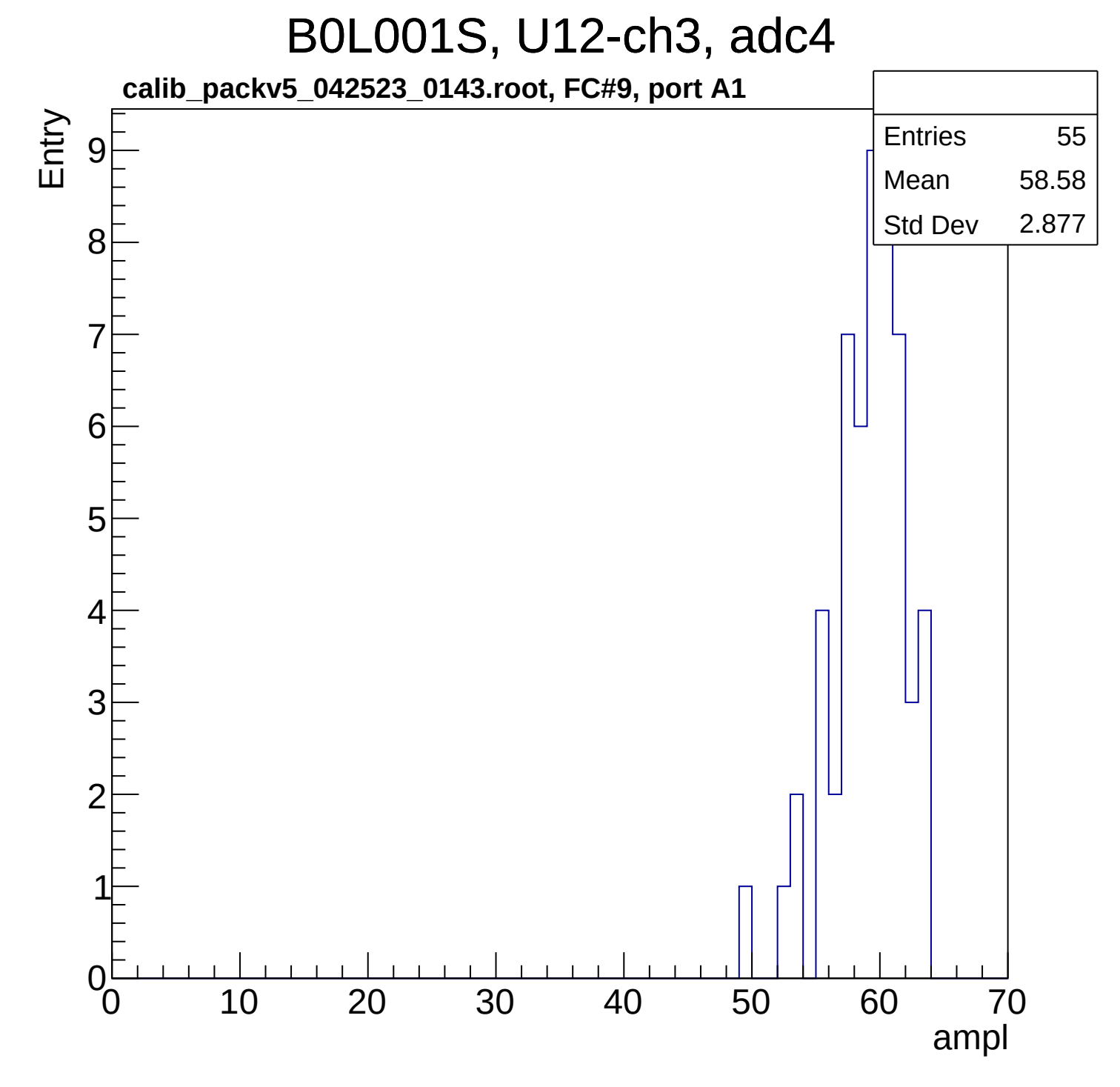
B0L001S, U12-ch3, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 55
Mean 58.58
Std Dev 2.877
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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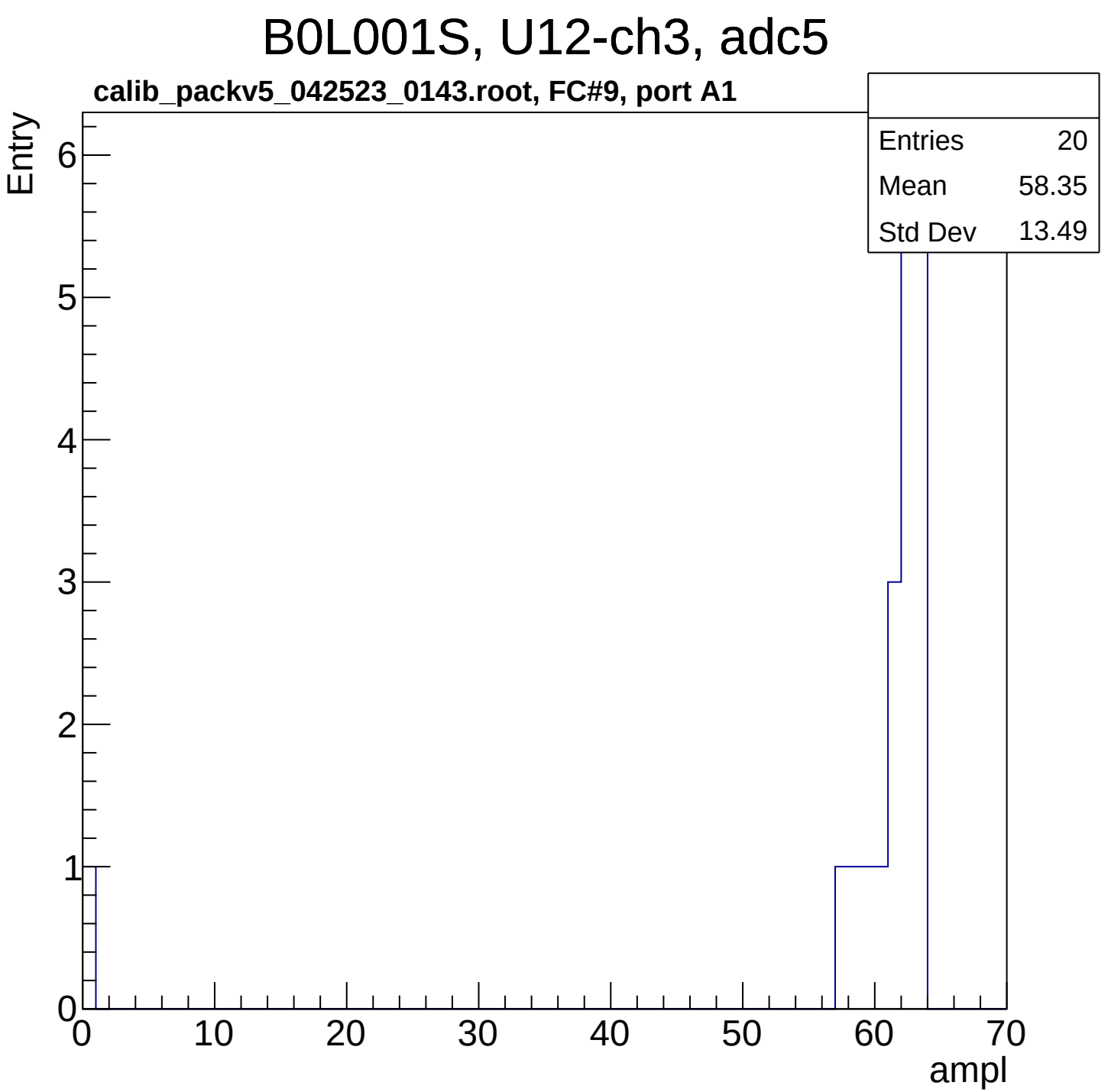
B0L001S, U12-ch3, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 20
Mean 58.35
Std Dev 13.49
Entry
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2
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4
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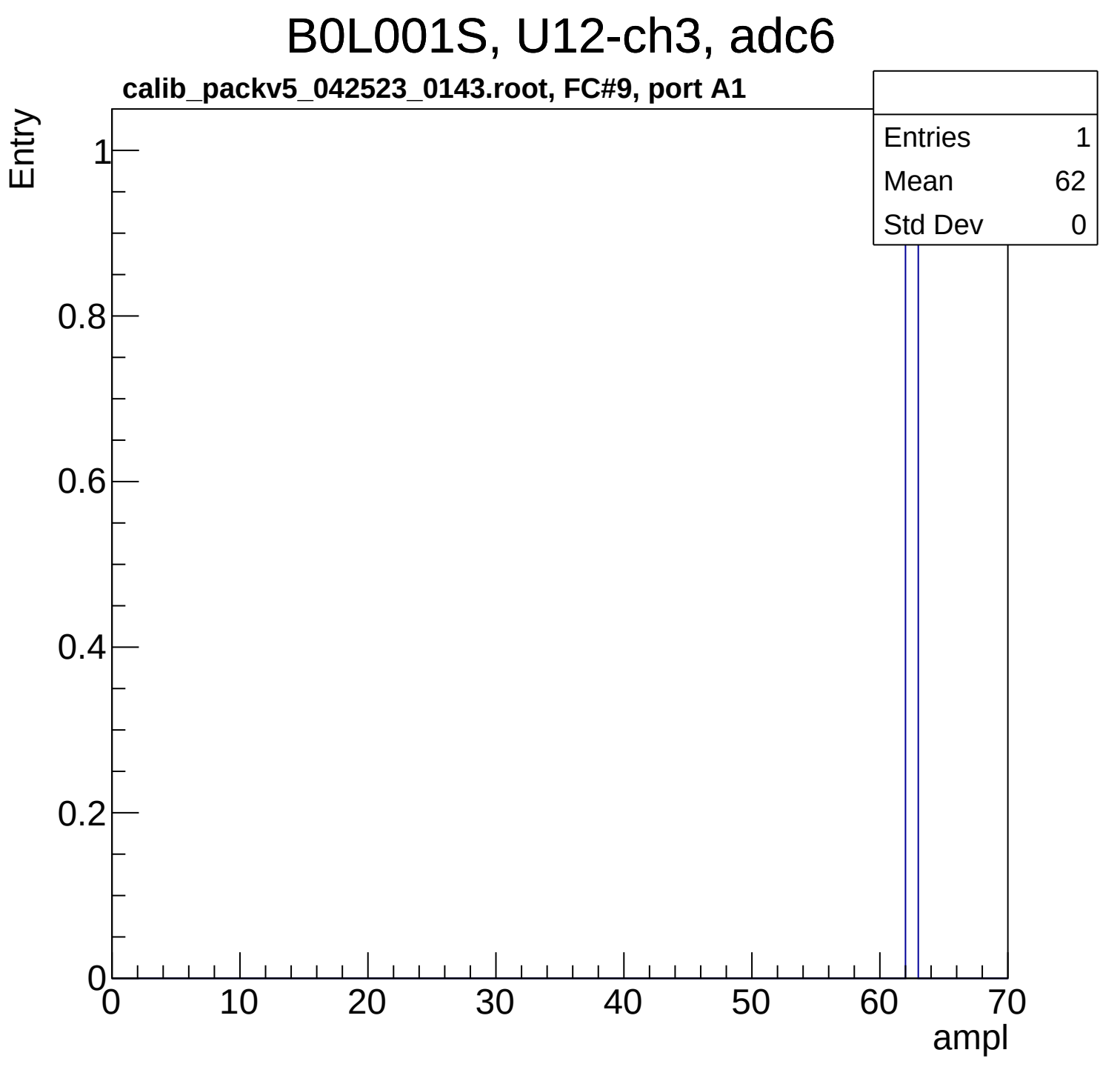
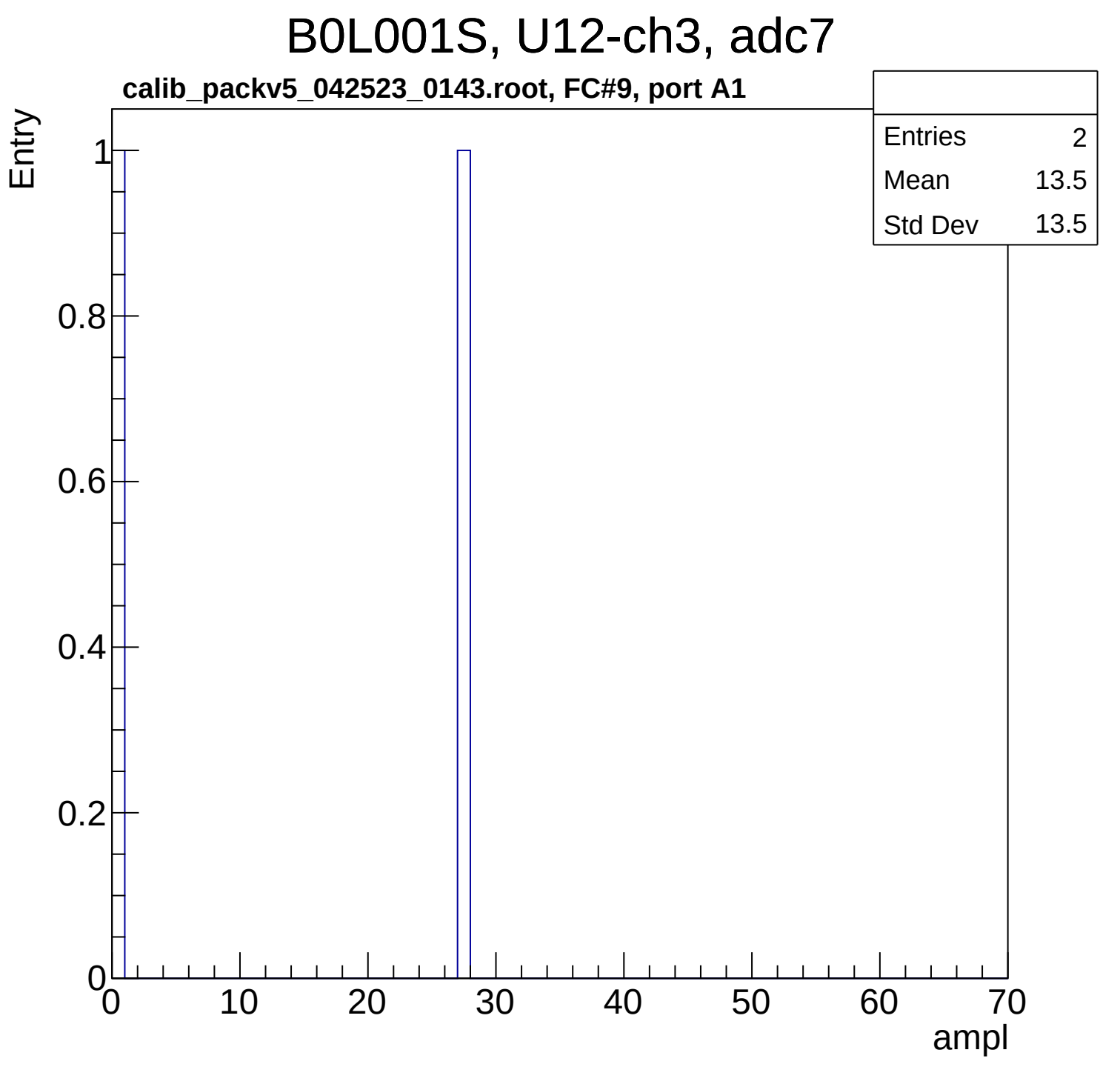
6
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch3, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch3, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 13.5
Std Dev 13.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
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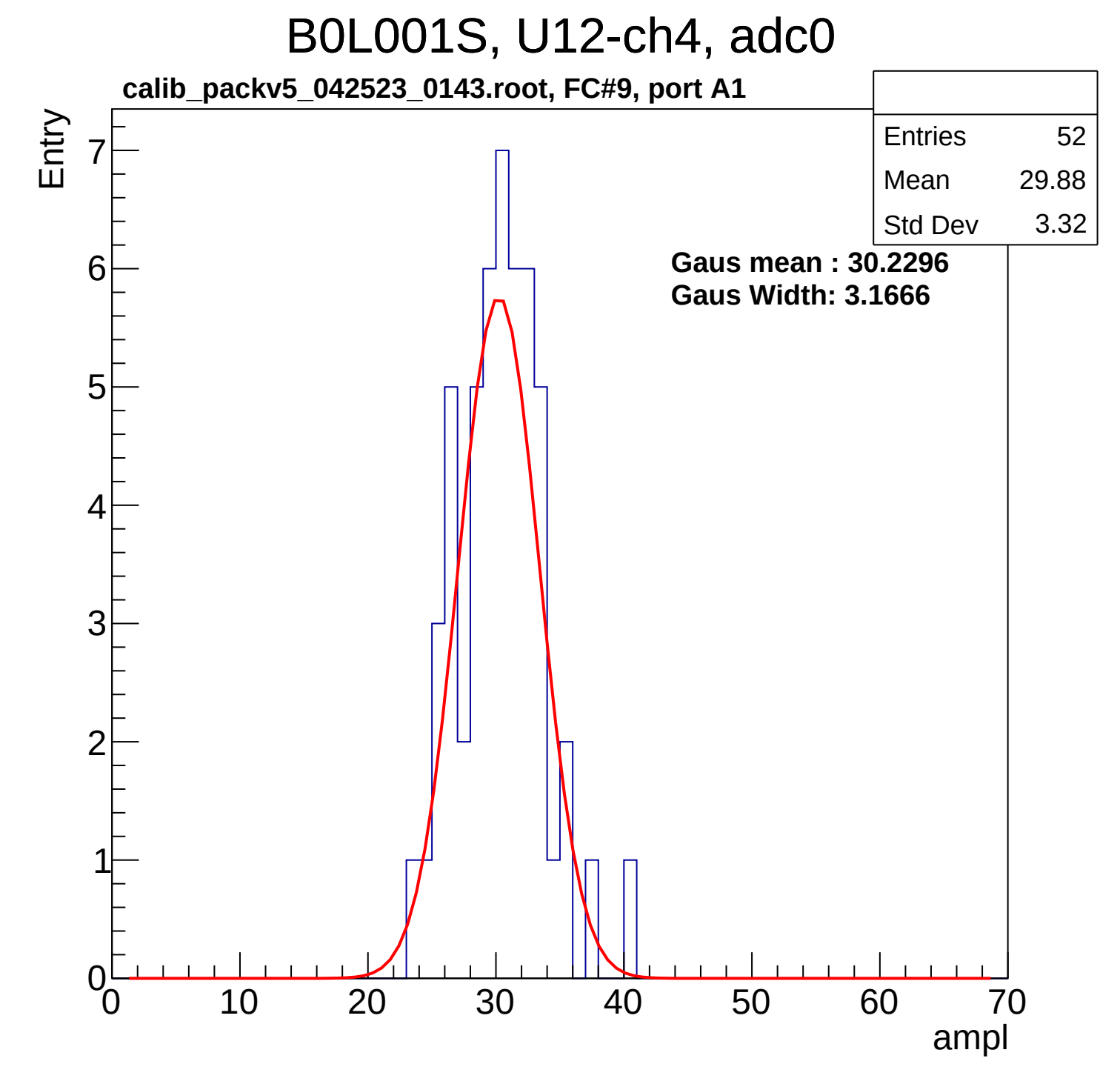
50
60
70
ampl


B0L001S, U12-ch4, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 52
Mean 29.88
Std Dev 3.32
Gaus mean : 30.2296
Gaus Width: 3.1666
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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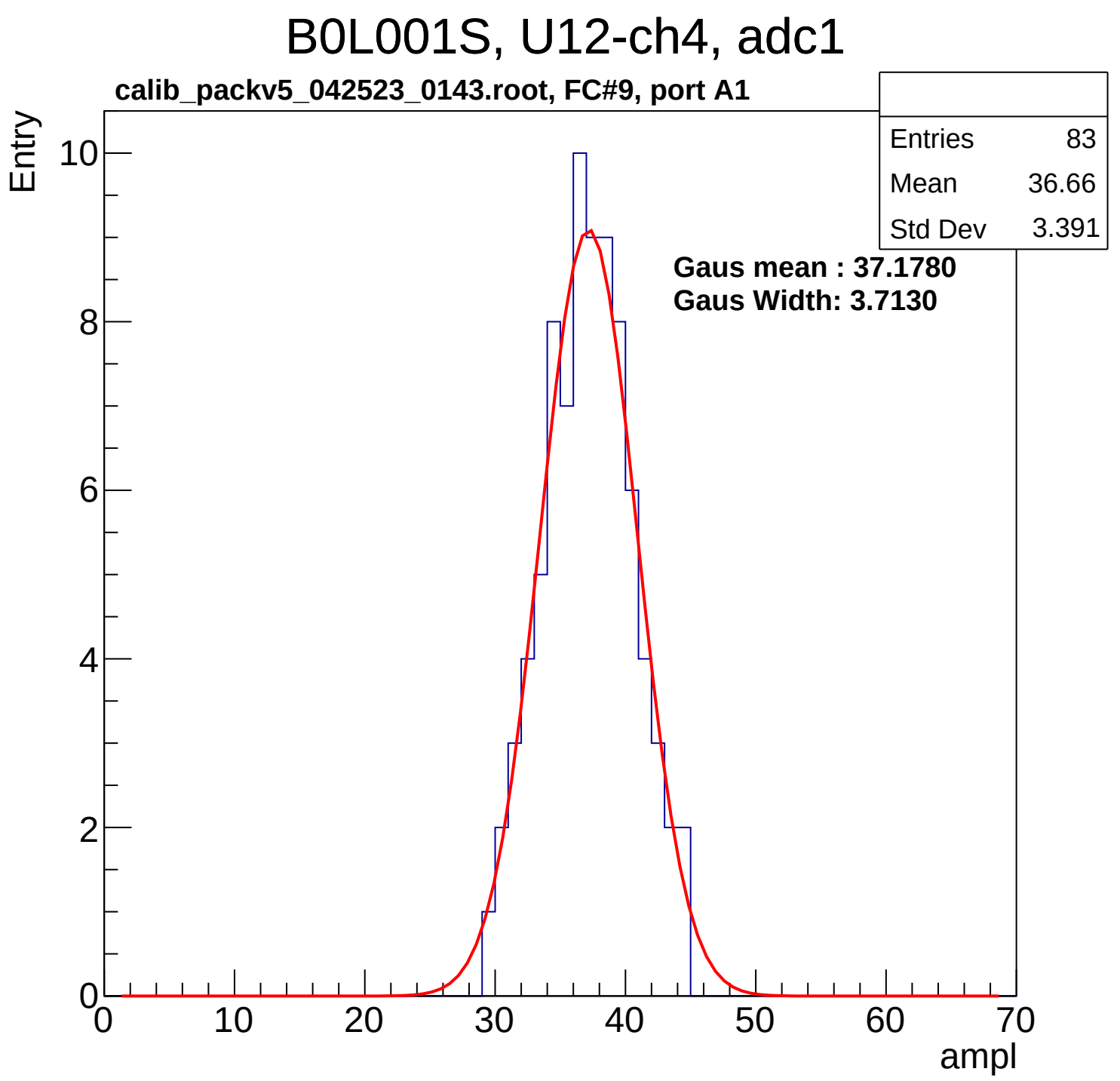
B0L001S, U12-ch4, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 83
Mean 36.66
Std Dev 3.391
Gaus mean : 37.1780
Gaus Width: 3.7130
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
50
60
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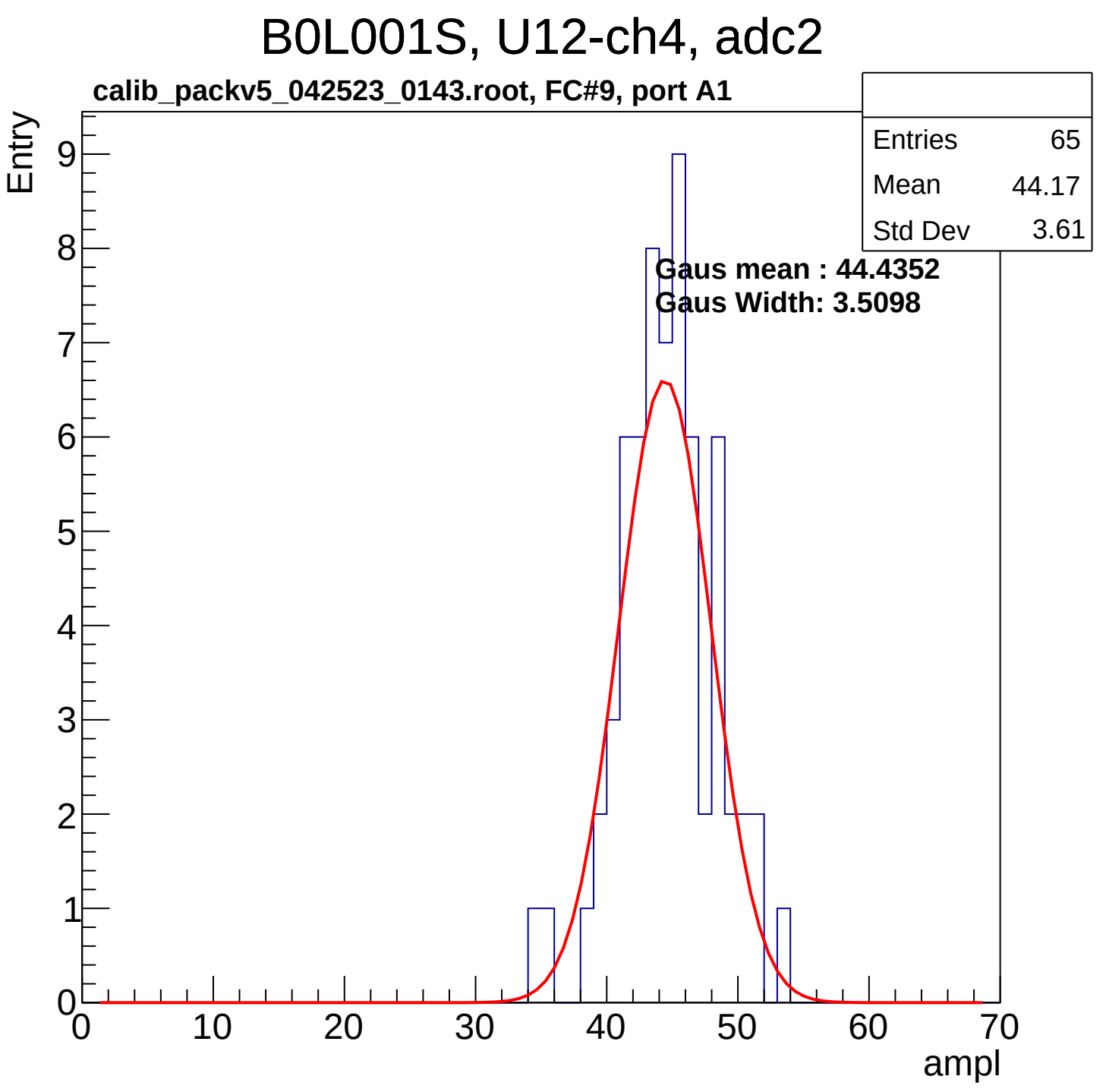
B0L001S, U12-ch4, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 65
Mean 44.17
Std Dev 3.61
Gaus mean : 44.4352
Gaus Width: 3.5098
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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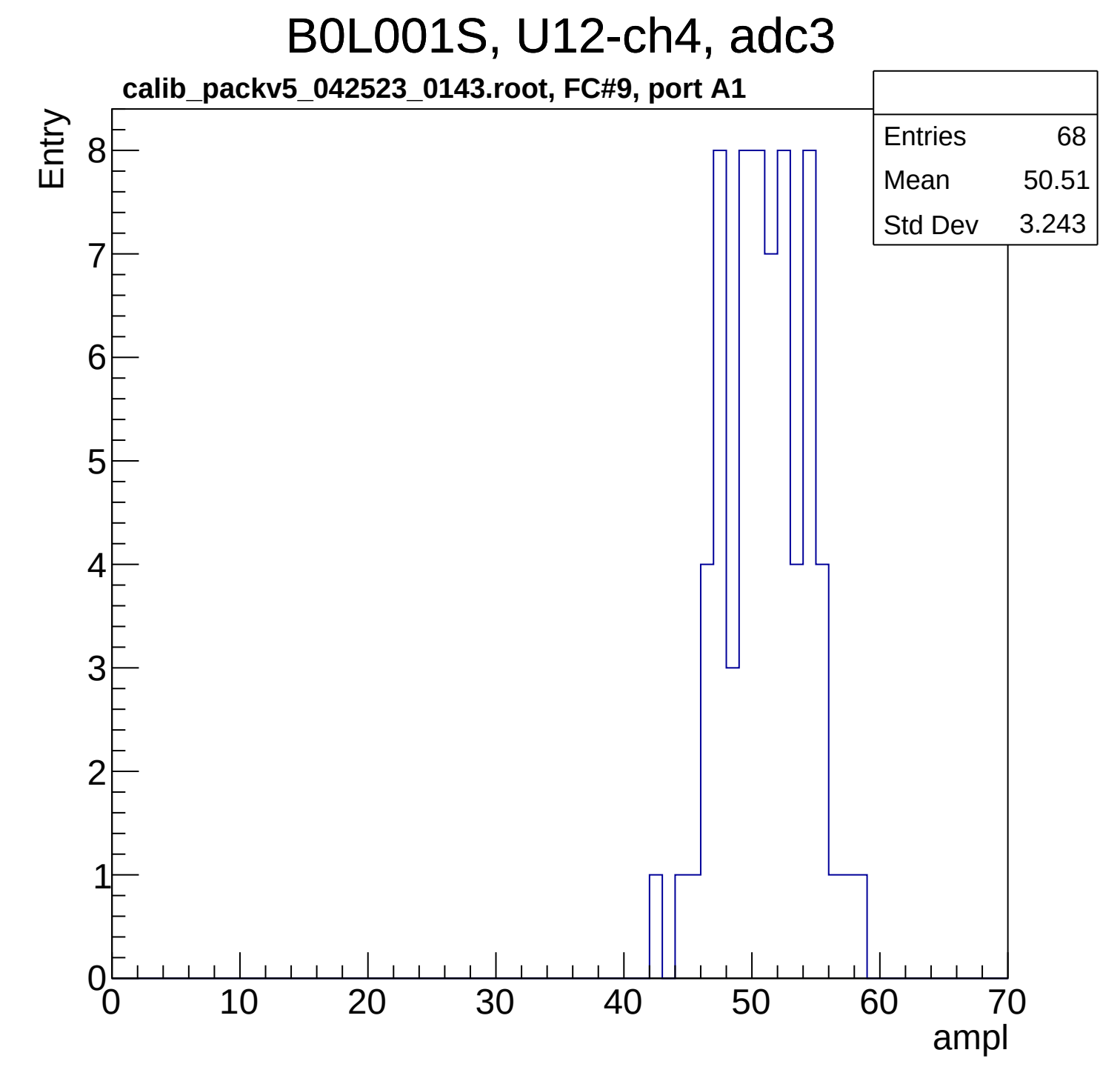
B0L001S, U12-ch4, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 68
Mean 50.51
Std Dev 3.243
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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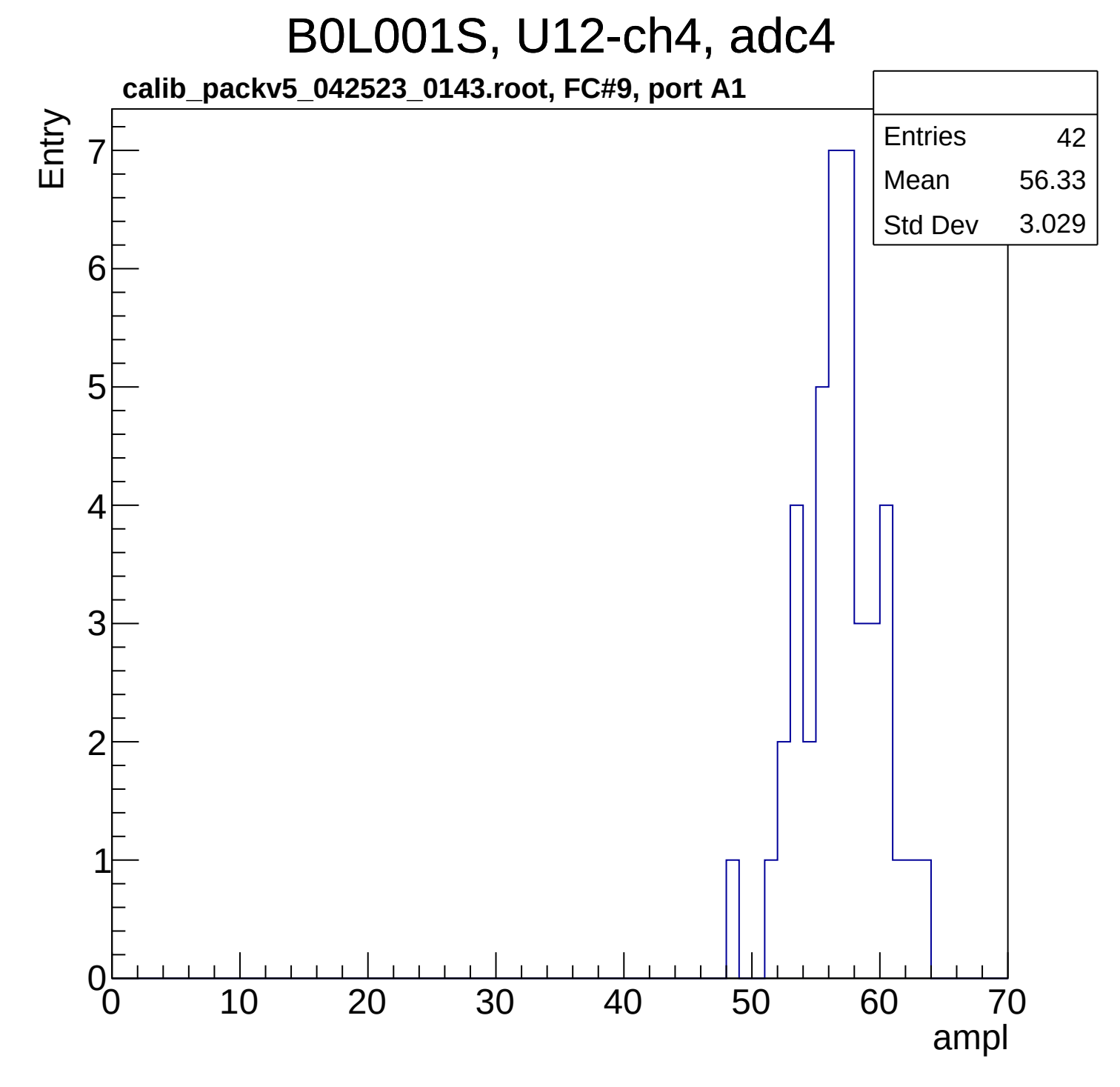
B0L001S, U12-ch4, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 42
Mean 56.33
Std Dev 3.029
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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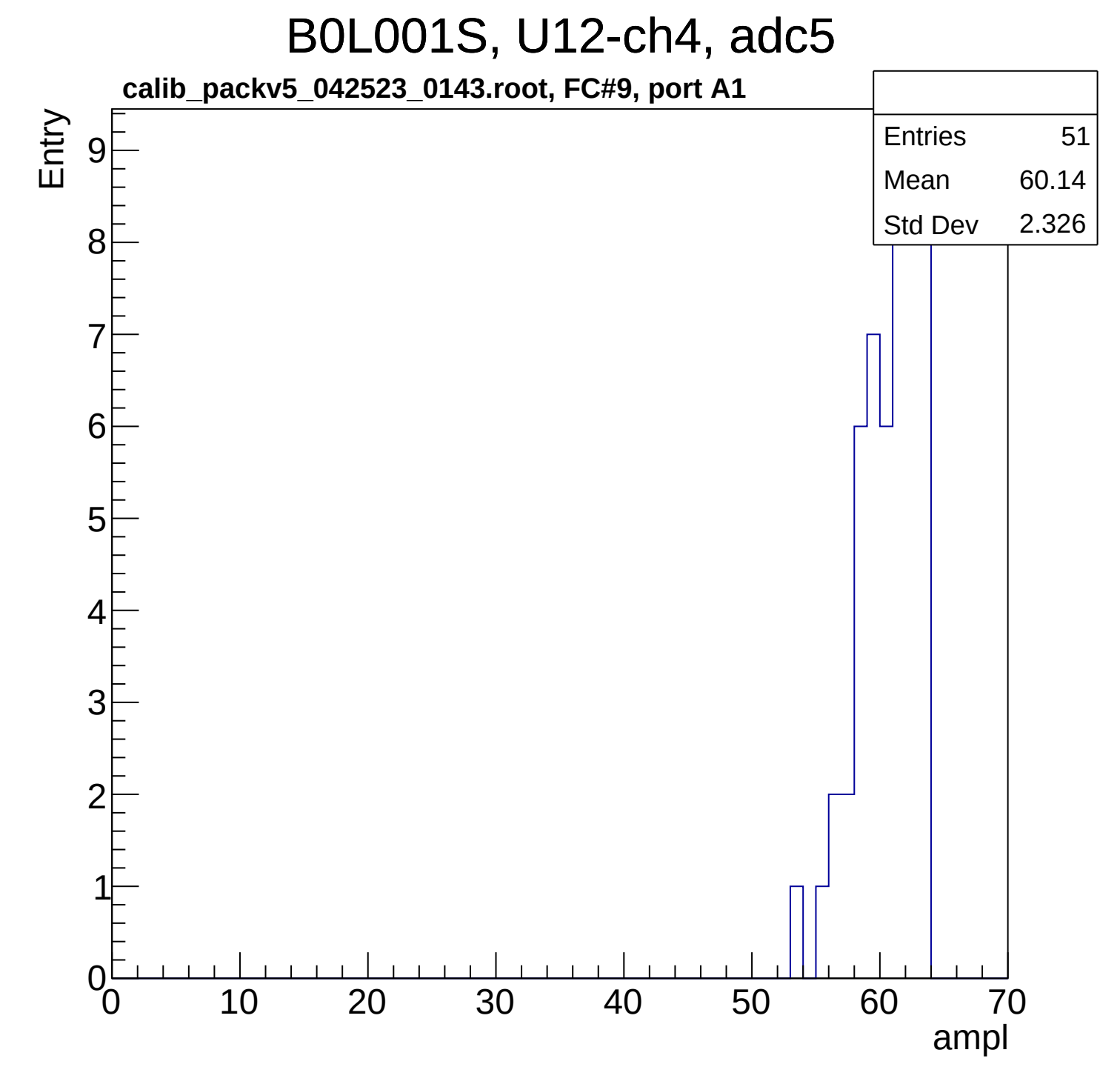
B0L001S, U12-ch4, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 51
Mean 60.14
Std Dev 2.326
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
50
60
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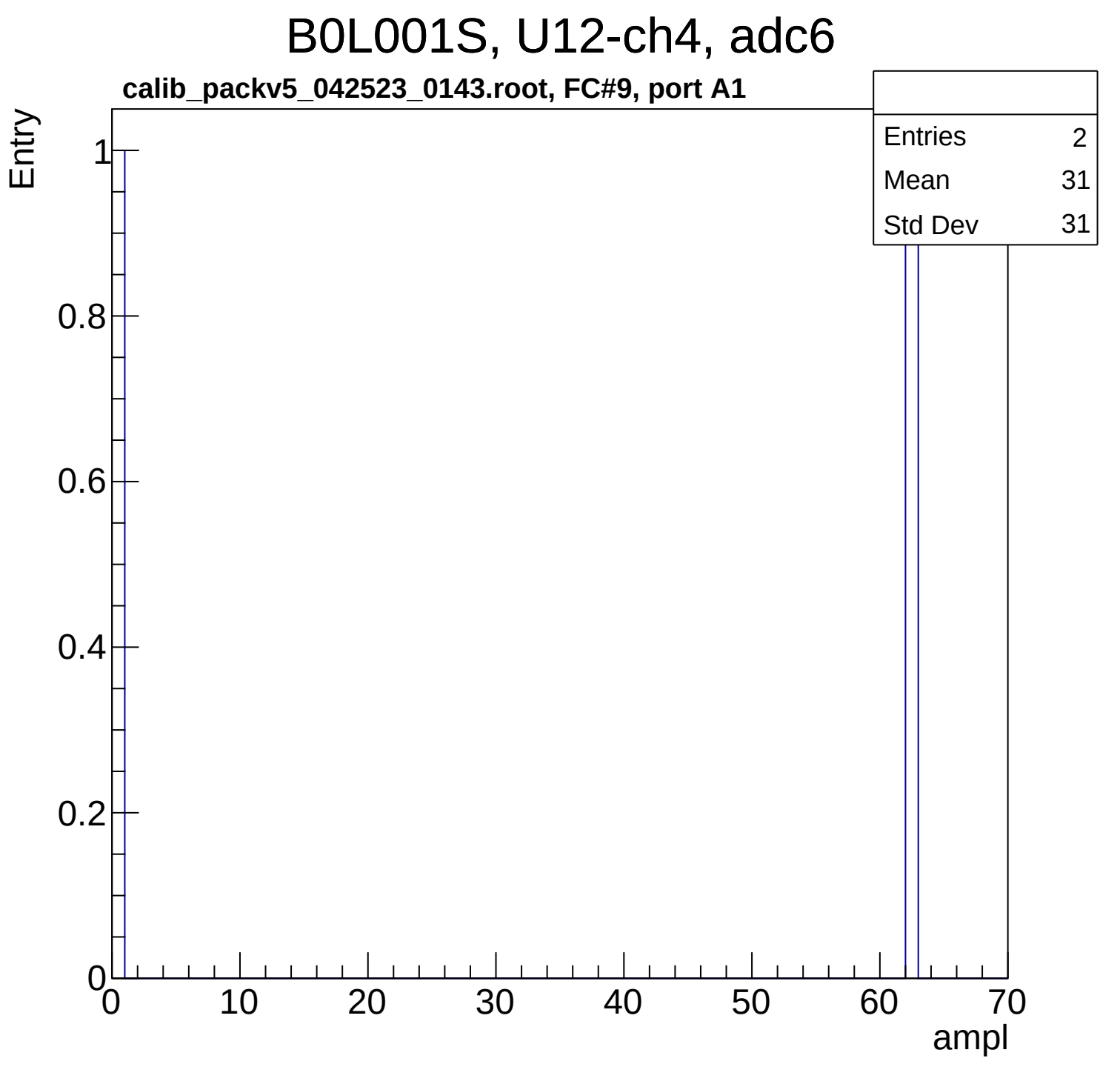
B0L001S, U12-ch4, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 31
Std Dev 31
Entry
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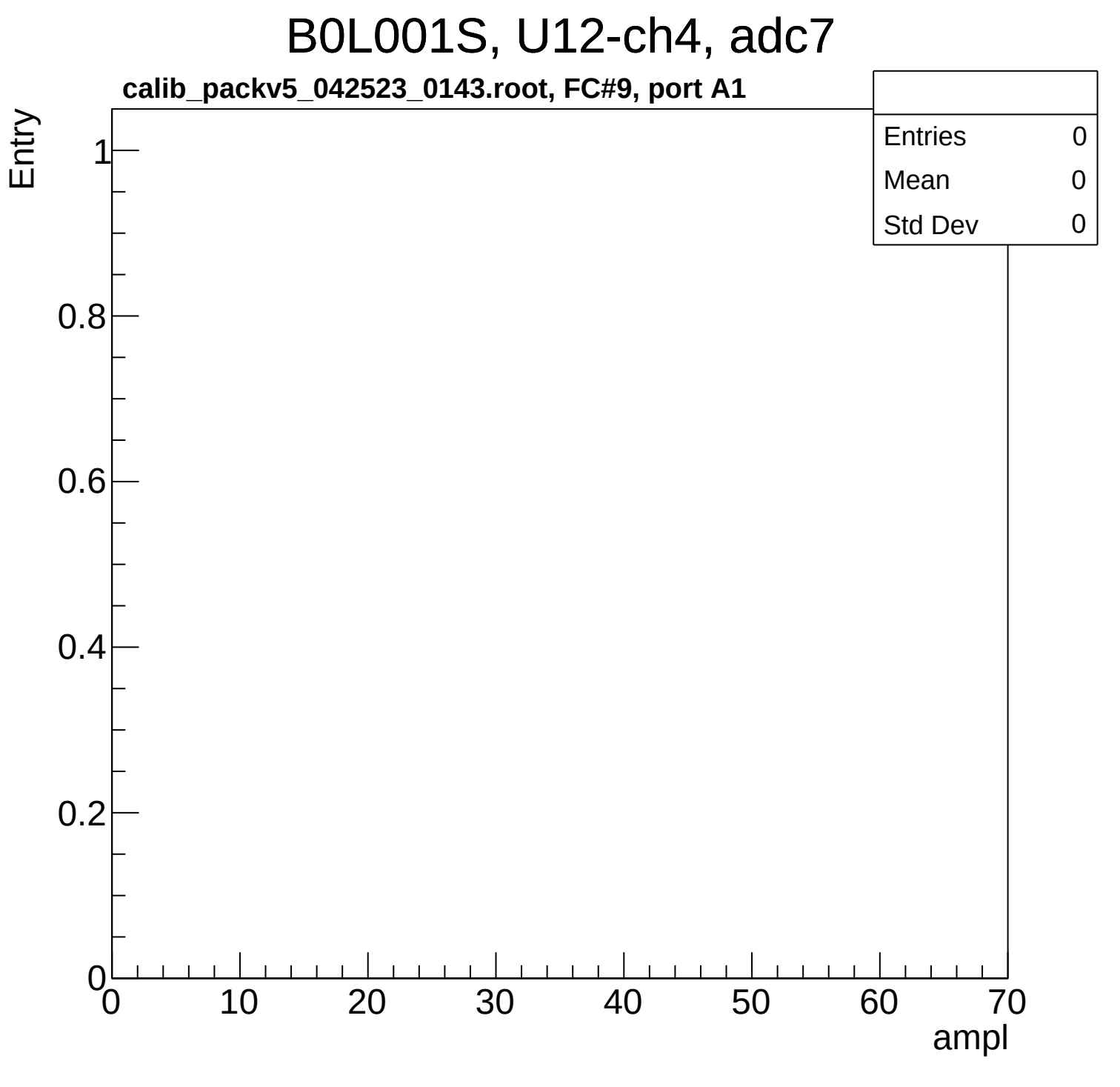
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch4, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
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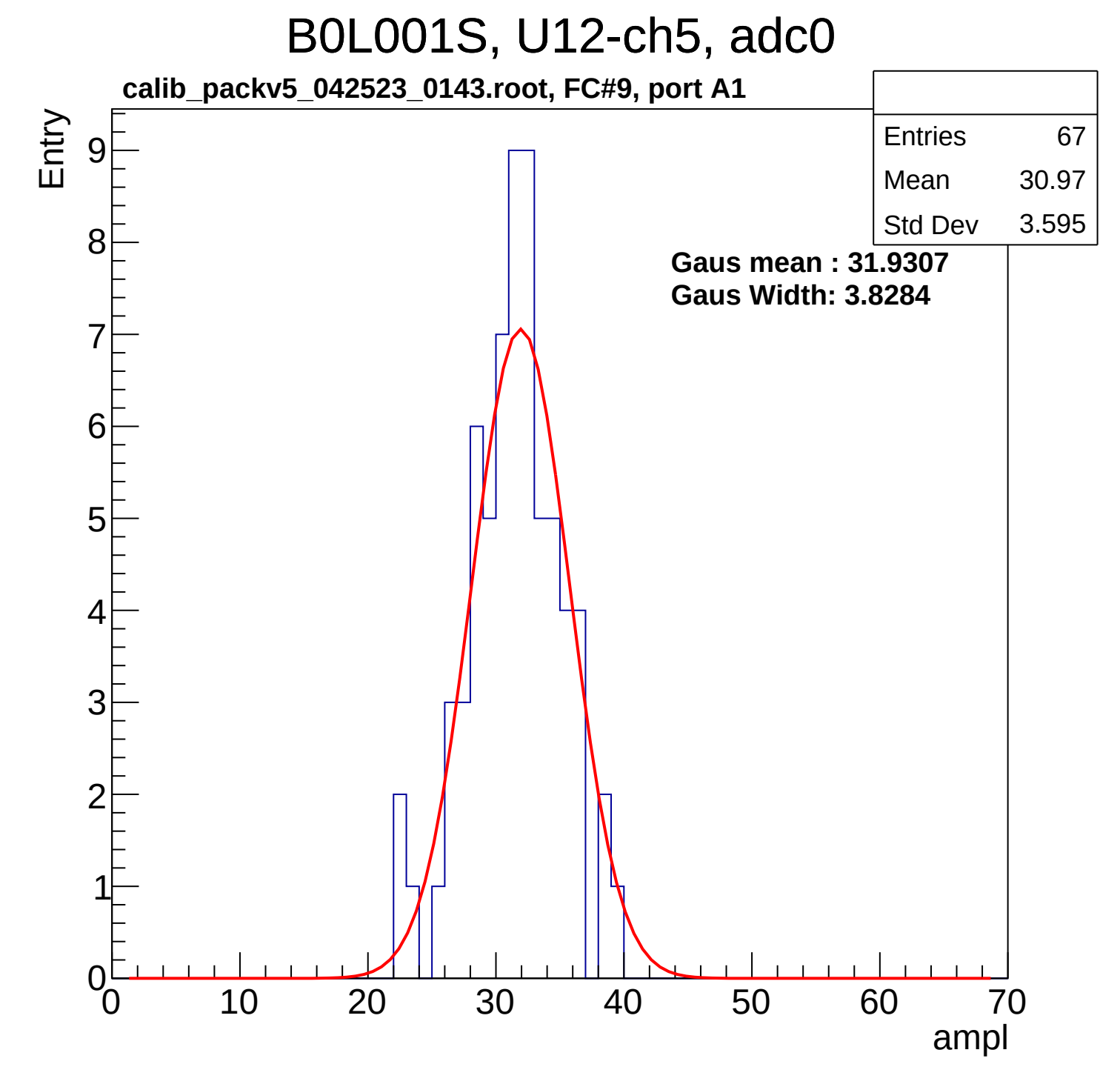
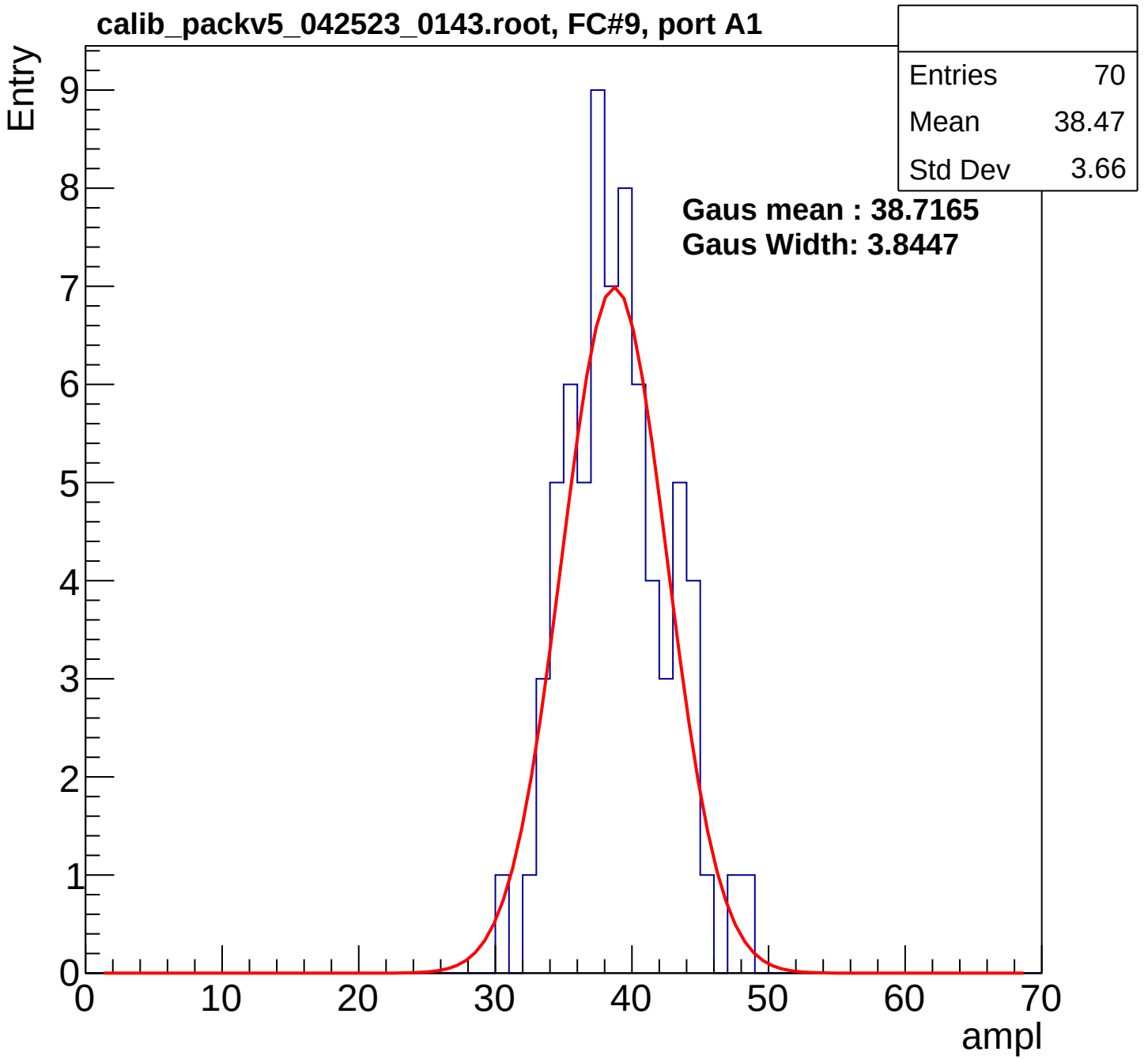
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch5, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 67
Mean 30.97
Std Dev 3.595
Gaus mean : 31.9307
Gaus Width: 3.8284
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch5, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 70
Mean 38.47
Std Dev 3.66
Gaus mean : 38.7165
Gaus Width: 3.8447
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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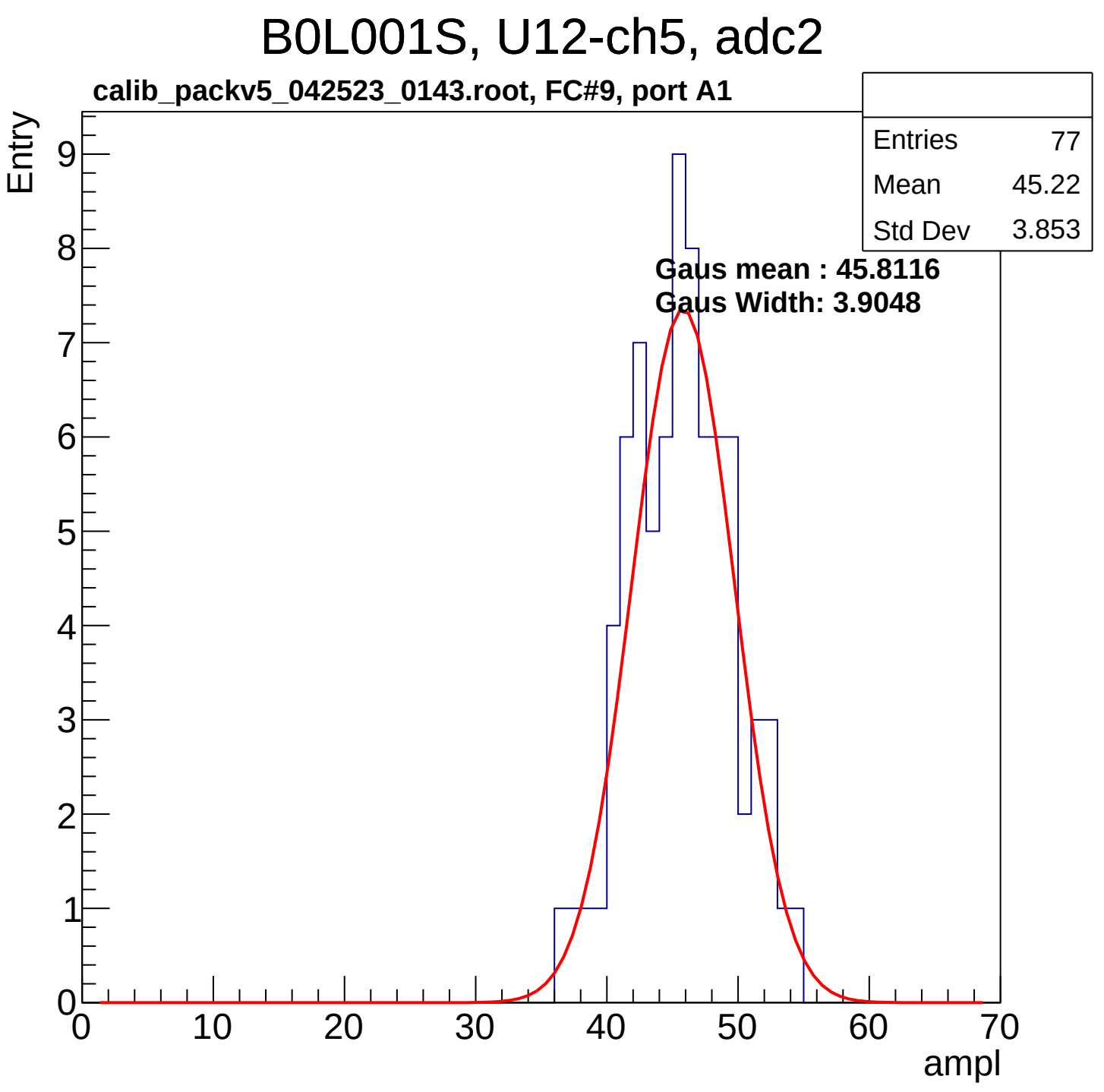
B0L001S, U12-ch5, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 77
Mean 45.22
Std Dev 3.853
Gaus mean : 45.8116
Gaus Width: 3.9048
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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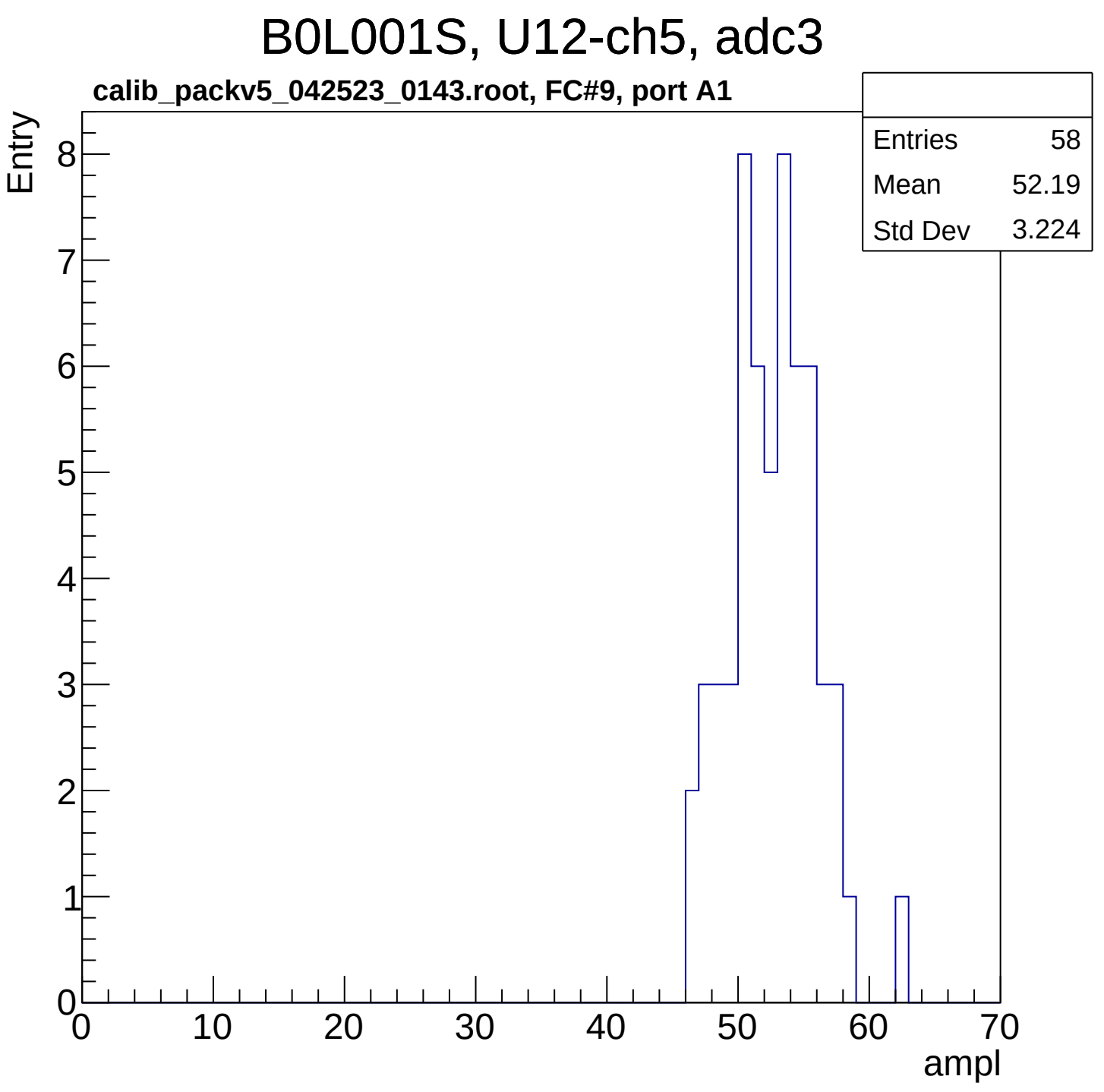
B0L001S, U12-ch5, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 58
Mean 52.19
Std Dev 3.224
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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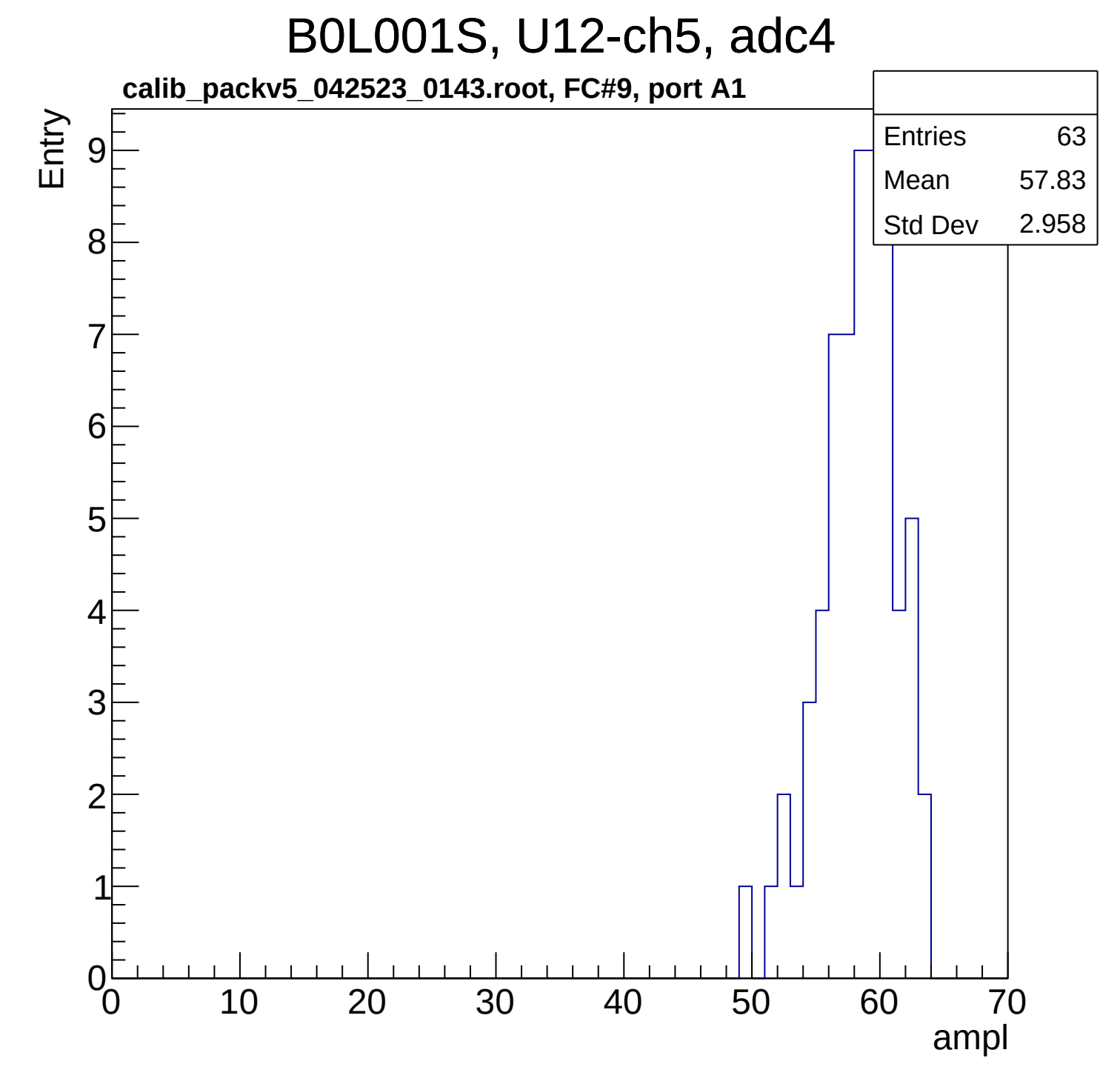
B0L001S, U12-ch5, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 63
Mean 57.83
Std Dev 2.958
Entry
ampl
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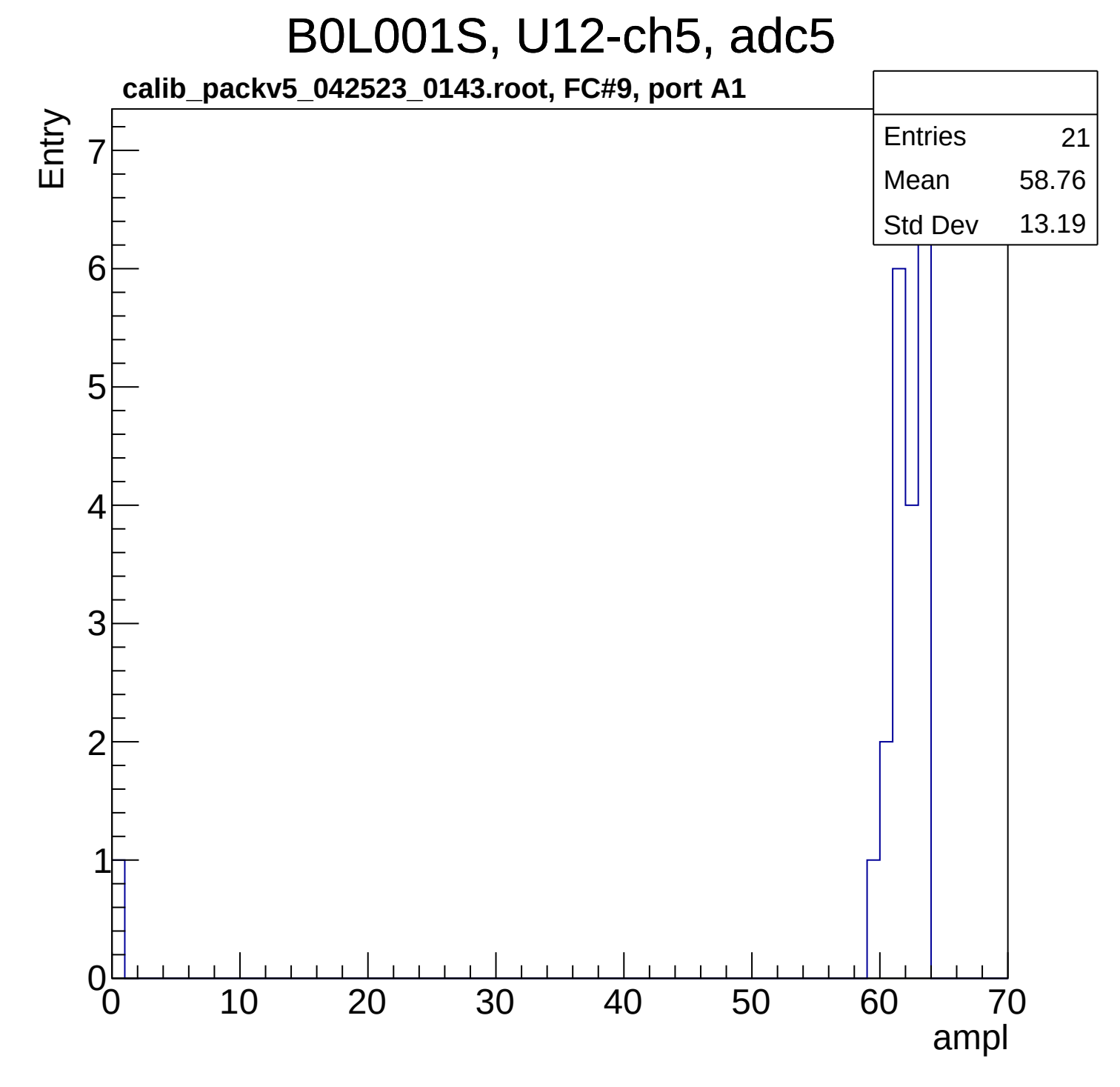
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch5, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 21
Mean 58.76
Std Dev 13.19
Entry
ampl
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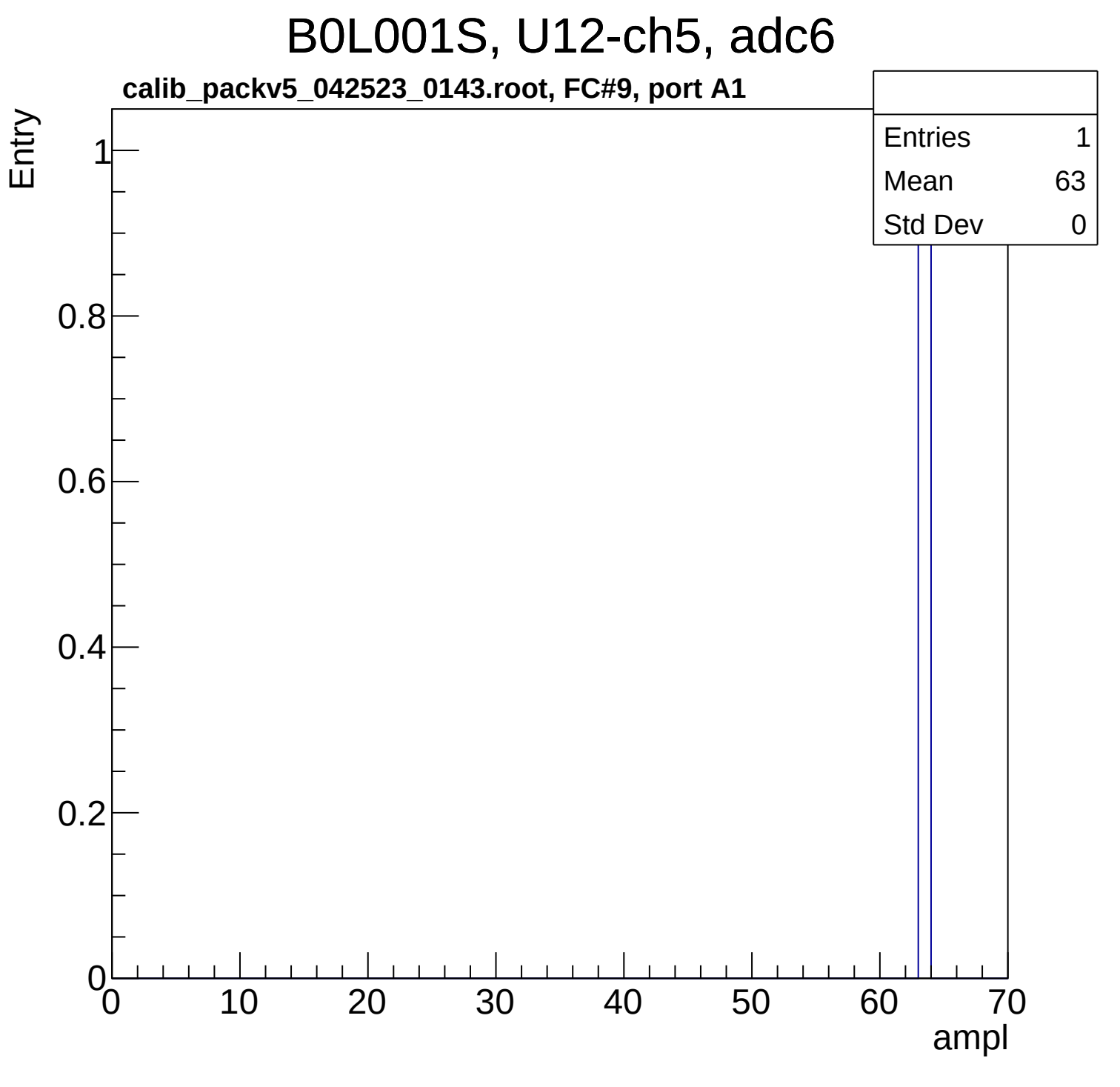
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B0L001S, U12-ch5, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 63
Std Dev 0
Entry
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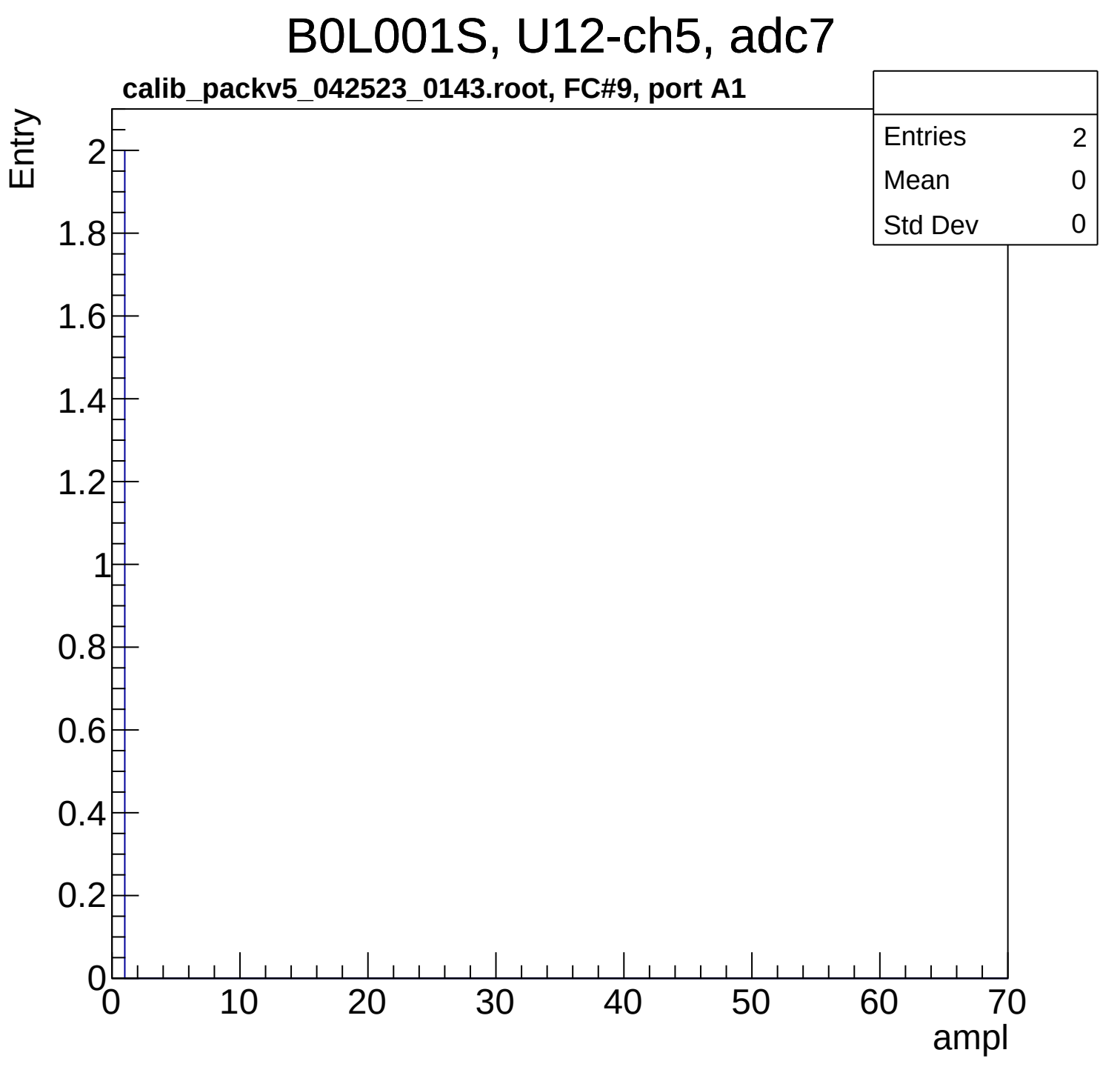
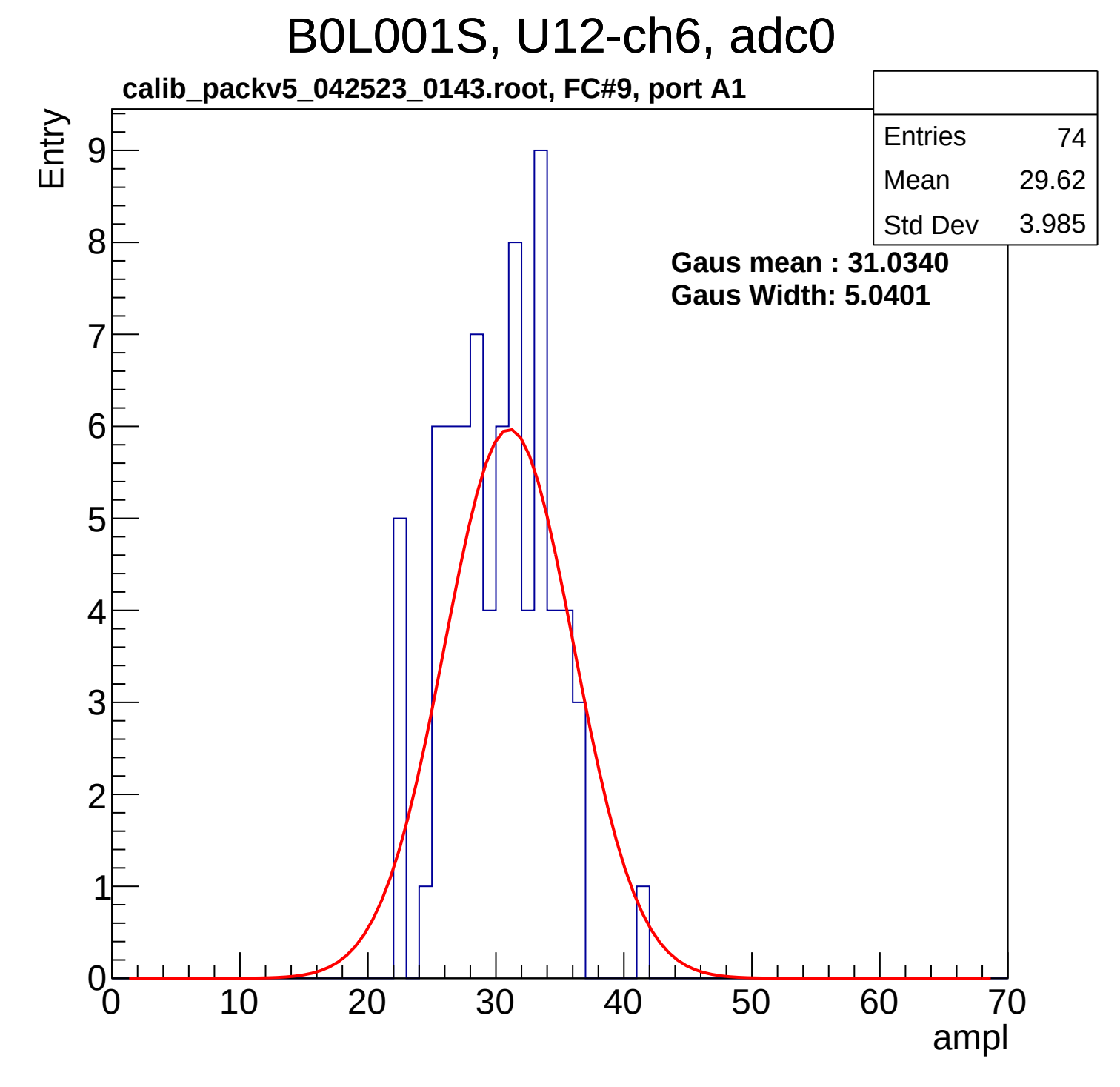
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch5, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch6, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 74
Mean 29.62
Std Dev 3.985
Gaus mean : 31.0340
Gaus Width: 5.0401
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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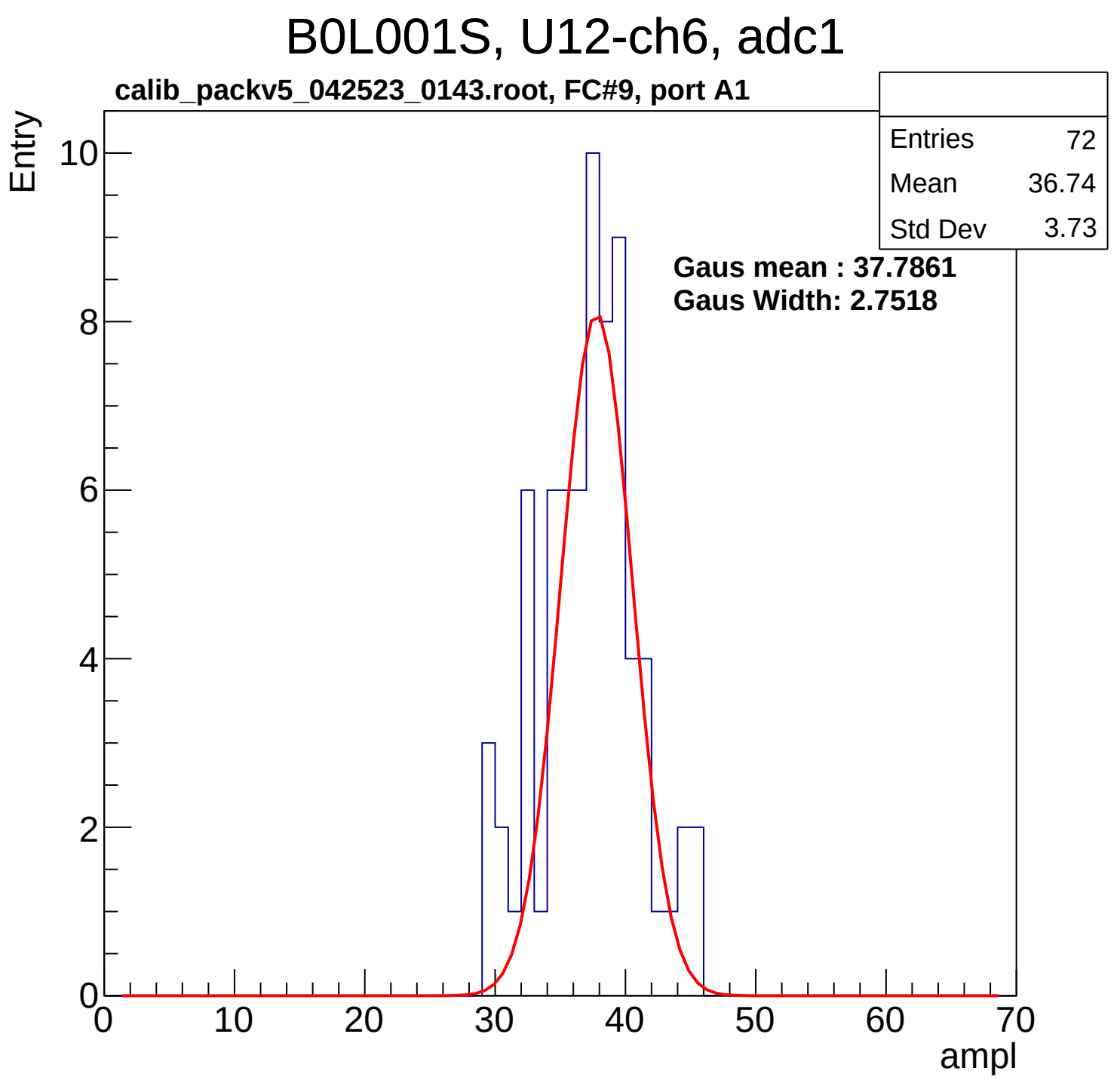
20
30
40
50
60
70


B0L001S, U12-ch6, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 72
Mean 36.74
Std Dev 3.73
Gaus mean : 37.7861
Gaus Width: 2.7518
Entry
ampl
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2
4
6
8
10
0
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20
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40
50
60
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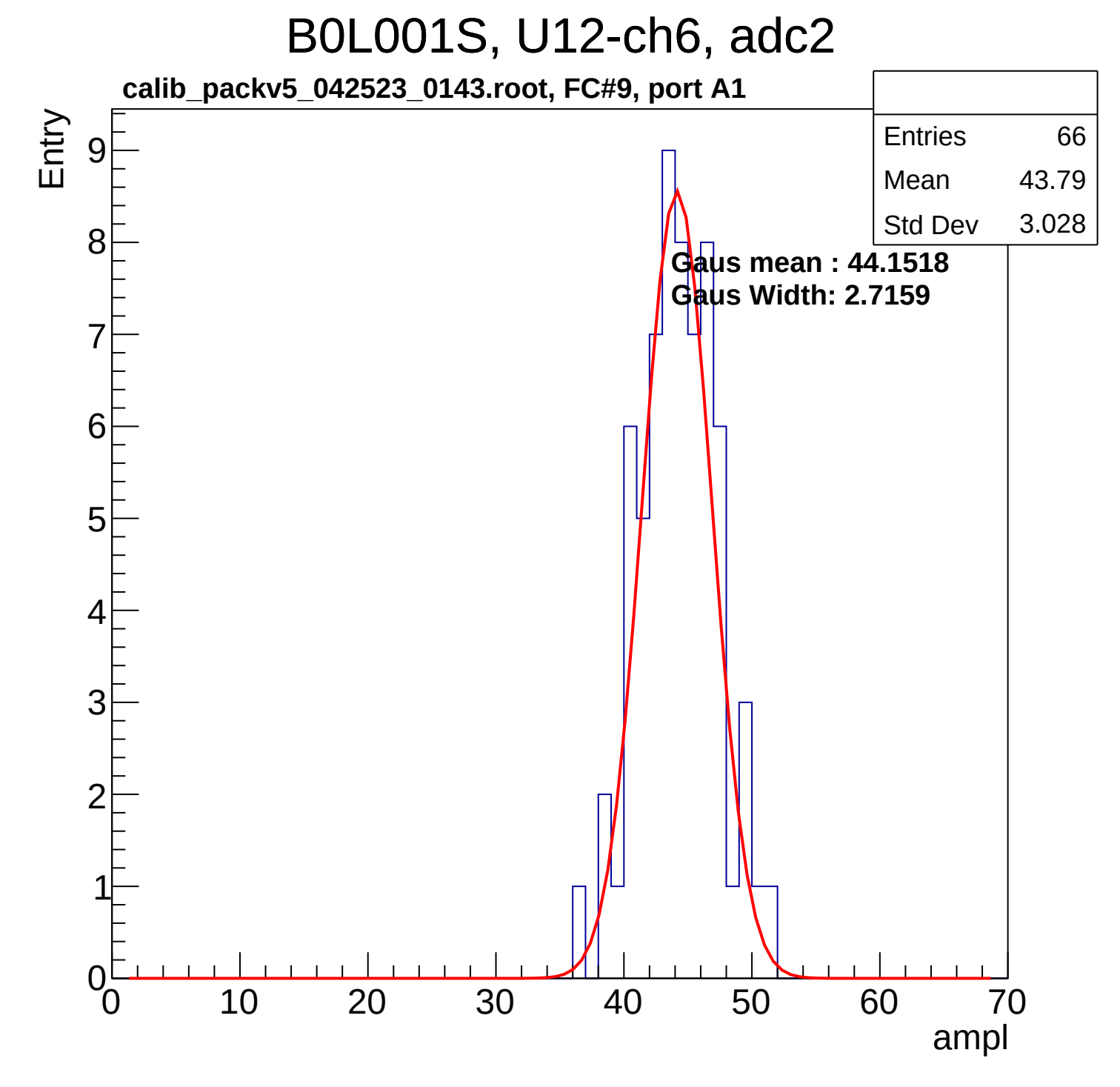
B0L001S, U12-ch6, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 66
Mean 43.79
Std Dev 3.028
Gaus mean : 44.1518
Gaus Width: 2.7159
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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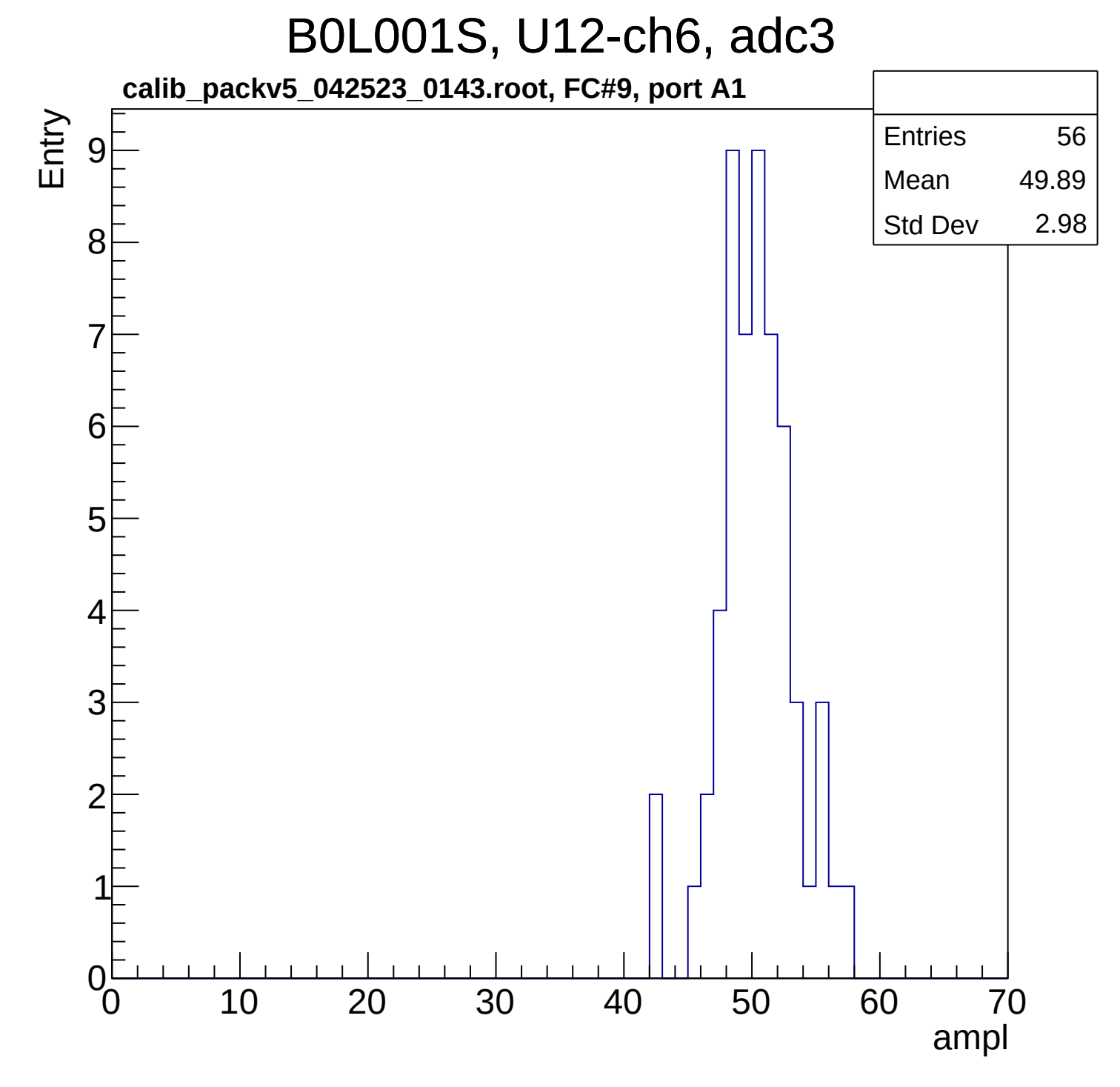
B0L001S, U12-ch6, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 56
Mean 49.89
Std Dev 2.98
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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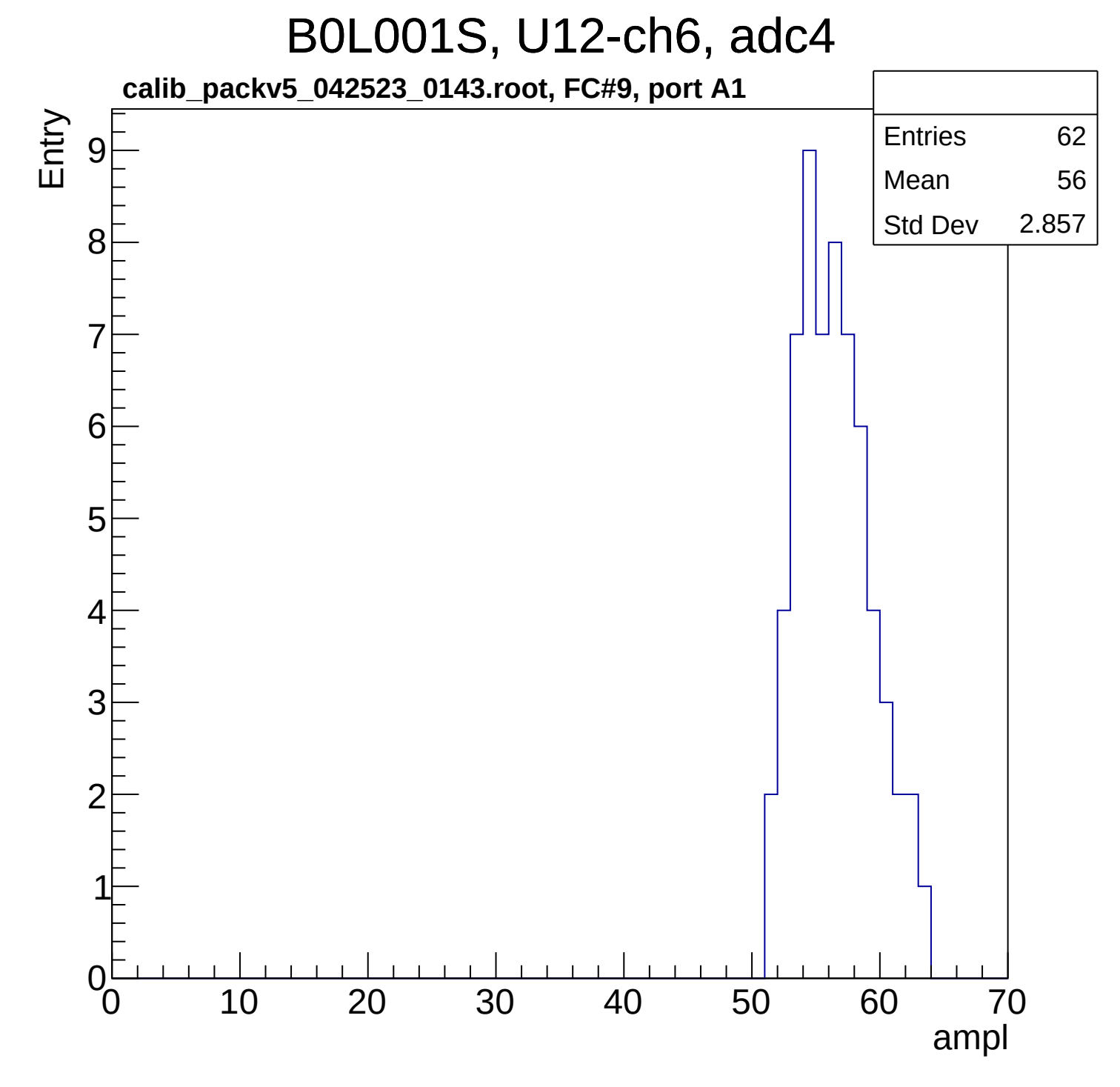
40
50
60
70


B0L001S, U12-ch6, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 62
Mean 56
Std Dev 2.857
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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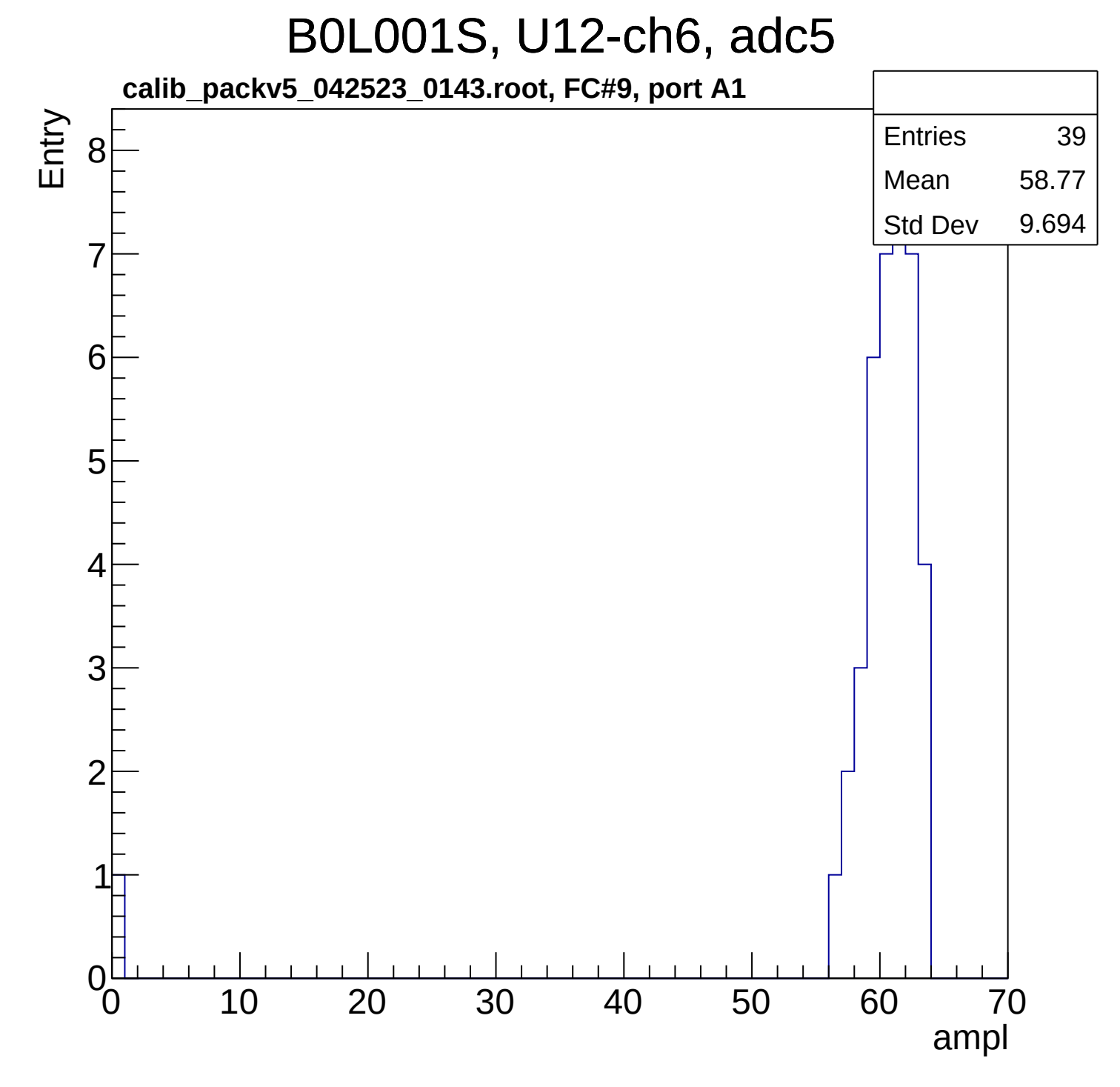
40
50
60
70


B0L001S, U12-ch6, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 39
Mean 58.77
Std Dev 9.694
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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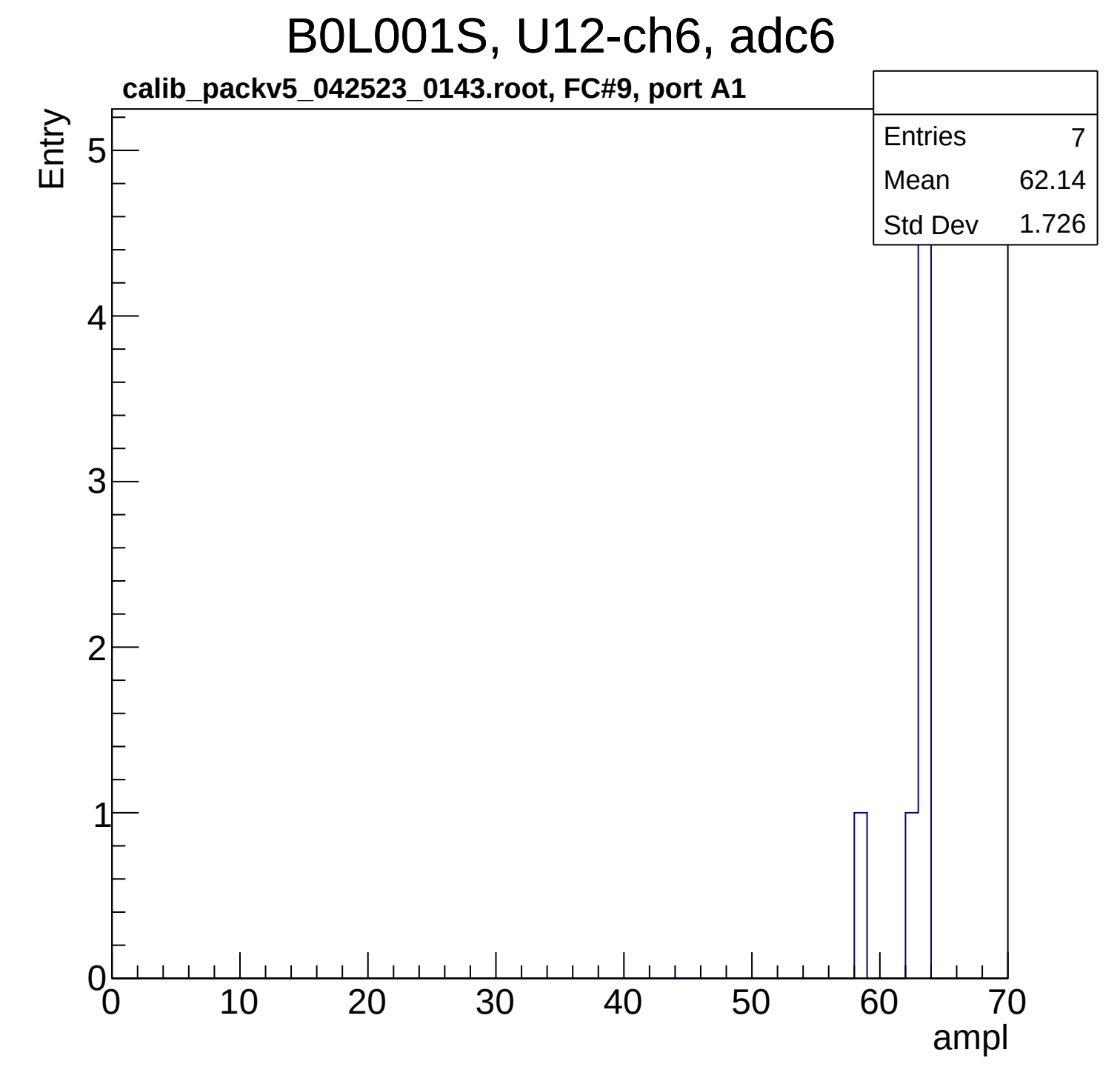
B0L001S, U12-ch6, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 7
Mean 62.14
Std Dev 1.726
Entry
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1
2
3
4
5
0
10
20
30
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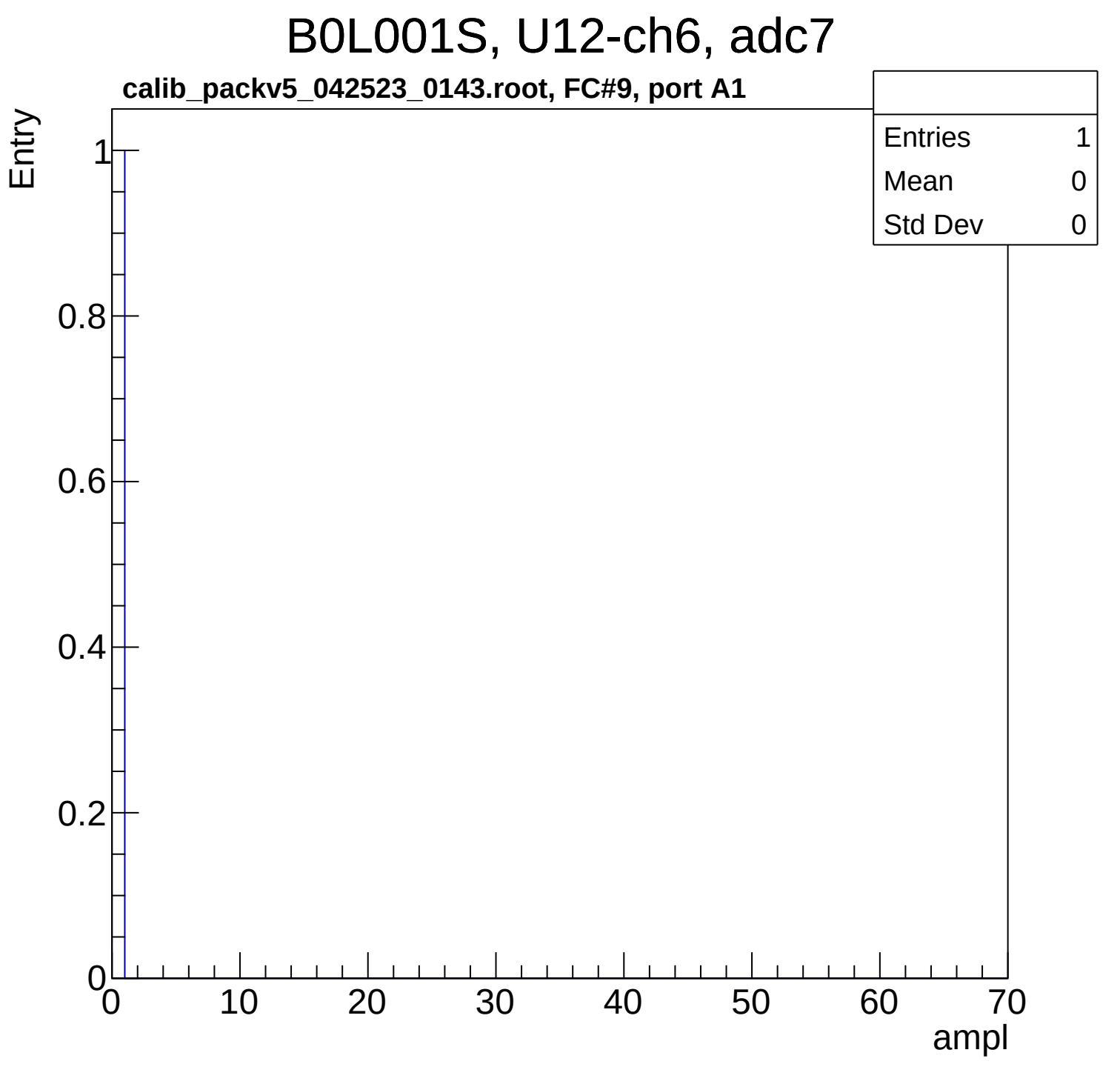
50
60
70
ampl


B0L001S, U12-ch6, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 0
Std Dev 0
Entry
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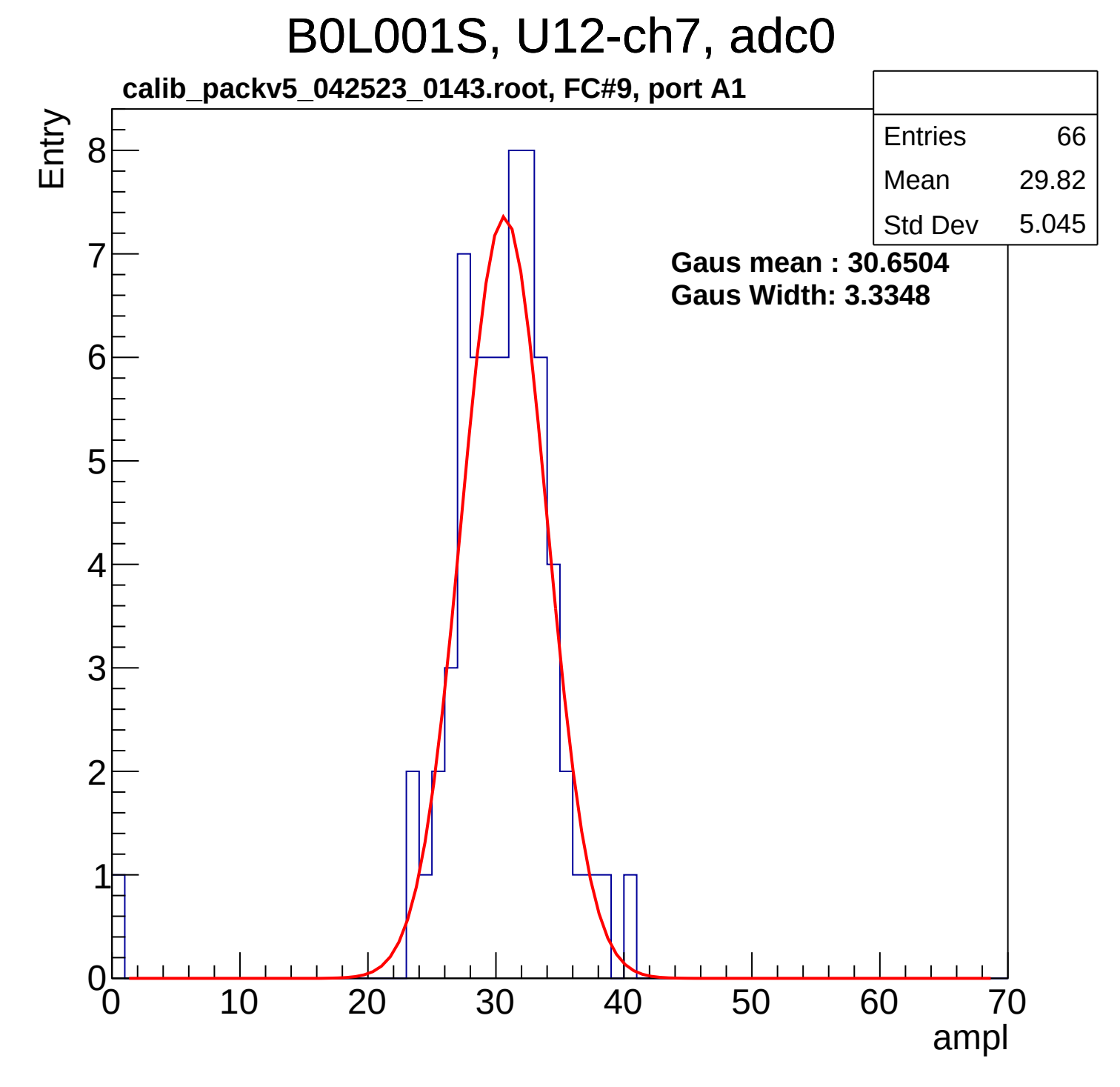
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch7, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 66
Mean 29.82
Std Dev 5.045
Gaus mean : 30.6504
Gaus Width: 3.3348
Entry
ampl
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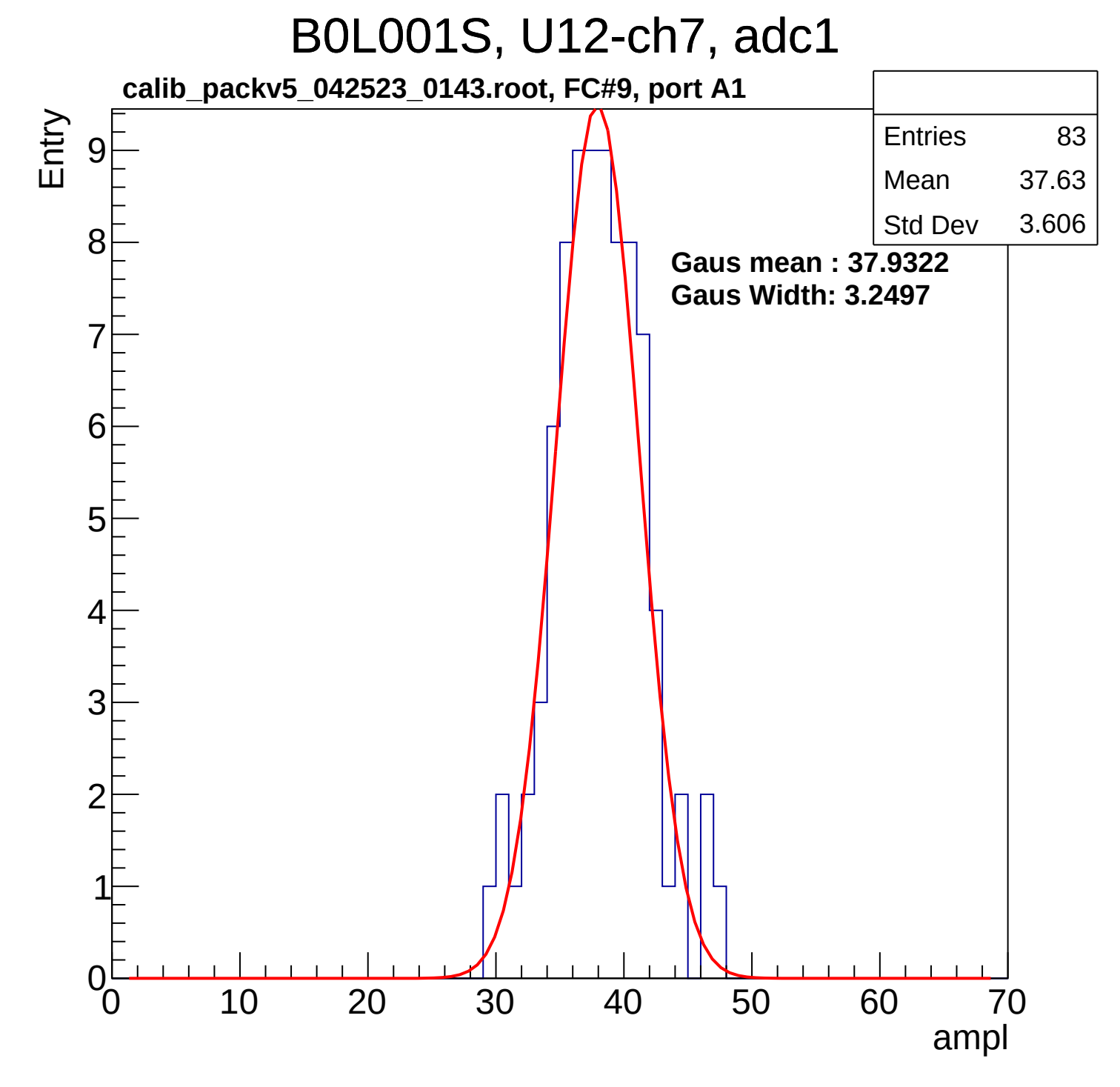
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch7, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 83
Mean 37.63
Std Dev 3.606
Gaus mean : 37.9322
Gaus Width: 3.2497
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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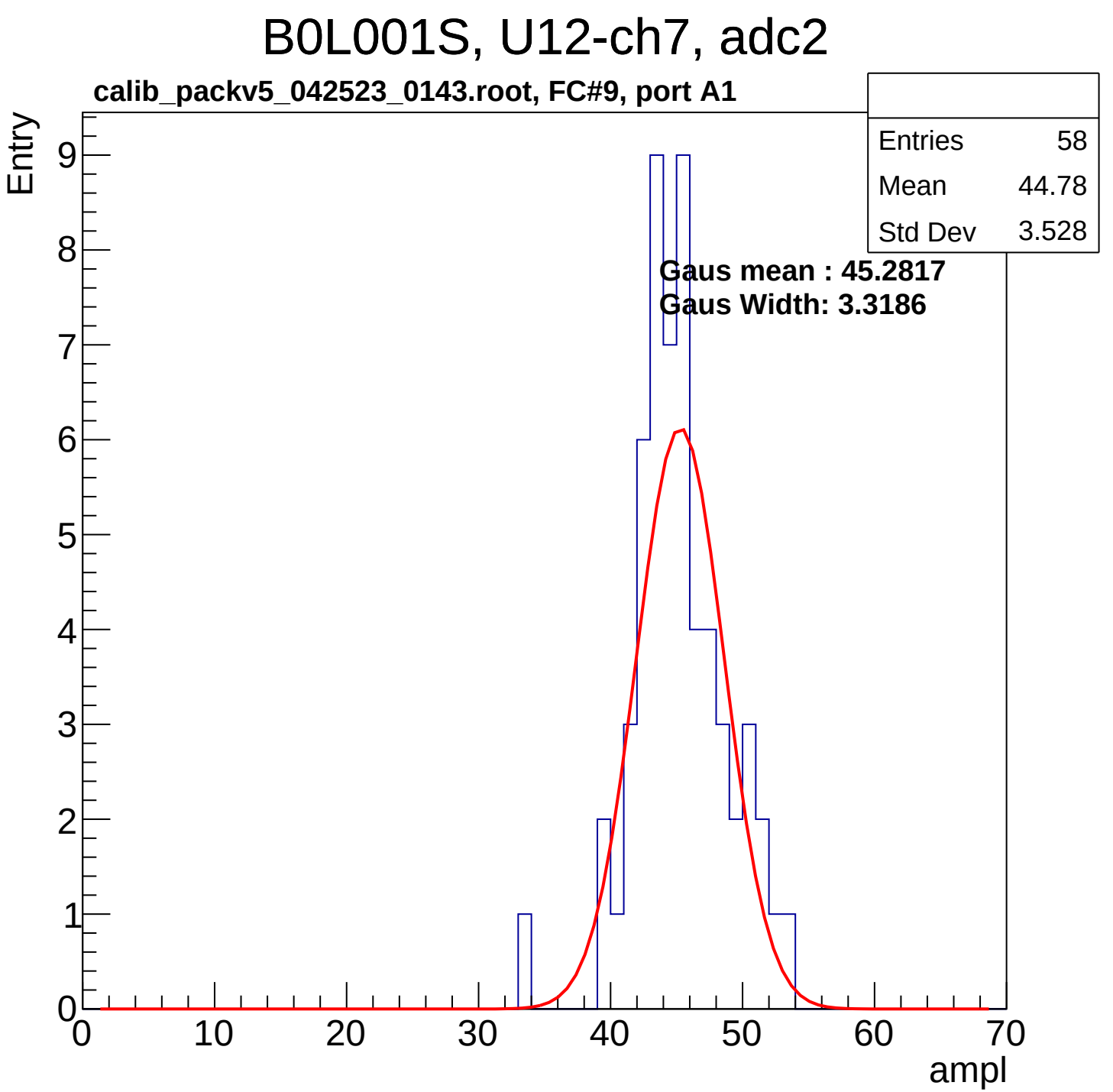
B0L001S, U12-ch7, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 58
Mean 44.78
Std Dev 3.528
Gaus mean : 45.2817
Gaus Width: 3.3186
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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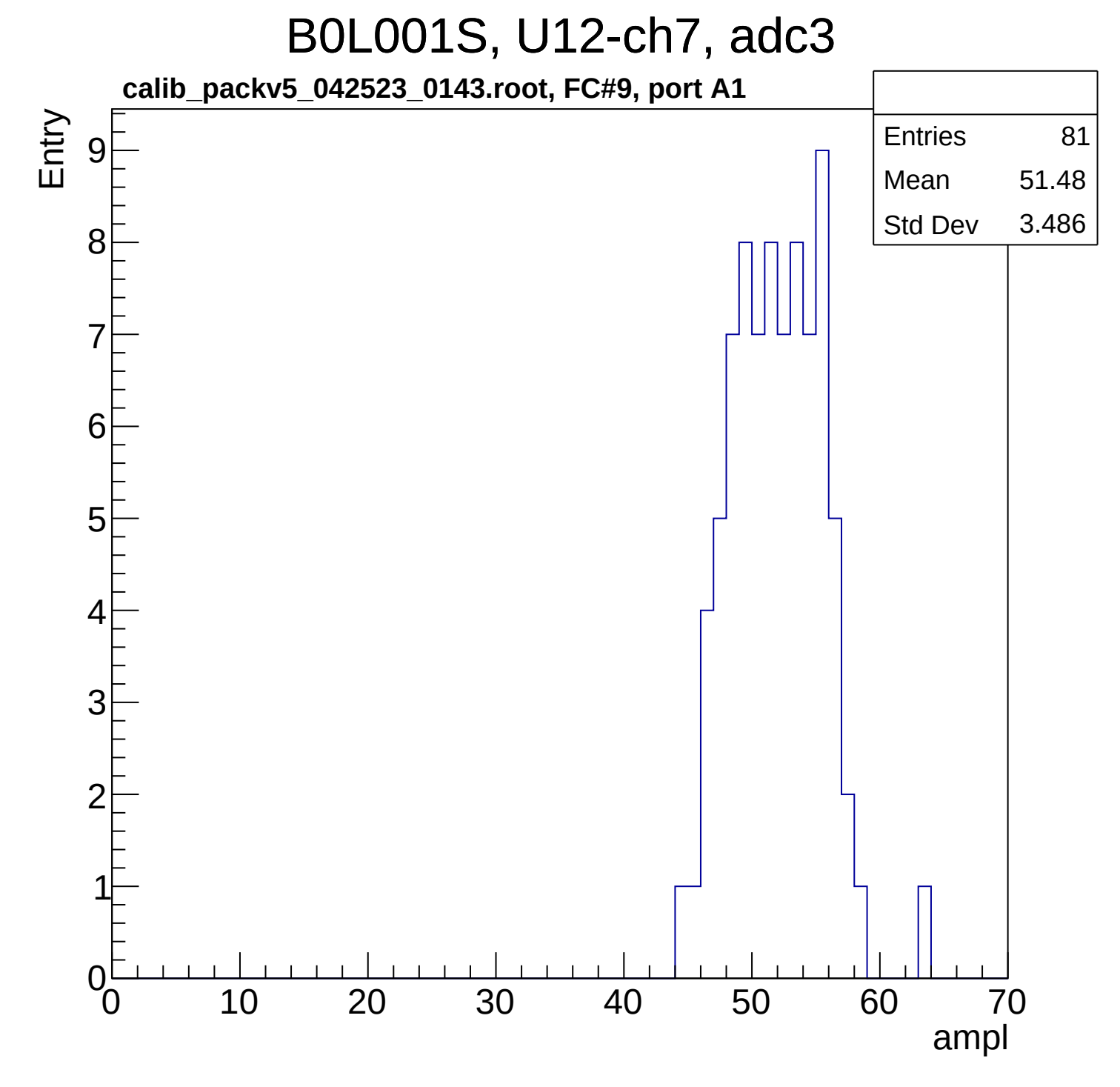
B0L001S, U12-ch7, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 81
Mean 51.48
Std Dev 3.486
Entry
ampl
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3
4
5
6
7
8
9
0
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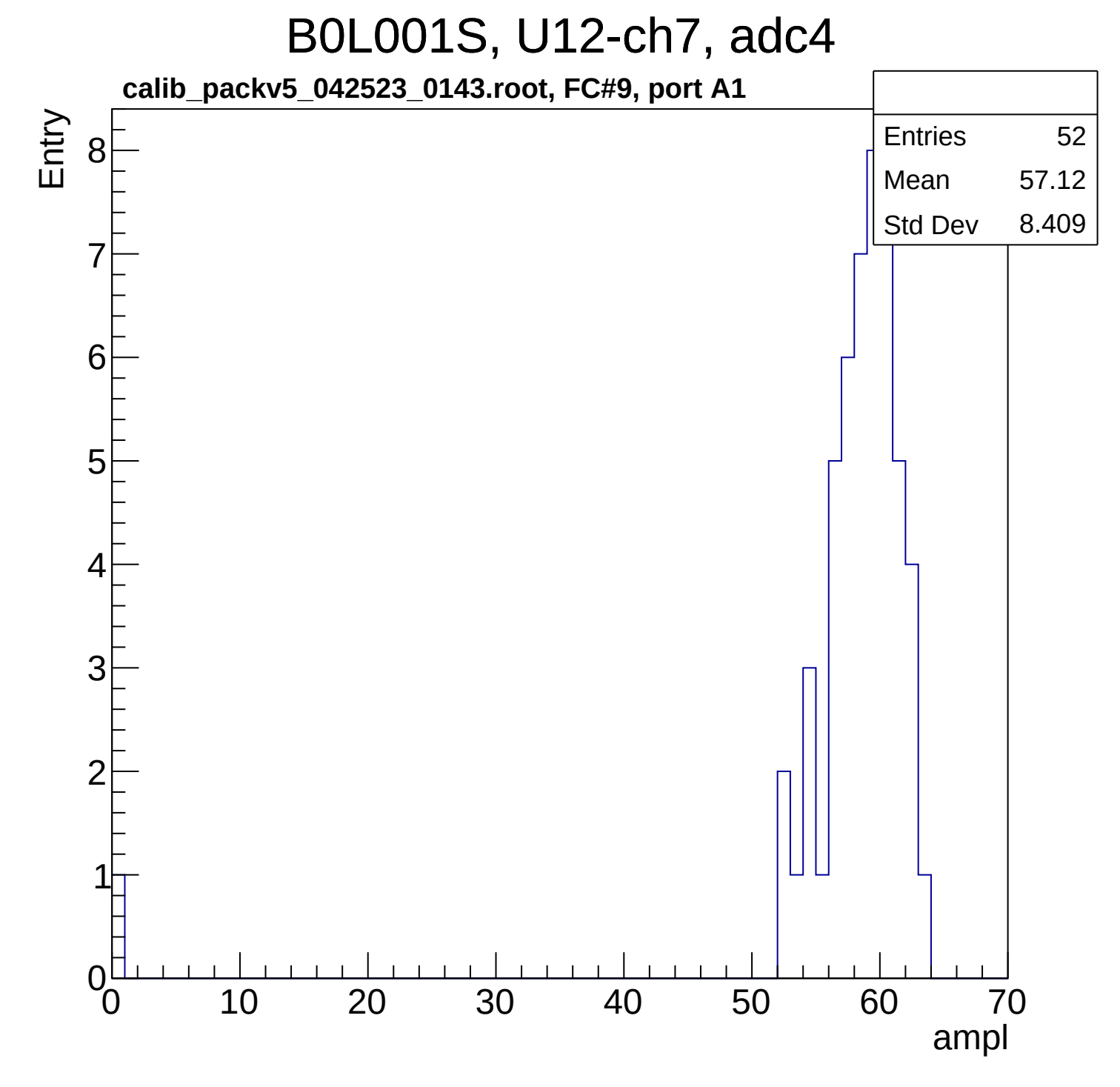
B0L001S, U12-ch7, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 52
Mean 57.12
Std Dev 8.409
Entry
ampl
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5
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7
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0
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50
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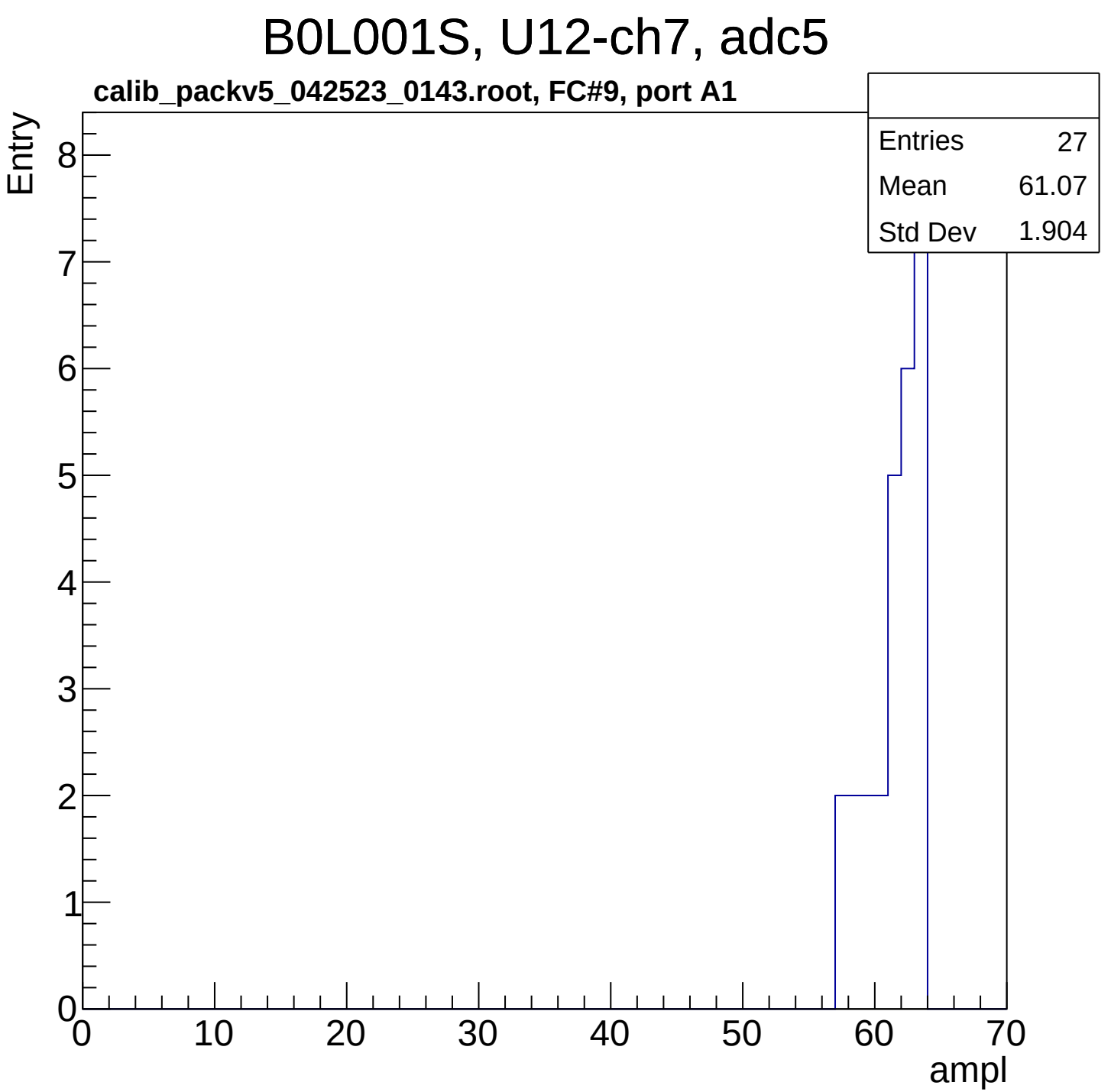
B0L001S, U12-ch7, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 27
Mean 61.07
Std Dev 1.904
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
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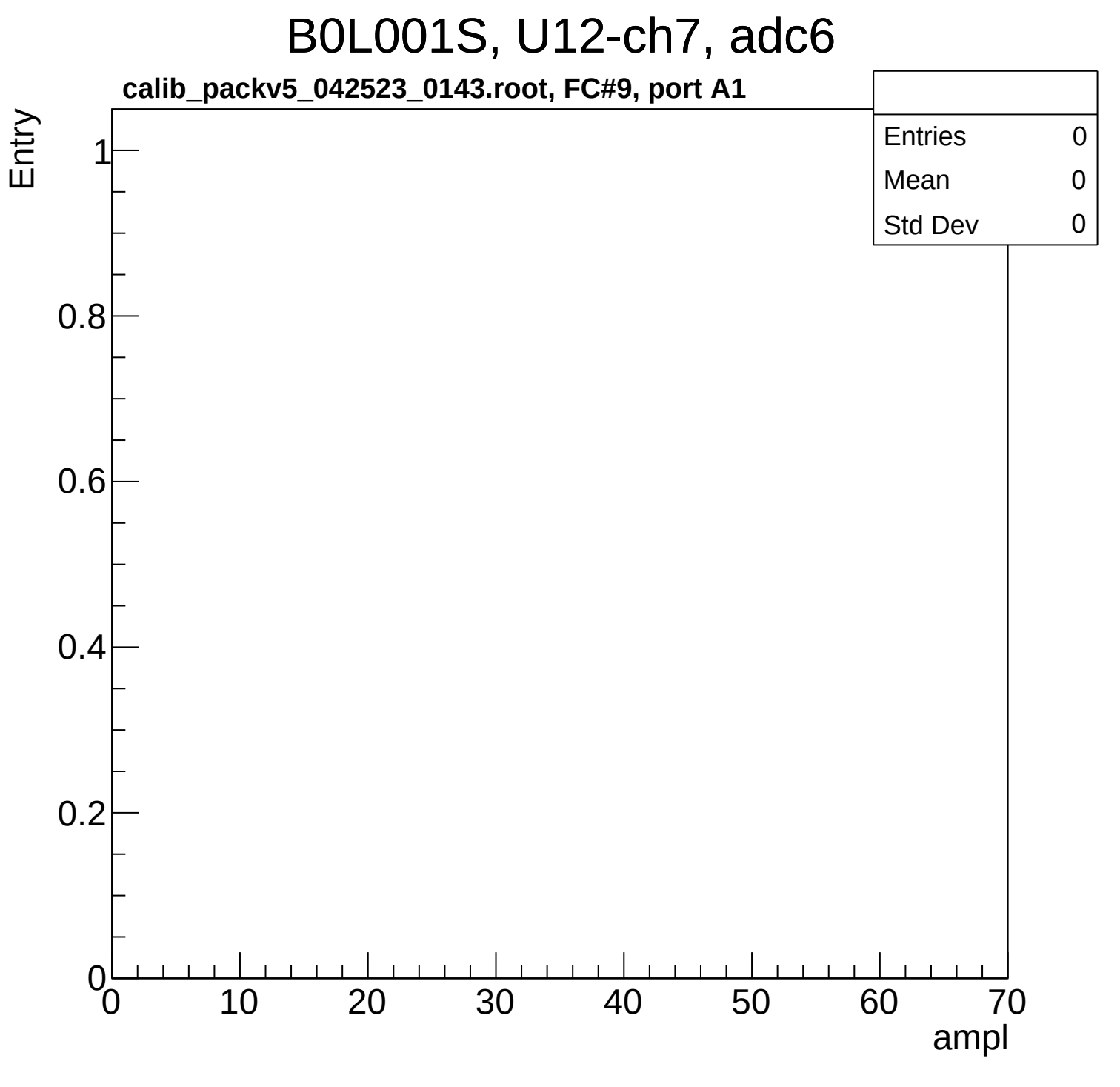
50
60
70
ampl


B0L001S, U12-ch7, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
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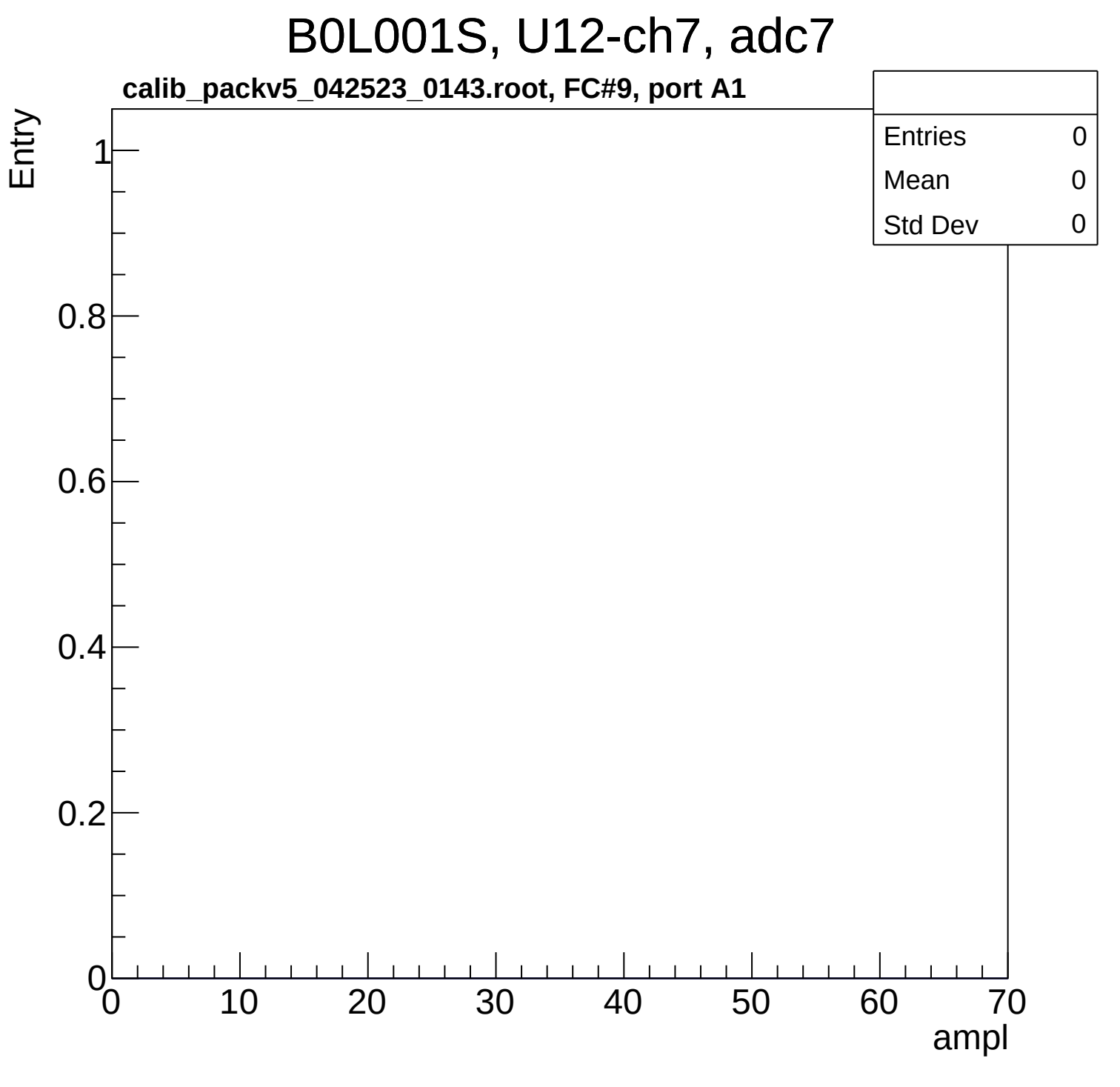
50
60
70
ampl


B0L001S, U12-ch7, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
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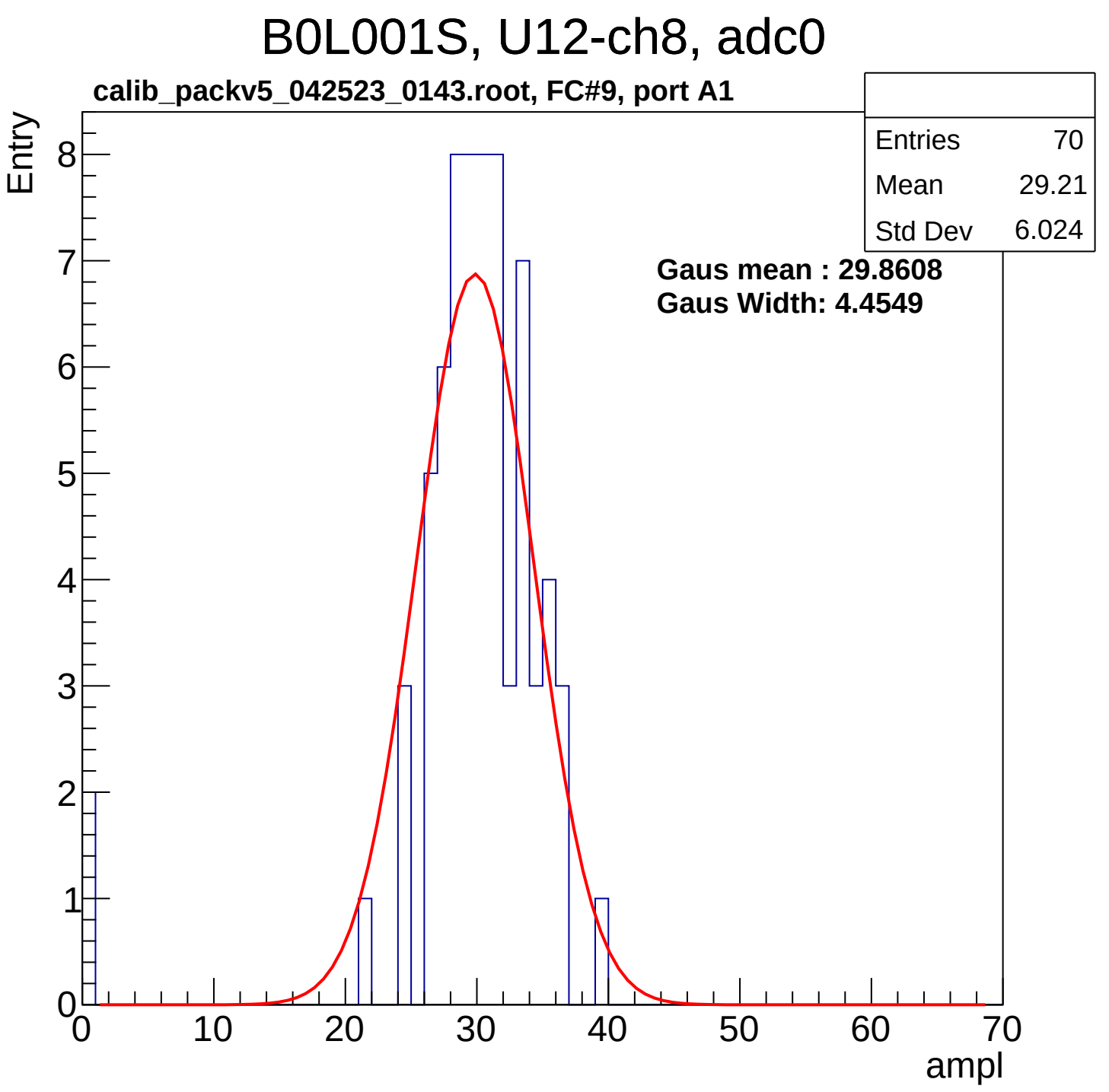
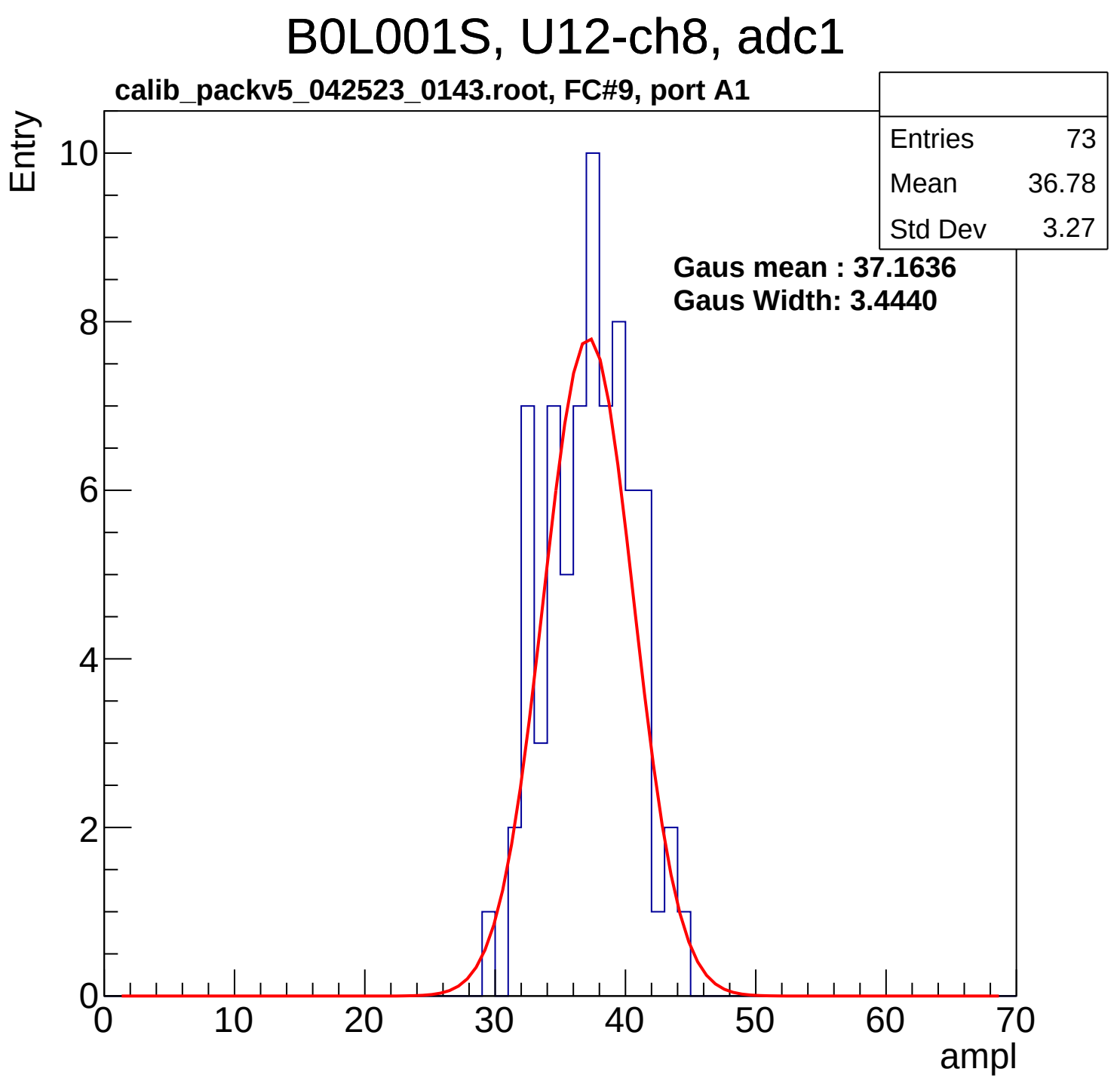
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch8, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 70
Mean 29.21
Std Dev 6.024
Gaus mean : 29.8608
Gaus Width: 4.4549
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch8, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 73
Mean 36.78
Std Dev 3.27
Gaus mean : 37.1636
Gaus Width: 3.4440
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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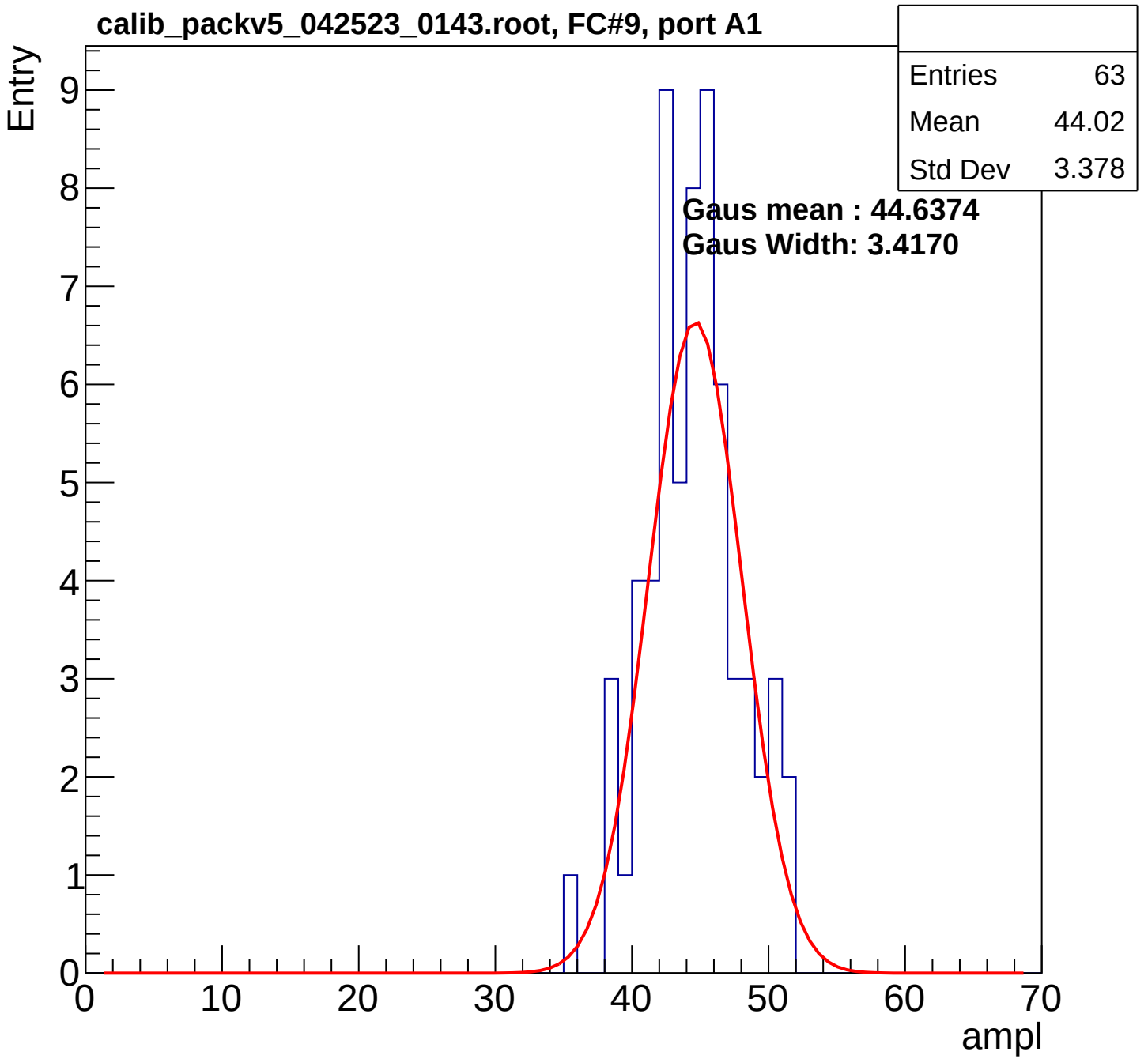
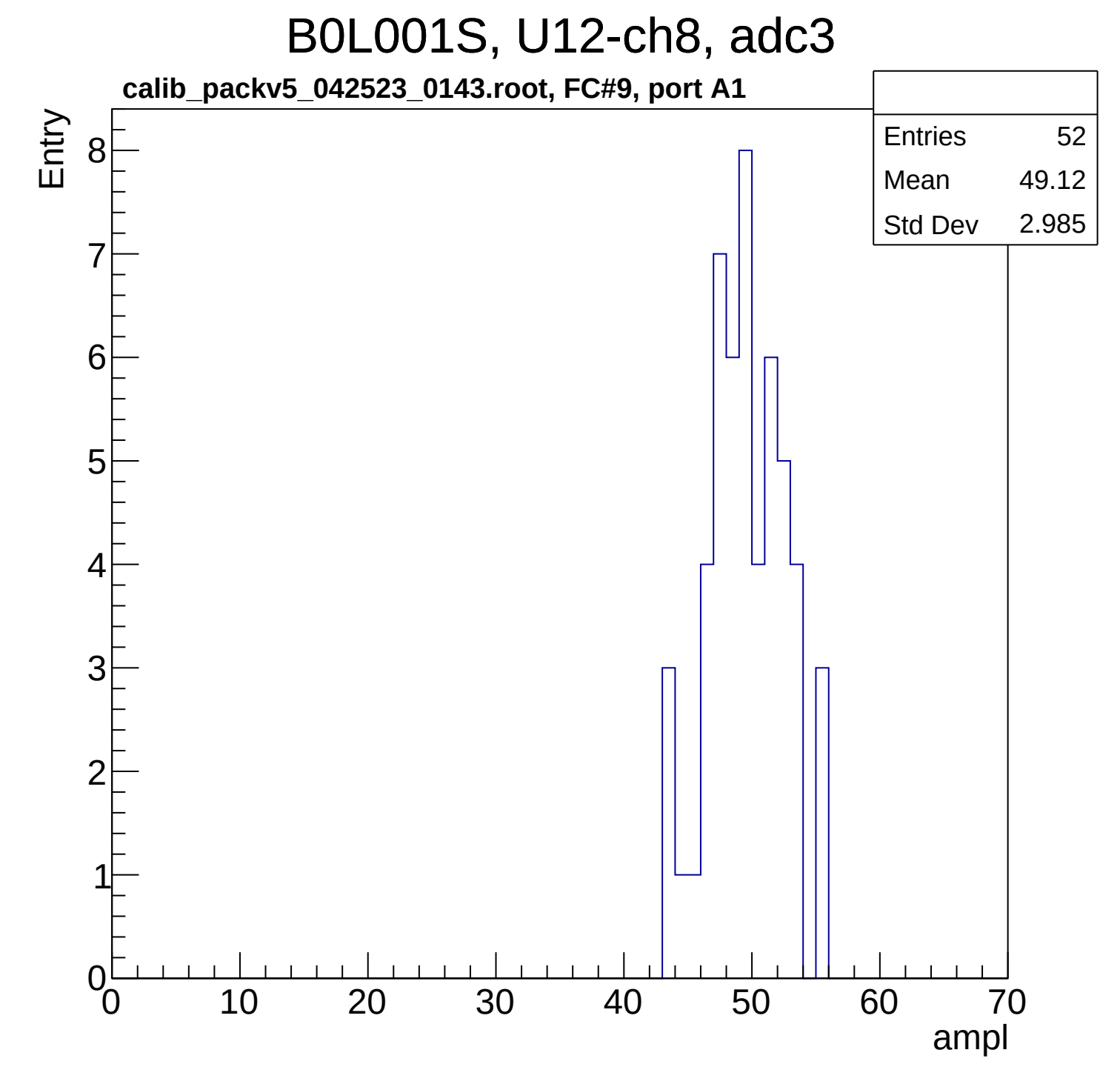

B0L001S, U12-ch8, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 63
Mean 44.02
Std Dev 3.378
Gaus mean : 44.6374
Gaus Width: 3.4170
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch8, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 52
Mean 49.12
Std Dev 2.985
Entry
ampl
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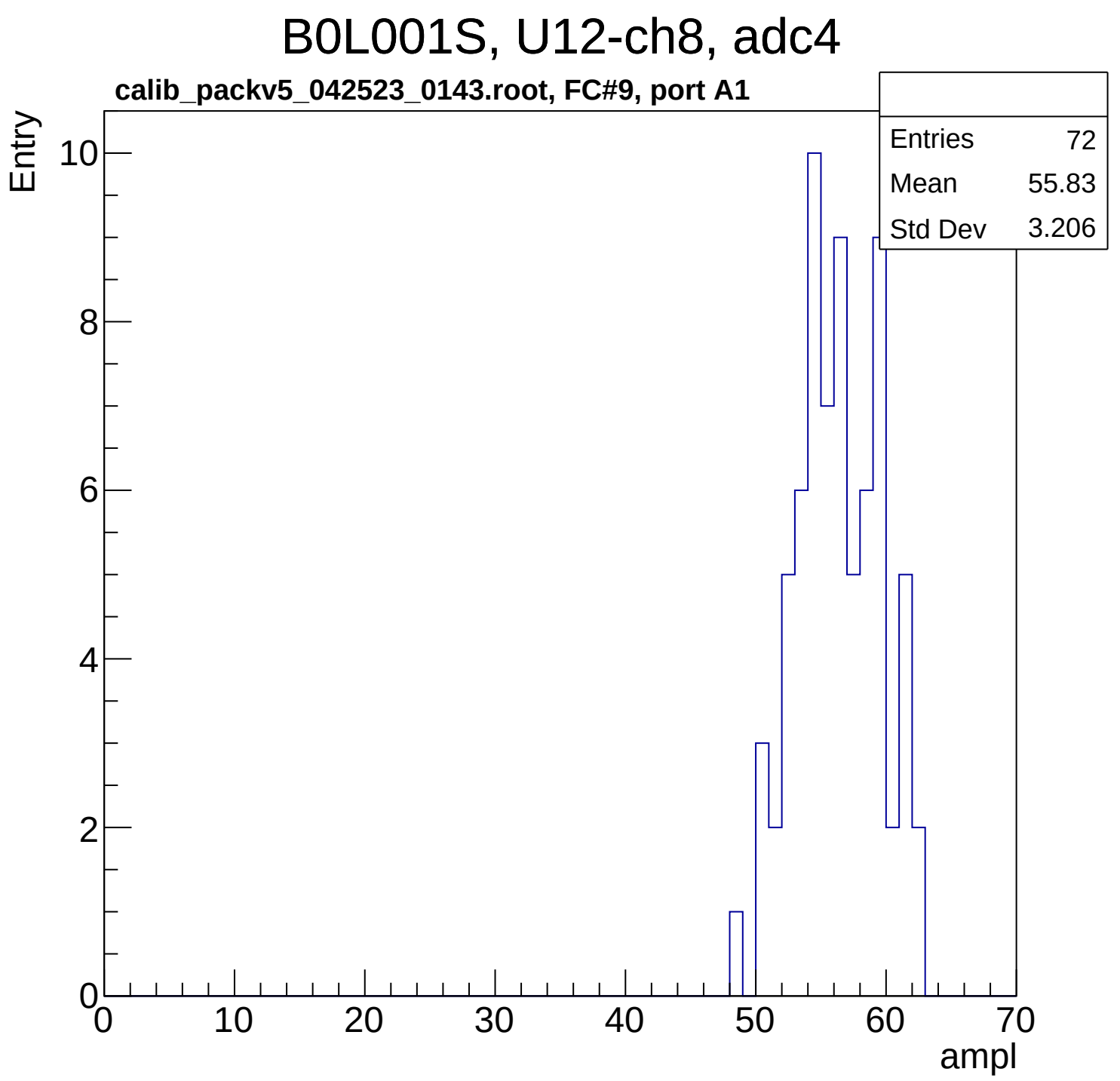
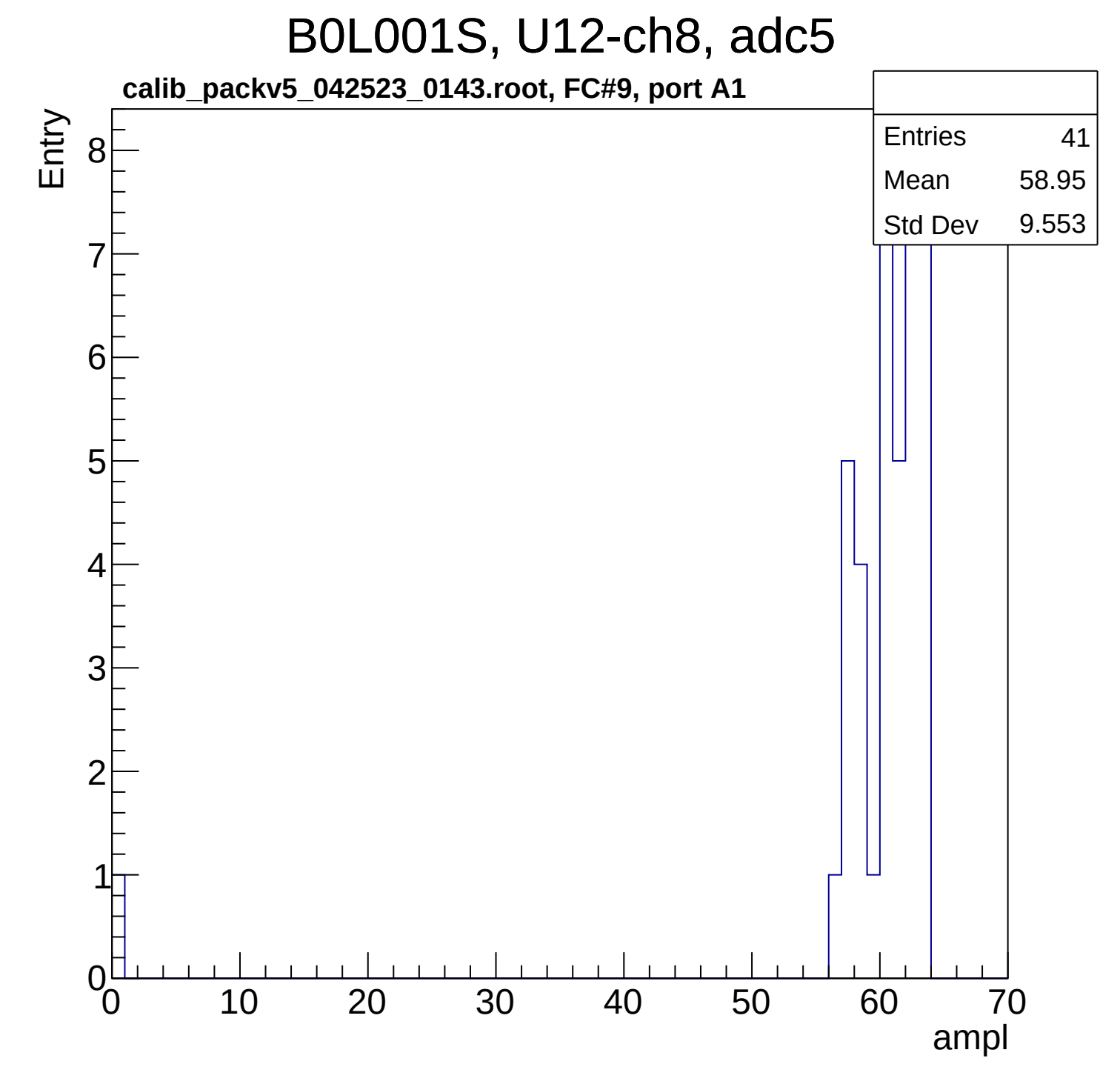
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch8, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 72
Mean 55.83
Std Dev 3.206
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch8, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 41
Mean 58.95
Std Dev 9.553
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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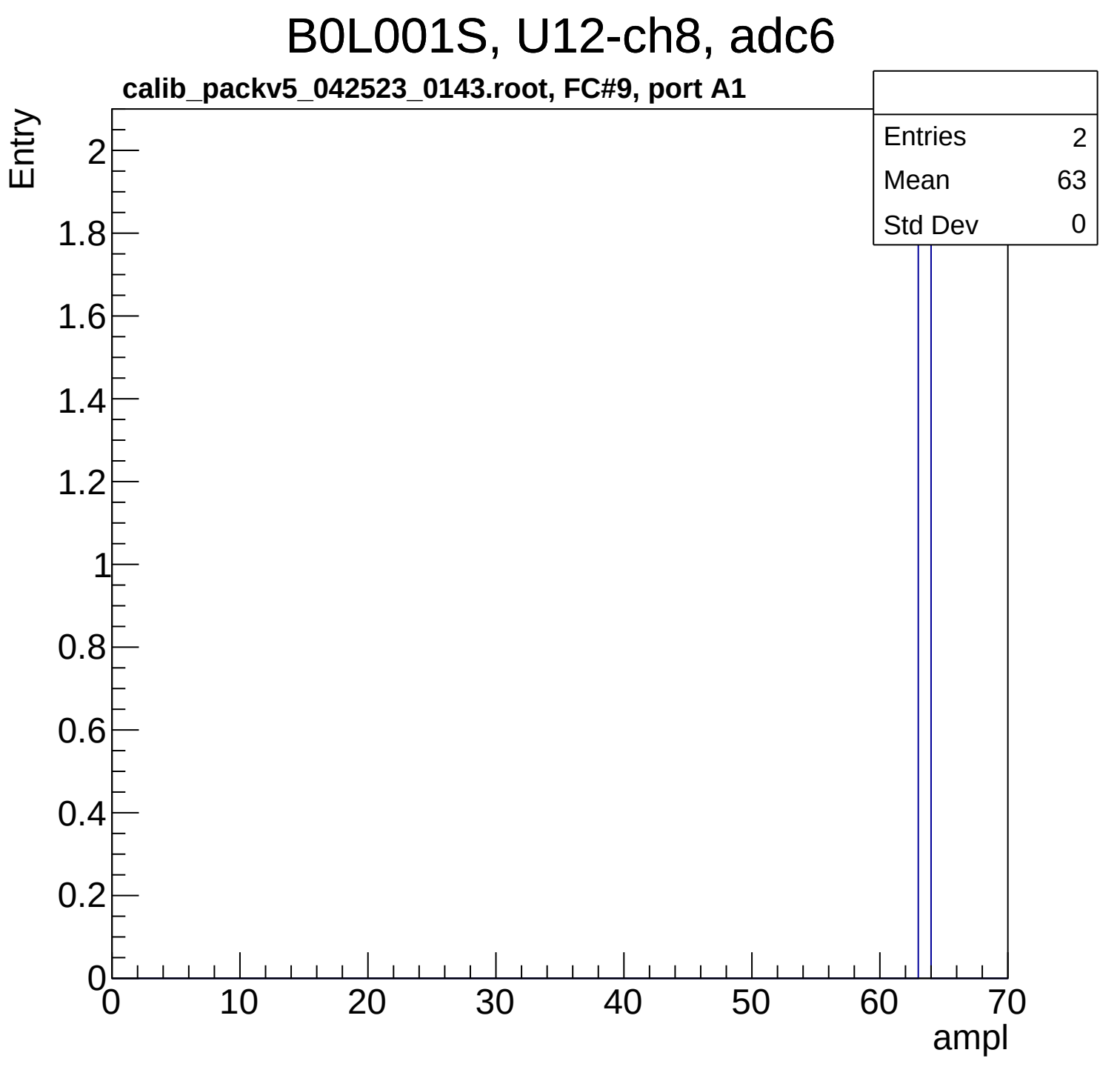
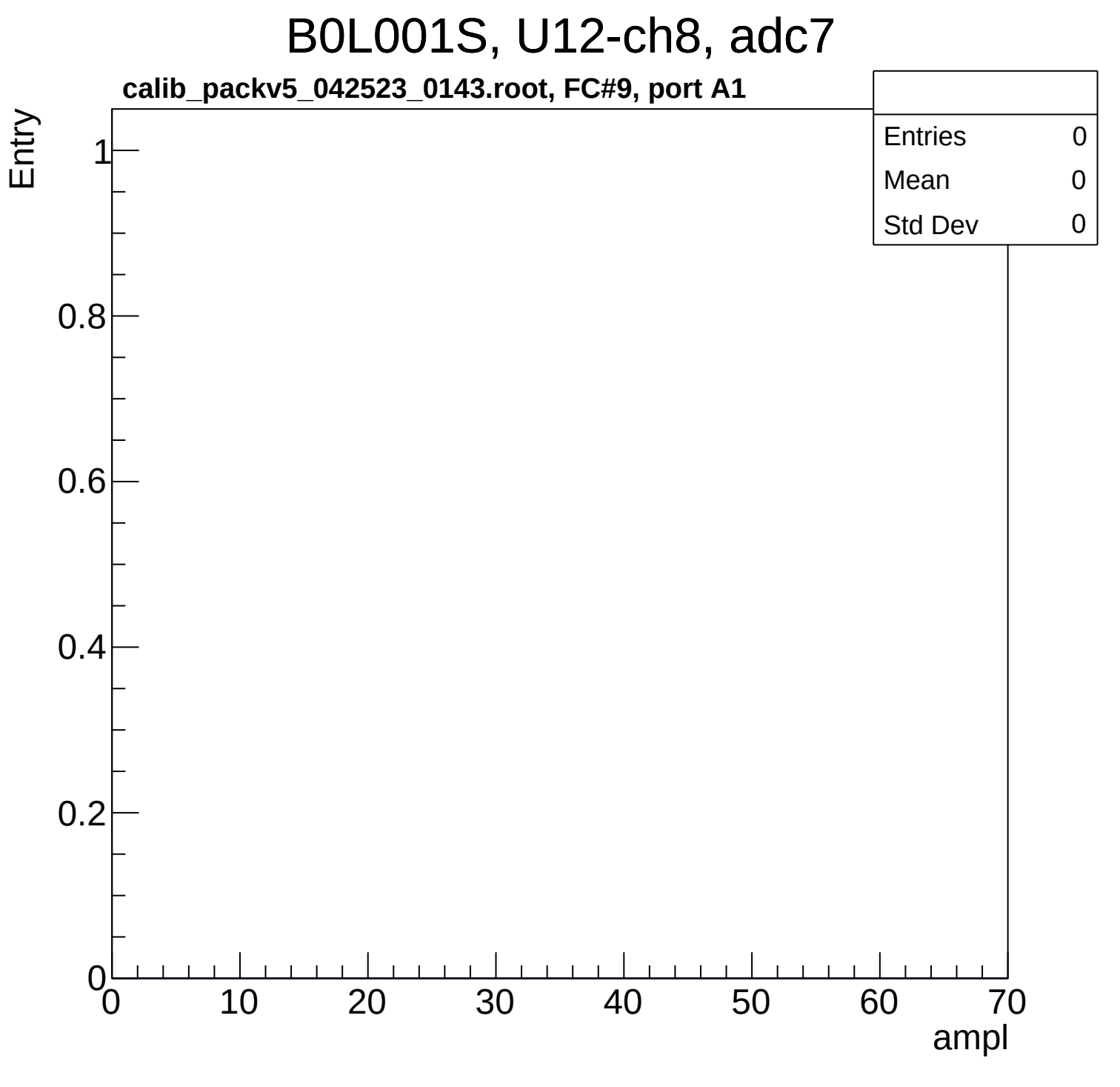

B0L001S, U12-ch8, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L001S, U12-ch8, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
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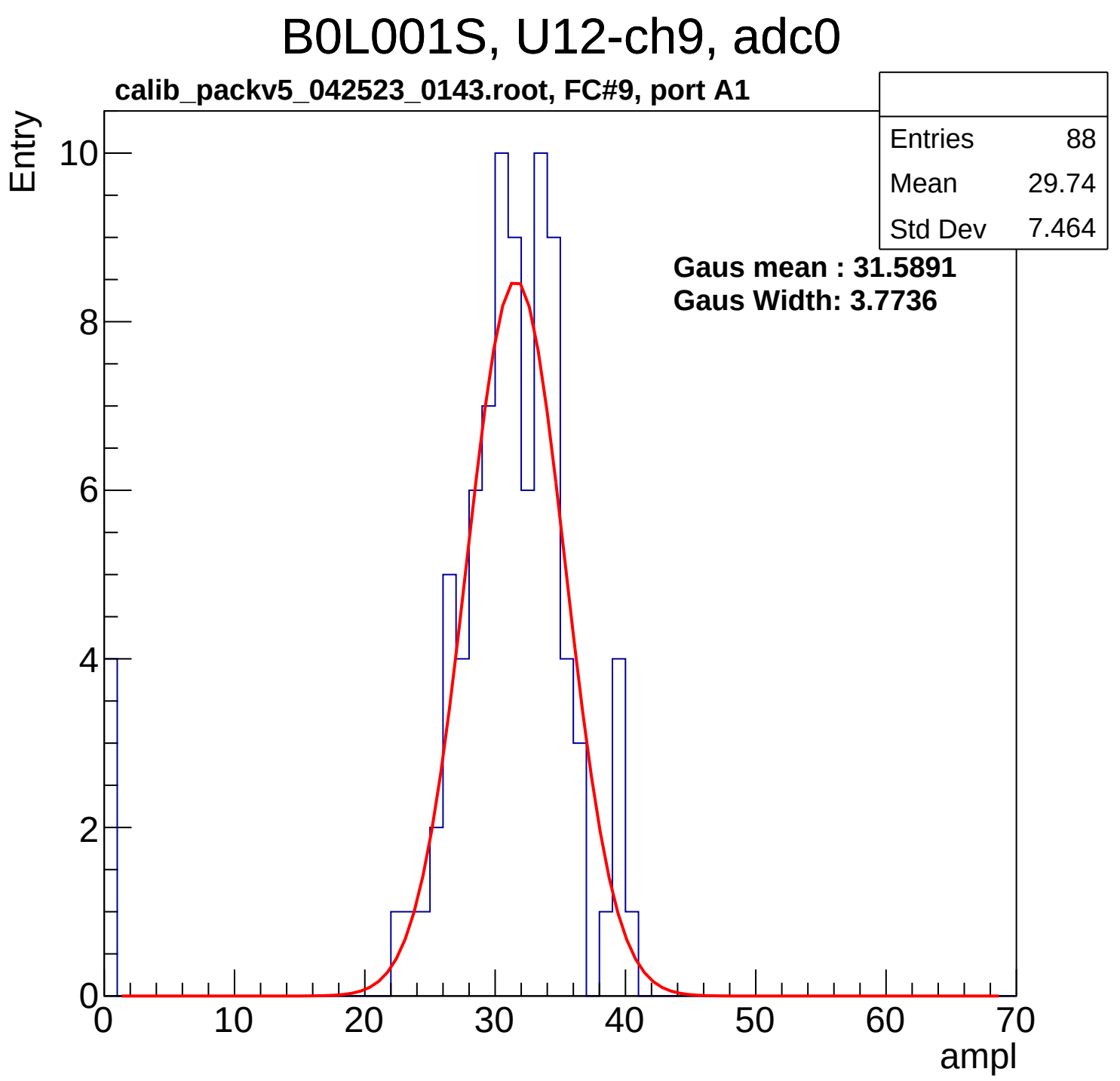
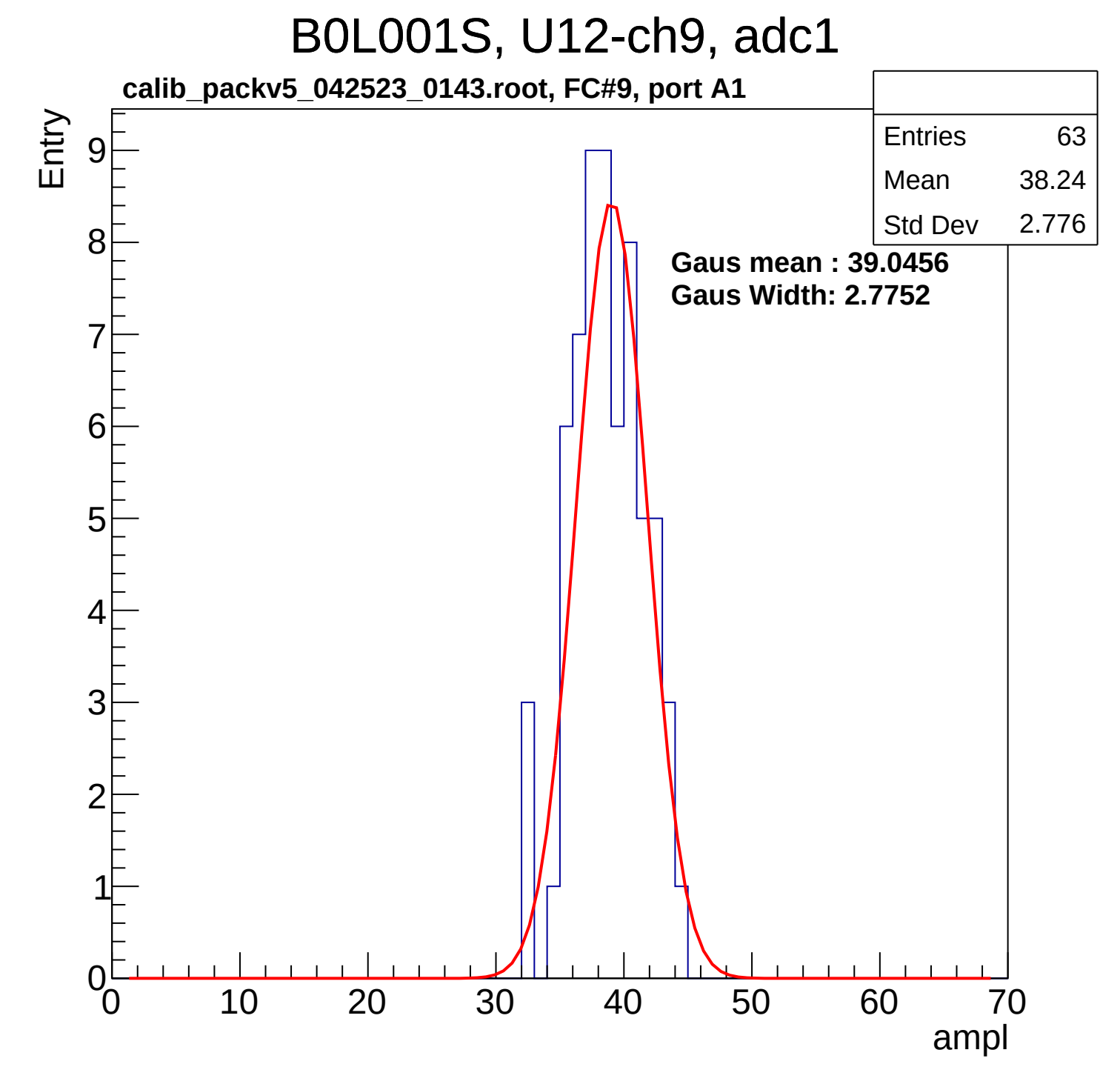
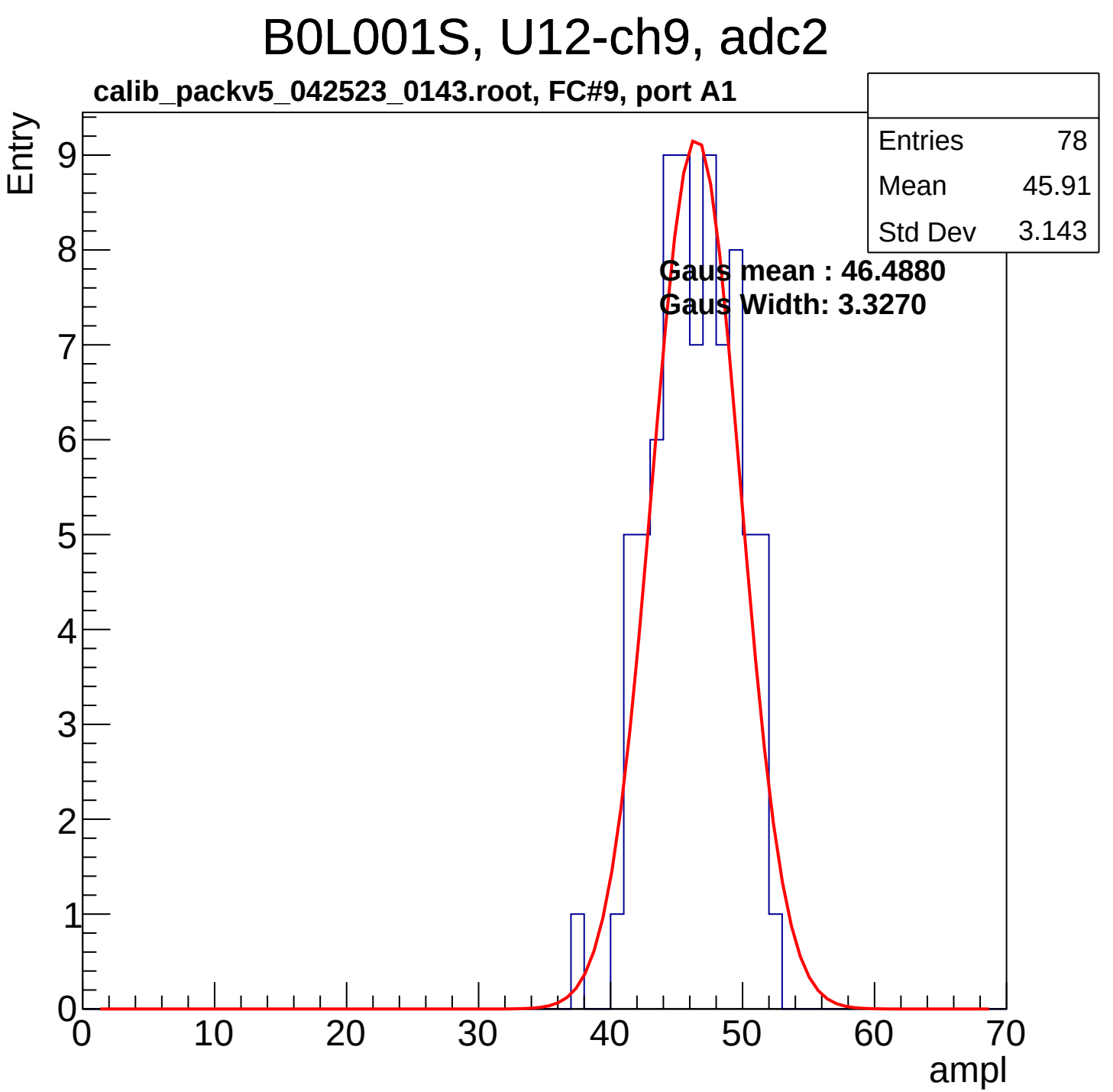
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch9, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 88
Mean 29.74
Std Dev 7.464
Gaus mean : 31.5891
Gaus Width: 3.7736
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch9, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 63
Mean 38.24
Std Dev 2.776
Gaus mean : 39.0456
Gaus Width: 2.7752
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch9, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 78
Mean 45.91
Std Dev 3.143
Gaus mean : 46.4880
Gaus Width: 3.3270
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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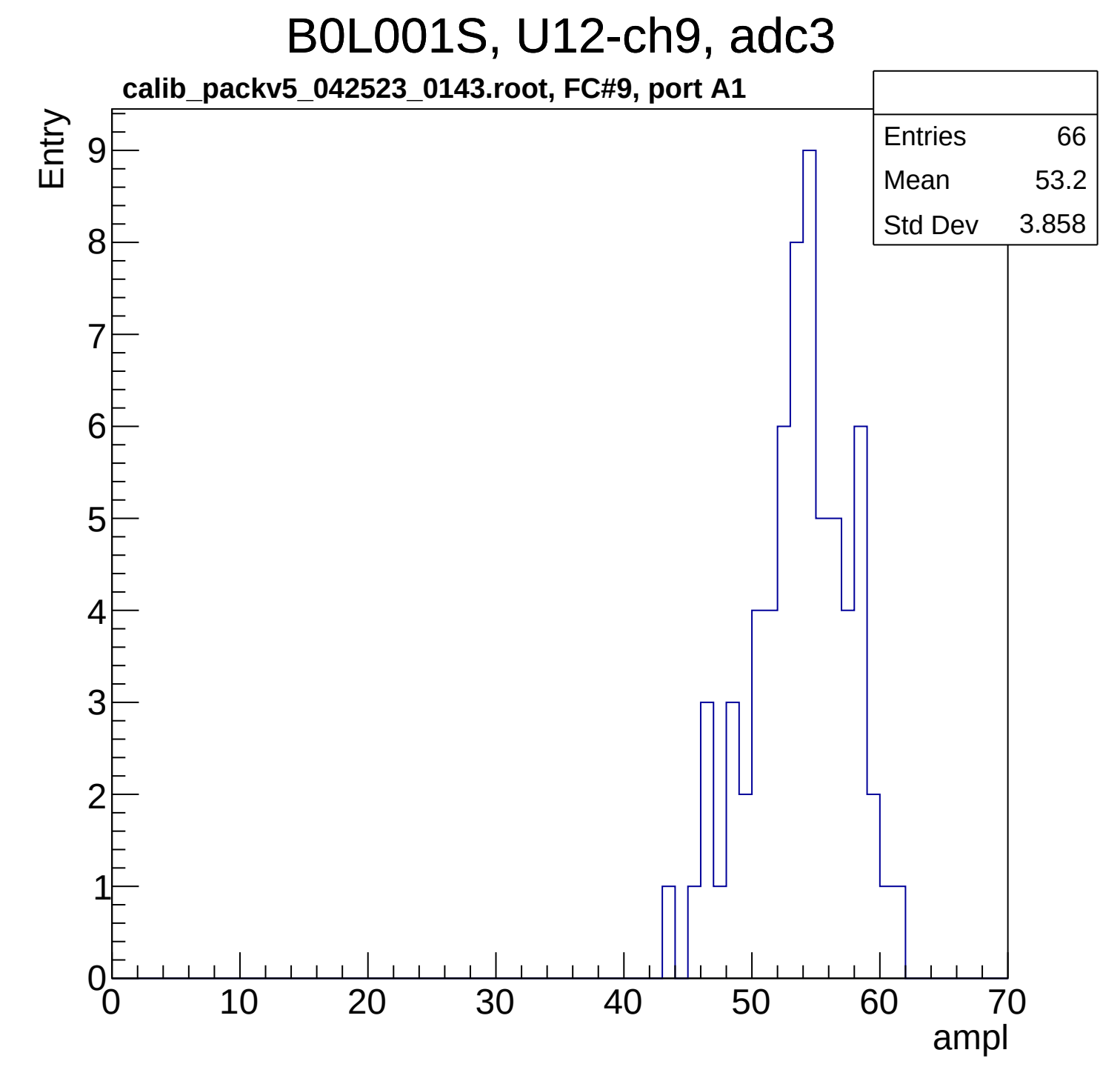
B0L001S, U12-ch9, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 66
Mean 53.2
Std Dev 3.858
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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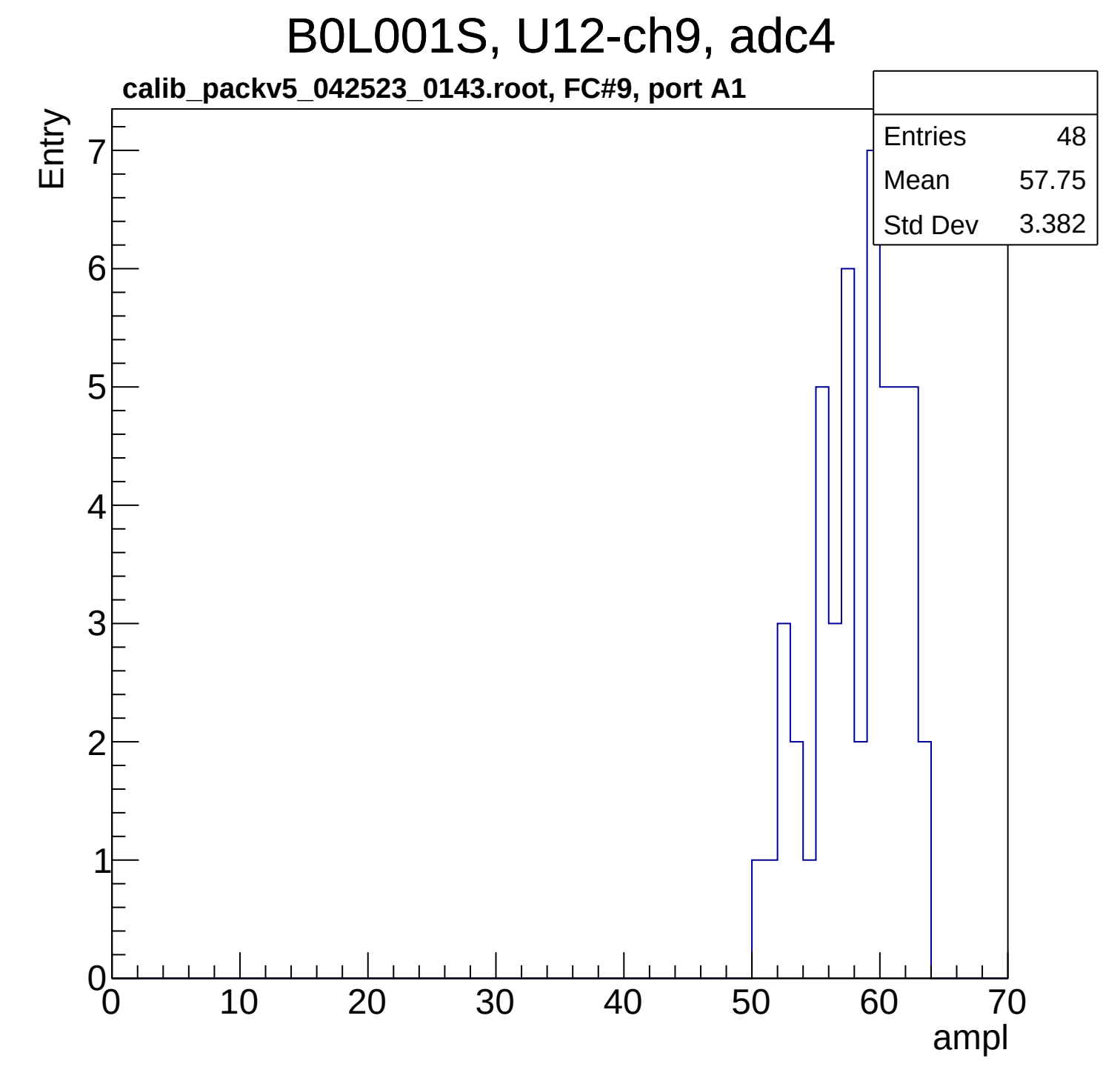
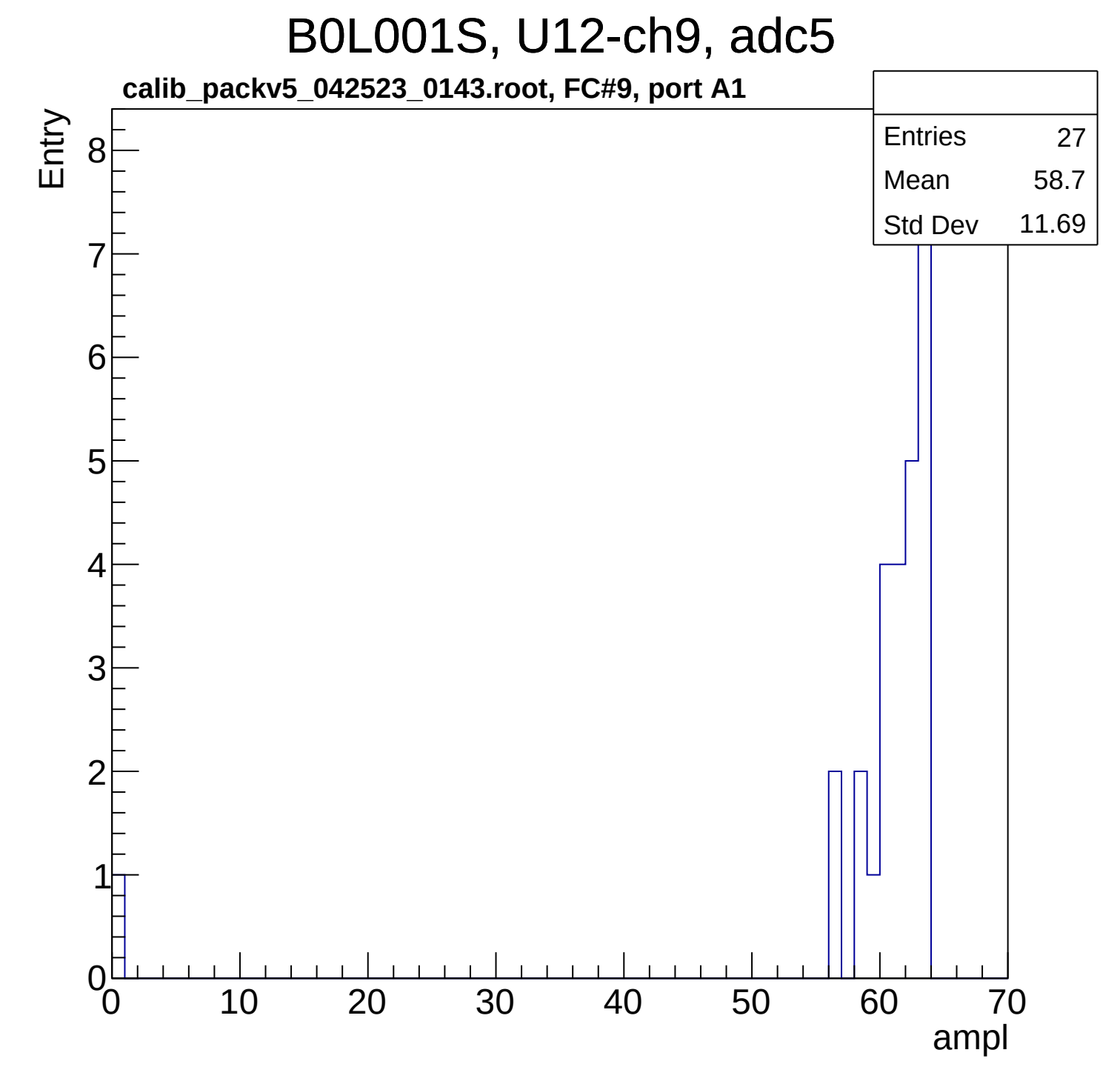

B0L001S, U12-ch9, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 48
Mean 57.75
Std Dev 3.382
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B0L001S, U12-ch9, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 27
Mean 58.7
Std Dev 11.69
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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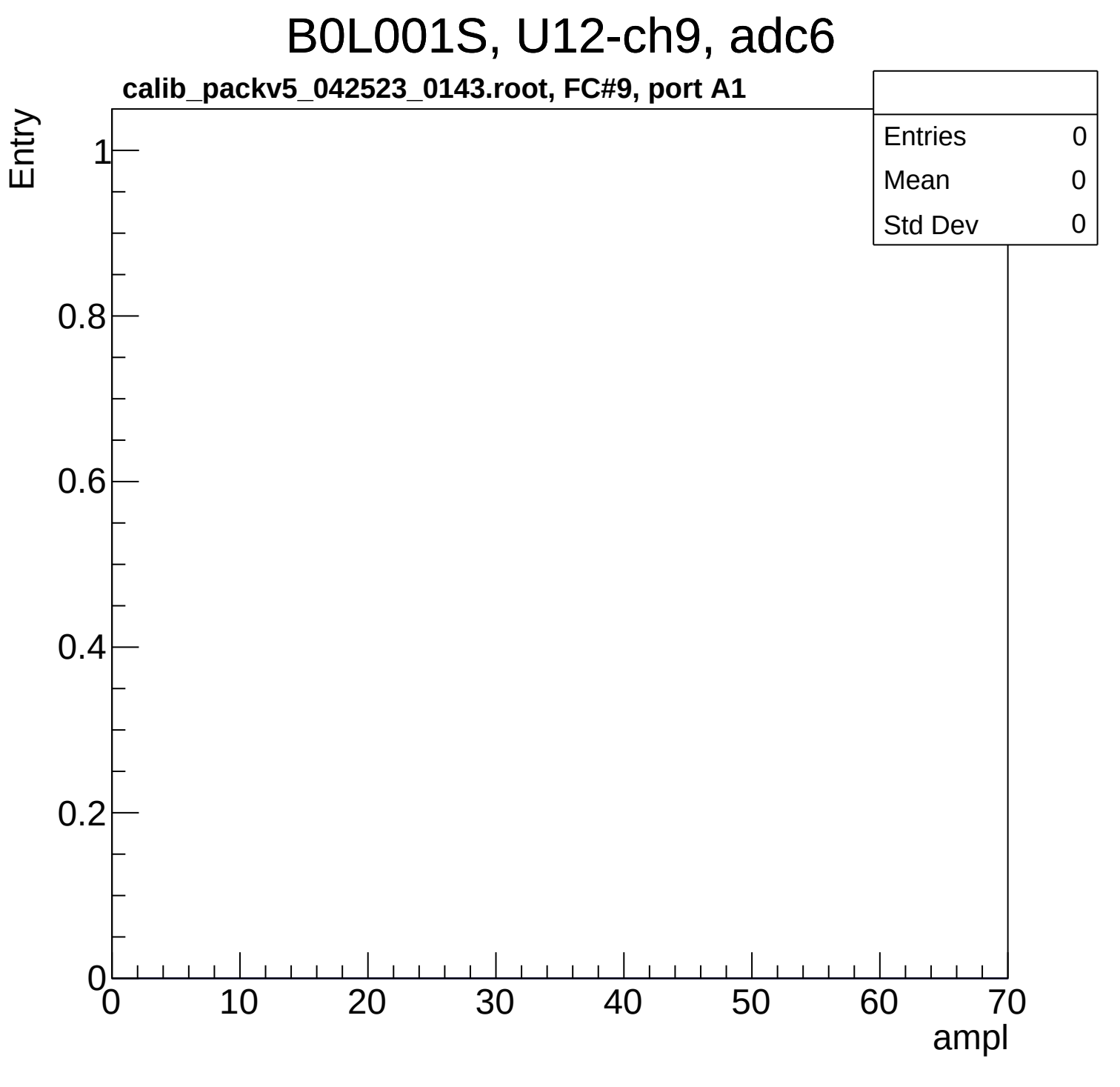
B0L001S, U12-ch9, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
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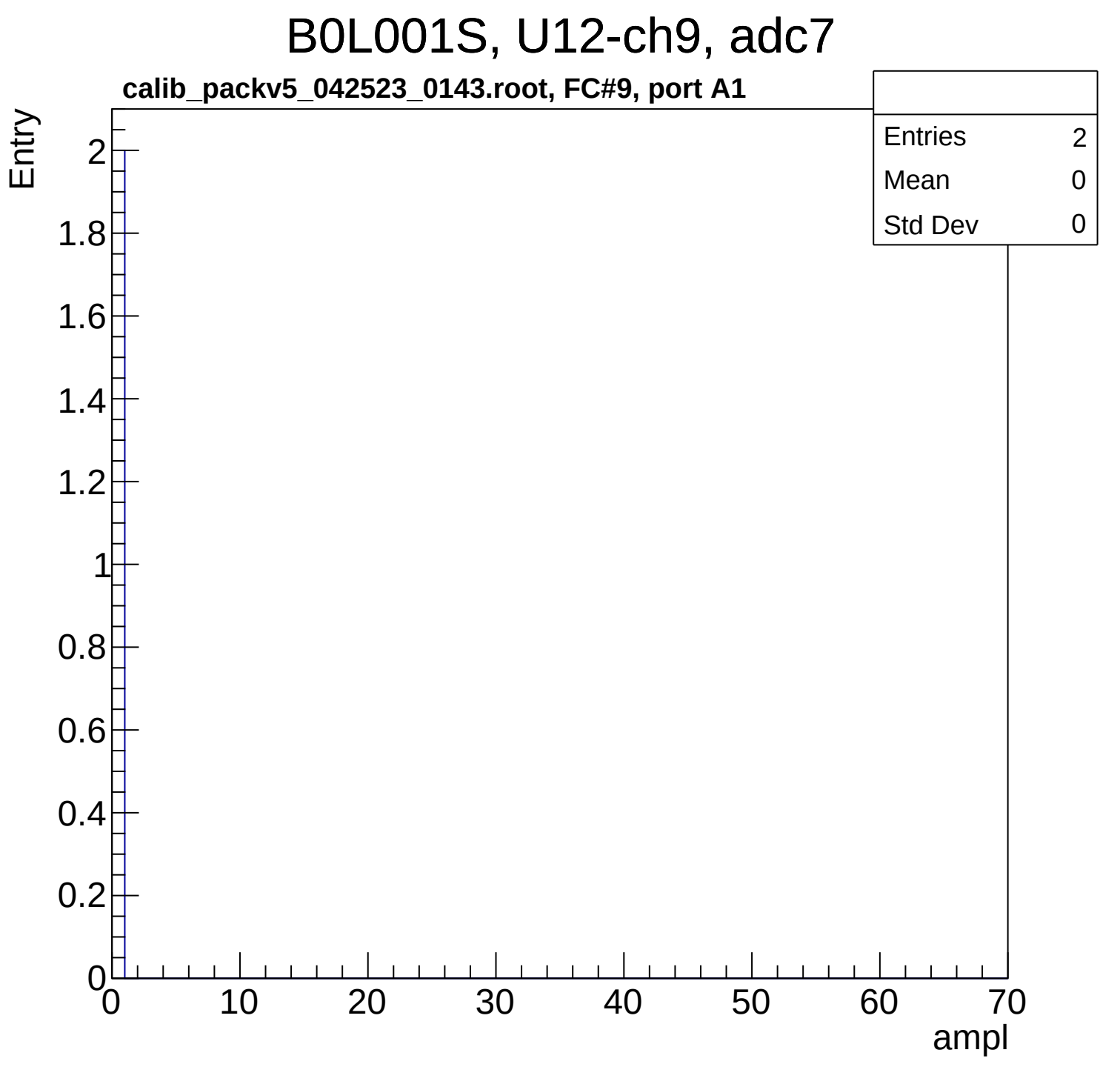
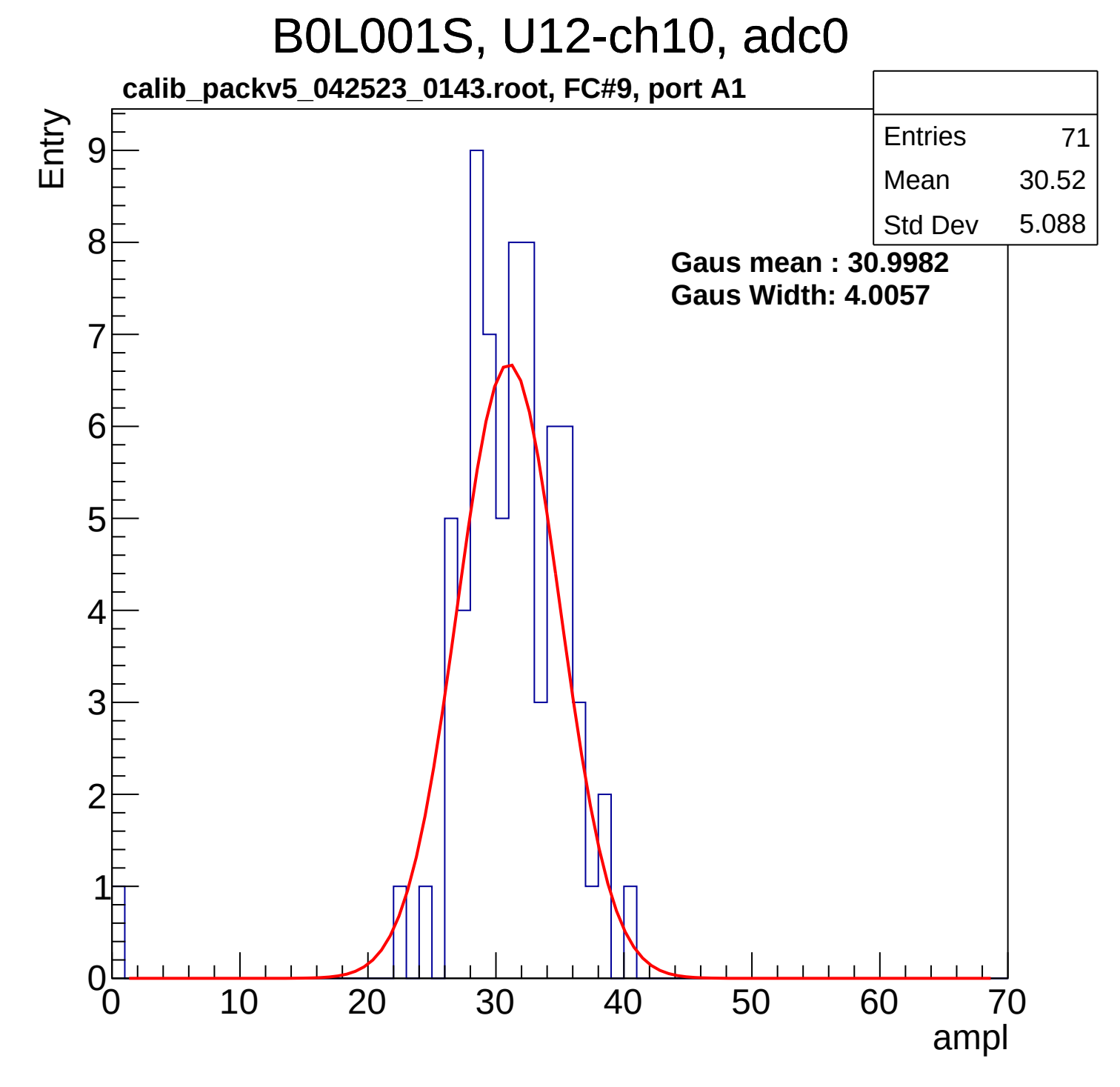
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch9, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch10, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 71
Mean 30.52
Std Dev 5.088
Gaus mean : 30.9982
Gaus Width: 4.0057
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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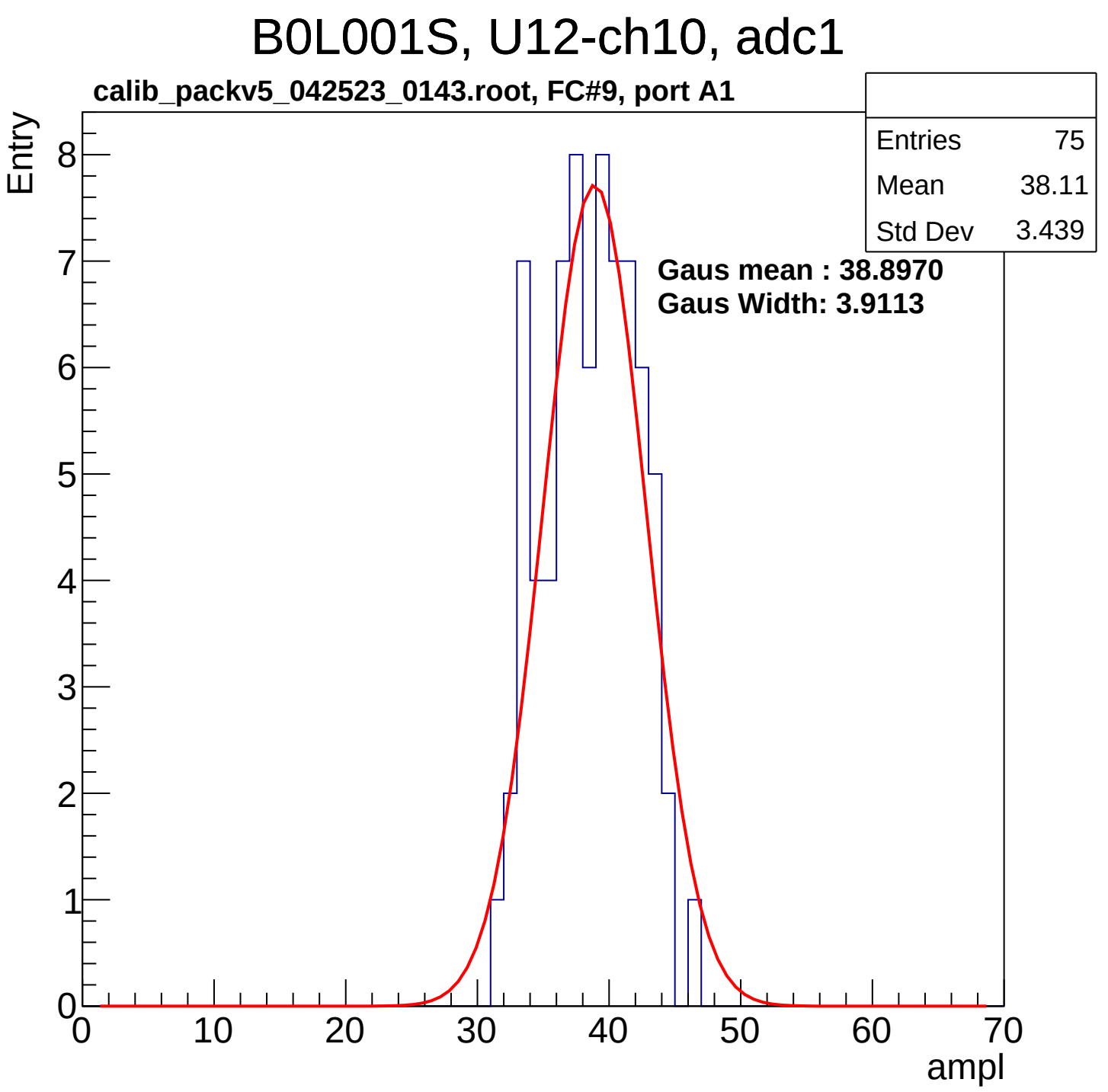
B0L001S, U12-ch10, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 75
Mean 38.11
Std Dev 3.439
Gaus mean : 38.8970
Gaus Width: 3.9113
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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40
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60
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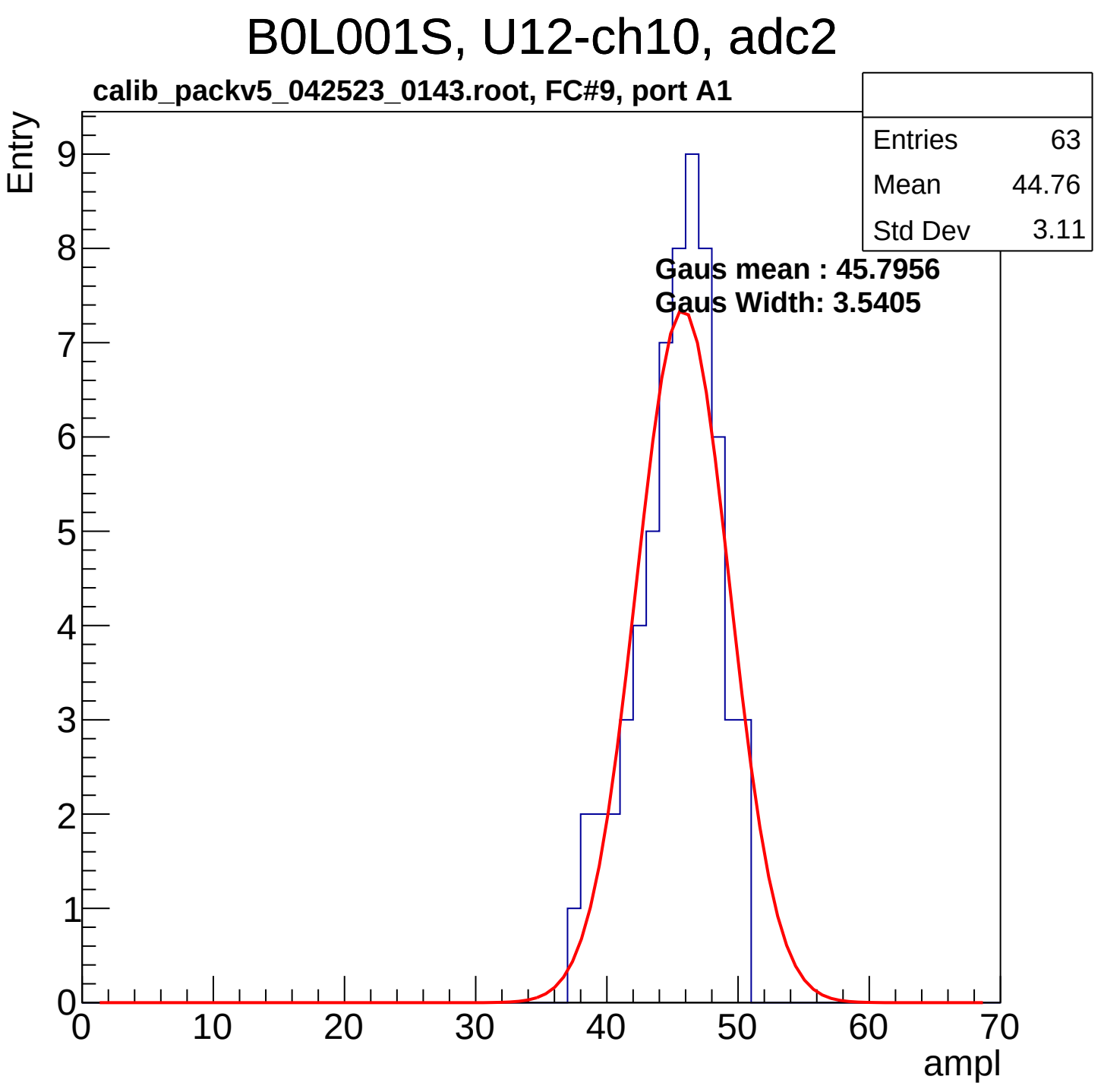
B0L001S, U12-ch10, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 63
Mean 44.76
Std Dev 3.11
Gaus mean : 45.7956
Gaus Width: 3.5405
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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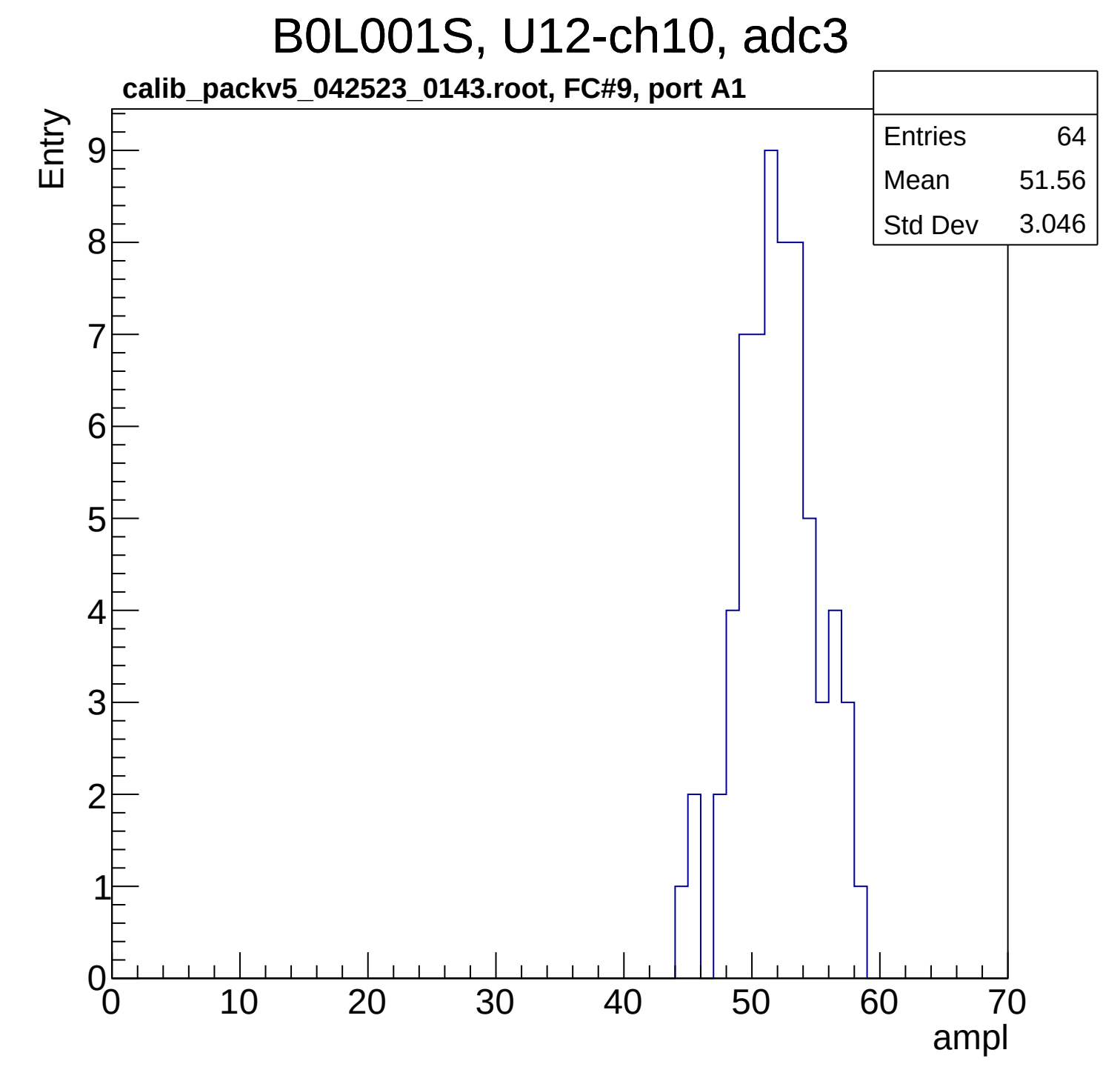
B0L001S, U12-ch10, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 64
Mean 51.56
Std Dev 3.046
Entry
ampl
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2
3
4
5
6
7
8
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0
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20
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40
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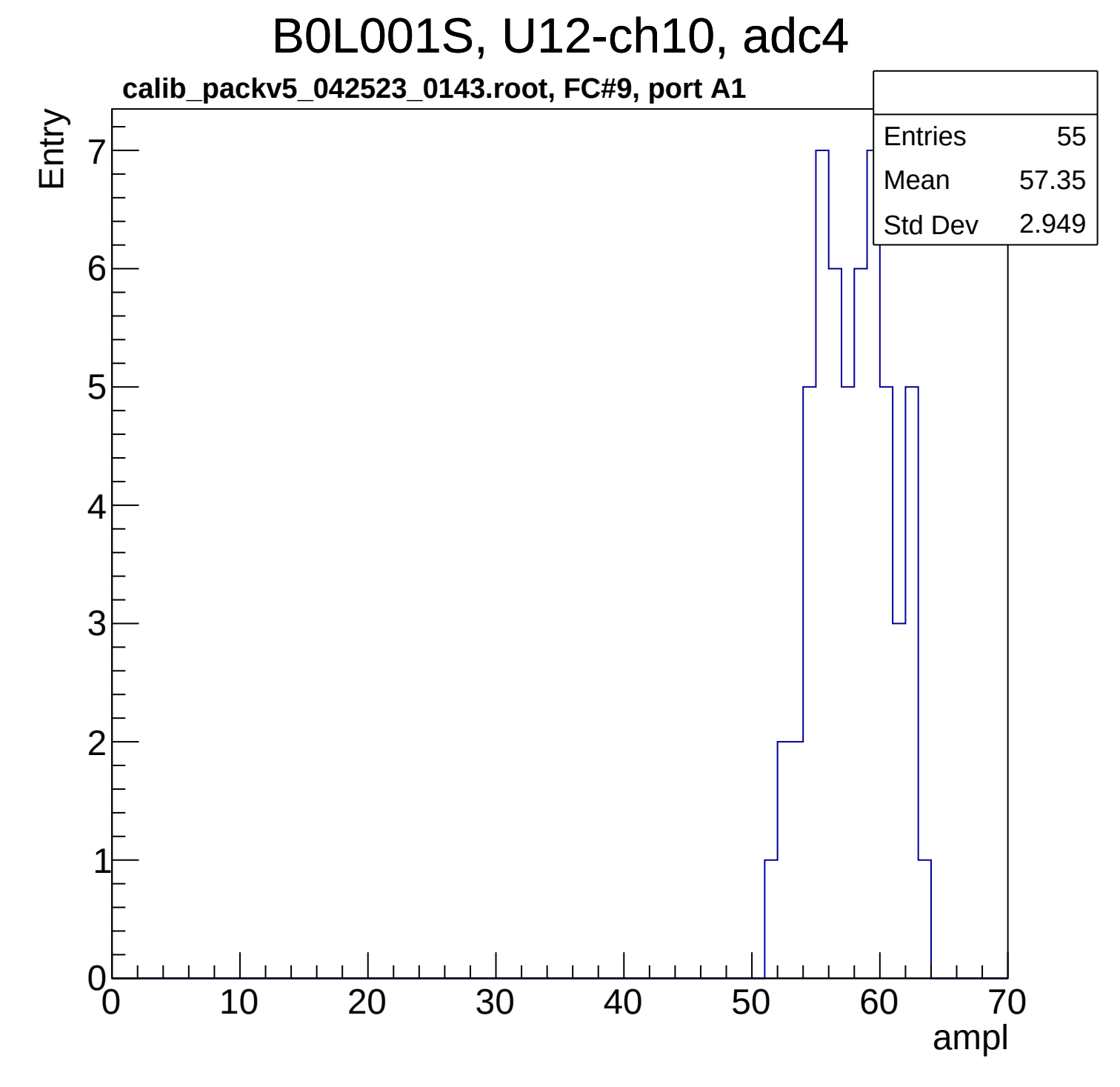
B0L001S, U12-ch10, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 55
Mean 57.35
Std Dev 2.949
Entry
ampl
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2
3
4
5
6
7
0
10
20
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40
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60
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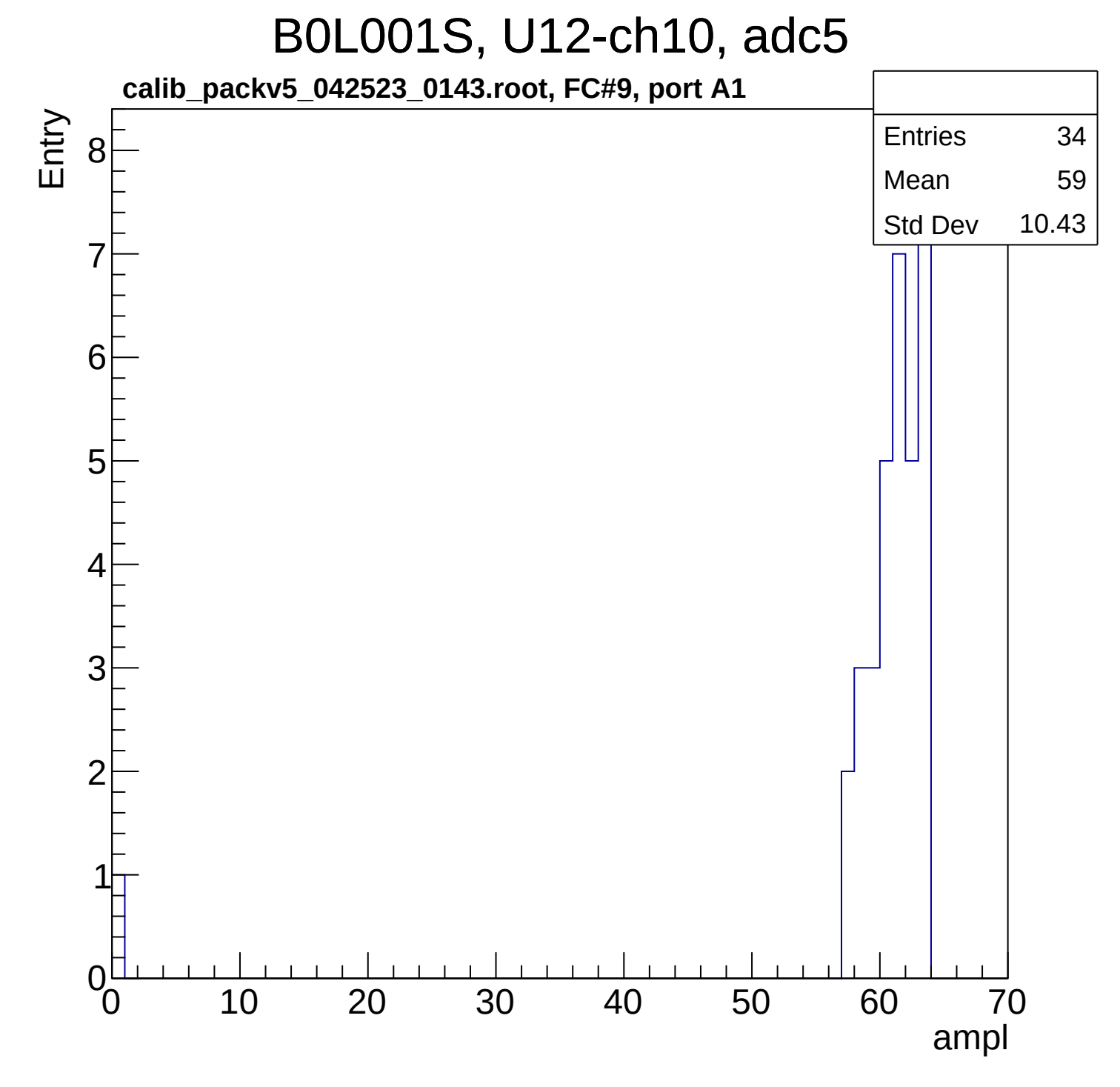
B0L001S, U12-ch10, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 34
Mean 59
Std Dev 10.43
Entry
ampl
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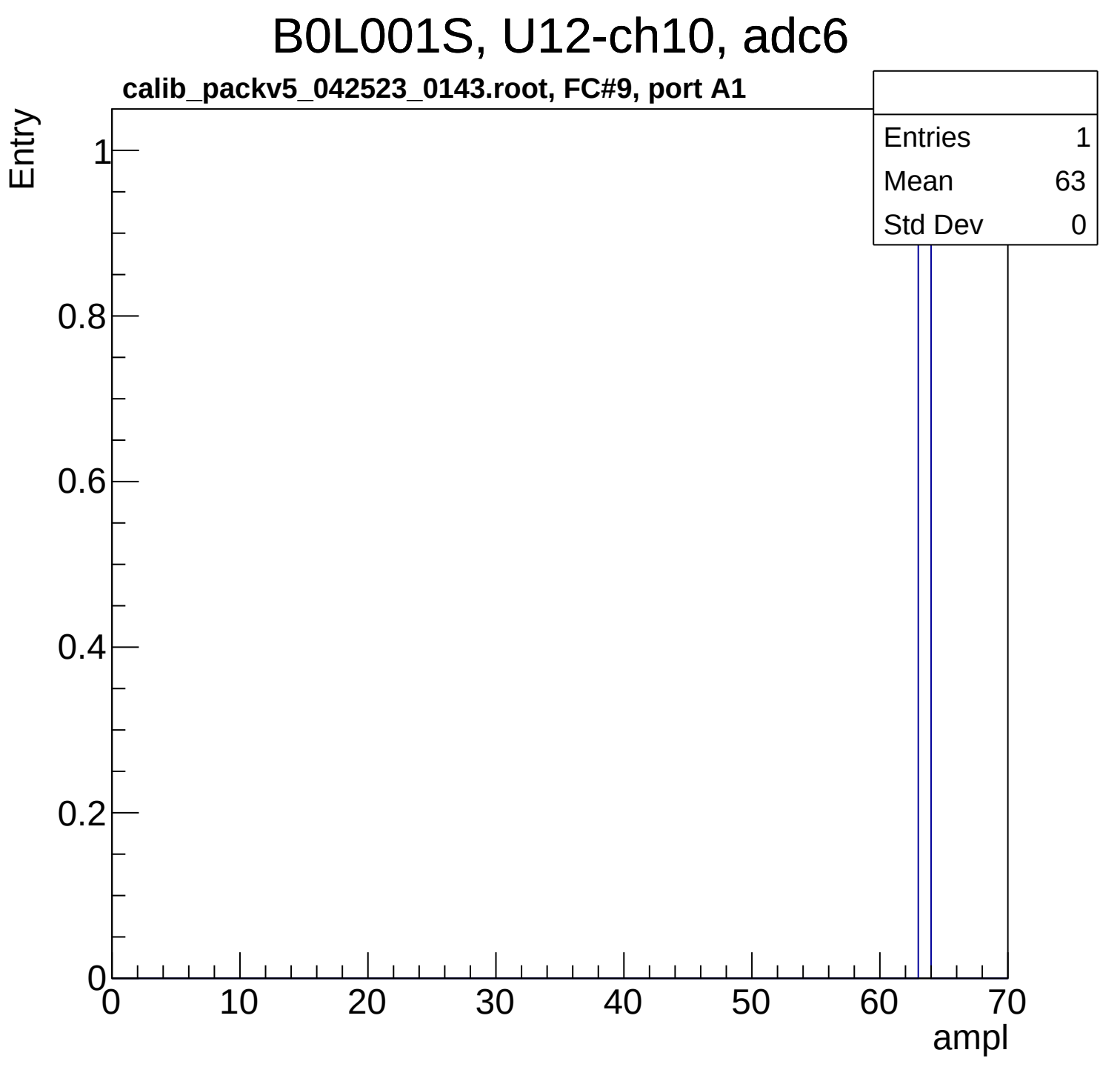
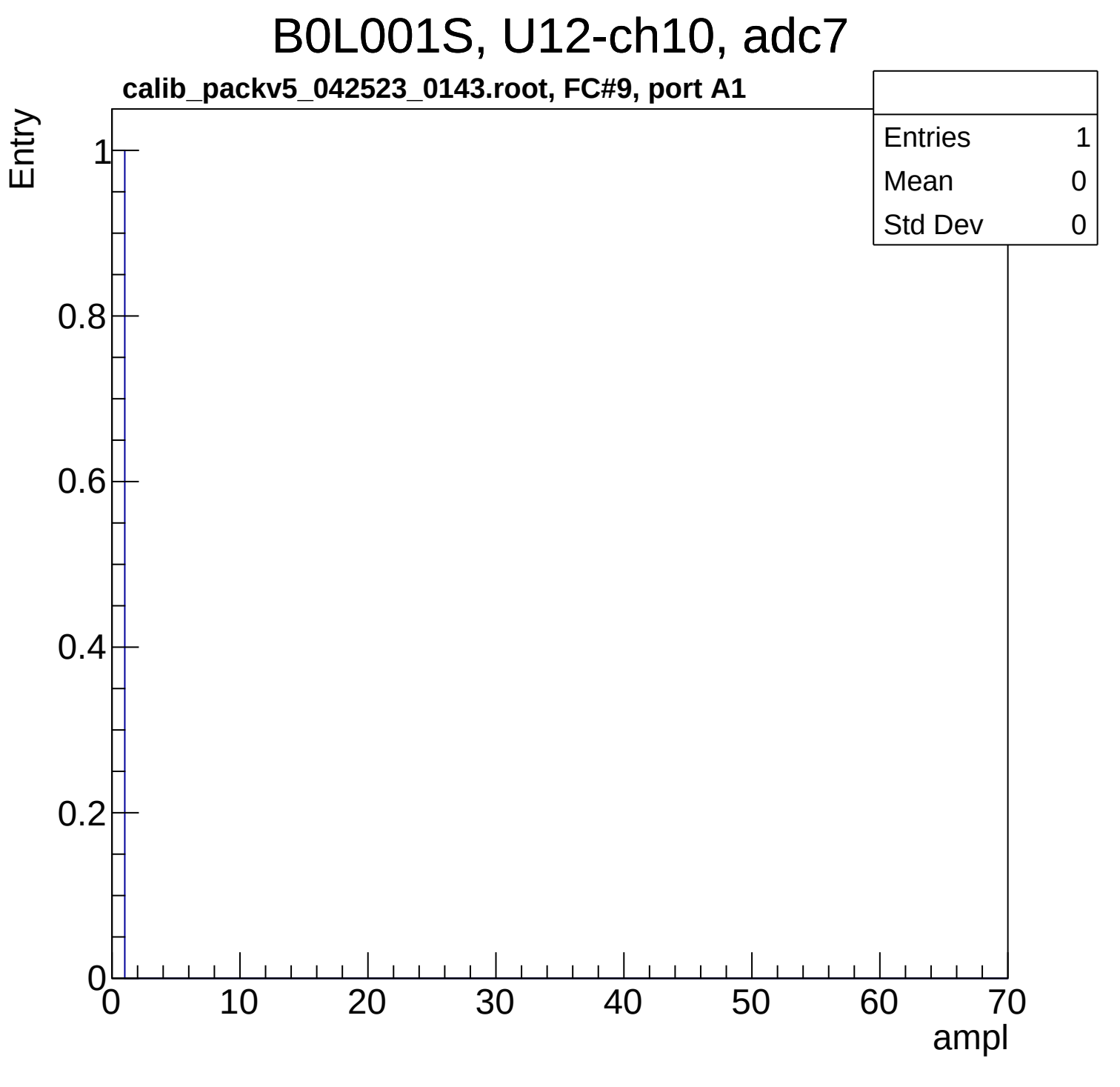
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch10, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch10, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 0
Std Dev 0
Entry
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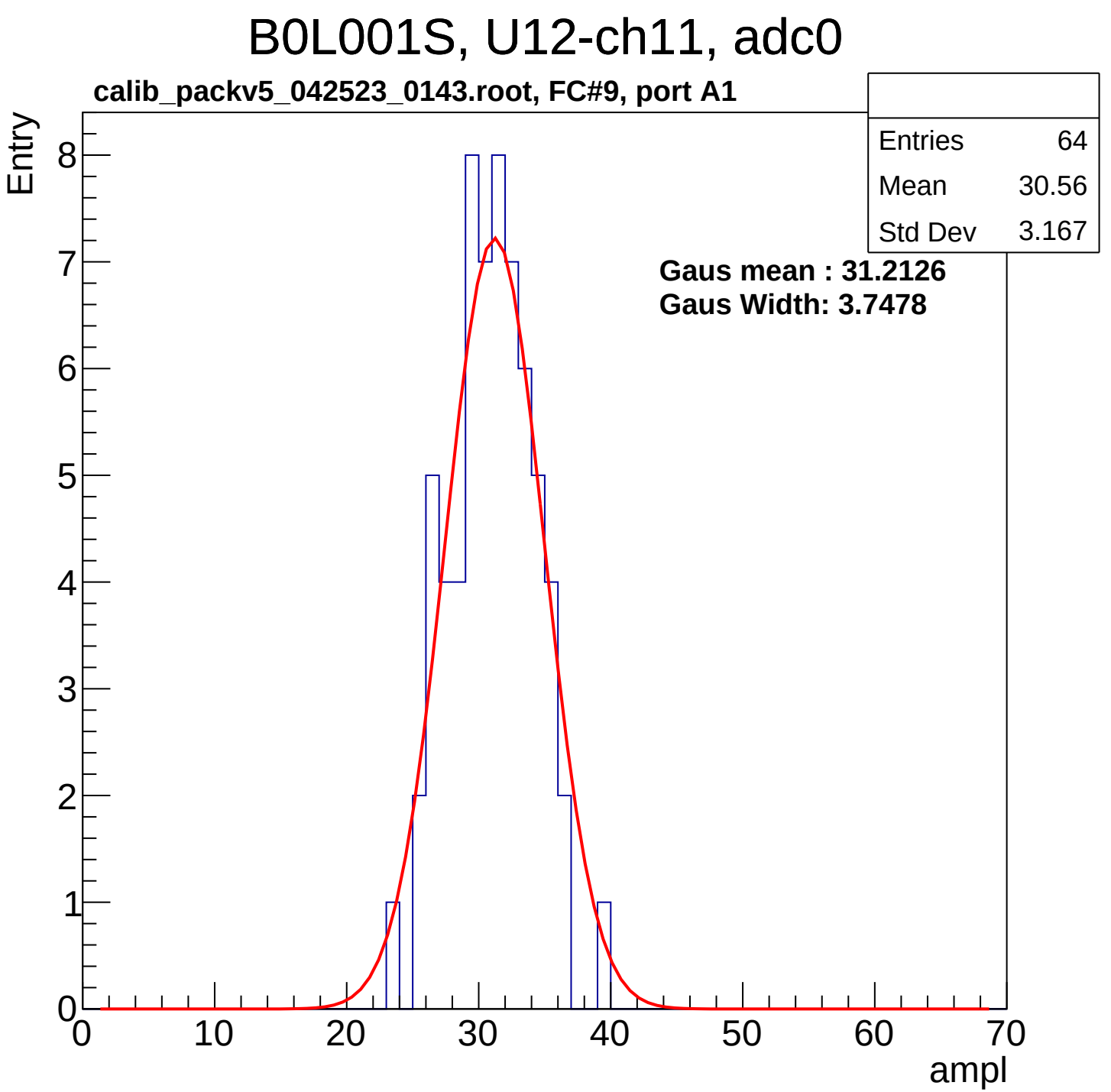
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch11, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 64
Mean 30.56
Std Dev 3.167
Gaus mean : 31.2126
Gaus Width: 3.7478
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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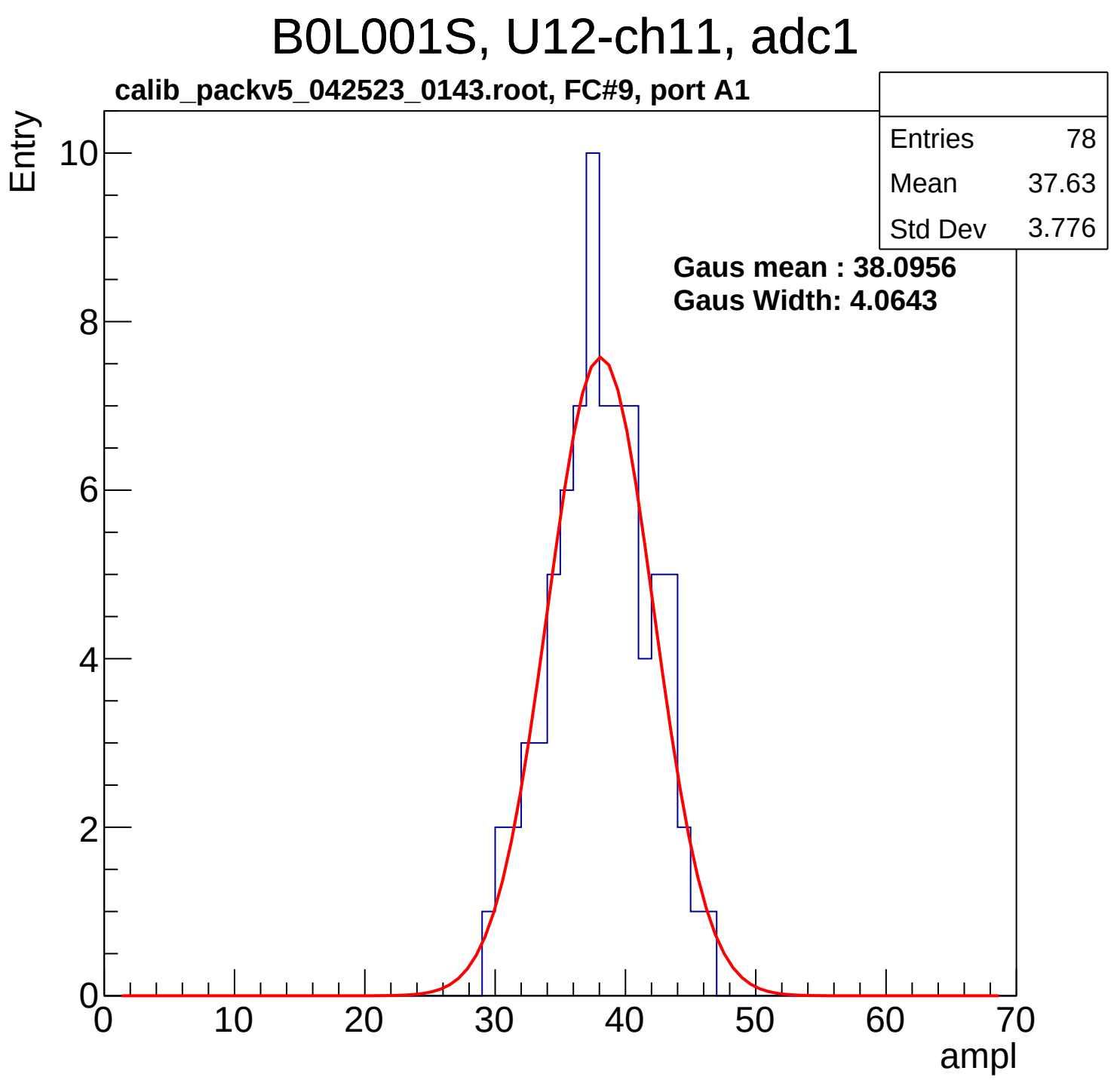
B0L001S, U12-ch11, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 78
Mean 37.63
Std Dev 3.776
Gaus mean : 38.0956
Gaus Width: 4.0643
Entry
ampl
0
2
4
6
8
10
0
10
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40
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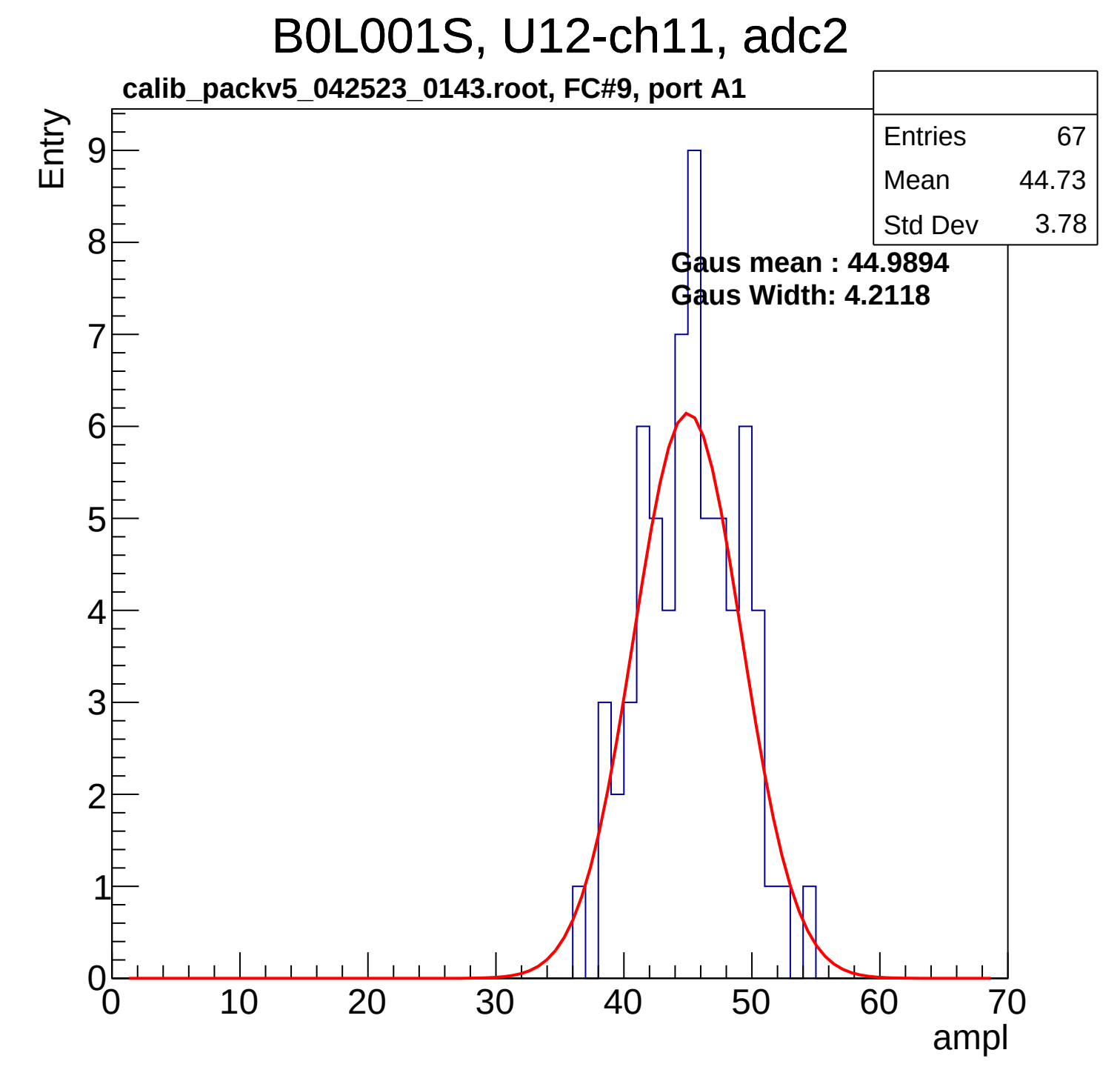
B0L001S, U12-ch11, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 67
Mean 44.73
Std Dev 3.78
Gaus mean : 44.9894
Gaus Width: 4.2118
Entry
ampl
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2
3
4
5
6
7
8
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0
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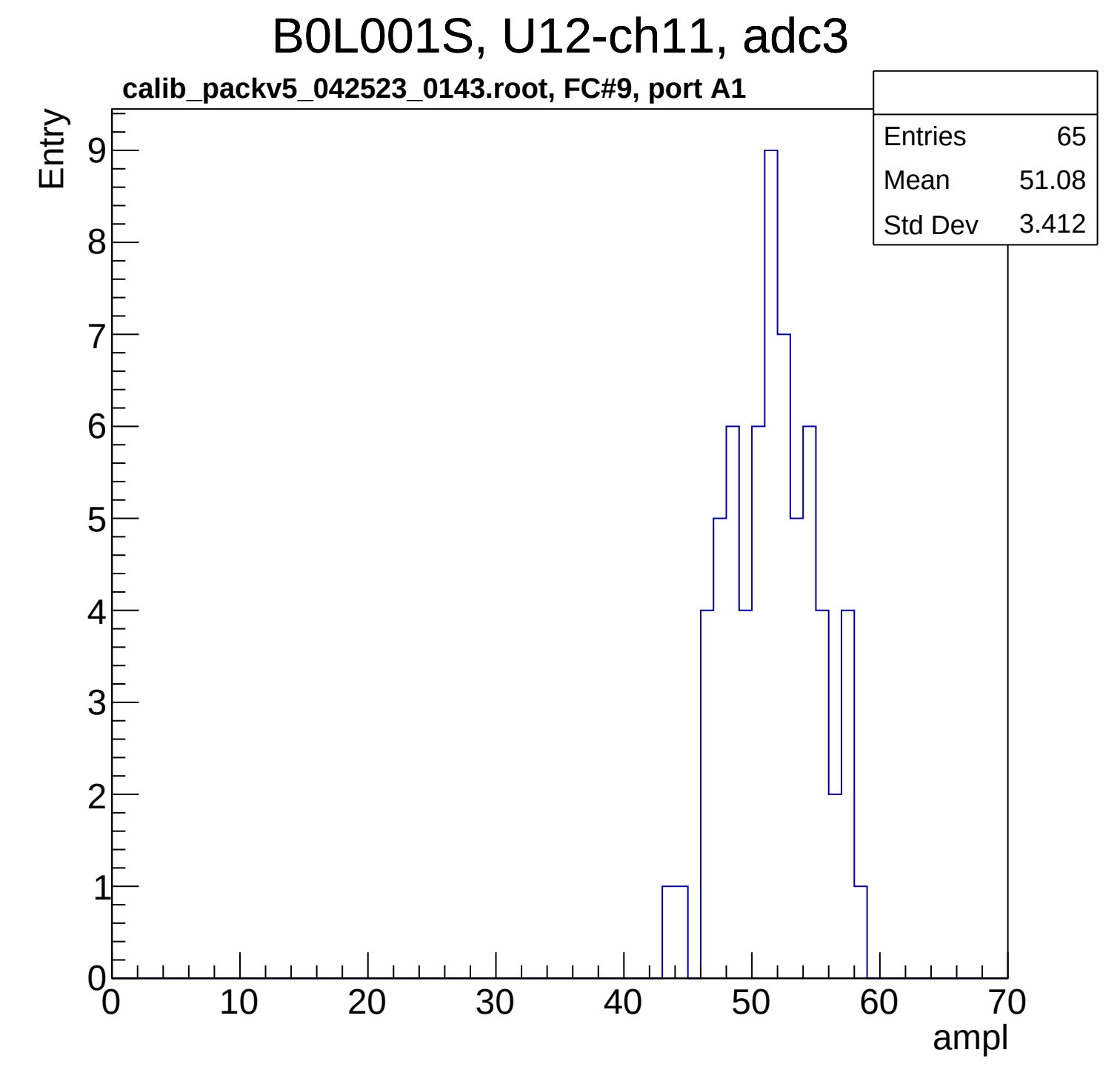
B0L001S, U12-ch11, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 65
Mean 51.08
Std Dev 3.412
Entry
ampl
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0
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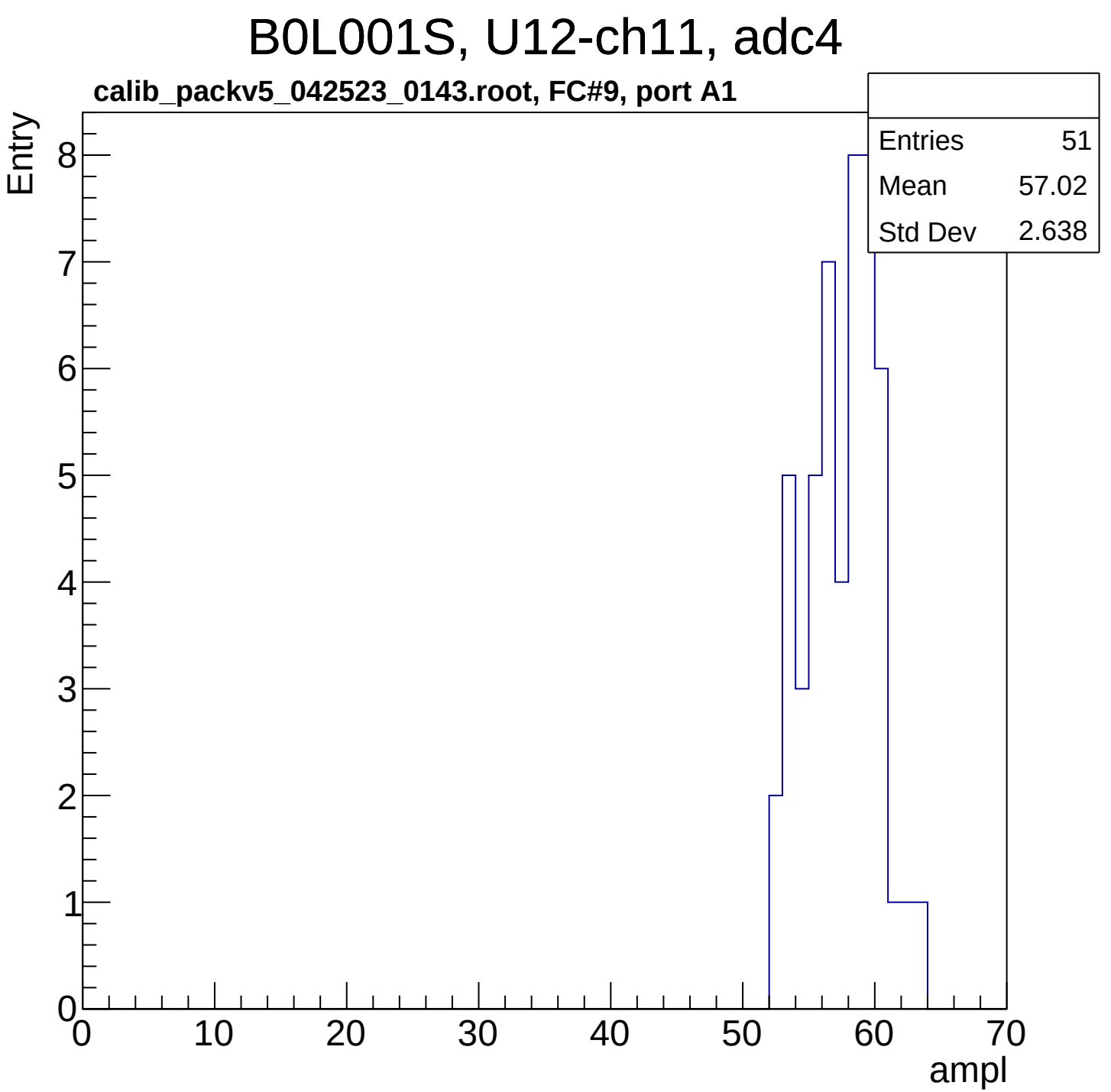
B0L001S, U12-ch11, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 51
Mean 57.02
Std Dev 2.638
Entry
ampl
0
1
2
3
4
5
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7
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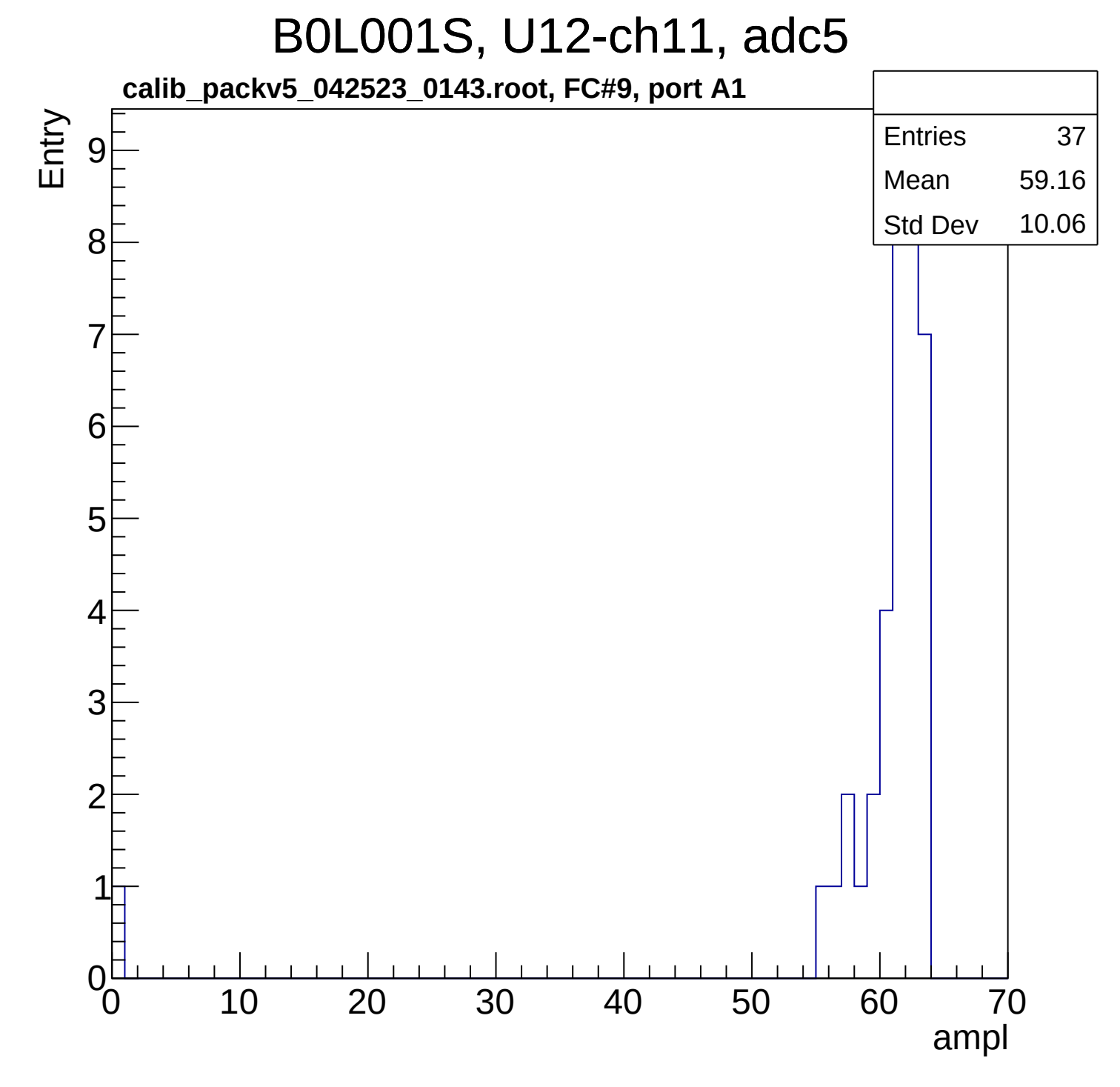
B0L001S, U12-ch11, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 37
Mean 59.16
Std Dev 10.06
Entry
ampl
0
1
2
3
4
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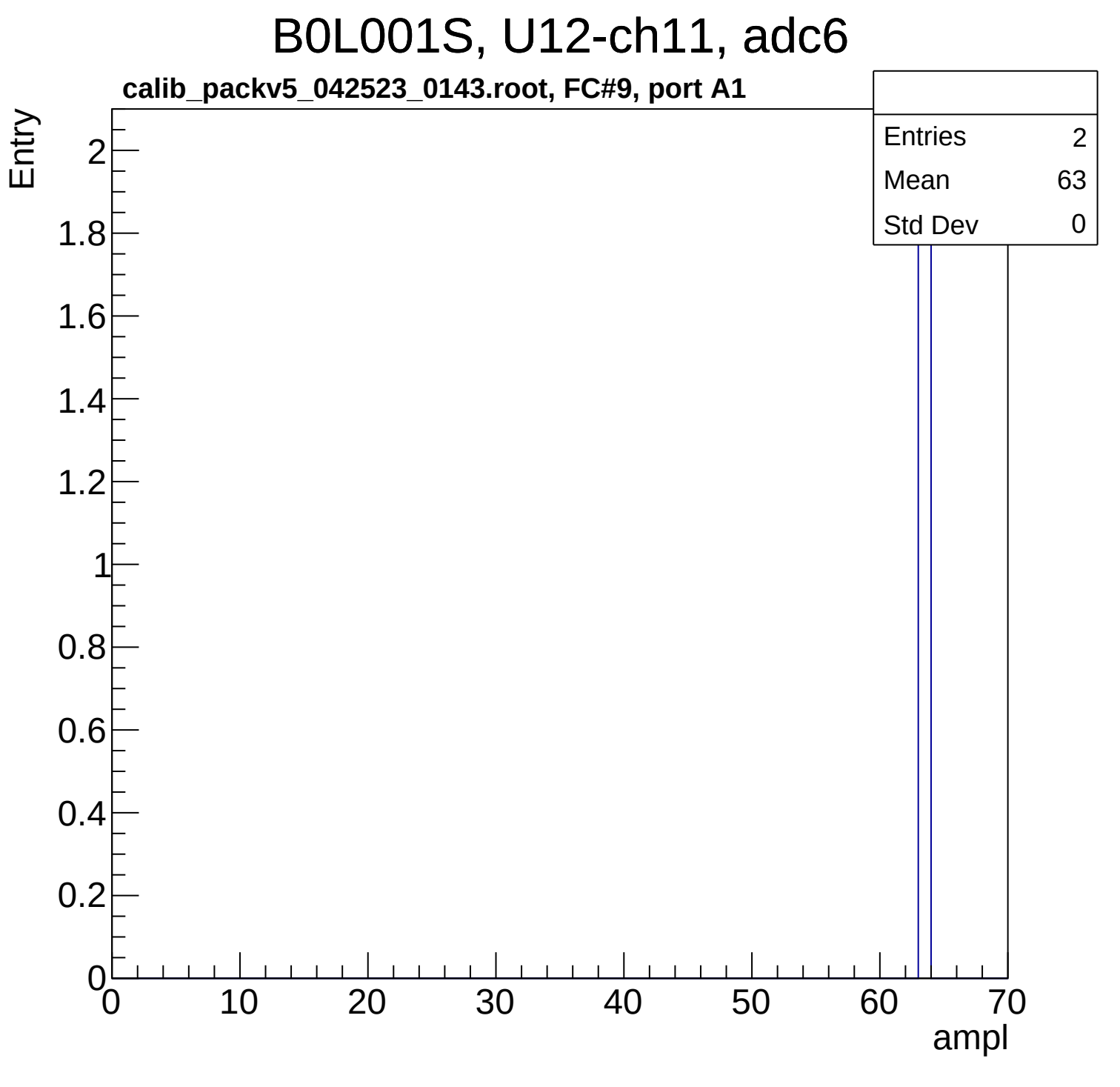
B0L001S, U12-ch11, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
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60
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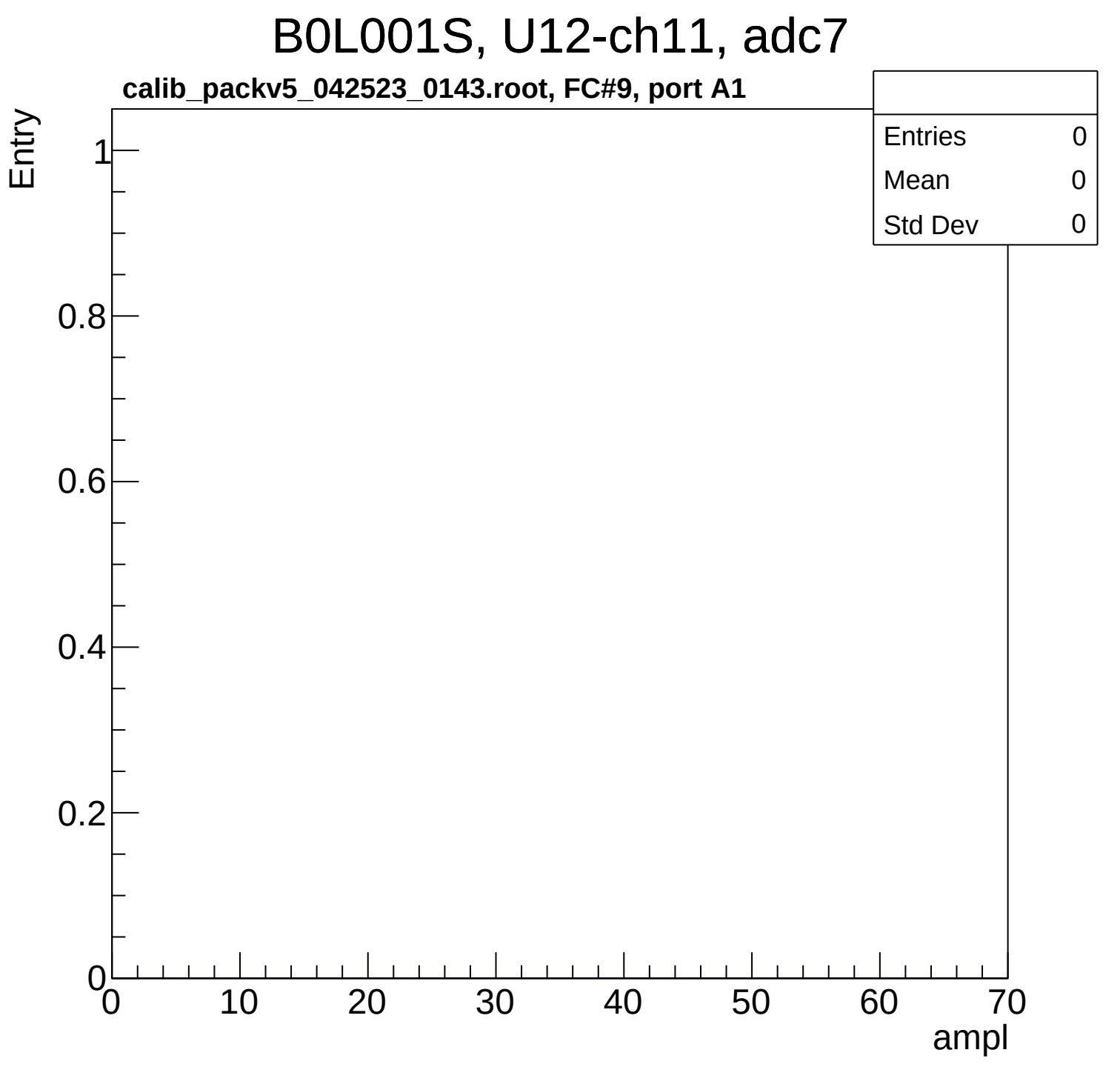
B0L001S, U12-ch11, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
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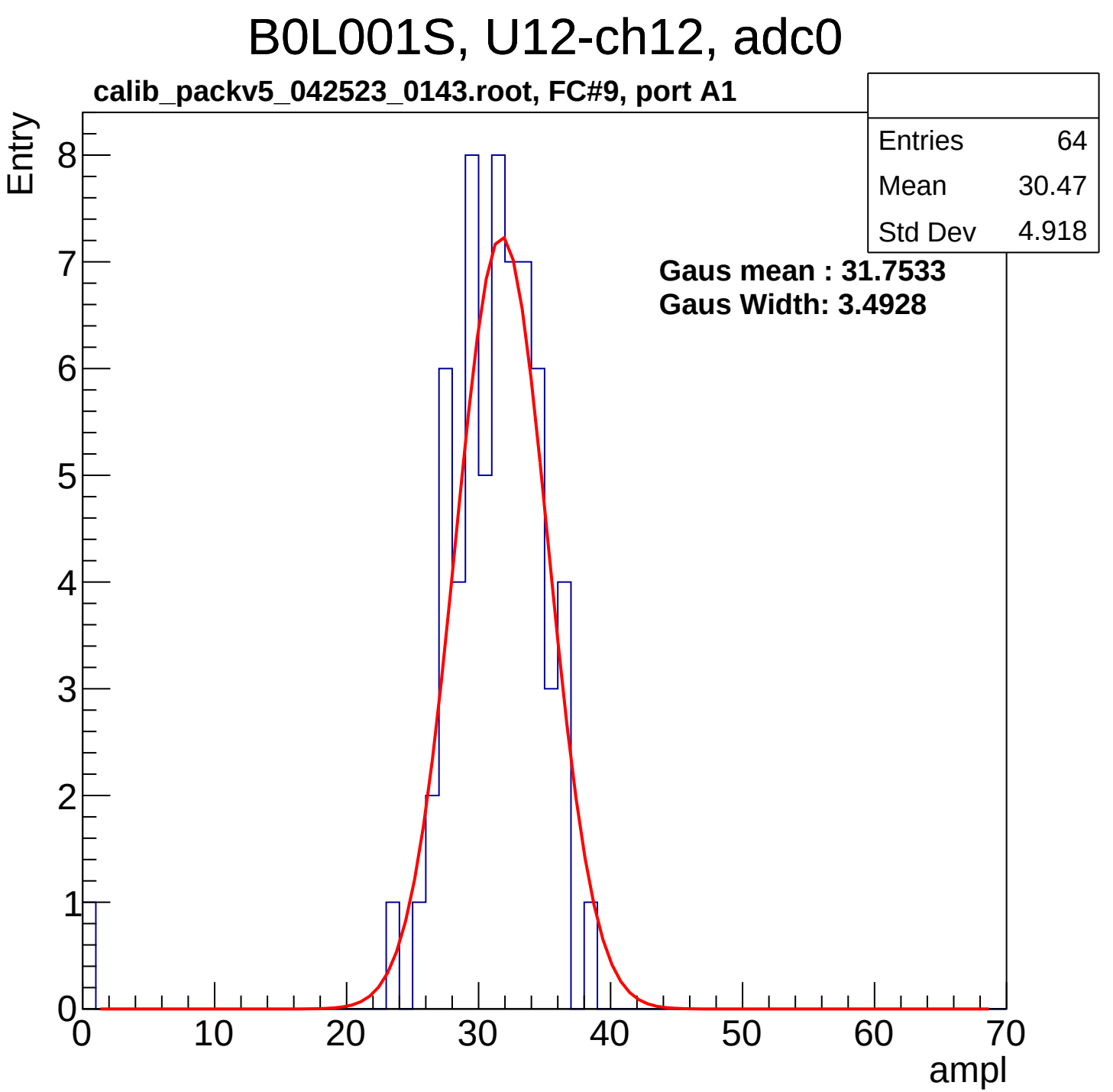
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch12, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 64
Mean 30.47
Std Dev 4.918
Gaus mean : 31.7533
Gaus Width: 3.4928
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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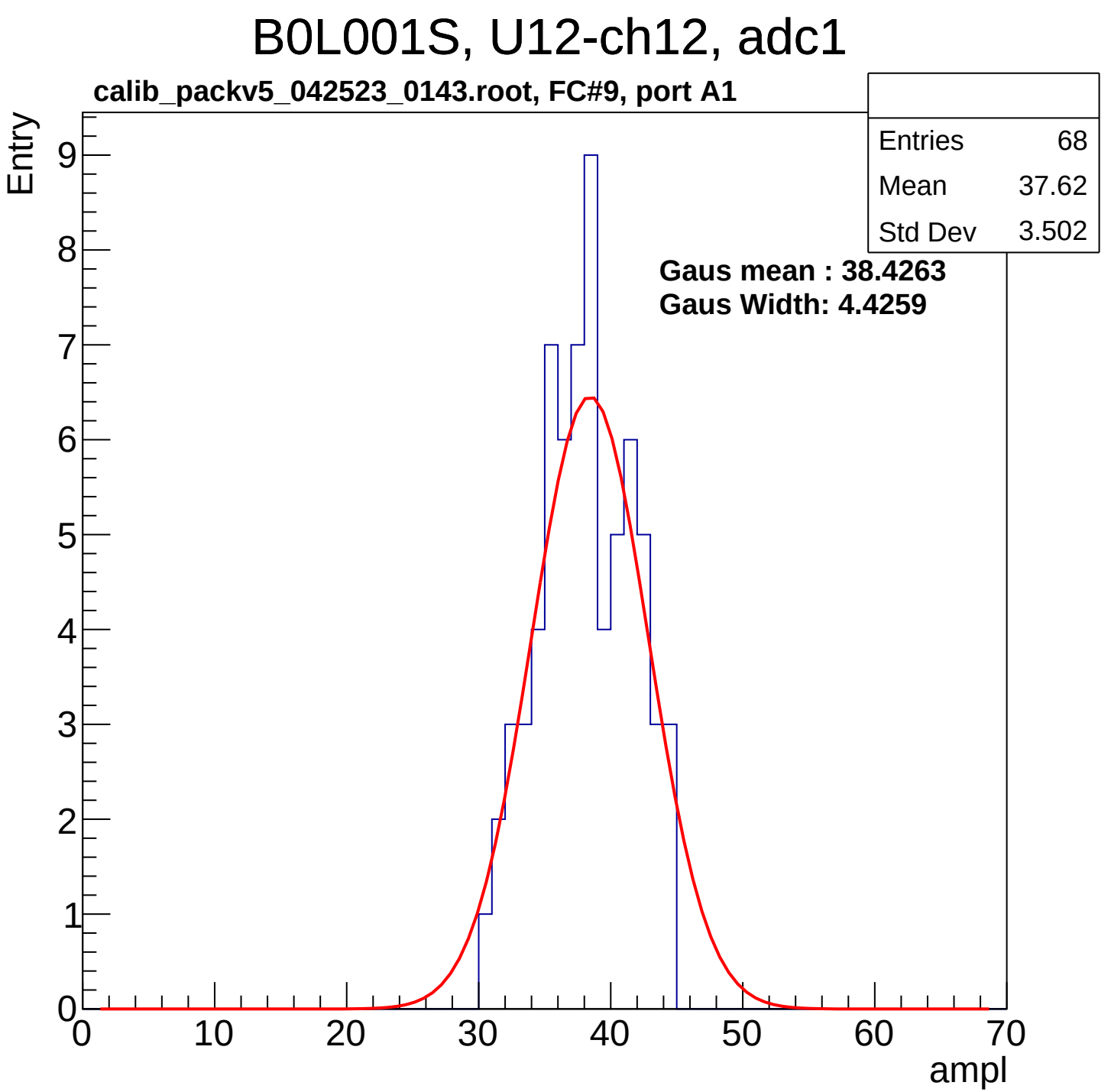
B0L001S, U12-ch12, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 68
Mean 37.62
Std Dev 3.502
Gaus mean : 38.4263
Gaus Width: 4.4259
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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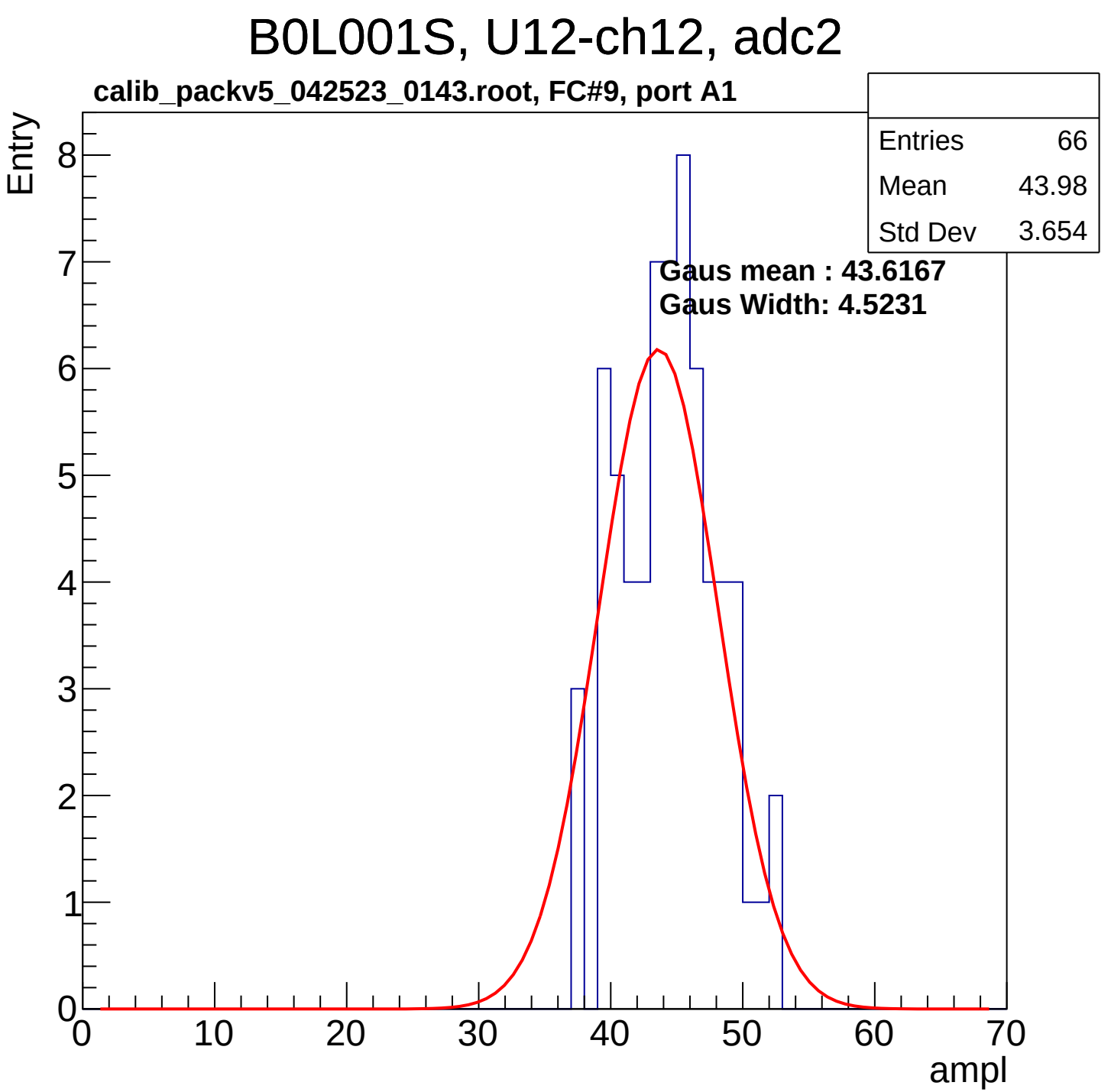
B0L001S, U12-ch12, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 66
Mean 43.98
Std Dev 3.654
Gaus mean : 43.6167
Gaus Width: 4.5231
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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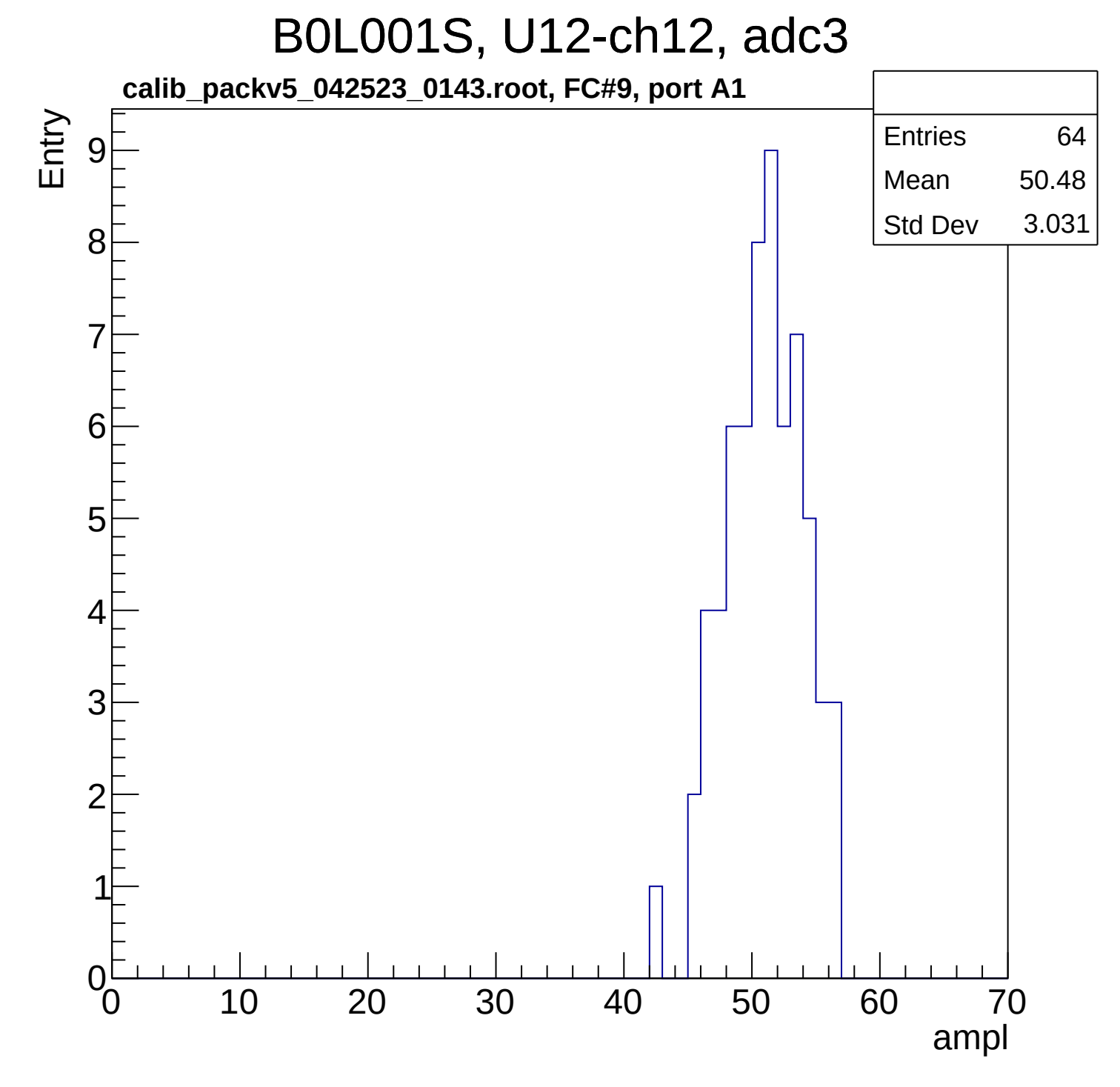
B0L001S, U12-ch12, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 64
Mean 50.48
Std Dev 3.031
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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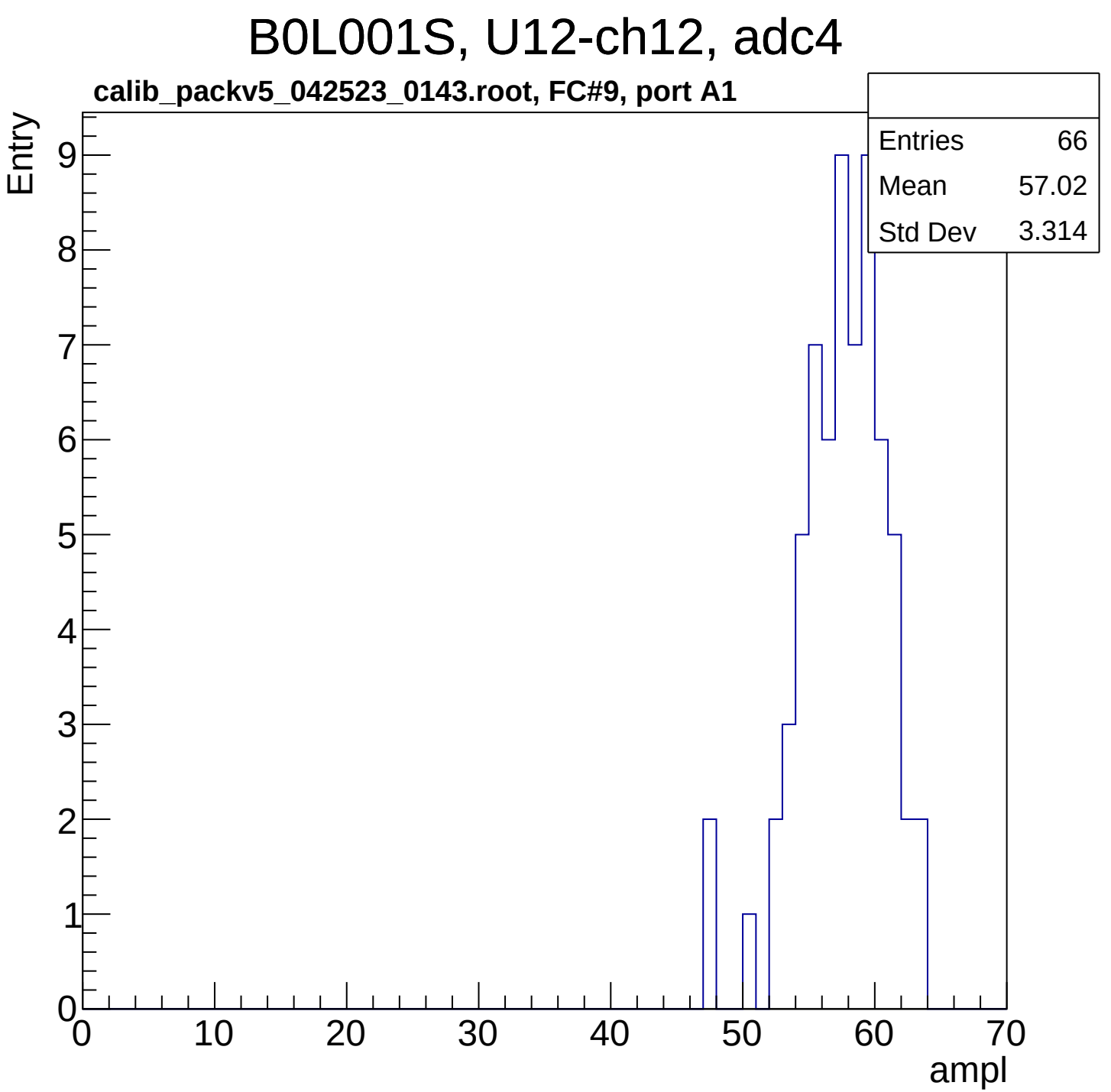
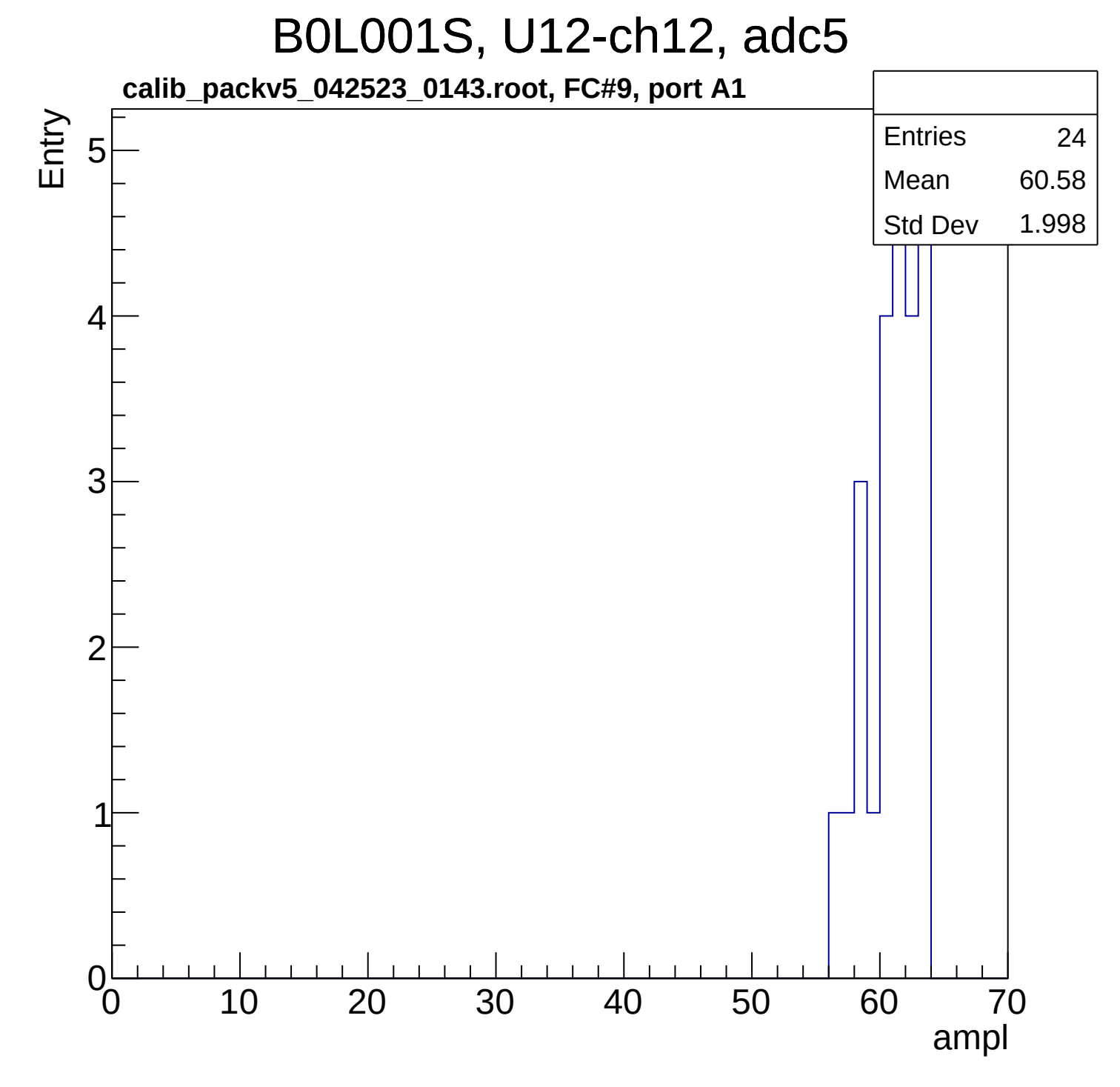
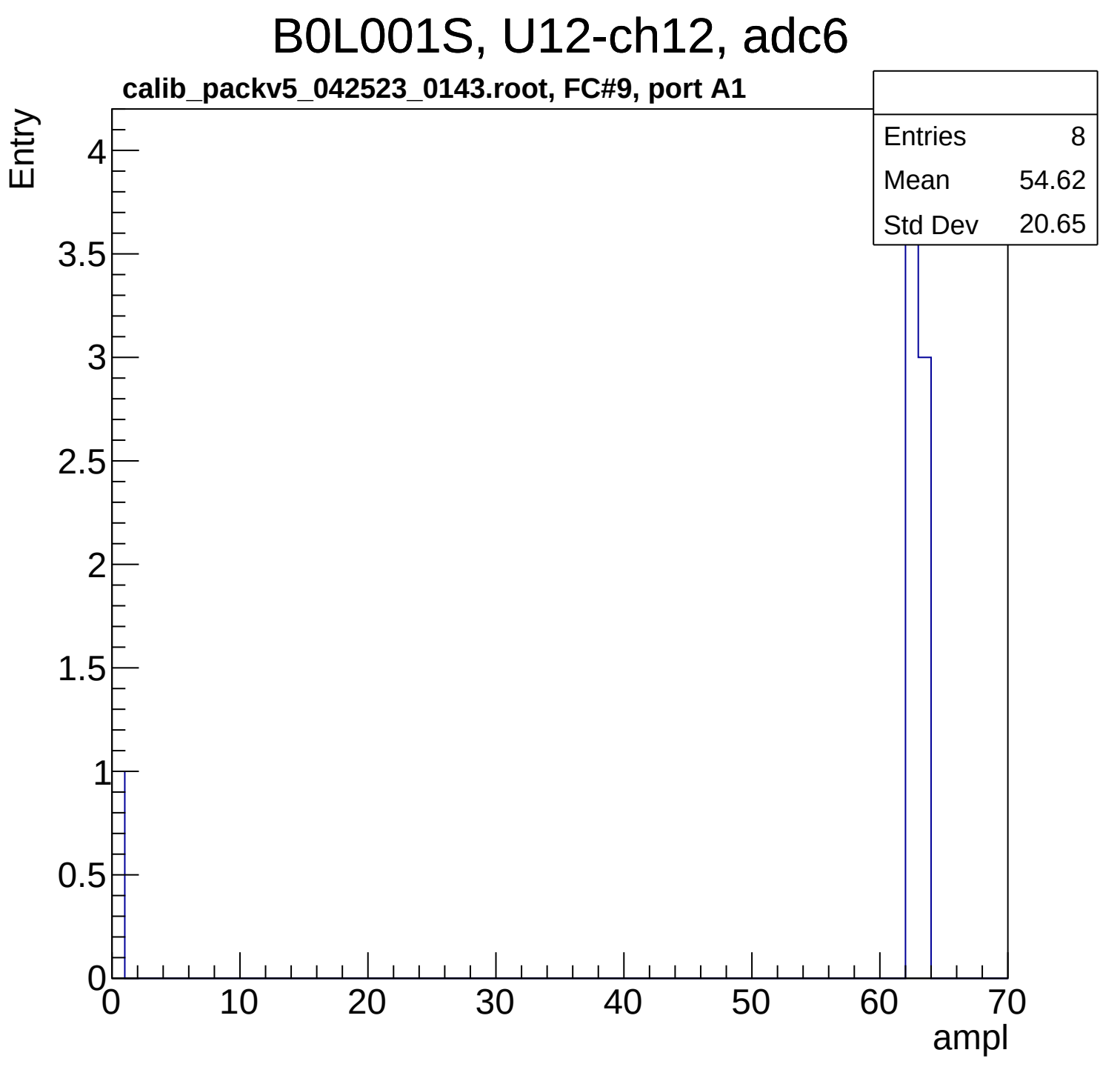
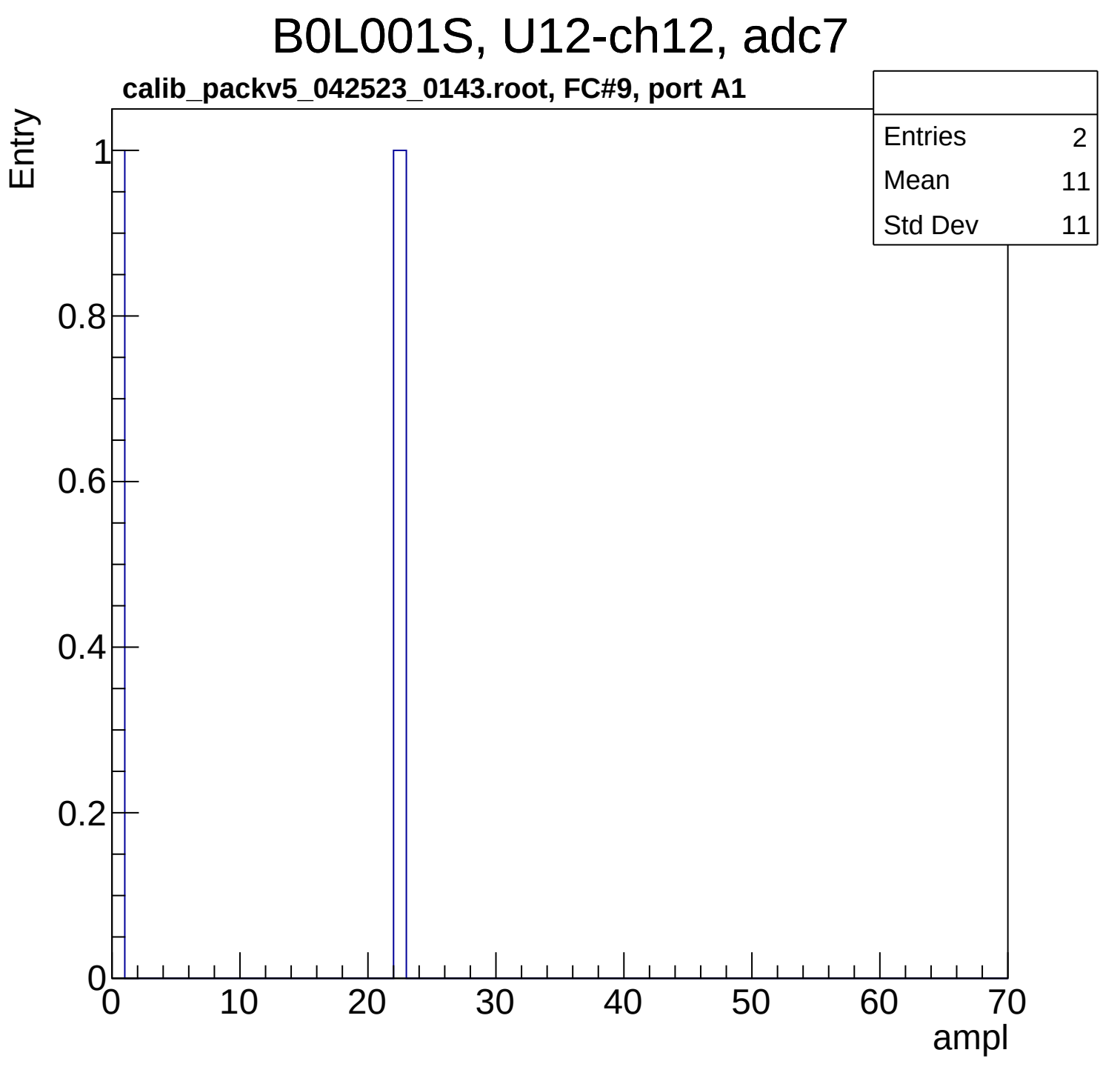
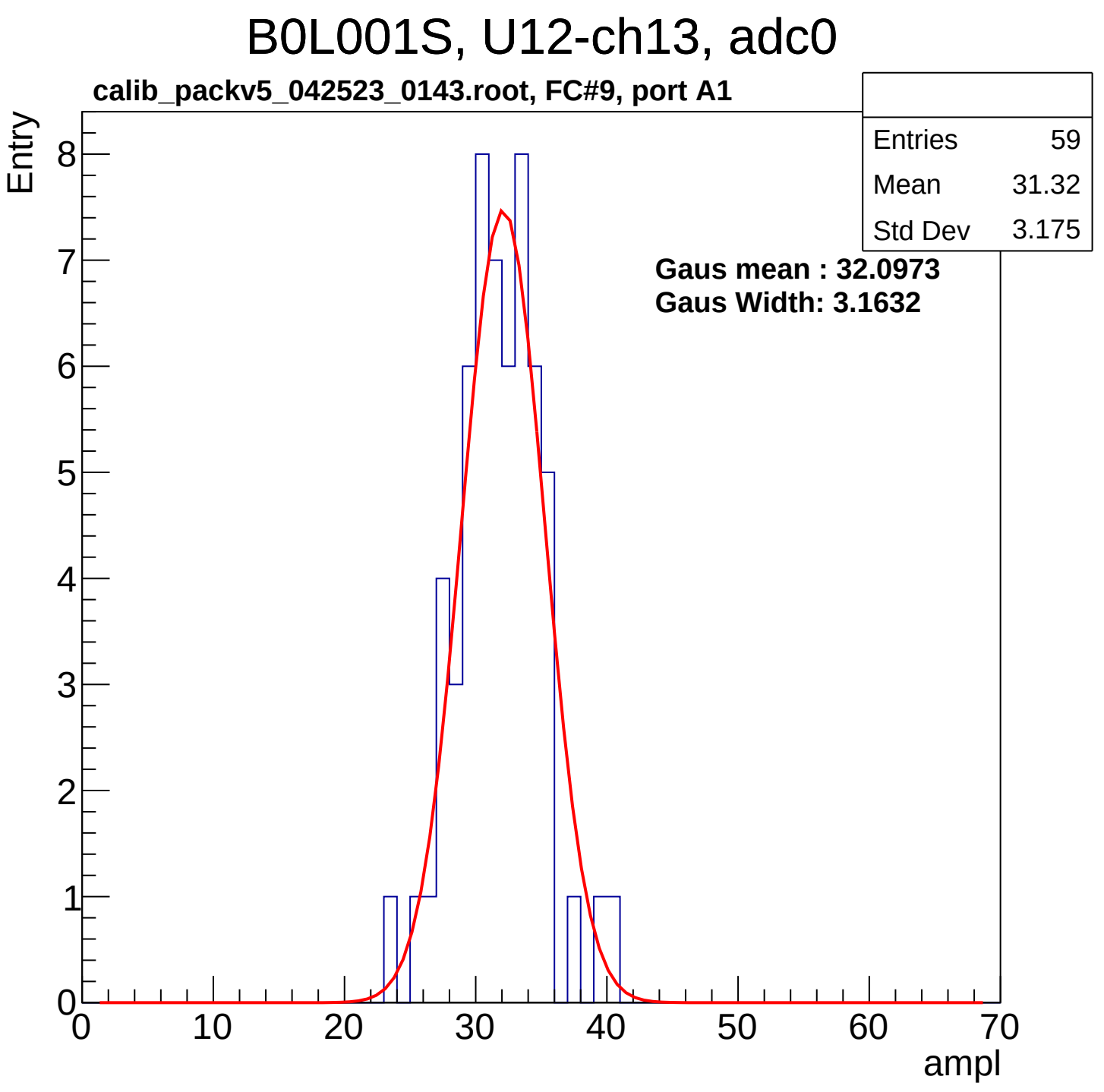
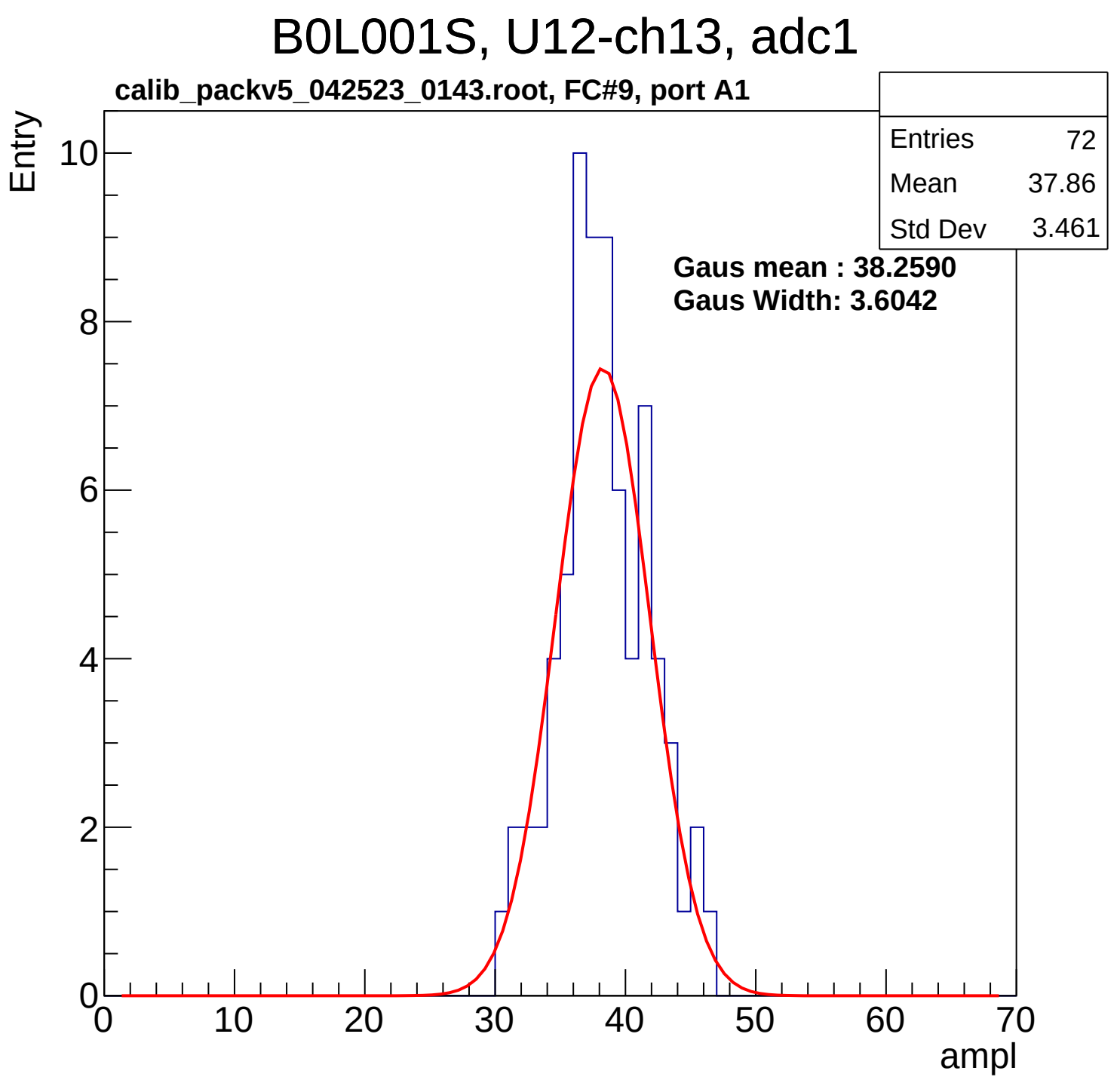

B0L001S, U12-ch12, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 66
Mean 57.02
Std Dev 3.314
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch12, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 24
Mean 60.58
Std Dev 1.998
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L001S, U12-ch12, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 8
Mean 54.62
Std Dev 20.65
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B0L001S, U12-ch12, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 11
Std Dev 11
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch13, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 59
Mean 31.32
Std Dev 3.175
Gaus mean : 32.0973
Gaus Width: 3.1632
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch13, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 72
Mean 37.86
Std Dev 3.461
Gaus mean : 38.2590
Gaus Width: 3.6042
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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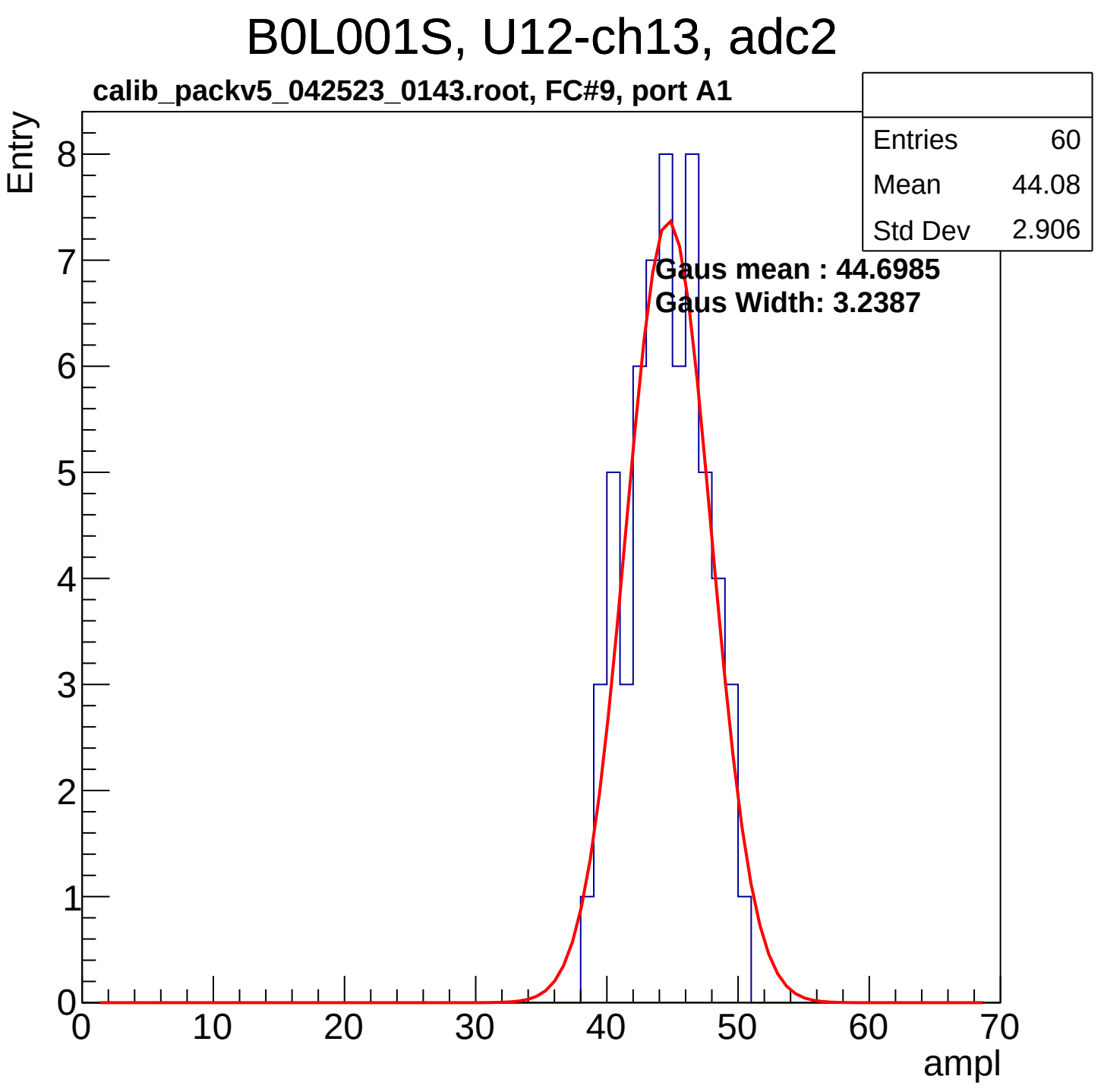
B0L001S, U12-ch13, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 60
Mean 44.08
Std Dev 2.906
Gaus mean : 44.6985
Gaus Width: 3.2387
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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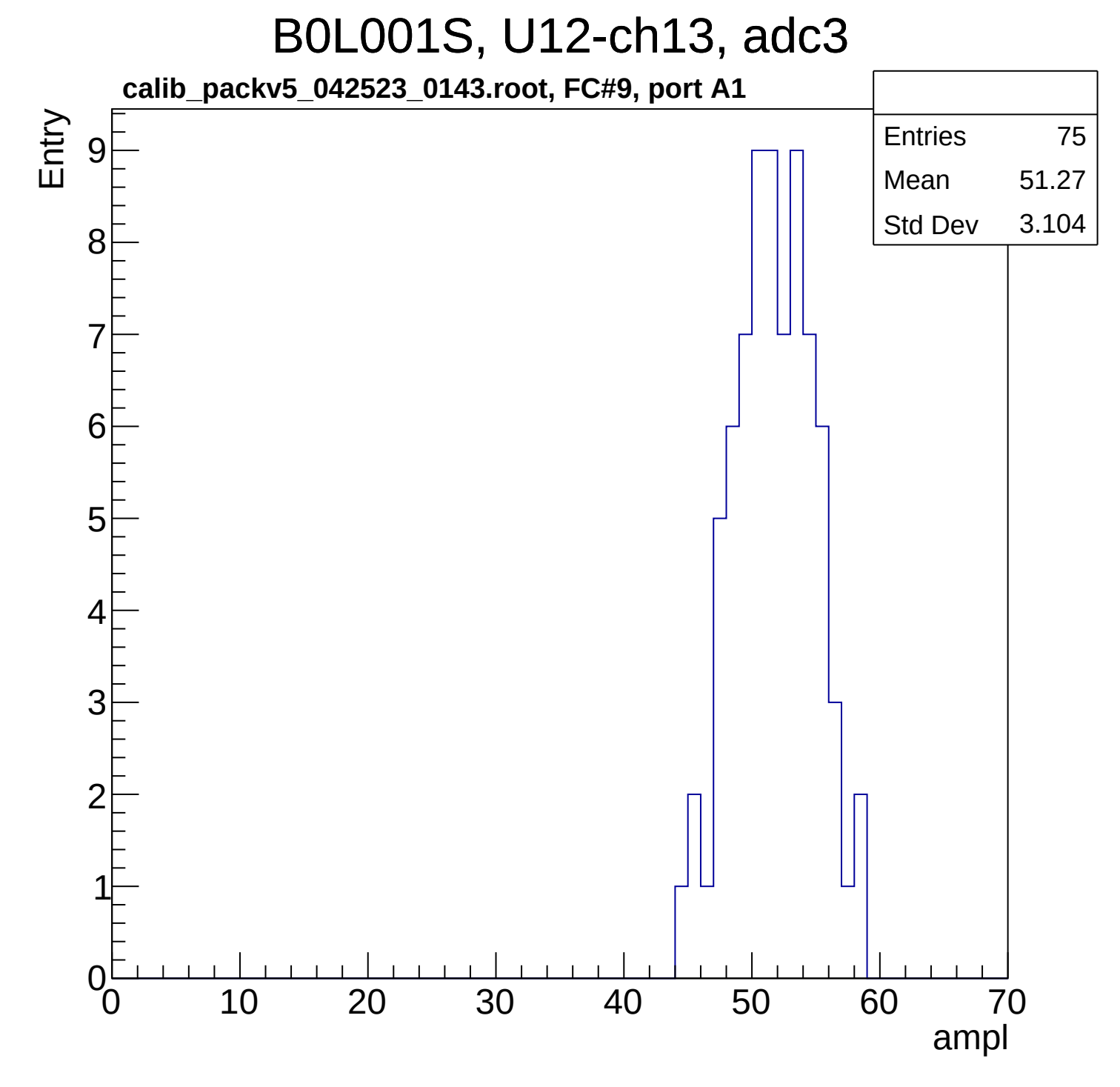
B0L001S, U12-ch13, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 75
Mean 51.27
Std Dev 3.104
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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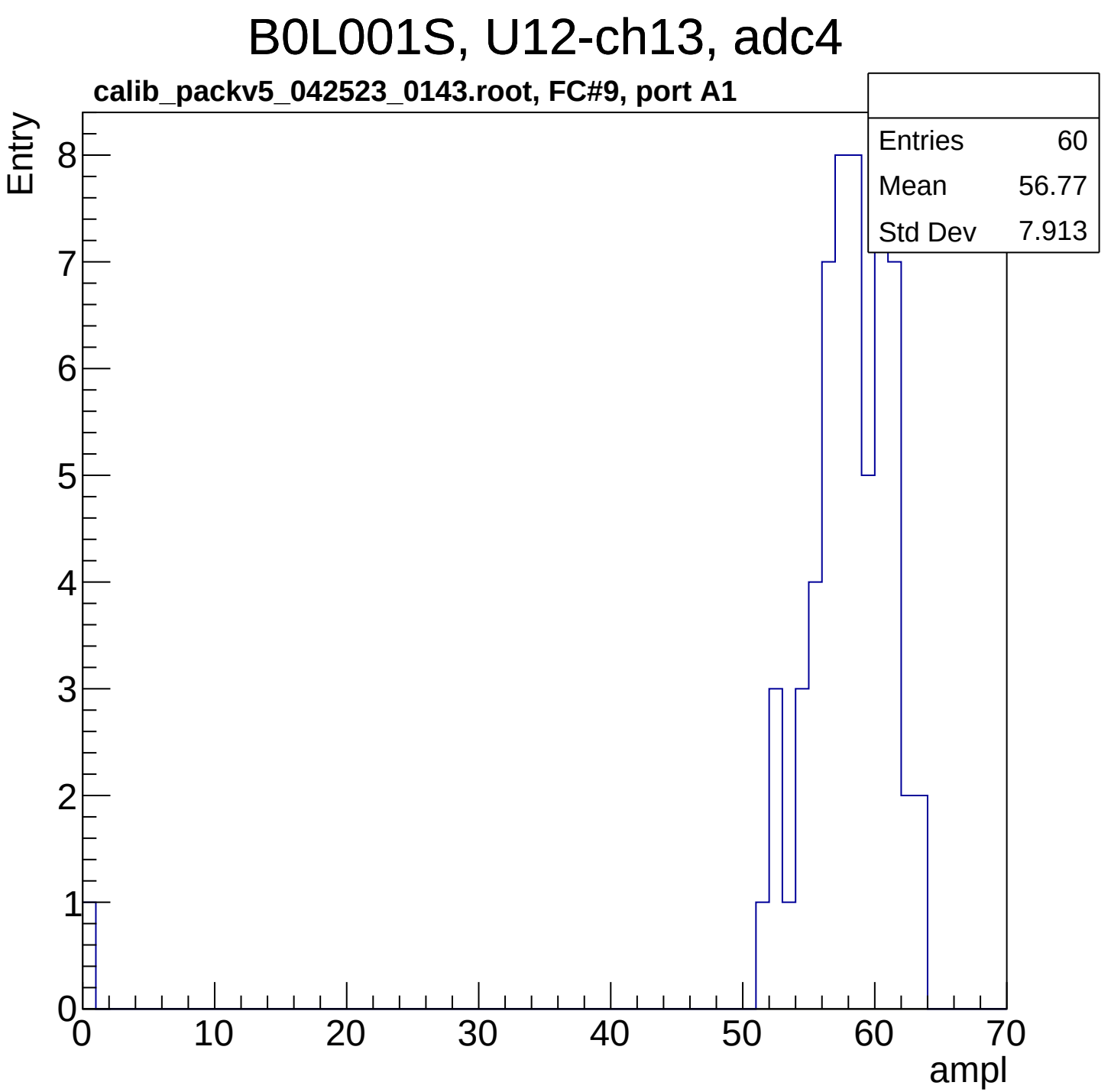
B0L001S, U12-ch13, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 60
Mean 56.77
Std Dev 7.913
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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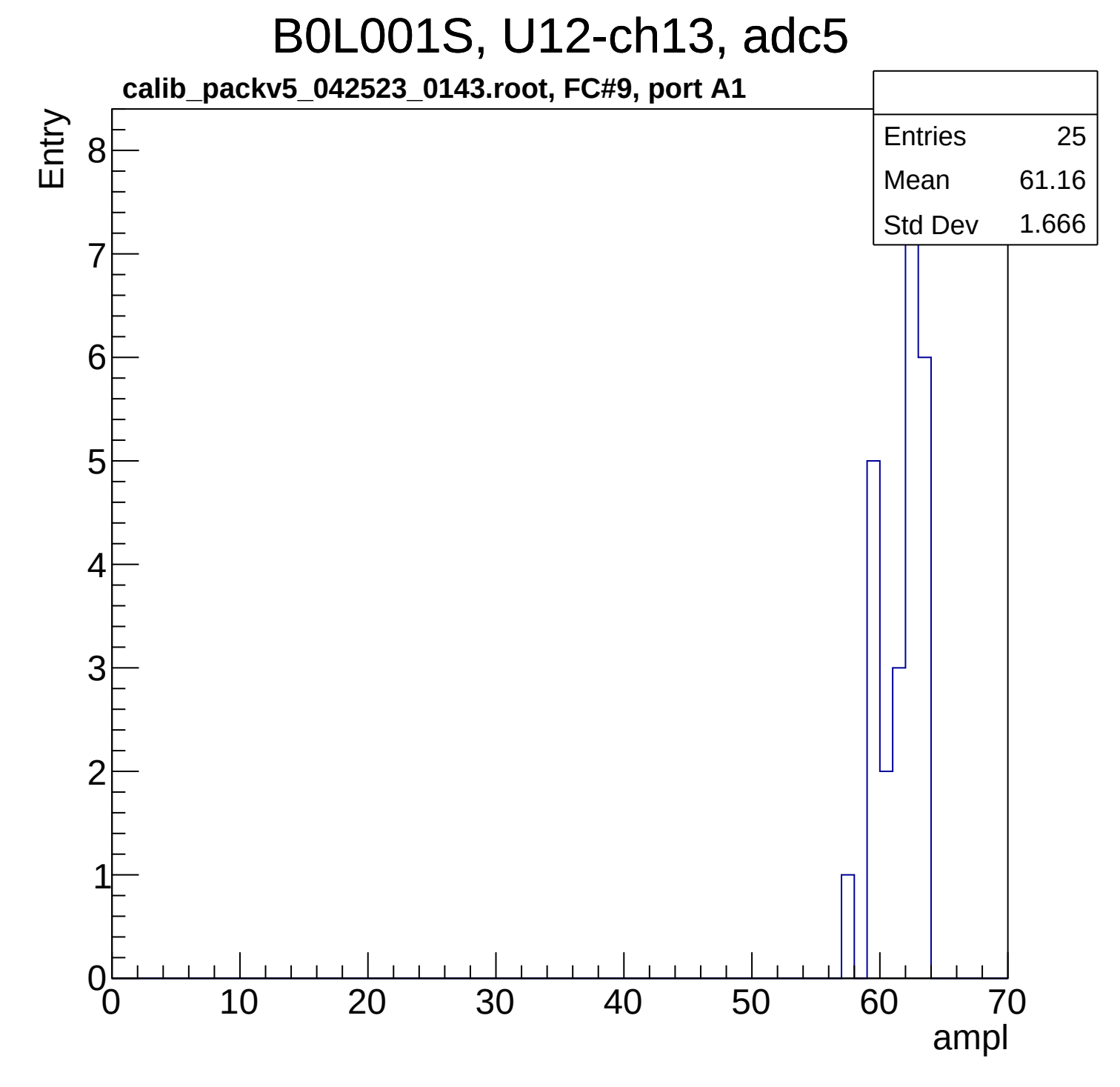
B0L001S, U12-ch13, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 25
Mean 61.16
Std Dev 1.666
Entry
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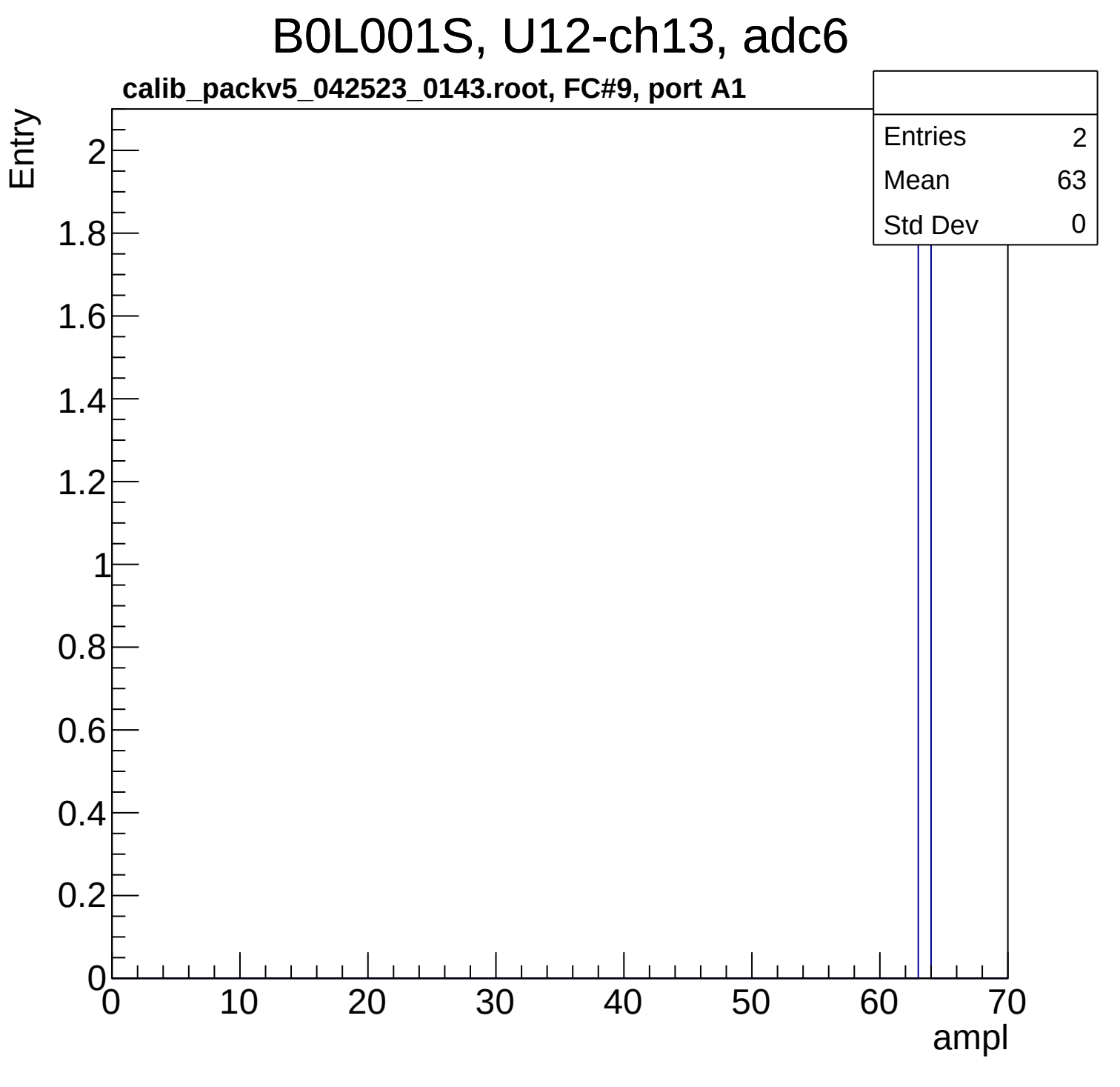
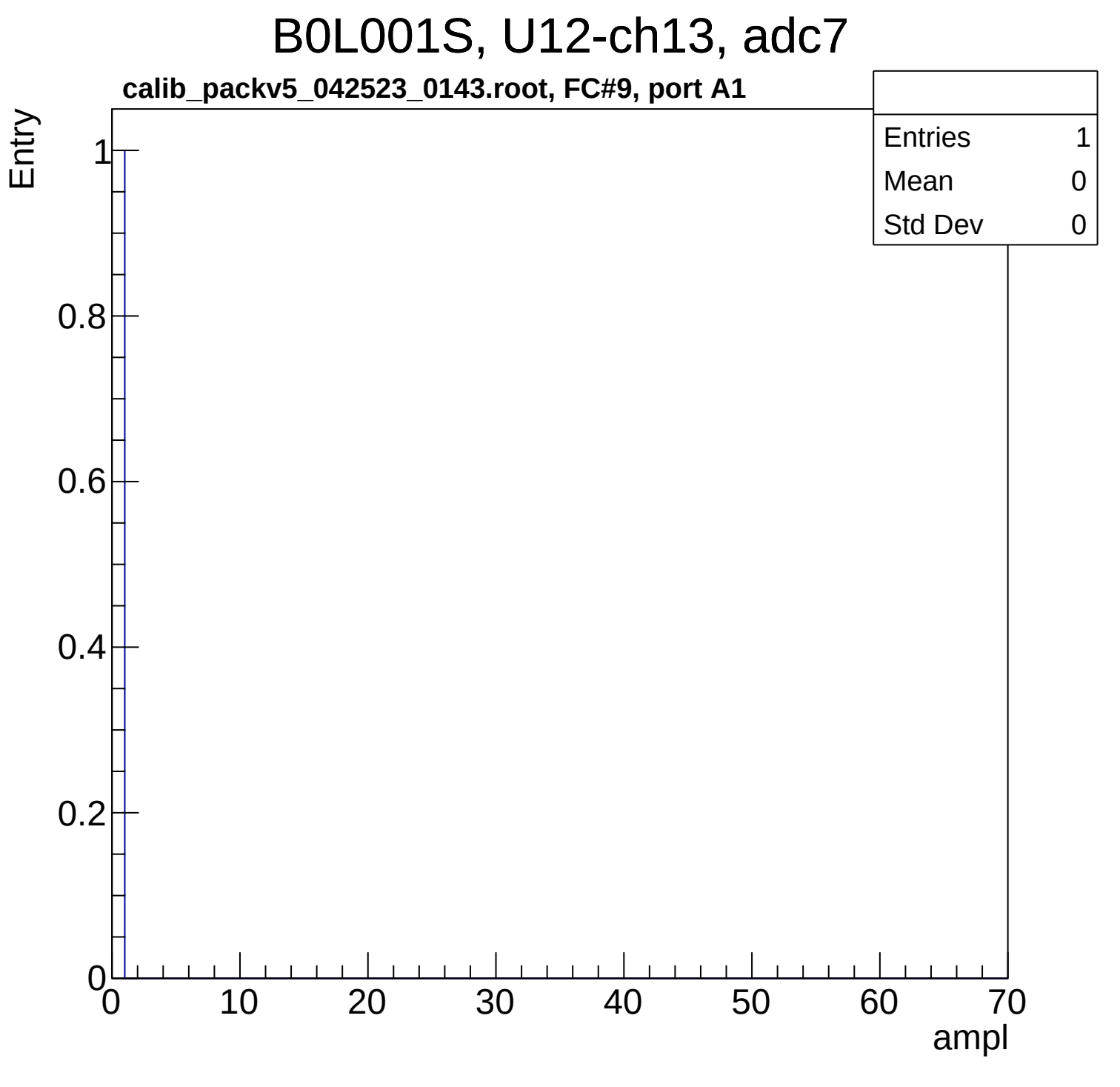
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch13, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L001S, U12-ch13, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 0
Std Dev 0
Entry
1
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0.6
0.4
0.2
0
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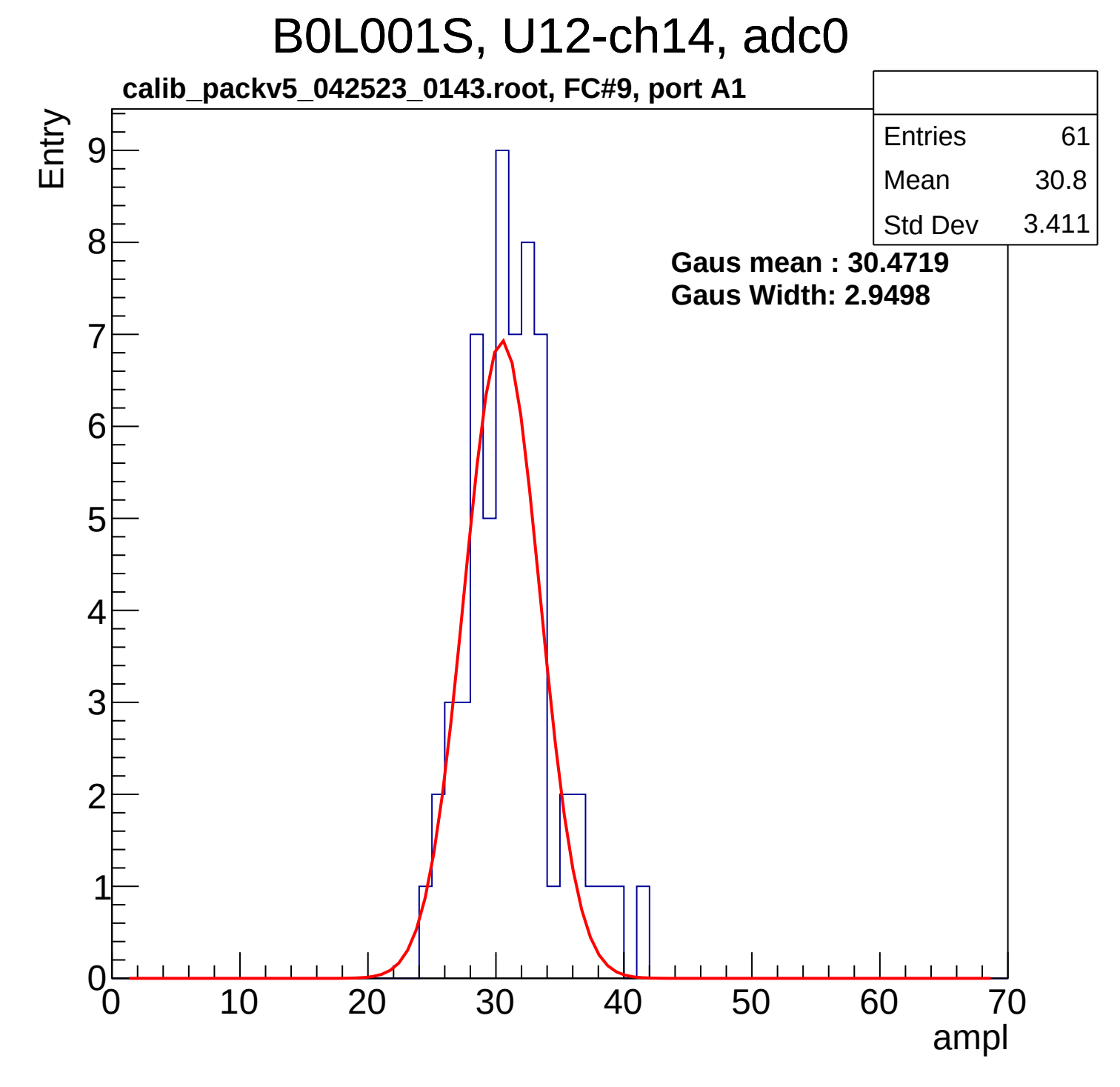
50
60
70
ampl


B0L001S, U12-ch14, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 61
Mean 30.8
Std Dev 3.411
Gaus mean : 30.4719
Gaus Width: 2.9498
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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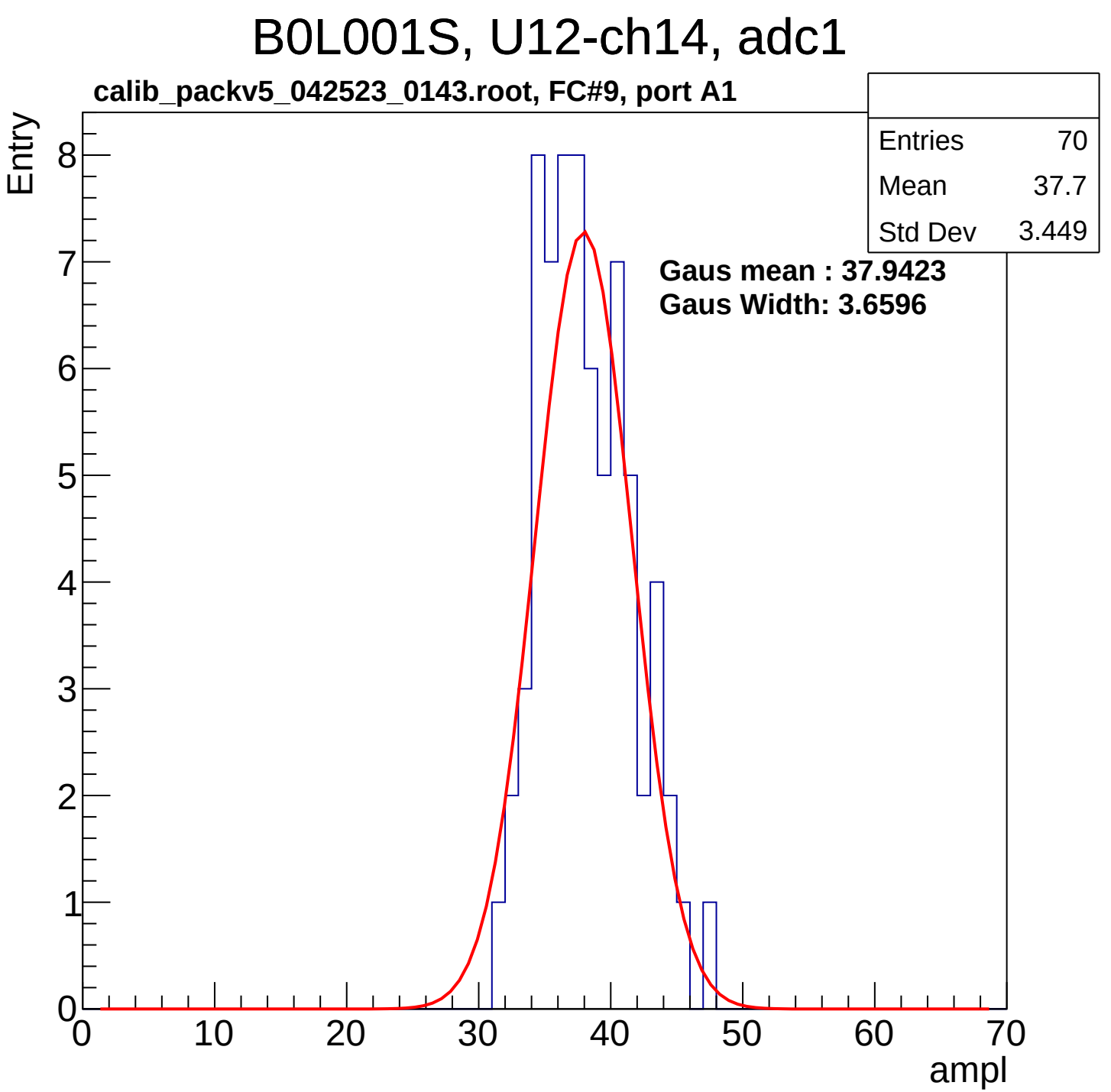
B0L001S, U12-ch14, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 70
Mean 37.7
Std Dev 3.449
Gaus mean : 37.9423
Gaus Width: 3.6596
Entry
ampl
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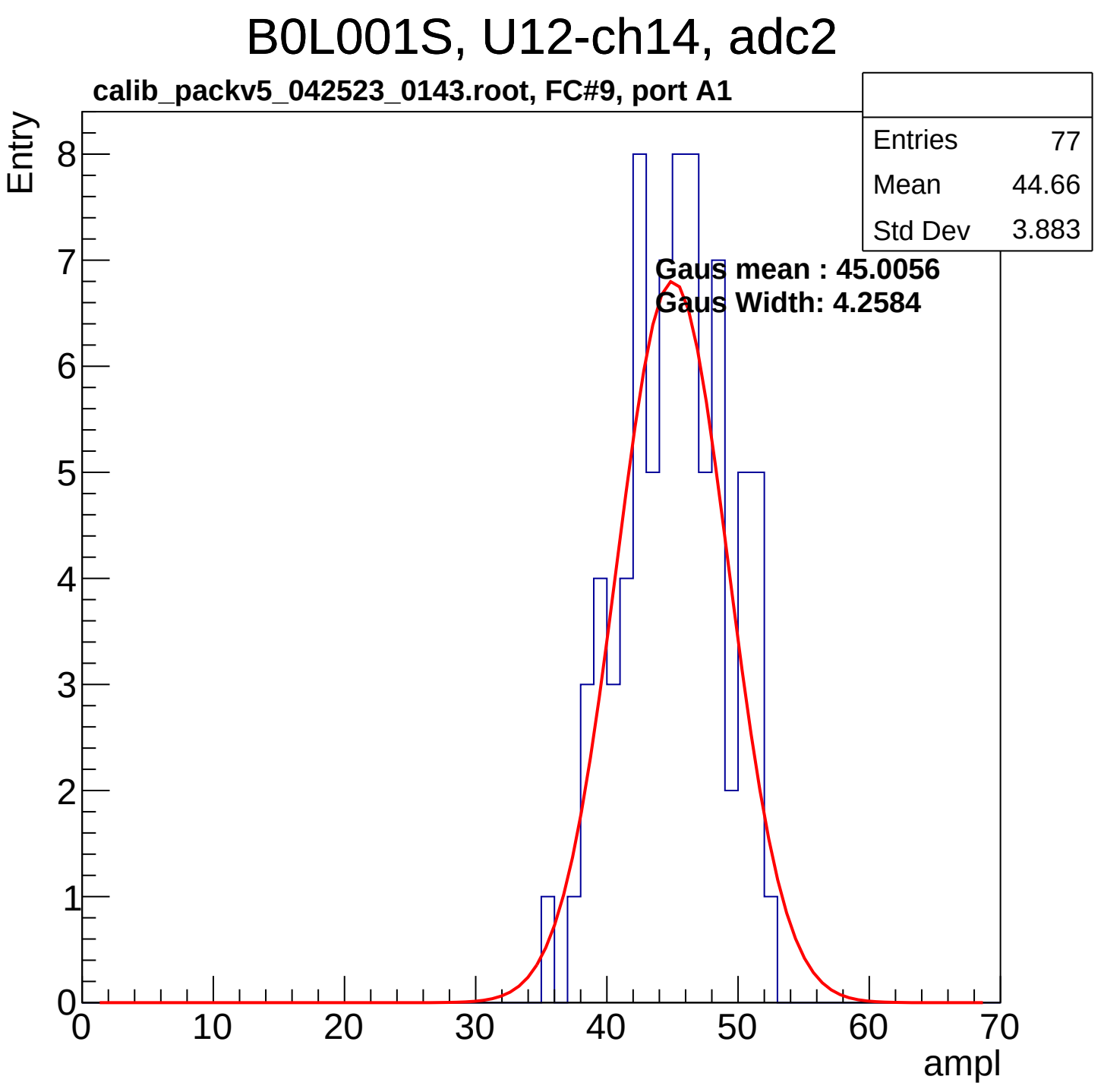
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch14, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 77
Mean 44.66
Std Dev 3.883
Gaus mean : 45.0056
Gaus Width: 4.2584
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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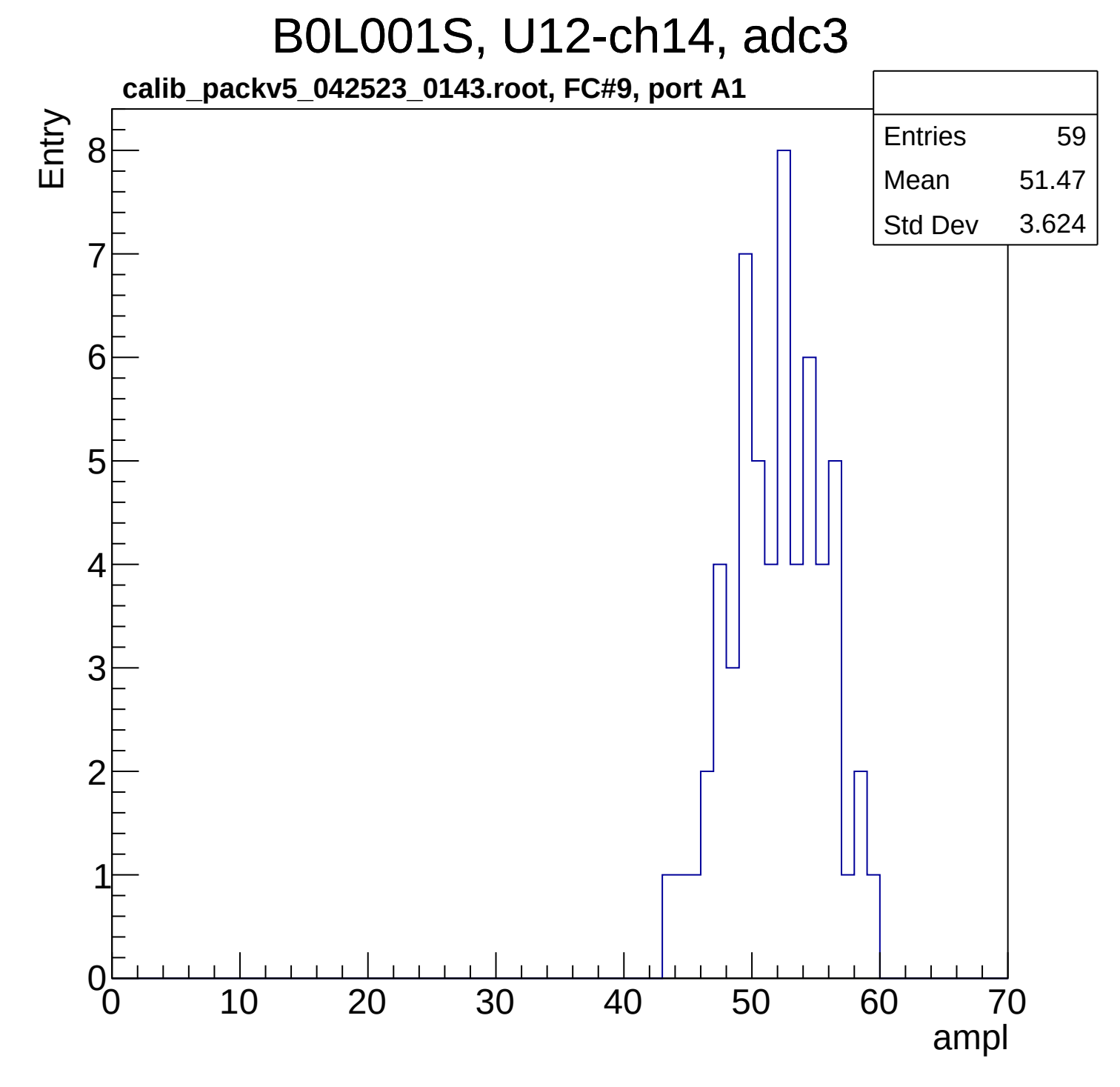
60
70


B0L001S, U12-ch14, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 59
Mean 51.47
Std Dev 3.624
Entry
ampl
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2
3
4
5
6
7
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0
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60
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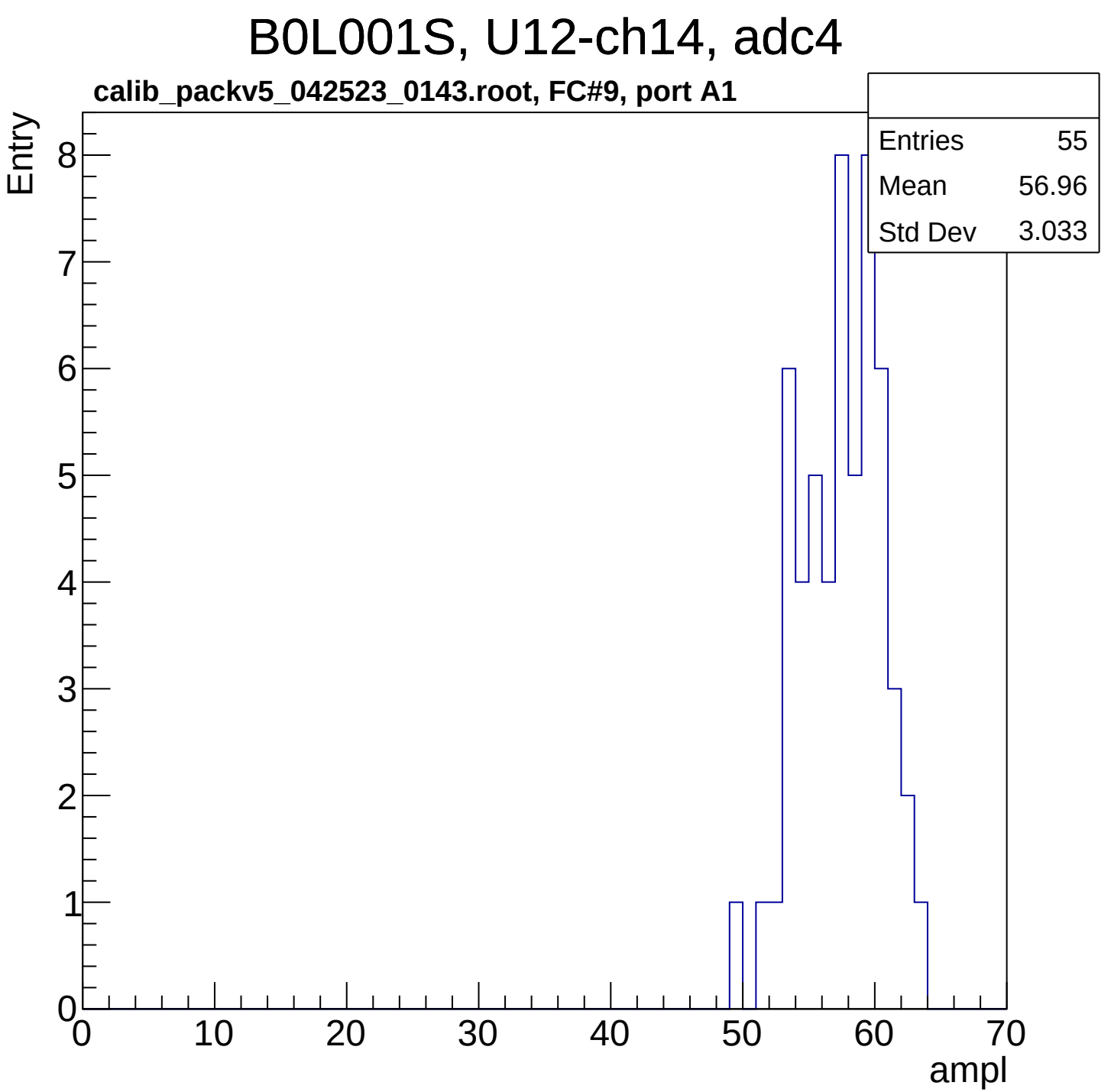
B0L001S, U12-ch14, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 55
Mean 56.96
Std Dev 3.033
Entry
ampl
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5
6
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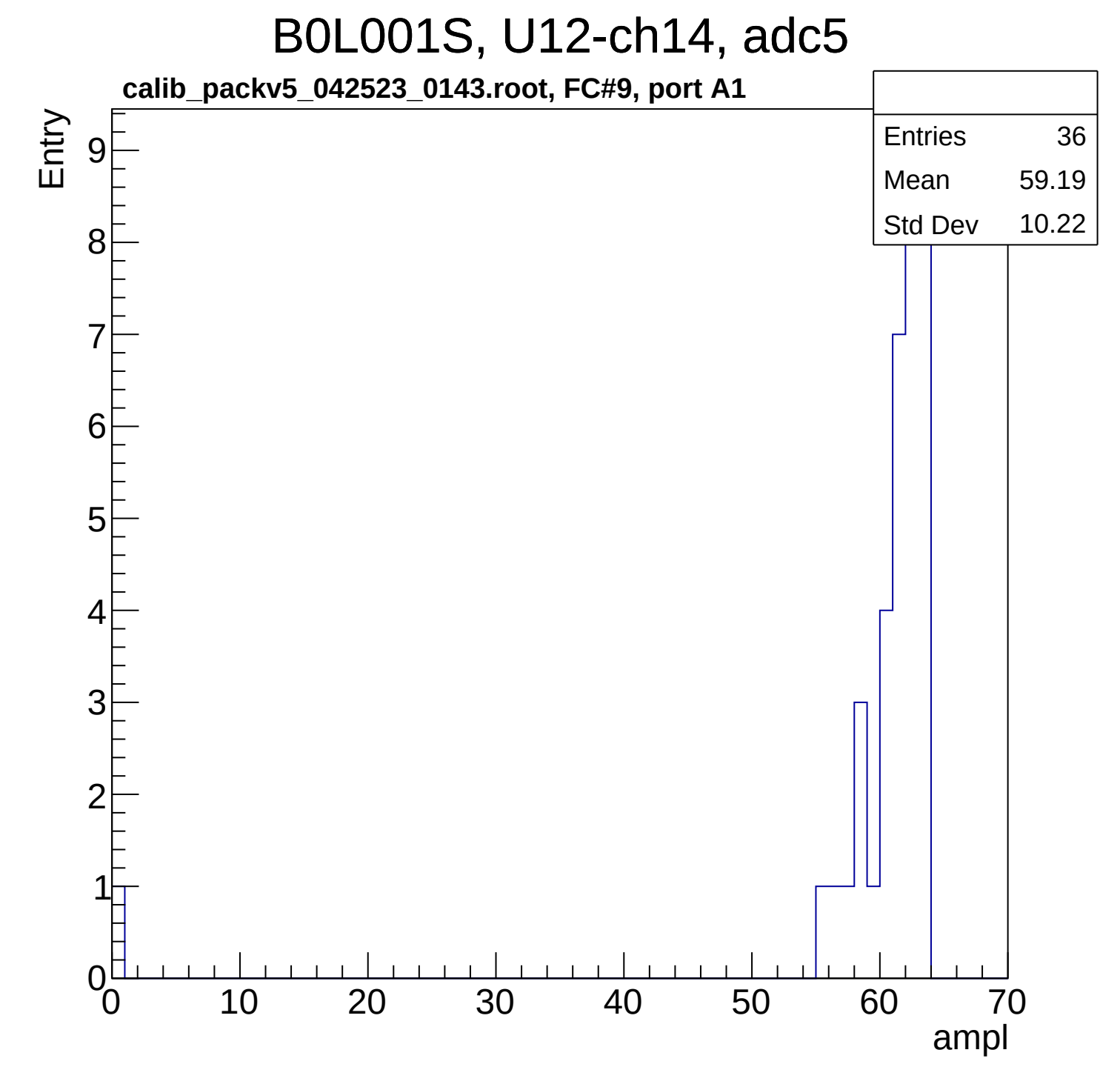
B0L001S, U12-ch14, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 36
Mean 59.19
Std Dev 10.22
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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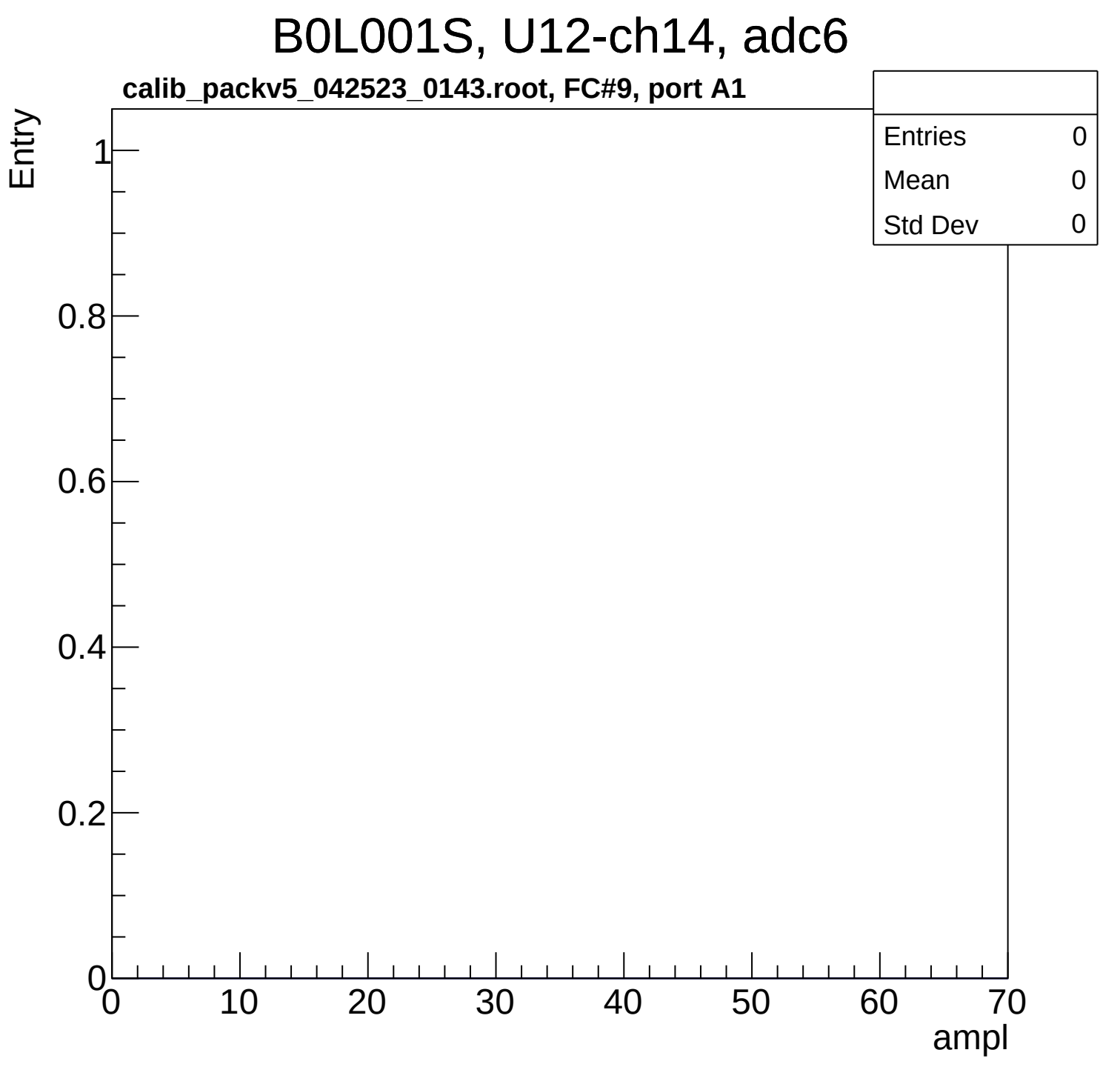
B0L001S, U12-ch14, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
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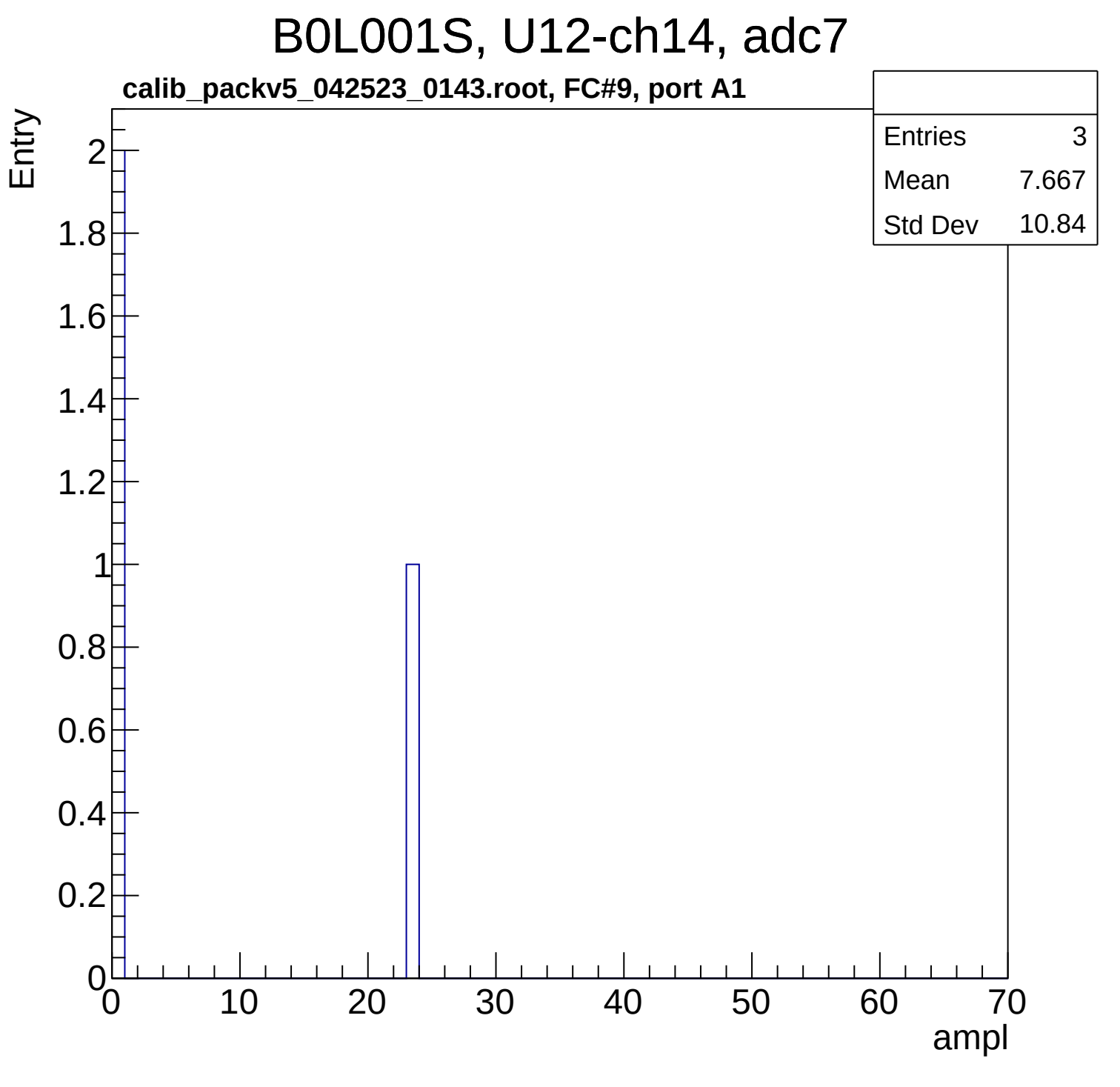
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch14, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 3
Mean 7.667
Std Dev 10.84
Entry
ampl
0
0.2
0.4
0.6
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1.2
1.4
1.6
1.8
2
0
10
20
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40
50
60
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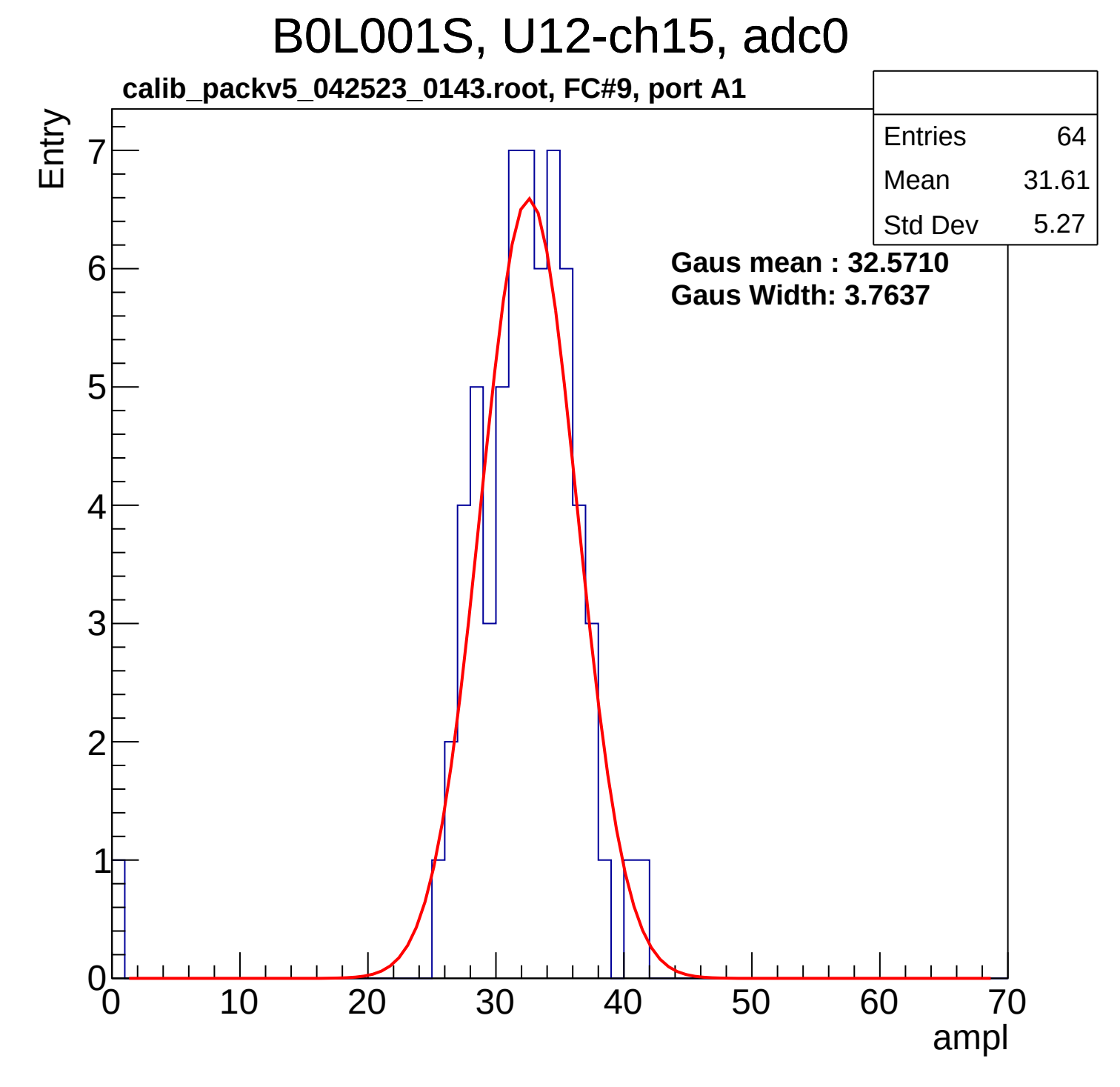
B0L001S, U12-ch15, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 64
Mean 31.61
Std Dev 5.27
Gaus mean : 32.5710
Gaus Width: 3.7637
Entry
ampl
0
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2
3
4
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6
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10
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60
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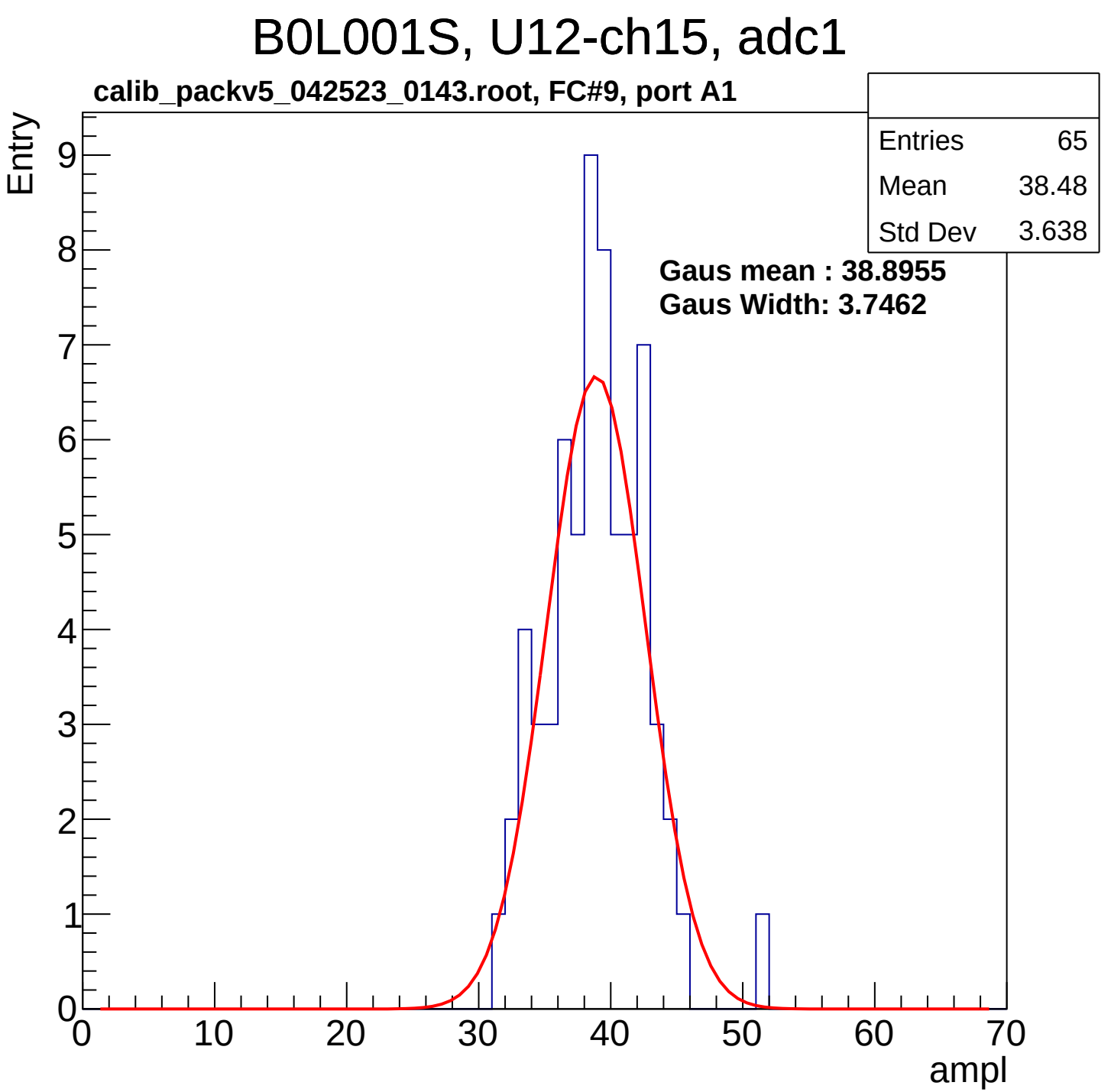
B0L001S, U12-ch15, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 65
Mean 38.48
Std Dev 3.638
Gaus mean : 38.8955
Gaus Width: 3.7462
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
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40
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60
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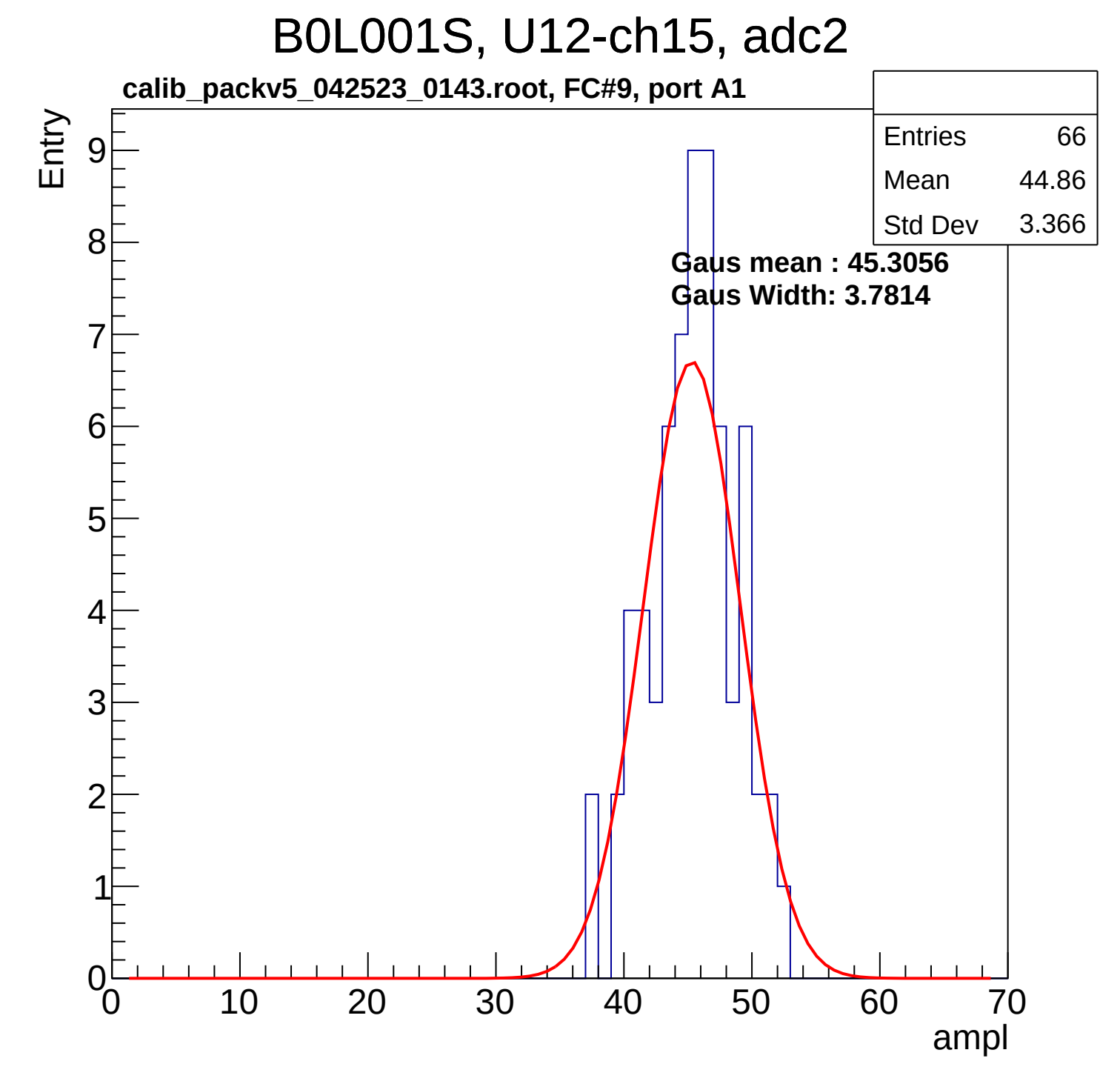
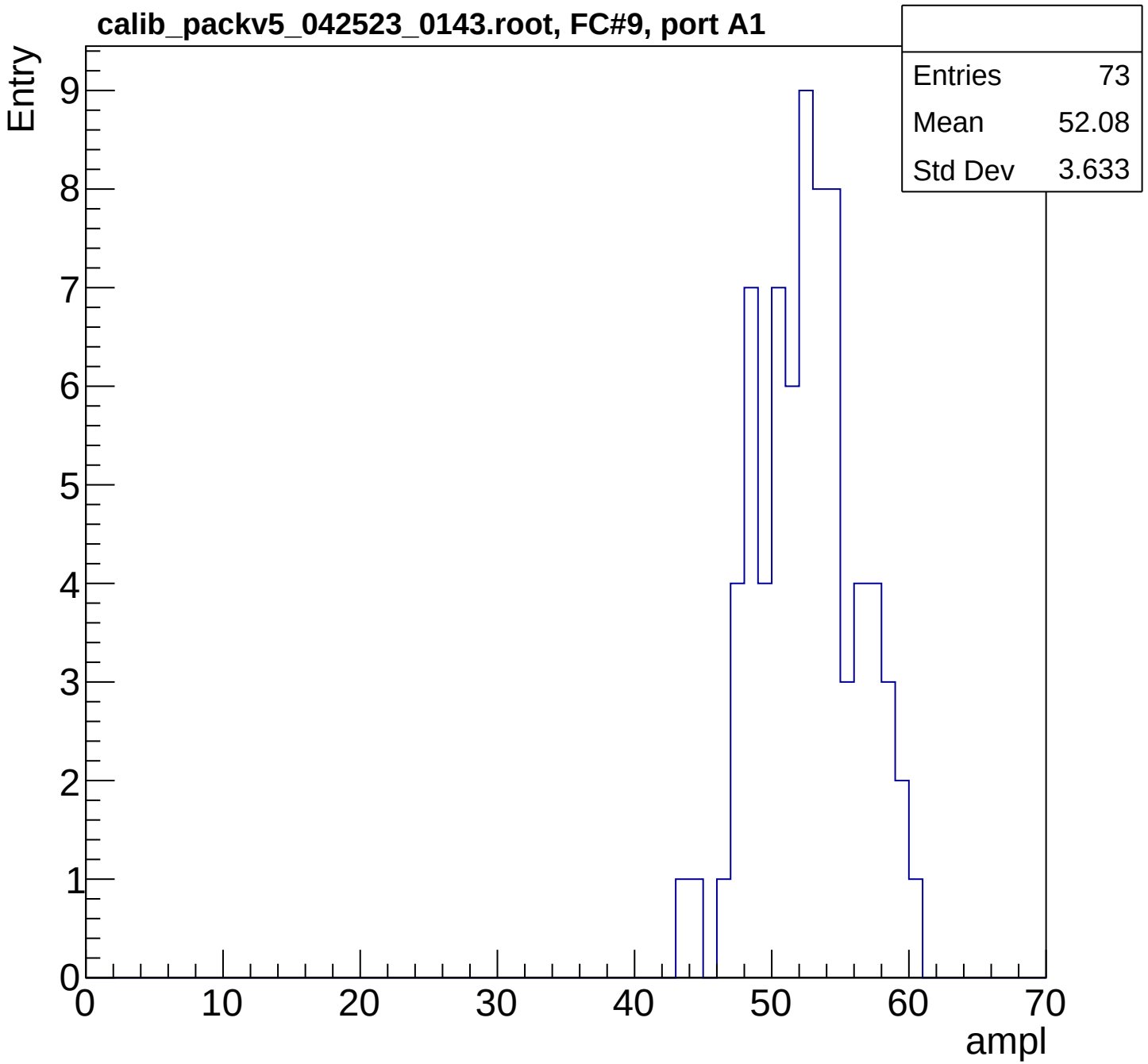

B0L001S, U12-ch15, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 66
Mean 44.86
Std Dev 3.366
Gaus mean : 45.3056
Gaus Width: 3.7814
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch15, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 73
Mean 52.08
Std Dev 3.633
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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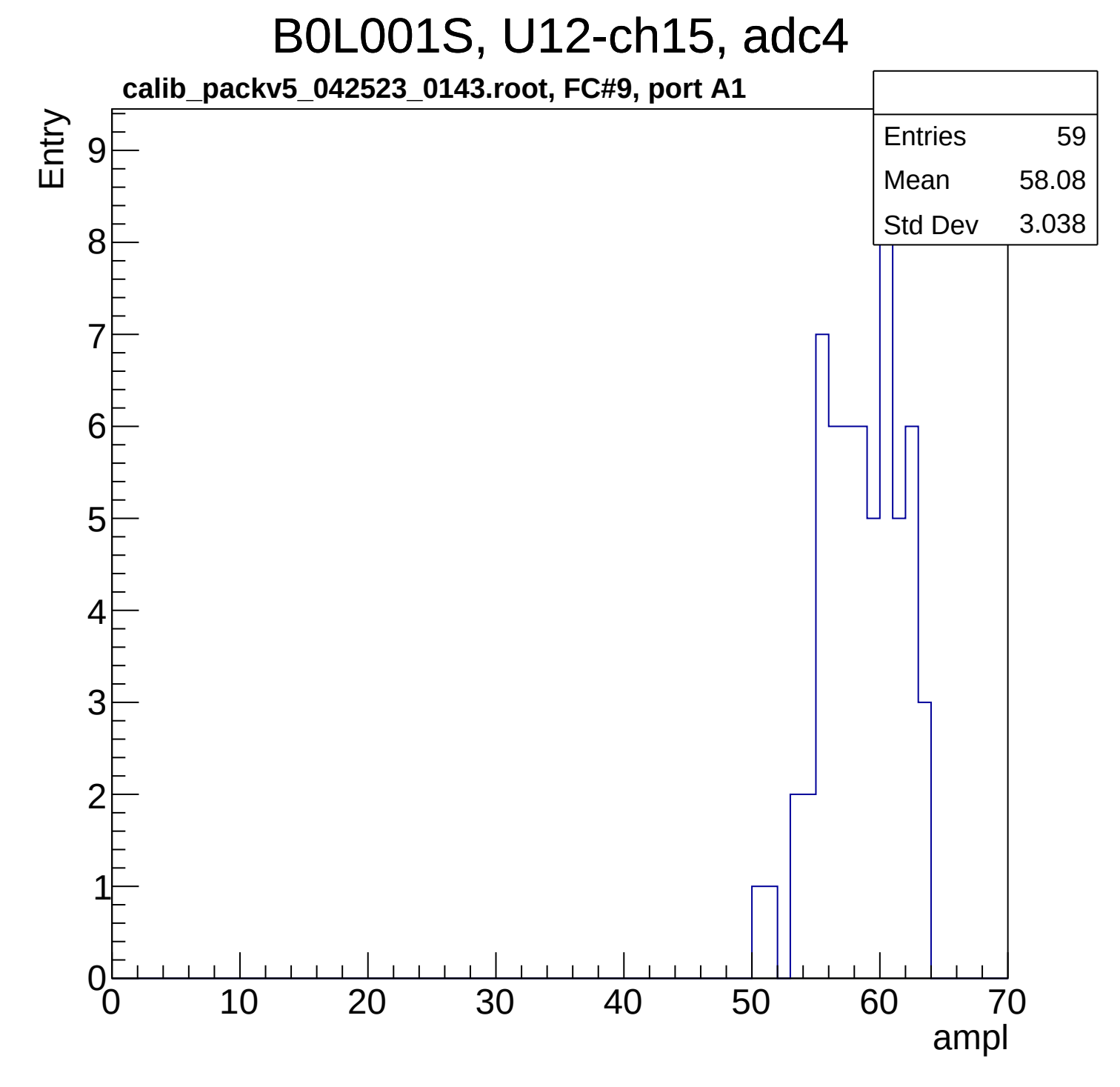
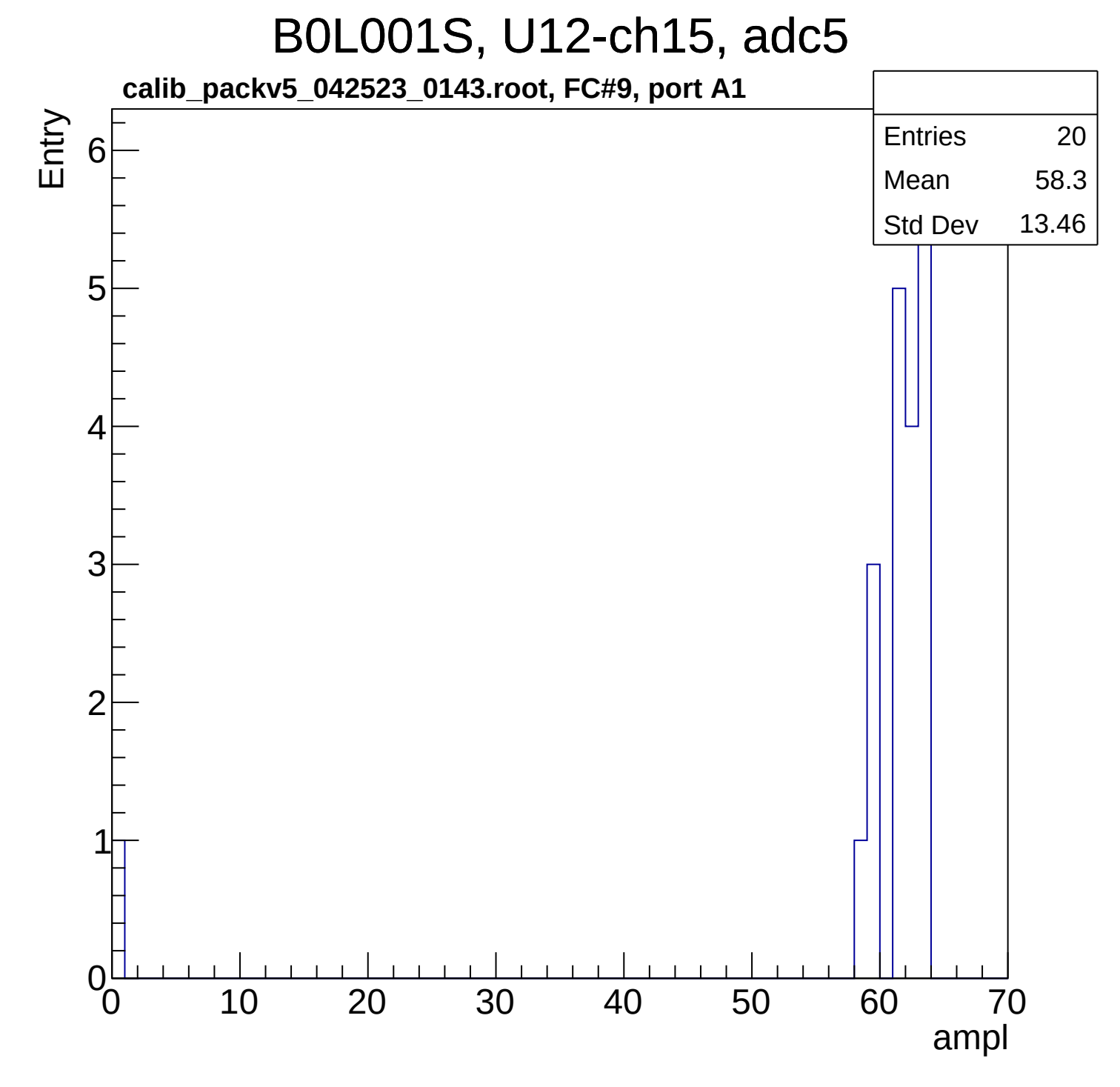
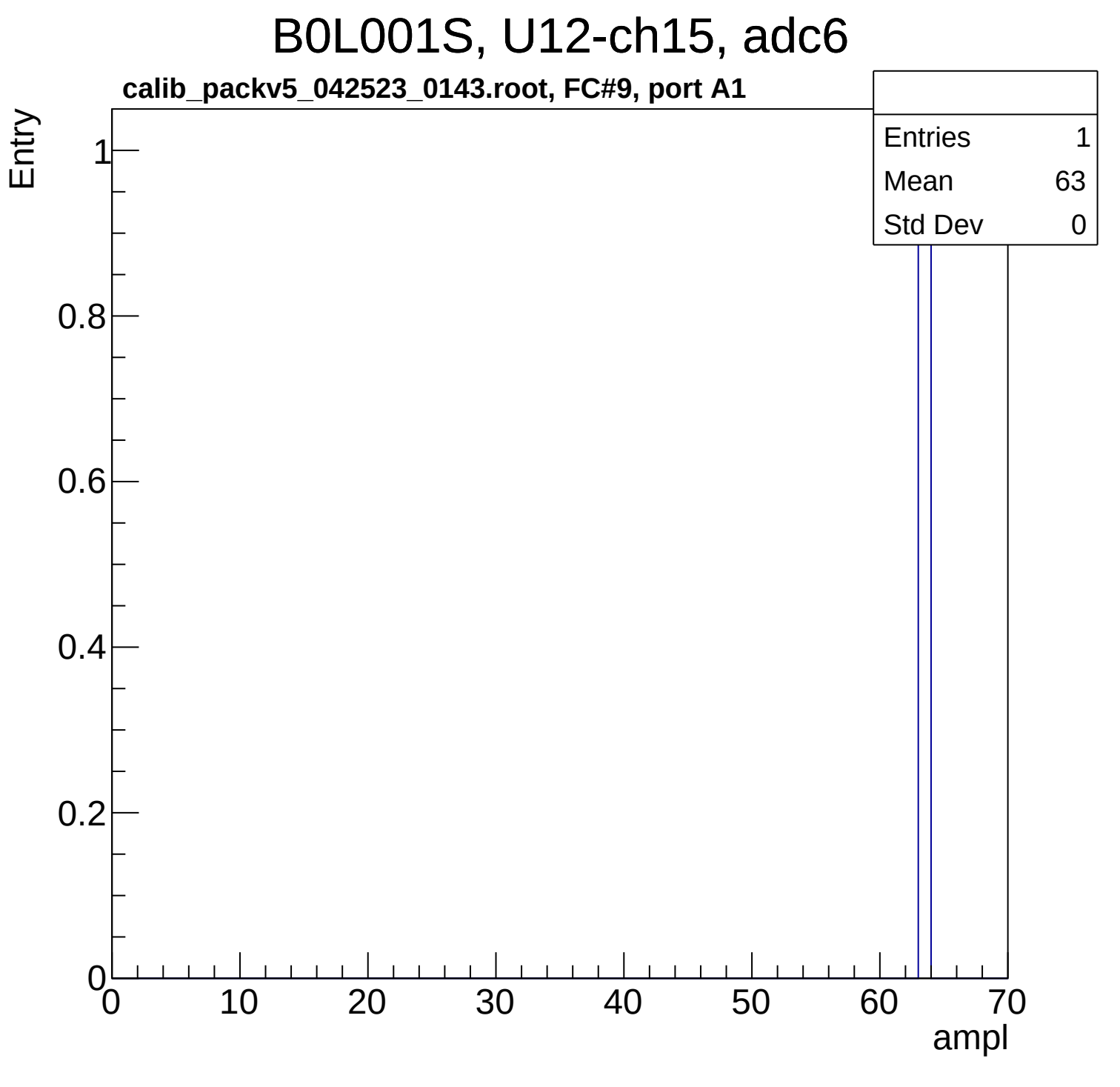
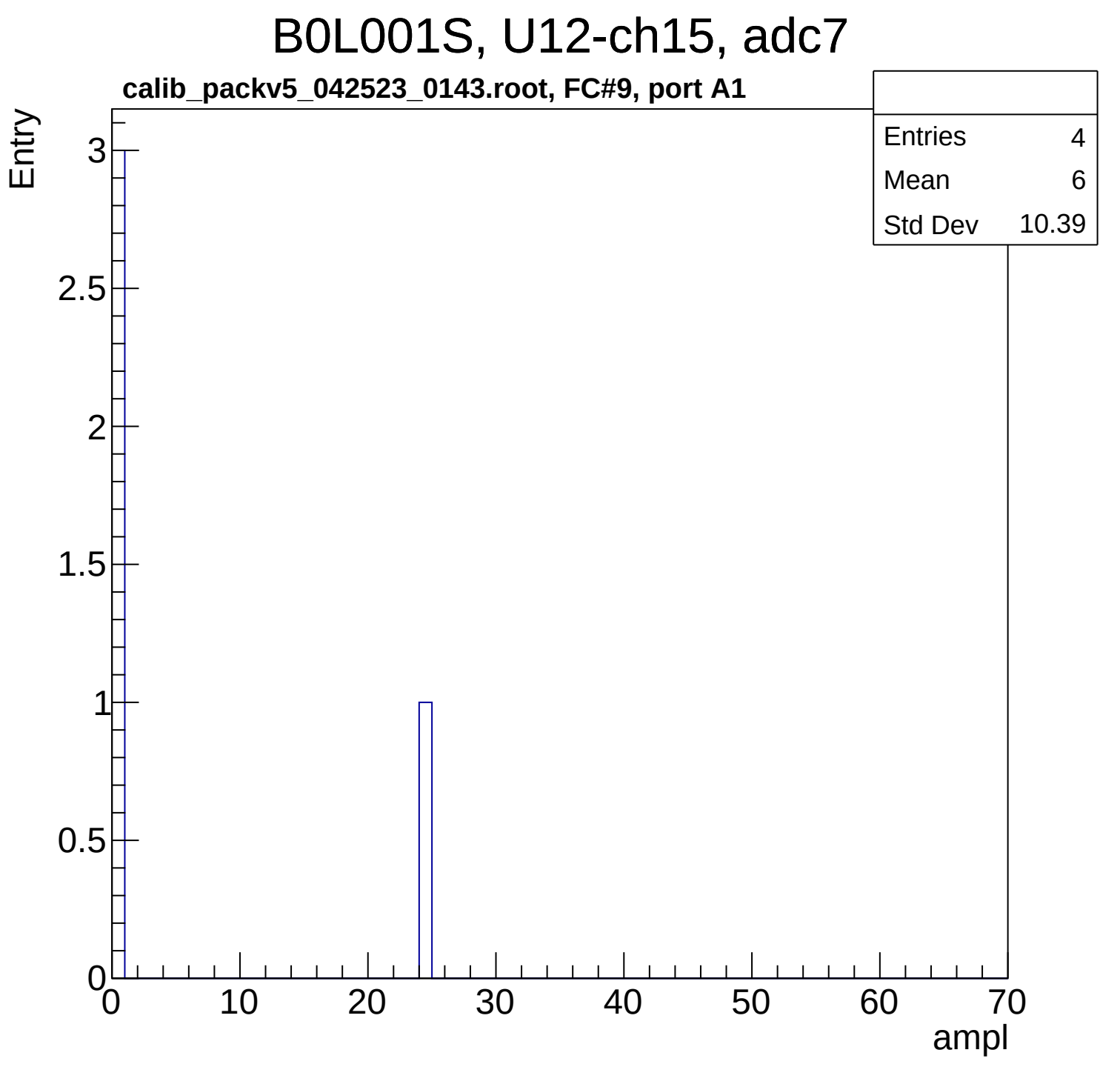
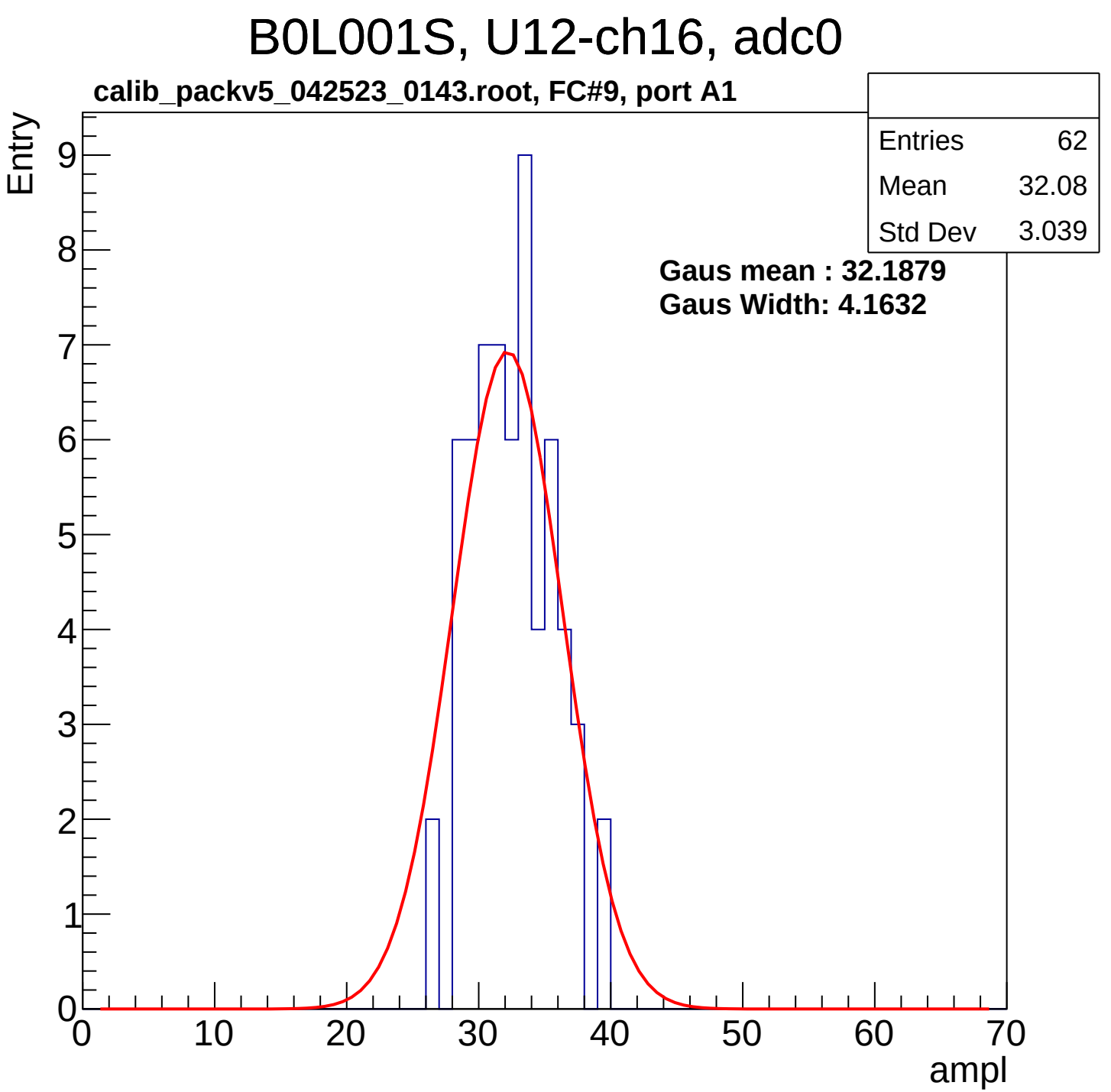
40
50
60
70

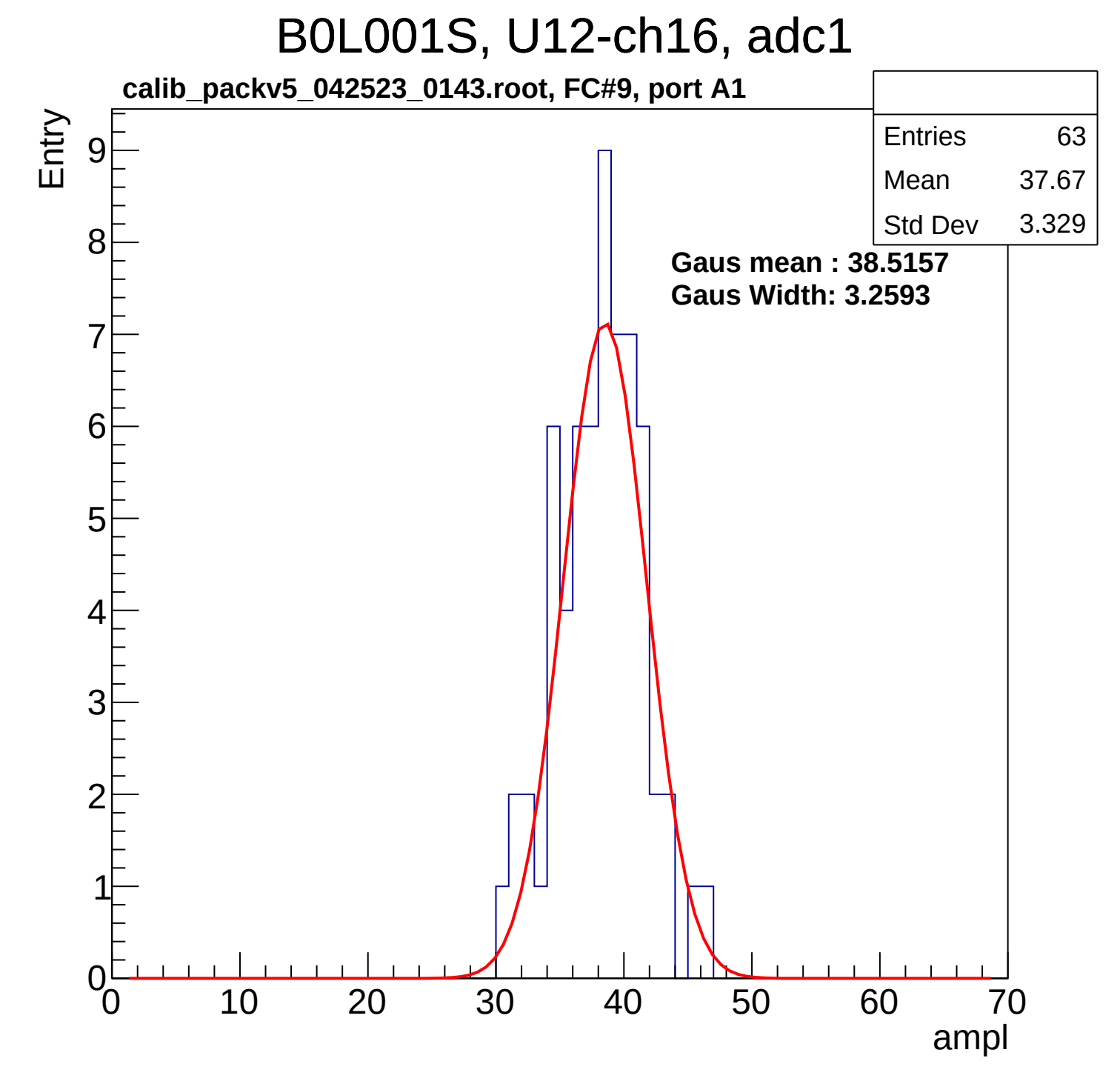

B0L001S, U12-ch15, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 59
Mean 58.08
Std Dev 3.038
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

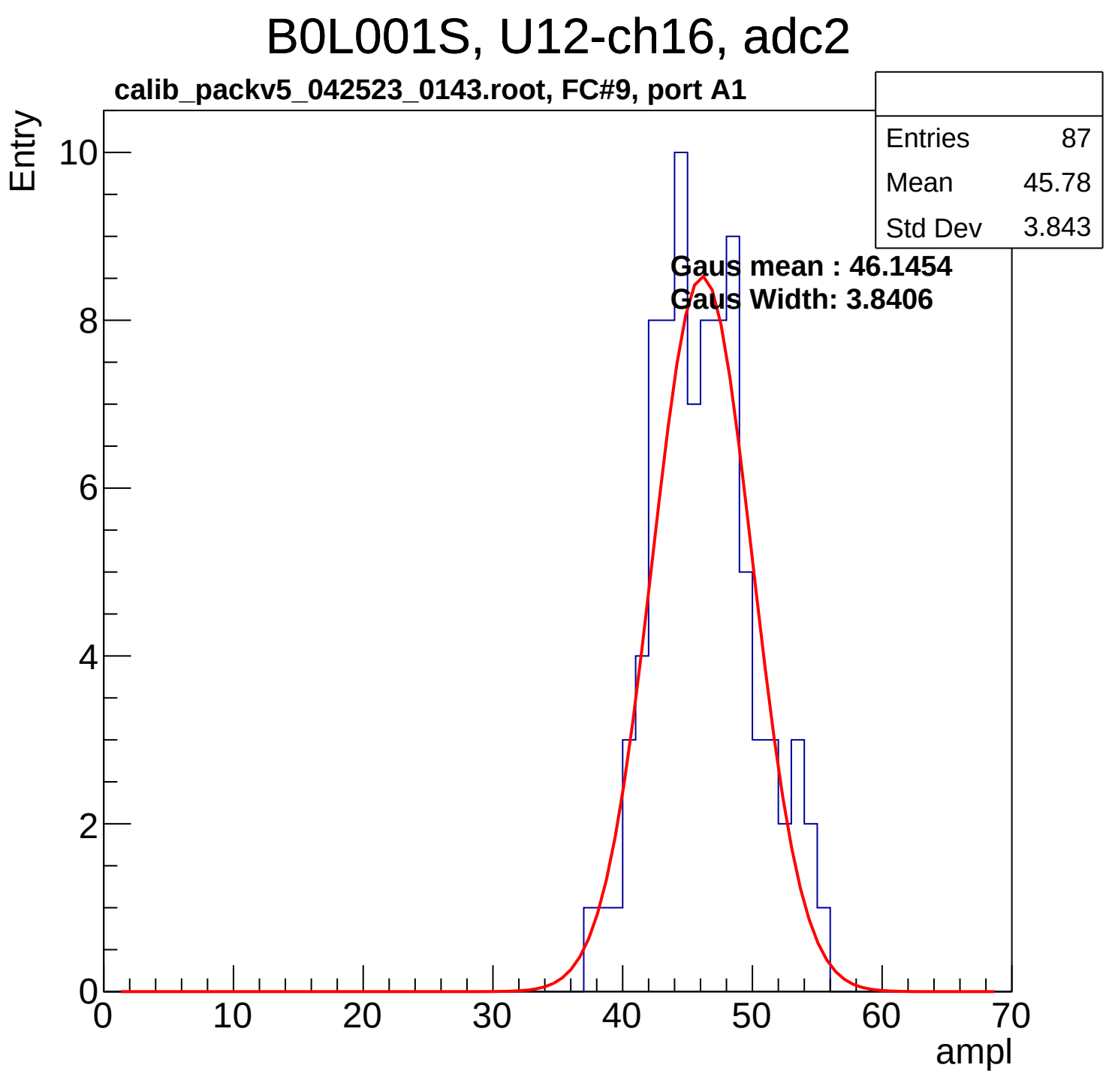

B0L001S, U12-ch15, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 20
Mean 58.3
Std Dev 13.46
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

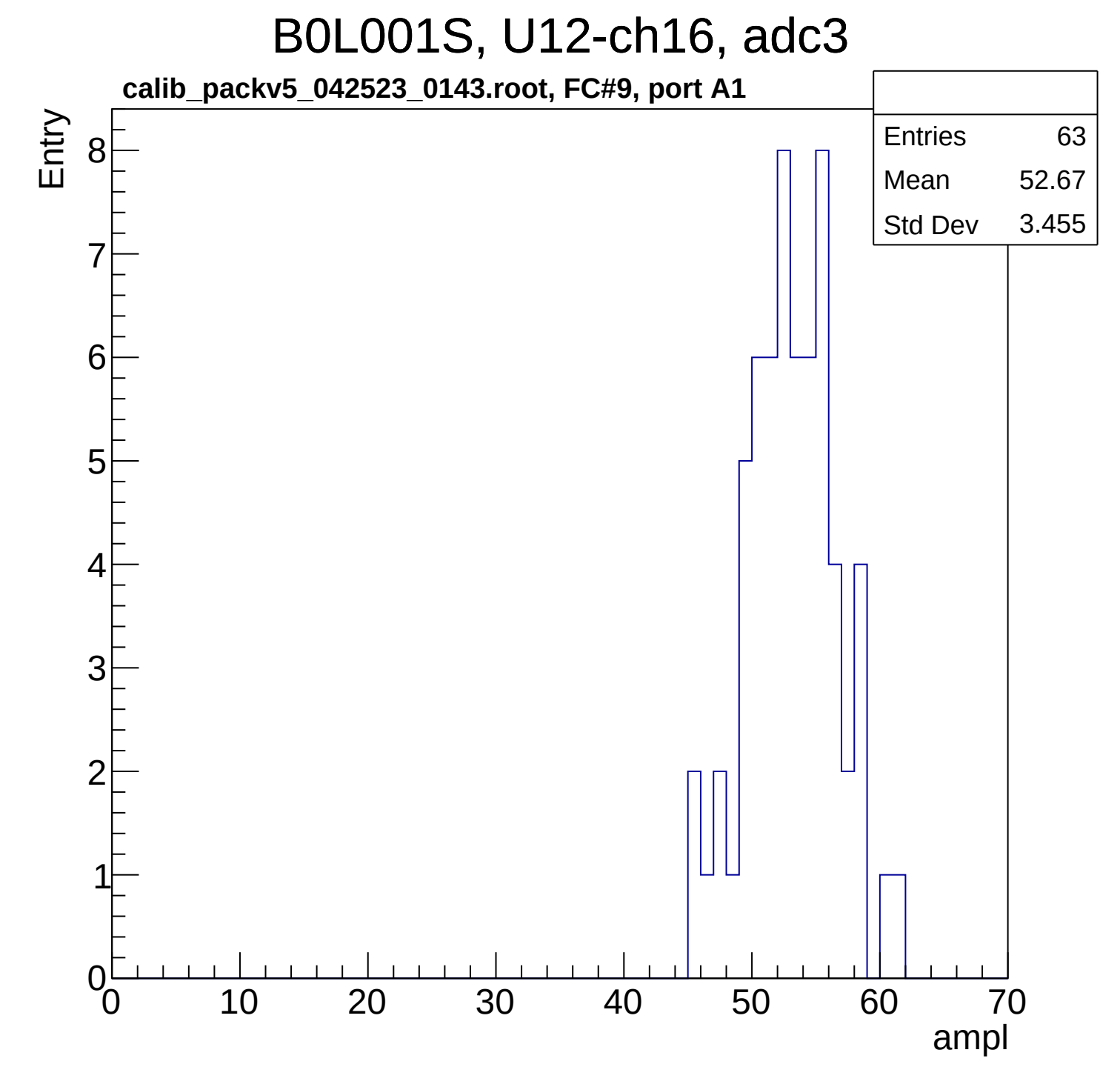

B0L001S, U12-ch15, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

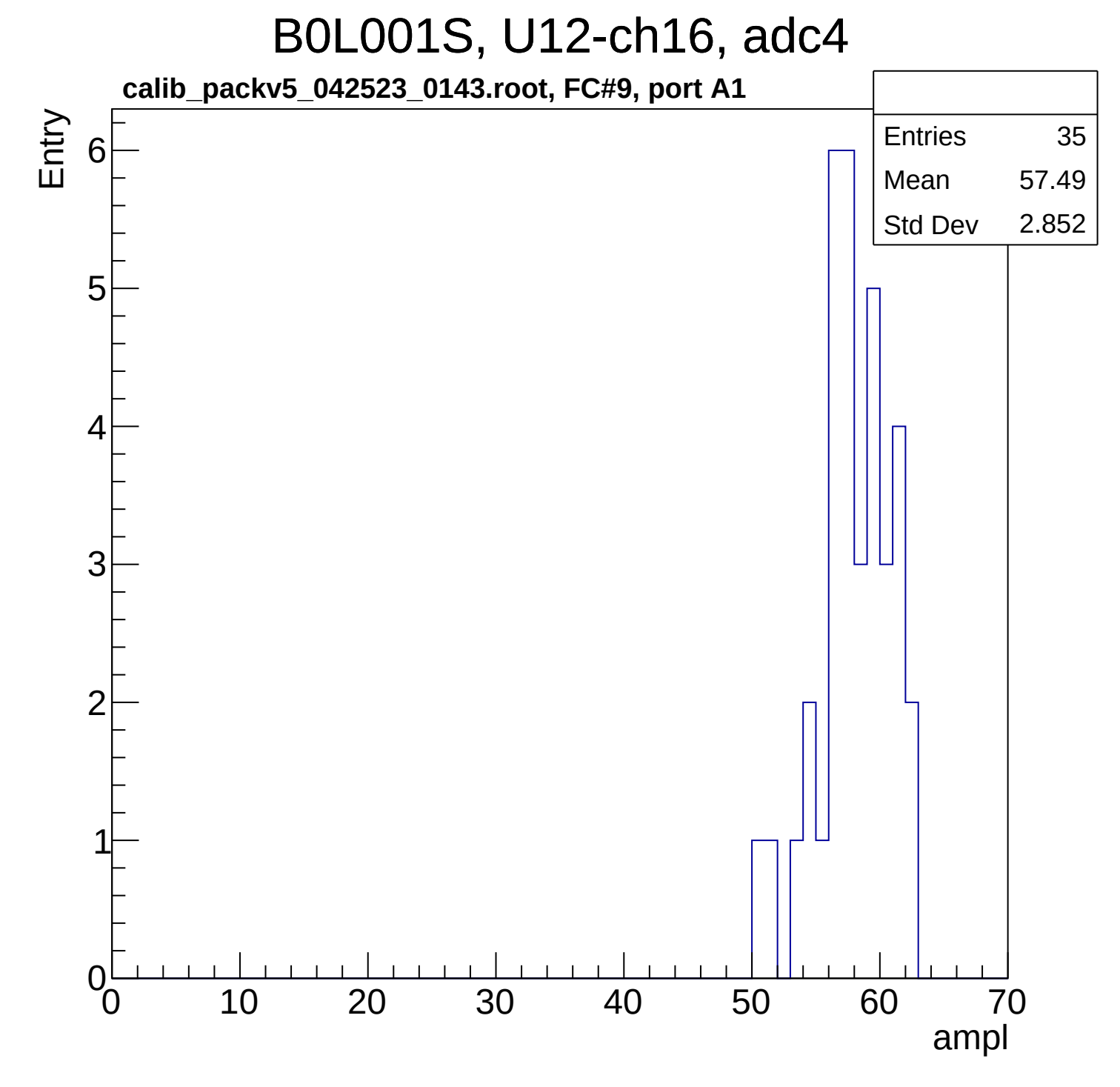

B0L001S, U12-ch15, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 4
Mean 6
Std Dev 10.39
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

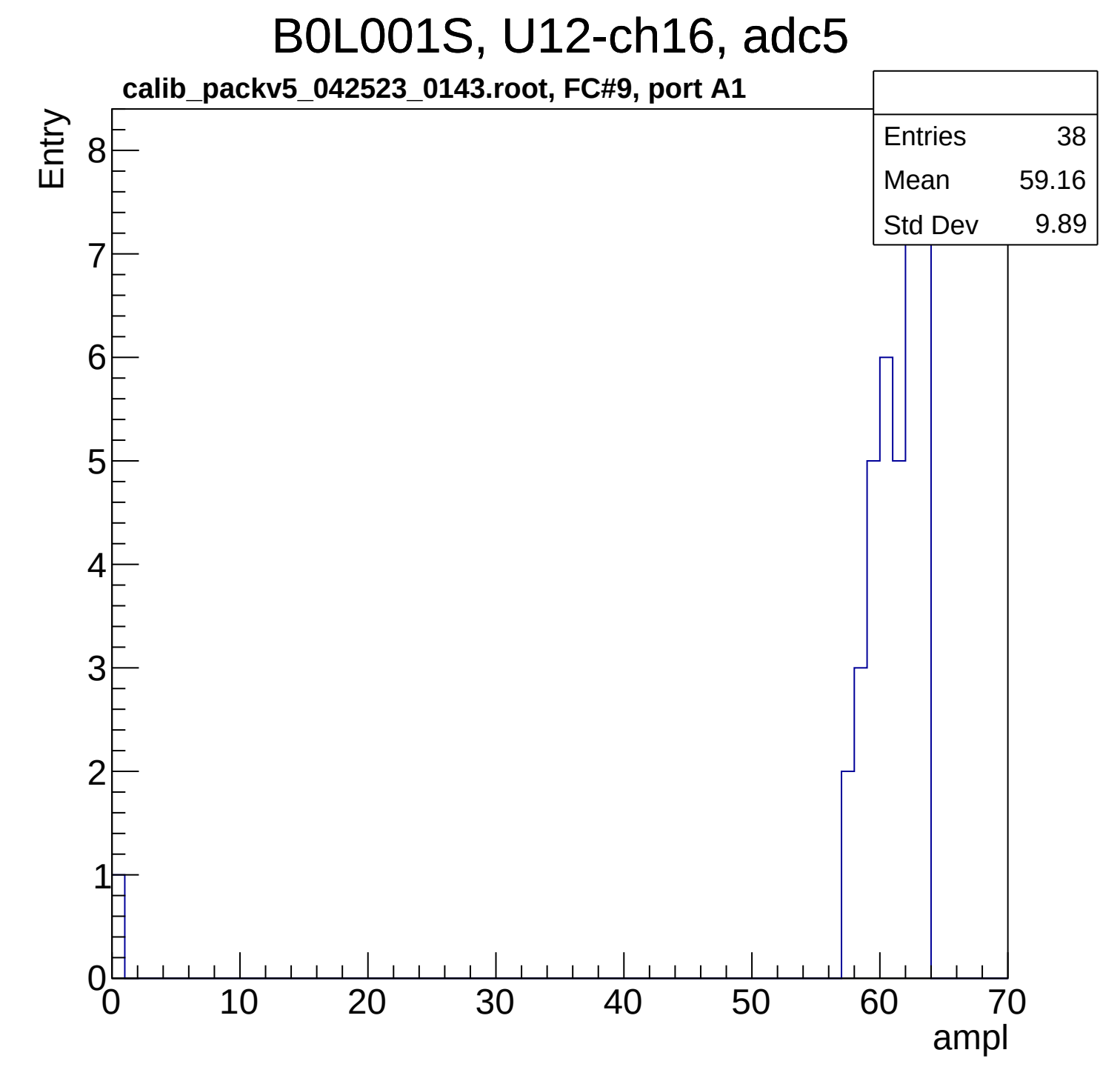

B0L001S, U12-ch16, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 62
Mean 32.08
Std Dev 3.039
Gaus mean : 32.1879
Gaus Width: 4.1632
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

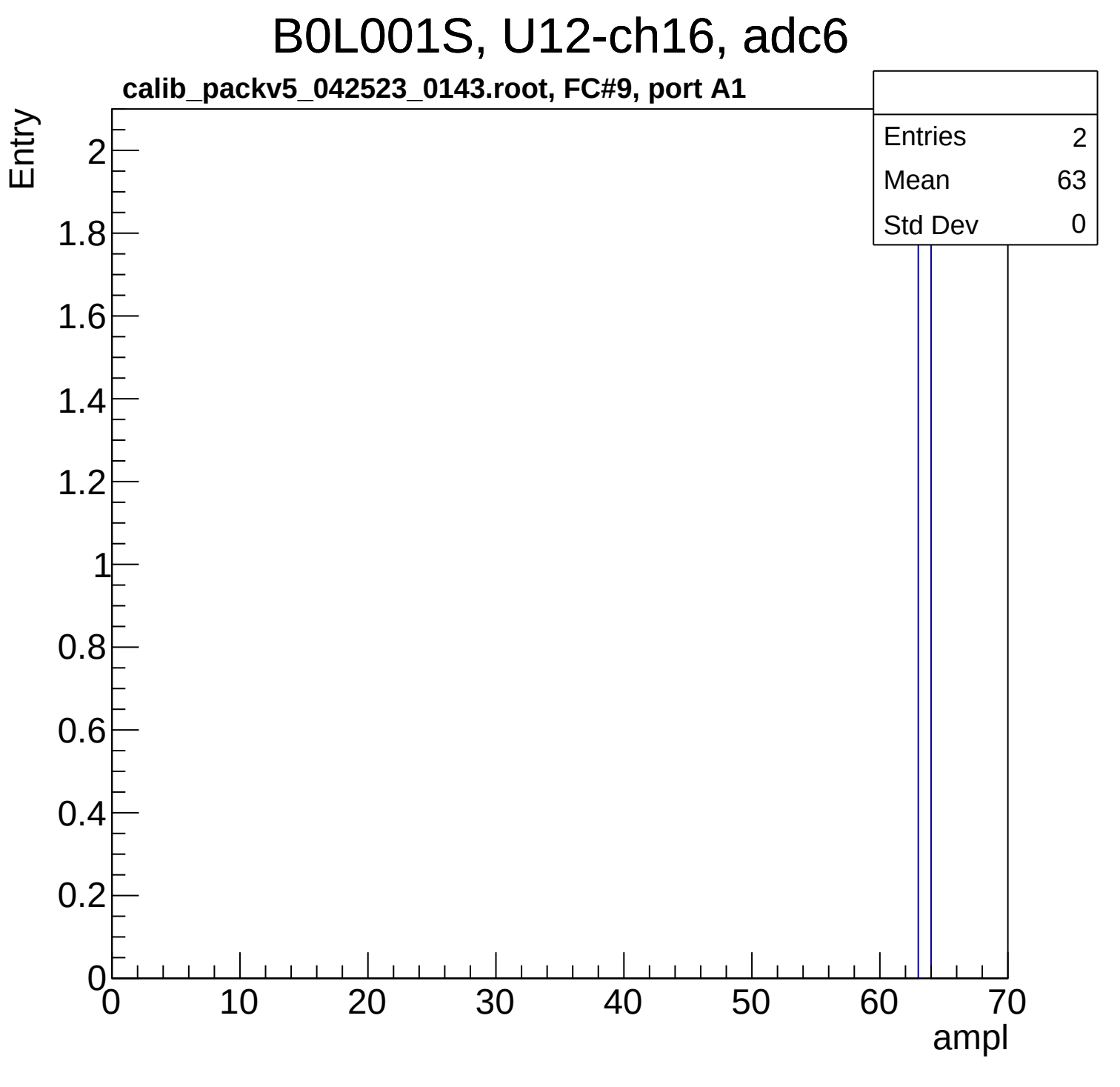

B0L001S, U12-ch16, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 63
Mean 37.67
Std Dev 3.329
Gaus mean : 38.5157
Gaus Width: 3.2593
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

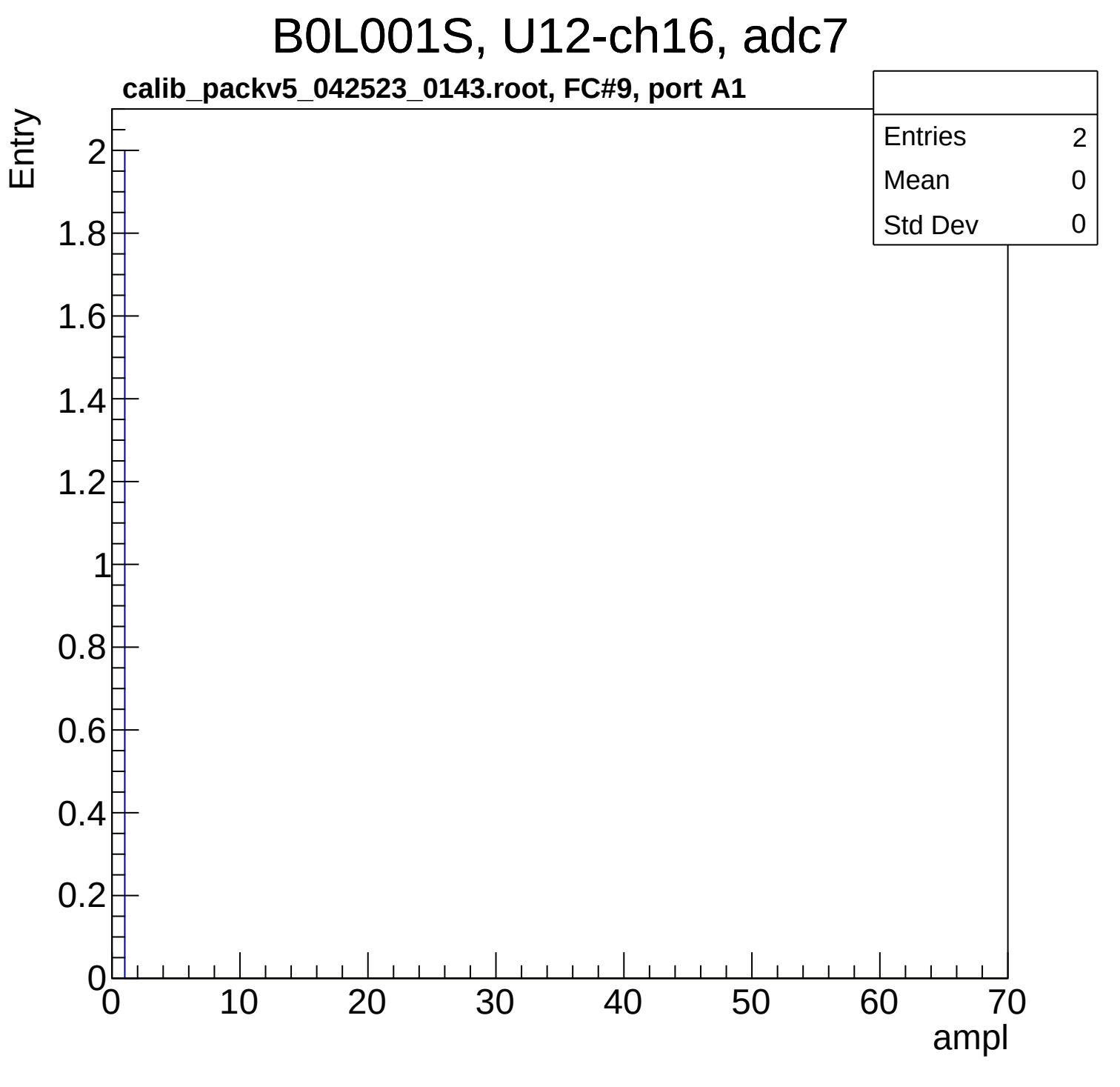

B0L001S, U12-ch16, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 87
Mean 45.78
Std Dev 3.843
Gaus mean : 46.1454
Gaus Width: 3.8406
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

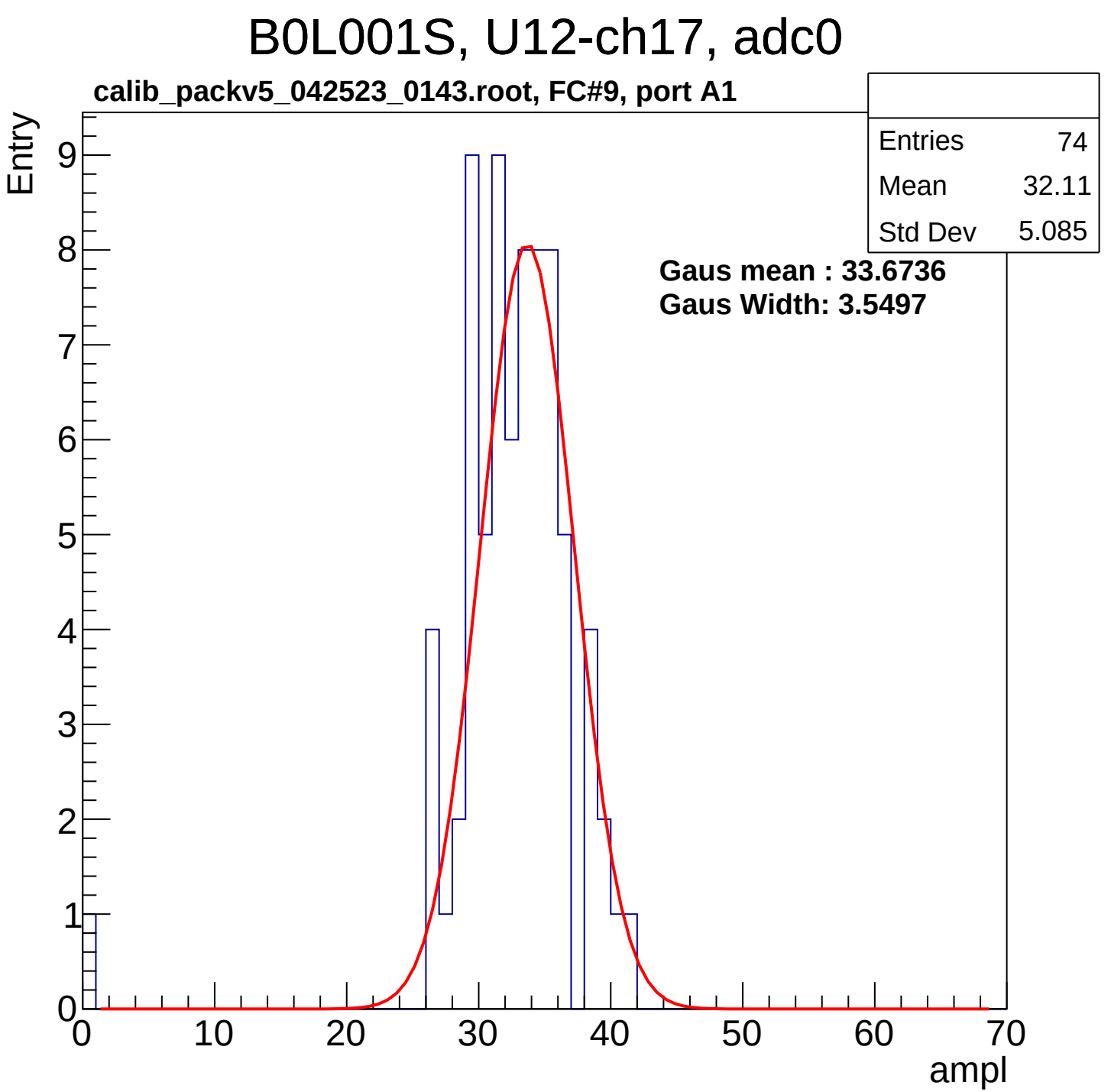

B0L001S, U12-ch16, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 63
Mean 52.67
Std Dev 3.455
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

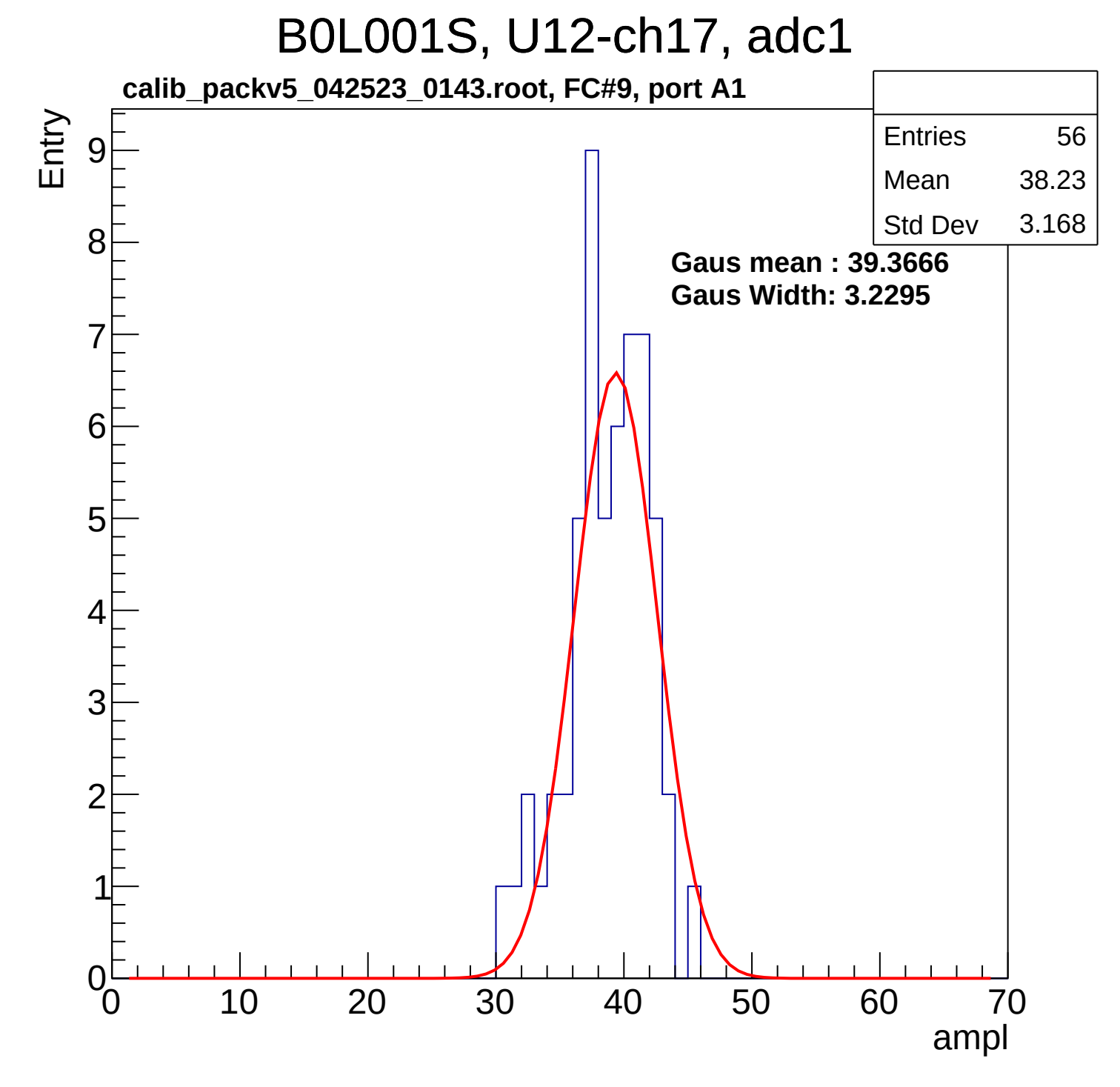

B0L001S, U12-ch16, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 35
Mean 57.49
Std Dev 2.852
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

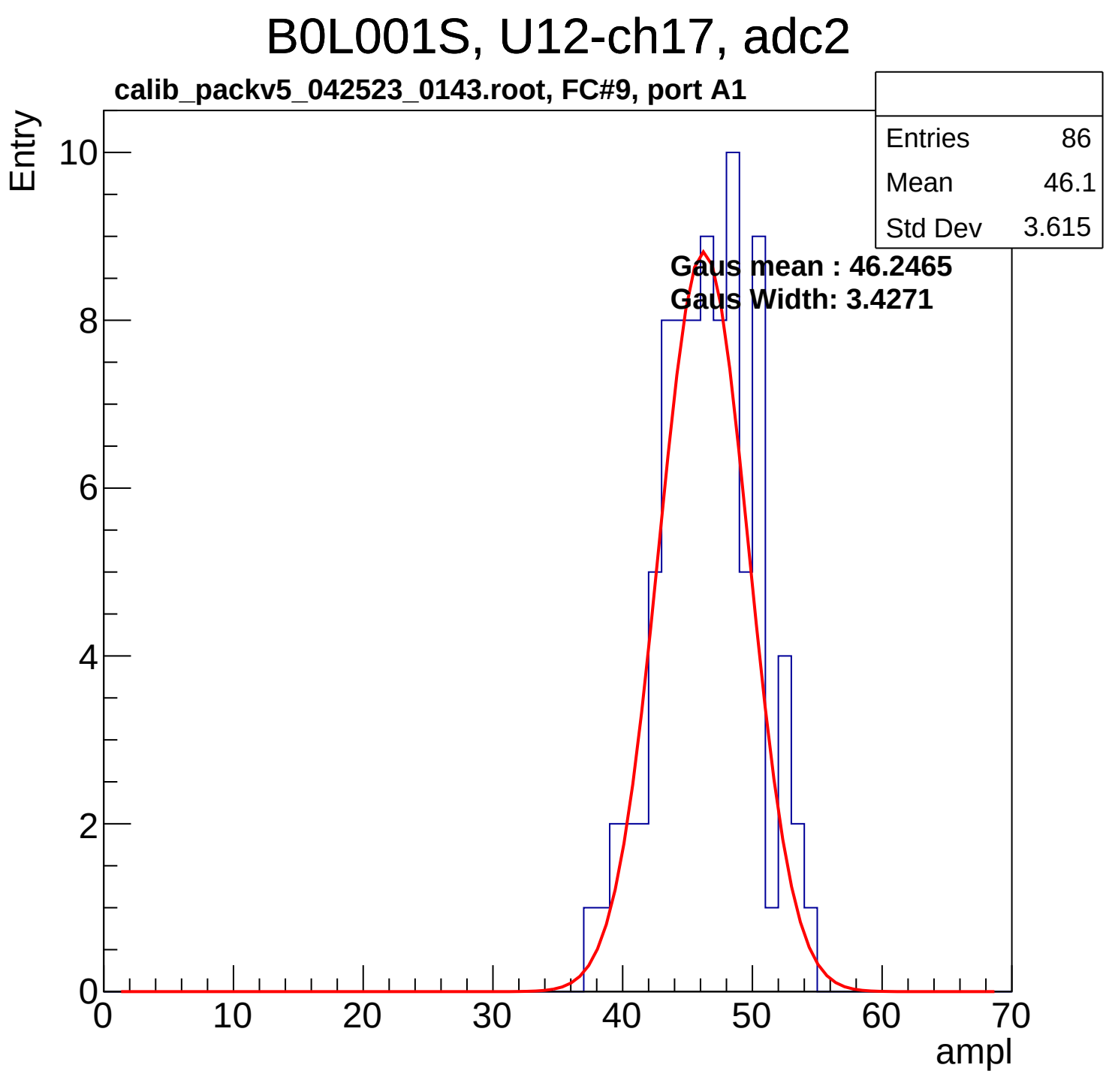

B0L001S, U12-ch16, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 38
Mean 59.16
Std Dev 9.89
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

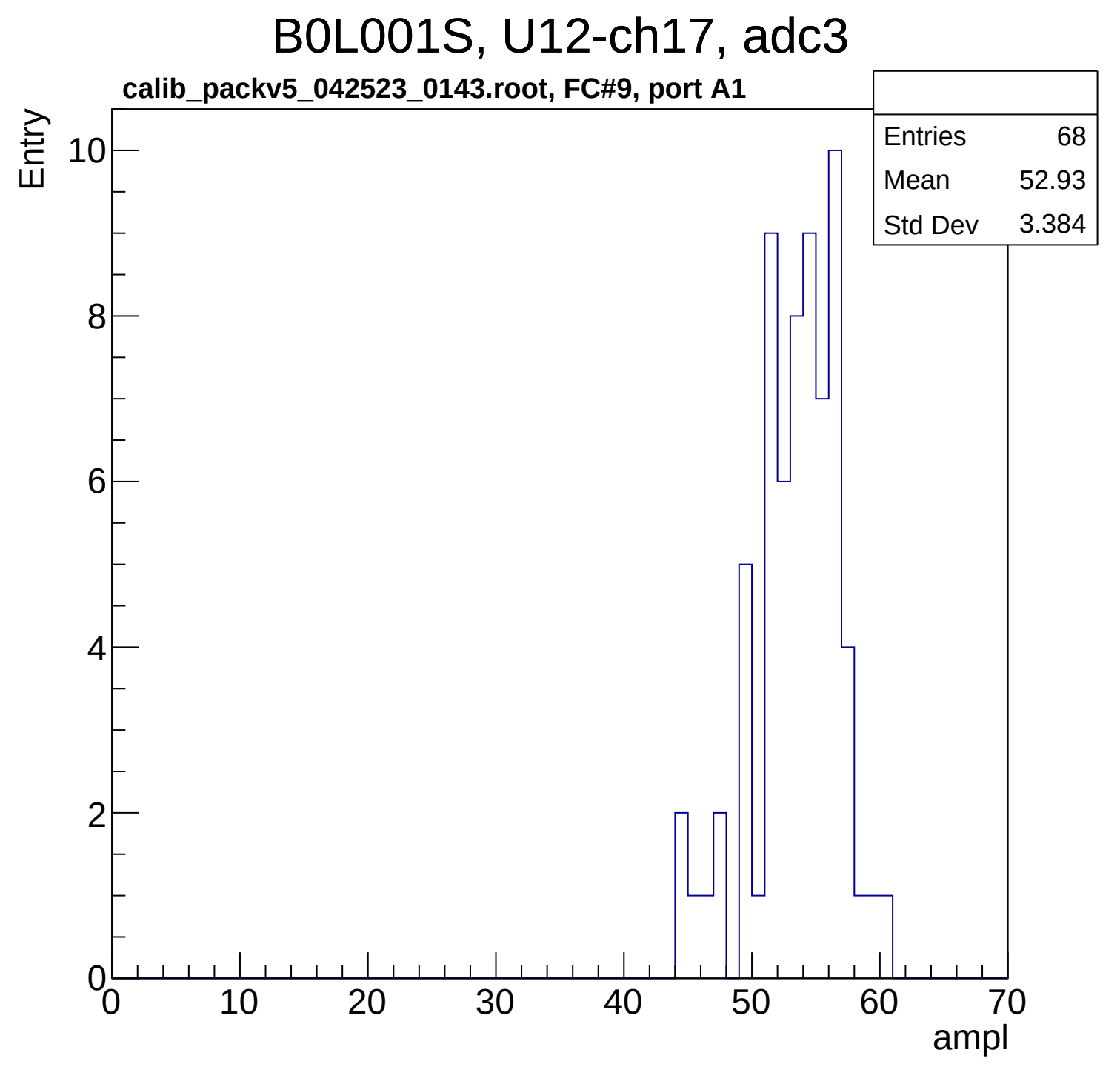

B0L001S, U12-ch16, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

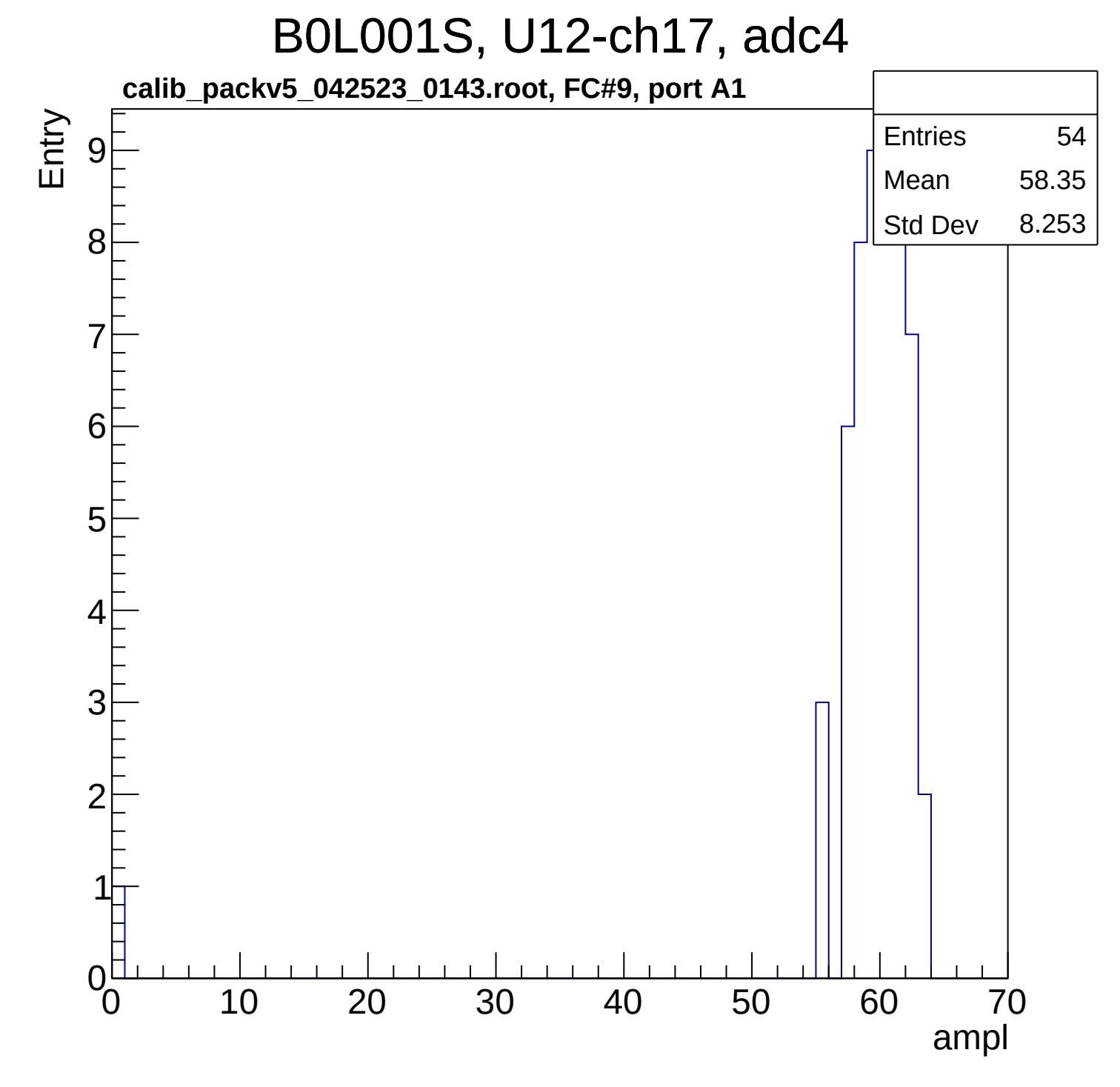

B0L001S, U12-ch16, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch17, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 74
Mean 32.11
Std Dev 5.085
Gaus mean : 33.6736
Gaus Width: 3.5497
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch17, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 56
Mean 38.23
Std Dev 3.168
Gaus mean : 39.3666
Gaus Width: 3.2295
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch17, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 86
Mean 46.1
Std Dev 3.615
Gaus mean : 46.2465
Gaus Width: 3.4271
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch17, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 68
Mean 52.93
Std Dev 3.384
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch17, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 54
Mean 58.35
Std Dev 8.253
Entry
ampl
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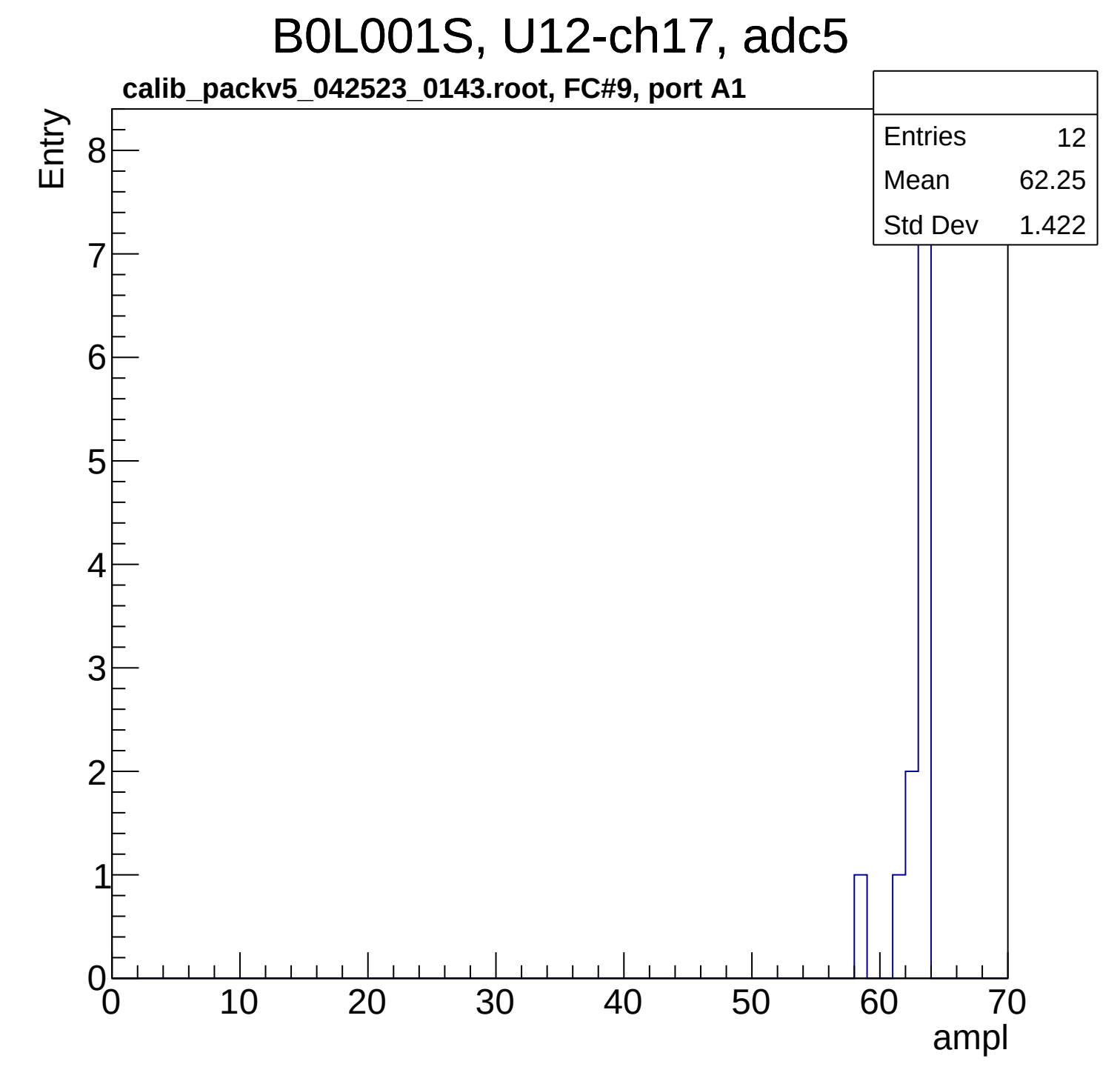
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch17, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 12
Mean 62.25
Std Dev 1.422
Entry
ampl
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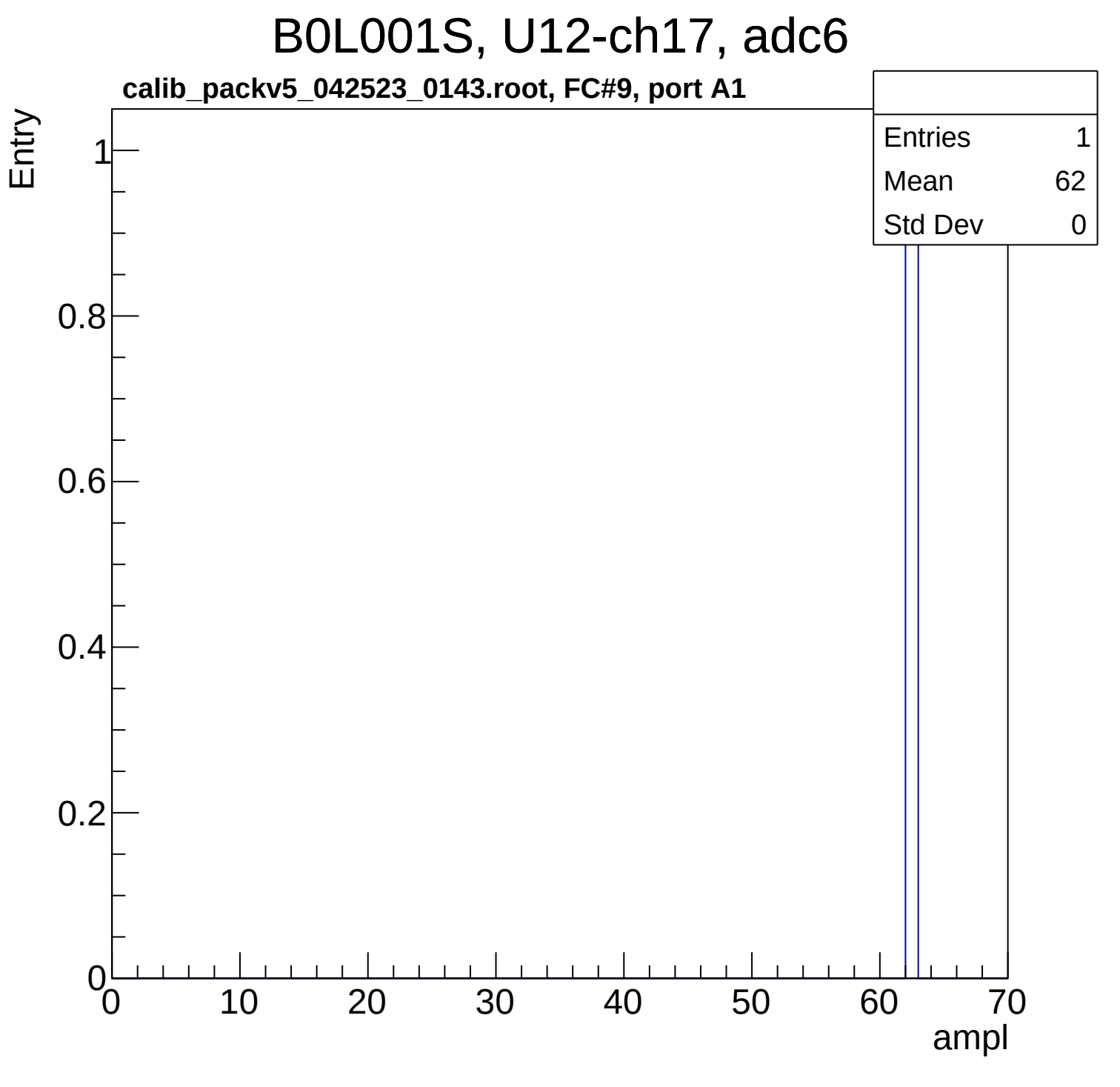
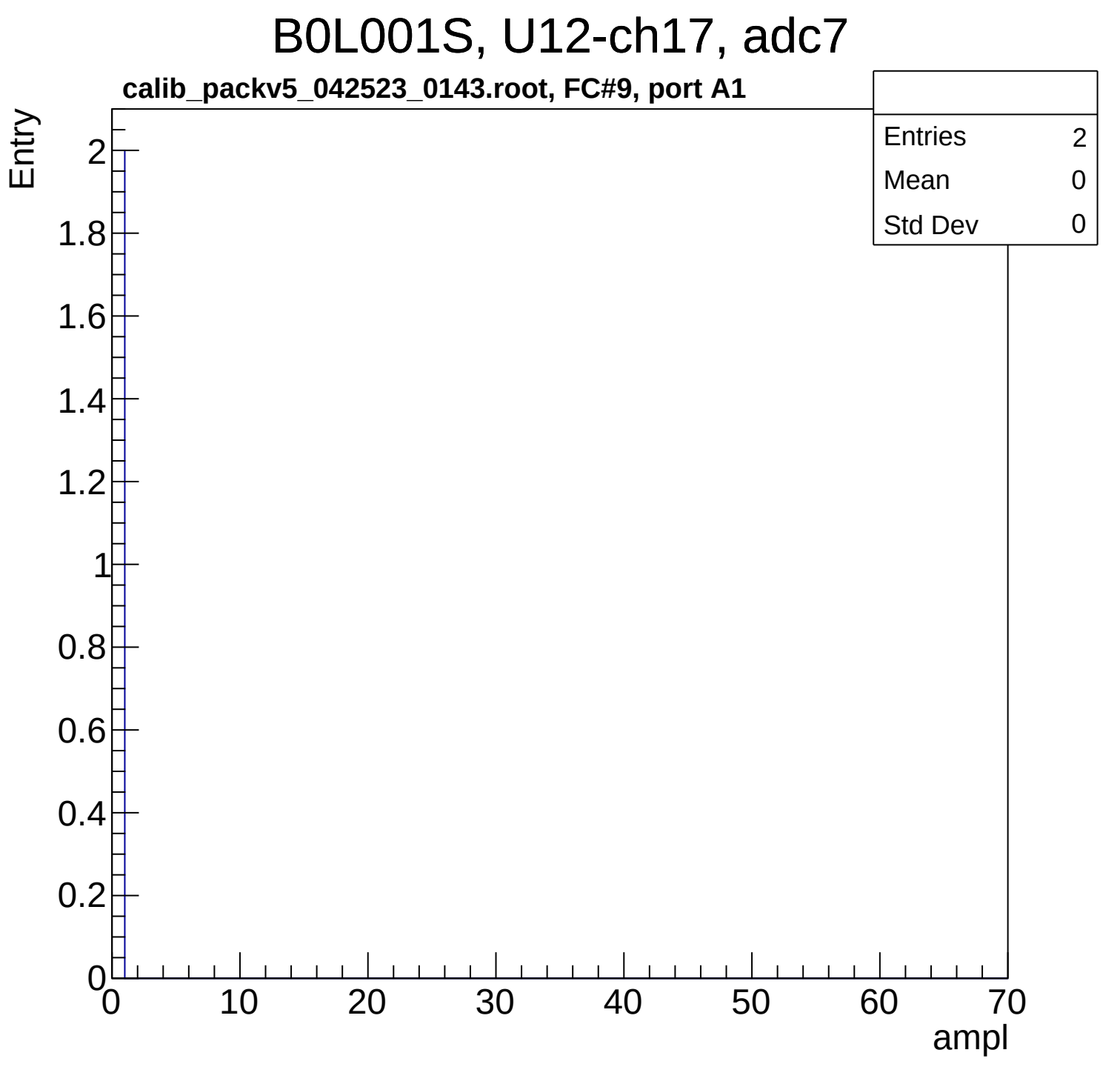
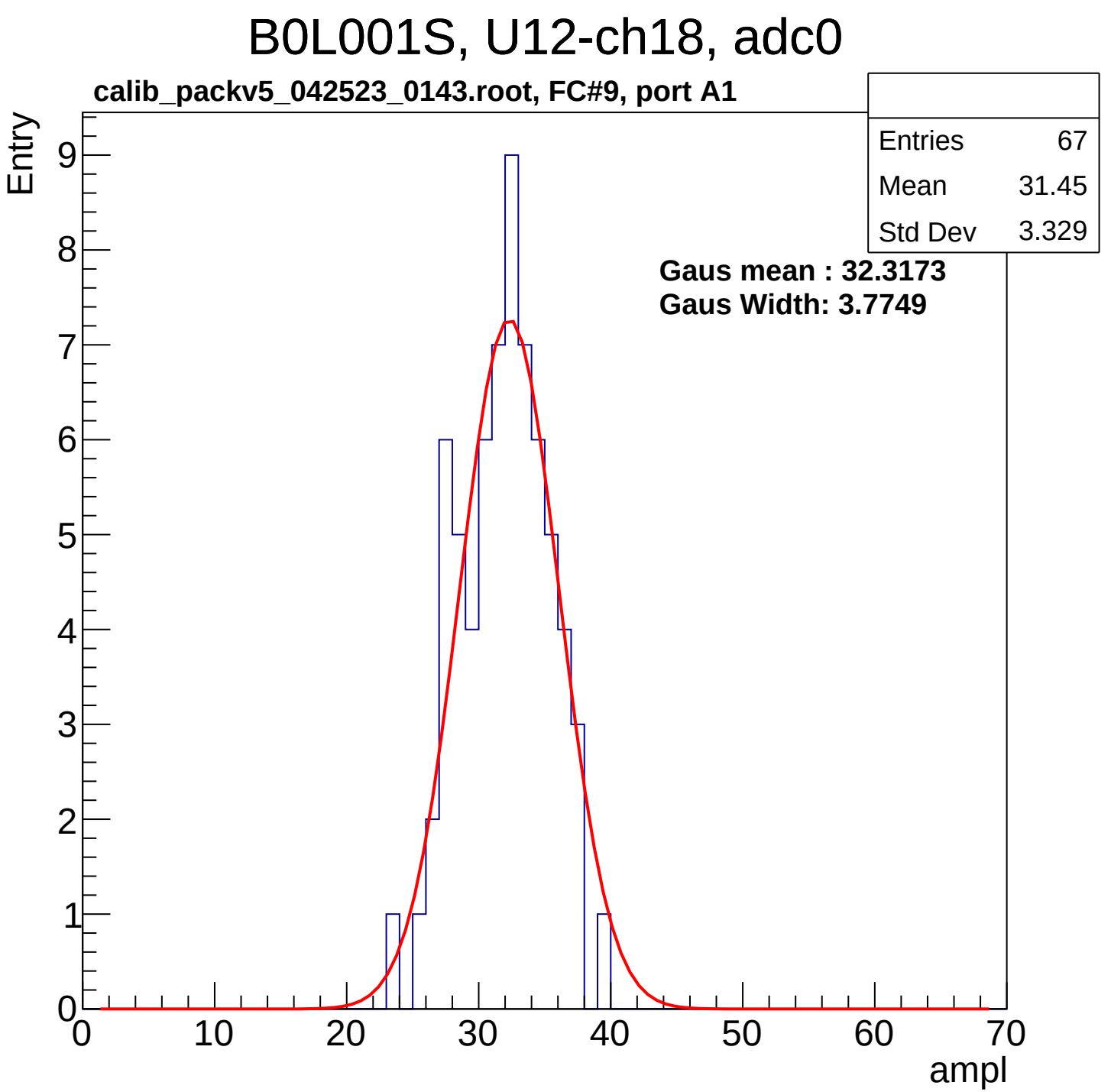
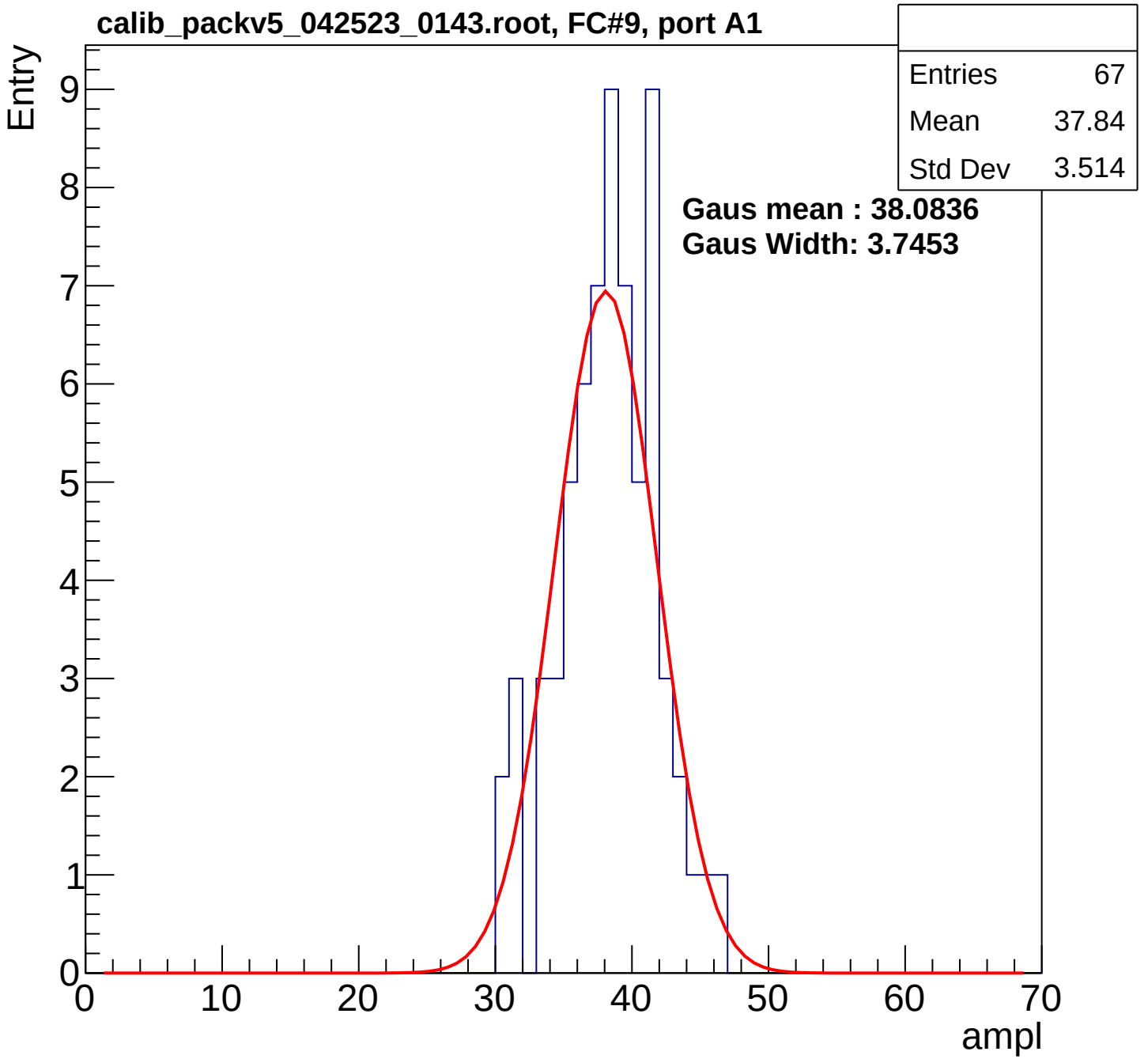
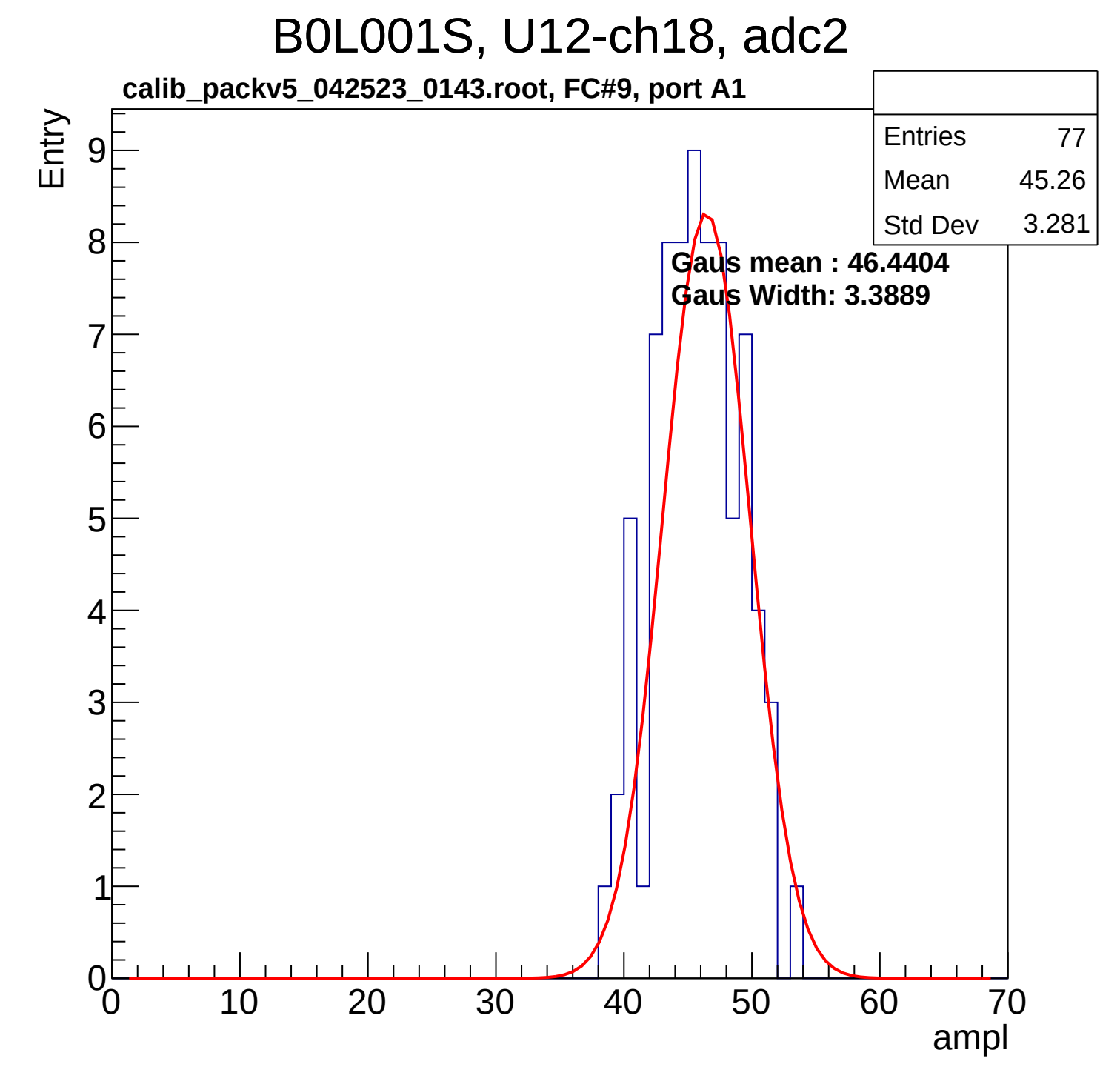
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch17, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch17, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch18, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 67
Mean 31.45
Std Dev 3.329
Gaus mean : 32.3173
Gaus Width: 3.7749
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch18, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 67
Mean 37.84
Std Dev 3.514
Gaus mean : 38.0836
Gaus Width: 3.7453
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch18, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 77
Mean 45.26
Std Dev 3.281
Gaus mean : 46.4404
Gaus Width: 3.3889
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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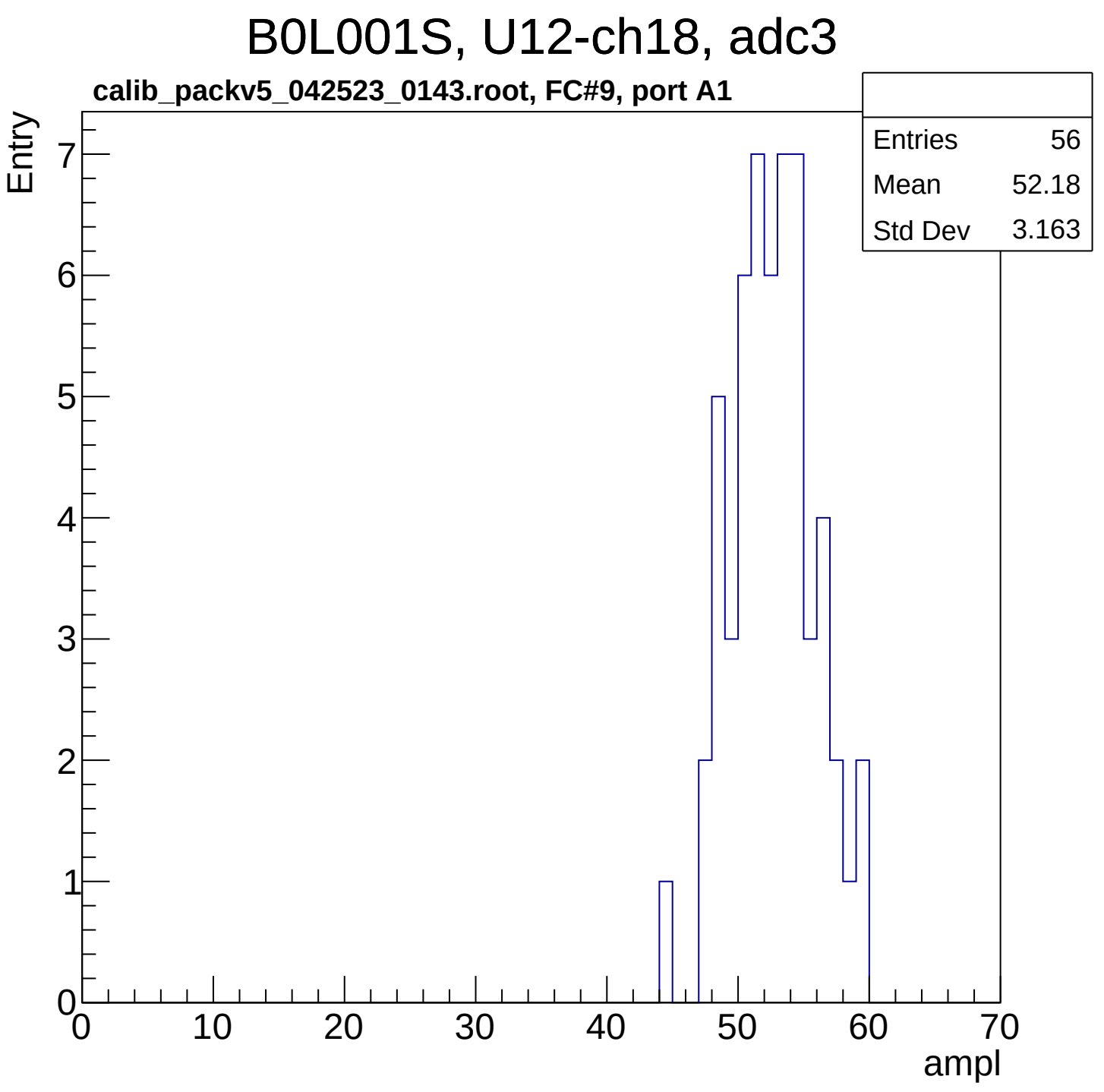
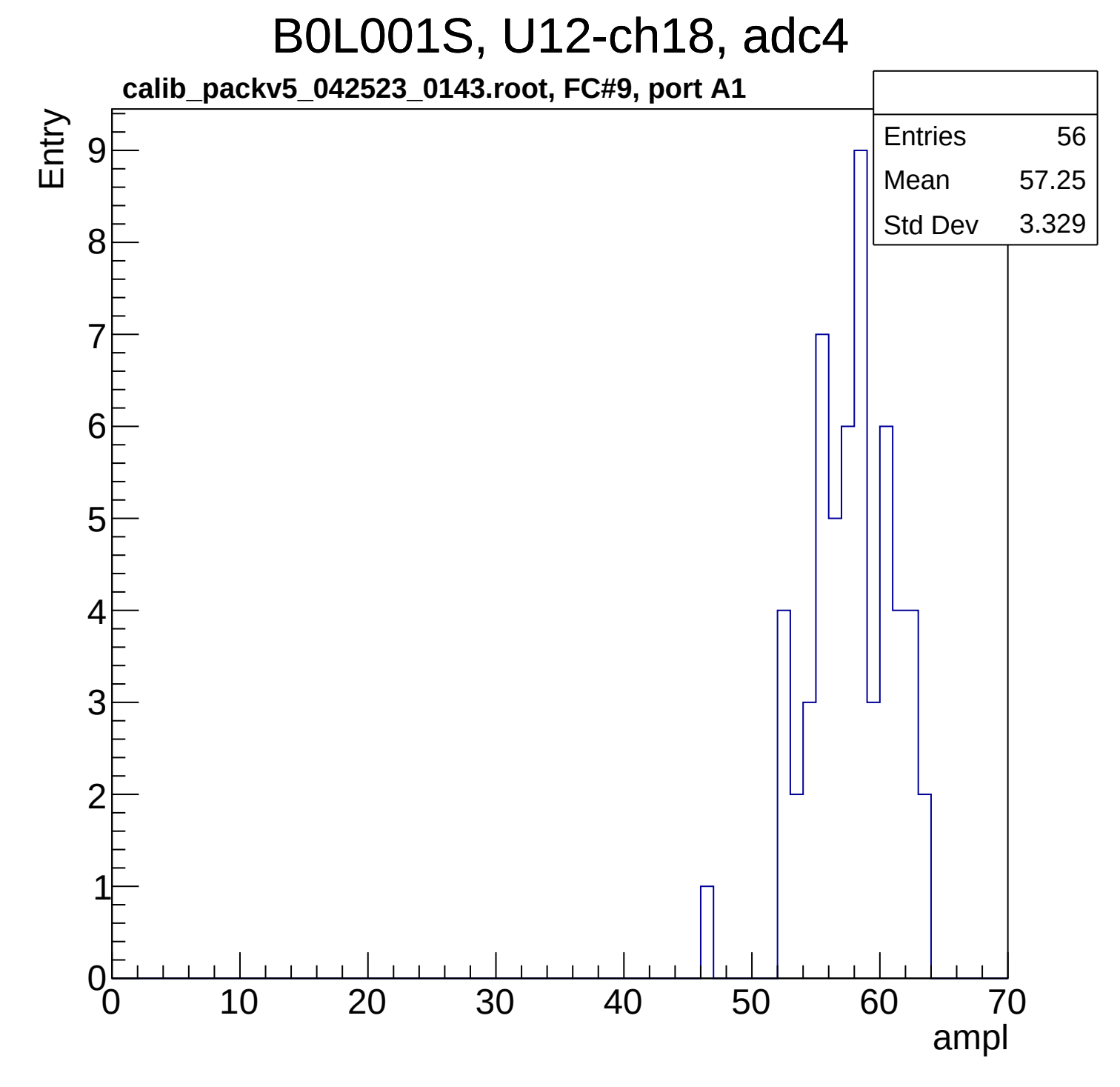

B0L001S, U12-ch18, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 56
Mean 52.18
Std Dev 3.163
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch18, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 56
Mean 57.25
Std Dev 3.329
Entry
ampl
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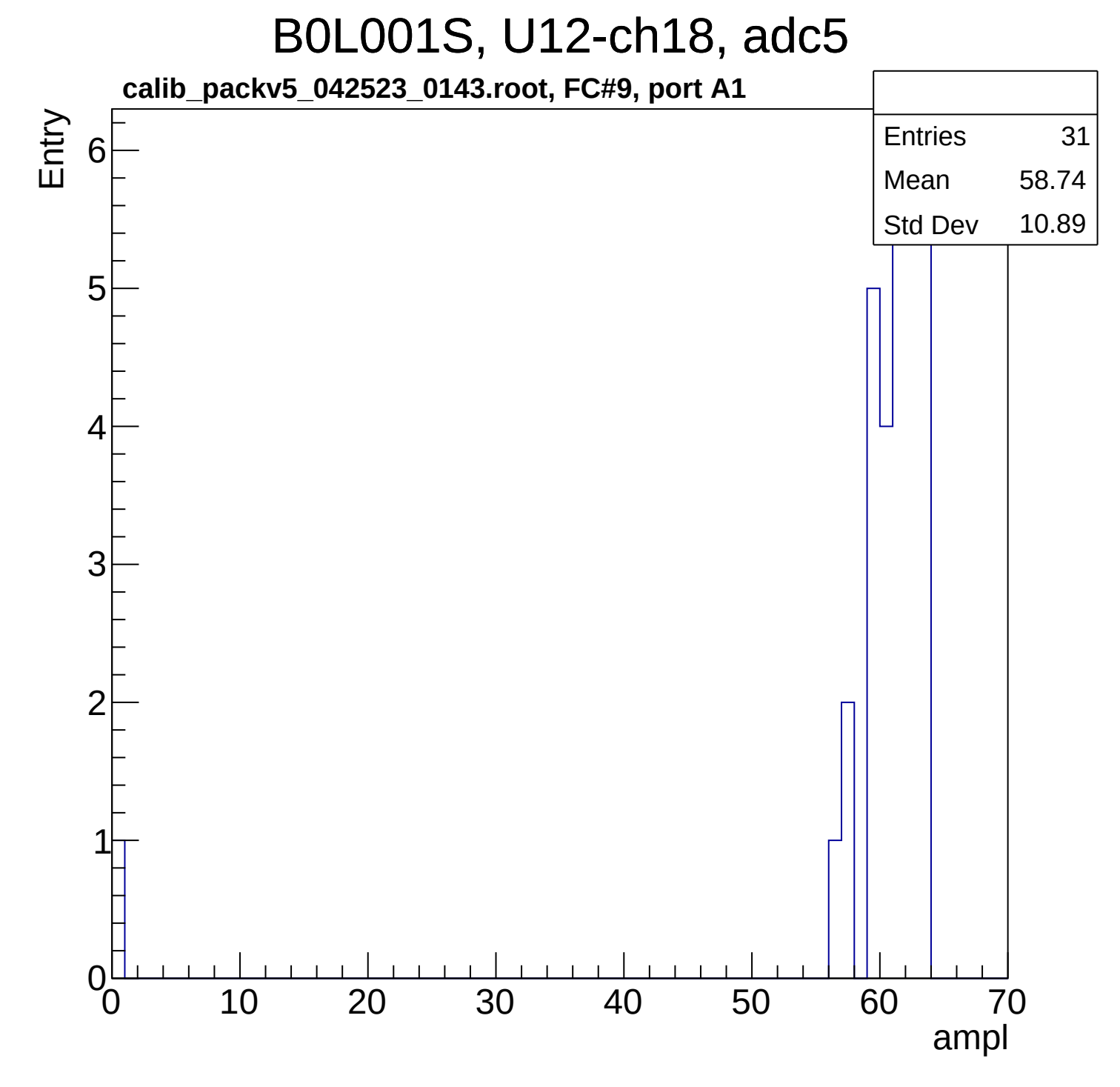
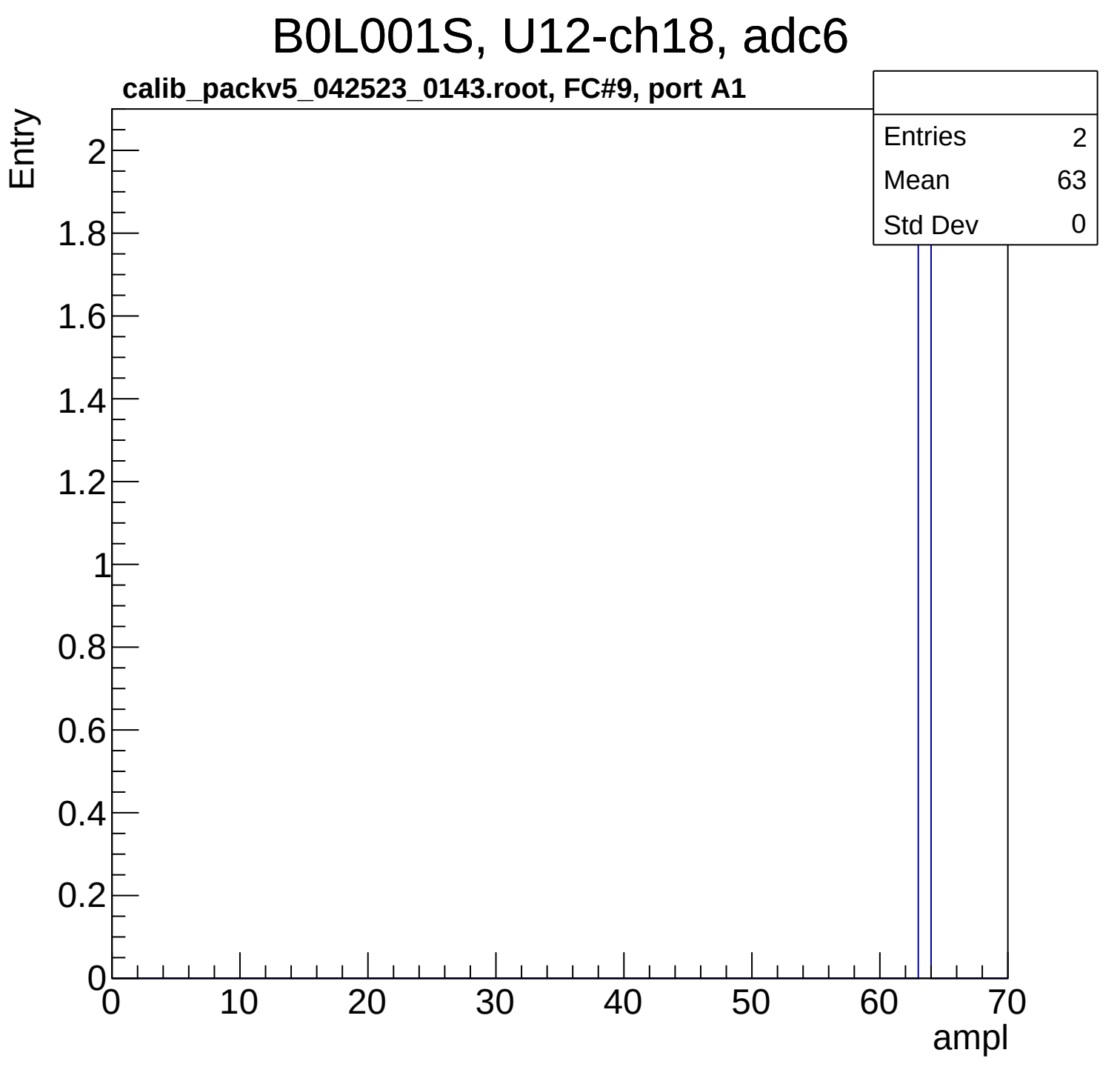
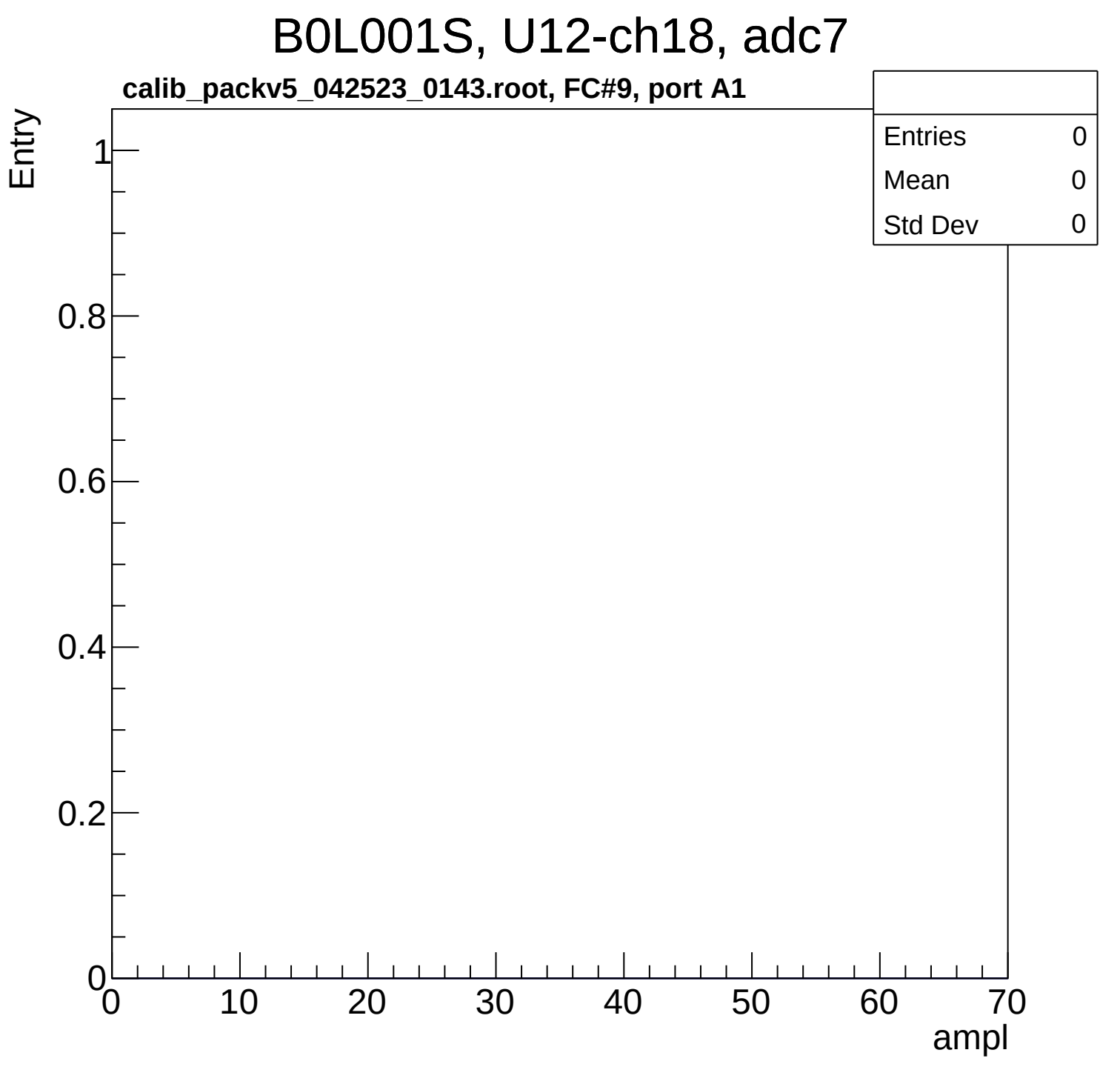
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch18, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 31
Mean 58.74
Std Dev 10.89
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch18, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L001S, U12-ch18, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
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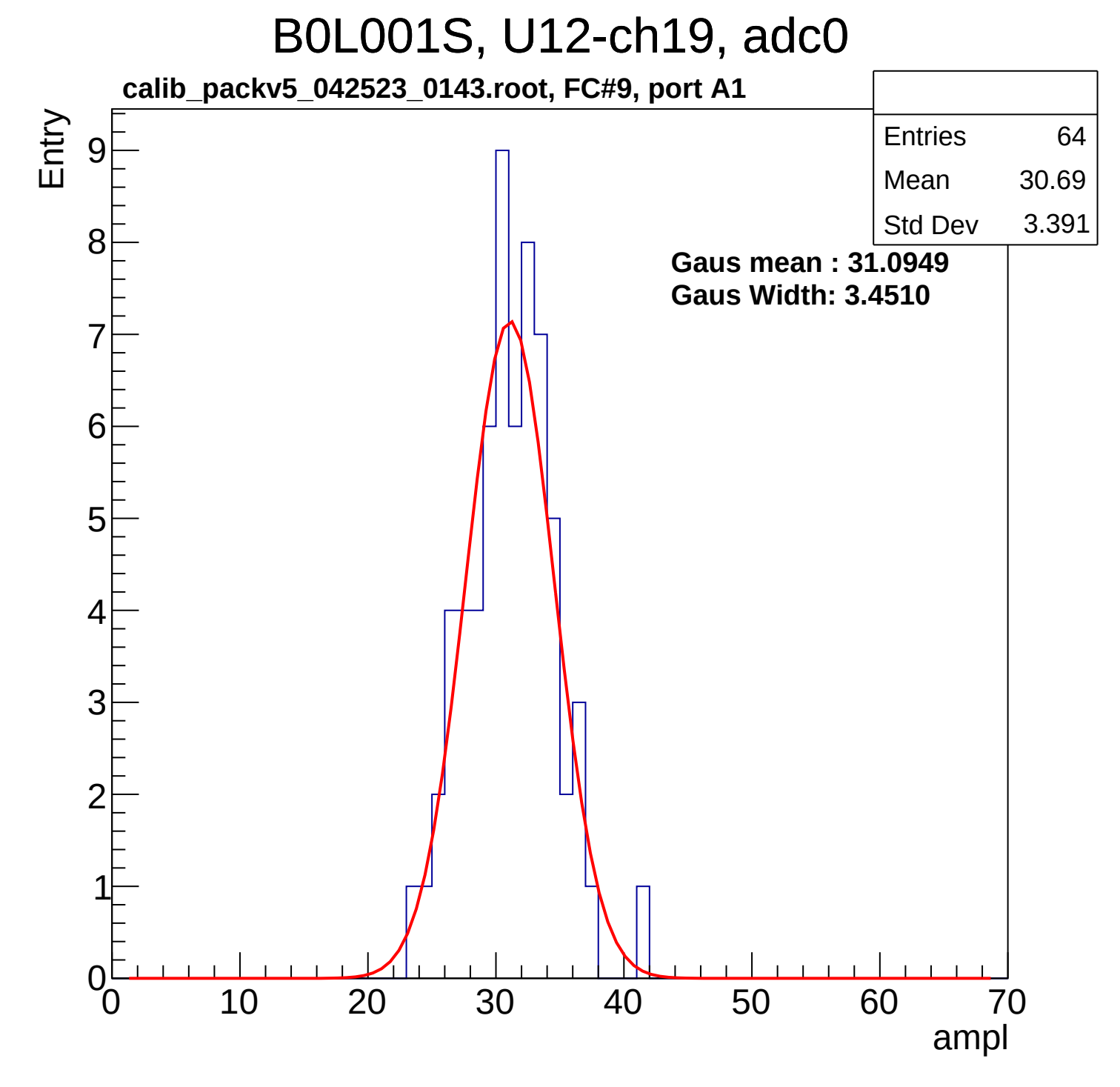
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch19, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 64
Mean 30.69
Std Dev 3.391
Gaus mean : 31.0949
Gaus Width: 3.4510
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
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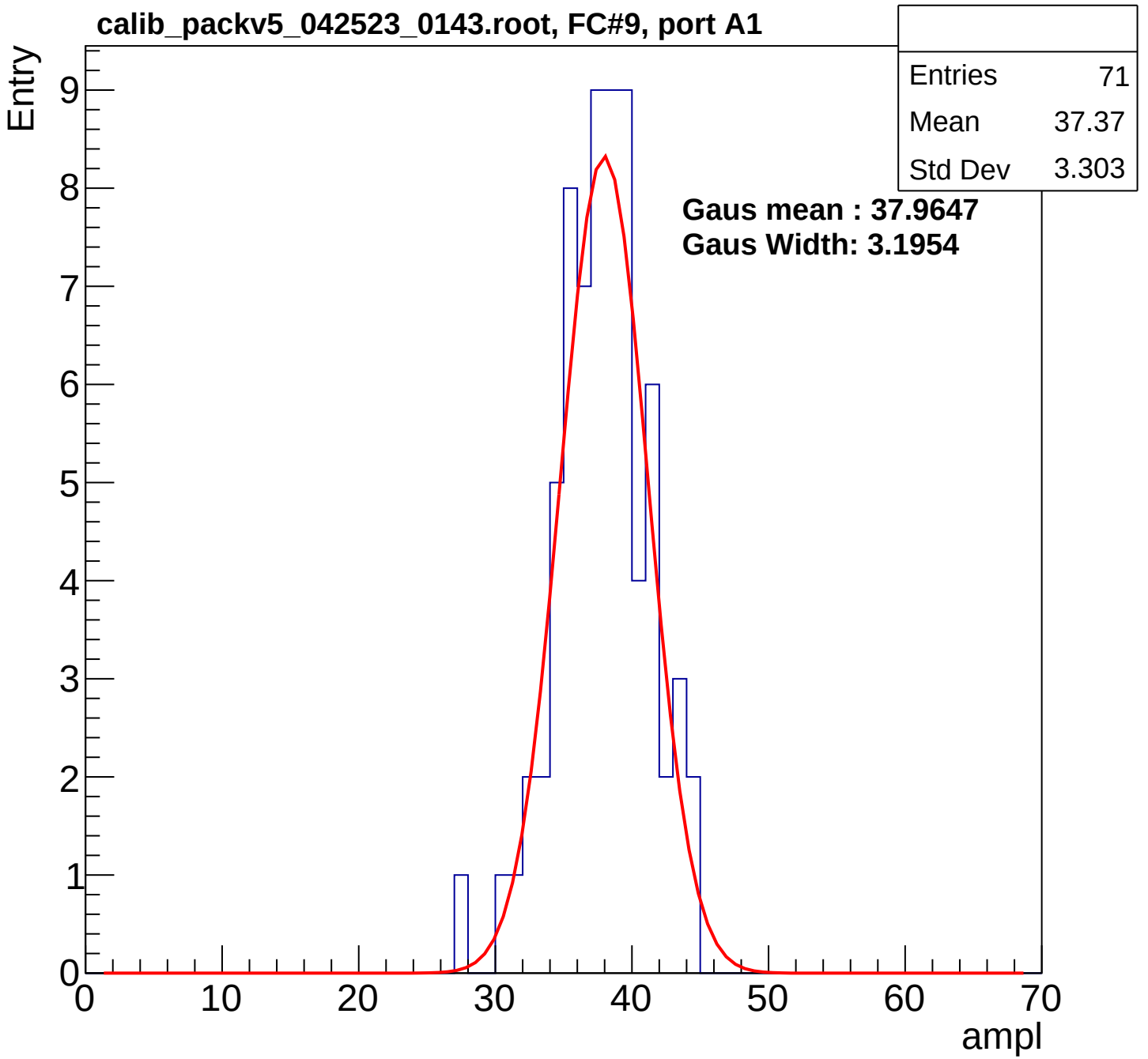
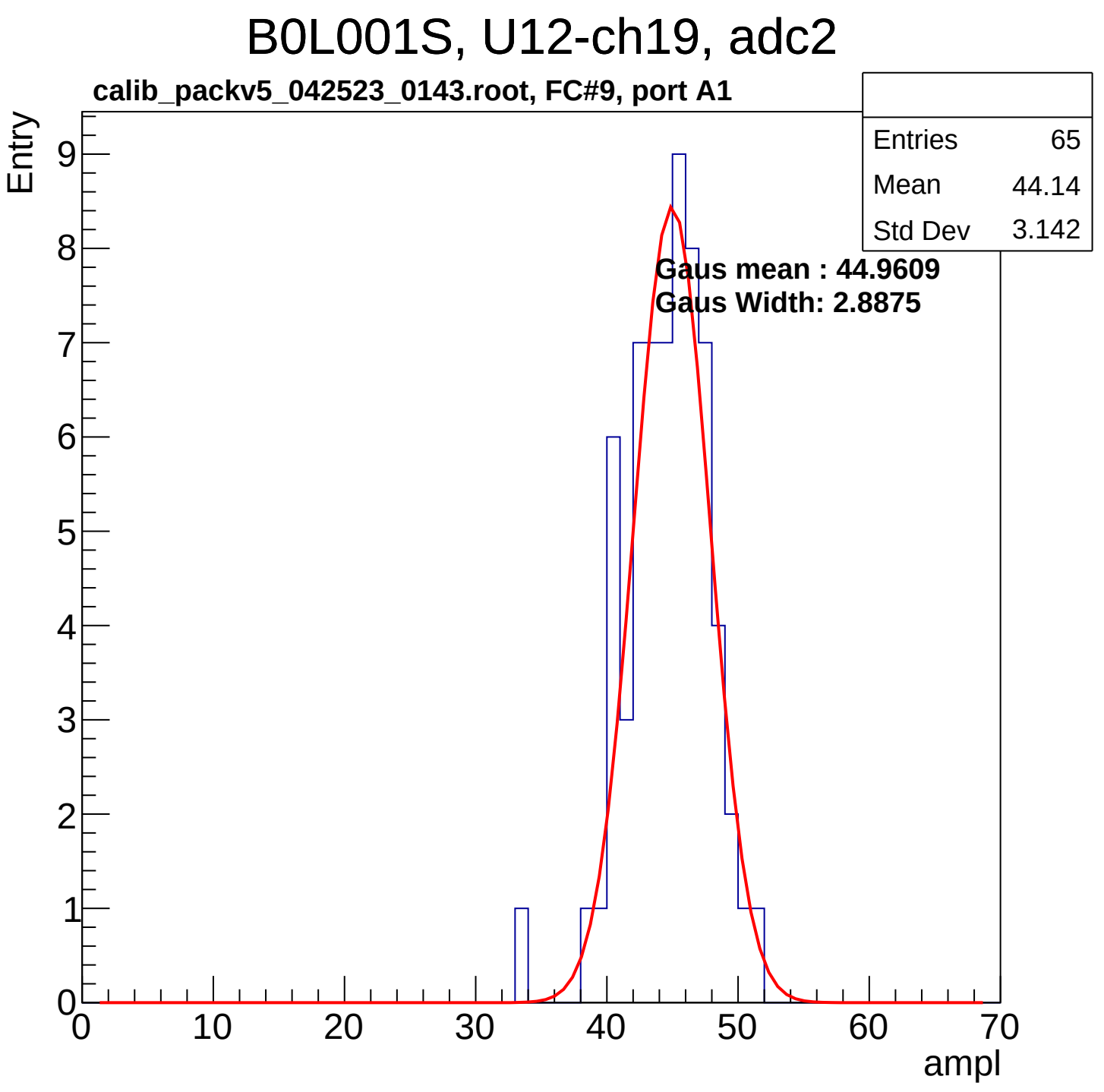
40
50
60
70


B0L001S, U12-ch19, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 71
Mean 37.37
Std Dev 3.303
Gaus mean : 37.9647
Gaus Width: 3.1954
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch19, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 65
Mean 44.14
Std Dev 3.142
Gaus mean : 44.9609
Gaus Width: 2.8875
Entry
ampl
0
1
2
3
4
5
6
7
8
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0
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60
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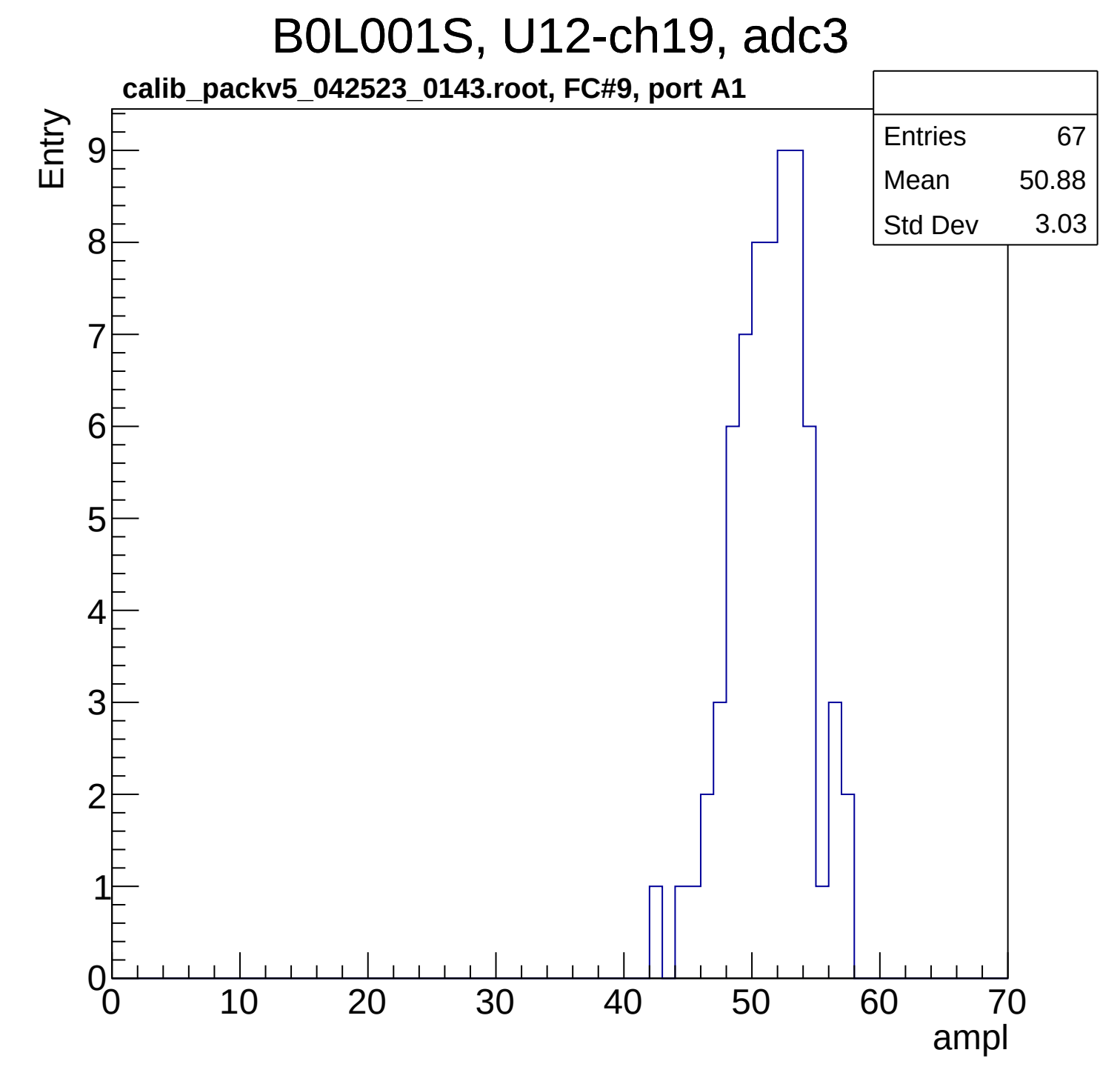
B0L001S, U12-ch19, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 67
Mean 50.88
Std Dev 3.03
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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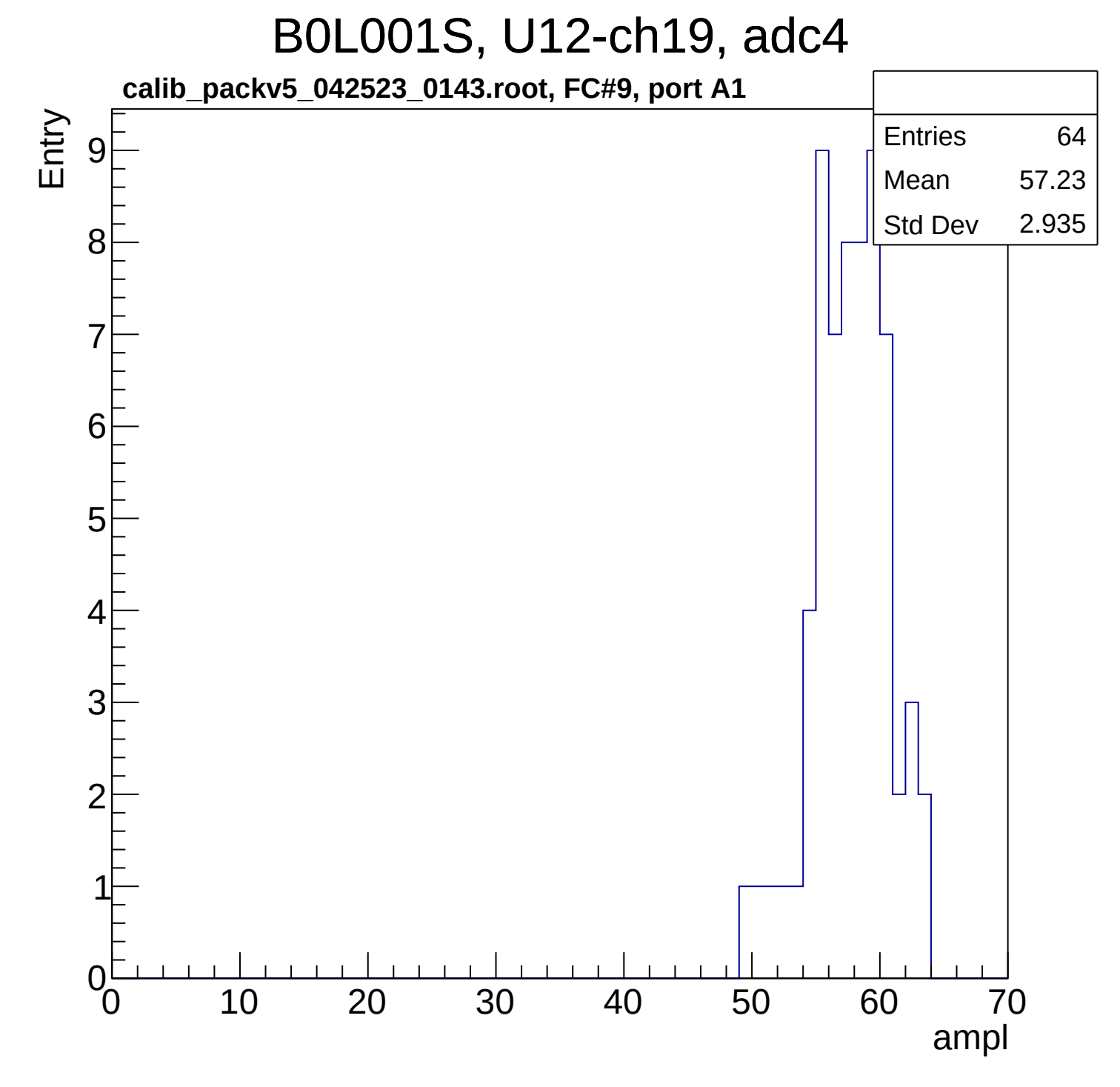
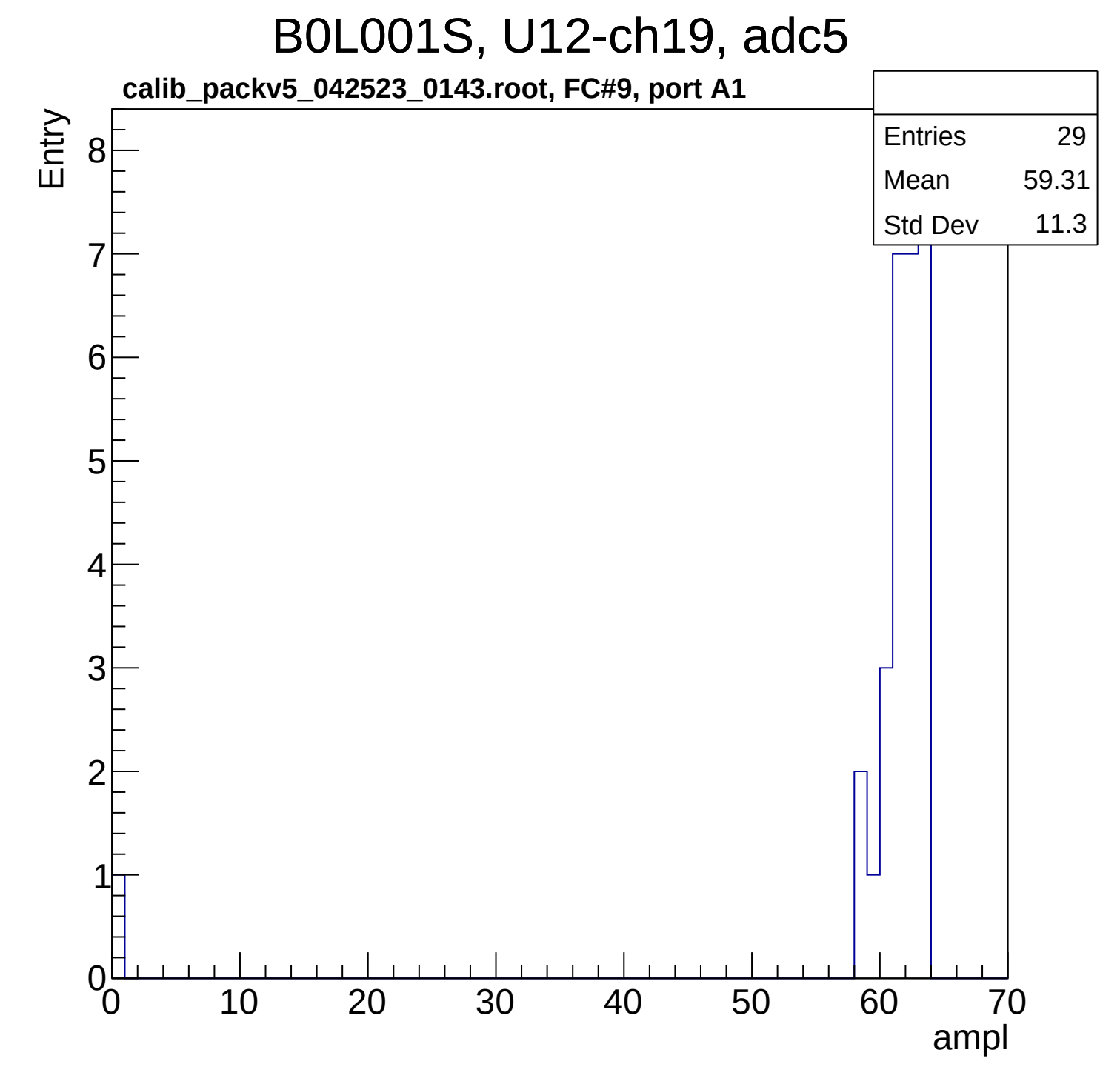
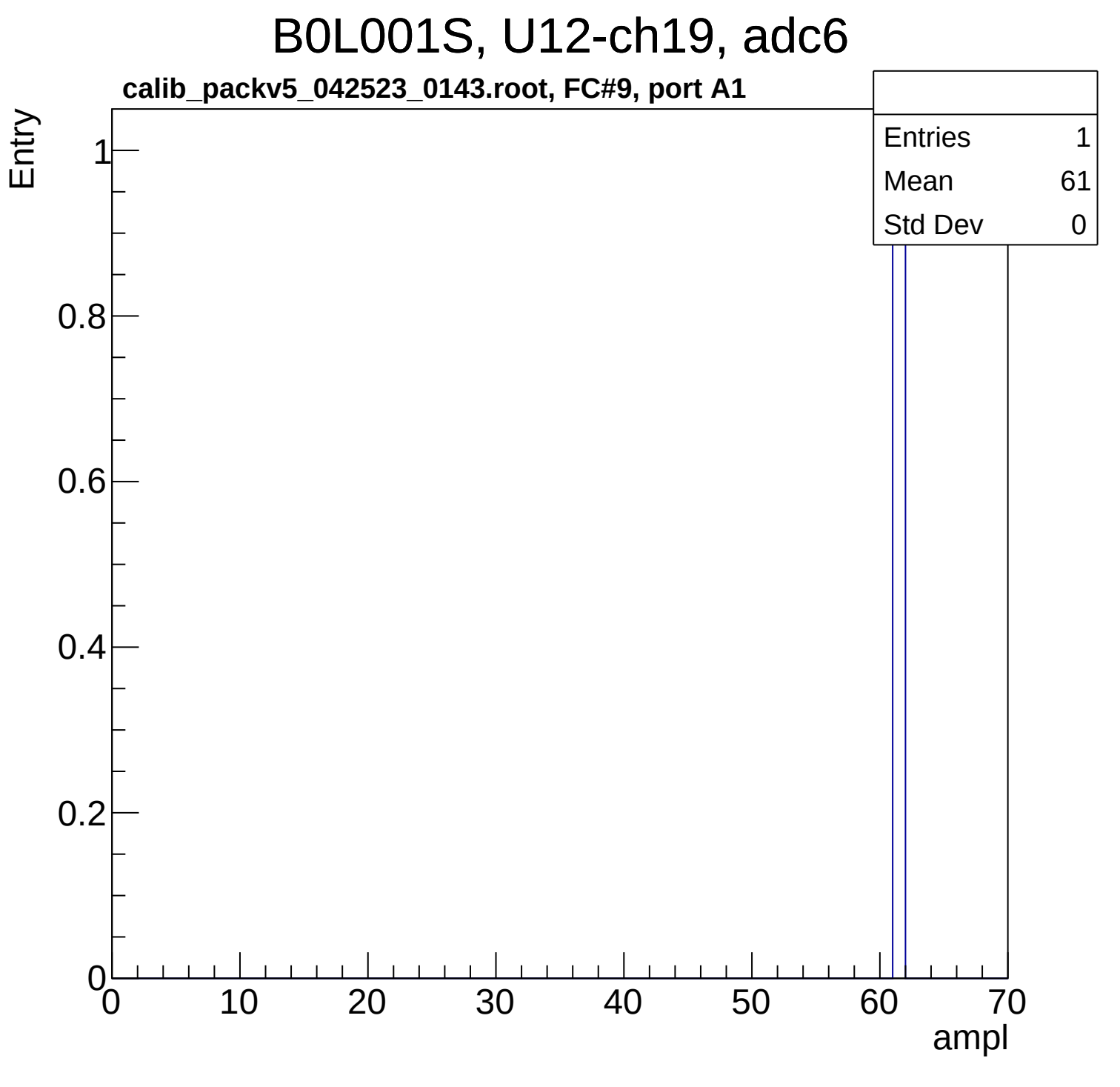
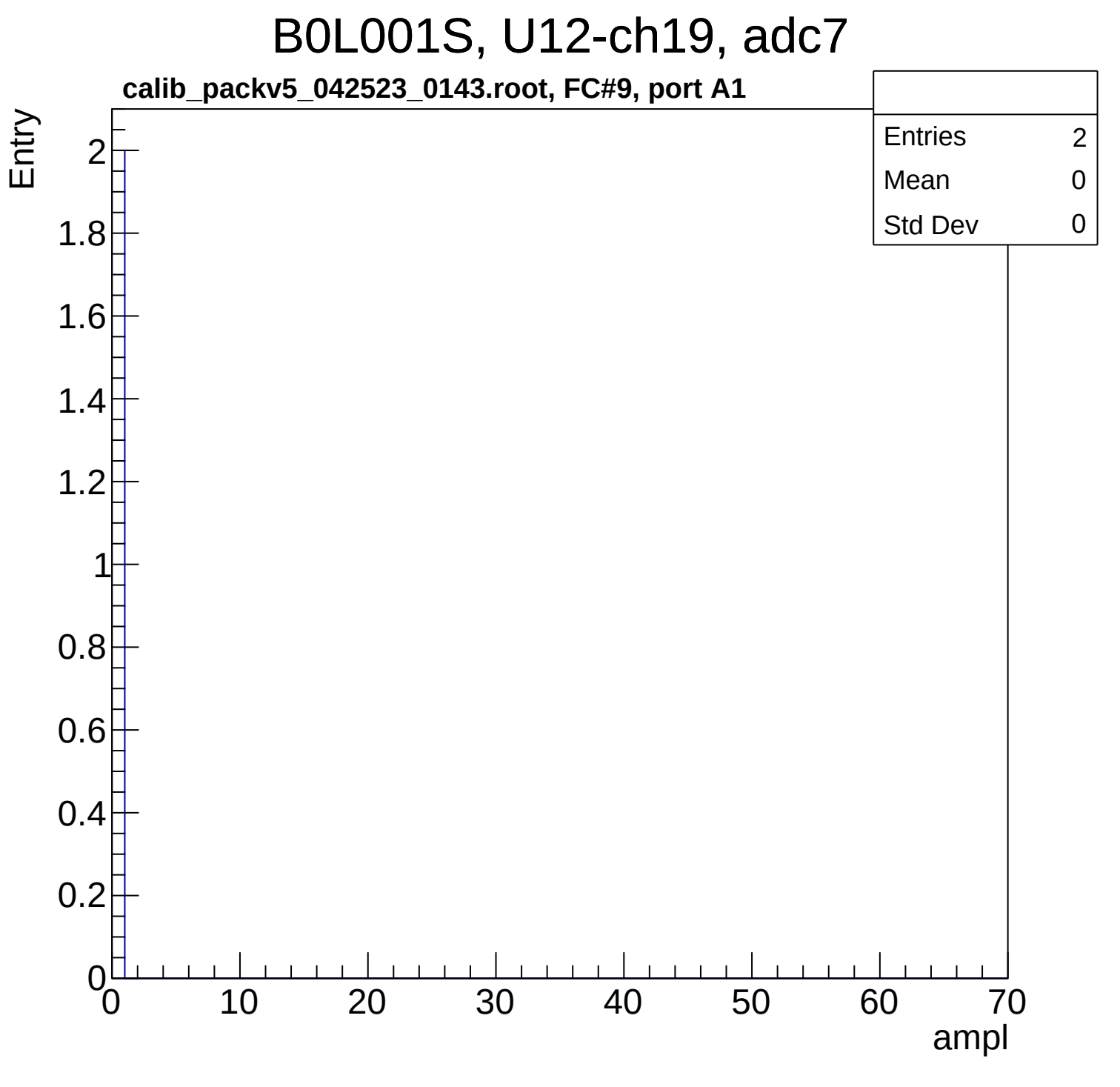
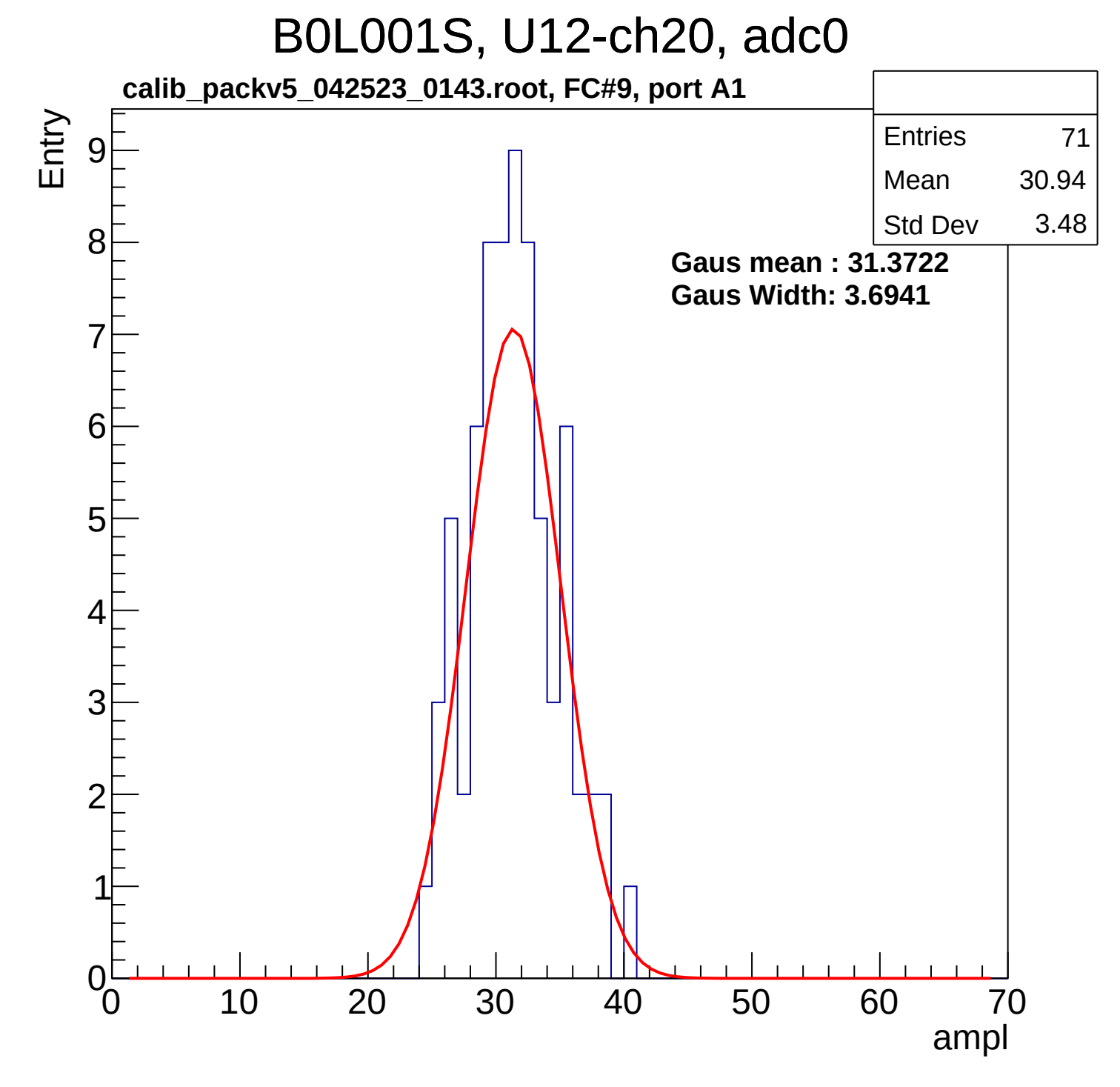
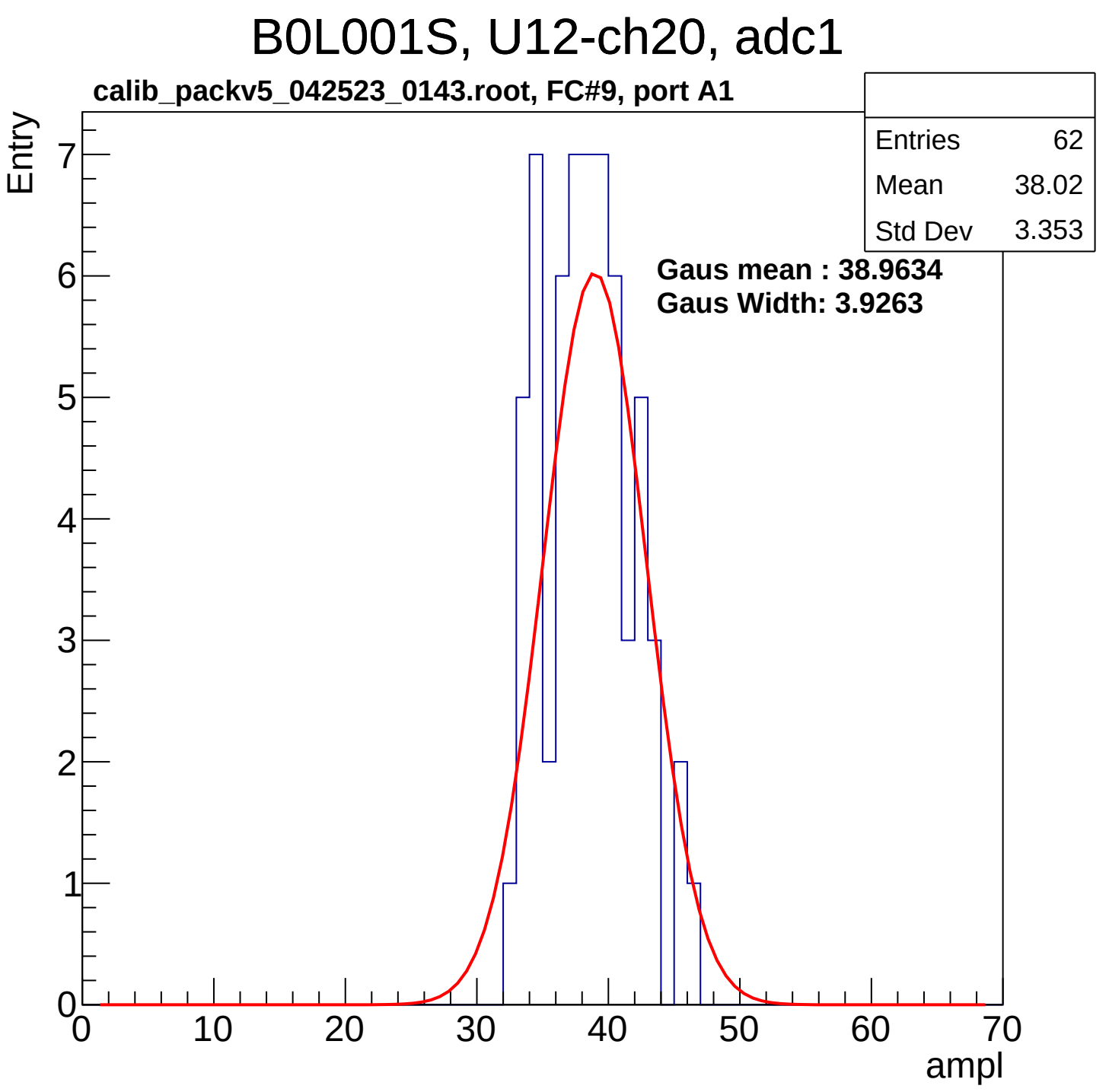

B0L001S, U12-ch19, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 64
Mean 57.23
Std Dev 2.935
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

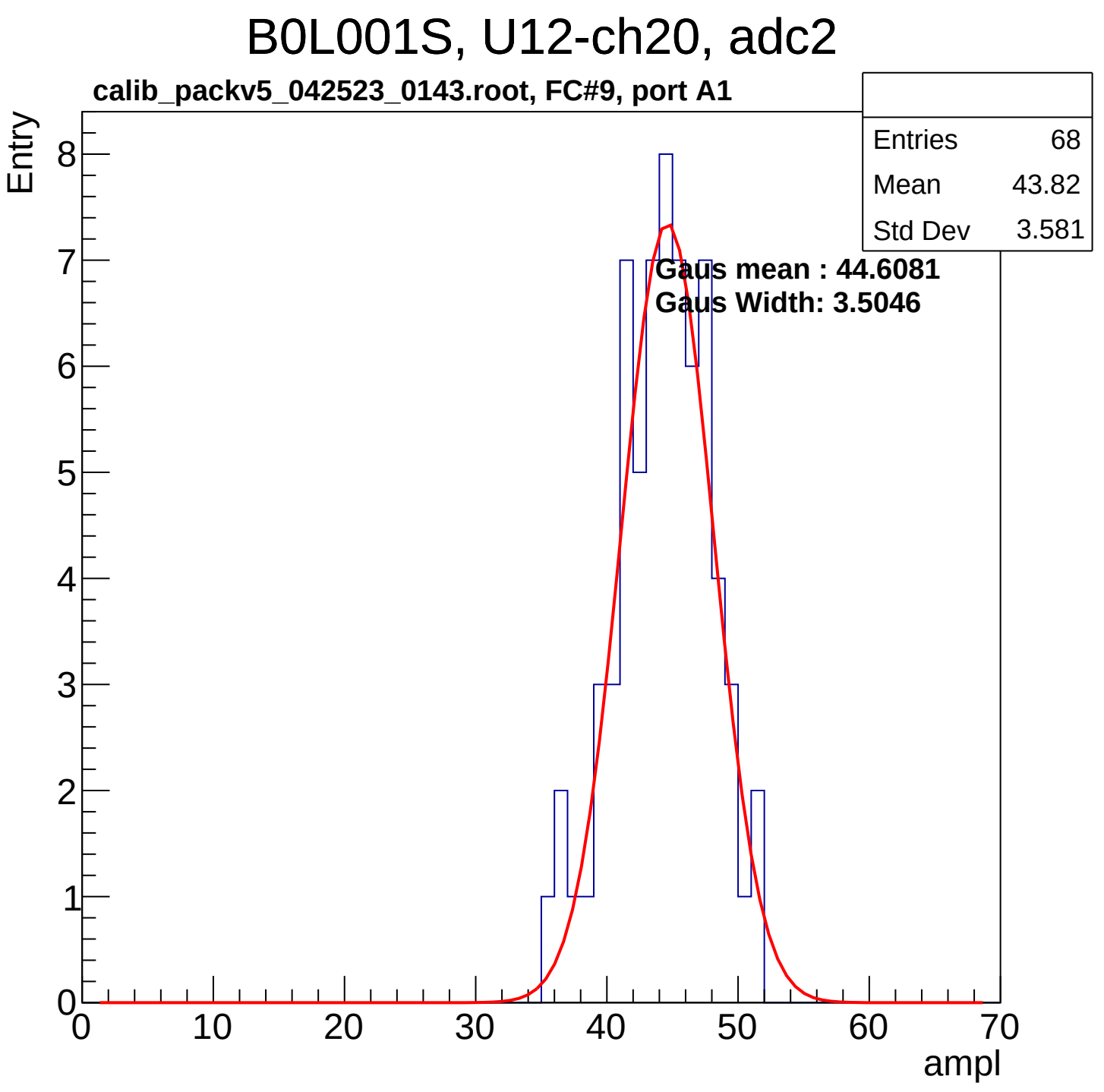

B0L001S, U12-ch19, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 29
Mean 59.31
Std Dev 11.3
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch19, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 61
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch19, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch20, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 71
Mean 30.94
Std Dev 3.48
Gaus mean : 31.3722
Gaus Width: 3.6941
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch20, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 62
Mean 38.02
Std Dev 3.353
Gaus mean : 38.9634
Gaus Width: 3.9263
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B0L001S, U12-ch20, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 68
Mean 43.82
Std Dev 3.581
Gaus mean : 44.6081
Gaus Width: 3.5046
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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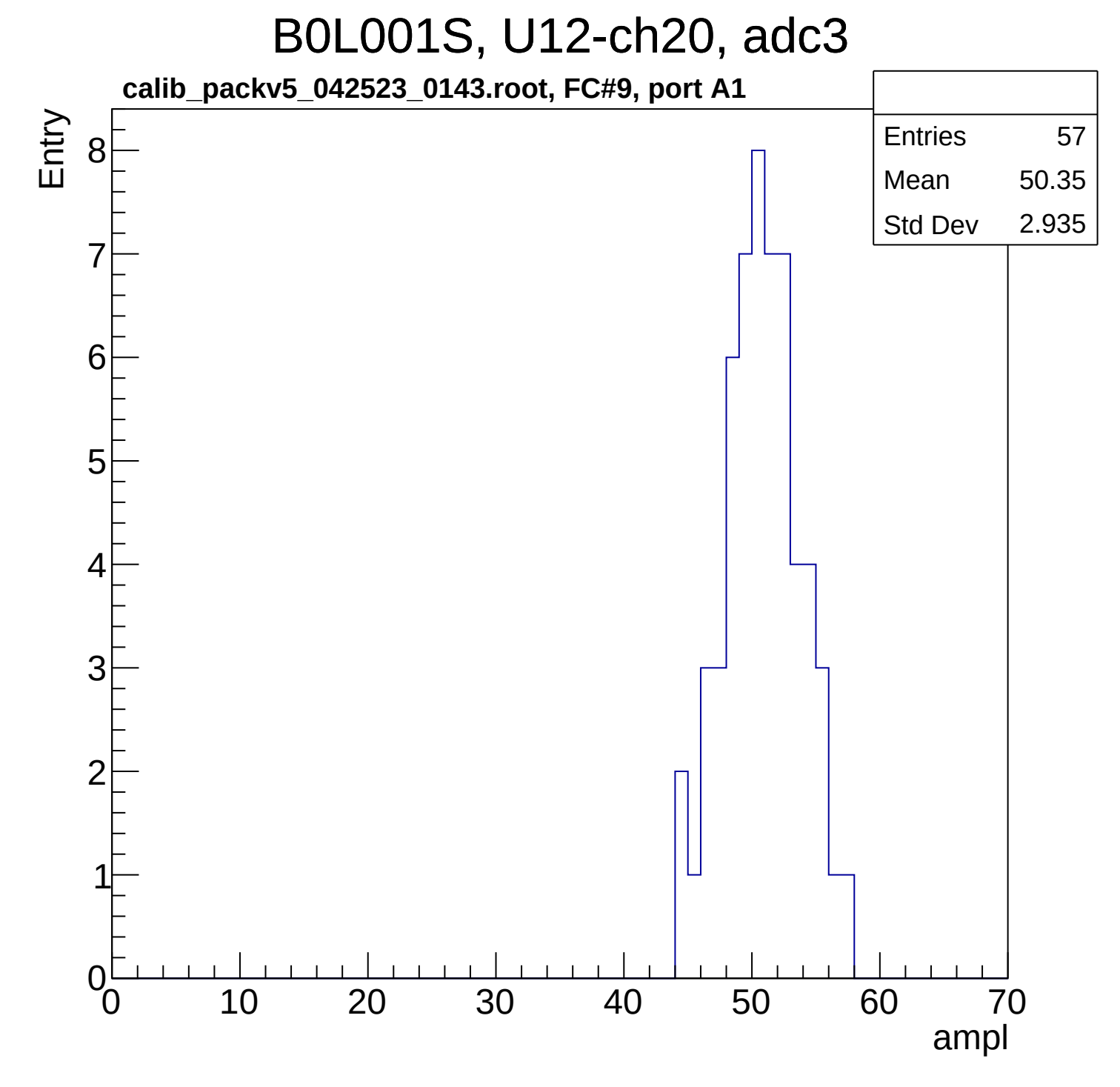
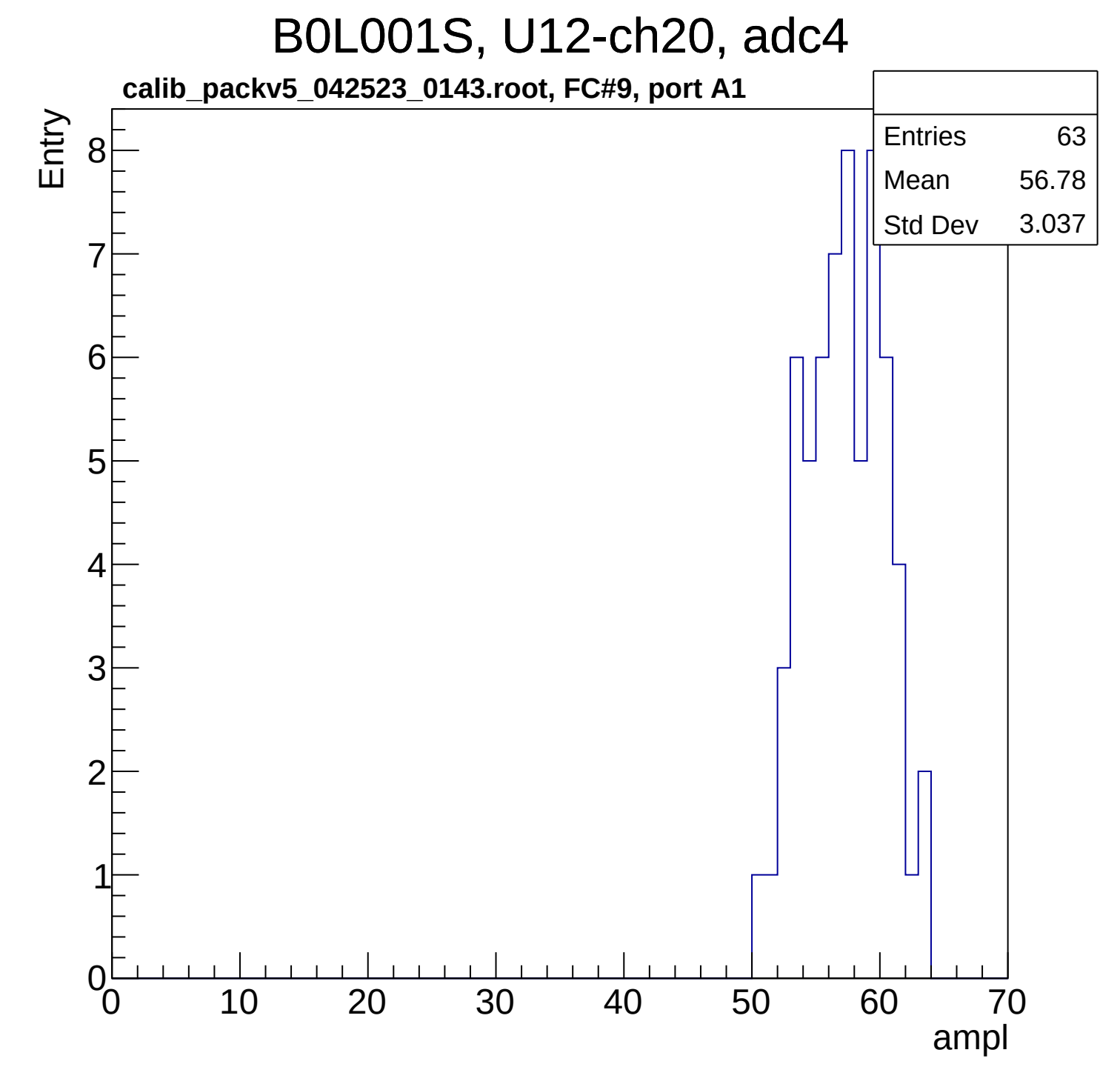

B0L001S, U12-ch20, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 57
Mean 50.35
Std Dev 2.935
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch20, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 63
Mean 56.78
Std Dev 3.037
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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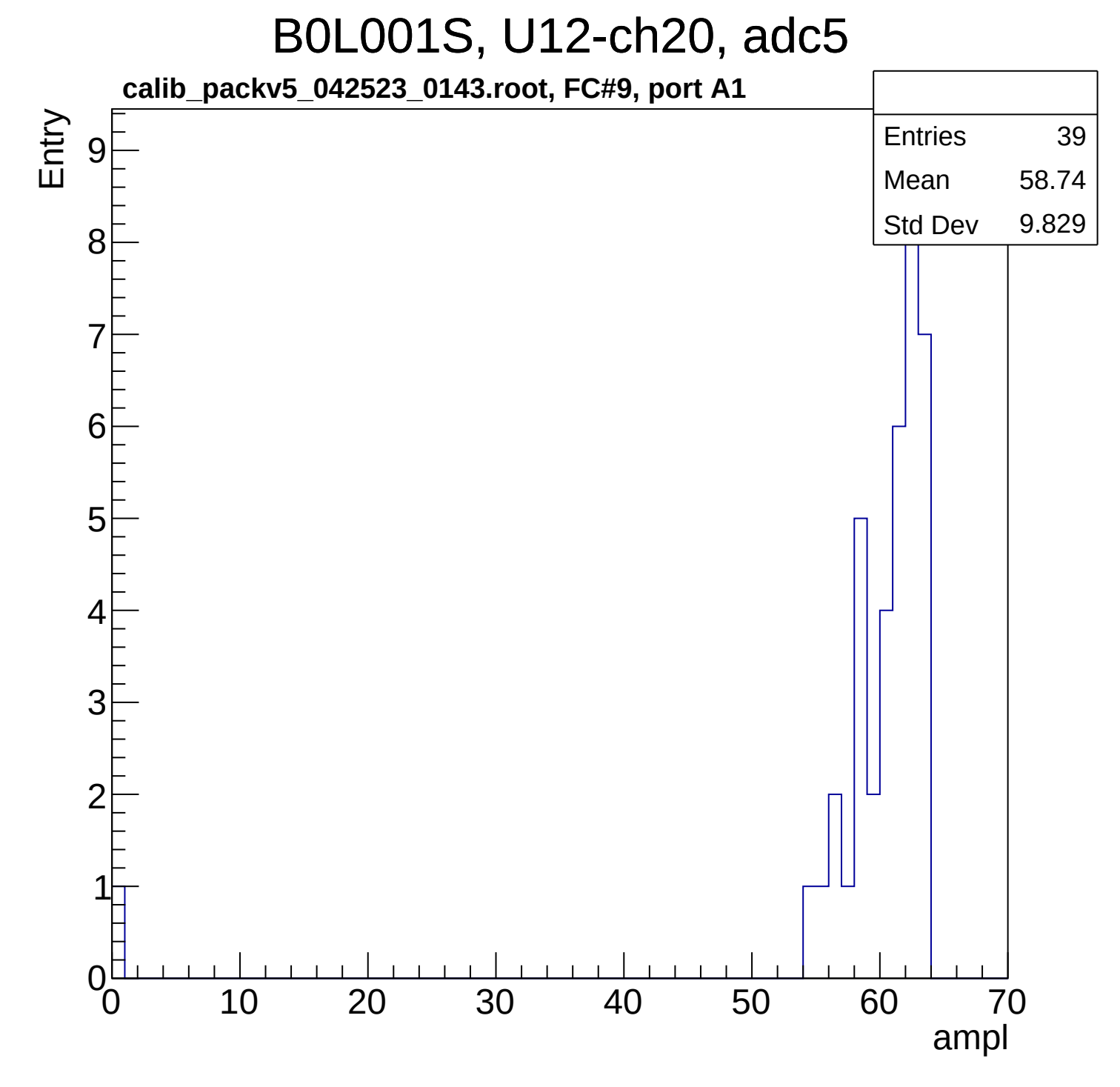
B0L001S, U12-ch20, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 39
Mean 58.74
Std Dev 9.829
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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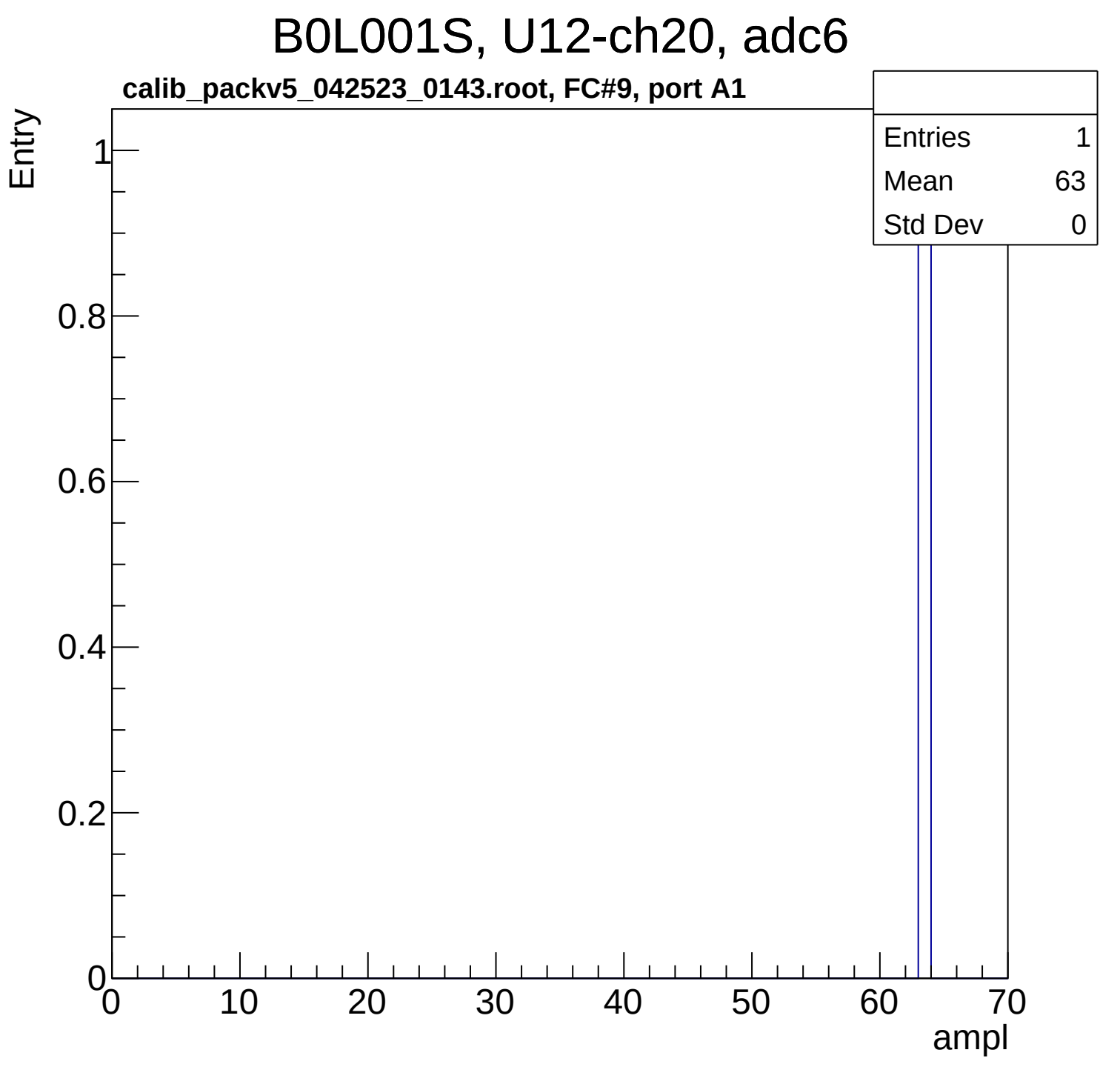
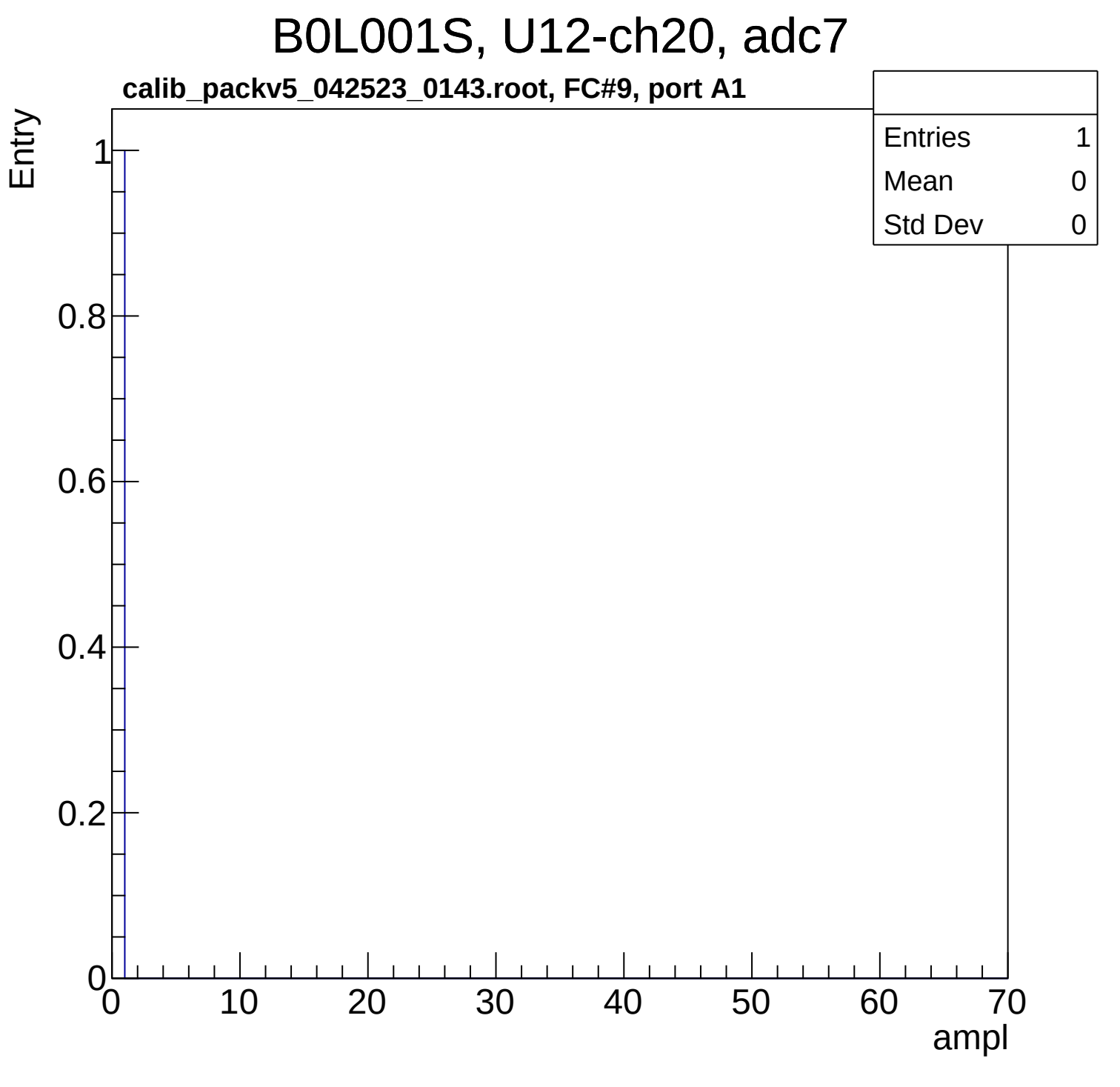
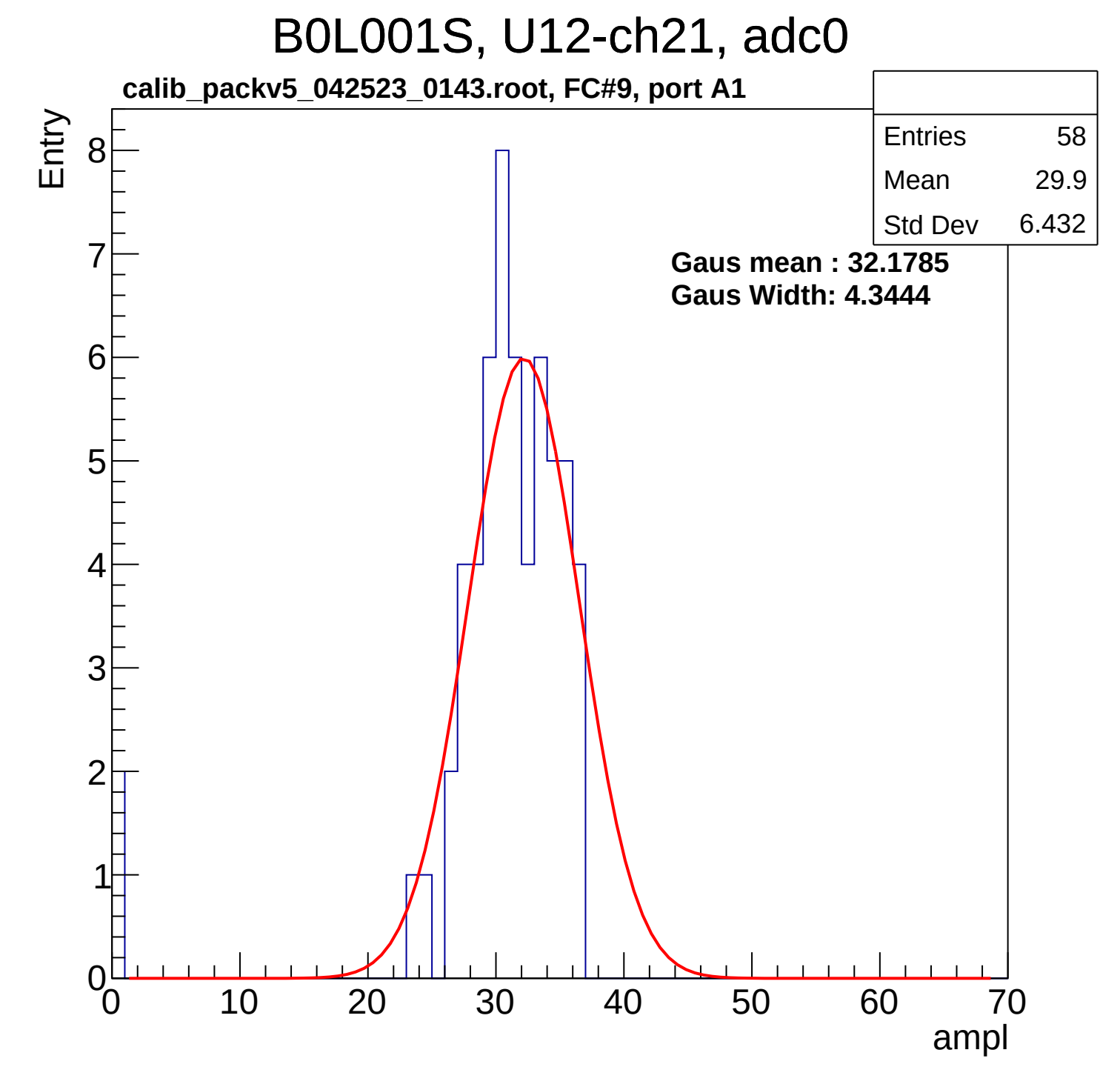
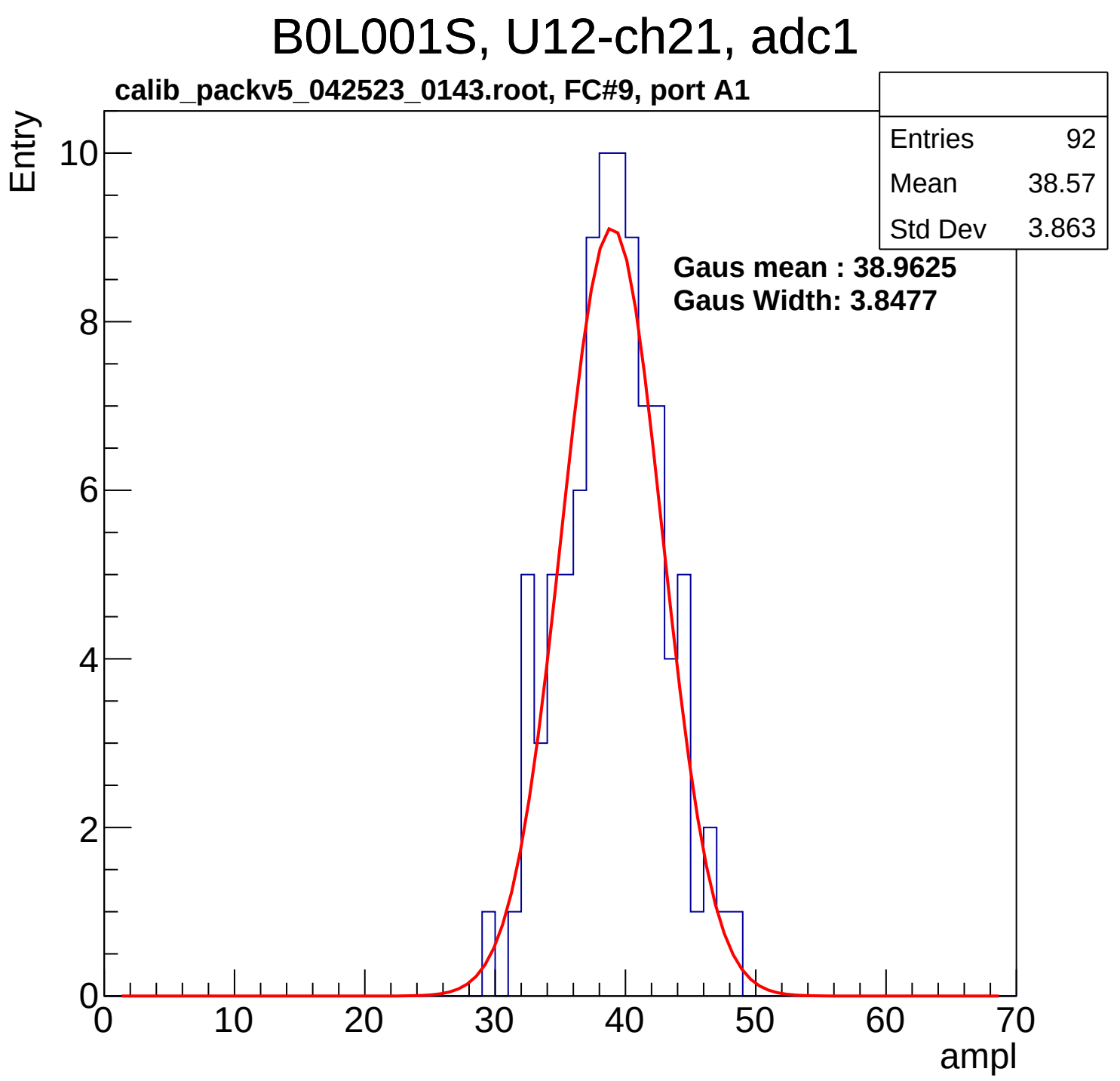
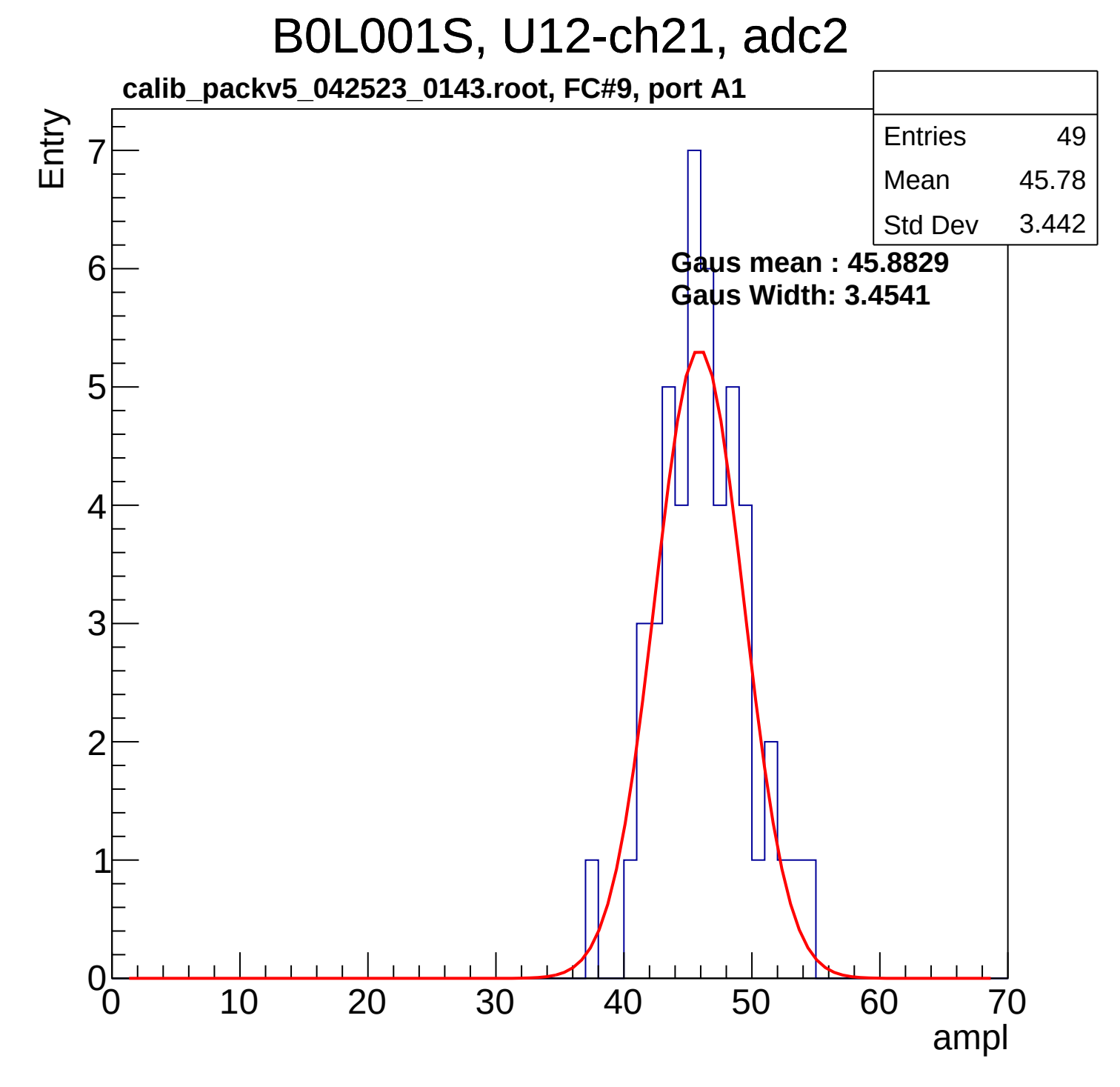
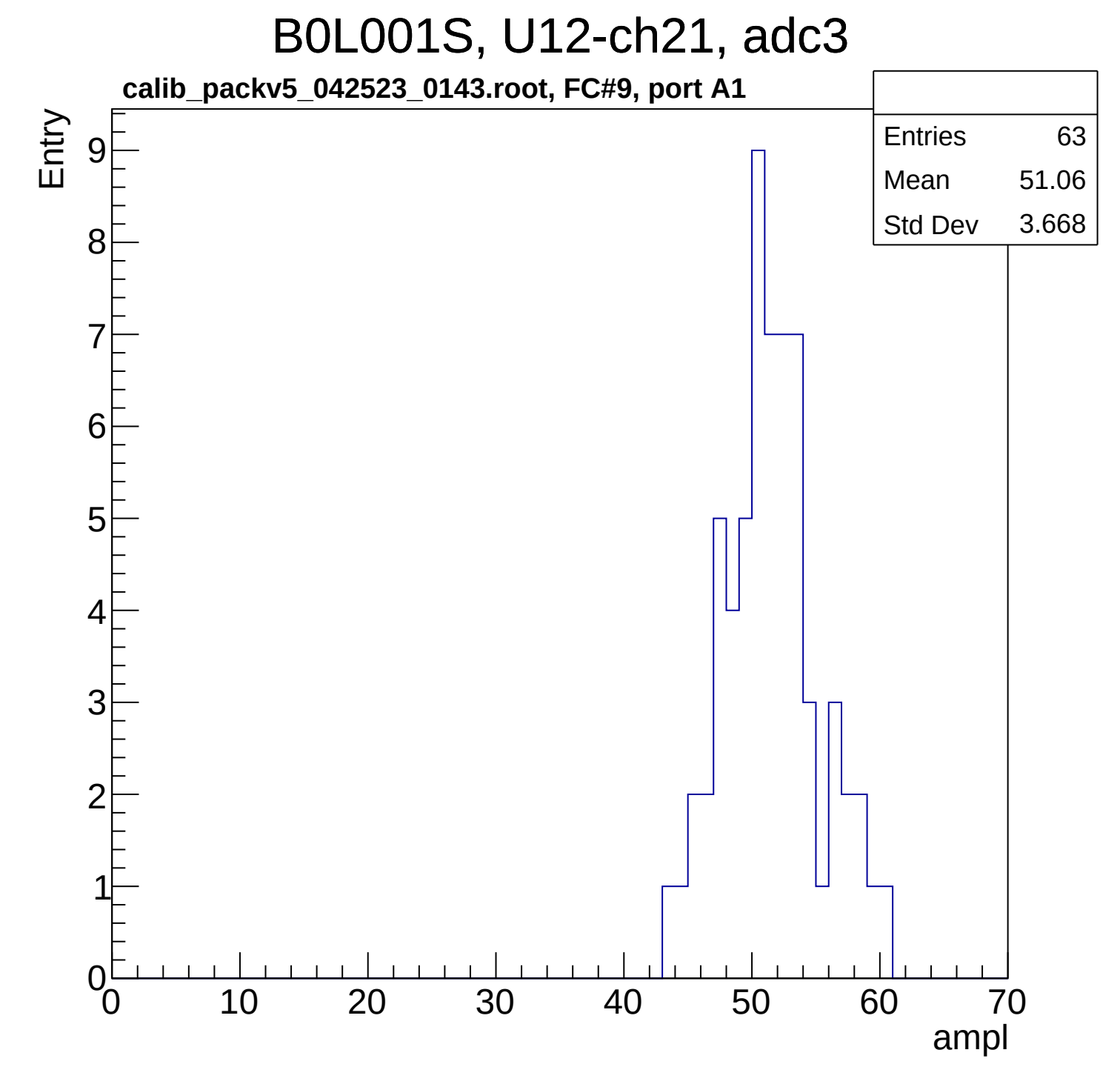

B0L001S, U12-ch20, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch20, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch21, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 58
Mean 29.9
Std Dev 6.432
Gaus mean : 32.1785
Gaus Width: 4.3444
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch21, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 92
Mean 38.57
Std Dev 3.863
Gaus mean : 38.9625
Gaus Width: 3.8477
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch21, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 49
Mean 45.78
Std Dev 3.442
Gaus mean : 45.8829
Gaus Width: 3.4541
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B0L001S, U12-ch21, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 63
Mean 51.06
Std Dev 3.668
Entry
ampl
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2
3
4
5
6
7
8
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0
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20
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40
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60
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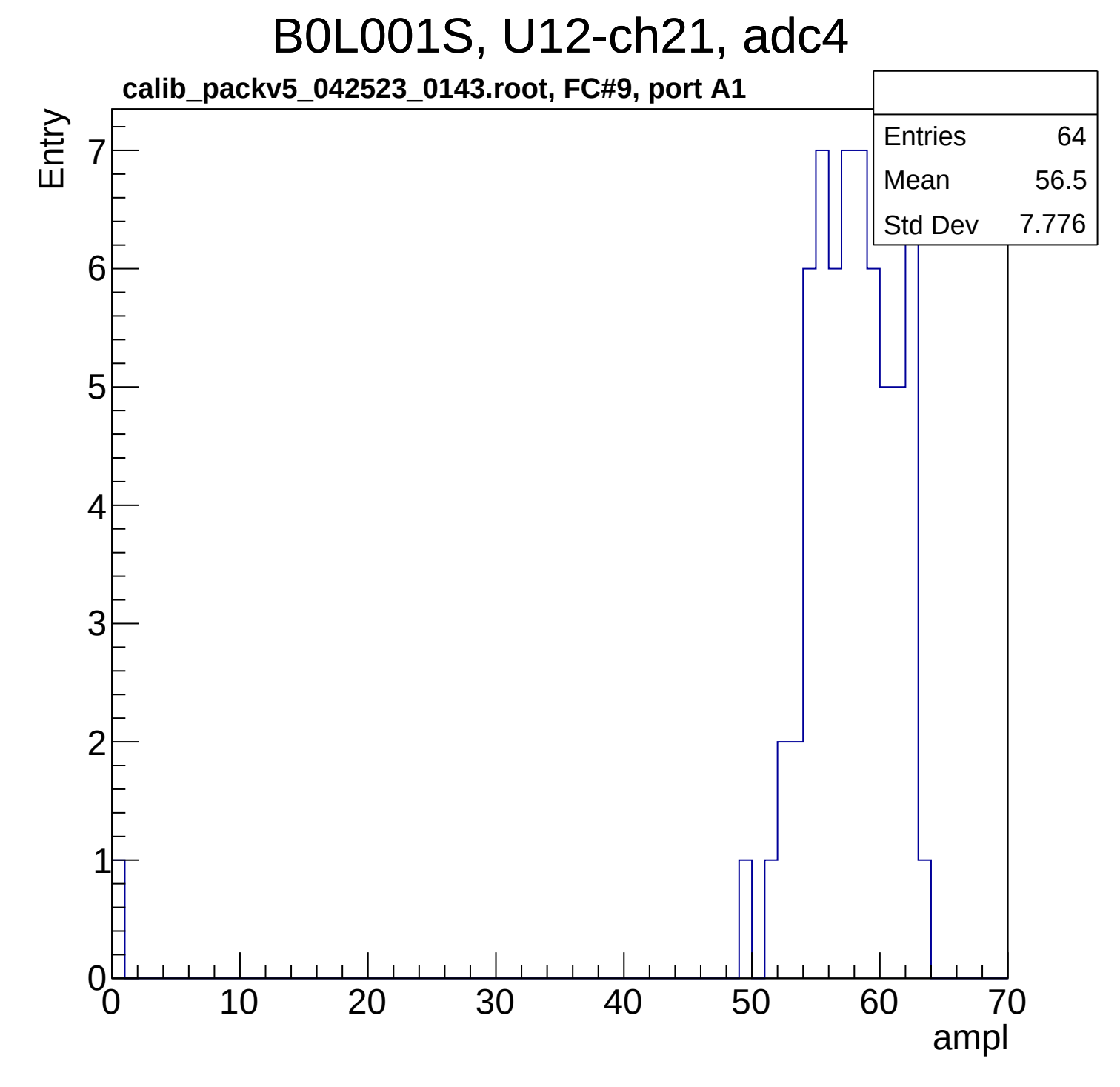
B0L001S, U12-ch21, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 64
Mean 56.5
Std Dev 7.776
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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40
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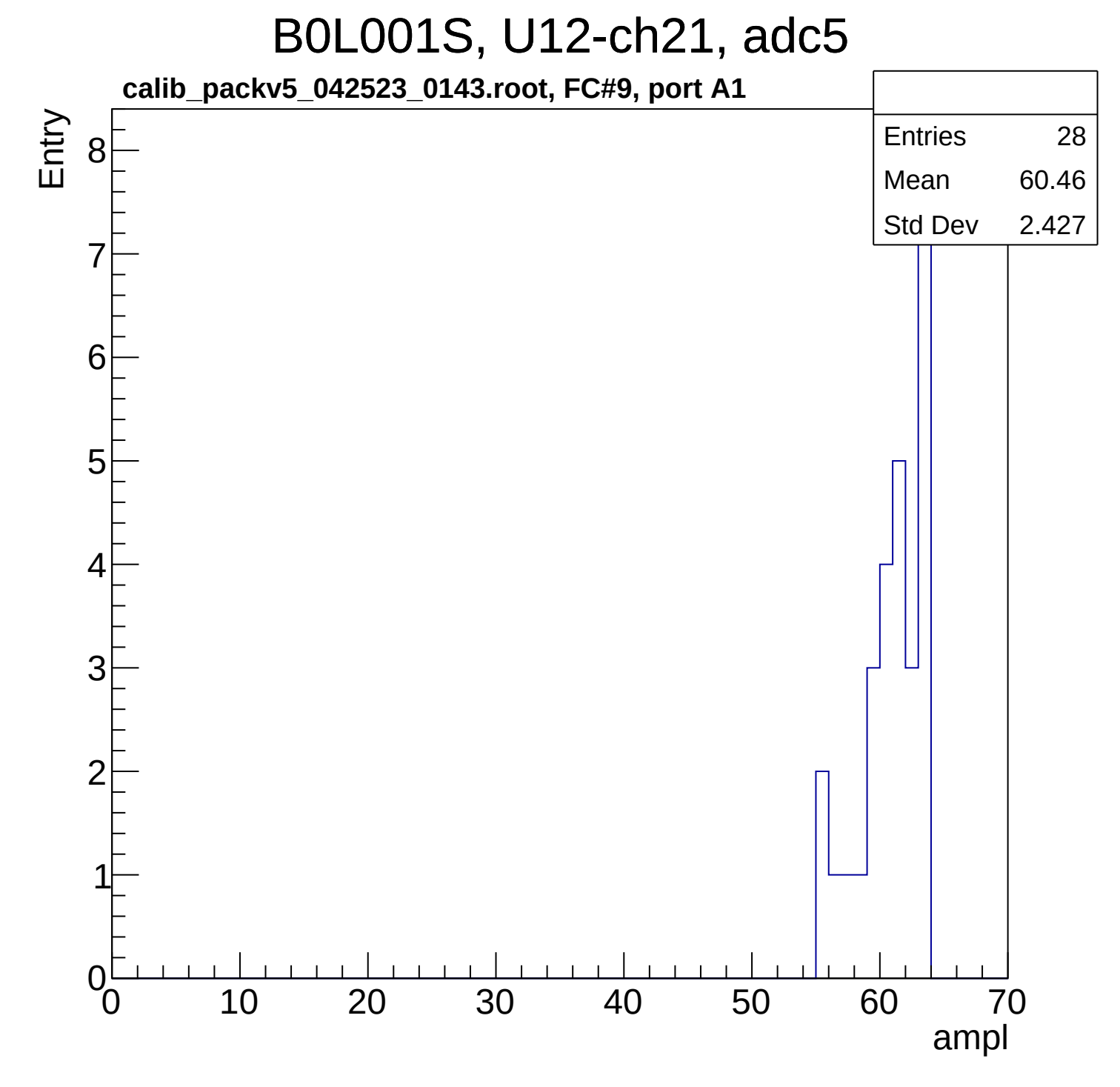
60
70


B0L001S, U12-ch21, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 28
Mean 60.46
Std Dev 2.427
Entry
ampl
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1
2
3
4
5
6
7
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0
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60
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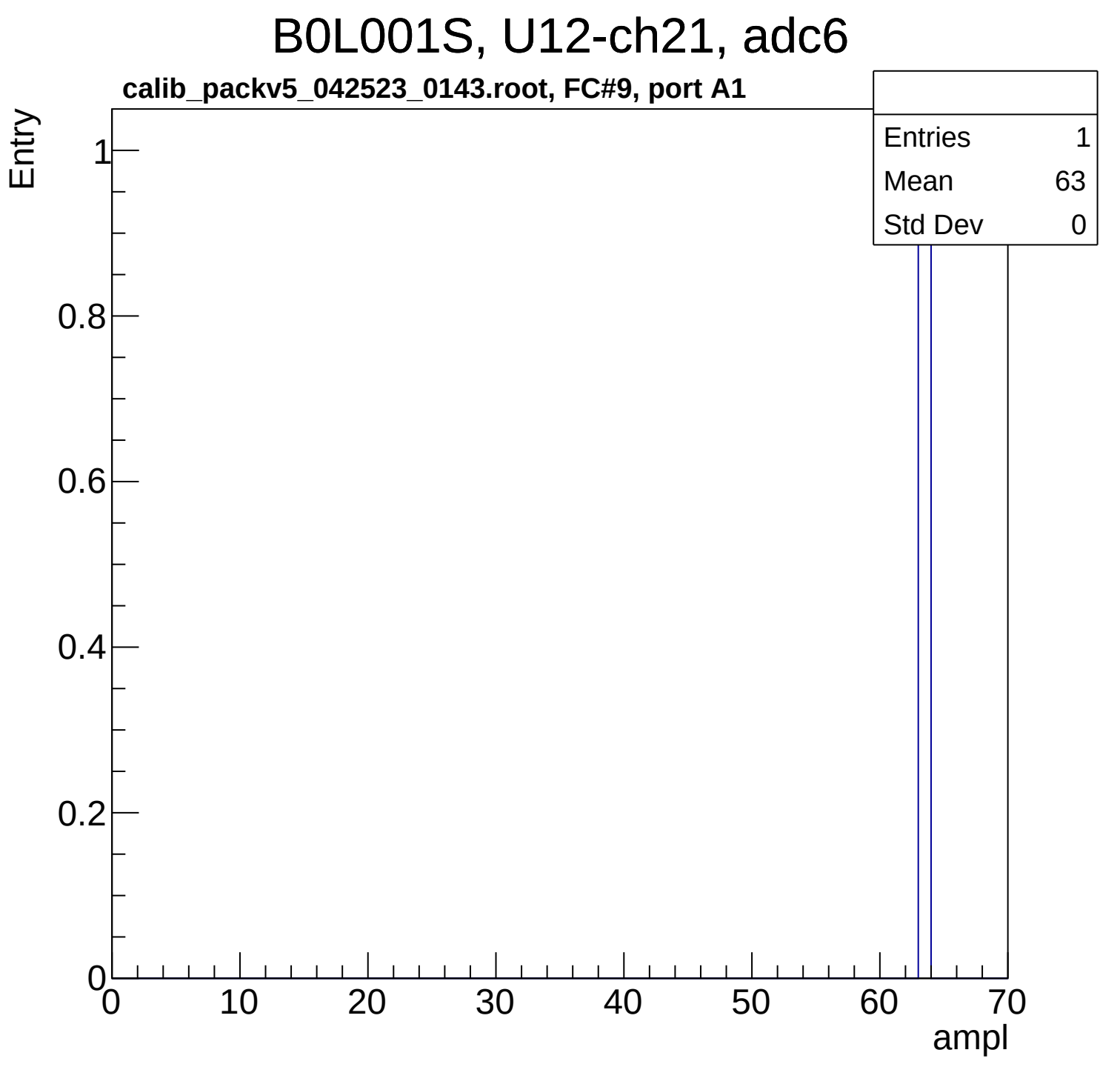
B0L001S, U12-ch21, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 63
Std Dev 0
Entry
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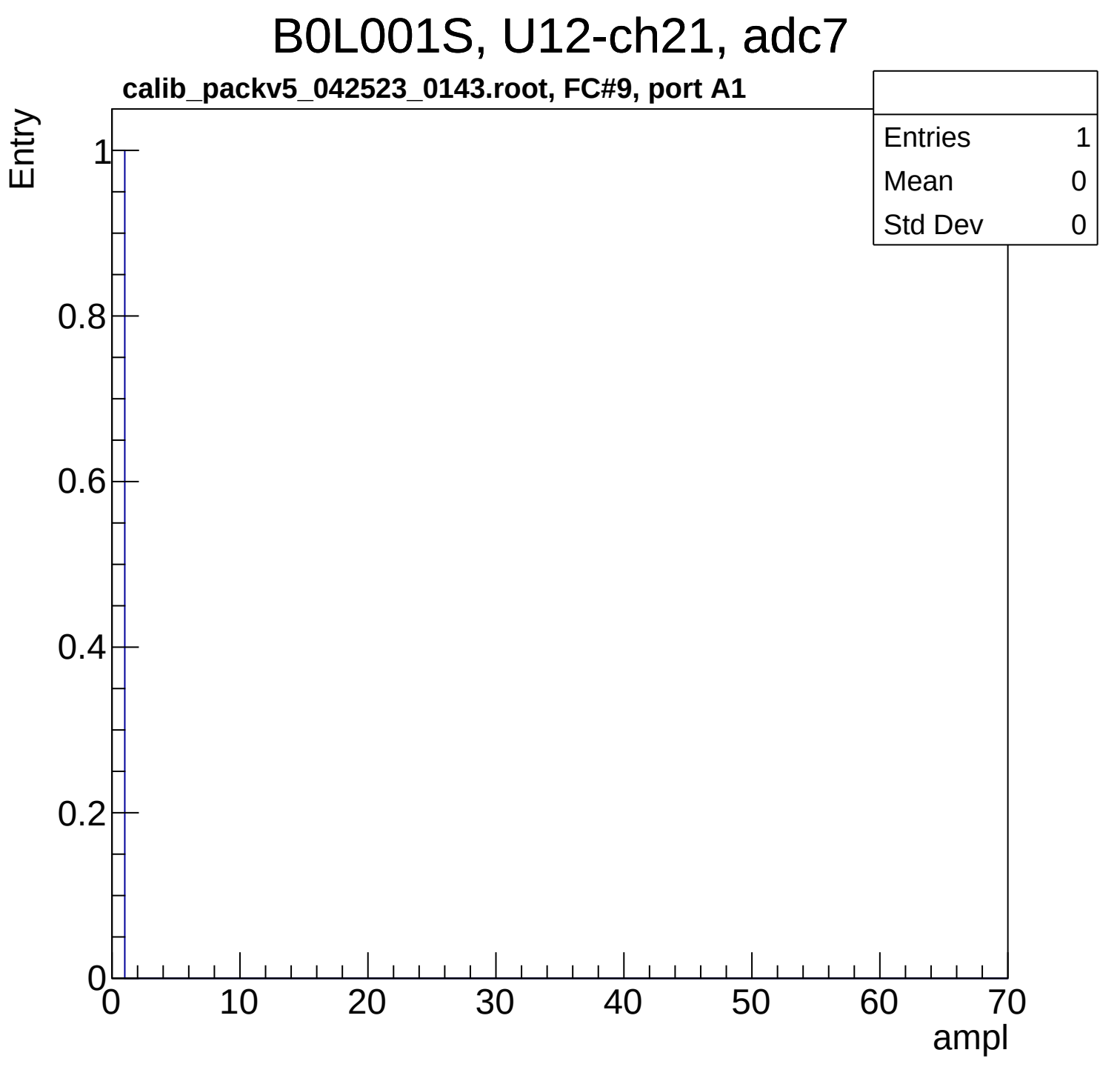
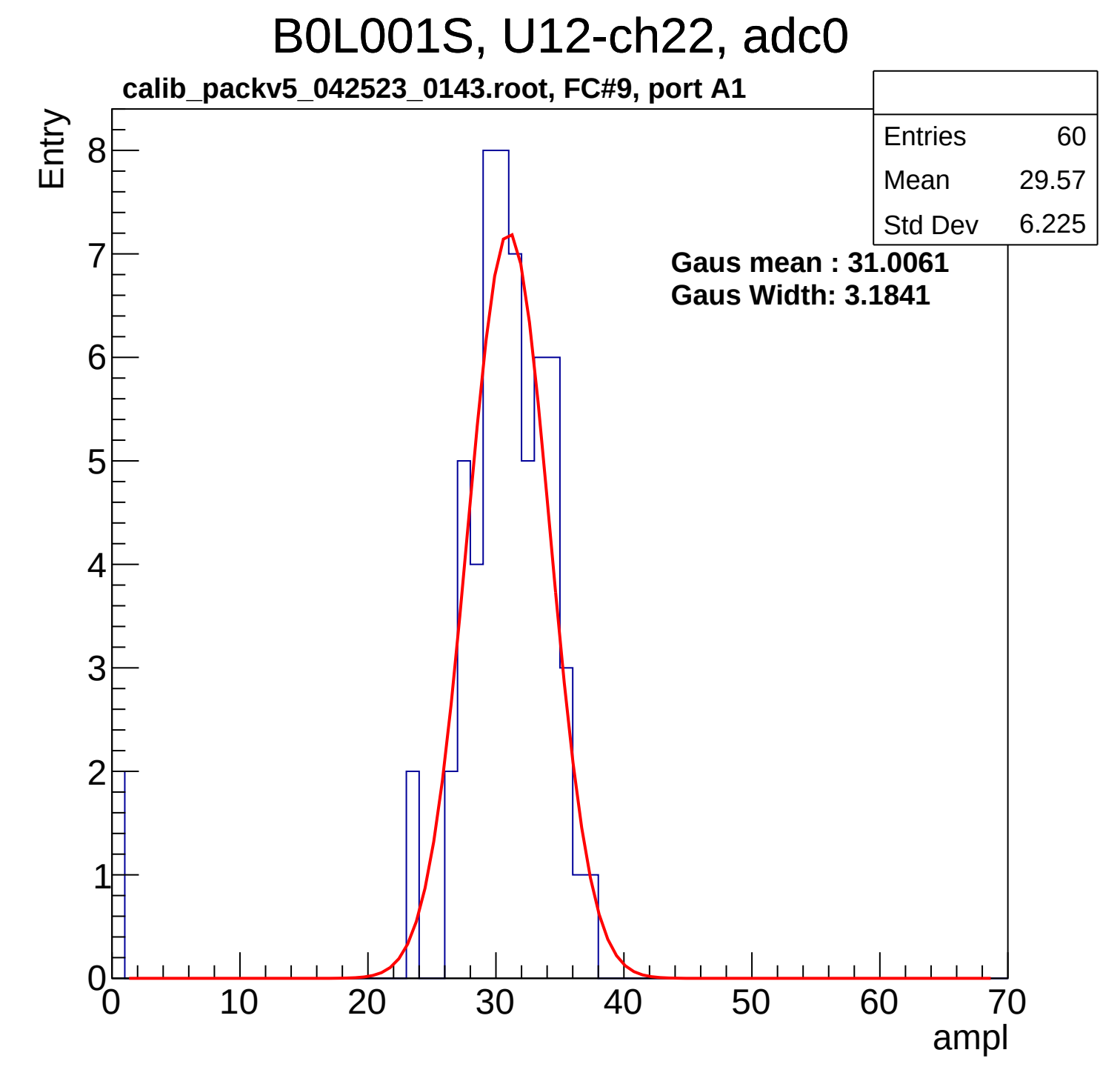
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch21, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch22, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 60
Mean 29.57
Std Dev 6.225
Gaus mean : 31.0061
Gaus Width: 3.1841
Entry
ampl
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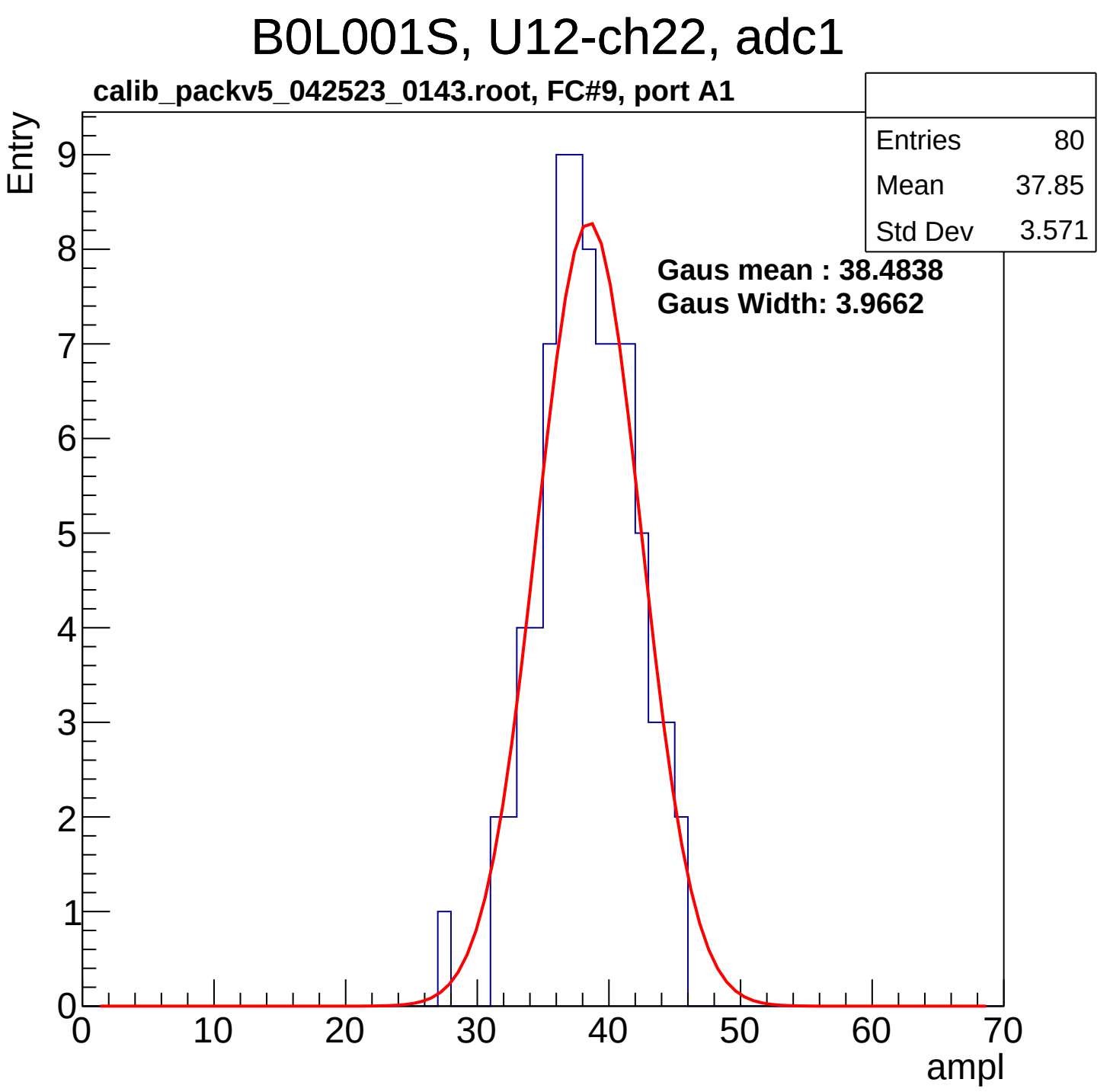
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch22, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 80
Mean 37.85
Std Dev 3.571
Gaus mean : 38.4838
Gaus Width: 3.9662
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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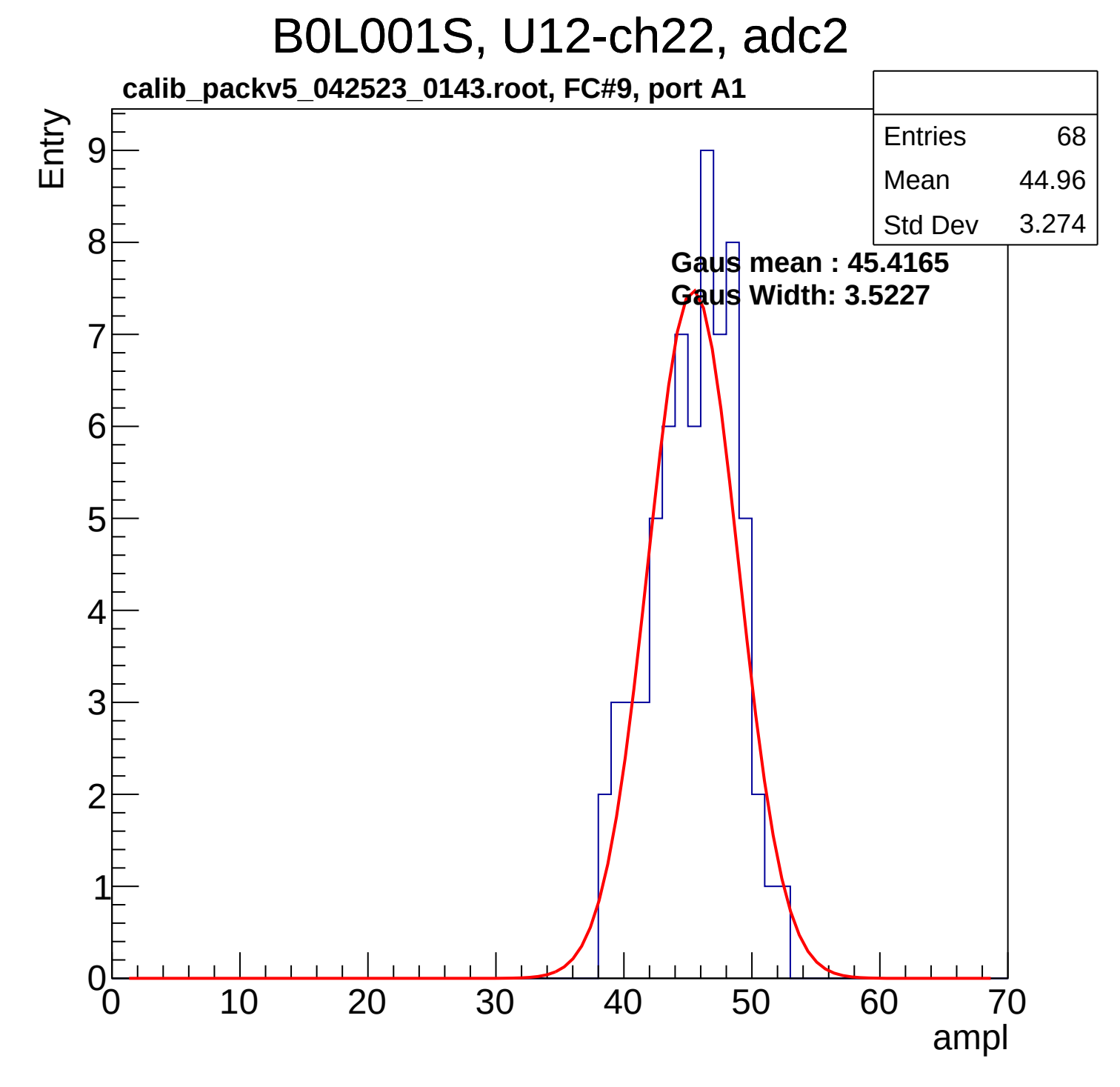
B0L001S, U12-ch22, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 68
Mean 44.96
Std Dev 3.274
Gaus mean : 45.4165
Gaus Width: 3.5227
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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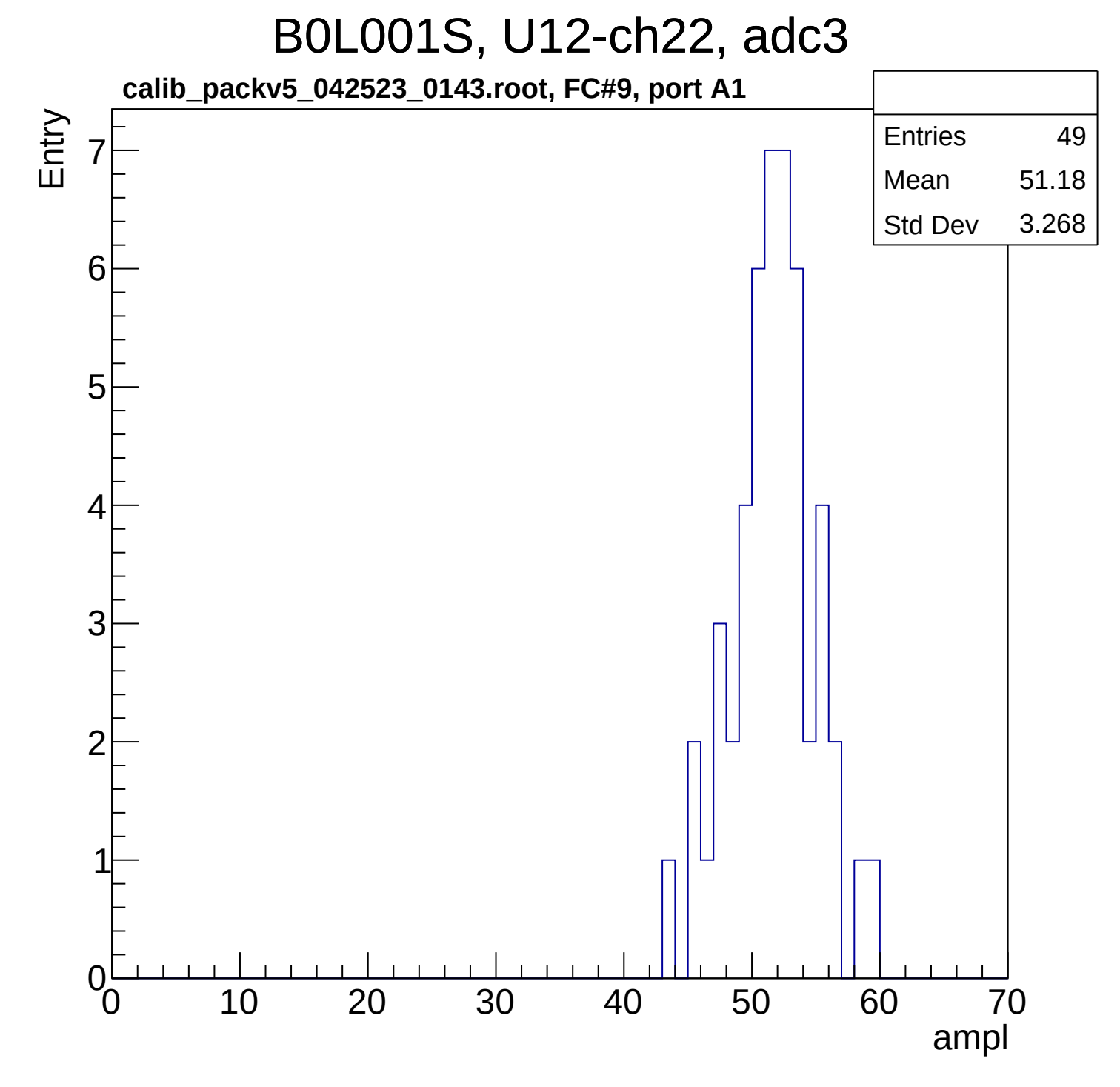
B0L001S, U12-ch22, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 49
Mean 51.18
Std Dev 3.268
Entry
ampl
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3
4
5
6
7
0
10
20
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40
50
60
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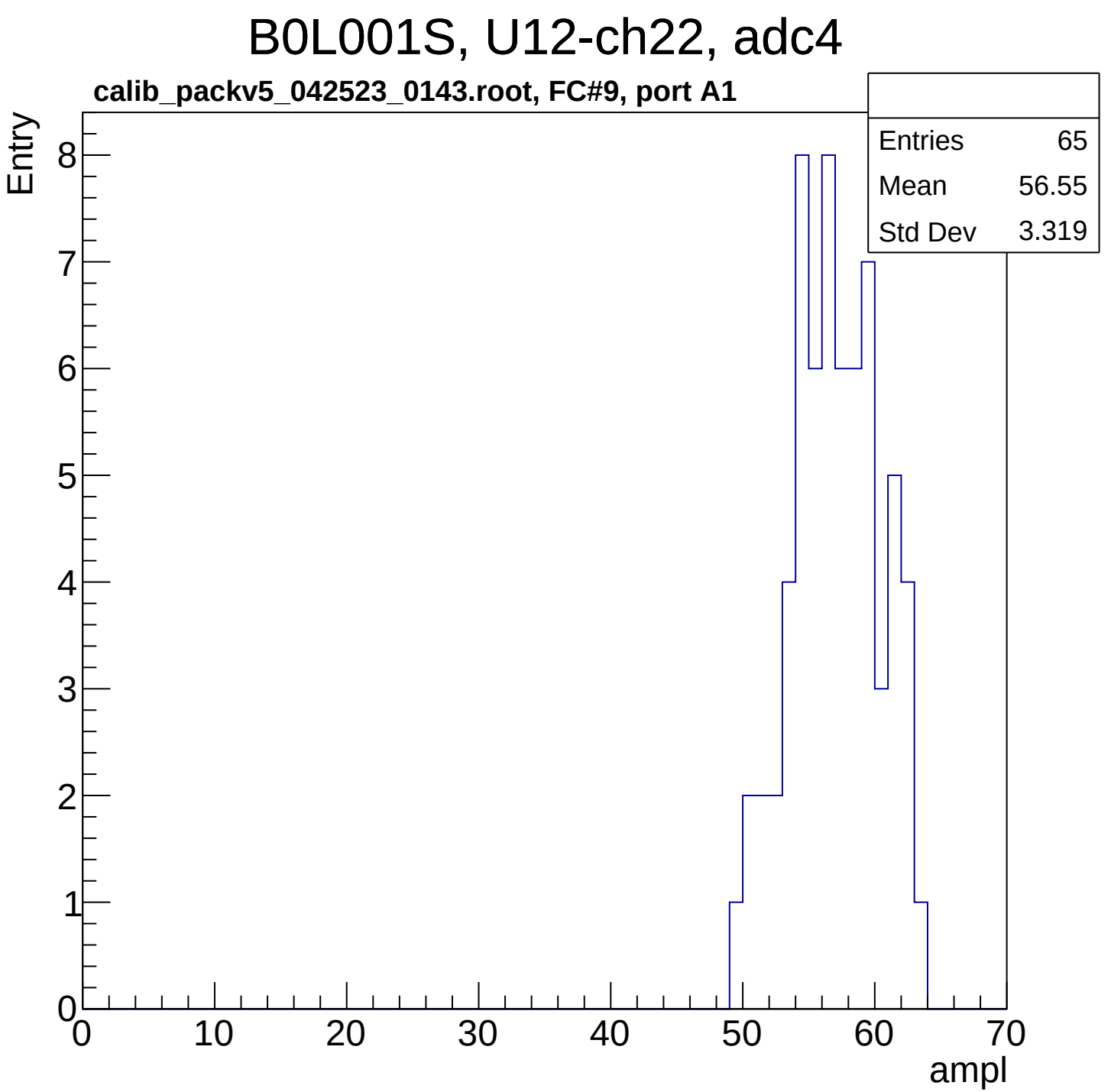
B0L001S, U12-ch22, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 65
Mean 56.55
Std Dev 3.319
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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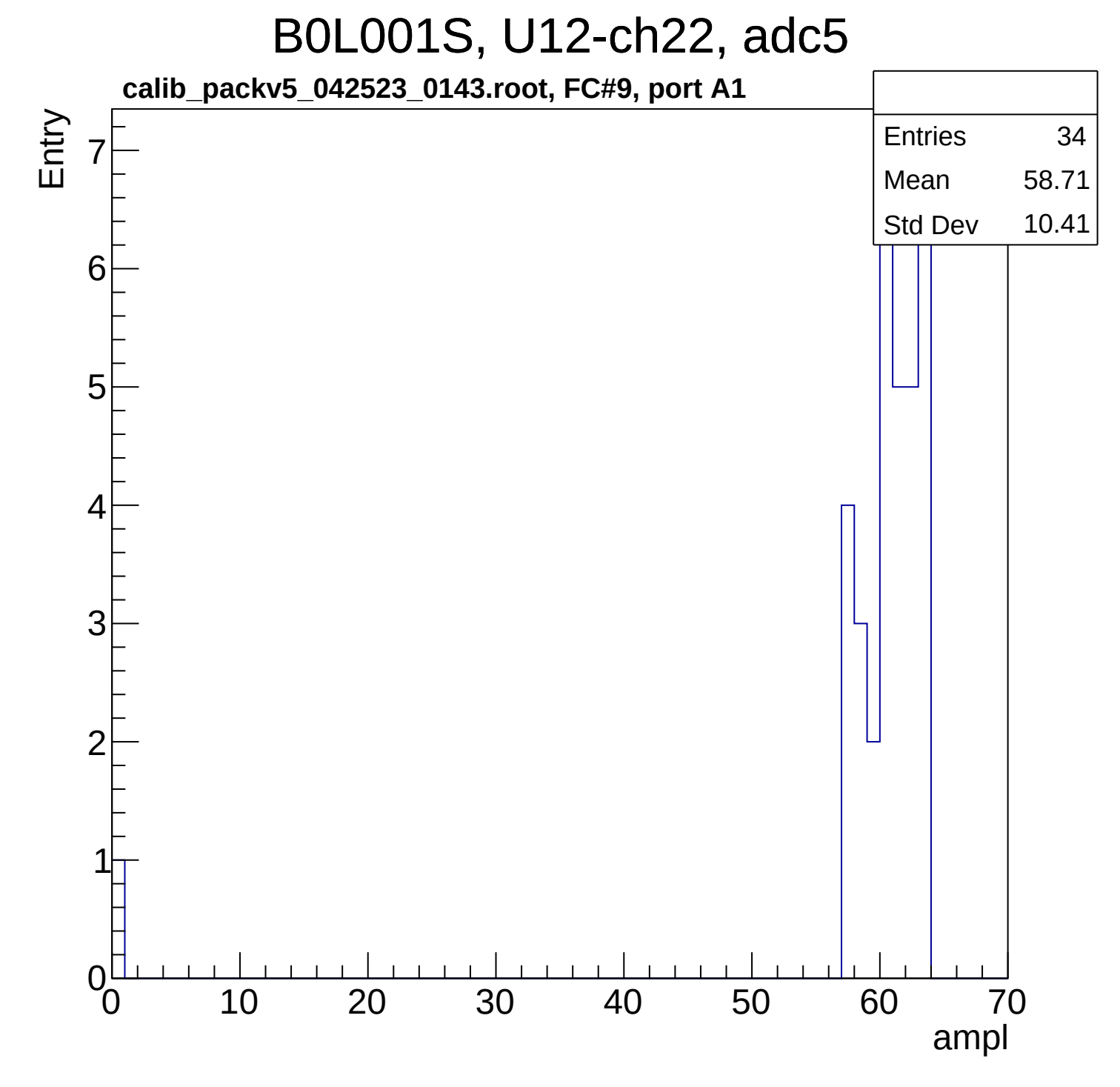
B0L001S, U12-ch22, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 34
Mean 58.71
Std Dev 10.41
Entry
ampl
0
1
2
3
4
5
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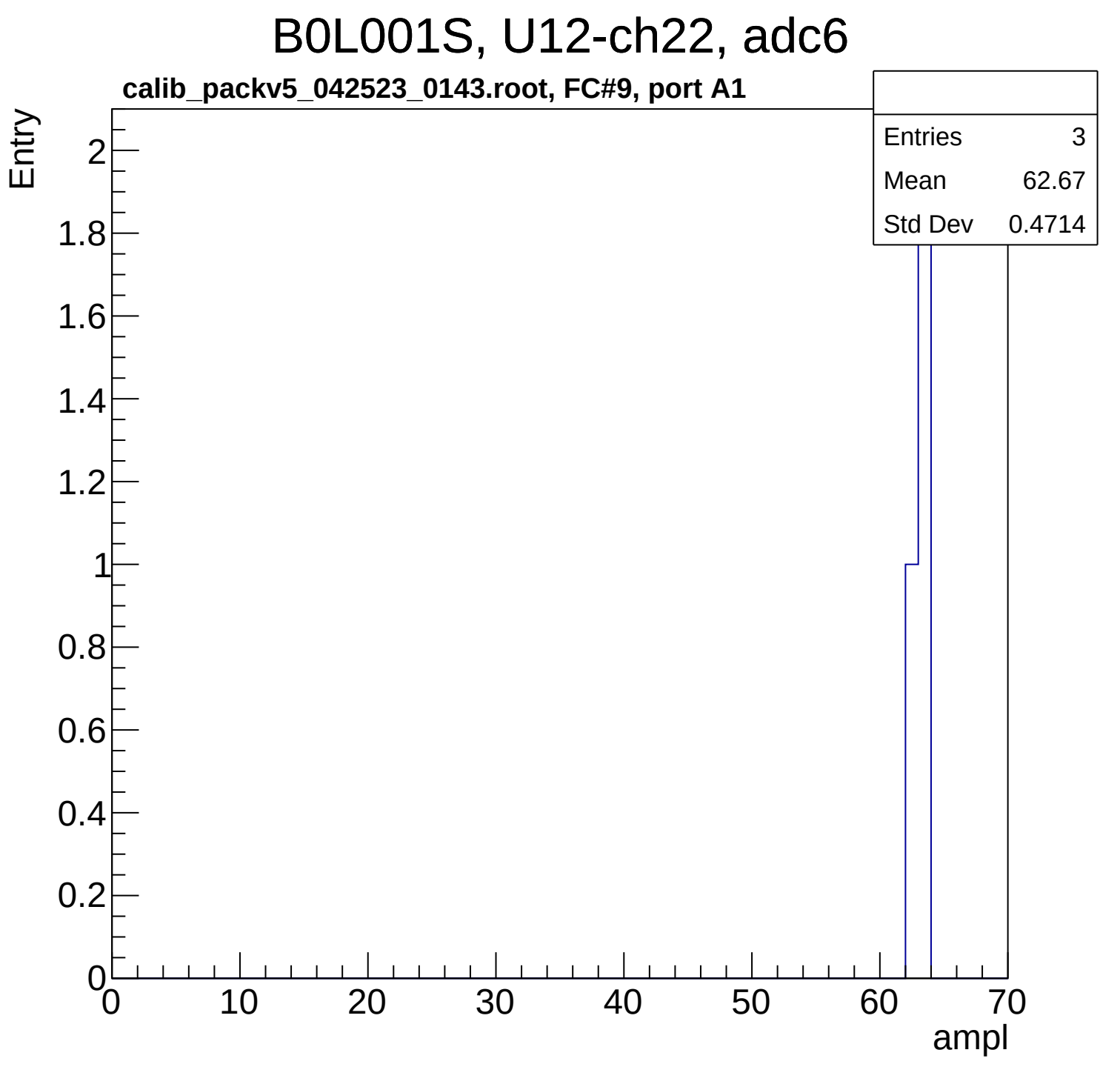
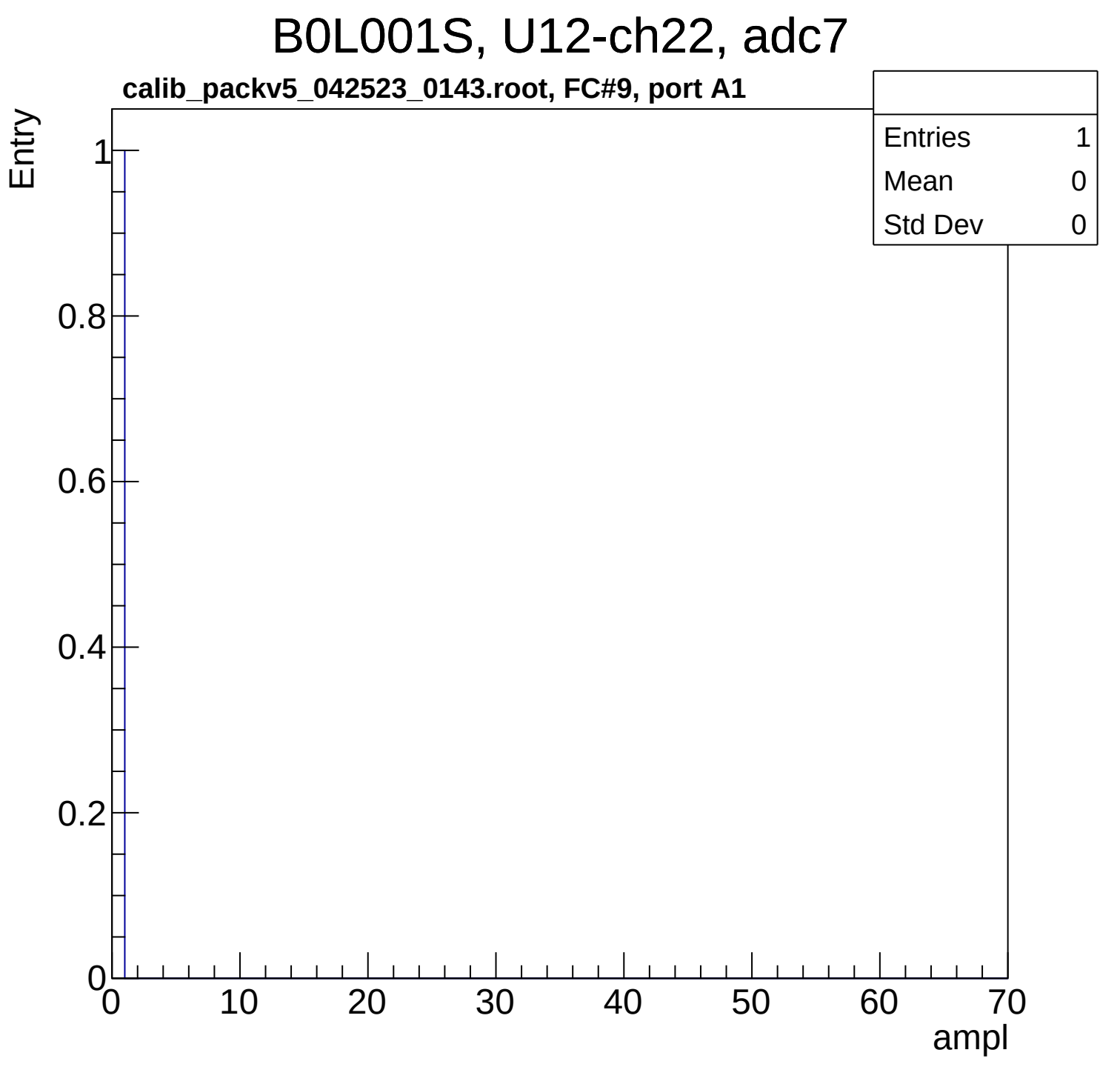

B0L001S, U12-ch22, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L001S, U12-ch22, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 0
Std Dev 0
Entry
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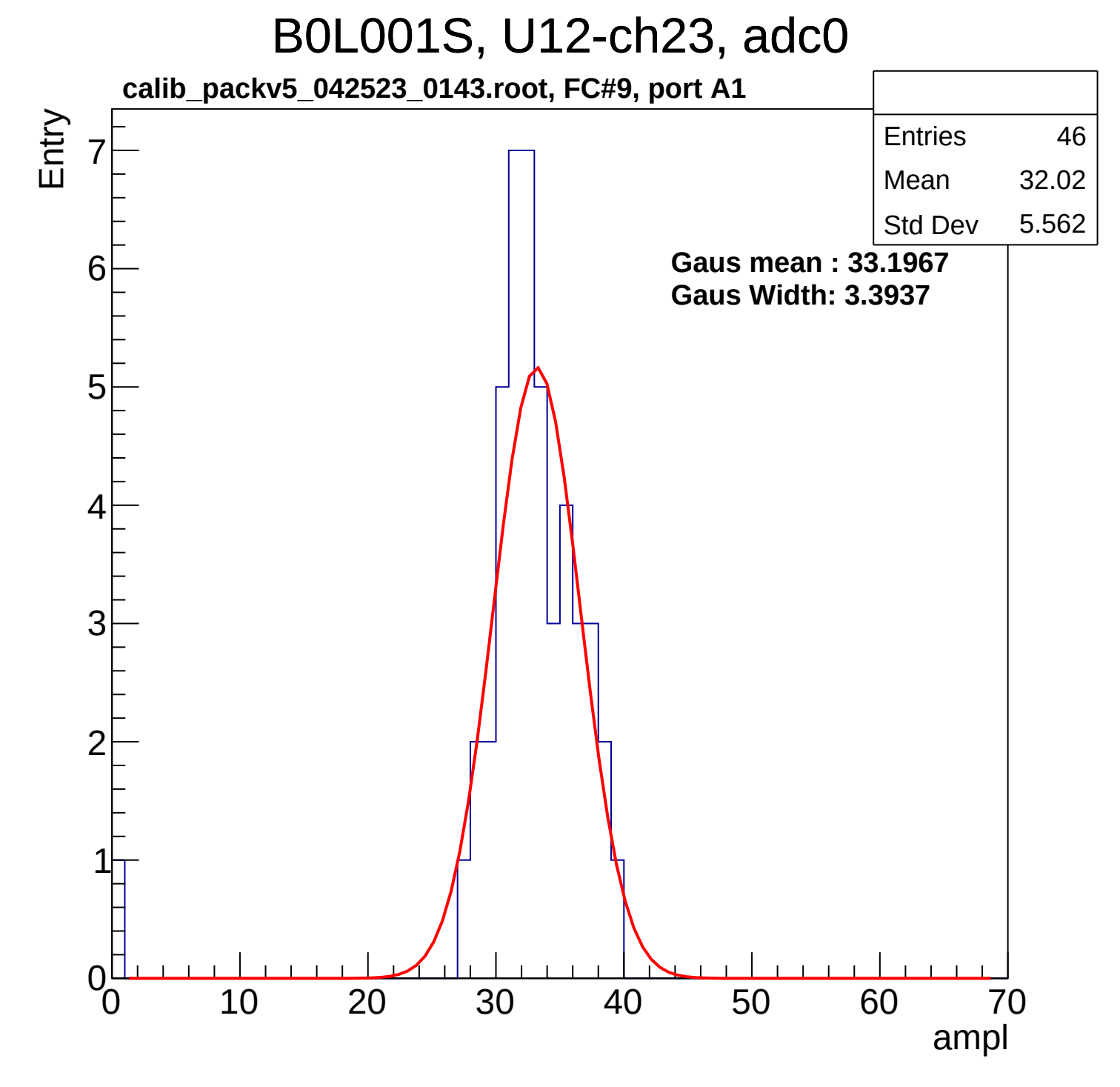
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch23, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 46
Mean 32.02
Std Dev 5.562
Gaus mean : 33.1967
Gaus Width: 3.3937
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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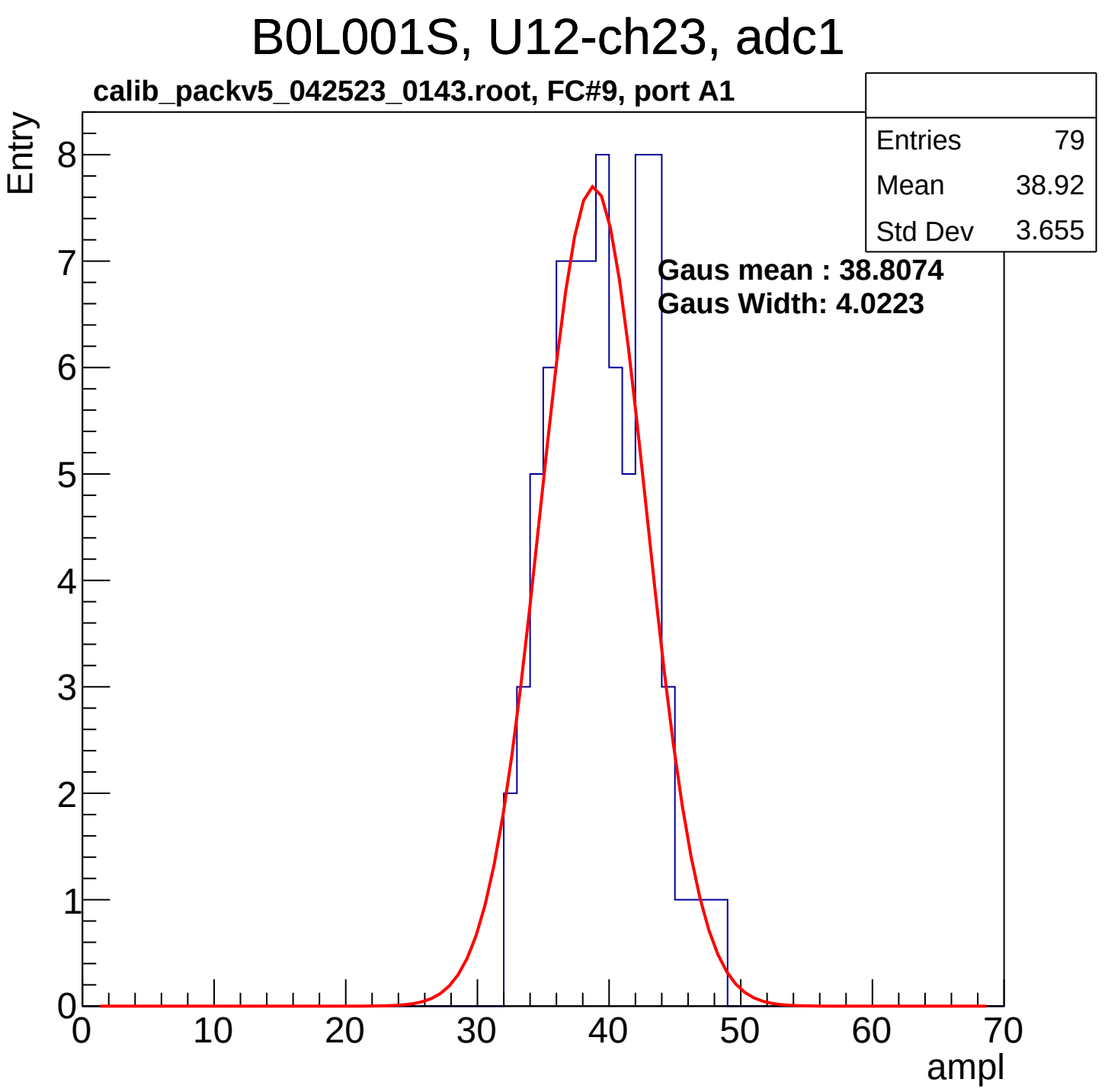
B0L001S, U12-ch23, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 79
Mean 38.92
Std Dev 3.655
Gaus mean : 38.8074
Gaus Width: 4.0223
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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40
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60
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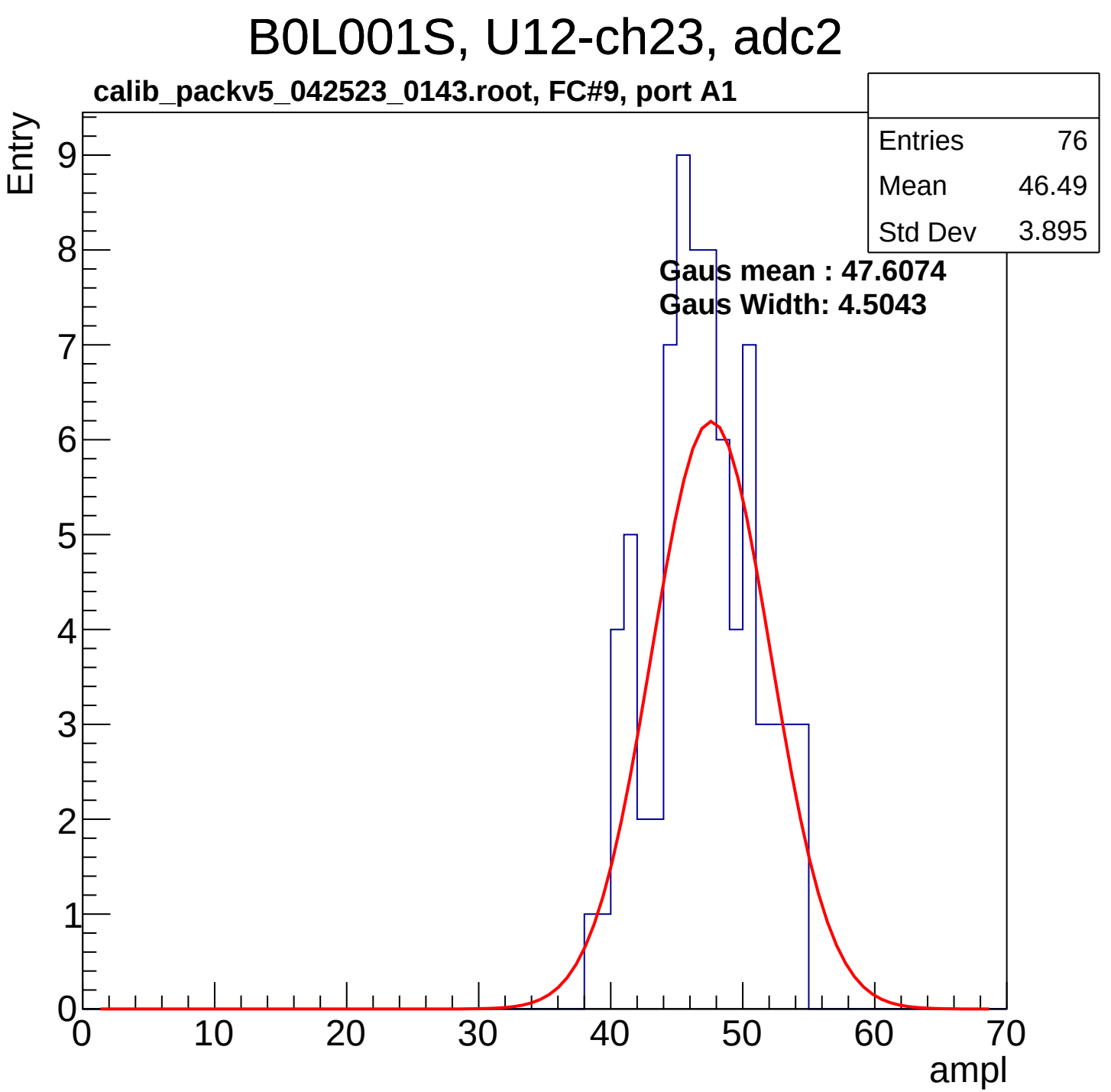
B0L001S, U12-ch23, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 76
Mean 46.49
Std Dev 3.895
Gaus mean : 47.6074
Gaus Width: 4.5043
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
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40
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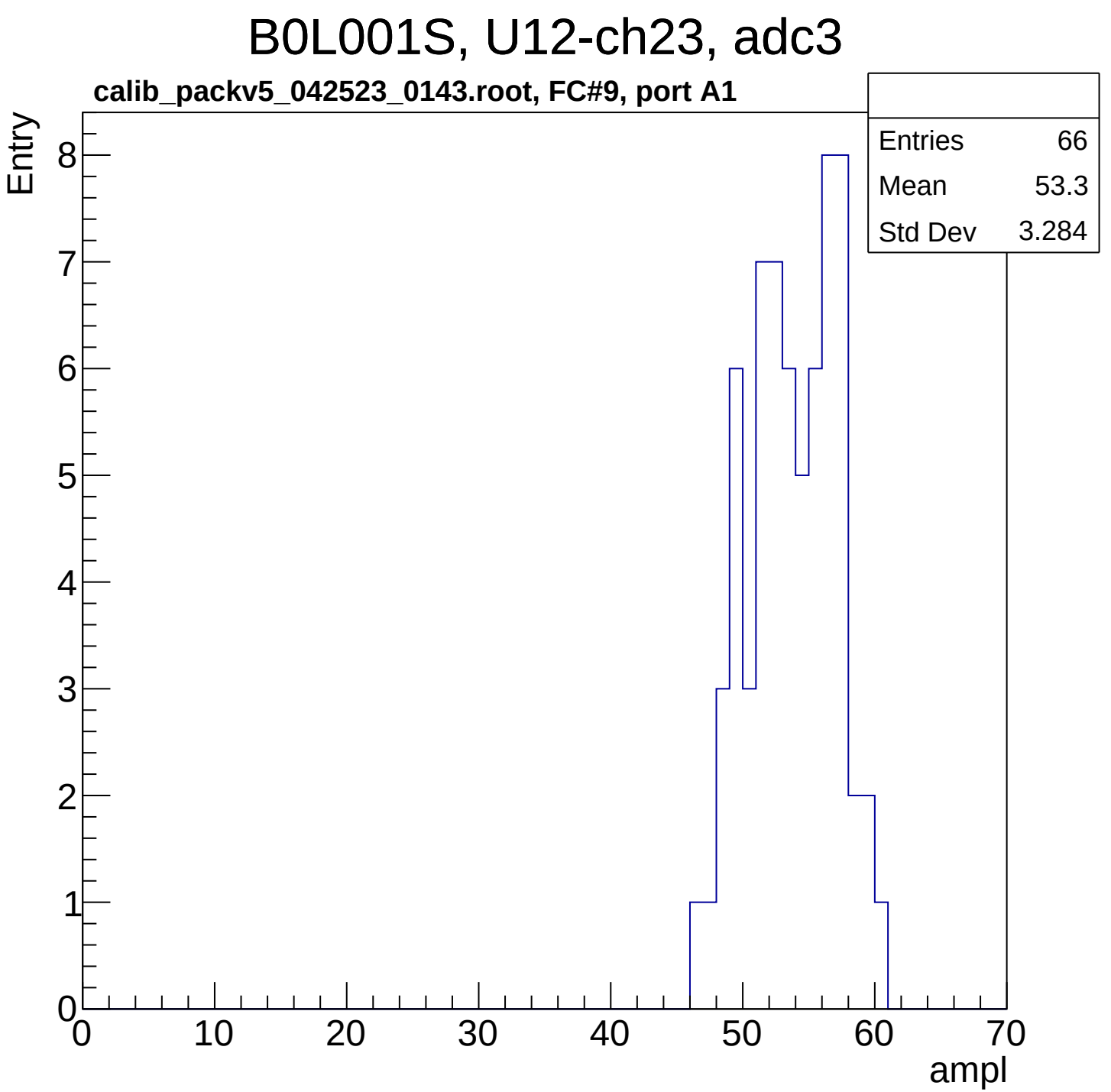
B0L001S, U12-ch23, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 66
Mean 53.3
Std Dev 3.284
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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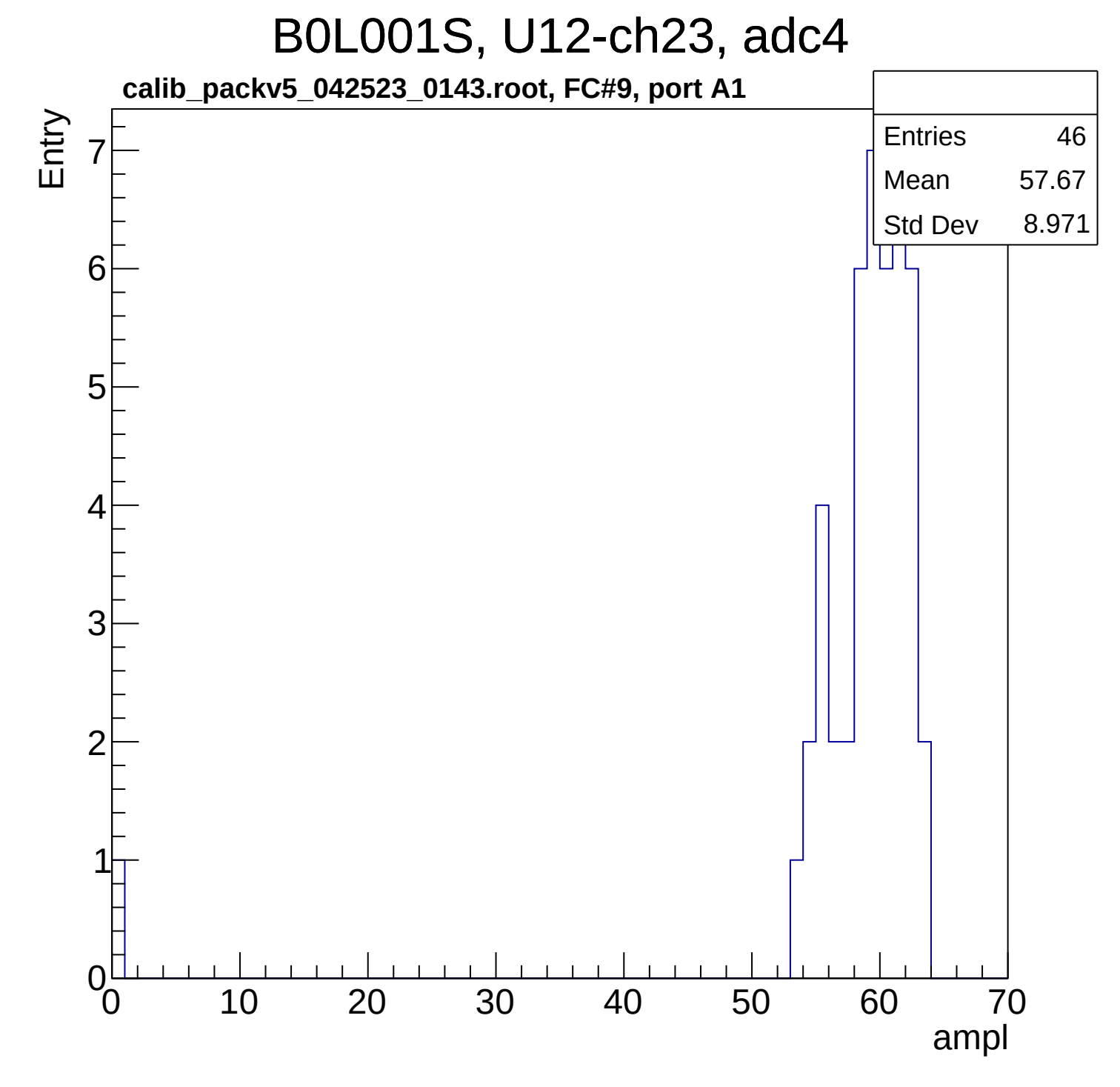
B0L001S, U12-ch23, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 46
Mean 57.67
Std Dev 8.971
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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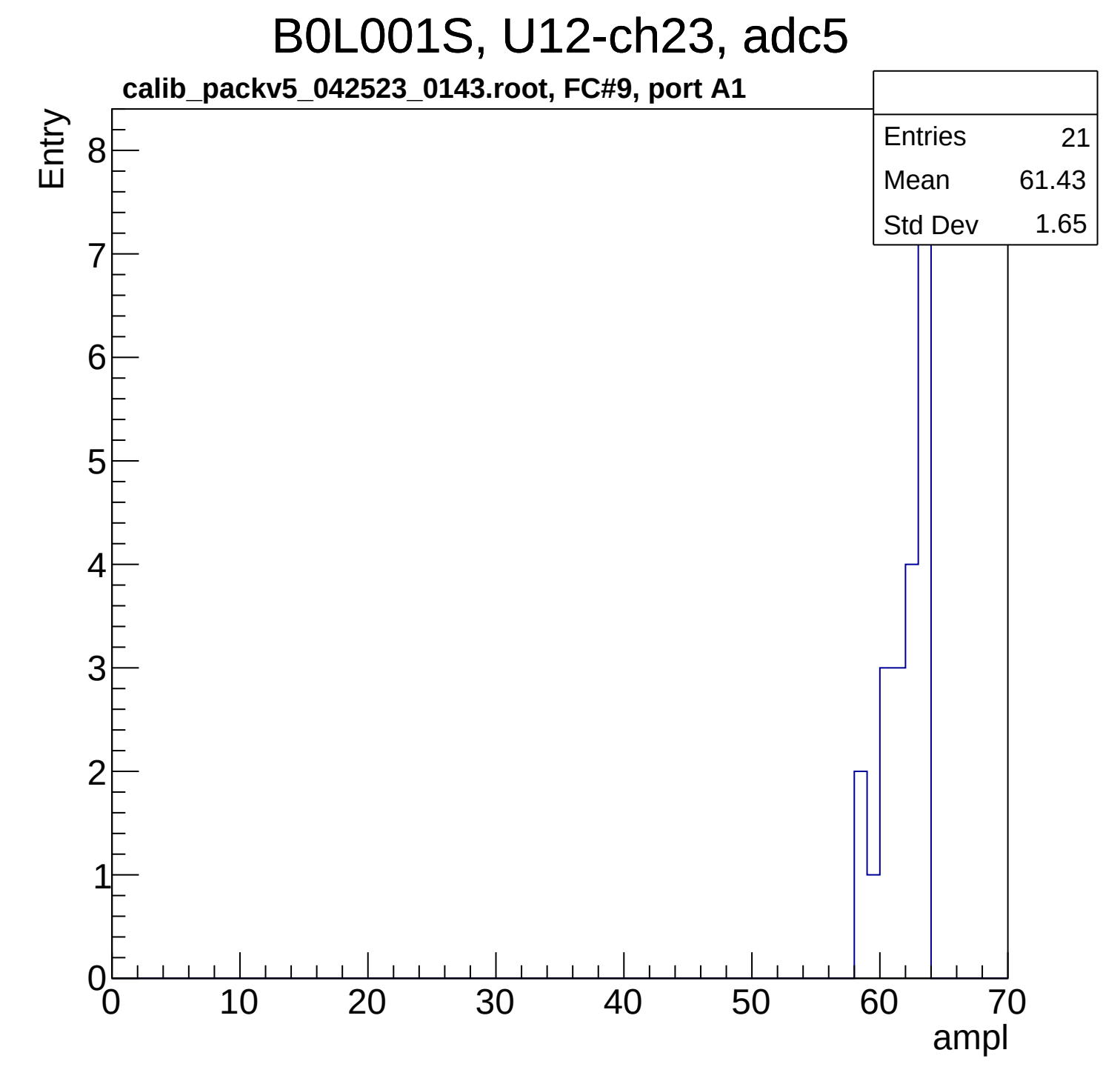
B0L001S, U12-ch23, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 21
Mean 61.43
Std Dev 1.65
Entry
ampl
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1
2
3
4
5
6
7
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0
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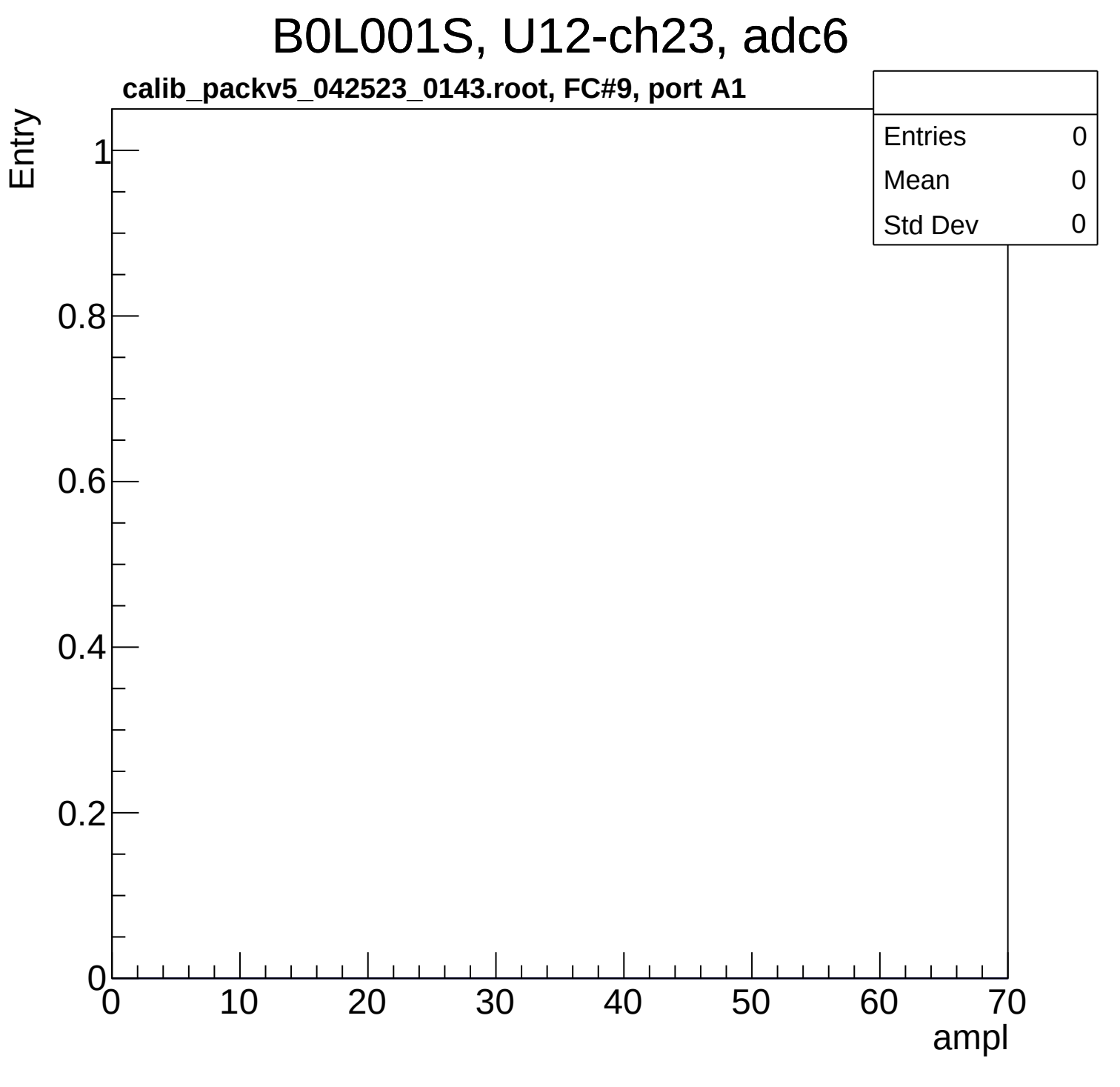
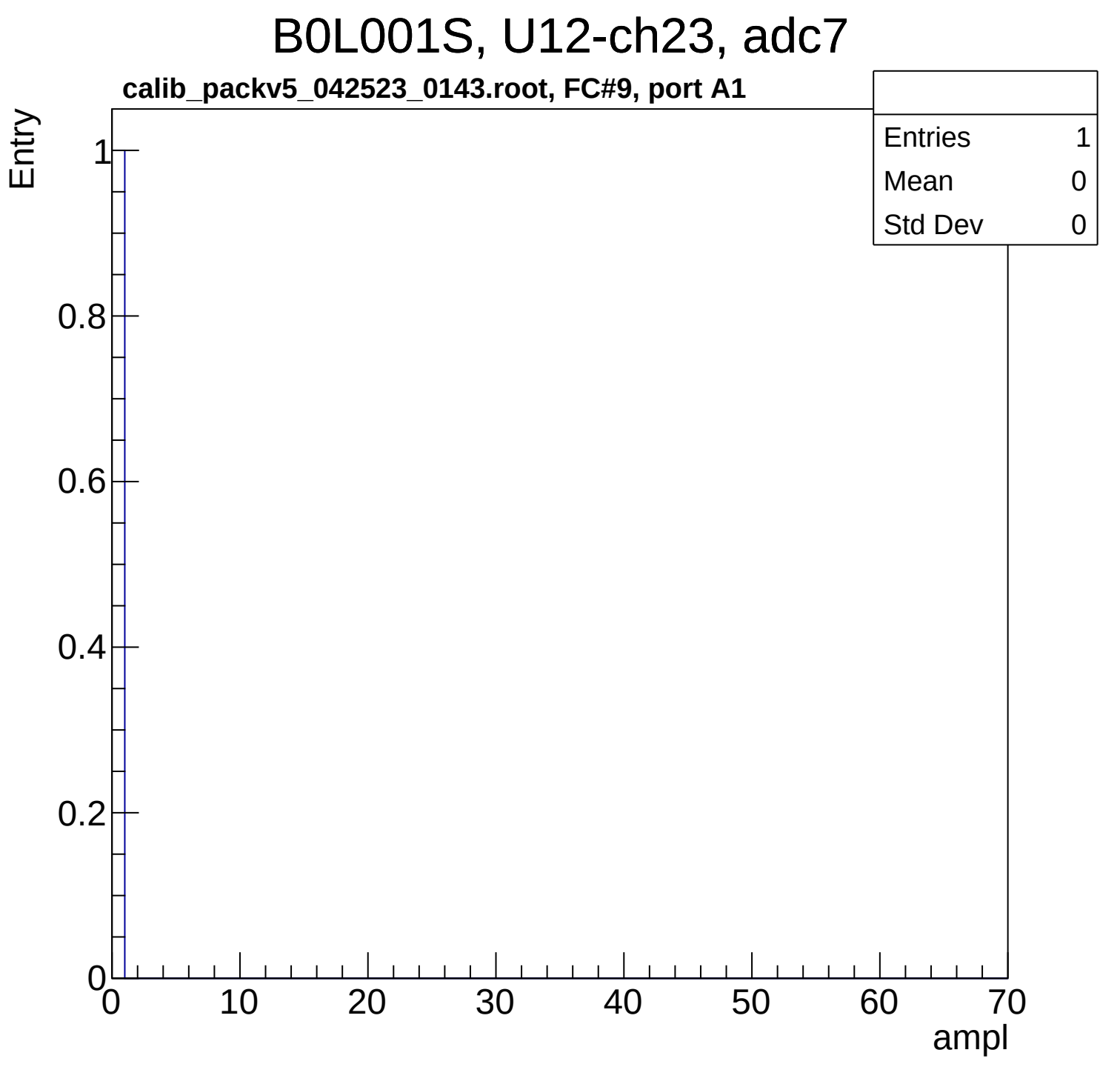
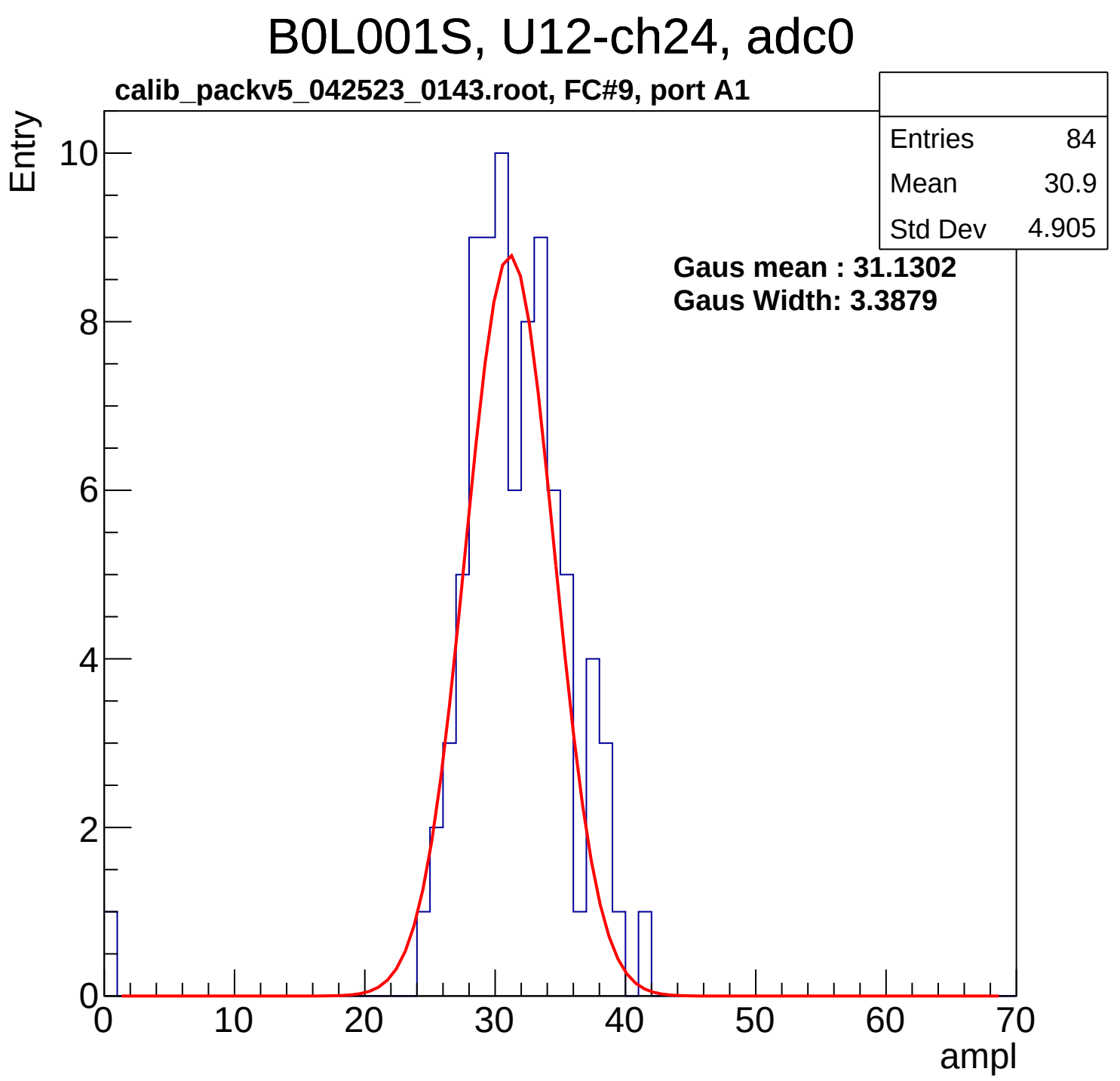
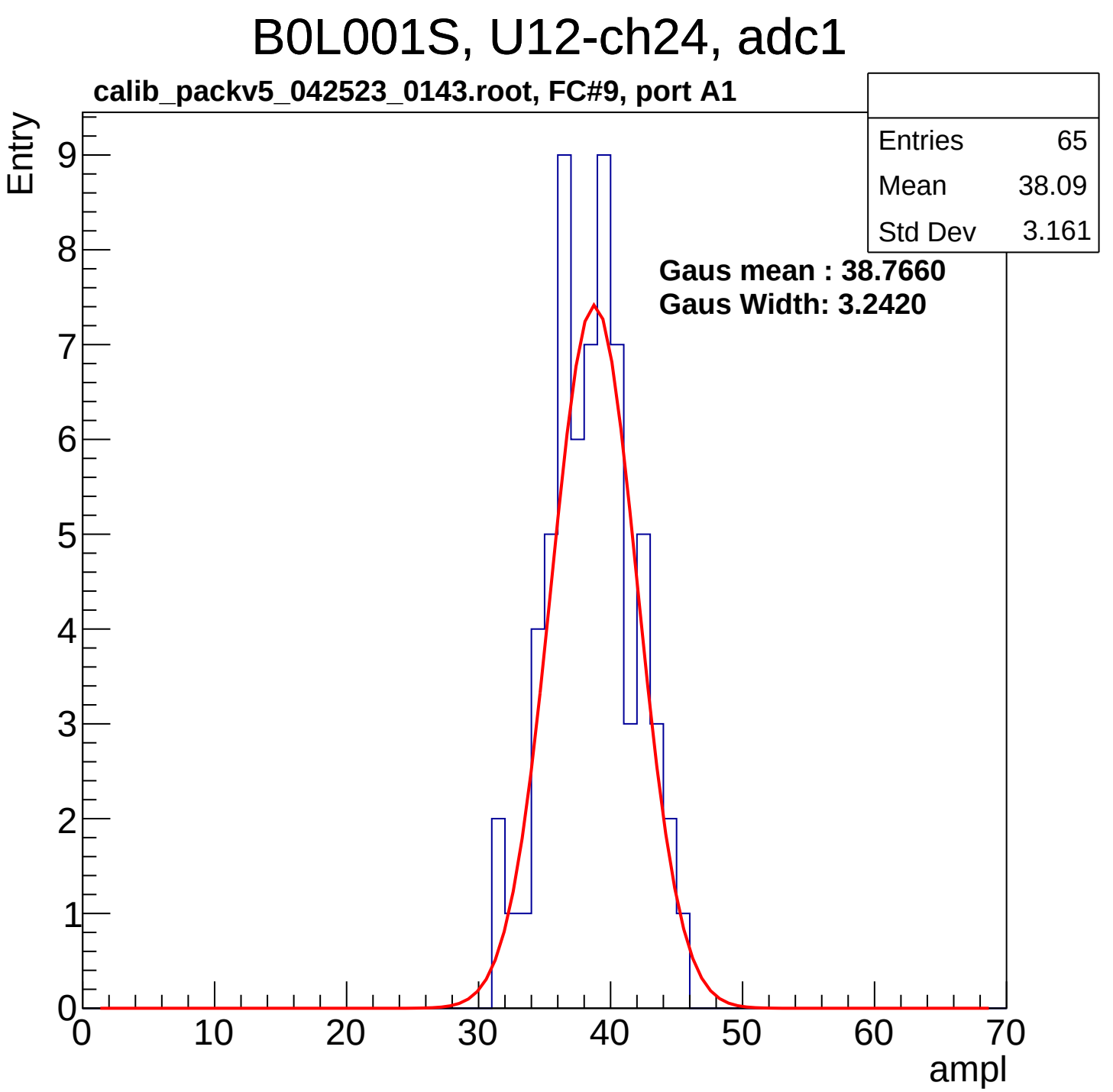

B0L001S, U12-ch23, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch23, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch24, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 84
Mean 30.9
Std Dev 4.905
Gaus mean : 31.1302
Gaus Width: 3.3879
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch24, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 65
Mean 38.09
Std Dev 3.161
Gaus mean : 38.7660
Gaus Width: 3.2420
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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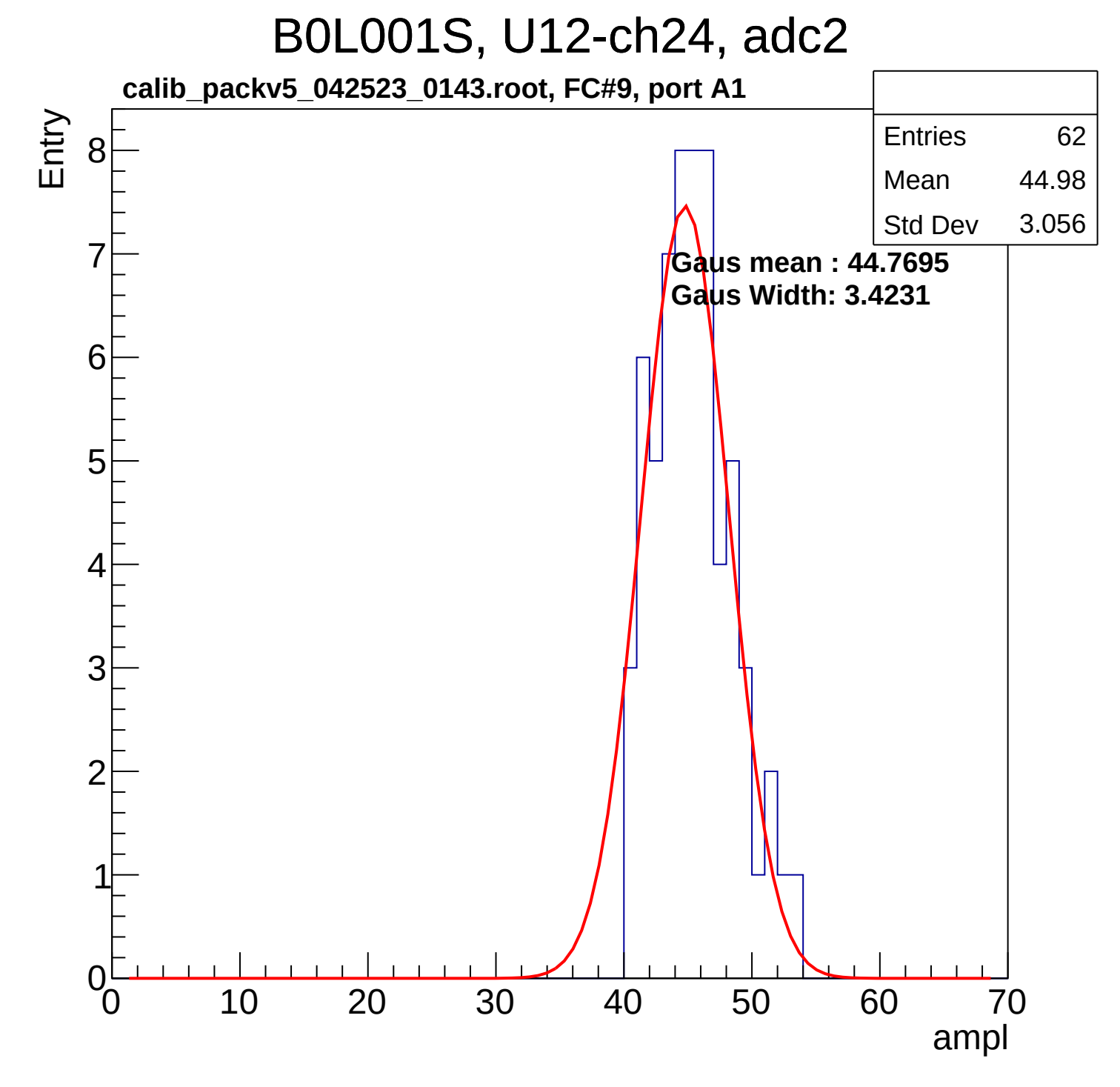
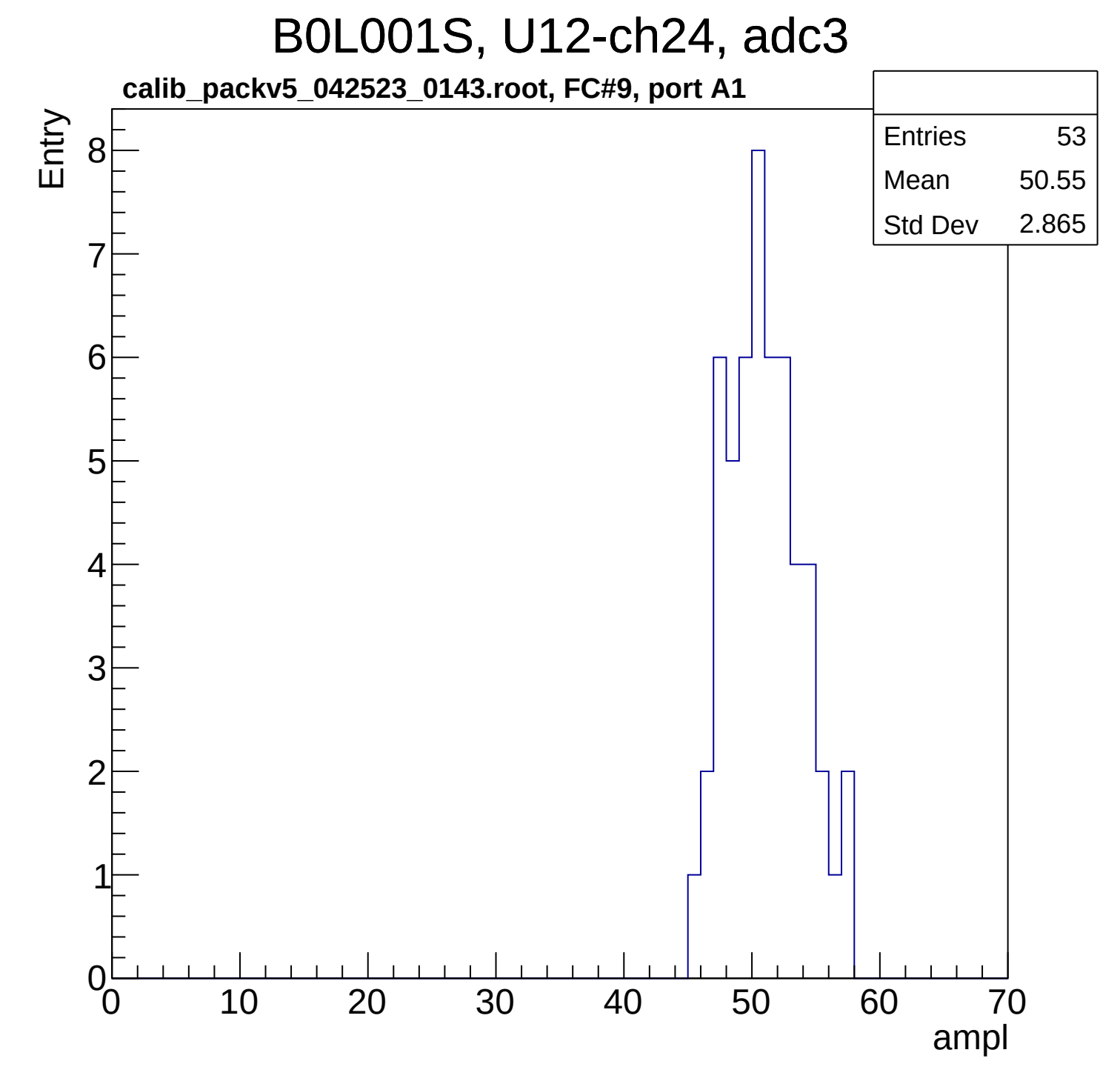
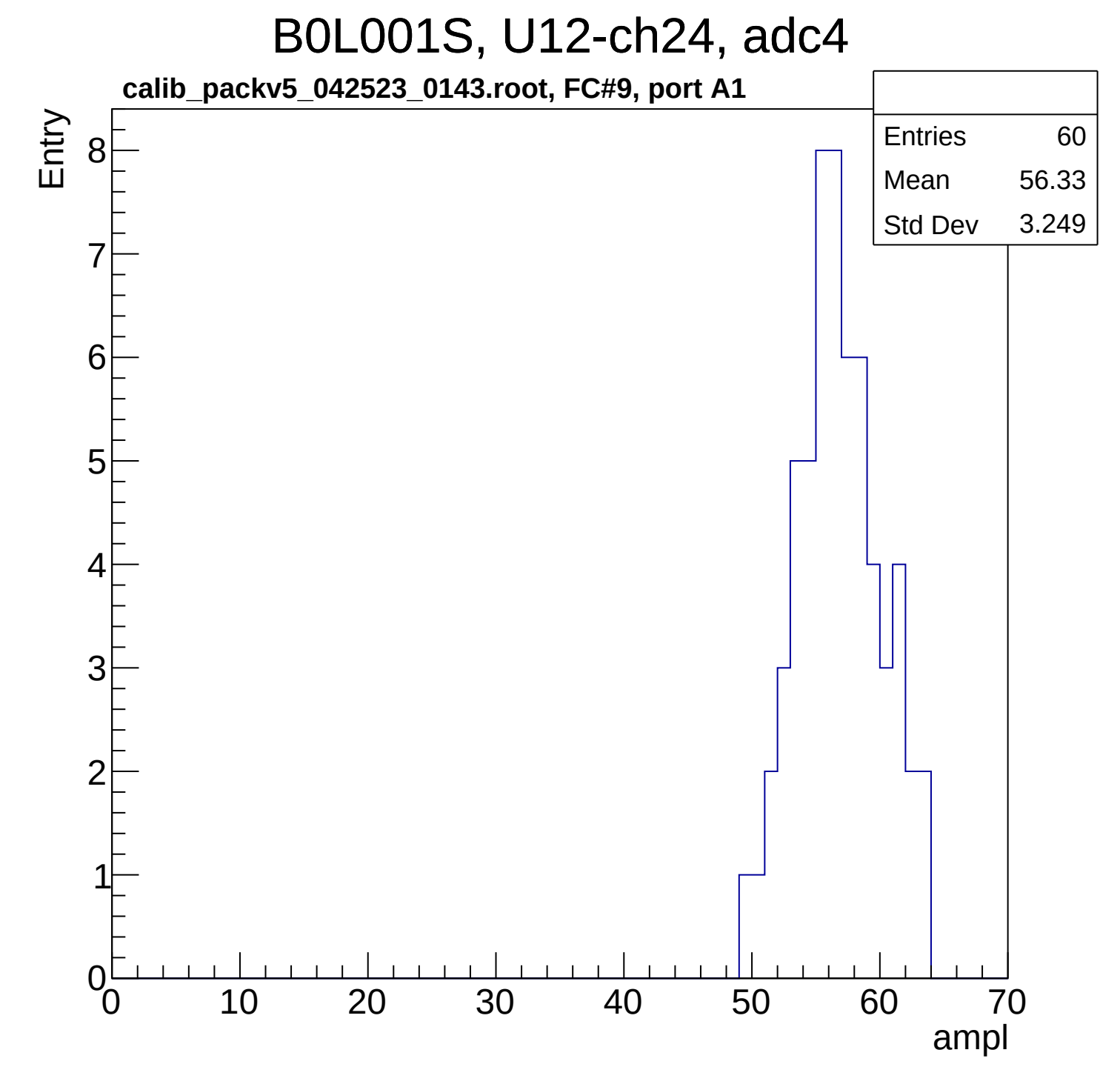

B0L001S, U12-ch24, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 62
Mean 44.98
Std Dev 3.056
Gaus mean : 44.7695
Gaus Width: 3.4231
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch24, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 53
Mean 50.55
Std Dev 2.865
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch24, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 60
Mean 56.33
Std Dev 3.249
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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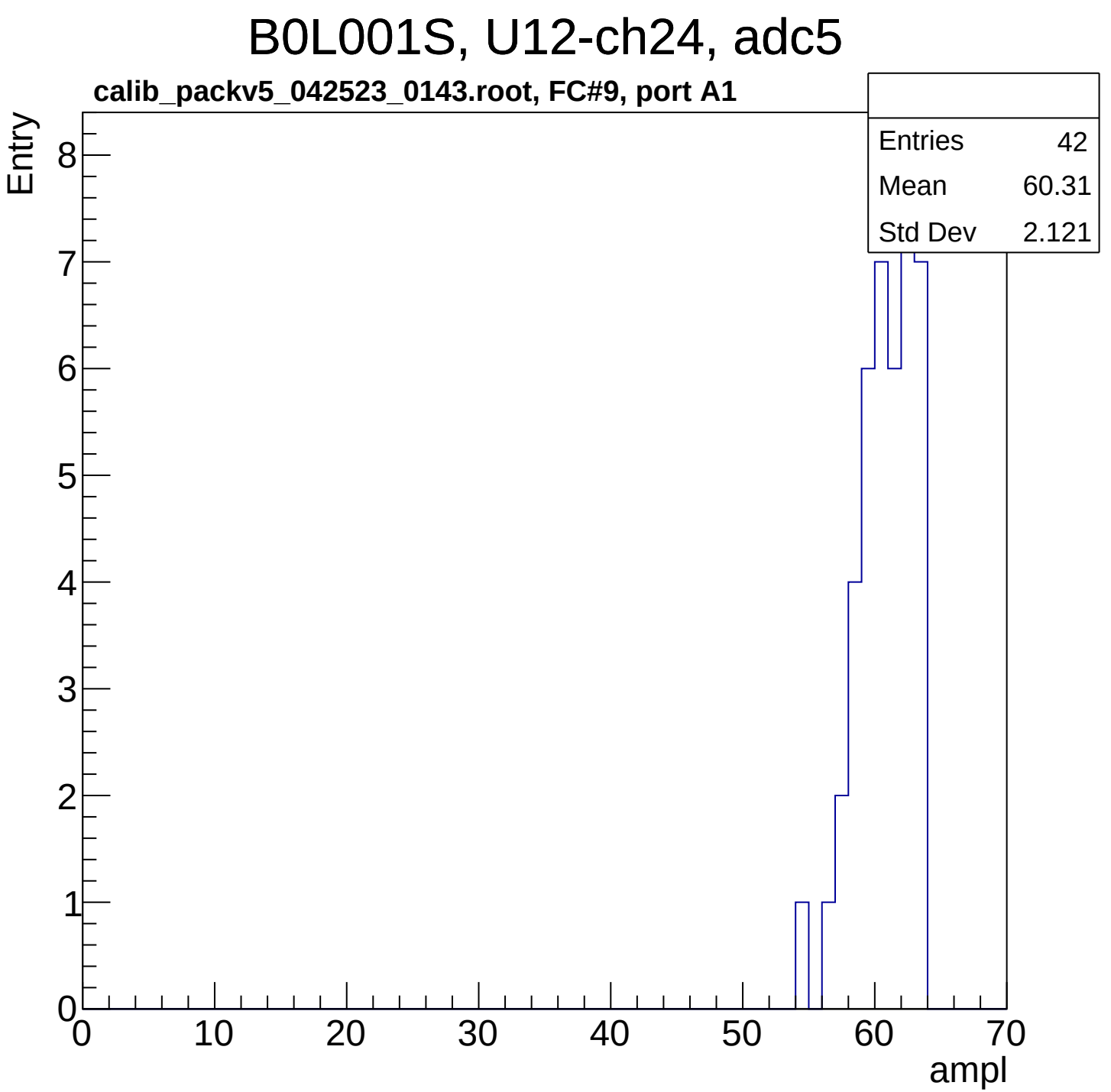
B0L001S, U12-ch24, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 42
Mean 60.31
Std Dev 2.121
Entry
ampl
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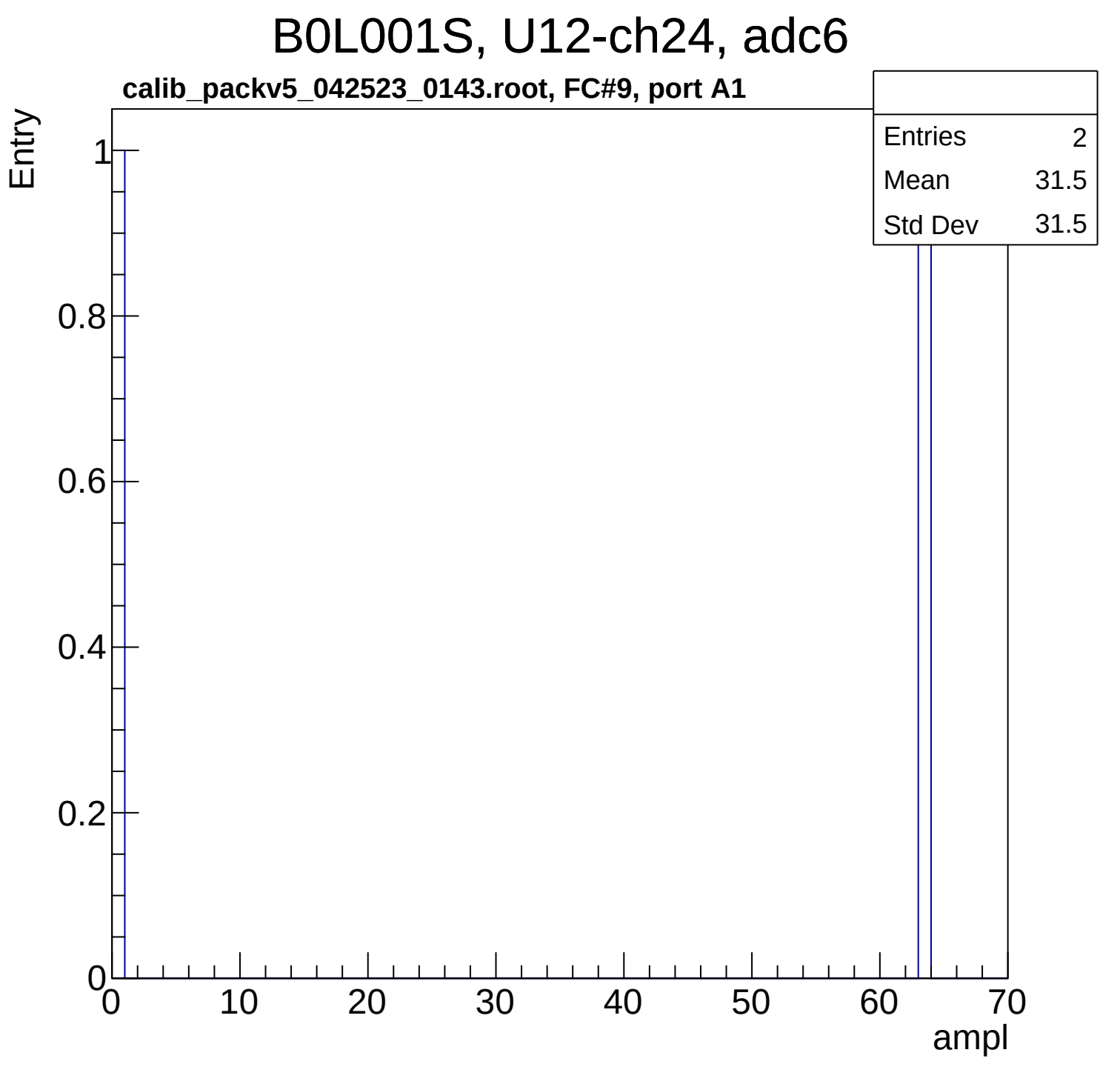
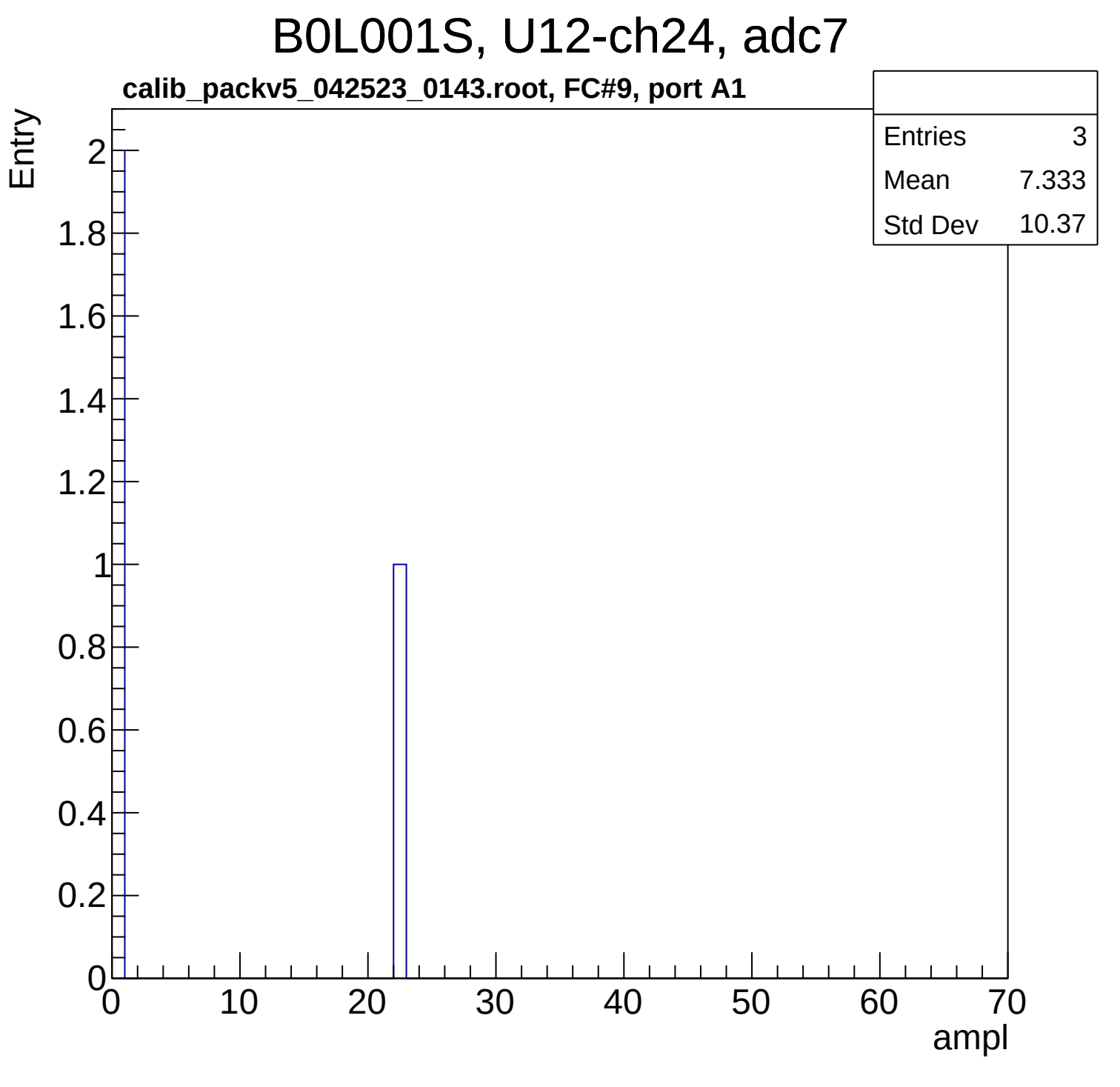
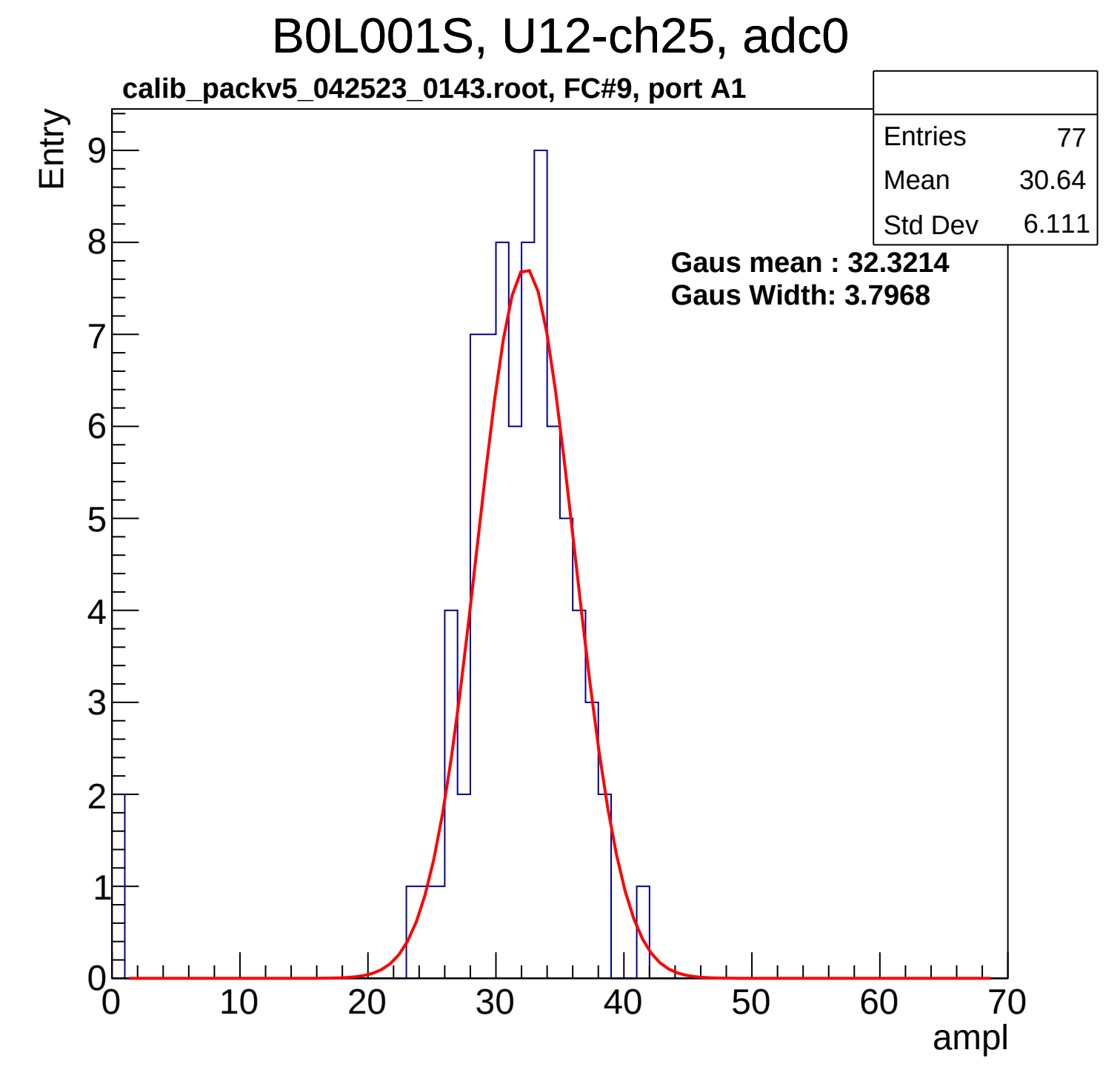
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch24, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch24, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 3
Mean 7.333
Std Dev 10.37
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L001S, U12-ch25, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 77
Mean 30.64
Std Dev 6.111
Gaus mean : 32.3214
Gaus Width: 3.7968
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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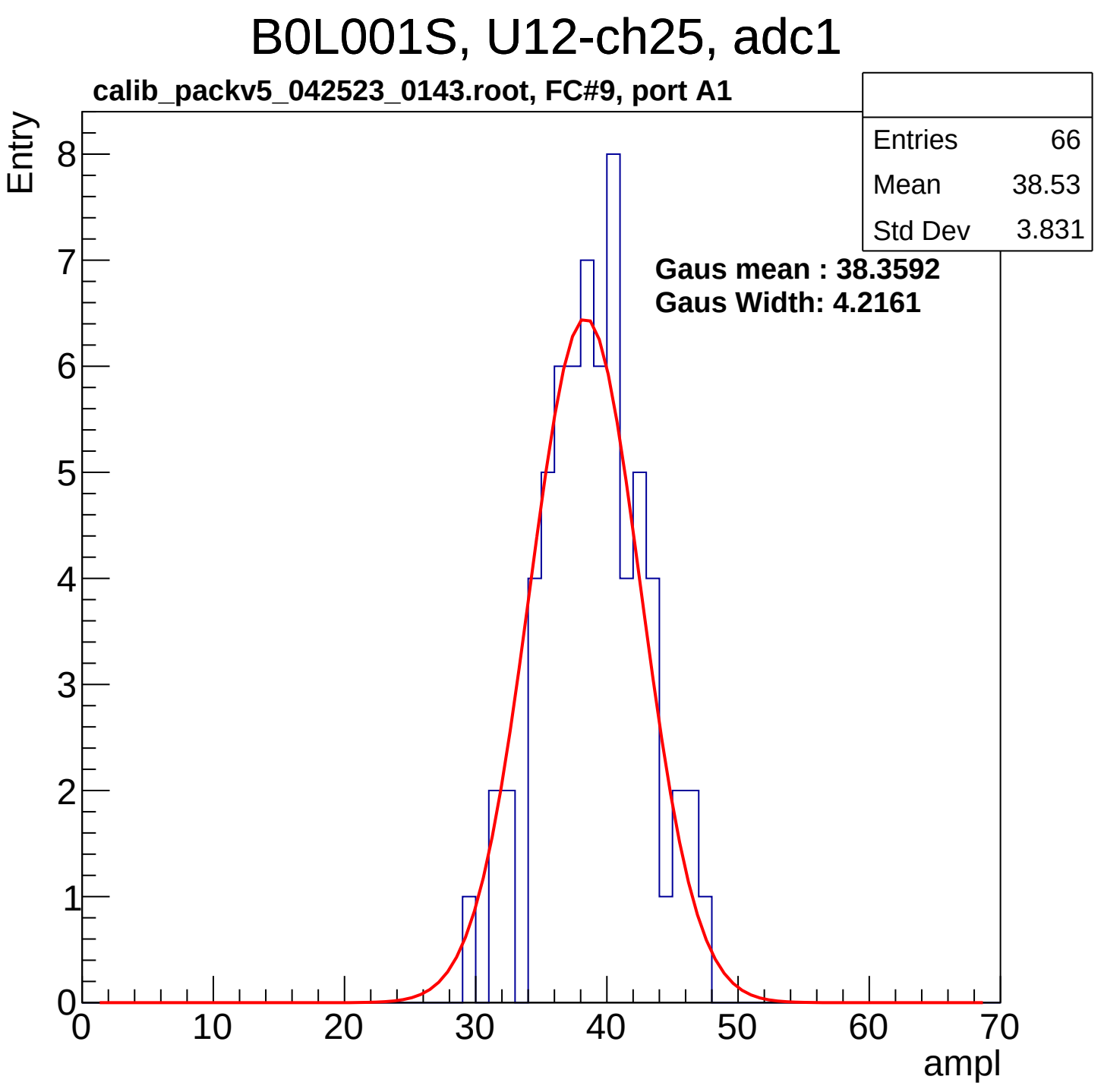
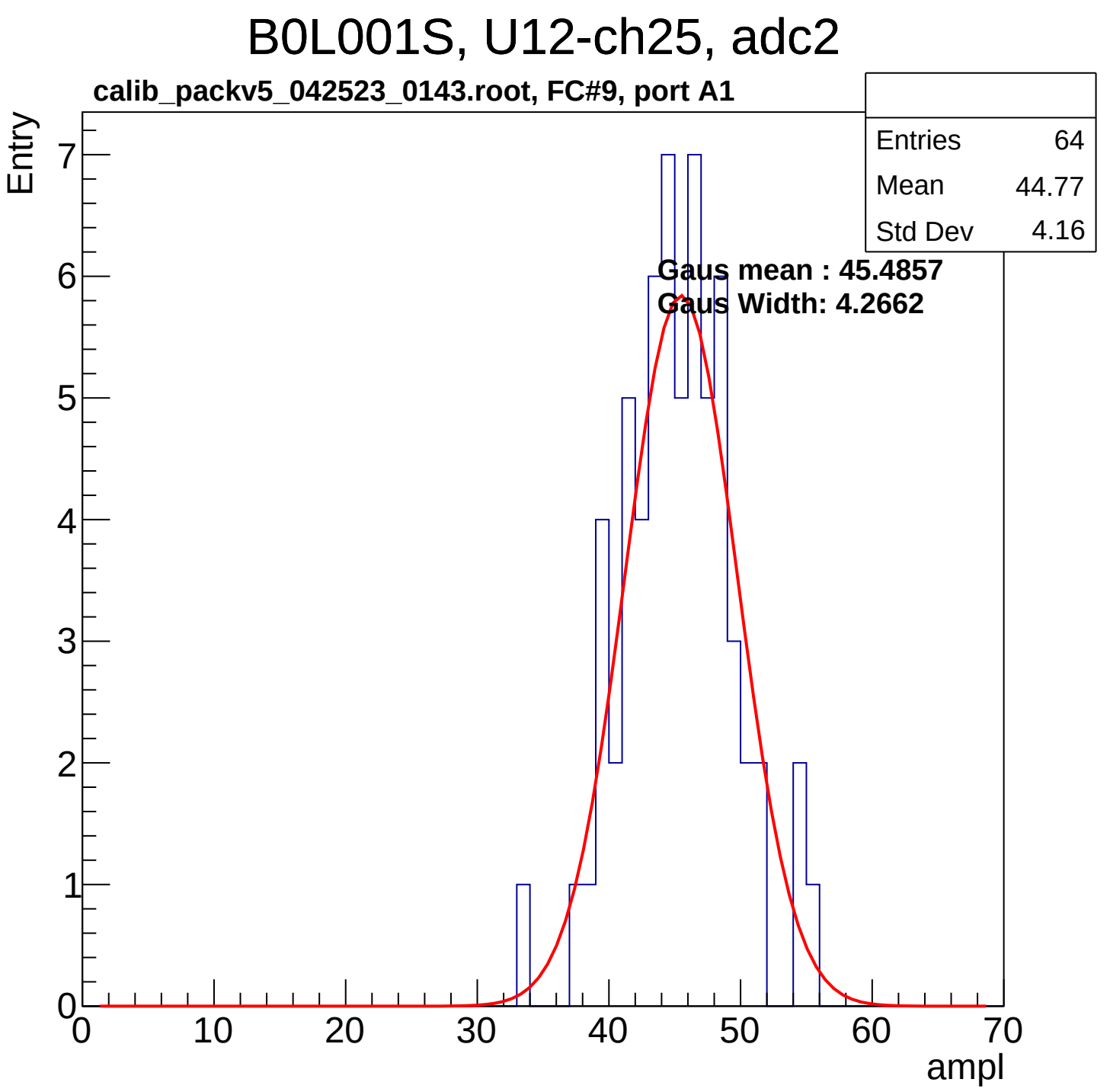

B0L001S, U12-ch25, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 66
Mean 38.53
Std Dev 3.831
Gaus mean : 38.3592
Gaus Width: 4.2161
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch25, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 64
Mean 44.77
Std Dev 4.16
Gaus mean : 45.4857
Gaus Width: 4.2662
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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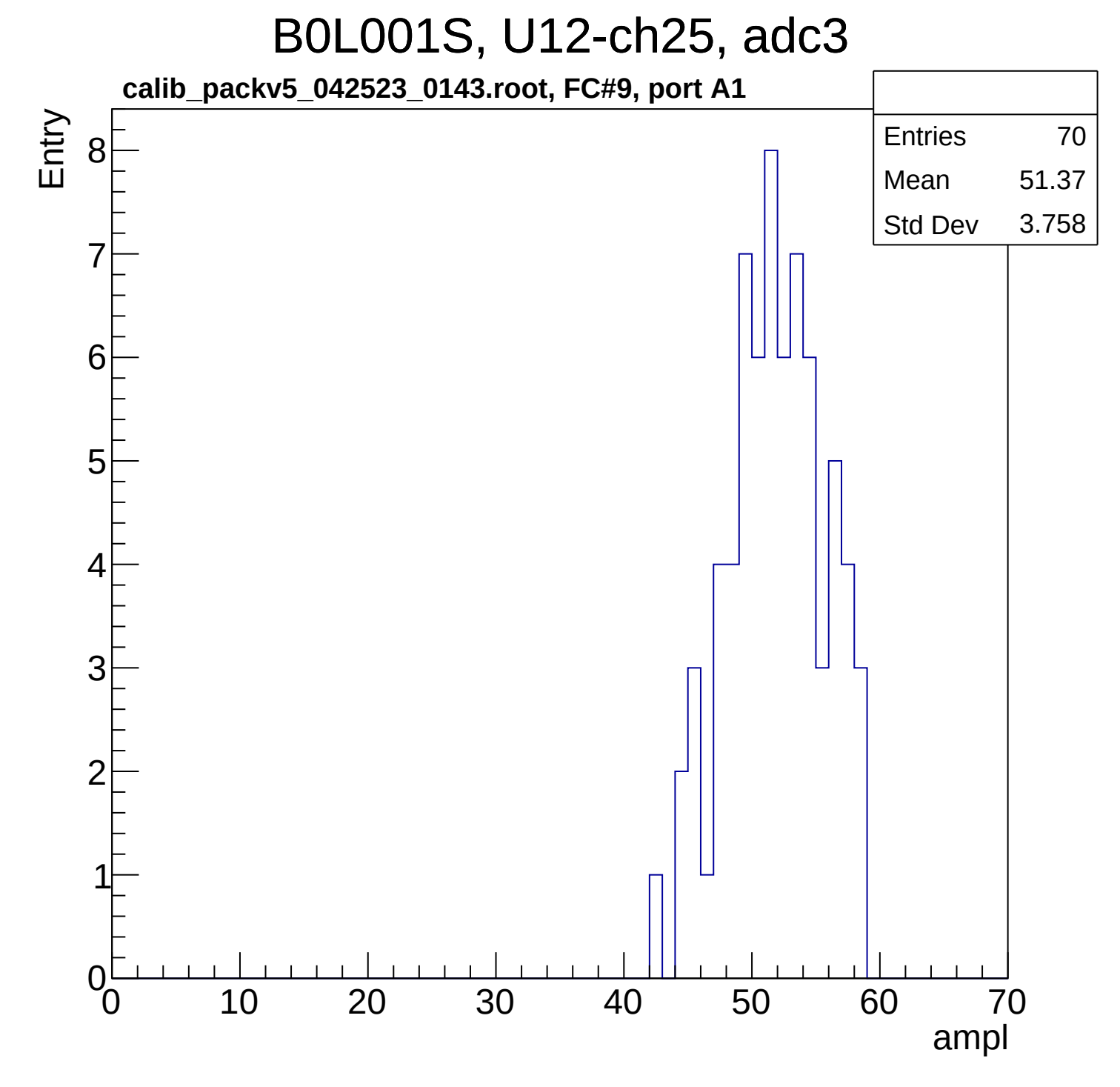
B0L001S, U12-ch25, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 70
Mean 51.37
Std Dev 3.758
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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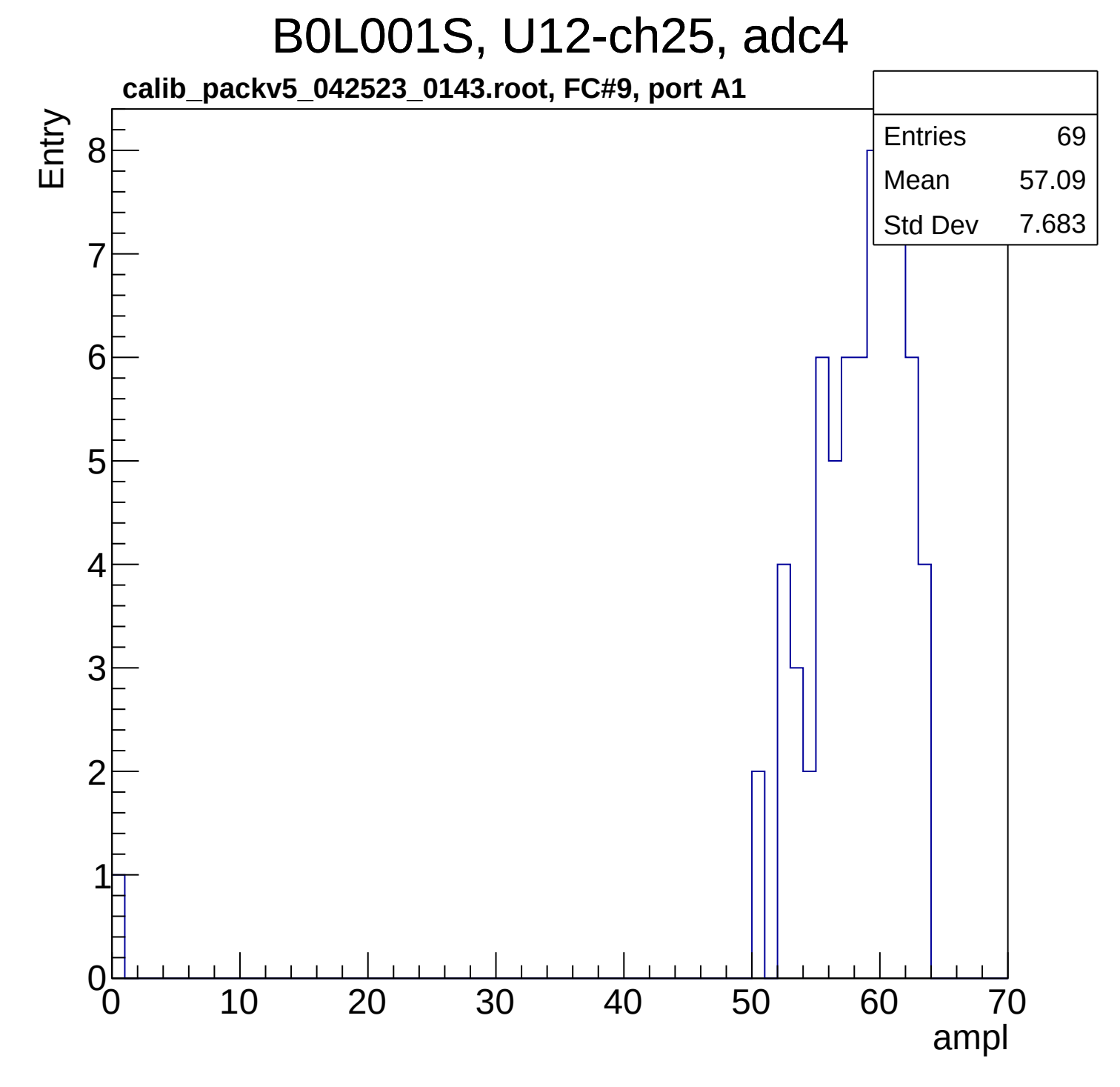
40
50
60
70


B0L001S, U12-ch25, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 69
Mean 57.09
Std Dev 7.683
Entry
ampl
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2
3
4
5
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7
8
0
10
20
30
40
50
60
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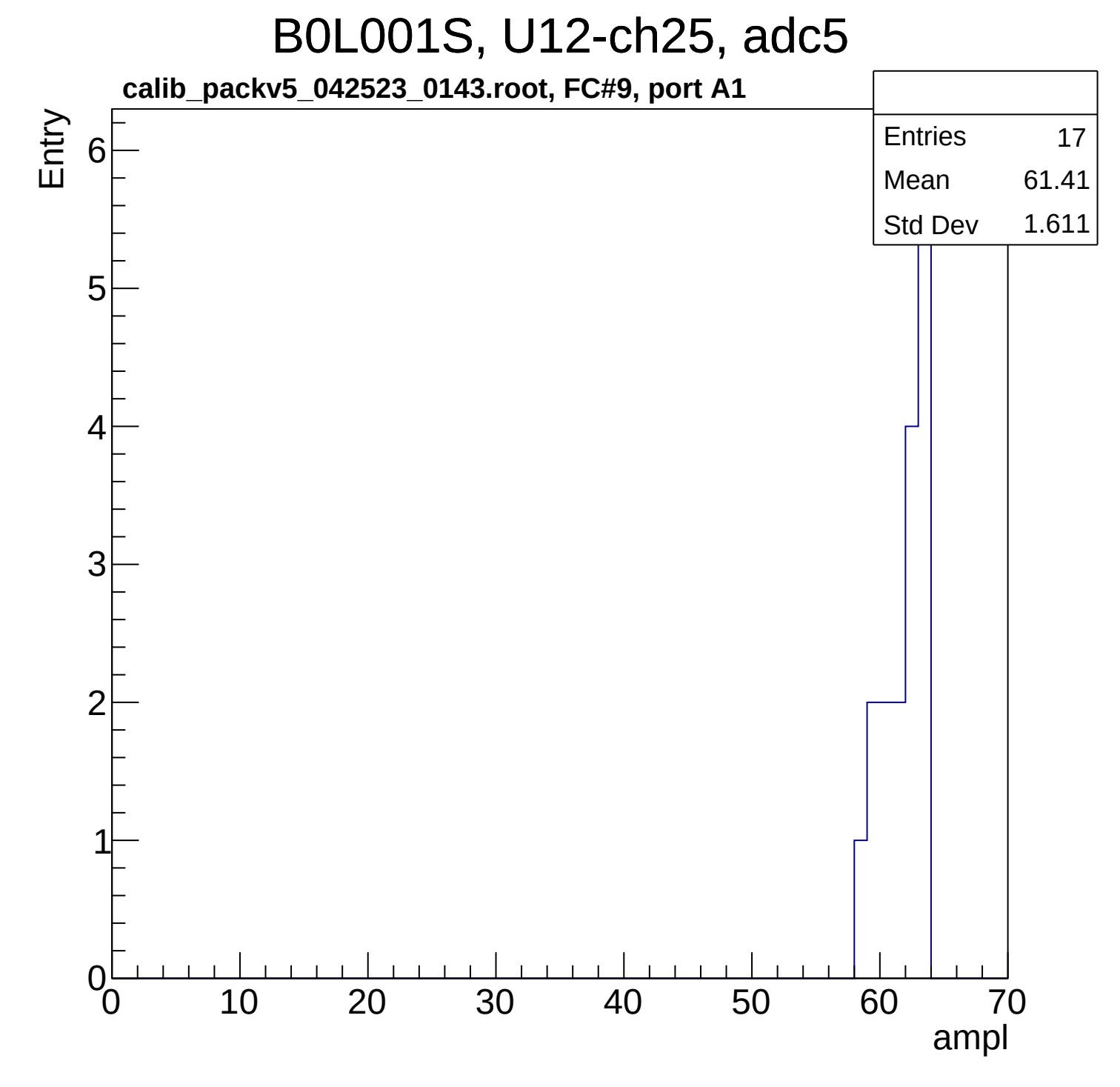
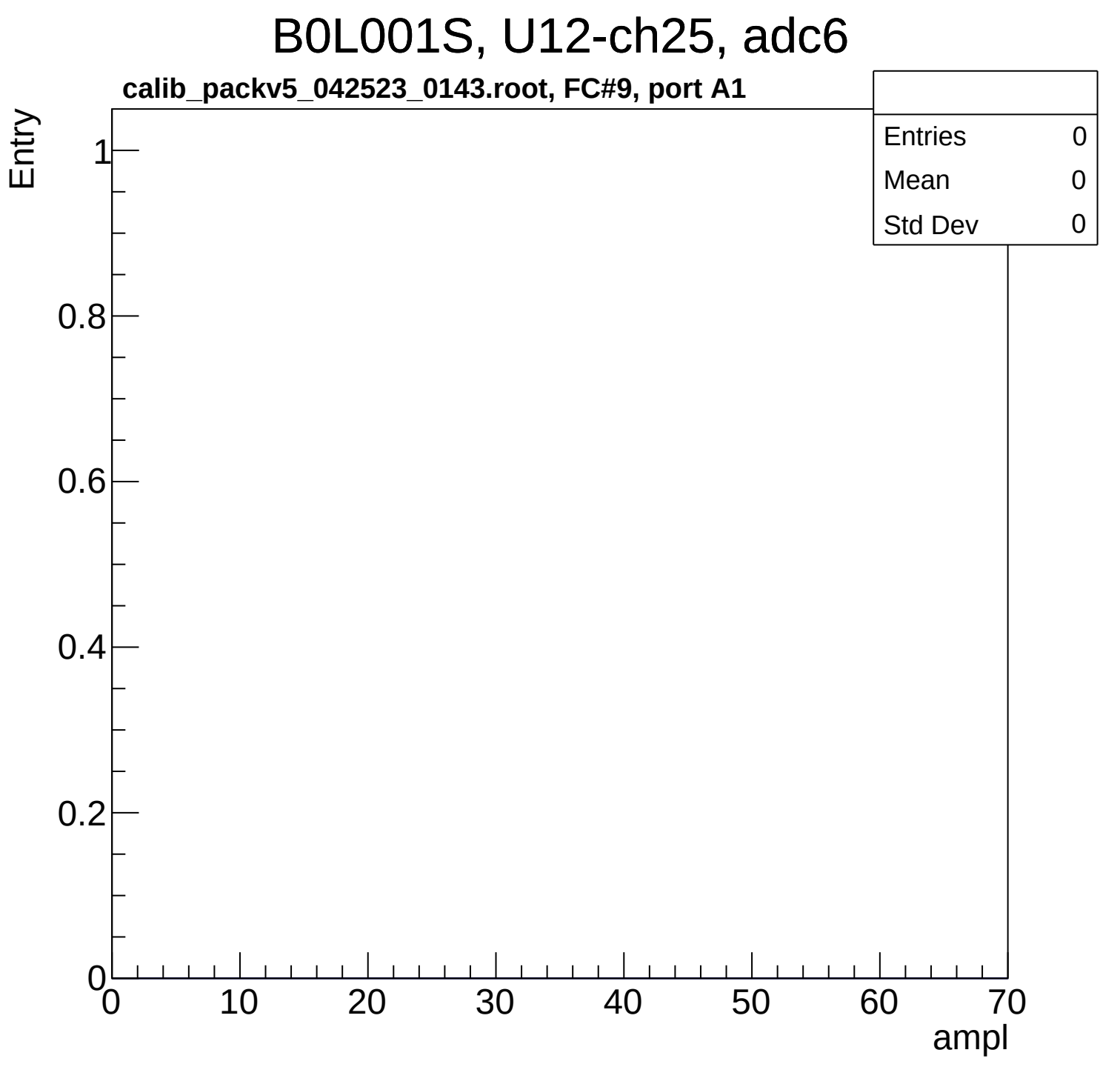

B0L001S, U12-ch25, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 17
Mean 61.41
Std Dev 1.611
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch25, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
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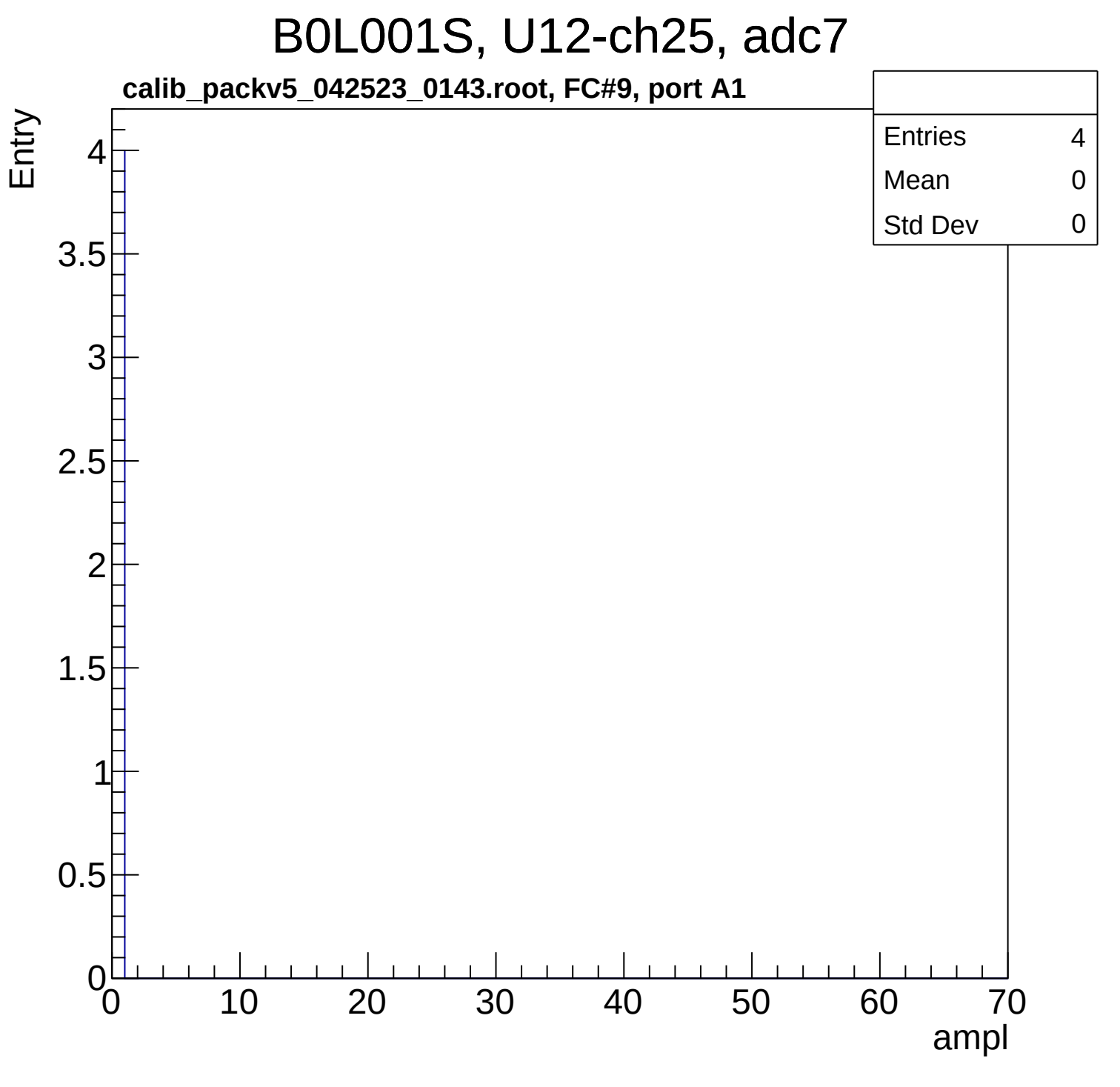
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch25, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 4
Mean 0
Std Dev 0
Entry
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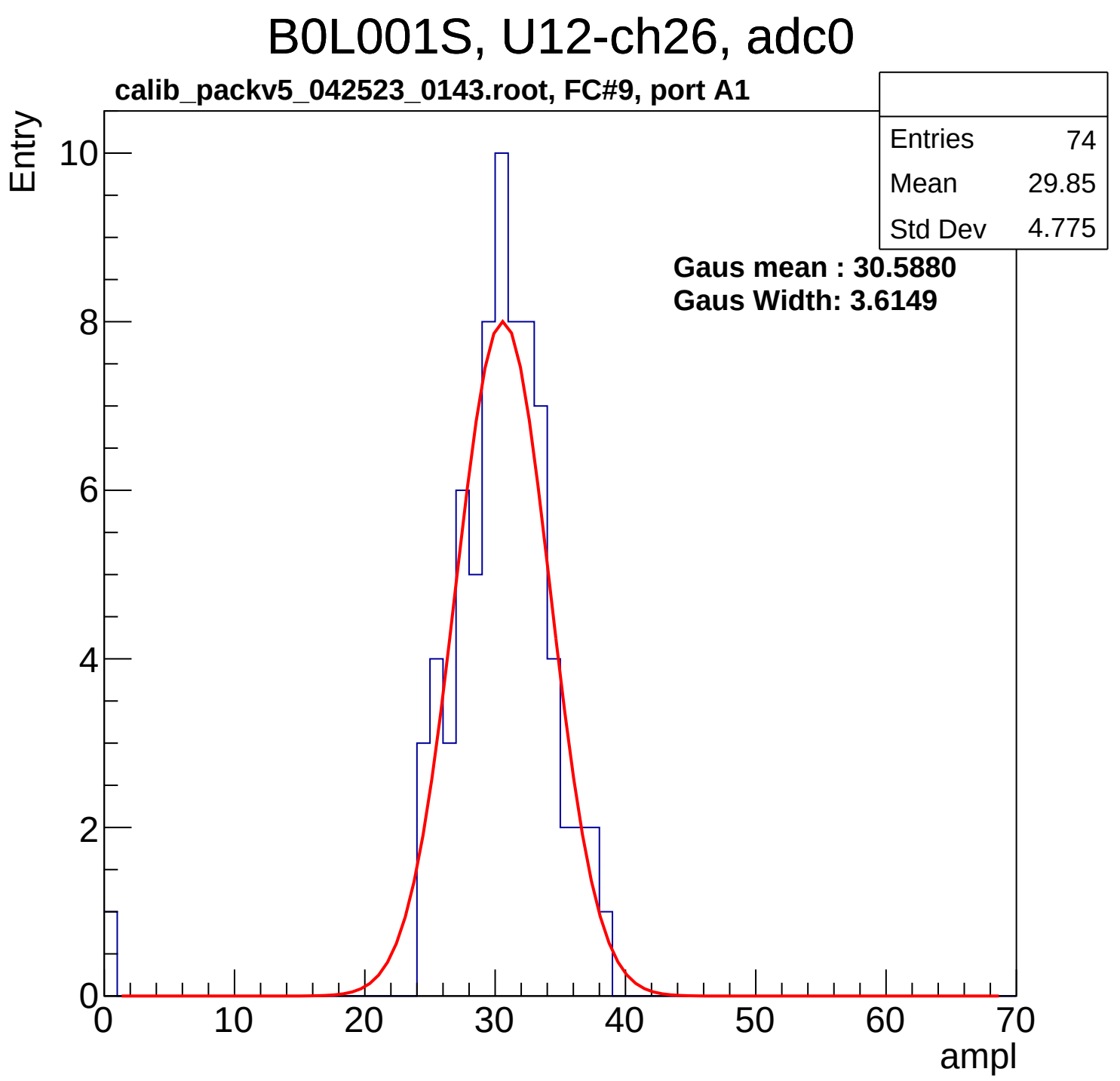
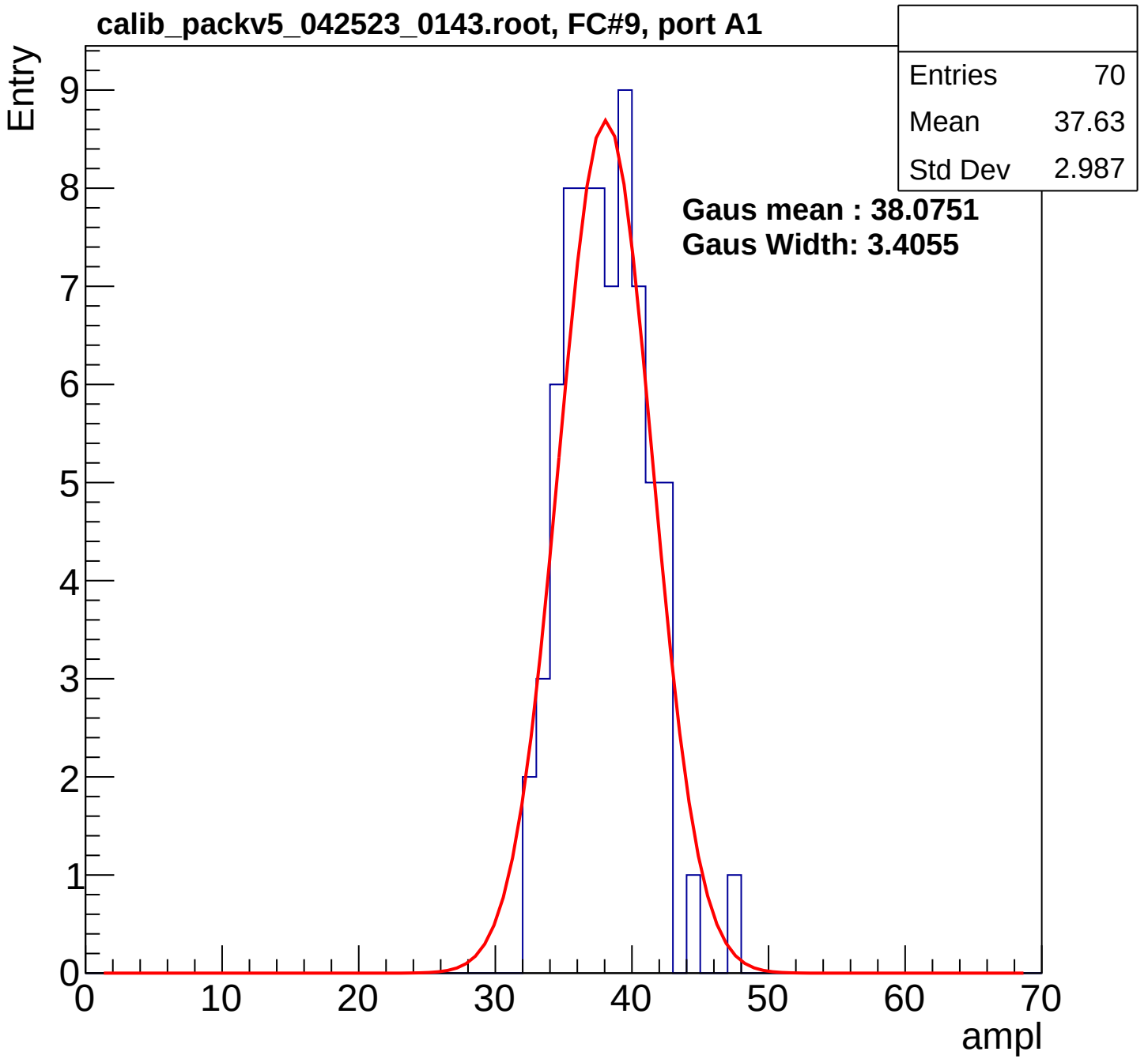
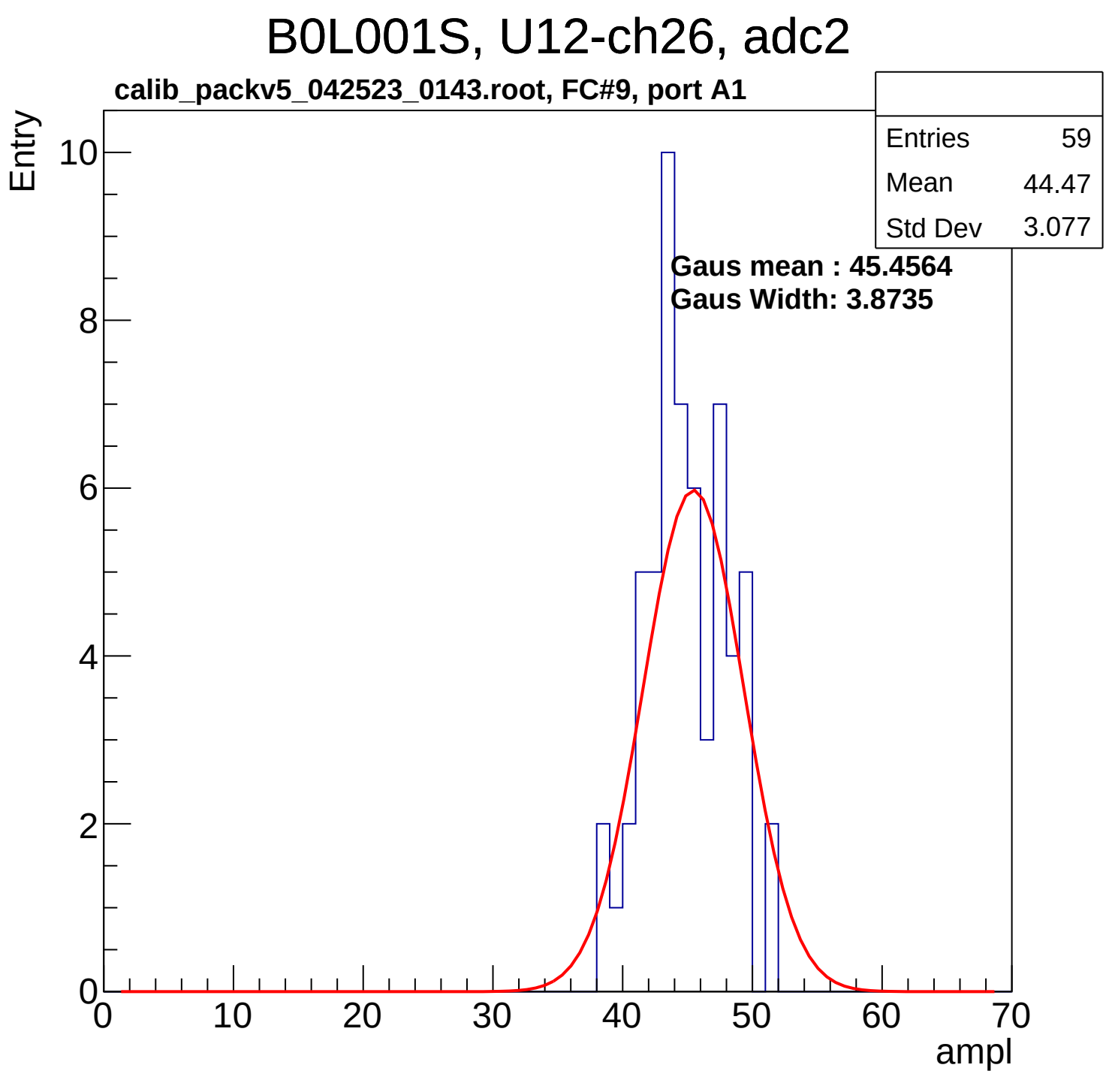
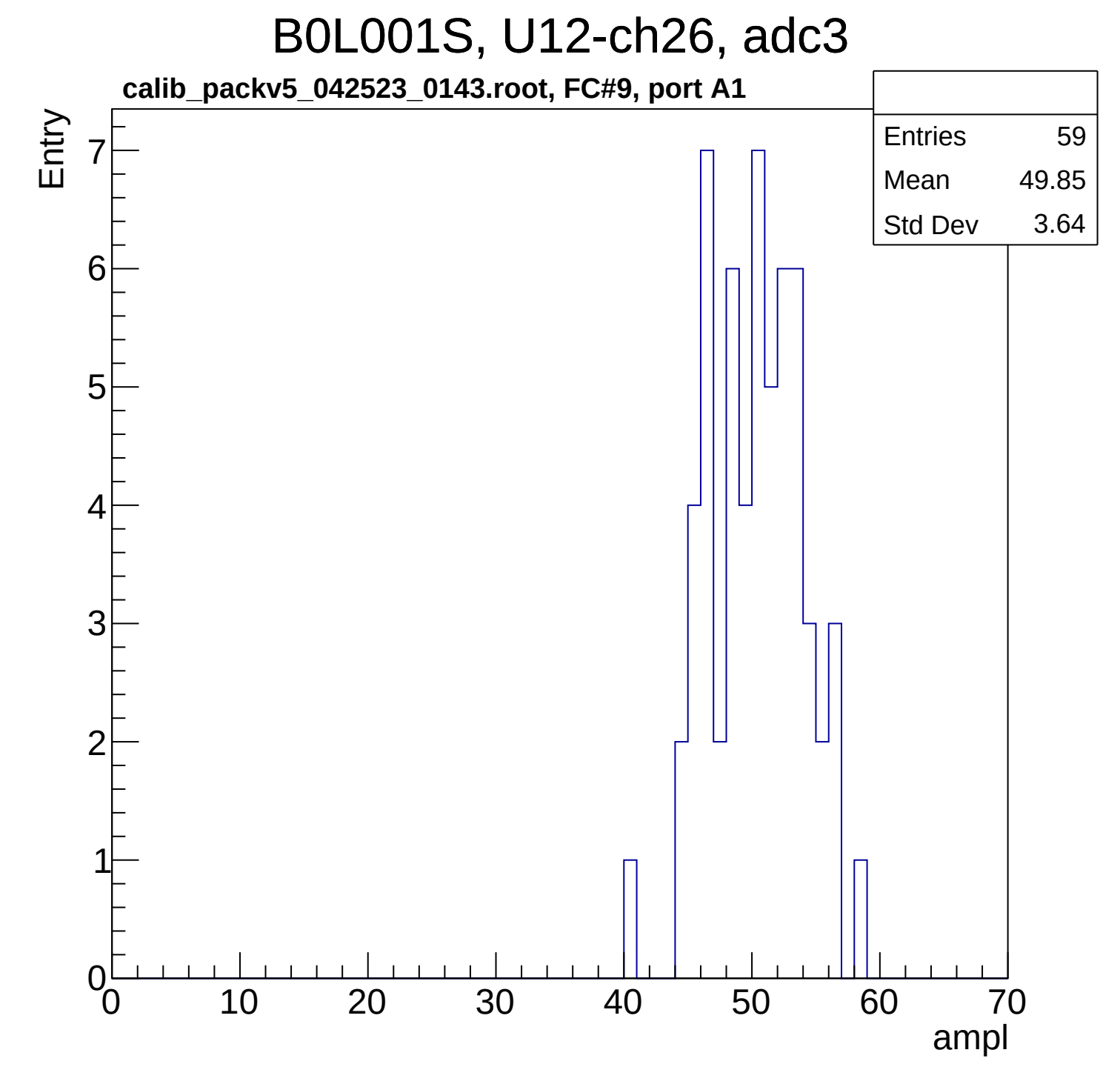
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch26, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 74
Mean 29.85
Std Dev 4.775
Gaus mean : 30.5880
Gaus Width: 3.6149
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch26, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 70
Mean 37.63
Std Dev 2.987
Gaus mean : 38.0751
Gaus Width: 3.4055
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch26, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 59
Mean 44.47
Std Dev 3.077
Gaus mean : 45.4564
Gaus Width: 3.8735
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch26, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 59
Mean 49.85
Std Dev 3.64
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
30
40
50
60
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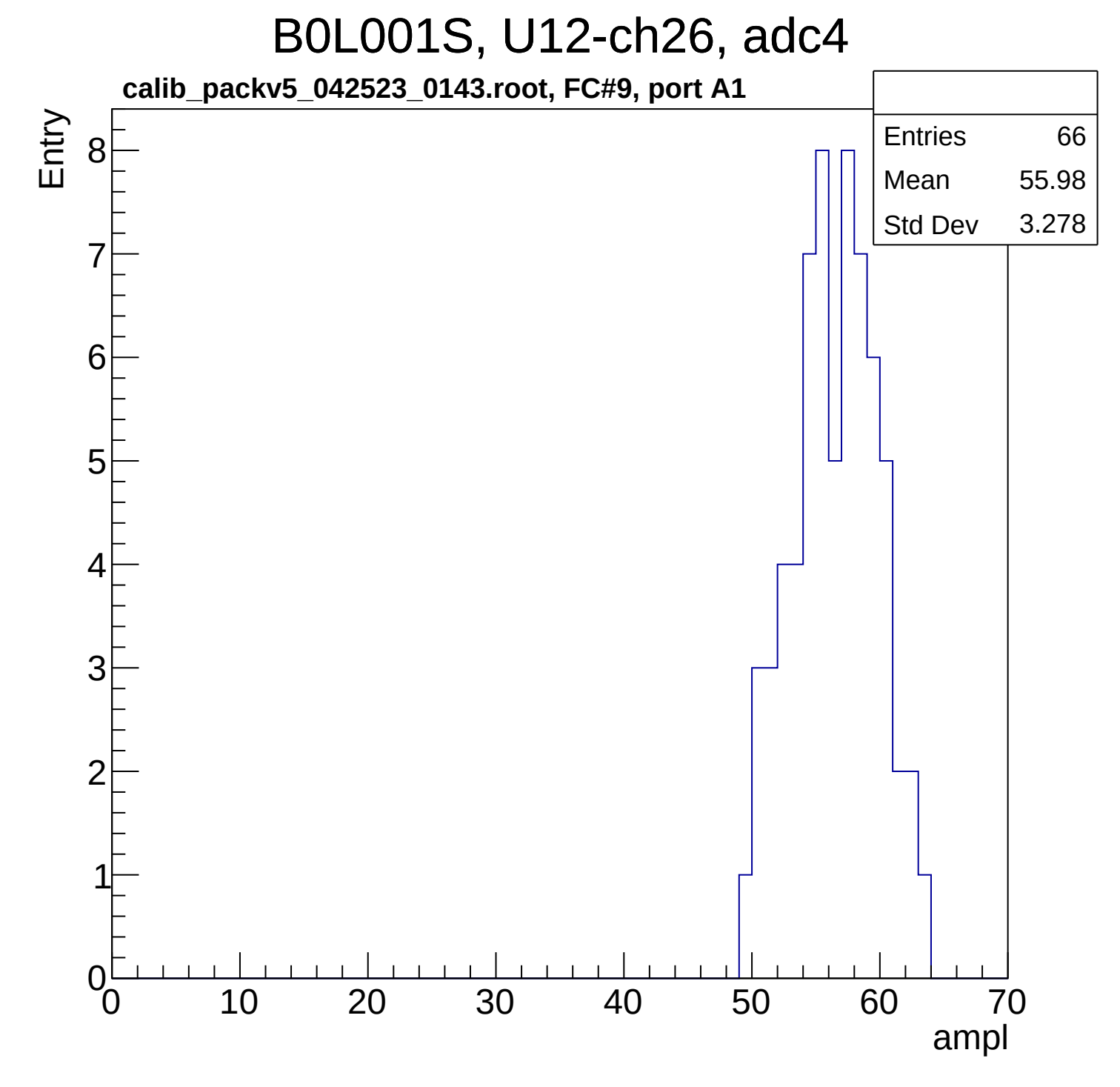
B0L001S, U12-ch26, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 66
Mean 55.98
Std Dev 3.278
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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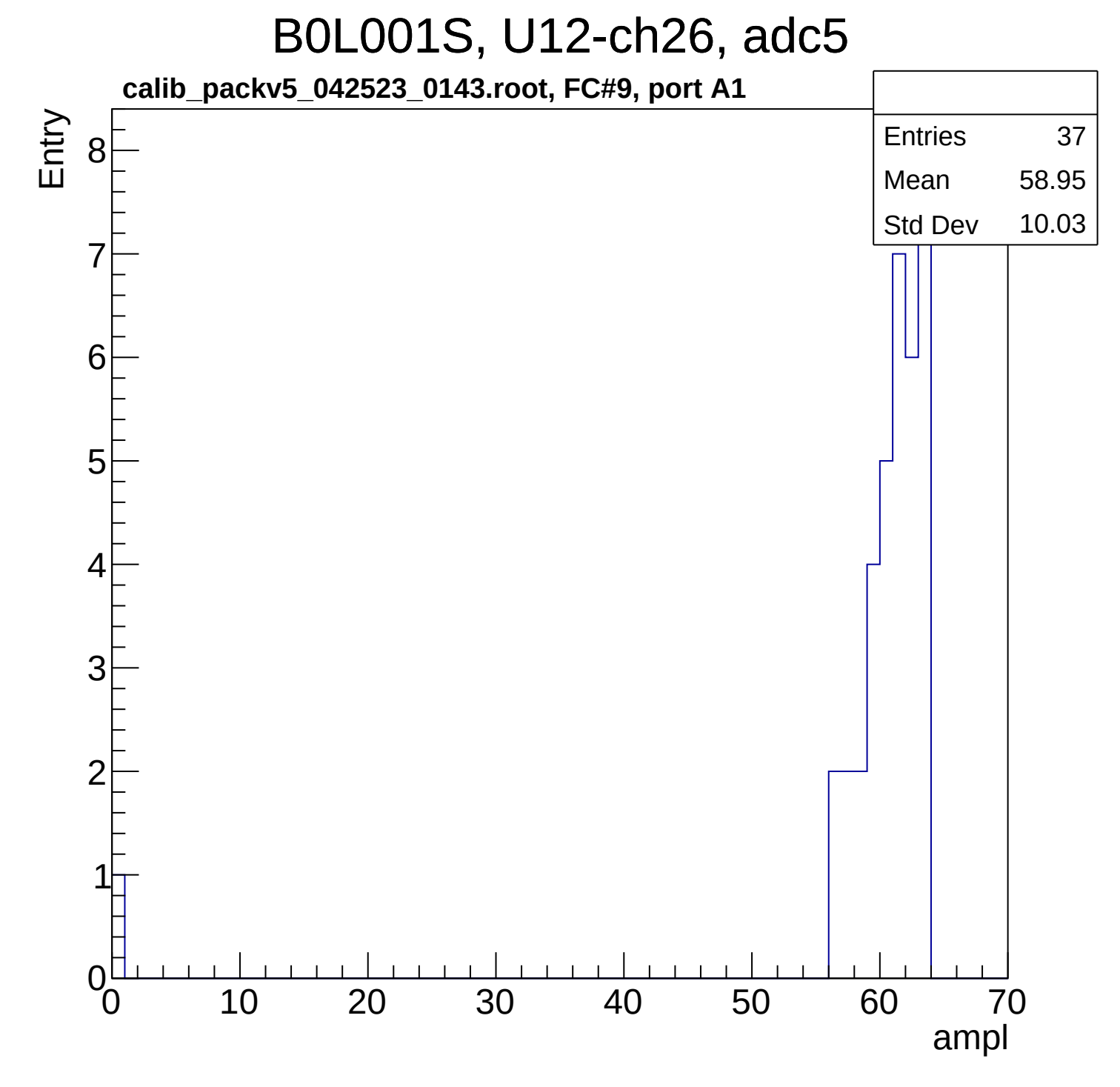
B0L001S, U12-ch26, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 37
Mean 58.95
Std Dev 10.03
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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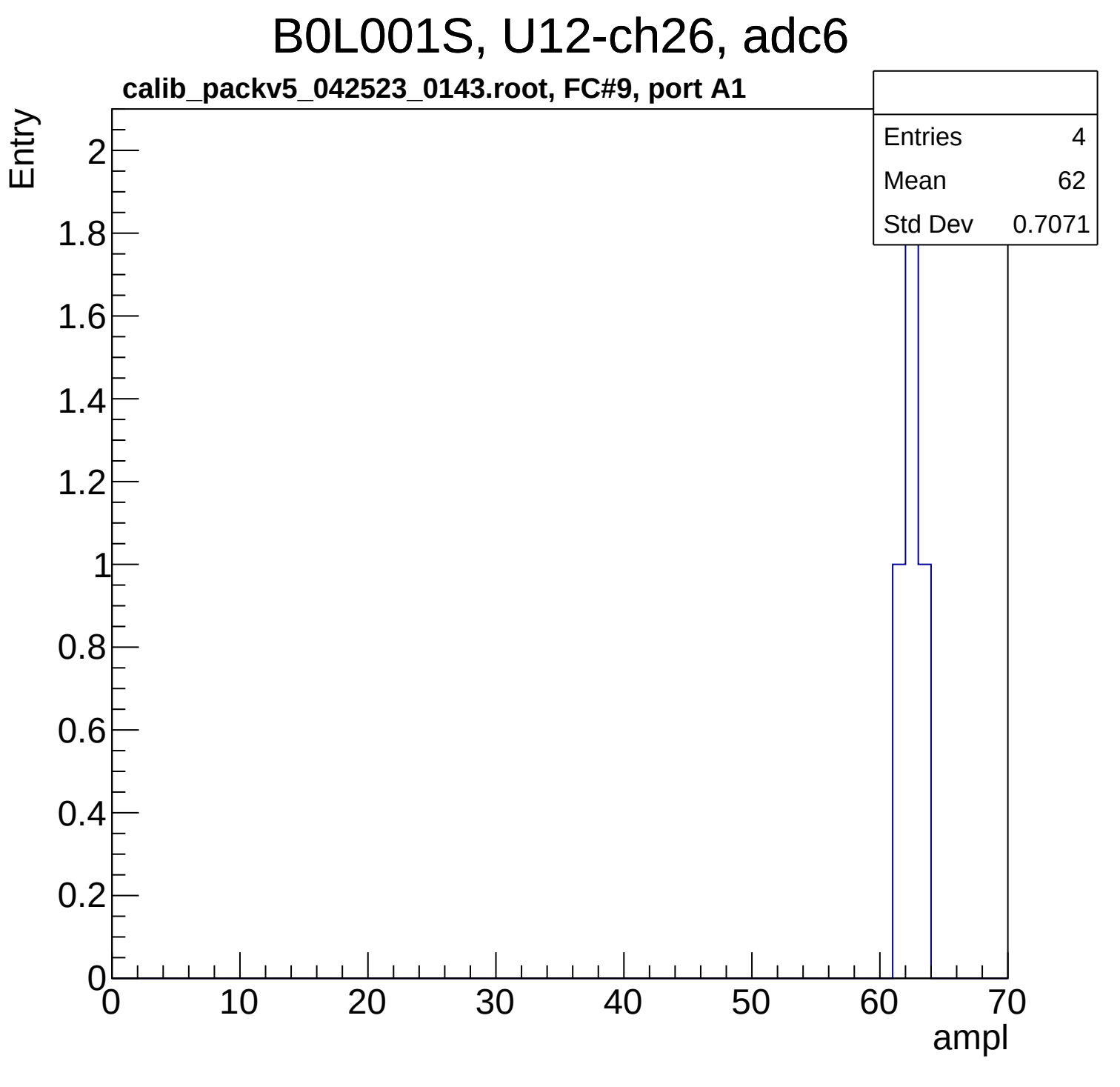
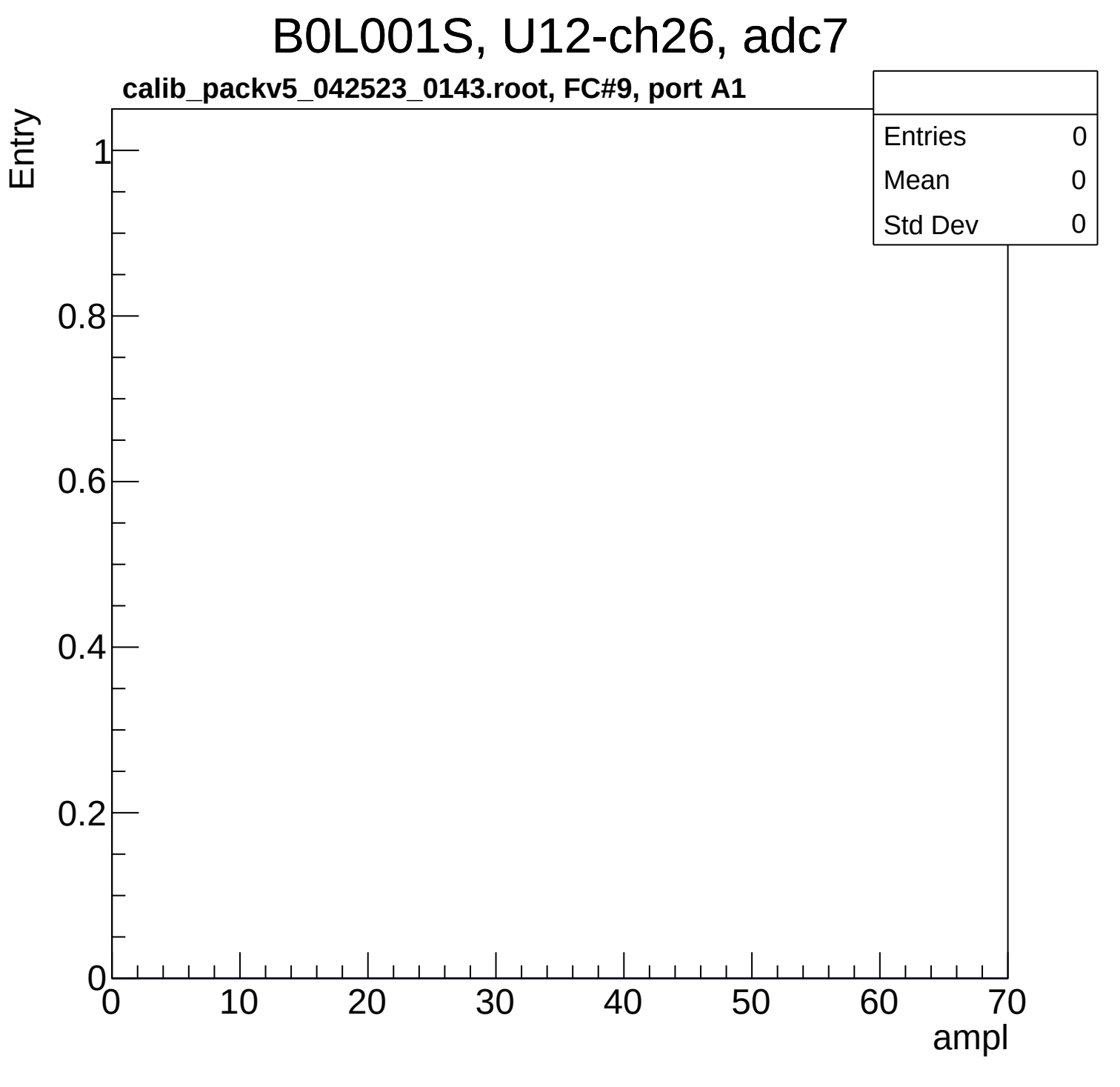

B0L001S, U12-ch26, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 4
Mean 62
Std Dev 0.7071
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L001S, U12-ch26, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
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0.6
0.4
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10
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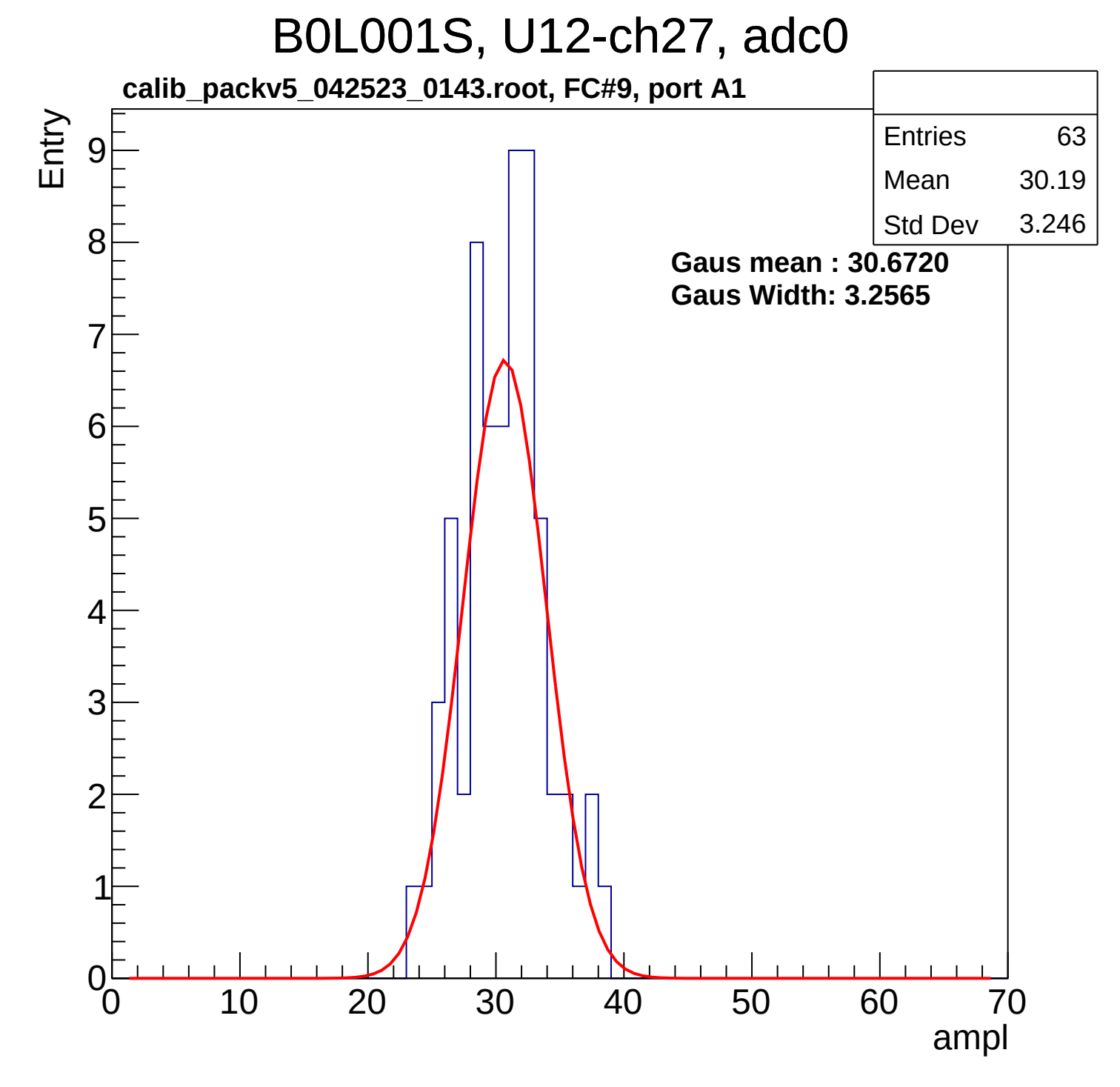
70
ampl


B0L001S, U12-ch27, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 63
Mean 30.19
Std Dev 3.246
Gaus mean : 30.6720
Gaus Width: 3.2565
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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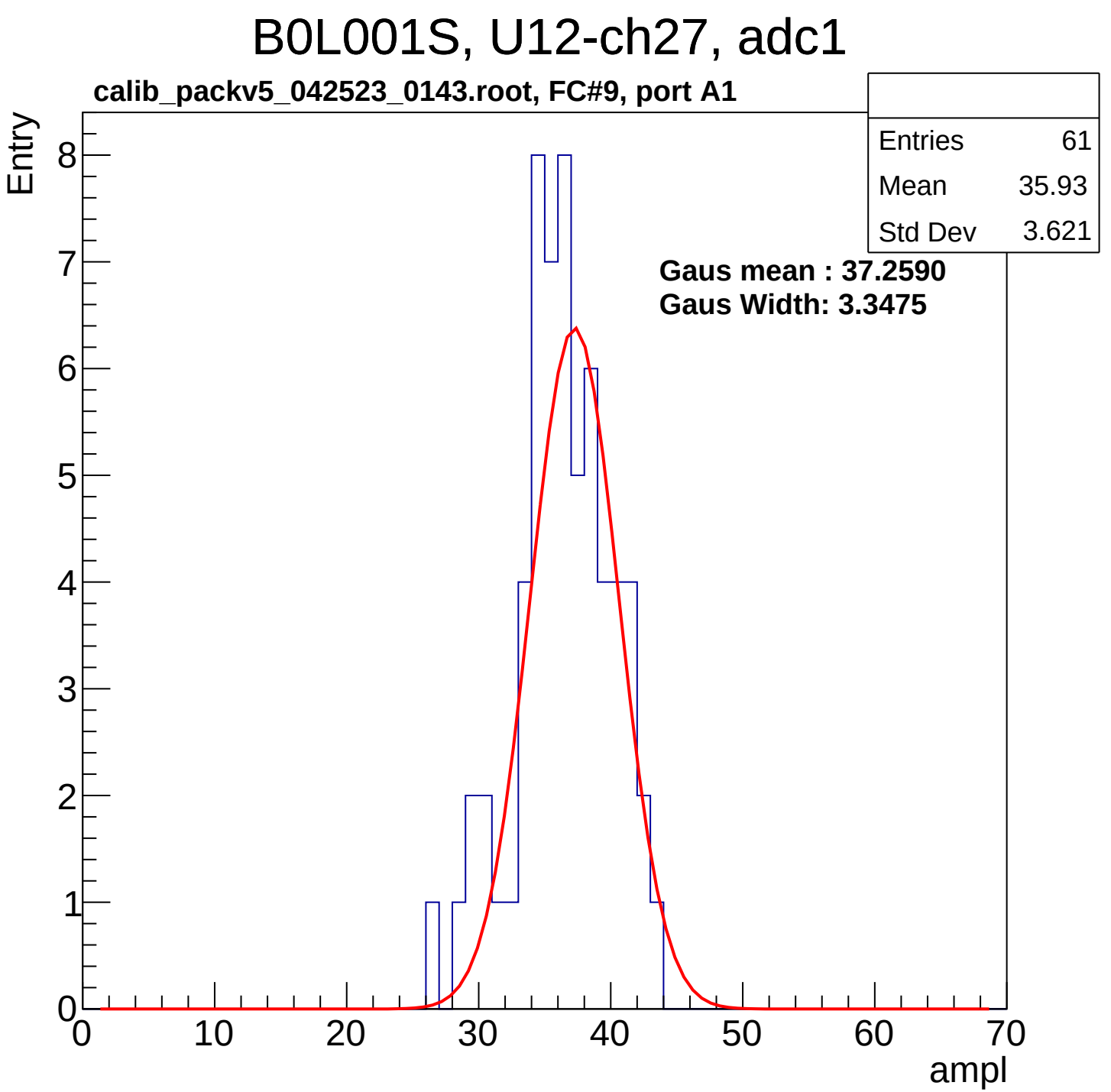
B0L001S, U12-ch27, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 61
Mean 35.93
Std Dev 3.621
Gaus mean : 37.2590
Gaus Width: 3.3475
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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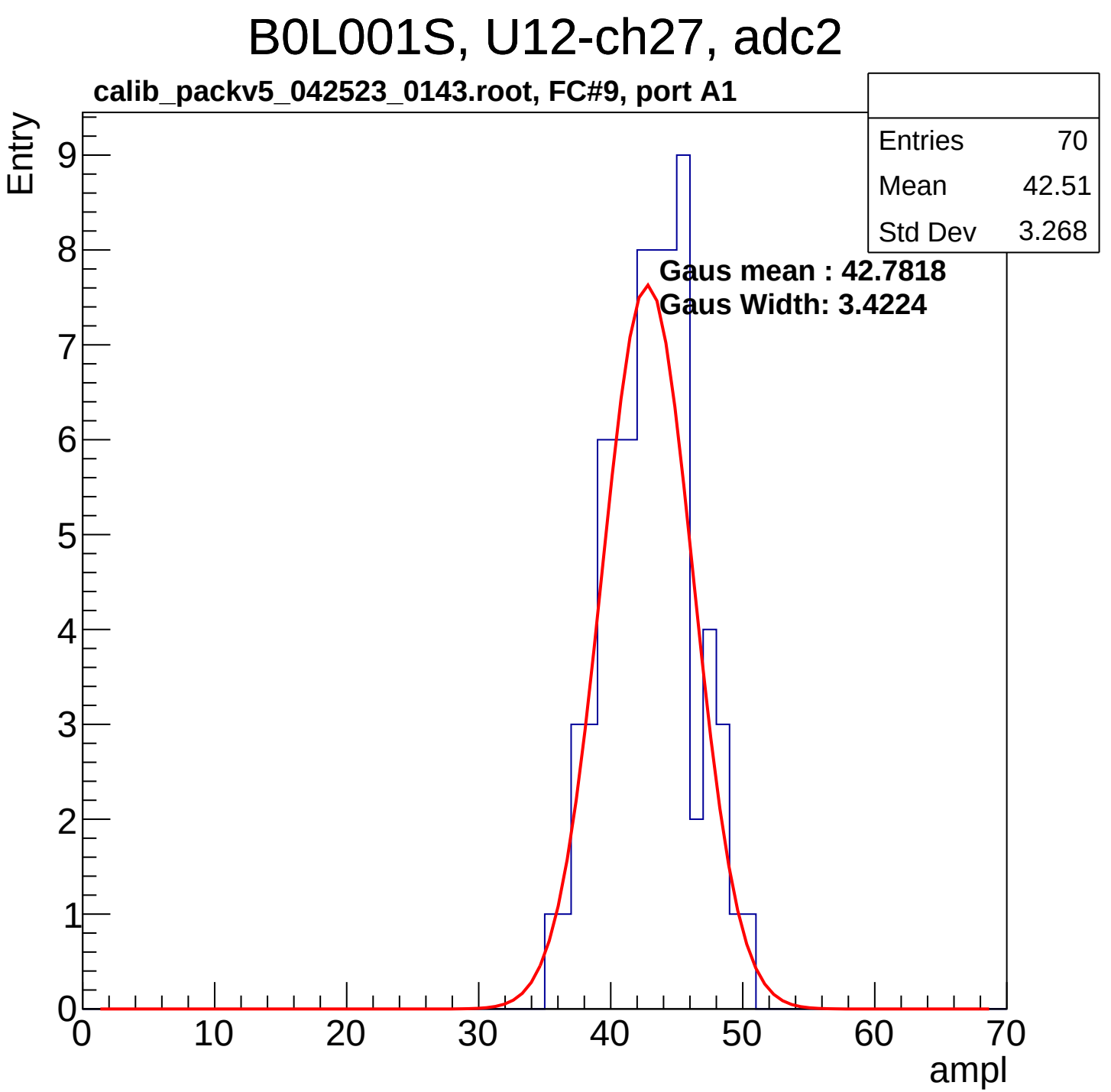
B0L001S, U12-ch27, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 70
Mean 42.51
Std Dev 3.268
Gaus mean : 42.7818
Gaus Width: 3.4224
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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40
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60
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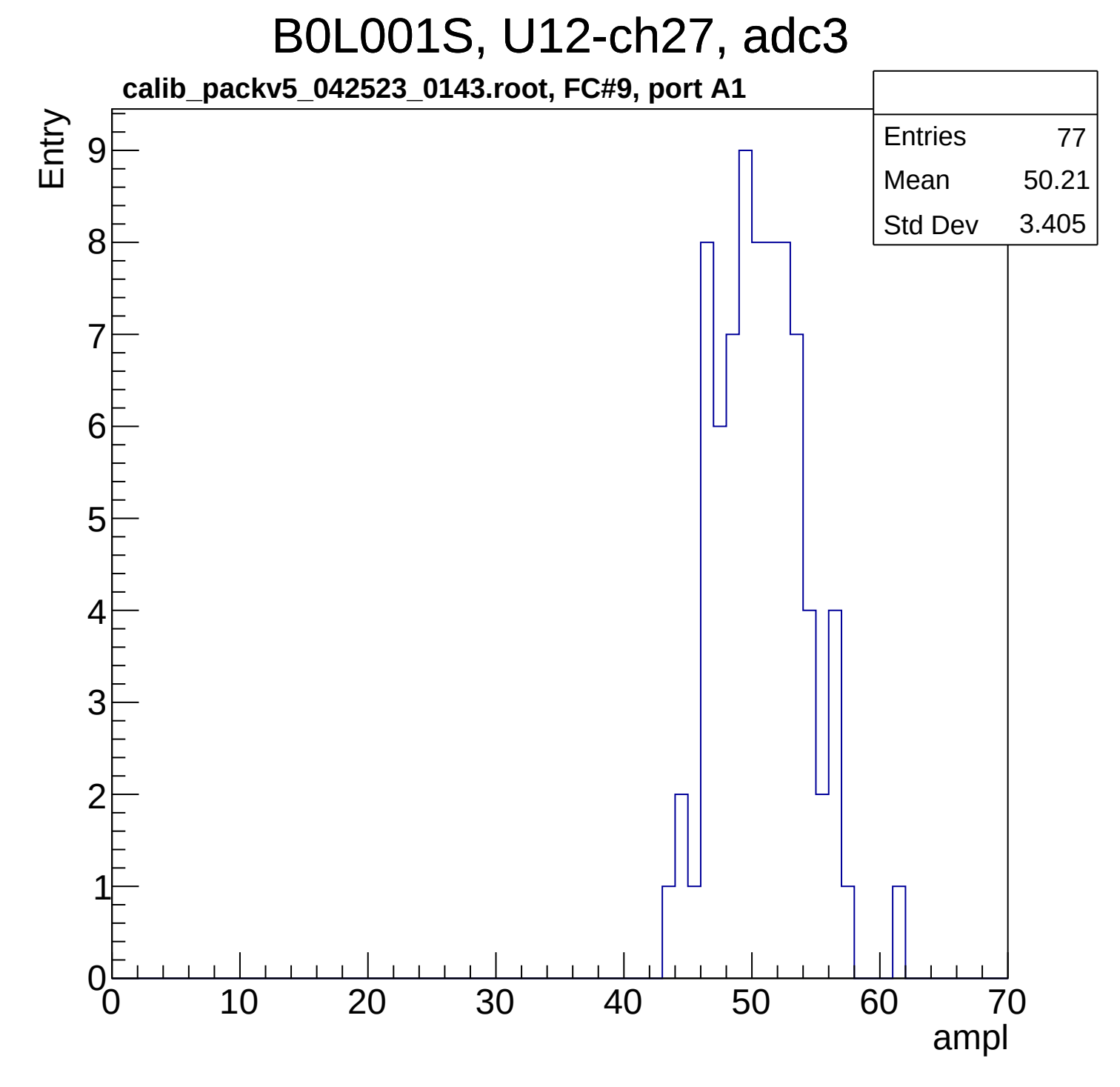
B0L001S, U12-ch27, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 77
Mean 50.21
Std Dev 3.405
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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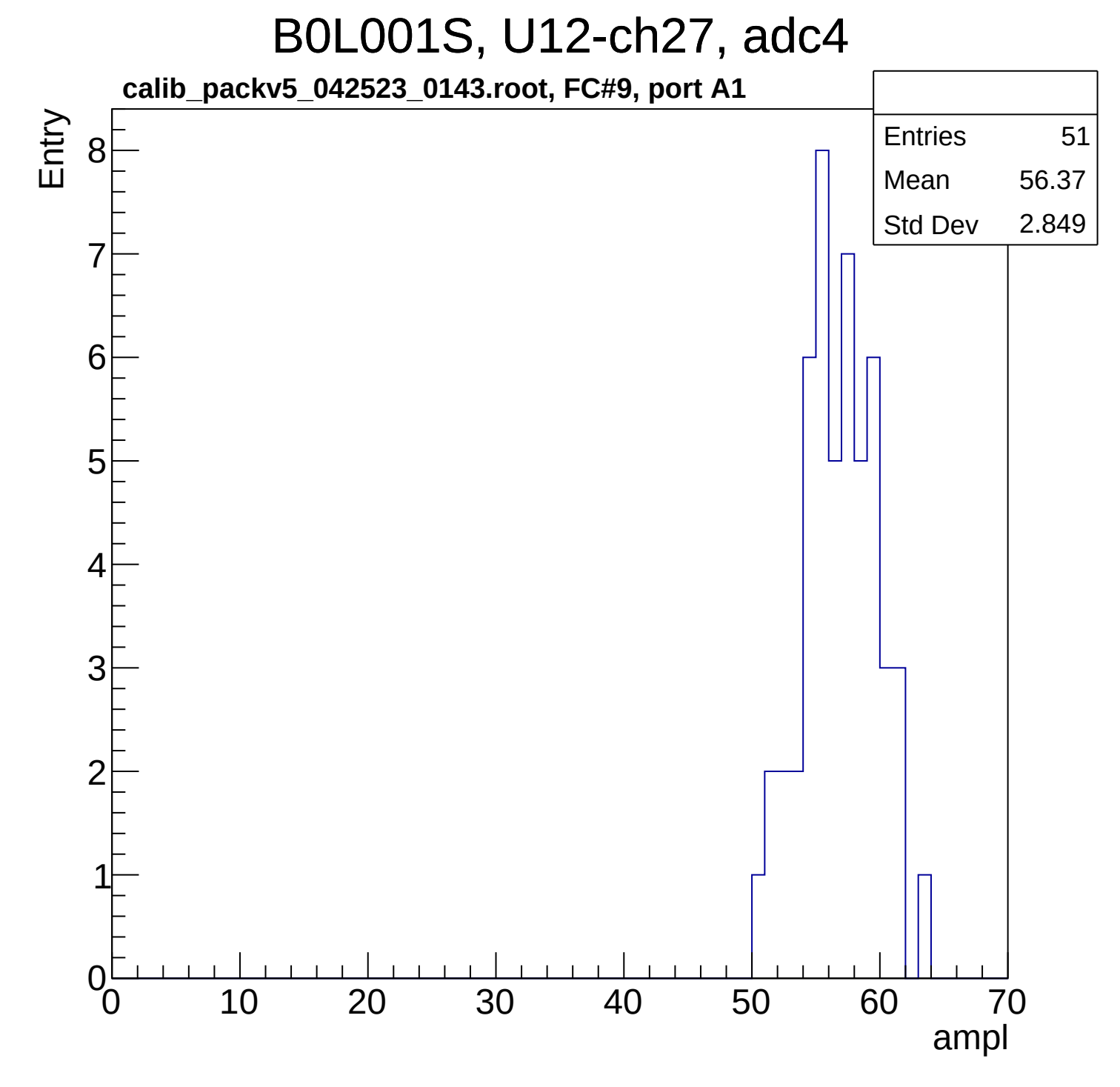
B0L001S, U12-ch27, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 51
Mean 56.37
Std Dev 2.849
Entry
ampl
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1
2
3
4
5
6
7
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0
10
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40
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60
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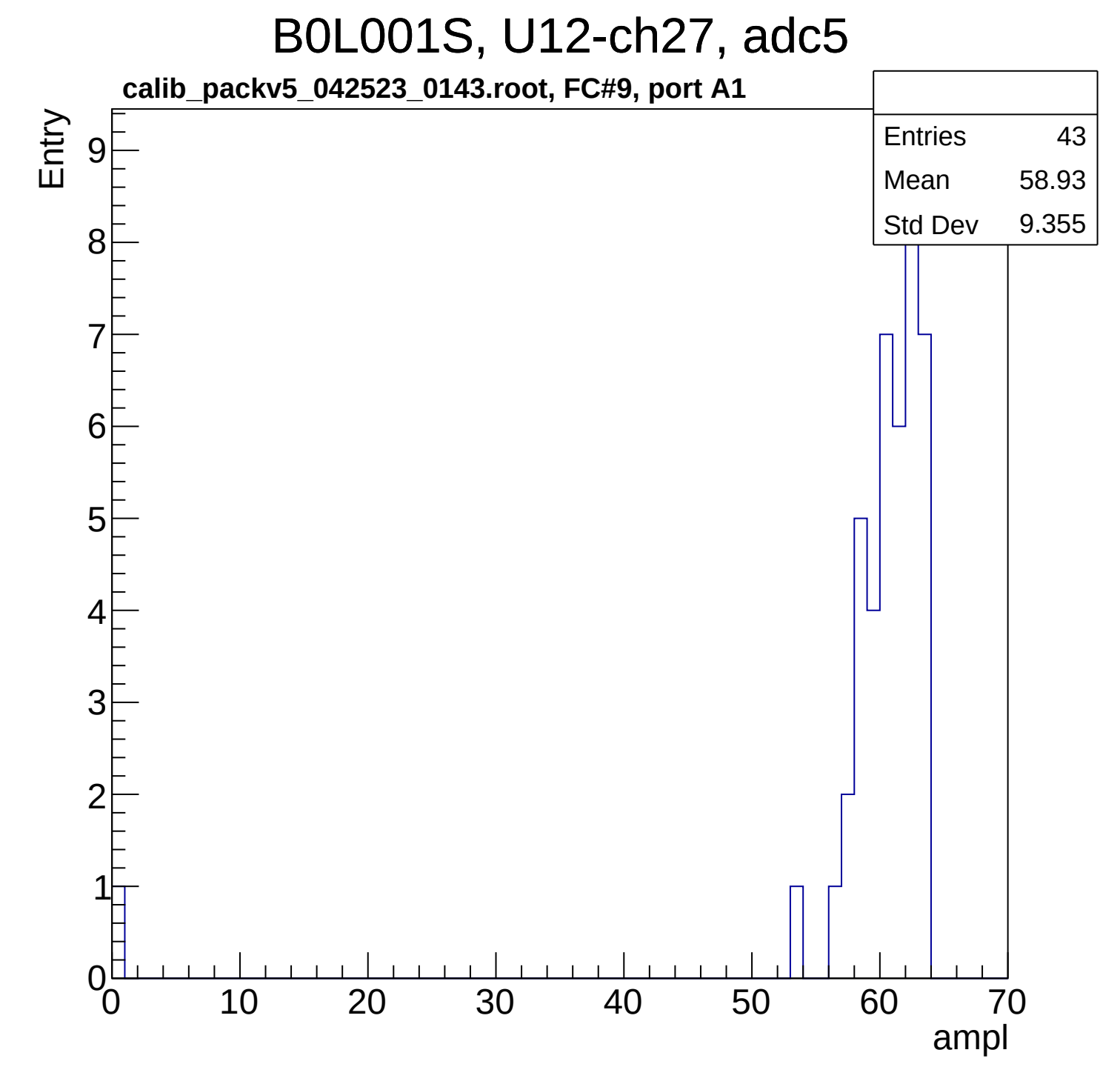
B0L001S, U12-ch27, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 43
Mean 58.93
Std Dev 9.355
Entry
ampl
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6
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0
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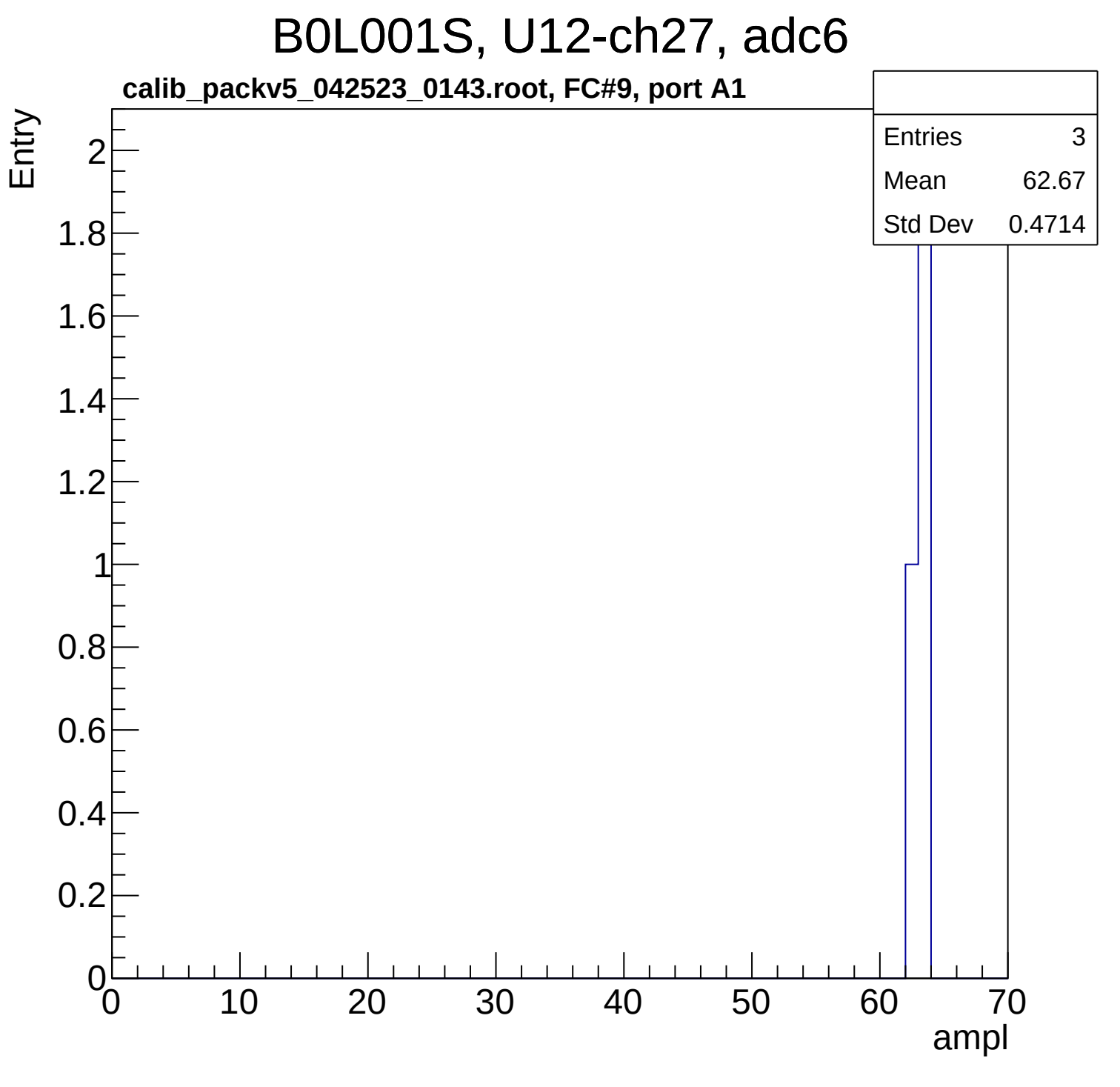
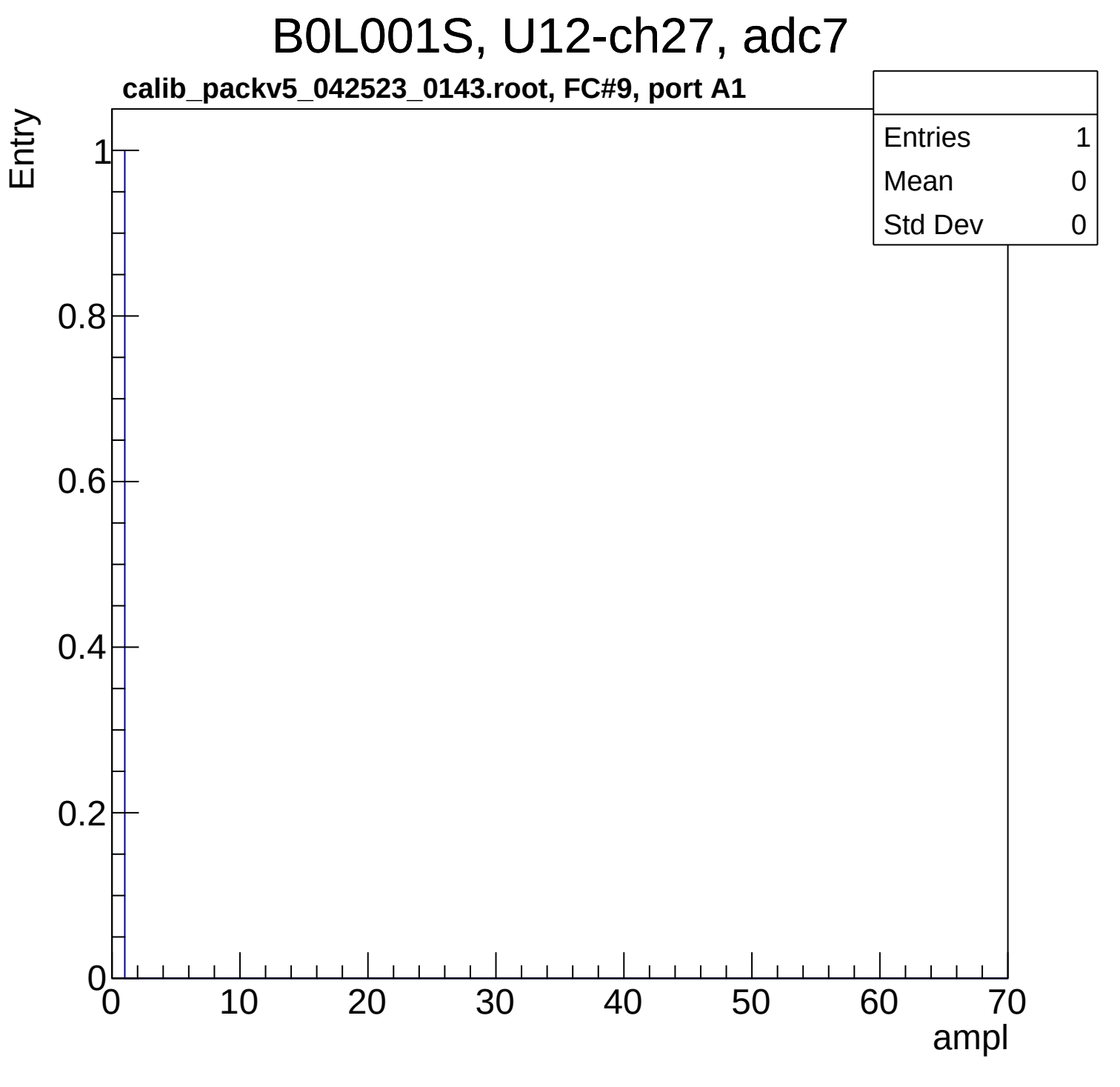

B0L001S, U12-ch27, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L001S, U12-ch27, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 0
Std Dev 0
Entry
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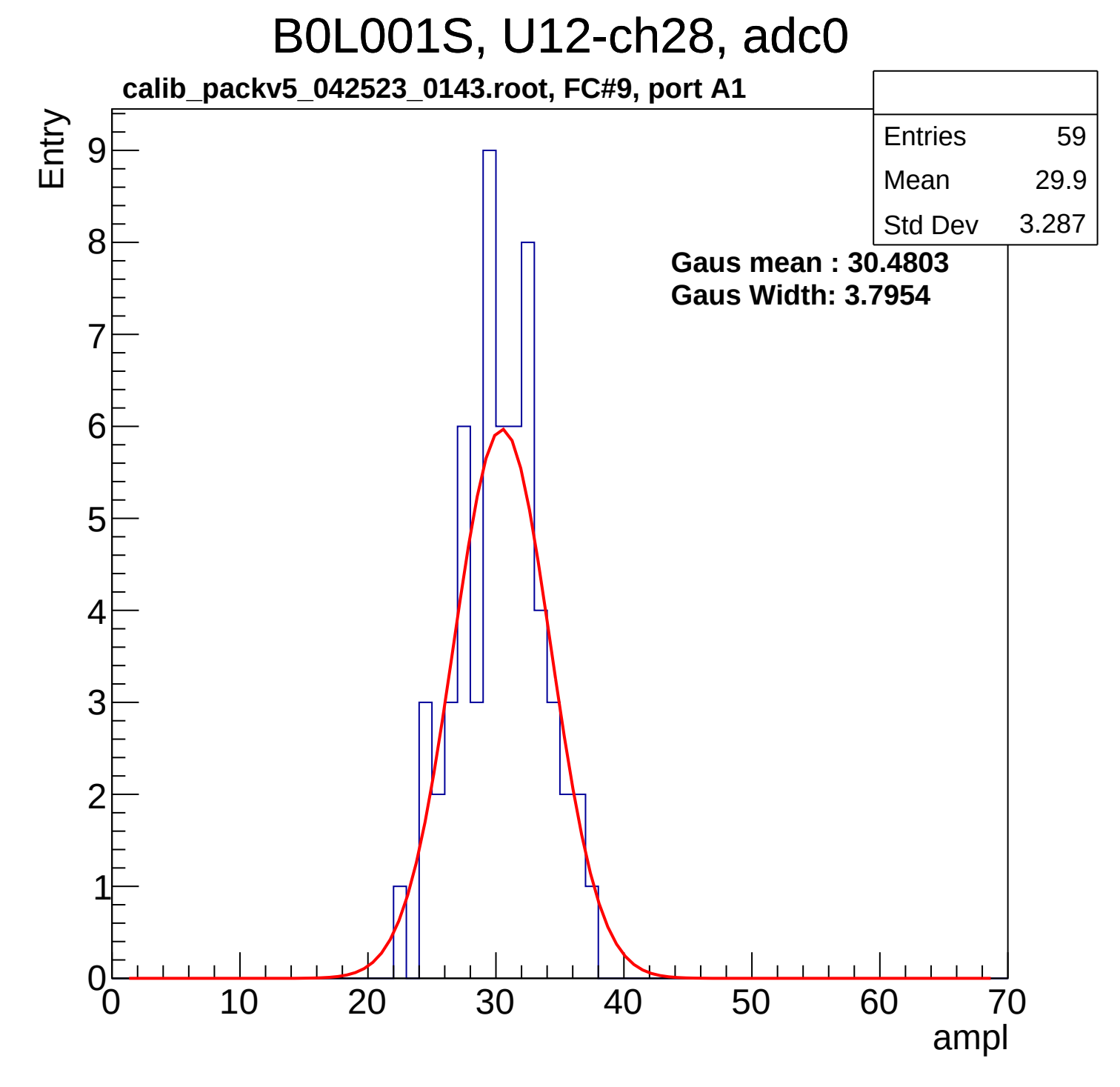
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch28, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 59
Mean 29.9
Std Dev 3.287
Gaus mean : 30.4803
Gaus Width: 3.7954
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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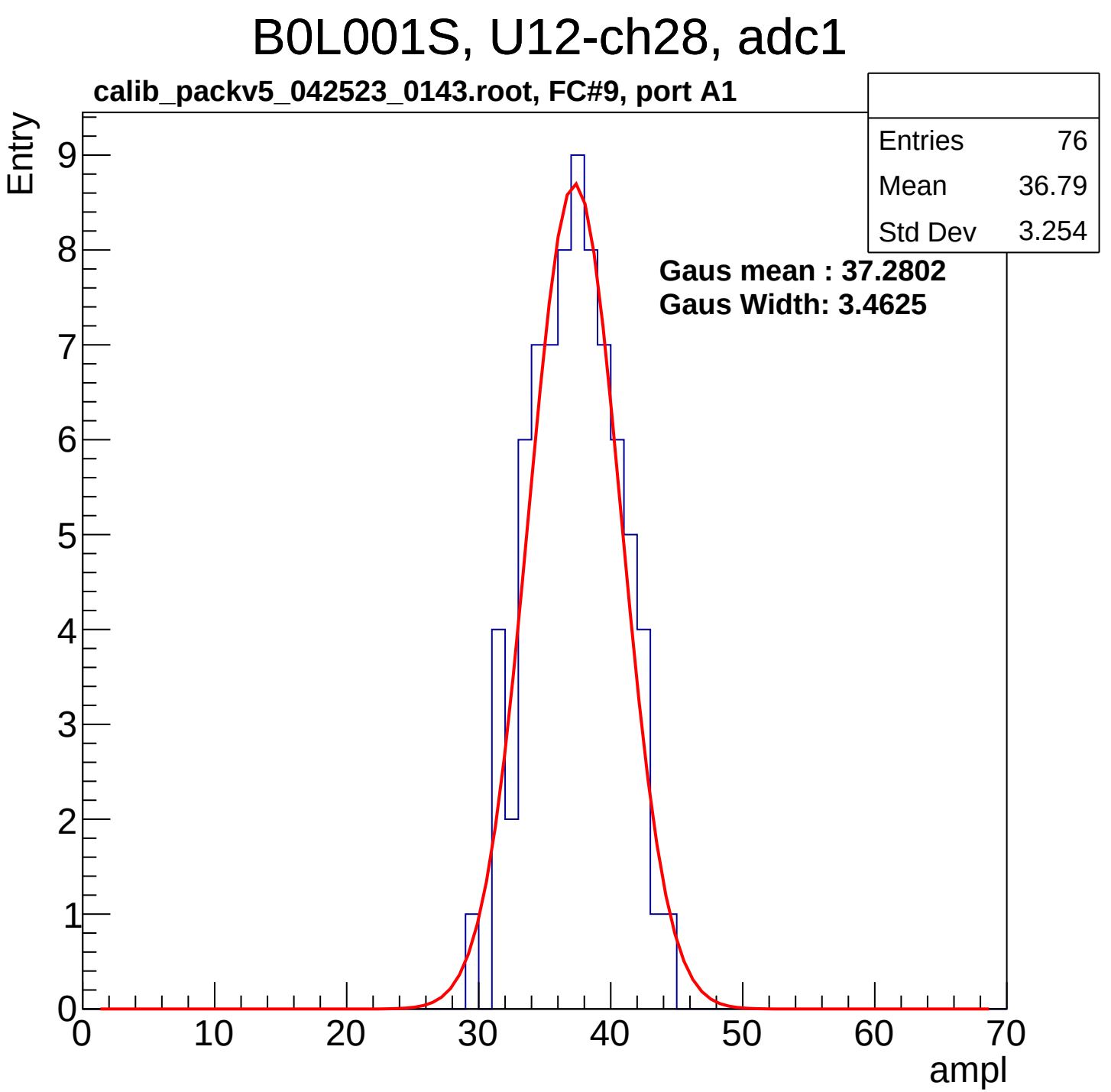
B0L001S, U12-ch28, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 76
Mean 36.79
Std Dev 3.254
Gaus mean : 37.2802
Gaus Width: 3.4625
Entry
ampl
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2
3
4
5
6
7
8
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0
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20
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40
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60
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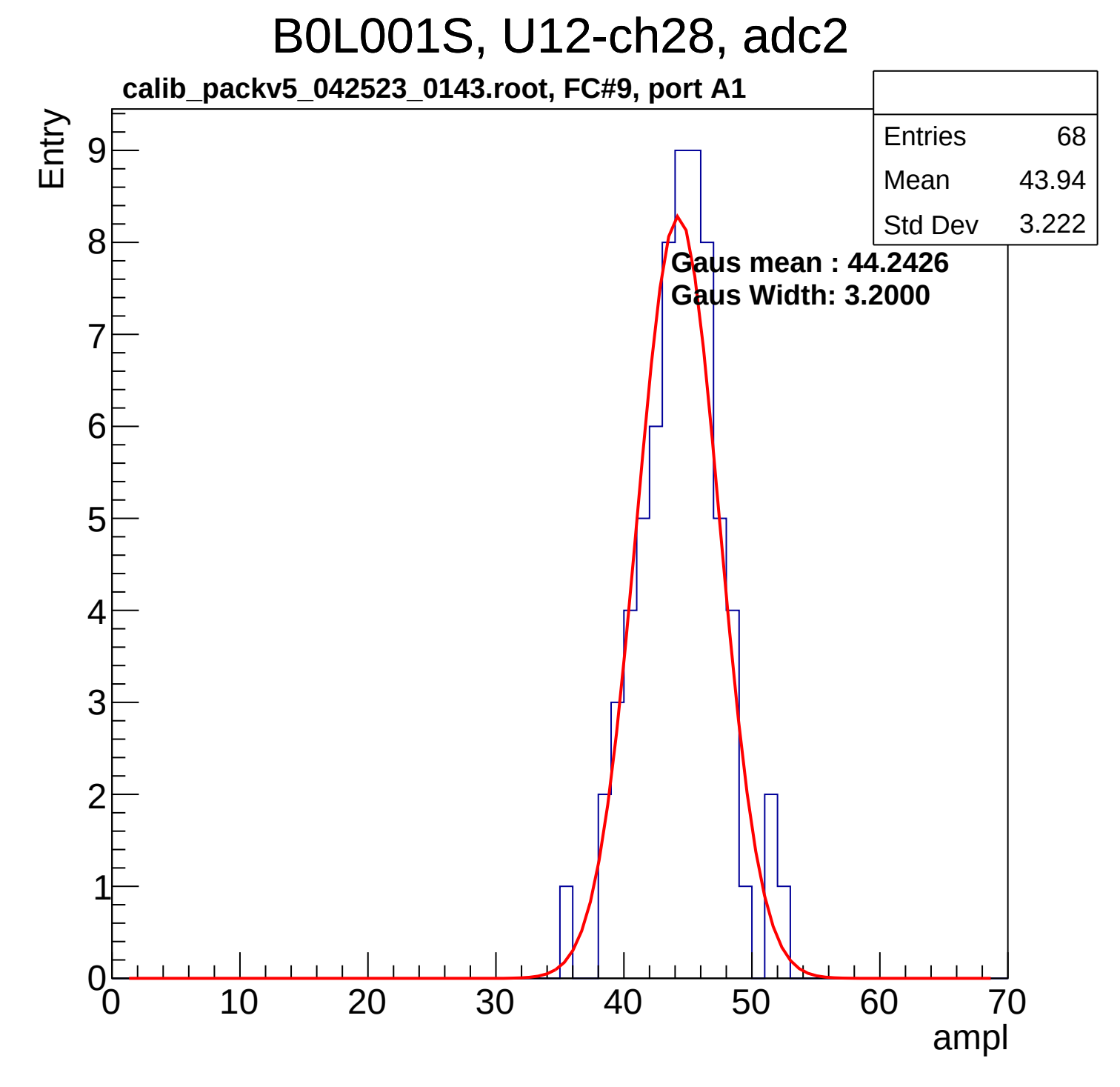
B0L001S, U12-ch28, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 68
Mean 43.94
Std Dev 3.222
Gaus mean : 44.2426
Gaus Width: 3.2000
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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60
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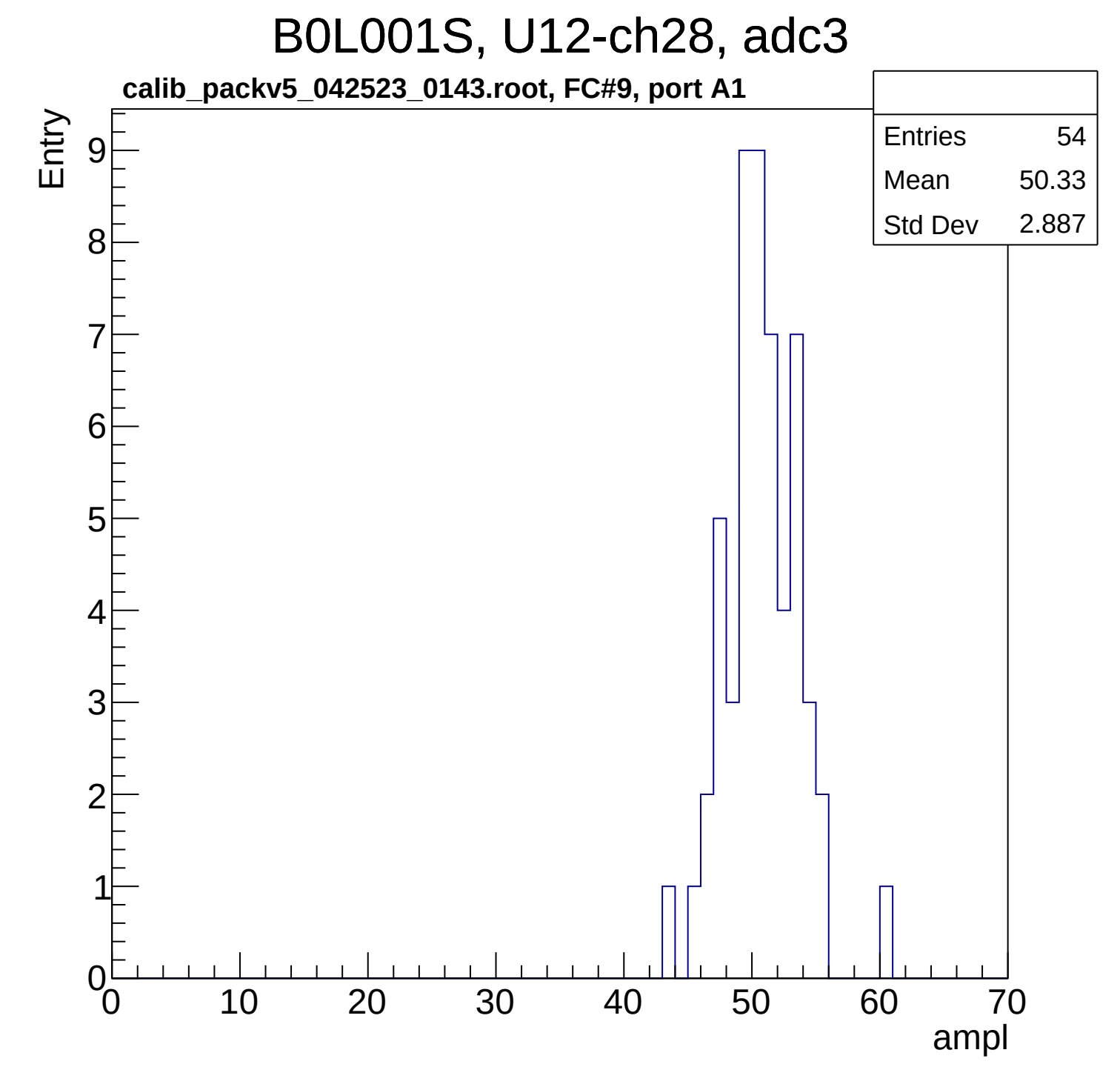
B0L001S, U12-ch28, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 54
Mean 50.33
Std Dev 2.887
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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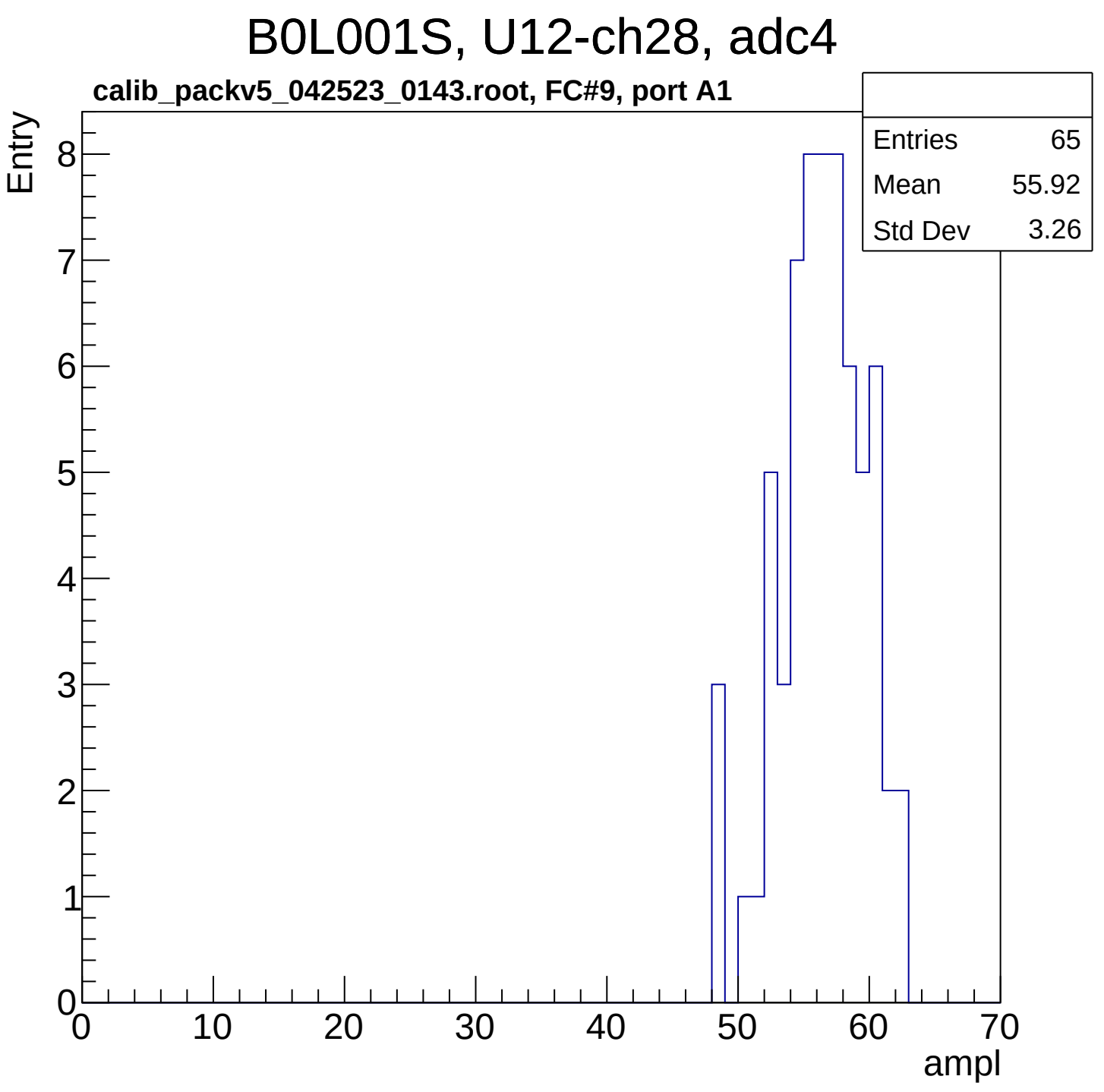
B0L001S, U12-ch28, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 65
Mean 55.92
Std Dev 3.26
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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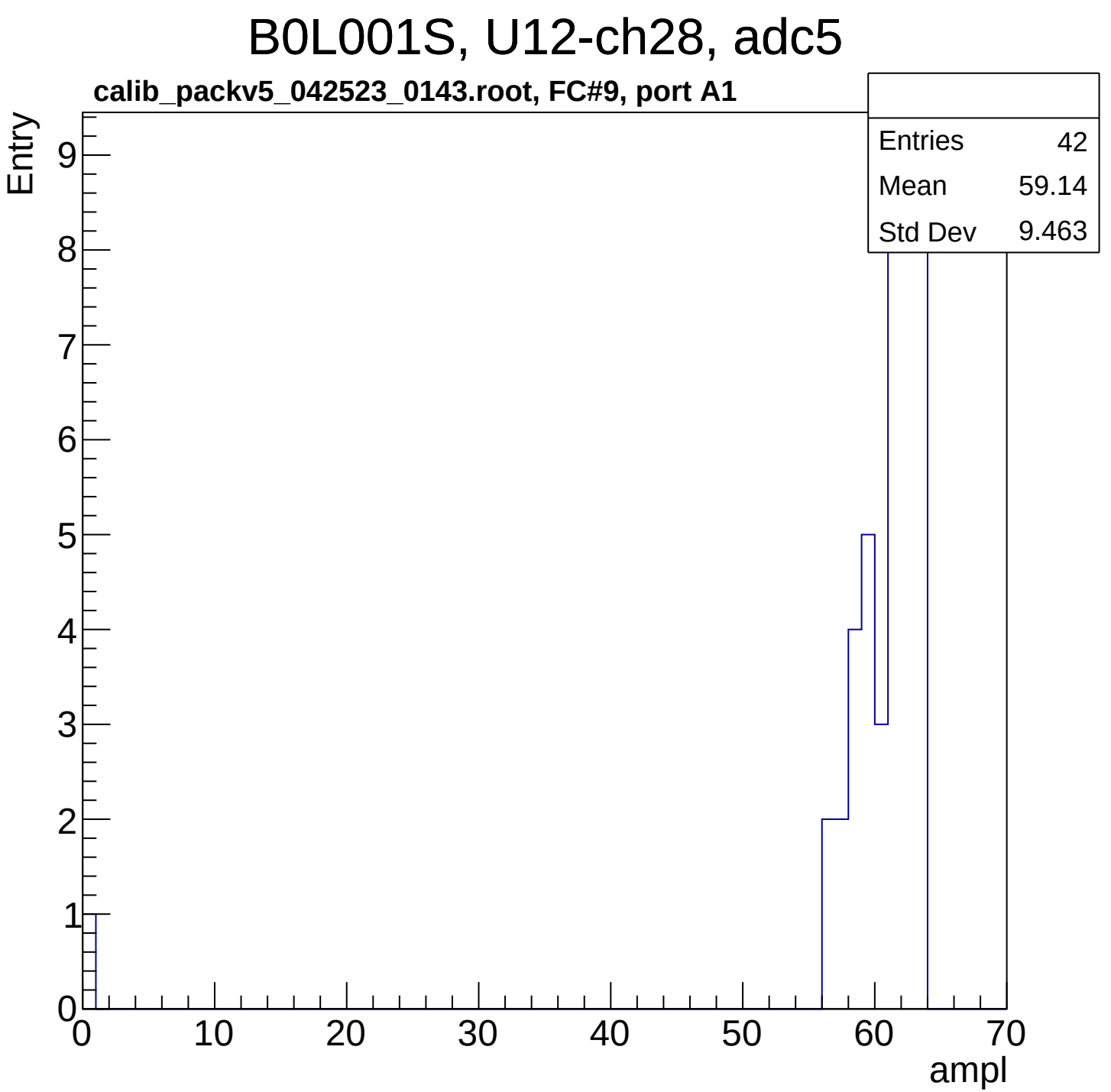
B0L001S, U12-ch28, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 42
Mean 59.14
Std Dev 9.463
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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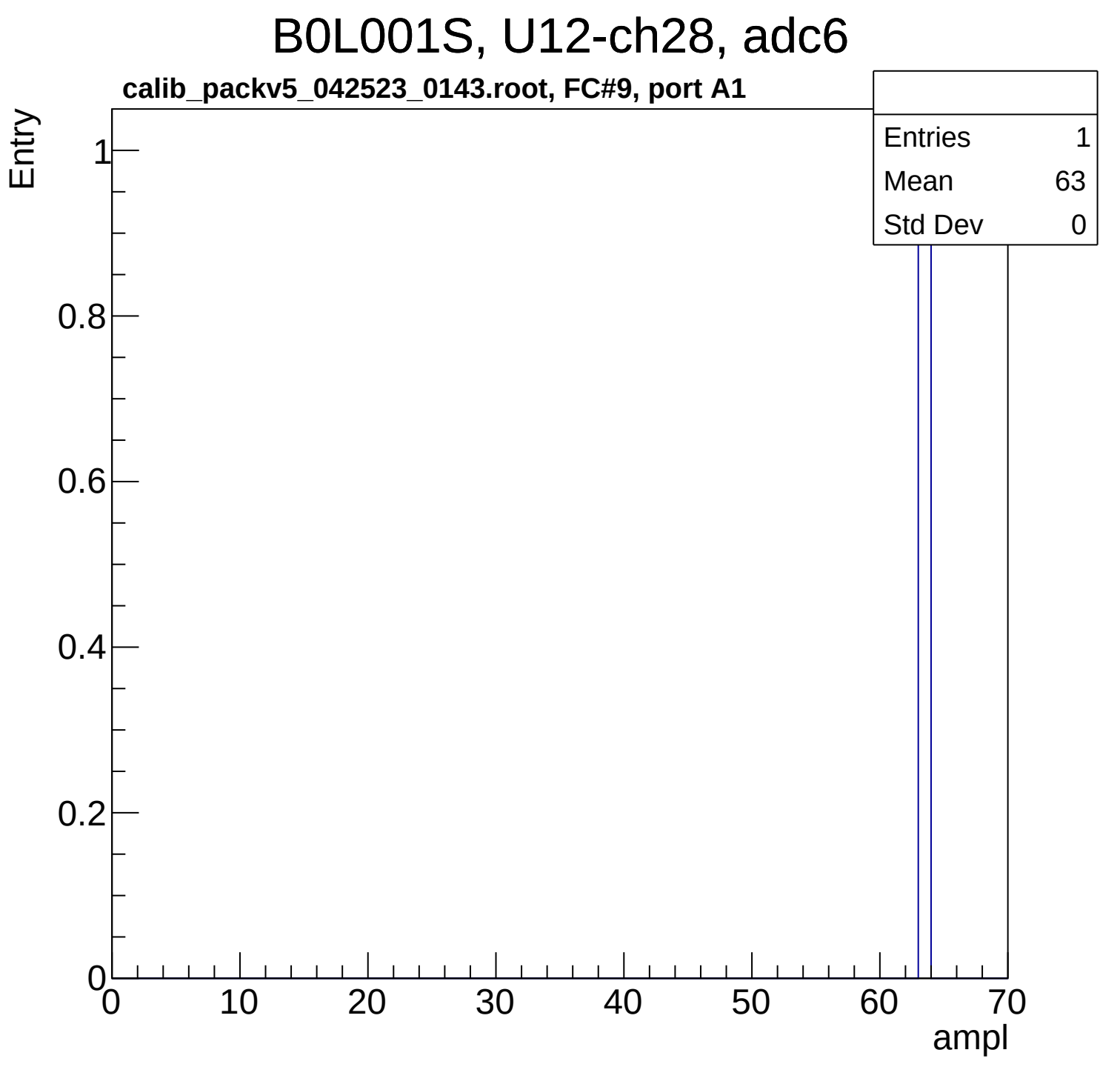
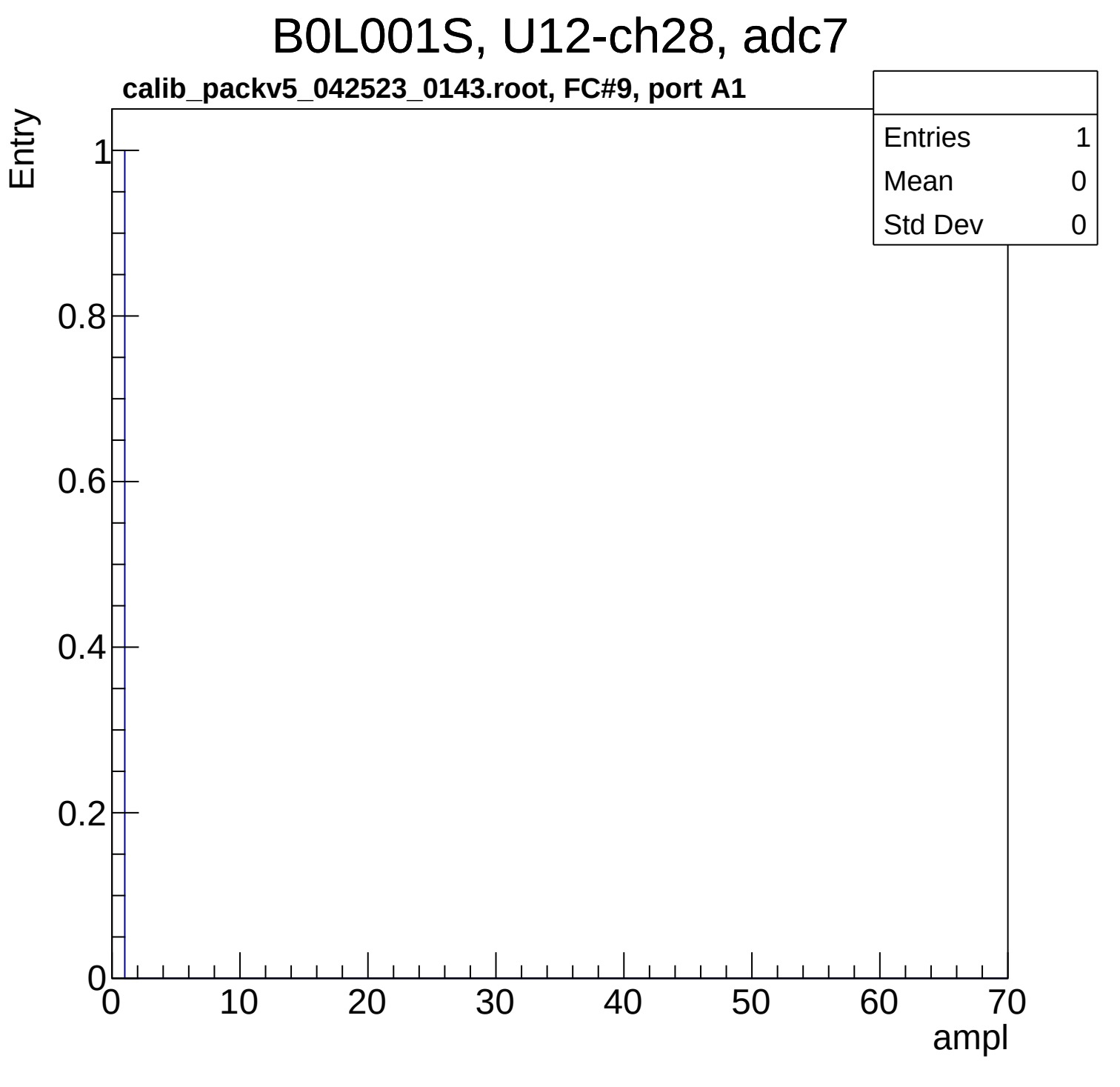

B0L001S, U12-ch28, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch28, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 0
Std Dev 0
Entry
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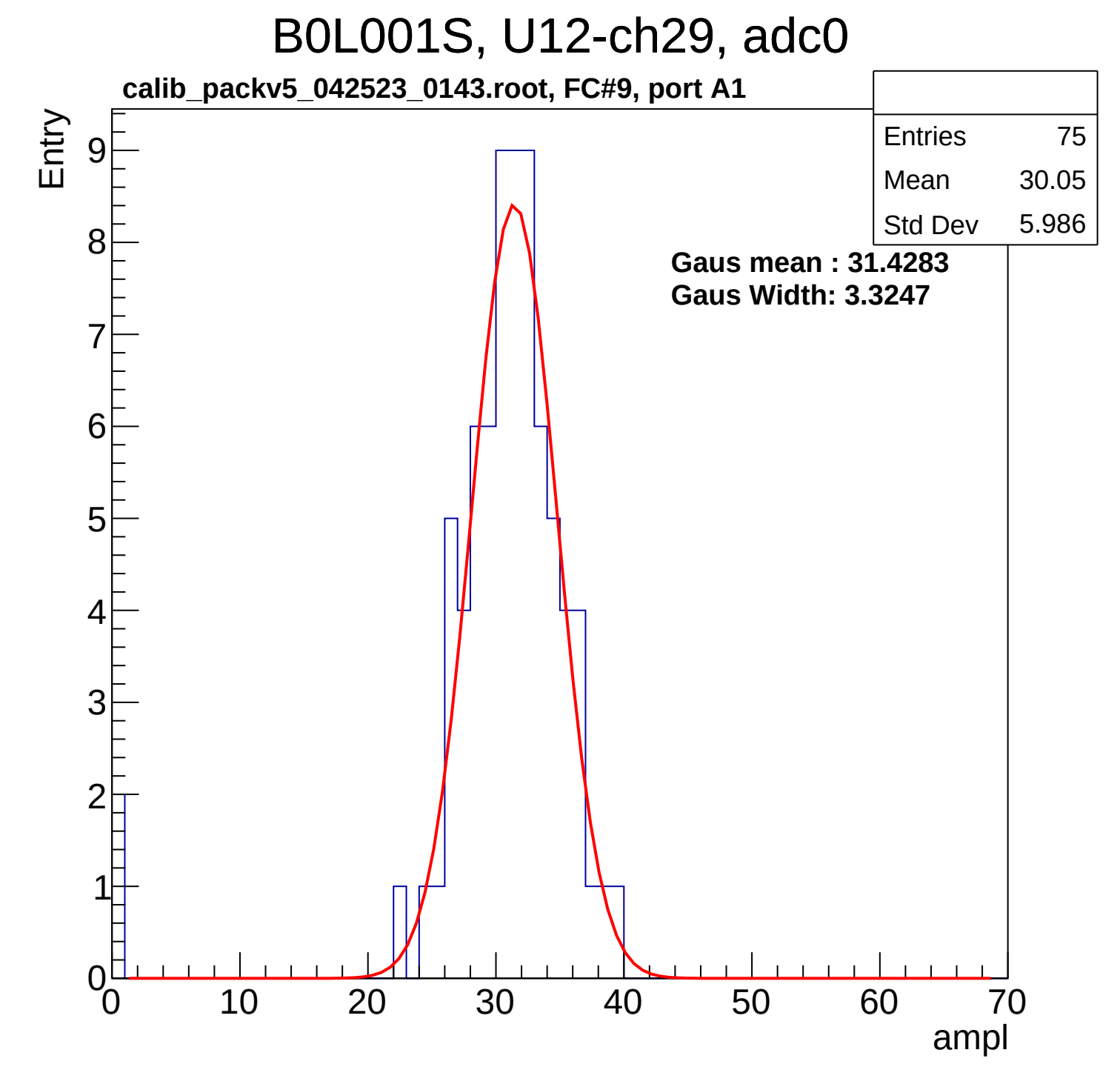
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch29, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 75
Mean 30.05
Std Dev 5.986
Gaus mean : 31.4283
Gaus Width: 3.3247
Entry
ampl
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3
4
5
6
7
8
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0
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20
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40
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60
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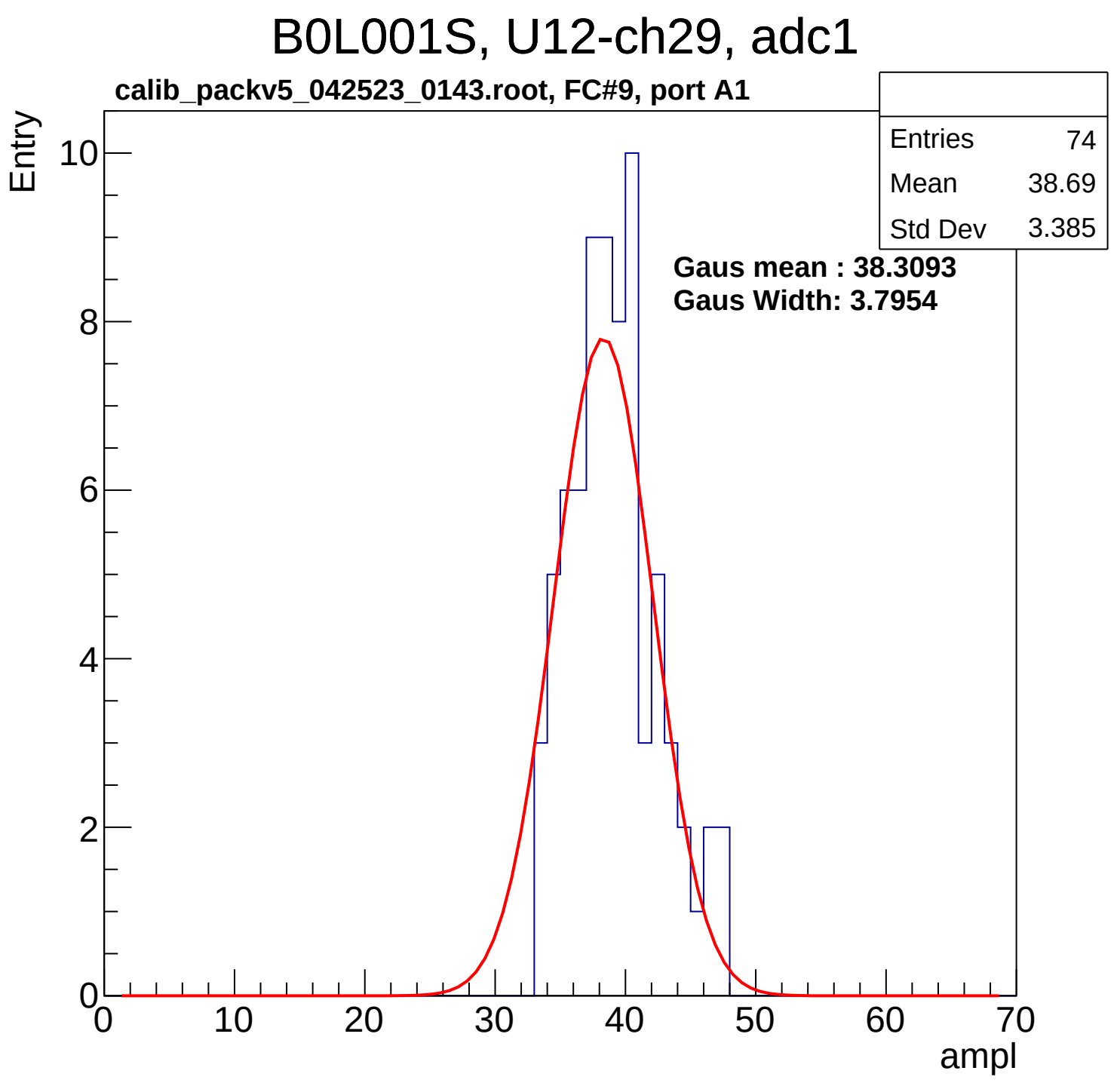
B0L001S, U12-ch29, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 74
Mean 38.69
Std Dev 3.385
Gaus mean : 38.3093
Gaus Width: 3.7954
Entry
ampl
0
2
4
6
8
10
0
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60
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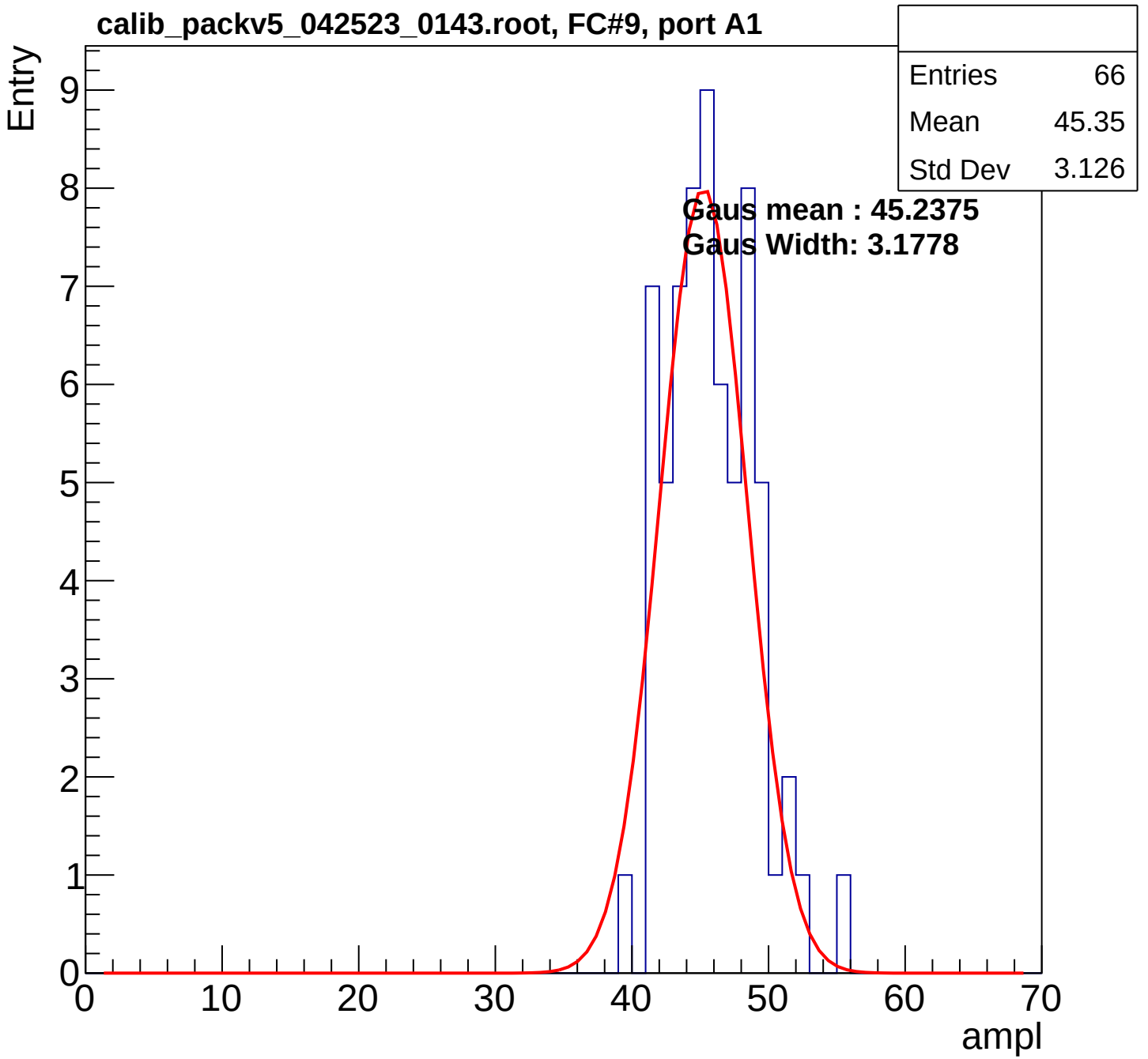
B0L001S, U12-ch29, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 66
Mean 45.35
Std Dev 3.126
Gaus mean : 45.2375
Gaus Width: 3.1778
Entry
ampl
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3
4
5
6
7
8
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0
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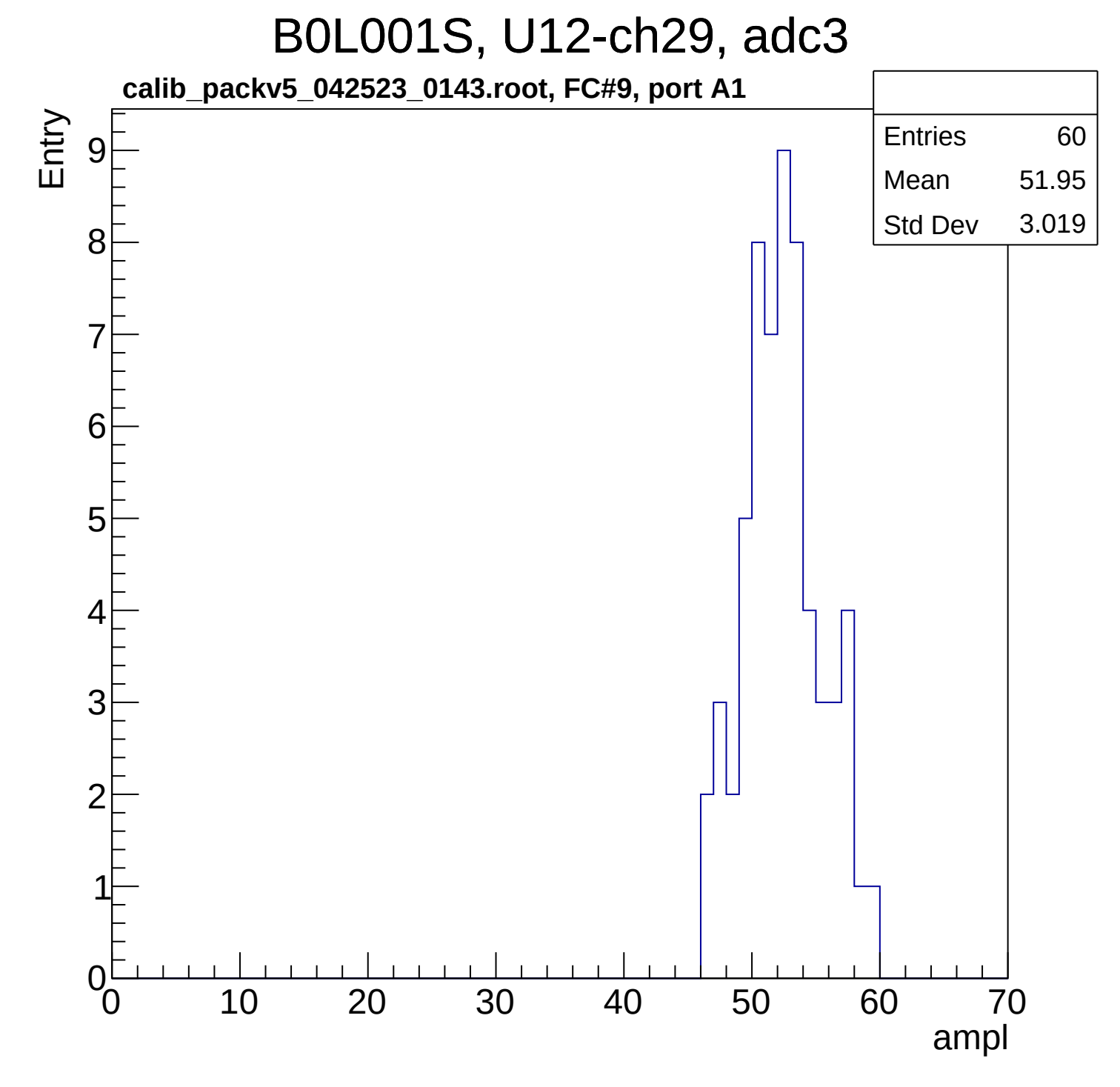
B0L001S, U12-ch29, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 60
Mean 51.95
Std Dev 3.019
Entry
ampl
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3
4
5
6
7
8
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0
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60
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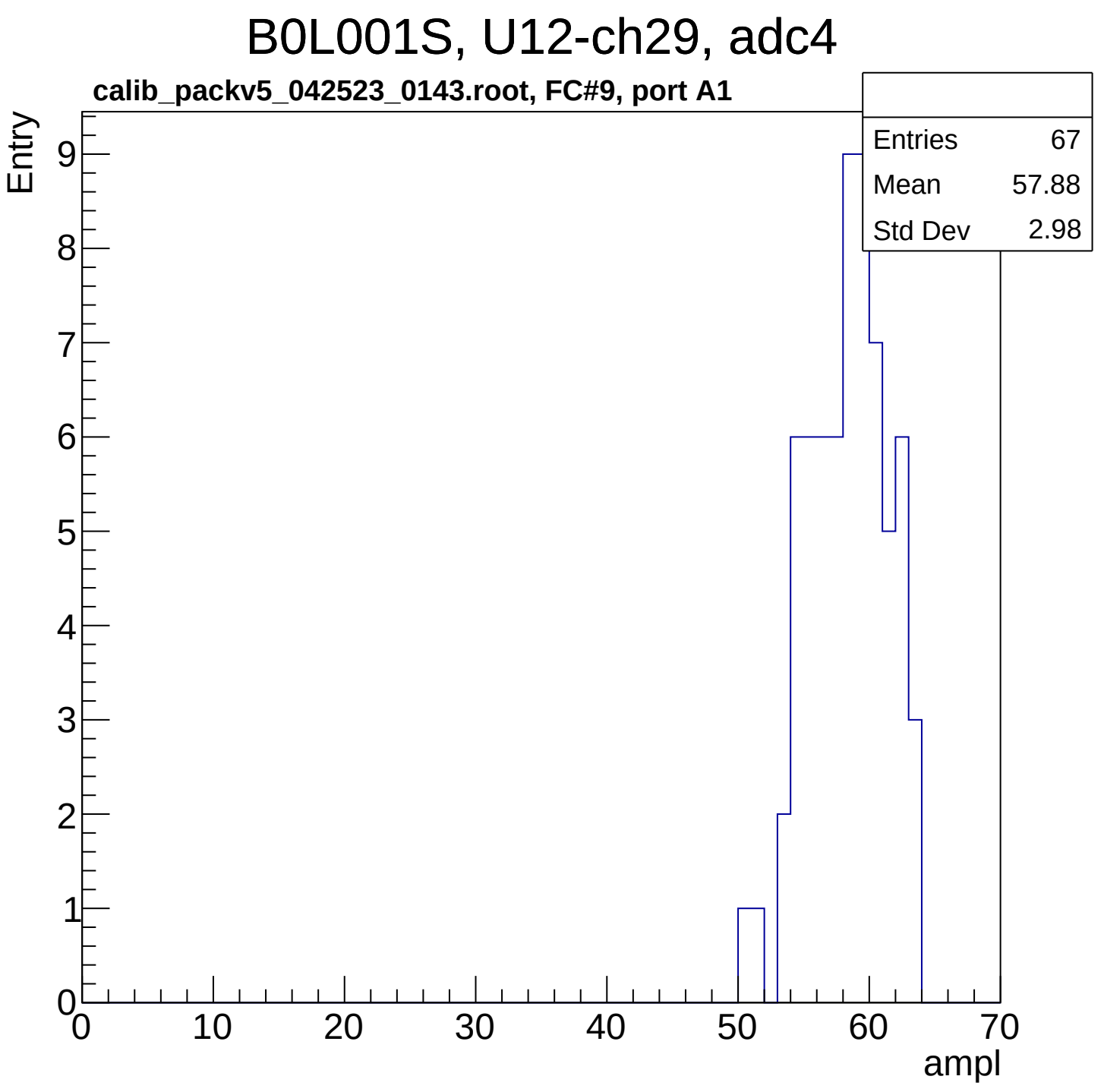
B0L001S, U12-ch29, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 67
Mean 57.88
Std Dev 2.98
Entry
ampl
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2
3
4
5
6
7
8
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0
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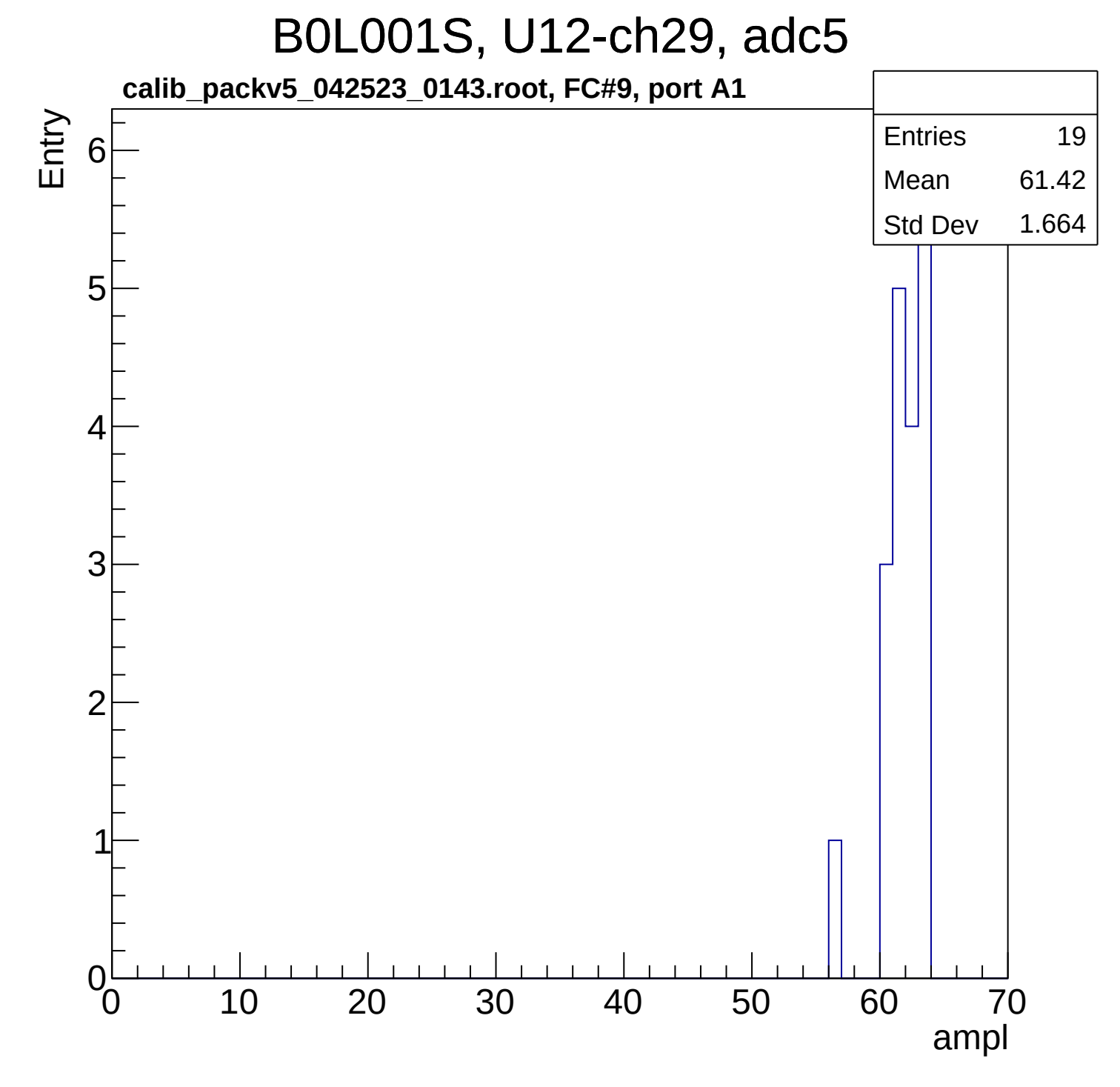
B0L001S, U12-ch29, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 19
Mean 61.42
Std Dev 1.664
Entry
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2
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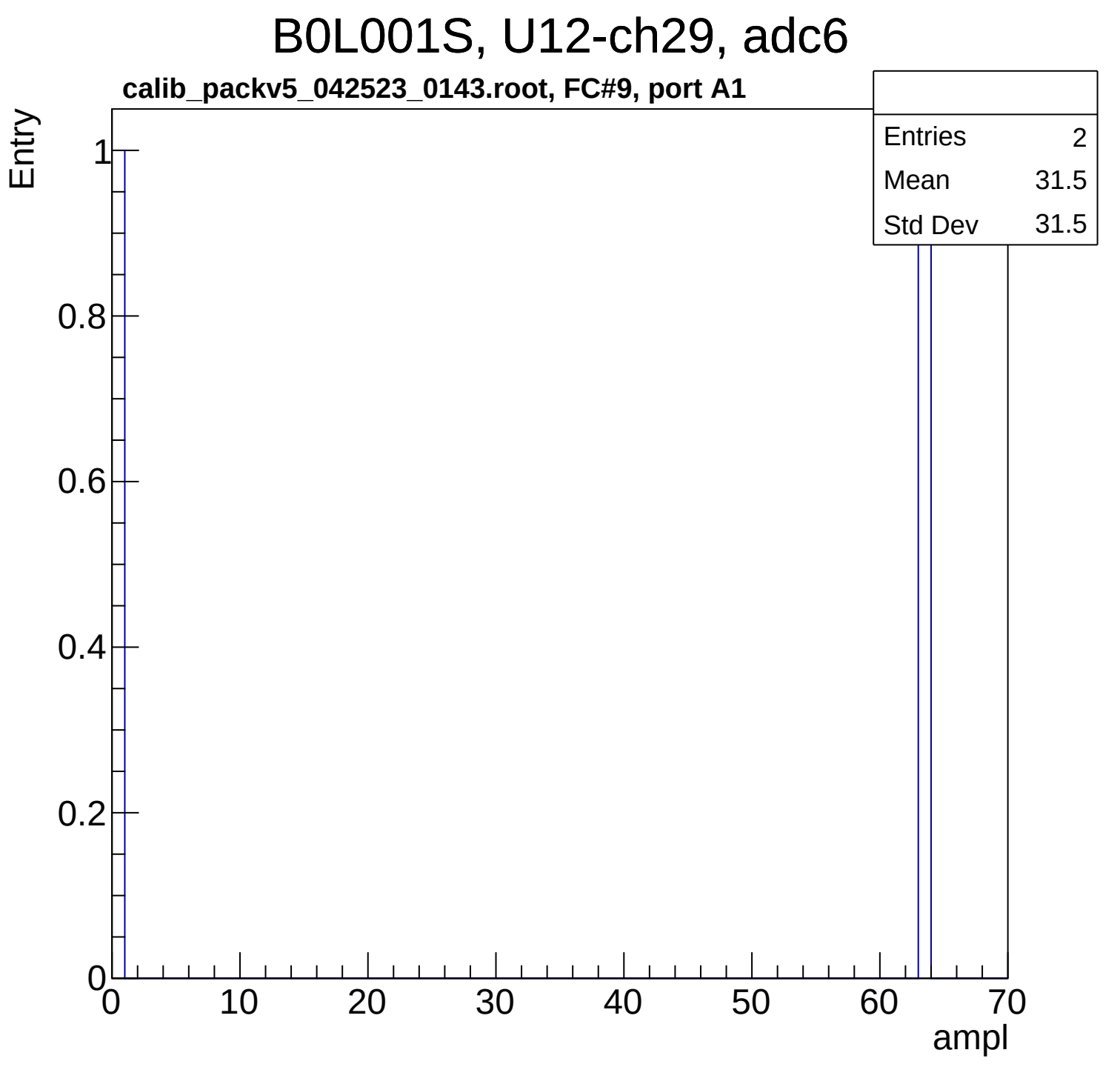
4
5
6
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch29, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 31.5
Std Dev 31.5
Entry
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0.6
0.4
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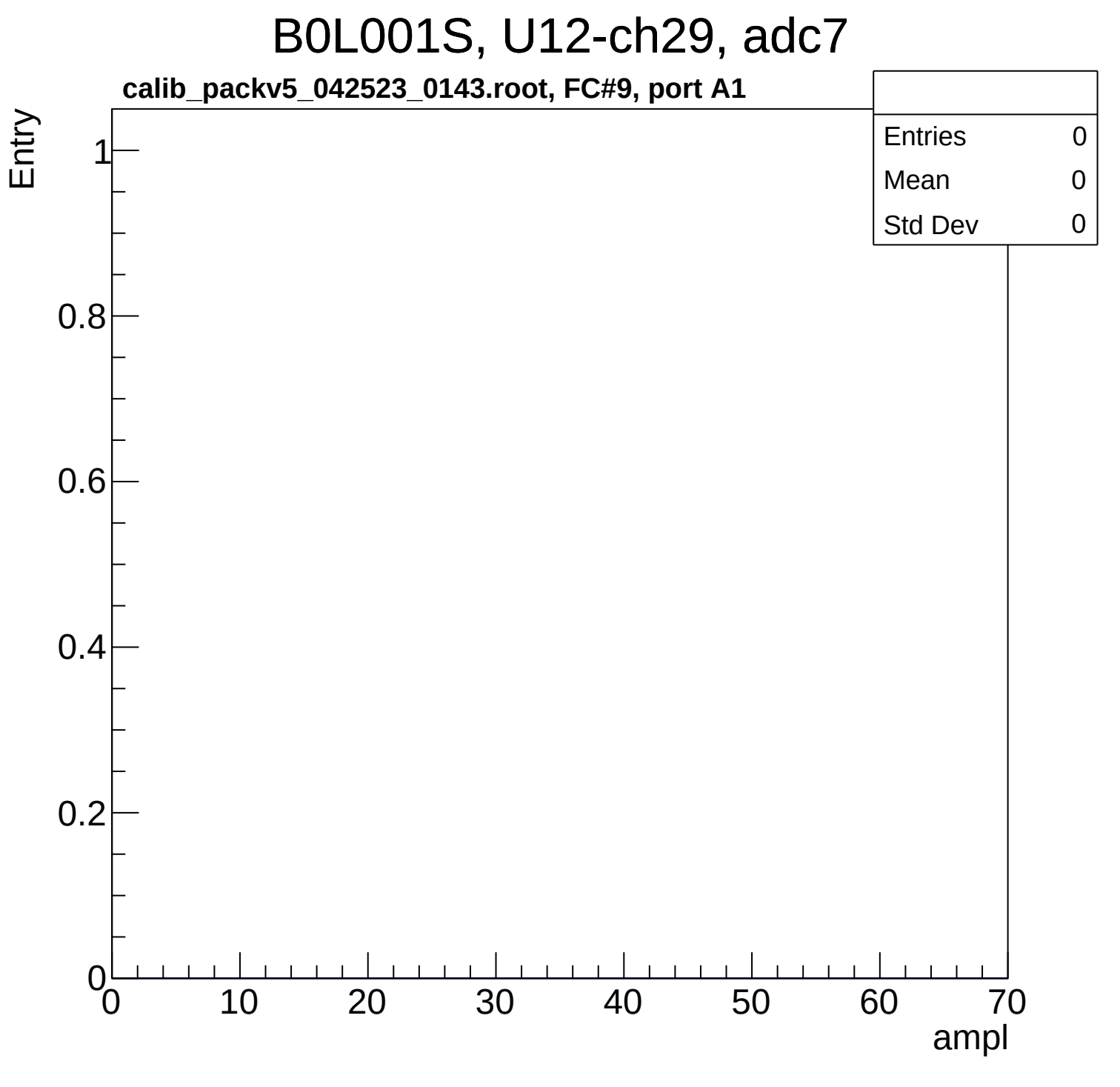
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch29, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
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0.6
0.4
0.2
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10
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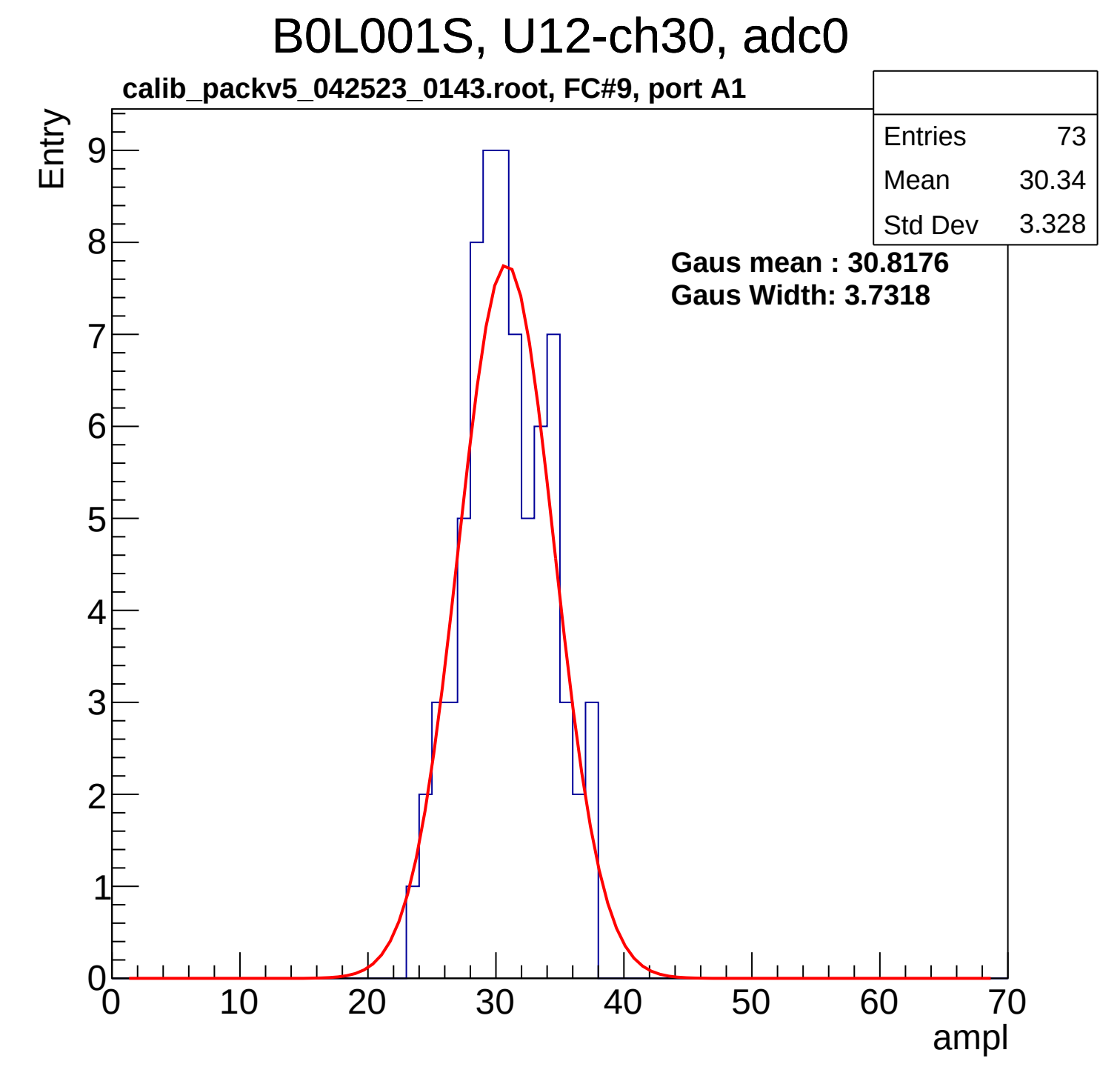
50
60
70
ampl


B0L001S, U12-ch30, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 73
Mean 30.34
Std Dev 3.328
Gaus mean : 30.8176
Gaus Width: 3.7318
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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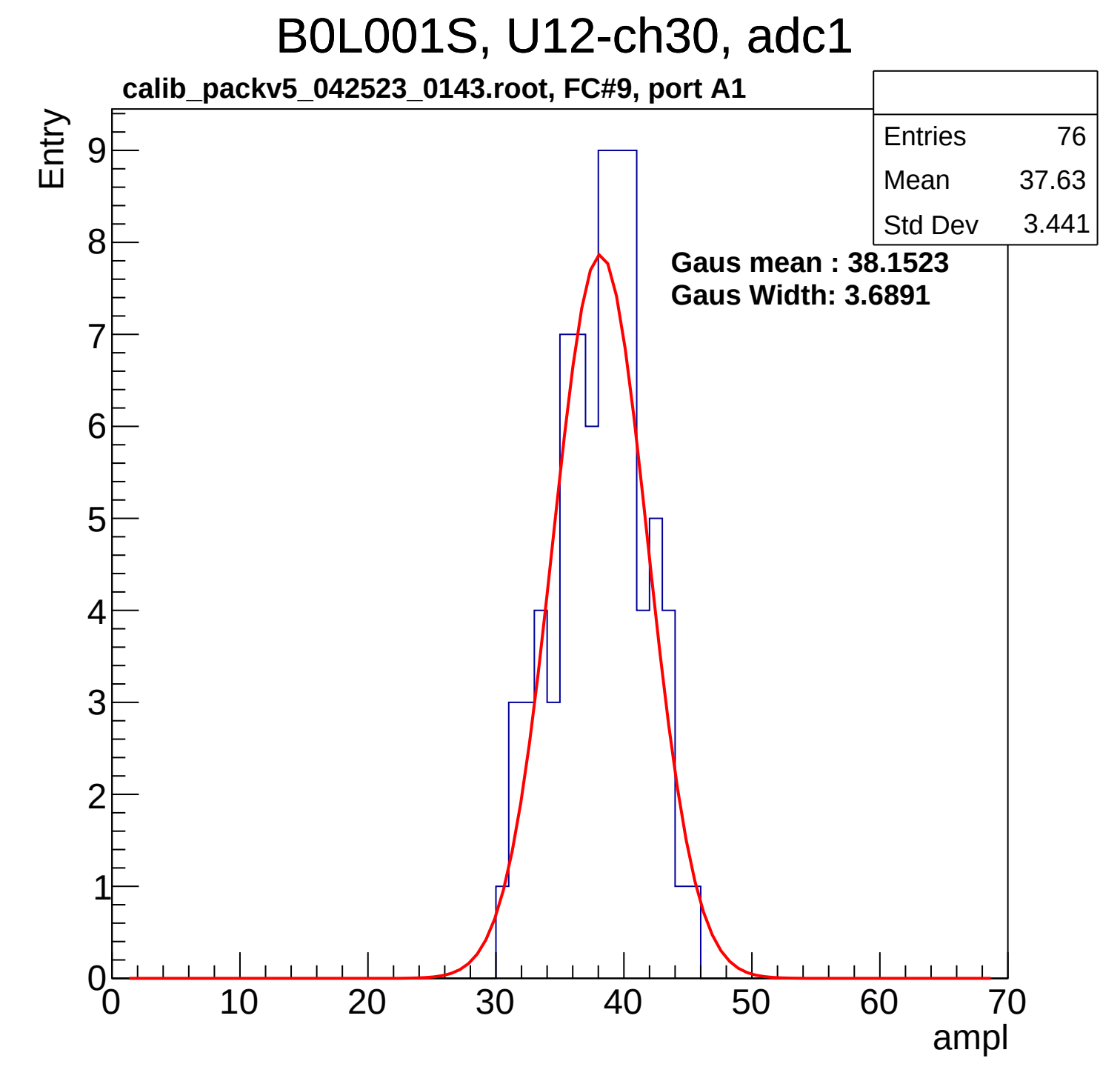
B0L001S, U12-ch30, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 76
Mean 37.63
Std Dev 3.441
Gaus mean : 38.1523
Gaus Width: 3.6891
Entry
ampl
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3
4
5
6
7
8
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0
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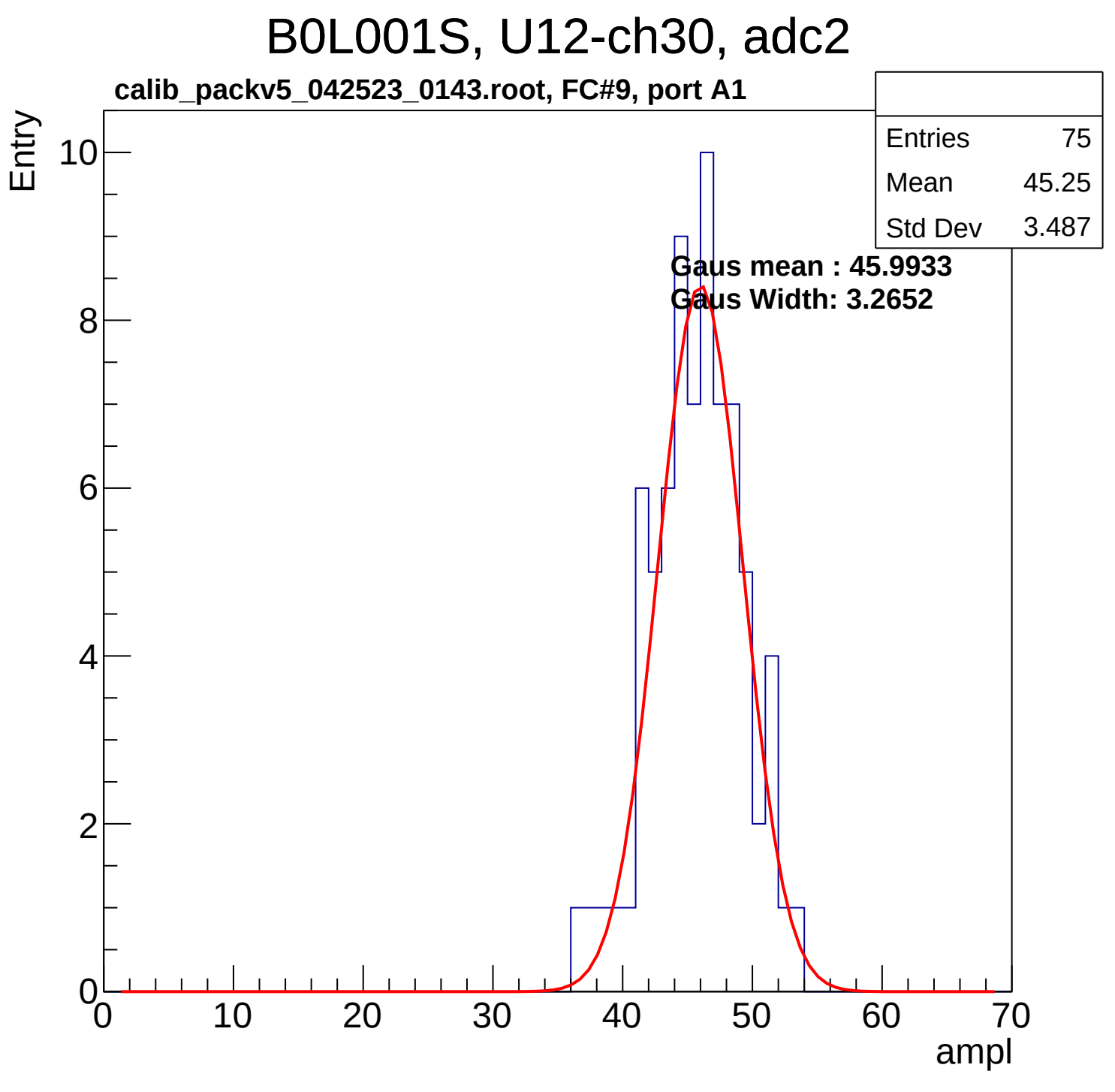
B0L001S, U12-ch30, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 75
Mean 45.25
Std Dev 3.487
Gaus mean : 45.9933
Gaus Width: 3.2652
Entry
ampl
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8
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0
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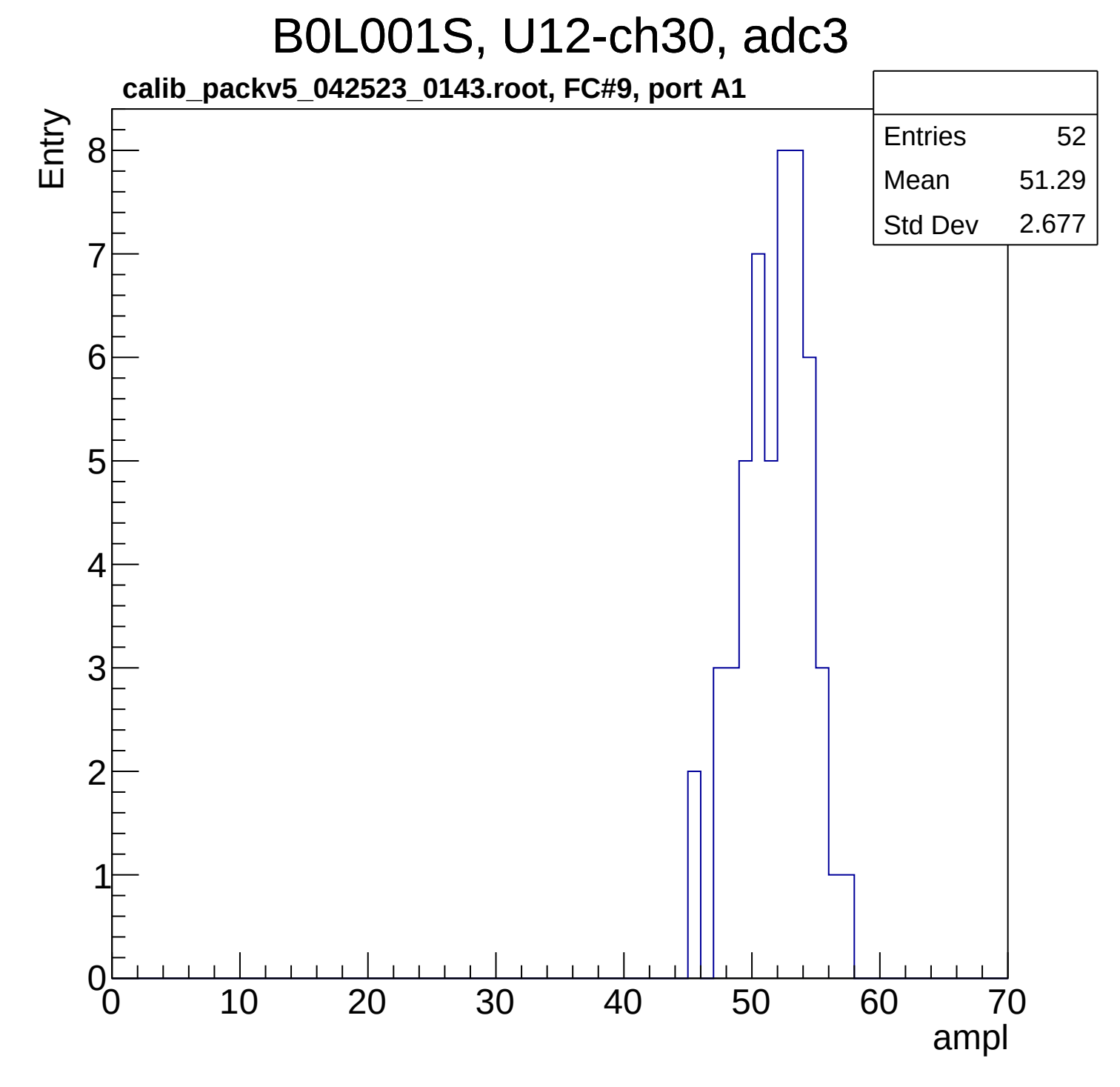
B0L001S, U12-ch30, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 52
Mean 51.29
Std Dev 2.677
Entry
ampl
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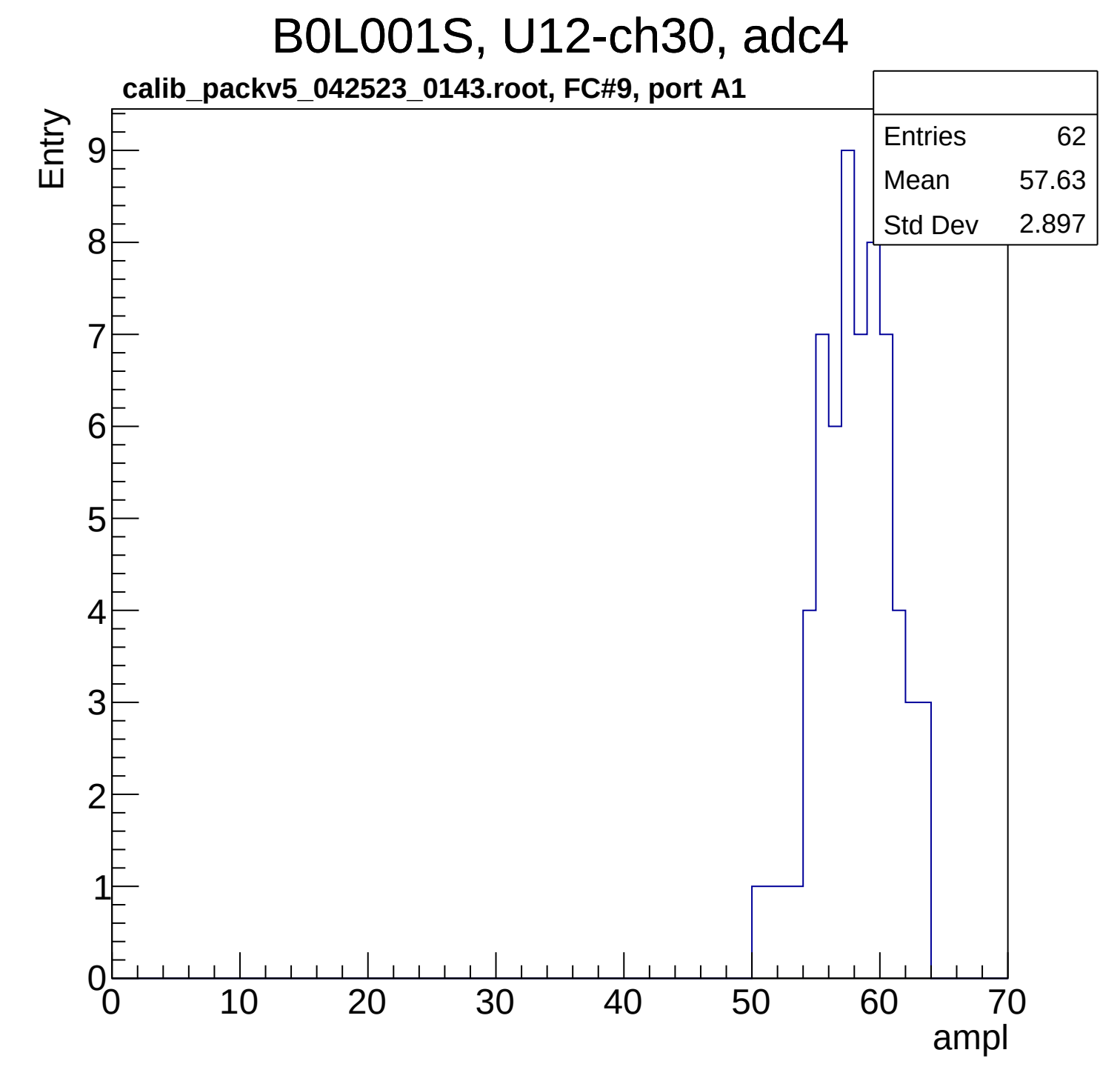
B0L001S, U12-ch30, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 62
Mean 57.63
Std Dev 2.897
Entry
ampl
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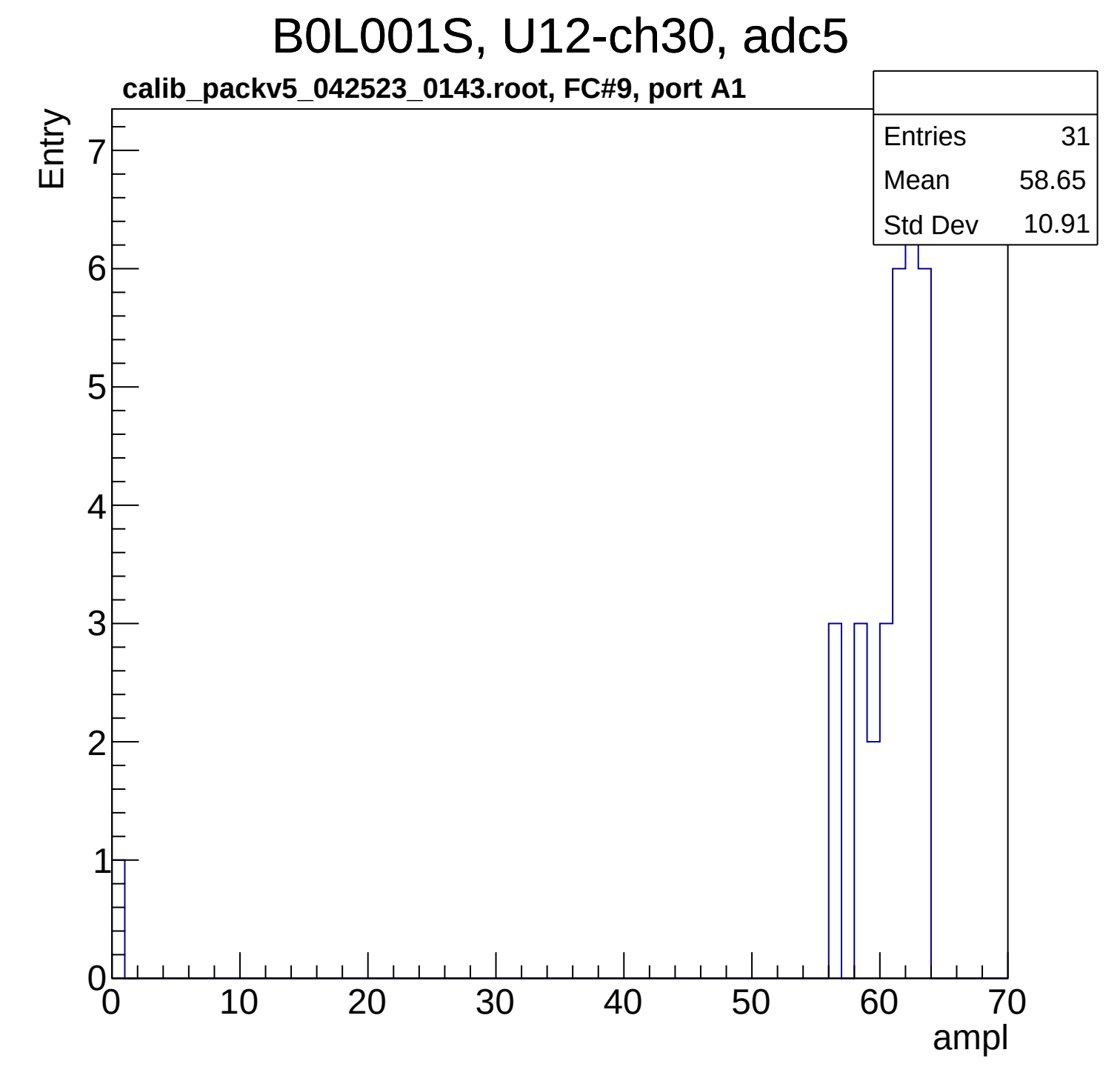
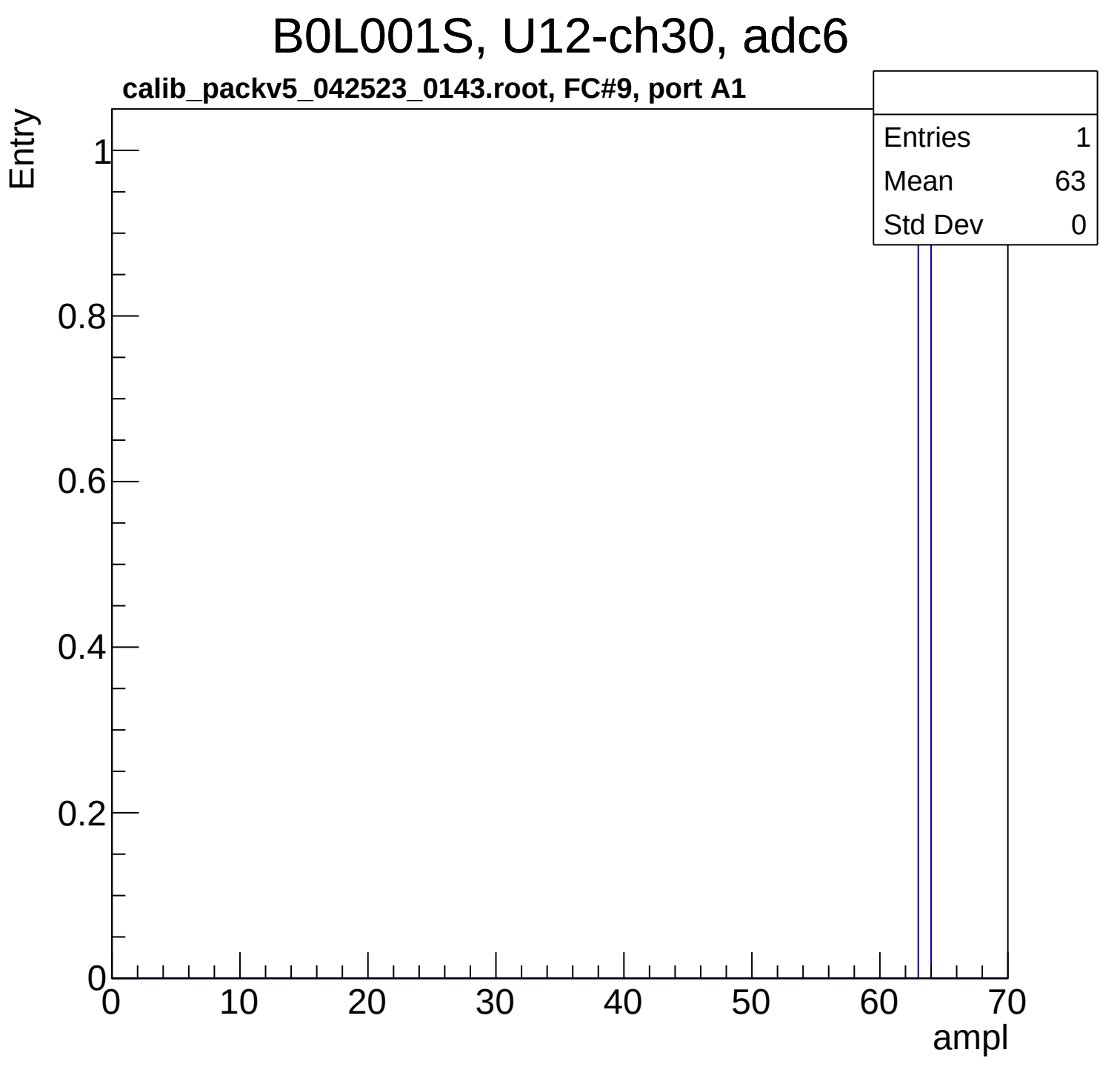

B0L001S, U12-ch30, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 31
Mean 58.65
Std Dev 10.91
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B0L001S, U12-ch30, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
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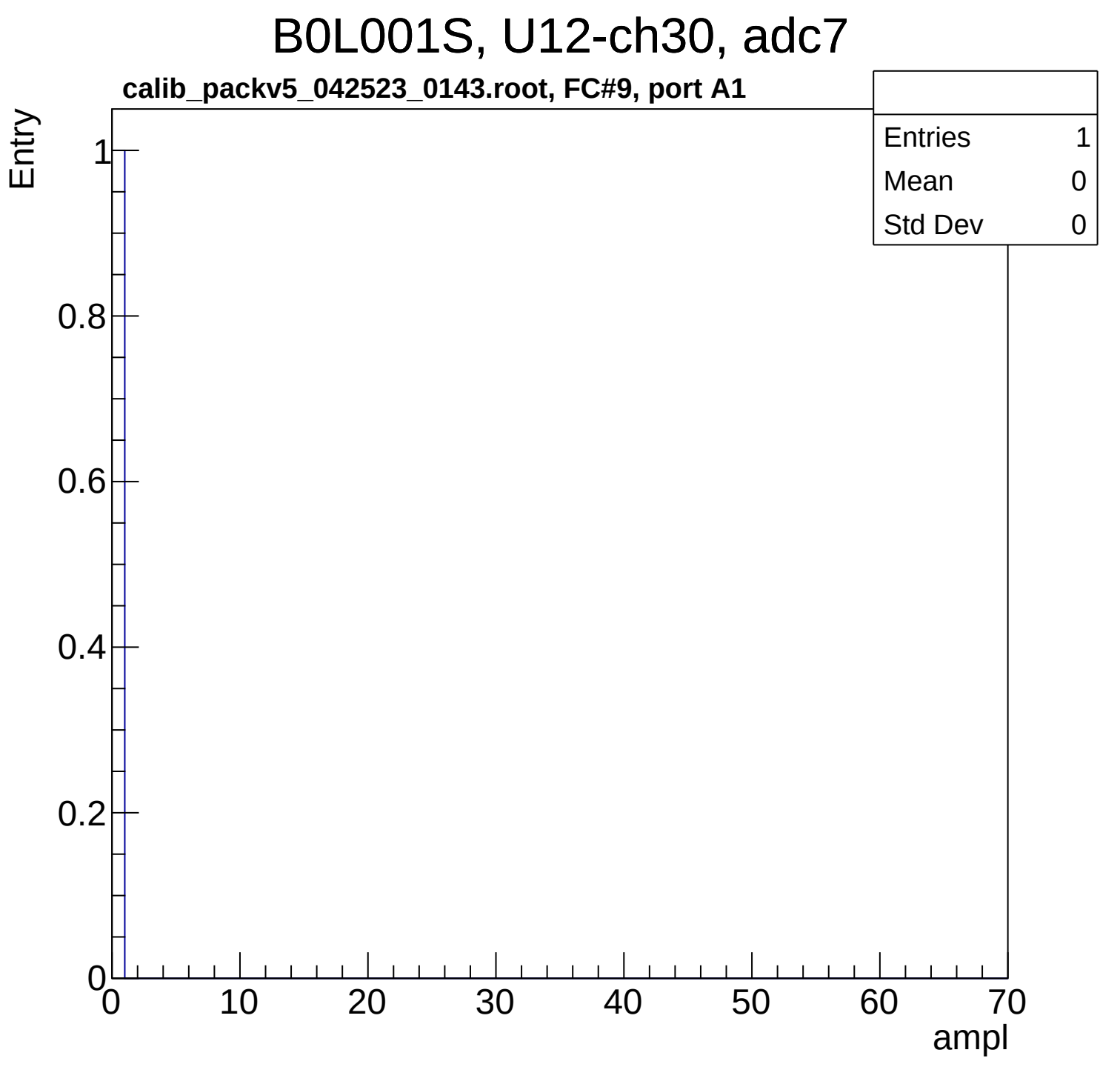
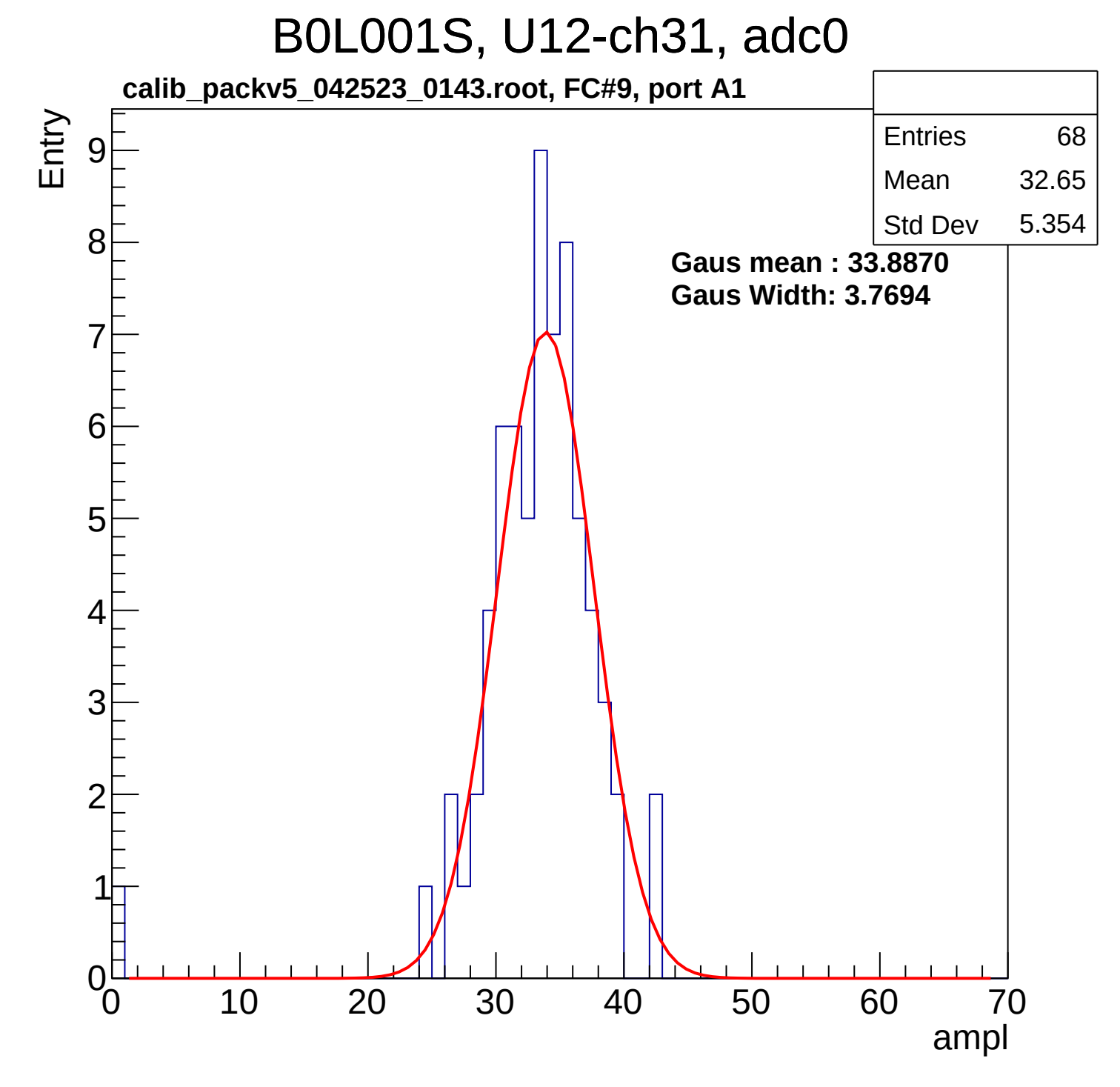
40
50
60
70
ampl


B0L001S, U12-ch30, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch31, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 68
Mean 32.65
Std Dev 5.354
Gaus mean : 33.8870
Gaus Width: 3.7694
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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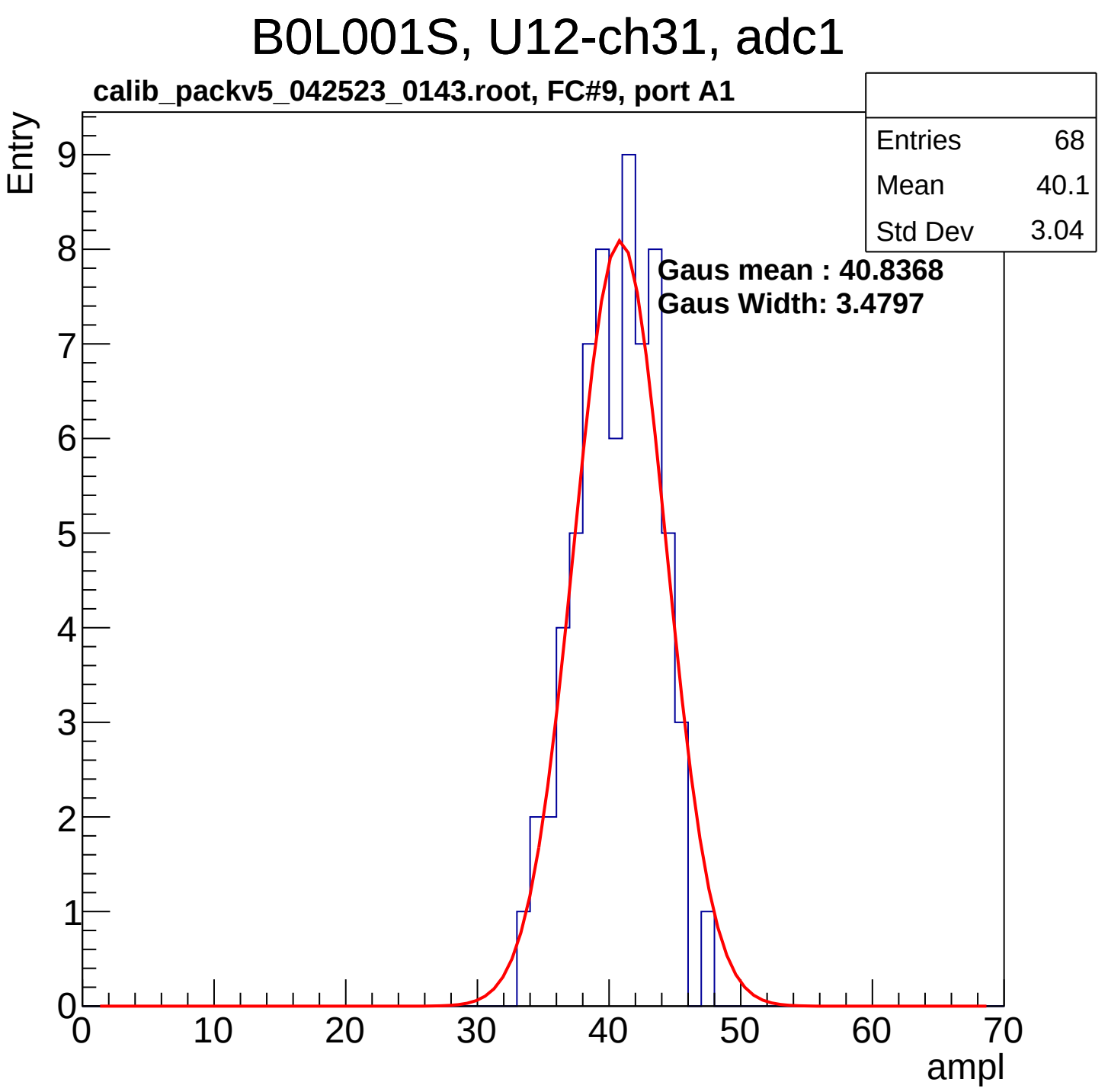
B0L001S, U12-ch31, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 68
Mean 40.1
Std Dev 3.04
Gaus mean : 40.8368
Gaus Width: 3.4797
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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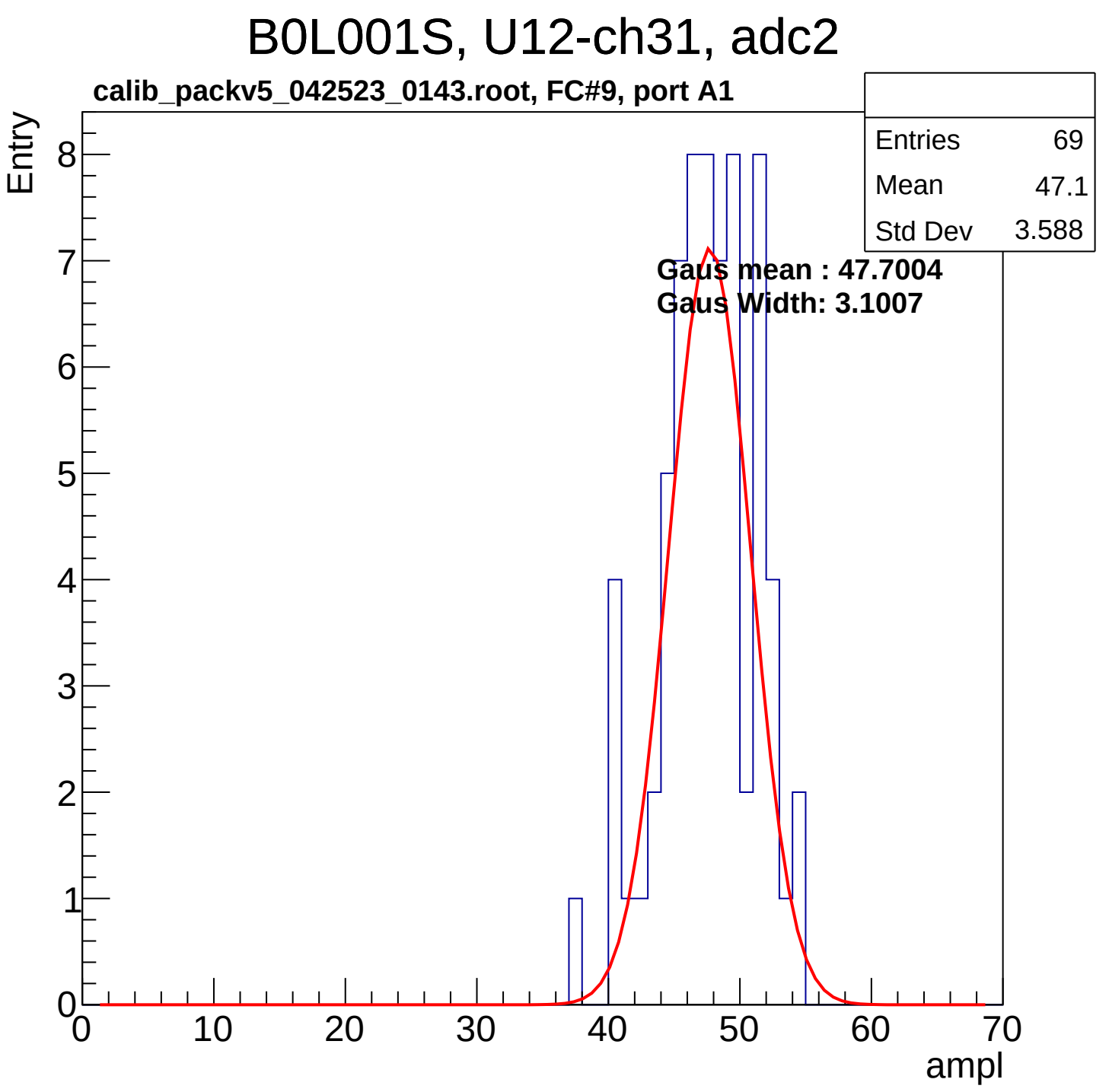
B0L001S, U12-ch31, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 69
Mean 47.1
Std Dev 3.588
Gaus mean : 47.7004
Gaus Width: 3.1007
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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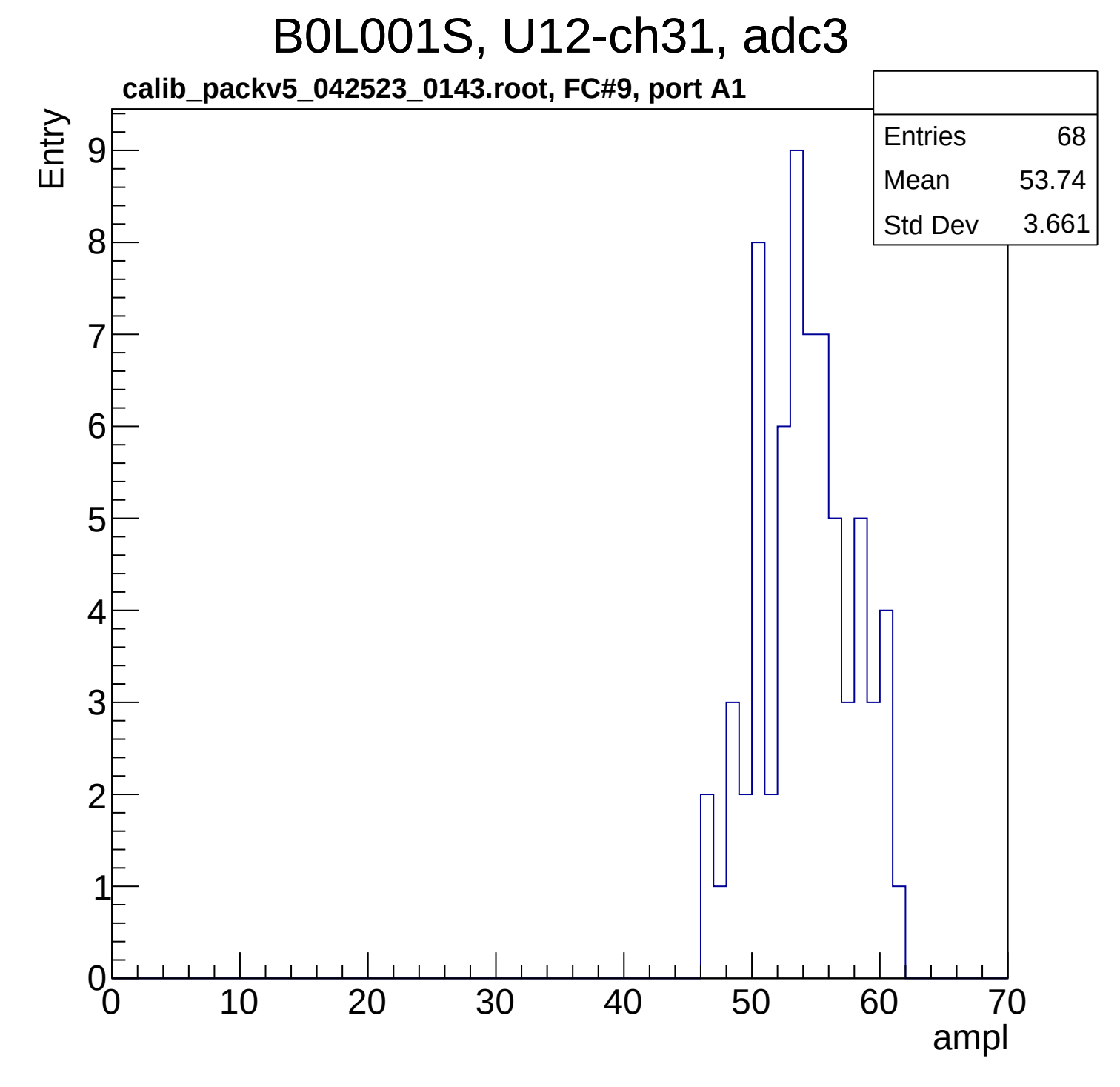
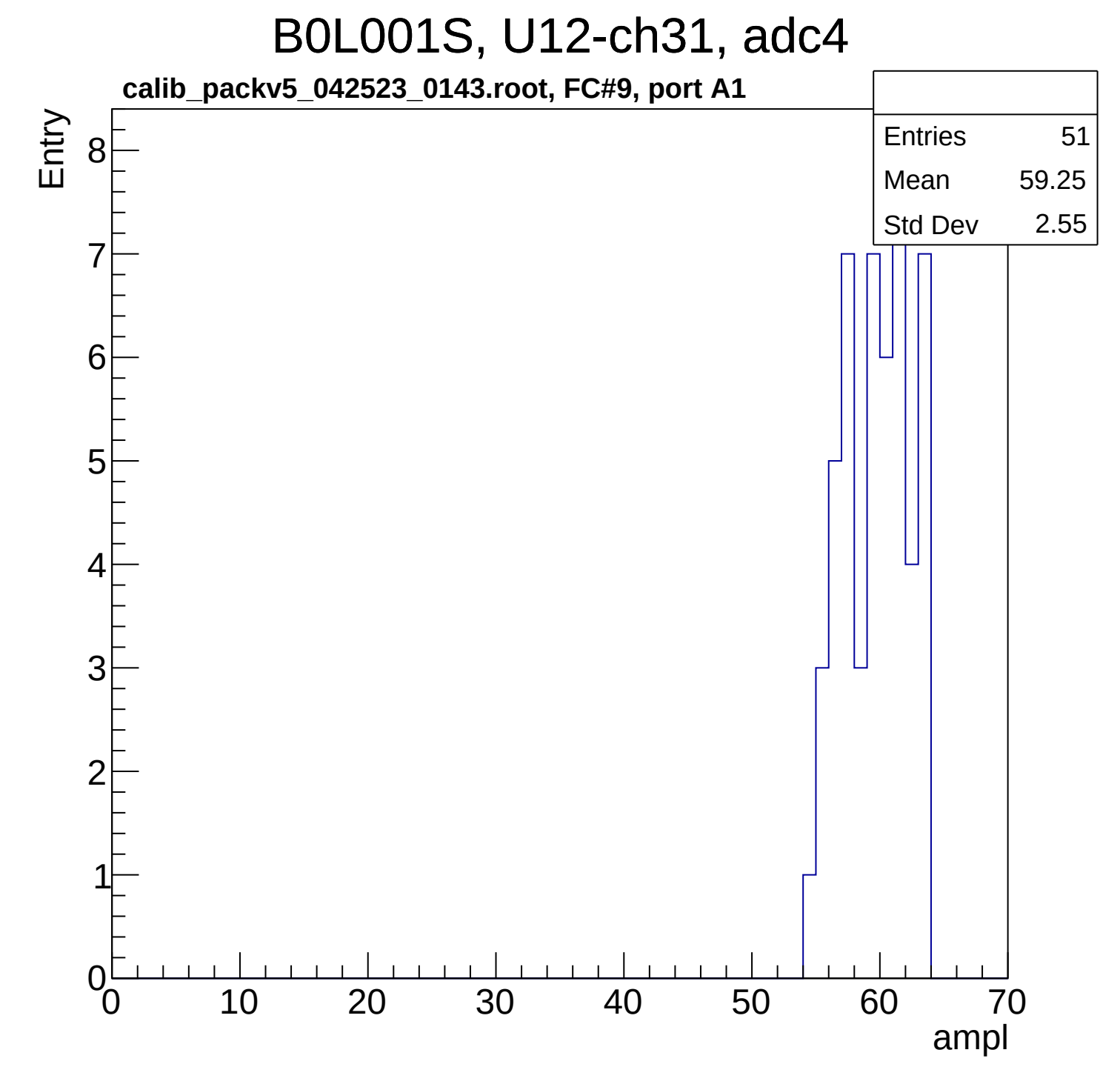
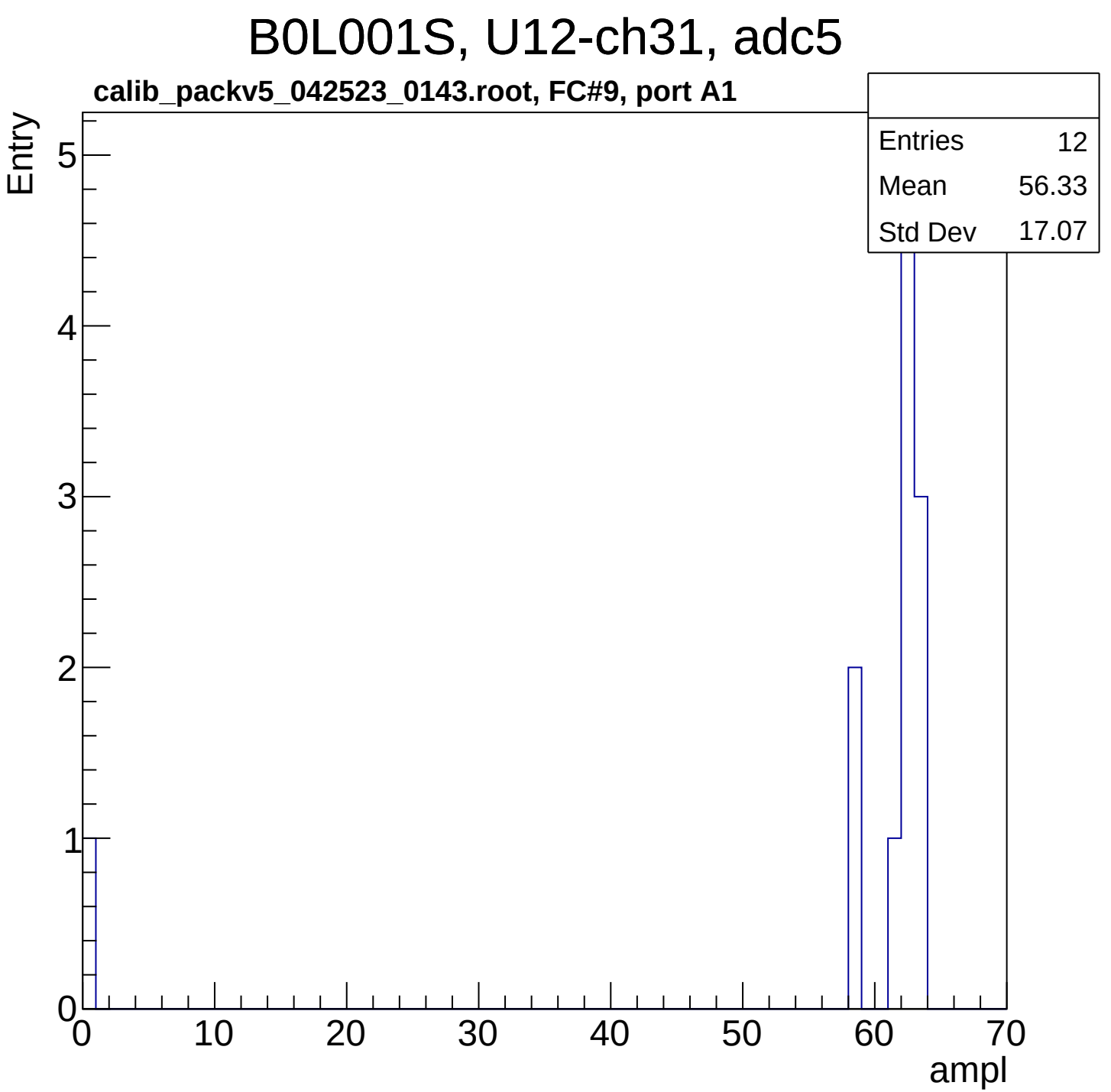
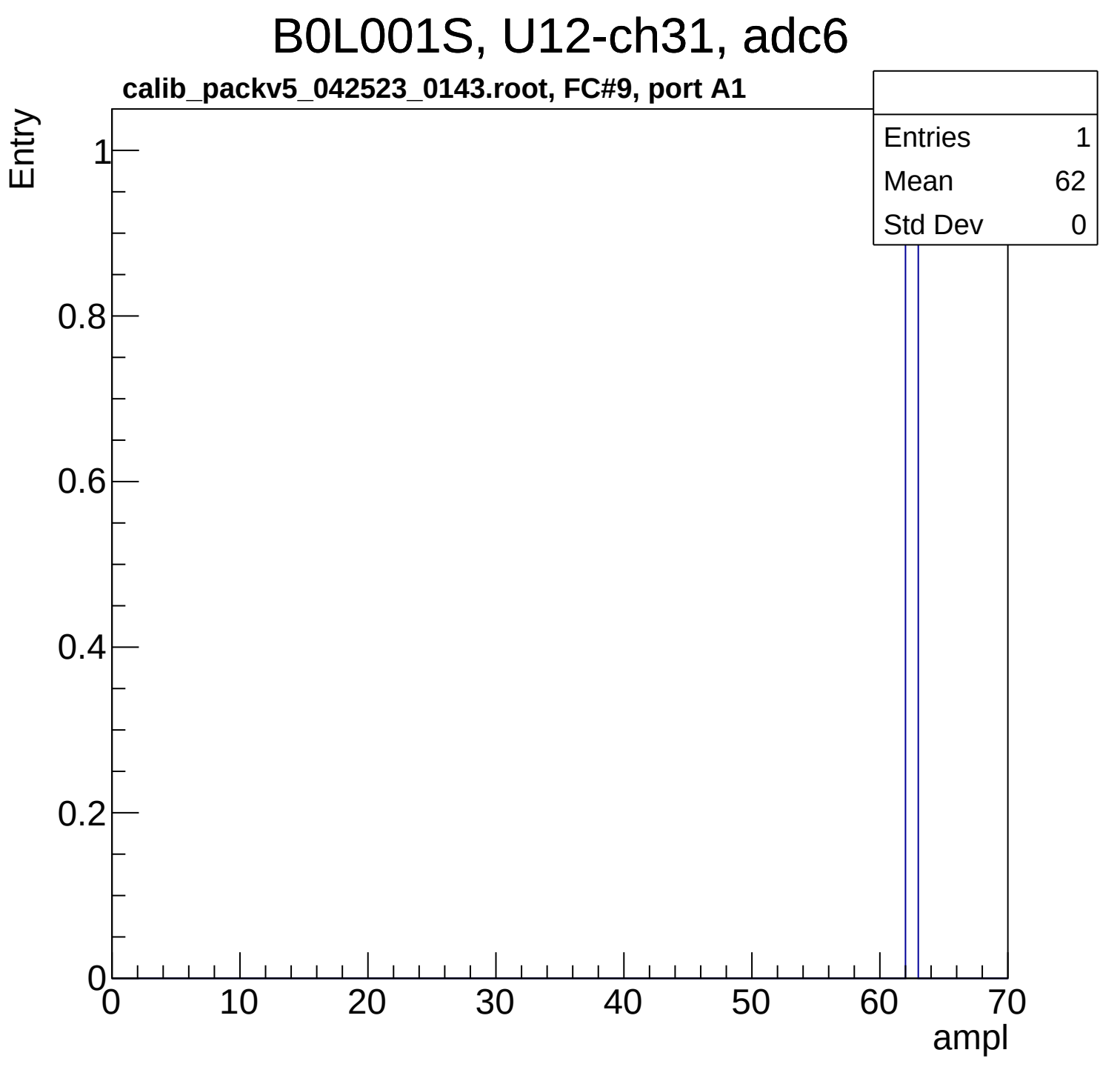
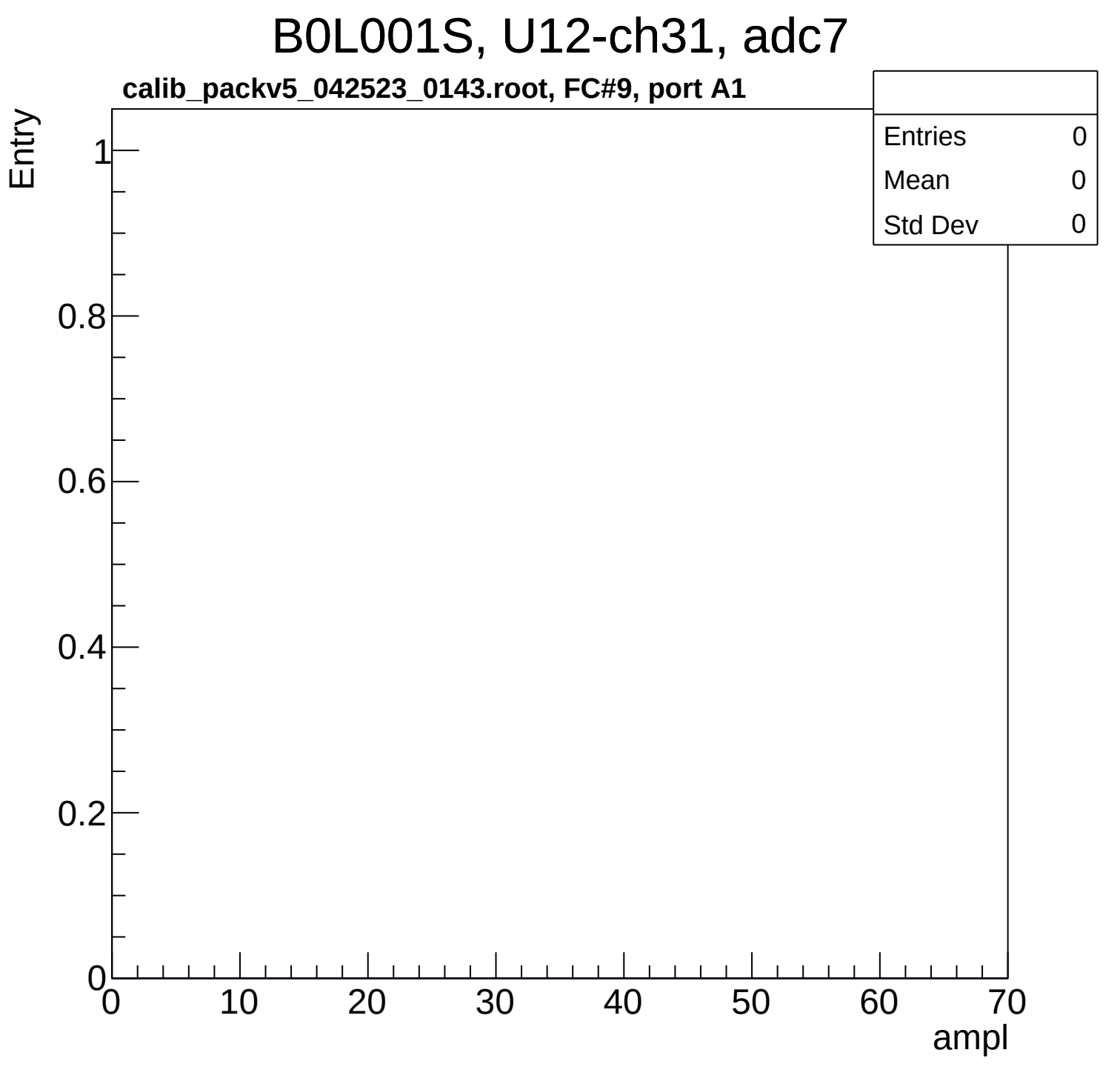
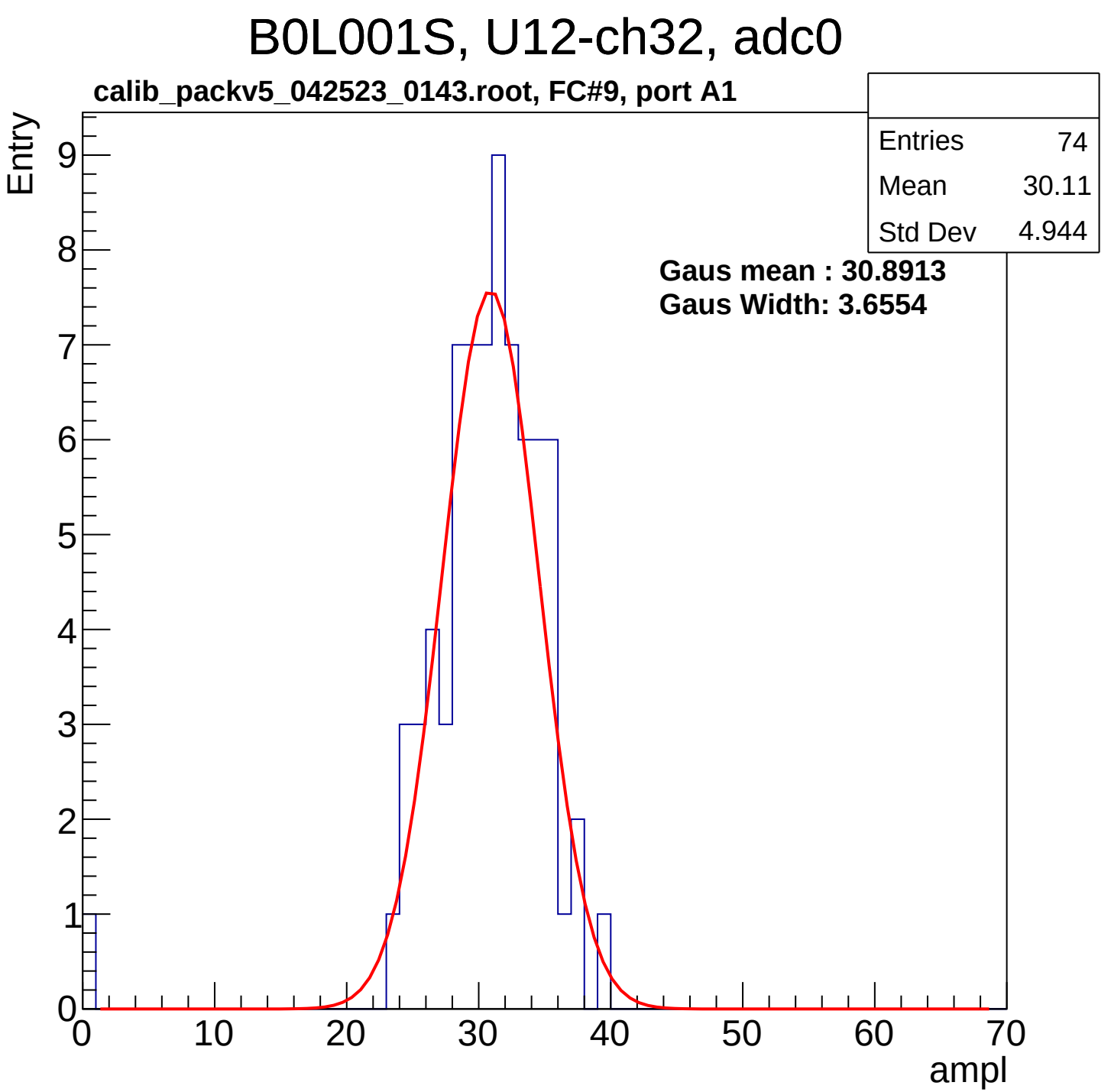

B0L001S, U12-ch31, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 68
Mean 53.74
Std Dev 3.661
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

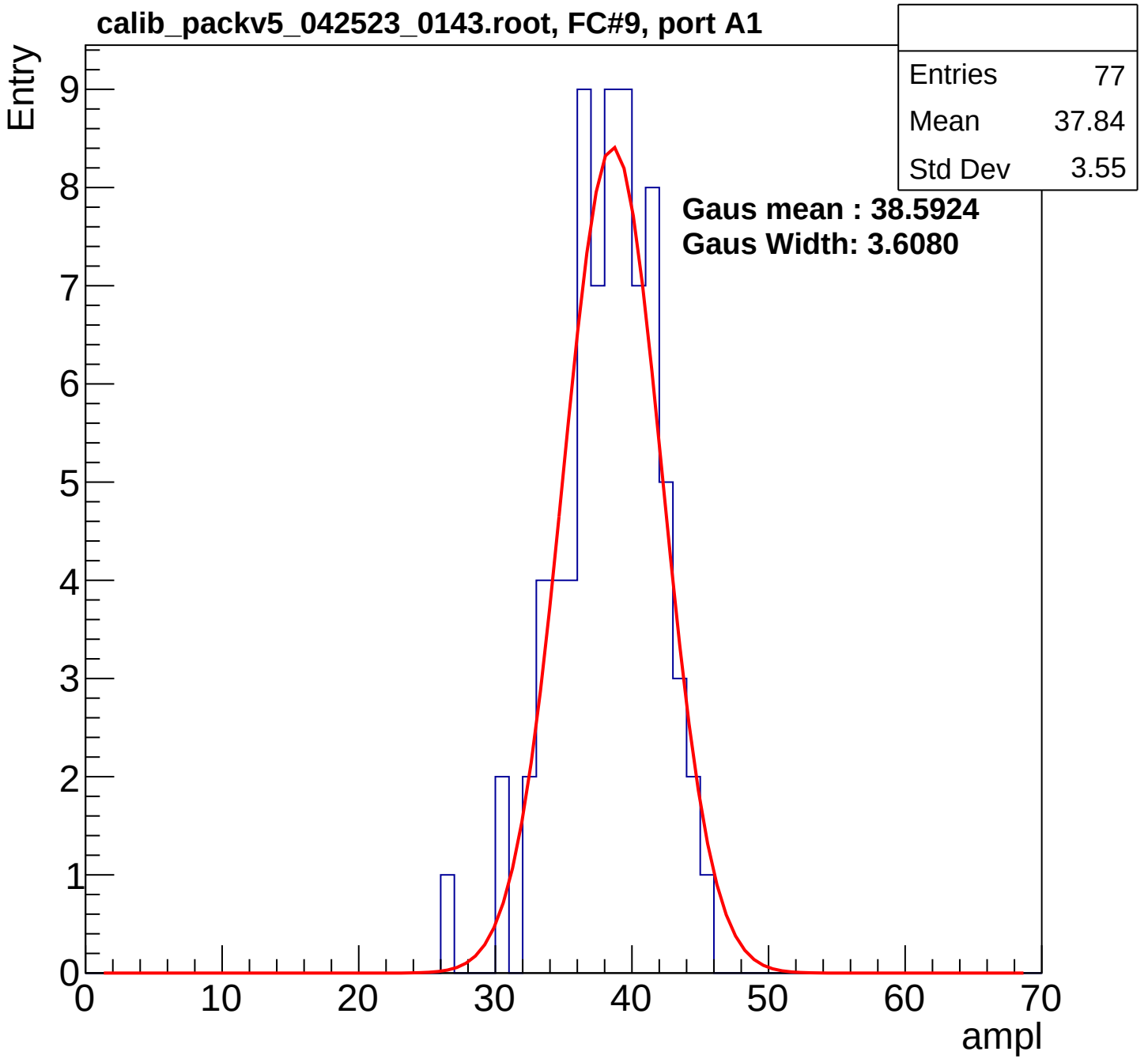

B0L001S, U12-ch31, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 51
Mean 59.25
Std Dev 2.55
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

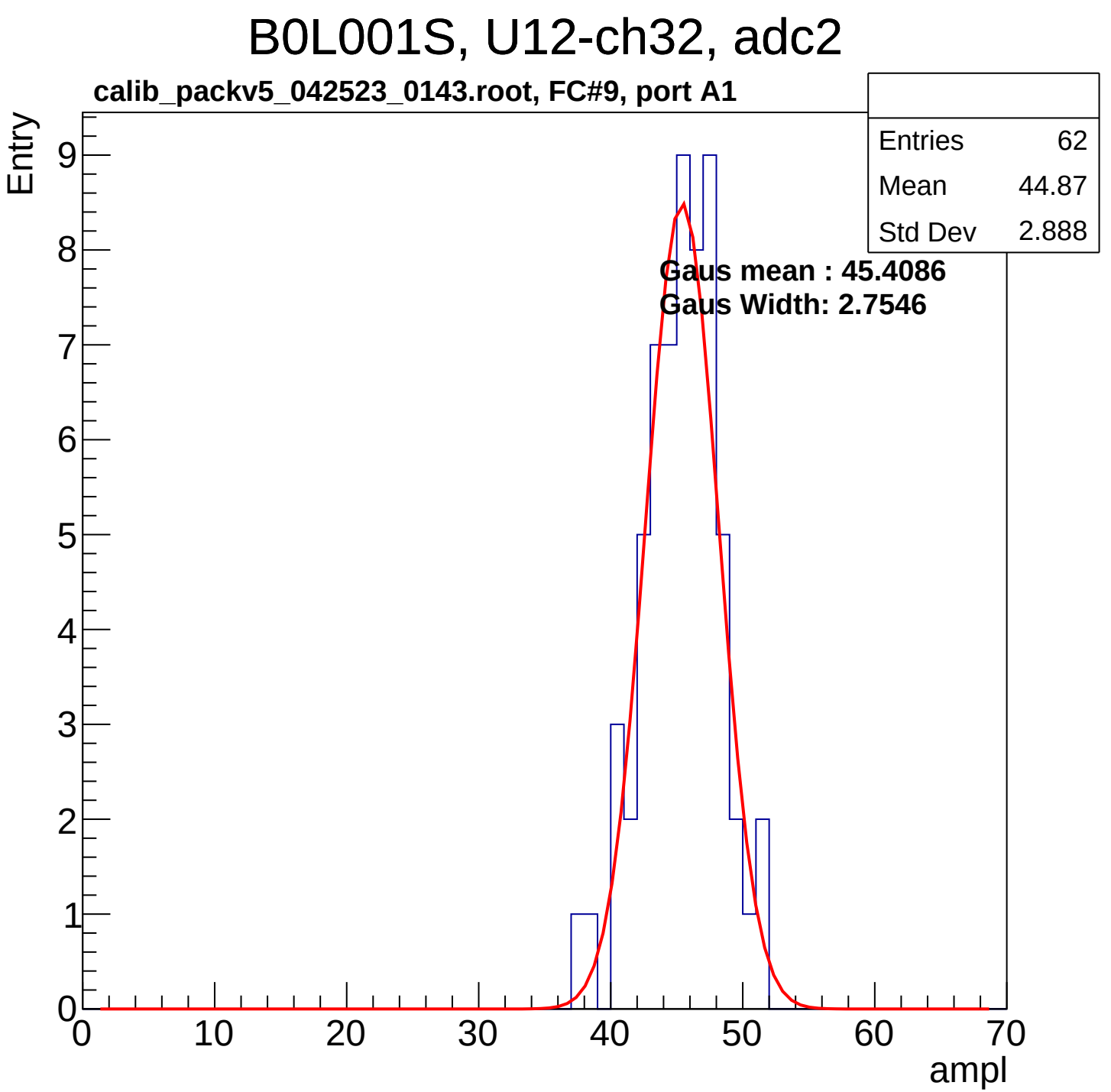

B0L001S, U12-ch31, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 12
Mean 56.33
Std Dev 17.07
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

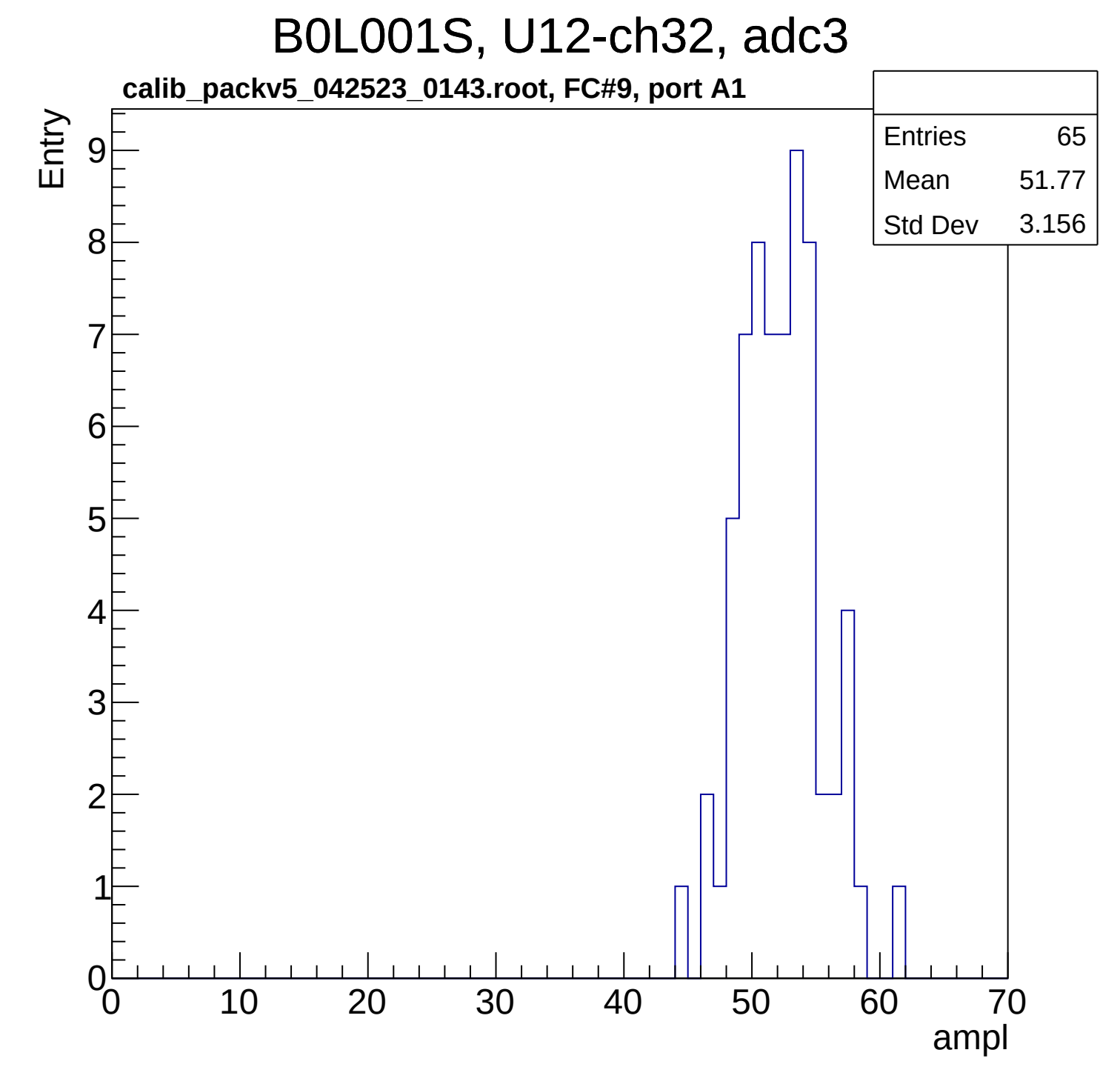

B0L001S, U12-ch31, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

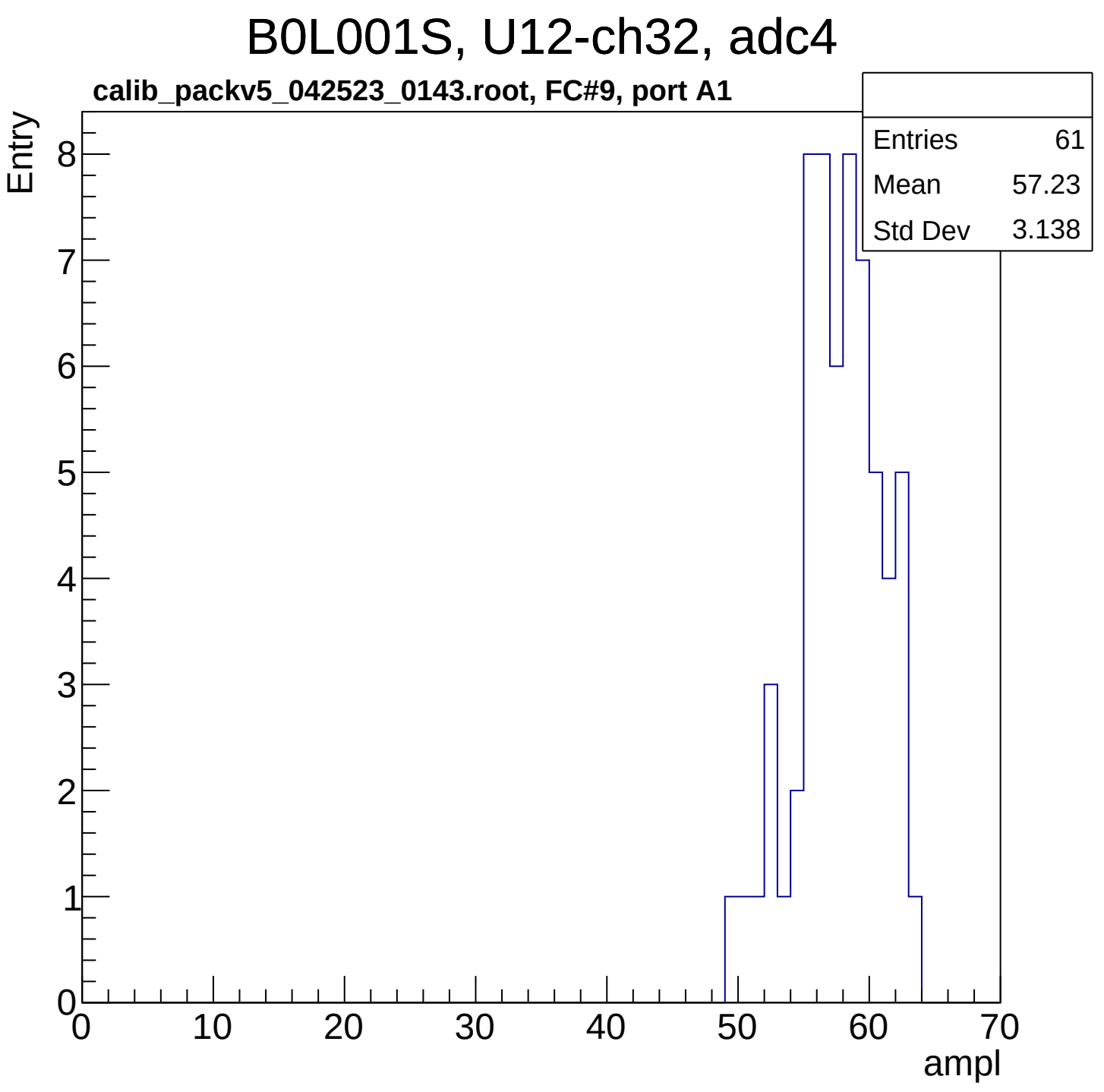

B0L001S, U12-ch31, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

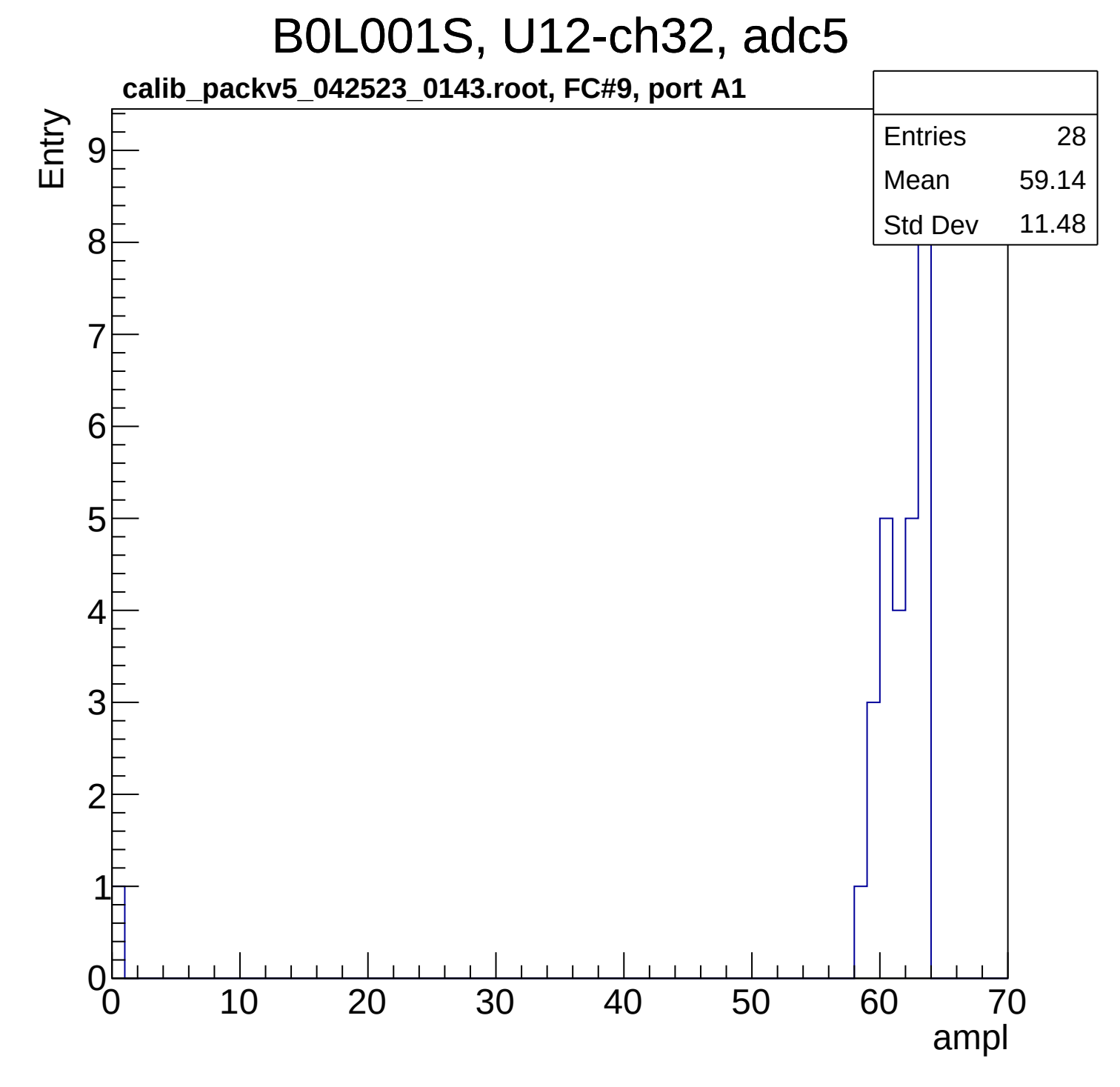

B0L001S, U12-ch32, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 74
Mean 30.11
Std Dev 4.944
Gaus mean : 30.8913
Gaus Width: 3.6554
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch32, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 77
Mean 37.84
Std Dev 3.55
Gaus mean : 38.5924
Gaus Width: 3.6080
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch32, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 62
Mean 44.87
Std Dev 2.888
Gaus mean : 45.4086
Gaus Width: 2.7546
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch32, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 65
Mean 51.77
Std Dev 3.156
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch32, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 61
Mean 57.23
Std Dev 3.138
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch32, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 28
Mean 59.14
Std Dev 11.48
Entry
ampl
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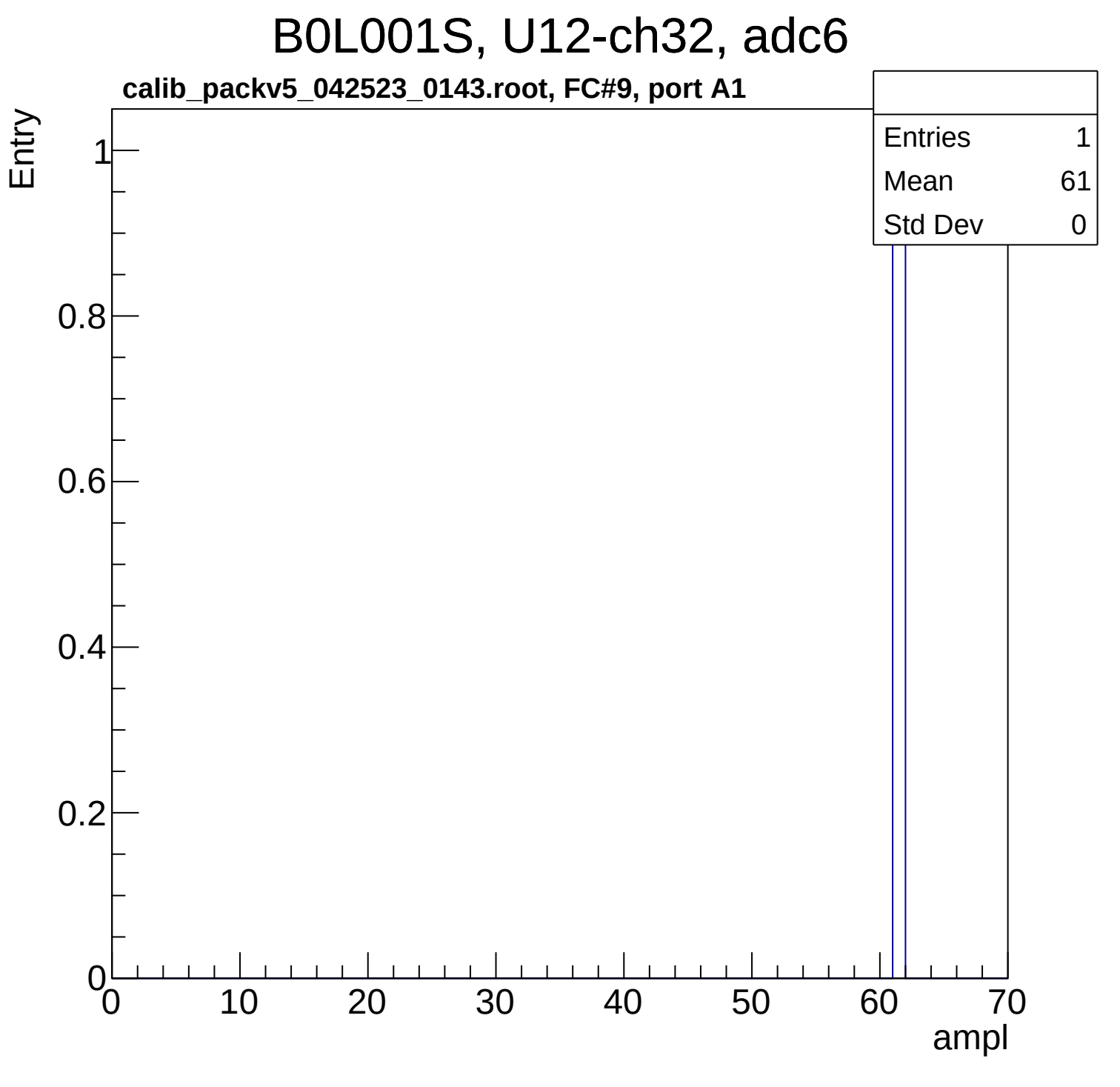
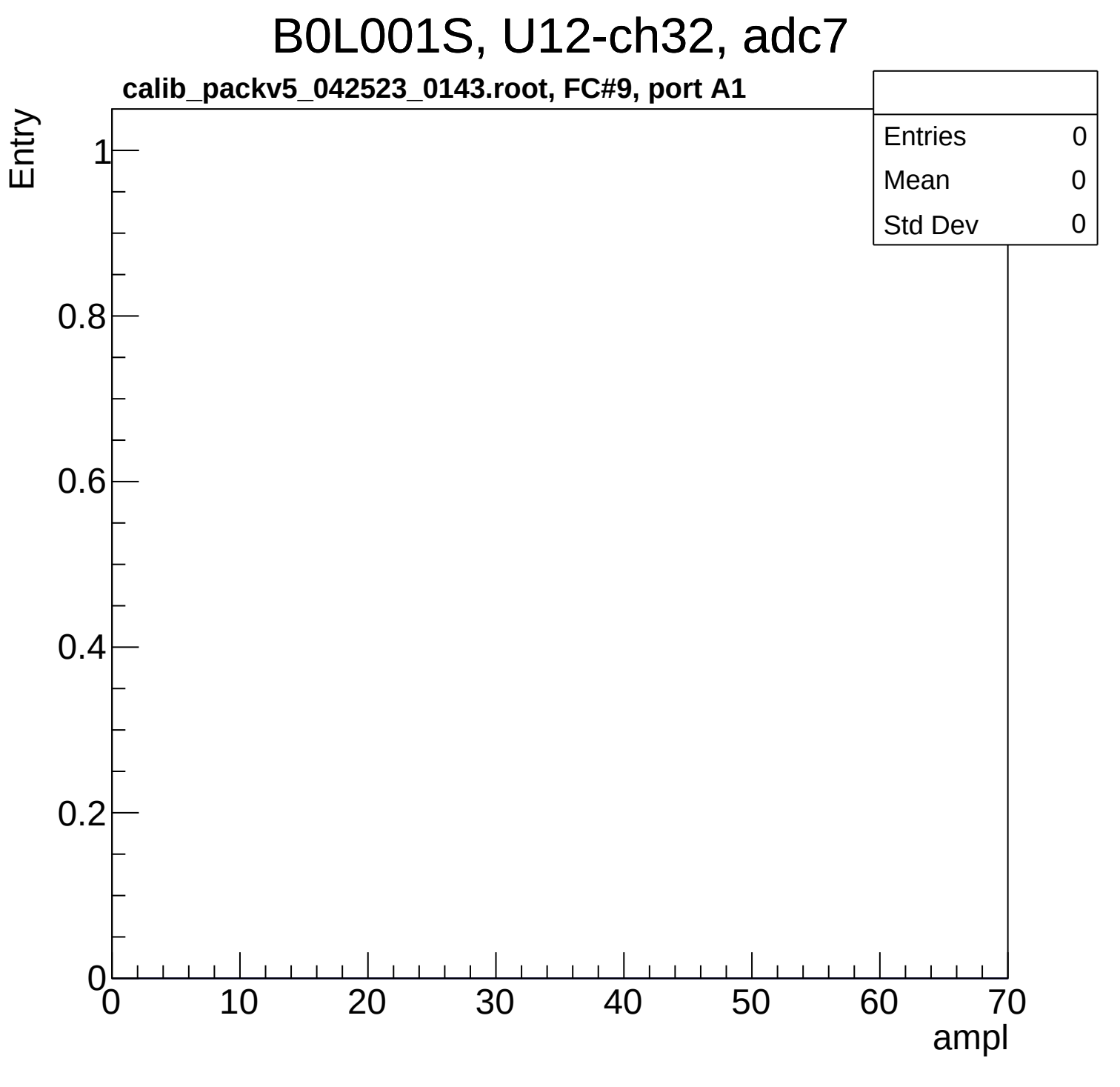
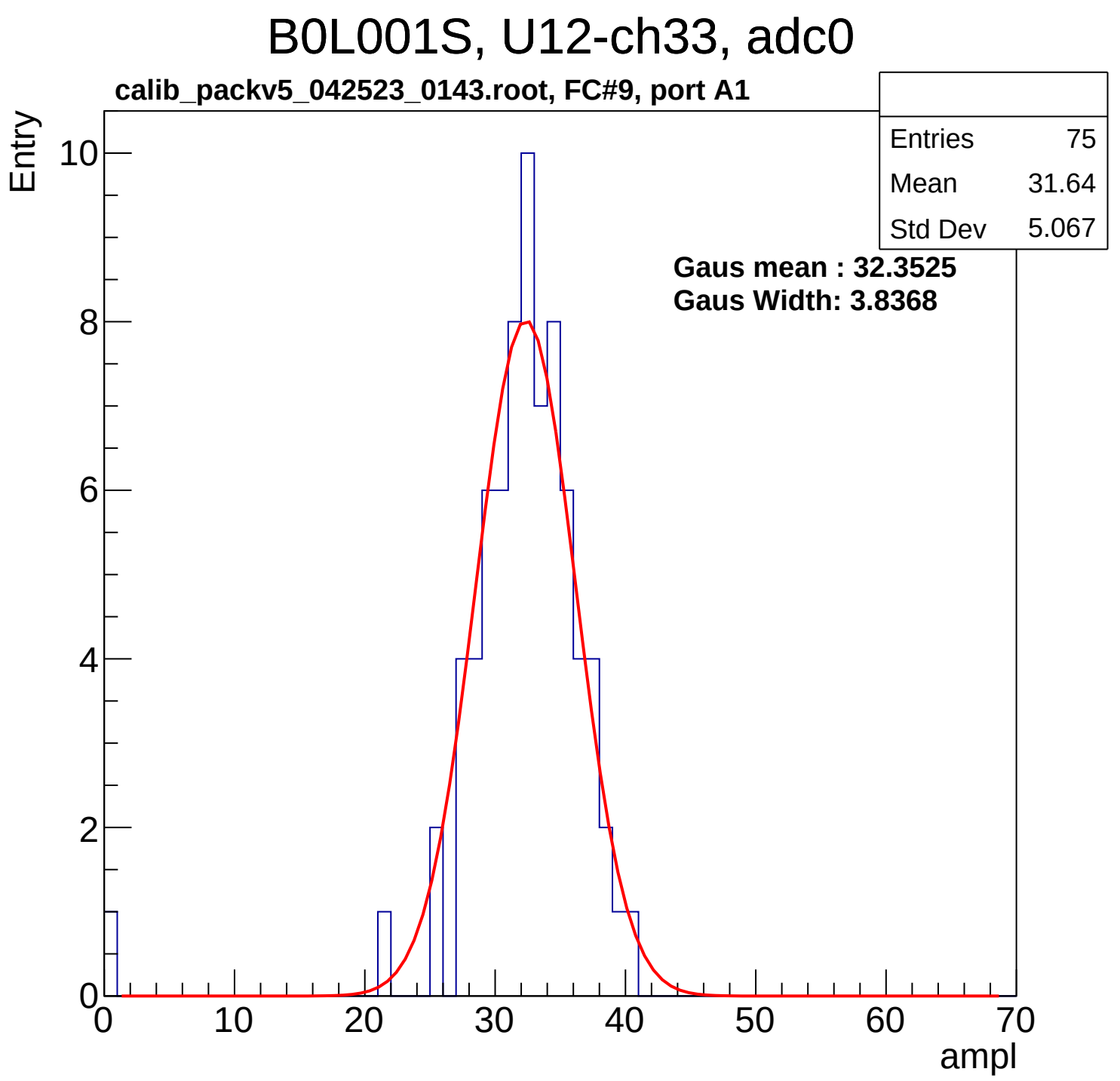
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch32, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 61
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch32, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch33, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 75
Mean 31.64
Std Dev 5.067
Gaus mean : 32.3525
Gaus Width: 3.8368
Entry
ampl
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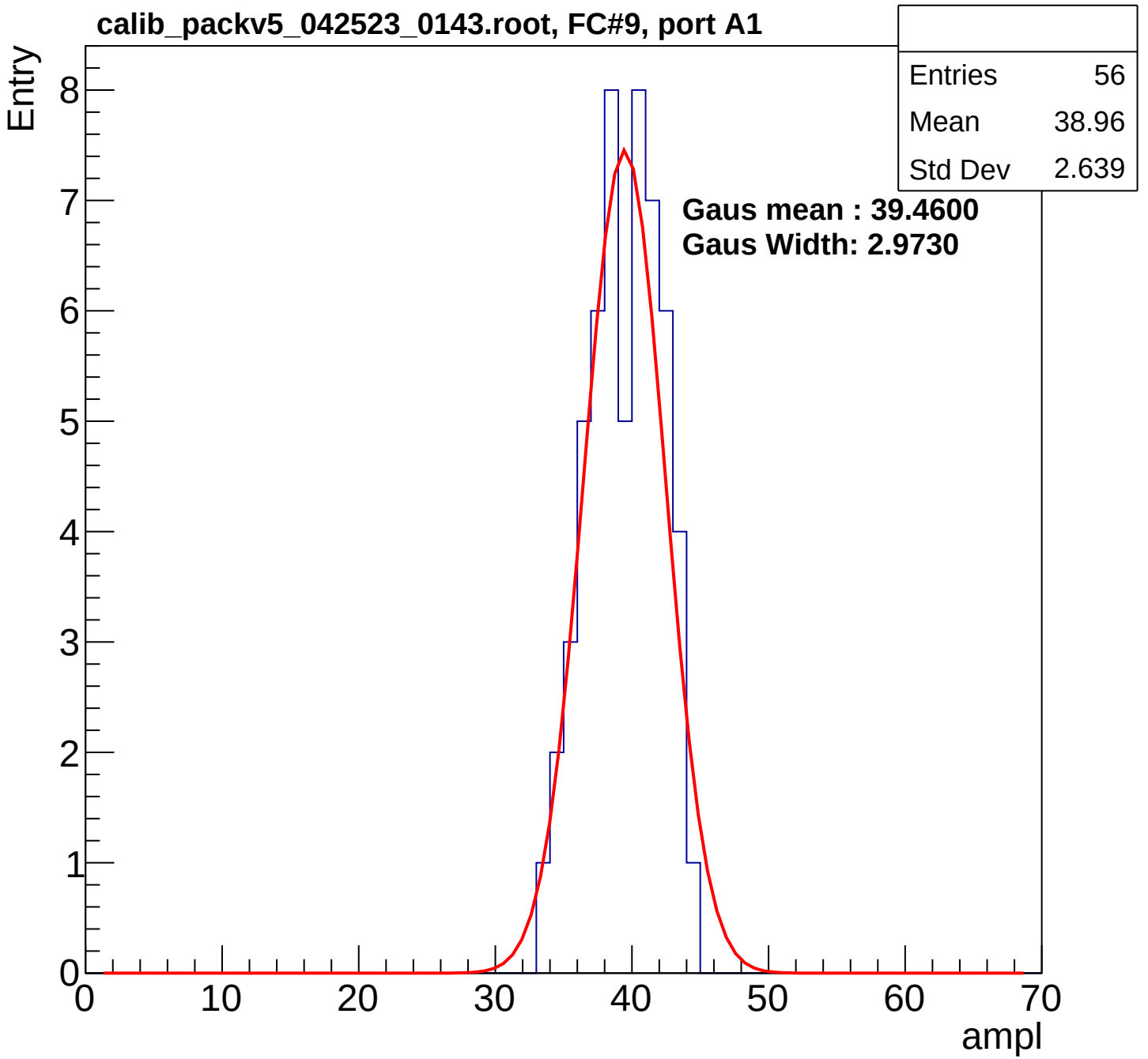
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch33, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 56
Mean 38.96
Std Dev 2.639
Gaus mean : 39.4600
Gaus Width: 2.9730
Entry
ampl
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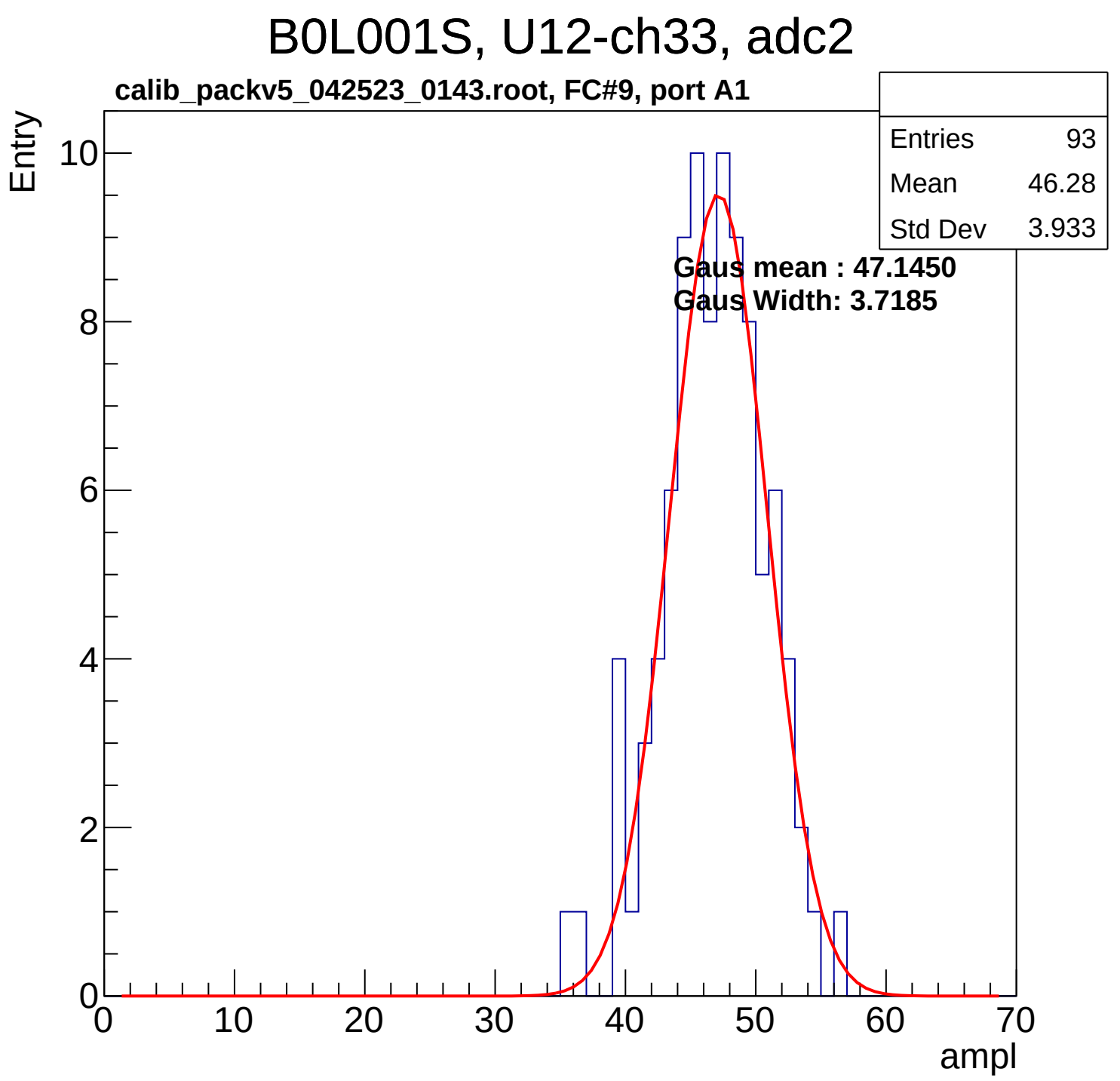
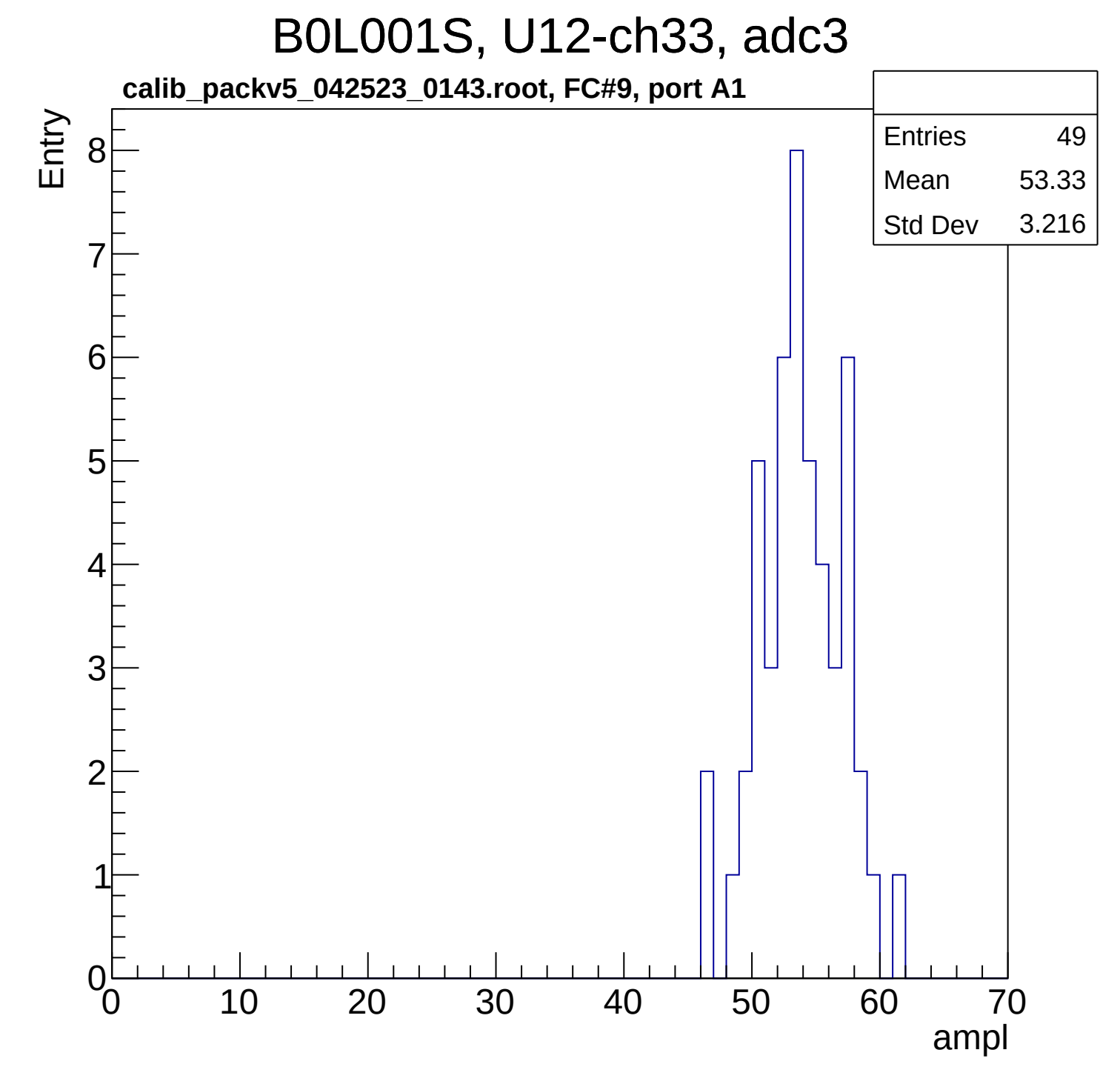
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch33, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 93
Mean 46.28
Std Dev 3.933
Gaus mean : 47.1450
Gaus Width: 3.7185
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch33, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 49
Mean 53.33
Std Dev 3.216
Entry
ampl
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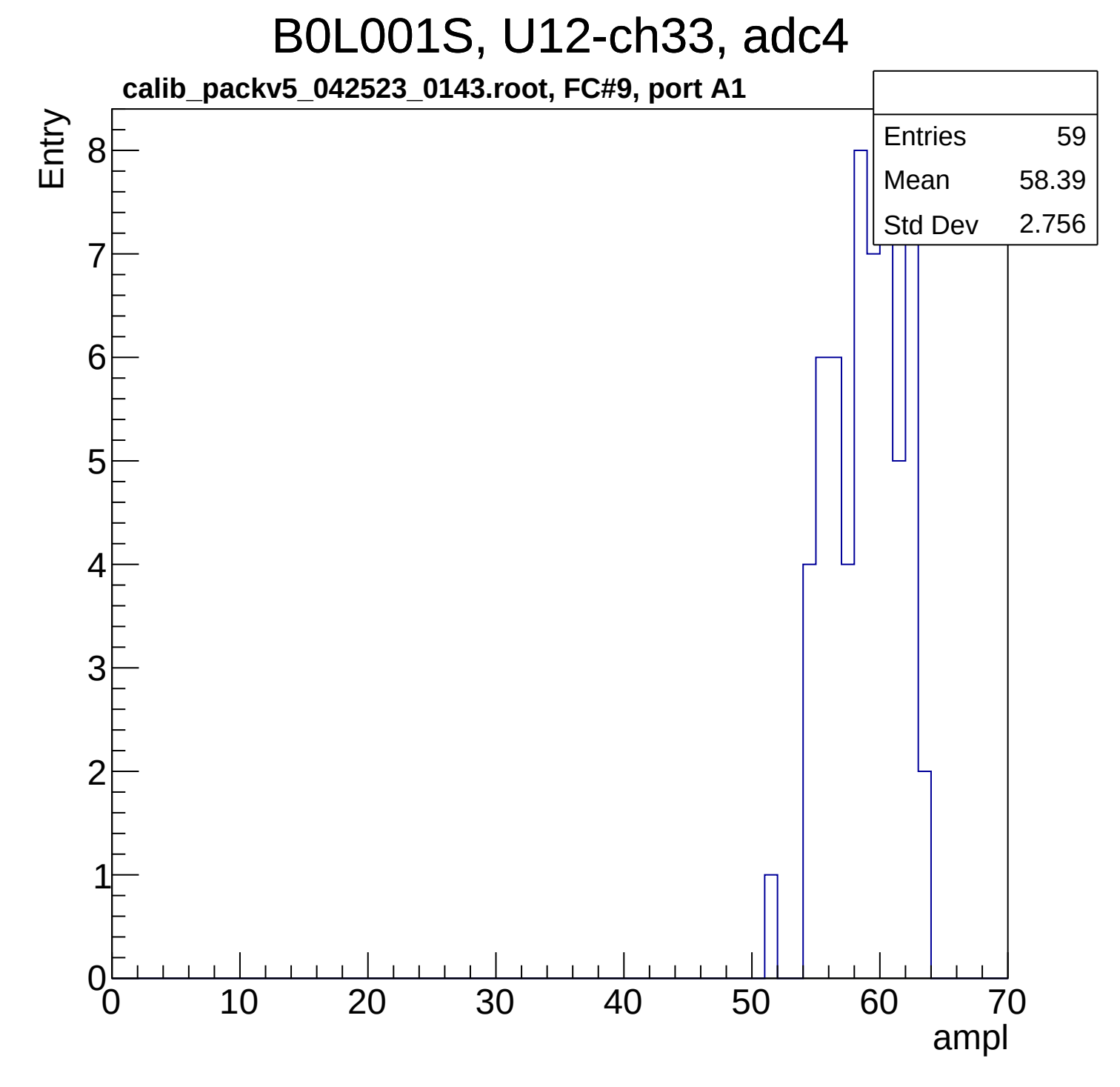
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch33, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 59
Mean 58.39
Std Dev 2.756
Entry
ampl
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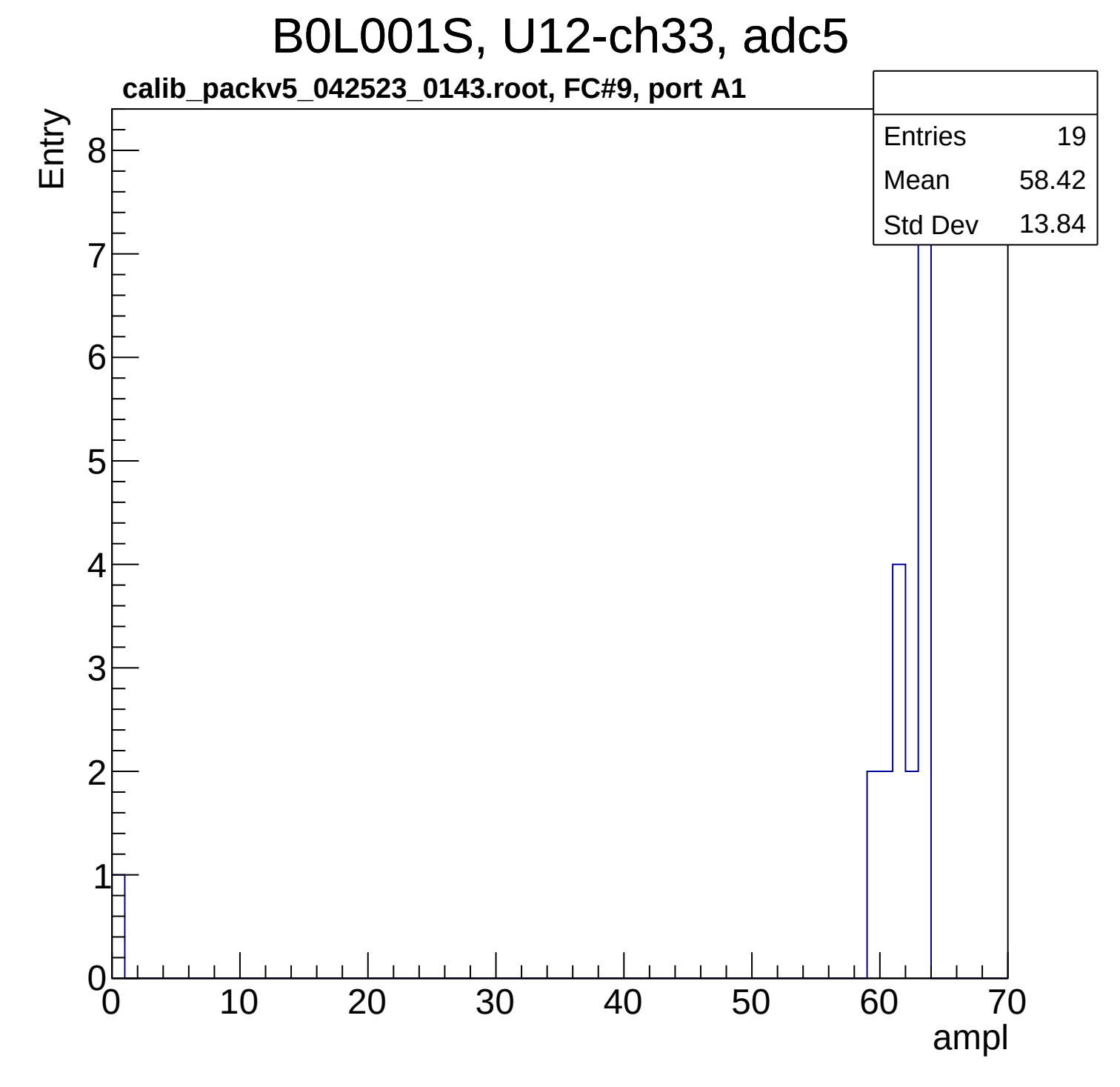
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch33, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 19
Mean 58.42
Std Dev 13.84
Entry
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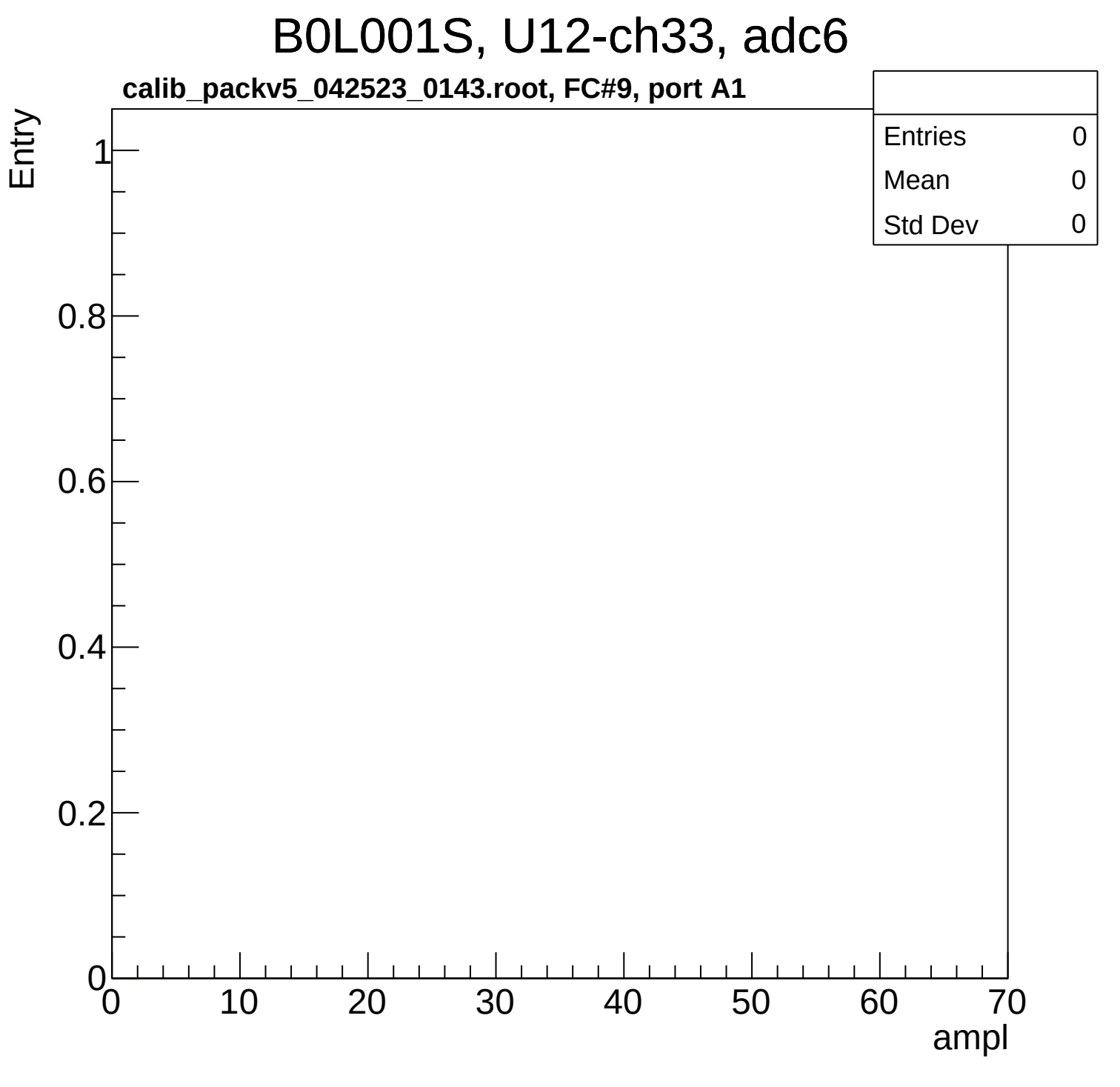
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch33, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
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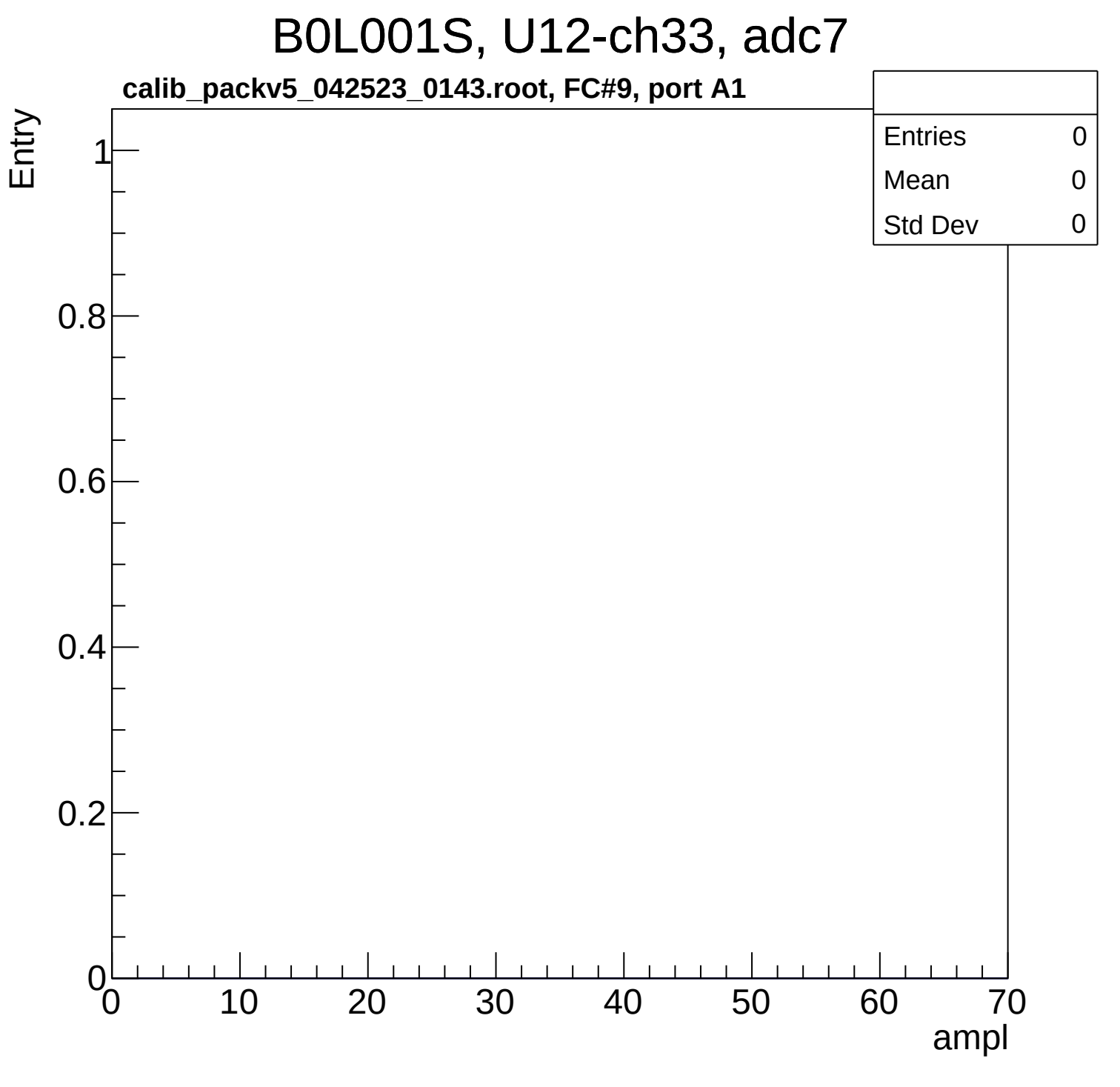
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch33, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
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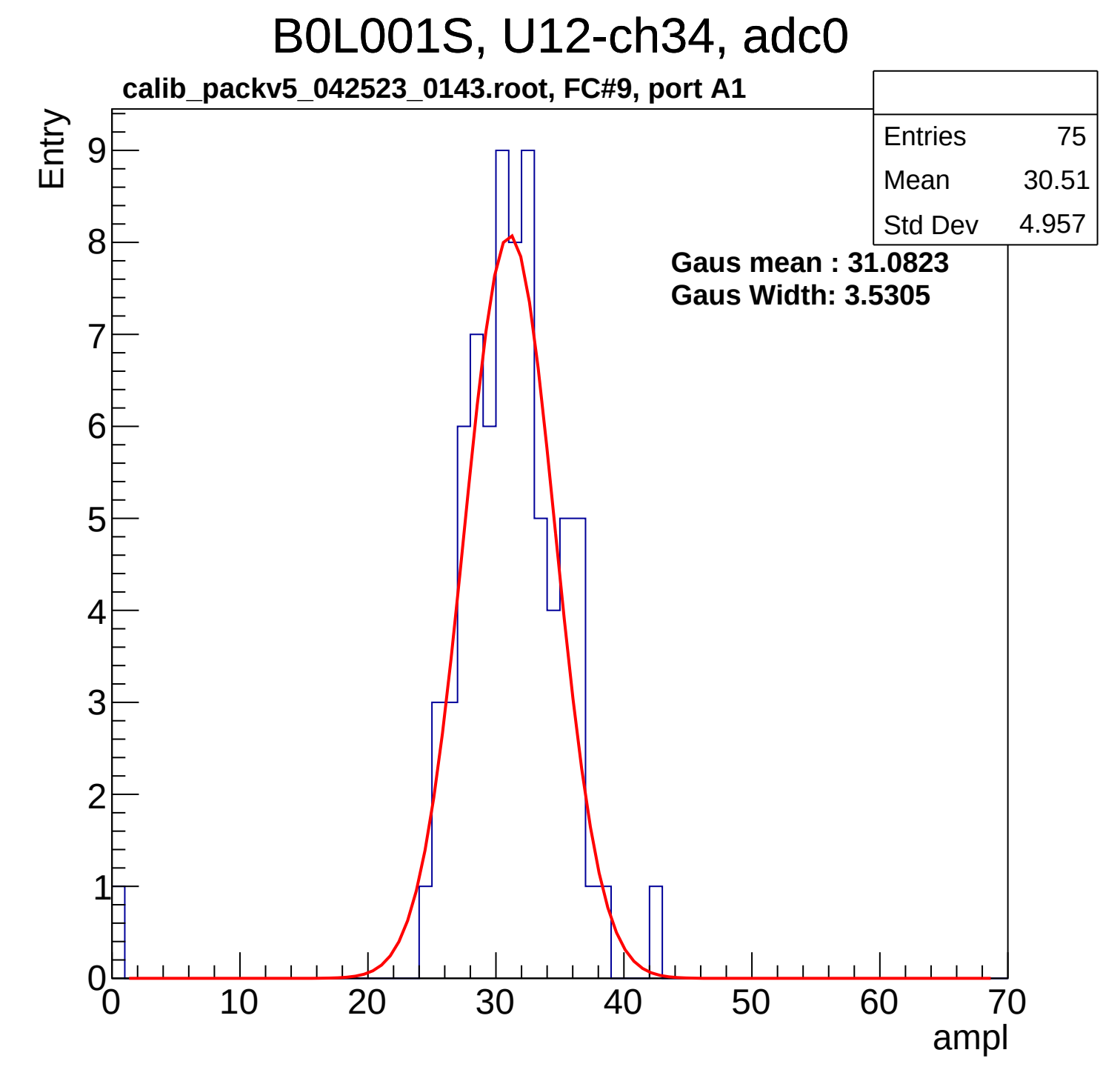
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch34, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 75
Mean 30.51
Std Dev 4.957
Gaus mean : 31.0823
Gaus Width: 3.5305
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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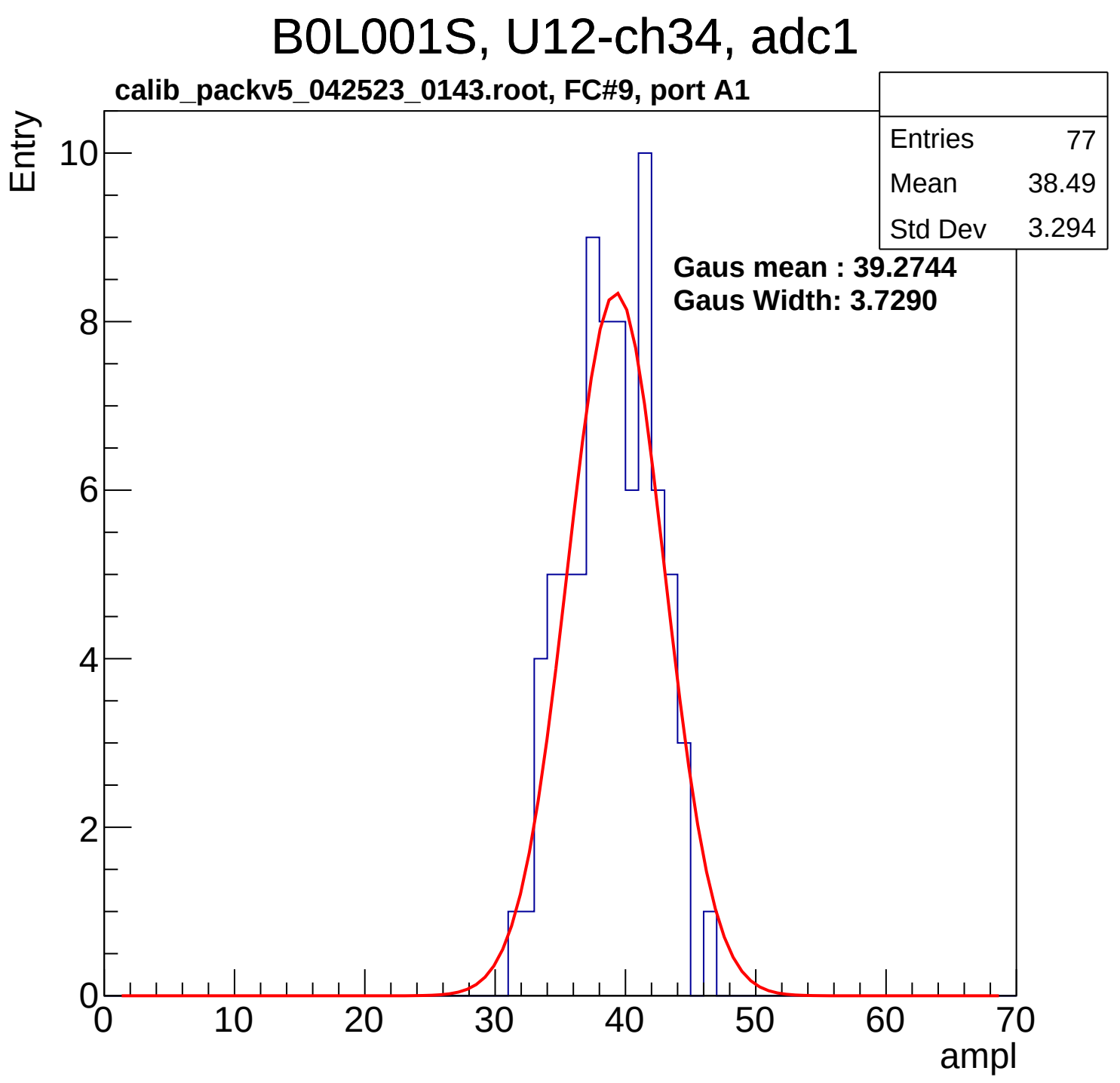
B0L001S, U12-ch34, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 77
Mean 38.49
Std Dev 3.294
Gaus mean : 39.2744
Gaus Width: 3.7290
Entry
ampl
0
2
4
6
8
10
0
10
20
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60
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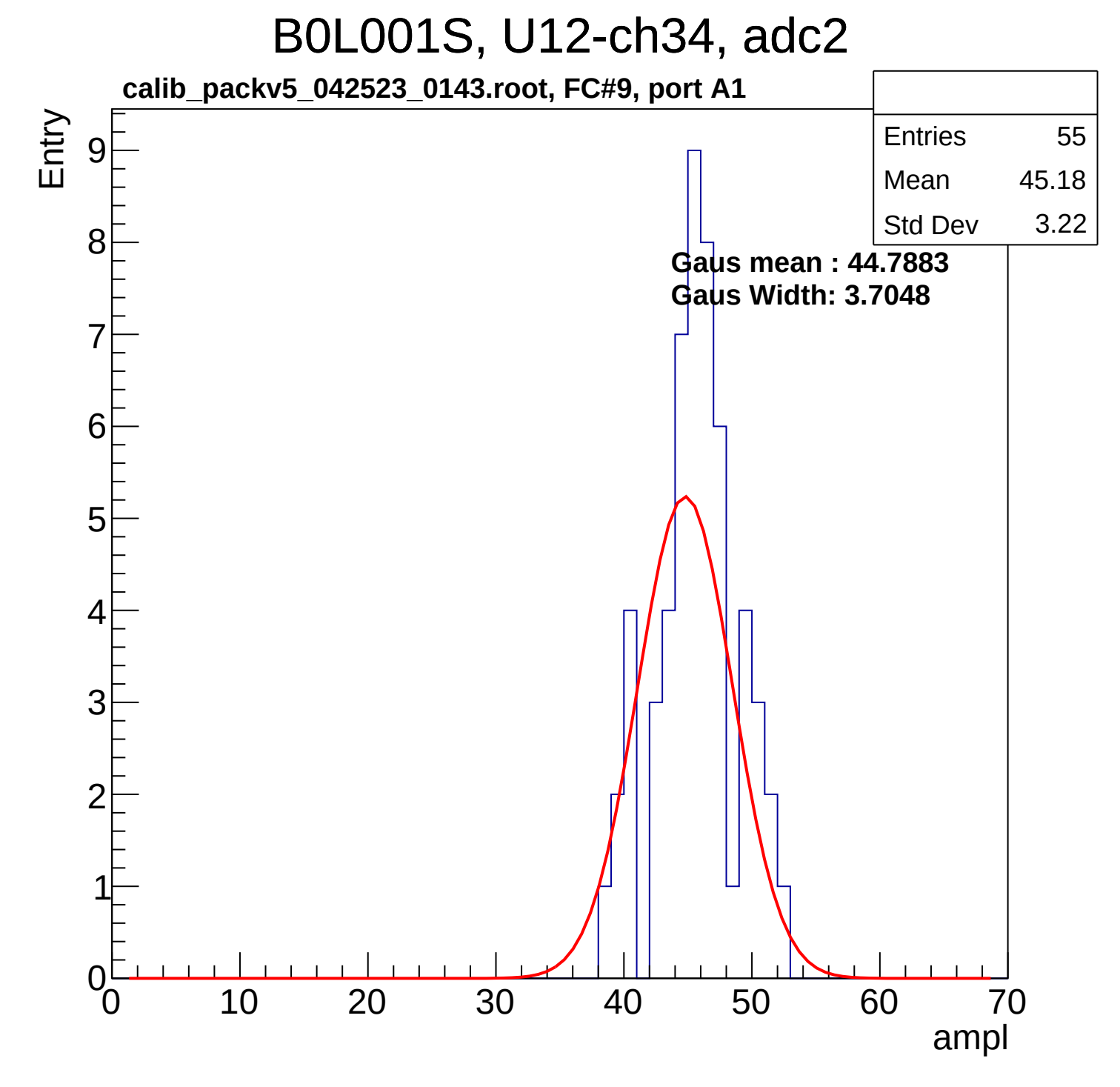
B0L001S, U12-ch34, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 55
Mean 45.18
Std Dev 3.22
Gaus mean : 44.7883
Gaus Width: 3.7048
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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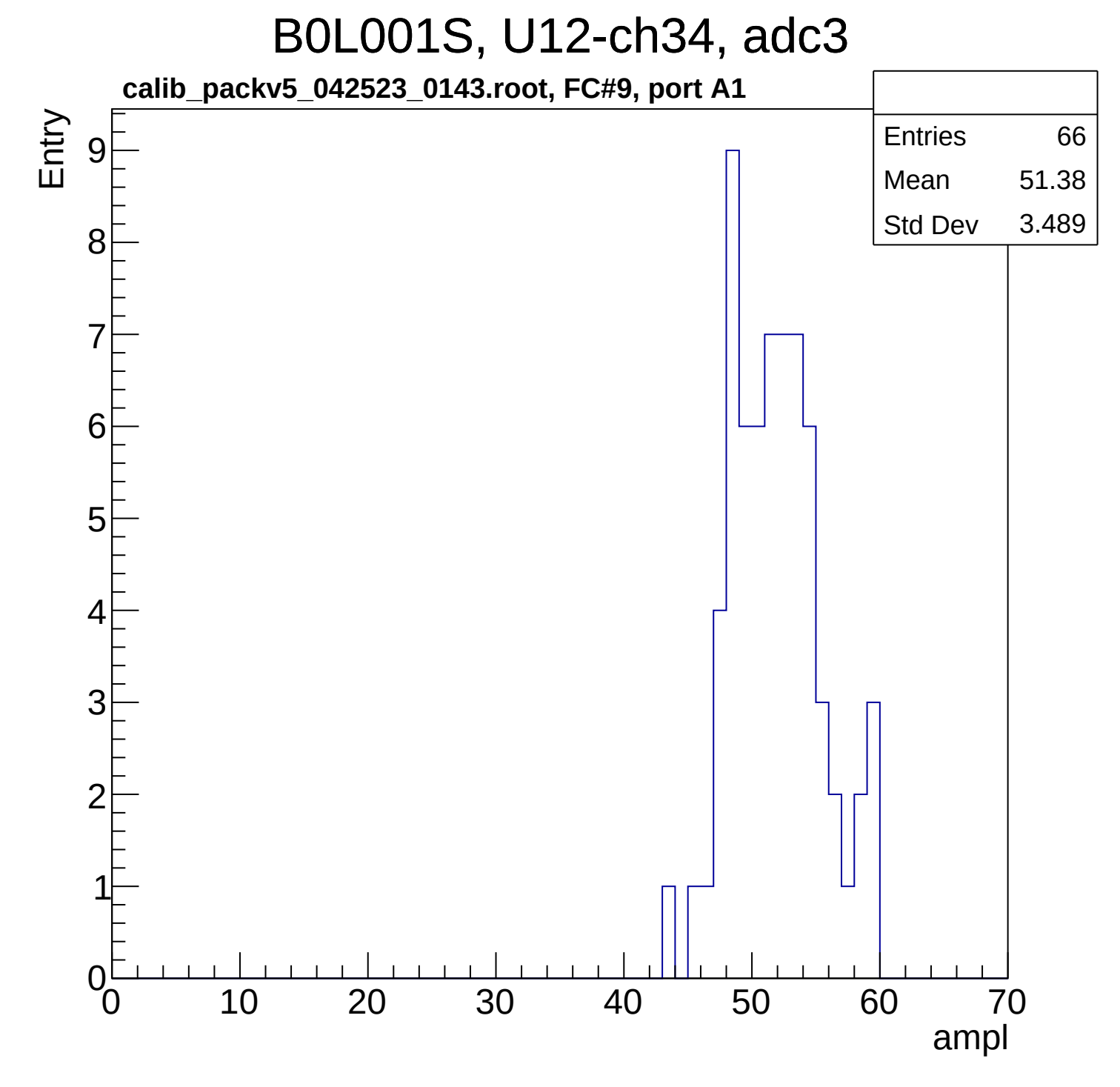
B0L001S, U12-ch34, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 66
Mean 51.38
Std Dev 3.489
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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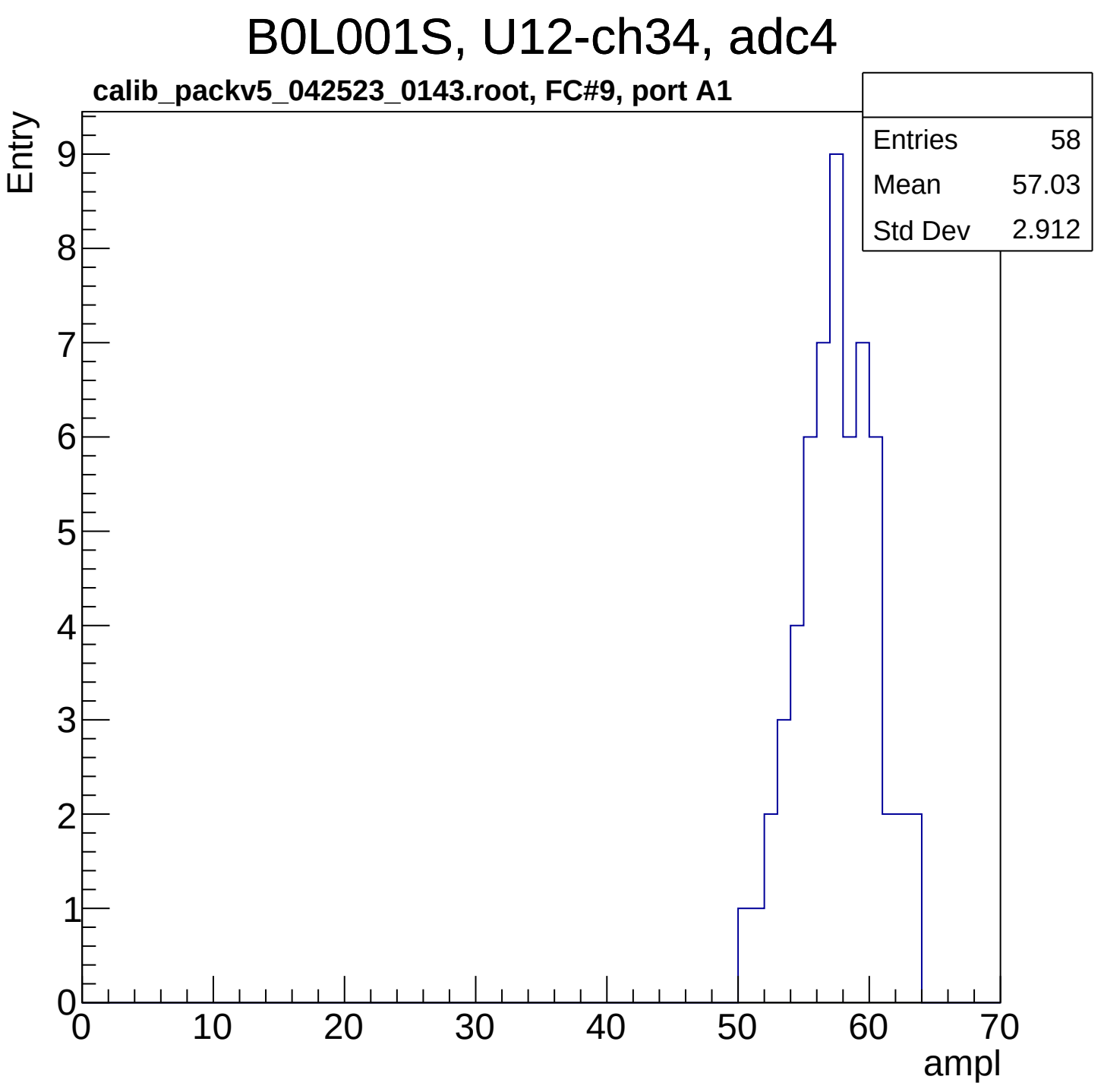
B0L001S, U12-ch34, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 58
Mean 57.03
Std Dev 2.912
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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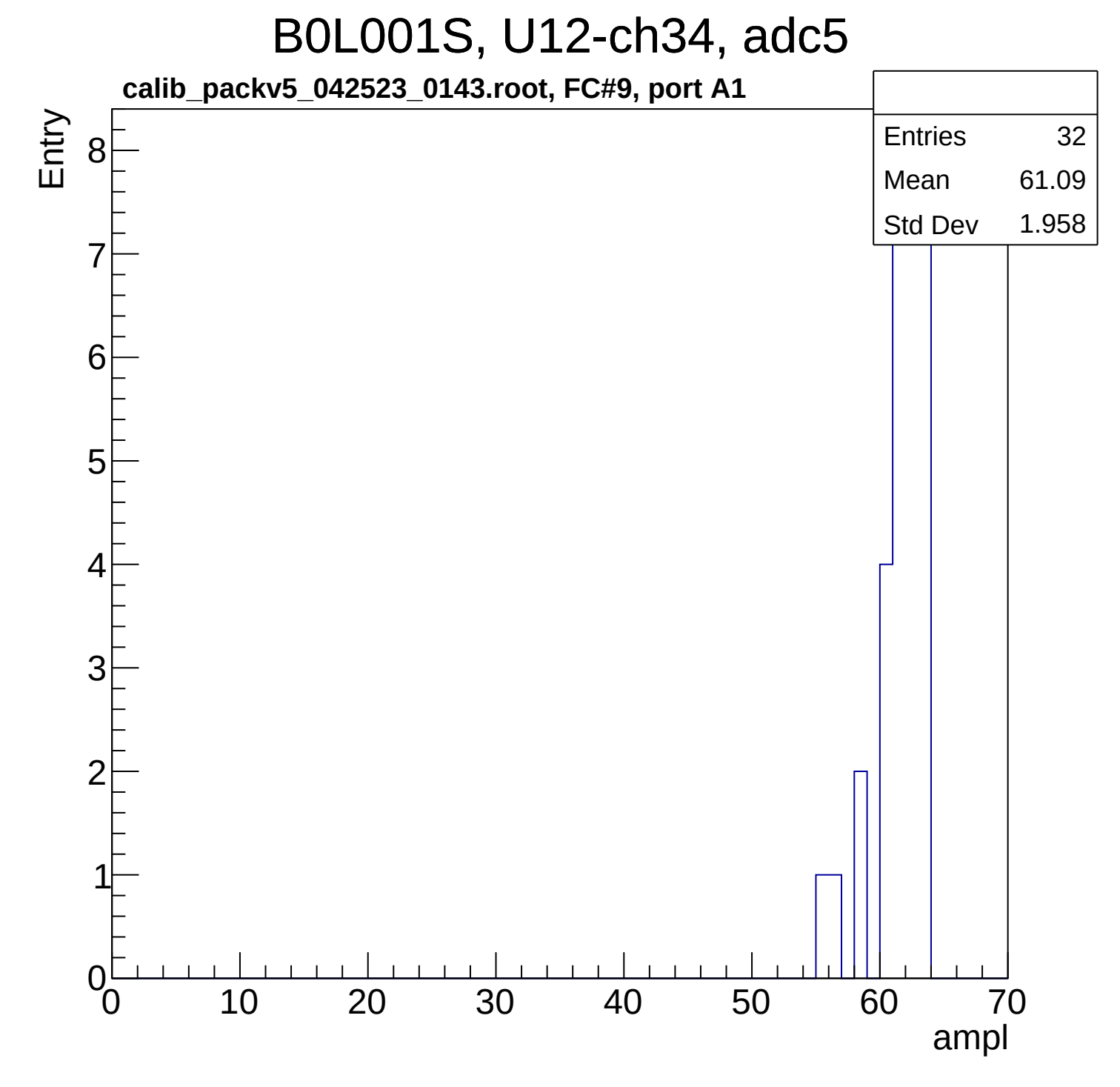
40
50
60
70


B0L001S, U12-ch34, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 32
Mean 61.09
Std Dev 1.958
Entry
ampl
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1
2
3
4
5
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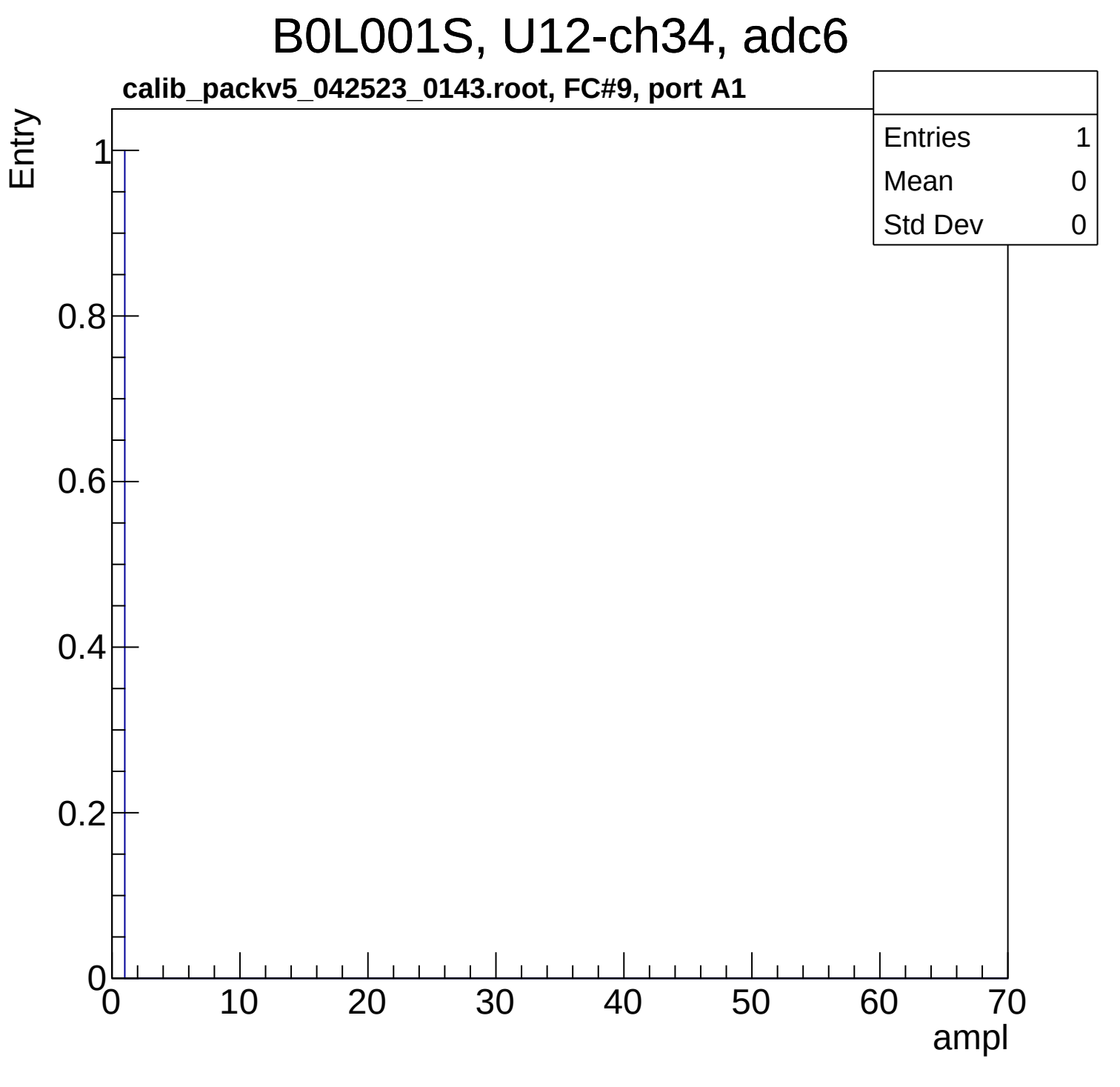
B0L001S, U12-ch34, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
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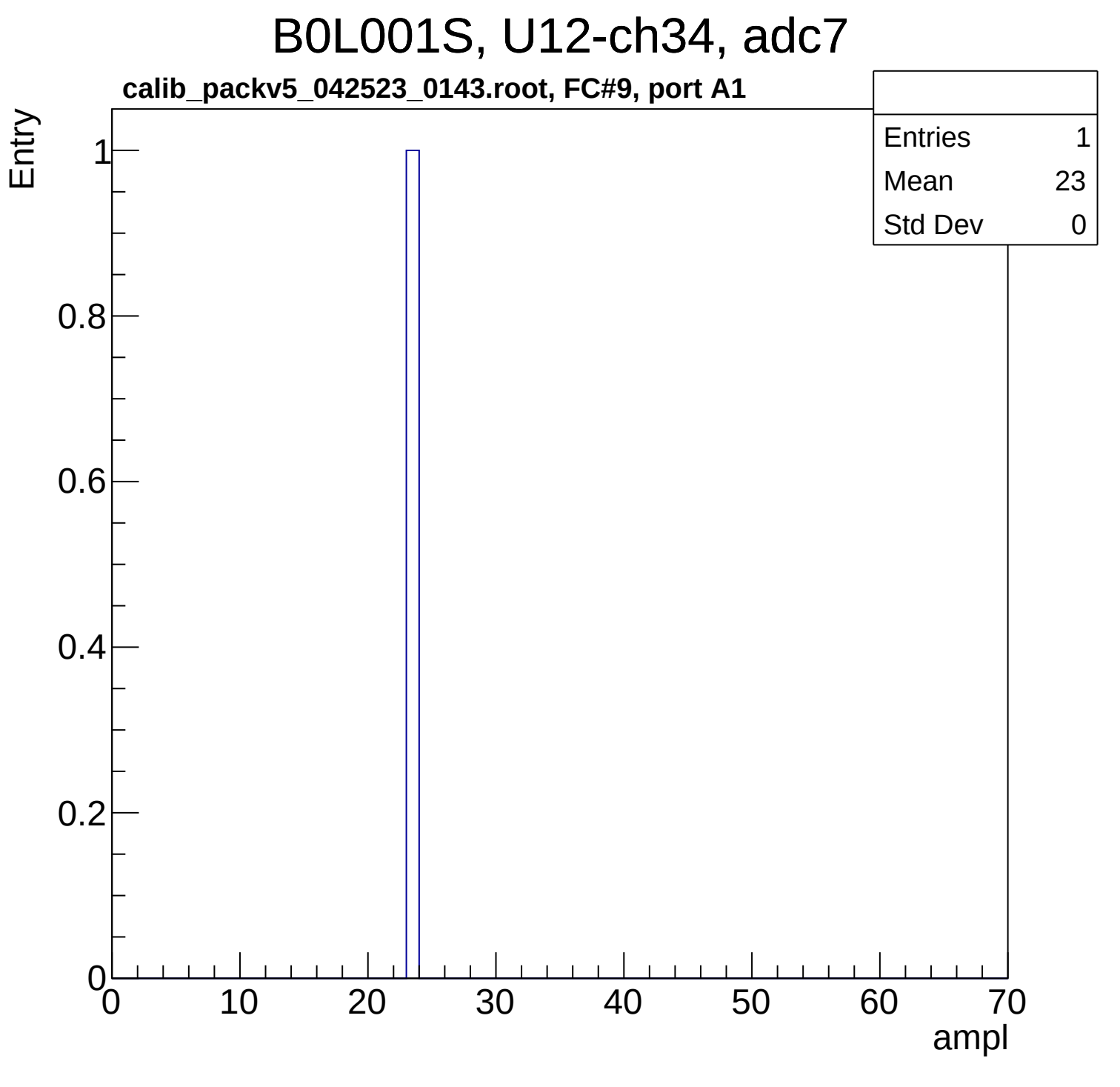
40
50
60
70
ampl


B0L001S, U12-ch34, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 23
Std Dev 0
Entry
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0.8
0.6
0.4
0.2
0
0
10
20
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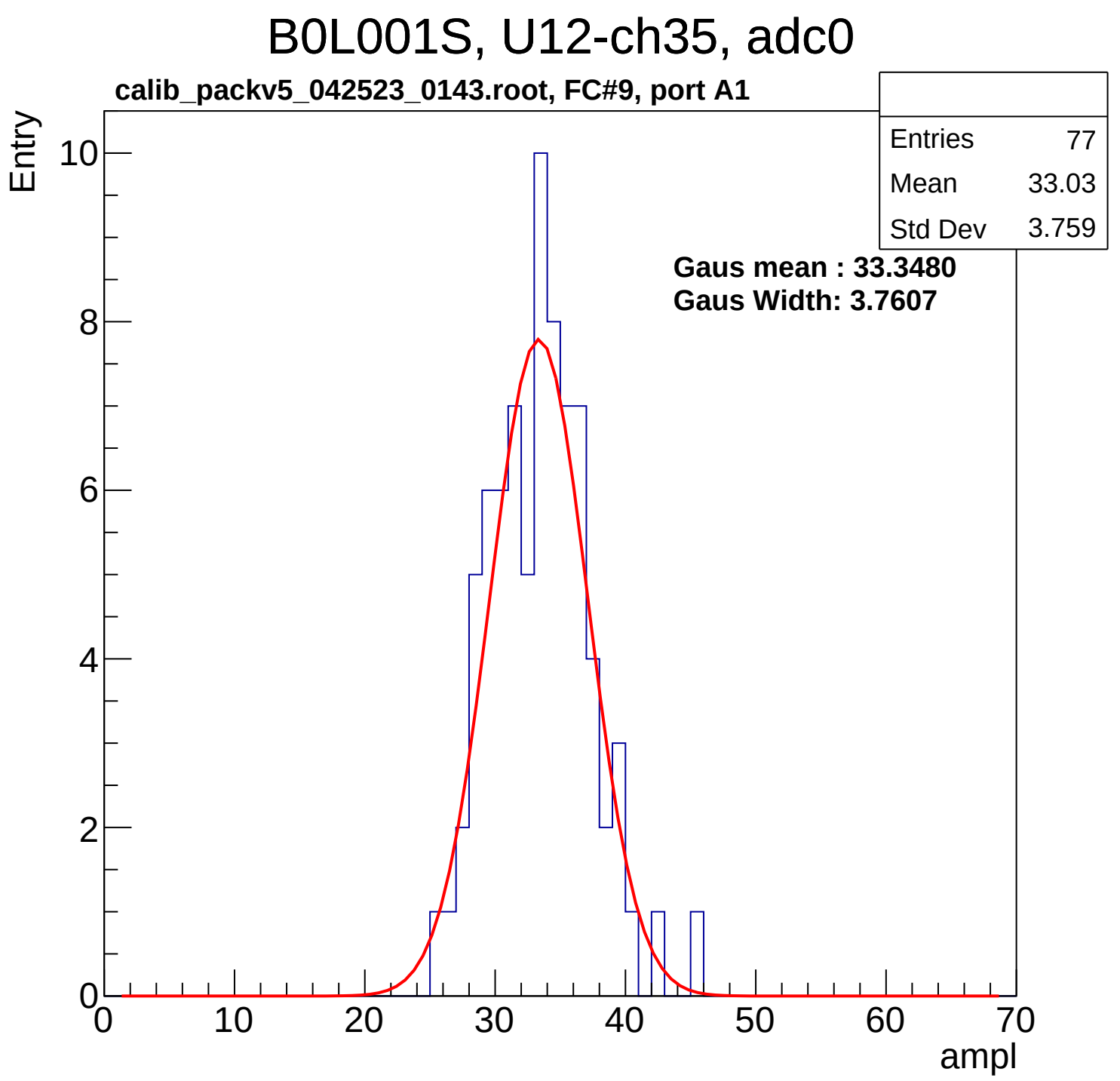
40
50
60
70
ampl


B0L001S, U12-ch35, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 77
Mean 33.03
Std Dev 3.759
Gaus mean : 33.3480
Gaus Width: 3.7607
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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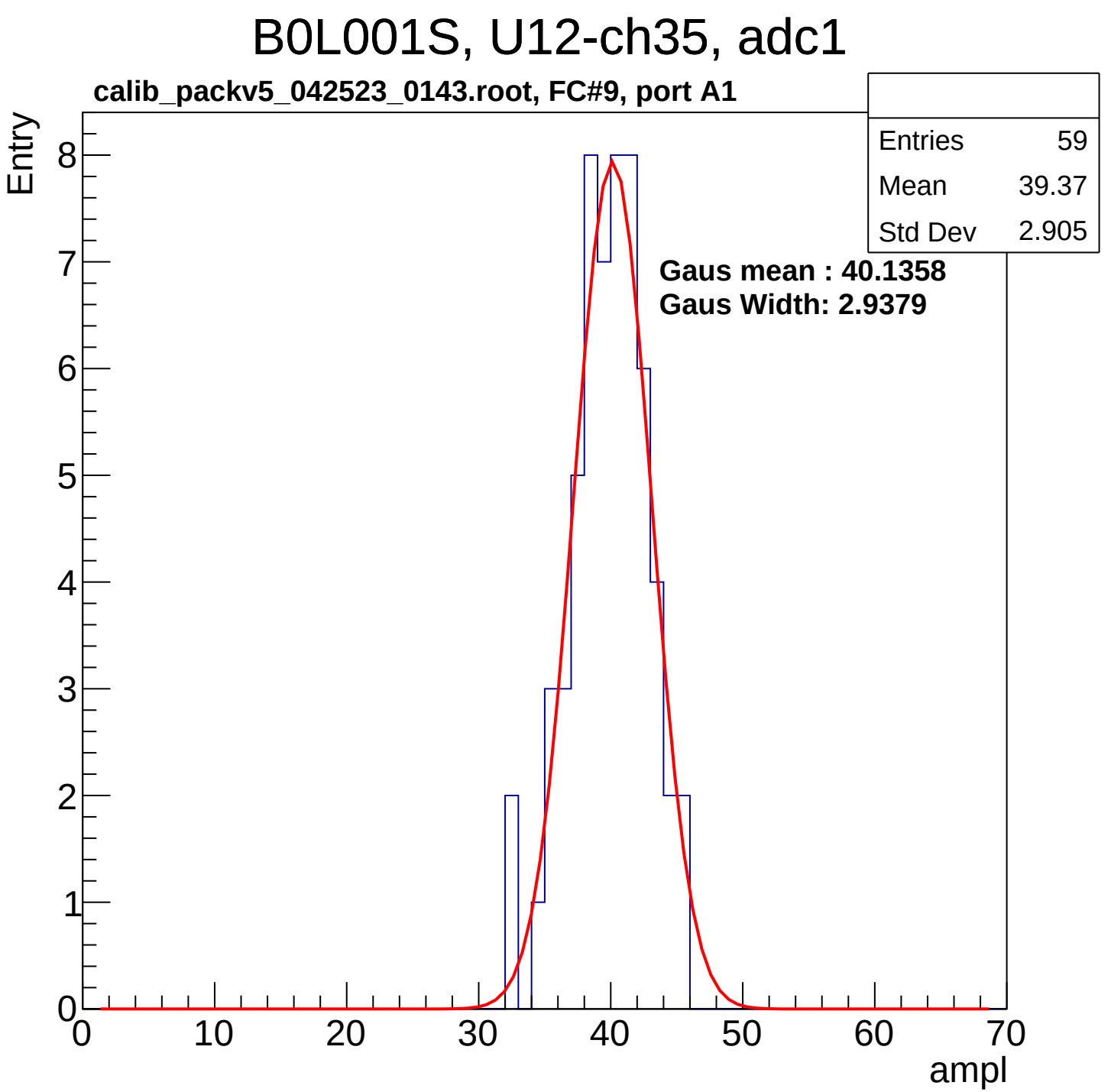
B0L001S, U12-ch35, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 59
Mean 39.37
Std Dev 2.905
Gaus mean : 40.1358
Gaus Width: 2.9379
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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20
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40
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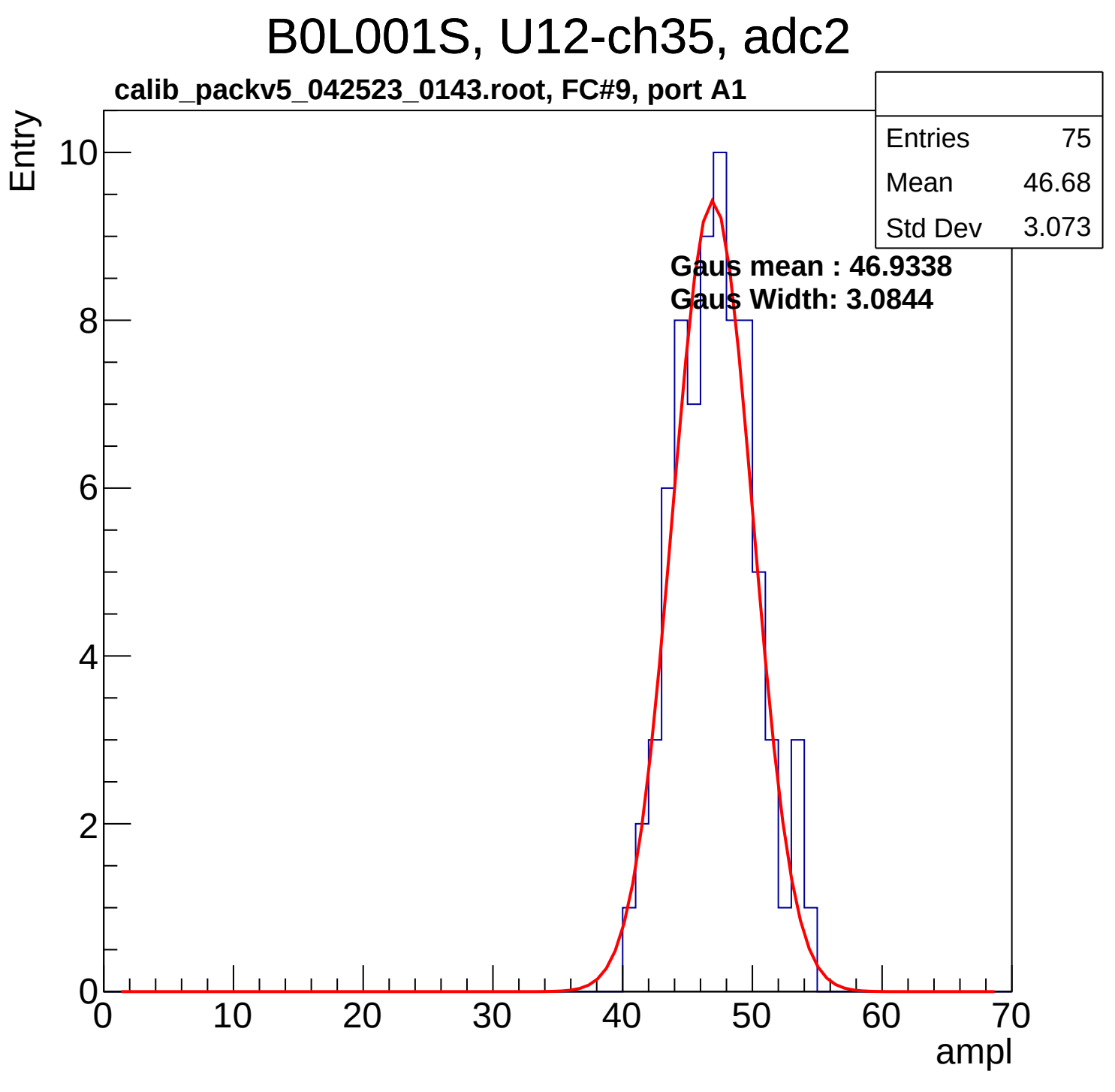
B0L001S, U12-ch35, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 75
Mean 46.68
Std Dev 3.073
Gaus mean : 46.9338
Gaus Width: 3.0844
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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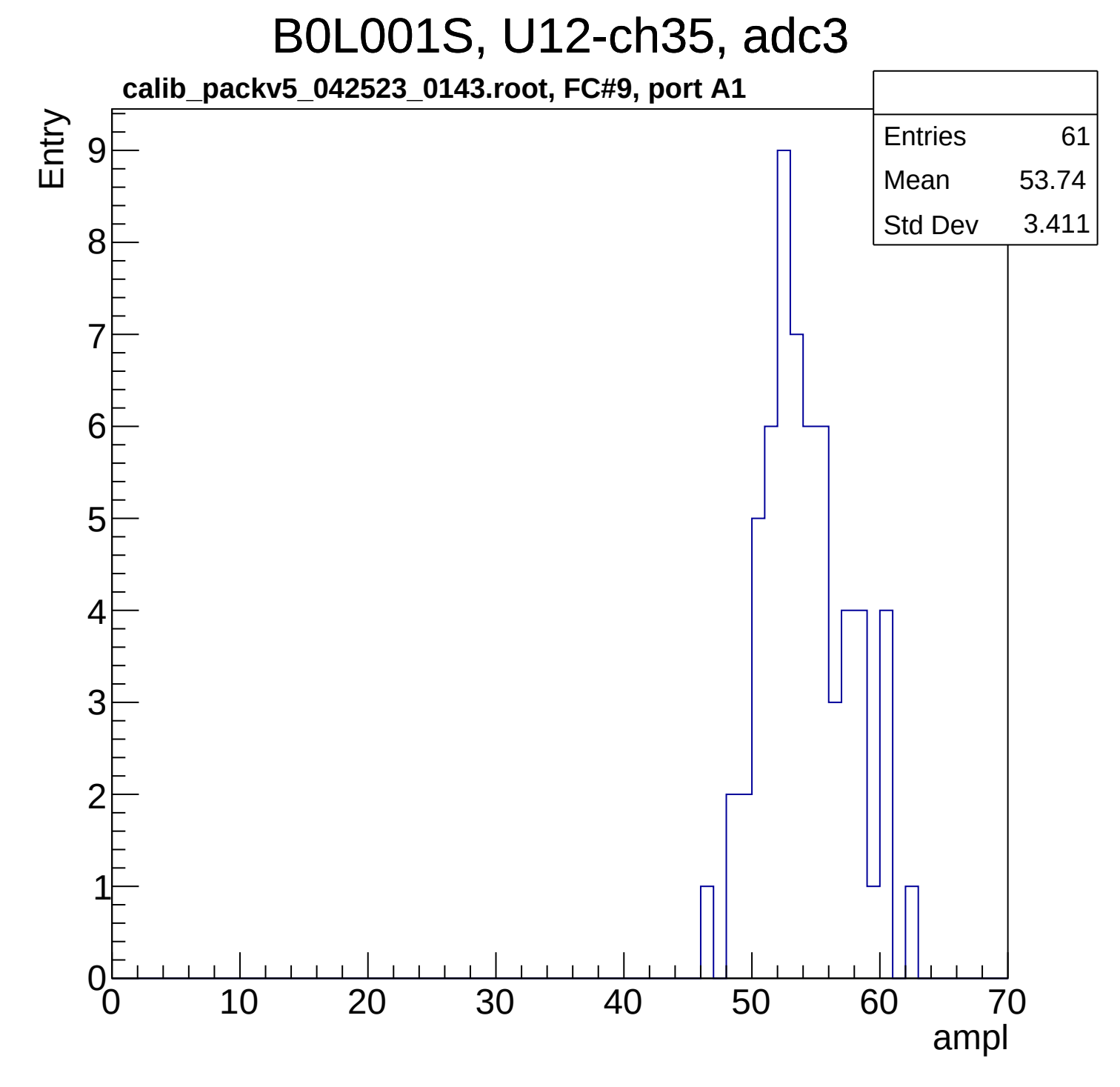
B0L001S, U12-ch35, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 61
Mean 53.74
Std Dev 3.411
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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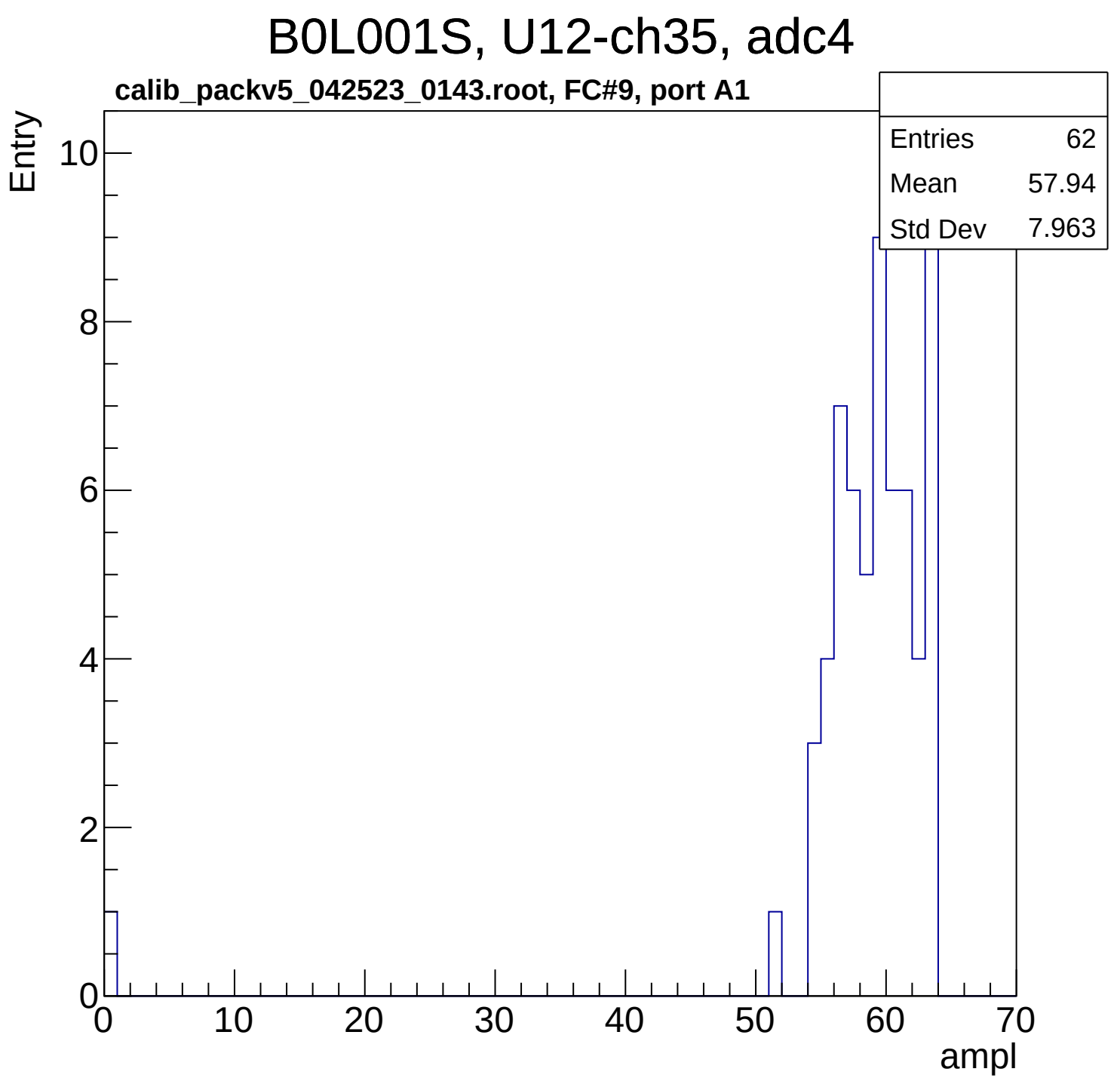
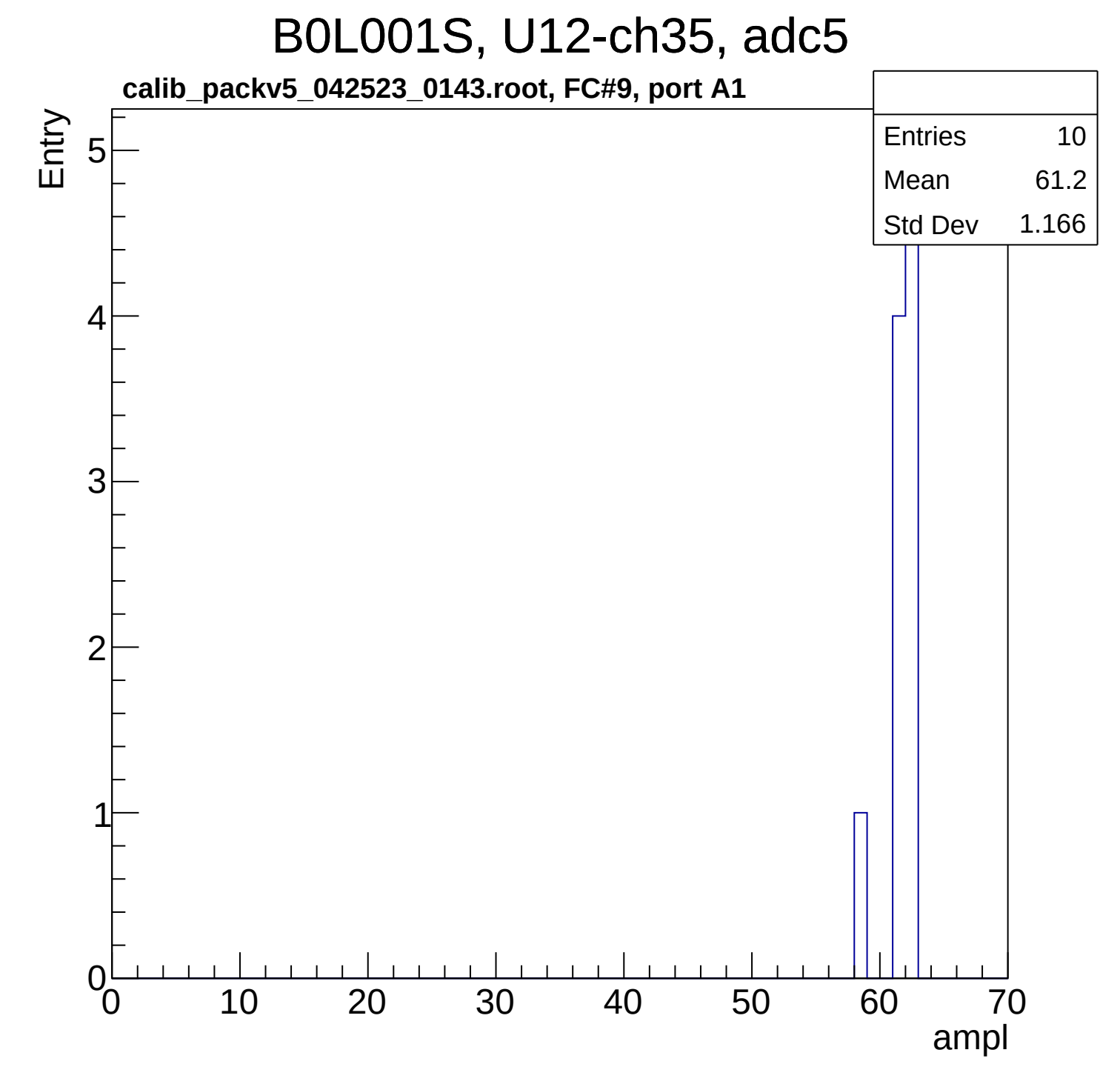
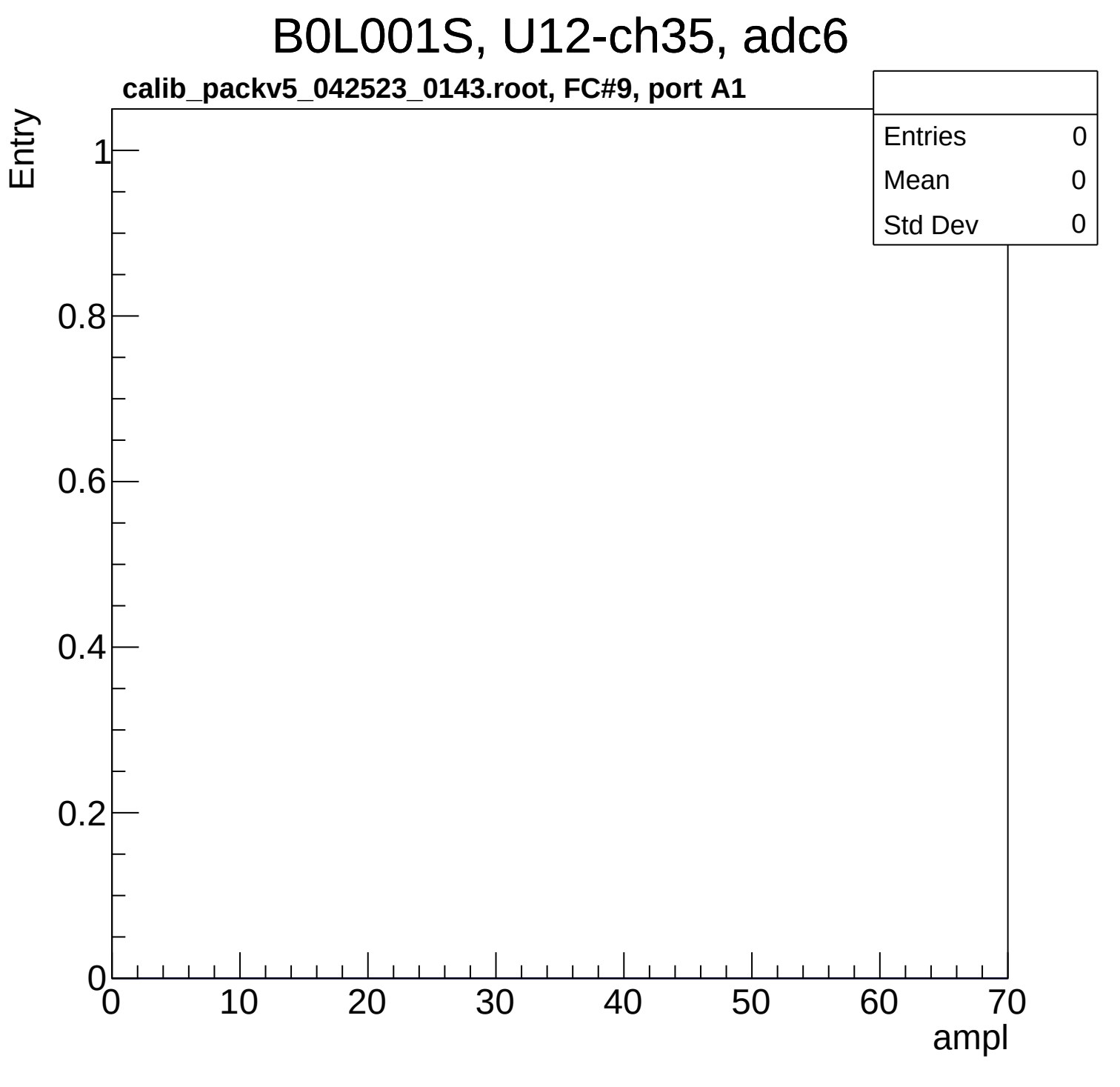
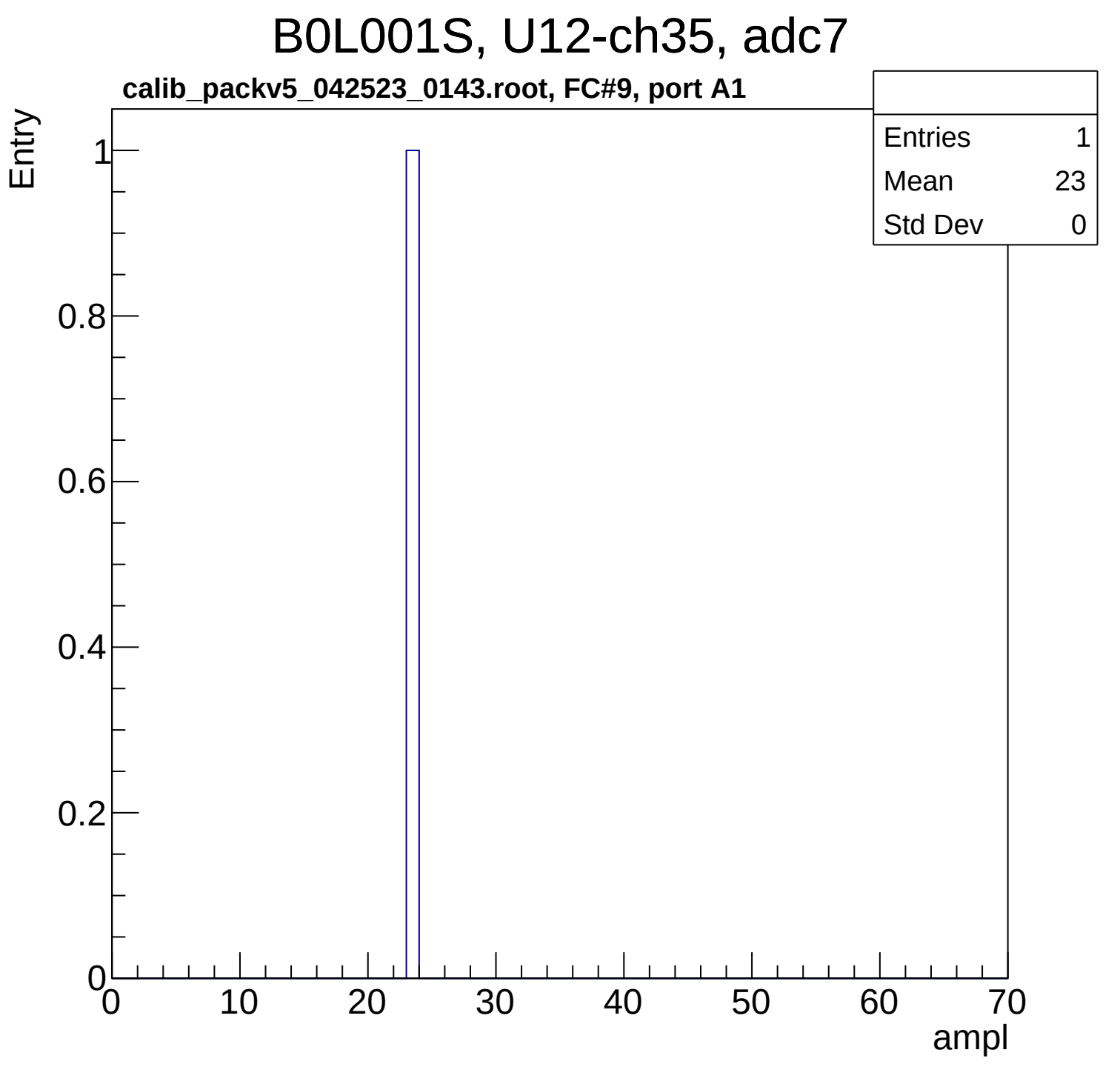

B0L001S, U12-ch35, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 62
Mean 57.94
Std Dev 7.963
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch35, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 10
Mean 61.2
Std Dev 1.166
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch35, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch35, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 23
Std Dev 0
Entry
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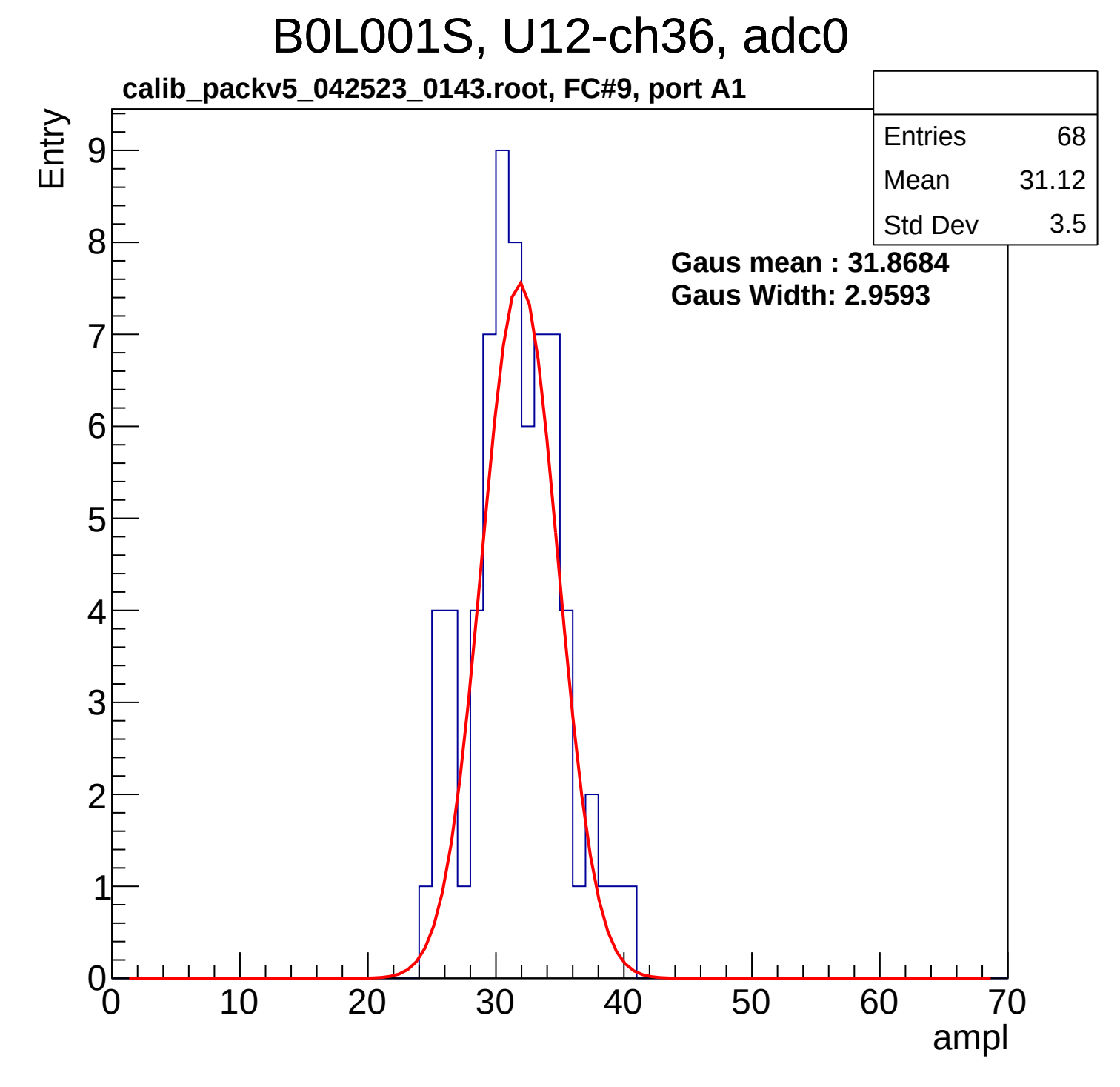
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch36, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 68
Mean 31.12
Std Dev 3.5
Gaus mean : 31.8684
Gaus Width: 2.9593
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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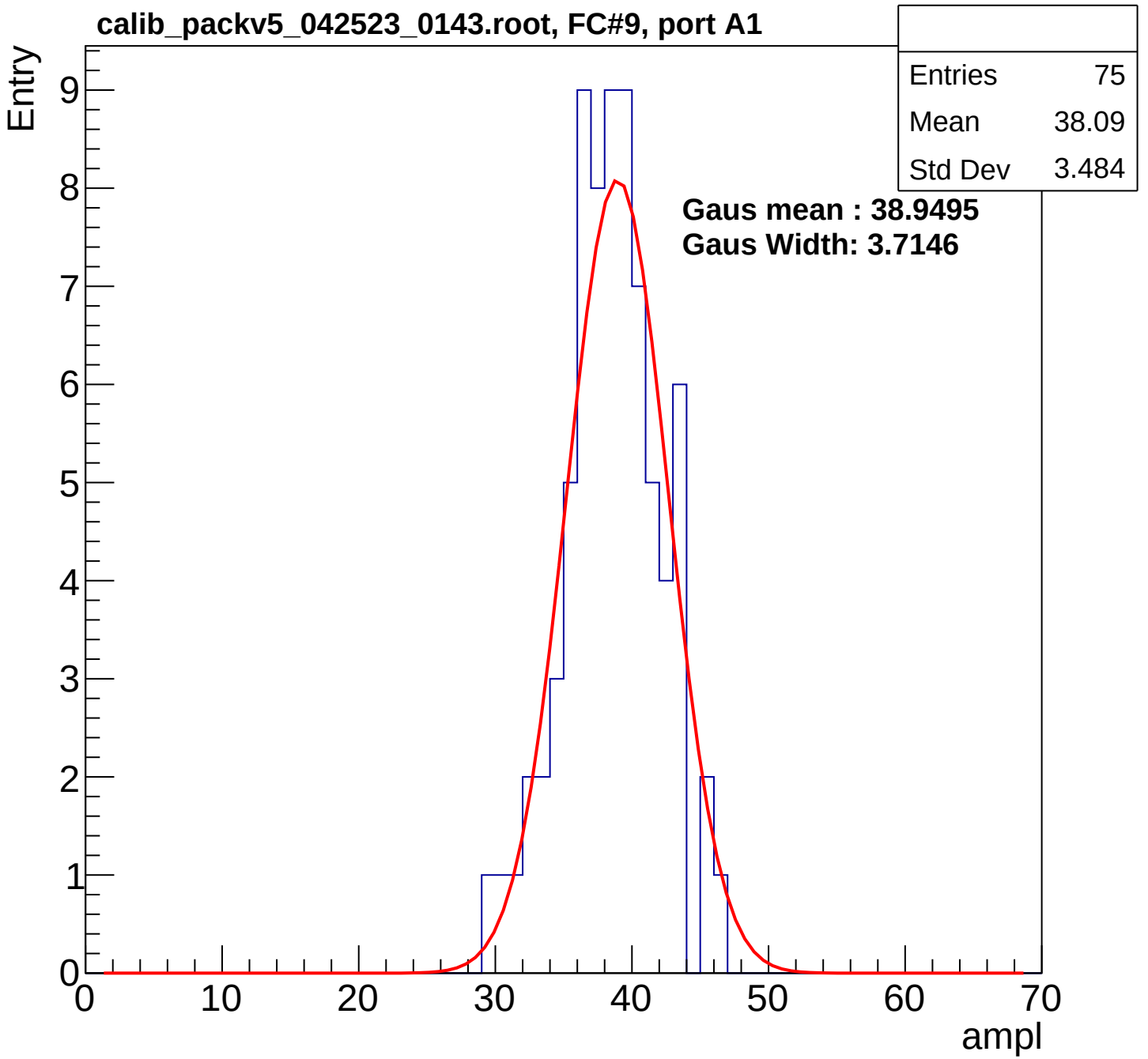
B0L001S, U12-ch36, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 75
Mean 38.09
Std Dev 3.484
Gaus mean : 38.9495
Gaus Width: 3.7146
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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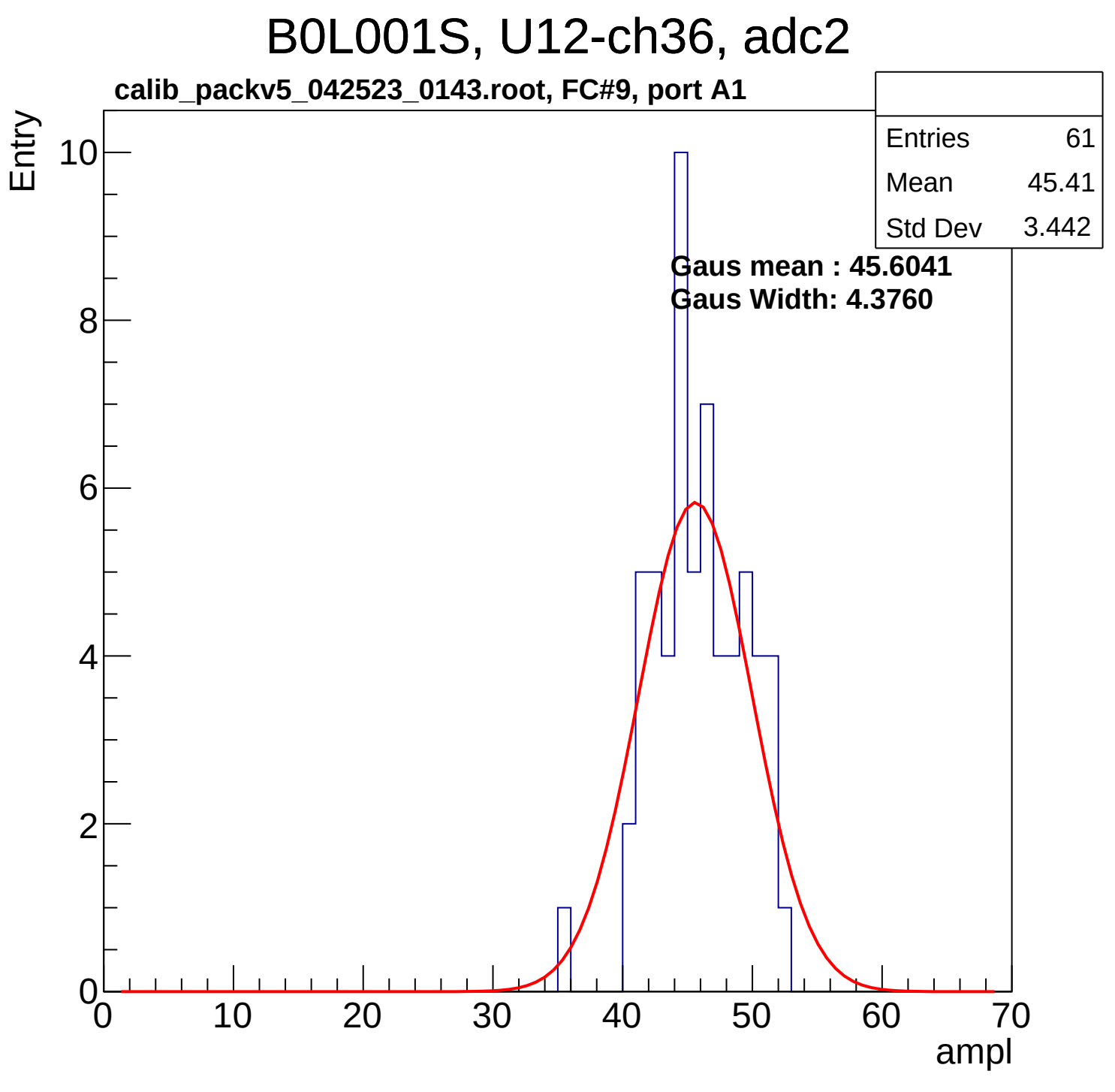
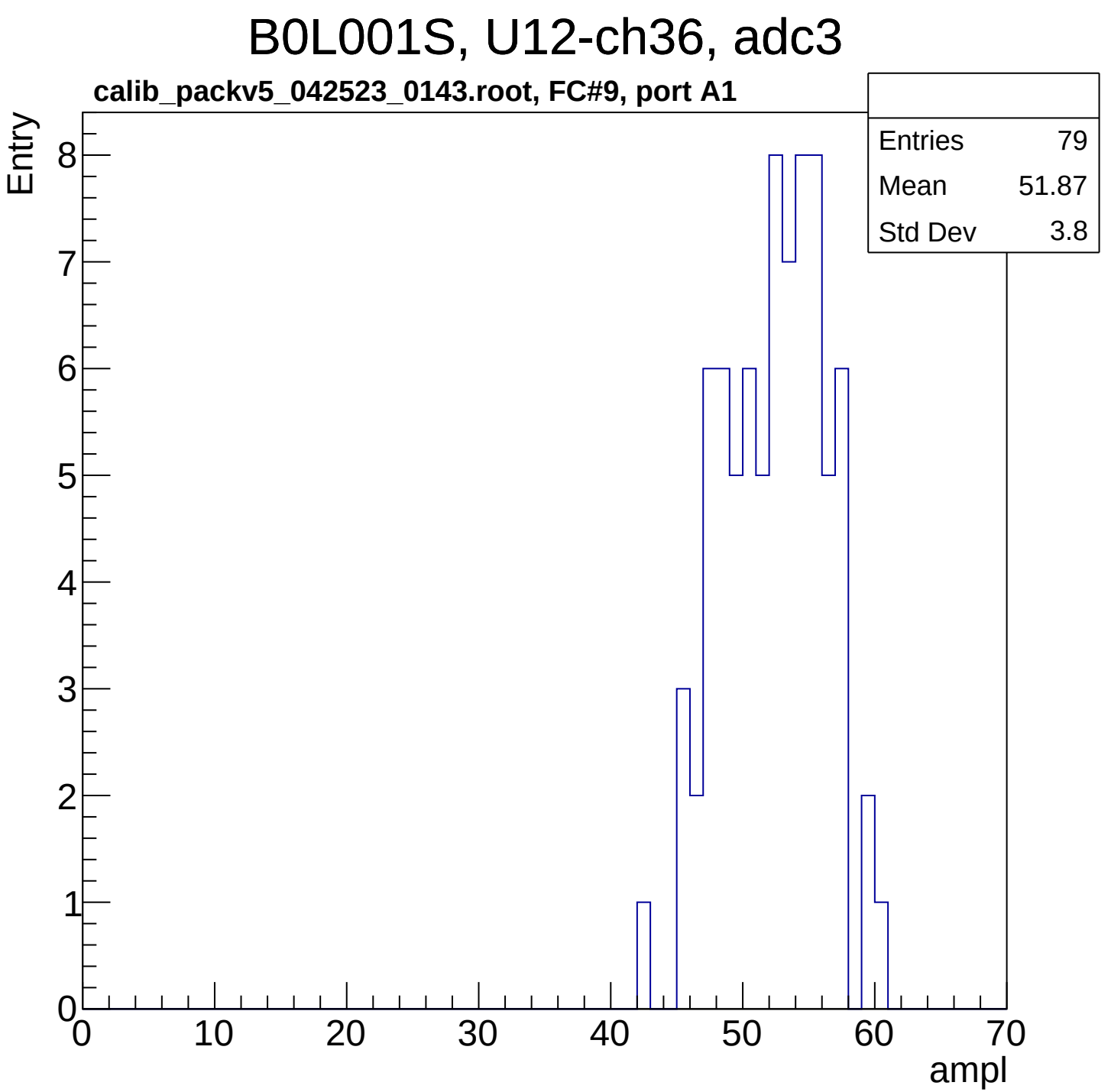
40
50
60
70


B0L001S, U12-ch36, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 61
Mean 45.41
Std Dev 3.442
Gaus mean : 45.6041
Gaus Width: 4.3760
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch36, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 79
Mean 51.87
Std Dev 3.8
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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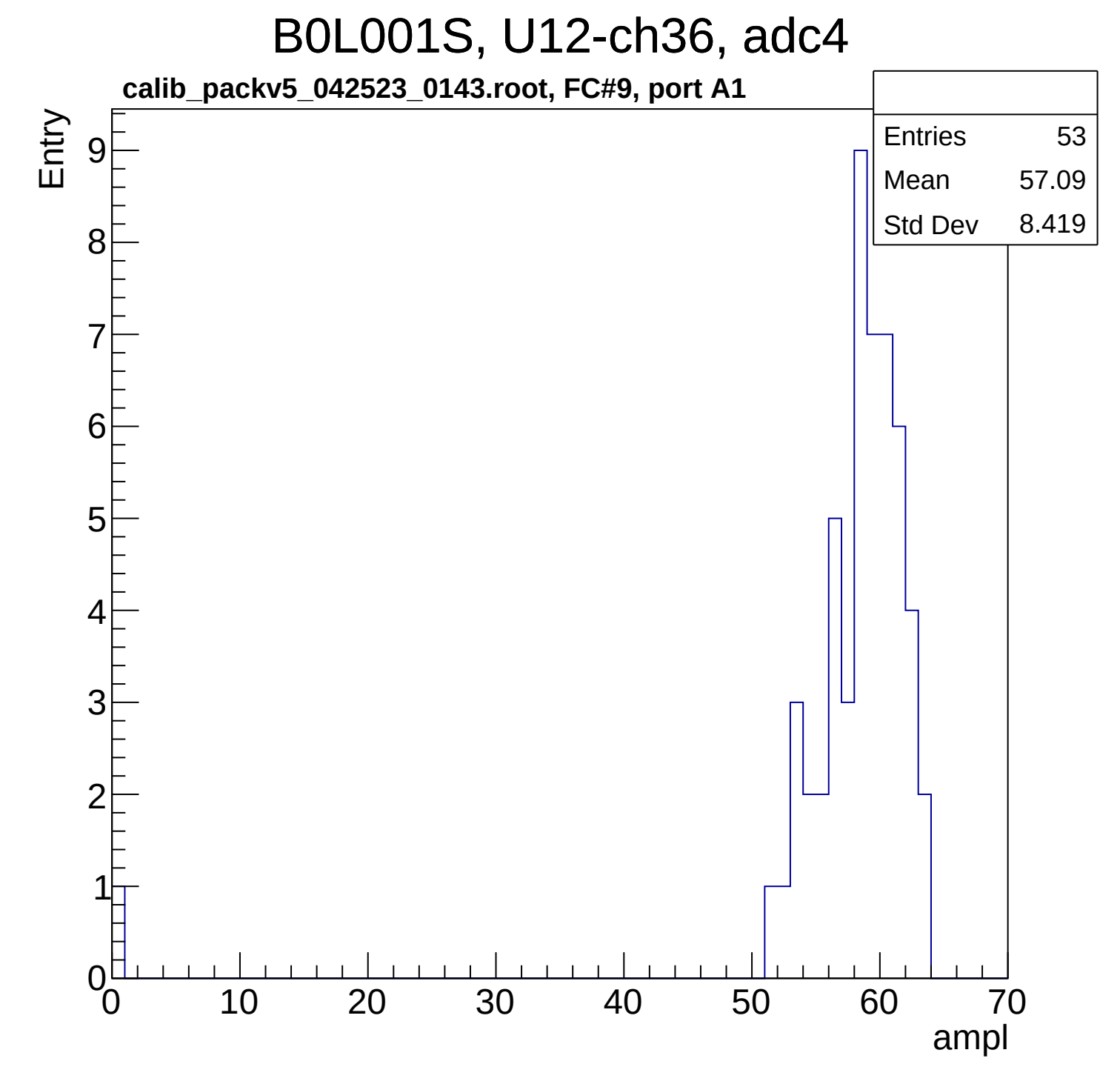
B0L001S, U12-ch36, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 53
Mean 57.09
Std Dev 8.419
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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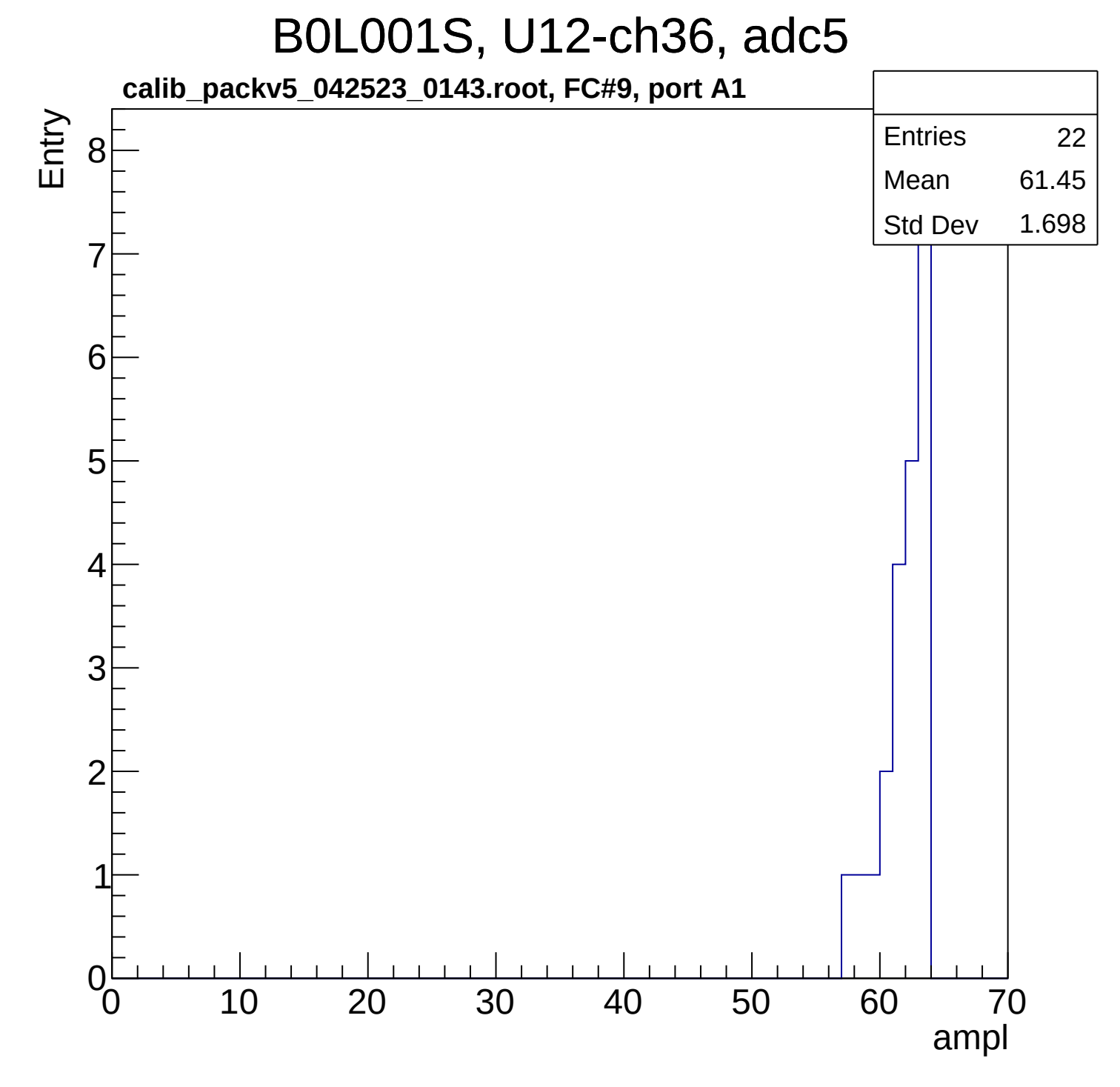
40
50
60
70


B0L001S, U12-ch36, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 22
Mean 61.45
Std Dev 1.698
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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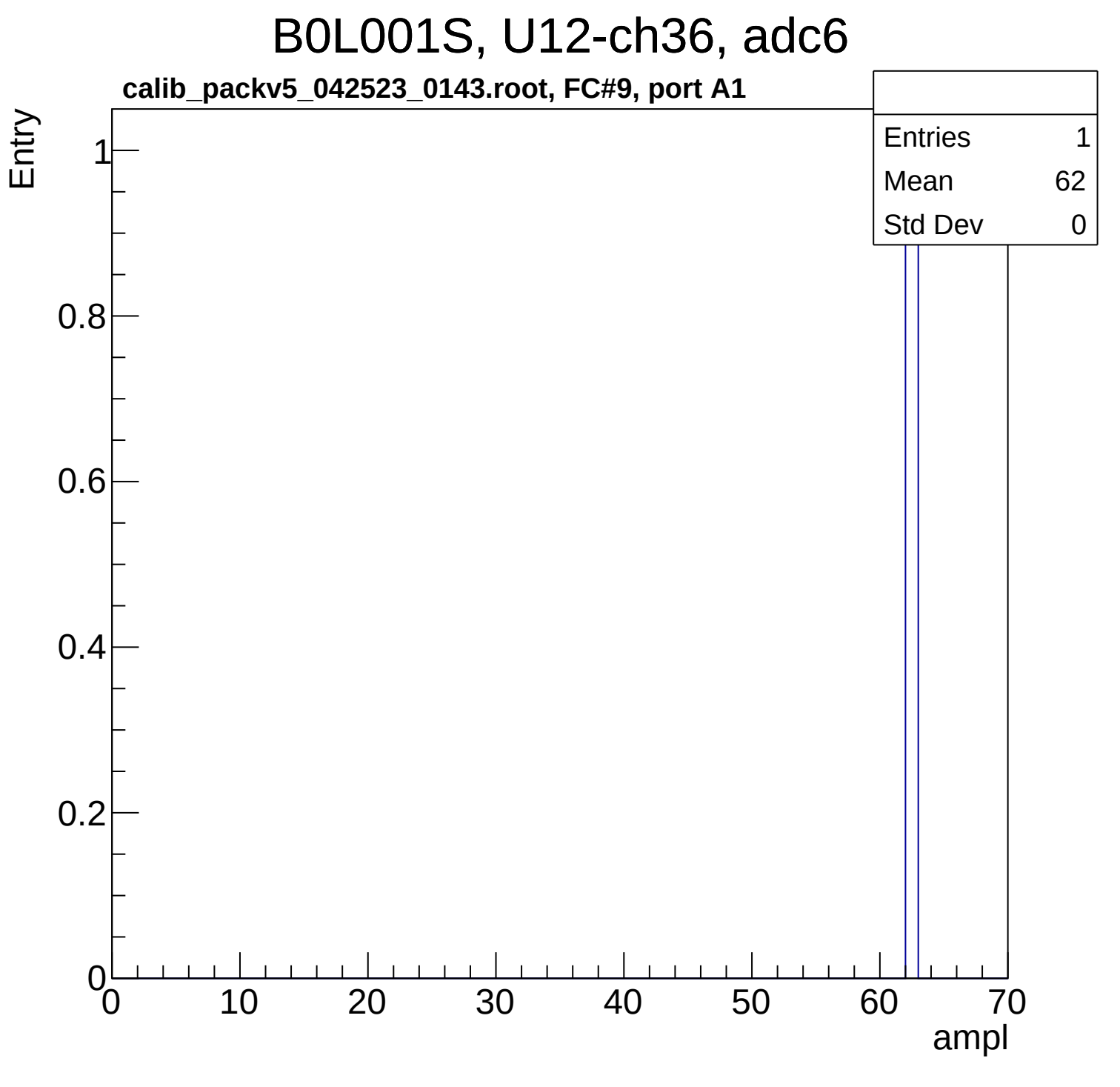
40
50
60
70


B0L001S, U12-ch36, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 62
Std Dev 0
Entry
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0.6
0.4
0.2
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10
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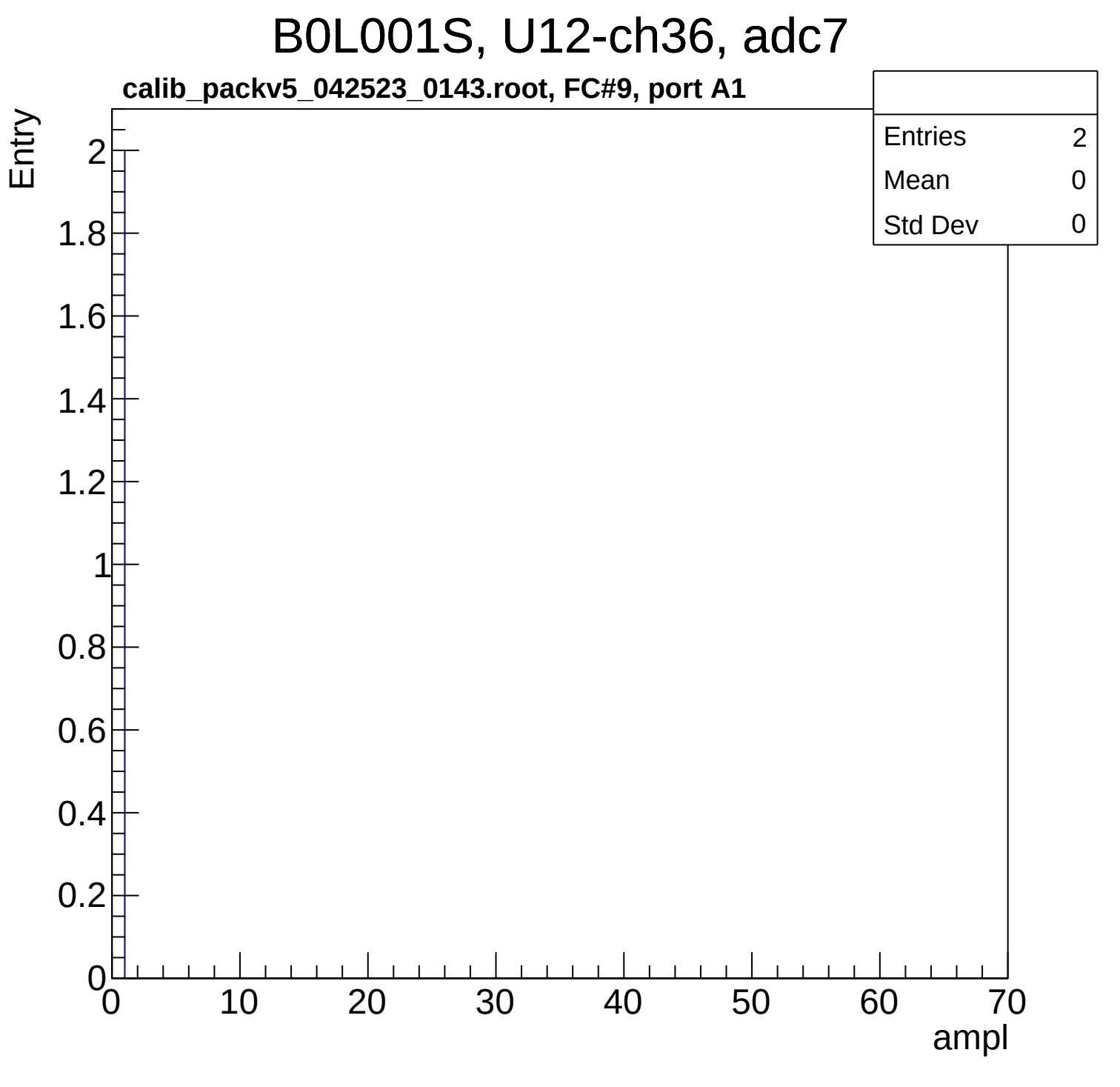
30
40
50
60
70
ampl


B0L001S, U12-ch36, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
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0.6
0.4
0.2
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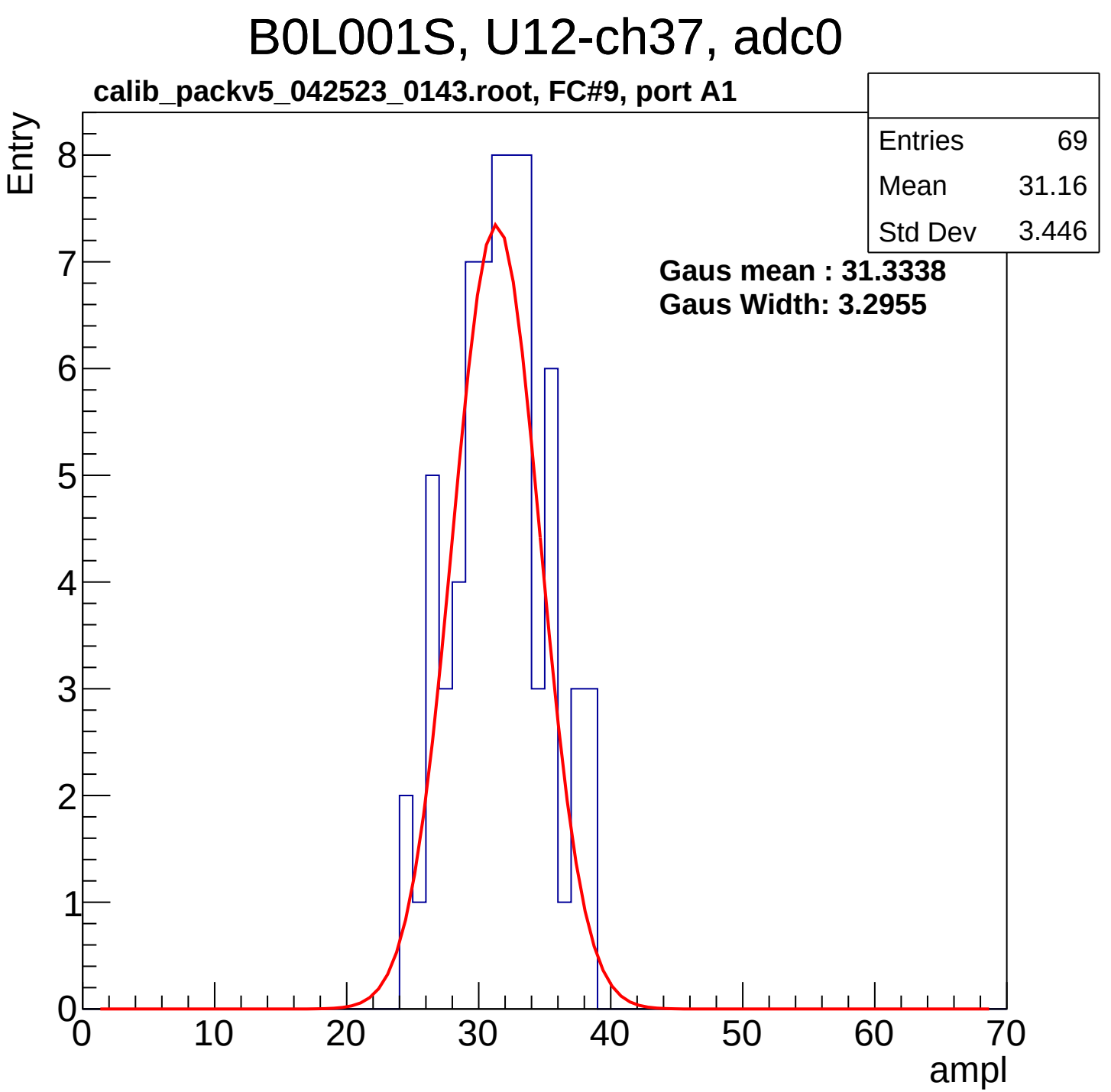
70
ampl


B0L001S, U12-ch37, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 69
Mean 31.16
Std Dev 3.446
Gaus mean : 31.3338
Gaus Width: 3.2955
Entry
ampl
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4
5
6
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0
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60
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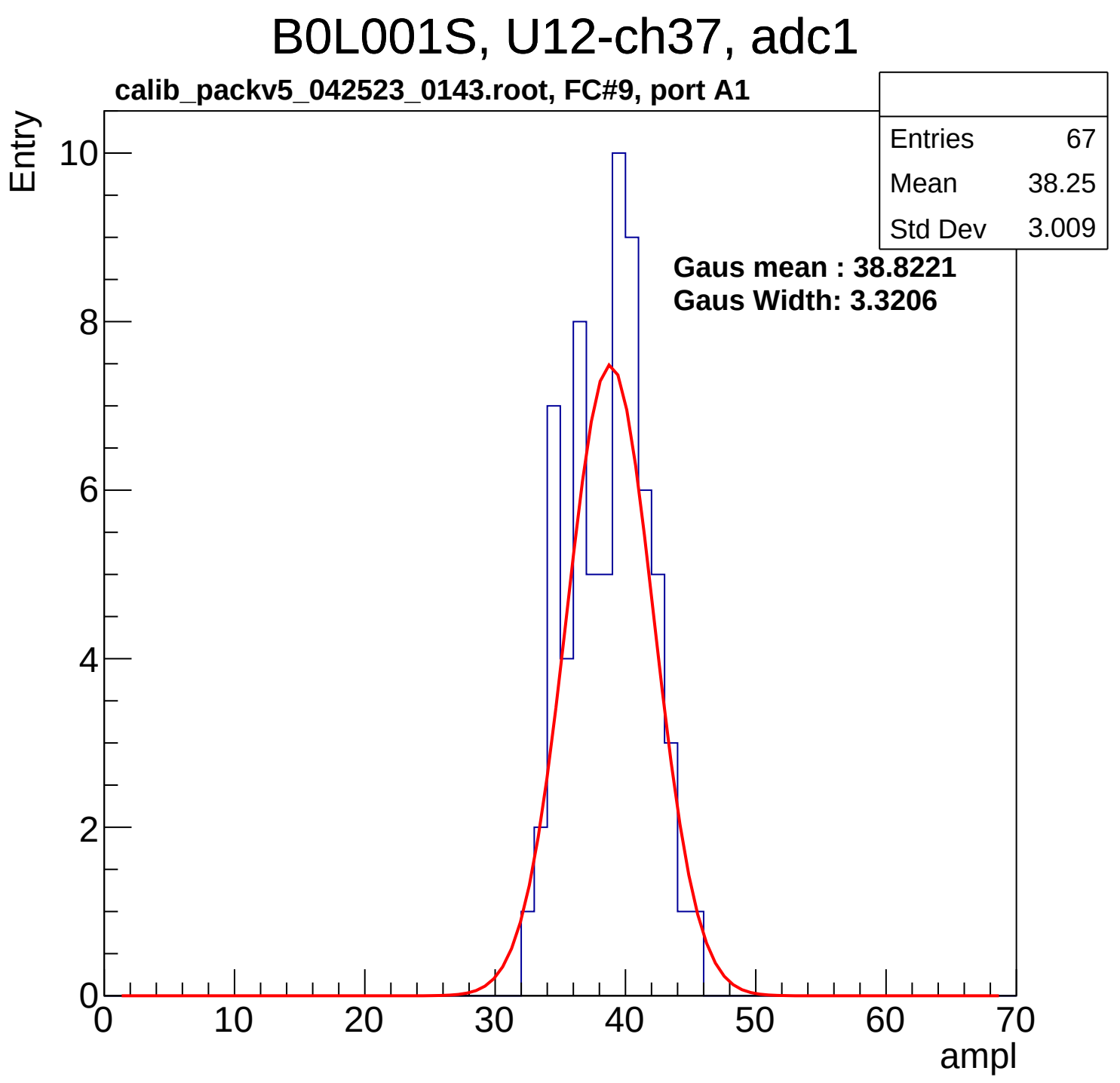
B0L001S, U12-ch37, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 67
Mean 38.25
Std Dev 3.009
Gaus mean : 38.8221
Gaus Width: 3.3206
Entry
ampl
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2
4
6
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0
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20
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40
50
60
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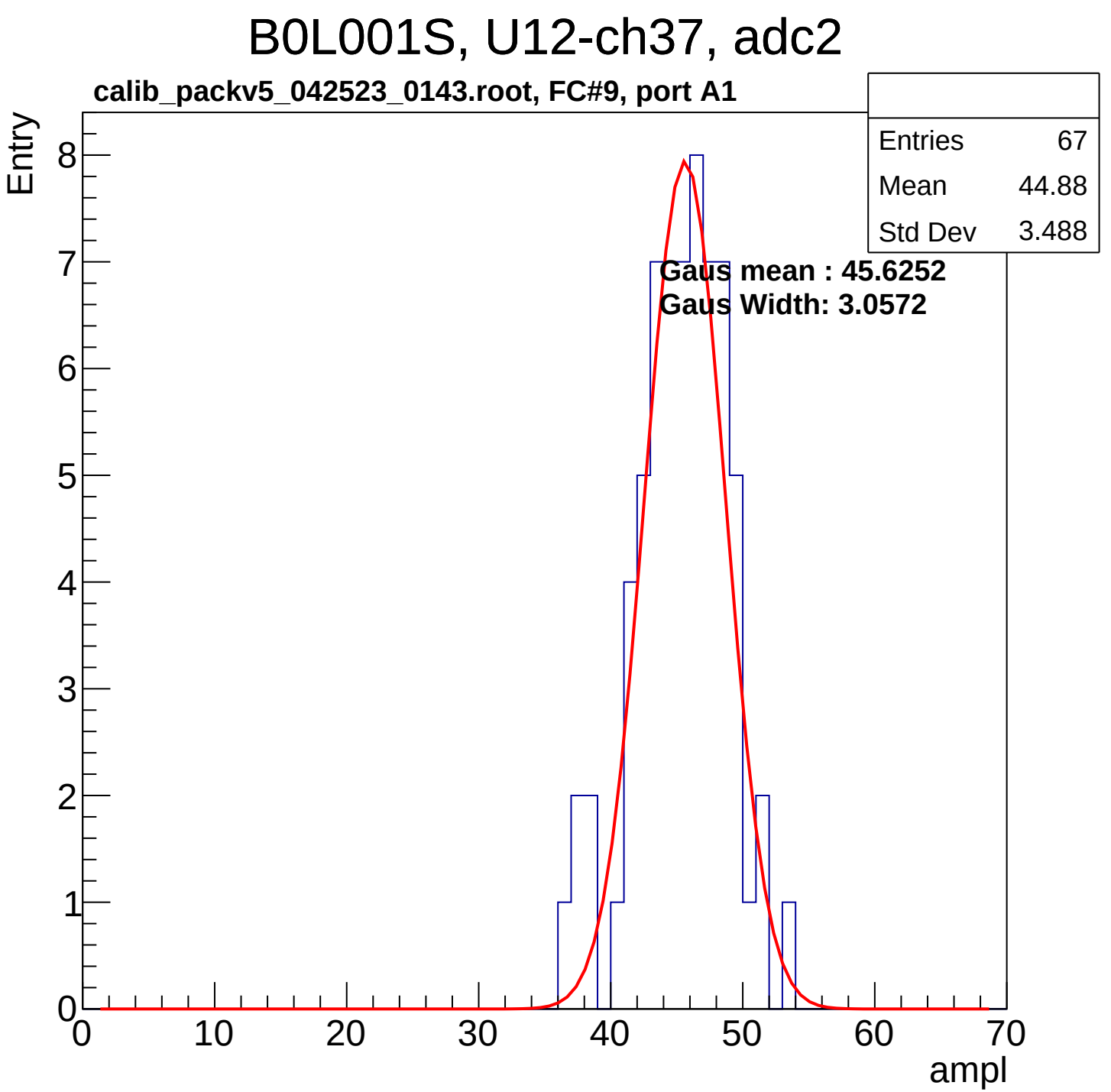
B0L001S, U12-ch37, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 67
Mean 44.88
Std Dev 3.488
Gaus mean : 45.6252
Gaus Width: 3.0572
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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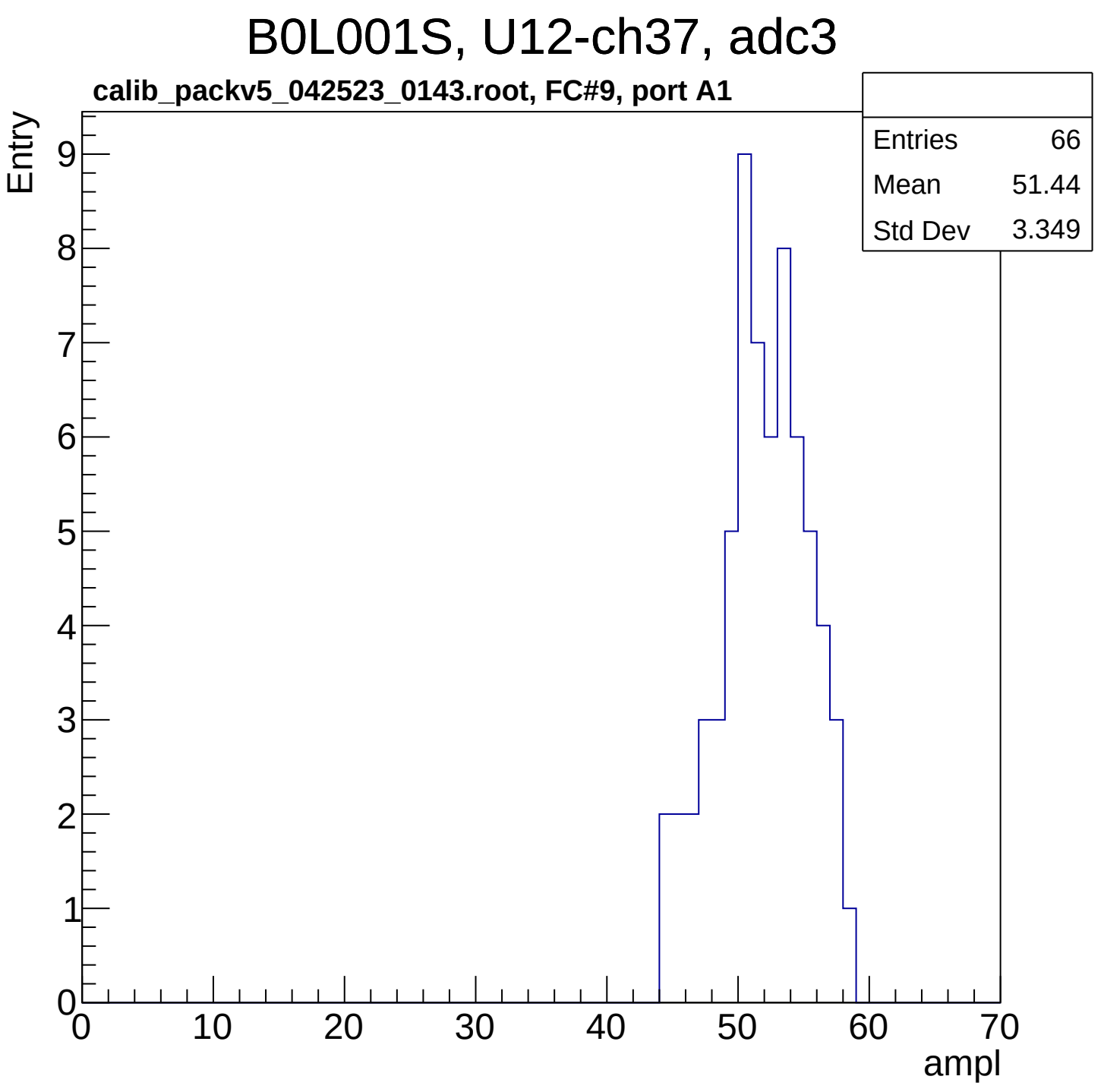
B0L001S, U12-ch37, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 66
Mean 51.44
Std Dev 3.349
Entry
ampl
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3
4
5
6
7
8
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0
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60
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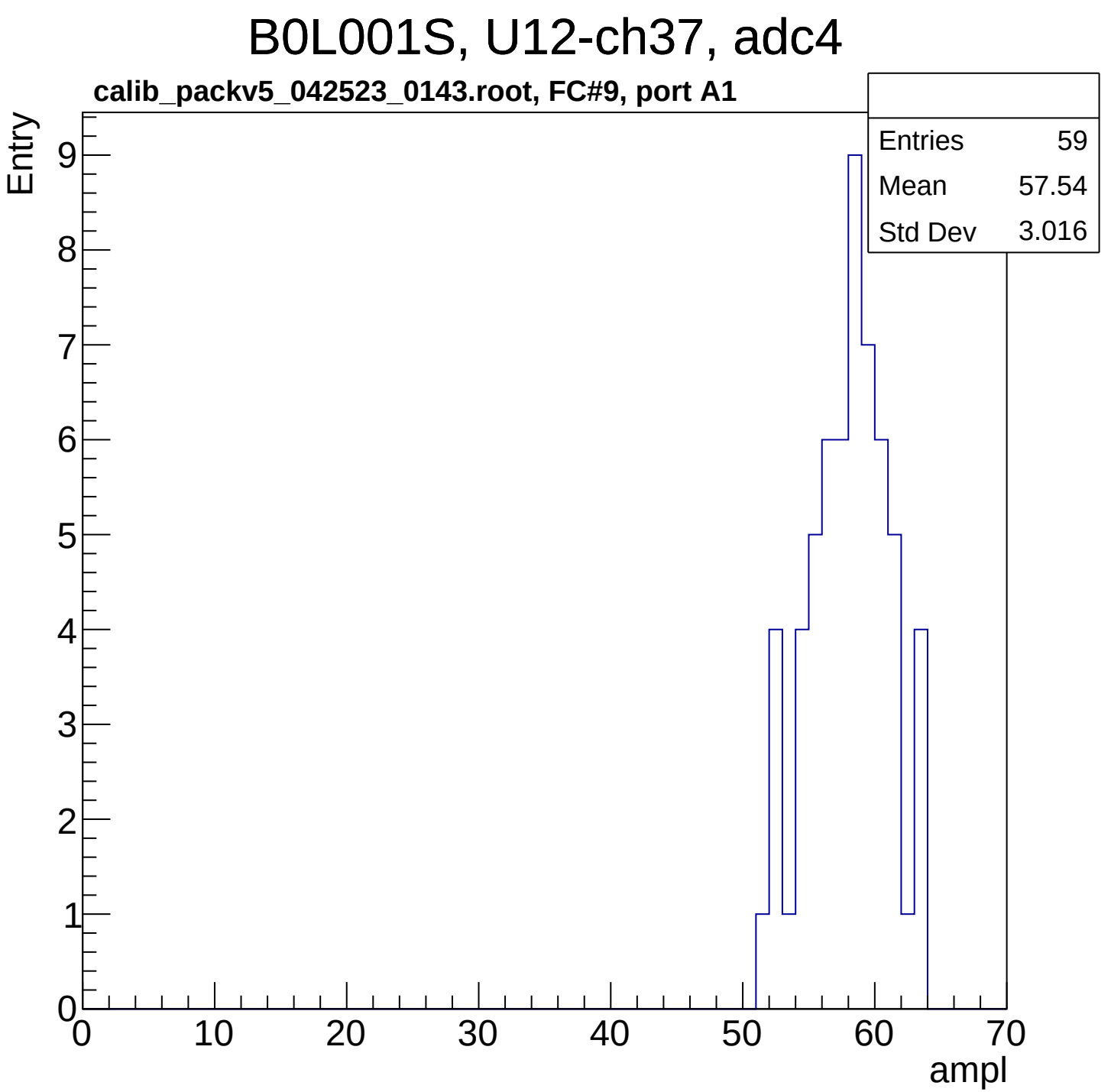
B0L001S, U12-ch37, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 59
Mean 57.54
Std Dev 3.016
Entry
ampl
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3
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5
6
7
8
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0
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60
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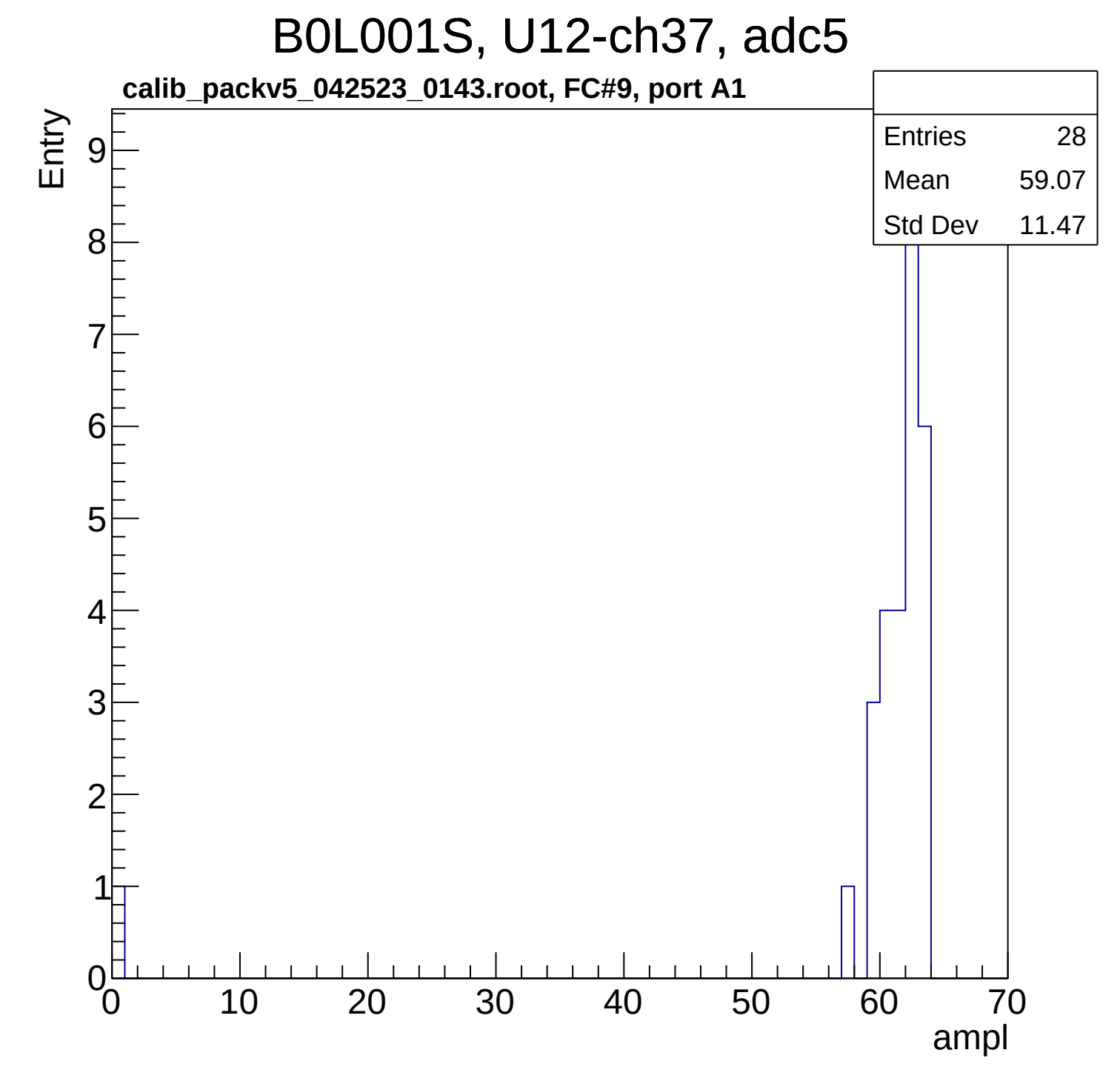
B0L001S, U12-ch37, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 28
Mean 59.07
Std Dev 11.47
Entry
ampl
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3
4
5
6
7
8
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0
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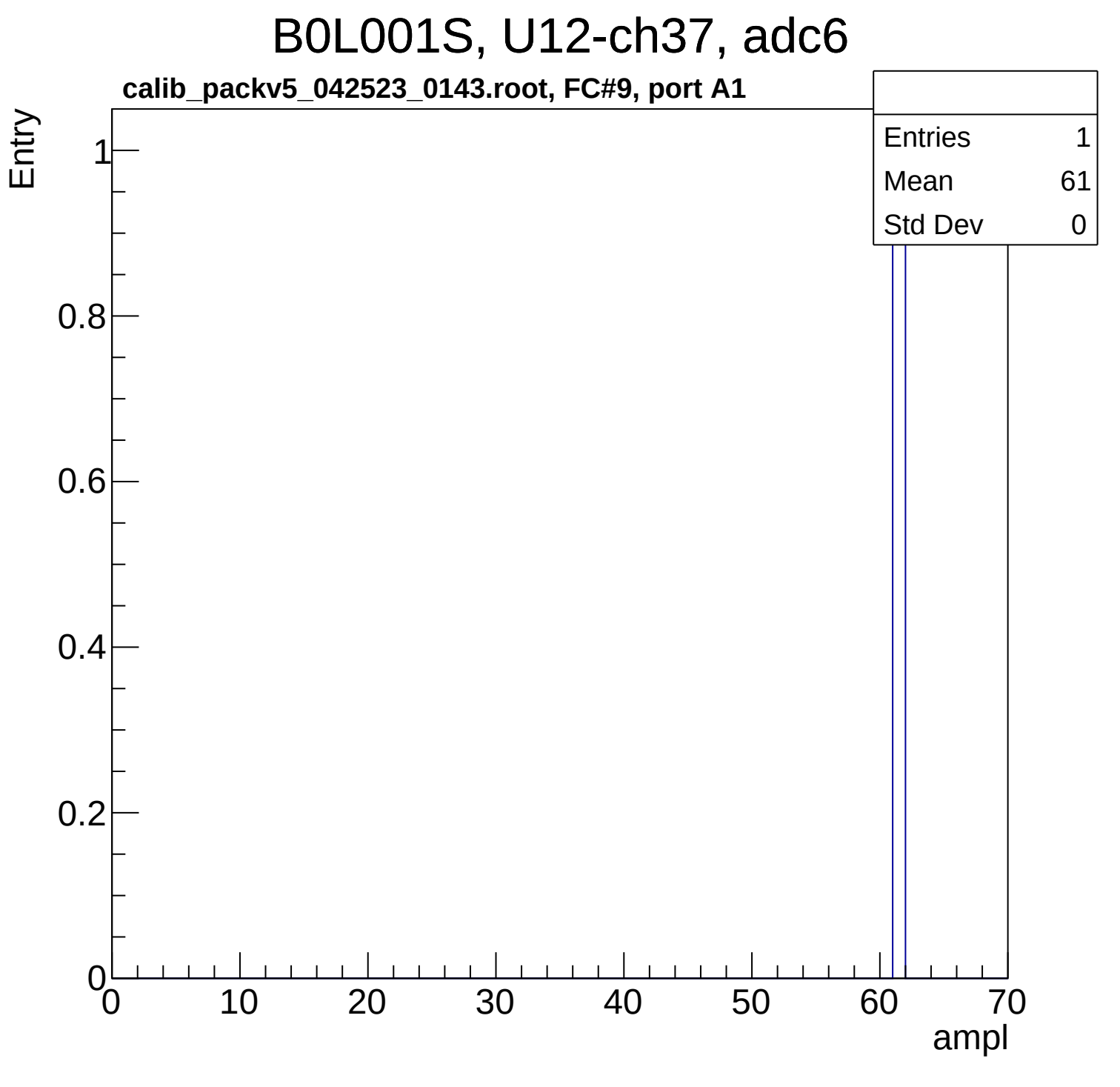
B0L001S, U12-ch37, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 61
Std Dev 0
Entry
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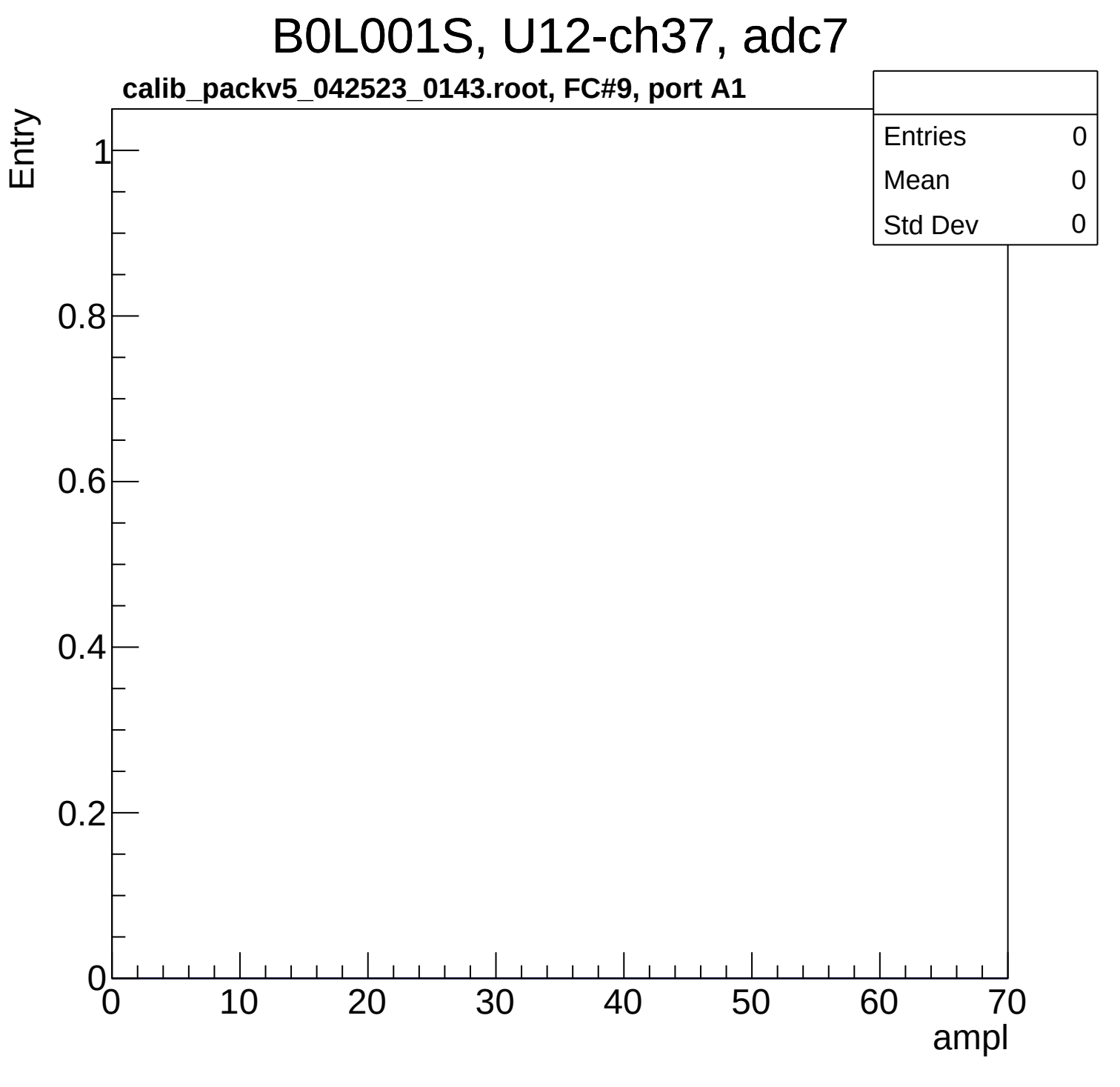
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch37, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
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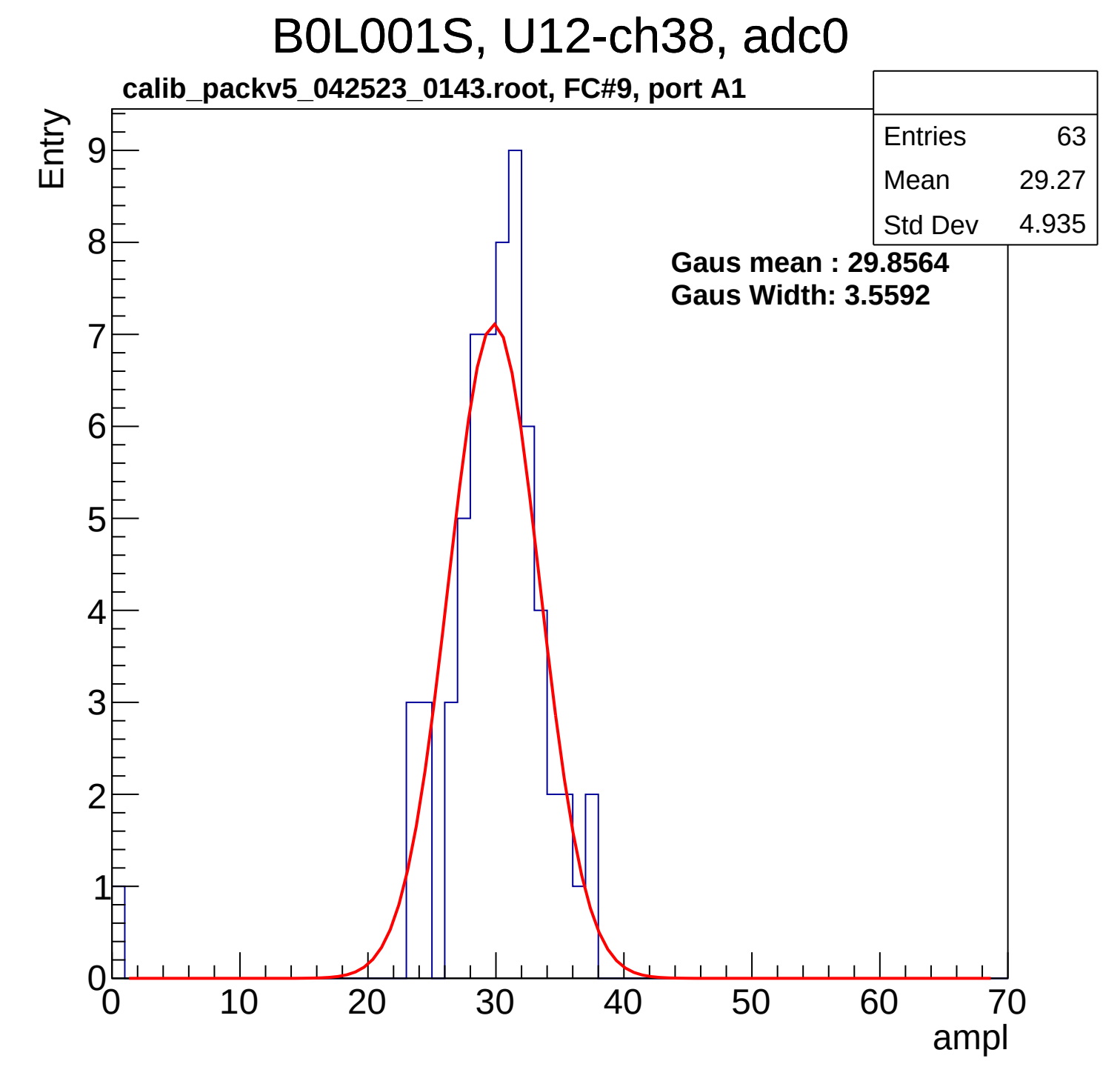
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch38, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 63
Mean 29.27
Std Dev 4.935
Gaus mean : 29.8564
Gaus Width: 3.5592
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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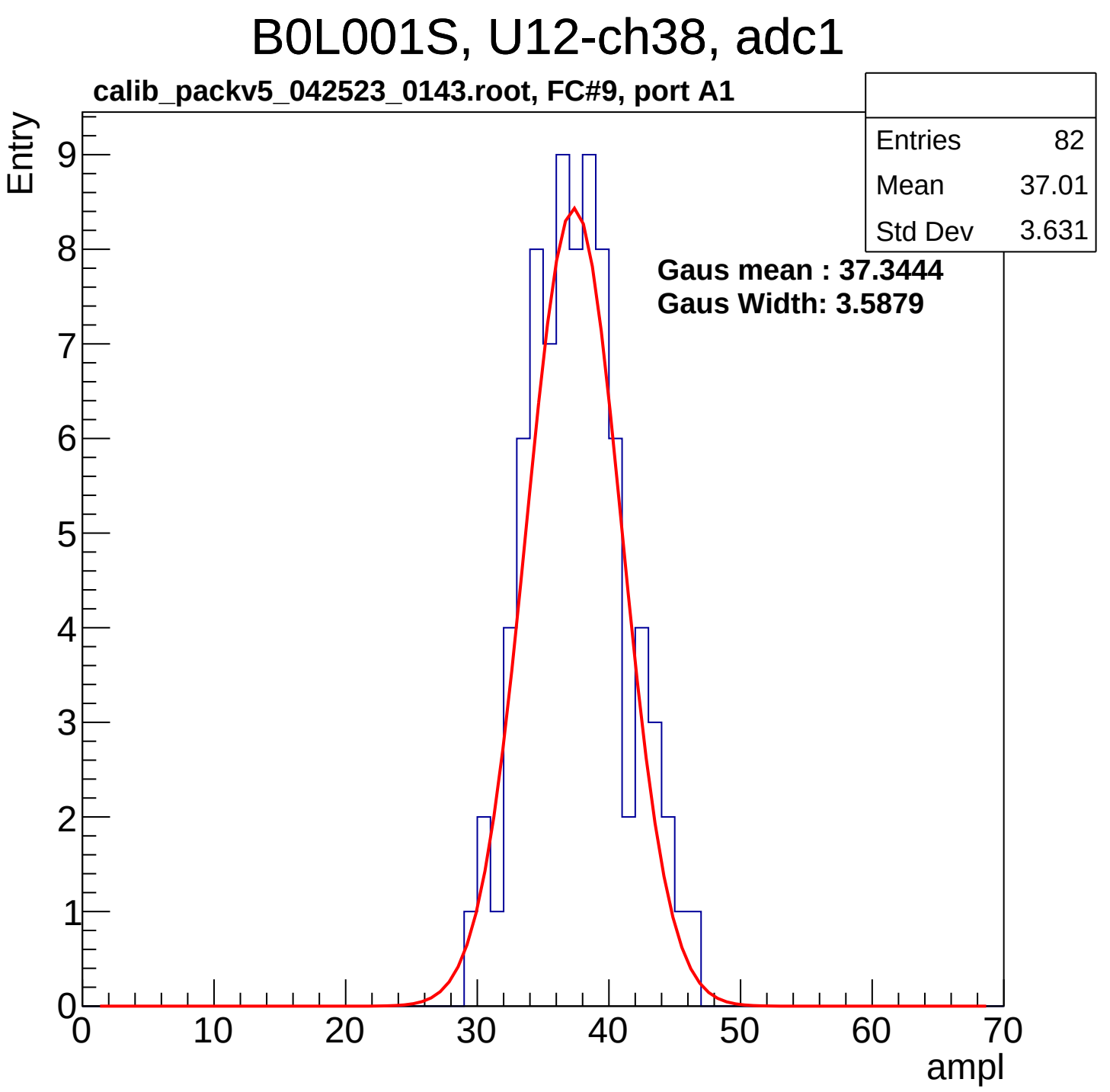
60
70


B0L001S, U12-ch38, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 82
Mean 37.01
Std Dev 3.631
Gaus mean : 37.3444
Gaus Width: 3.5879
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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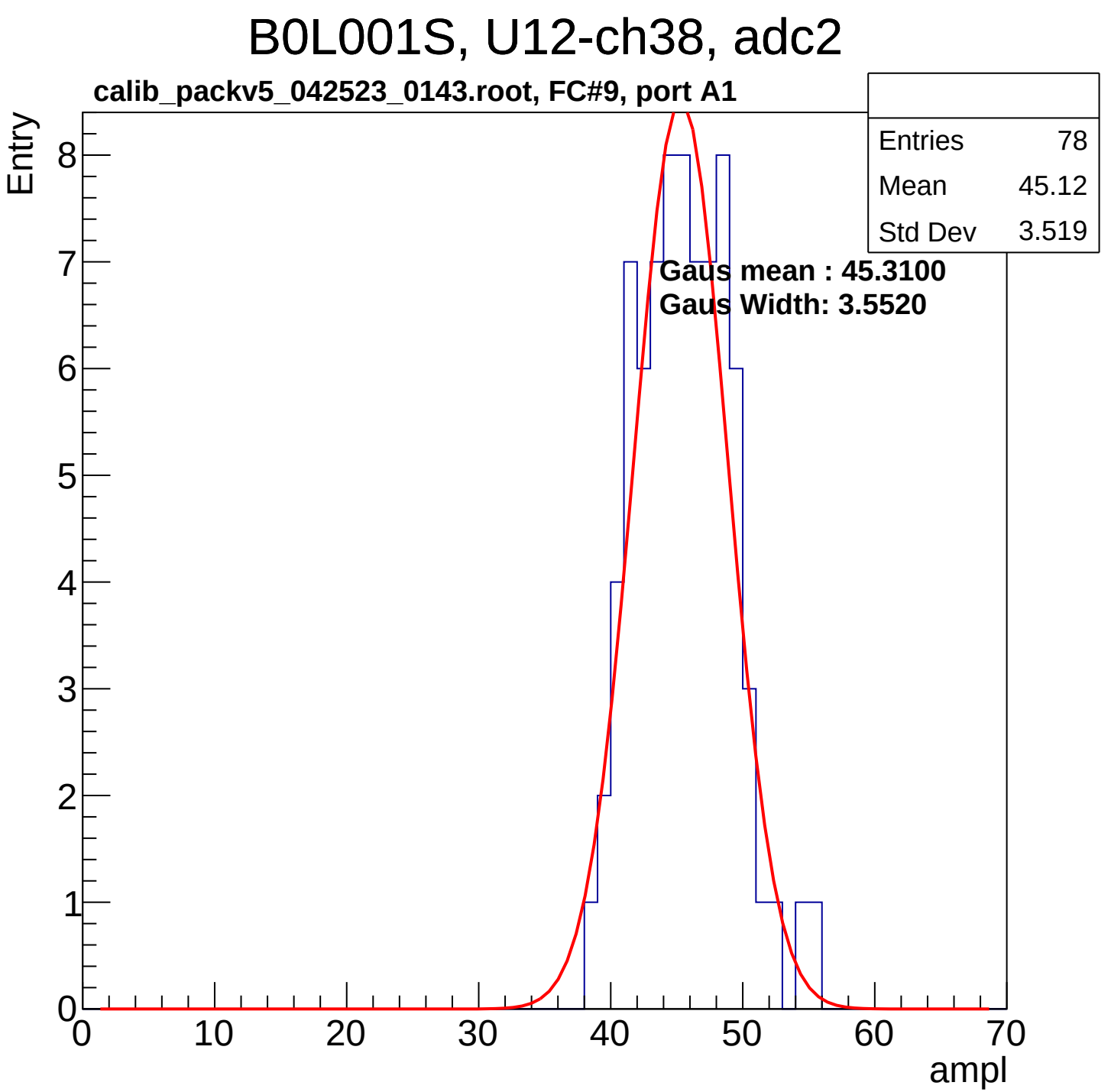
B0L001S, U12-ch38, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 78
Mean 45.12
Std Dev 3.519
Gaus mean : 45.3100
Gaus Width: 3.5520
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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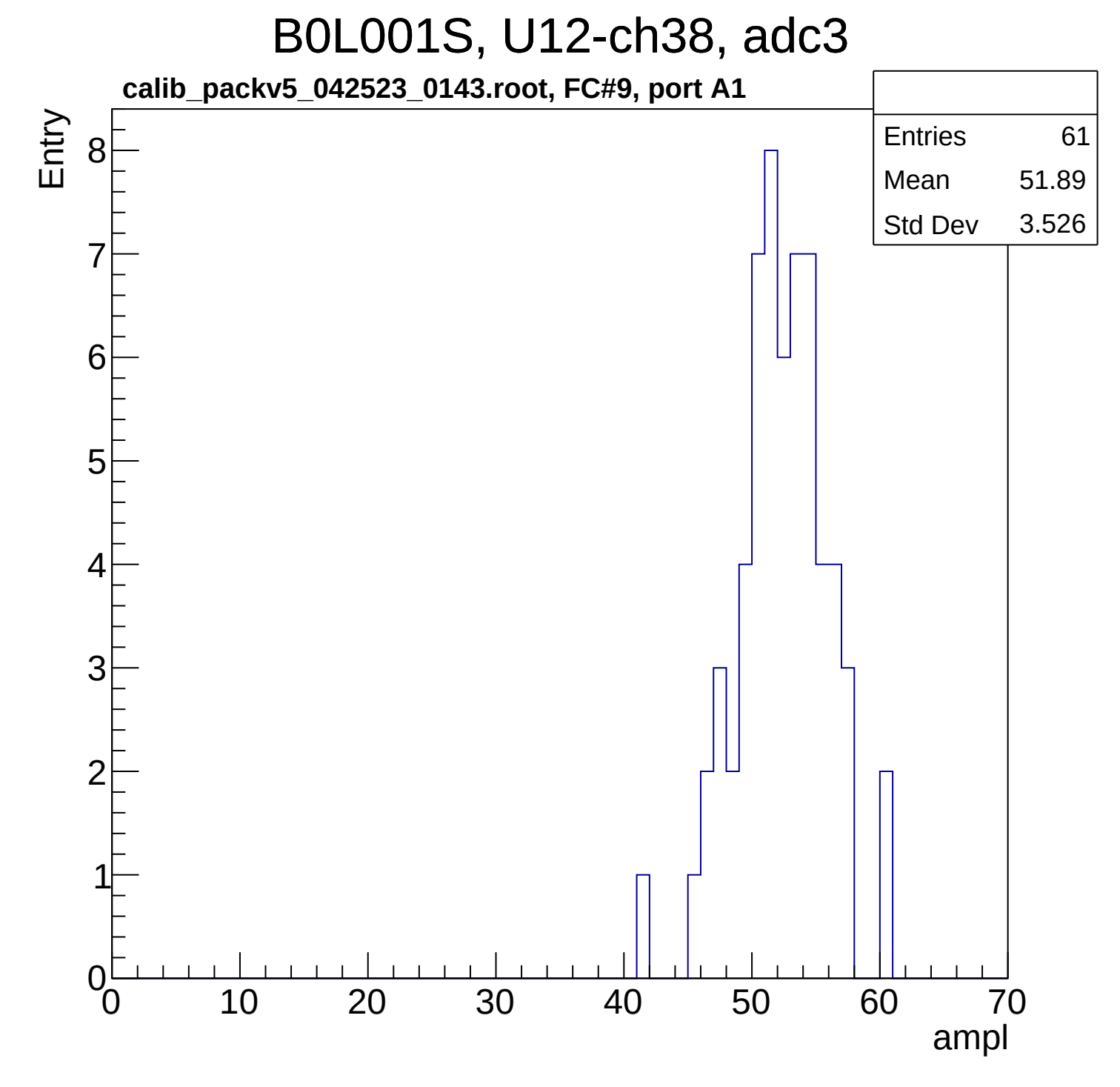
B0L001S, U12-ch38, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 61
Mean 51.89
Std Dev 3.526
Entry
ampl
0
1
2
3
4
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60
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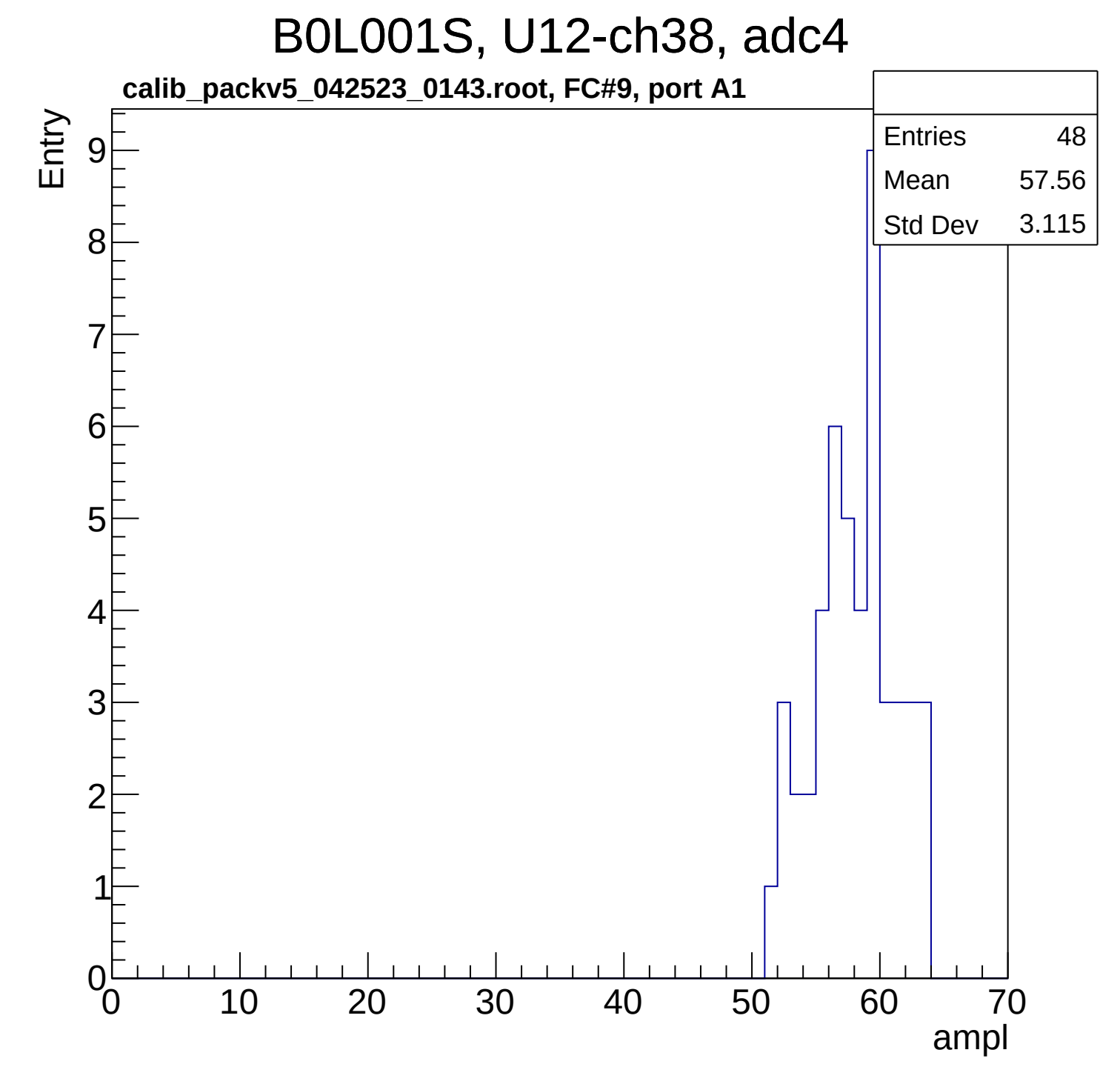
B0L001S, U12-ch38, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 48
Mean 57.56
Std Dev 3.115
Entry
ampl
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2
3
4
5
6
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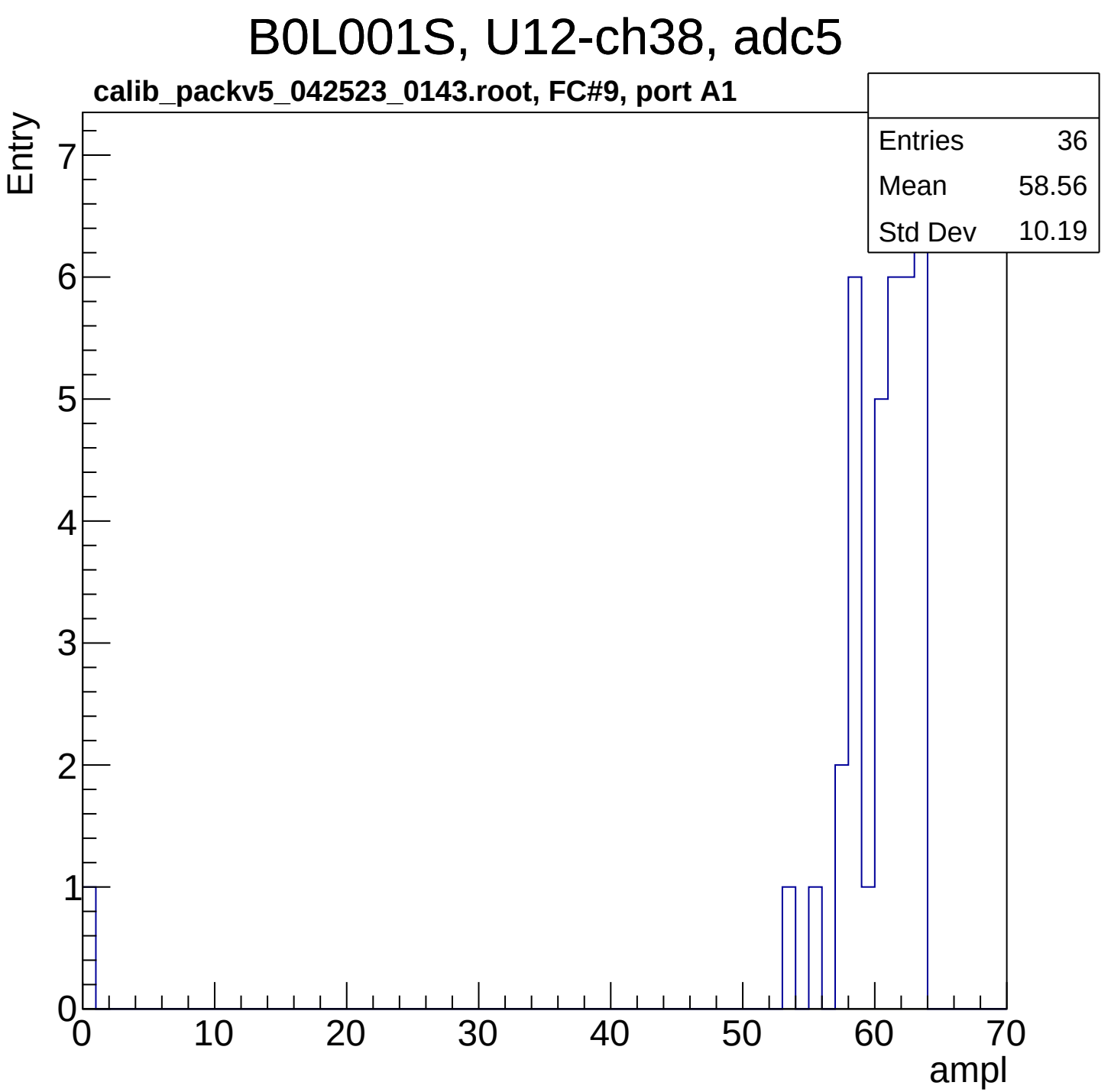
B0L001S, U12-ch38, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 36
Mean 58.56
Std Dev 10.19
Entry
ampl
0
1
2
3
4
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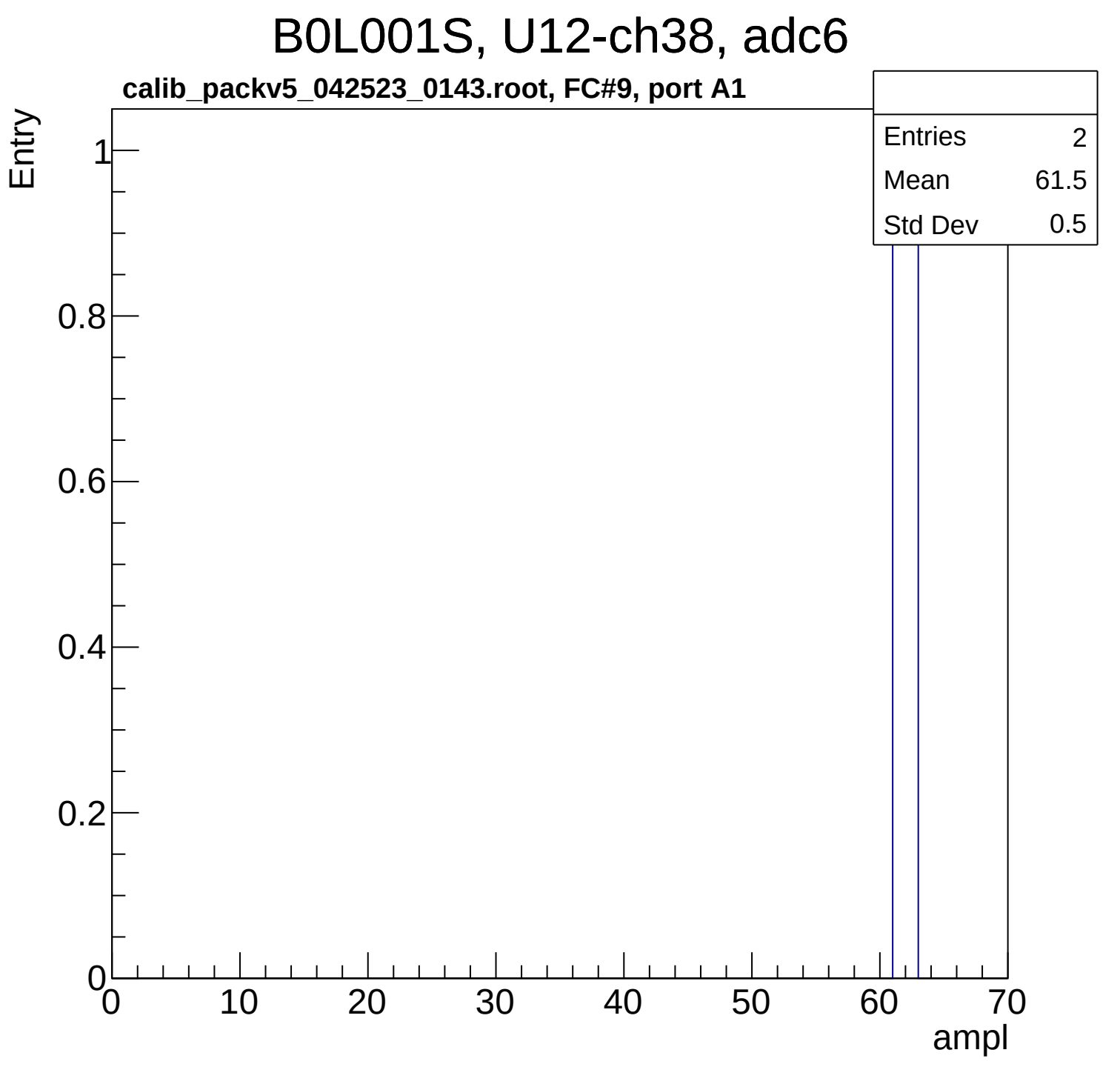
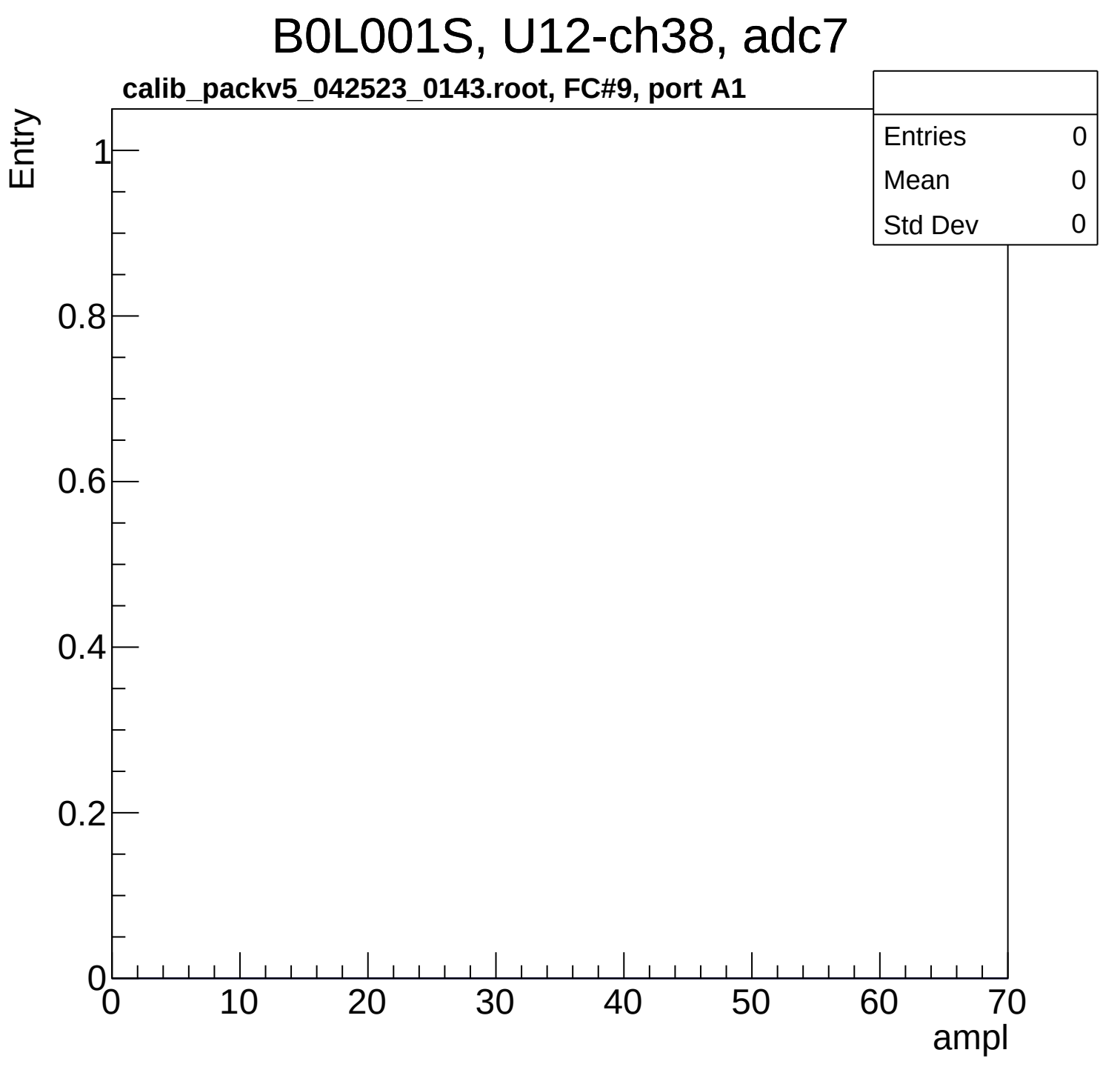
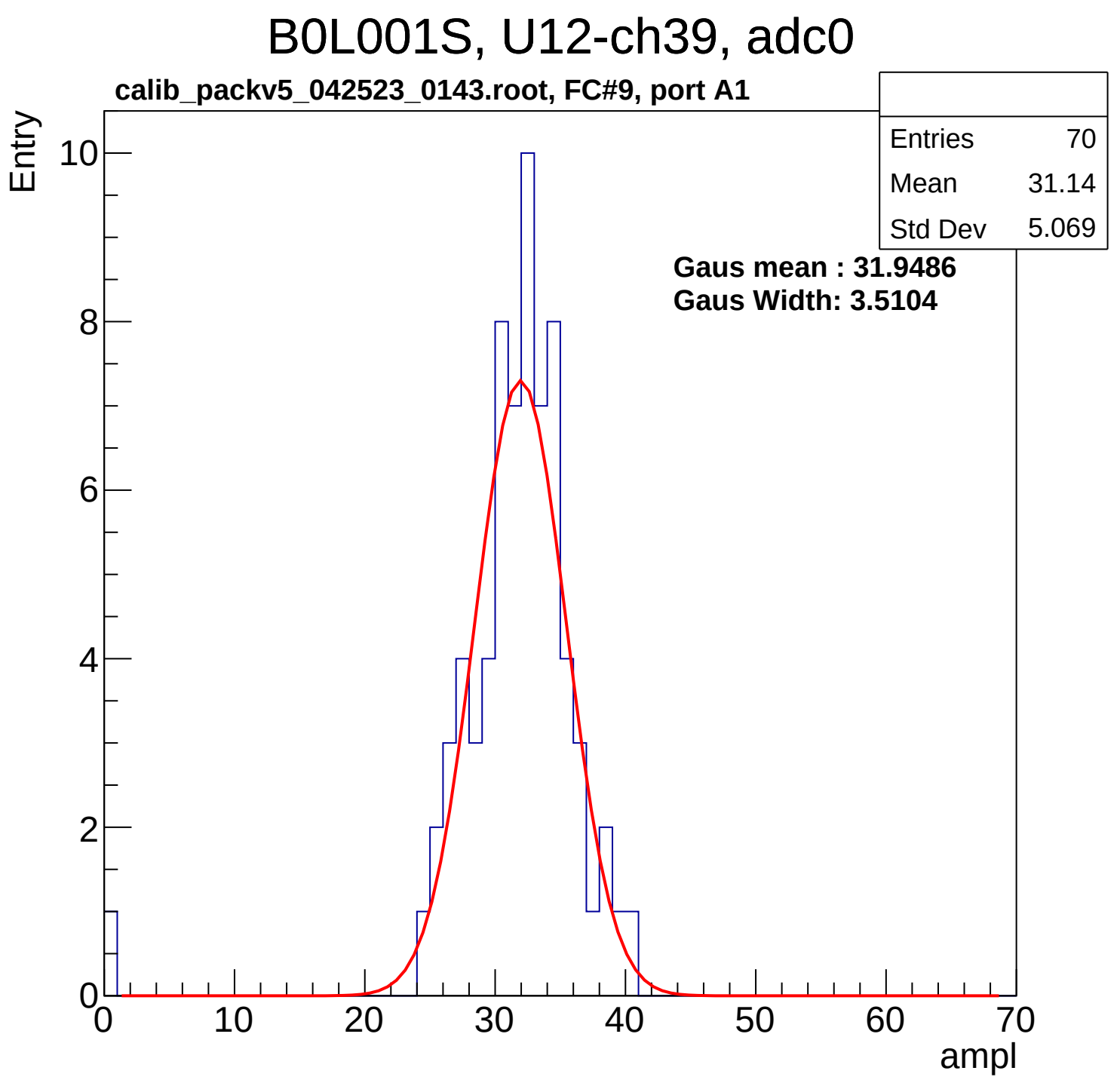
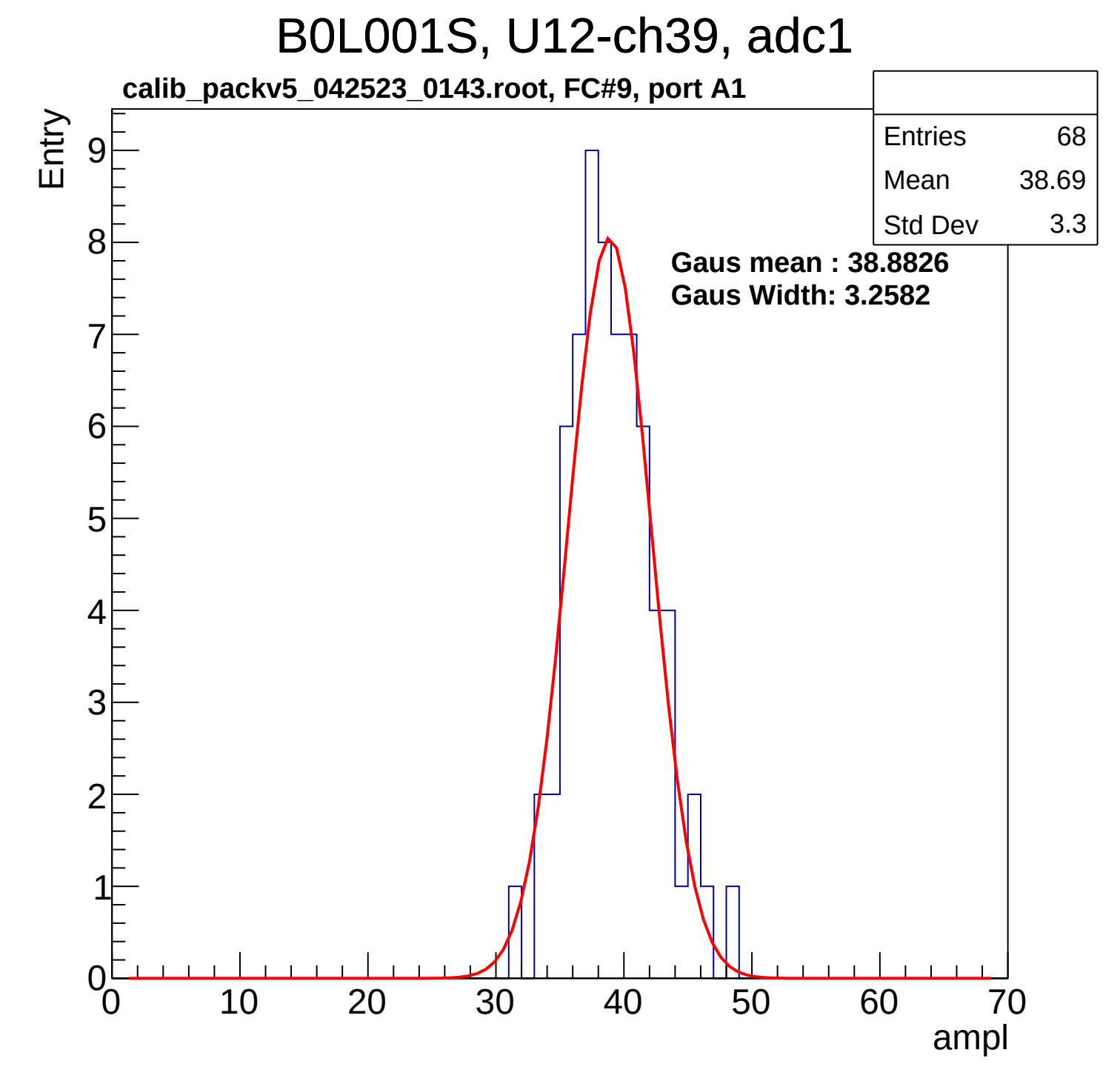

B0L001S, U12-ch38, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 61.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch38, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch39, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 70
Mean 31.14
Std Dev 5.069
Gaus mean : 31.9486
Gaus Width: 3.5104
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch39, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 68
Mean 38.69
Std Dev 3.3
Gaus mean : 38.8826
Gaus Width: 3.2582
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
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40
50
60
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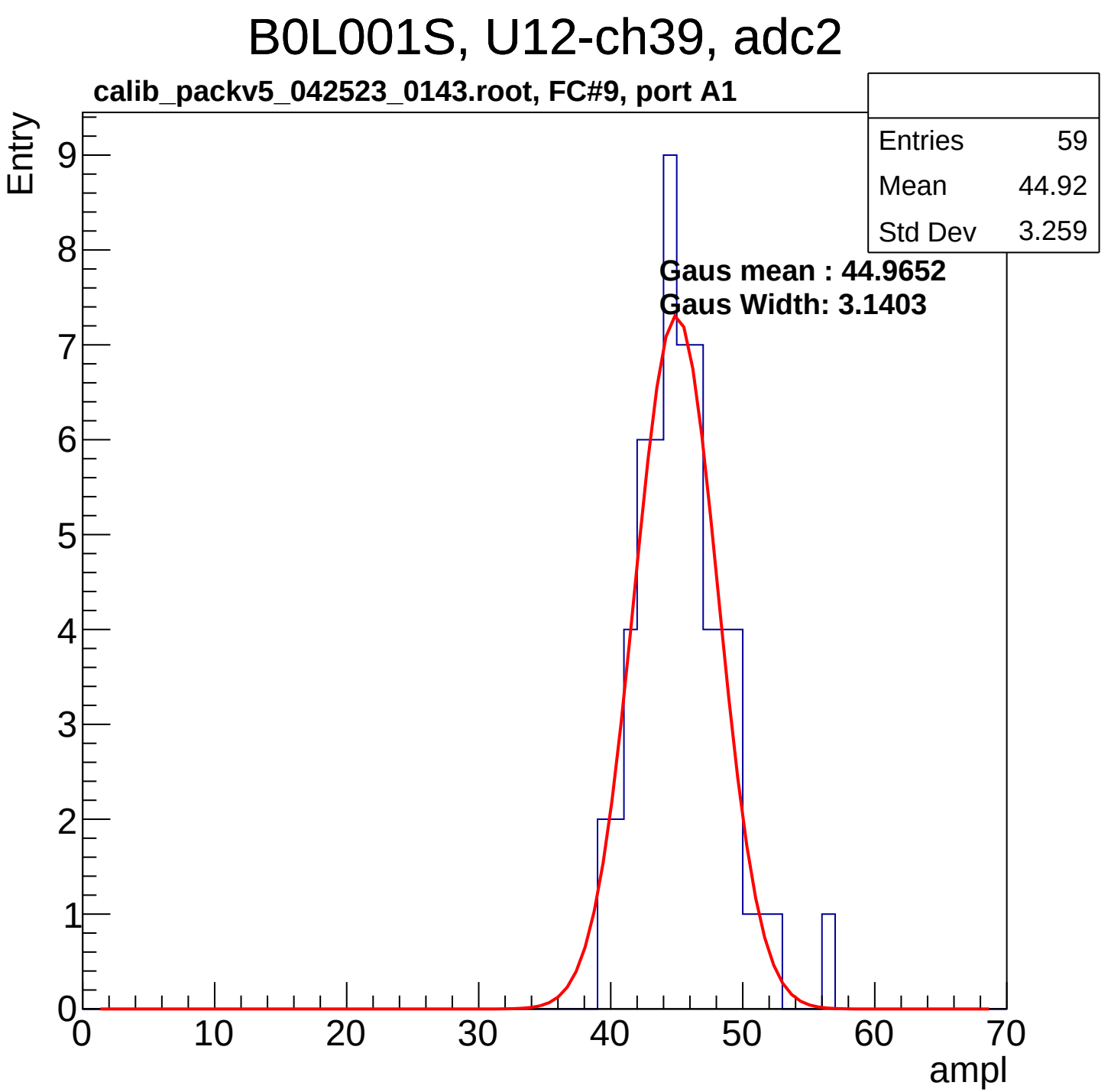
B0L001S, U12-ch39, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 59
Mean 44.92
Std Dev 3.259
Gaus mean : 44.9652
Gaus Width: 3.1403
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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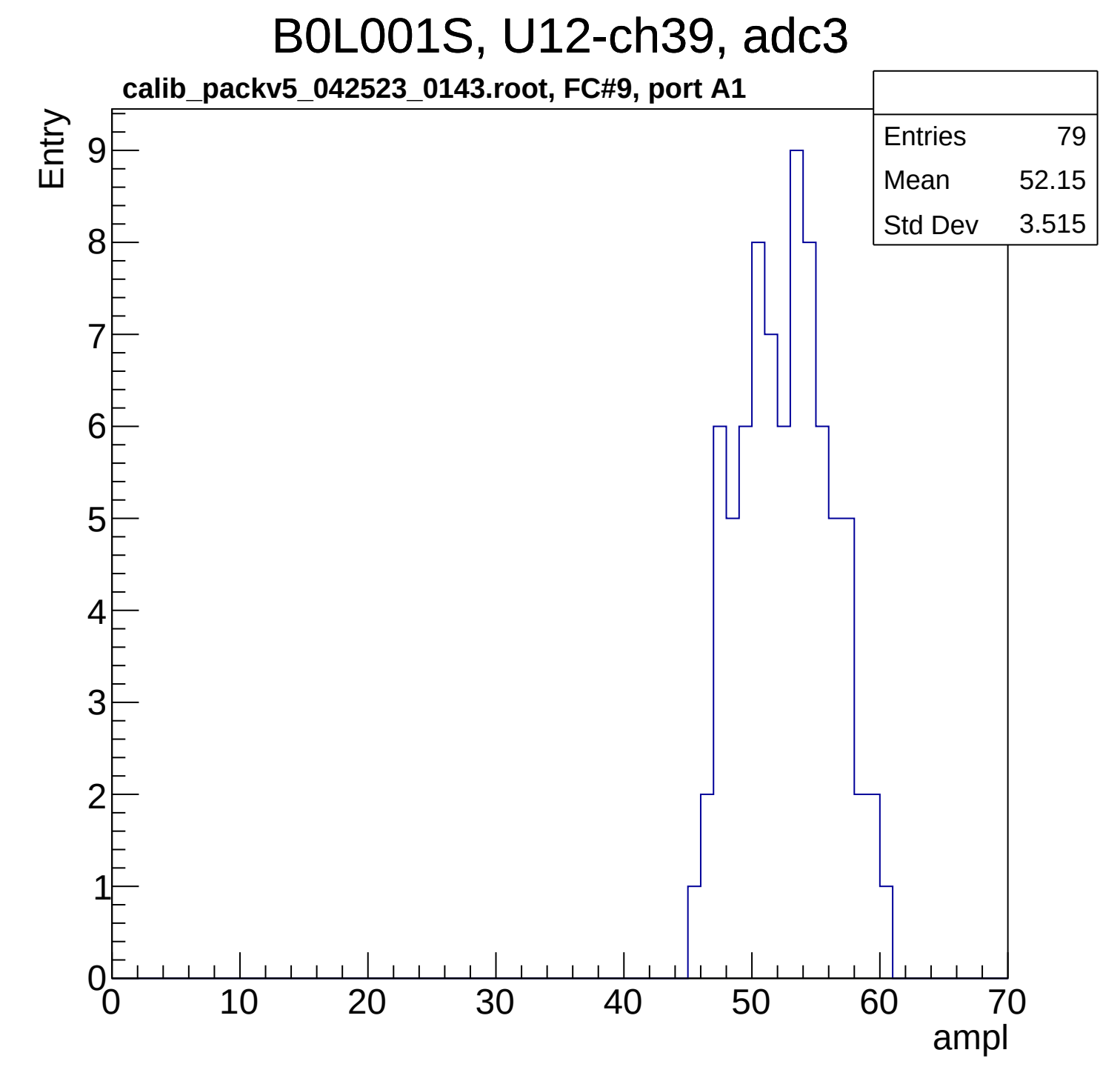
B0L001S, U12-ch39, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 79
Mean 52.15
Std Dev 3.515
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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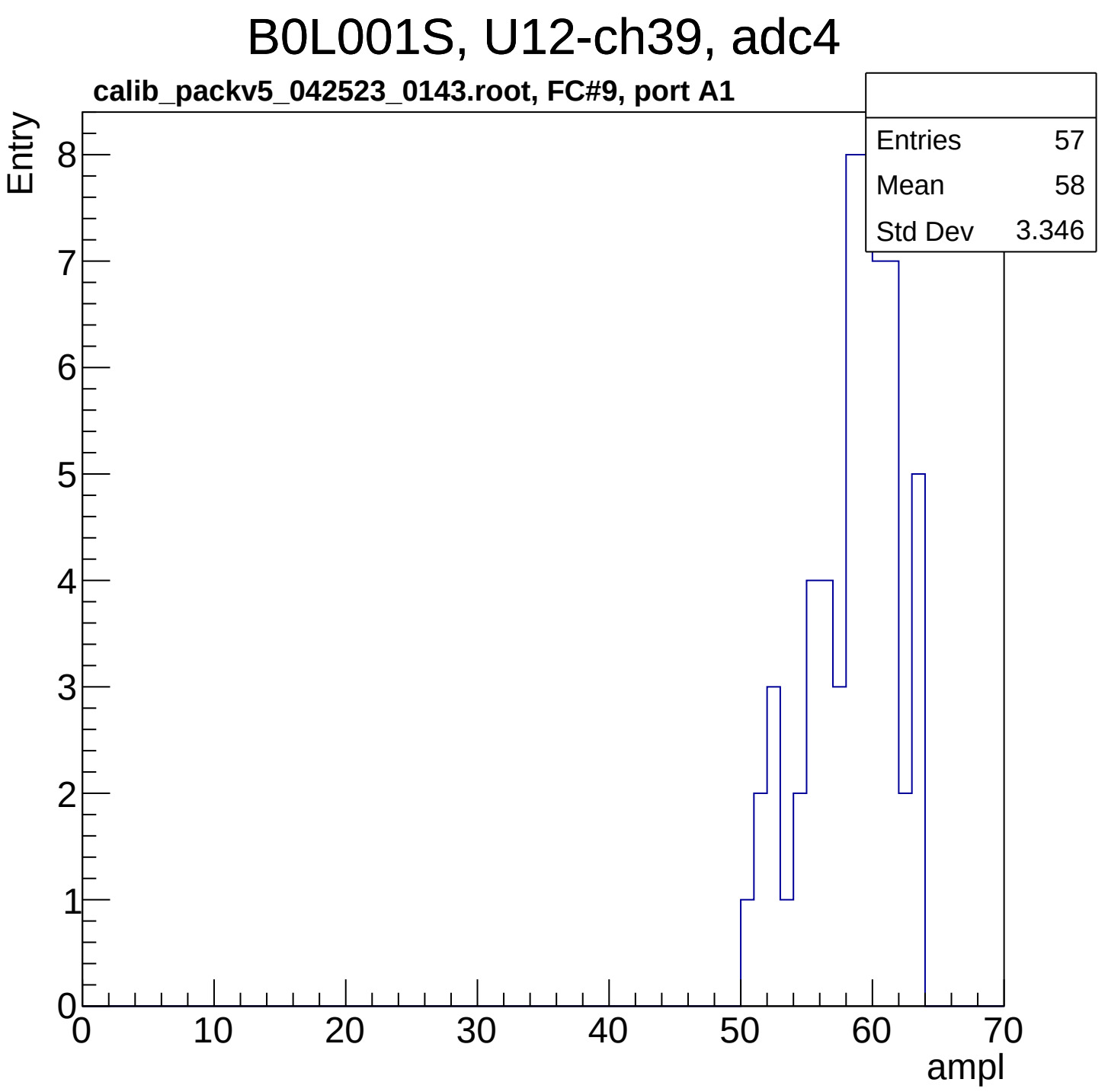
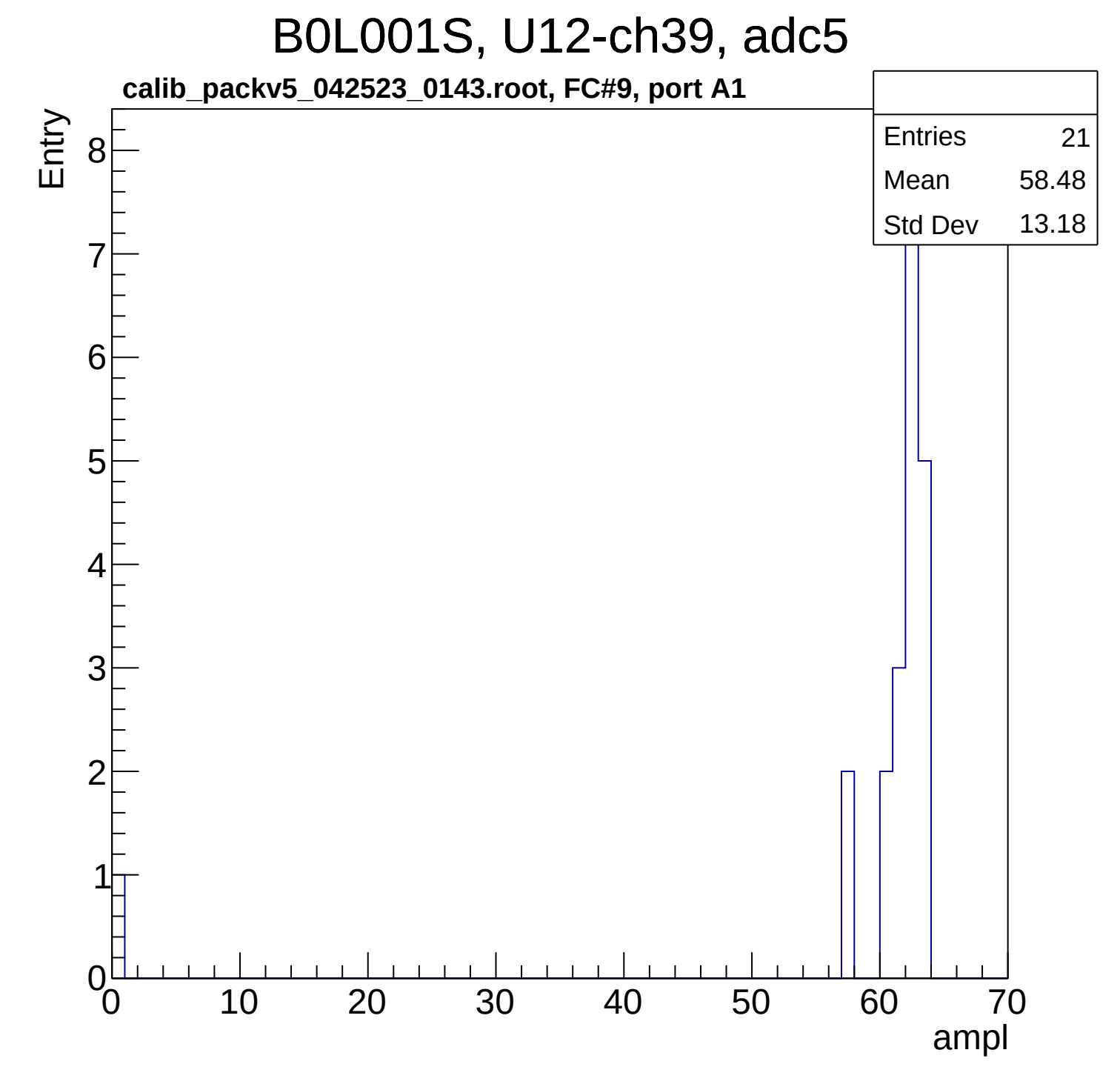
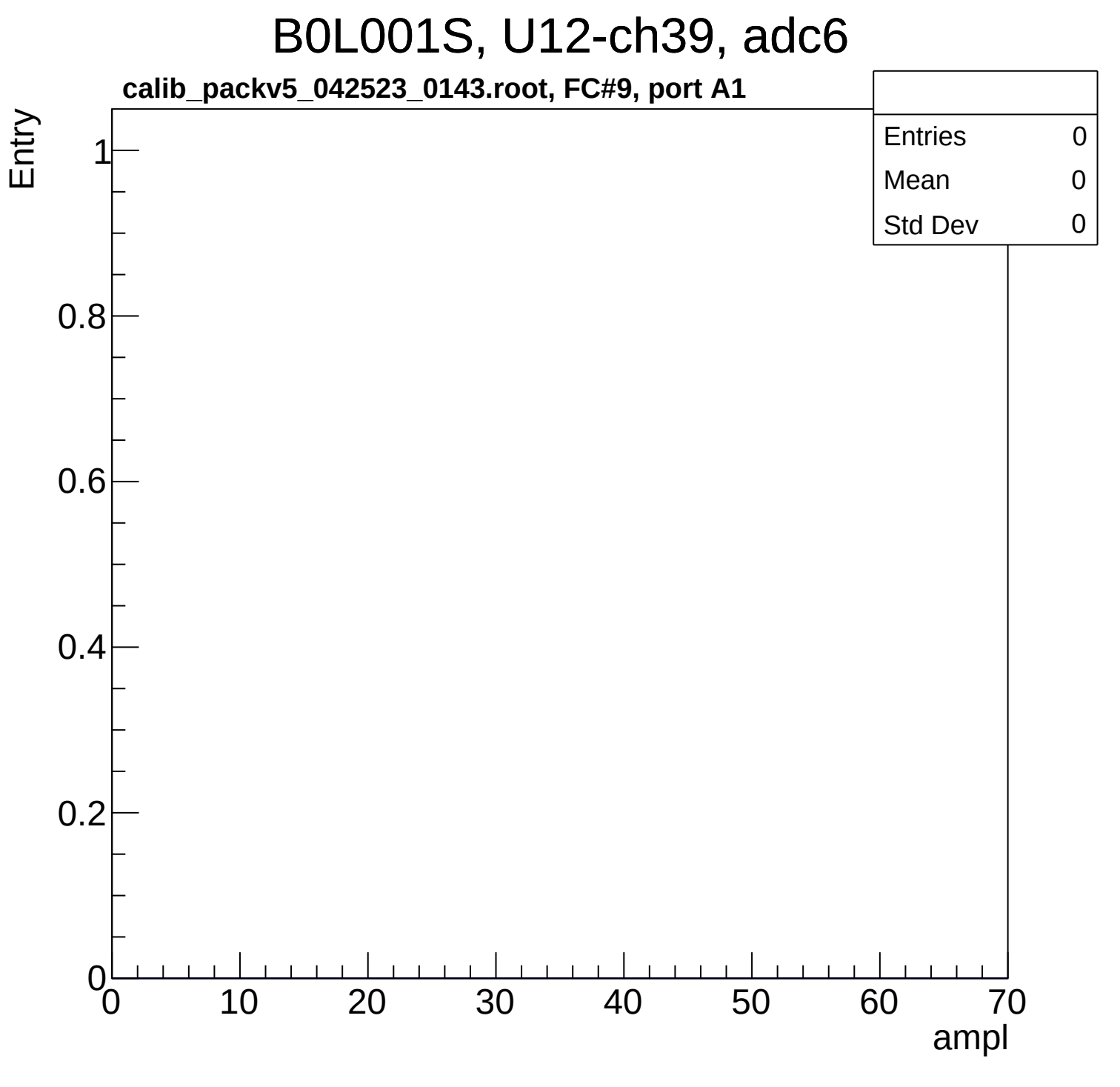
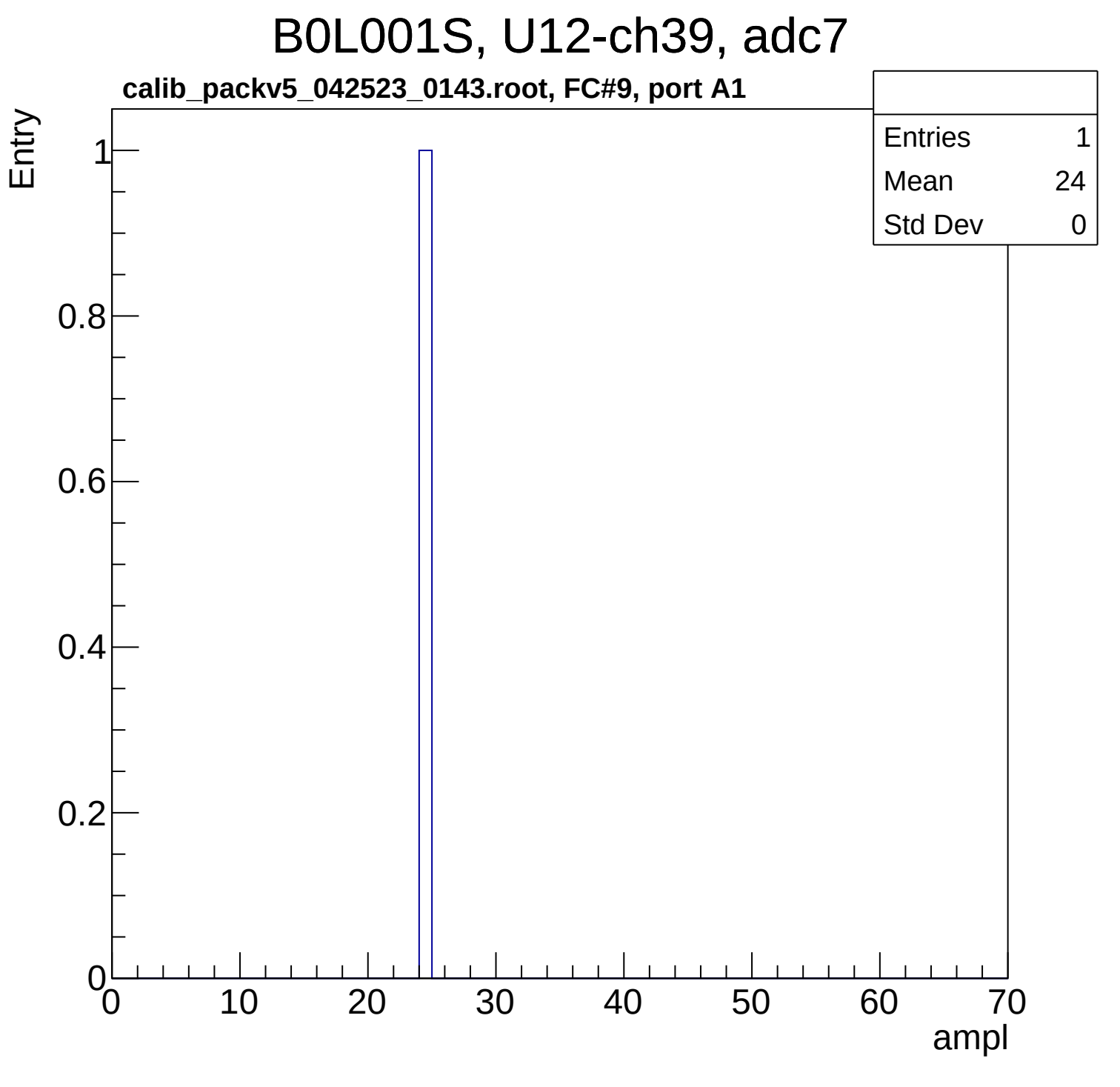
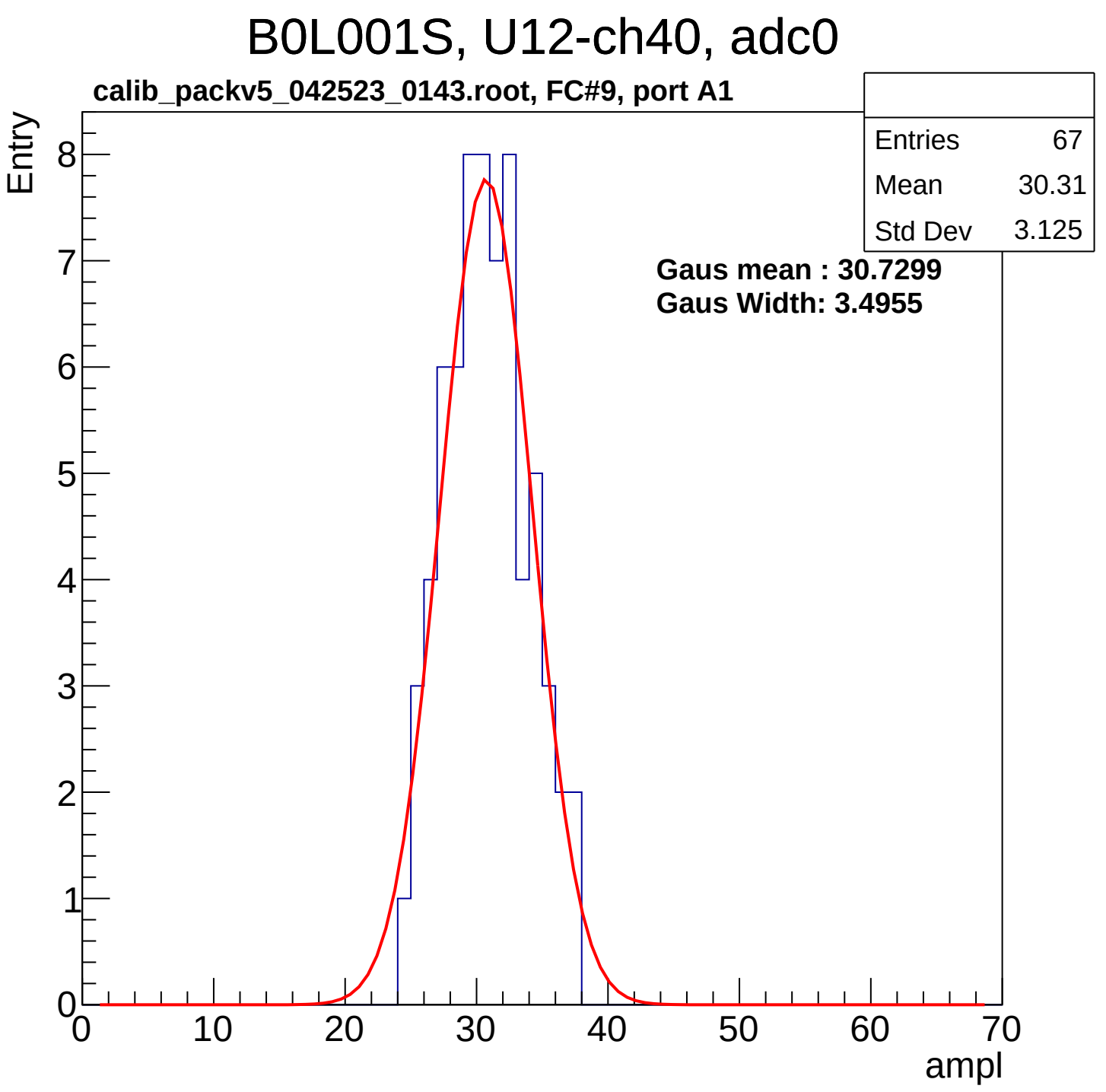
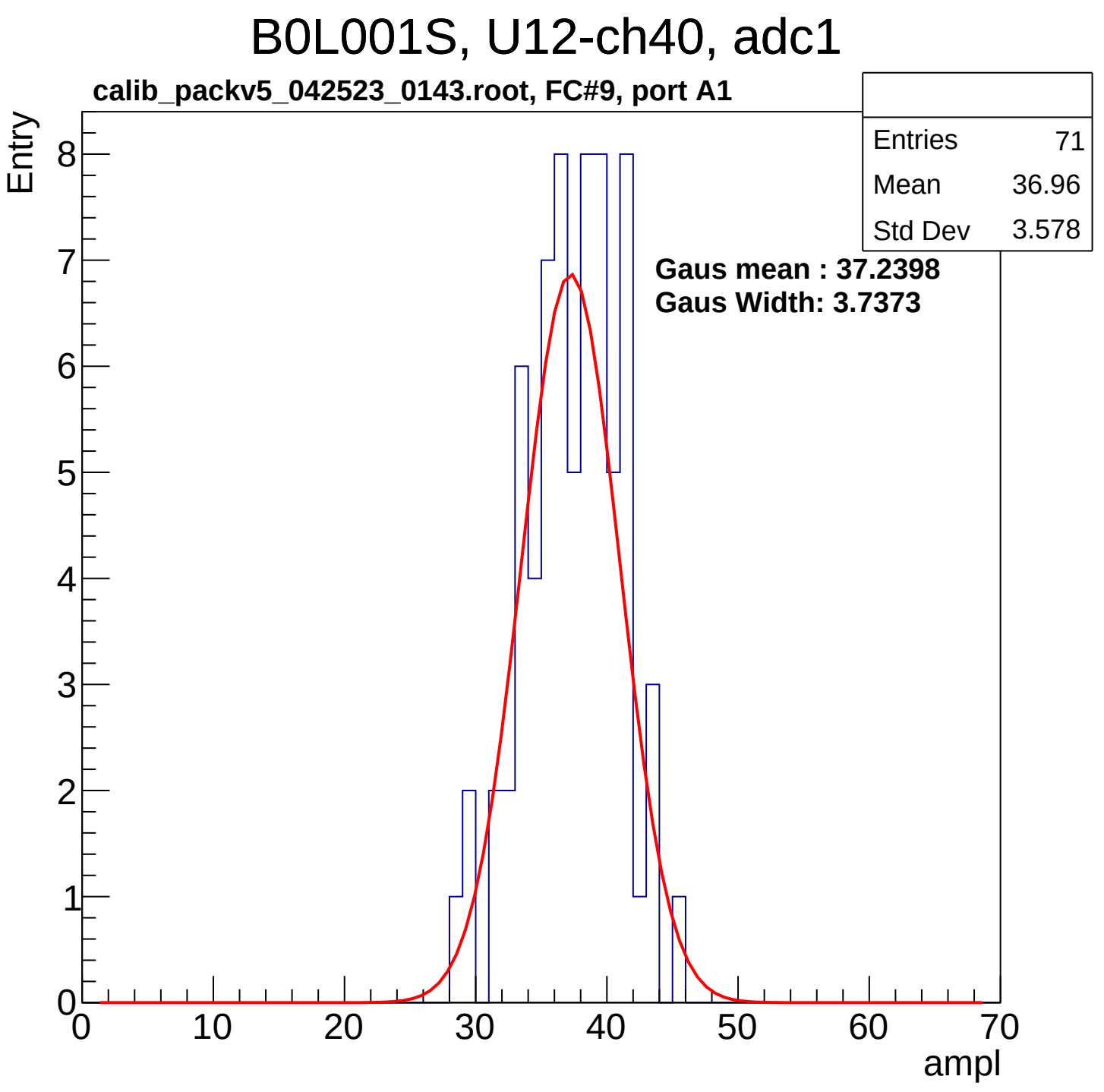

B0L001S, U12-ch39, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 57
Mean 58
Std Dev 3.346
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

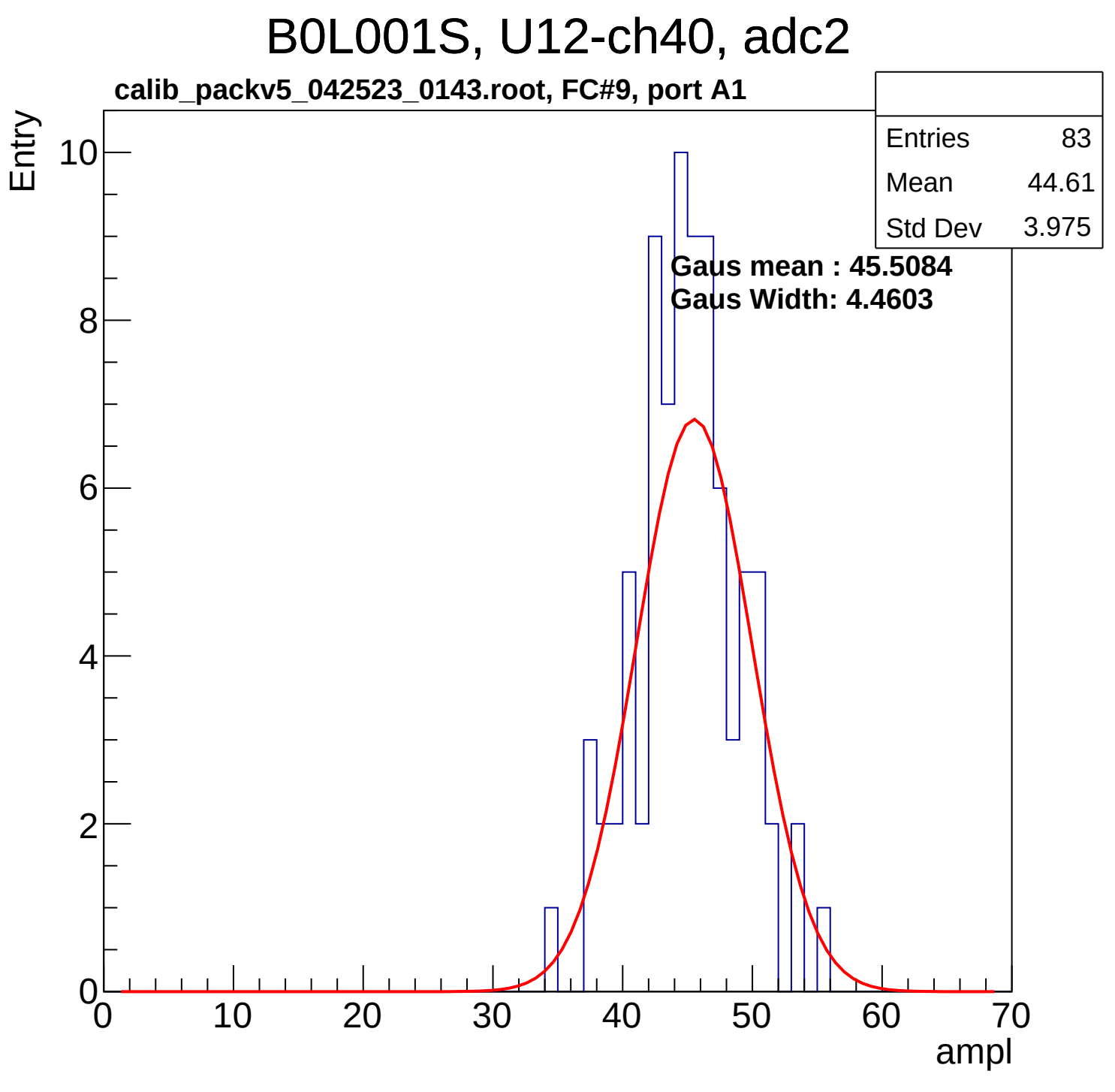

B0L001S, U12-ch39, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 21
Mean 58.48
Std Dev 13.18
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

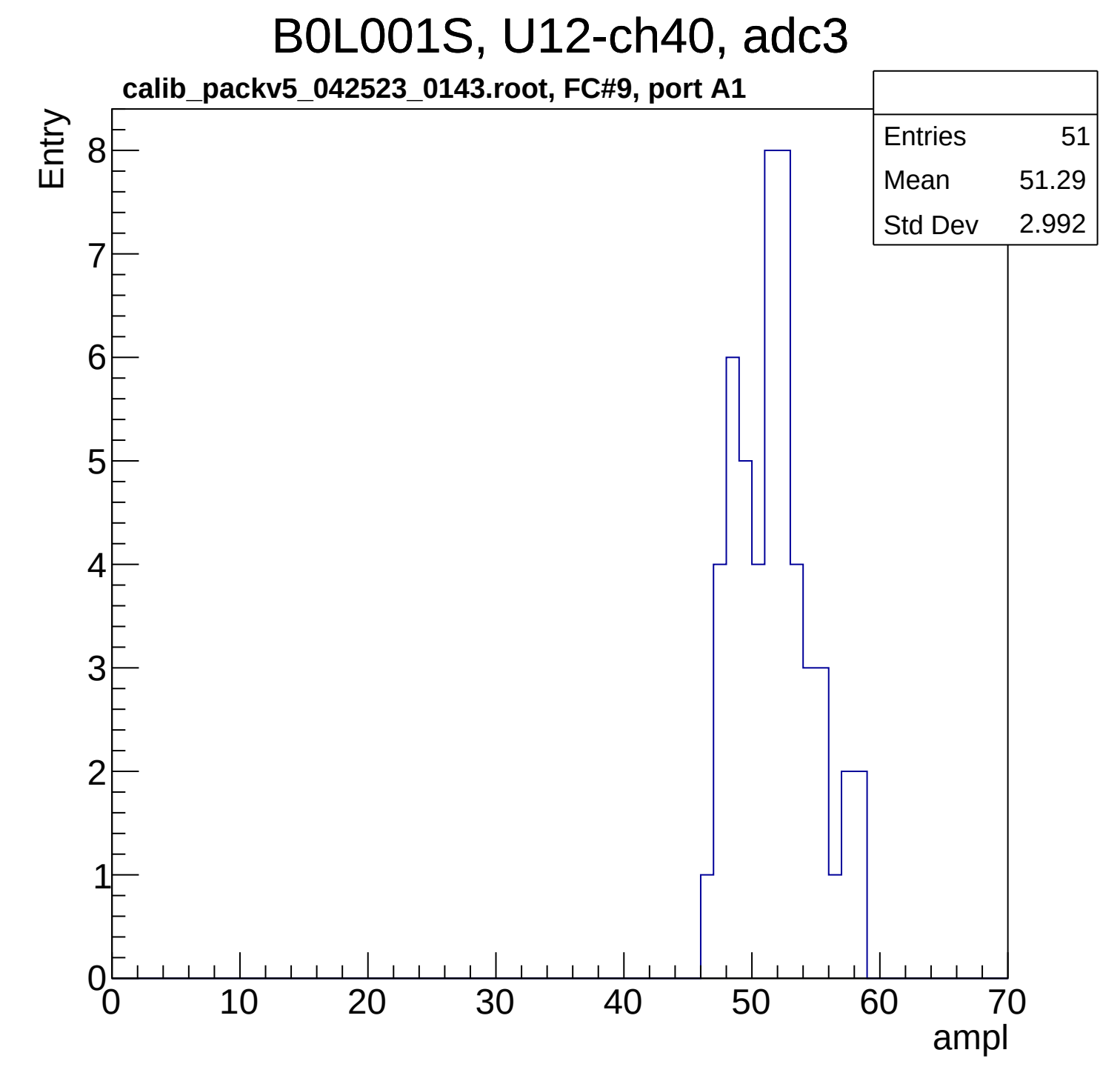

B0L001S, U12-ch39, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch39, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 24
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch40, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 67
Mean 30.31
Std Dev 3.125
Gaus mean : 30.7299
Gaus Width: 3.4955
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch40, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 71
Mean 36.96
Std Dev 3.578
Gaus mean : 37.2398
Gaus Width: 3.7373
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch40, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 83
Mean 44.61
Std Dev 3.975
Gaus mean : 45.5084
Gaus Width: 4.4603
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch40, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 51
Mean 51.29
Std Dev 2.992
Entry
ampl
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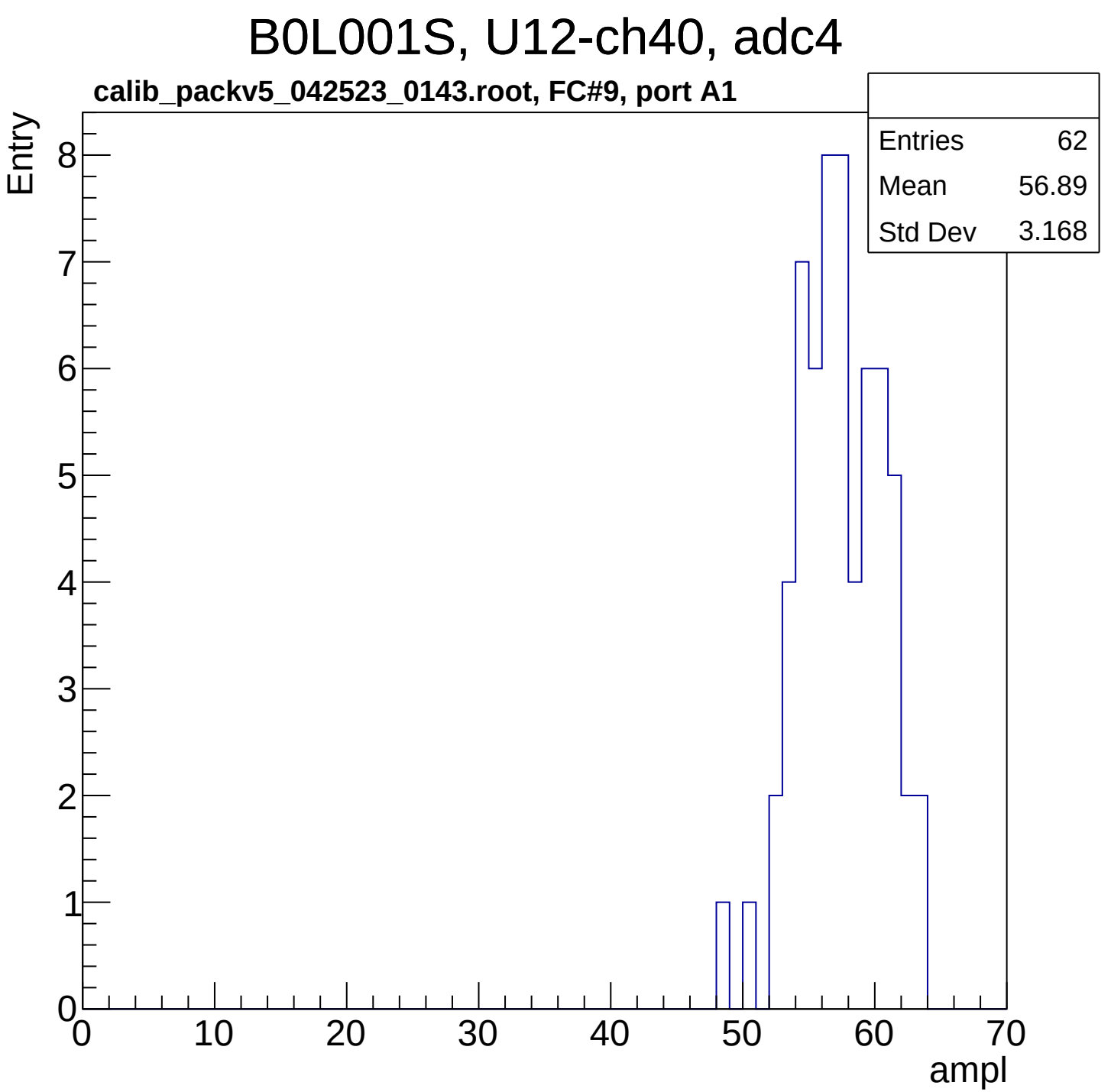
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch40, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 62
Mean 56.89
Std Dev 3.168
Entry
ampl
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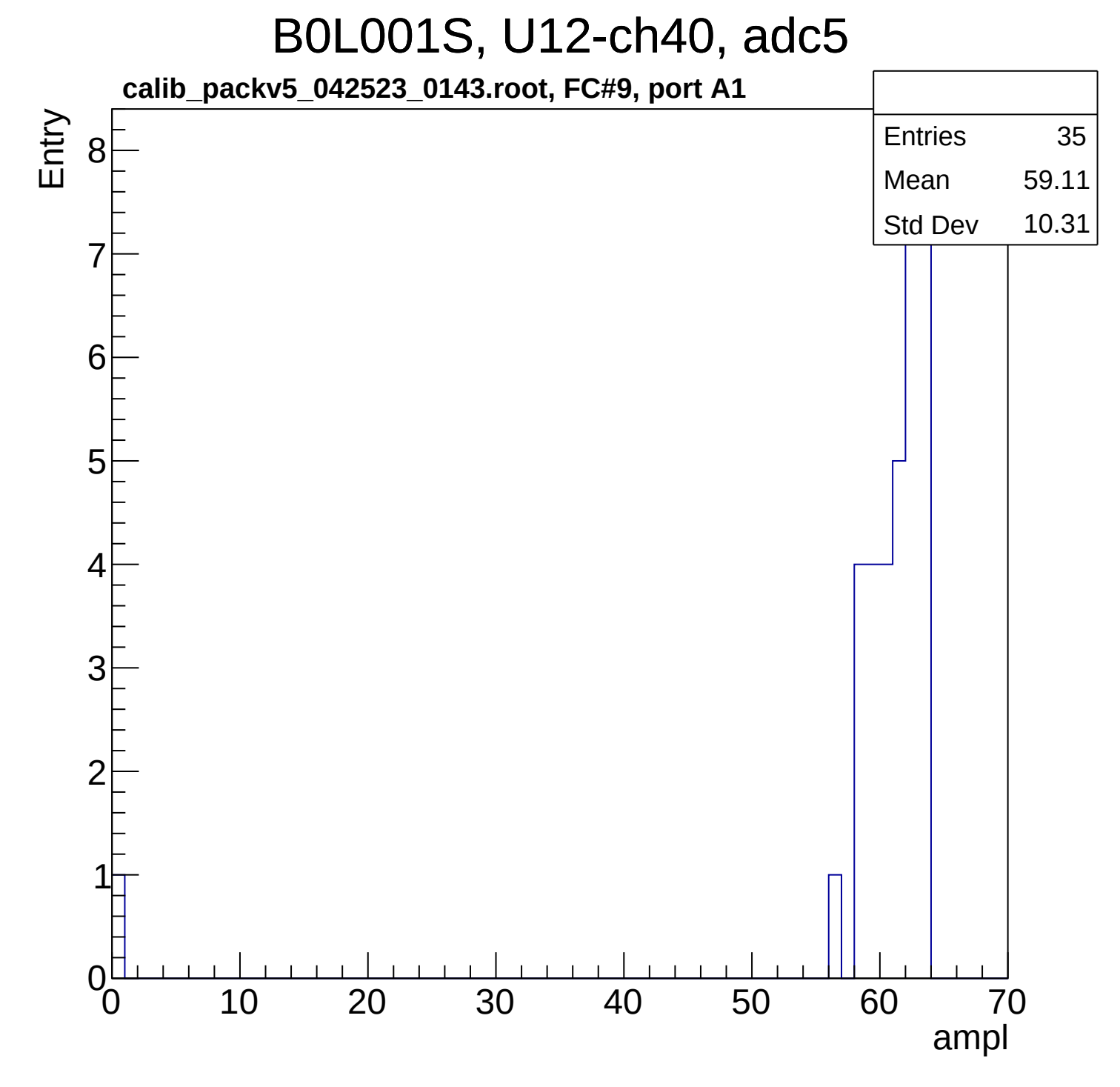
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch40, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 35
Mean 59.11
Std Dev 10.31
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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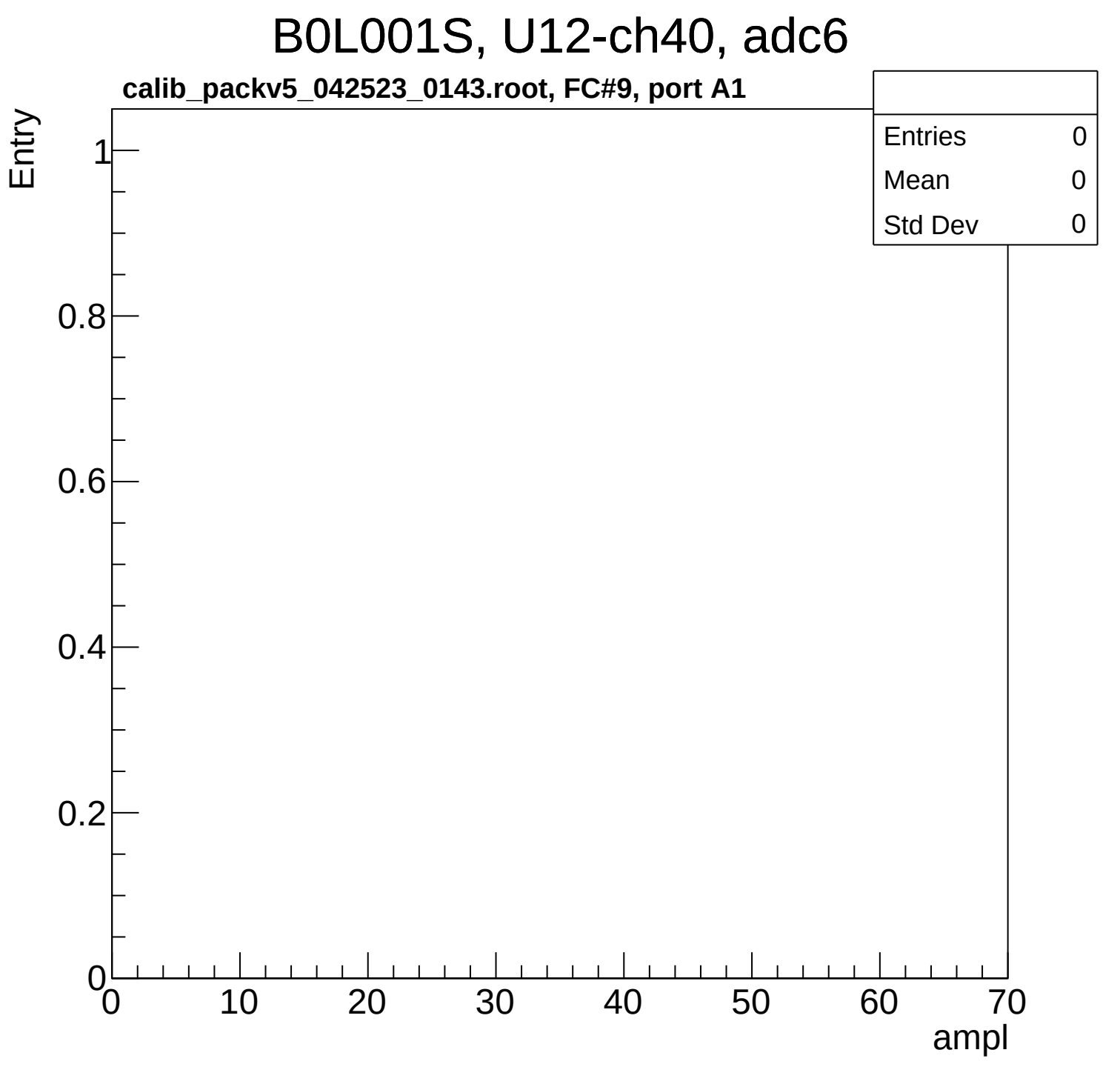
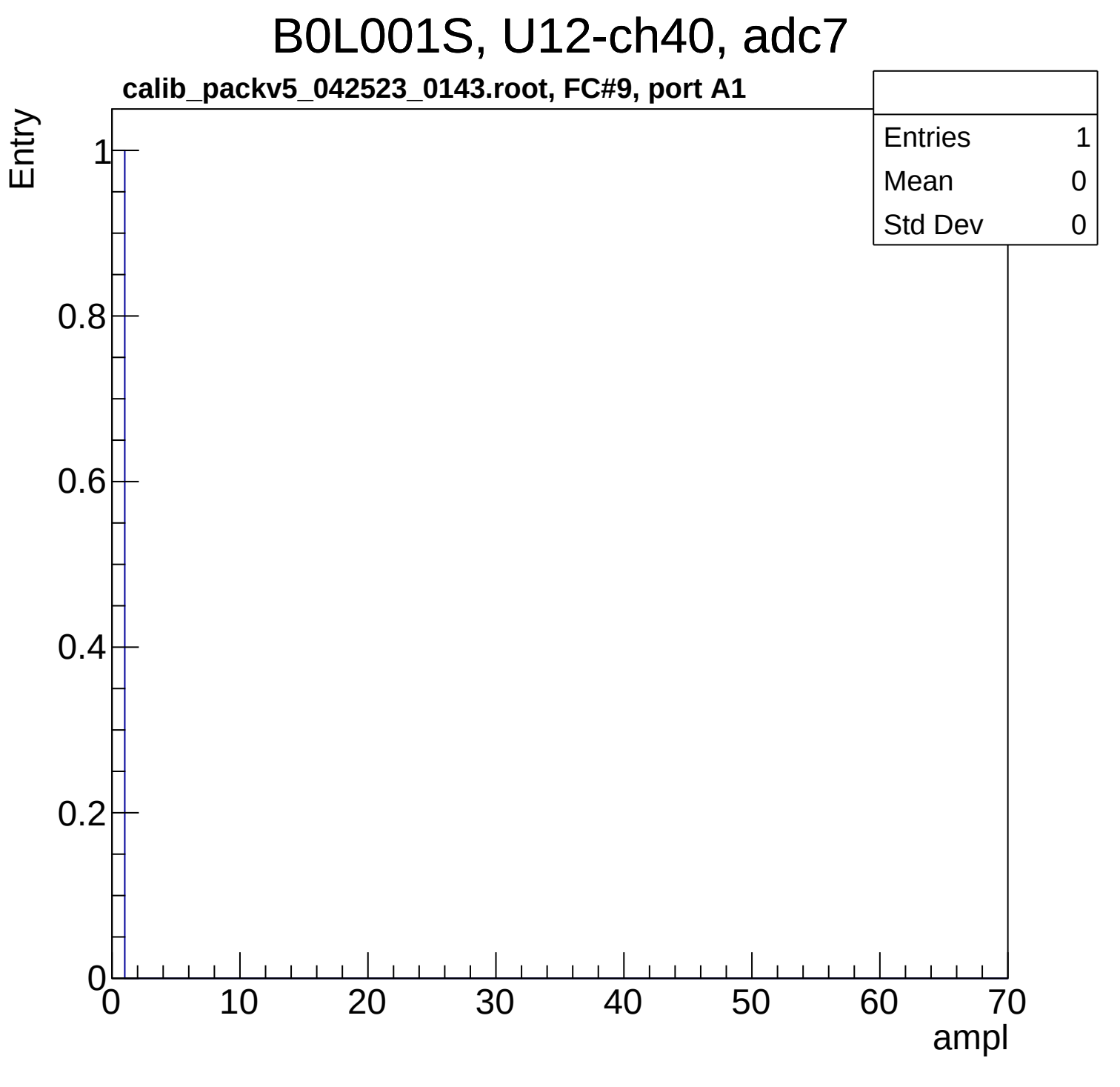
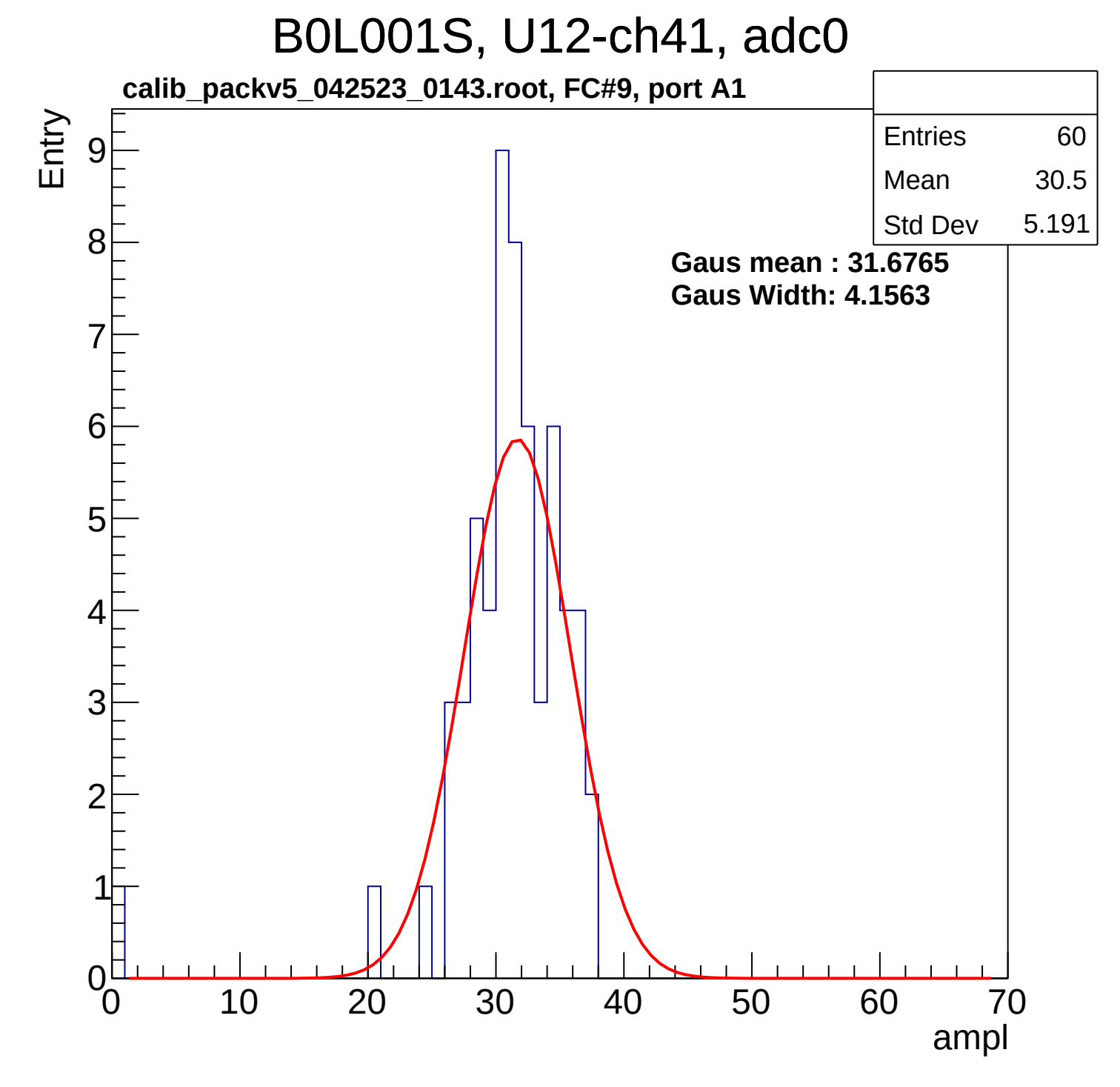

B0L001S, U12-ch40, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch40, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch41, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 60
Mean 30.5
Std Dev 5.191
Gaus mean : 31.6765
Gaus Width: 4.1563
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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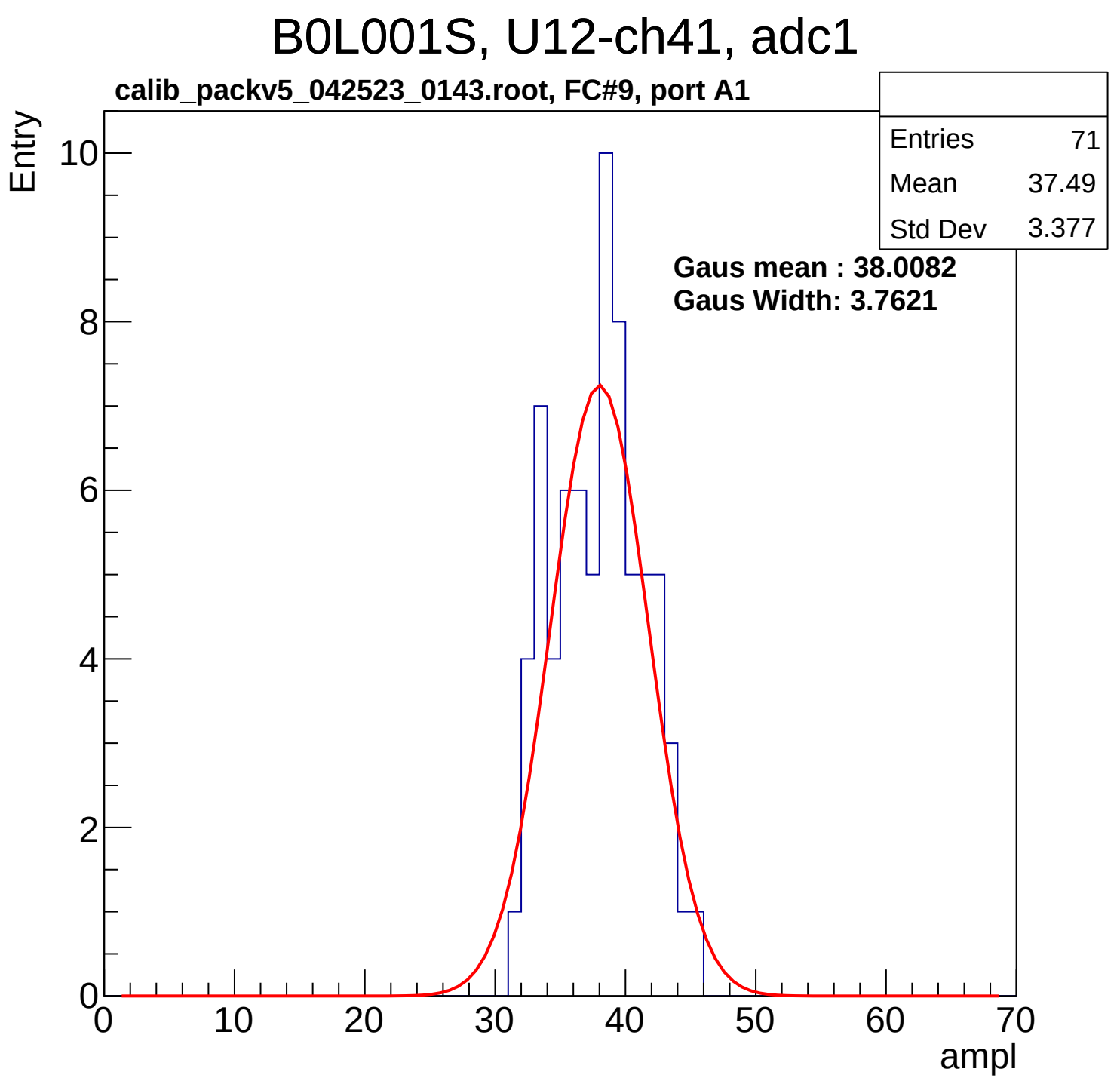
60
70


B0L001S, U12-ch41, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 71
Mean 37.49
Std Dev 3.377
Gaus mean : 38.0082
Gaus Width: 3.7621
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
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60
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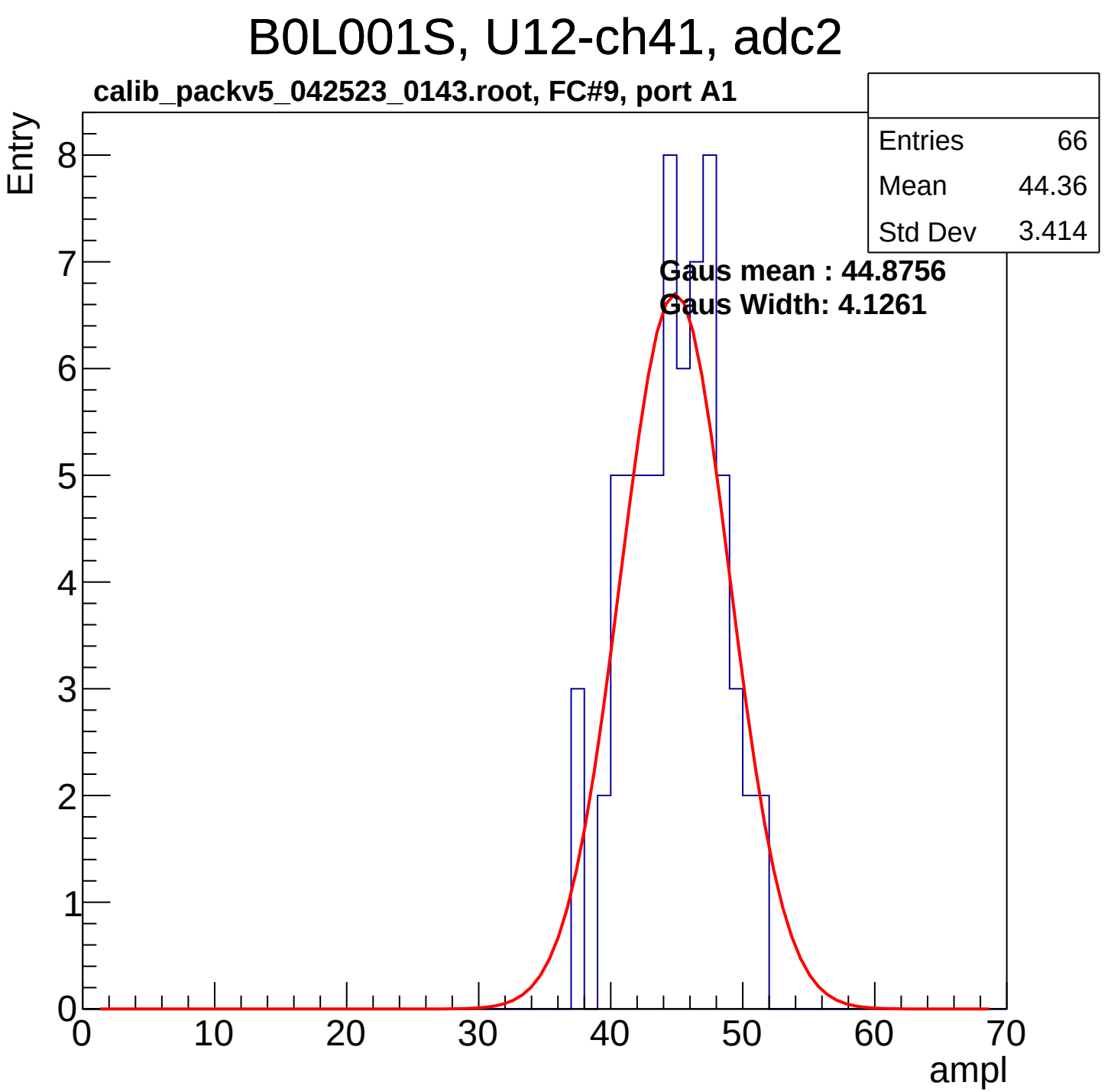
B0L001S, U12-ch41, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 66
Mean 44.36
Std Dev 3.414
Gaus mean : 44.8756
Gaus Width: 4.1261
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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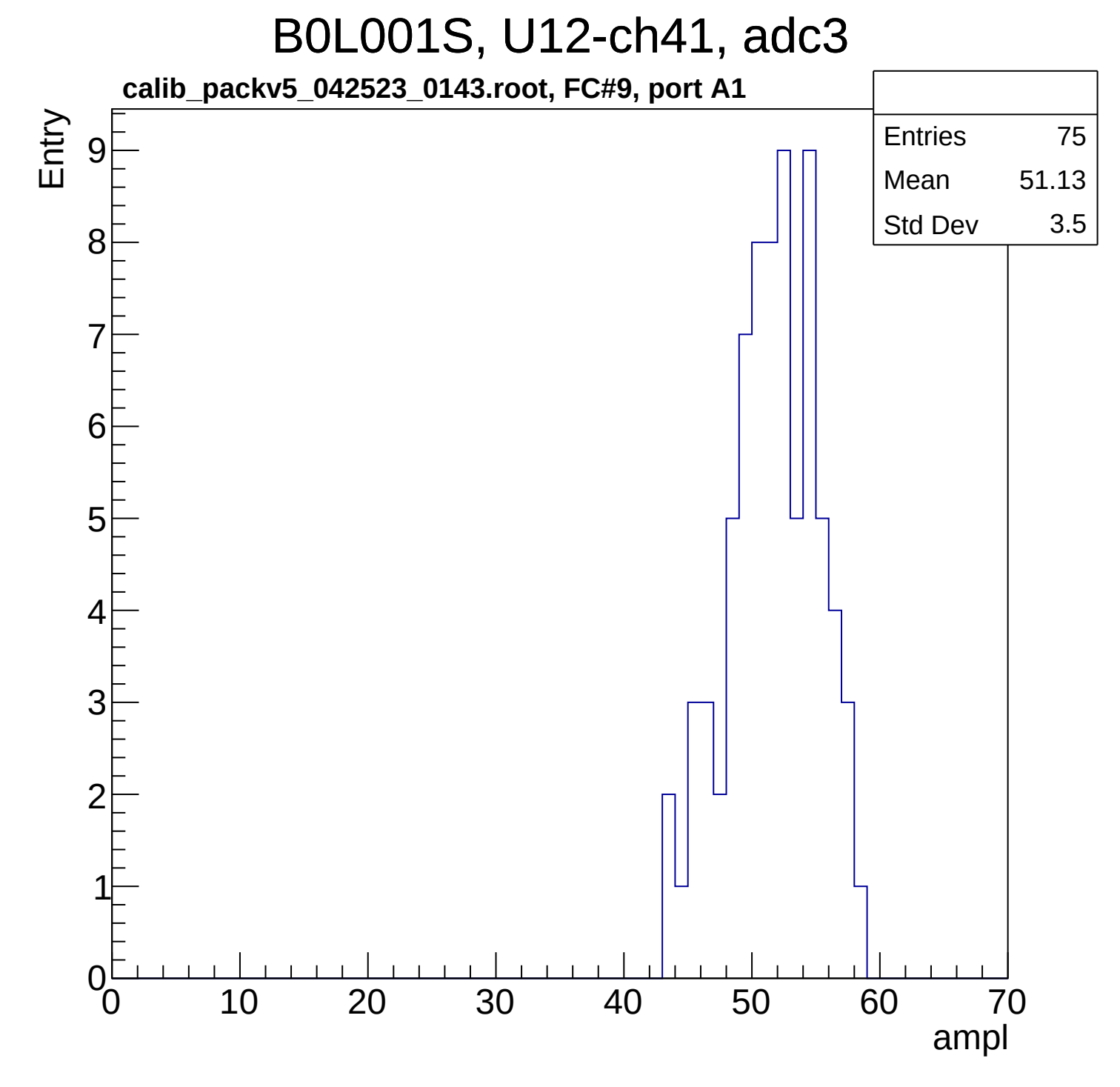
40
50
60
70


B0L001S, U12-ch41, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 75
Mean 51.13
Std Dev 3.5
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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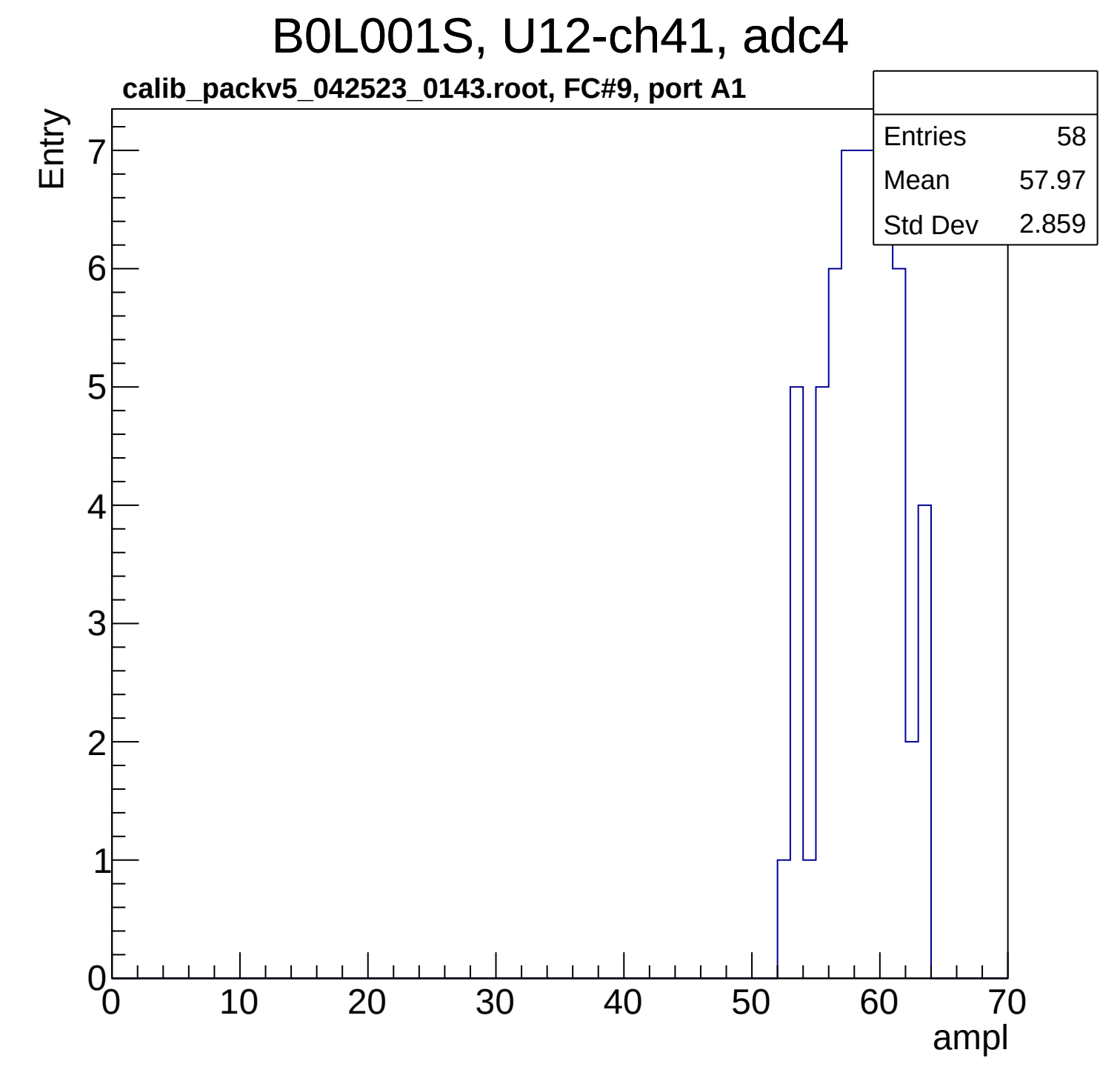
40
50
60
70


B0L001S, U12-ch41, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 58
Mean 57.97
Std Dev 2.859
Entry
ampl
0
1
2
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4
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6
7
0
10
20
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40
50
60
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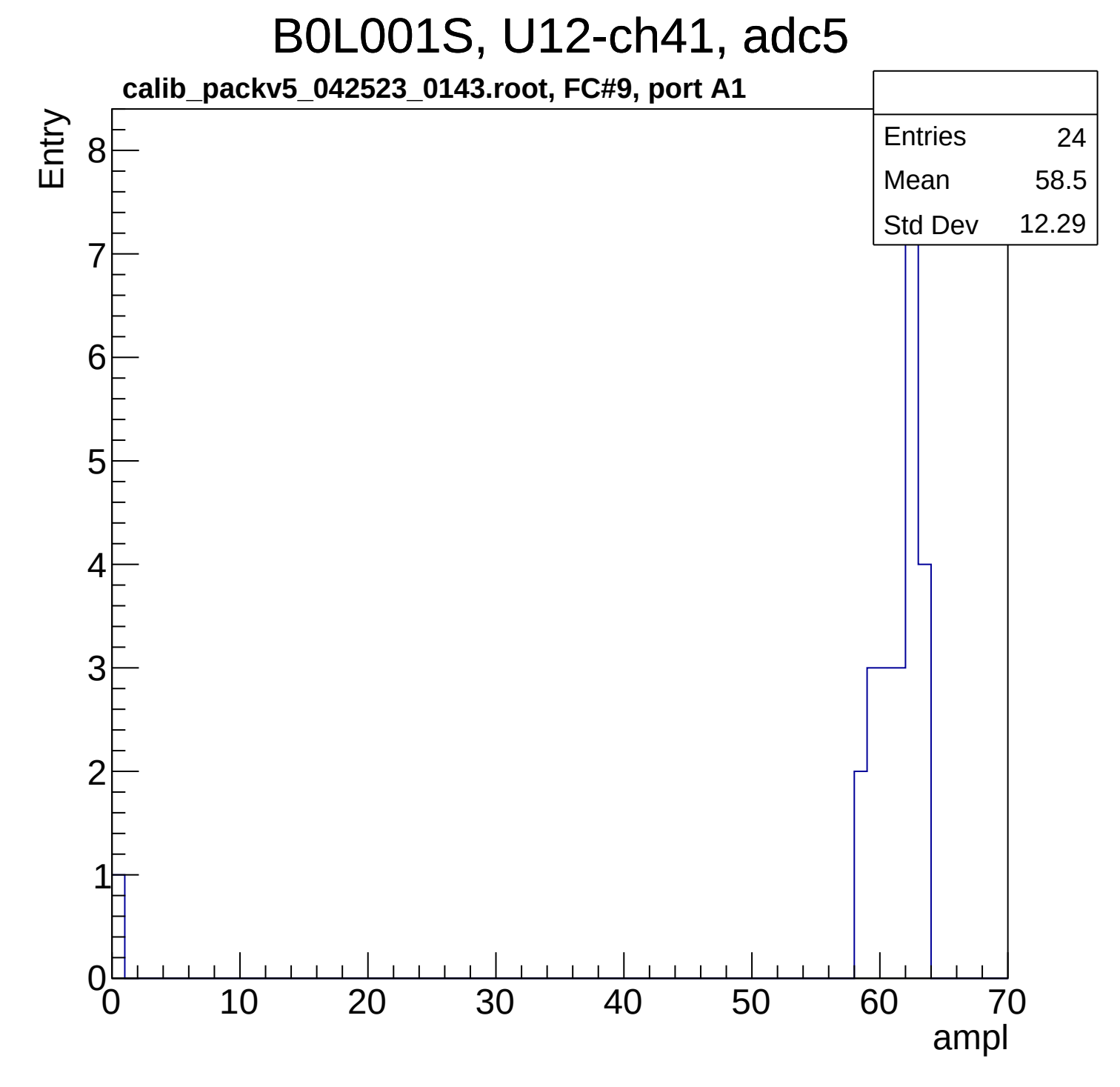
B0L001S, U12-ch41, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 24
Mean 58.5
Std Dev 12.29
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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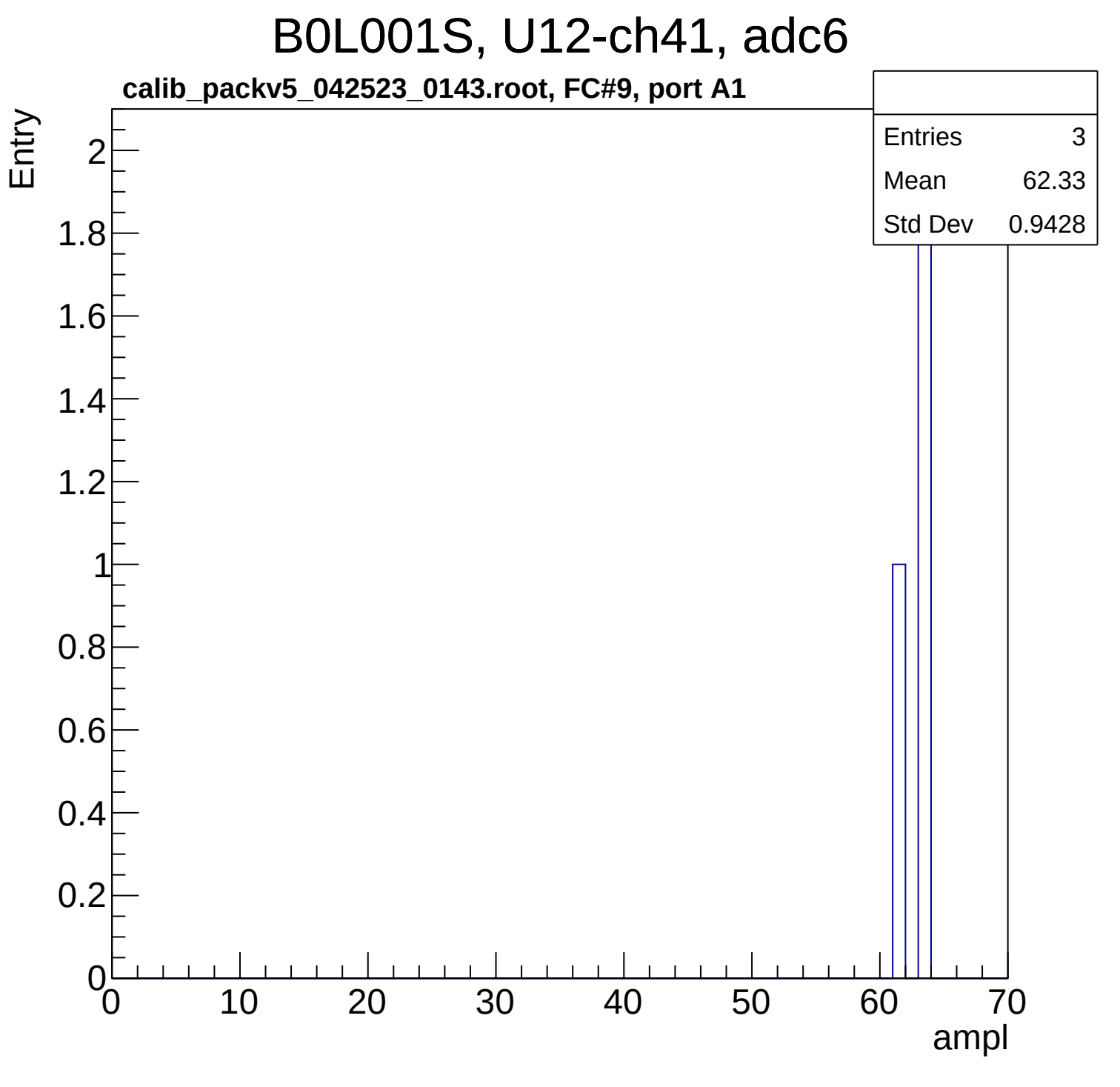
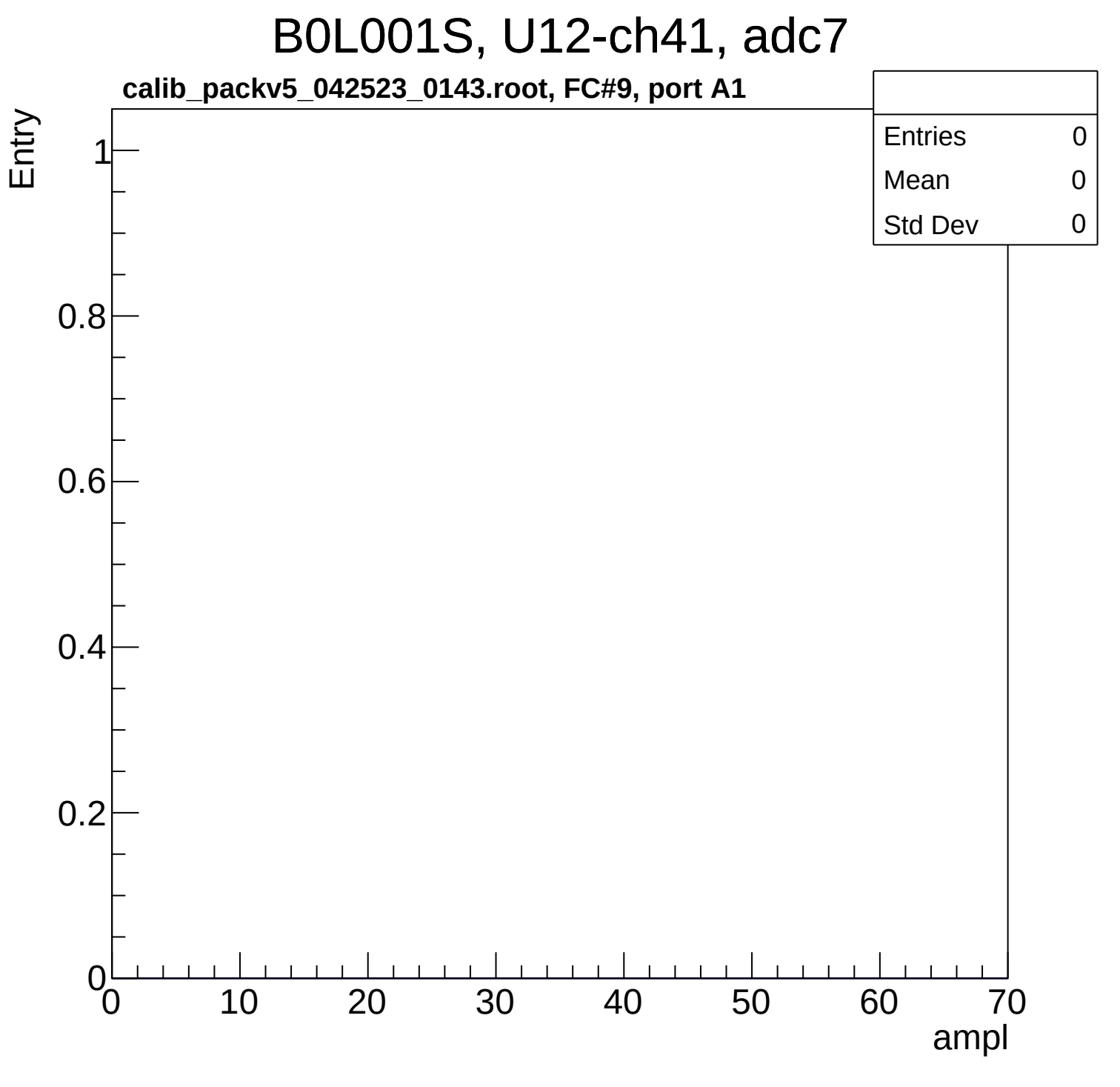
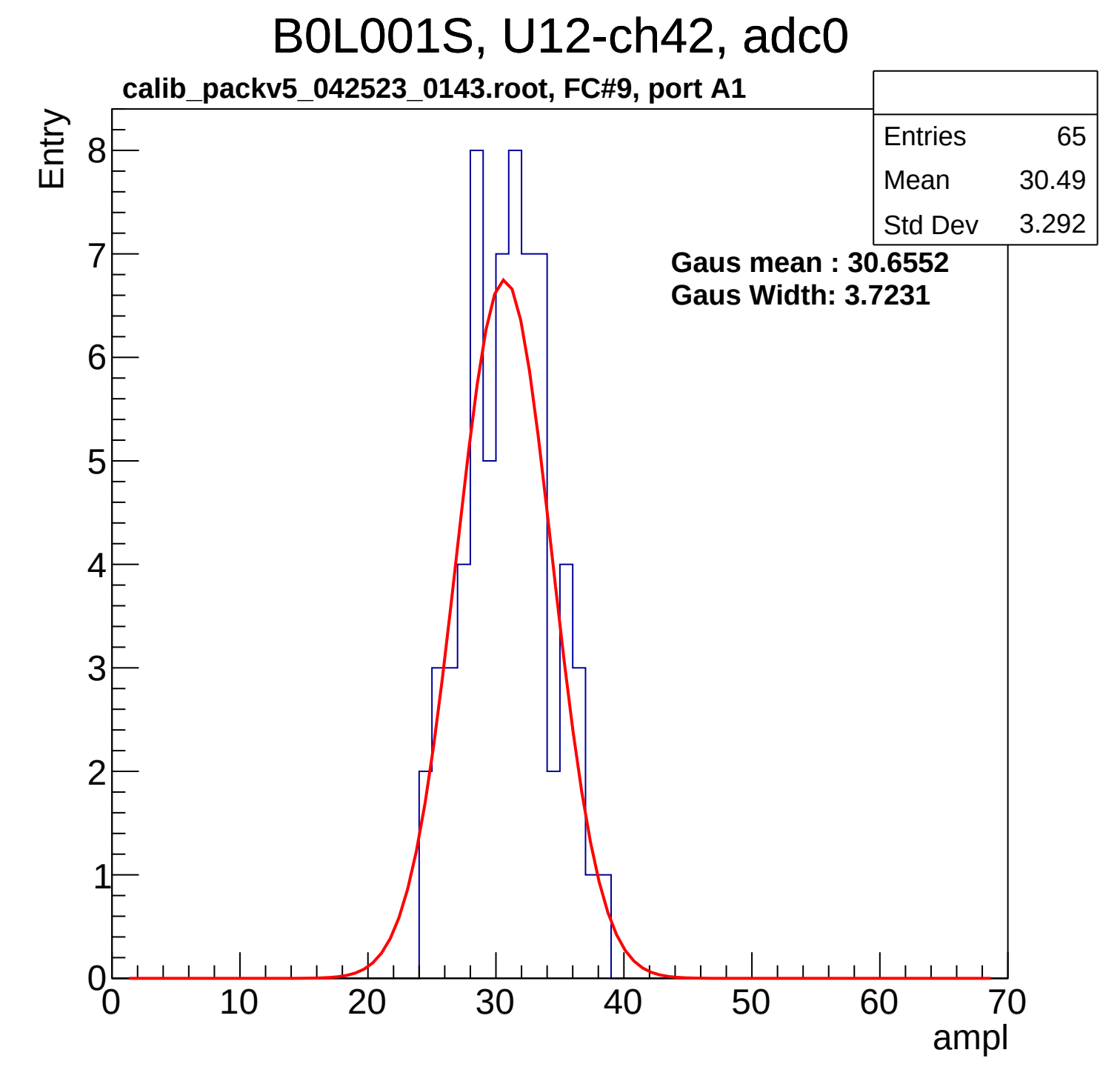

B0L001S, U12-ch41, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 3
Mean 62.33
Std Dev 0.9428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L001S, U12-ch41, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch42, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 65
Mean 30.49
Std Dev 3.292
Gaus mean : 30.6552
Gaus Width: 3.7231
Entry
ampl
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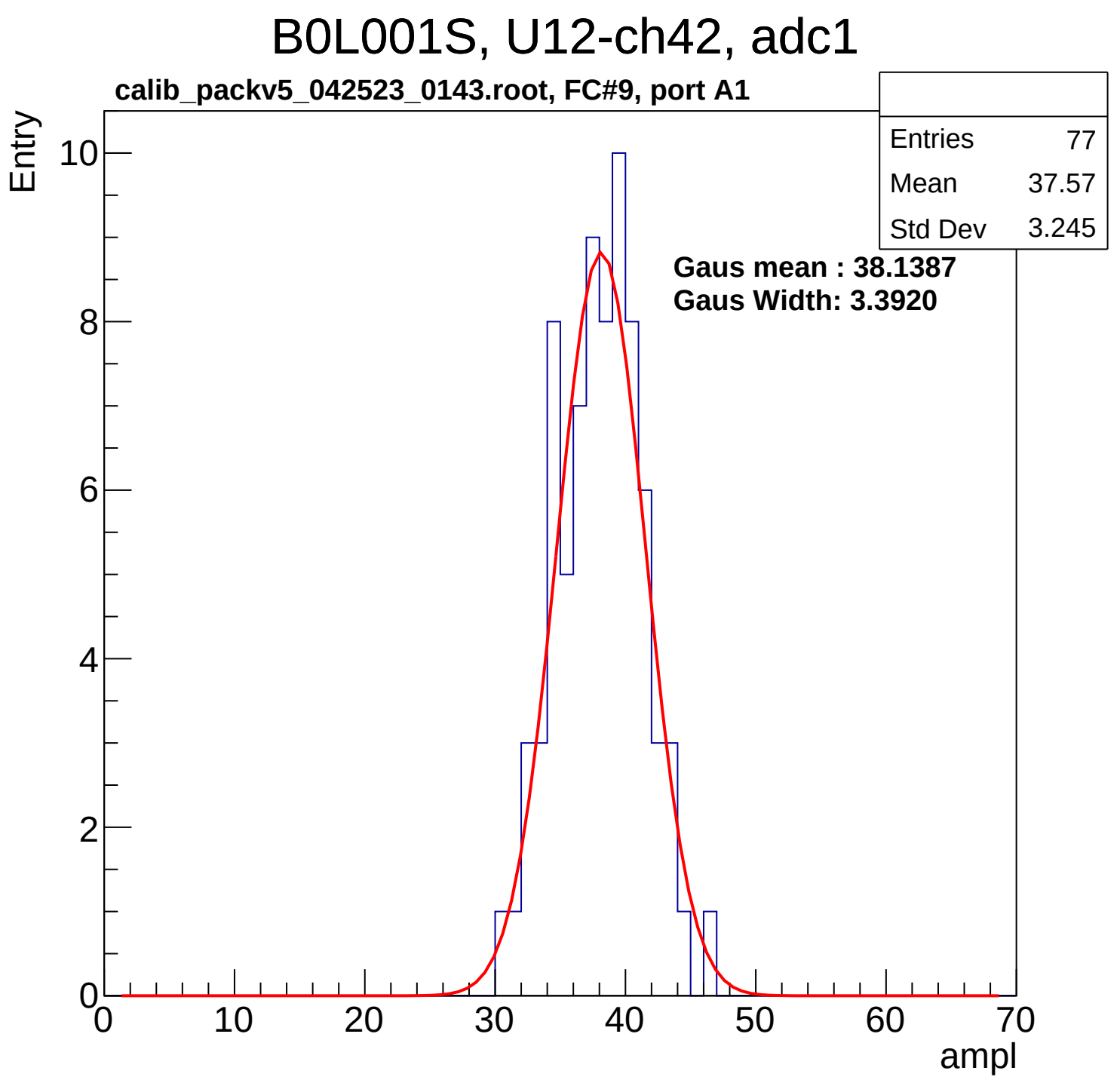
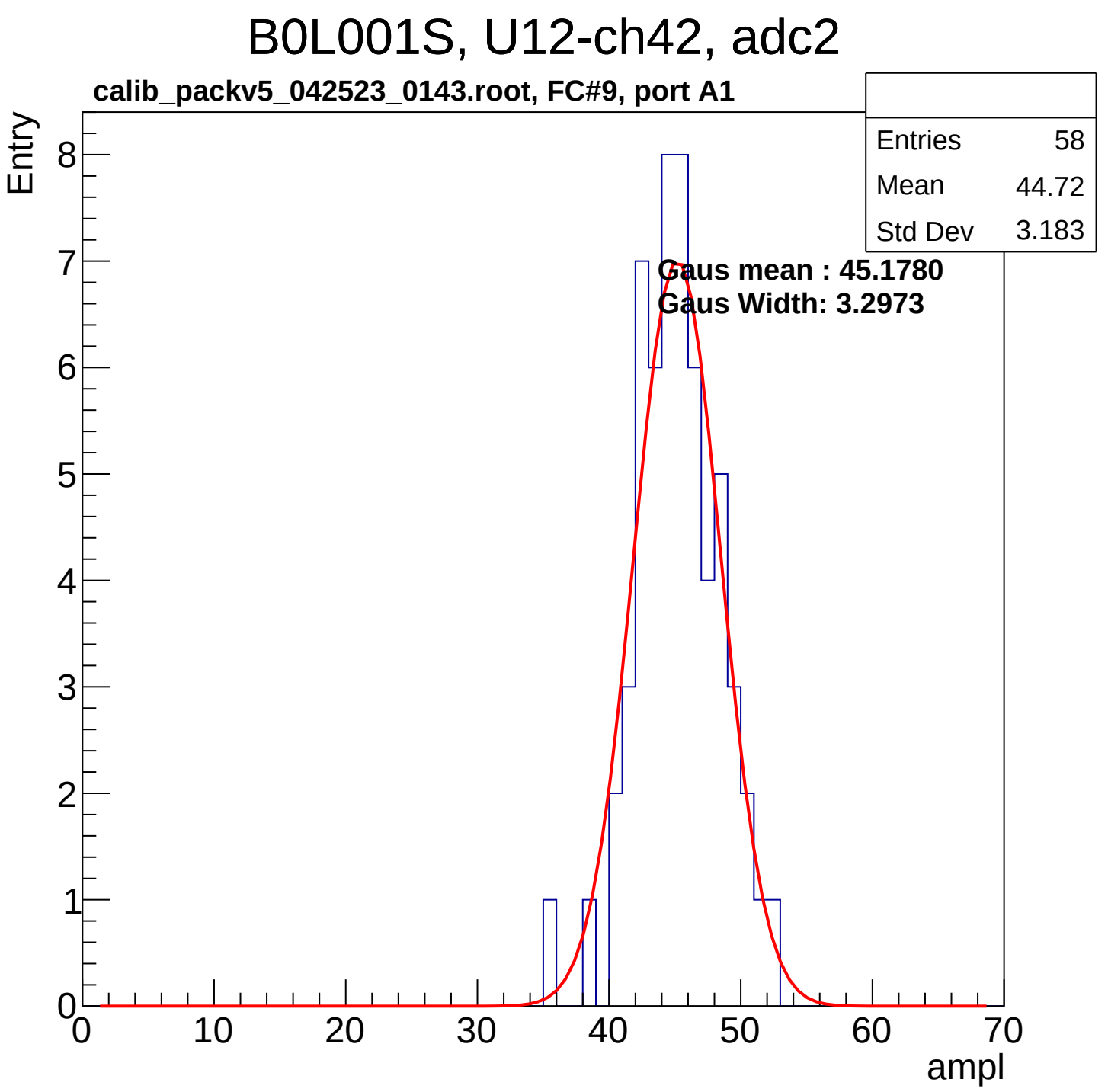
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch42, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 77
Mean 37.57
Std Dev 3.245
Gaus mean : 38.1387
Gaus Width: 3.3920
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch42, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 58
Mean 44.72
Std Dev 3.183
Gaus mean : 45.1780
Gaus Width: 3.2973
Entry
ampl
0
1
2
3
4
5
6
7
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0
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20
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40
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60
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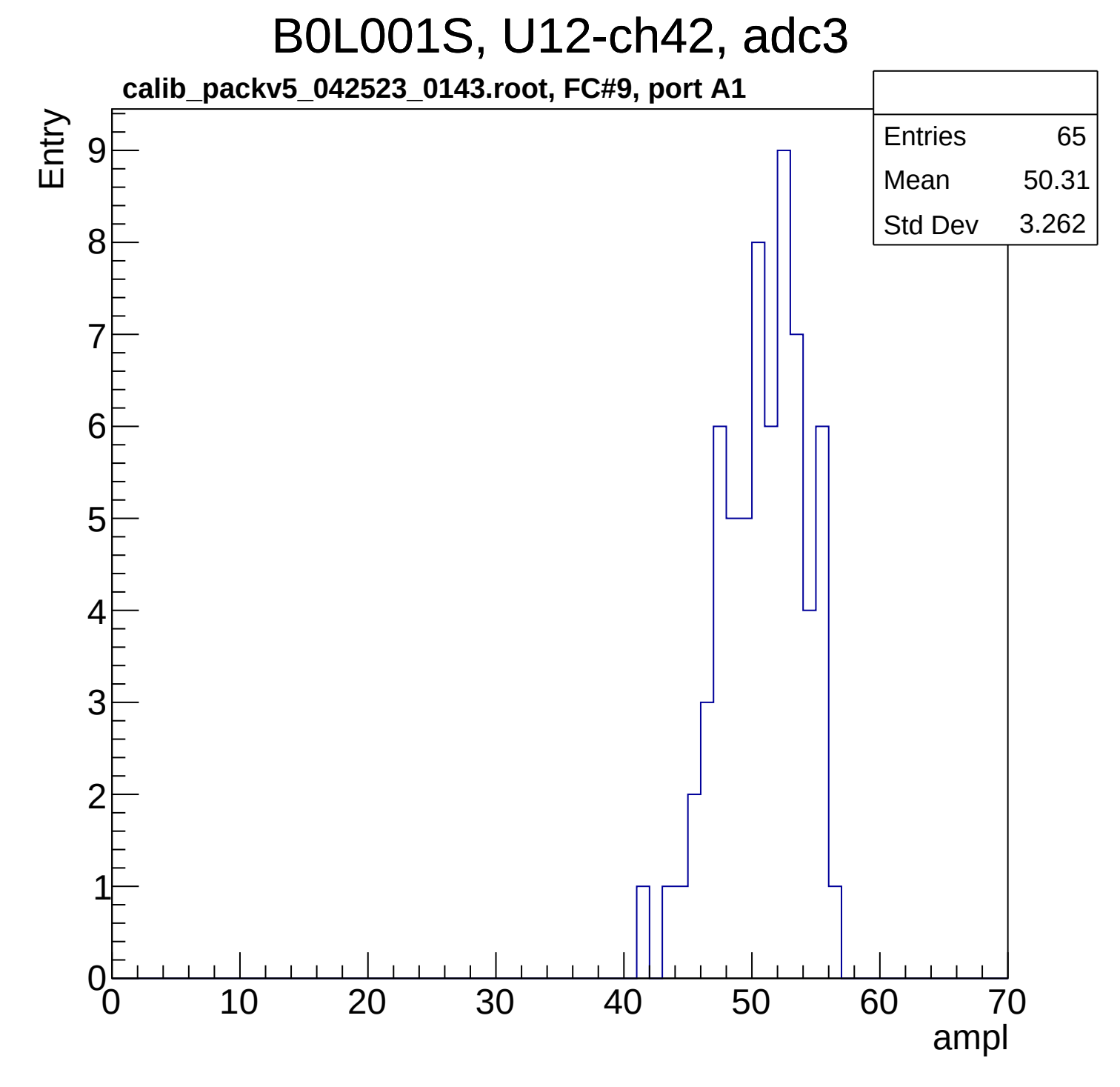
B0L001S, U12-ch42, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 65
Mean 50.31
Std Dev 3.262
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
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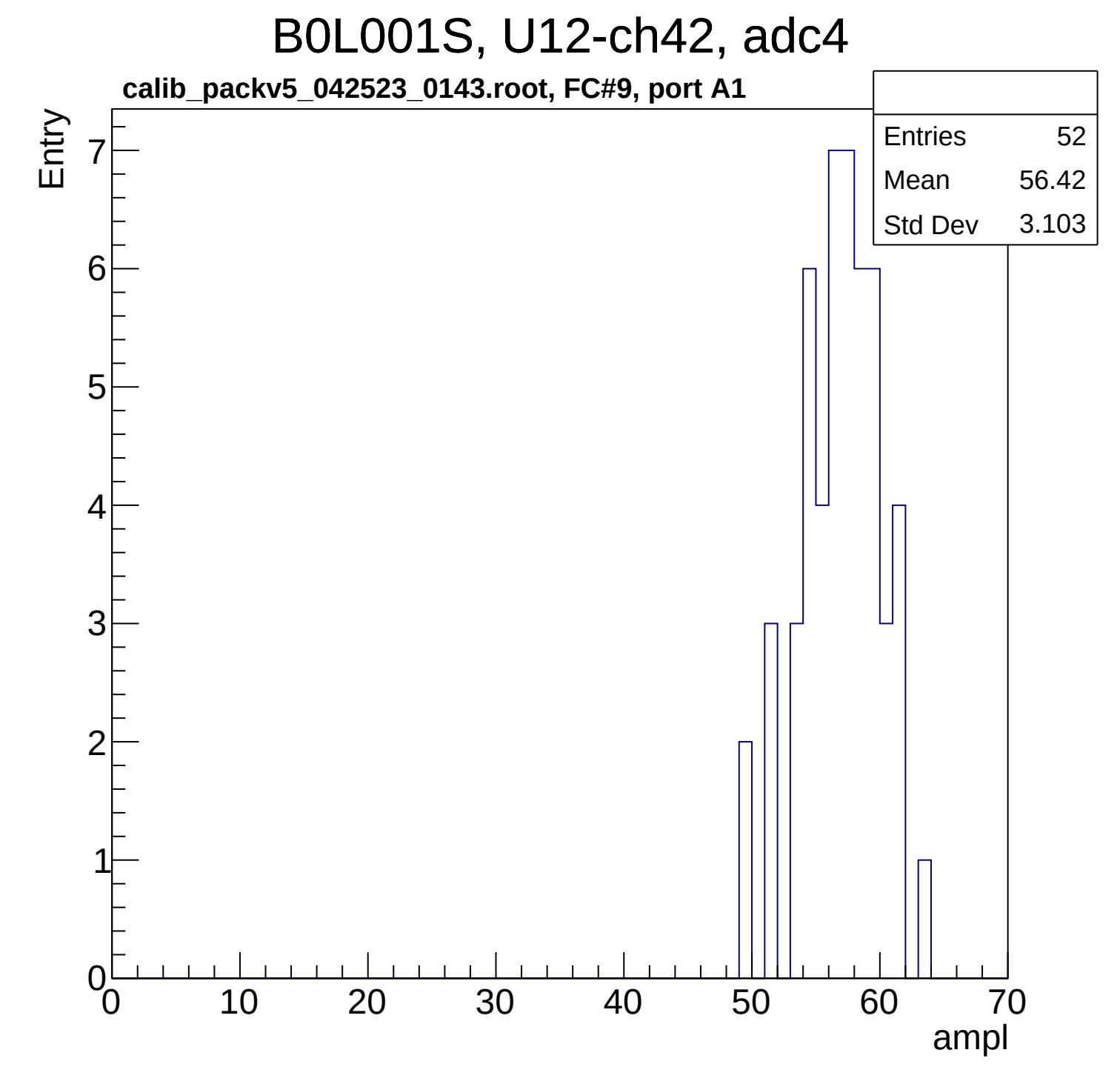
B0L001S, U12-ch42, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 52
Mean 56.42
Std Dev 3.103
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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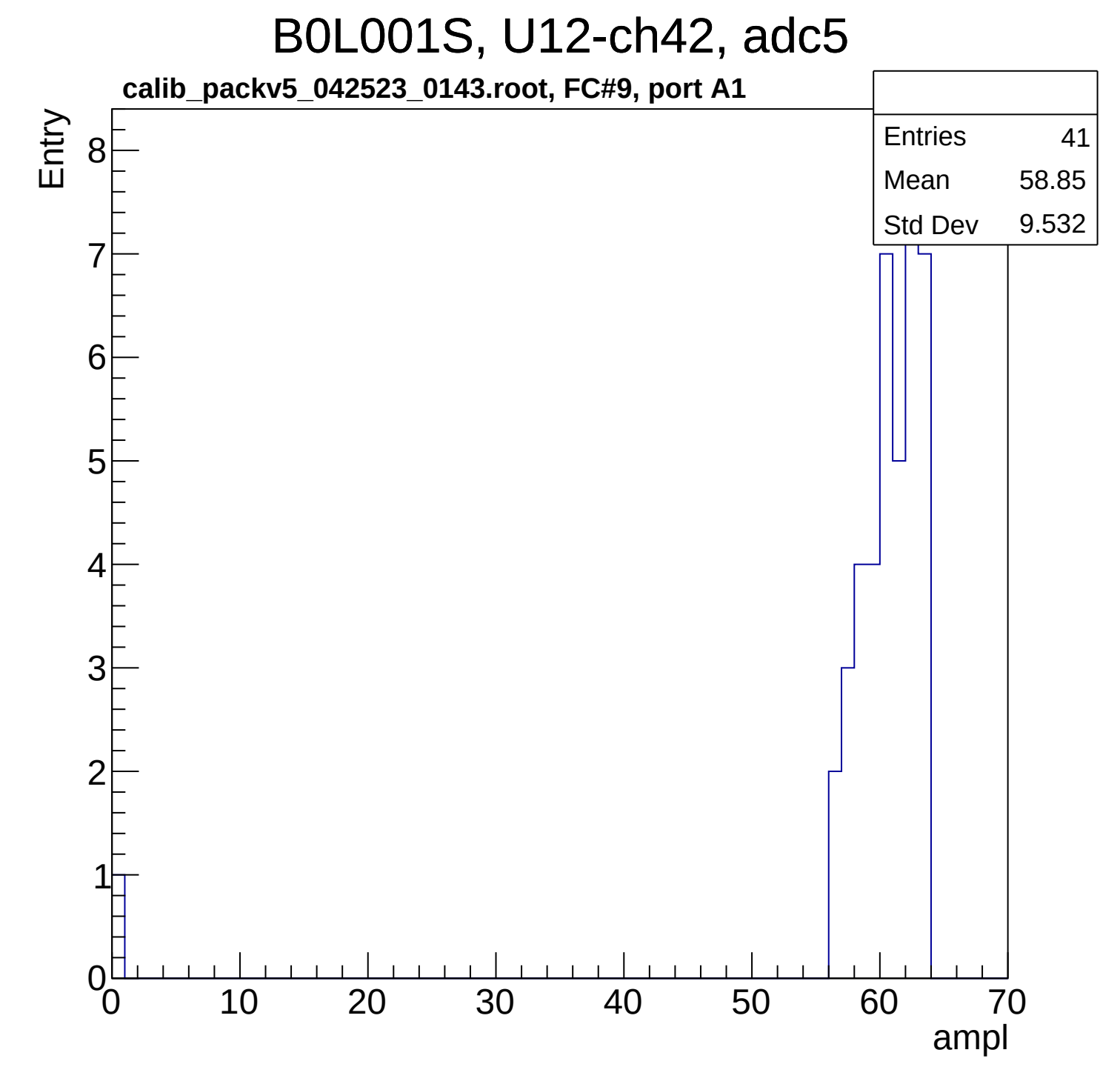
B0L001S, U12-ch42, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 41
Mean 58.85
Std Dev 9.532
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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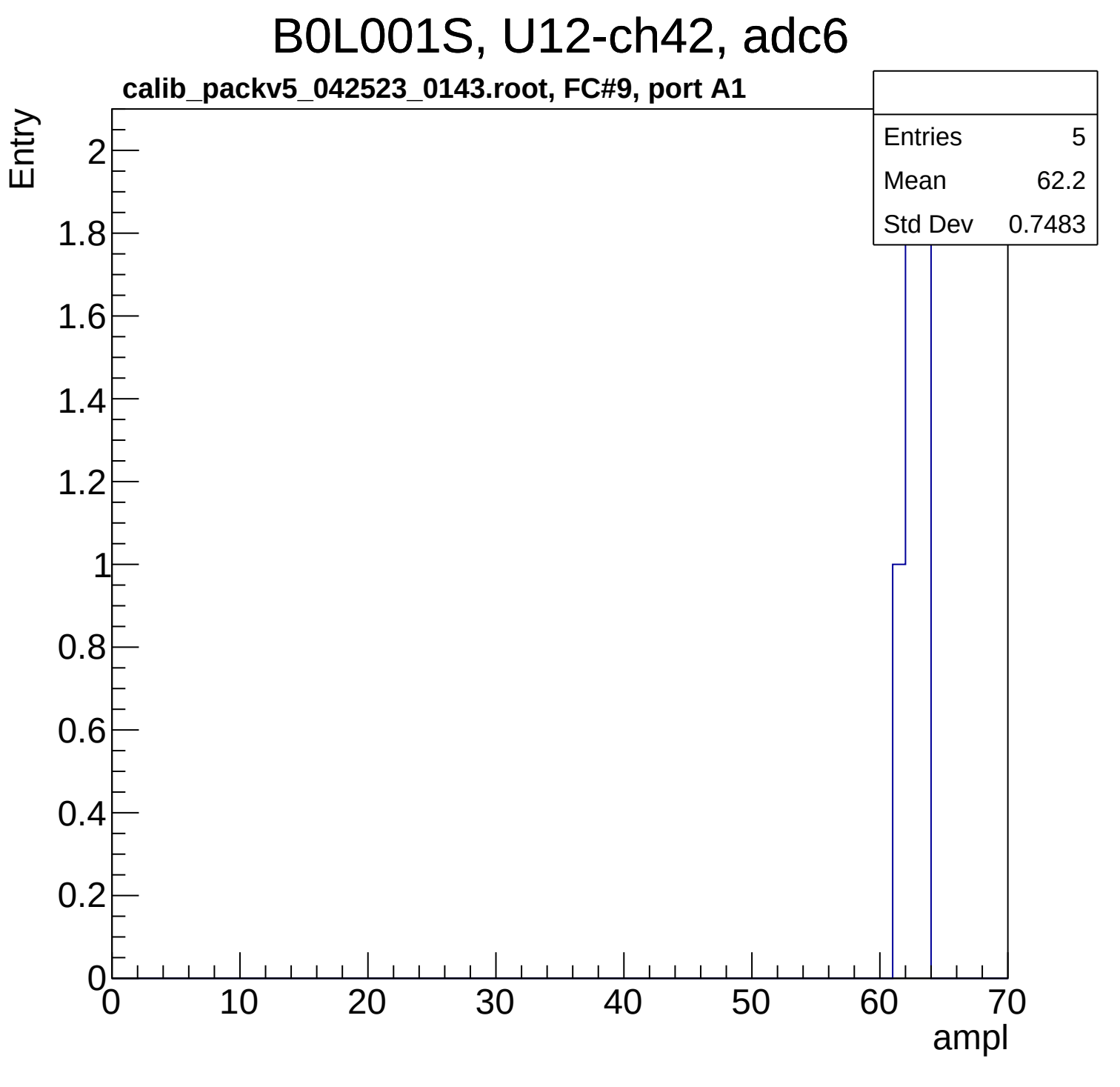
B0L001S, U12-ch42, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 5
Mean 62.2
Std Dev 0.7483
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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40
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60
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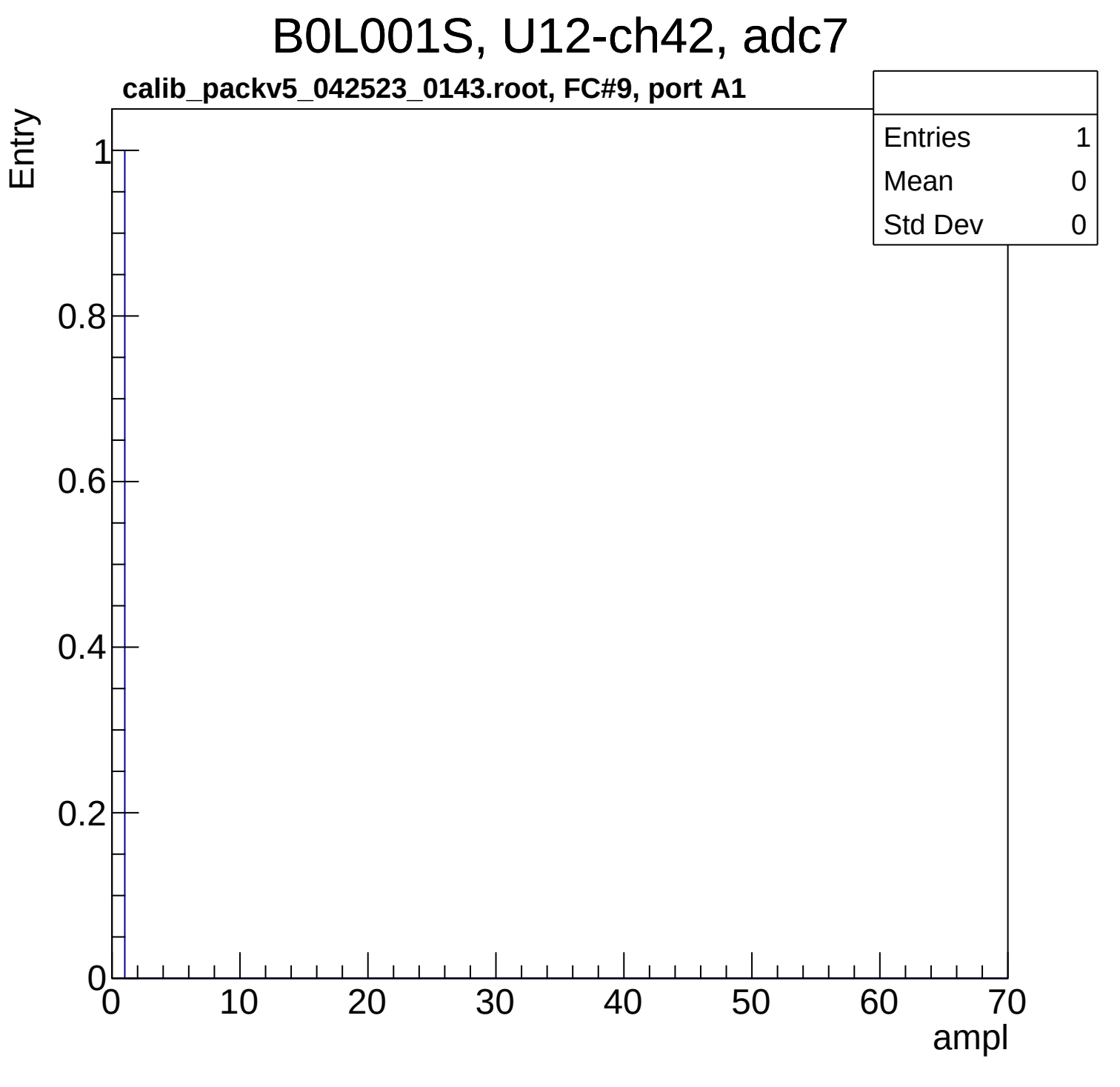
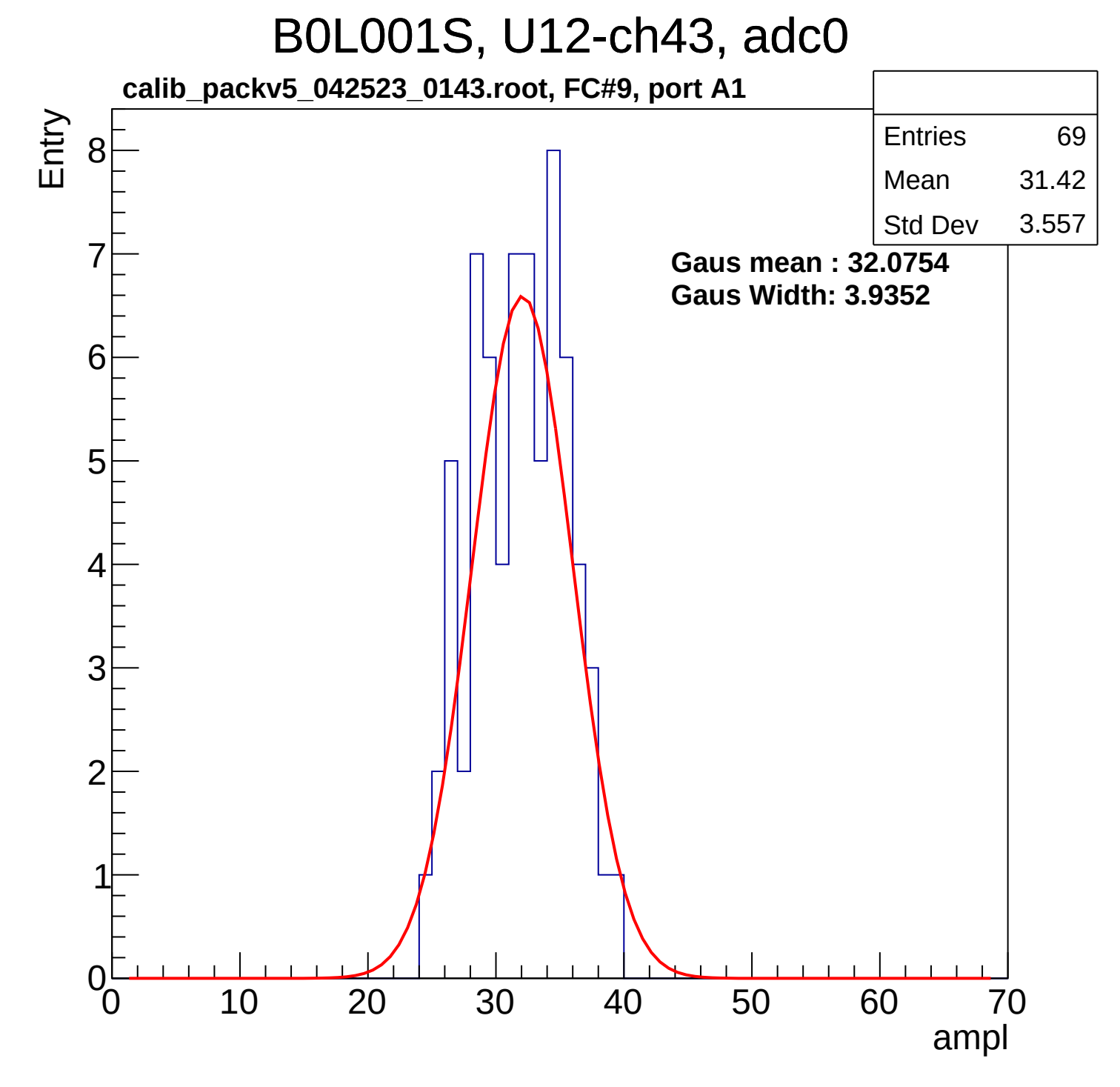
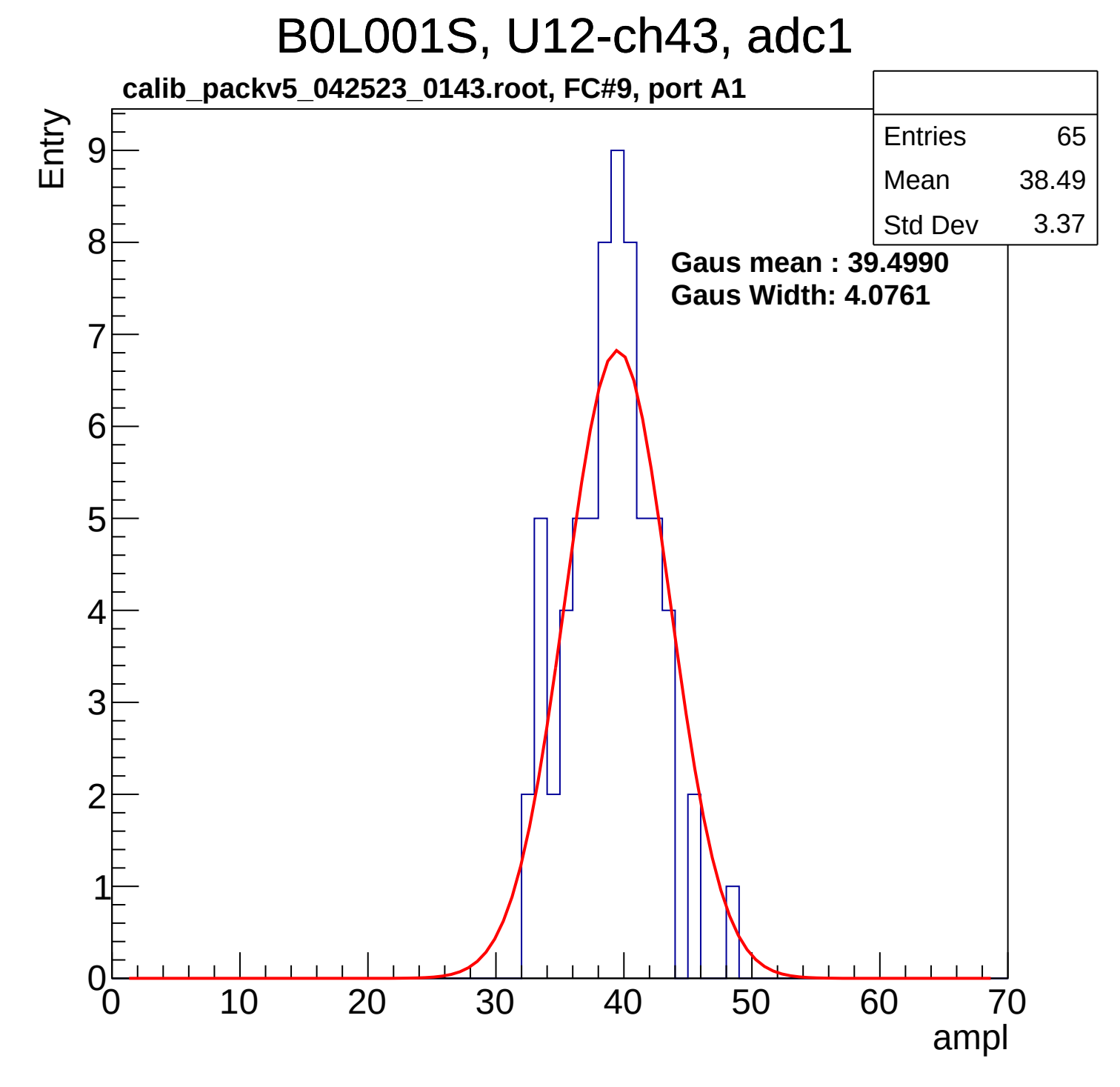
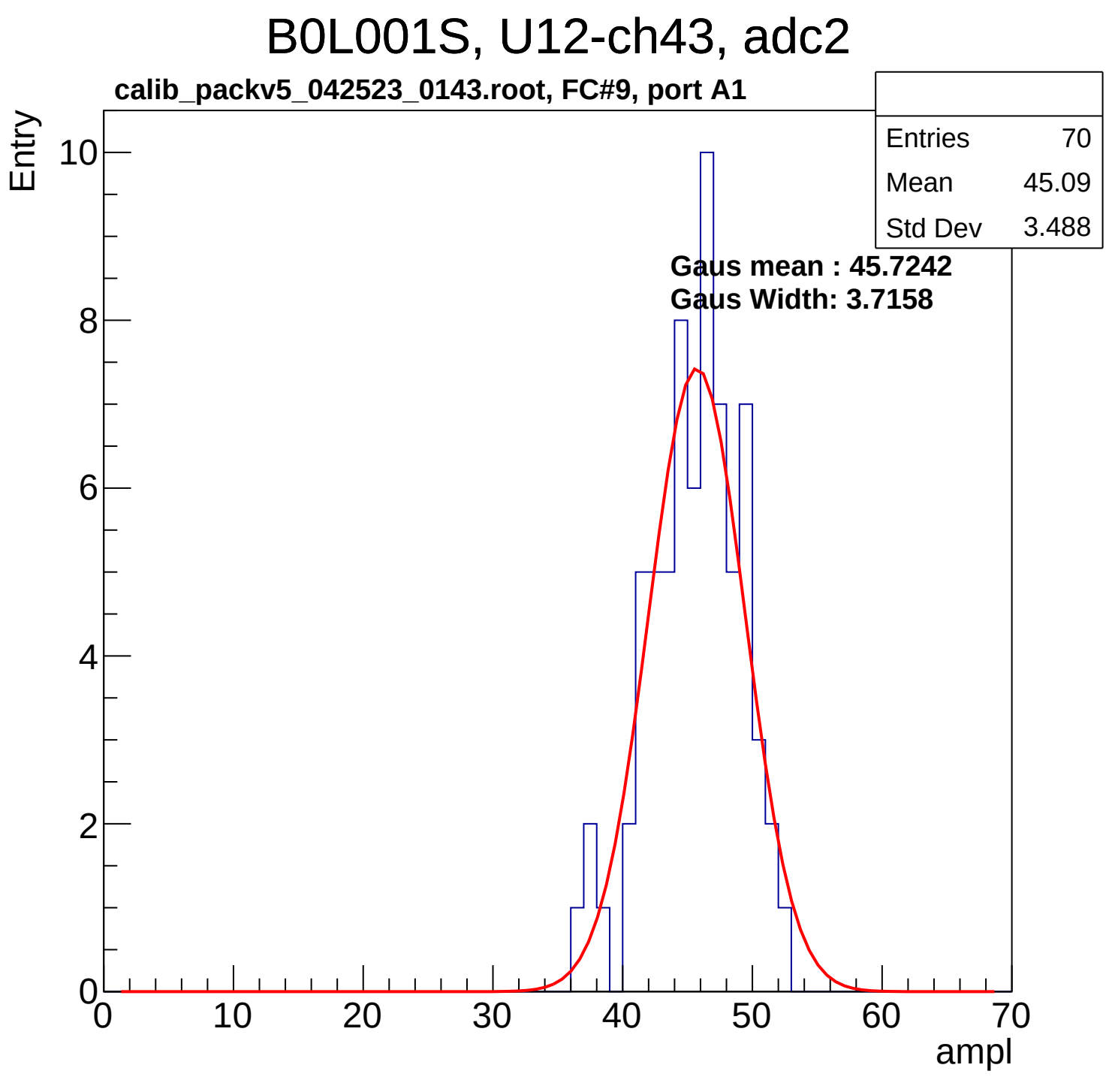
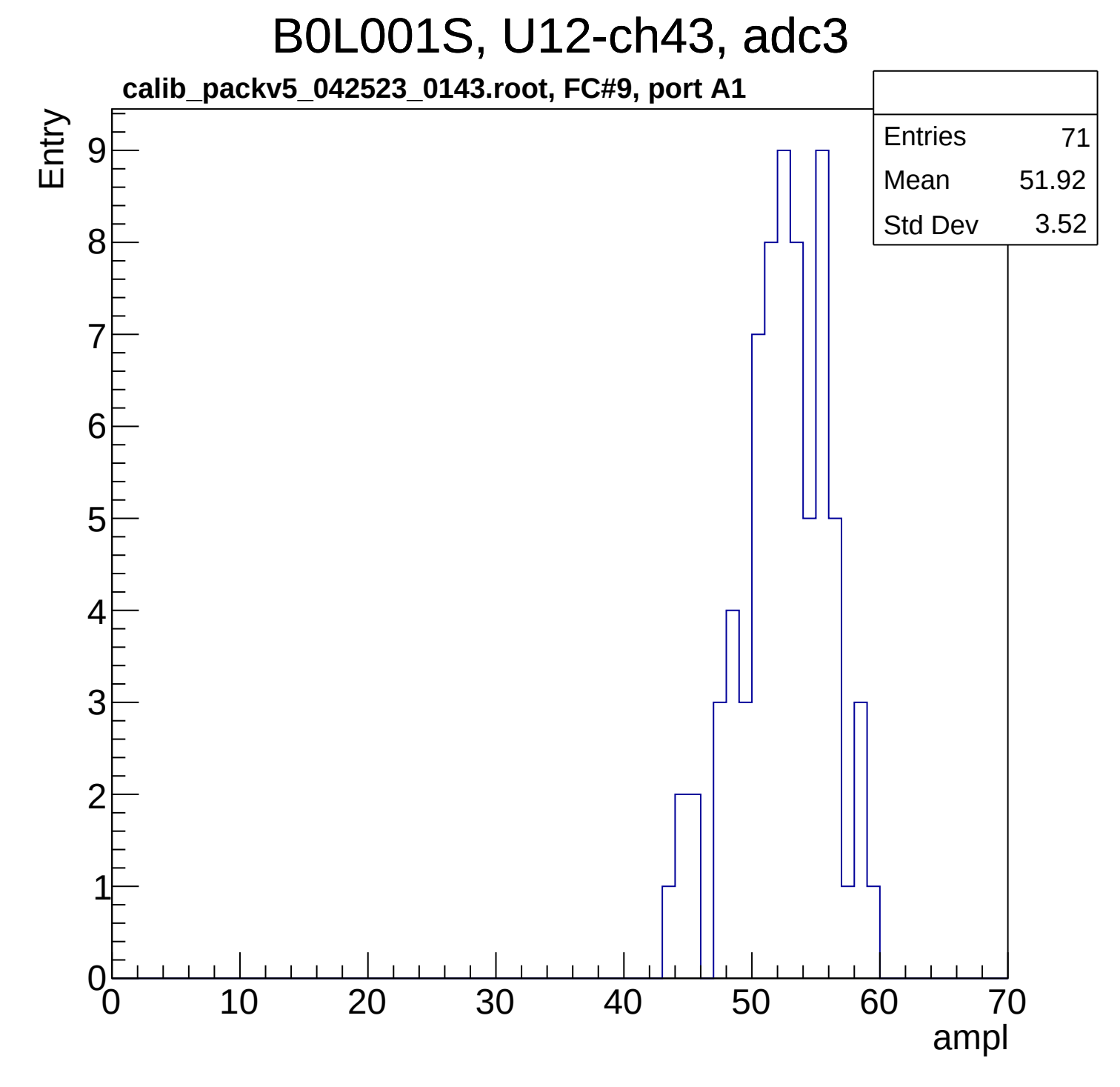
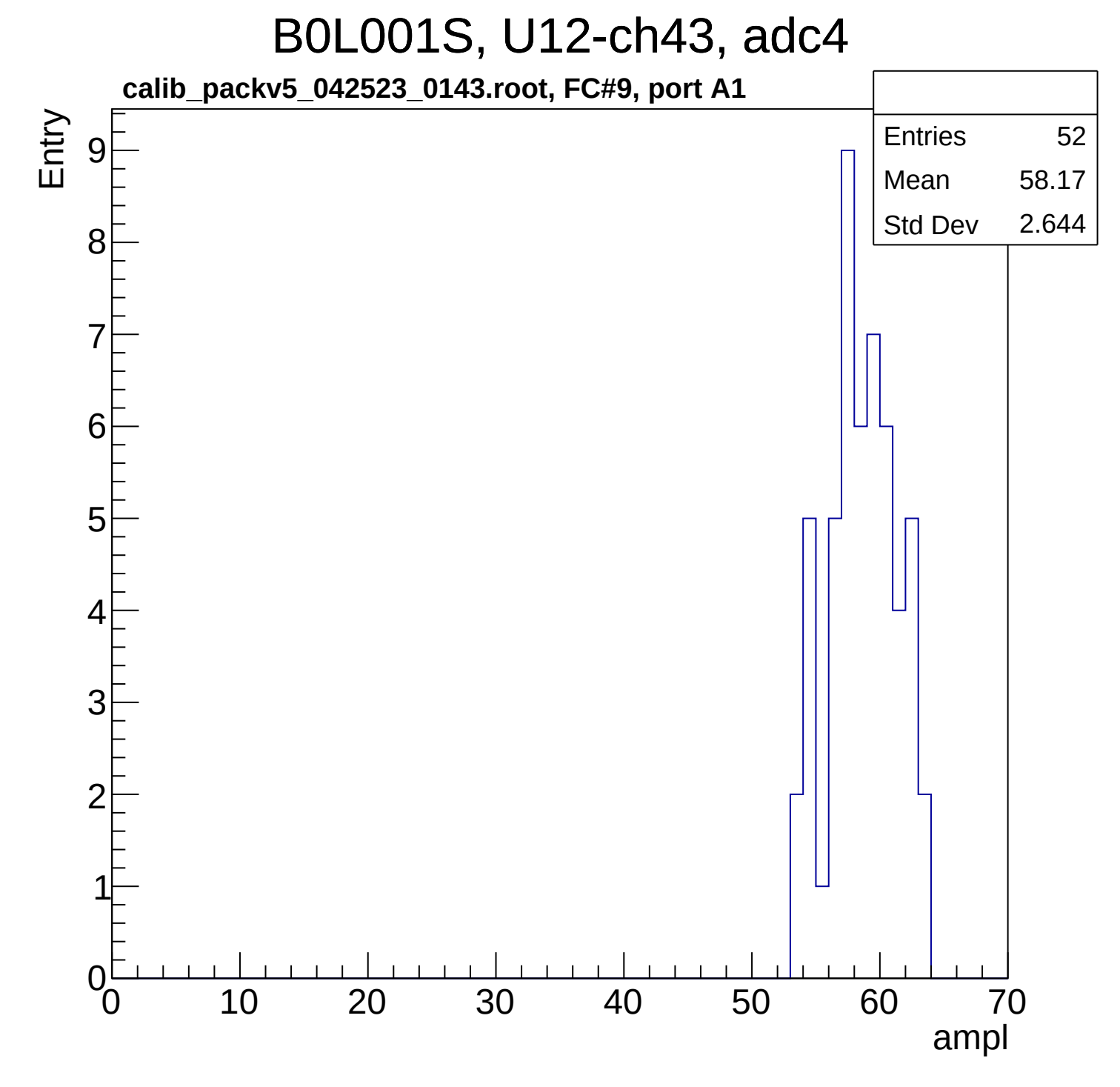

B0L001S, U12-ch42, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

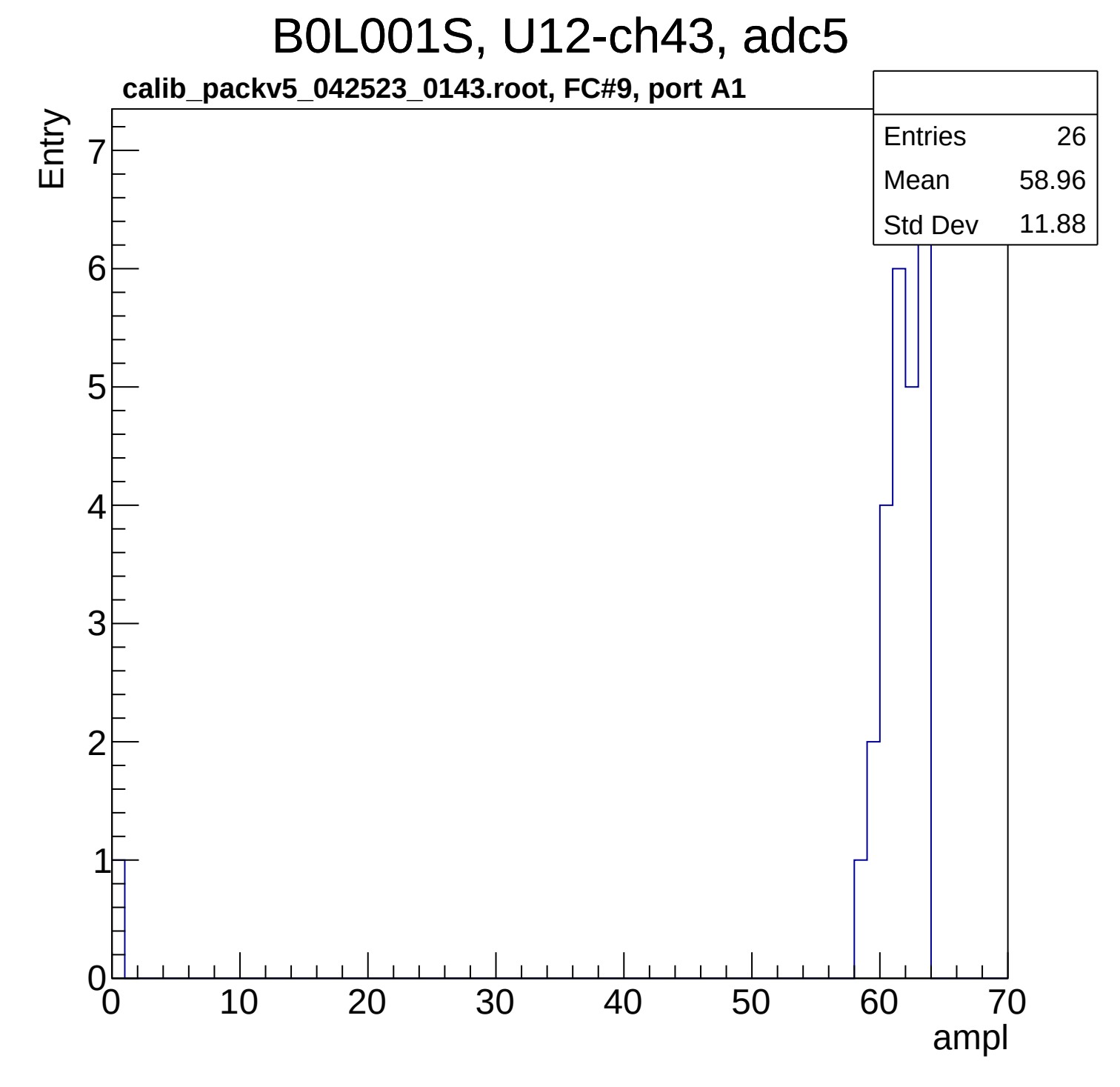

B0L001S, U12-ch43, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 69
Mean 31.42
Std Dev 3.557
Gaus mean : 32.0754
Gaus Width: 3.9352
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

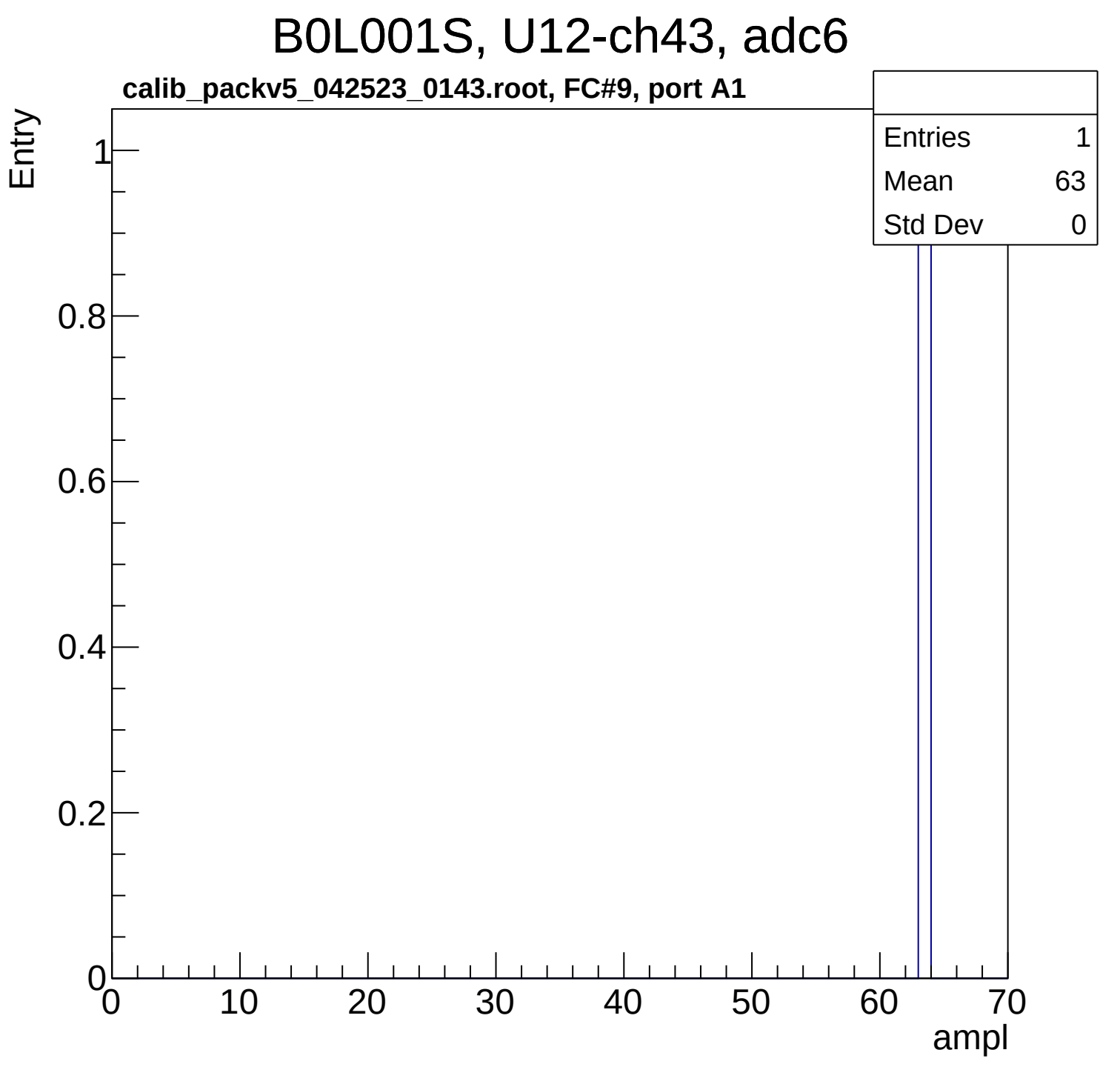

B0L001S, U12-ch43, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 65
Mean 38.49
Std Dev 3.37
Gaus mean : 39.4990
Gaus Width: 4.0761
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

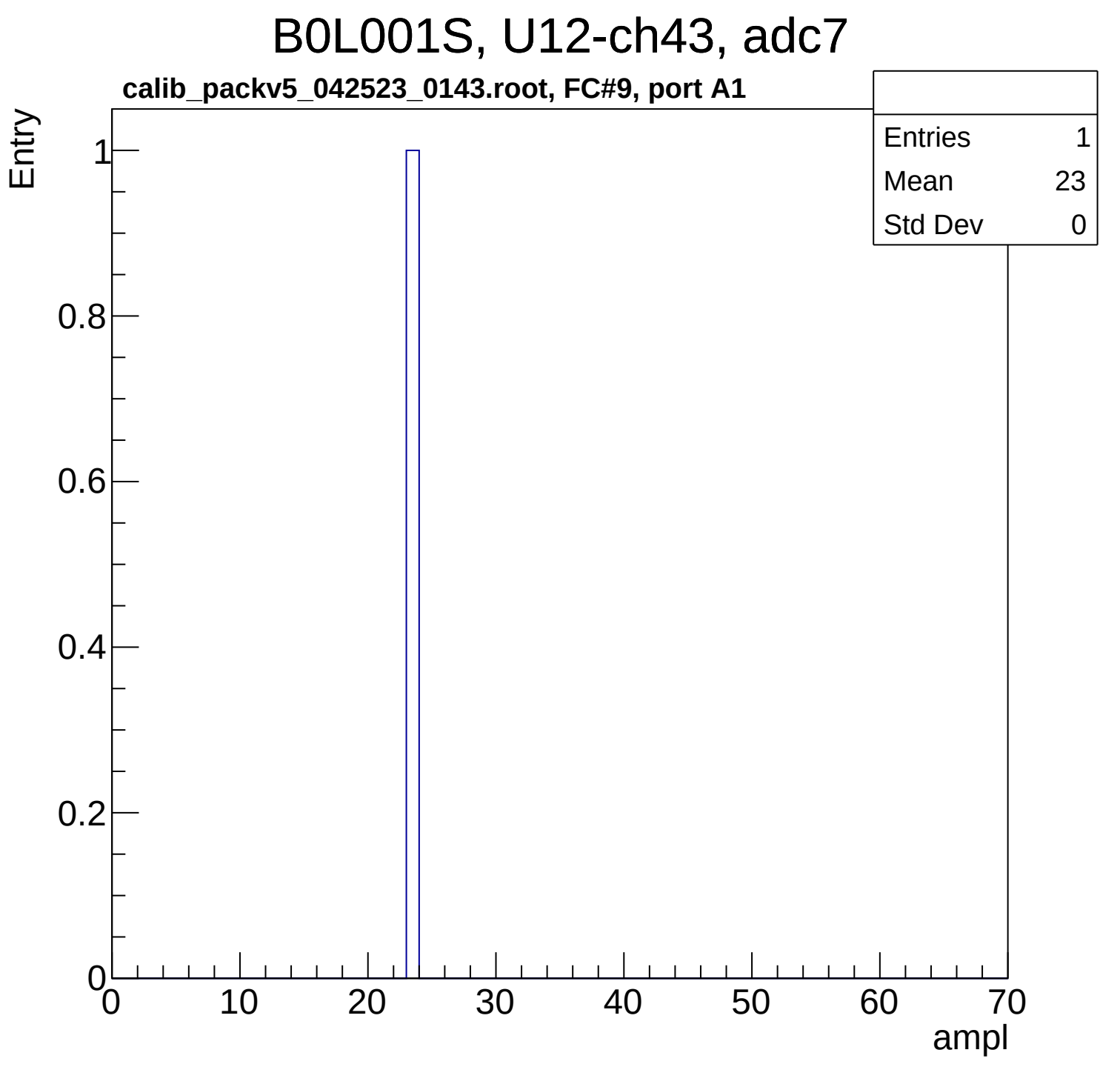

B0L001S, U12-ch43, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 70
Mean 45.09
Std Dev 3.488
Gaus mean : 45.7242
Gaus Width: 3.7158
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

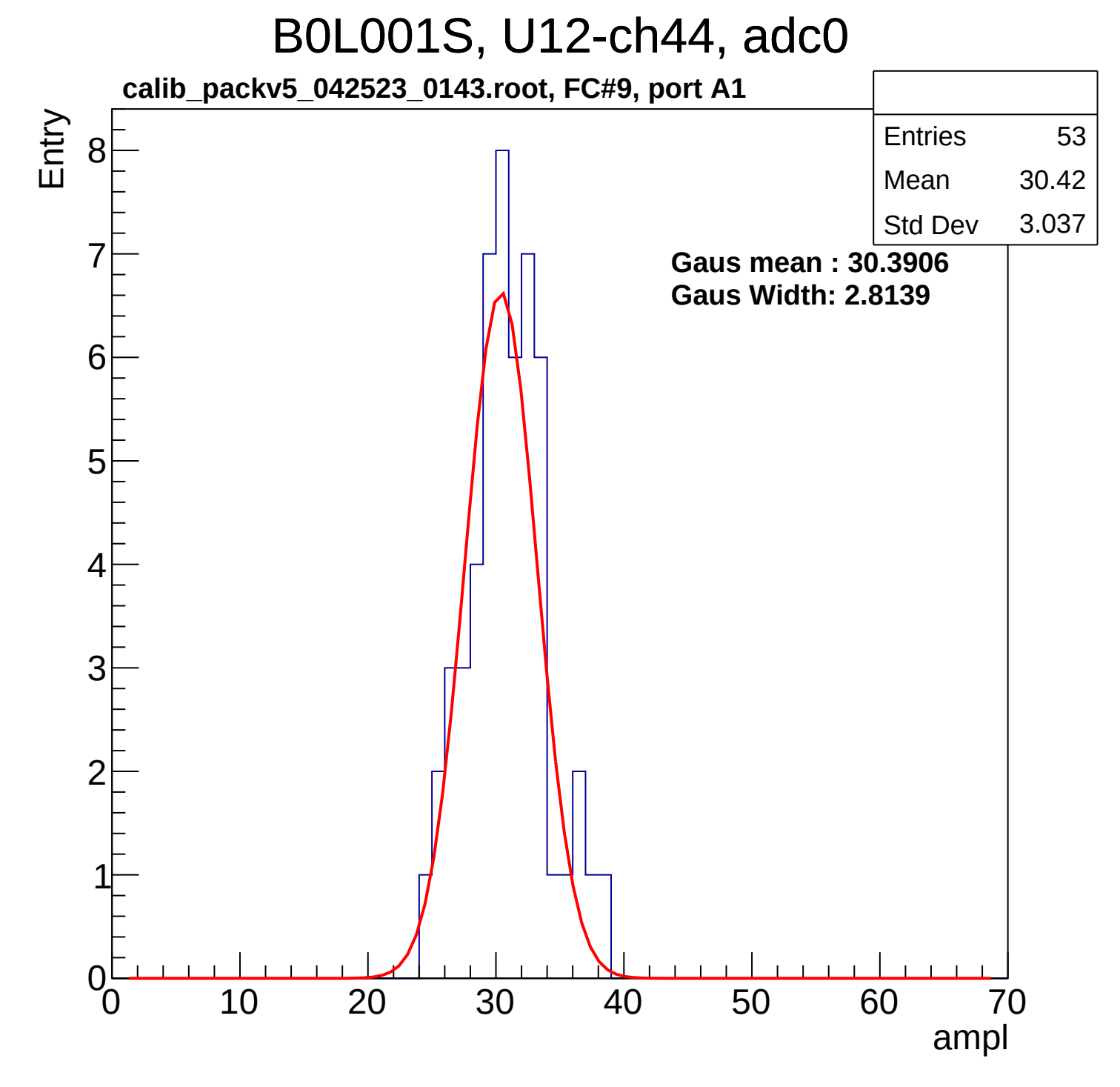

B0L001S, U12-ch43, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 71
Mean 51.92
Std Dev 3.52
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

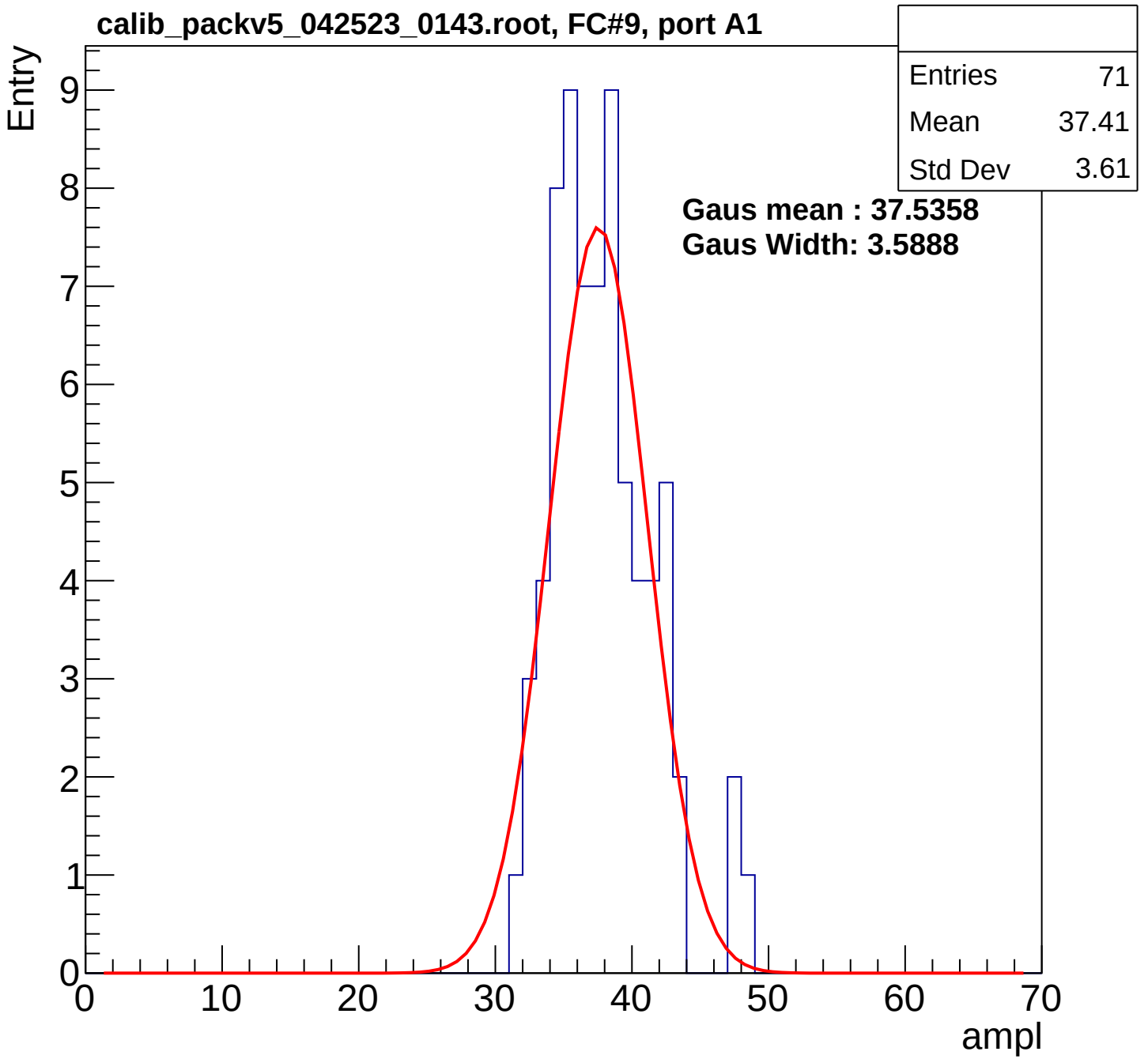

B0L001S, U12-ch43, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 52
Mean 58.17
Std Dev 2.644
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch43, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 26
Mean 58.96
Std Dev 11.88
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B0L001S, U12-ch43, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch43, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 23
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch44, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 53
Mean 30.42
Std Dev 3.037
Gaus mean : 30.3906
Gaus Width: 2.8139
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch44, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 71
Mean 37.41
Std Dev 3.61
Gaus mean : 37.5358
Gaus Width: 3.5888
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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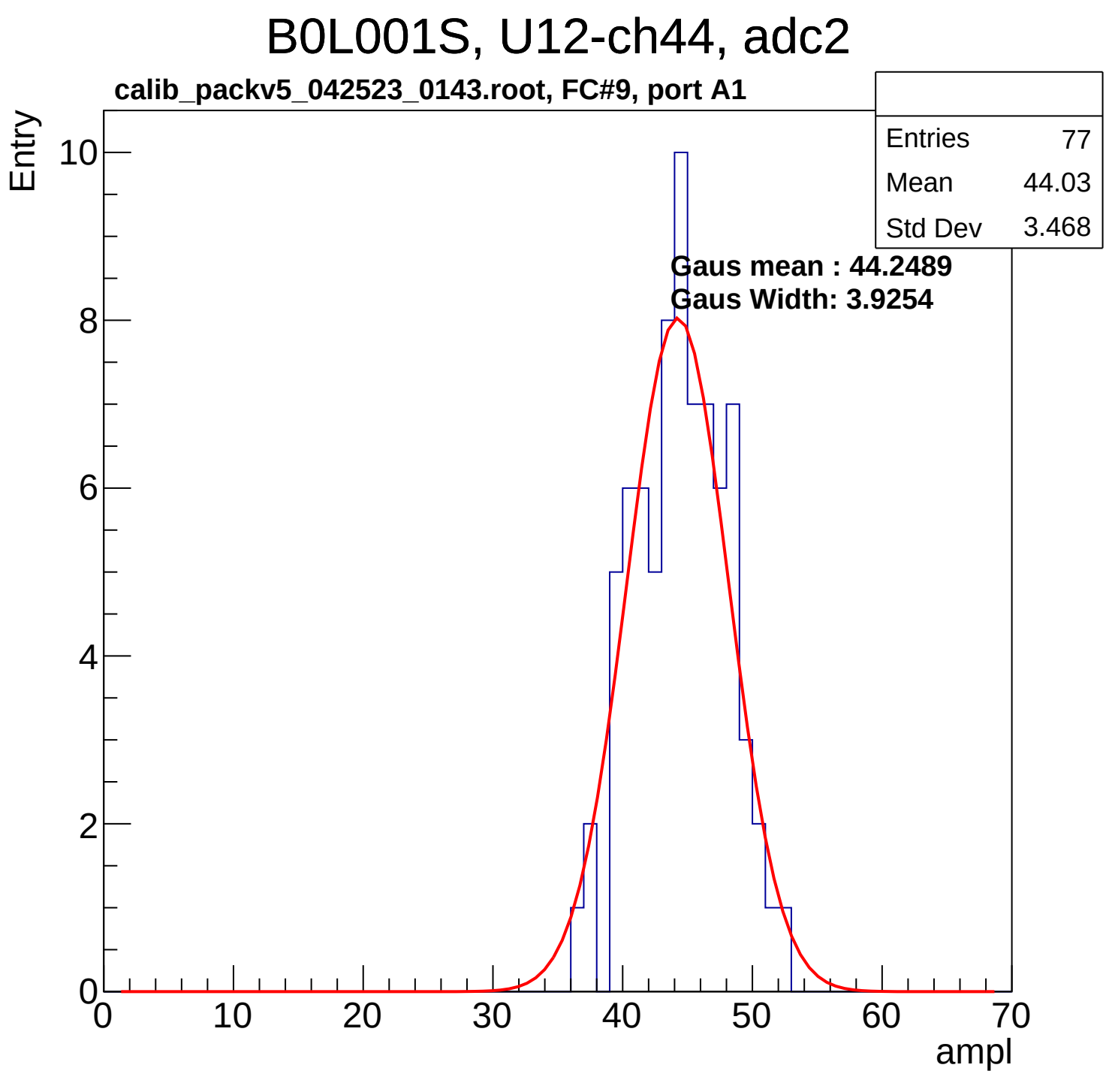
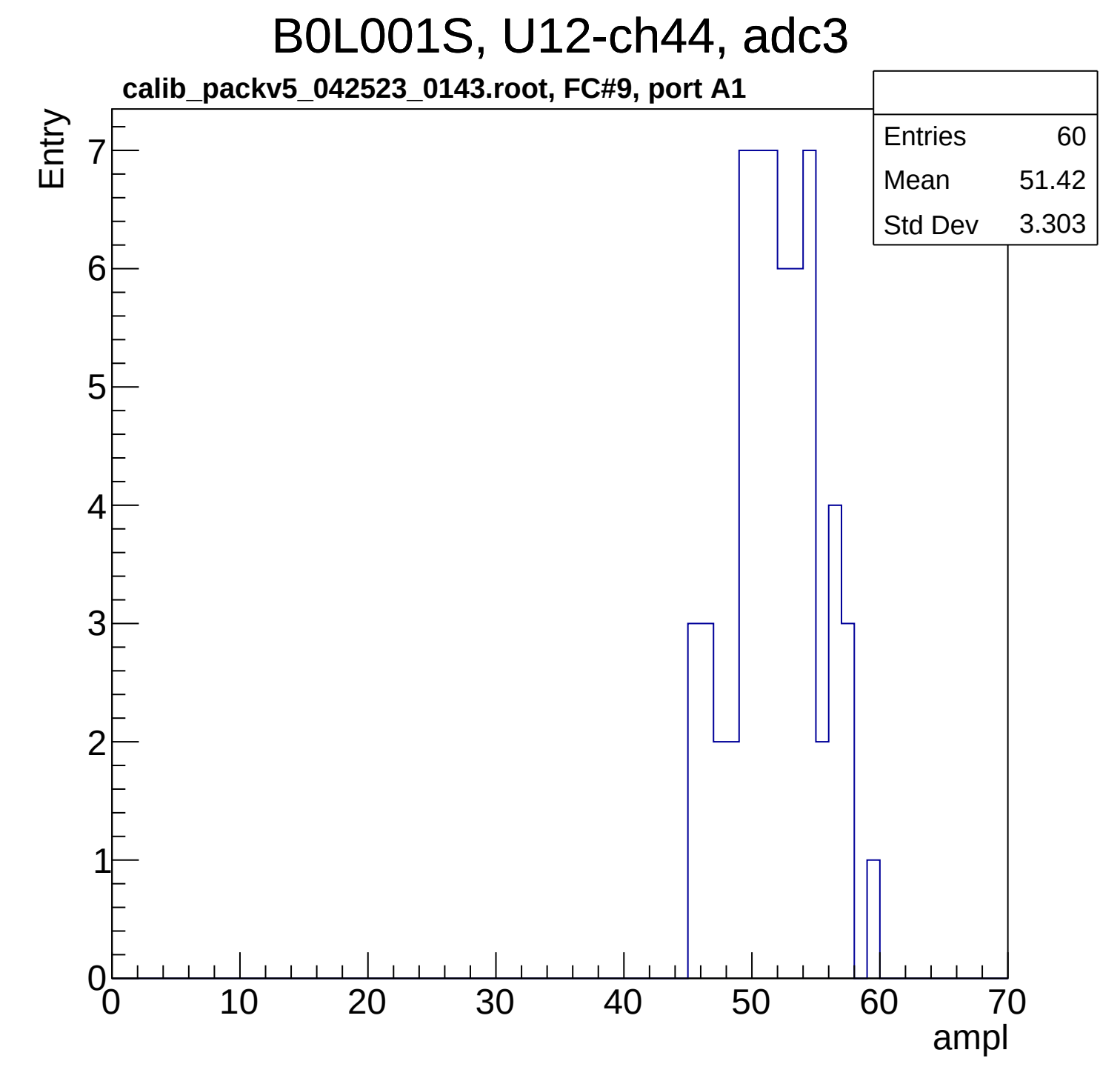
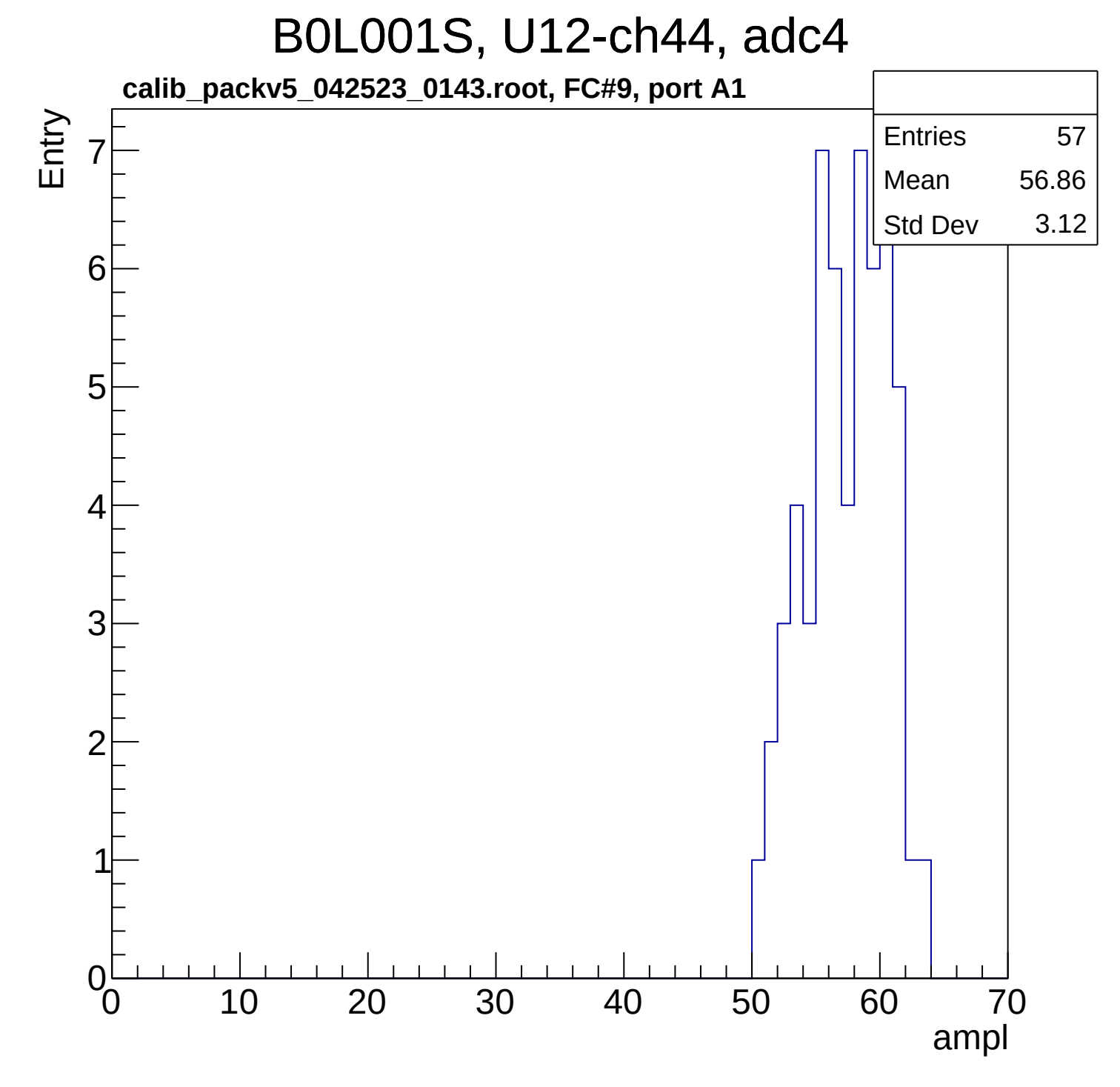

B0L001S, U12-ch44, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 77
Mean 44.03
Std Dev 3.468
Gaus mean : 44.2489
Gaus Width: 3.9254
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch44, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 60
Mean 51.42
Std Dev 3.303
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B0L001S, U12-ch44, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 57
Mean 56.86
Std Dev 3.12
Entry
ampl
0
1
2
3
4
5
6
7
0
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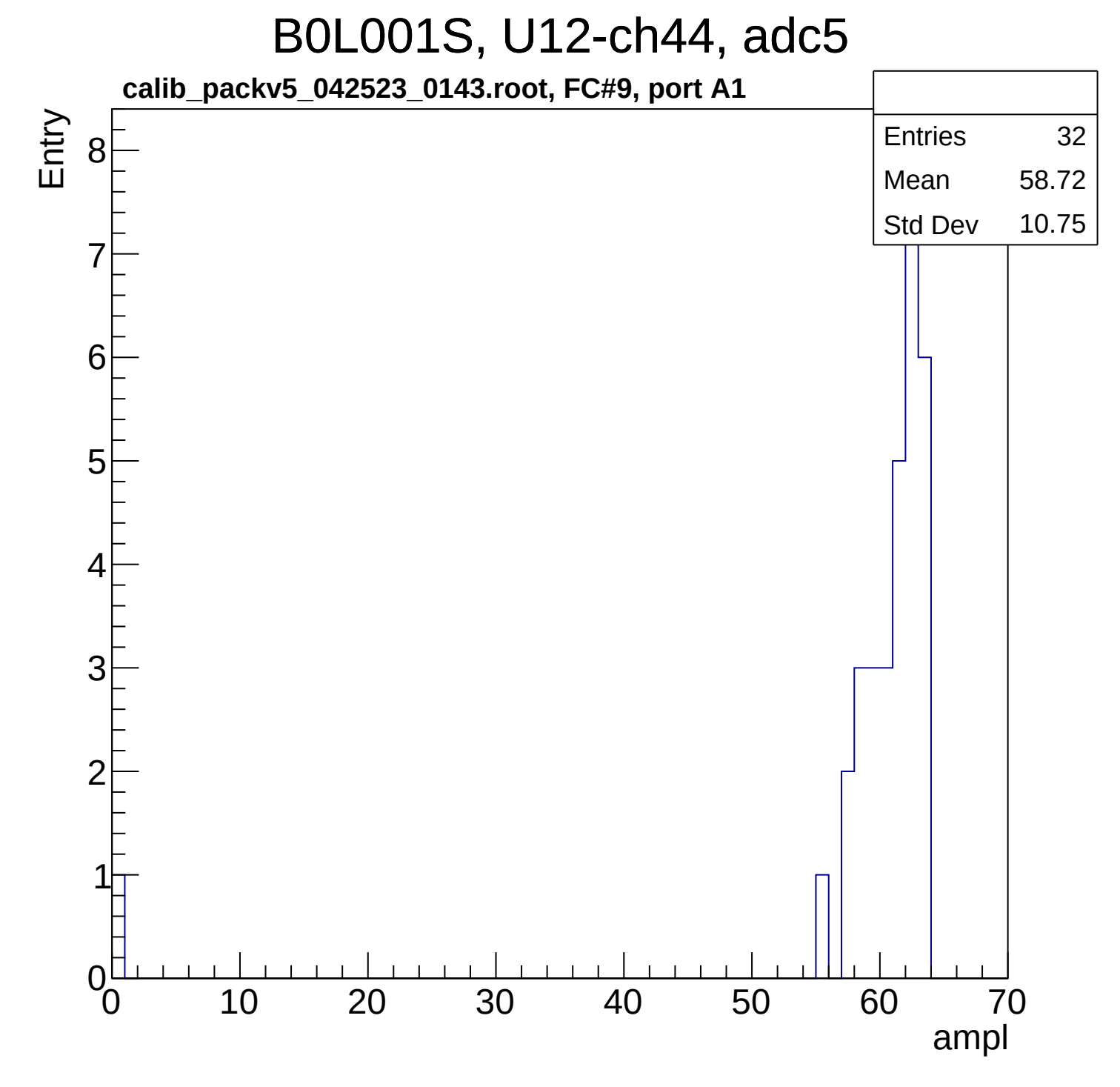
20
30
40
50
60
70


B0L001S, U12-ch44, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 32
Mean 58.72
Std Dev 10.75
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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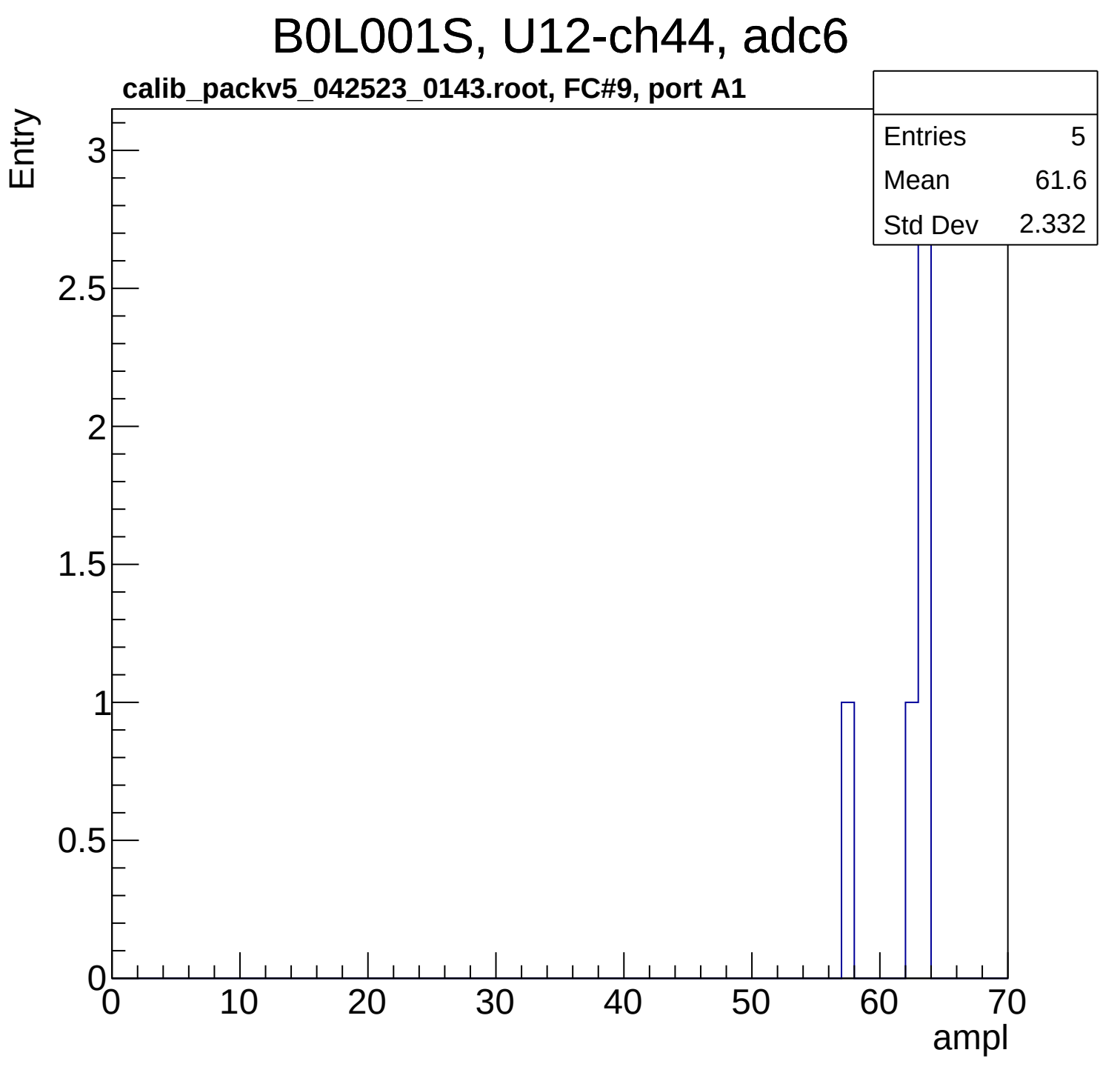
B0L001S, U12-ch44, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 5
Mean 61.6
Std Dev 2.332
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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40
50
60
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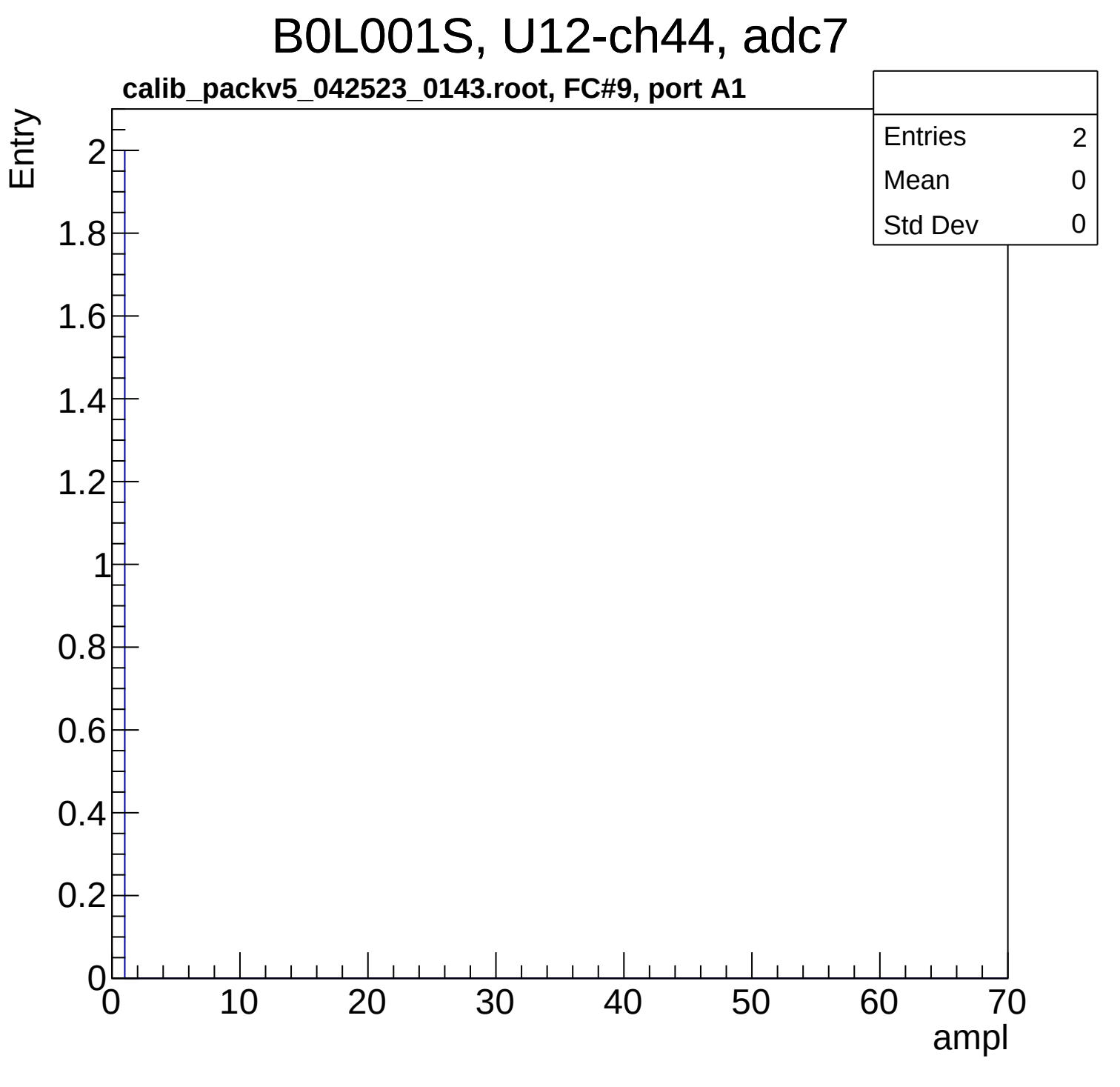
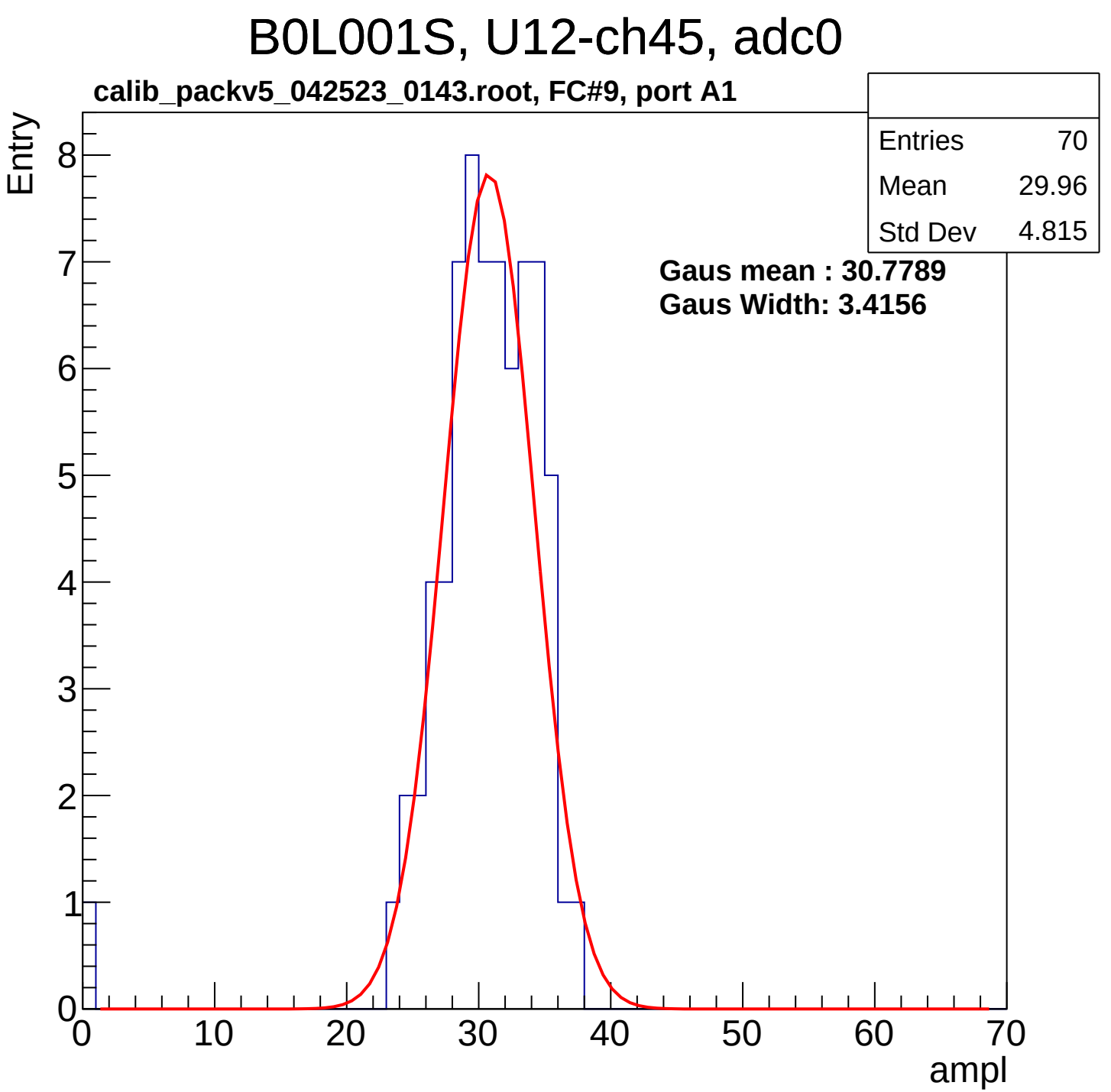
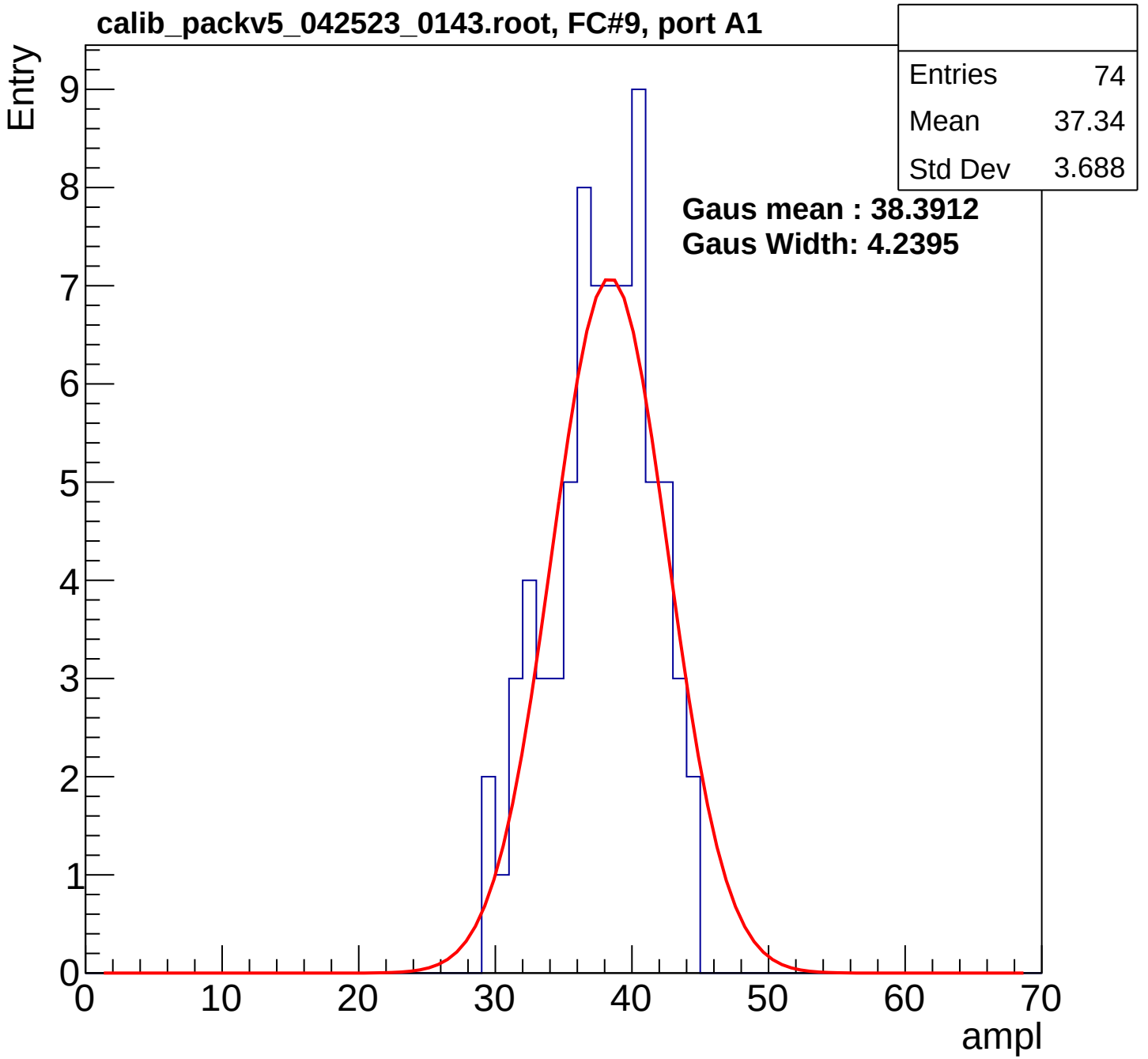
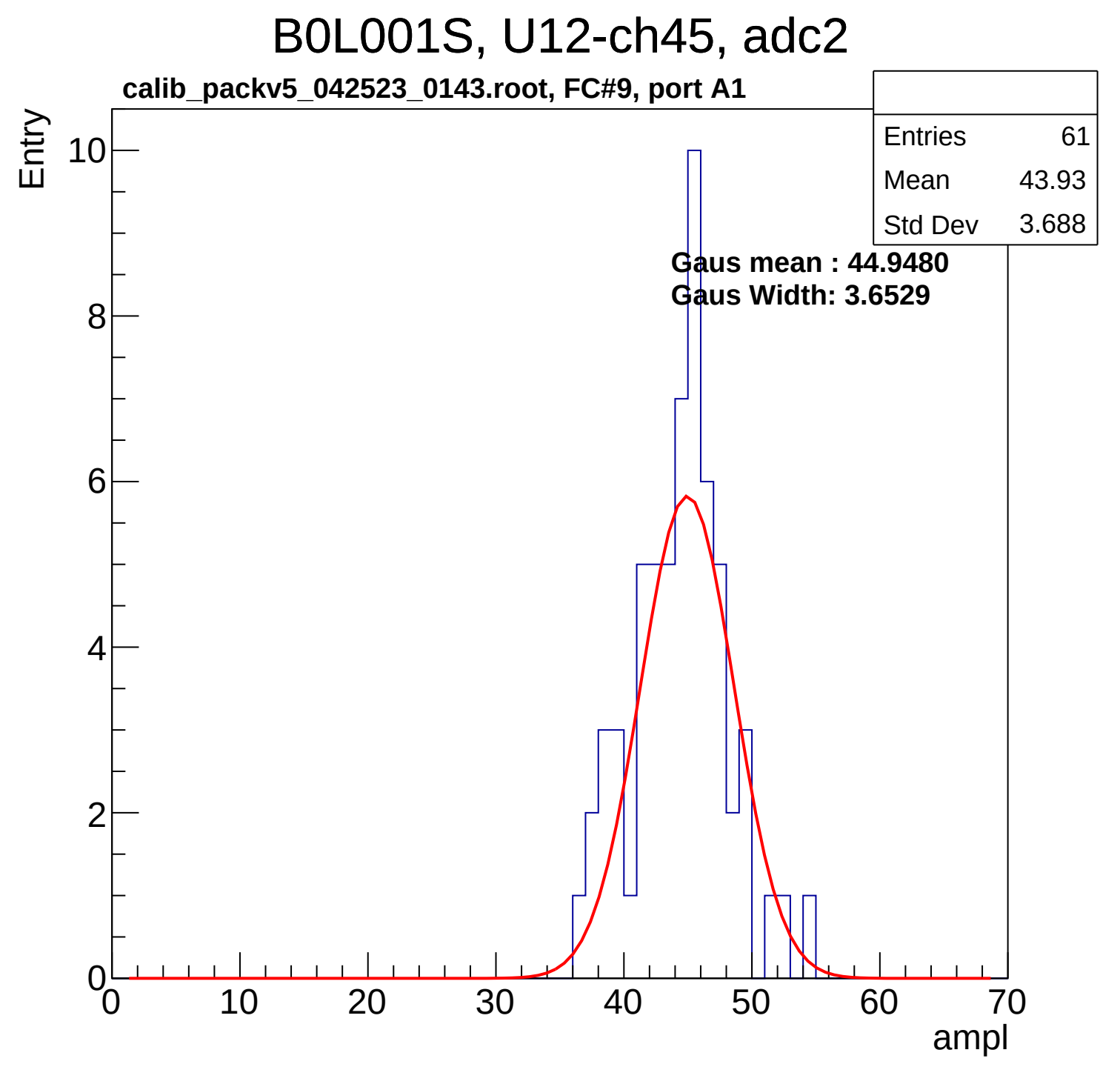
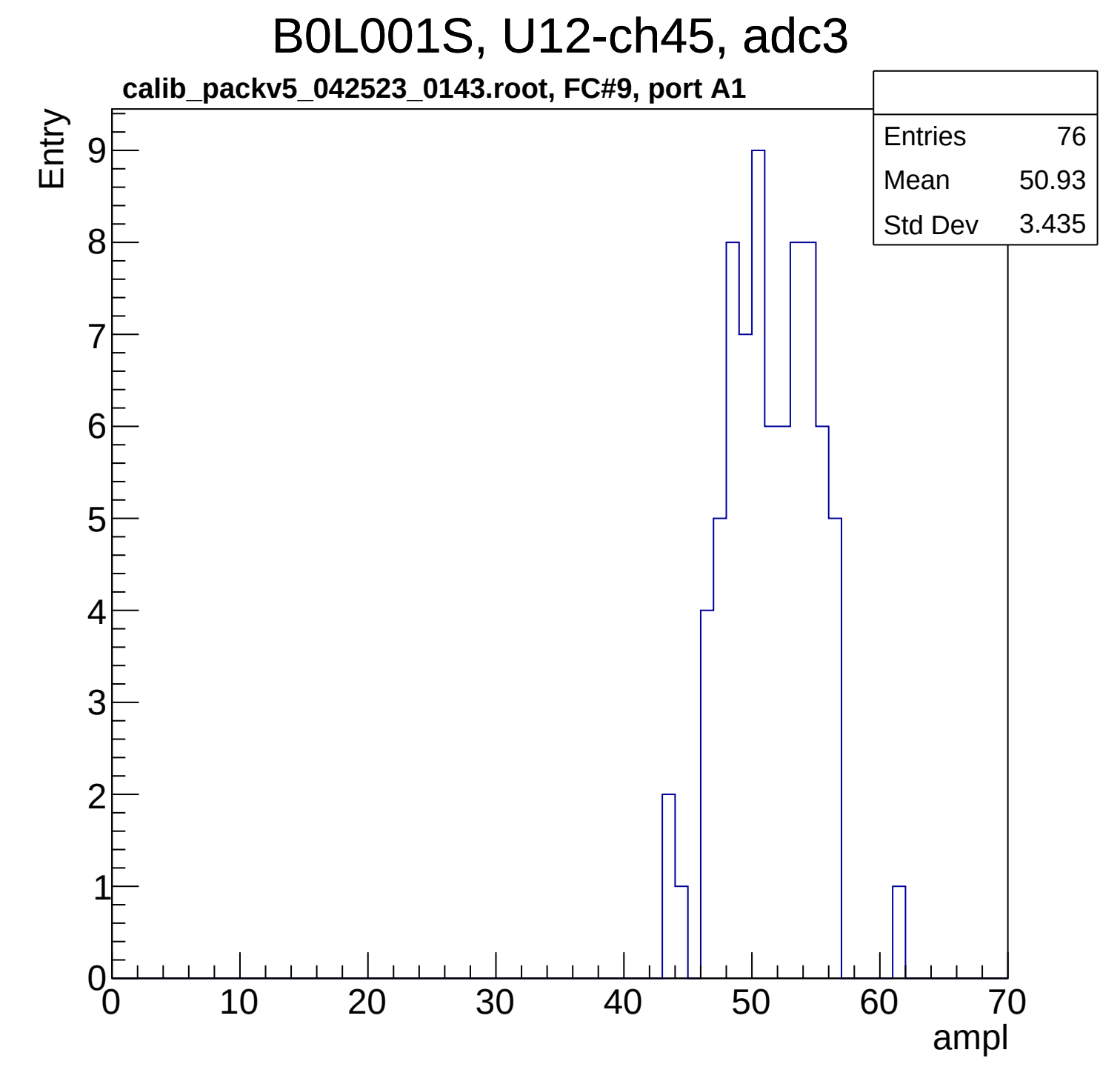

B0L001S, U12-ch44, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch45, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 70
Mean 29.96
Std Dev 4.815
Gaus mean : 30.7789
Gaus Width: 3.4156
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch45, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 74
Mean 37.34
Std Dev 3.688
Gaus mean : 38.3912
Gaus Width: 4.2395
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch45, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 61
Mean 43.93
Std Dev 3.688
Gaus mean : 44.9480
Gaus Width: 3.6529
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch45, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 76
Mean 50.93
Std Dev 3.435
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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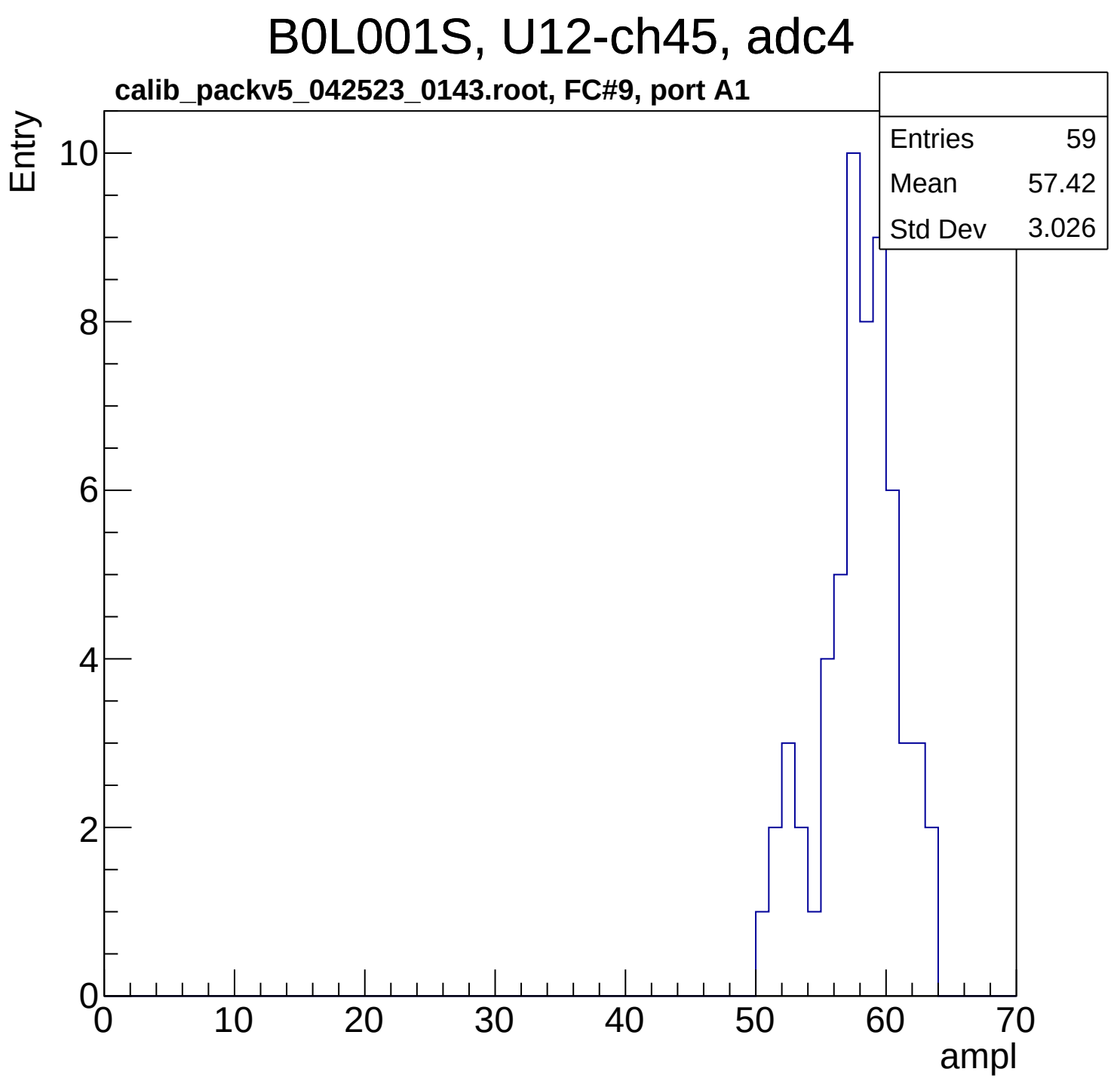
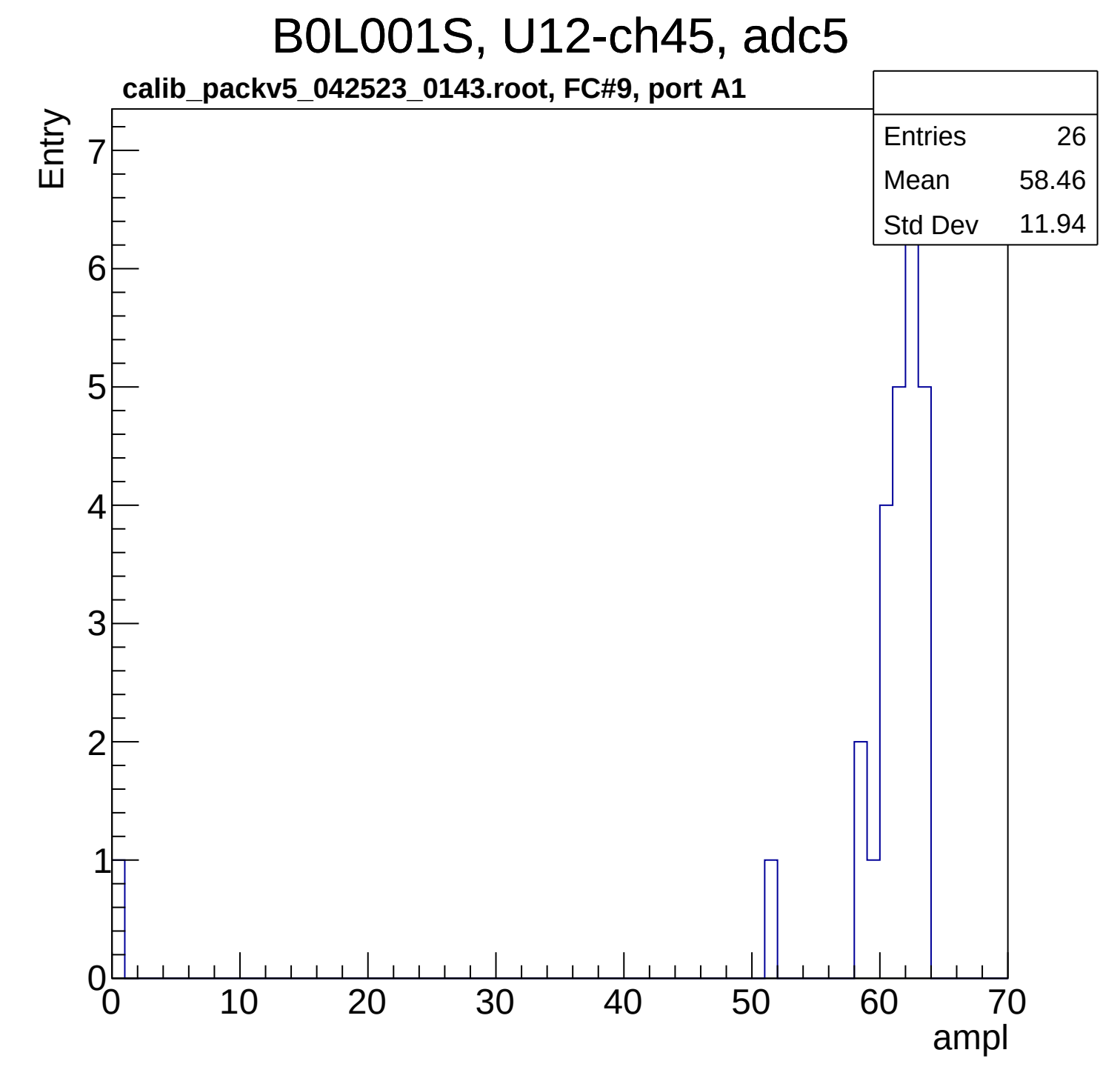
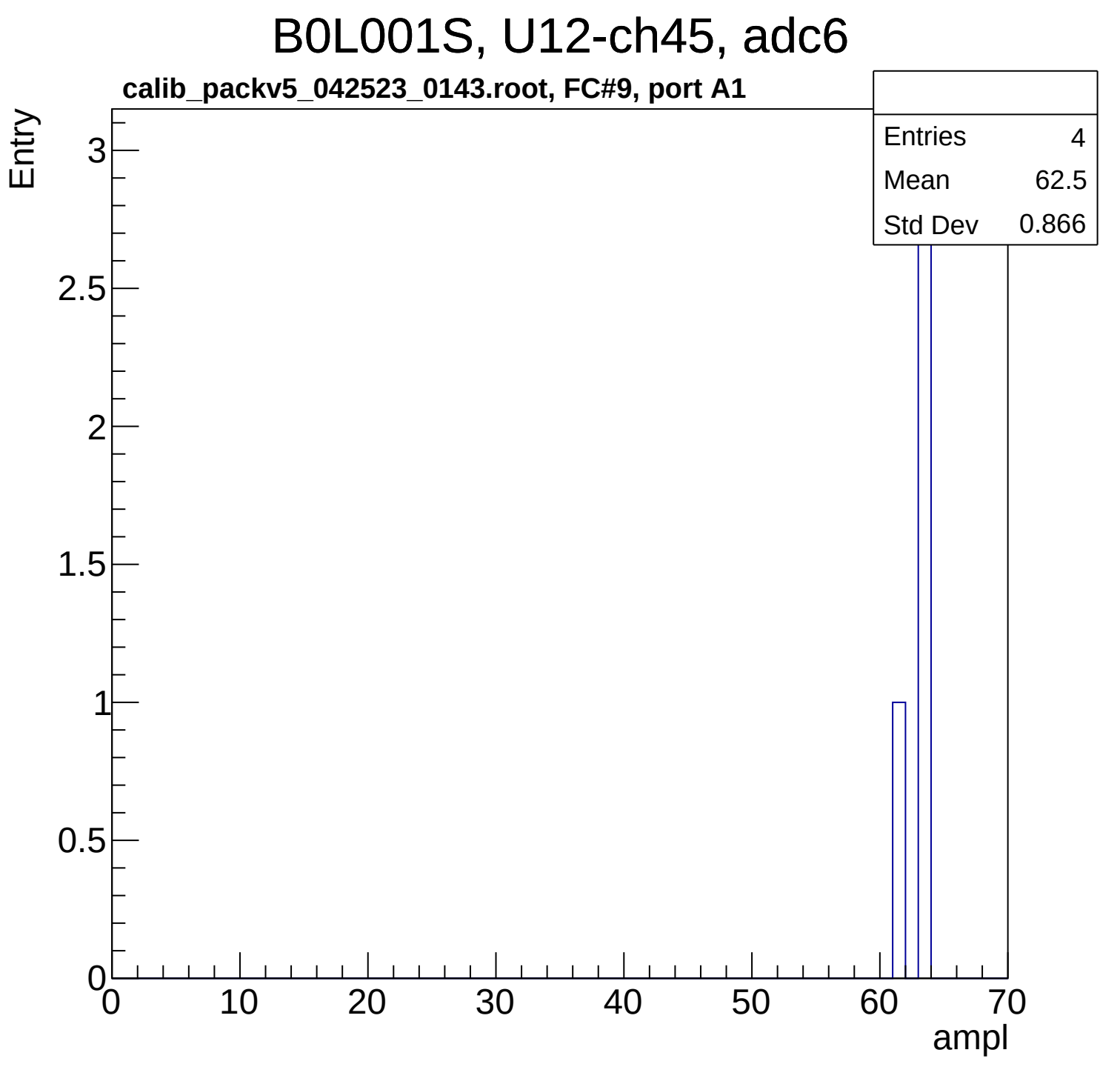
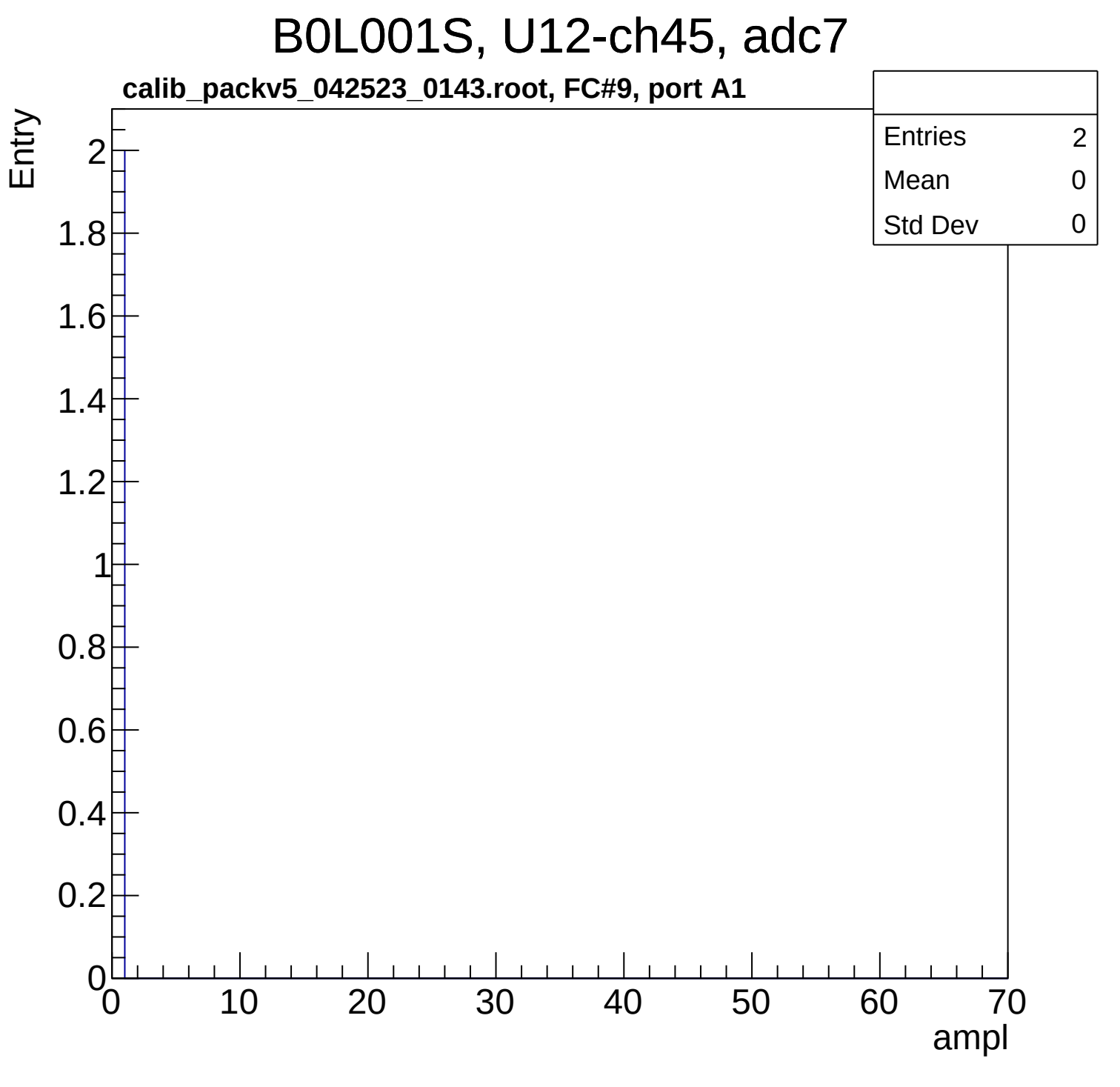
40
50
60
70


B0L001S, U12-ch45, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 59
Mean 57.42
Std Dev 3.026
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch45, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 26
Mean 58.46
Std Dev 11.94
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B0L001S, U12-ch45, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 4
Mean 62.5
Std Dev 0.866
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B0L001S, U12-ch45, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
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0.8
0.6
0.4
0.2
0
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10
20
30
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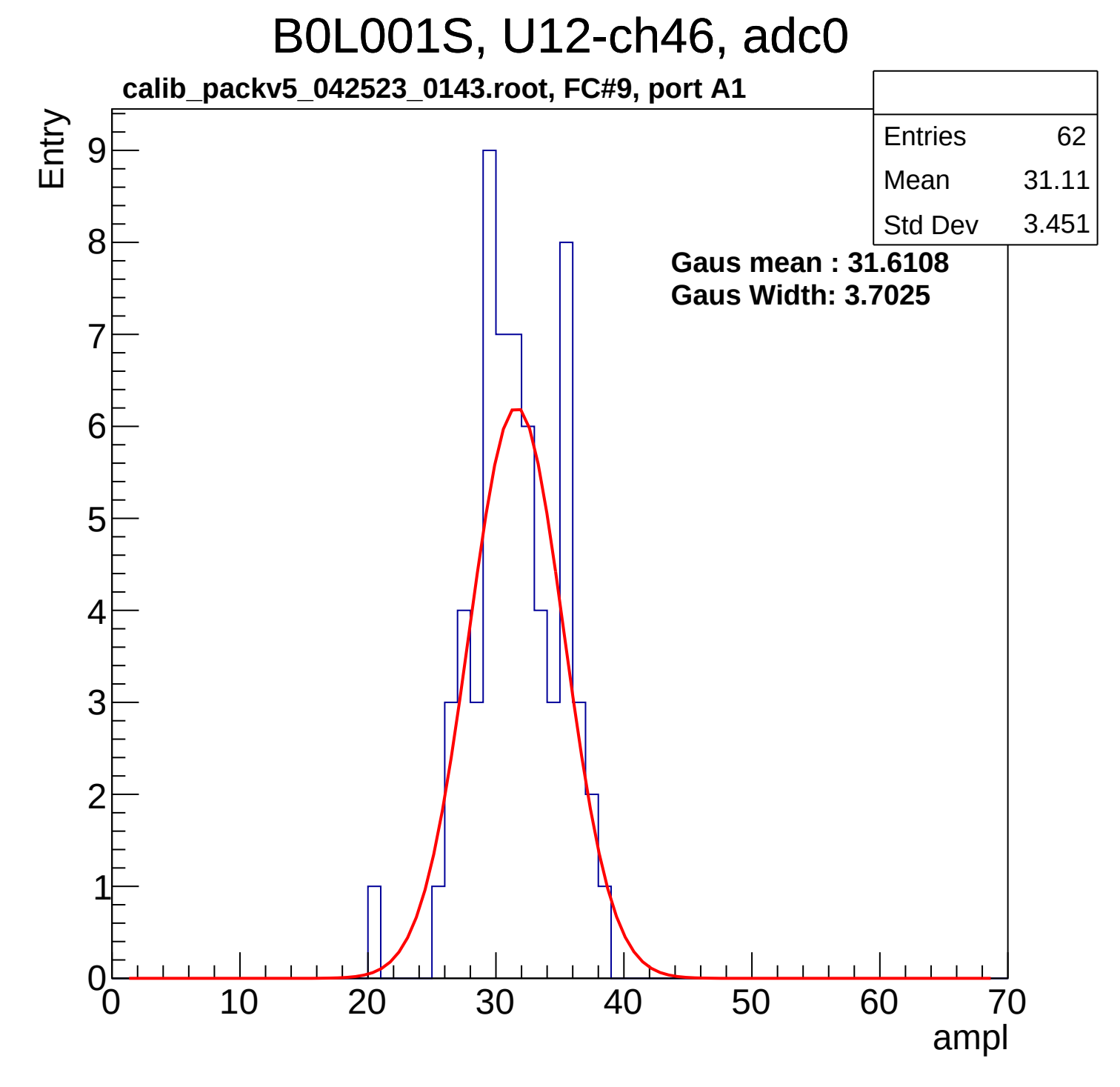
50
60
70
ampl


B0L001S, U12-ch46, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 62
Mean 31.11
Std Dev 3.451
Gaus mean : 31.6108
Gaus Width: 3.7025
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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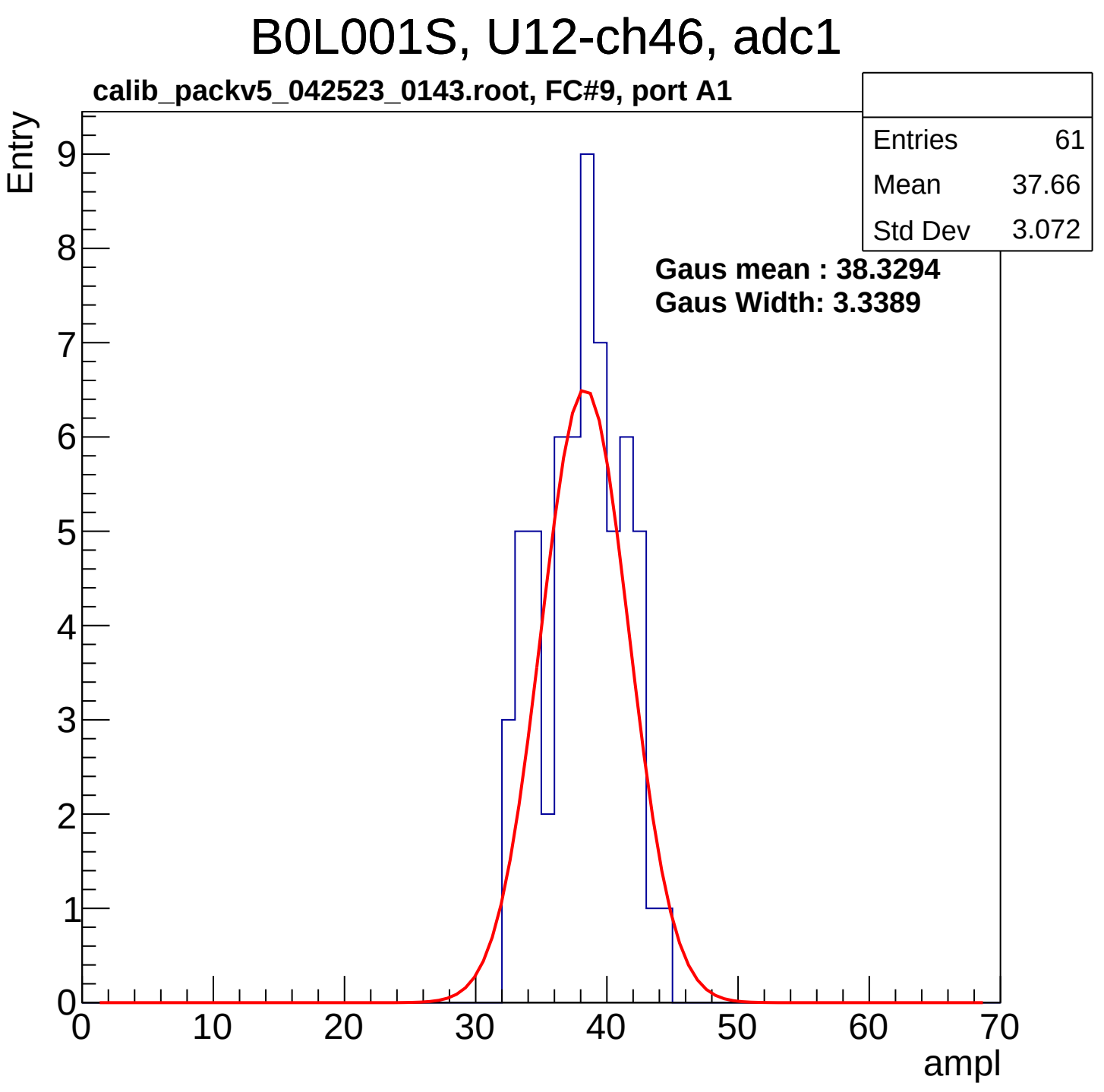
60
70


B0L001S, U12-ch46, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 61
Mean 37.66
Std Dev 3.072
Gaus mean : 38.3294
Gaus Width: 3.3389
Entry
ampl
0
1
2
3
4
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6
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8
9
0
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20
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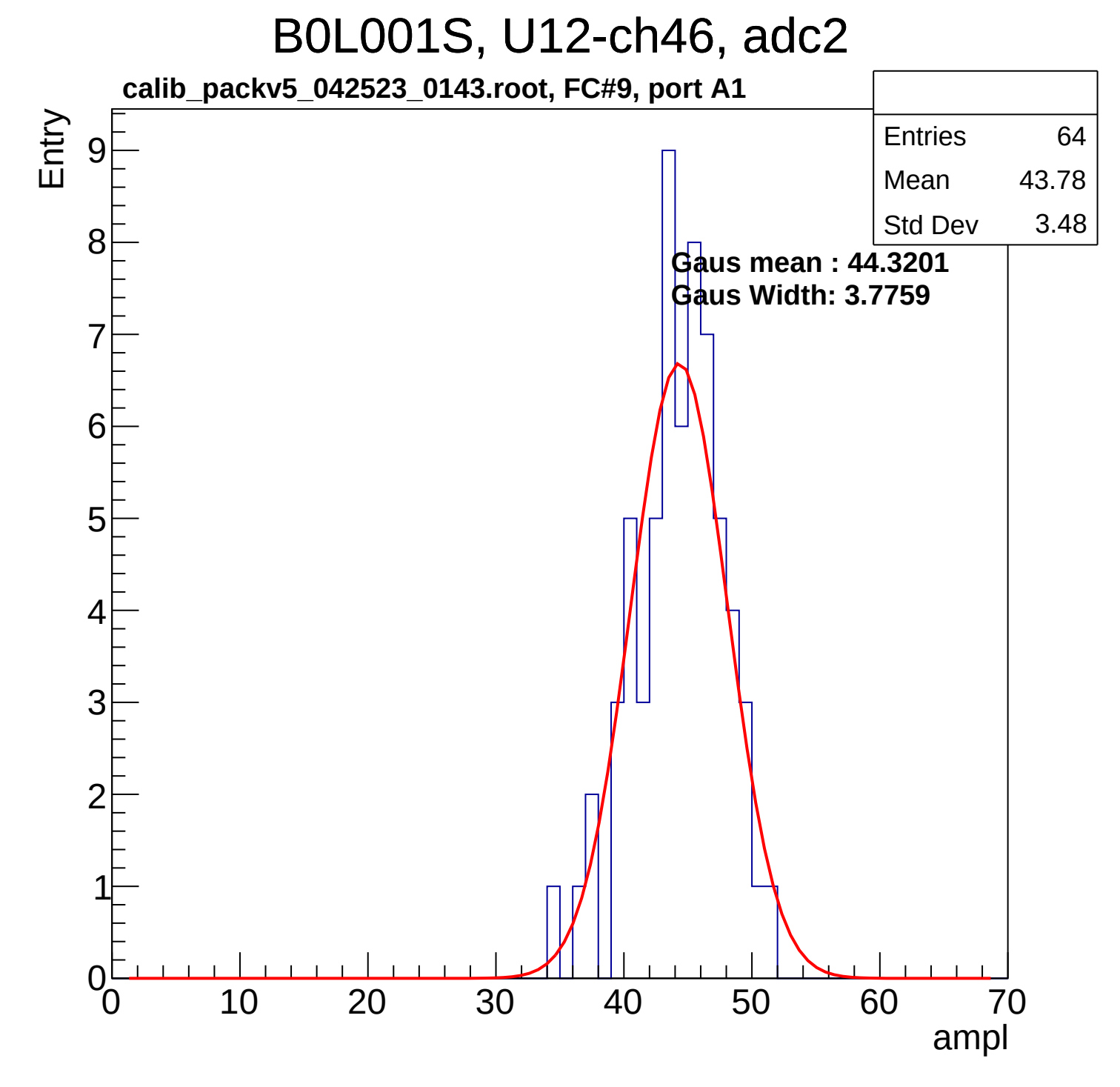
40
50
60
70


B0L001S, U12-ch46, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 64
Mean 43.78
Std Dev 3.48
Gaus mean : 44.3201
Gaus Width: 3.7759
Entry
ampl
0
1
2
3
4
5
6
7
8
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0
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60
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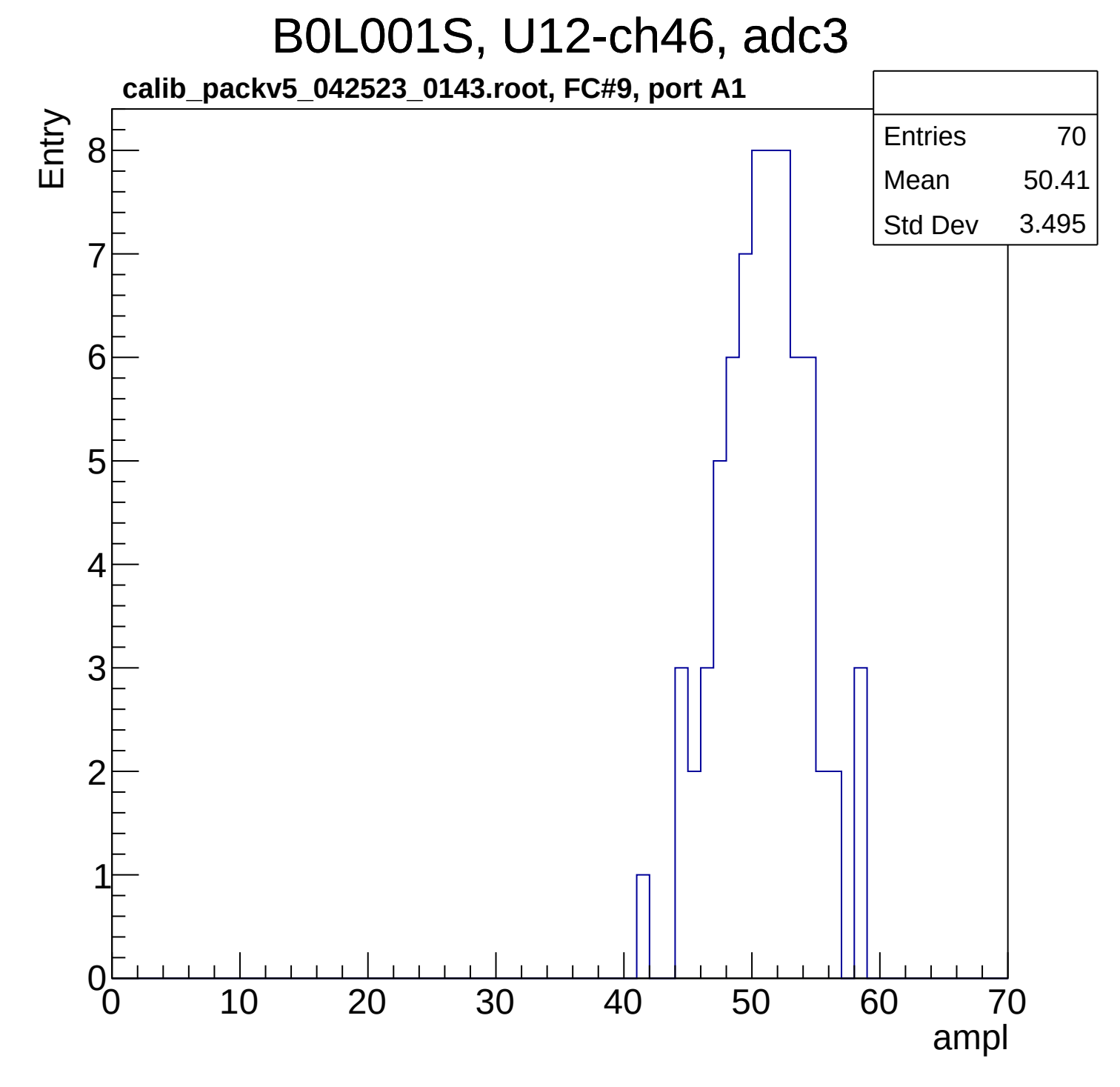
B0L001S, U12-ch46, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 70
Mean 50.41
Std Dev 3.495
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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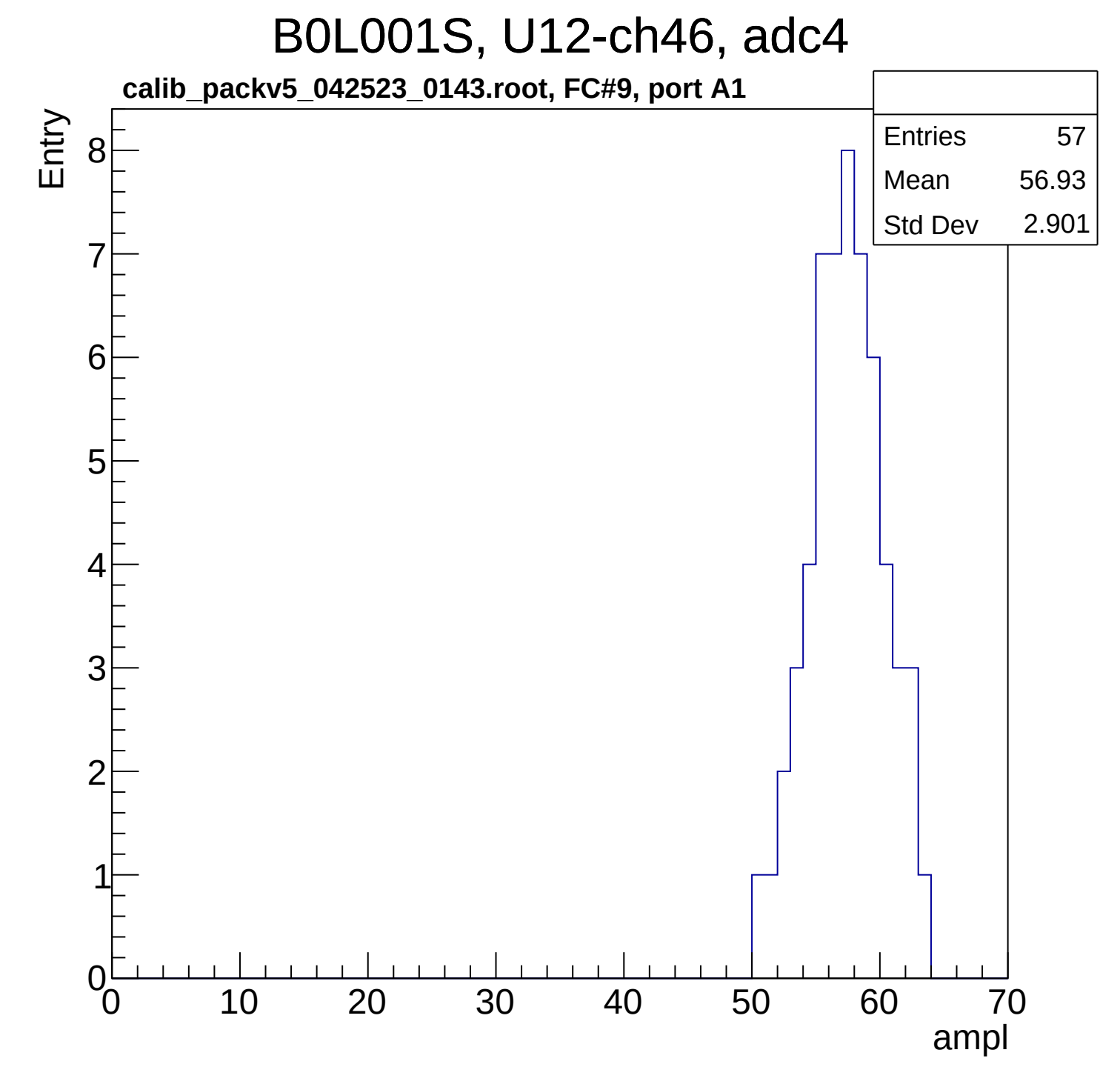
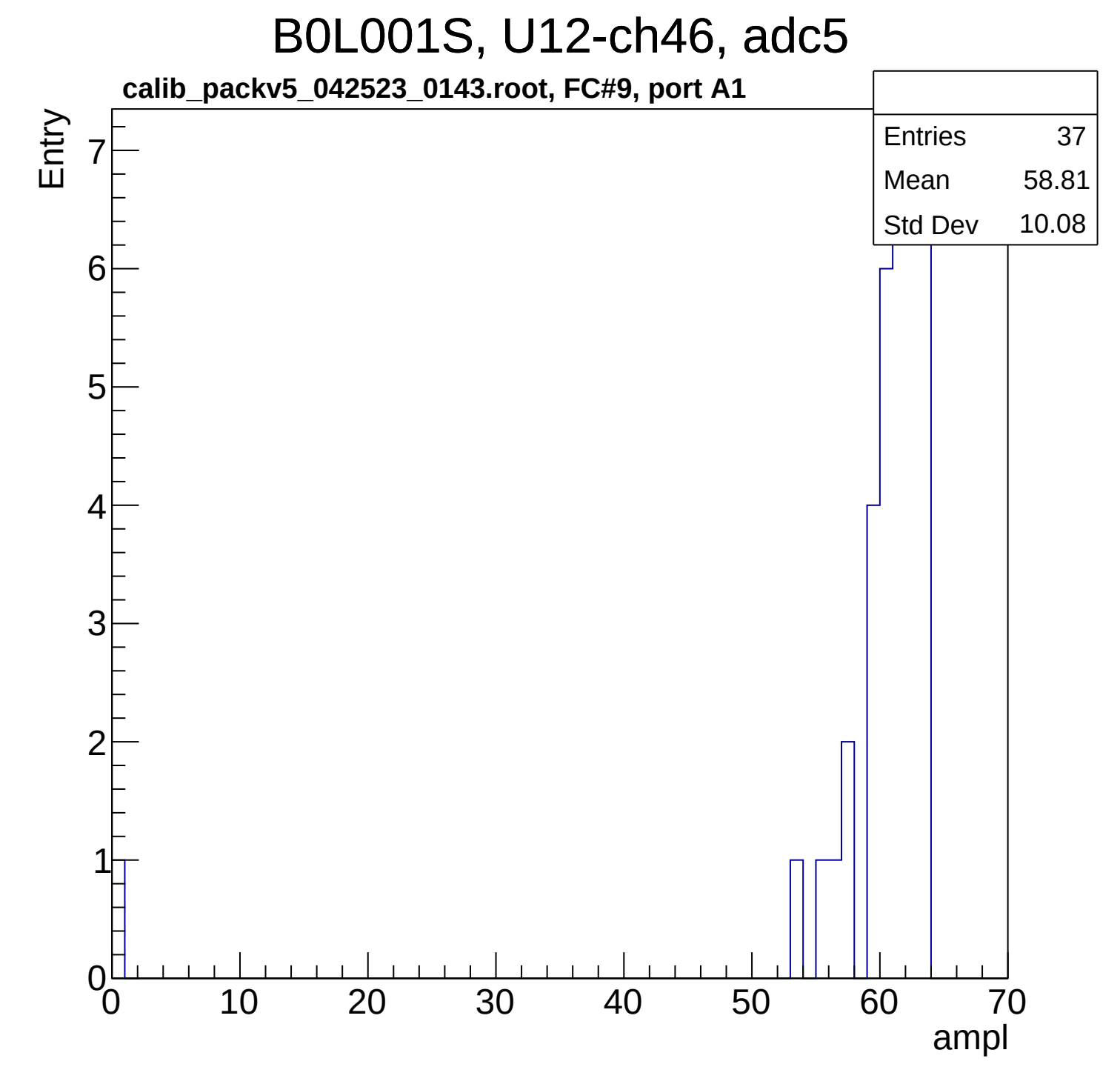
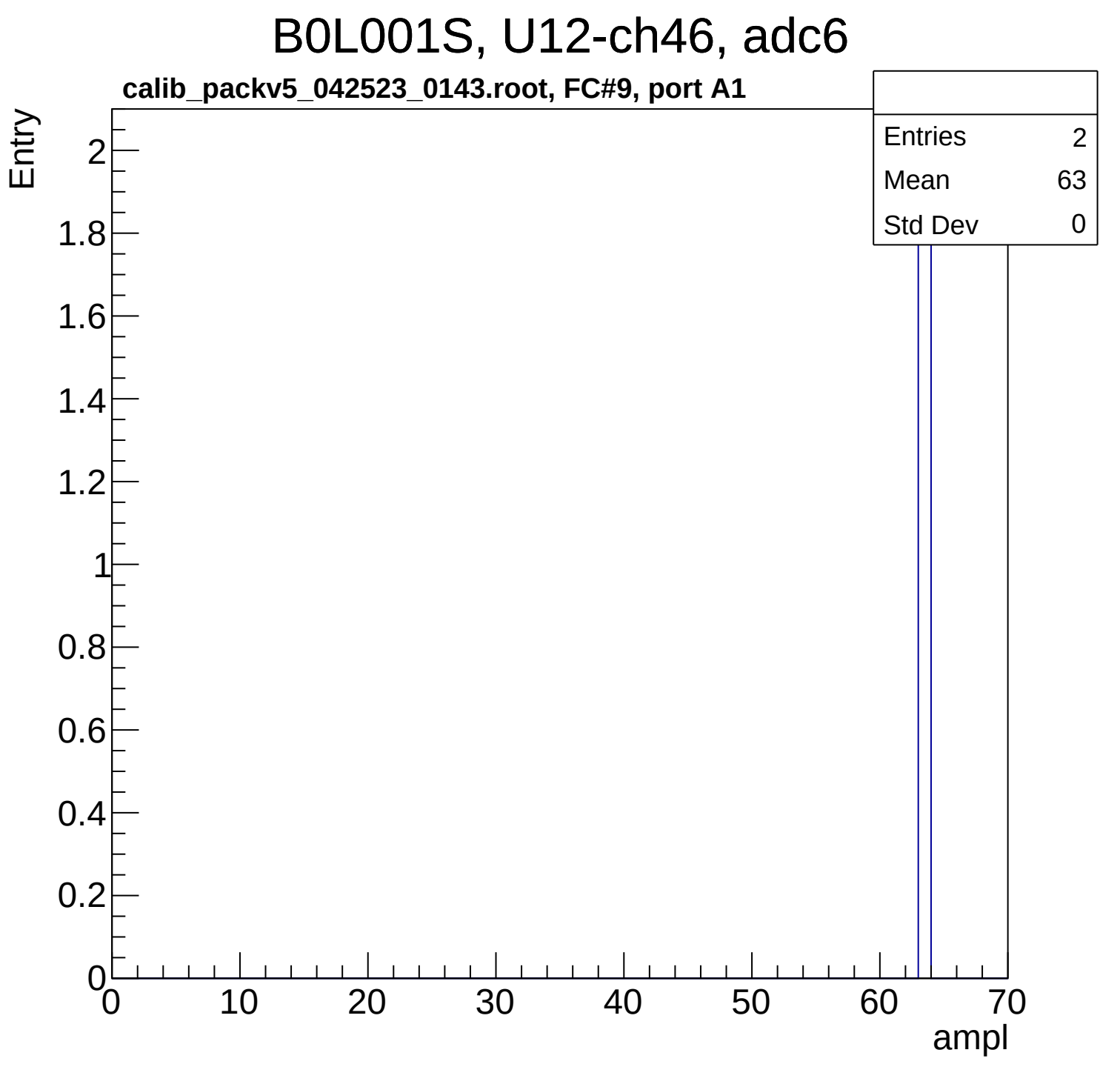

B0L001S, U12-ch46, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 57
Mean 56.93
Std Dev 2.901
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch46, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 37
Mean 58.81
Std Dev 10.08
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch46, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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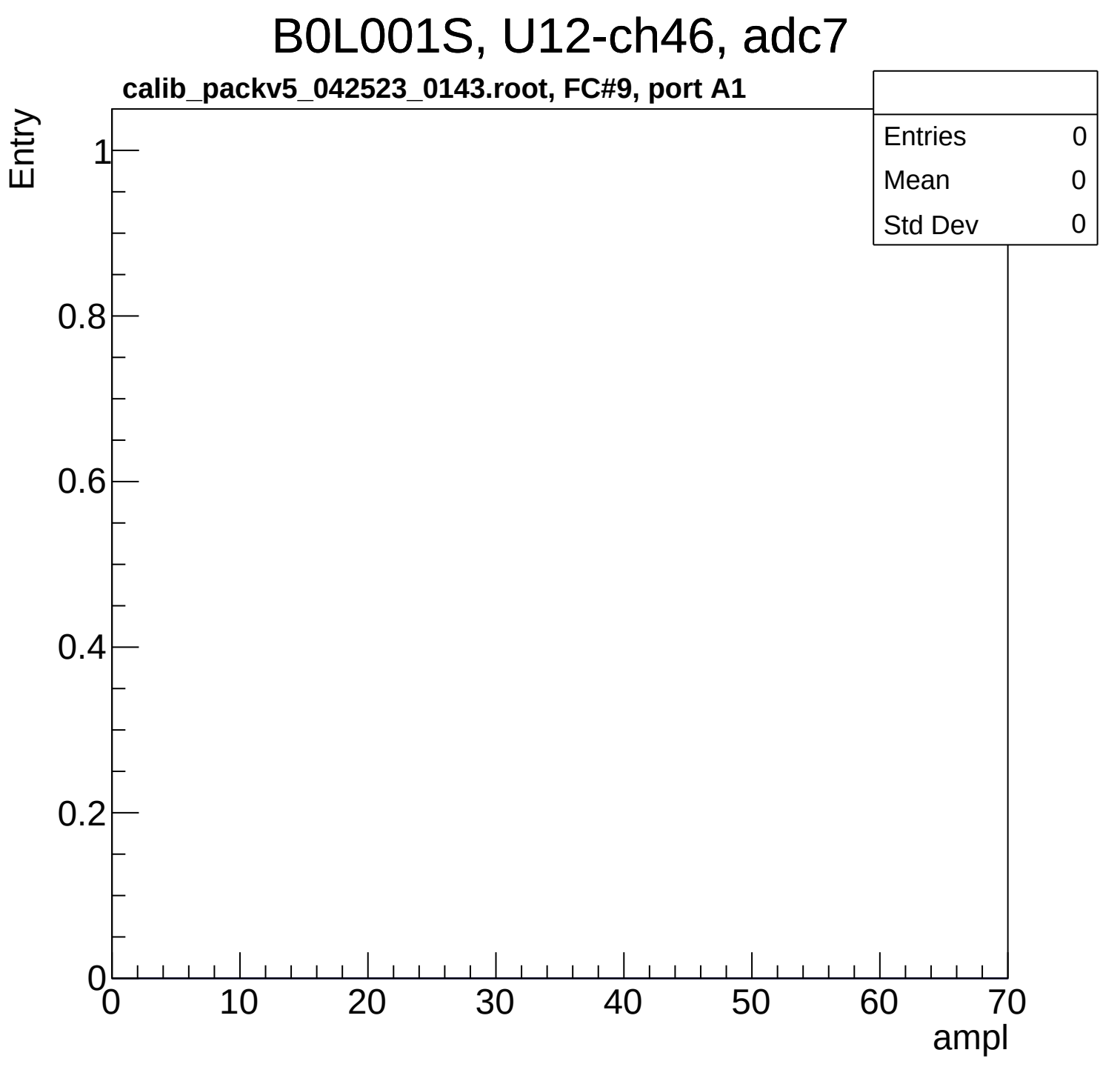
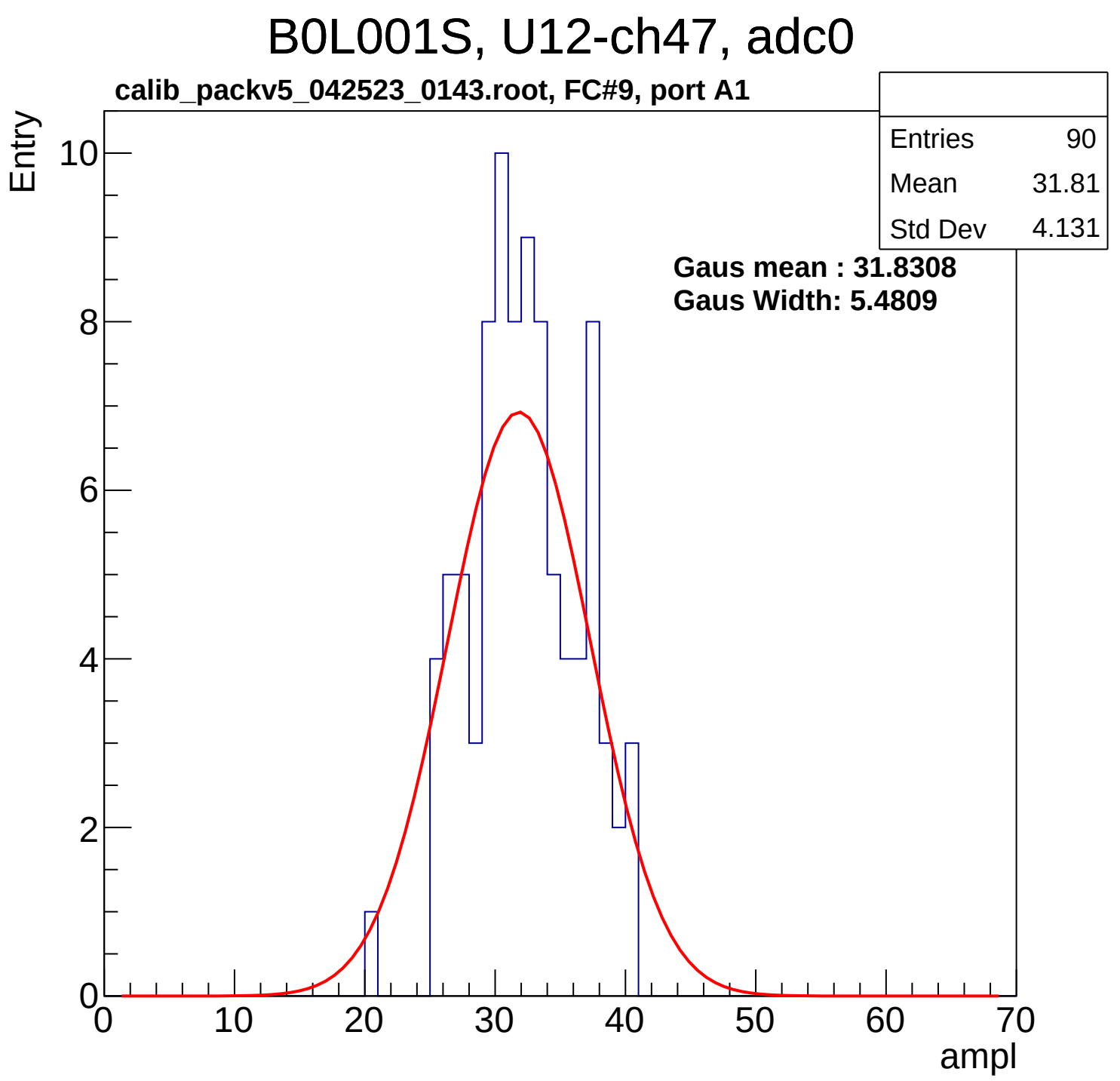
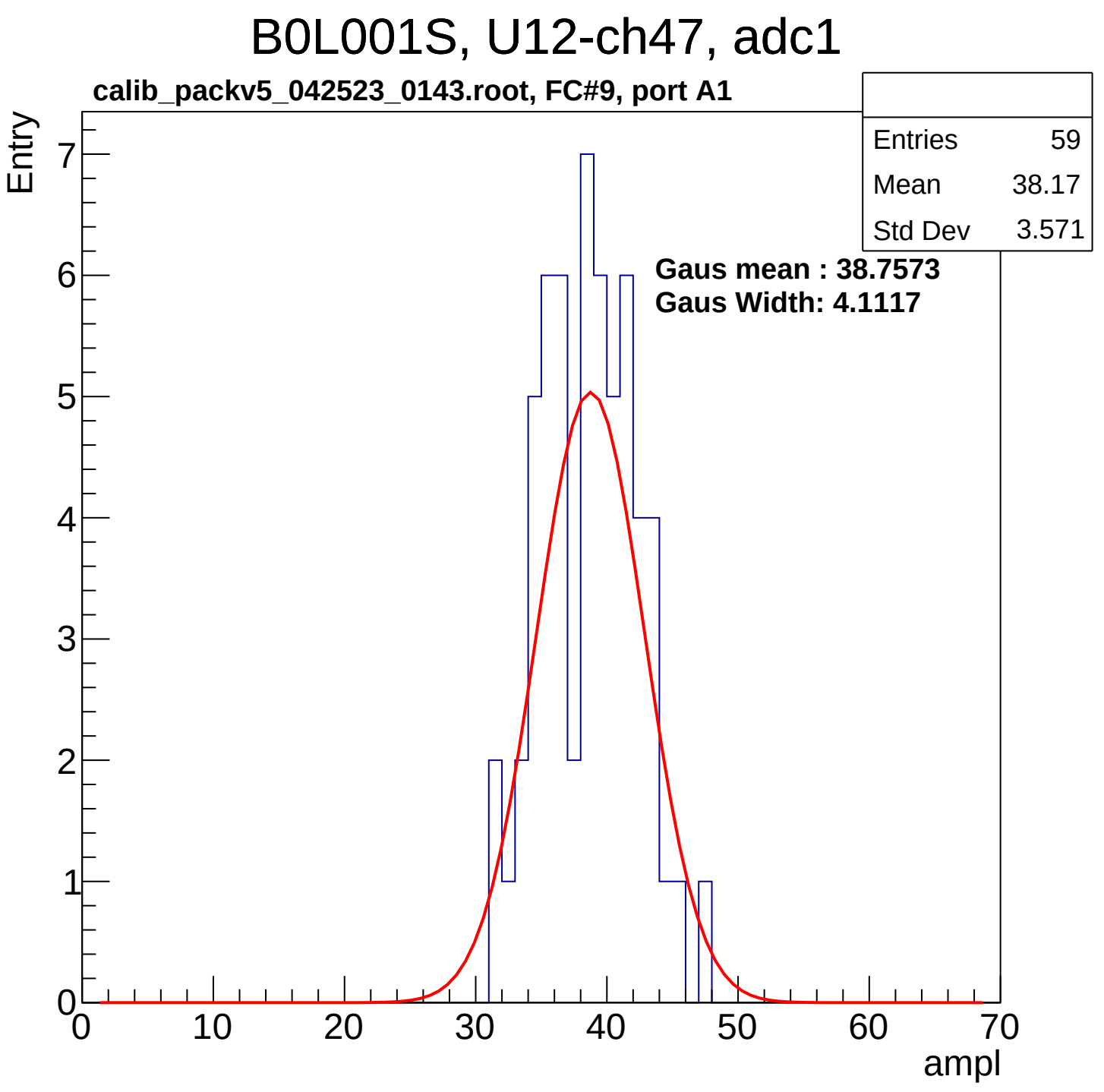
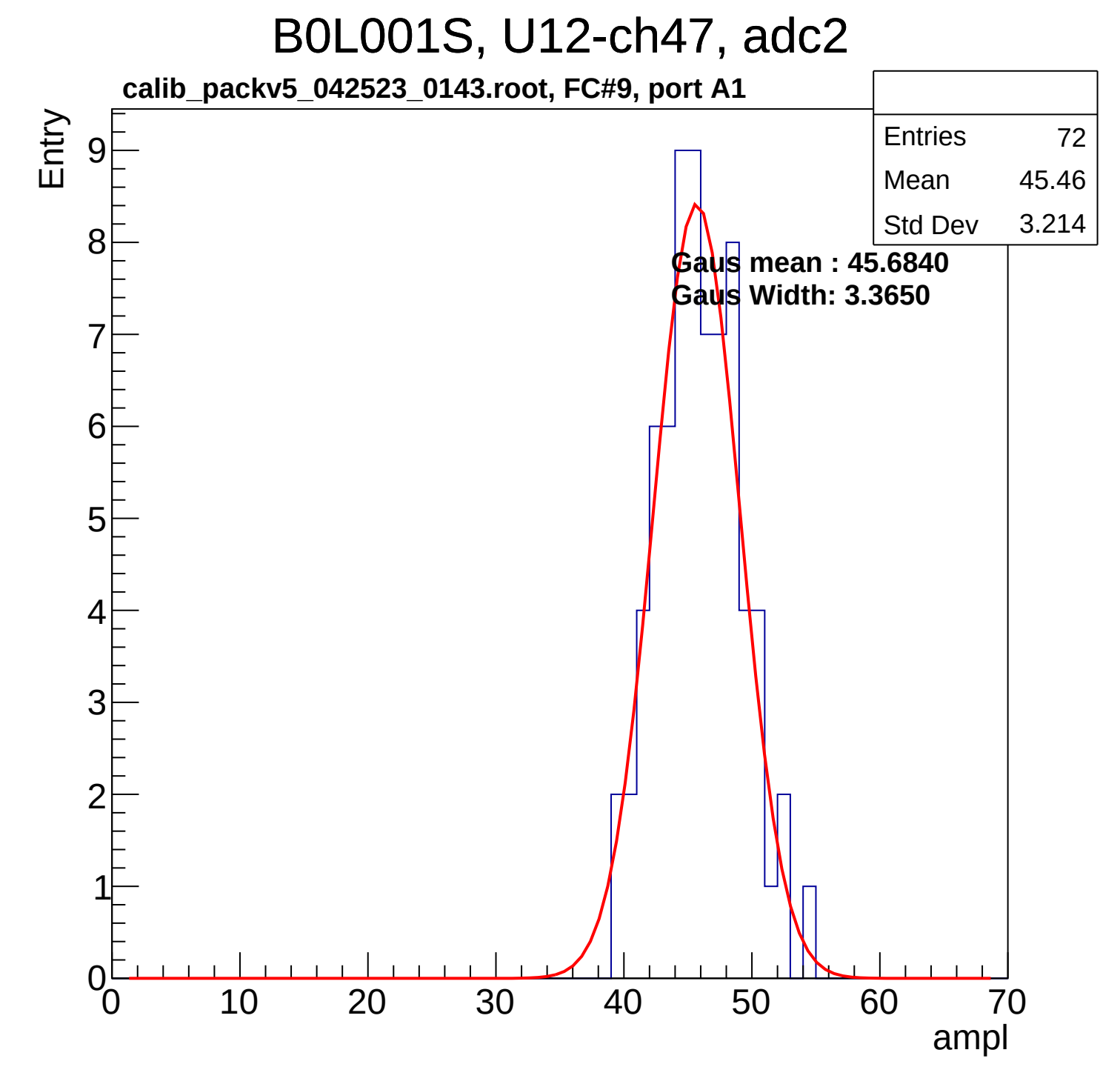
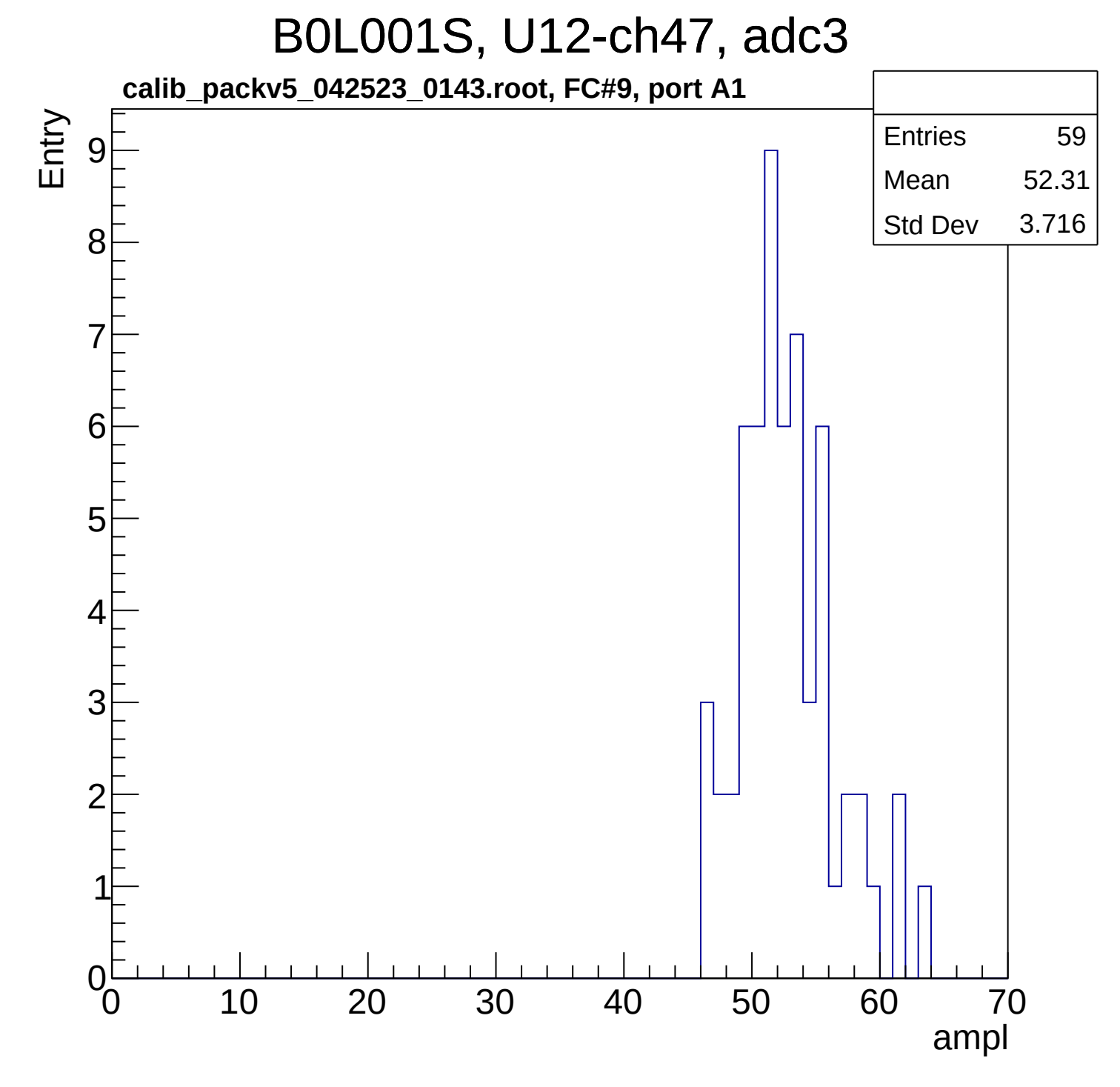
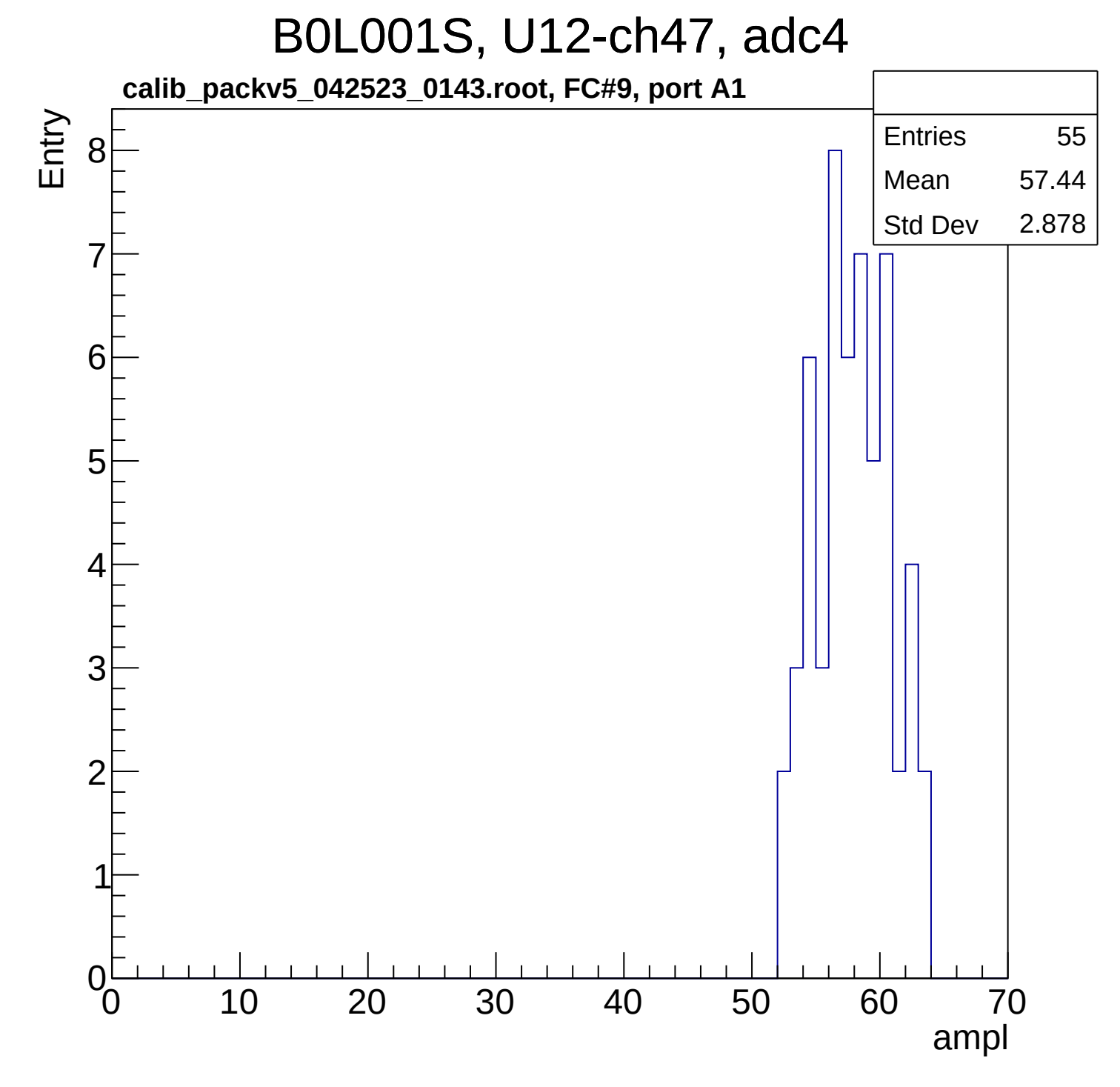

B0L001S, U12-ch46, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

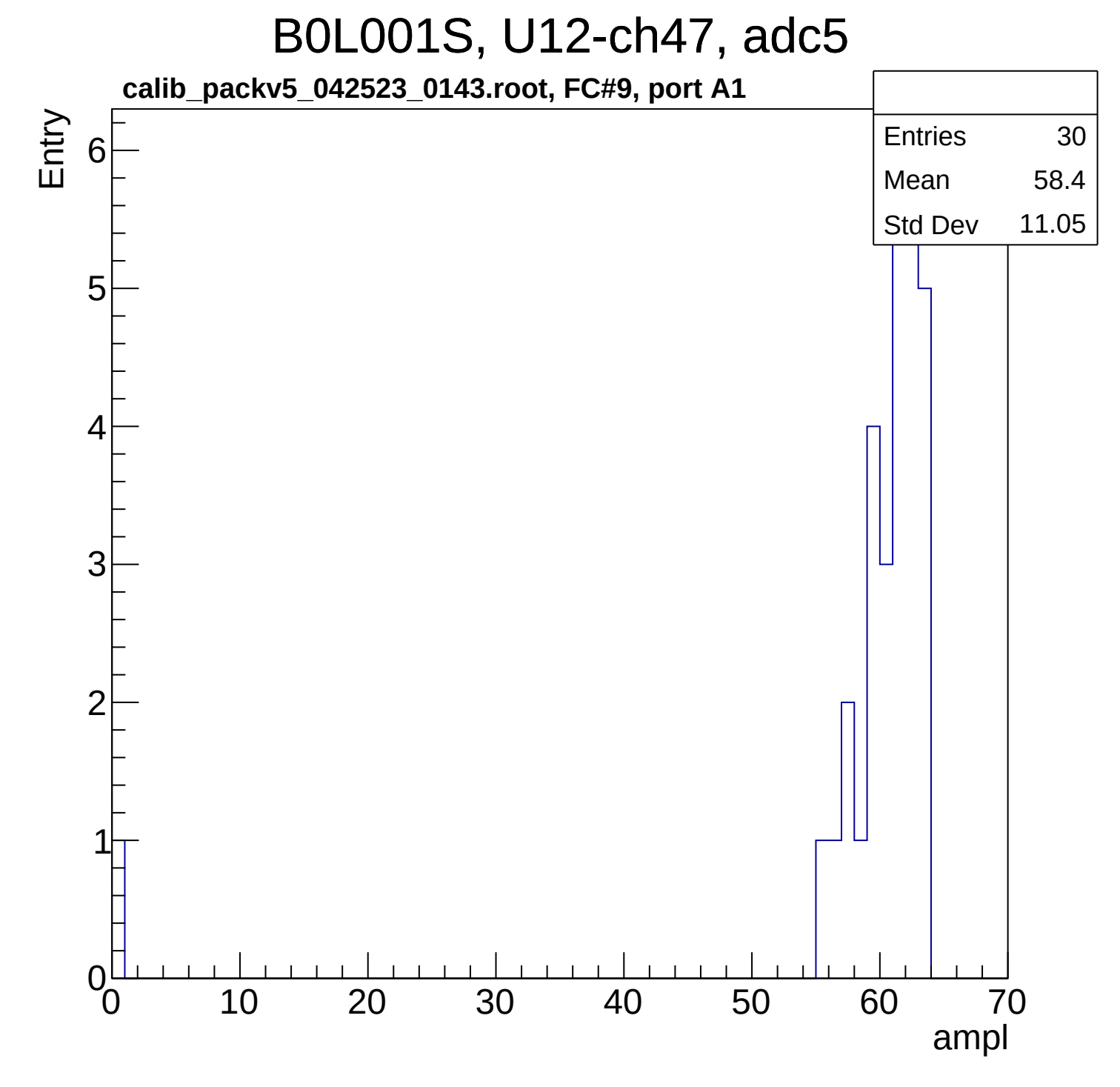

B0L001S, U12-ch47, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 90
Mean 31.81
Std Dev 4.131
Gaus mean : 31.8308
Gaus Width: 5.4809
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

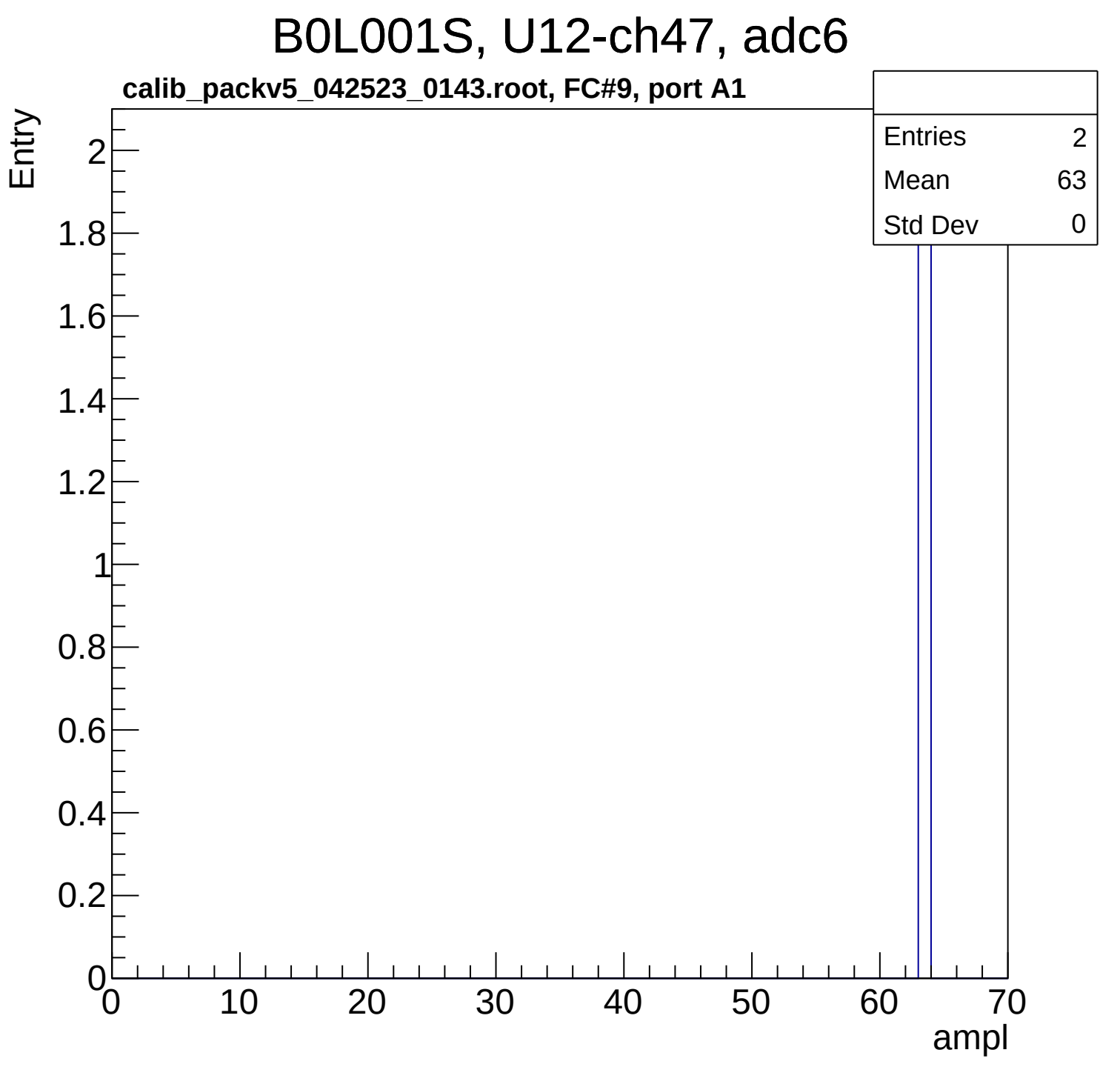

B0L001S, U12-ch47, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 59
Mean 38.17
Std Dev 3.571
Gaus mean : 38.7573
Gaus Width: 4.1117
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

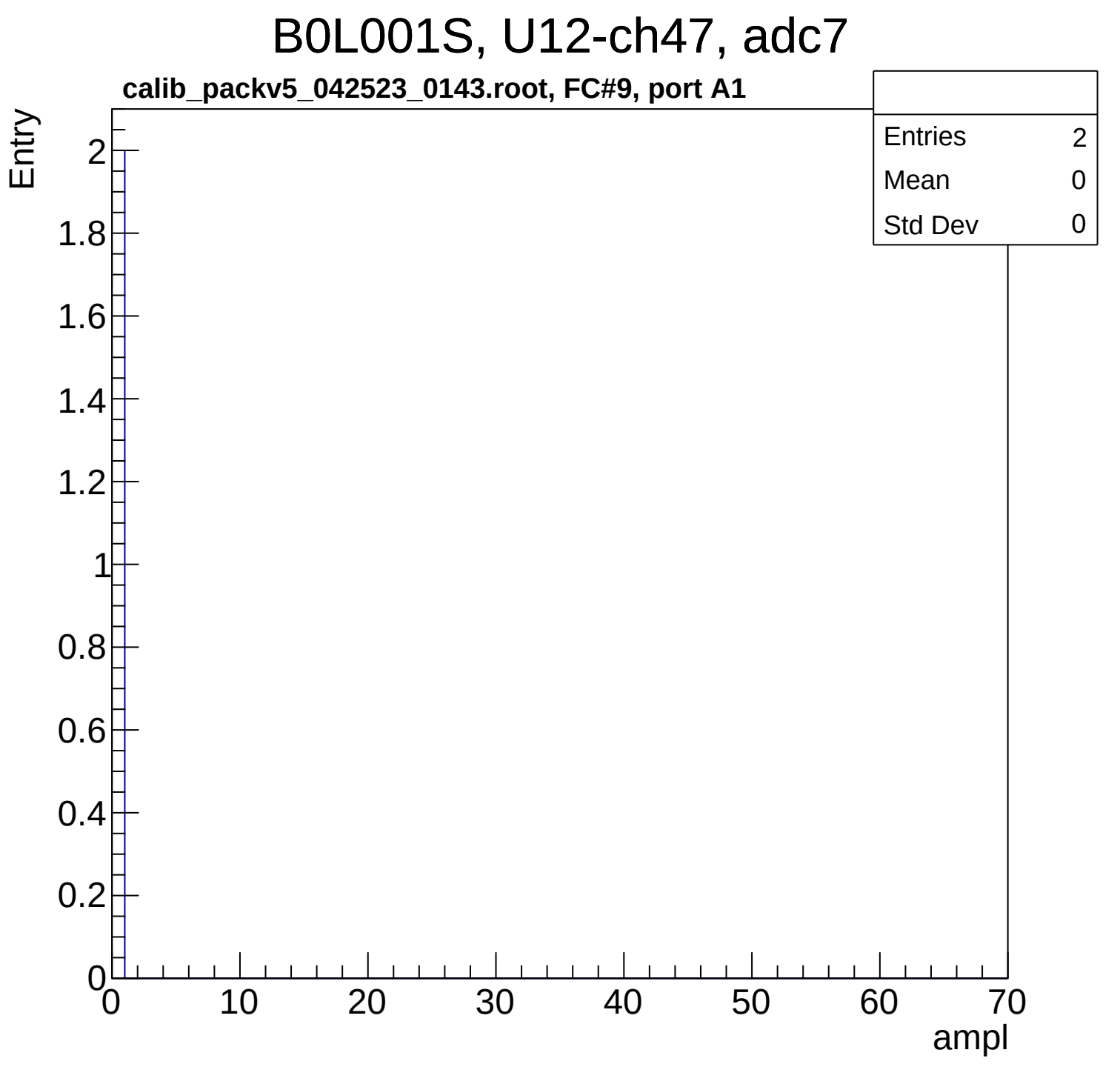

B0L001S, U12-ch47, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 72
Mean 45.46
Std Dev 3.214
Gaus mean : 45.6840
Gaus Width: 3.3650
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

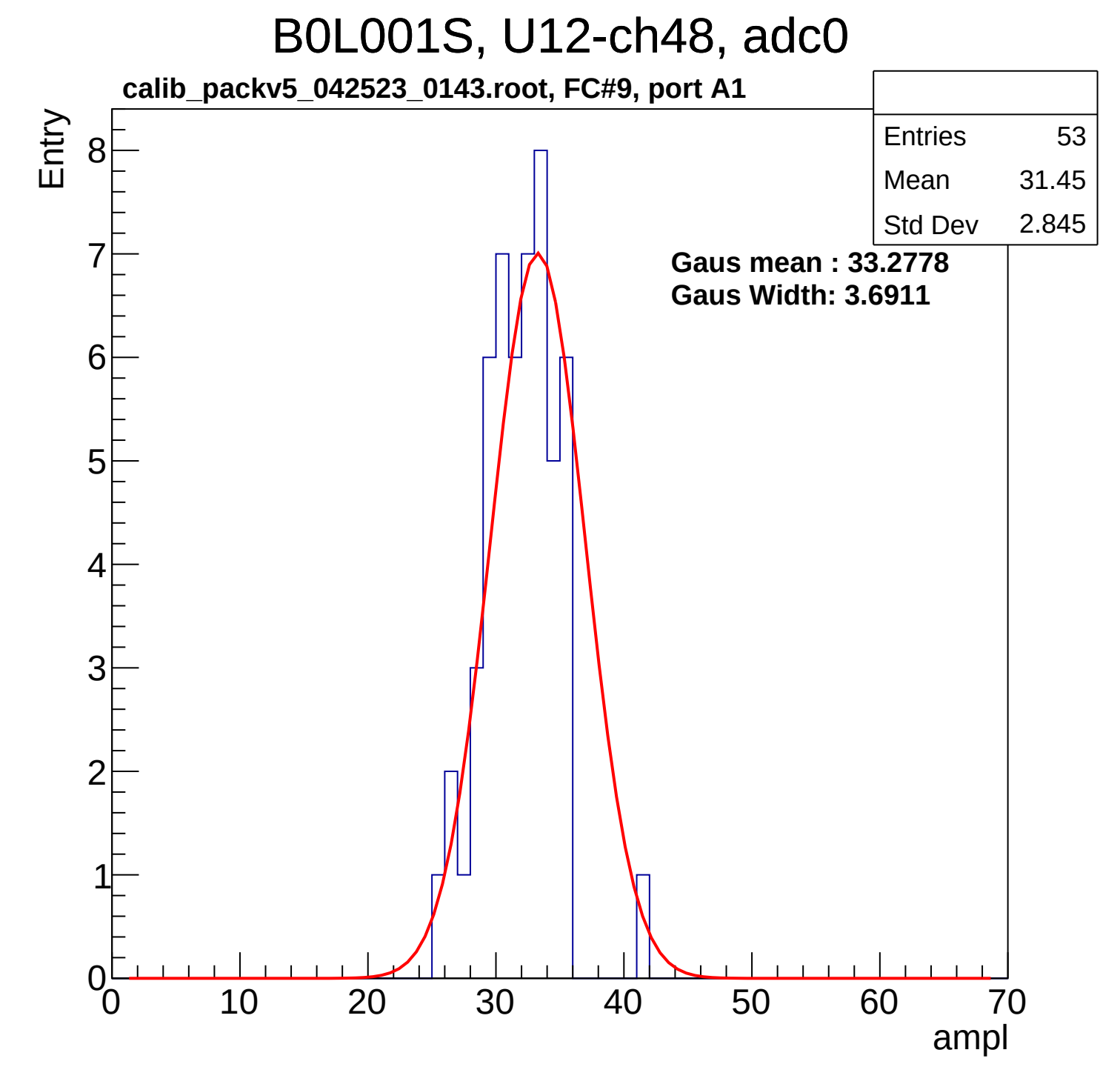

B0L001S, U12-ch47, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 59
Mean 52.31
Std Dev 3.716
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

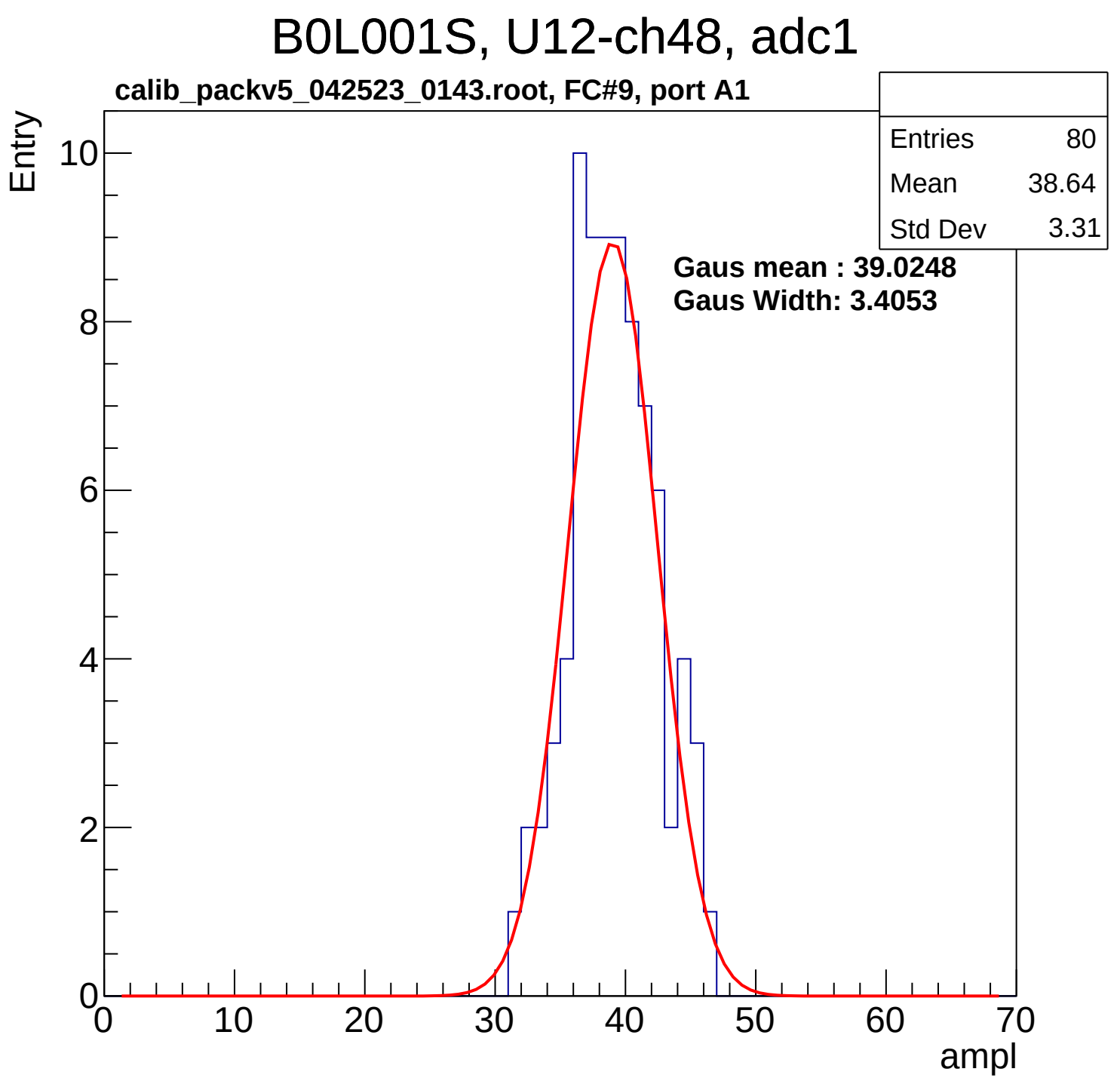

B0L001S, U12-ch47, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 55
Mean 57.44
Std Dev 2.878
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

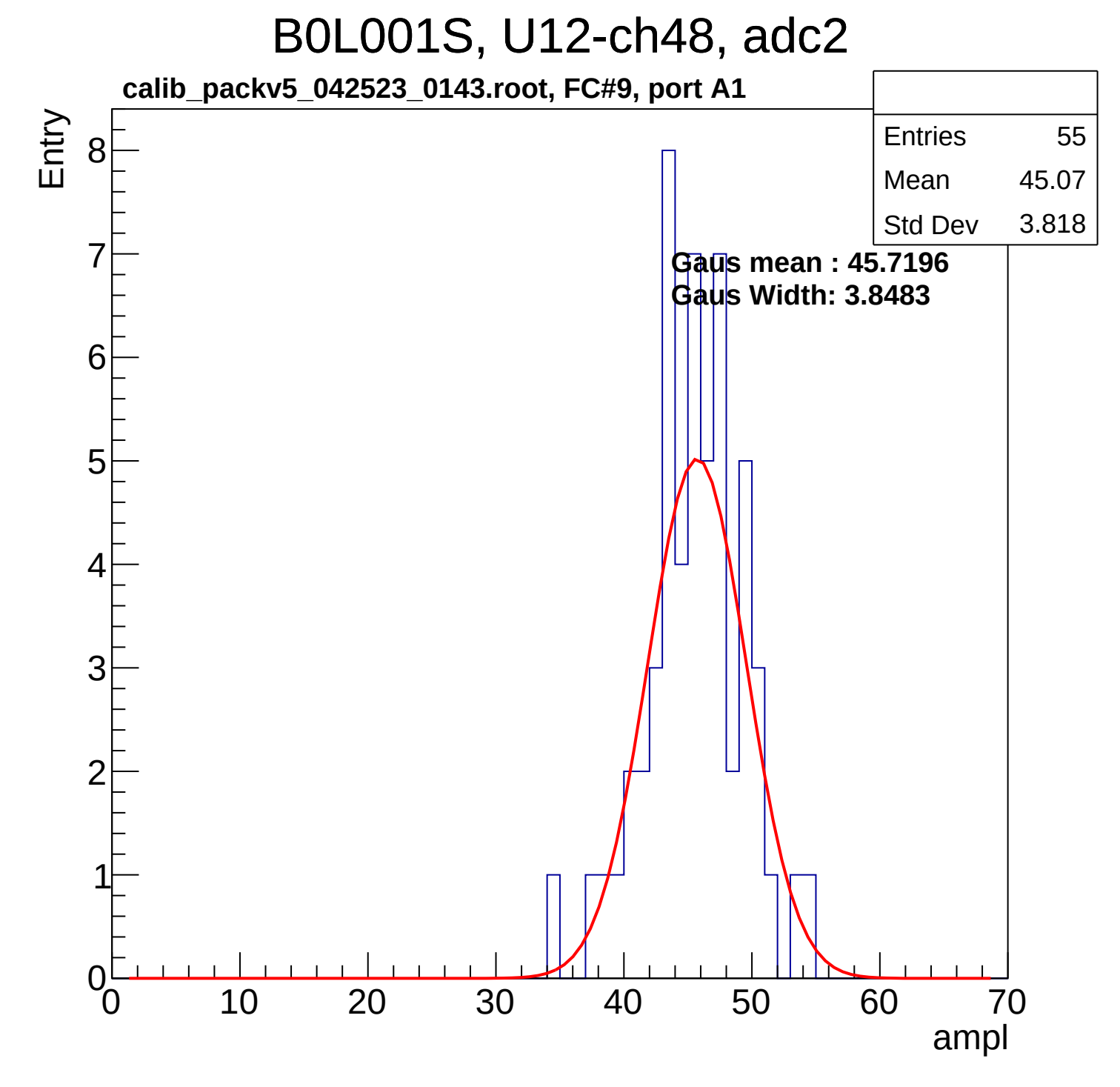

B0L001S, U12-ch47, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 30
Mean 58.4
Std Dev 11.05
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

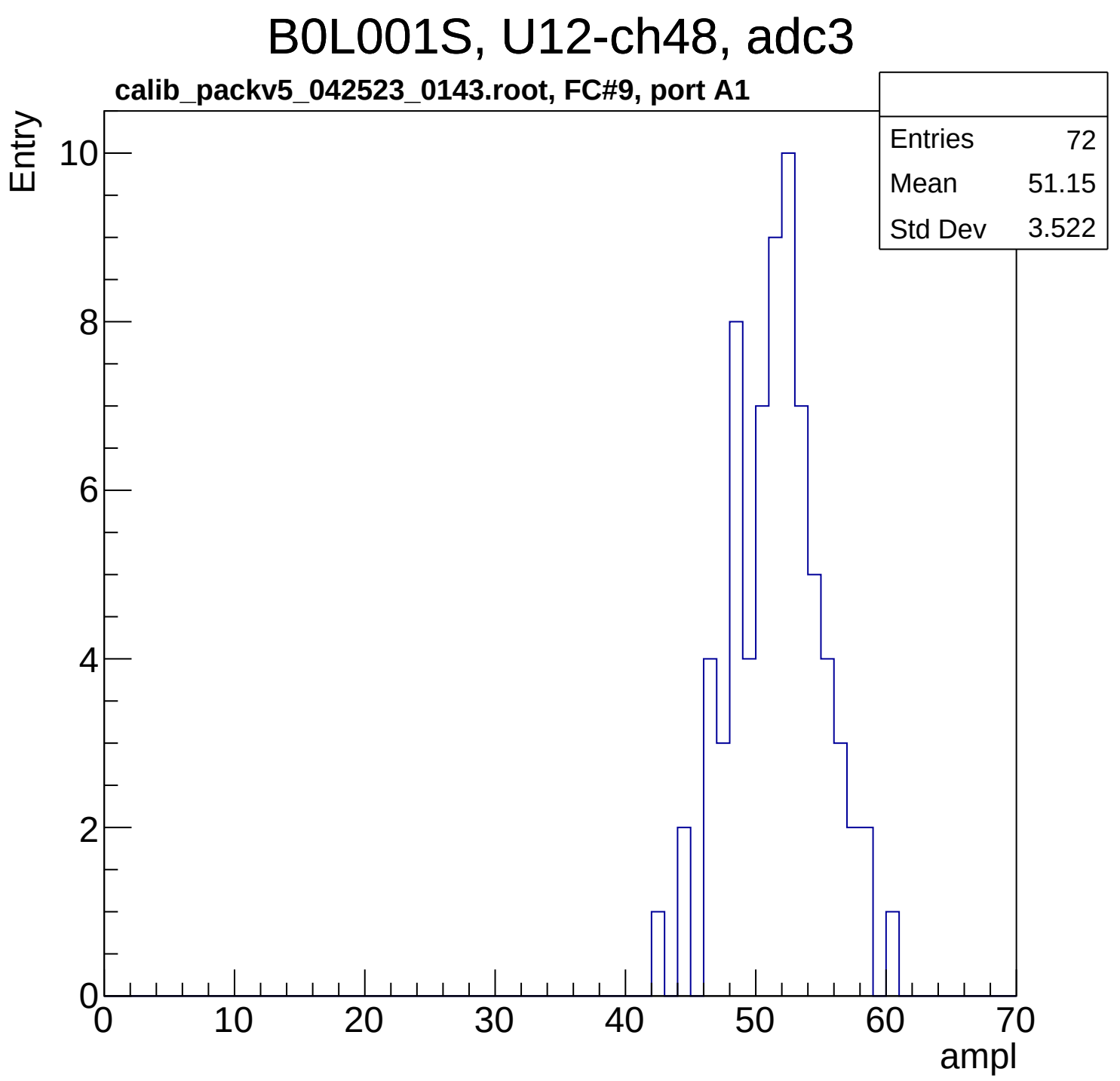

B0L001S, U12-ch47, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

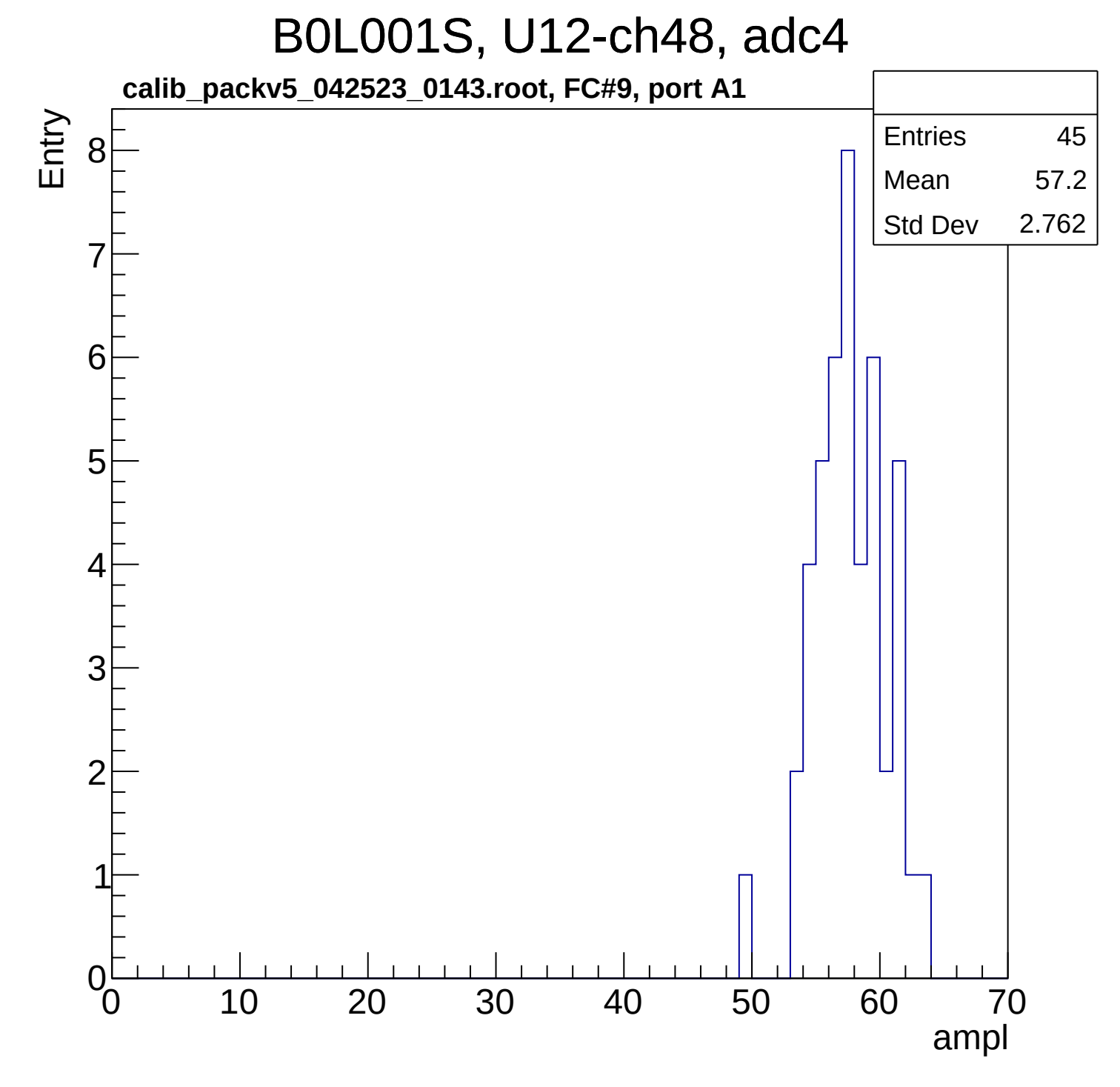

B0L001S, U12-ch47, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

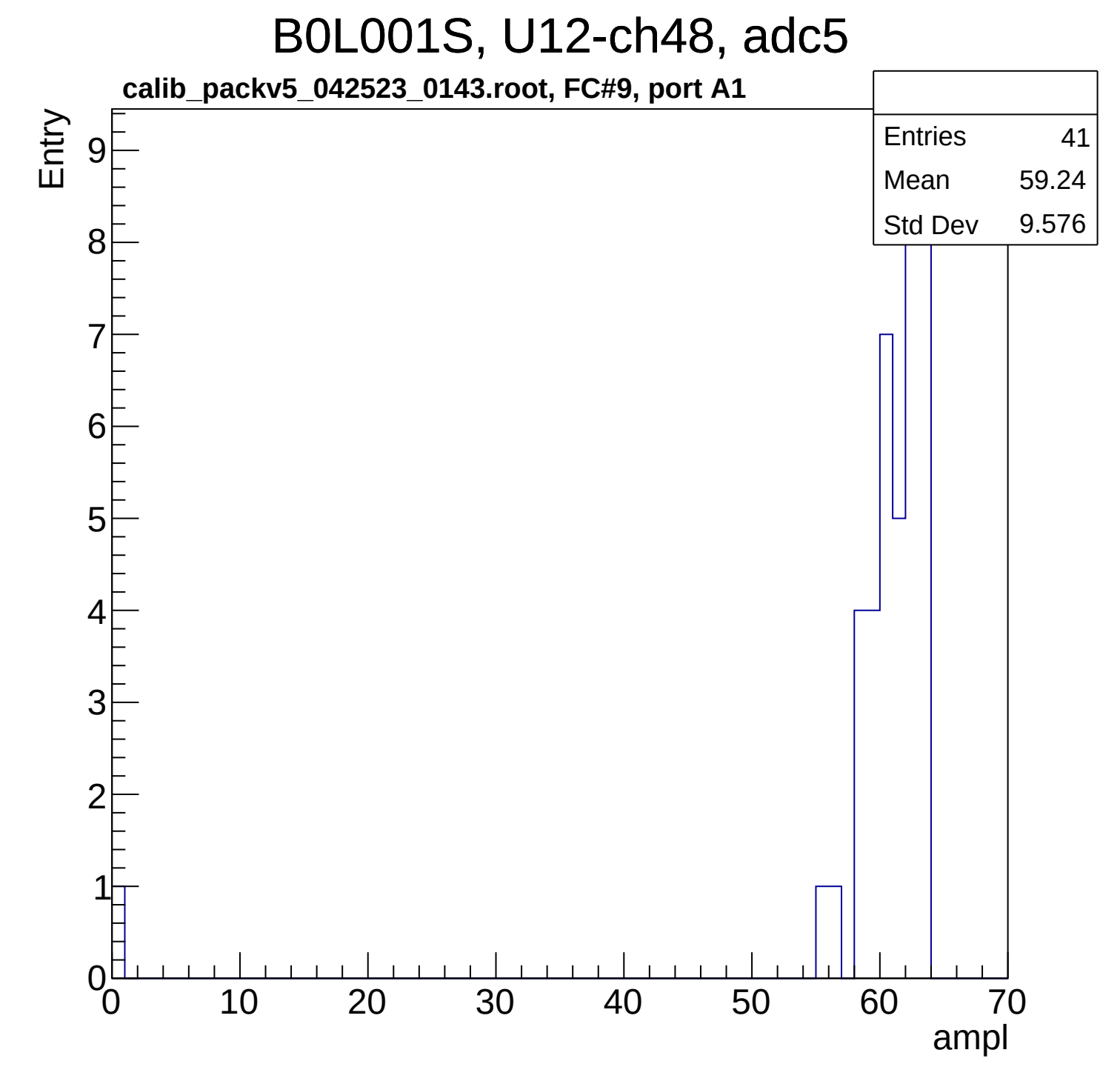

B0L001S, U12-ch48, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 53
Mean 31.45
Std Dev 2.845
Gaus mean : 33.2778
Gaus Width: 3.6911
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch48, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 80
Mean 38.64
Std Dev 3.31
Gaus mean : 39.0248
Gaus Width: 3.4053
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch48, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 55
Mean 45.07
Std Dev 3.818
Gaus mean : 45.7196
Gaus Width: 3.8483
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch48, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 72
Mean 51.15
Std Dev 3.522
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch48, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 45
Mean 57.2
Std Dev 2.762
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch48, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 41
Mean 59.24
Std Dev 9.576
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
50
60
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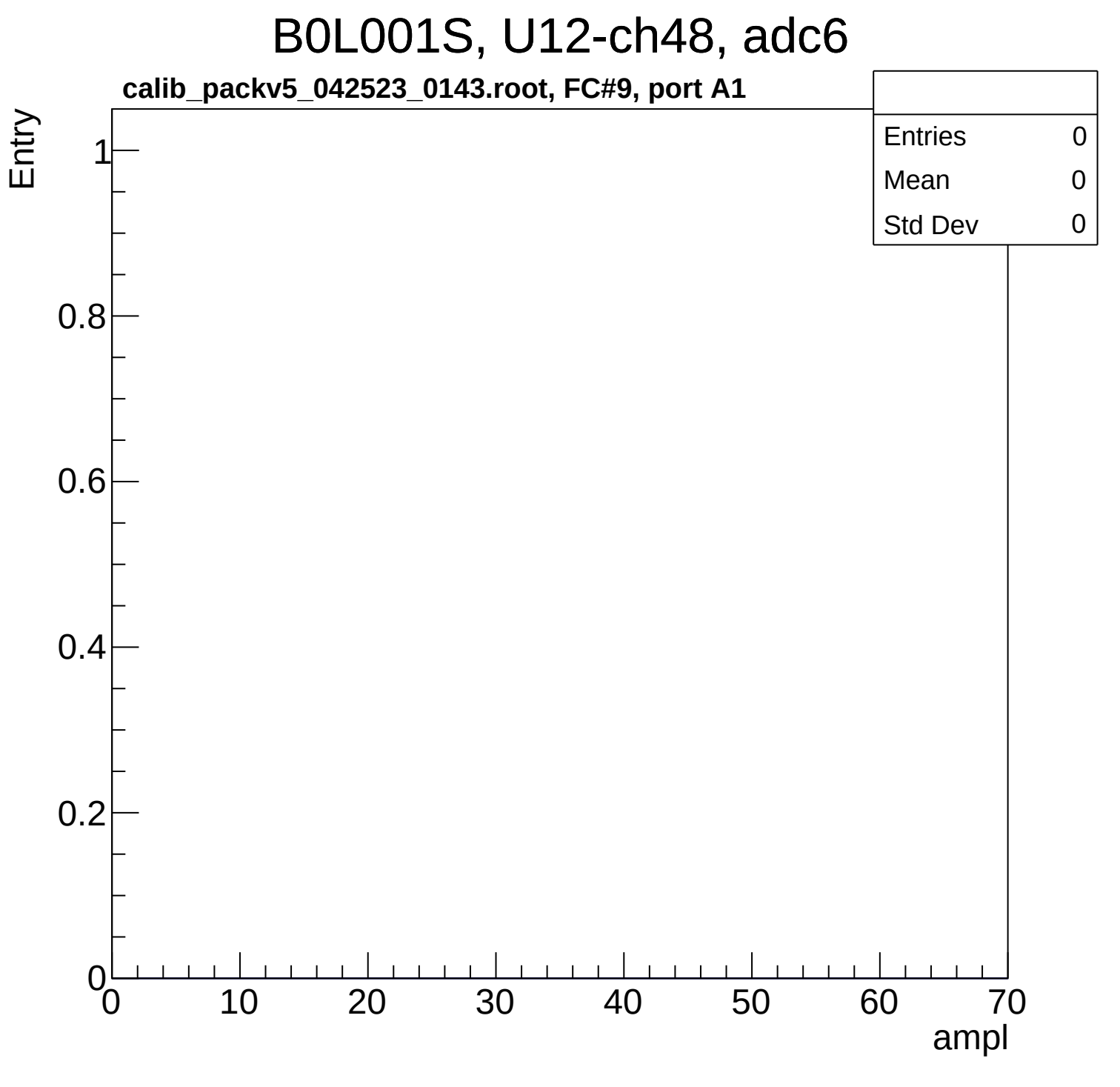
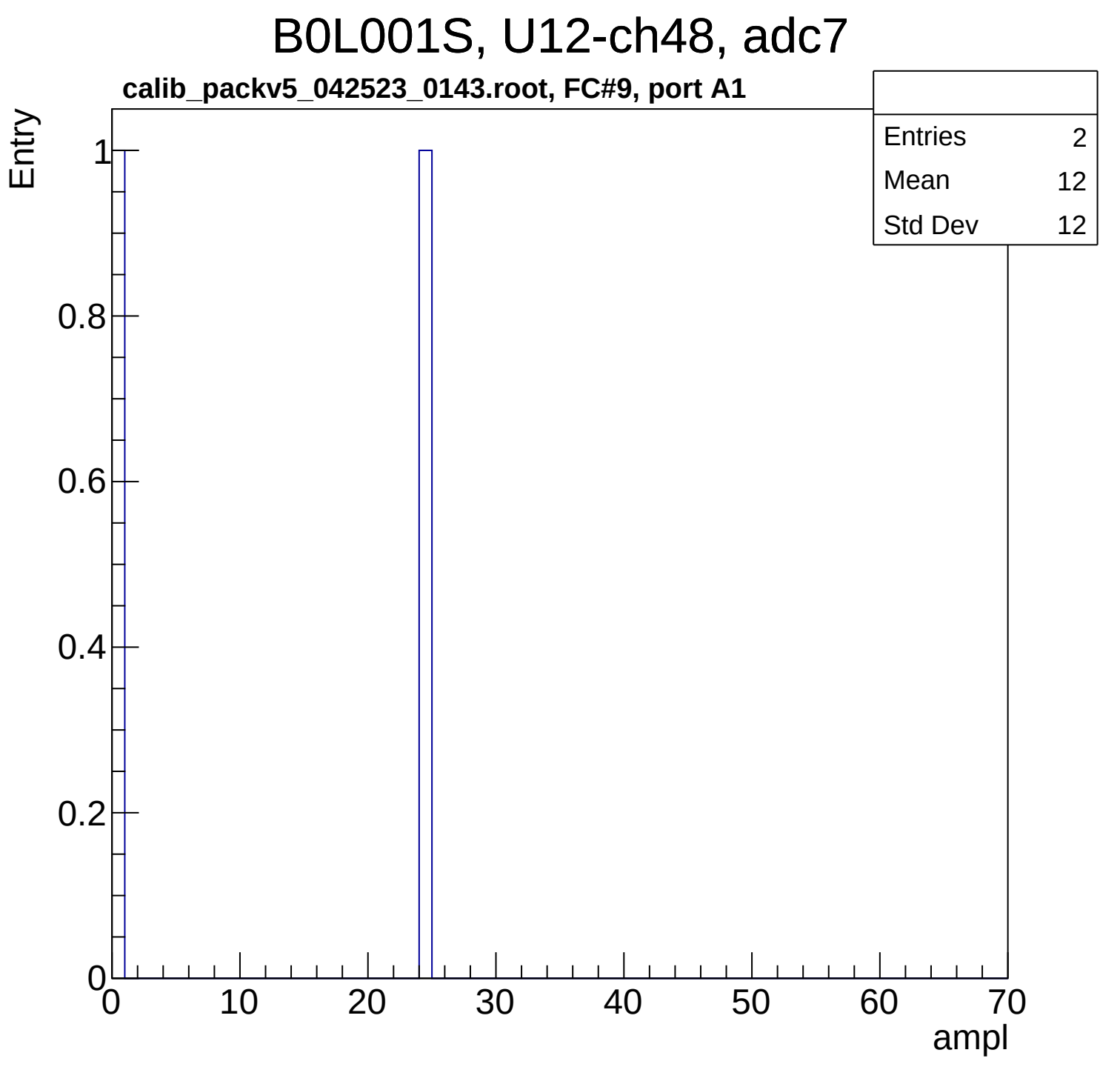

B0L001S, U12-ch48, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch48, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 12
Std Dev 12
Entry
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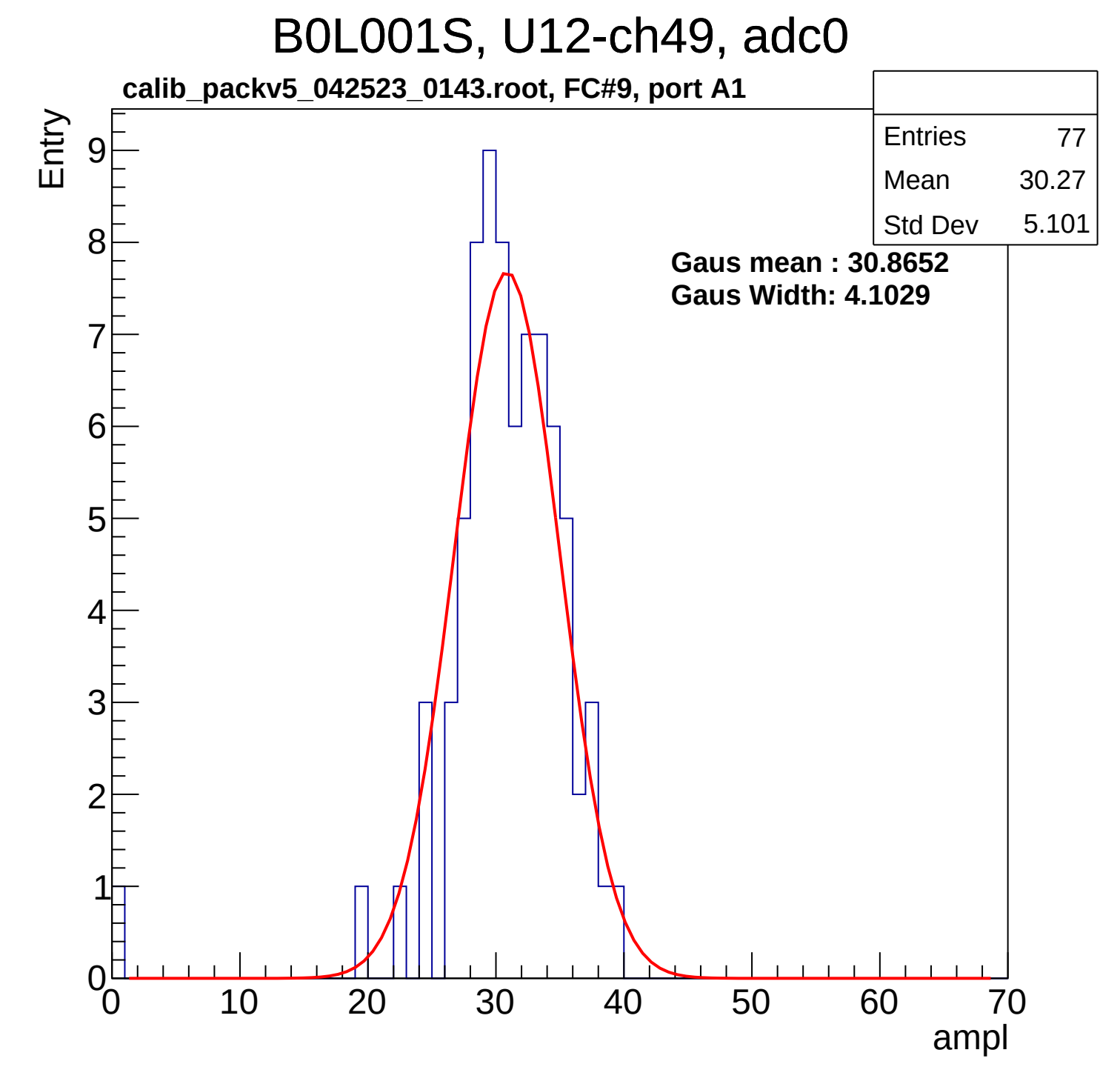
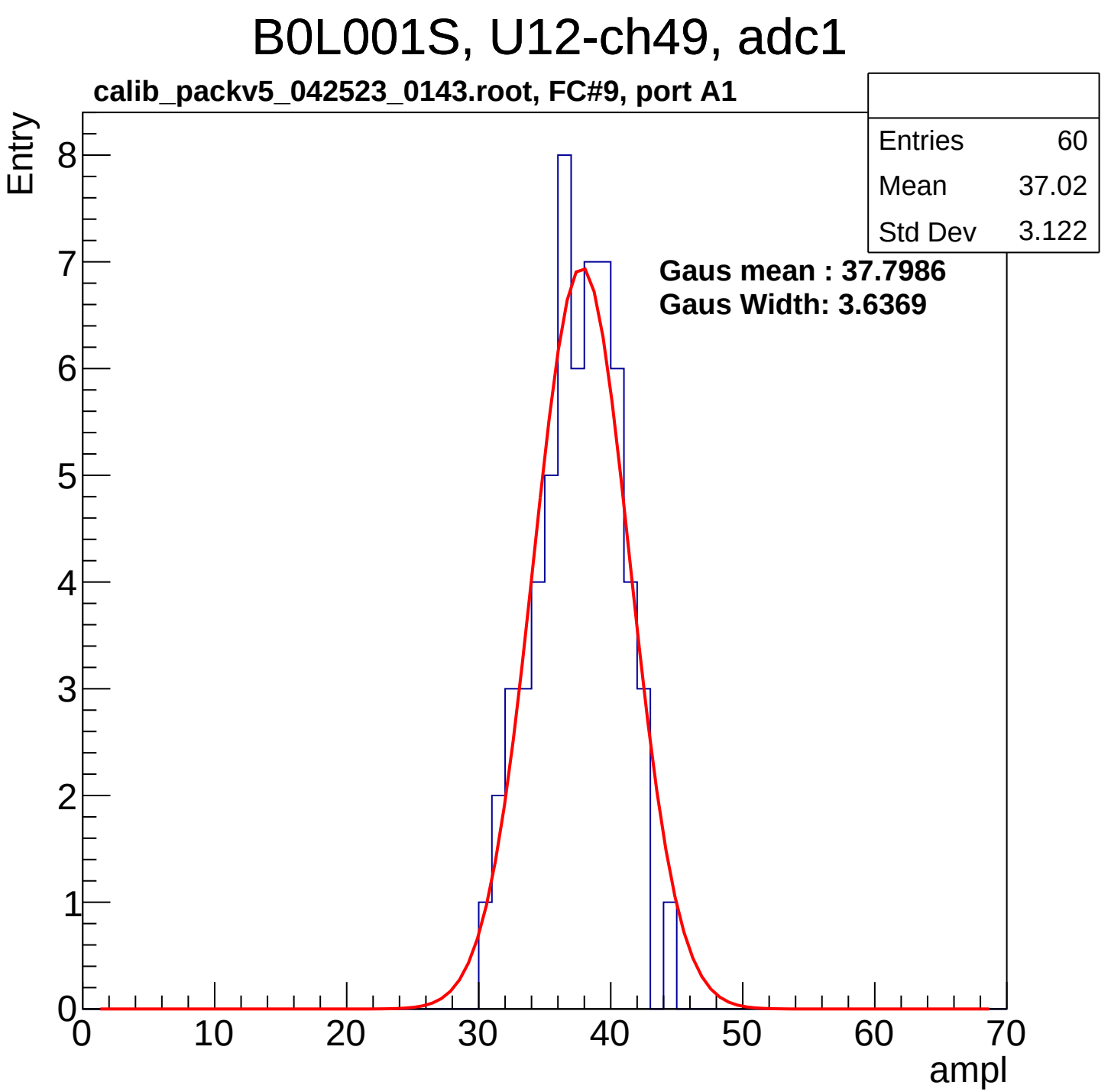
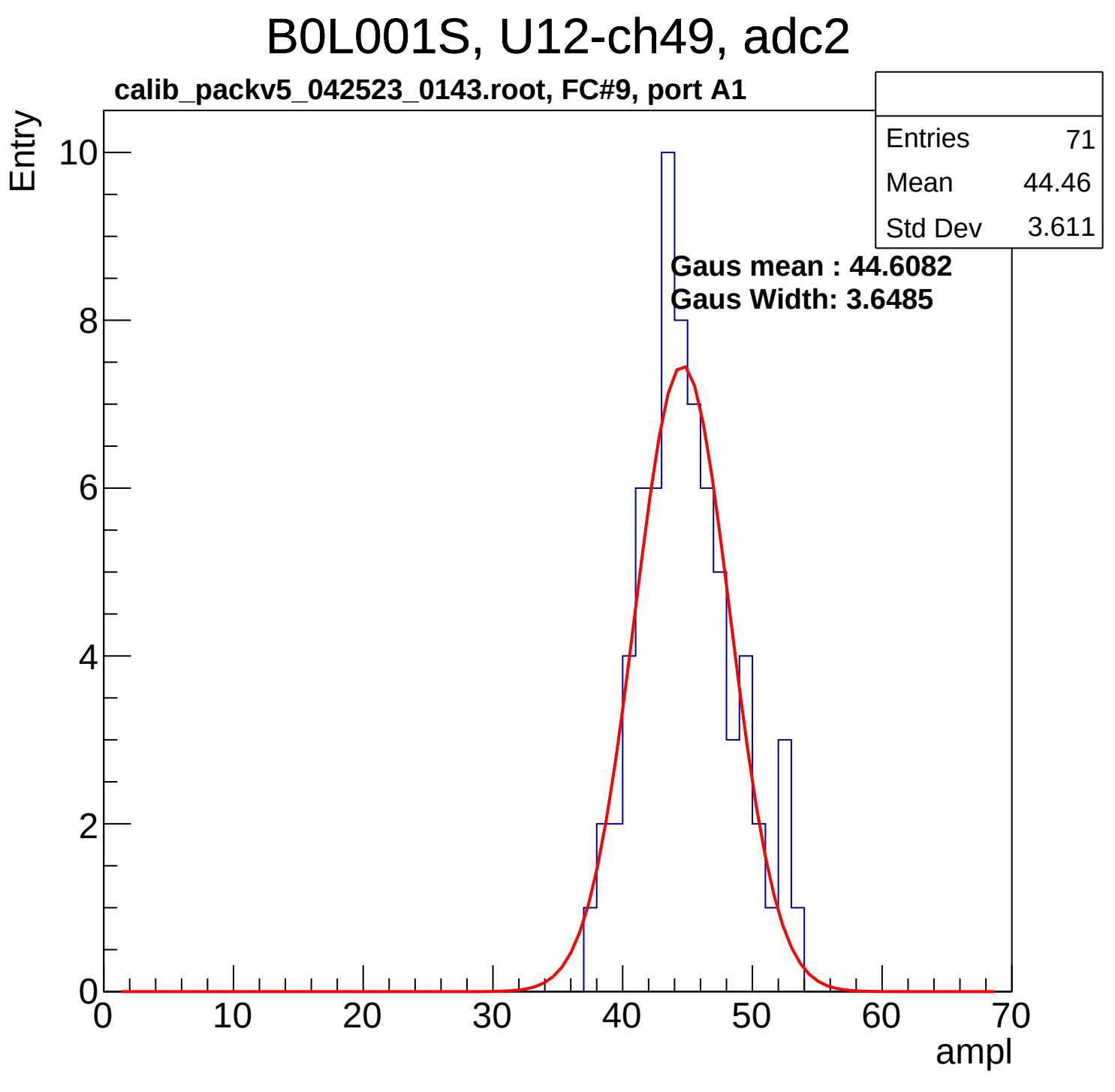
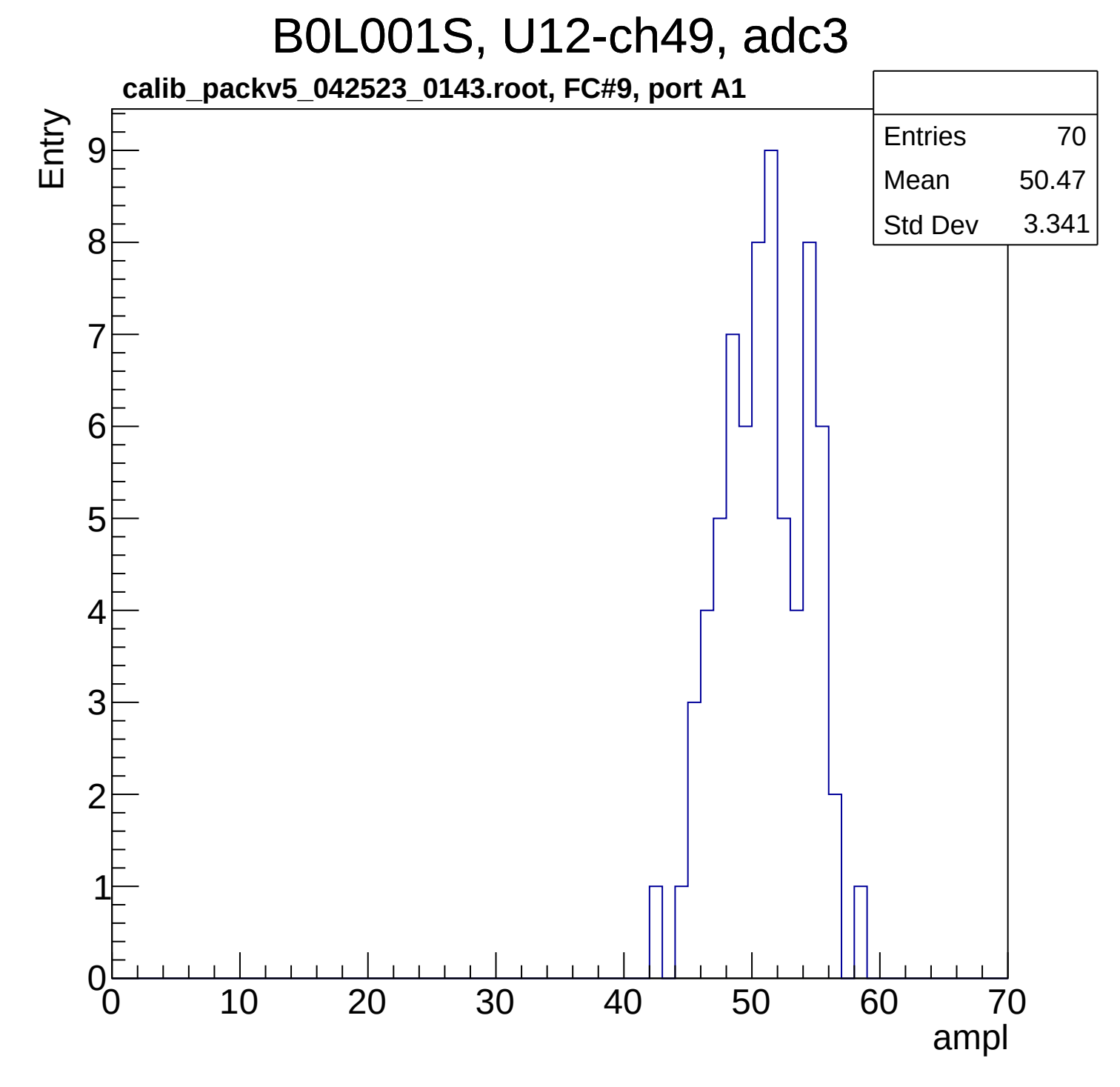
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch49, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 77
Mean 30.27
Std Dev 5.101
Gaus mean : 30.8652
Gaus Width: 4.1029
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch49, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 60
Mean 37.02
Std Dev 3.122
Gaus mean : 37.7986
Gaus Width: 3.6369
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch49, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 71
Mean 44.46
Std Dev 3.611
Gaus mean : 44.6082
Gaus Width: 3.6485
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch49, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 70
Mean 50.47
Std Dev 3.341
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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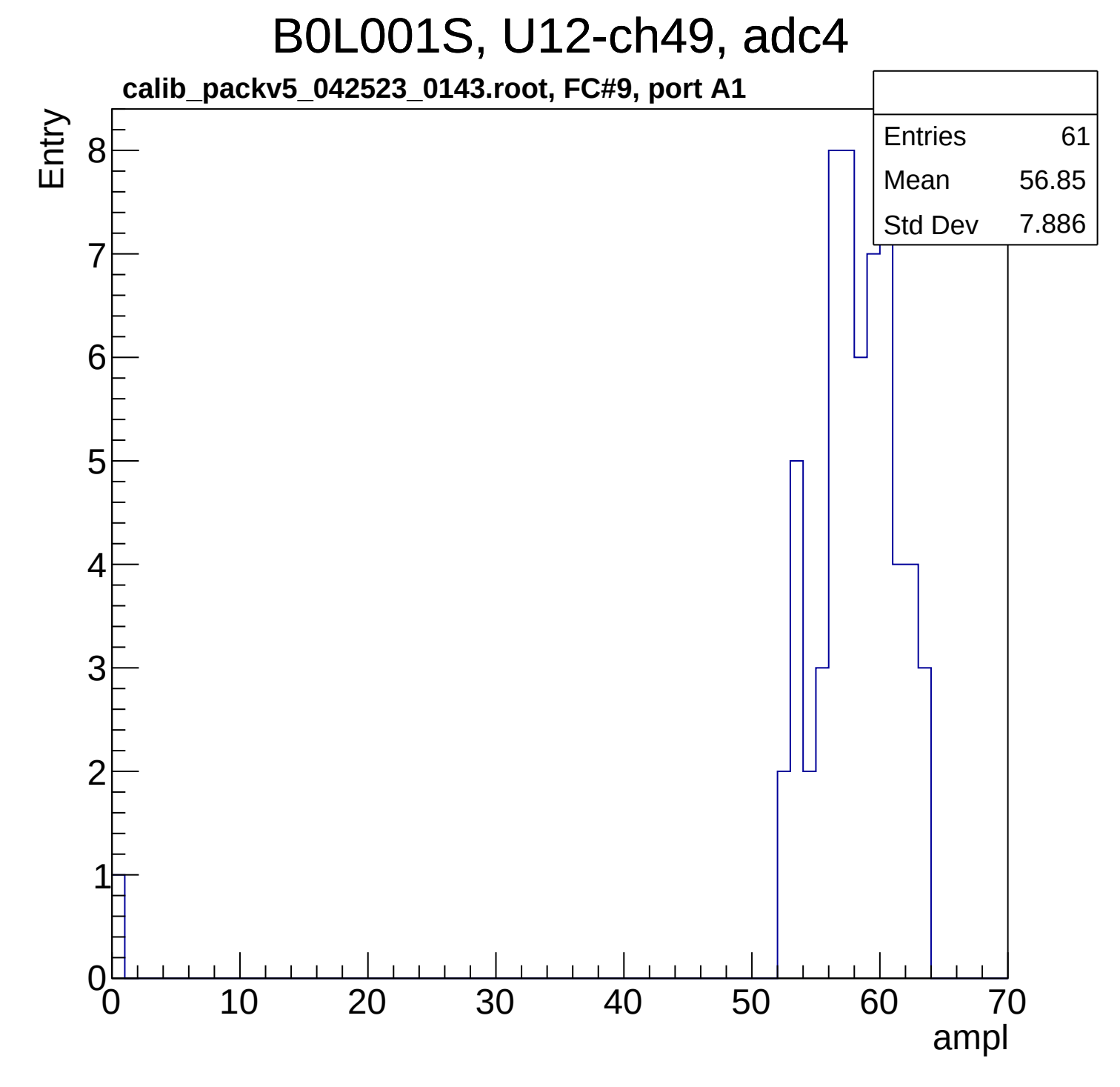
B0L001S, U12-ch49, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 61
Mean 56.85
Std Dev 7.886
Entry
ampl
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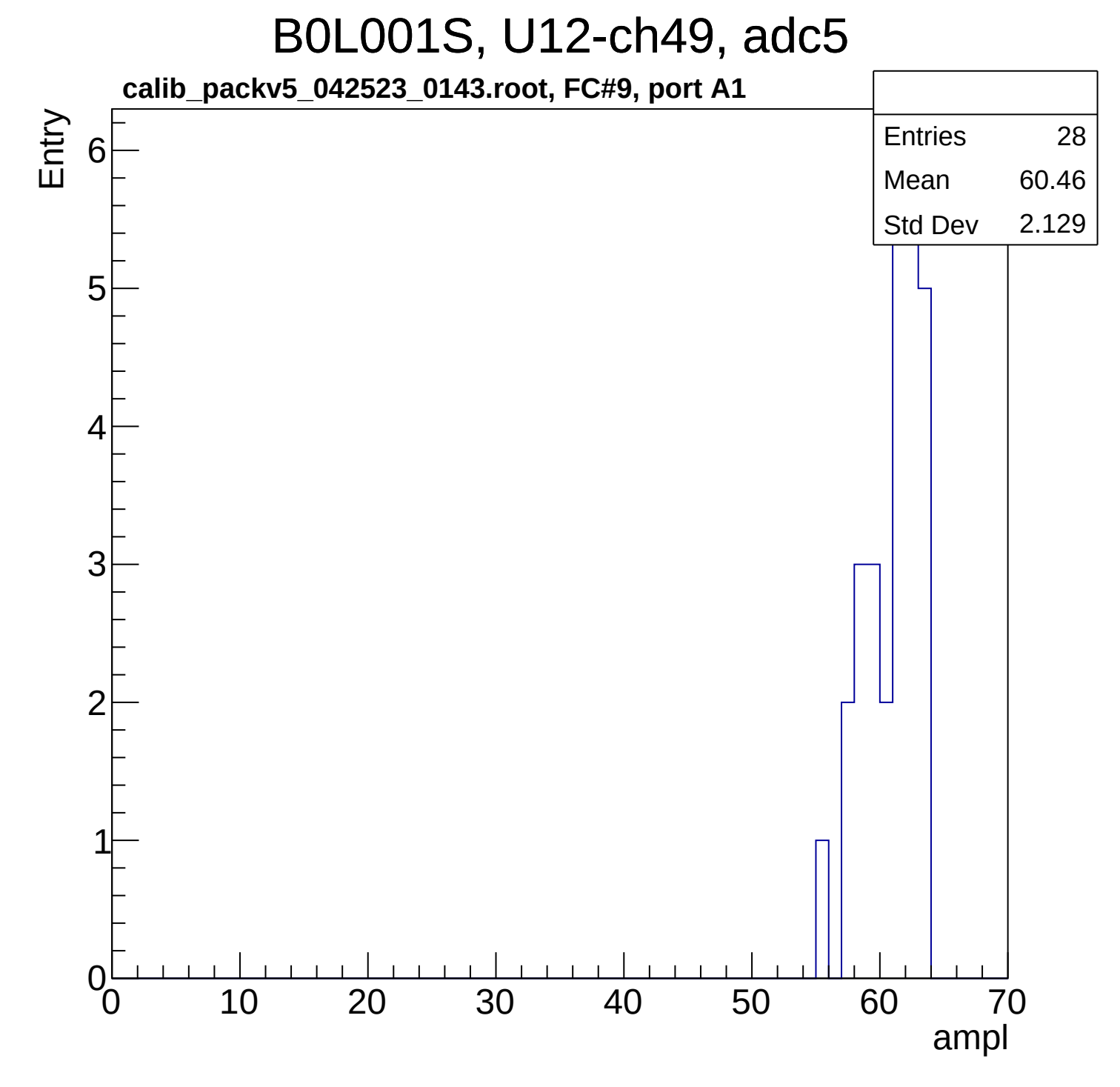
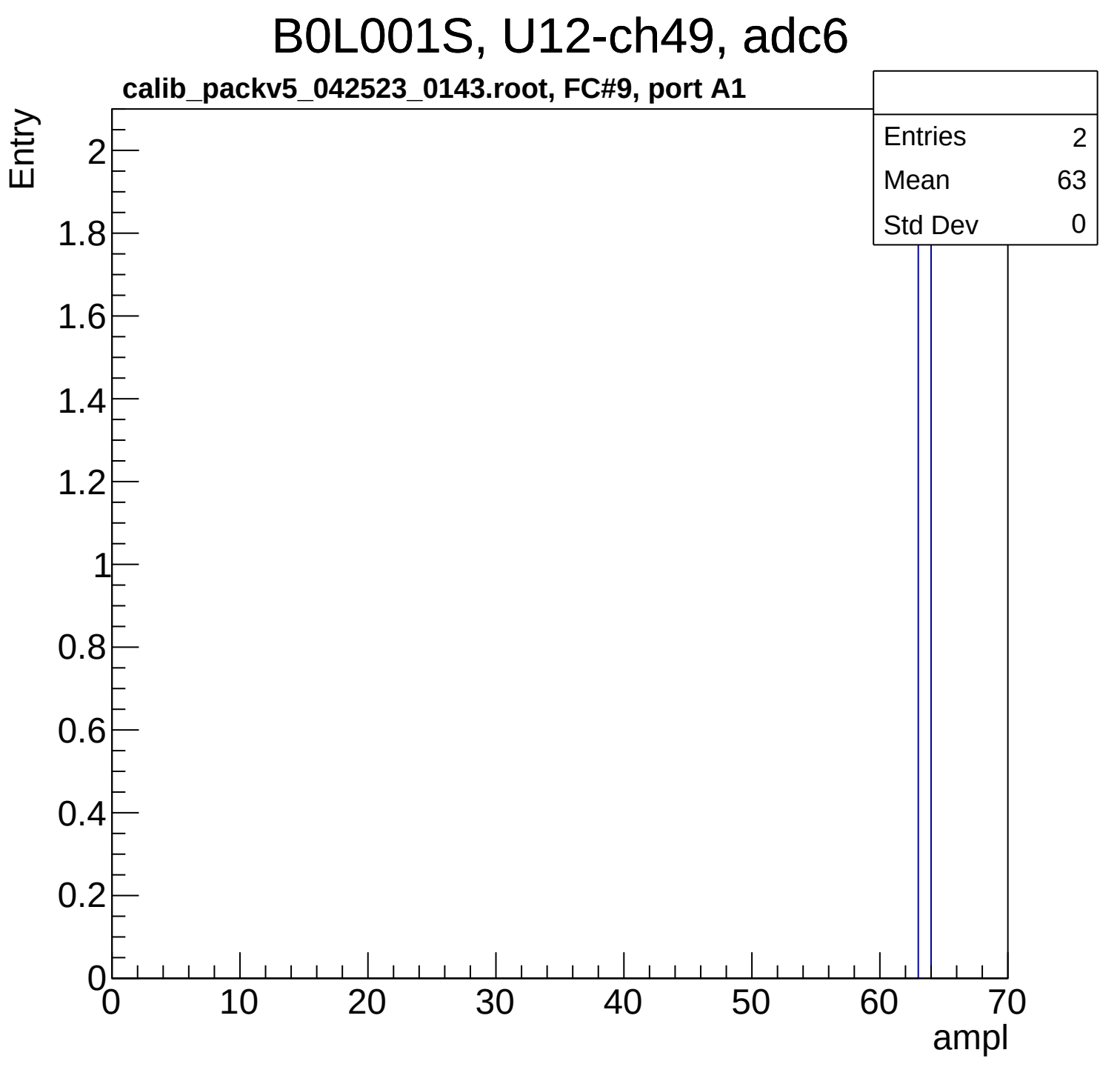
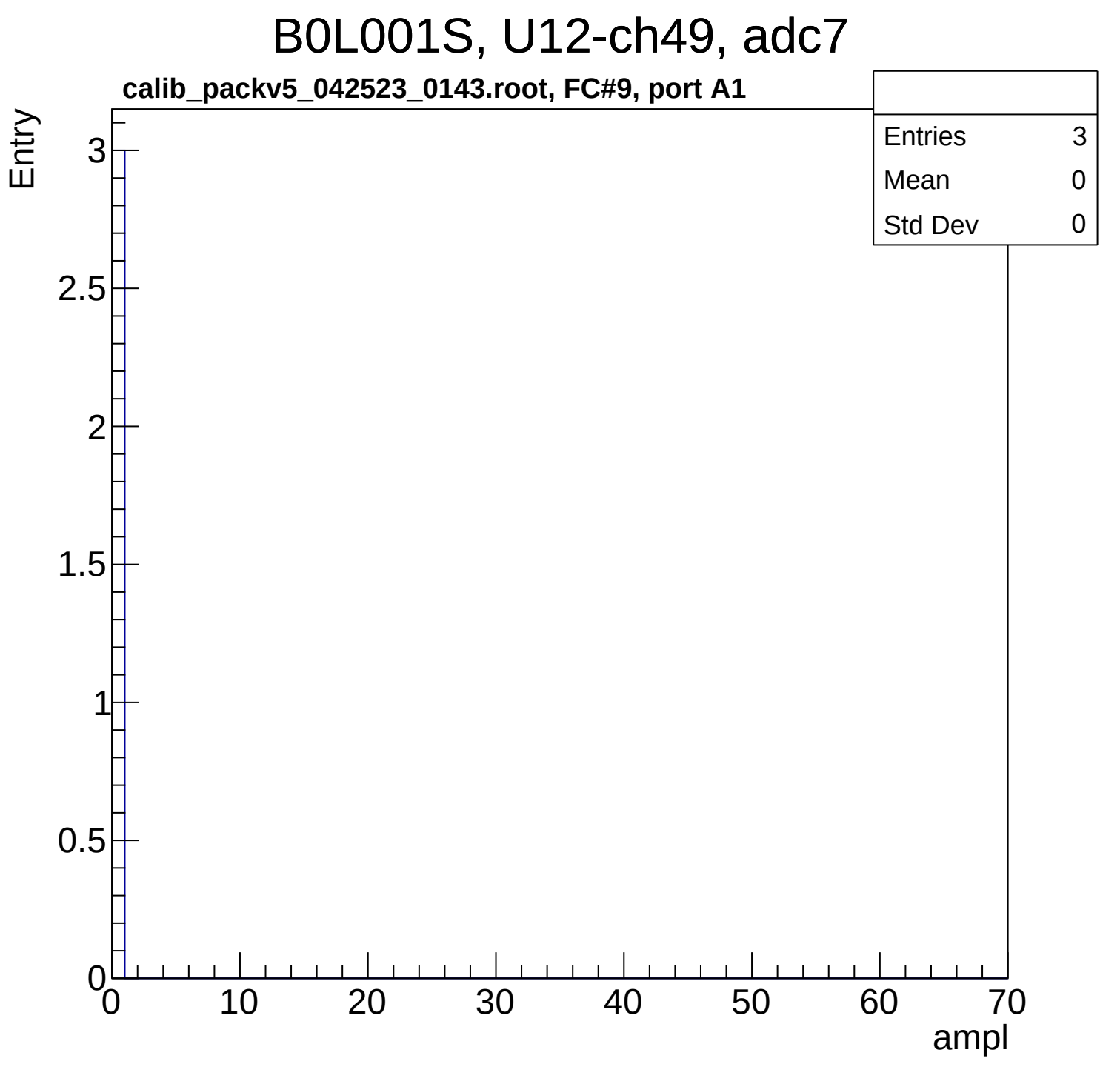
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch49, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 28
Mean 60.46
Std Dev 2.129
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch49, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L001S, U12-ch49, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 3
Mean 0
Std Dev 0
Entry
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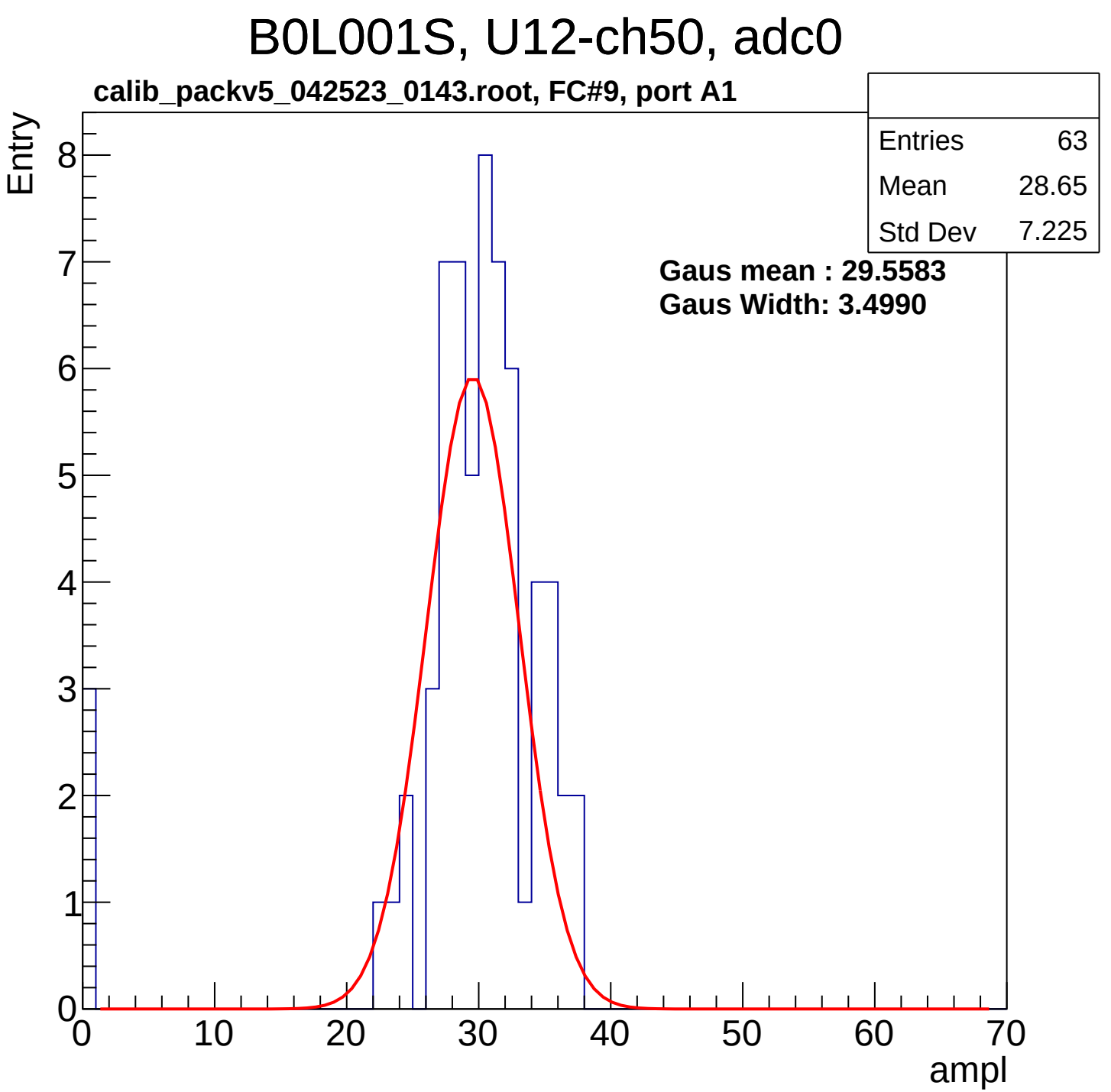
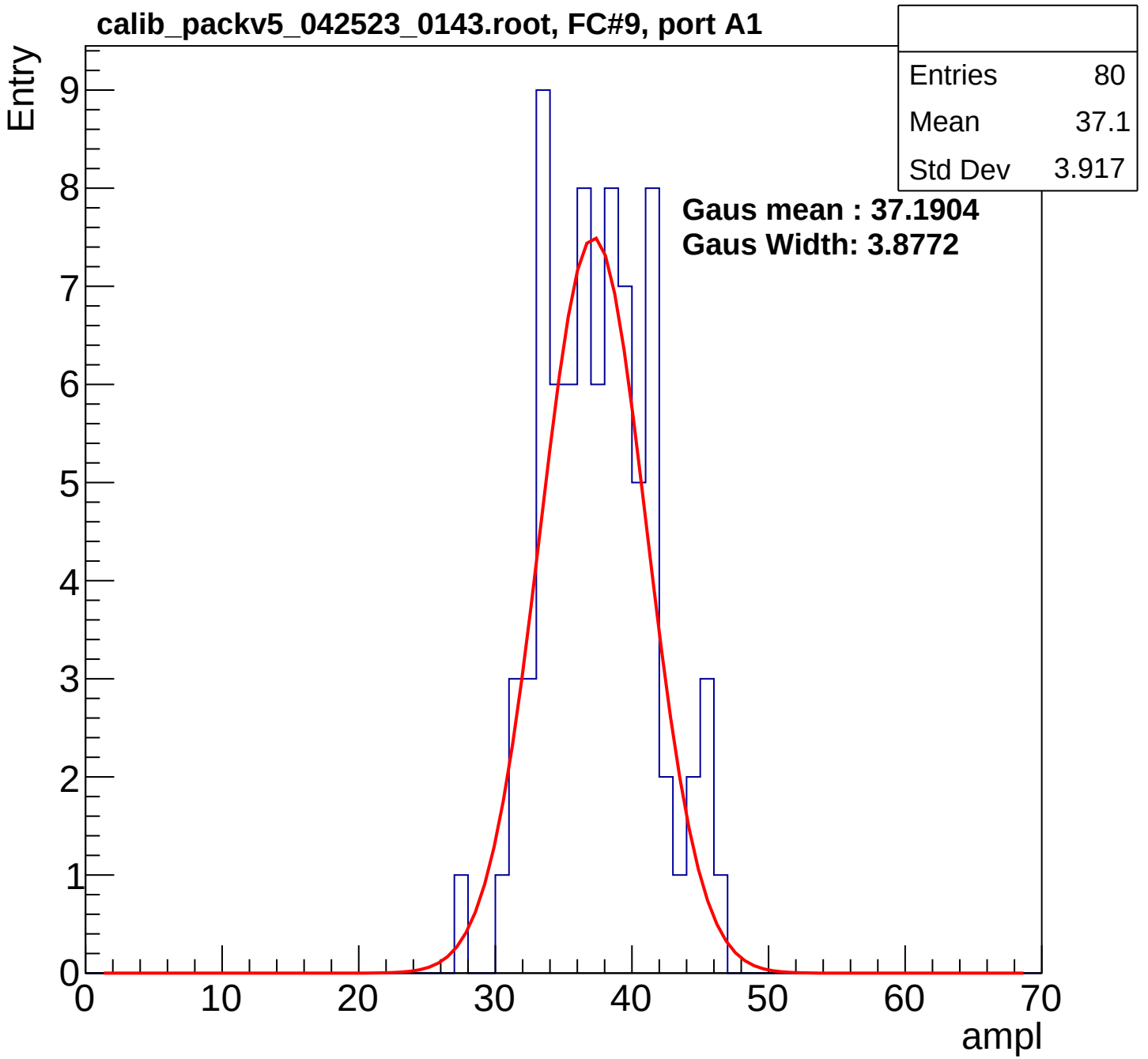
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch50, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 63
Mean 28.65
Std Dev 7.225
Gaus mean : 29.5583
Gaus Width: 3.4990
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch50, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 80
Mean 37.1
Std Dev 3.917
Gaus mean : 37.1904
Gaus Width: 3.8772
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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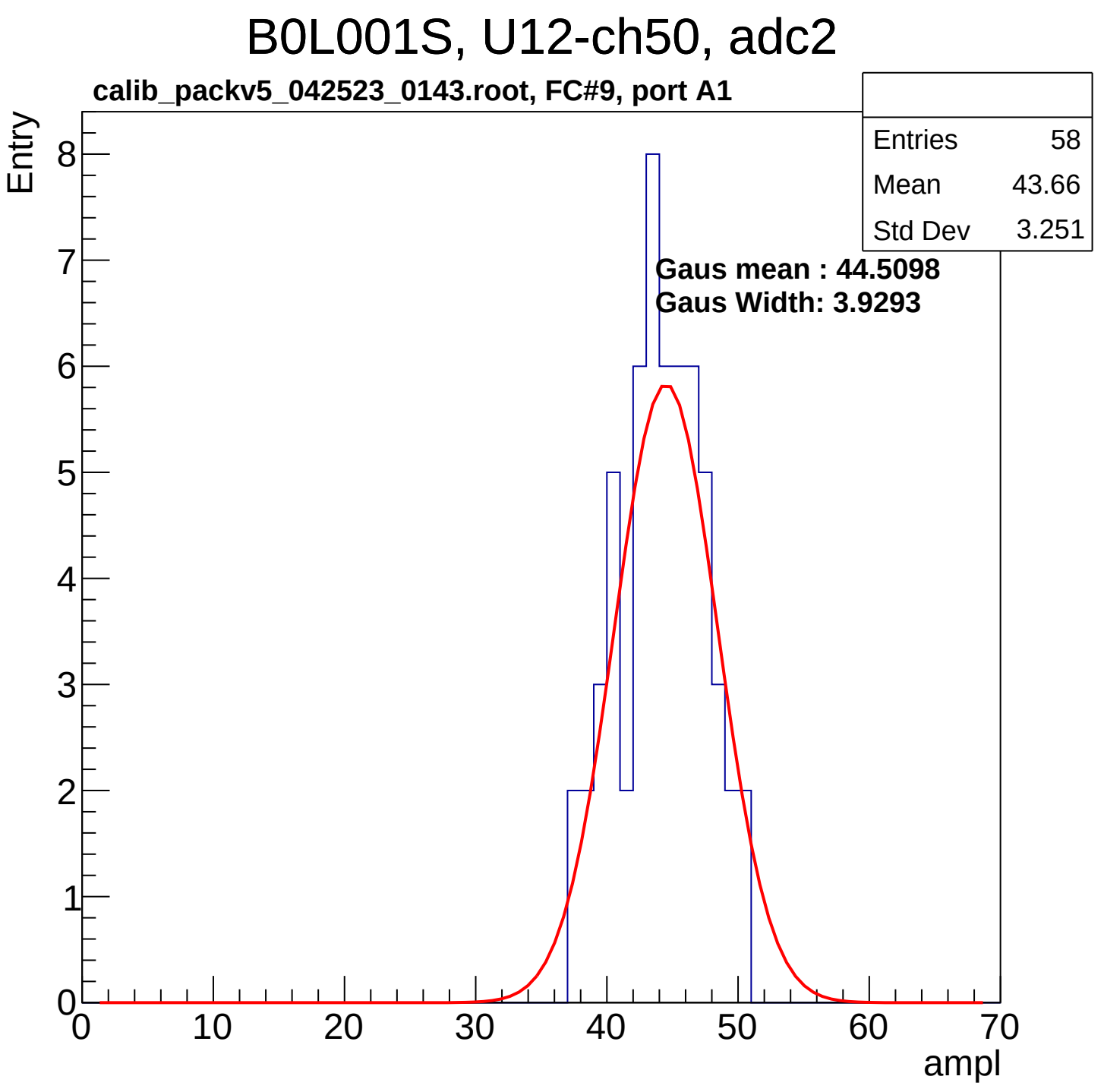
B0L001S, U12-ch50, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 58
Mean 43.66
Std Dev 3.251
Gaus mean : 44.5098
Gaus Width: 3.9293
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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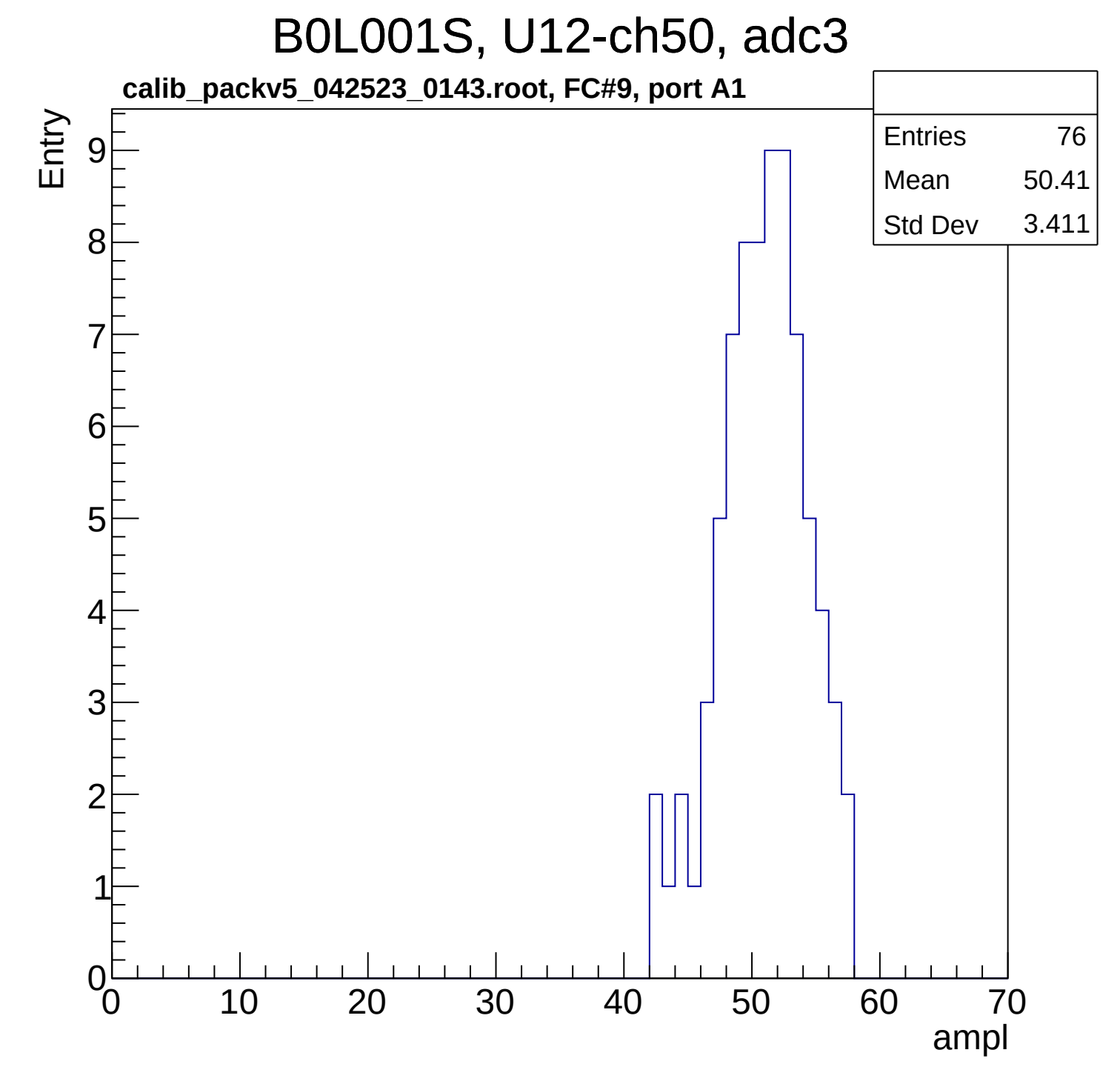
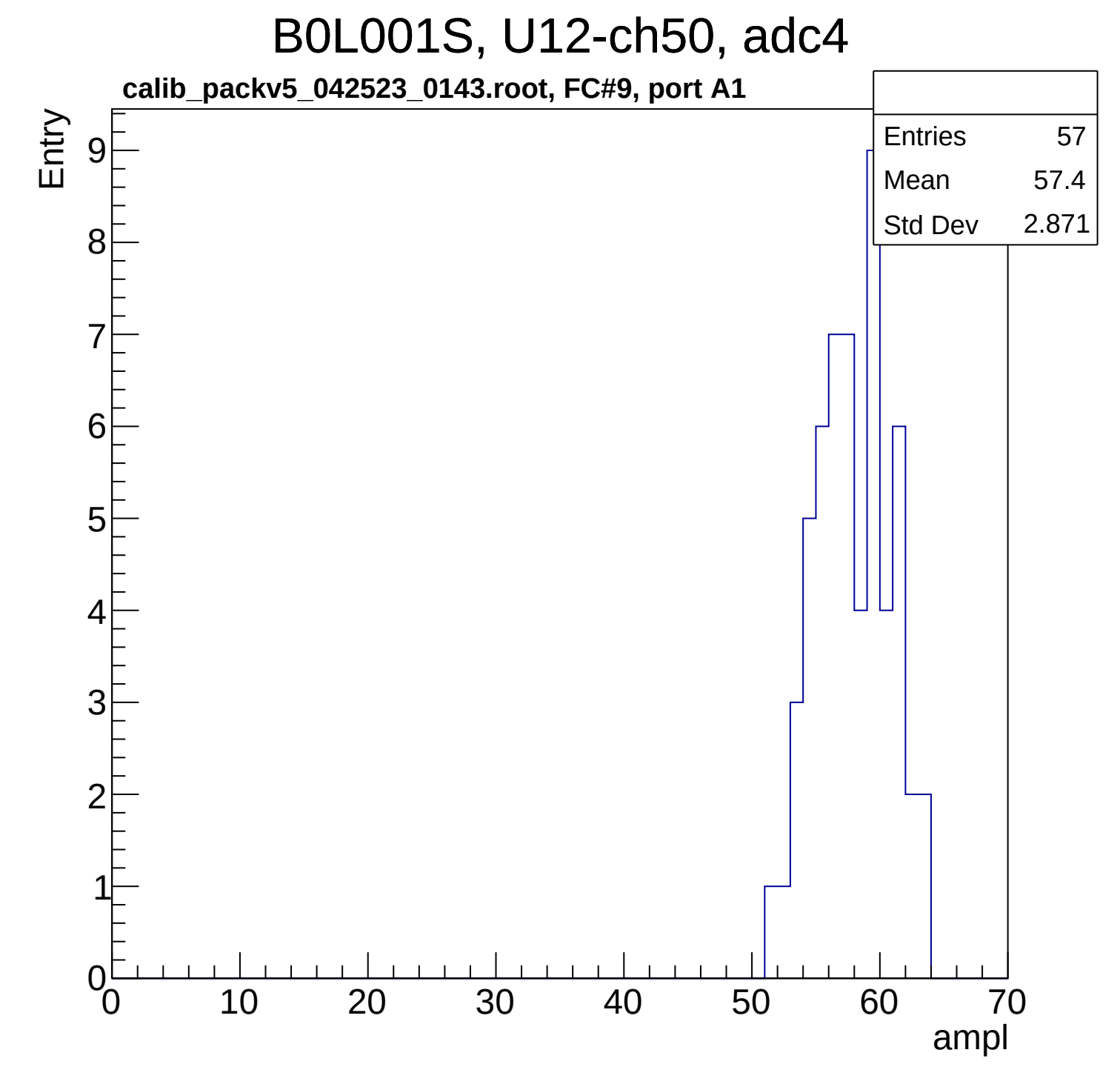
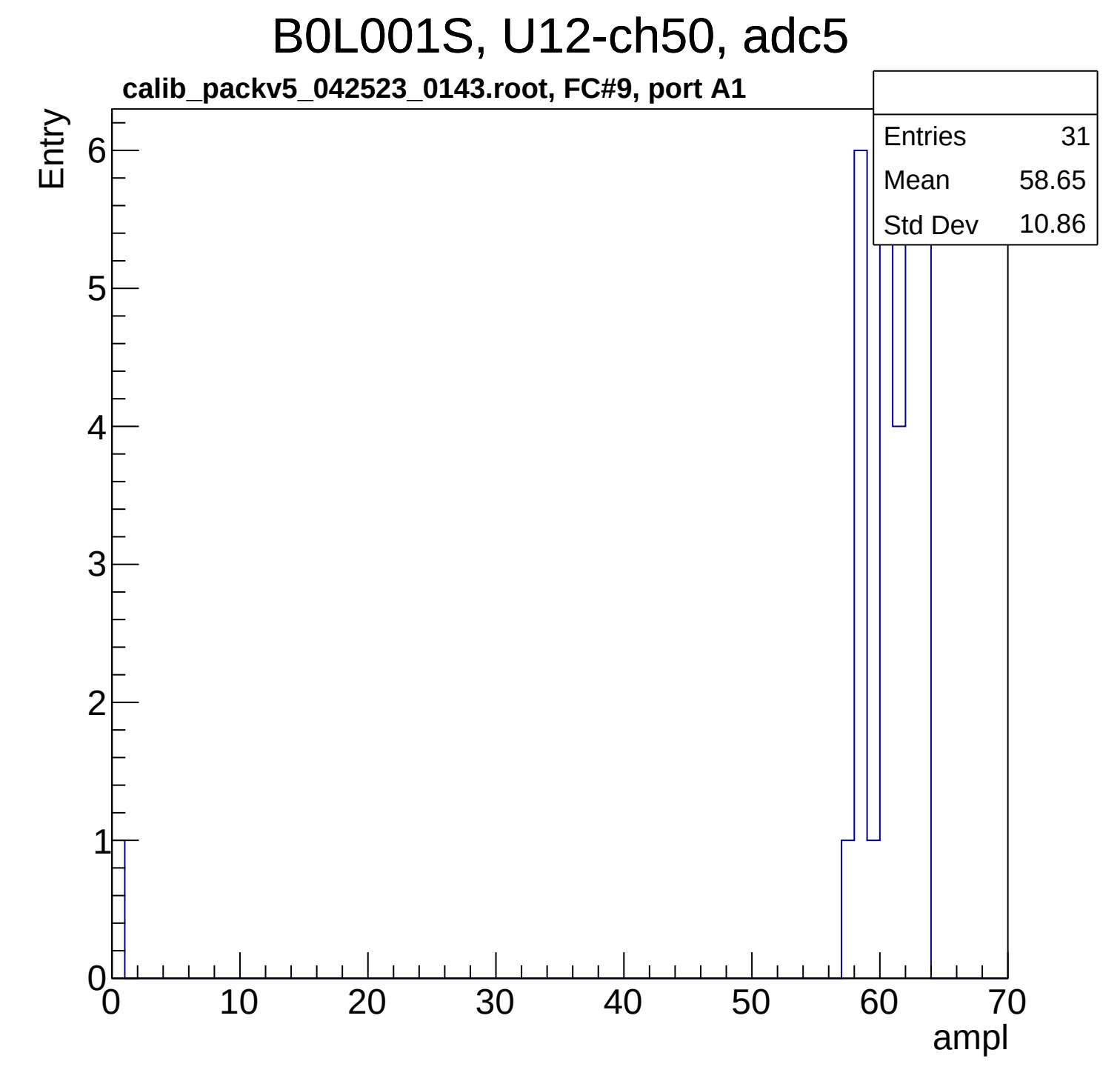
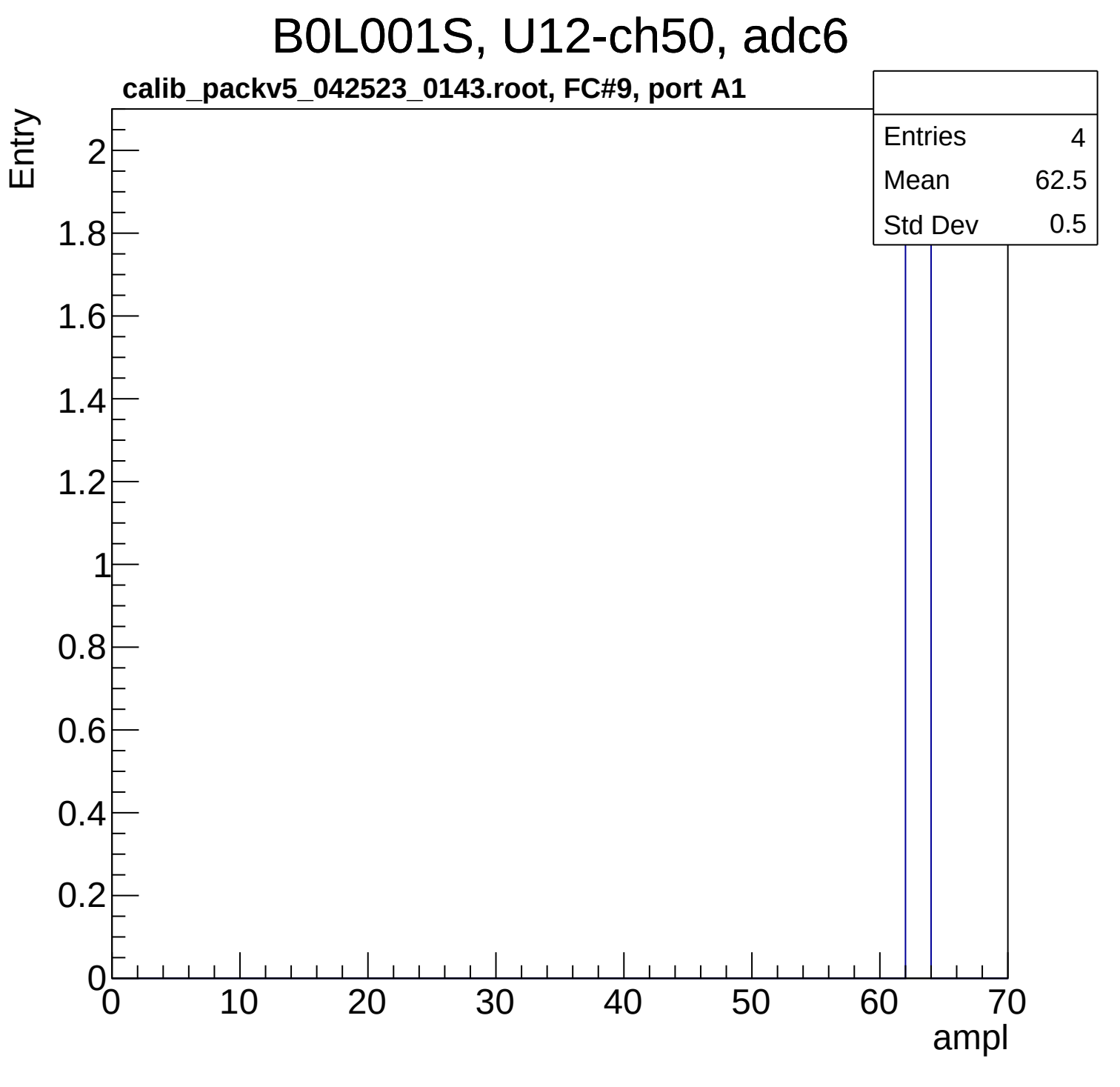
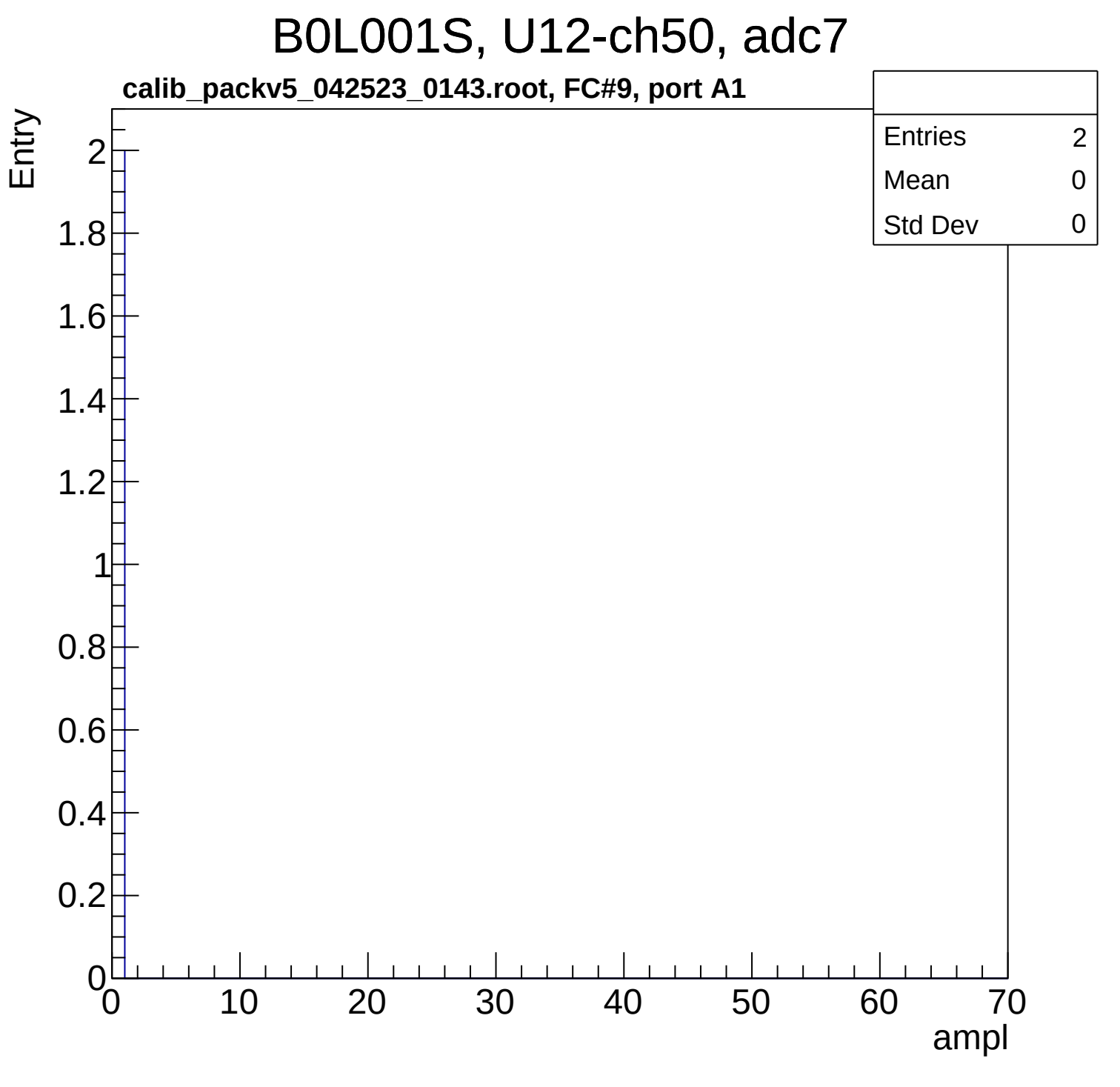
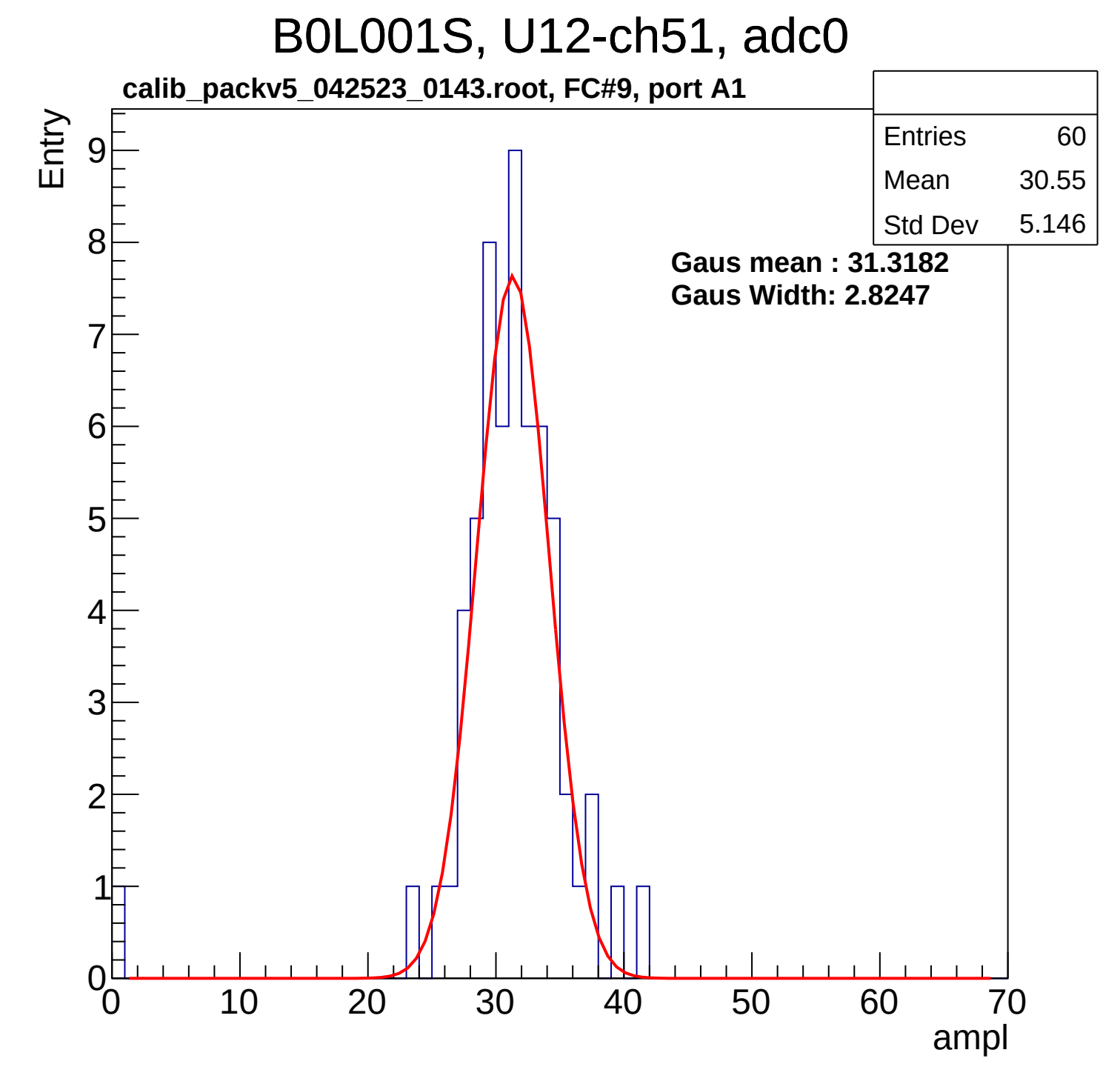

B0L001S, U12-ch50, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 76
Mean 50.41
Std Dev 3.411
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

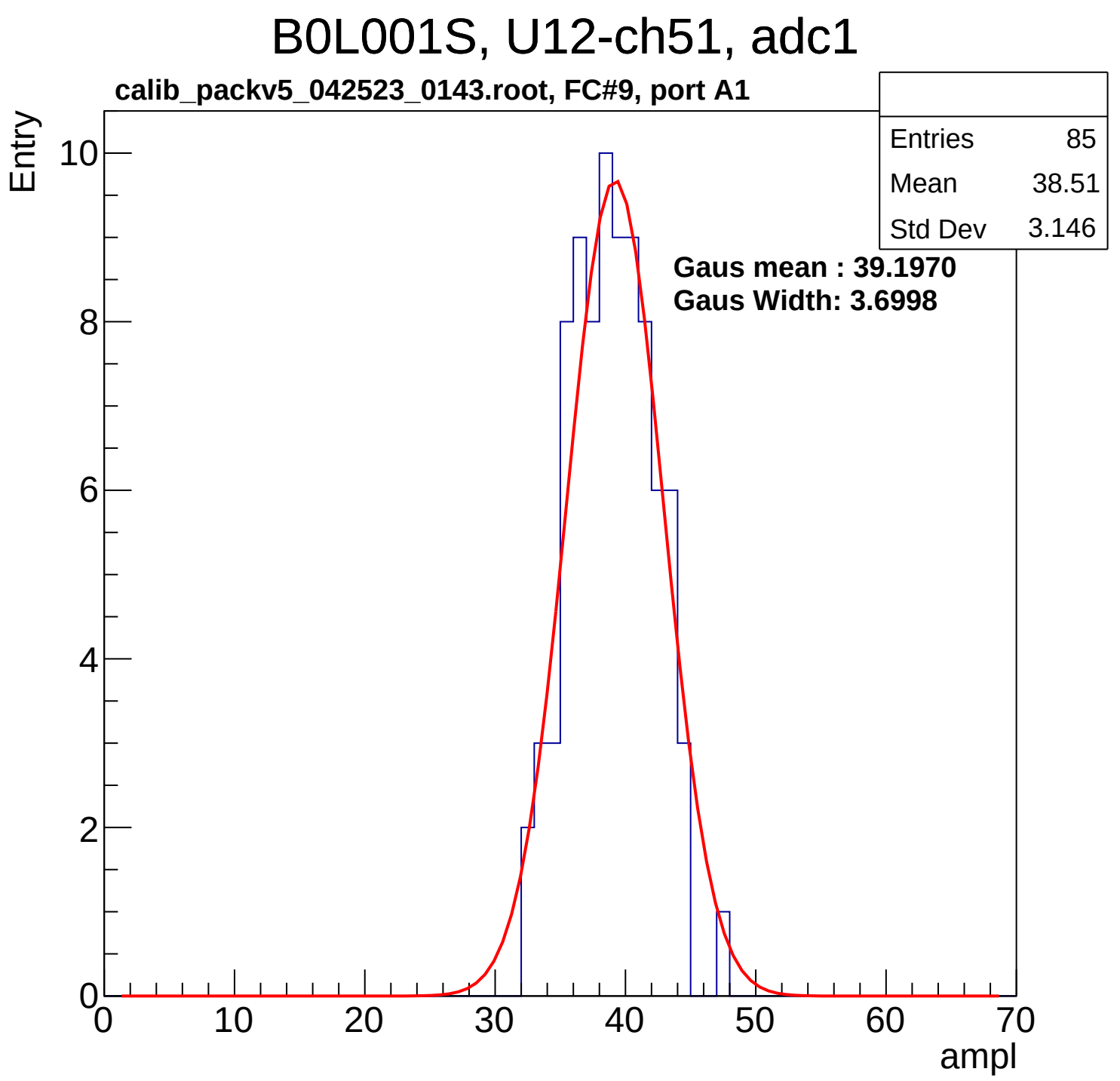

B0L001S, U12-ch50, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 57
Mean 57.4
Std Dev 2.871
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

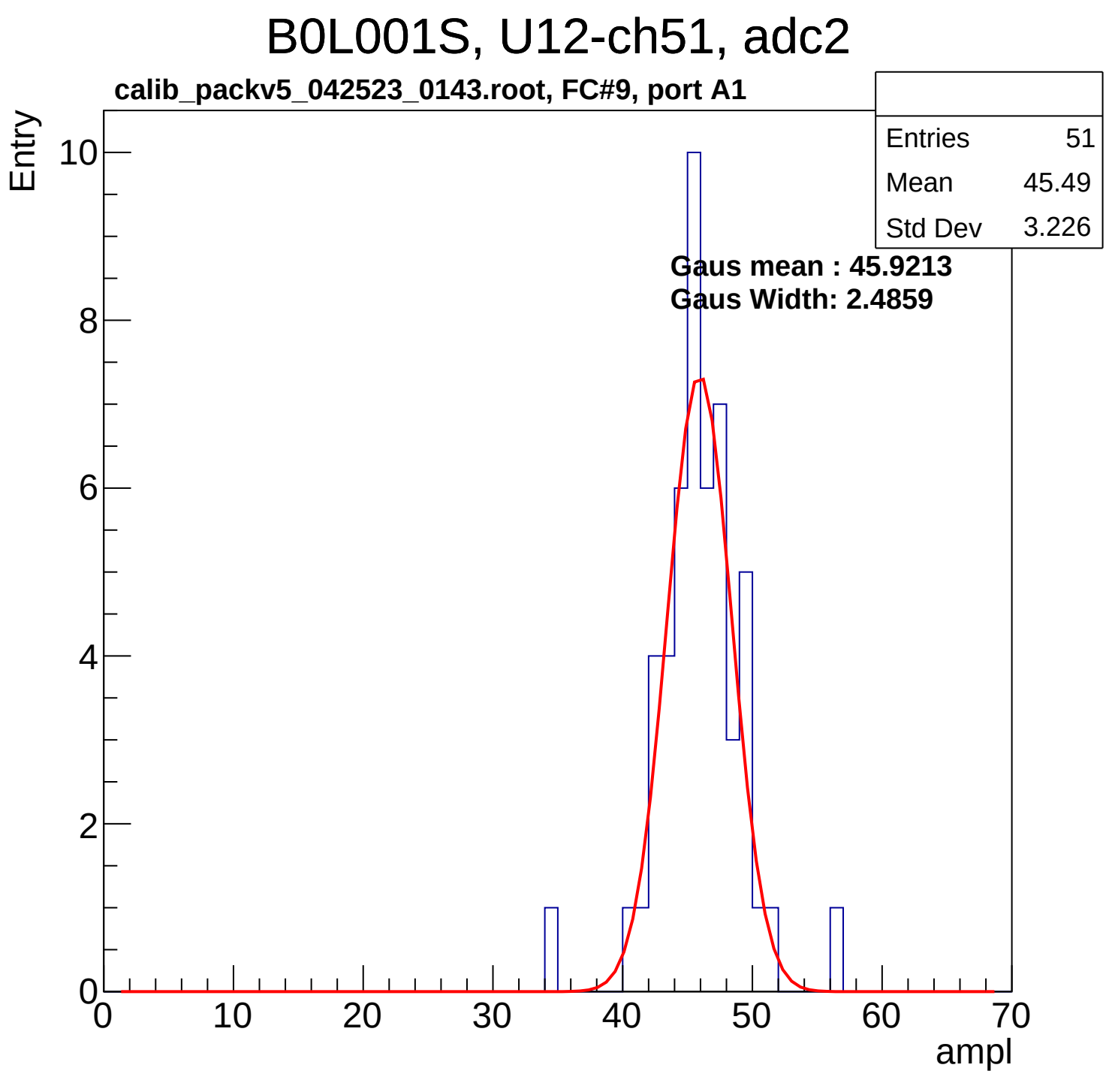

B0L001S, U12-ch50, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 31
Mean 58.65
Std Dev 10.86
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

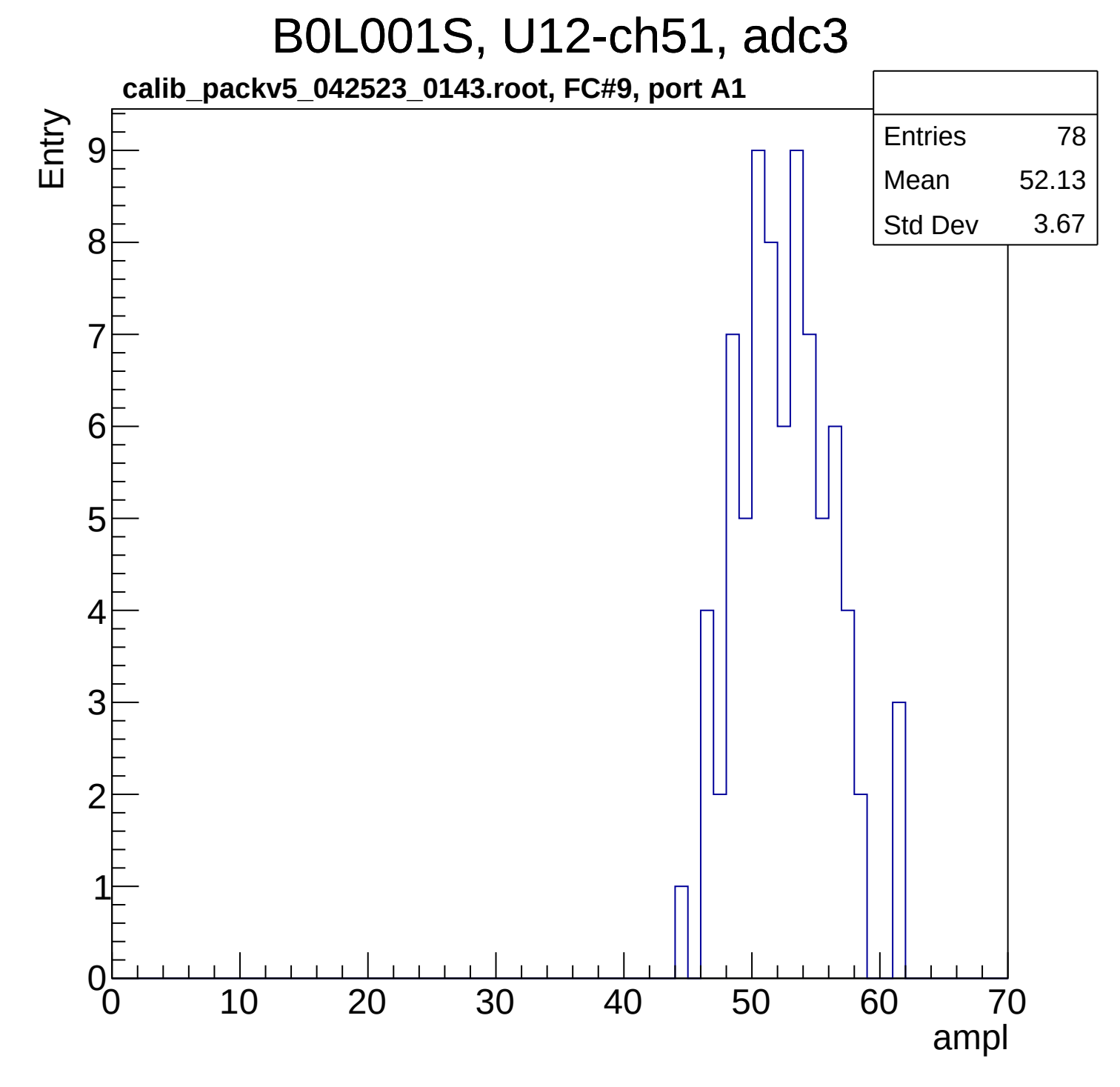

B0L001S, U12-ch50, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 4
Mean 62.5
Std Dev 0.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L001S, U12-ch50, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch51, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 60
Mean 30.55
Std Dev 5.146
Gaus mean : 31.3182
Gaus Width: 2.8247
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch51, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 85
Mean 38.51
Std Dev 3.146
Gaus mean : 39.1970
Gaus Width: 3.6998
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch51, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 51
Mean 45.49
Std Dev 3.226
Gaus mean : 45.9213
Gaus Width: 2.4859
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch51, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 78
Mean 52.13
Std Dev 3.67
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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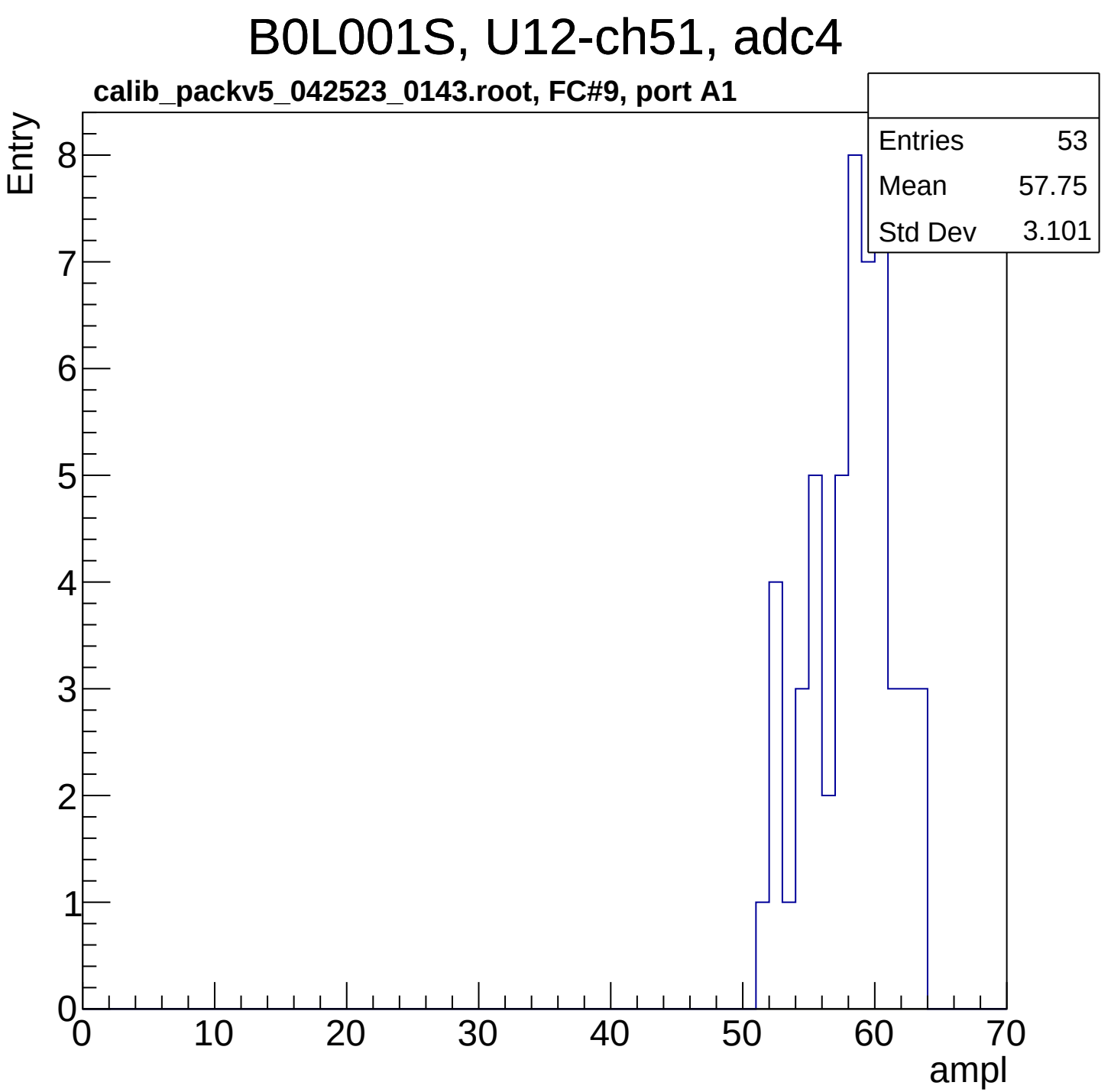
B0L001S, U12-ch51, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 53
Mean 57.75
Std Dev 3.101
Entry
ampl
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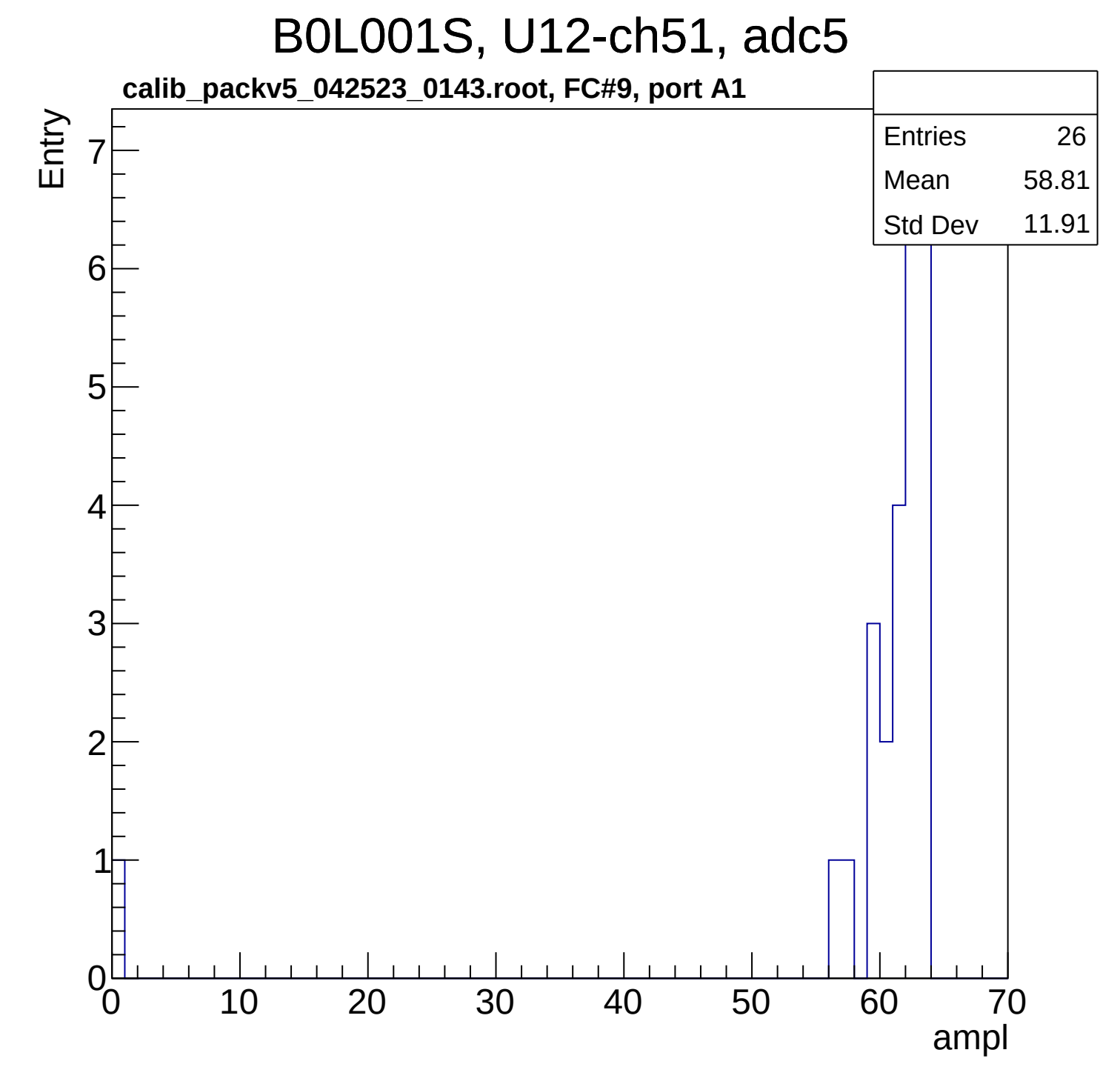
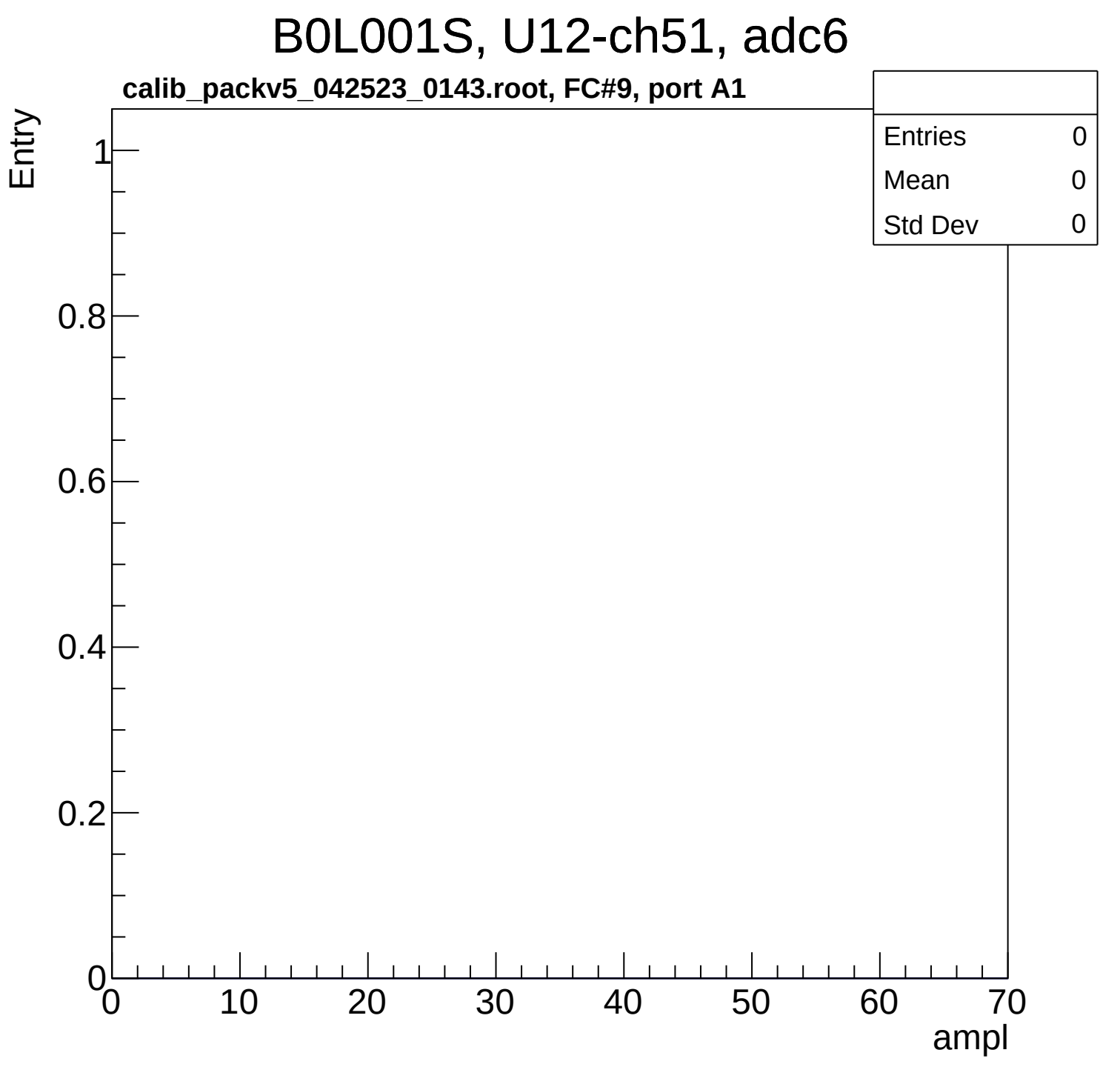
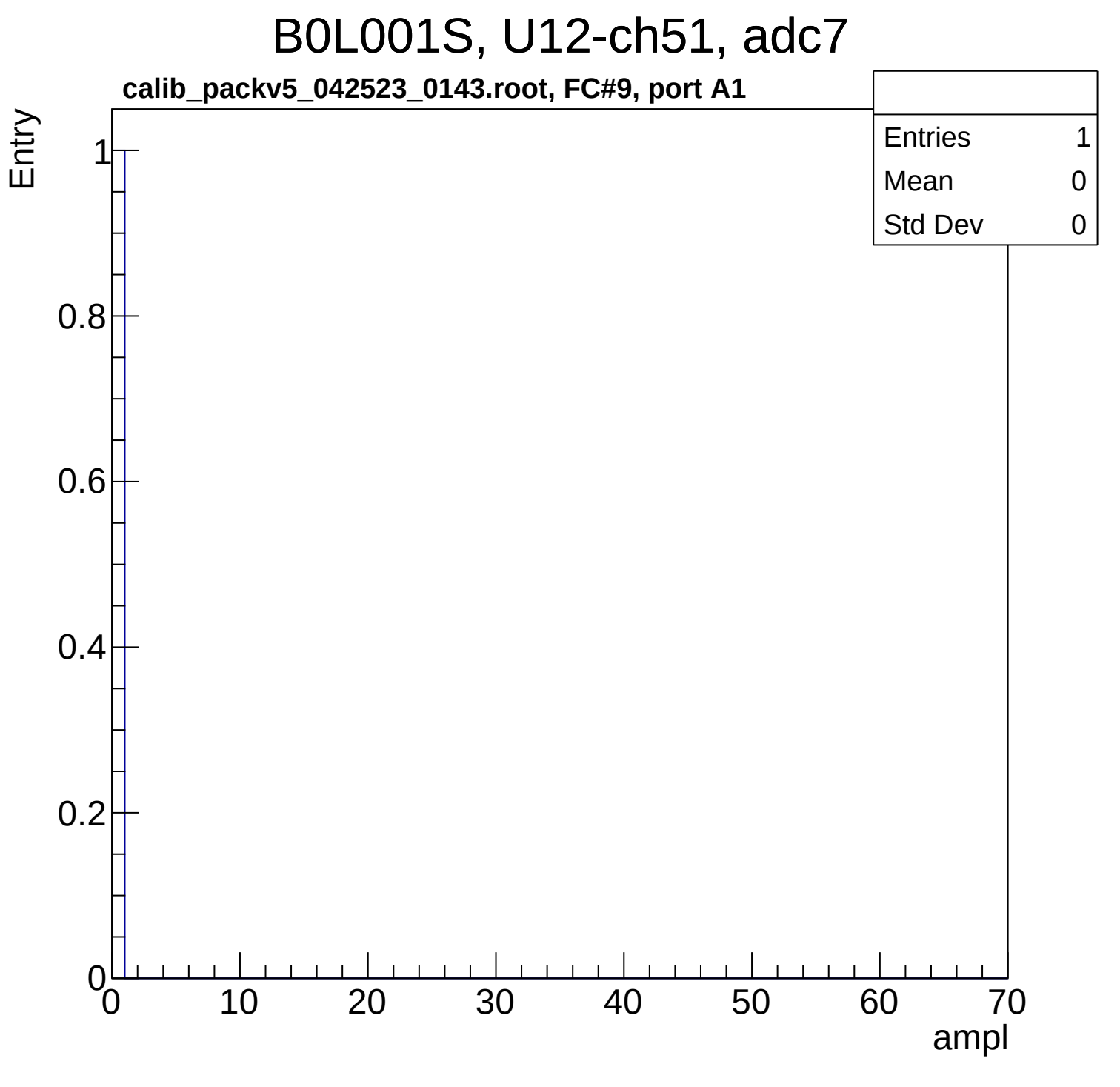
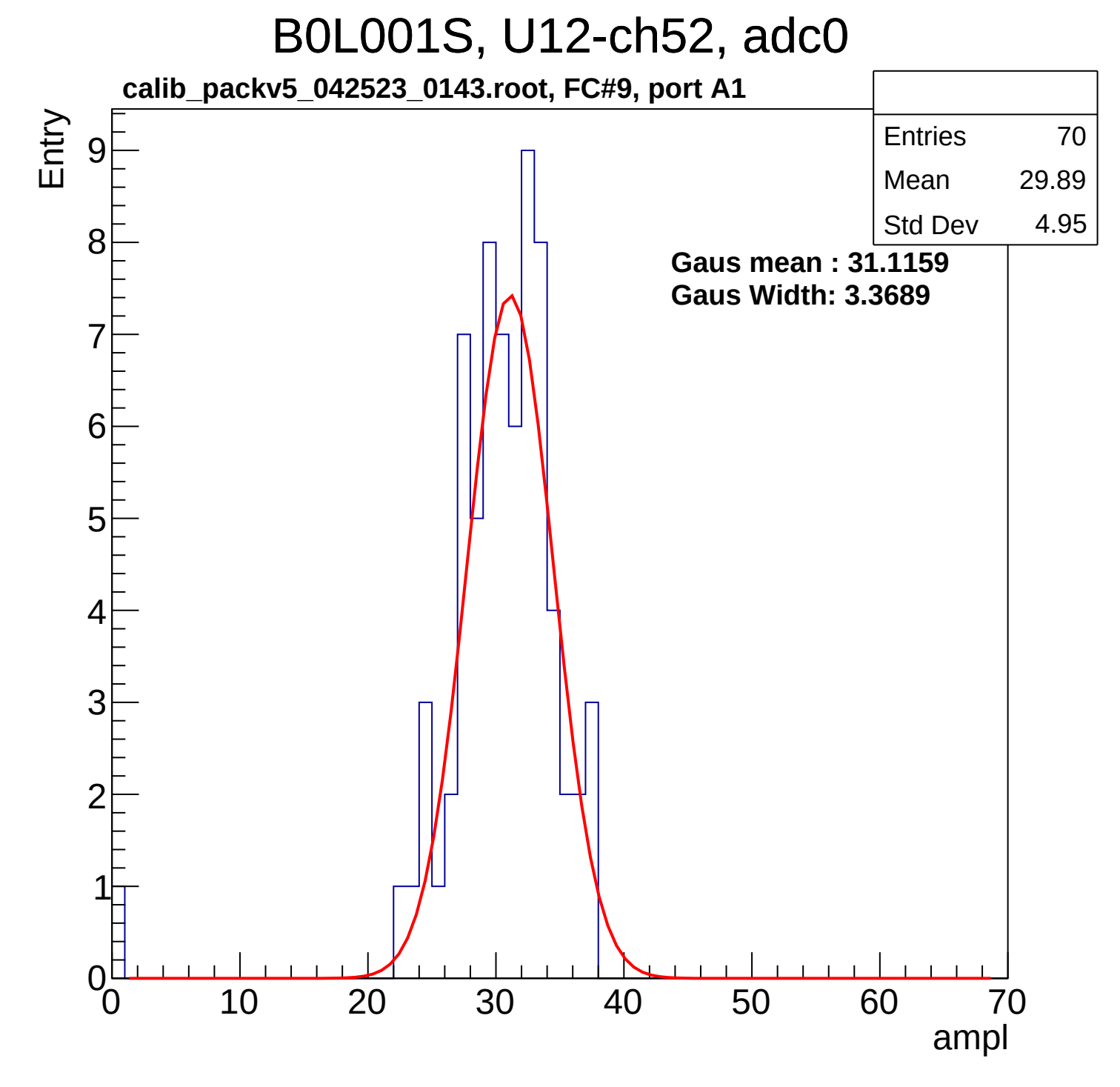
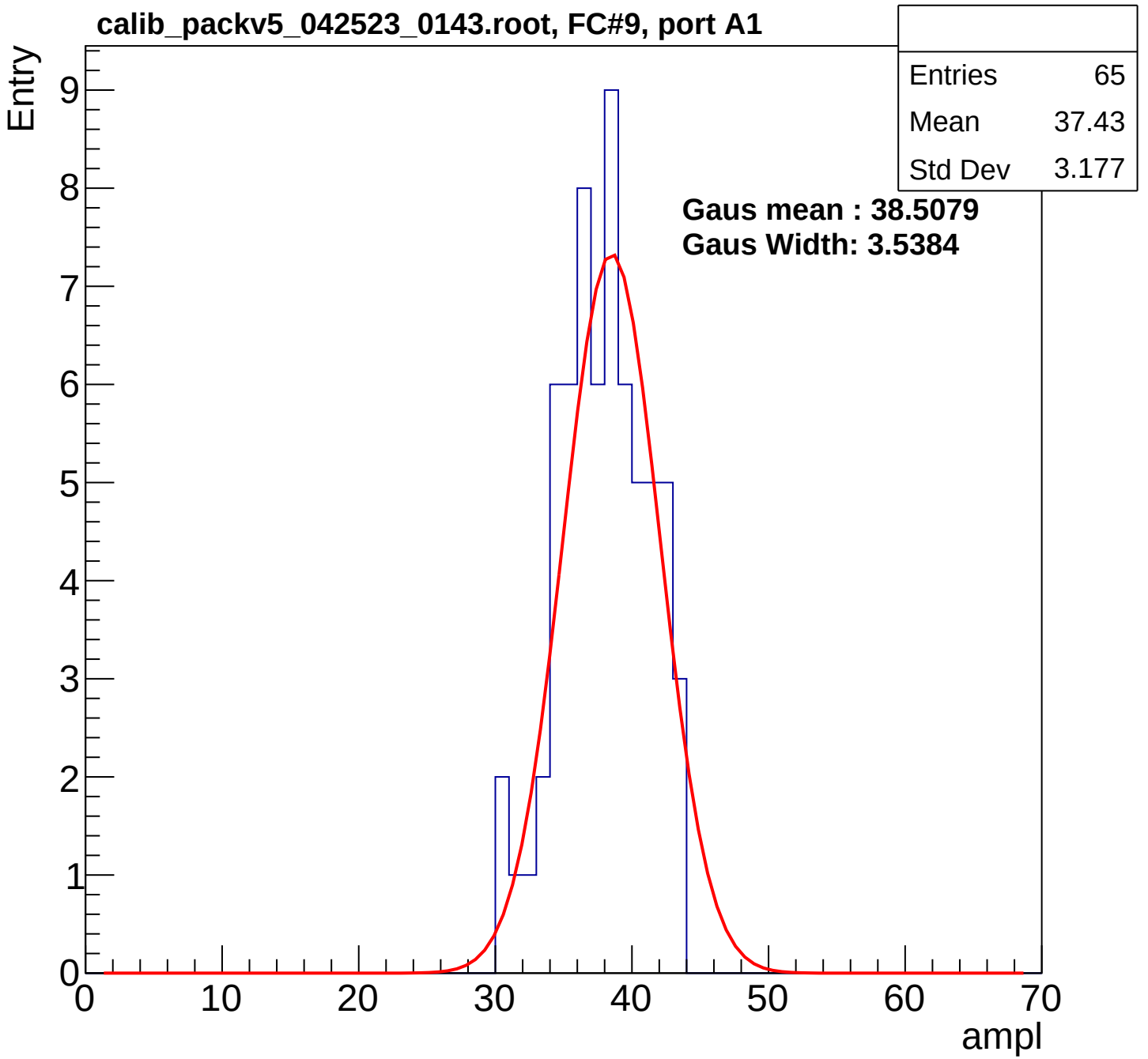
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

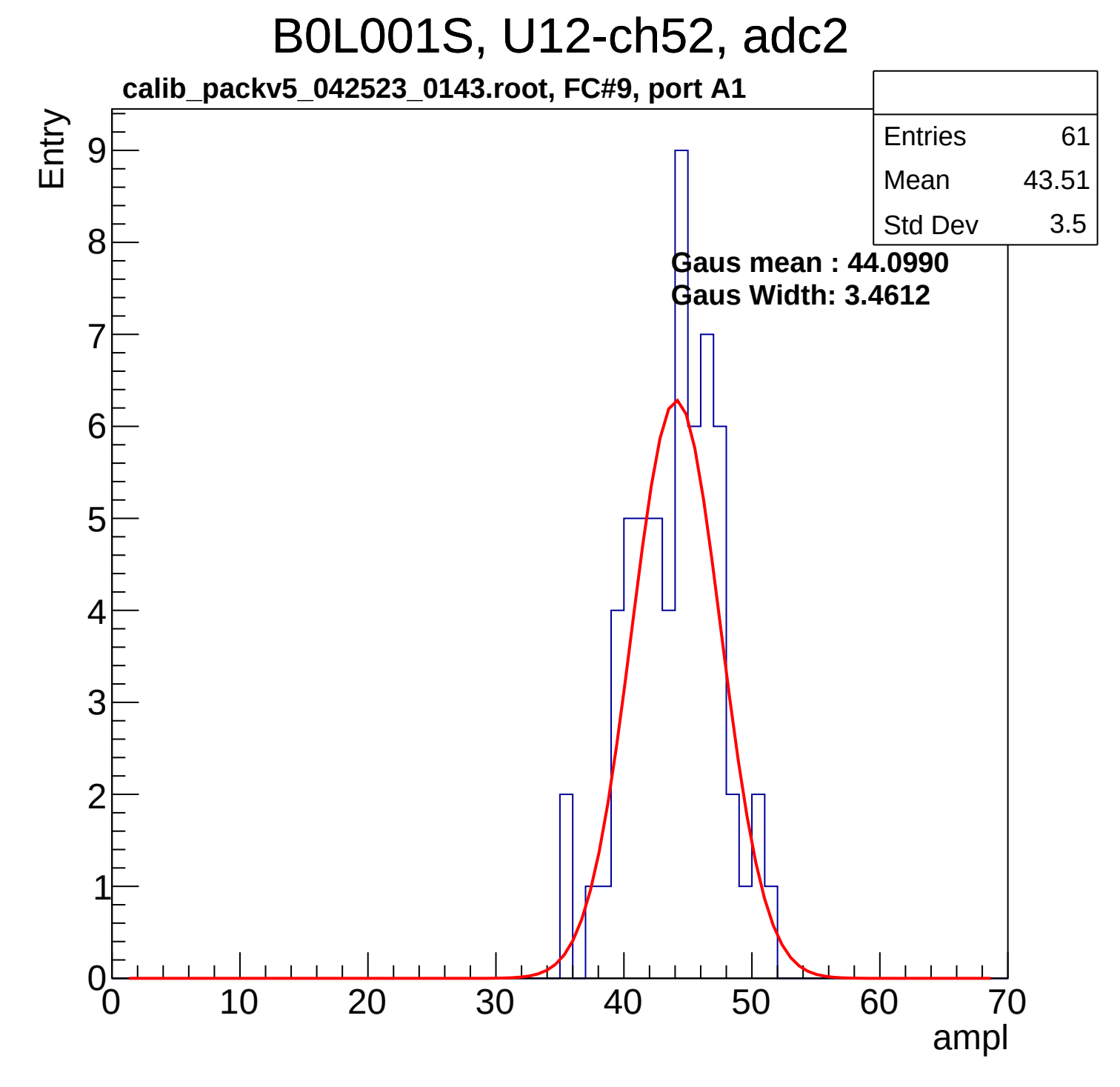

B0L001S, U12-ch51, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 26
Mean 58.81
Std Dev 11.91
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

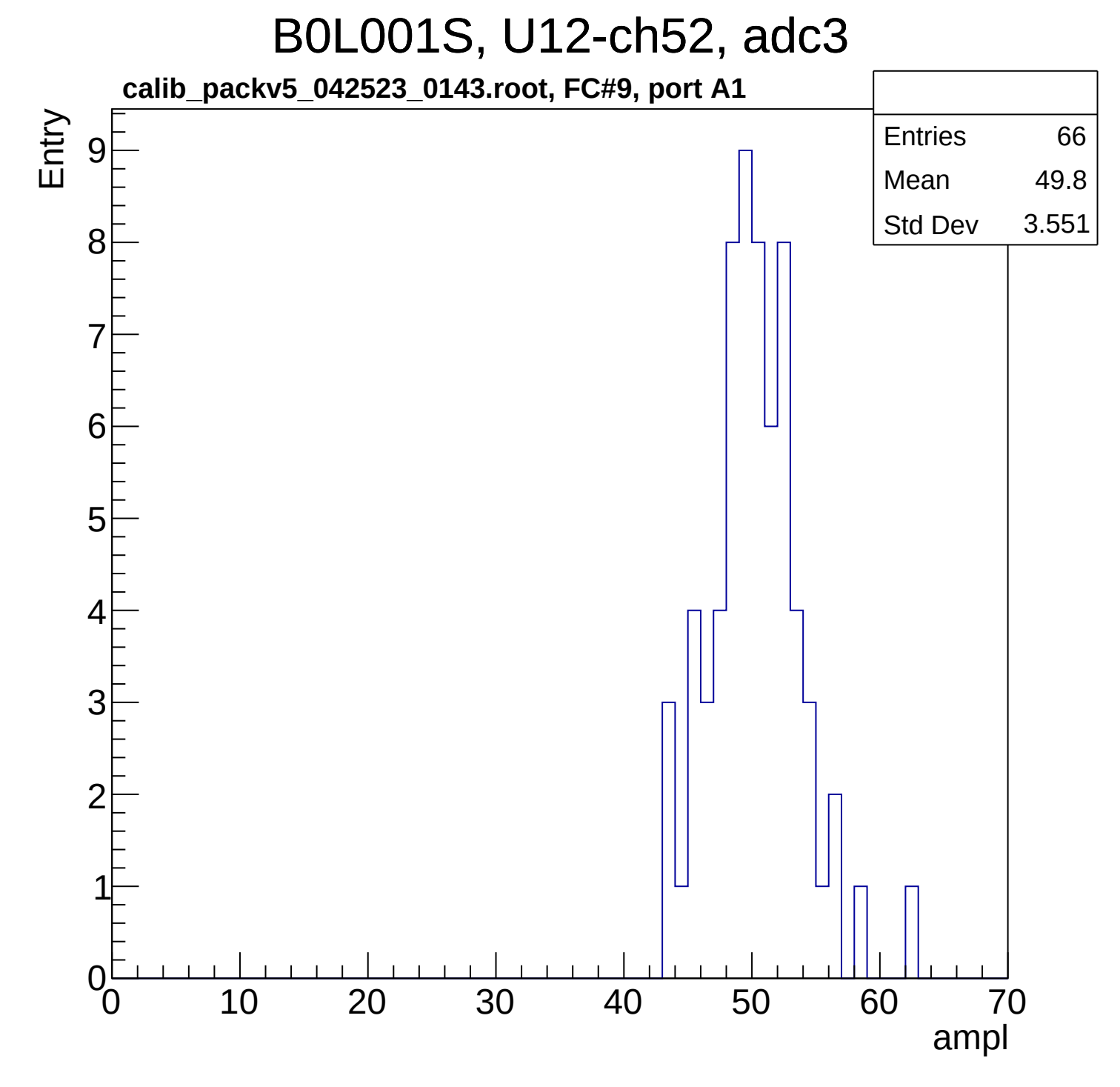

B0L001S, U12-ch51, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch51, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch52, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 70
Mean 29.89
Std Dev 4.95
Gaus mean : 31.1159
Gaus Width: 3.3689
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch52, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 65
Mean 37.43
Std Dev 3.177
Gaus mean : 38.5079
Gaus Width: 3.5384
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch52, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 61
Mean 43.51
Std Dev 3.5
Gaus mean : 44.0990
Gaus Width: 3.4612
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch52, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 66
Mean 49.8
Std Dev 3.551
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
50
60
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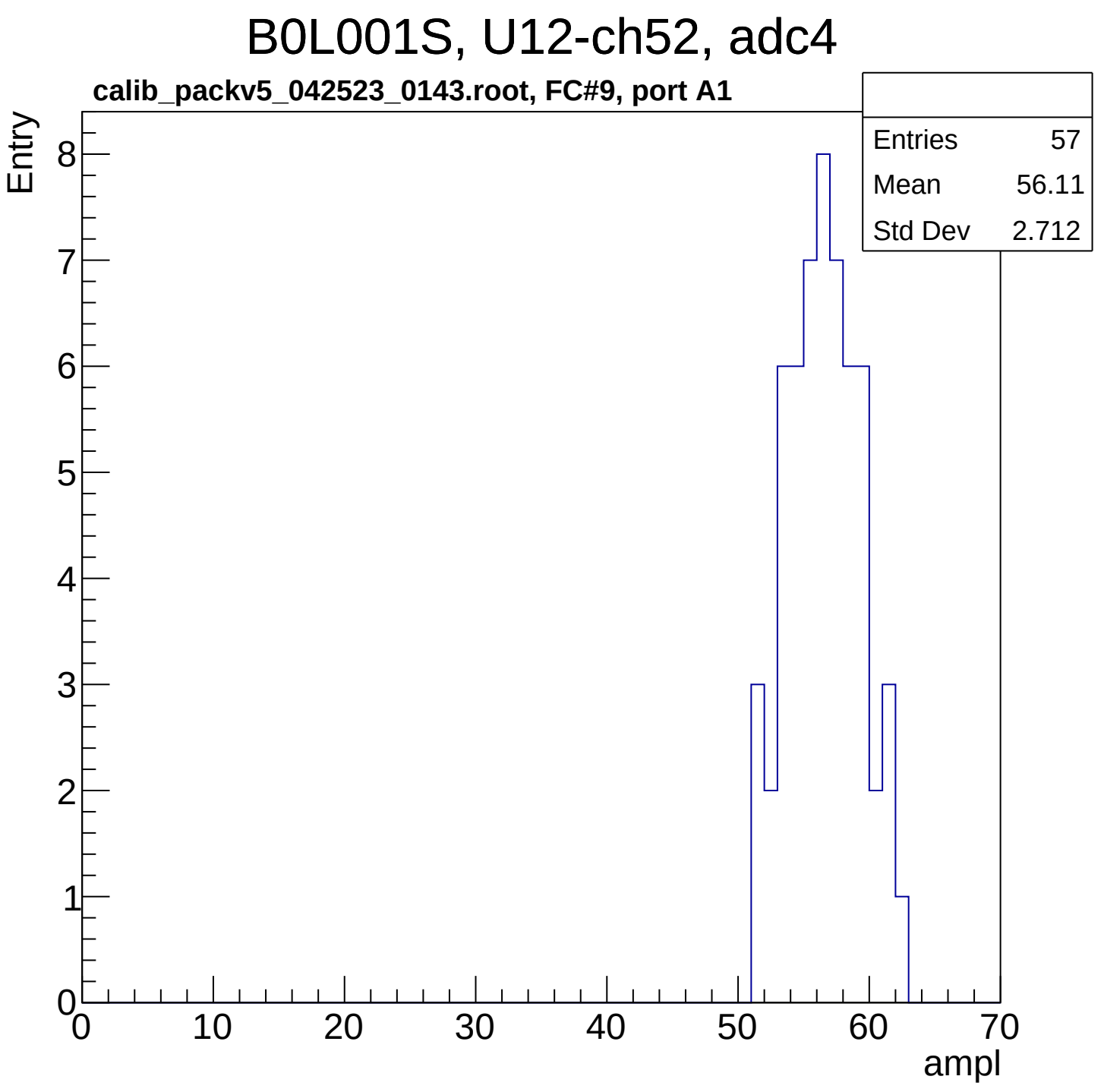
B0L001S, U12-ch52, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 57
Mean 56.11
Std Dev 2.712
Entry
ampl
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1
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3
4
5
6
7
8
0
10
20
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40
50
60
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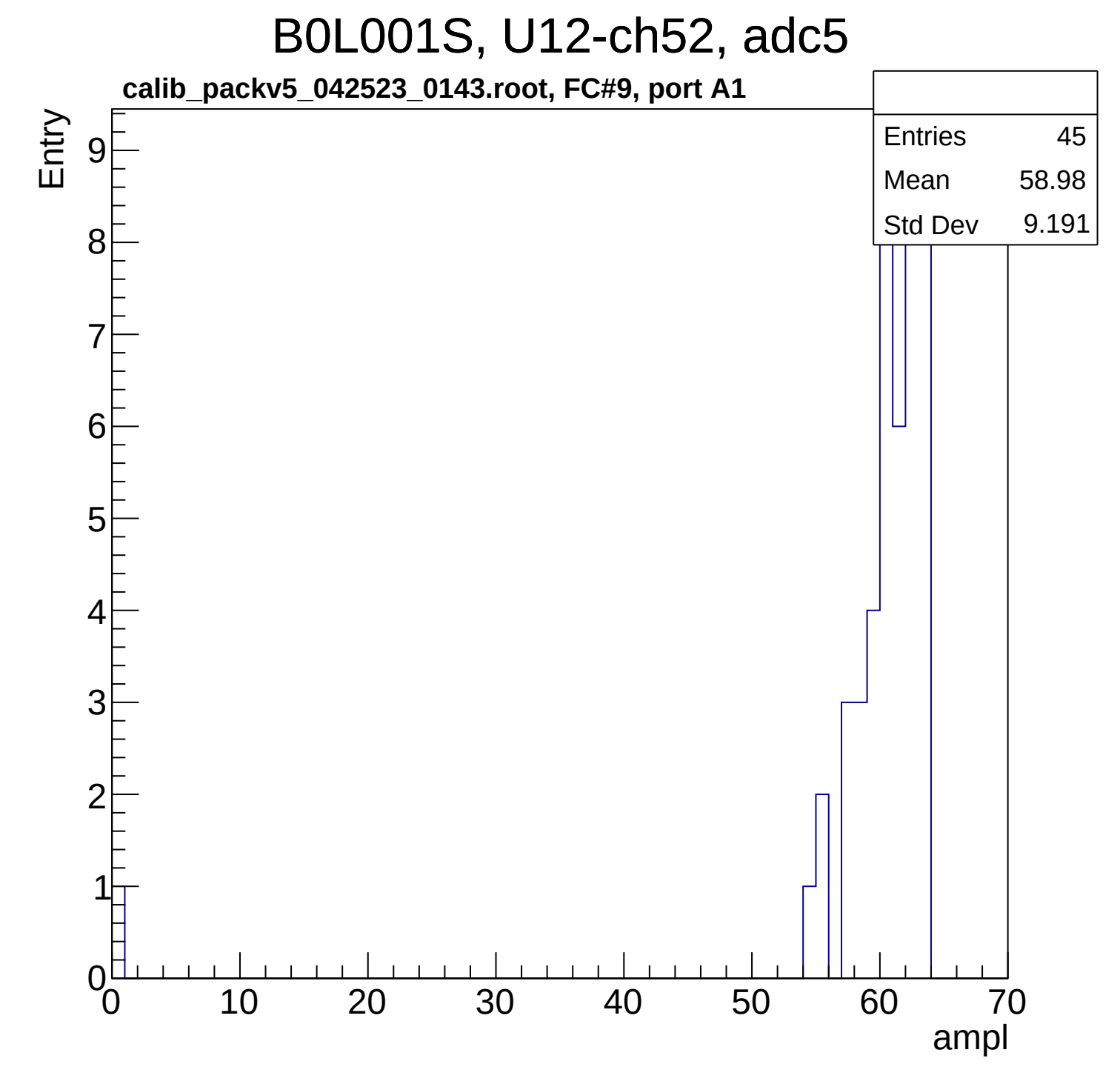
B0L001S, U12-ch52, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 45
Mean 58.98
Std Dev 9.191
Entry
ampl
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7
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0
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60
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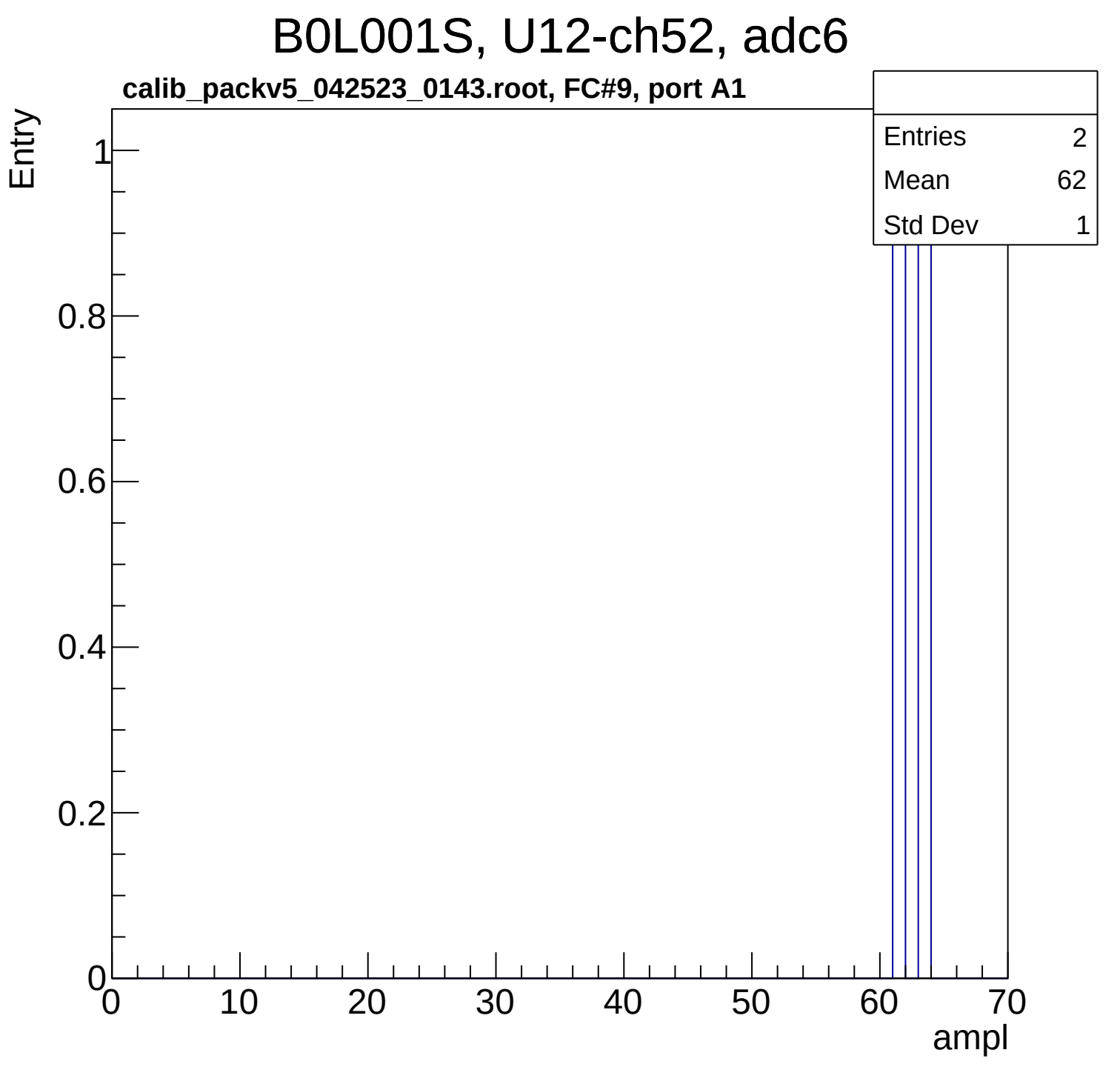
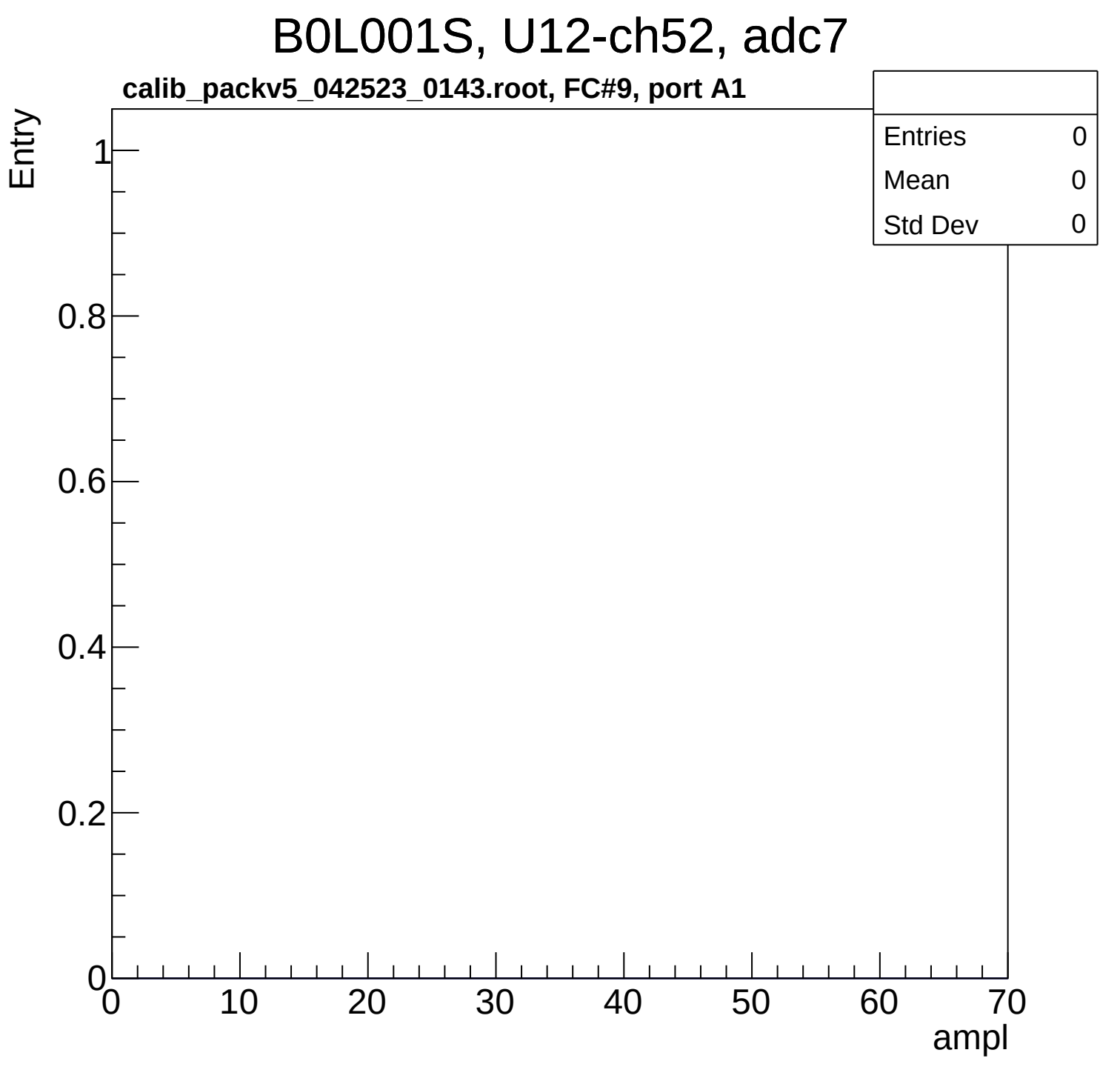

B0L001S, U12-ch52, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 62
Std Dev 1
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch52, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
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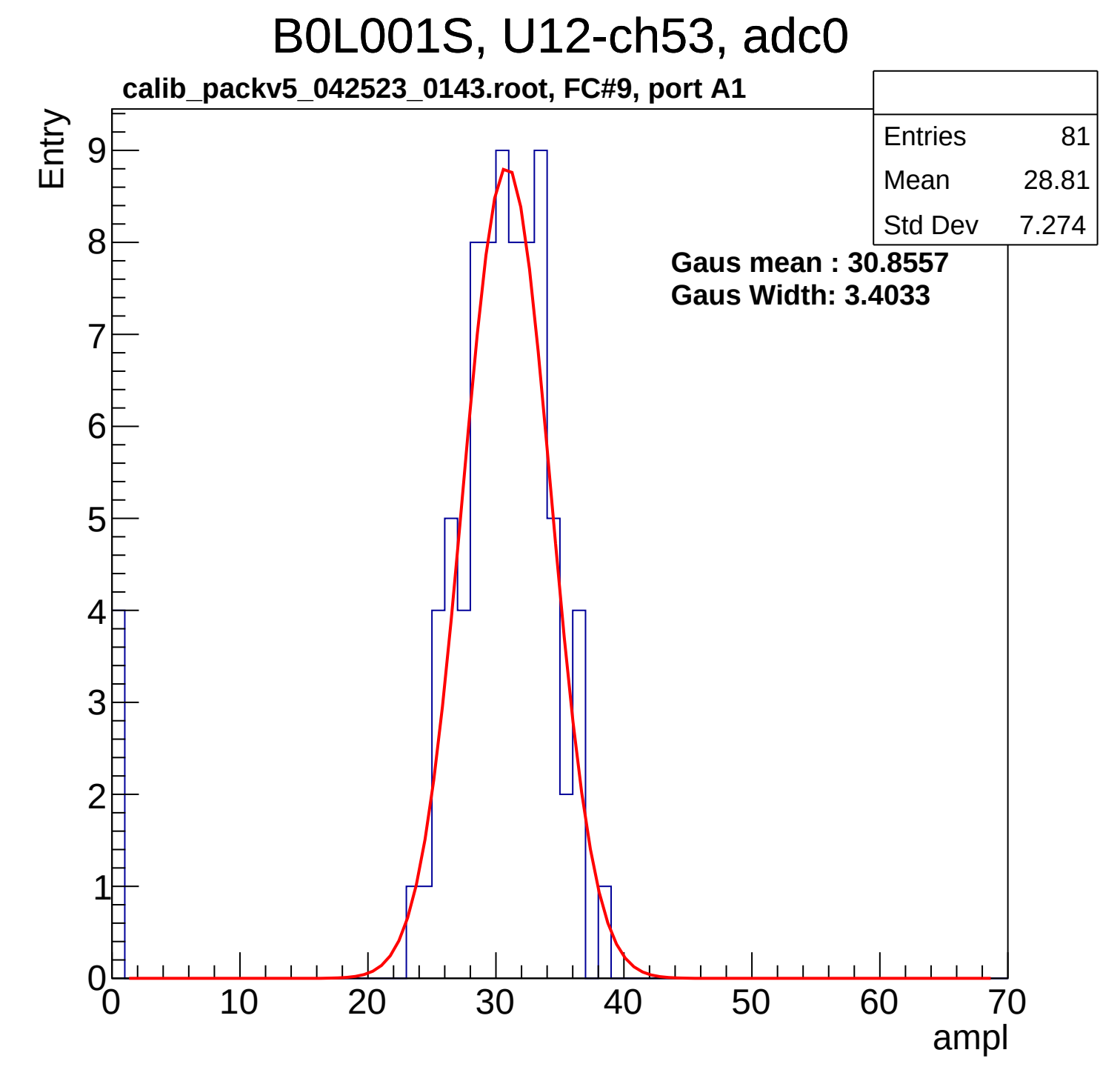
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch53, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 81
Mean 28.81
Std Dev 7.274
Gaus mean : 30.8557
Gaus Width: 3.4033
Entry
ampl
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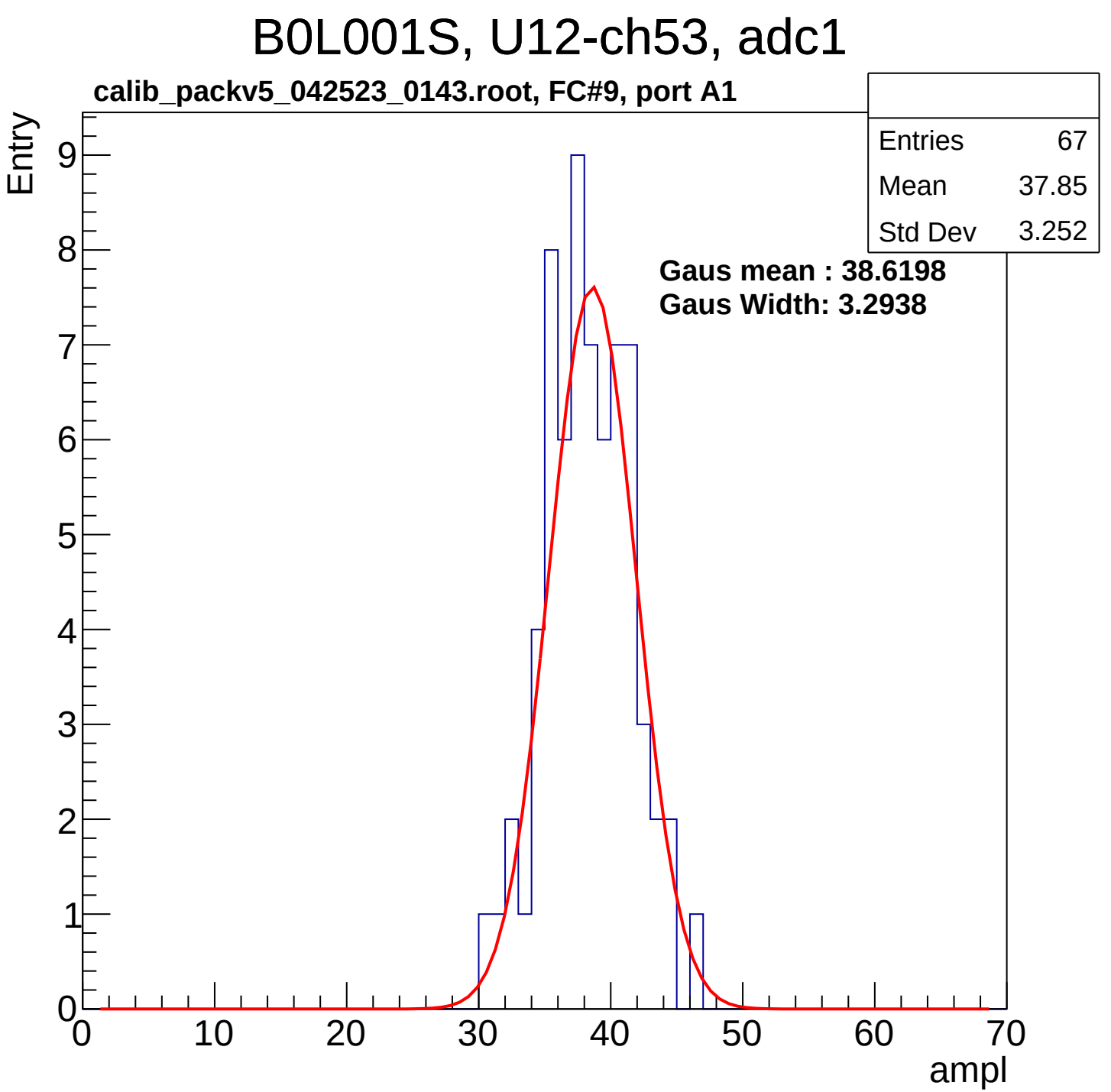
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch53, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 67
Mean 37.85
Std Dev 3.252
Gaus mean : 38.6198
Gaus Width: 3.2938
Entry
ampl
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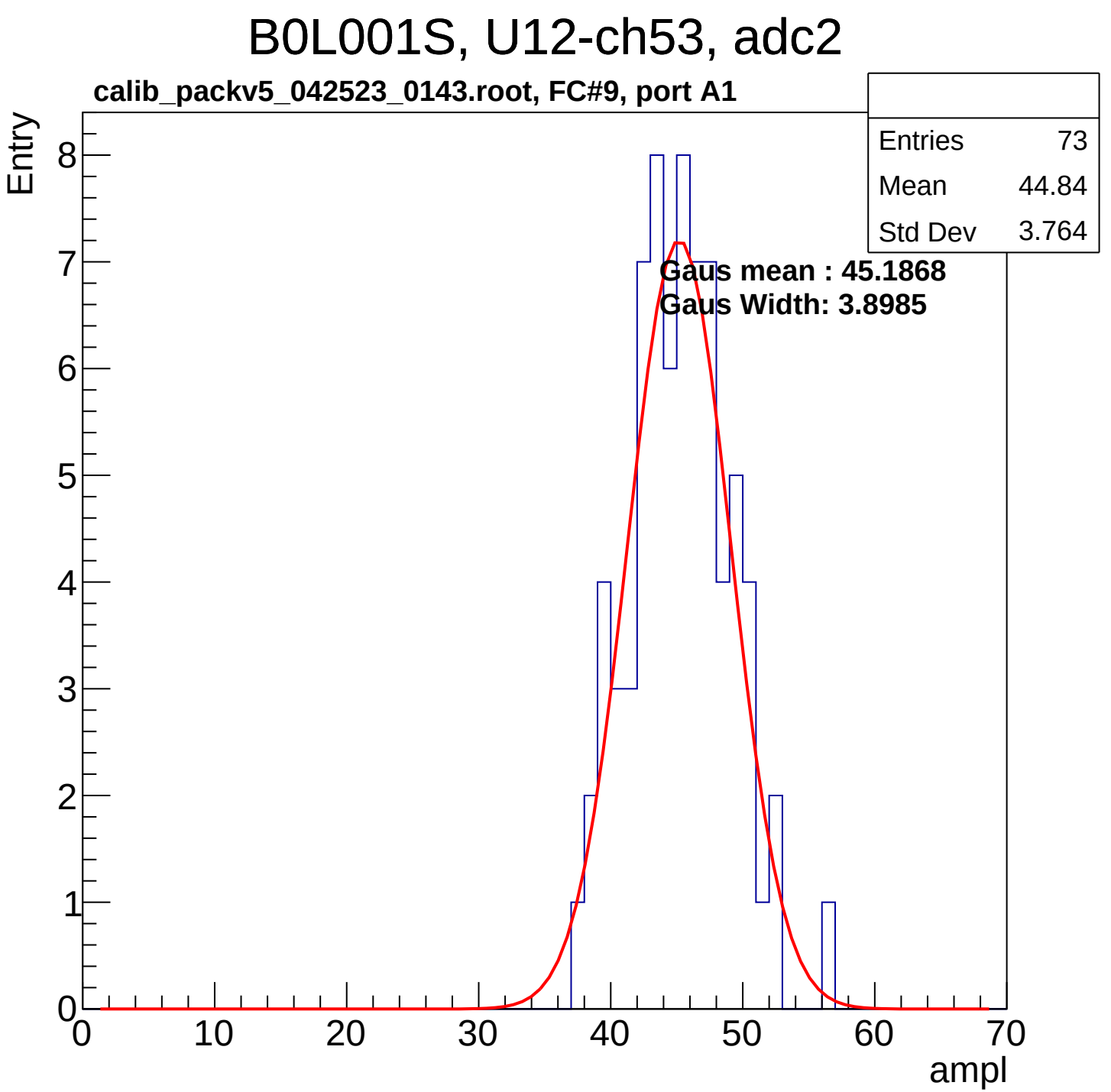
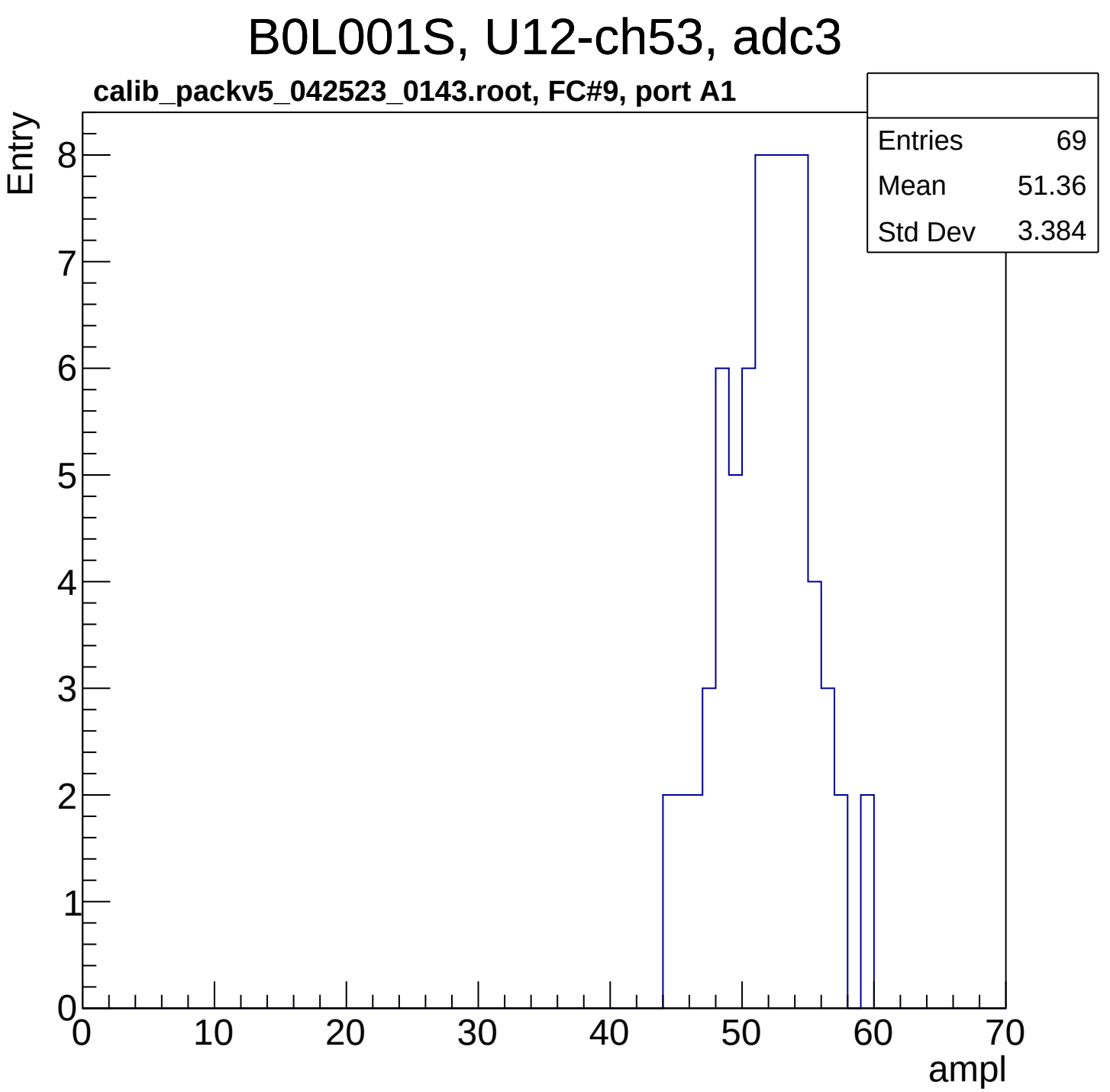
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch53, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 73
Mean 44.84
Std Dev 3.764
Gaus mean : 45.1868
Gaus Width: 3.8985
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch53, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 69
Mean 51.36
Std Dev 3.384
Entry
ampl
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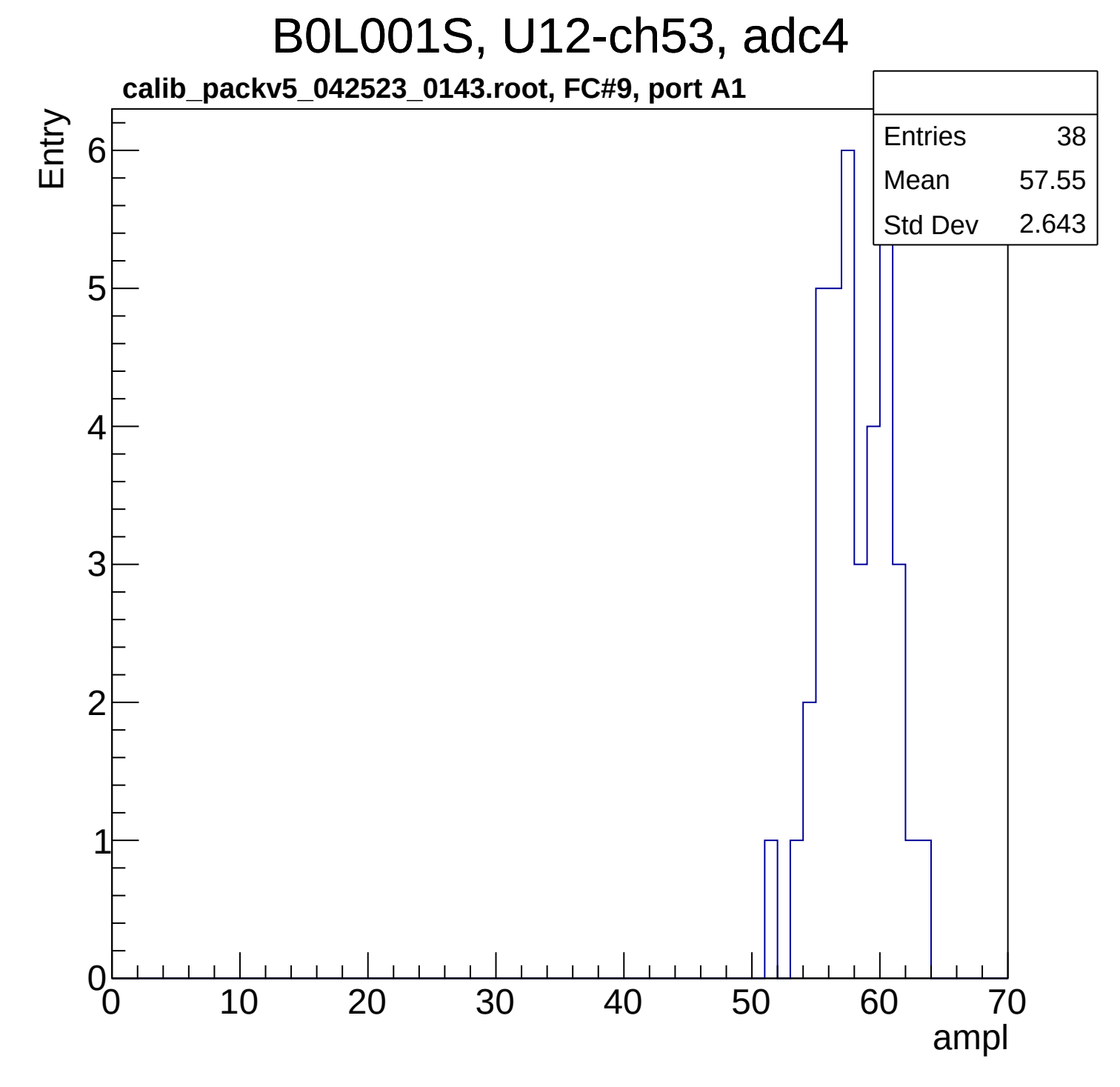
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch53, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 38
Mean 57.55
Std Dev 2.643
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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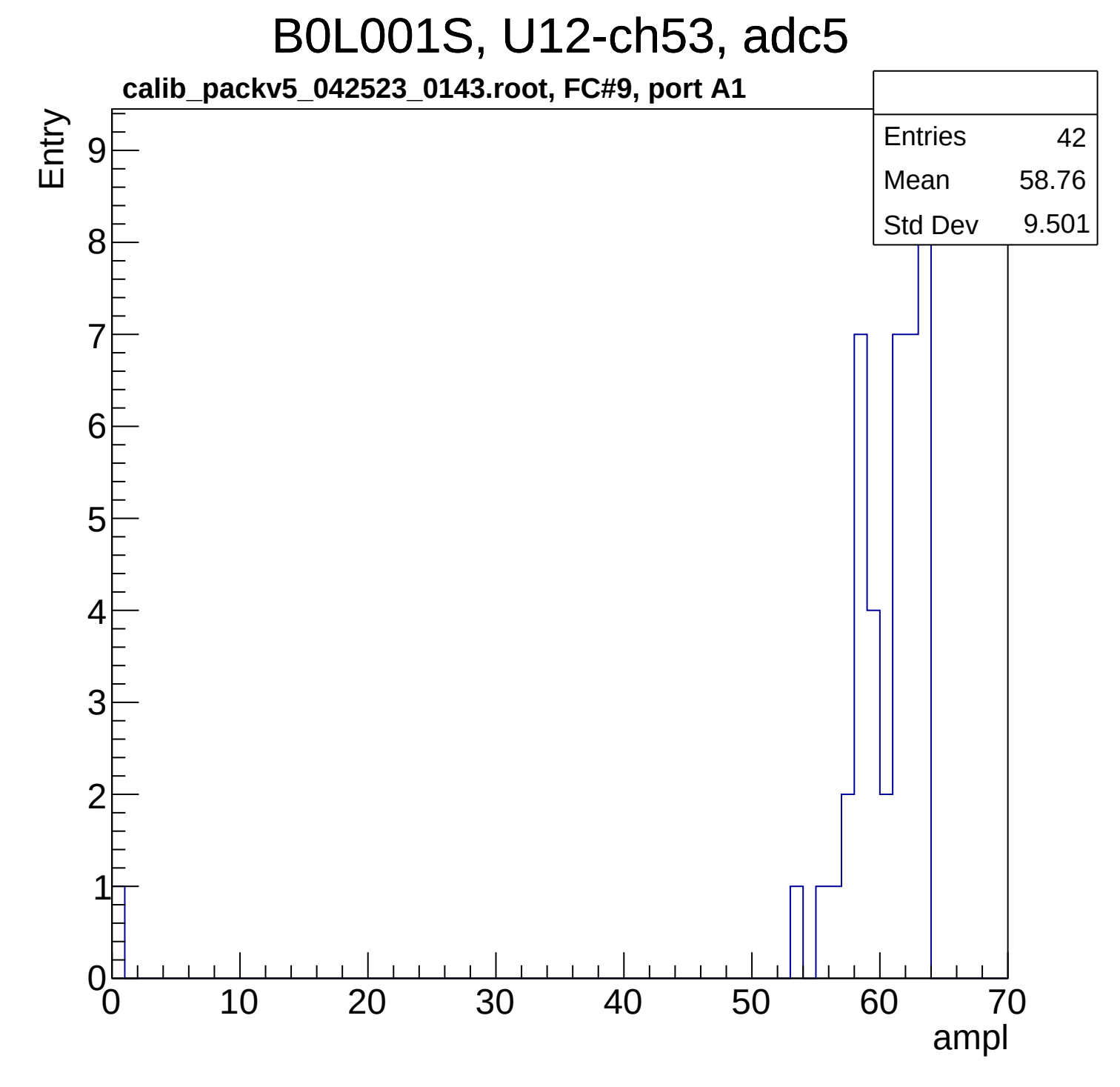
B0L001S, U12-ch53, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 42
Mean 58.76
Std Dev 9.501
Entry
ampl
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2
3
4
5
6
7
8
9
0
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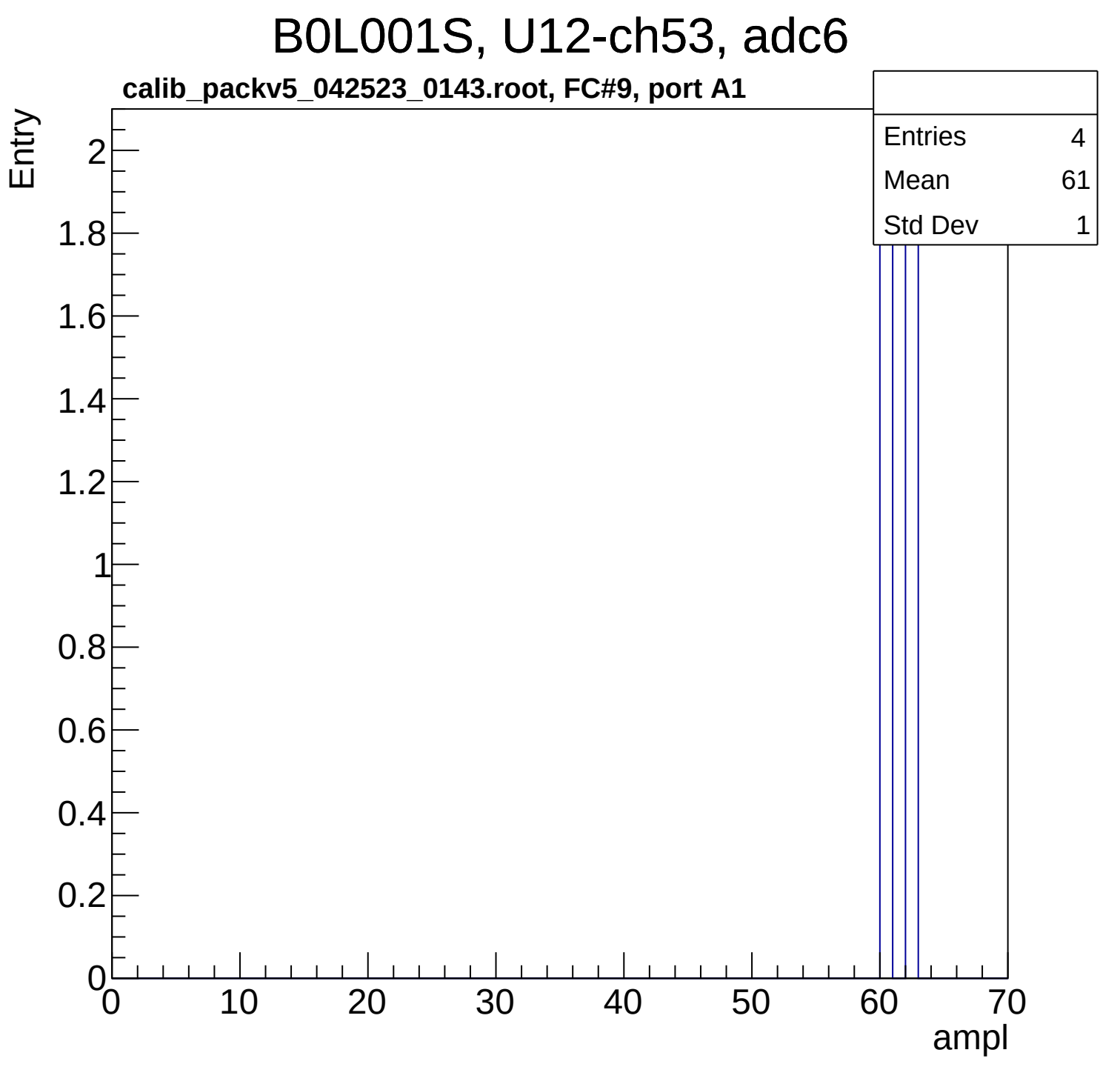
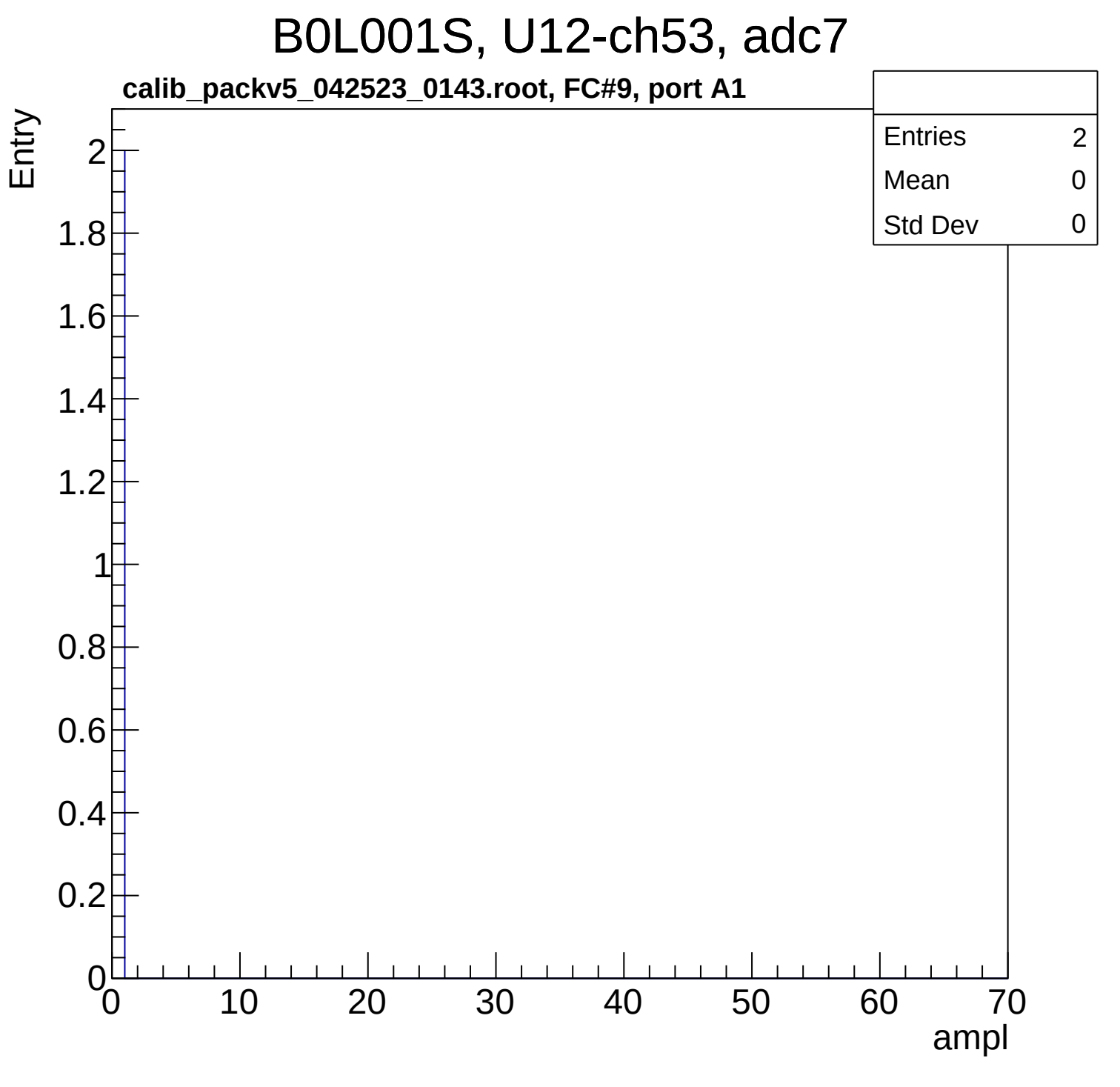
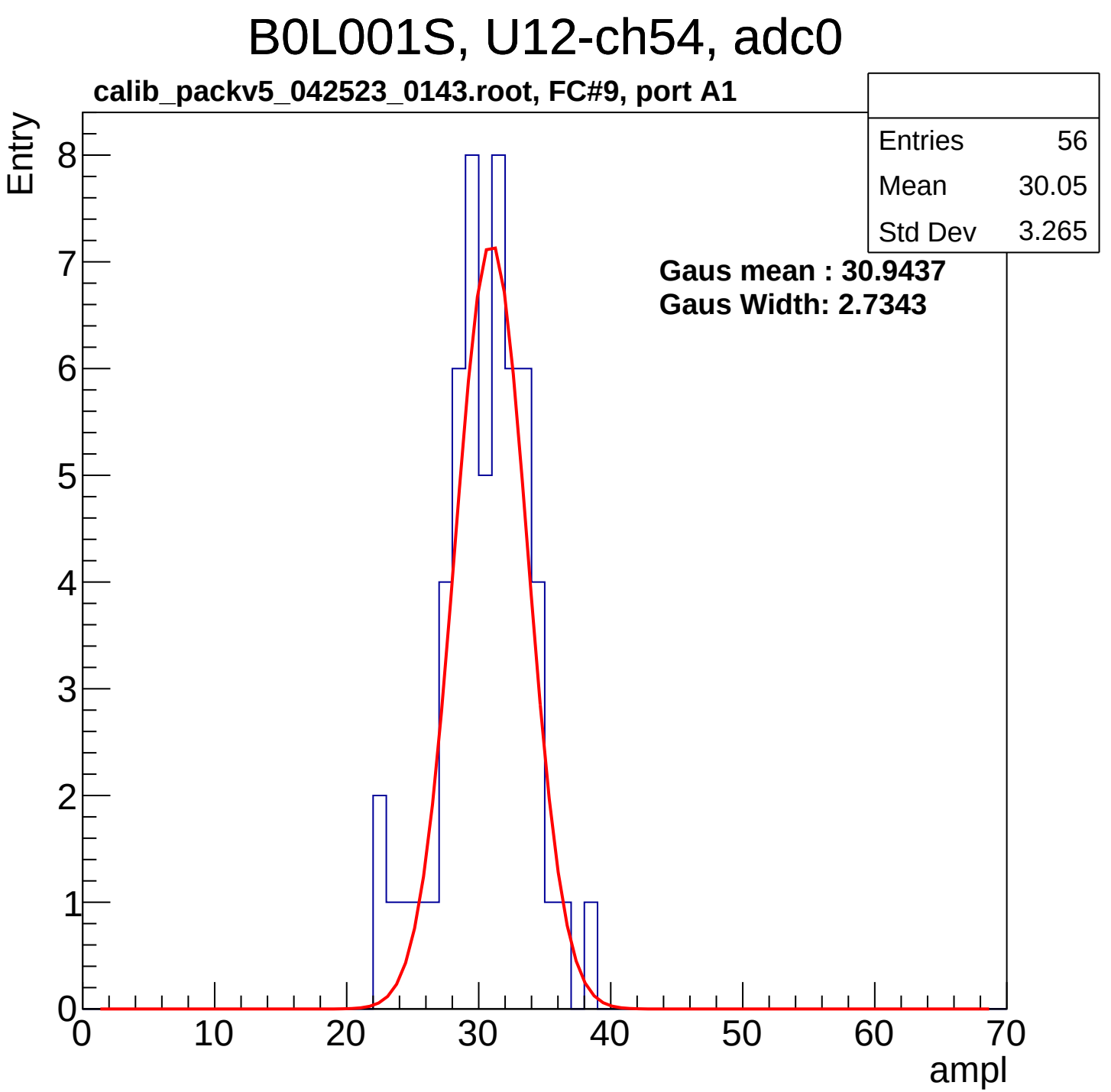

B0L001S, U12-ch53, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 4
Mean 61
Std Dev 1
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L001S, U12-ch53, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch54, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 56
Mean 30.05
Std Dev 3.265
Gaus mean : 30.9437
Gaus Width: 2.7343
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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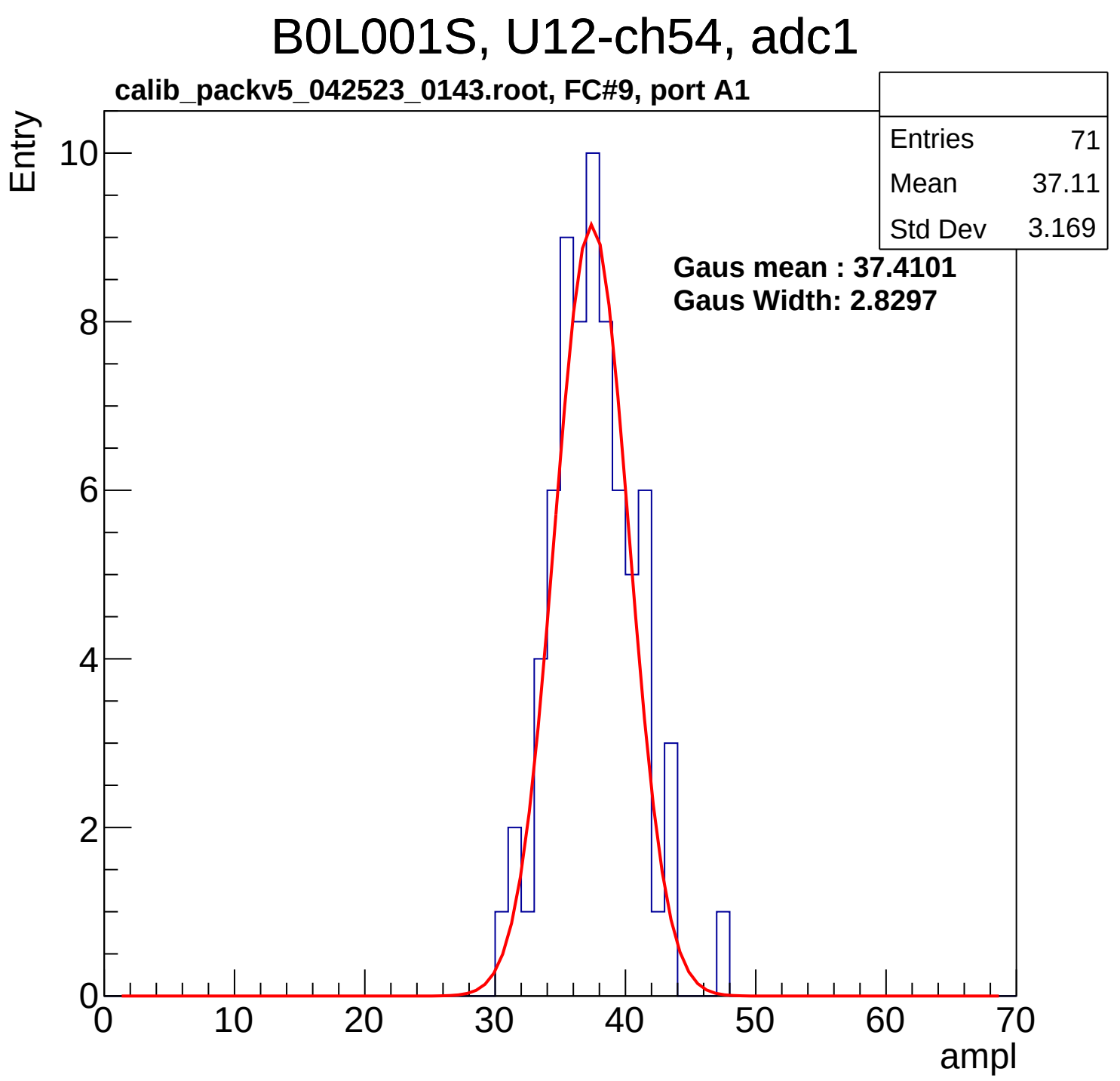
B0L001S, U12-ch54, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 71
Mean 37.11
Std Dev 3.169
Gaus mean : 37.4101
Gaus Width: 2.8297
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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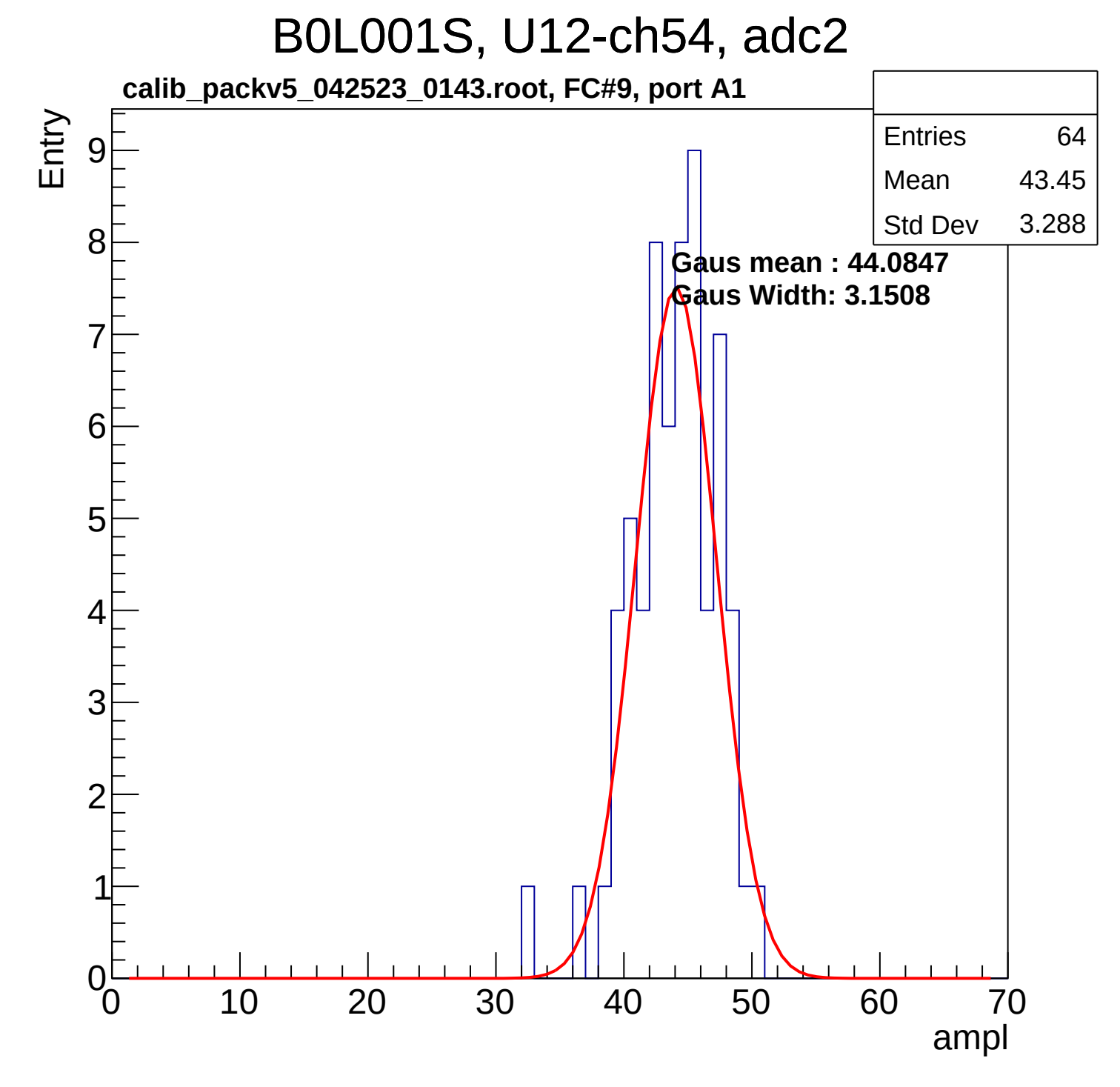
B0L001S, U12-ch54, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 64
Mean 43.45
Std Dev 3.288
Gaus mean : 44.0847
Gaus Width: 3.1508
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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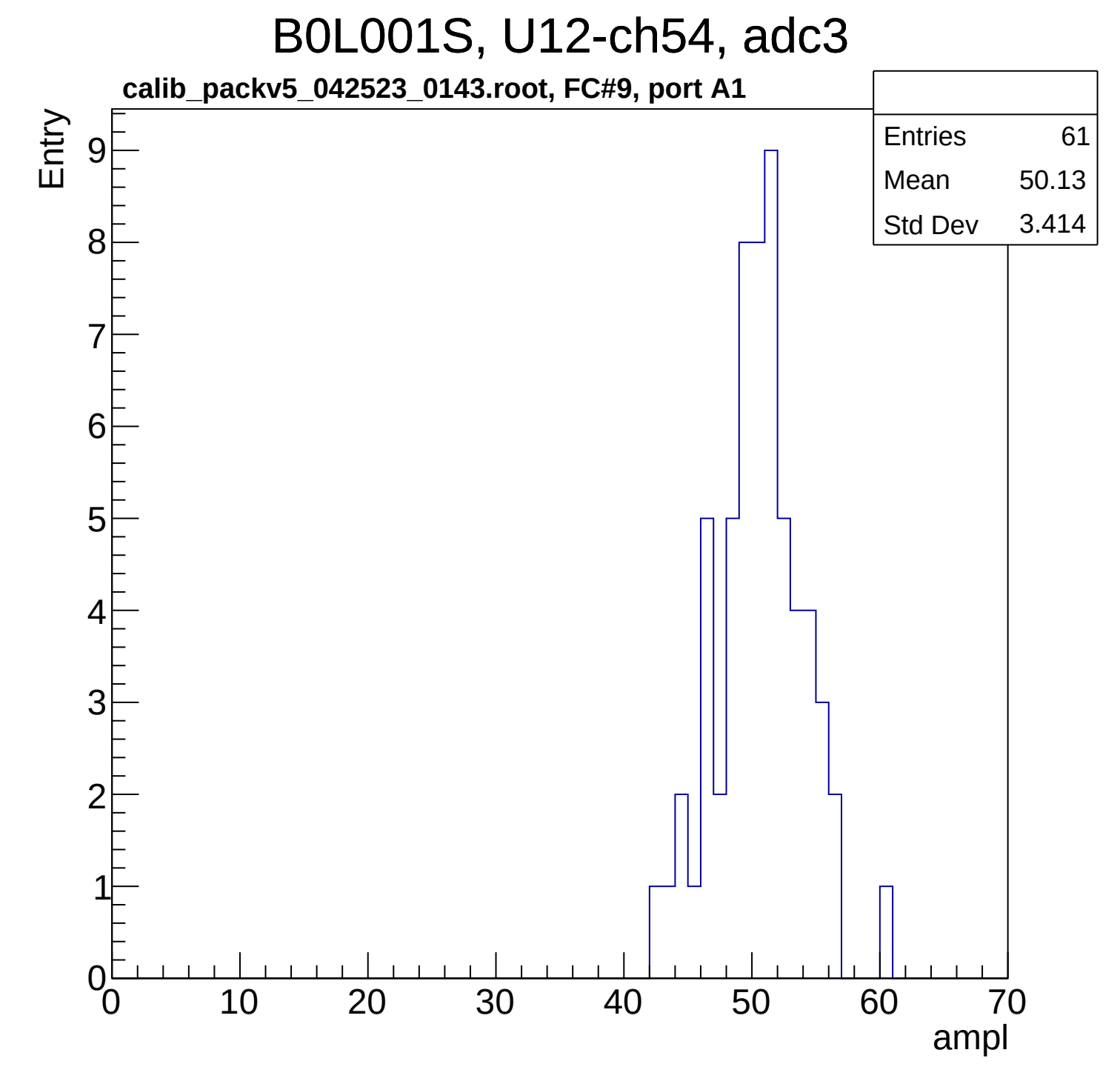
B0L001S, U12-ch54, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 61
Mean 50.13
Std Dev 3.414
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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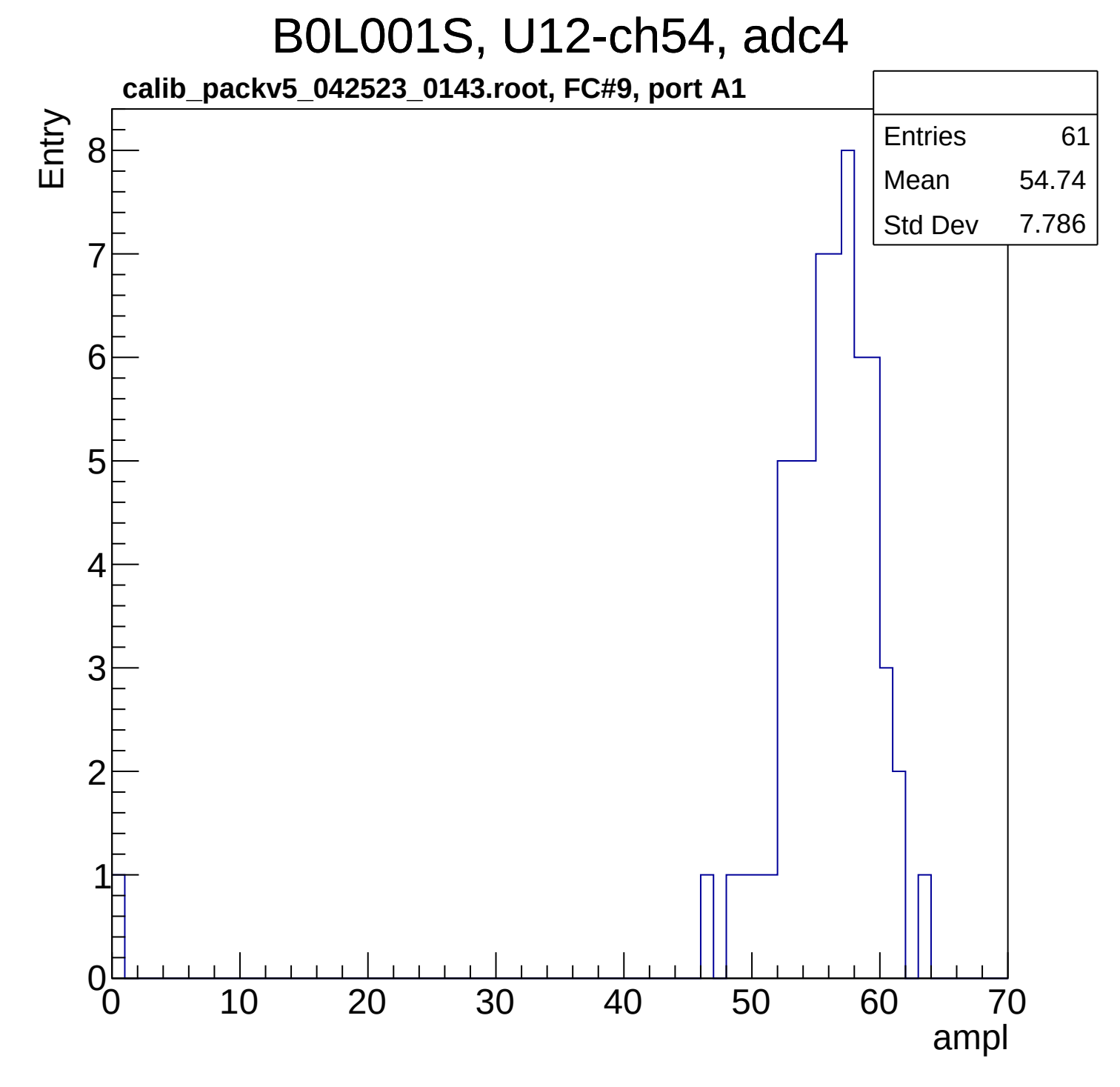
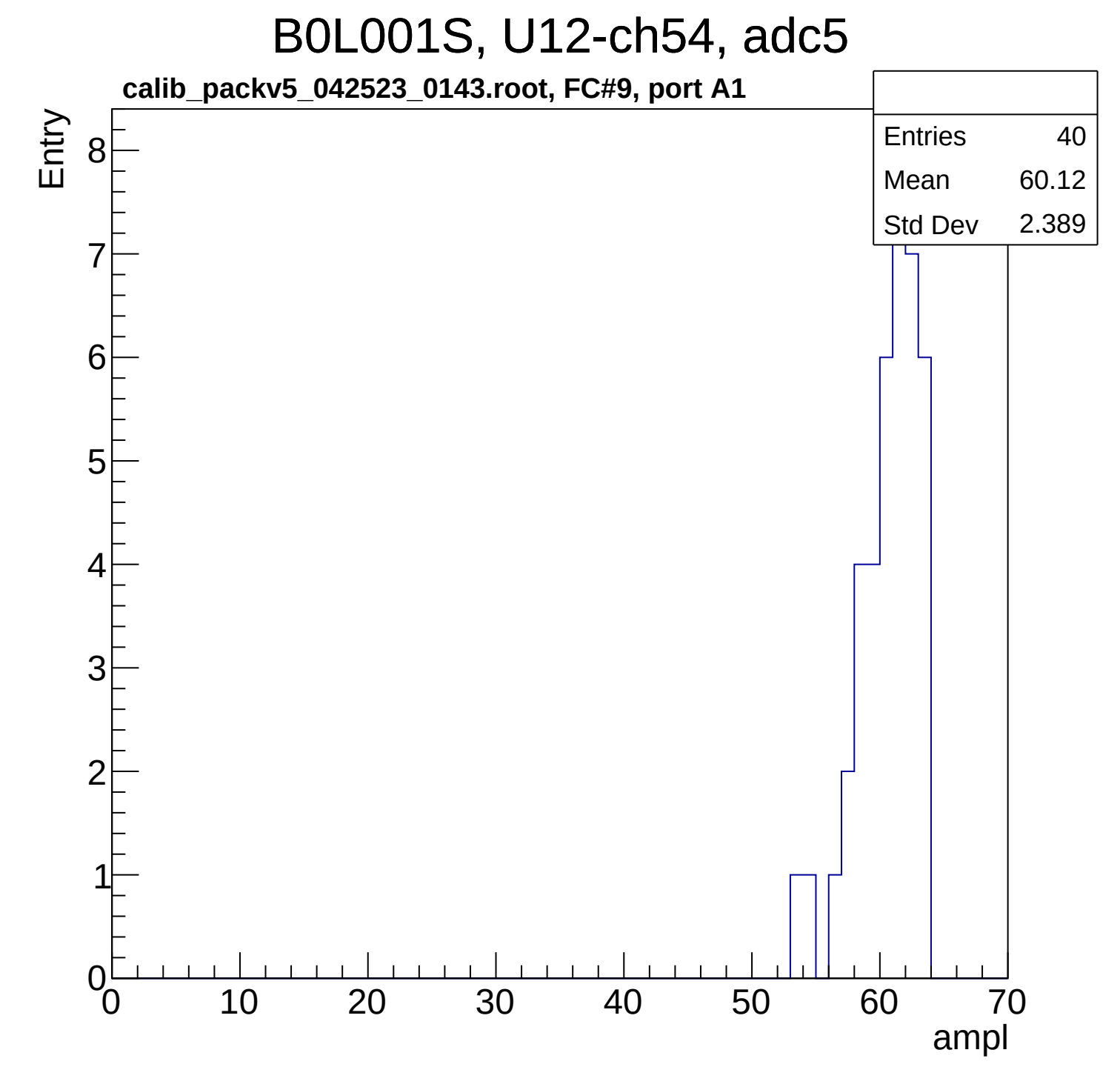
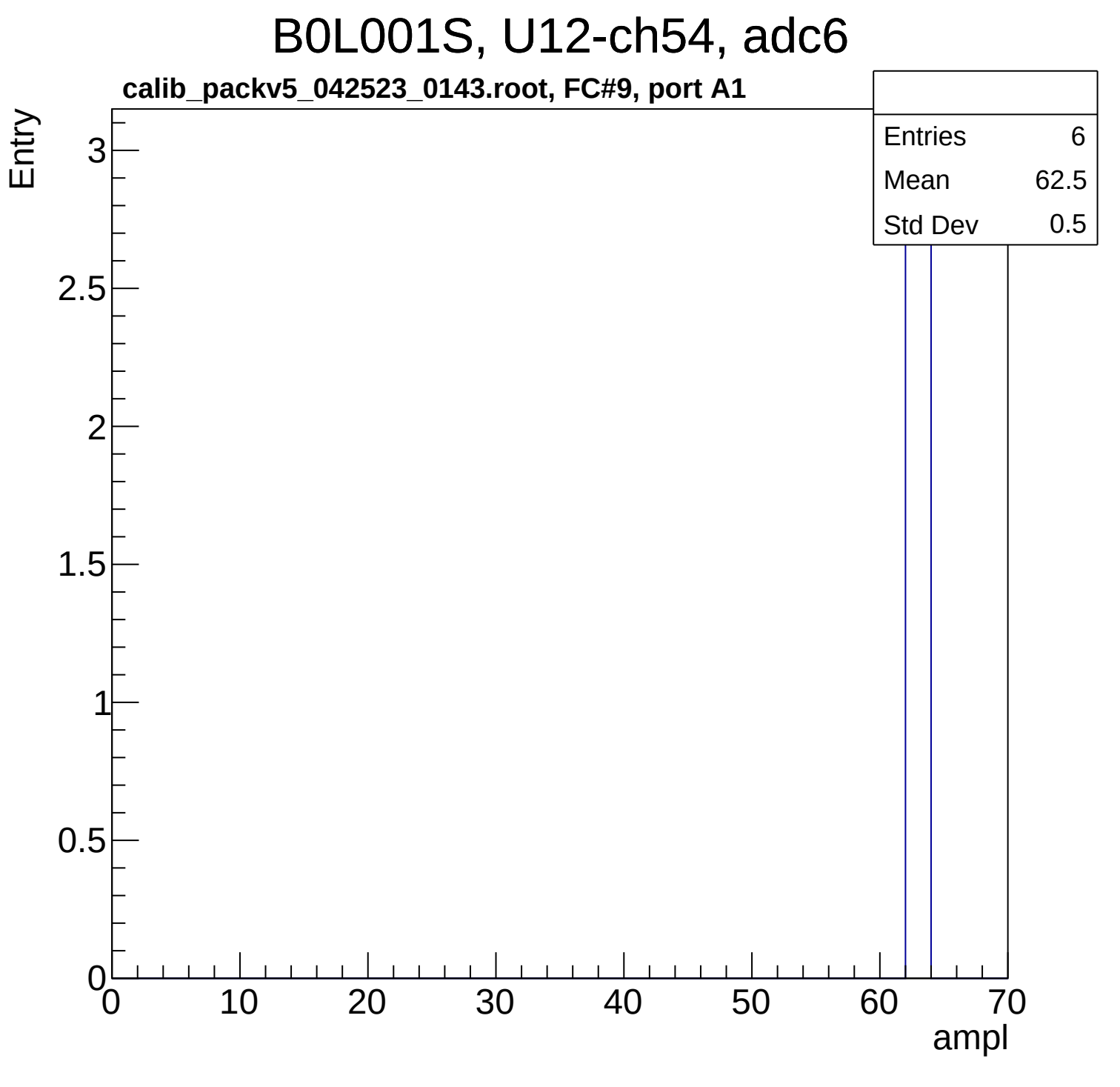
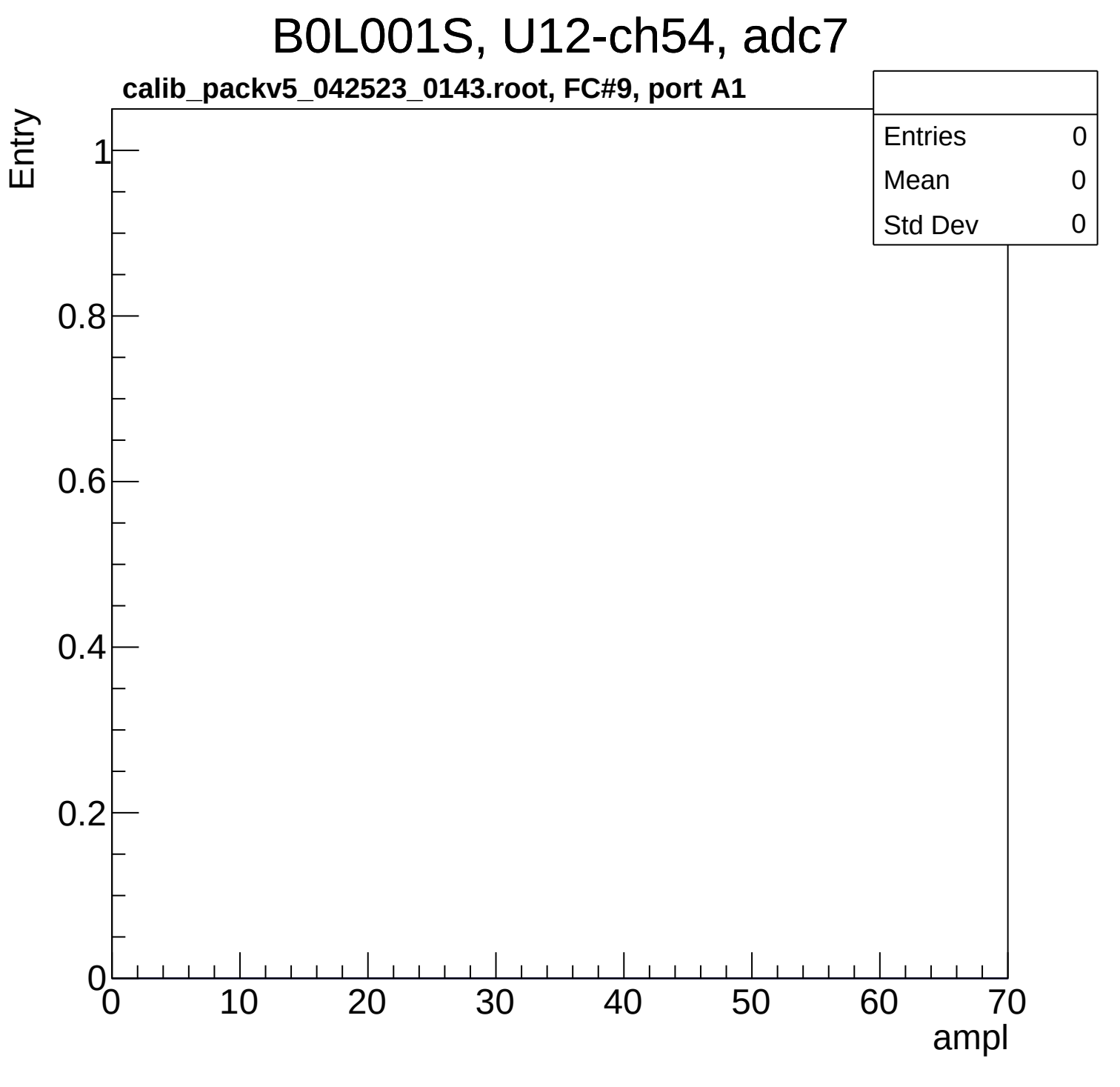
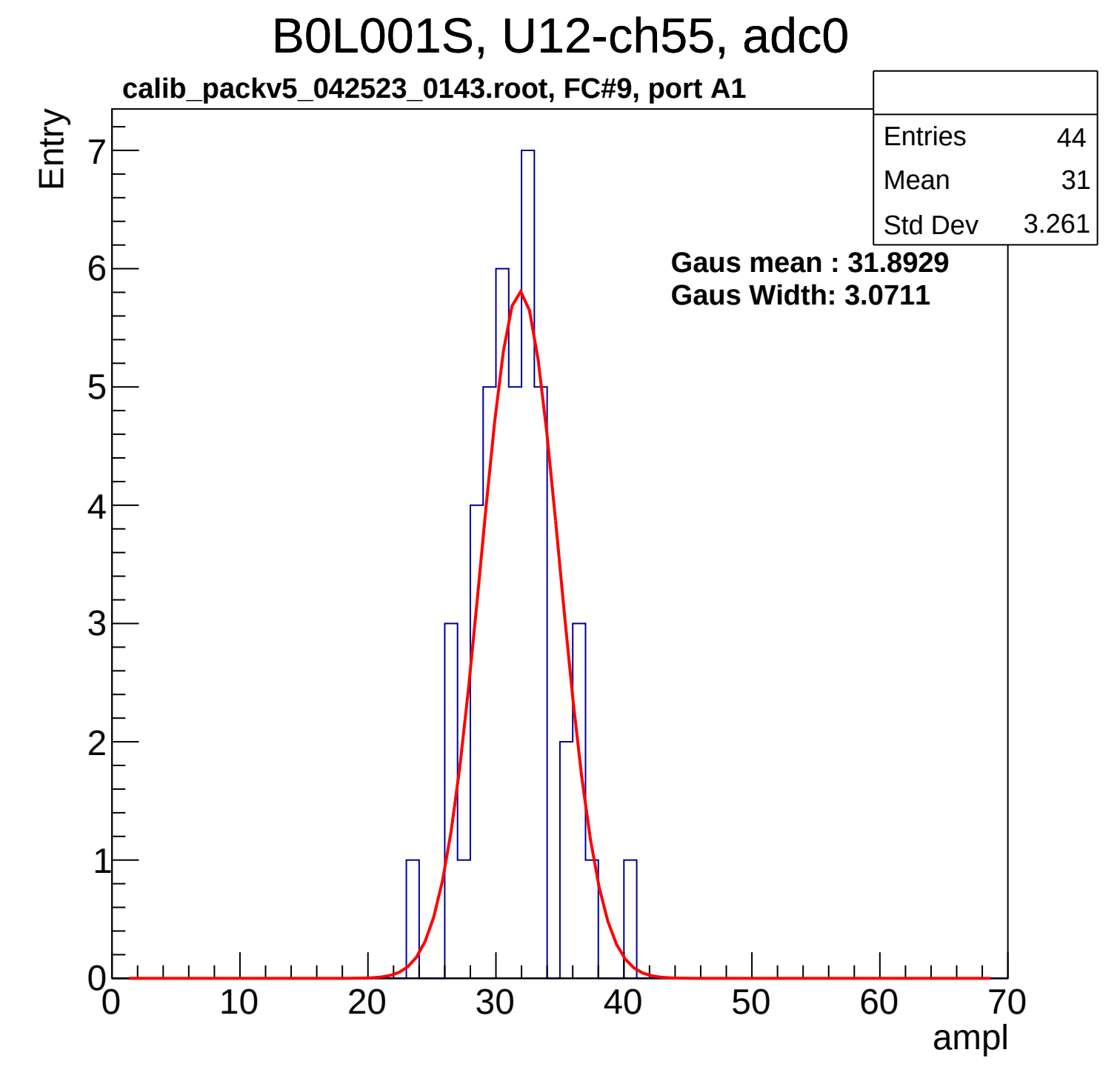
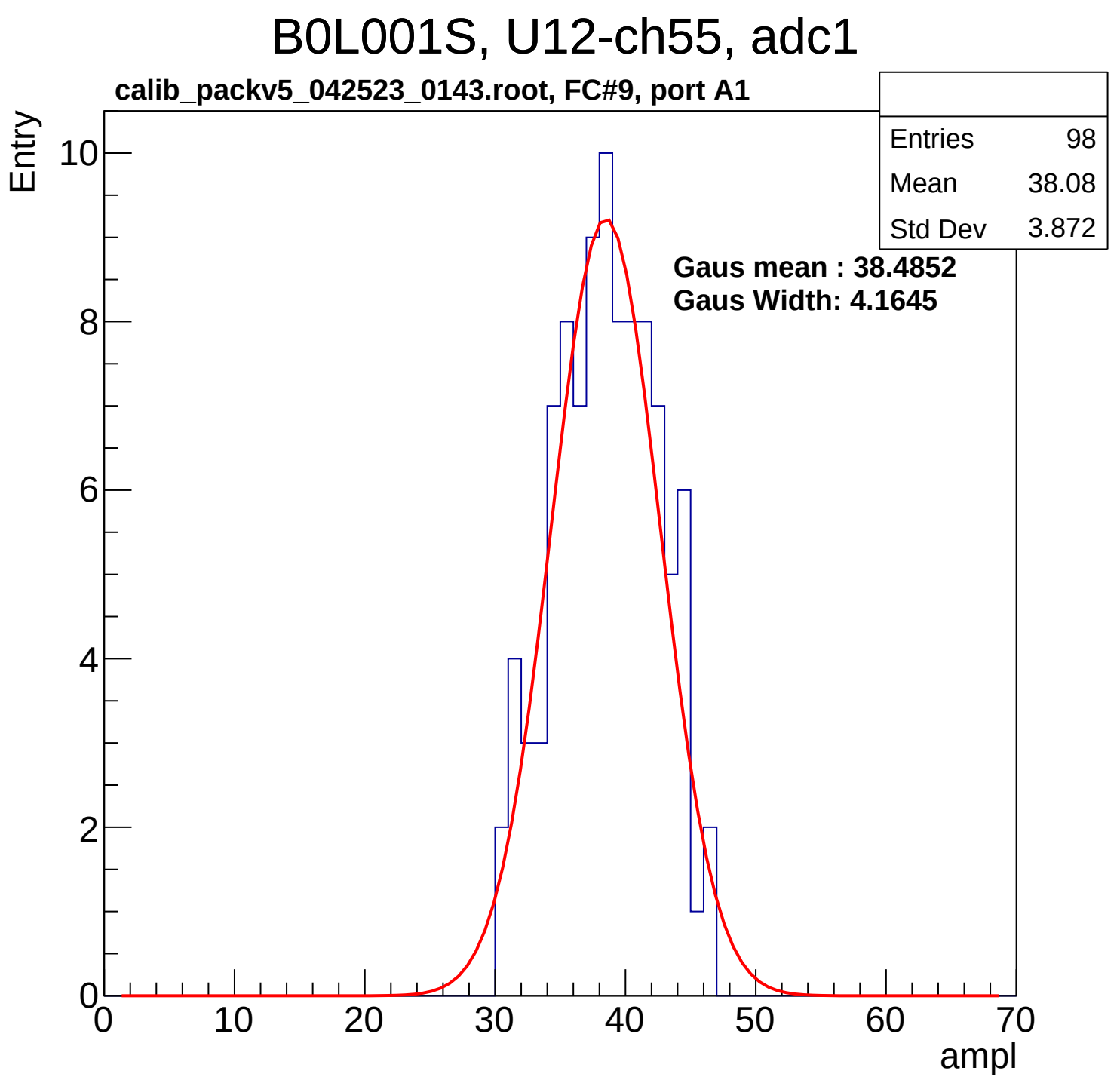

B0L001S, U12-ch54, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 61
Mean 54.74
Std Dev 7.786
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch54, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 40
Mean 60.12
Std Dev 2.389
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch54, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 6
Mean 62.5
Std Dev 0.5
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B0L001S, U12-ch54, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch55, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 44
Mean 31
Std Dev 3.261
Gaus mean : 31.8929
Gaus Width: 3.0711
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B0L001S, U12-ch55, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 98
Mean 38.08
Std Dev 3.872
Gaus mean : 38.4852
Gaus Width: 4.1645
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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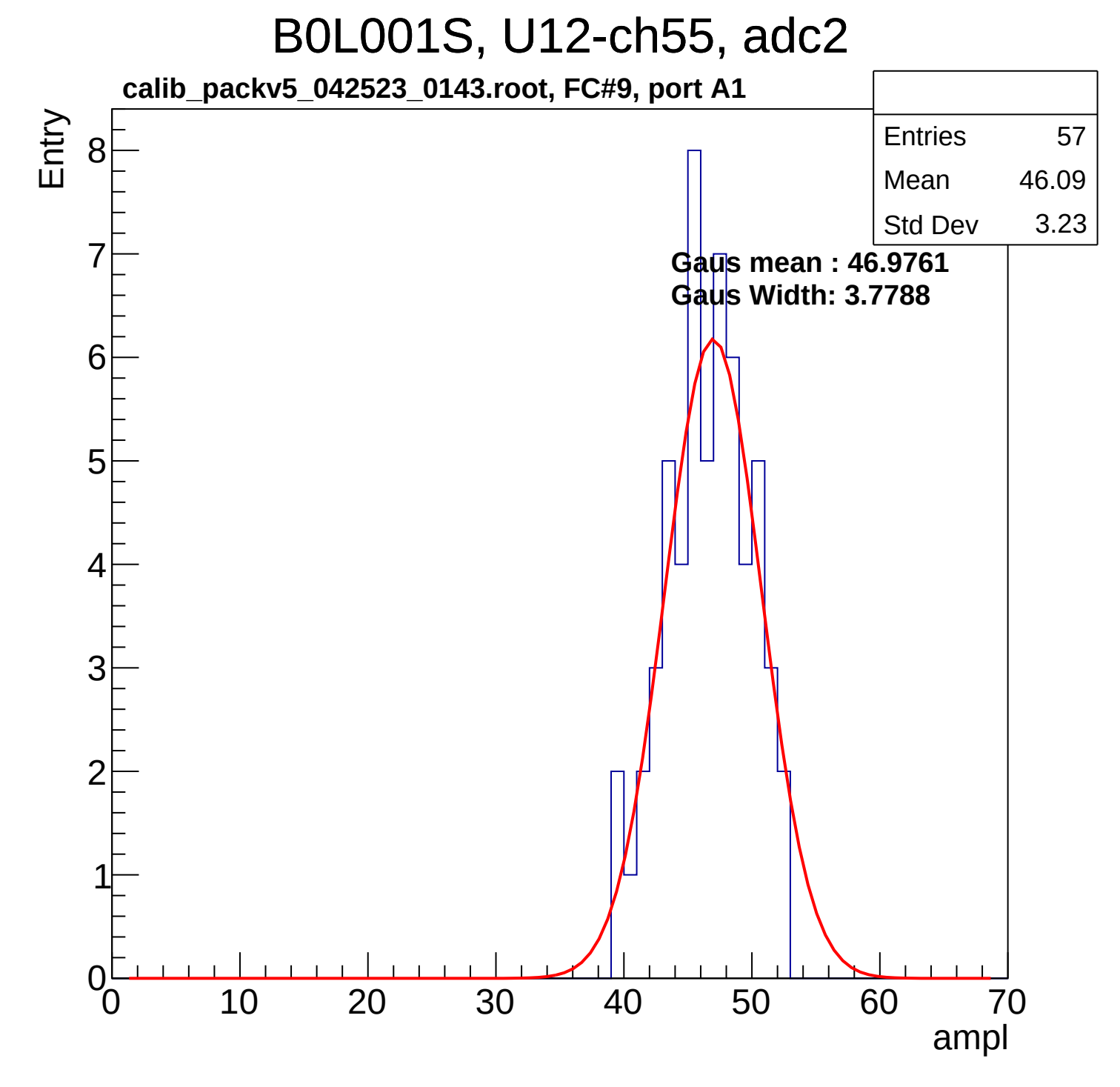
B0L001S, U12-ch55, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 57
Mean 46.09
Std Dev 3.23
Gaus mean : 46.9761
Gaus Width: 3.7788
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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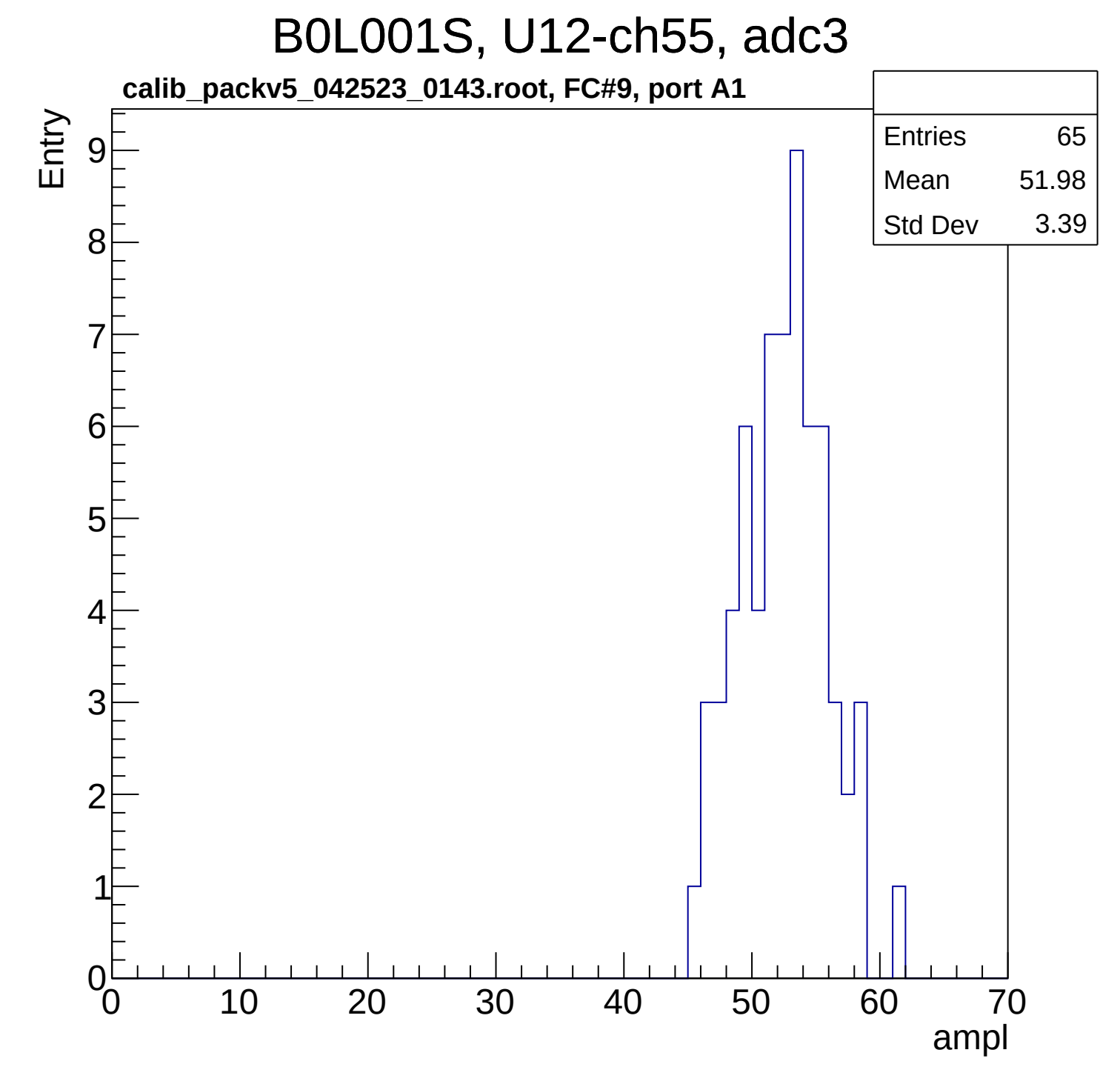
B0L001S, U12-ch55, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 65
Mean 51.98
Std Dev 3.39
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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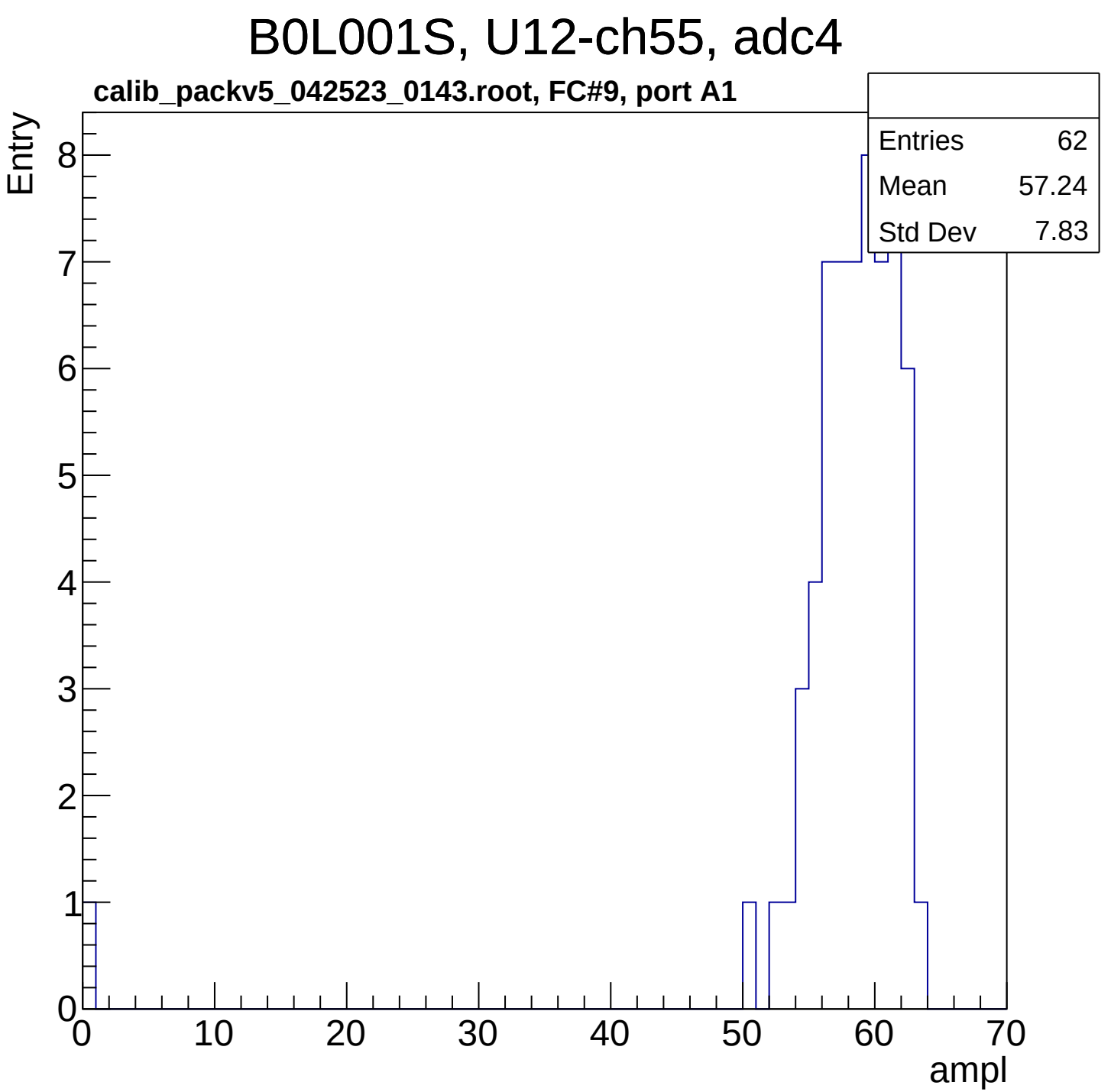
B0L001S, U12-ch55, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 62
Mean 57.24
Std Dev 7.83
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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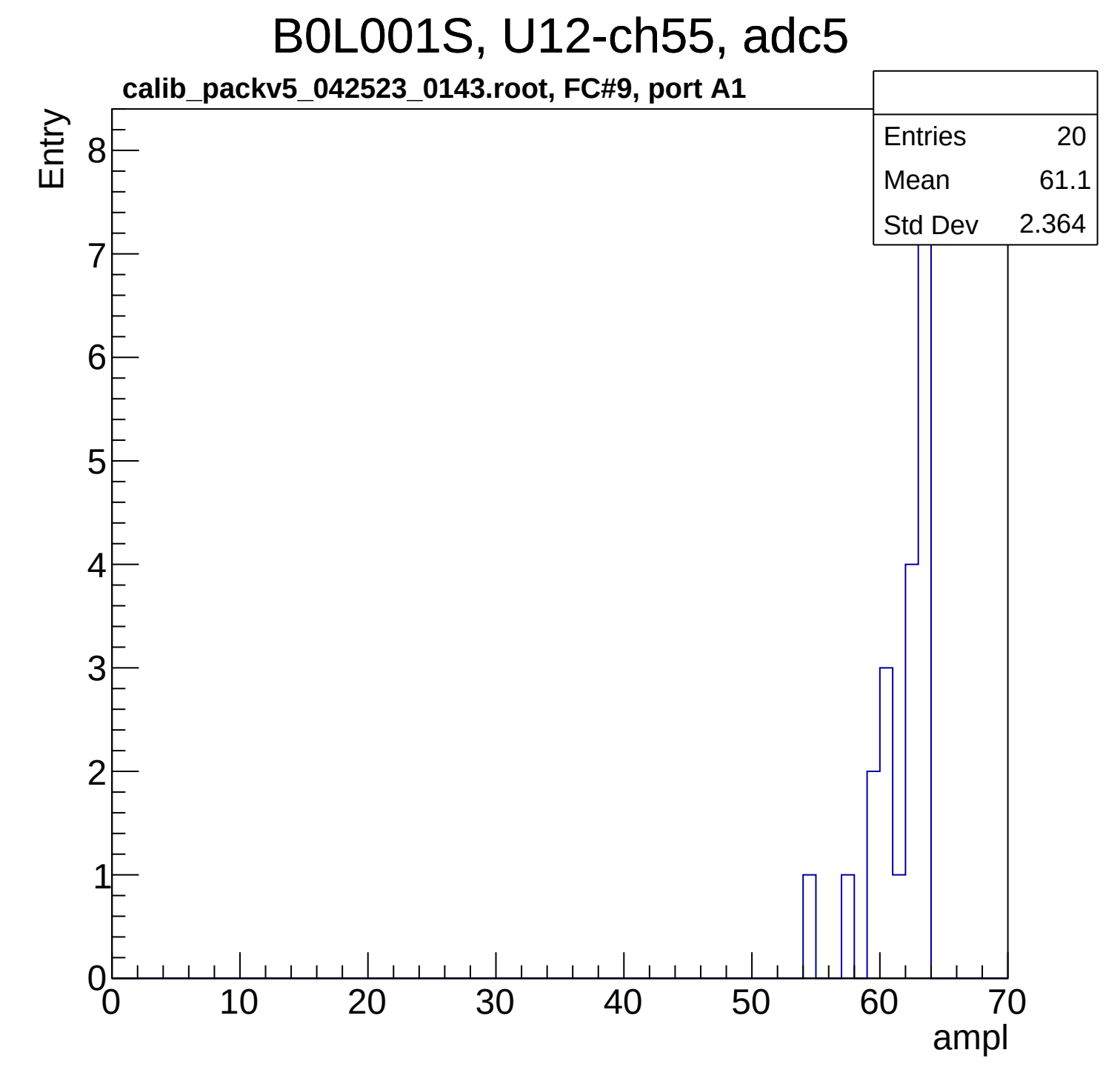
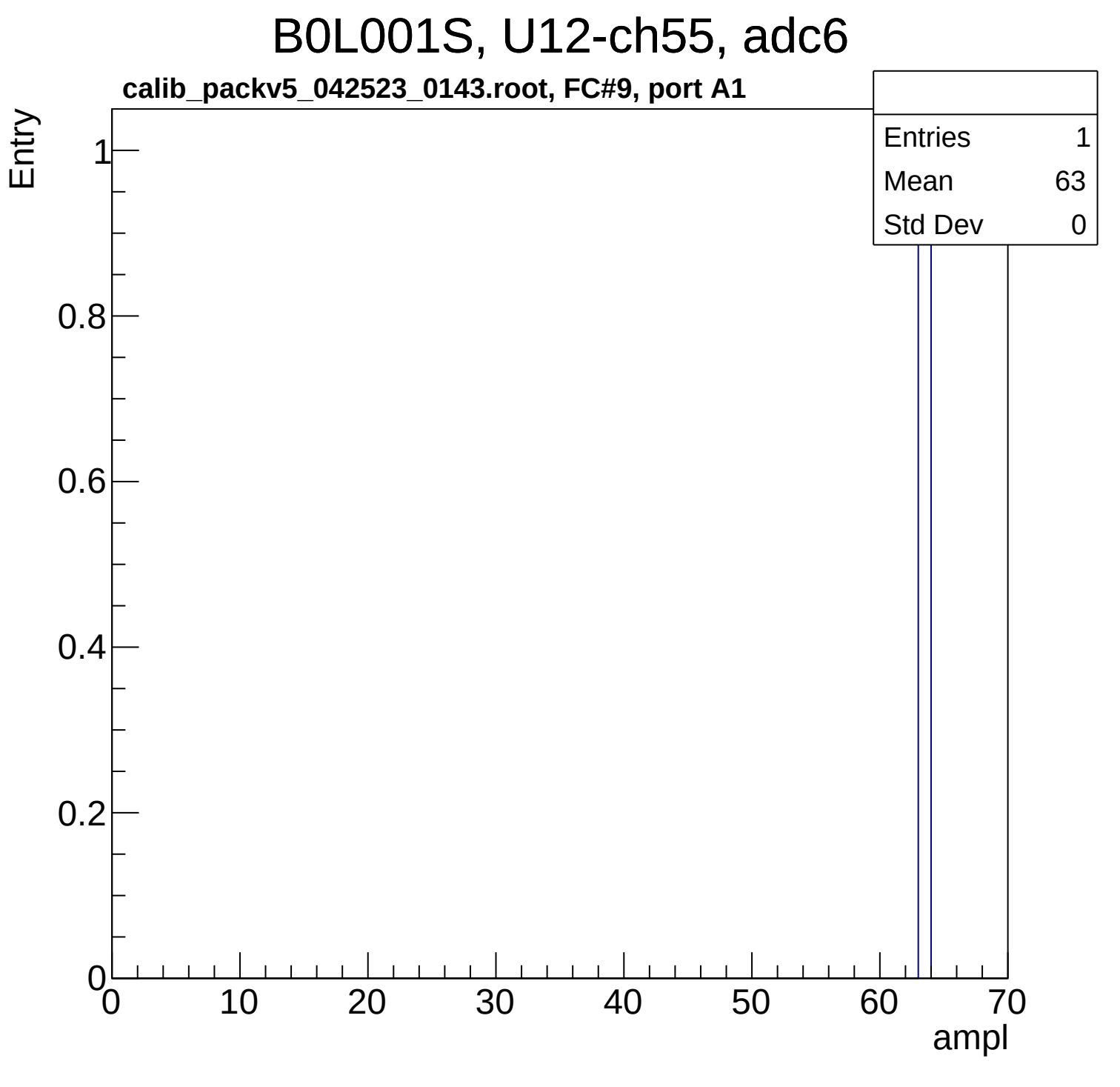
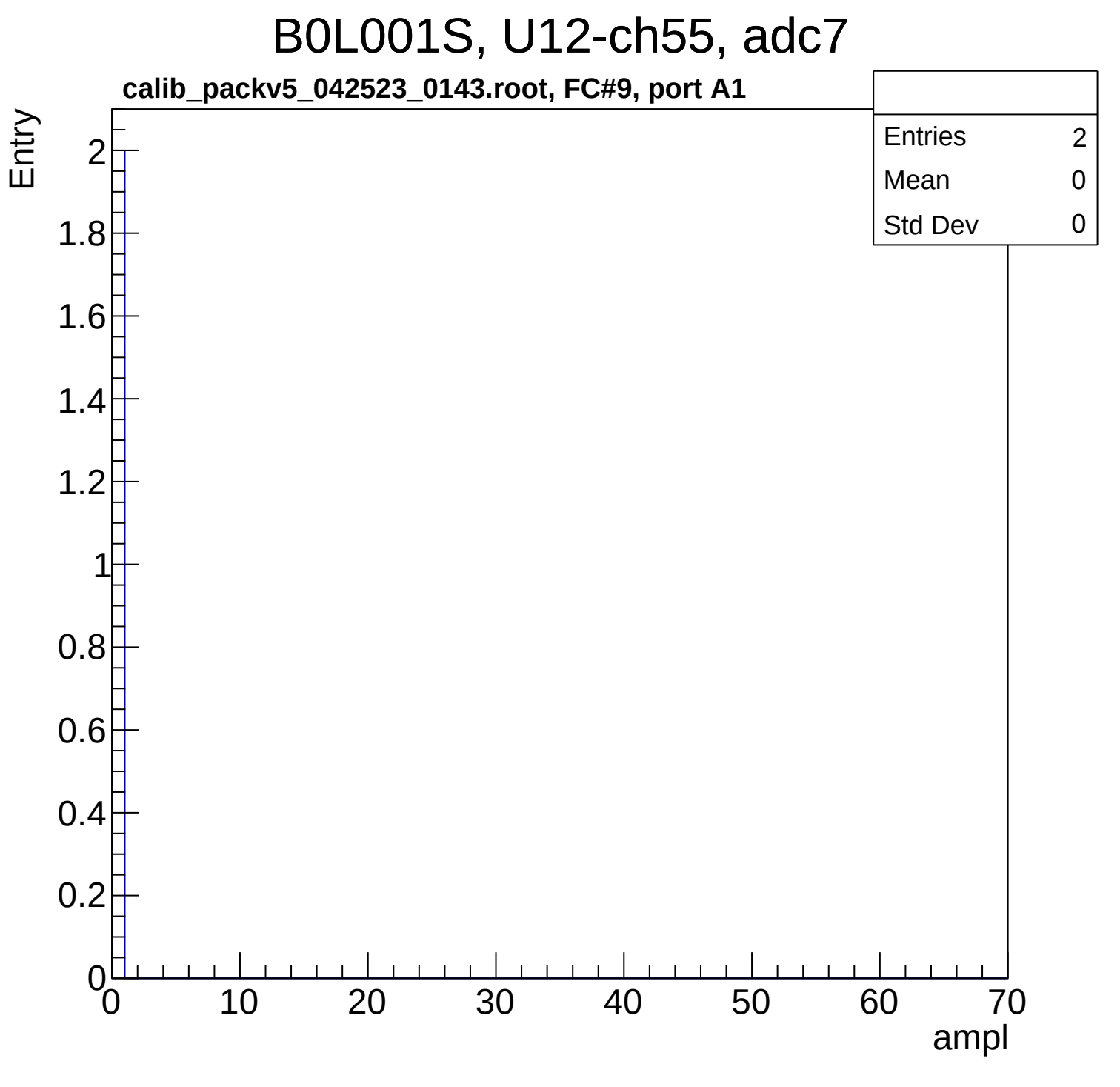
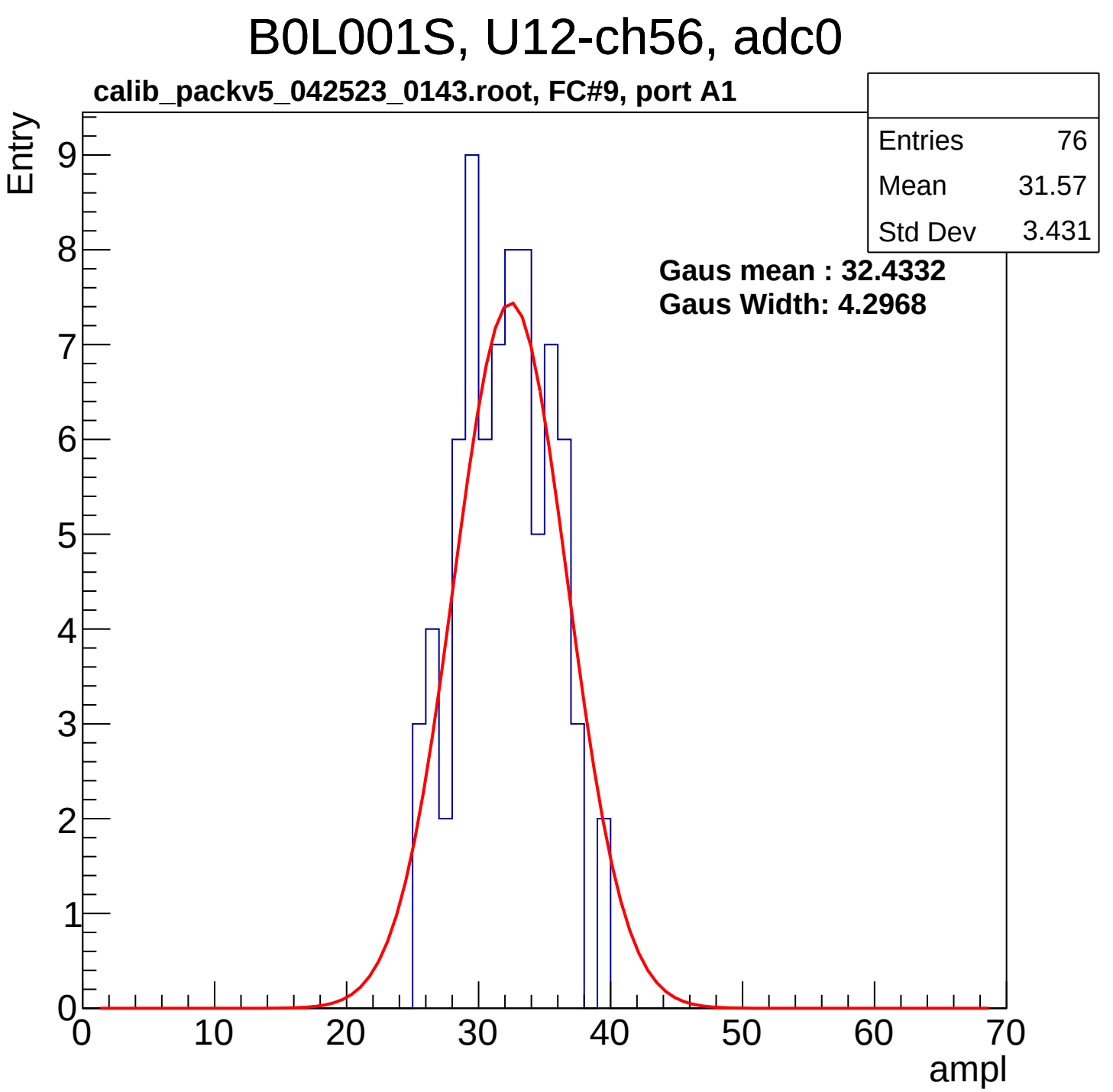
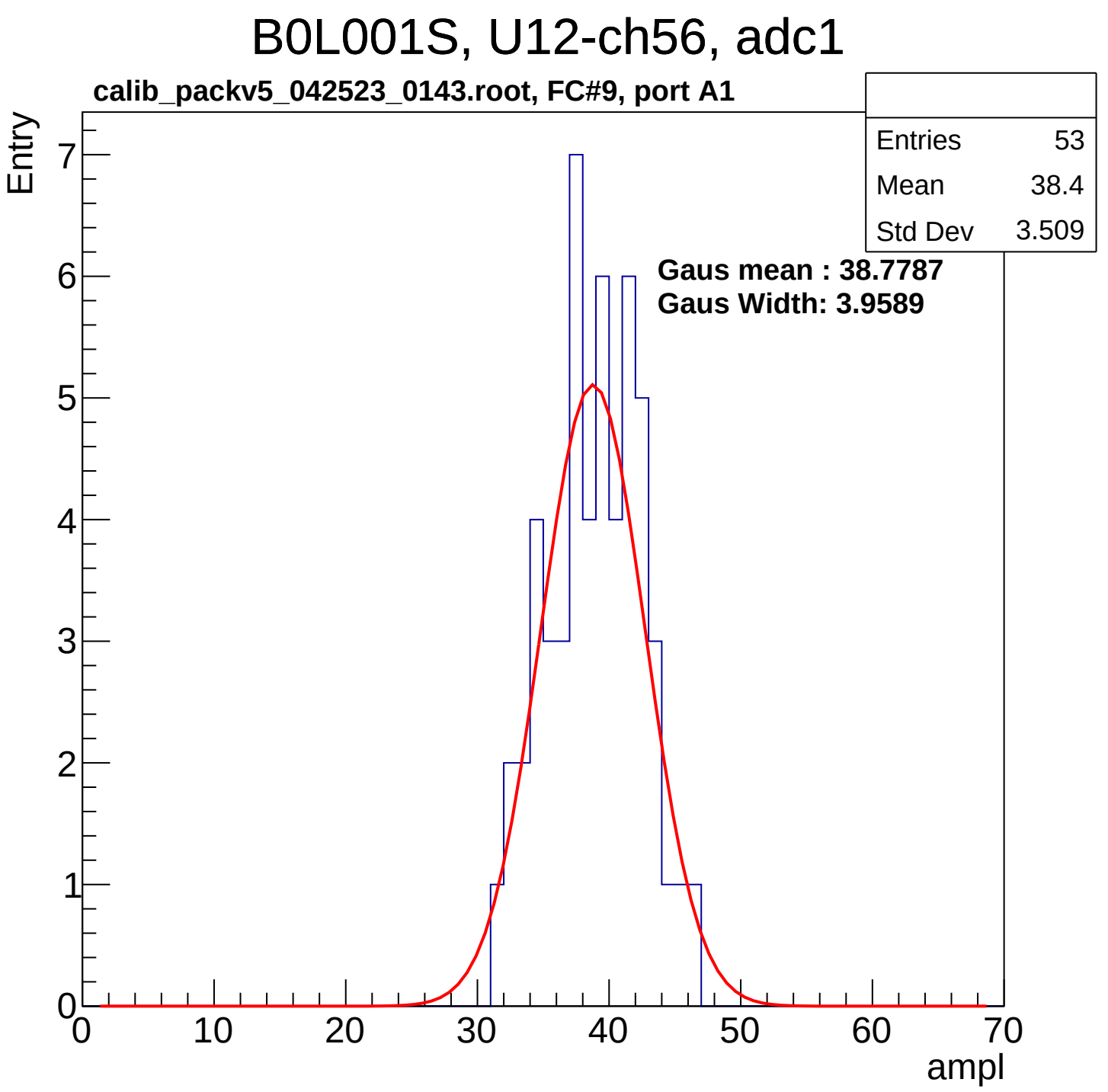
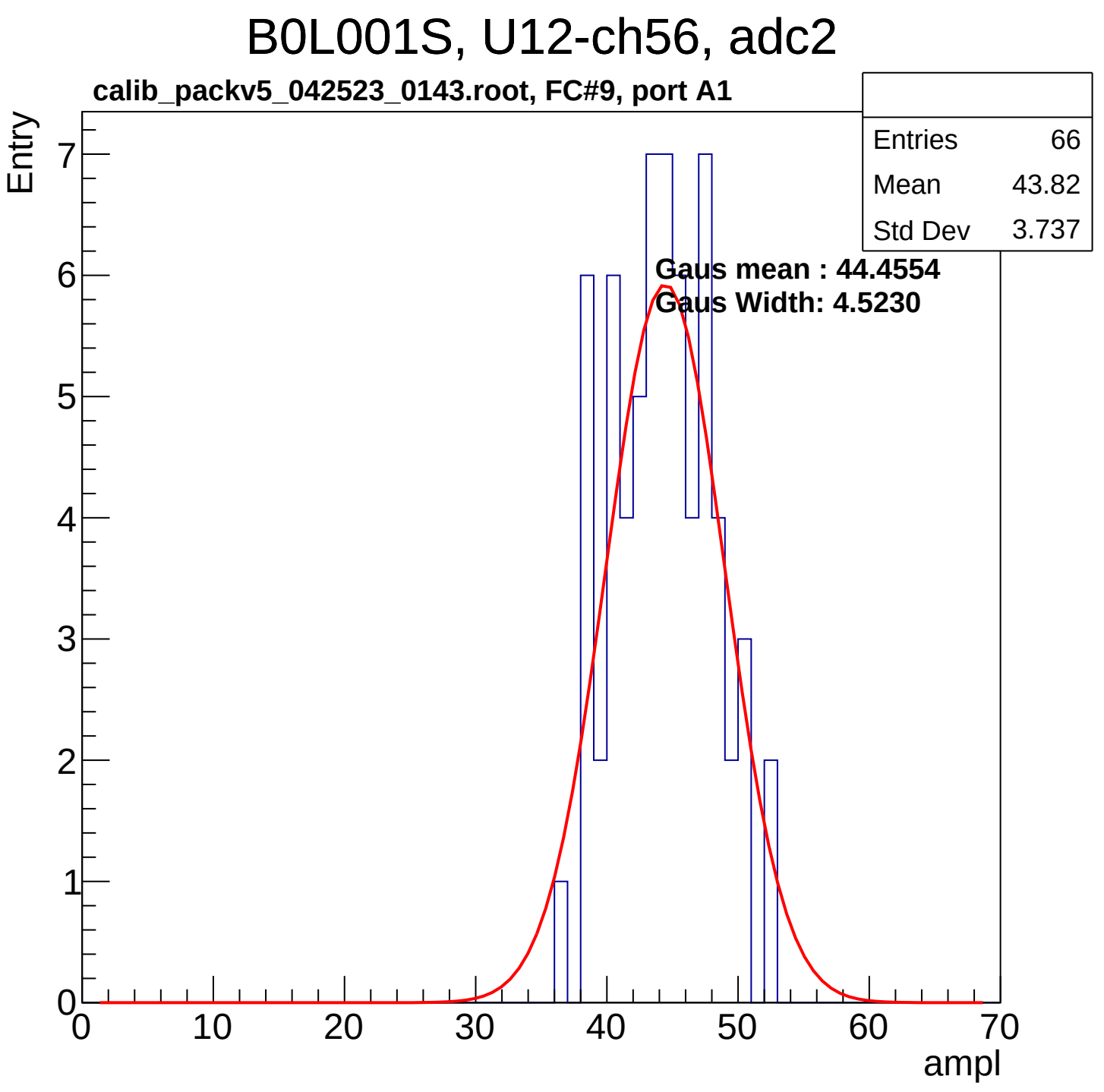

B0L001S, U12-ch55, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 20
Mean 61.1
Std Dev 2.364
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

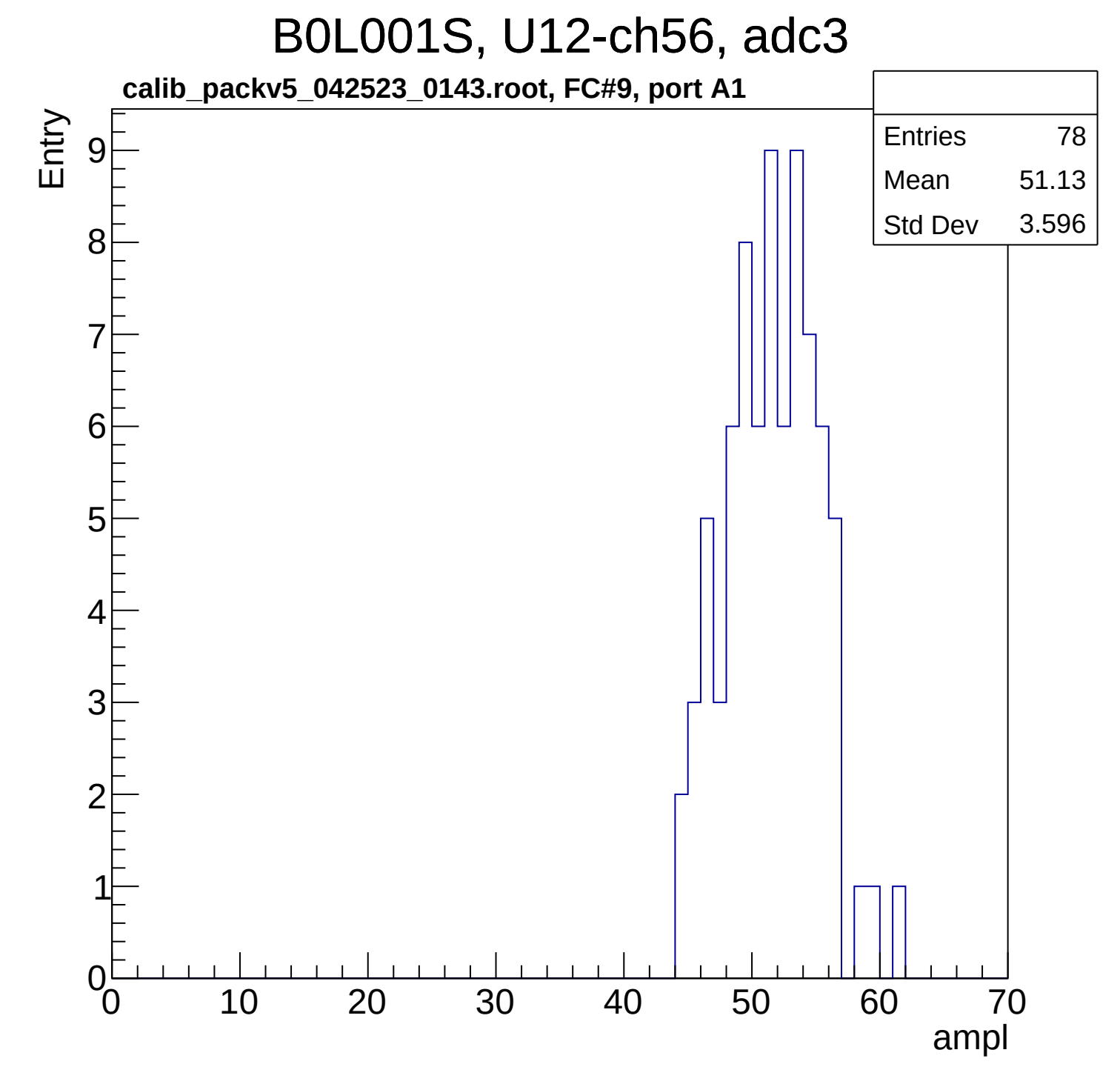

B0L001S, U12-ch55, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch55, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L001S, U12-ch56, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 76
Mean 31.57
Std Dev 3.431
Gaus mean : 32.4332
Gaus Width: 4.2968
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch56, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 53
Mean 38.4
Std Dev 3.509
Gaus mean : 38.7787
Gaus Width: 3.9589
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B0L001S, U12-ch56, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 66
Mean 43.82
Std Dev 3.737
Gaus mean : 44.4554
Gaus Width: 4.5230
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B0L001S, U12-ch56, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 78
Mean 51.13
Std Dev 3.596
Entry
ampl
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4
5
6
7
8
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0
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60
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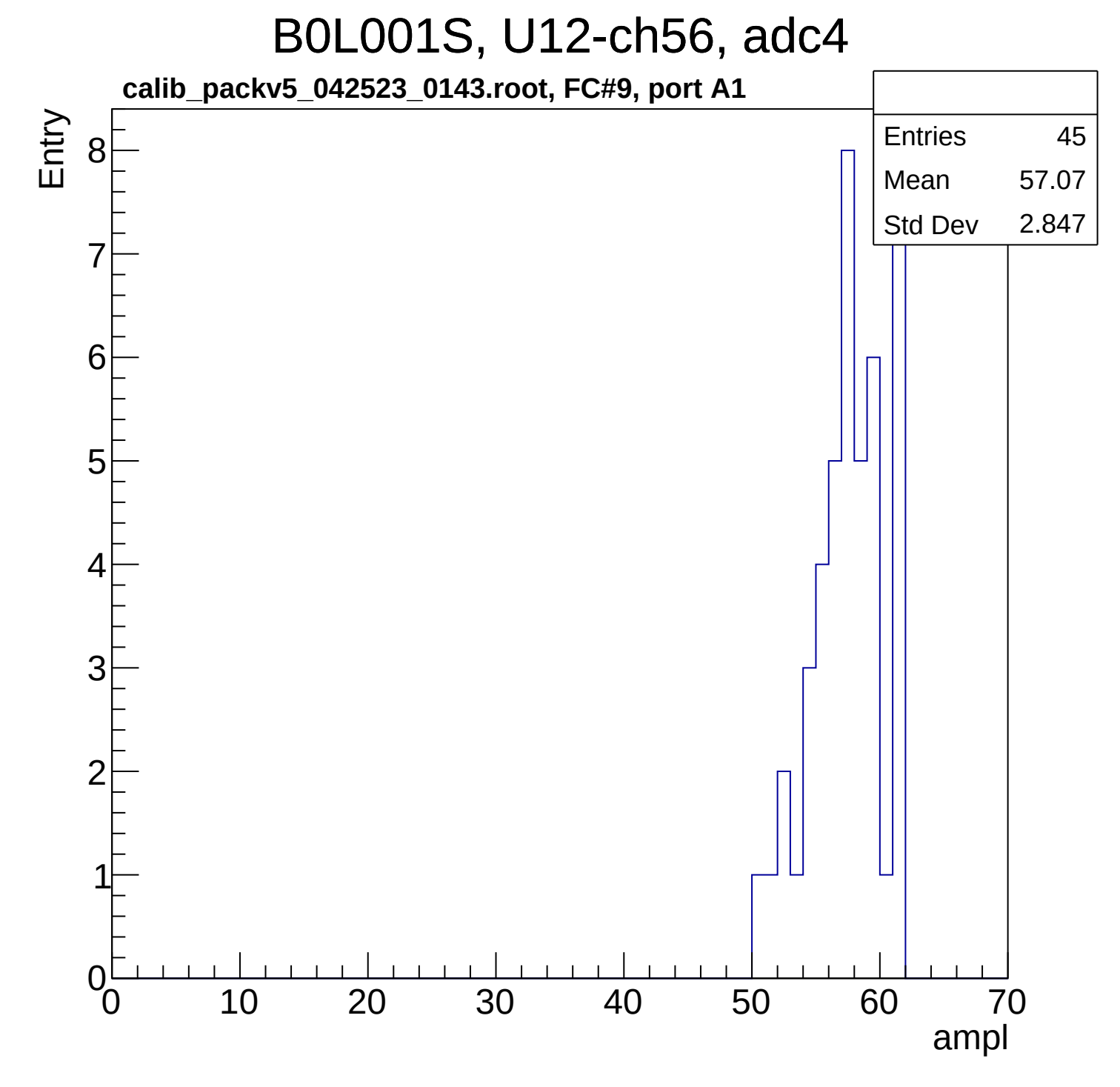
B0L001S, U12-ch56, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 45
Mean 57.07
Std Dev 2.847
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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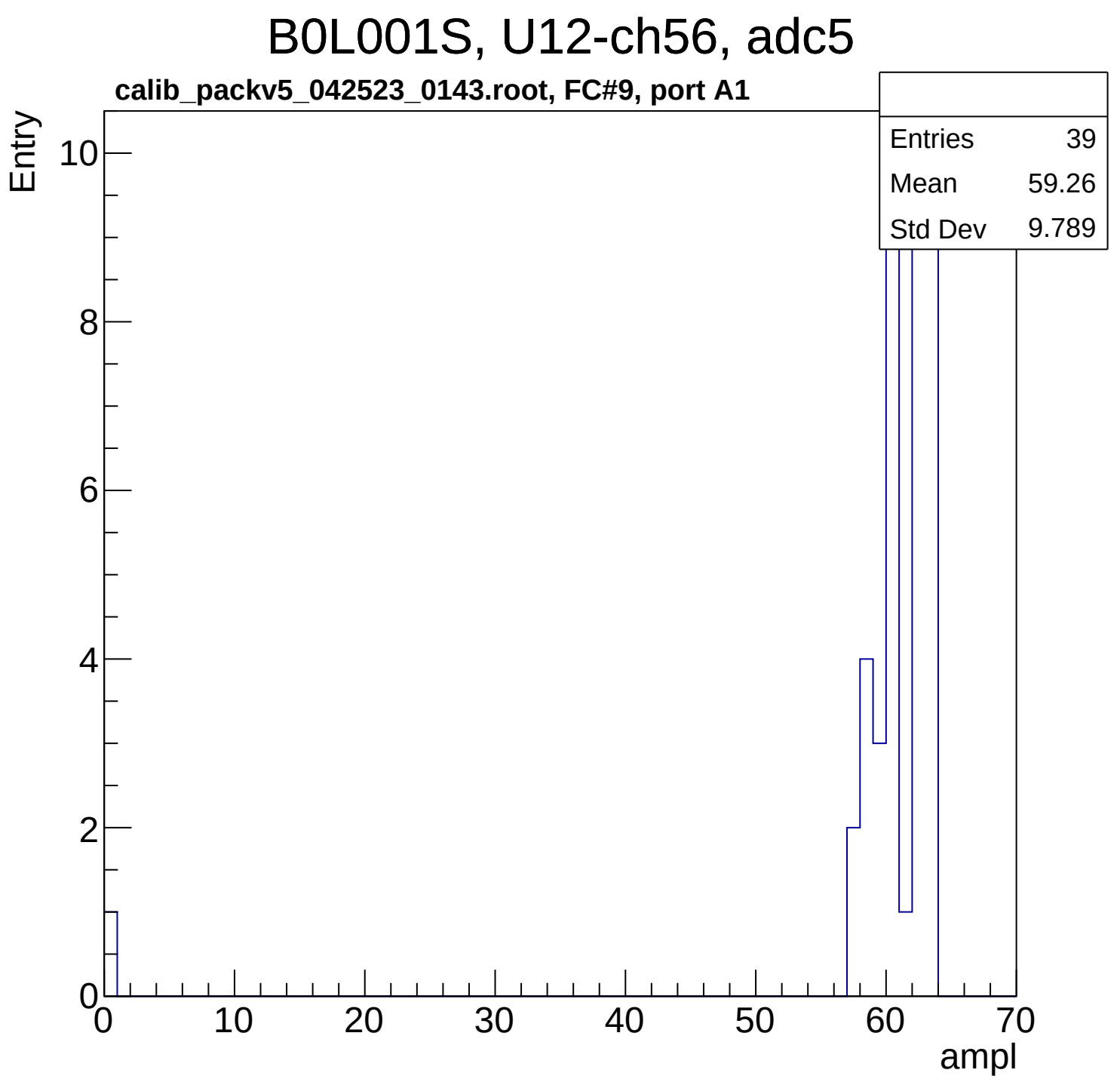
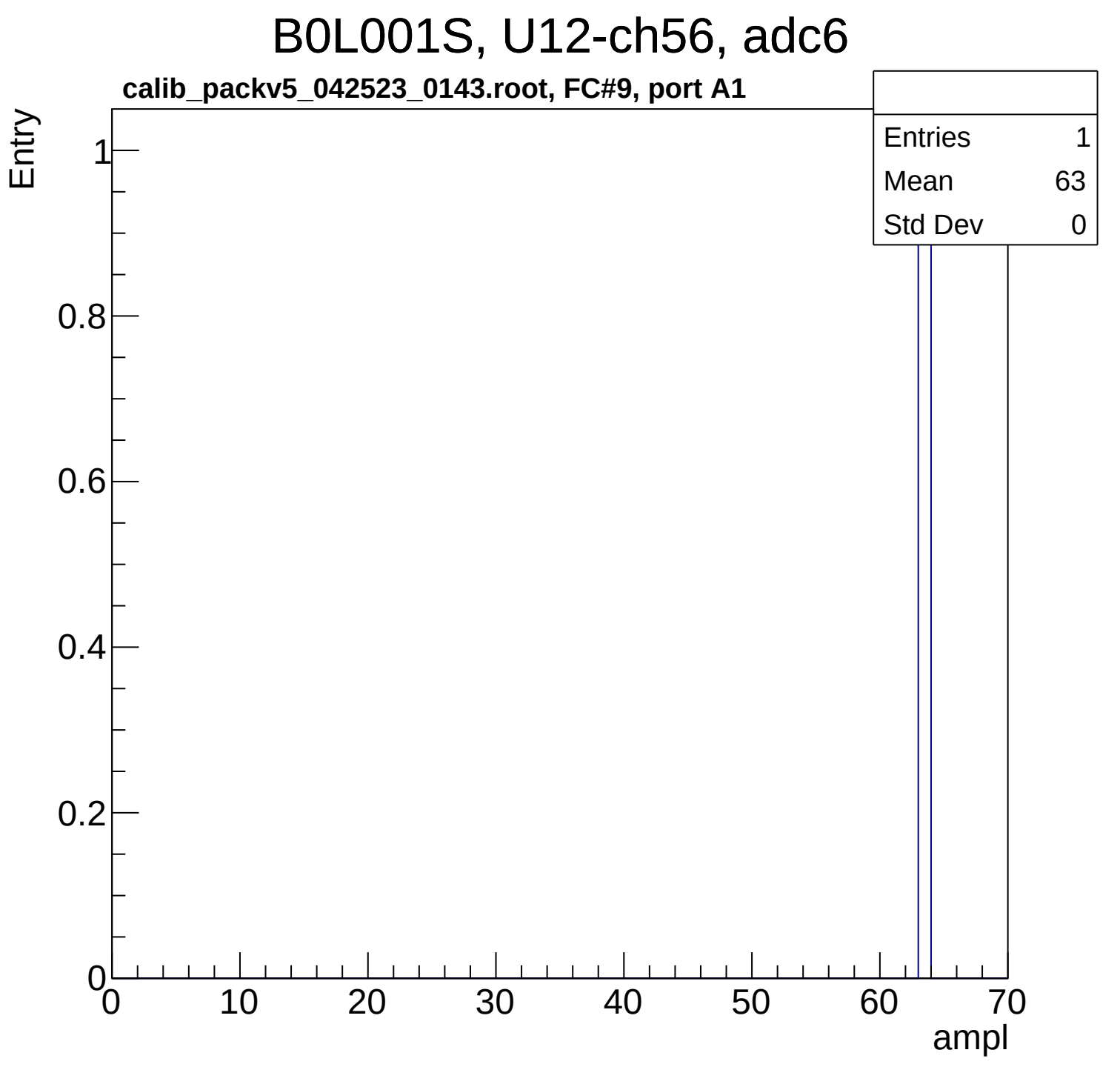

B0L001S, U12-ch56, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 39
Mean 59.26
Std Dev 9.789
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch56, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 63
Std Dev 0
Entry
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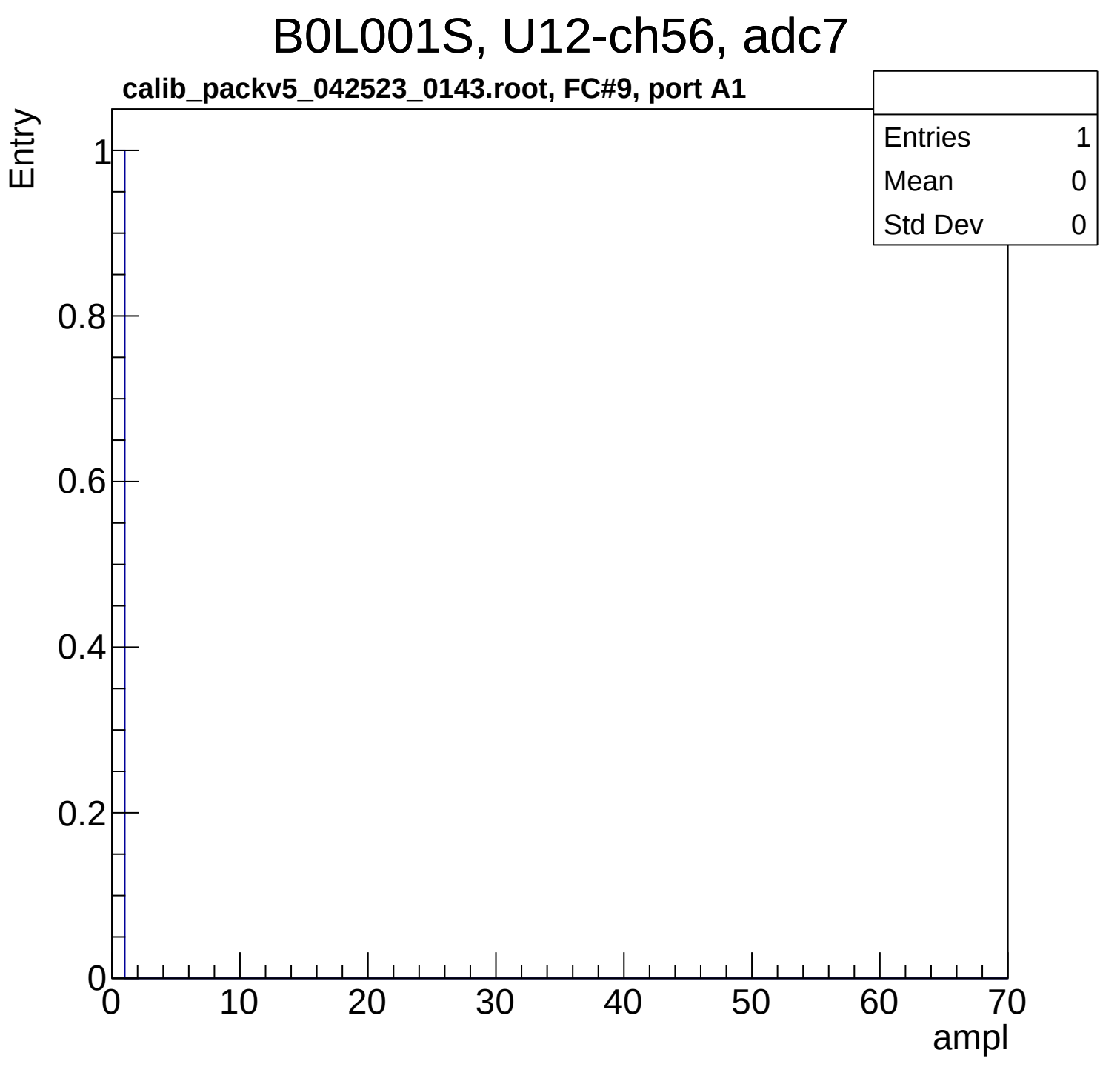
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch56, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 0
Std Dev 0
Entry
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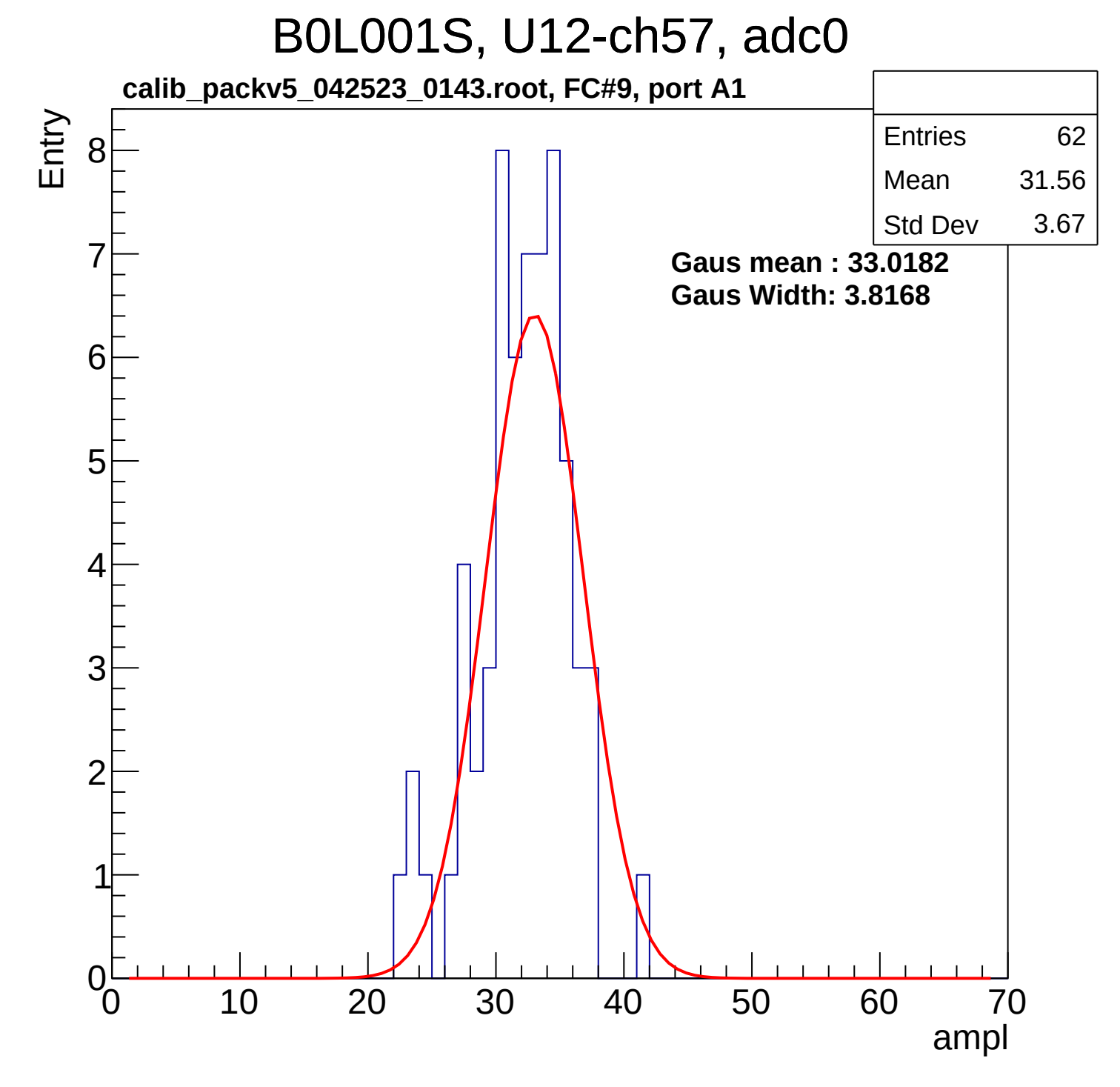
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch57, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 62
Mean 31.56
Std Dev 3.67
Gaus mean : 33.0182
Gaus Width: 3.8168
Entry
ampl
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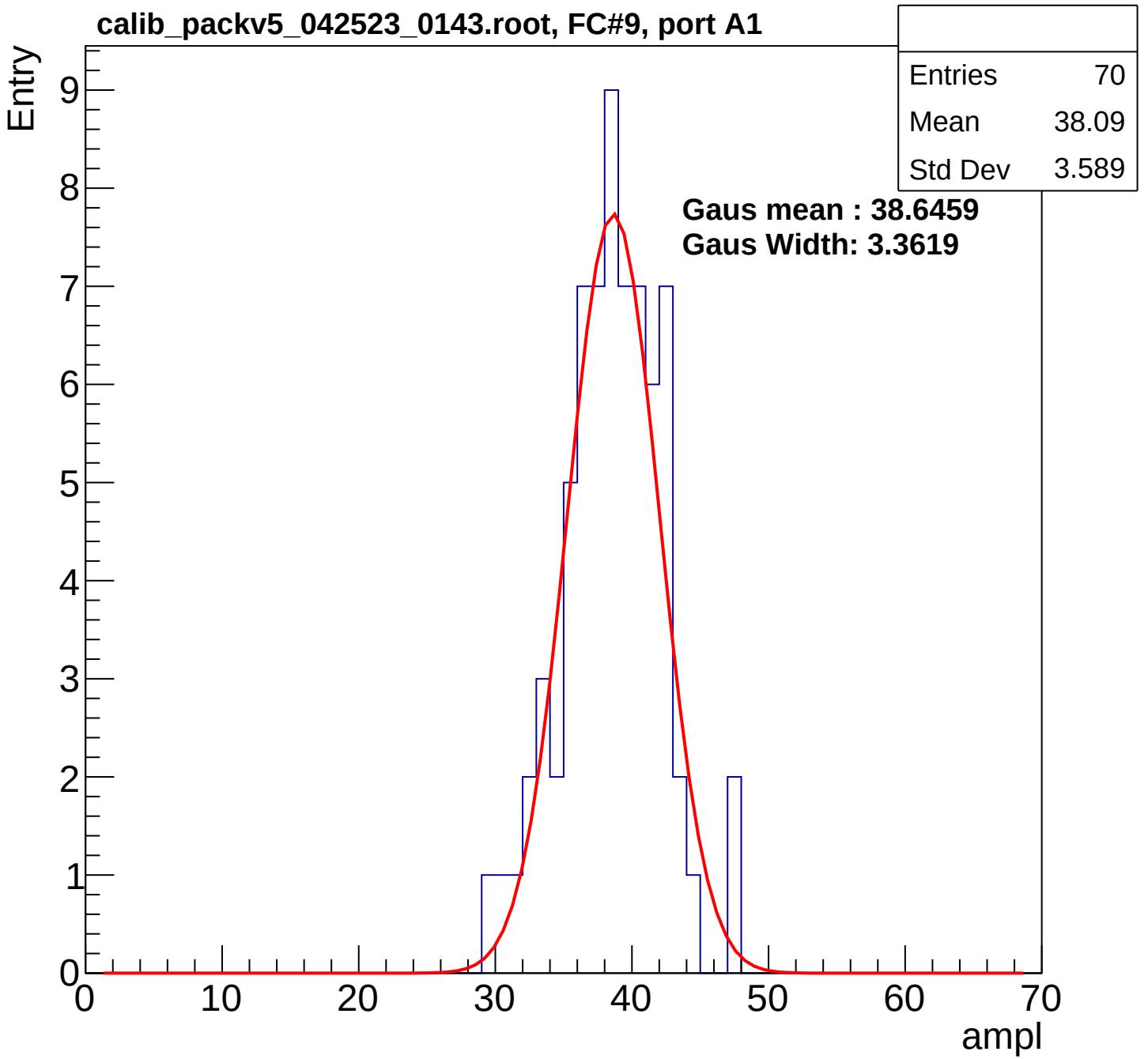
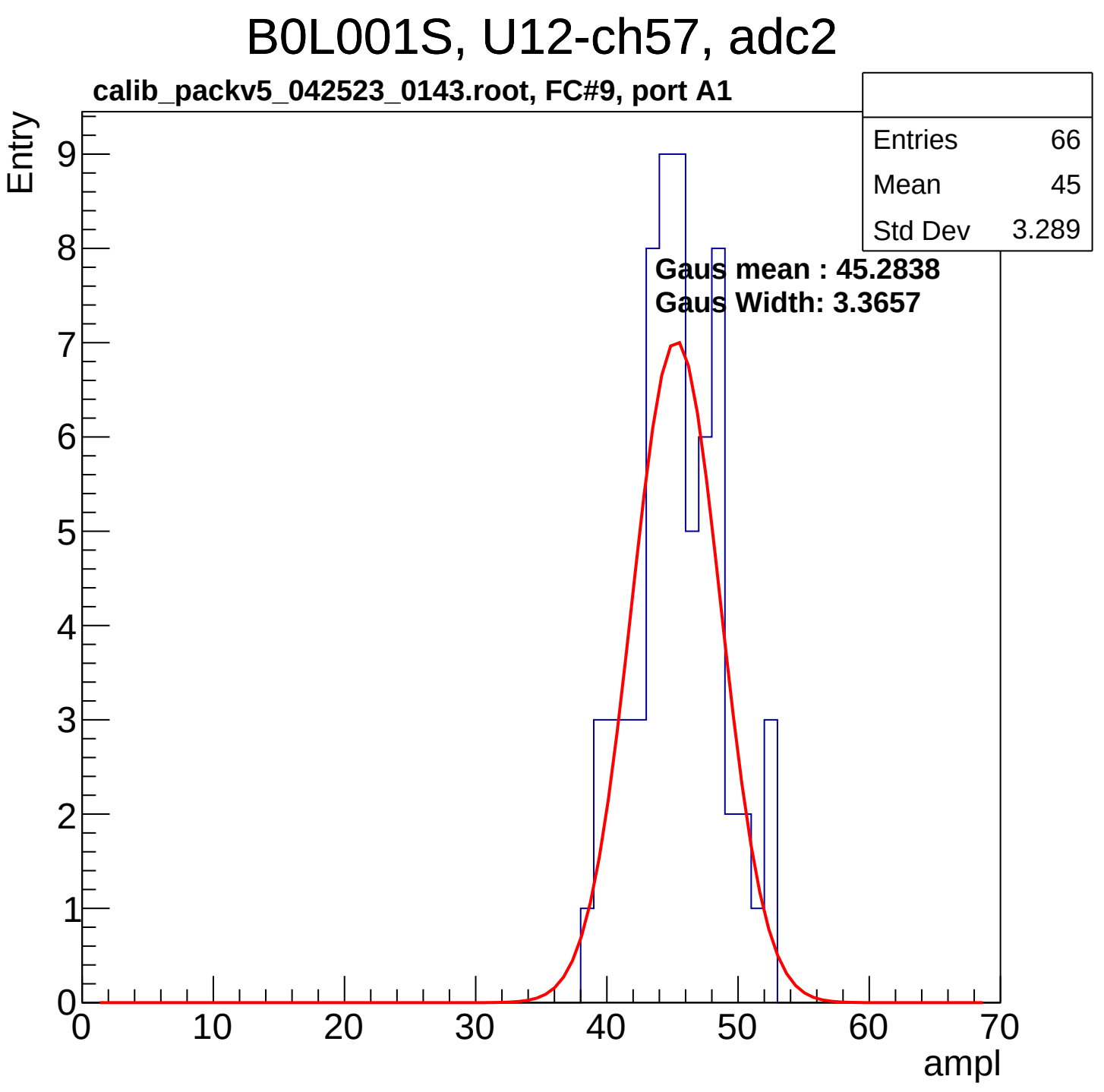
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch57, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 70
Mean 38.09
Std Dev 3.589
Gaus mean : 38.6459
Gaus Width: 3.3619
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch57, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 66
Mean 45
Std Dev 3.289
Gaus mean : 45.2838
Gaus Width: 3.3657
Entry
ampl
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2
3
4
5
6
7
8
9
0
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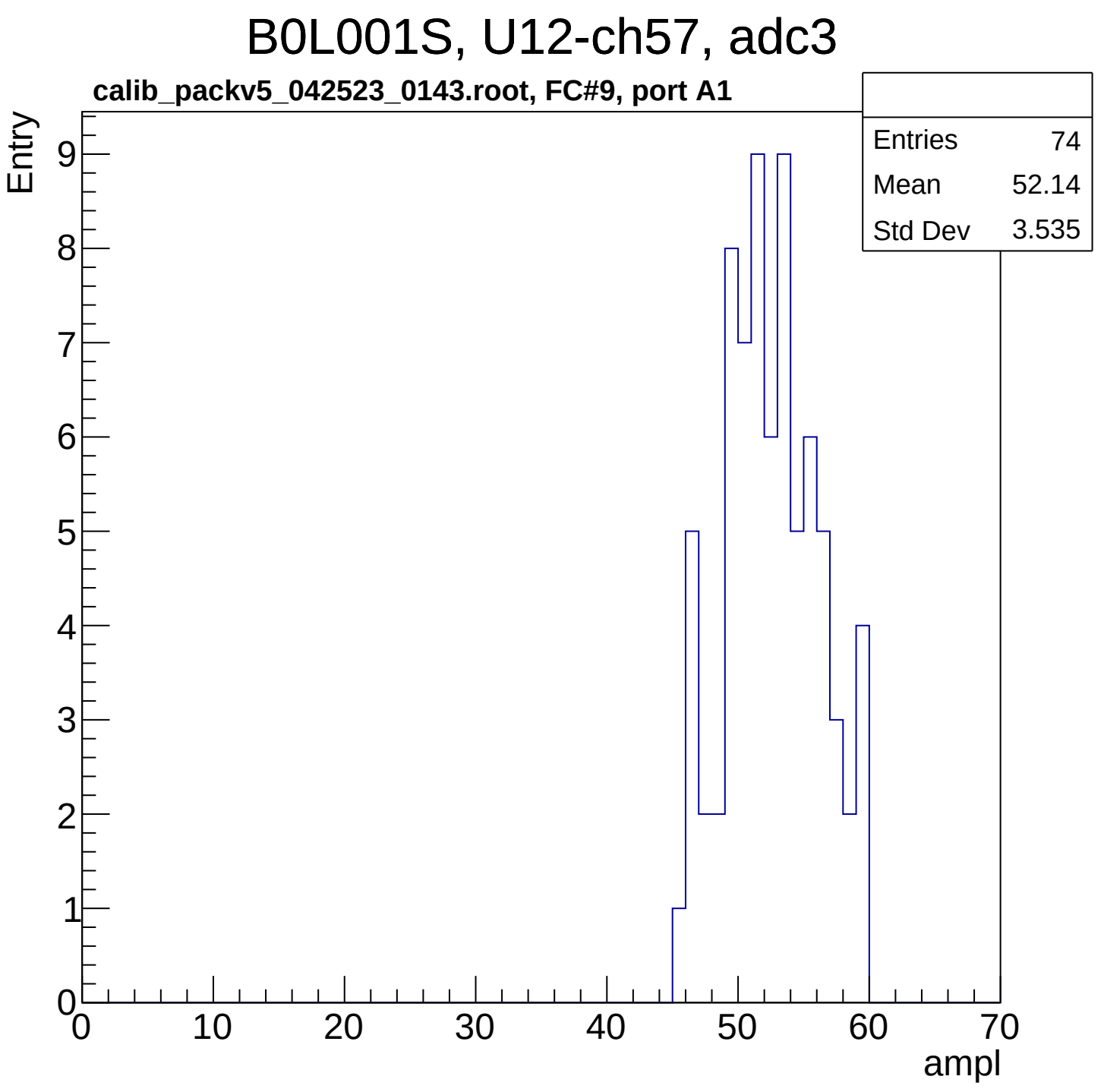
B0L001S, U12-ch57, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 74
Mean 52.14
Std Dev 3.535
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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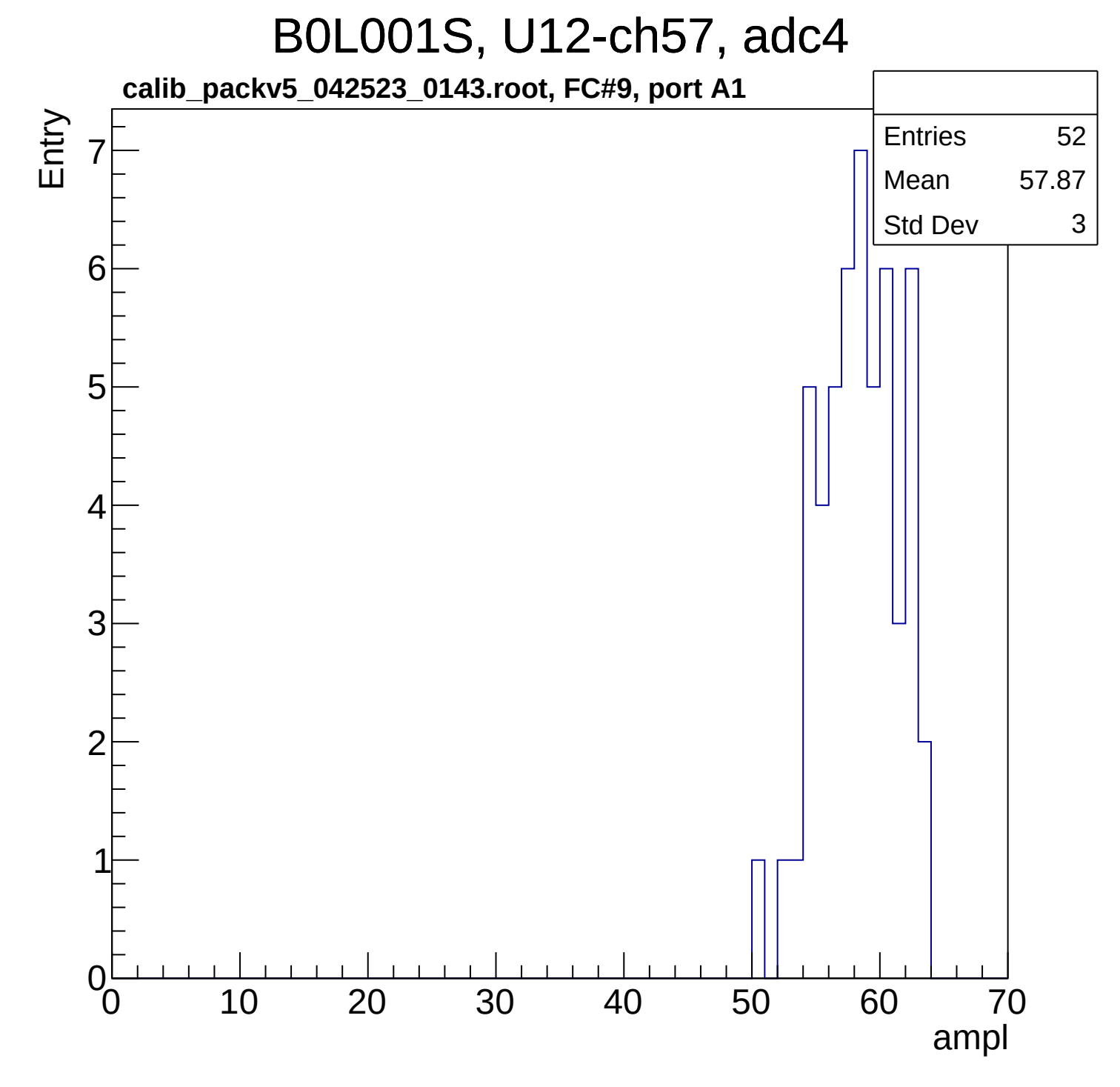
B0L001S, U12-ch57, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 52
Mean 57.87
Std Dev 3
Entry
ampl
0
1
2
3
4
5
6
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0
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40
50
60
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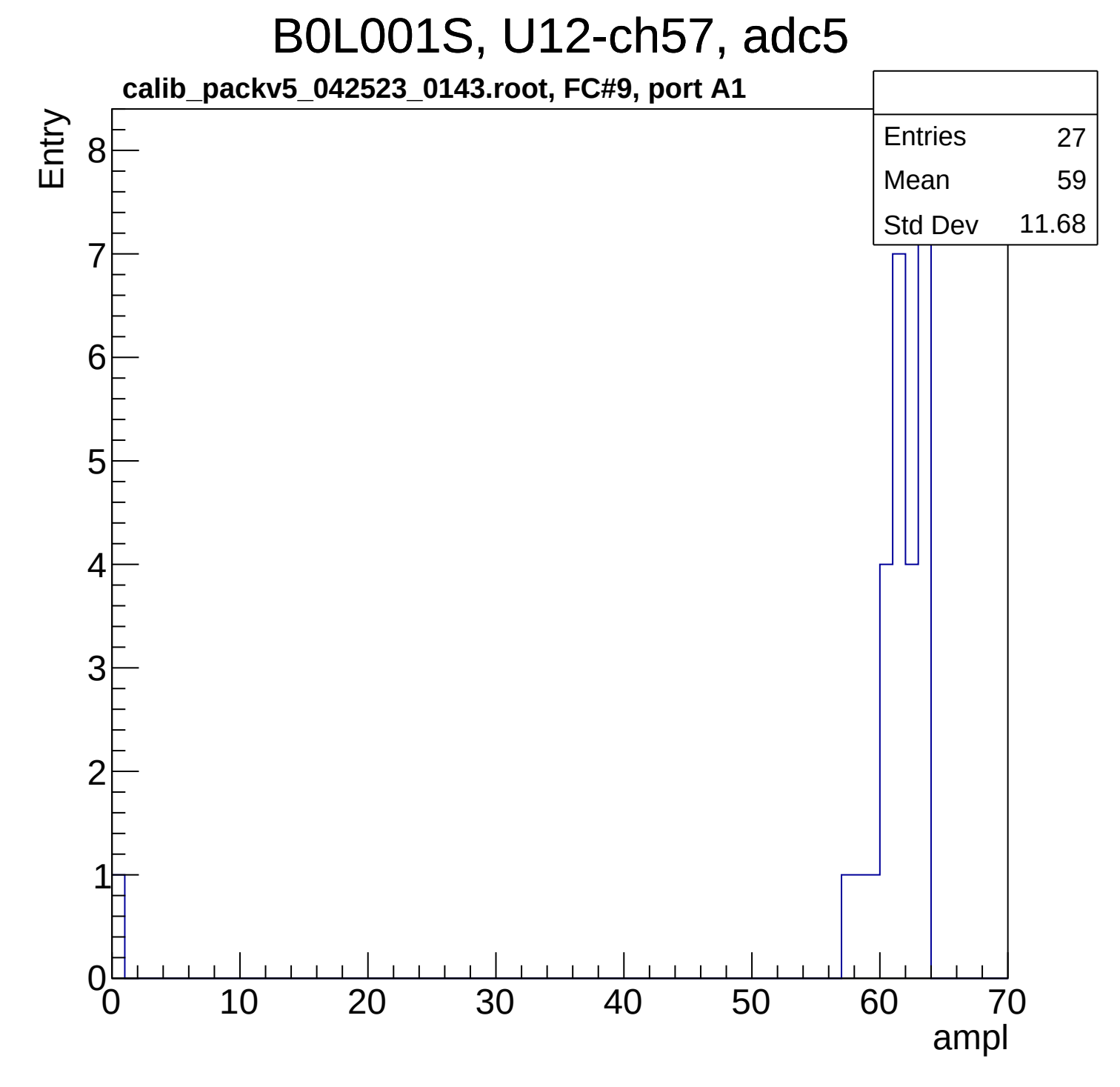
B0L001S, U12-ch57, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 27
Mean 59
Std Dev 11.68
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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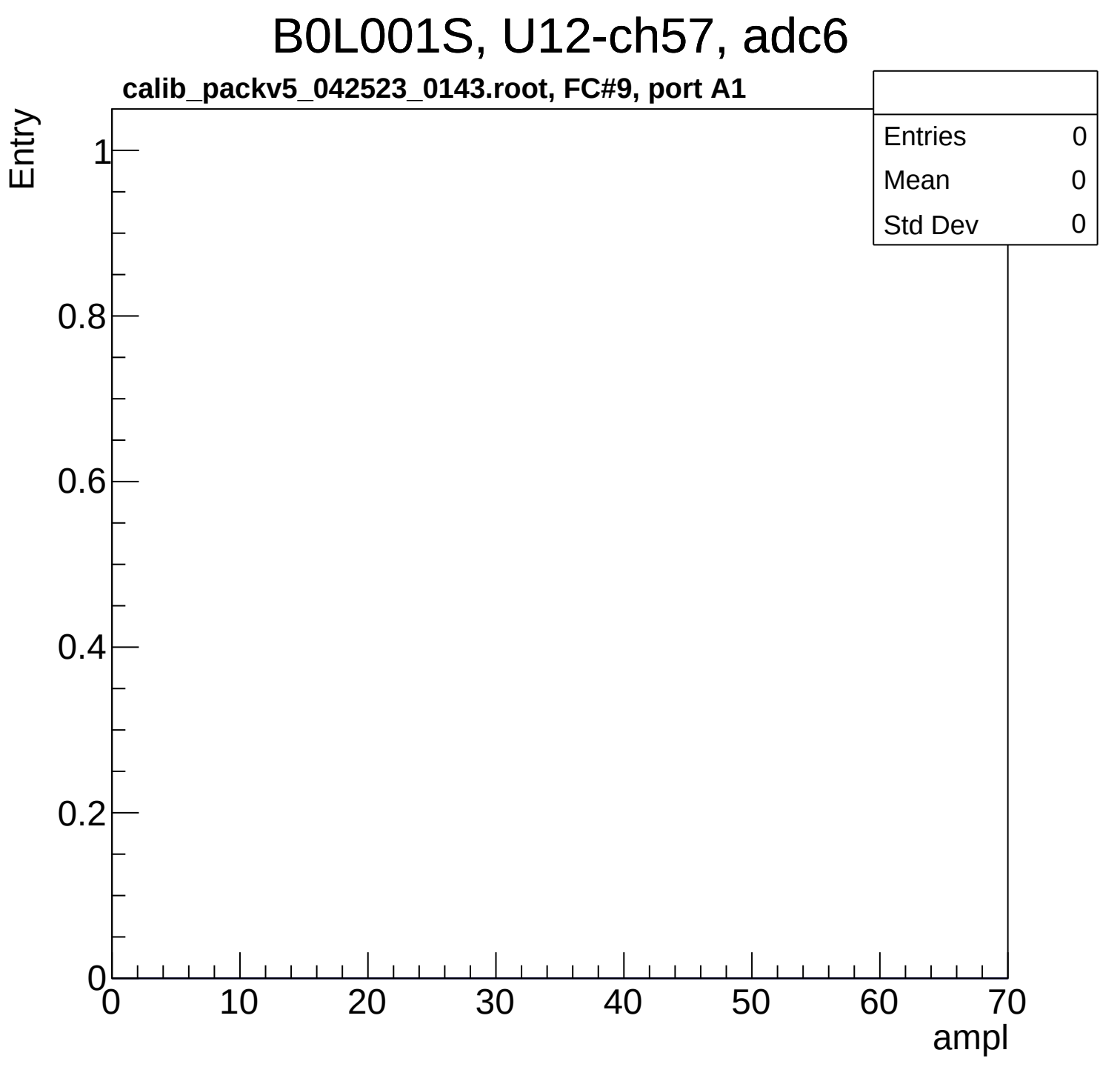
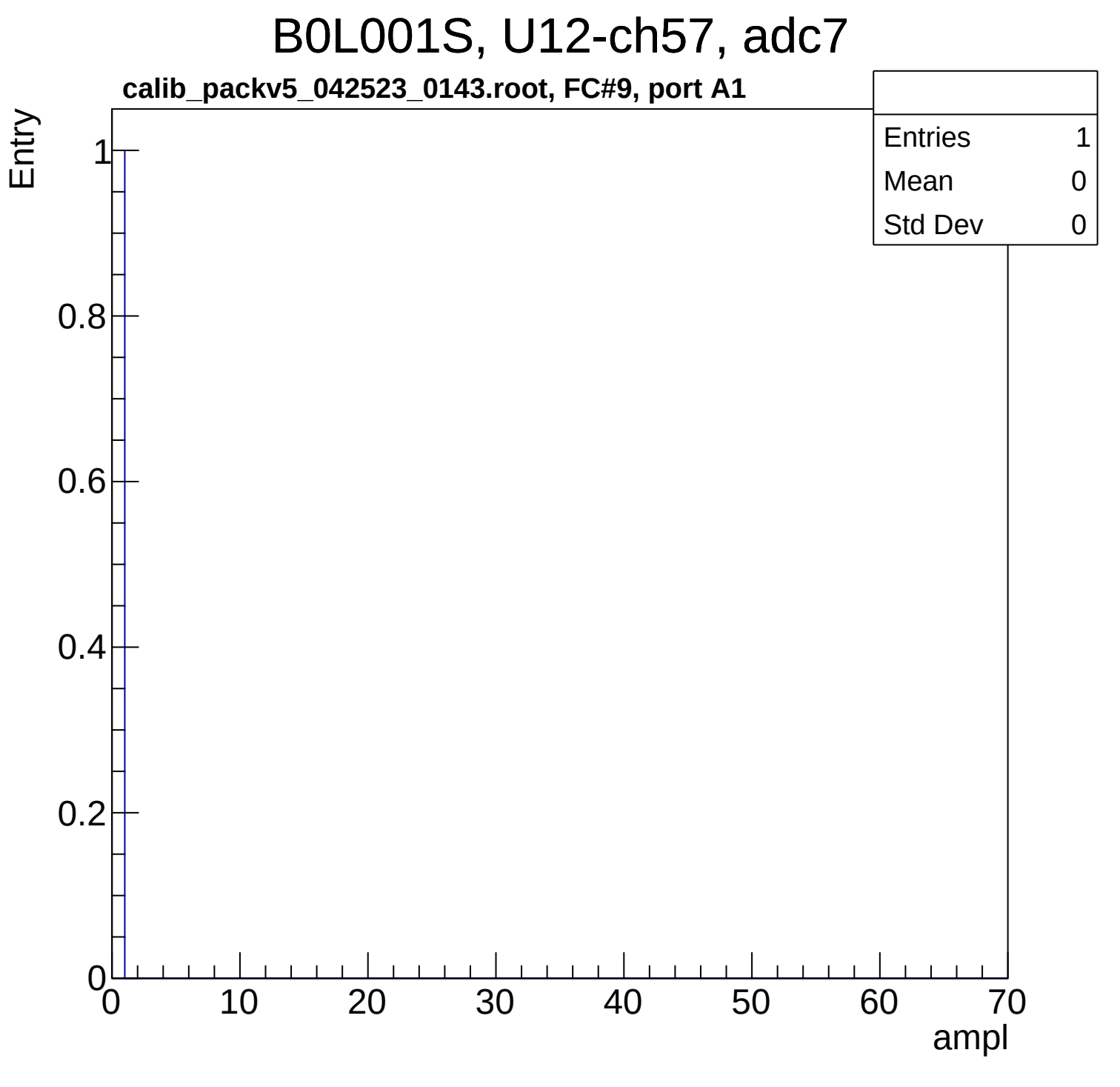
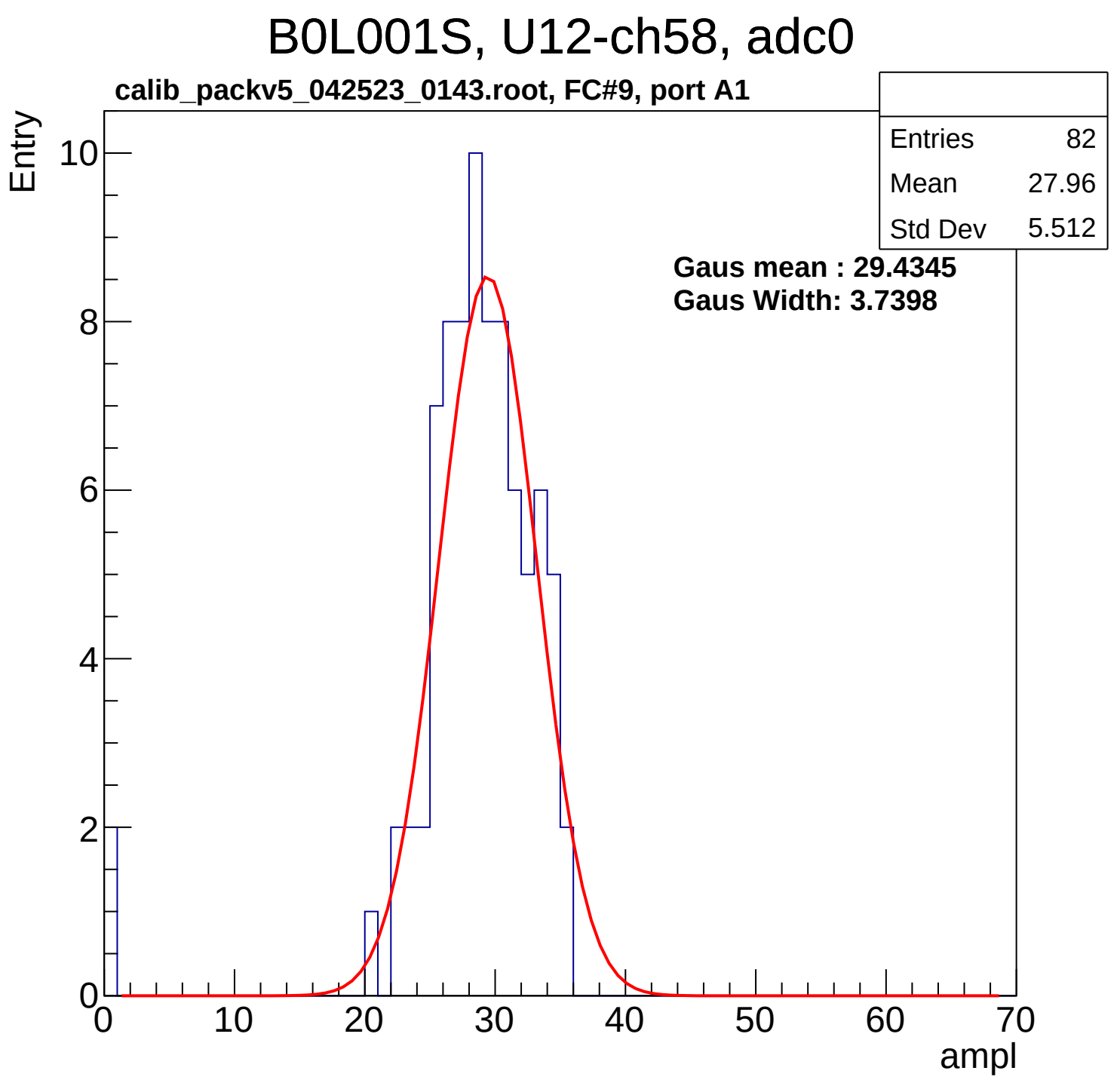
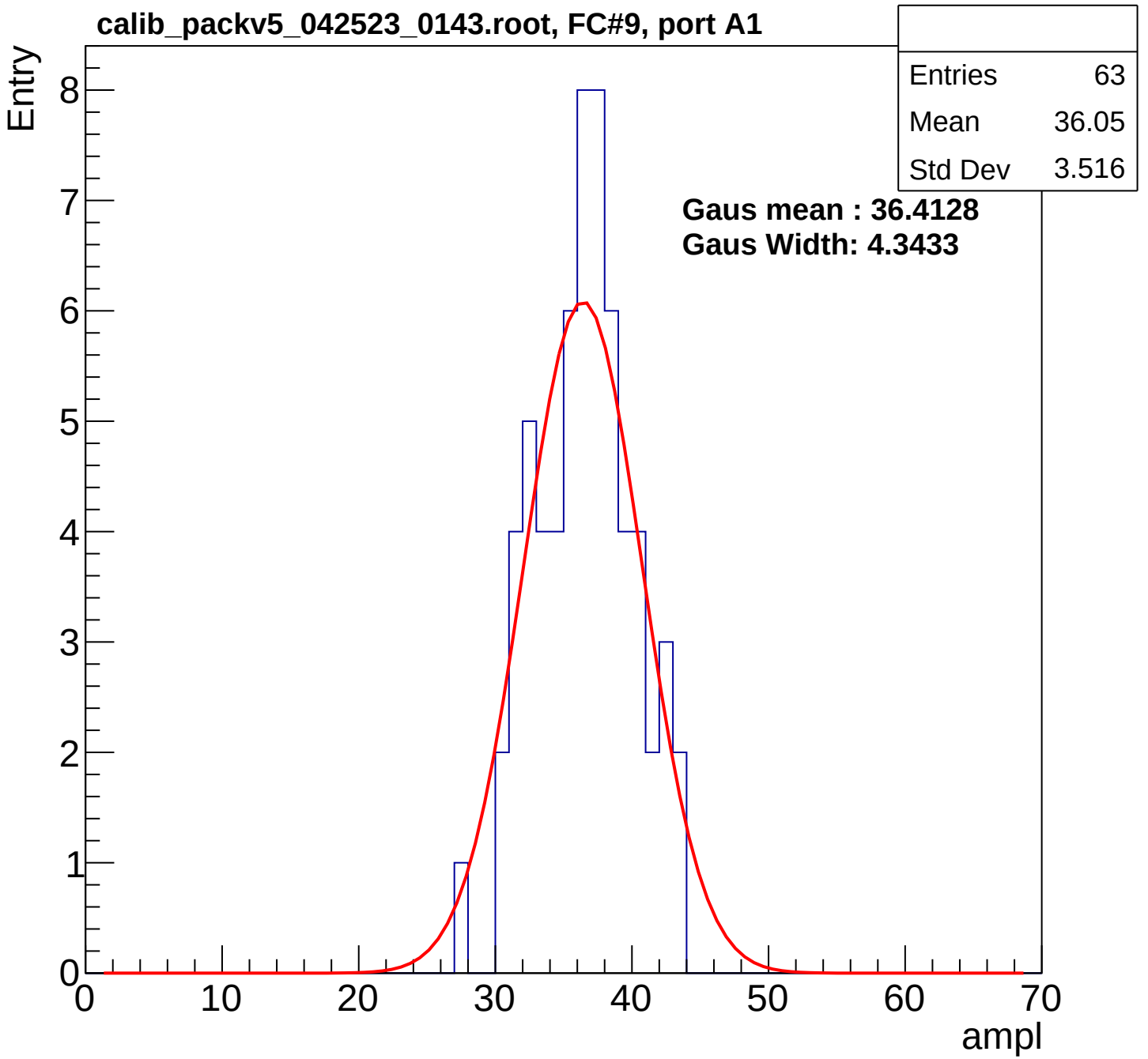

B0L001S, U12-ch57, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch57, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch58, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 82
Mean 27.96
Std Dev 5.512
Gaus mean : 29.4345
Gaus Width: 3.7398
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch58, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 63
Mean 36.05
Std Dev 3.516
Gaus mean : 36.4128
Gaus Width: 4.3433
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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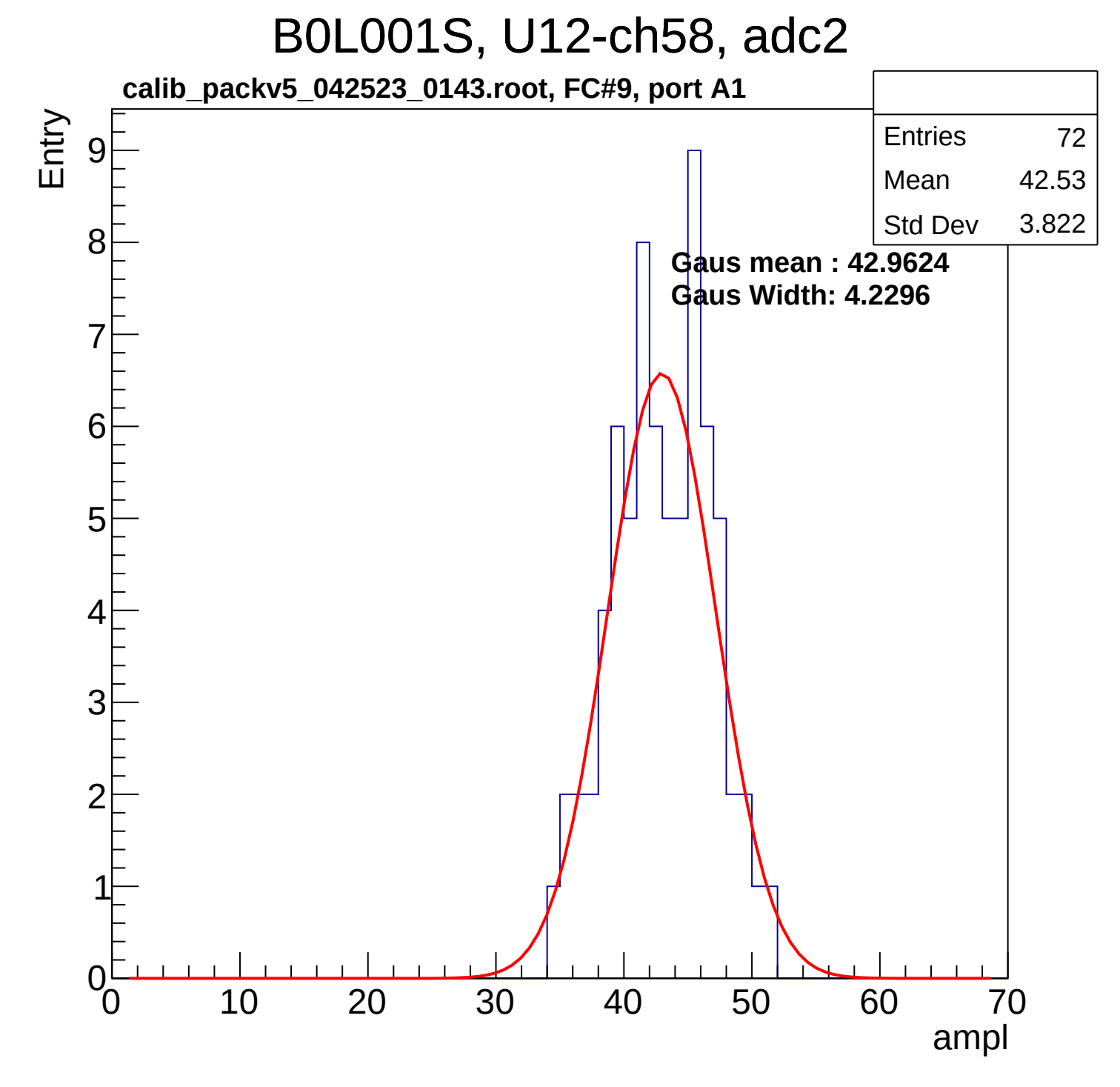
B0L001S, U12-ch58, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 72
Mean 42.53
Std Dev 3.822
Gaus mean : 42.9624
Gaus Width: 4.2296
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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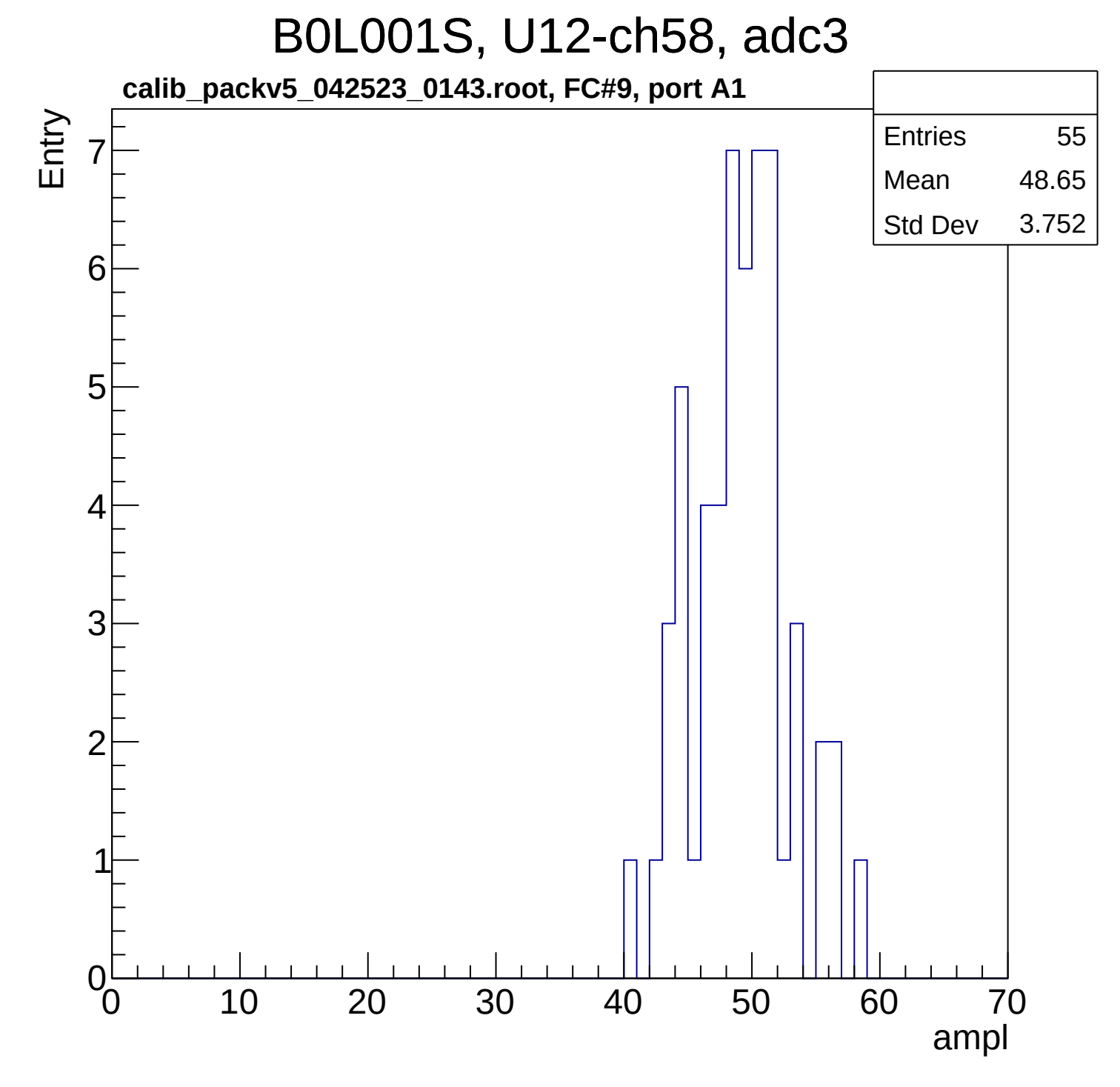
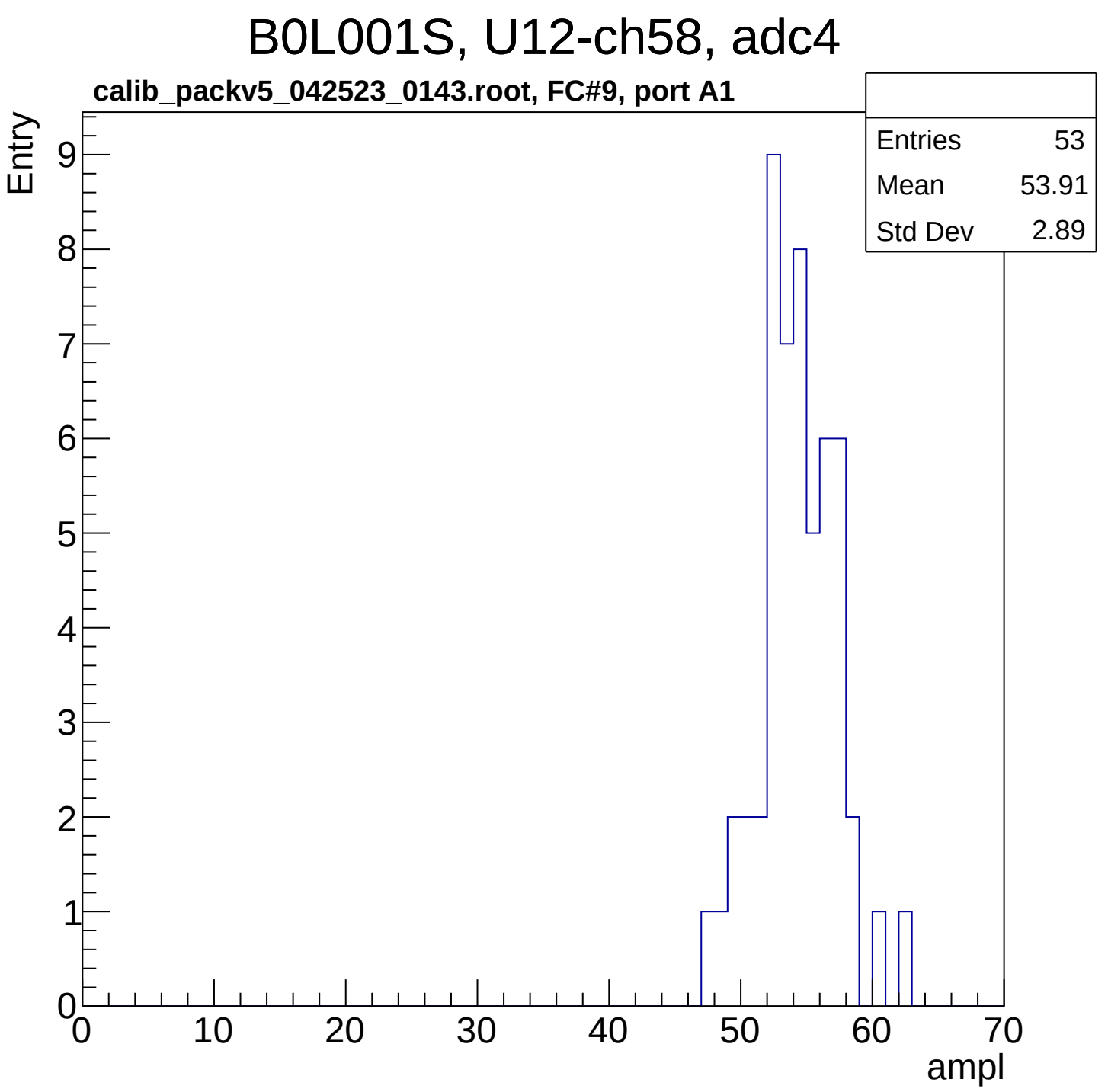
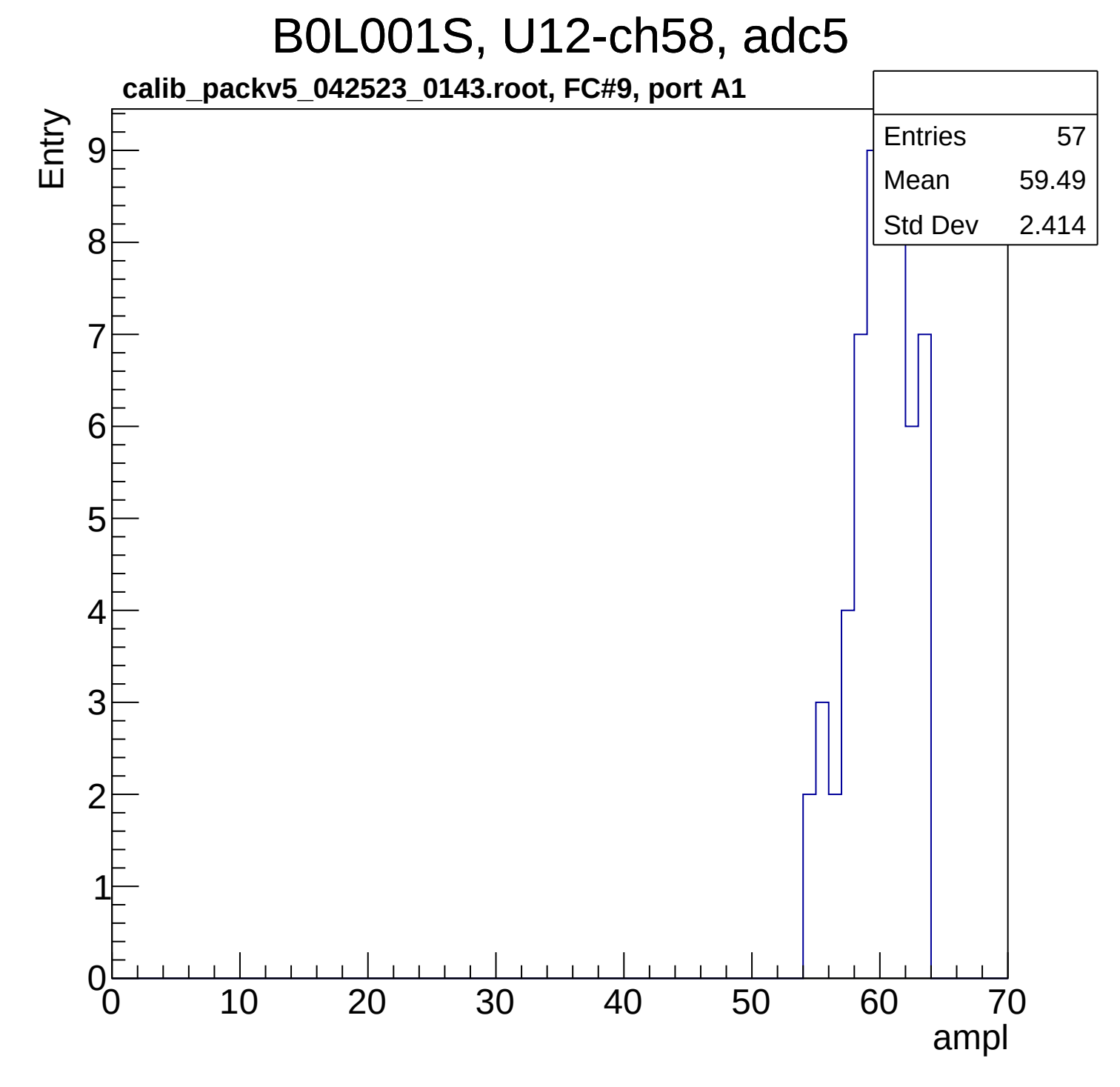

B0L001S, U12-ch58, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 55
Mean 48.65
Std Dev 3.752
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B0L001S, U12-ch58, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 53
Mean 53.91
Std Dev 2.89
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch58, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 57
Mean 59.49
Std Dev 2.414
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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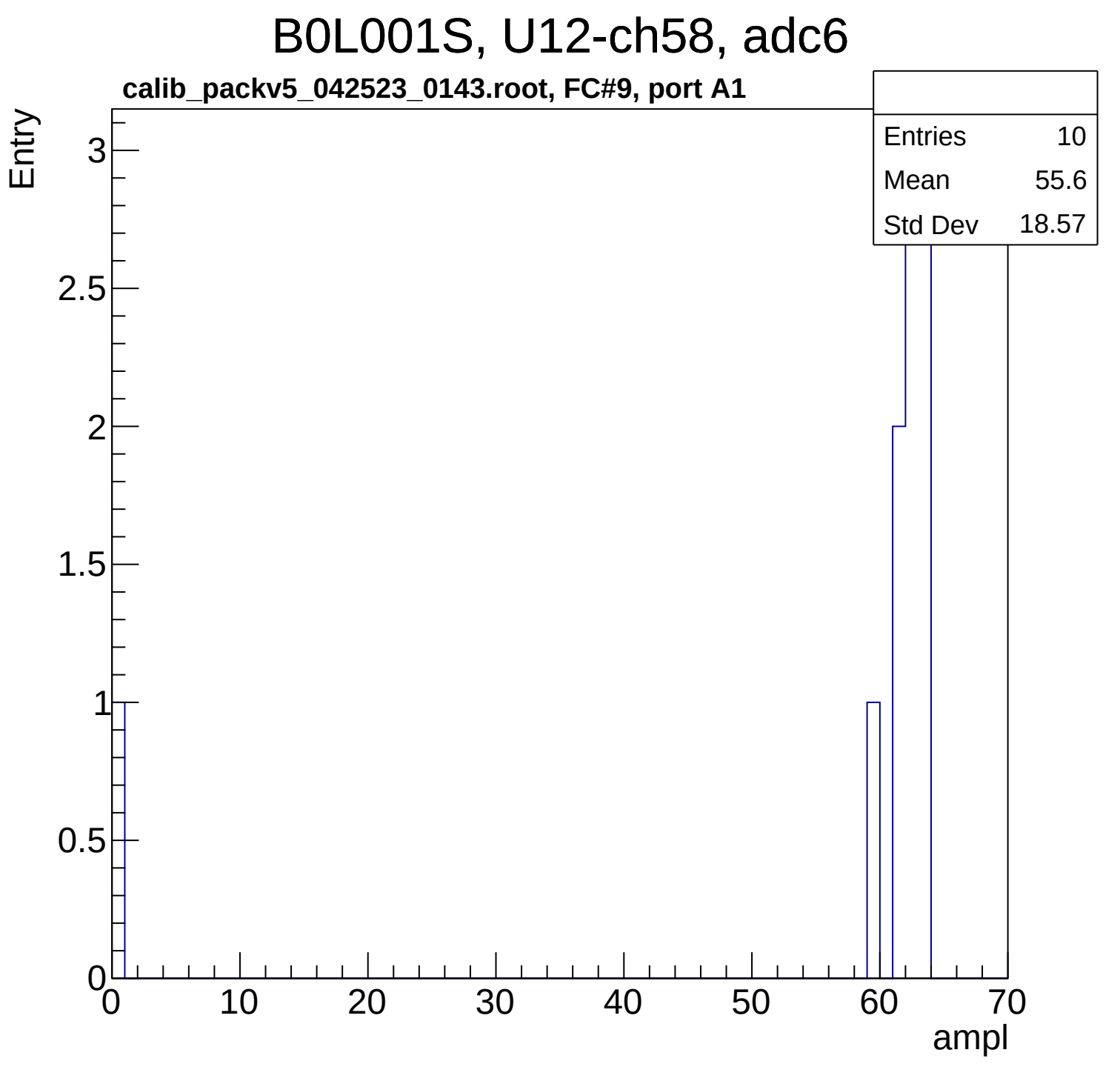
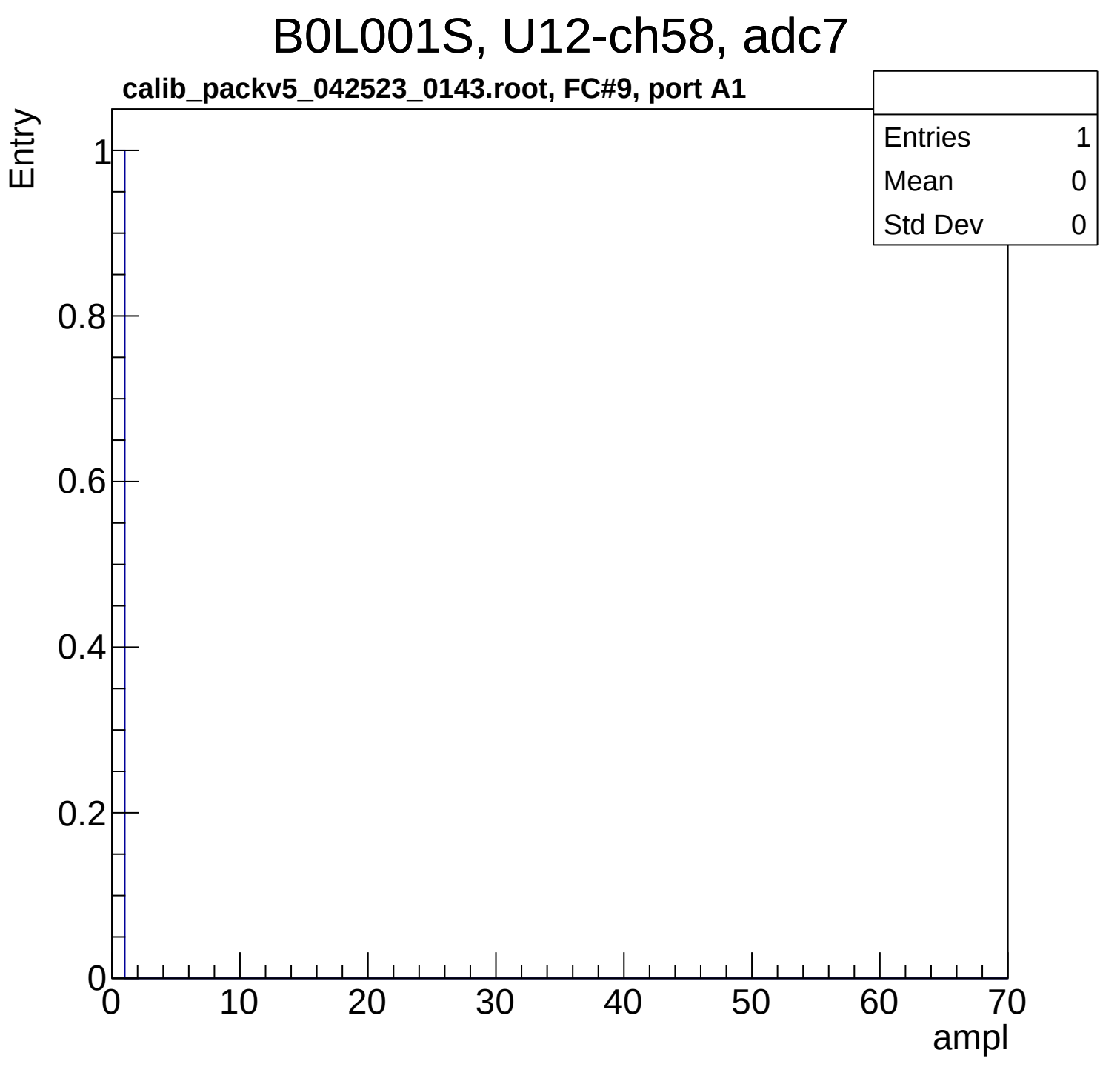
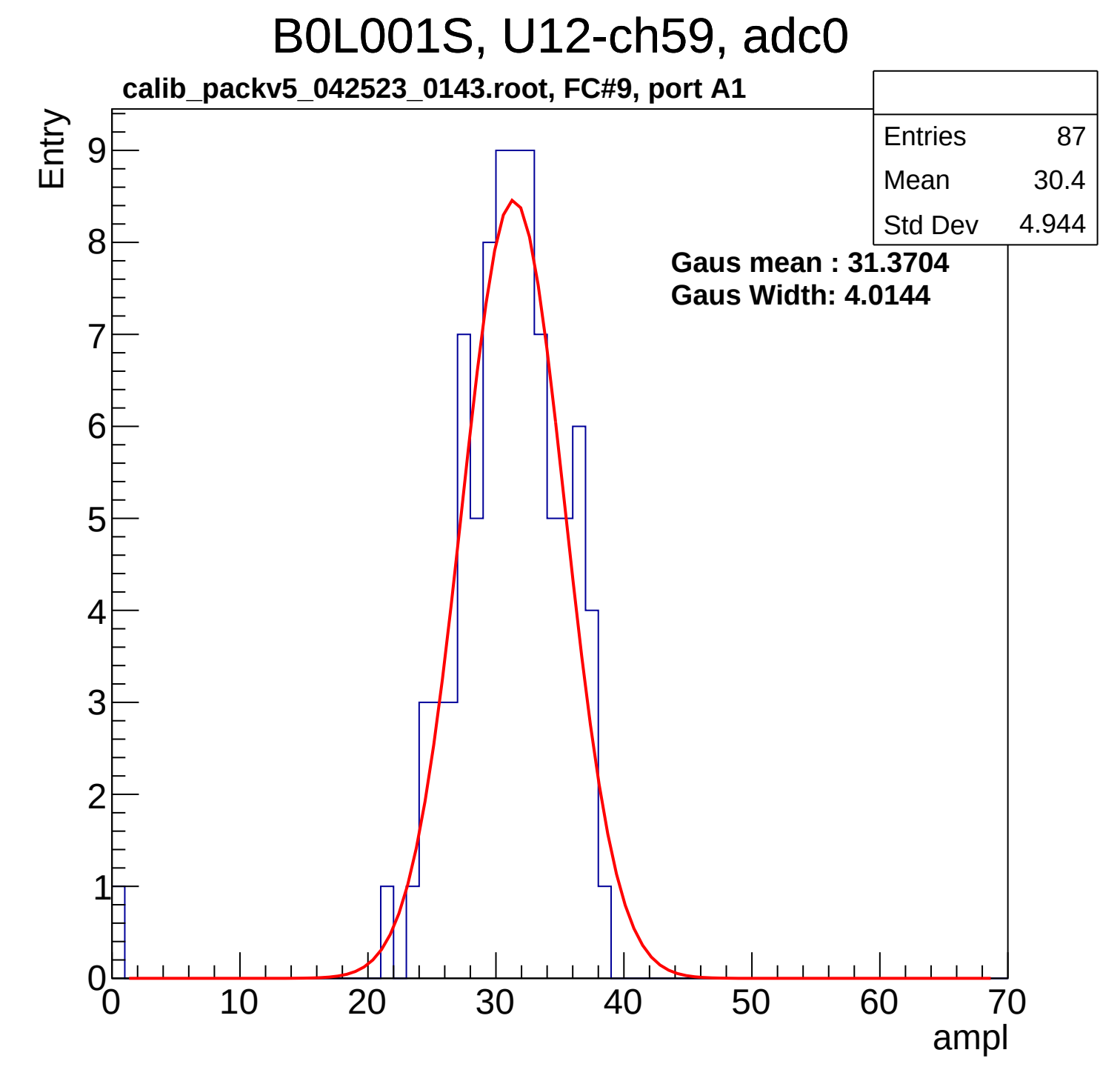
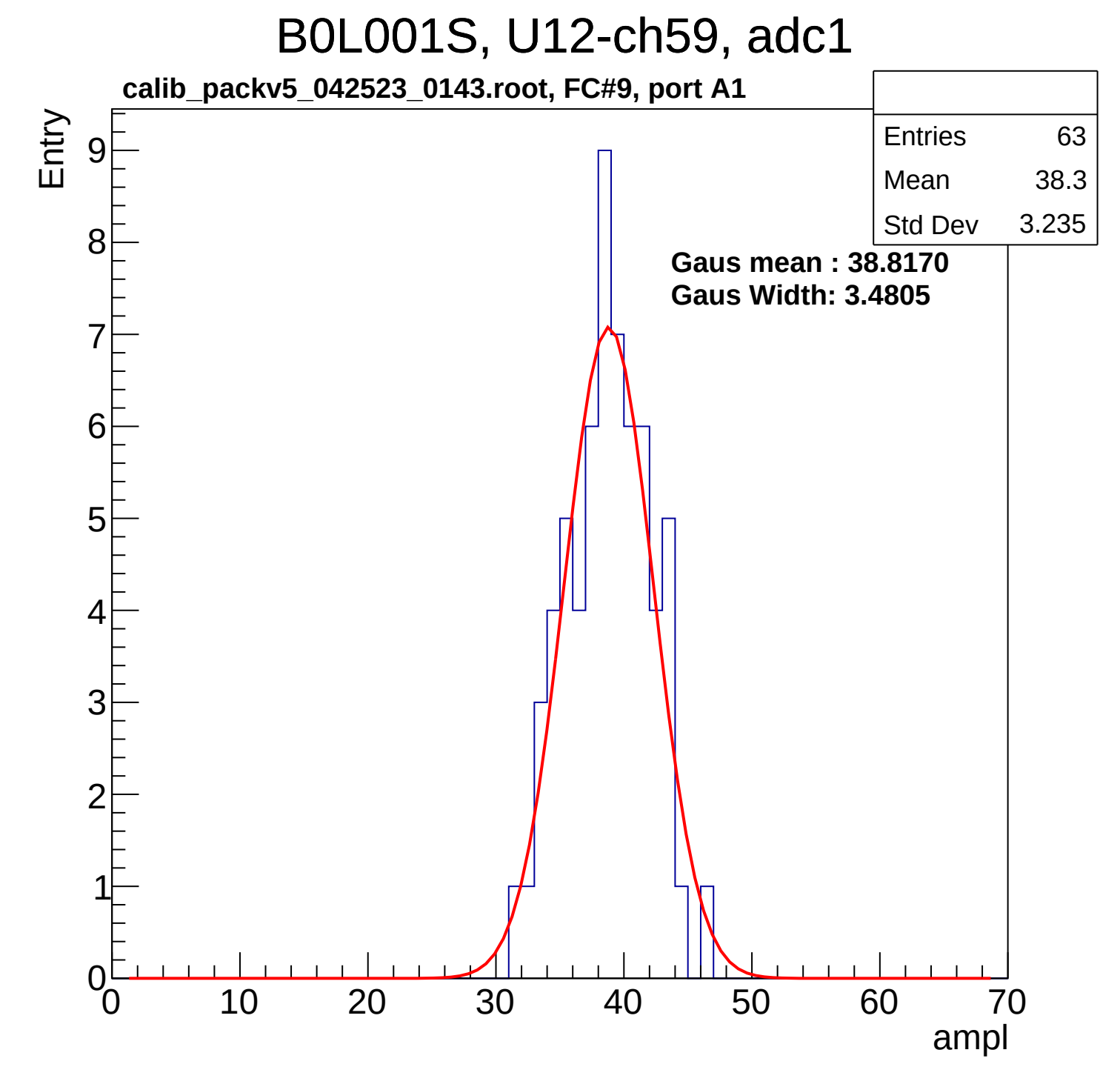
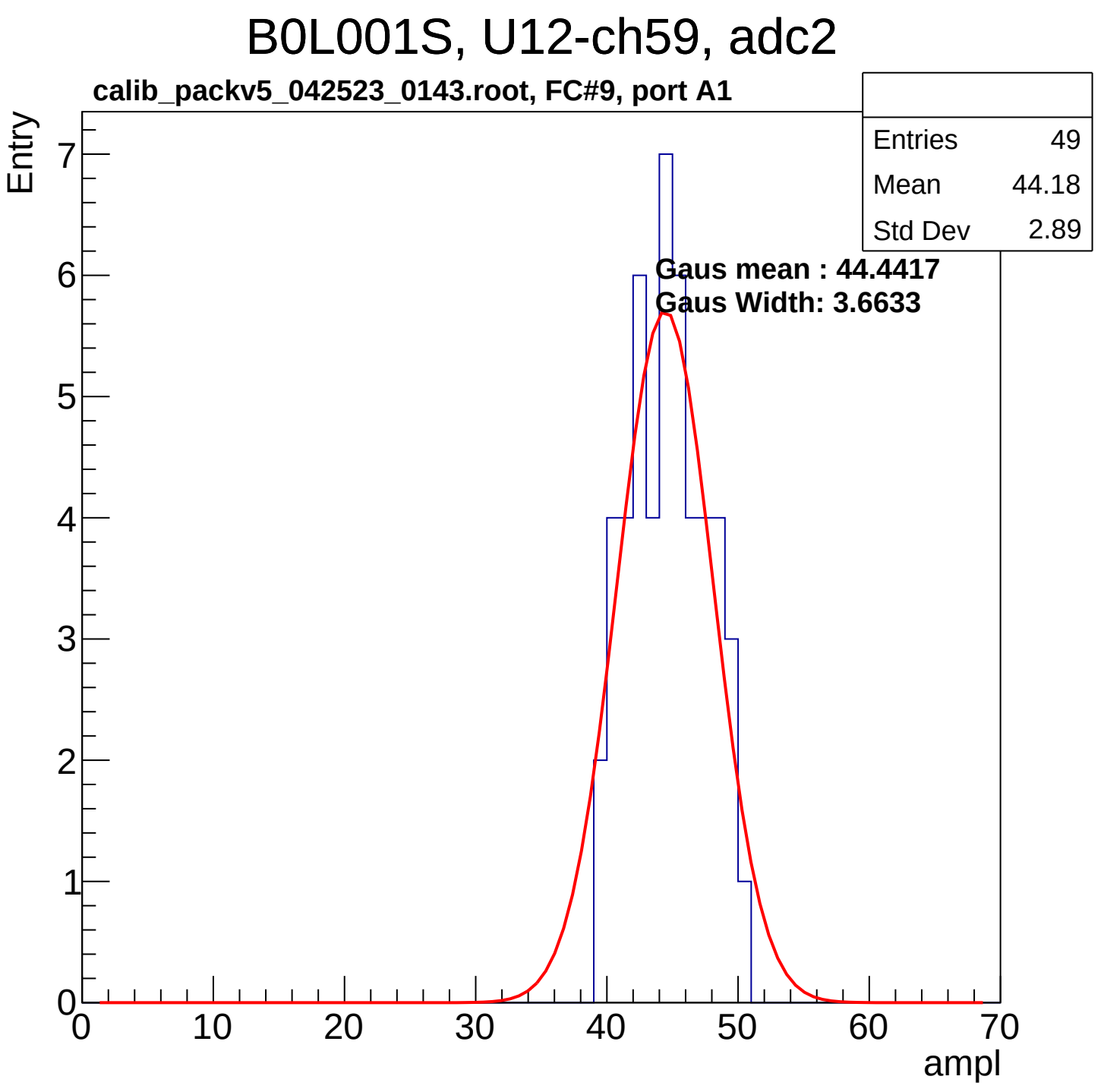

B0L001S, U12-ch58, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 10
Mean 55.6
Std Dev 18.57
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B0L001S, U12-ch58, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch59, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 87
Mean 30.4
Std Dev 4.944
Gaus mean : 31.3704
Gaus Width: 4.0144
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch59, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 63
Mean 38.3
Std Dev 3.235
Gaus mean : 38.8170
Gaus Width: 3.4805
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch59, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 49
Mean 44.18
Std Dev 2.89
Gaus mean : 44.4417
Gaus Width: 3.6633
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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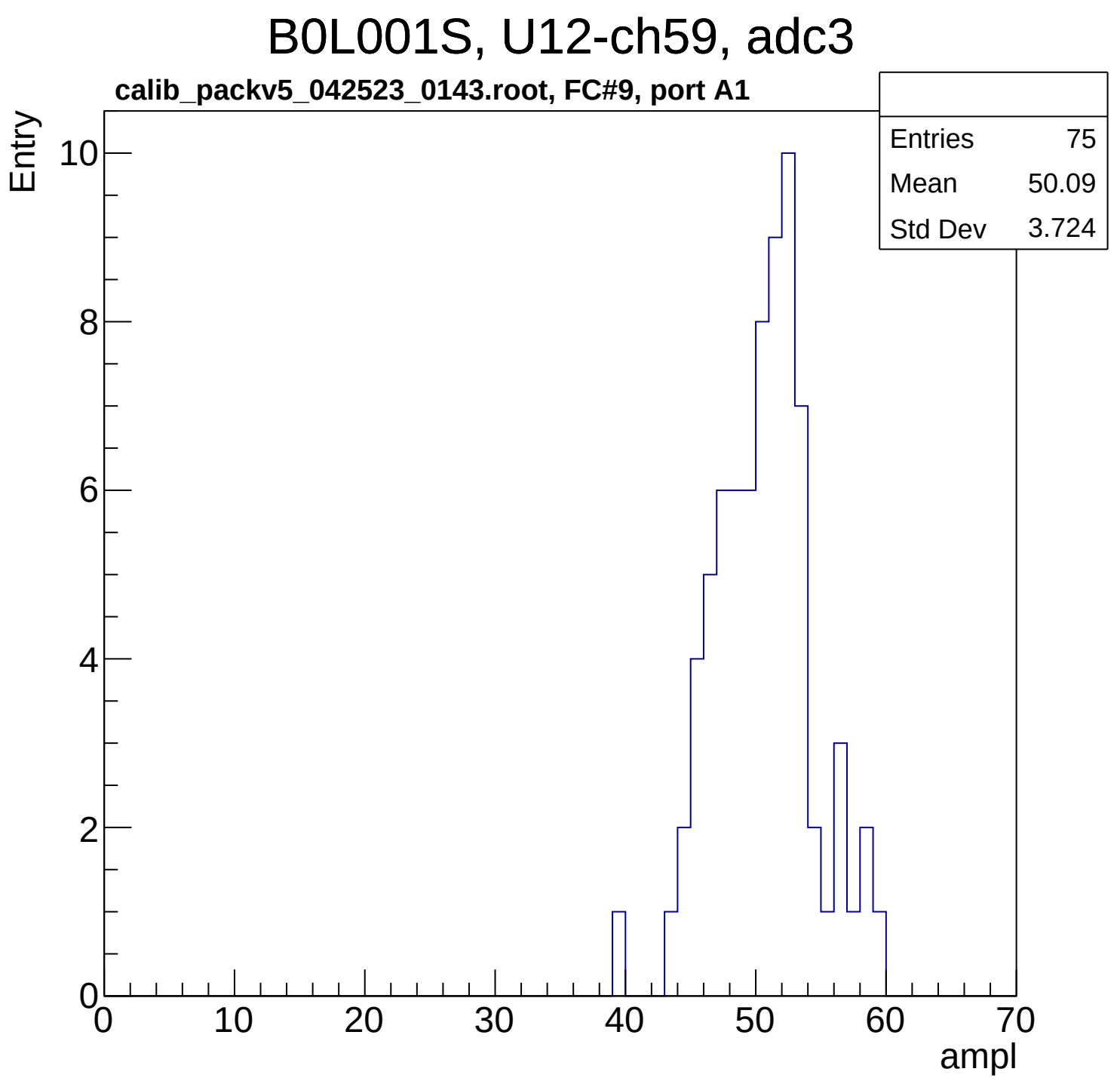
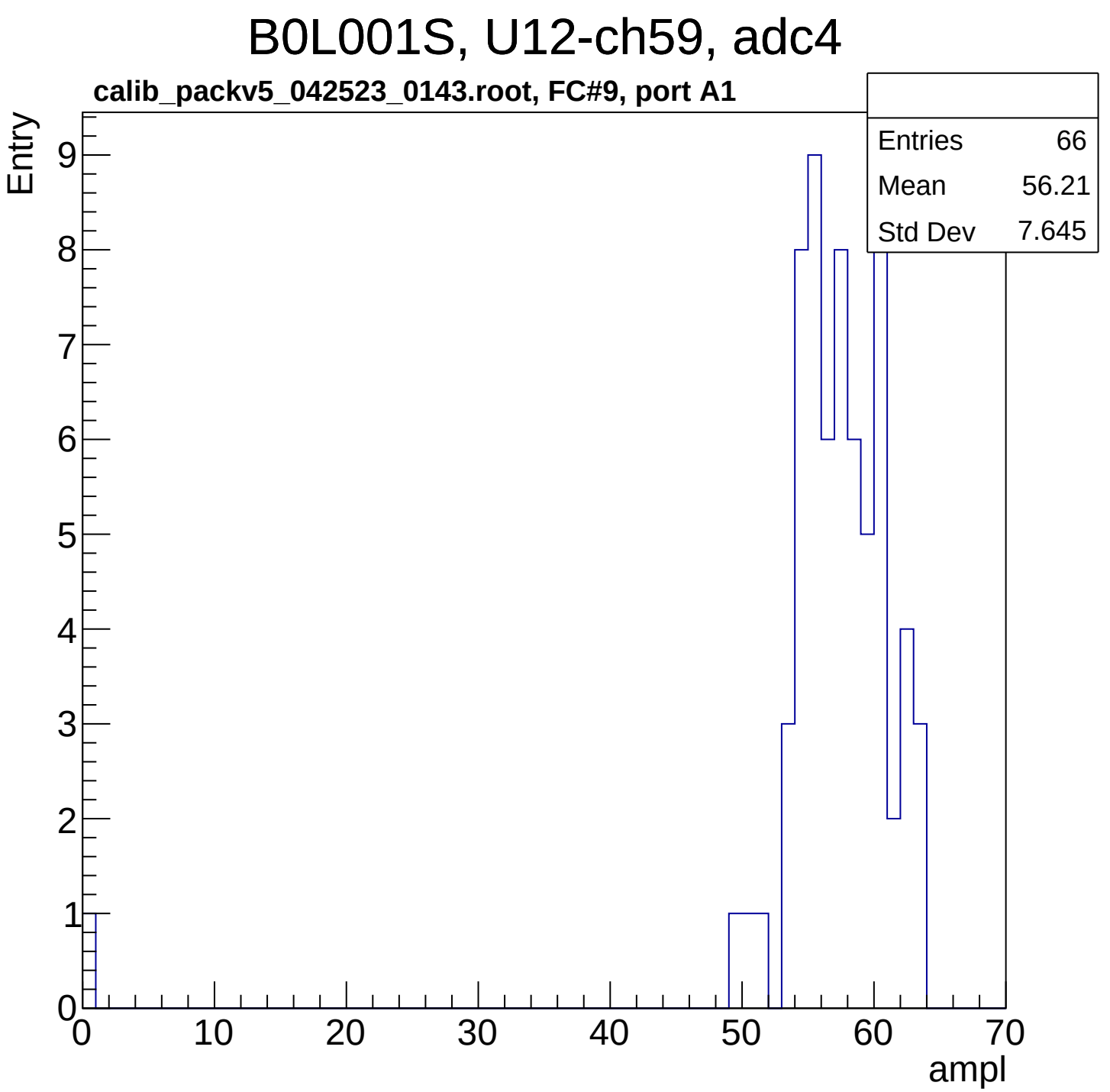
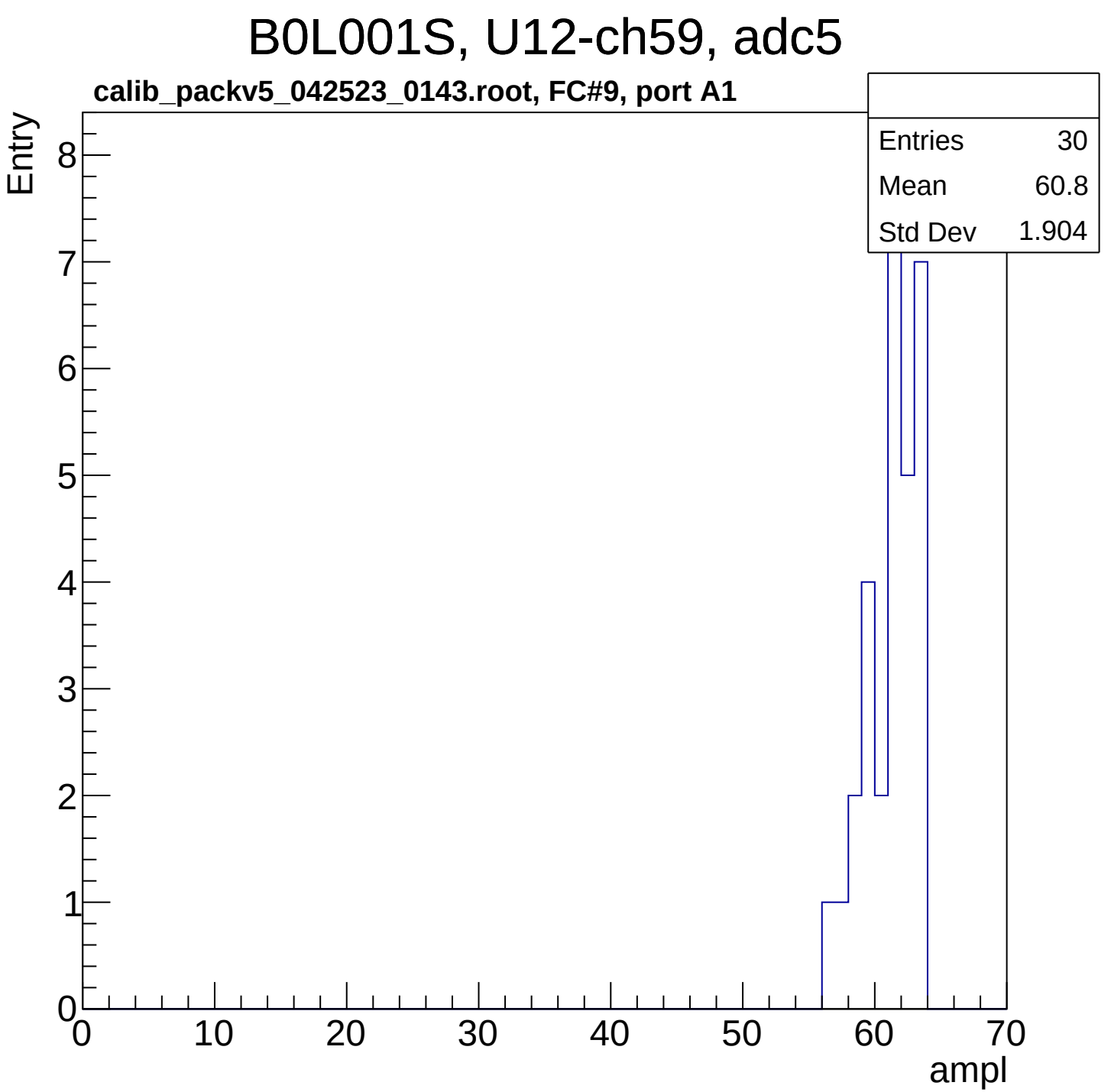
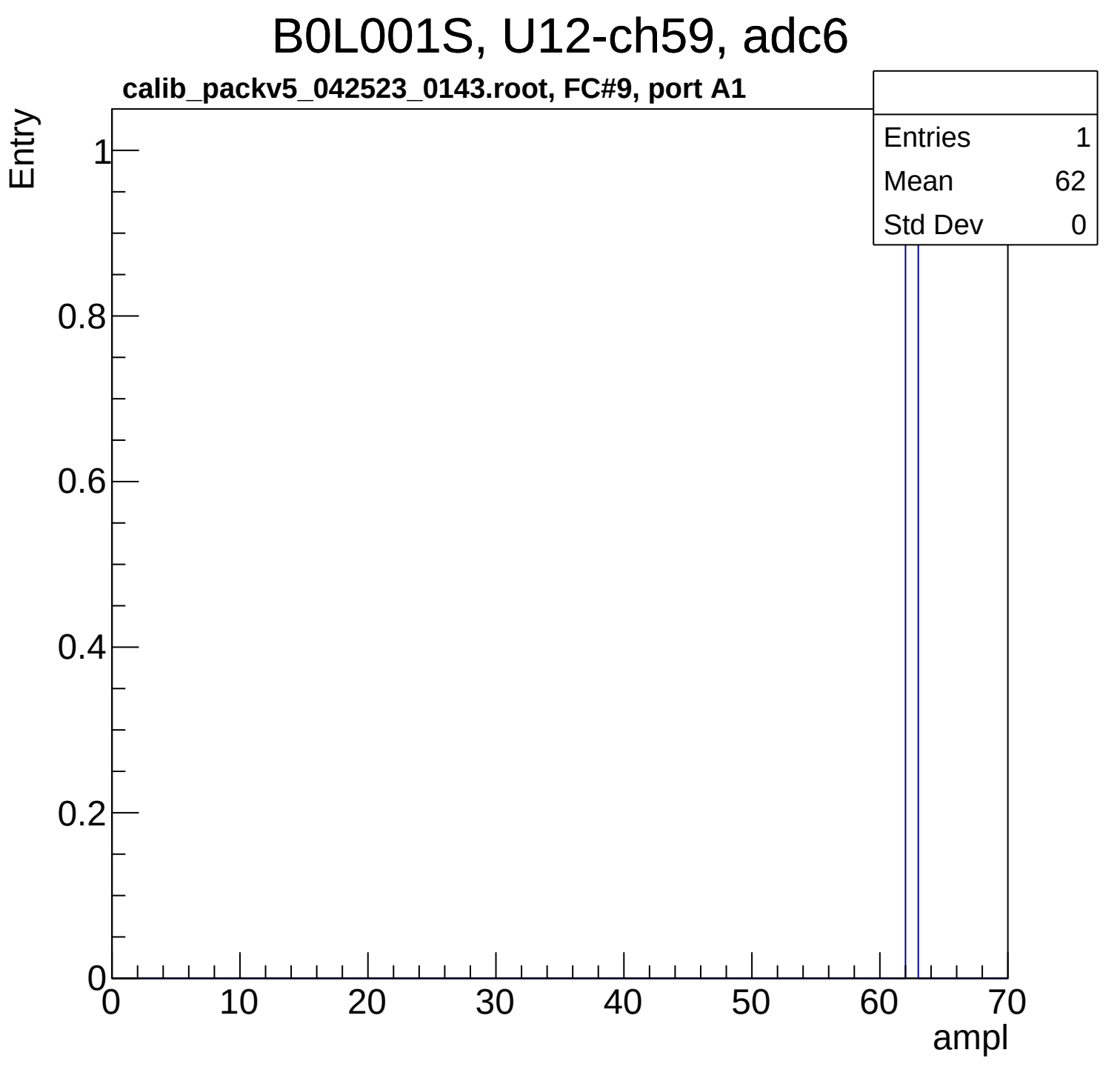
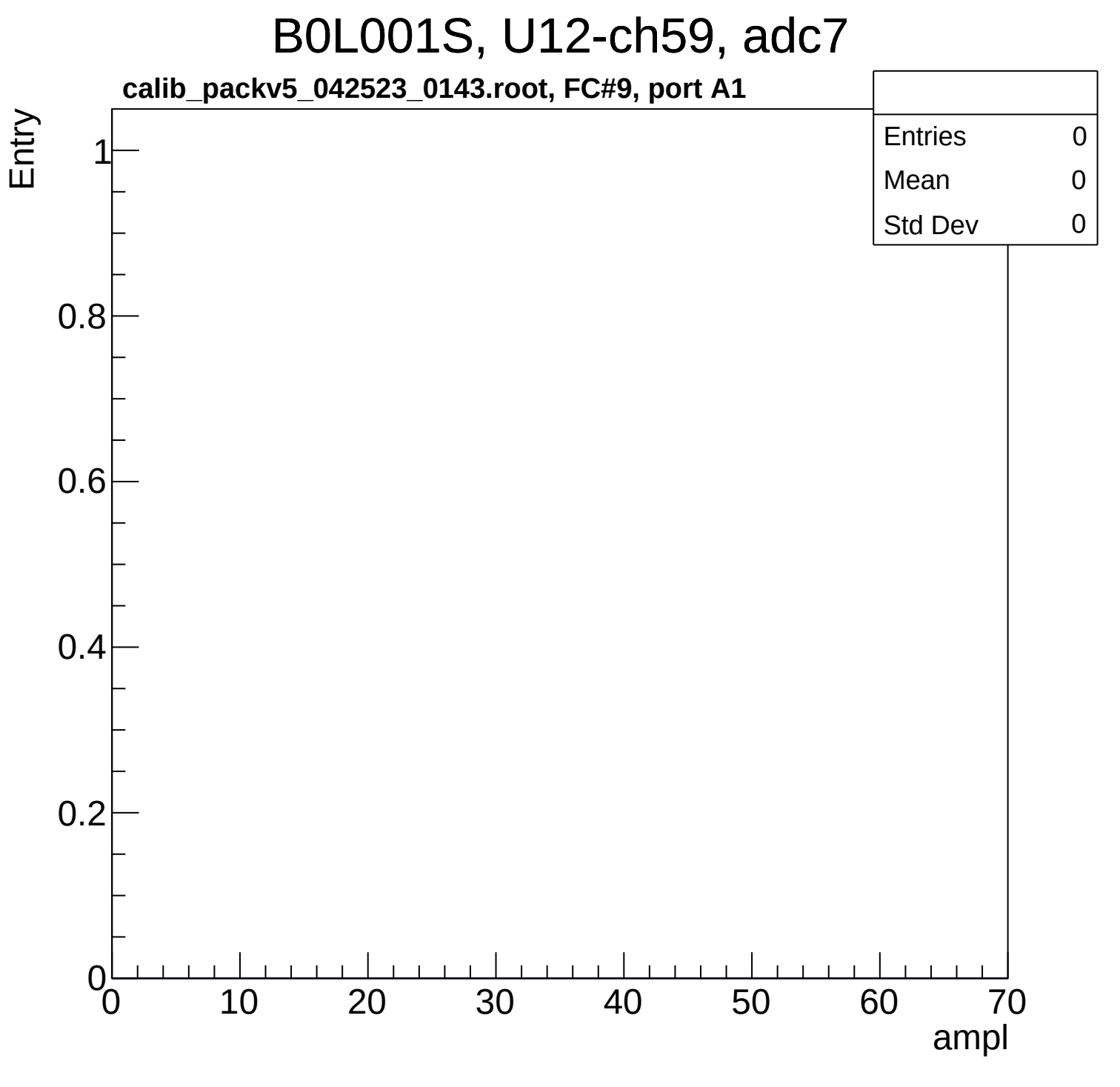
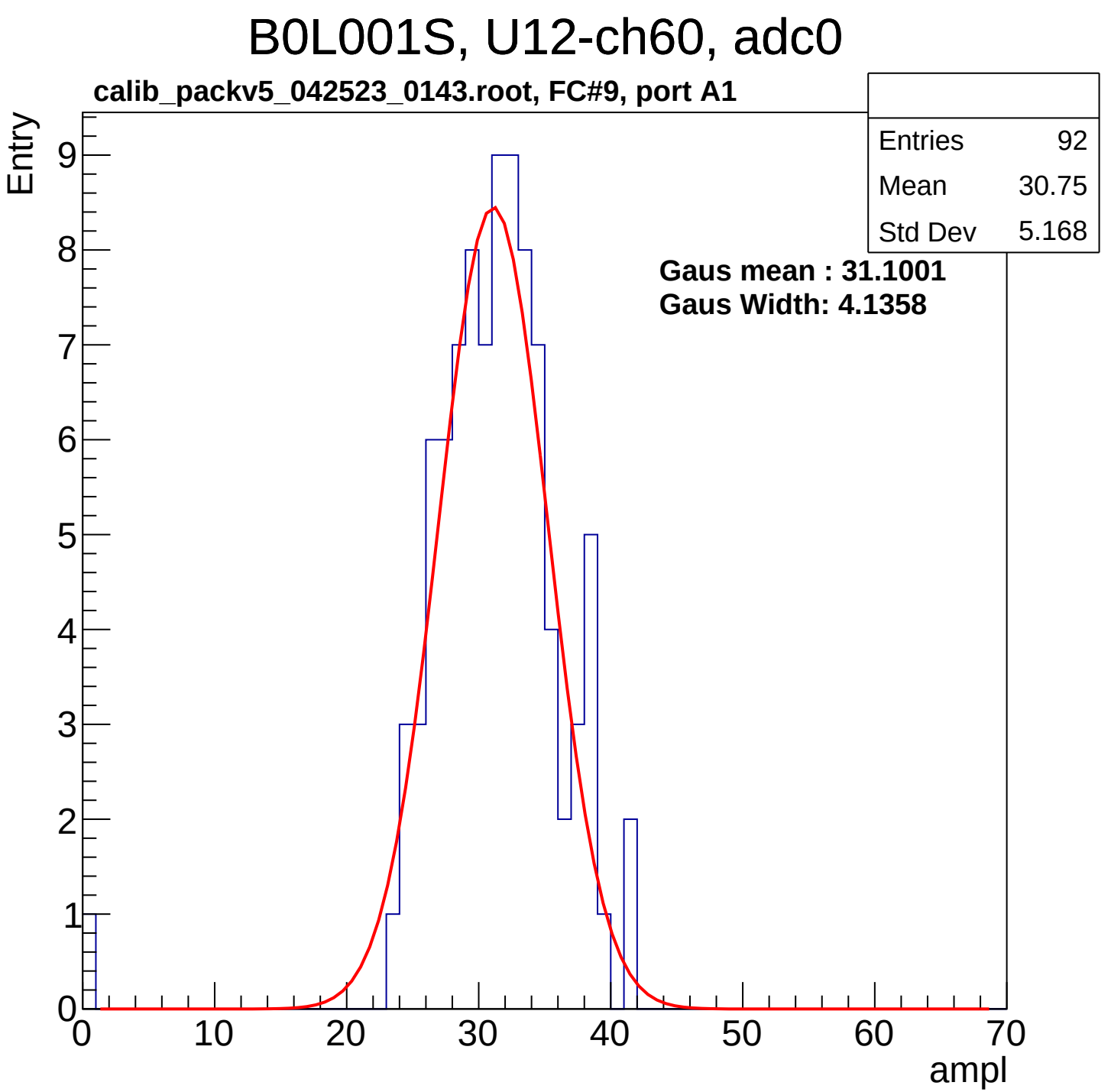

B0L001S, U12-ch59, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 75
Mean 50.09
Std Dev 3.724
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch59, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 66
Mean 56.21
Std Dev 7.645
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch59, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 30
Mean 60.8
Std Dev 1.904
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch59, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch59, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch60, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 92
Mean 30.75
Std Dev 5.168
Gaus mean : 31.1001
Gaus Width: 4.1358
Entry
ampl
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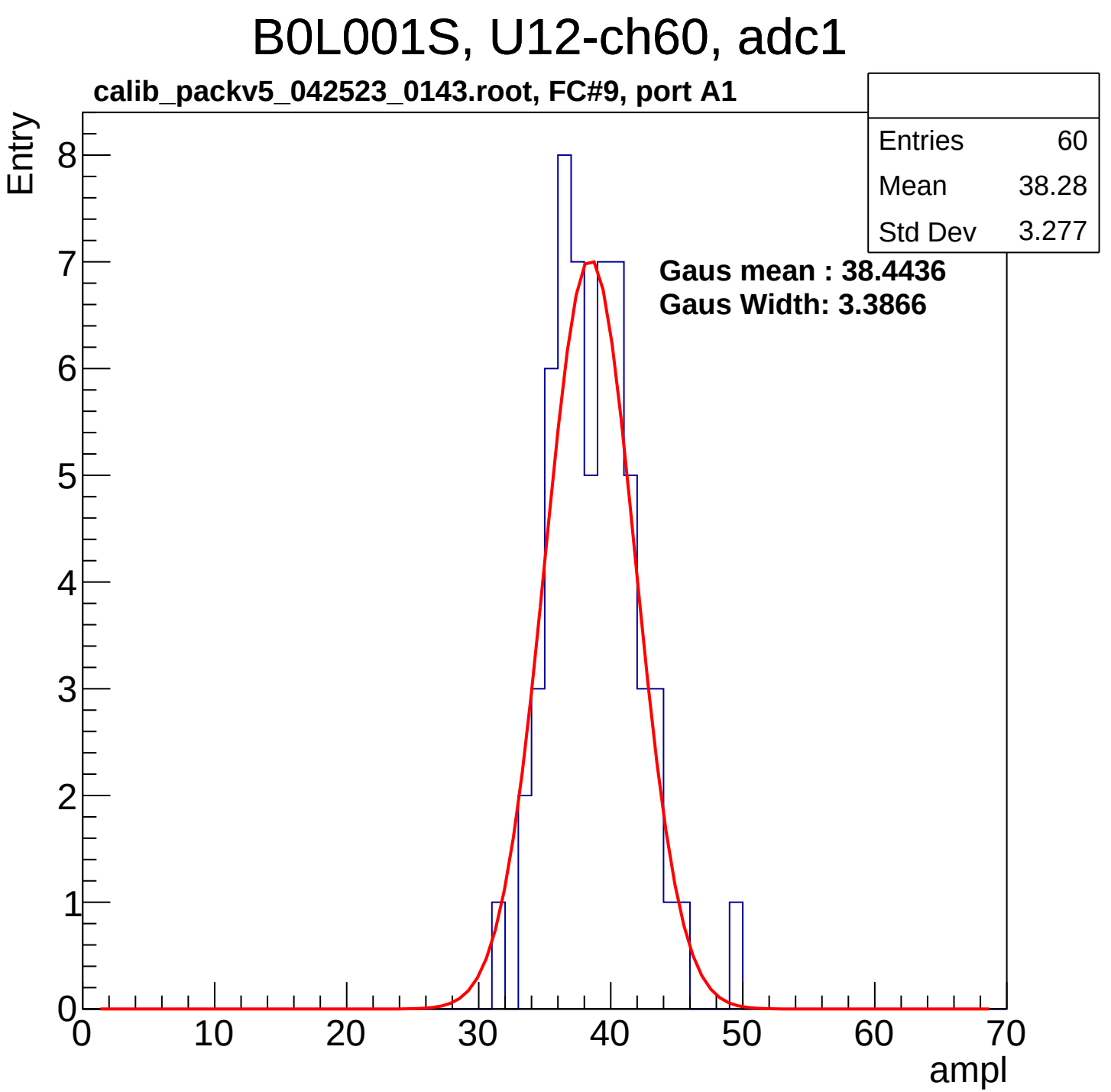
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch60, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 60
Mean 38.28
Std Dev 3.277
Gaus mean : 38.4436
Gaus Width: 3.3866
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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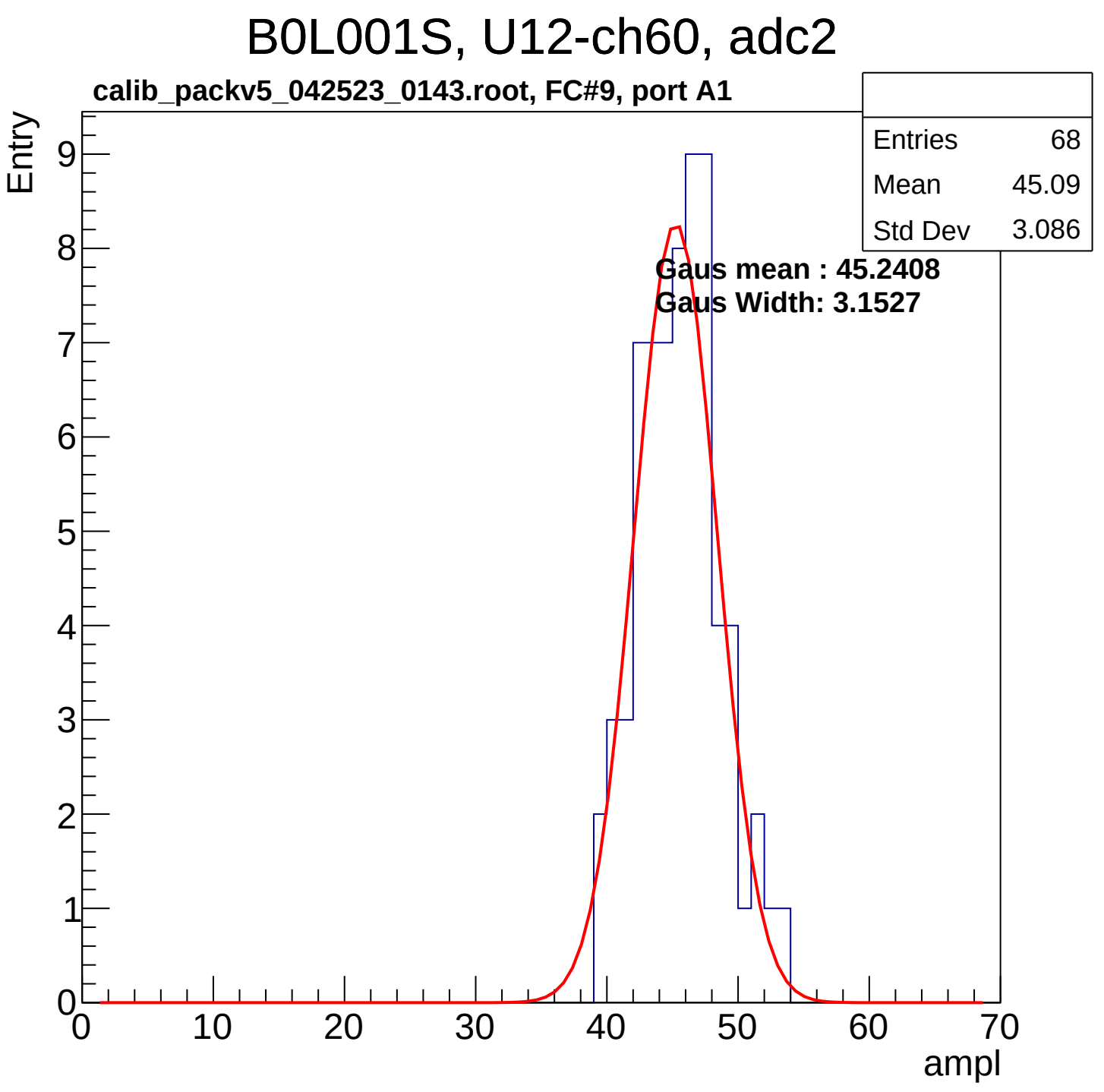
40
50
60
70


B0L001S, U12-ch60, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 68
Mean 45.09
Std Dev 3.086
Gaus mean : 45.2408
Gaus Width: 3.1527
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
50
60
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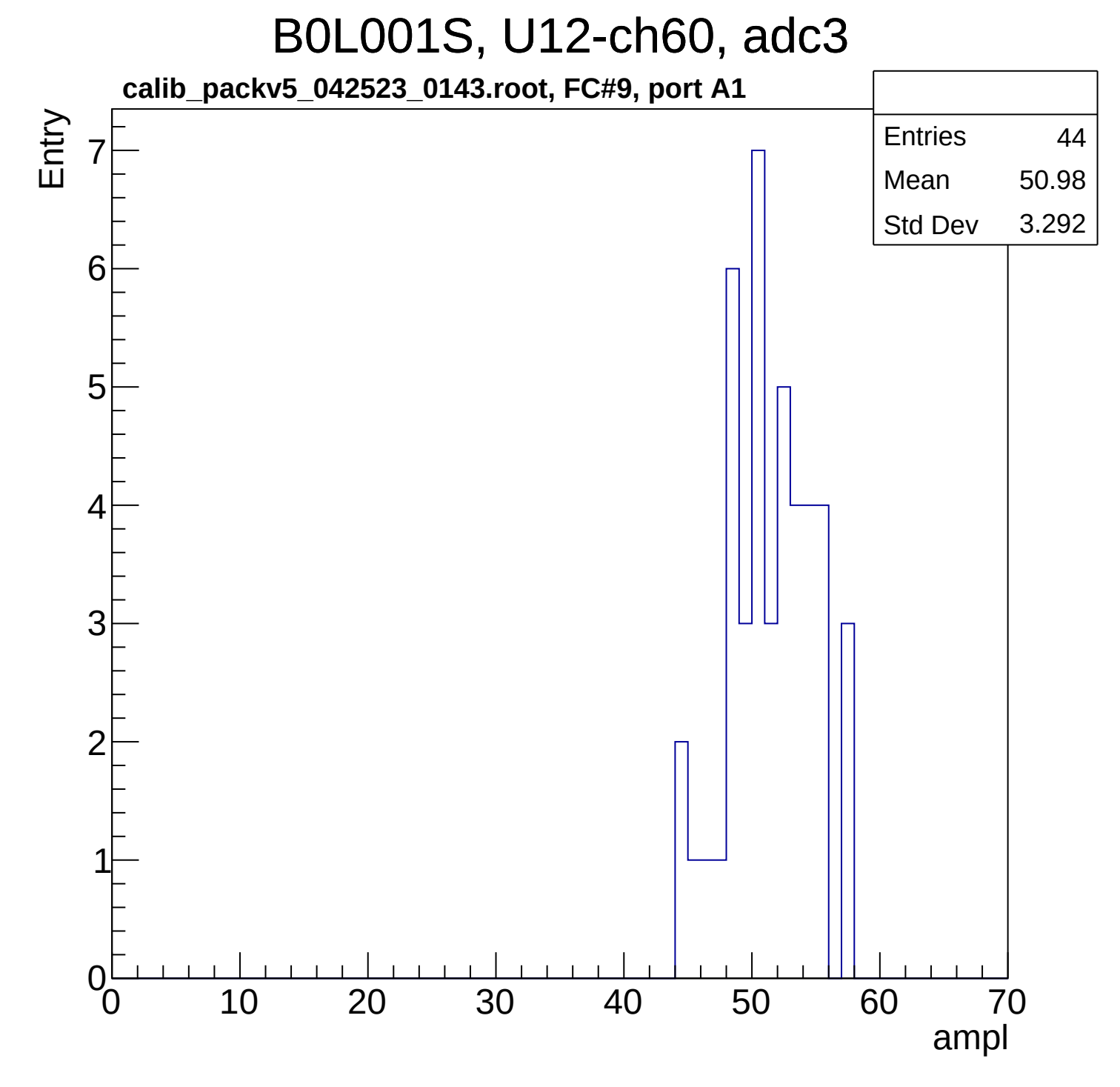
B0L001S, U12-ch60, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 44
Mean 50.98
Std Dev 3.292
Entry
ampl
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3
4
5
6
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0
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40
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60
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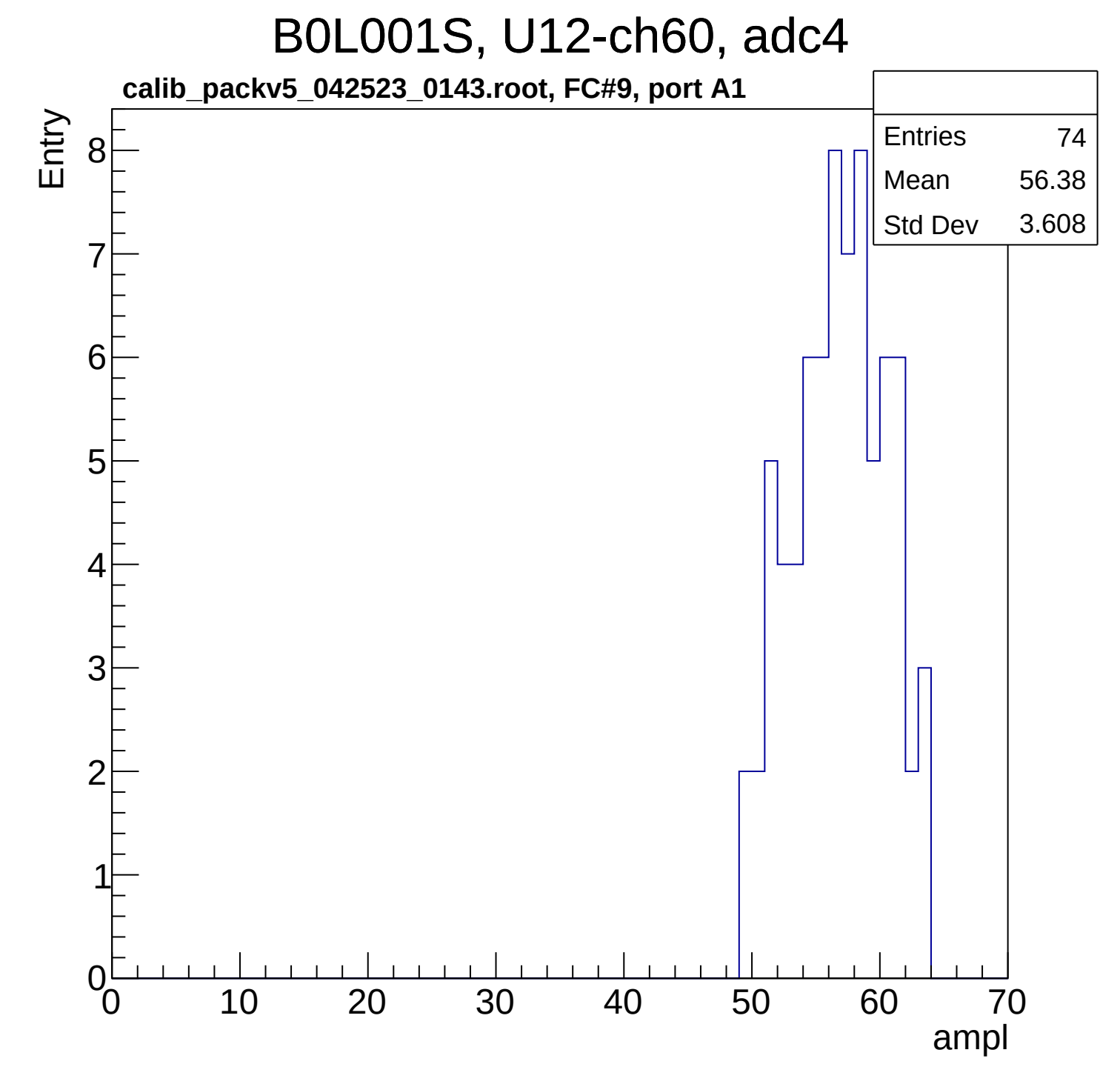
B0L001S, U12-ch60, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 74
Mean 56.38
Std Dev 3.608
Entry
ampl
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3
4
5
6
7
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0
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20
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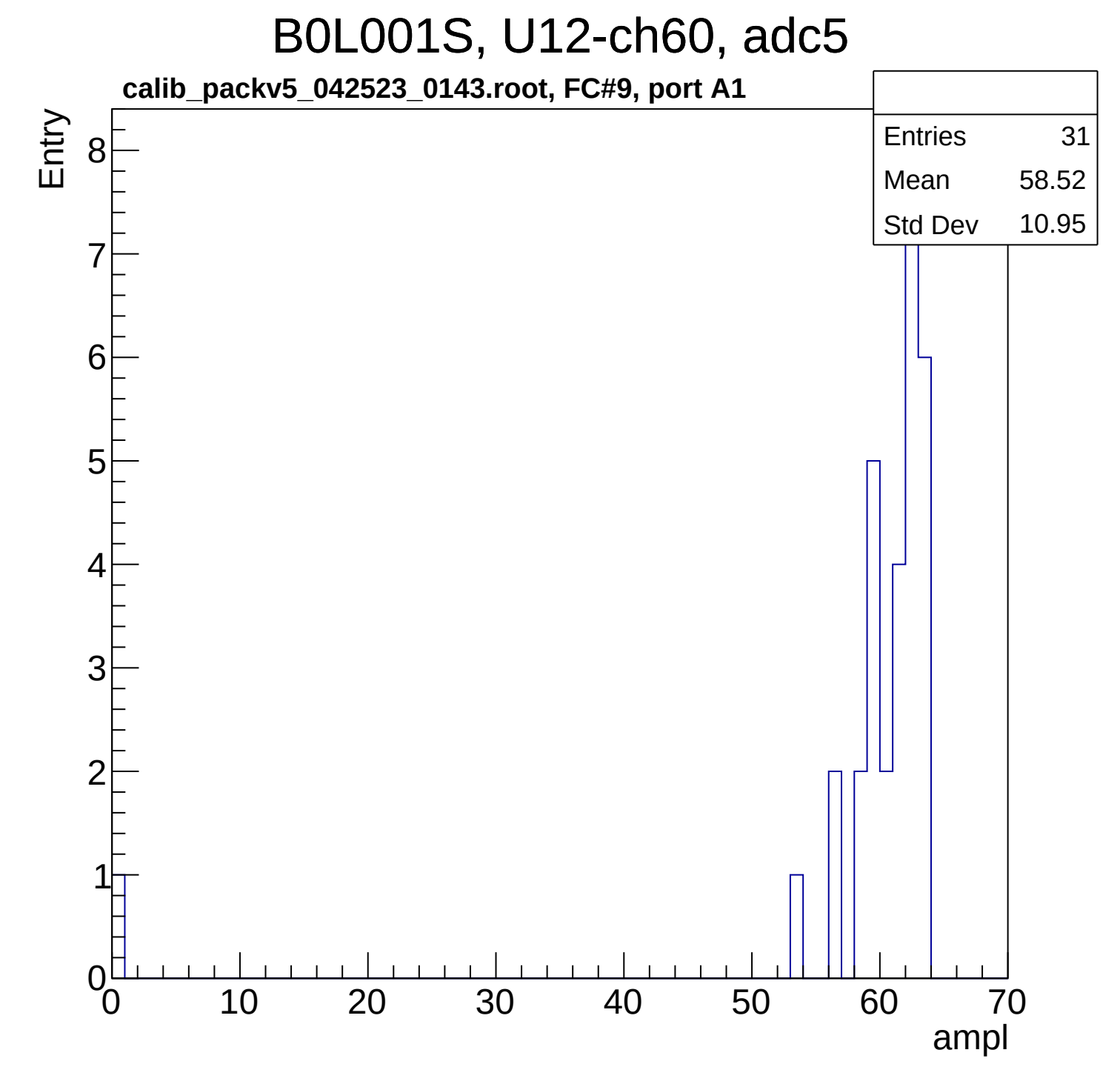
40
50
60
70


B0L001S, U12-ch60, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 31
Mean 58.52
Std Dev 10.95
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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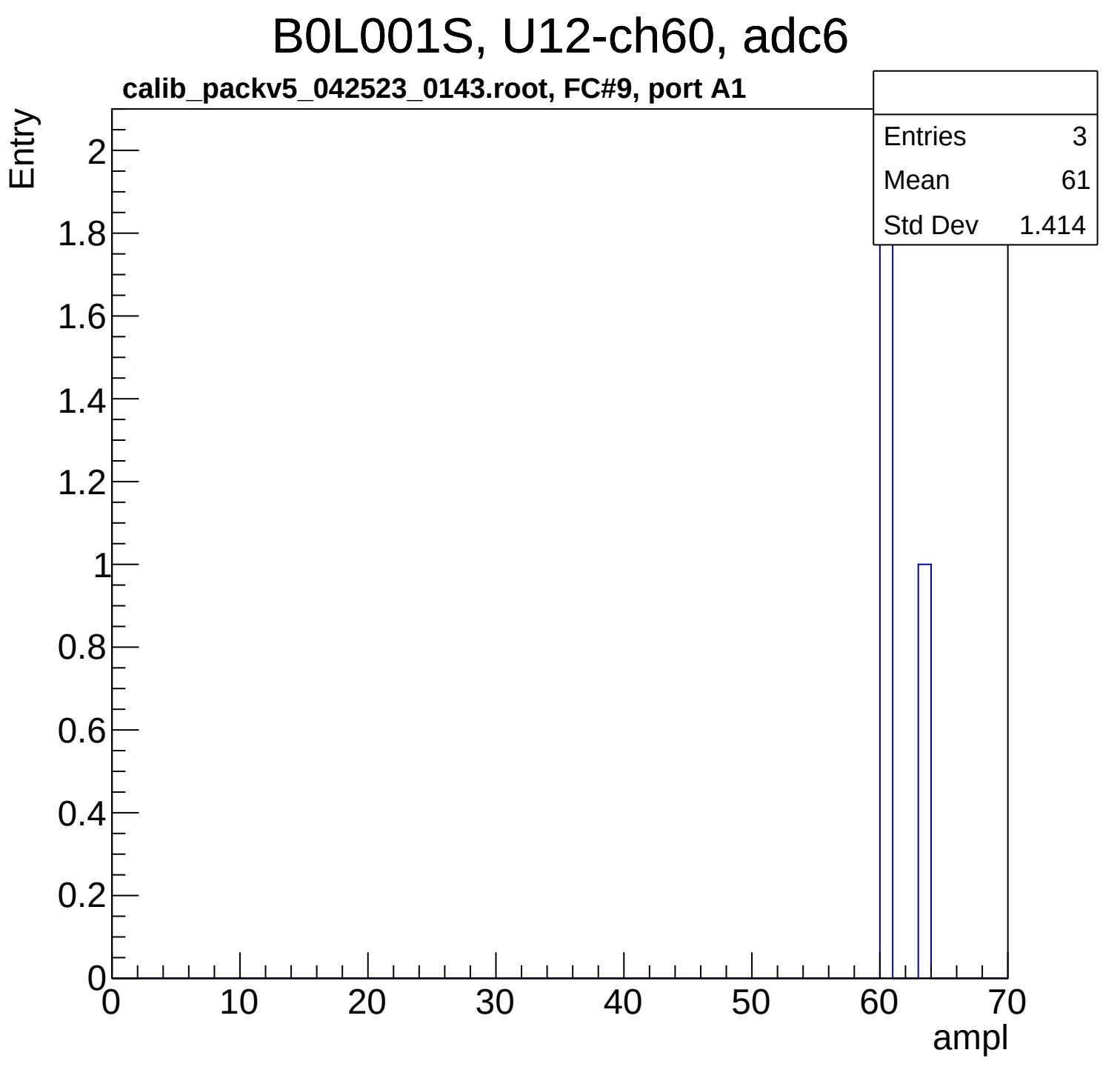
40
50
60
70


B0L001S, U12-ch60, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 3
Mean 61
Std Dev 1.414
Entry
ampl
0
0.2
0.4
0.6
0.8
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1.2
1.4
1.6
1.8
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10
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40
50
60
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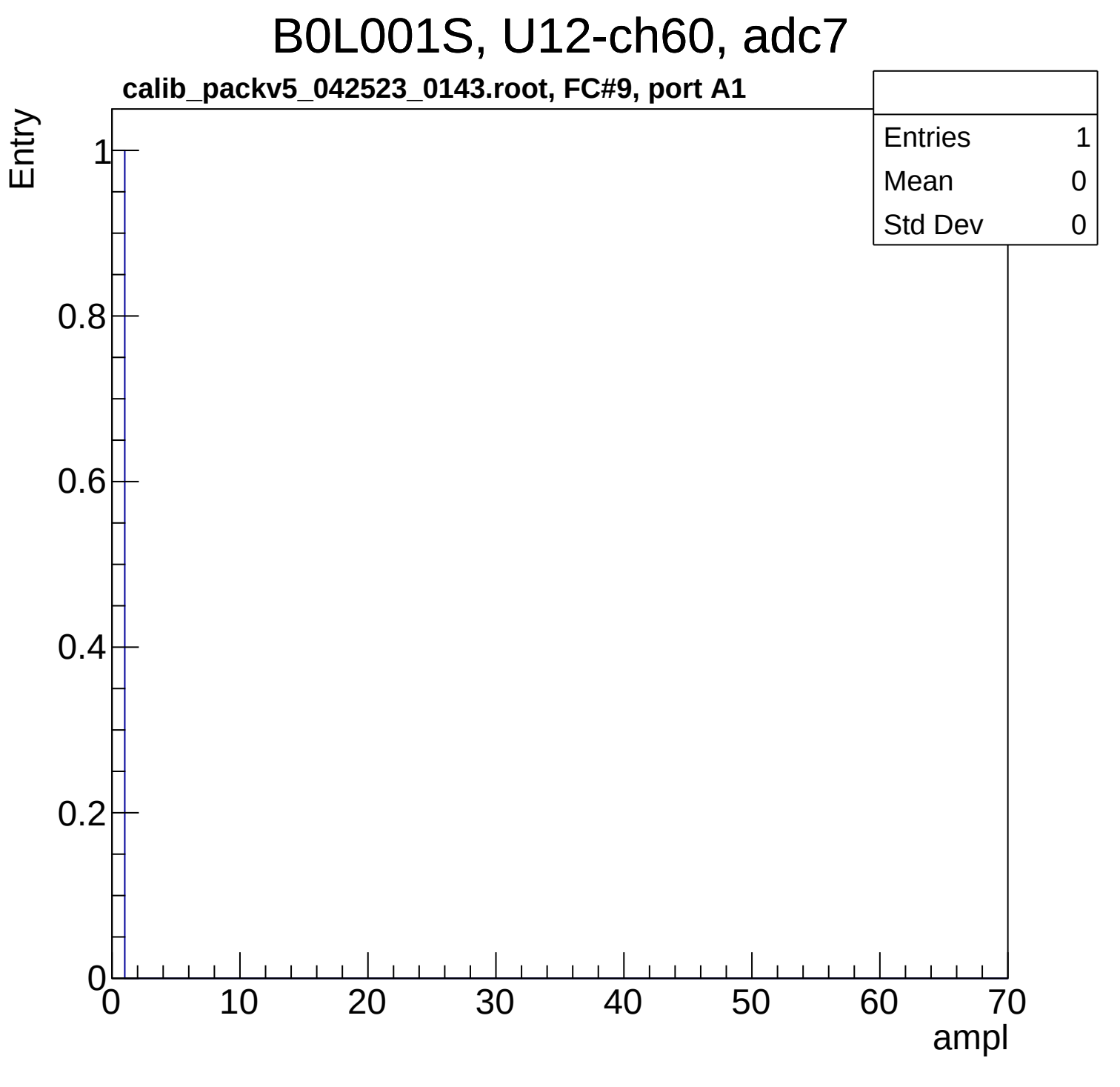
B0L001S, U12-ch60, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 0
Std Dev 0
Entry
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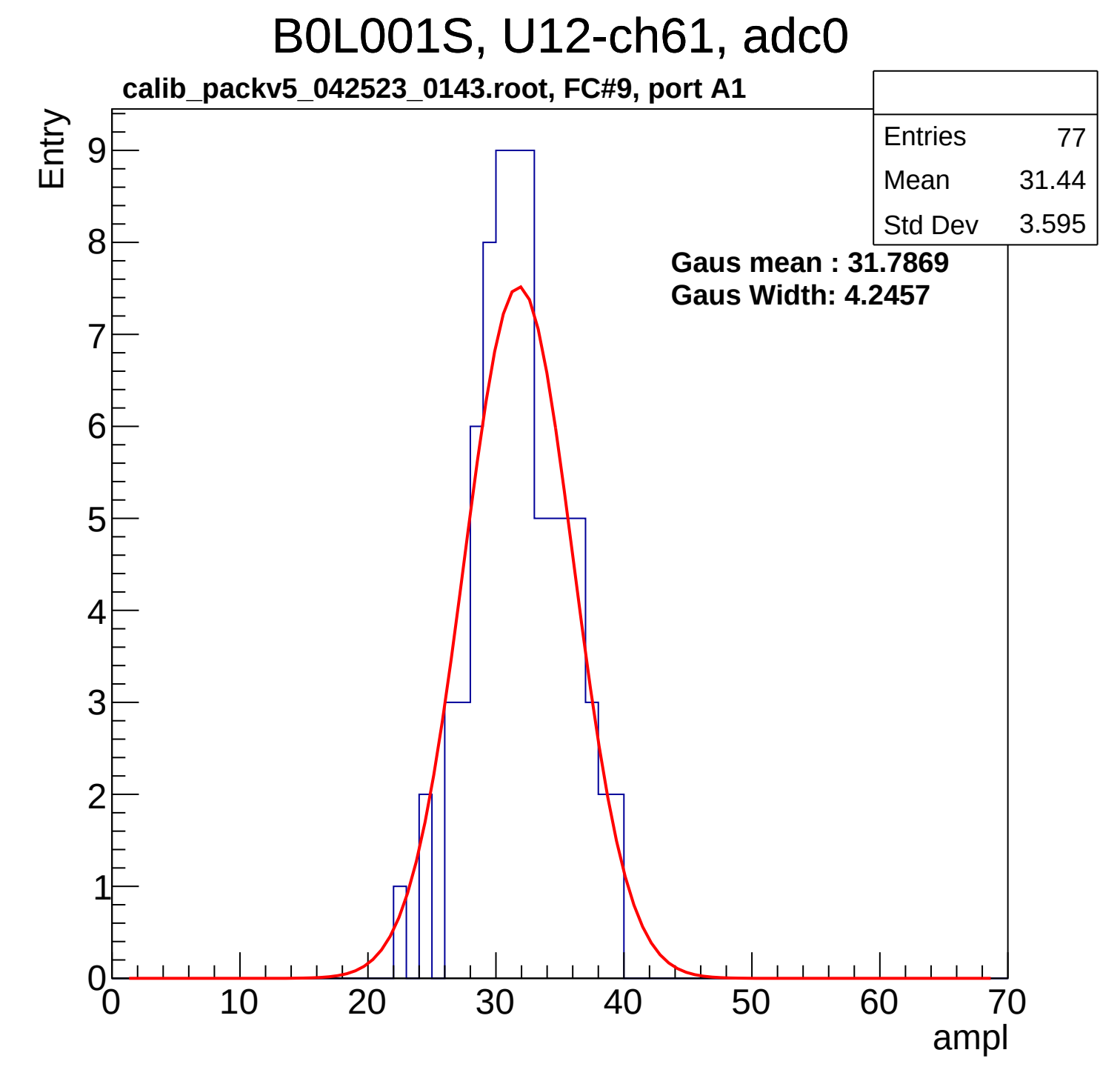
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch61, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 77
Mean 31.44
Std Dev 3.595
Gaus mean : 31.7869
Gaus Width: 4.2457
Entry
ampl
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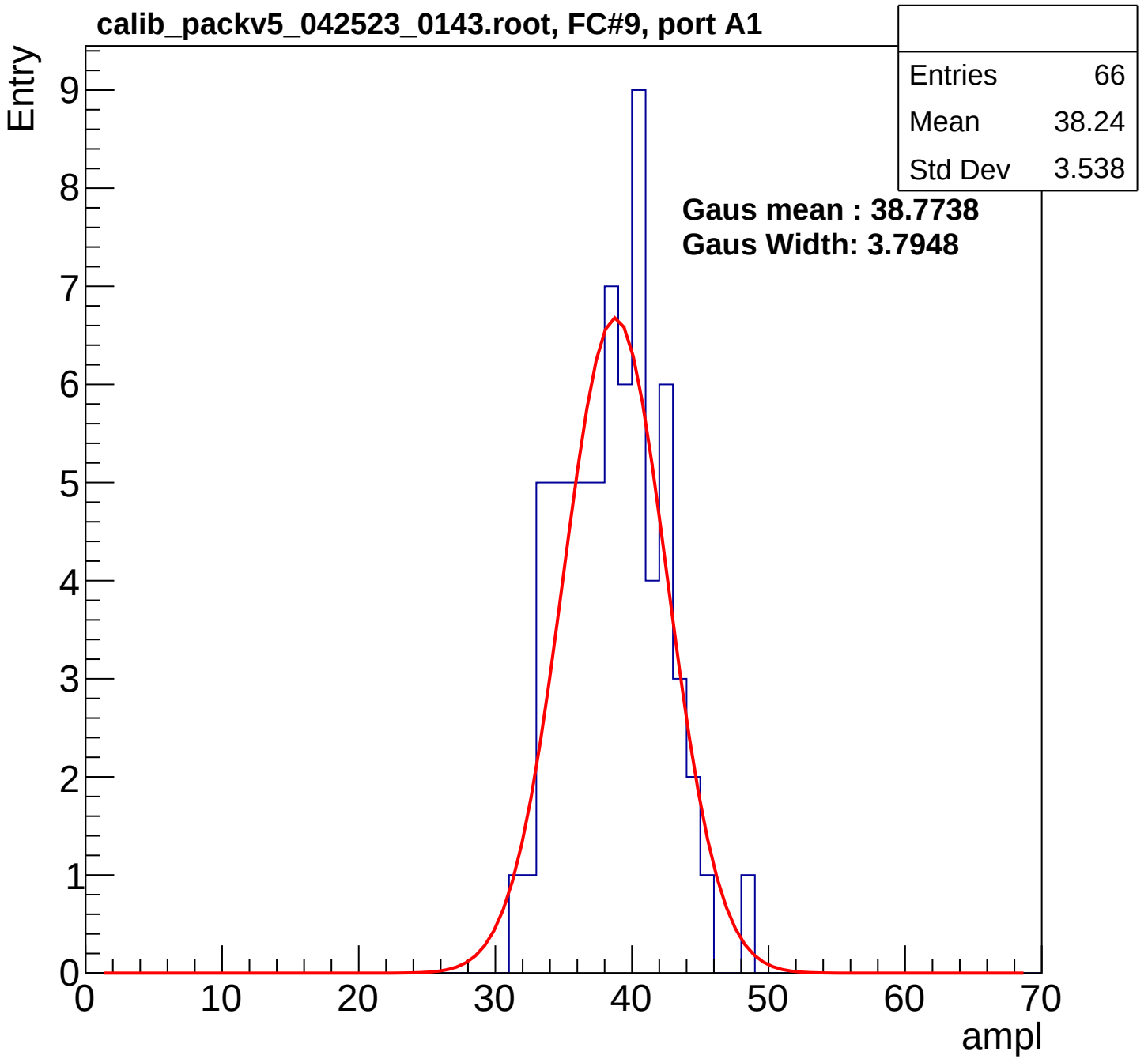
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch61, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 66
Mean 38.24
Std Dev 3.538
Gaus mean : 38.7738
Gaus Width: 3.7948
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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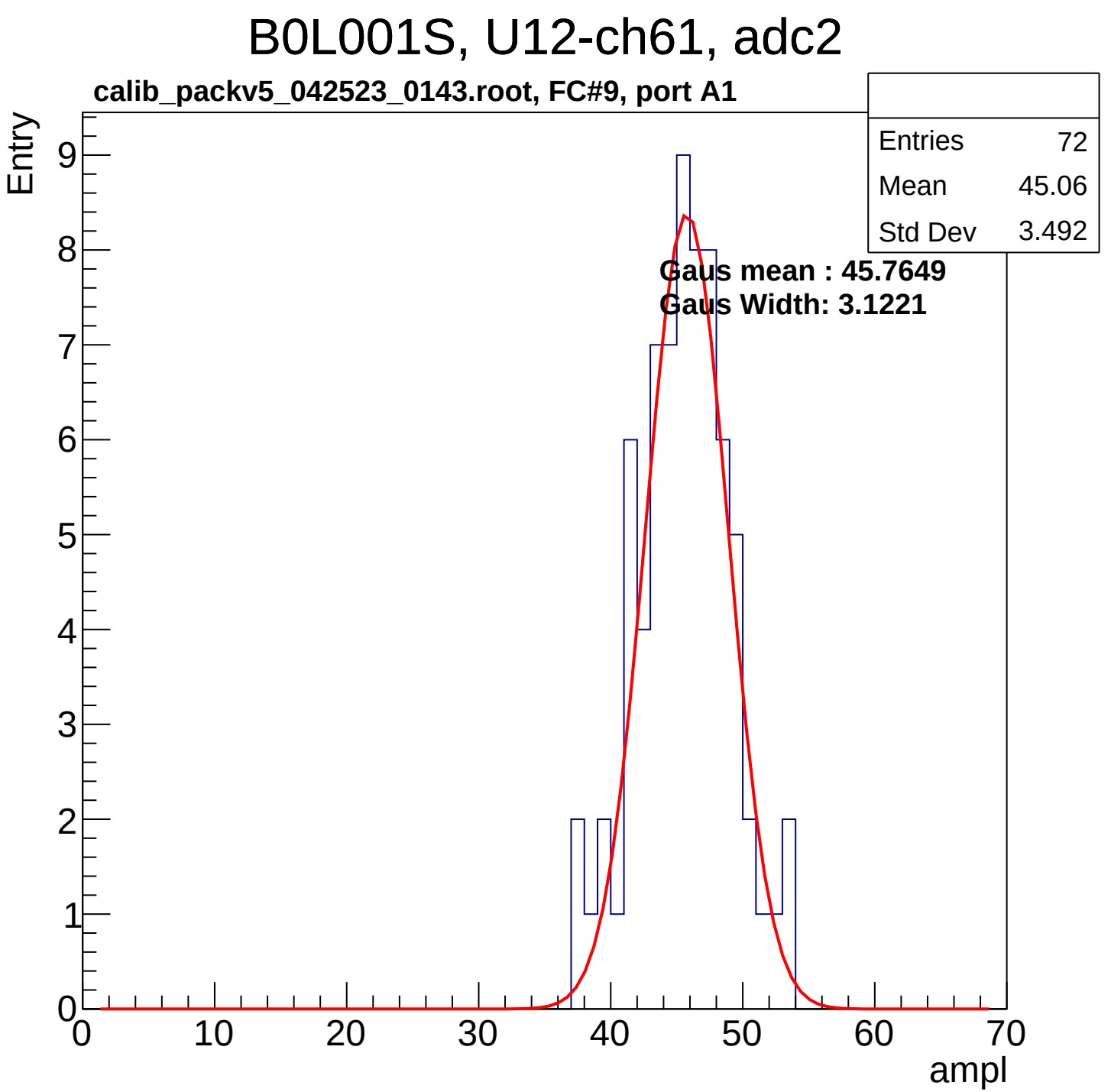
B0L001S, U12-ch61, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 72
Mean 45.06
Std Dev 3.492
Gaus mean : 45.7649
Gaus Width: 3.1221
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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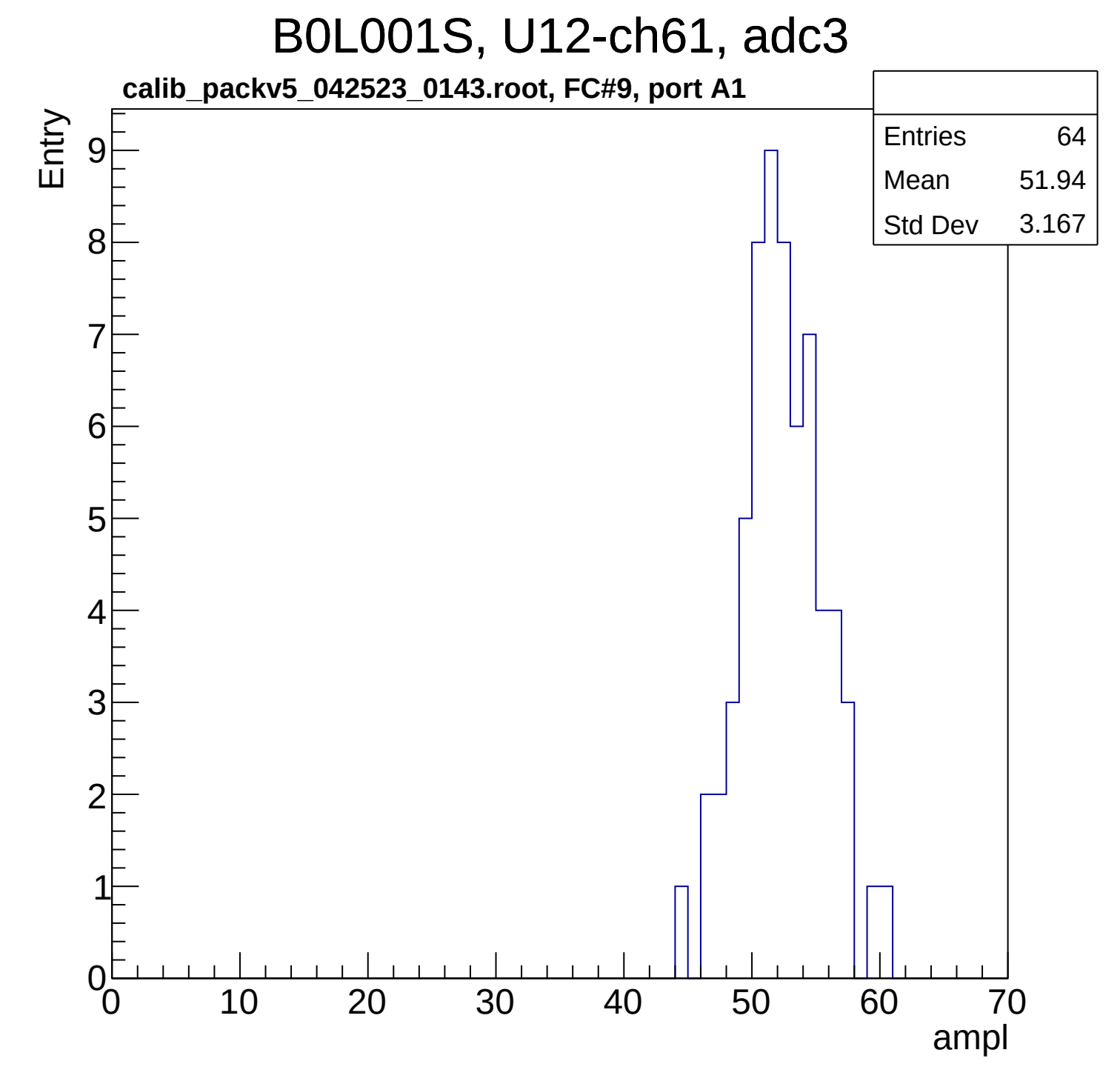
B0L001S, U12-ch61, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 64
Mean 51.94
Std Dev 3.167
Entry
ampl
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6
7
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0
10
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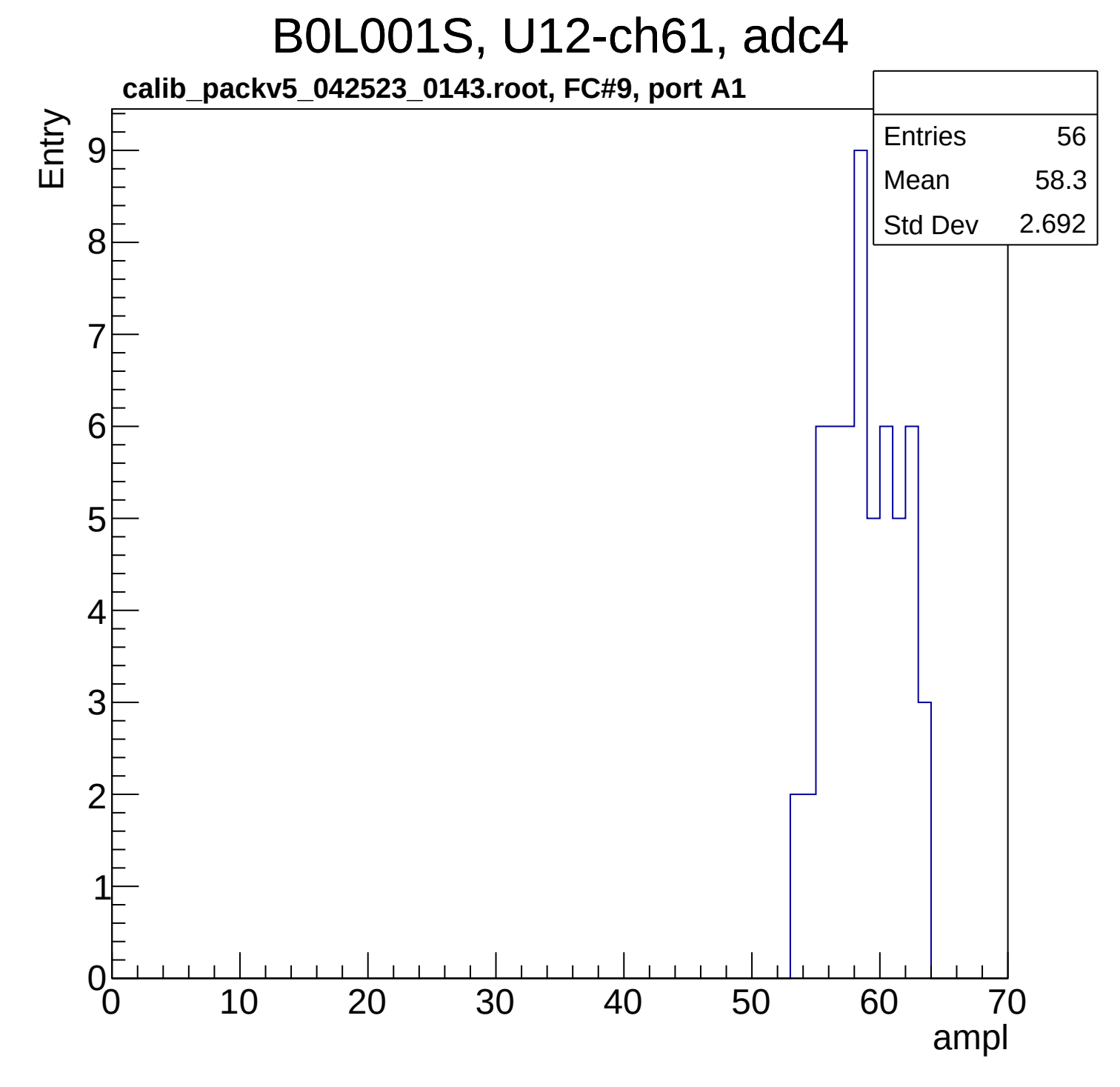
60
70


B0L001S, U12-ch61, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 56
Mean 58.3
Std Dev 2.692
Entry
ampl
0
1
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0
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60
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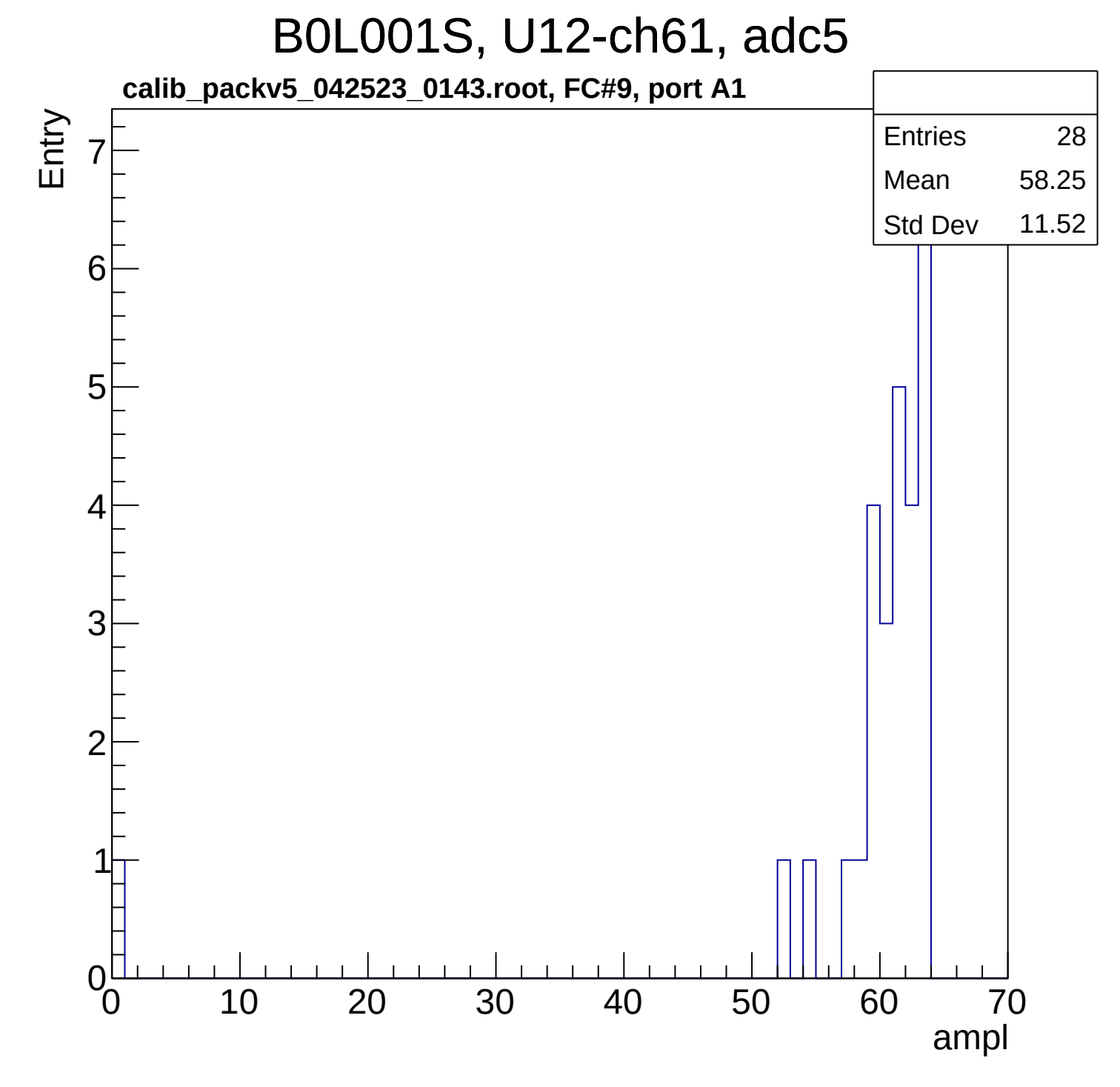
B0L001S, U12-ch61, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 28
Mean 58.25
Std Dev 11.52
Entry
ampl
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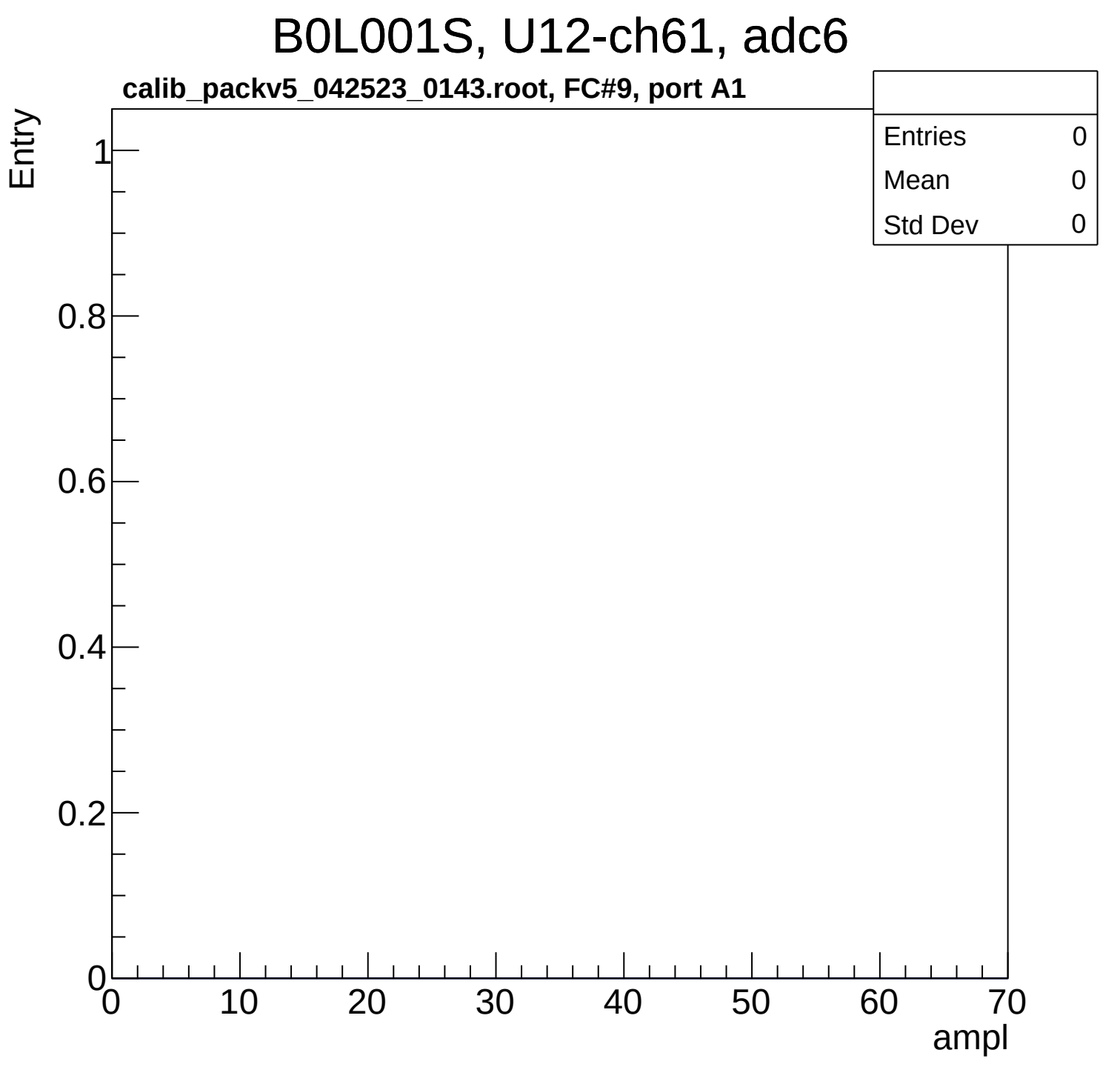
B0L001S, U12-ch61, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
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0.6
0.4
0.2
0
0
10
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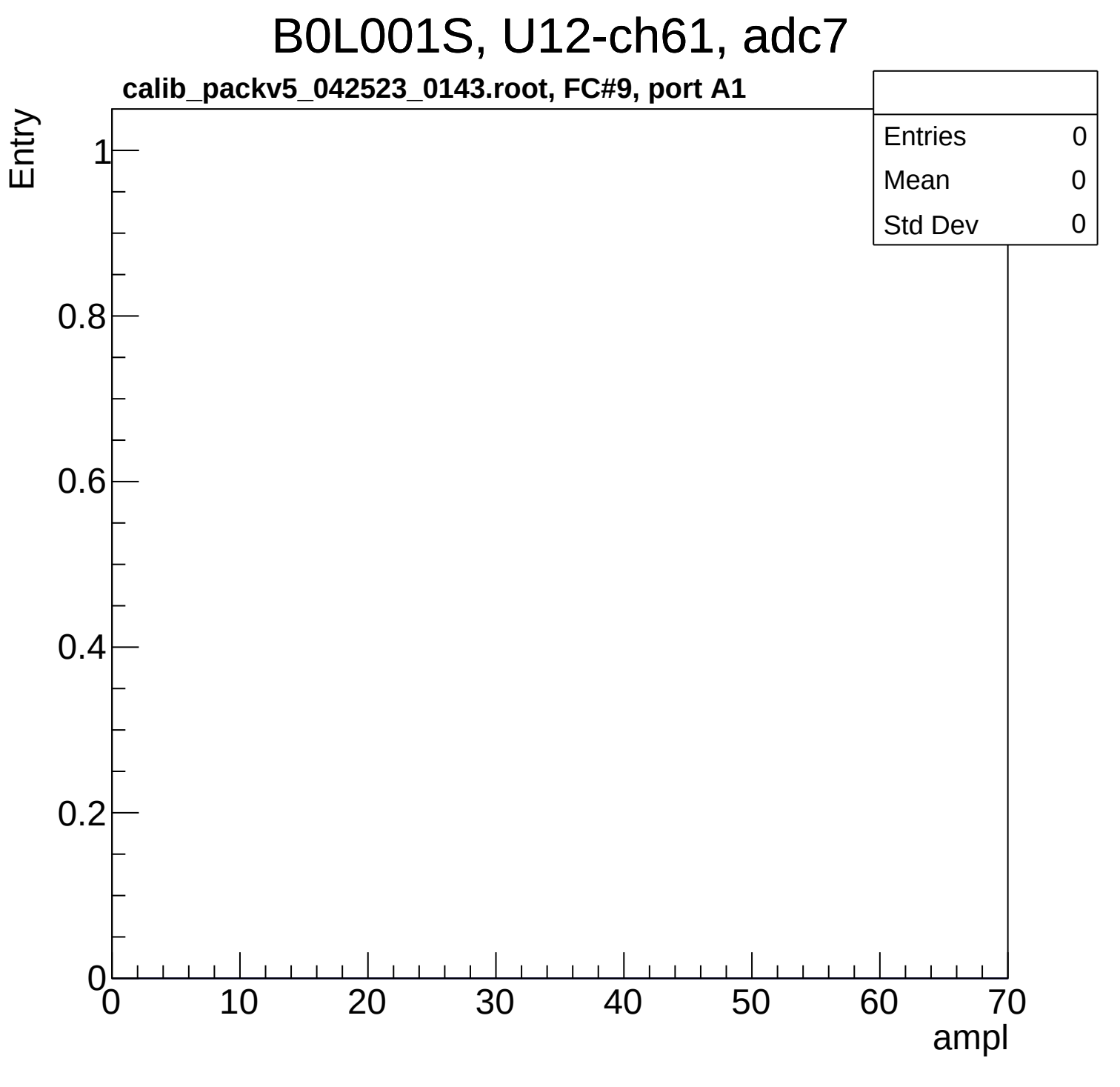
50
60
70
ampl


B0L001S, U12-ch61, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
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0.6
0.4
0.2
0
0
10
20
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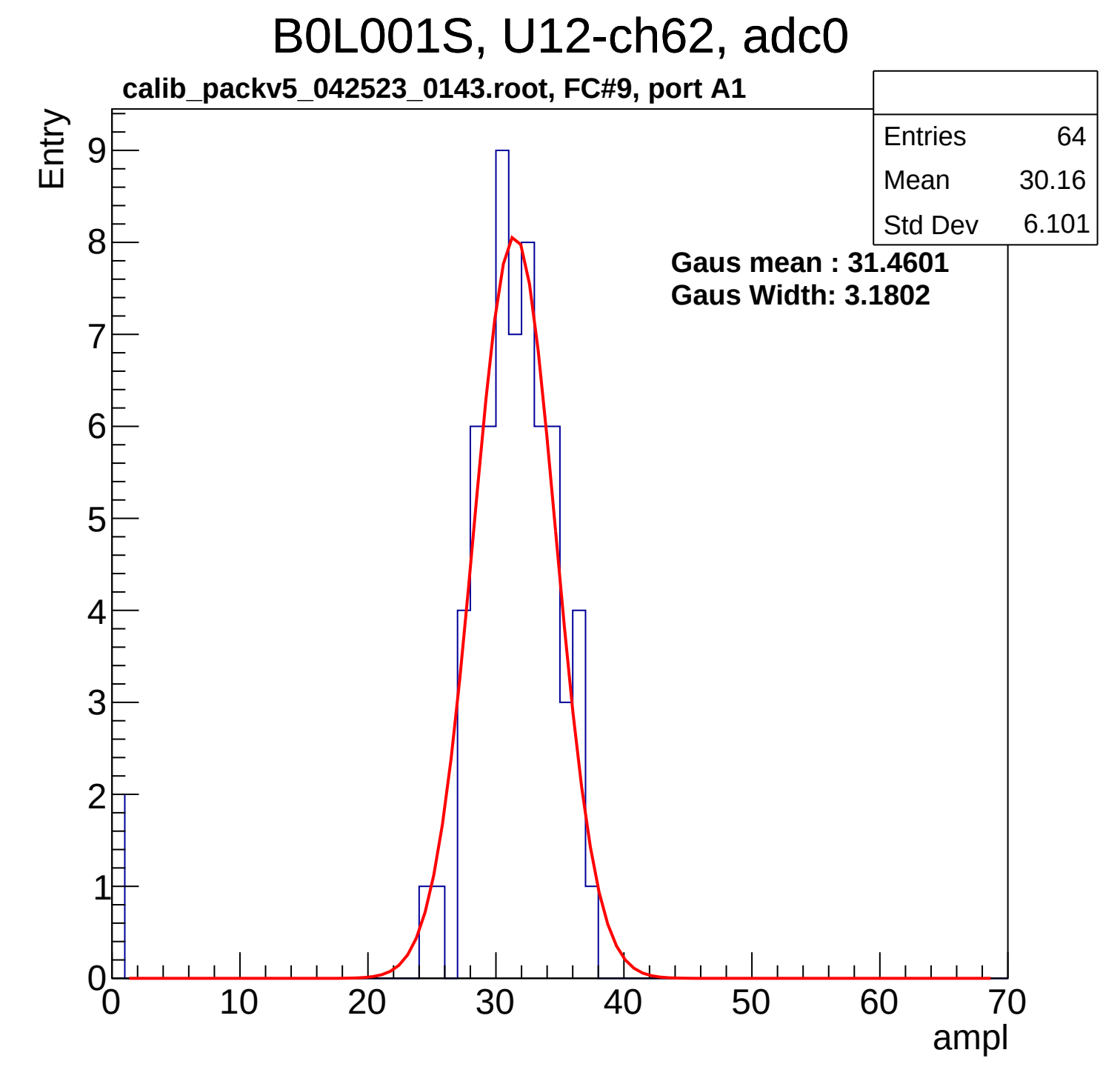
50
60
70
ampl


B0L001S, U12-ch62, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 64
Mean 30.16
Std Dev 6.101
Gaus mean : 31.4601
Gaus Width: 3.1802
Entry
ampl
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3
4
5
6
7
8
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0
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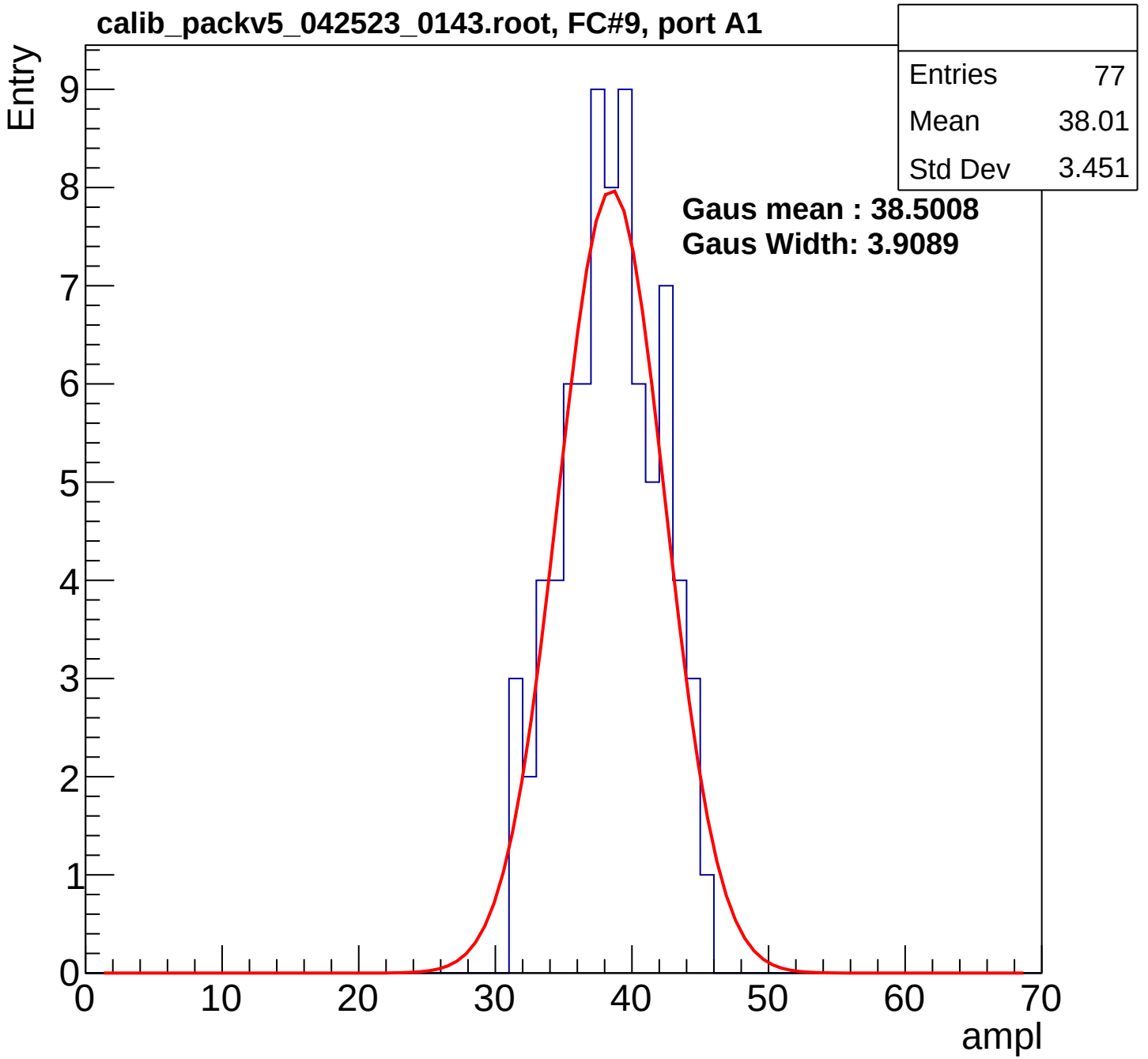
B0L001S, U12-ch62, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 77
Mean 38.01
Std Dev 3.451
Gaus mean : 38.5008
Gaus Width: 3.9089
Entry
ampl
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2
3
4
5
6
7
8
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0
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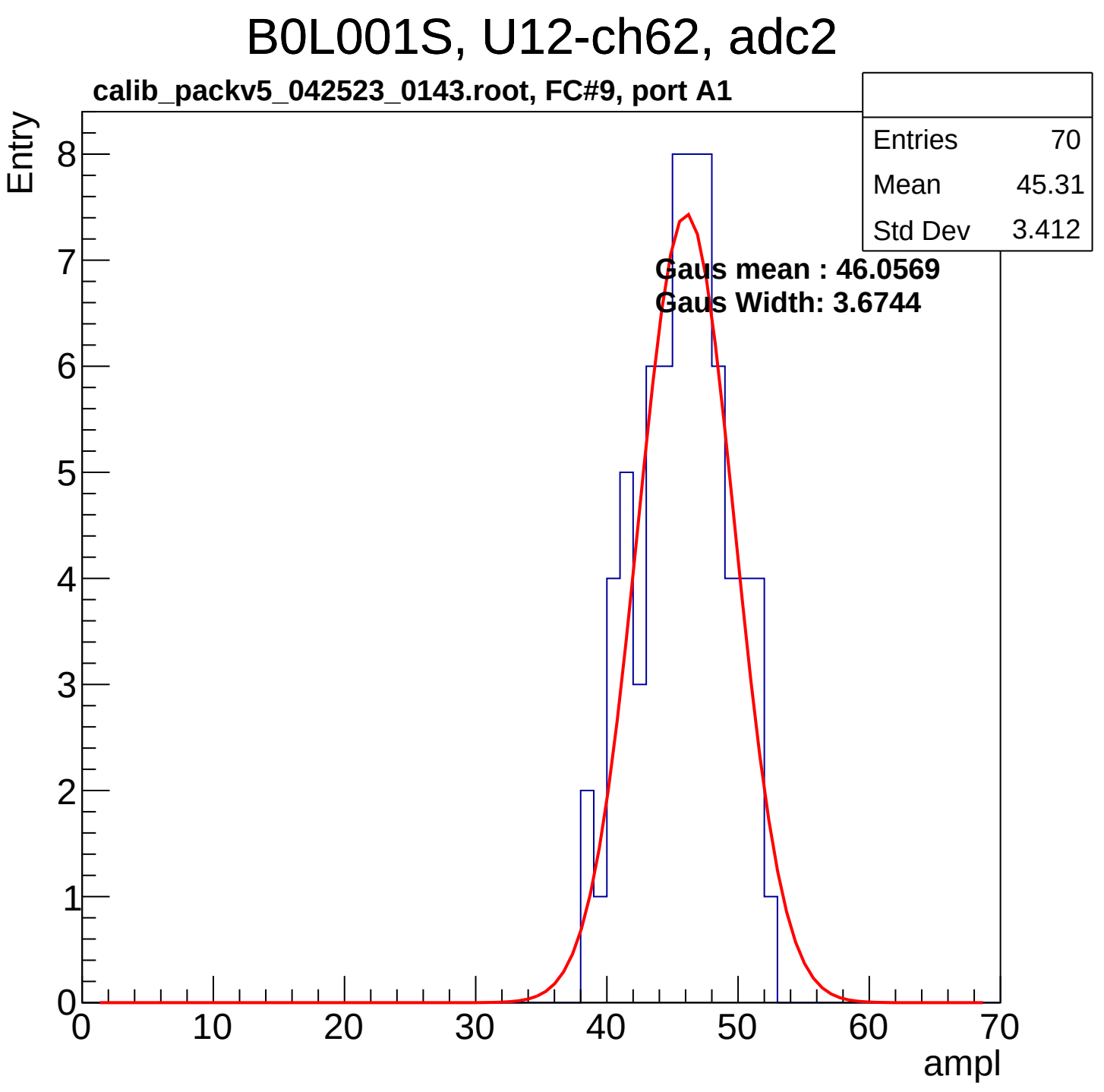
B0L001S, U12-ch62, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 70
Mean 45.31
Std Dev 3.412
Gaus mean : 46.0569
Gaus Width: 3.6744
Entry
ampl
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1
2
3
4
5
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0
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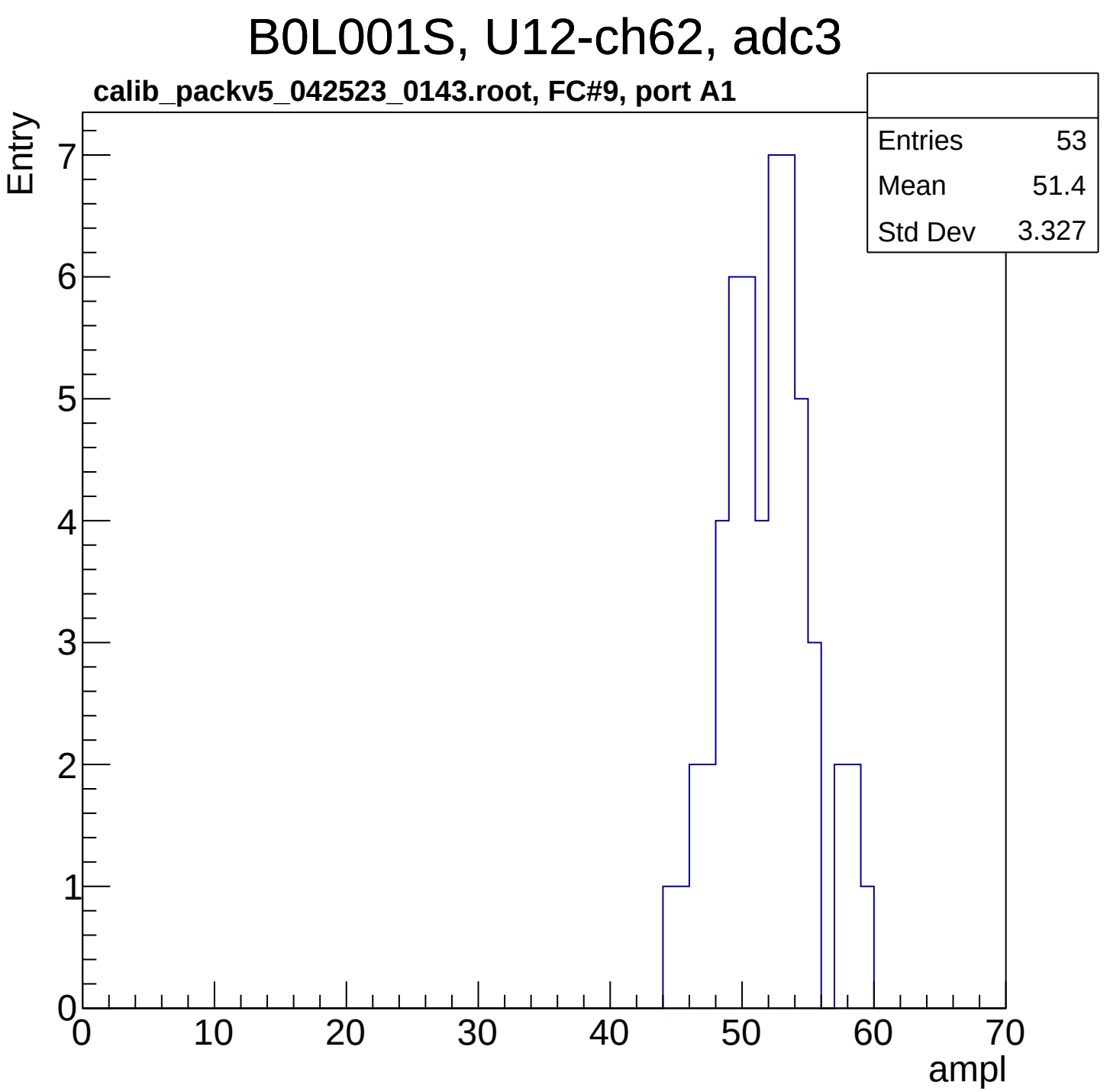
B0L001S, U12-ch62, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 53
Mean 51.4
Std Dev 3.327
Entry
ampl
0
1
2
3
4
5
6
7
0
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60
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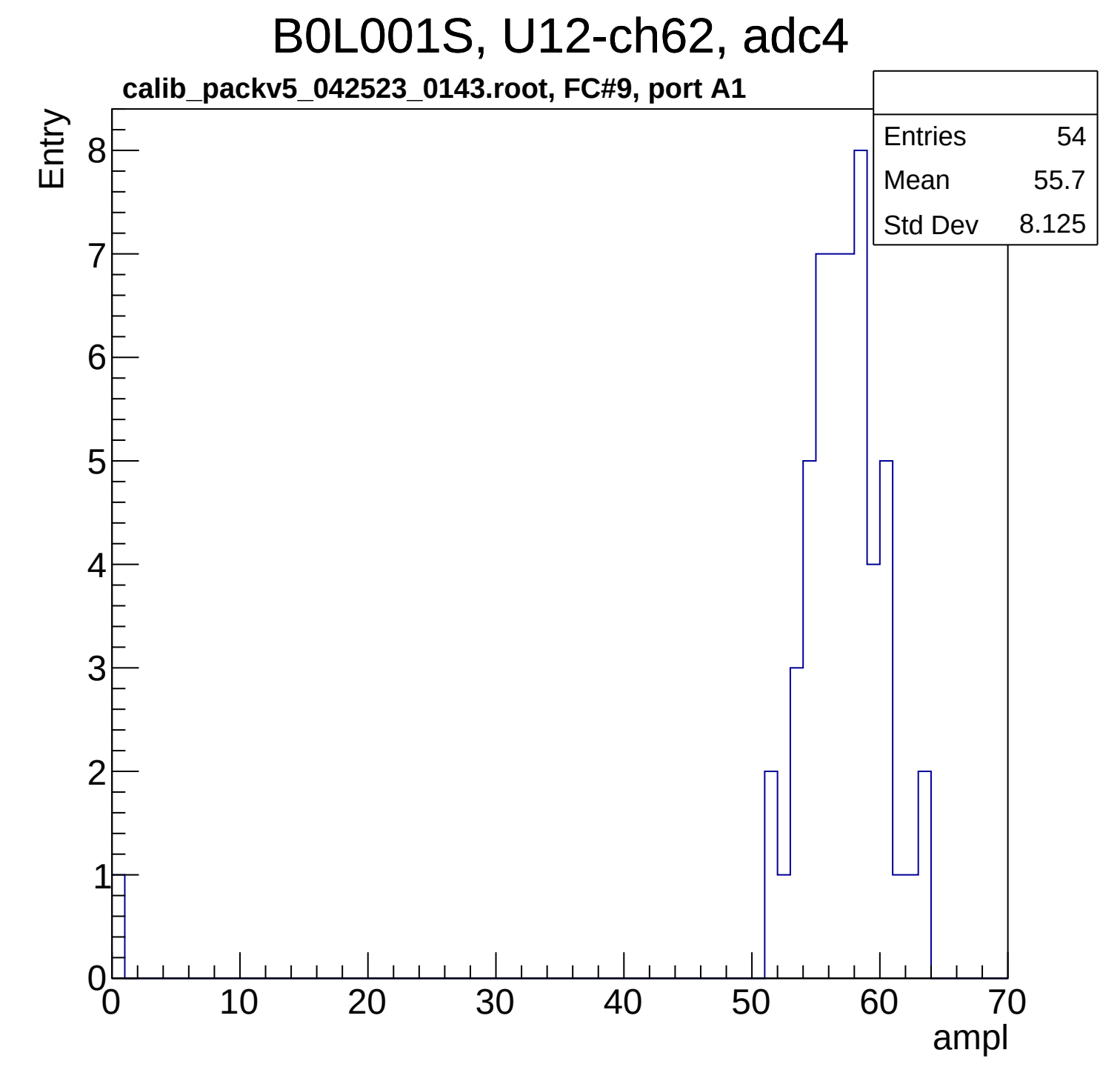
B0L001S, U12-ch62, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 54
Mean 55.7
Std Dev 8.125
Entry
ampl
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2
3
4
5
6
7
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0
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20
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40
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60
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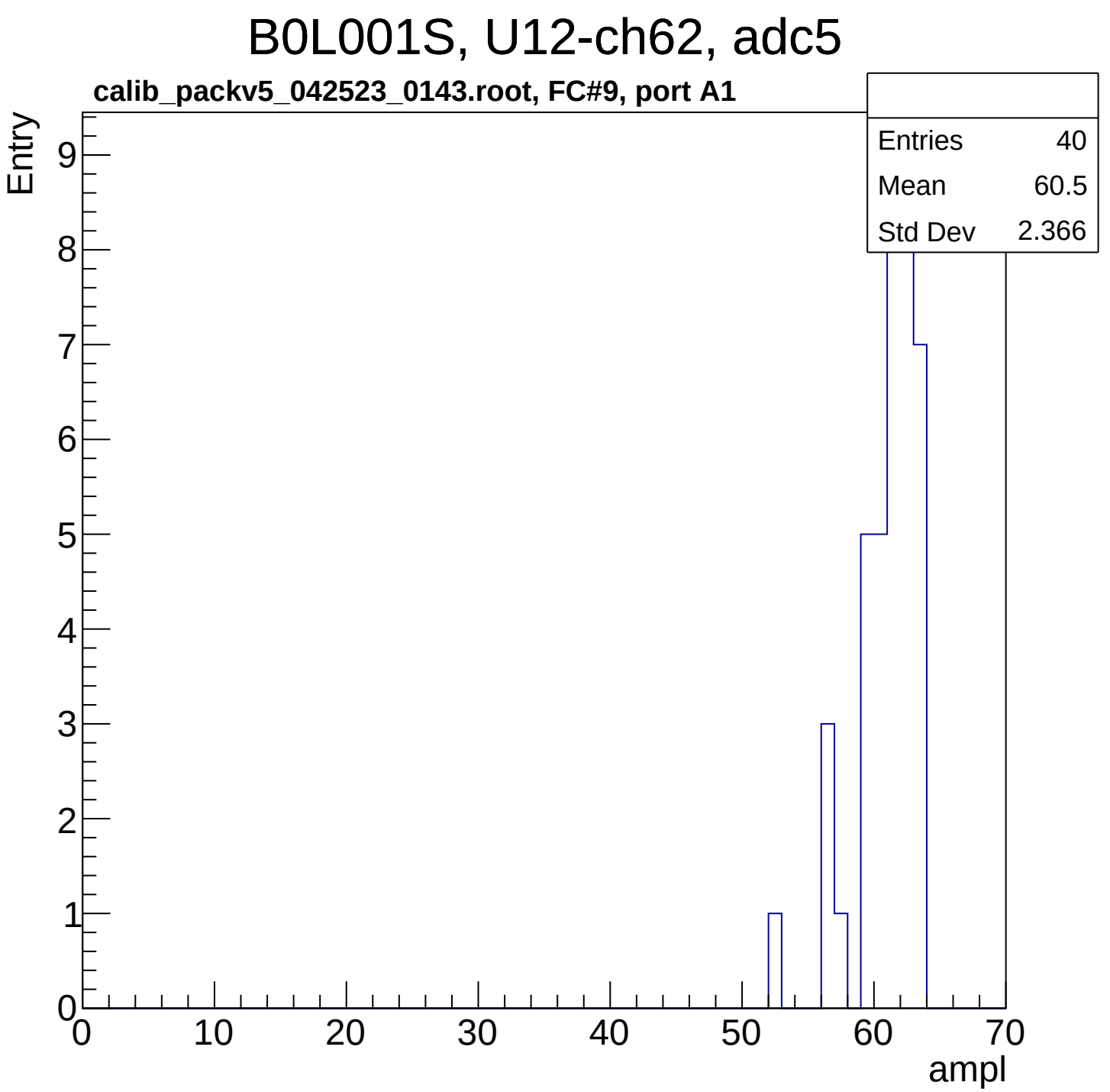
B0L001S, U12-ch62, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 40
Mean 60.5
Std Dev 2.366
Entry
ampl
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3
4
5
6
7
8
9
0
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60
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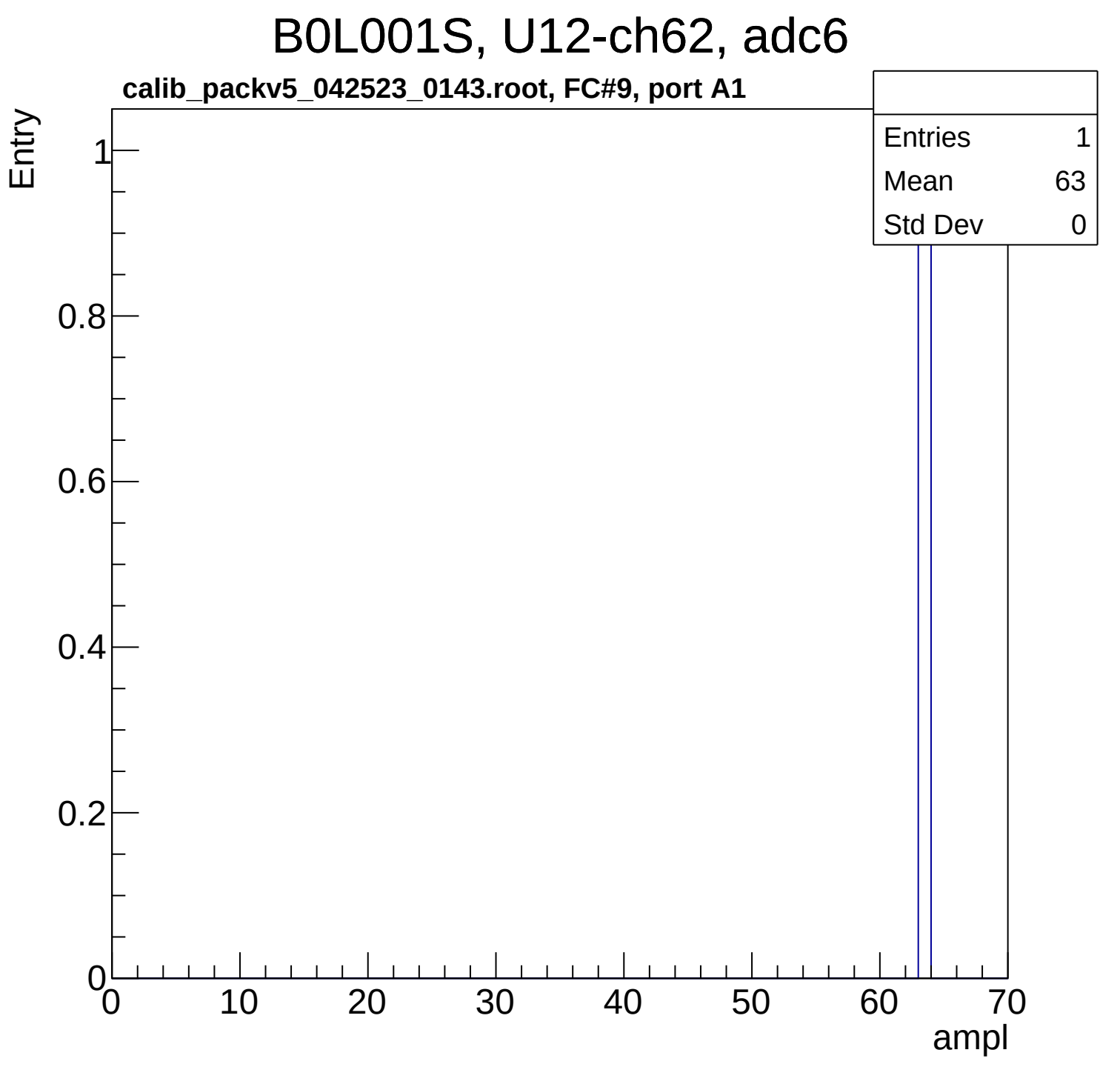
B0L001S, U12-ch62, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 63
Std Dev 0
Entry
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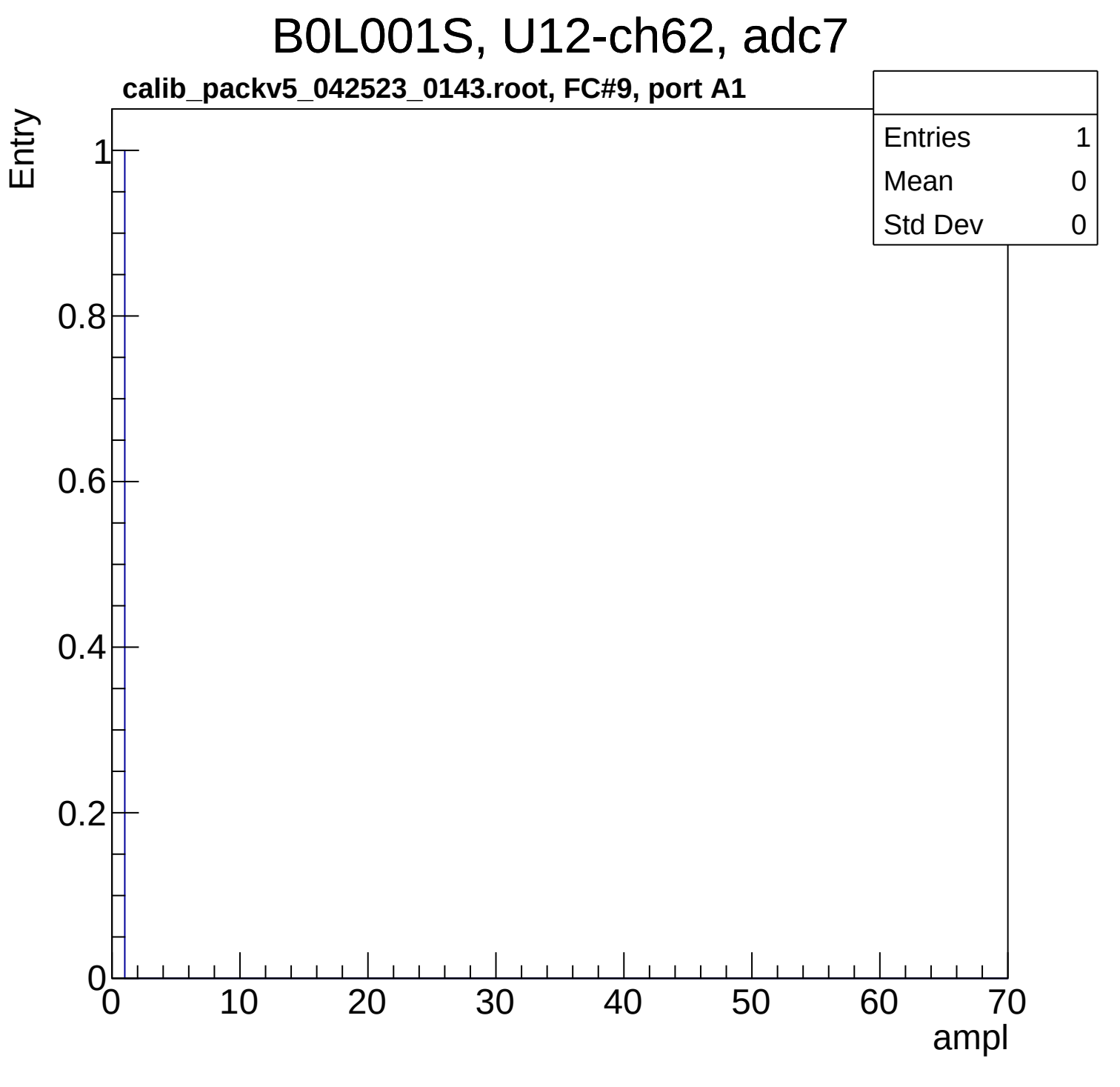
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch62, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 0
Std Dev 0
Entry
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0.8
0.6
0.4
0.2
0
0
10
20
30
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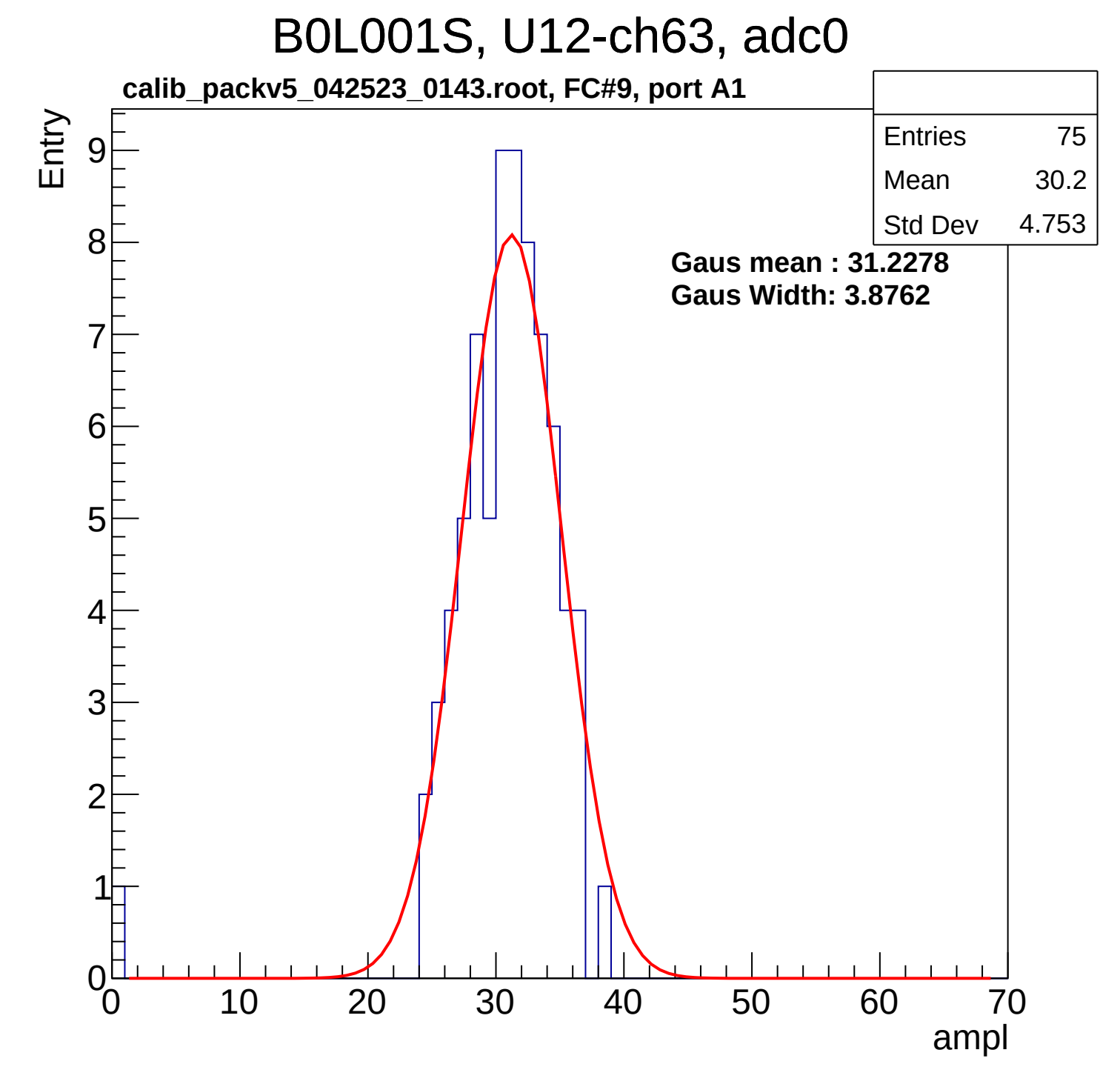
50
60
70
ampl


B0L001S, U12-ch63, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 75
Mean 30.2
Std Dev 4.753
Gaus mean : 31.2278
Gaus Width: 3.8762
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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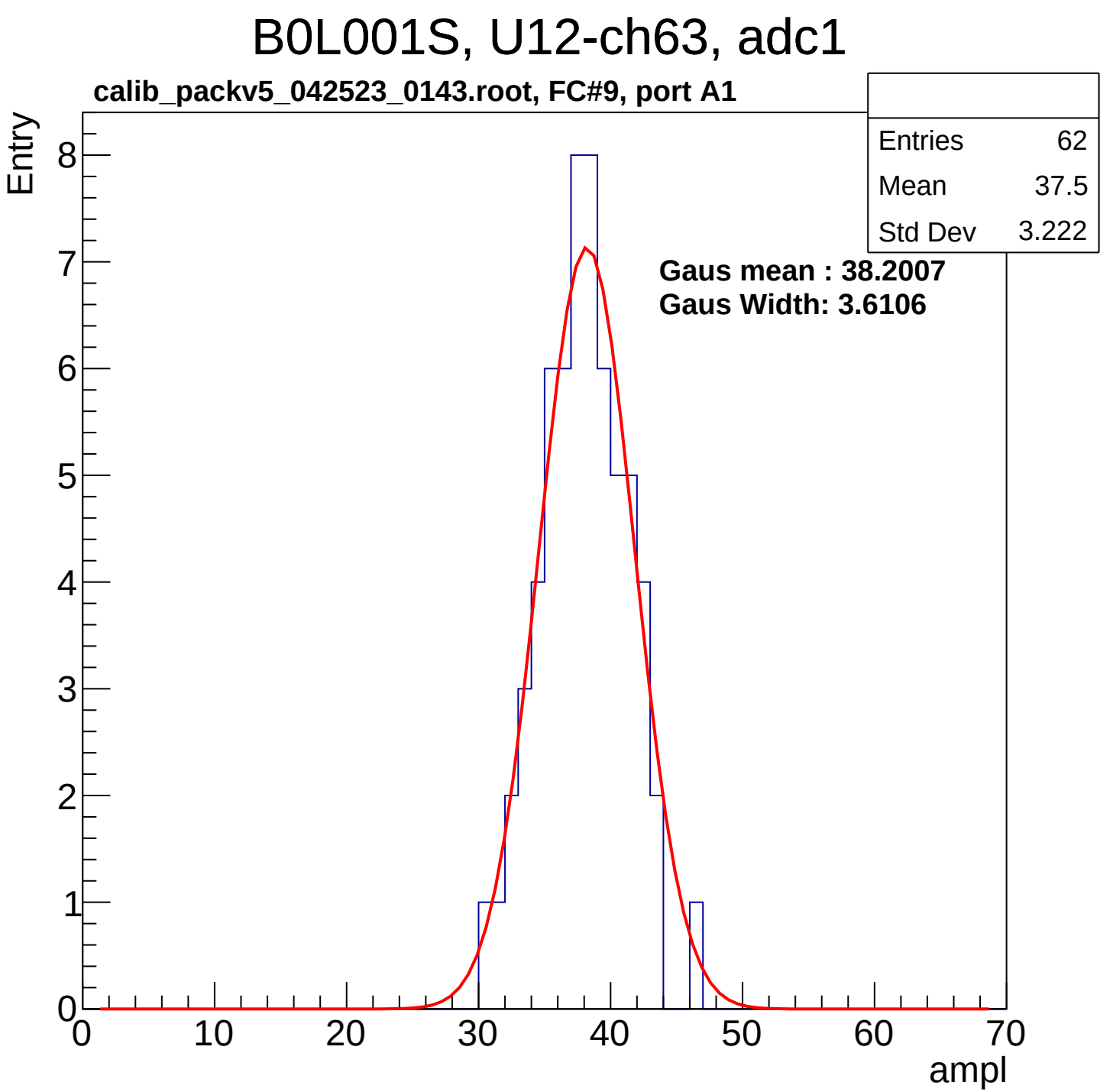
B0L001S, U12-ch63, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 62
Mean 37.5
Std Dev 3.222
Gaus mean : 38.2007
Gaus Width: 3.6106
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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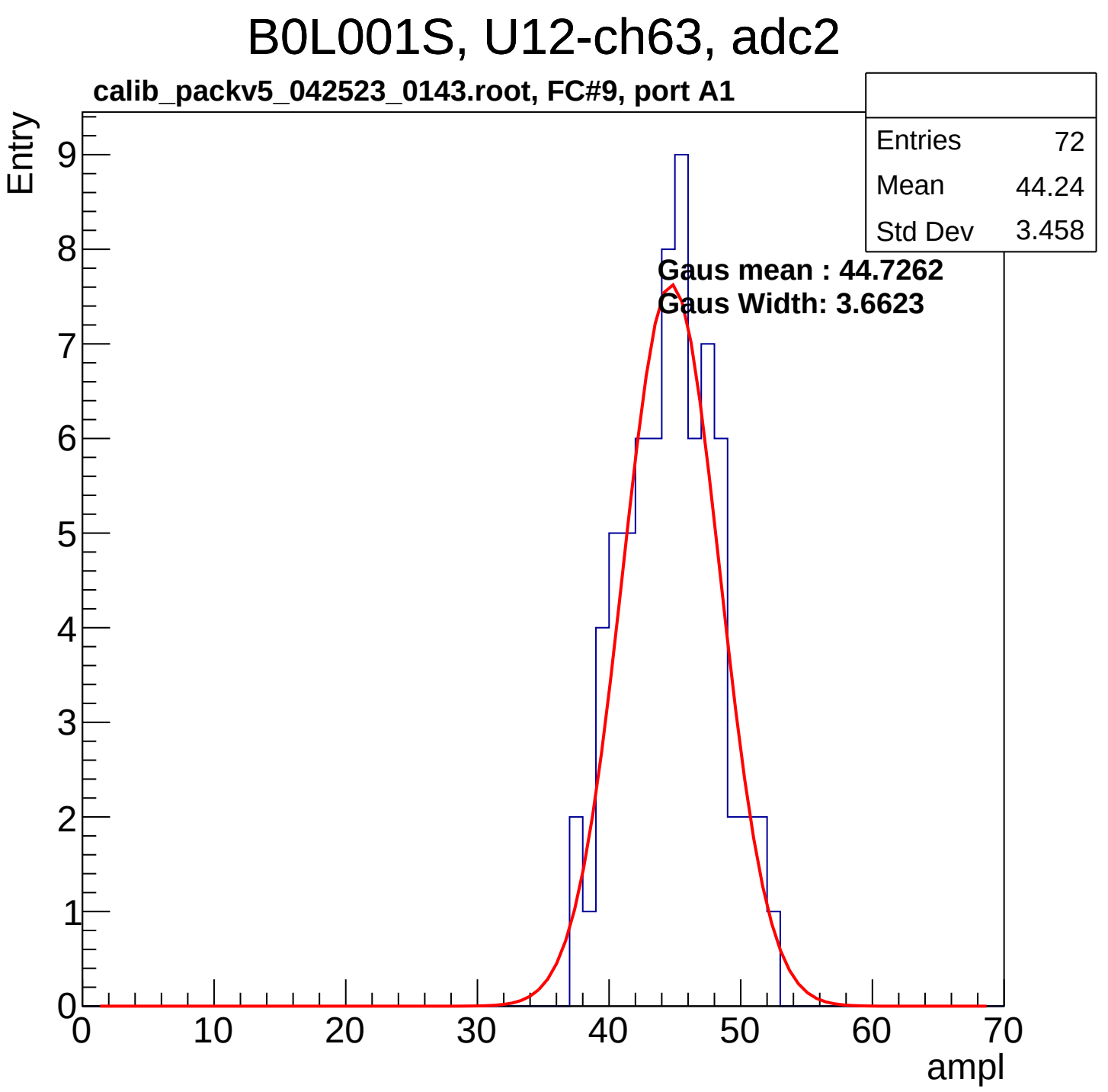
B0L001S, U12-ch63, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 72
Mean 44.24
Std Dev 3.458
Gaus mean : 44.7262
Gaus Width: 3.6623
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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60
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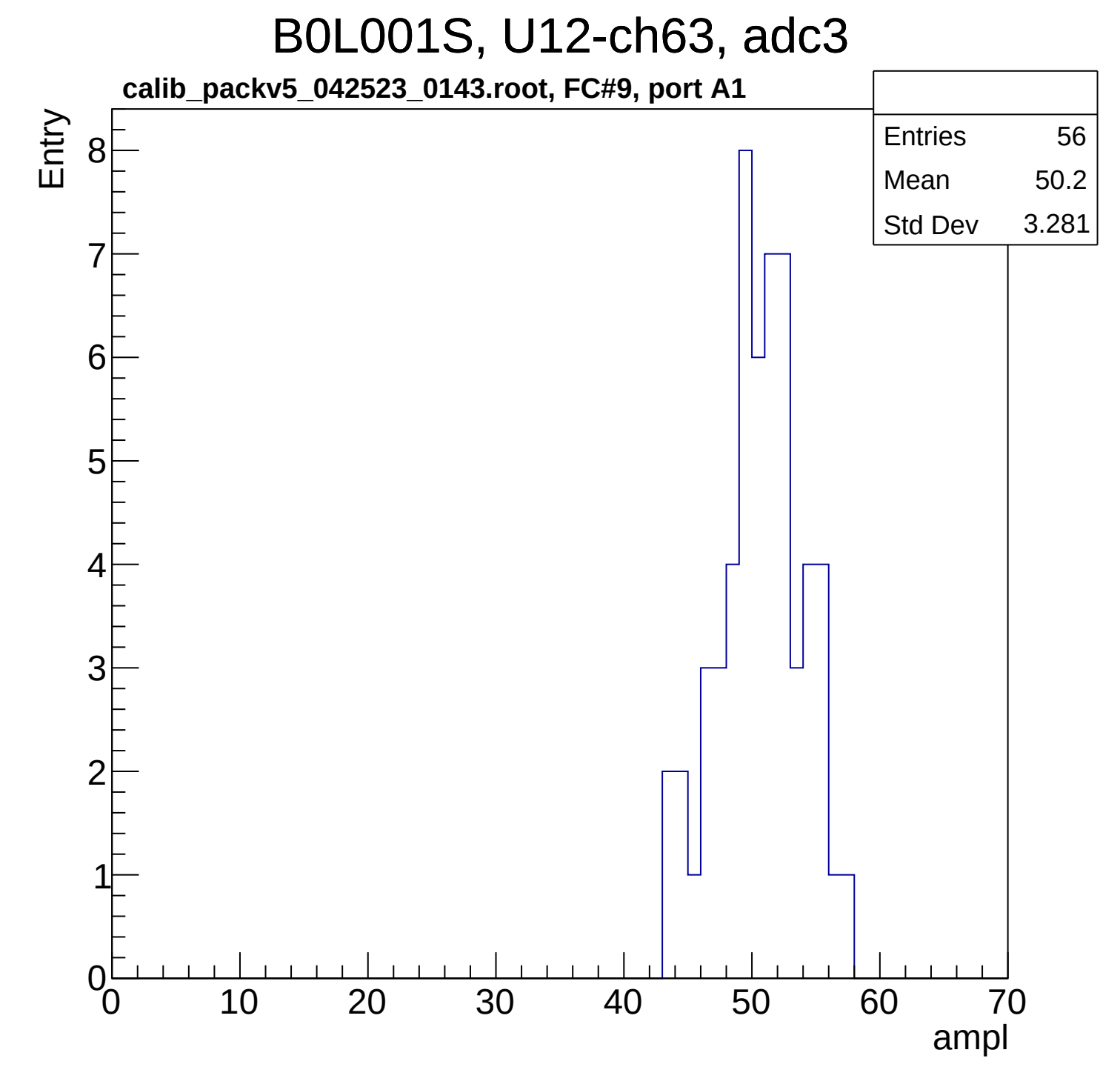
B0L001S, U12-ch63, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 56
Mean 50.2
Std Dev 3.281
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
50
60
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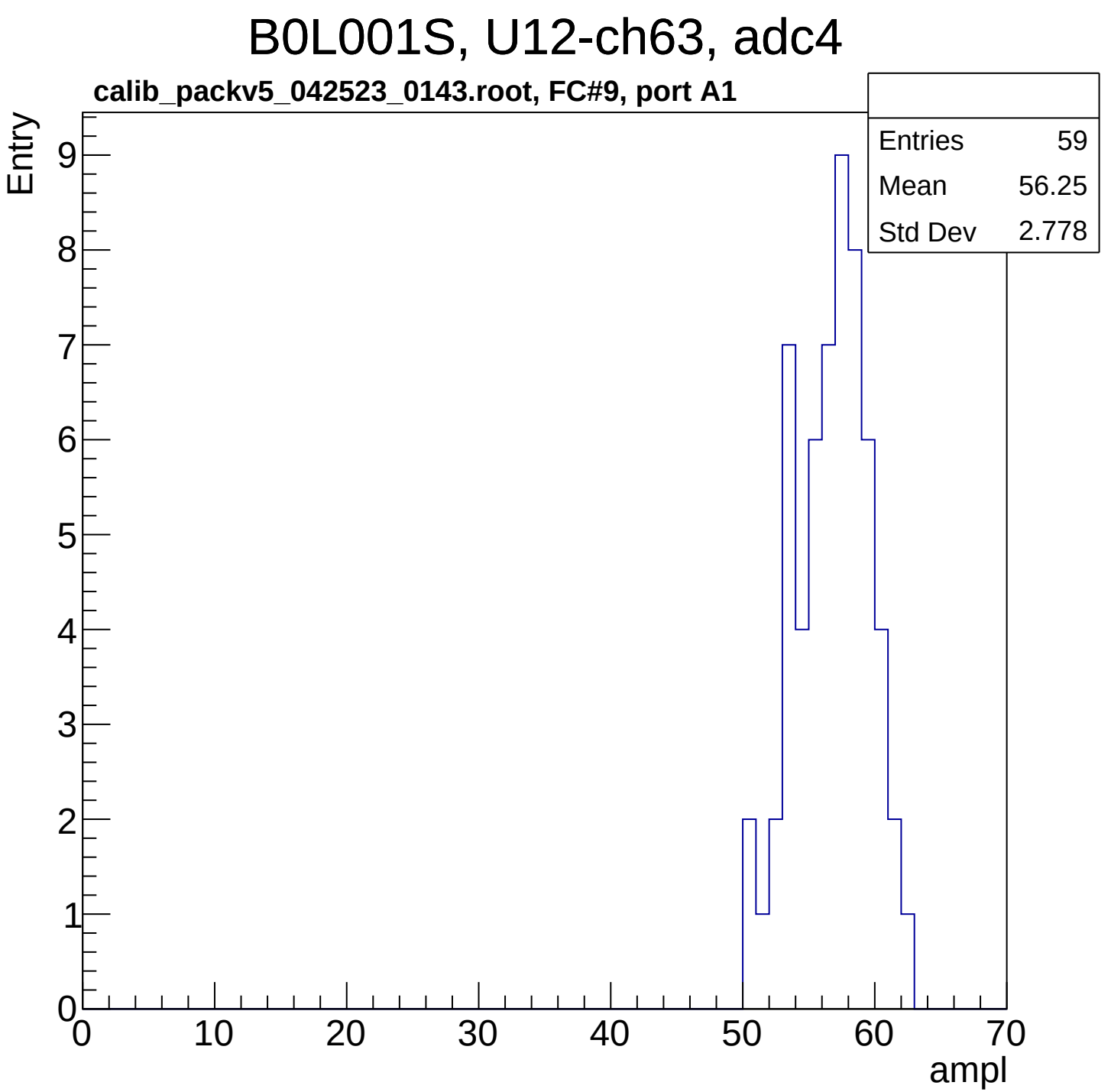
B0L001S, U12-ch63, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 59
Mean 56.25
Std Dev 2.778
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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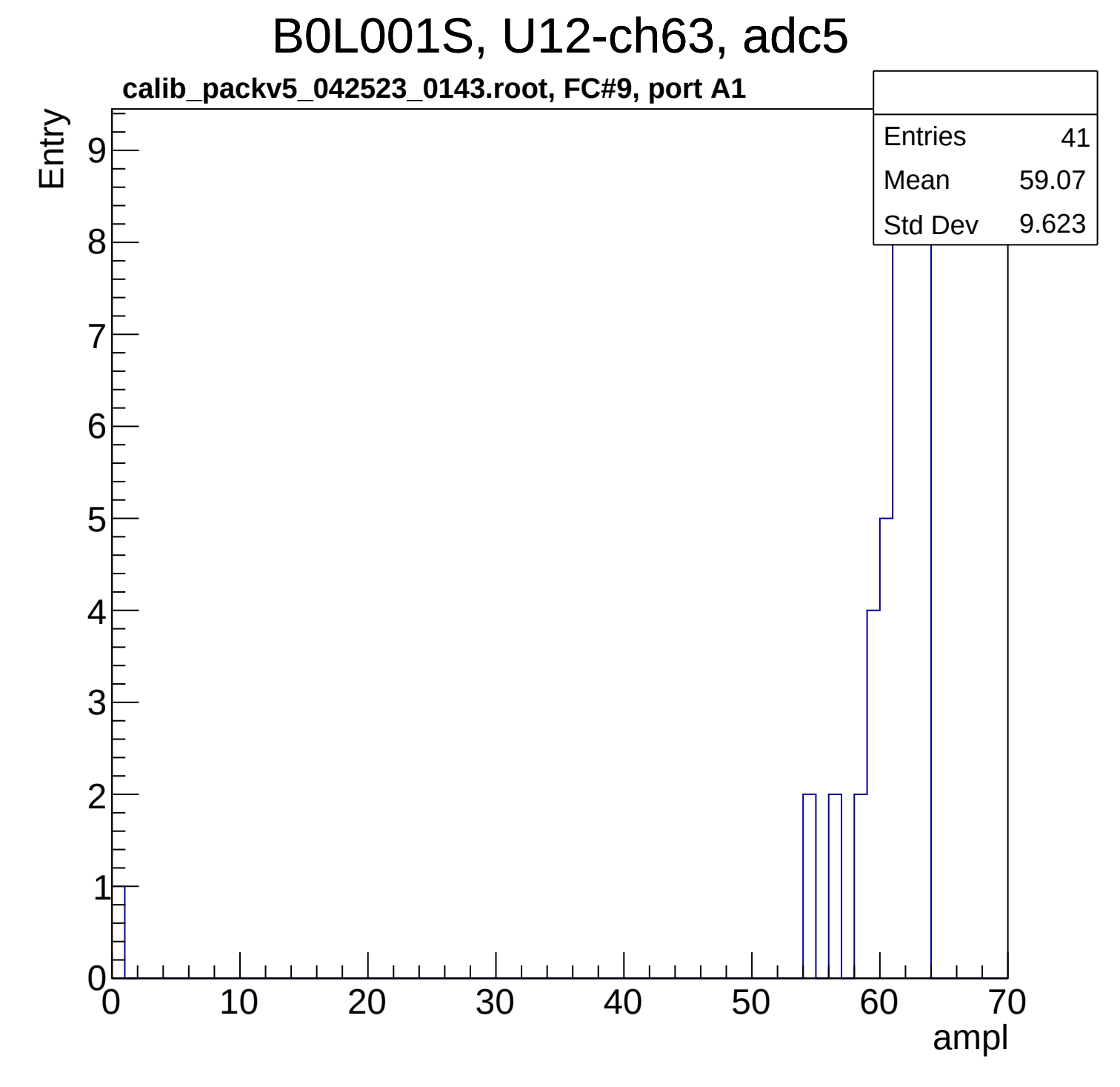
B0L001S, U12-ch63, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 41
Mean 59.07
Std Dev 9.623
Entry
ampl
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3
4
5
6
7
8
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0
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60
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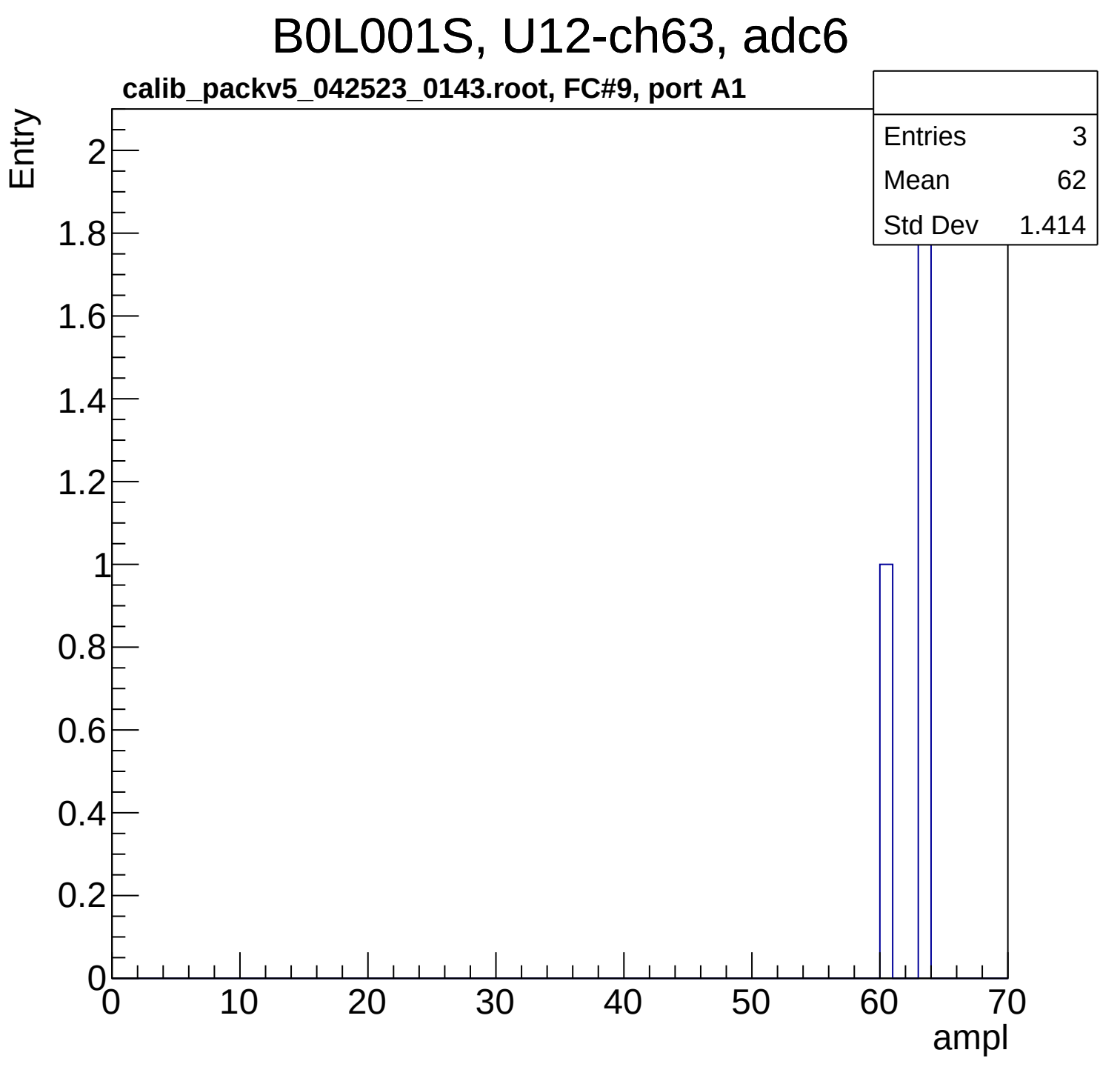
B0L001S, U12-ch63, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 3
Mean 62
Std Dev 1.414
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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40
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60
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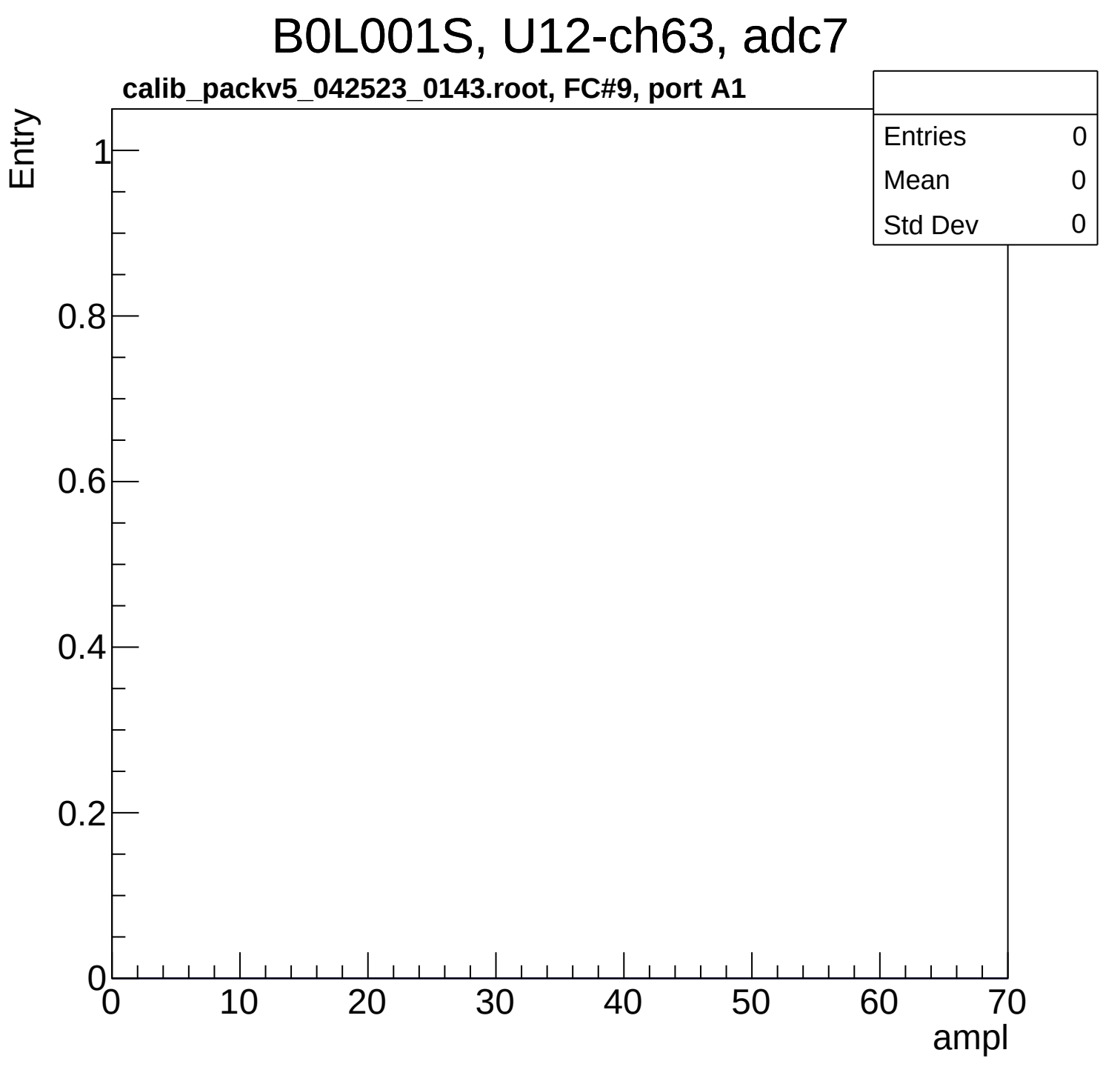
B0L001S, U12-ch63, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
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0.6
0.4
0.2
0
0
10
20
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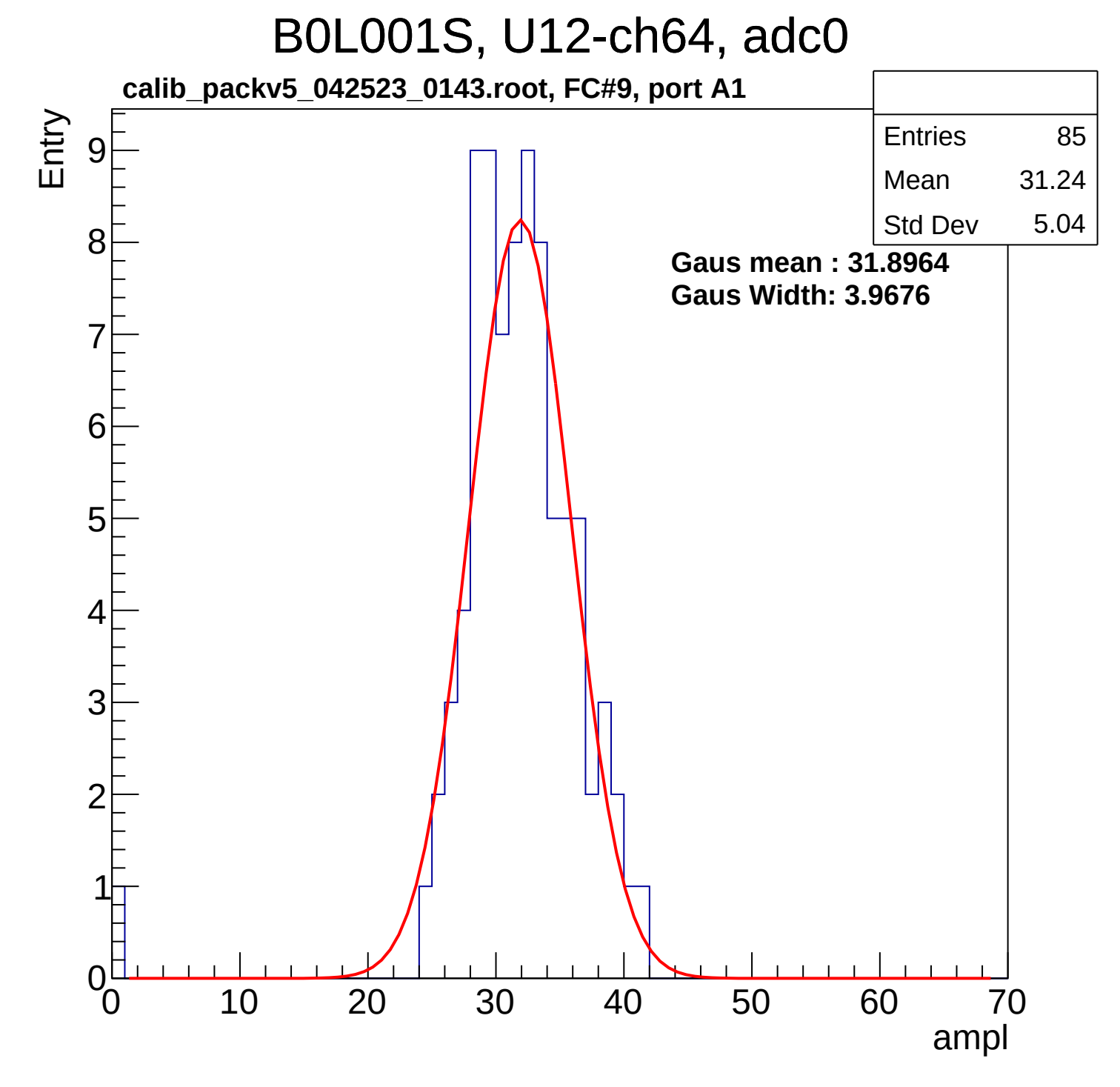
50
60
70
ampl


B0L001S, U12-ch64, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 85
Mean 31.24
Std Dev 5.04
Gaus mean : 31.8964
Gaus Width: 3.9676
Entry
ampl
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3
4
5
6
7
8
9
0
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60
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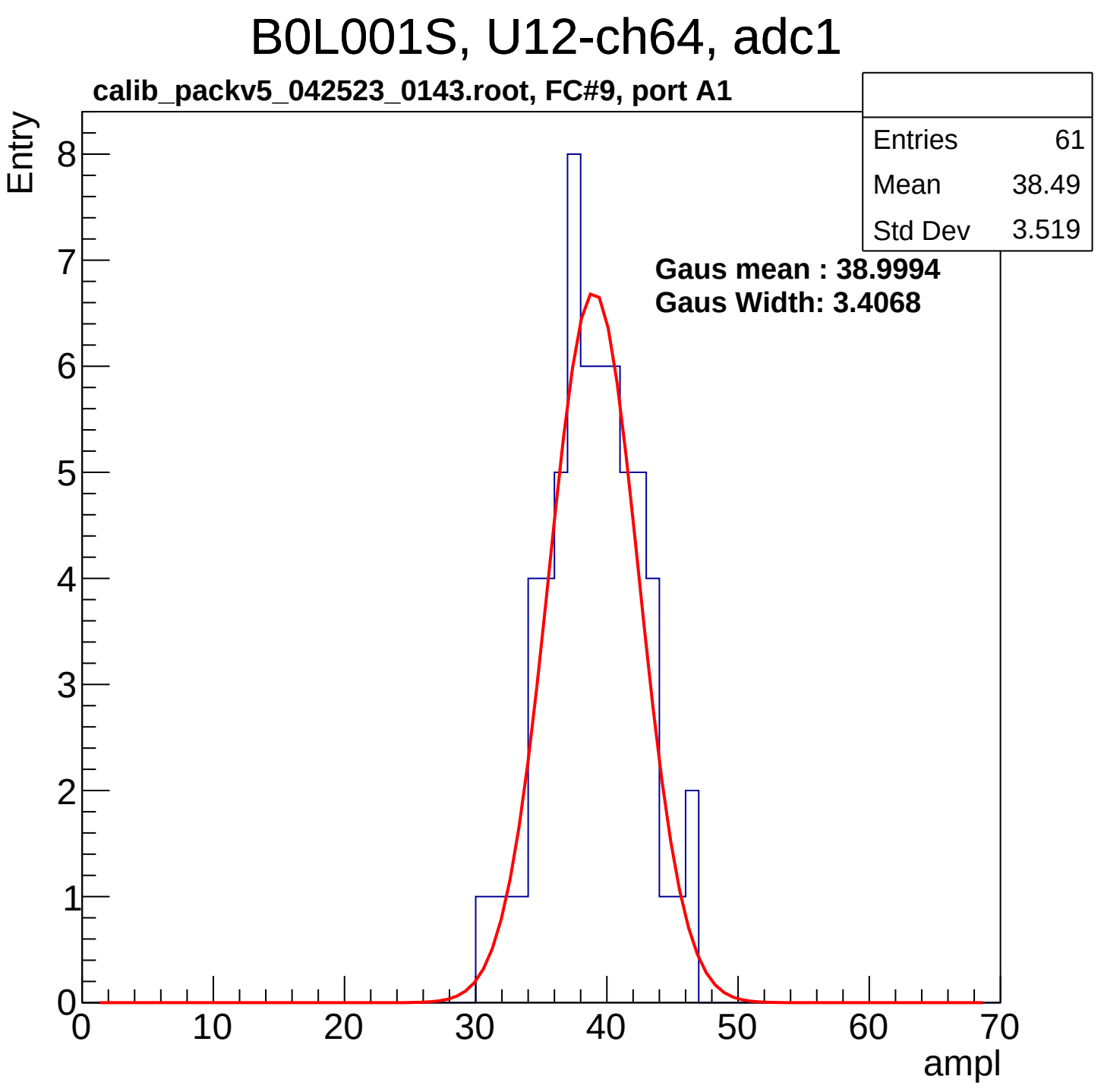
B0L001S, U12-ch64, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 61
Mean 38.49
Std Dev 3.519
Gaus mean : 38.9994
Gaus Width: 3.4068
Entry
ampl
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1
2
3
4
5
6
7
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0
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40
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60
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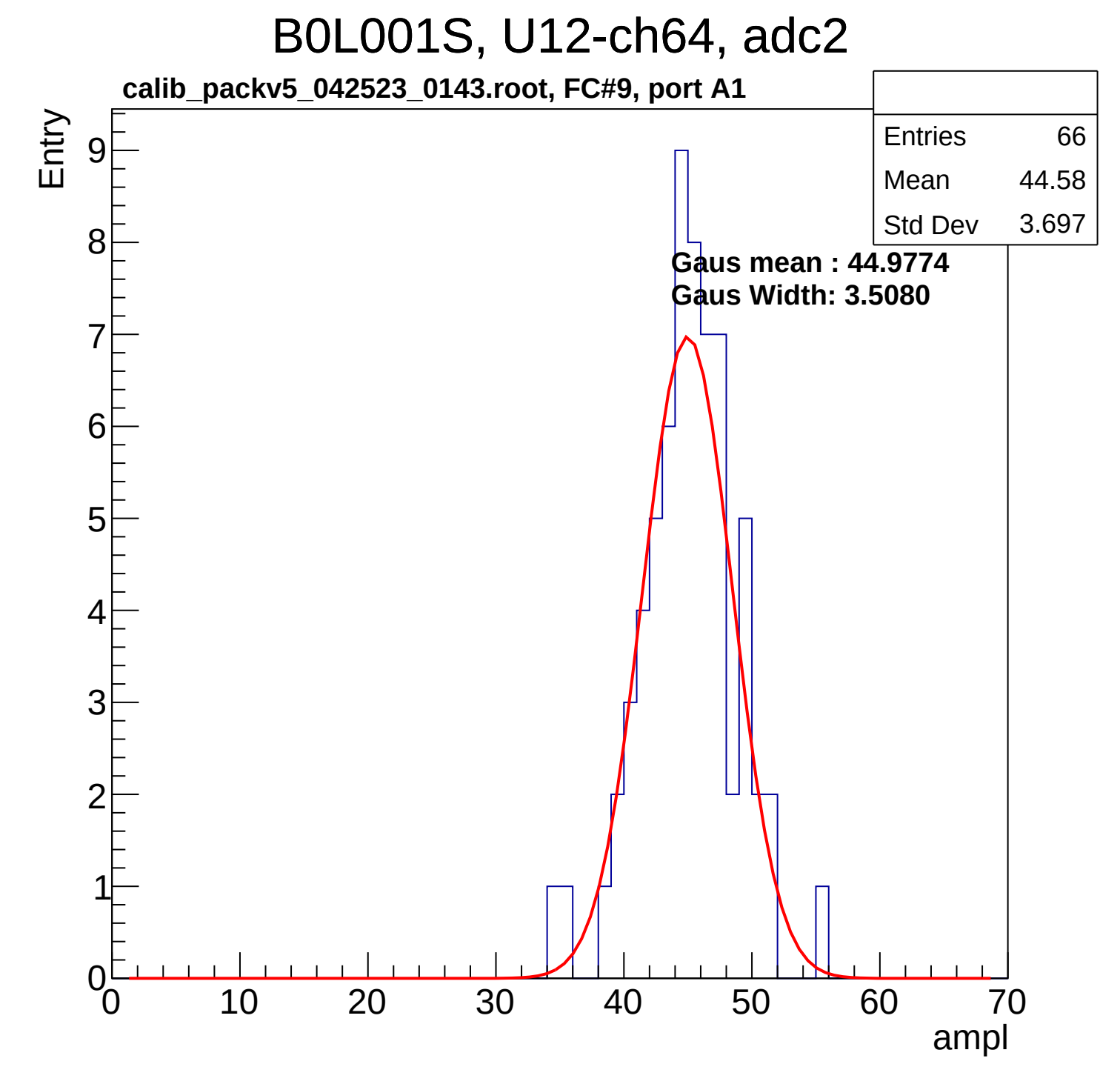
B0L001S, U12-ch64, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 66
Mean 44.58
Std Dev 3.697
Gaus mean : 44.9774
Gaus Width: 3.5080
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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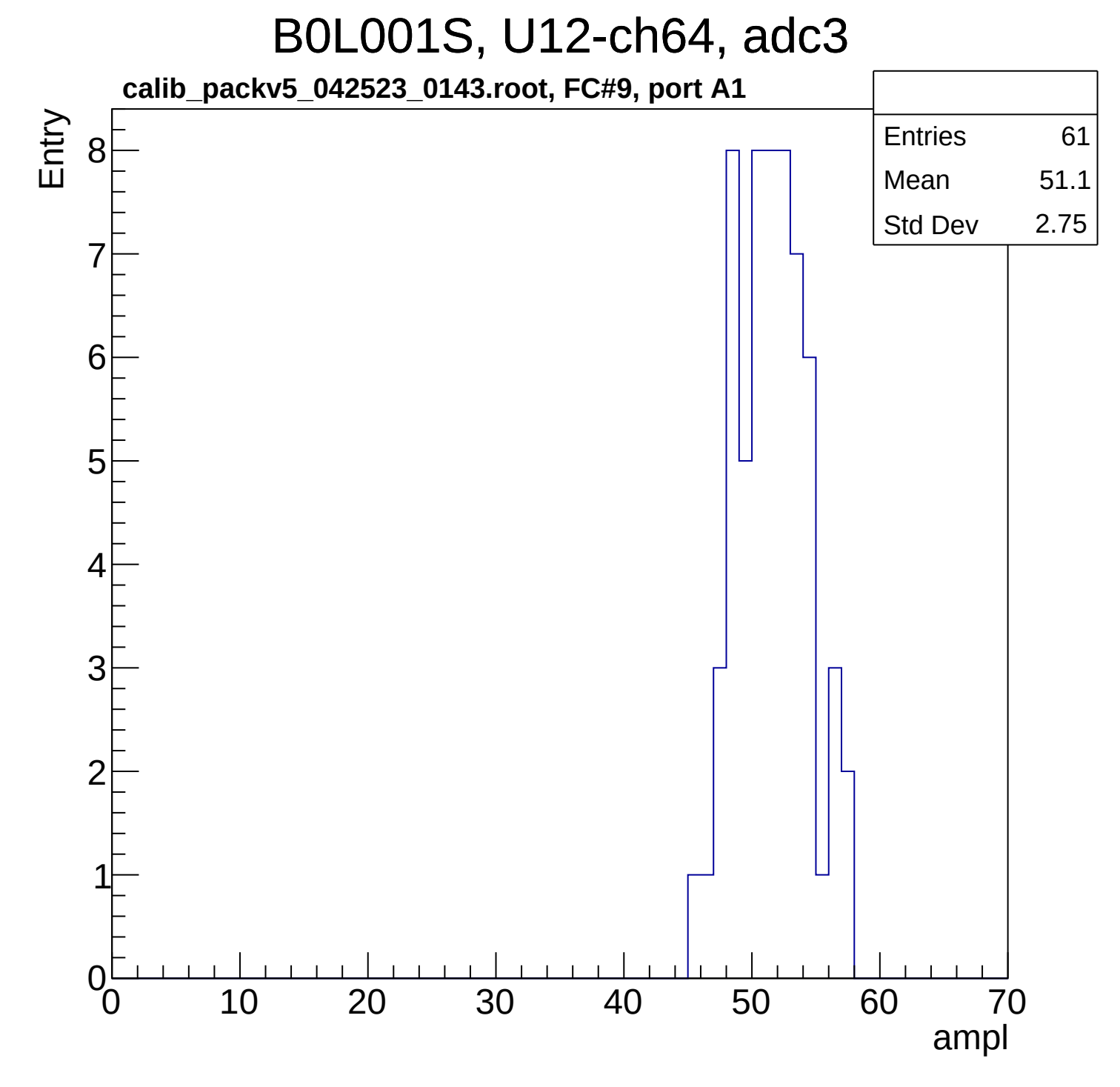
B0L001S, U12-ch64, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 61
Mean 51.1
Std Dev 2.75
Entry
ampl
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0
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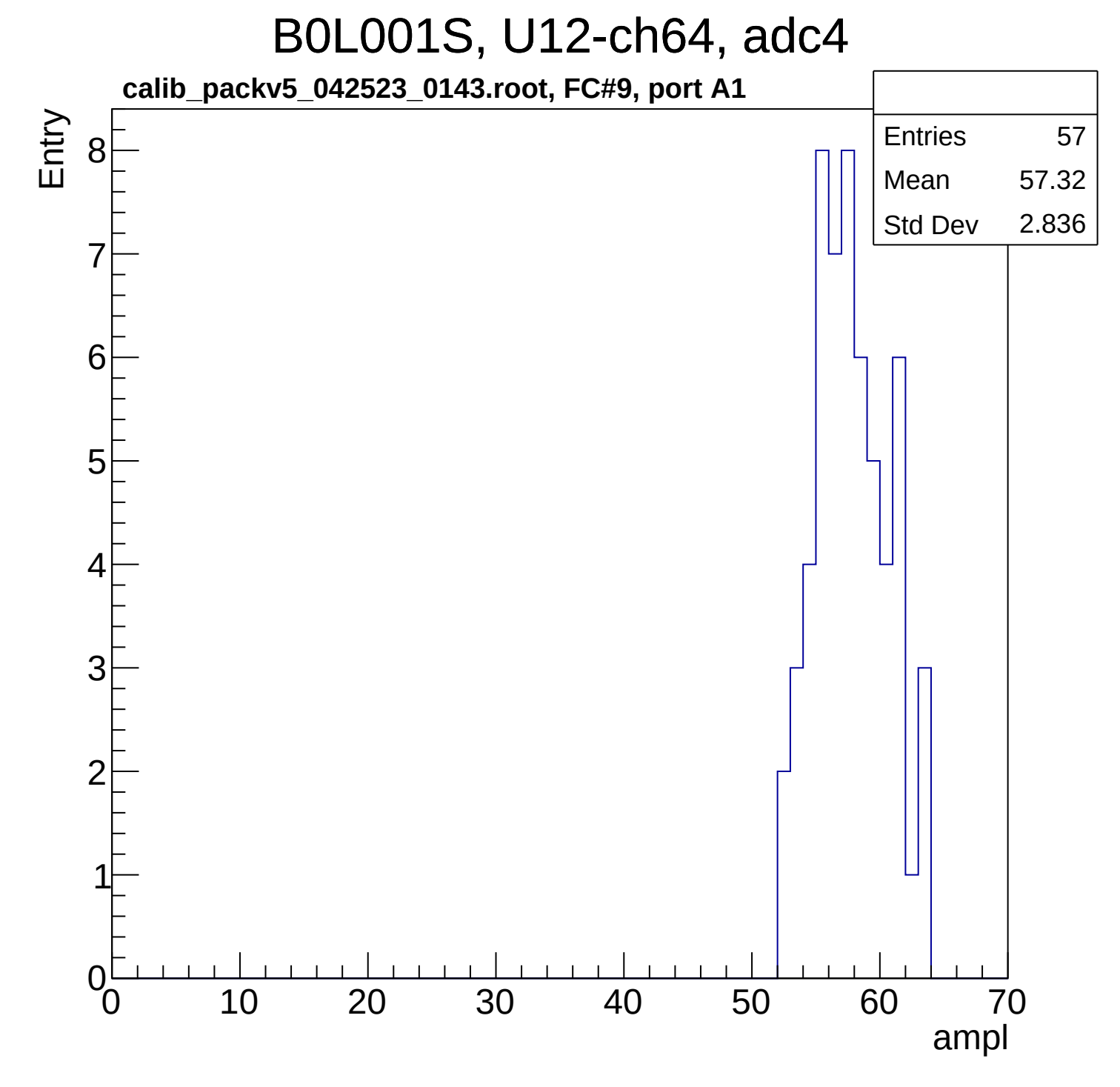
B0L001S, U12-ch64, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 57
Mean 57.32
Std Dev 2.836
Entry
ampl
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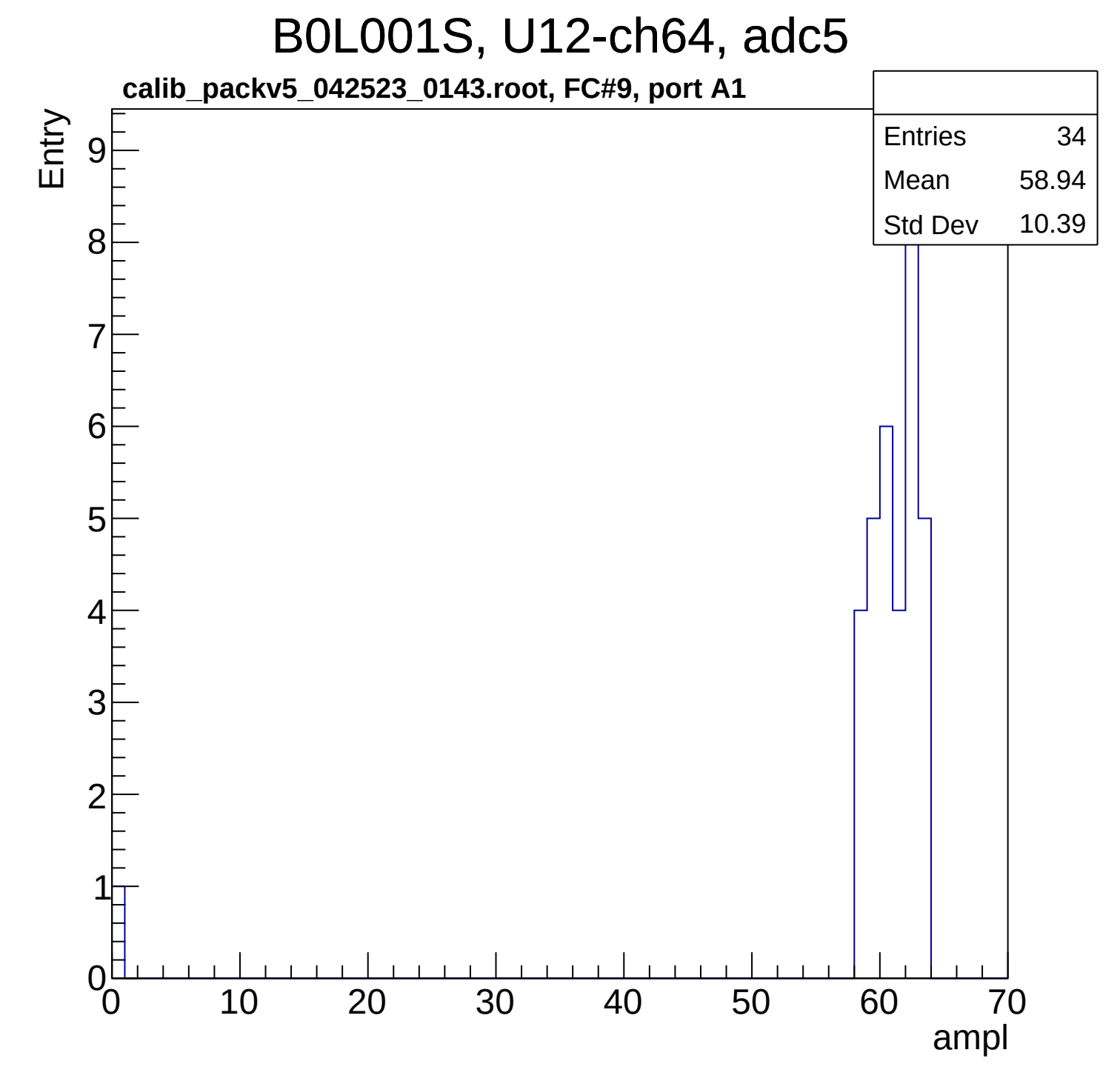
B0L001S, U12-ch64, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 34
Mean 58.94
Std Dev 10.39
Entry
ampl
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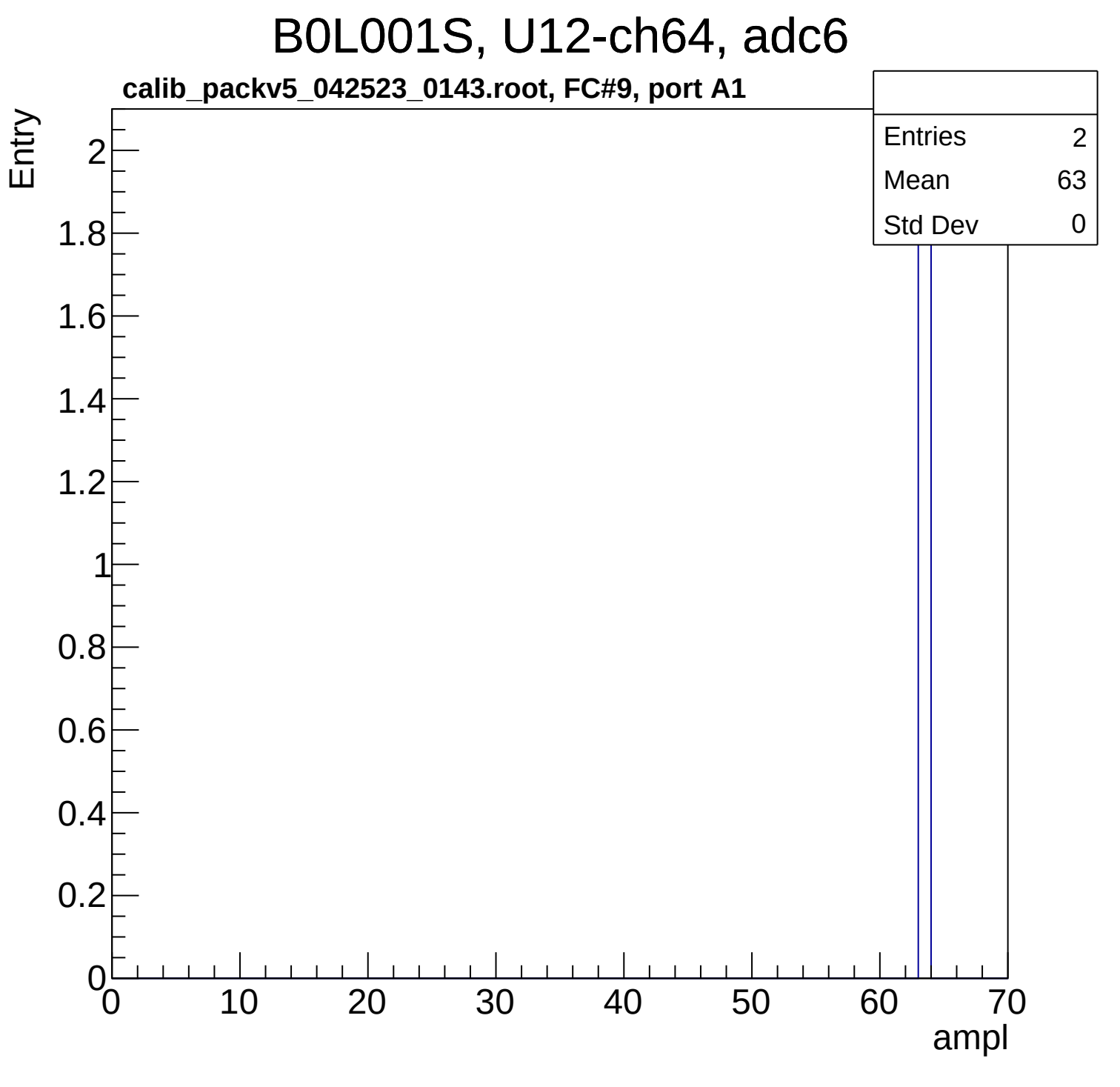
B0L001S, U12-ch64, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
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1.2
1.4
1.6
1.8
2
0
10
20
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40
50
60
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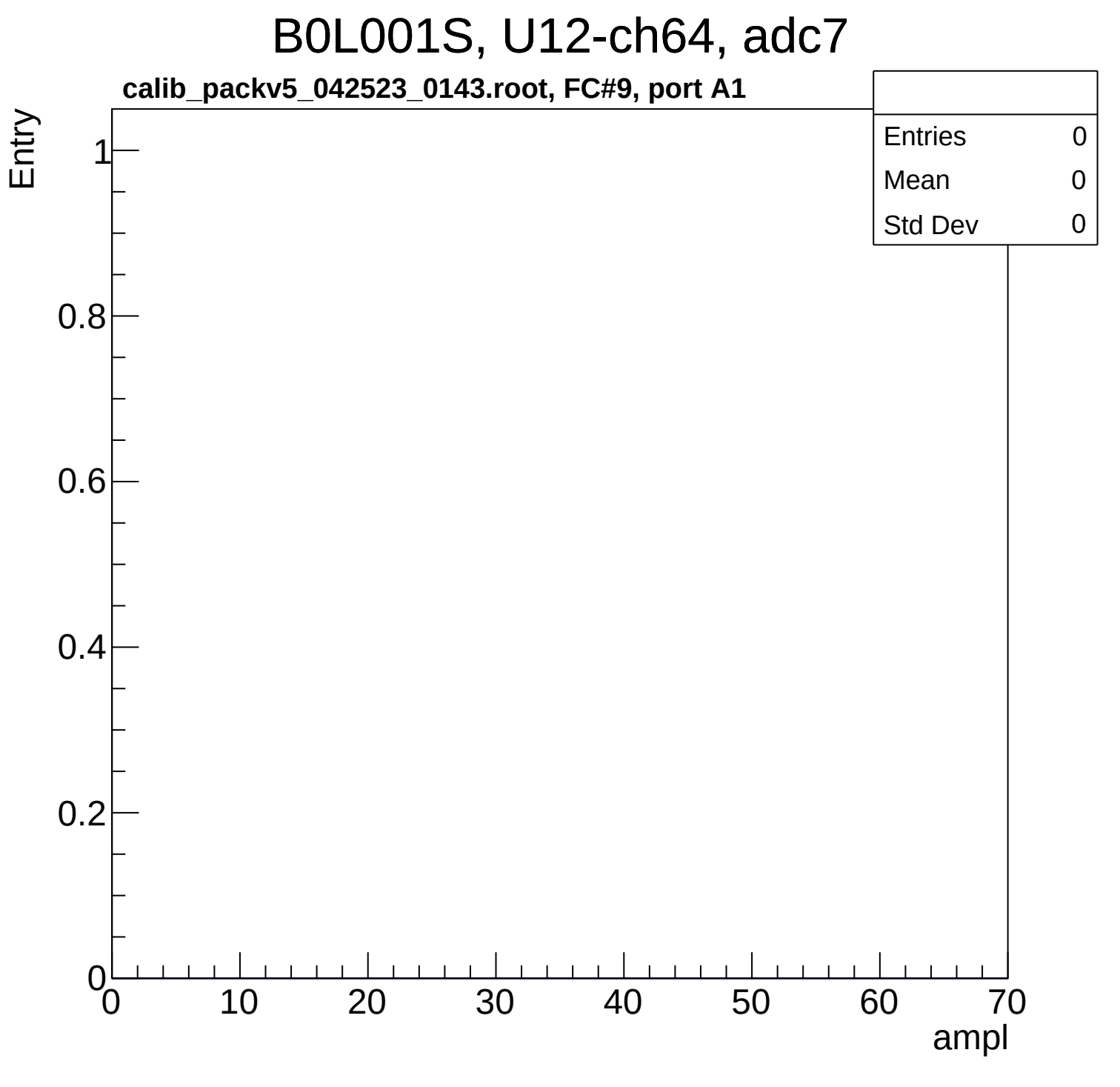
B0L001S, U12-ch64, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
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0.6
0.4
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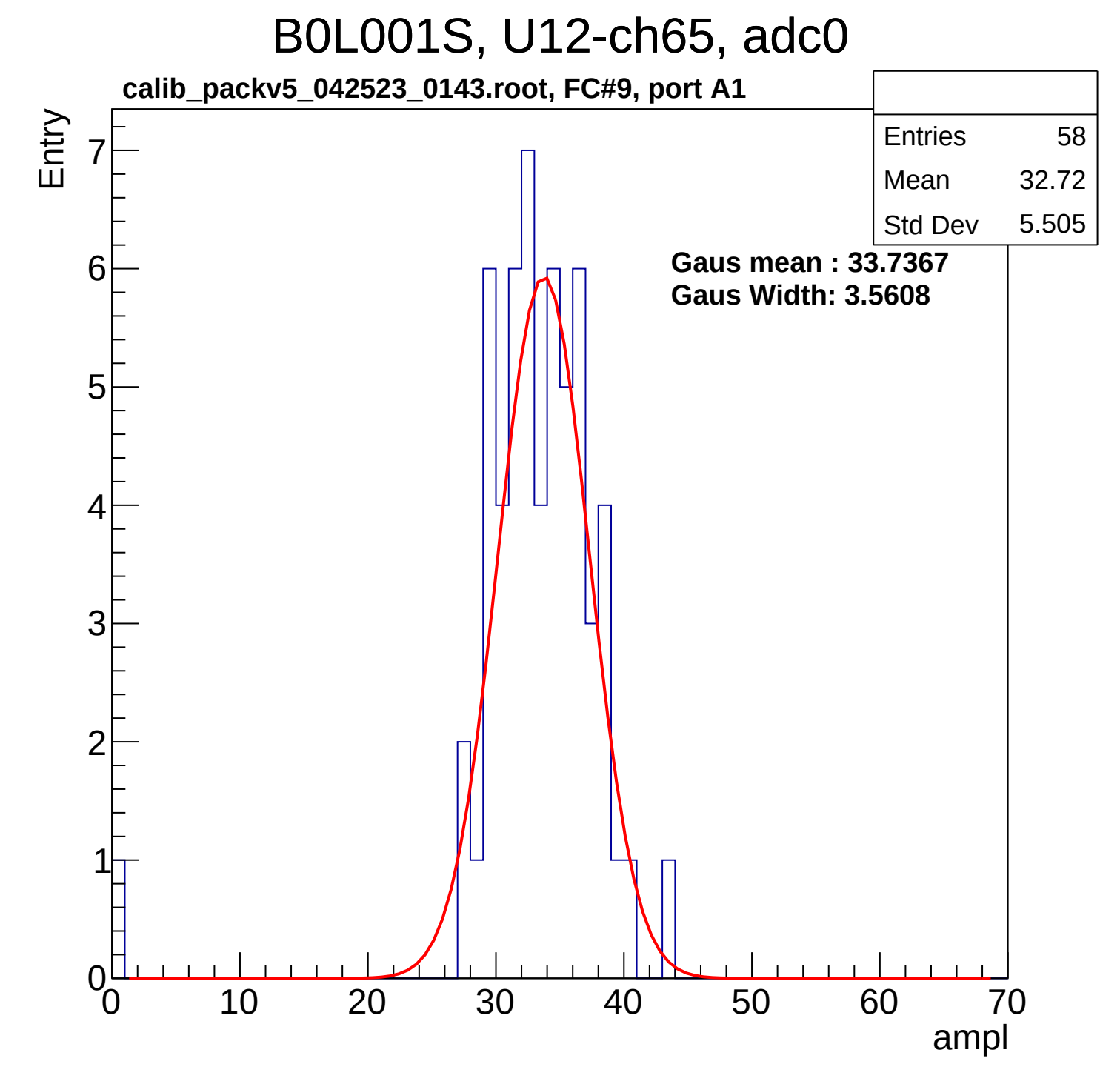
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch65, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 58
Mean 32.72
Std Dev 5.505
Gaus mean : 33.7367
Gaus Width: 3.5608
Entry
ampl
0
1
2
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7
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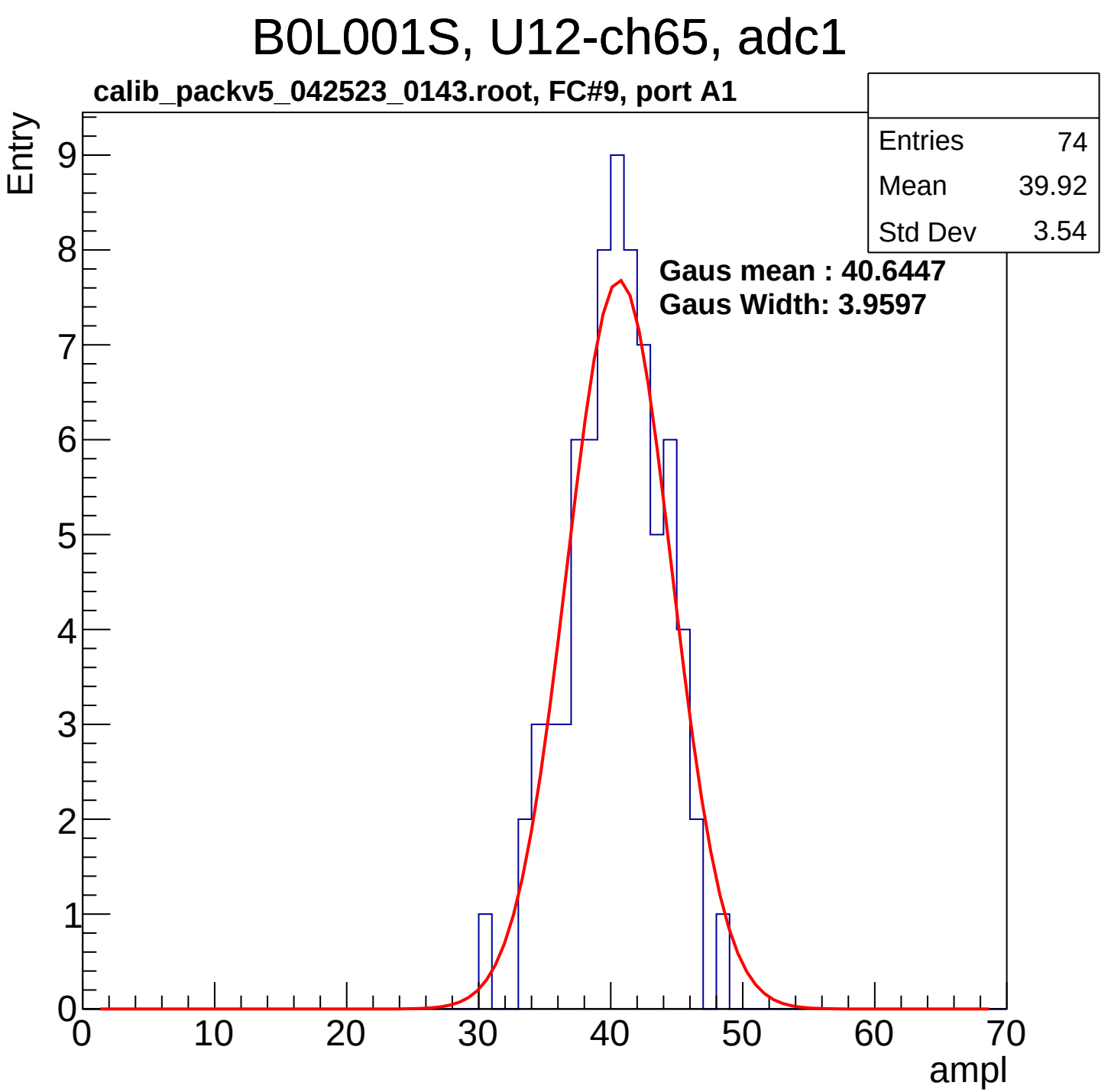
B0L001S, U12-ch65, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 74
Mean 39.92
Std Dev 3.54
Gaus mean : 40.6447
Gaus Width: 3.9597
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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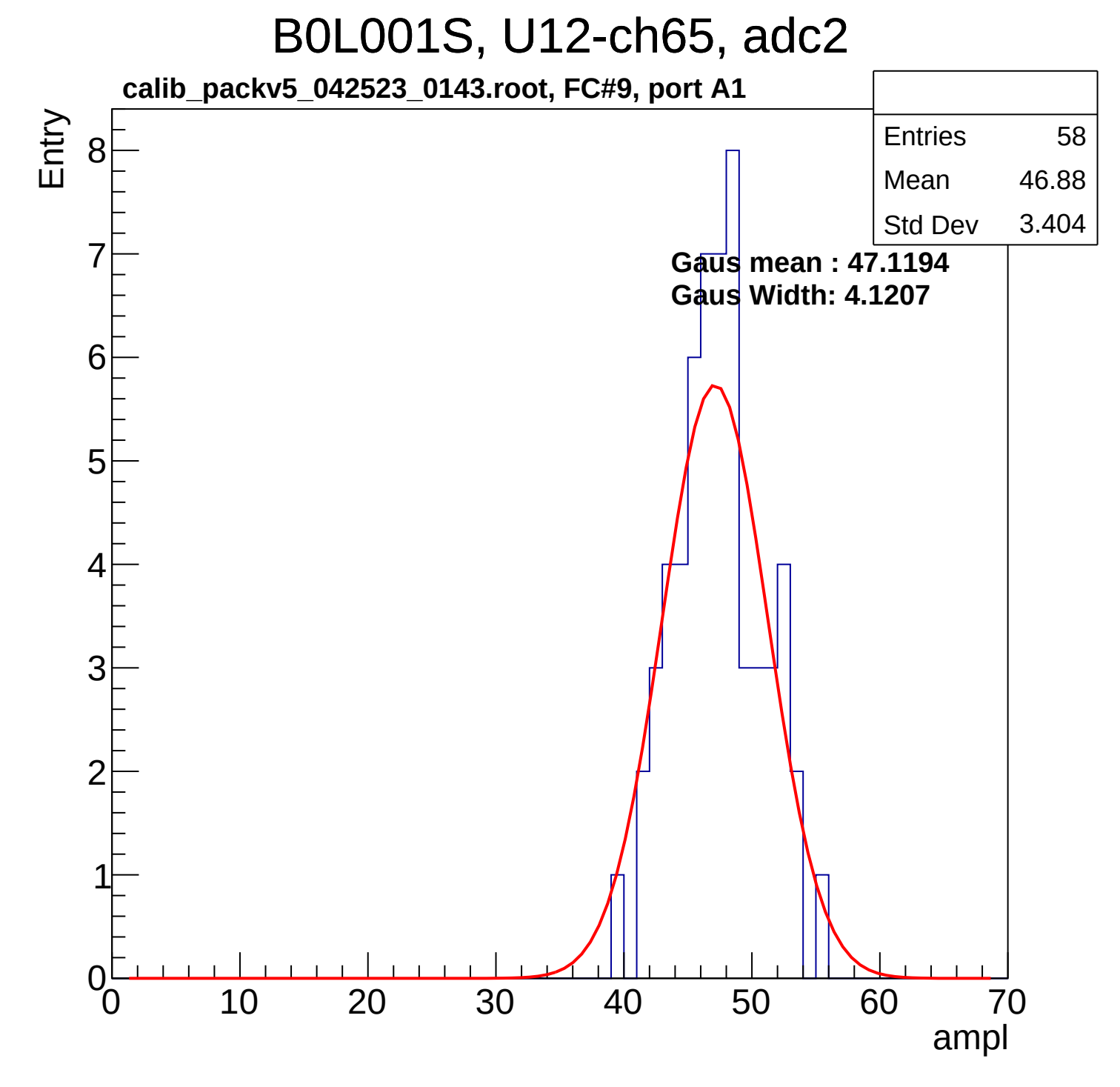
B0L001S, U12-ch65, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 58
Mean 46.88
Std Dev 3.404
Gaus mean : 47.1194
Gaus Width: 4.1207
Entry
ampl
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1
2
3
4
5
6
7
8
0
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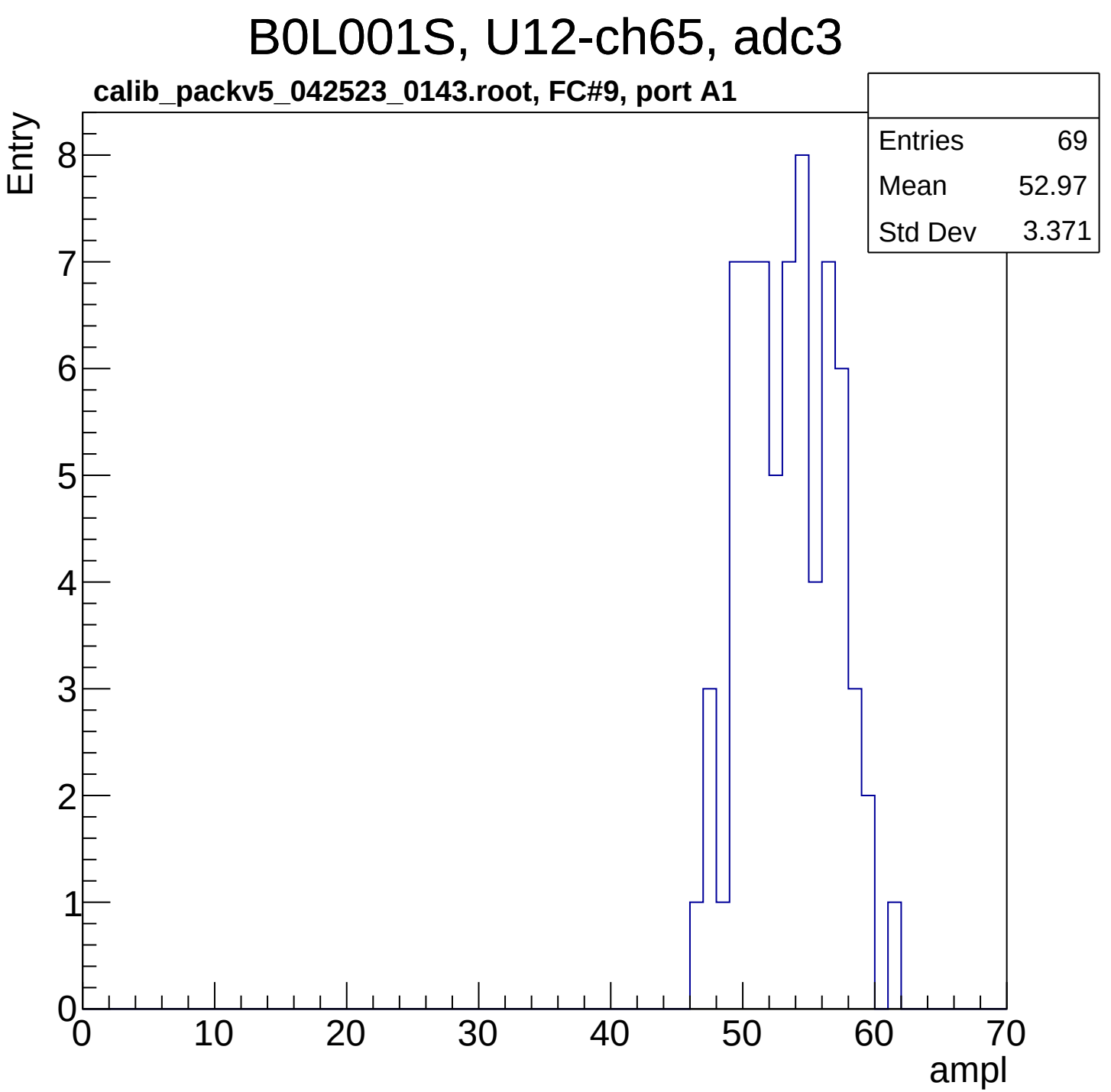
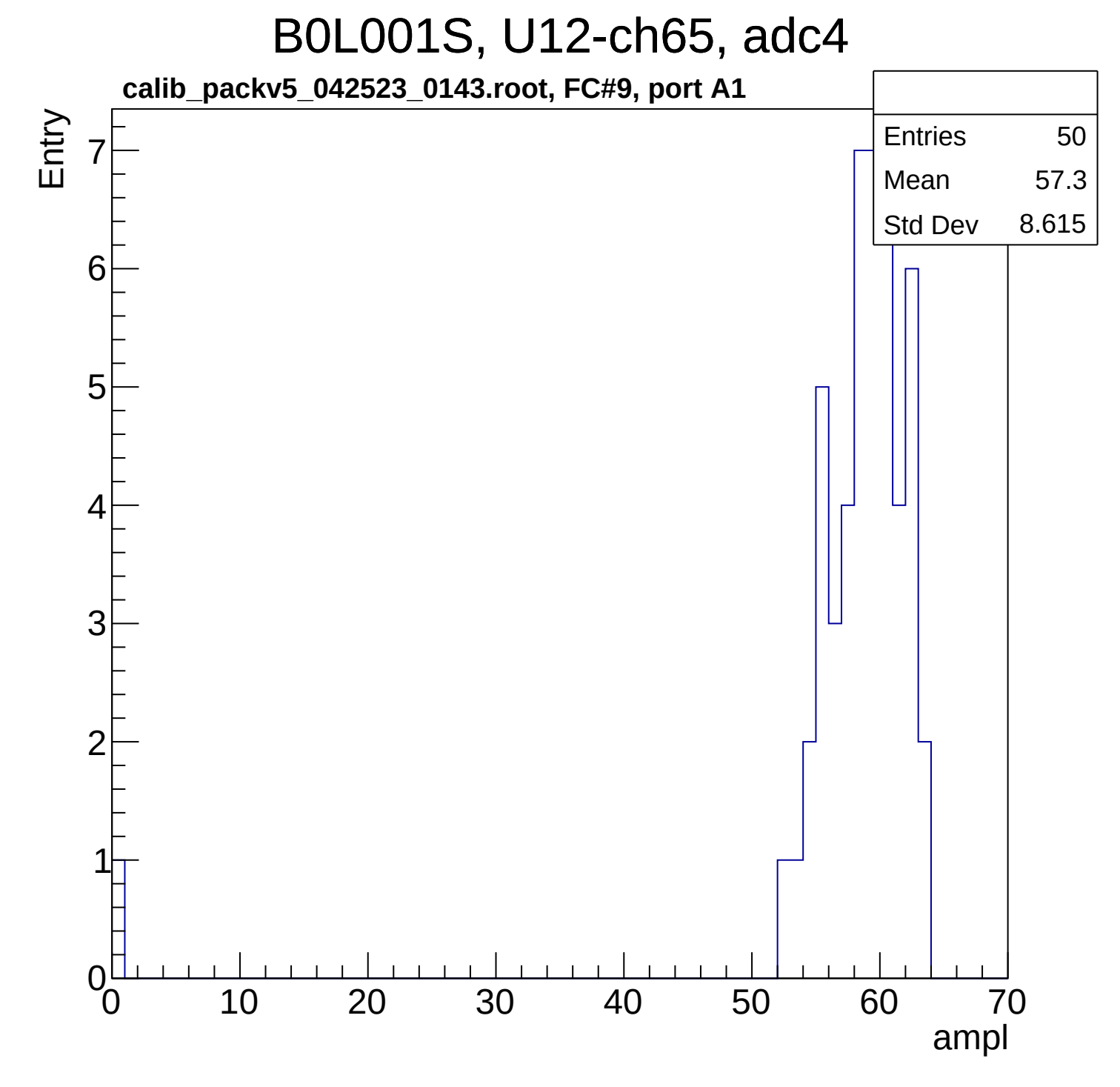
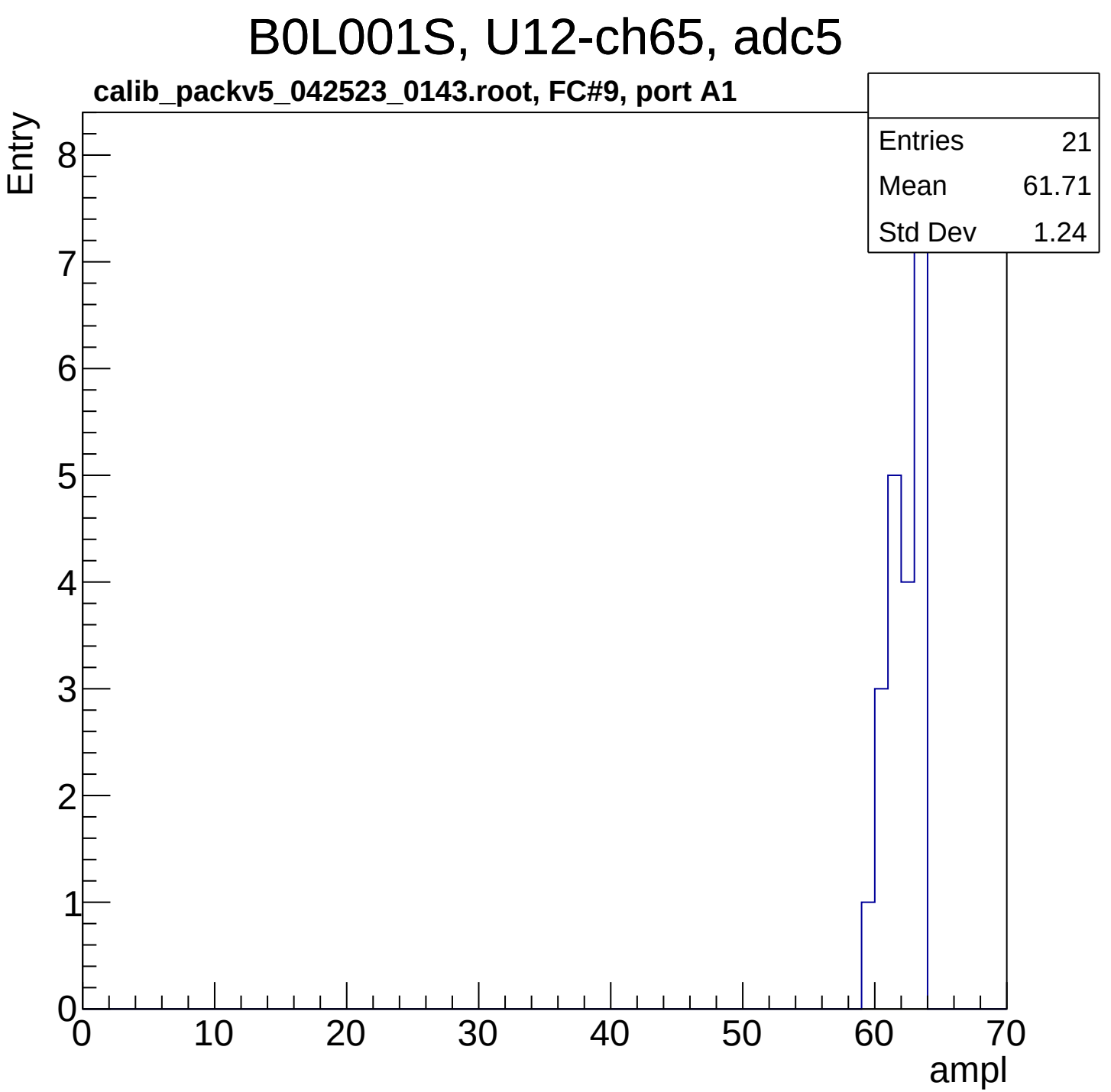
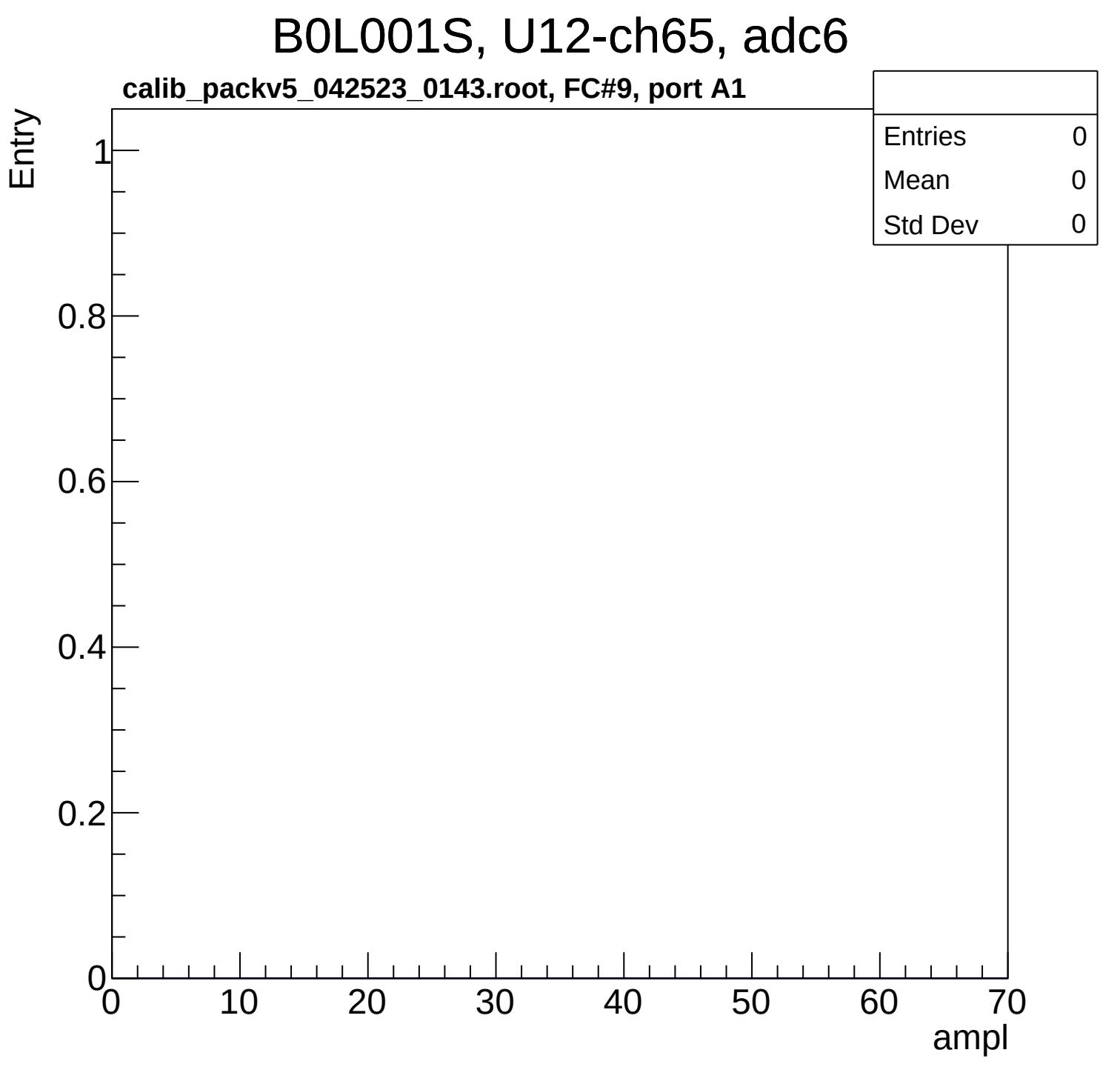
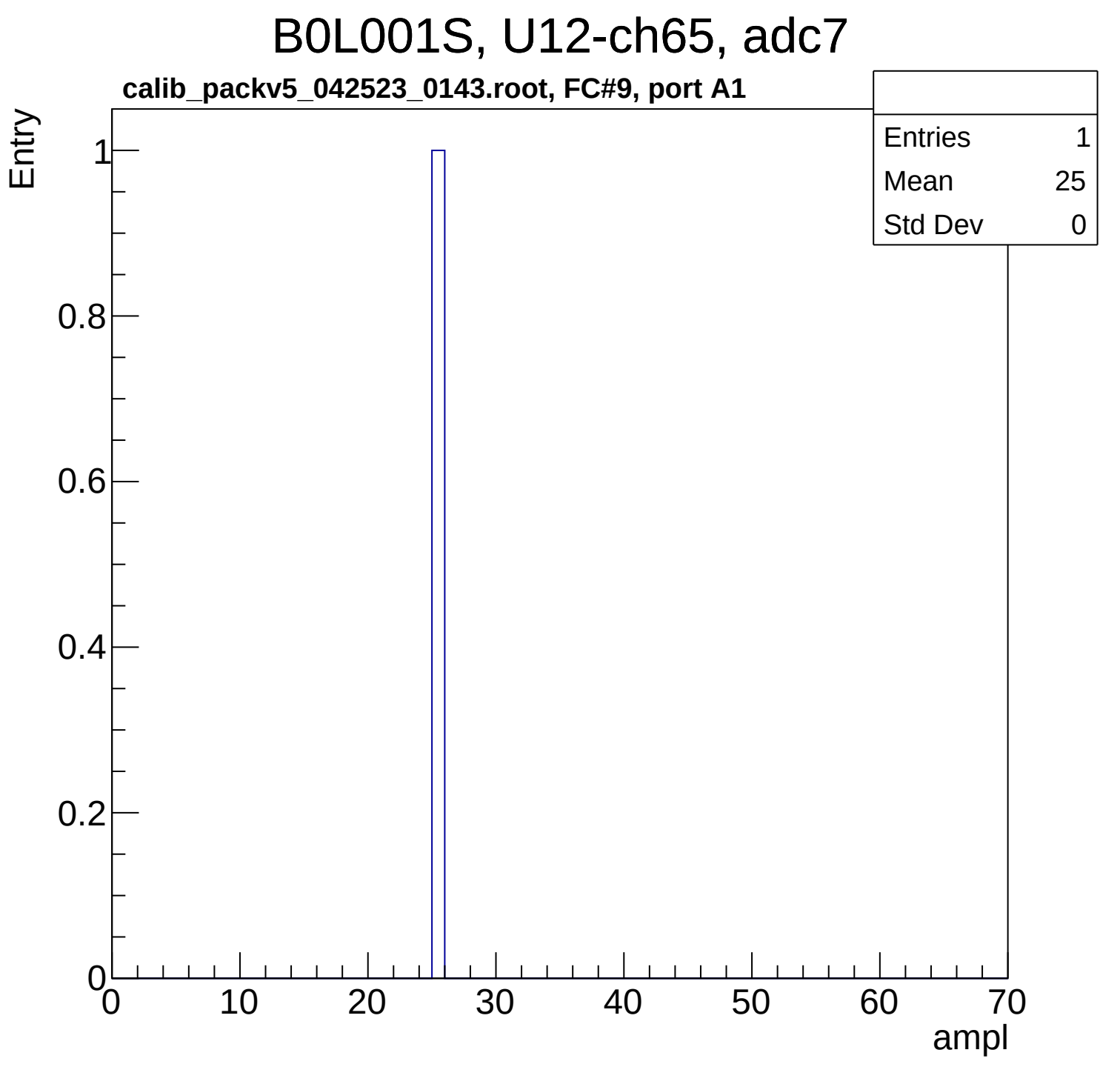

B0L001S, U12-ch65, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 69
Mean 52.97
Std Dev 3.371
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch65, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 50
Mean 57.3
Std Dev 8.615
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B0L001S, U12-ch65, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 21
Mean 61.71
Std Dev 1.24
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch65, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch65, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 25
Std Dev 0
Entry
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0.8
0.6
0.4
0.2
0
0
10
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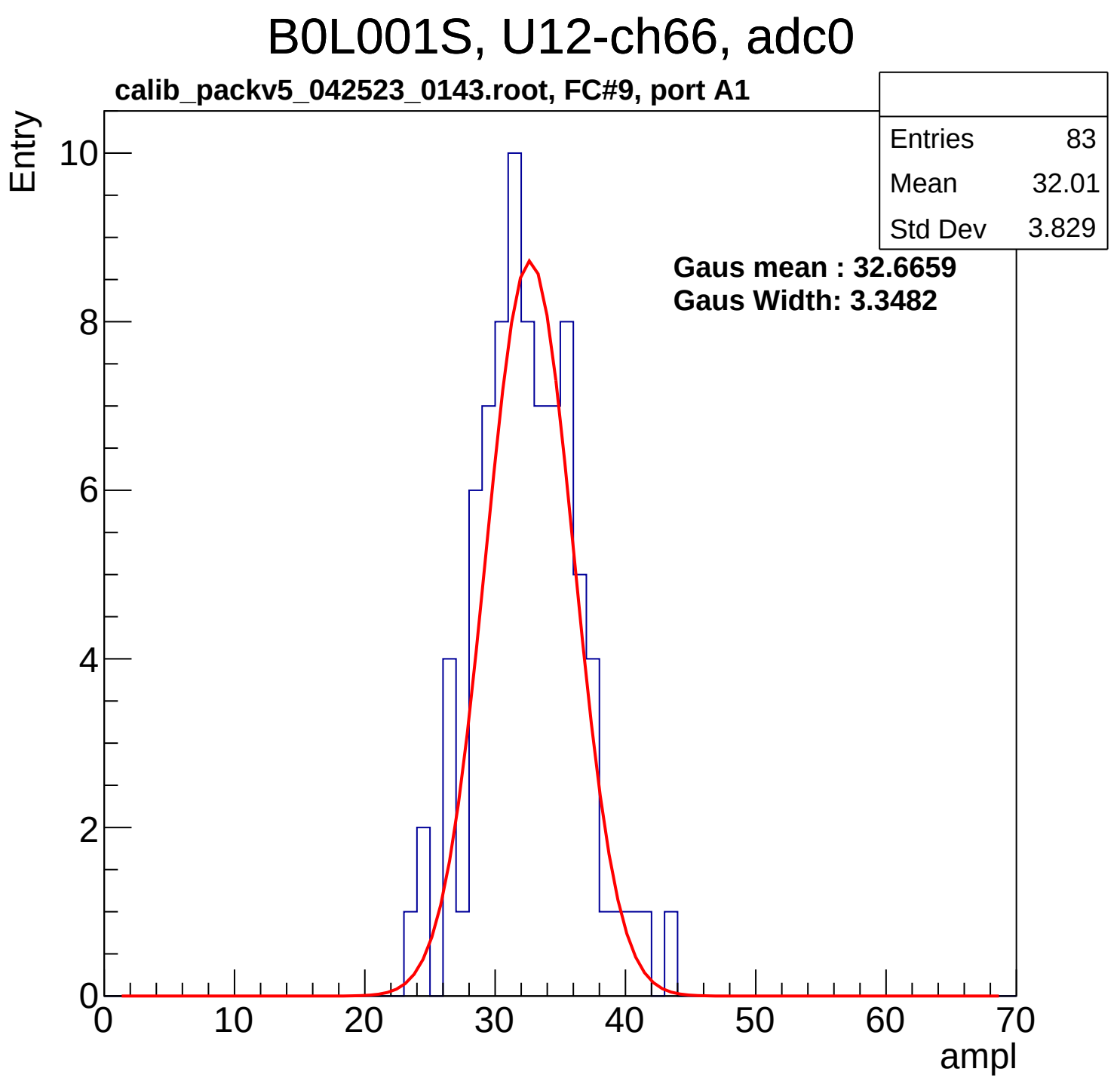
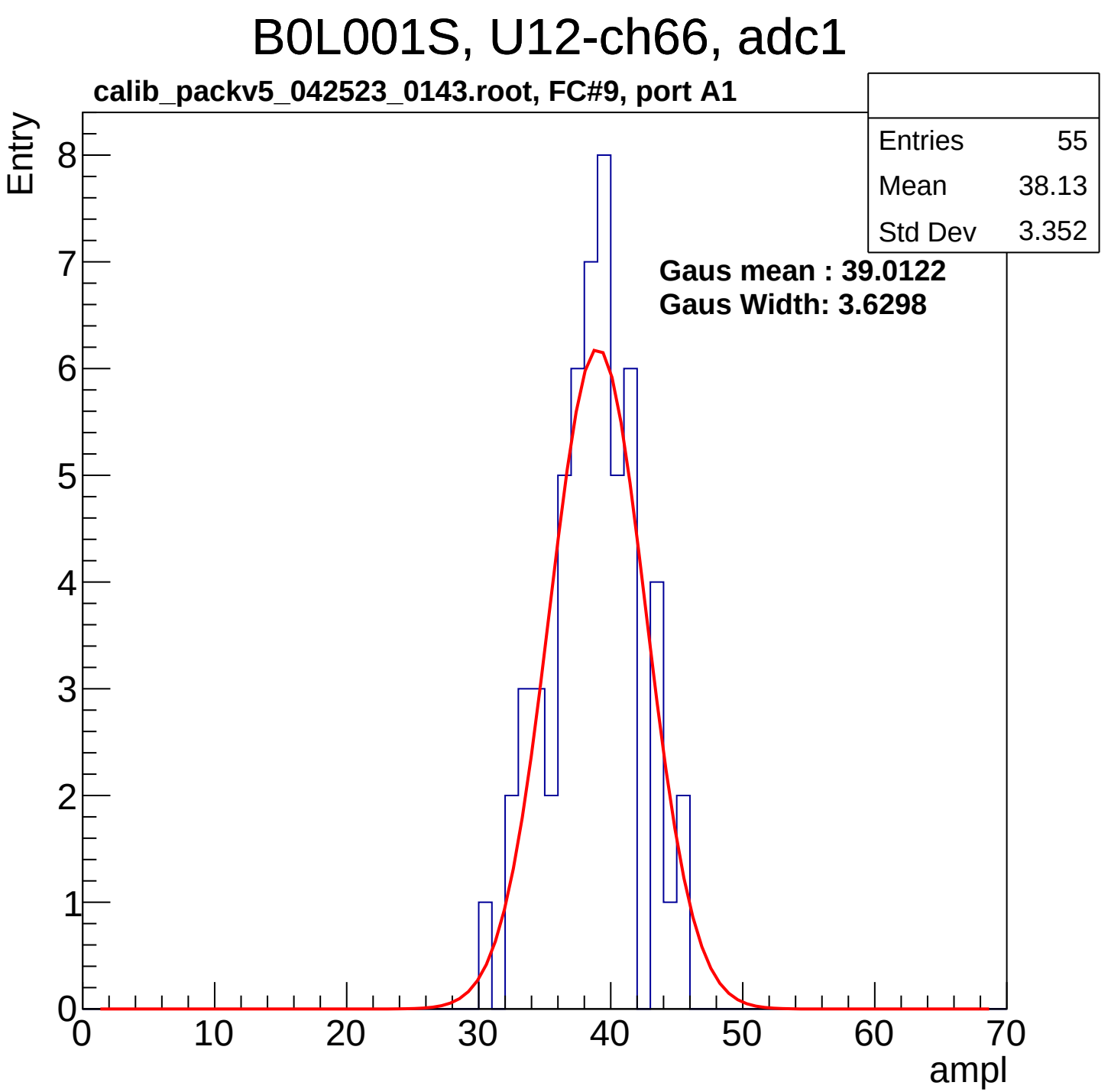
50
60
70
ampl


B0L001S, U12-ch66, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 83
Mean 32.01
Std Dev 3.829
Gaus mean : 32.6659
Gaus Width: 3.3482
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch66, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 55
Mean 38.13
Std Dev 3.352
Gaus mean : 39.0122
Gaus Width: 3.6298
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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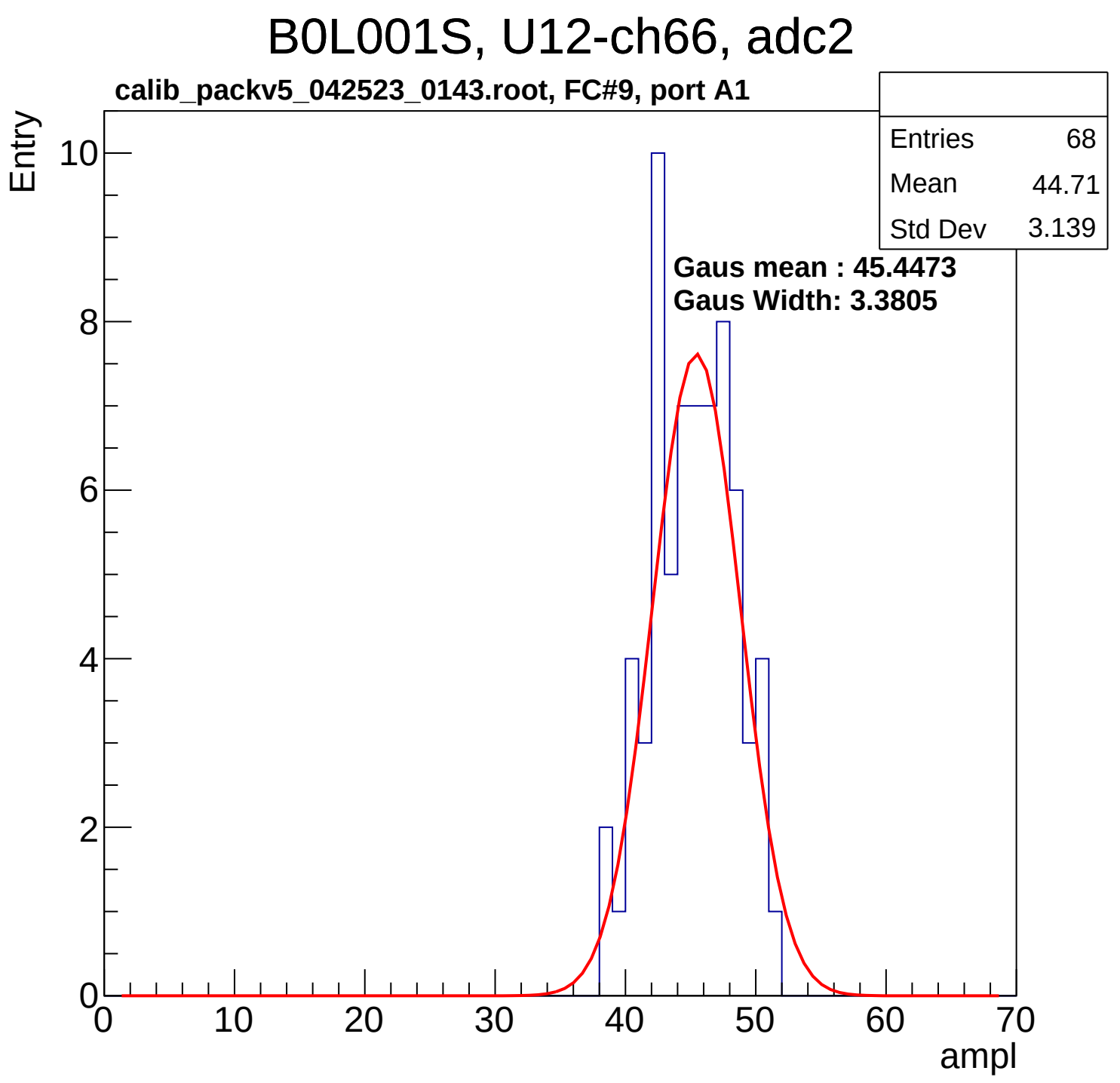
B0L001S, U12-ch66, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 68
Mean 44.71
Std Dev 3.139
Gaus mean : 45.4473
Gaus Width: 3.3805
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
50
60
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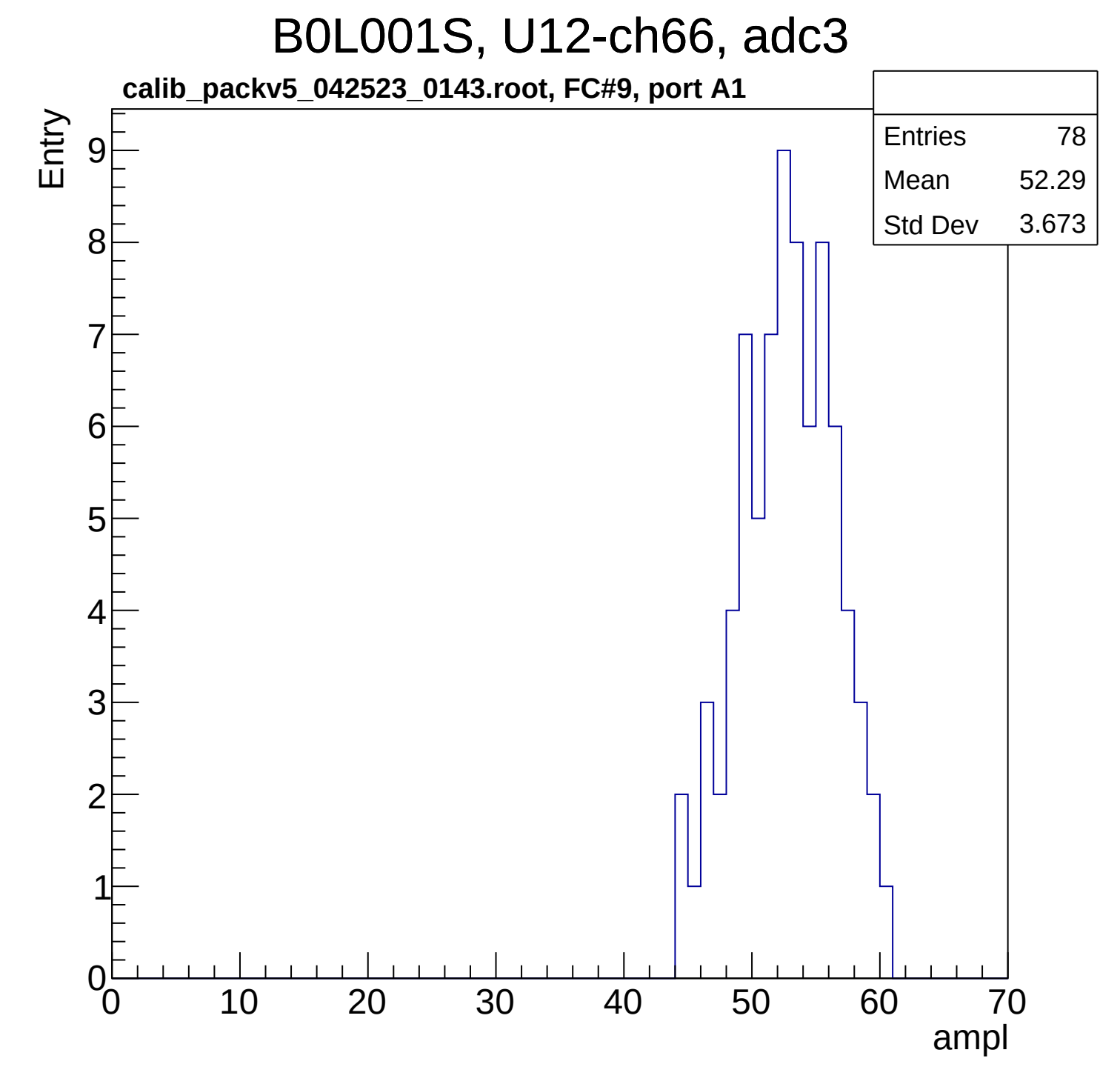
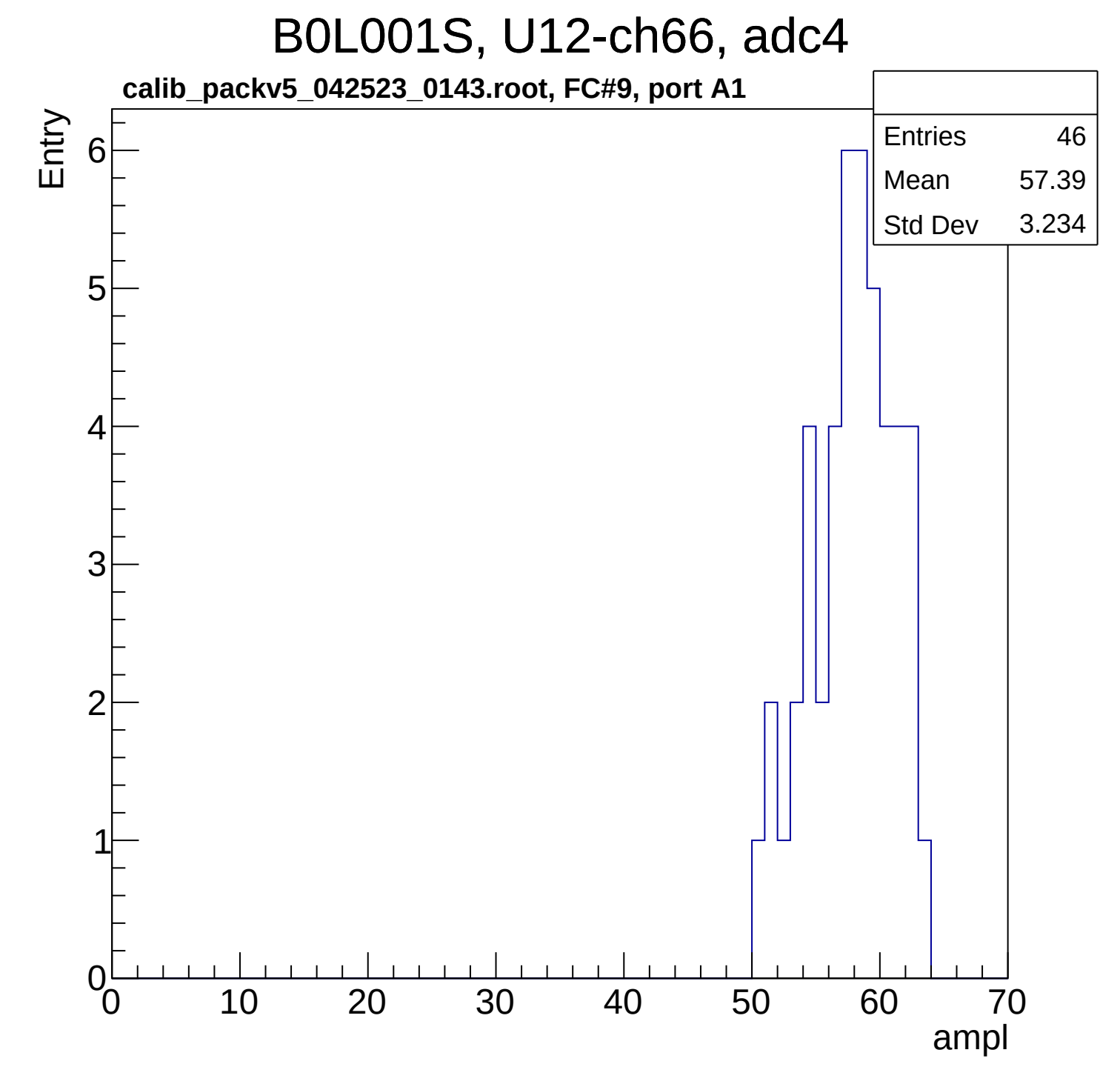
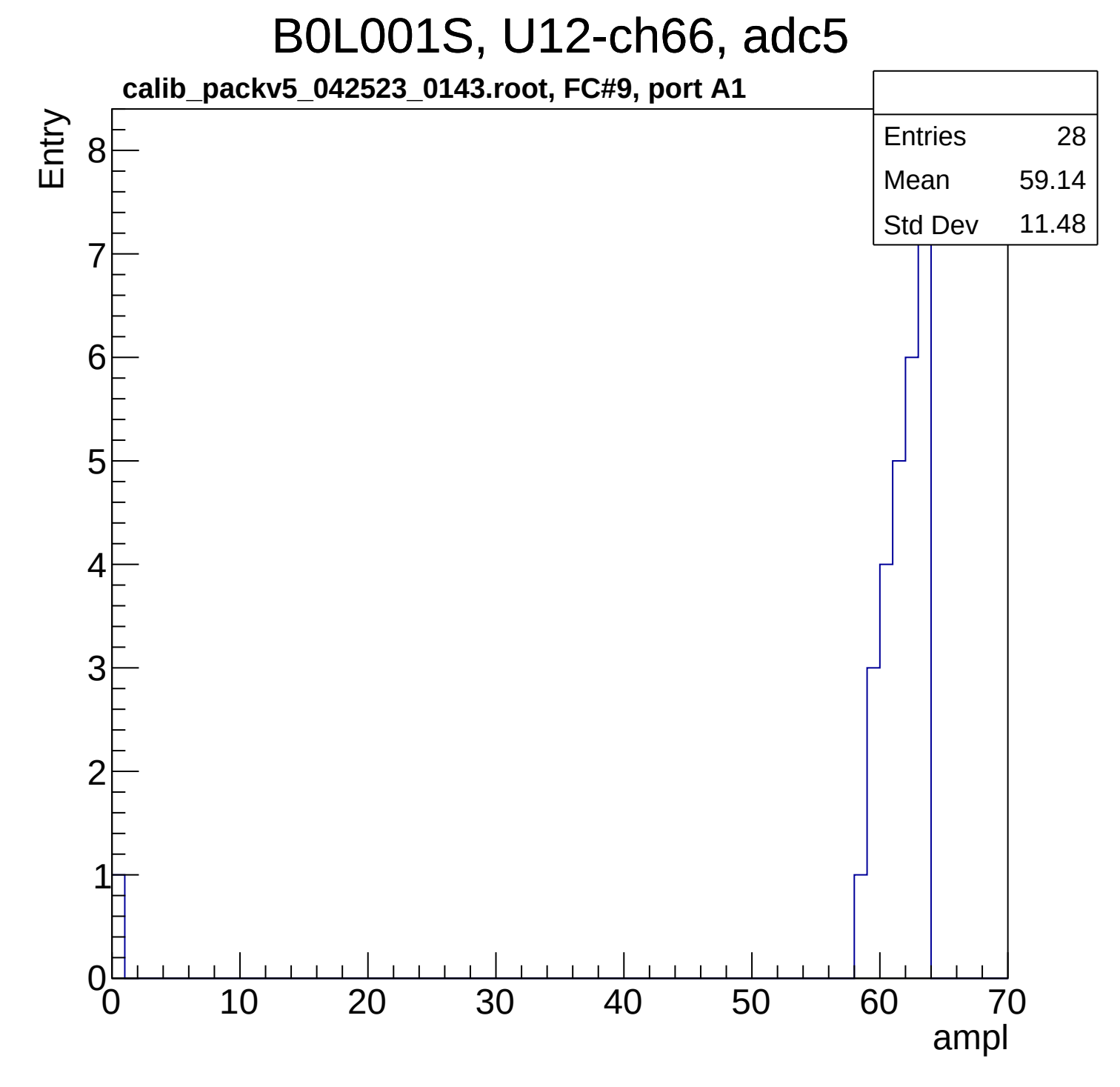

B0L001S, U12-ch66, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 78
Mean 52.29
Std Dev 3.673
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch66, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 46
Mean 57.39
Std Dev 3.234
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B0L001S, U12-ch66, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 28
Mean 59.14
Std Dev 11.48
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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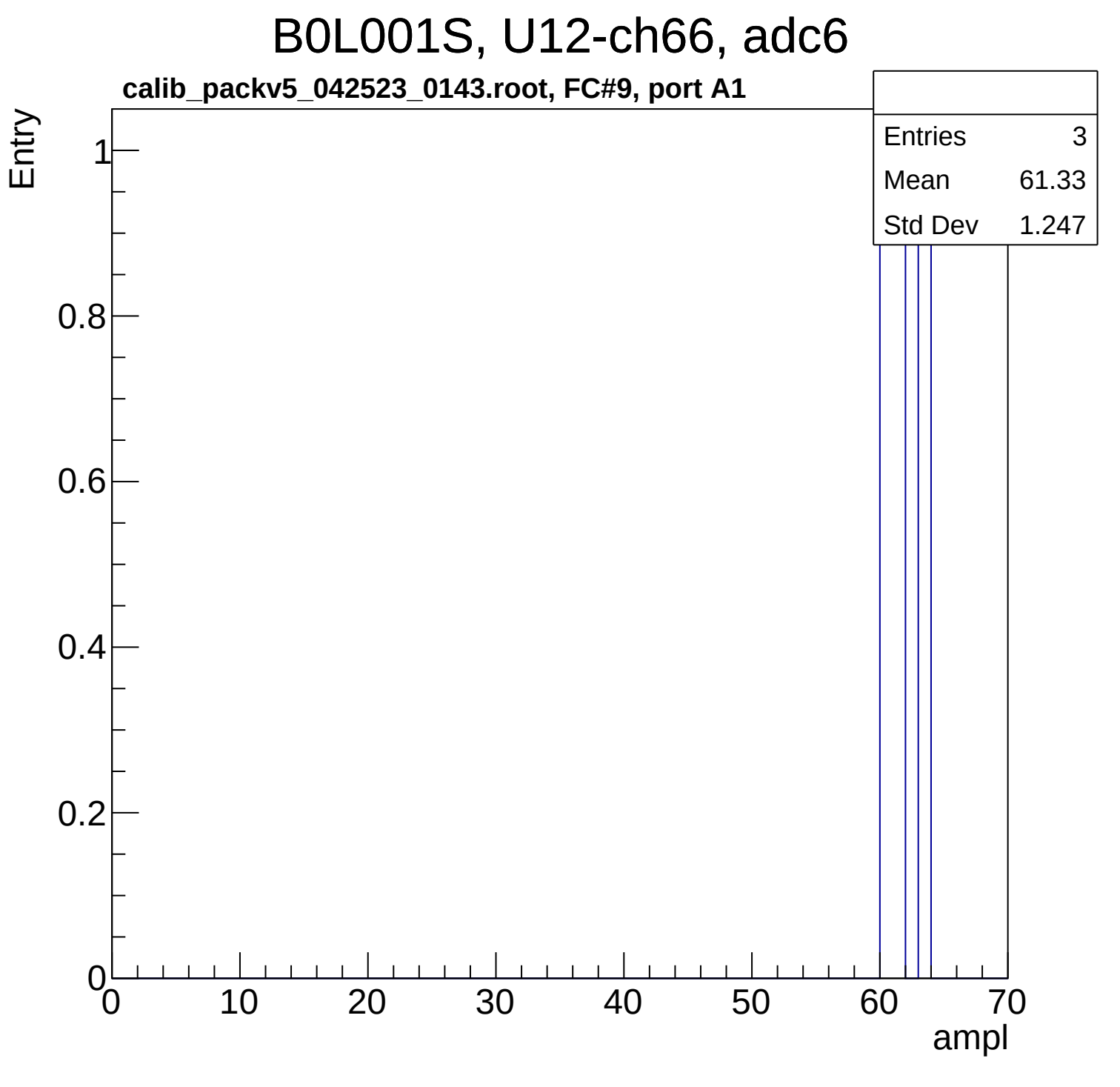
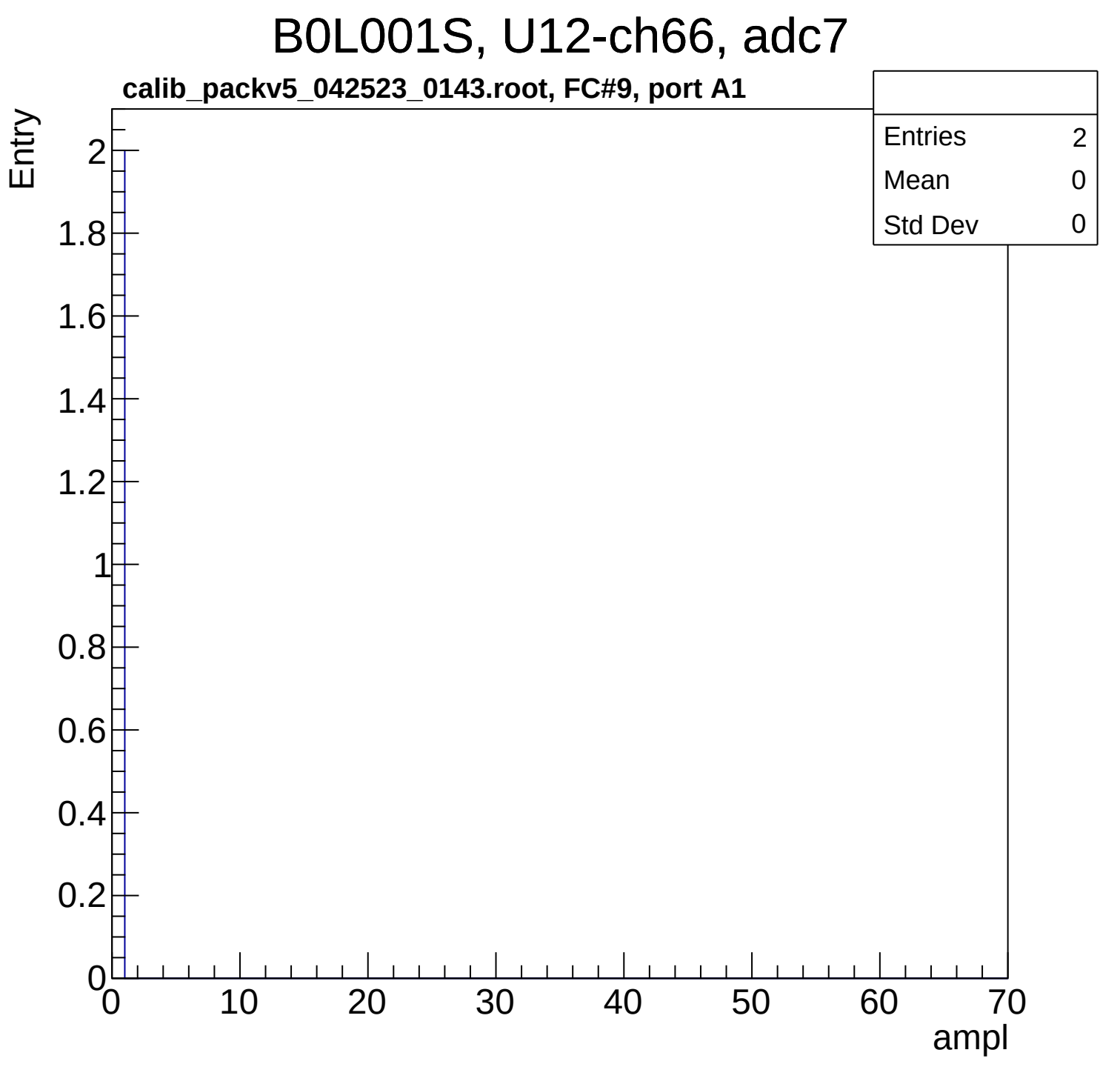
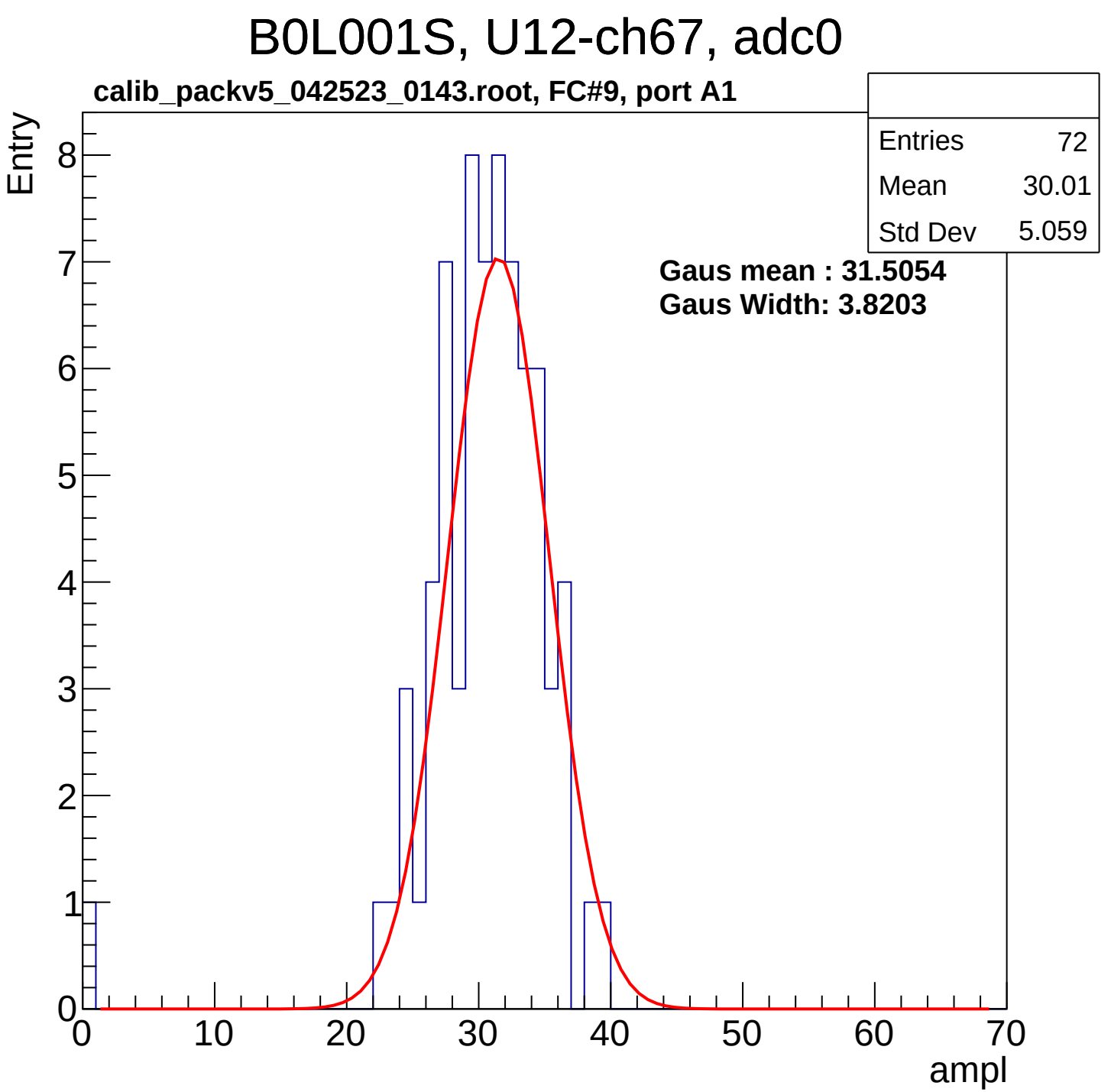
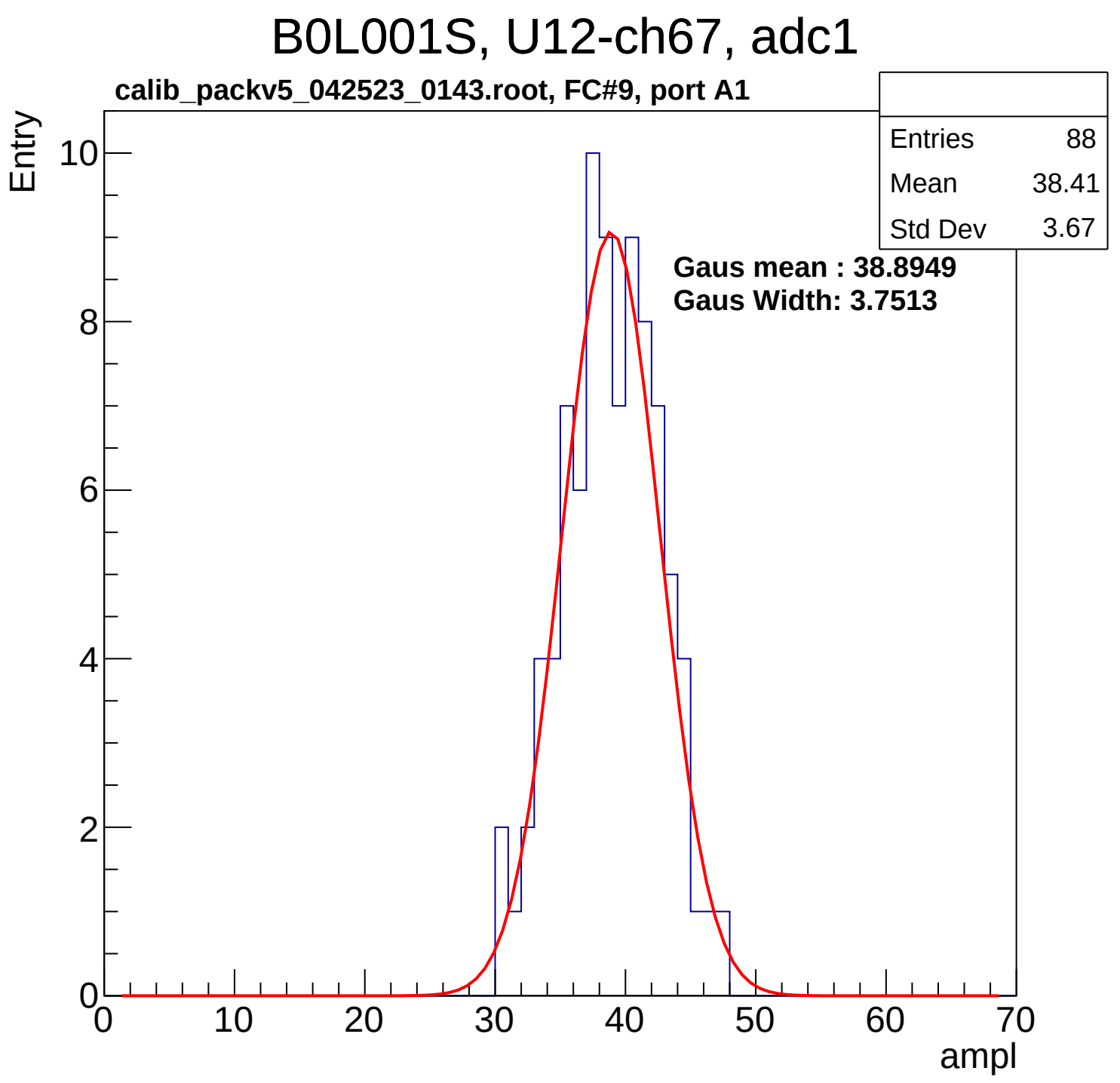
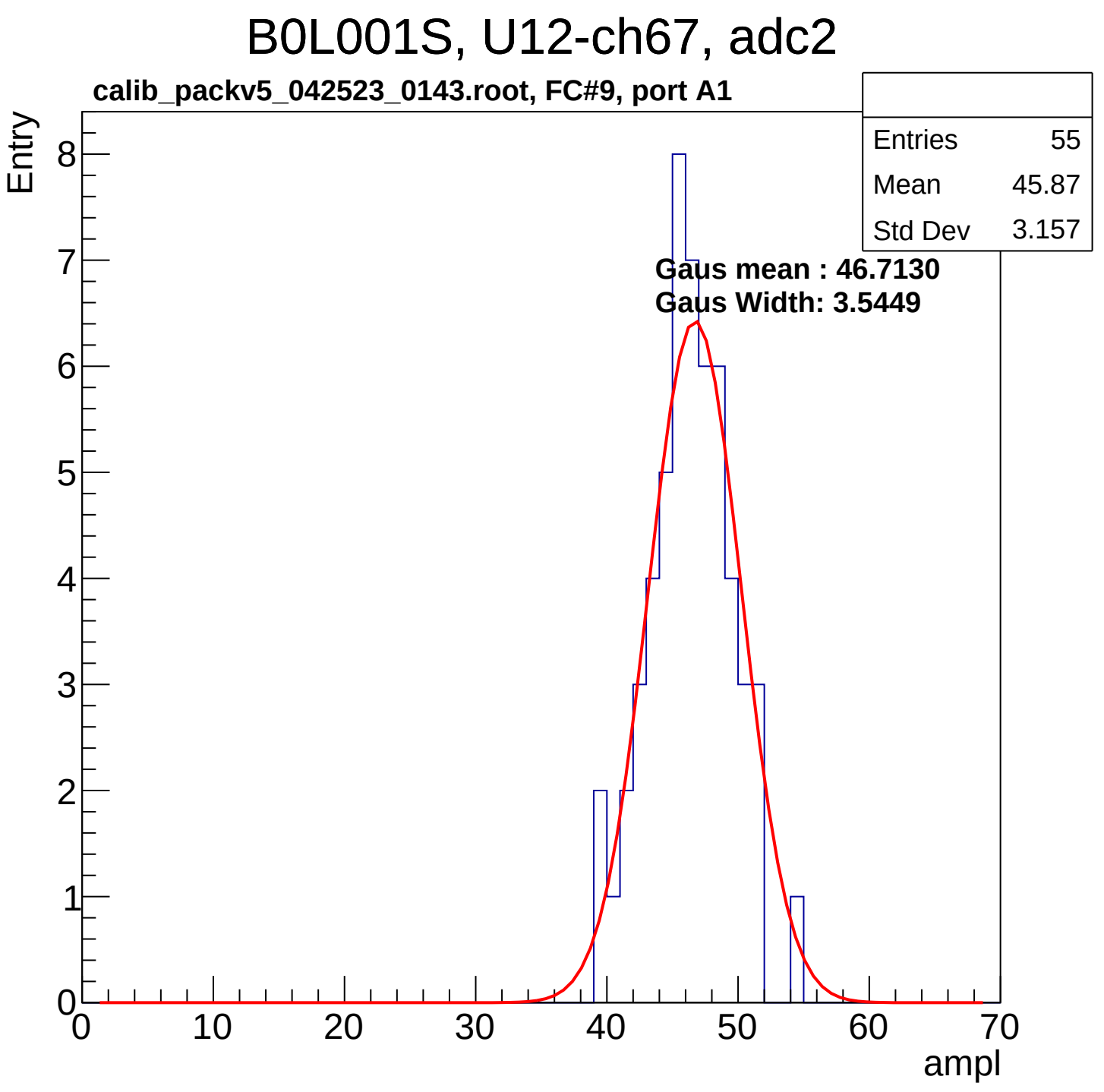
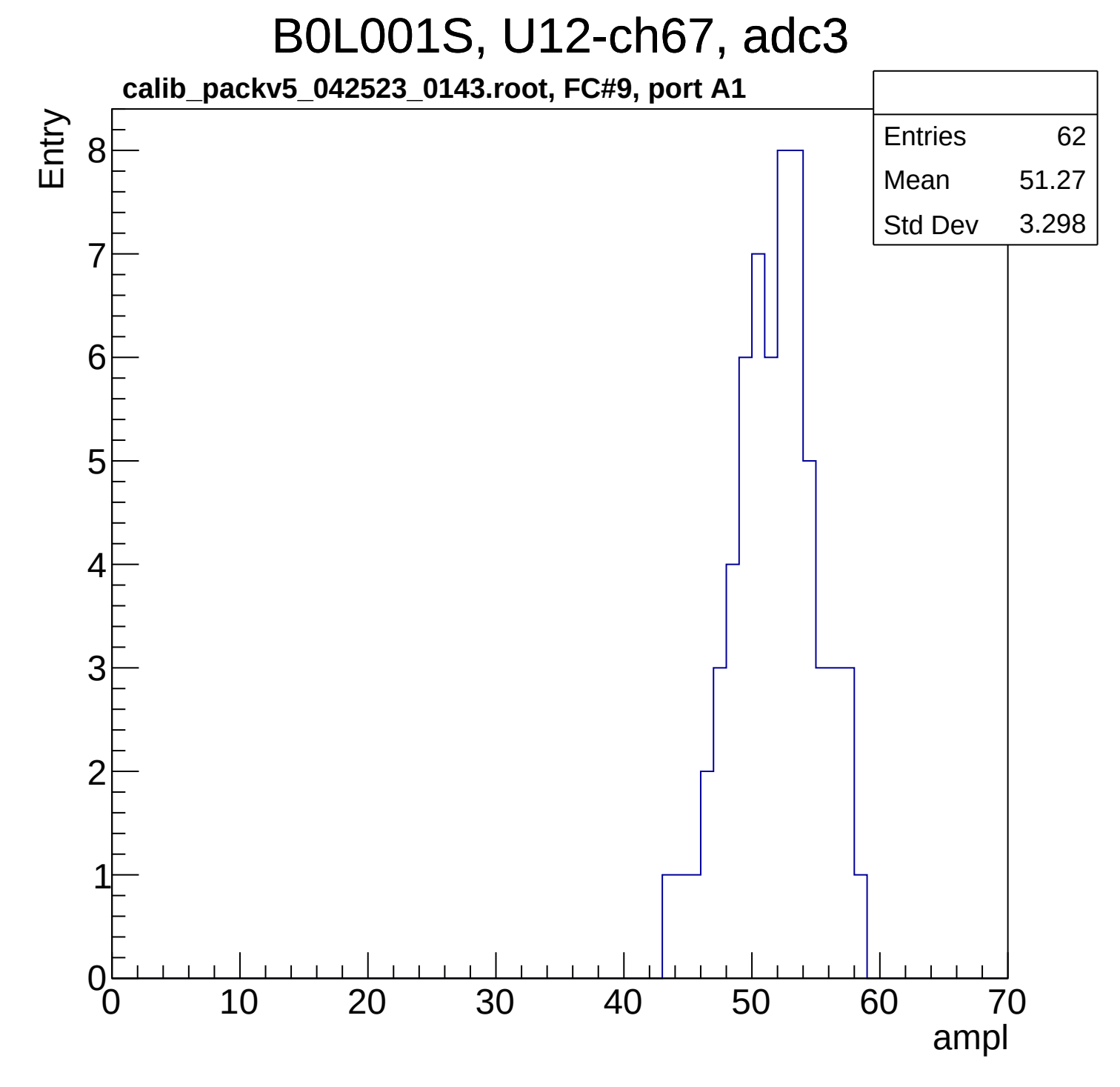

B0L001S, U12-ch66, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 3
Mean 61.33
Std Dev 1.247
Entry
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70
ampl

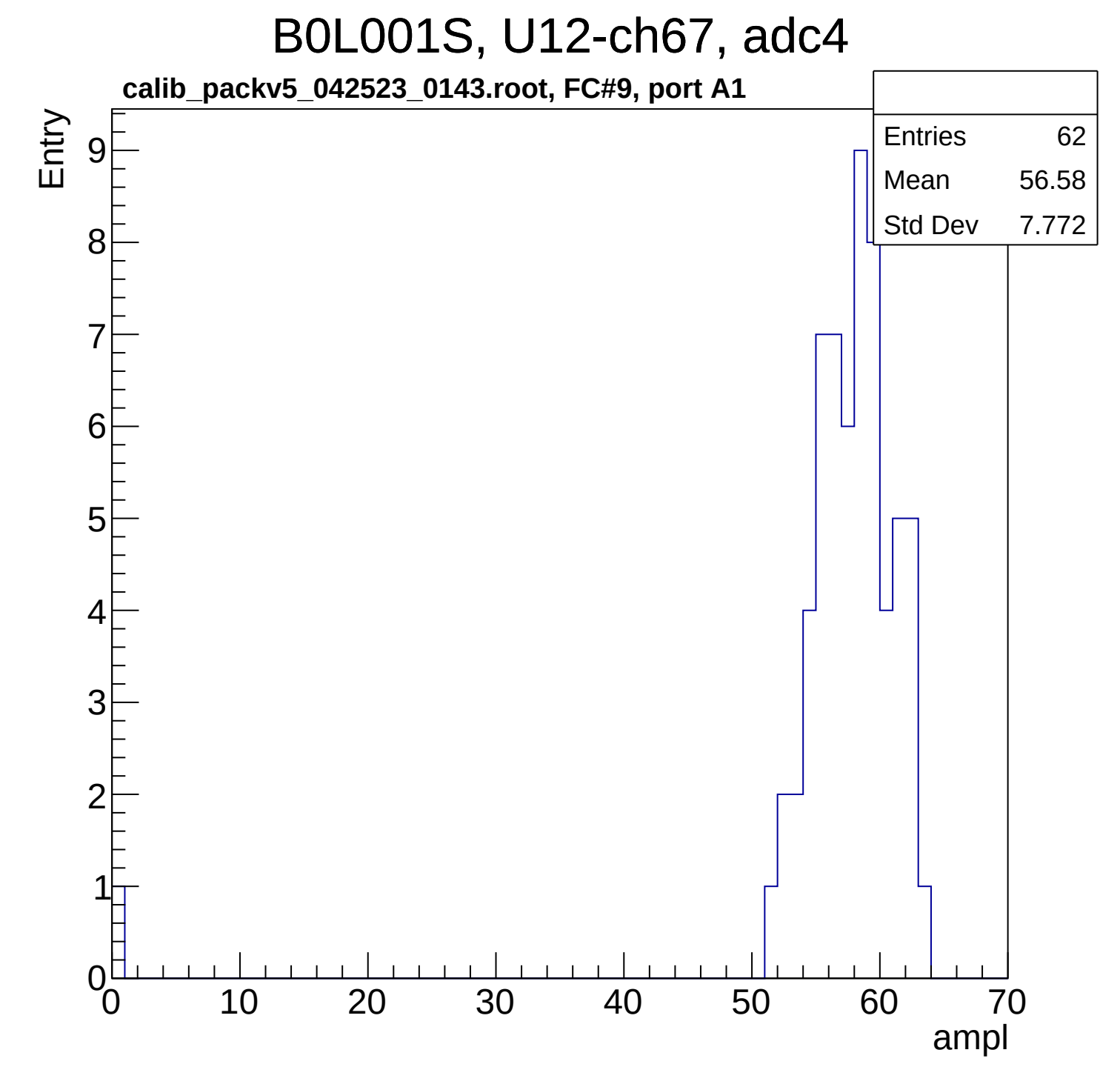

B0L001S, U12-ch66, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

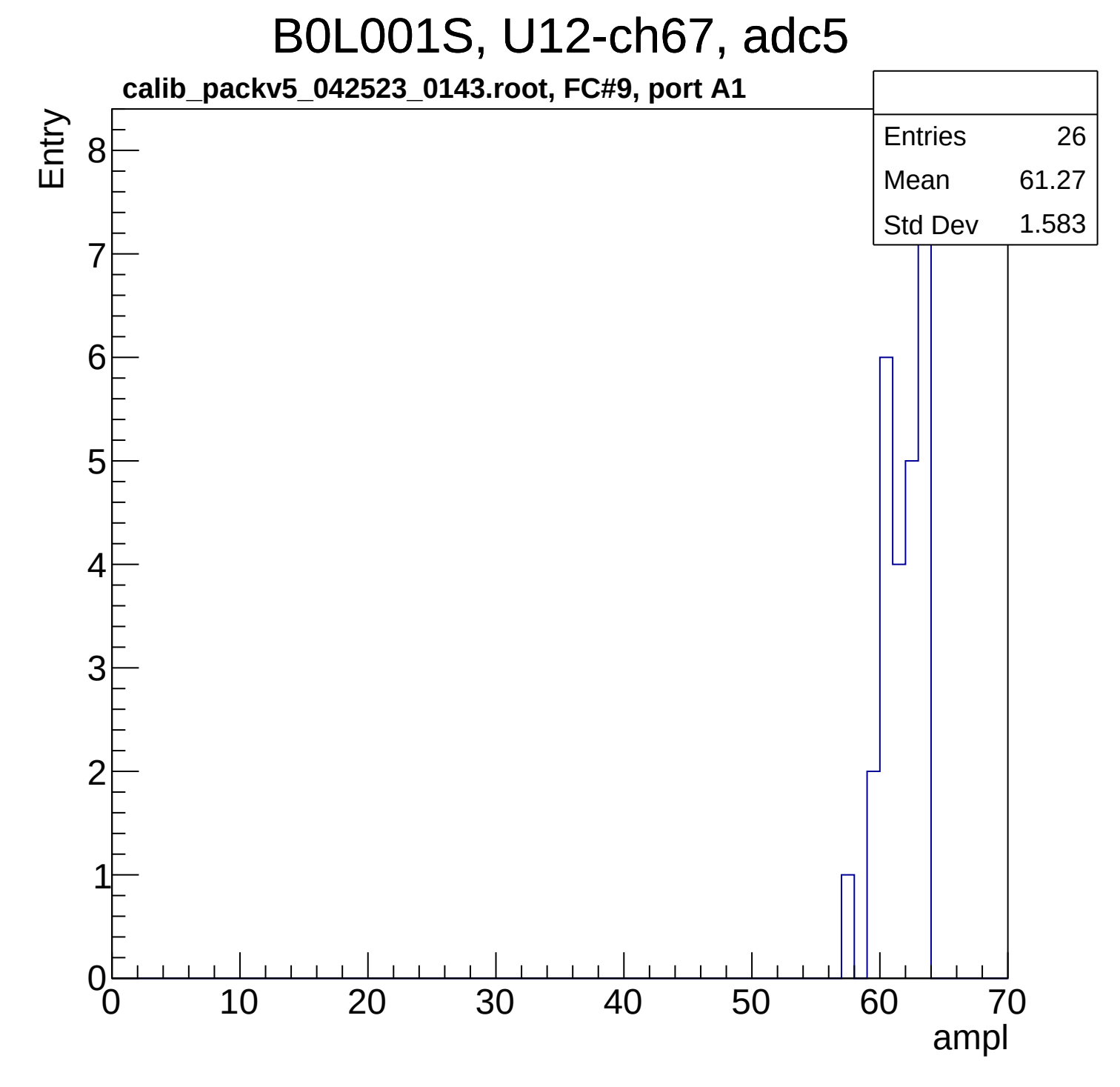

B0L001S, U12-ch67, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 72
Mean 30.01
Std Dev 5.059
Gaus mean : 31.5054
Gaus Width: 3.8203
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch67, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 88
Mean 38.41
Std Dev 3.67
Gaus mean : 38.8949
Gaus Width: 3.7513
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch67, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 55
Mean 45.87
Std Dev 3.157
Gaus mean : 46.7130
Gaus Width: 3.5449
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch67, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 62
Mean 51.27
Std Dev 3.298
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch67, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 62
Mean 56.58
Std Dev 7.772
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch67, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 26
Mean 61.27
Std Dev 1.583
Entry
ampl
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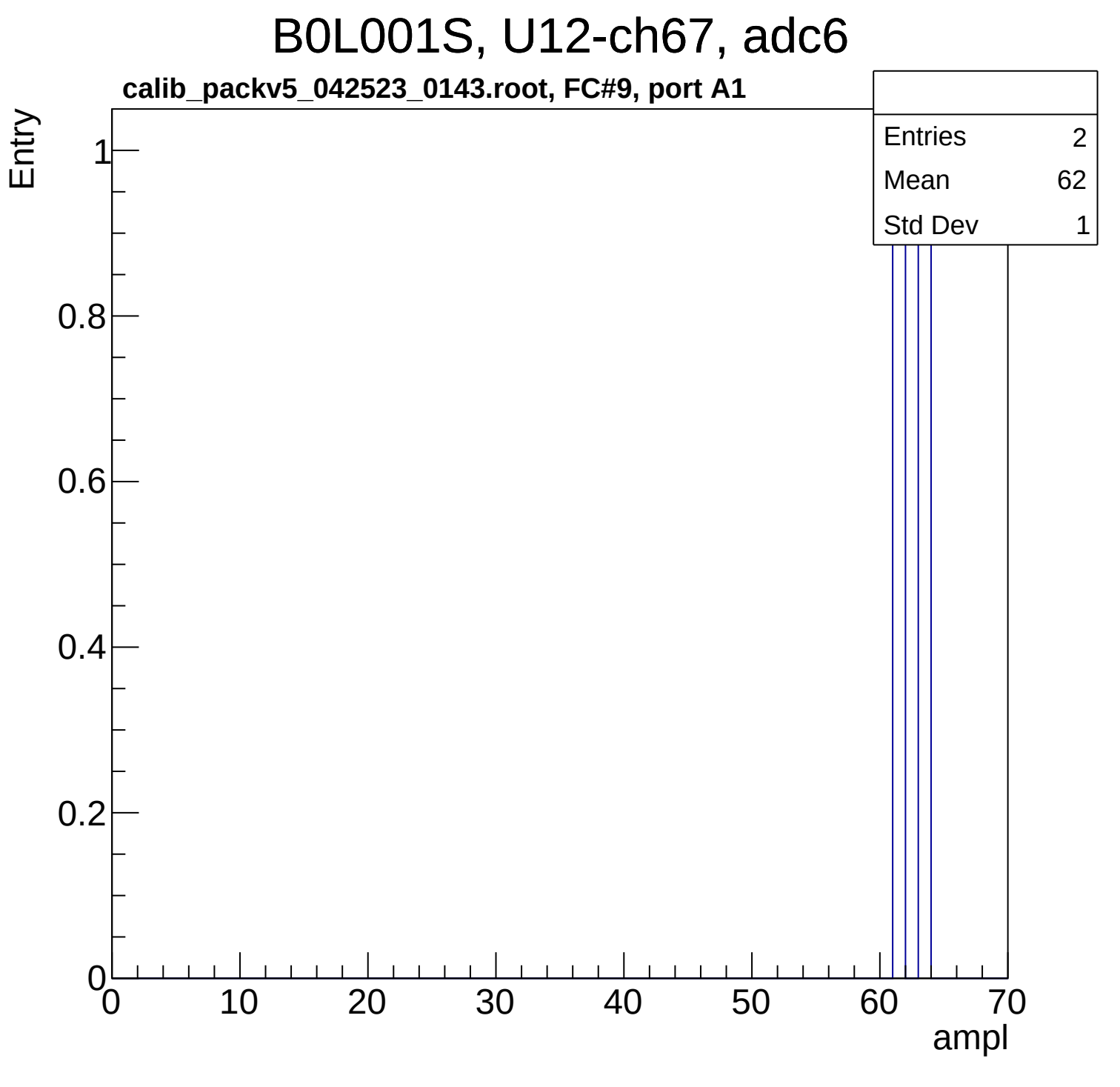
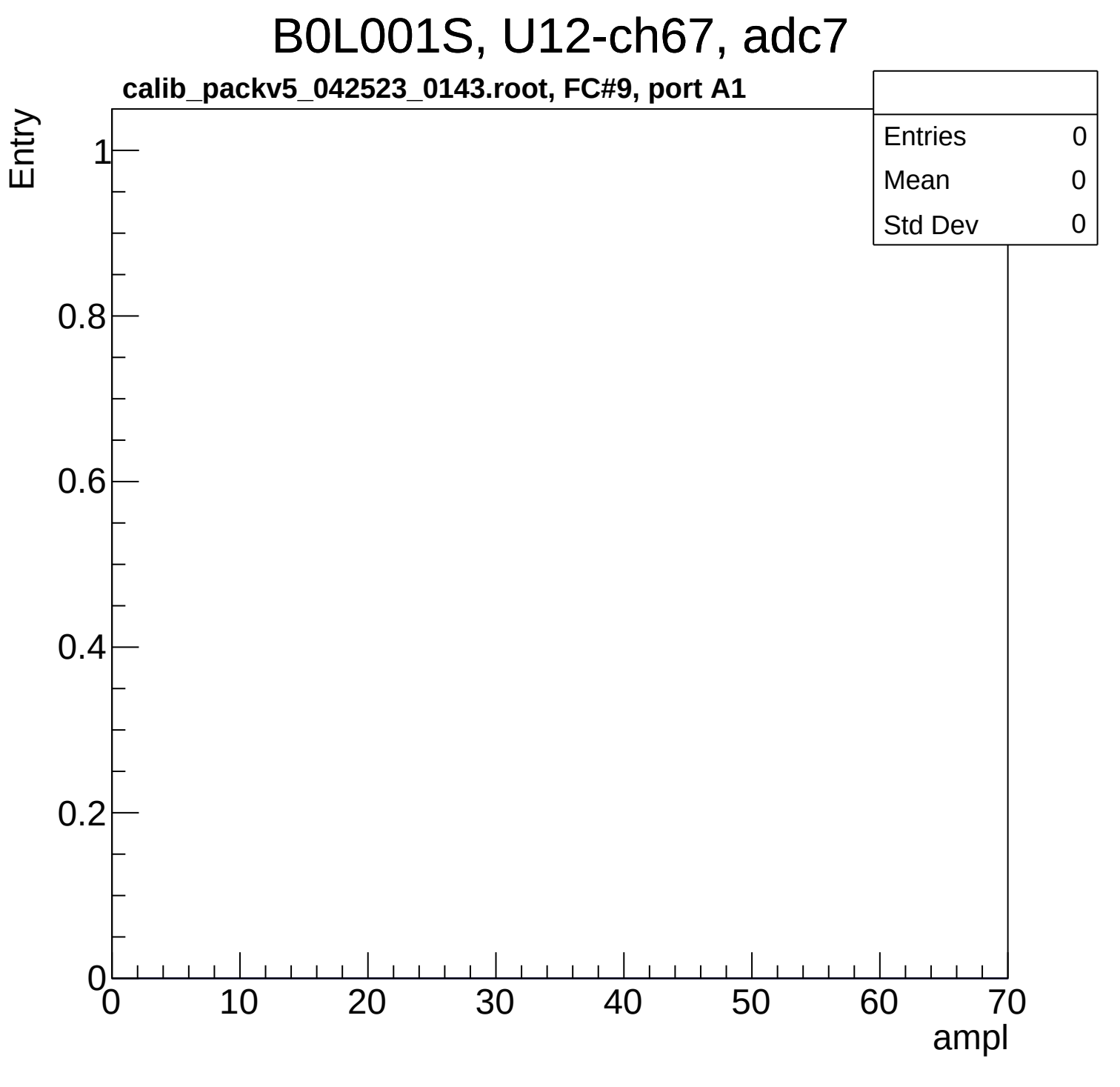
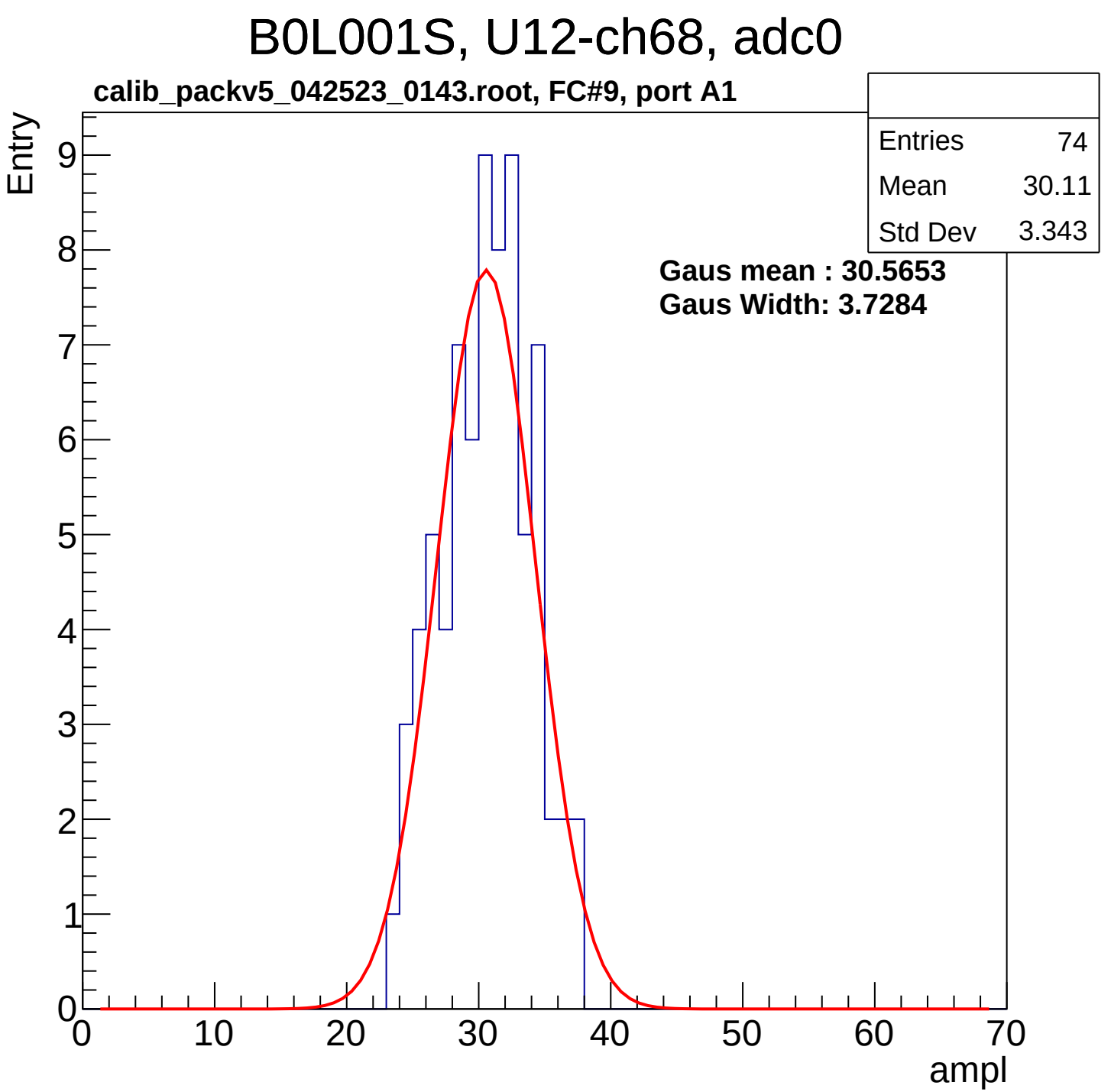
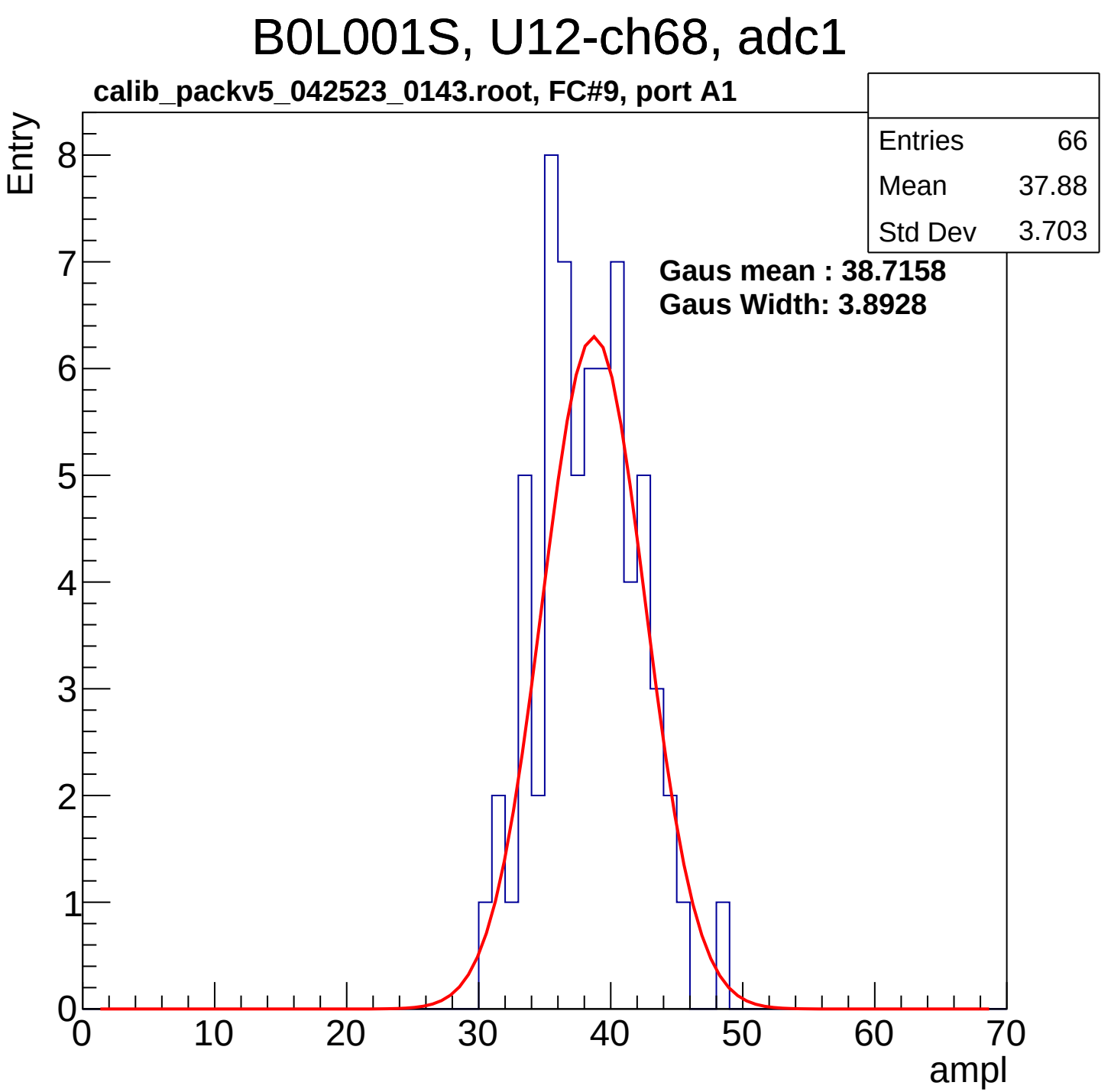
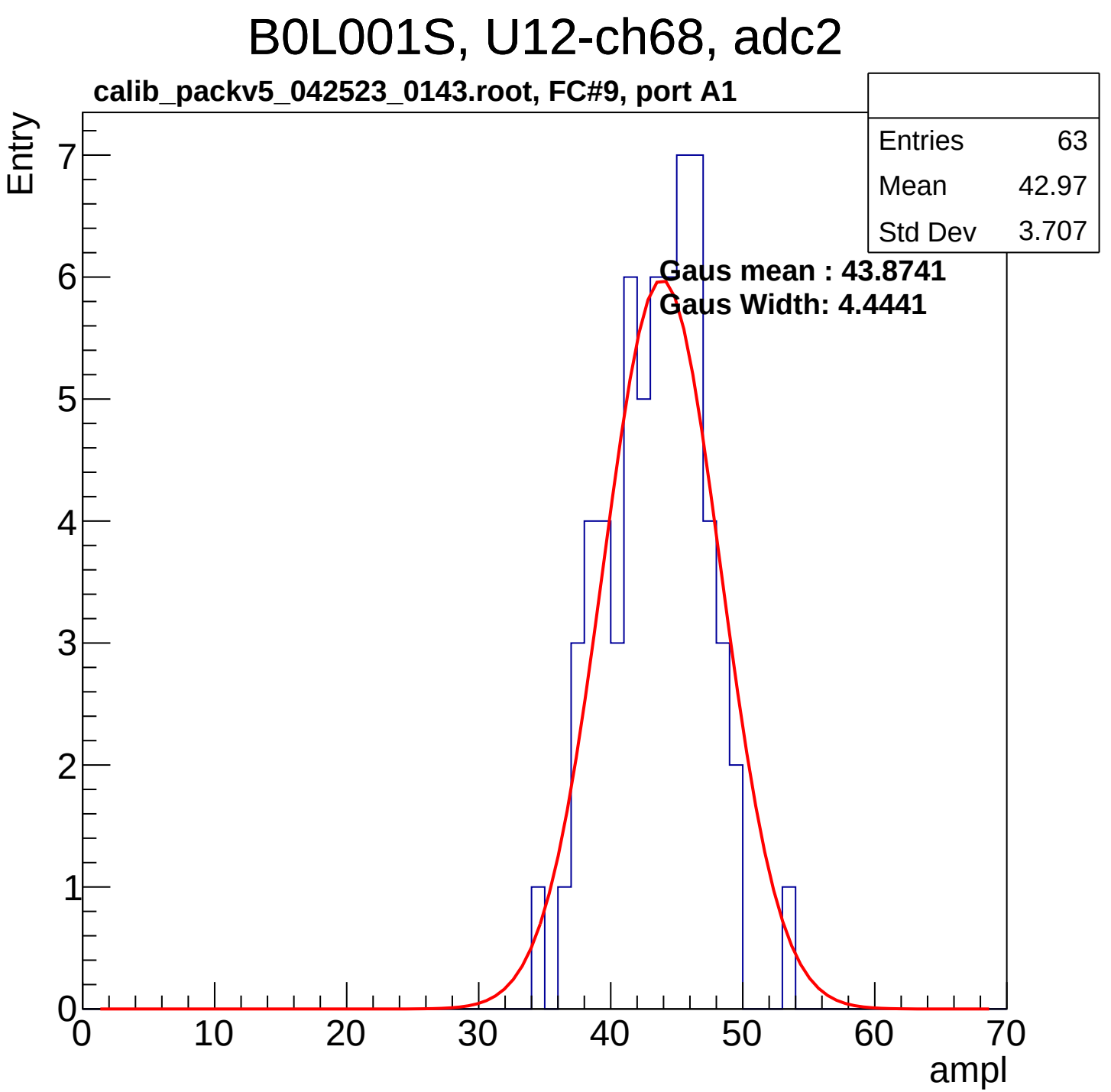
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

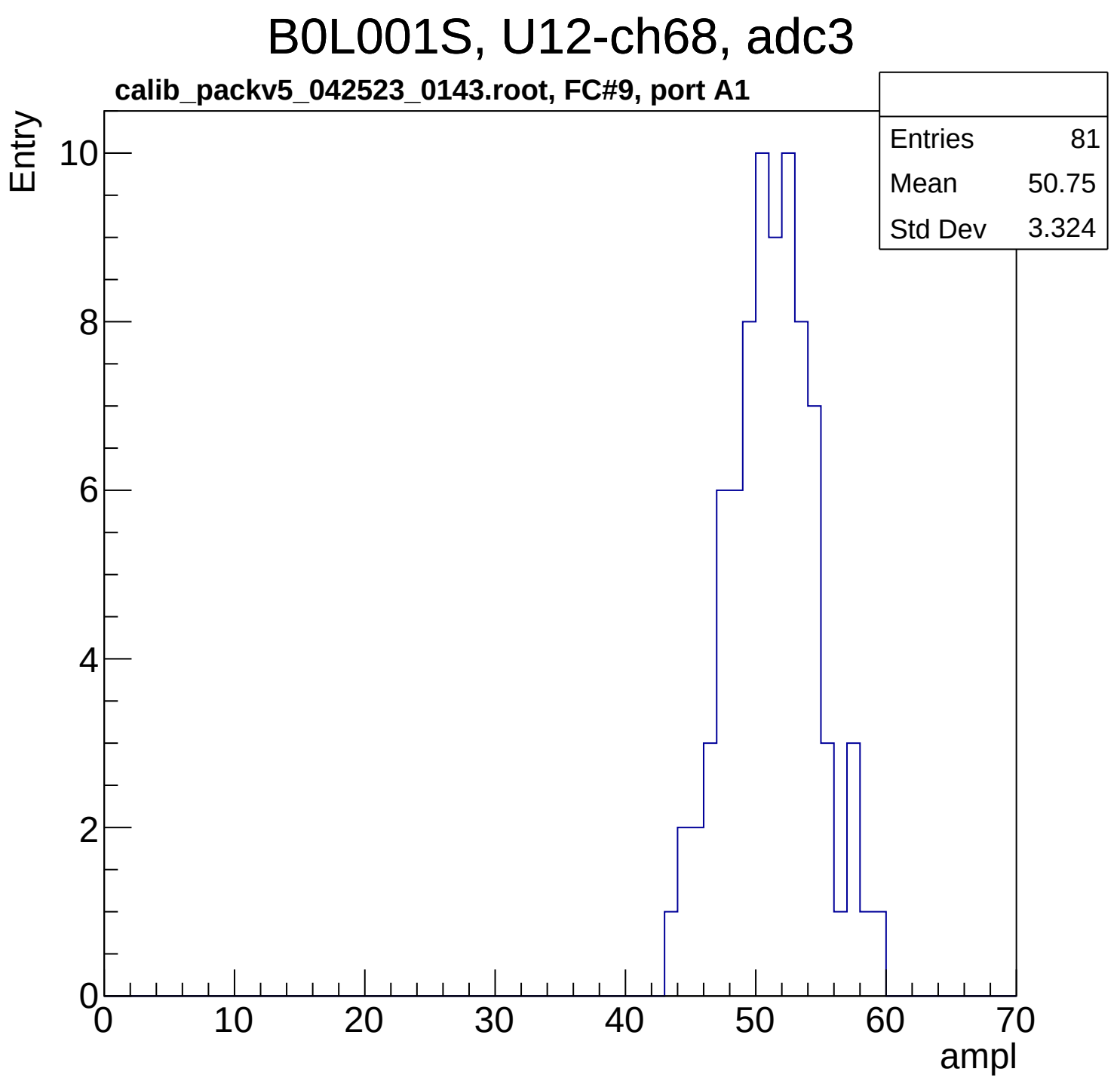

B0L001S, U12-ch67, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 62
Std Dev 1
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

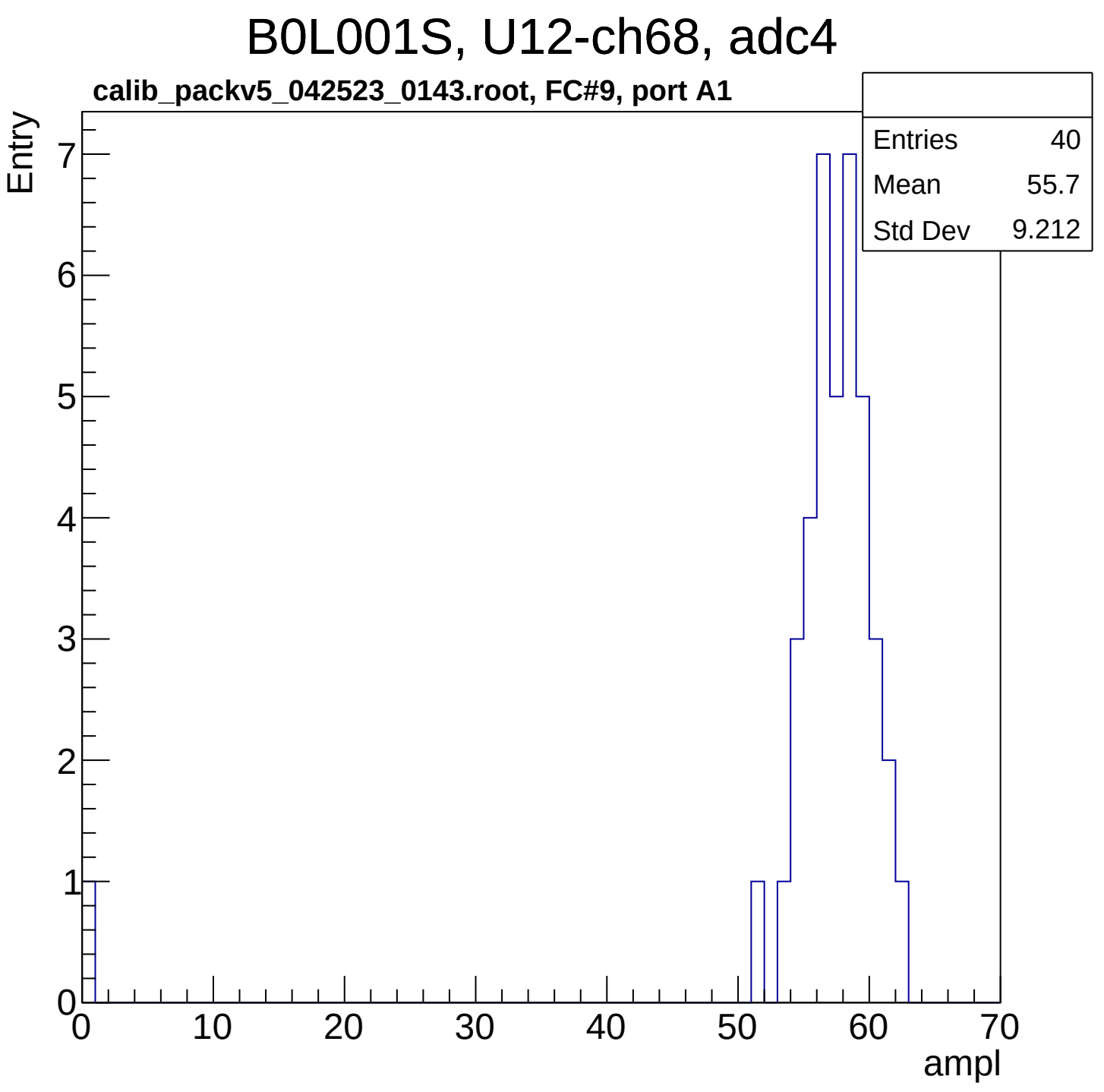

B0L001S, U12-ch67, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch68, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 74
Mean 30.11
Std Dev 3.343
Gaus mean : 30.5653
Gaus Width: 3.7284
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch68, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 66
Mean 37.88
Std Dev 3.703
Gaus mean : 38.7158
Gaus Width: 3.8928
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch68, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 63
Mean 42.97
Std Dev 3.707
Gaus mean : 43.8741
Gaus Width: 4.4441
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B0L001S, U12-ch68, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 81
Mean 50.75
Std Dev 3.324
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch68, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 40
Mean 55.7
Std Dev 9.212
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
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60
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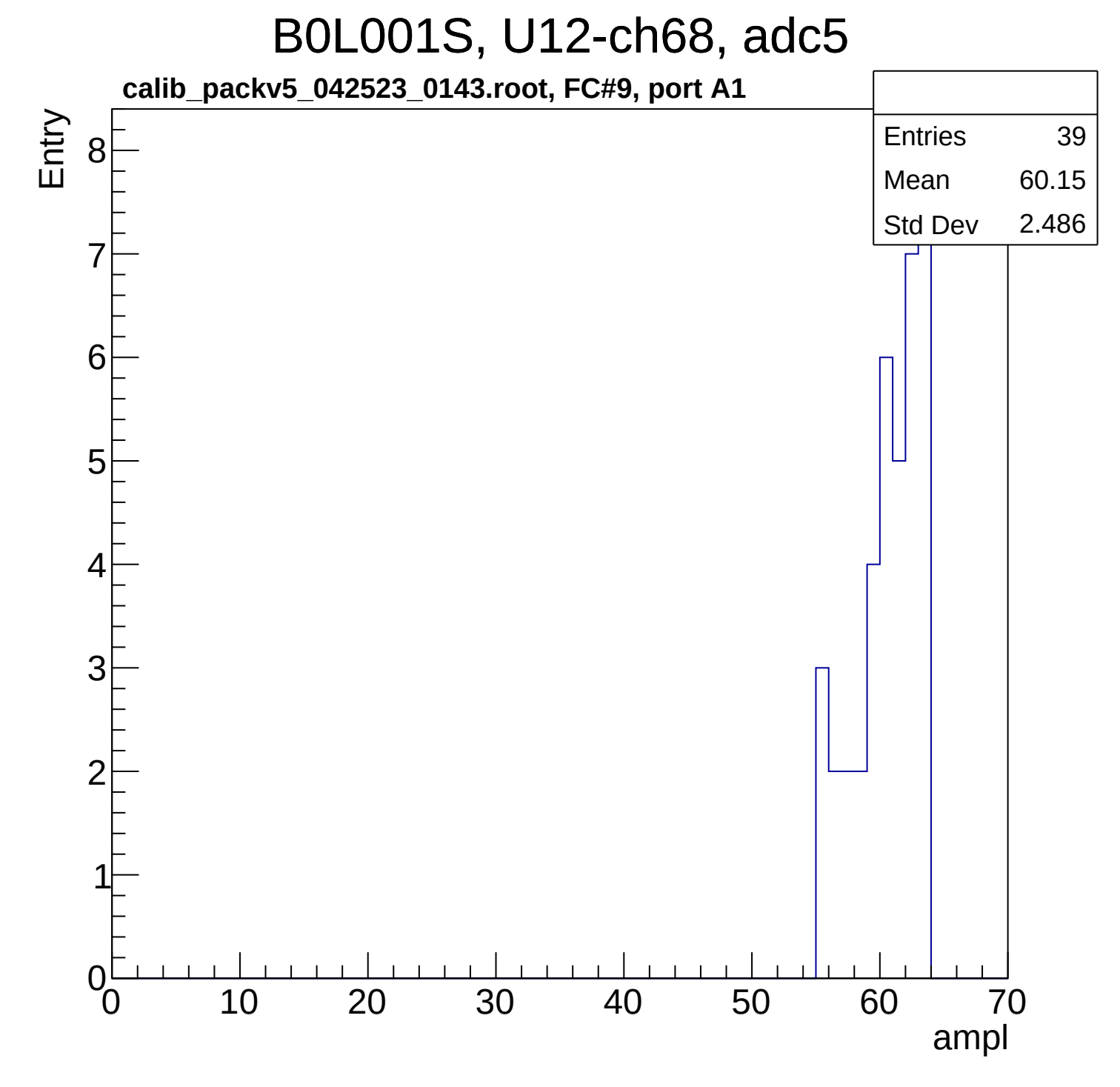
B0L001S, U12-ch68, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 39
Mean 60.15
Std Dev 2.486
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
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60
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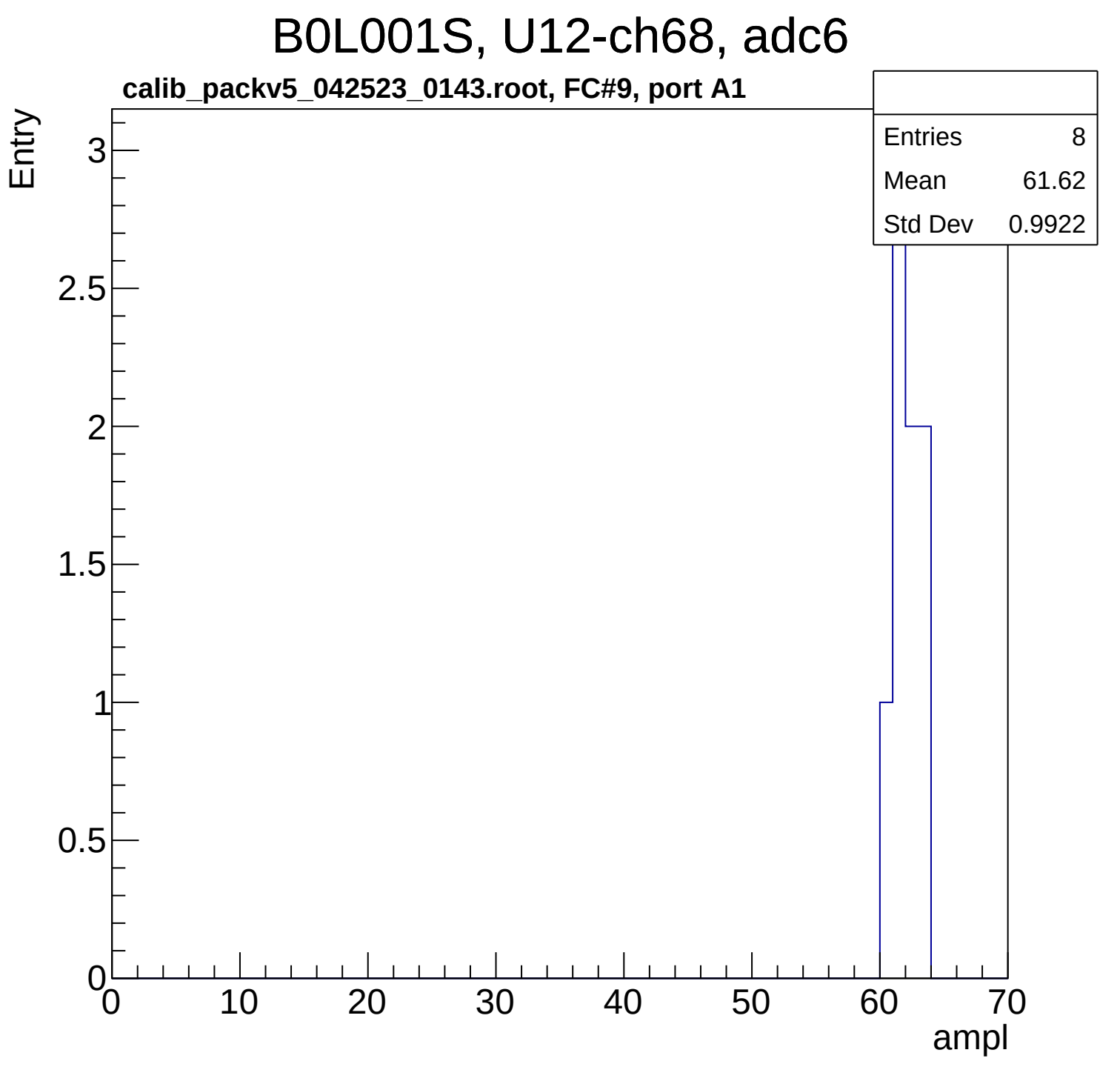
B0L001S, U12-ch68, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 8
Mean 61.62
Std Dev 0.9922
Entry
ampl
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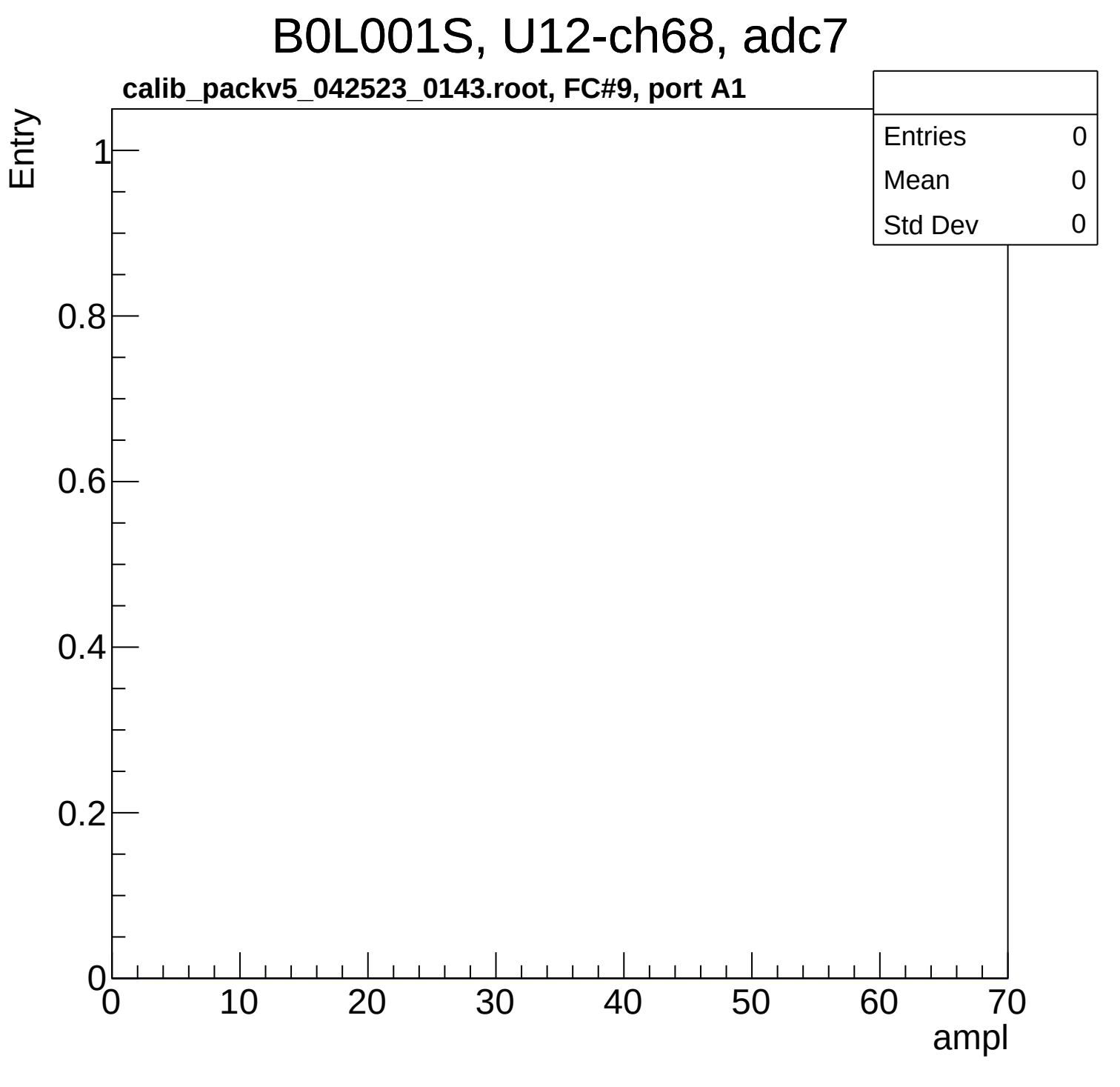
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B0L001S, U12-ch68, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
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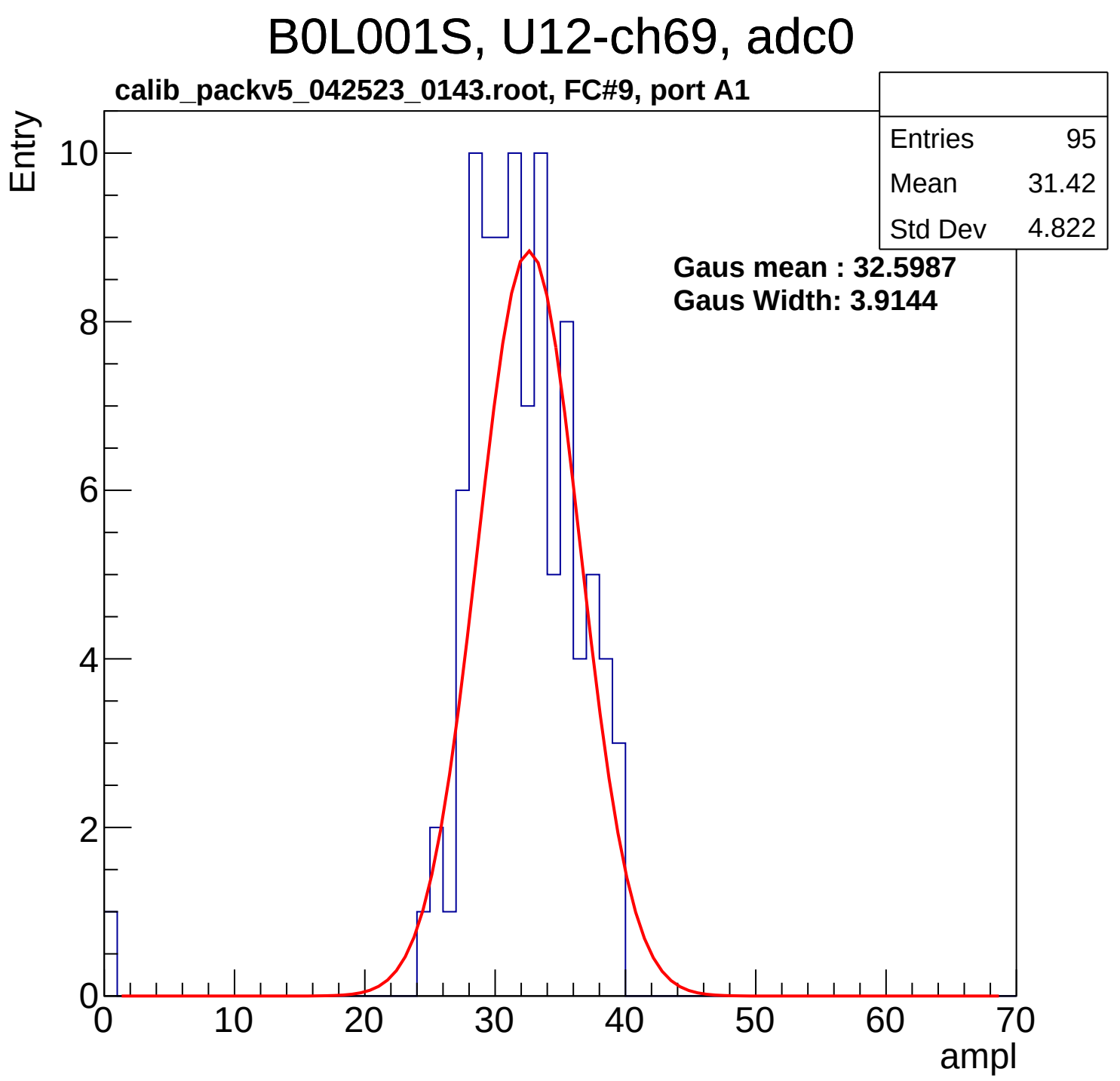
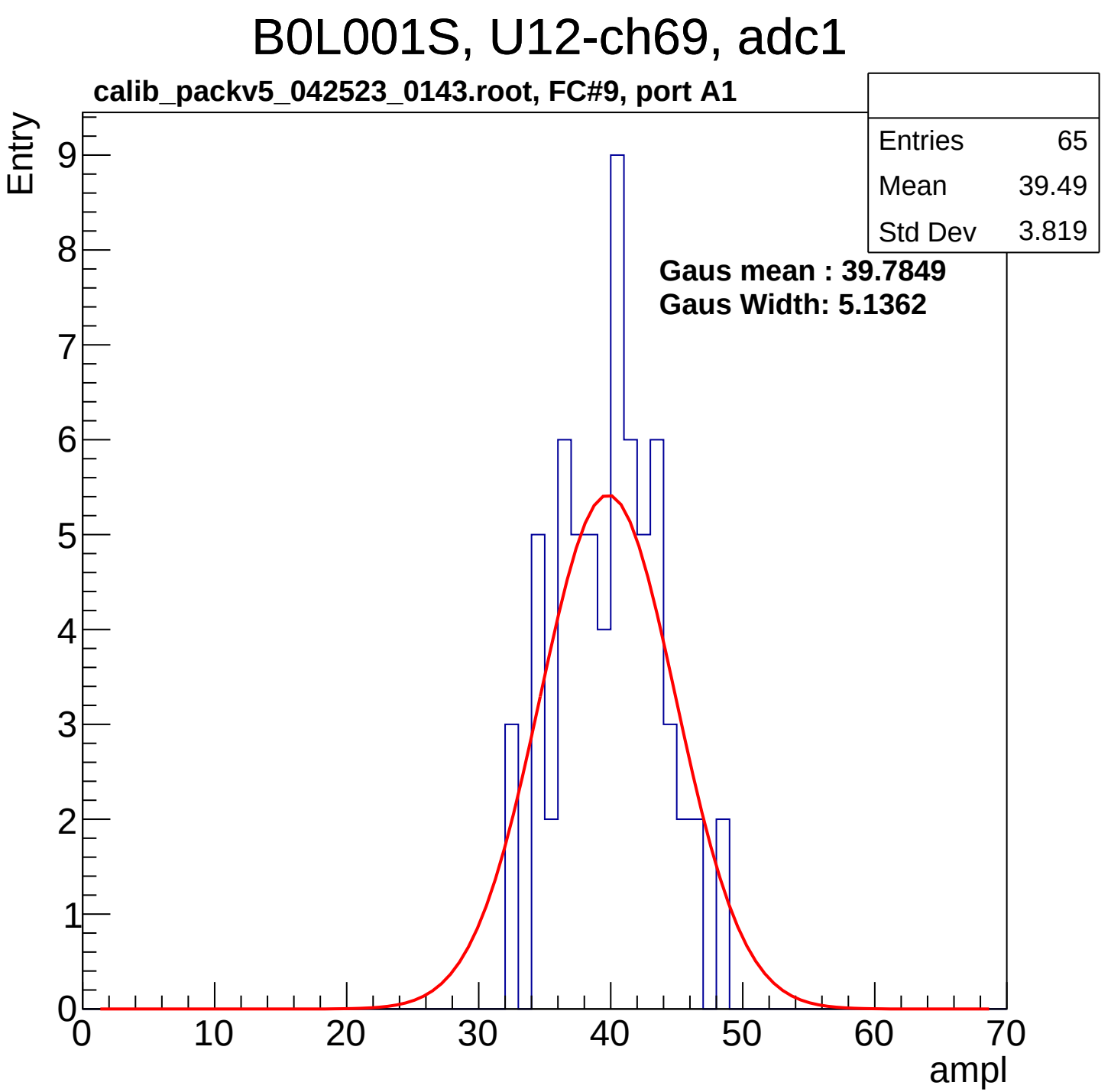
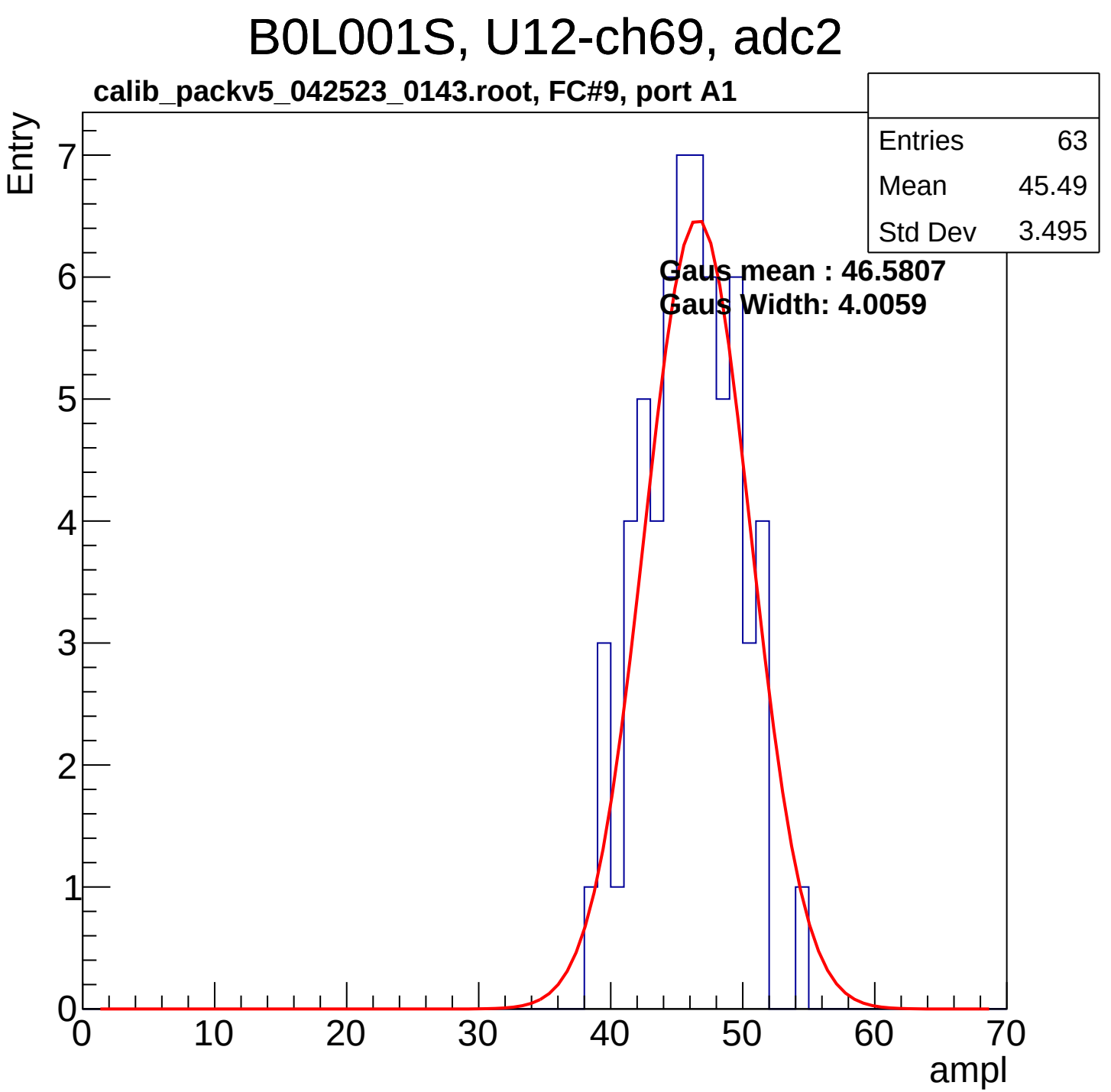
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch69, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 95
Mean 31.42
Std Dev 4.822
Gaus mean : 32.5987
Gaus Width: 3.9144
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch69, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 65
Mean 39.49
Std Dev 3.819
Gaus mean : 39.7849
Gaus Width: 5.1362
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch69, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 63
Mean 45.49
Std Dev 3.495
Gaus mean : 46.5807
Gaus Width: 4.0059
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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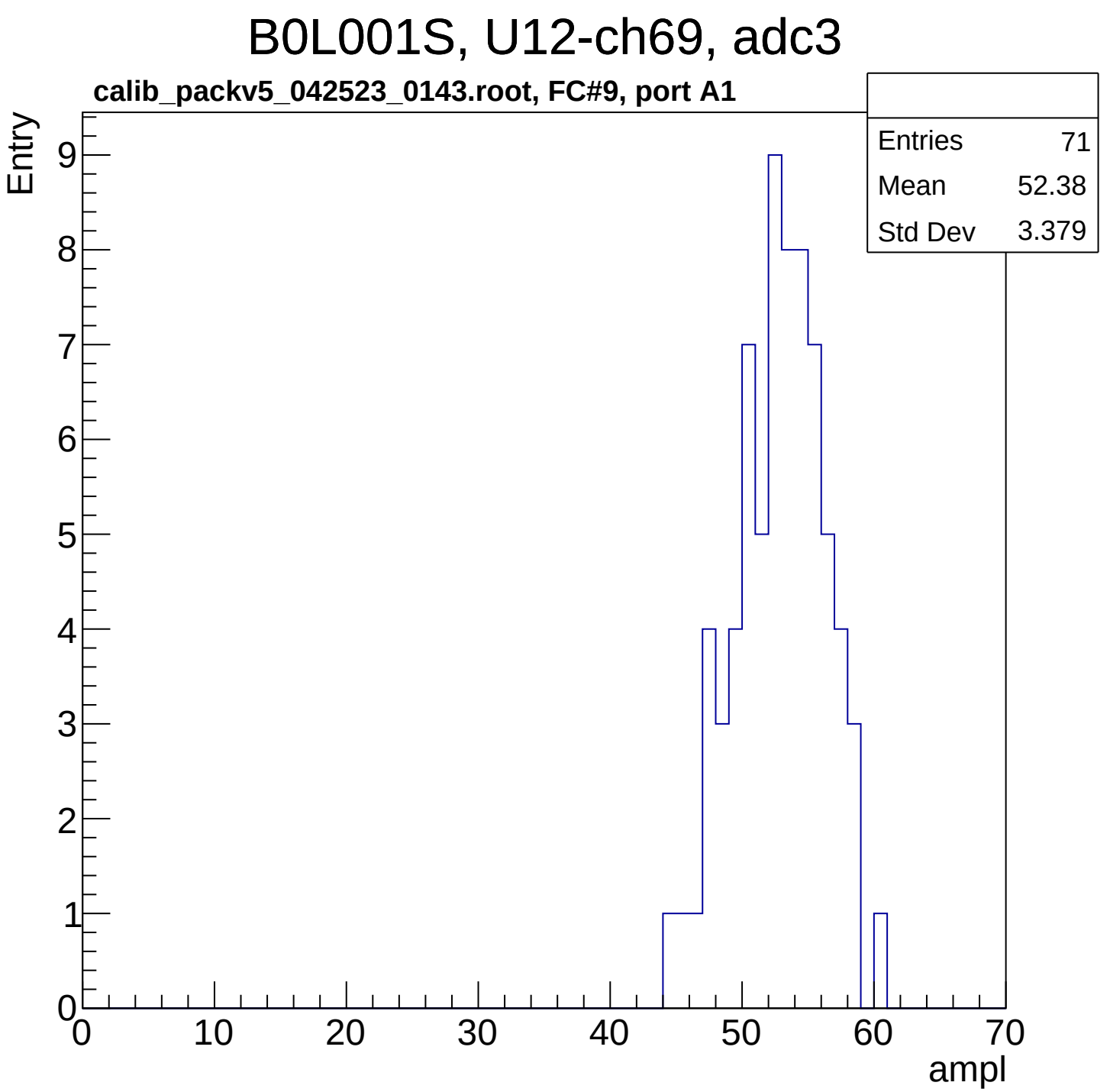
B0L001S, U12-ch69, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 71
Mean 52.38
Std Dev 3.379
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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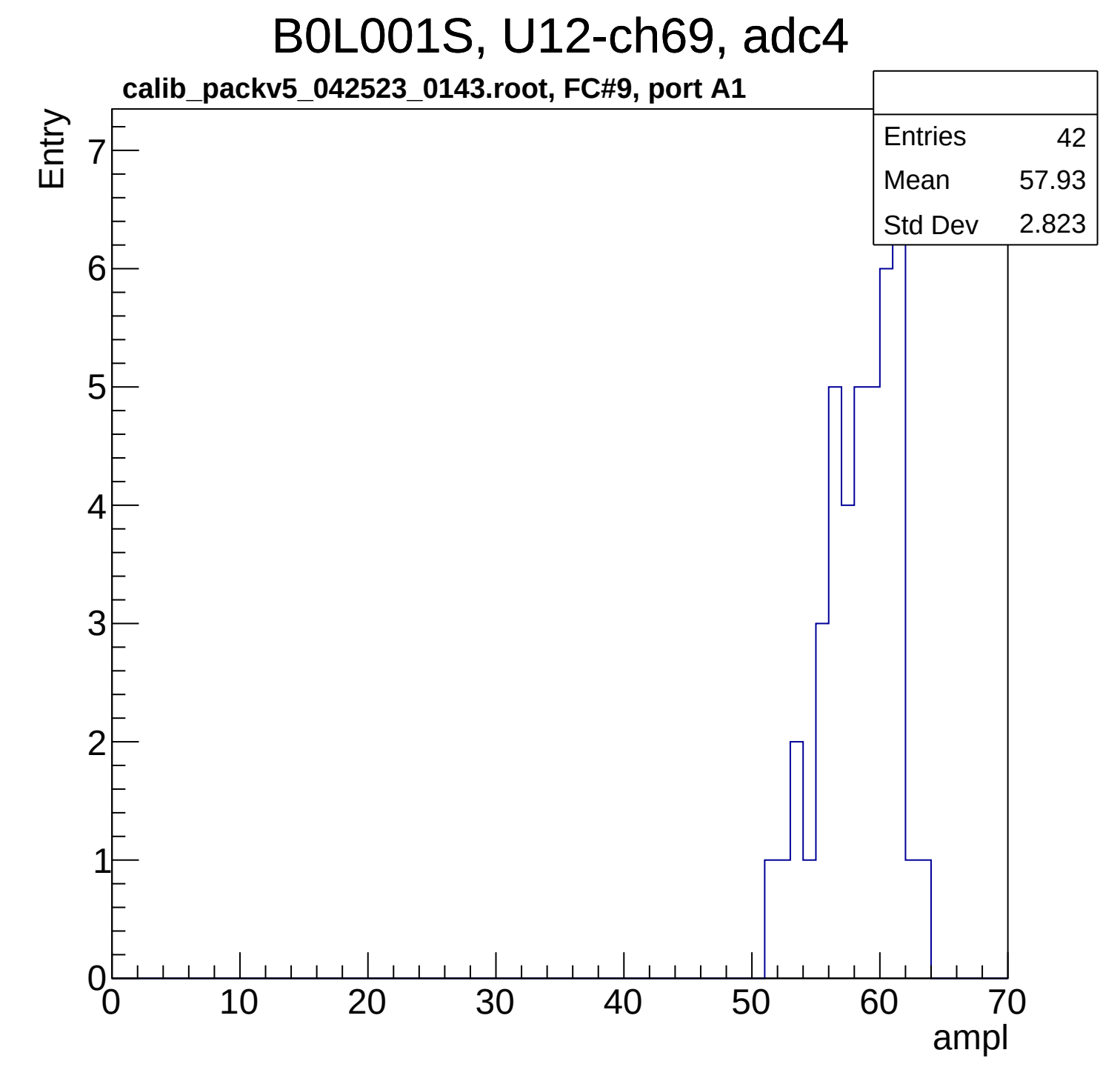
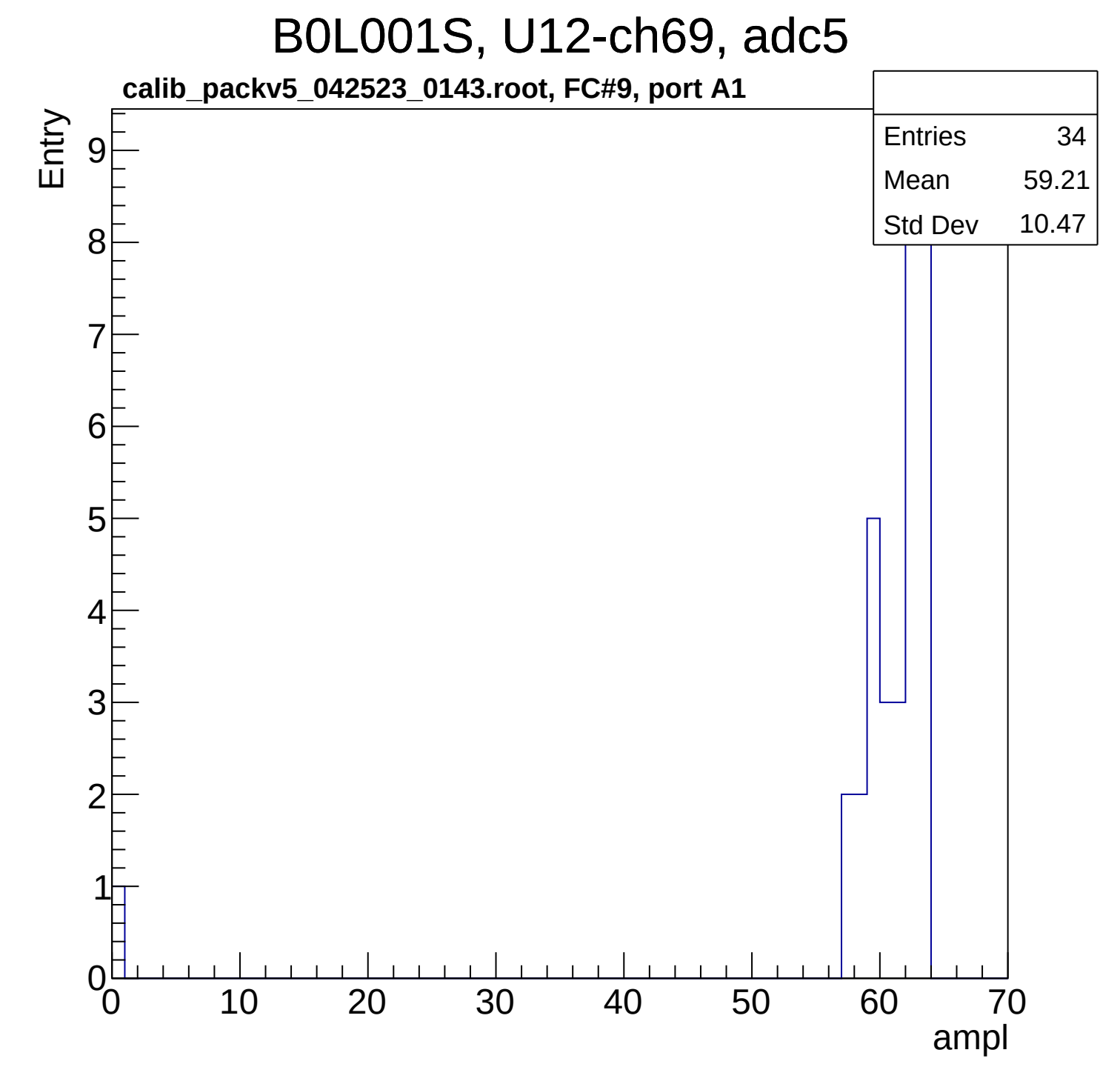

B0L001S, U12-ch69, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 42
Mean 57.93
Std Dev 2.823
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch69, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 34
Mean 59.21
Std Dev 10.47
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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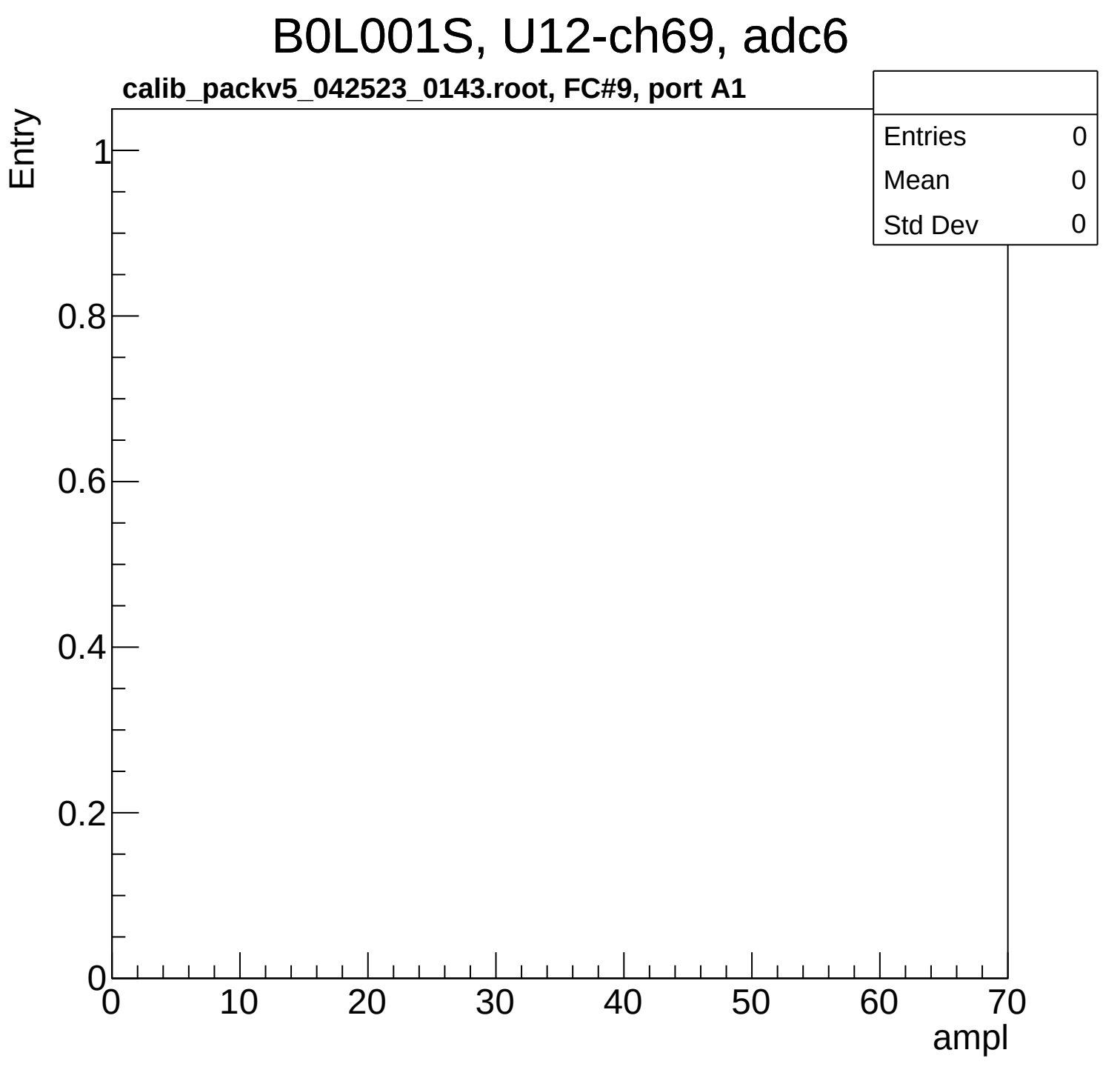
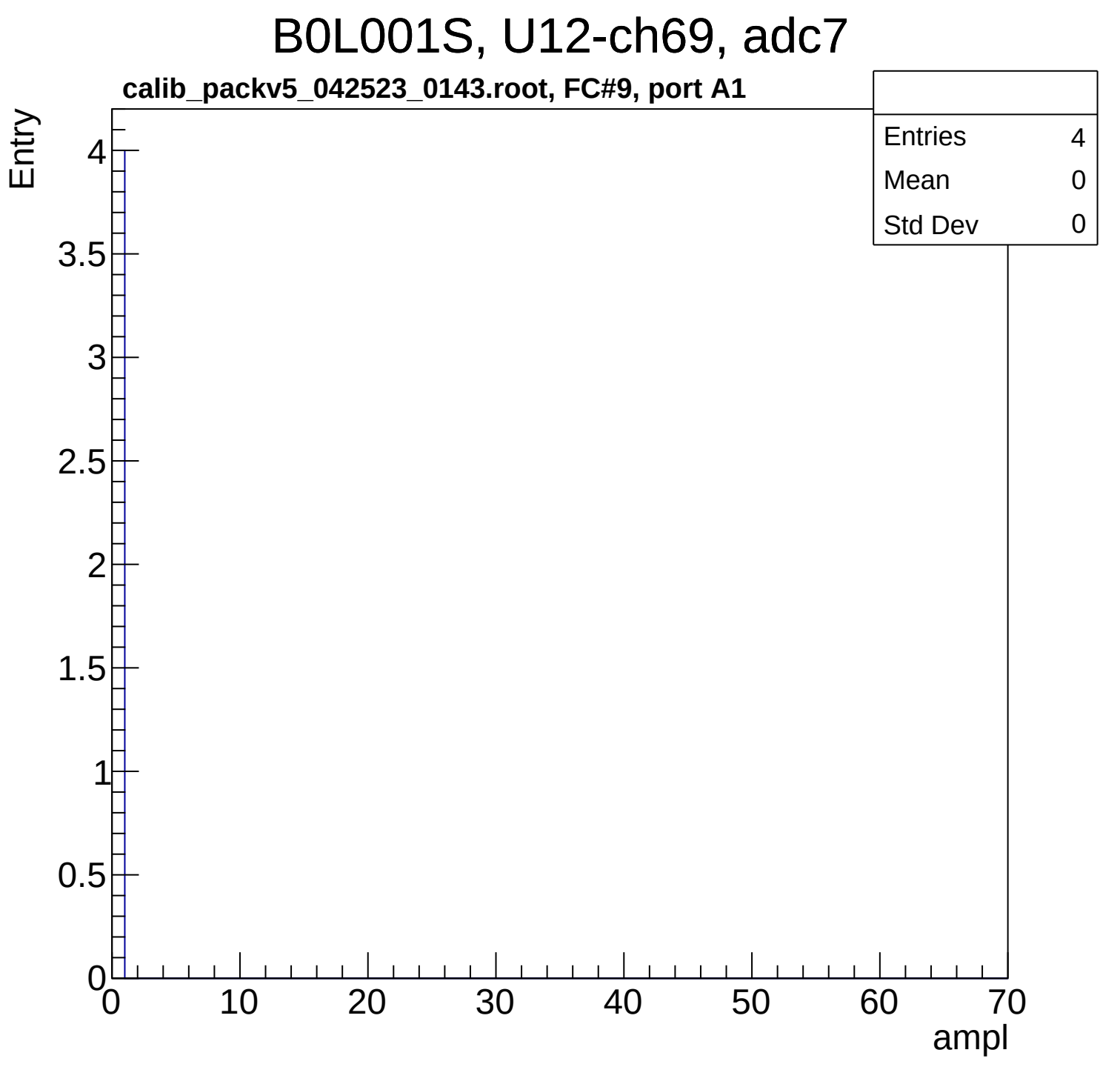
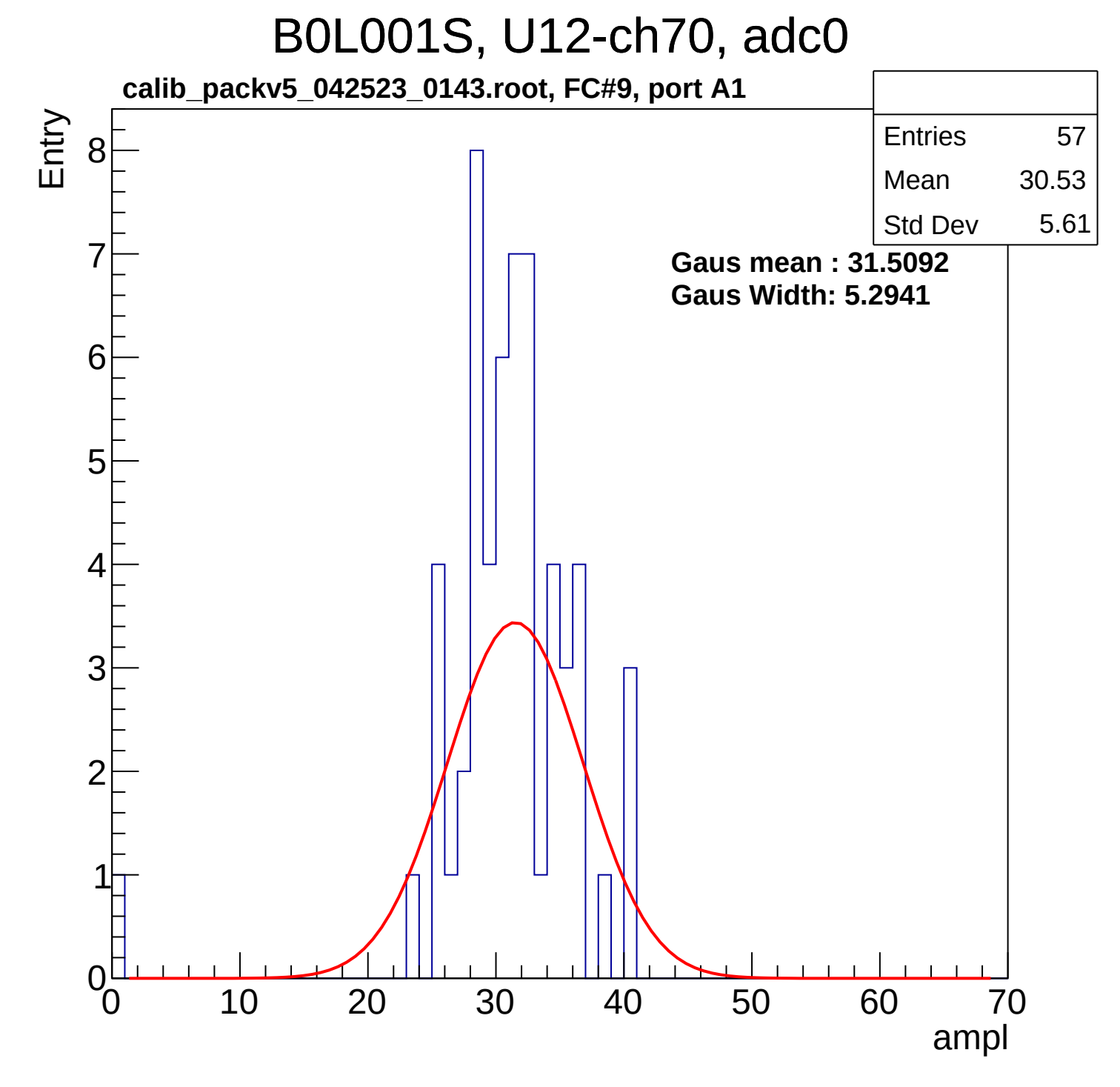
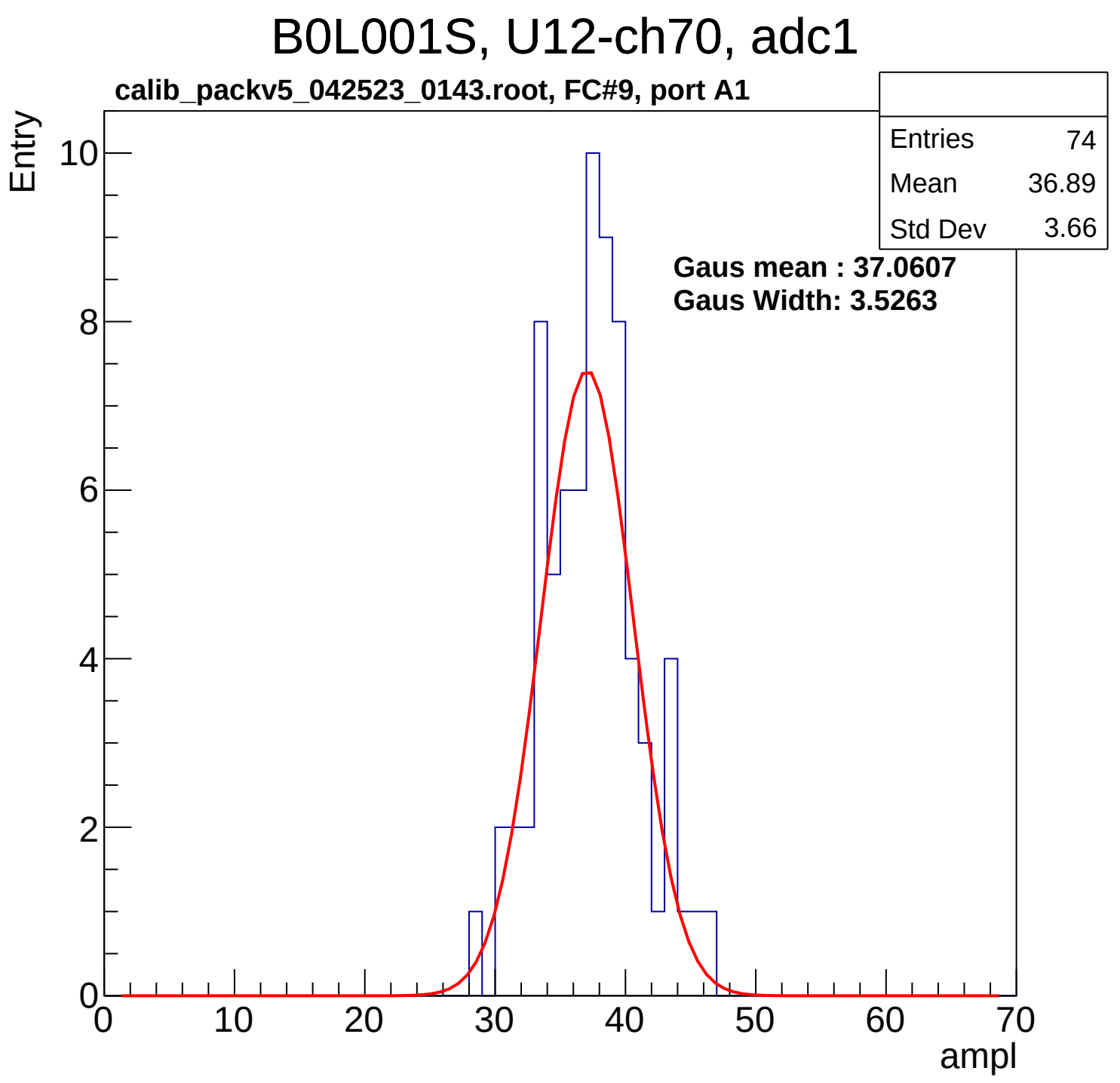
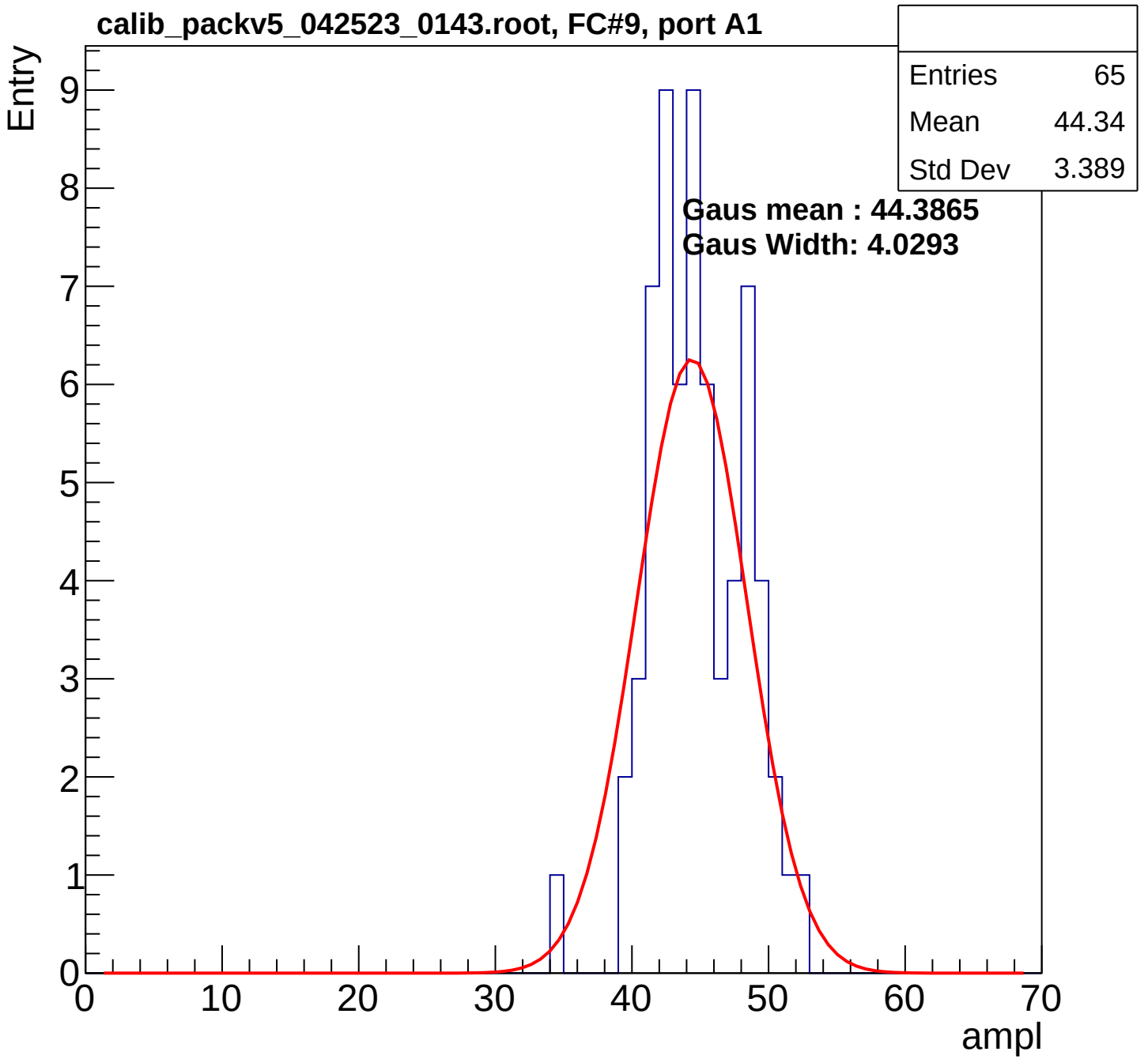
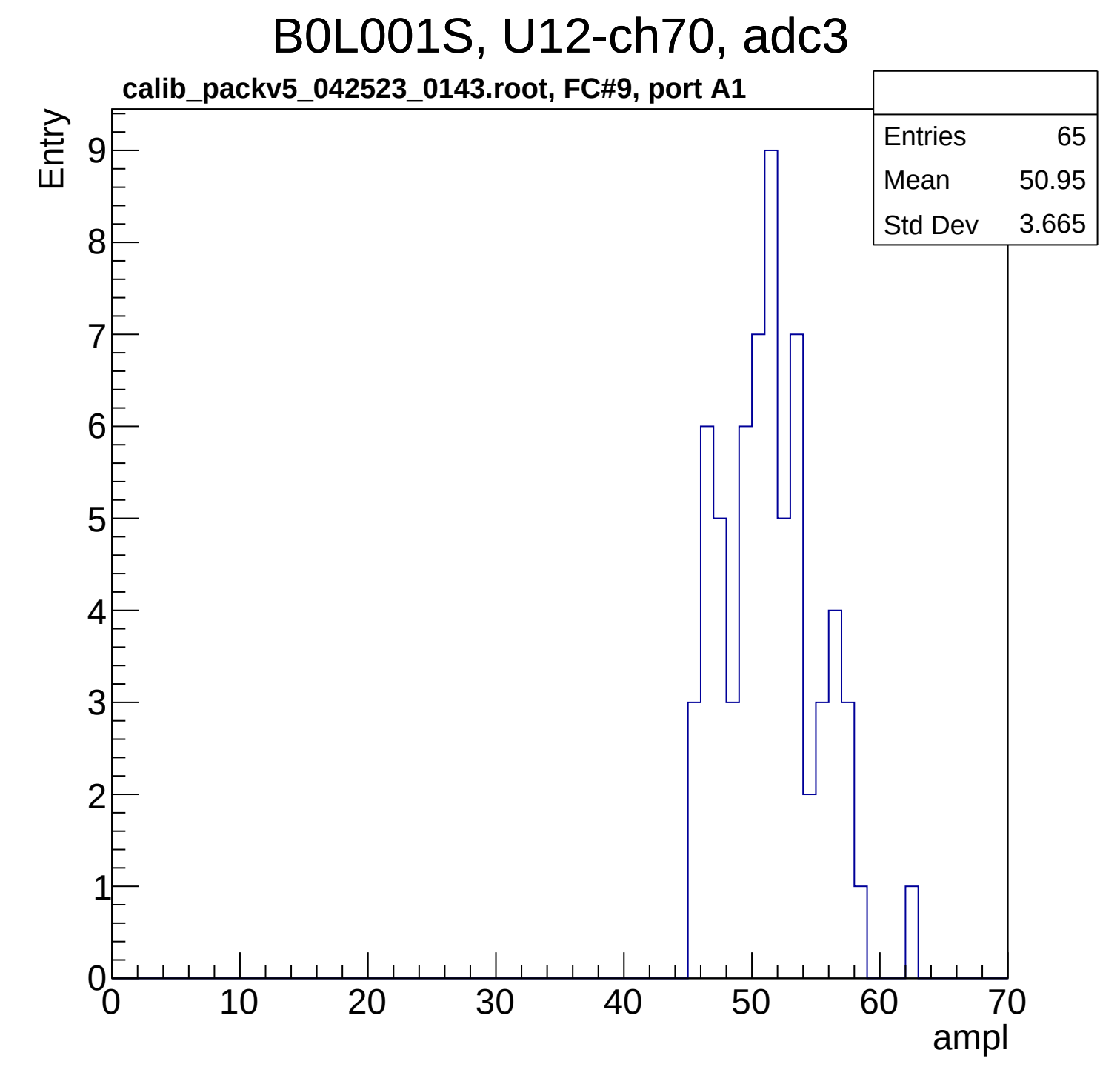

B0L001S, U12-ch69, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

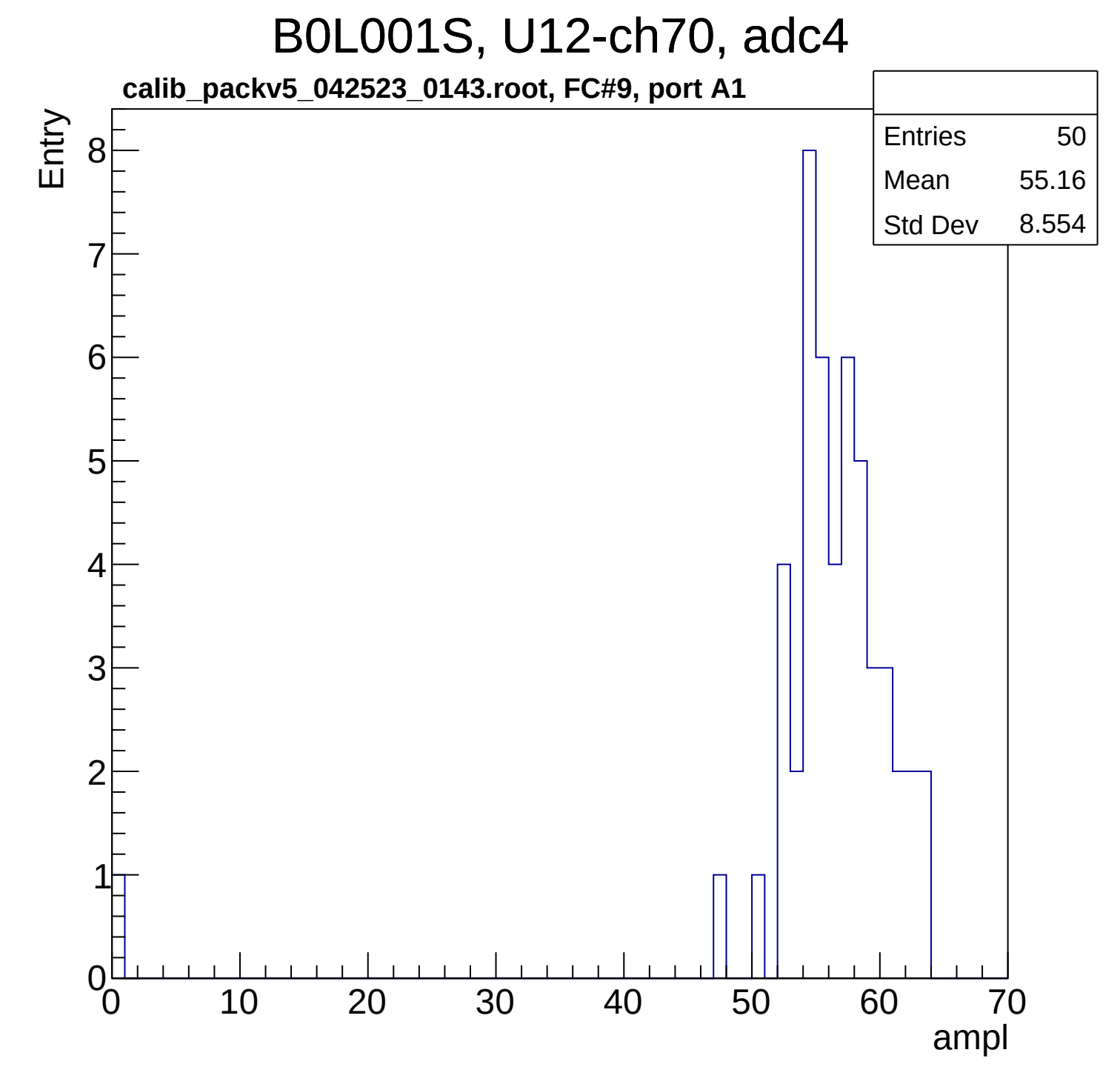

B0L001S, U12-ch69, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 4
Mean 0
Std Dev 0
Entry
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch70, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 57
Mean 30.53
Std Dev 5.61
Gaus mean : 31.5092
Gaus Width: 5.2941
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch70, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 74
Mean 36.89
Std Dev 3.66
Gaus mean : 37.0607
Gaus Width: 3.5263
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch70, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 65
Mean 44.34
Std Dev 3.389
Gaus mean : 44.3865
Gaus Width: 4.0293
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch70, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 65
Mean 50.95
Std Dev 3.665
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch70, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 50
Mean 55.16
Std Dev 8.554
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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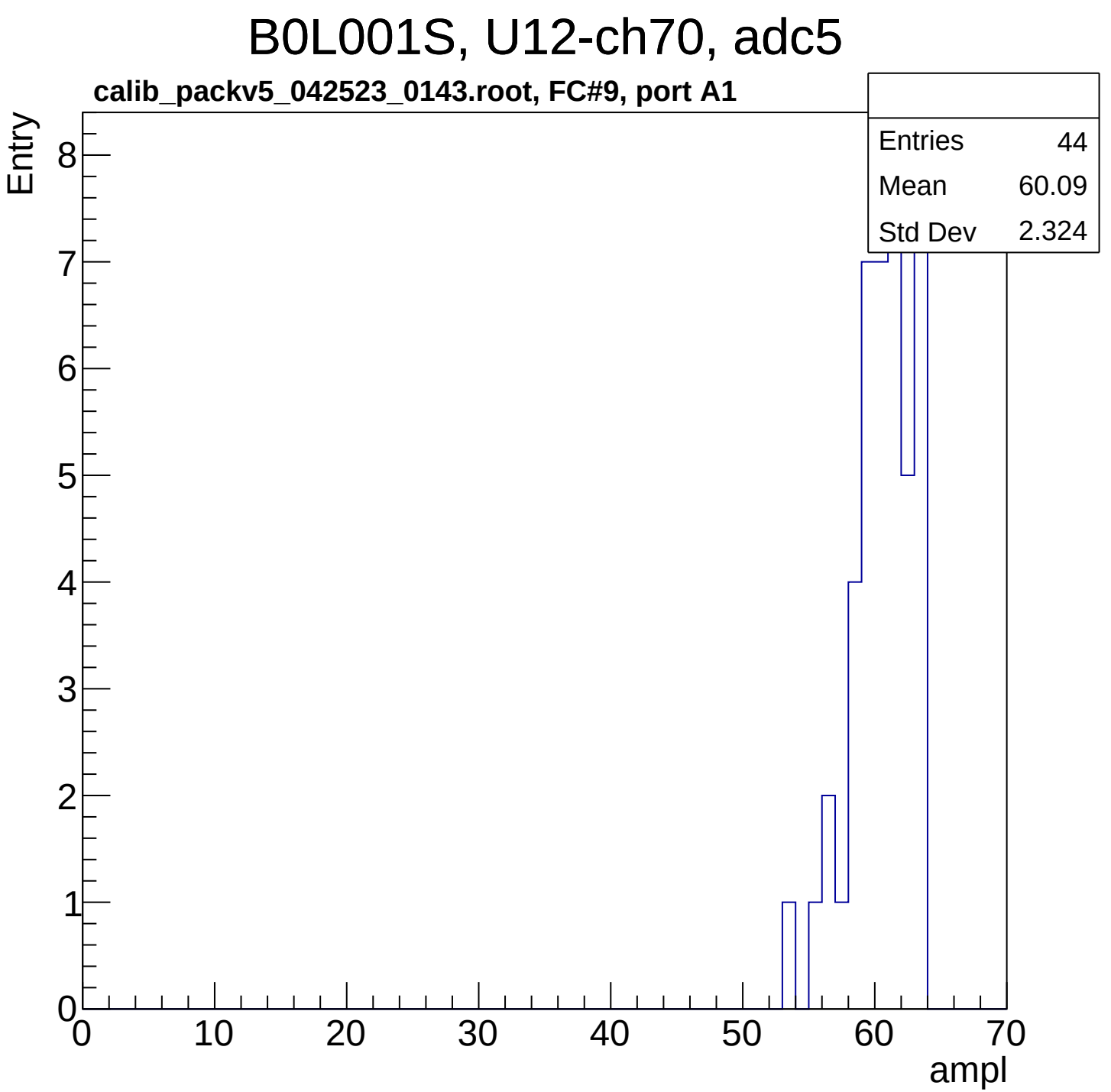
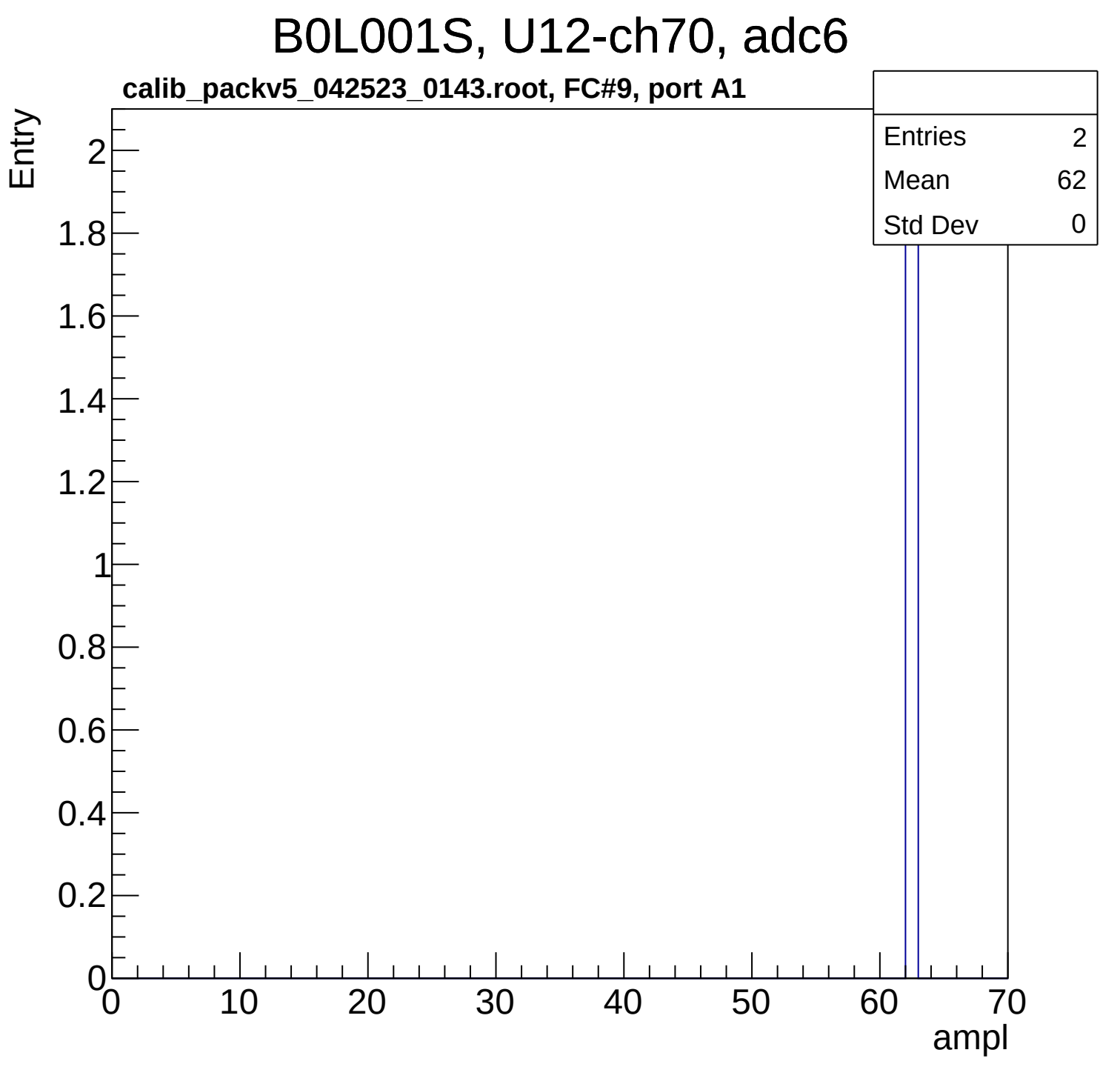
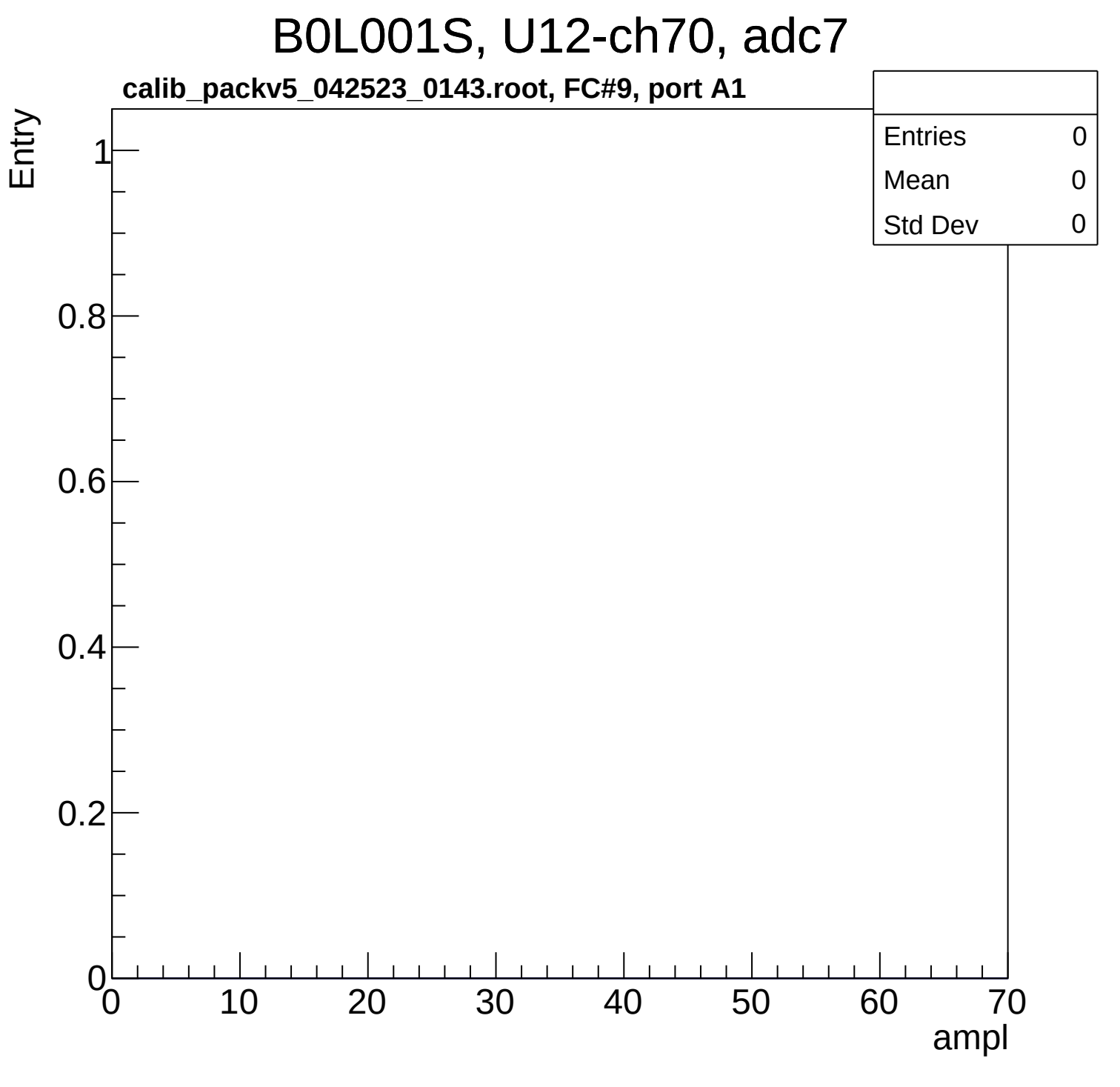
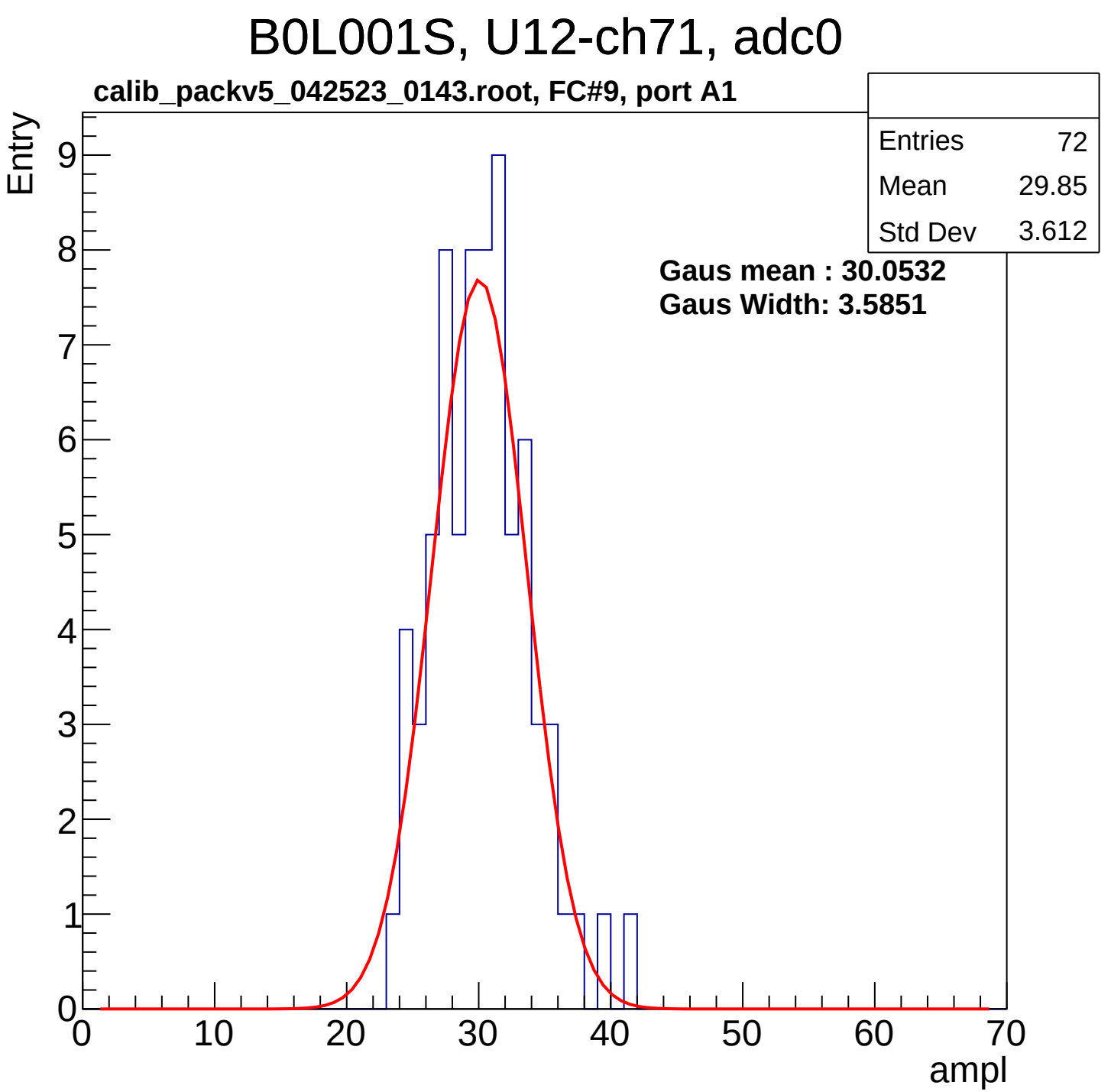
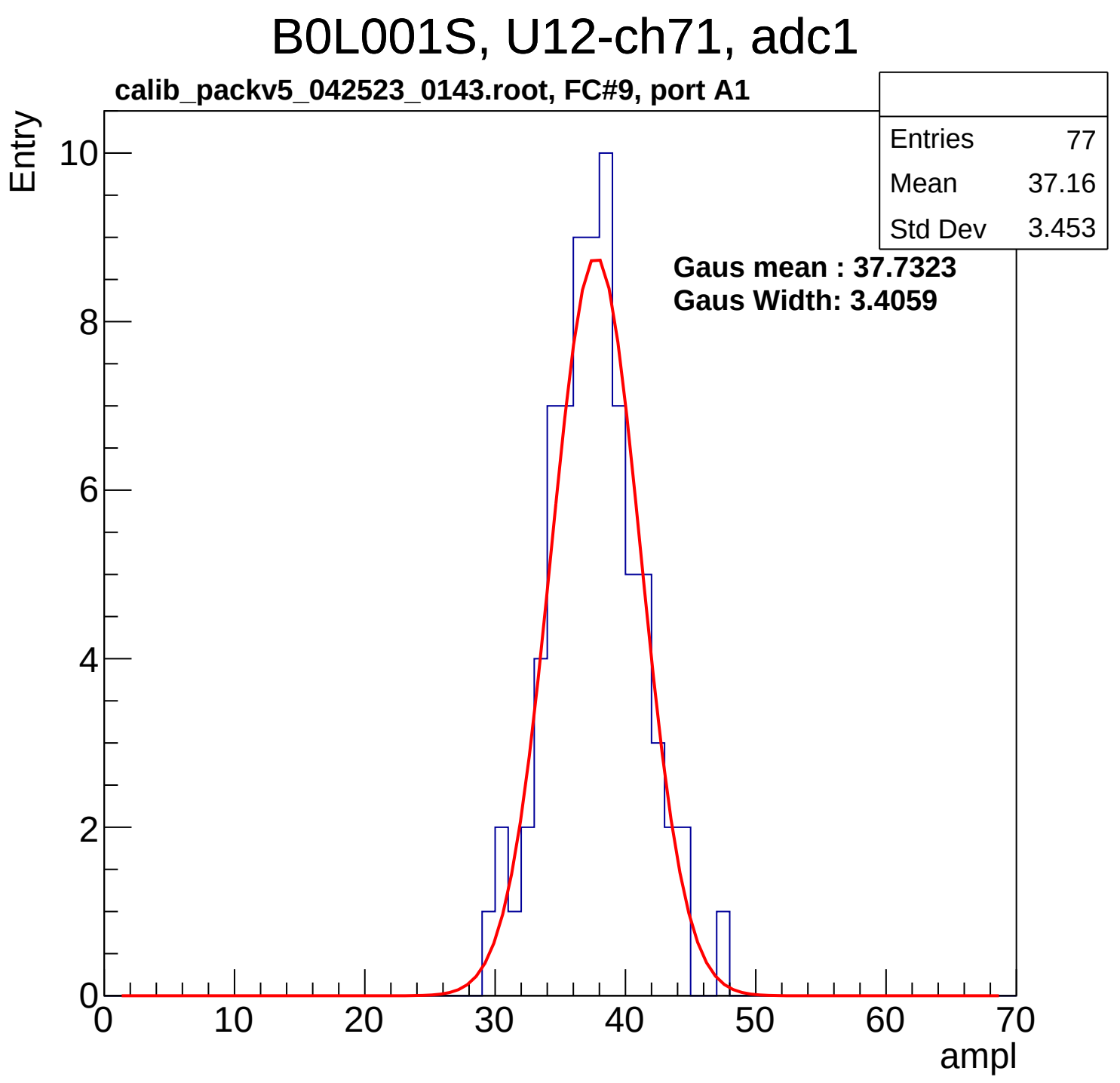
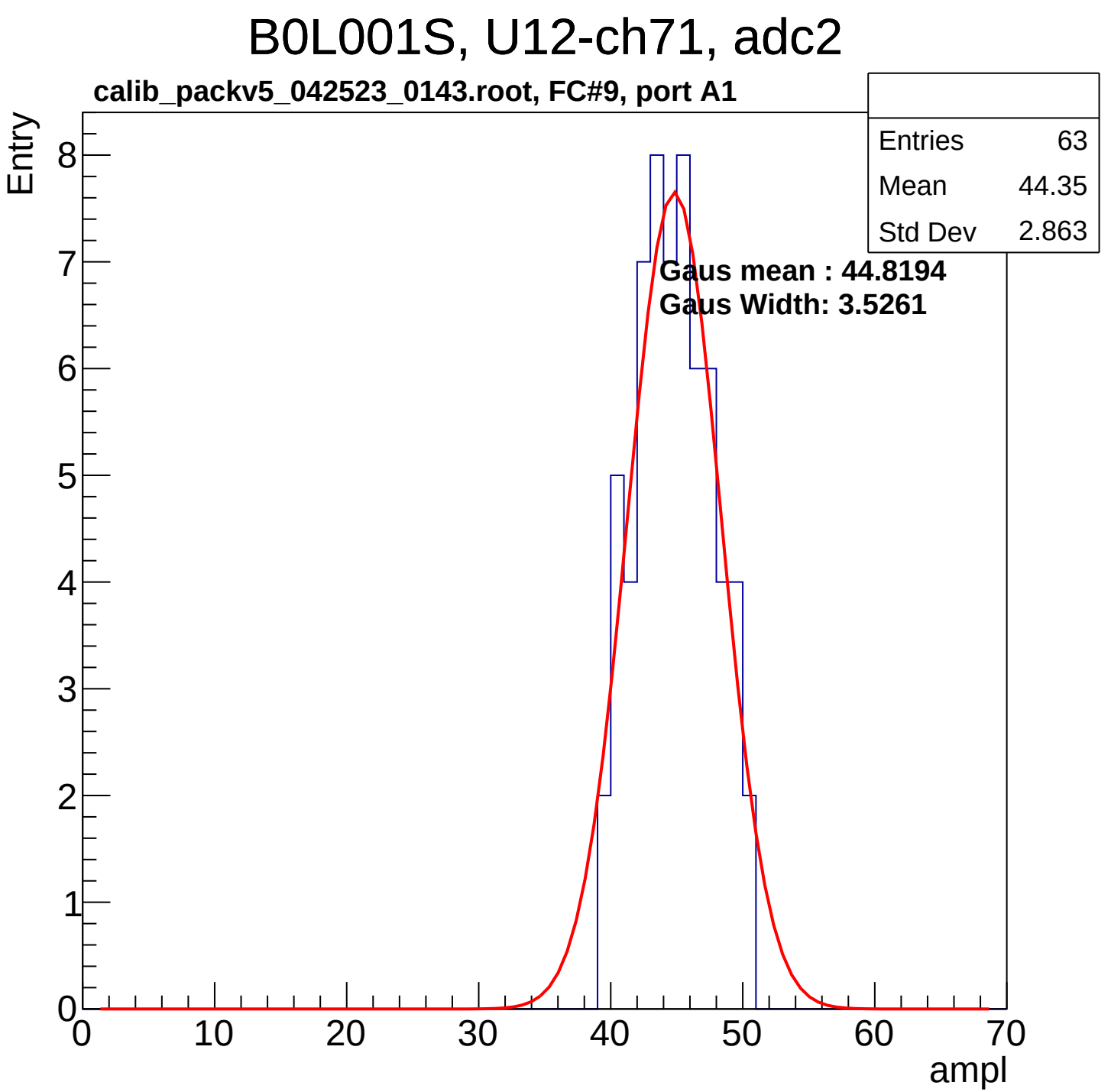

B0L001S, U12-ch70, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 44
Mean 60.09
Std Dev 2.324
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

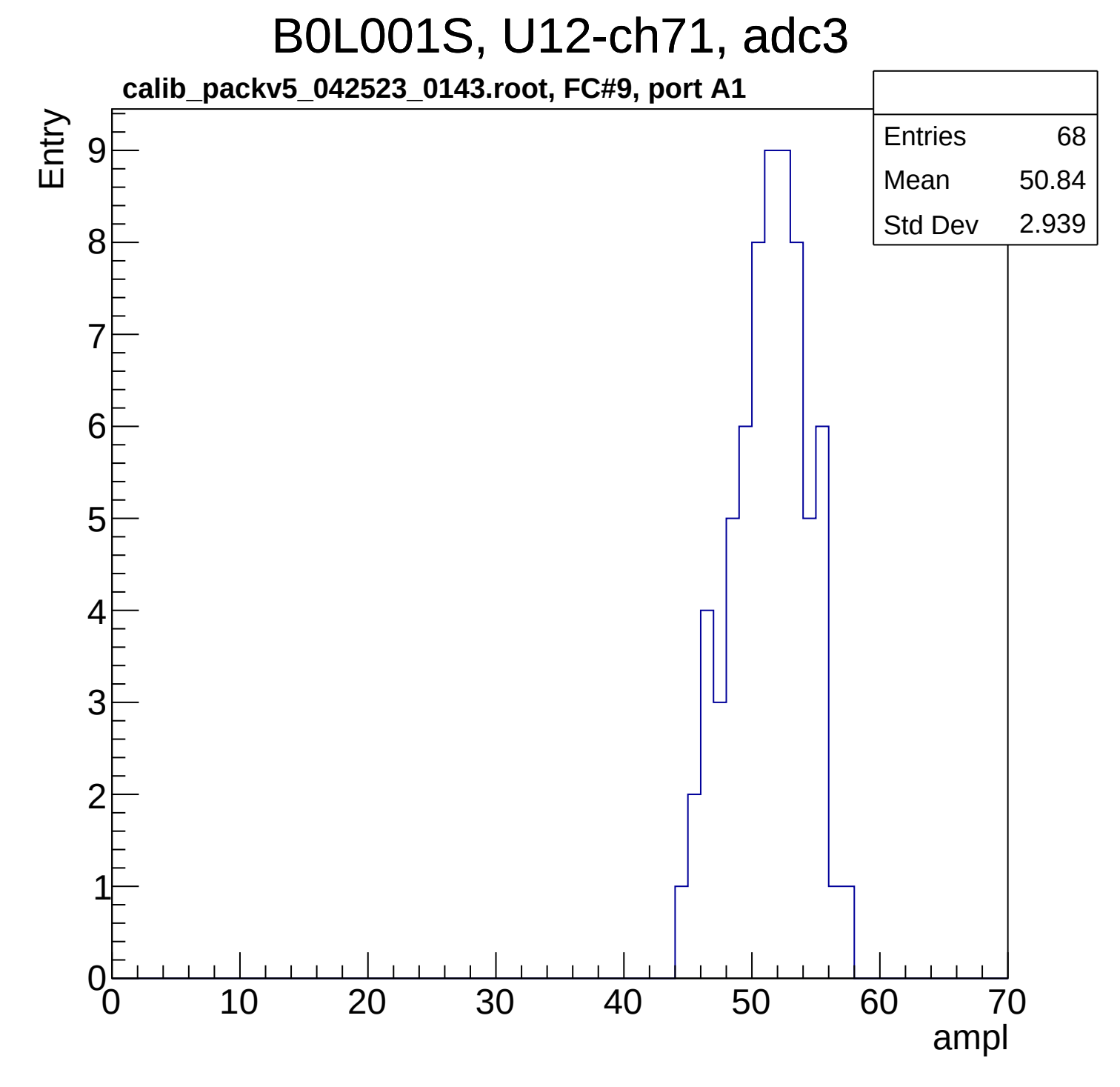

B0L001S, U12-ch70, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 62
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

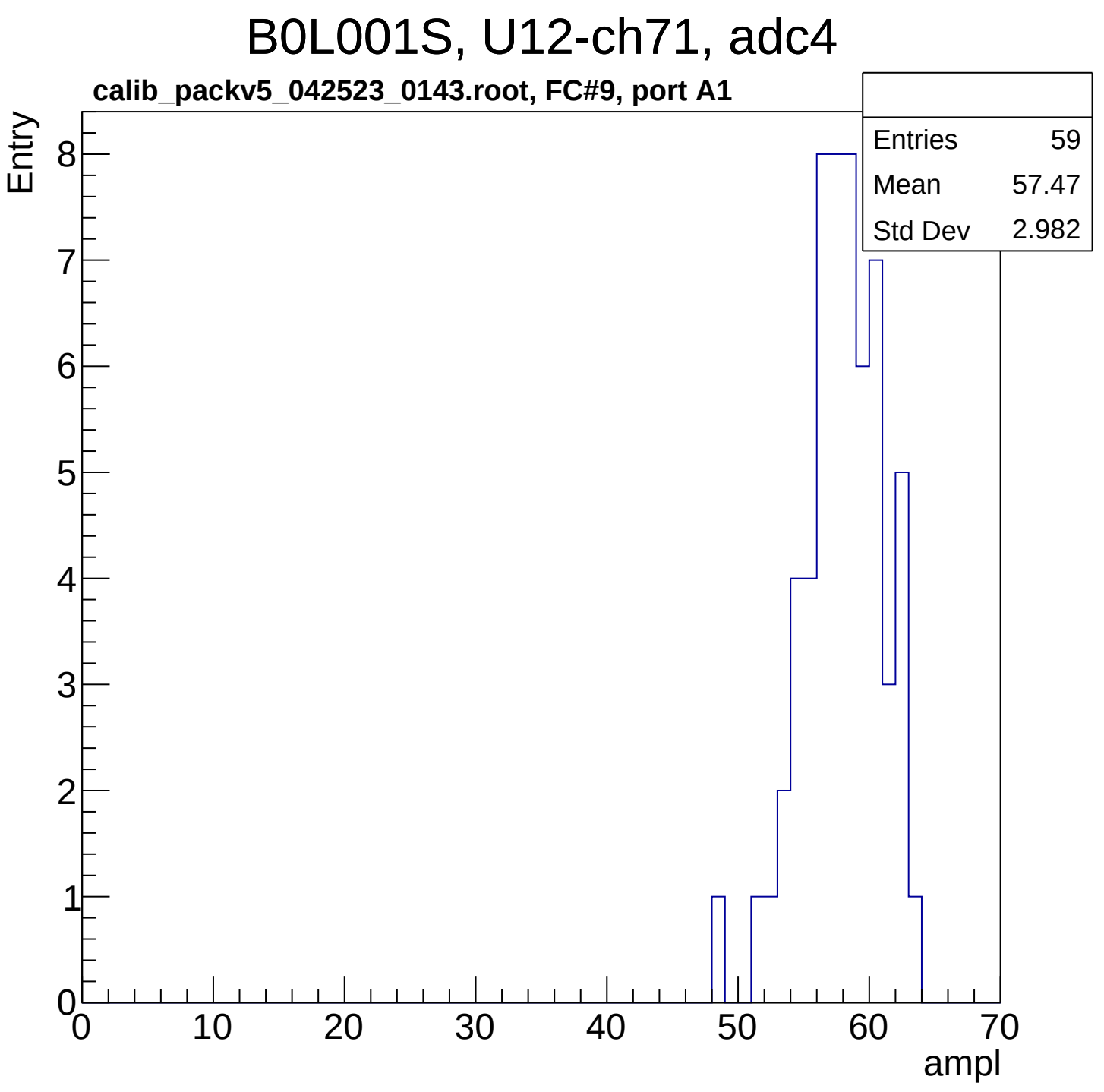

B0L001S, U12-ch70, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch71, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 72
Mean 29.85
Std Dev 3.612
Gaus mean : 30.0532
Gaus Width: 3.5851
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch71, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 77
Mean 37.16
Std Dev 3.453
Gaus mean : 37.7323
Gaus Width: 3.4059
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch71, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 63
Mean 44.35
Std Dev 2.863
Gaus mean : 44.8194
Gaus Width: 3.5261
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch71, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 68
Mean 50.84
Std Dev 2.939
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch71, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 59
Mean 57.47
Std Dev 2.982
Entry
ampl
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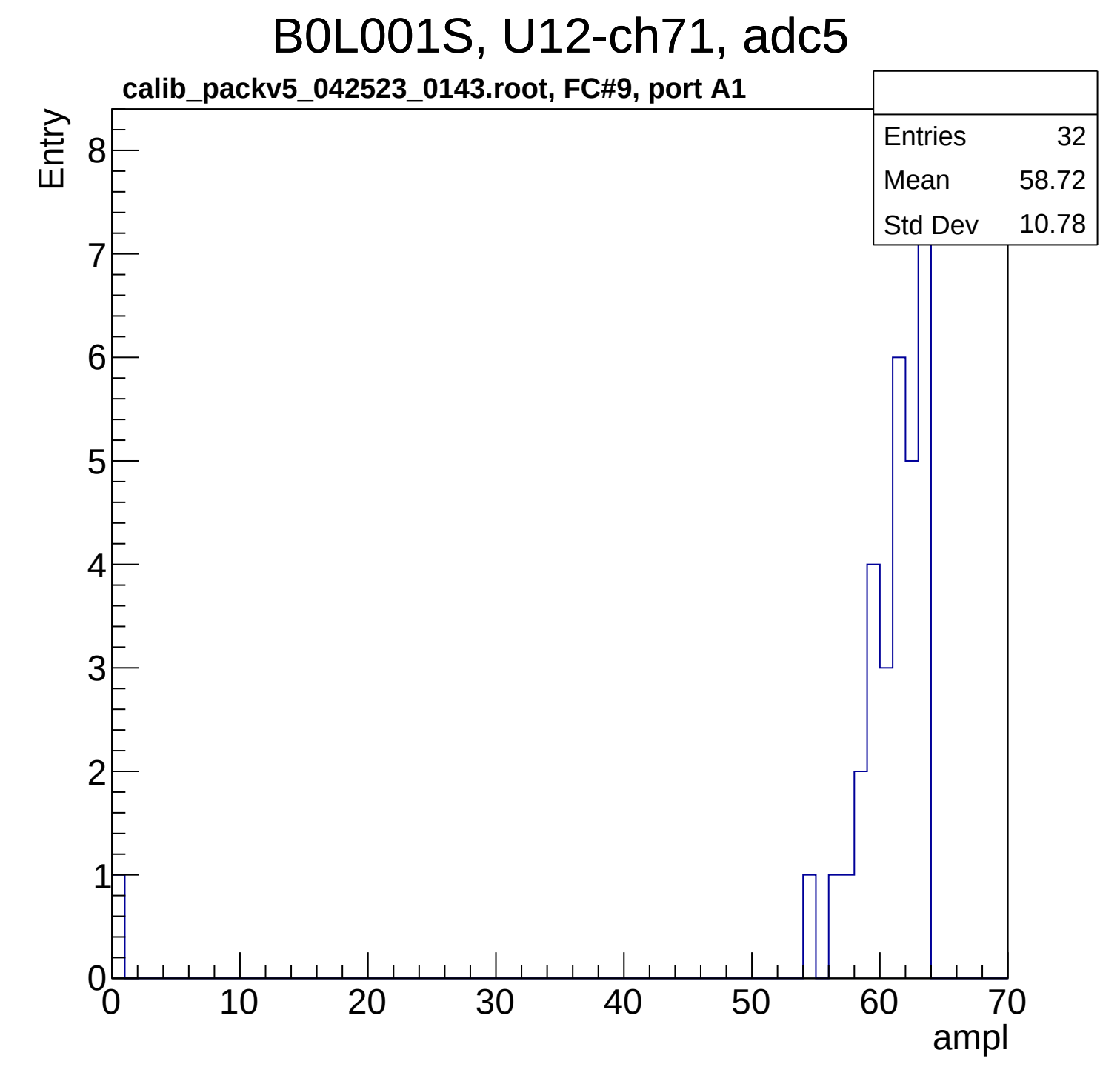
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch71, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 32
Mean 58.72
Std Dev 10.78
Entry
ampl
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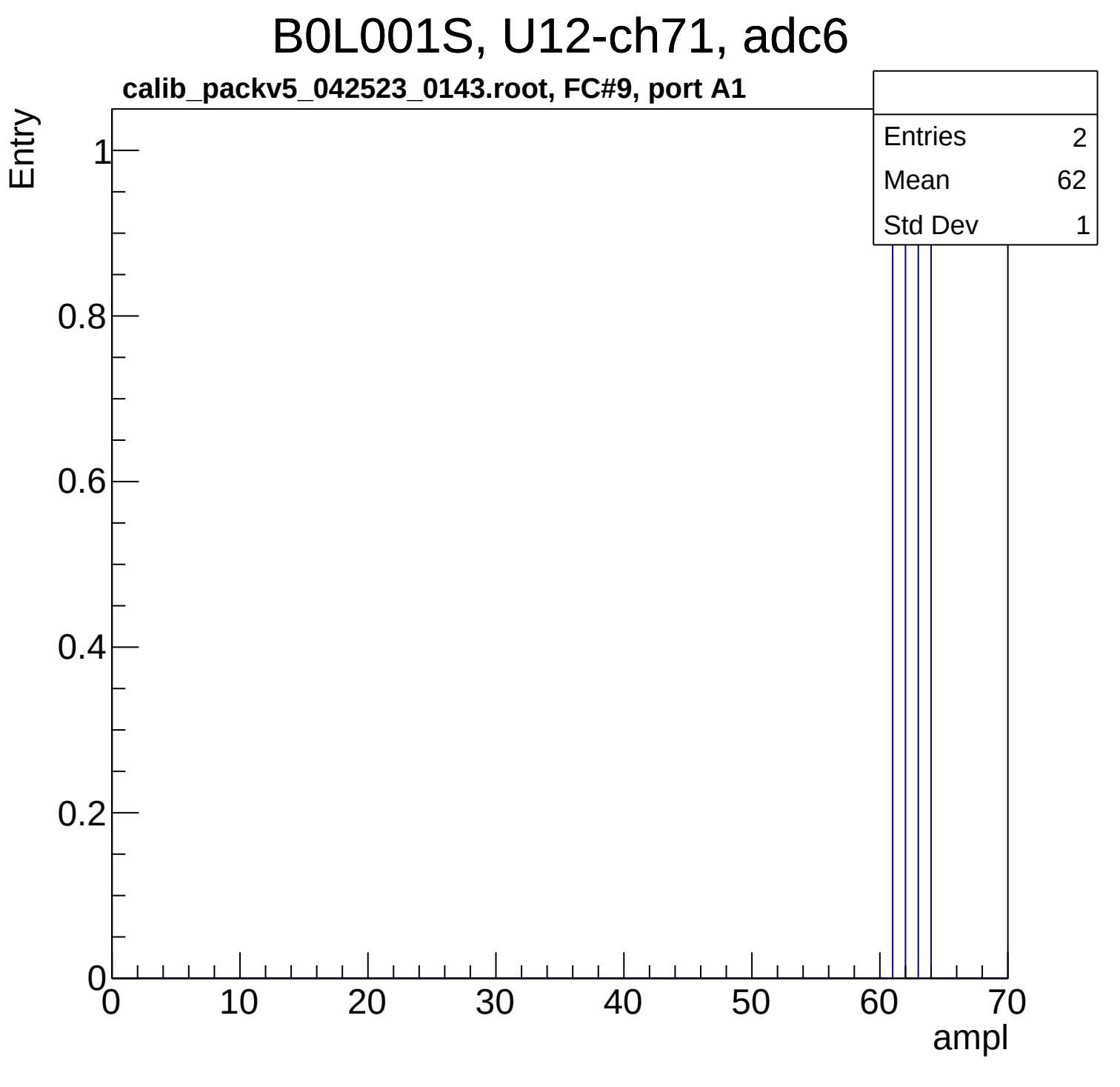
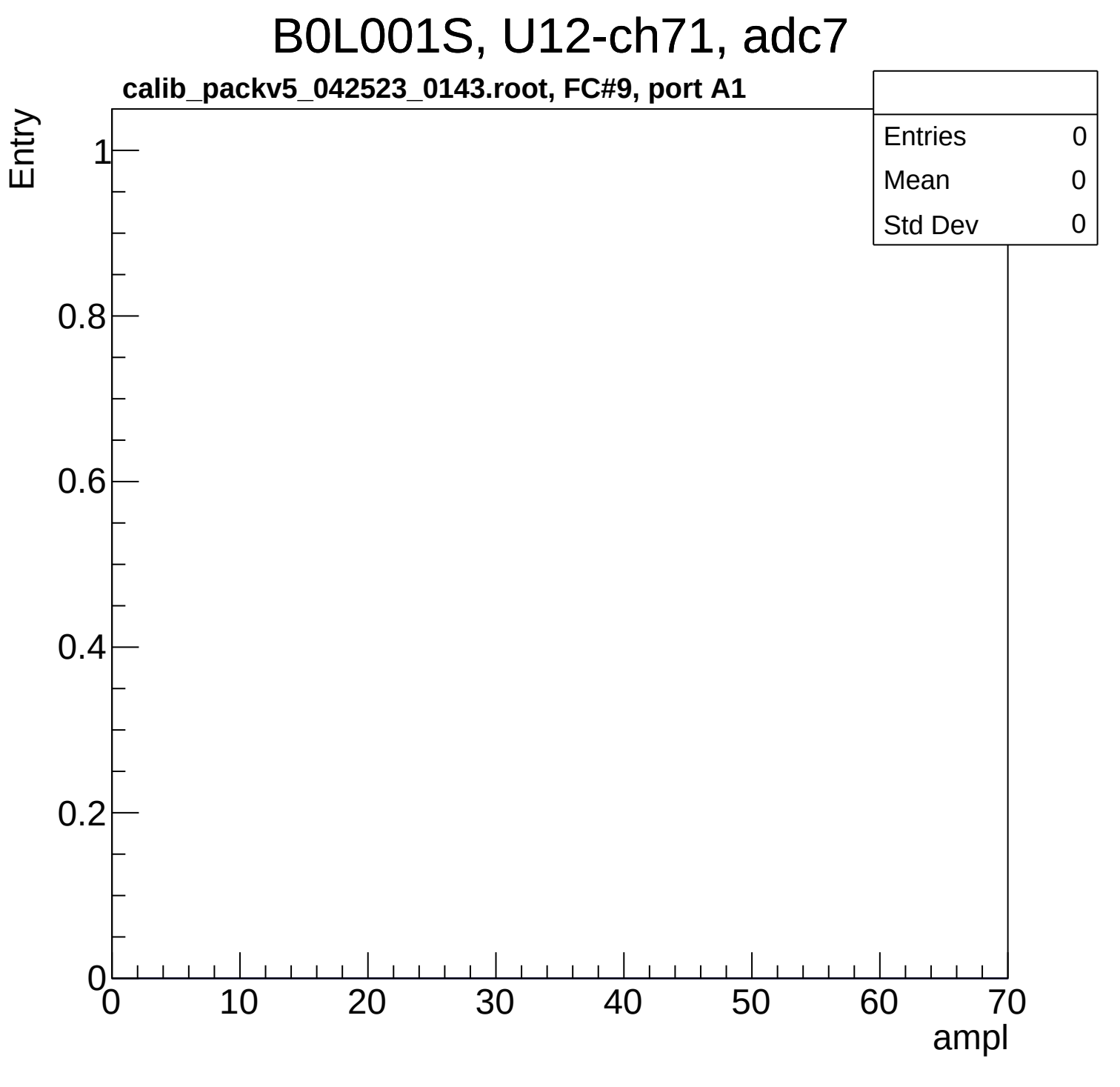
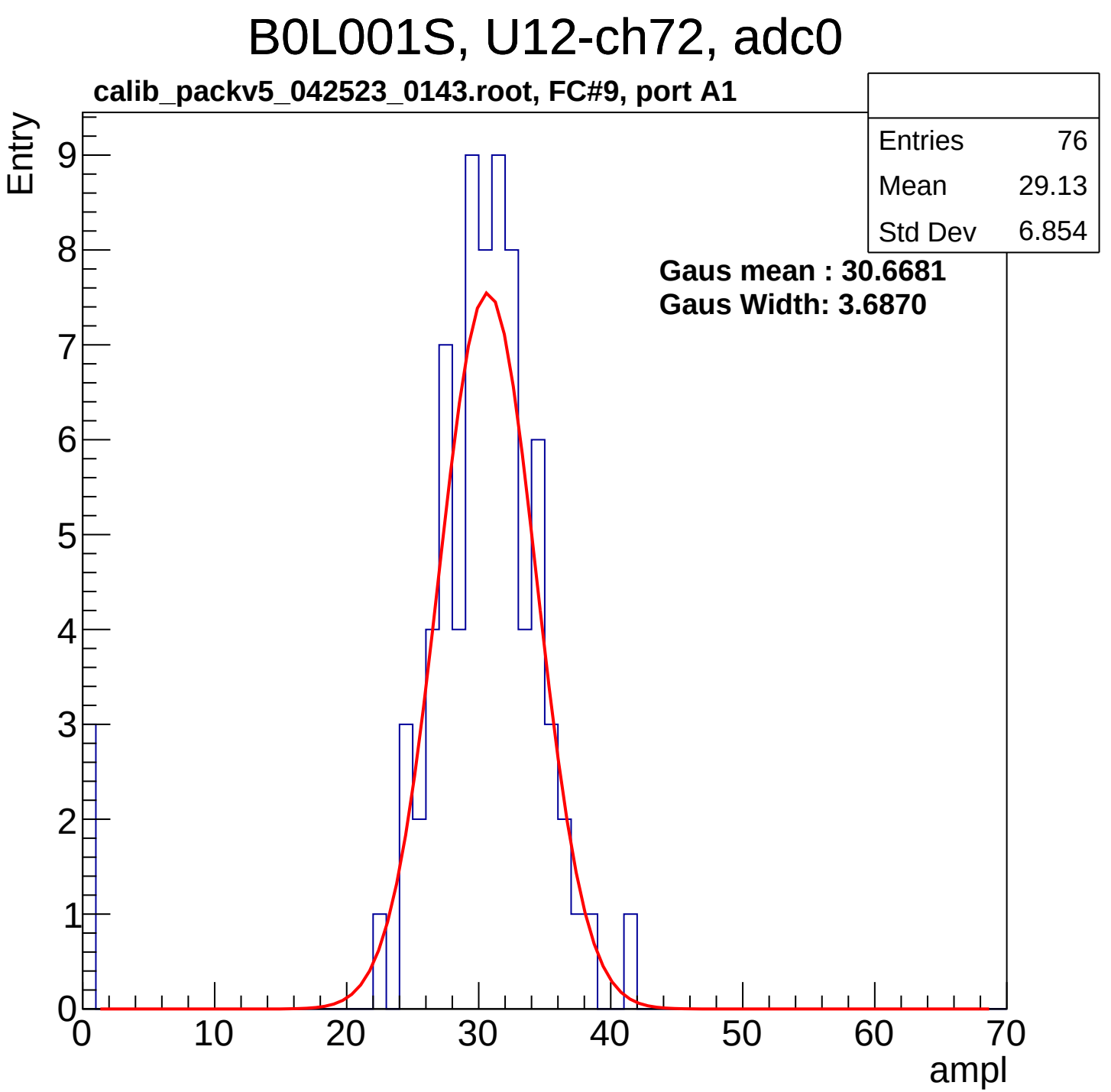
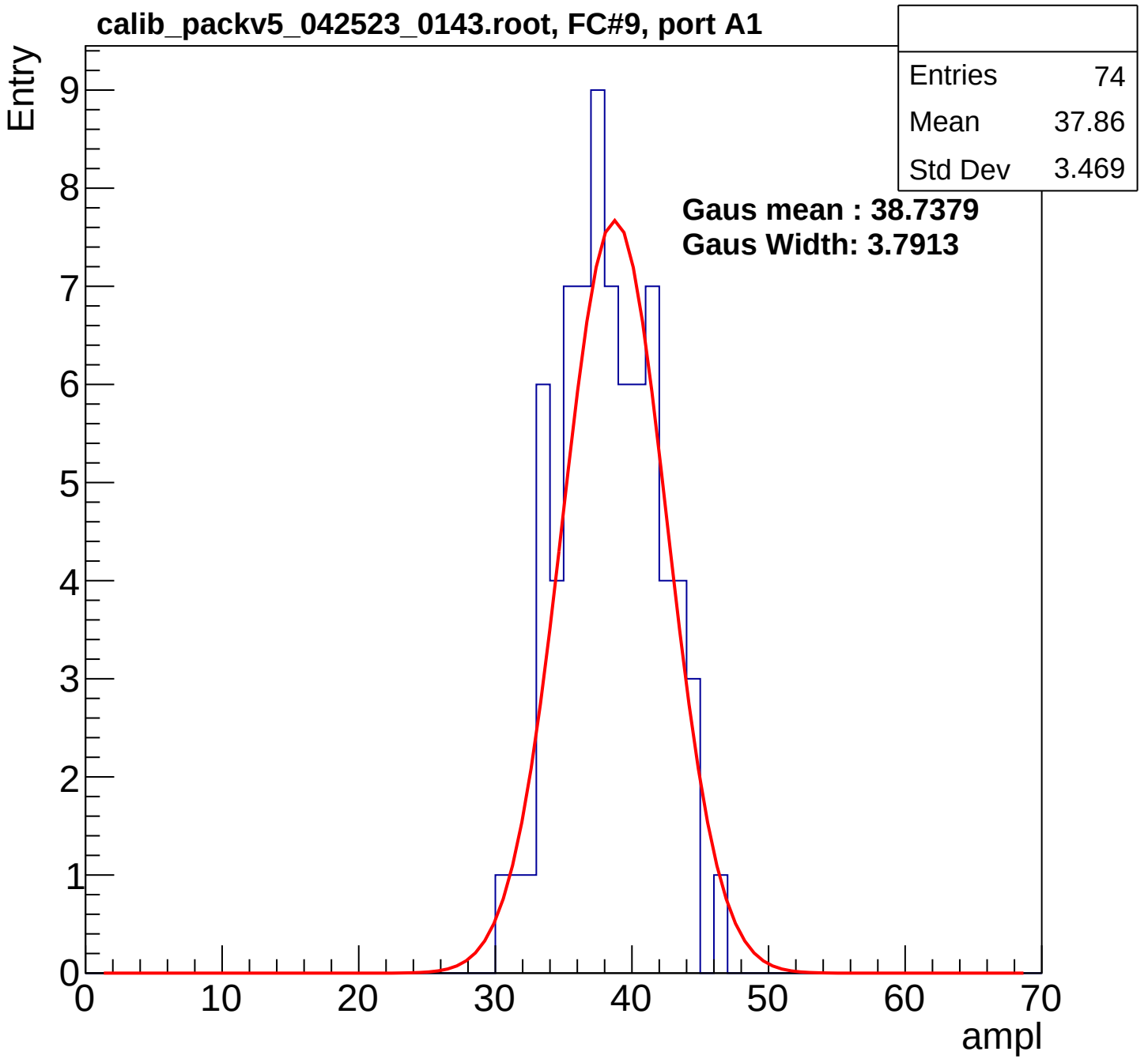
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch71, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 62
Std Dev 1
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch71, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch72, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 76
Mean 29.13
Std Dev 6.854
Gaus mean : 30.6681
Gaus Width: 3.6870
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch72, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 74
Mean 37.86
Std Dev 3.469
Gaus mean : 38.7379
Gaus Width: 3.7913
Entry
ampl
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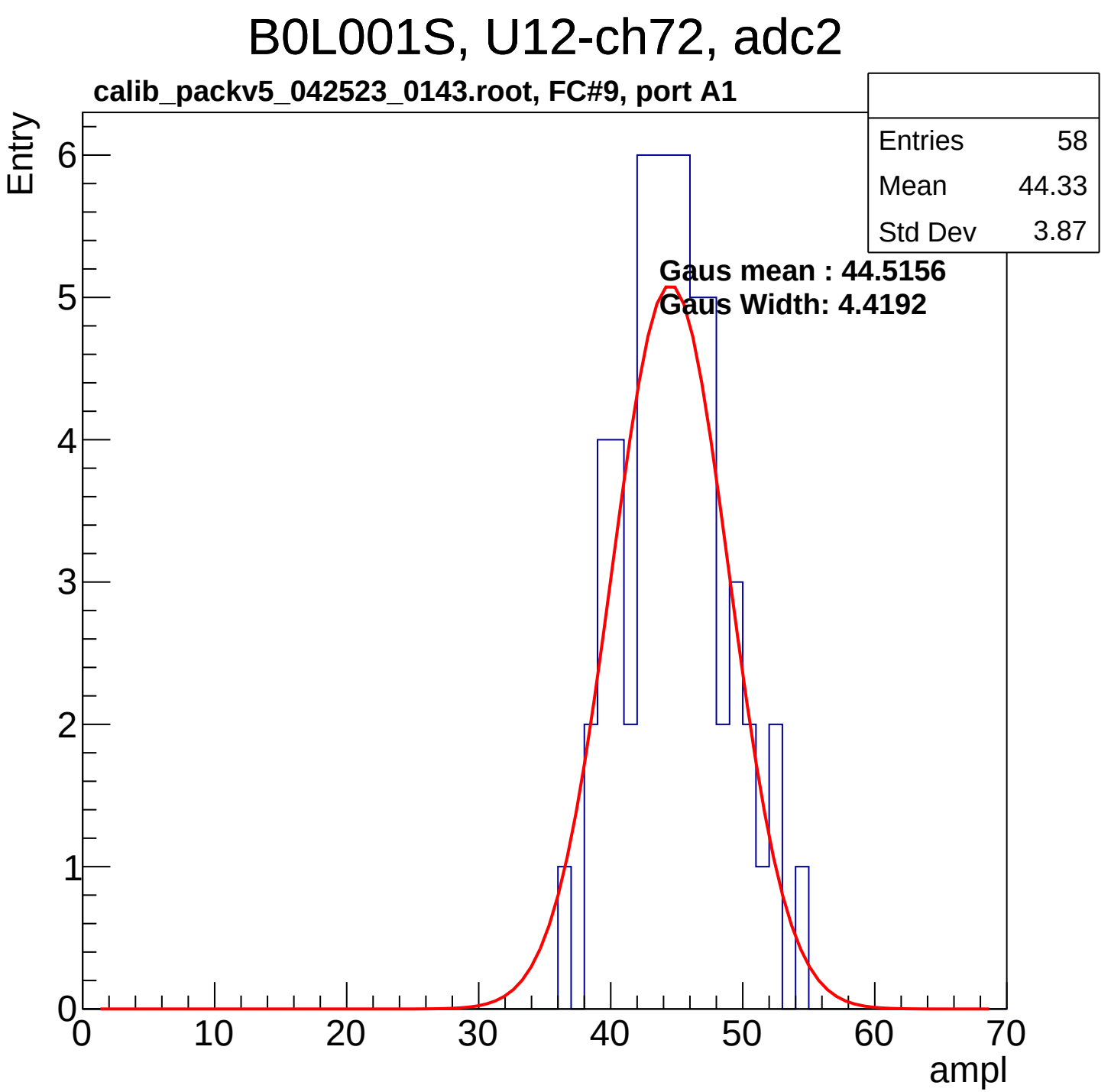
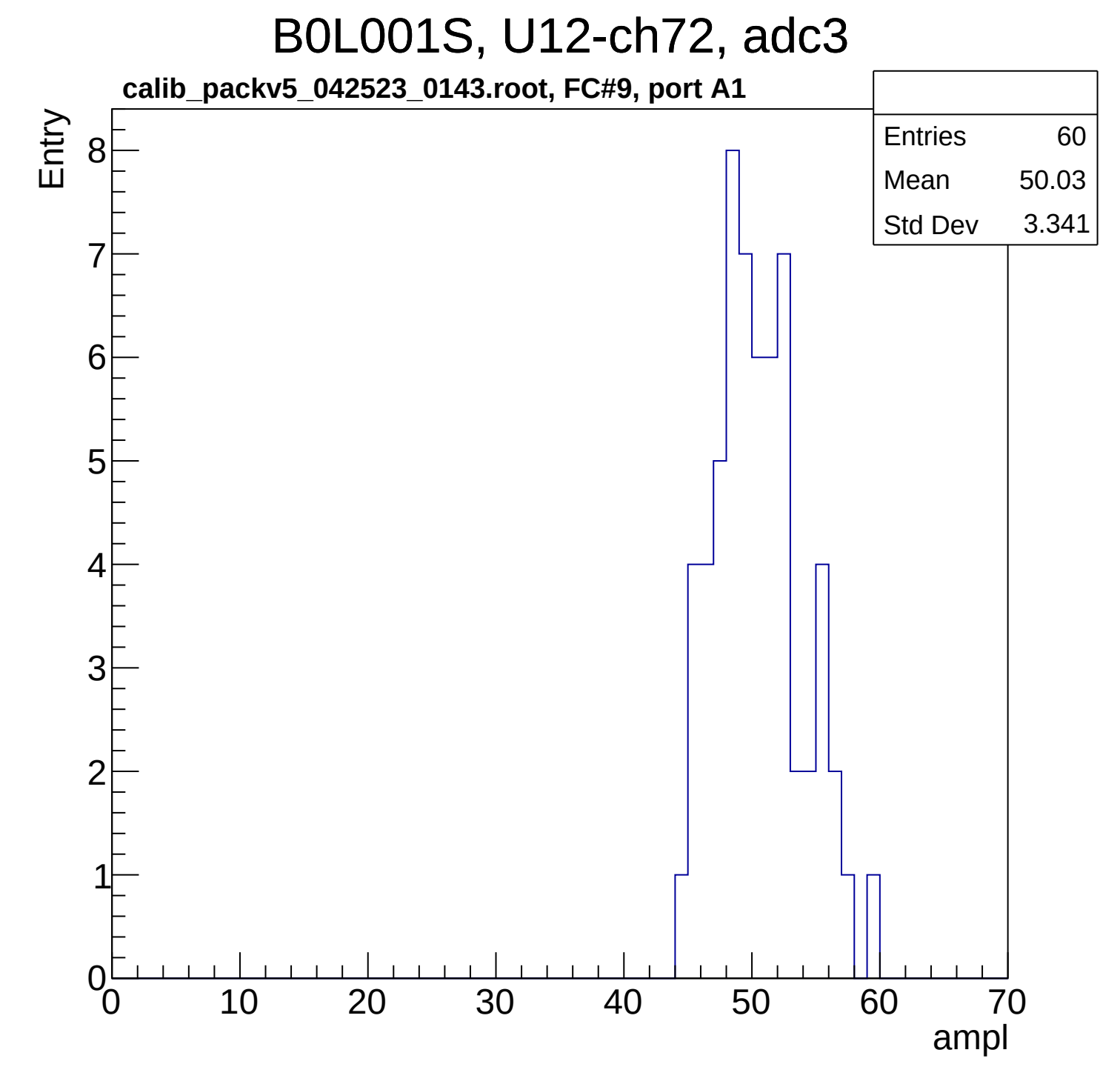
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch72, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 58
Mean 44.33
Std Dev 3.87
Gaus mean : 44.5156
Gaus Width: 4.4192
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B0L001S, U12-ch72, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 60
Mean 50.03
Std Dev 3.341
Entry
ampl
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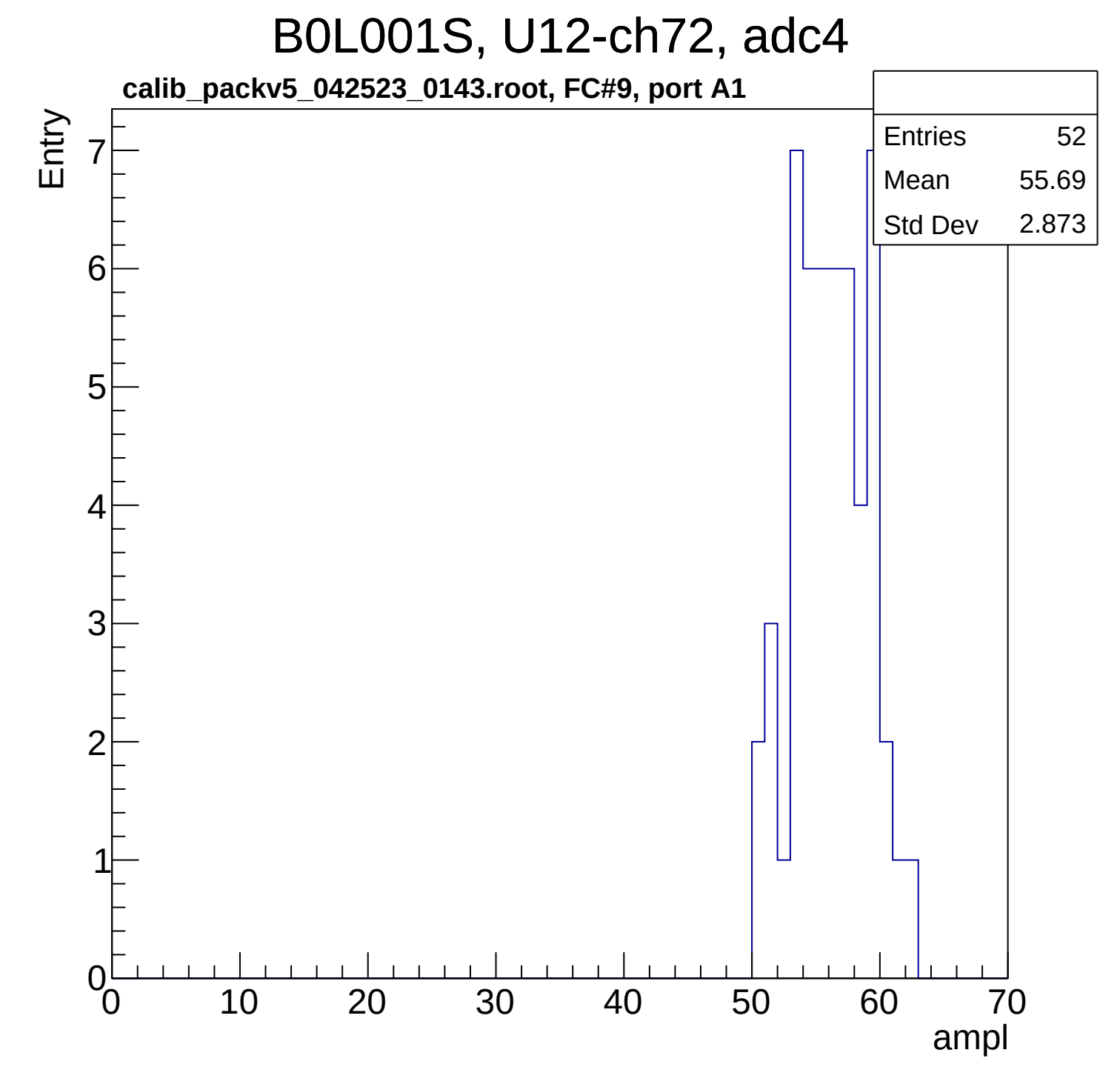
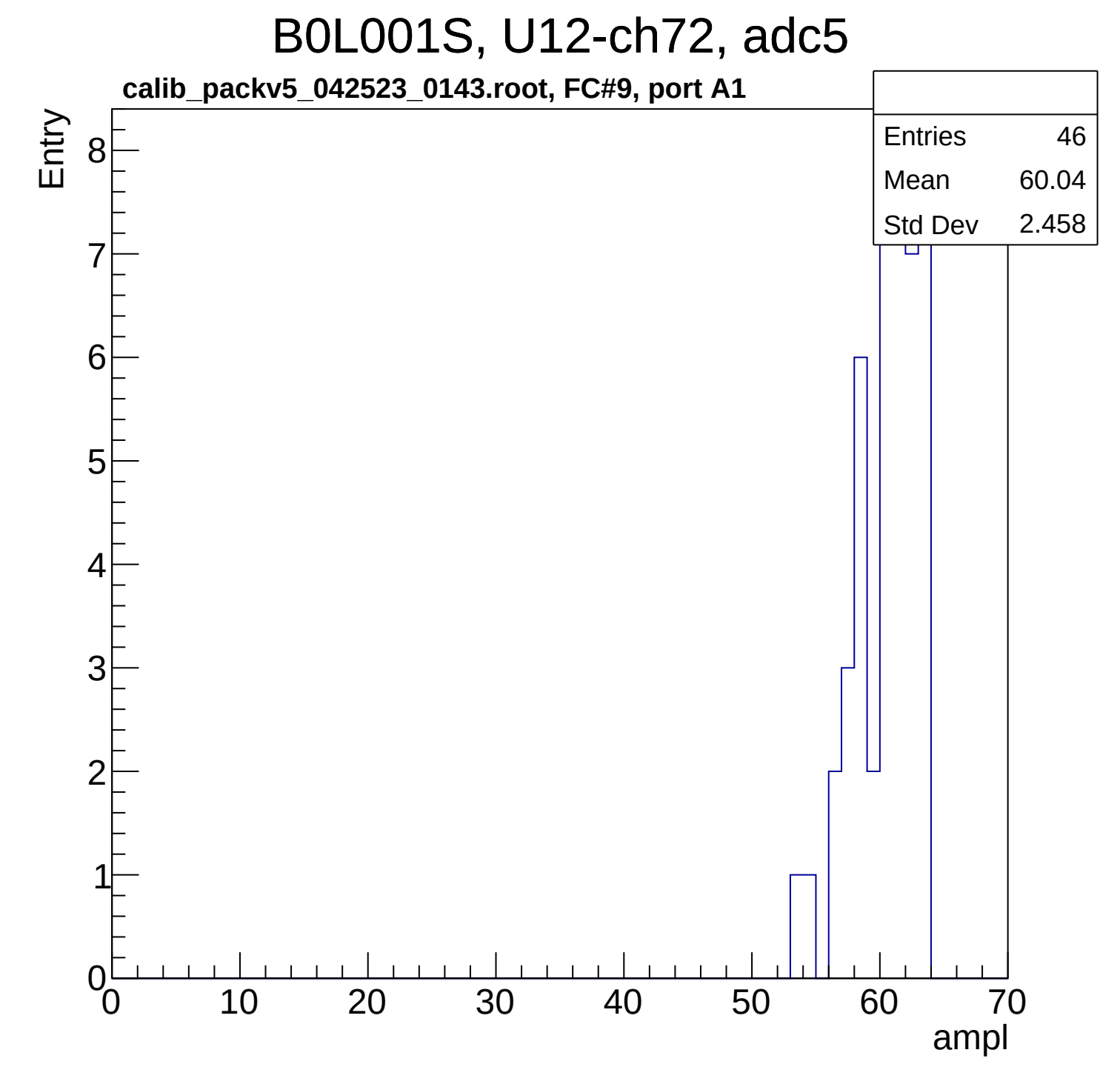
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch72, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 52
Mean 55.69
Std Dev 2.873
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B0L001S, U12-ch72, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 46
Mean 60.04
Std Dev 2.458
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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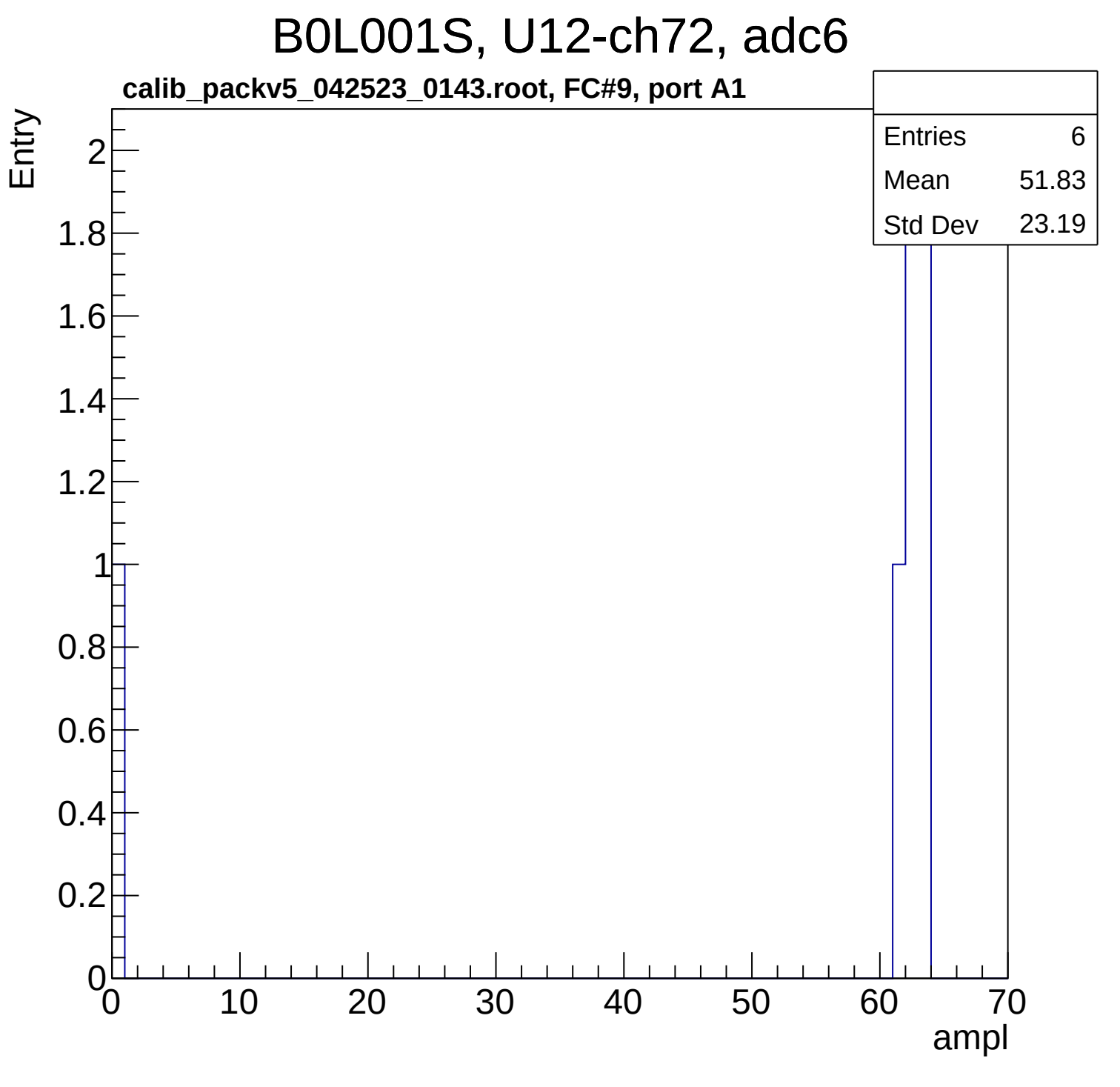
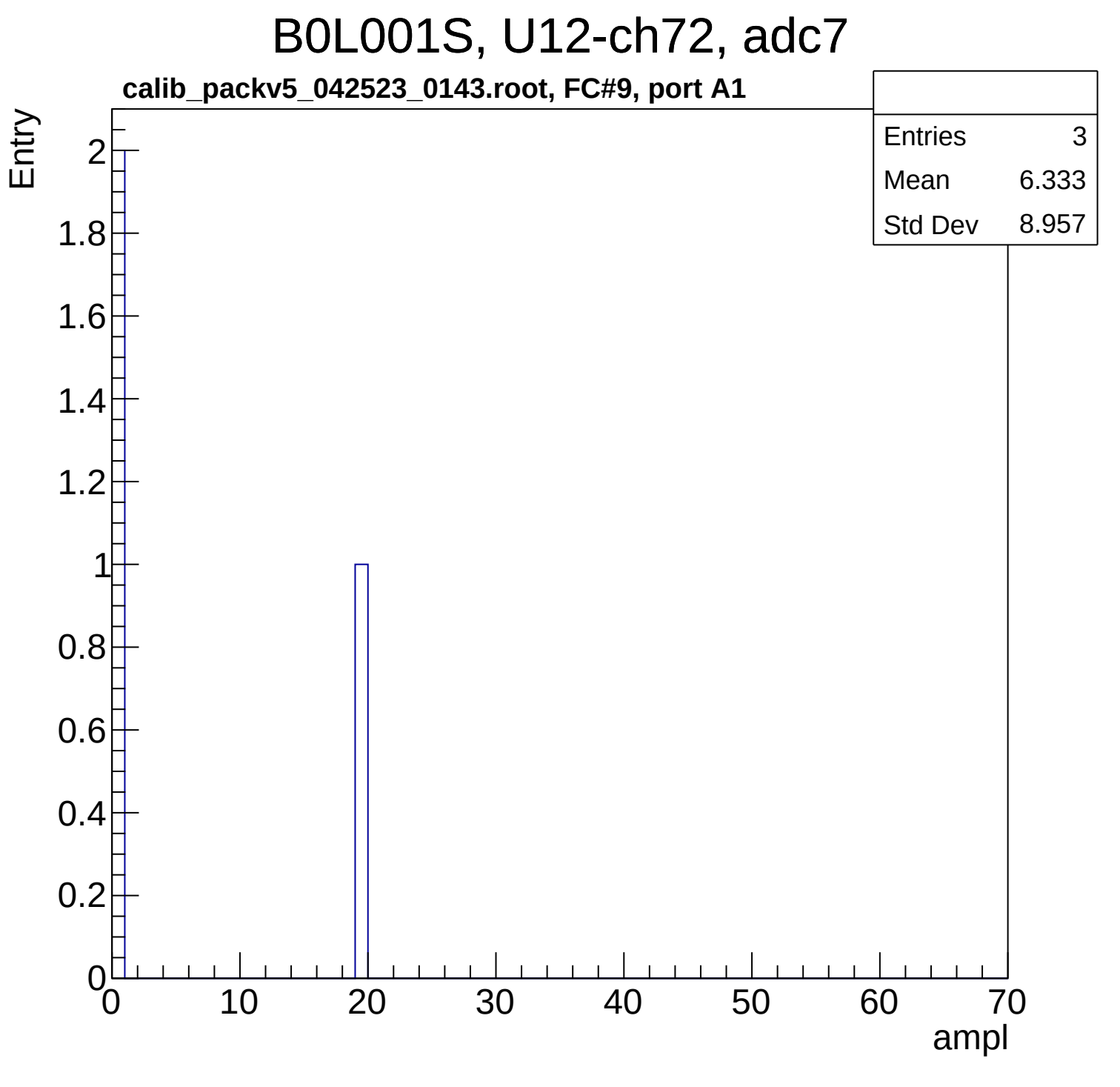
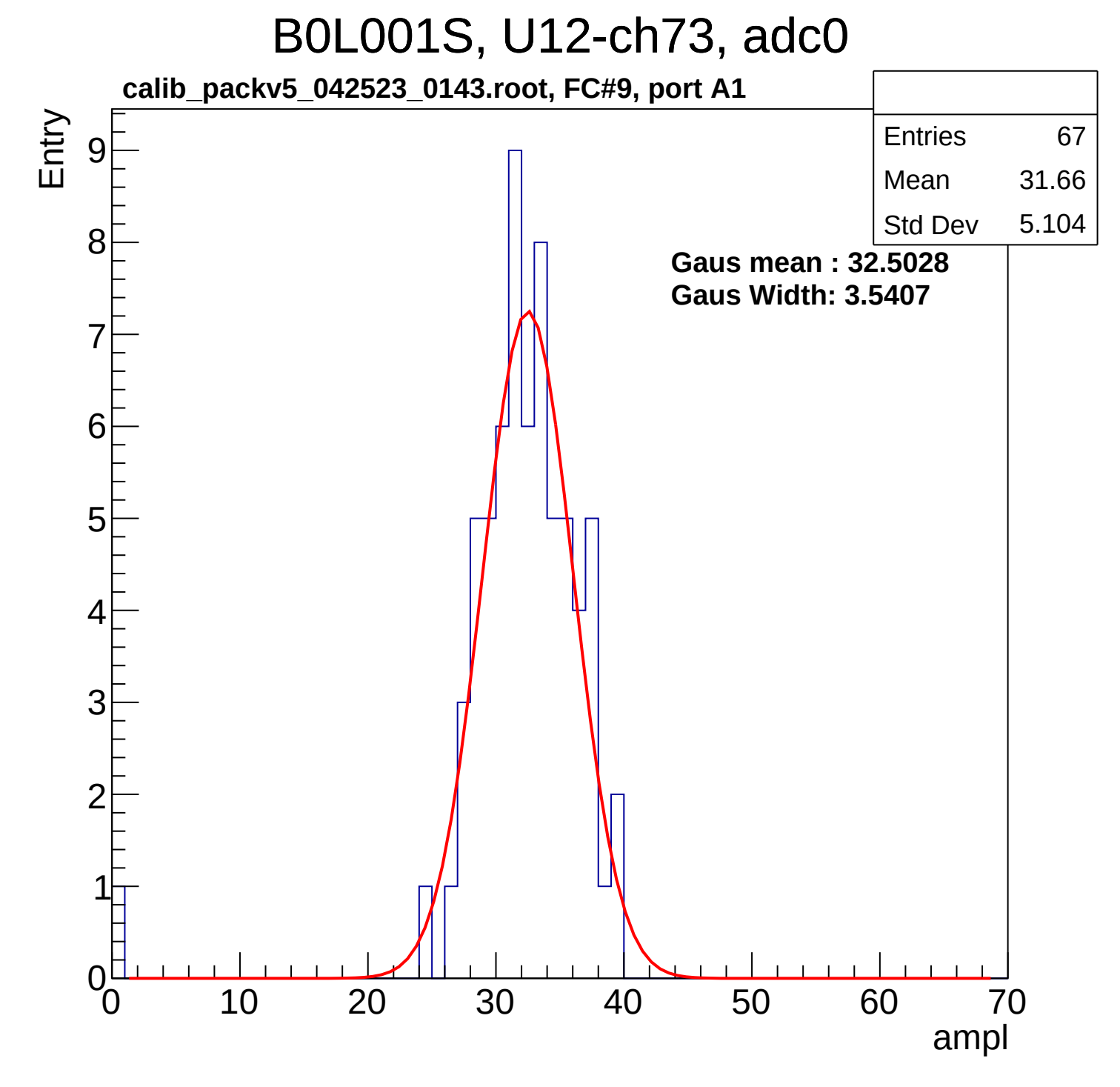

B0L001S, U12-ch72, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 6
Mean 51.83
Std Dev 23.19
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L001S, U12-ch72, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 3
Mean 6.333
Std Dev 8.957
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L001S, U12-ch73, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 67
Mean 31.66
Std Dev 5.104
Gaus mean : 32.5028
Gaus Width: 3.5407
Entry
ampl
0
1
2
3
4
5
6
7
8
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0
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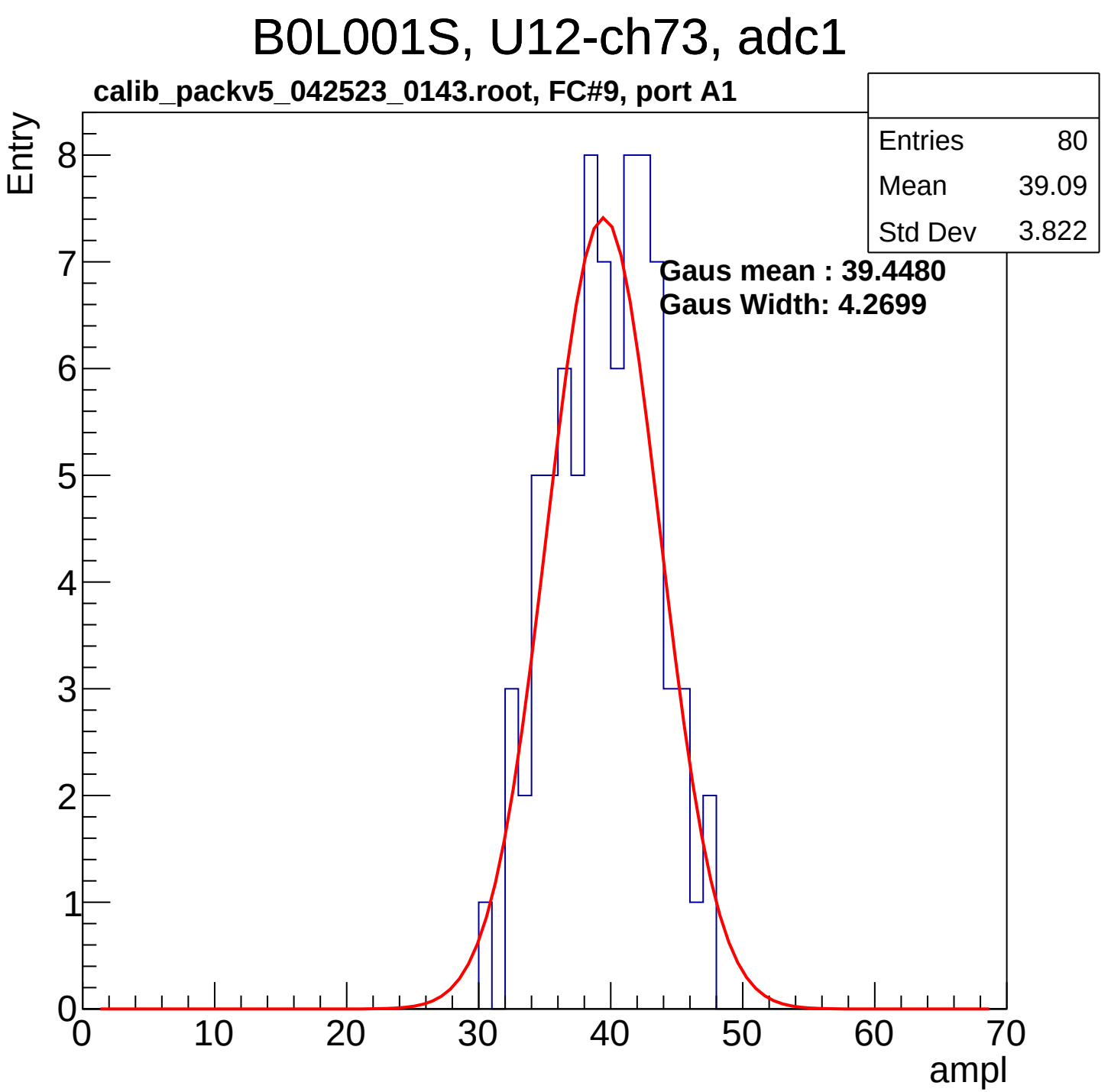
B0L001S, U12-ch73, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 80
Mean 39.09
Std Dev 3.822
Gaus mean : 39.4480
Gaus Width: 4.2699
Entry
ampl
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1
2
3
4
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0
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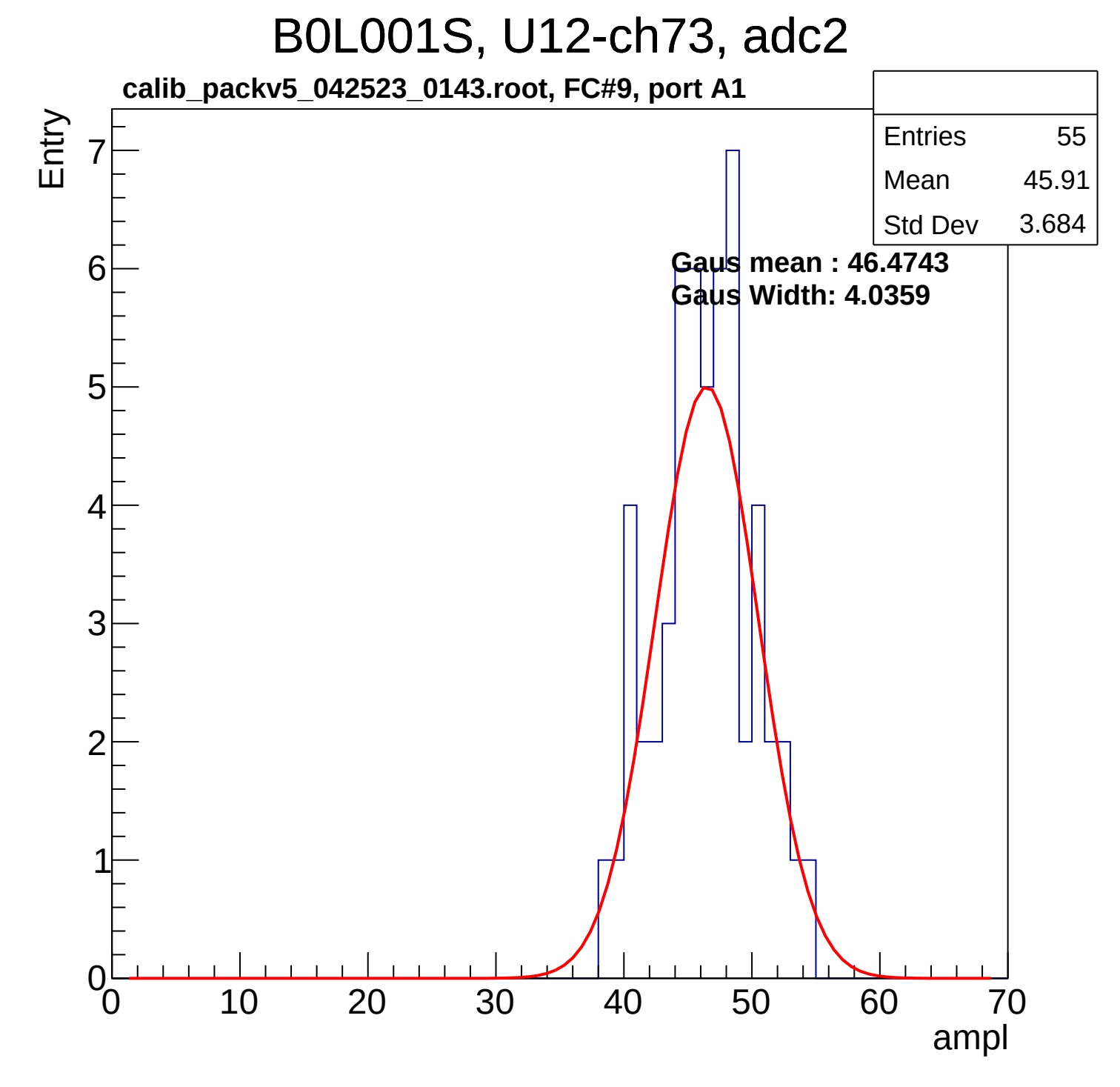
B0L001S, U12-ch73, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 55
Mean 45.91
Std Dev 3.684
Gaus mean : 46.4743
Gaus Width: 4.0359
Entry
ampl
0
1
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4
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0
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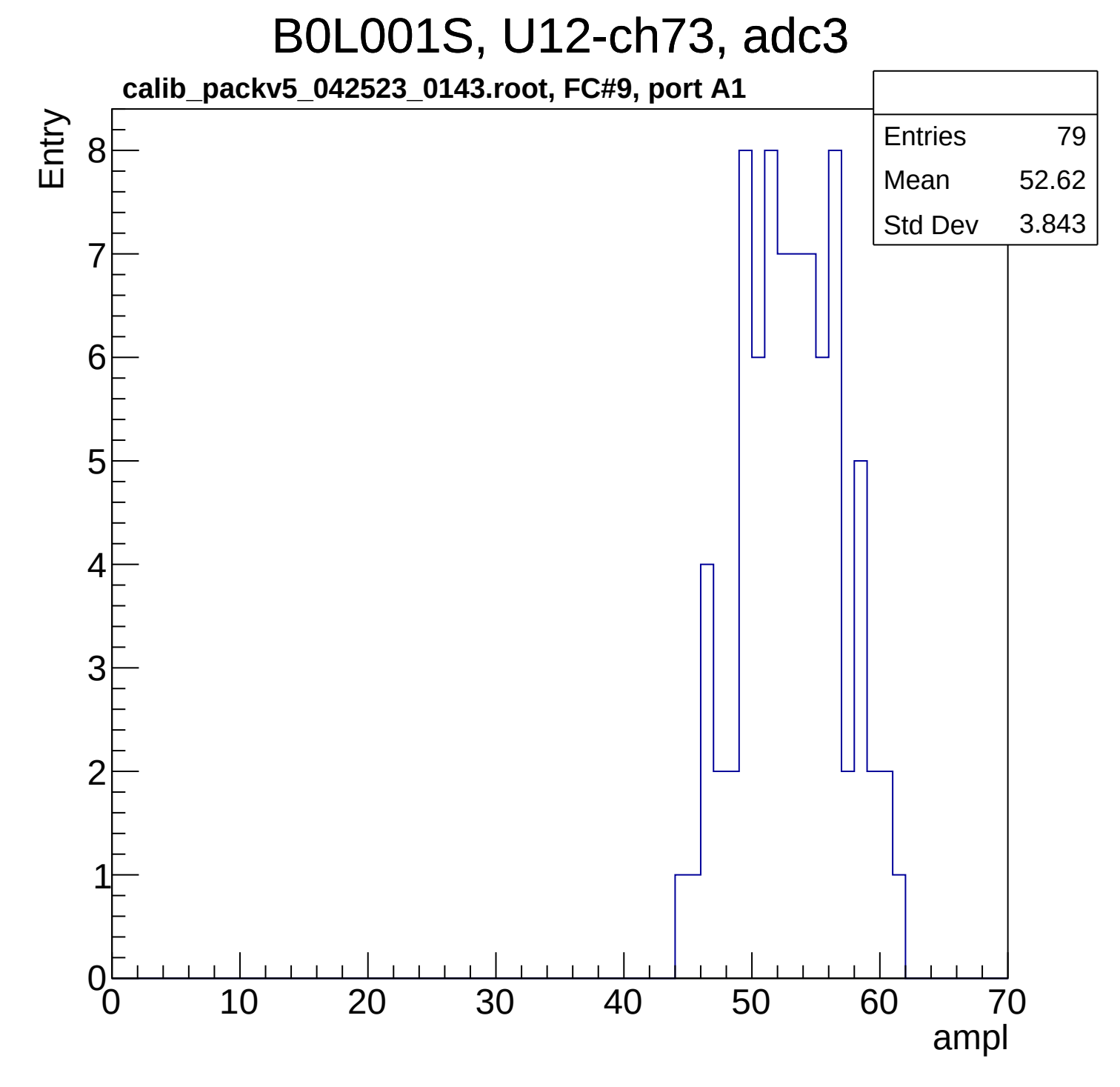
B0L001S, U12-ch73, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 79
Mean 52.62
Std Dev 3.843
Entry
ampl
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1
2
3
4
5
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7
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0
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60
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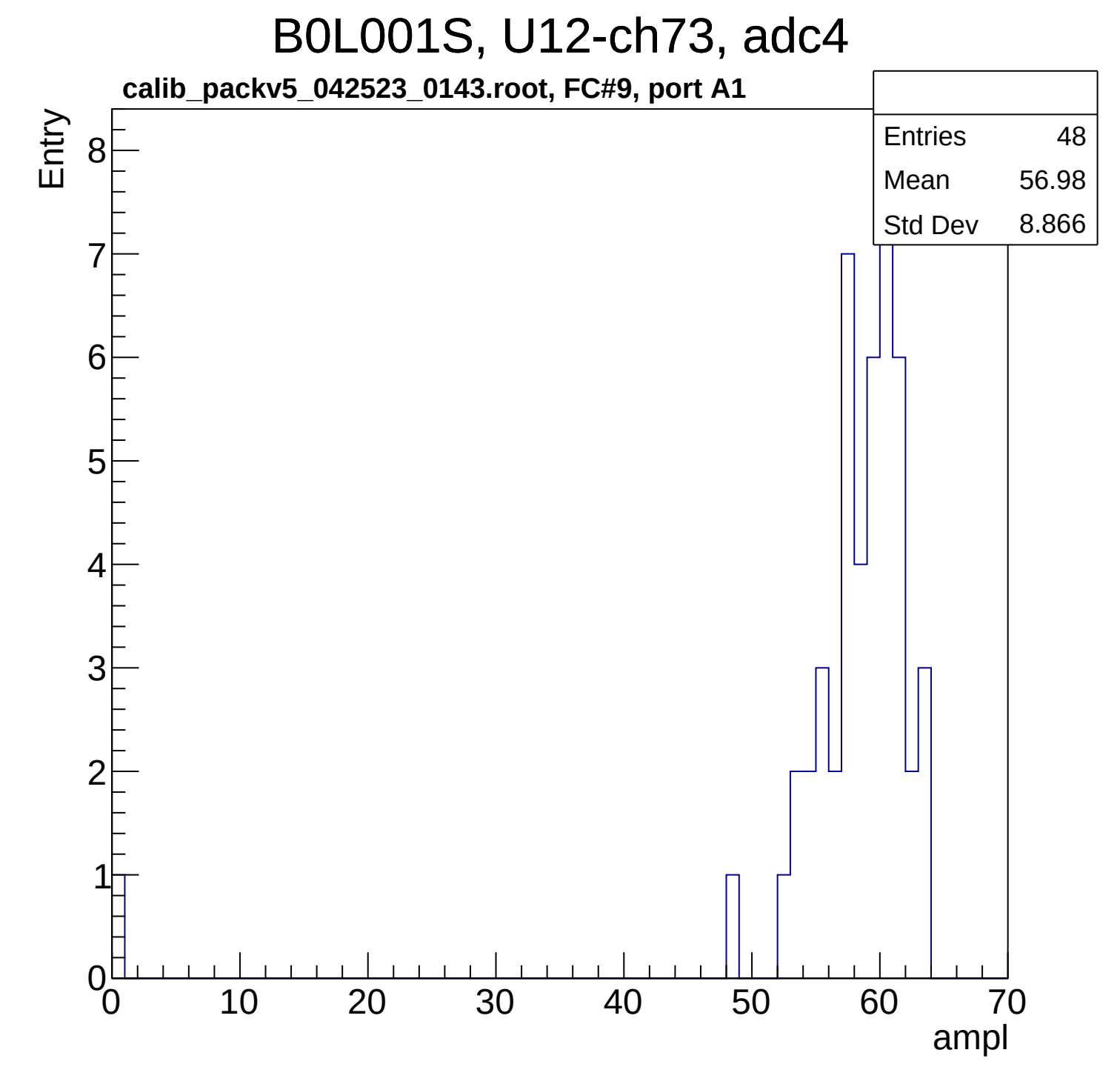
B0L001S, U12-ch73, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 48
Mean 56.98
Std Dev 8.866
Entry
ampl
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1
2
3
4
5
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7
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0
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60
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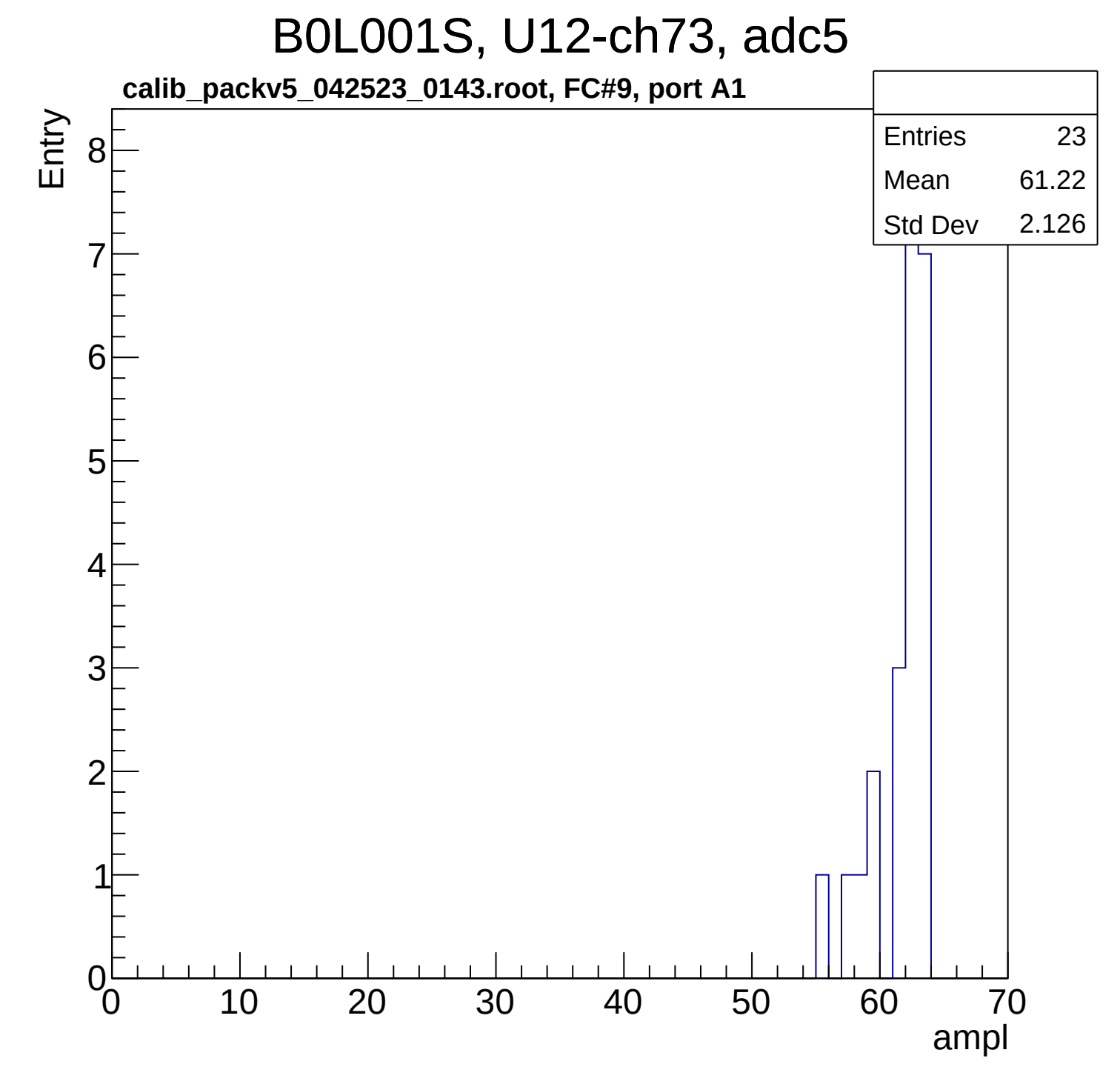
B0L001S, U12-ch73, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 23
Mean 61.22
Std Dev 2.126
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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40
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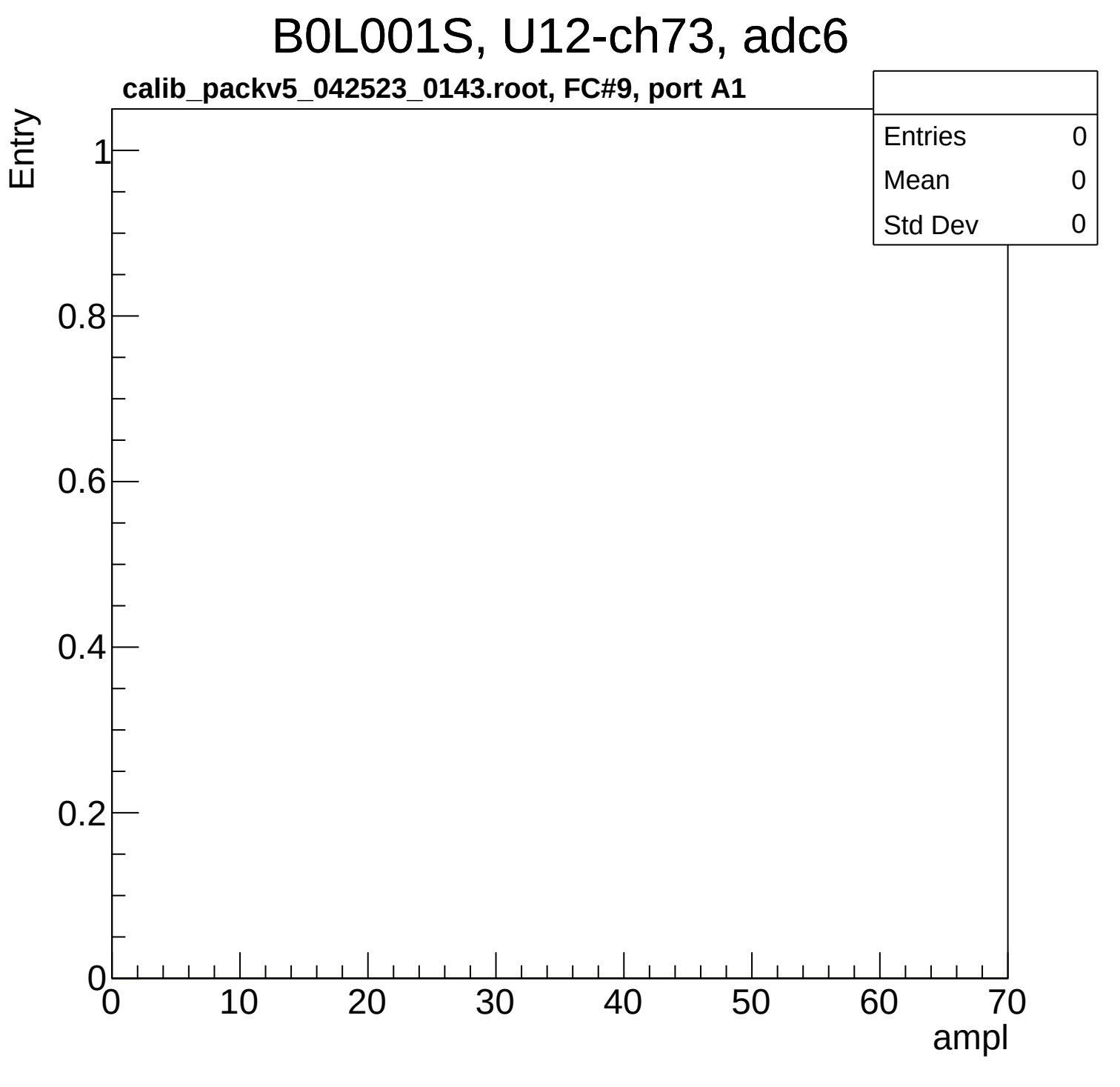
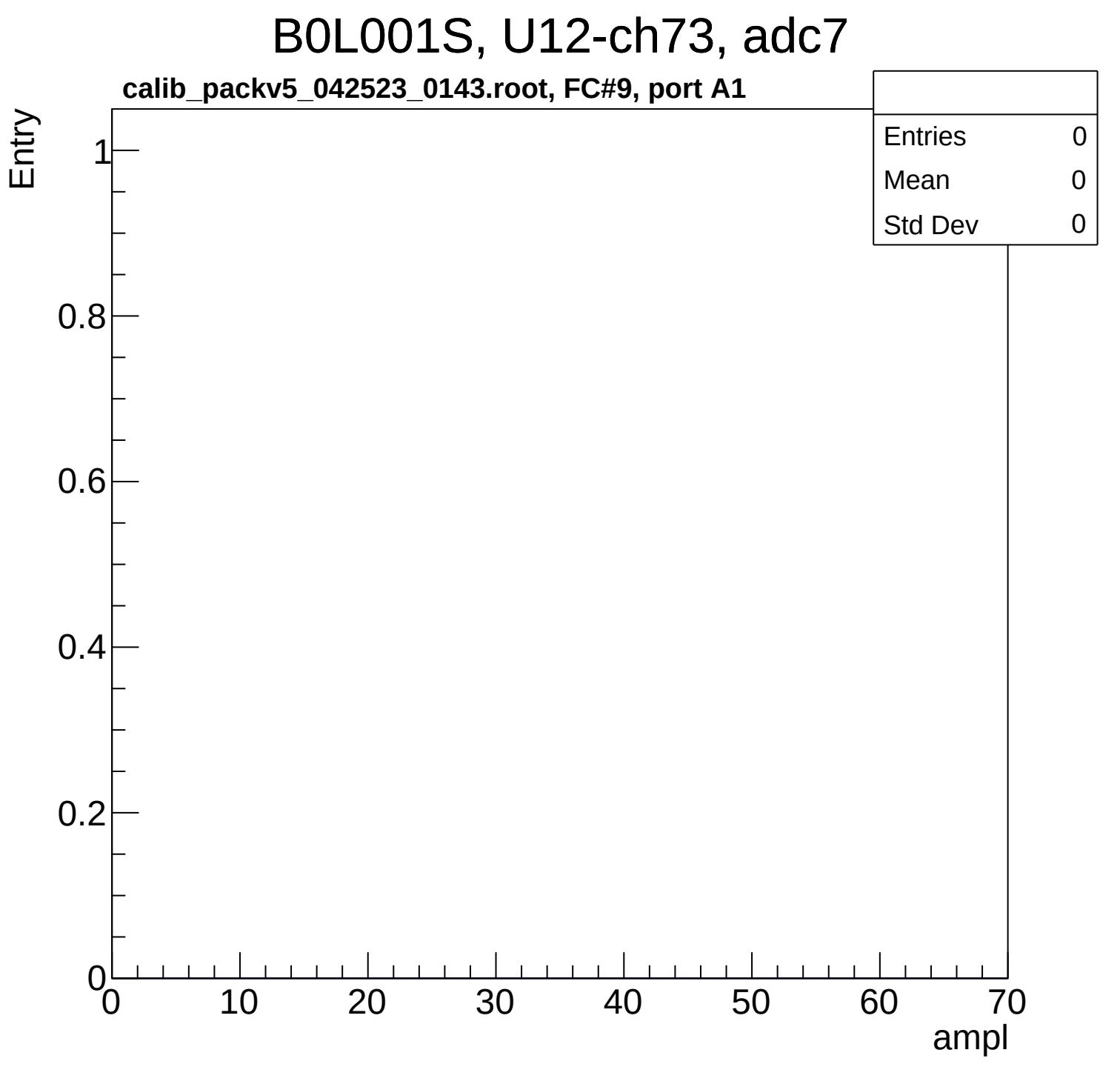
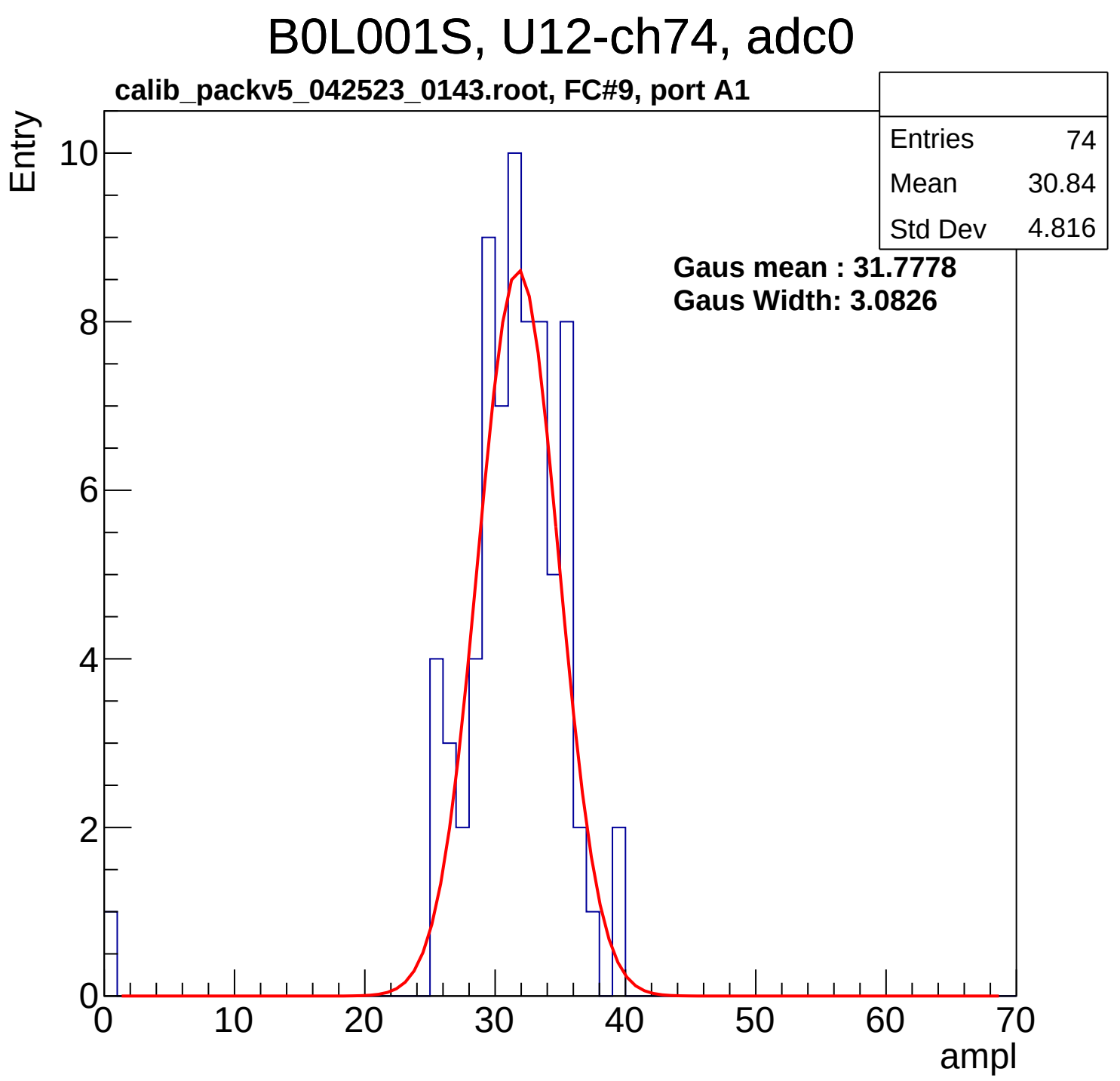
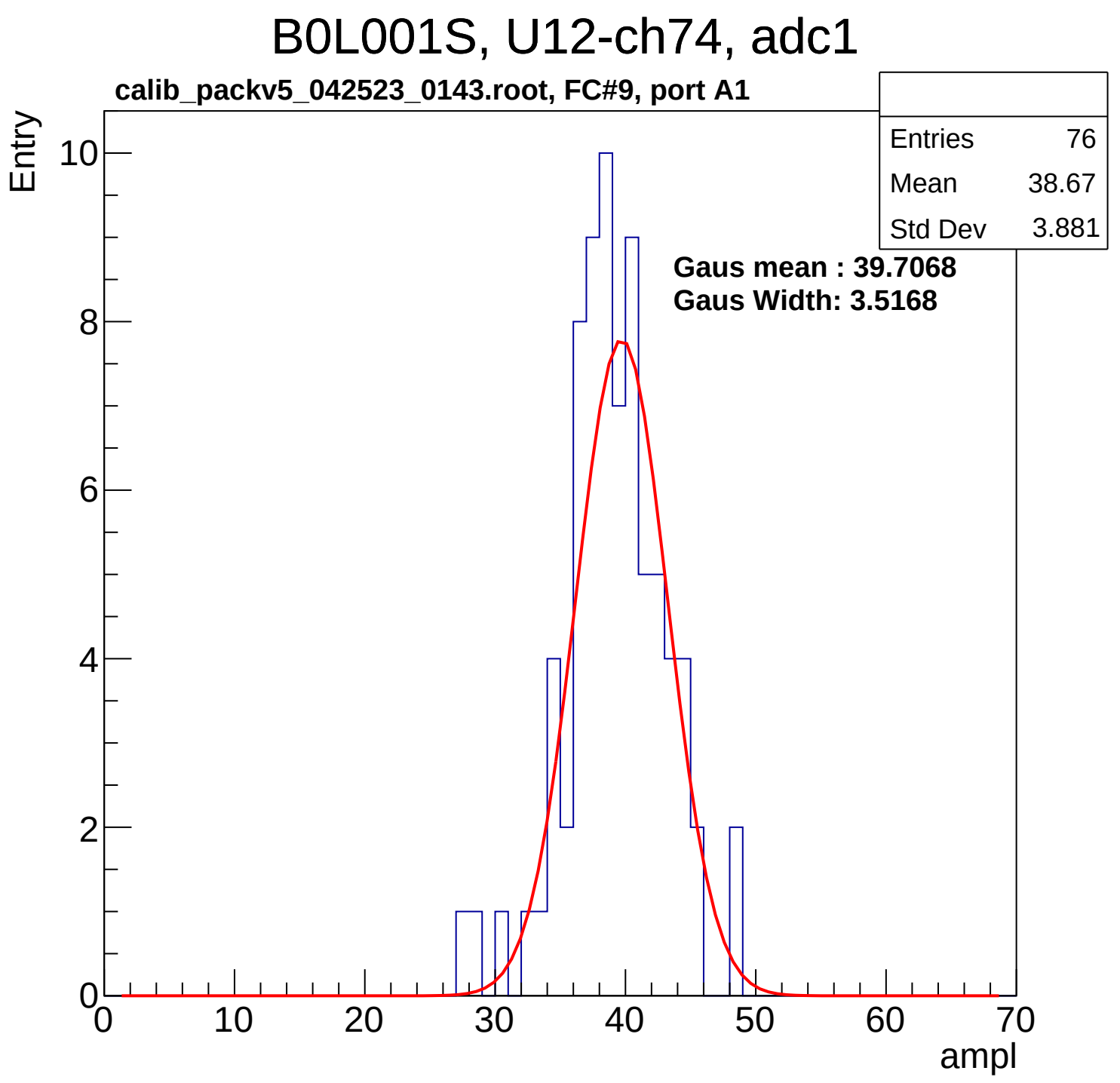
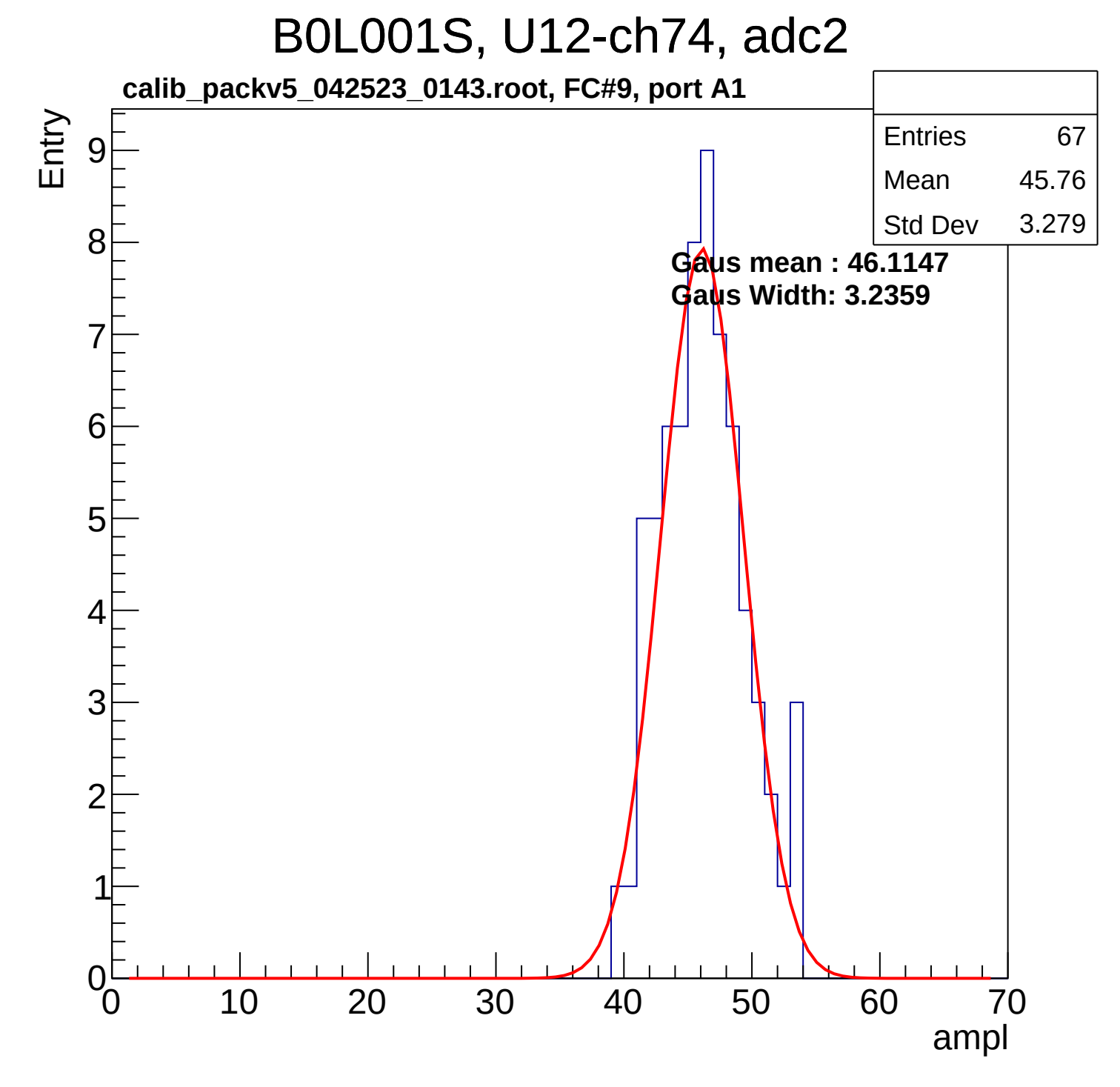

B0L001S, U12-ch73, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch73, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch74, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 74
Mean 30.84
Std Dev 4.816
Gaus mean : 31.7778
Gaus Width: 3.0826
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch74, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 76
Mean 38.67
Std Dev 3.881
Gaus mean : 39.7068
Gaus Width: 3.5168
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch74, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 67
Mean 45.76
Std Dev 3.279
Gaus mean : 46.1147
Gaus Width: 3.2359
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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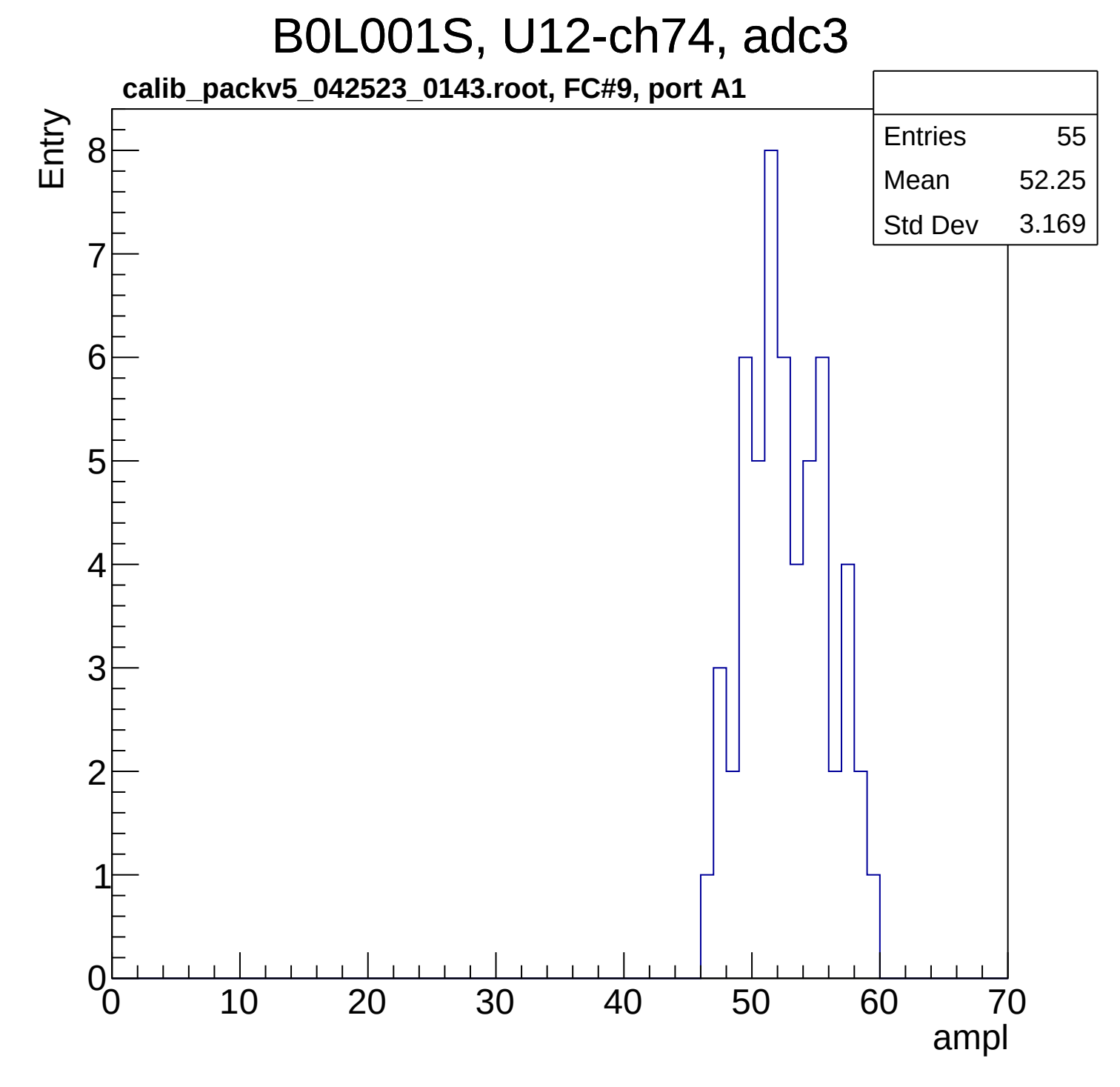
B0L001S, U12-ch74, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 55
Mean 52.25
Std Dev 3.169
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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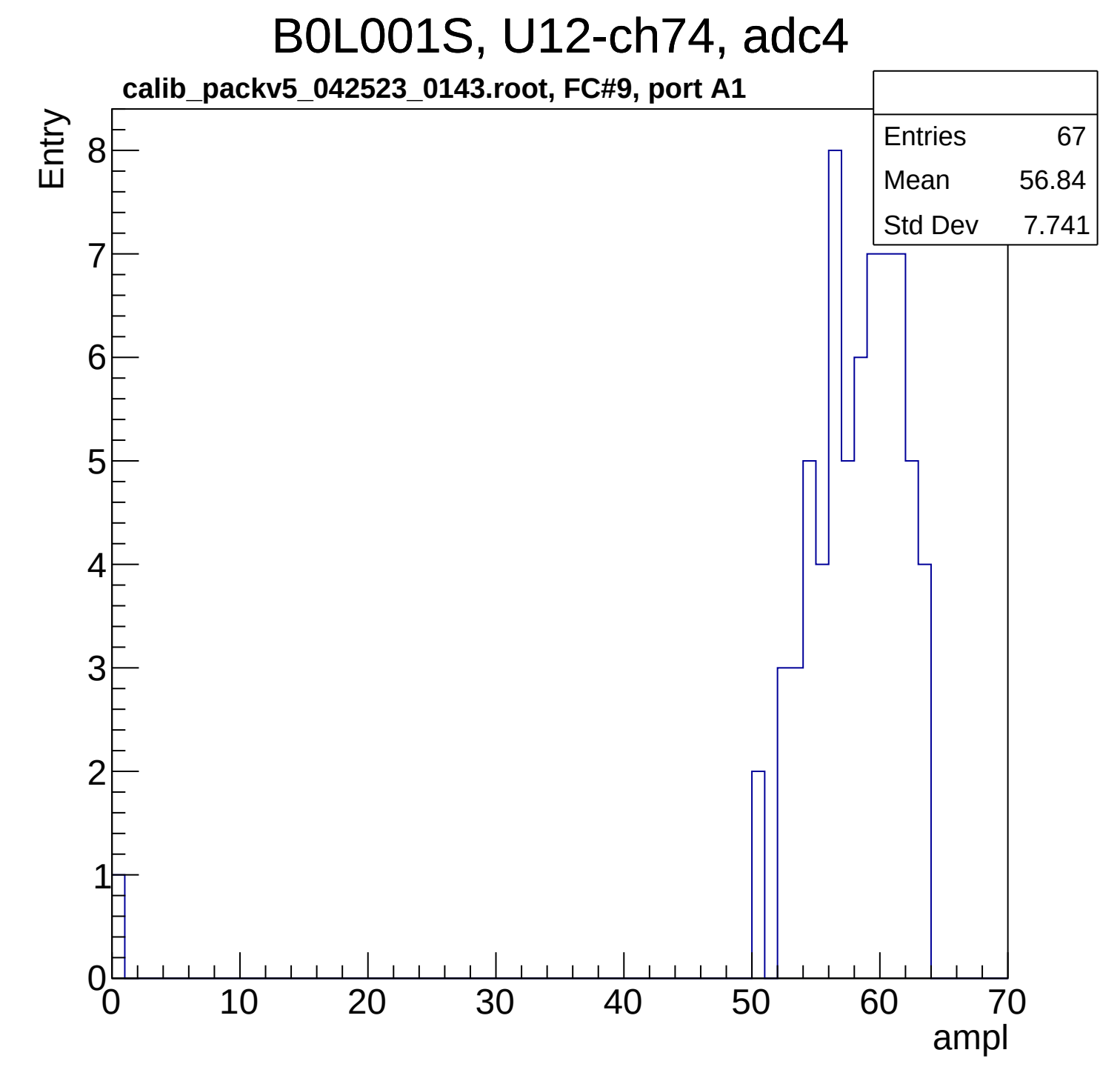
B0L001S, U12-ch74, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 67
Mean 56.84
Std Dev 7.741
Entry
ampl
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1
2
3
4
5
6
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0
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40
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60
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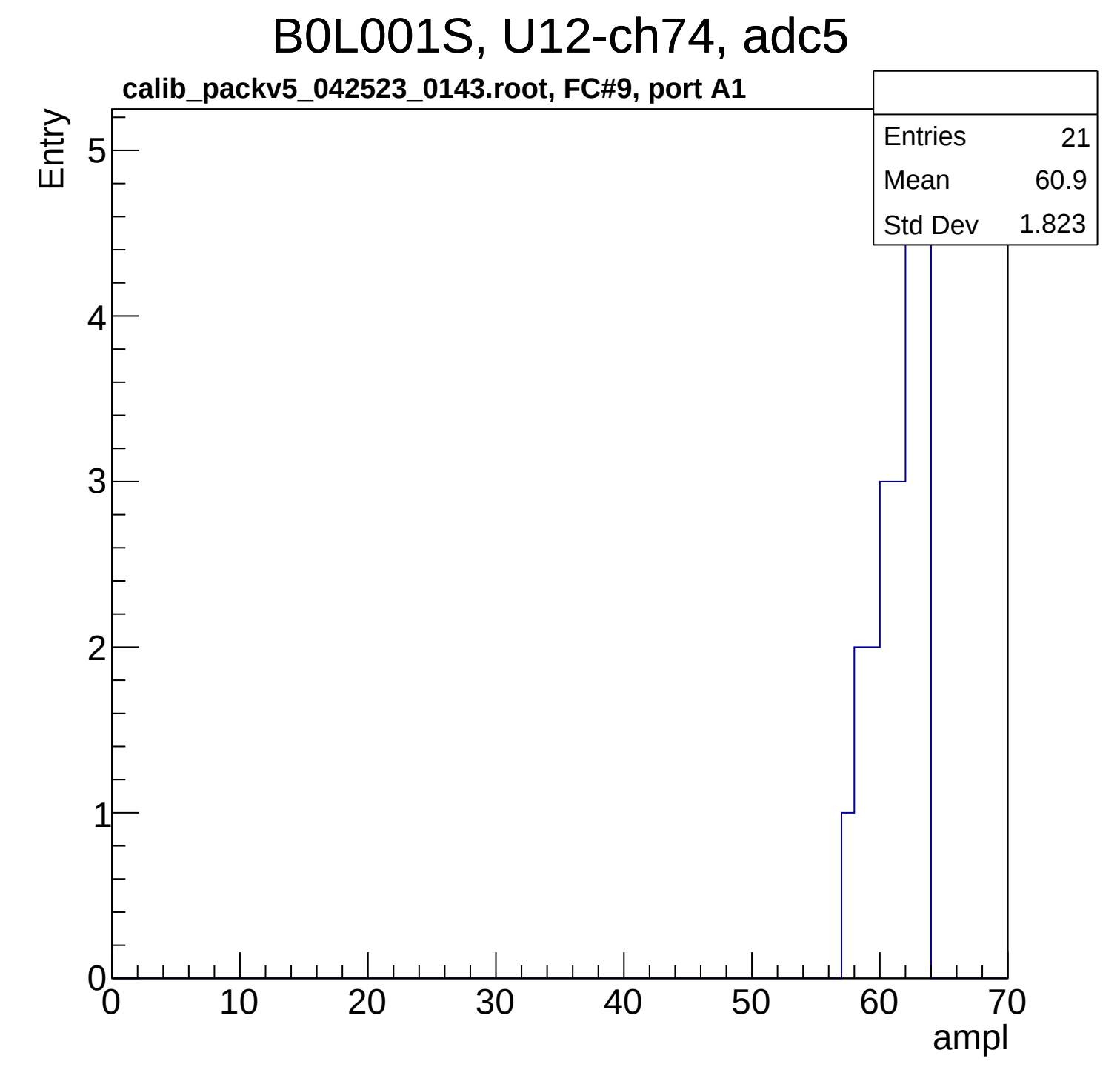
B0L001S, U12-ch74, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 21
Mean 60.9
Std Dev 1.823
Entry
ampl
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1
2
3
4
5
0
10
20
30
40
50
60
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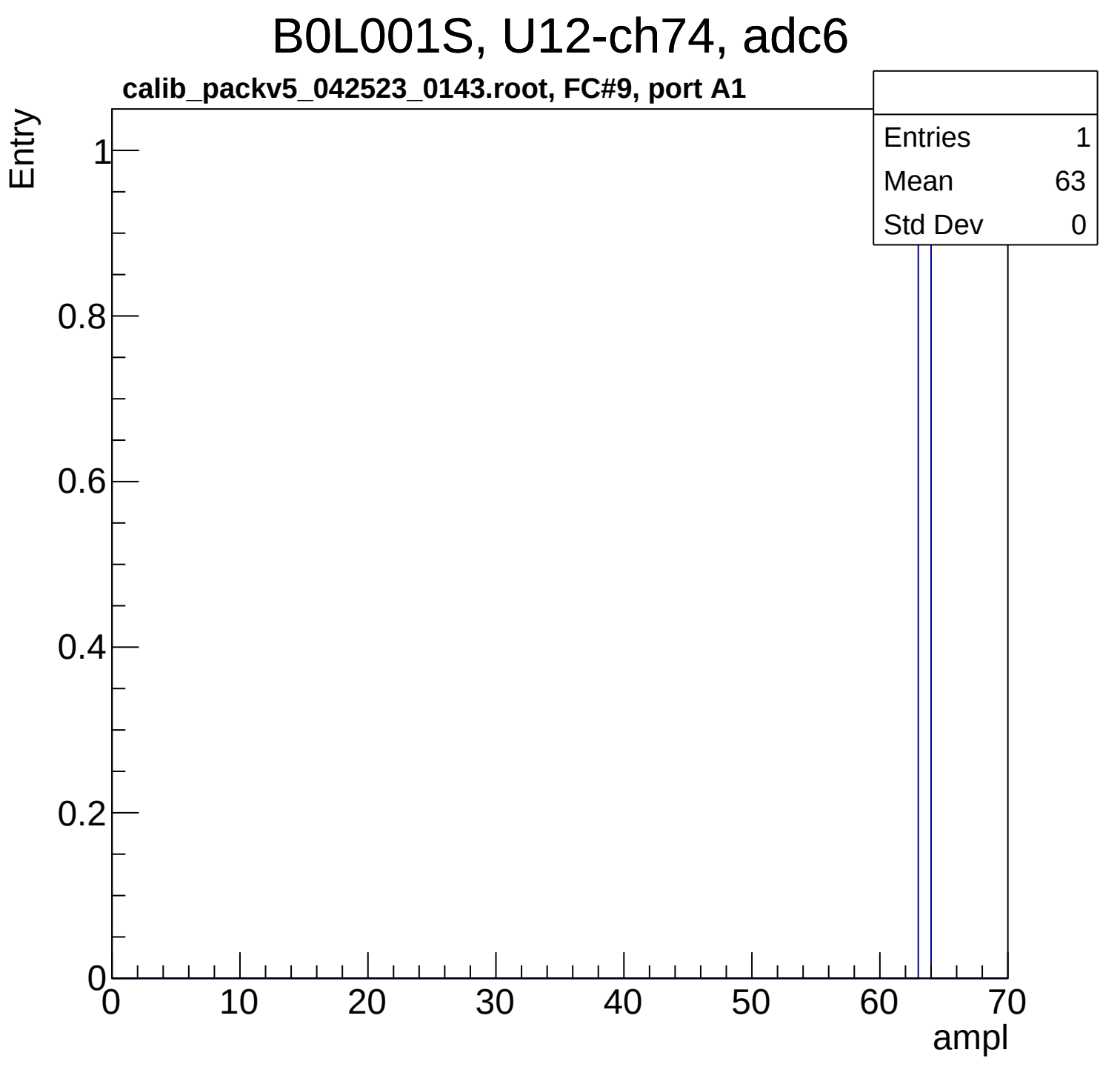
B0L001S, U12-ch74, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 63
Std Dev 0
Entry
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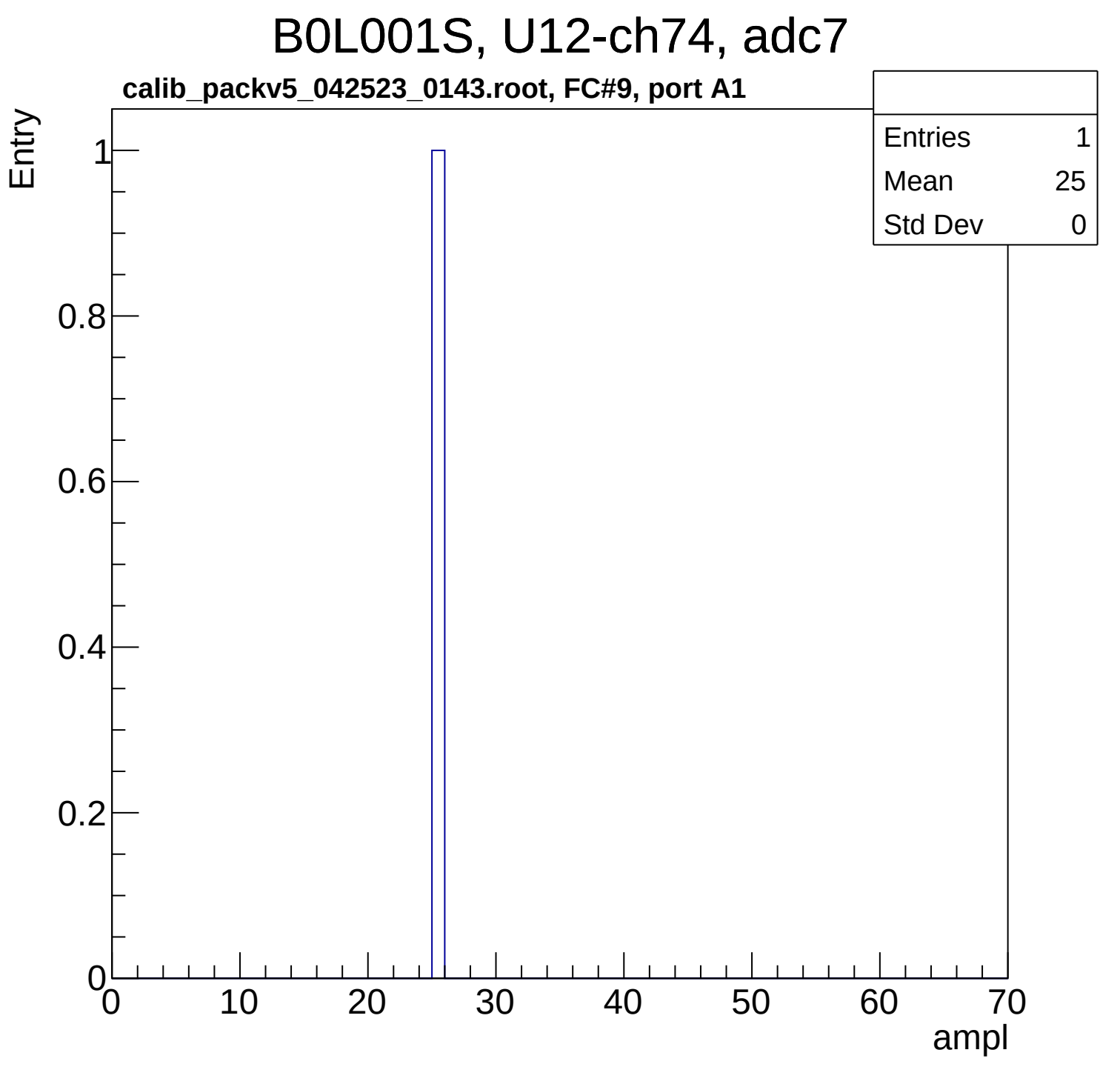
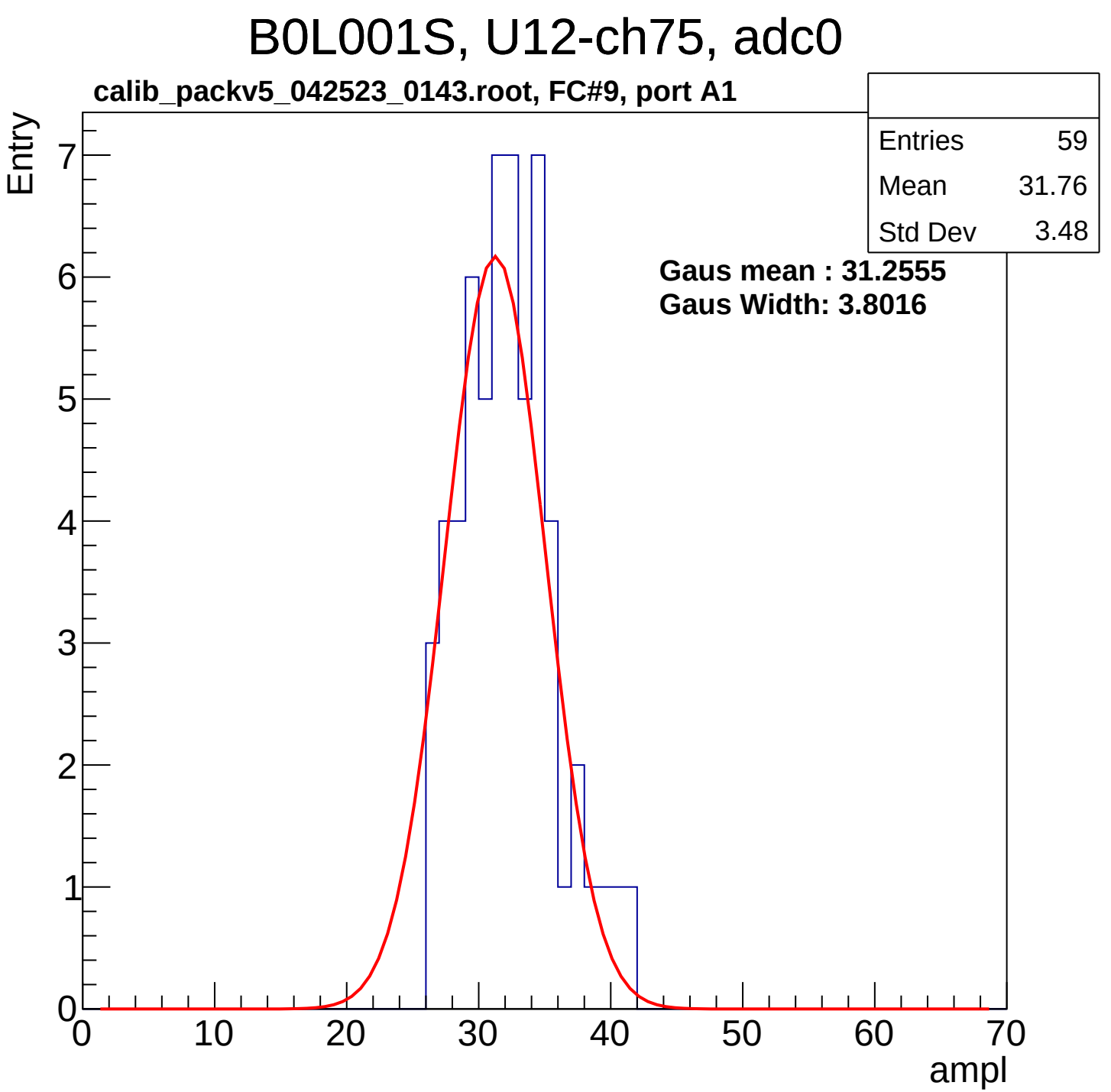
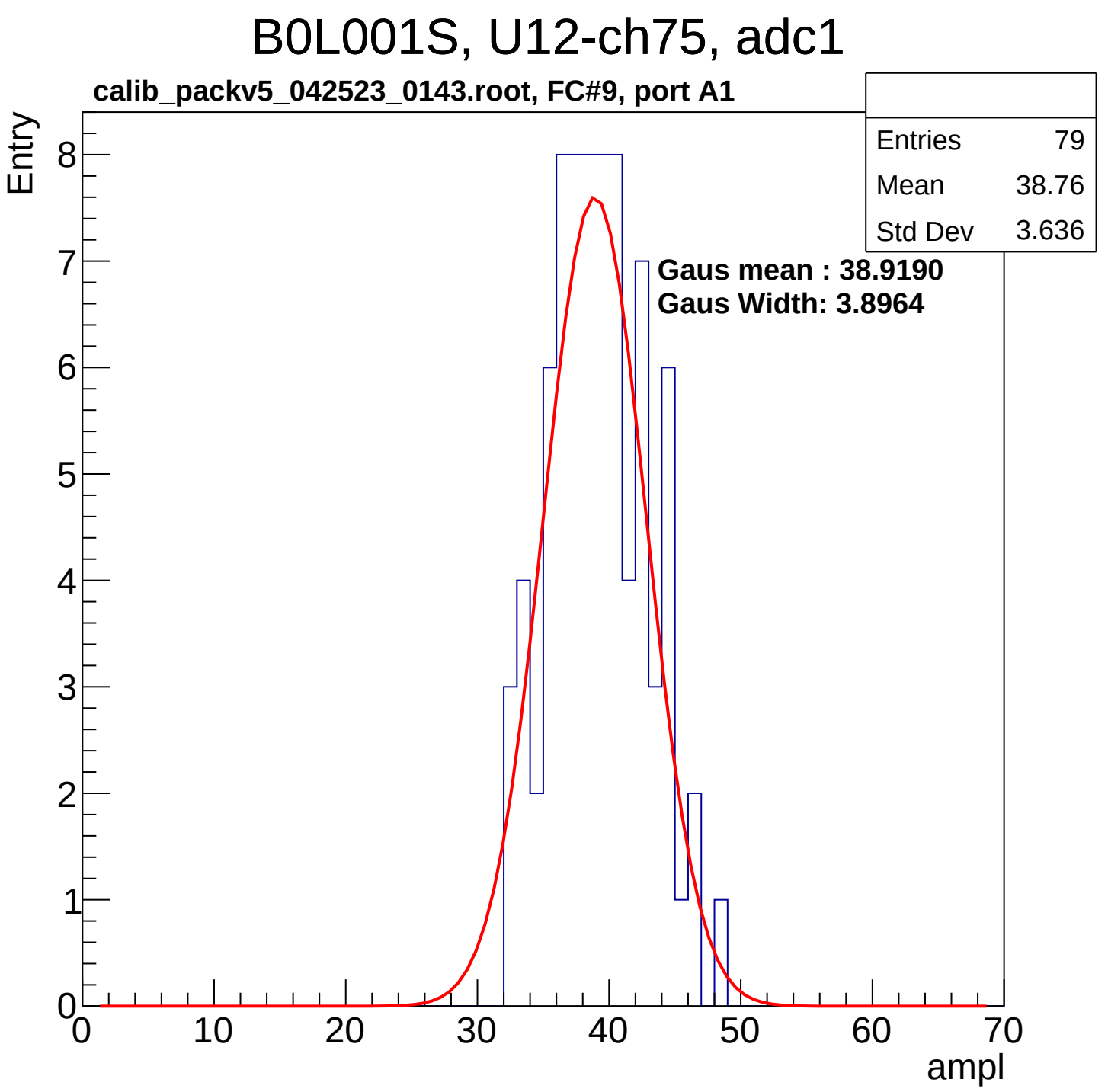
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch74, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 25
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch75, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 59
Mean 31.76
Std Dev 3.48
Gaus mean : 31.2555
Gaus Width: 3.8016
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B0L001S, U12-ch75, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 79
Mean 38.76
Std Dev 3.636
Gaus mean : 38.9190
Gaus Width: 3.8964
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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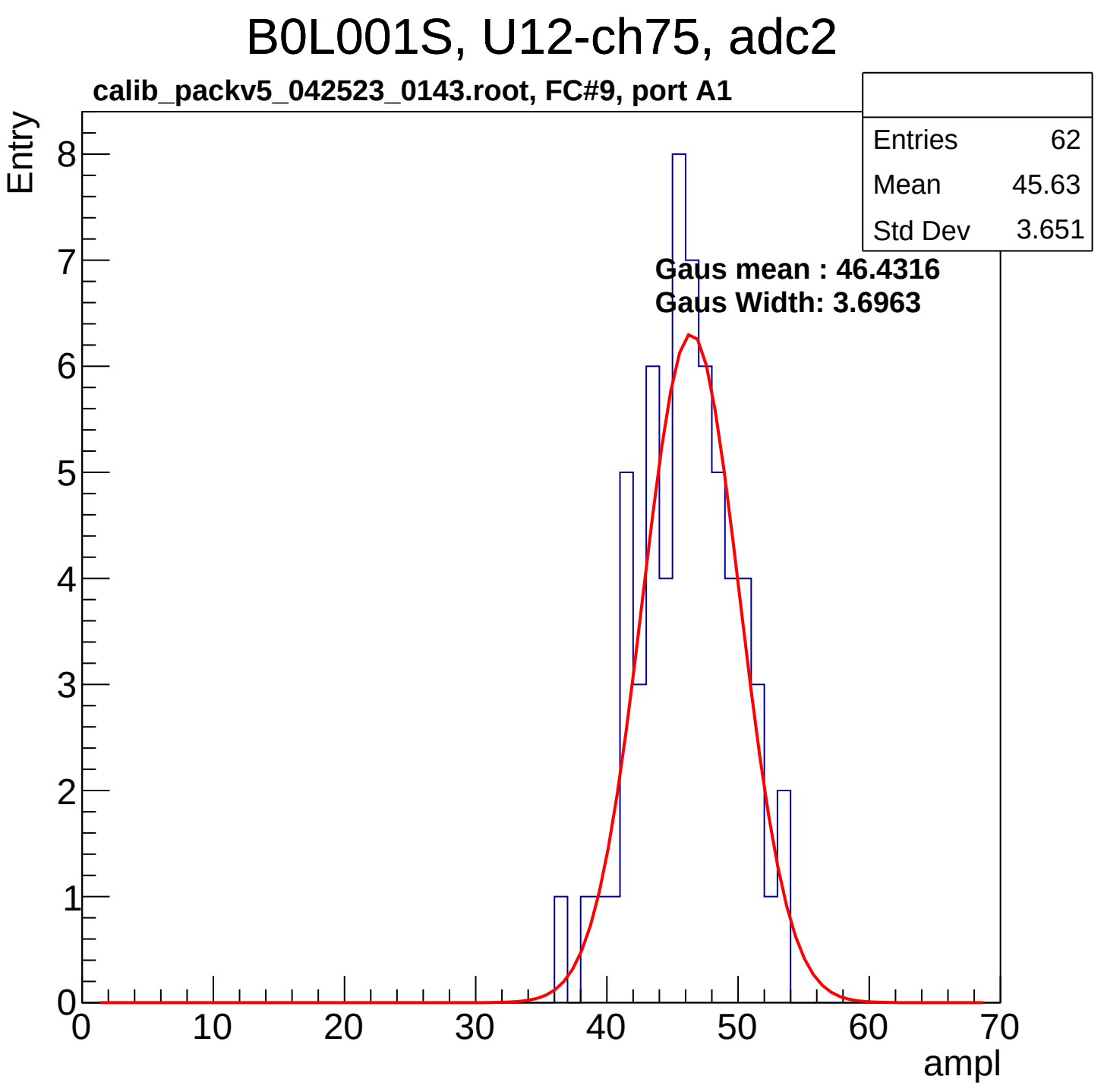
B0L001S, U12-ch75, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 62
Mean 45.63
Std Dev 3.651
Gaus mean : 46.4316
Gaus Width: 3.6963
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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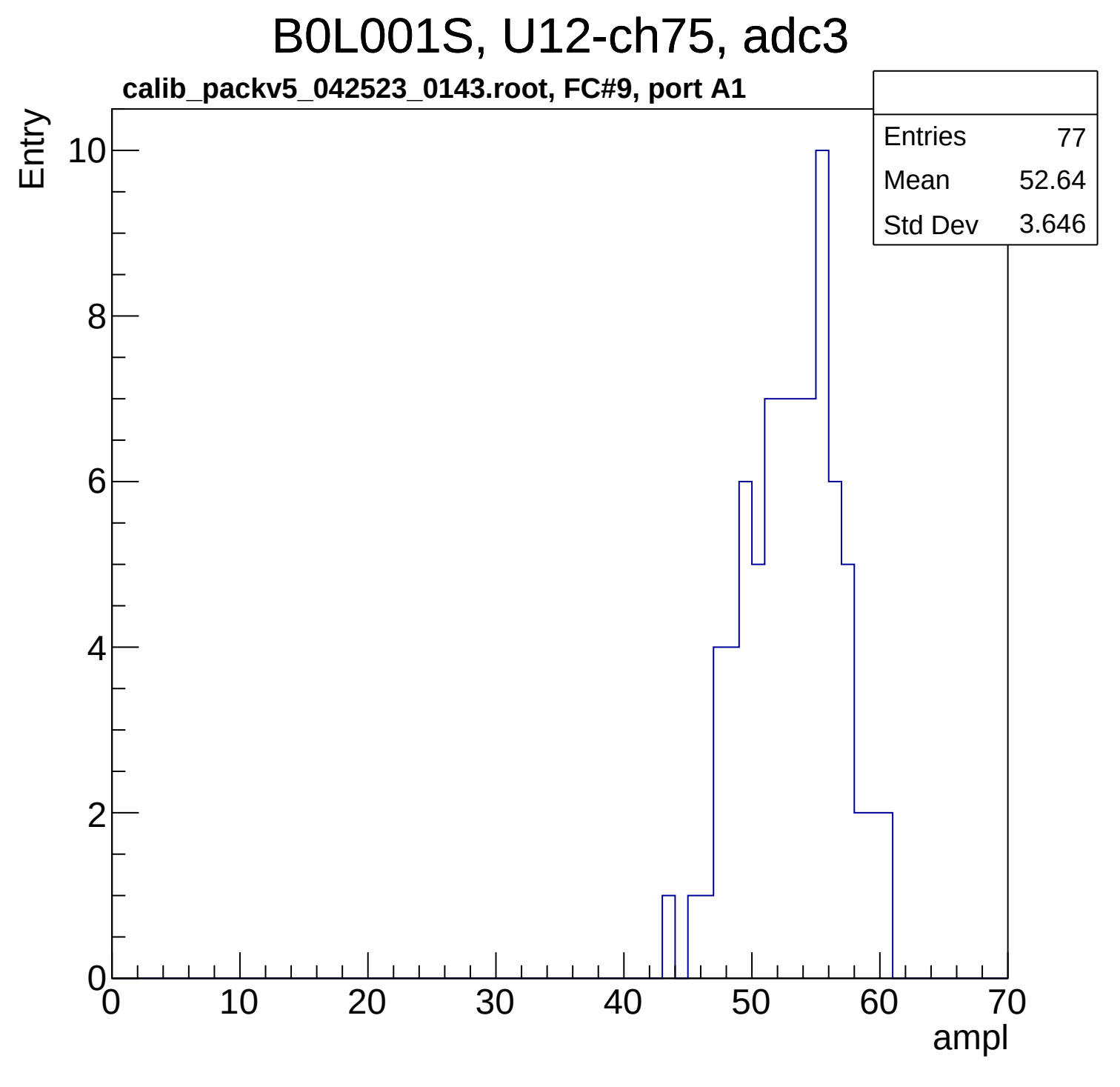
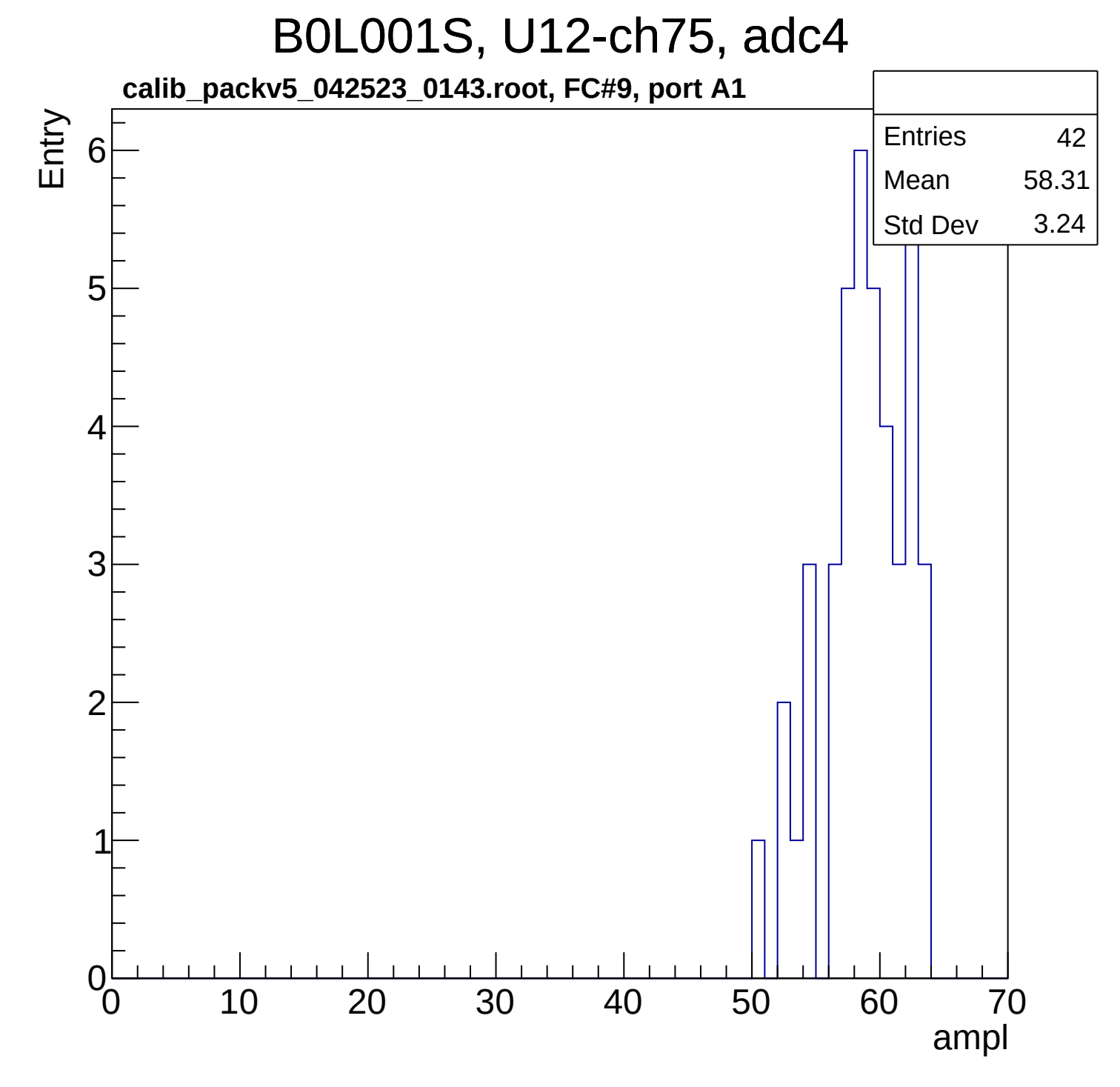

B0L001S, U12-ch75, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 77
Mean 52.64
Std Dev 3.646
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch75, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 42
Mean 58.31
Std Dev 3.24
Entry
ampl
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60
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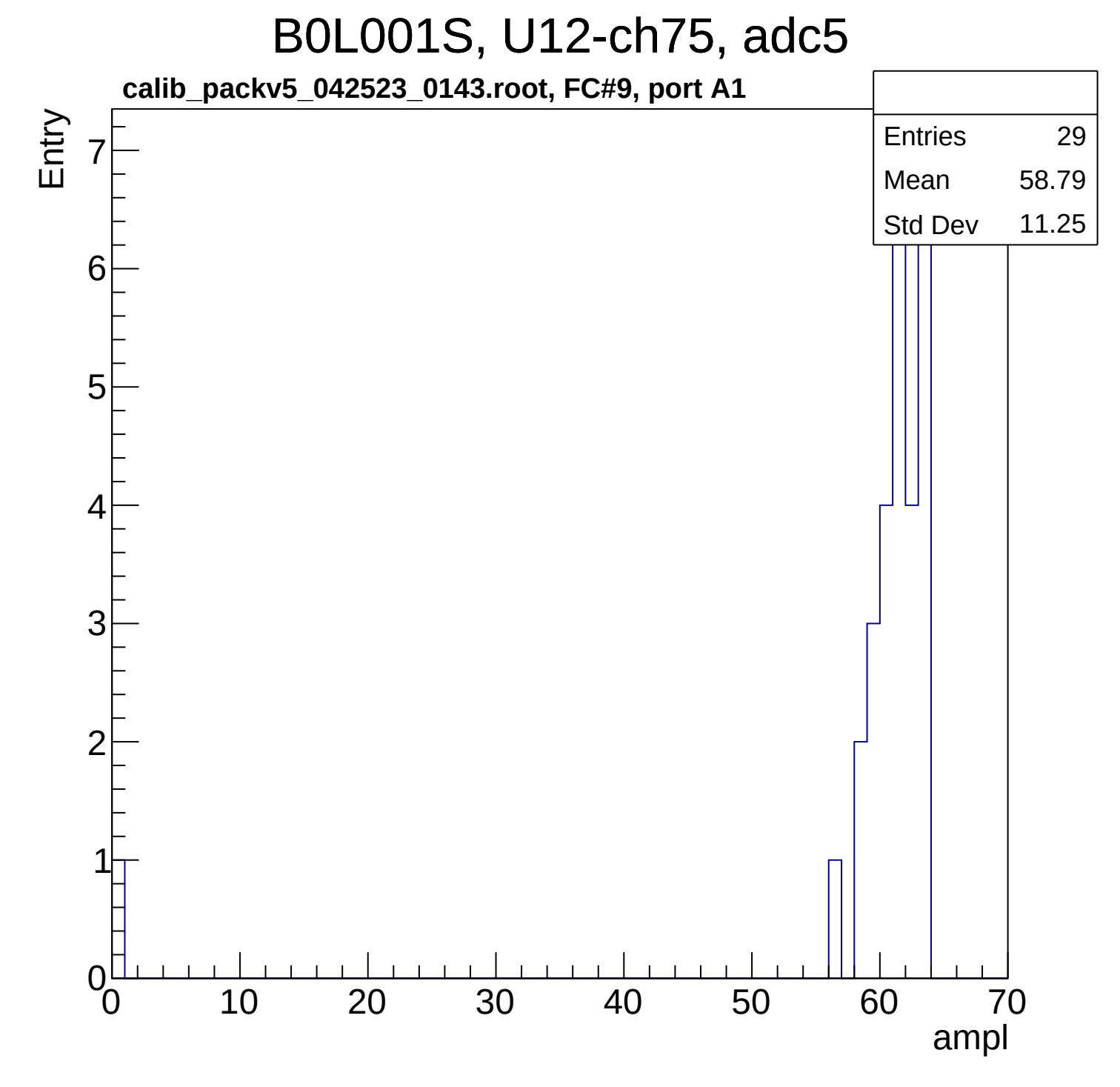
B0L001S, U12-ch75, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 29
Mean 58.79
Std Dev 11.25
Entry
ampl
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1
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3
4
5
6
7
0
10
20
30
40
50
60
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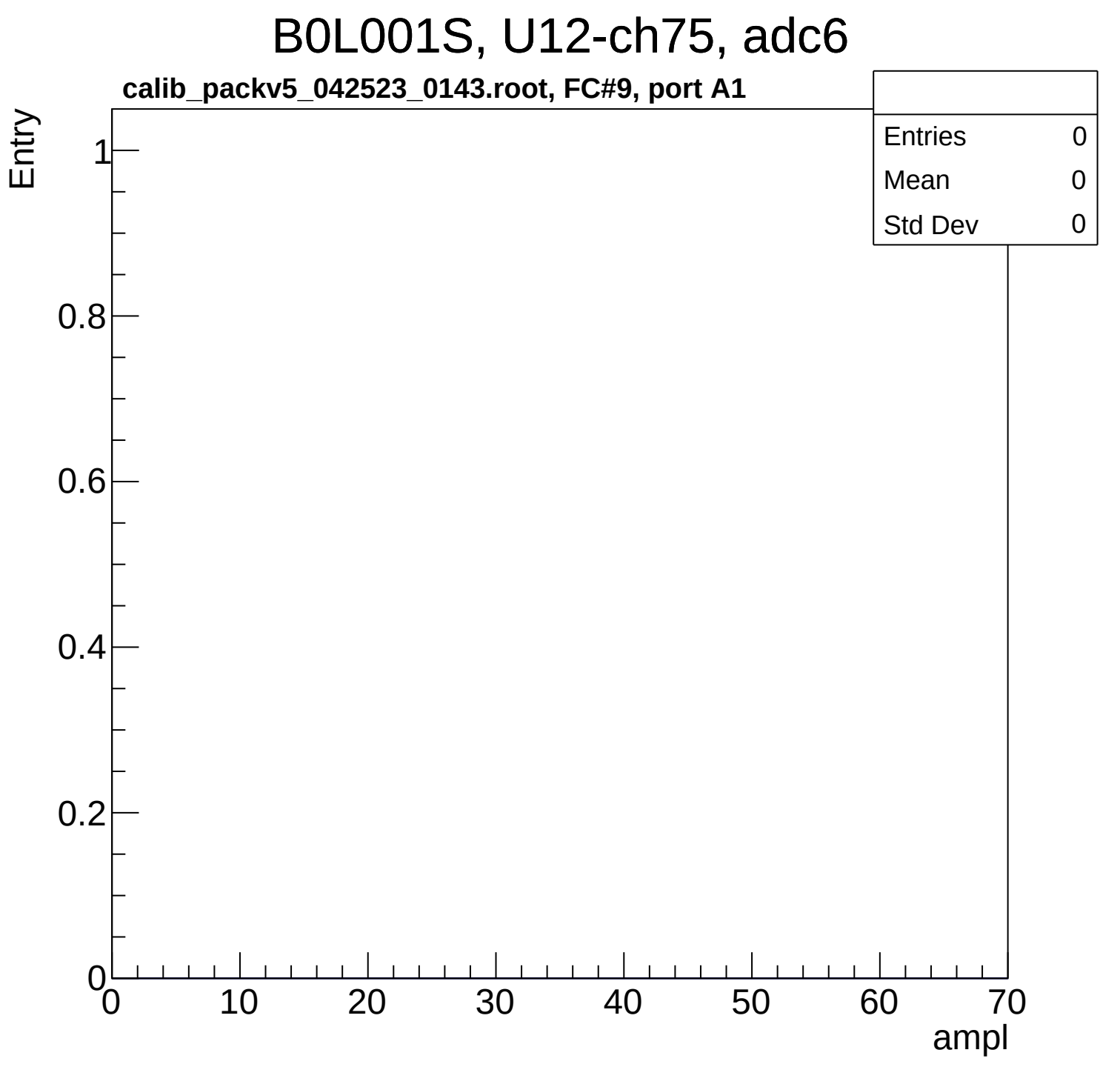
B0L001S, U12-ch75, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
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0.6
0.4
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0
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10
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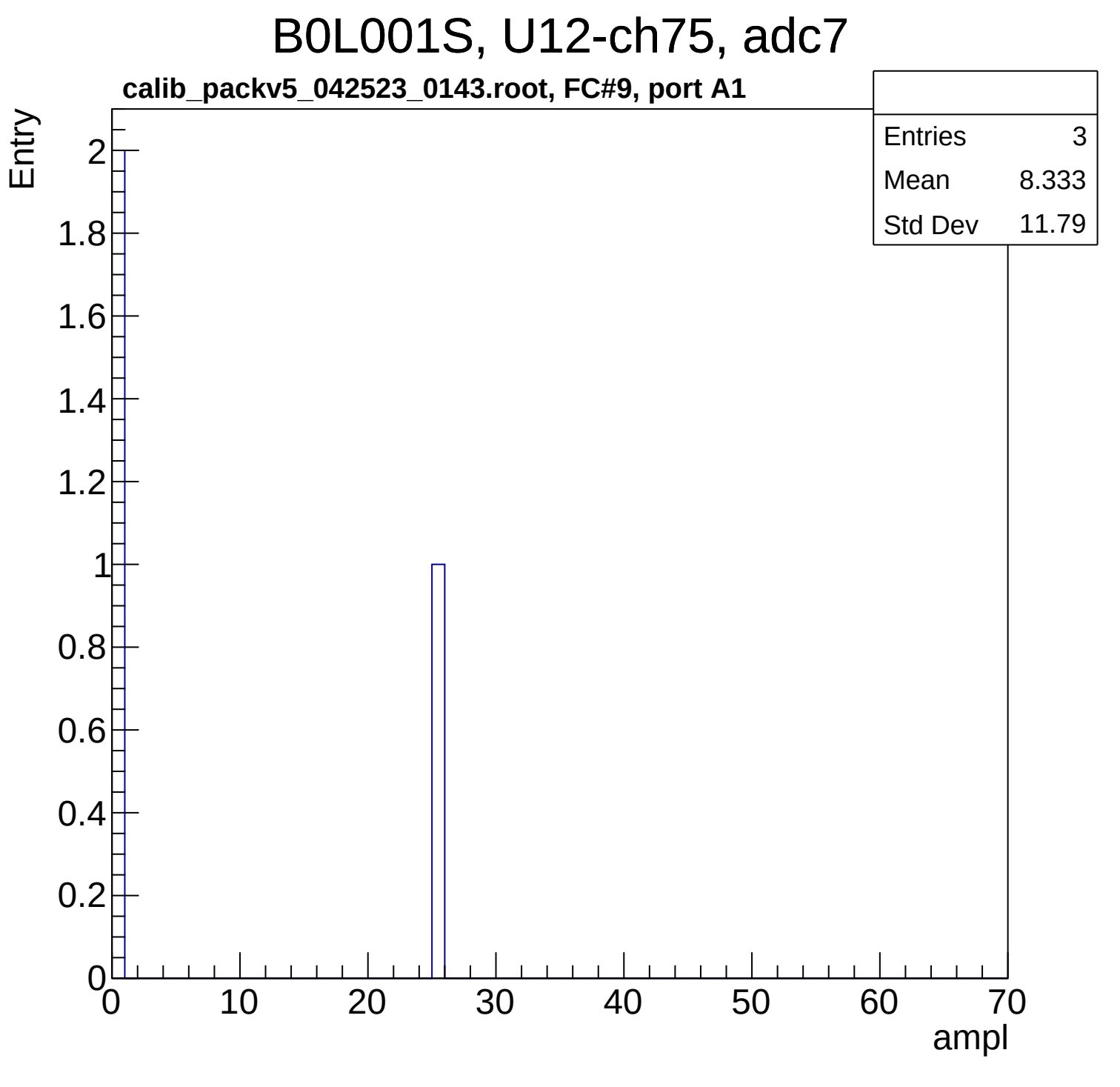
50
60
70
ampl


B0L001S, U12-ch75, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 3
Mean 8.333
Std Dev 11.79
Entry
ampl
0
0.2
0.4
0.6
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1
1.2
1.4
1.6
1.8
2
0
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60
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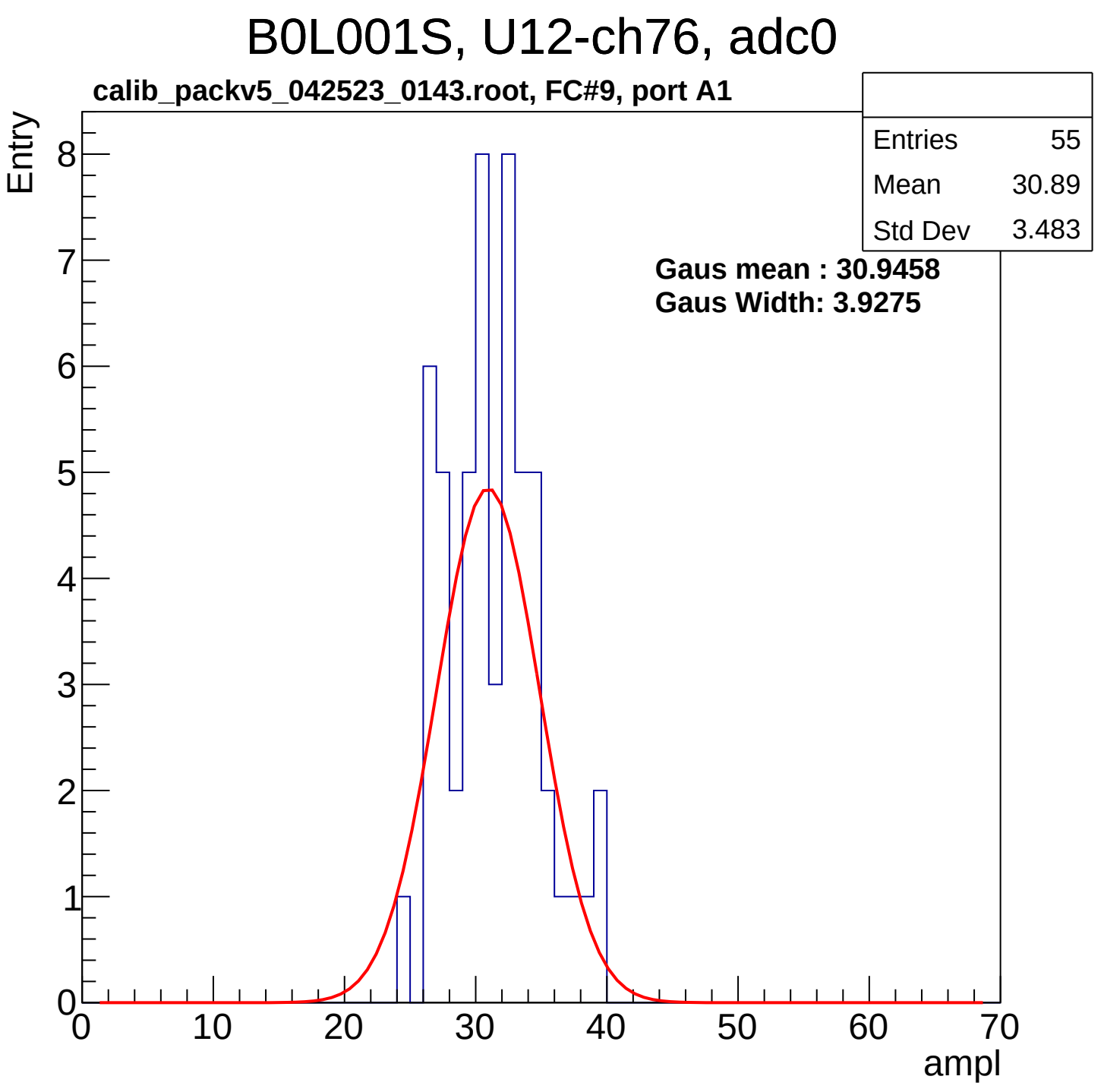
B0L001S, U12-ch76, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 55
Mean 30.89
Std Dev 3.483
Gaus mean : 30.9458
Gaus Width: 3.9275
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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40
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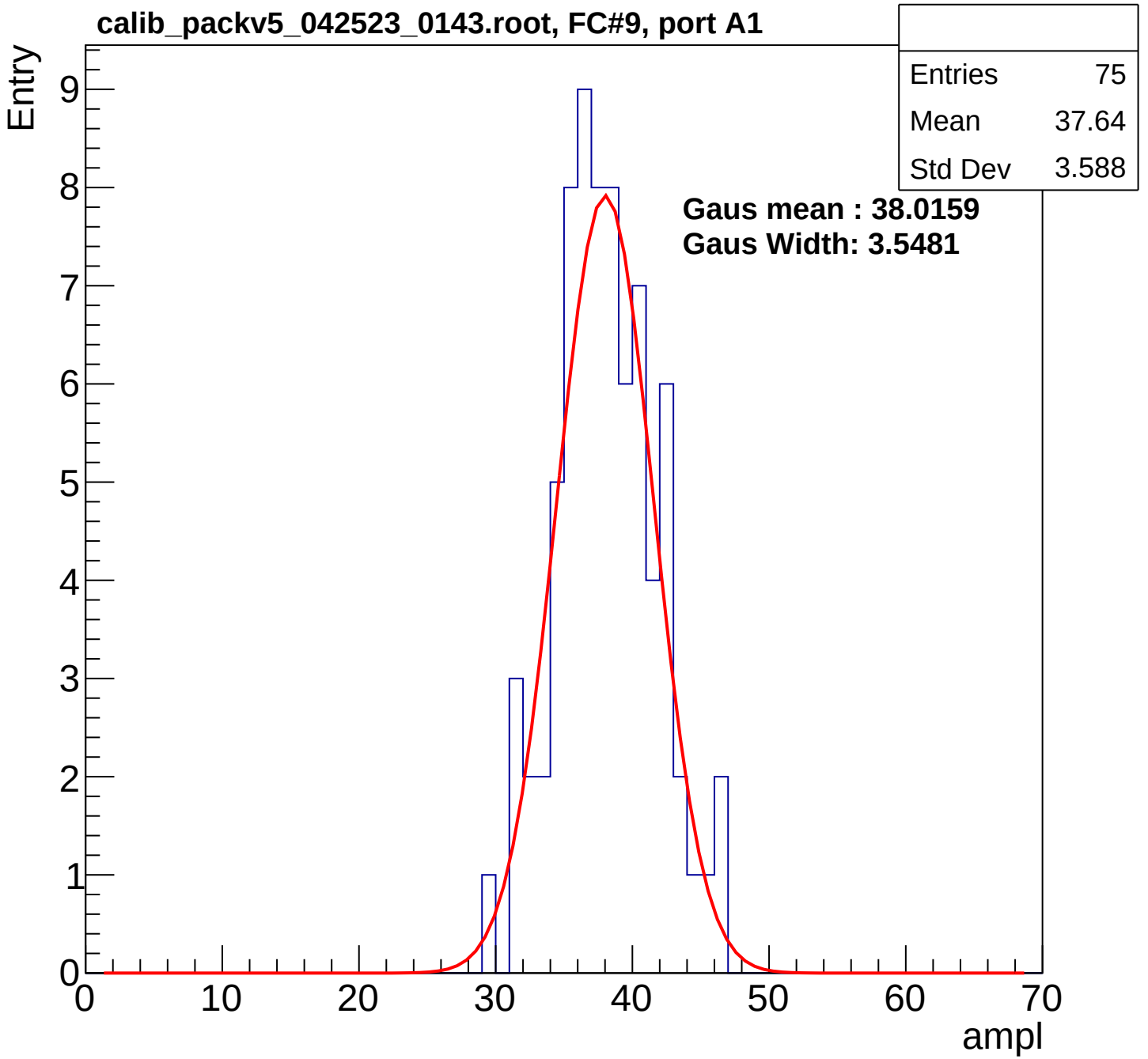
60
70


B0L001S, U12-ch76, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 75
Mean 37.64
Std Dev 3.588
Gaus mean : 38.0159
Gaus Width: 3.5481
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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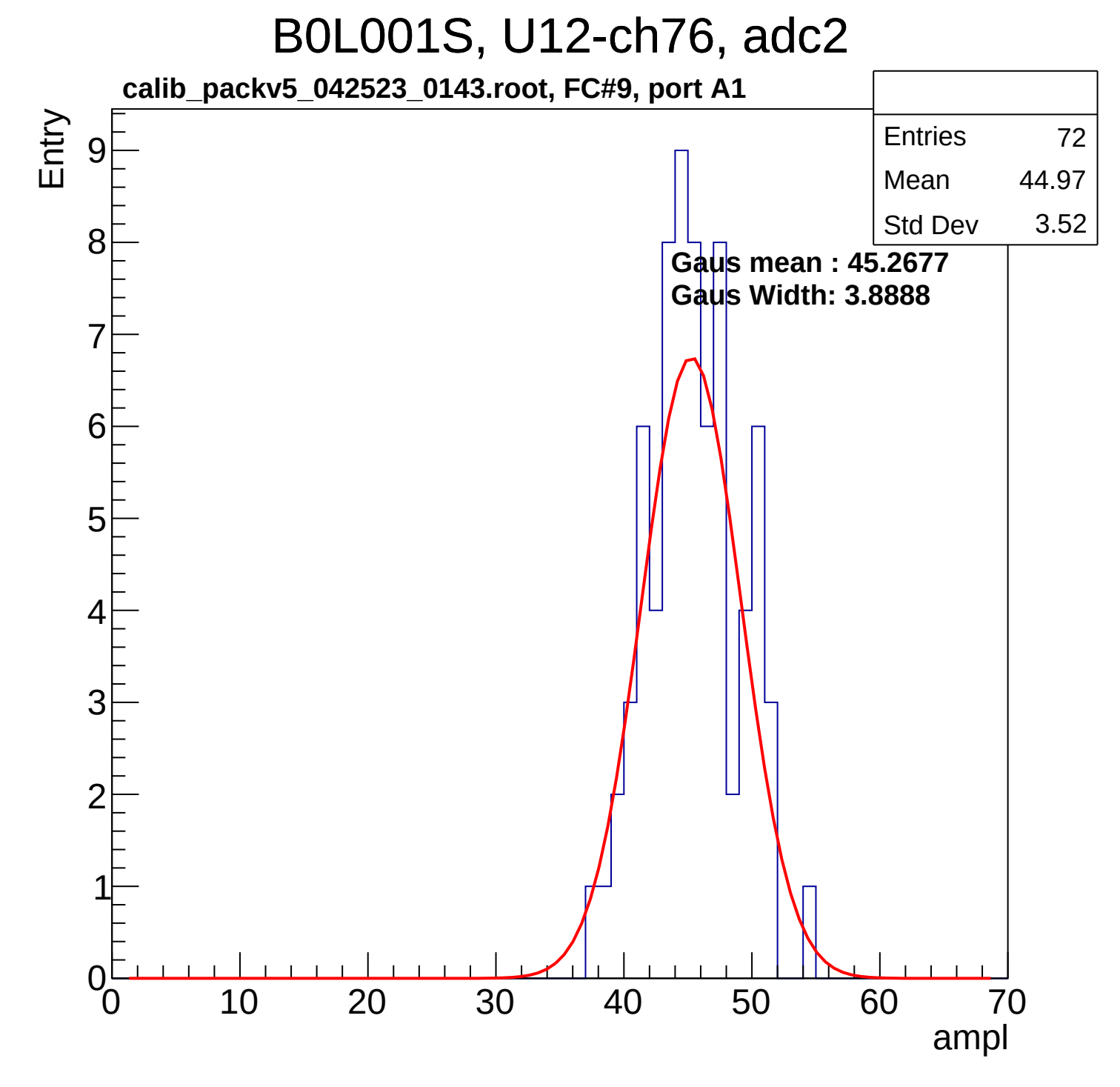
40
50
60
70


B0L001S, U12-ch76, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 72
Mean 44.97
Std Dev 3.52
Gaus mean : 45.2677
Gaus Width: 3.8888
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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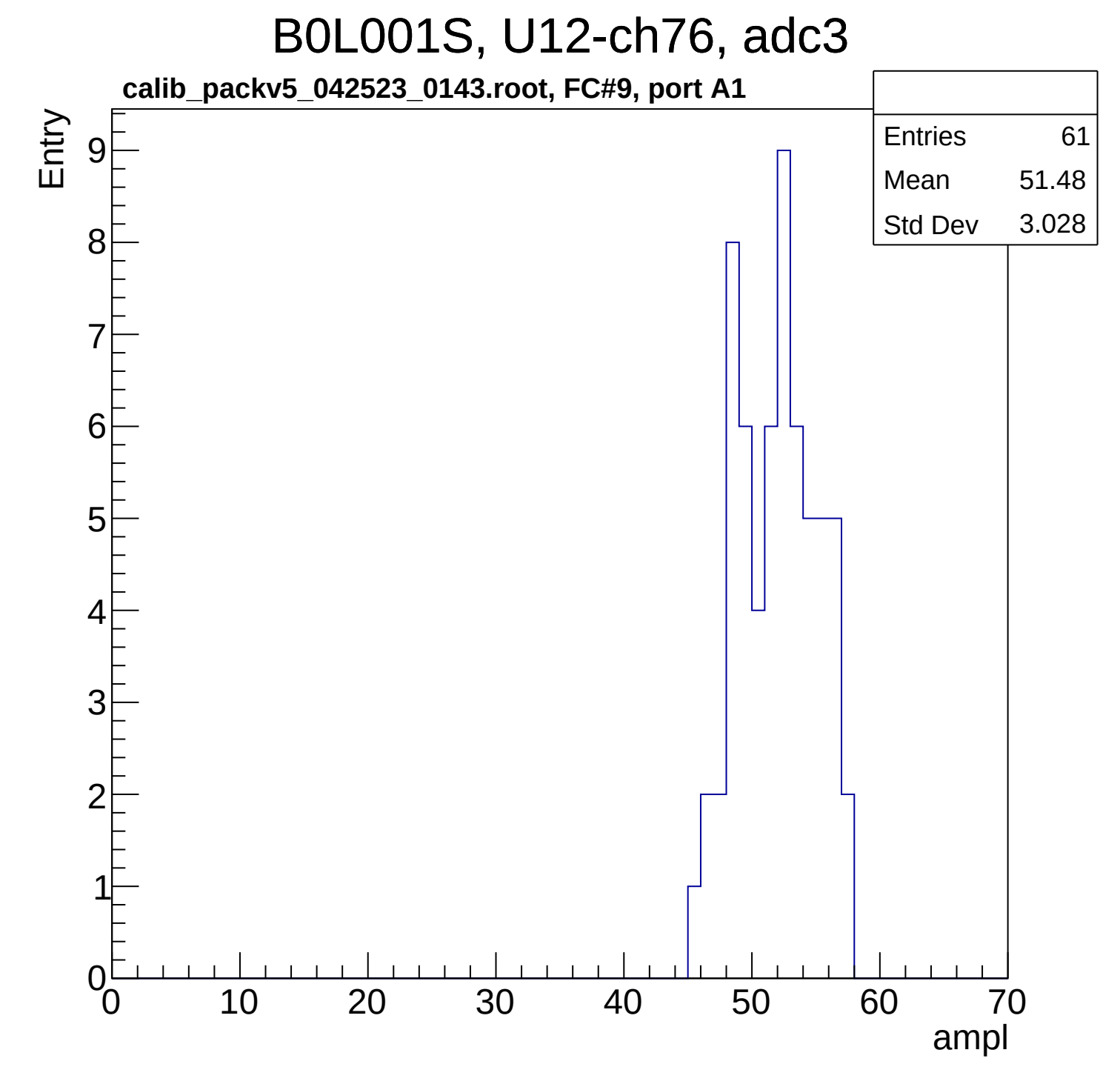
B0L001S, U12-ch76, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 61
Mean 51.48
Std Dev 3.028
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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60
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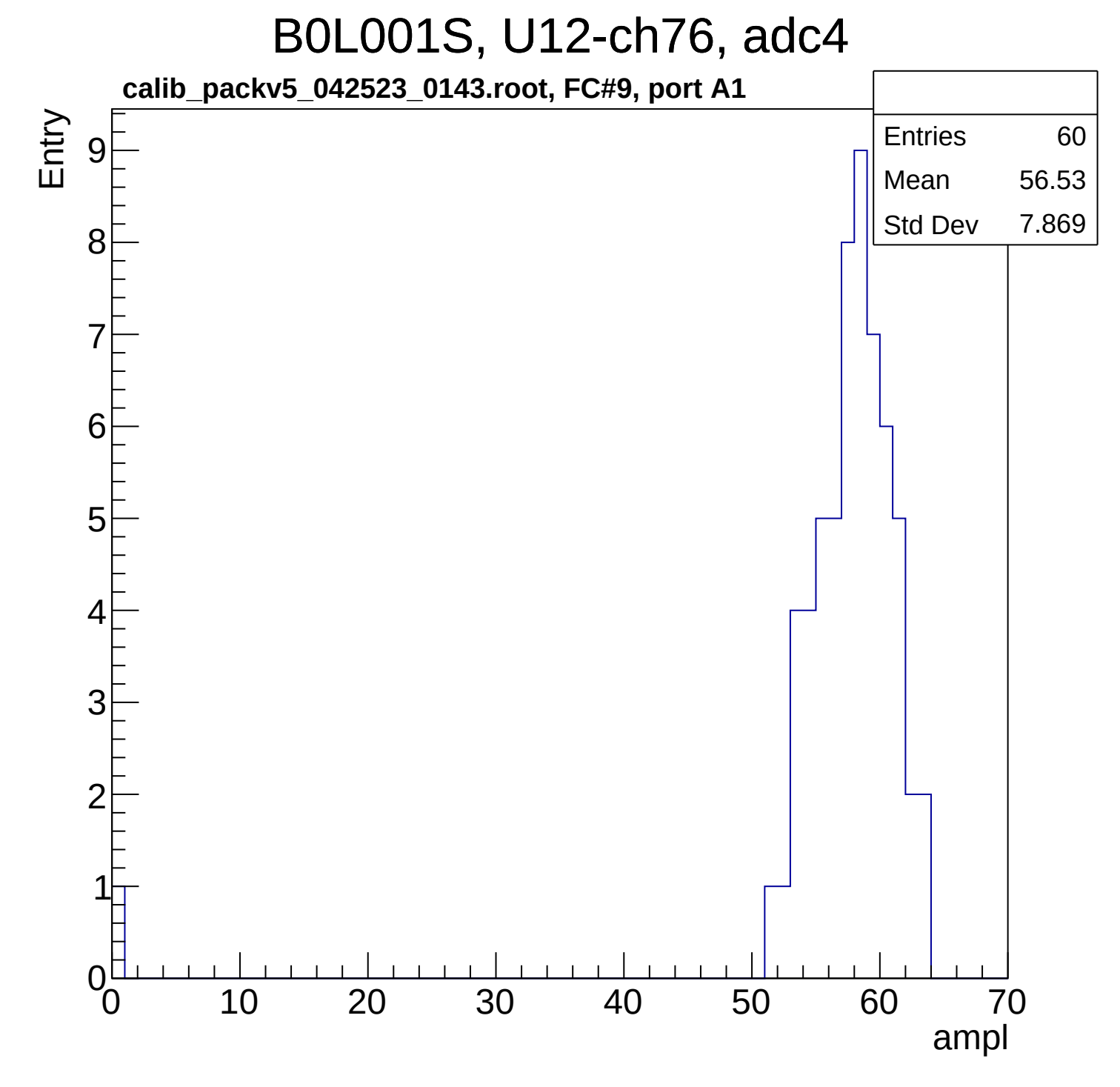
B0L001S, U12-ch76, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 60
Mean 56.53
Std Dev 7.869
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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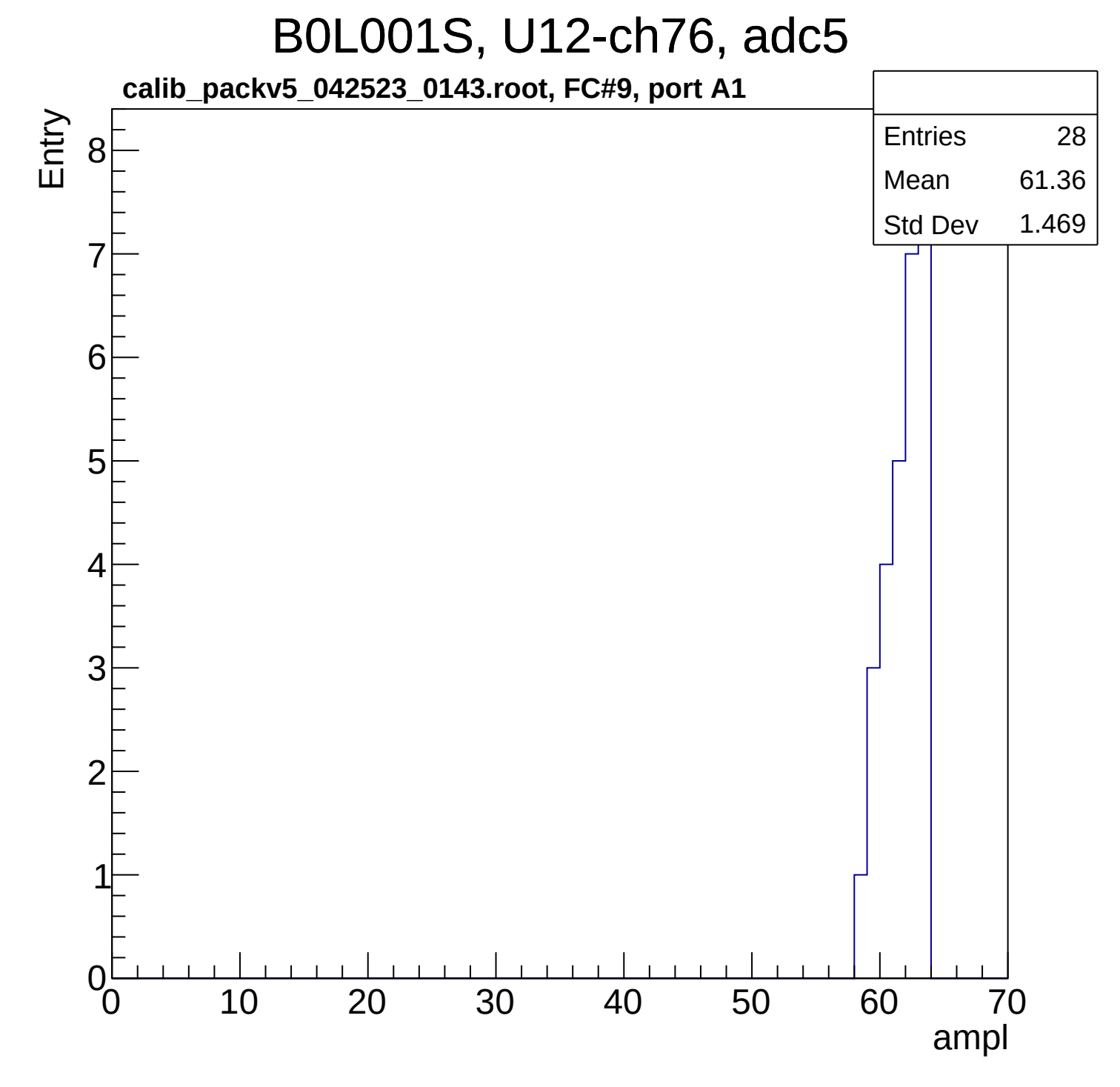
B0L001S, U12-ch76, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 28
Mean 61.36
Std Dev 1.469
Entry
ampl
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4
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6
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0
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60
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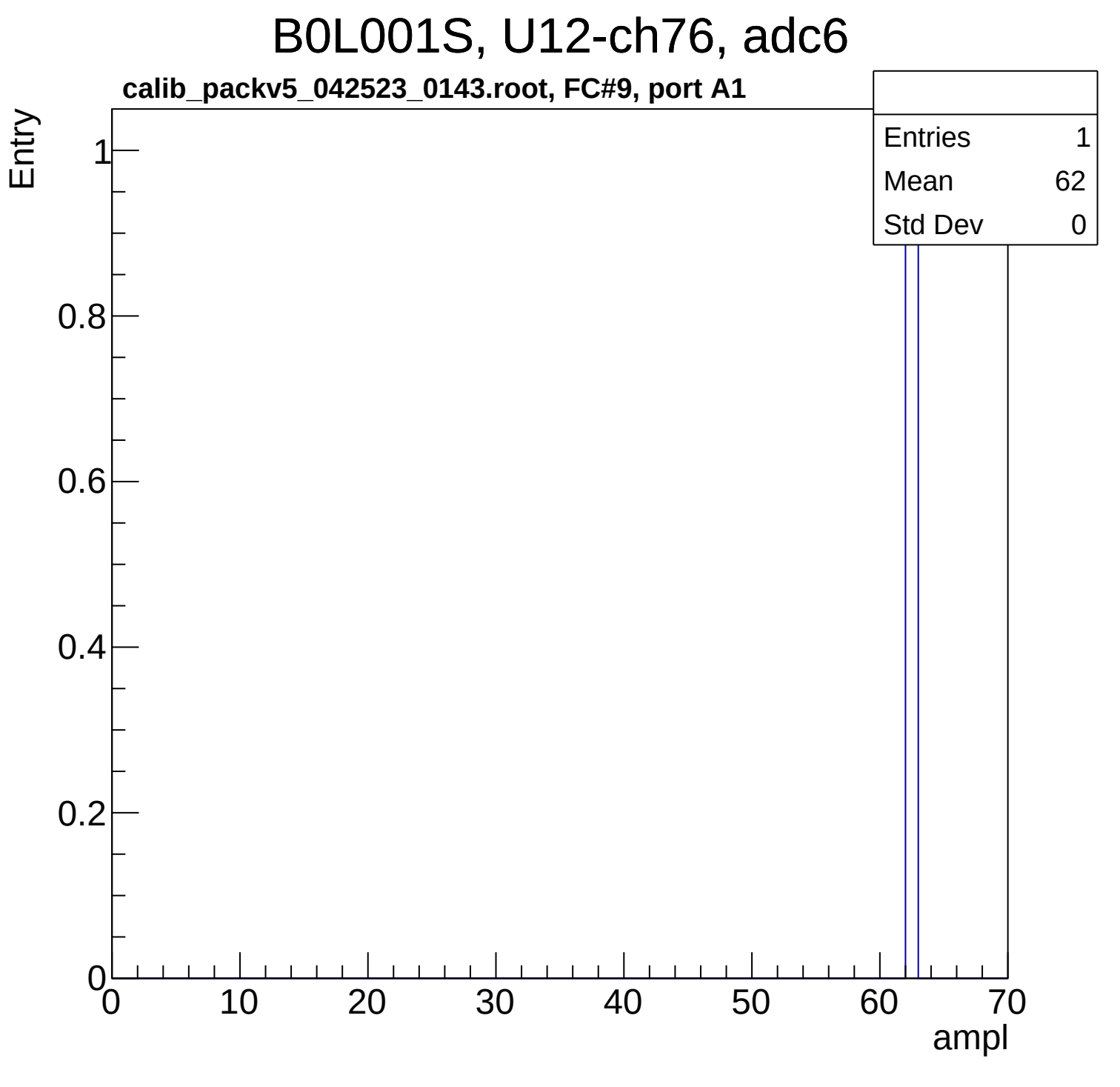
B0L001S, U12-ch76, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 62
Std Dev 0
Entry
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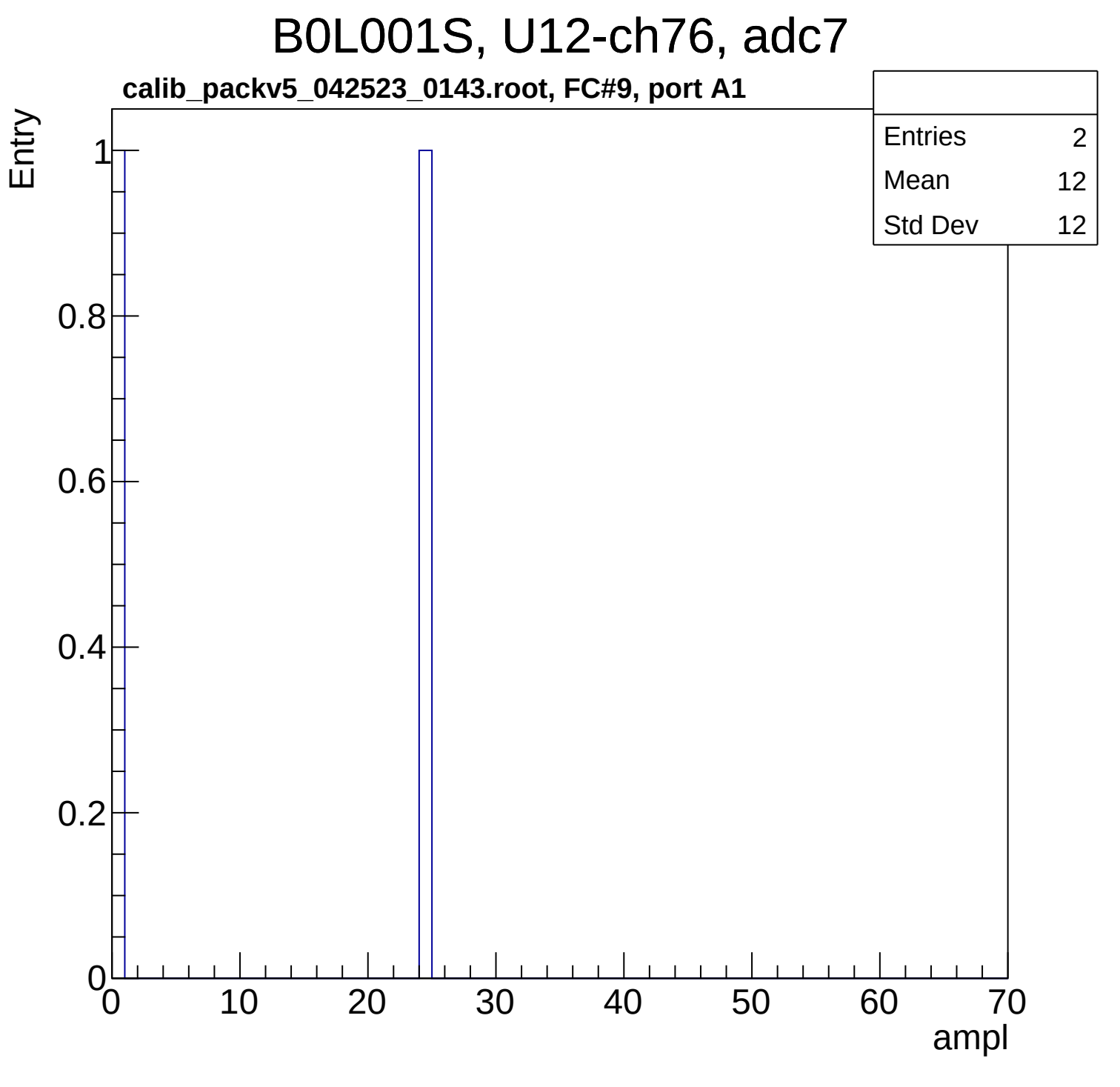
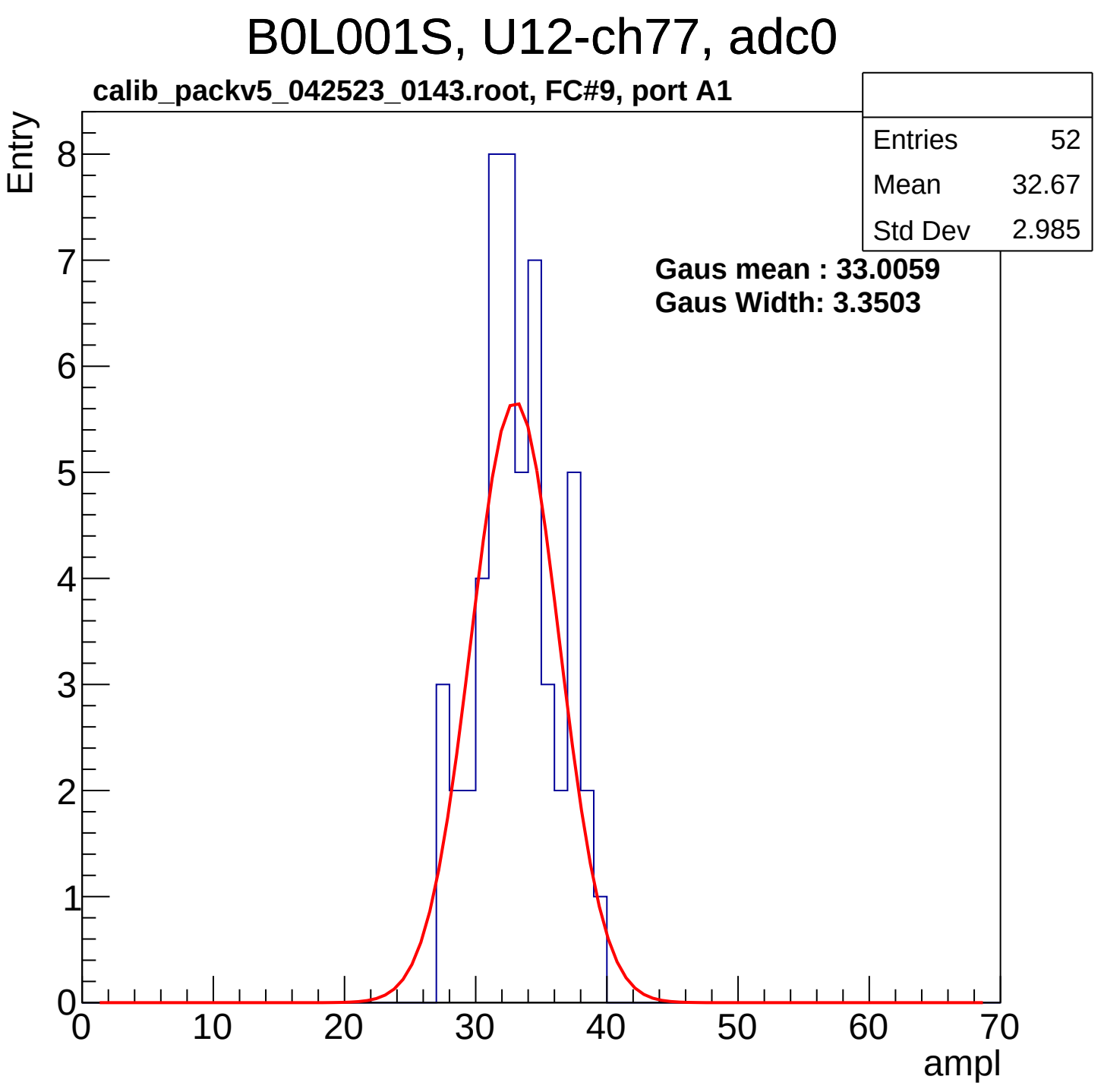
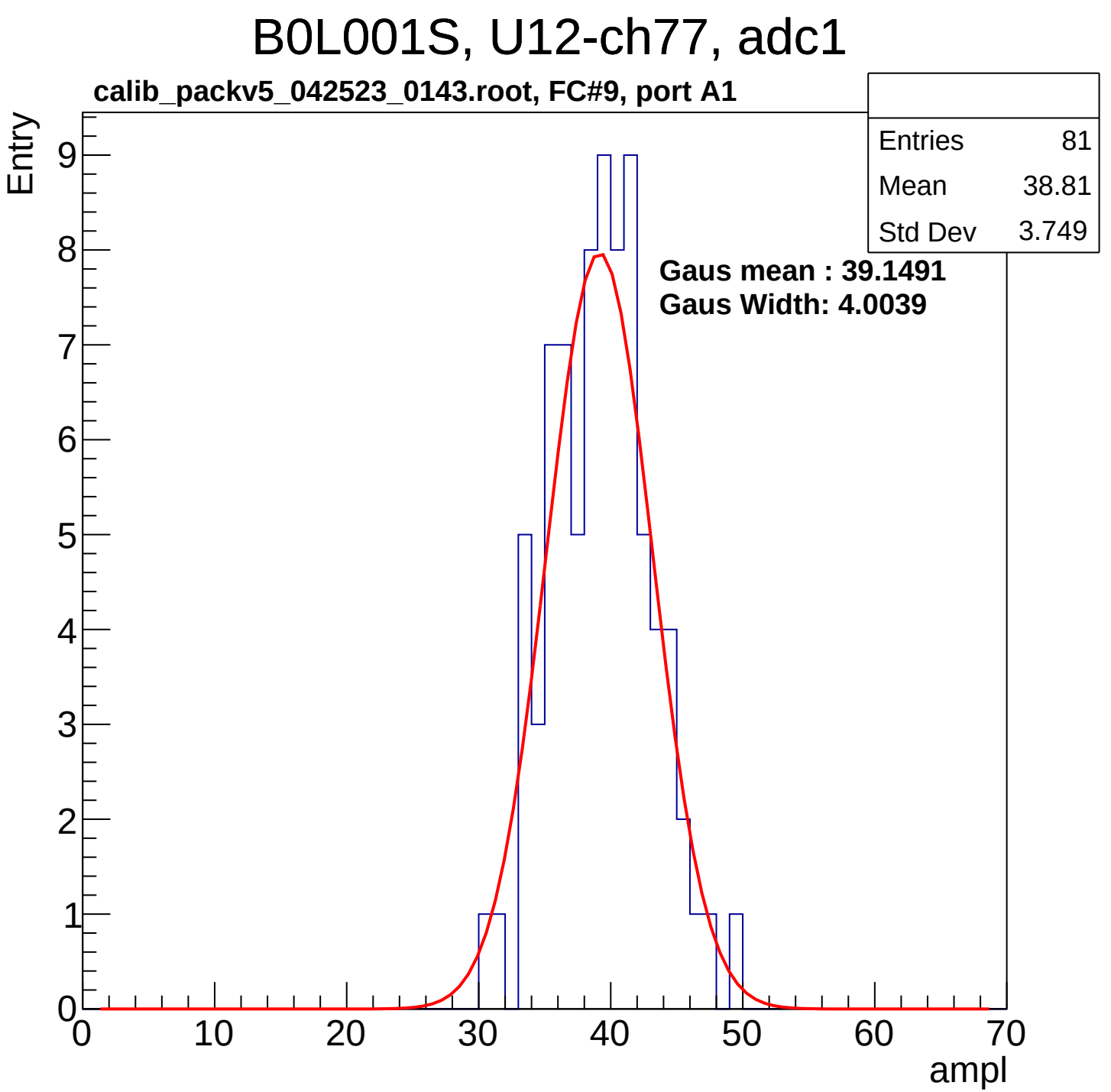
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch76, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 12
Std Dev 12
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch77, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 52
Mean 32.67
Std Dev 2.985
Gaus mean : 33.0059
Gaus Width: 3.3503
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch77, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 81
Mean 38.81
Std Dev 3.749
Gaus mean : 39.1491
Gaus Width: 4.0039
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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40
50
60
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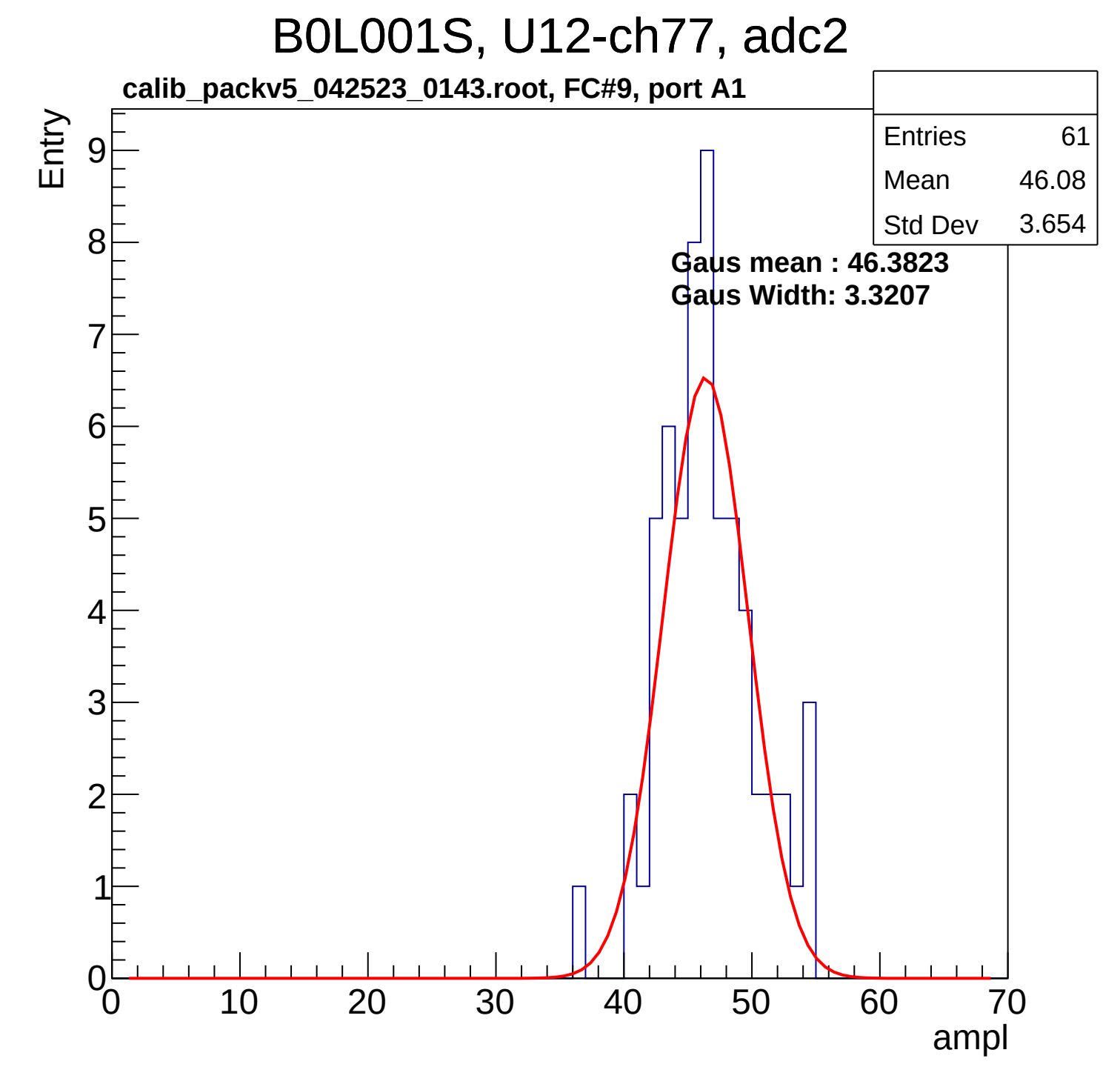
B0L001S, U12-ch77, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 61
Mean 46.08
Std Dev 3.654
Gaus mean : 46.3823
Gaus Width: 3.3207
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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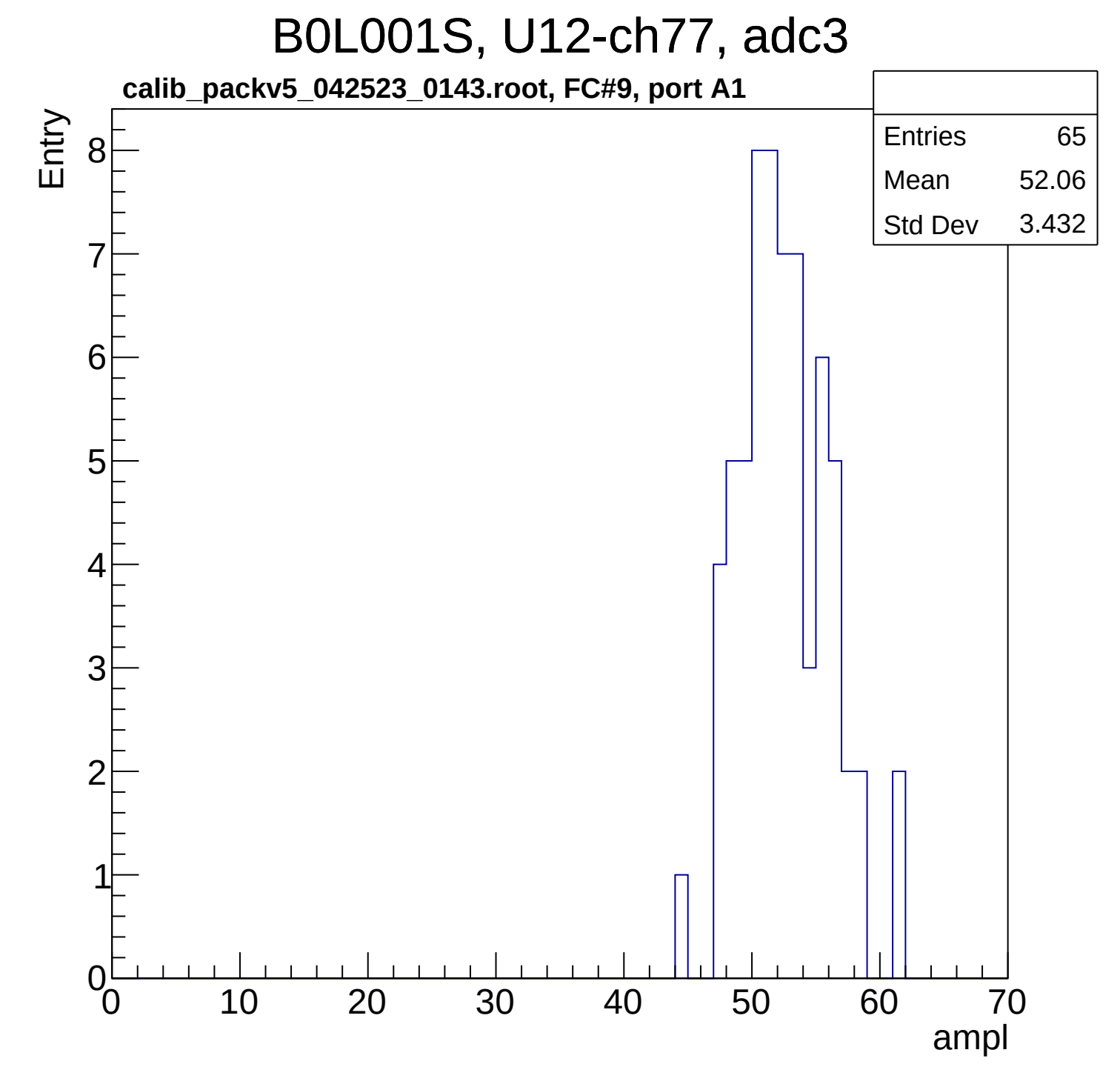
B0L001S, U12-ch77, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 65
Mean 52.06
Std Dev 3.432
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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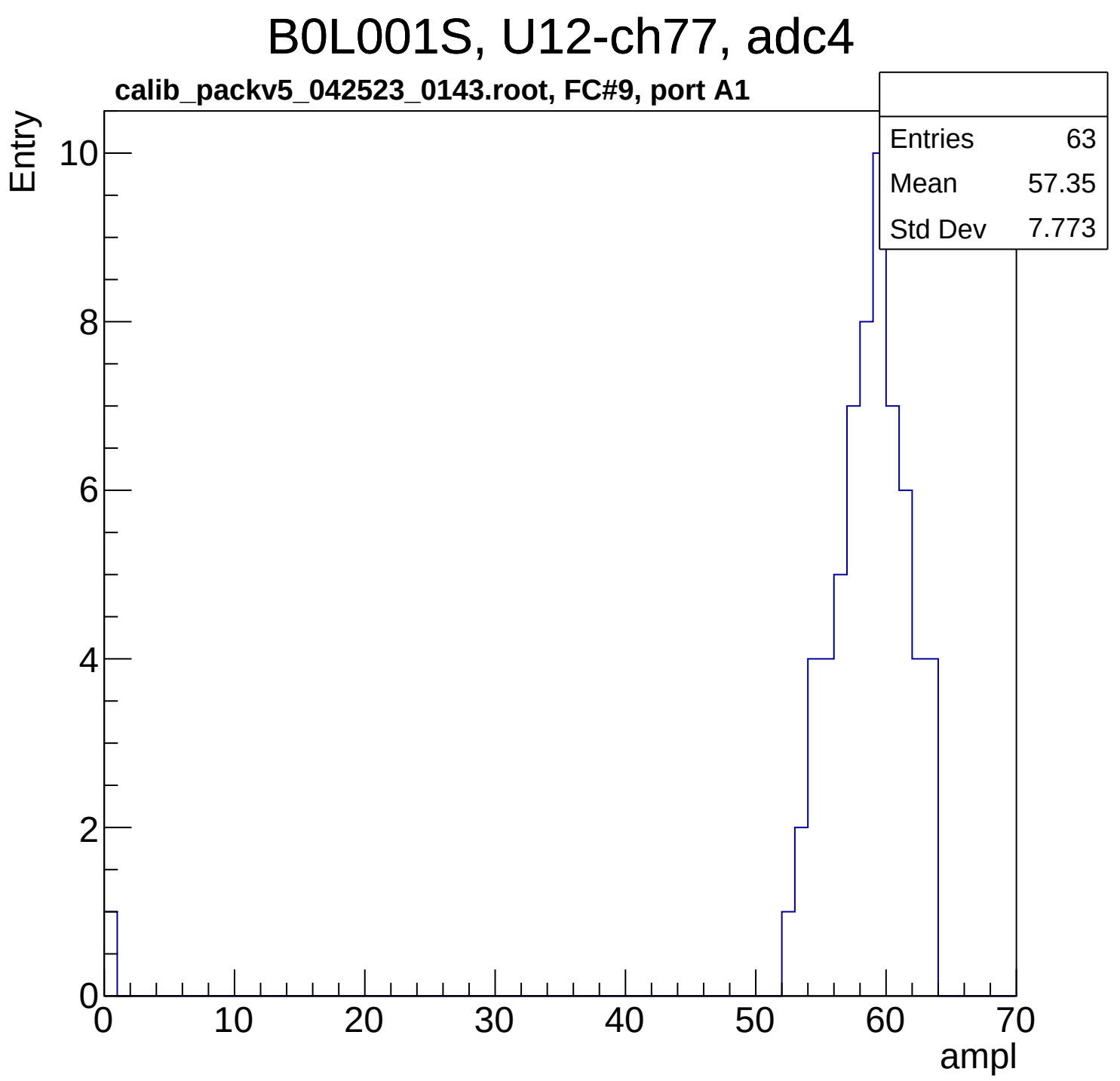
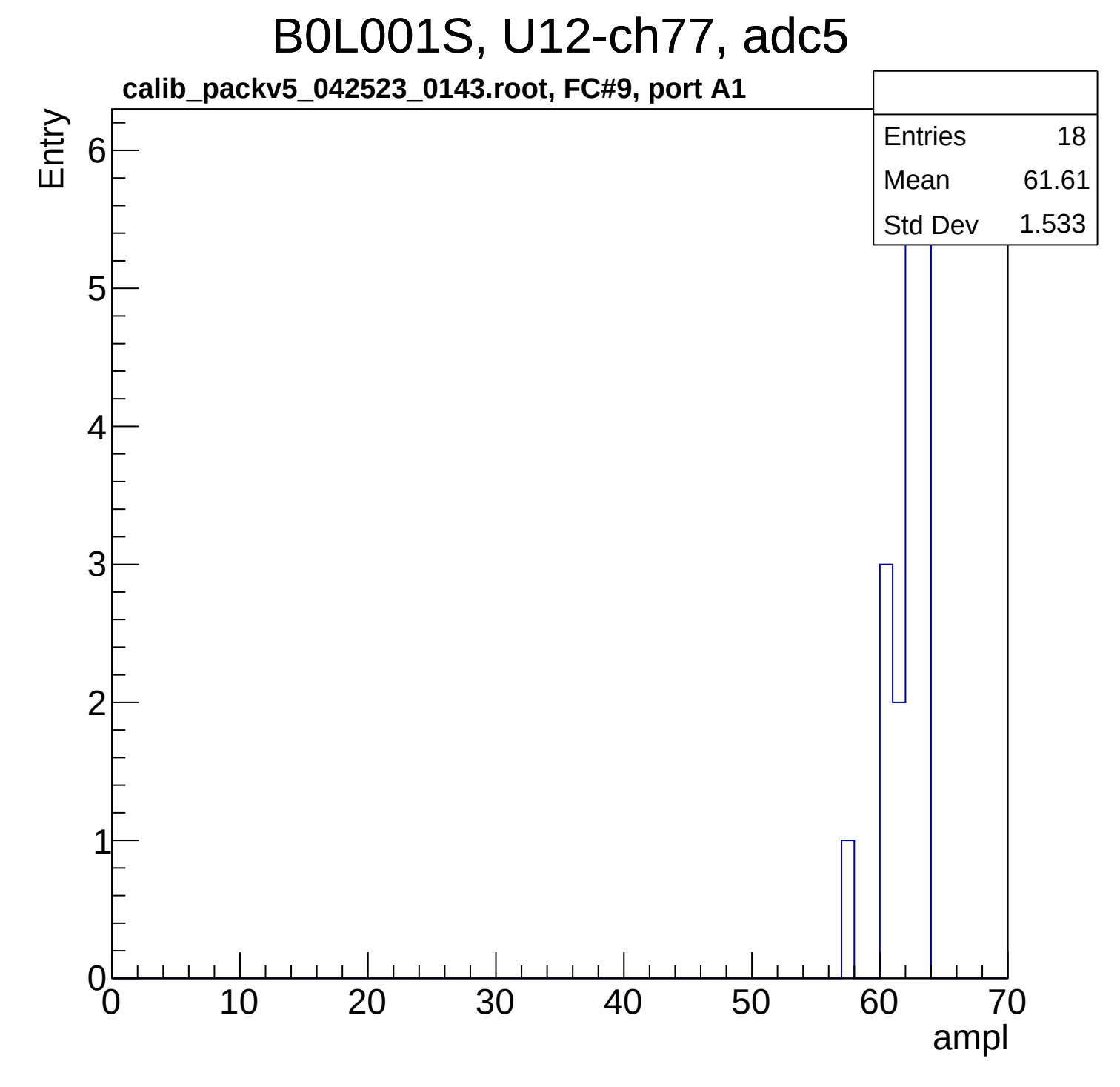
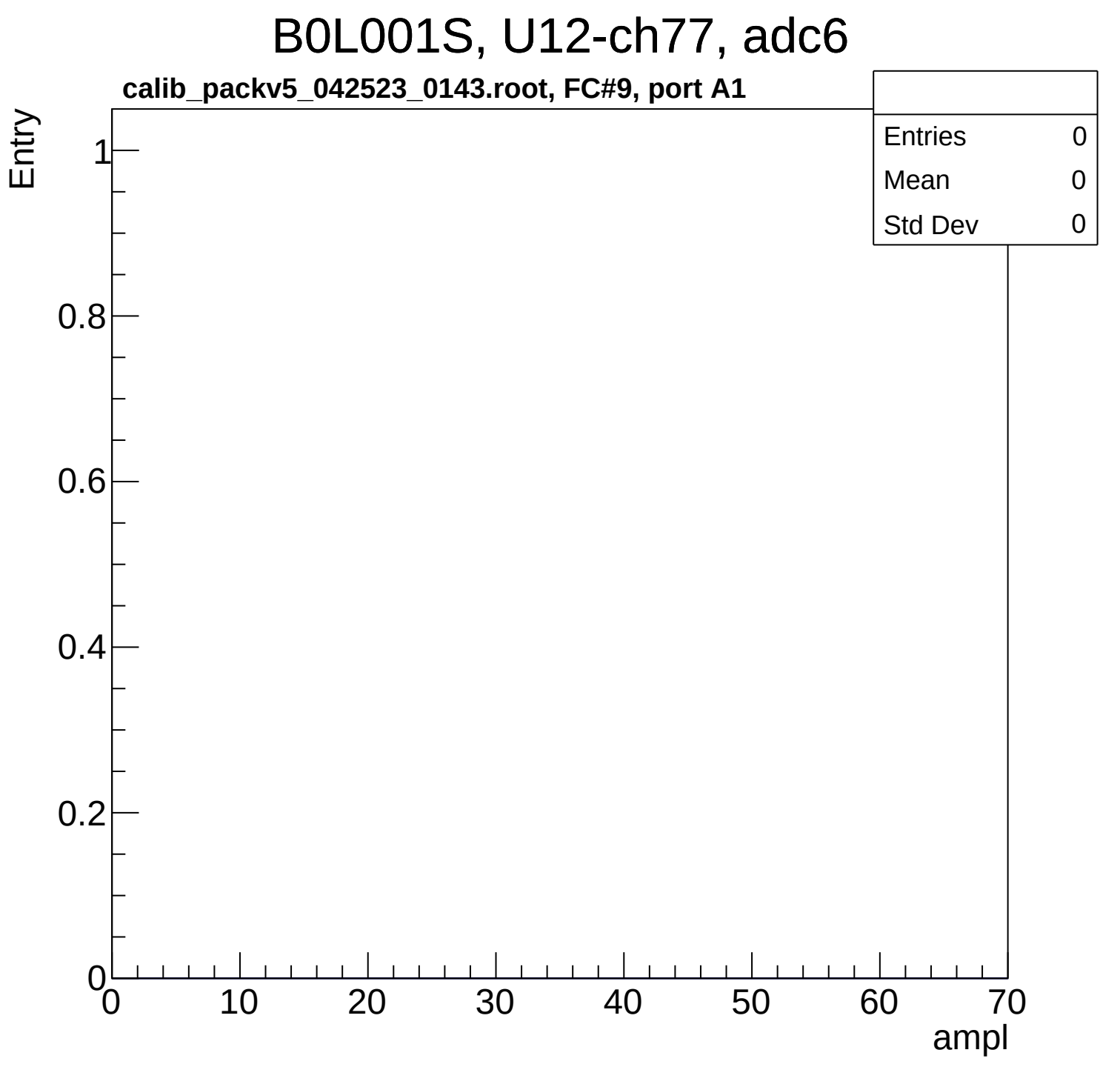
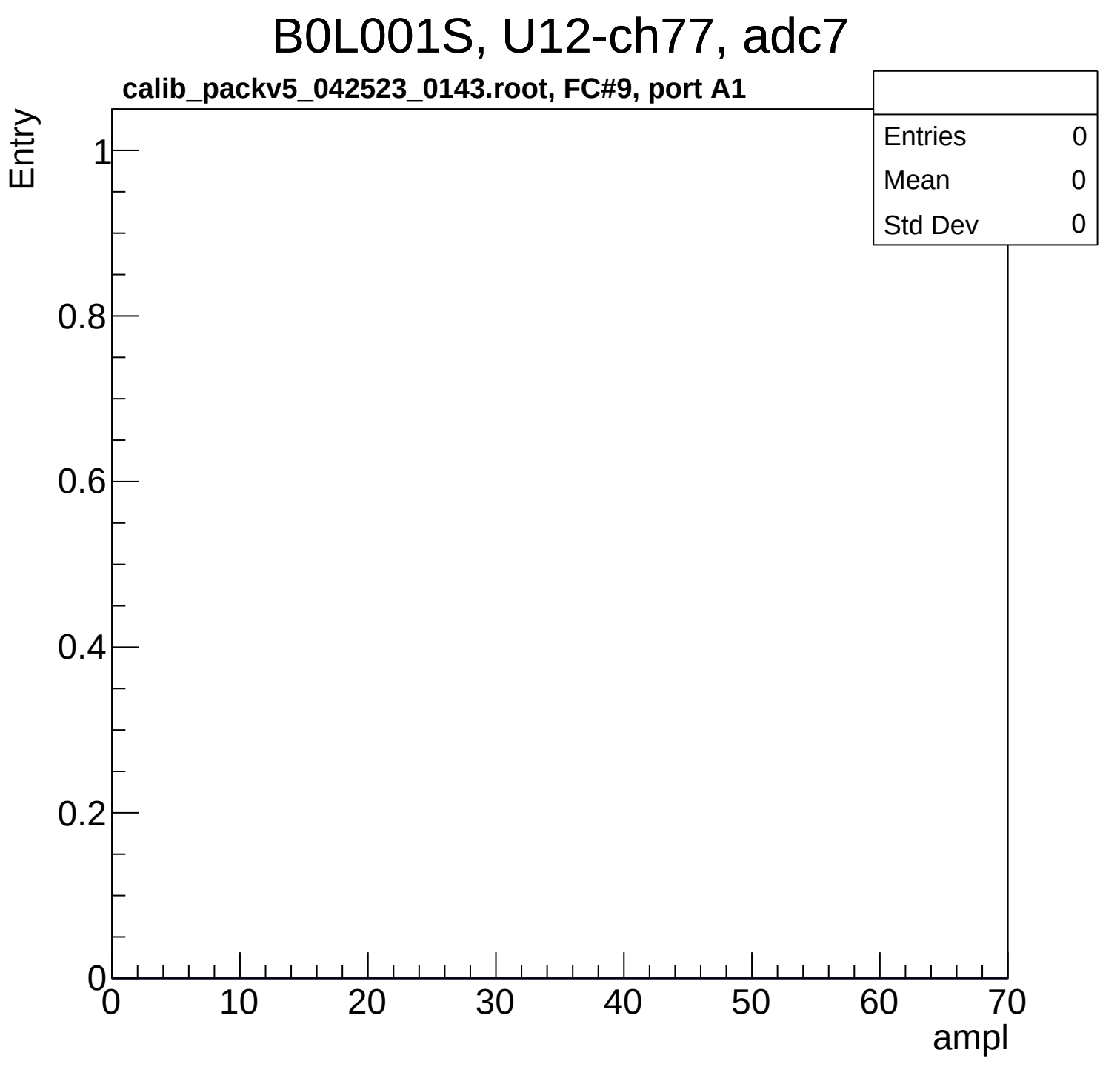
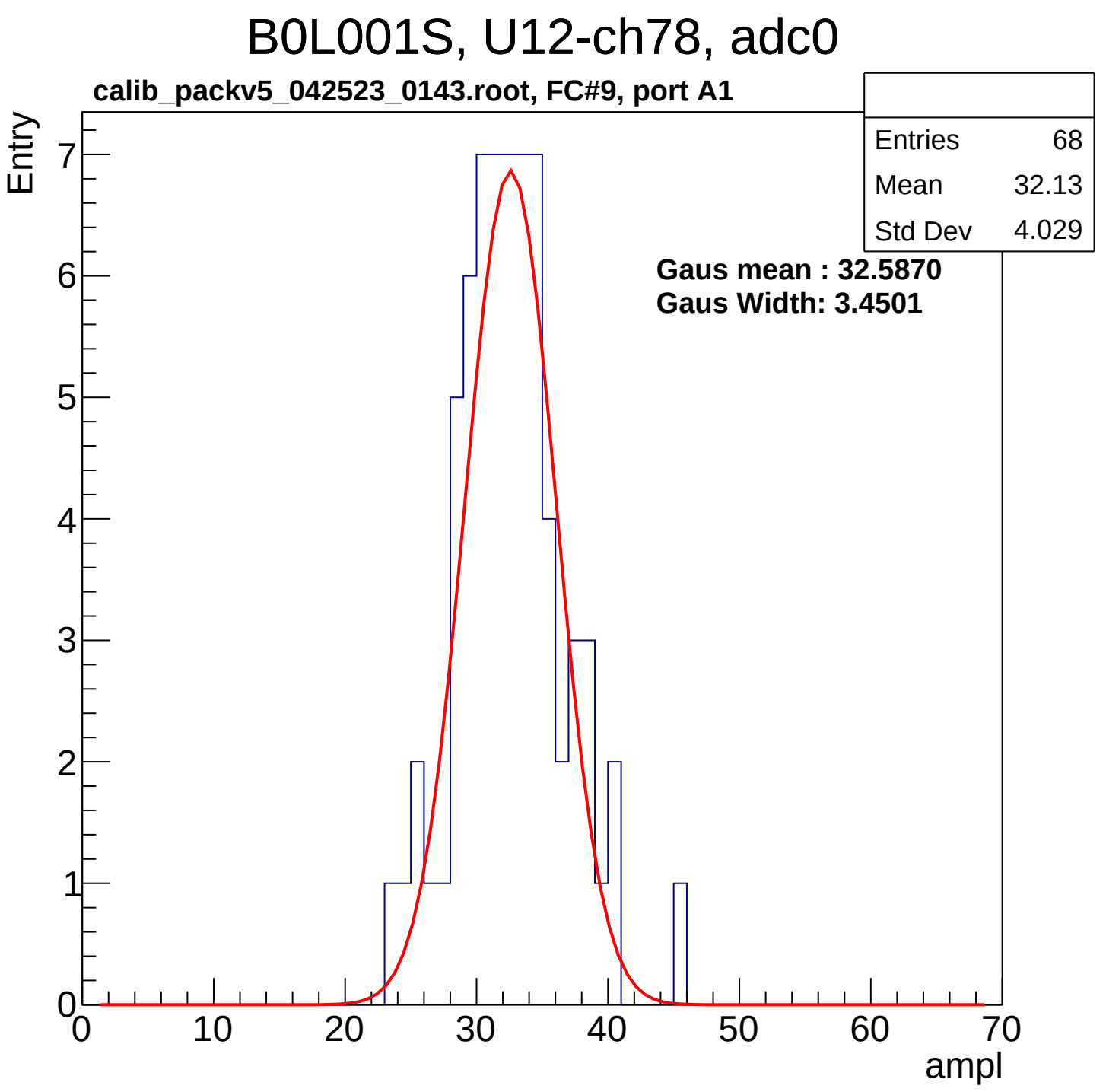
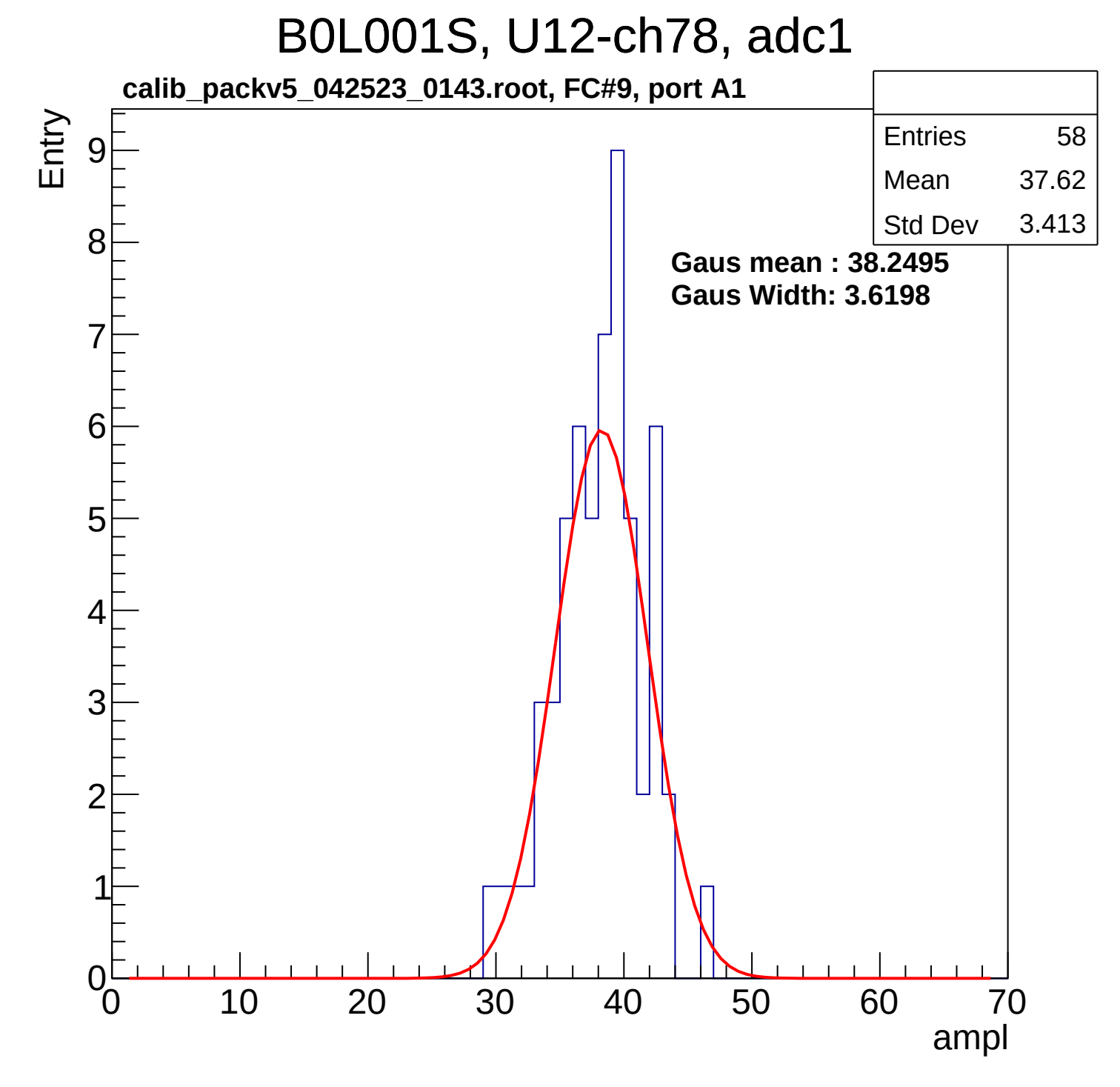

B0L001S, U12-ch77, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 63
Mean 57.35
Std Dev 7.773
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

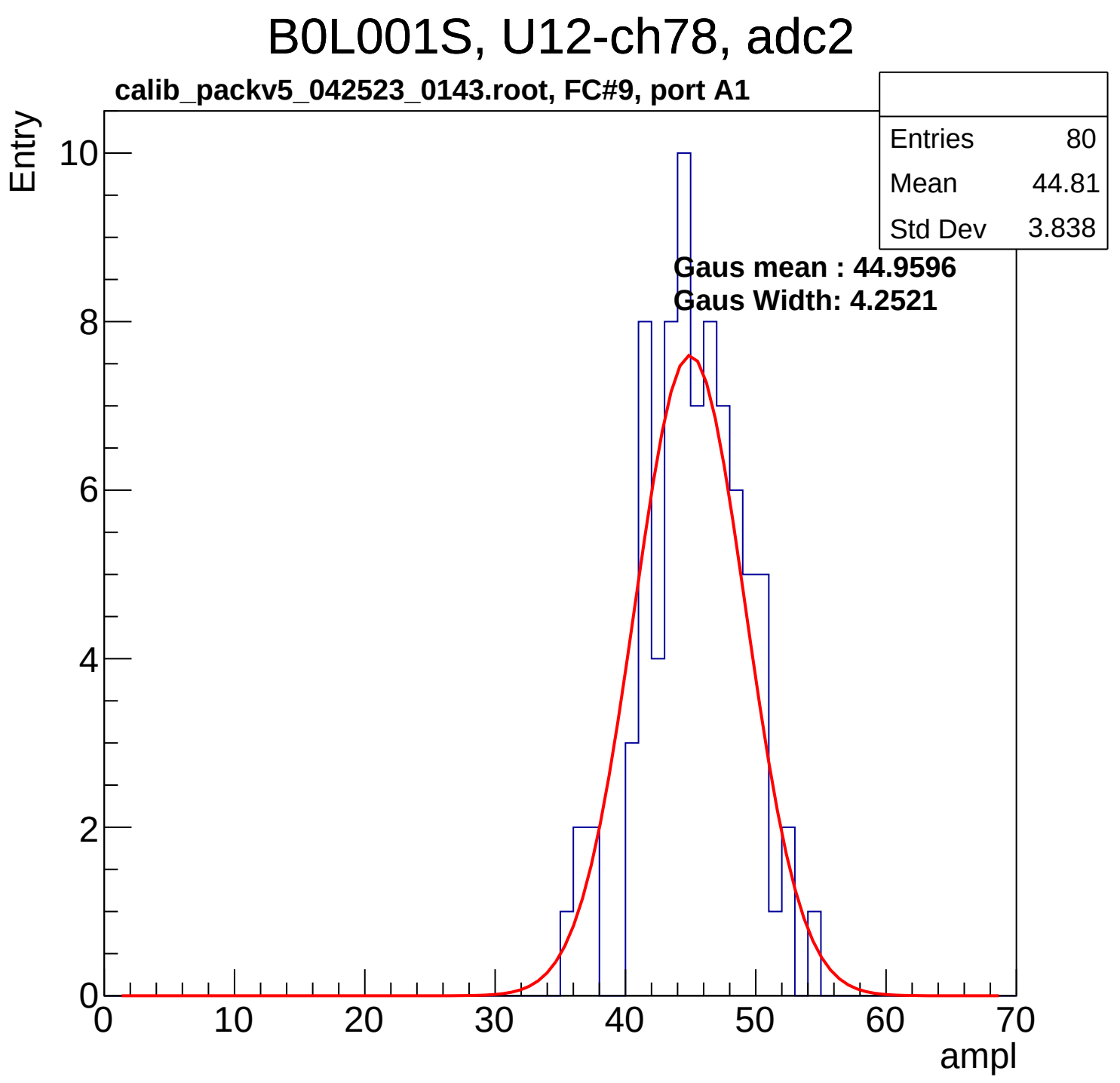

B0L001S, U12-ch77, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 18
Mean 61.61
Std Dev 1.533
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

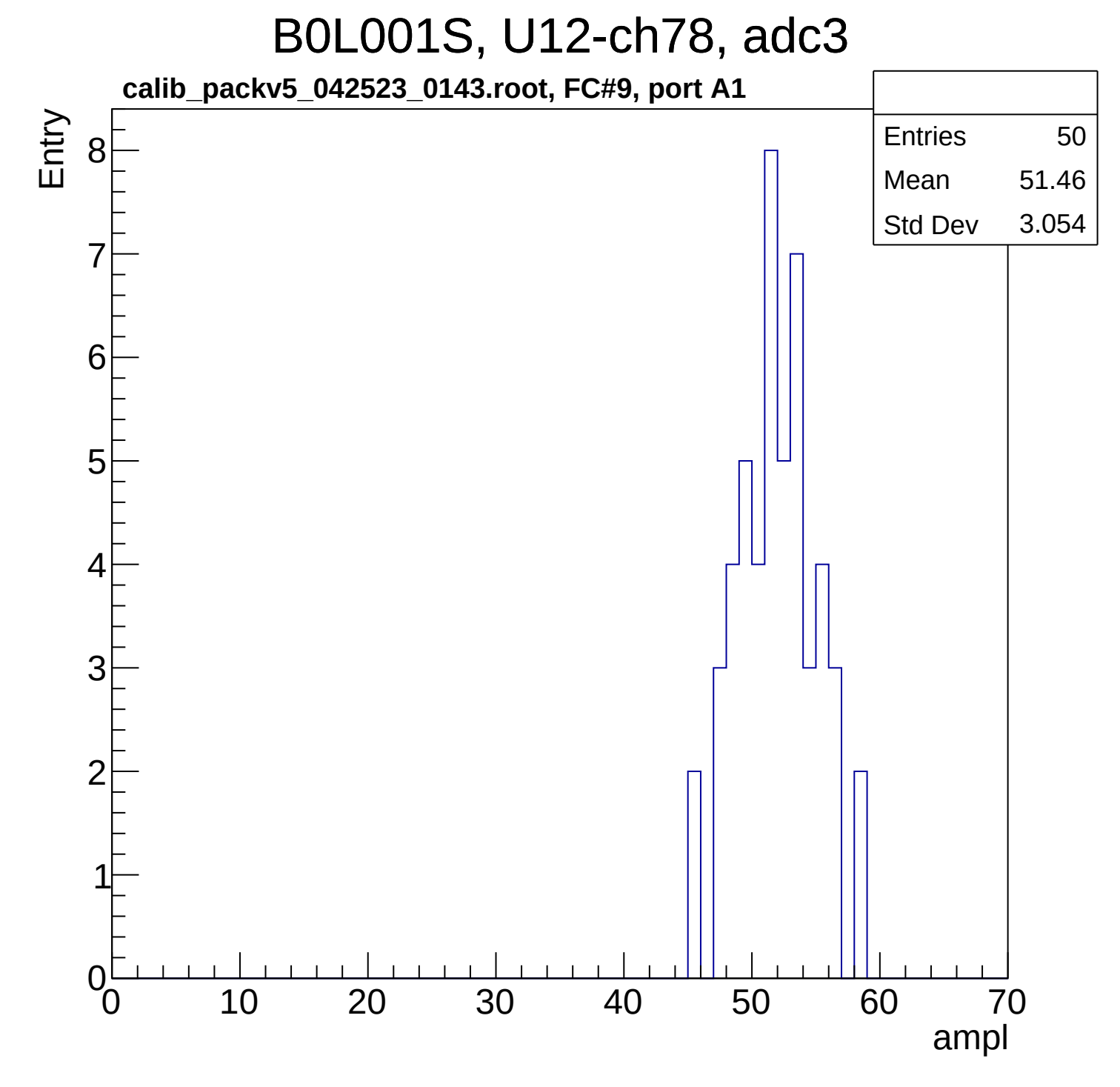

B0L001S, U12-ch77, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

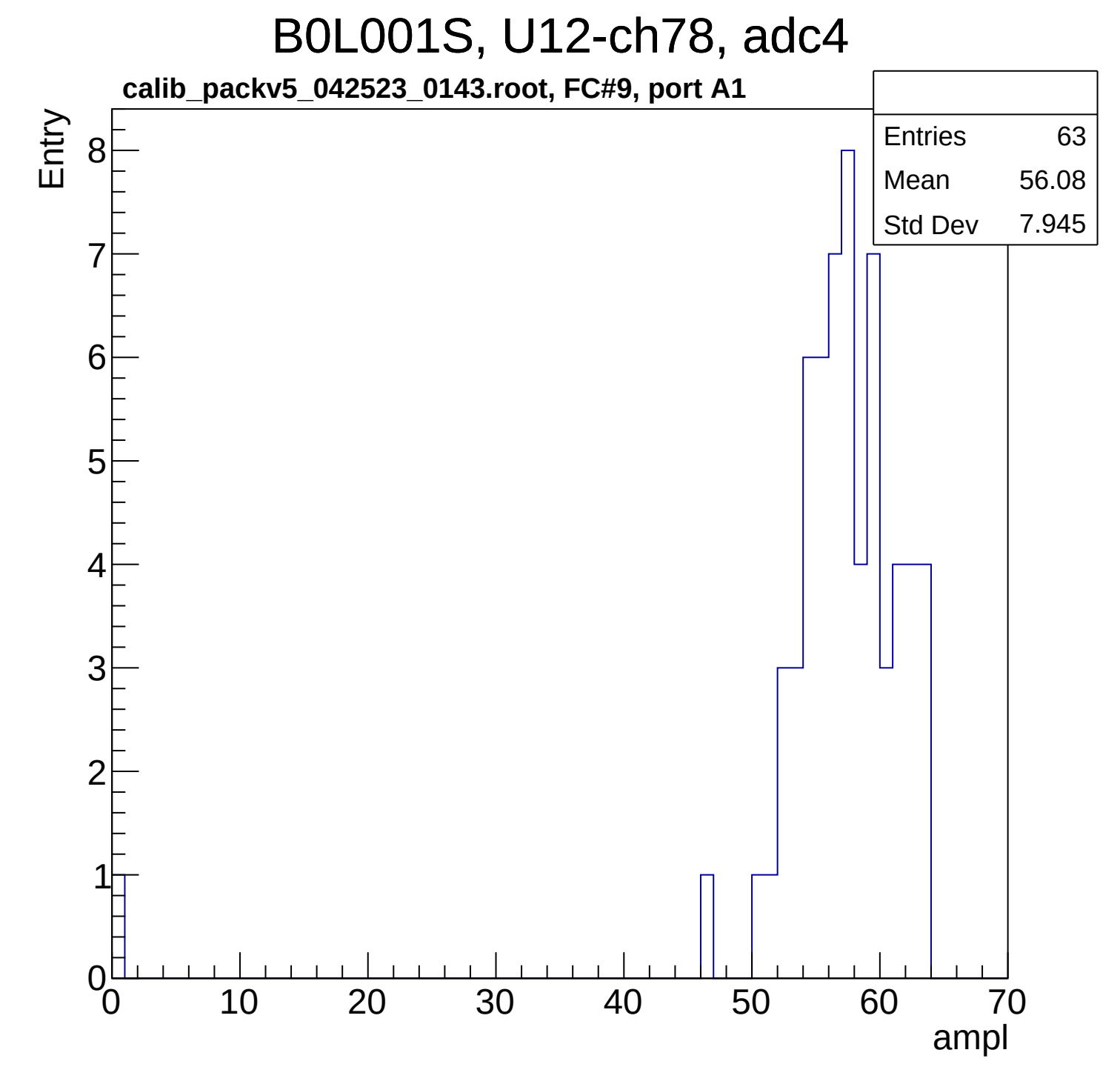

B0L001S, U12-ch77, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

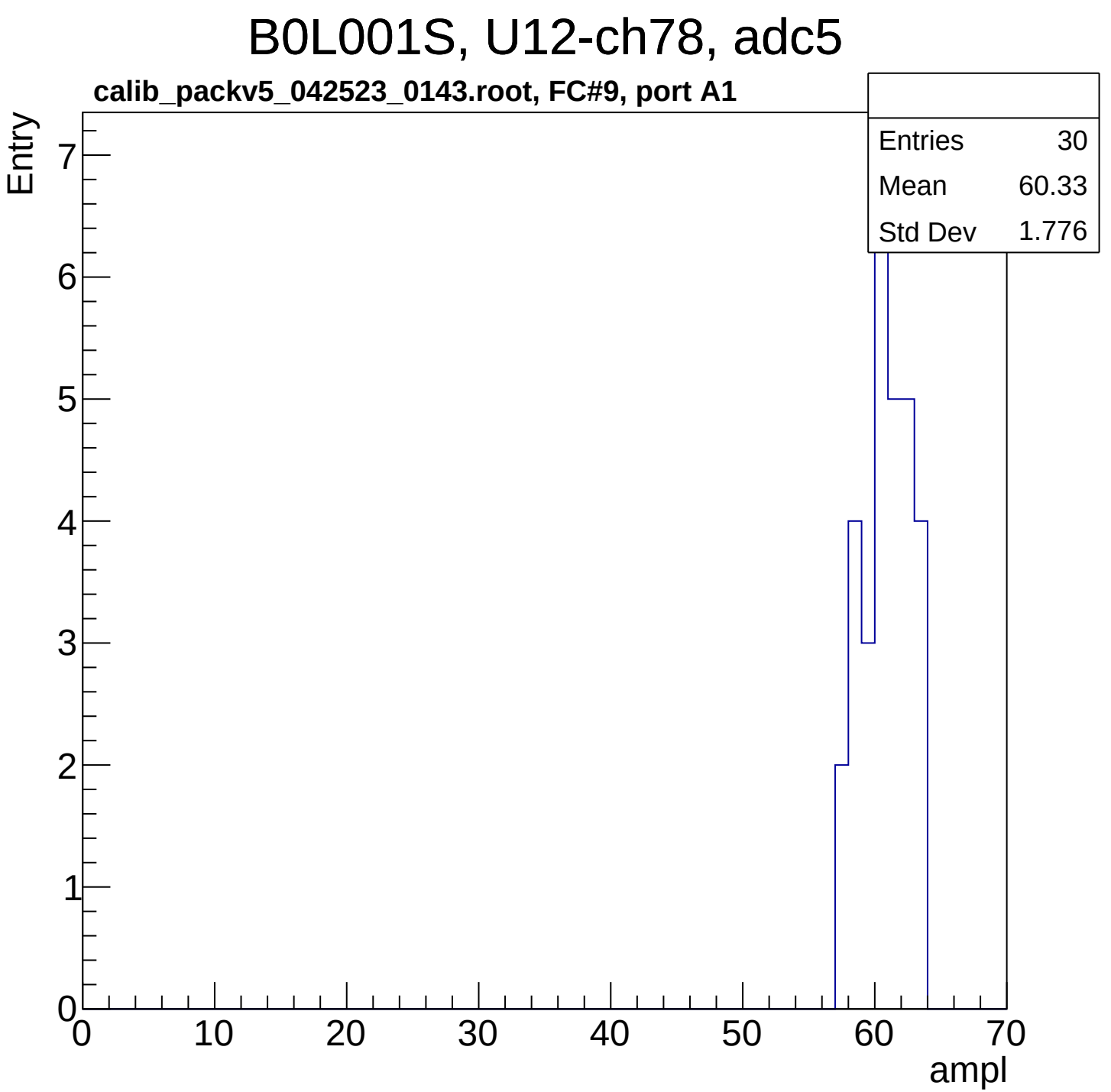

B0L001S, U12-ch78, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 68
Mean 32.13
Std Dev 4.029
Gaus mean : 32.5870
Gaus Width: 3.4501
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

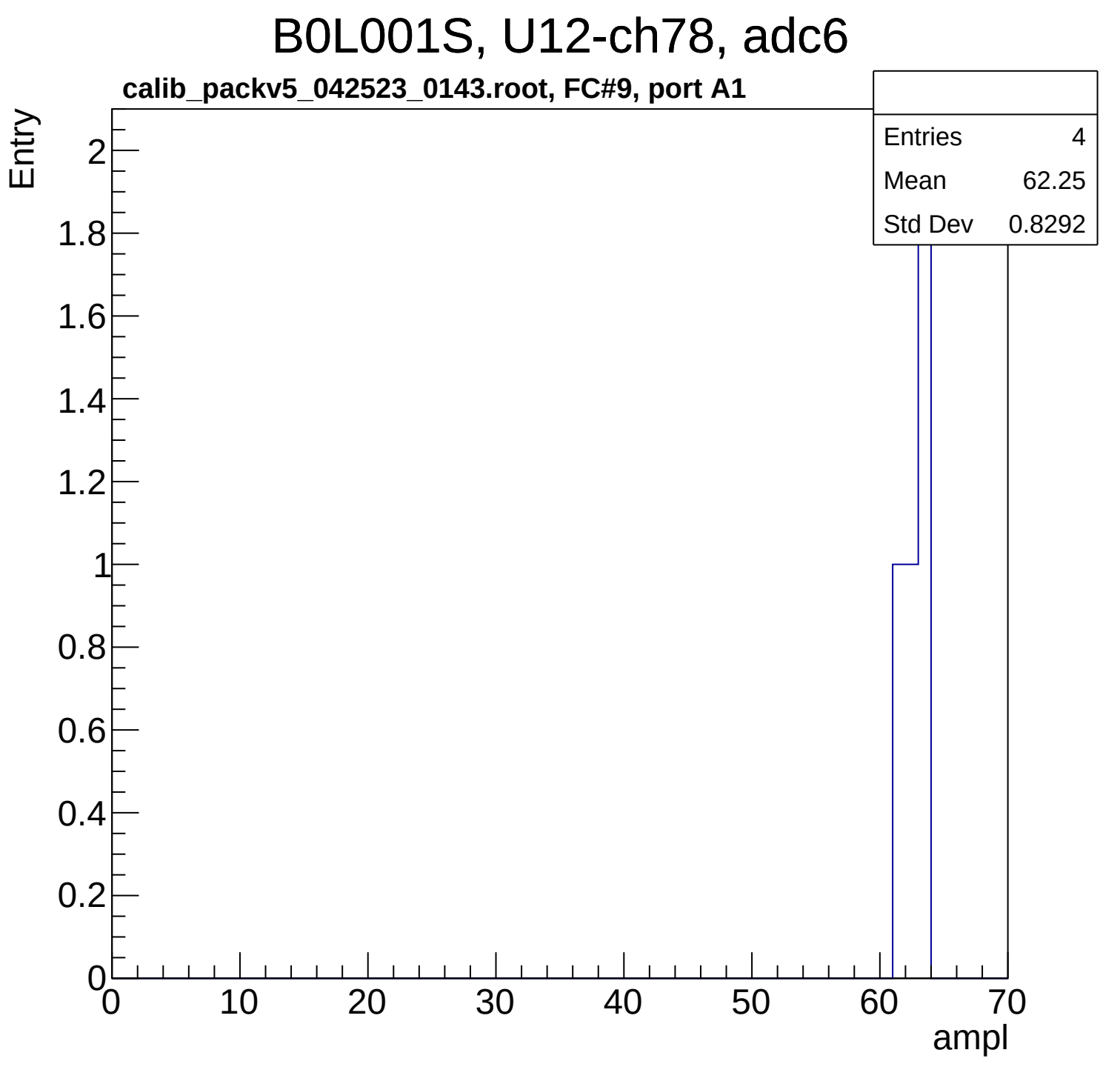

B0L001S, U12-ch78, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 58
Mean 37.62
Std Dev 3.413
Gaus mean : 38.2495
Gaus Width: 3.6198
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

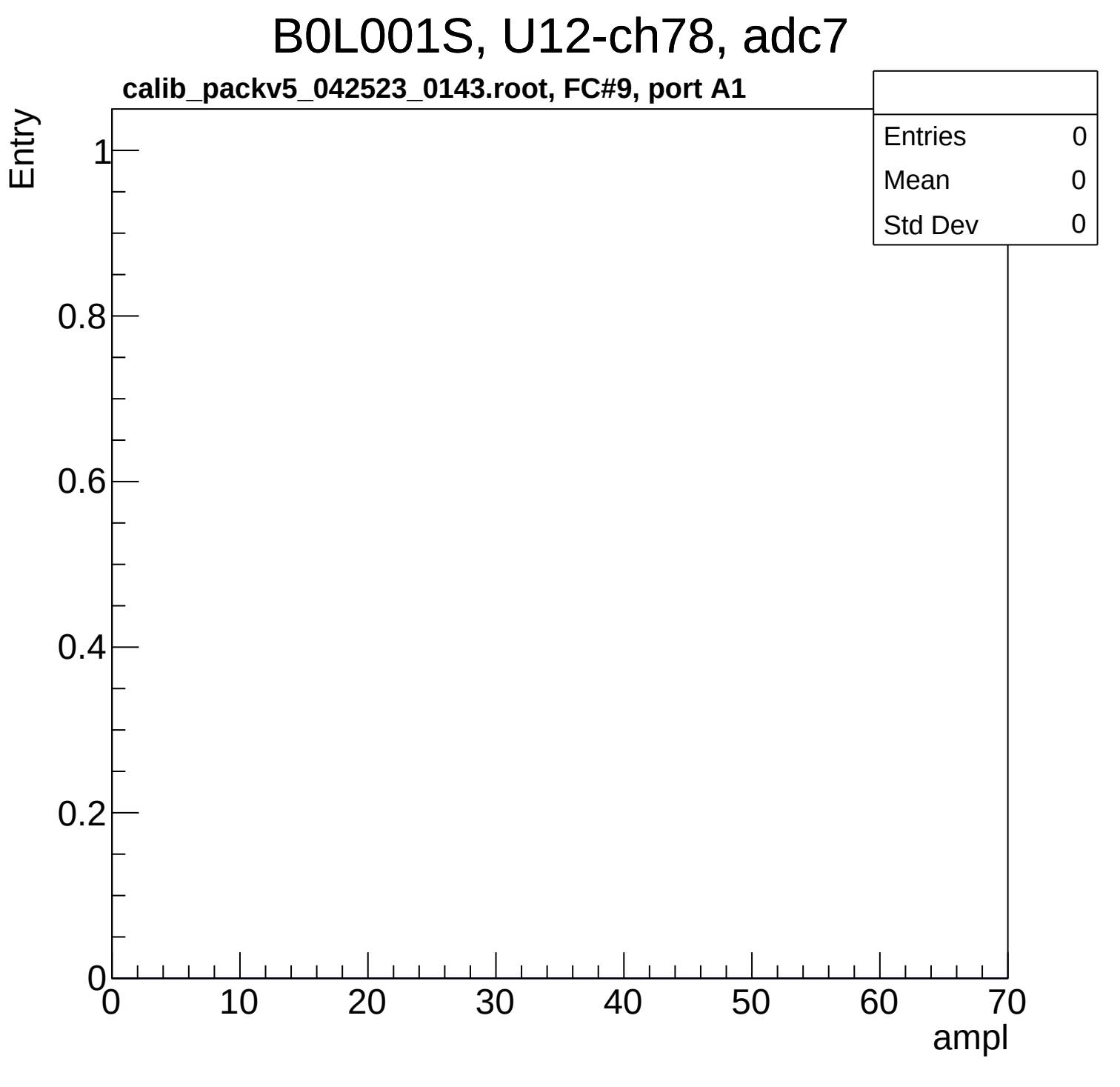

B0L001S, U12-ch78, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 80
Mean 44.81
Std Dev 3.838
Gaus mean : 44.9596
Gaus Width: 4.2521
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

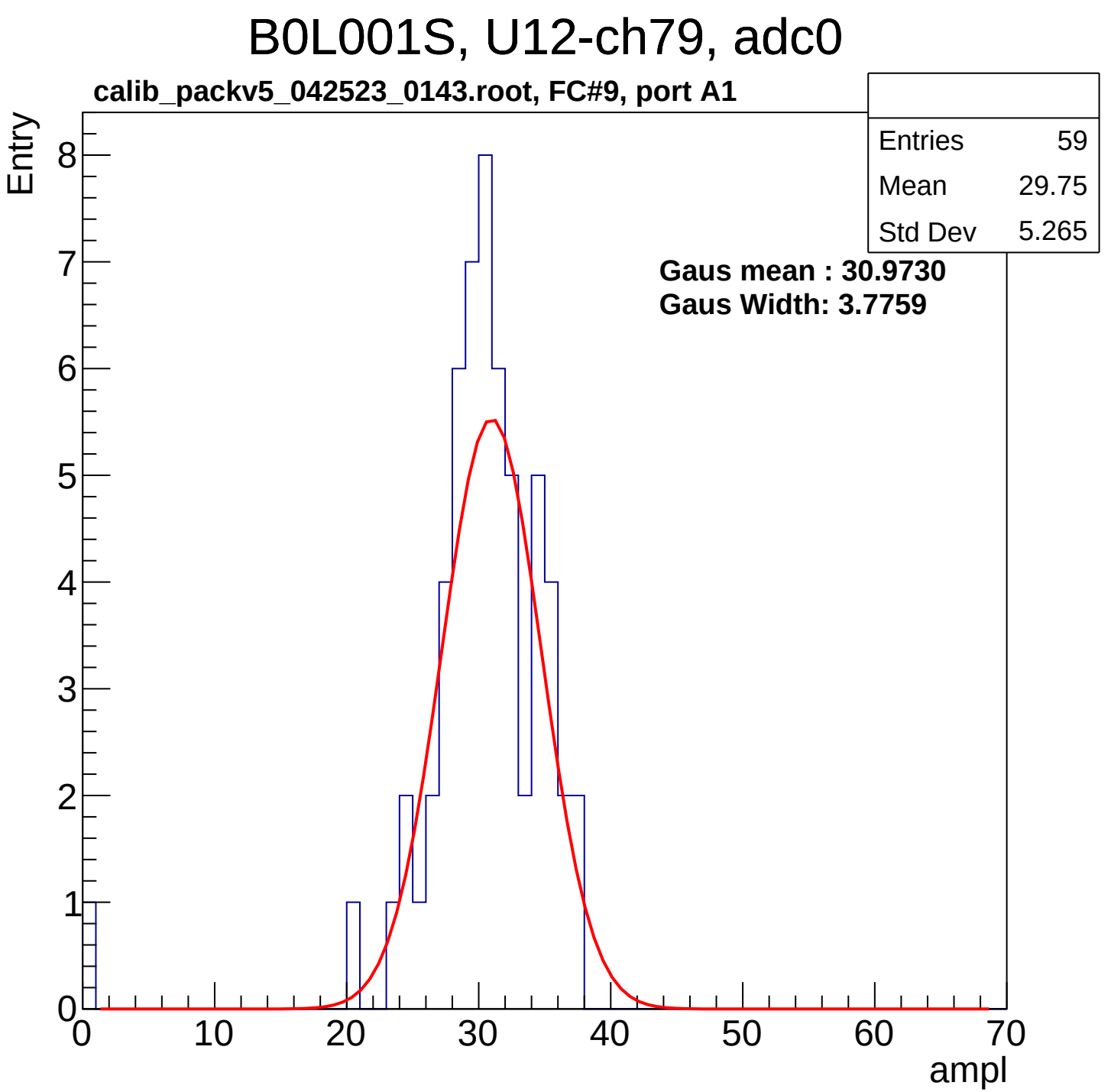

B0L001S, U12-ch78, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 50
Mean 51.46
Std Dev 3.054
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

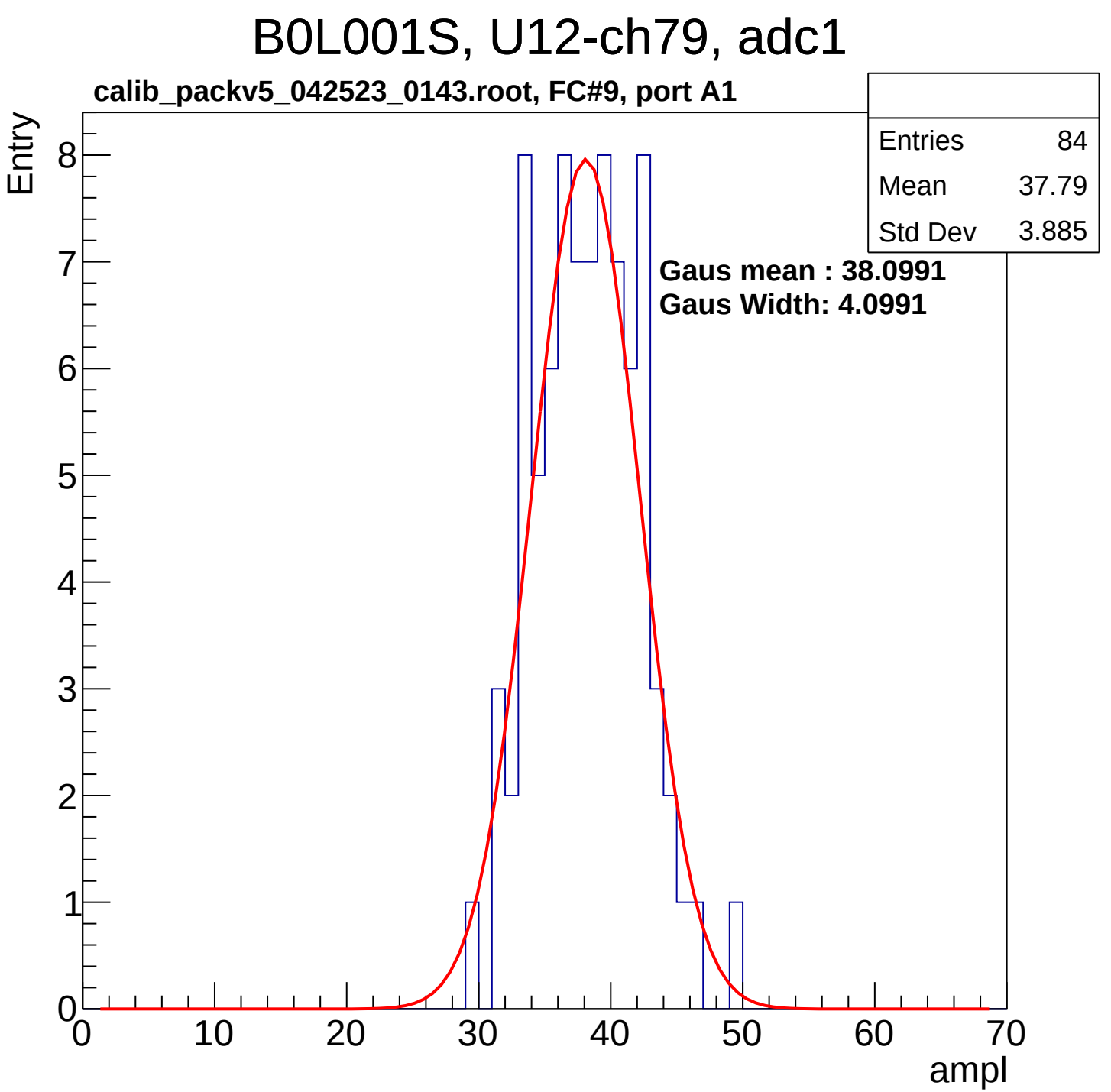

B0L001S, U12-ch78, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 63
Mean 56.08
Std Dev 7.945
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

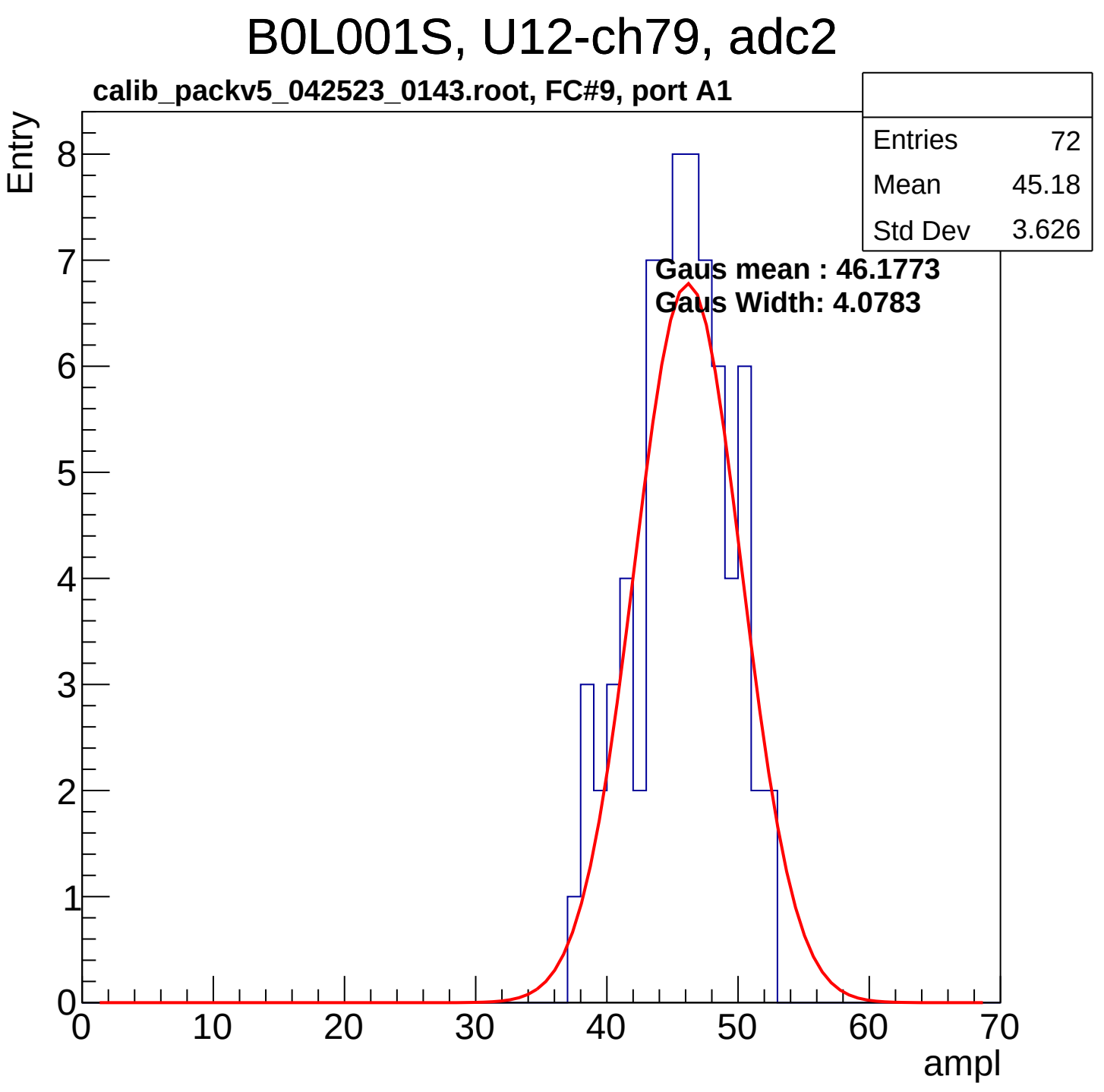

B0L001S, U12-ch78, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 30
Mean 60.33
Std Dev 1.776
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

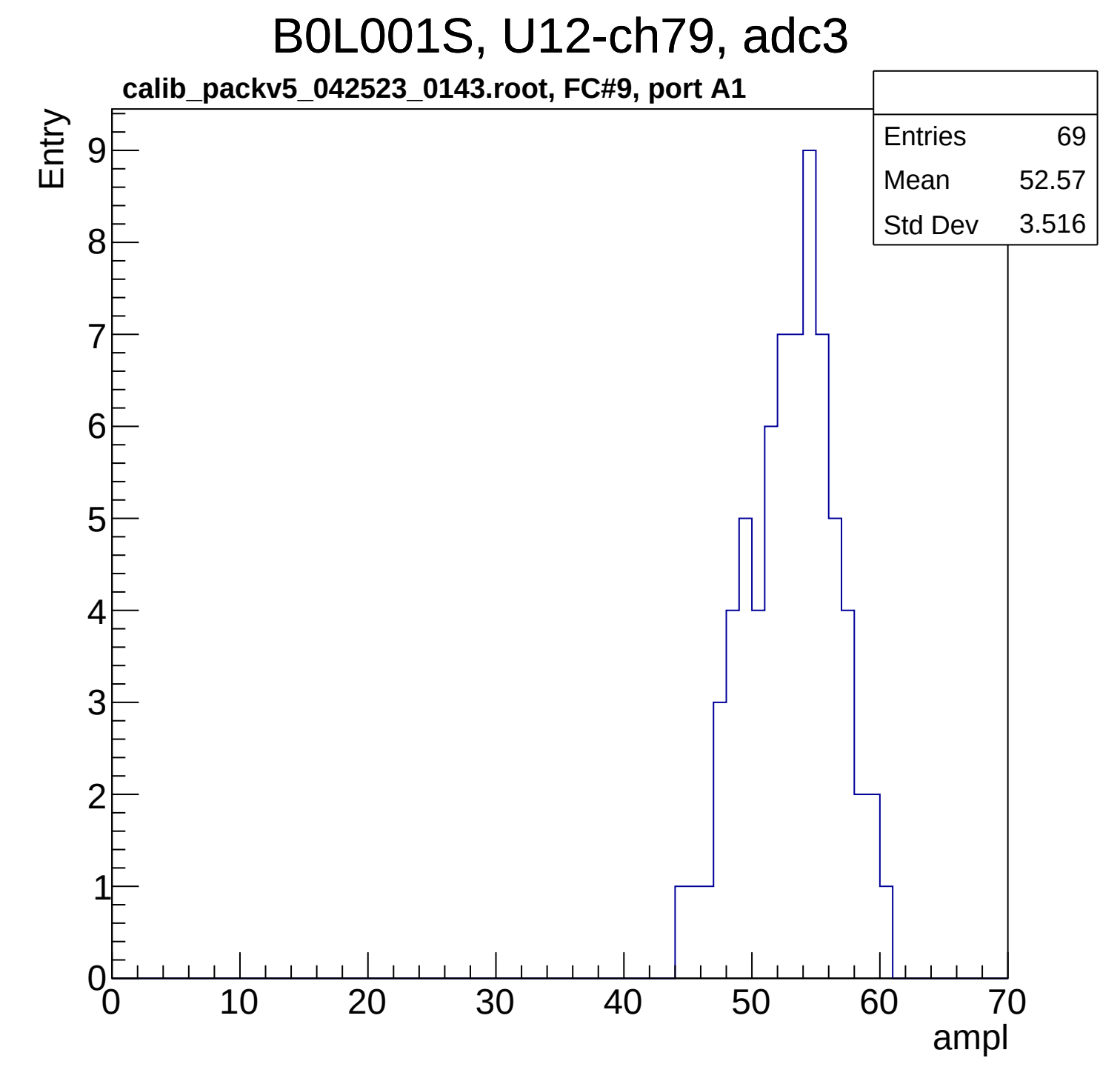

B0L001S, U12-ch78, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

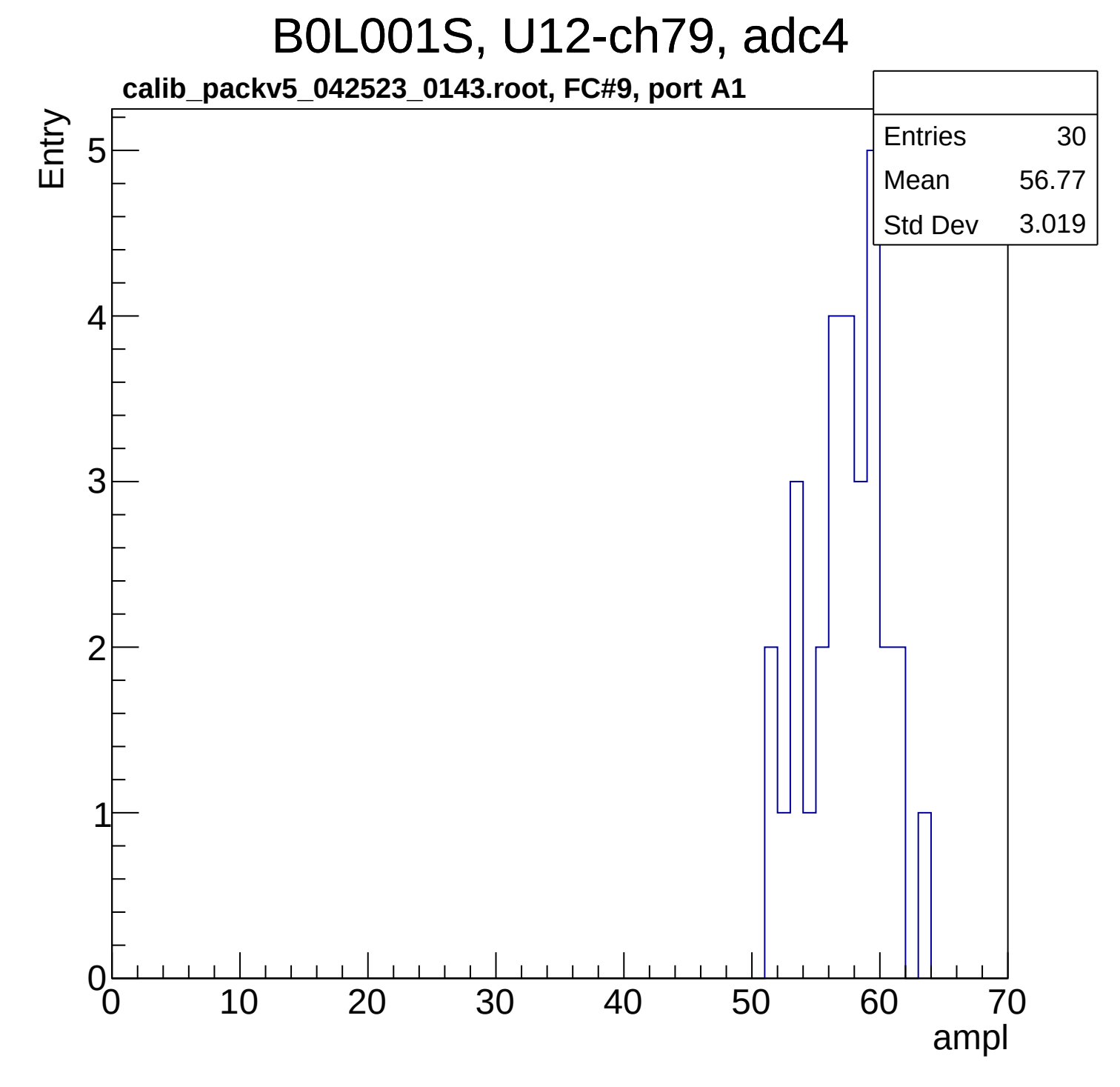

B0L001S, U12-ch78, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

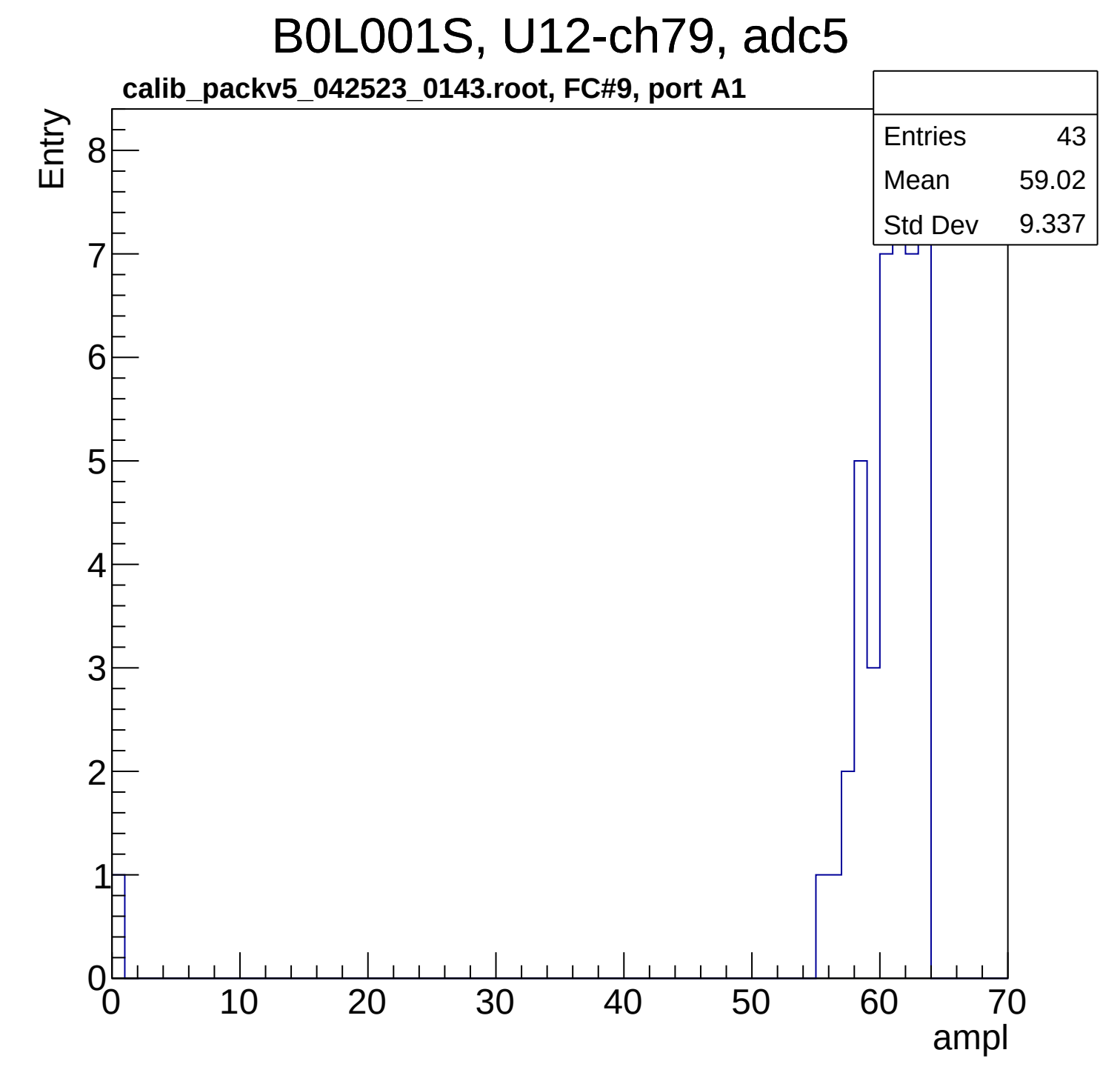

B0L001S, U12-ch79, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 59
Mean 29.75
Std Dev 5.265
Gaus mean : 30.9730
Gaus Width: 3.7759
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch79, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 84
Mean 37.79
Std Dev 3.885
Gaus mean : 38.0991
Gaus Width: 4.0991
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch79, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 72
Mean 45.18
Std Dev 3.626
Gaus mean : 46.1773
Gaus Width: 4.0783
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch79, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 69
Mean 52.57
Std Dev 3.516
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch79, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 30
Mean 56.77
Std Dev 3.019
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L001S, U12-ch79, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 43
Mean 59.02
Std Dev 9.337
Entry
ampl
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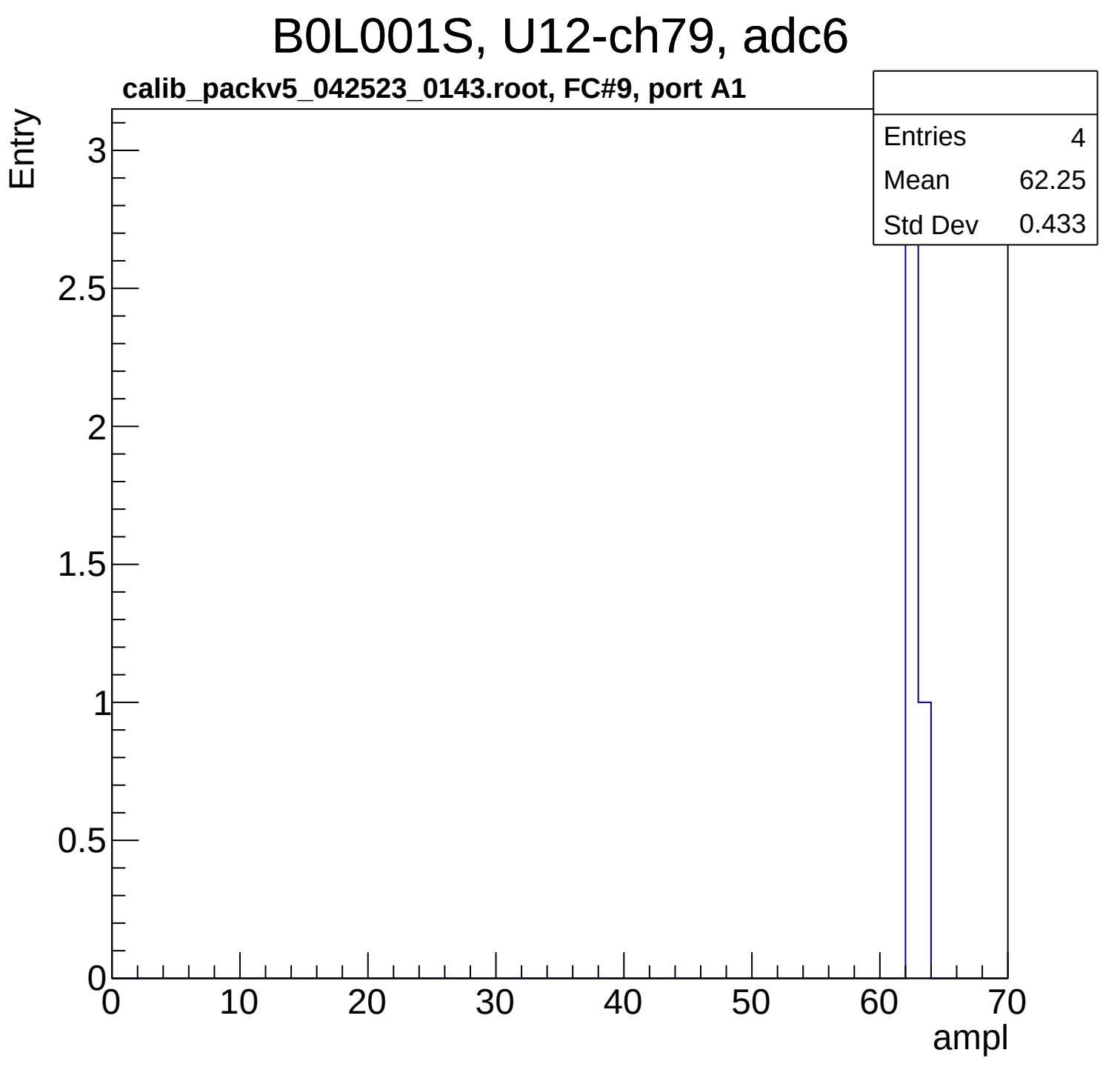
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch79, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 4
Mean 62.25
Std Dev 0.433
Entry
ampl
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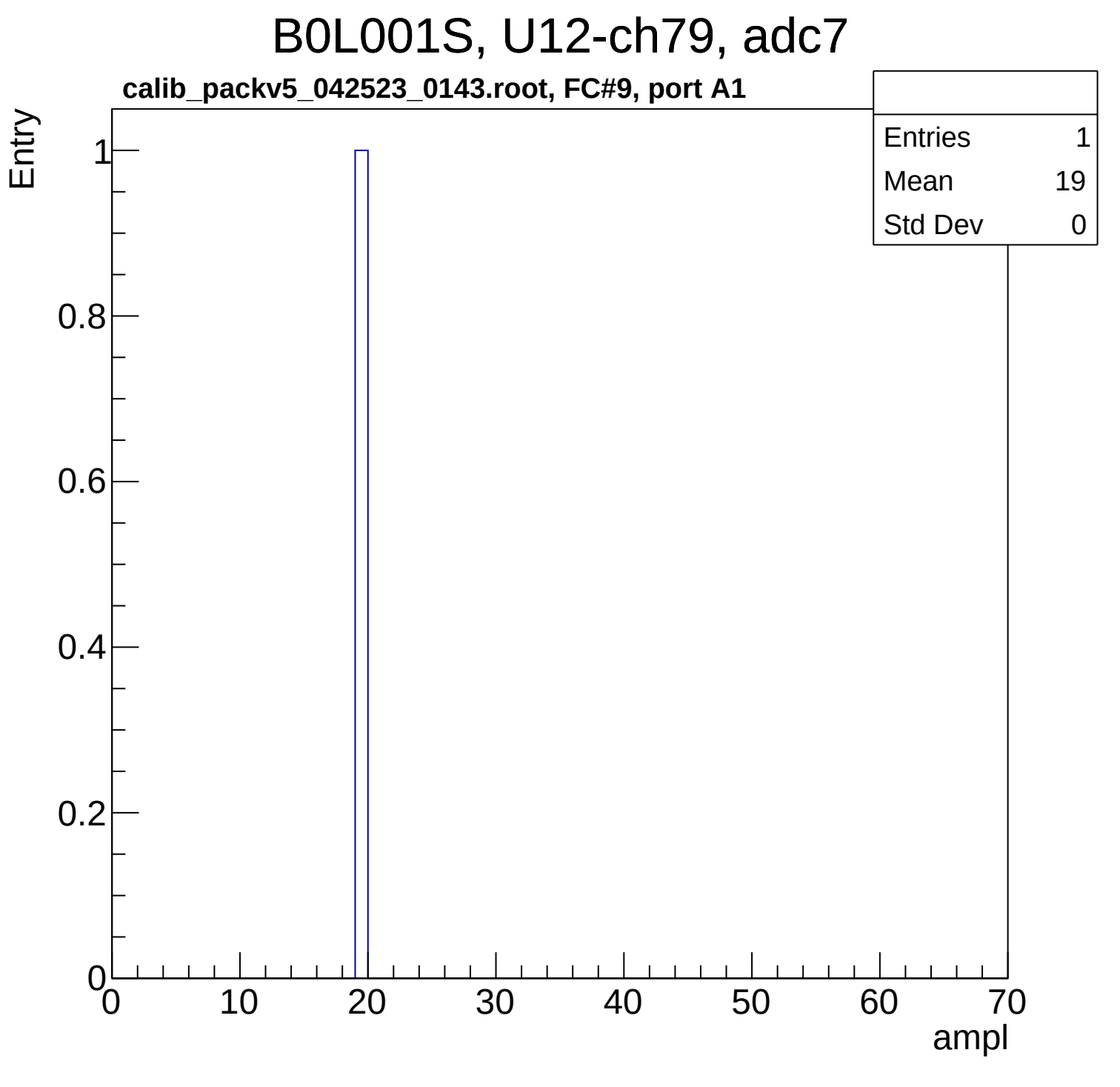
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B0L001S, U12-ch79, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 19
Std Dev 0
Entry
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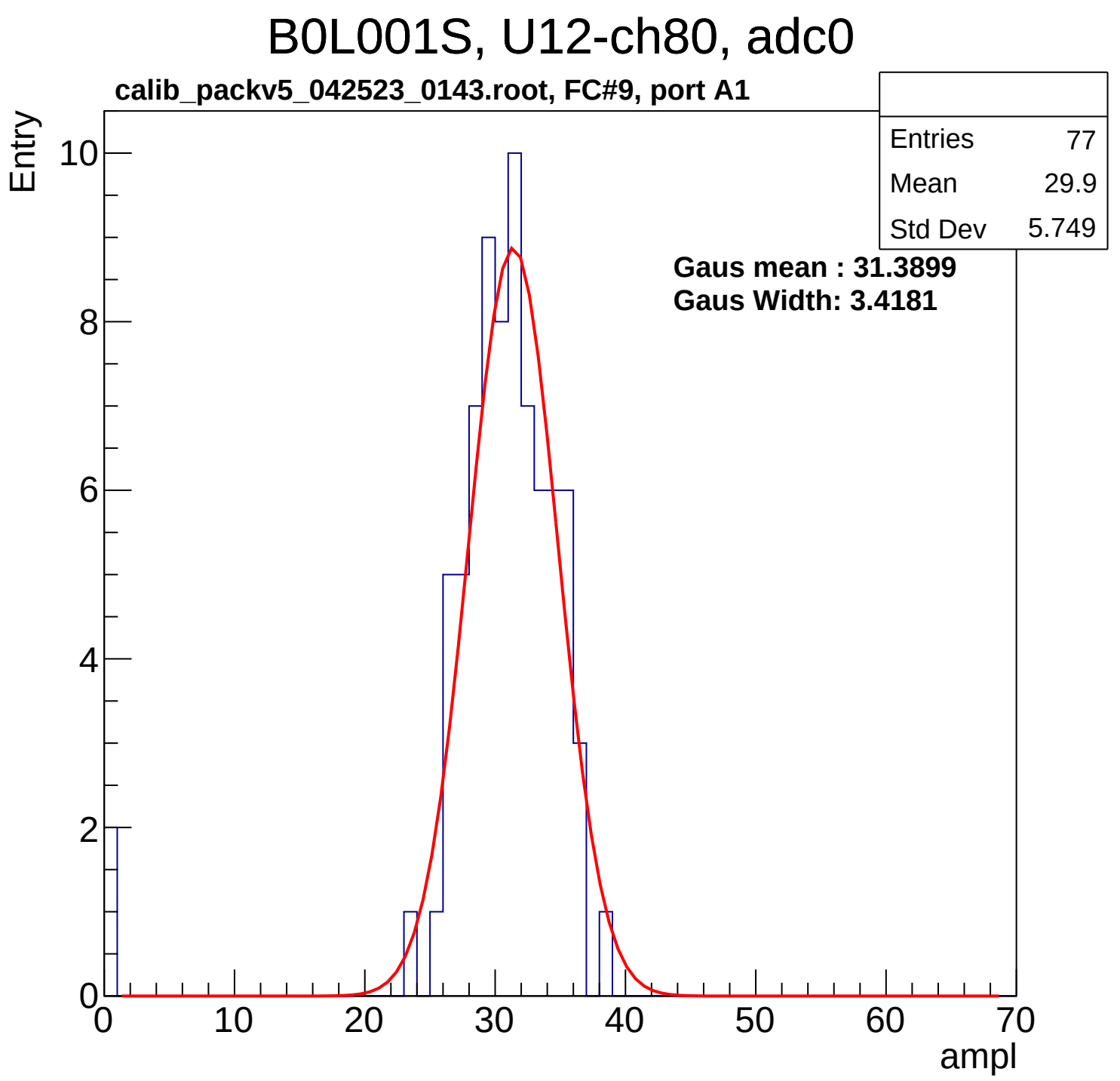
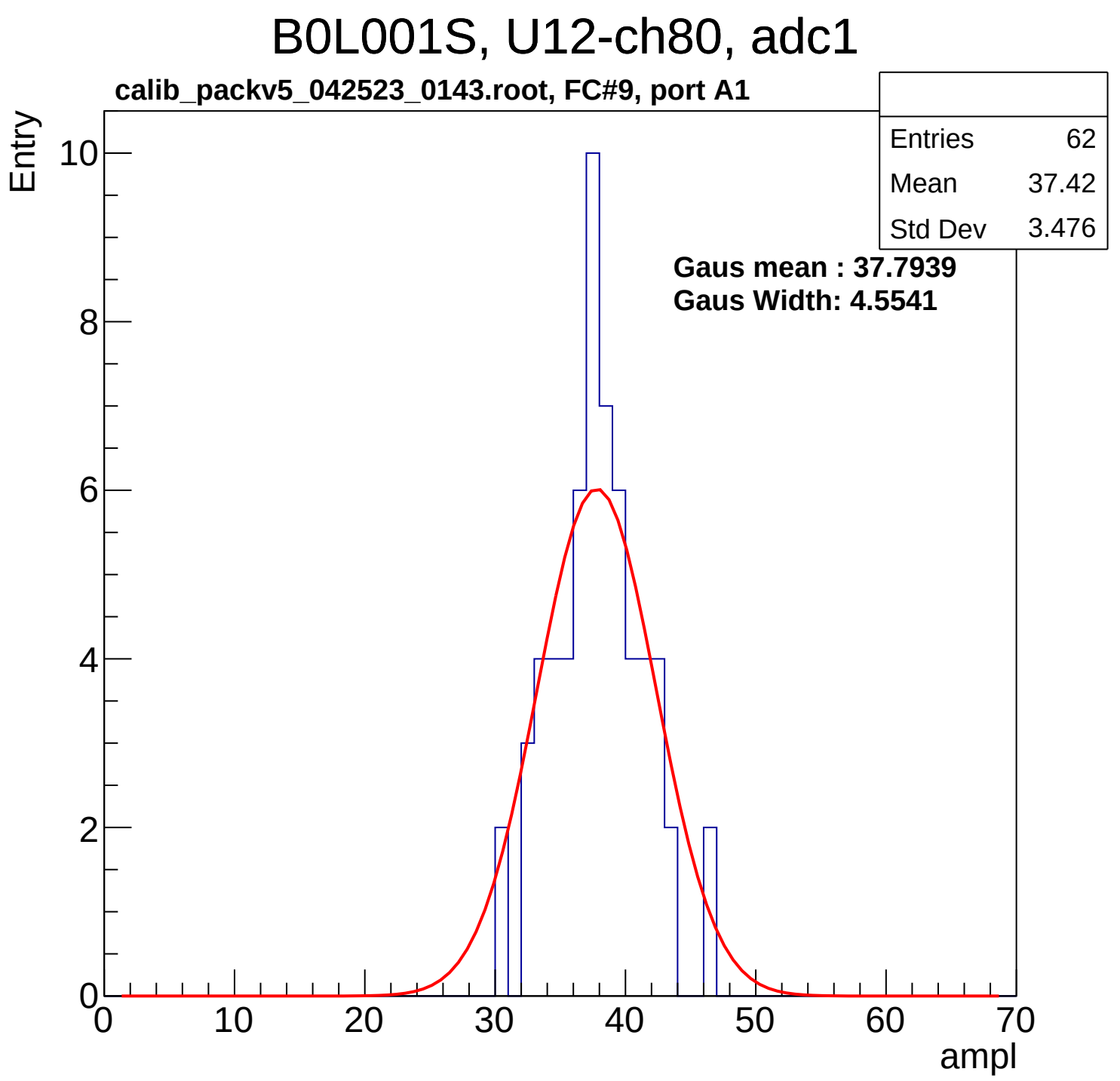
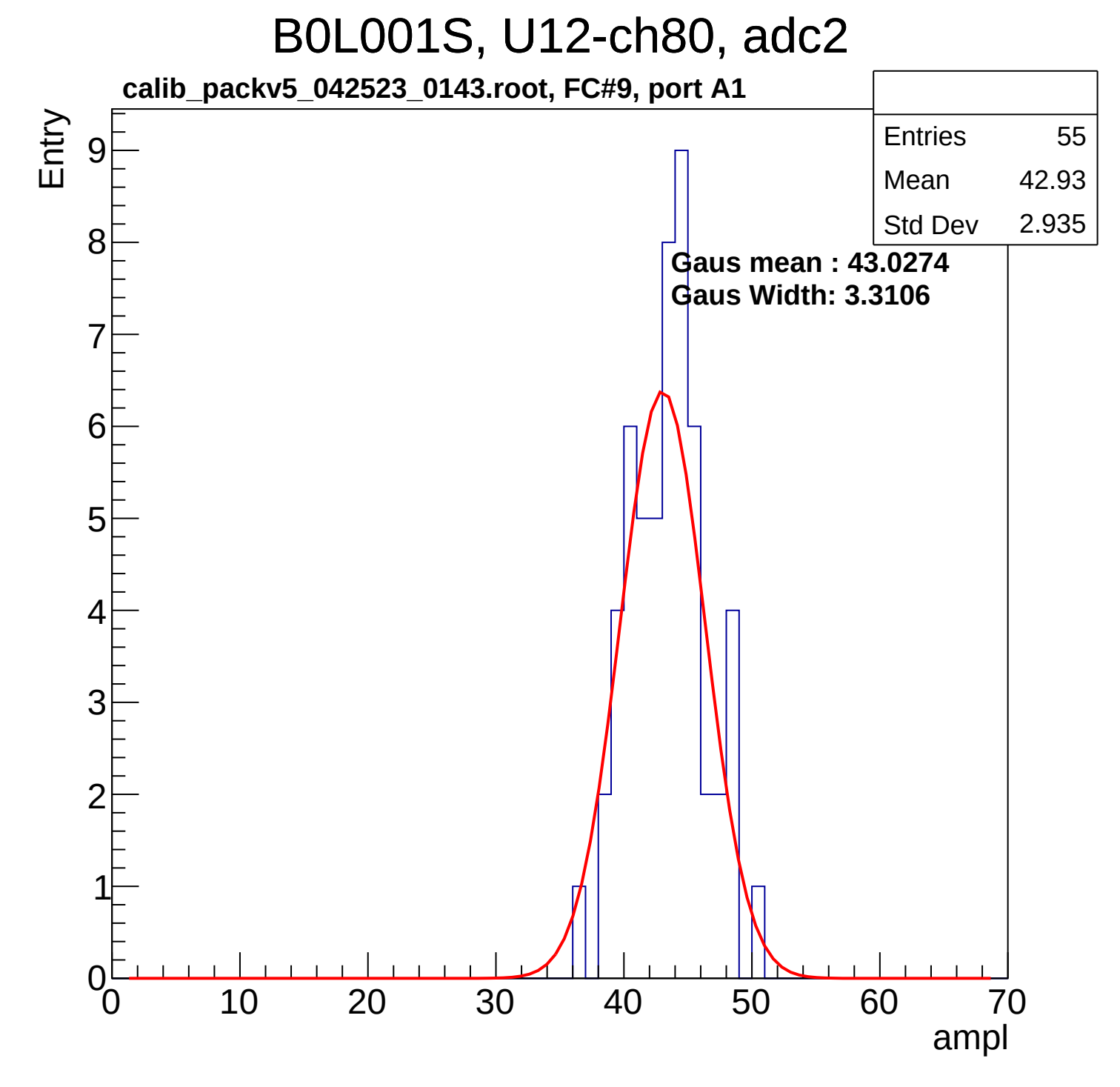
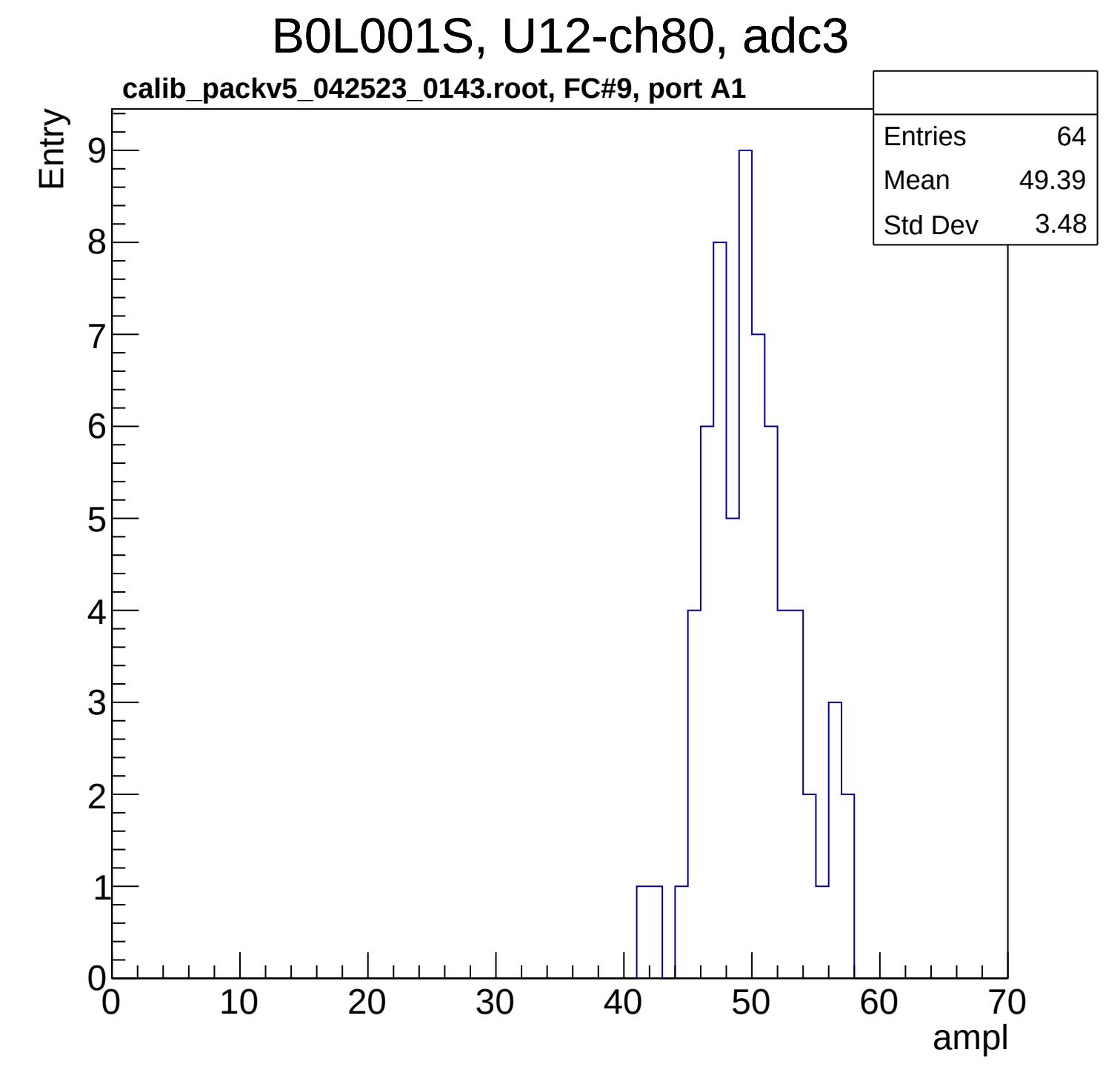
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch80, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 77
Mean 29.9
Std Dev 5.749
Gaus mean : 31.3899
Gaus Width: 3.4181
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch80, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 62
Mean 37.42
Std Dev 3.476
Gaus mean : 37.7939
Gaus Width: 4.5541
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch80, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 55
Mean 42.93
Std Dev 2.935
Gaus mean : 43.0274
Gaus Width: 3.3106
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch80, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 64
Mean 49.39
Std Dev 3.48
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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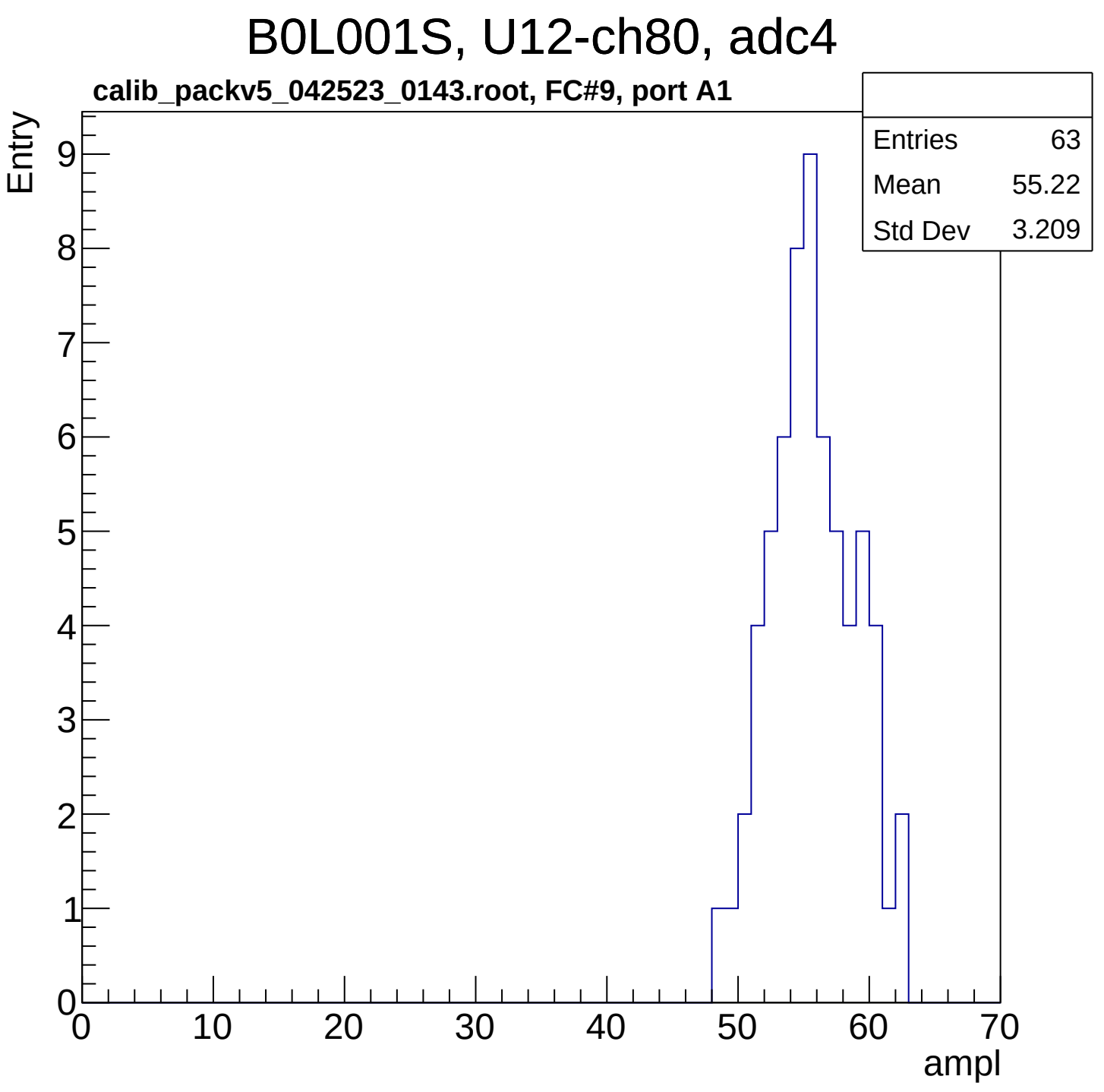
40
50
60
70


B0L001S, U12-ch80, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 63
Mean 55.22
Std Dev 3.209
Entry
ampl
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1
2
3
4
5
6
7
8
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0
10
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40
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60
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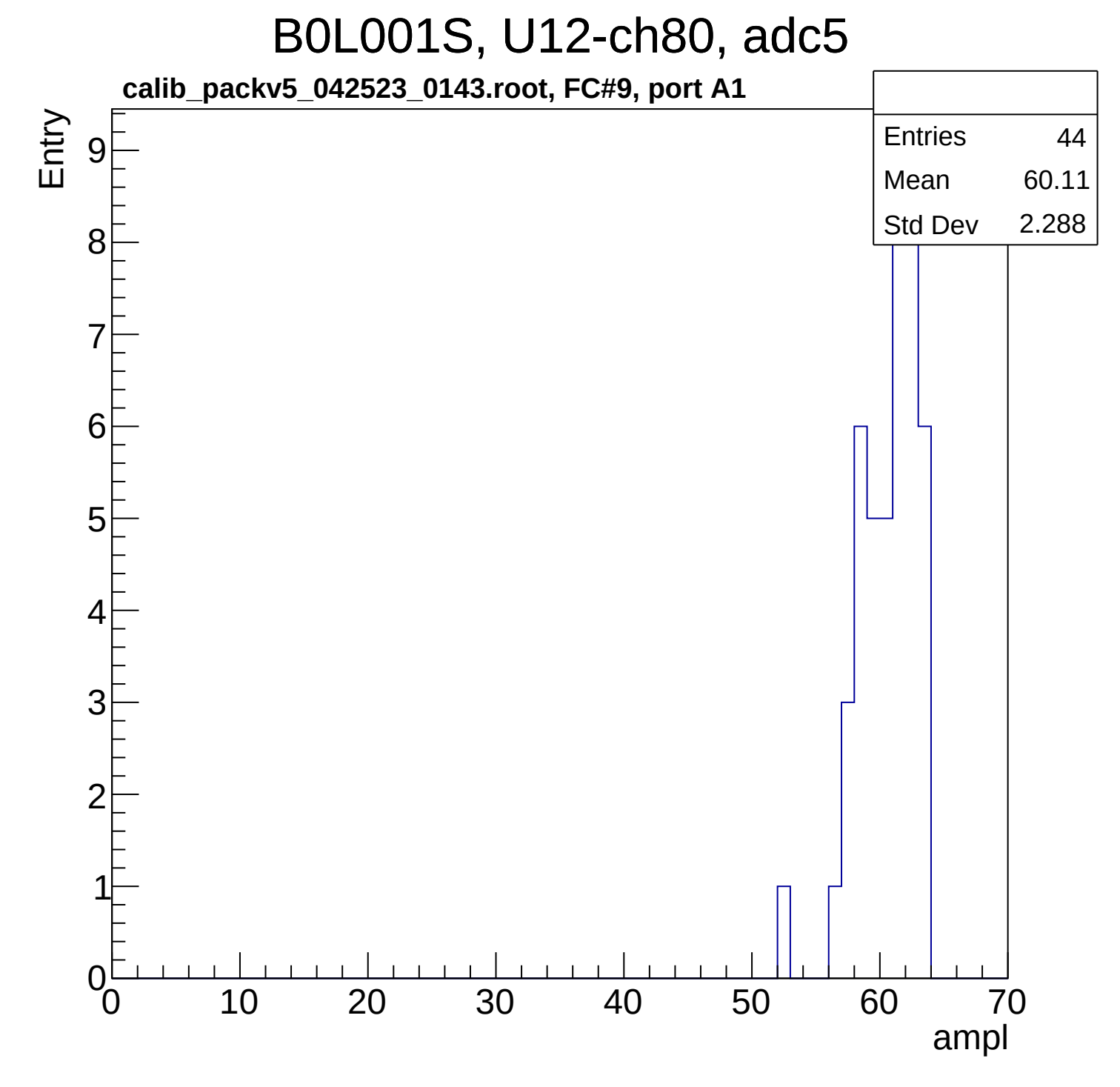
B0L001S, U12-ch80, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 44
Mean 60.11
Std Dev 2.288
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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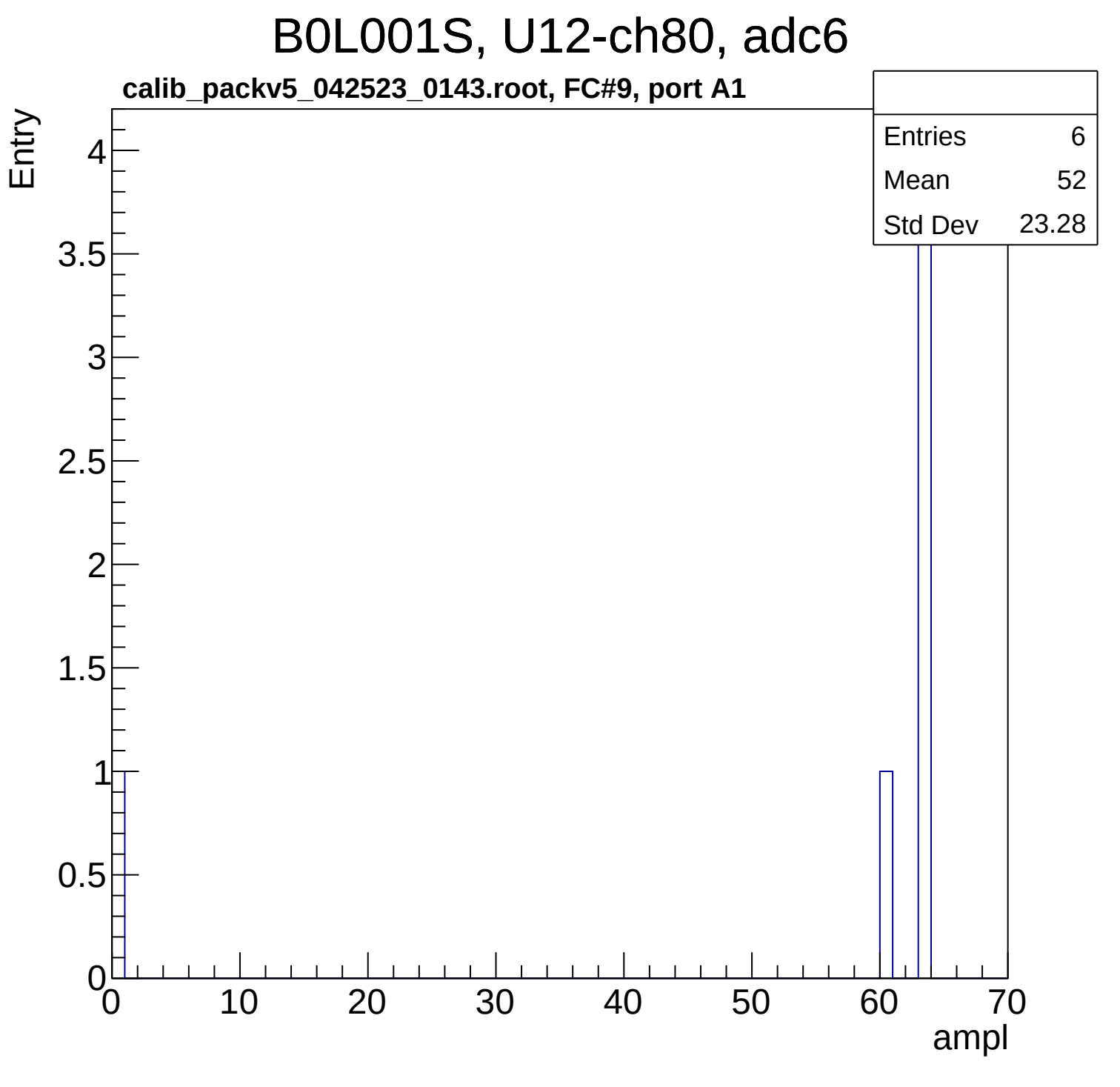
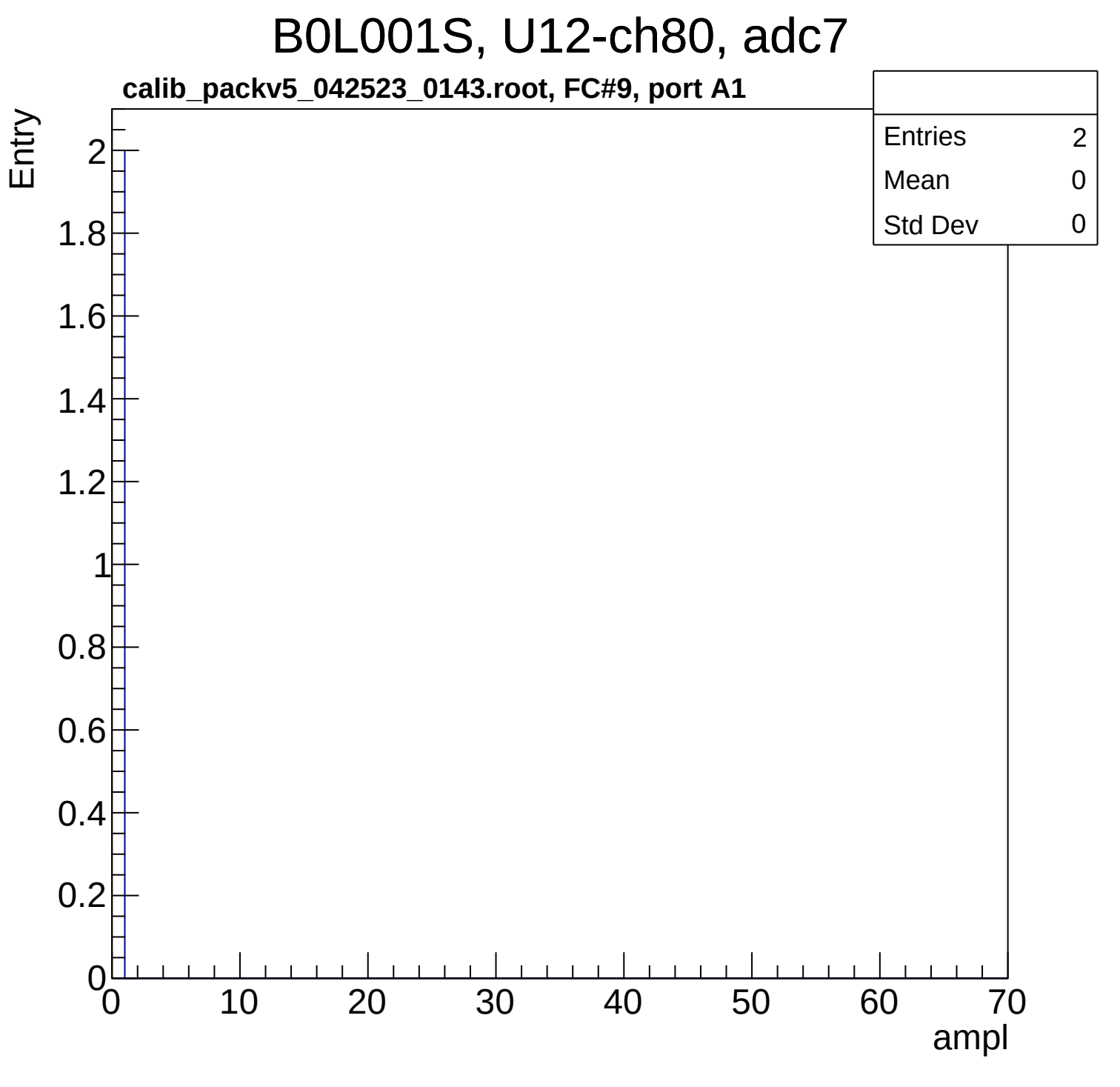

B0L001S, U12-ch80, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 6
Mean 52
Std Dev 23.28
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B0L001S, U12-ch80, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
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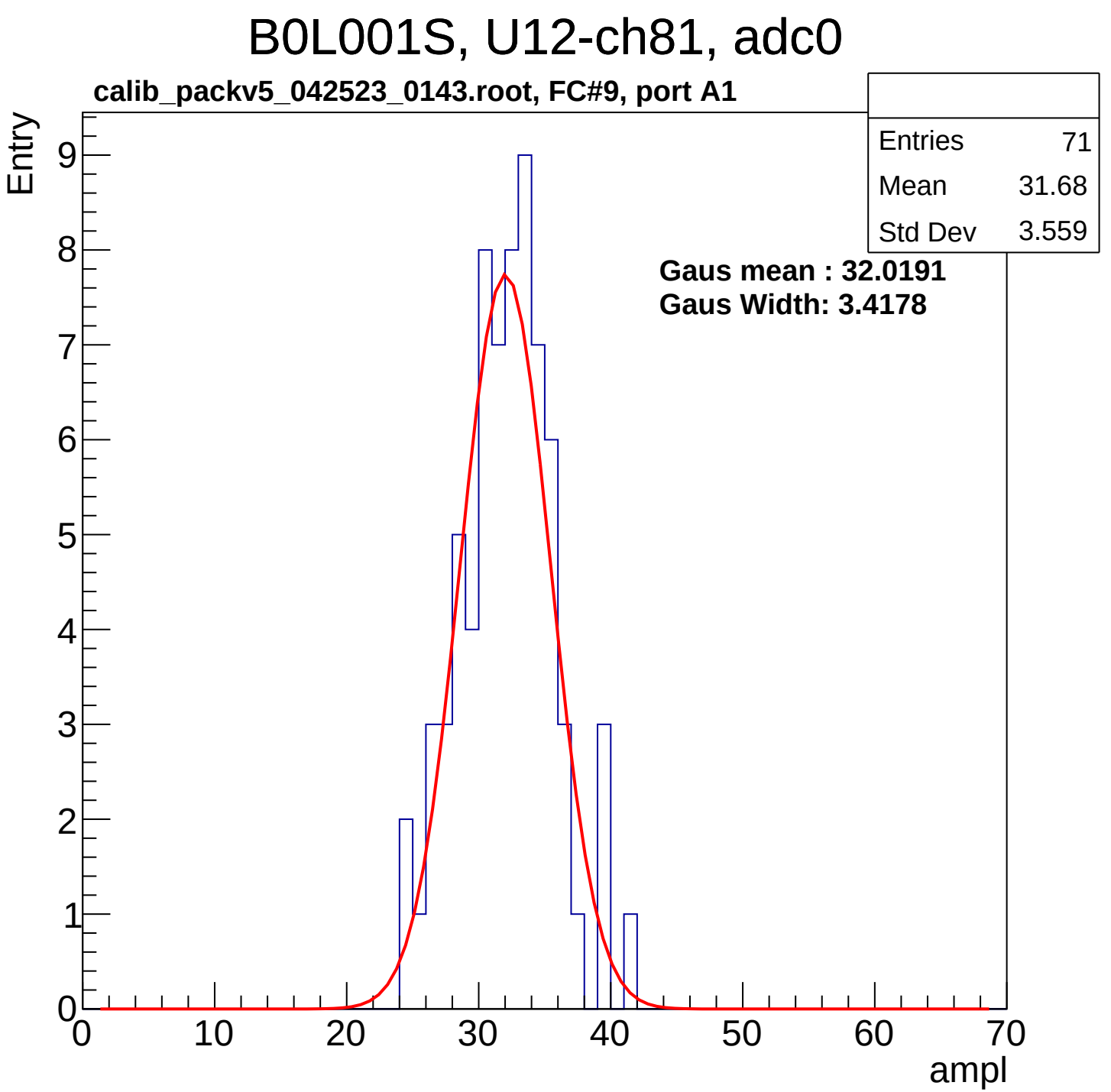
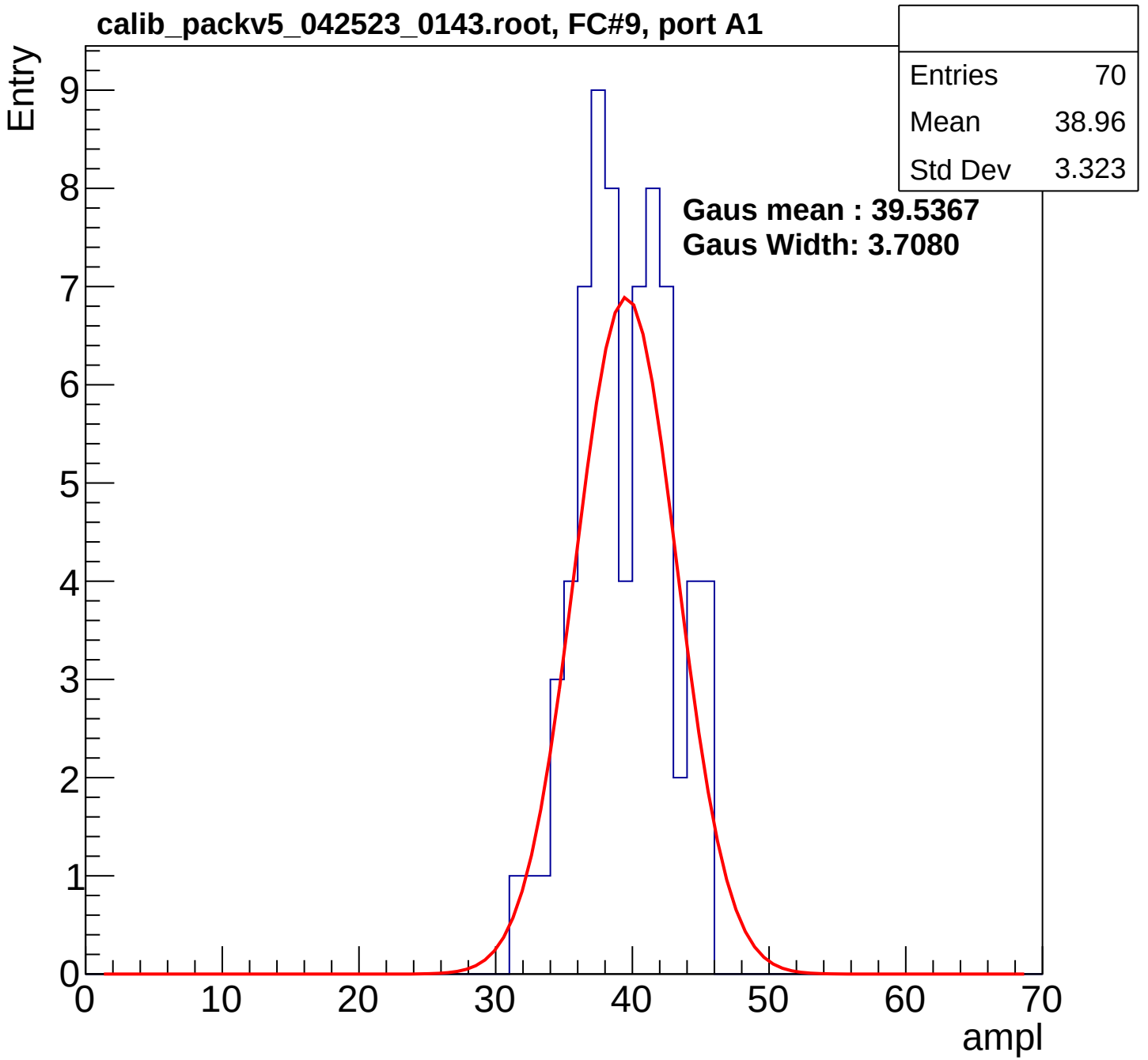
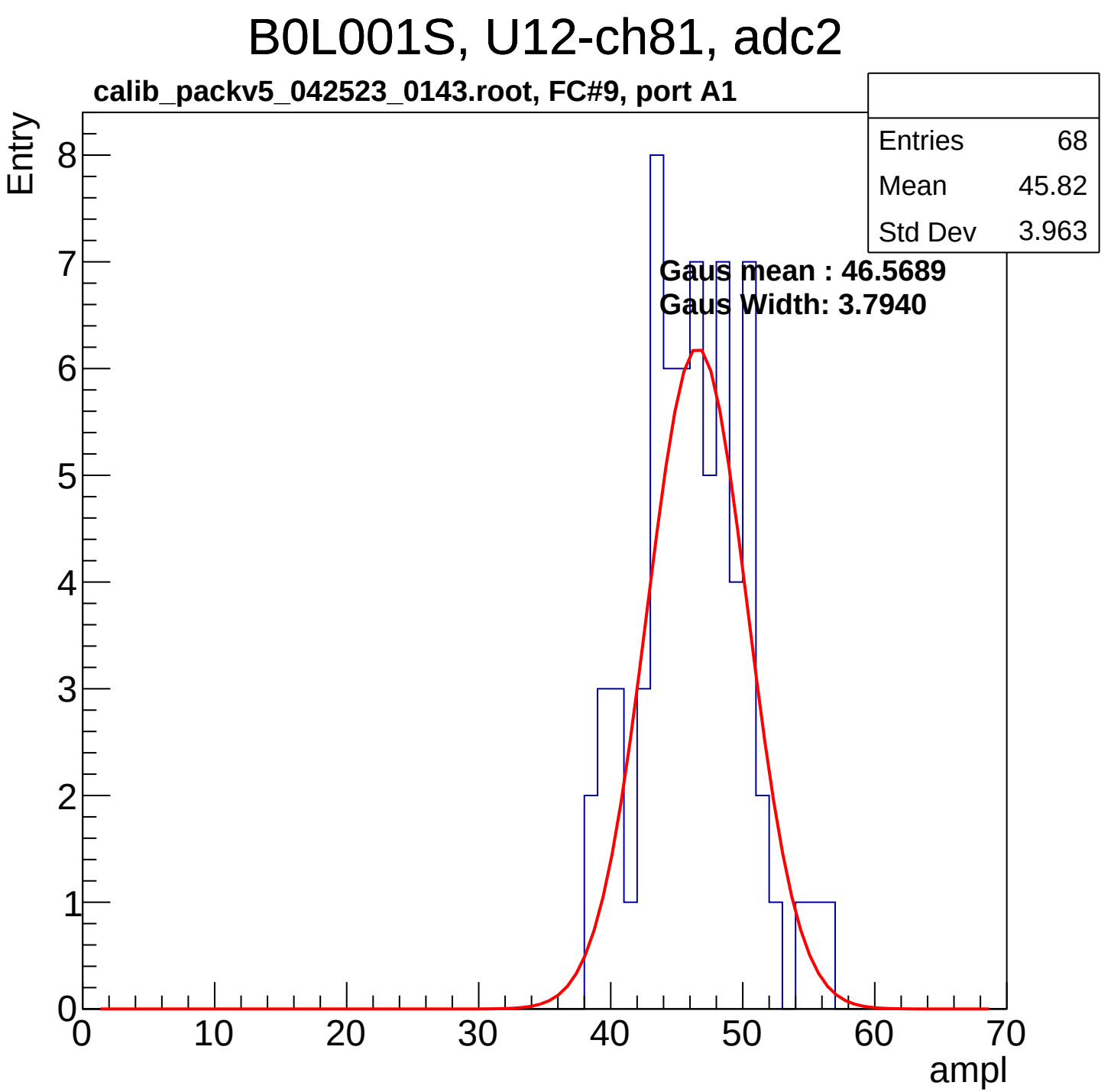
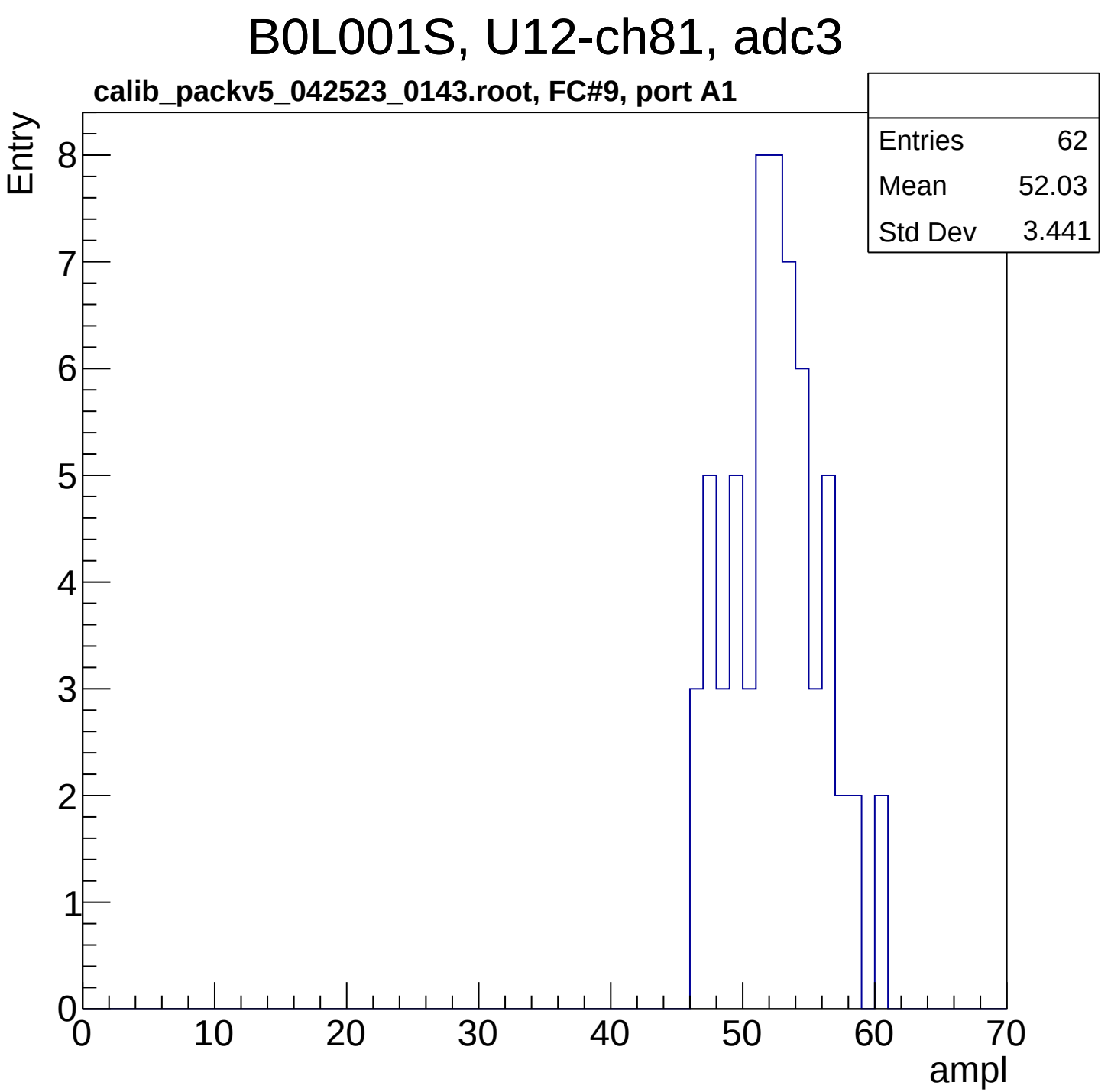
30
40
50
60
70
ampl


B0L001S, U12-ch81, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 71
Mean 31.68
Std Dev 3.559
Gaus mean : 32.0191
Gaus Width: 3.4178
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch81, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 70
Mean 38.96
Std Dev 3.323
Gaus mean : 39.5367
Gaus Width: 3.7080
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch81, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 68
Mean 45.82
Std Dev 3.963
Gaus mean : 46.5689
Gaus Width: 3.7940
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch81, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 62
Mean 52.03
Std Dev 3.441
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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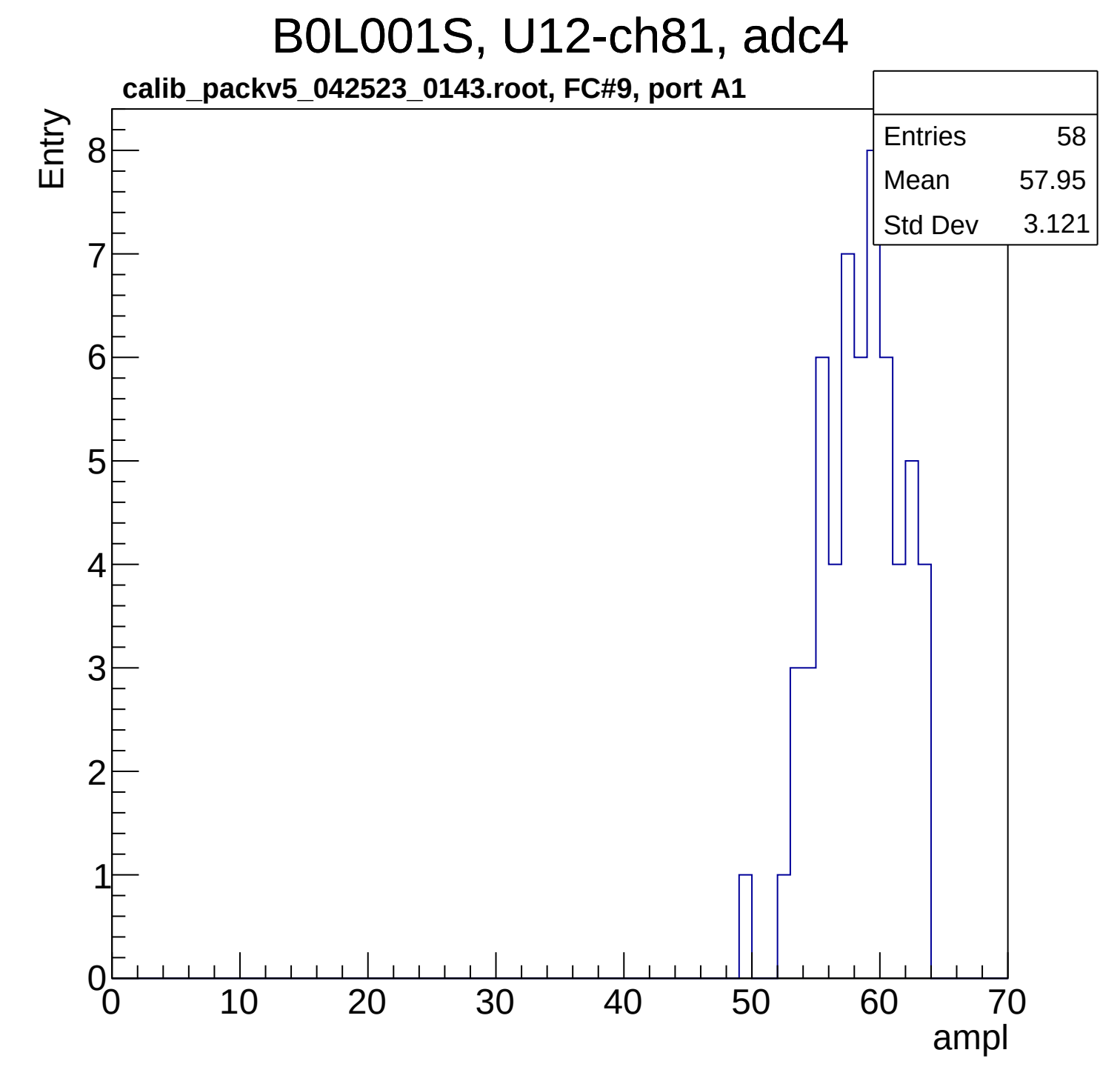
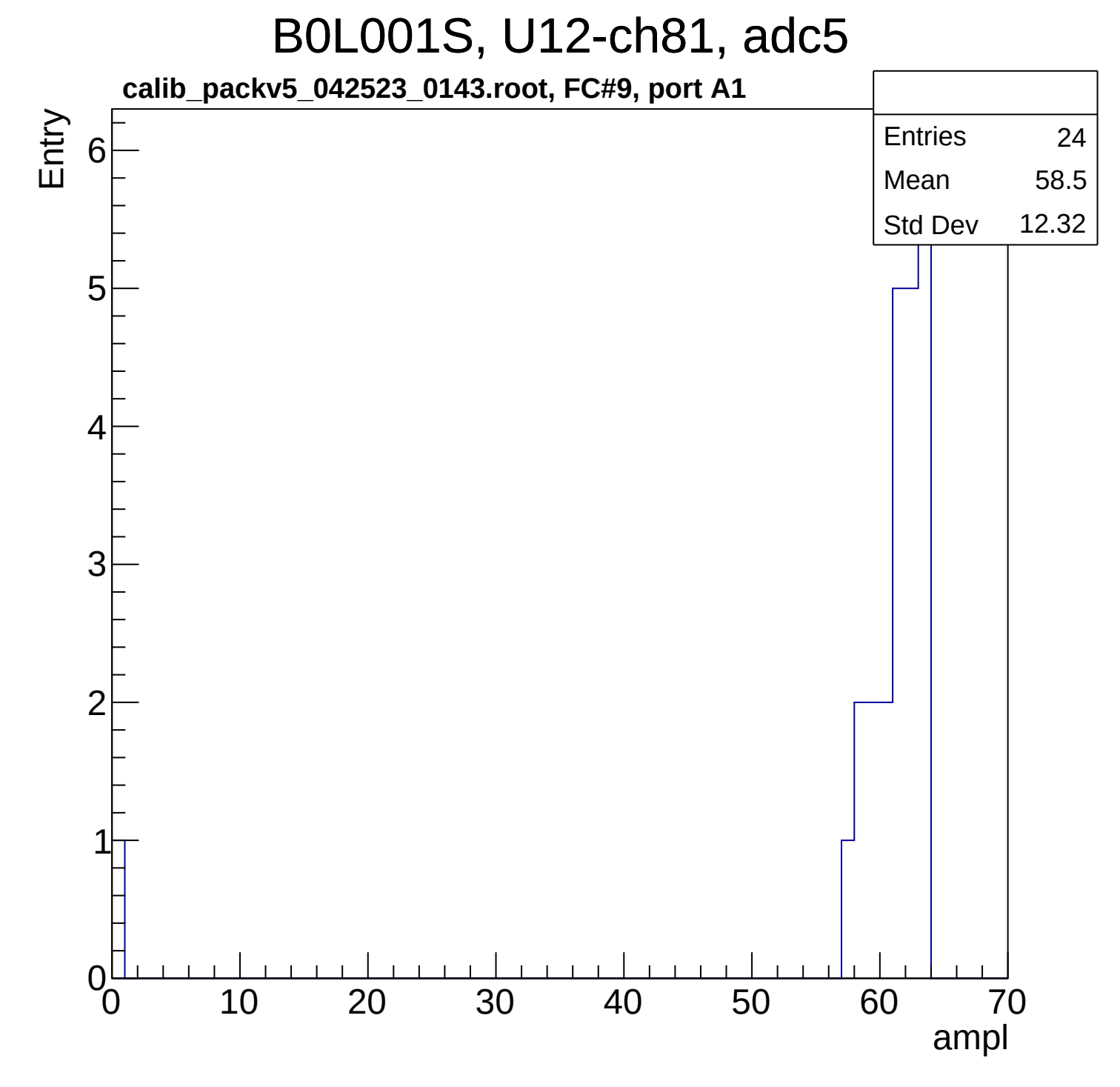
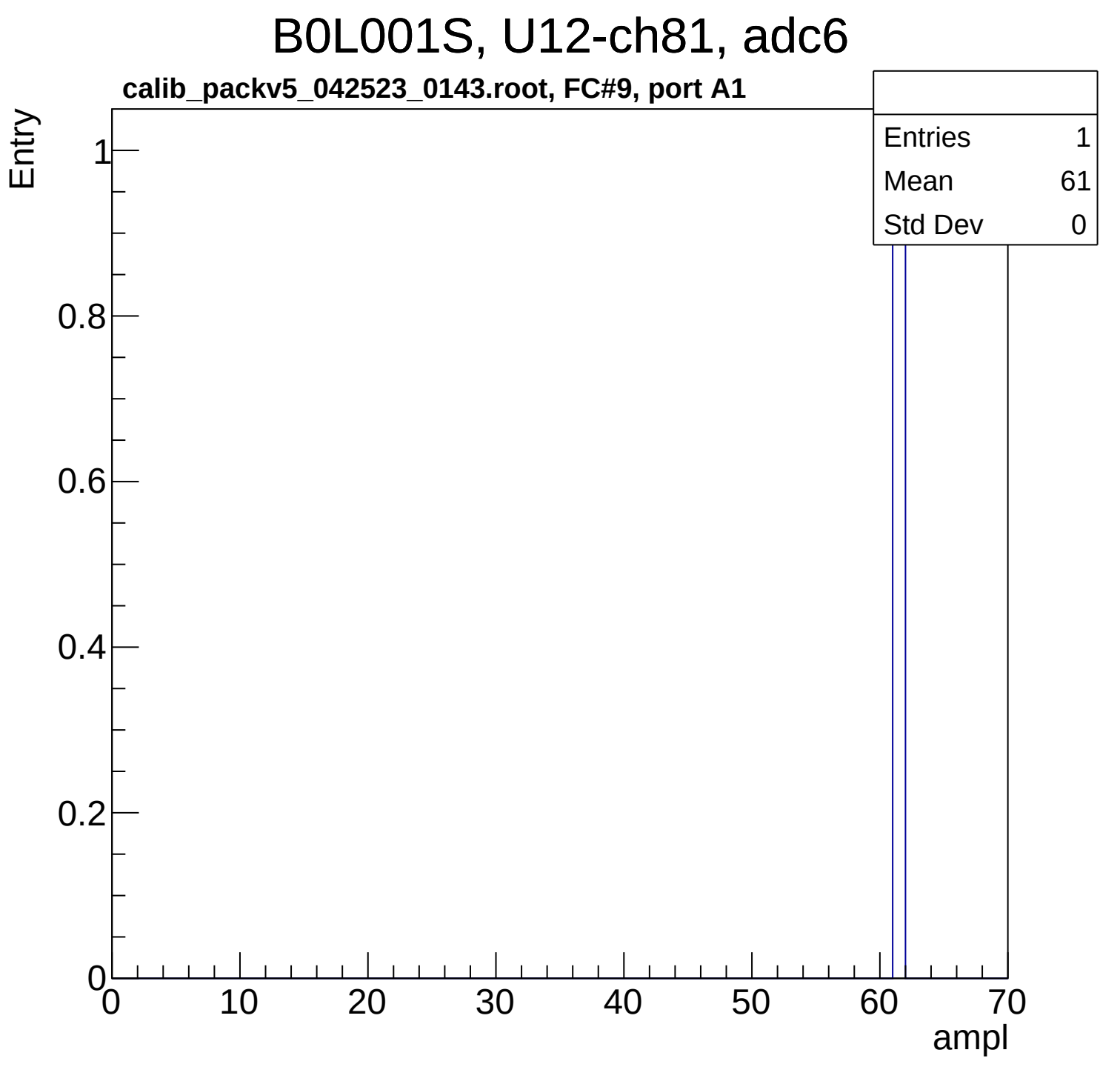
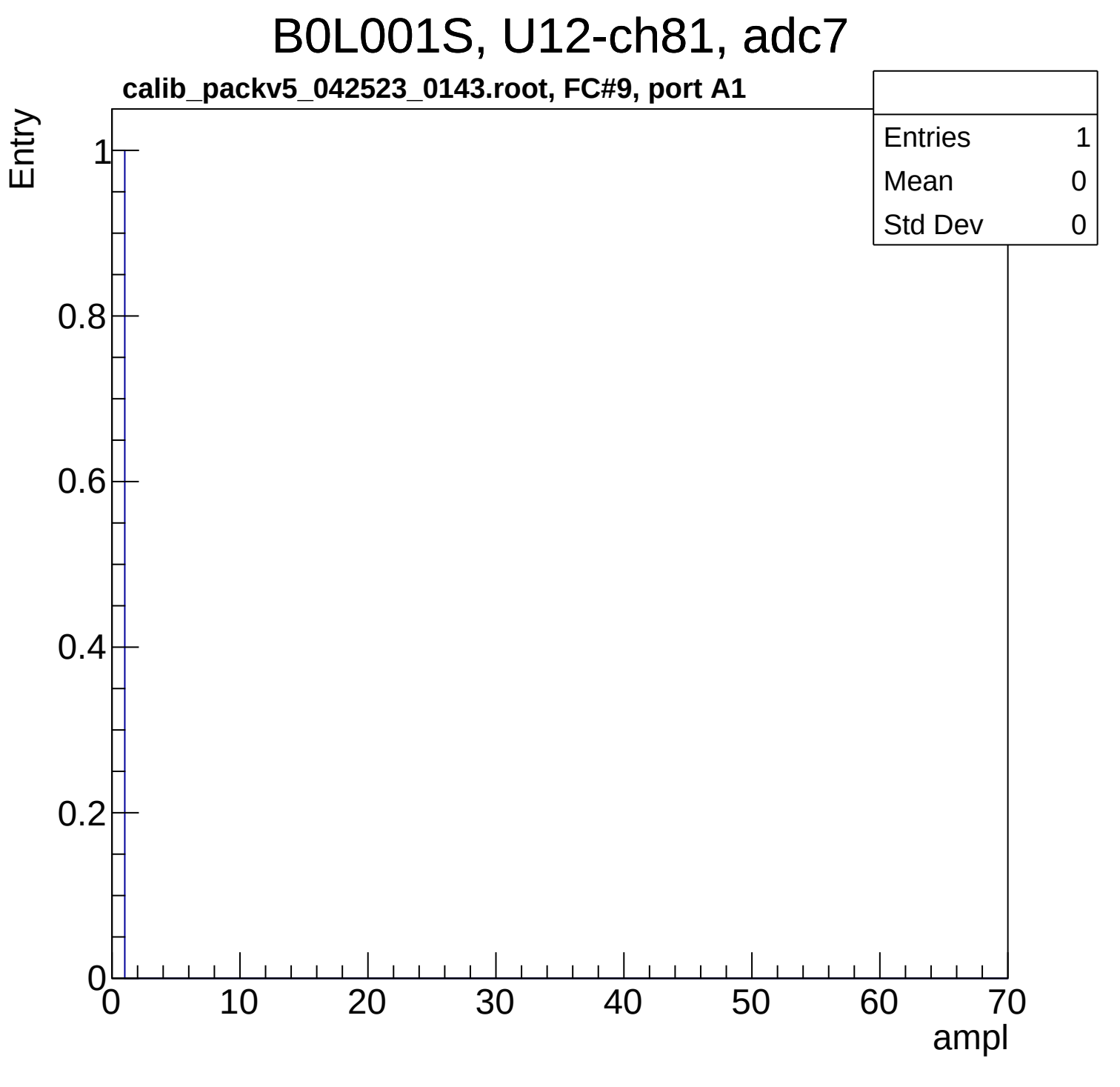
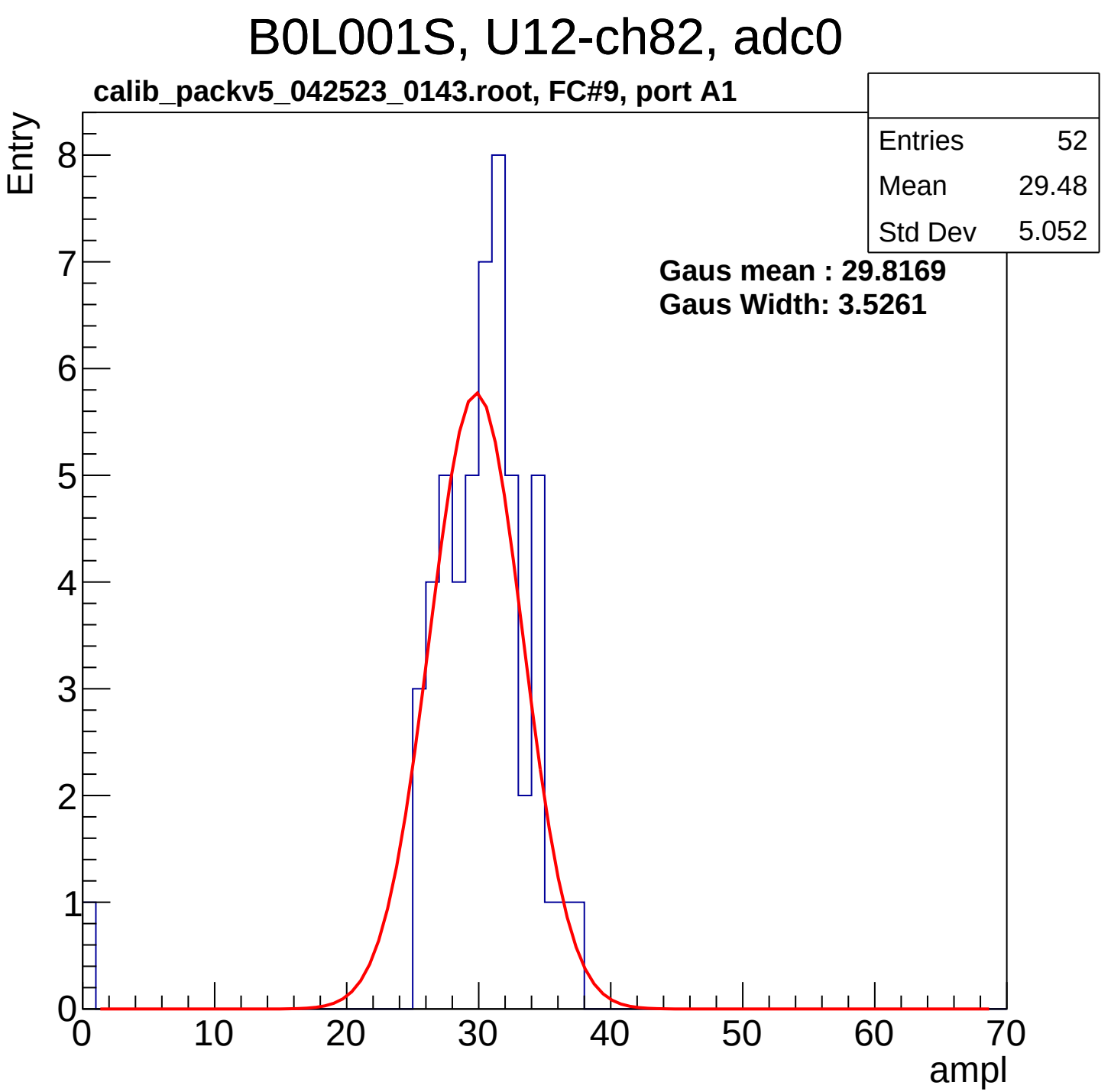
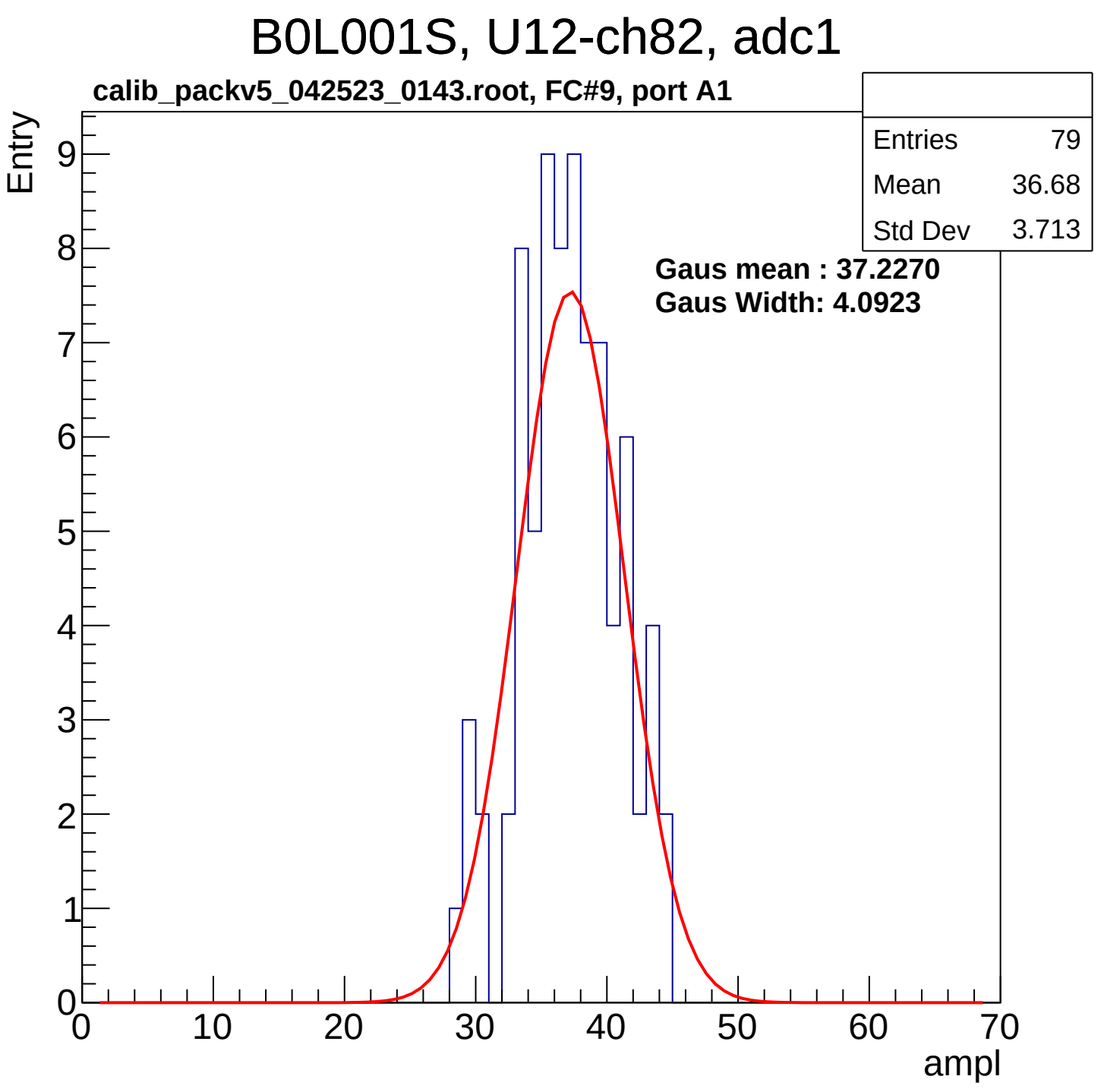

B0L001S, U12-ch81, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 58
Mean 57.95
Std Dev 3.121
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

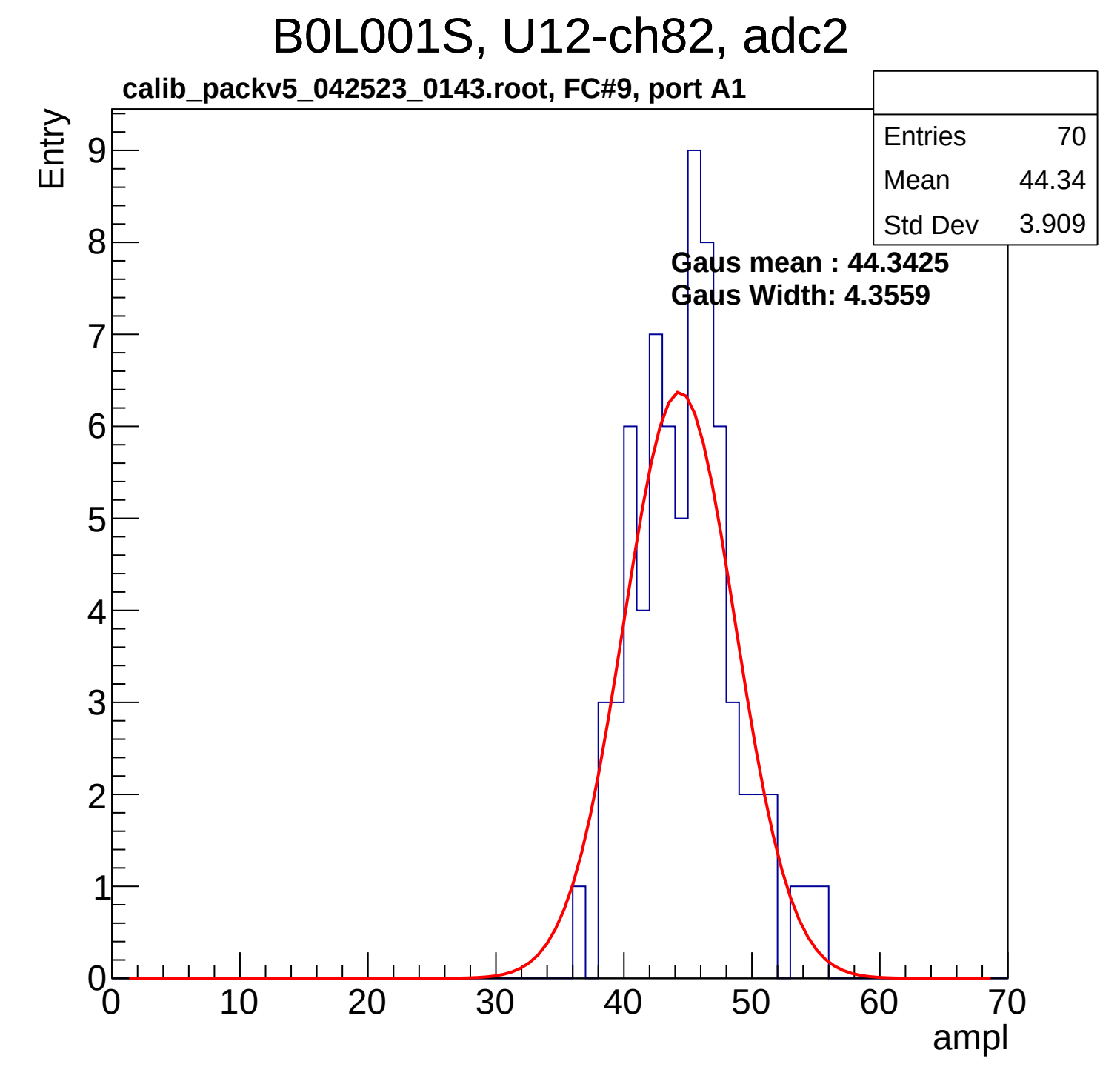

B0L001S, U12-ch81, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 24
Mean 58.5
Std Dev 12.32
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch81, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 61
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch81, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch82, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 52
Mean 29.48
Std Dev 5.052
Gaus mean : 29.8169
Gaus Width: 3.5261
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch82, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 79
Mean 36.68
Std Dev 3.713
Gaus mean : 37.2270
Gaus Width: 4.0923
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch82, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 70
Mean 44.34
Std Dev 3.909
Gaus mean : 44.3425
Gaus Width: 4.3559
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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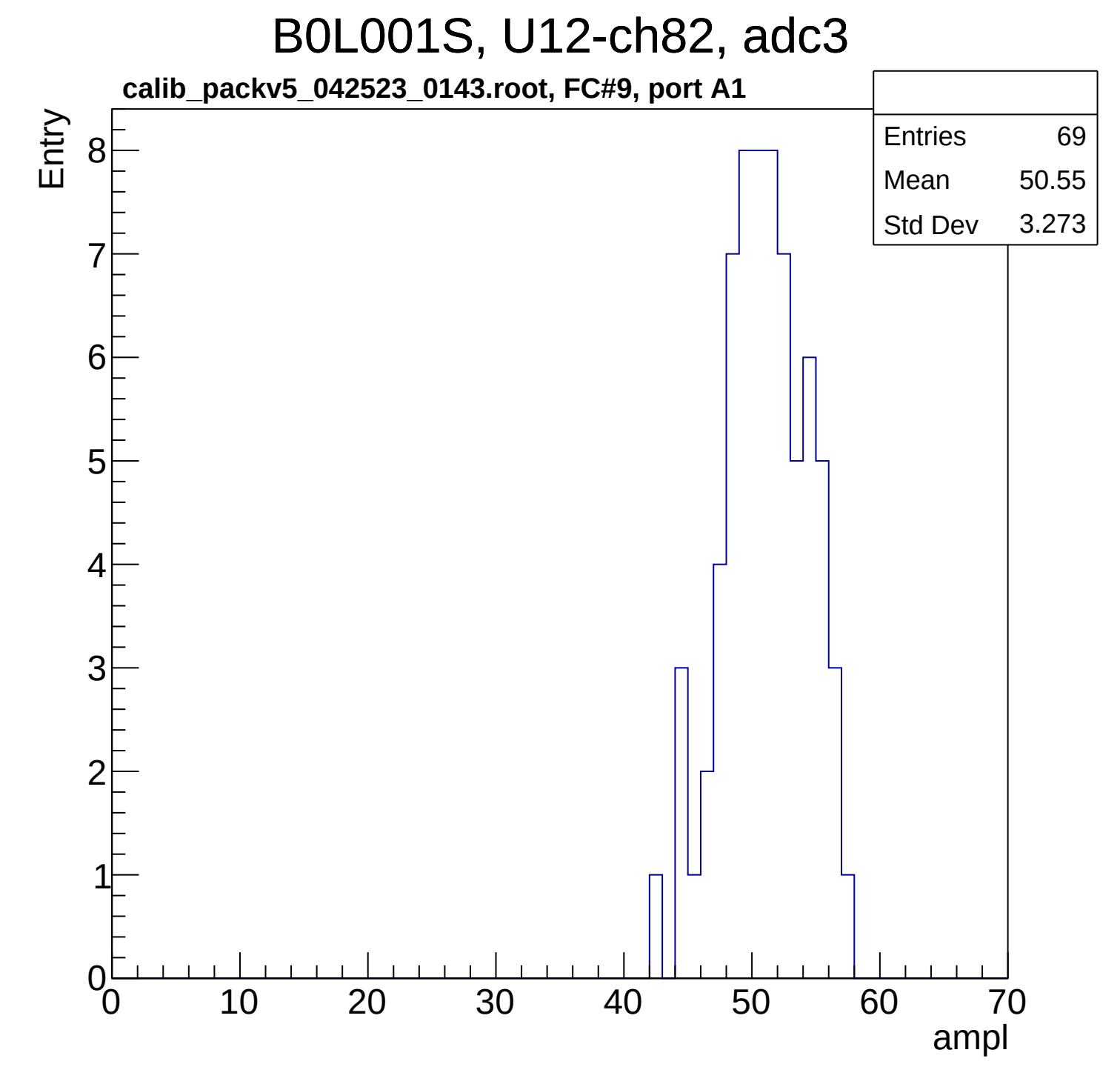
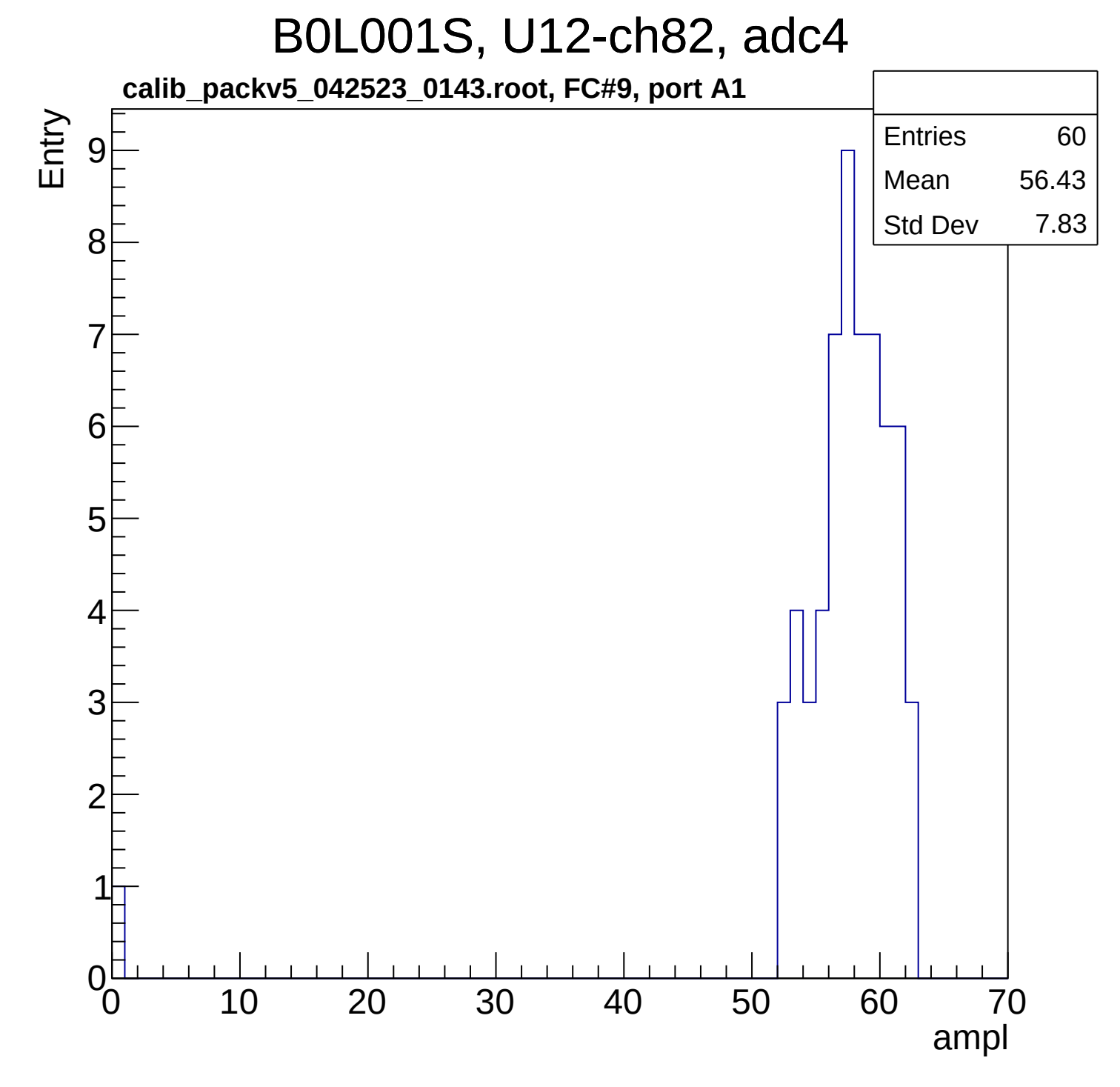
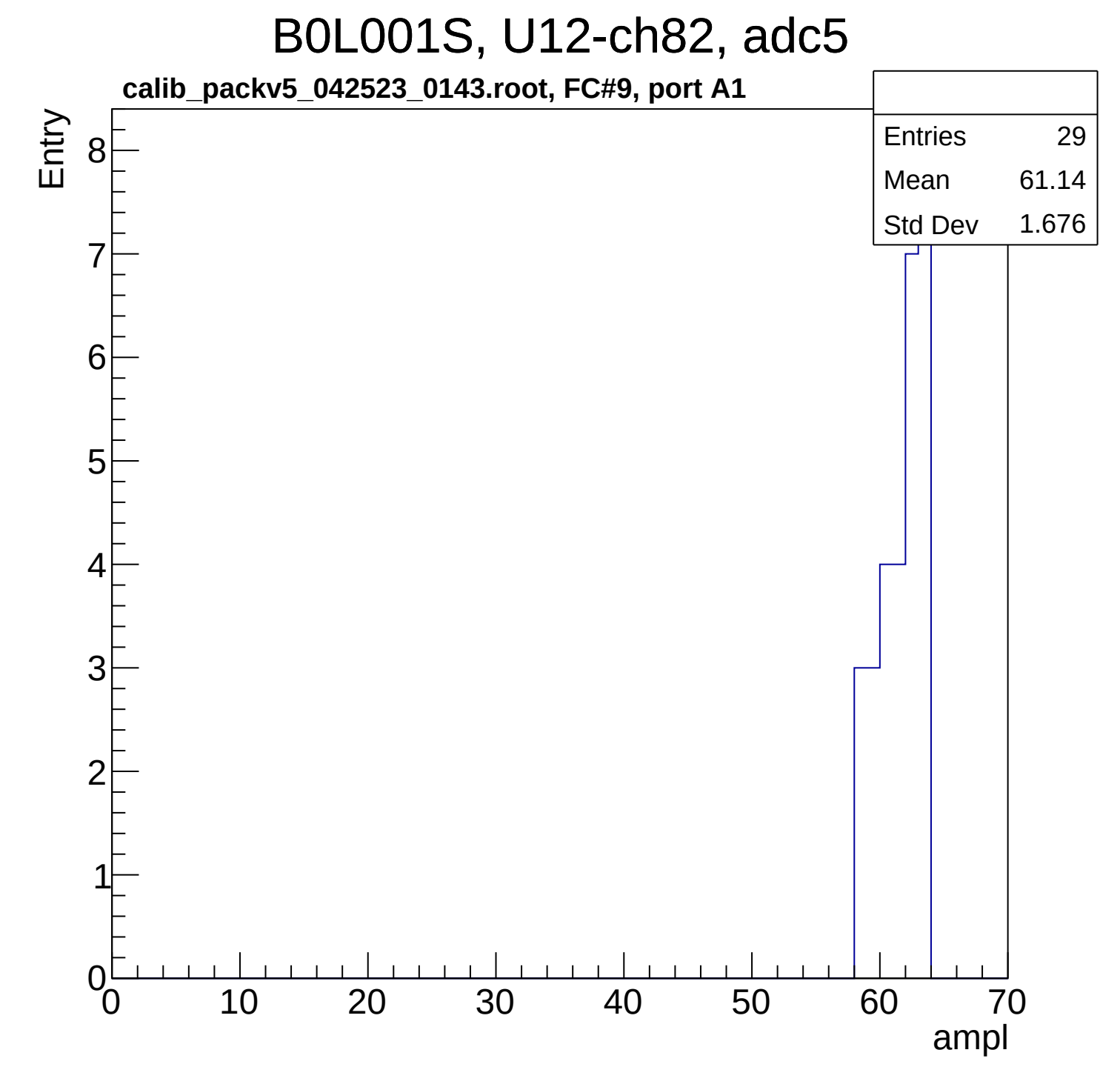
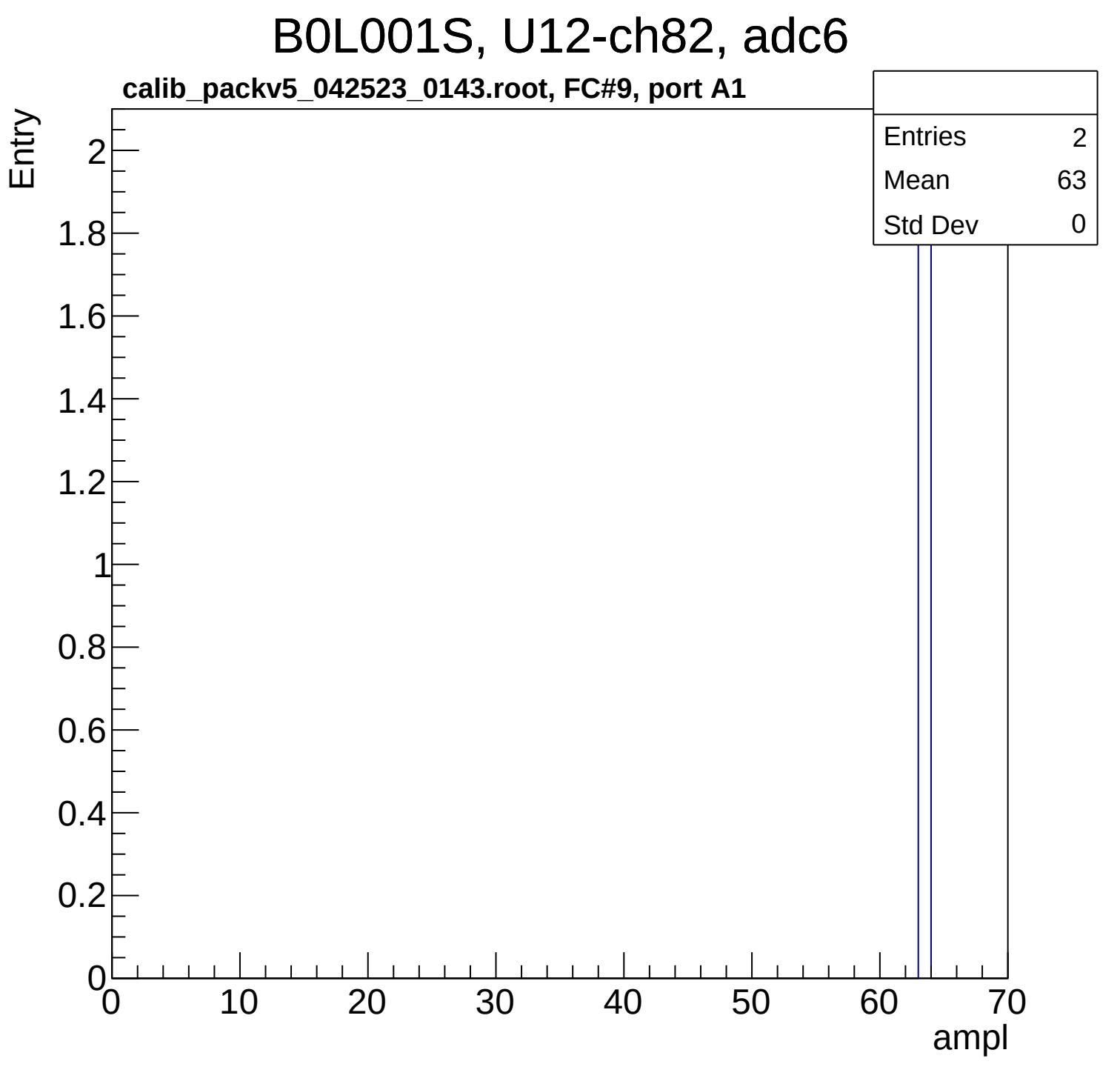
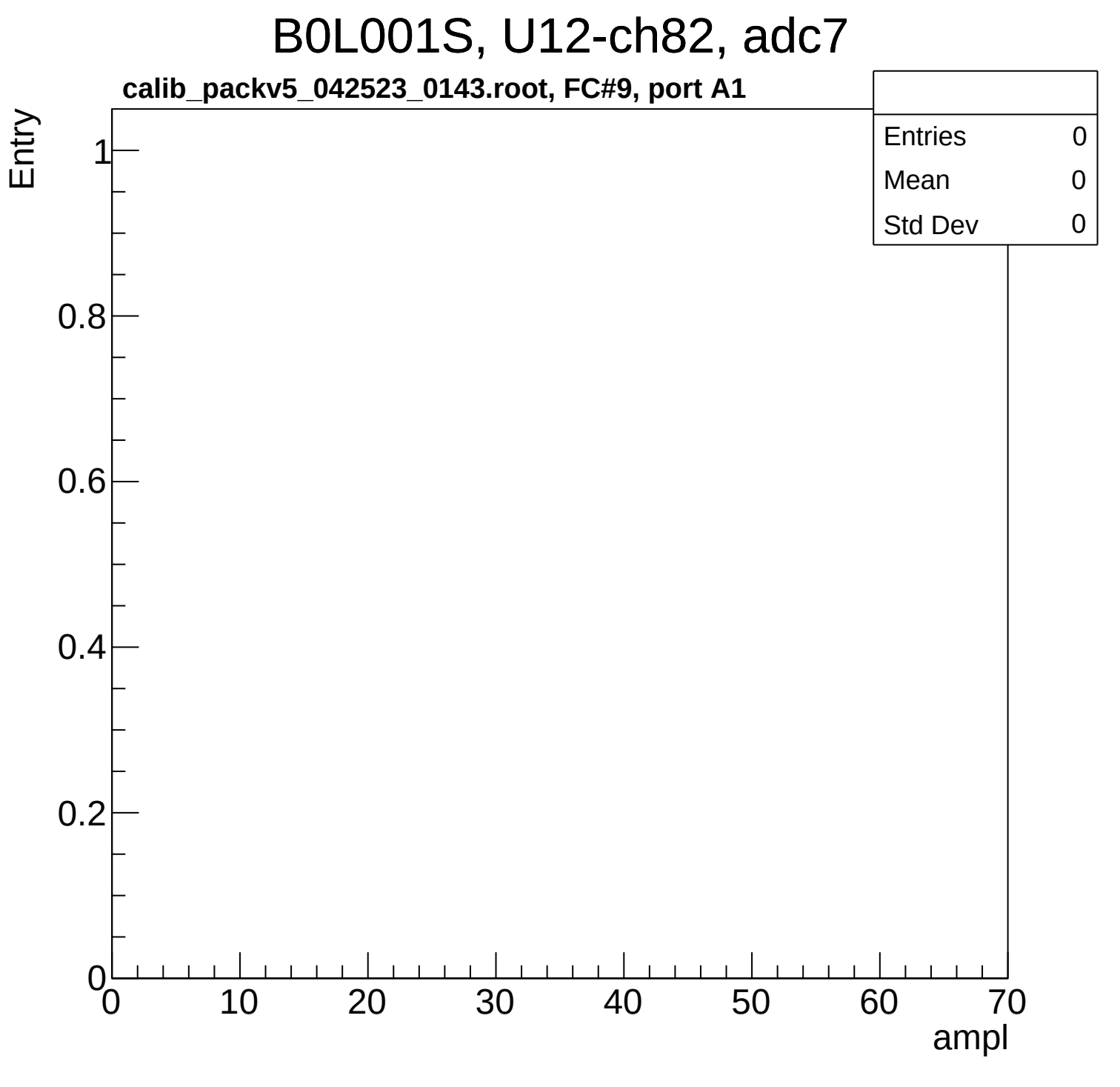
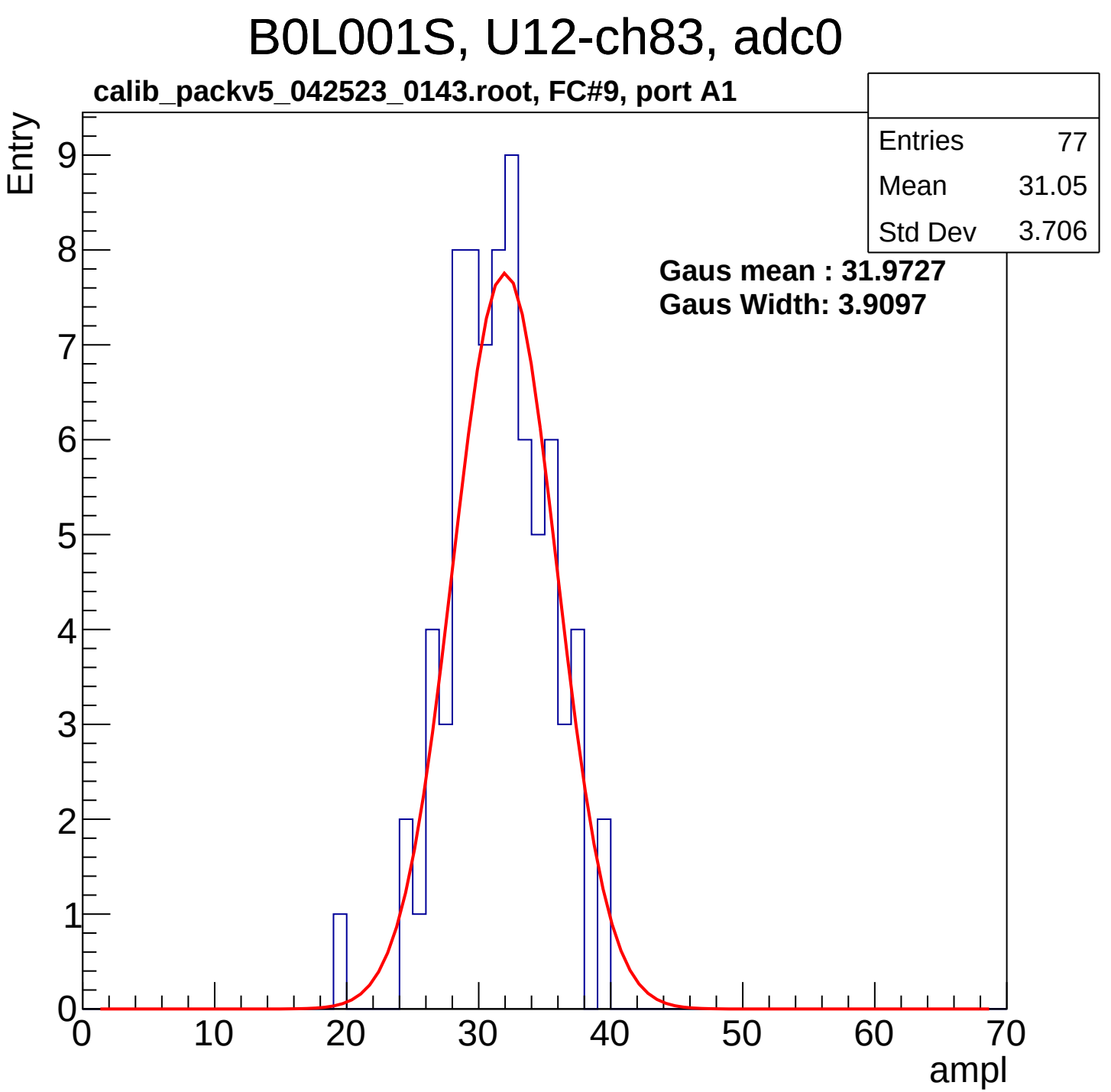

B0L001S, U12-ch82, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 69
Mean 50.55
Std Dev 3.273
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

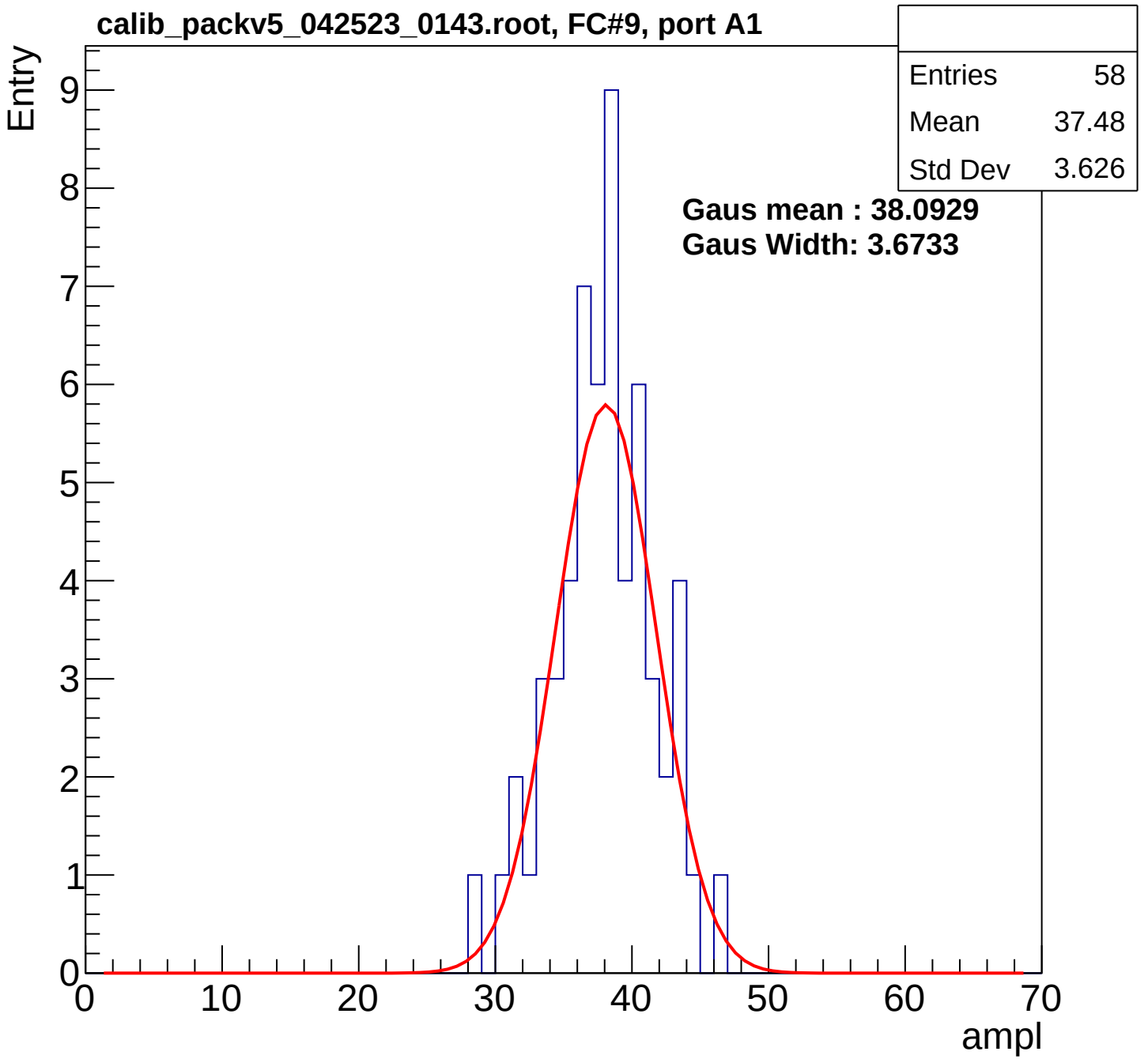

B0L001S, U12-ch82, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 60
Mean 56.43
Std Dev 7.83
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch82, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 29
Mean 61.14
Std Dev 1.676
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch82, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L001S, U12-ch82, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch83, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 77
Mean 31.05
Std Dev 3.706
Gaus mean : 31.9727
Gaus Width: 3.9097
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch83, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 58
Mean 37.48
Std Dev 3.626
Gaus mean : 38.0929
Gaus Width: 3.6733
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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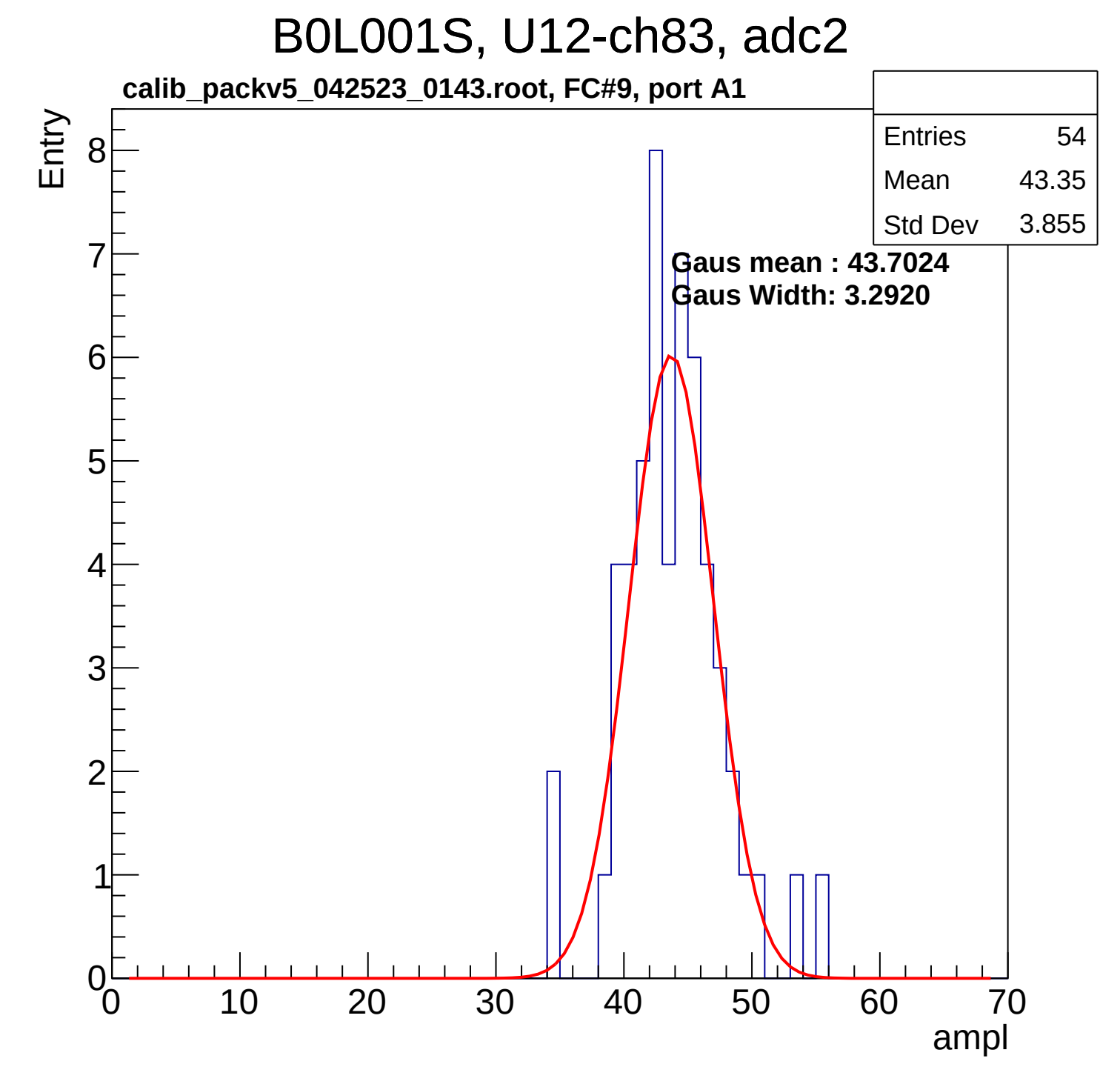
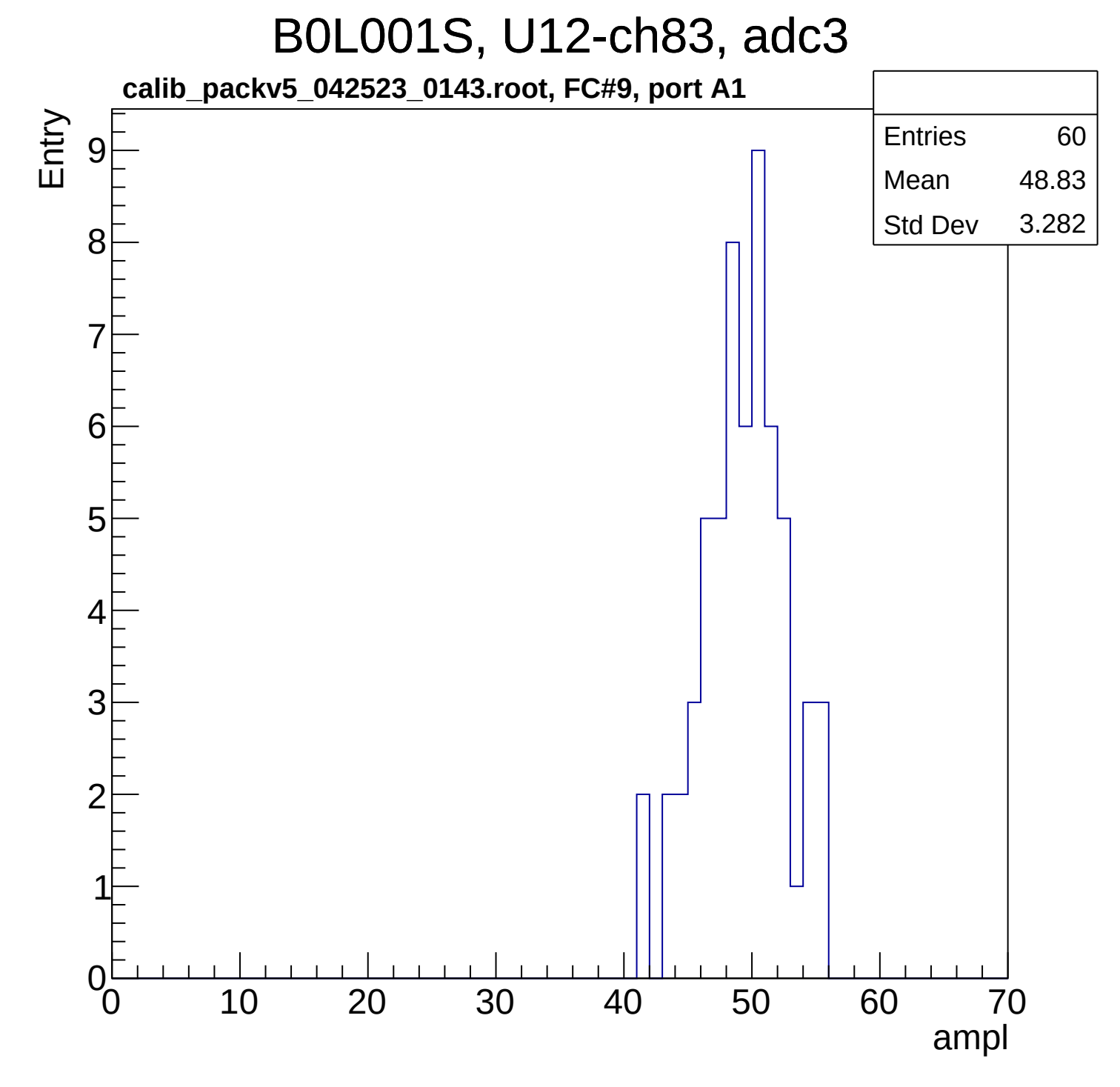
20
30
40
50
60
70


B0L001S, U12-ch83, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 54
Mean 43.35
Std Dev 3.855
Gaus mean : 43.7024
Gaus Width: 3.2920
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch83, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 60
Mean 48.83
Std Dev 3.282
Entry
ampl
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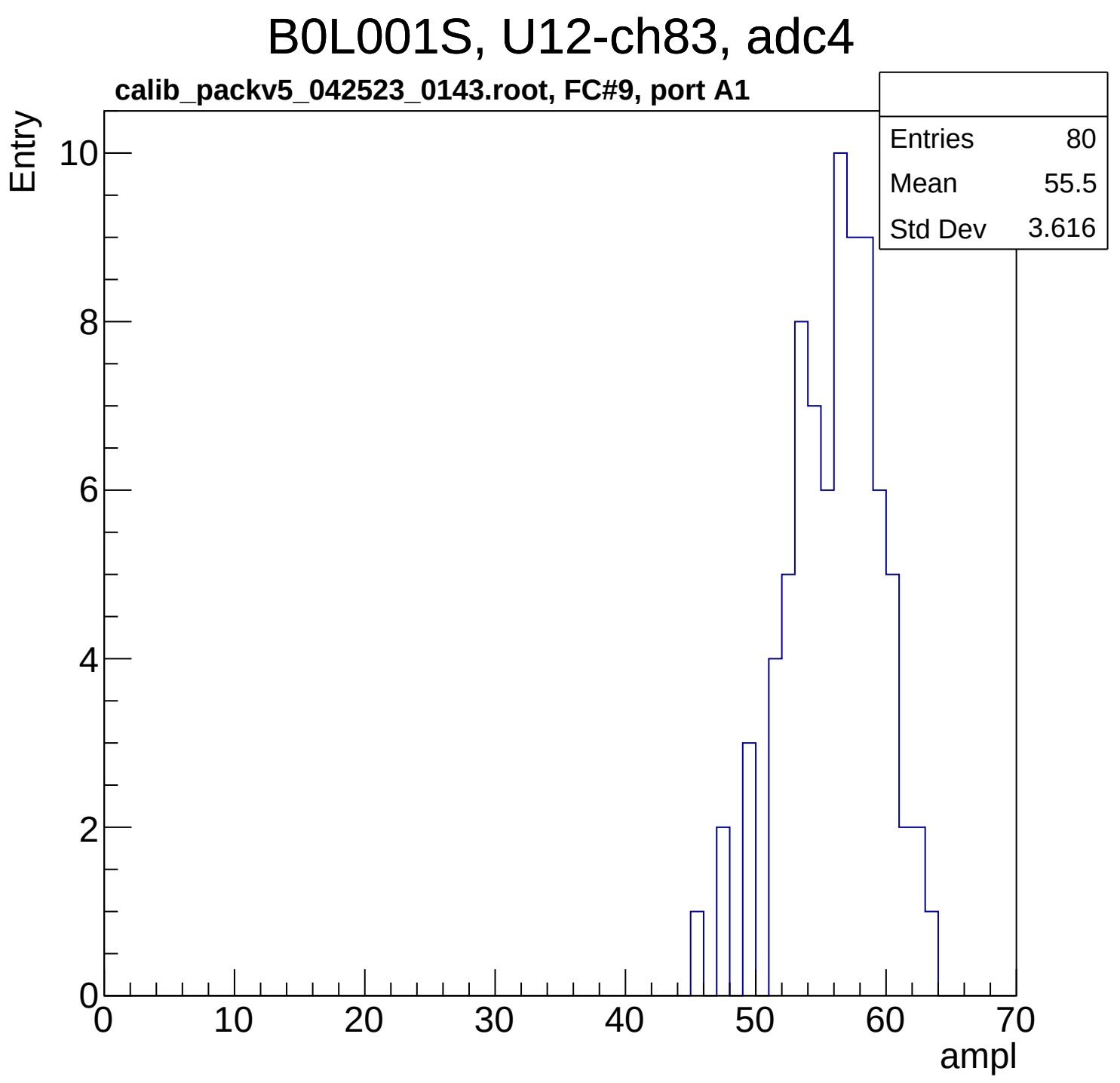
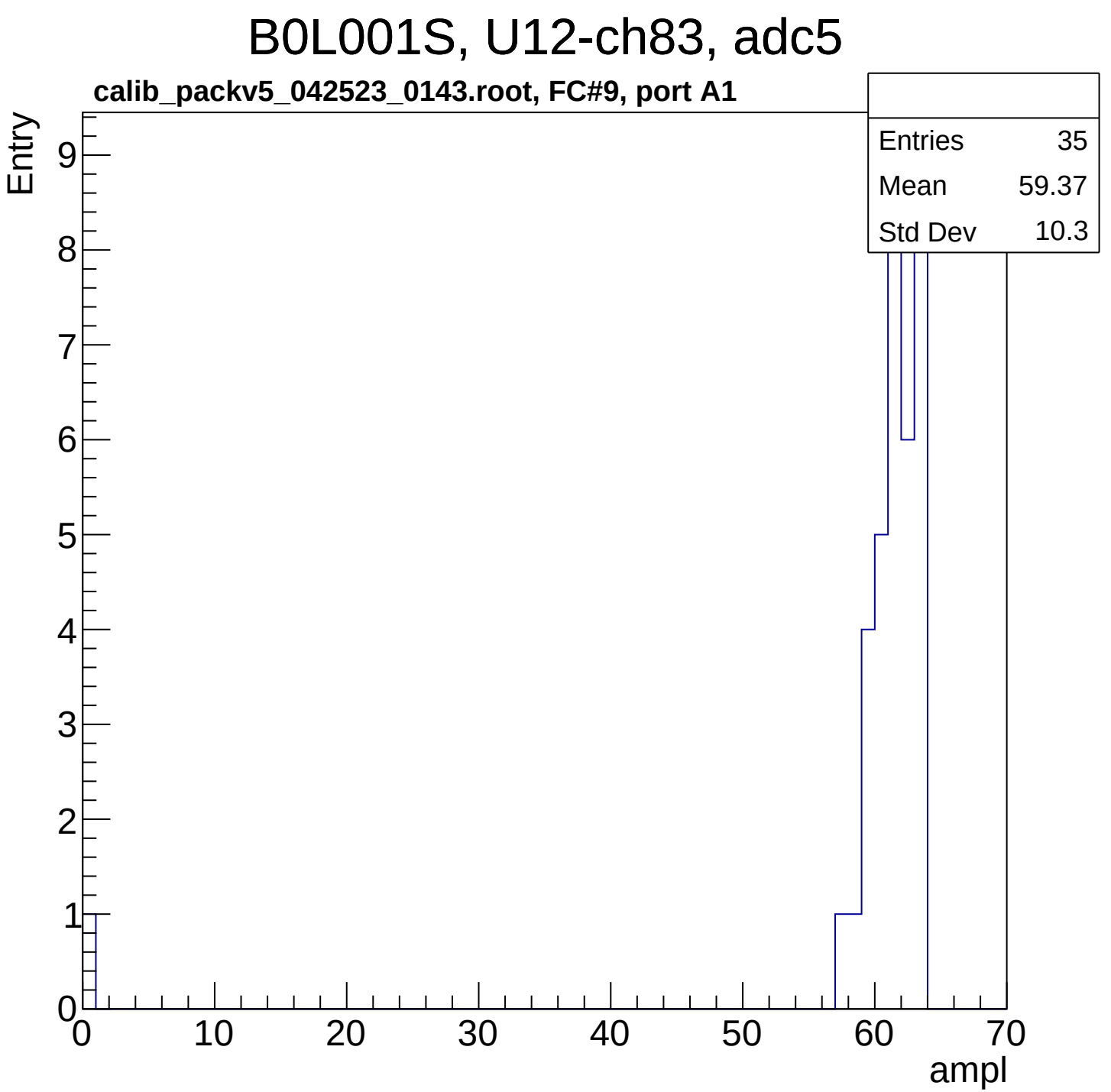
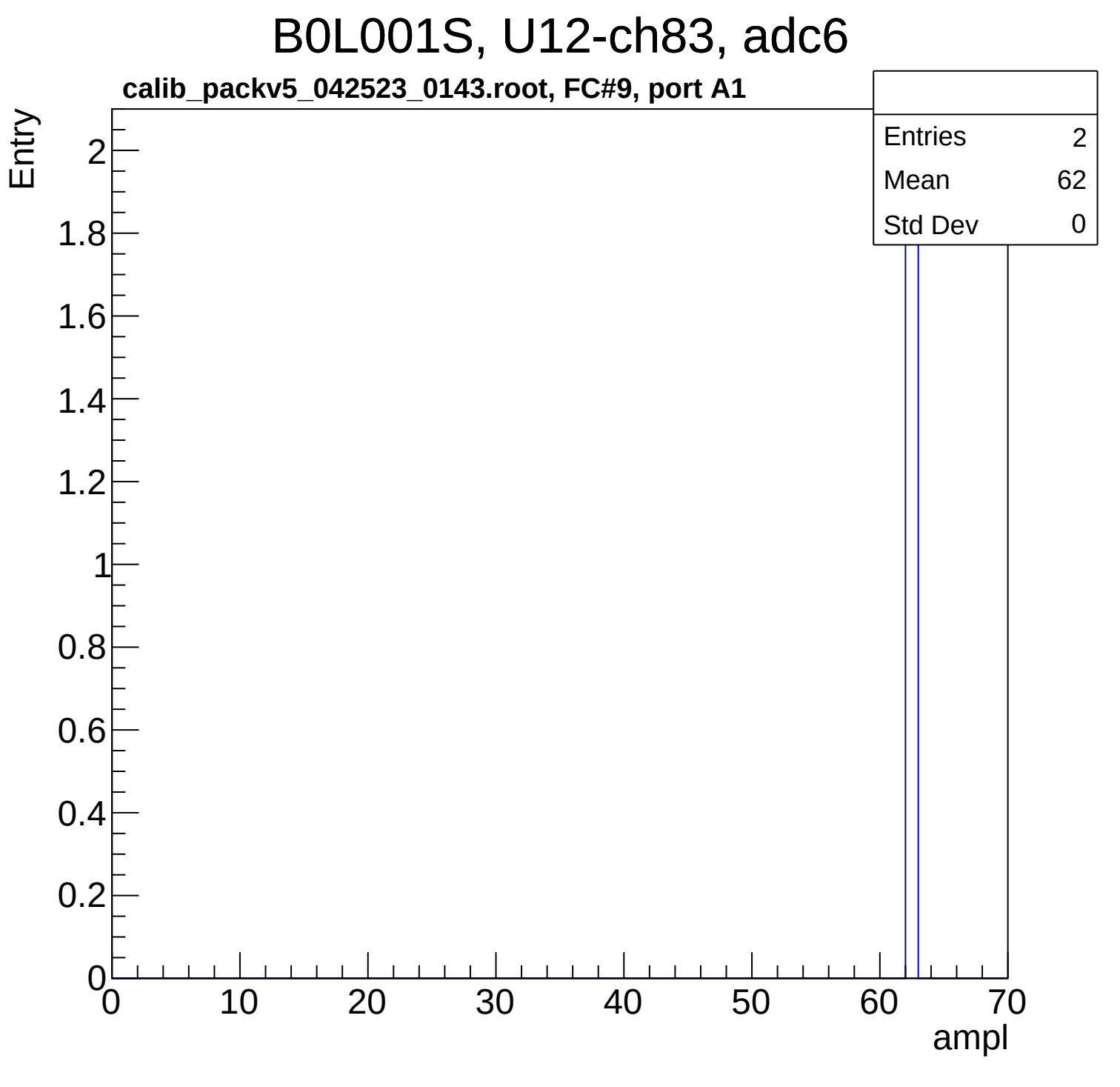
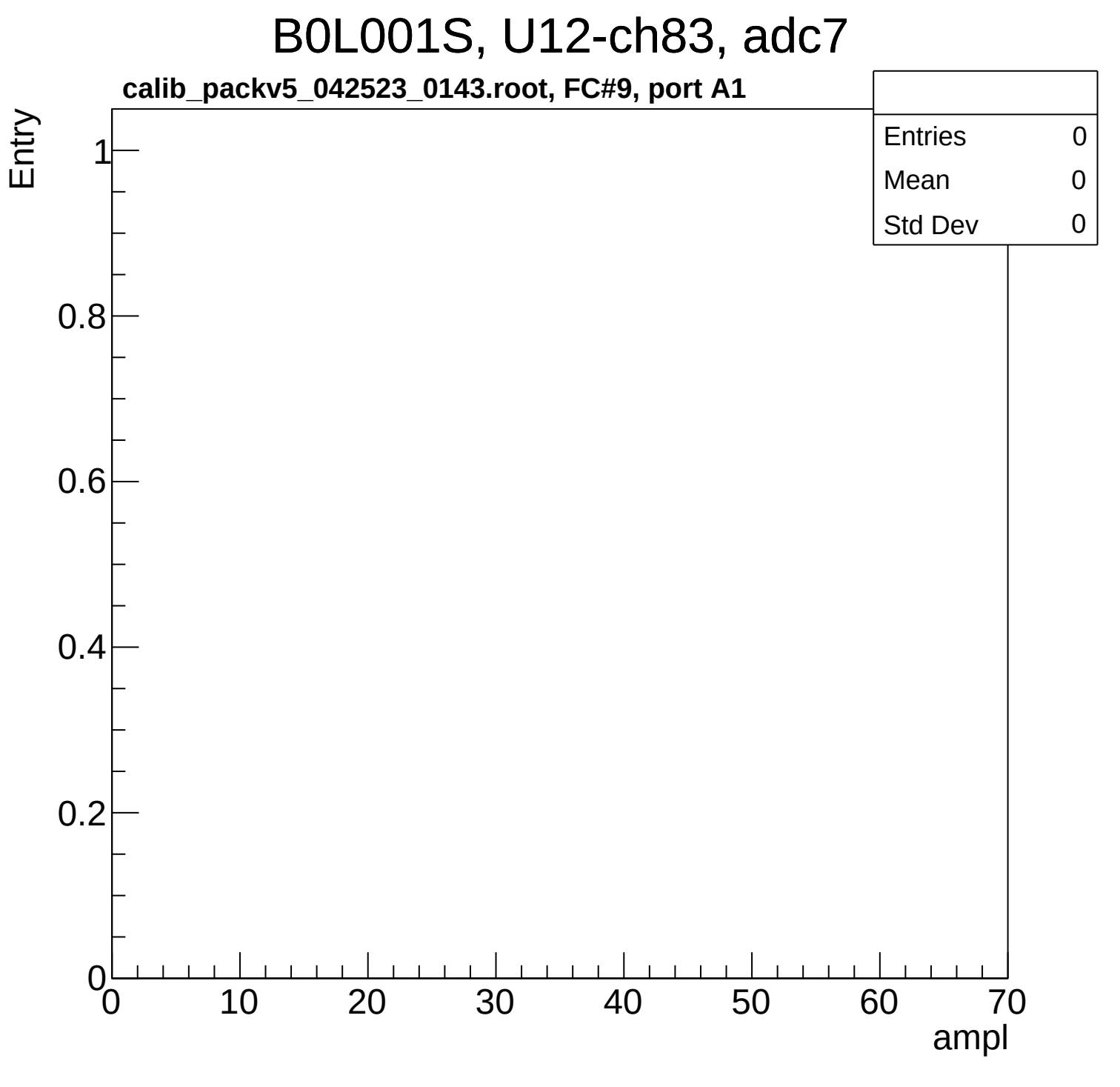
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch83, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 80
Mean 55.5
Std Dev 3.616
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch83, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 35
Mean 59.37
Std Dev 10.3
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch83, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 62
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L001S, U12-ch83, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
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0.8
0.6
0.4
0.2
0
0
10
20
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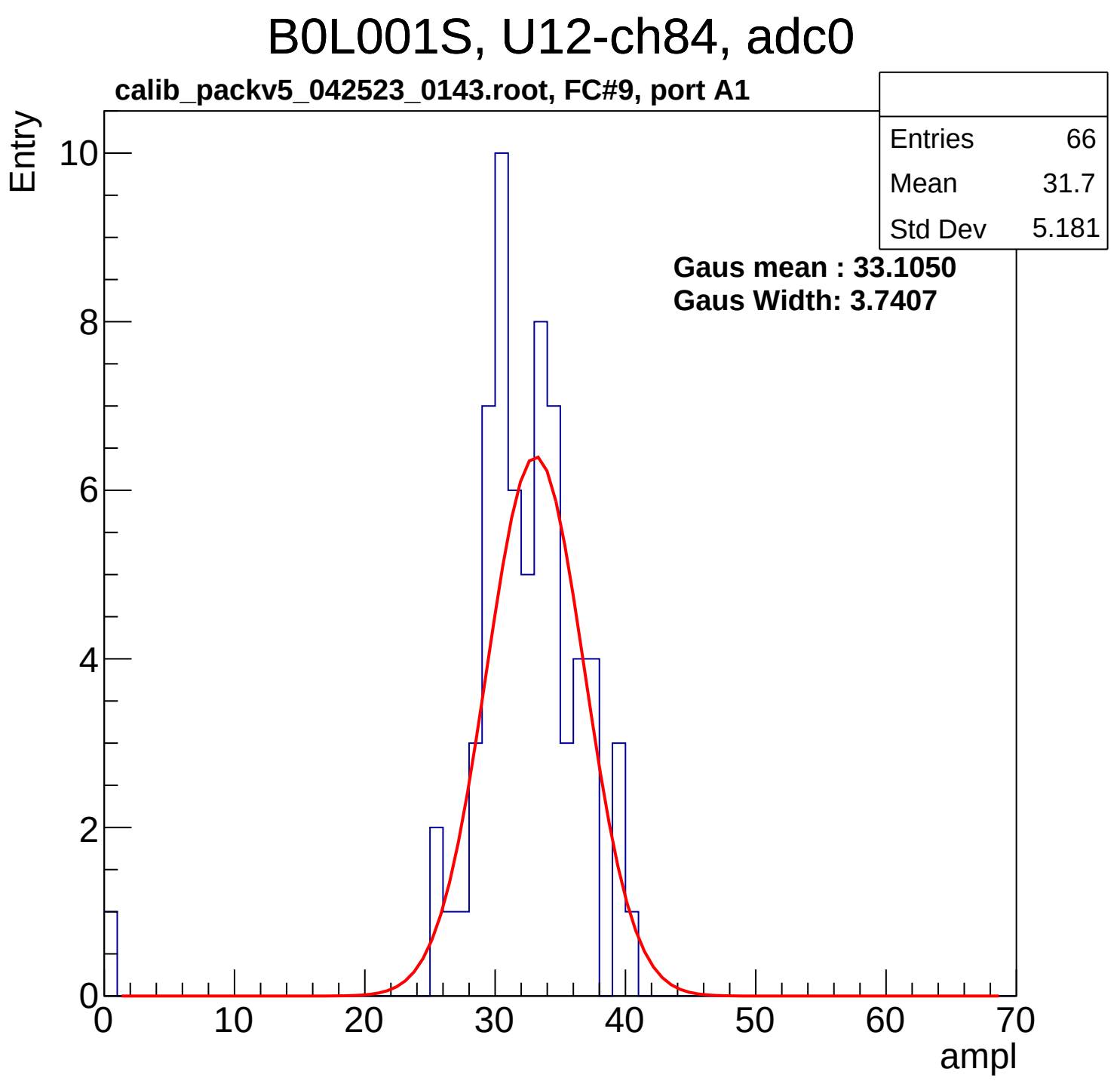
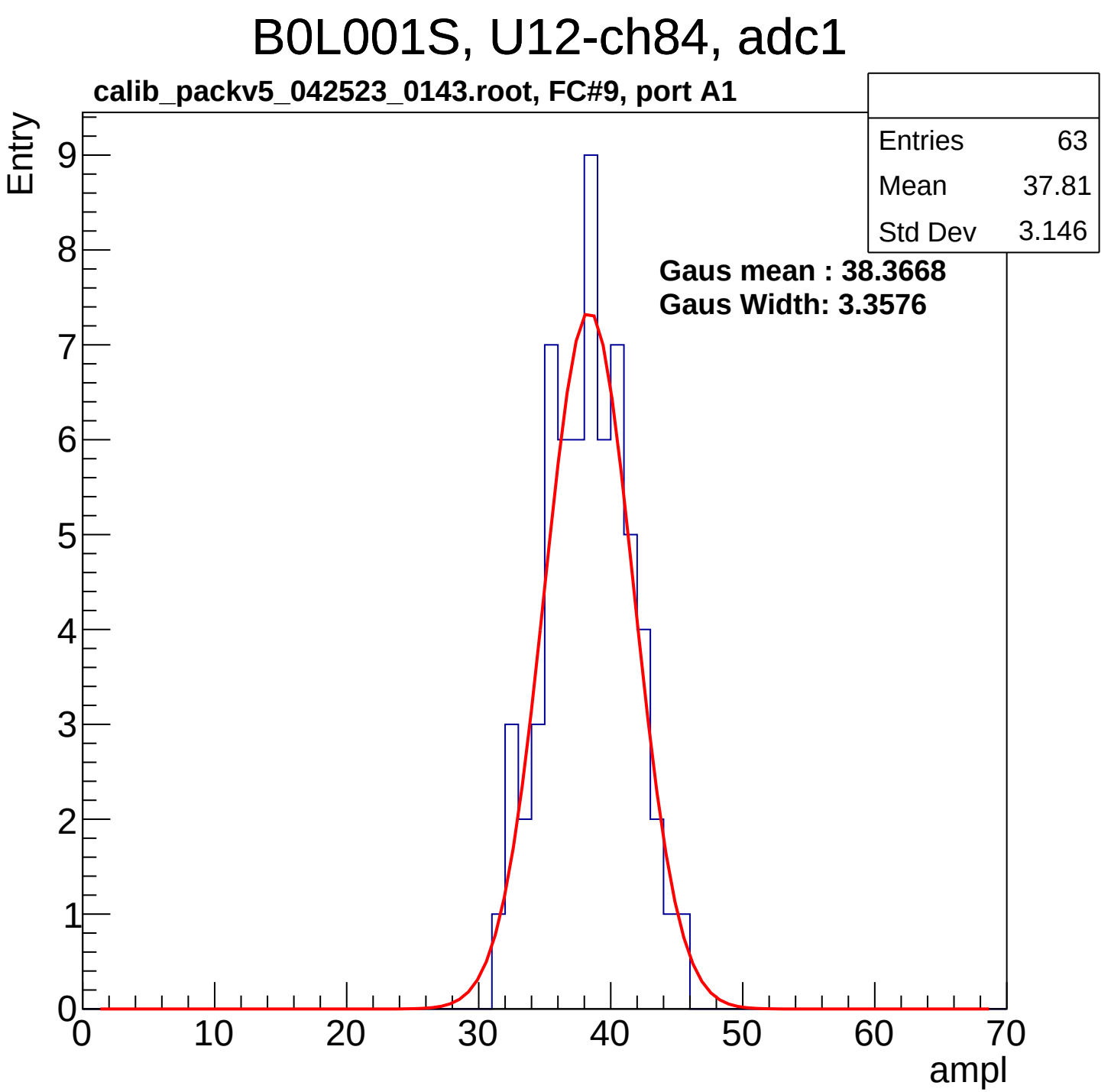
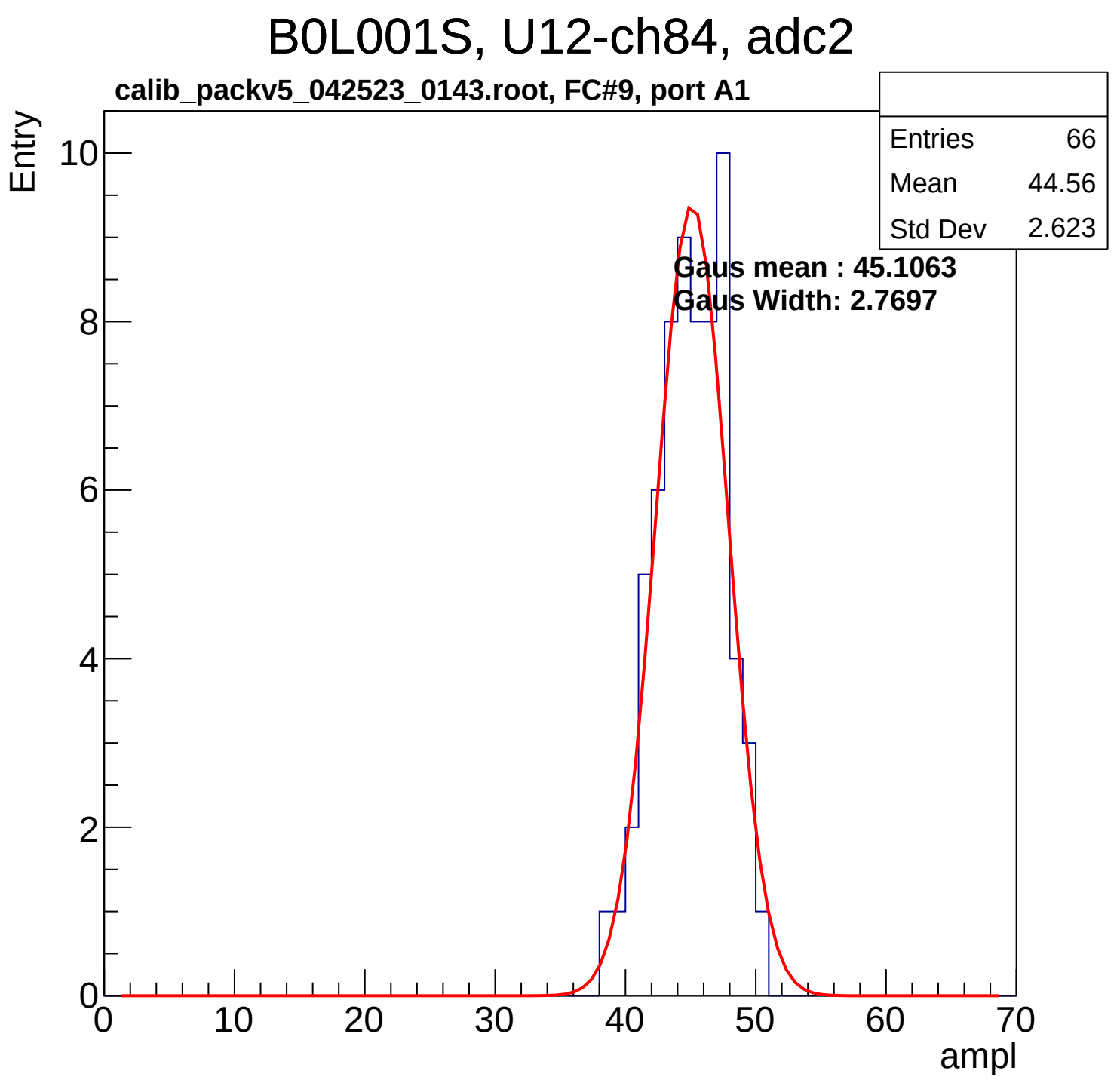
40
50
60
70
ampl


B0L001S, U12-ch84, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 66
Mean 31.7
Std Dev 5.181
Gaus mean : 33.1050
Gaus Width: 3.7407
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch84, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 63
Mean 37.81
Std Dev 3.146
Gaus mean : 38.3668
Gaus Width: 3.3576
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch84, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 66
Mean 44.56
Std Dev 2.623
Gaus mean : 45.1063
Gaus Width: 2.7697
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
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60
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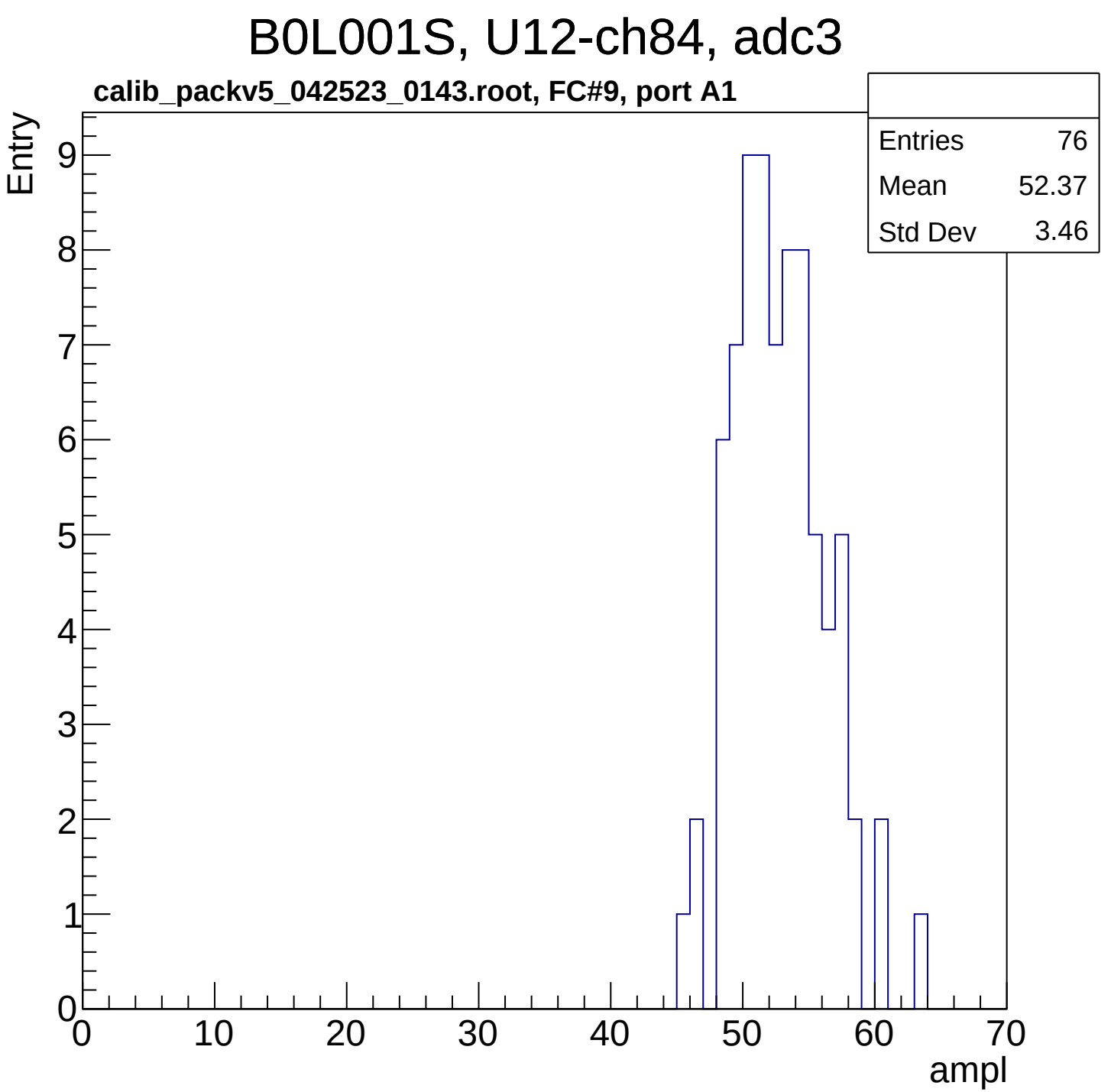
B0L001S, U12-ch84, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 76
Mean 52.37
Std Dev 3.46
Entry
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4
5
6
7
8
9
0
10
20
30
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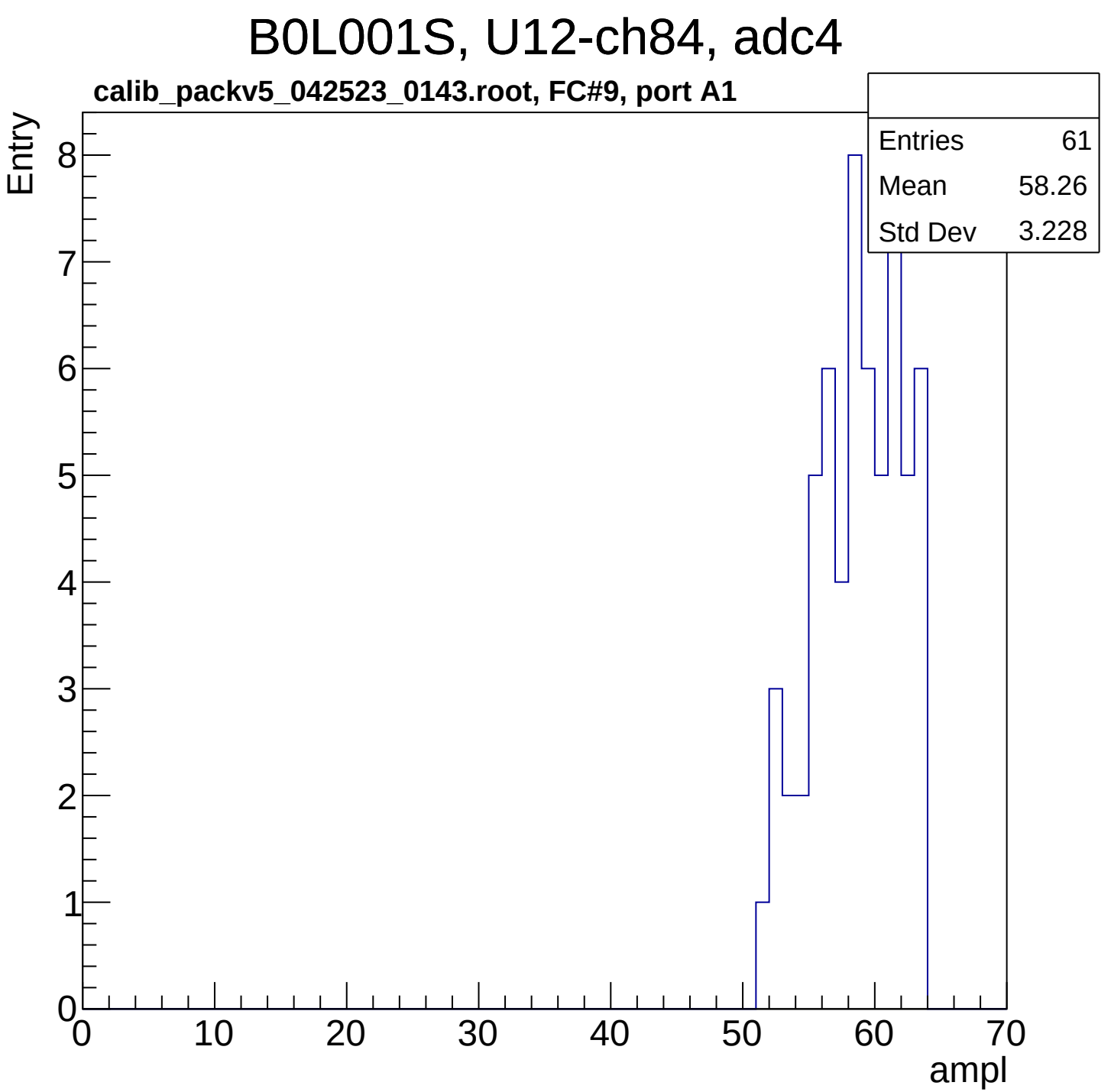
50
60
70
ampl


B0L001S, U12-ch84, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 61
Mean 58.26
Std Dev 3.228
Entry
ampl
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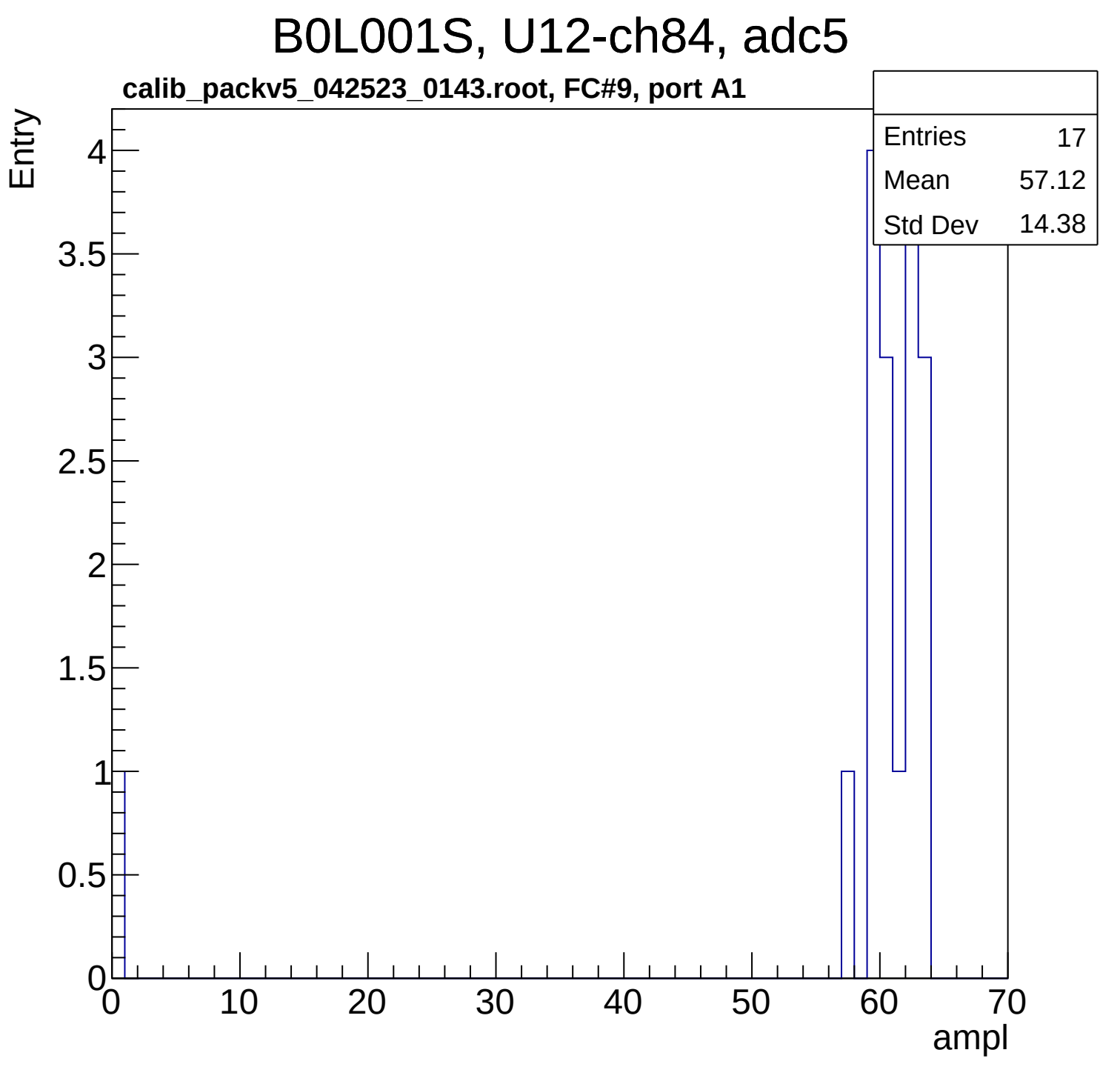
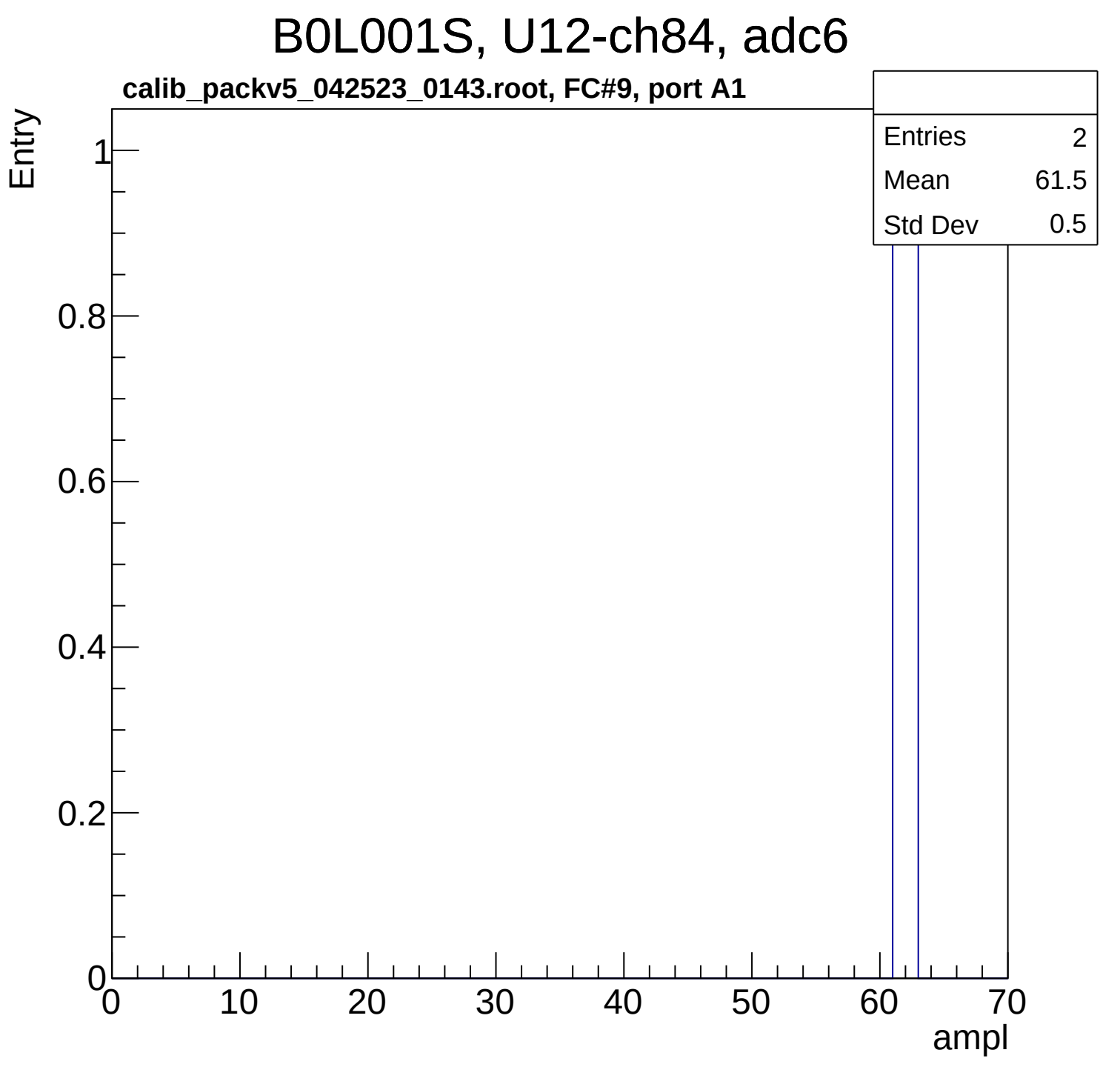
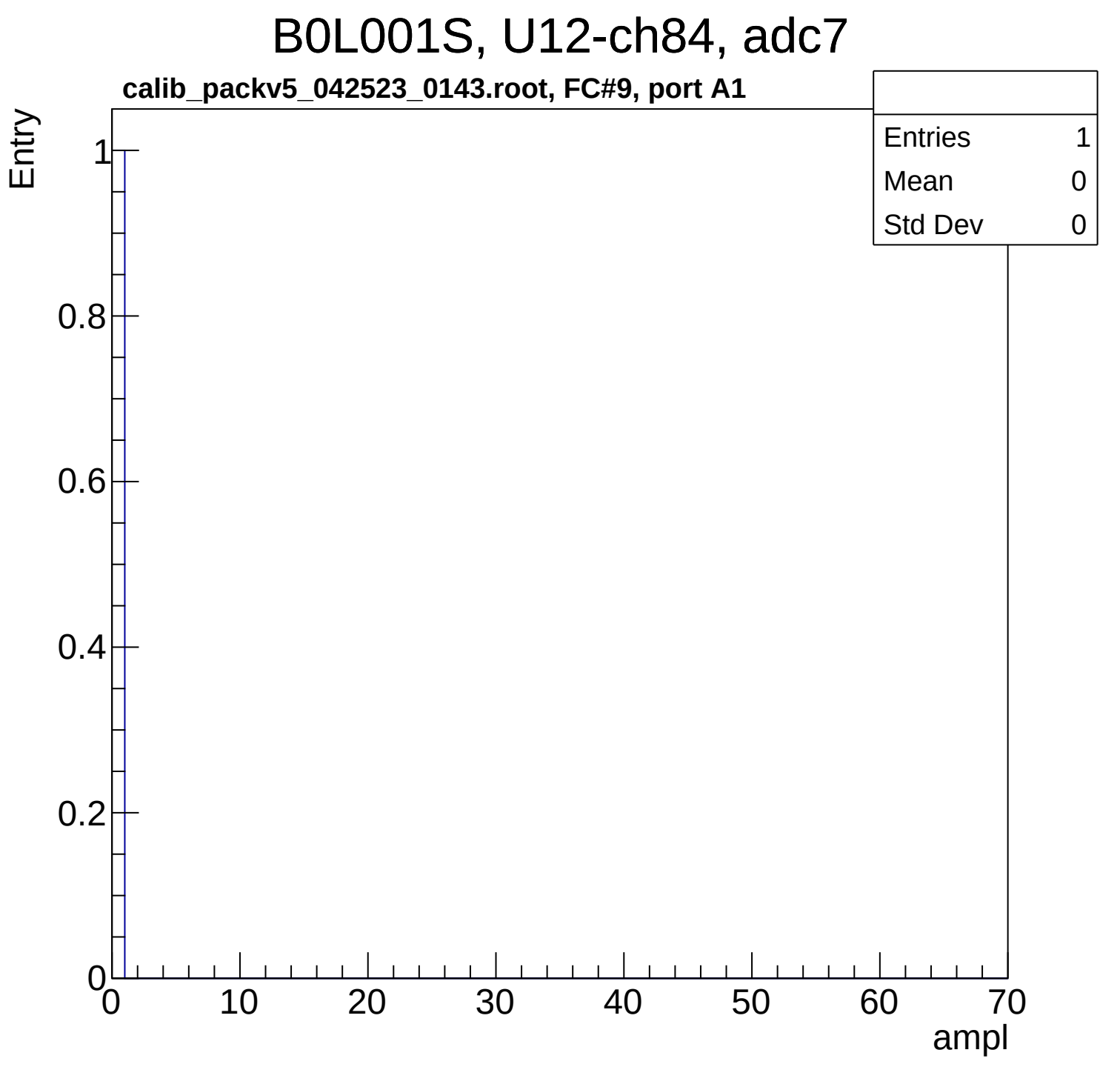
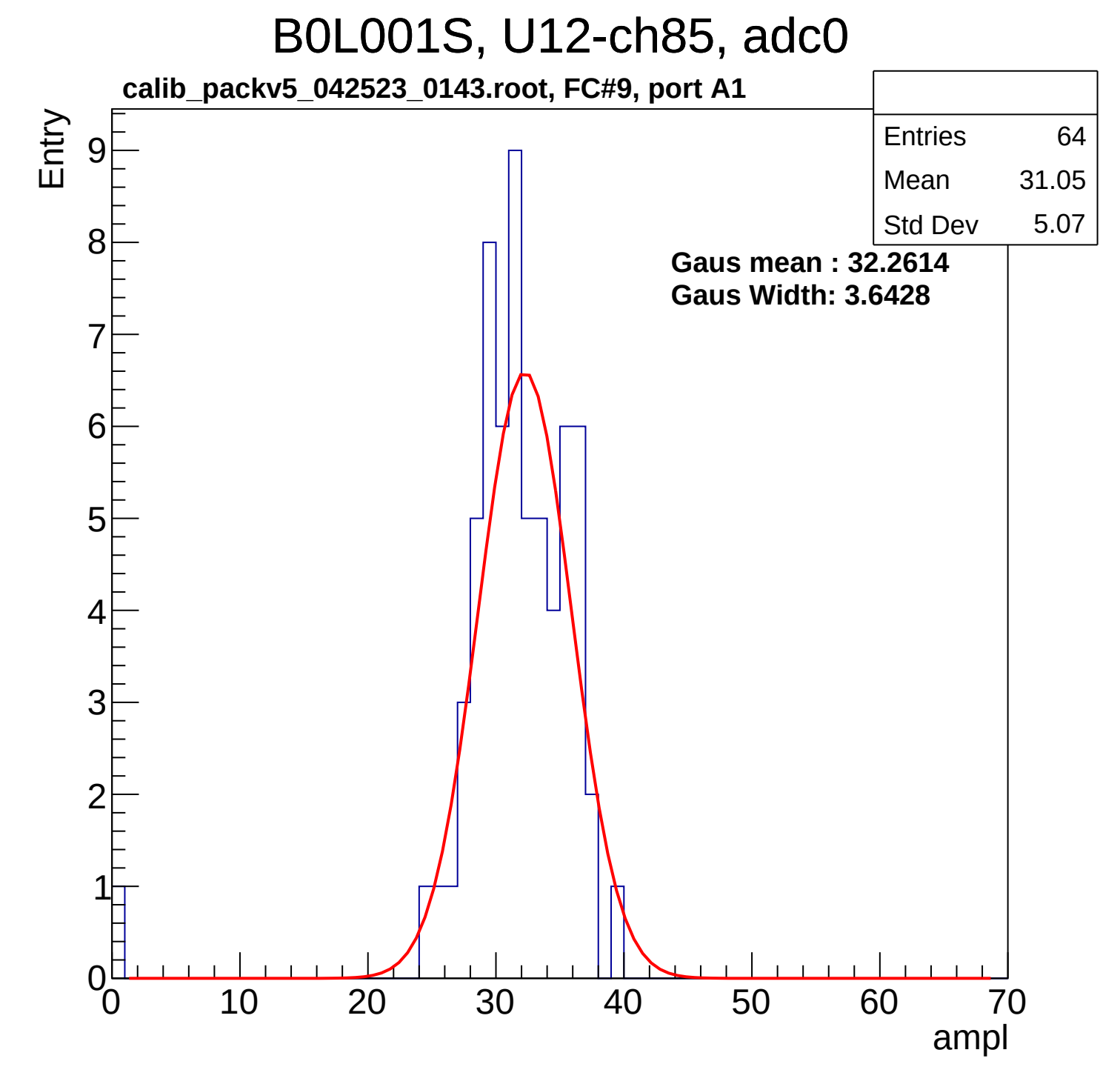
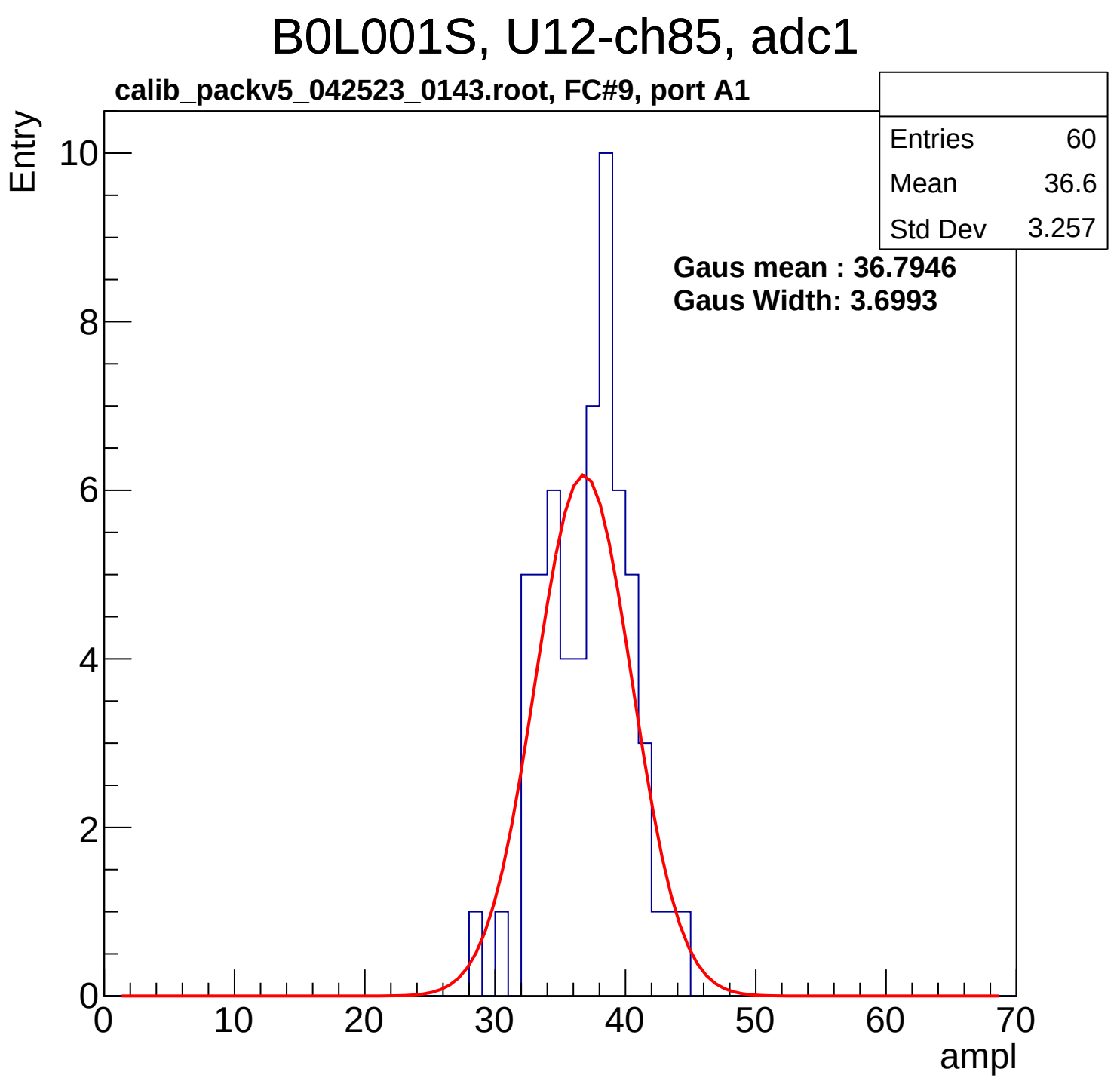
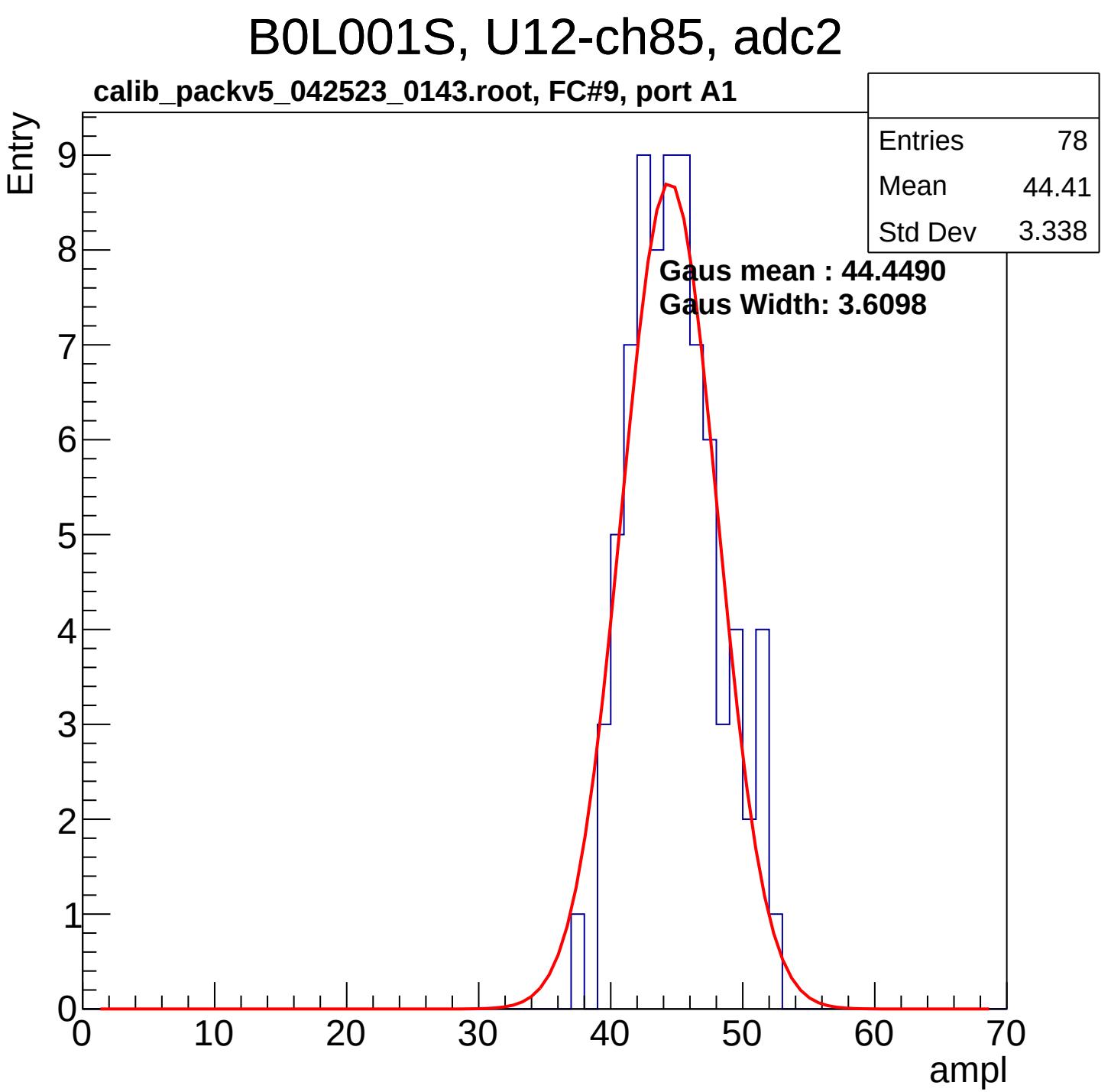

B0L001S, U12-ch84, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 17
Mean 57.12
Std Dev 14.38
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B0L001S, U12-ch84, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 61.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch84, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch85, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 64
Mean 31.05
Std Dev 5.07
Gaus mean : 32.2614
Gaus Width: 3.6428
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch85, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 60
Mean 36.6
Std Dev 3.257
Gaus mean : 36.7946
Gaus Width: 3.6993
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch85, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 78
Mean 44.41
Std Dev 3.338
Gaus mean : 44.4490
Gaus Width: 3.6098
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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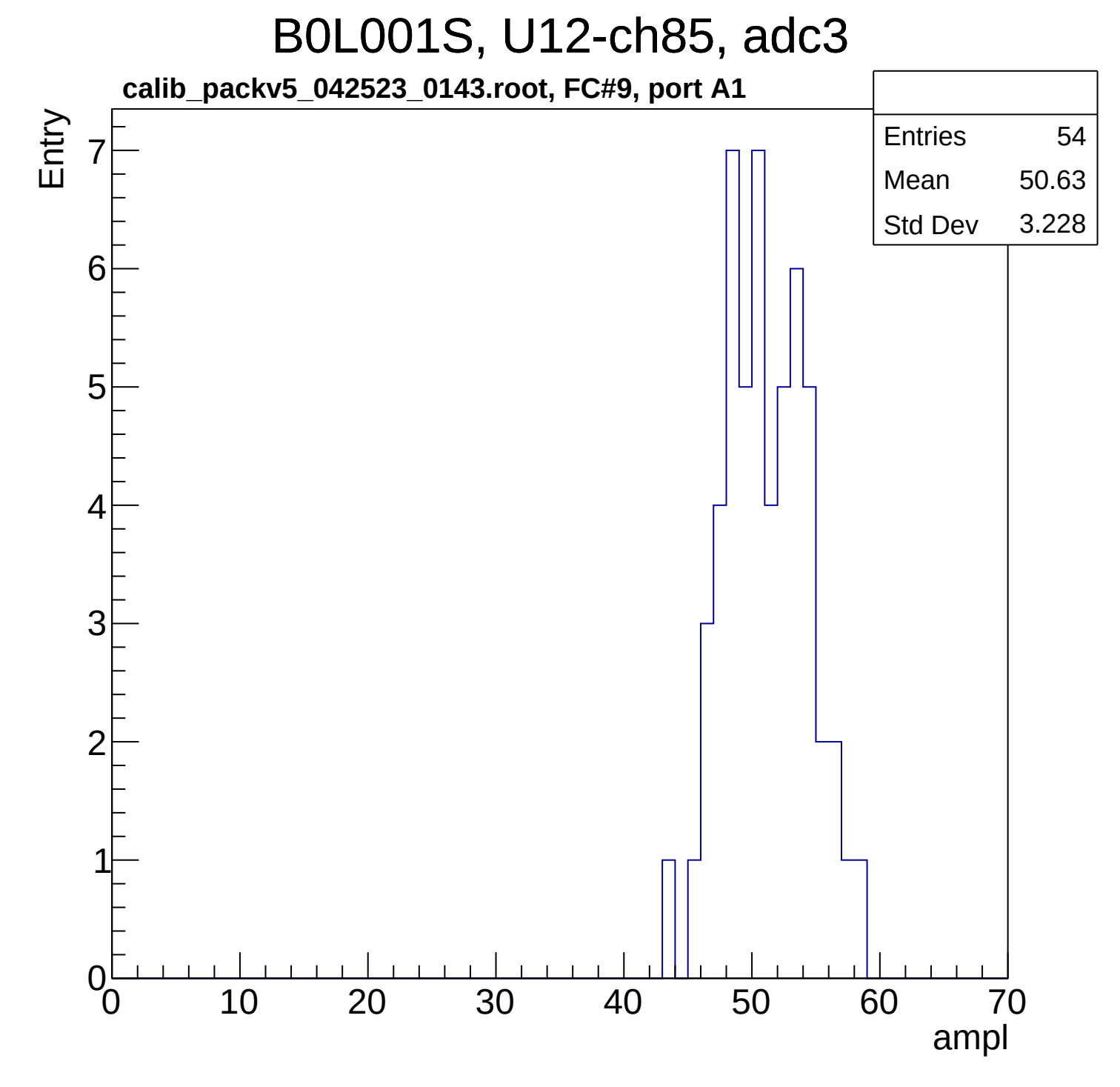
B0L001S, U12-ch85, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 54
Mean 50.63
Std Dev 3.228
Entry
ampl
0
1
2
3
4
5
6
7
0
10
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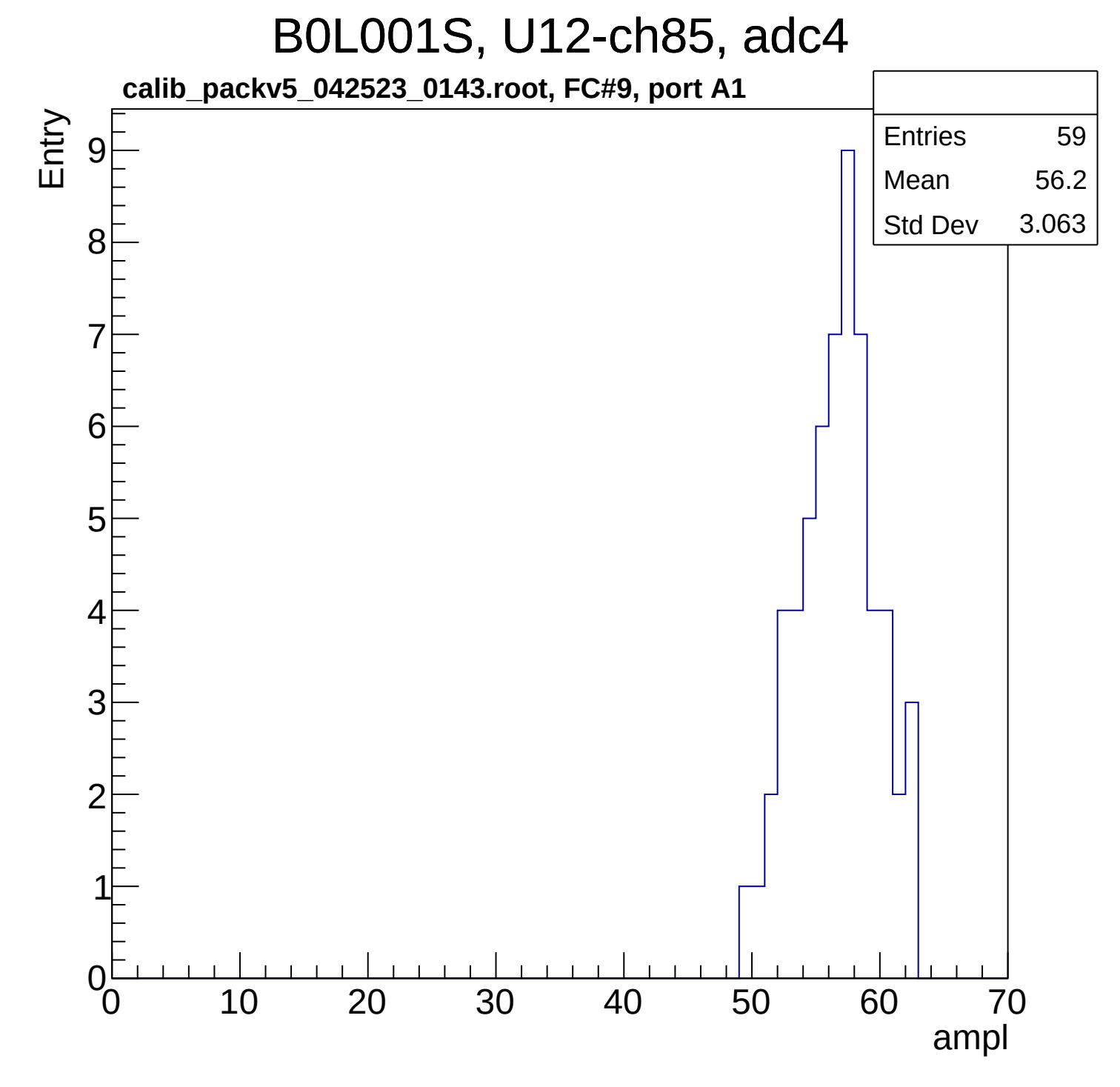
40
50
60
70


B0L001S, U12-ch85, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 59
Mean 56.2
Std Dev 3.063
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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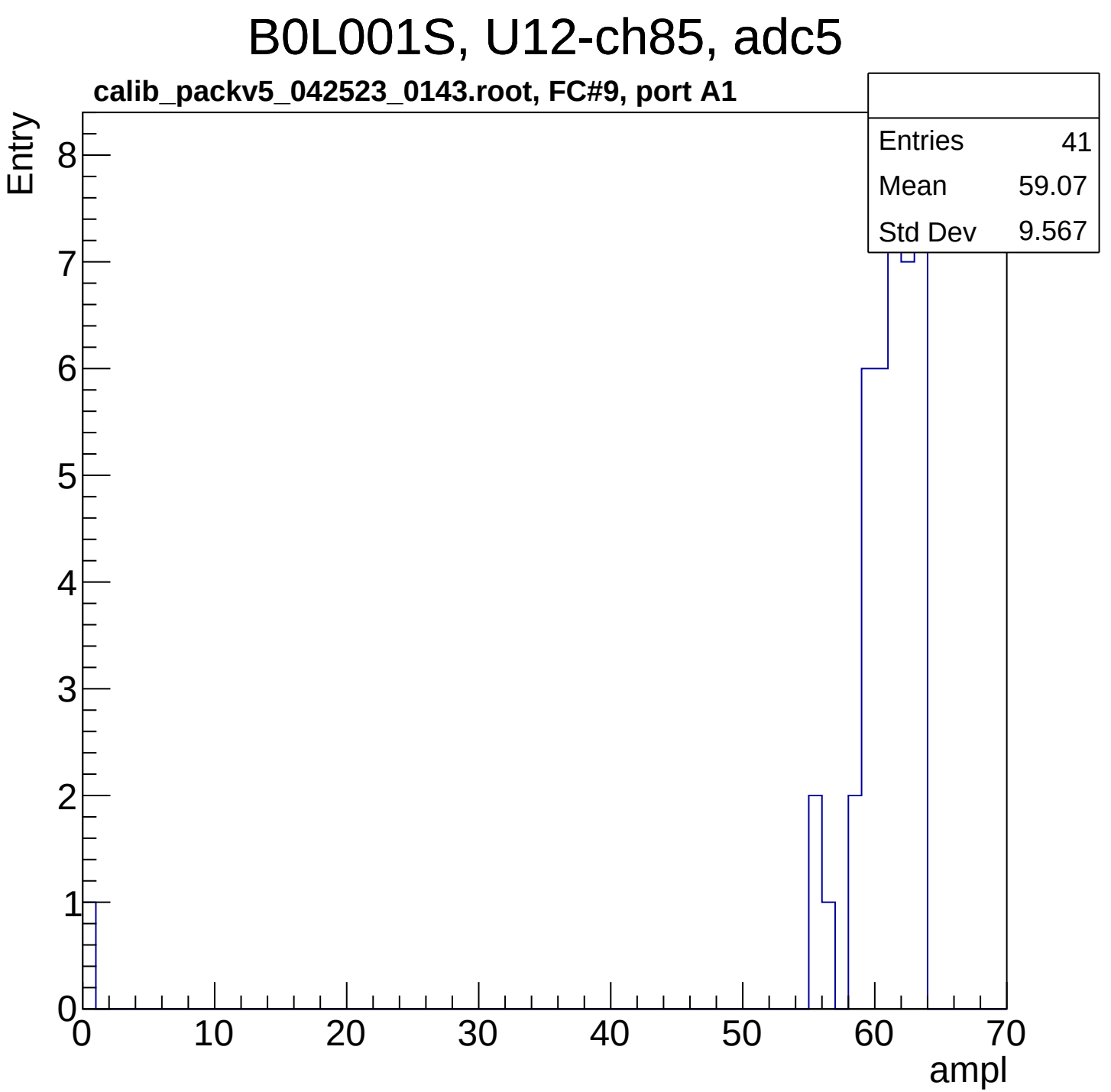
B0L001S, U12-ch85, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 41
Mean 59.07
Std Dev 9.567
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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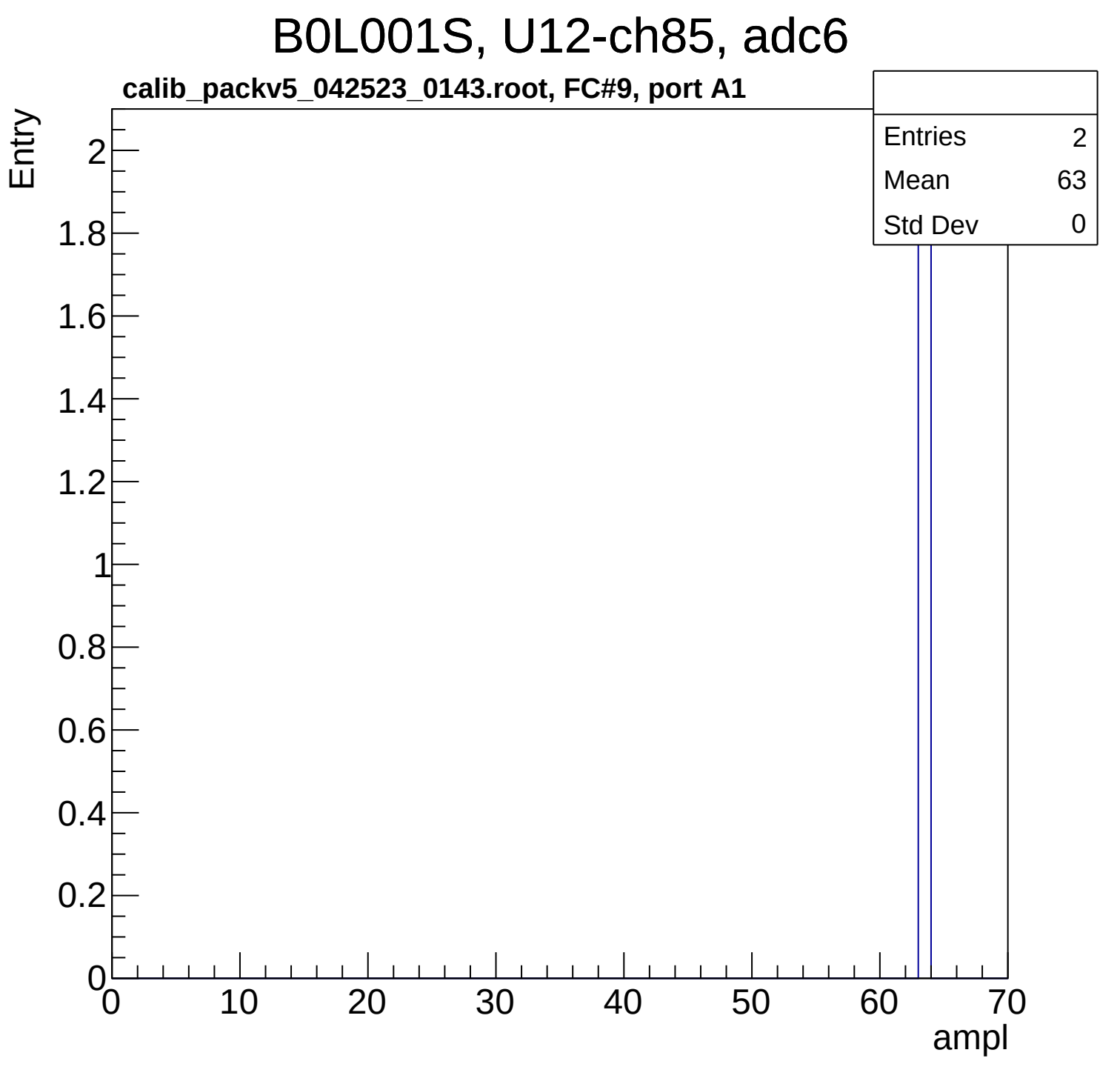
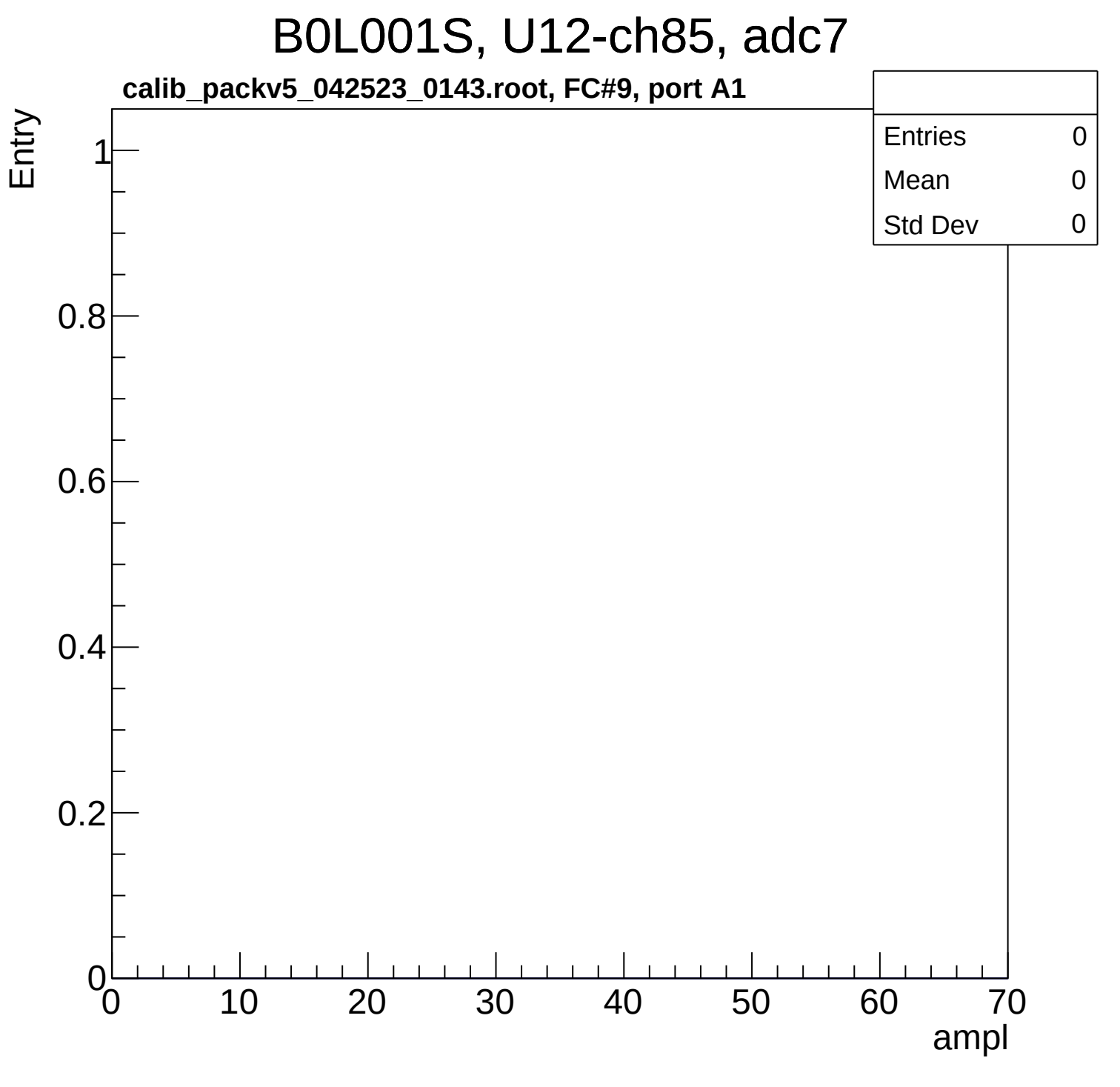
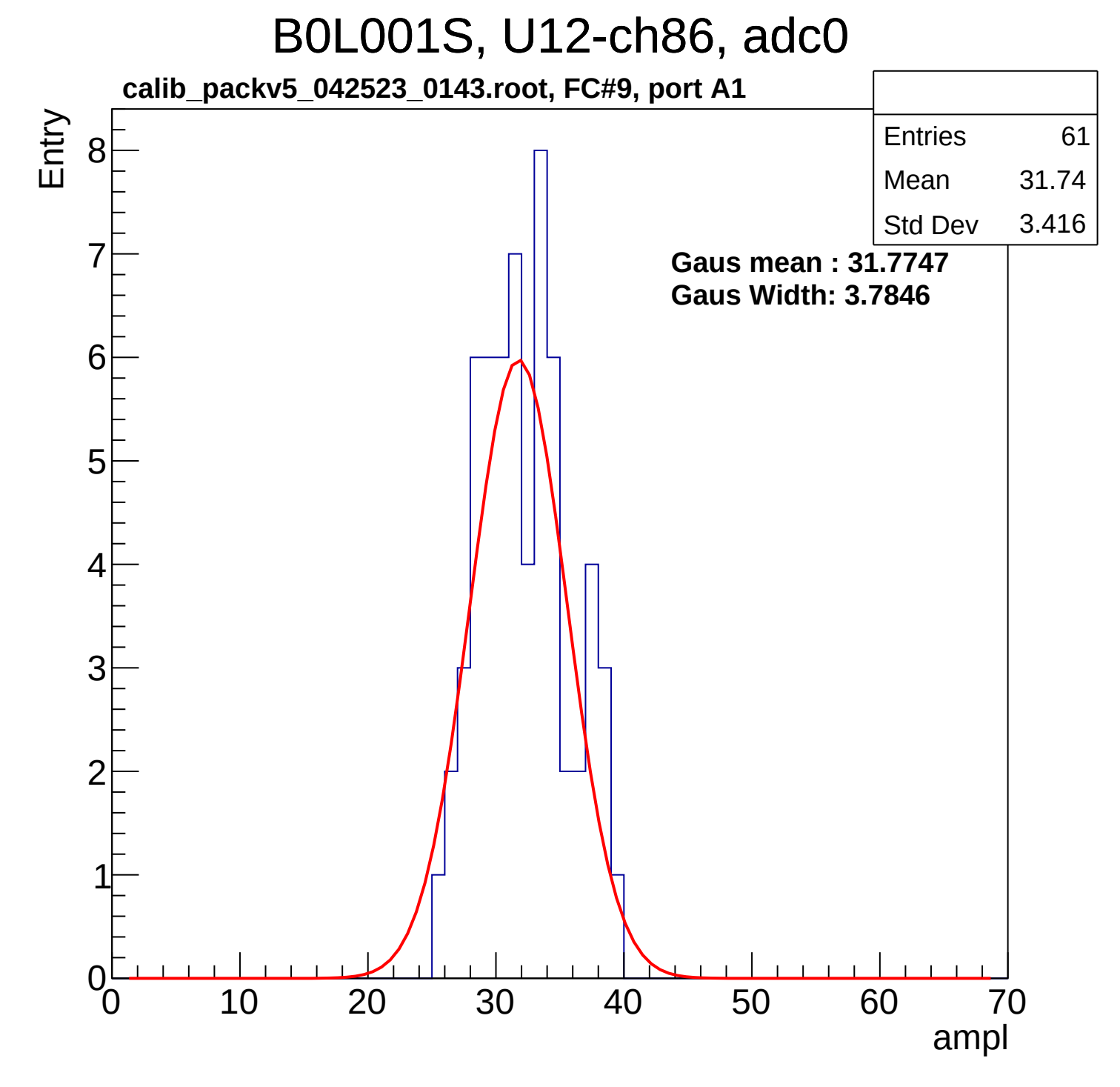
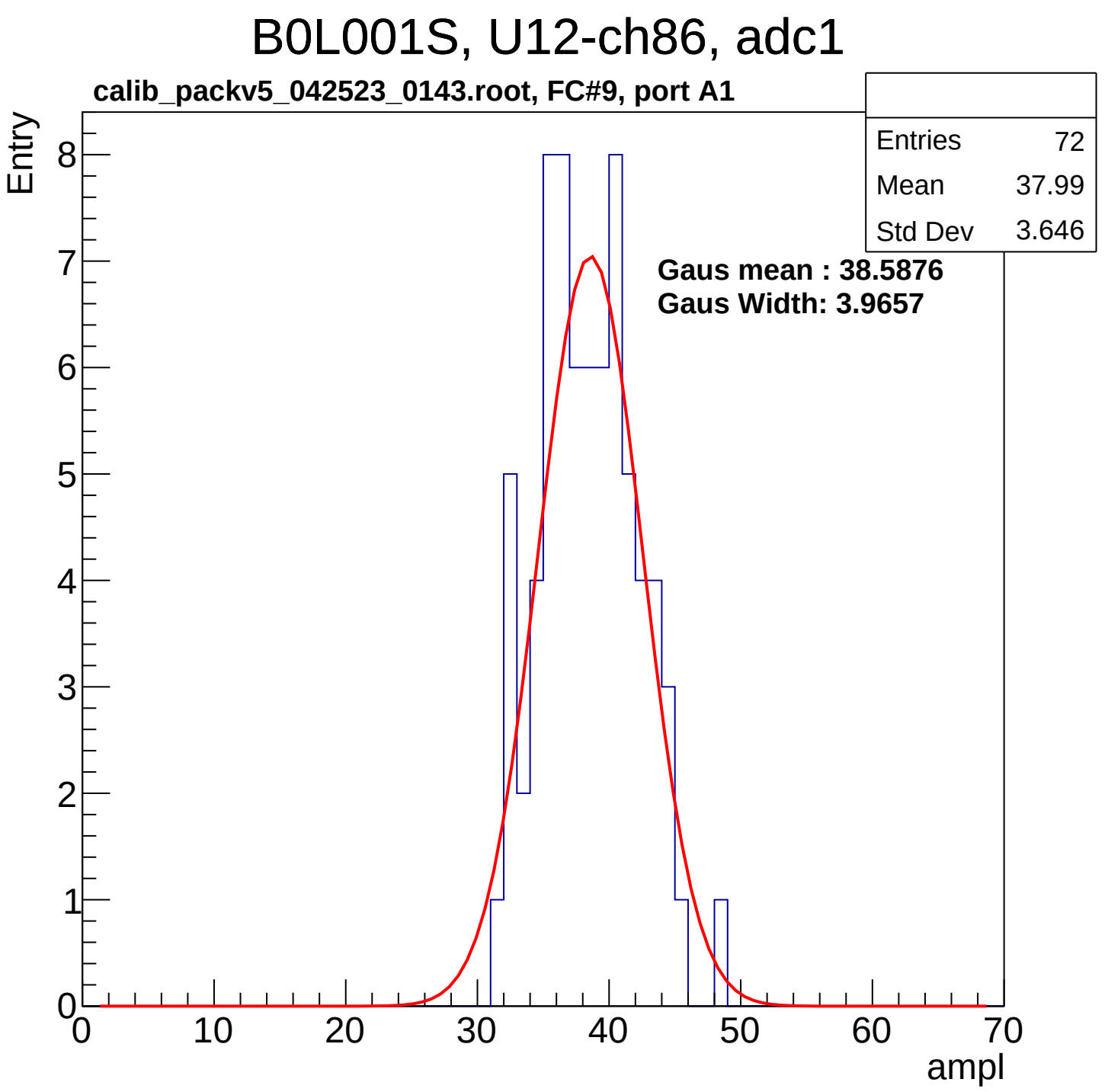

B0L001S, U12-ch85, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L001S, U12-ch85, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch86, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 61
Mean 31.74
Std Dev 3.416
Gaus mean : 31.7747
Gaus Width: 3.7846
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch86, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 72
Mean 37.99
Std Dev 3.646
Gaus mean : 38.5876
Gaus Width: 3.9657
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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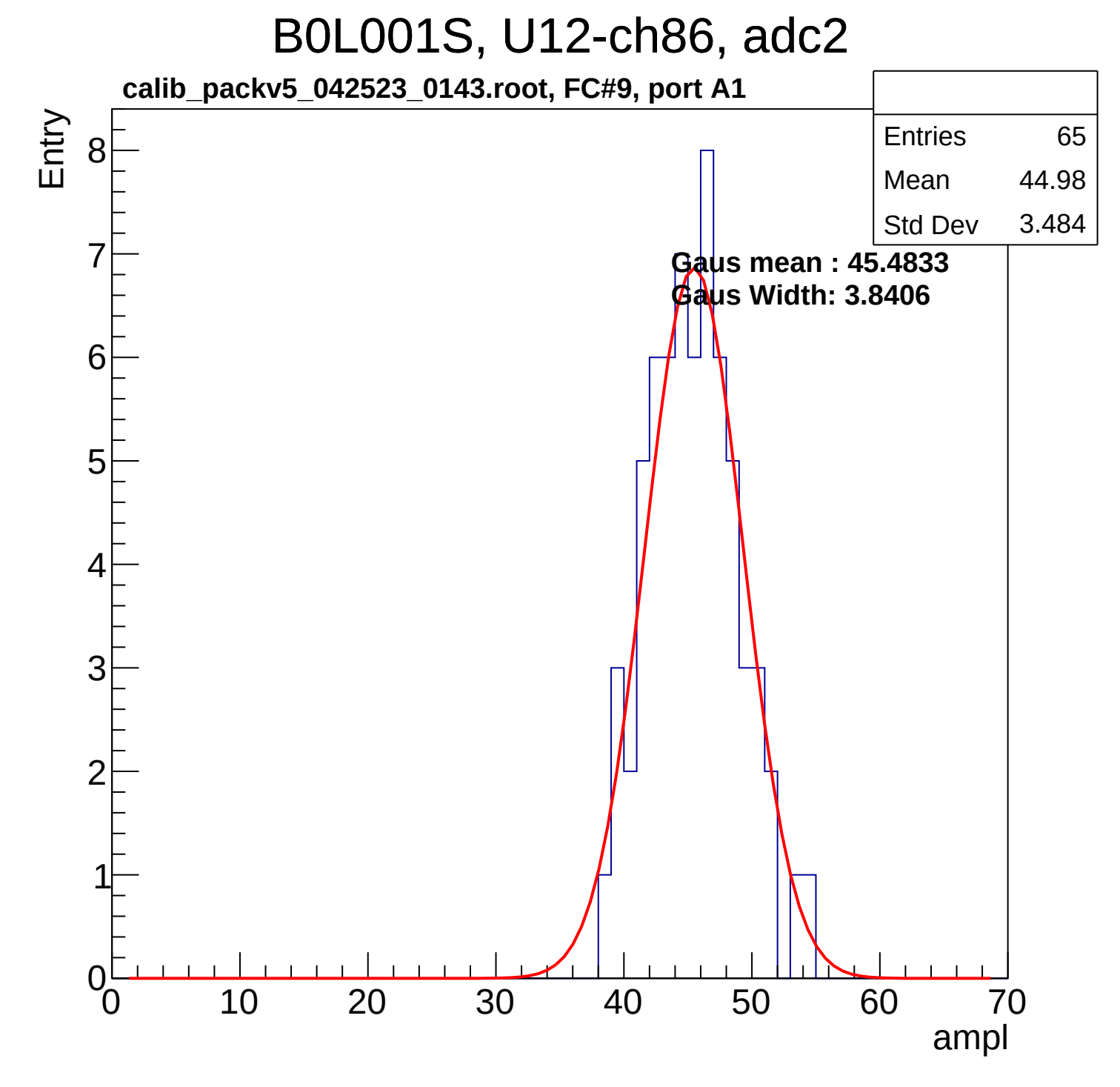
B0L001S, U12-ch86, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 65
Mean 44.98
Std Dev 3.484
Gaus mean : 45.4833
Gaus Width: 3.8406
Entry
ampl
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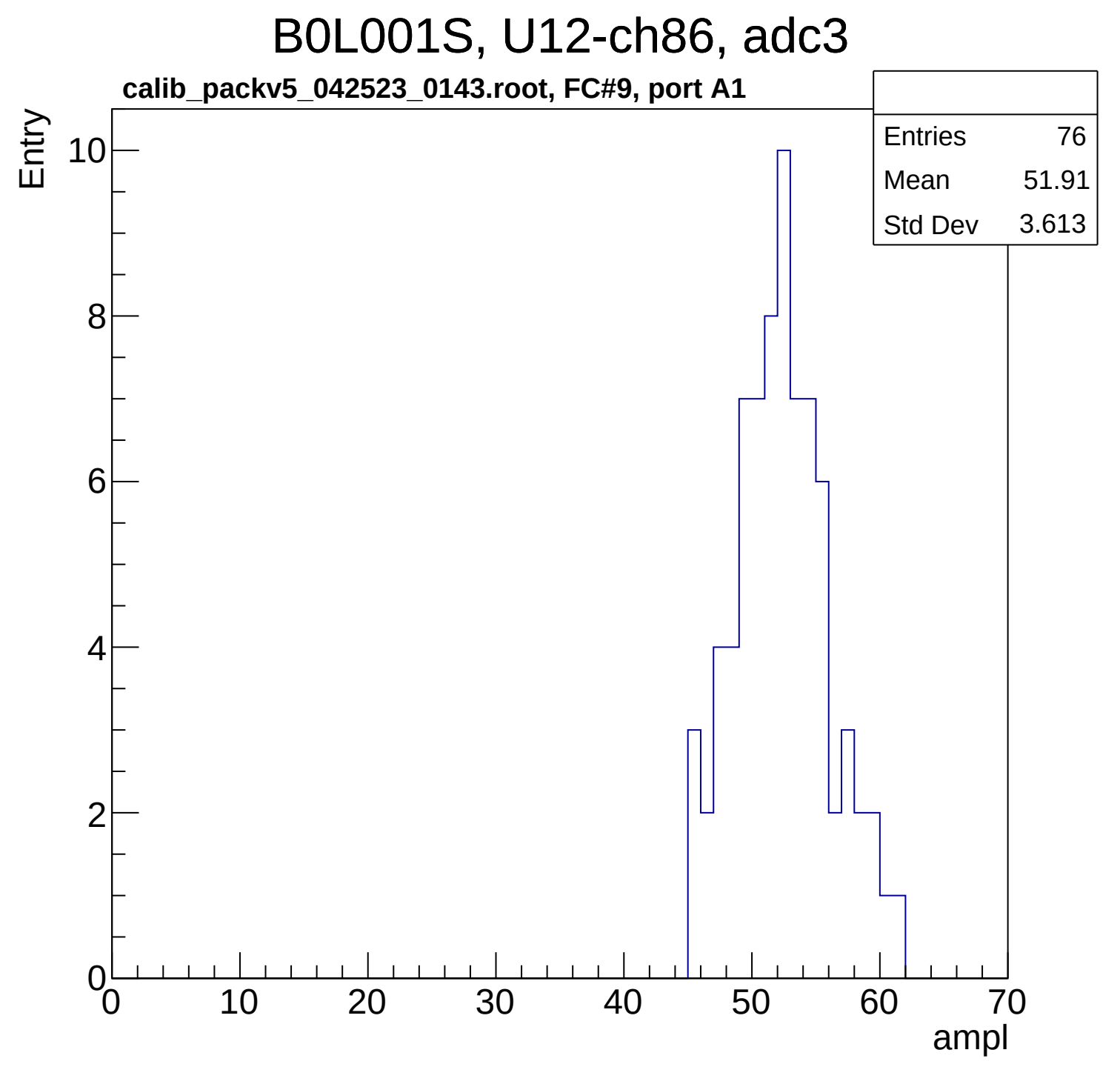
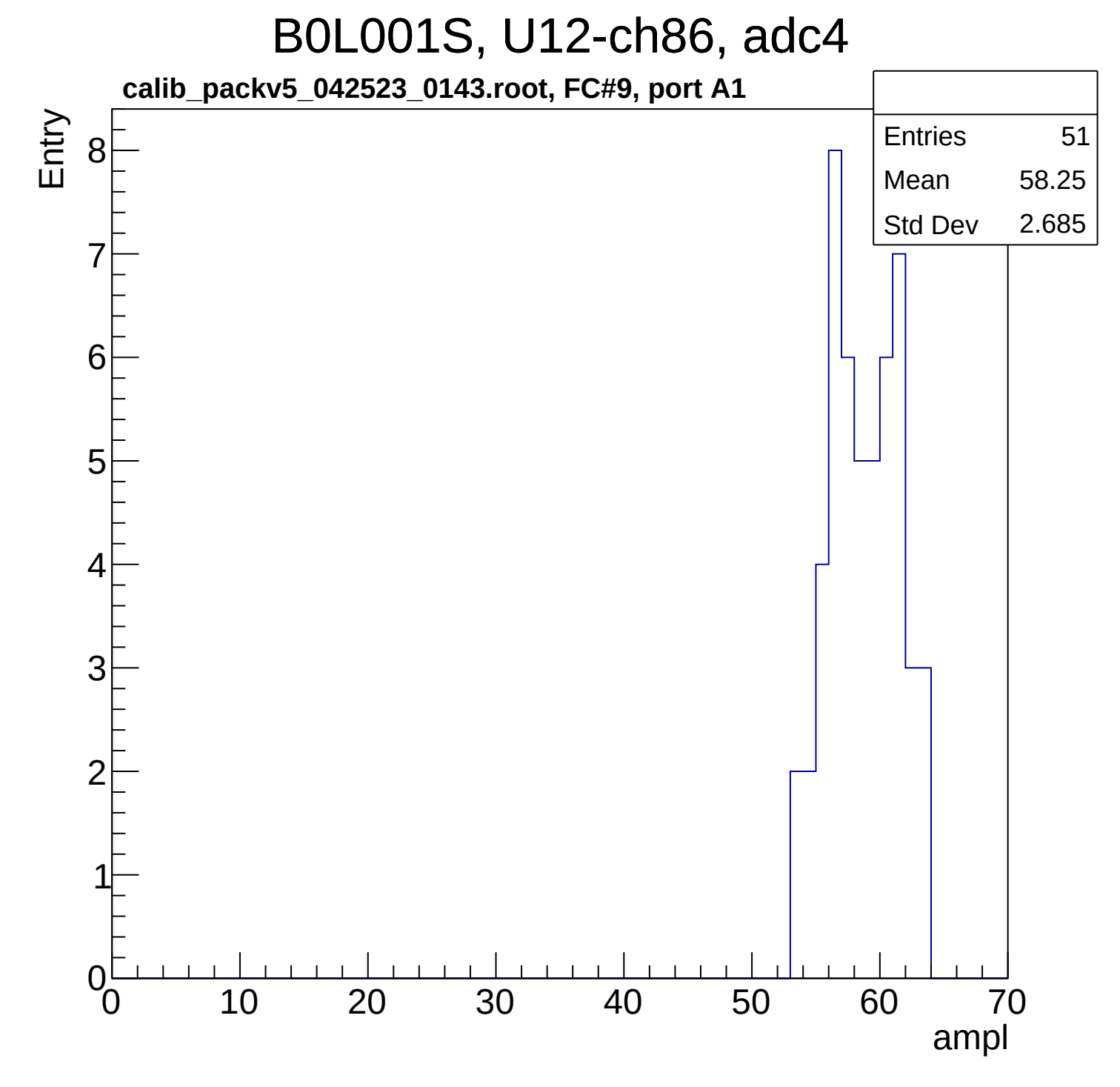
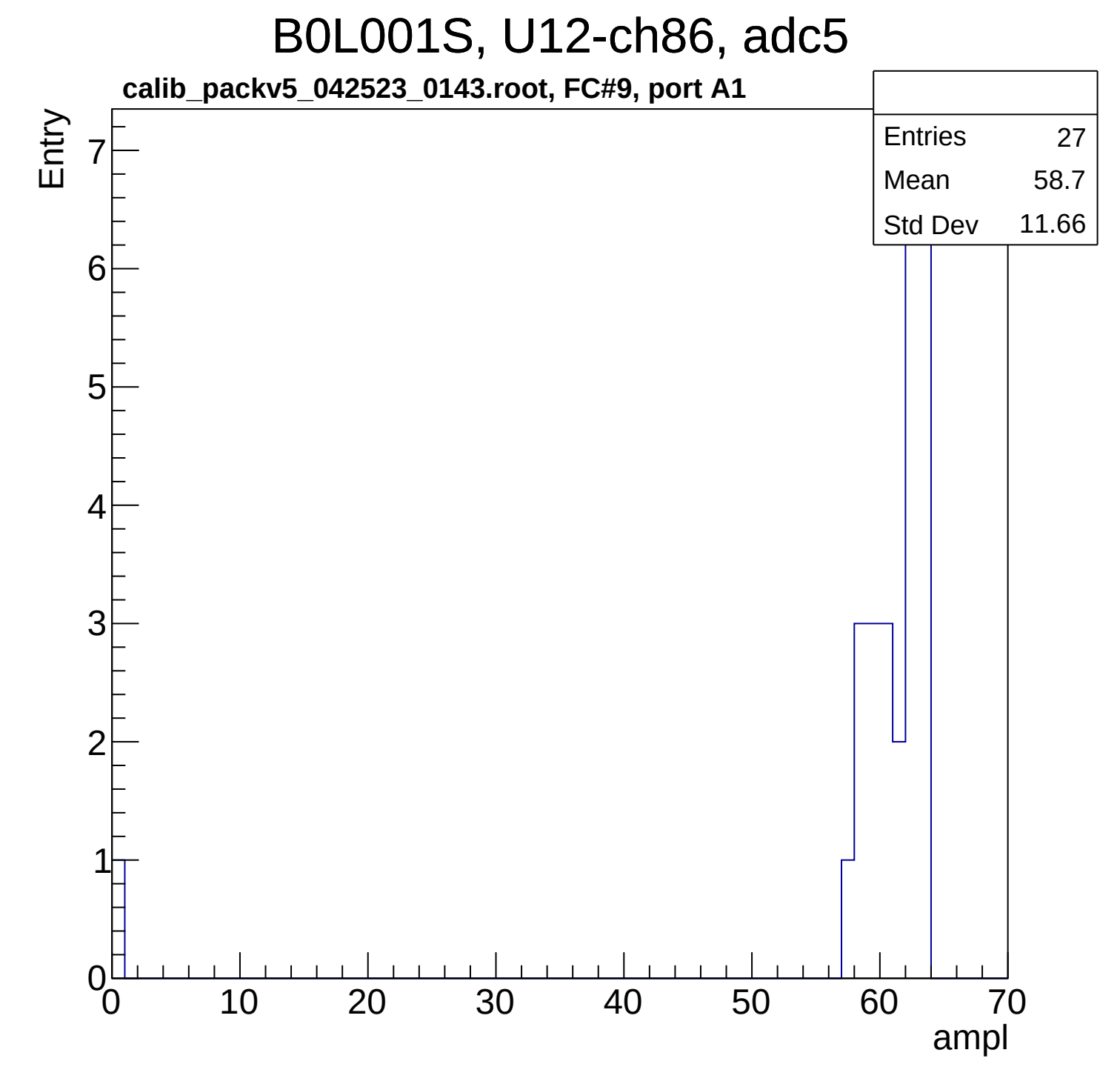
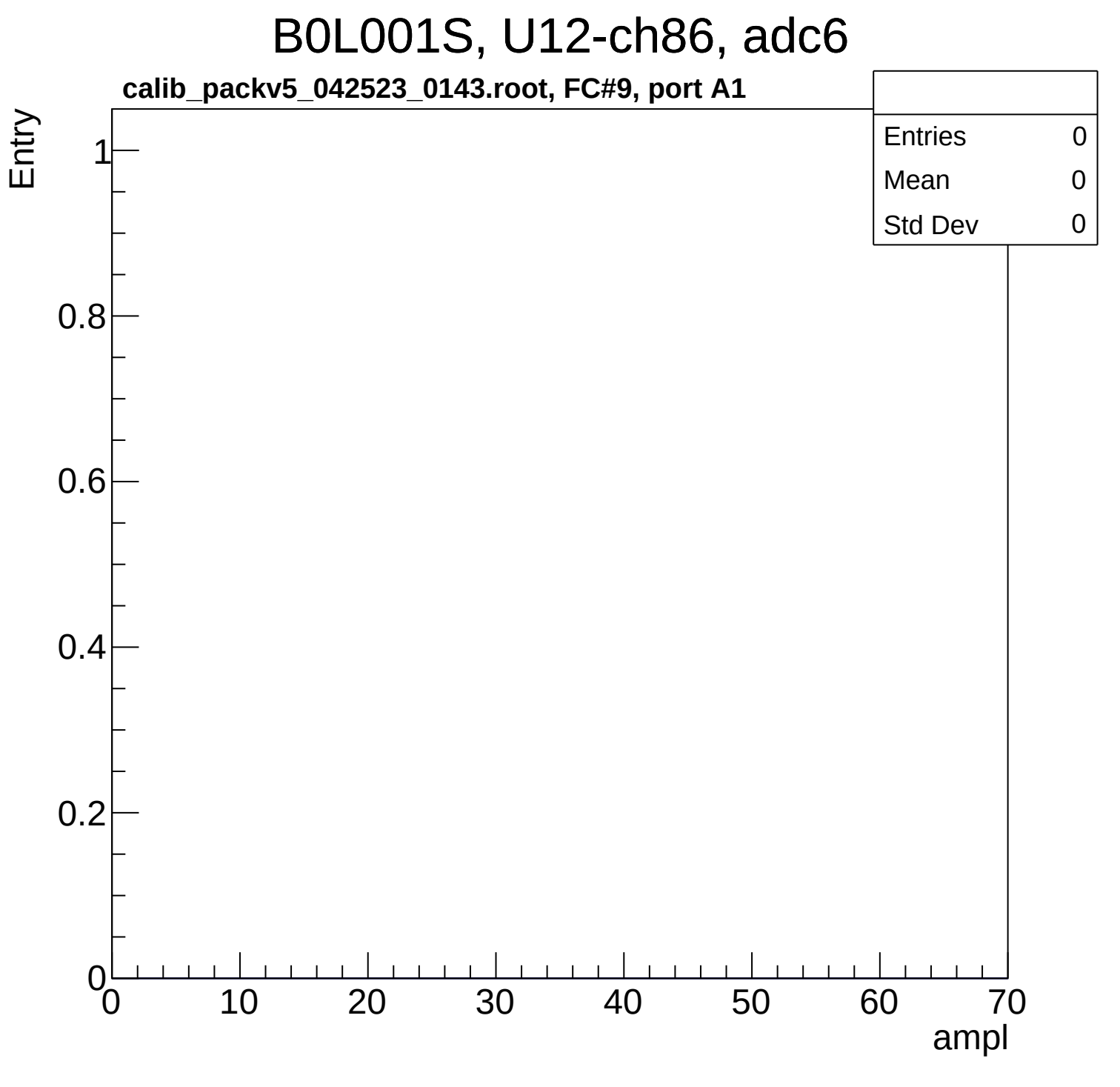
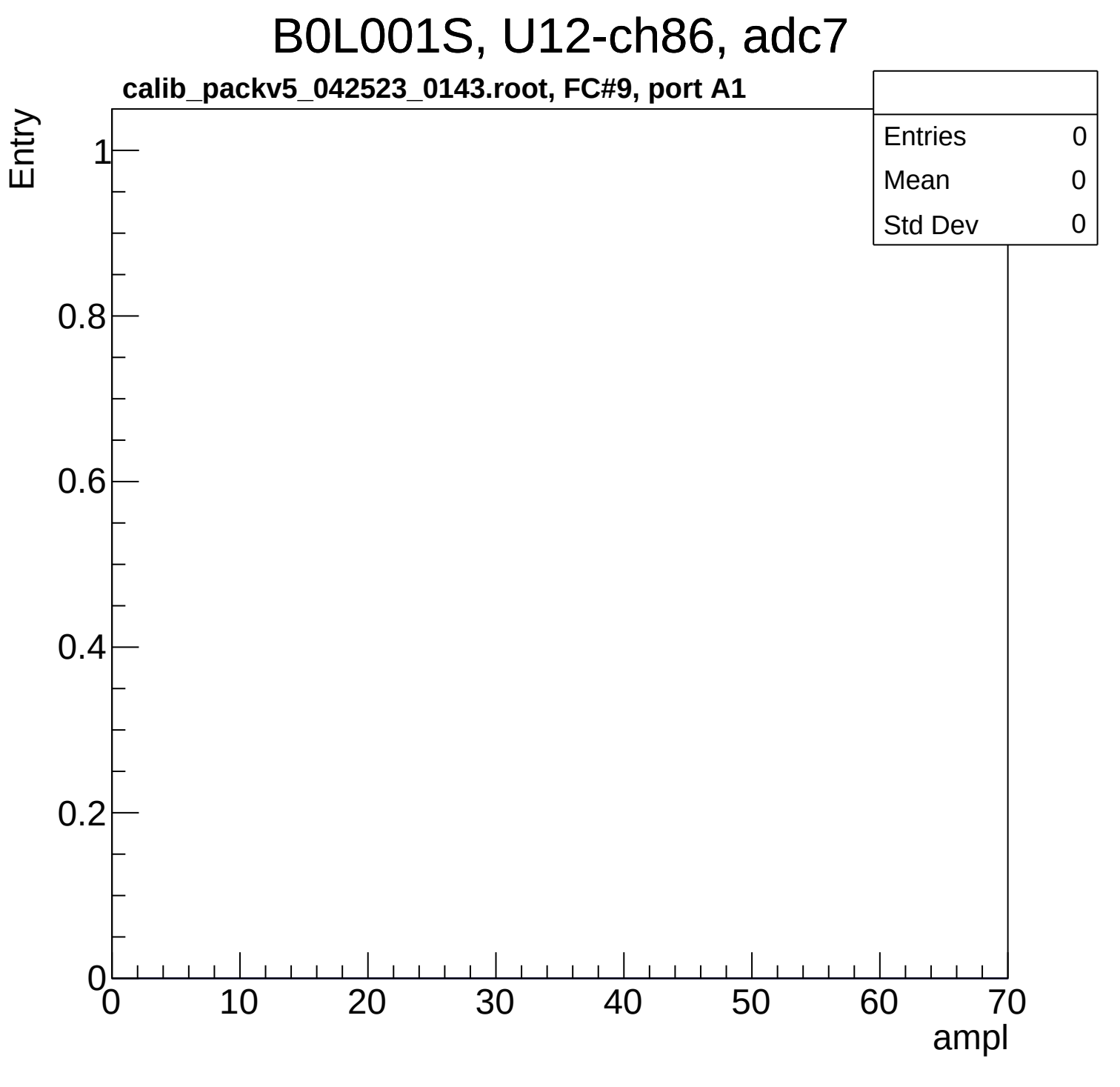
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

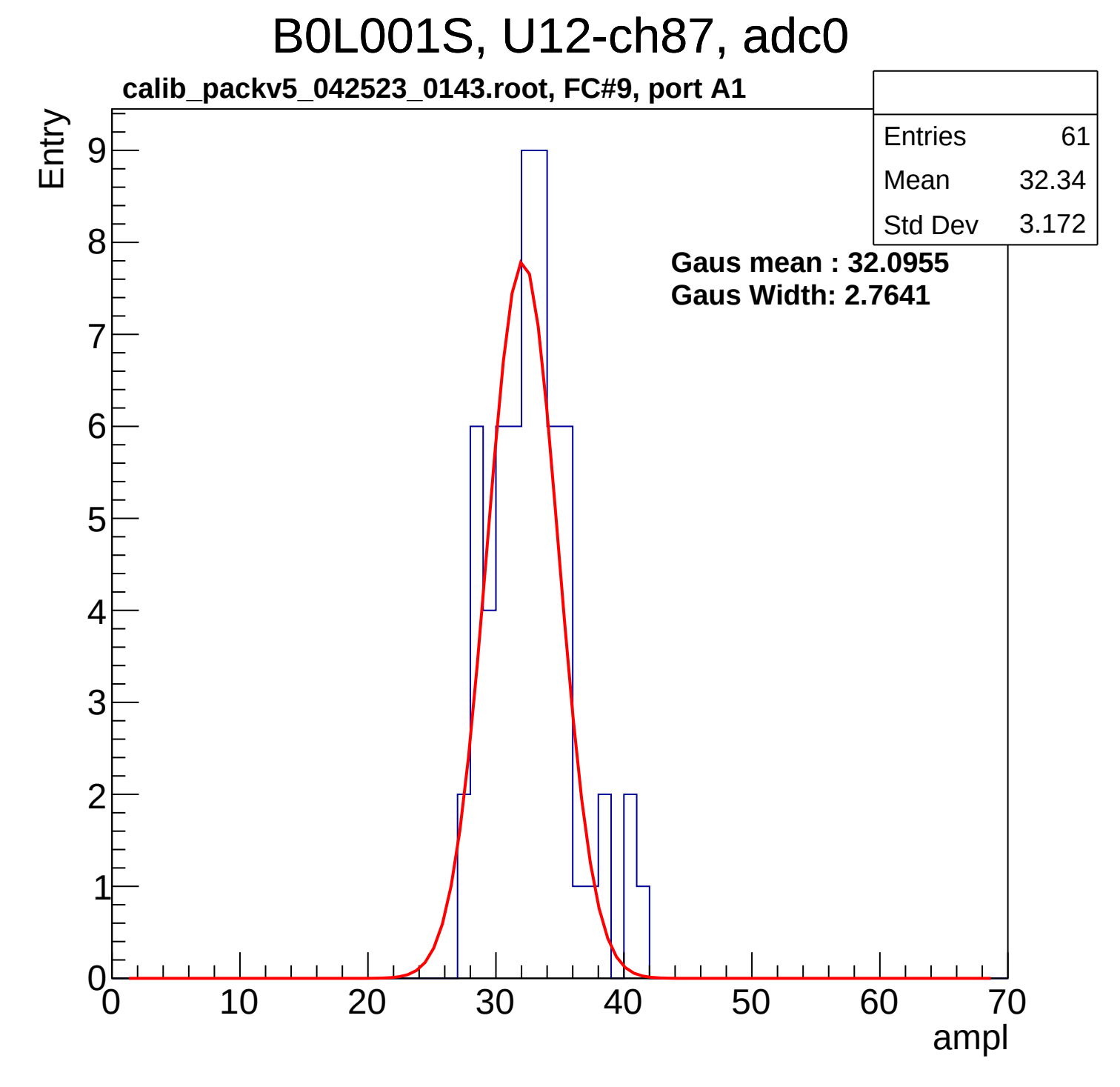

B0L001S, U12-ch86, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 76
Mean 51.91
Std Dev 3.613
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch86, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 51
Mean 58.25
Std Dev 2.685
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch86, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 27
Mean 58.7
Std Dev 11.66
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B0L001S, U12-ch86, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch86, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch87, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 61
Mean 32.34
Std Dev 3.172
Gaus mean : 32.0955
Gaus Width: 2.7641
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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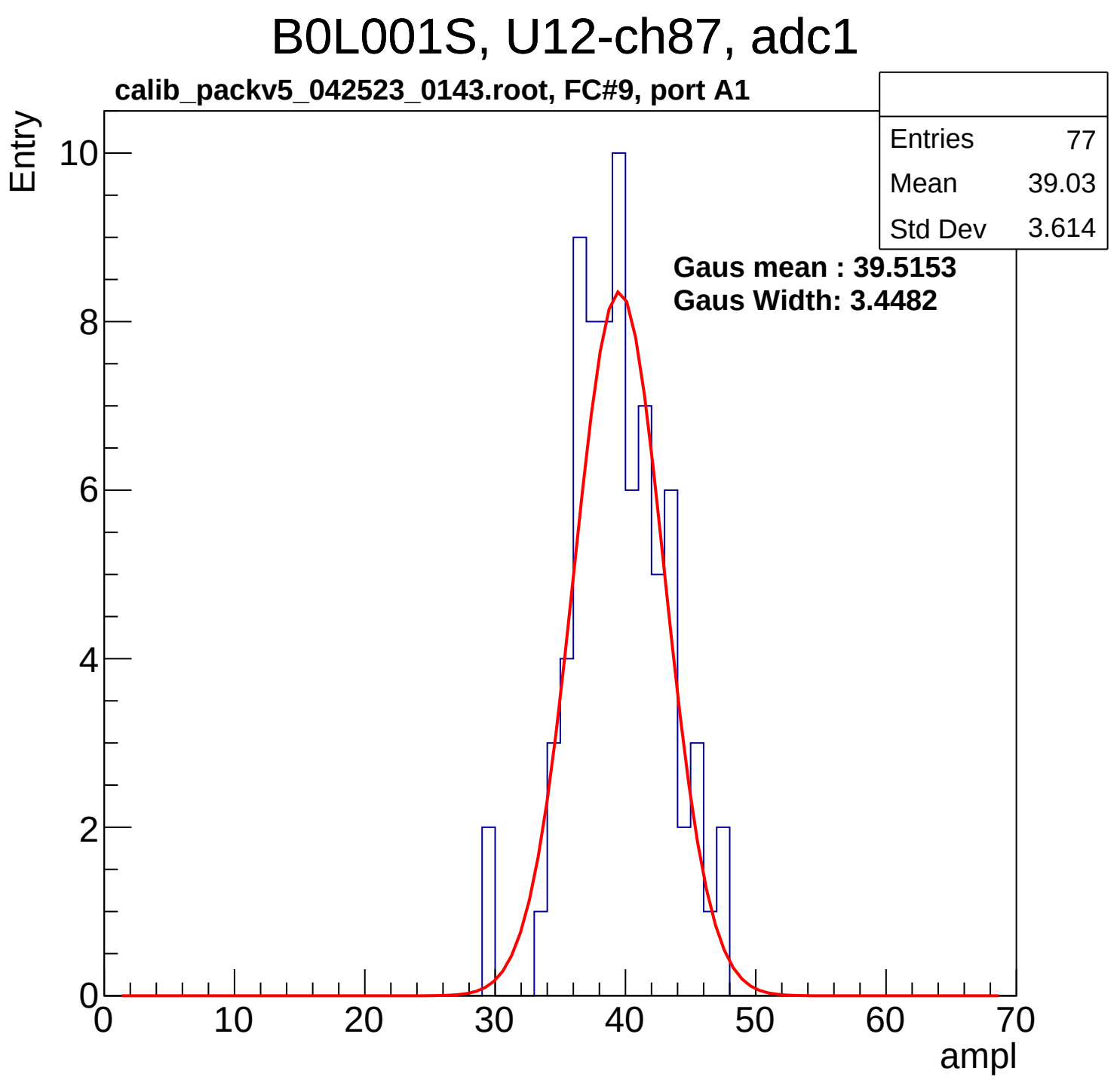
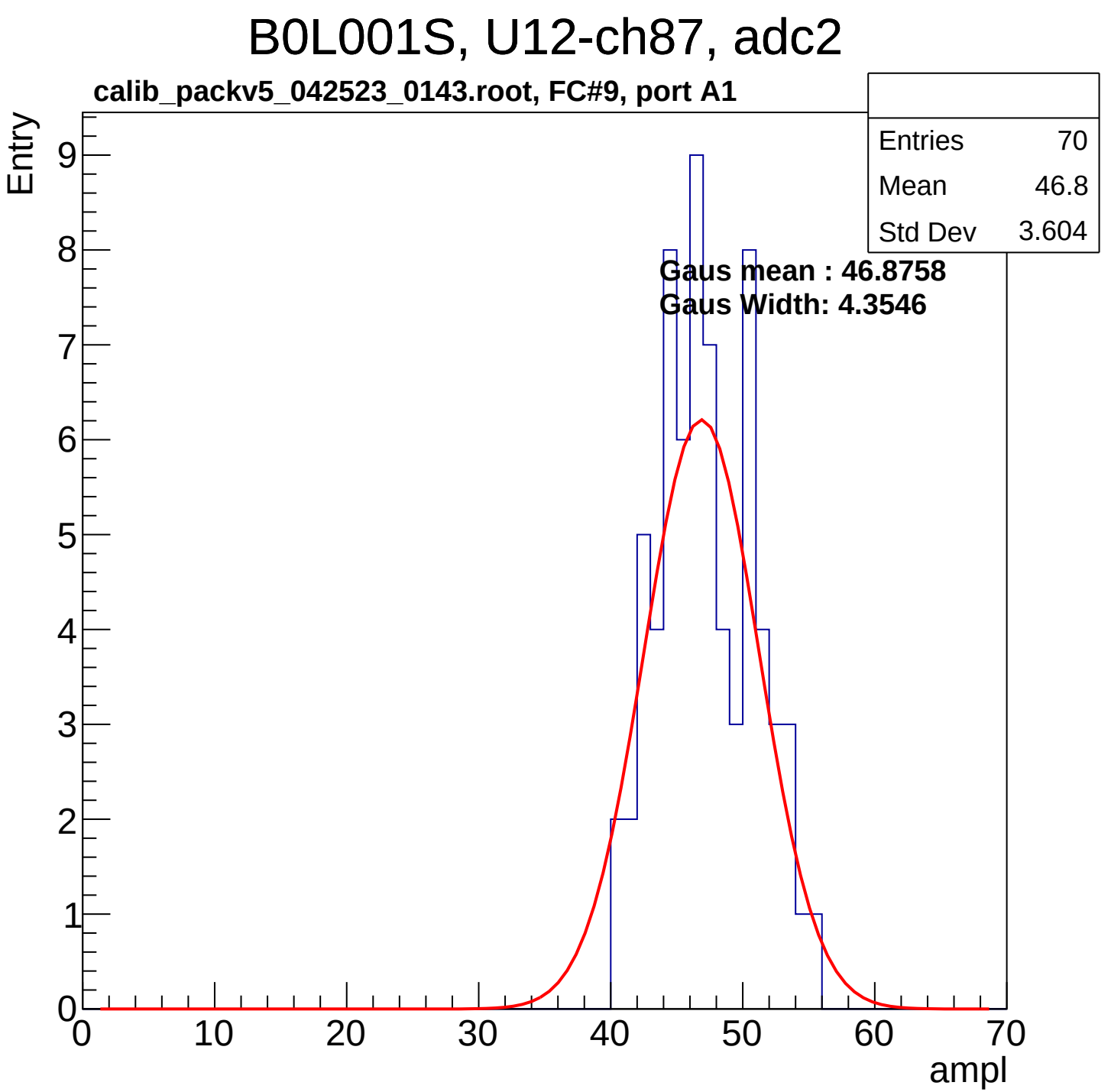
40
50
60
70


B0L001S, U12-ch87, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 77
Mean 39.03
Std Dev 3.614
Gaus mean : 39.5153
Gaus Width: 3.4482
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch87, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 70
Mean 46.8
Std Dev 3.604
Gaus mean : 46.8758
Gaus Width: 4.3546
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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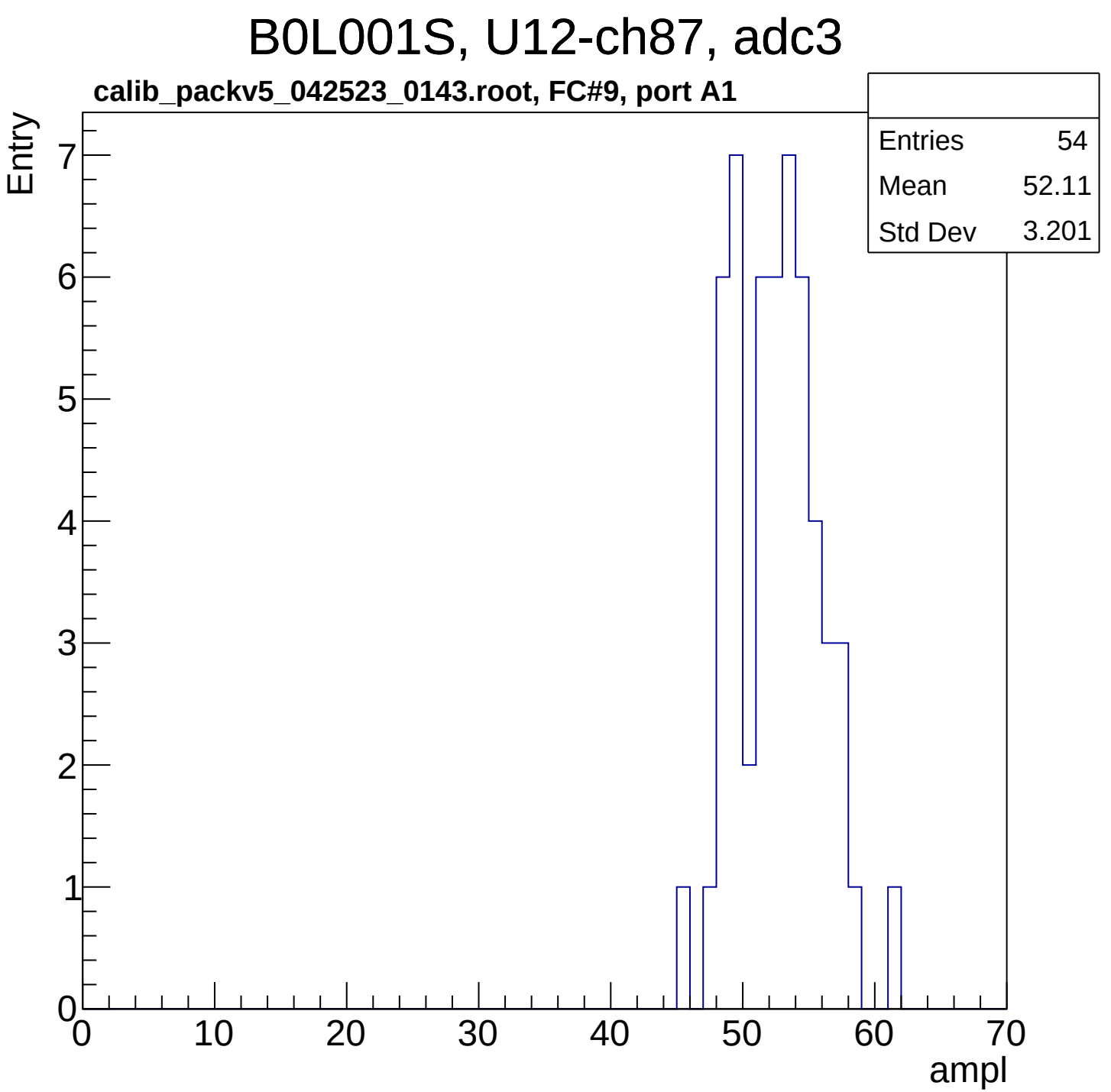
B0L001S, U12-ch87, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 54
Mean 52.11
Std Dev 3.201
Entry
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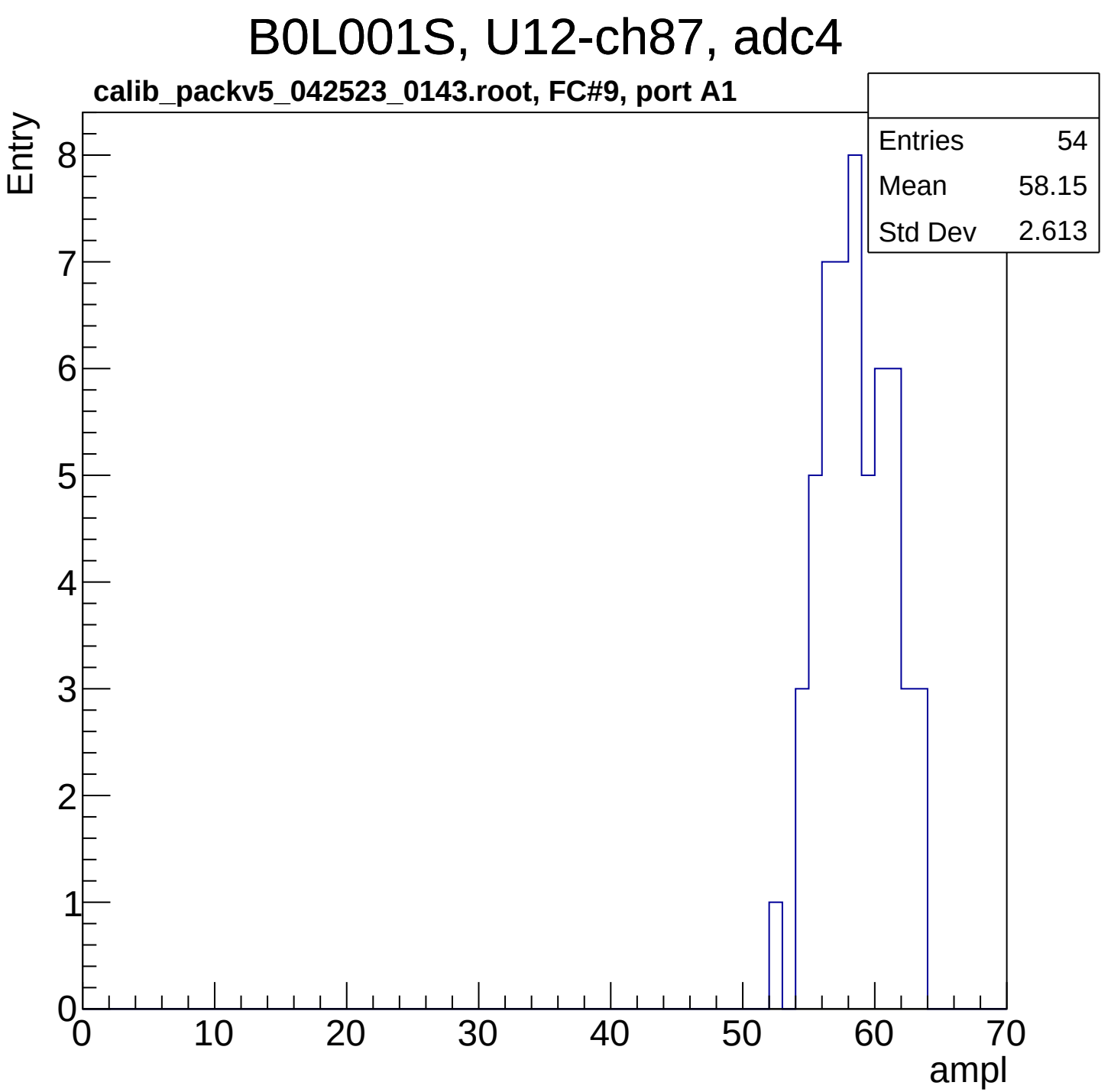
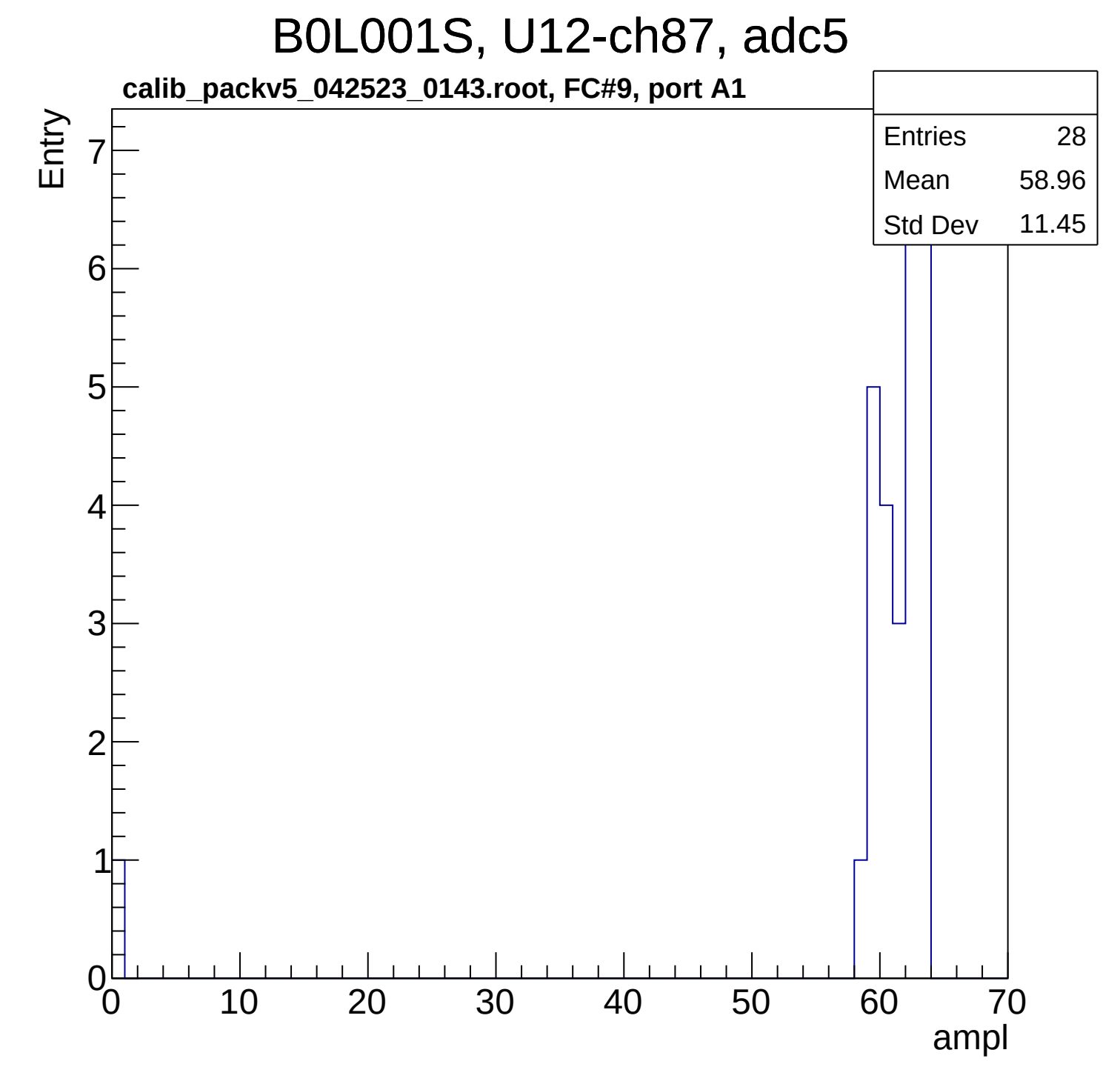
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch87, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 54
Mean 58.15
Std Dev 2.613
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch87, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 28
Mean 58.96
Std Dev 11.45
Entry
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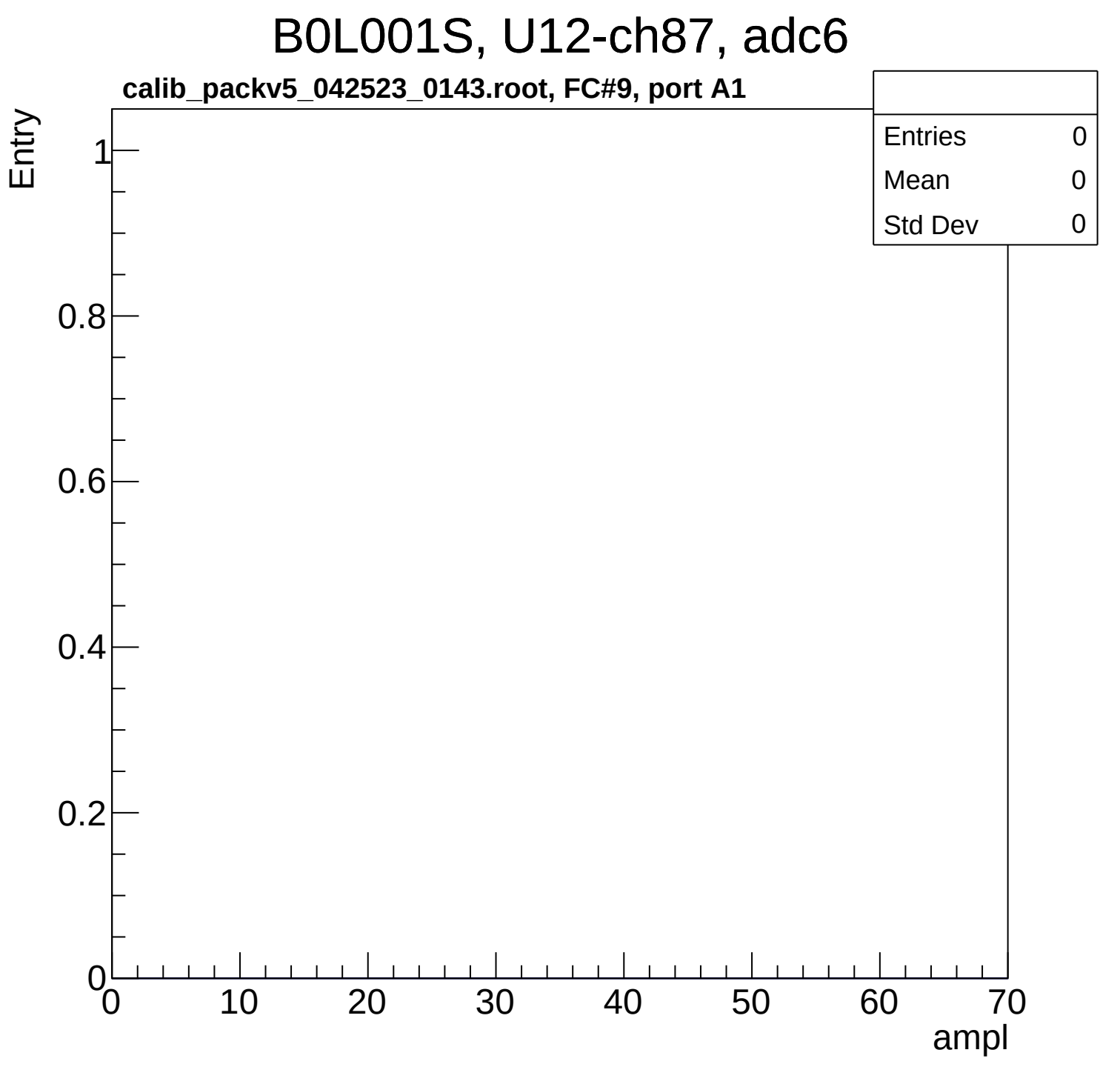
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch87, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
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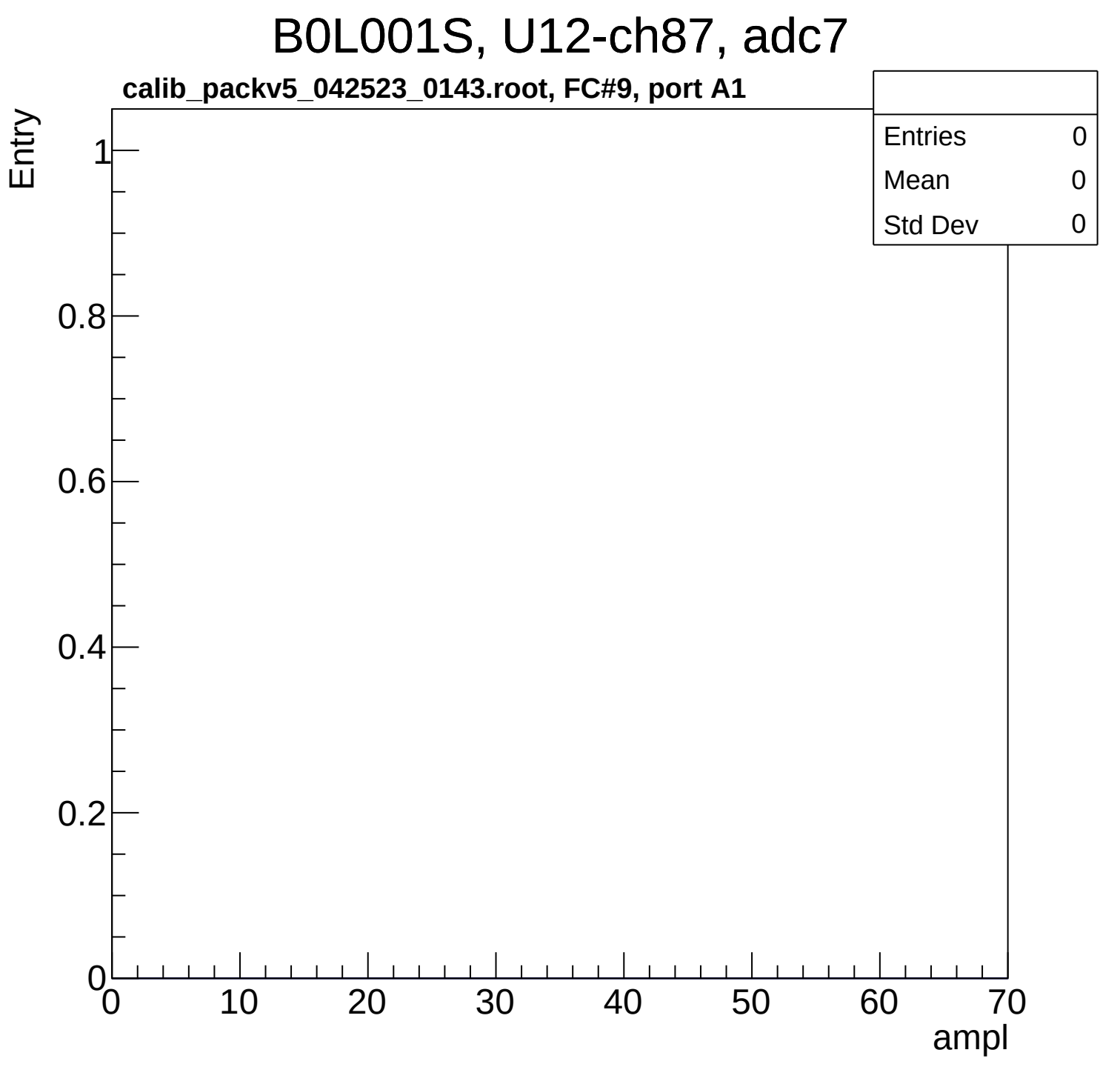
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch87, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
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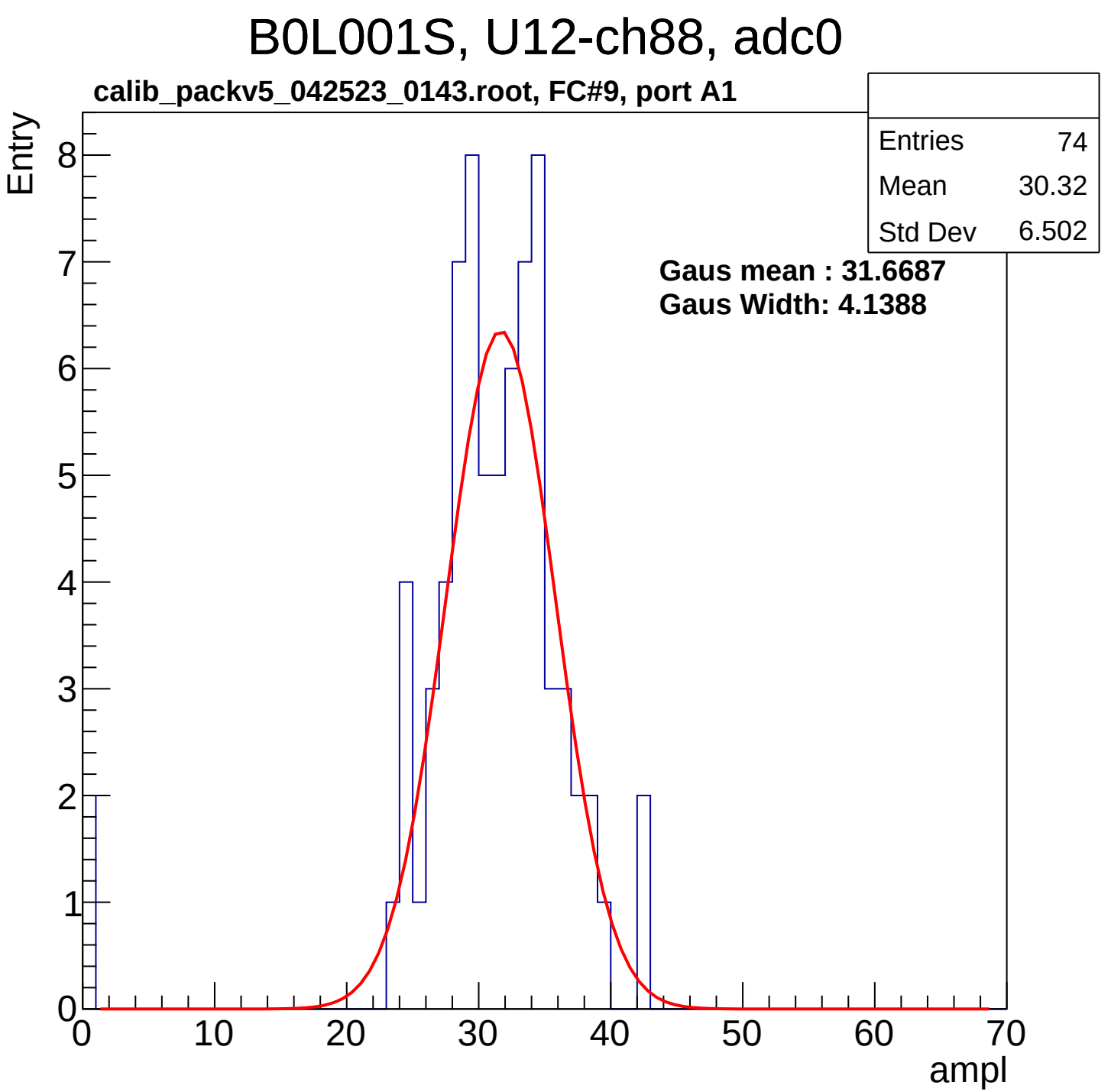
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch88, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 74
Mean 30.32
Std Dev 6.502
Gaus mean : 31.6687
Gaus Width: 4.1388
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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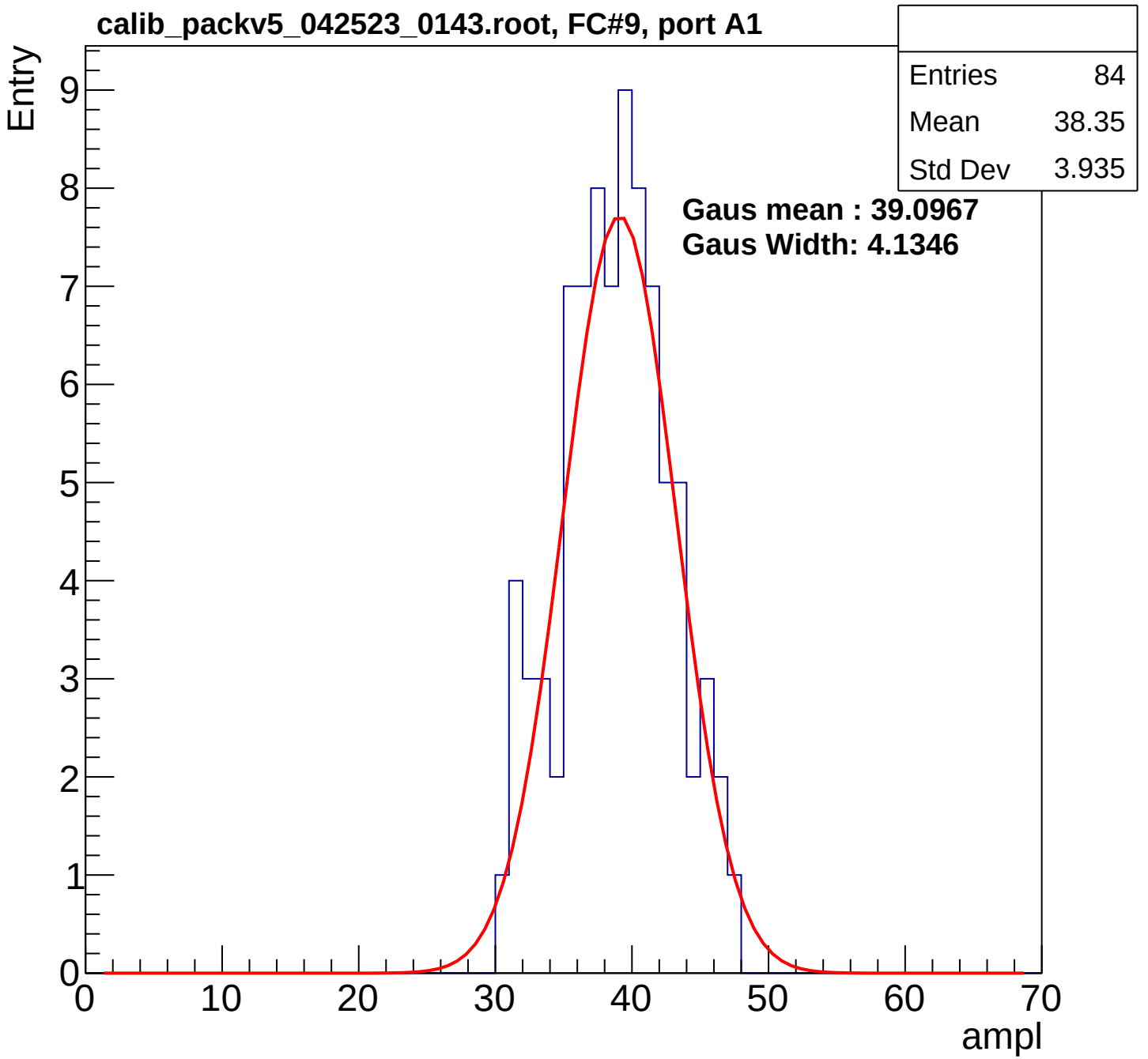
B0L001S, U12-ch88, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 84
Mean 38.35
Std Dev 3.935
Gaus mean : 39.0967
Gaus Width: 4.1346
Entry
ampl
0
1
2
3
4
5
6
7
8
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0
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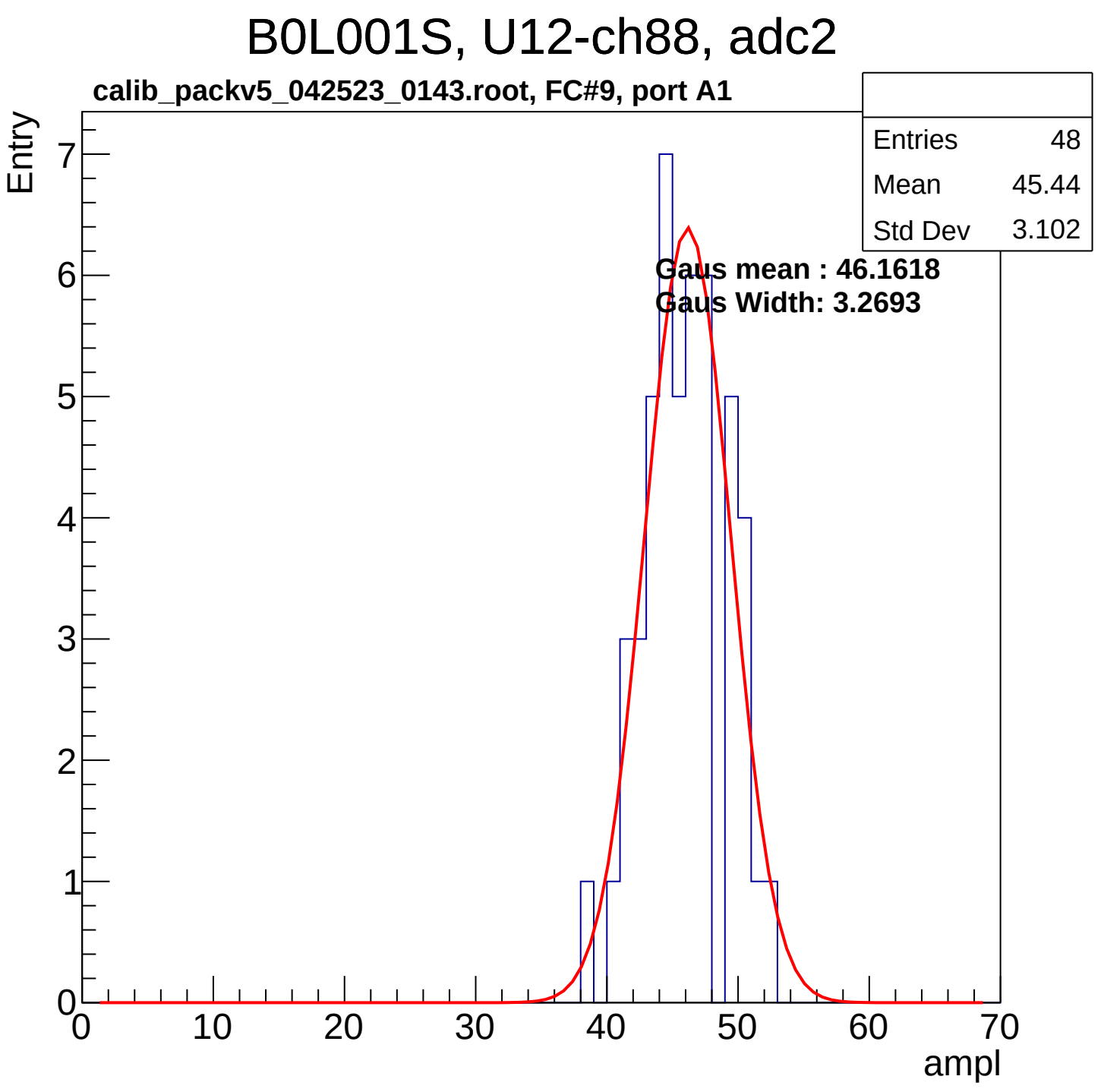
B0L001S, U12-ch88, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 48
Mean 45.44
Std Dev 3.102
Gaus mean : 46.1618
Gaus Width: 3.2693
Entry
ampl
0
1
2
3
4
5
6
7
0
10
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40
50
60
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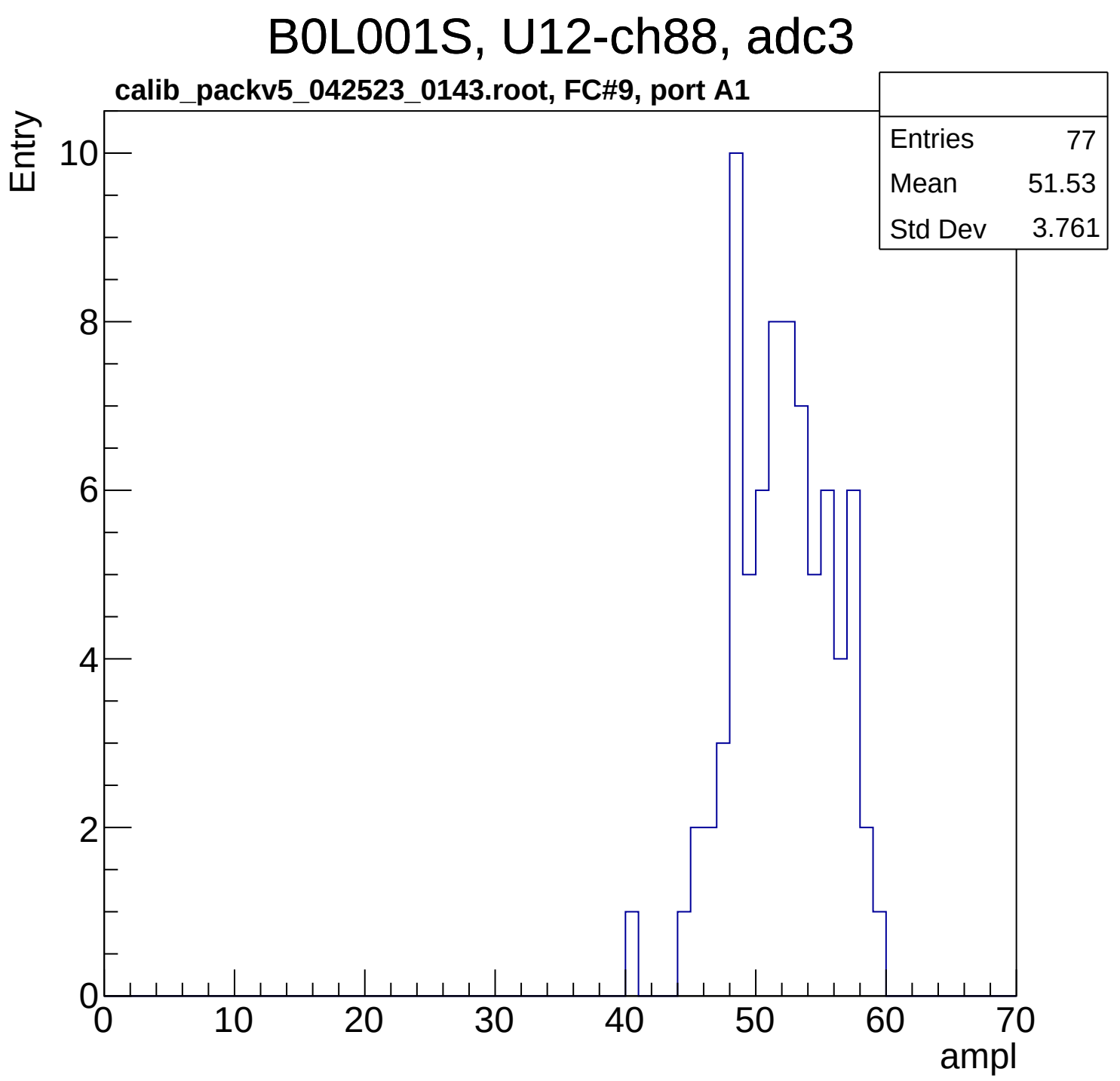
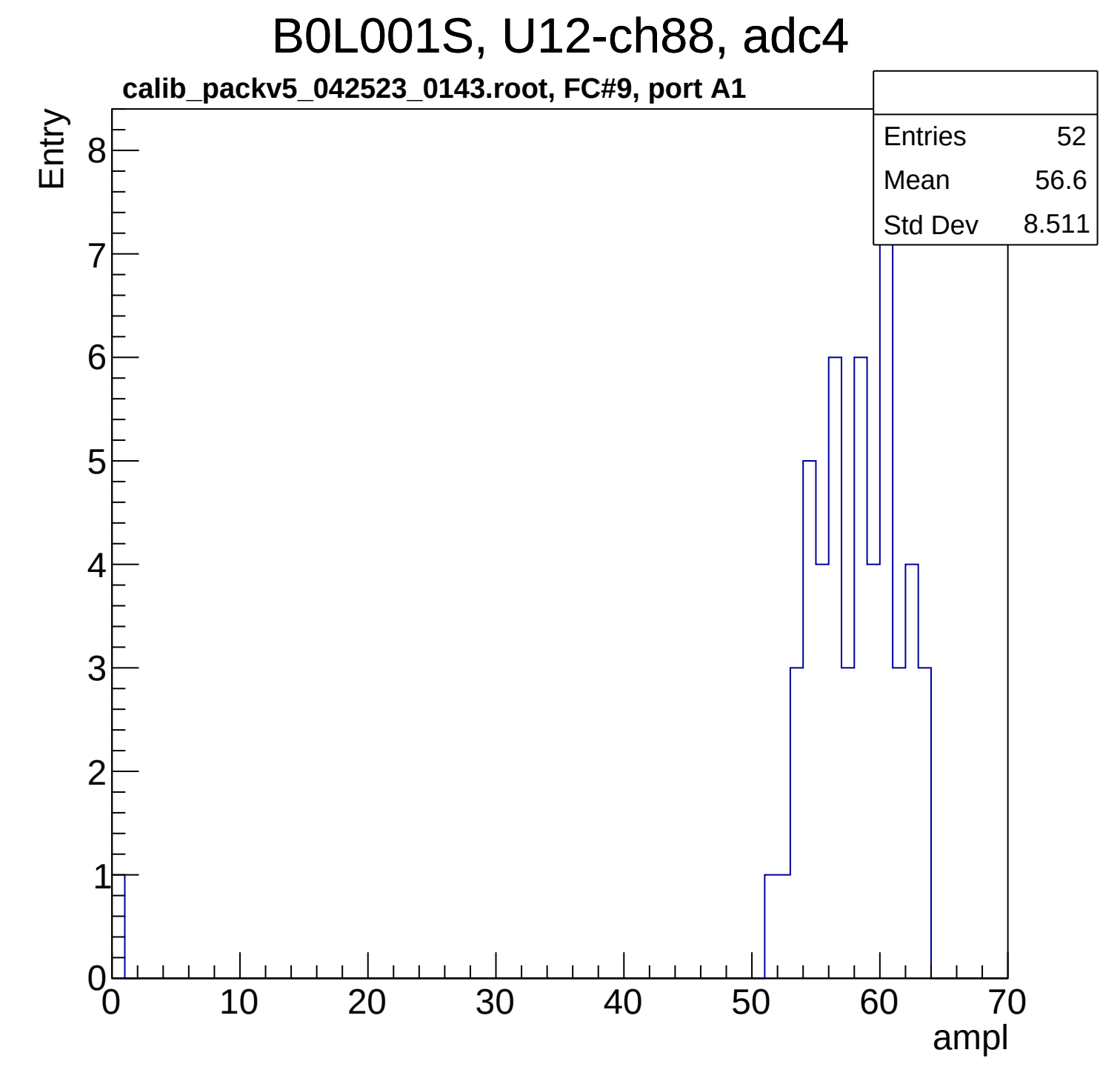
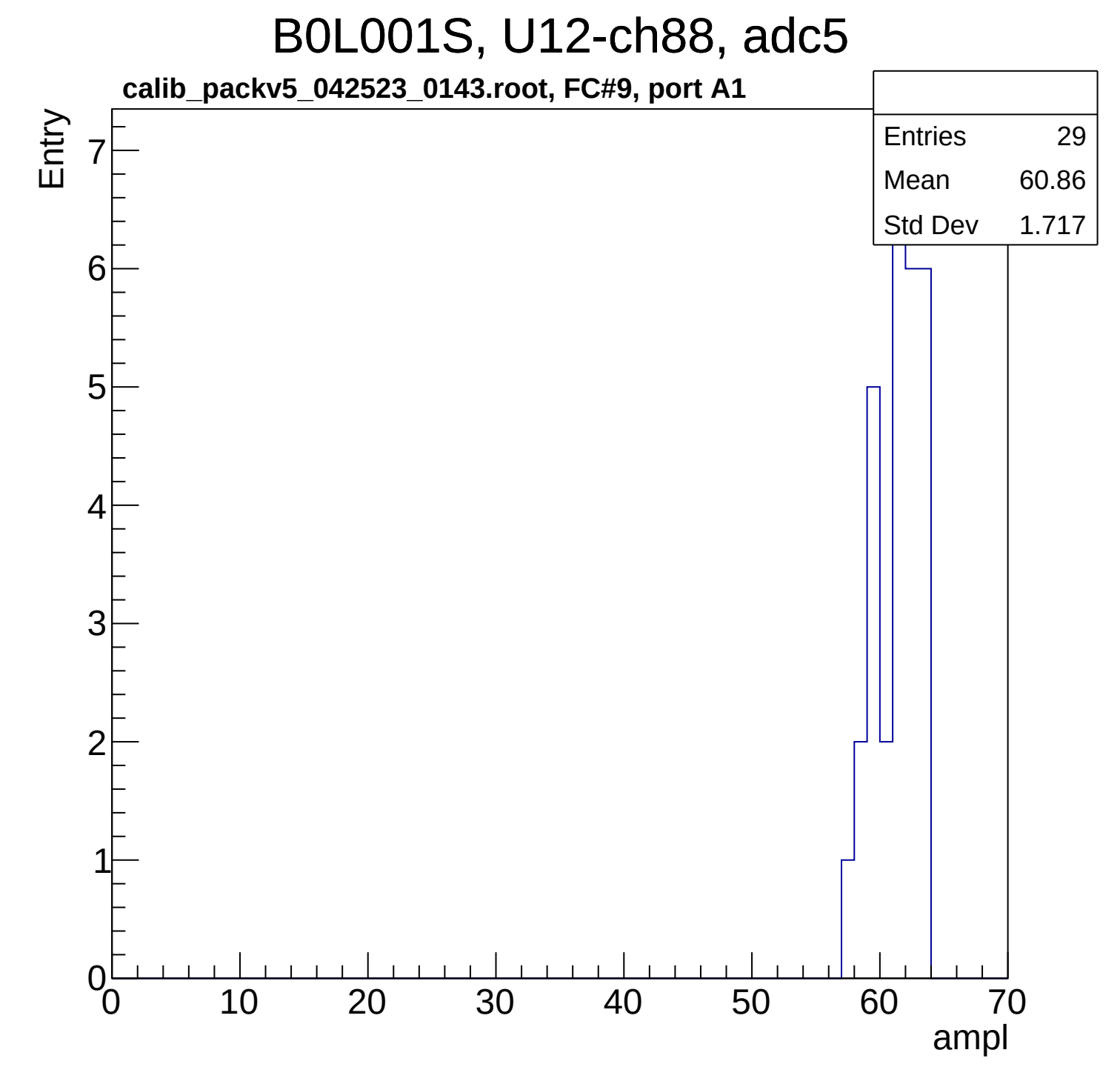

B0L001S, U12-ch88, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 77
Mean 51.53
Std Dev 3.761
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch88, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 52
Mean 56.6
Std Dev 8.511
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch88, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 29
Mean 60.86
Std Dev 1.717
Entry
ampl
0
1
2
3
4
5
6
7
0
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40
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60
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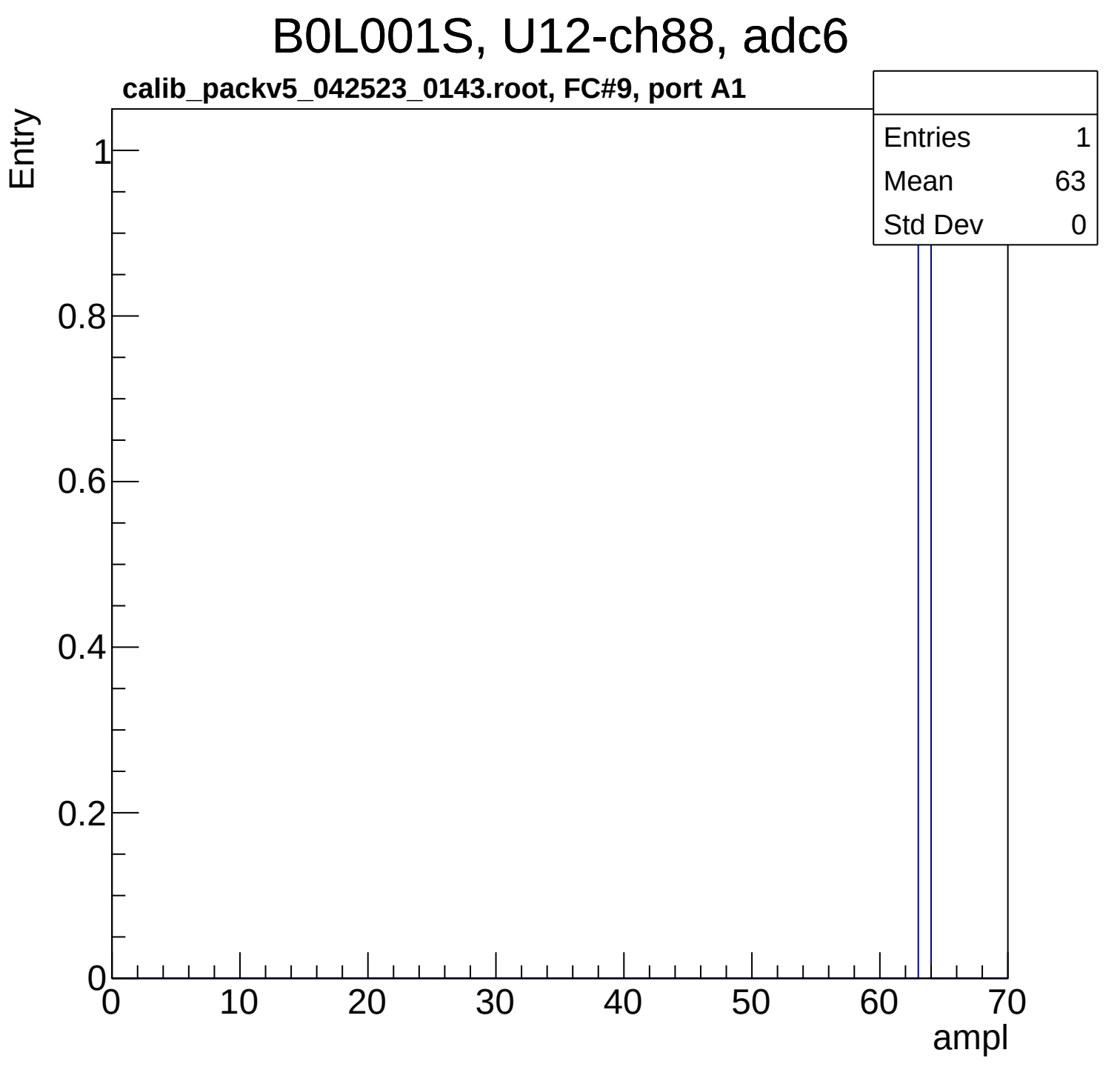
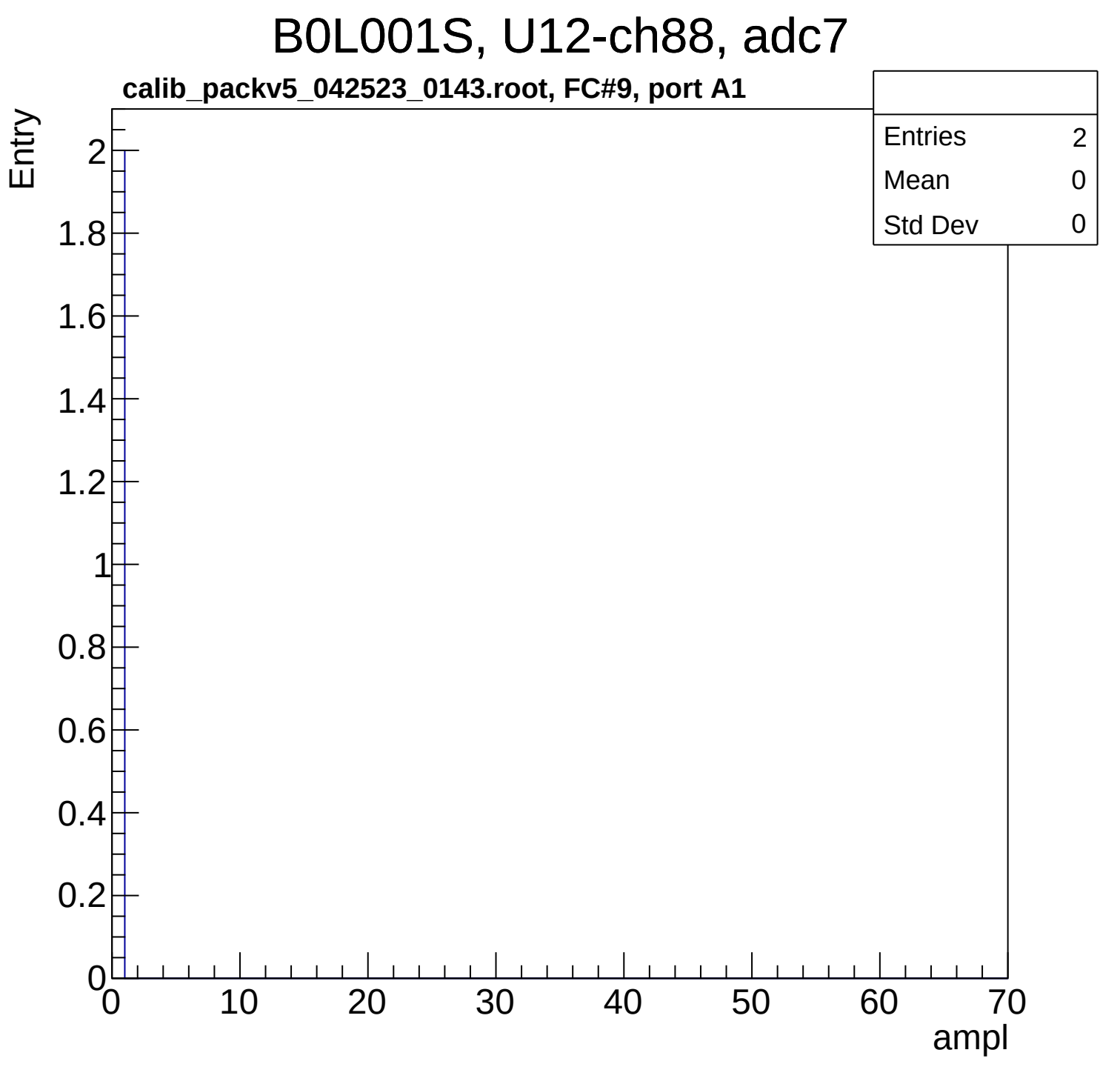
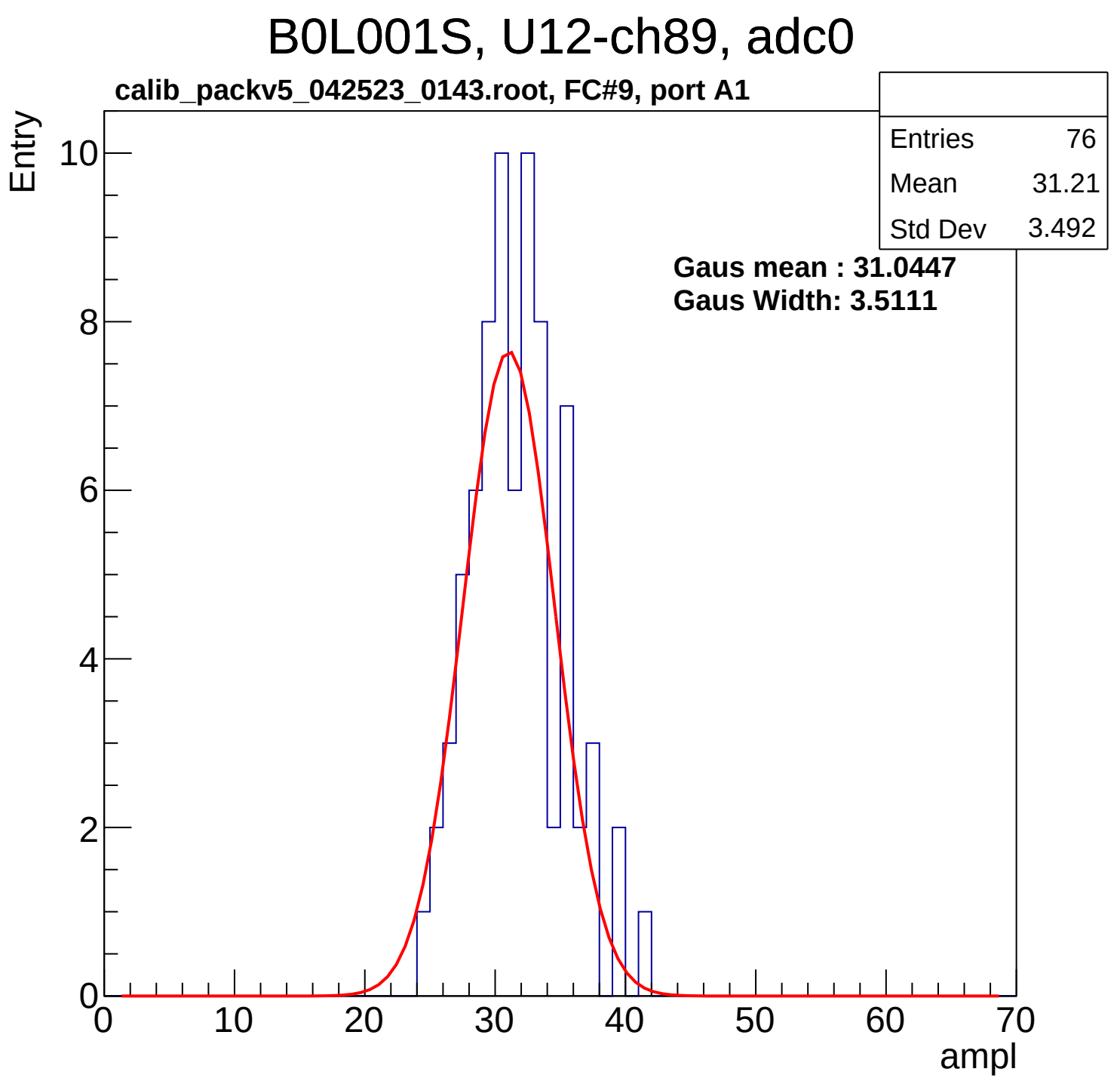
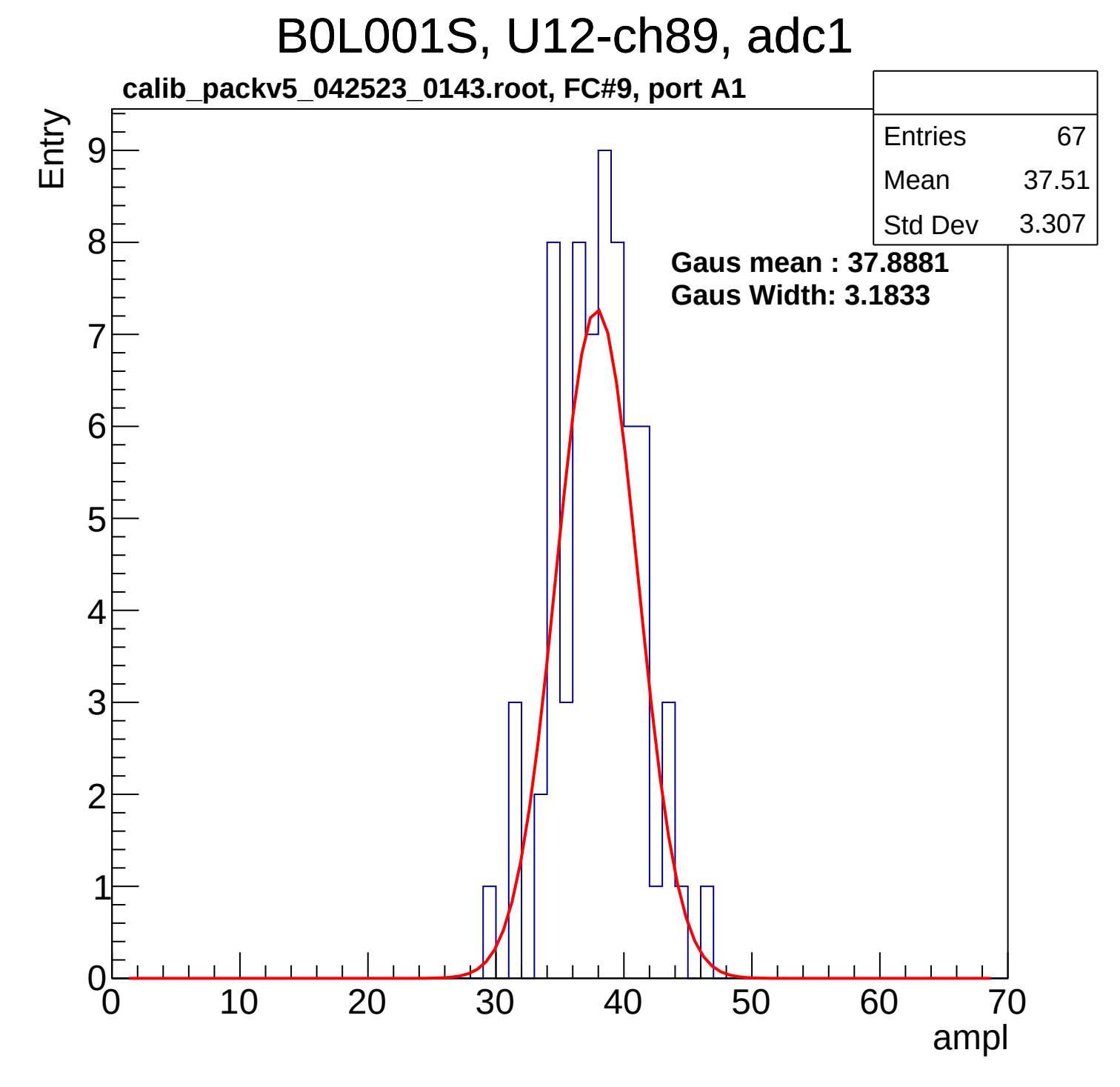

B0L001S, U12-ch88, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch88, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch89, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 76
Mean 31.21
Std Dev 3.492
Gaus mean : 31.0447
Gaus Width: 3.5111
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch89, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 67
Mean 37.51
Std Dev 3.307
Gaus mean : 37.8881
Gaus Width: 3.1833
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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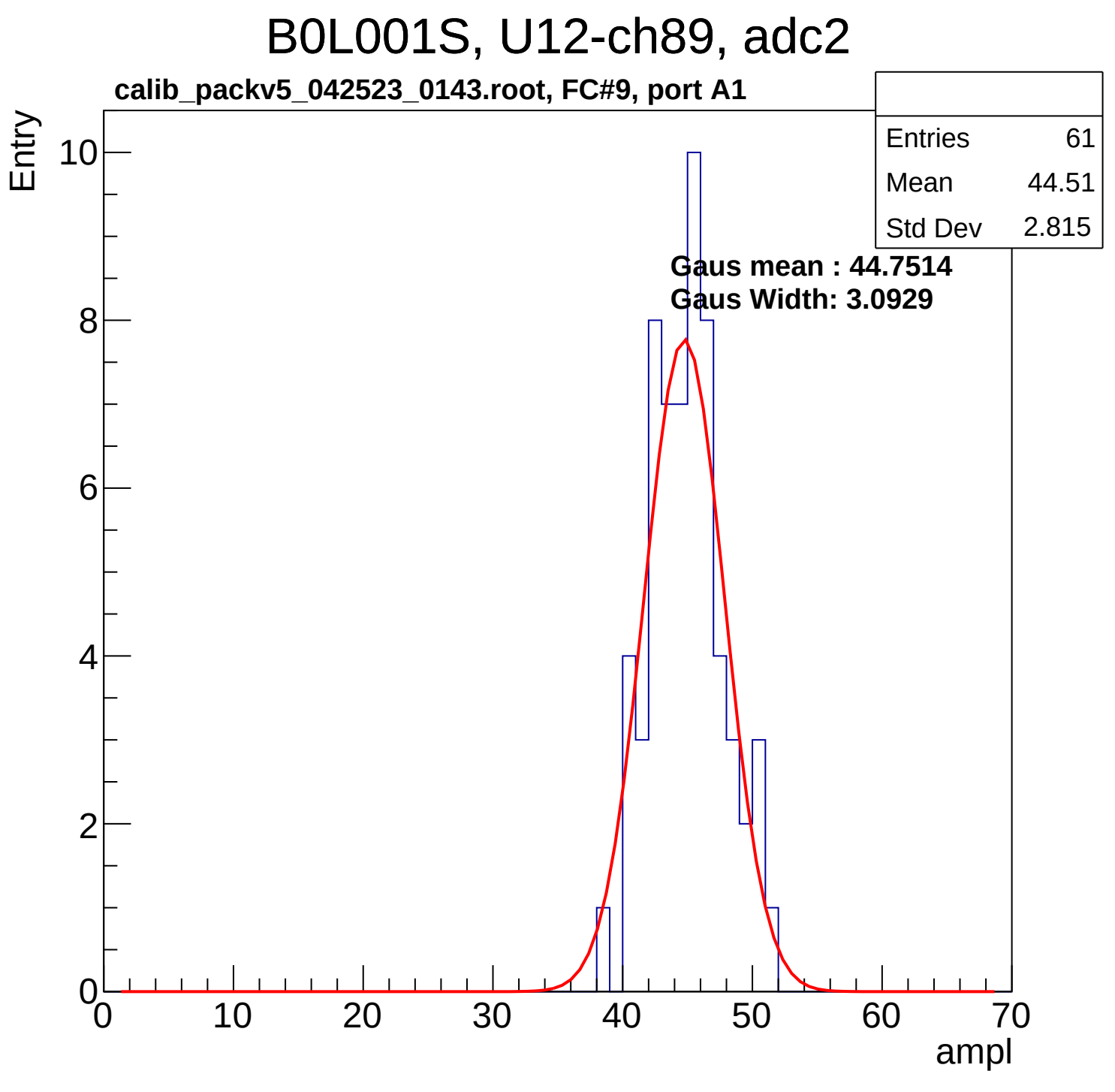
B0L001S, U12-ch89, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 61
Mean 44.51
Std Dev 2.815
Gaus mean : 44.7514
Gaus Width: 3.0929
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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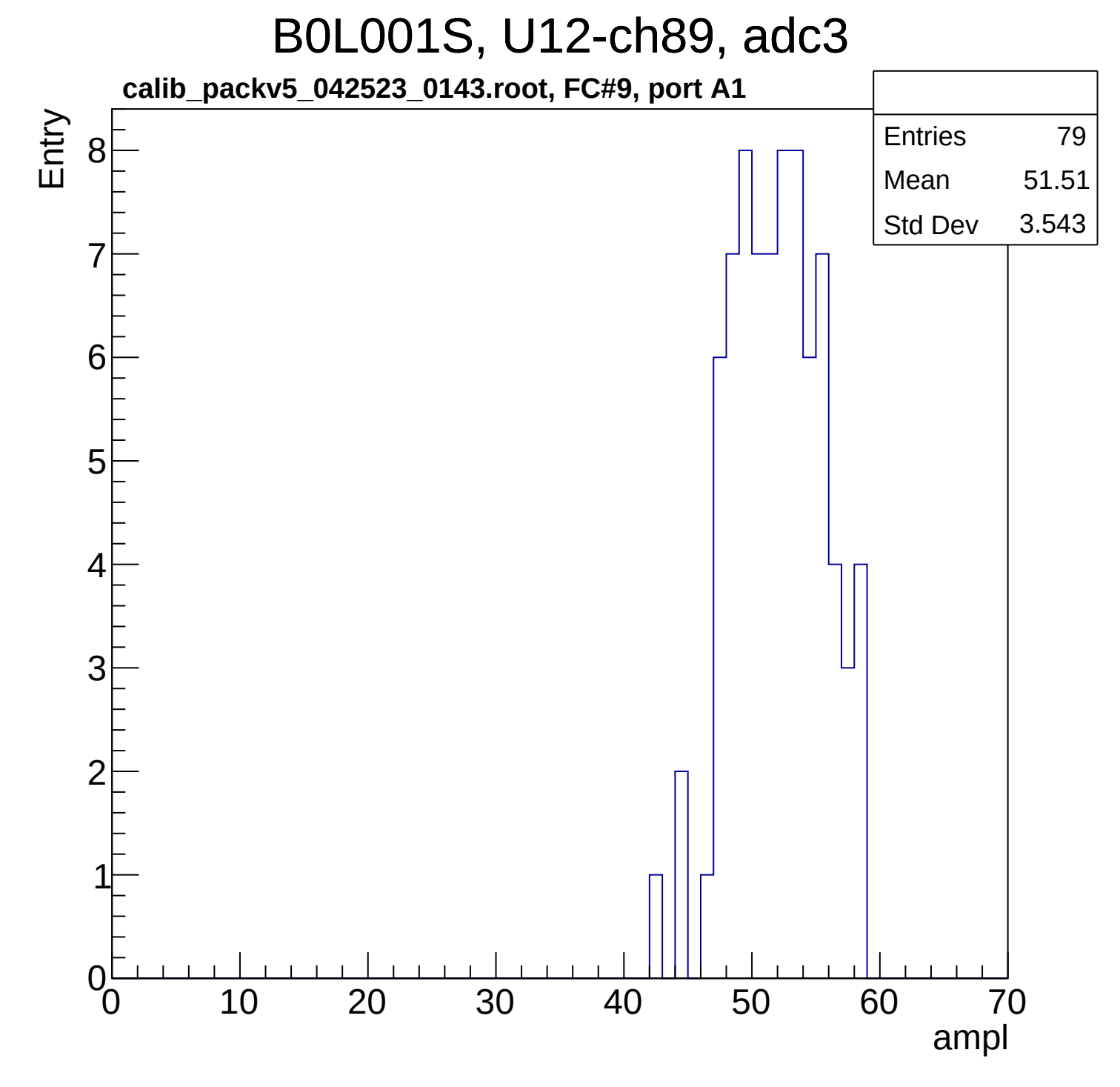
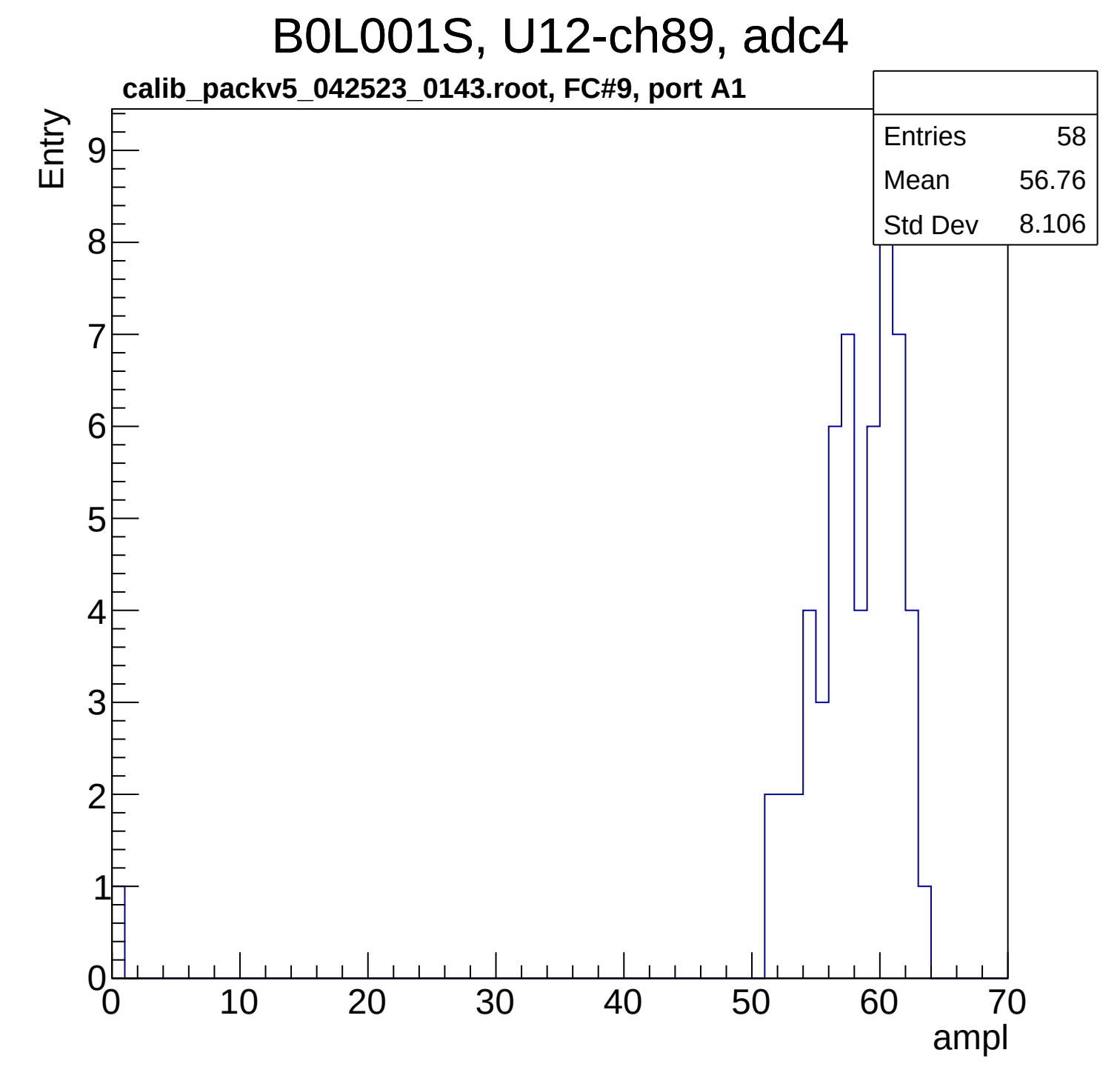

B0L001S, U12-ch89, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 79
Mean 51.51
Std Dev 3.543
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch89, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 58
Mean 56.76
Std Dev 8.106
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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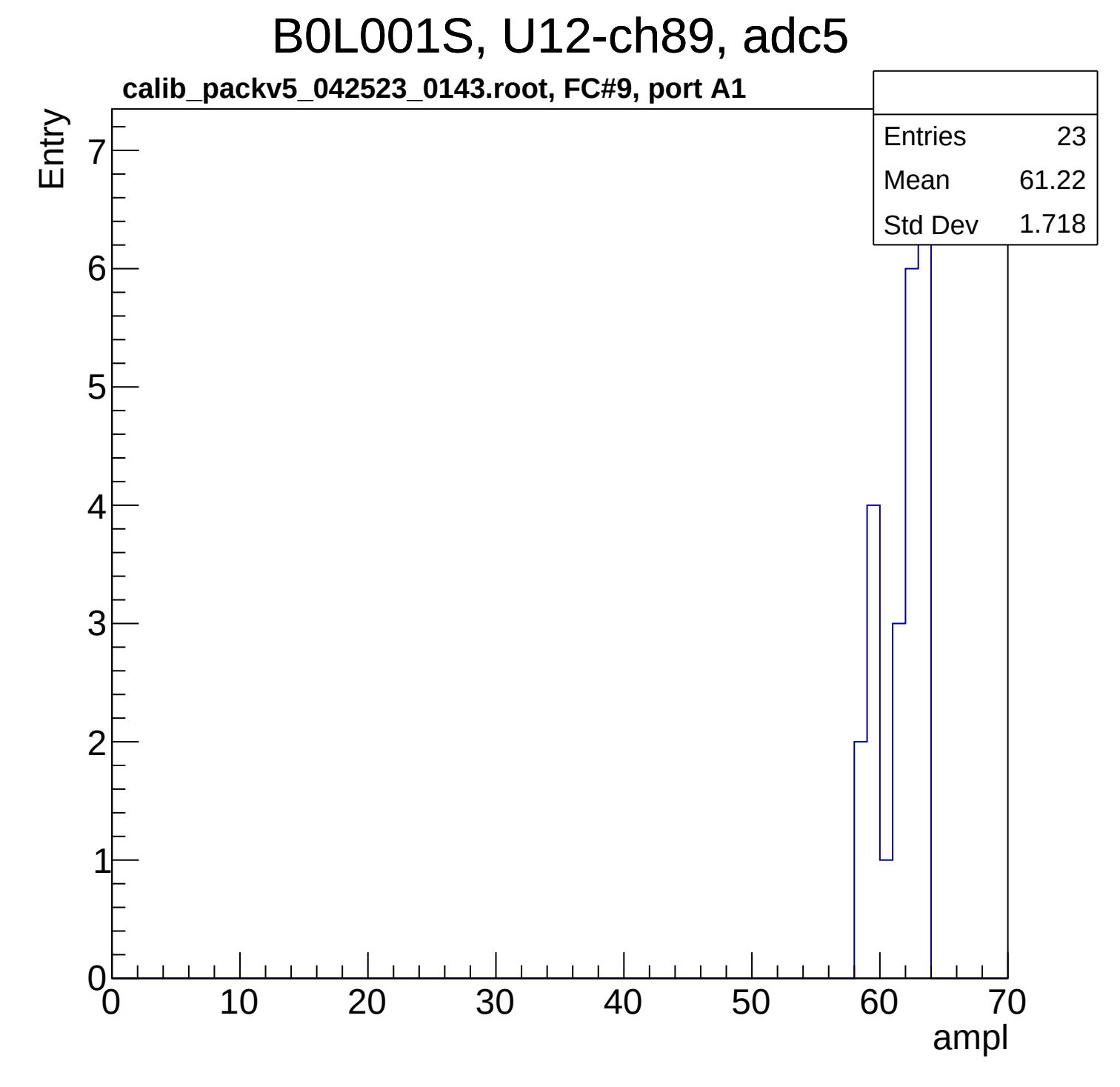
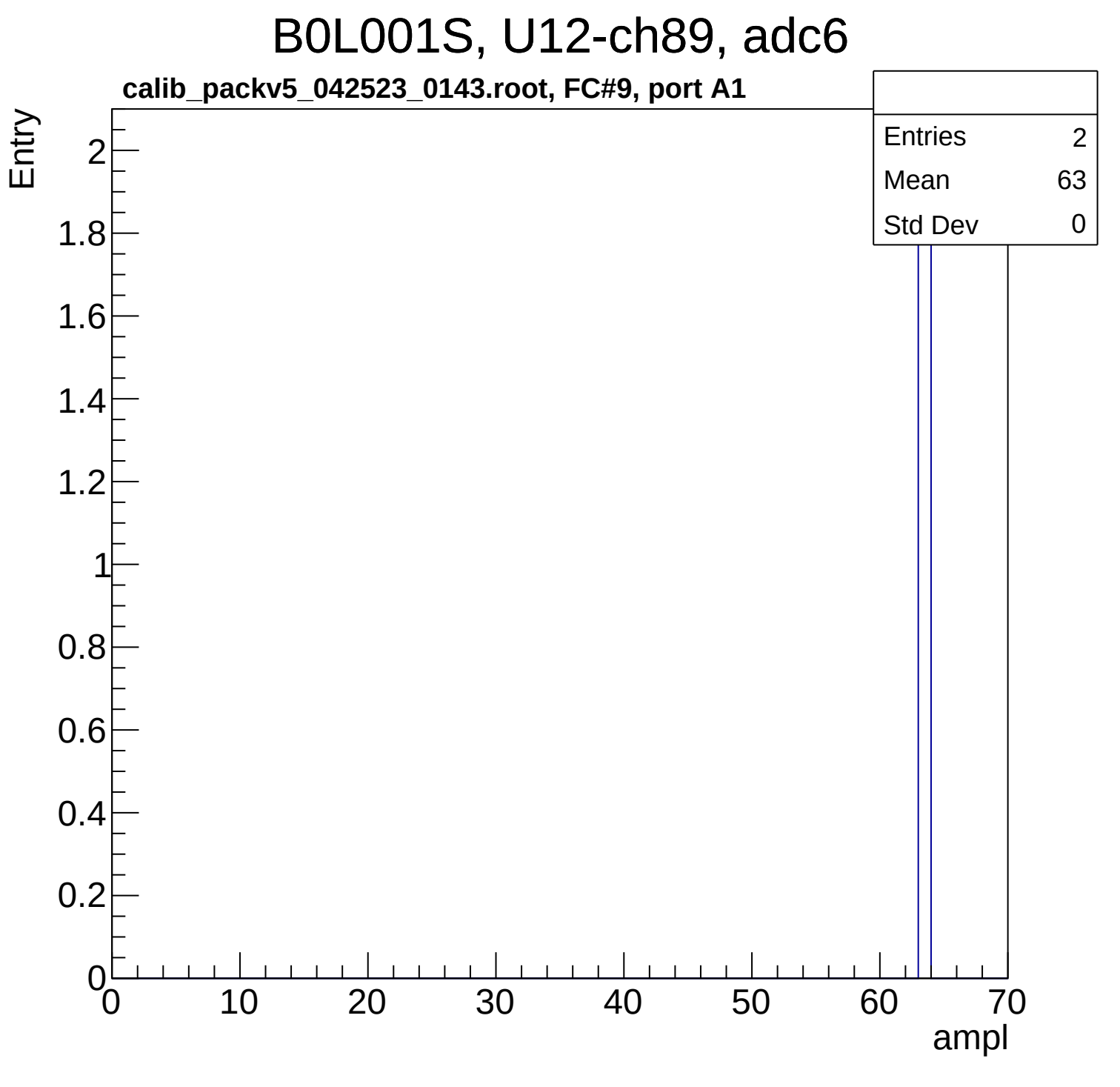
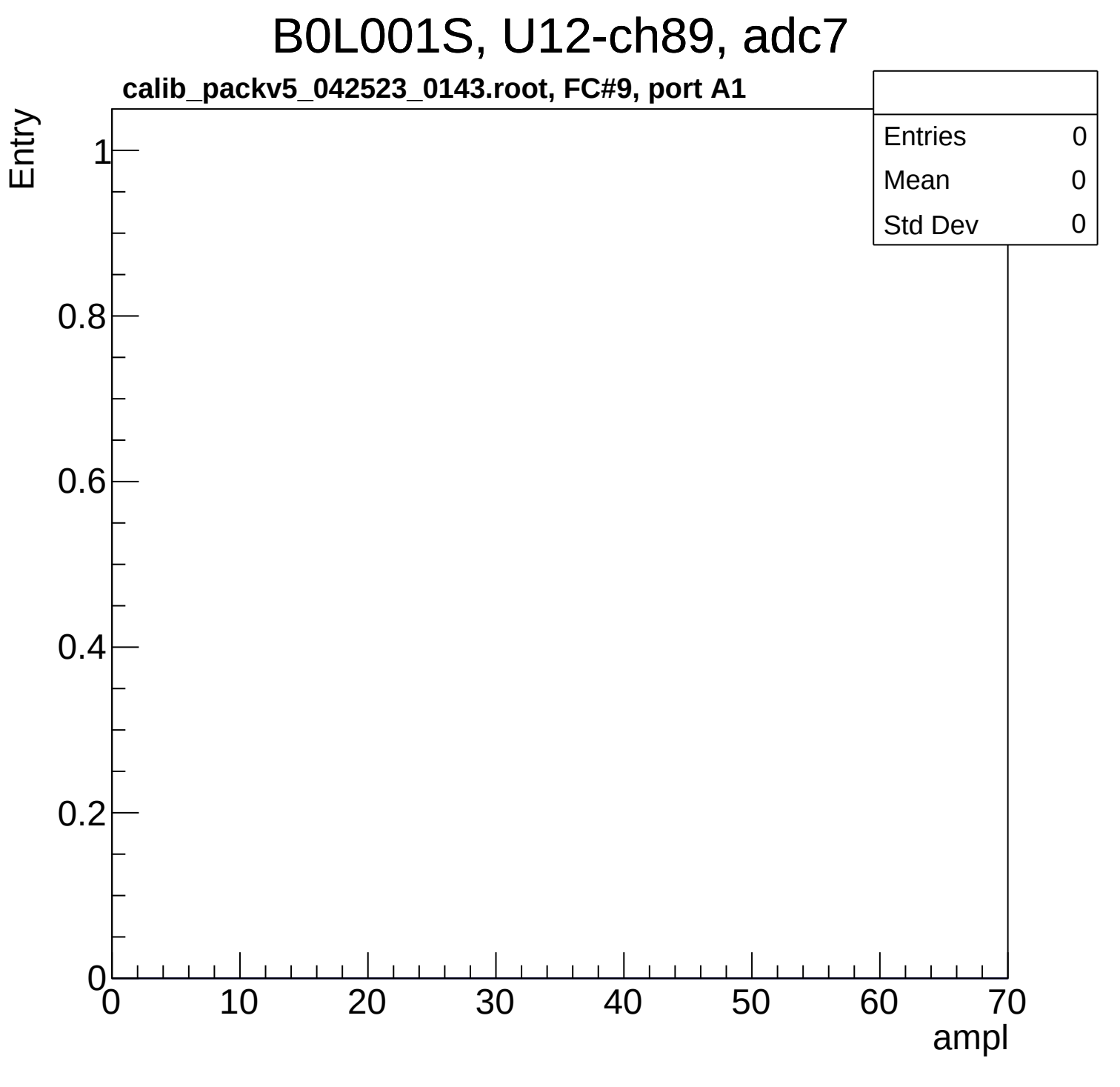
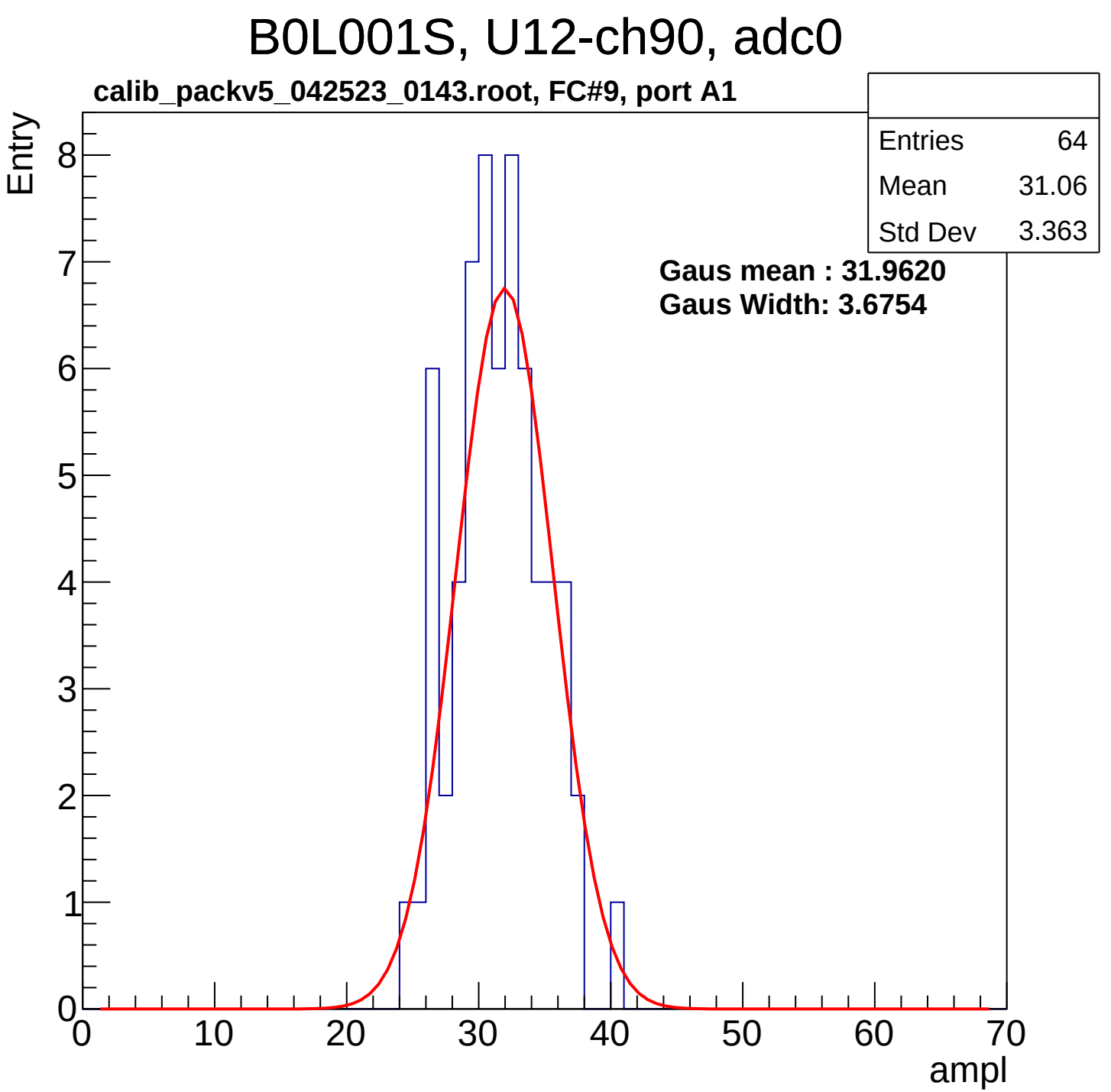

B0L001S, U12-ch89, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 23
Mean 61.22
Std Dev 1.718
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch89, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L001S, U12-ch89, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch90, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 64
Mean 31.06
Std Dev 3.363
Gaus mean : 31.9620
Gaus Width: 3.6754
Entry
ampl
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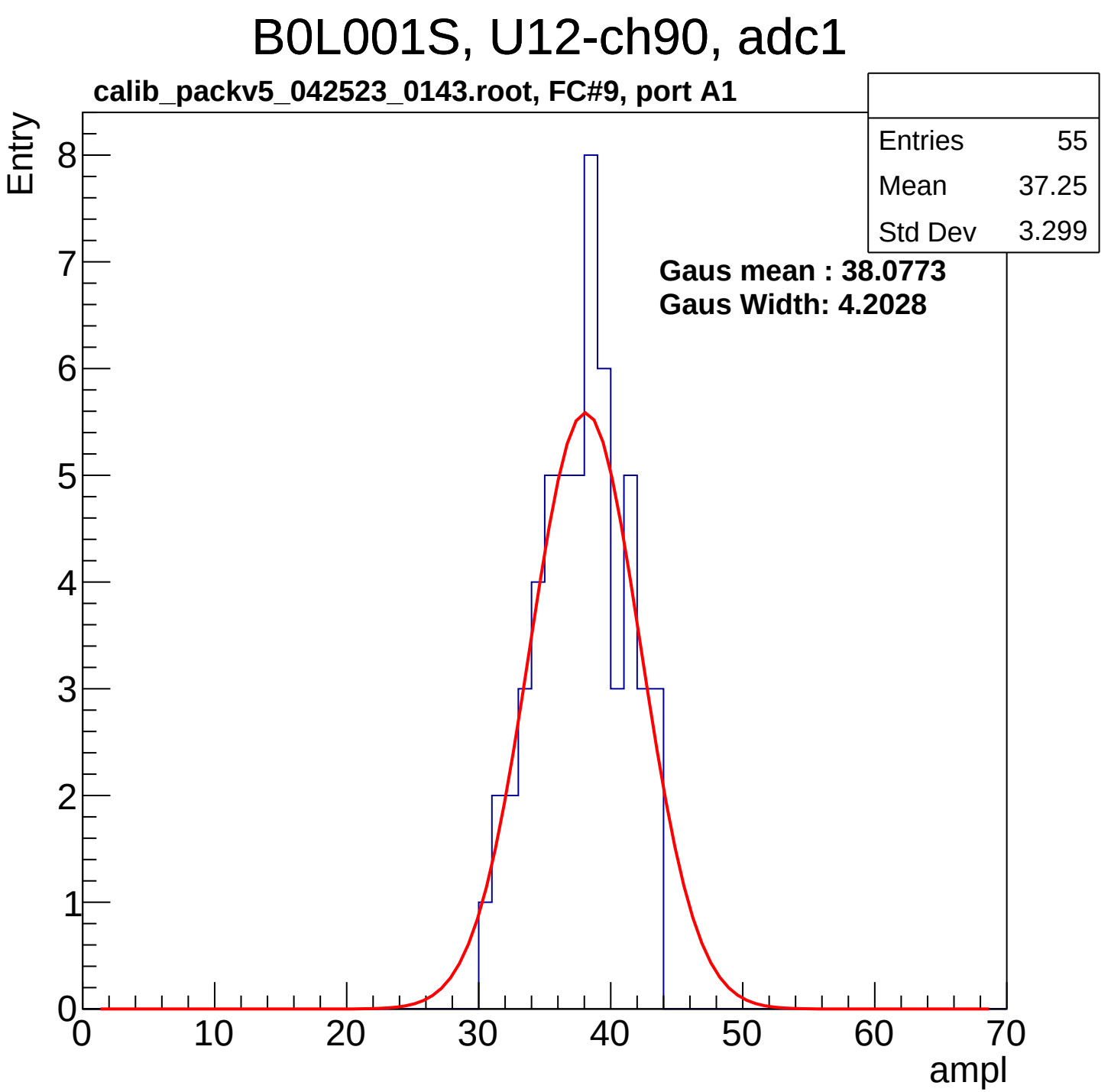
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch90, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 55
Mean 37.25
Std Dev 3.299
Gaus mean : 38.0773
Gaus Width: 4.2028
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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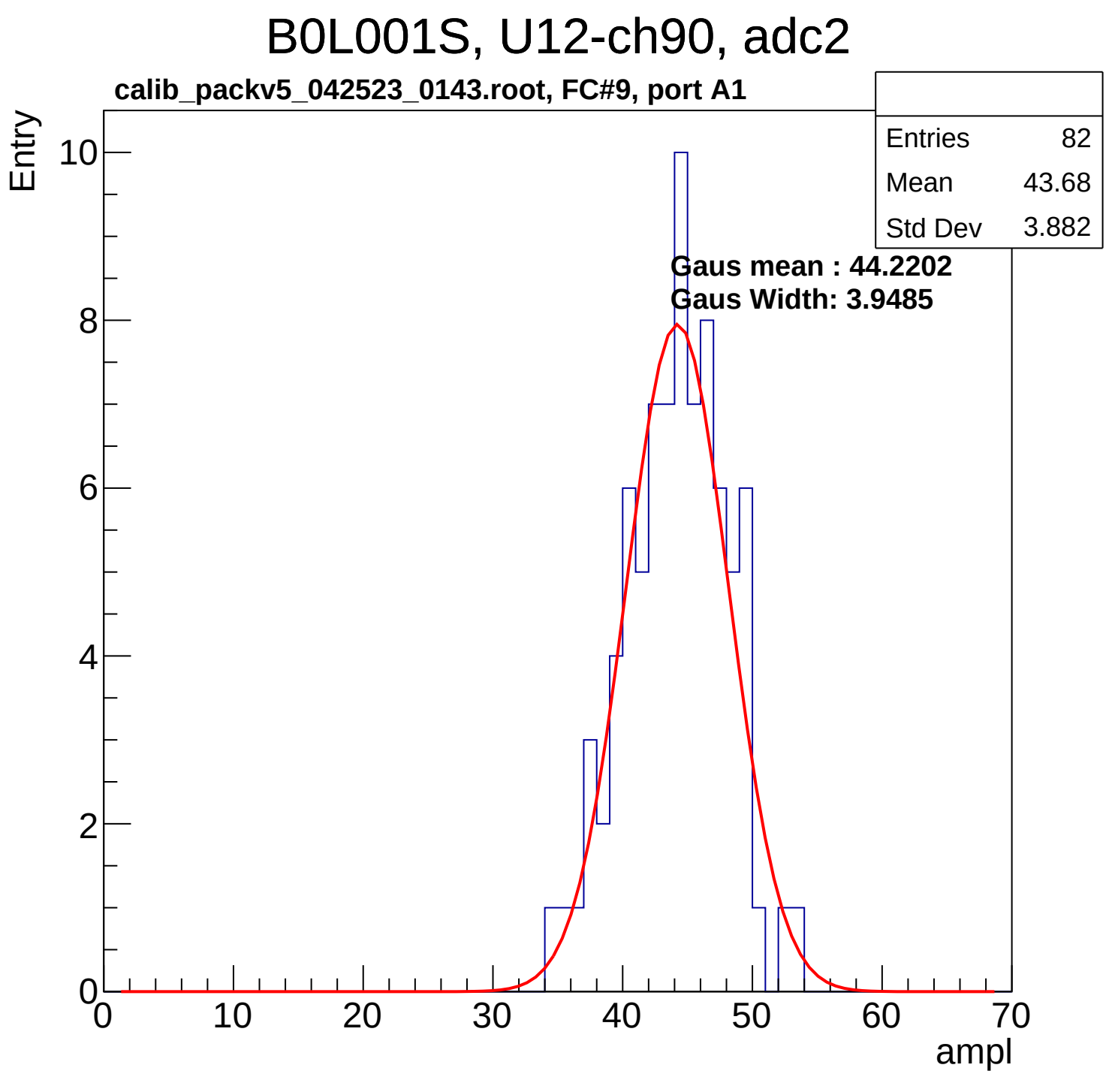
B0L001S, U12-ch90, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 82
Mean 43.68
Std Dev 3.882
Gaus mean : 44.2202
Gaus Width: 3.9485
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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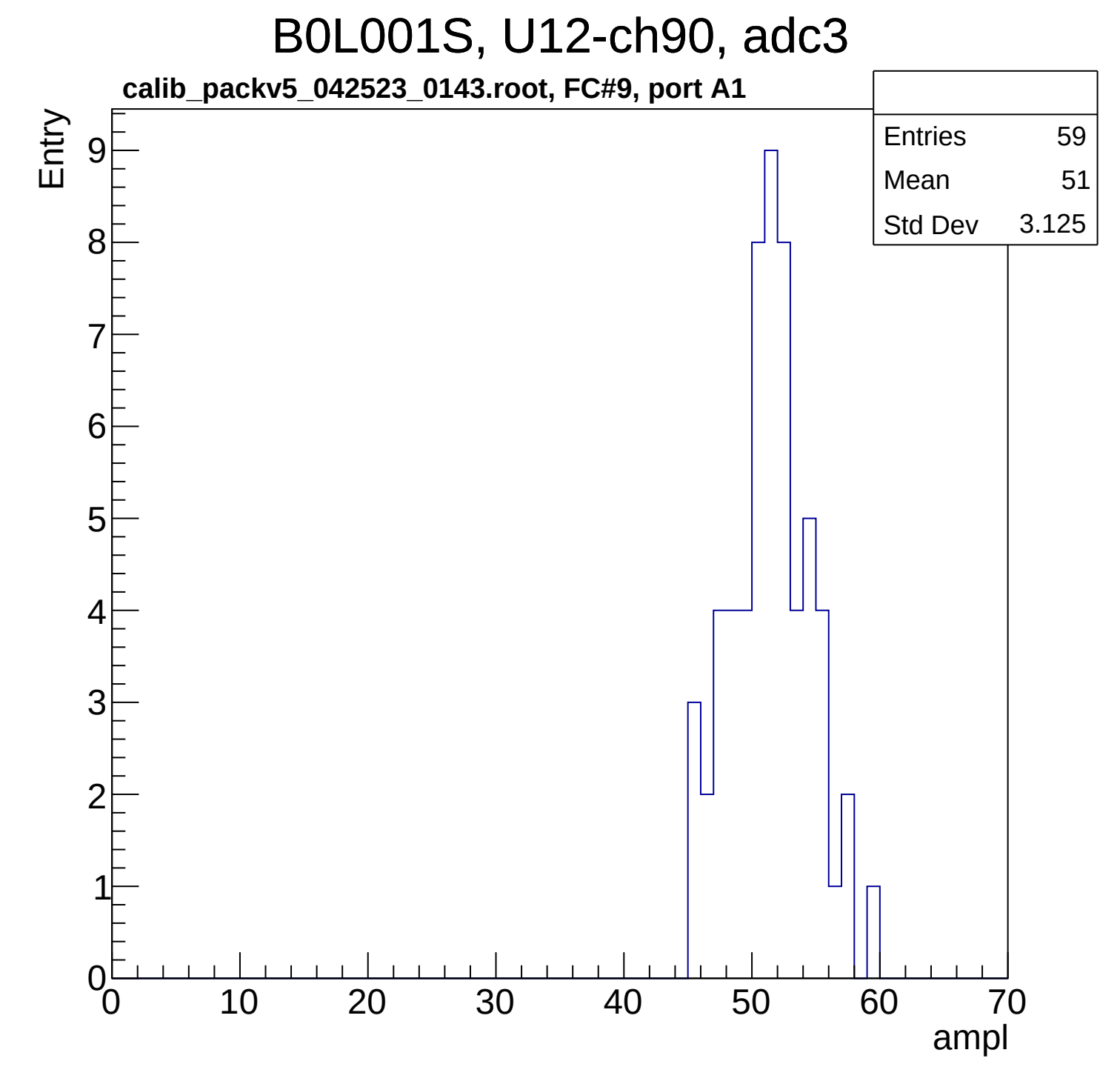
B0L001S, U12-ch90, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 59
Mean 51
Std Dev 3.125
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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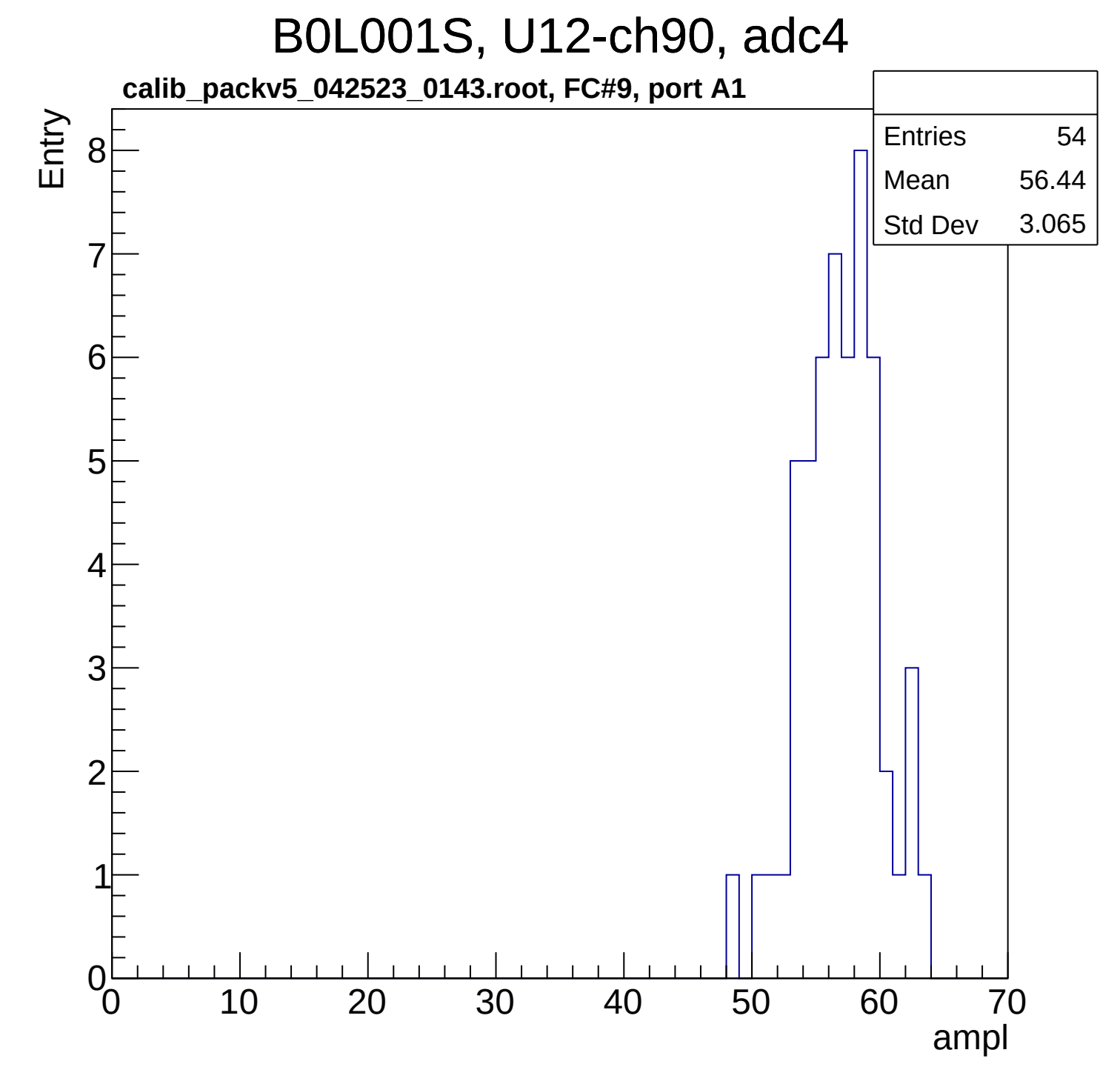
B0L001S, U12-ch90, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 54
Mean 56.44
Std Dev 3.065
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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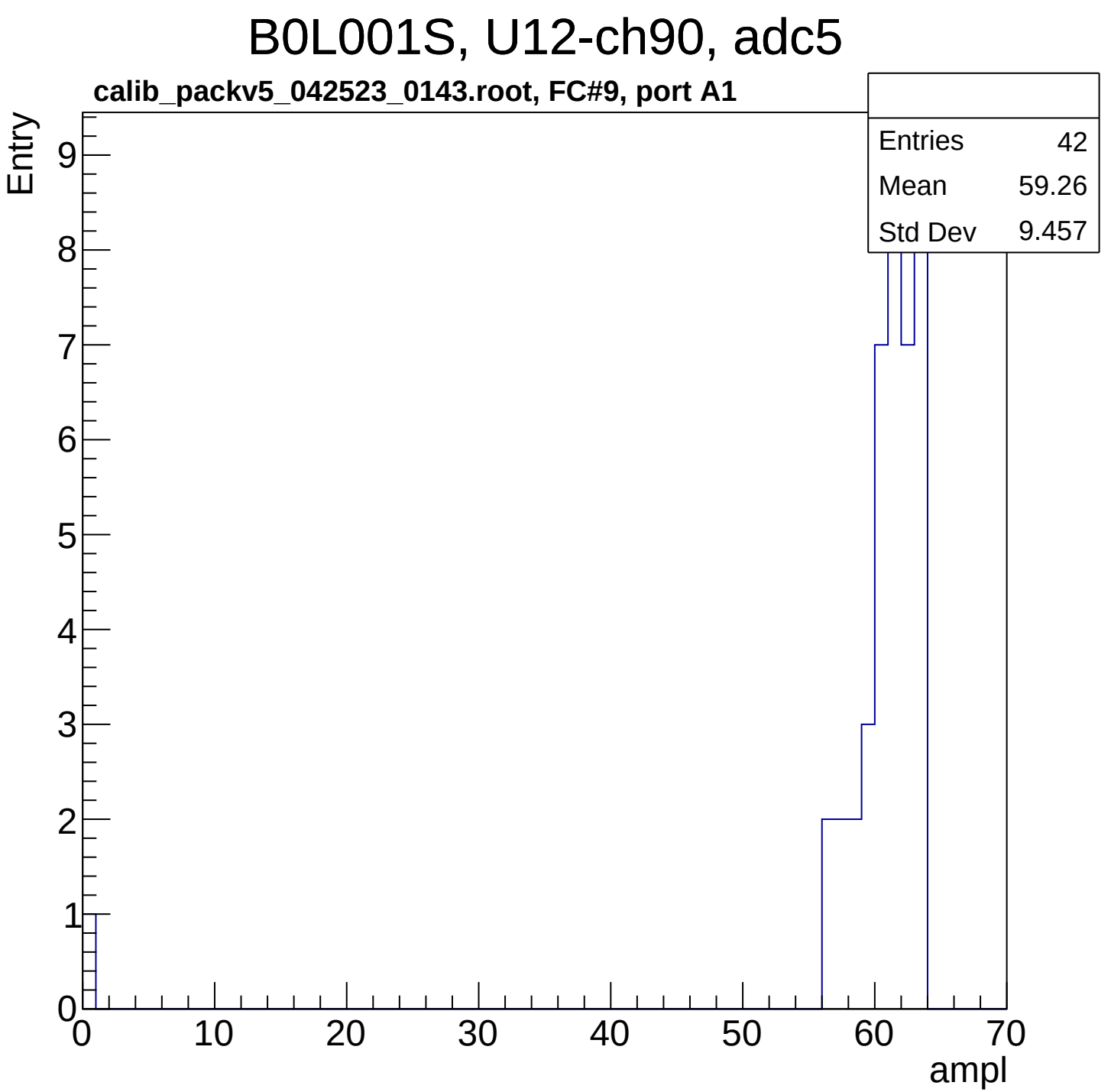
40
50
60
70


B0L001S, U12-ch90, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 42
Mean 59.26
Std Dev 9.457
Entry
ampl
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2
3
4
5
6
7
8
9
0
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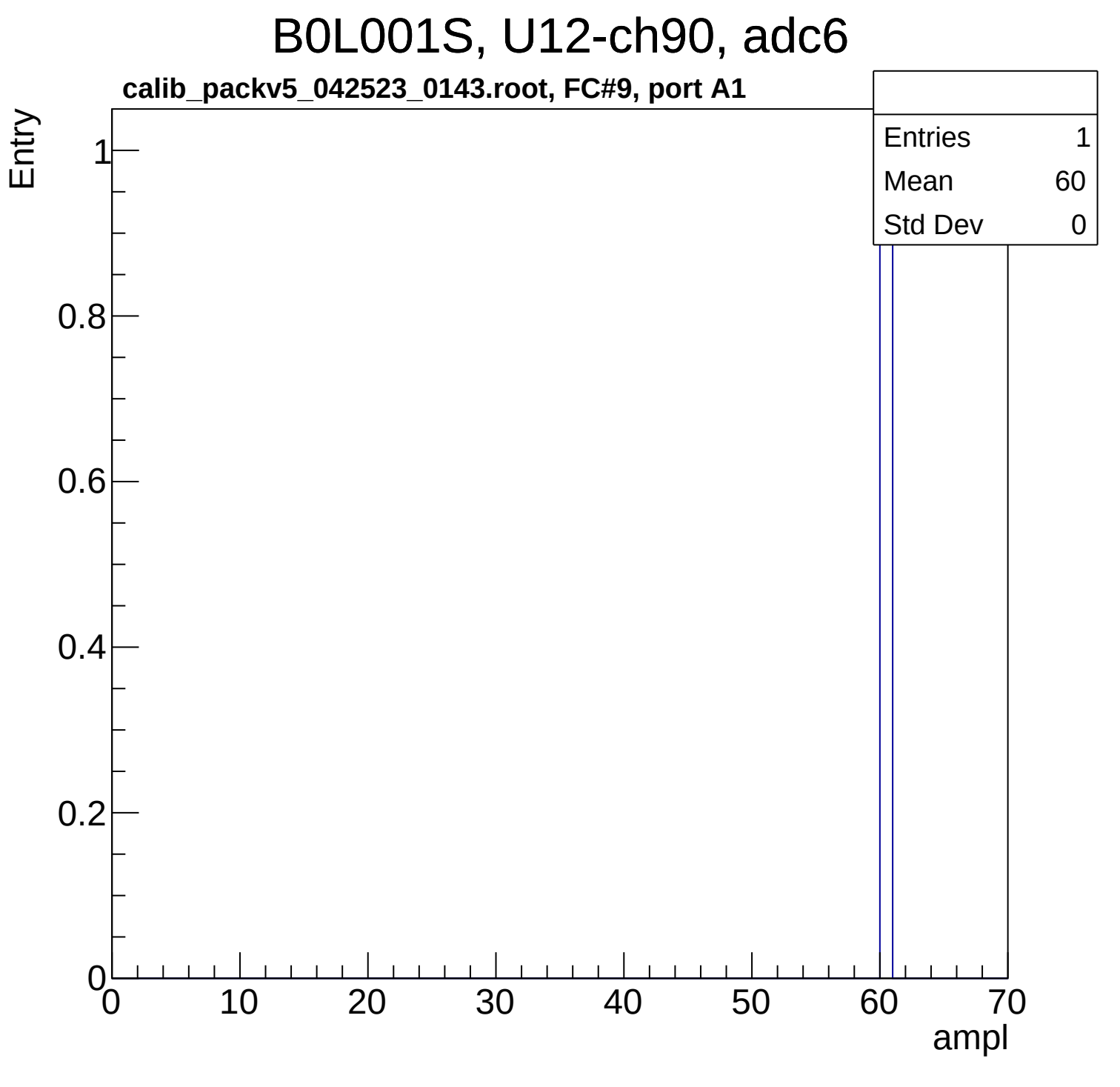
60
70


B0L001S, U12-ch90, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 60
Std Dev 0
Entry
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0.6
0.4
0.2
0
0
10
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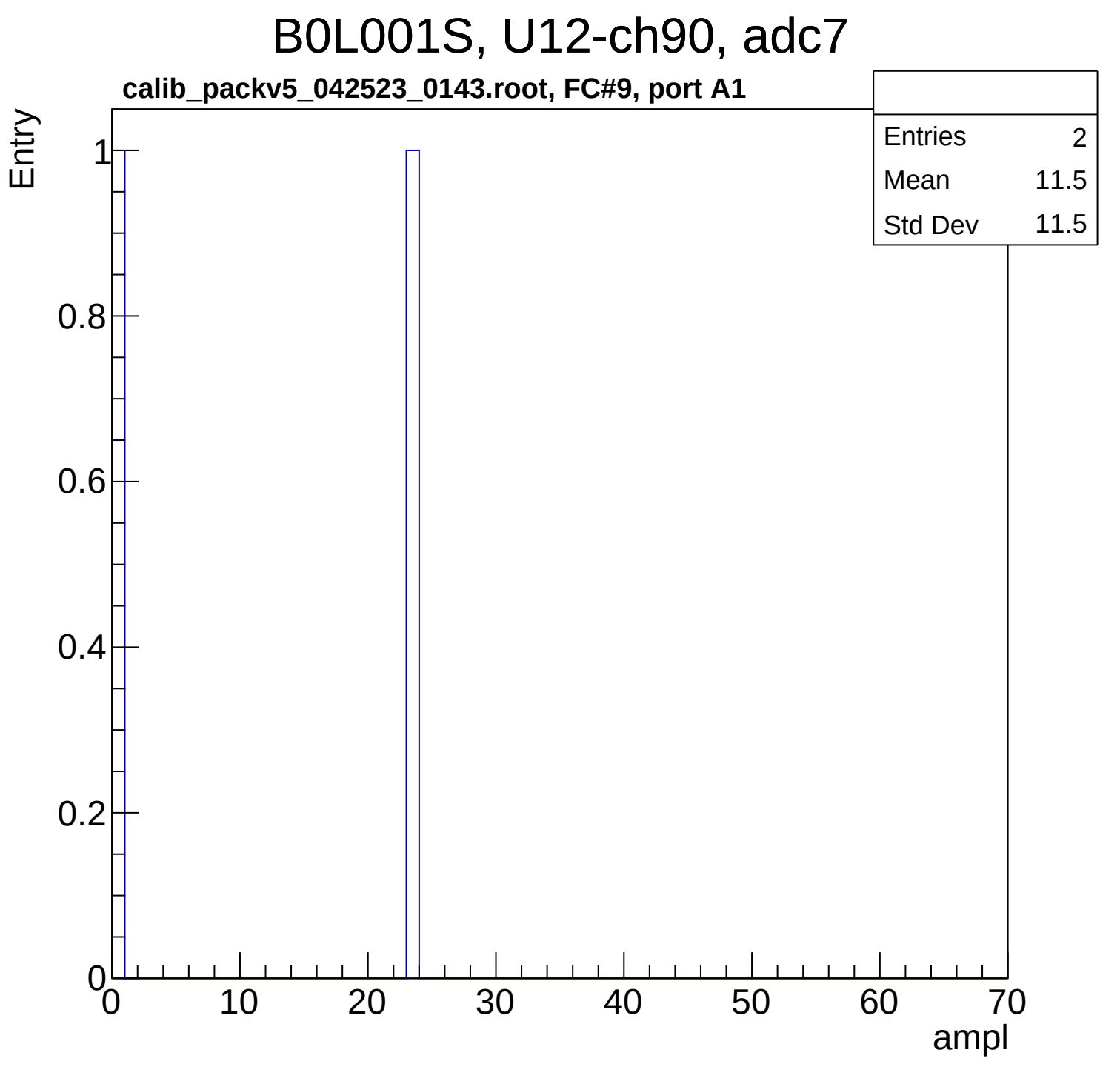
30
40
50
60
70
ampl


B0L001S, U12-ch90, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 11.5
Std Dev 11.5
Entry
1
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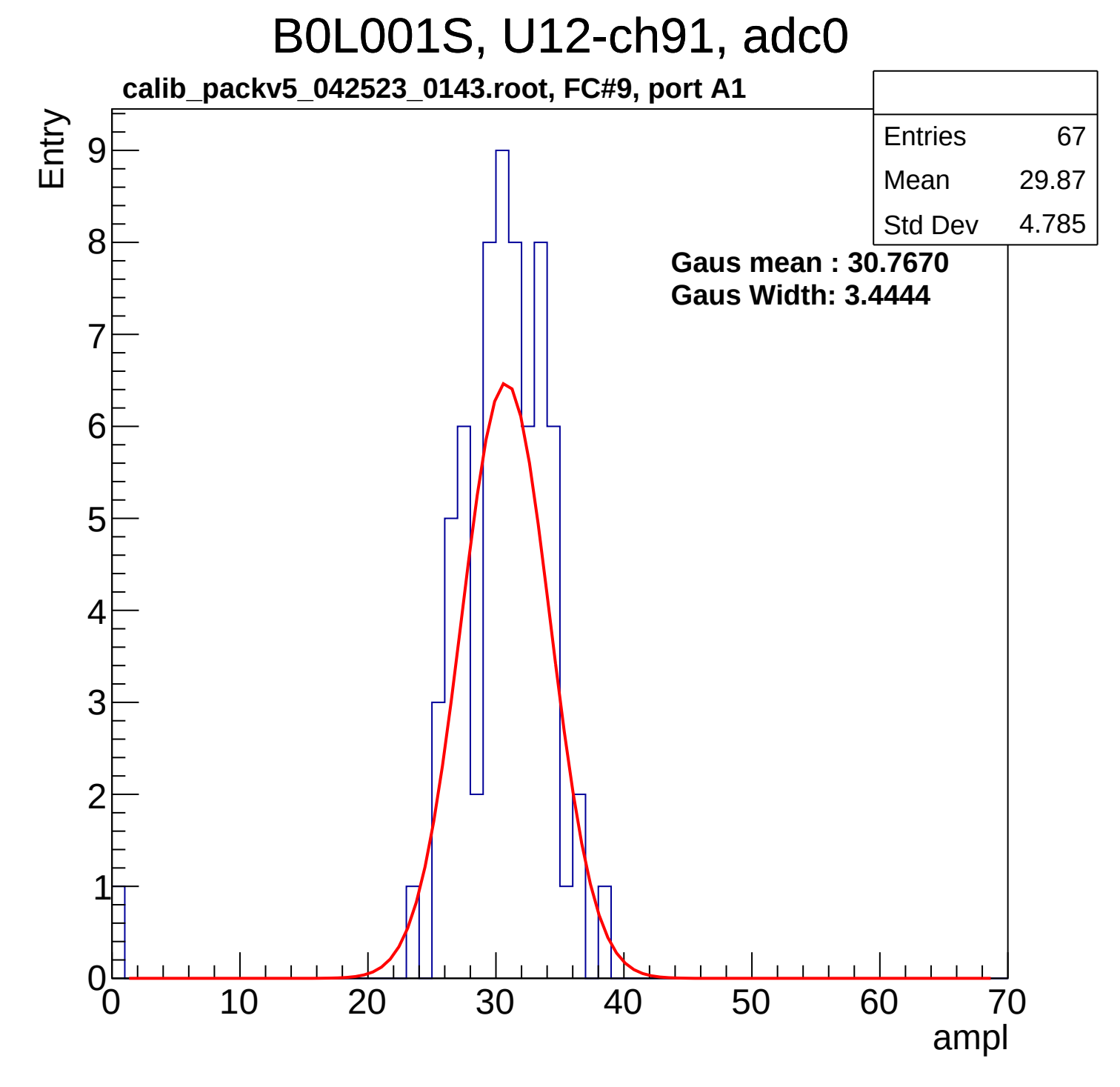
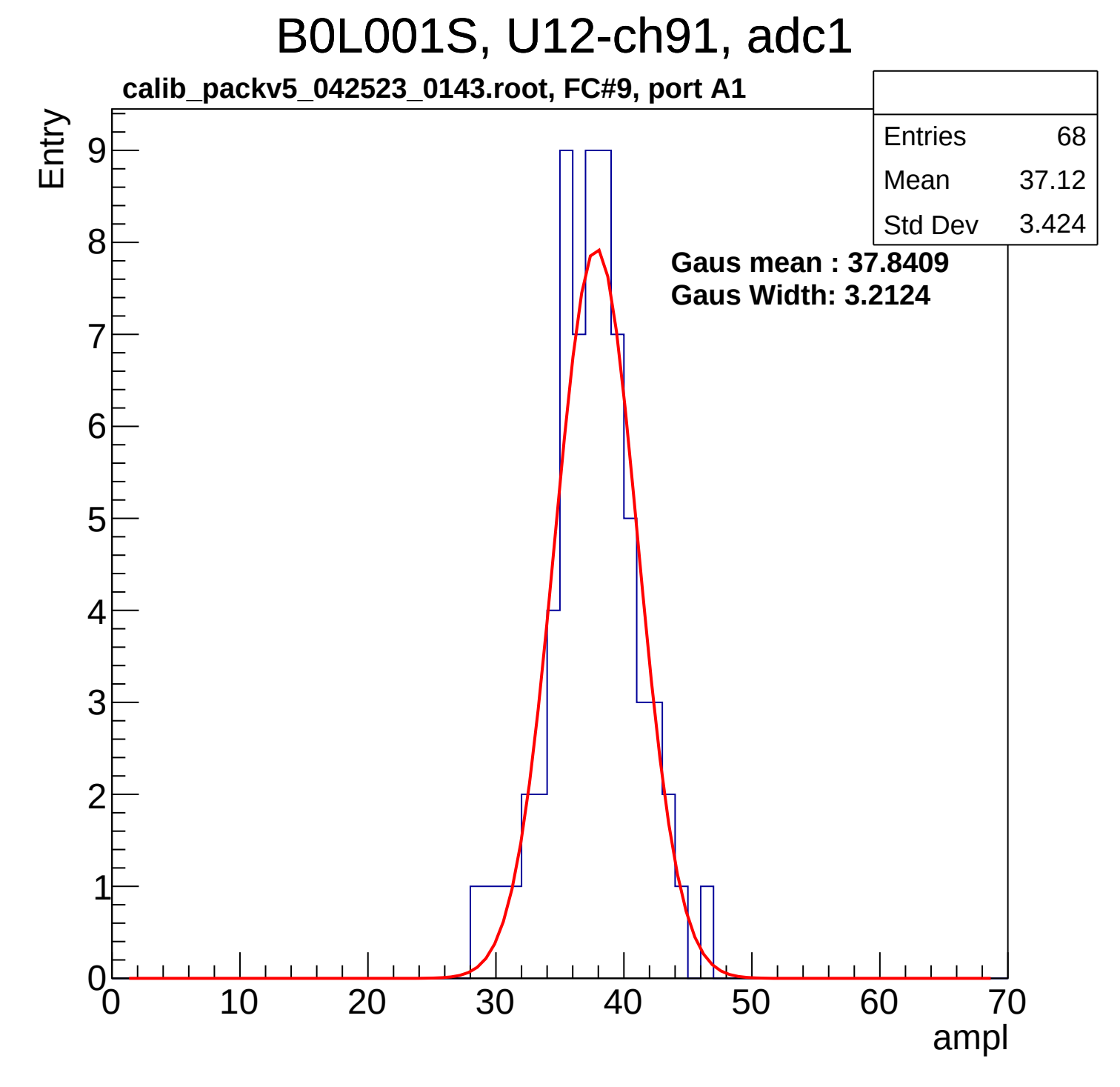
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch91, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 67
Mean 29.87
Std Dev 4.785
Gaus mean : 30.7670
Gaus Width: 3.4444
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch91, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 68
Mean 37.12
Std Dev 3.424
Gaus mean : 37.8409
Gaus Width: 3.2124
Entry
ampl
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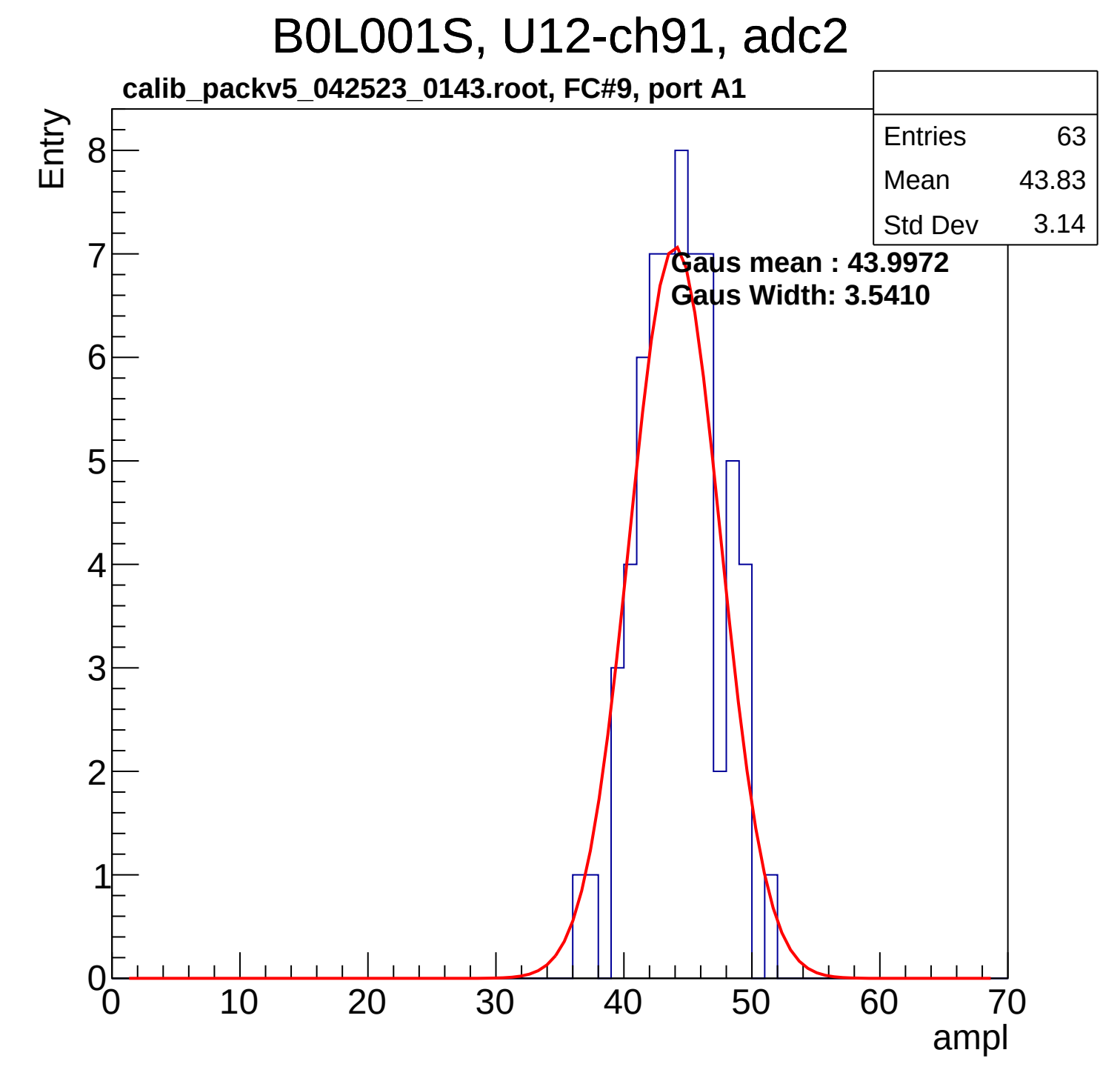
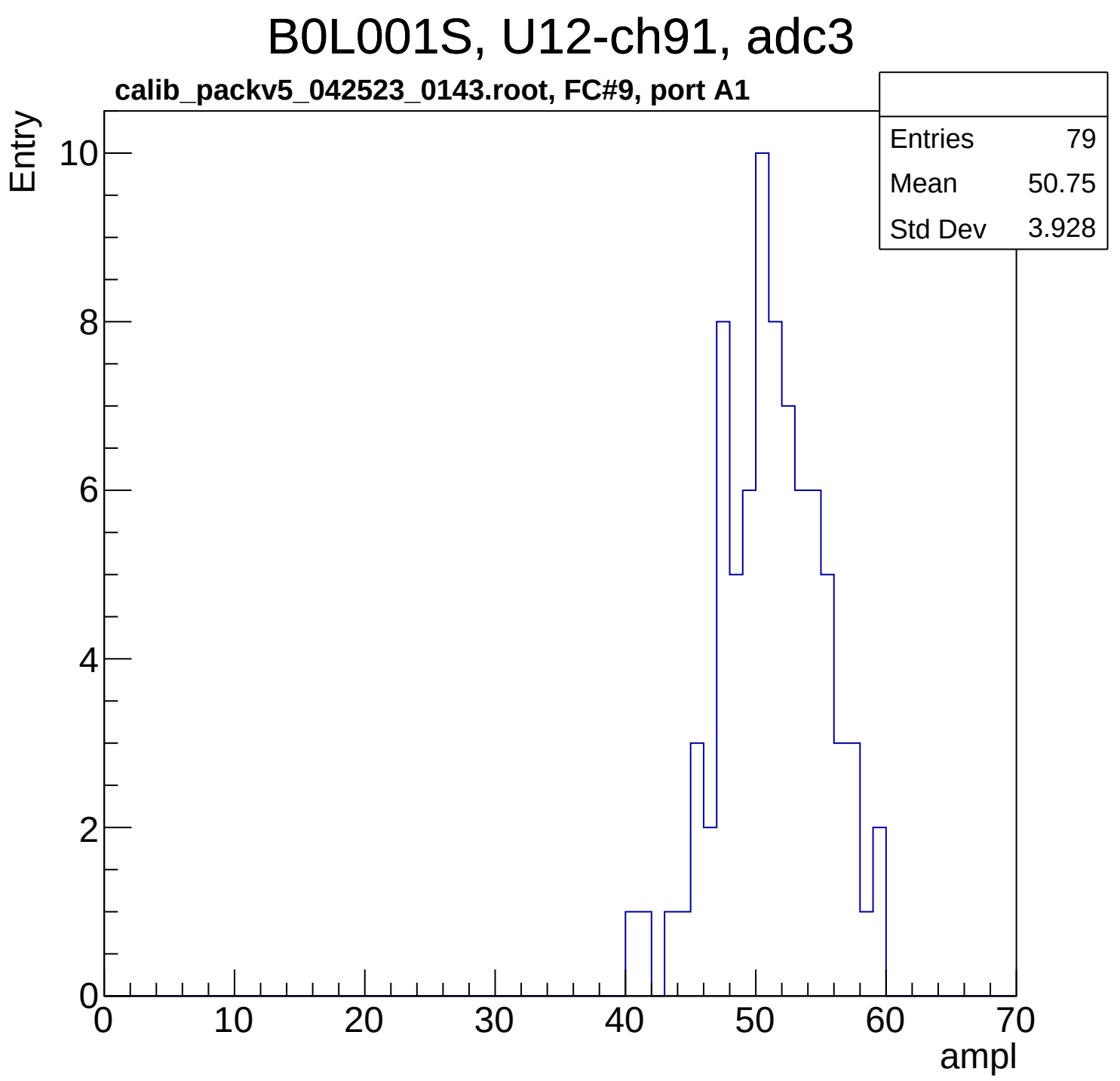
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch91, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 63
Mean 43.83
Std Dev 3.14
Gaus mean : 43.9972
Gaus Width: 3.5410
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch91, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 79
Mean 50.75
Std Dev 3.928
Entry
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2
4
6
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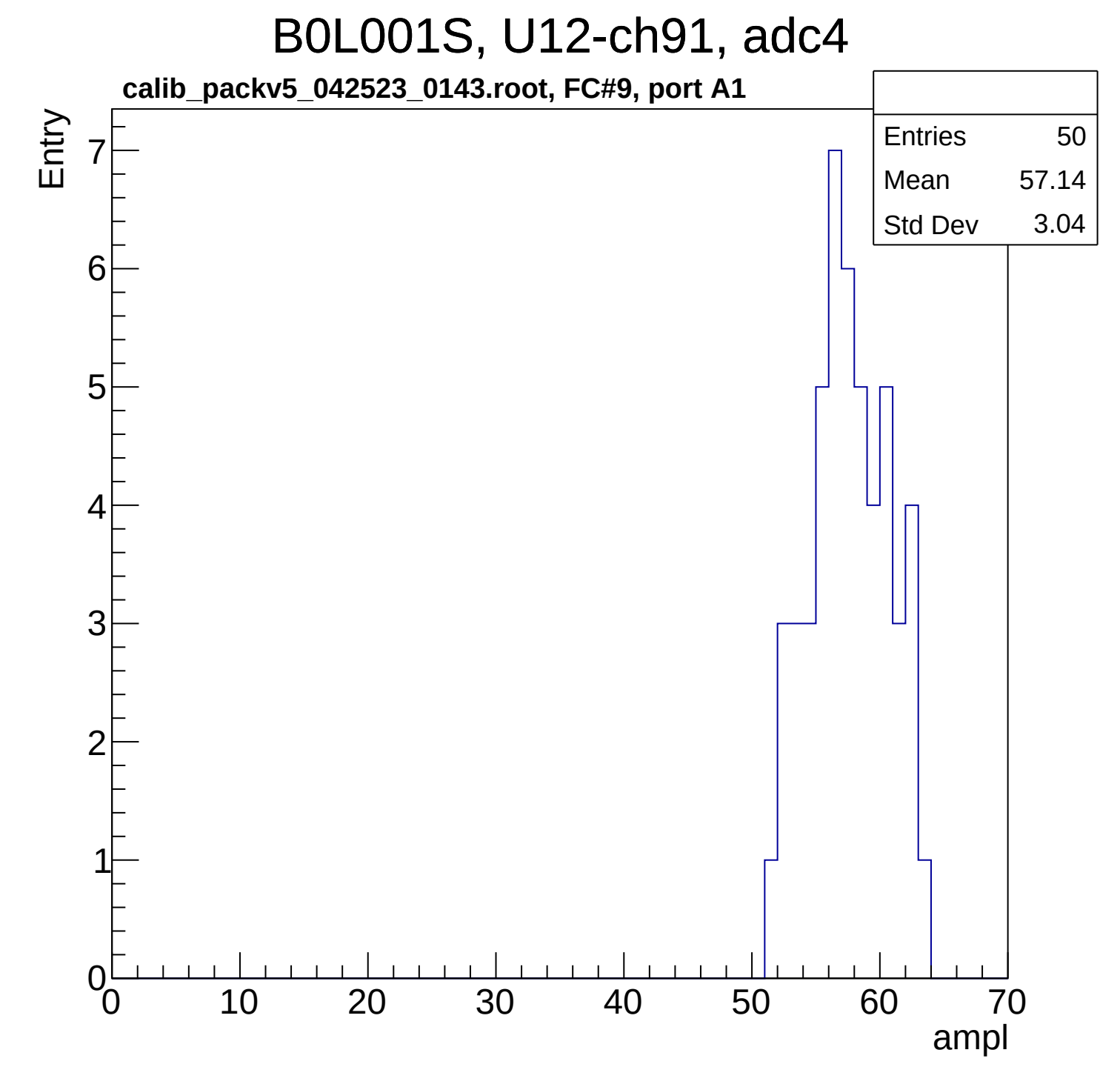
10
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch91, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 50
Mean 57.14
Std Dev 3.04
Entry
ampl
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1
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3
4
5
6
7
0
10
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40
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60
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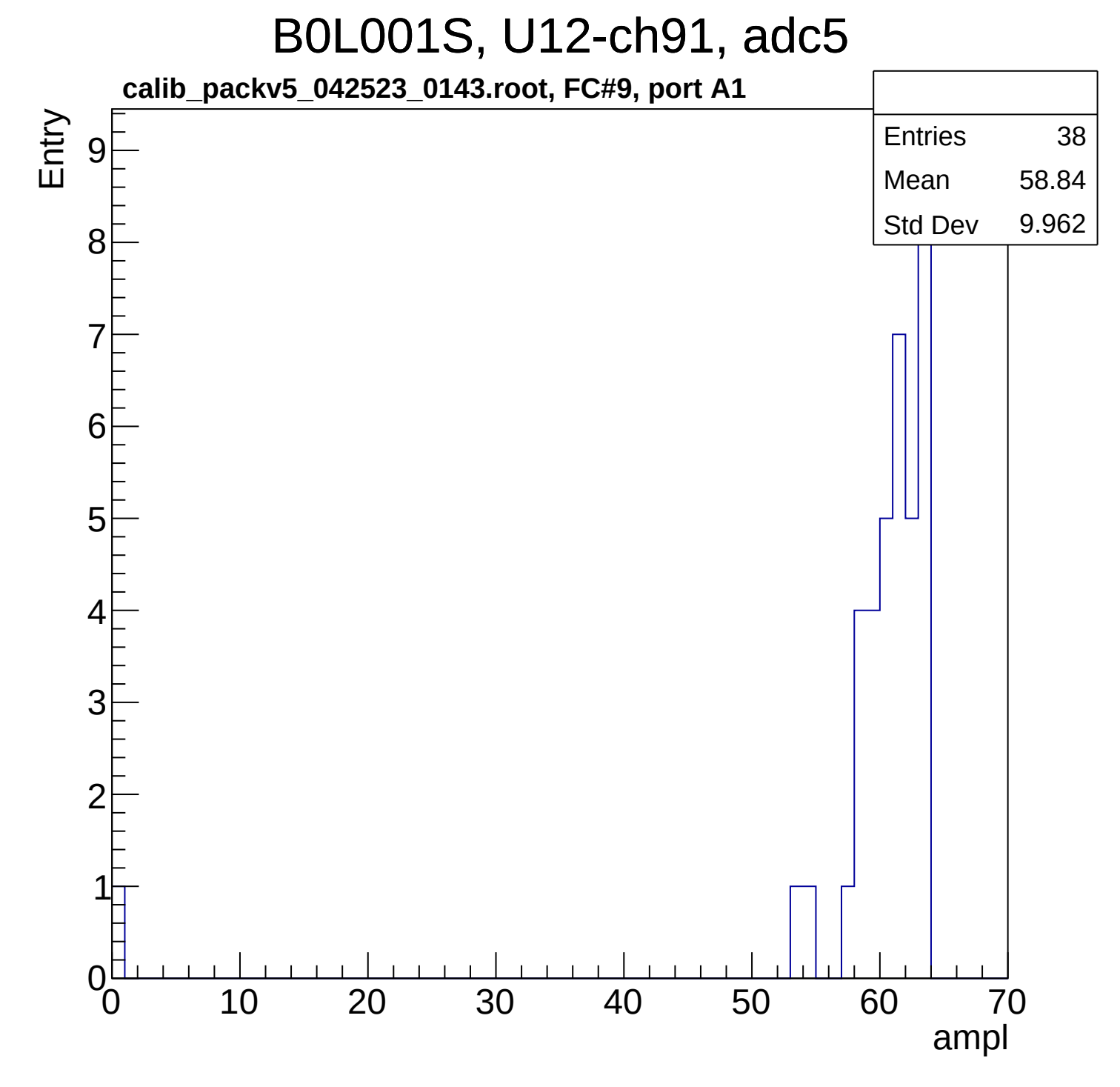
B0L001S, U12-ch91, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 38
Mean 58.84
Std Dev 9.962
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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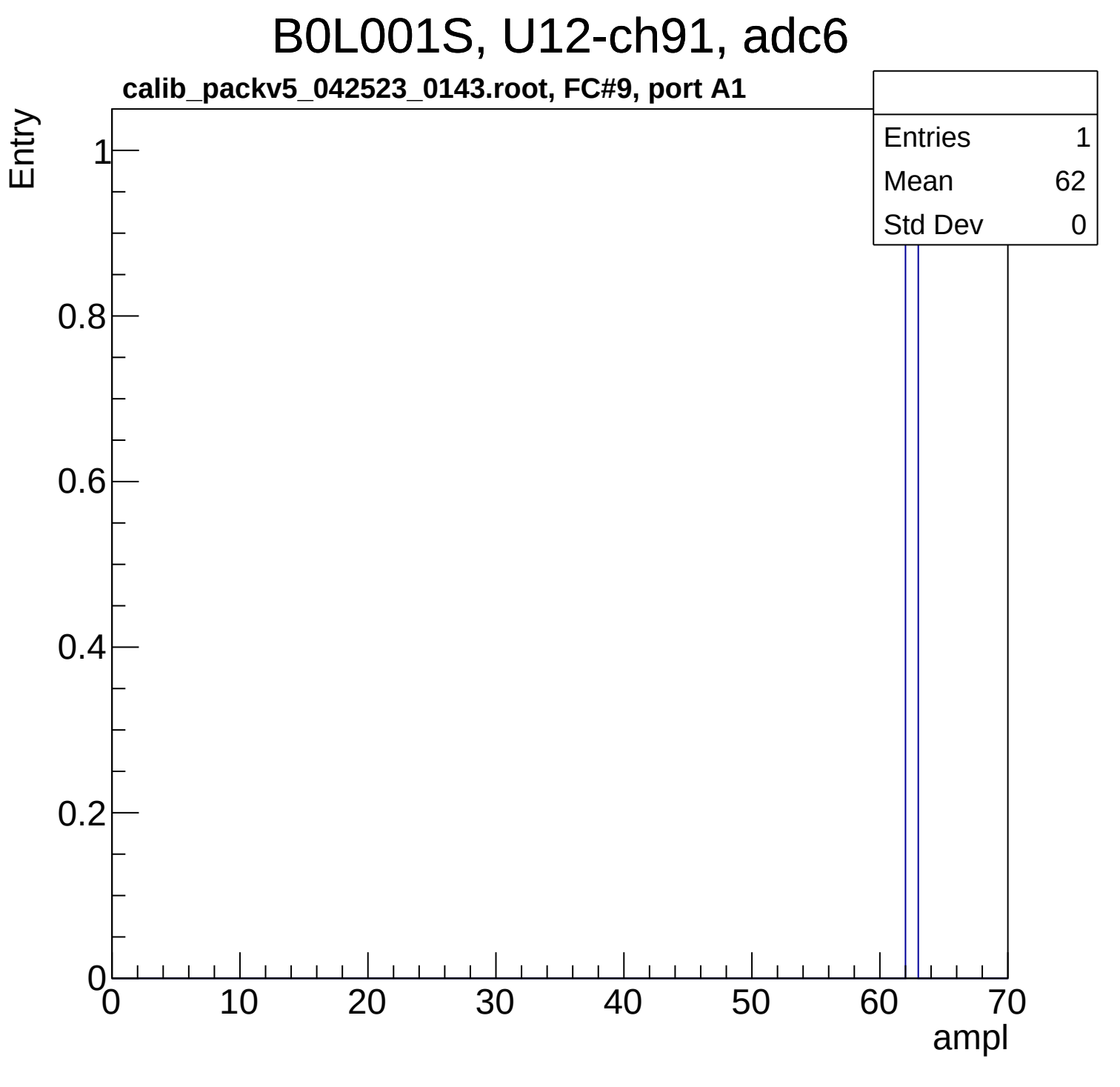
B0L001S, U12-ch91, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 62
Std Dev 0
Entry
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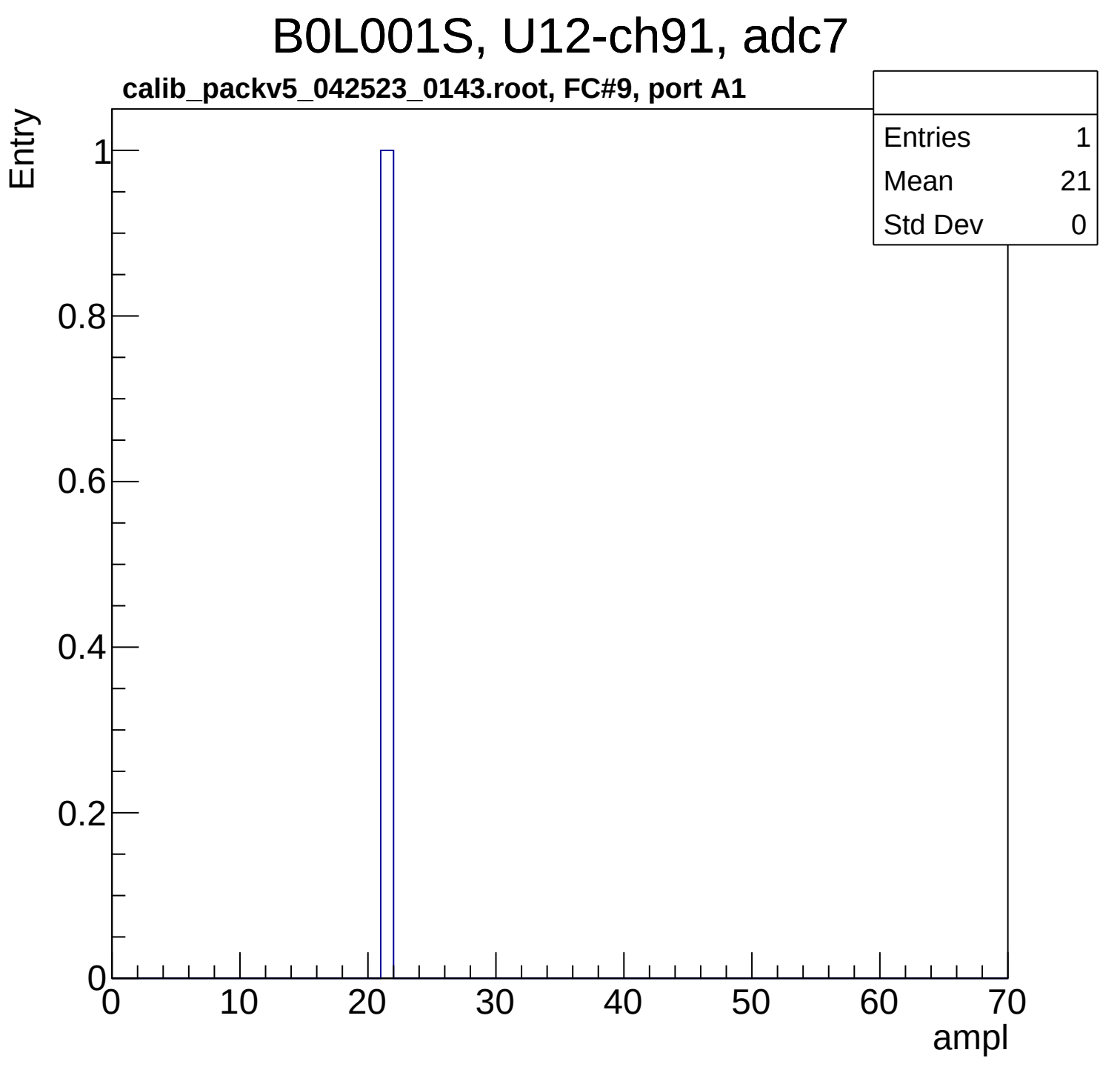
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch91, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 21
Std Dev 0
Entry
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0.4
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10
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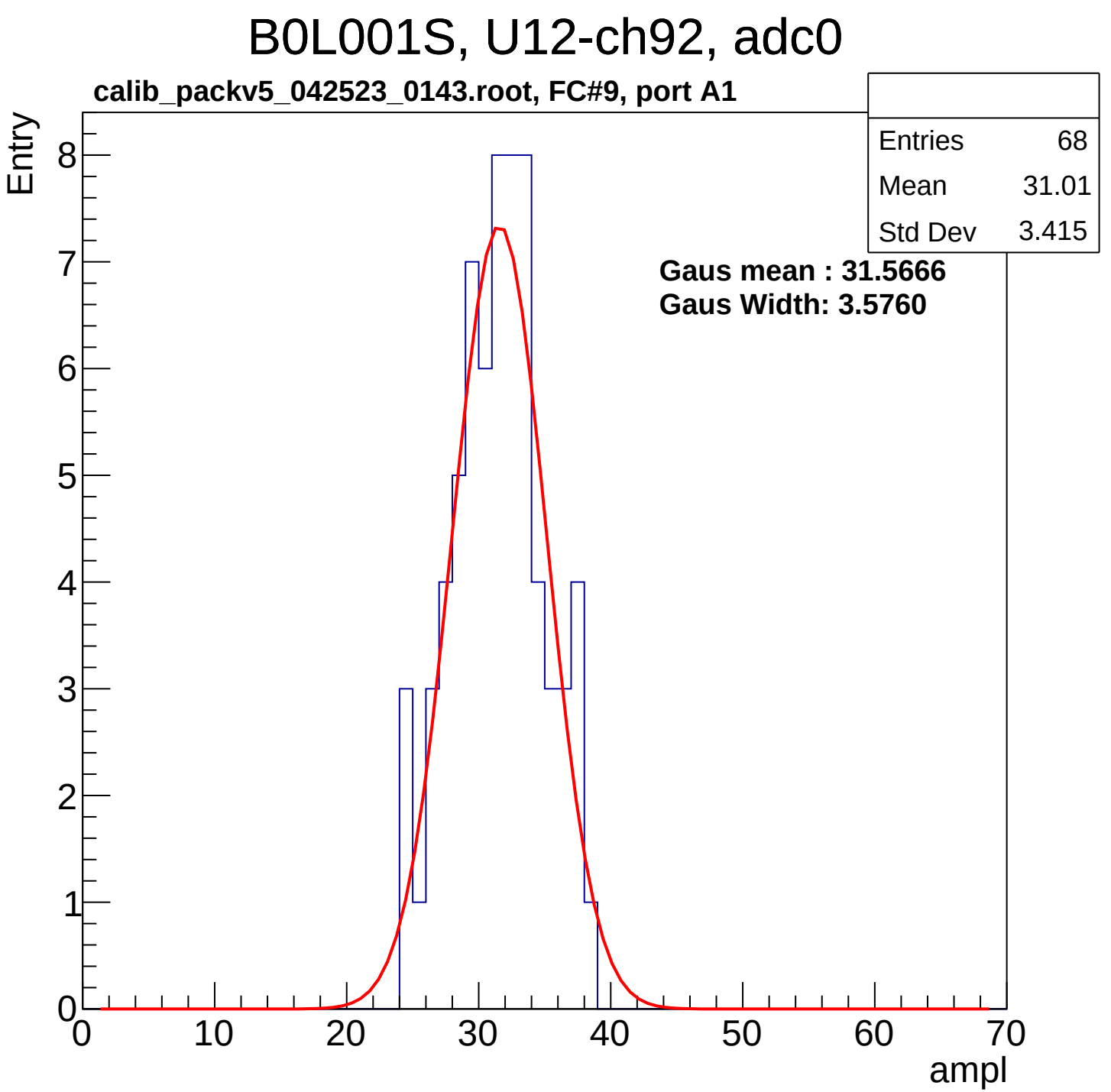
50
60
70
ampl


B0L001S, U12-ch92, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 68
Mean 31.01
Std Dev 3.415
Gaus mean : 31.5666
Gaus Width: 3.5760
Entry
ampl
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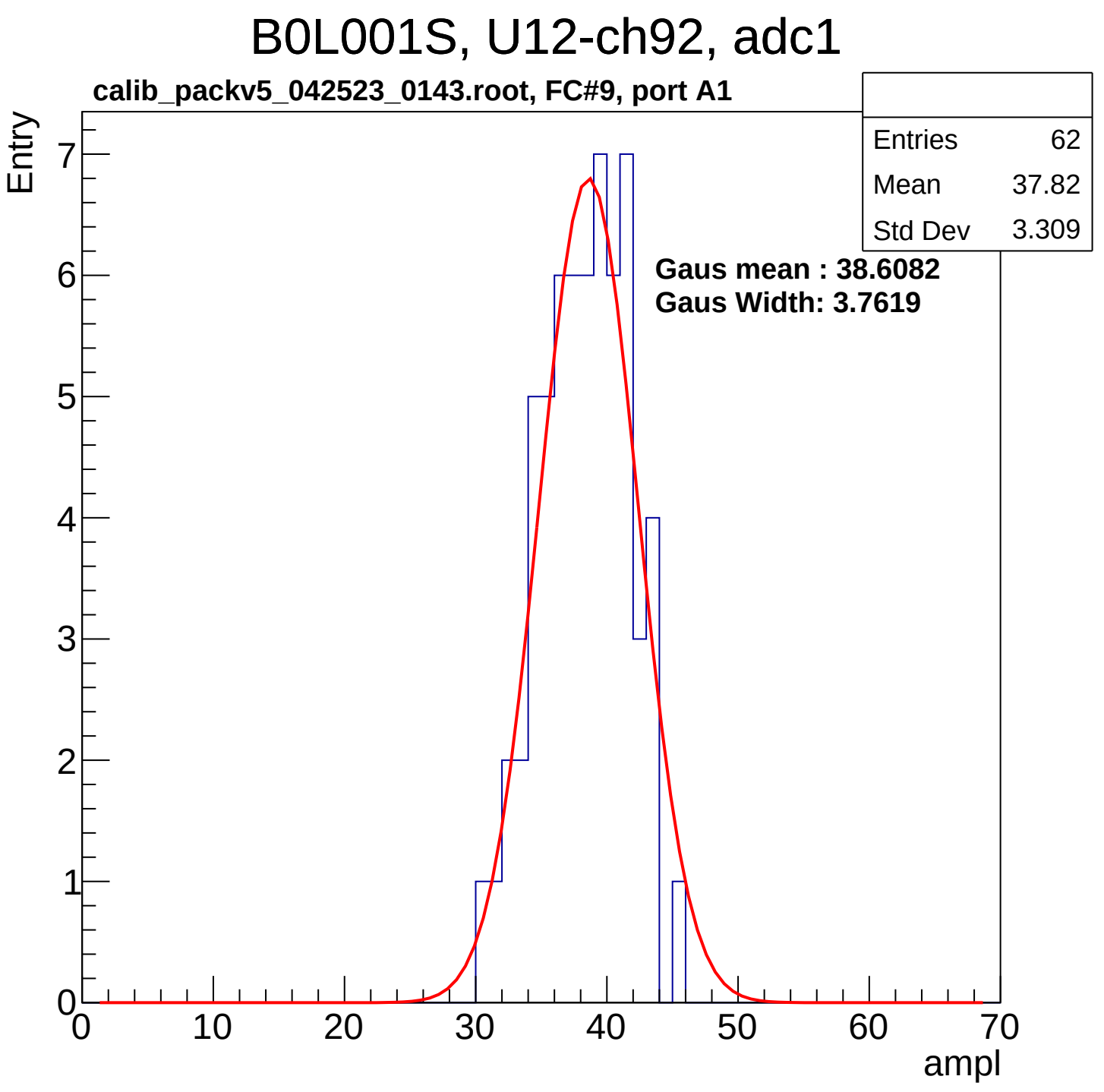
B0L001S, U12-ch92, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 62
Mean 37.82
Std Dev 3.309
Gaus mean : 38.6082
Gaus Width: 3.7619
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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50
60
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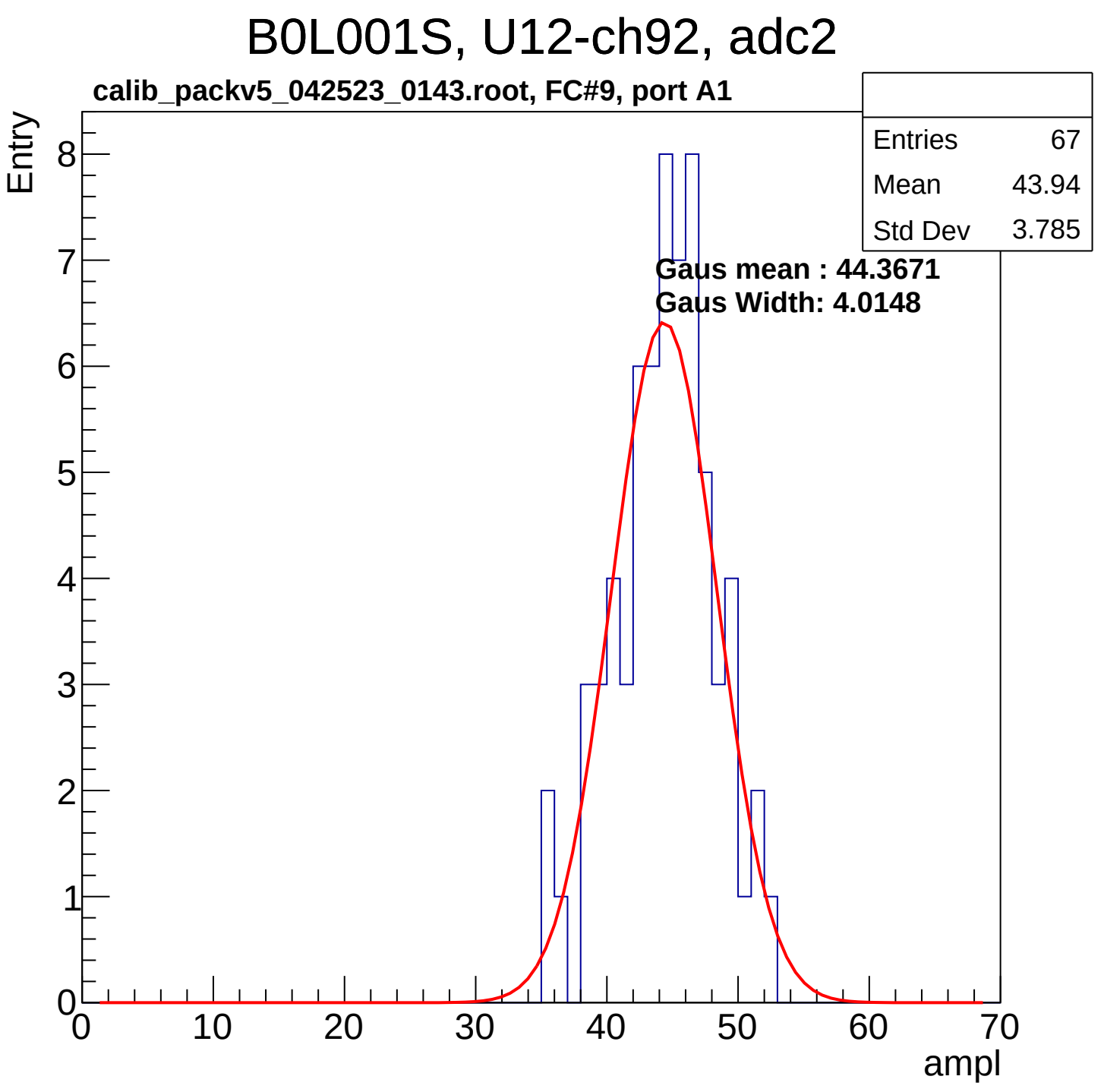
B0L001S, U12-ch92, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 67
Mean 43.94
Std Dev 3.785
Gaus mean : 44.3671
Gaus Width: 4.0148
Entry
ampl
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1
2
3
4
5
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7
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0
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20
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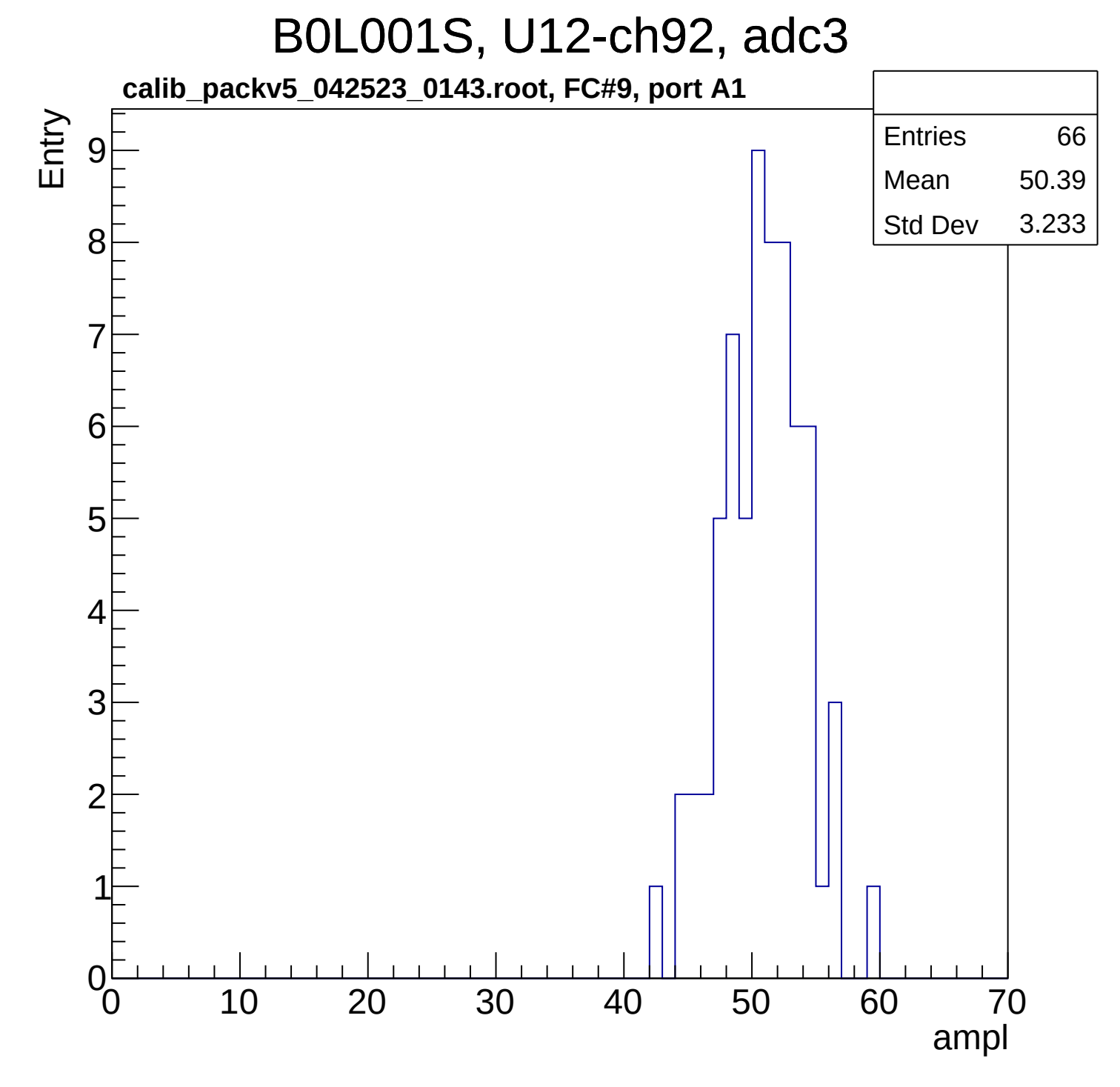
B0L001S, U12-ch92, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 66
Mean 50.39
Std Dev 3.233
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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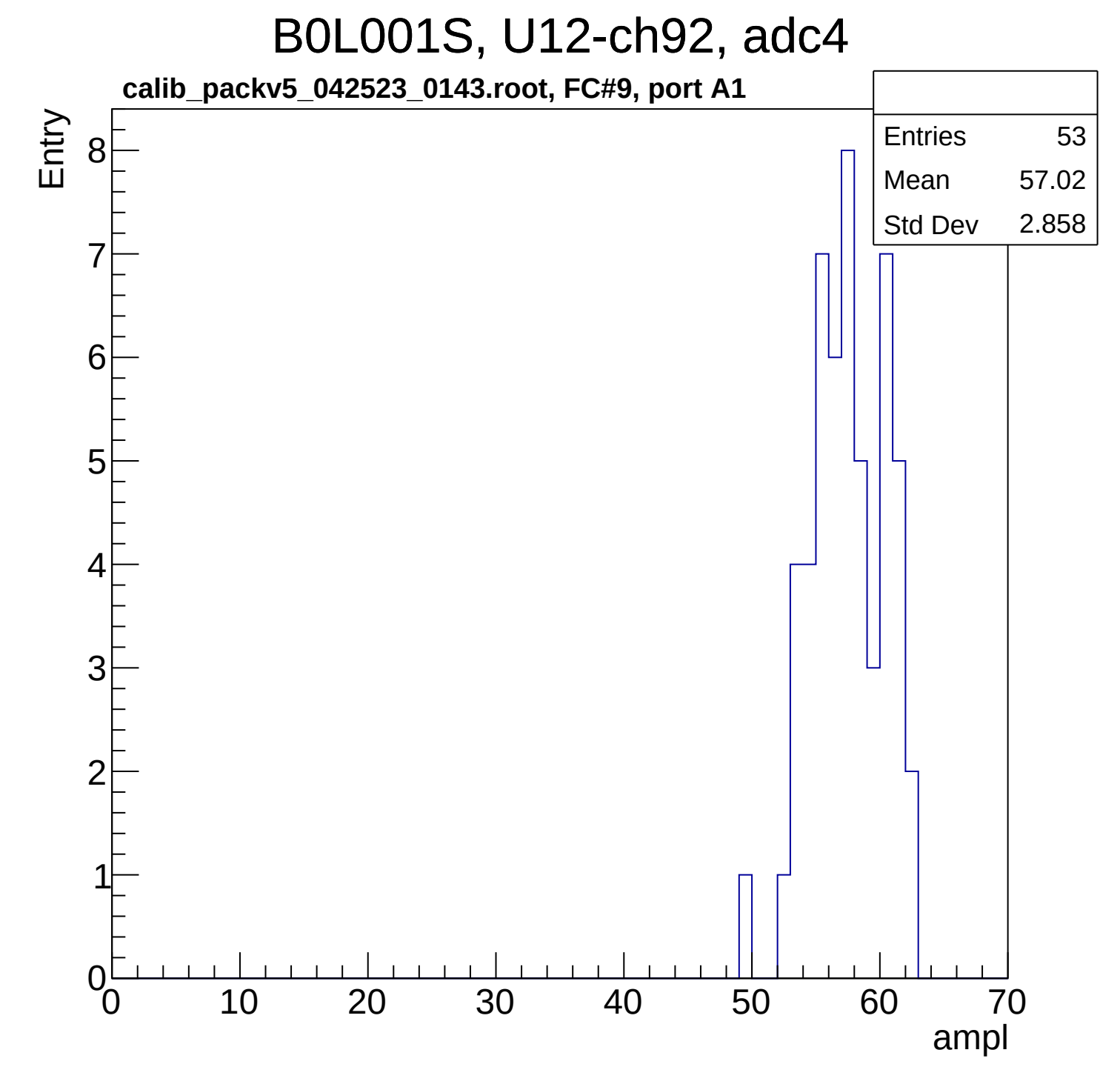
40
50
60
70


B0L001S, U12-ch92, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 53
Mean 57.02
Std Dev 2.858
Entry
ampl
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1
2
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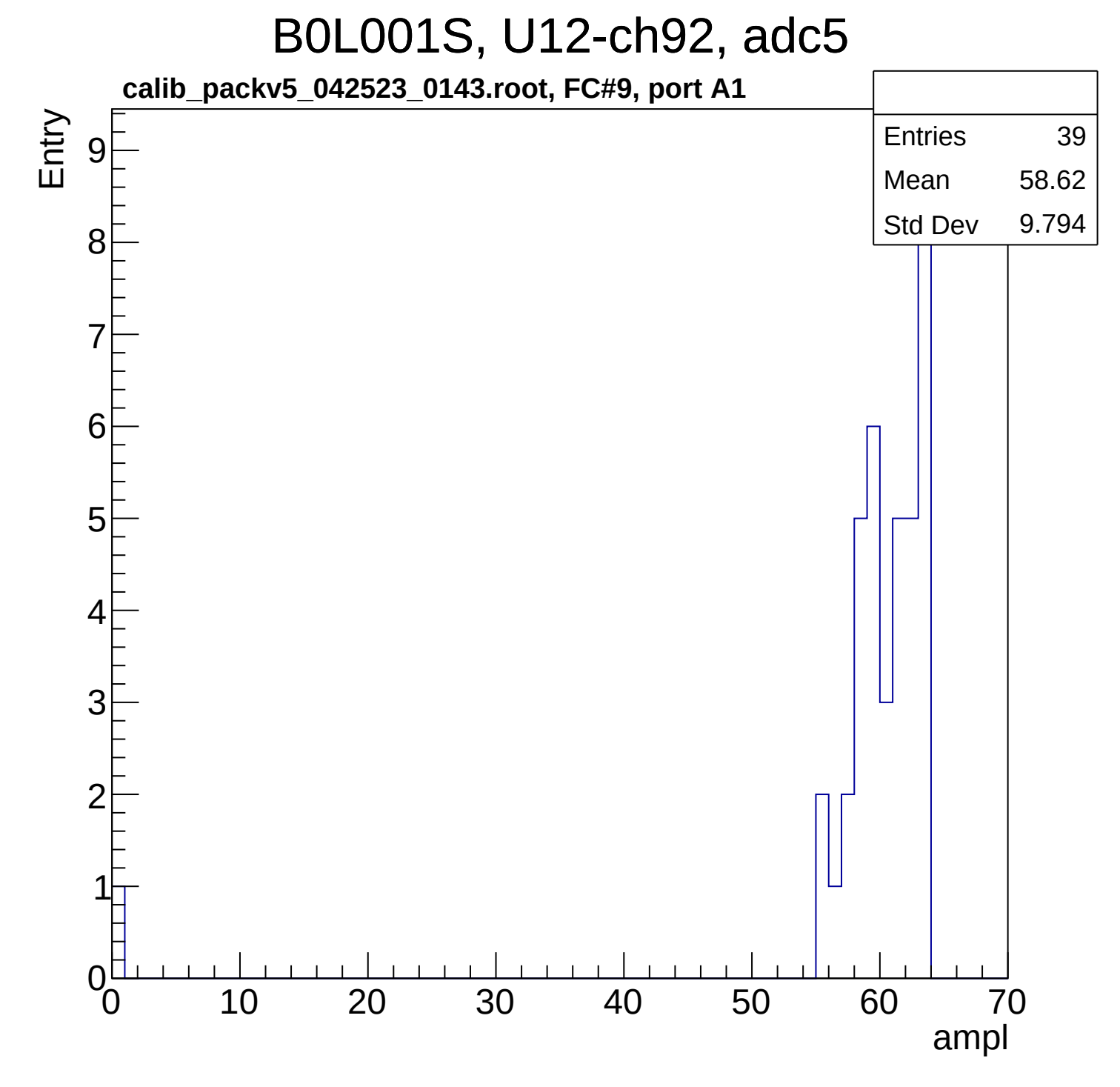
B0L001S, U12-ch92, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 39
Mean 58.62
Std Dev 9.794
Entry
ampl
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6
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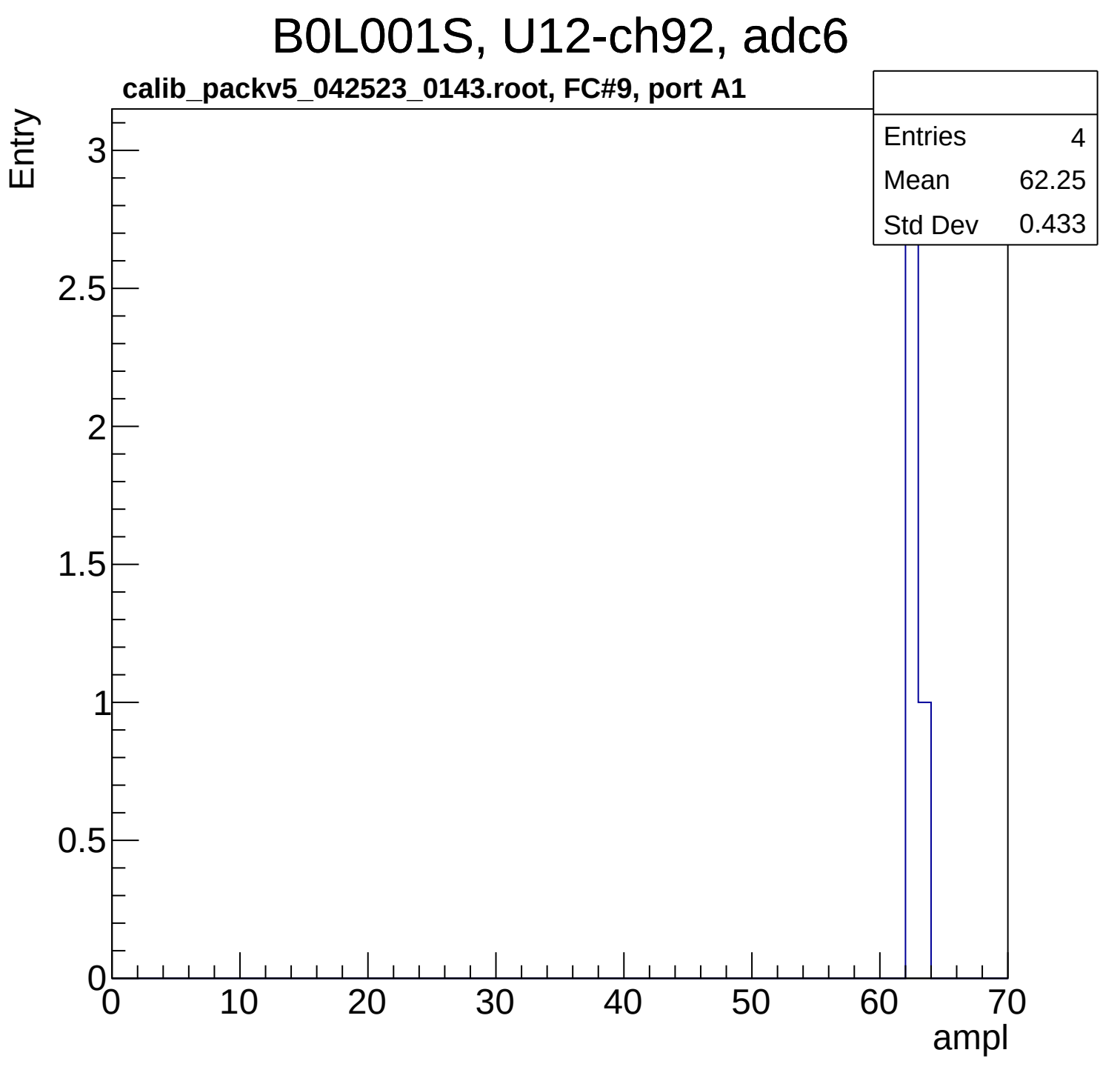
B0L001S, U12-ch92, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 4
Mean 62.25
Std Dev 0.433
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
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60
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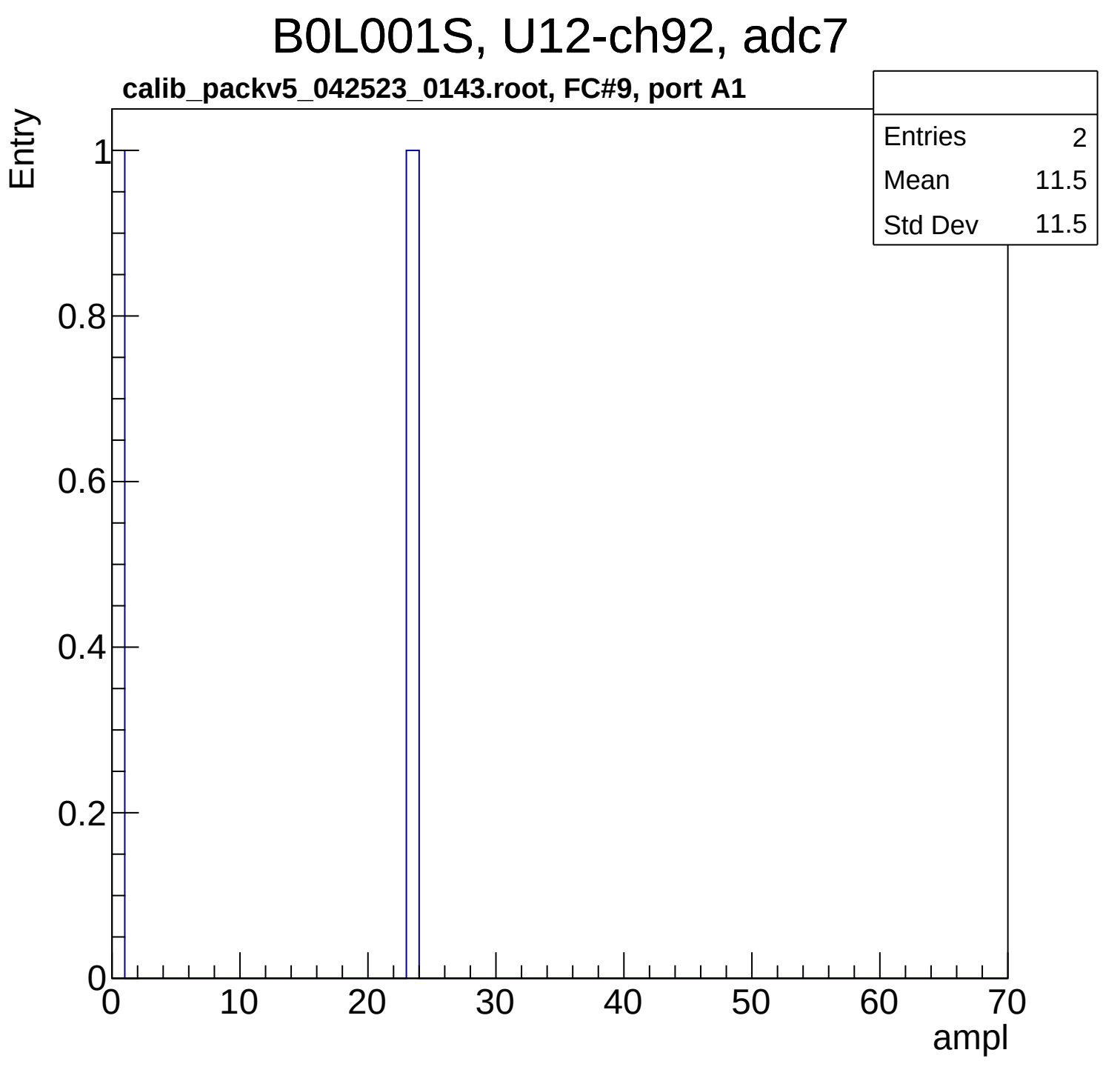
B0L001S, U12-ch92, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 11.5
Std Dev 11.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
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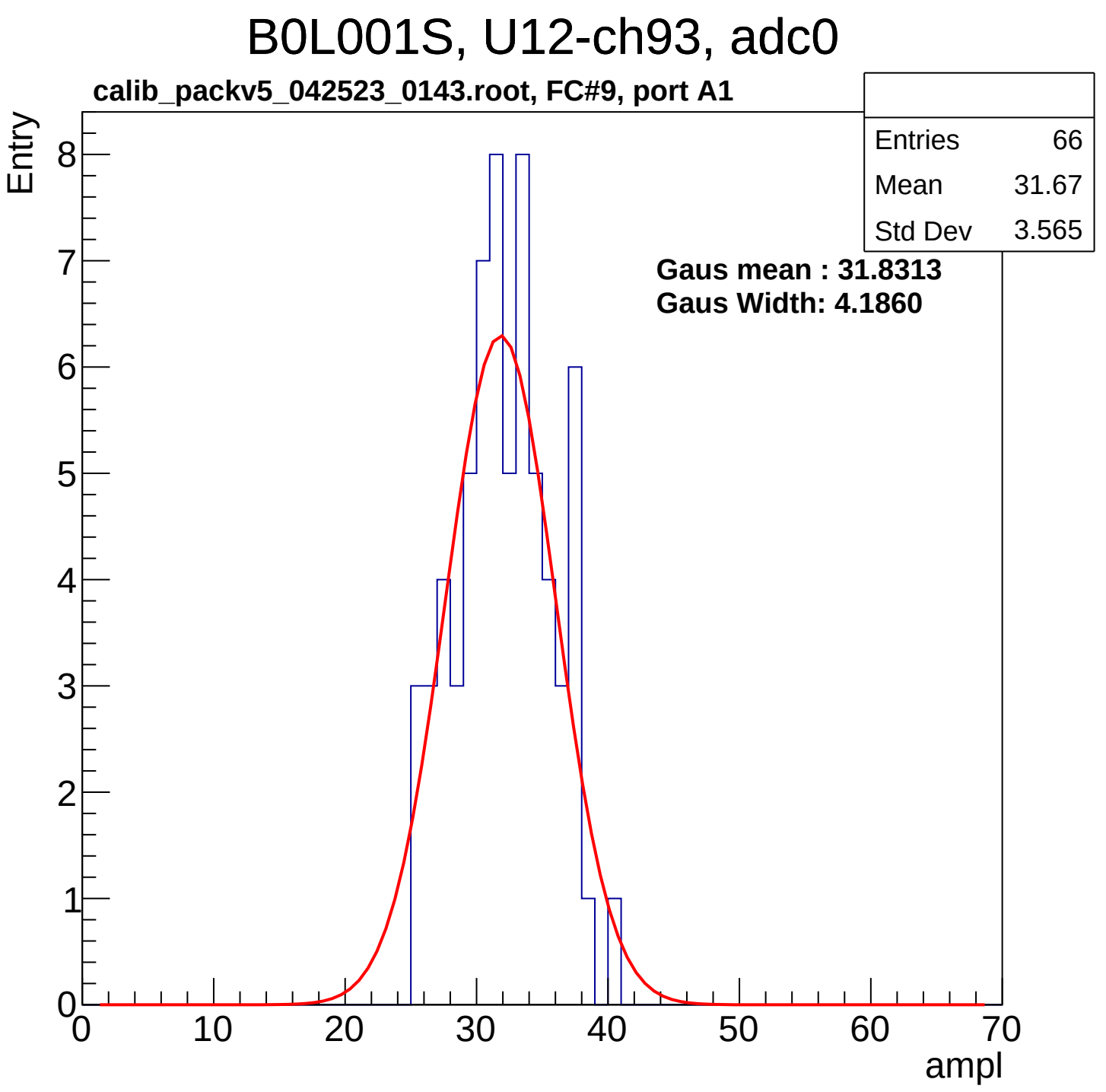
30
40
50
60
70
ampl


B0L001S, U12-ch93, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 66
Mean 31.67
Std Dev 3.565
Gaus mean : 31.8313
Gaus Width: 4.1860
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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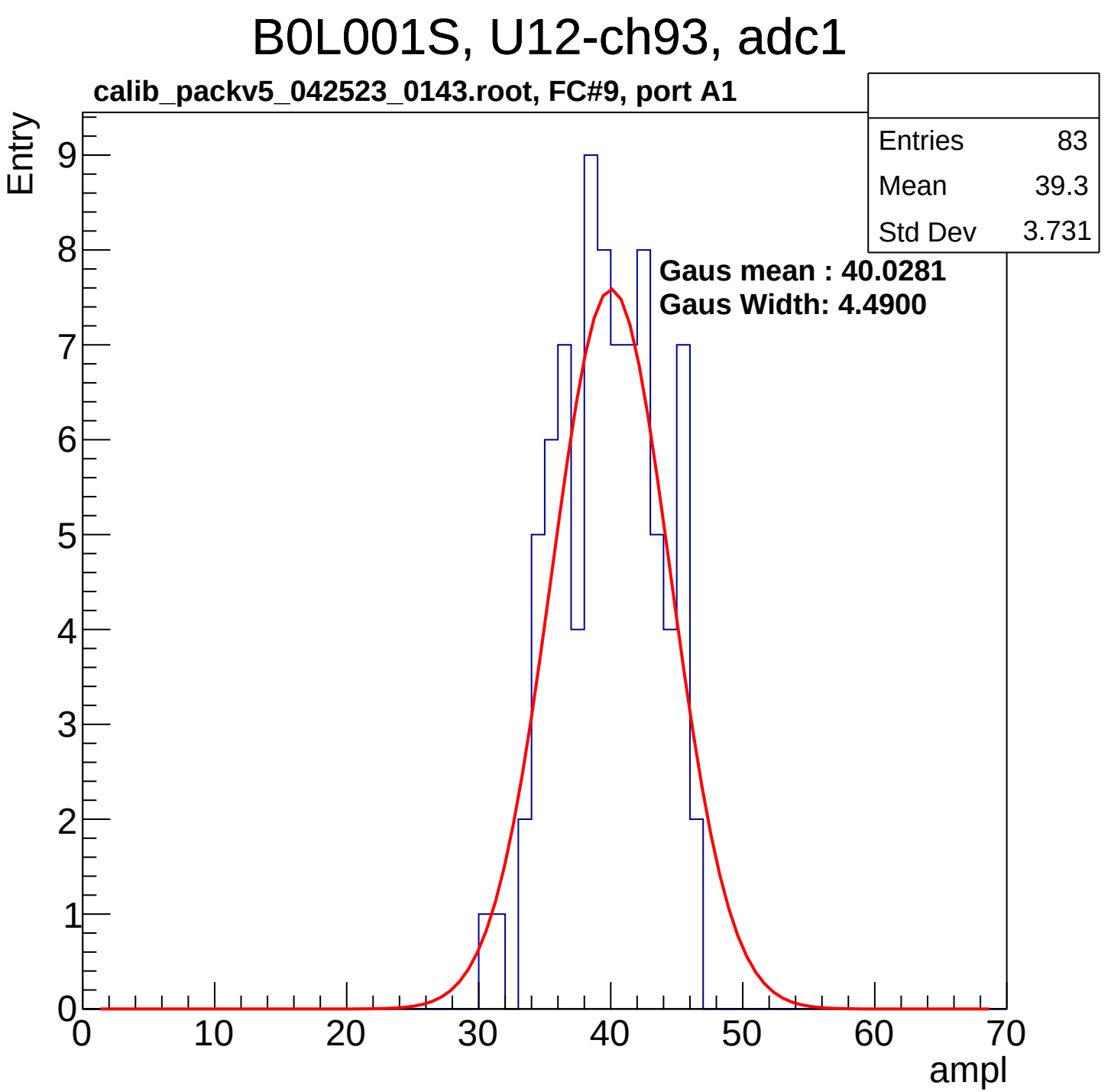
B0L001S, U12-ch93, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 83
Mean 39.3
Std Dev 3.731
Gaus mean : 40.0281
Gaus Width: 4.4900
Entry
ampl
0
1
2
3
4
5
6
7
8
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0
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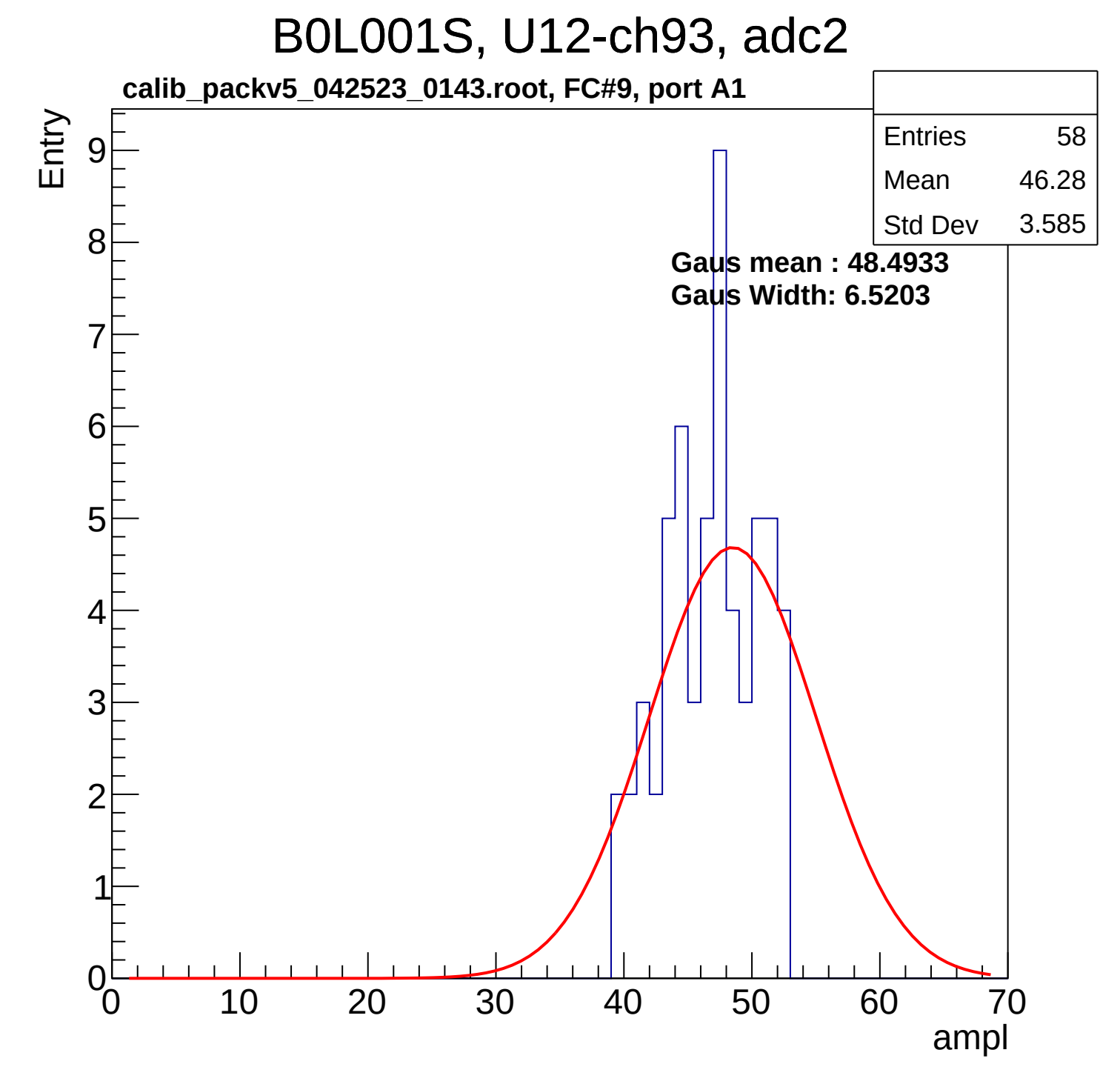
B0L001S, U12-ch93, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 58
Mean 46.28
Std Dev 3.585
Gaus mean : 48.4933
Gaus Width: 6.5203
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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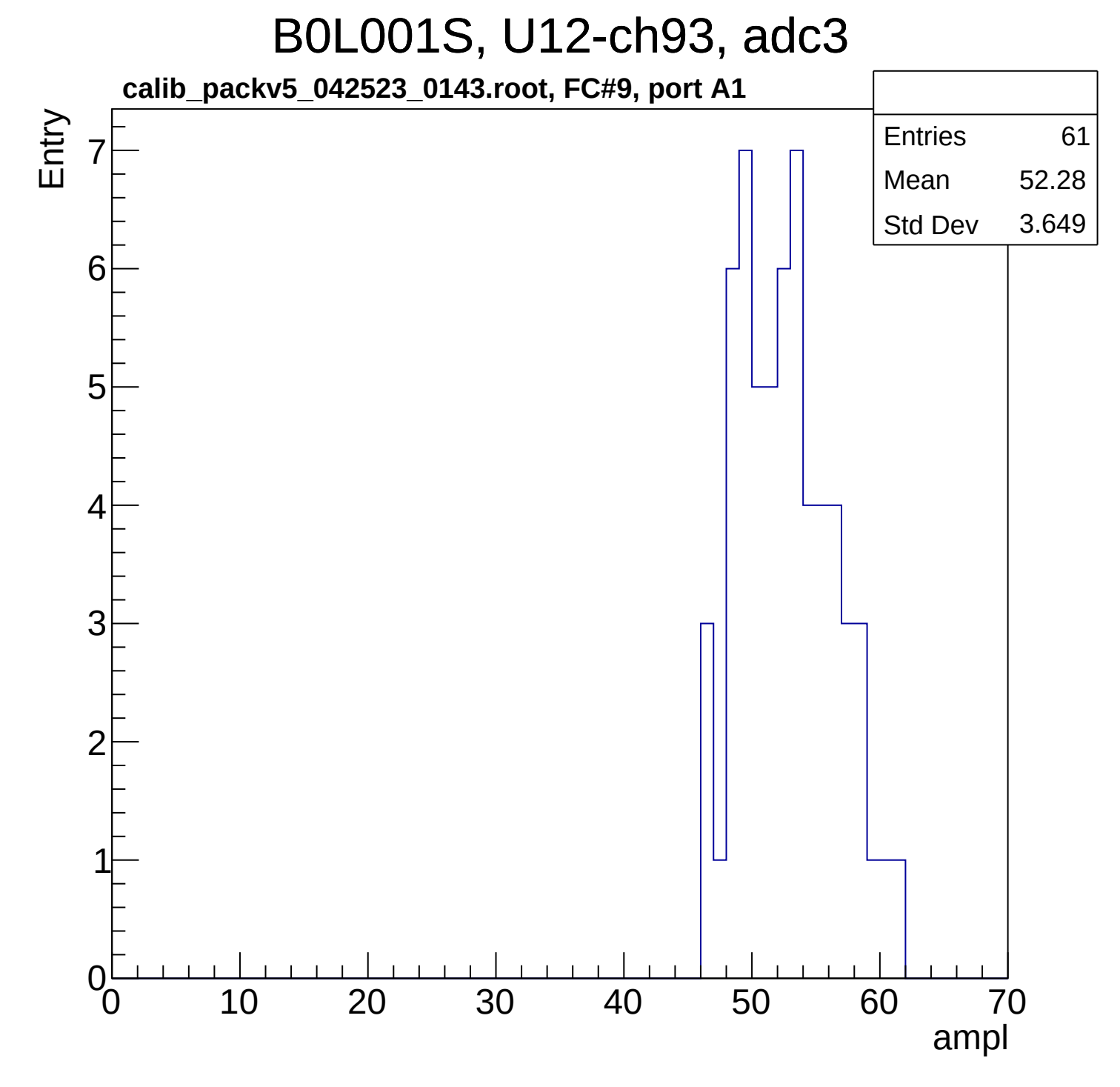
B0L001S, U12-ch93, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 61
Mean 52.28
Std Dev 3.649
Entry
ampl
0
1
2
3
4
5
6
7
0
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50
60
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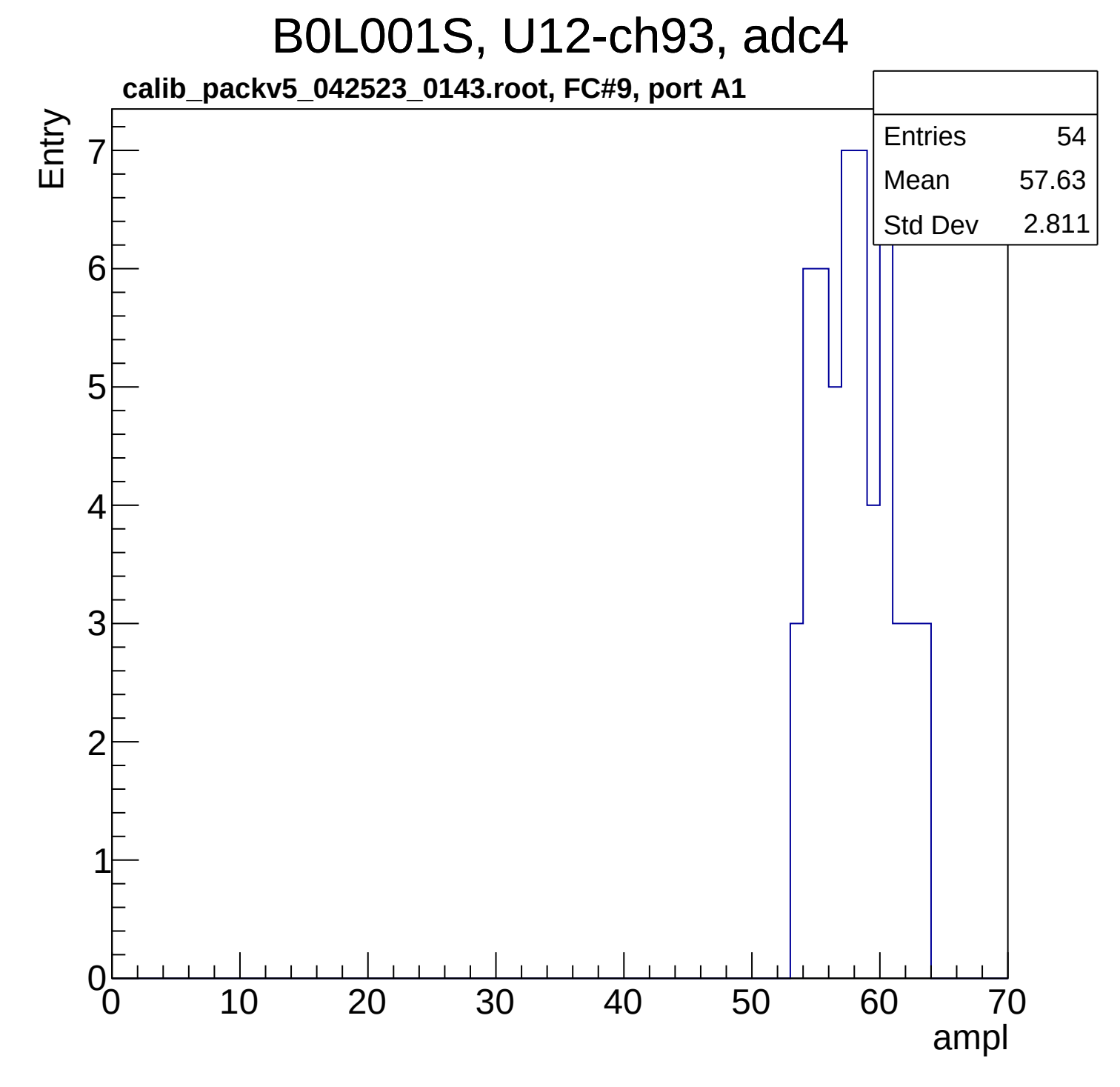
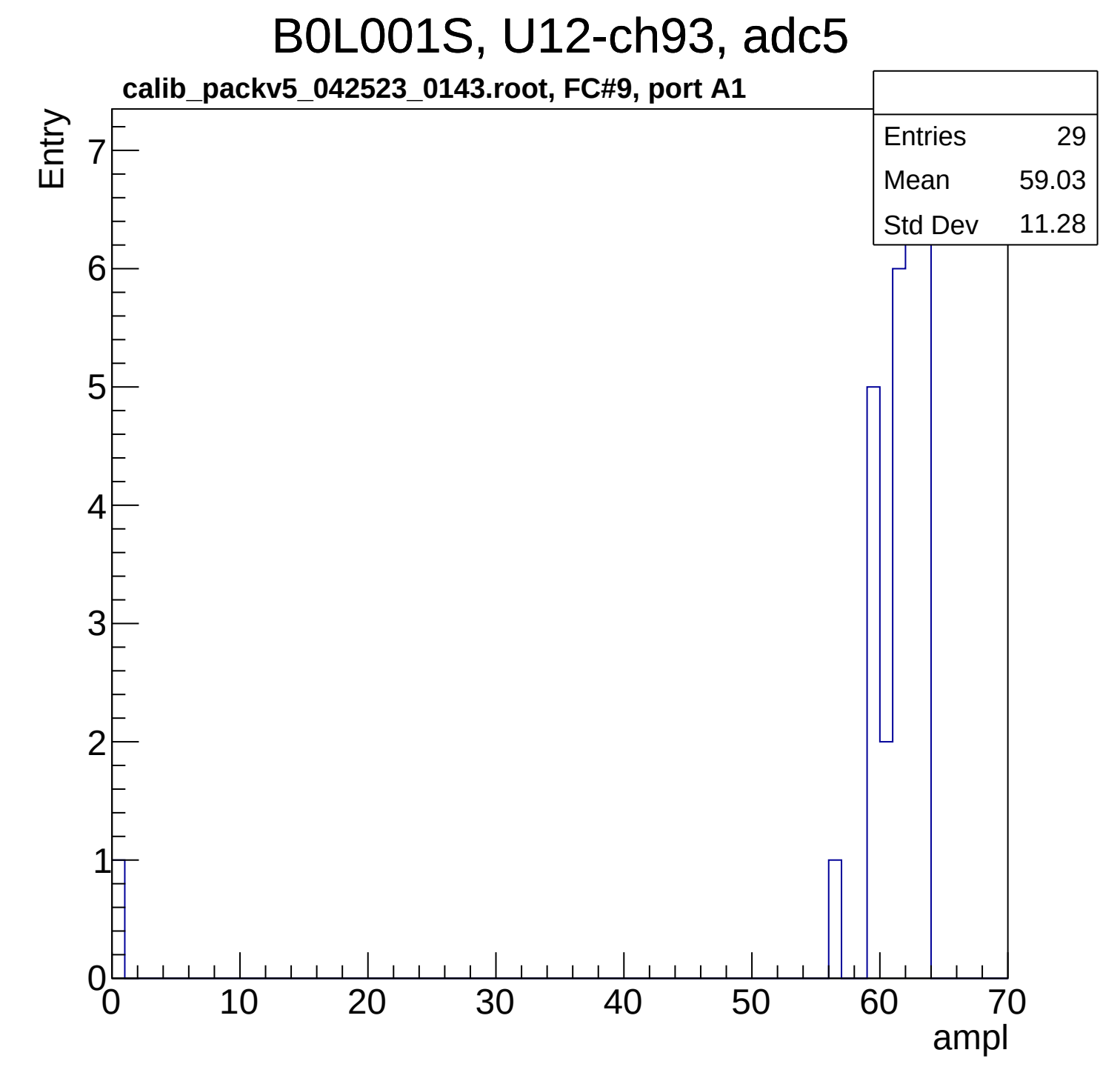
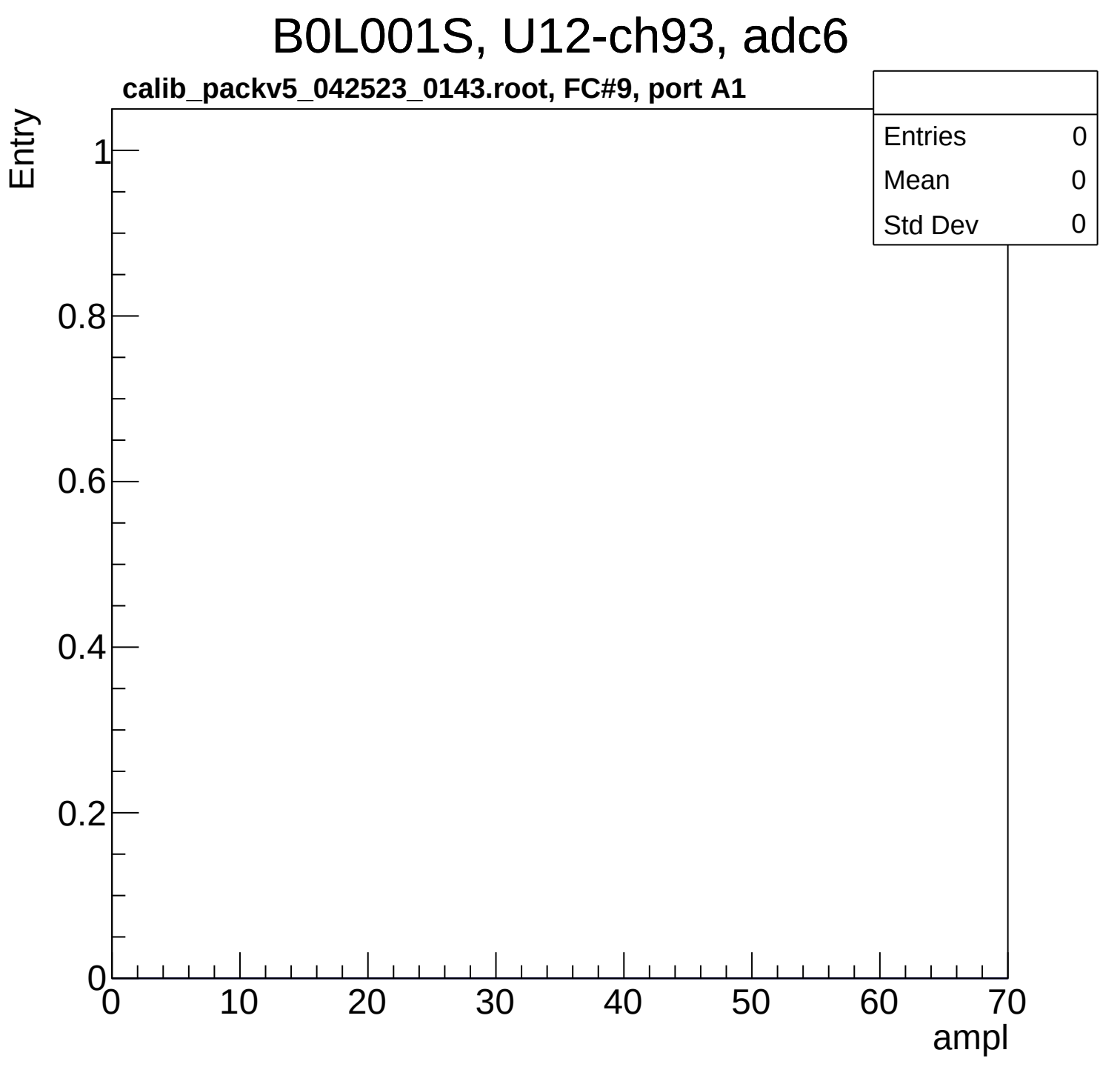
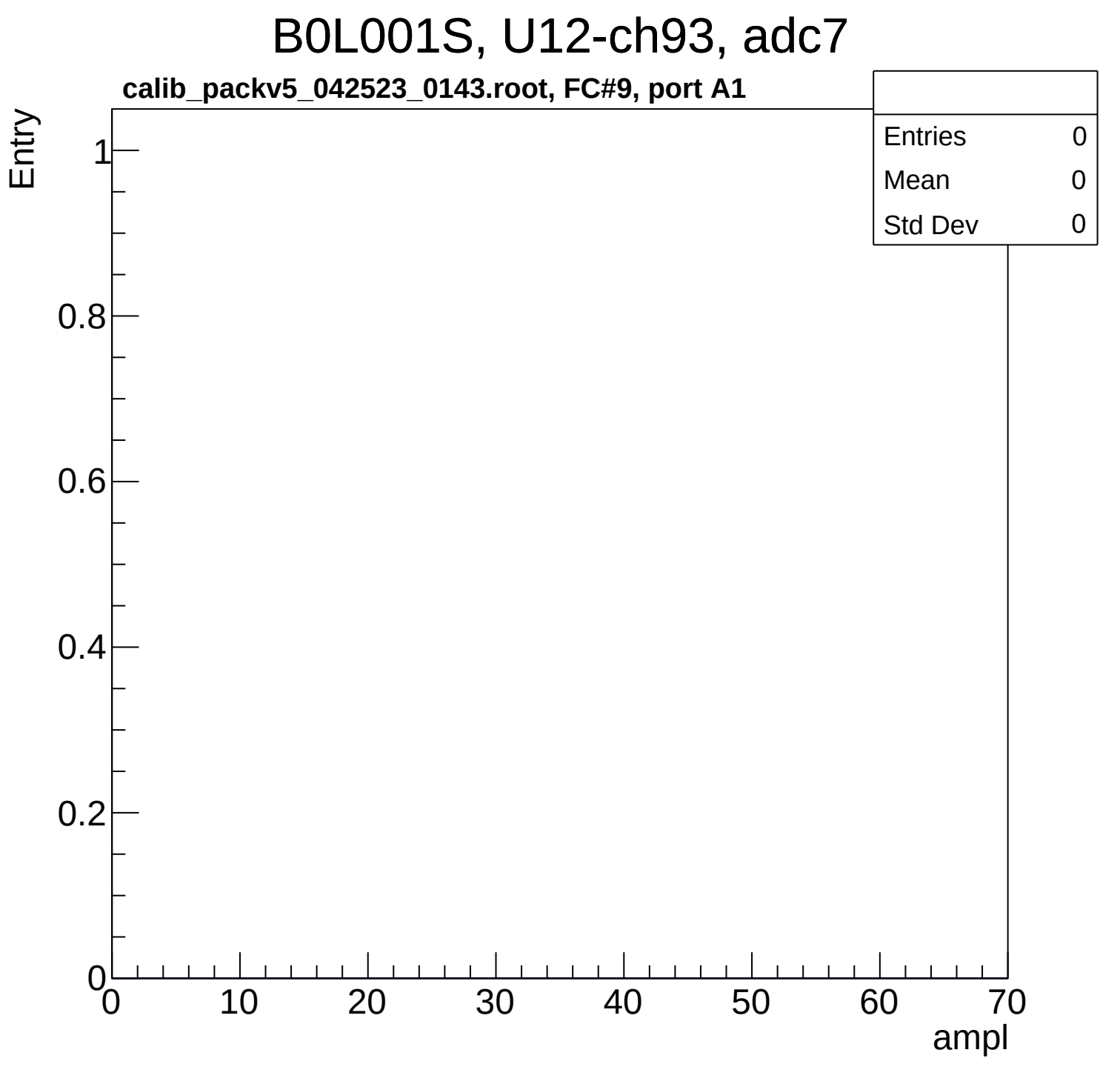
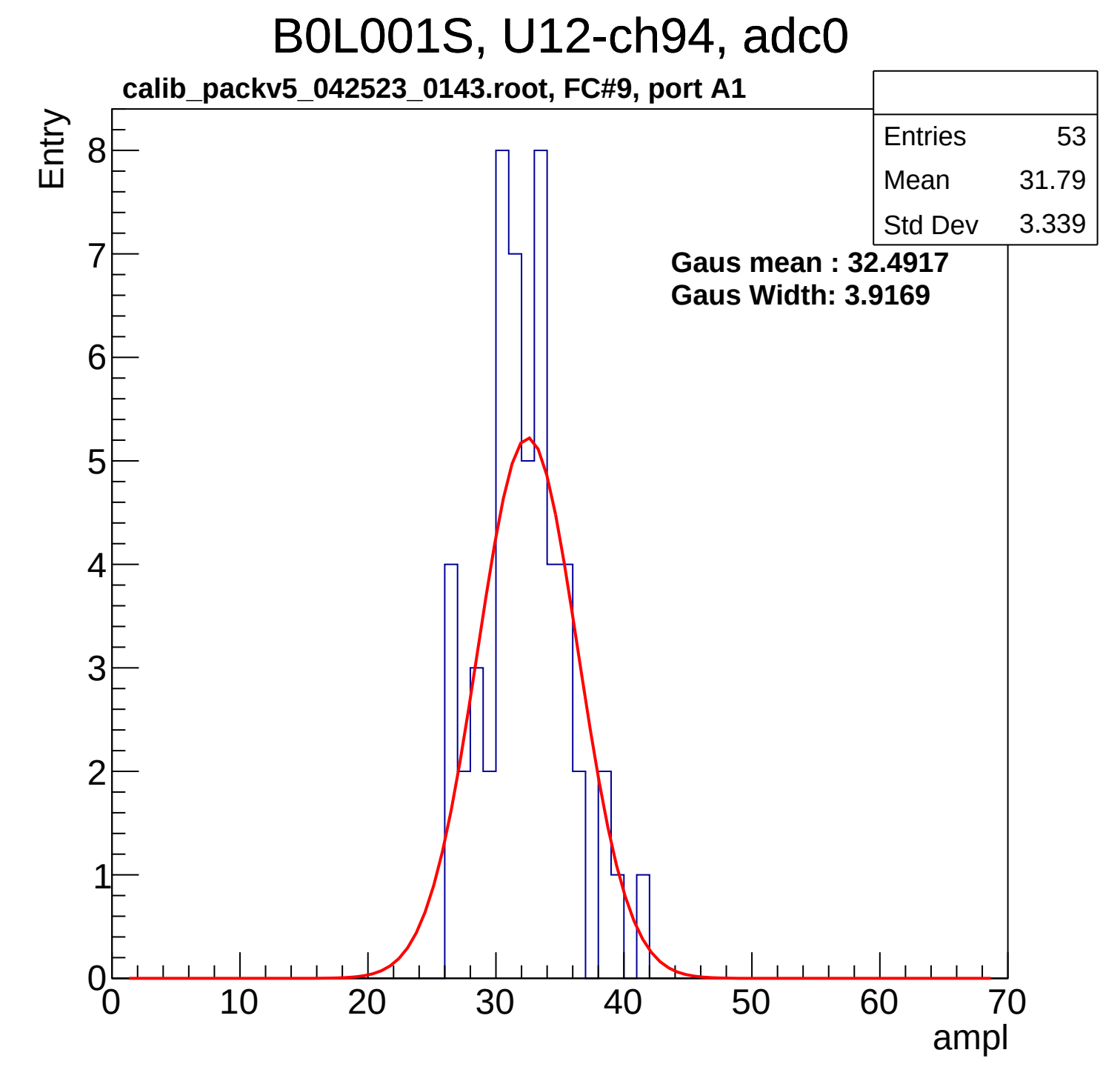

B0L001S, U12-ch93, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 54
Mean 57.63
Std Dev 2.811
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B0L001S, U12-ch93, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 29
Mean 59.03
Std Dev 11.28
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch93, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch93, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch94, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 53
Mean 31.79
Std Dev 3.339
Gaus mean : 32.4917
Gaus Width: 3.9169
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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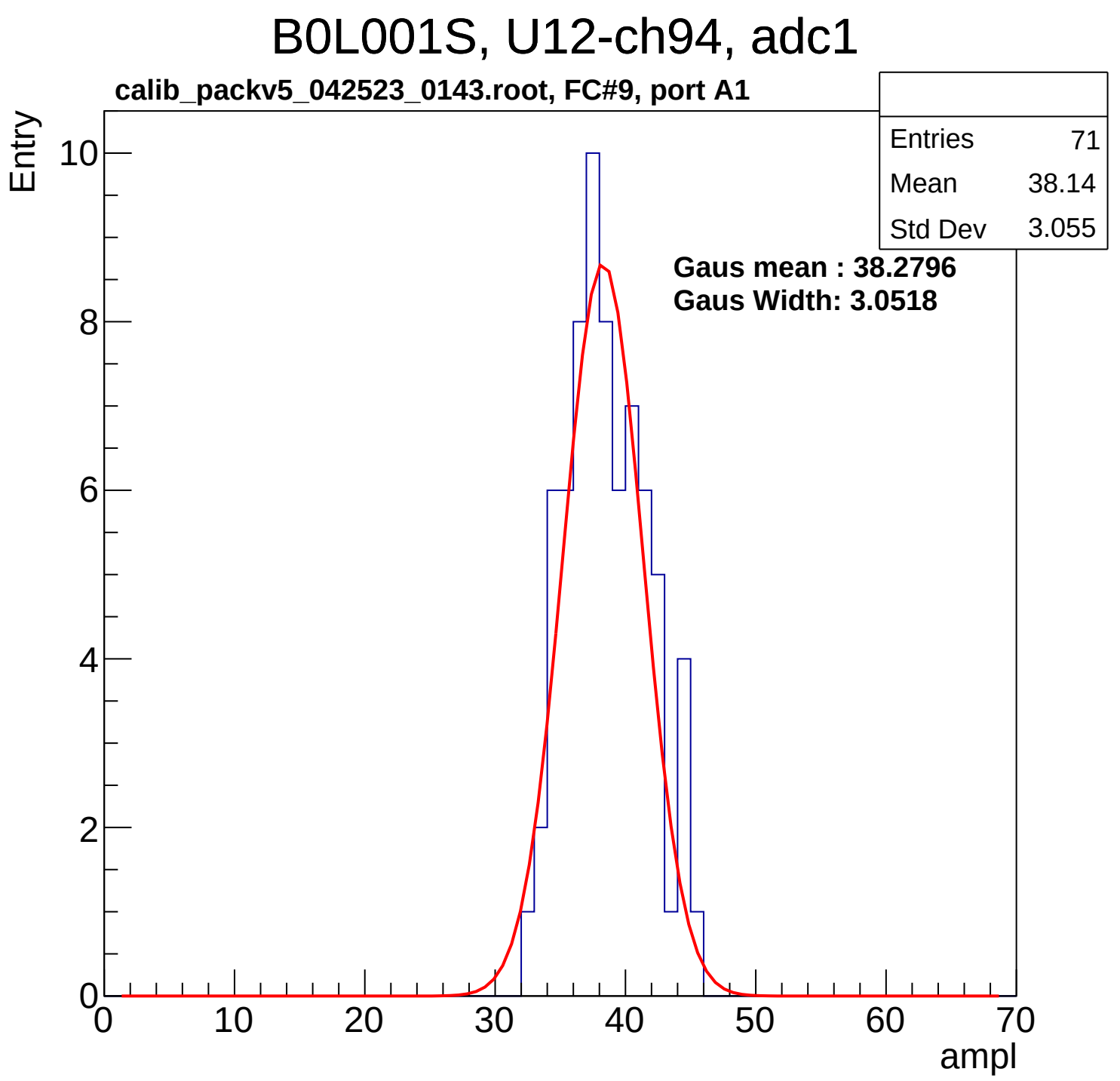
40
50
60
70


B0L001S, U12-ch94, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 71
Mean 38.14
Std Dev 3.055
Gaus mean : 38.2796
Gaus Width: 3.0518
Entry
ampl
0
2
4
6
8
10
0
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20
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40
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60
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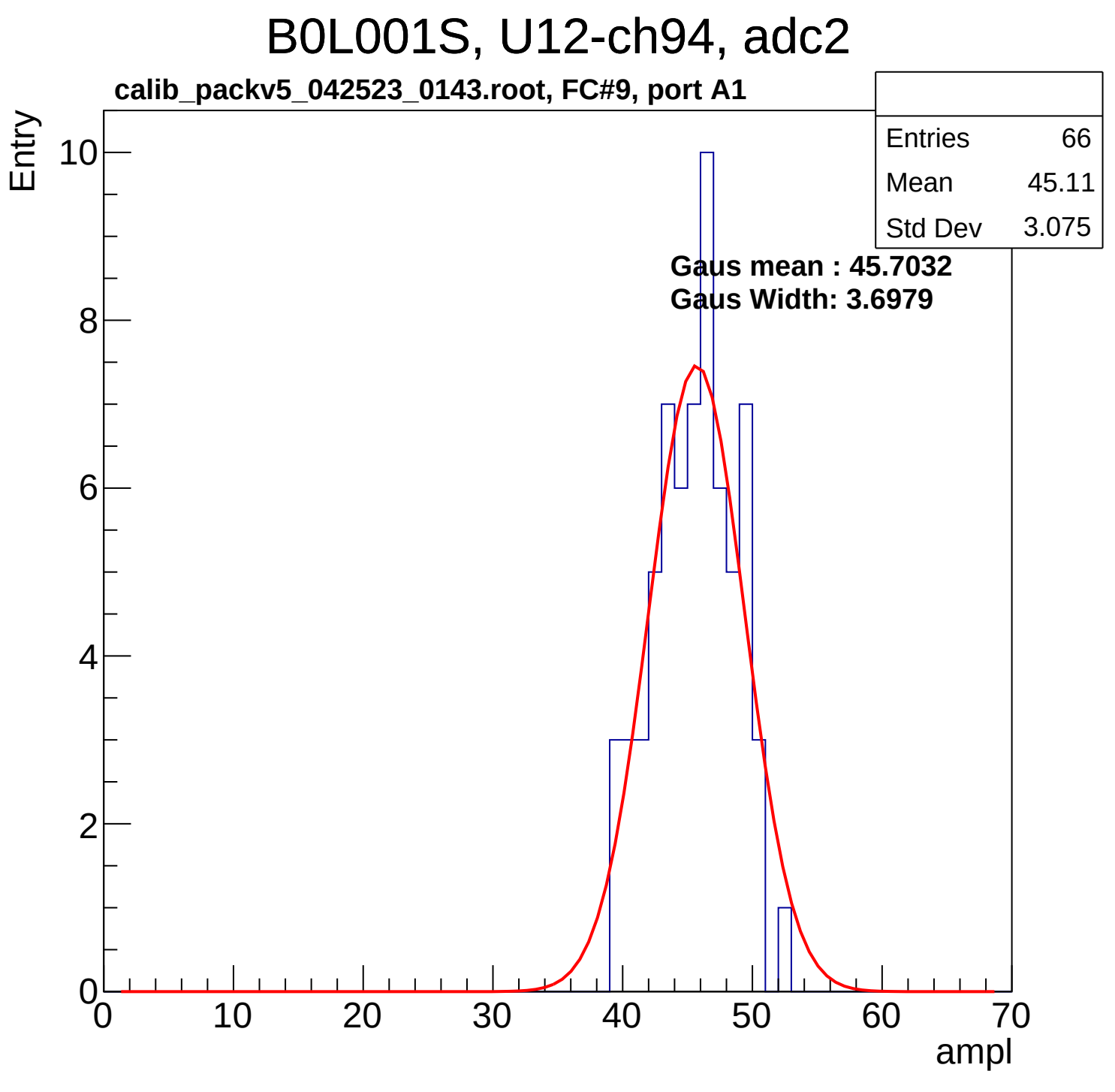
B0L001S, U12-ch94, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 66
Mean 45.11
Std Dev 3.075
Gaus mean : 45.7032
Gaus Width: 3.6979
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
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60
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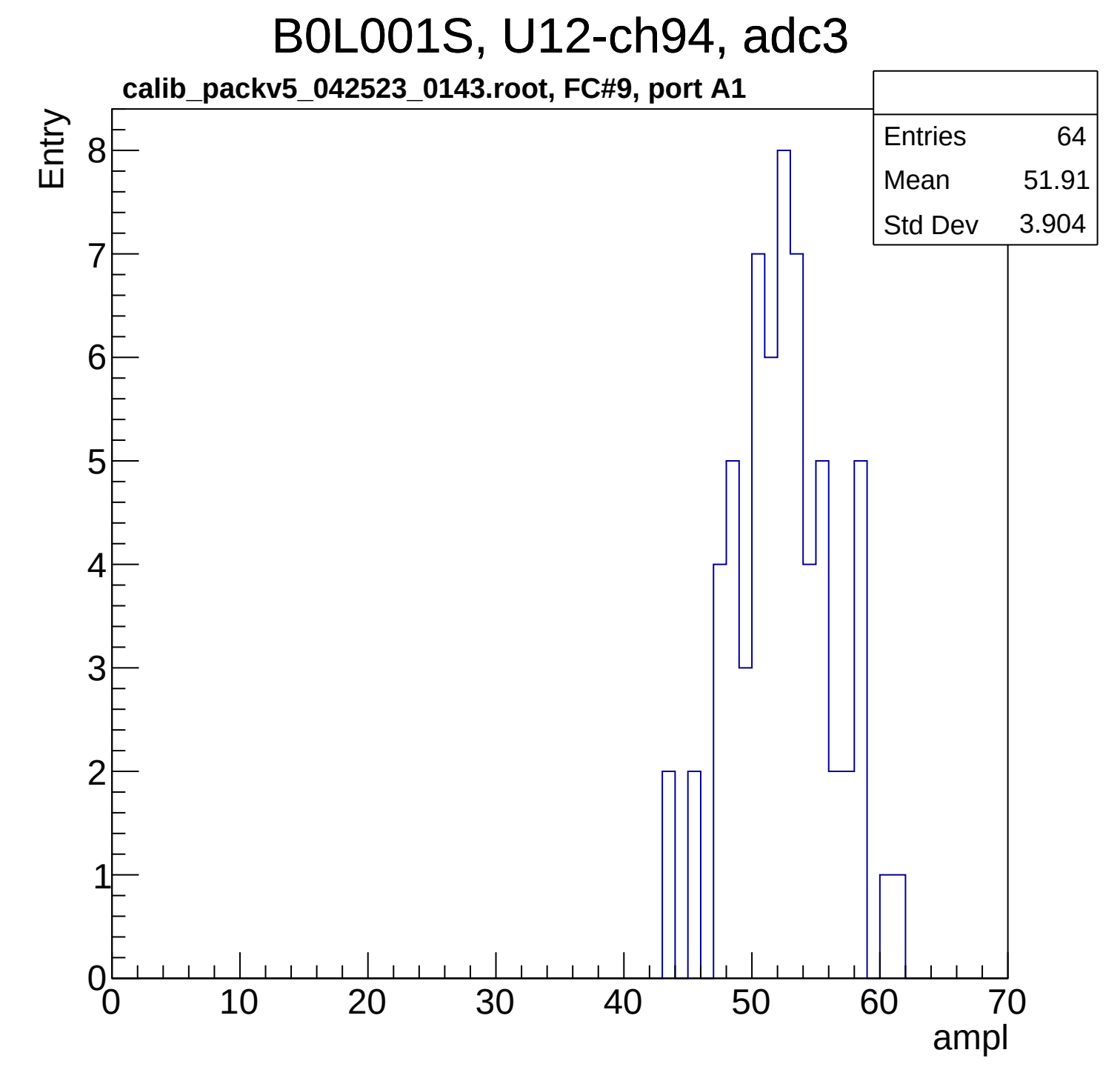
B0L001S, U12-ch94, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 64
Mean 51.91
Std Dev 3.904
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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60
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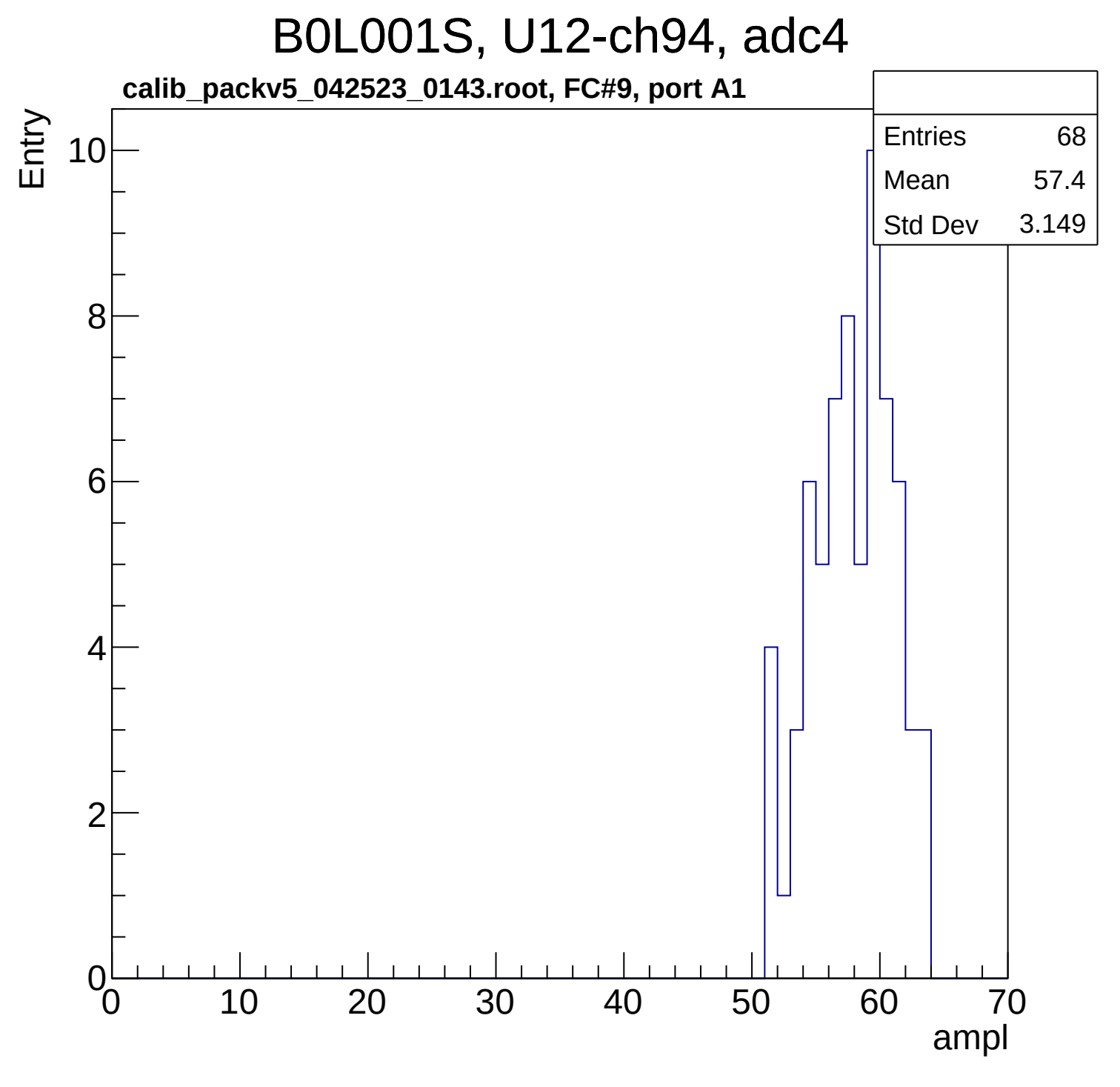
B0L001S, U12-ch94, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 68
Mean 57.4
Std Dev 3.149
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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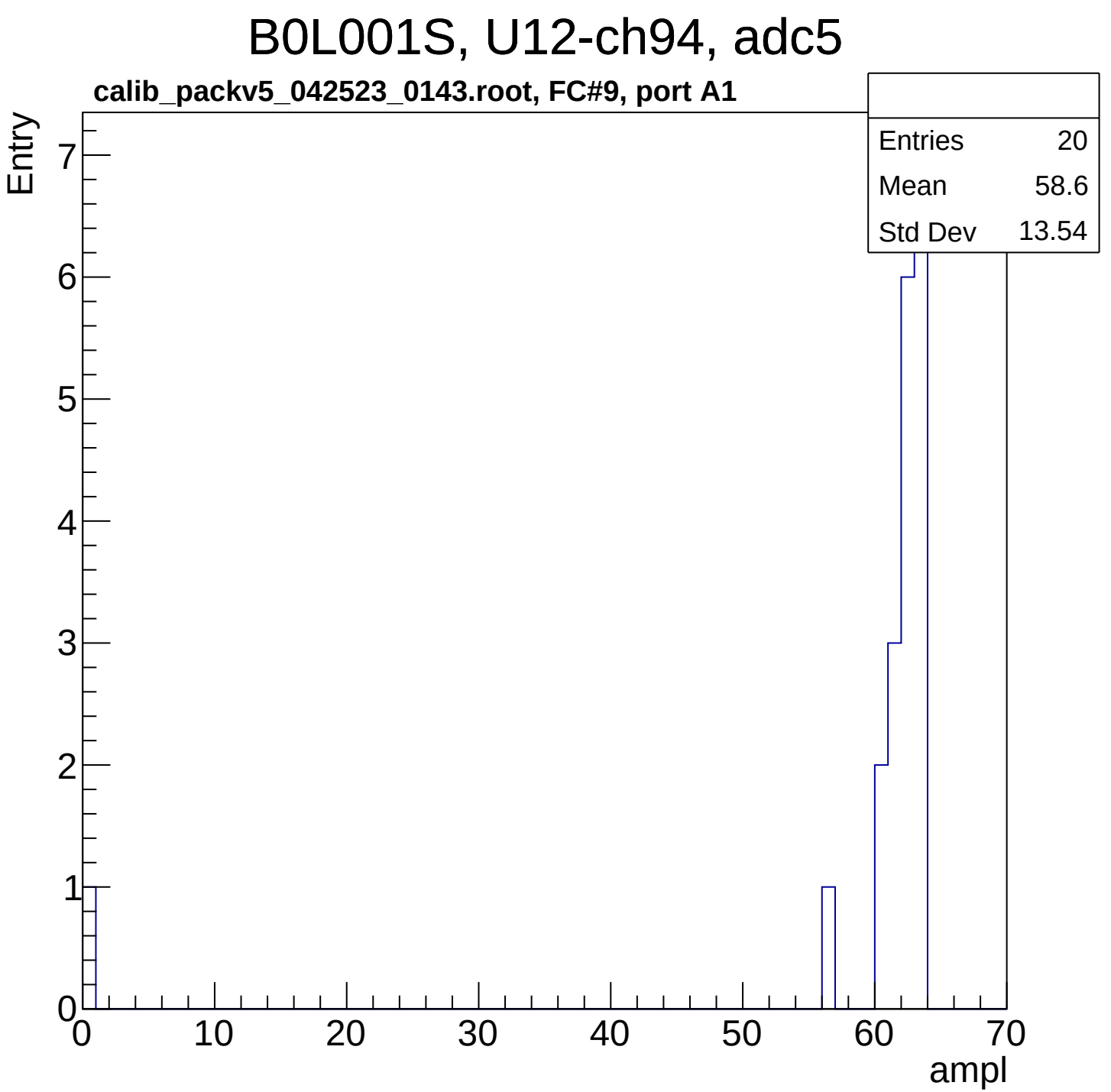
B0L001S, U12-ch94, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 20
Mean 58.6
Std Dev 13.54
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
50
60
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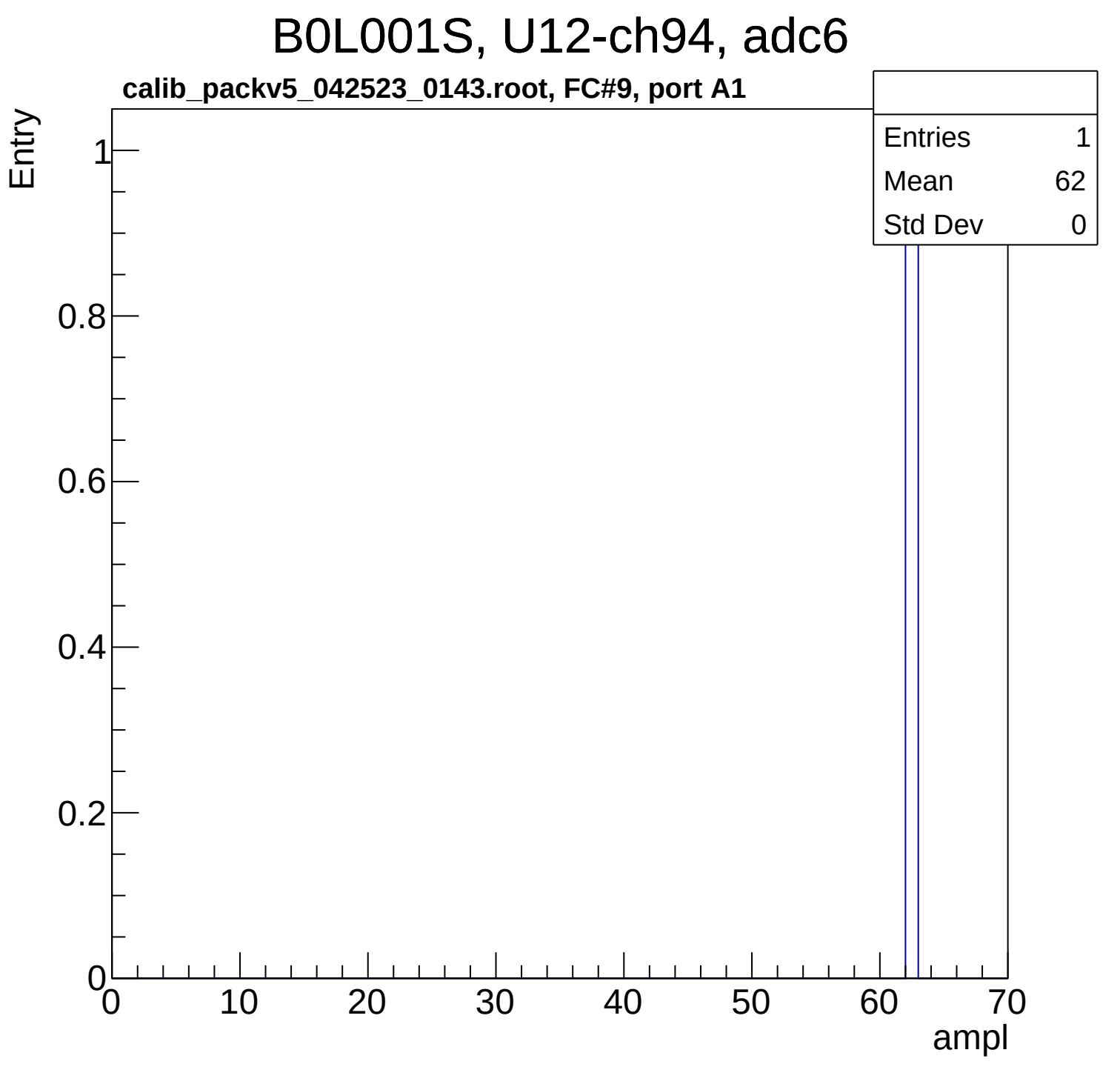
B0L001S, U12-ch94, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 62
Std Dev 0
Entry
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0.8
0.6
0.4
0.2
0
0
10
20
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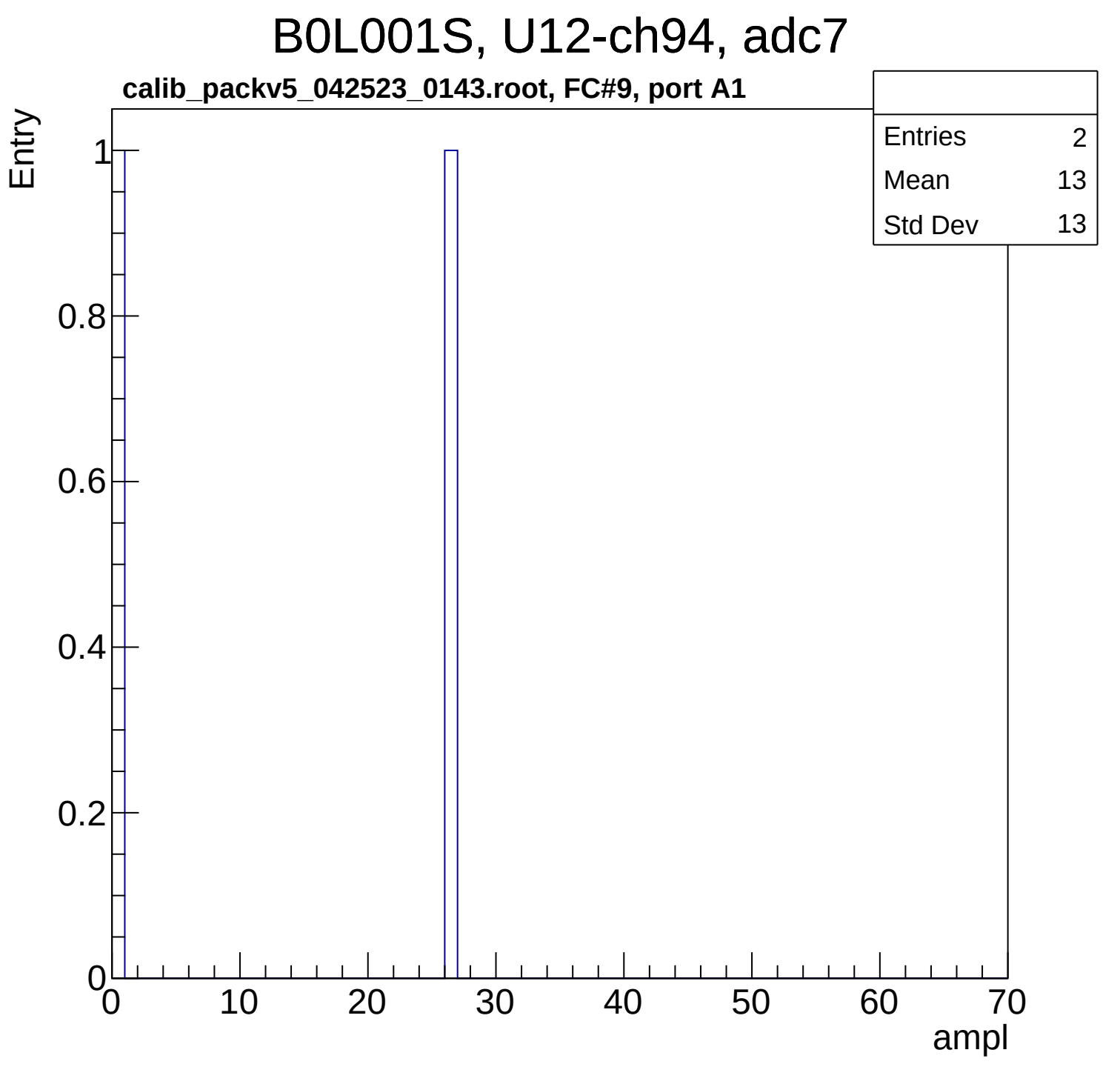
50
60
70
ampl


B0L001S, U12-ch94, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 13
Std Dev 13
Entry
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0.8
0.6
0.4
0.2
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10
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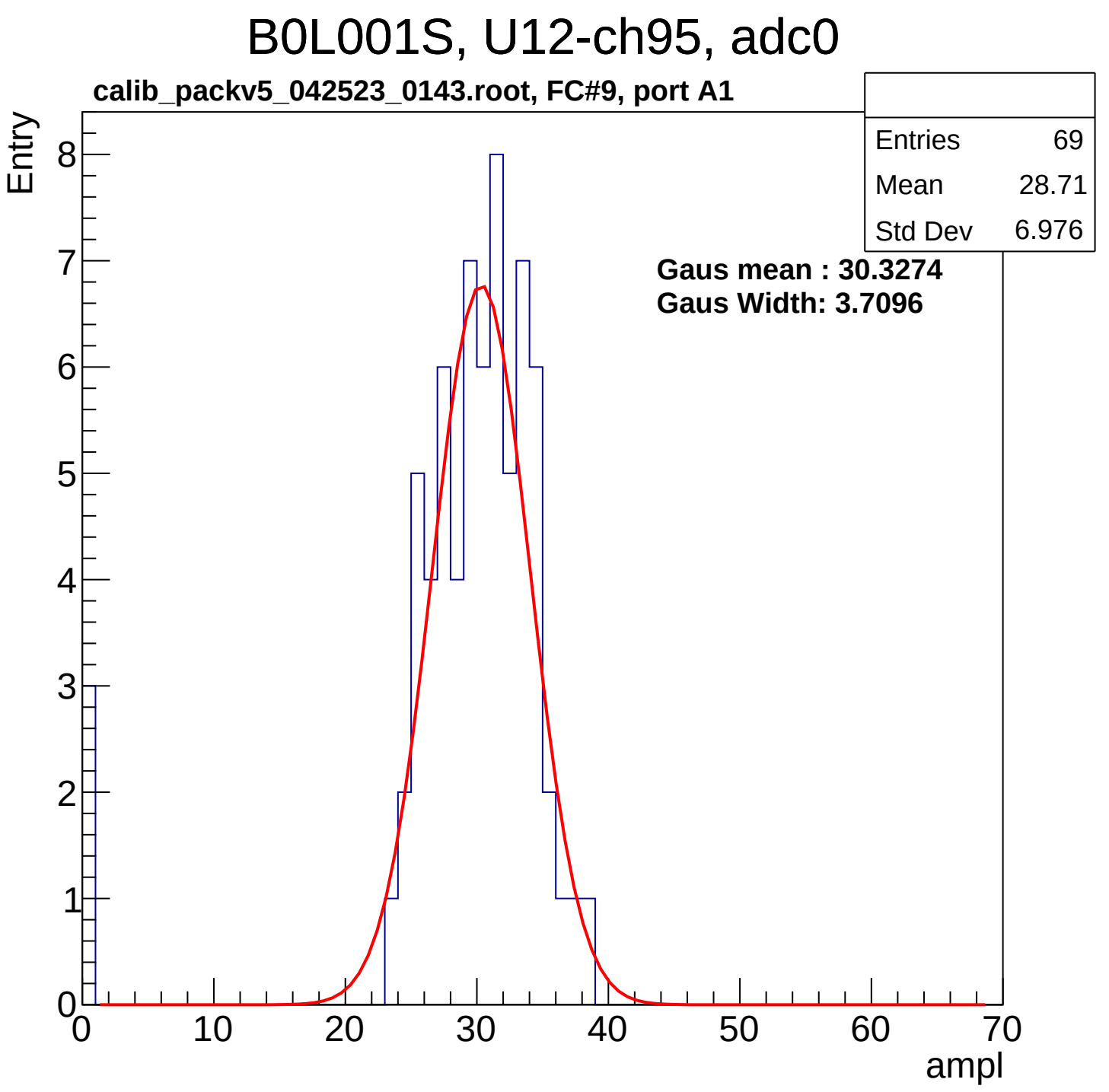
60
70
ampl


B0L001S, U12-ch95, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 69
Mean 28.71
Std Dev 6.976
Gaus mean : 30.3274
Gaus Width: 3.7096
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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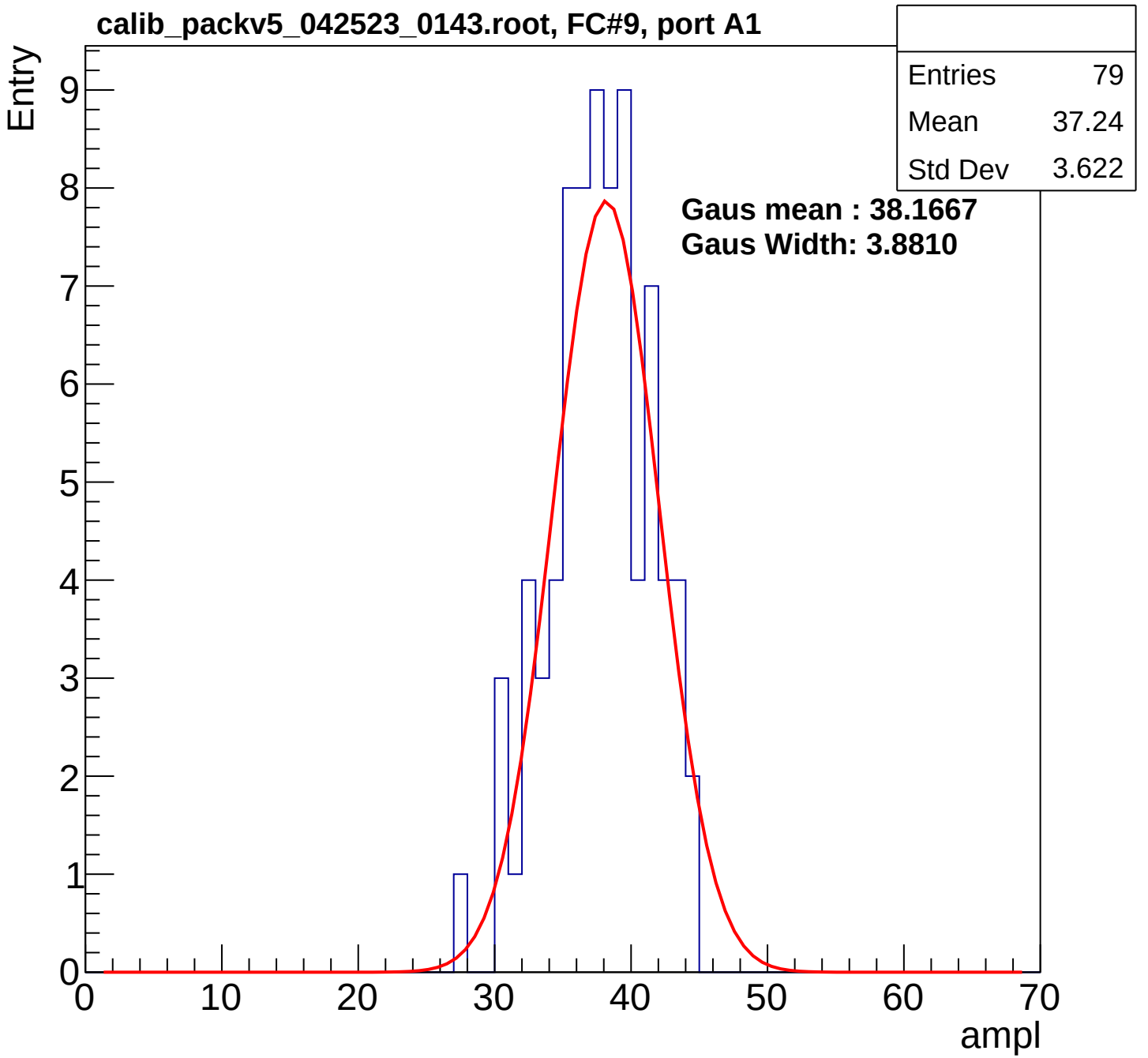
B0L001S, U12-ch95, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 79
Mean 37.24
Std Dev 3.622
Gaus mean : 38.1667
Gaus Width: 3.8810
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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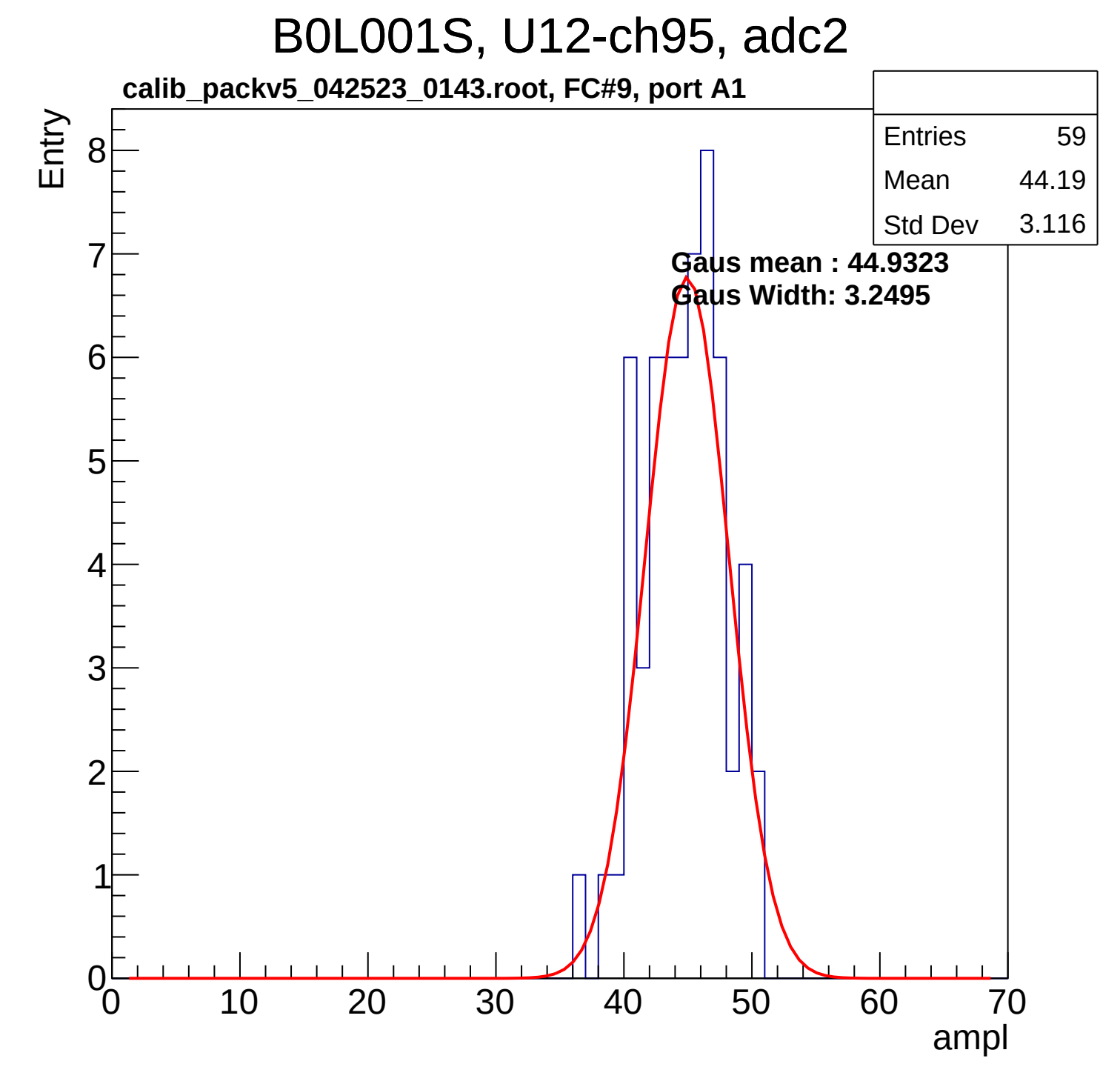
B0L001S, U12-ch95, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 59
Mean 44.19
Std Dev 3.116
Gaus mean : 44.9323
Gaus Width: 3.2495
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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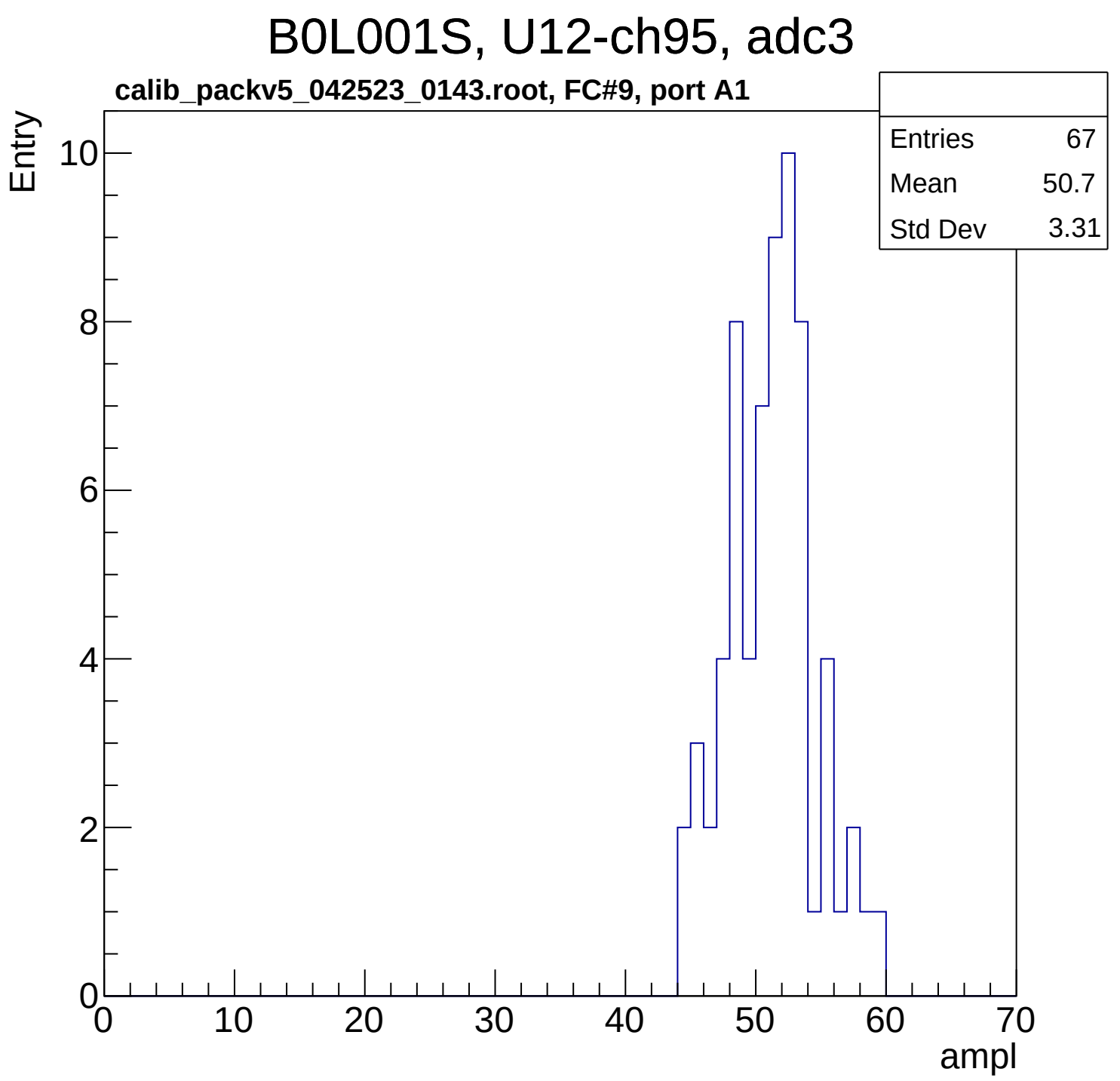
B0L001S, U12-ch95, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 67
Mean 50.7
Std Dev 3.31
Entry
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2
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6
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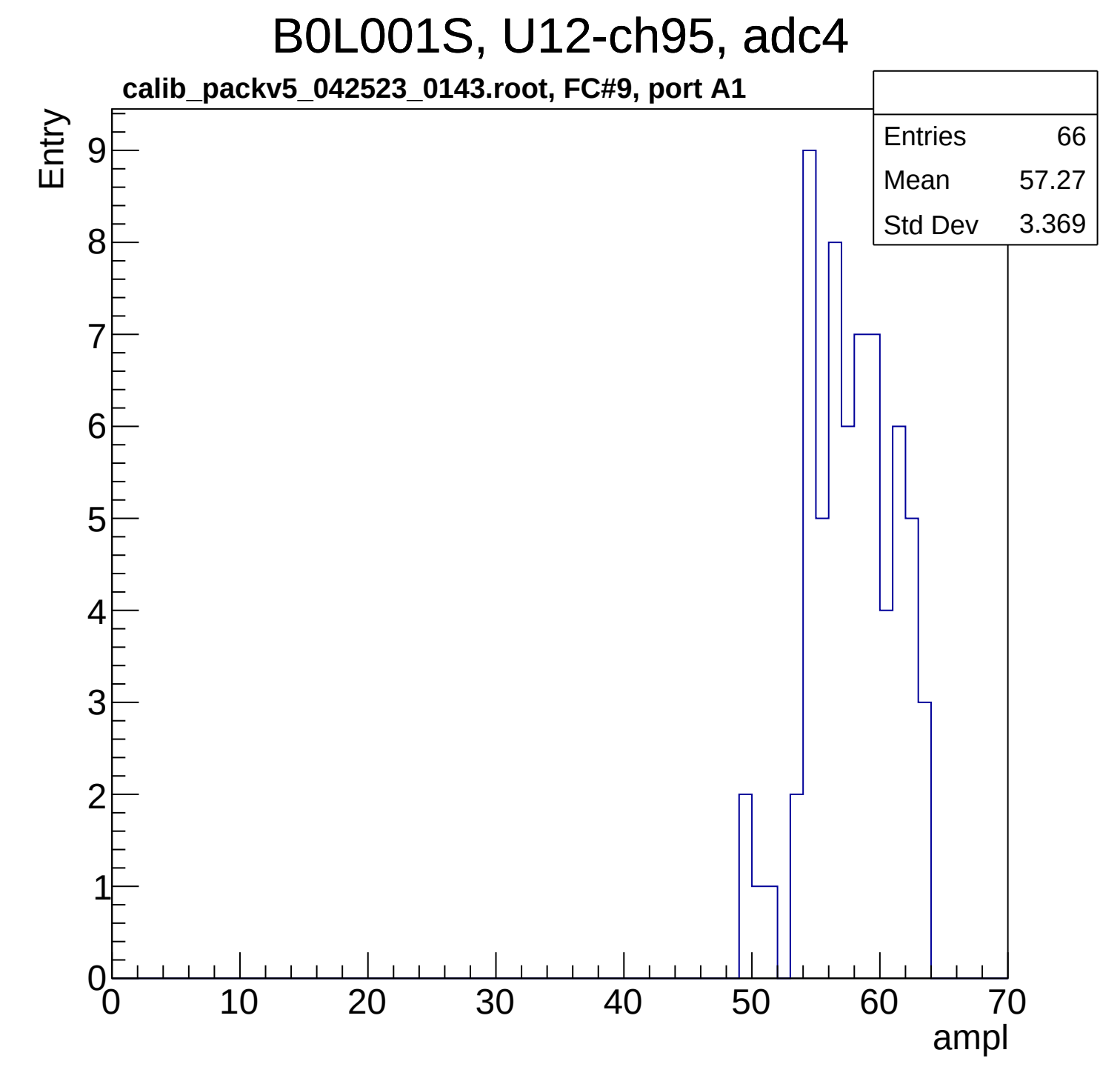
10
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch95, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 66
Mean 57.27
Std Dev 3.369
Entry
ampl
0
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2
3
4
5
6
7
8
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0
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40
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60
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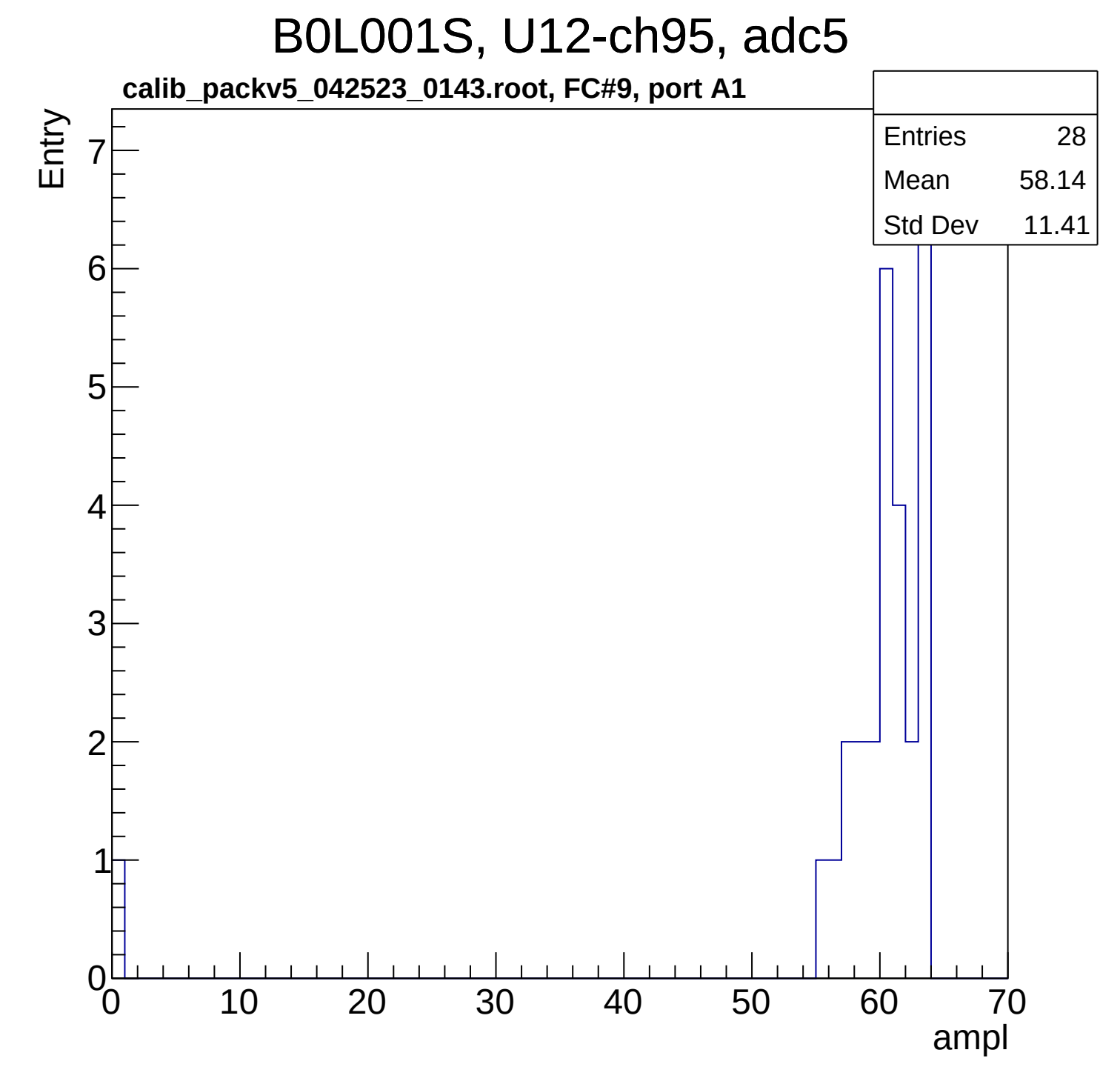
B0L001S, U12-ch95, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 28
Mean 58.14
Std Dev 11.41
Entry
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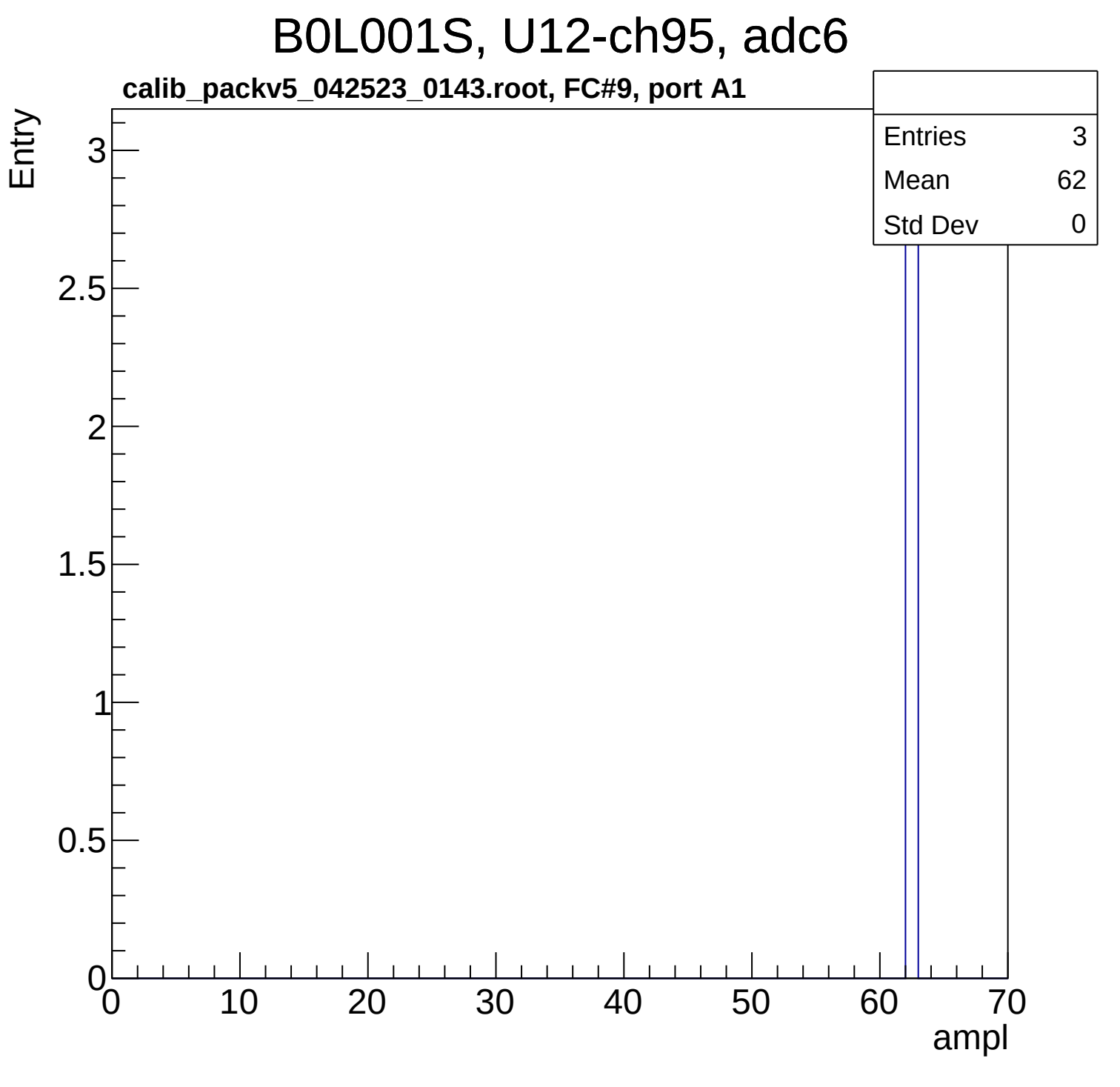
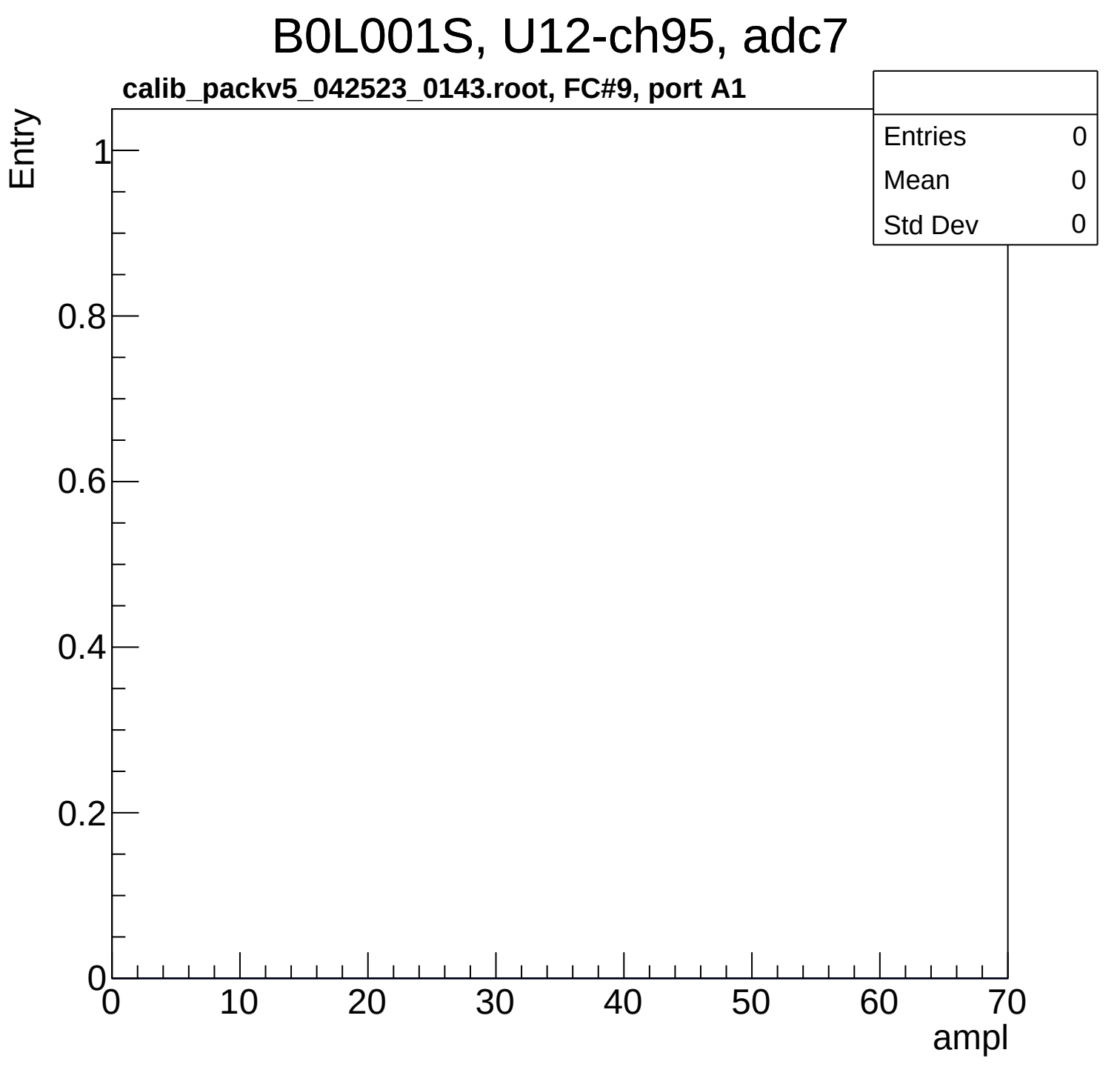
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch95, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 3
Mean 62
Std Dev 0
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B0L001S, U12-ch95, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
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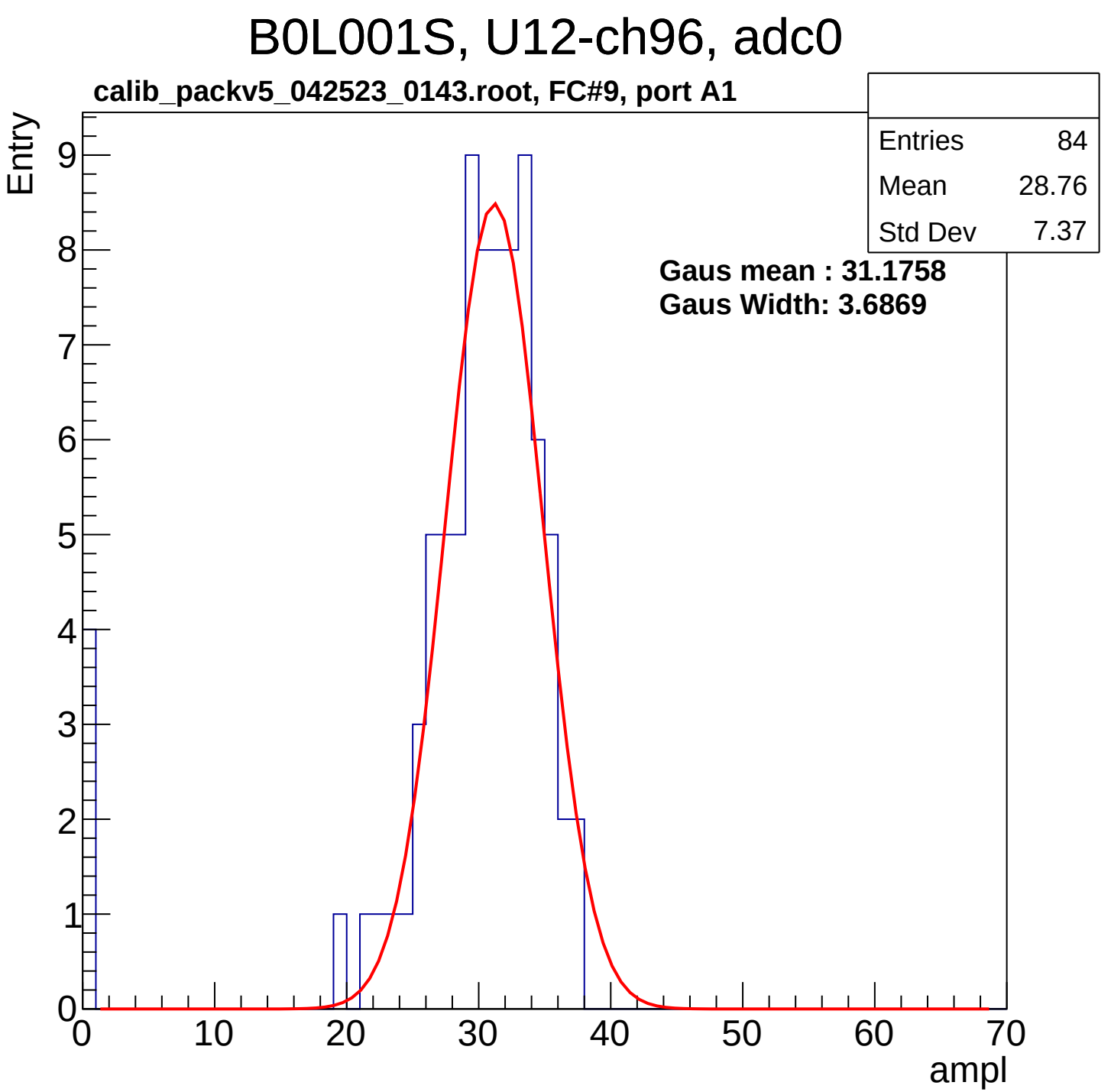
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch96, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 84
Mean 28.76
Std Dev 7.37
Gaus mean : 31.1758
Gaus Width: 3.6869
Entry
ampl
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2
3
4
5
6
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0
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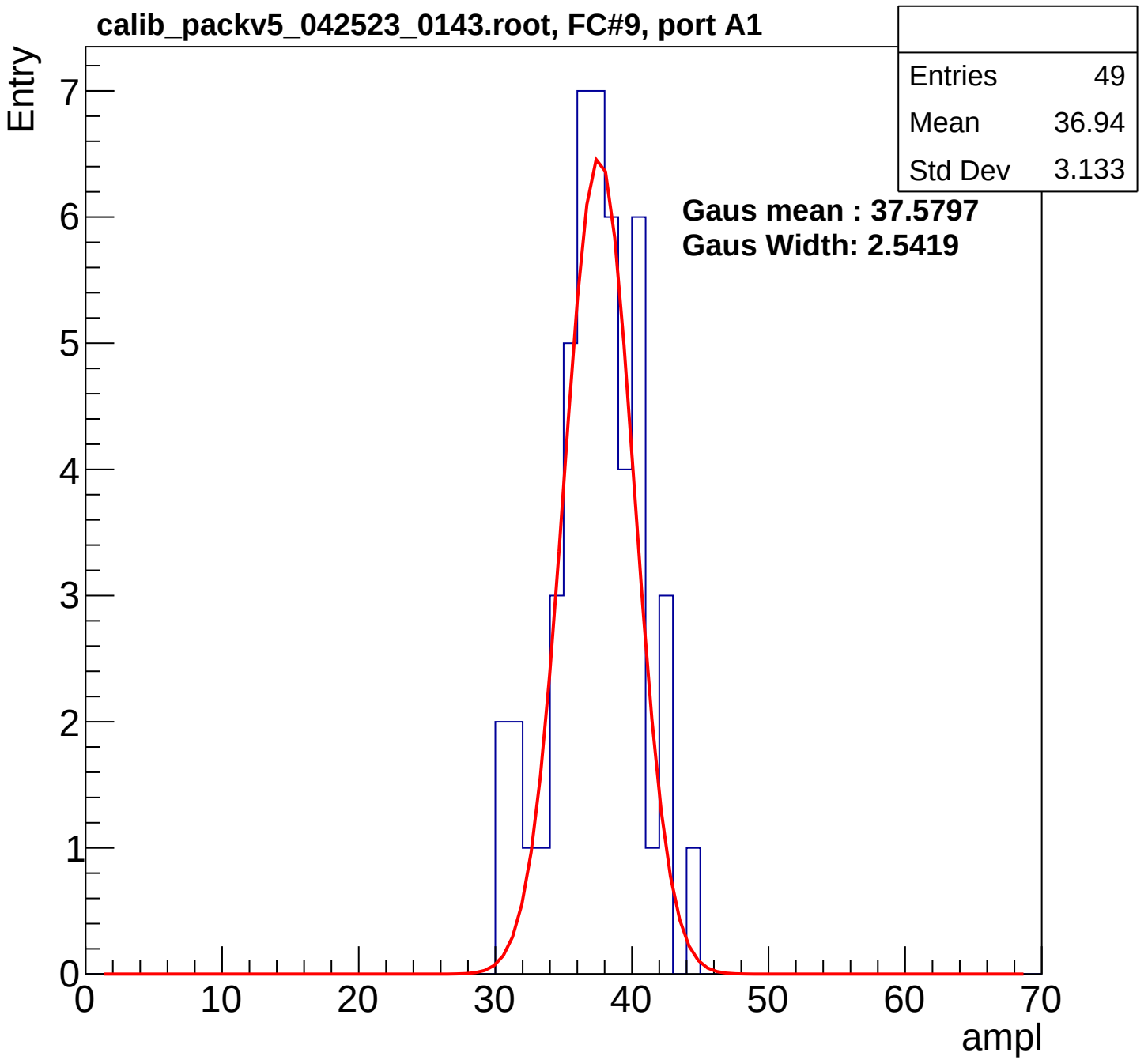
B0L001S, U12-ch96, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 49
Mean 36.94
Std Dev 3.133
Gaus mean : 37.5797
Gaus Width: 2.5419
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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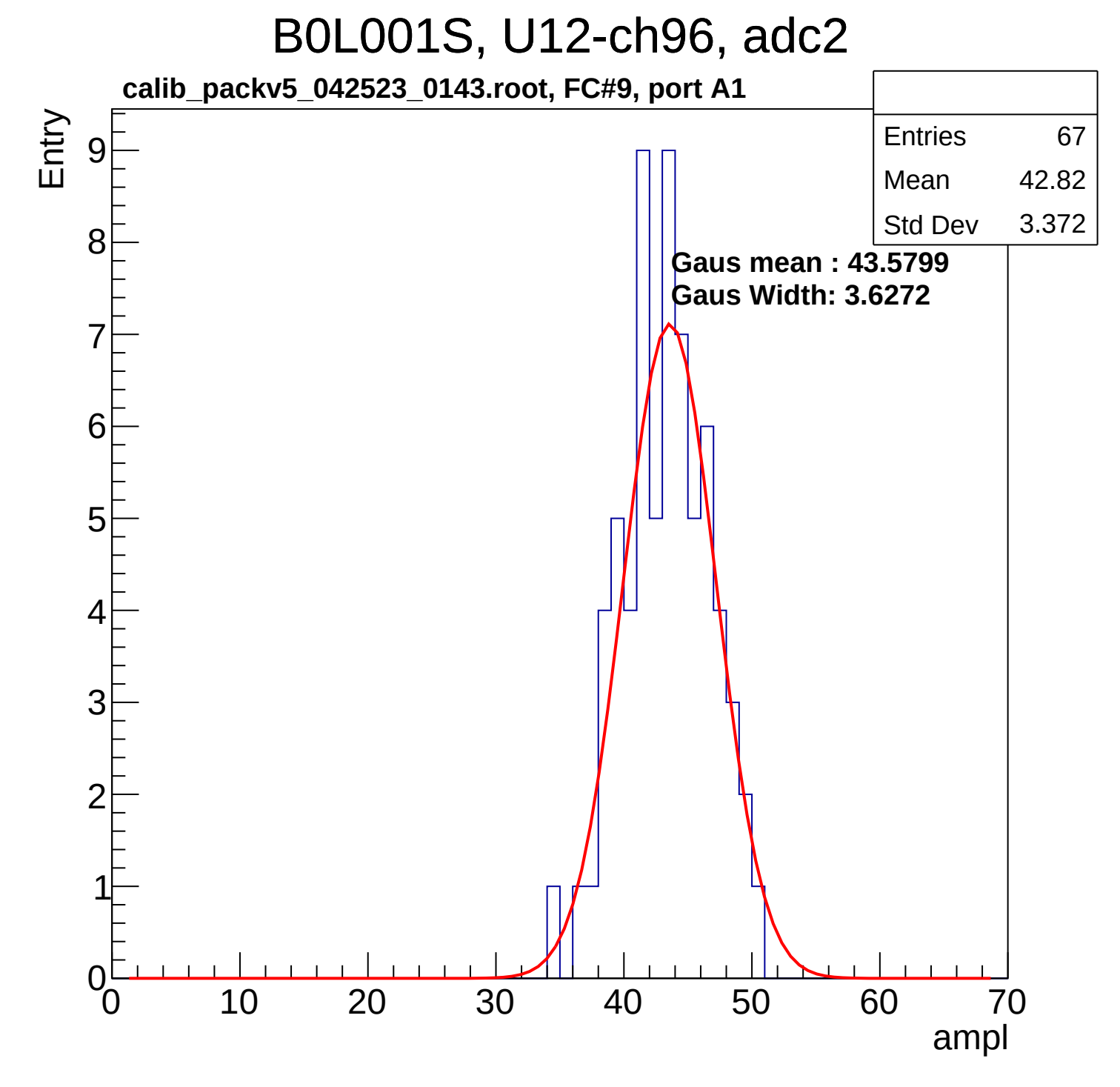
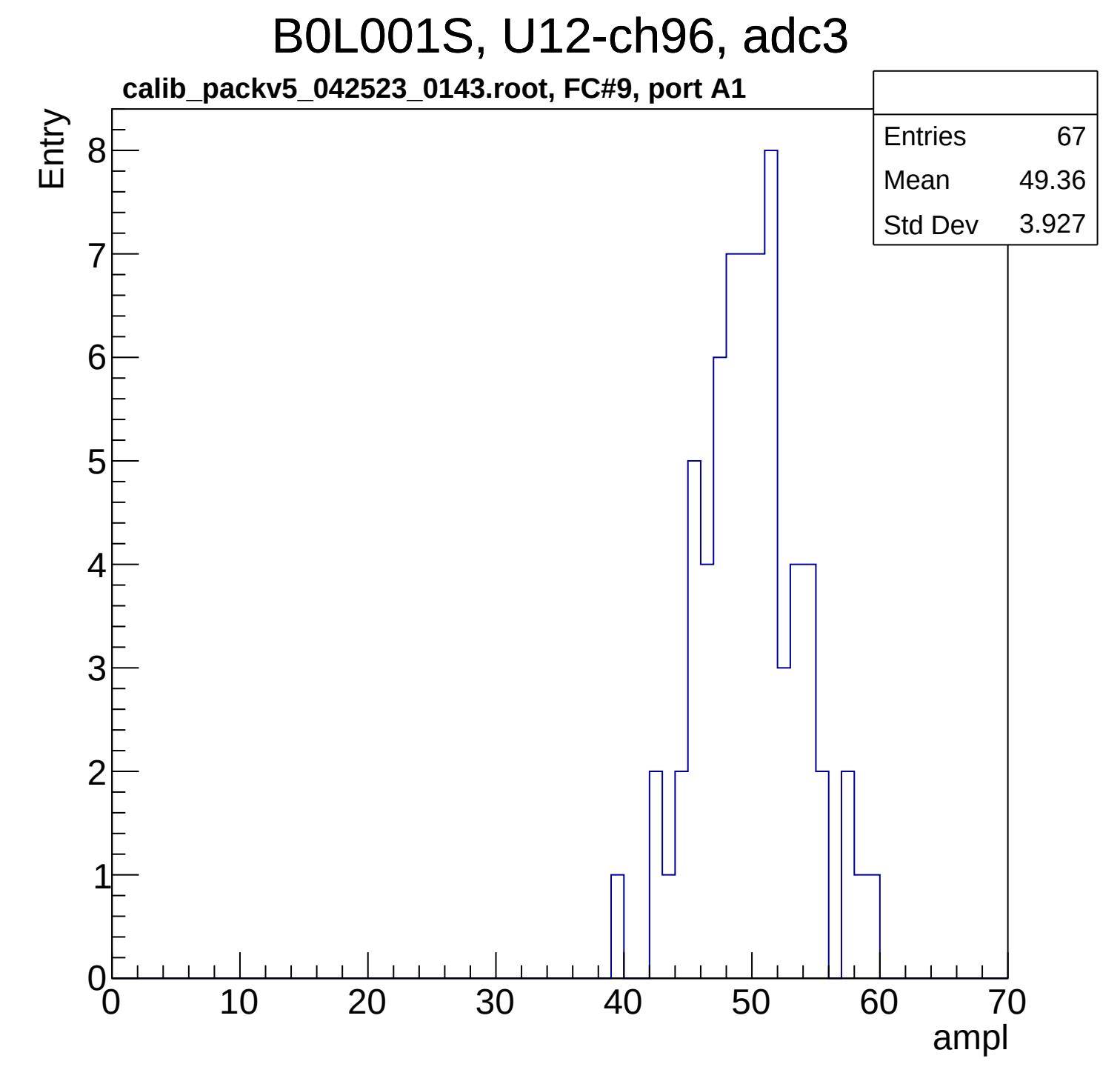

B0L001S, U12-ch96, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 67
Mean 42.82
Std Dev 3.372
Gaus mean : 43.5799
Gaus Width: 3.6272
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch96, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 67
Mean 49.36
Std Dev 3.927
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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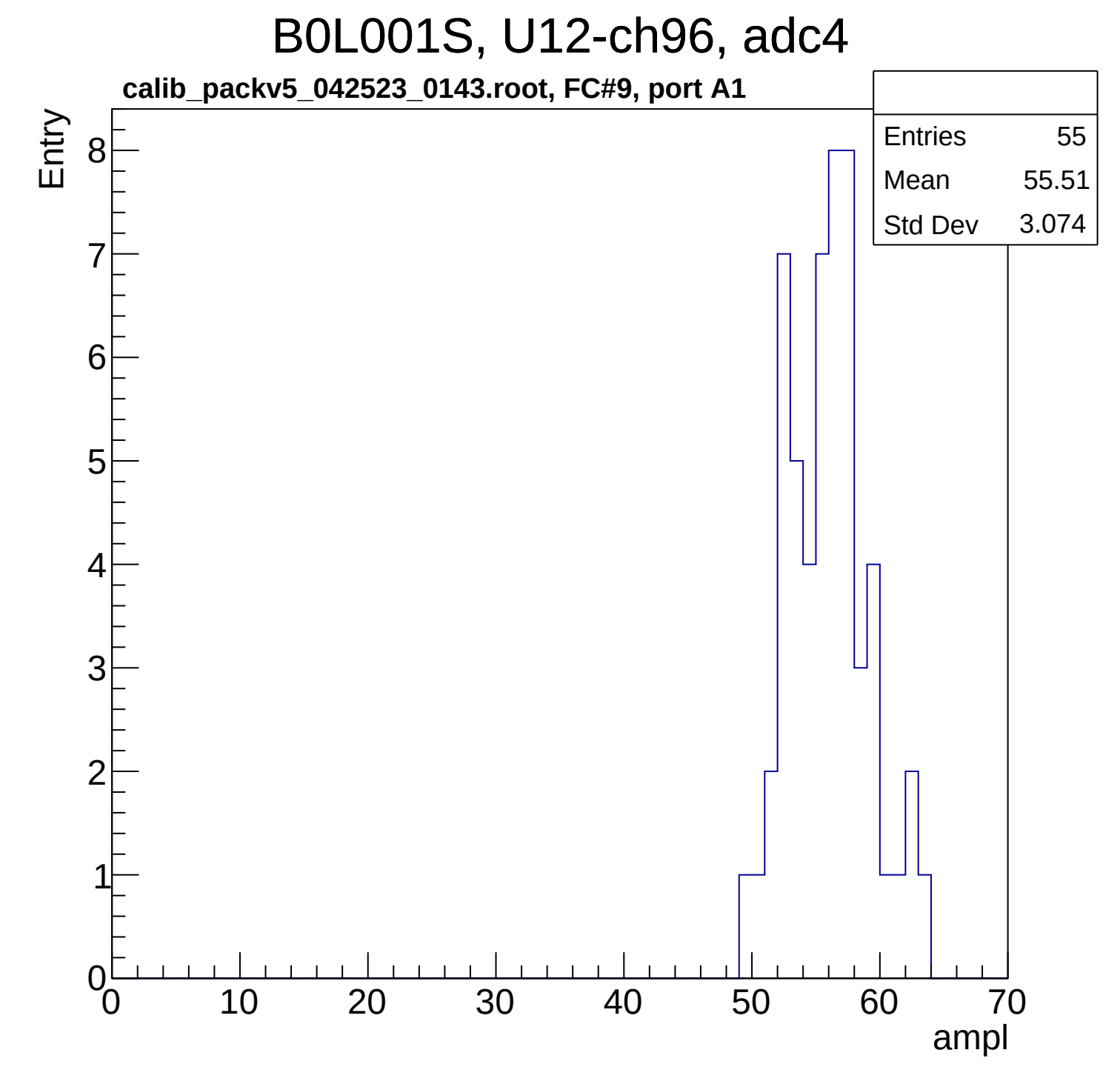
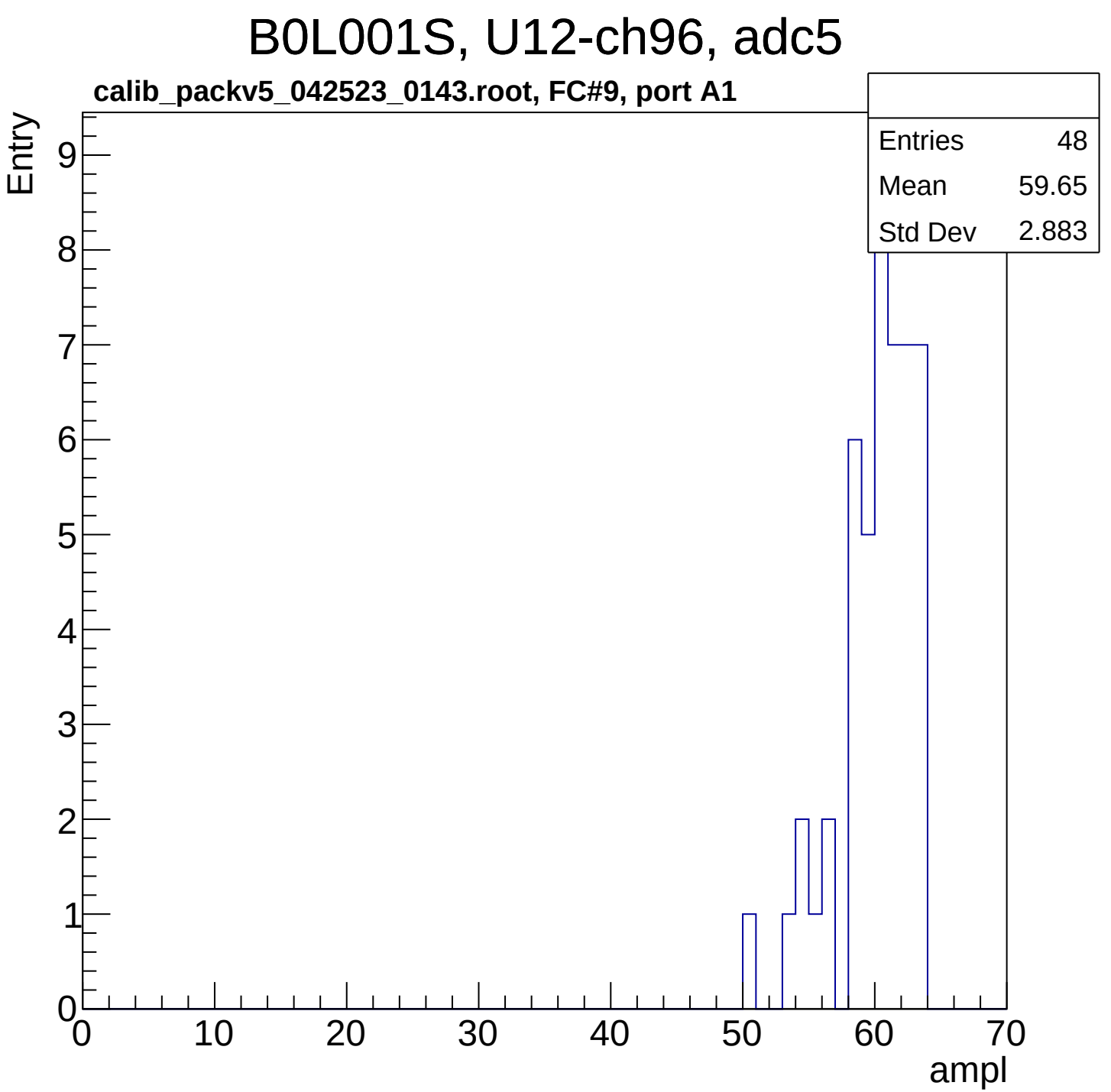
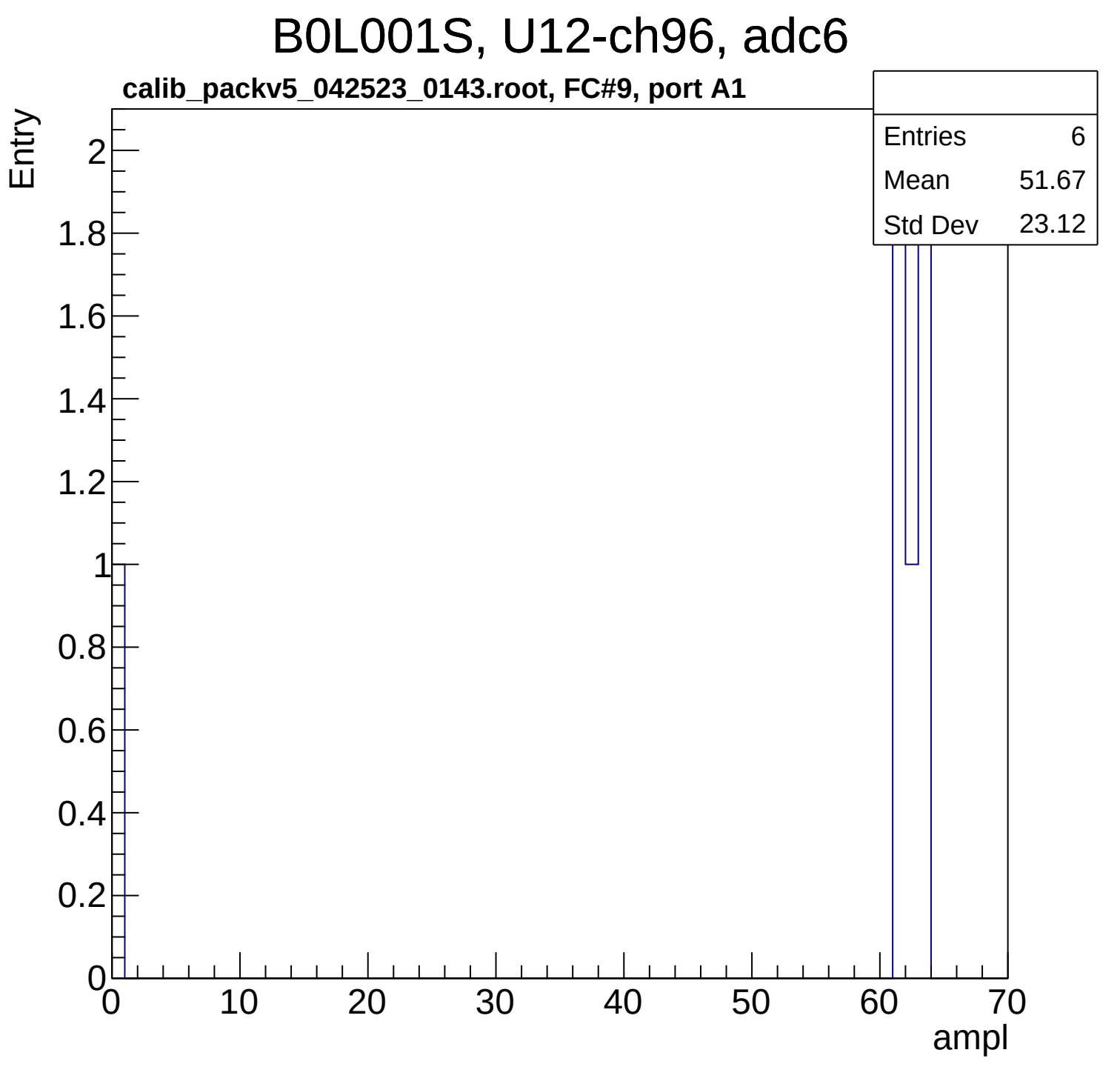

B0L001S, U12-ch96, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 55
Mean 55.51
Std Dev 3.074
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch96, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 48
Mean 59.65
Std Dev 2.883
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch96, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 6
Mean 51.67
Std Dev 23.12
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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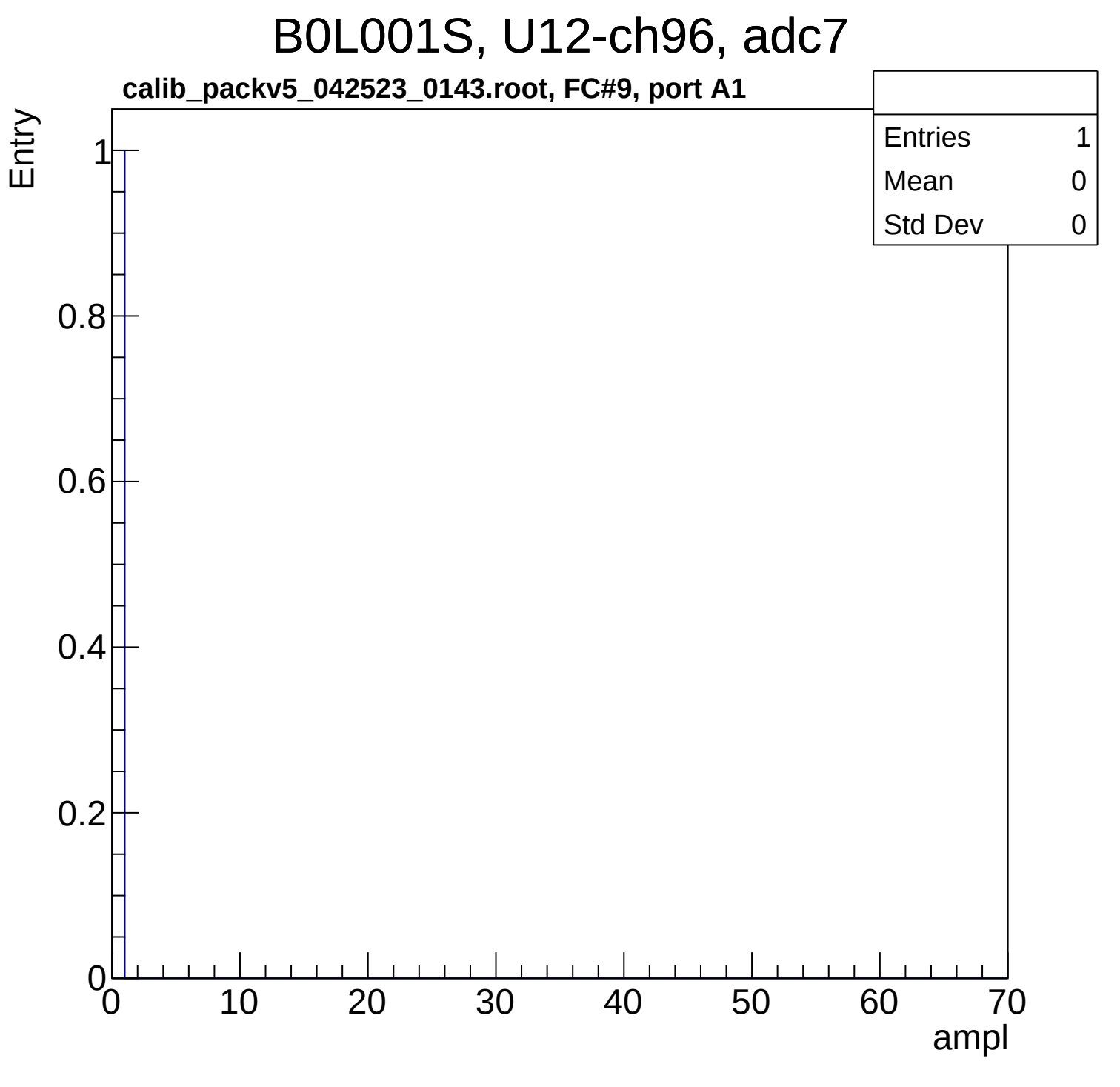
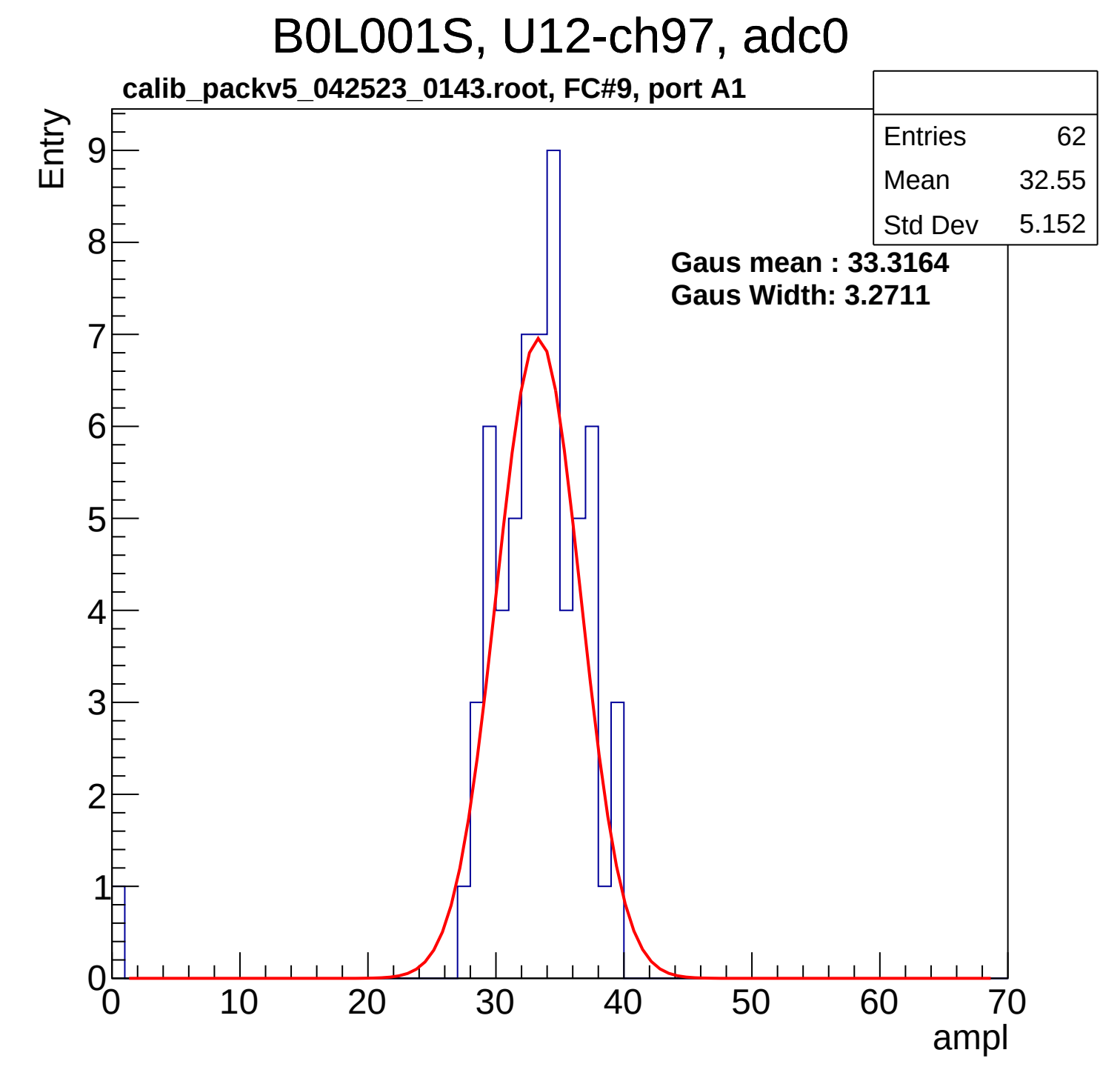
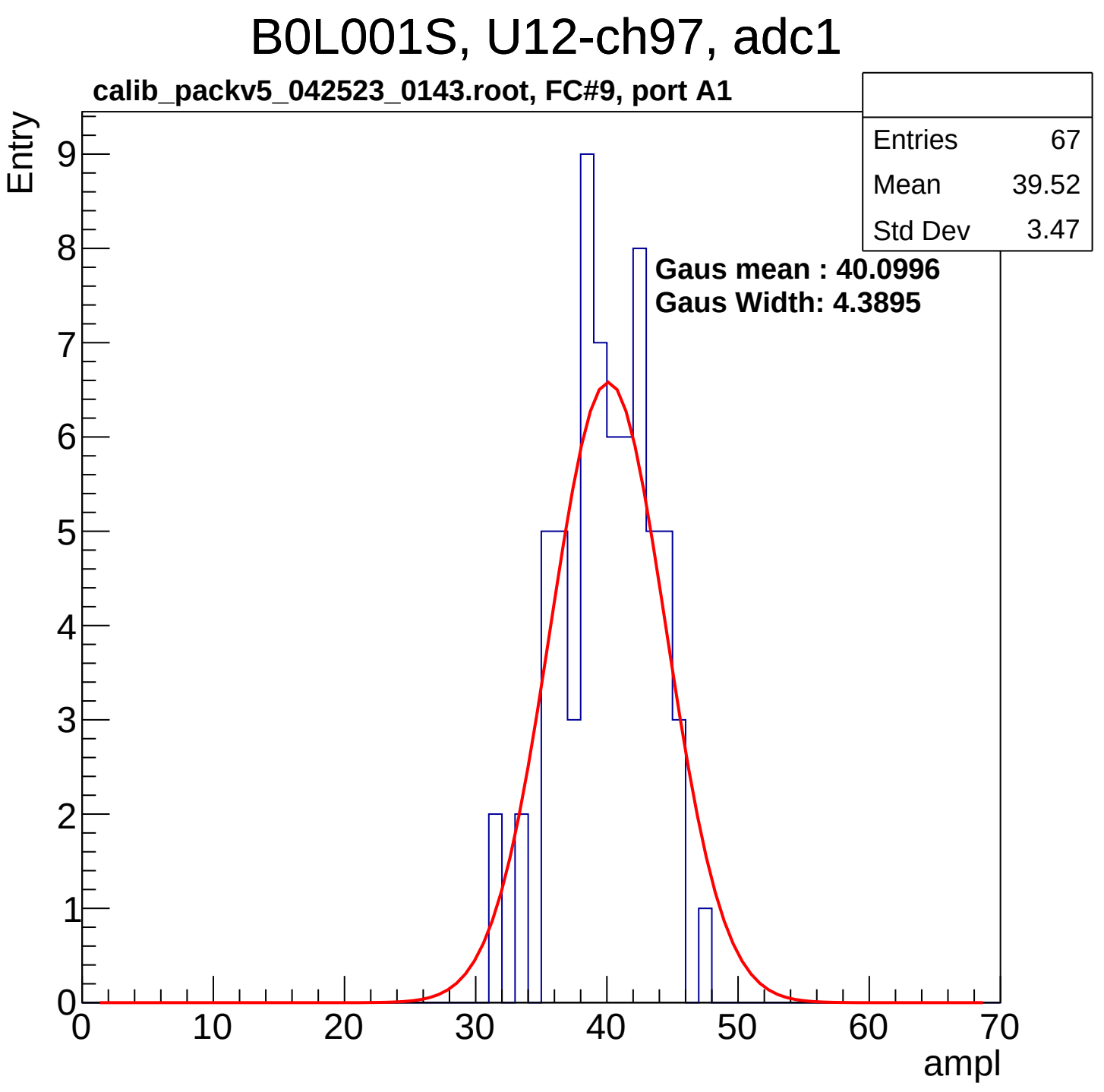
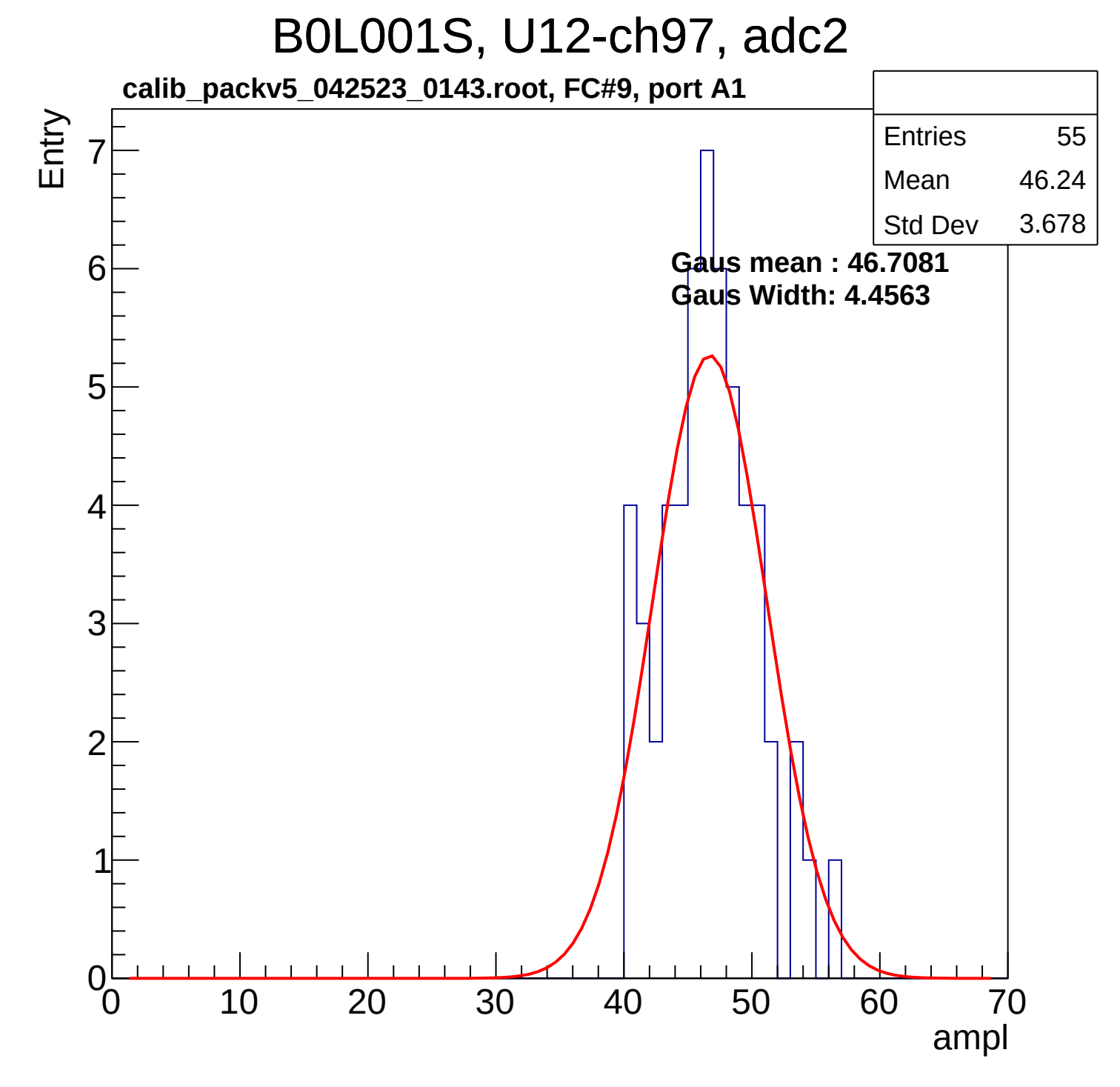
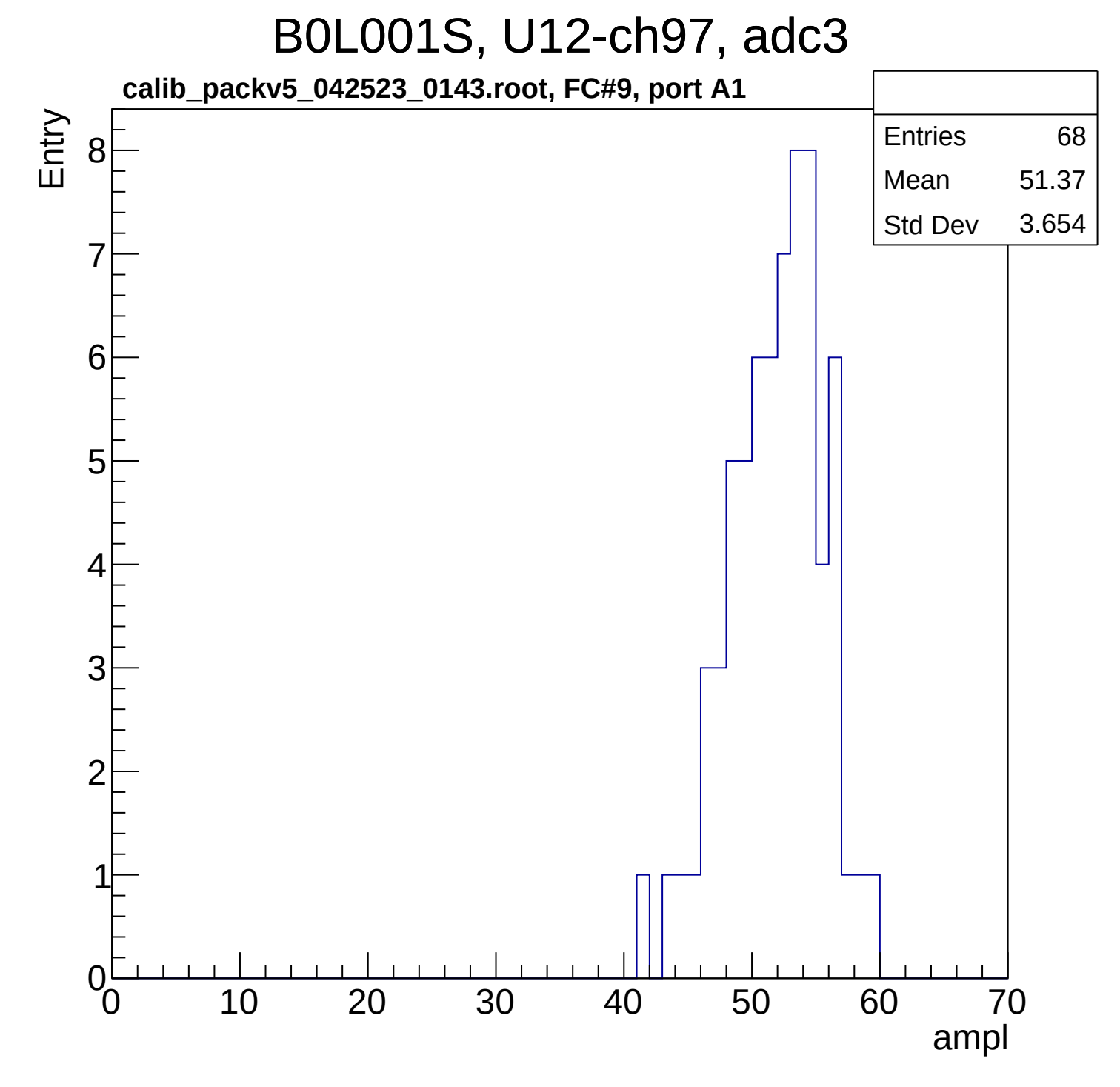
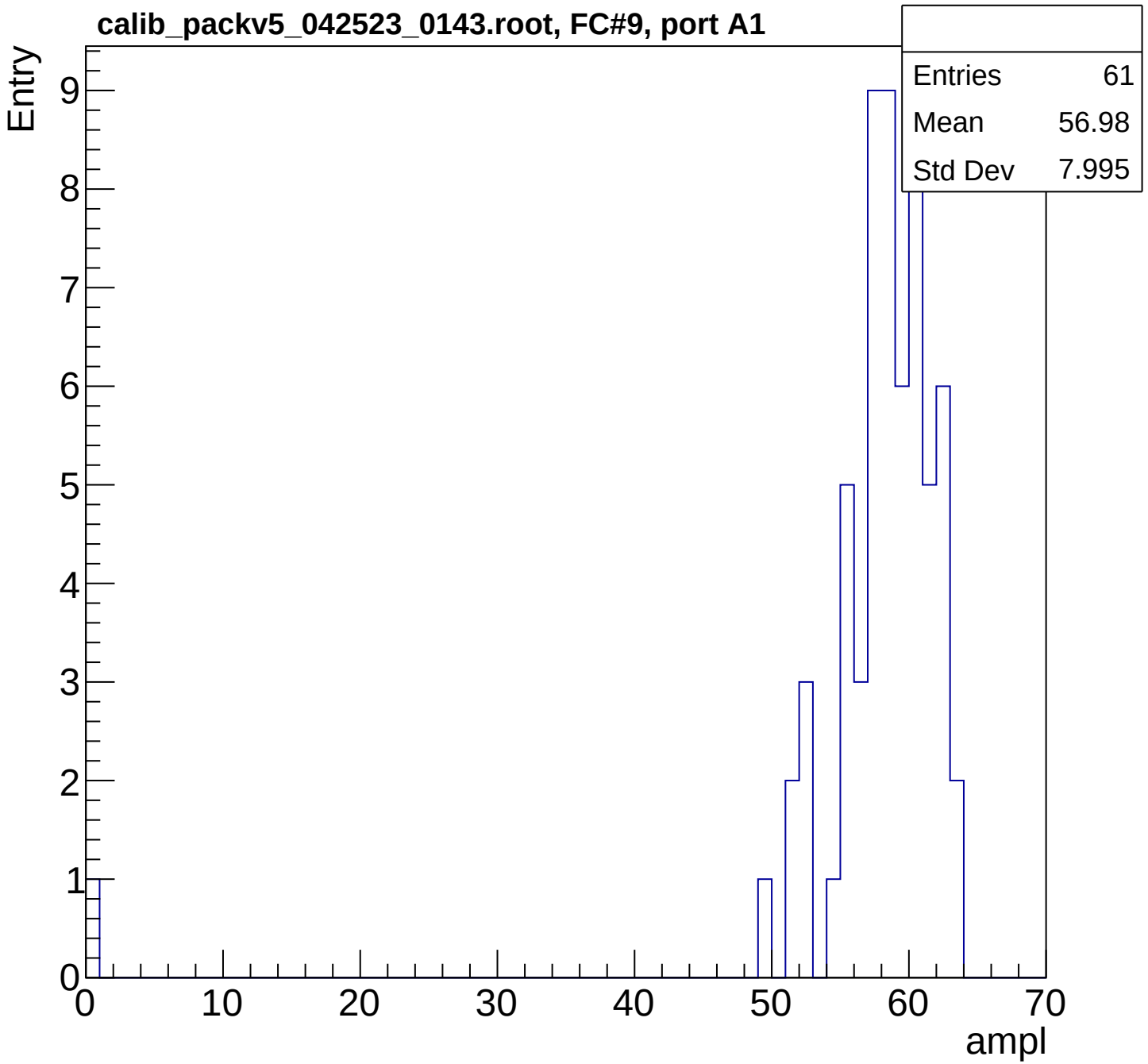

B0L001S, U12-ch96, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

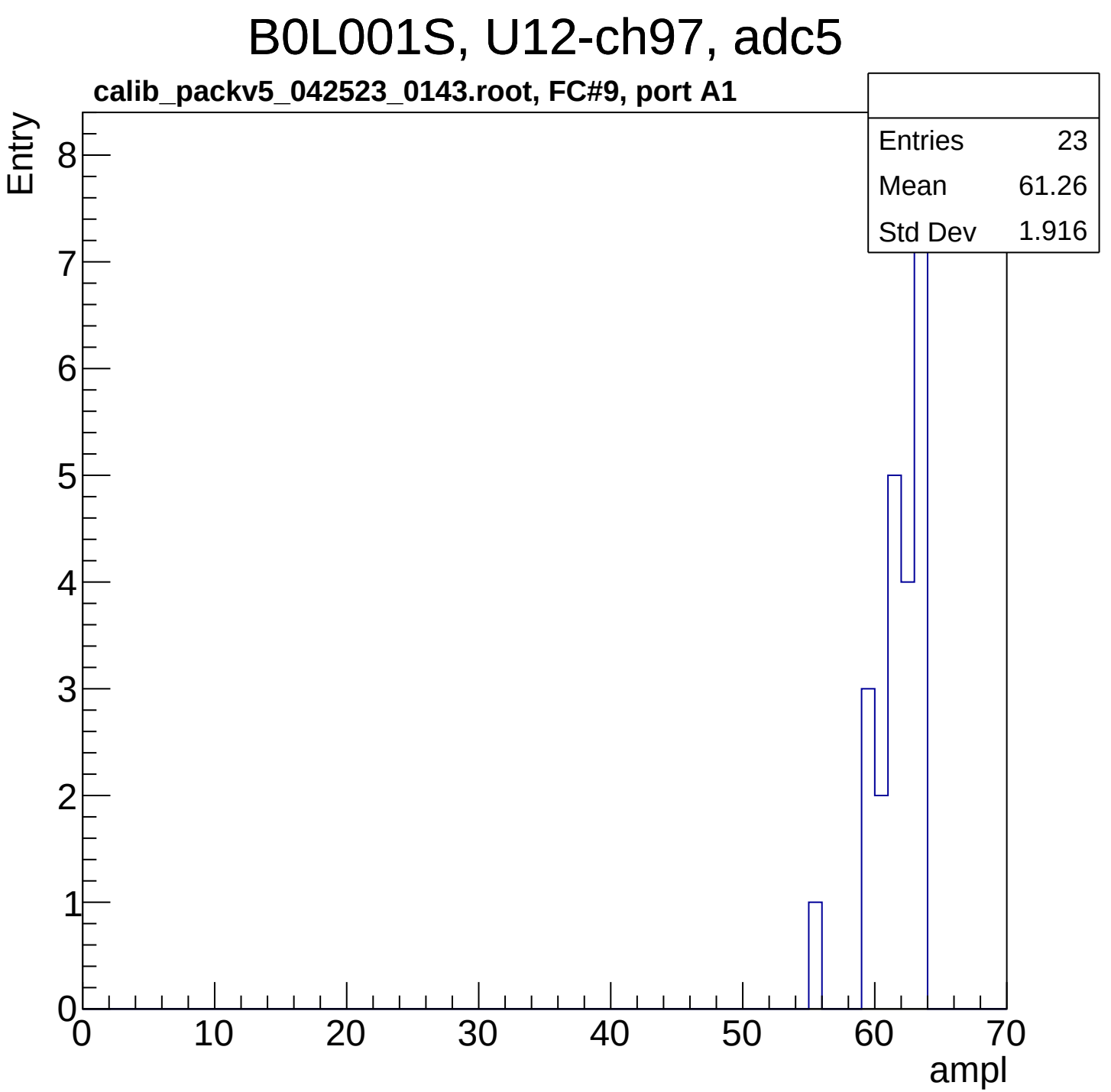

B0L001S, U12-ch97, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 62
Mean 32.55
Std Dev 5.152
Gaus mean : 33.3164
Gaus Width: 3.2711
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

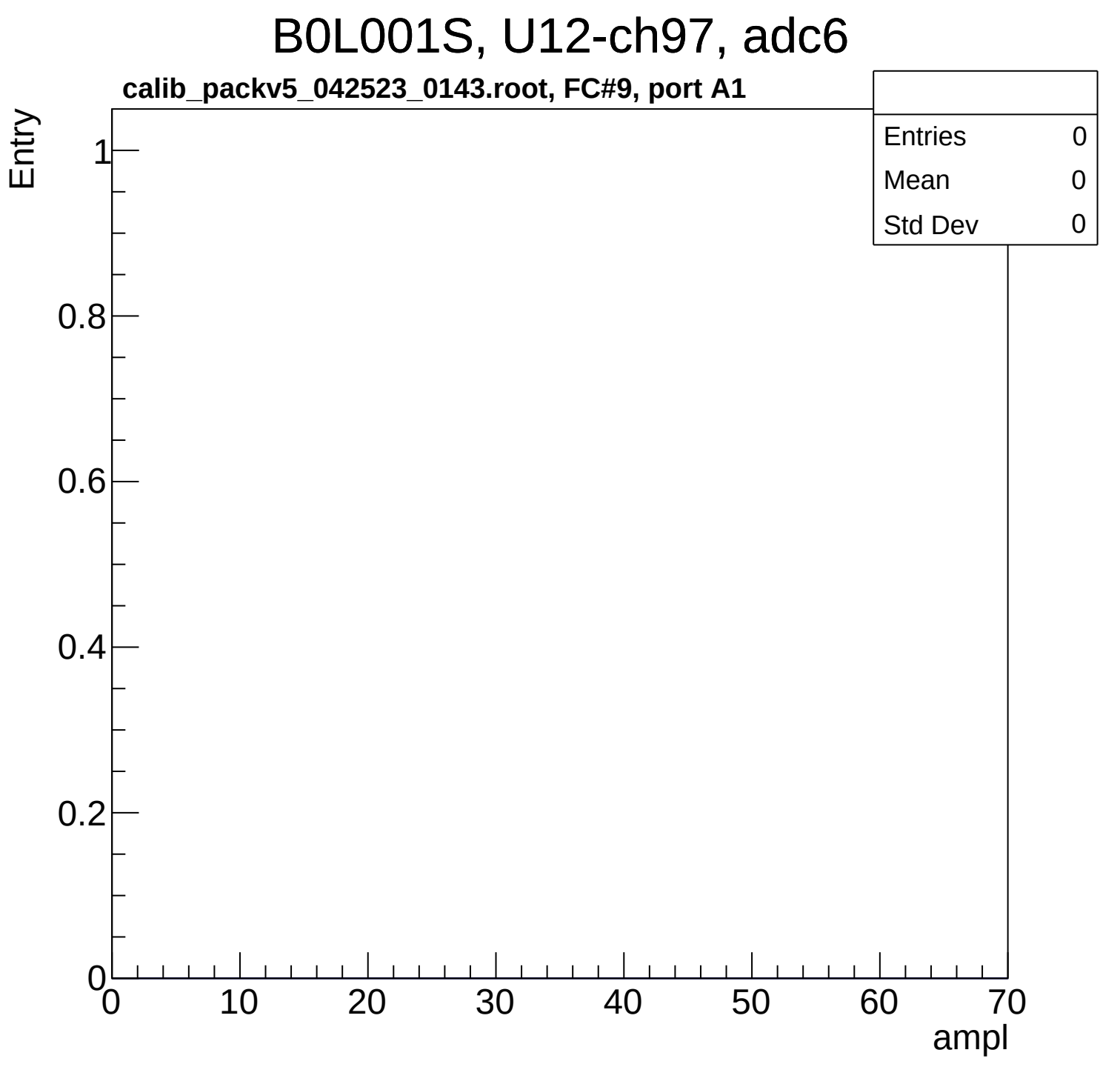

B0L001S, U12-ch97, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 67
Mean 39.52
Std Dev 3.47
Gaus mean : 40.0996
Gaus Width: 4.3895
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

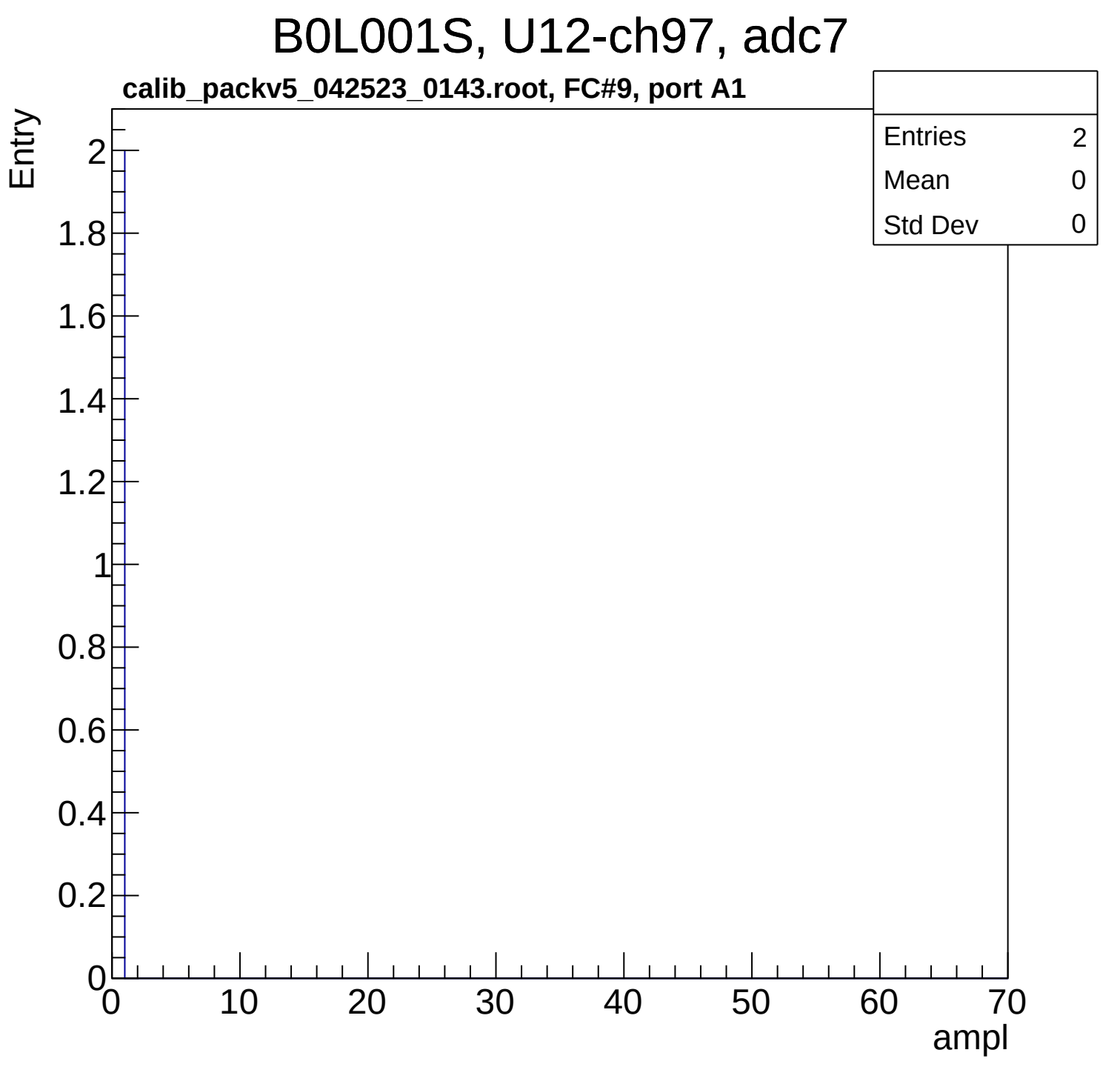

B0L001S, U12-ch97, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 55
Mean 46.24
Std Dev 3.678
Gaus mean : 46.7081
Gaus Width: 4.4563
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

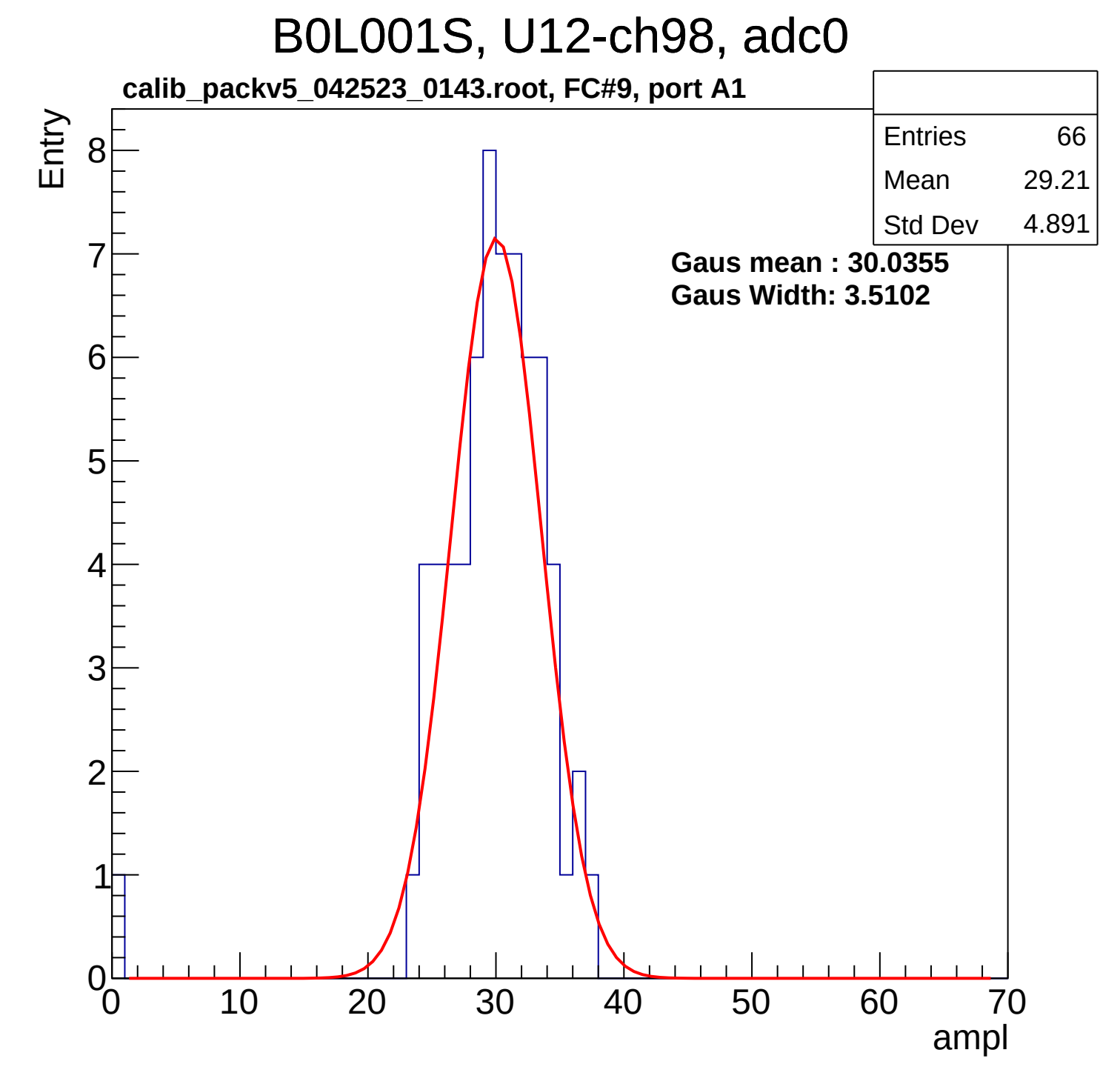

B0L001S, U12-ch97, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 68
Mean 51.37
Std Dev 3.654
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

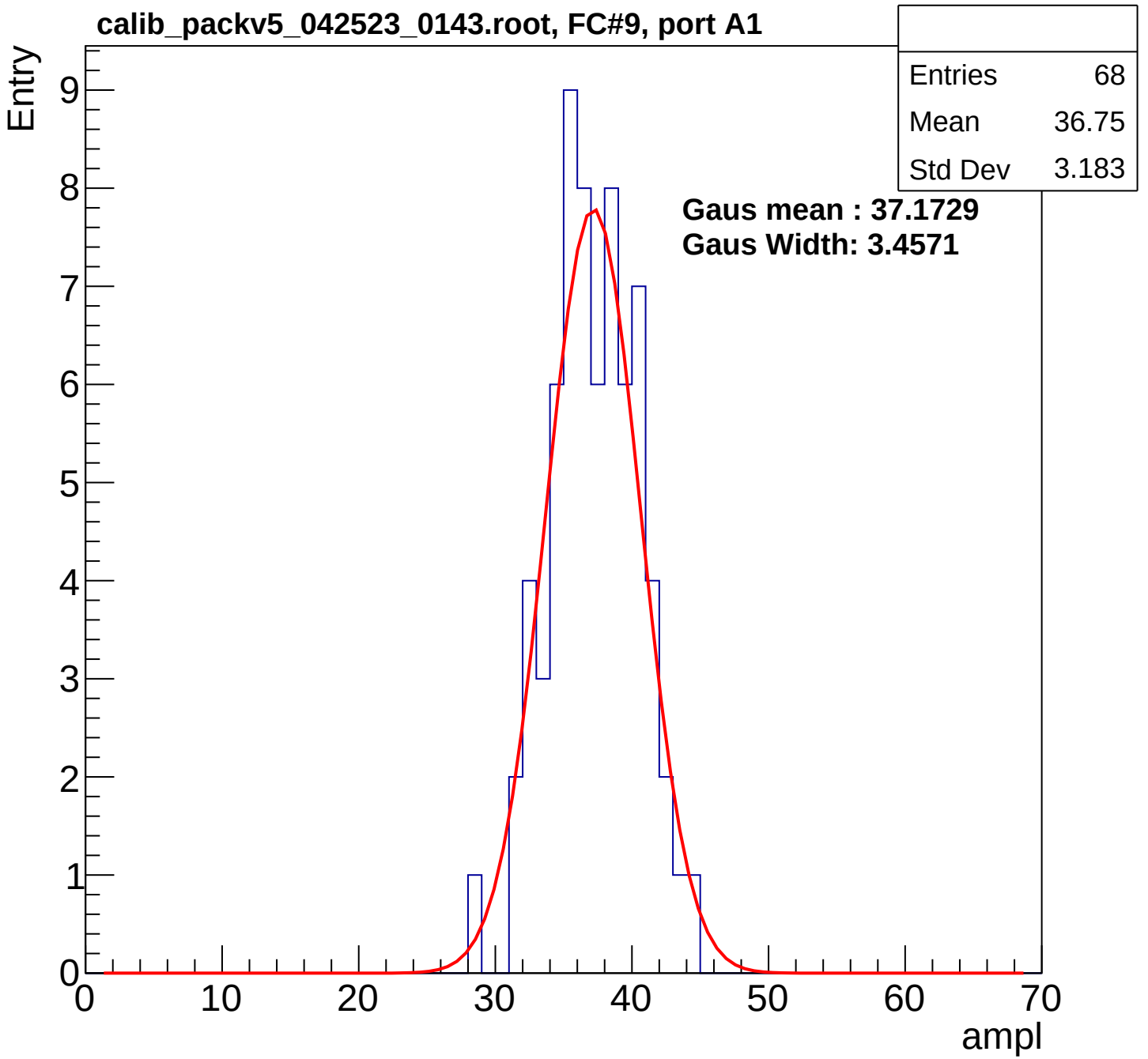

B0L001S, U12-ch97, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 61
Mean 56.98
Std Dev 7.995
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

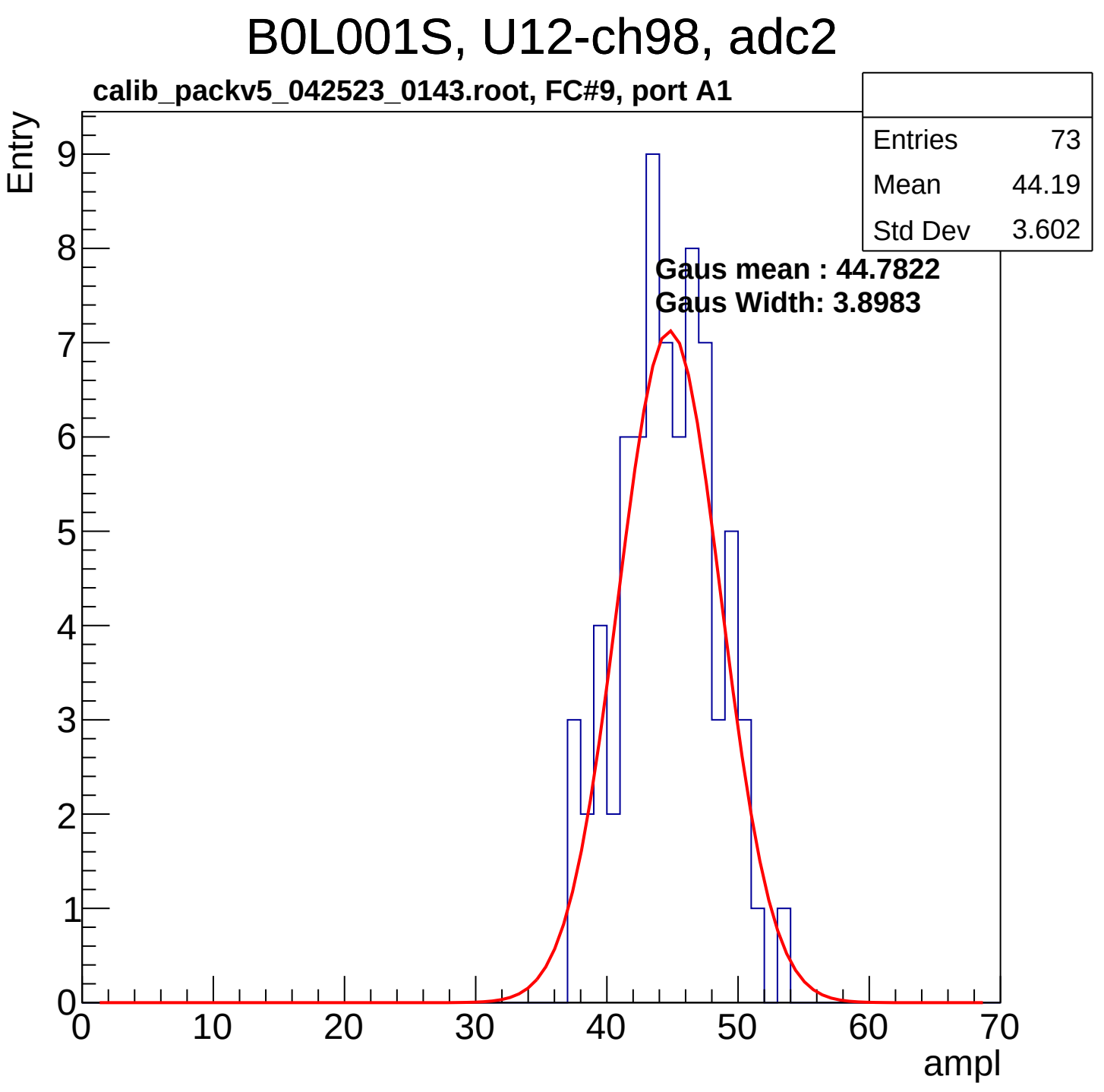

B0L001S, U12-ch97, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 23
Mean 61.26
Std Dev 1.916
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

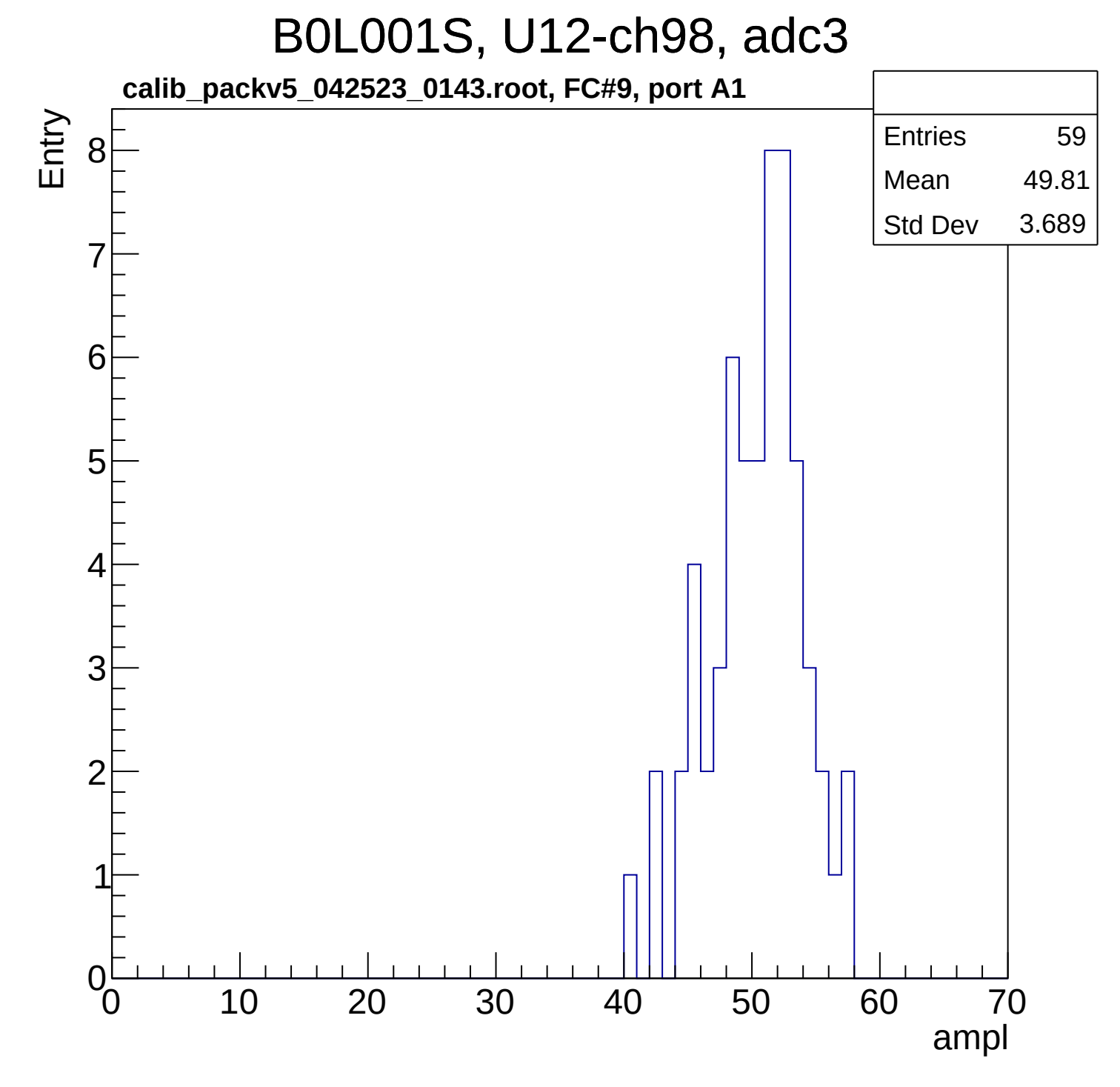

B0L001S, U12-ch97, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

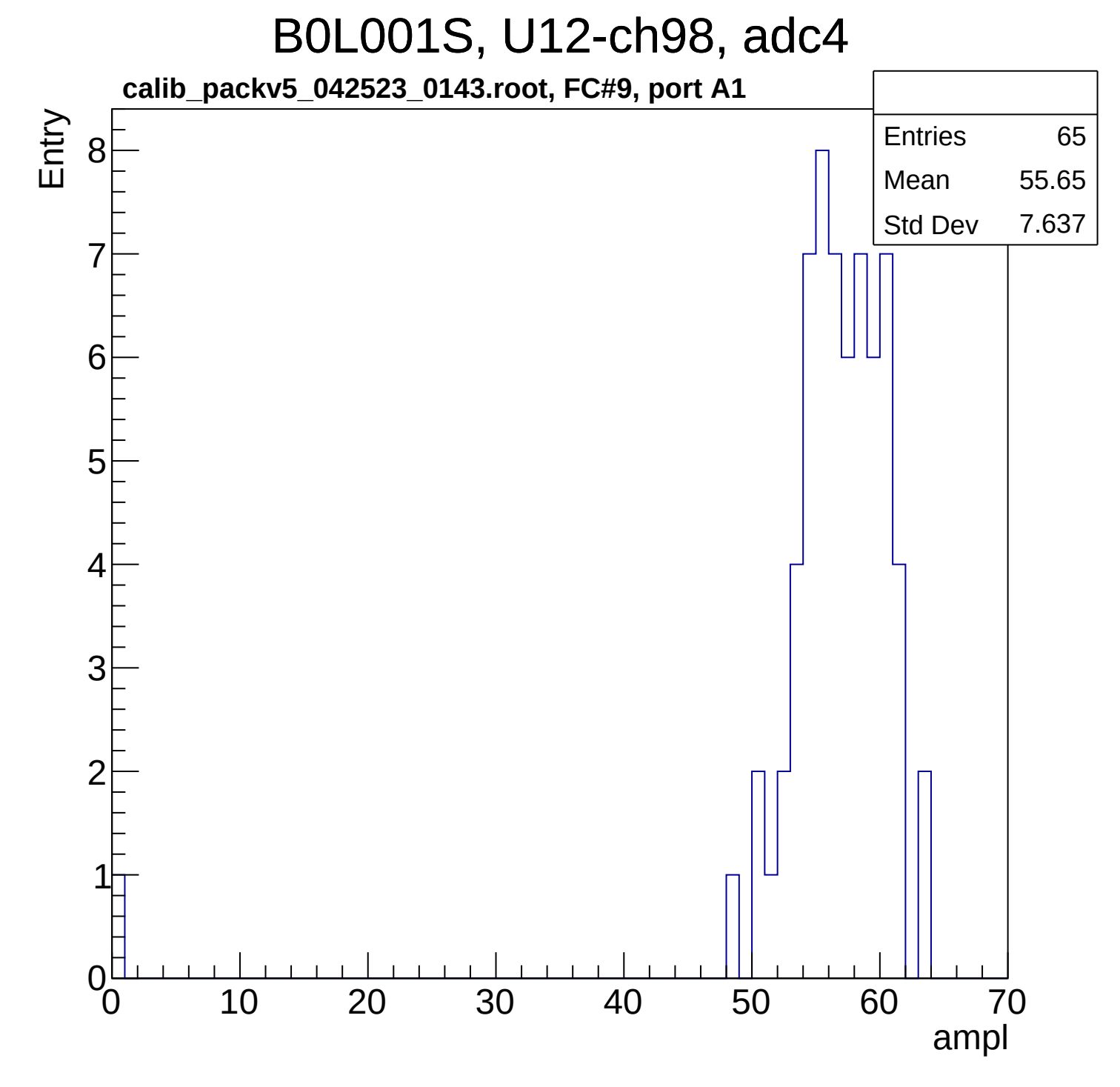

B0L001S, U12-ch97, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

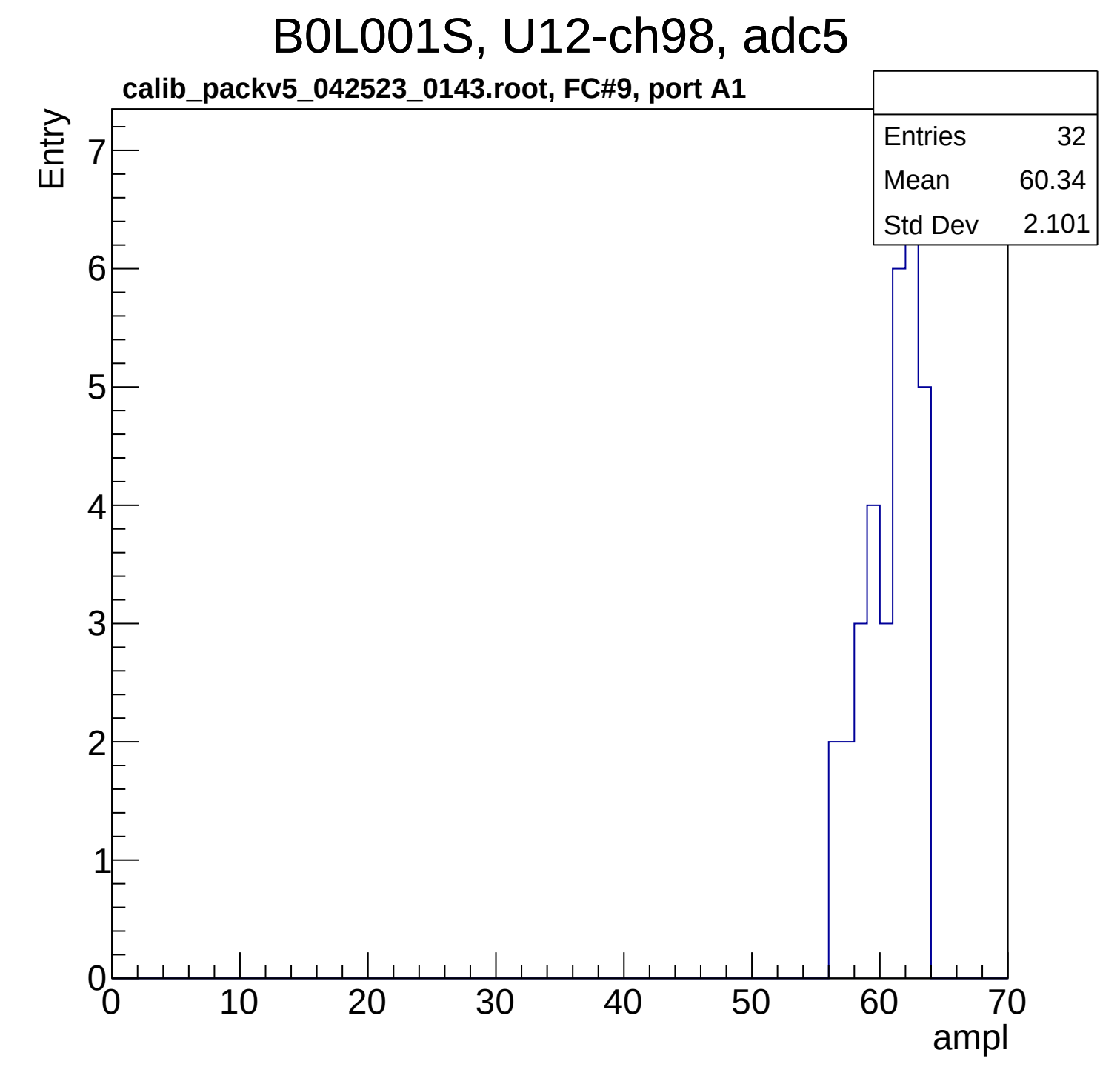

B0L001S, U12-ch98, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 66
Mean 29.21
Std Dev 4.891
Gaus mean : 30.0355
Gaus Width: 3.5102
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

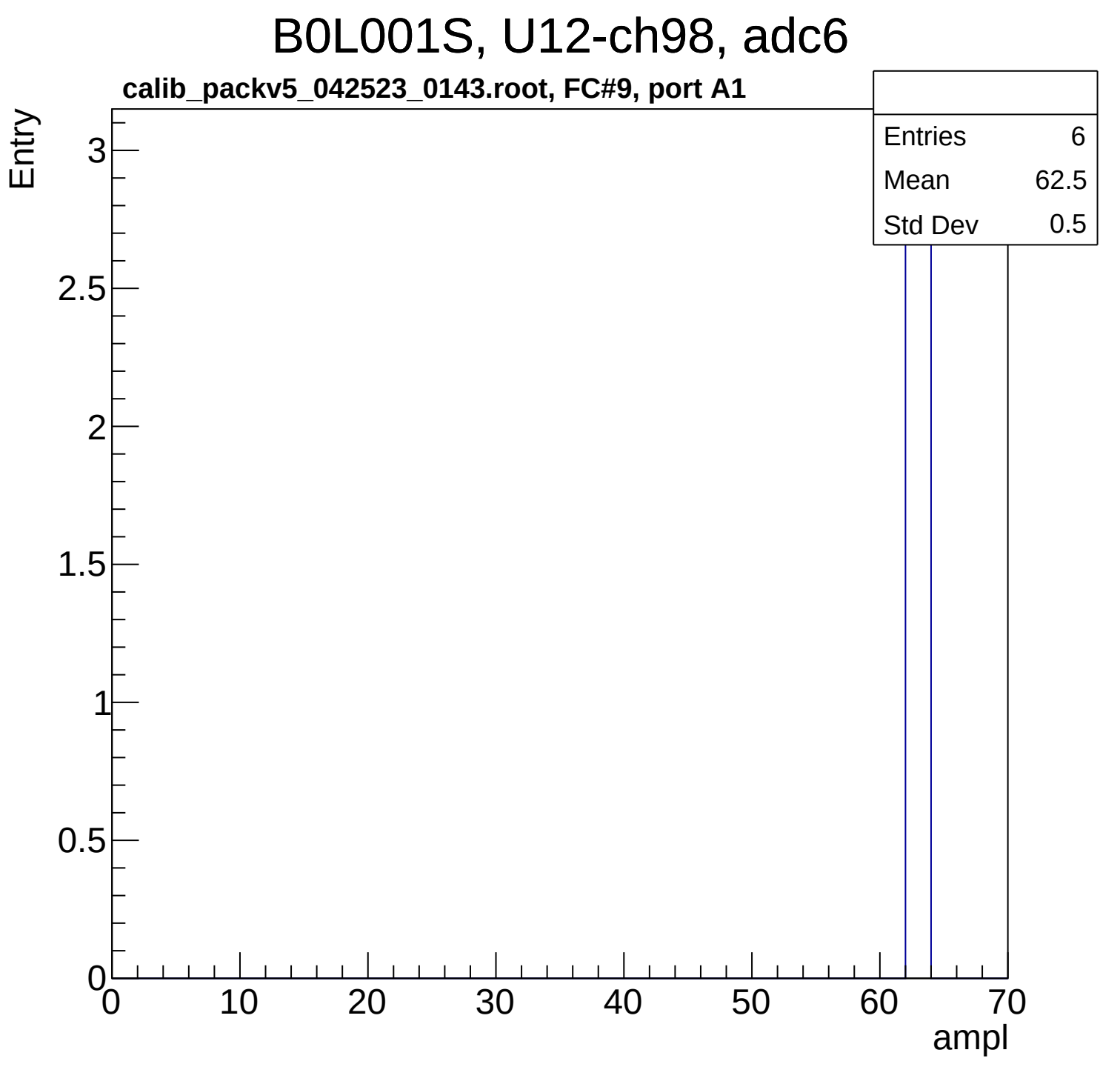

B0L001S, U12-ch98, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 68
Mean 36.75
Std Dev 3.183
Gaus mean : 37.1729
Gaus Width: 3.4571
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

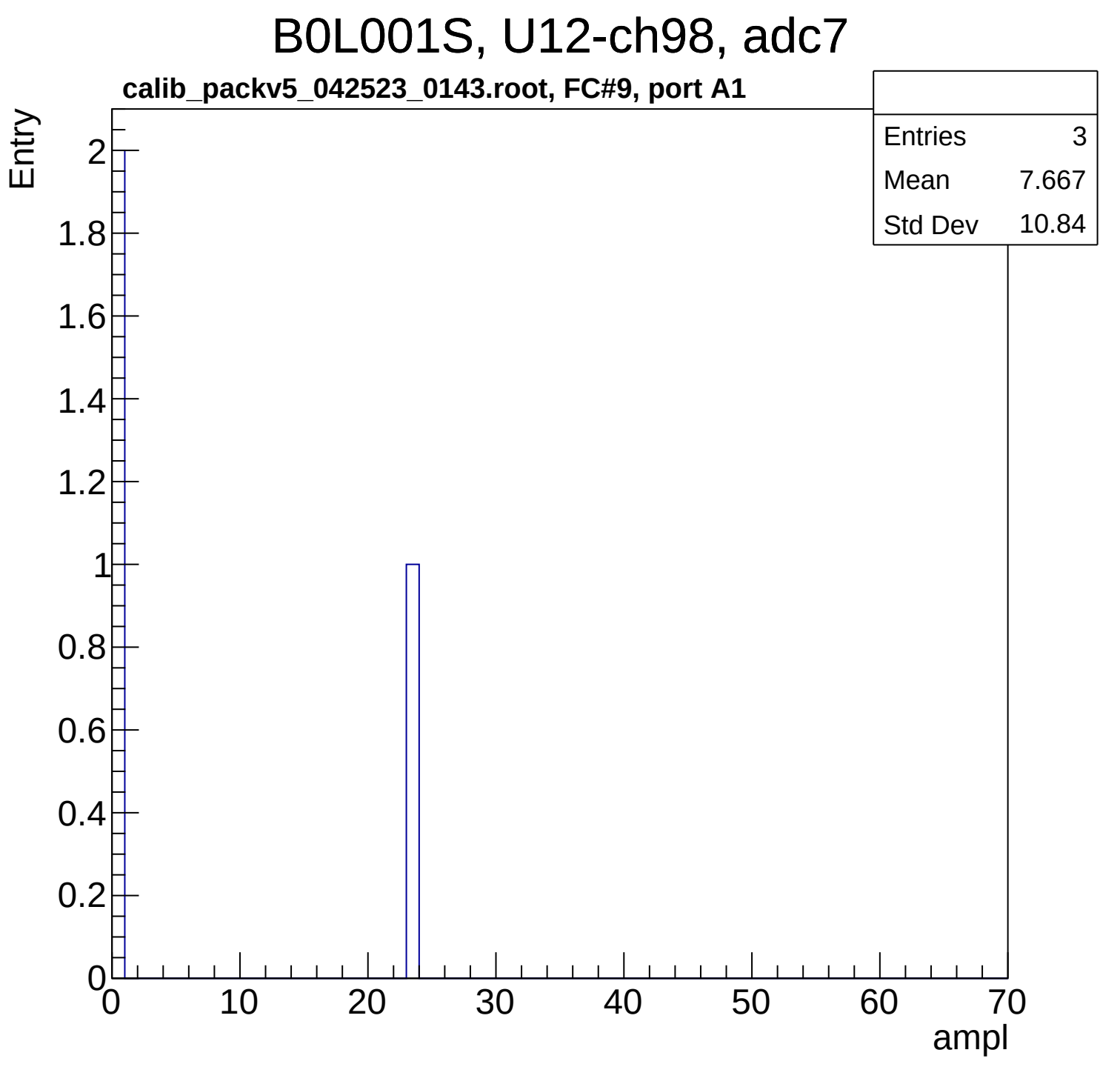

B0L001S, U12-ch98, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 73
Mean 44.19
Std Dev 3.602
Gaus mean : 44.7822
Gaus Width: 3.8983
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch98, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 59
Mean 49.81
Std Dev 3.689
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch98, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 65
Mean 55.65
Std Dev 7.637
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch98, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 32
Mean 60.34
Std Dev 2.101
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B0L001S, U12-ch98, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 6
Mean 62.5
Std Dev 0.5
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B0L001S, U12-ch98, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 3
Mean 7.667
Std Dev 10.84
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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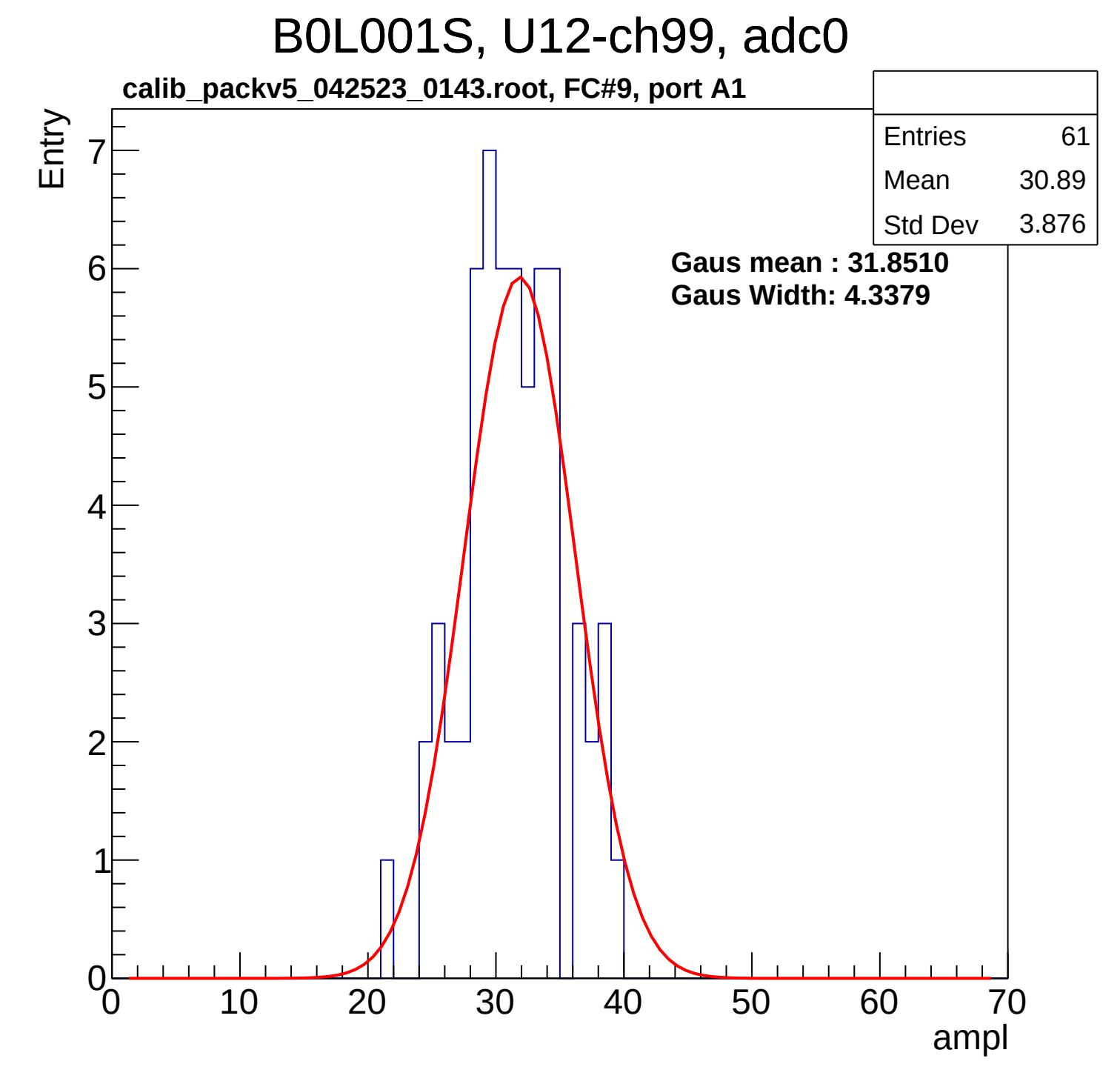
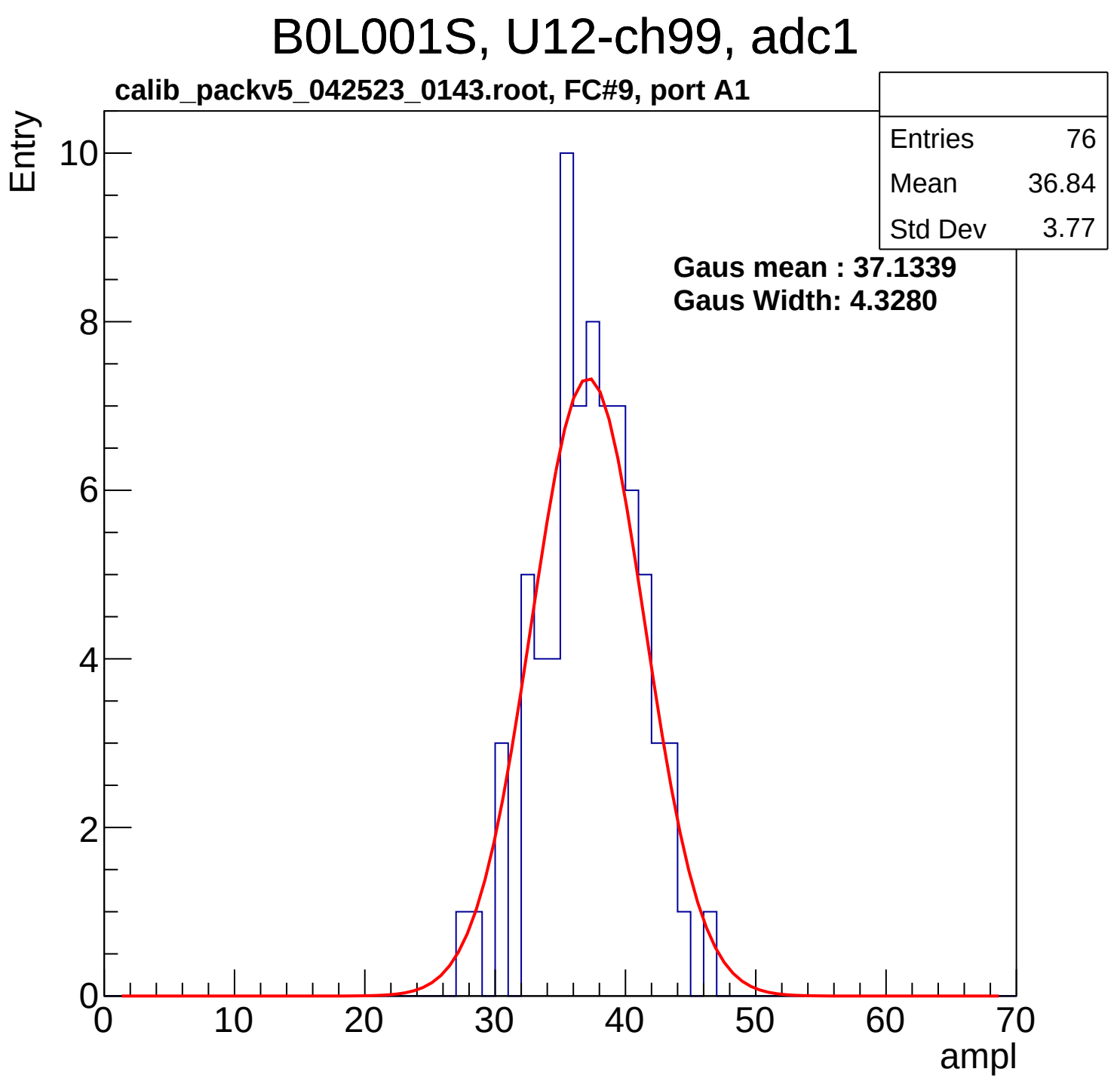
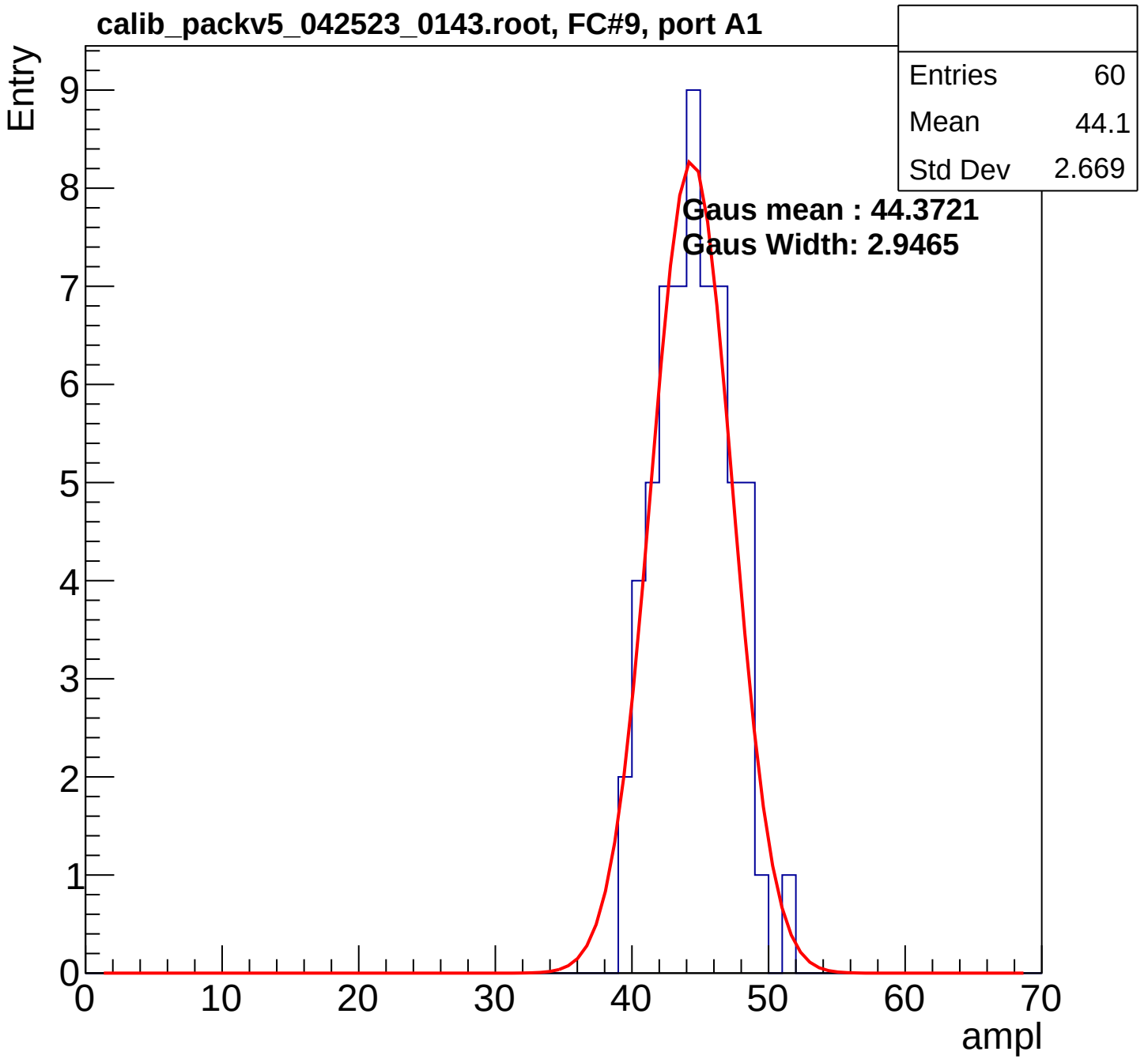

B0L001S, U12-ch99, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 61
Mean 30.89
Std Dev 3.876
Gaus mean : 31.8510
Gaus Width: 4.3379
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B0L001S, U12-ch99, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 76
Mean 36.84
Std Dev 3.77
Gaus mean : 37.1339
Gaus Width: 4.3280
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch99, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 60
Mean 44.1
Std Dev 2.669
Gaus mean : 44.3721
Gaus Width: 2.9465
Entry
ampl
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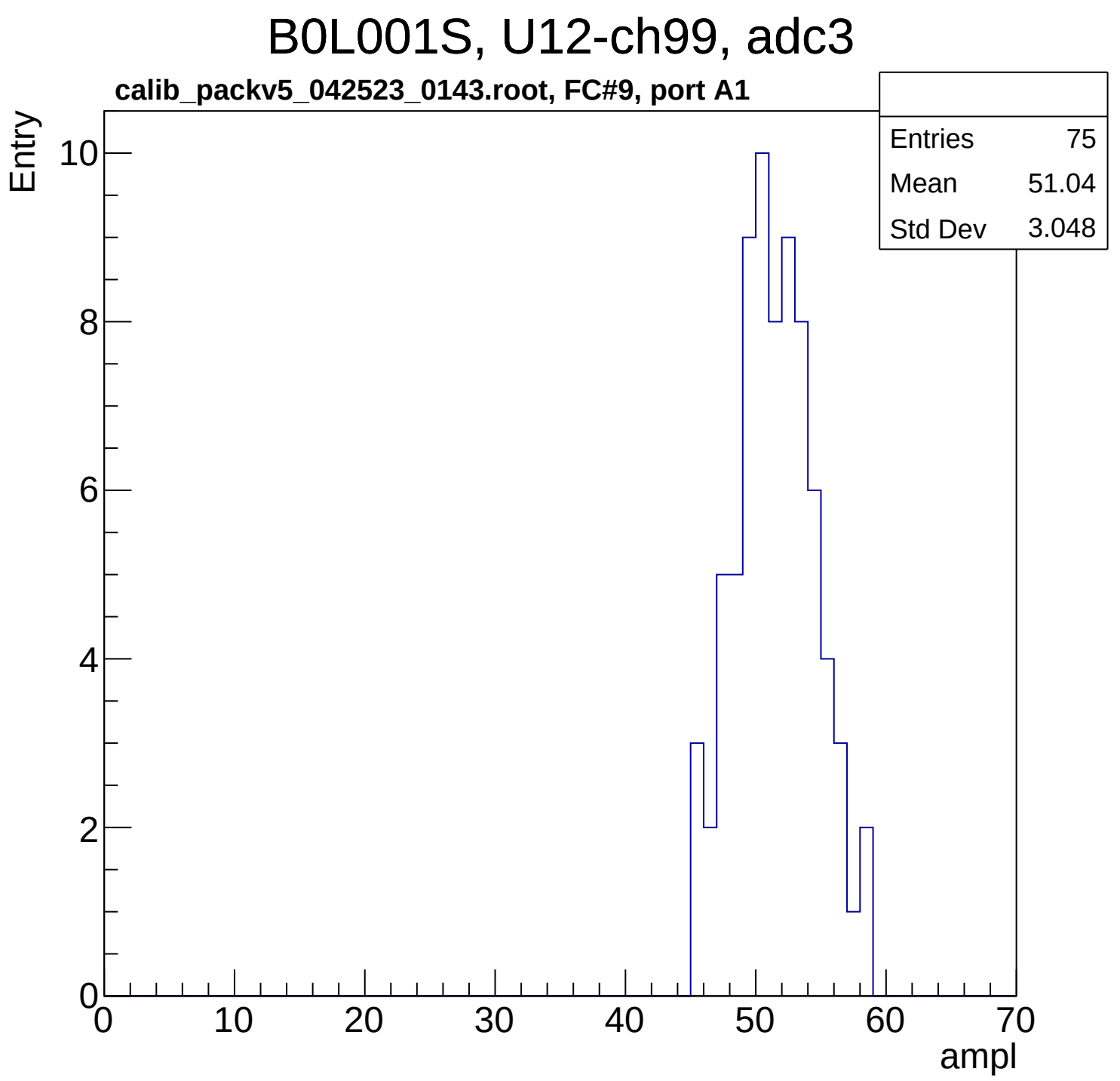
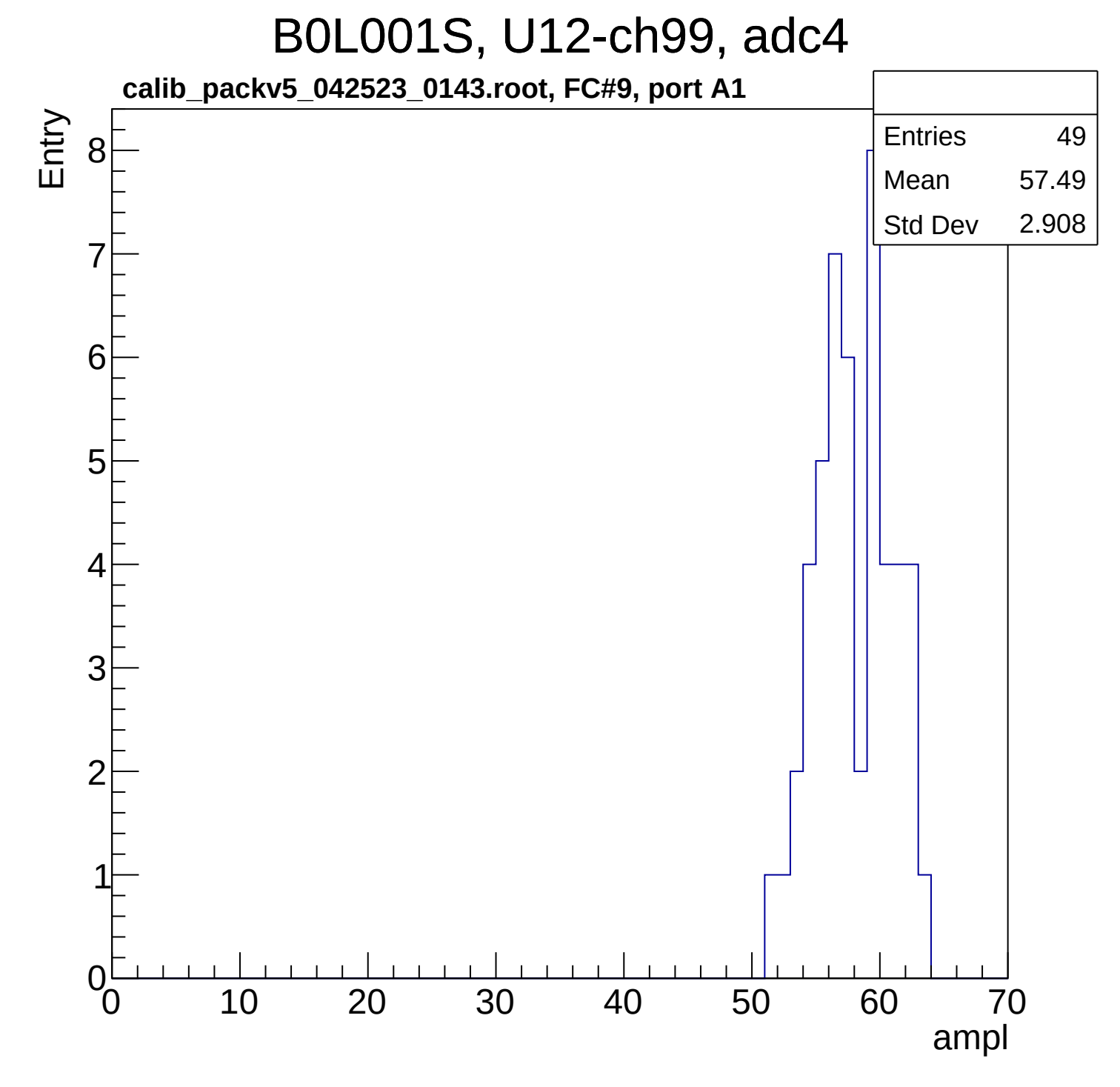
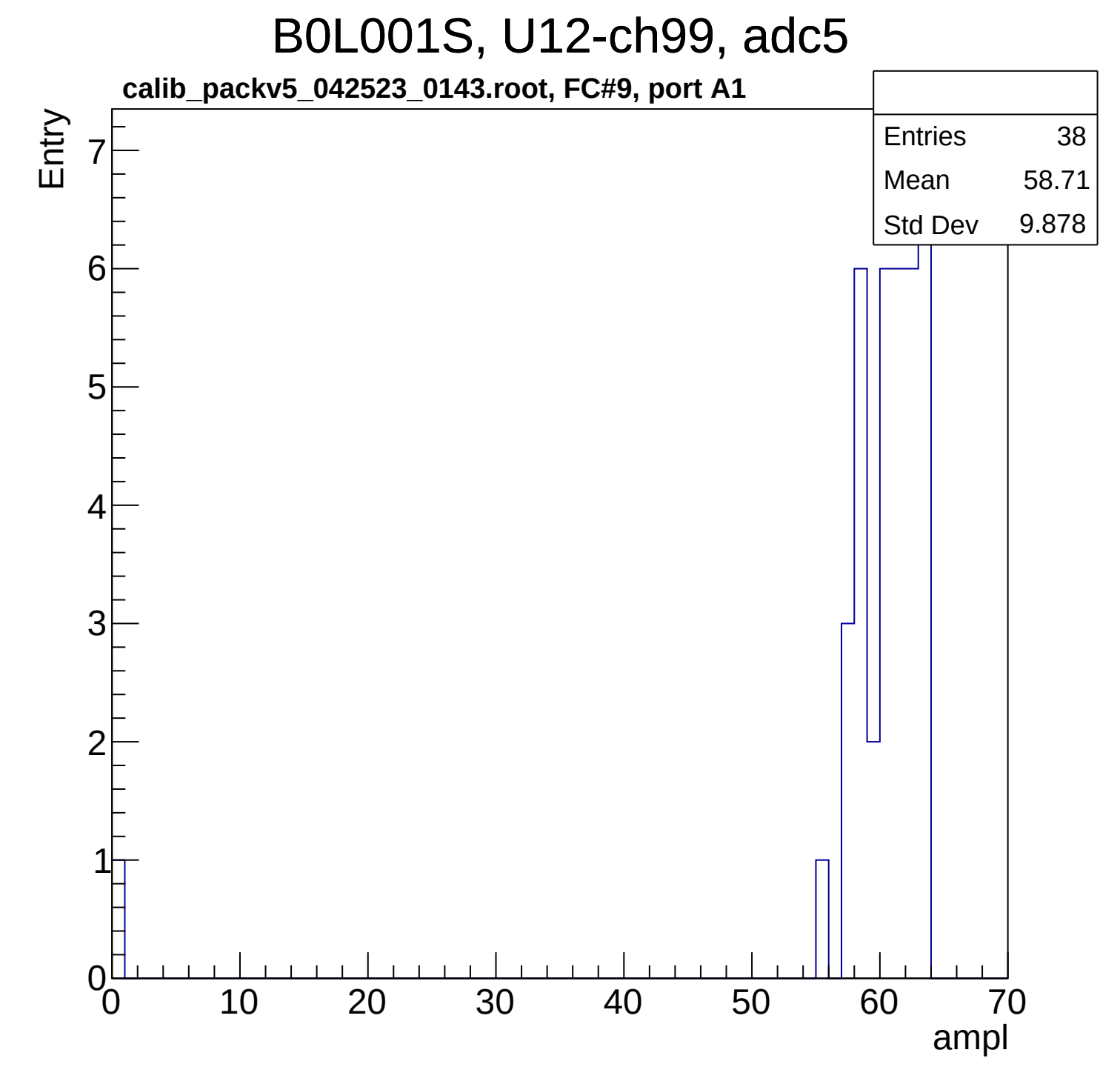
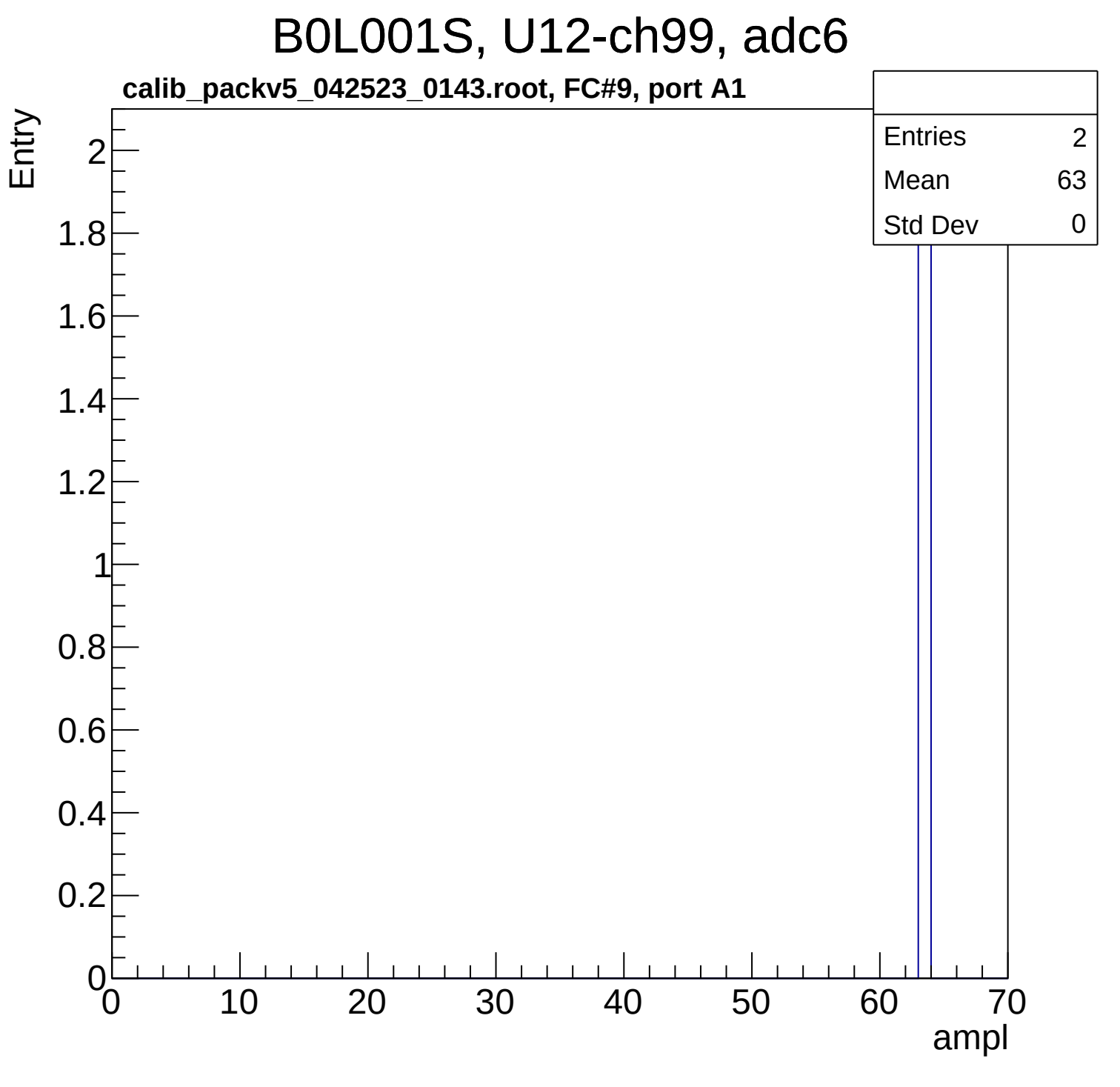
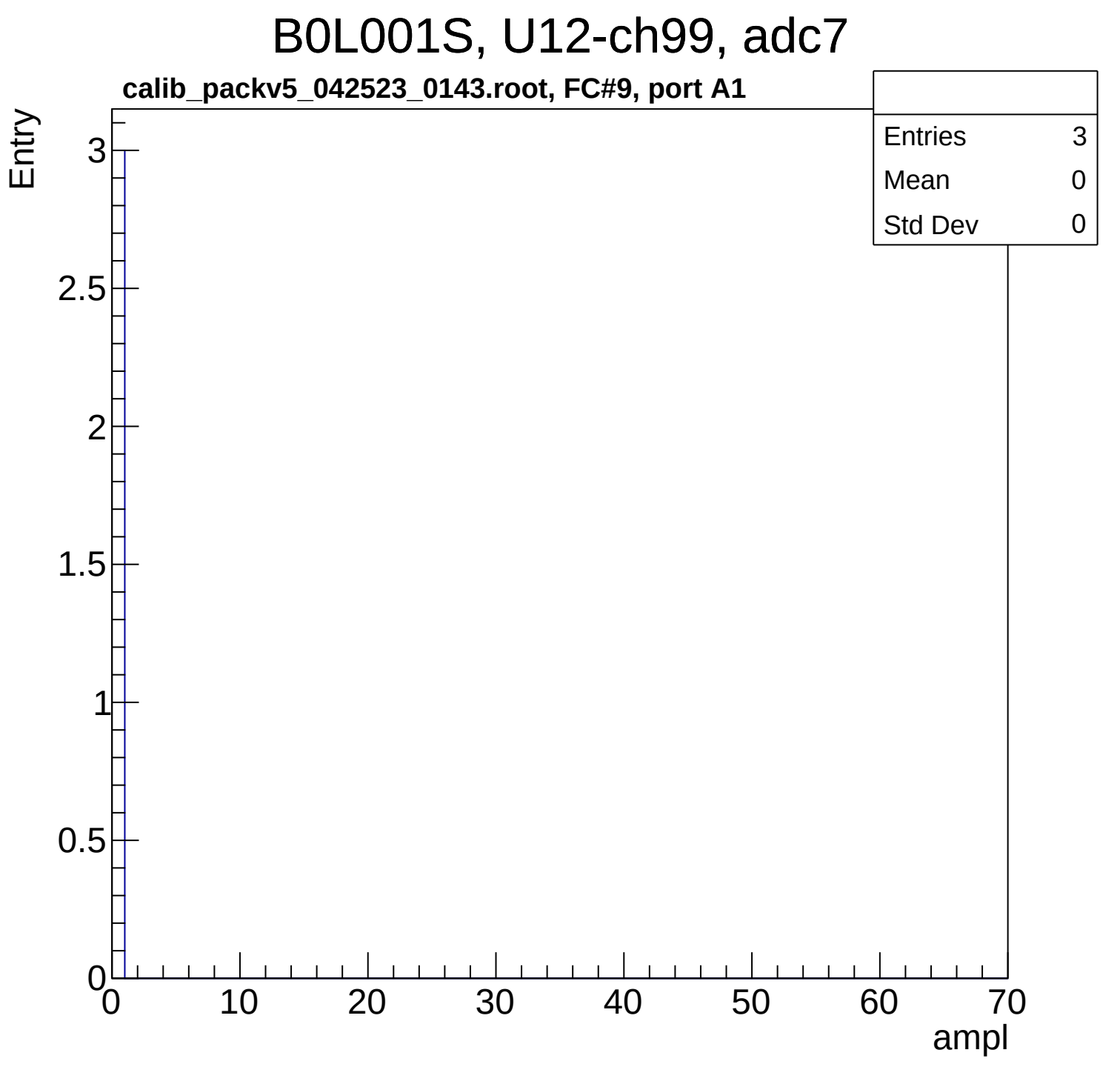
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch99, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 75
Mean 51.04
Std Dev 3.048
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch99, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 49
Mean 57.49
Std Dev 2.908
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch99, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 38
Mean 58.71
Std Dev 9.878
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B0L001S, U12-ch99, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L001S, U12-ch99, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 3
Mean 0
Std Dev 0
Entry
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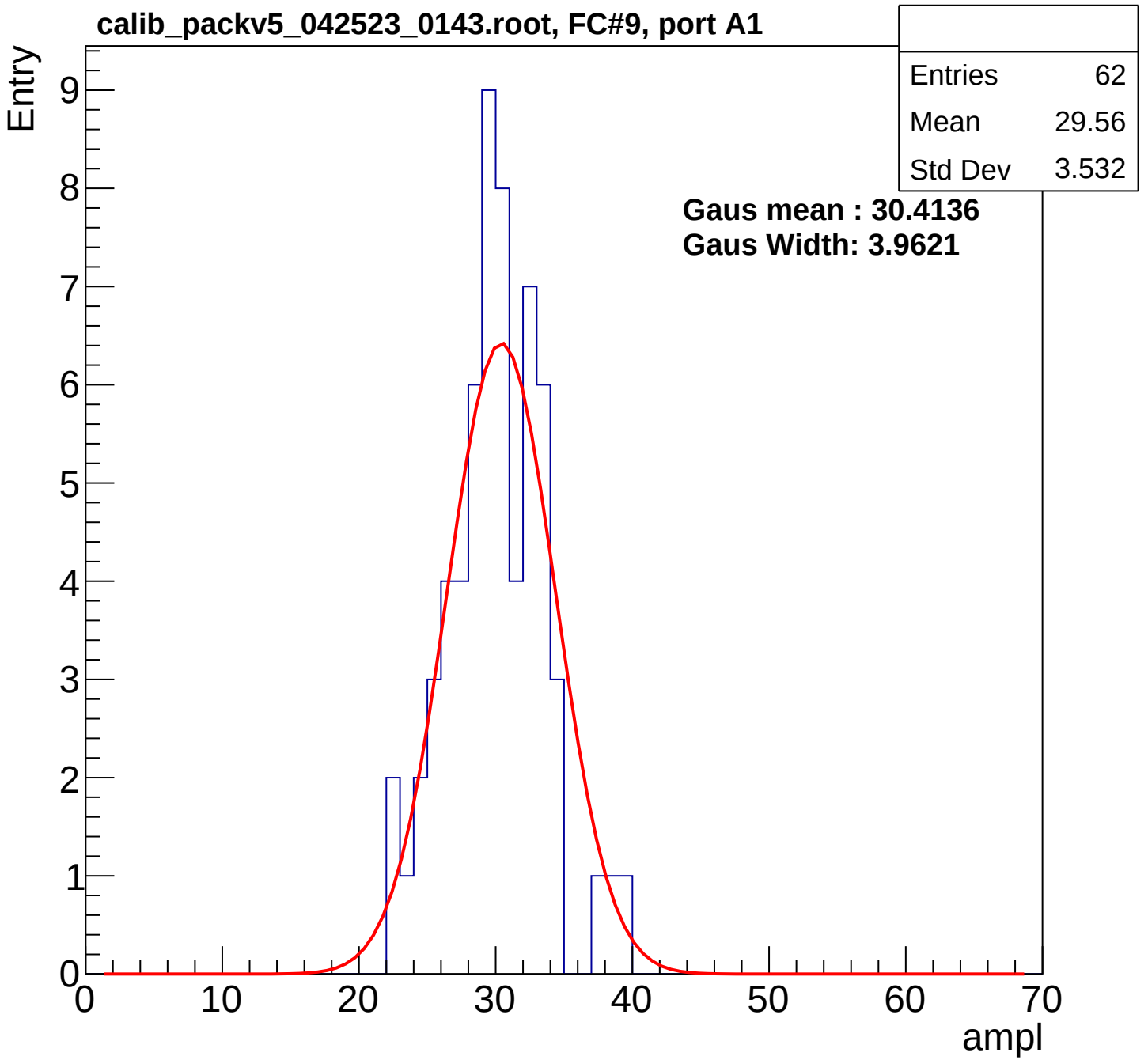
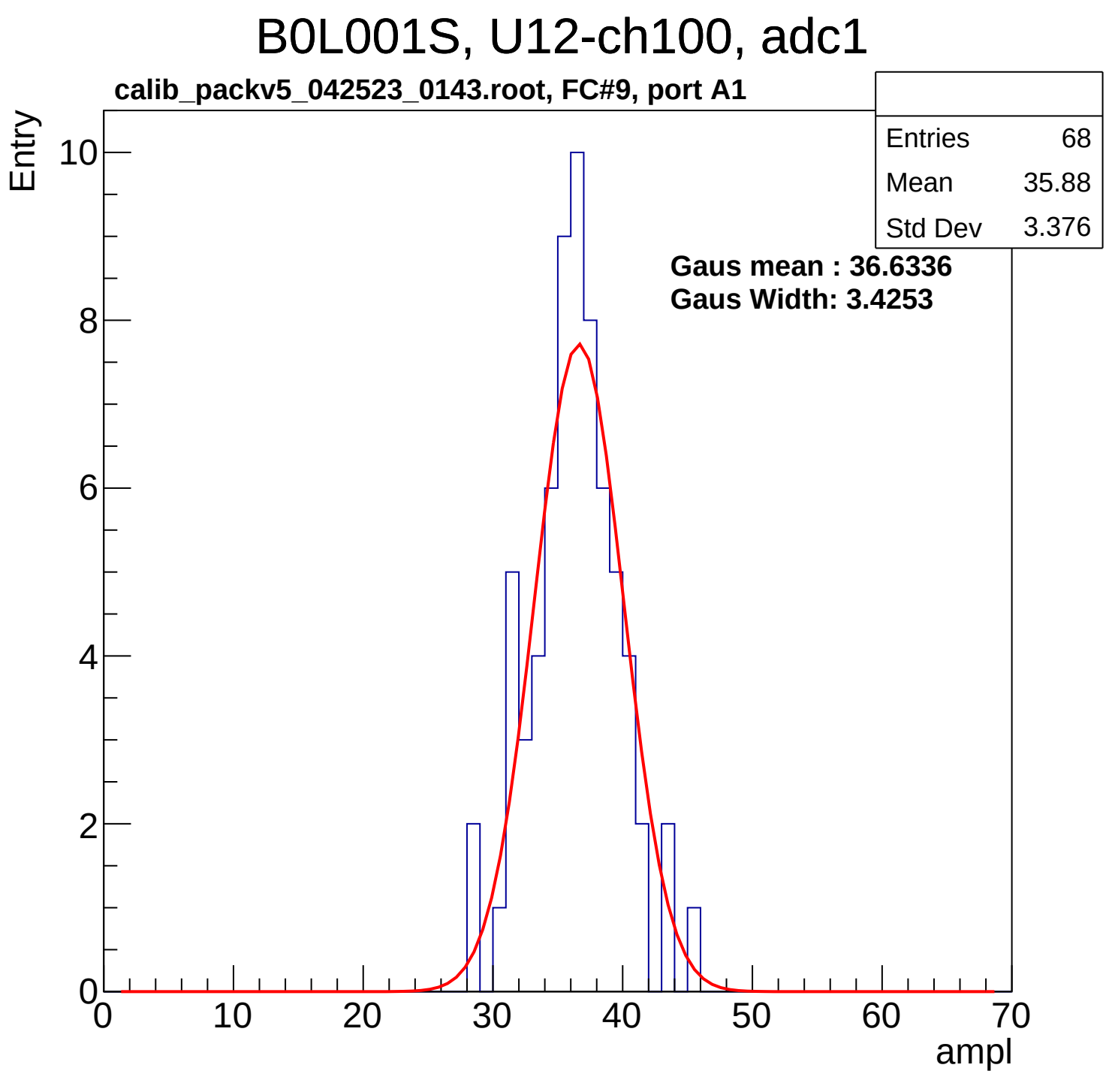
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch100, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 62
Mean 29.56
Std Dev 3.532
Gaus mean : 30.4136
Gaus Width: 3.9621
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch100, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 68
Mean 35.88
Std Dev 3.376
Gaus mean : 36.6336
Gaus Width: 3.4253
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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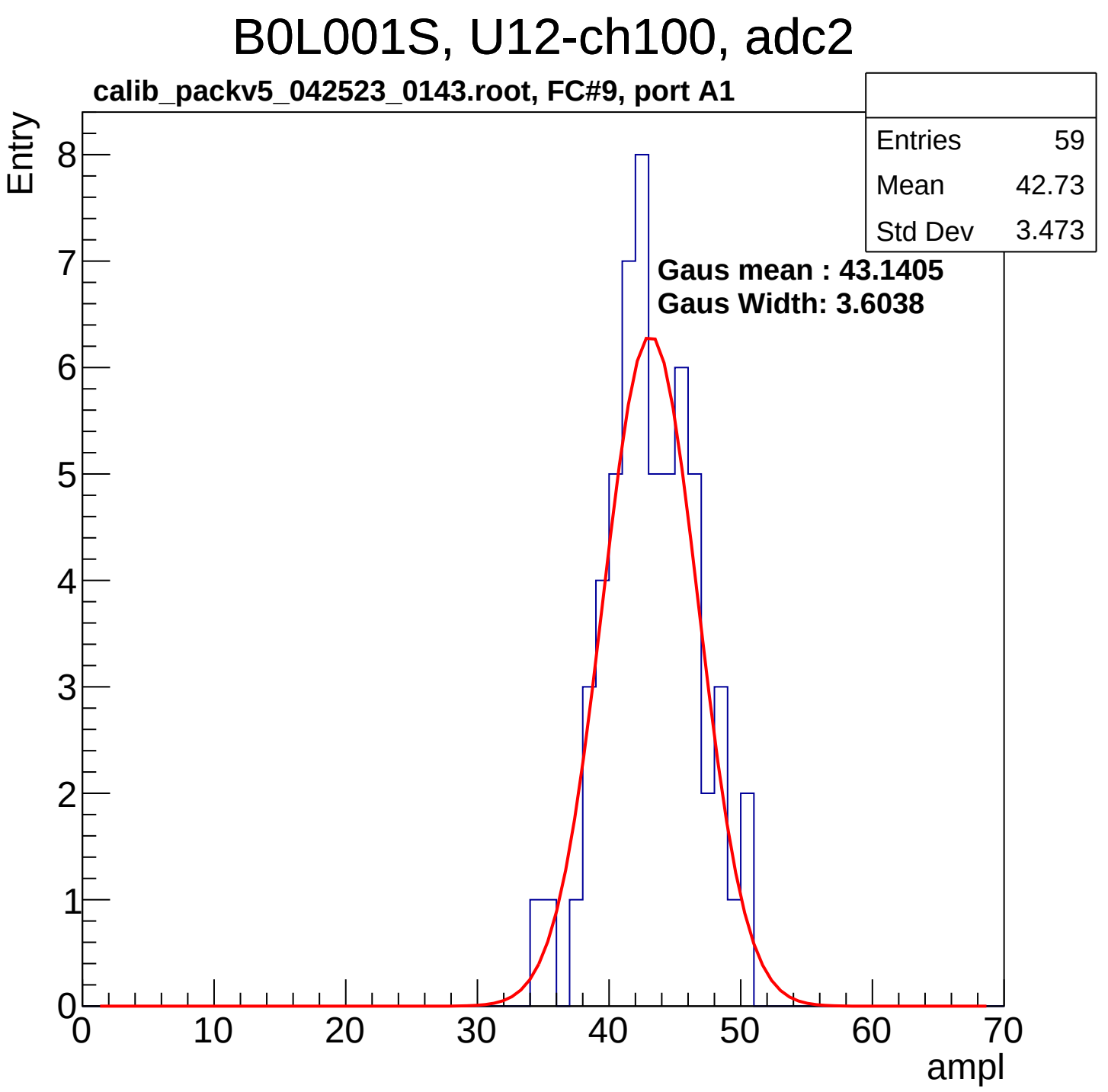
B0L001S, U12-ch100, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 59
Mean 42.73
Std Dev 3.473
Gaus mean : 43.1405
Gaus Width: 3.6038
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
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60
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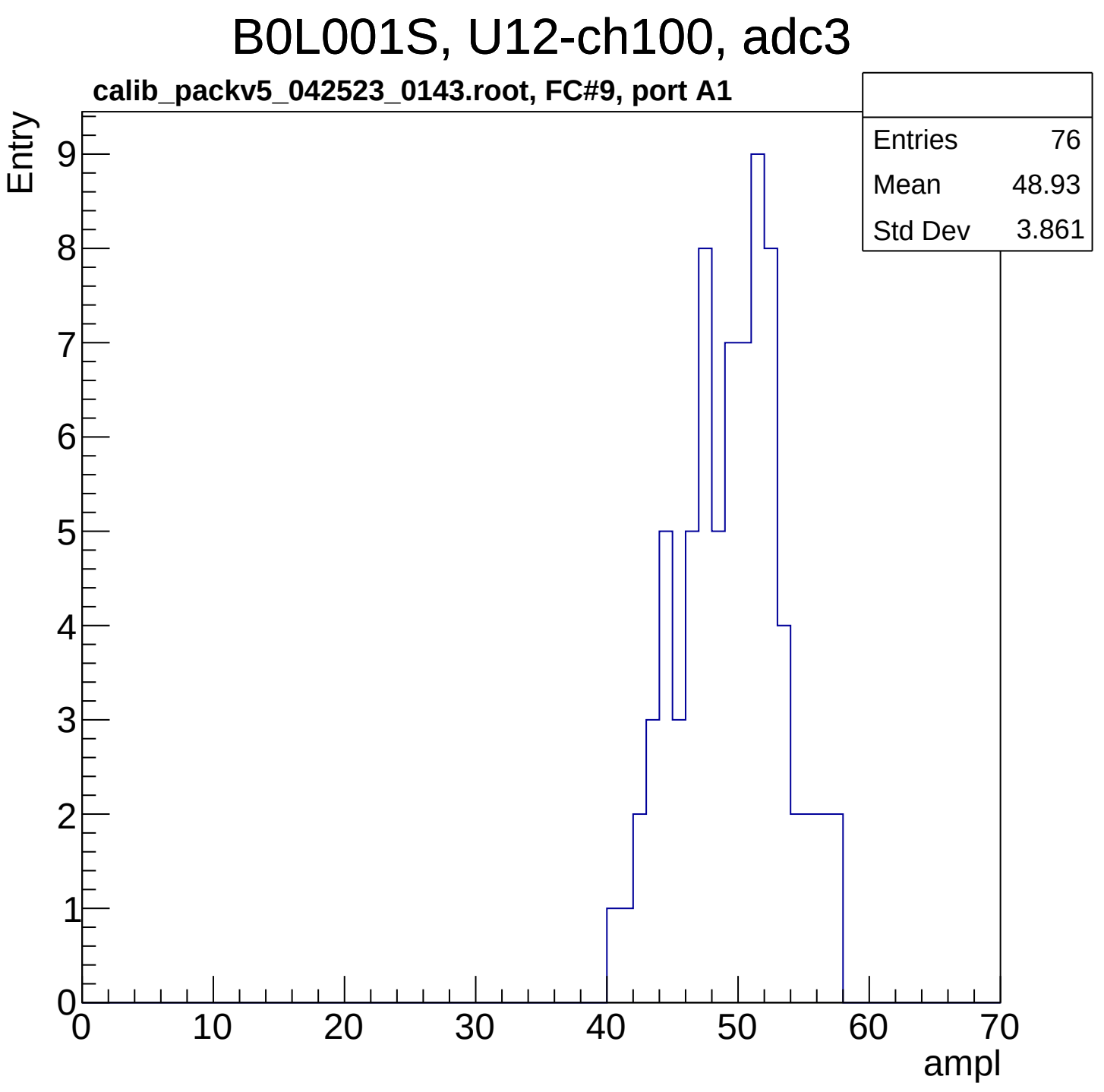
B0L001S, U12-ch100, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 76
Mean 48.93
Std Dev 3.861
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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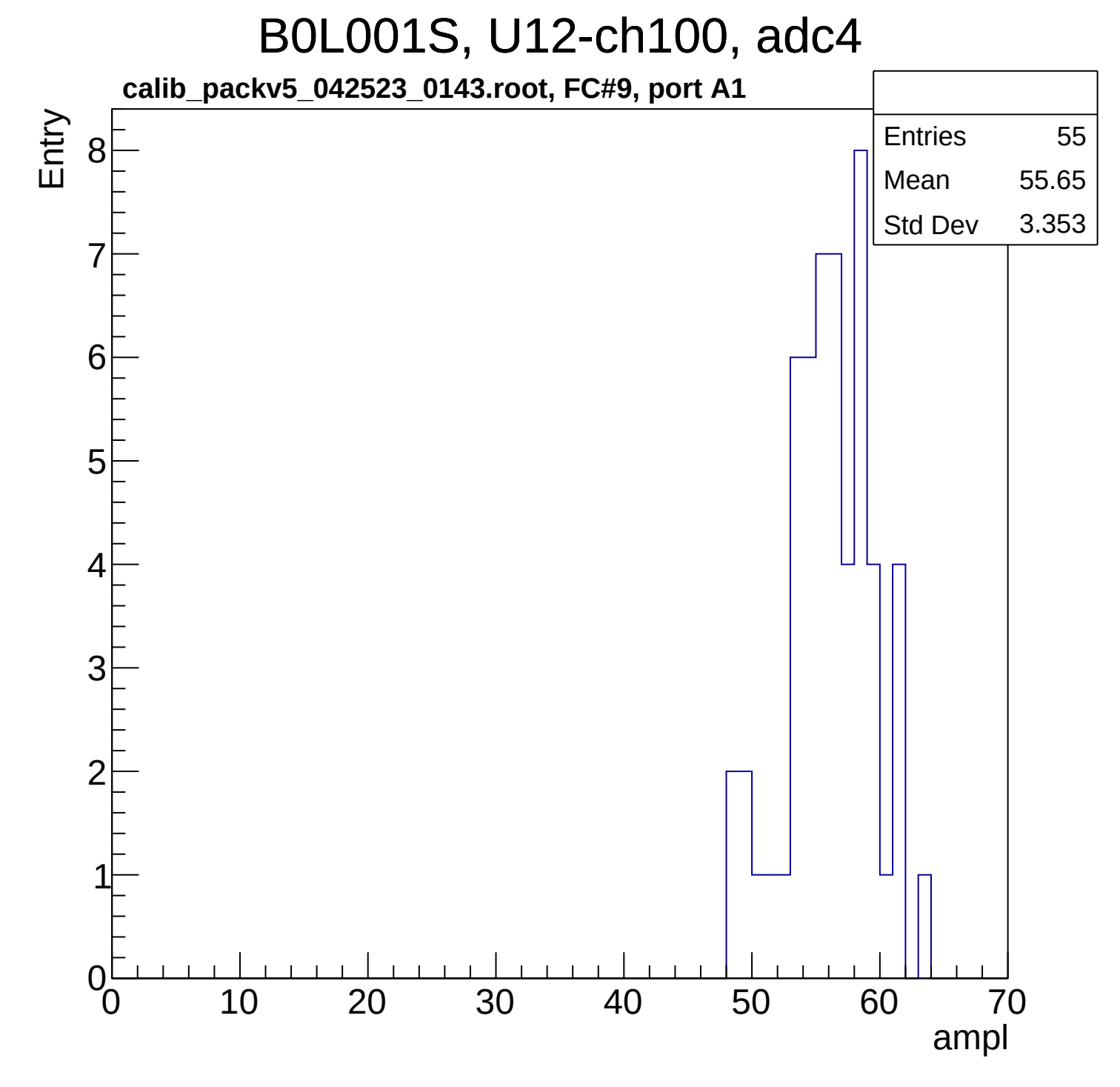
B0L001S, U12-ch100, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 55
Mean 55.65
Std Dev 3.353
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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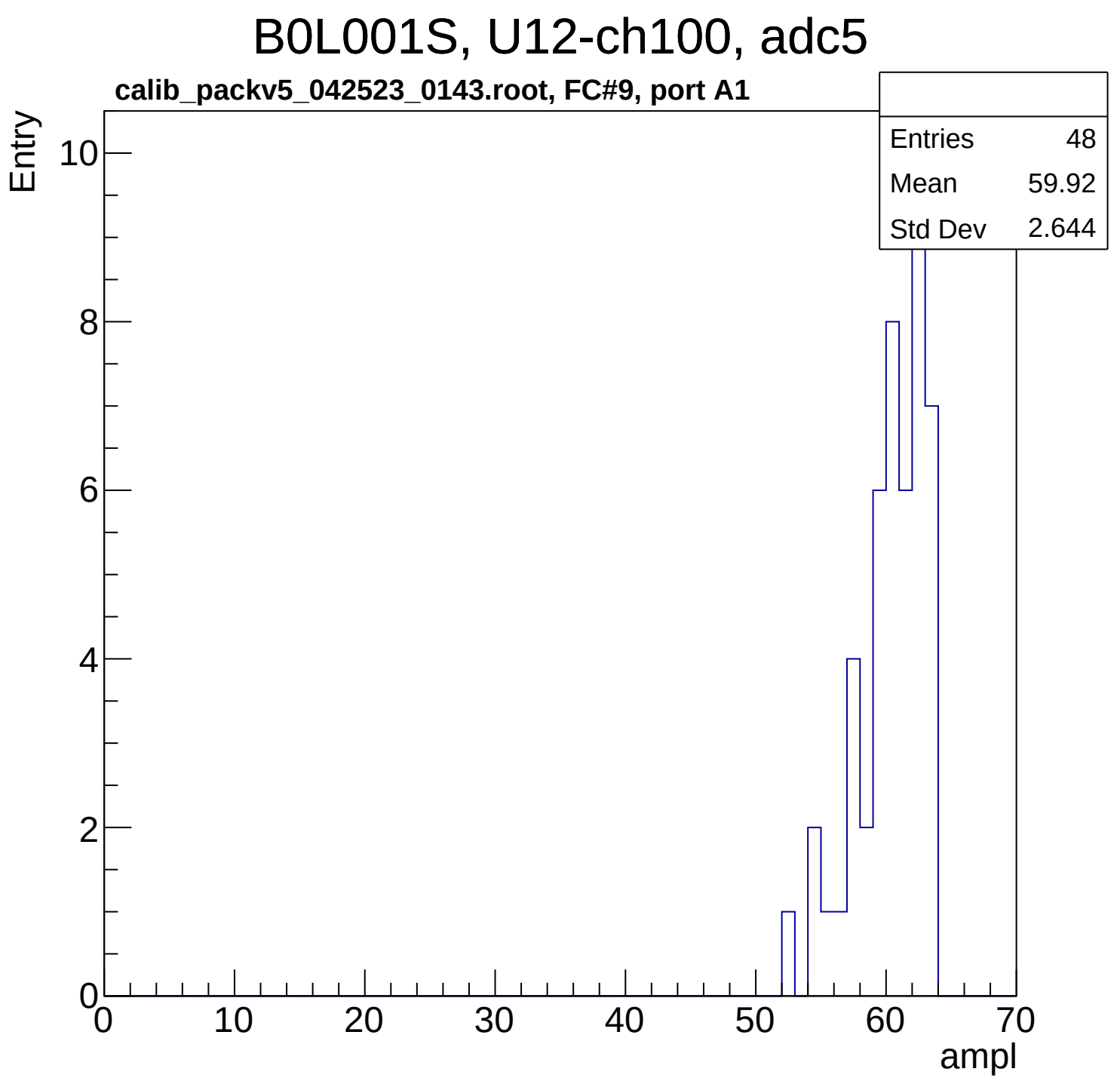
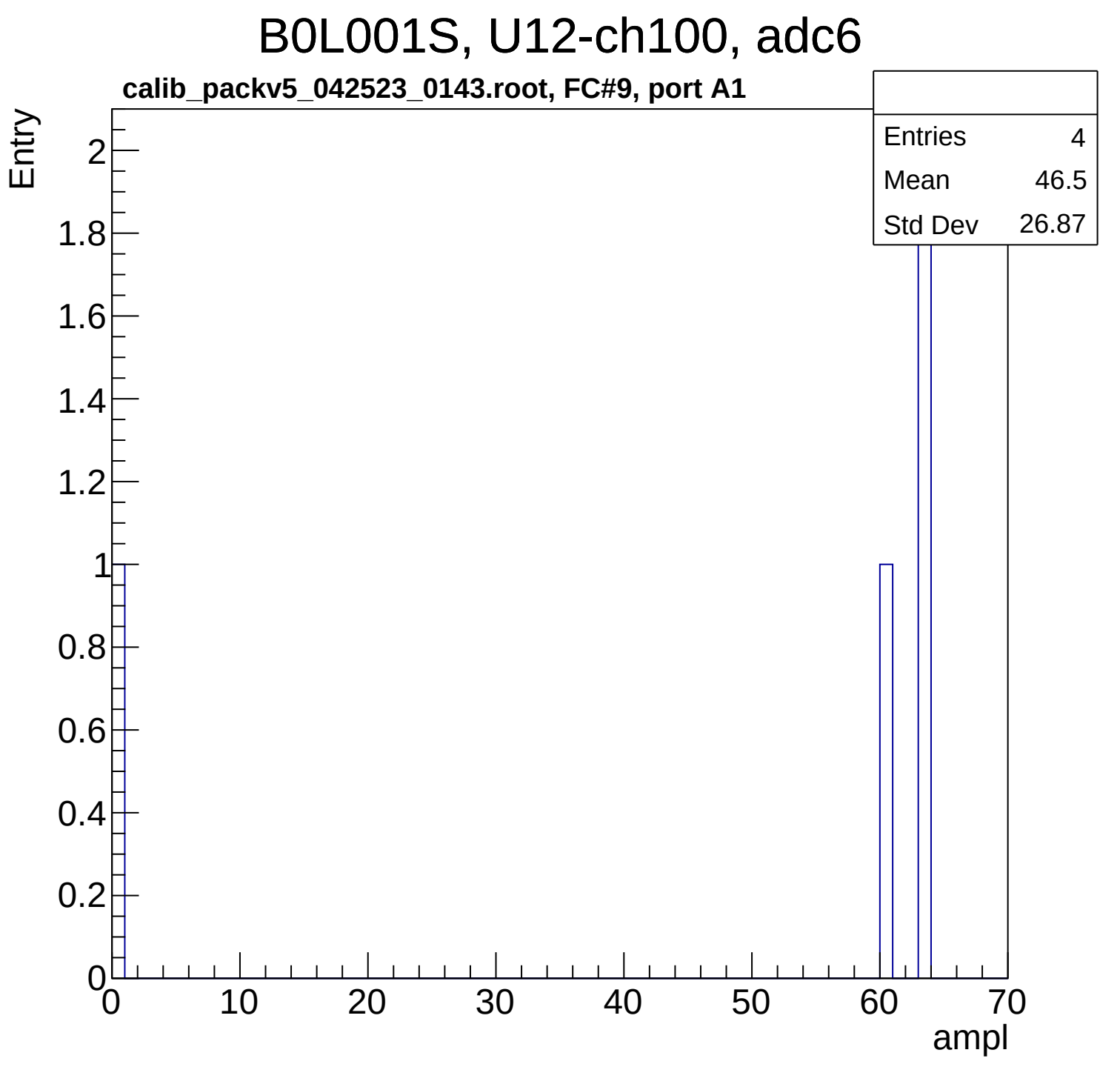

B0L001S, U12-ch100, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 48
Mean 59.92
Std Dev 2.644
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch100, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 4
Mean 46.5
Std Dev 26.87
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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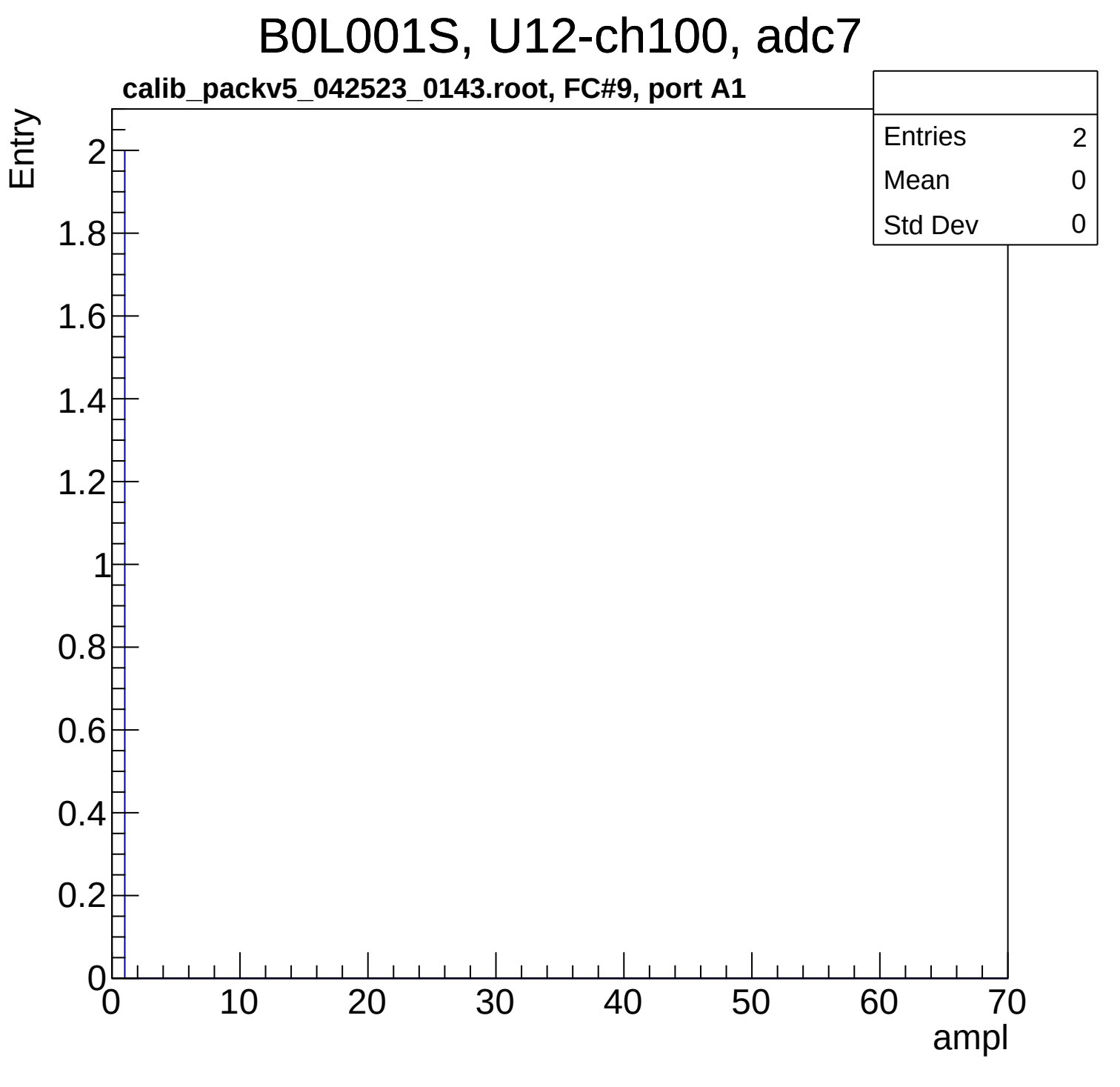
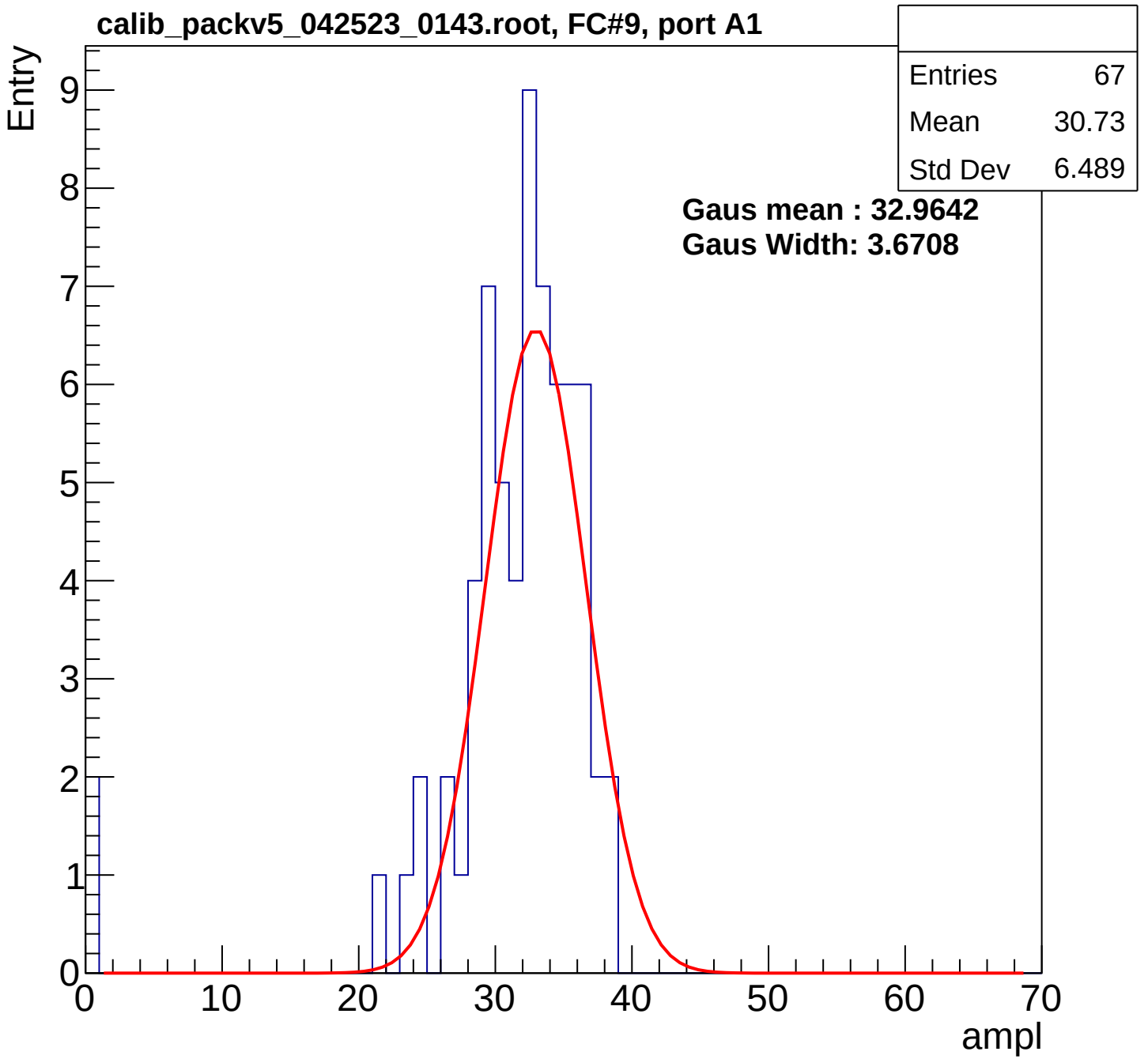

B0L001S, U12-ch100, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch101, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 67
Mean 30.73
Std Dev 6.489
Gaus mean : 32.9642
Gaus Width: 3.6708
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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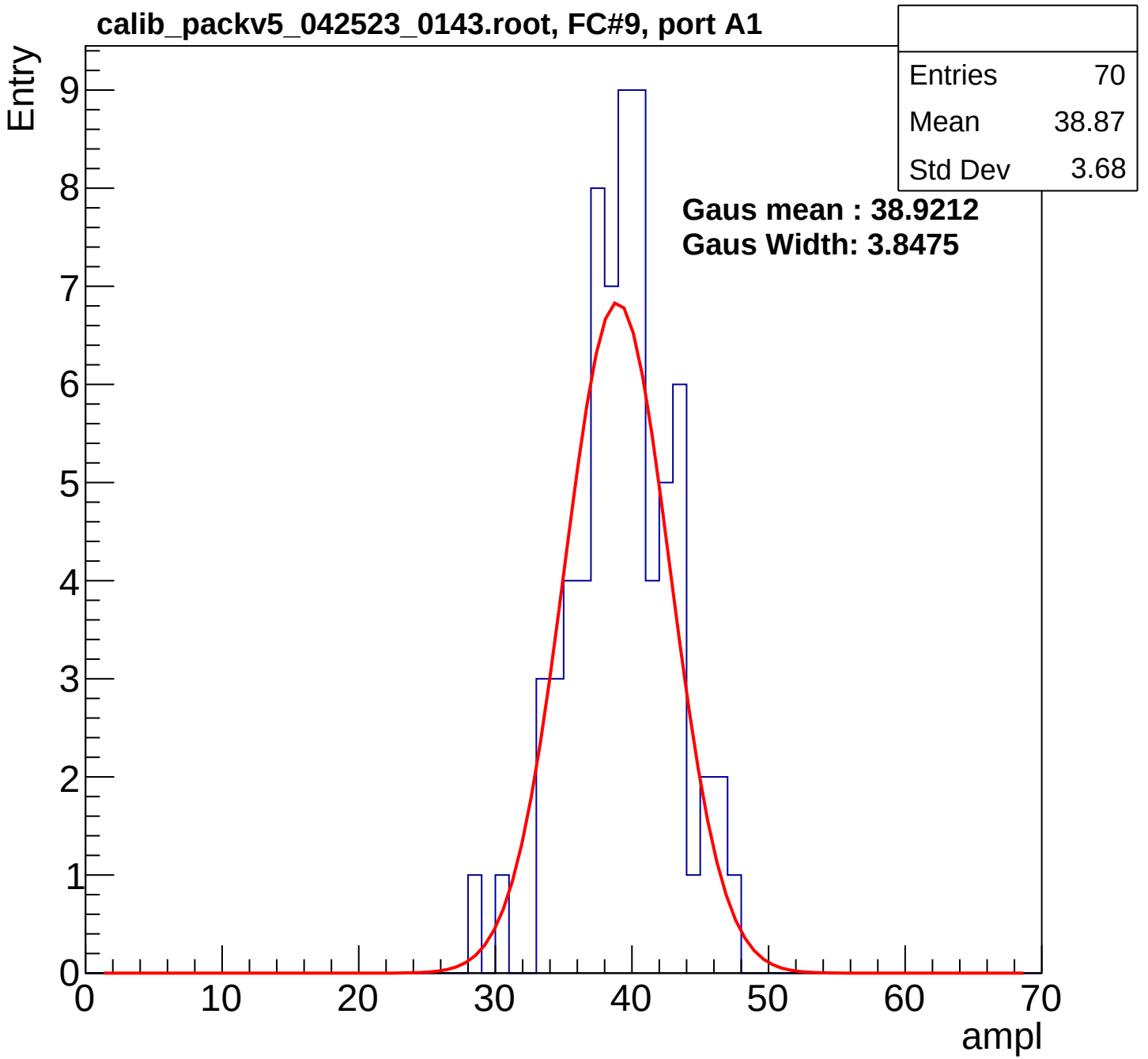
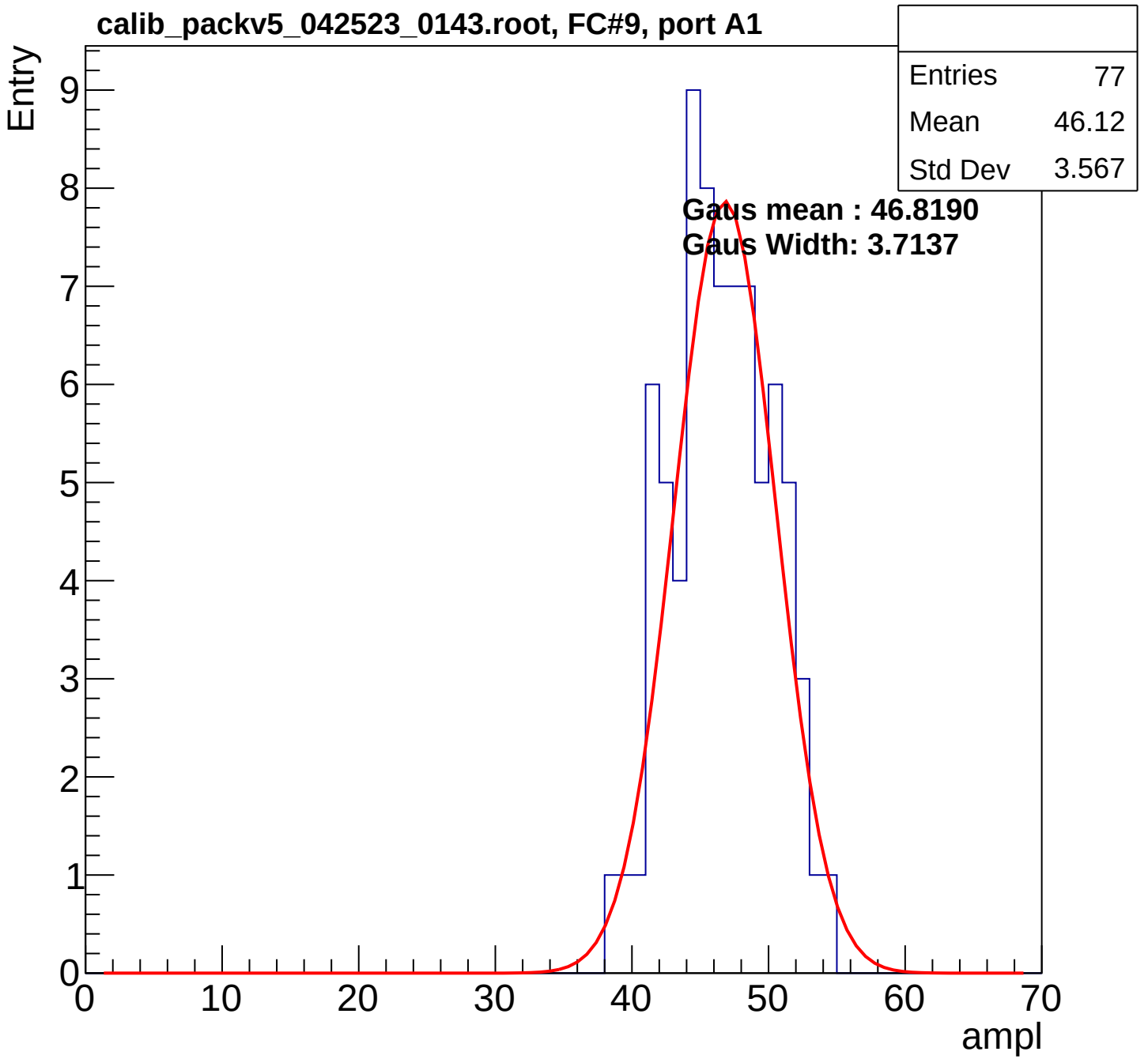

B0L001S, U12-ch101, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 70
Mean 38.87
Std Dev 3.68
Gaus mean : 38.9212
Gaus Width: 3.8475
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch101, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 77
Mean 46.12
Std Dev 3.567
Gaus mean : 46.8190
Gaus Width: 3.7137
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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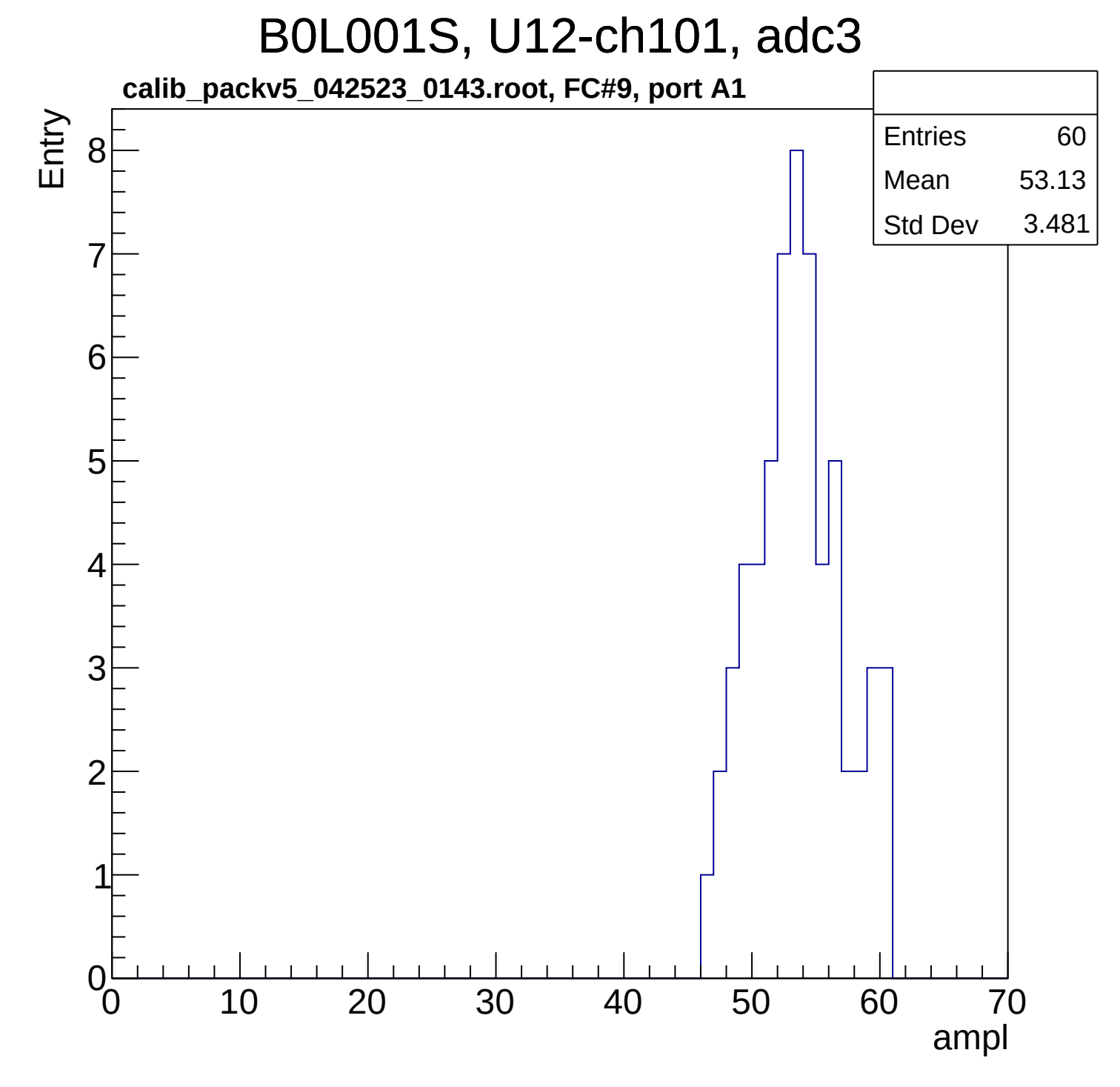
B0L001S, U12-ch101, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 60
Mean 53.13
Std Dev 3.481
Entry
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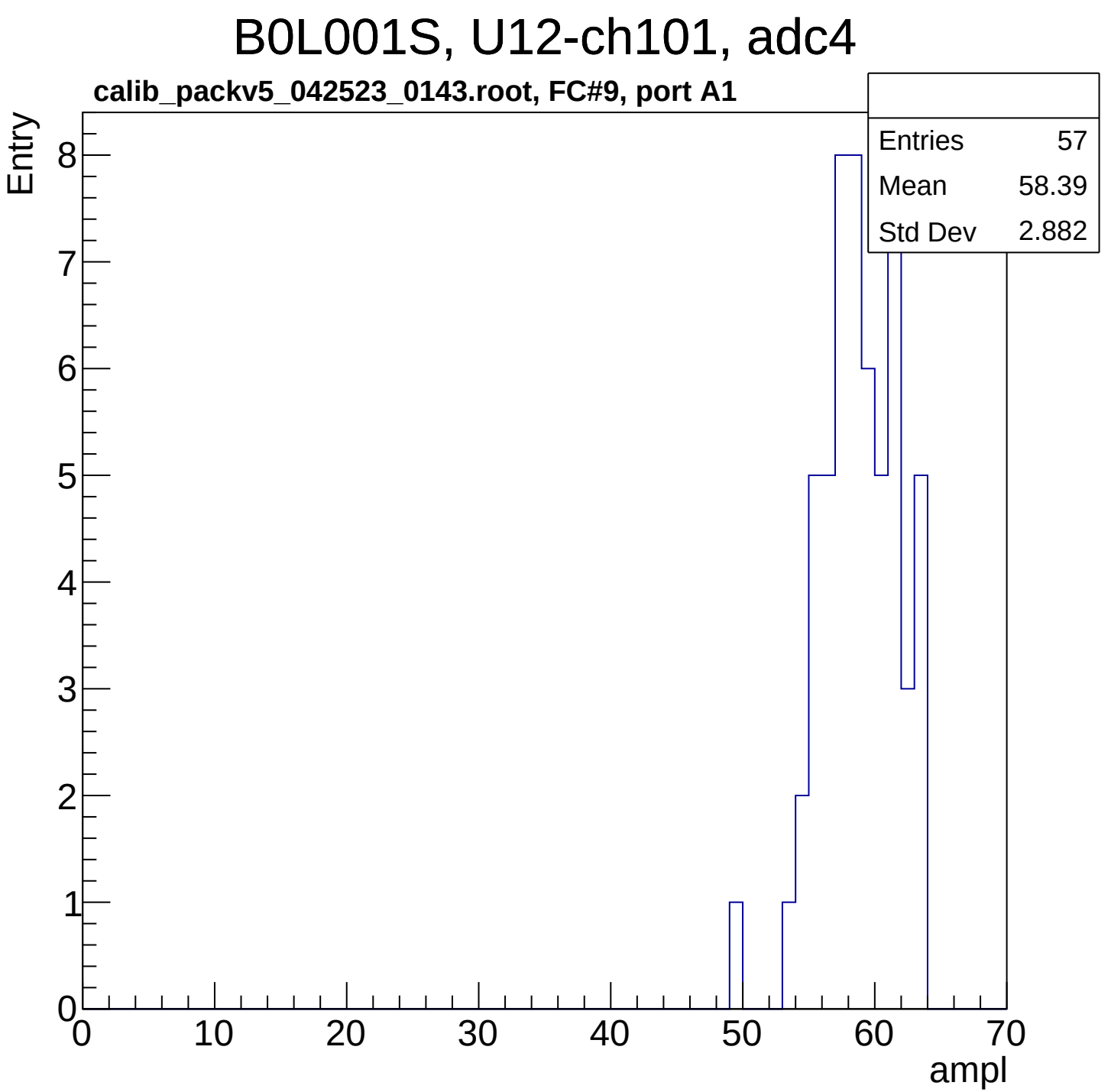
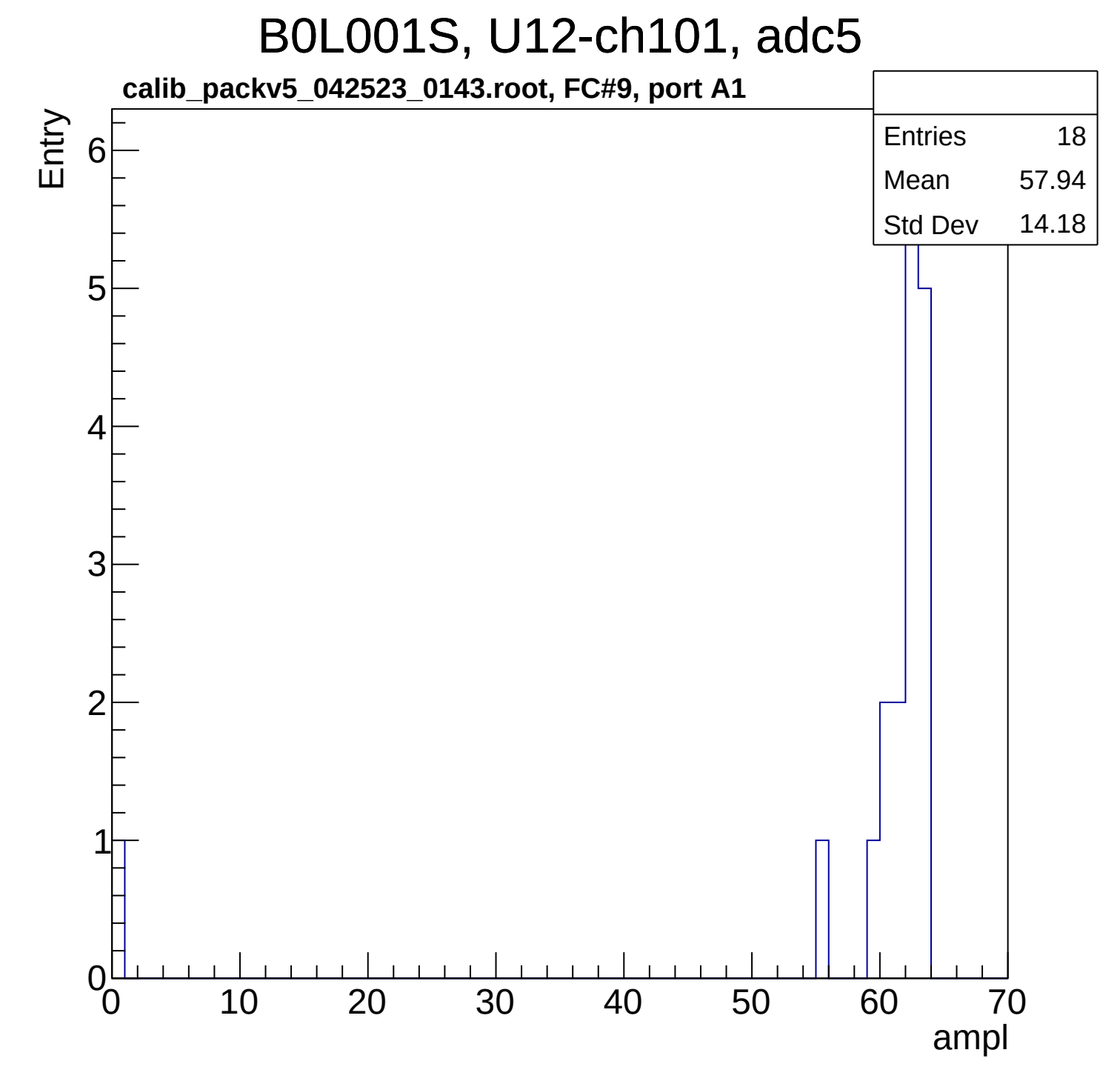
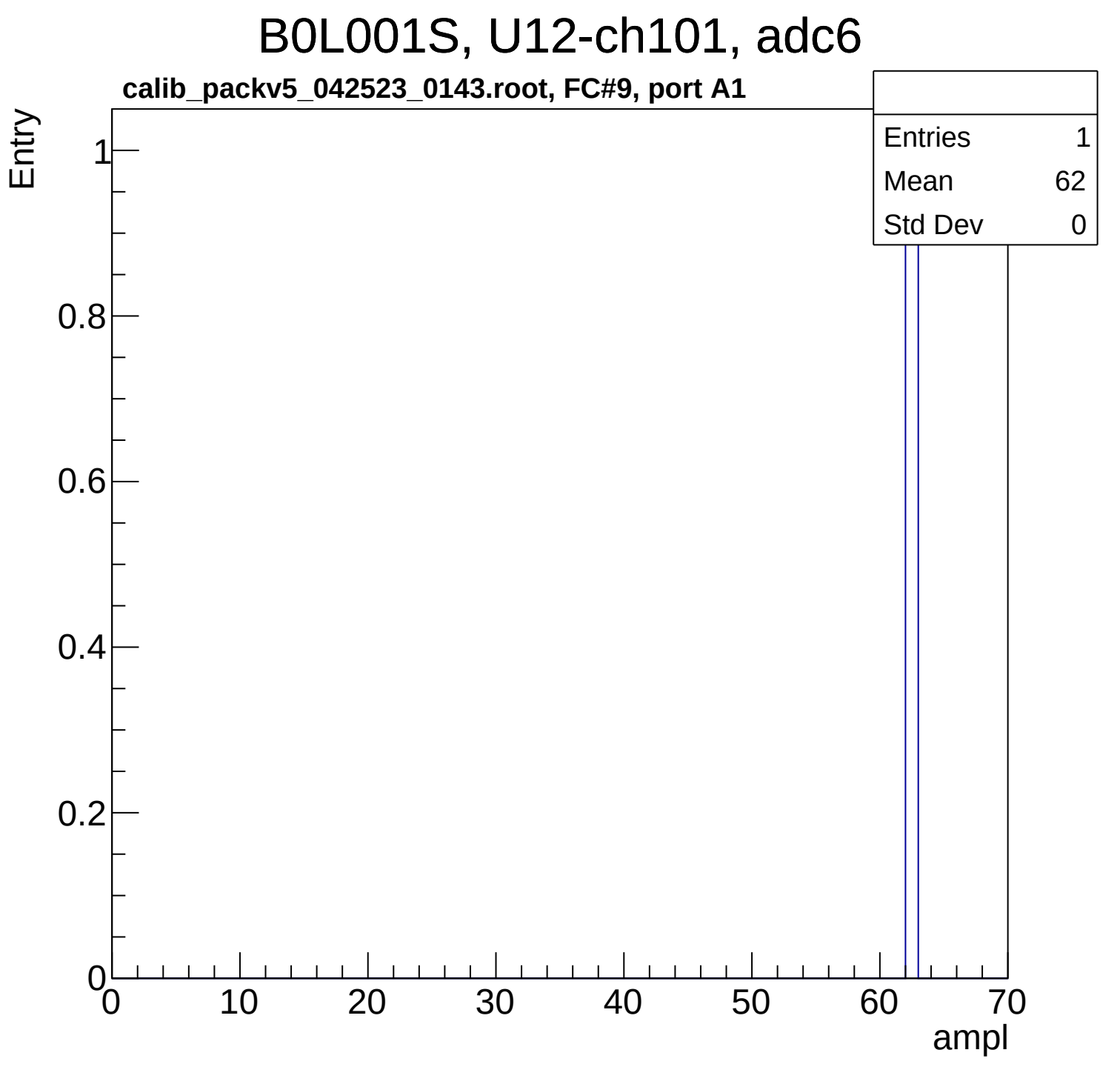
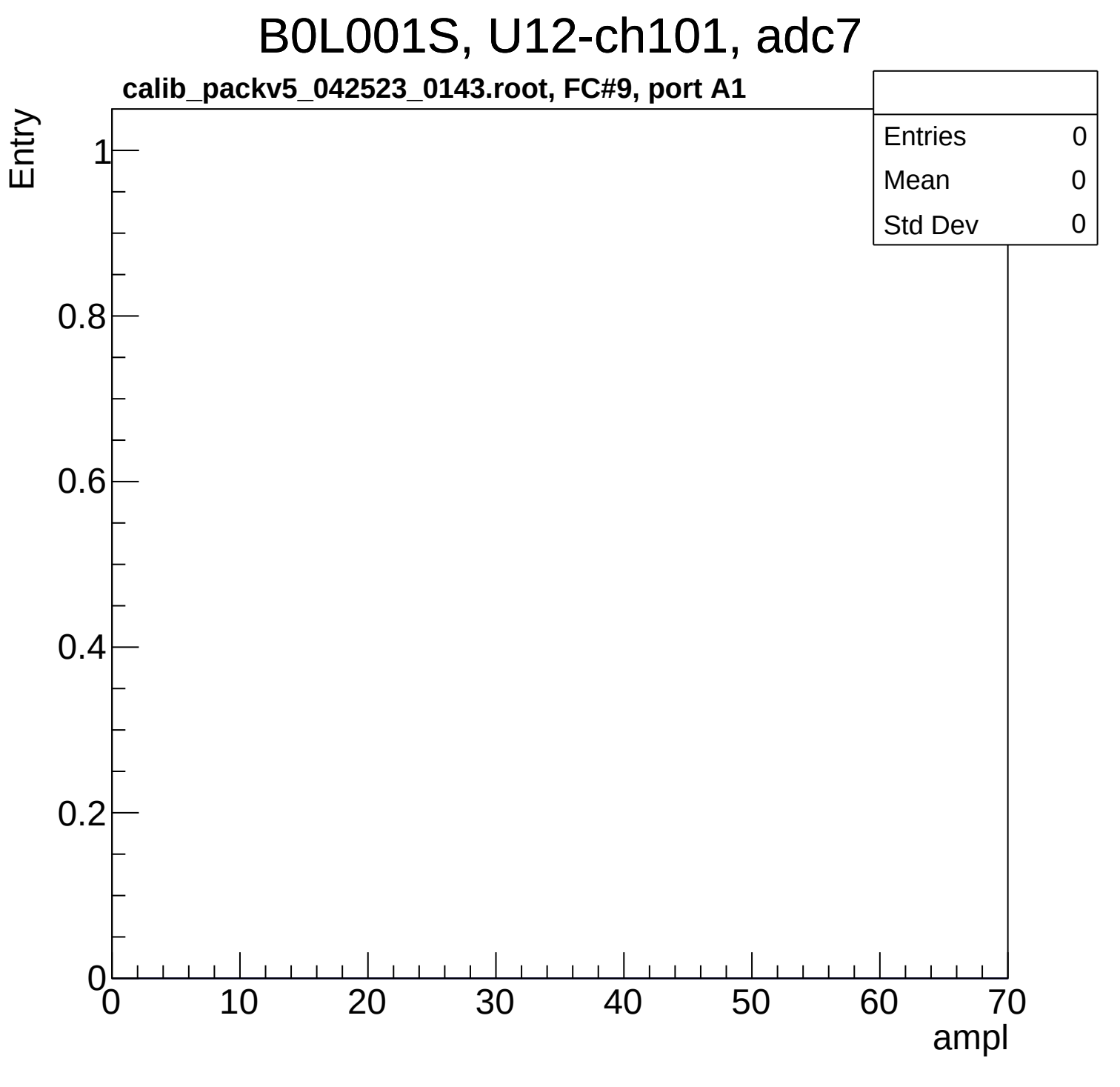
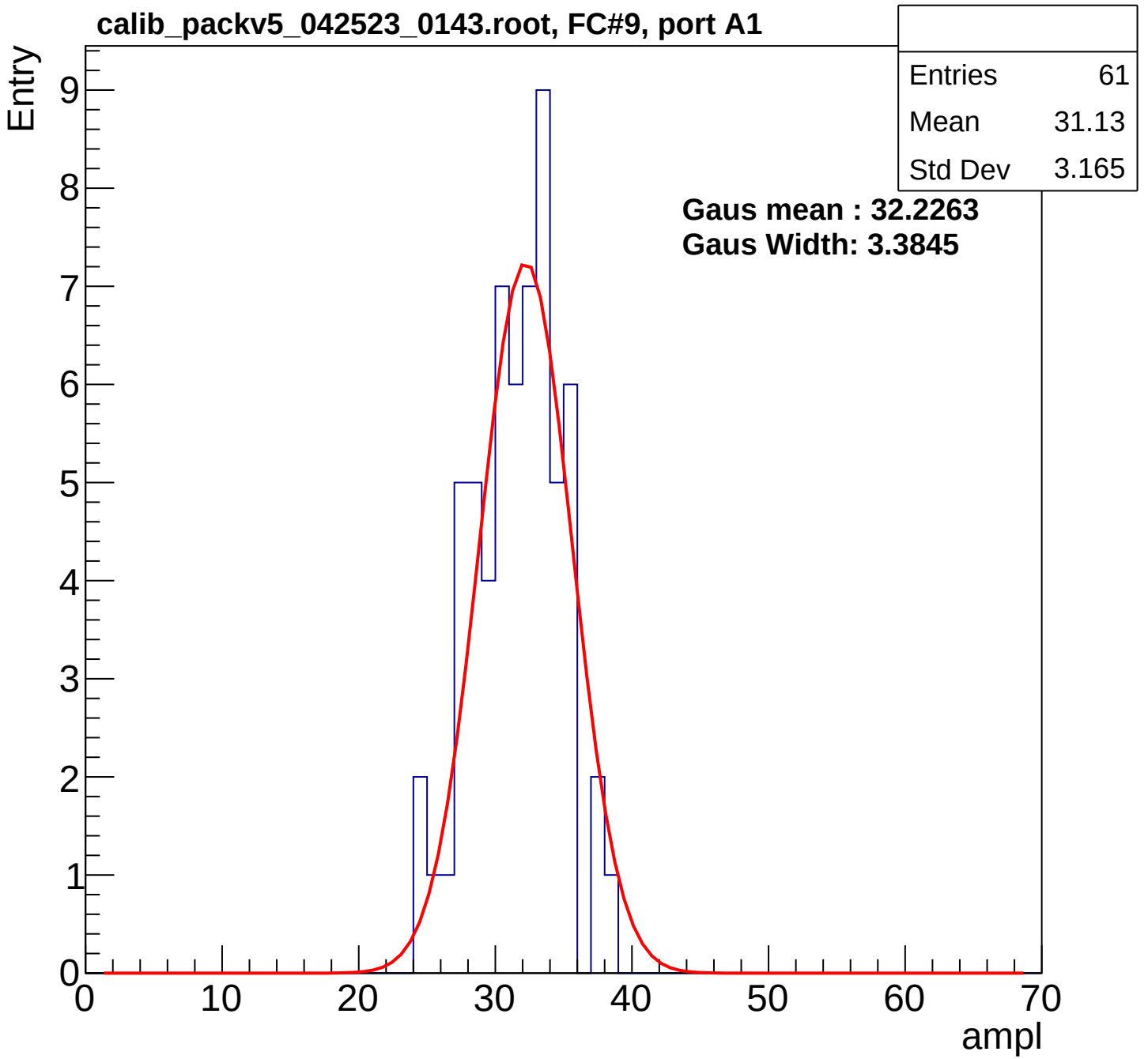
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch101, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 57
Mean 58.39
Std Dev 2.882
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch101, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 18
Mean 57.94
Std Dev 14.18
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch101, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch101, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch102, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 61
Mean 31.13
Std Dev 3.165
Gaus mean : 32.2263
Gaus Width: 3.3845
Entry
ampl
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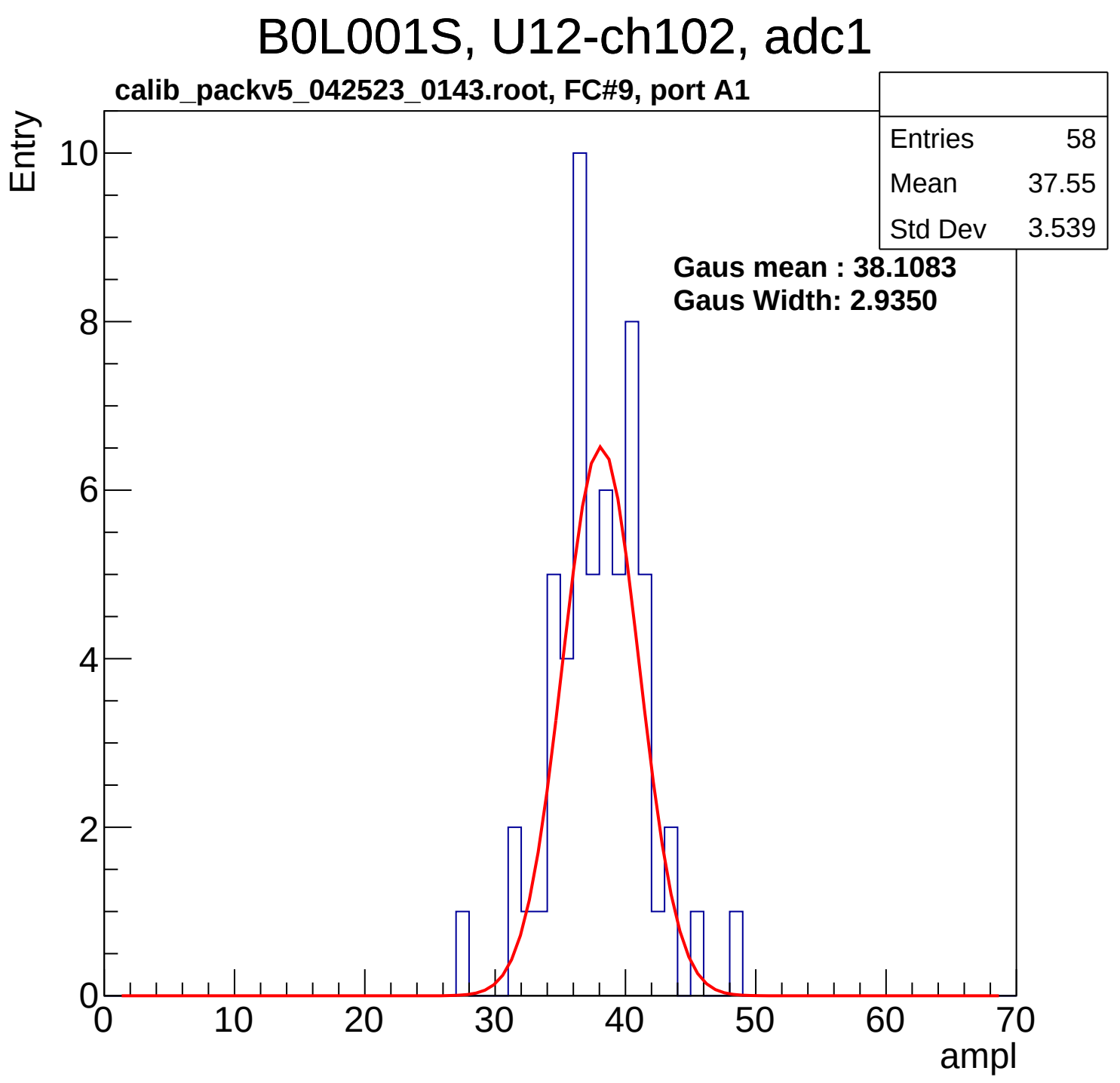
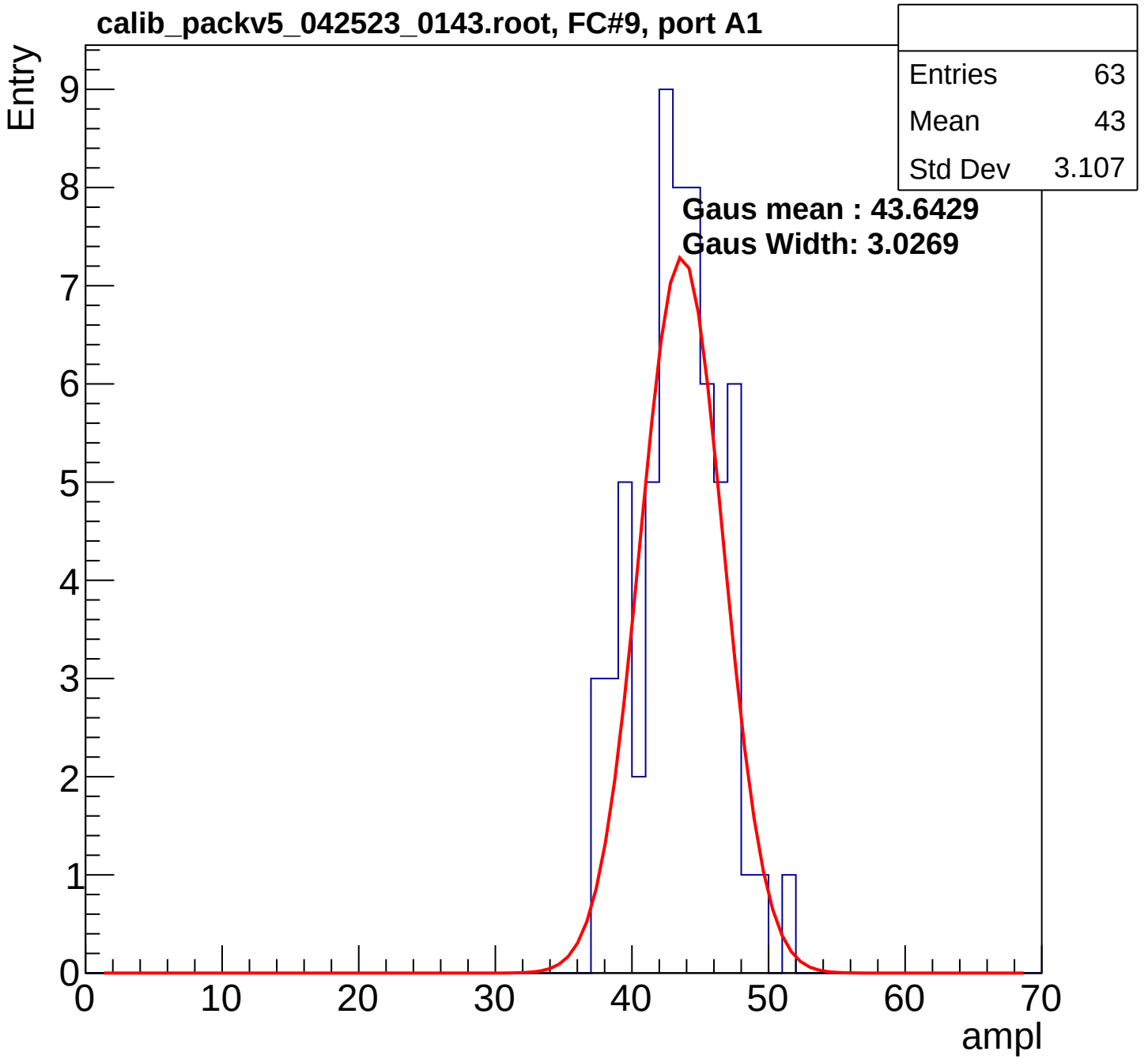
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch102, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 58
Mean 37.55
Std Dev 3.539
Gaus mean : 38.1083
Gaus Width: 2.9350
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch102, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 63
Mean 43
Std Dev 3.107
Gaus mean : 43.6429
Gaus Width: 3.0269
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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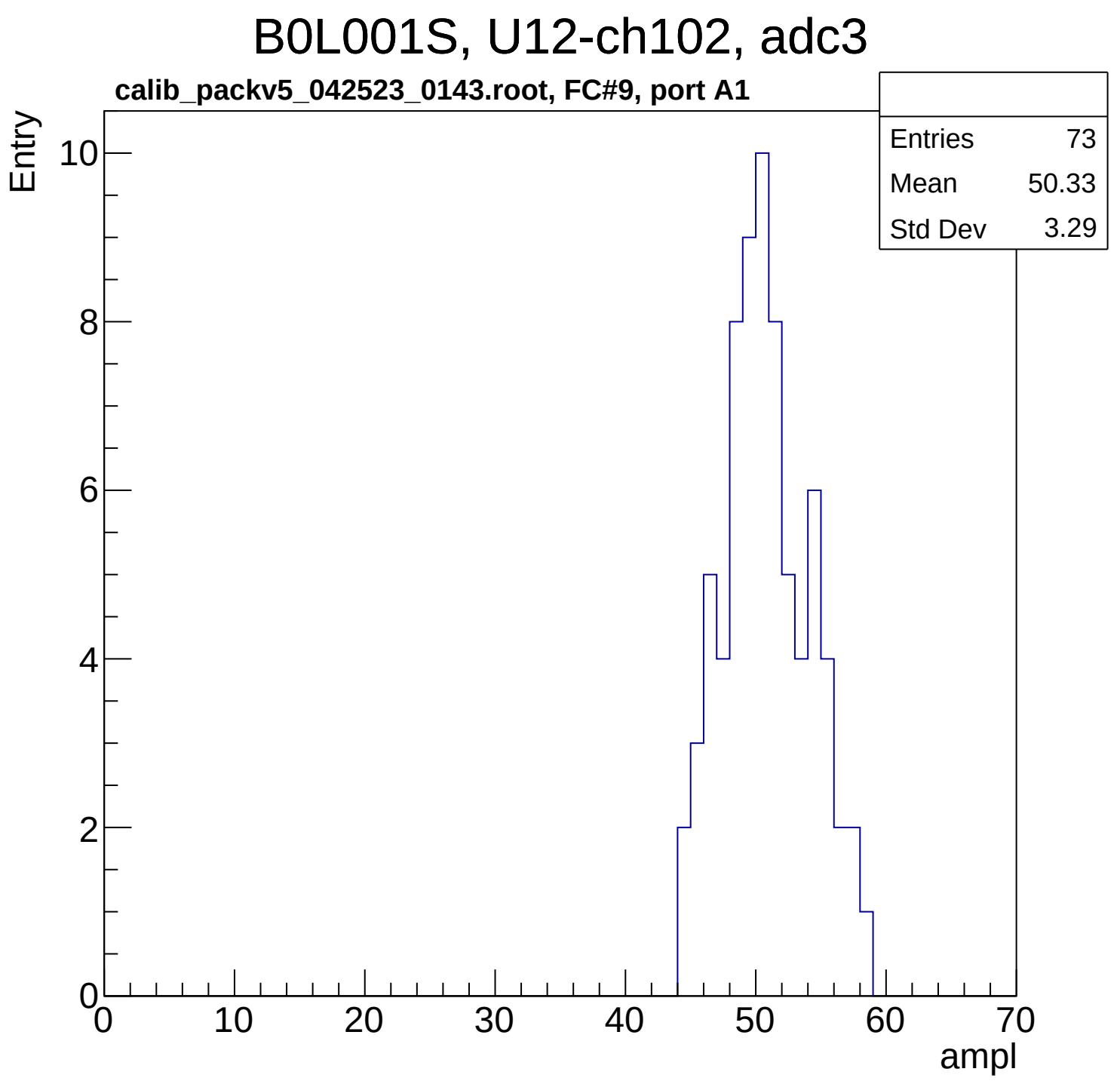
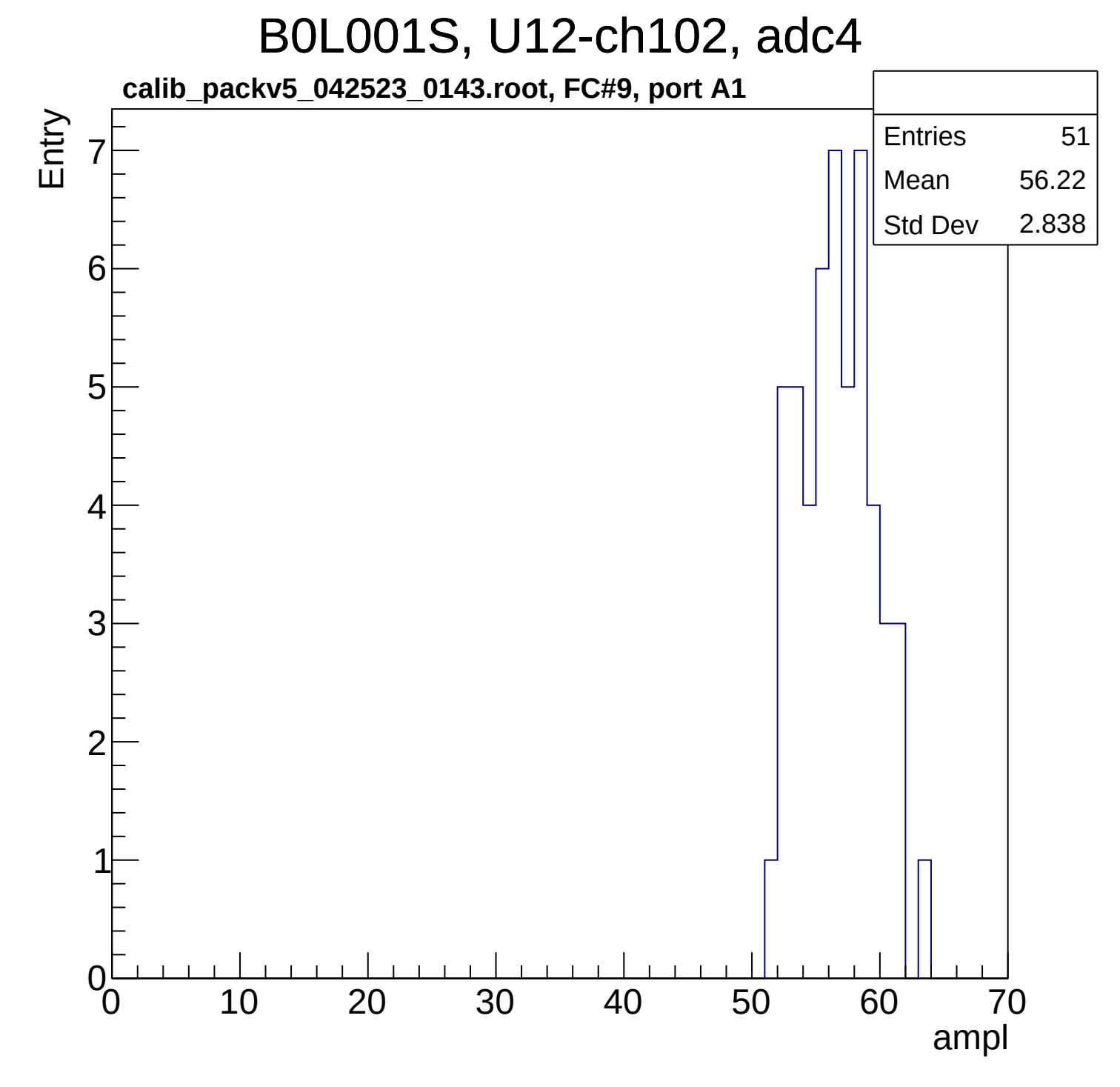

B0L001S, U12-ch102, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 73
Mean 50.33
Std Dev 3.29
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch102, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 51
Mean 56.22
Std Dev 2.838
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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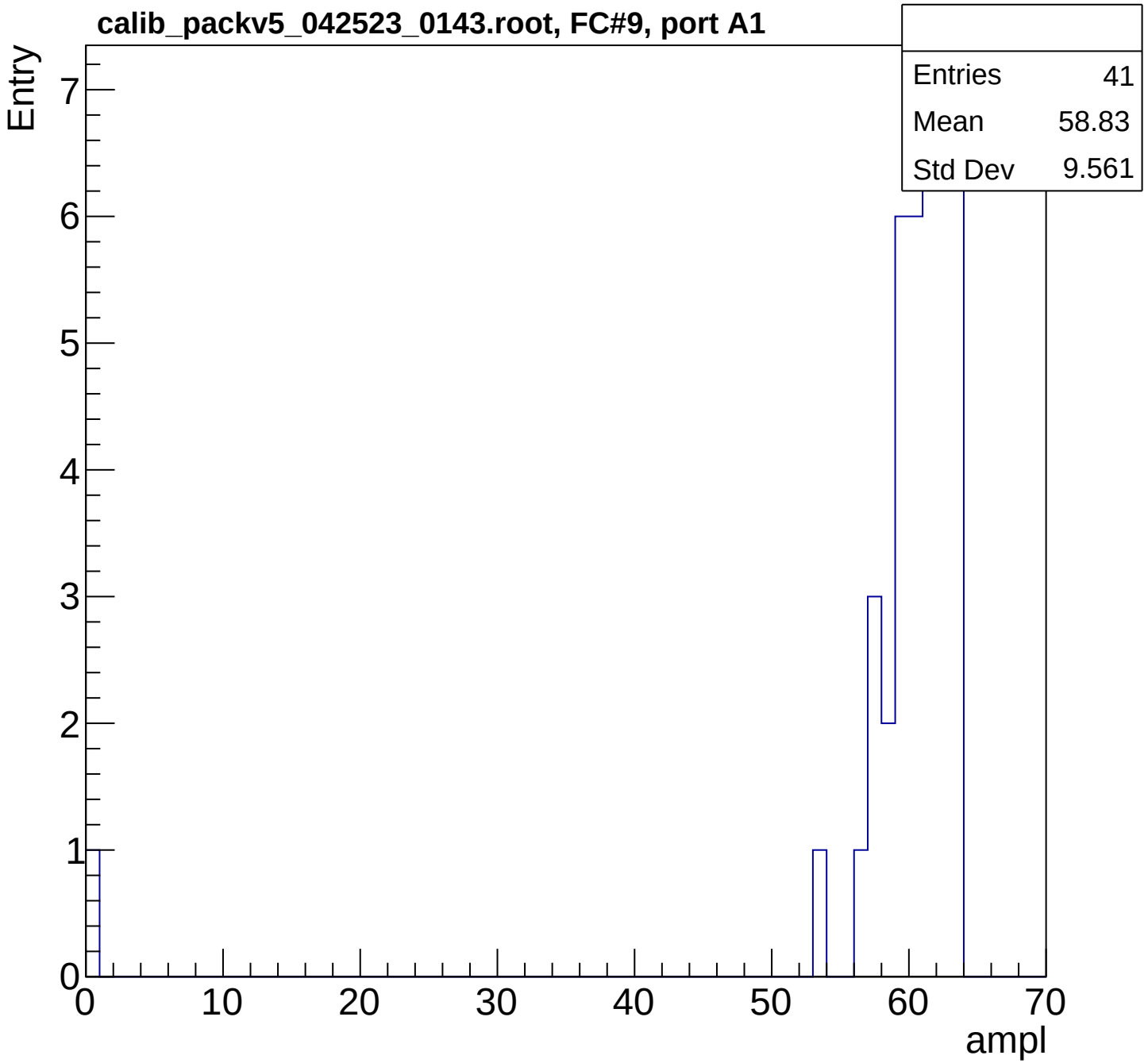
B0L001S, U12-ch102, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 41
Mean 58.83
Std Dev 9.561
Entry
ampl
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1
2
3
4
5
6
7
0
10
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40
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60
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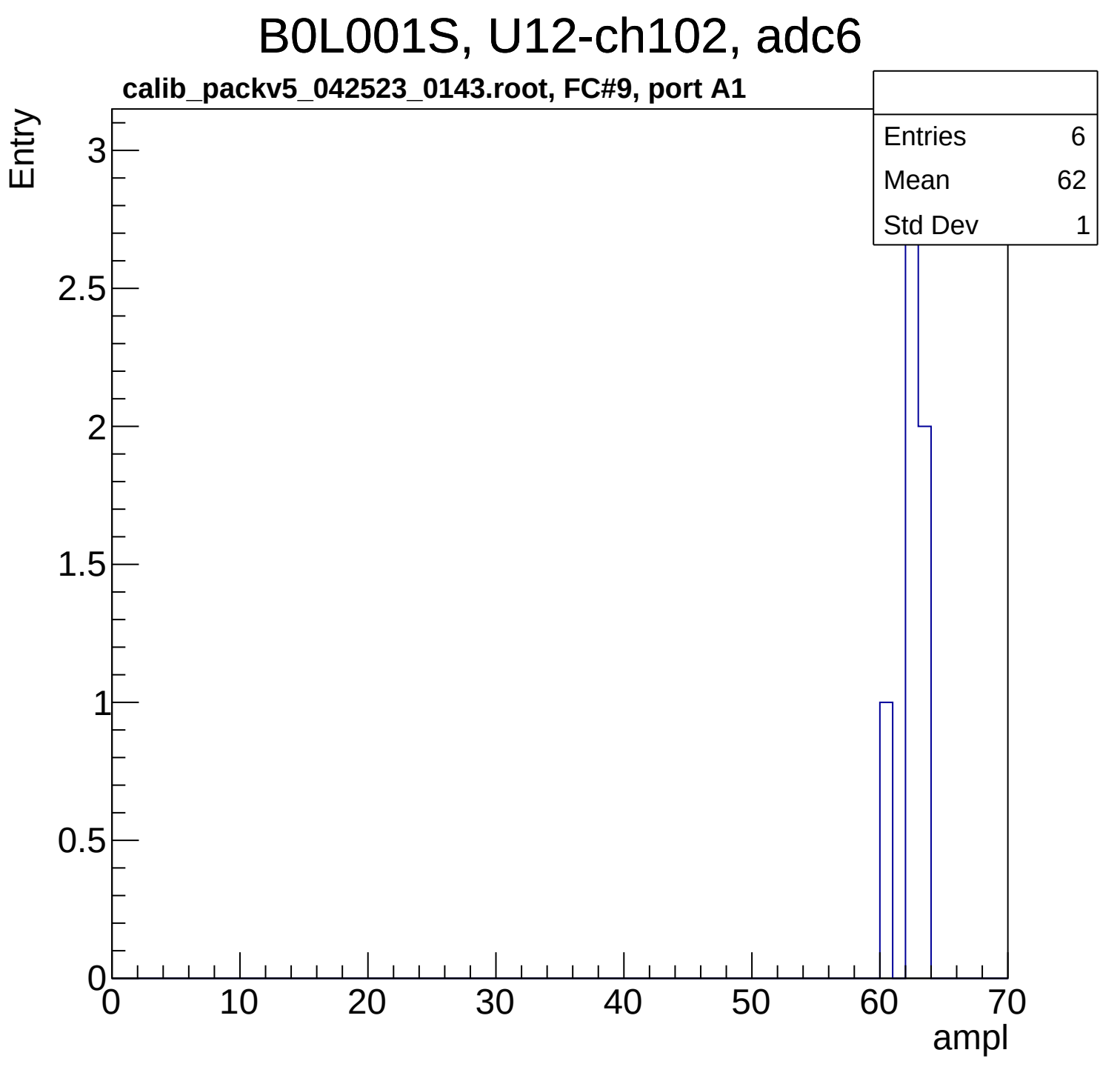
B0L001S, U12-ch102, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 6
Mean 62
Std Dev 1
Entry
ampl
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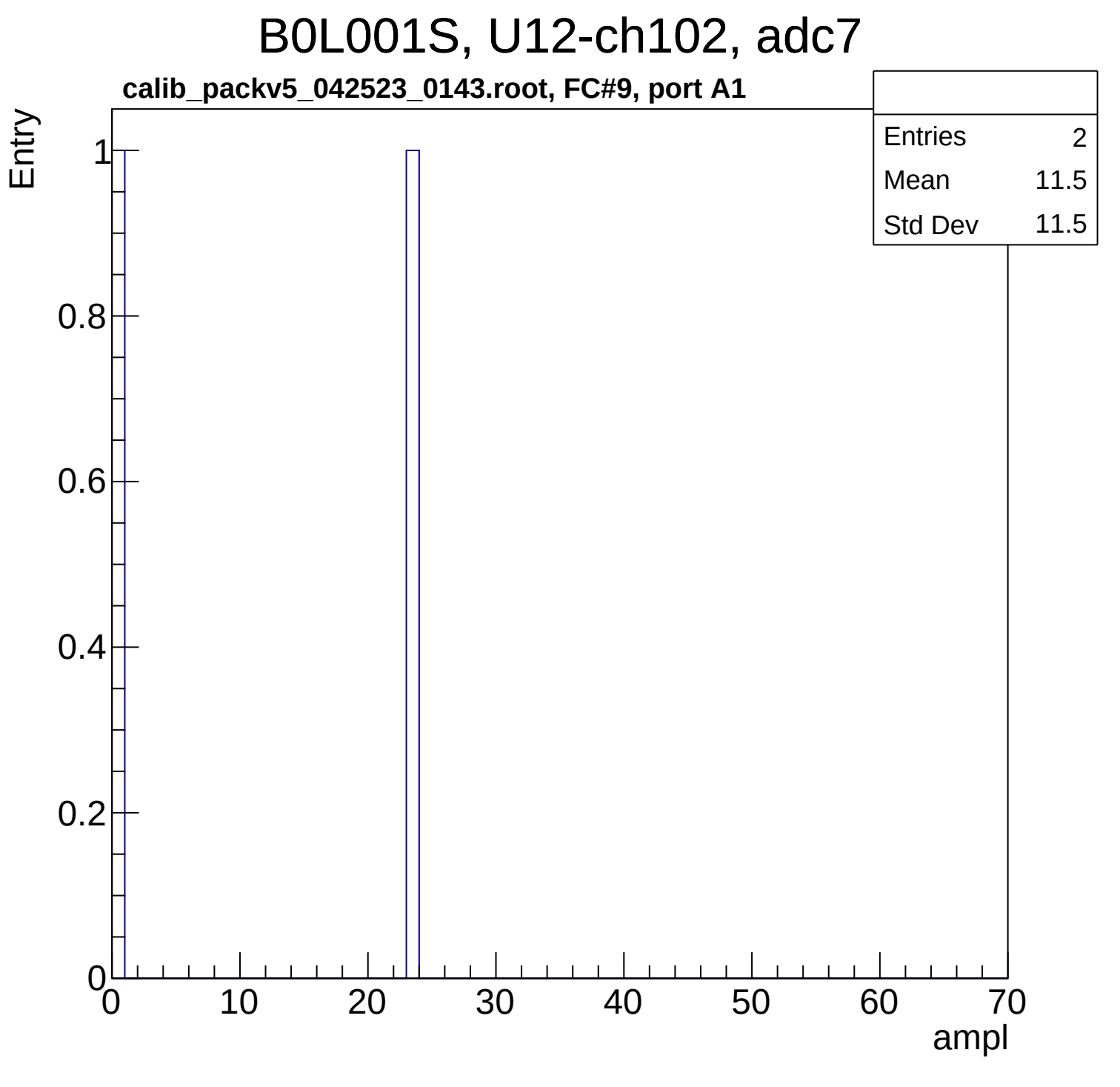
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B0L001S, U12-ch102, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 11.5
Std Dev 11.5
Entry
ampl
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0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
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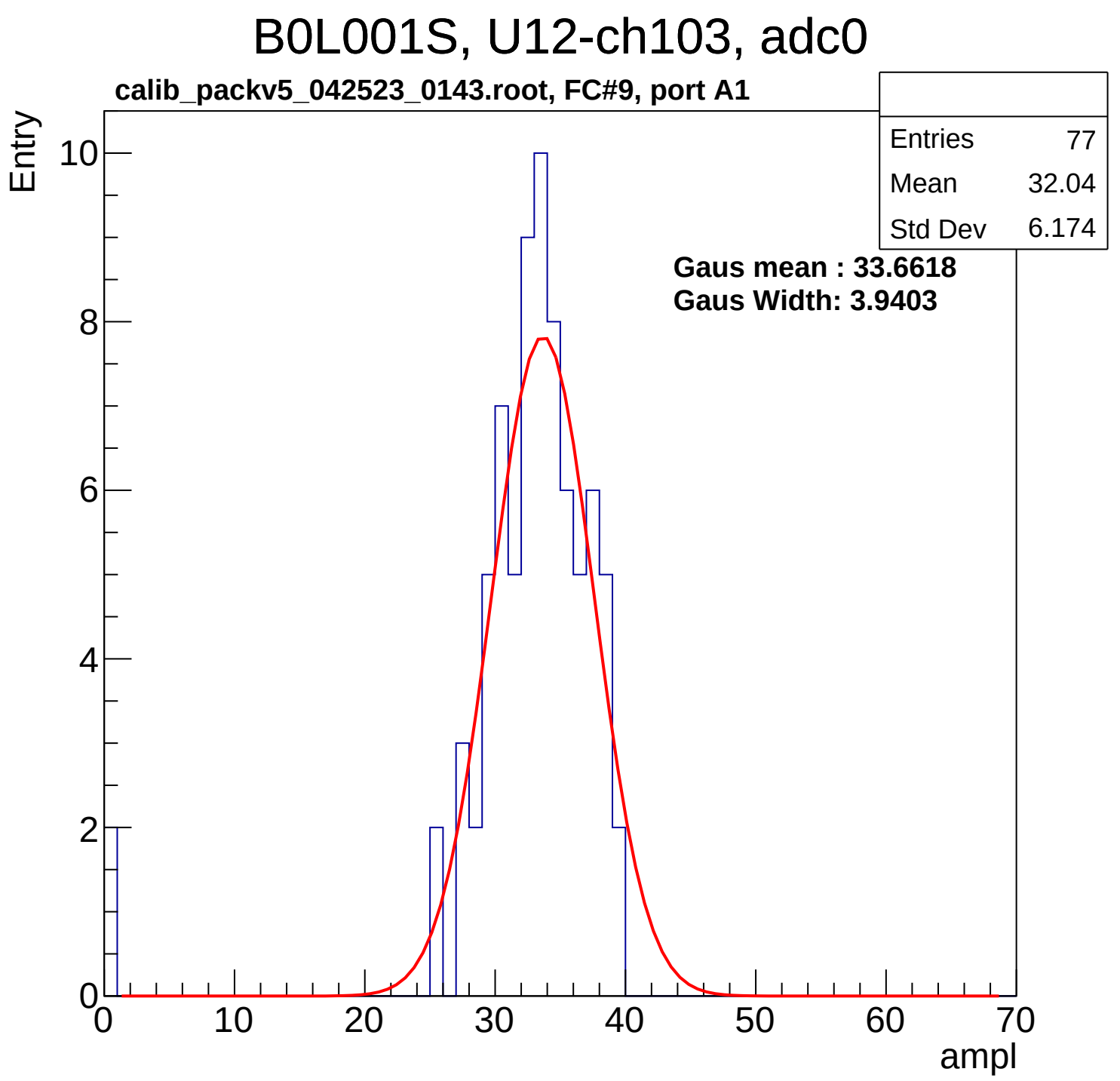
B0L001S, U12-ch103, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 77
Mean 32.04
Std Dev 6.174
Gaus mean : 33.6618
Gaus Width: 3.9403
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
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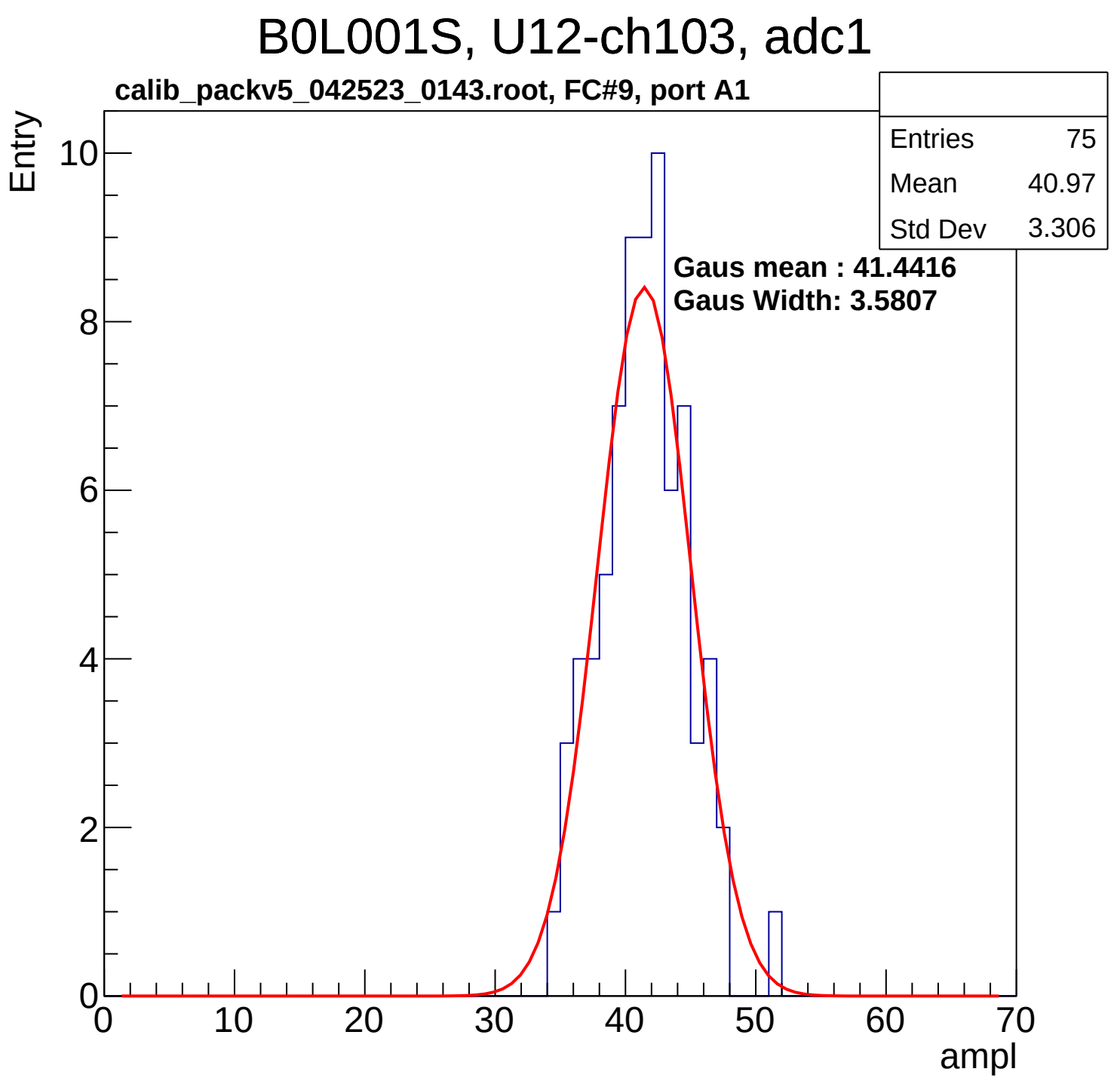
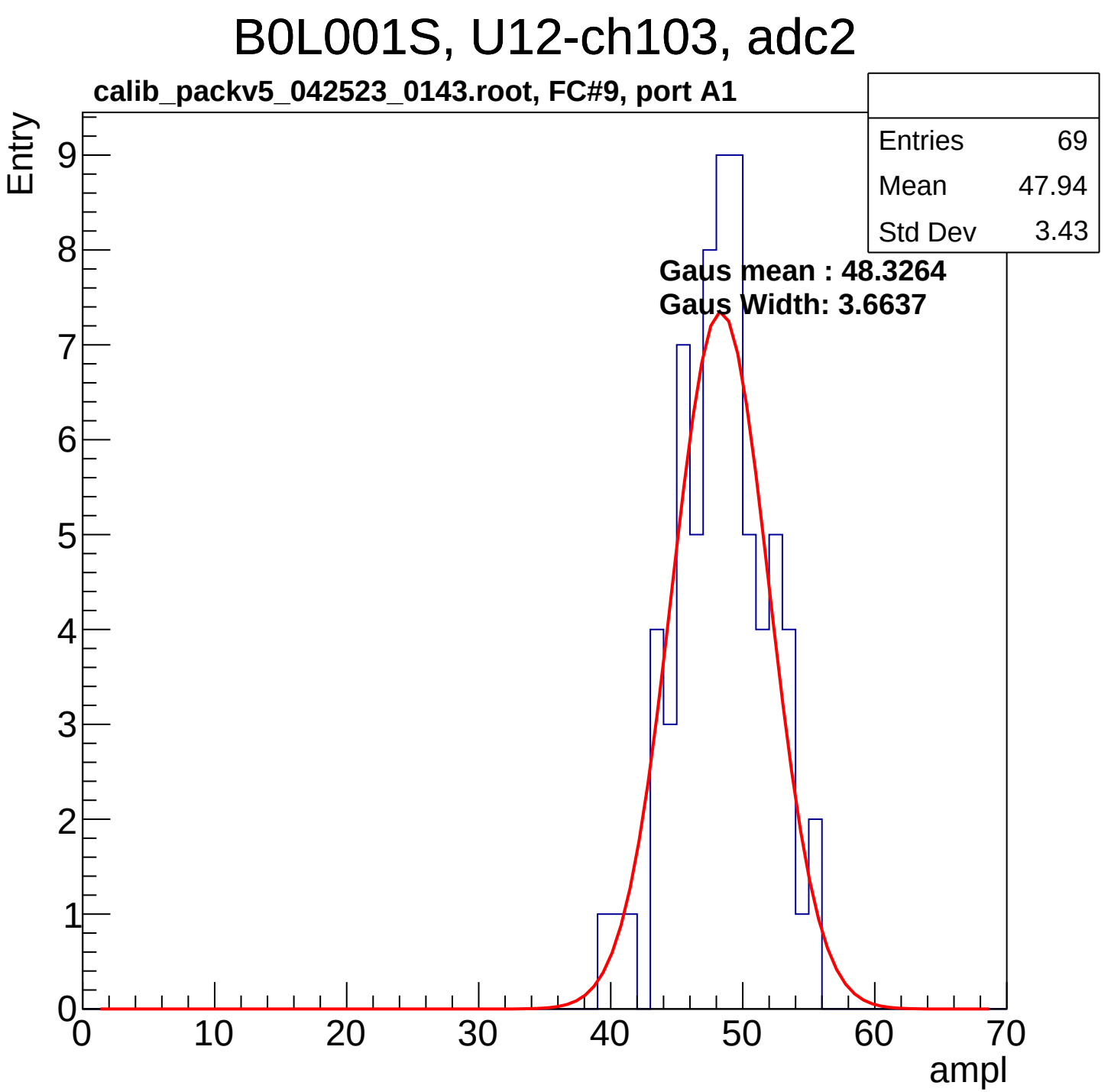
60
70


B0L001S, U12-ch103, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 75
Mean 40.97
Std Dev 3.306
Gaus mean : 41.4416
Gaus Width: 3.5807
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch103, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 69
Mean 47.94
Std Dev 3.43
Gaus mean : 48.3264
Gaus Width: 3.6637
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
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30
40
50
60
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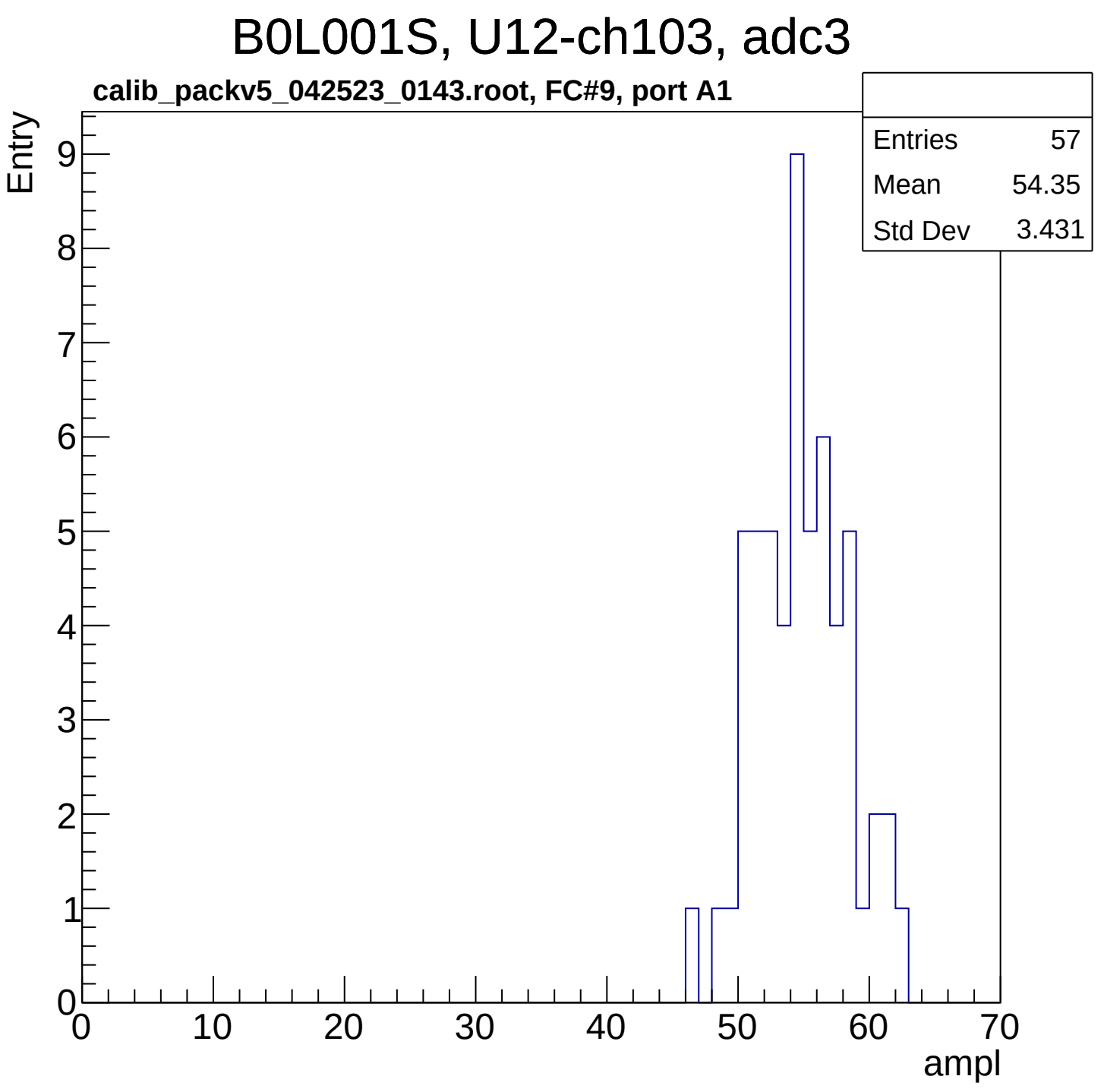
B0L001S, U12-ch103, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 57
Mean 54.35
Std Dev 3.431
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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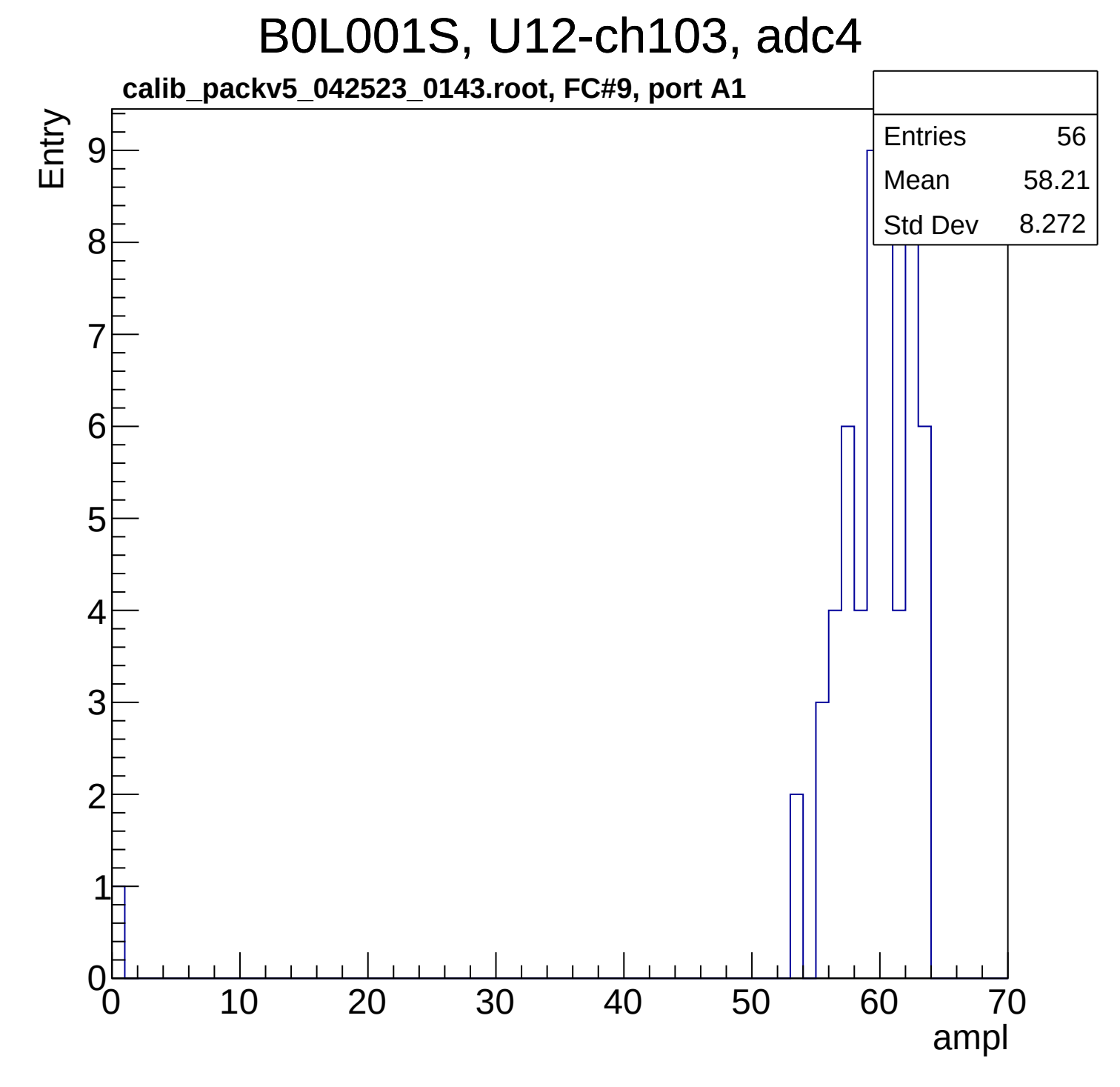
B0L001S, U12-ch103, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 56
Mean 58.21
Std Dev 8.272
Entry
ampl
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2
3
4
5
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7
8
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20
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40
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60
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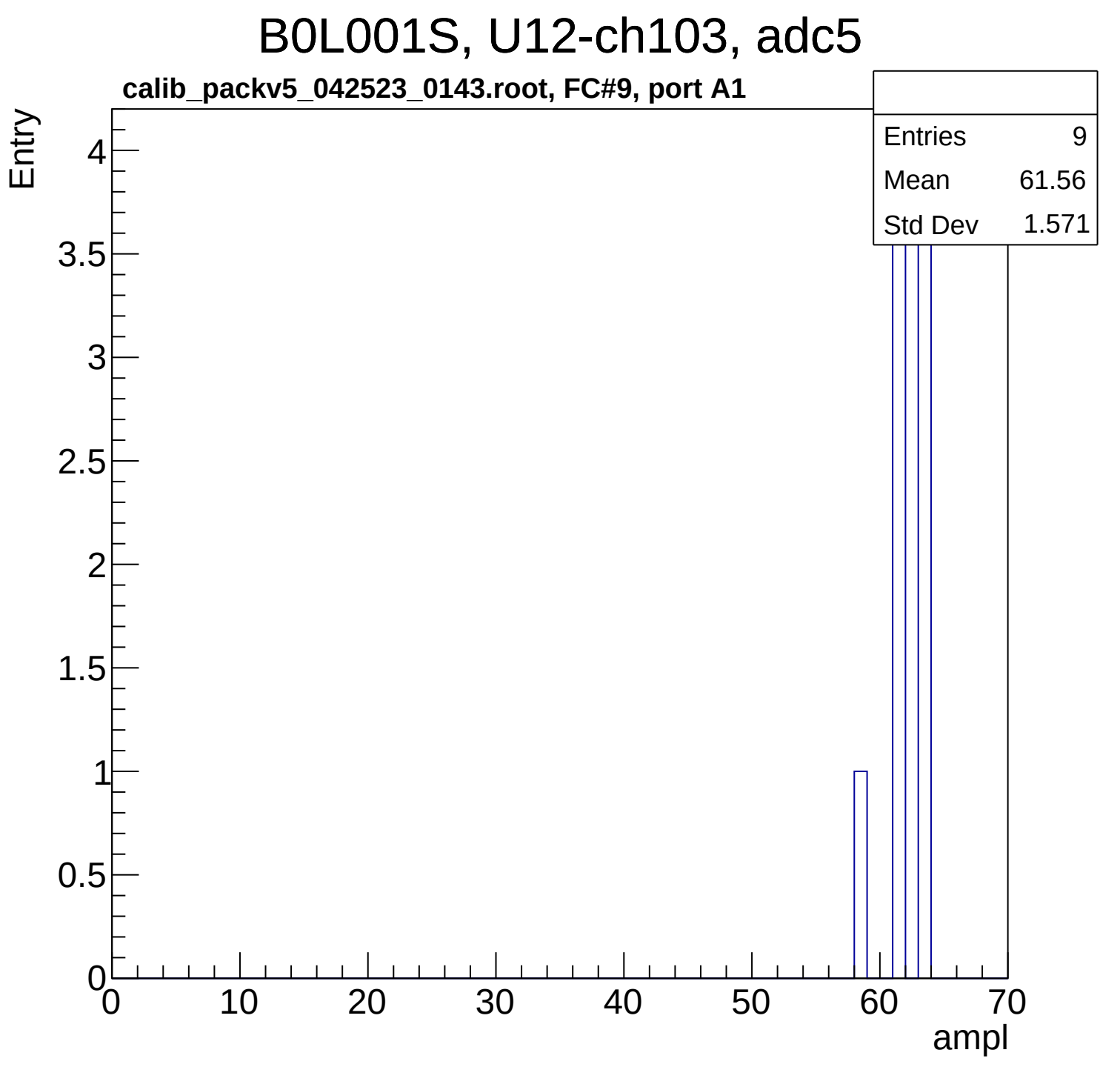
B0L001S, U12-ch103, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 9
Mean 61.56
Std Dev 1.571
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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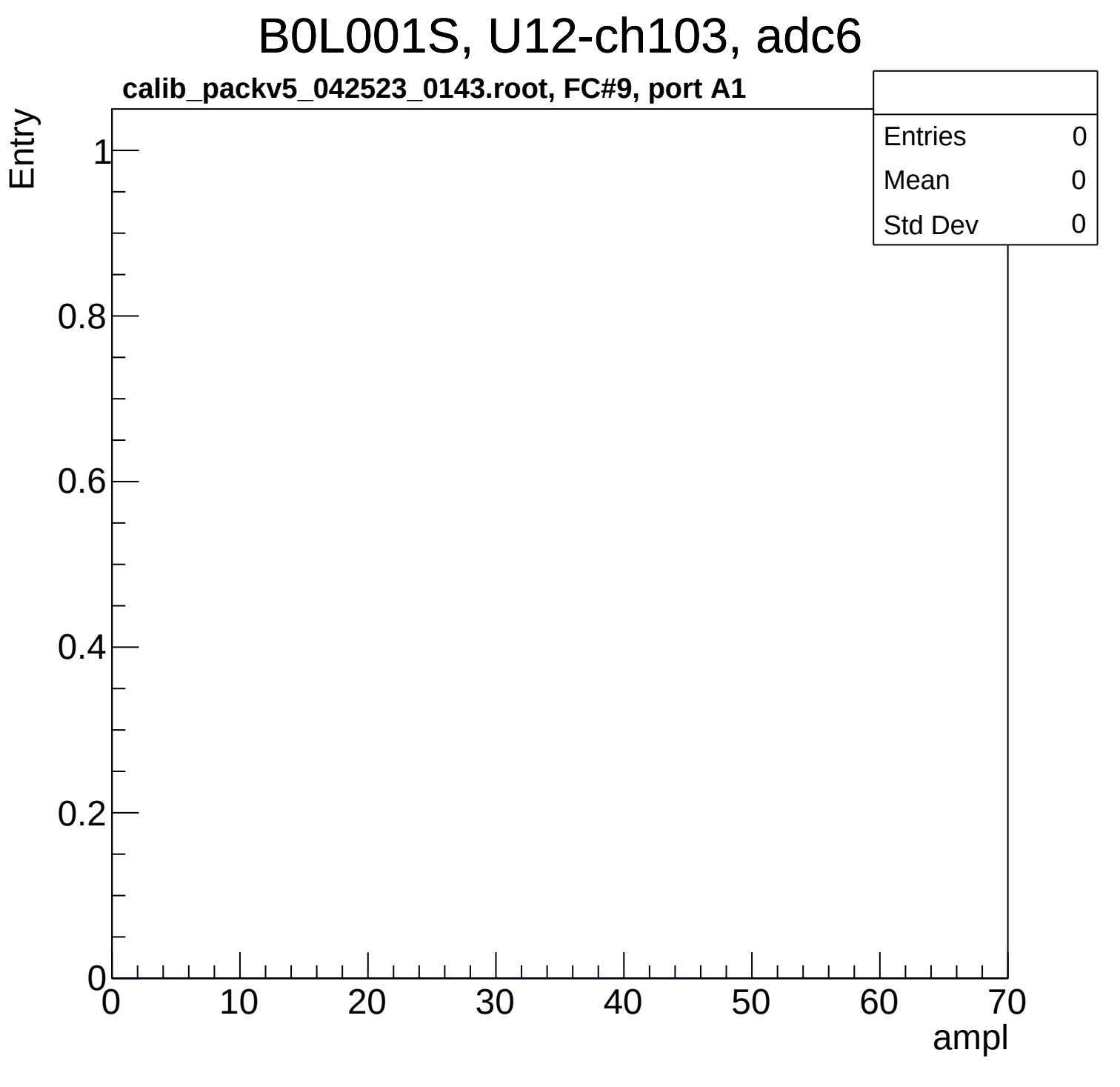
B0L001S, U12-ch103, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
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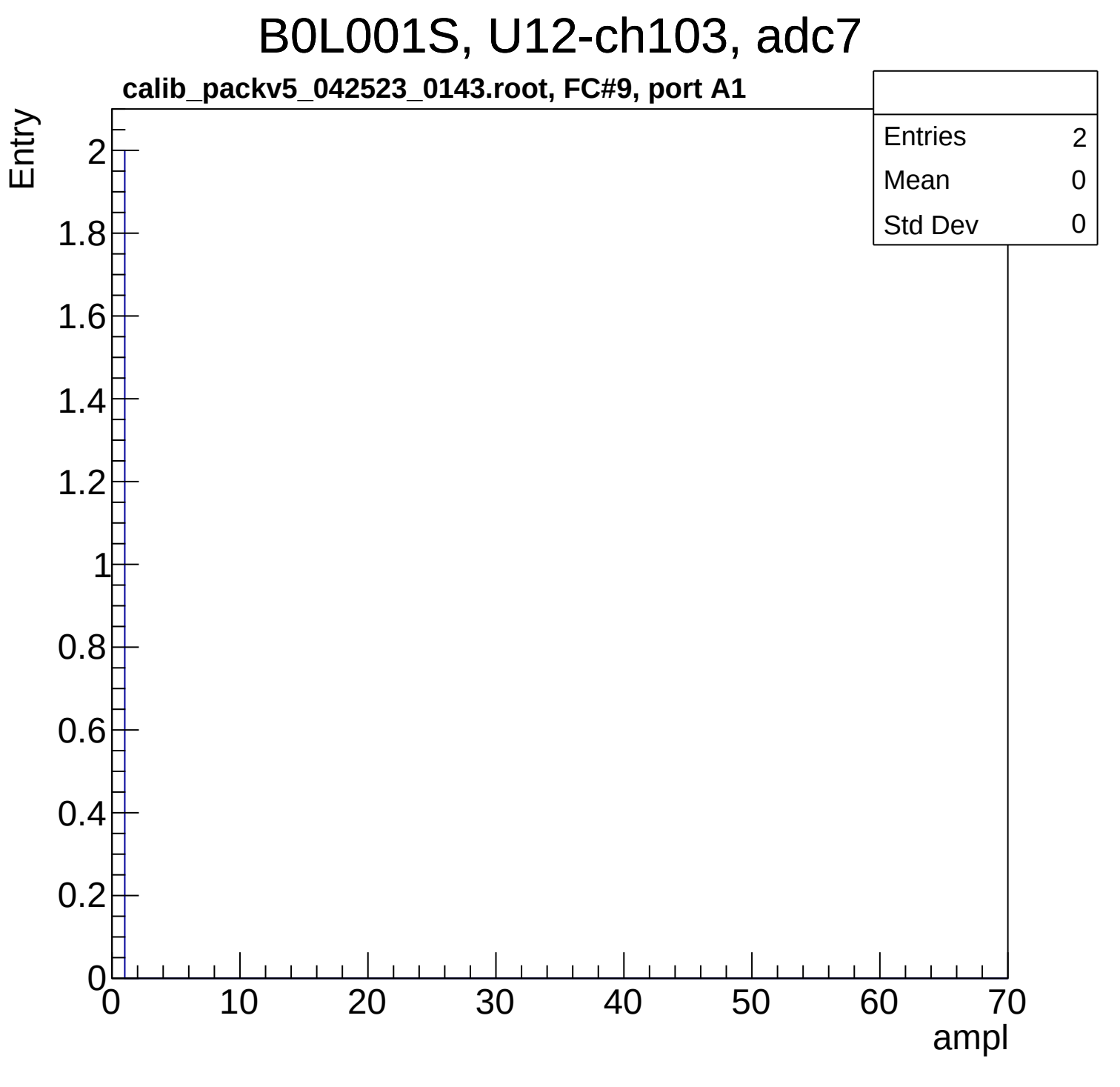
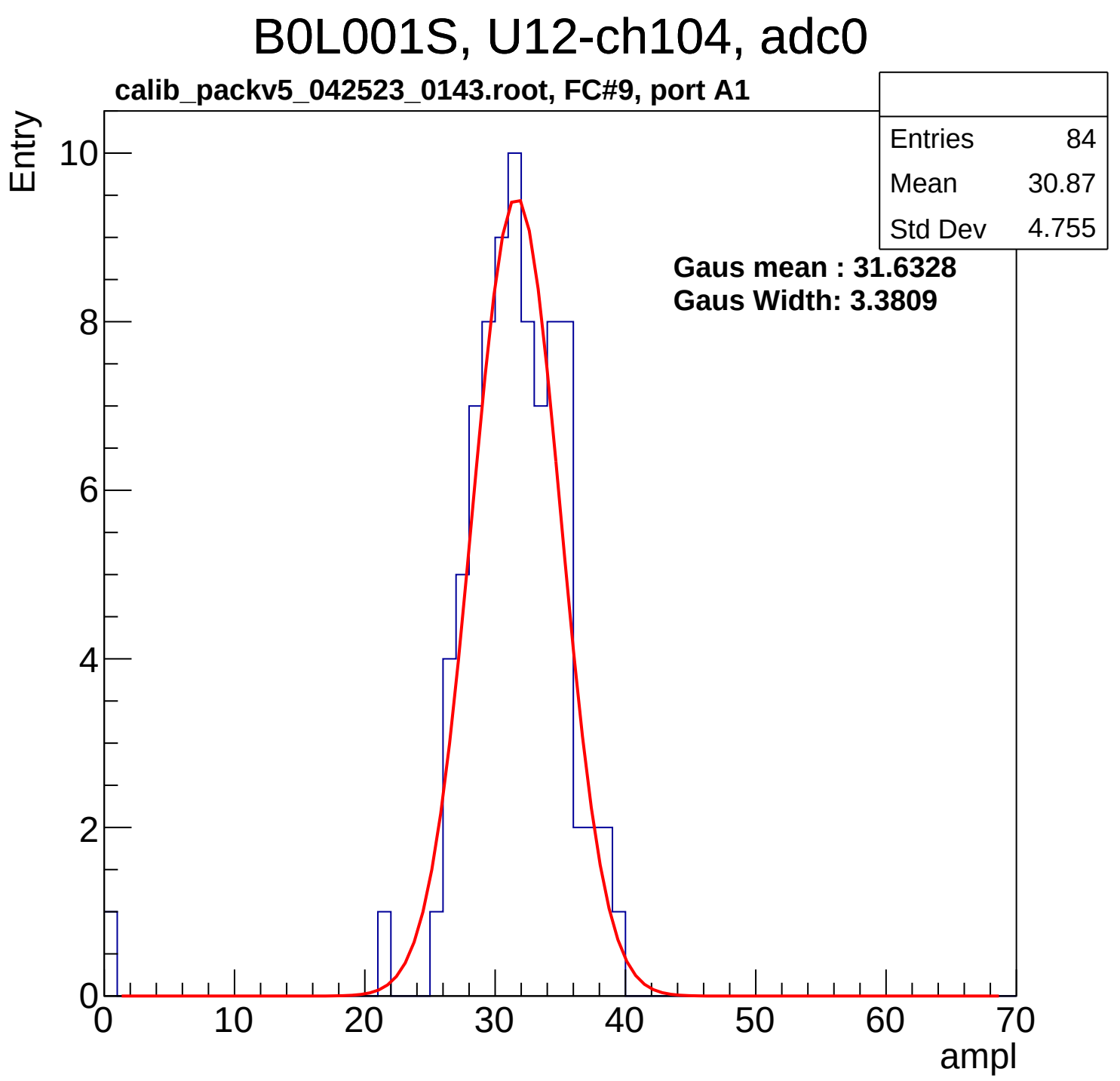
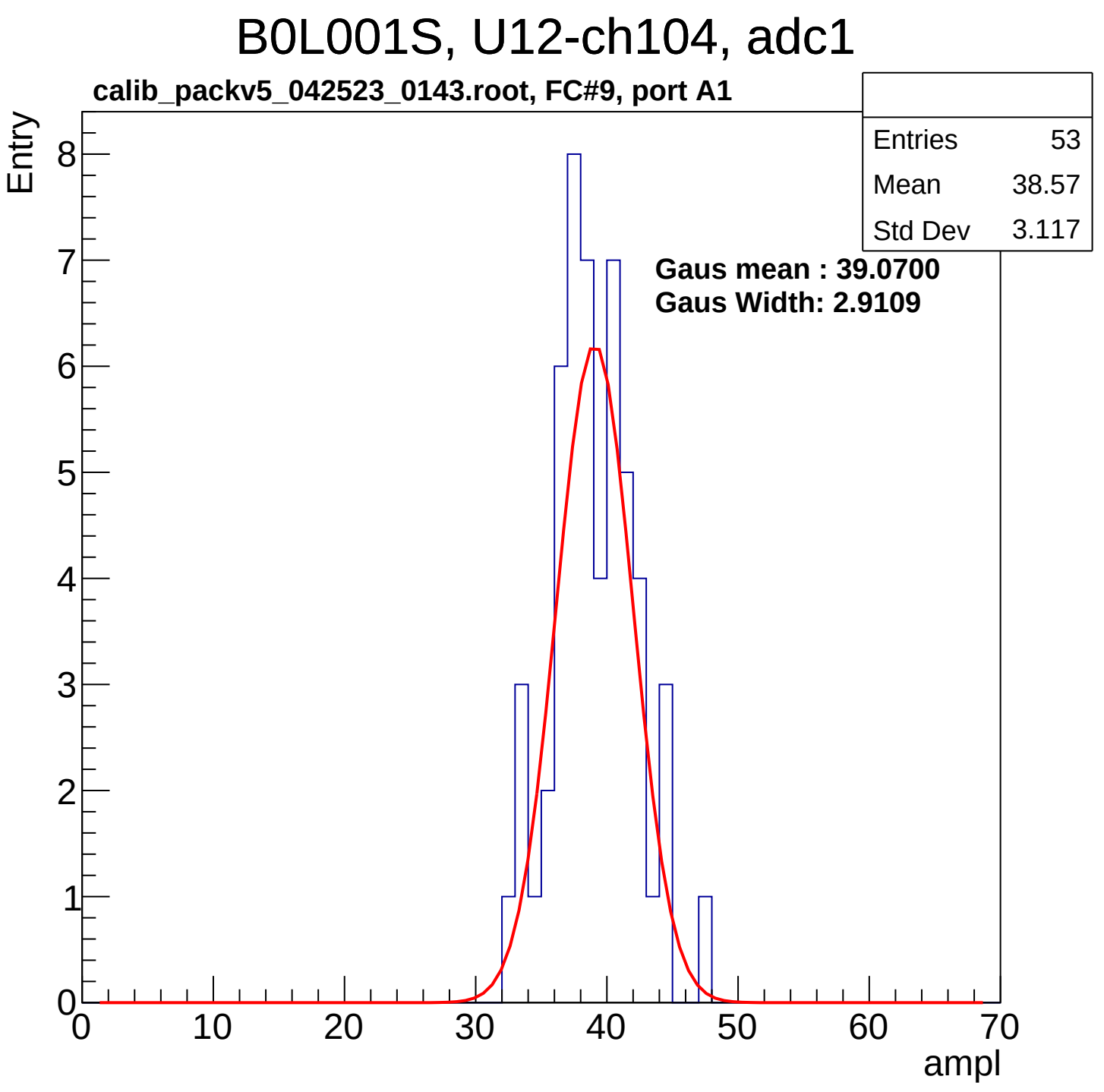
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch103, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch104, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 84
Mean 30.87
Std Dev 4.755
Gaus mean : 31.6328
Gaus Width: 3.3809
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch104, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 53
Mean 38.57
Std Dev 3.117
Gaus mean : 39.0700
Gaus Width: 2.9109
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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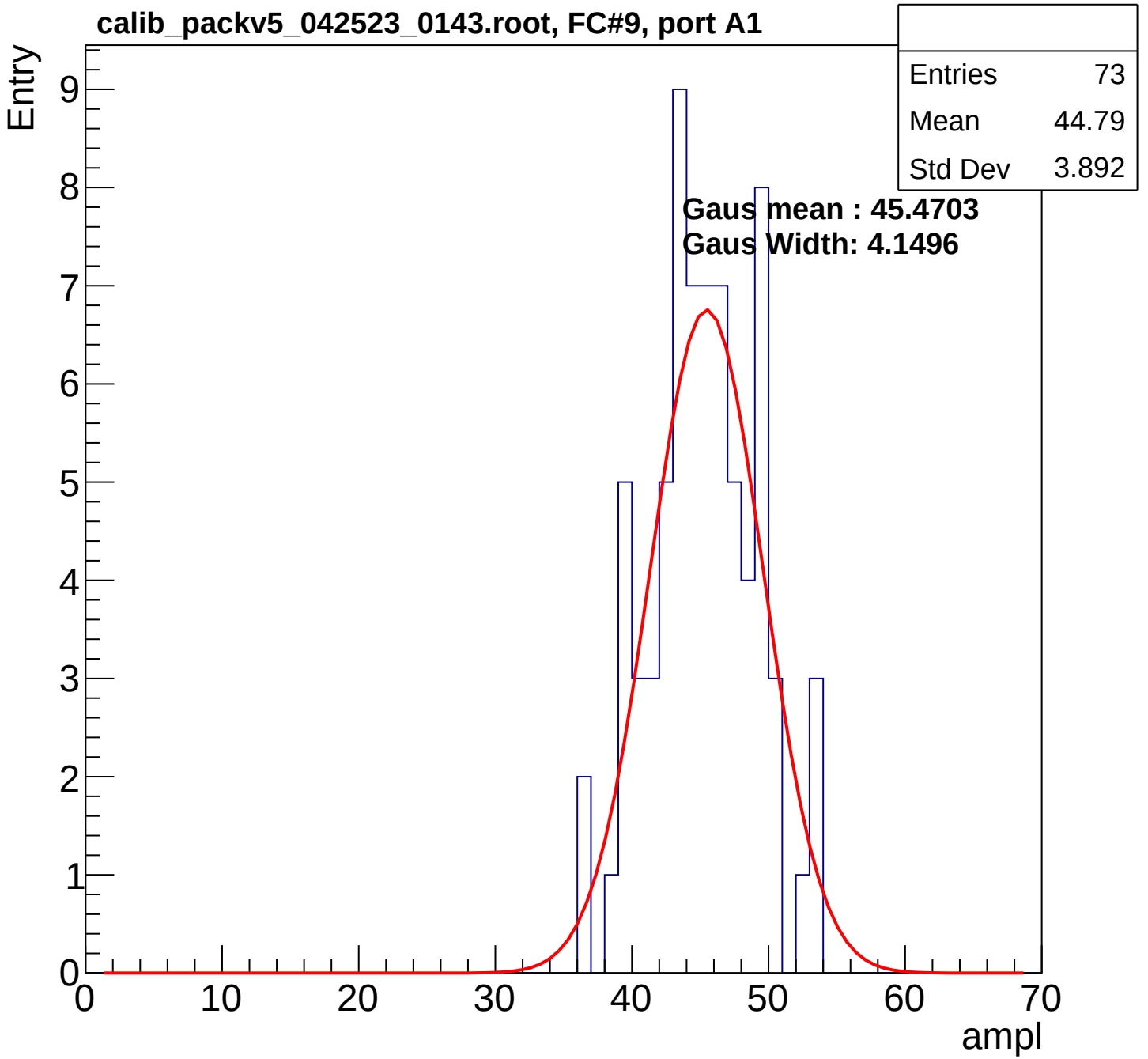
B0L001S, U12-ch104, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 73
Mean 44.79
Std Dev 3.892
Gaus mean : 45.4703
Gaus Width: 4.1496
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
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60
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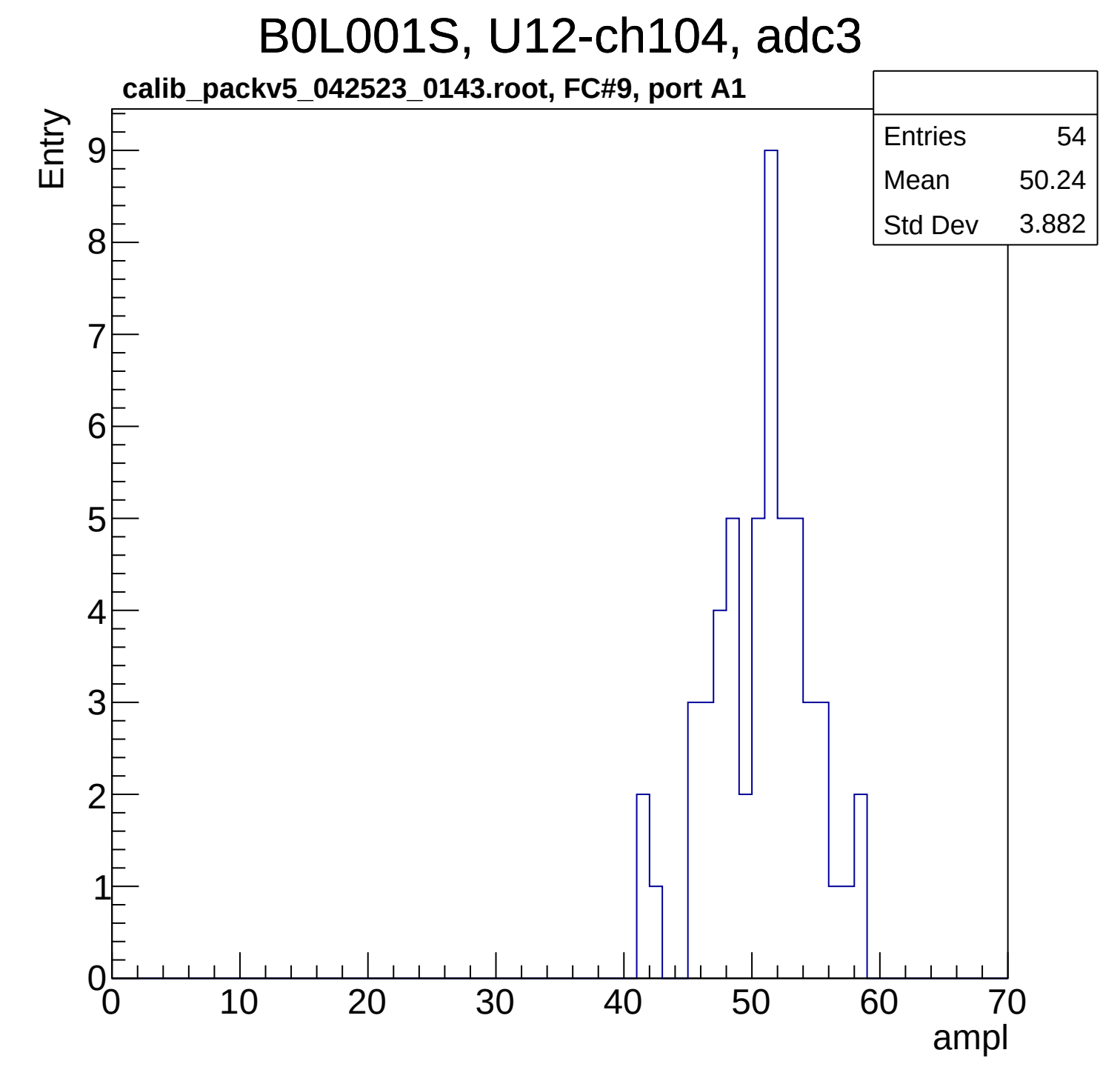
B0L001S, U12-ch104, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 54
Mean 50.24
Std Dev 3.882
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
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40
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60
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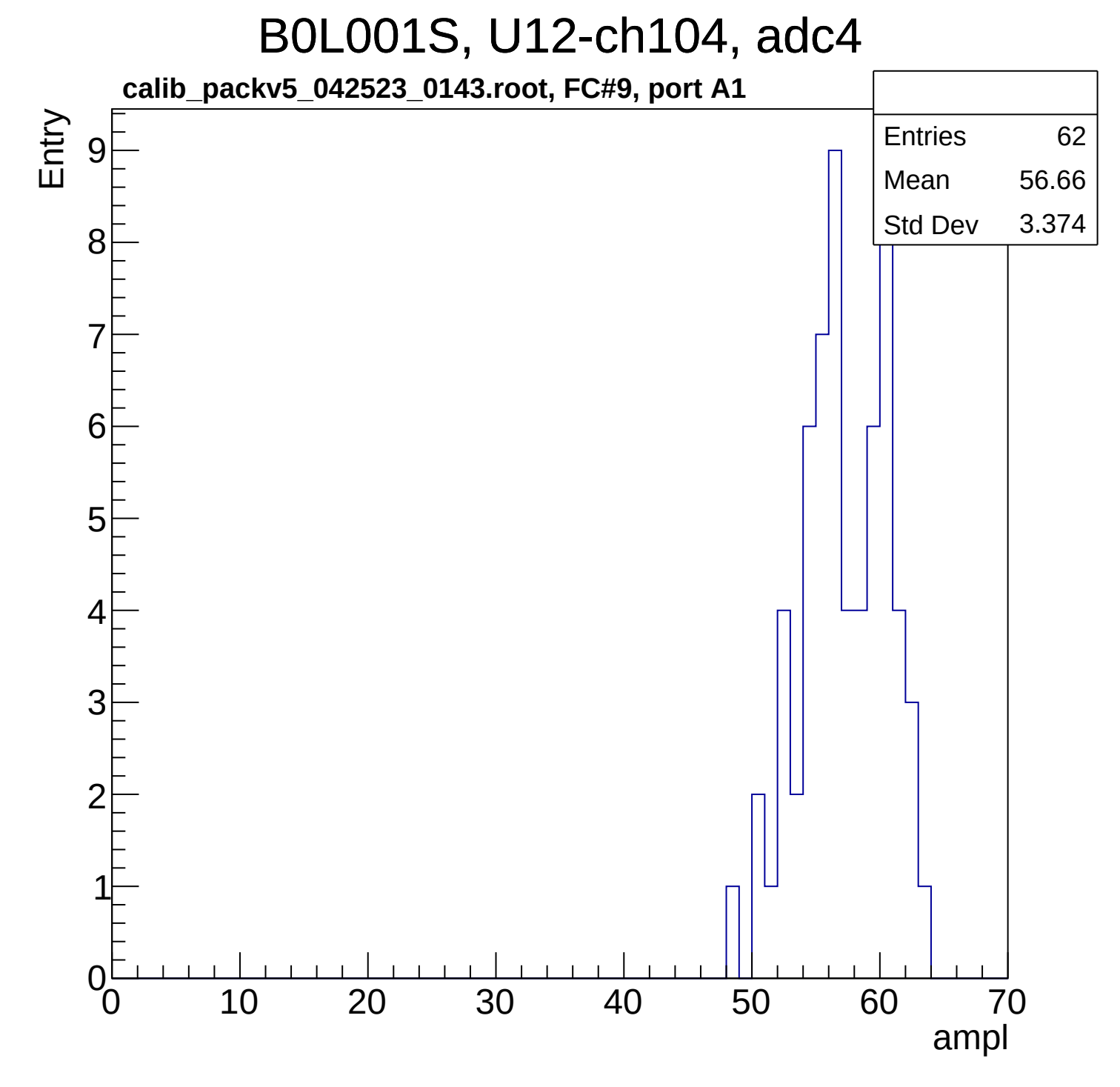
B0L001S, U12-ch104, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 62
Mean 56.66
Std Dev 3.374
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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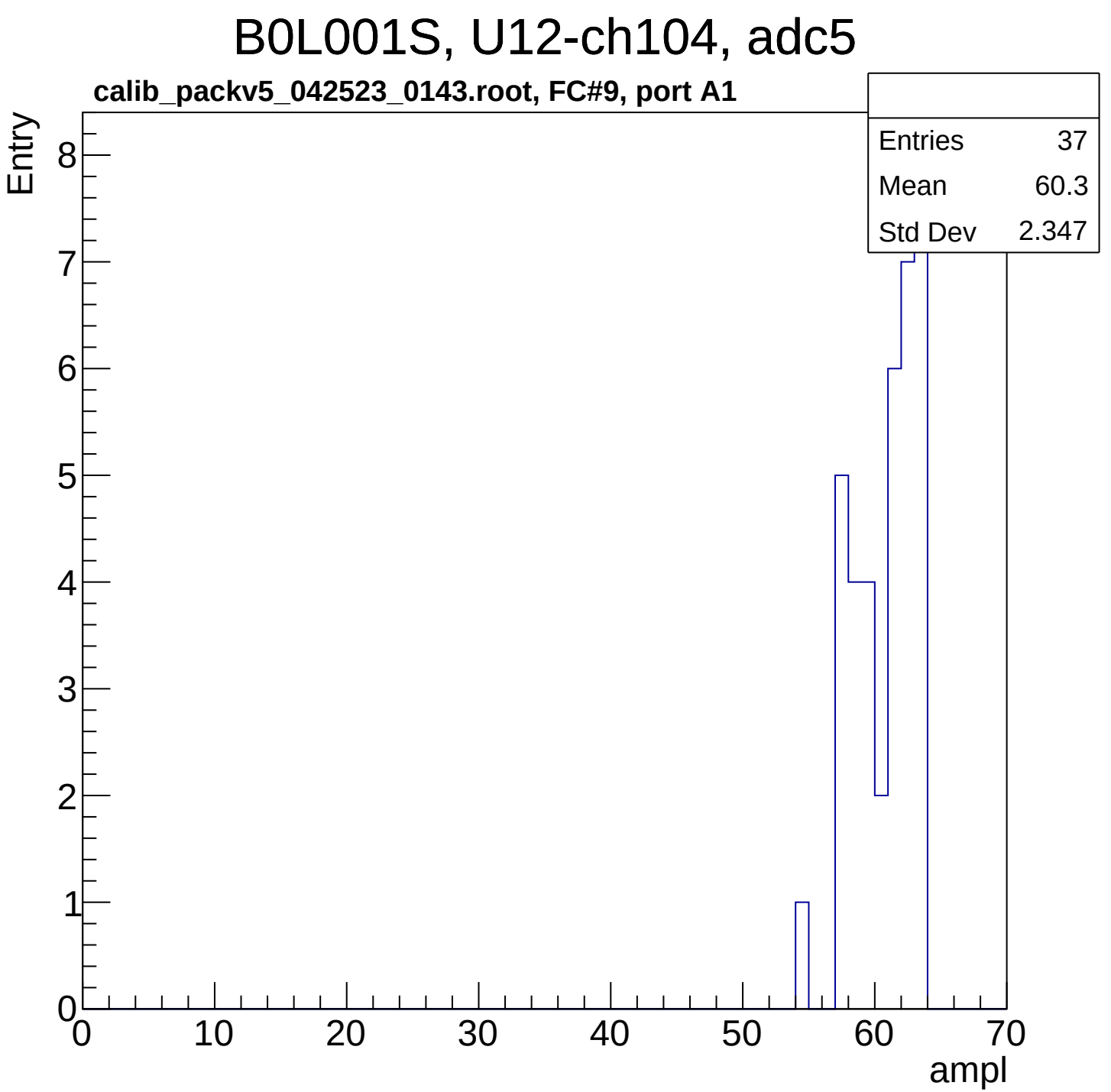
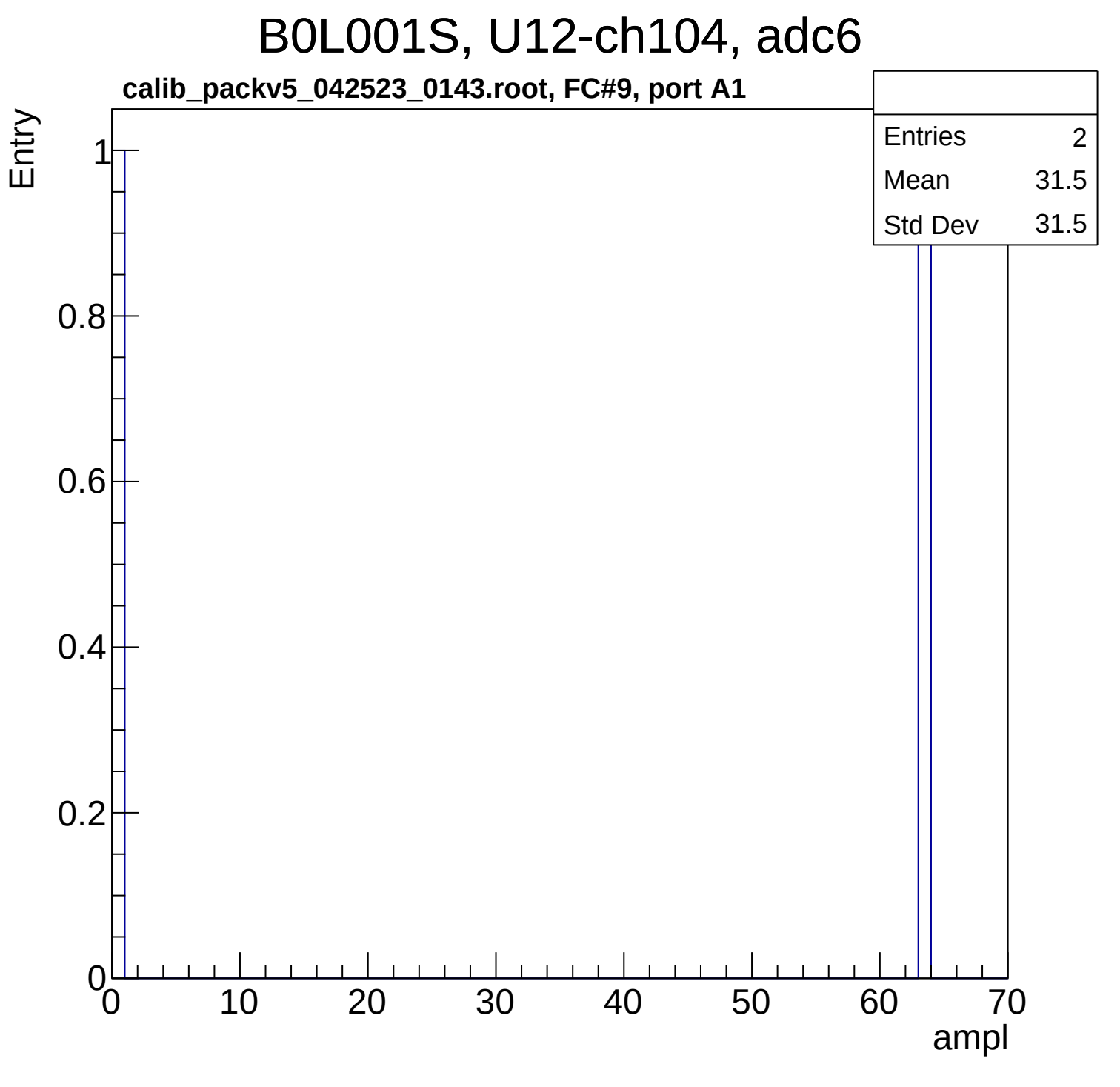
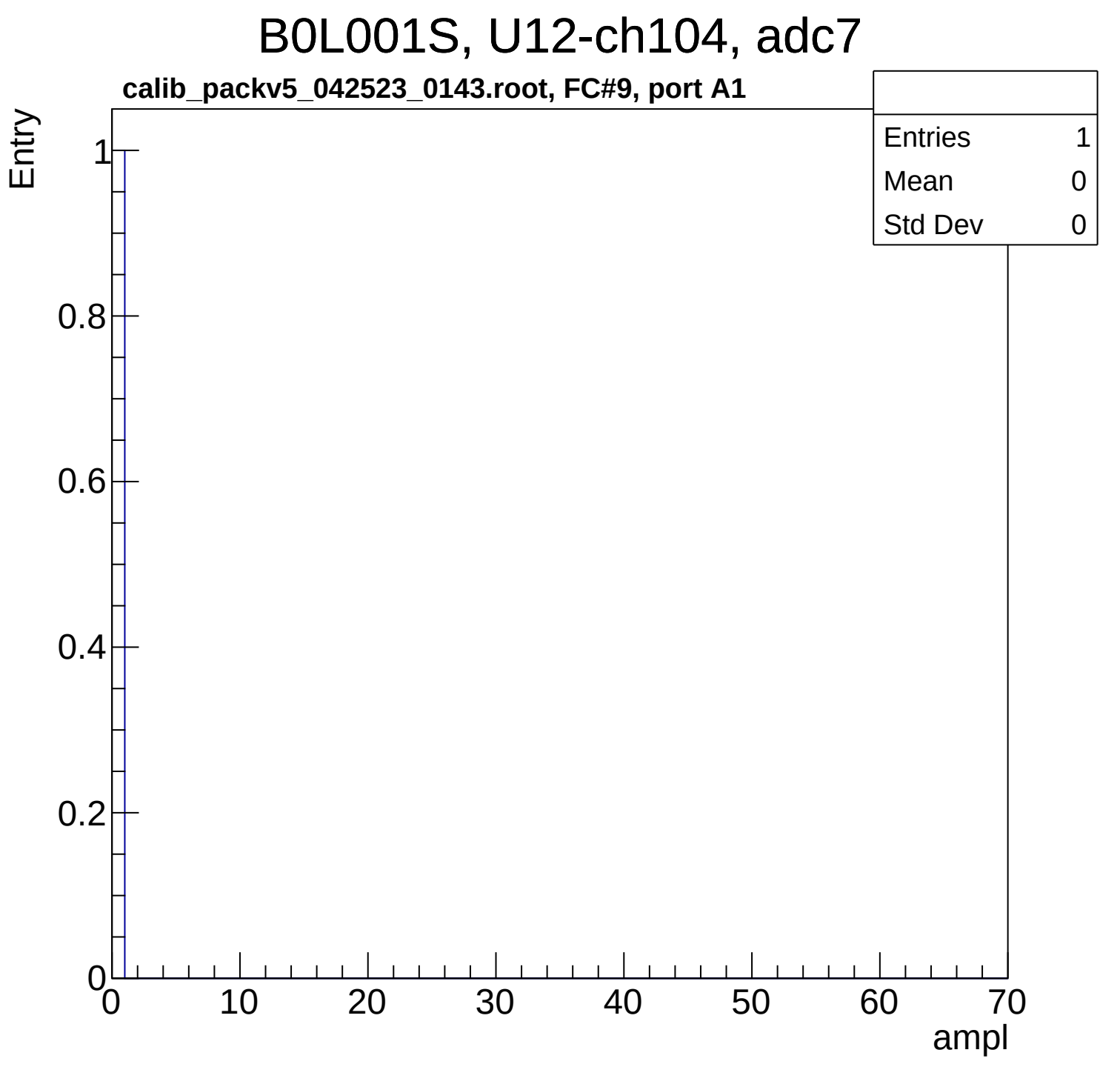
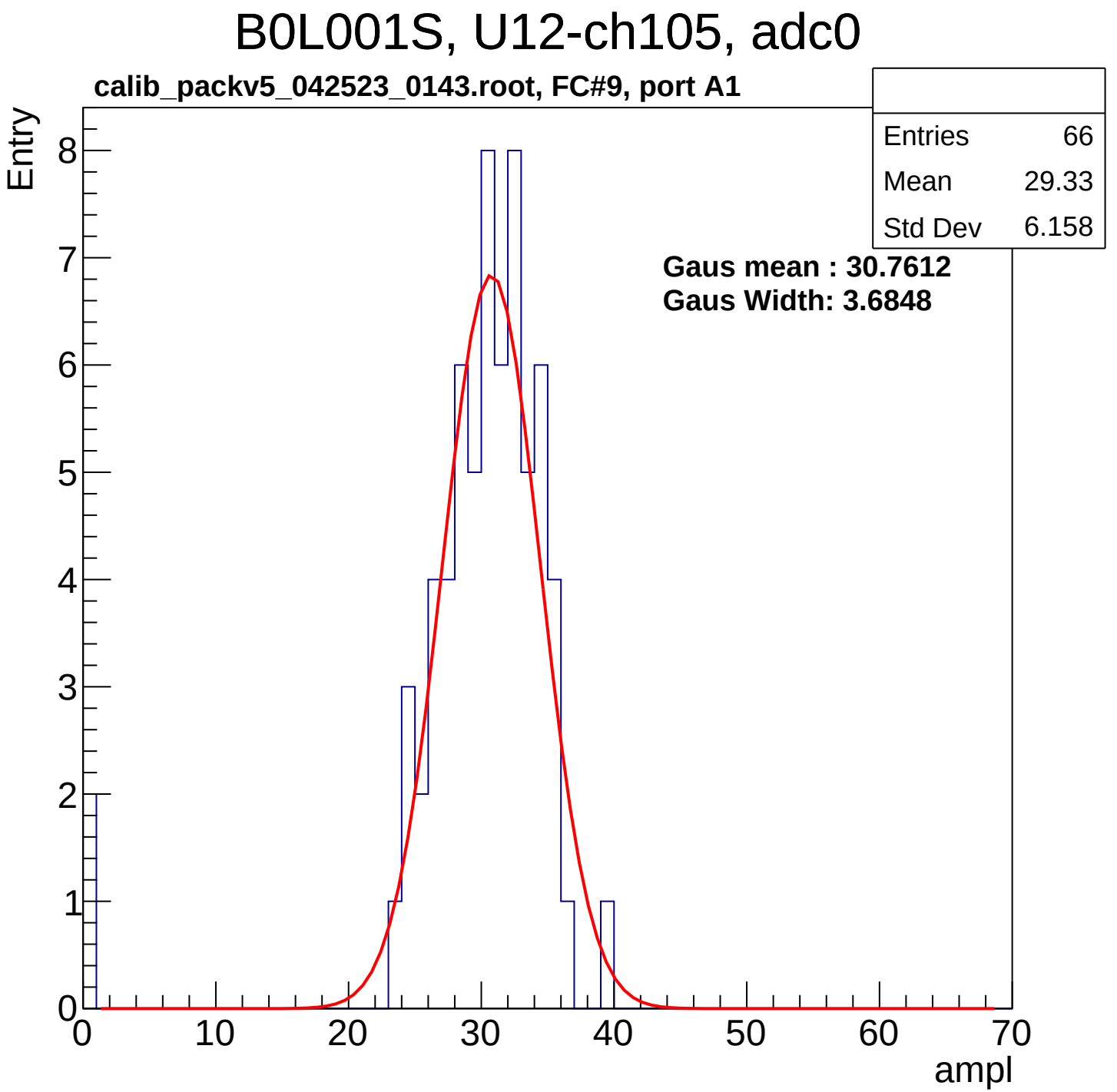
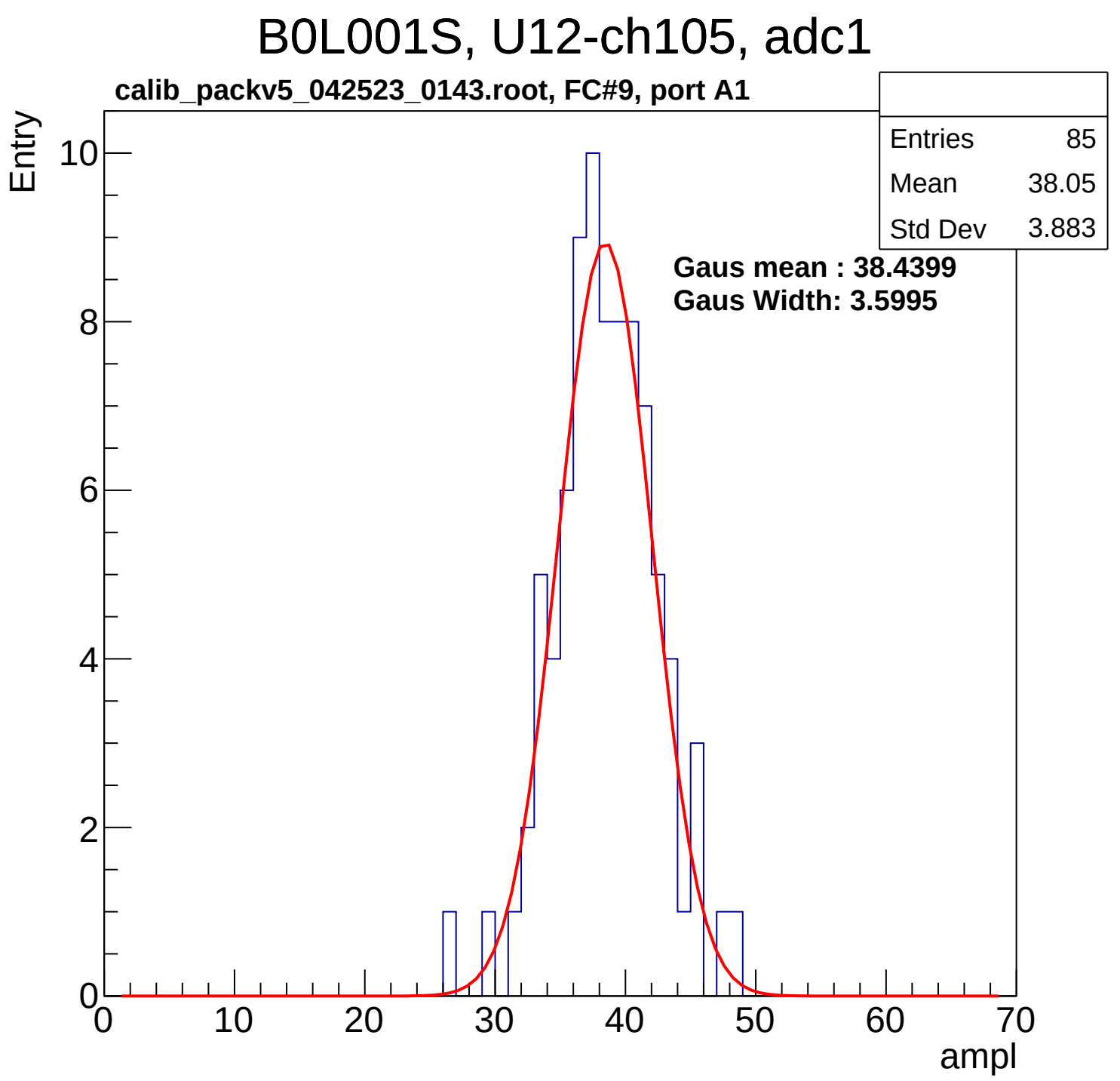
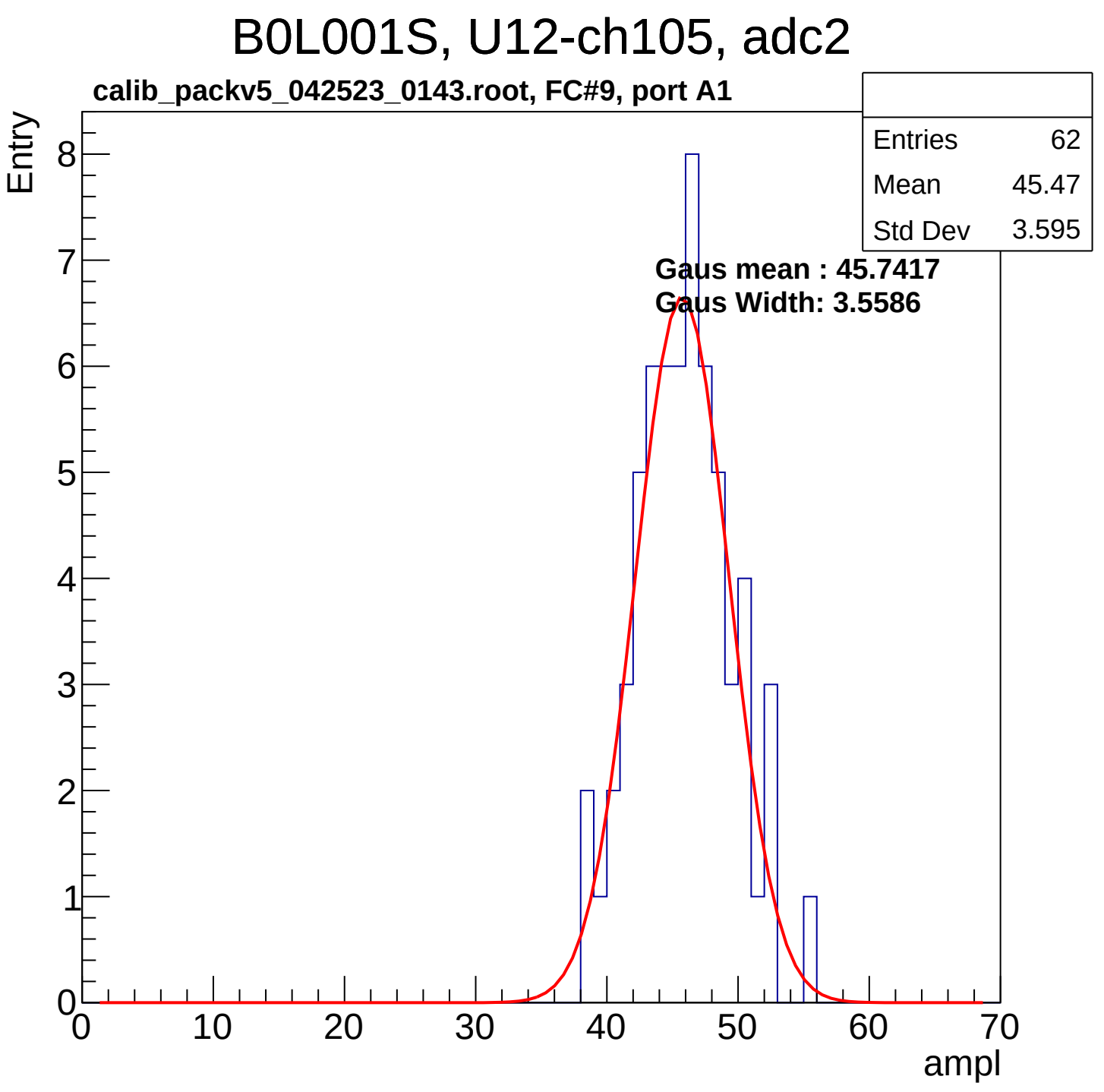

B0L001S, U12-ch104, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 37
Mean 60.3
Std Dev 2.347
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch104, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch104, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch105, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 66
Mean 29.33
Std Dev 6.158
Gaus mean : 30.7612
Gaus Width: 3.6848
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch105, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 85
Mean 38.05
Std Dev 3.883
Gaus mean : 38.4399
Gaus Width: 3.5995
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch105, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 62
Mean 45.47
Std Dev 3.595
Gaus mean : 45.7417
Gaus Width: 3.5586
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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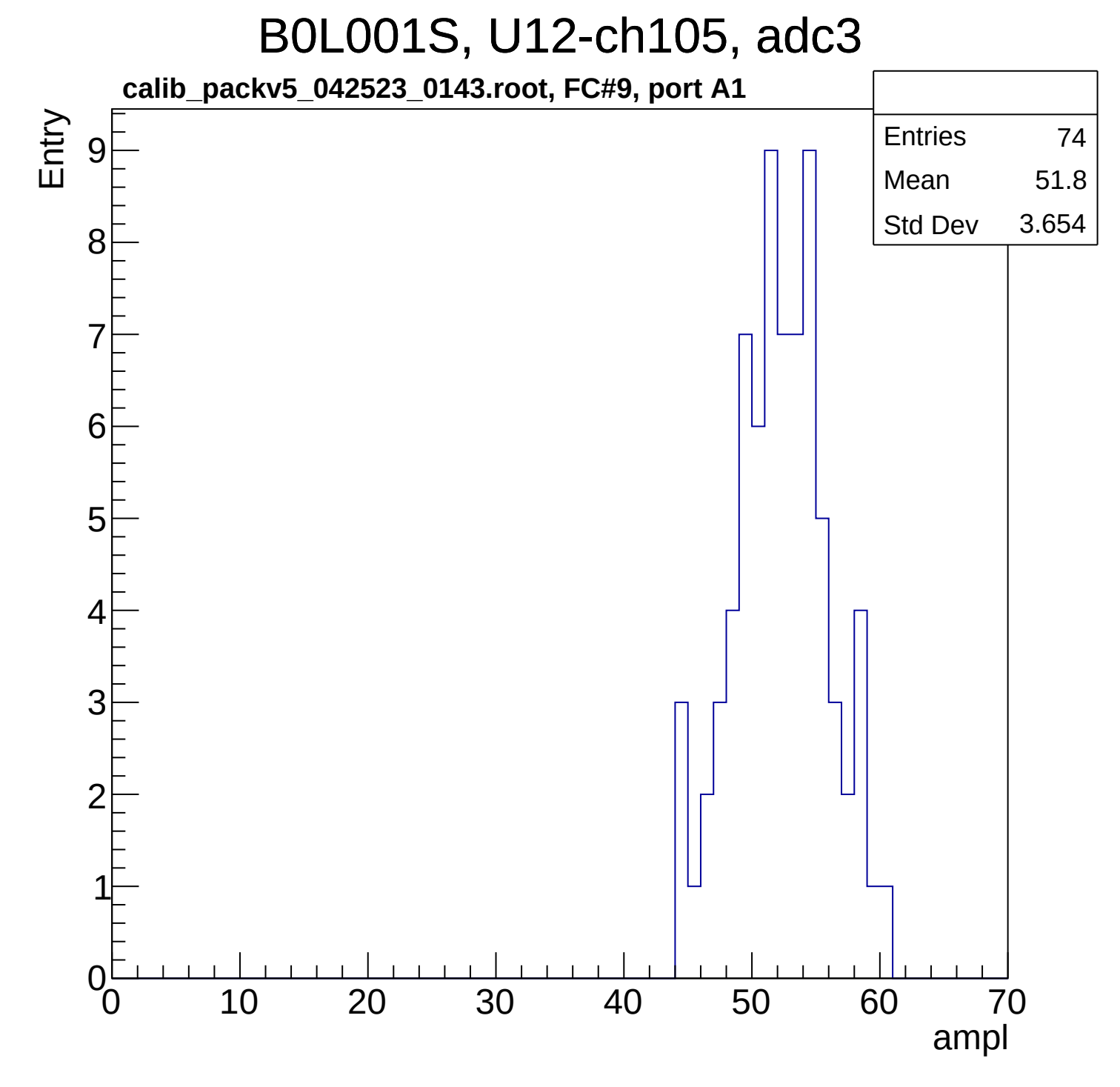
B0L001S, U12-ch105, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 74
Mean 51.8
Std Dev 3.654
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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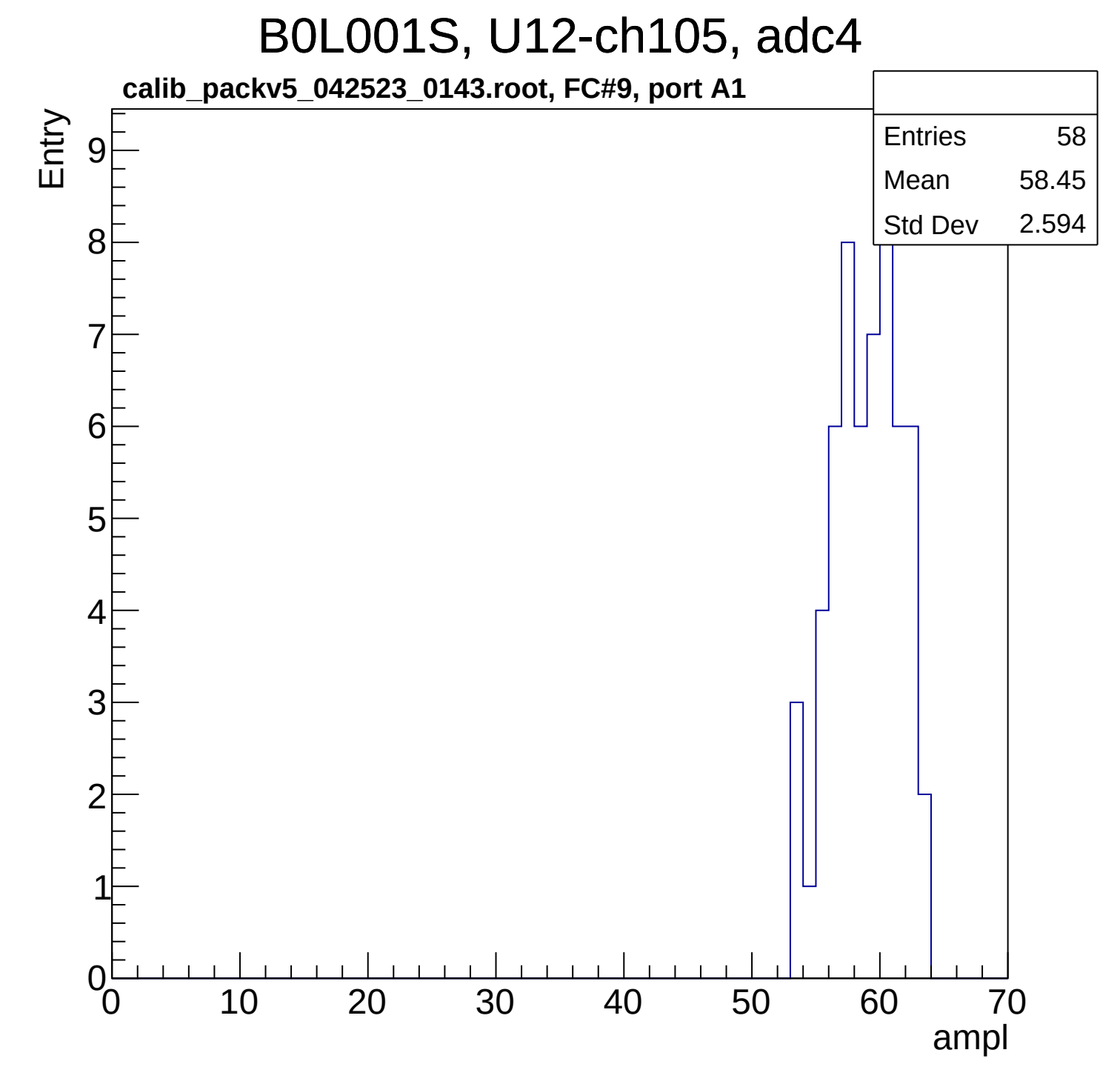
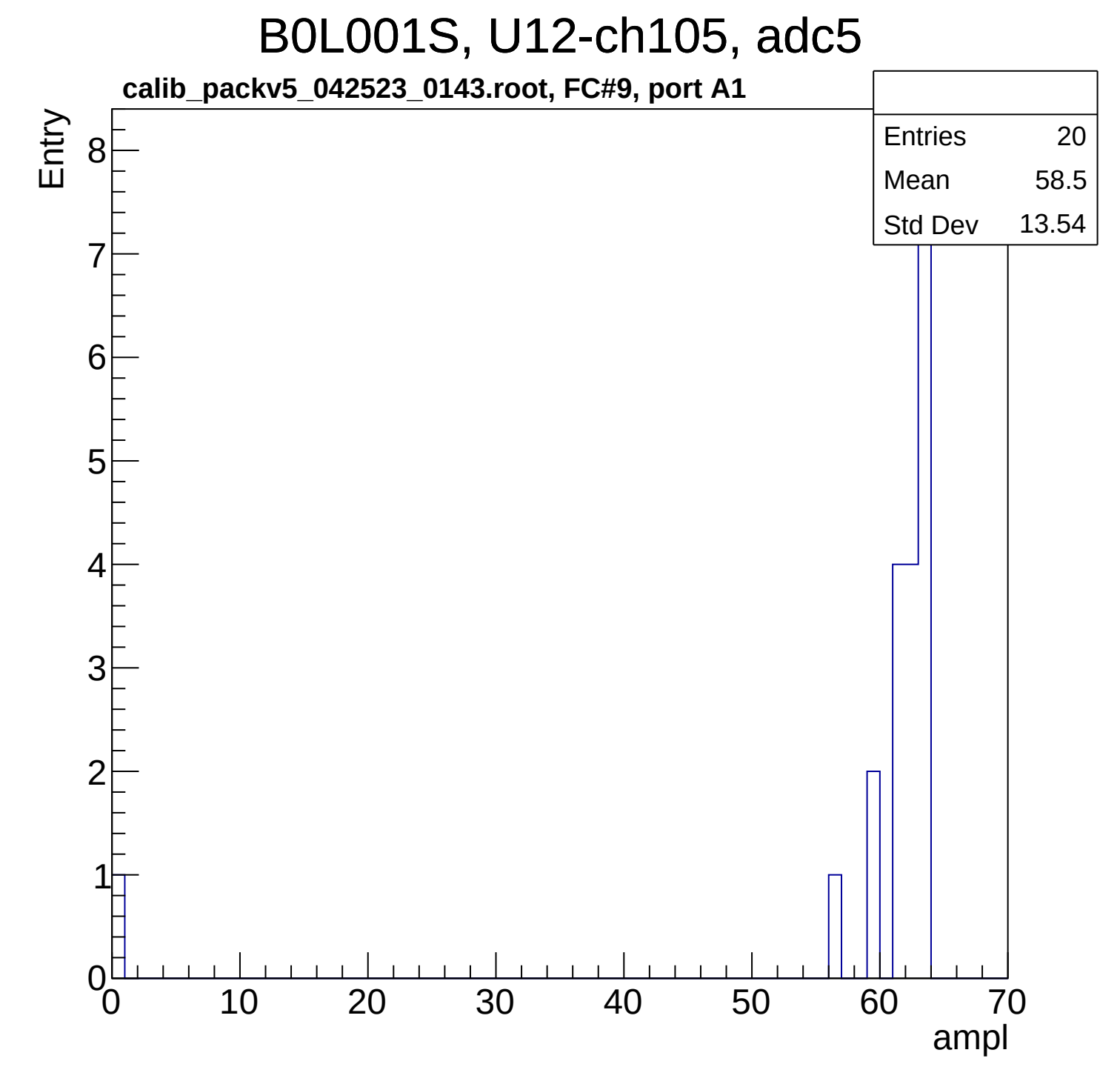
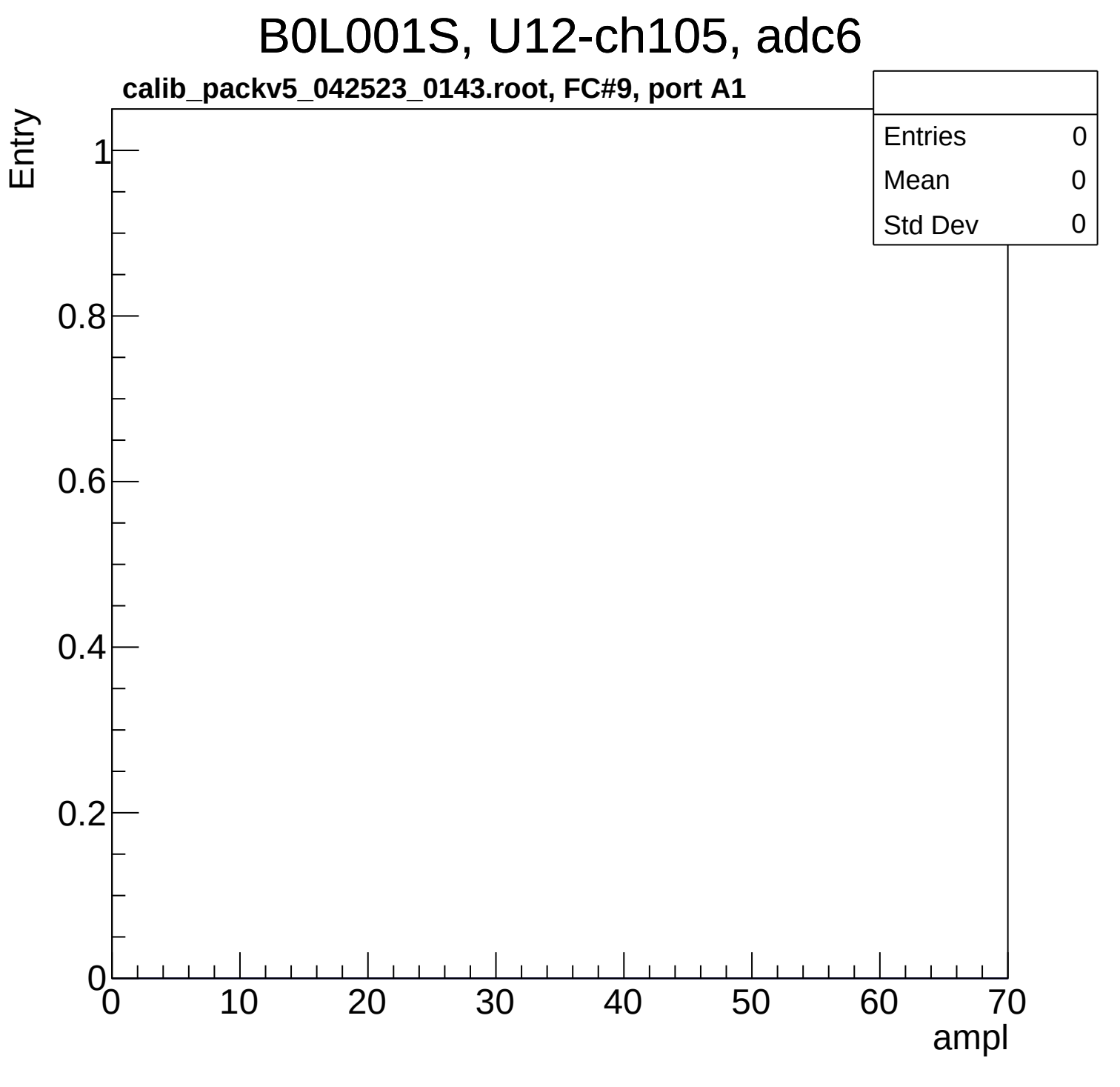
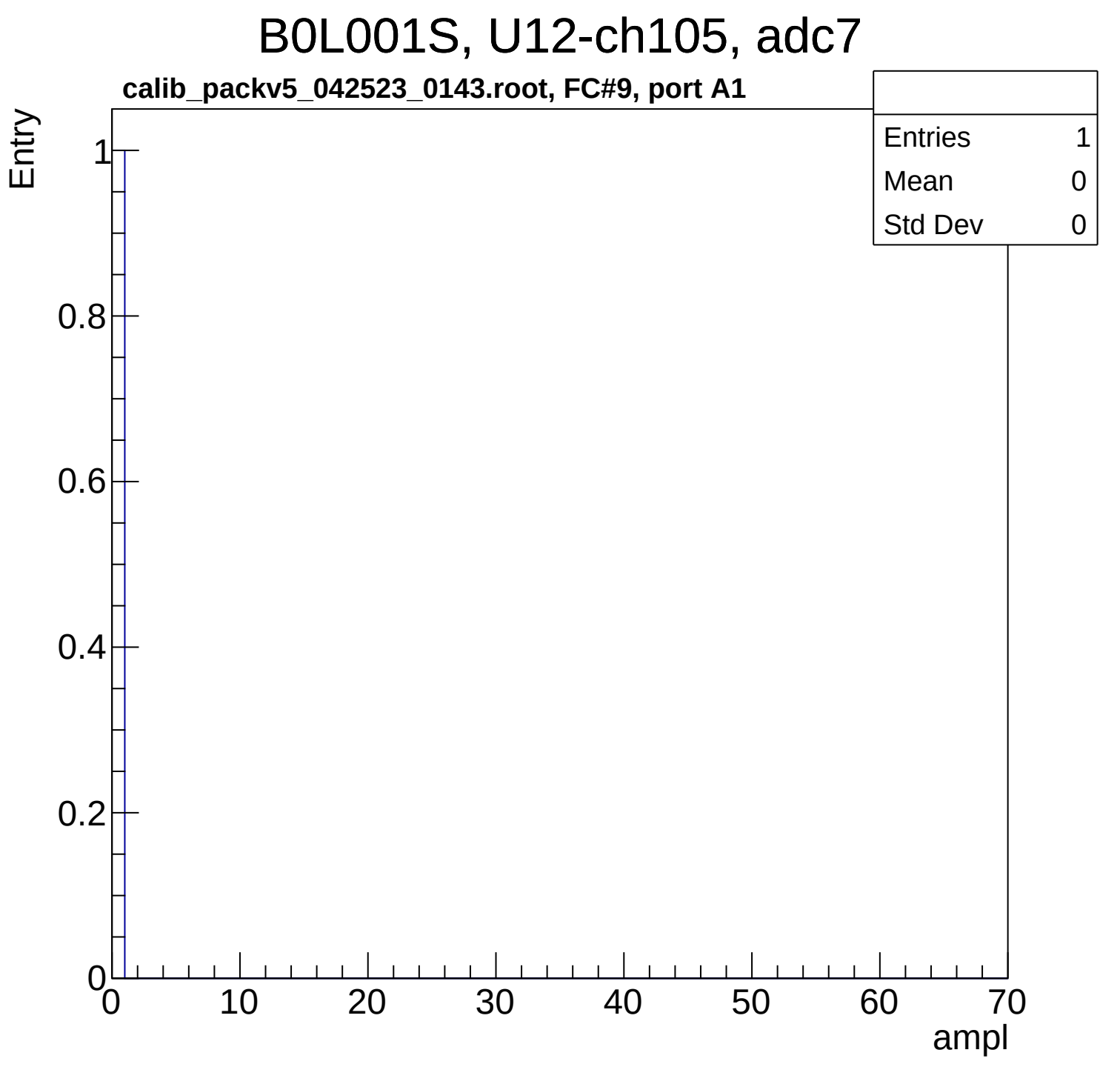
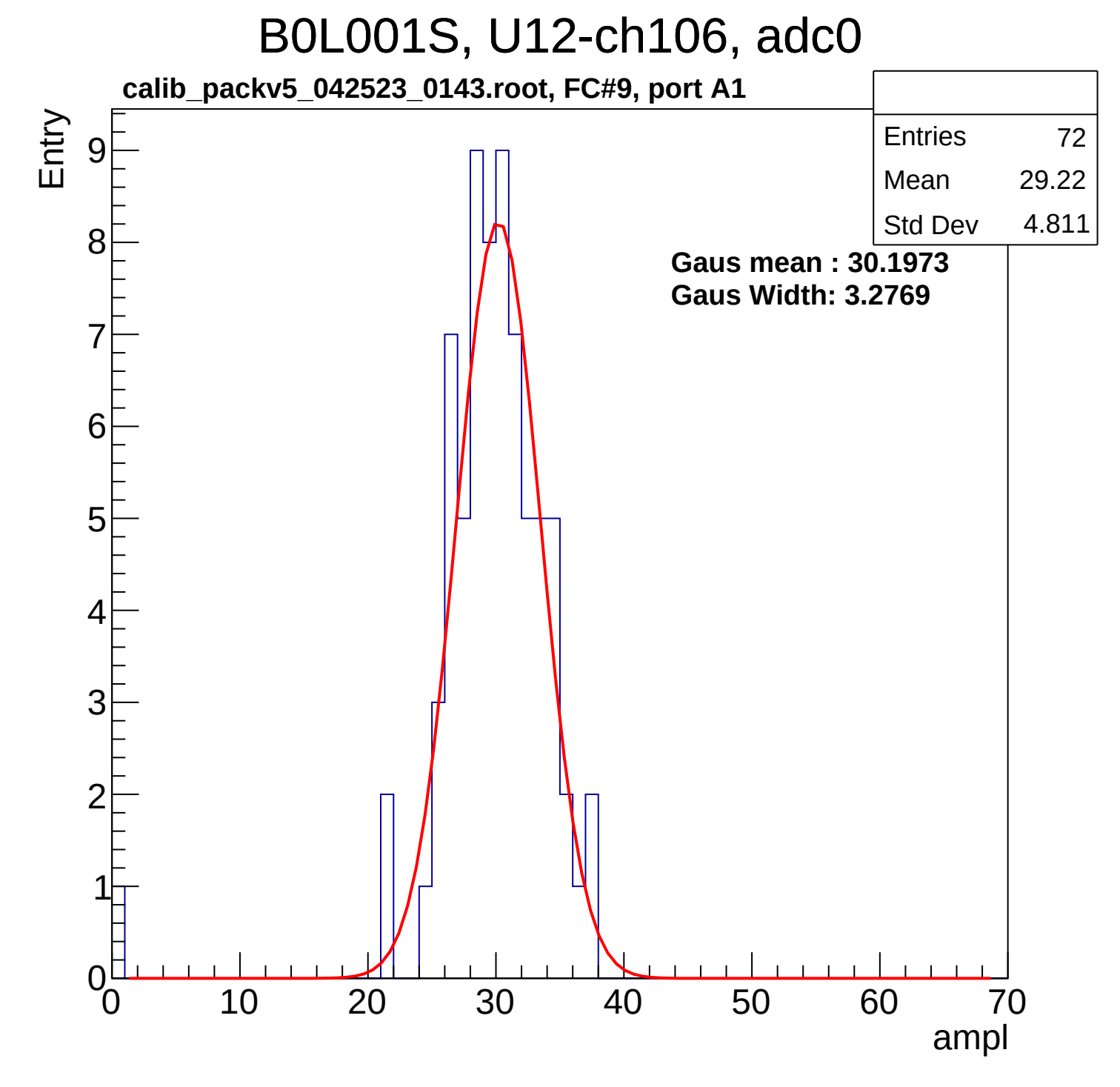

B0L001S, U12-ch105, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 58
Mean 58.45
Std Dev 2.594
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch105, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 20
Mean 58.5
Std Dev 13.54
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch105, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch105, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch106, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 72
Mean 29.22
Std Dev 4.811
Gaus mean : 30.1973
Gaus Width: 3.2769
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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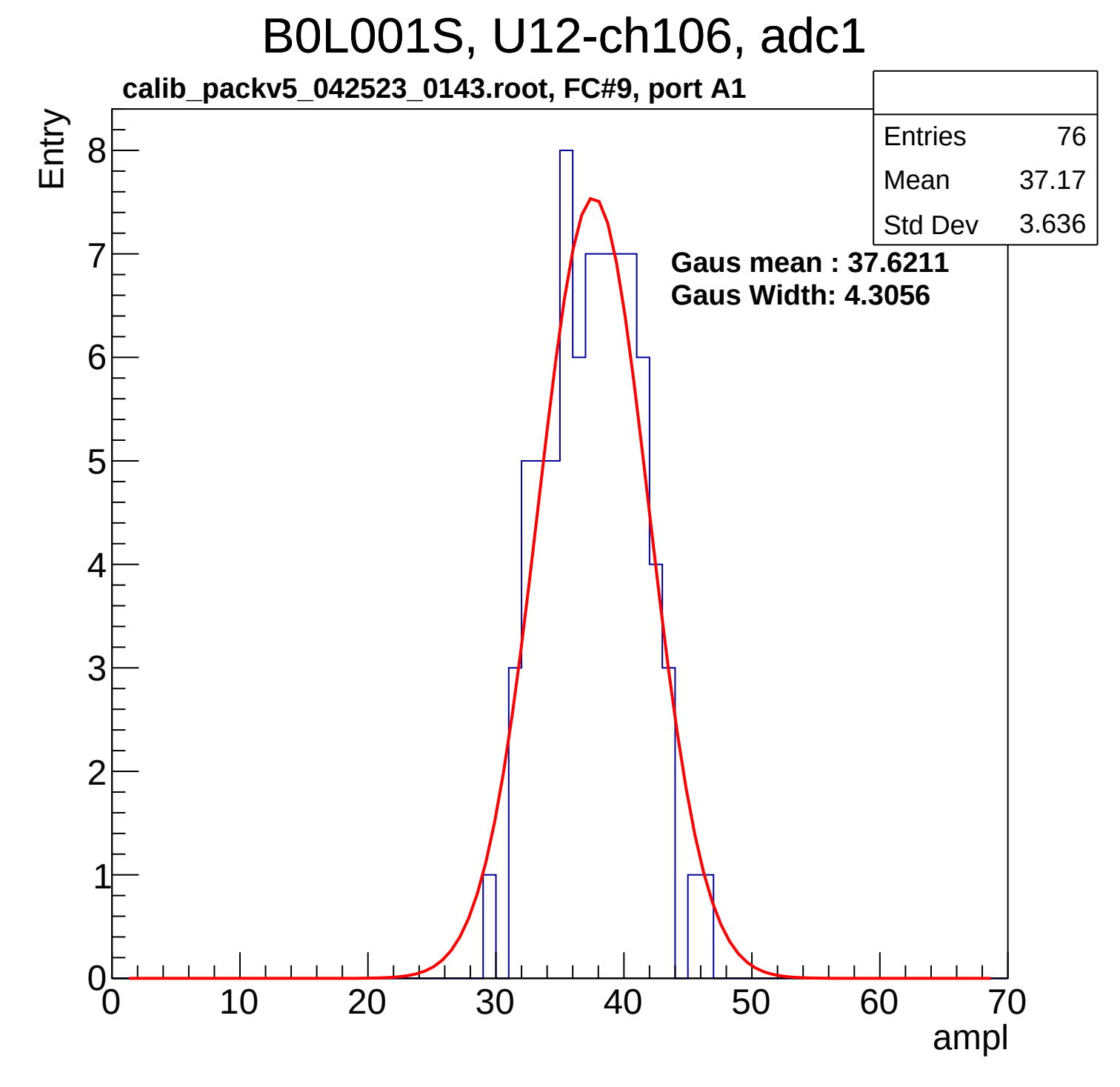
B0L001S, U12-ch106, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 76
Mean 37.17
Std Dev 3.636
Gaus mean : 37.6211
Gaus Width: 4.3056
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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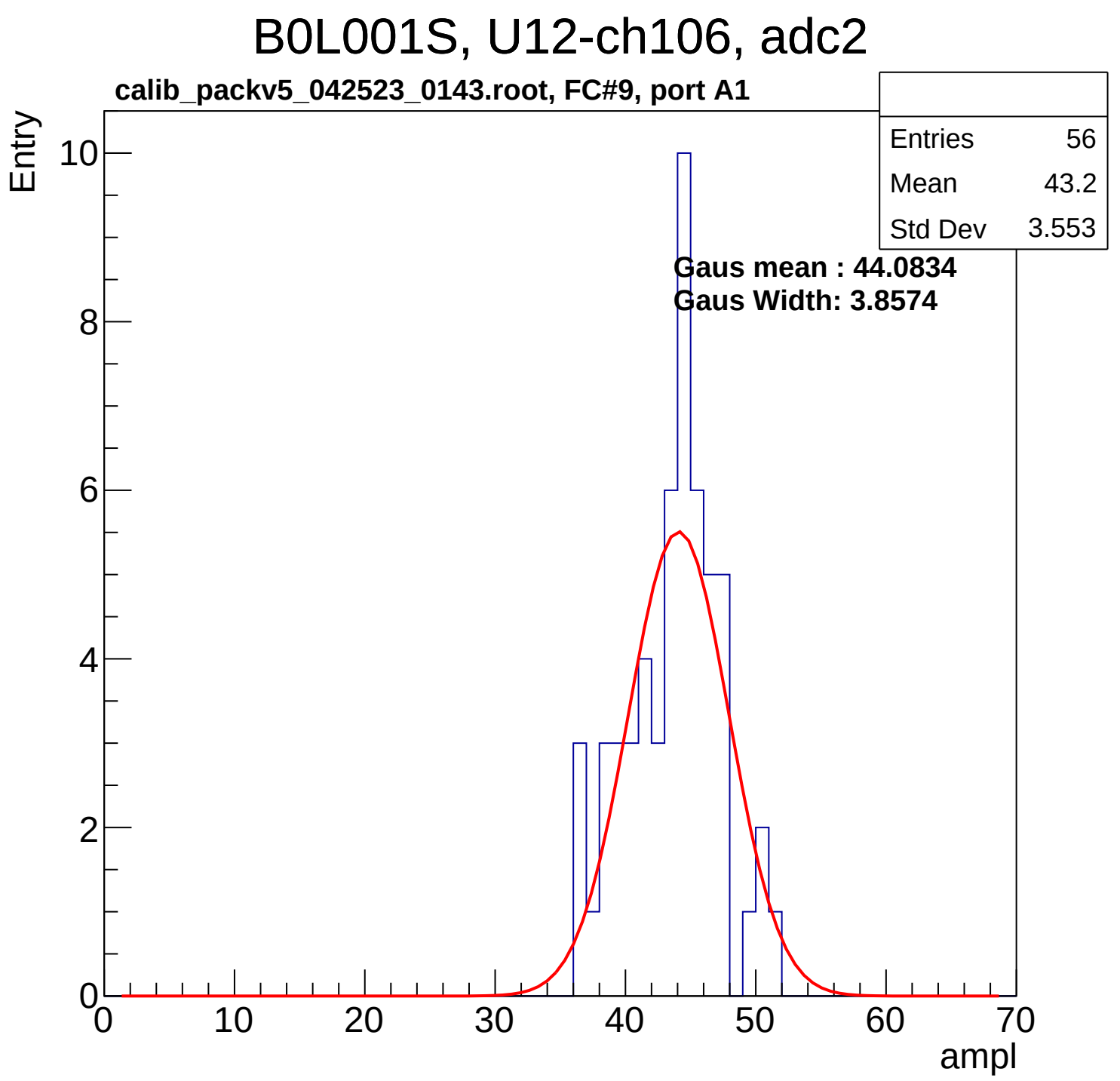
B0L001S, U12-ch106, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 56
Mean 43.2
Std Dev 3.553
Gaus mean : 44.0834
Gaus Width: 3.8574
Entry
ampl
0
2
4
6
8
10
0
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40
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60
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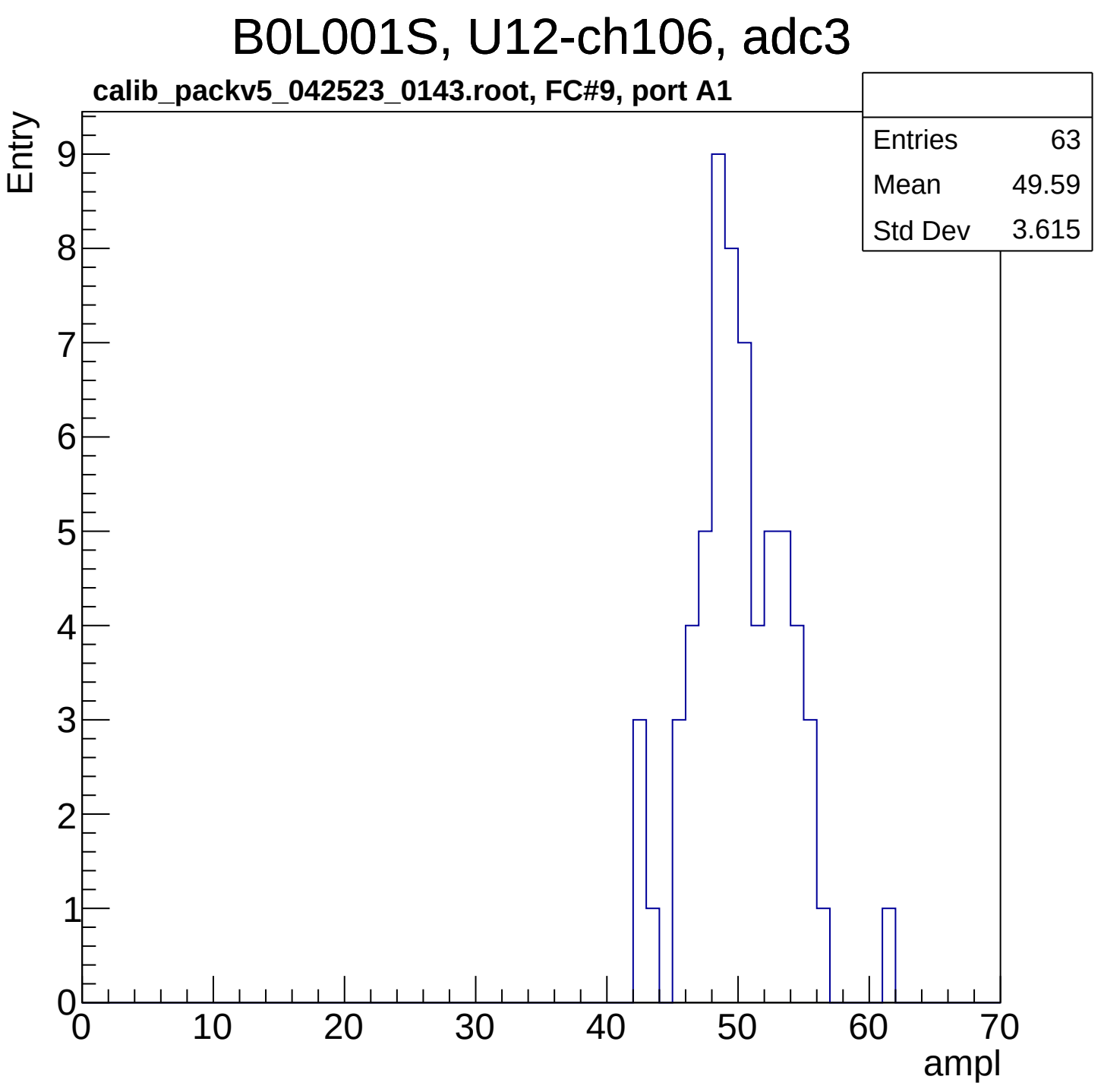
B0L001S, U12-ch106, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 63
Mean 49.59
Std Dev 3.615
Entry
ampl
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6
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0
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40
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60
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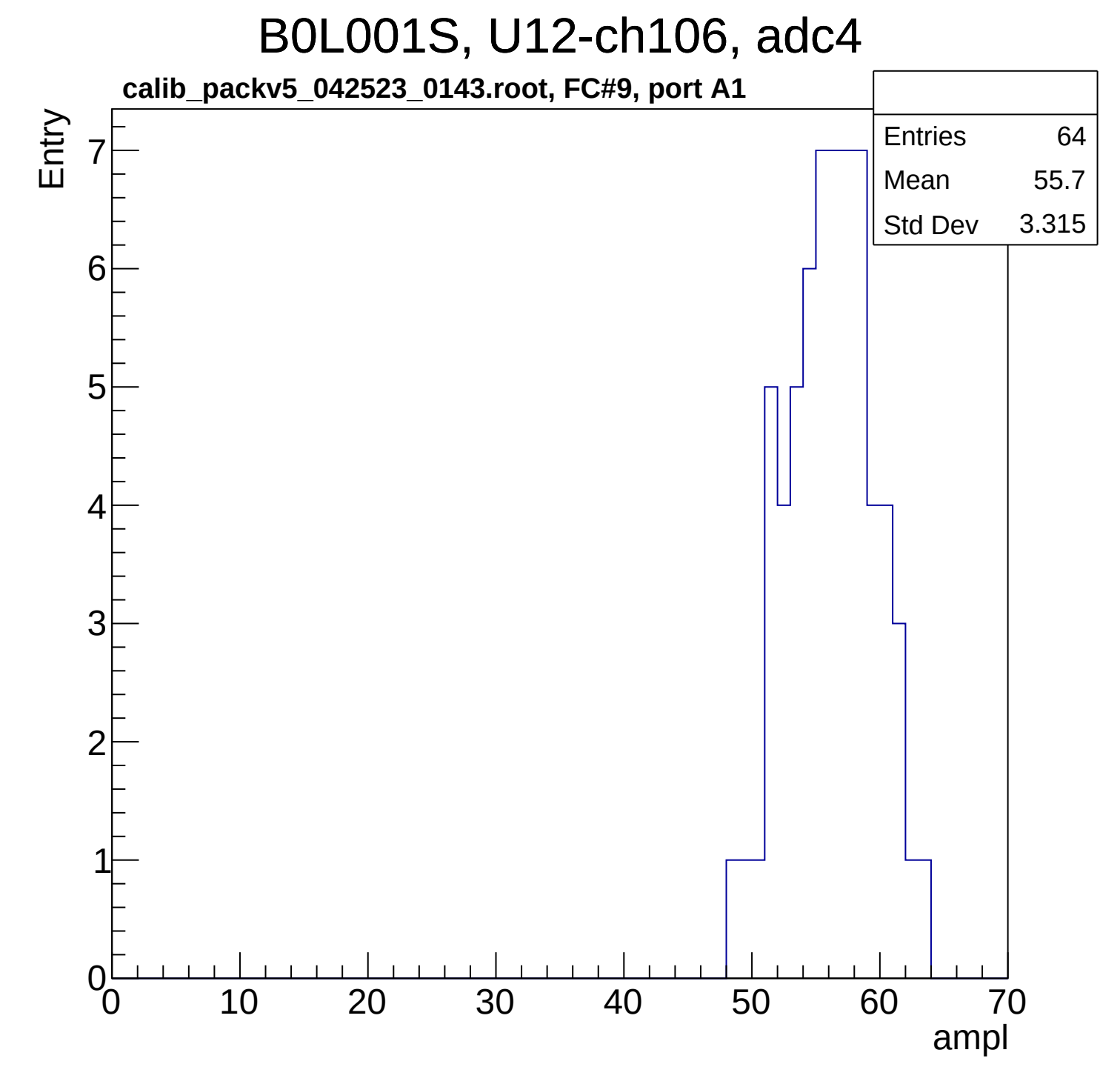
B0L001S, U12-ch106, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 64
Mean 55.7
Std Dev 3.315
Entry
ampl
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1
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3
4
5
6
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0
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20
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40
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60
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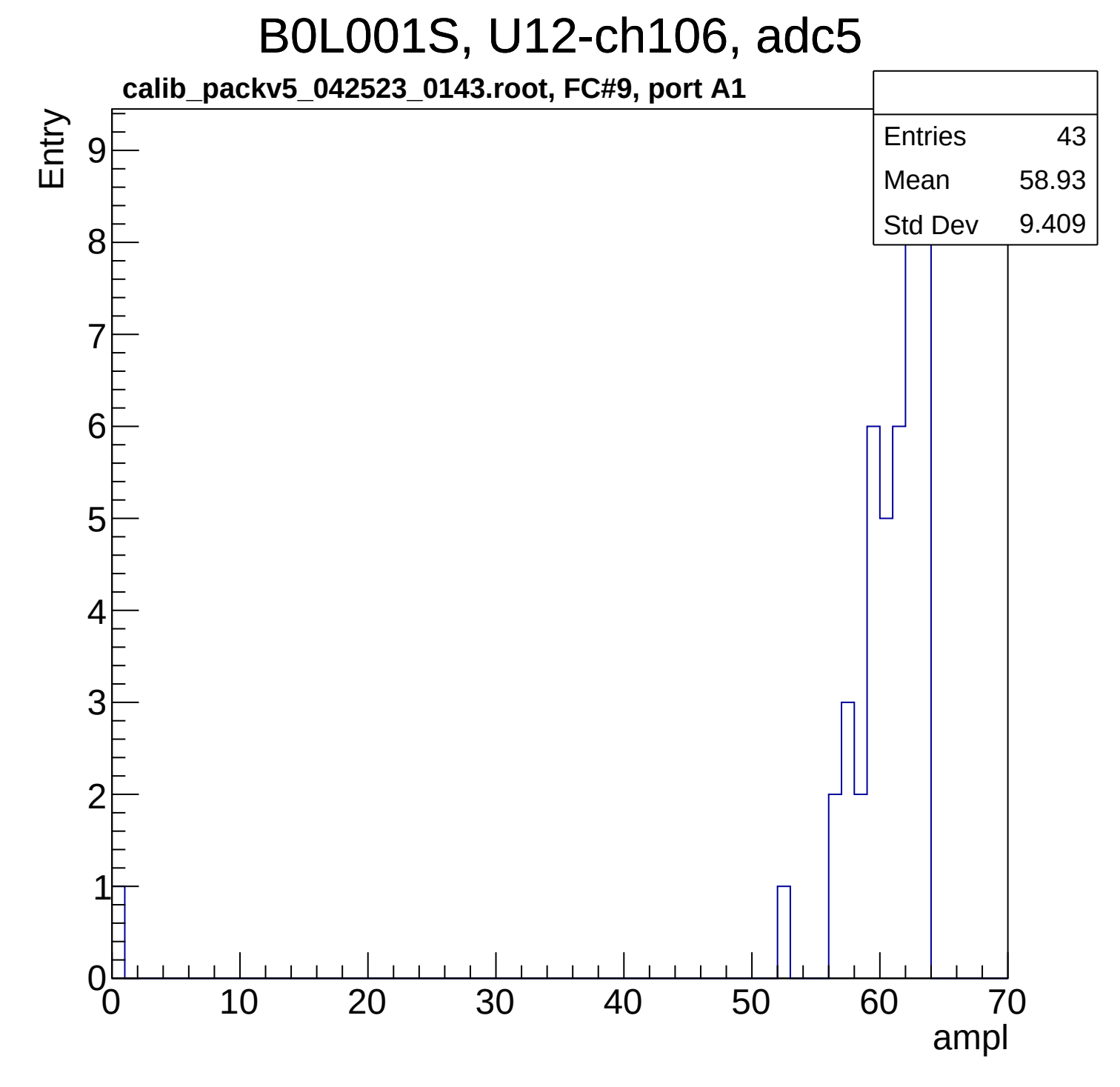
B0L001S, U12-ch106, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 43
Mean 58.93
Std Dev 9.409
Entry
ampl
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3
4
5
6
7
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0
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60
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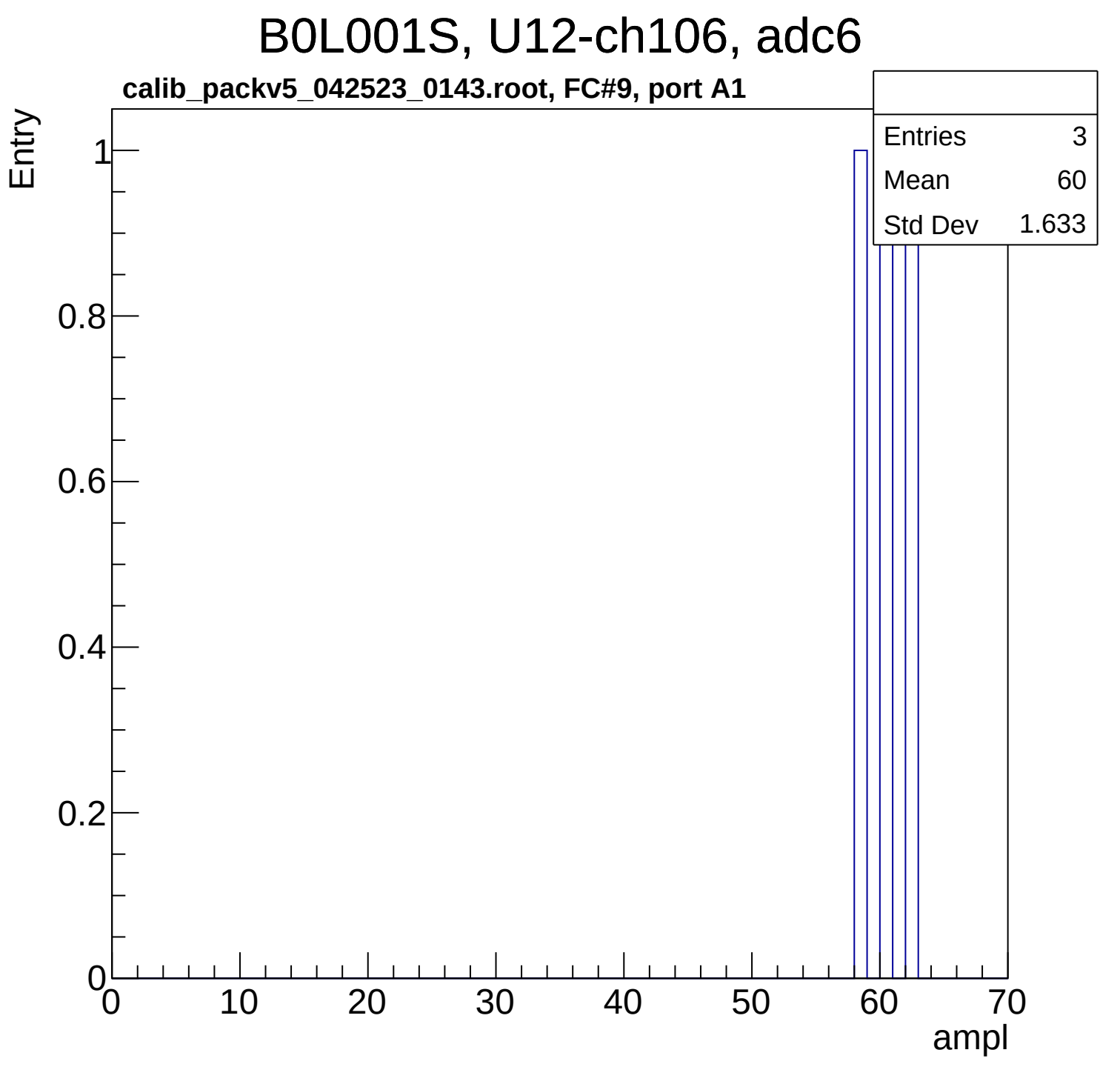
B0L001S, U12-ch106, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 3
Mean 60
Std Dev 1.633
Entry
ampl
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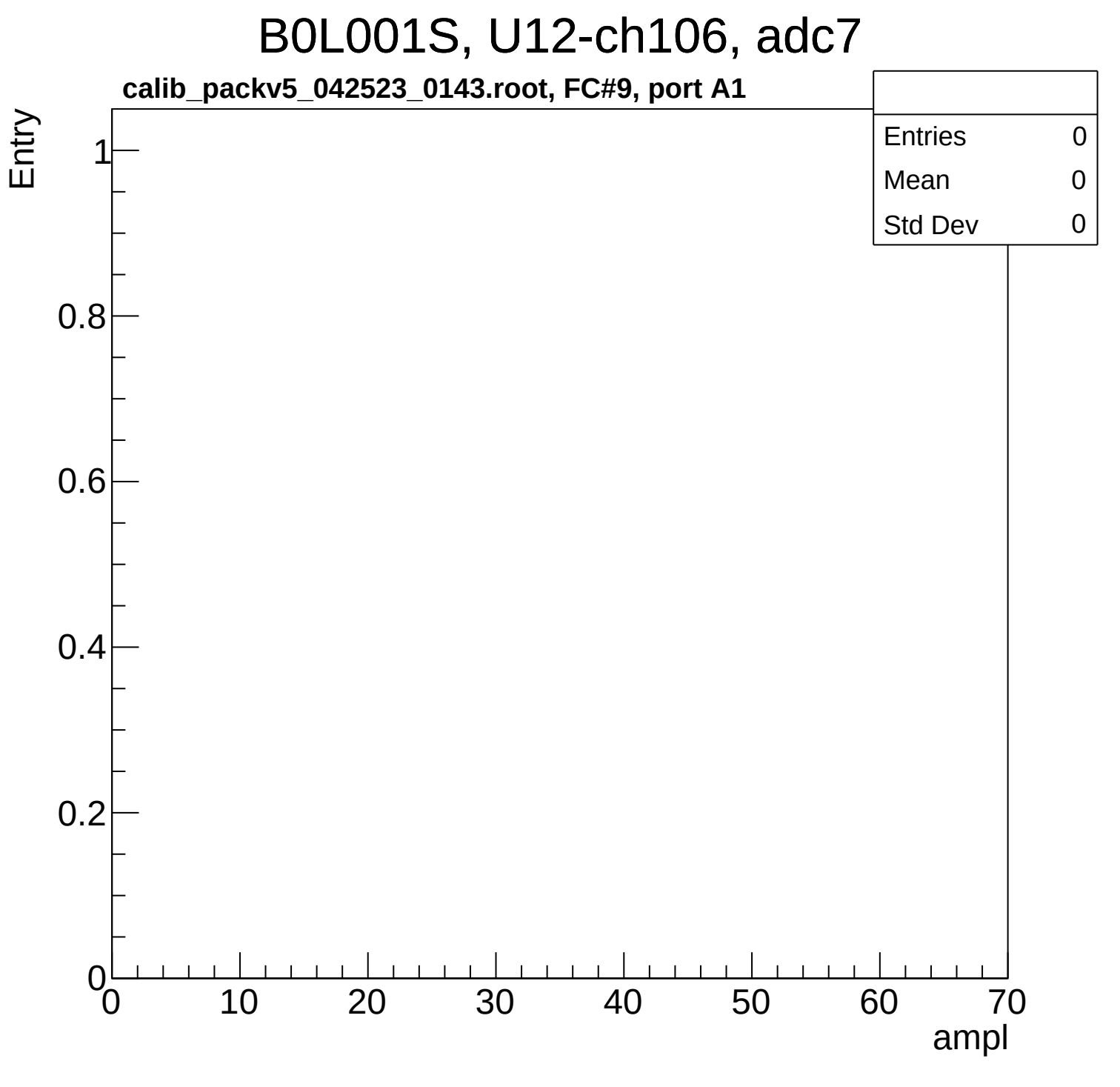
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L001S, U12-ch106, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
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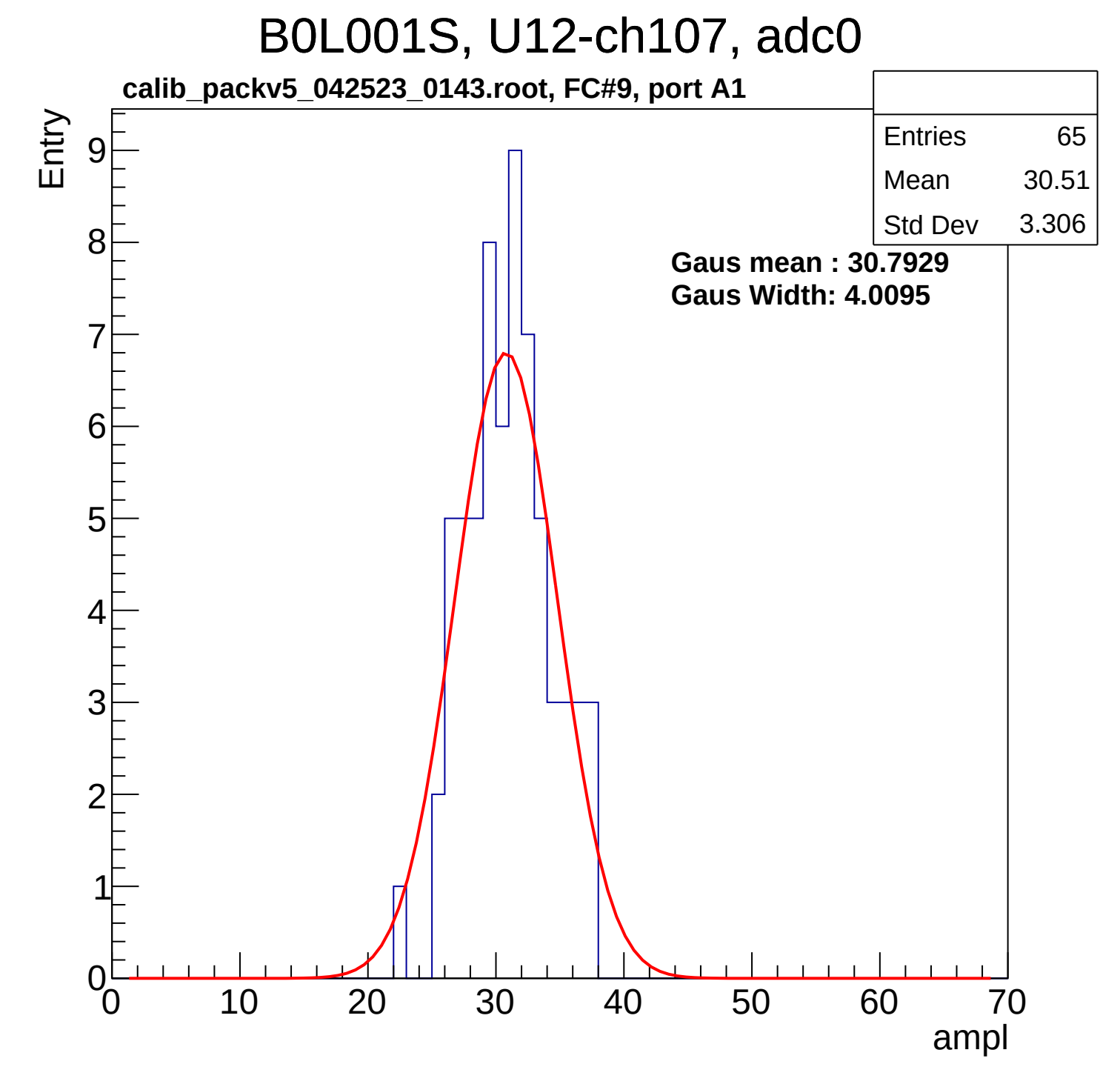
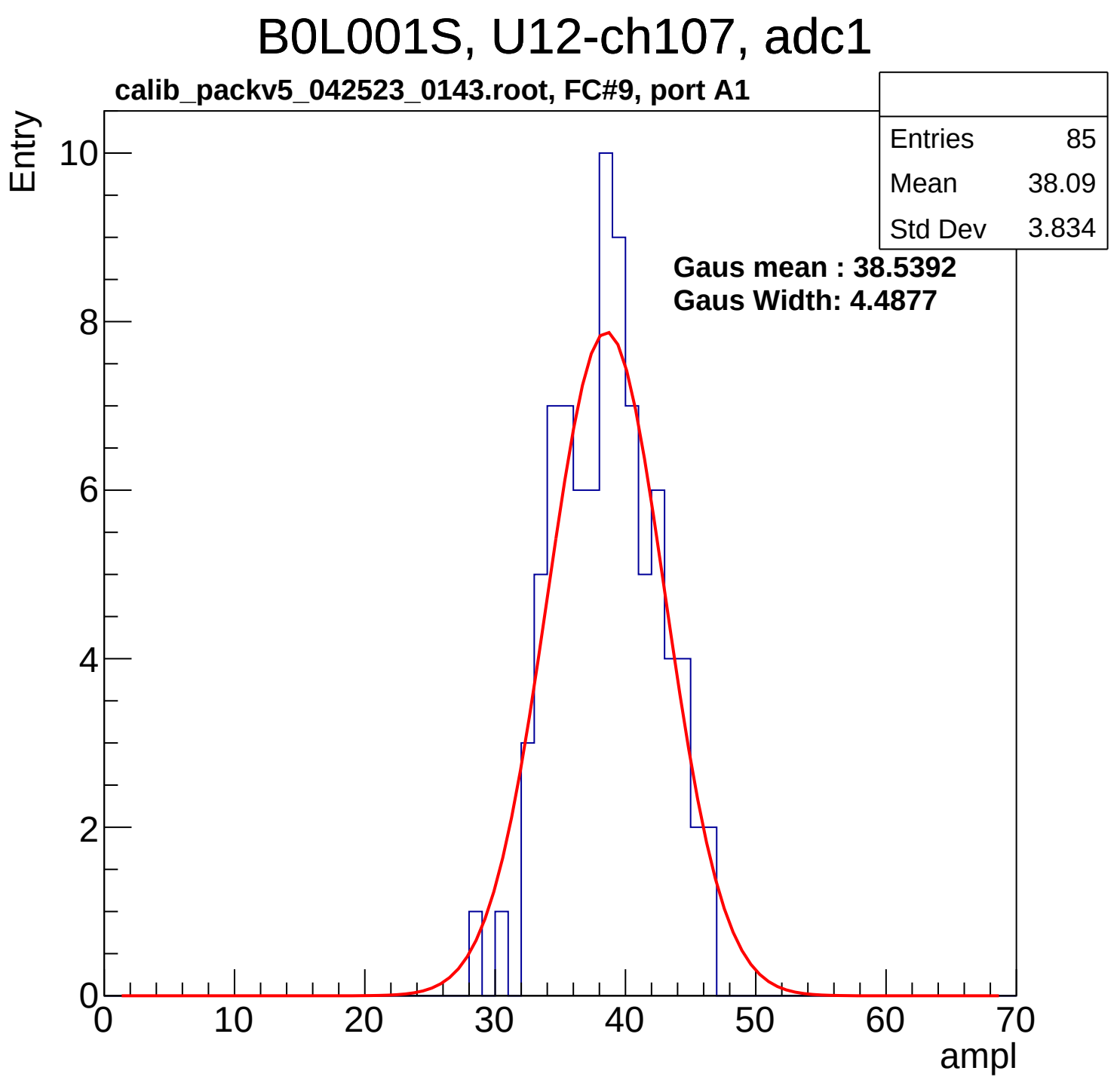
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch107, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 65
Mean 30.51
Std Dev 3.306
Gaus mean : 30.7929
Gaus Width: 4.0095
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch107, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 85
Mean 38.09
Std Dev 3.834
Gaus mean : 38.5392
Gaus Width: 4.4877
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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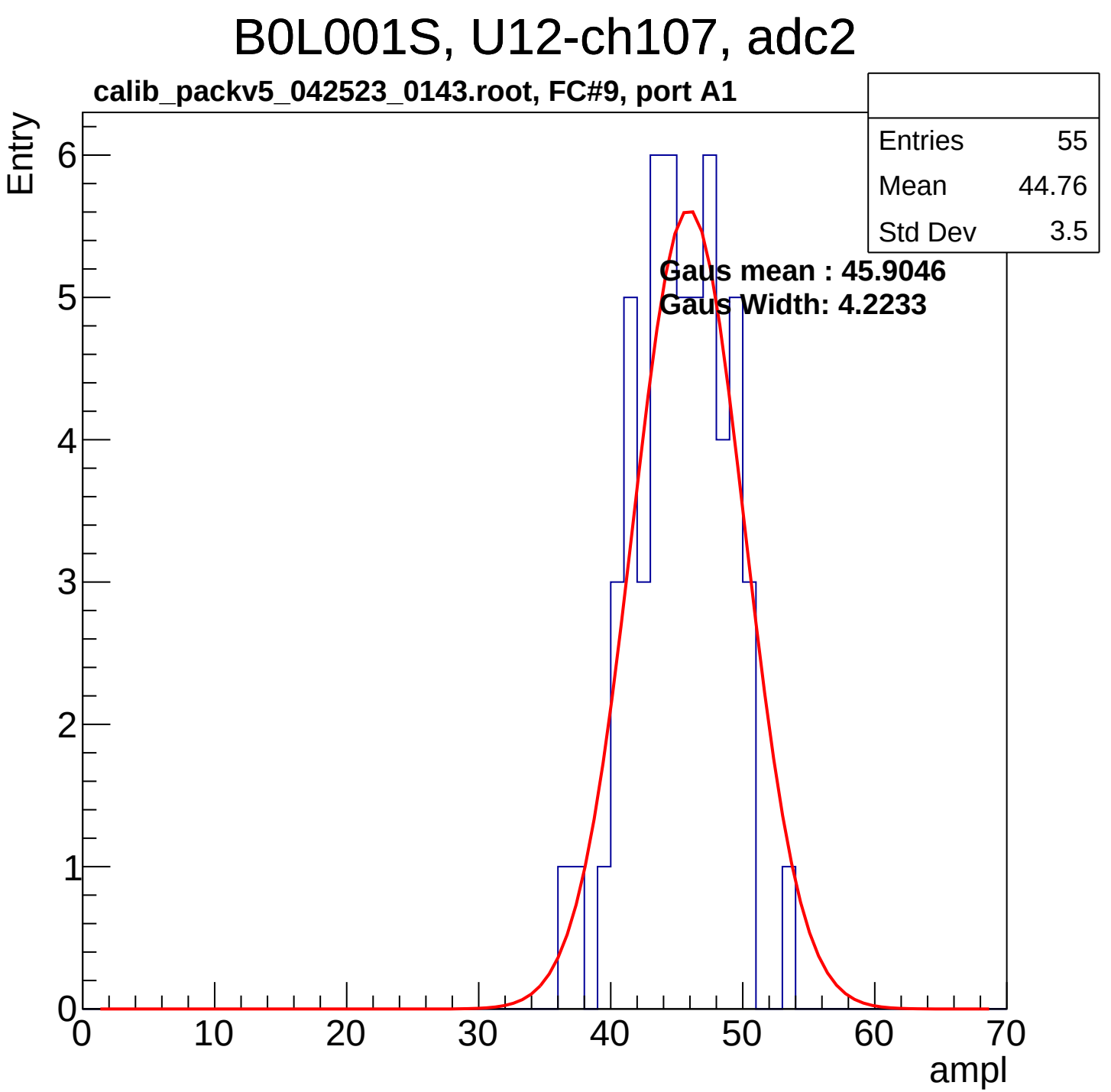
B0L001S, U12-ch107, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 55
Mean 44.76
Std Dev 3.5
Gaus mean : 45.9046
Gaus Width: 4.2233
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
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60
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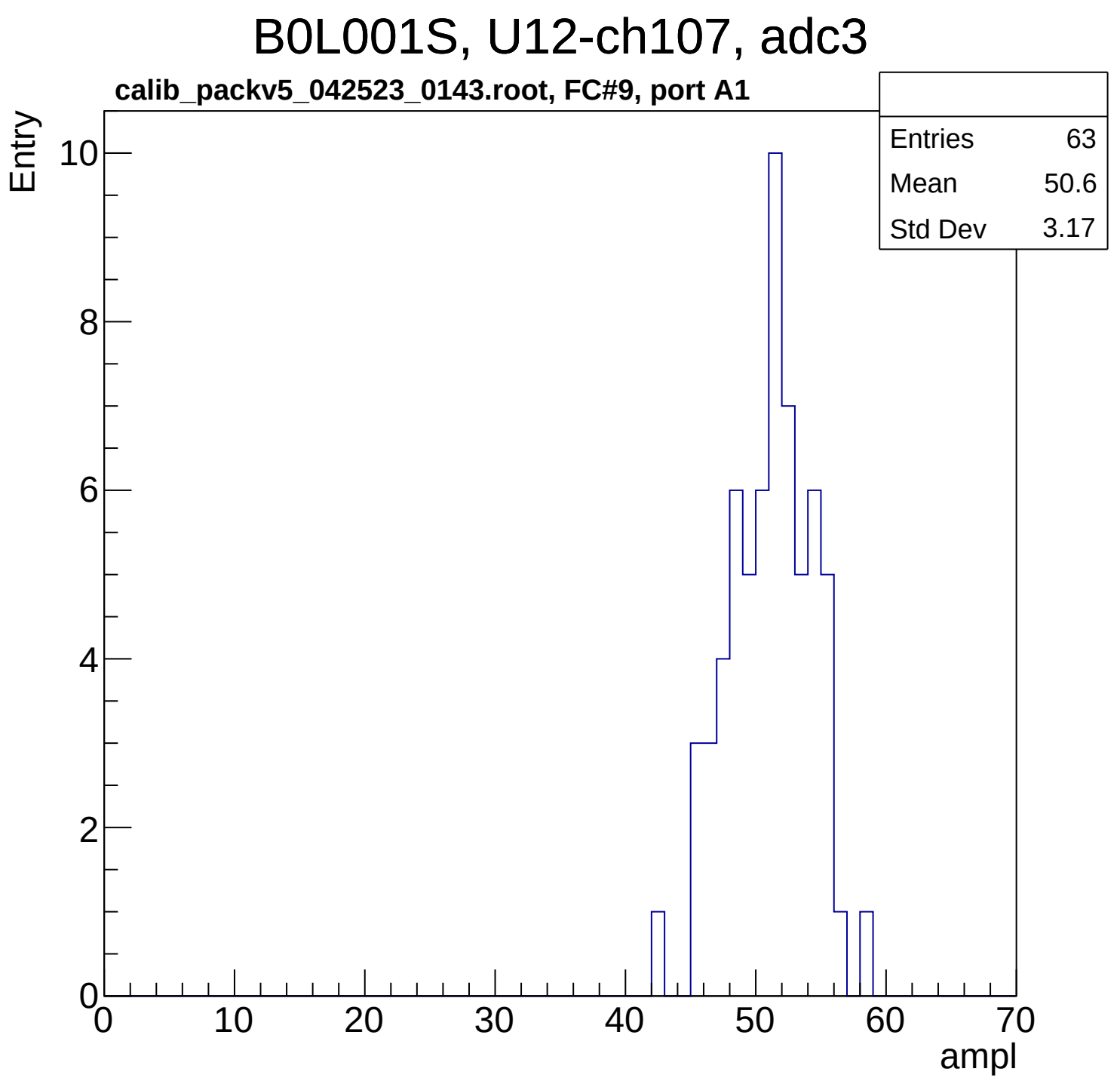
B0L001S, U12-ch107, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 63
Mean 50.6
Std Dev 3.17
Entry
ampl
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2
4
6
8
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0
10
20
30
40
50
60
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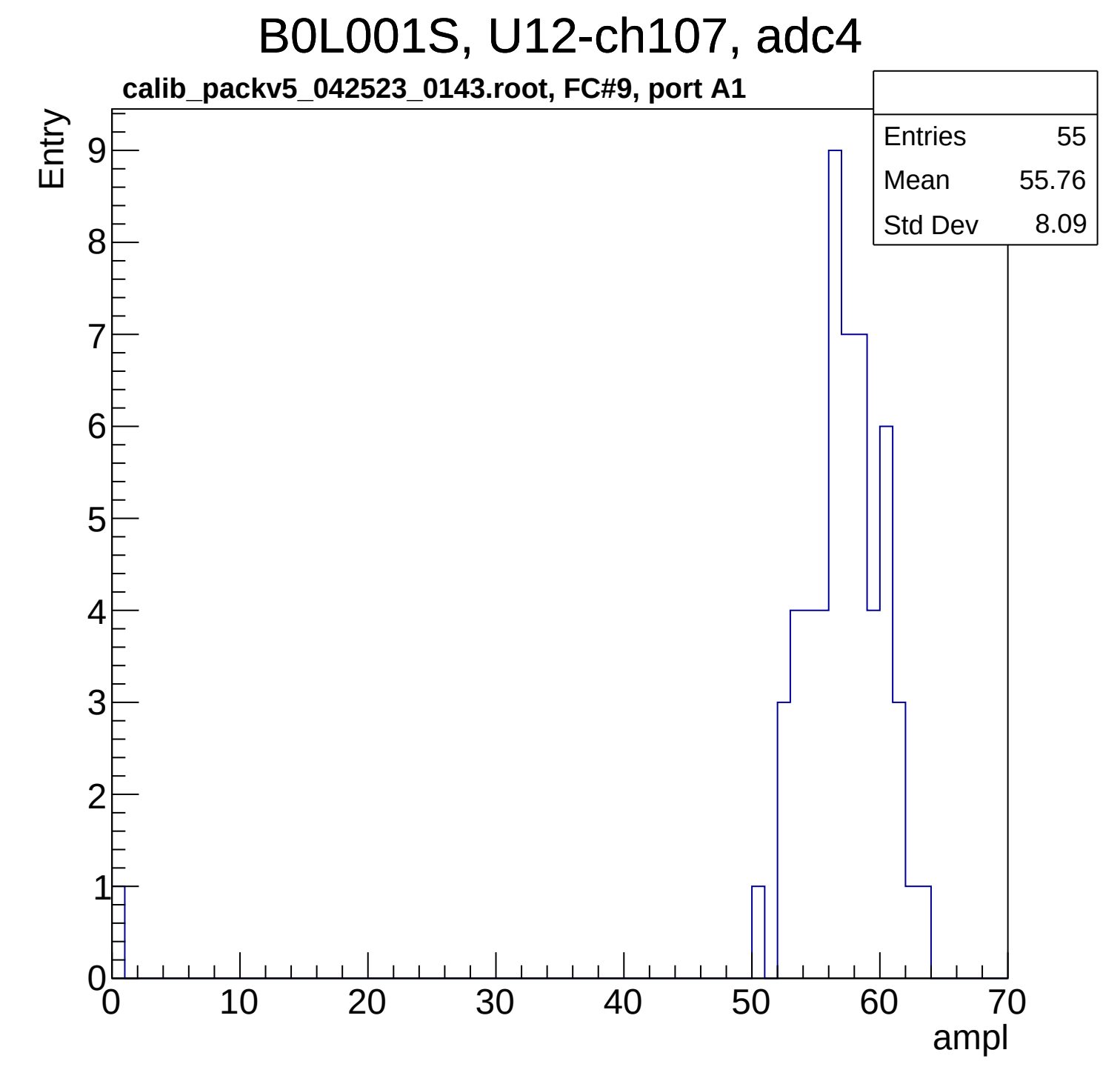
B0L001S, U12-ch107, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 55
Mean 55.76
Std Dev 8.09
Entry
ampl
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3
4
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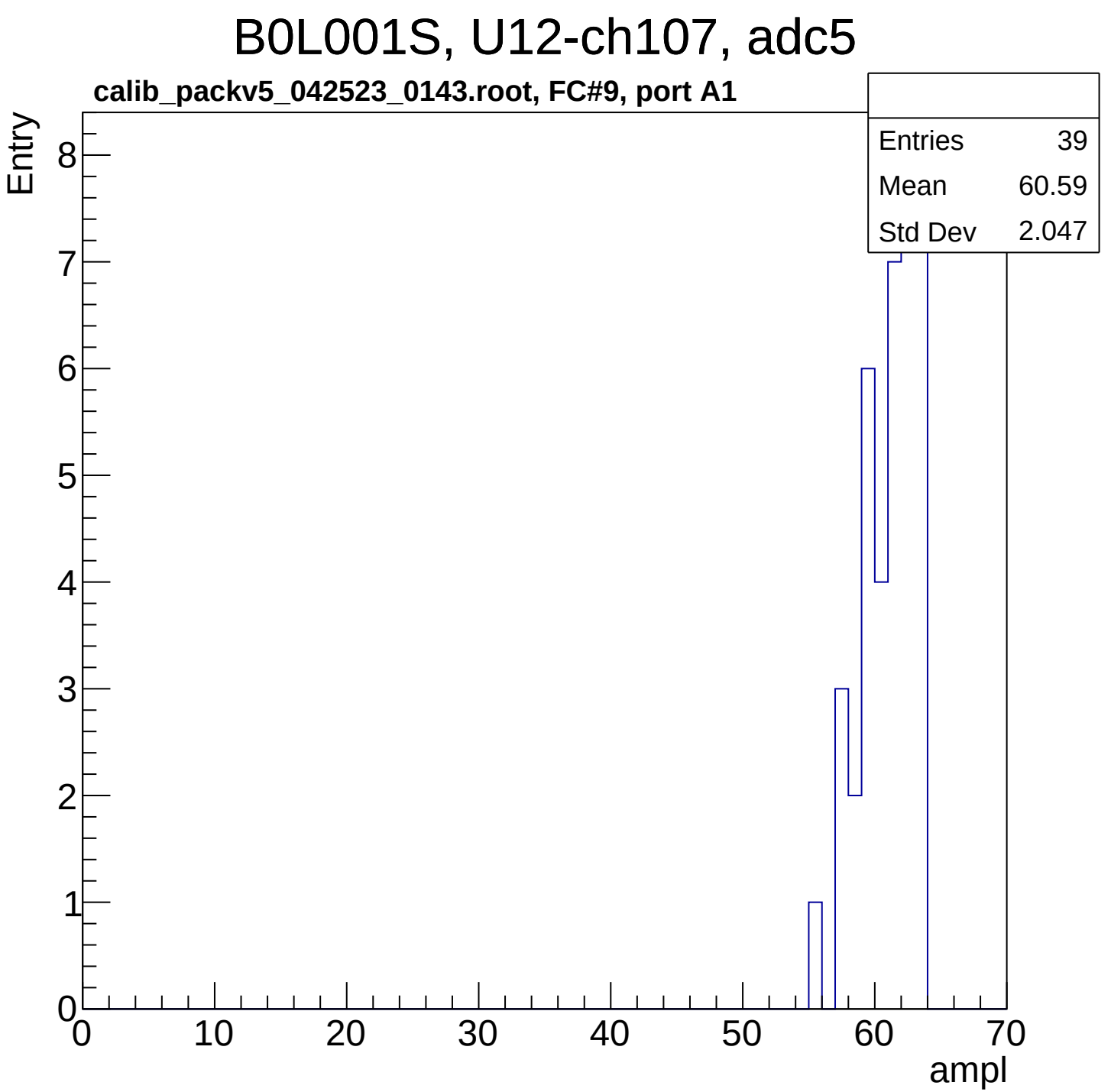
B0L001S, U12-ch107, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 39
Mean 60.59
Std Dev 2.047
Entry
ampl
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3
4
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0
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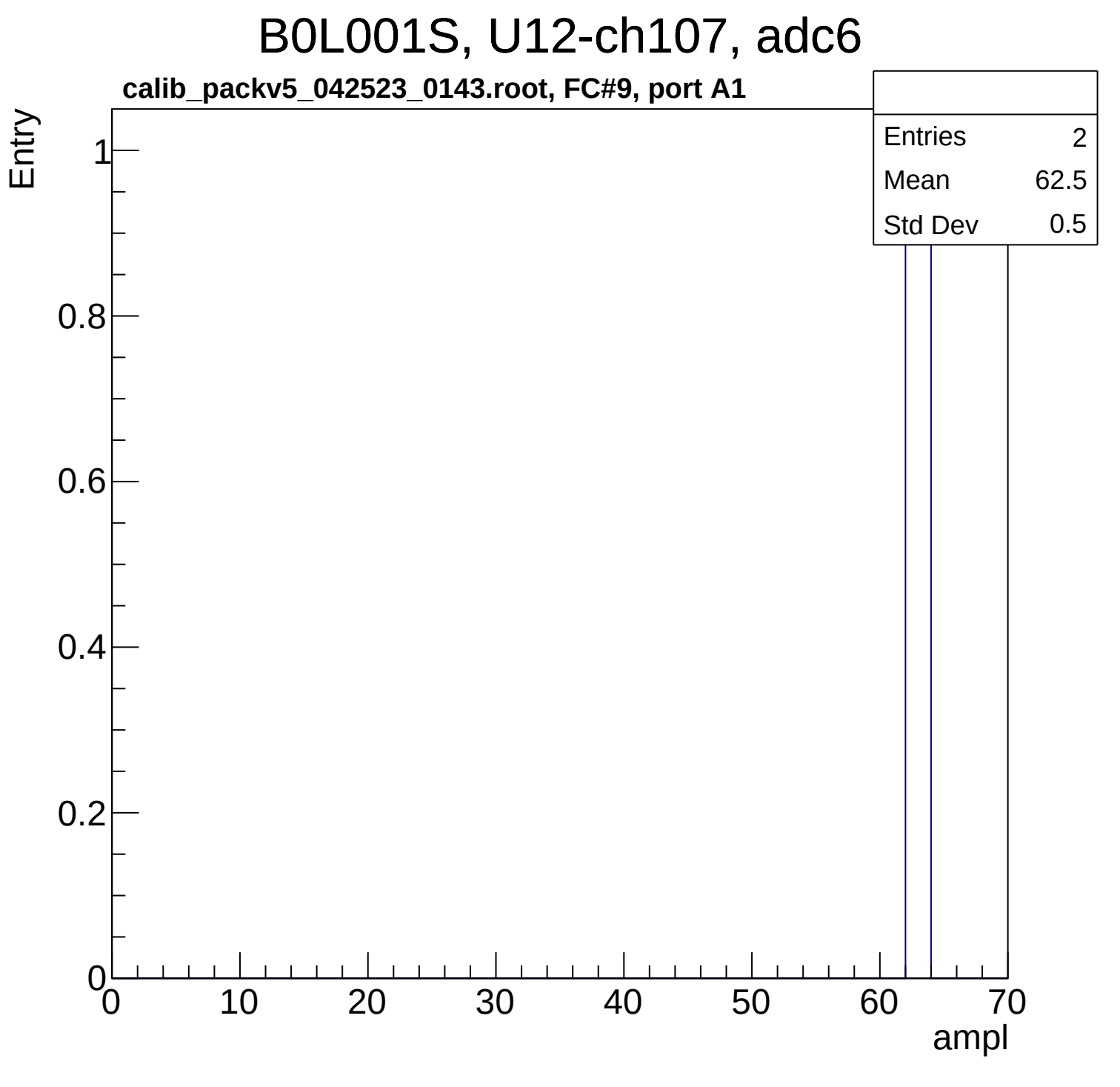
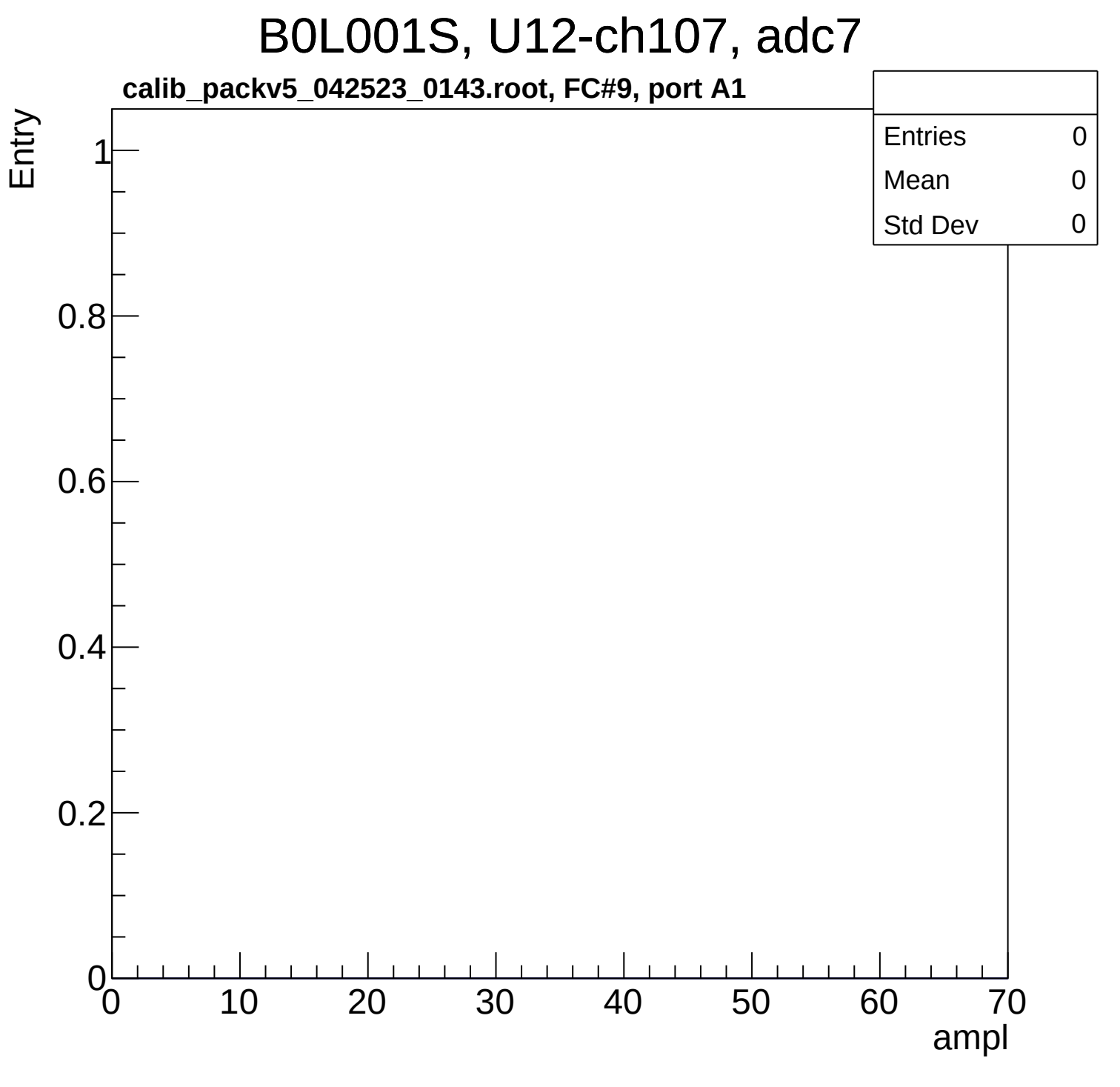

B0L001S, U12-ch107, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch107, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
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0.6
0.4
0.2
0
0
10
20
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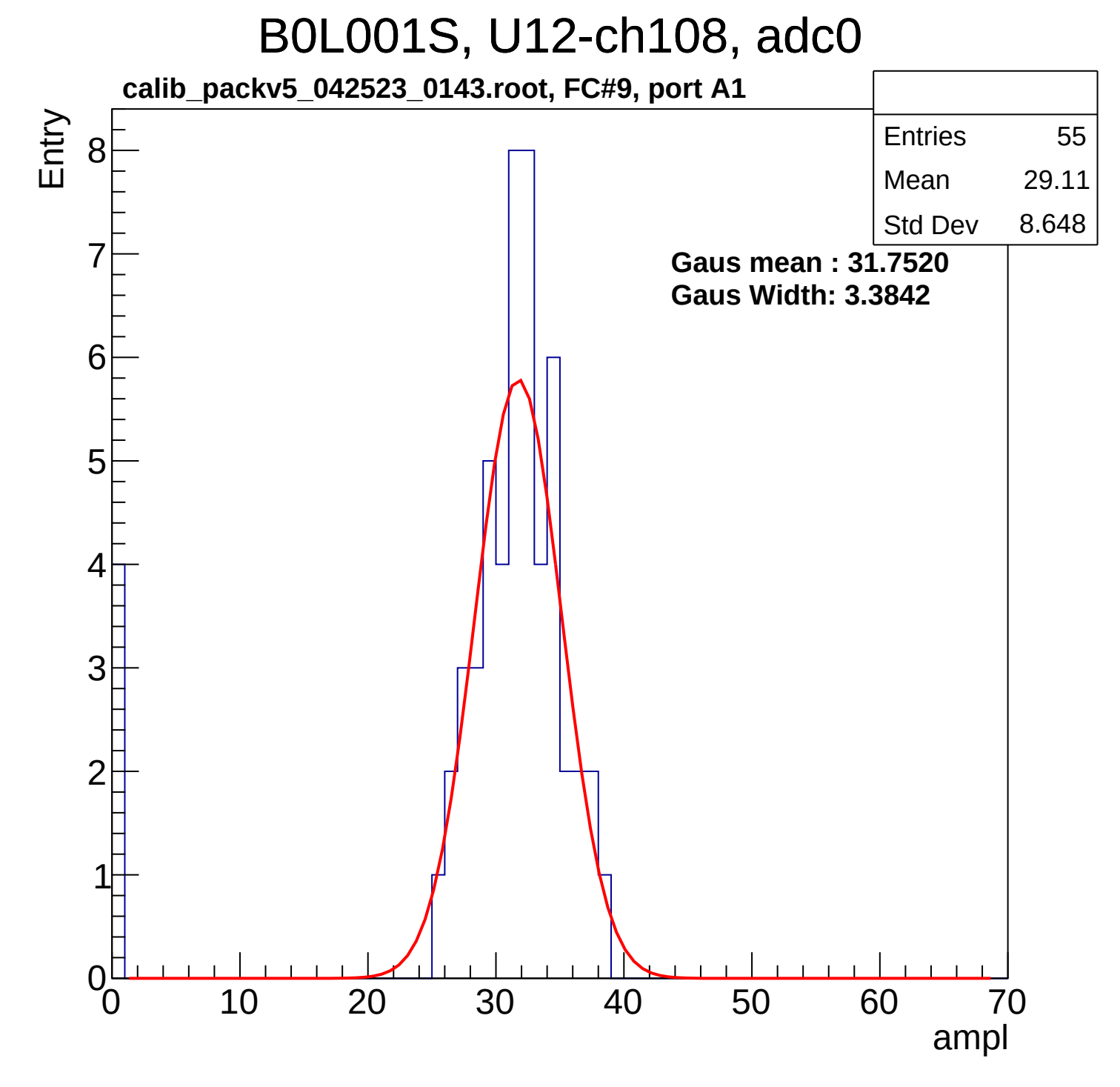
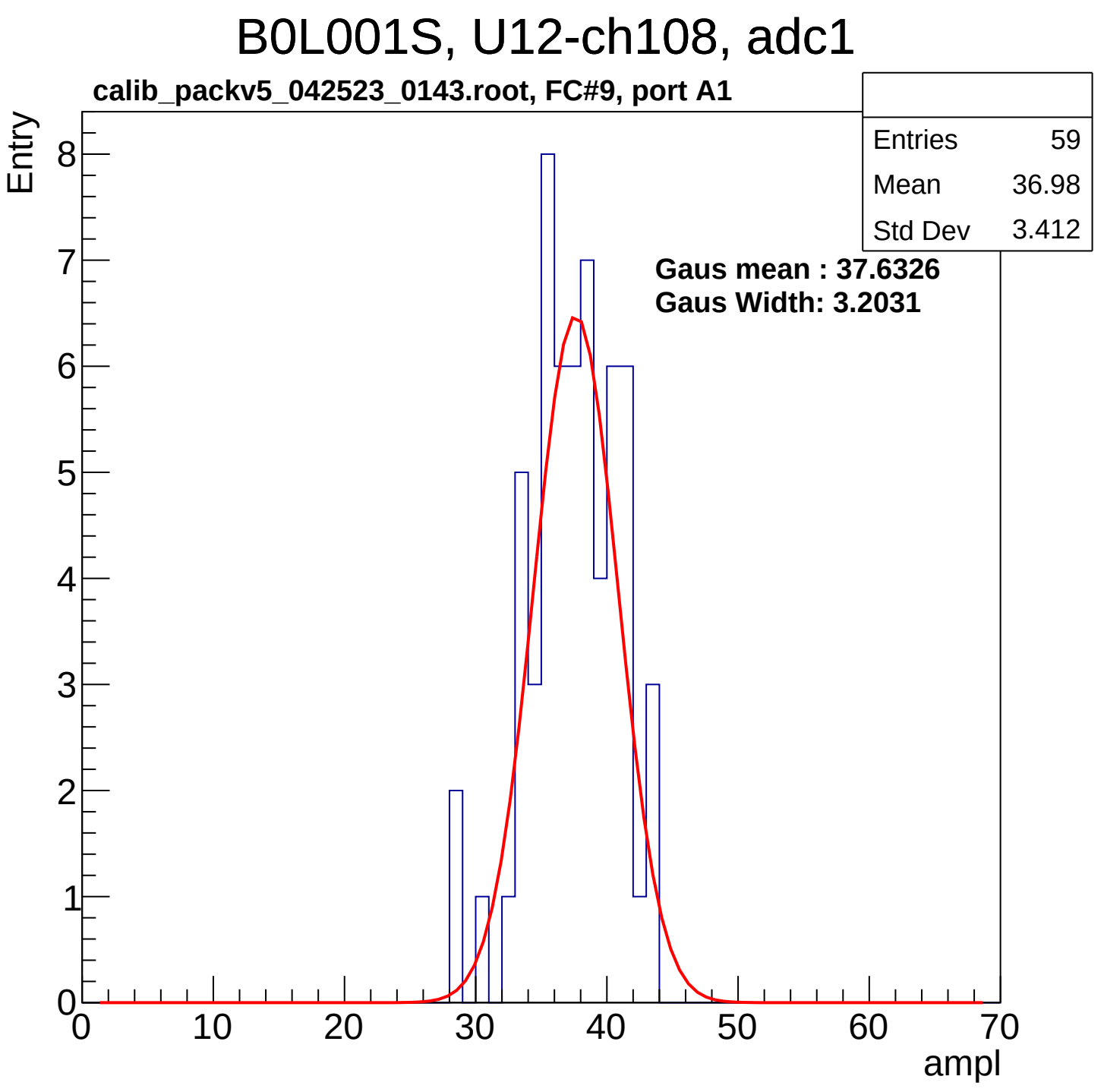
40
50
60
70
ampl


B0L001S, U12-ch108, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 55
Mean 29.11
Std Dev 8.648
Gaus mean : 31.7520
Gaus Width: 3.3842
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch108, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 59
Mean 36.98
Std Dev 3.412
Gaus mean : 37.6326
Gaus Width: 3.2031
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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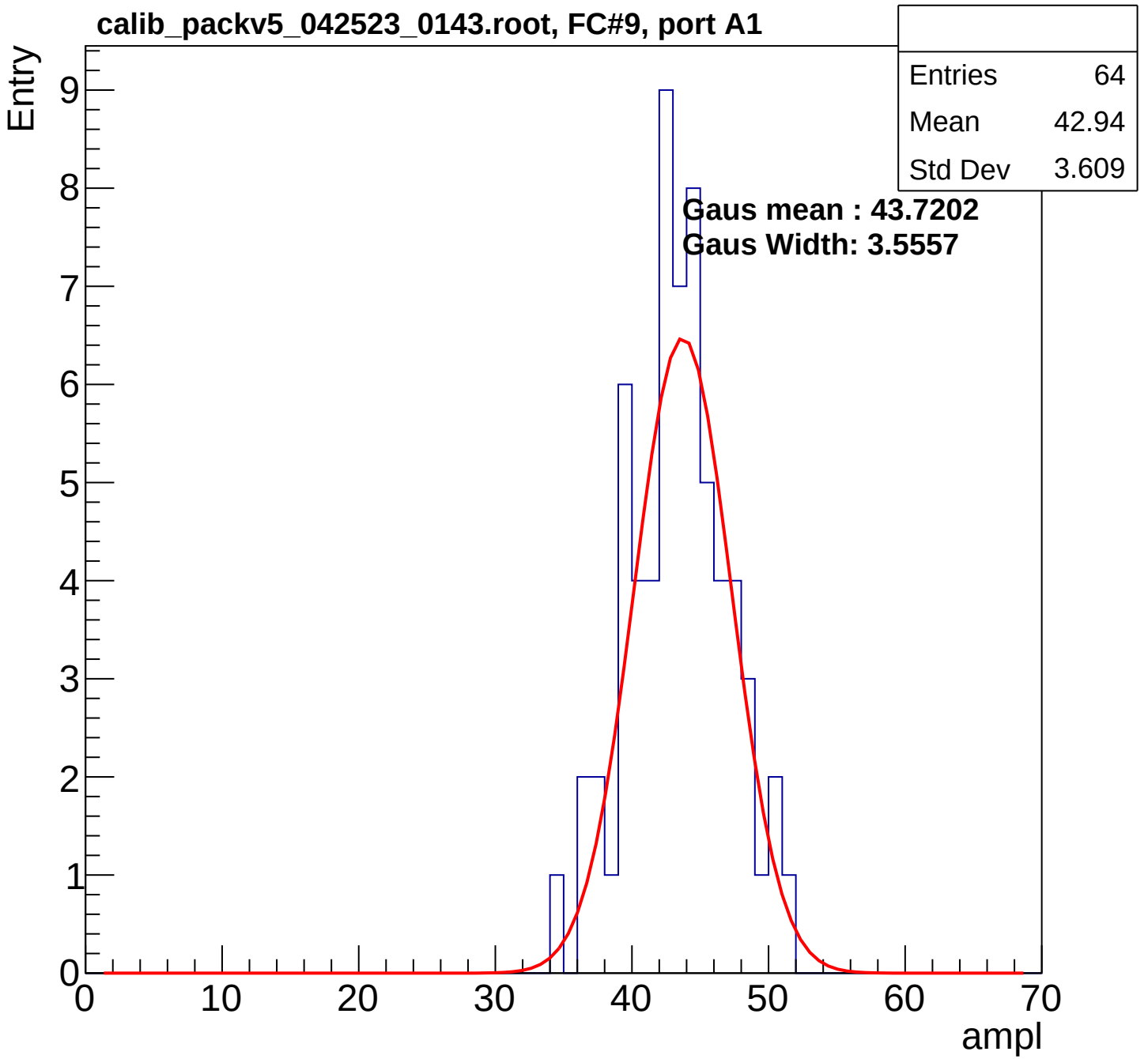
B0L001S, U12-ch108, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 64
Mean 42.94
Std Dev 3.609
Gaus mean : 43.7202
Gaus Width: 3.5557
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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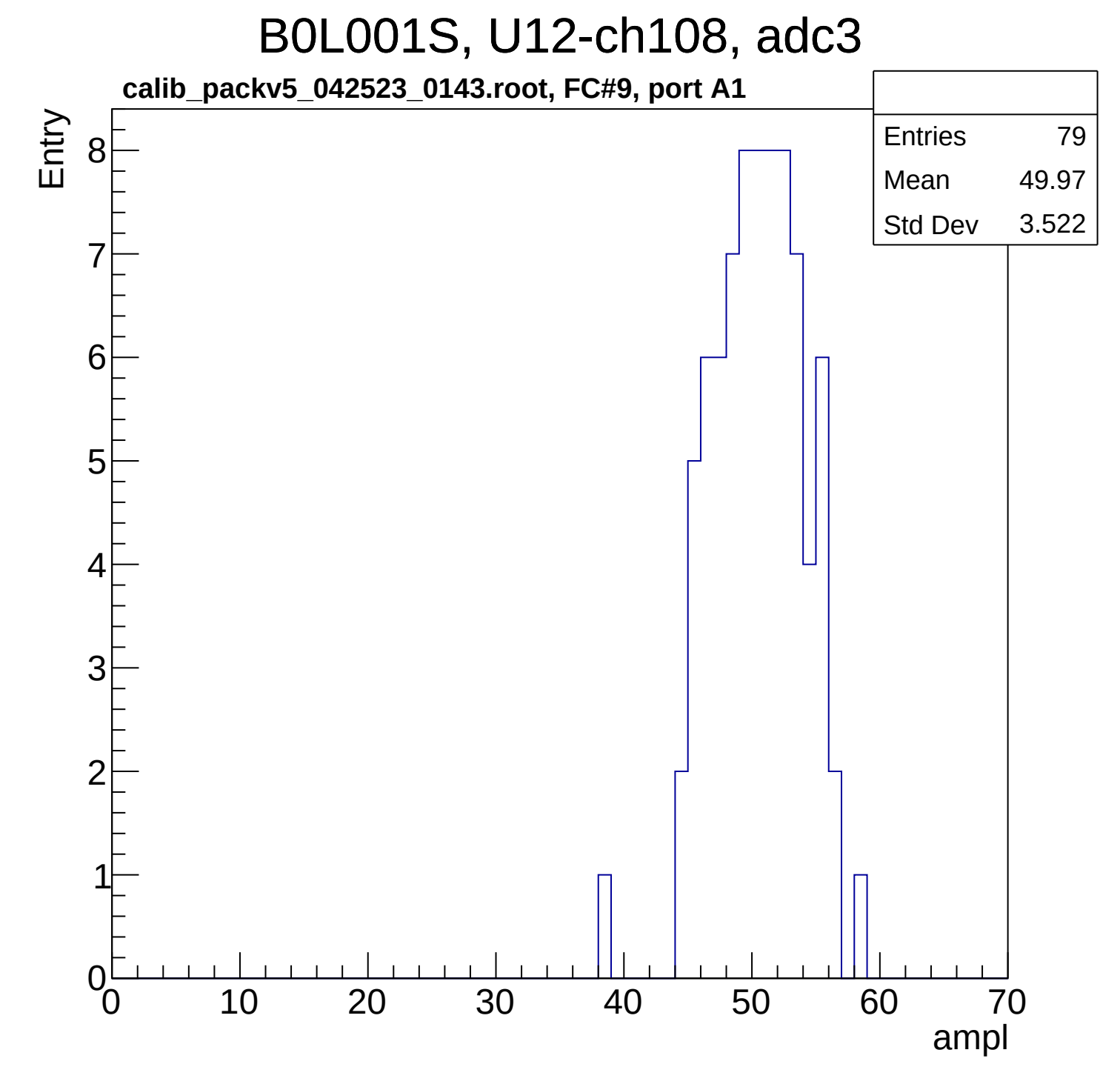
B0L001S, U12-ch108, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 79
Mean 49.97
Std Dev 3.522
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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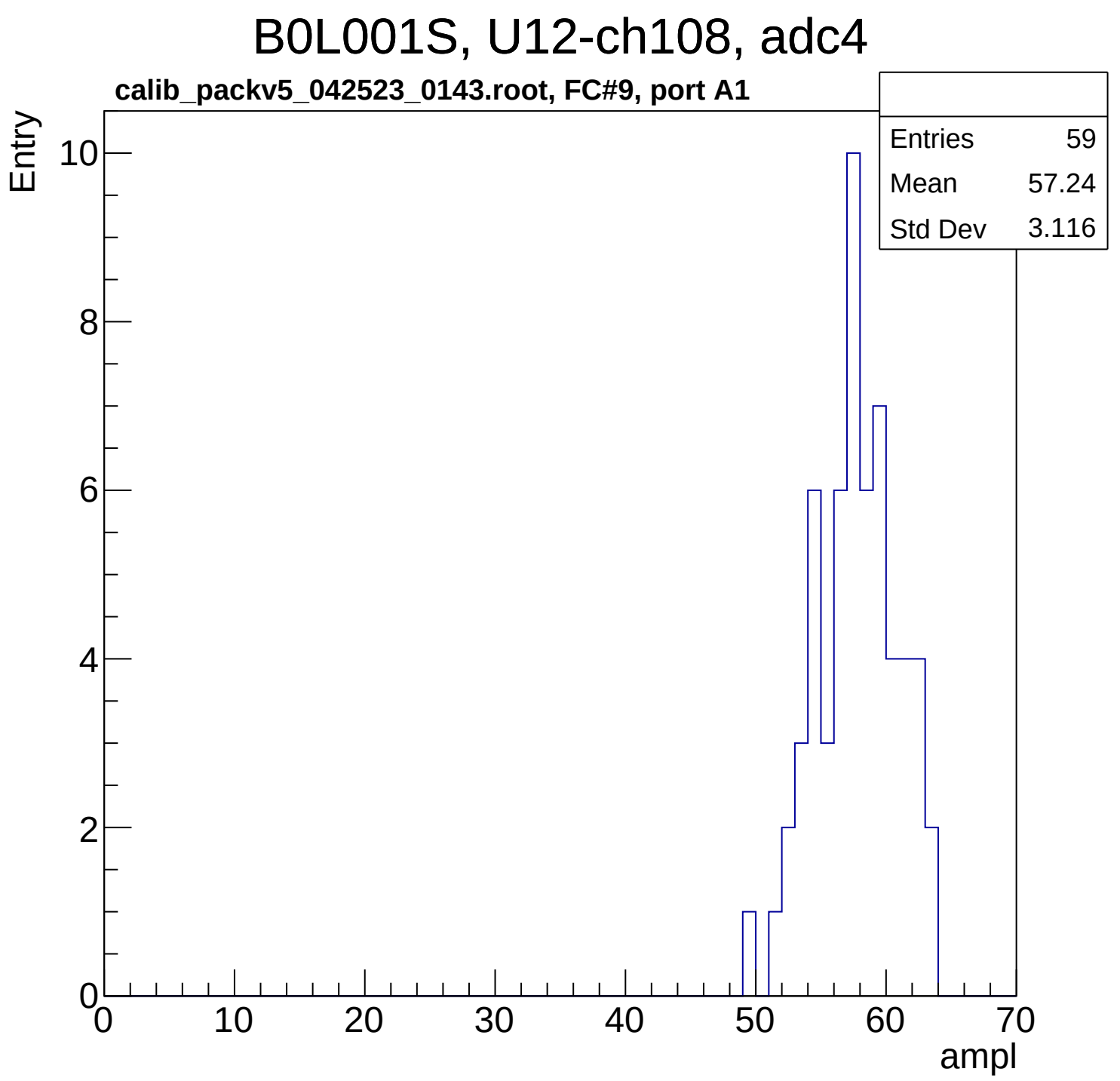
B0L001S, U12-ch108, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 59
Mean 57.24
Std Dev 3.116
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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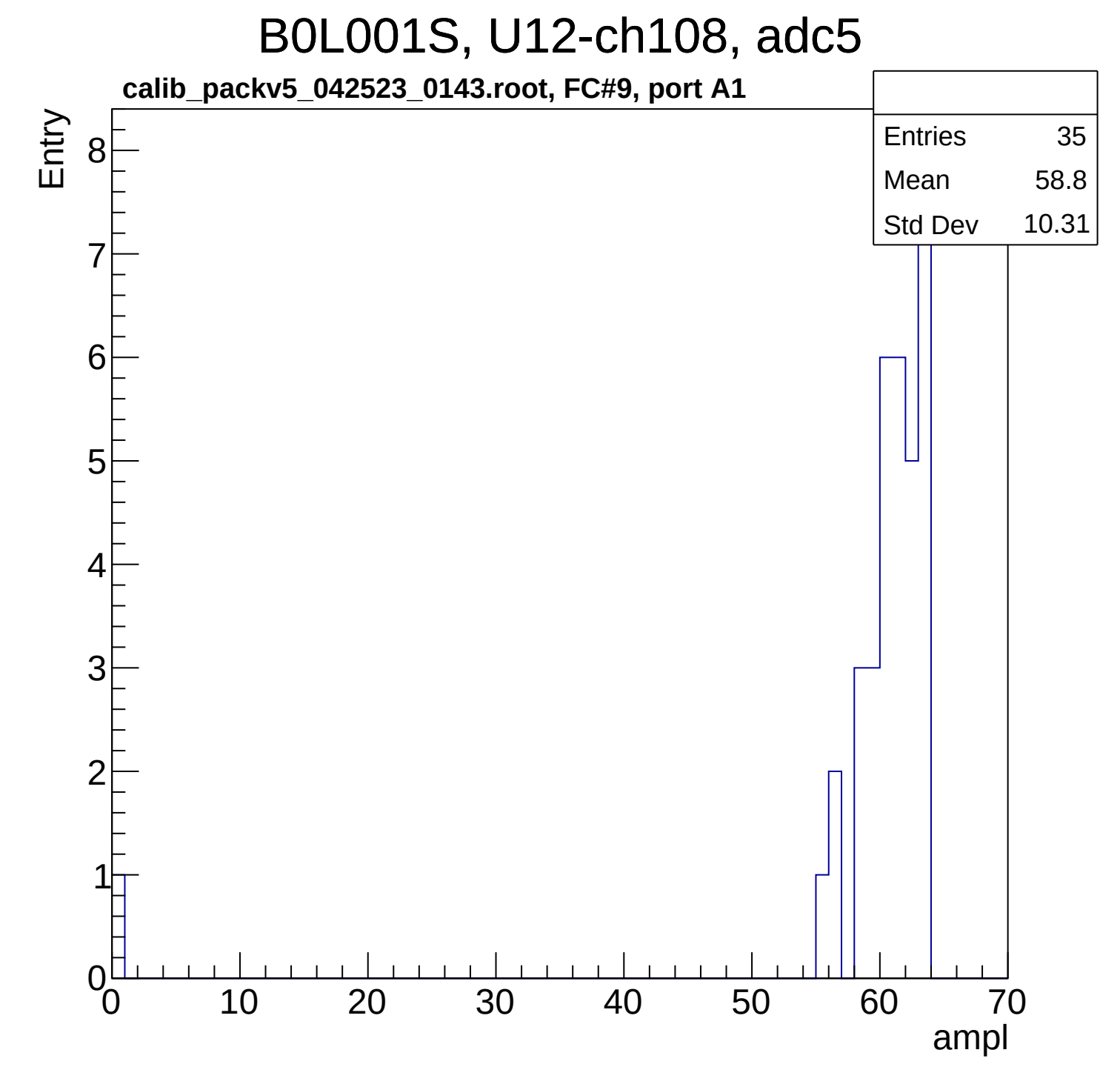
B0L001S, U12-ch108, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 35
Mean 58.8
Std Dev 10.31
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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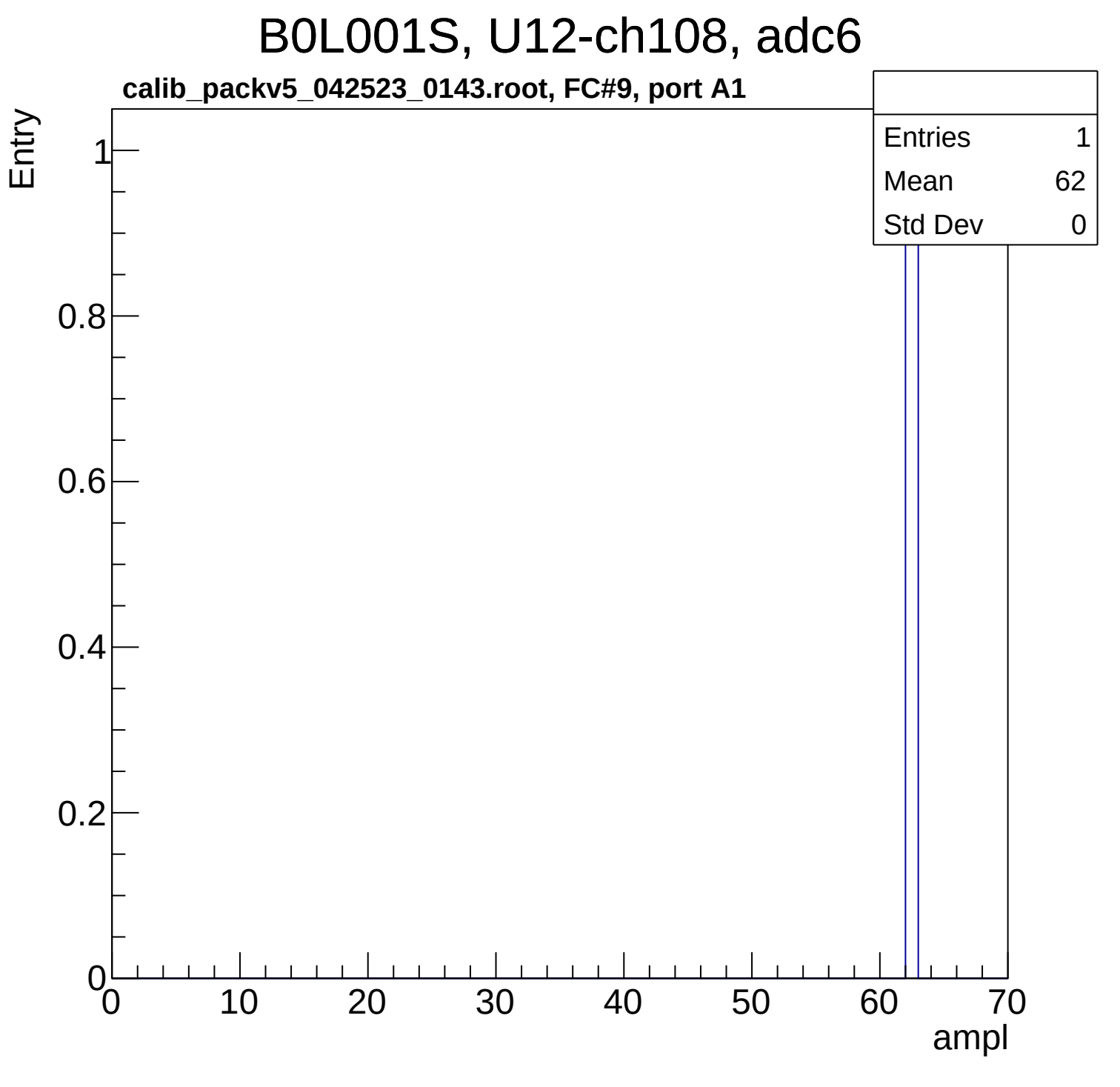
B0L001S, U12-ch108, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 62
Std Dev 0
Entry
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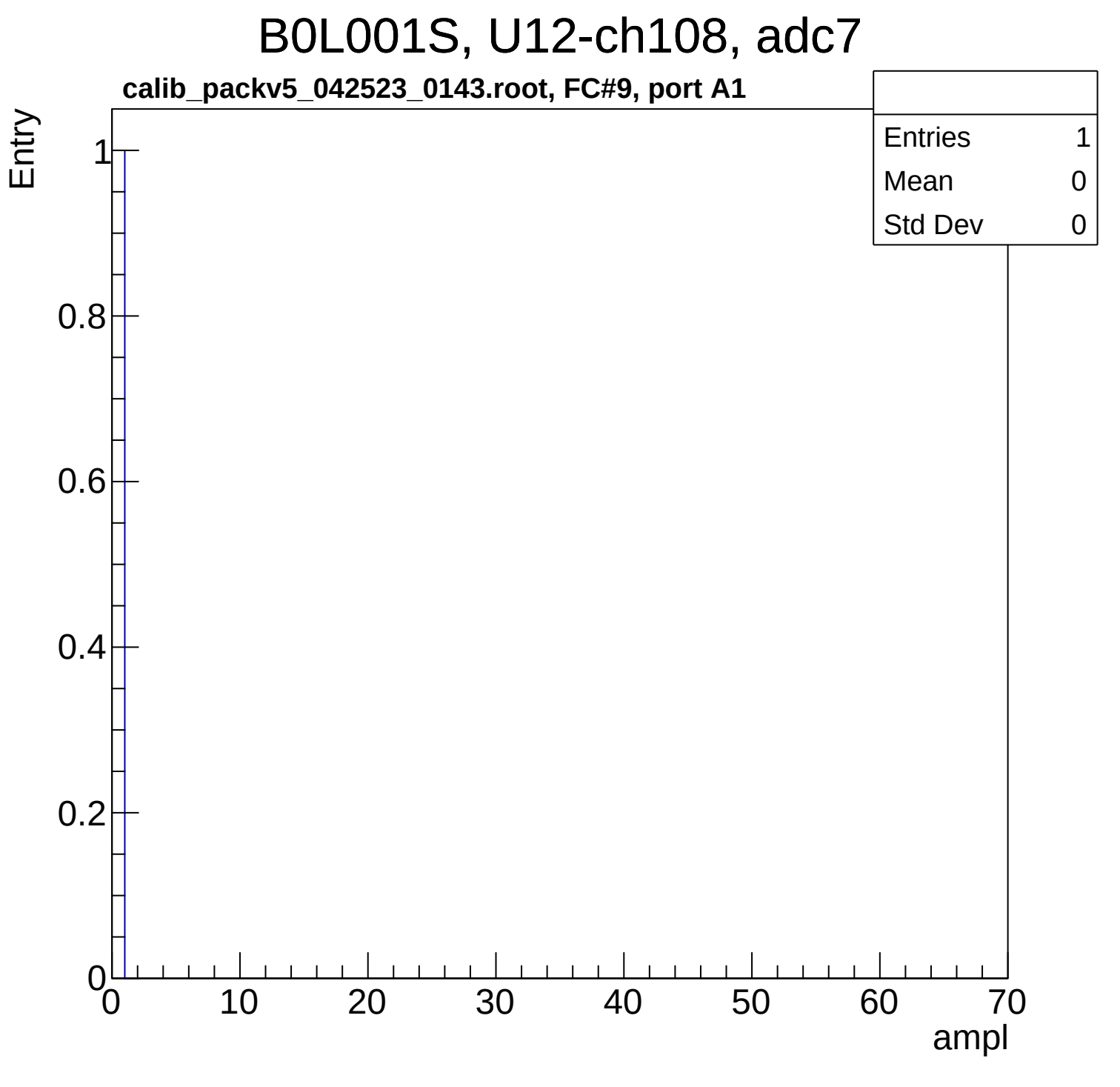
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch108, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 0
Std Dev 0
Entry
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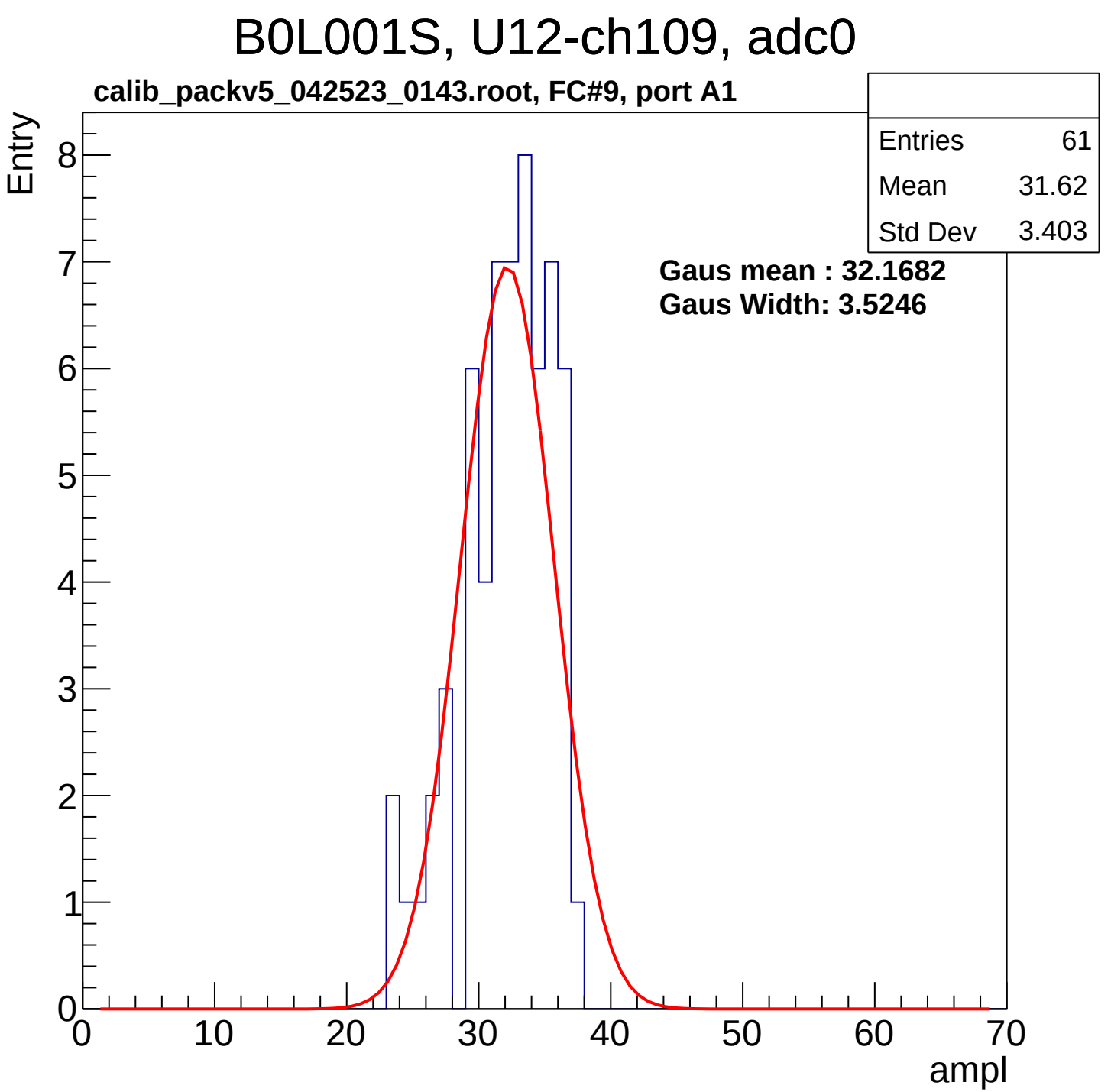
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch109, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 61
Mean 31.62
Std Dev 3.403
Gaus mean : 32.1682
Gaus Width: 3.5246
Entry
ampl
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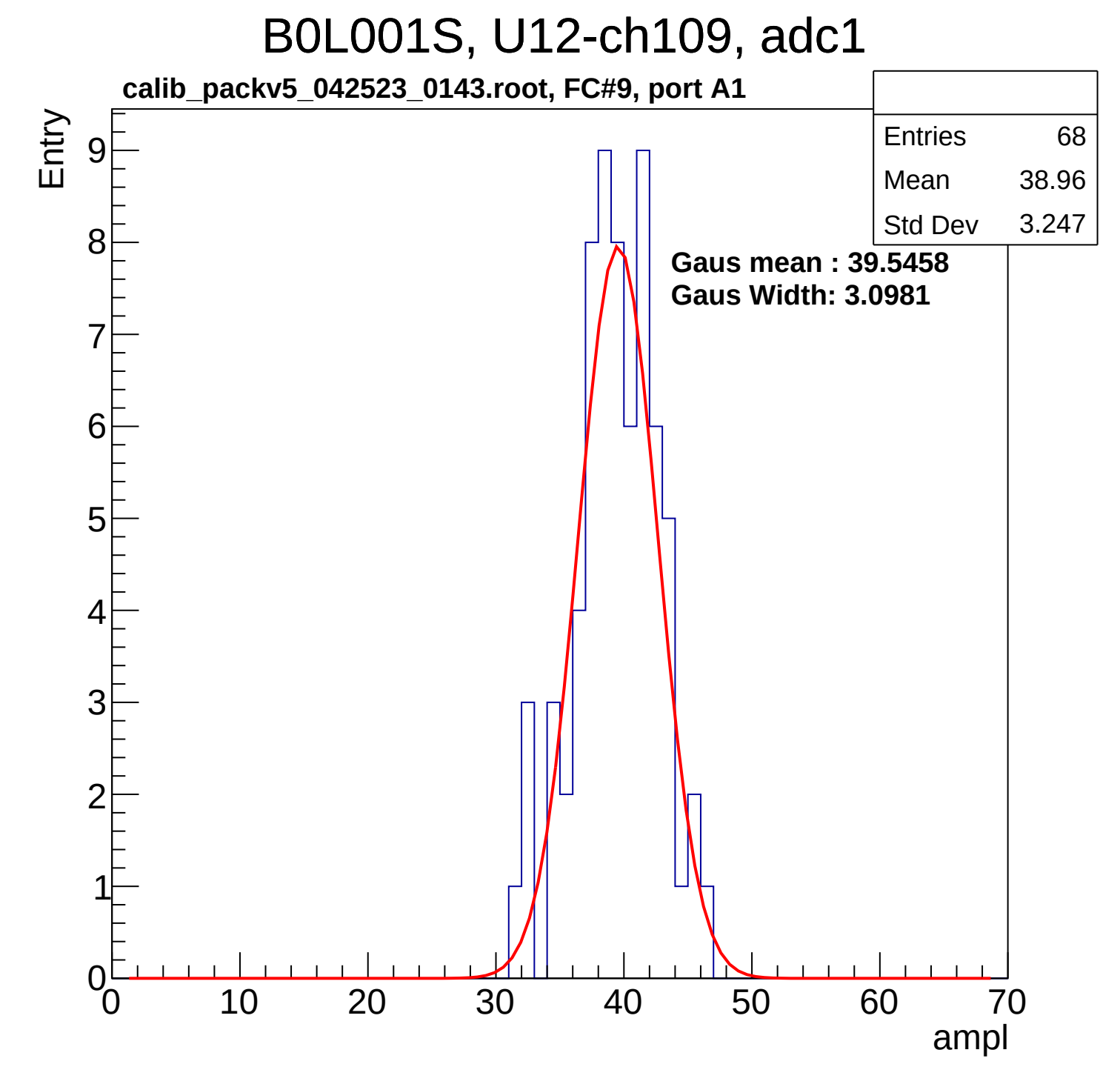
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch109, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 68
Mean 38.96
Std Dev 3.247
Gaus mean : 39.5458
Gaus Width: 3.0981
Entry
ampl
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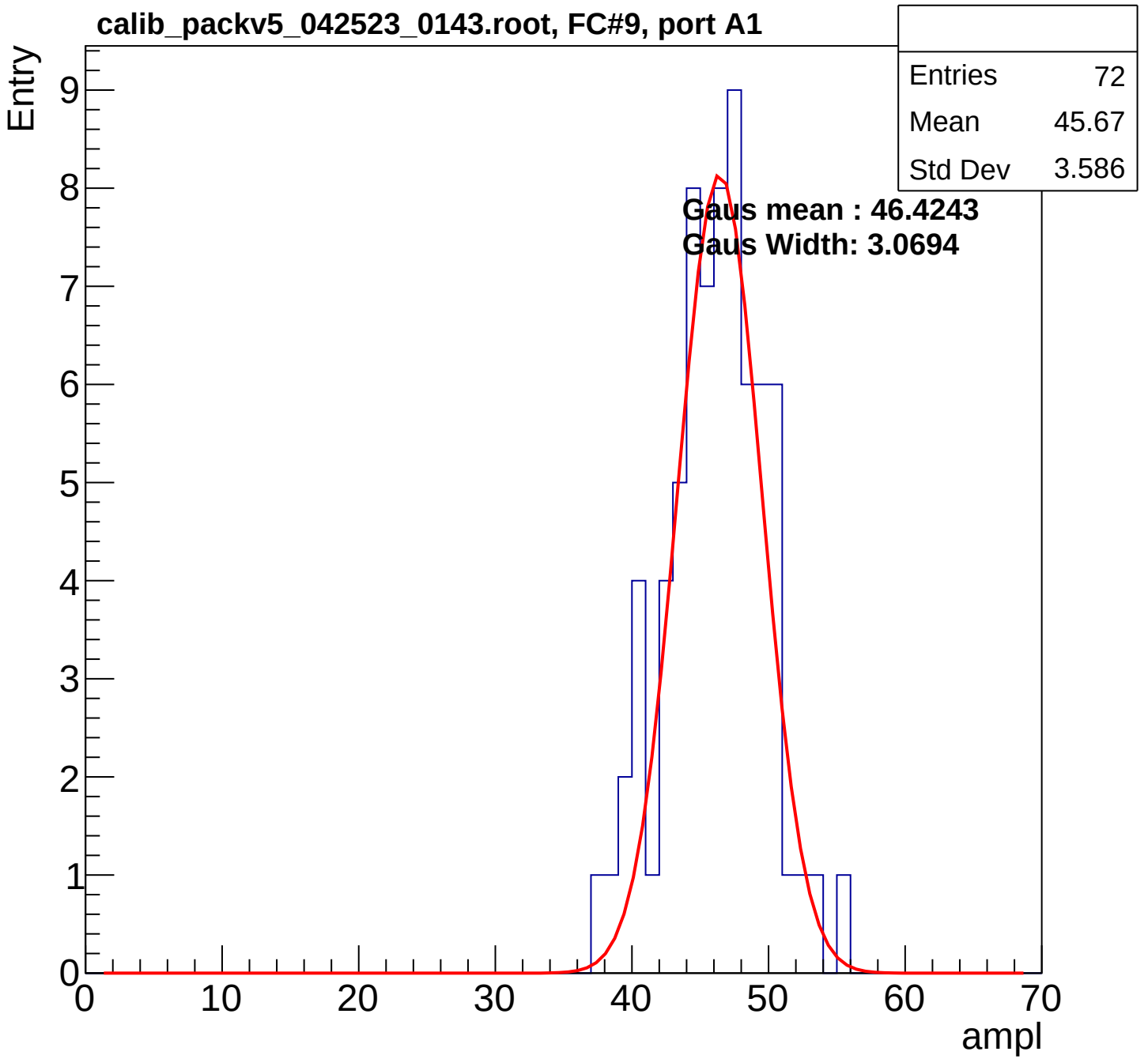
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch109, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 72
Mean 45.67
Std Dev 3.586
Gaus mean : 46.4243
Gaus Width: 3.0694
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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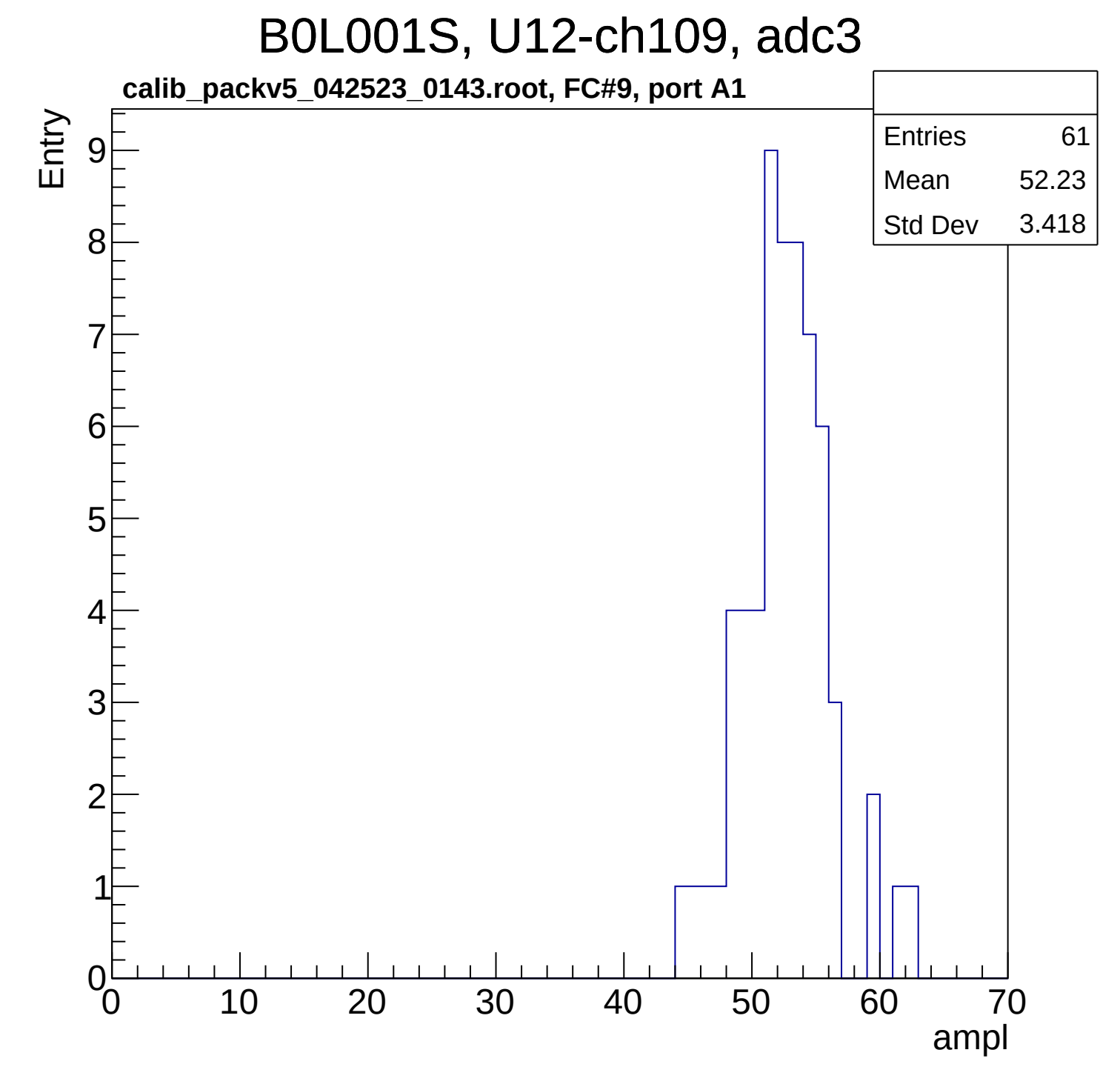
B0L001S, U12-ch109, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 61
Mean 52.23
Std Dev 3.418
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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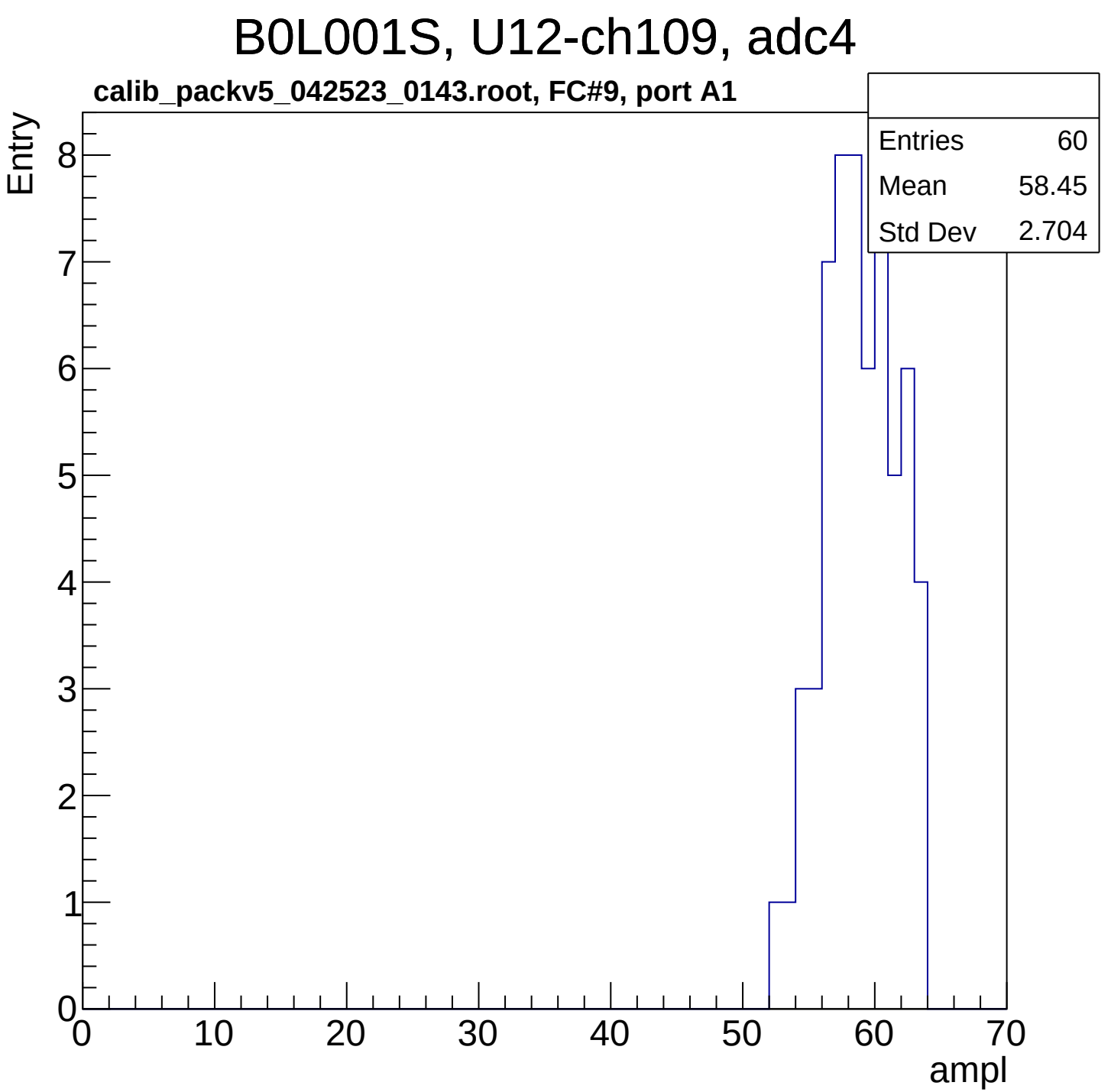
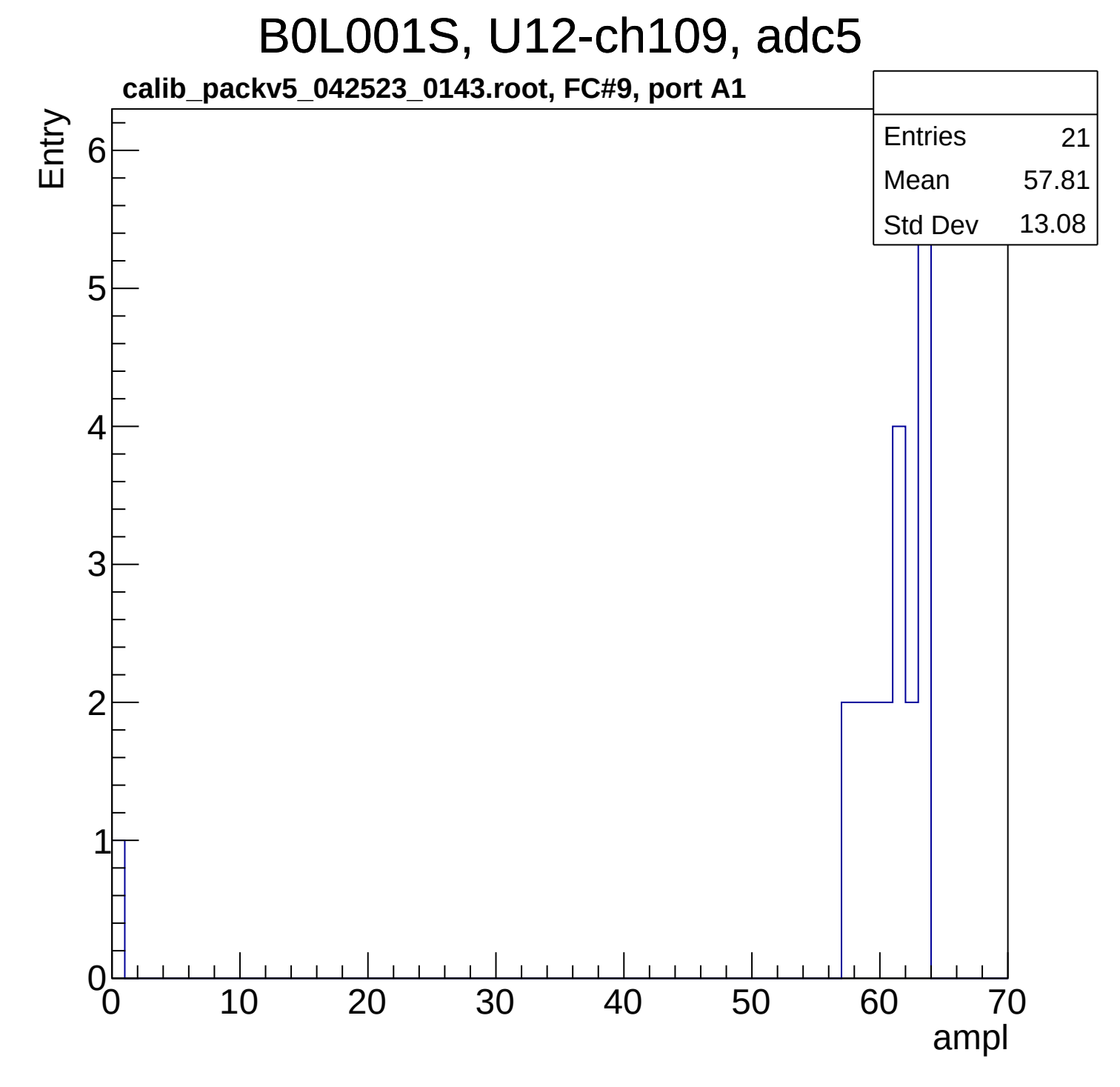
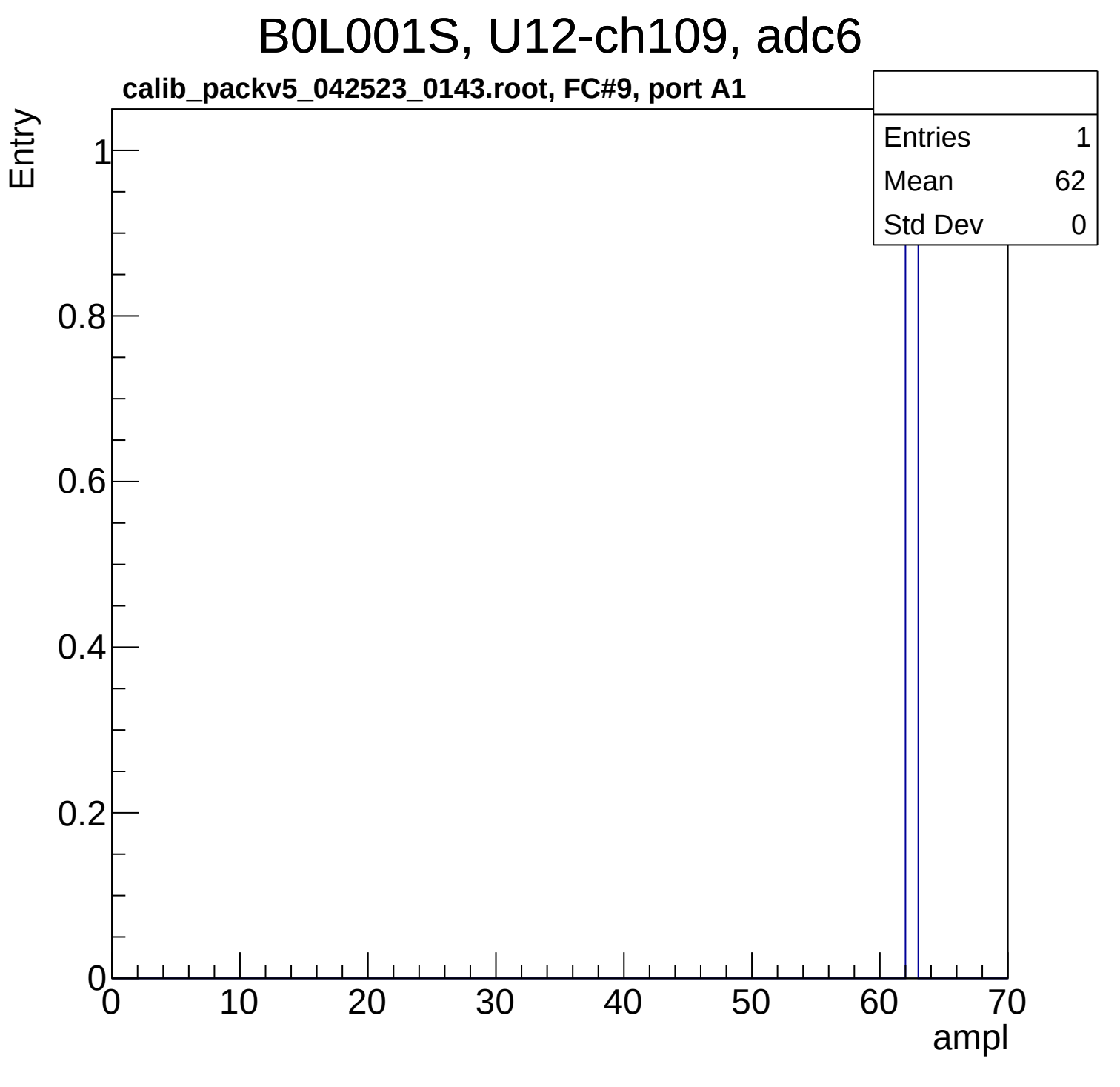
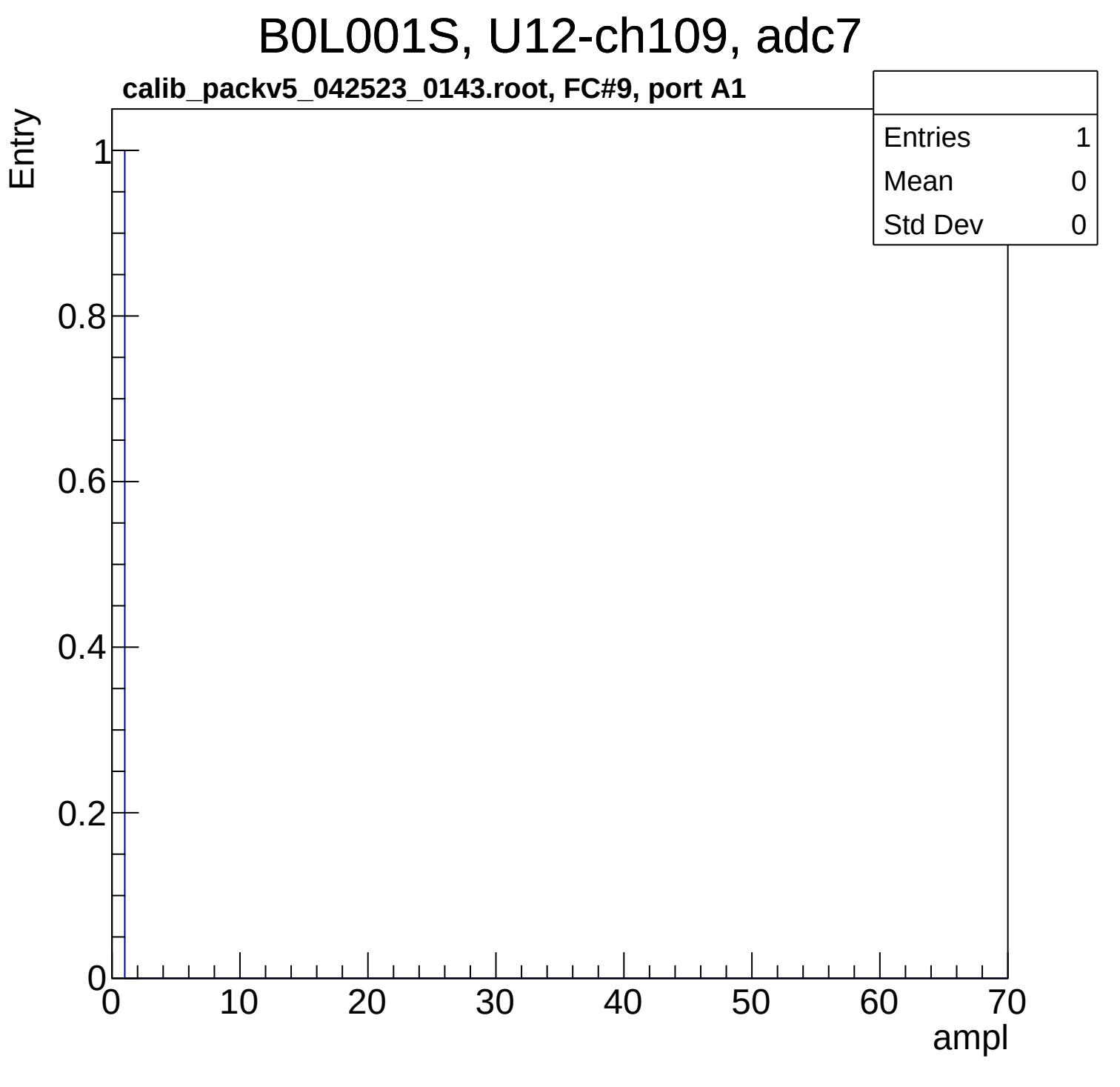
60
70


B0L001S, U12-ch109, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 60
Mean 58.45
Std Dev 2.704
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch109, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 21
Mean 57.81
Std Dev 13.08
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch109, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch109, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 0
Std Dev 0
Entry
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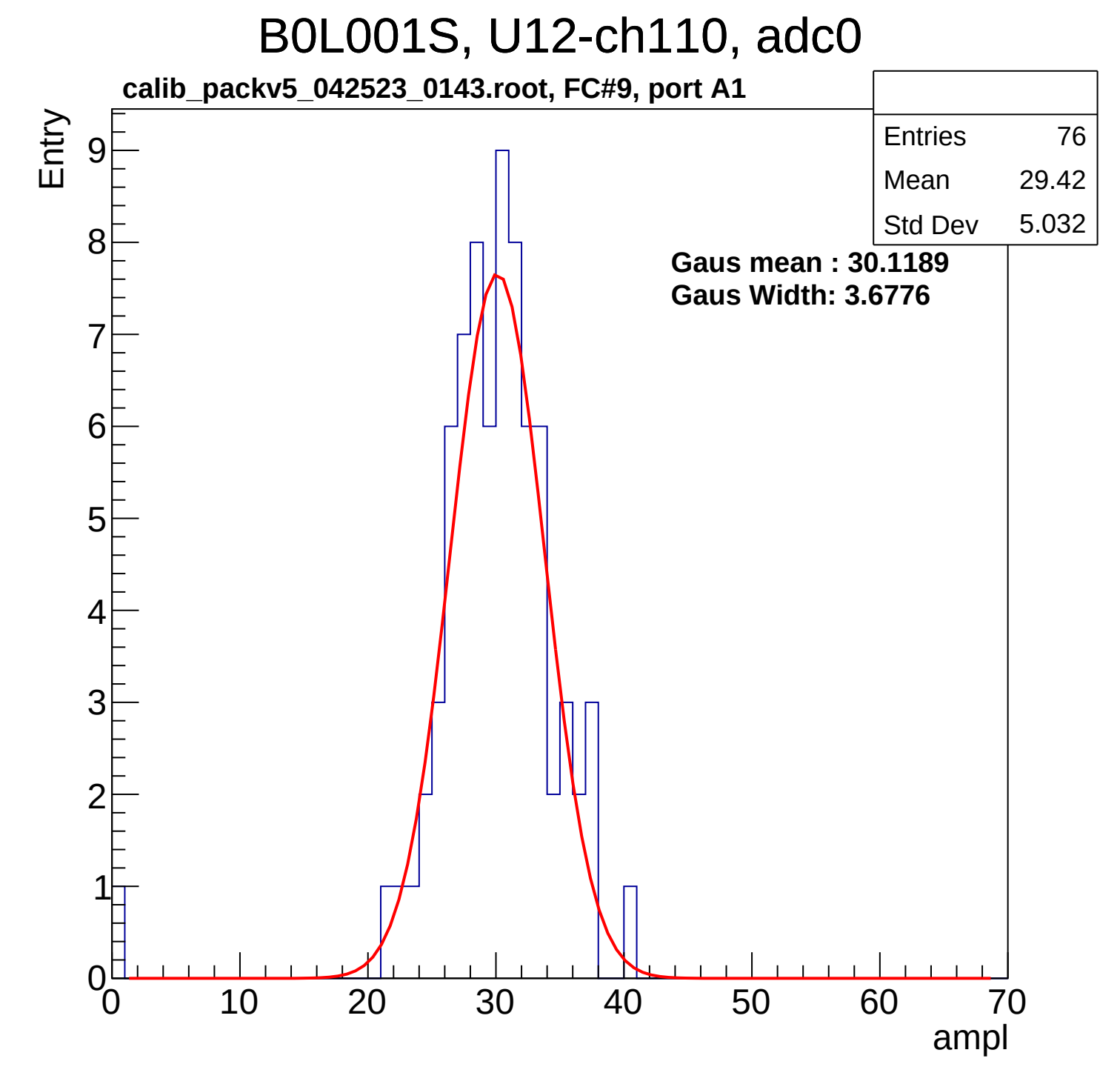
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch110, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 76
Mean 29.42
Std Dev 5.032
Gaus mean : 30.1189
Gaus Width: 3.6776
Entry
ampl
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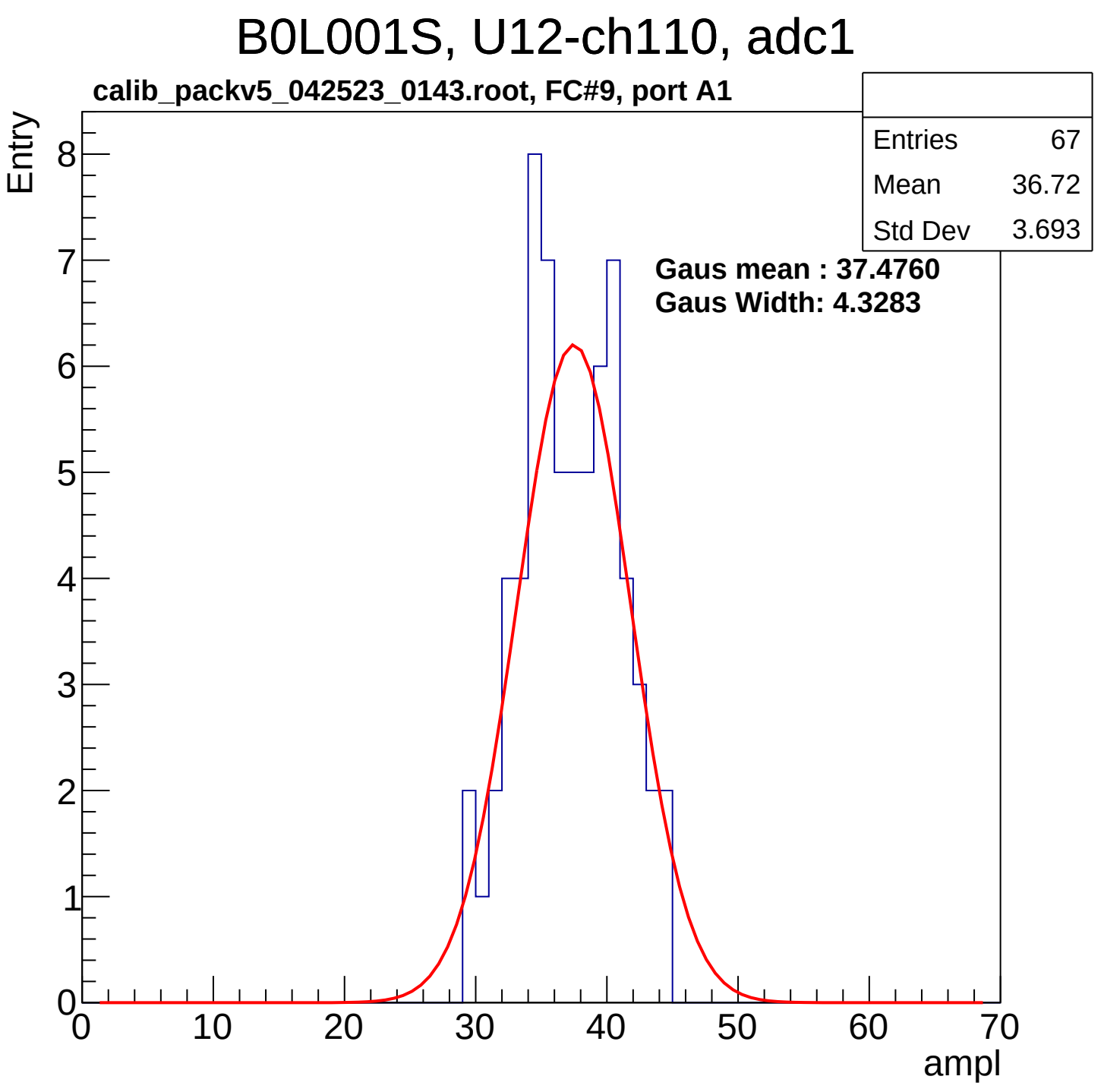
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch110, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 67
Mean 36.72
Std Dev 3.693
Gaus mean : 37.4760
Gaus Width: 4.3283
Entry
ampl
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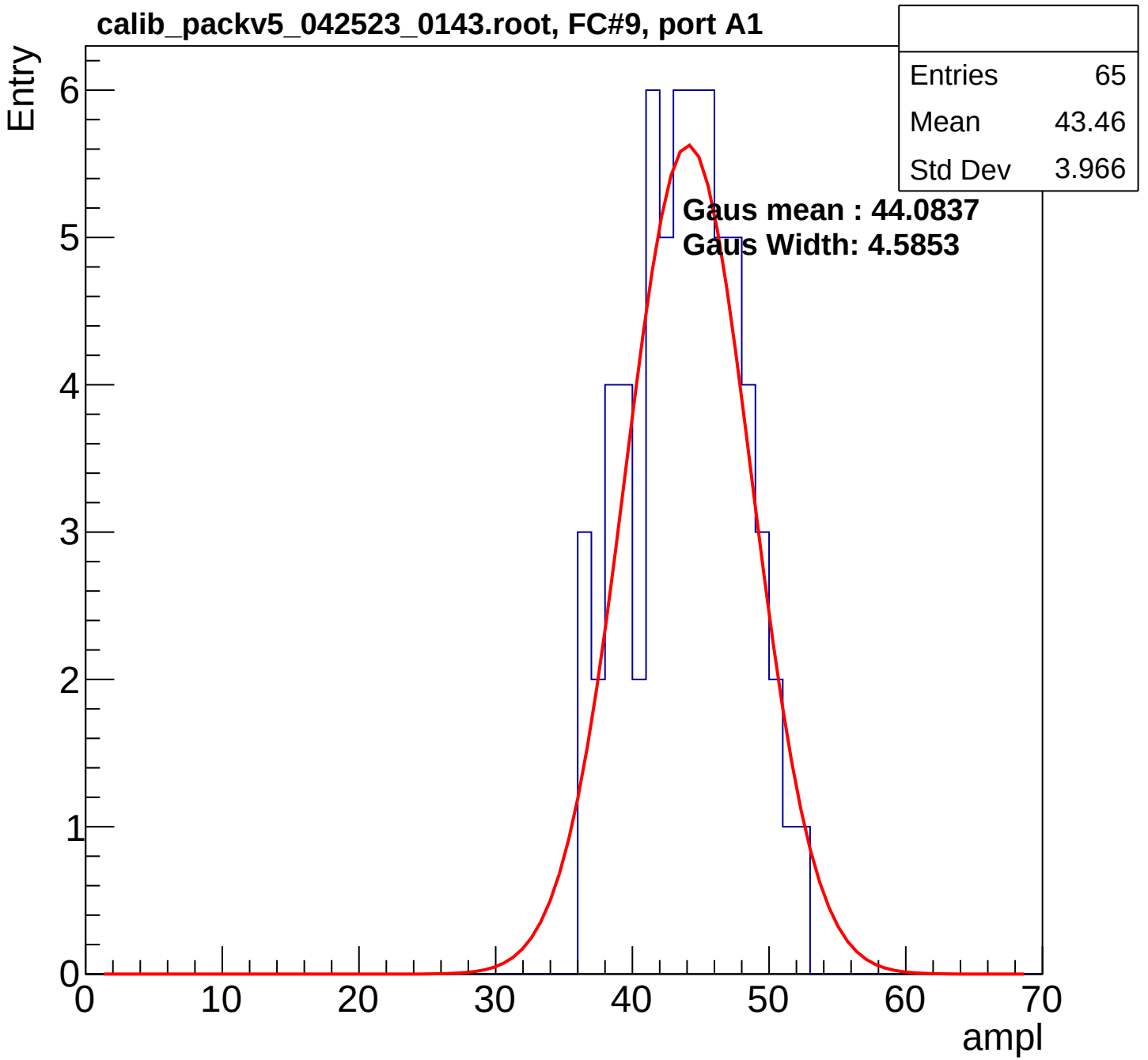
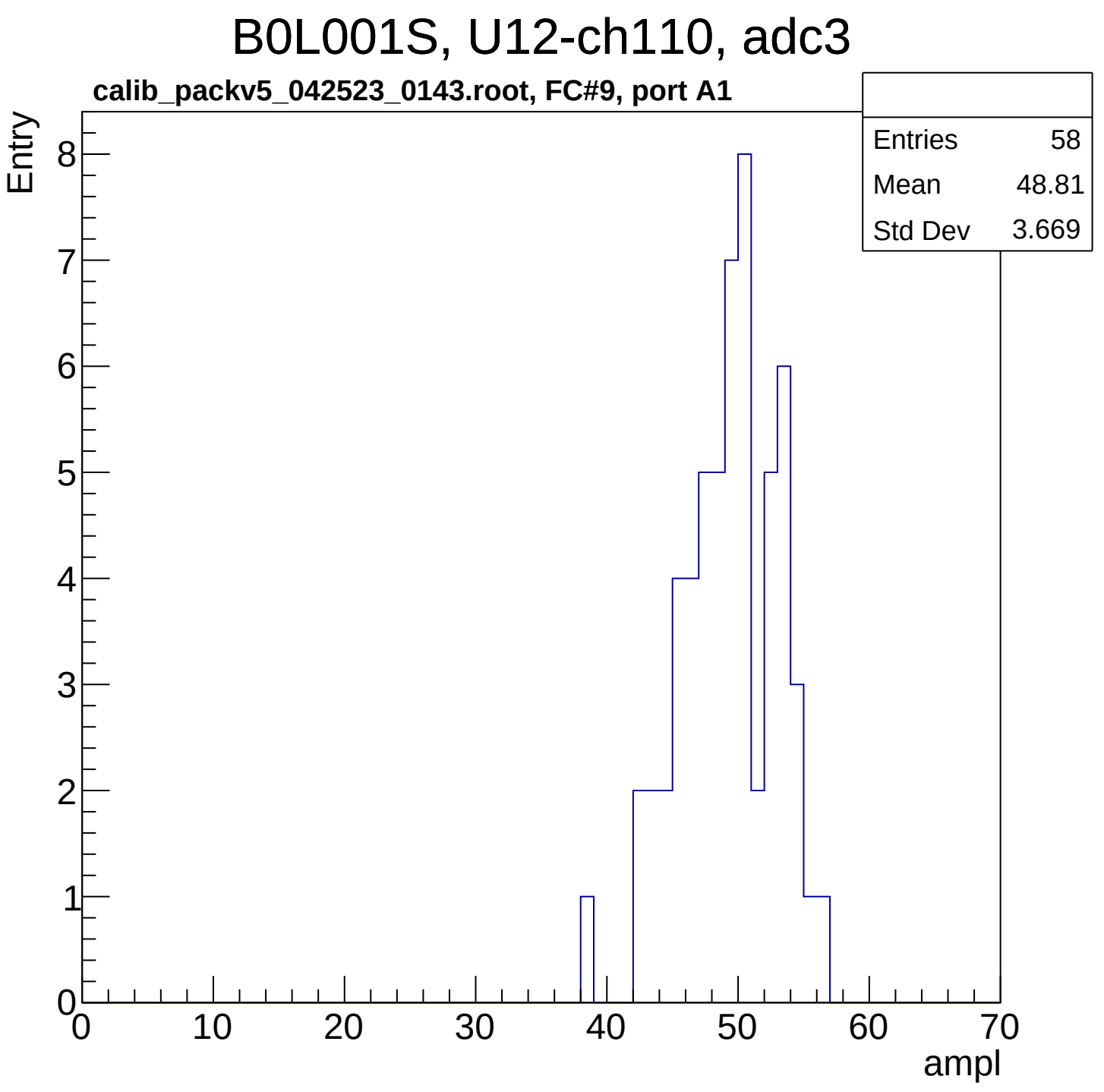
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch110, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 65
Mean 43.46
Std Dev 3.966
Gaus mean : 44.0837
Gaus Width: 4.5853
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B0L001S, U12-ch110, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 58
Mean 48.81
Std Dev 3.669
Entry
ampl
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3
4
5
6
7
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0
10
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60
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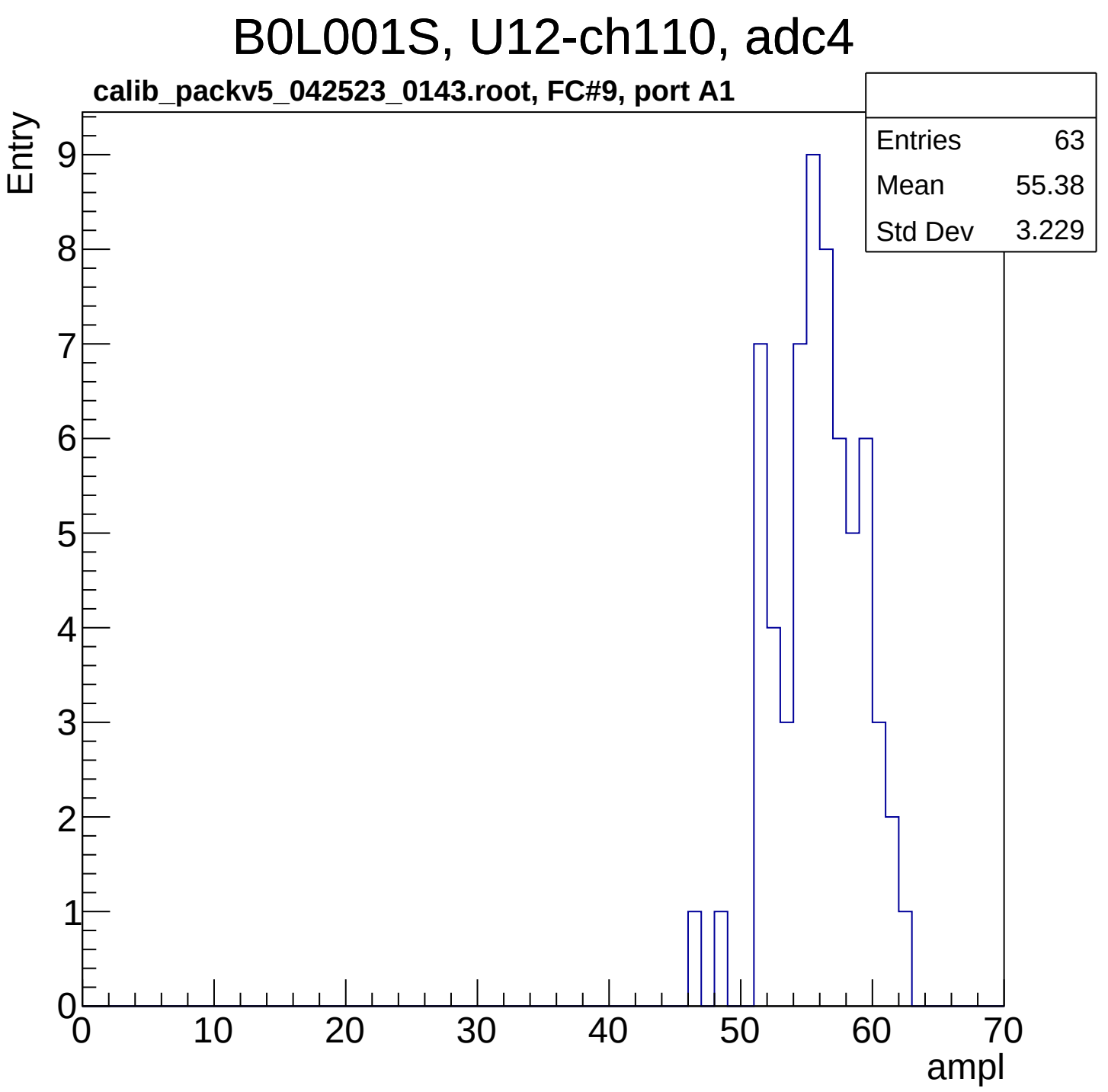
B0L001S, U12-ch110, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 63
Mean 55.38
Std Dev 3.229
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
50
60
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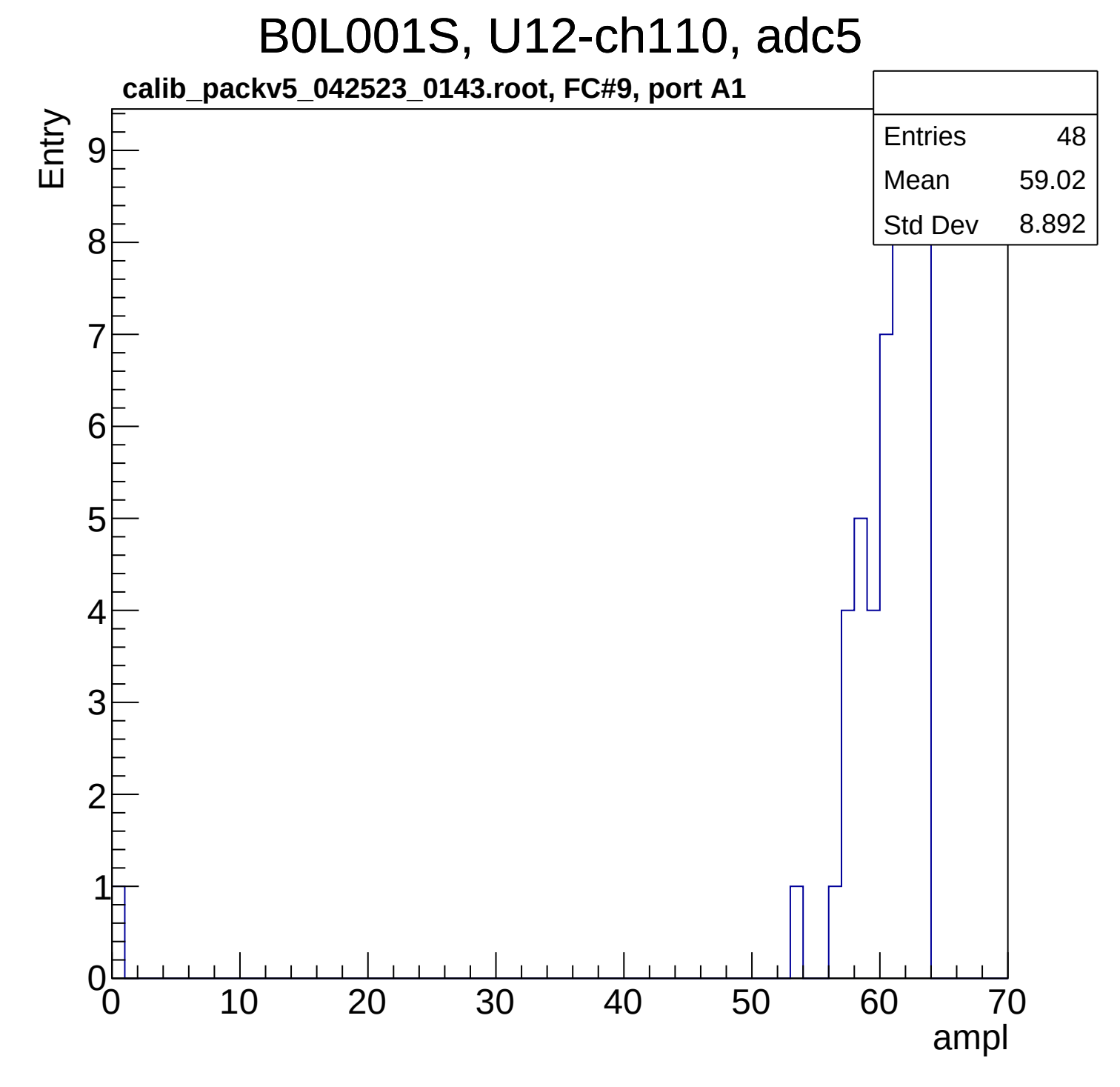
B0L001S, U12-ch110, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 48
Mean 59.02
Std Dev 8.892
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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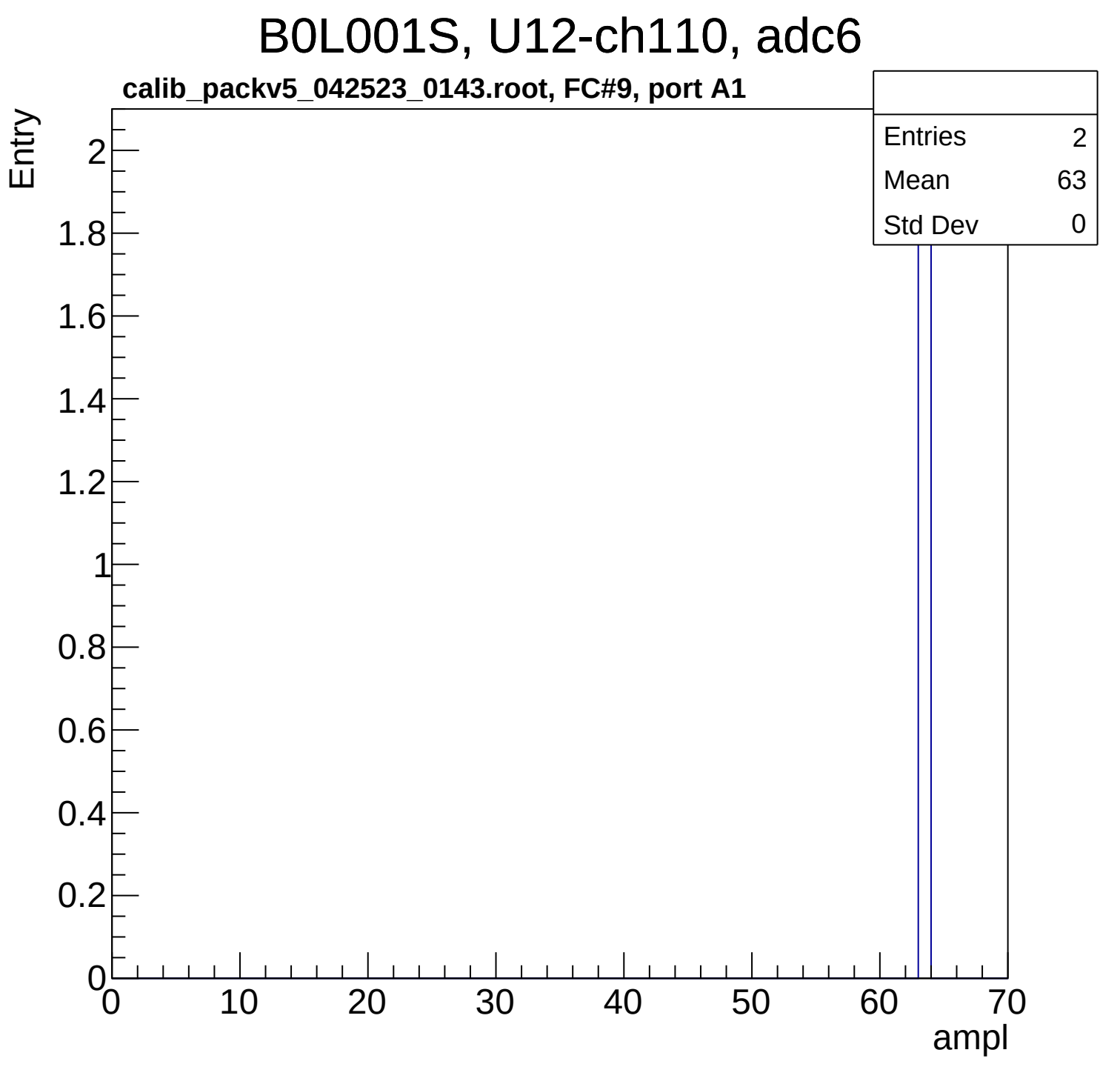
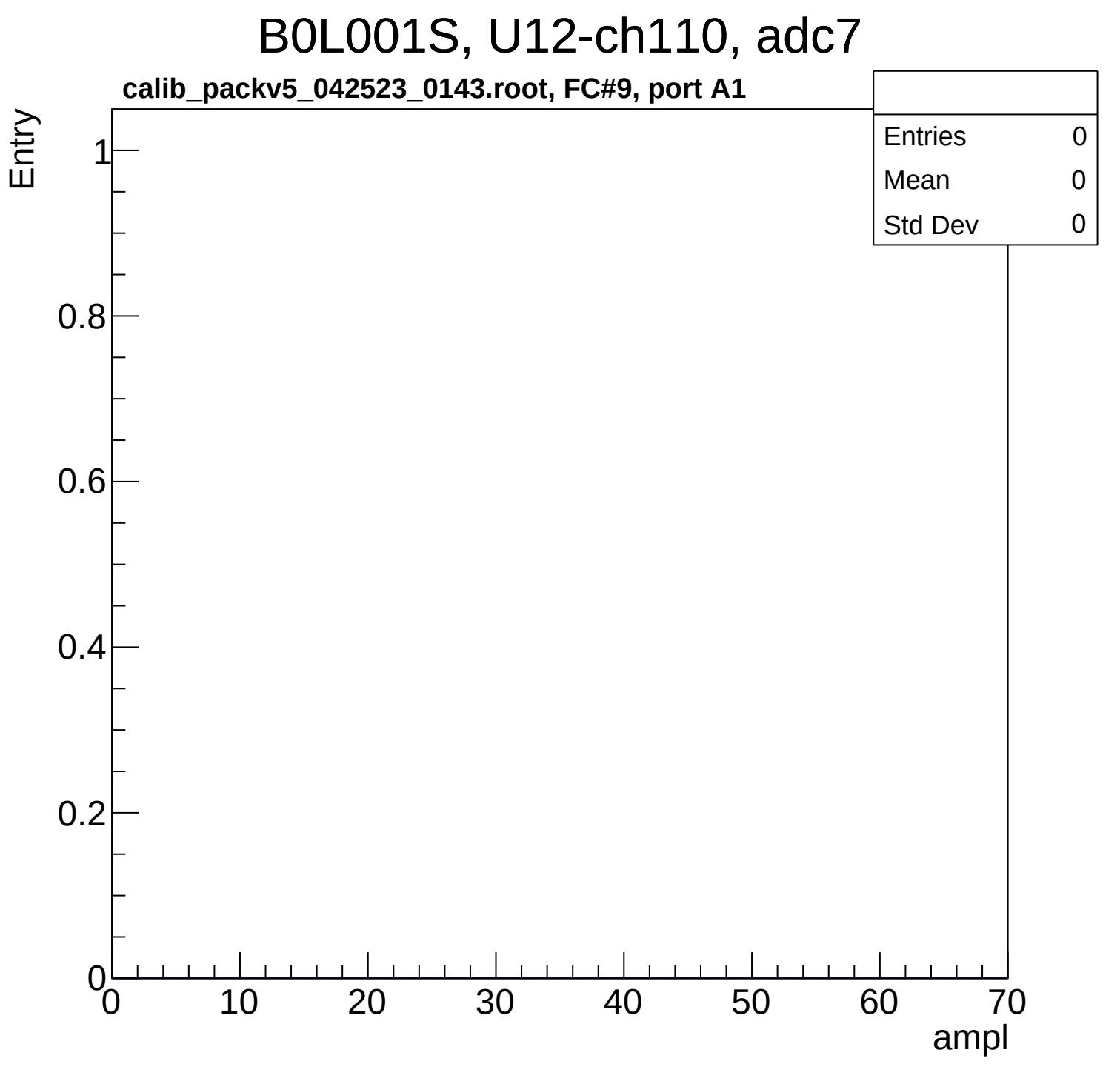

B0L001S, U12-ch110, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L001S, U12-ch110, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
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0.6
0.4
0.2
0
0
10
20
30
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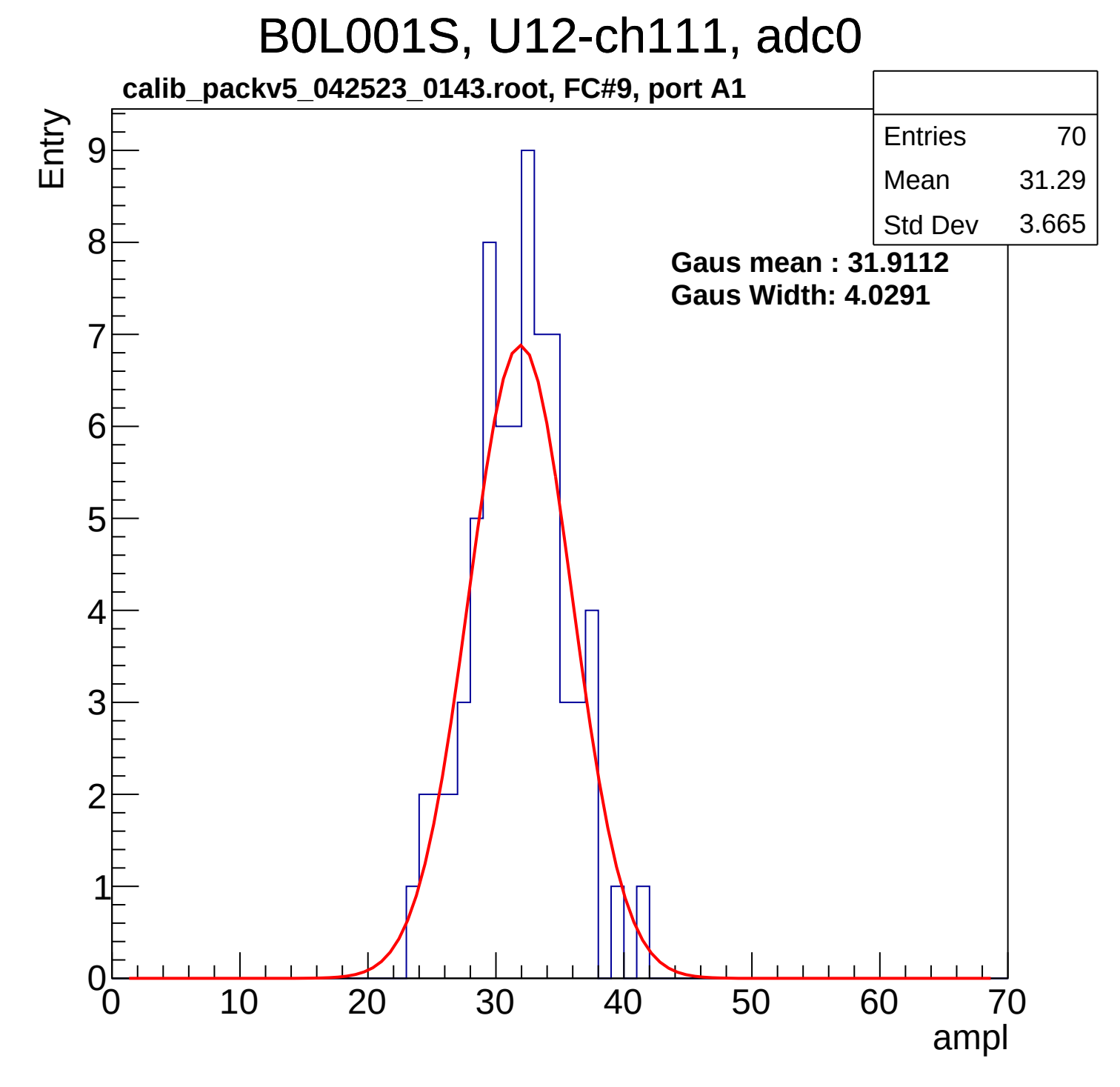
50
60
70
ampl


B0L001S, U12-ch111, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 70
Mean 31.29
Std Dev 3.665
Gaus mean : 31.9112
Gaus Width: 4.0291
Entry
ampl
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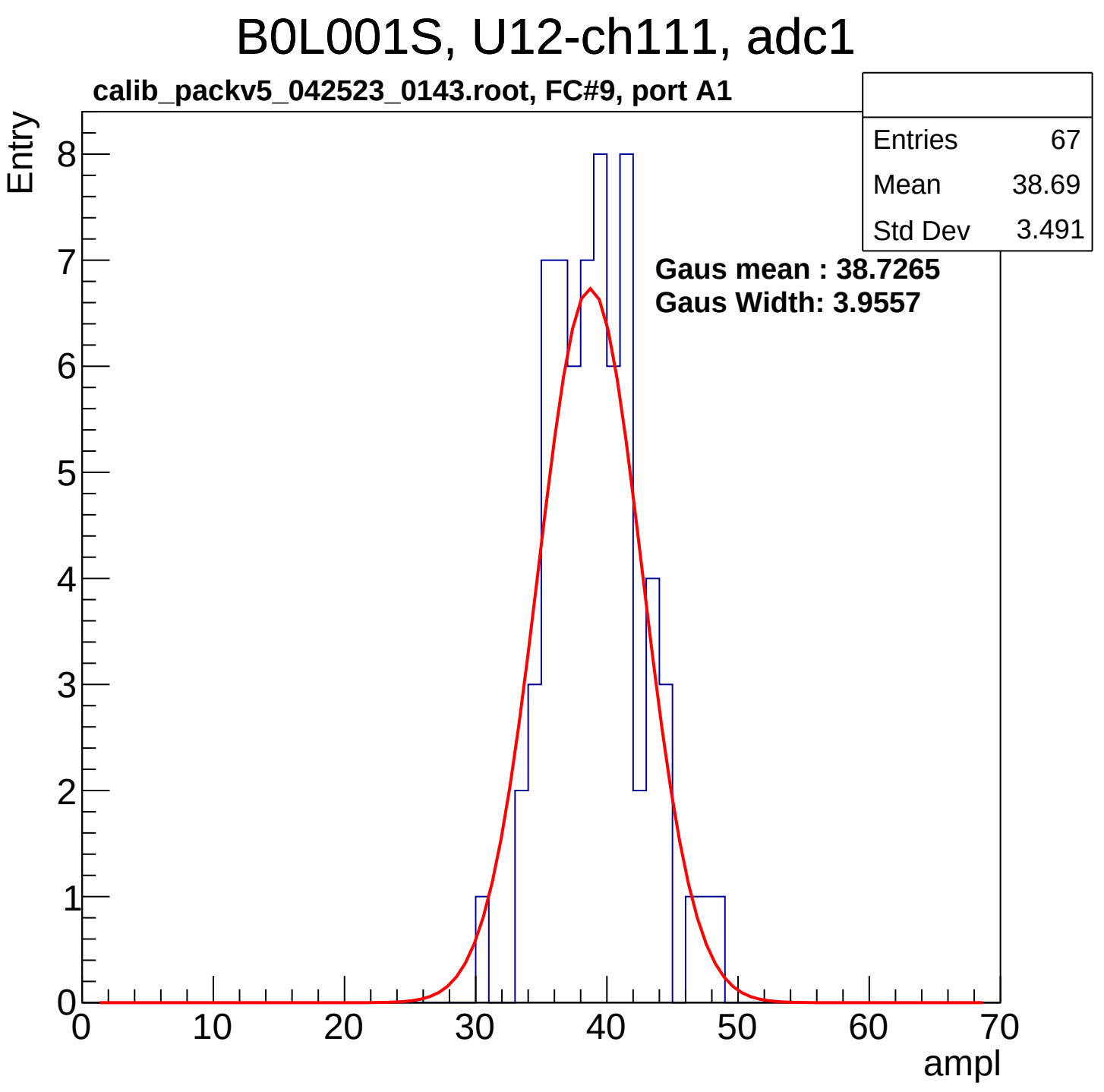
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch111, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 67
Mean 38.69
Std Dev 3.491
Gaus mean : 38.7265
Gaus Width: 3.9557
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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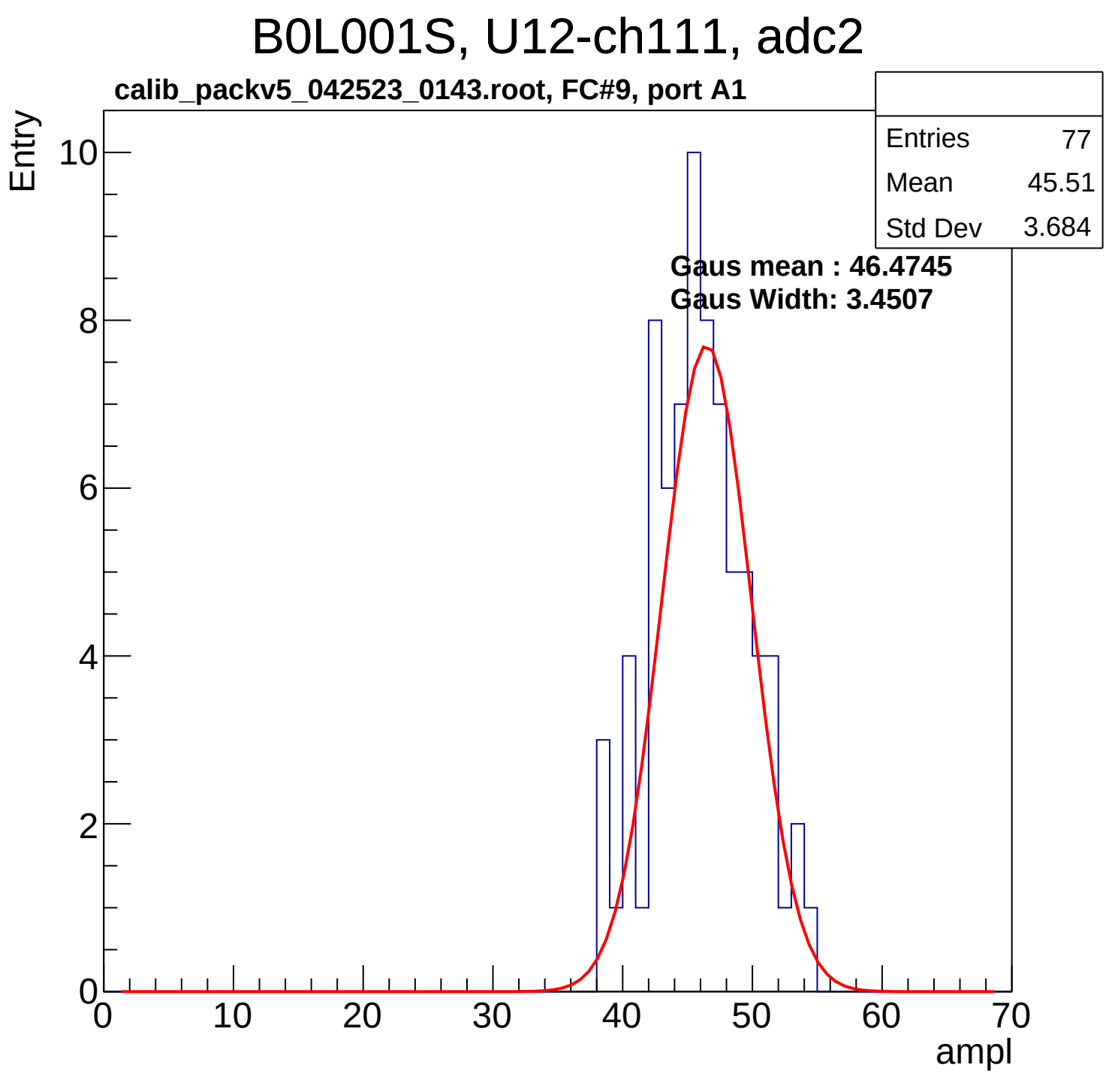
B0L001S, U12-ch111, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 77
Mean 45.51
Std Dev 3.684
Gaus mean : 46.4745
Gaus Width: 3.4507
Entry
ampl
0
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4
6
8
10
0
10
20
30
40
50
60
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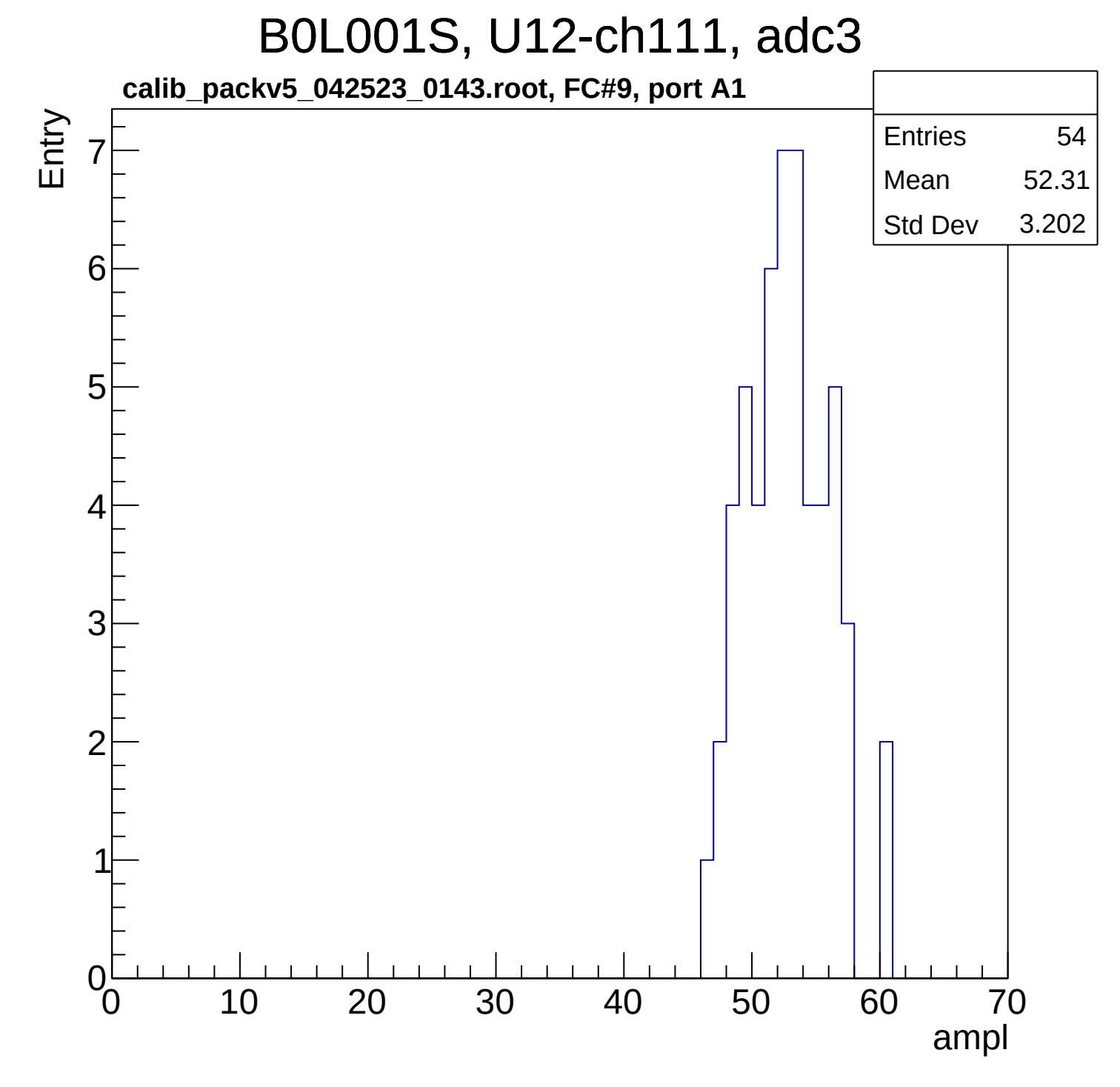
B0L001S, U12-ch111, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 54
Mean 52.31
Std Dev 3.202
Entry
ampl
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2
3
4
5
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7
0
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60
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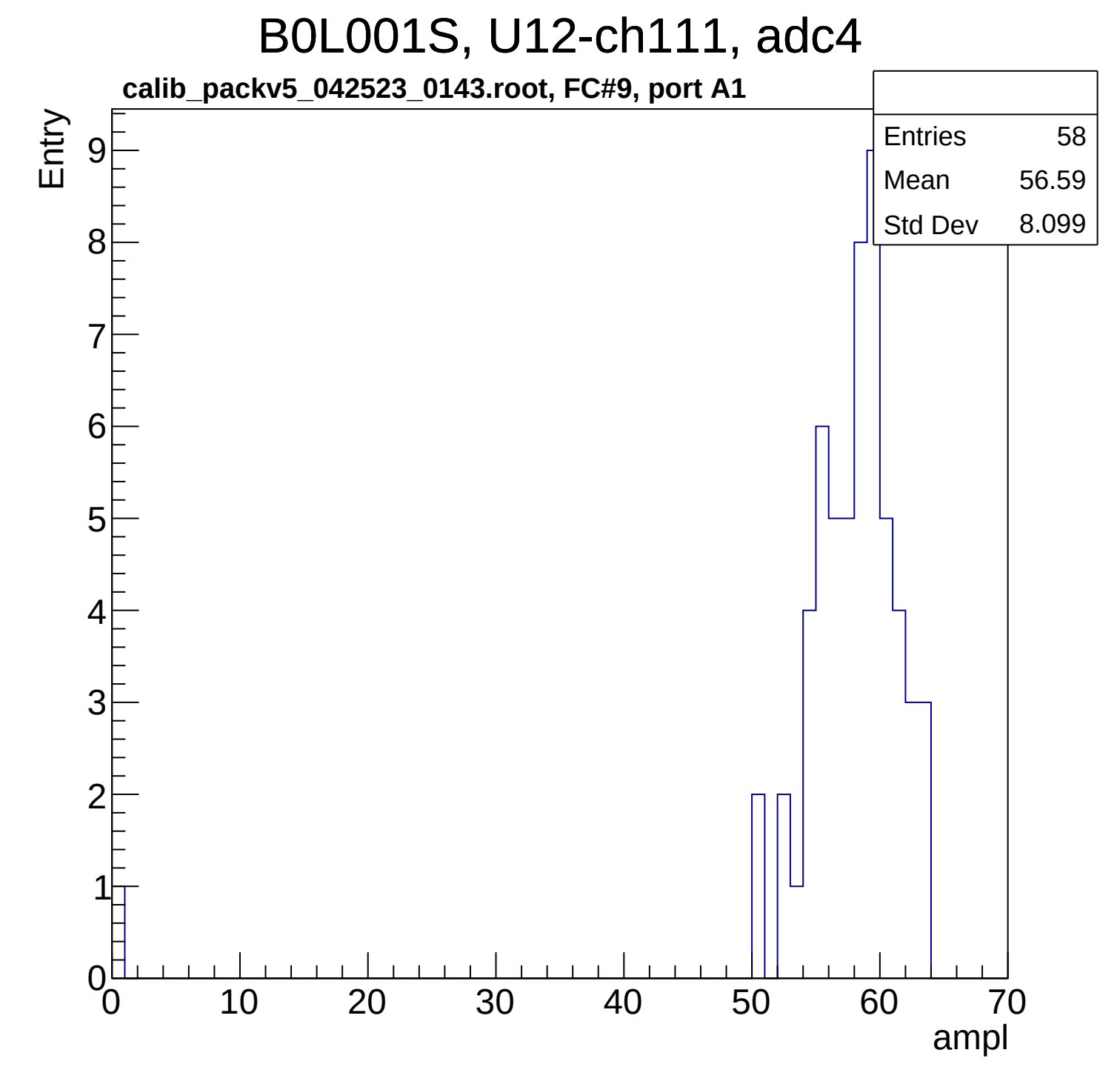
B0L001S, U12-ch111, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 58
Mean 56.59
Std Dev 8.099
Entry
ampl
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2
3
4
5
6
7
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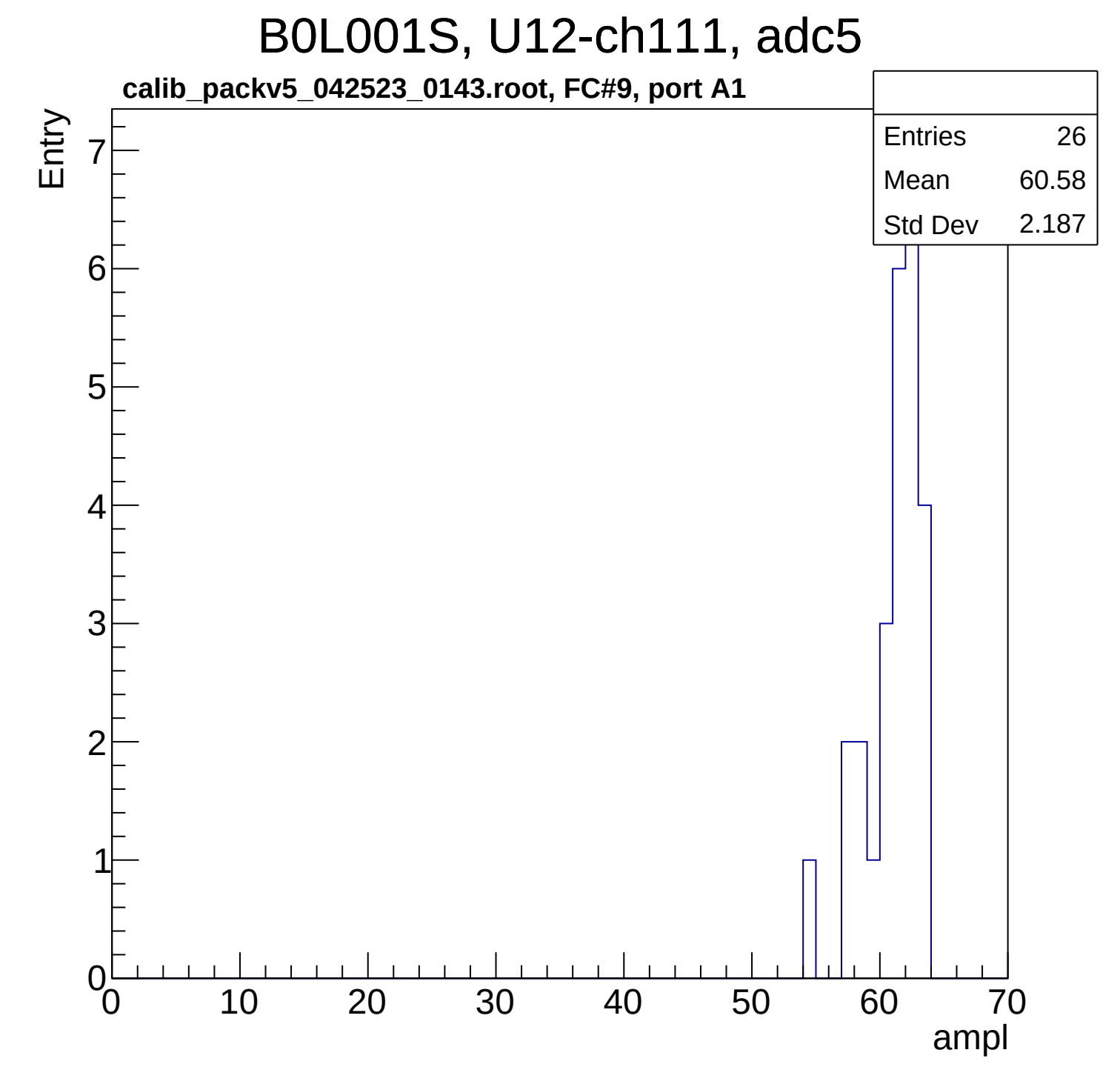
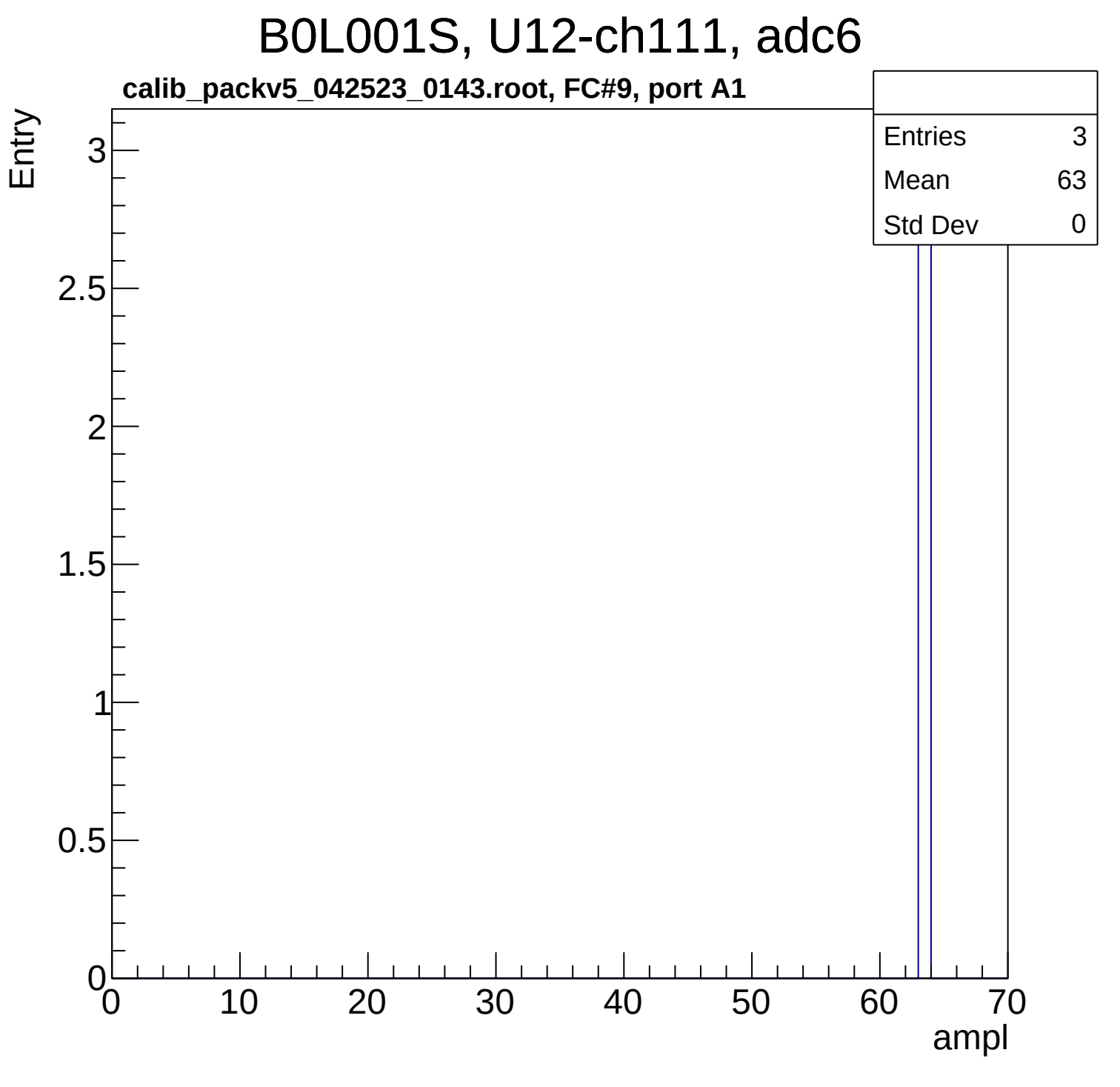
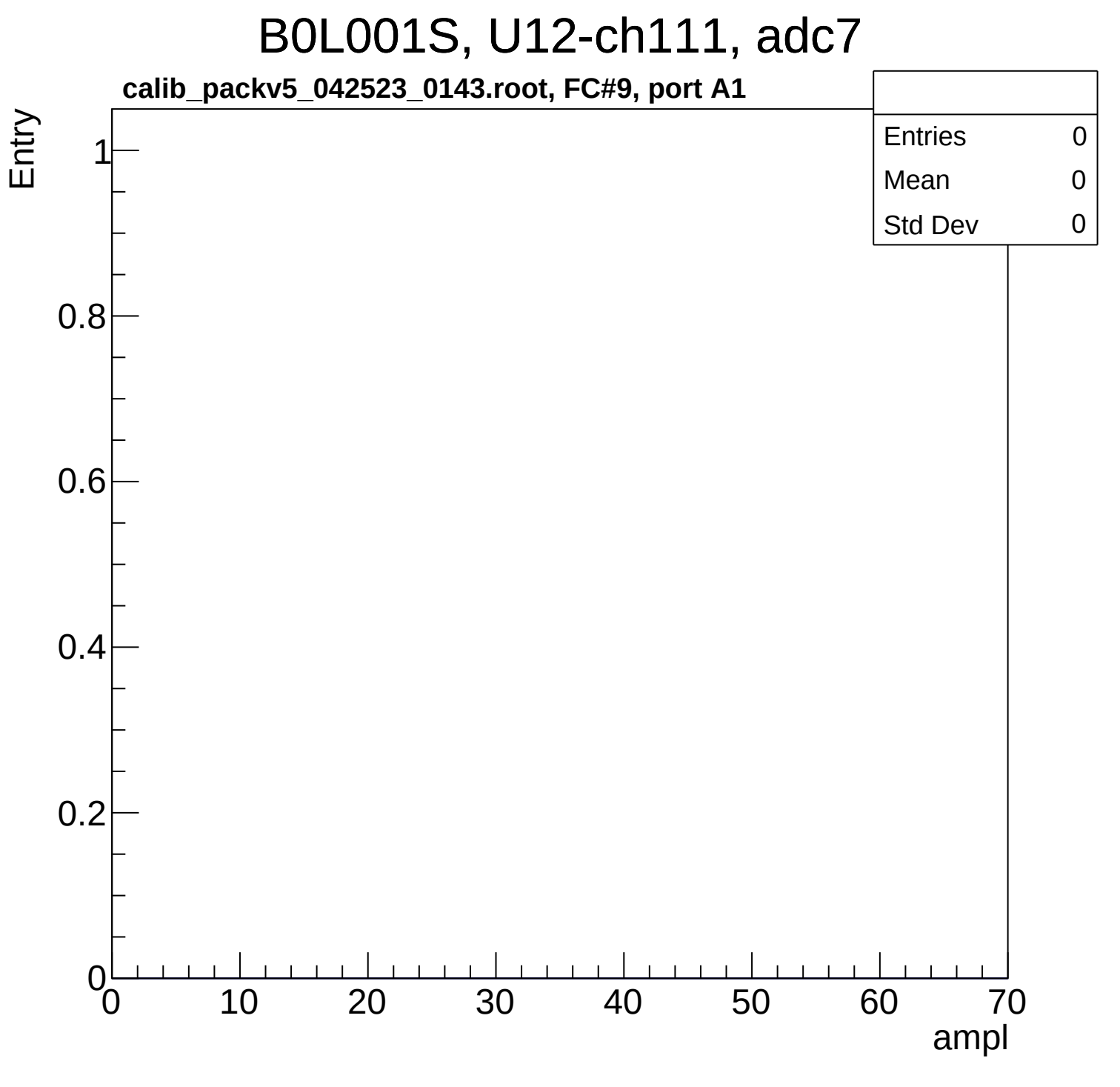
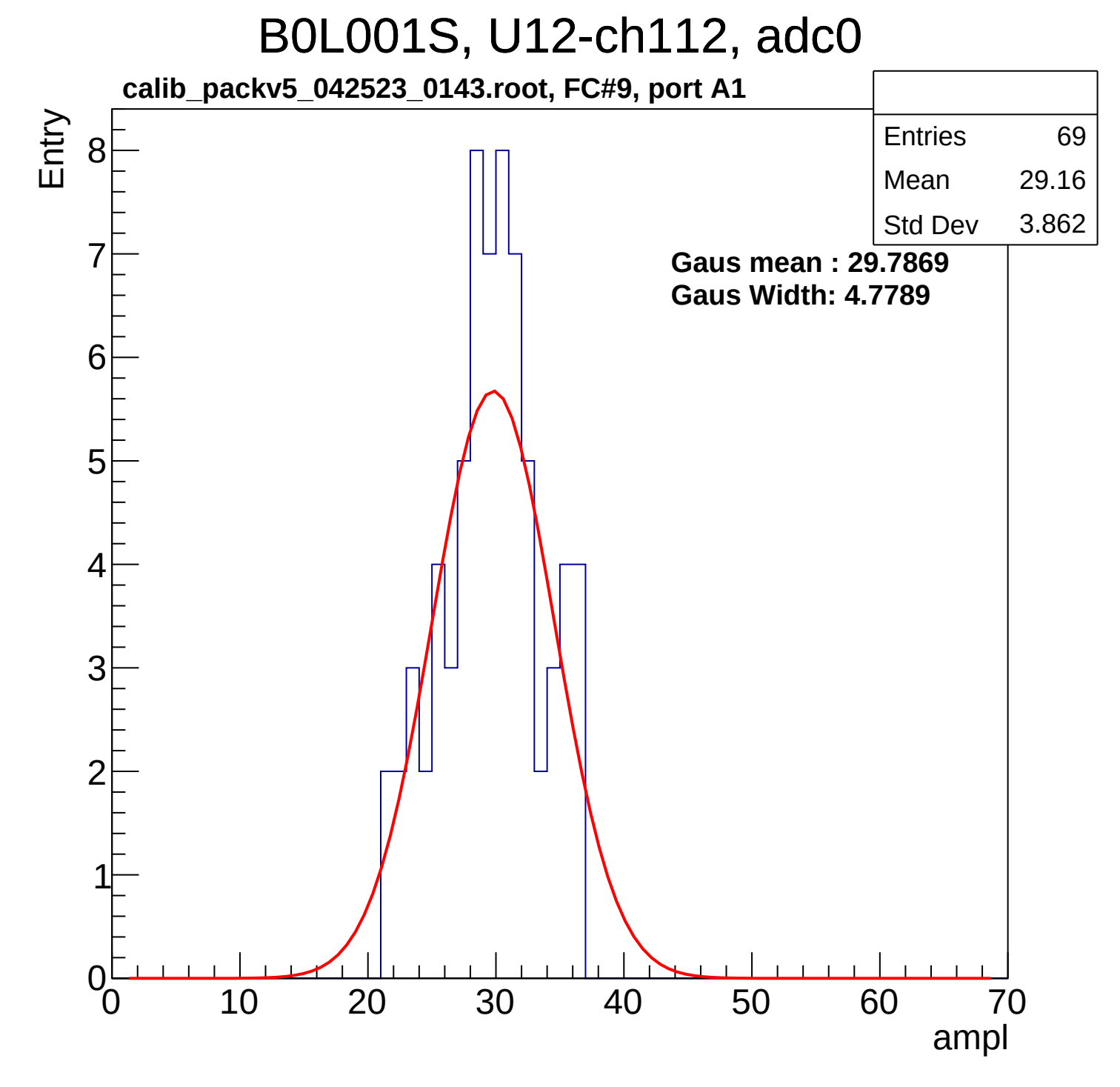

B0L001S, U12-ch111, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 26
Mean 60.58
Std Dev 2.187
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B0L001S, U12-ch111, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 3
Mean 63
Std Dev 0
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B0L001S, U12-ch111, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch112, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 69
Mean 29.16
Std Dev 3.862
Gaus mean : 29.7869
Gaus Width: 4.7789
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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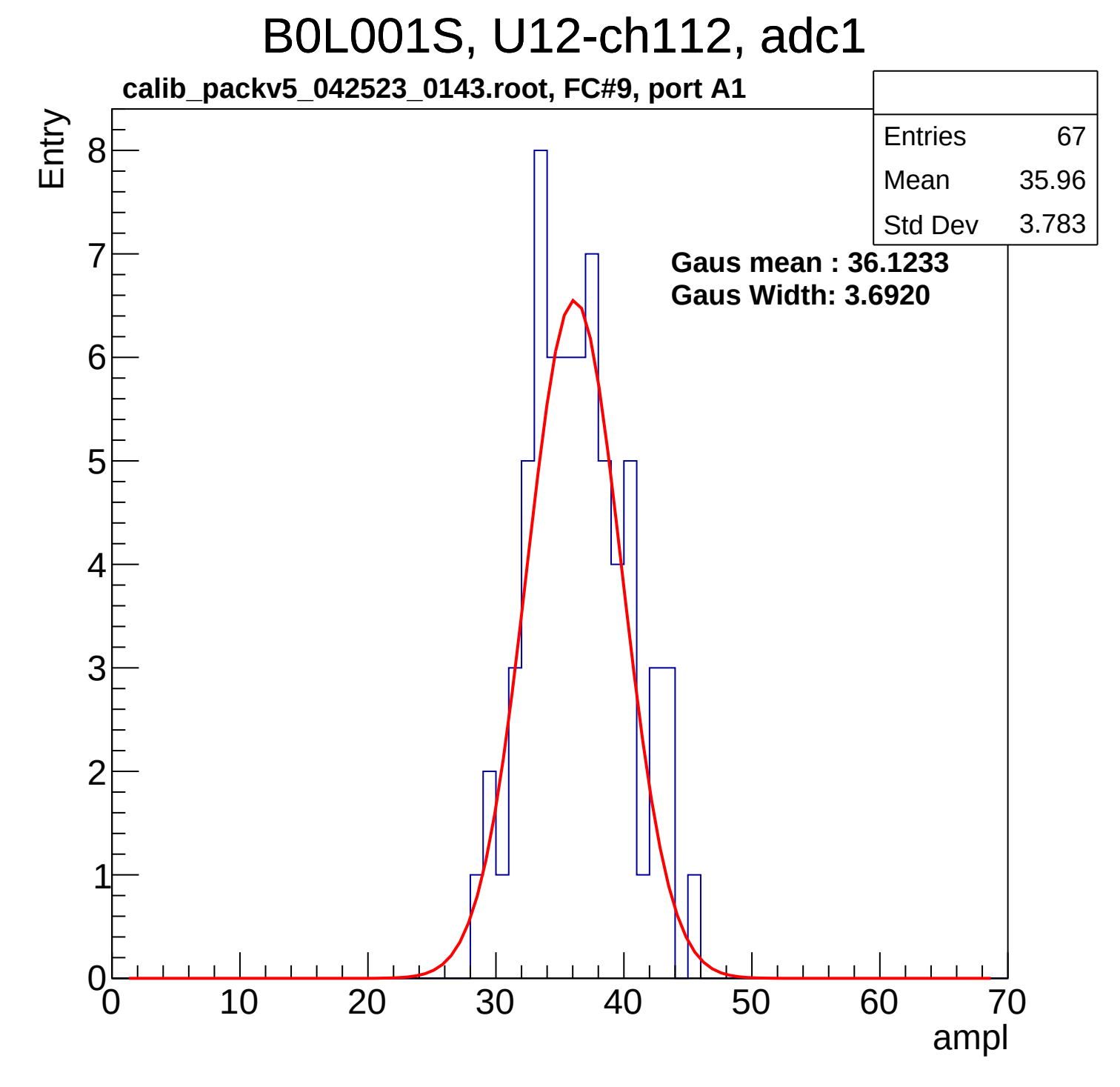
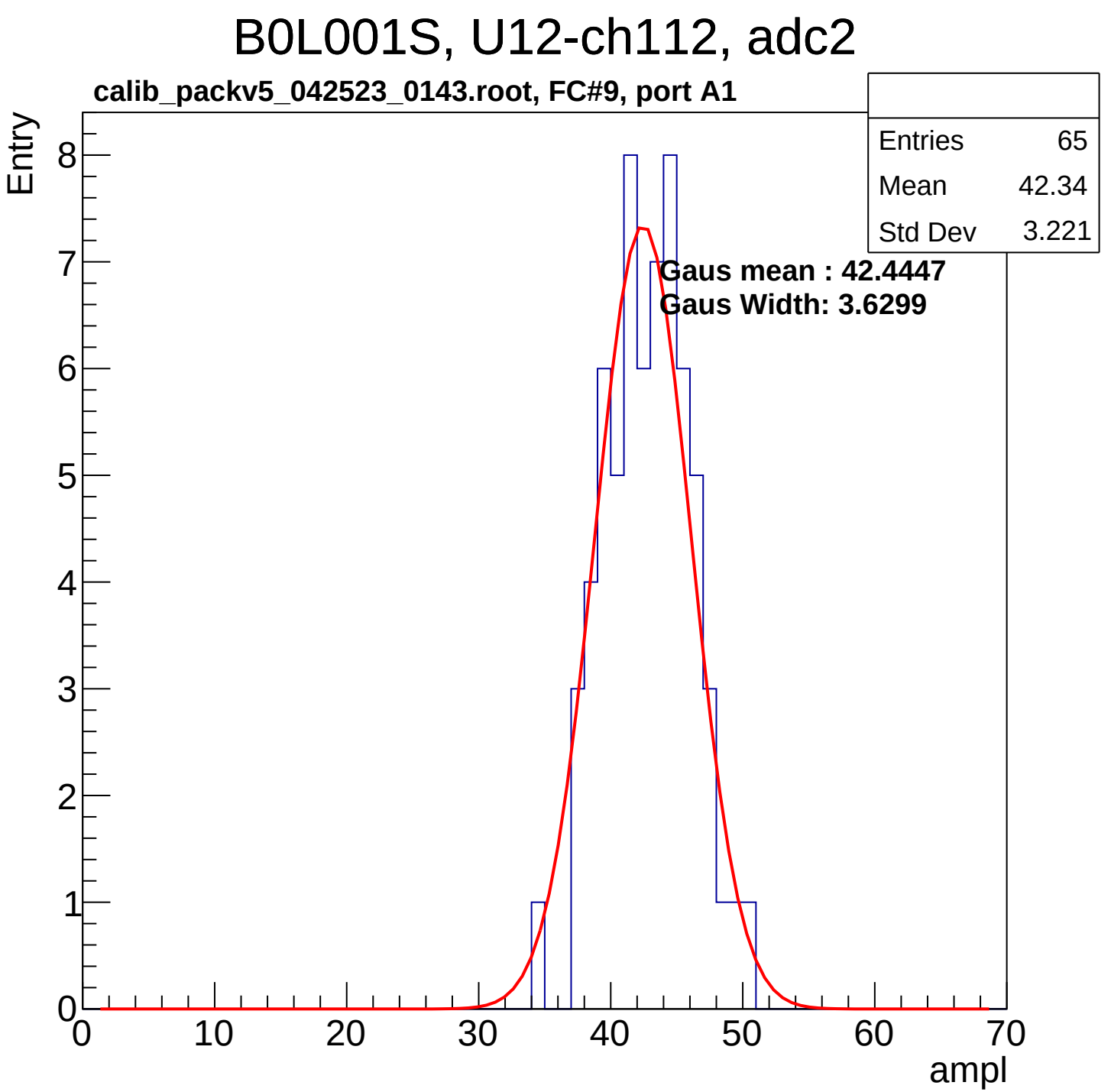

B0L001S, U12-ch112, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 67
Mean 35.96
Std Dev 3.783
Gaus mean : 36.1233
Gaus Width: 3.6920
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch112, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 65
Mean 42.34
Std Dev 3.221
Gaus mean : 42.4447
Gaus Width: 3.6299
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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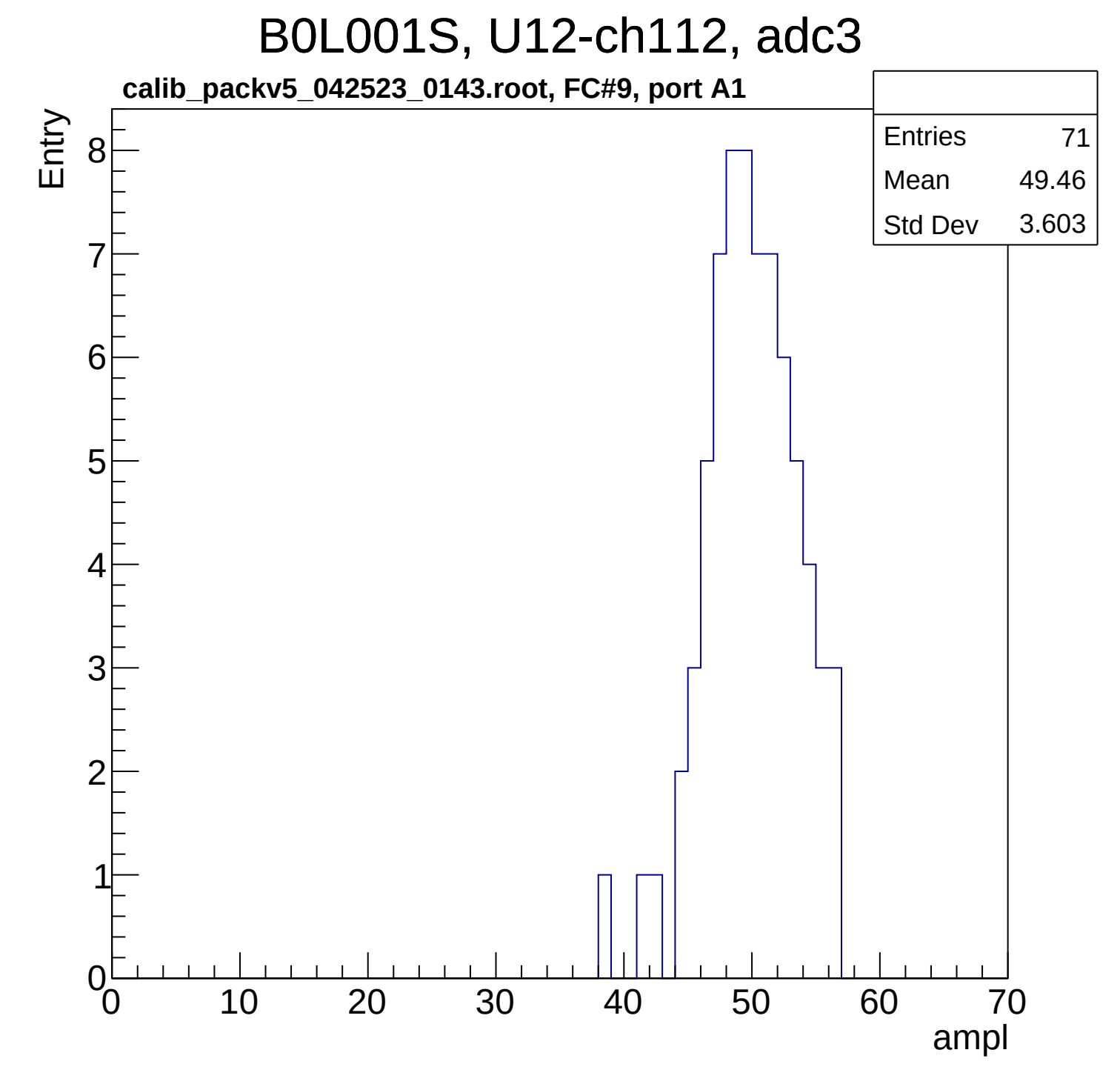
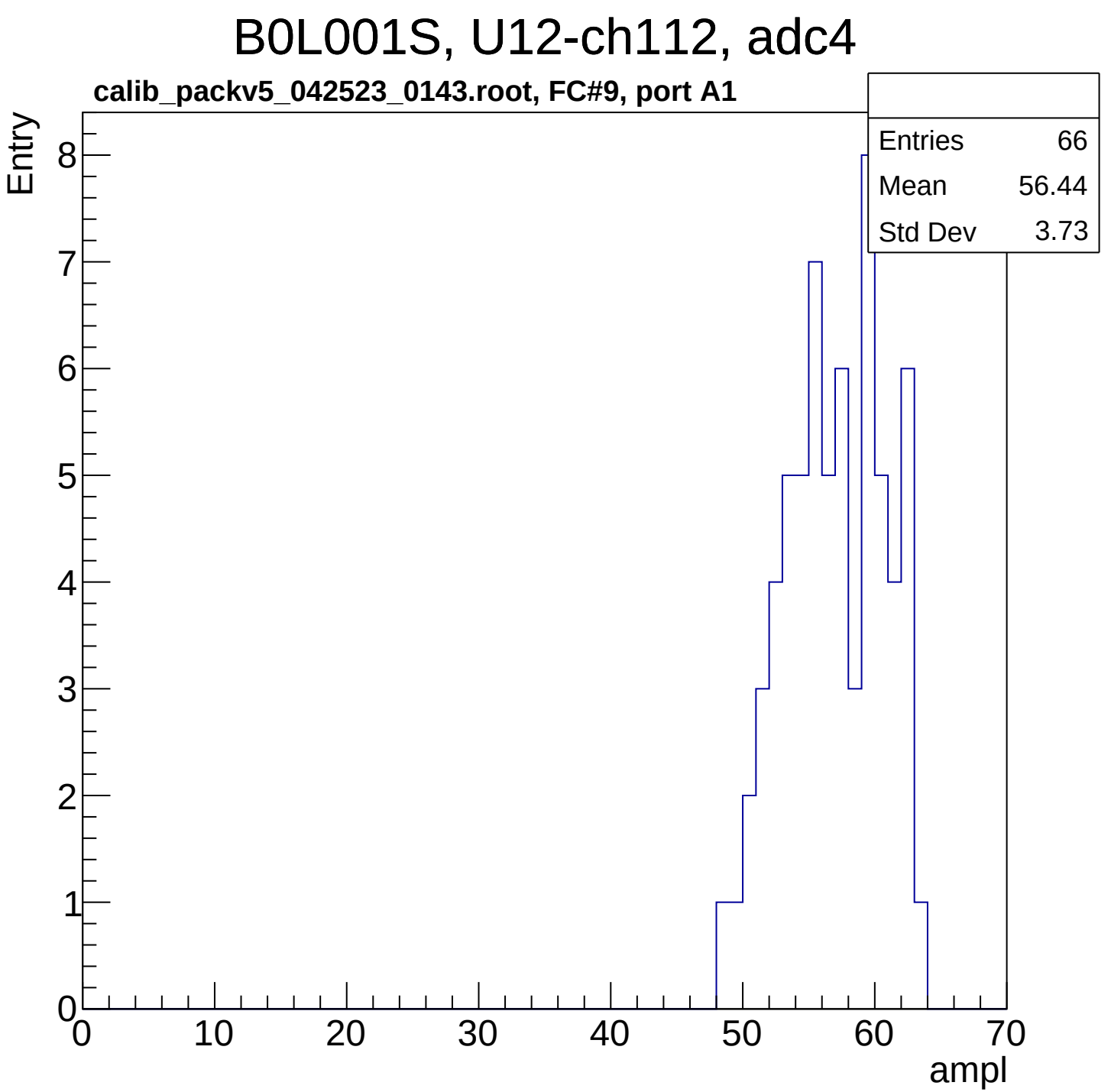
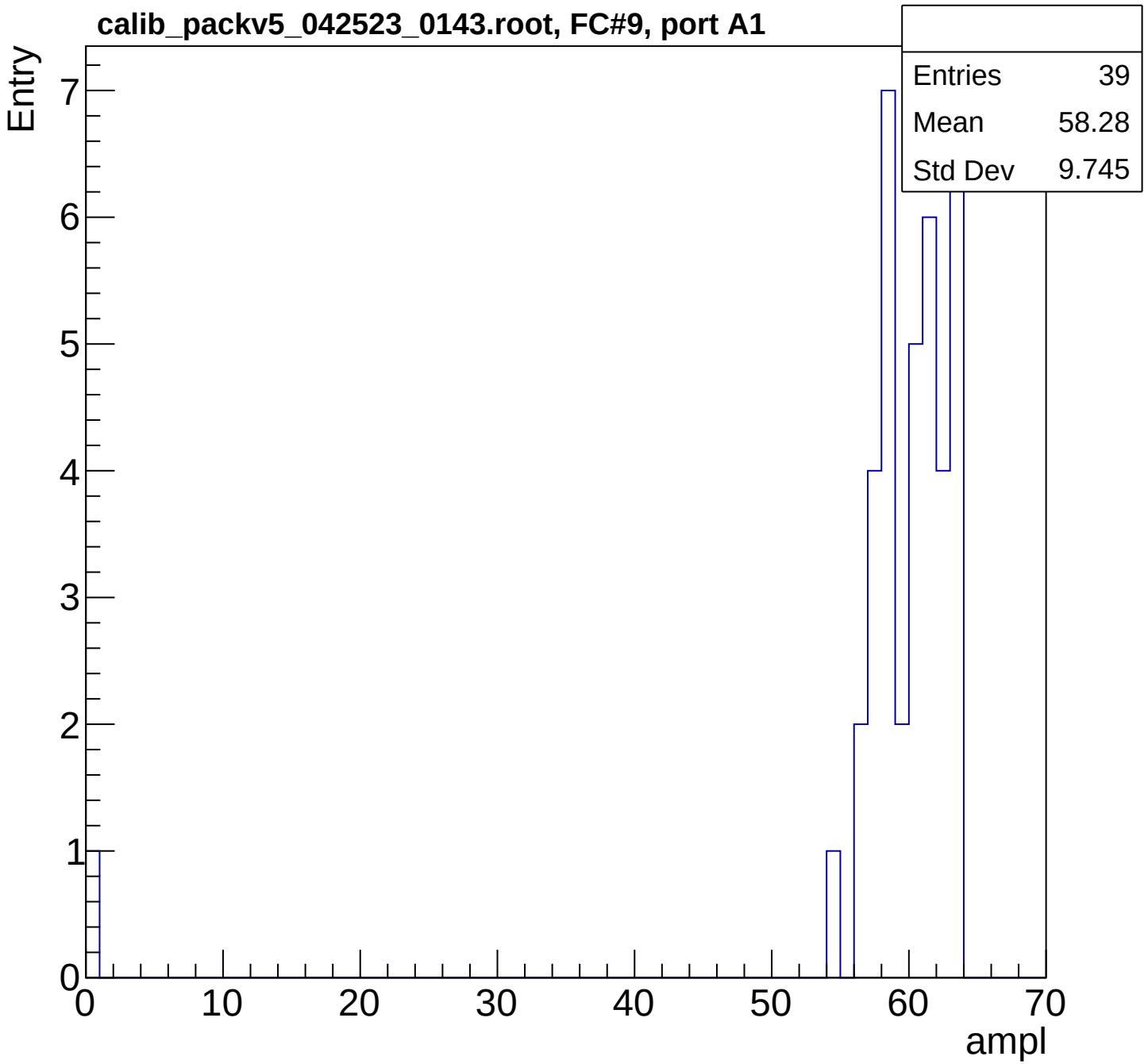
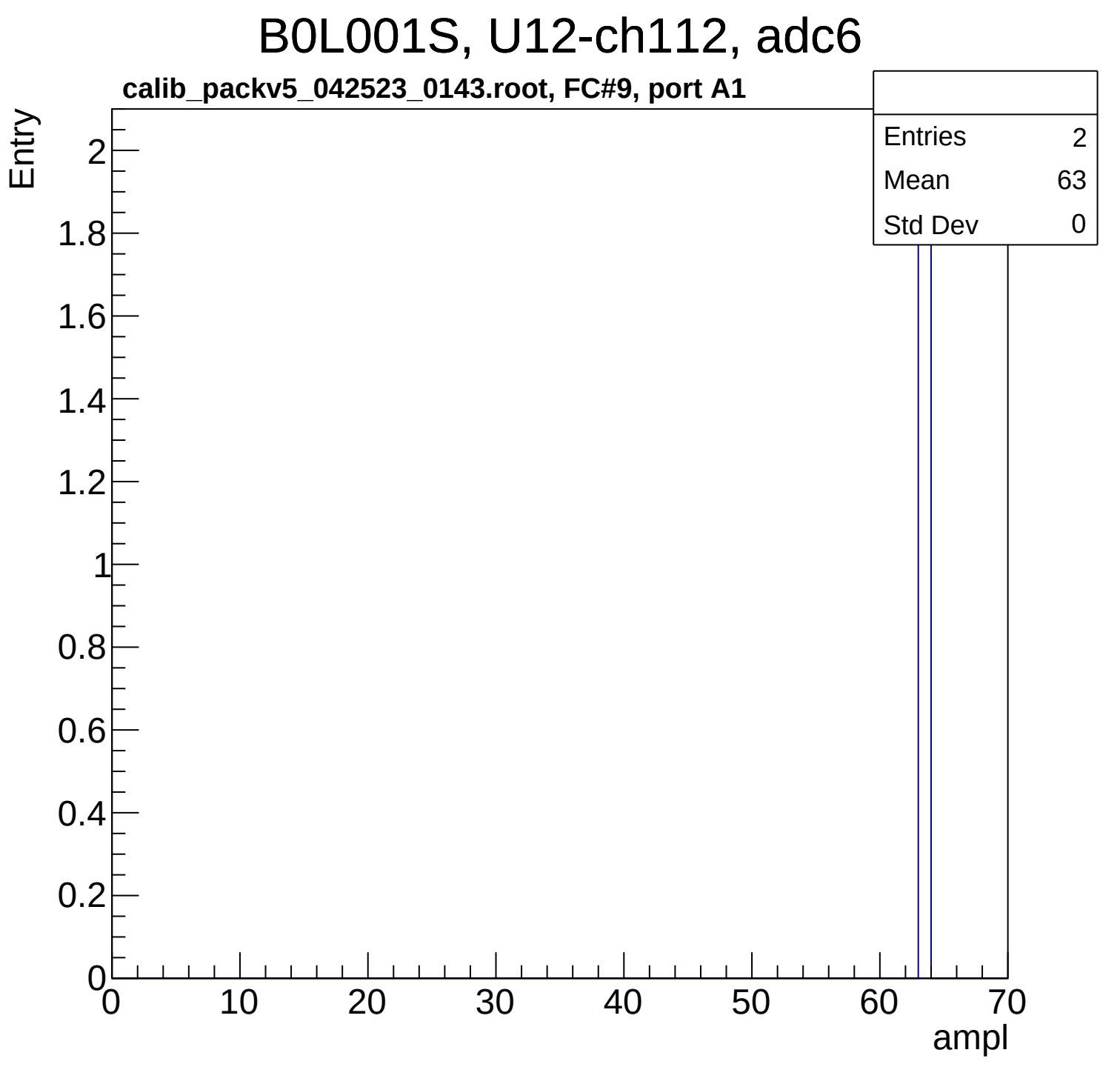
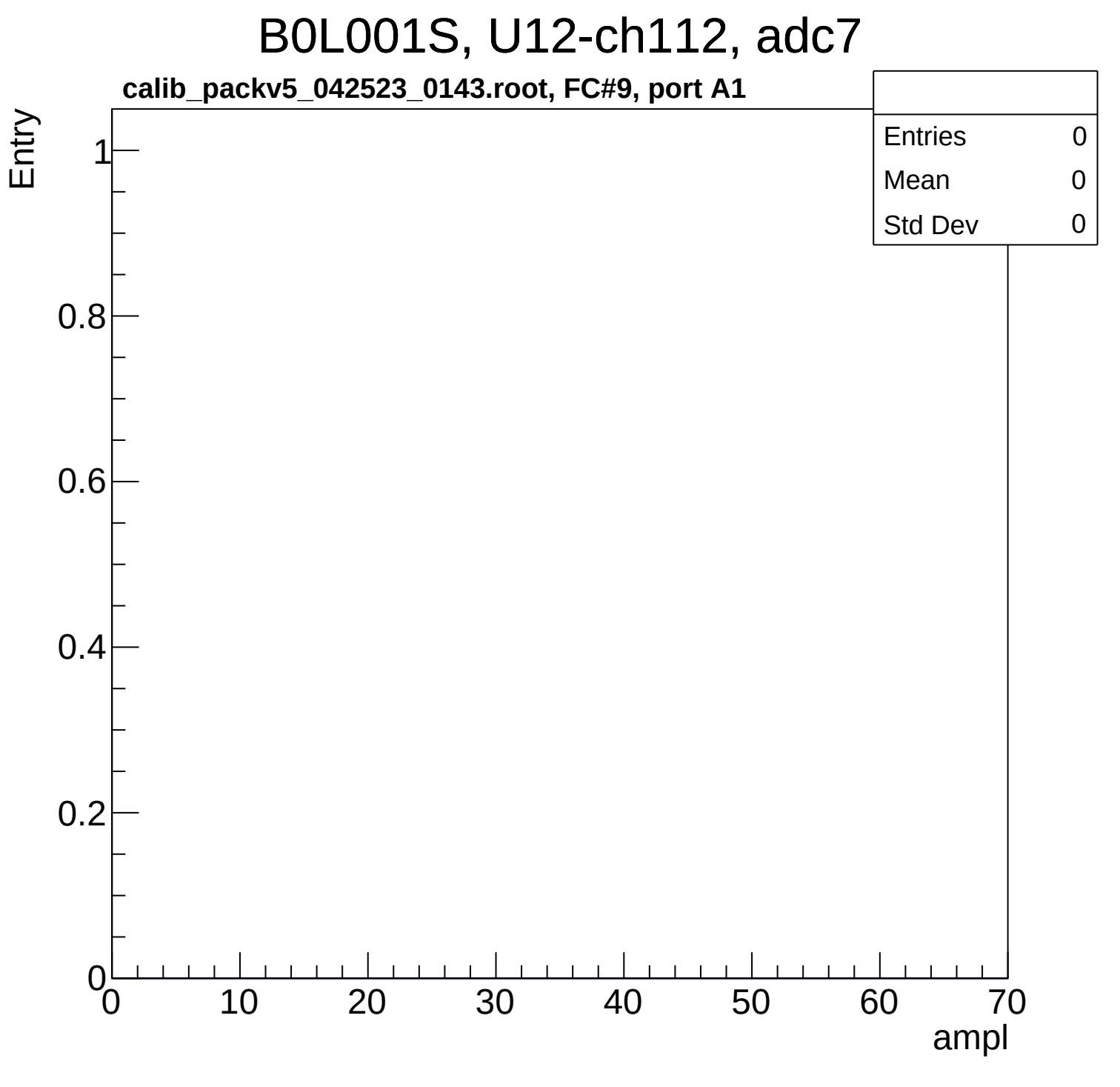
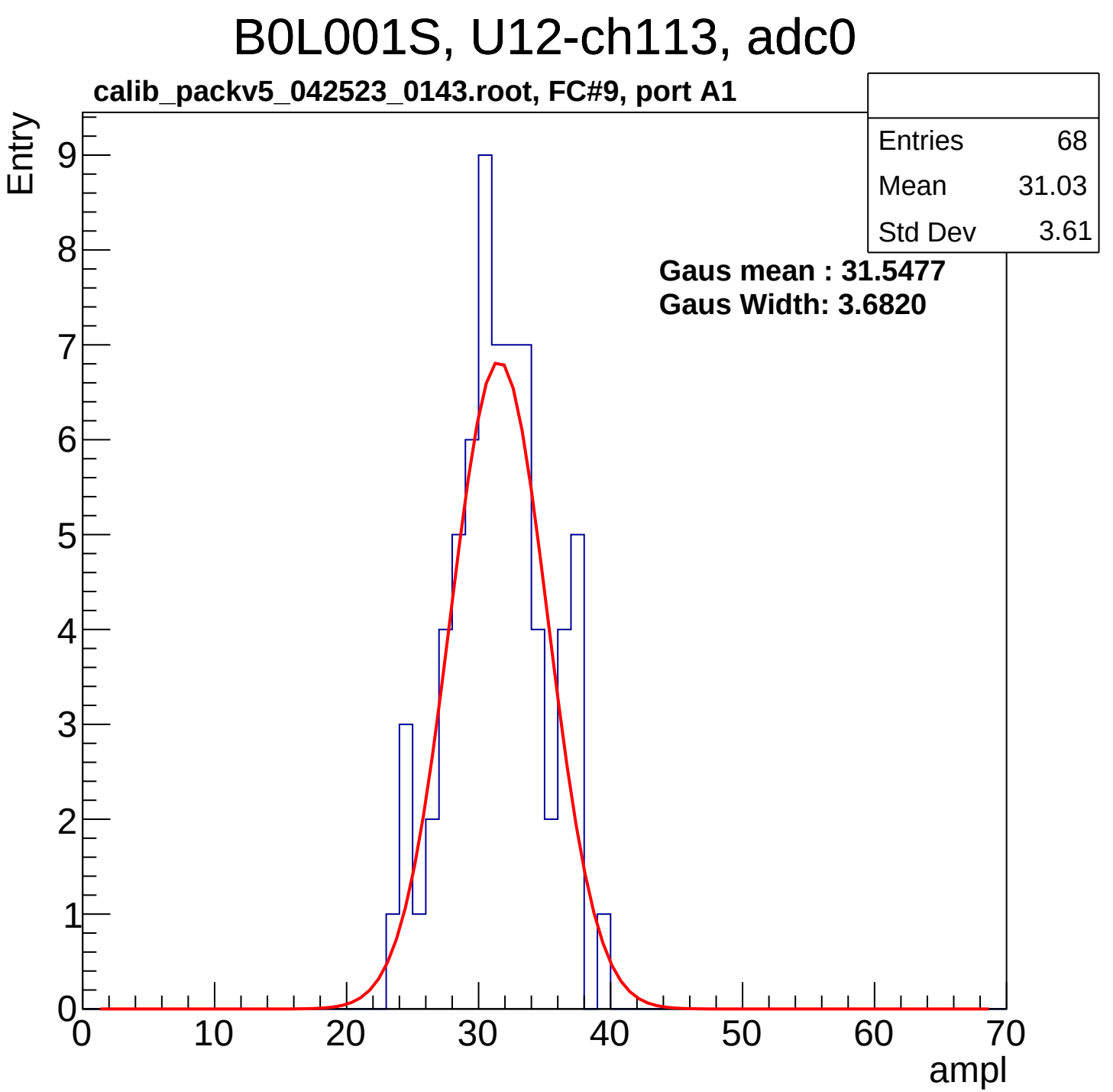

B0L001S, U12-ch112, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 71
Mean 49.46
Std Dev 3.603
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

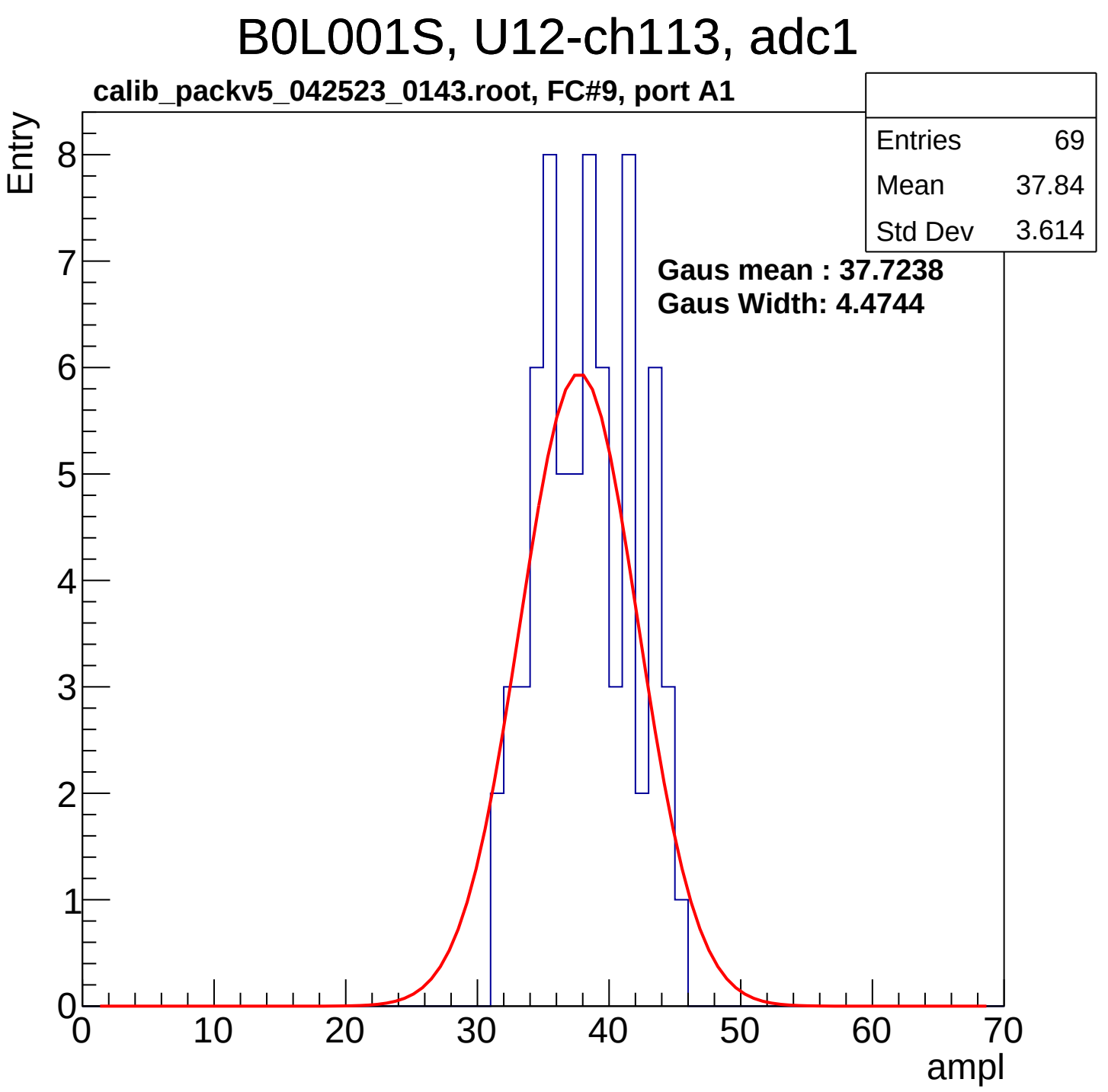

B0L001S, U12-ch112, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 66
Mean 56.44
Std Dev 3.73
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch112, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 39
Mean 58.28
Std Dev 9.745
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B0L001S, U12-ch112, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L001S, U12-ch112, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch113, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 68
Mean 31.03
Std Dev 3.61
Gaus mean : 31.5477
Gaus Width: 3.6820
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch113, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 69
Mean 37.84
Std Dev 3.614
Gaus mean : 37.7238
Gaus Width: 4.4744
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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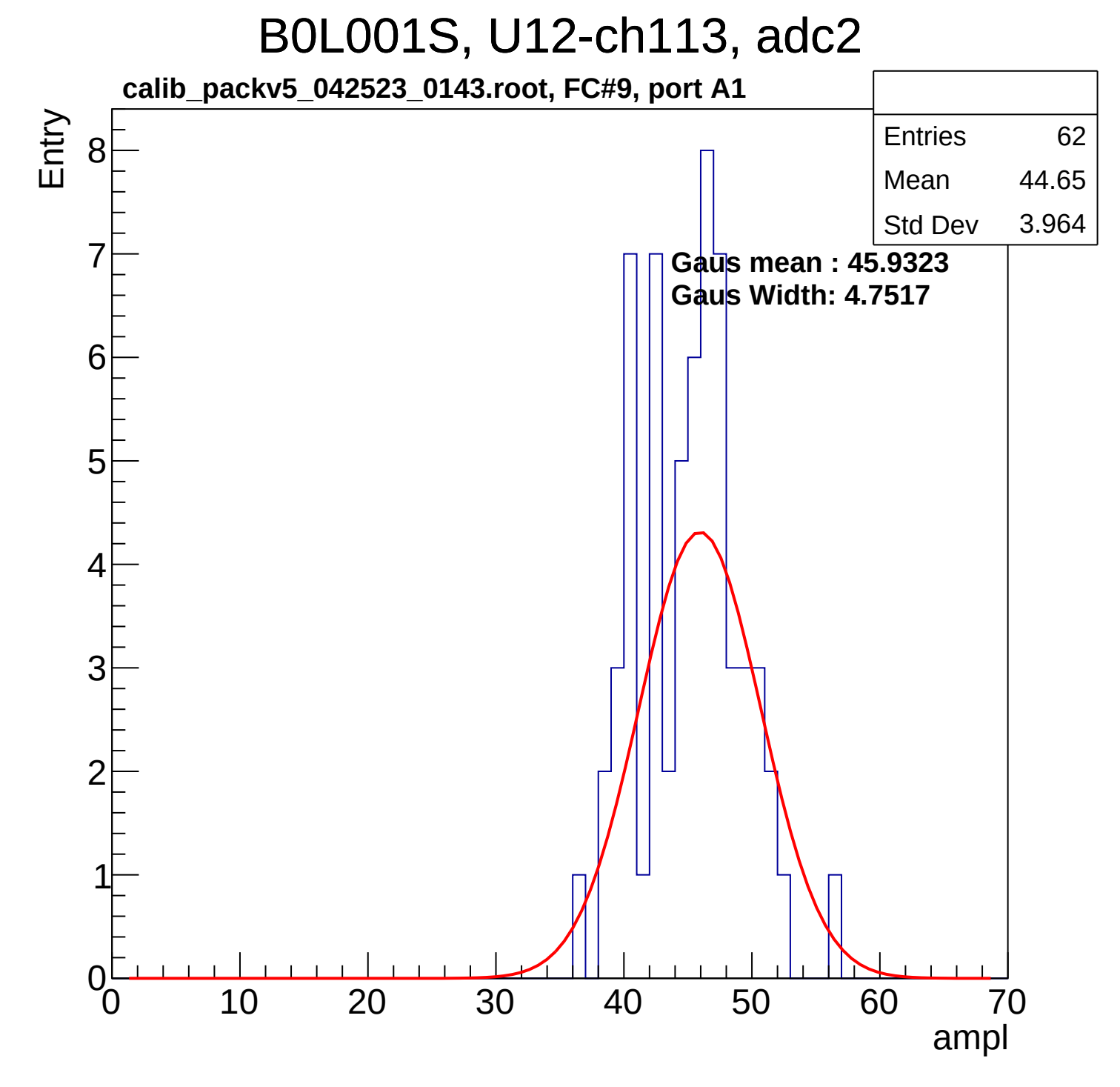
B0L001S, U12-ch113, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 62
Mean 44.65
Std Dev 3.964
Gaus mean : 45.9323
Gaus Width: 4.7517
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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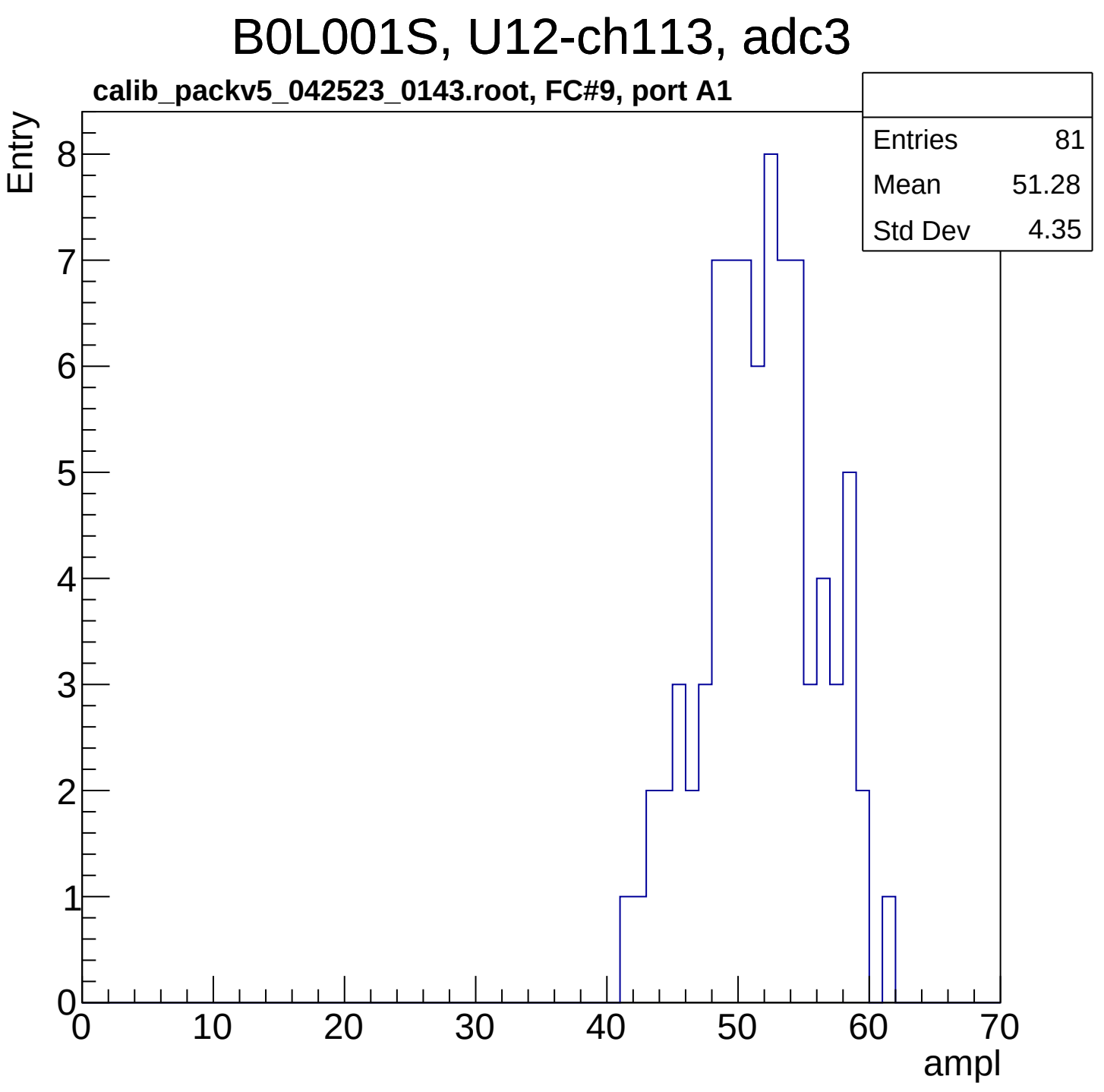
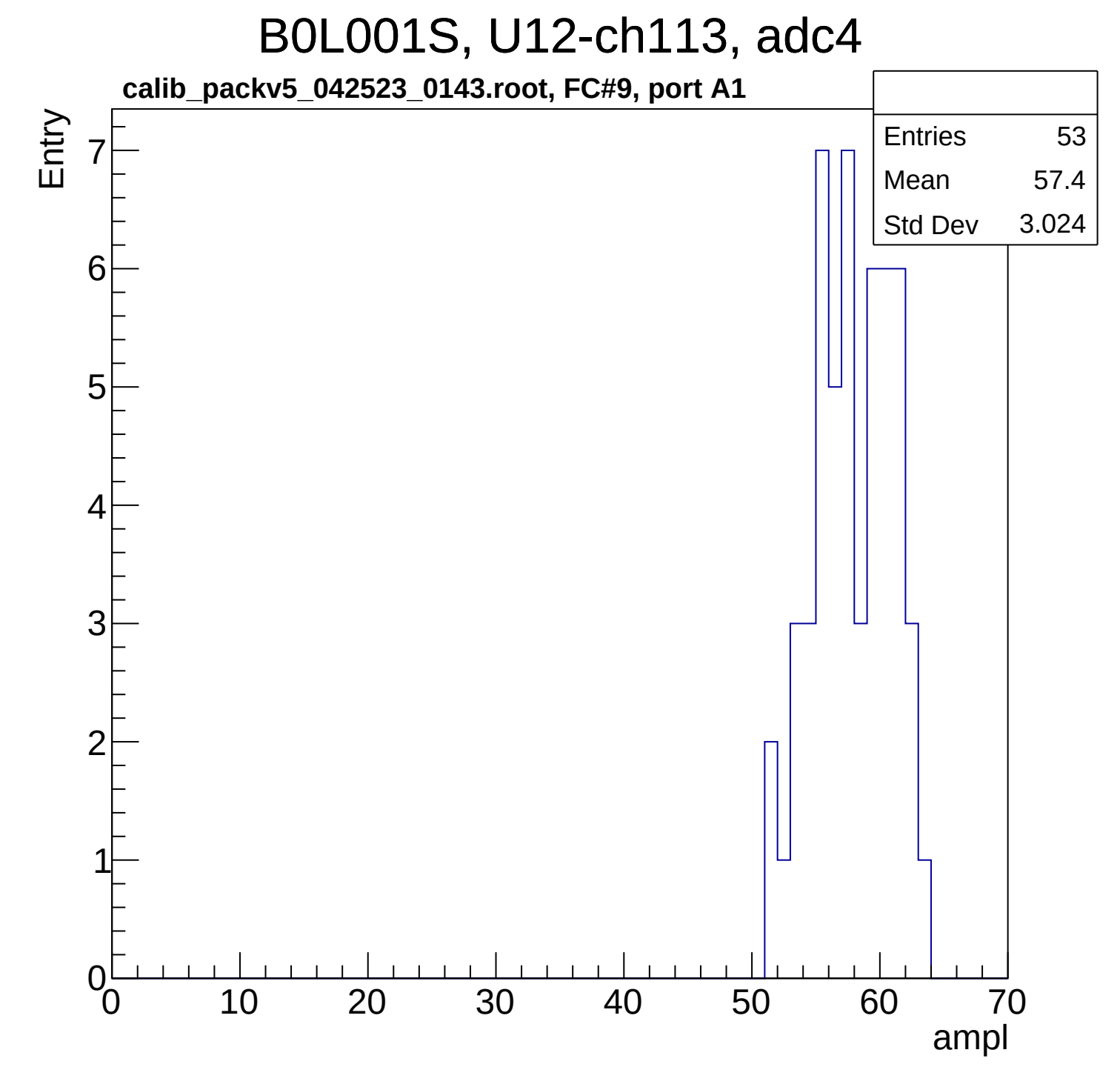
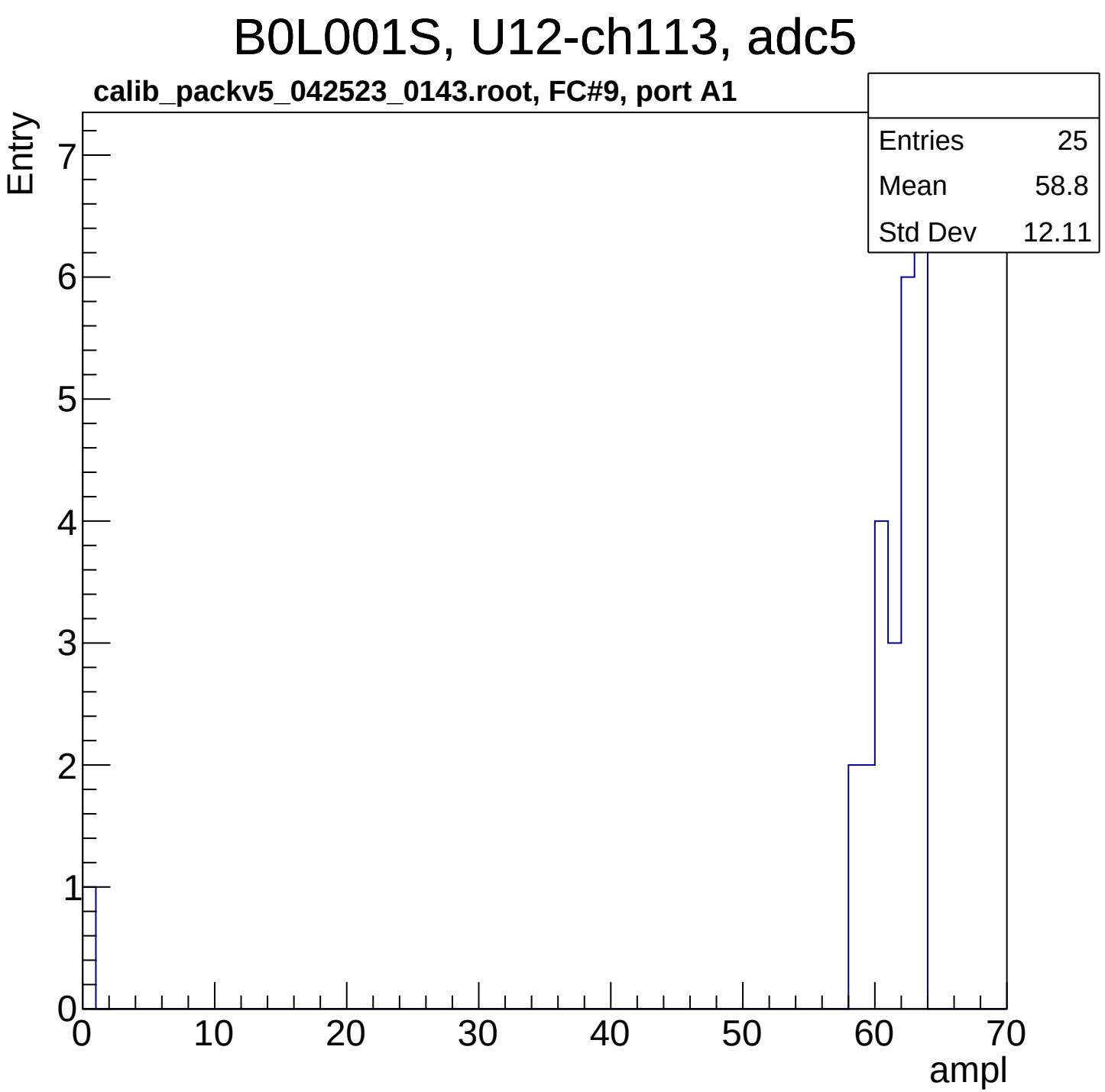
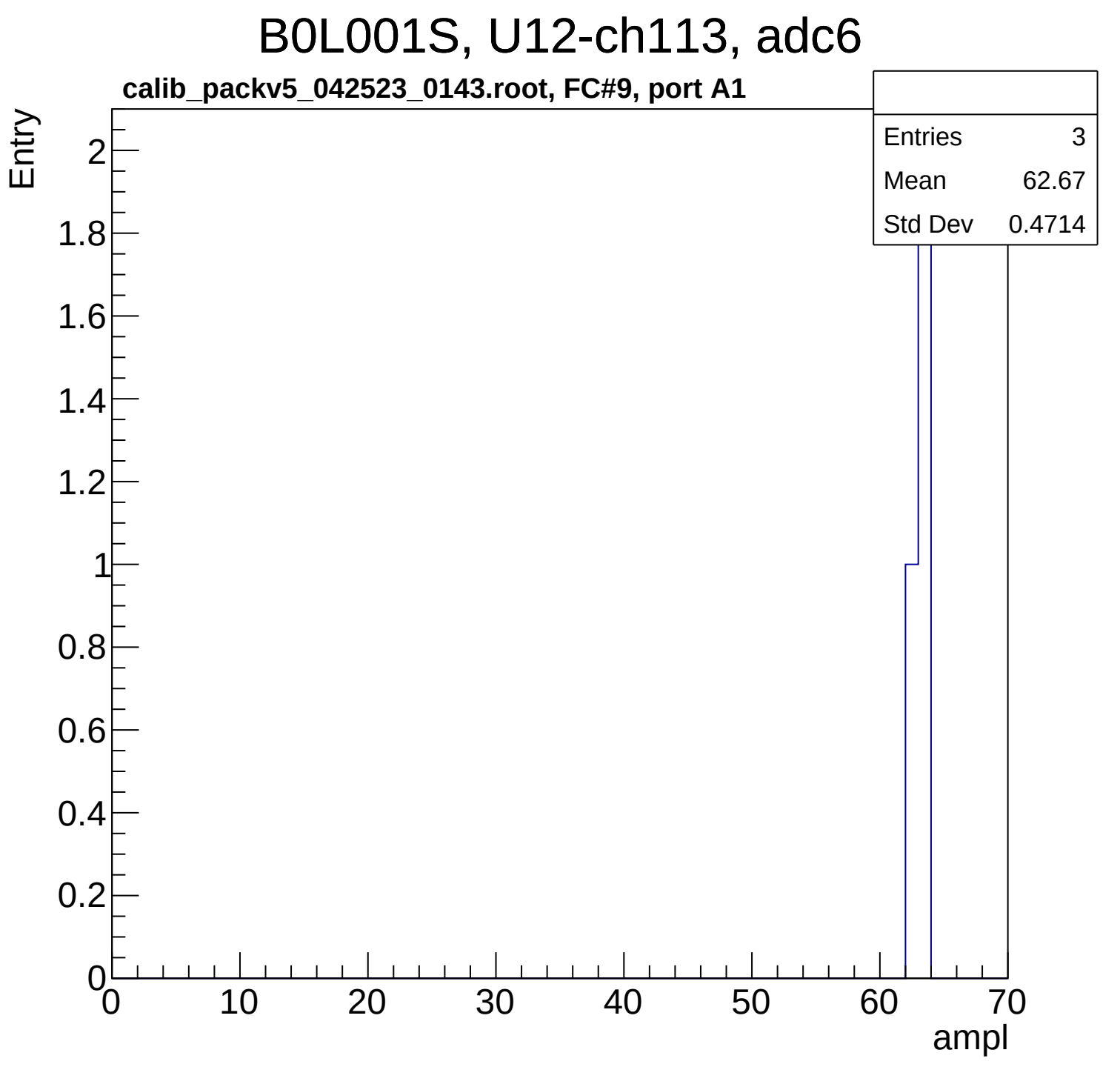
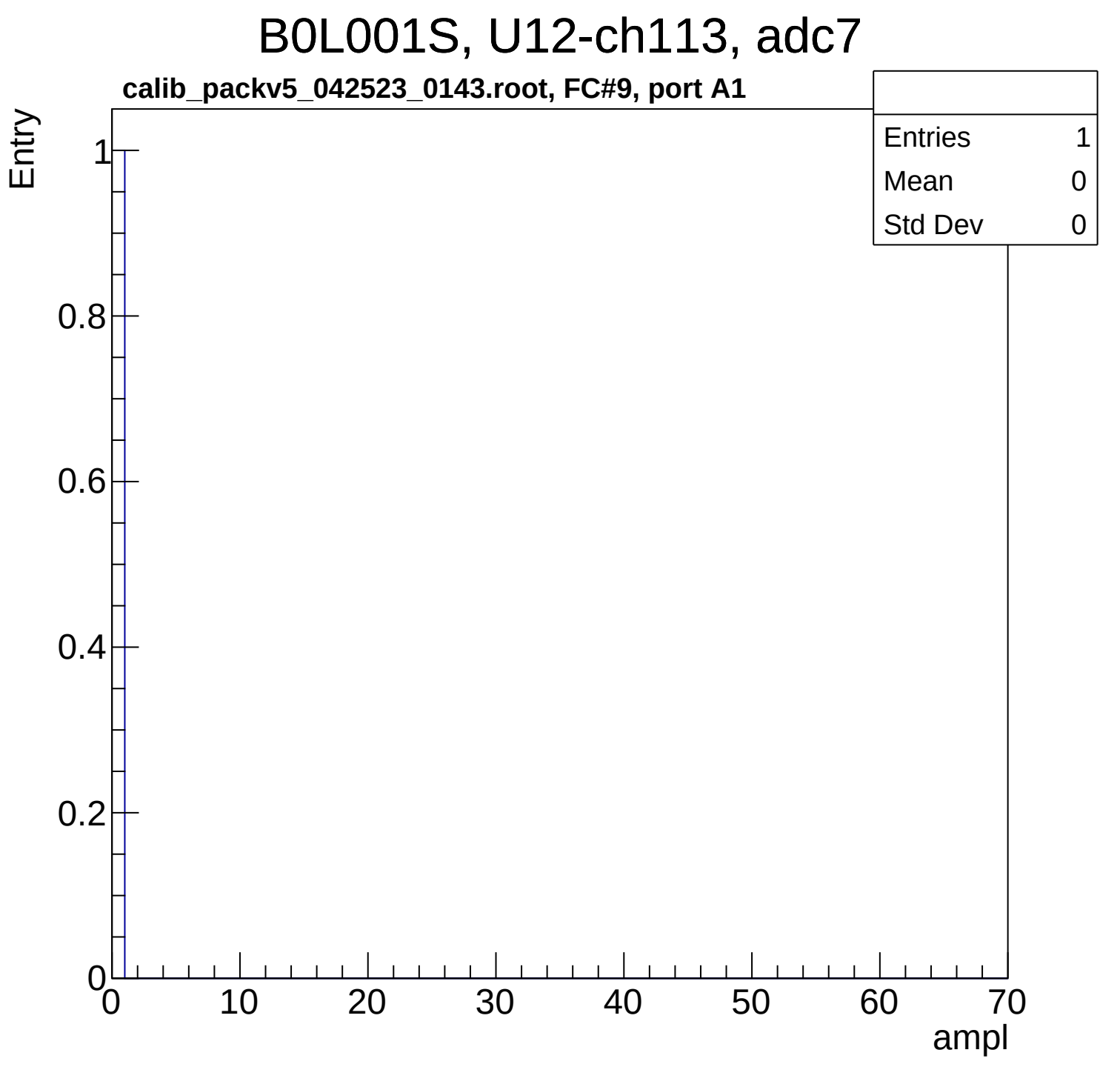
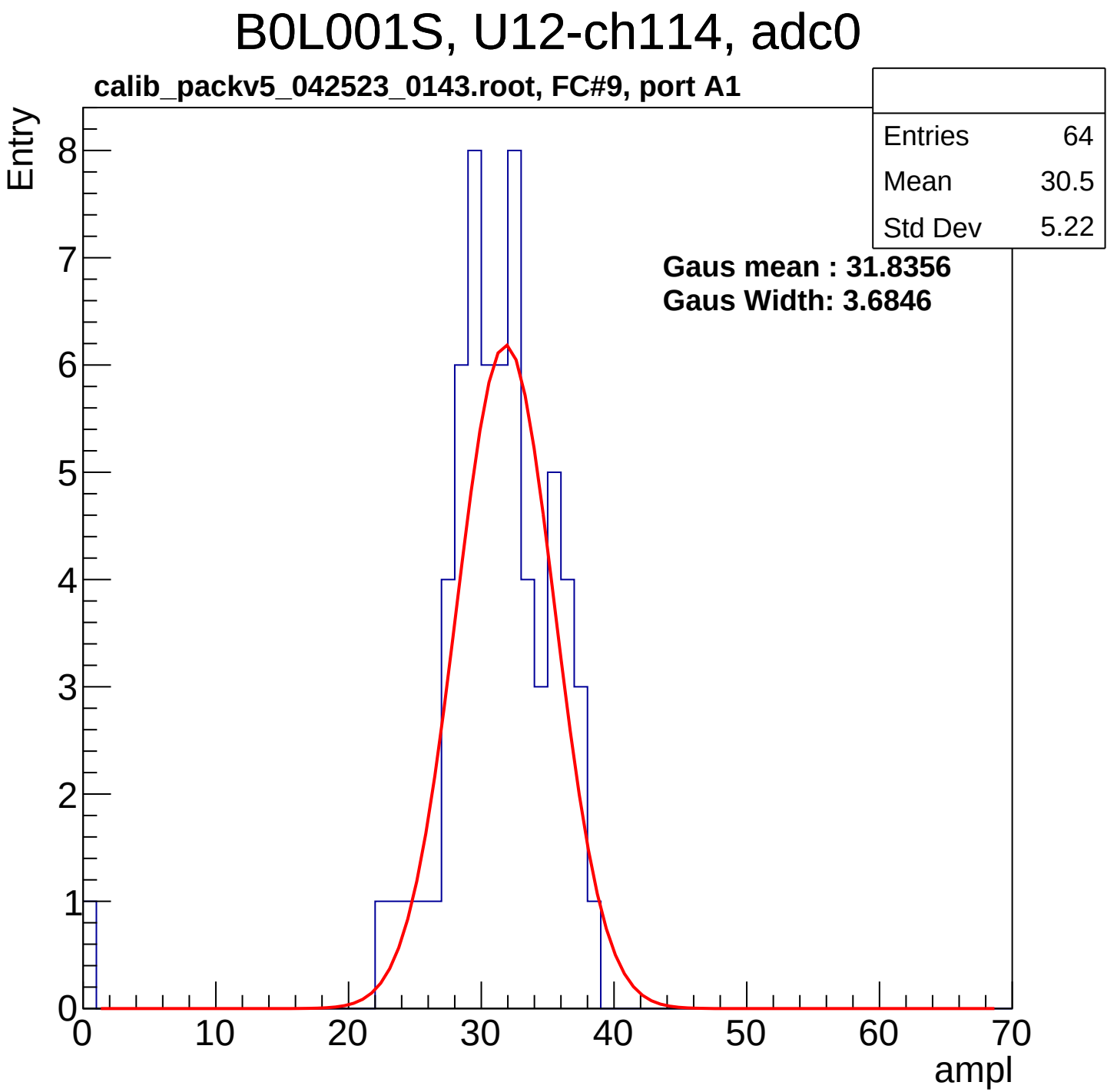

B0L001S, U12-ch113, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 81
Mean 51.28
Std Dev 4.35
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

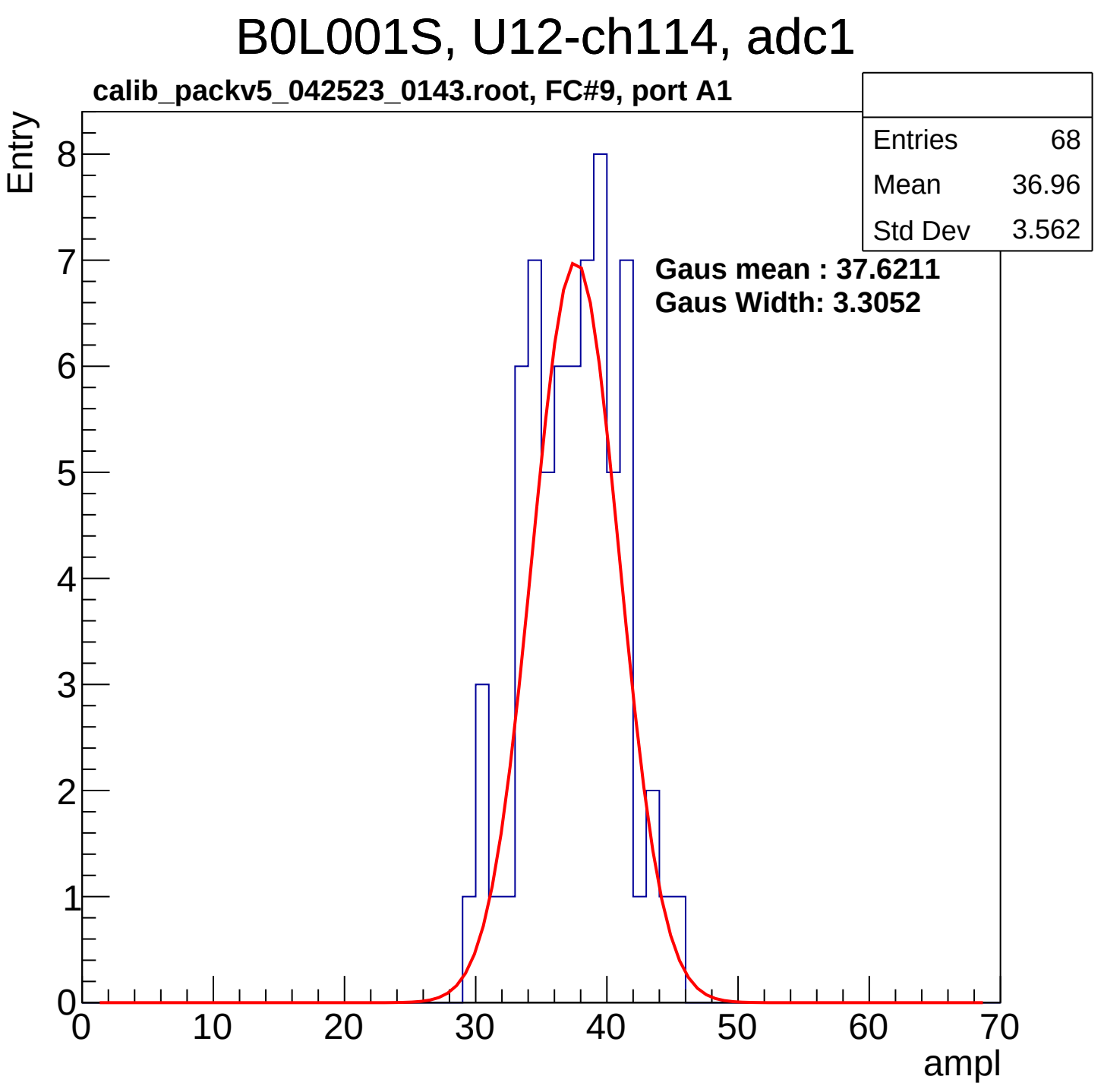

B0L001S, U12-ch113, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 53
Mean 57.4
Std Dev 3.024
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

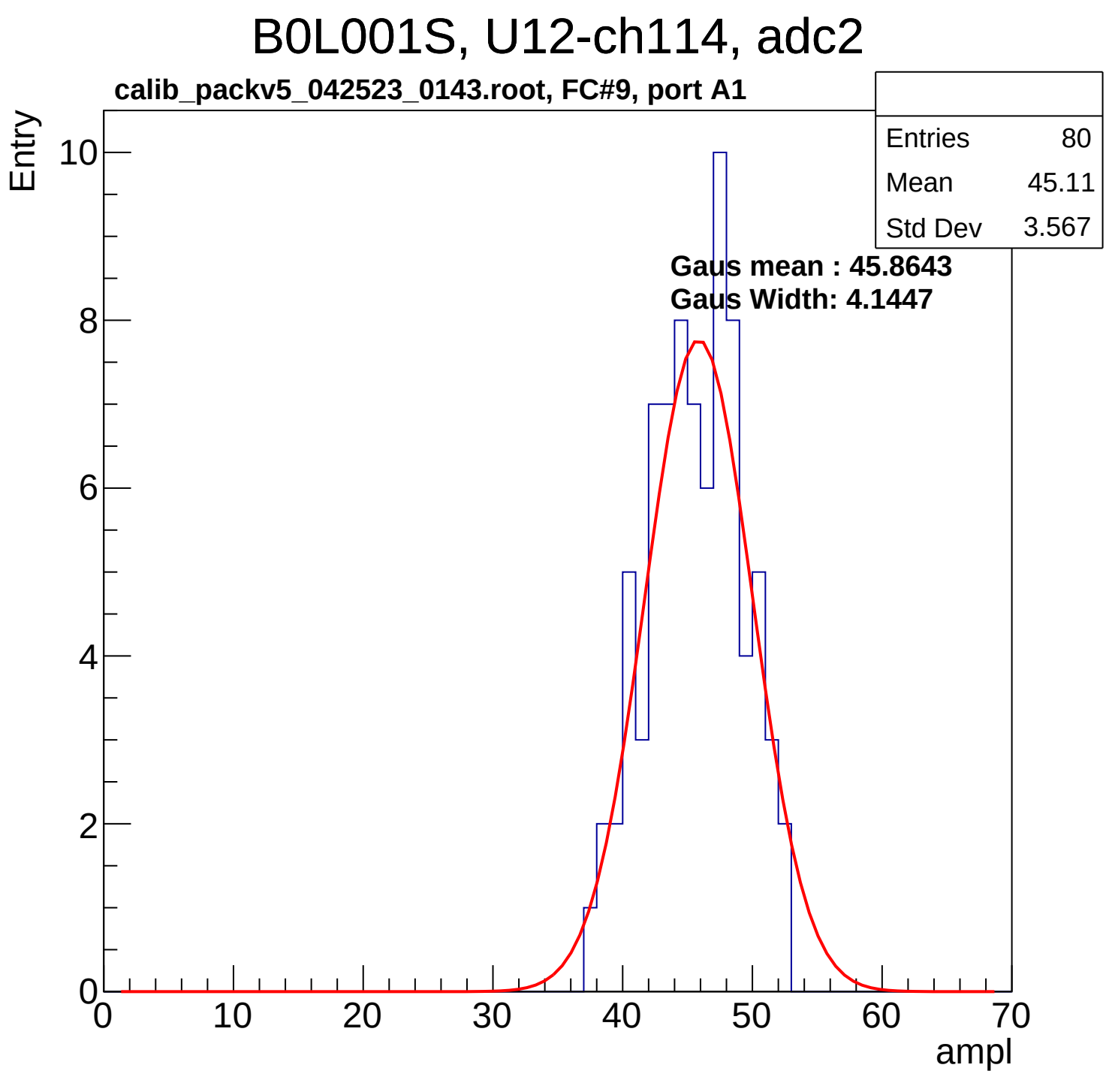

B0L001S, U12-ch113, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 25
Mean 58.8
Std Dev 12.11
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

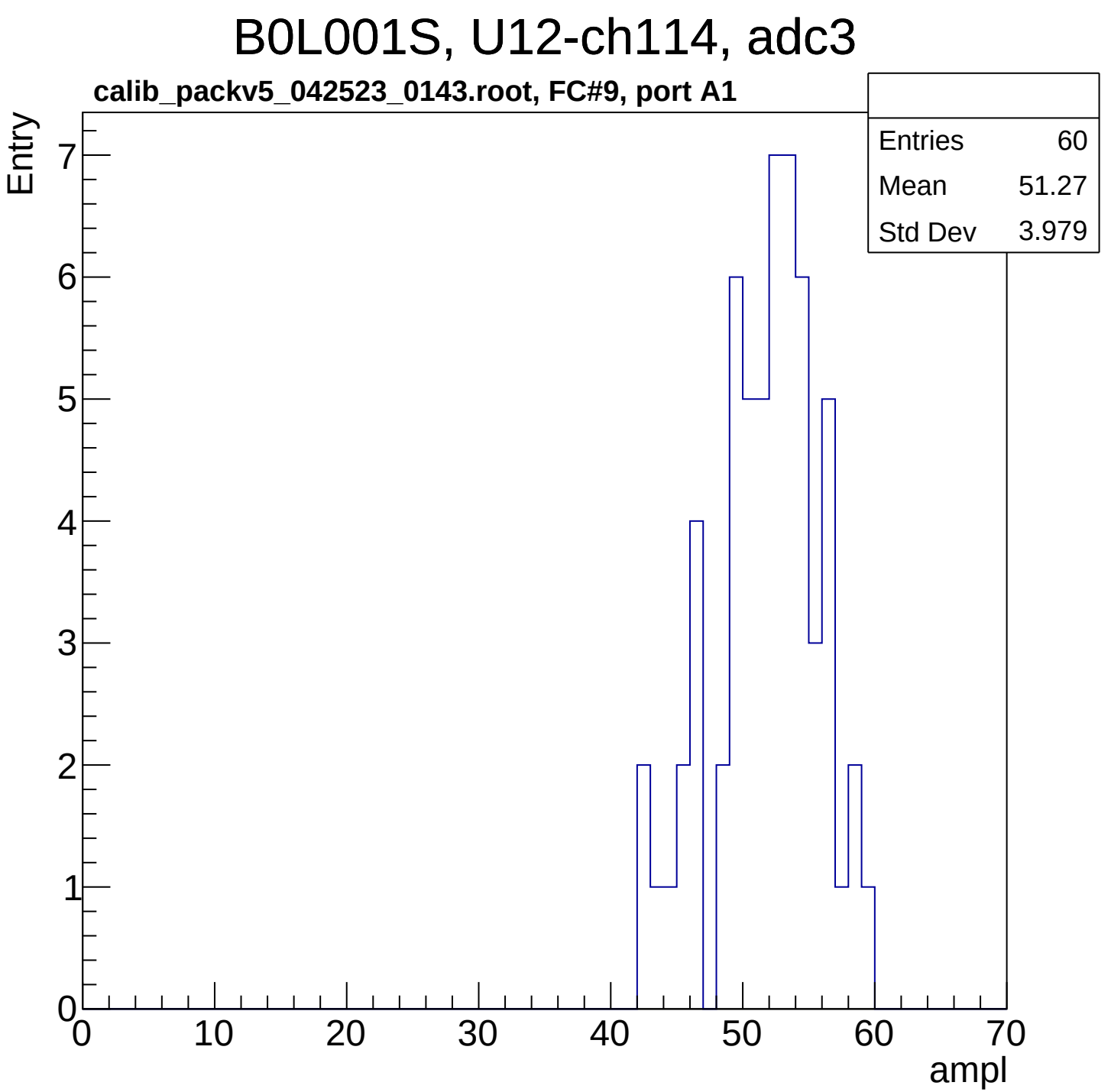

B0L001S, U12-ch113, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

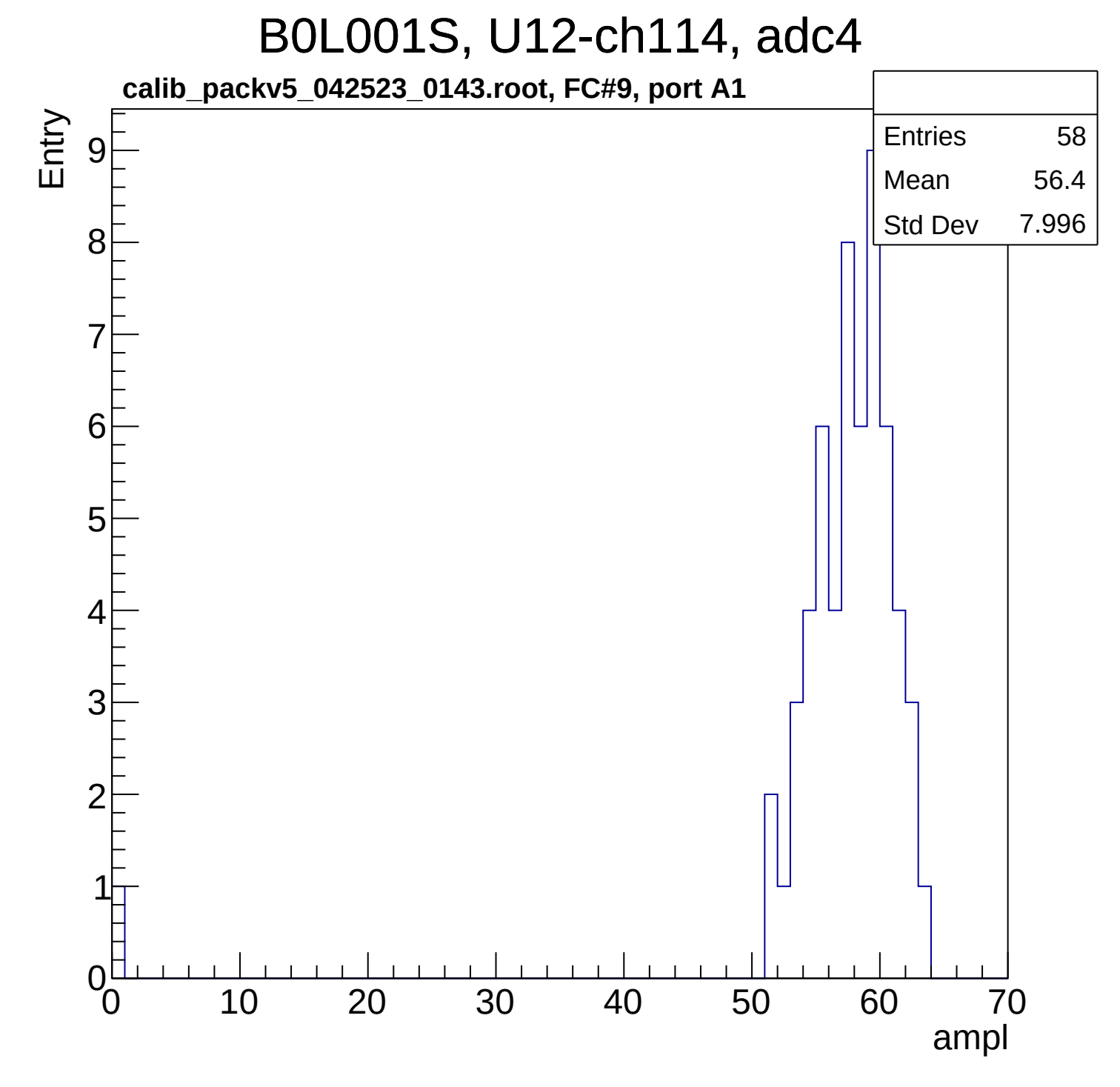

B0L001S, U12-ch113, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch114, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 64
Mean 30.5
Std Dev 5.22
Gaus mean : 31.8356
Gaus Width: 3.6846
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch114, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 68
Mean 36.96
Std Dev 3.562
Gaus mean : 37.6211
Gaus Width: 3.3052
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch114, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 80
Mean 45.11
Std Dev 3.567
Gaus mean : 45.8643
Gaus Width: 4.1447
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch114, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 60
Mean 51.27
Std Dev 3.979
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B0L001S, U12-ch114, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 58
Mean 56.4
Std Dev 7.996
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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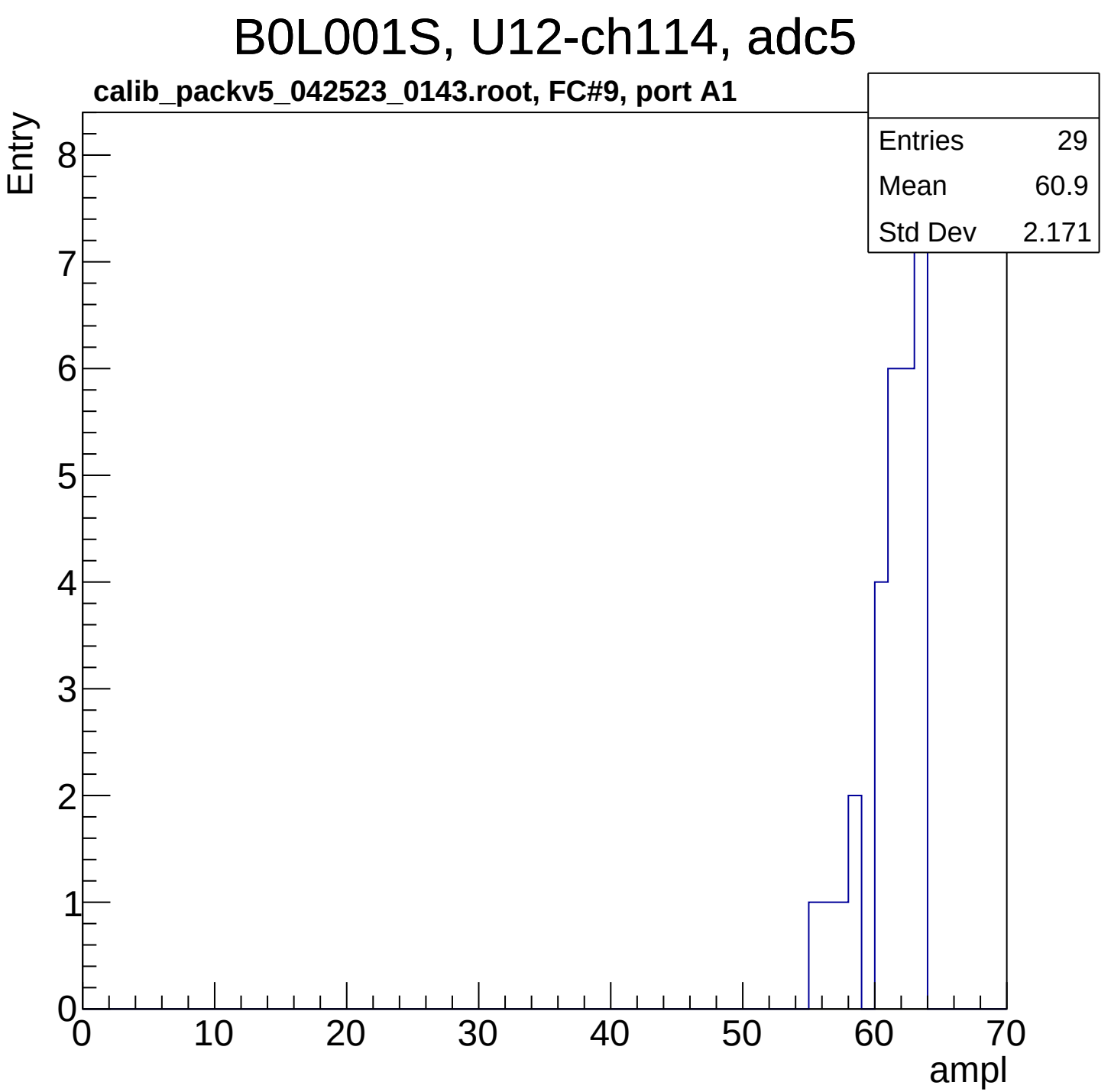
40
50
60
70


B0L001S, U12-ch114, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 29
Mean 60.9
Std Dev 2.171
Entry
ampl
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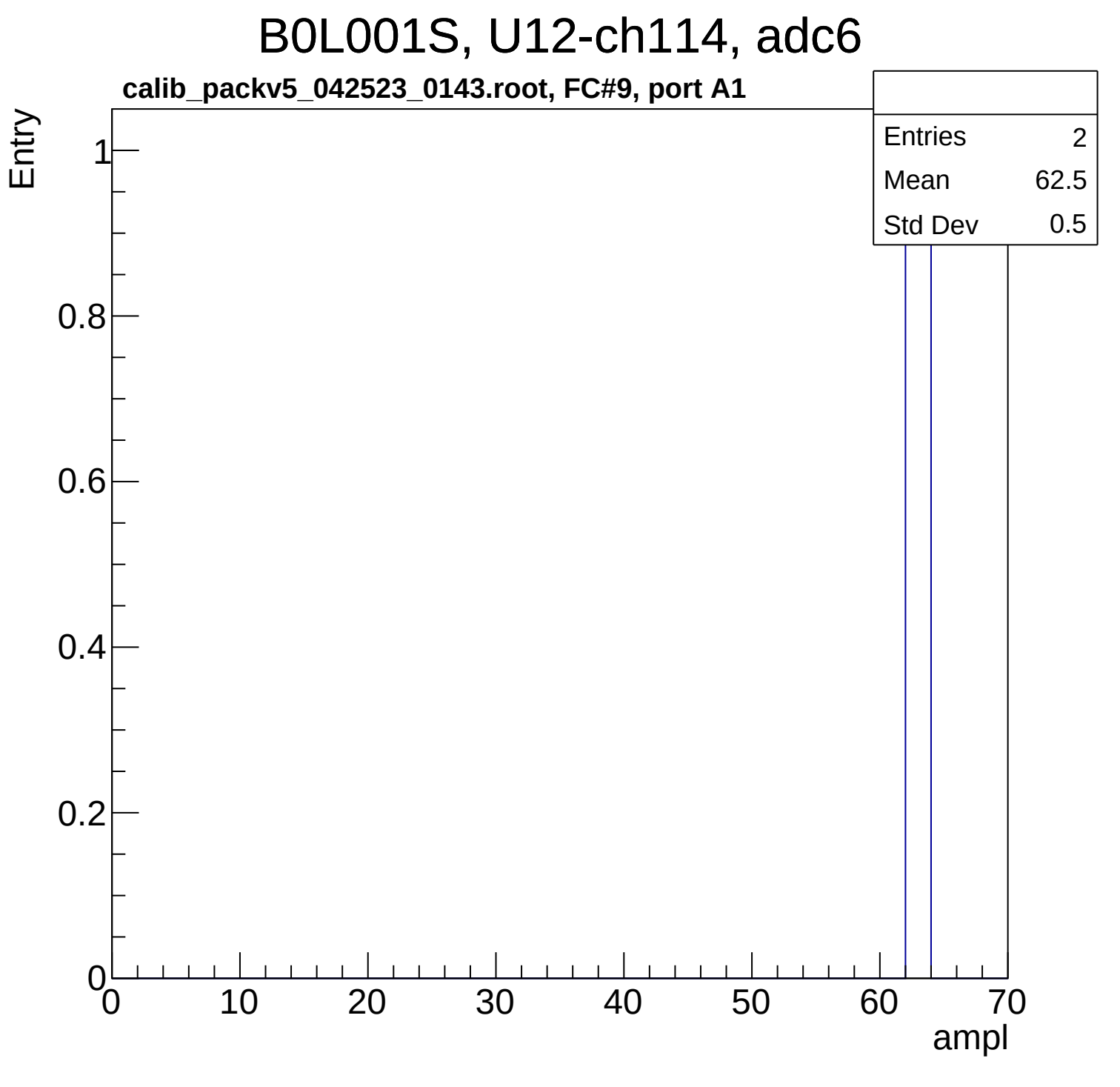
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch114, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 62.5
Std Dev 0.5
Entry
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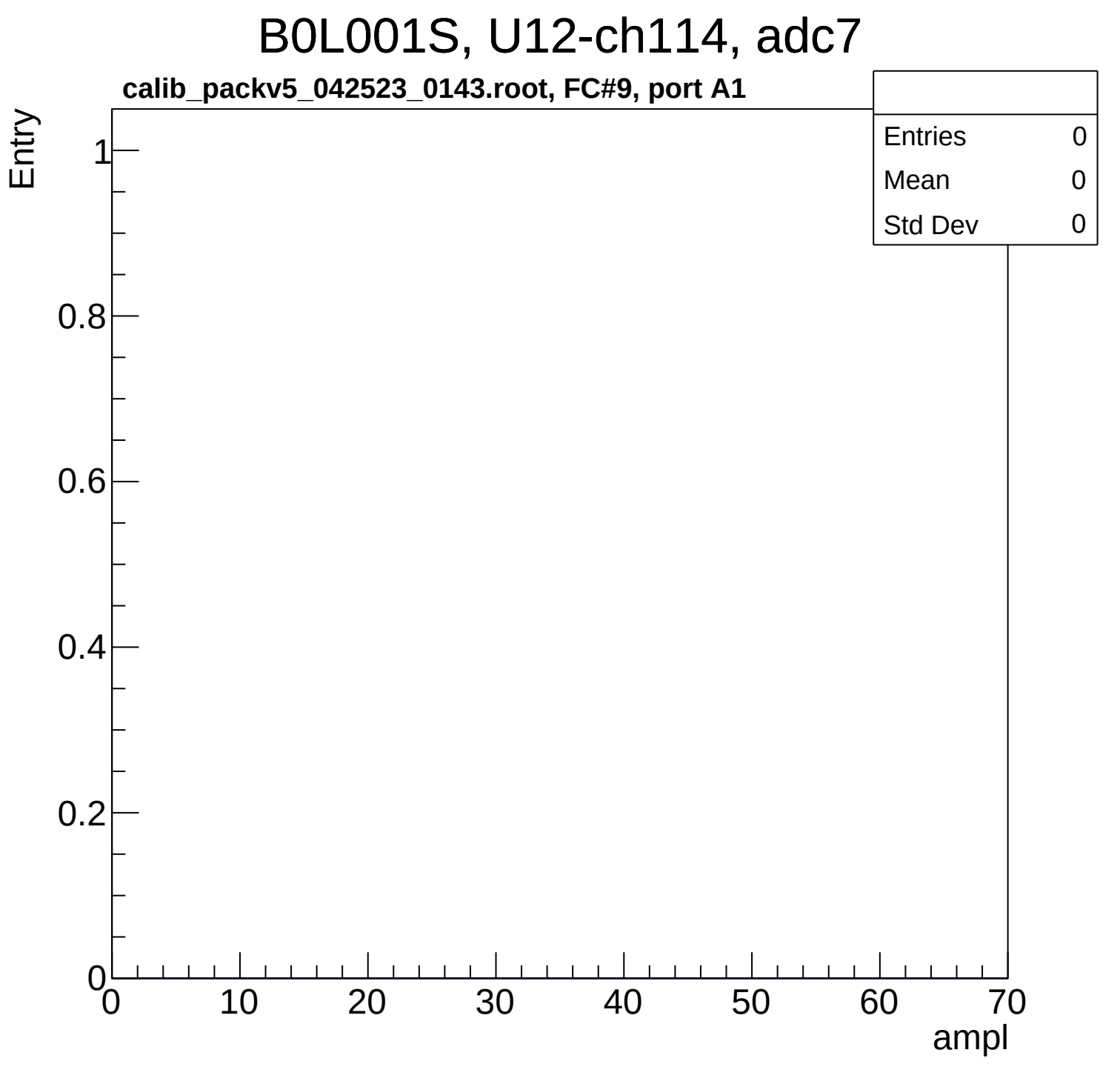
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch114, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
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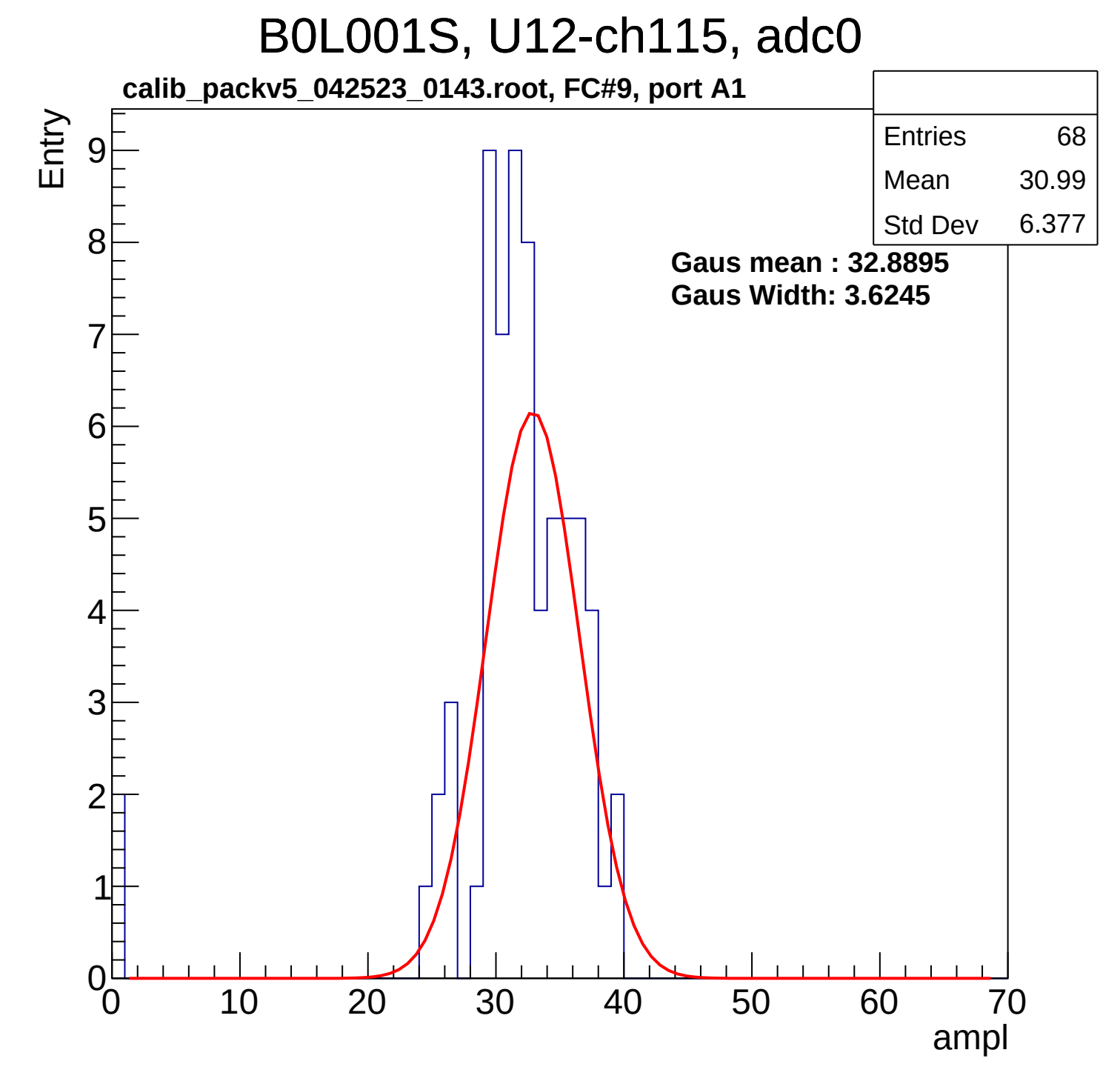
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch115, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 68
Mean 30.99
Std Dev 6.377
Gaus mean : 32.8895
Gaus Width: 3.6245
Entry
ampl
0
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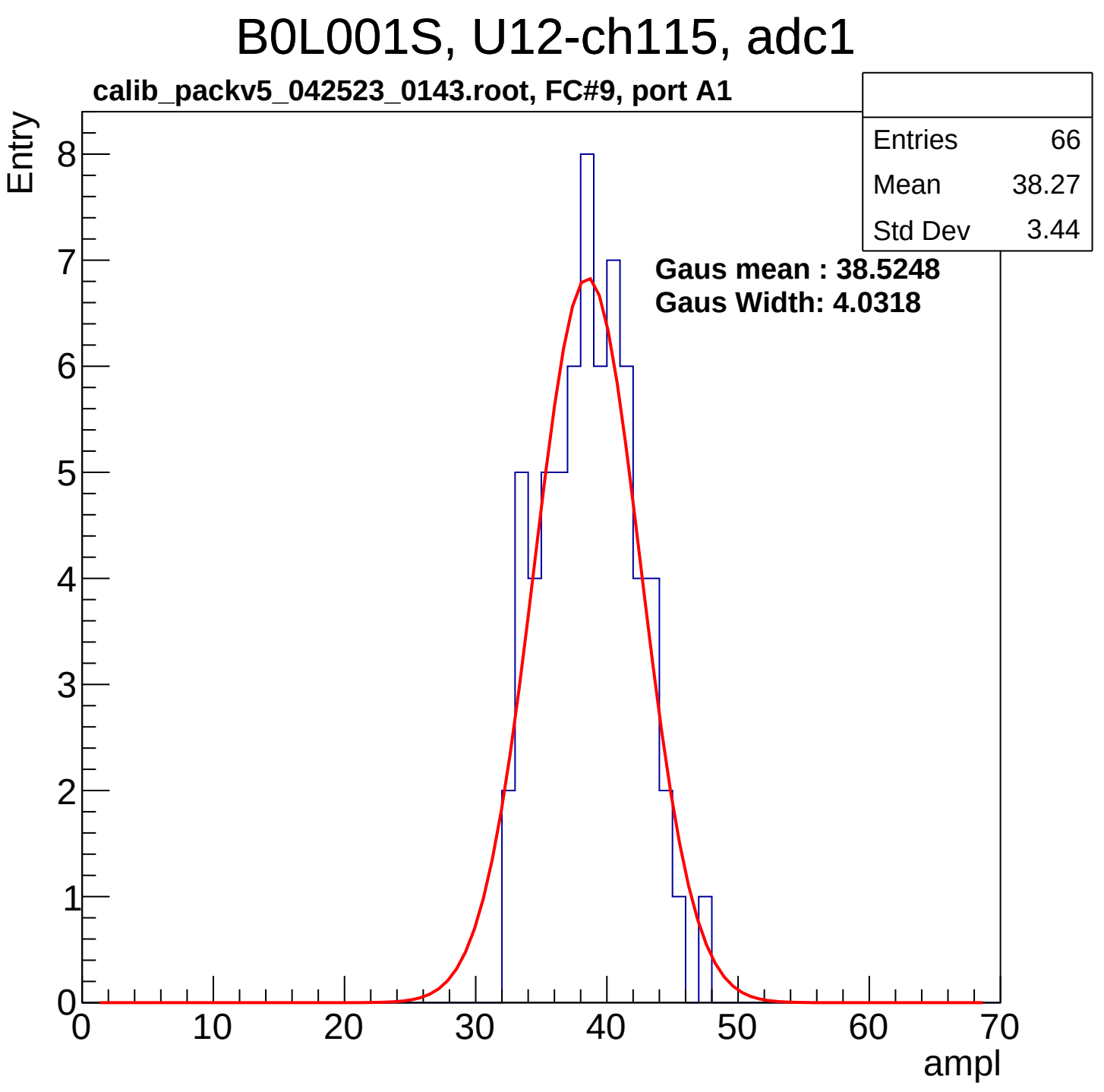
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch115, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 66
Mean 38.27
Std Dev 3.44
Gaus mean : 38.5248
Gaus Width: 4.0318
Entry
ampl
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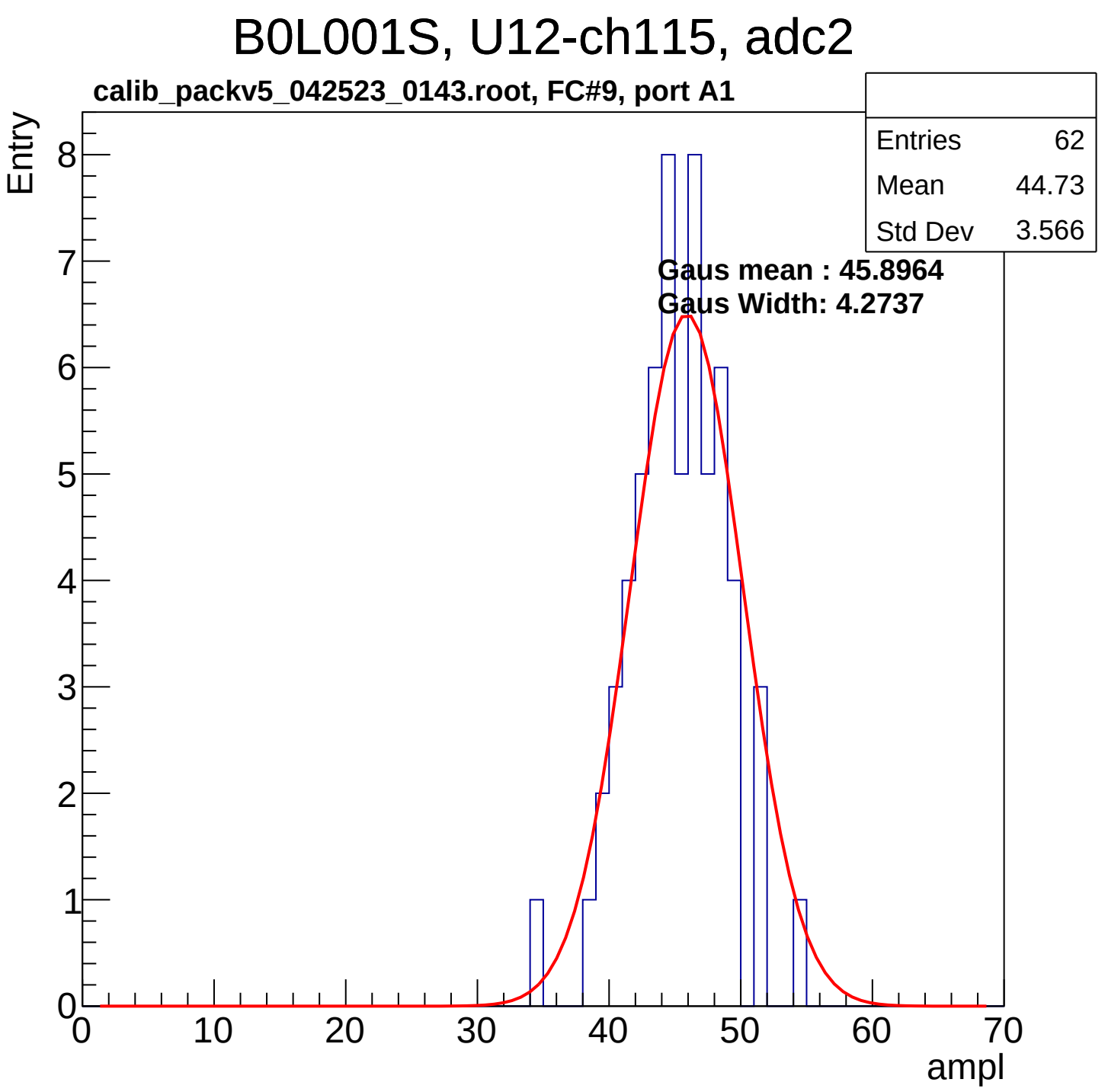
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch115, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 62
Mean 44.73
Std Dev 3.566
Gaus mean : 45.8964
Gaus Width: 4.2737
Entry
ampl
0
1
2
3
4
5
6
7
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0
10
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60
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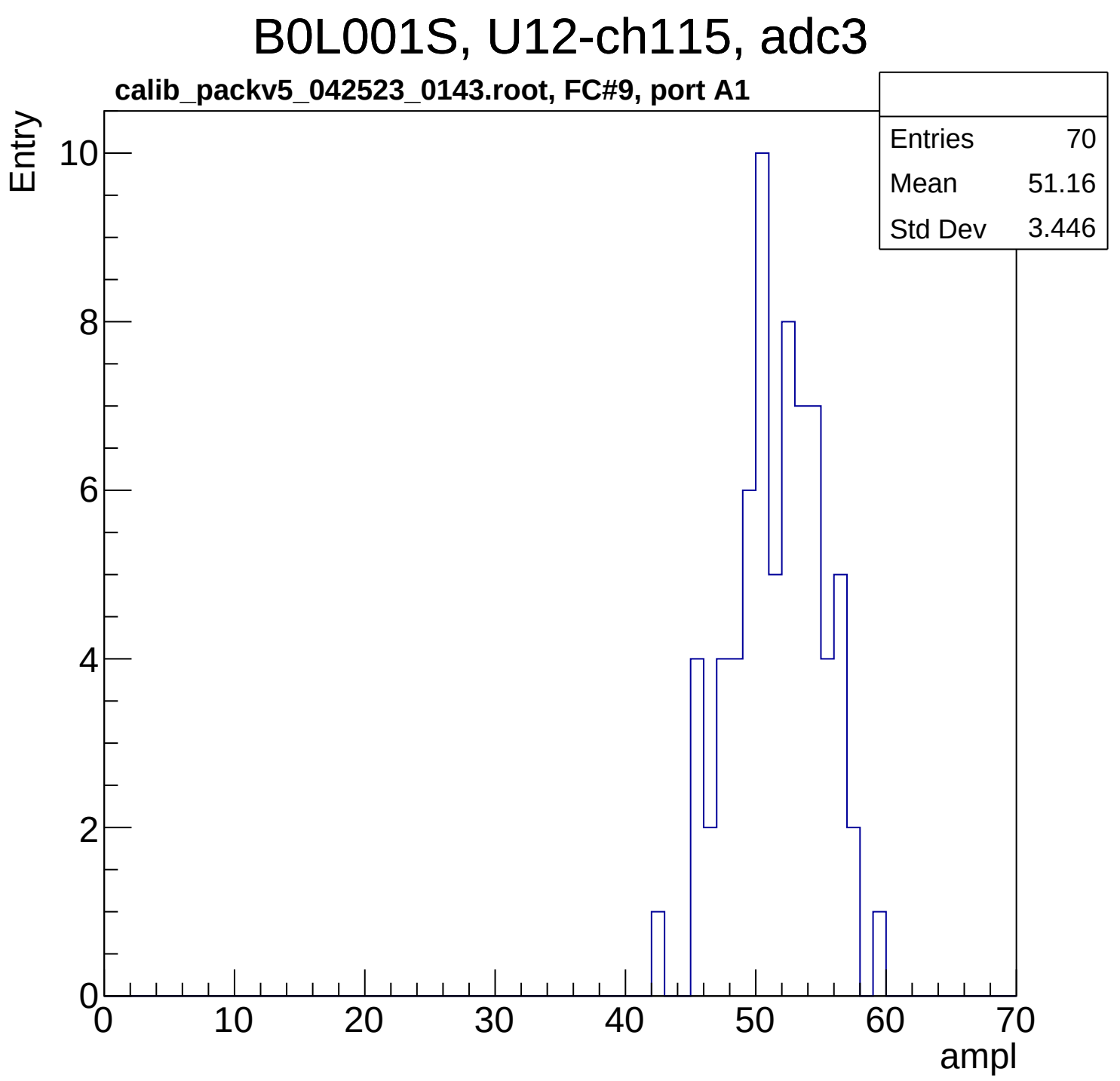
B0L001S, U12-ch115, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 70
Mean 51.16
Std Dev 3.446
Entry
ampl
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4
6
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60
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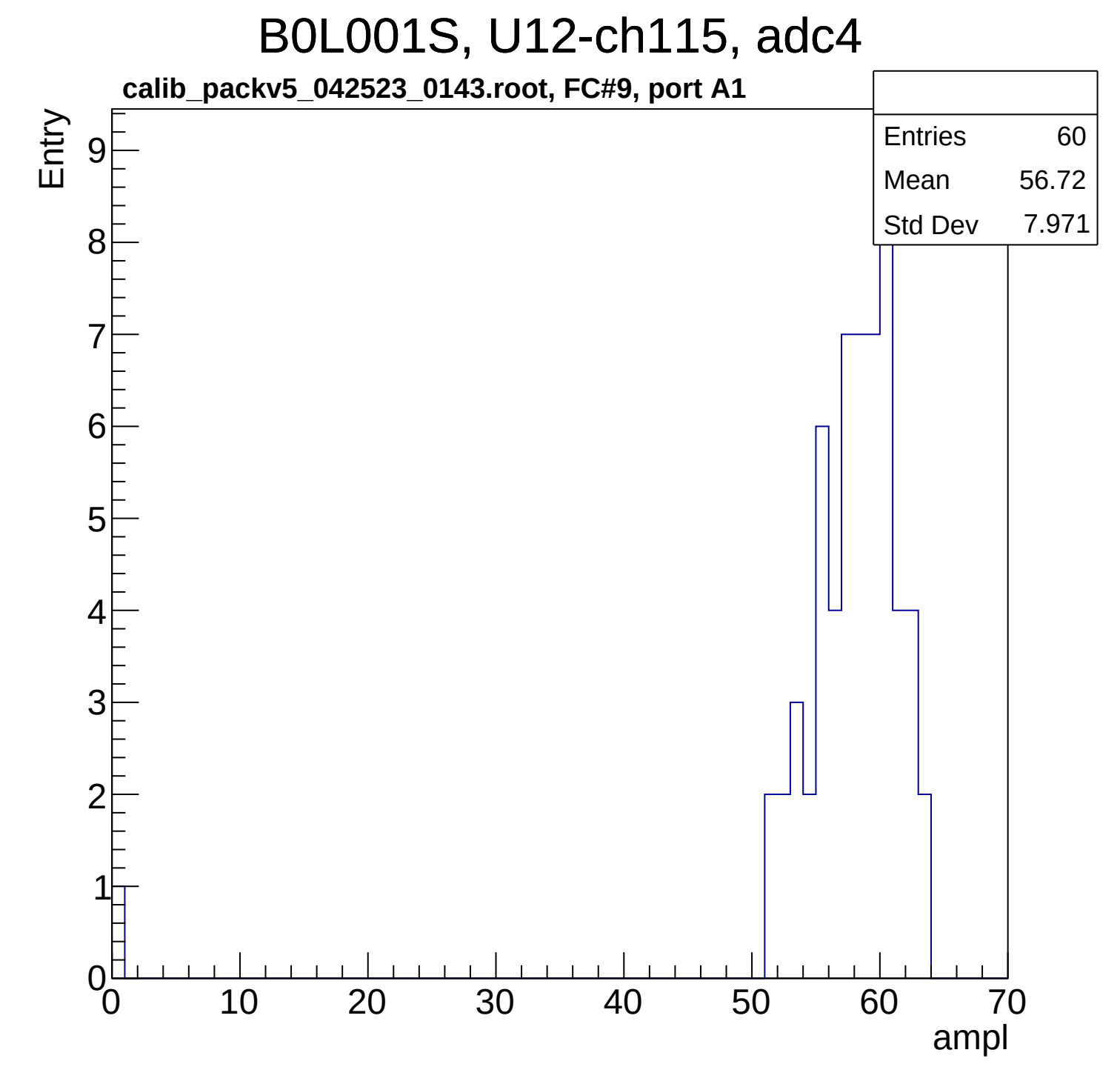
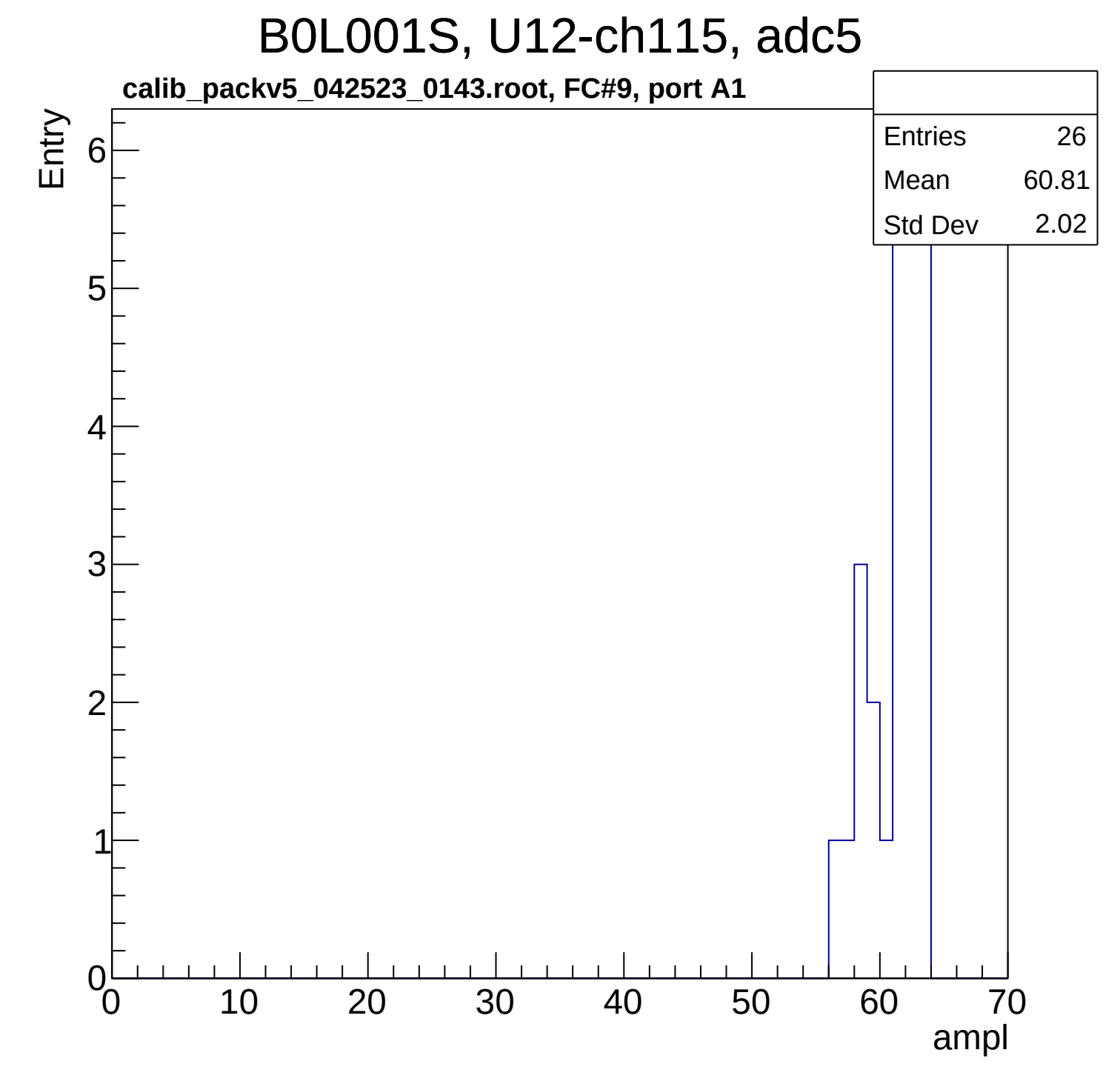
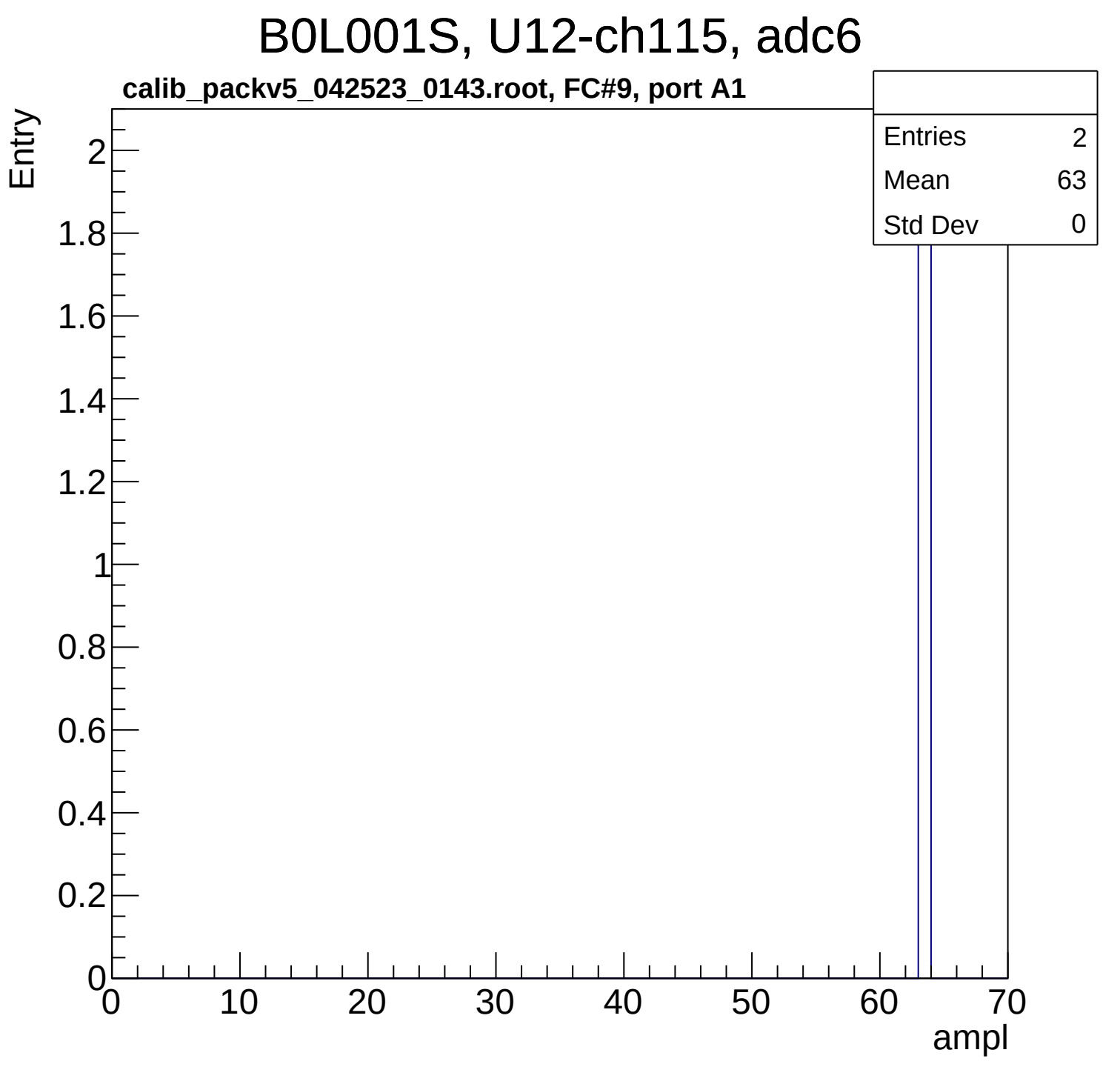
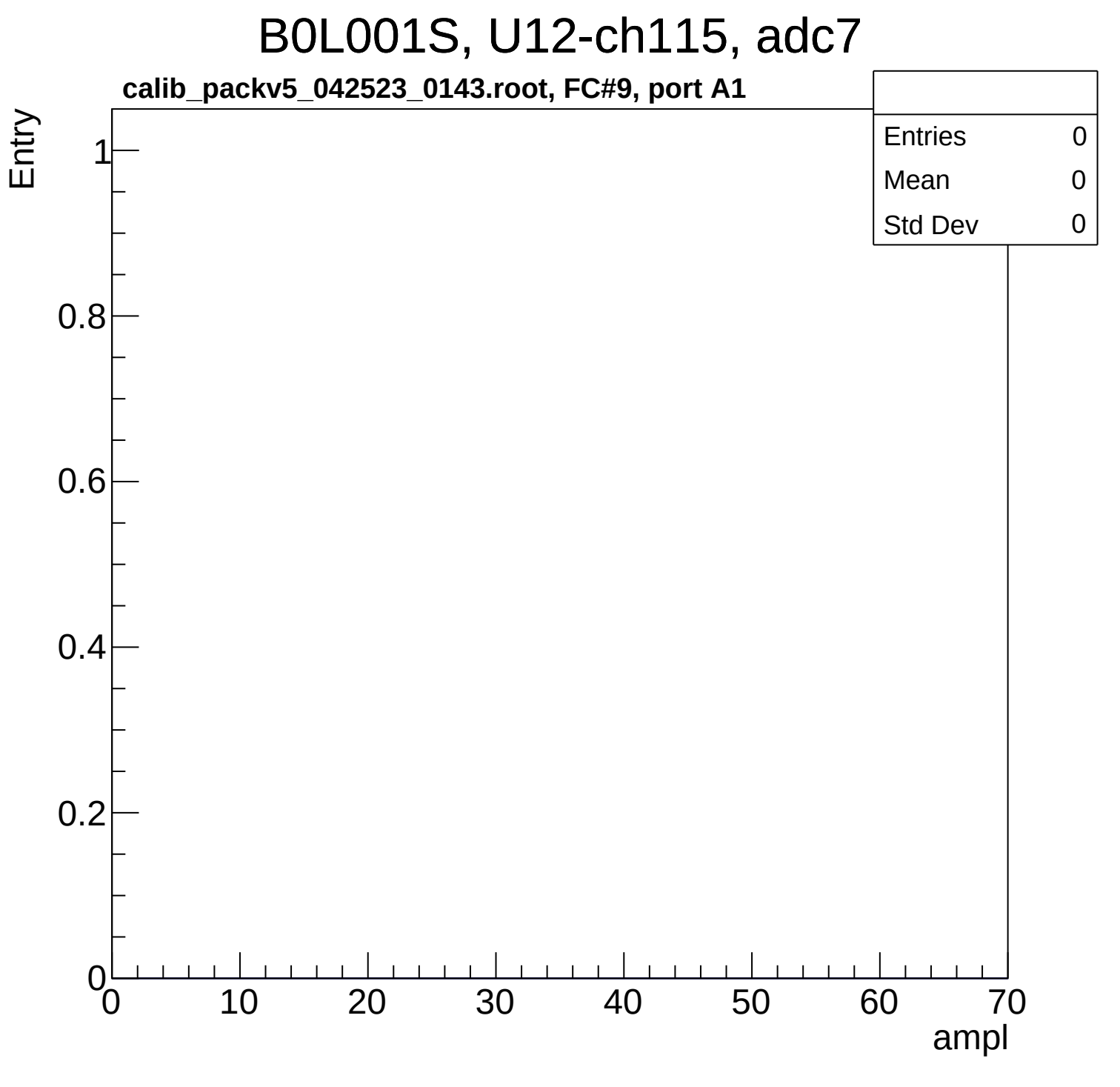
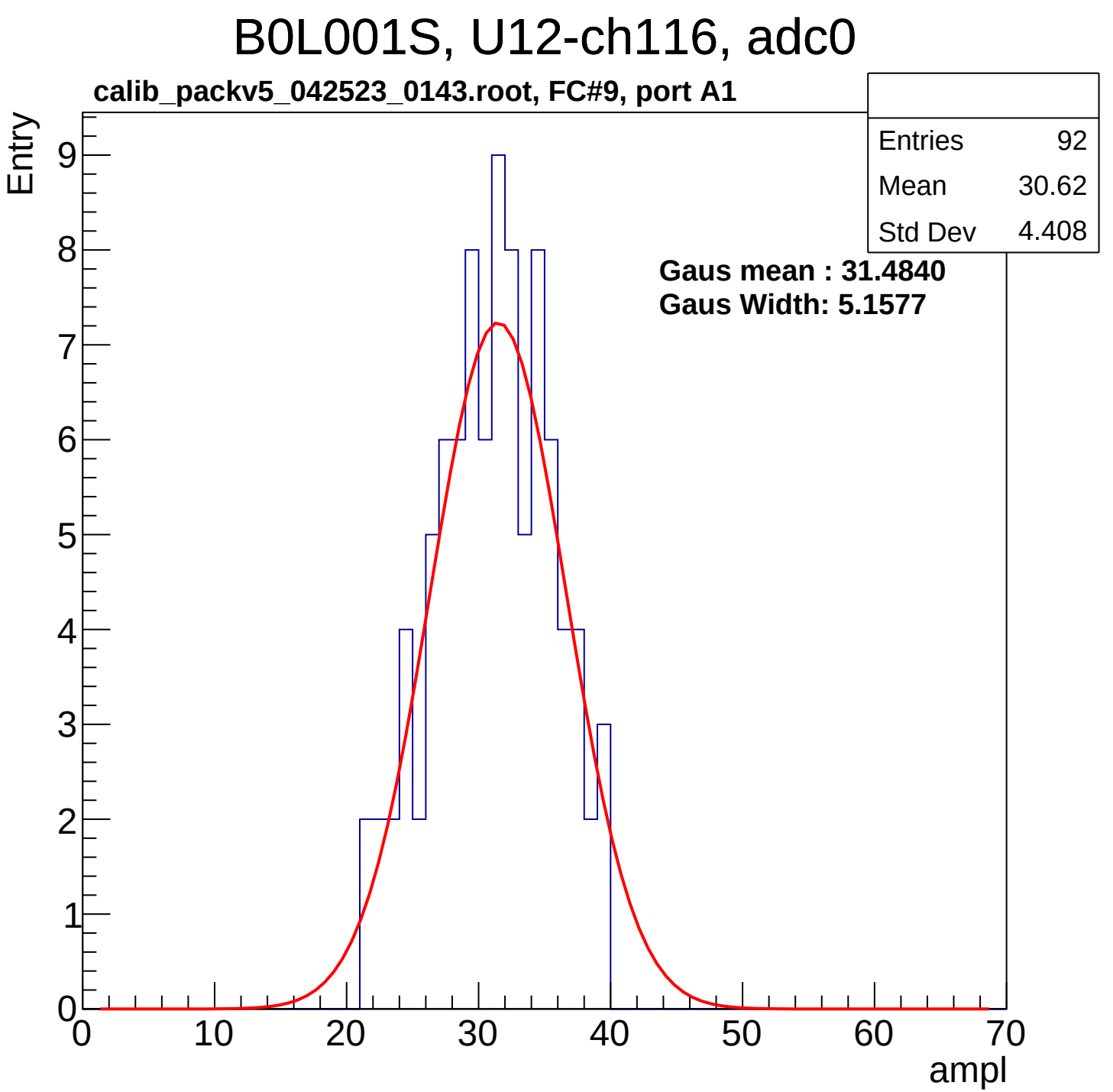
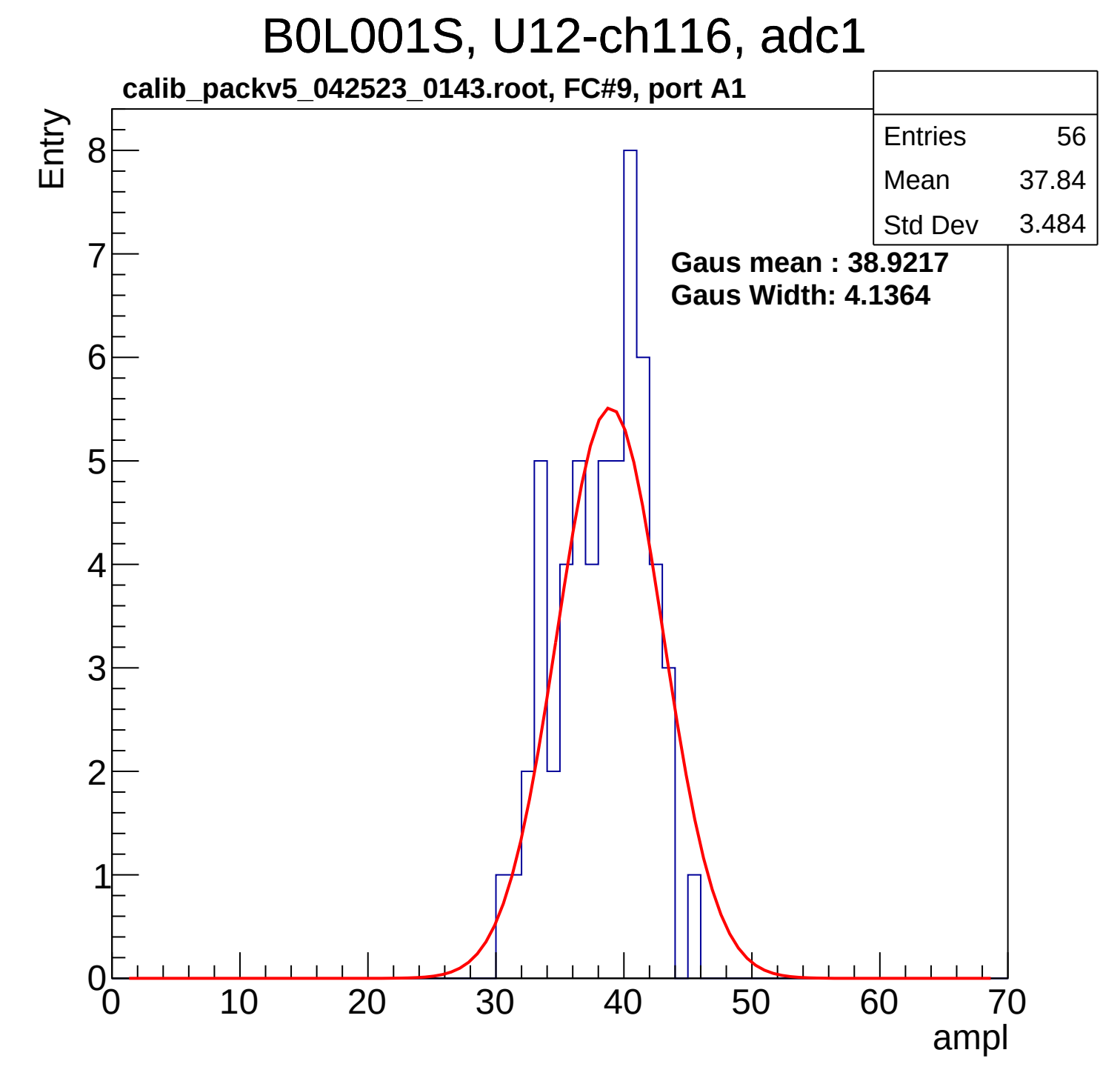

B0L001S, U12-ch115, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 60
Mean 56.72
Std Dev 7.971
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

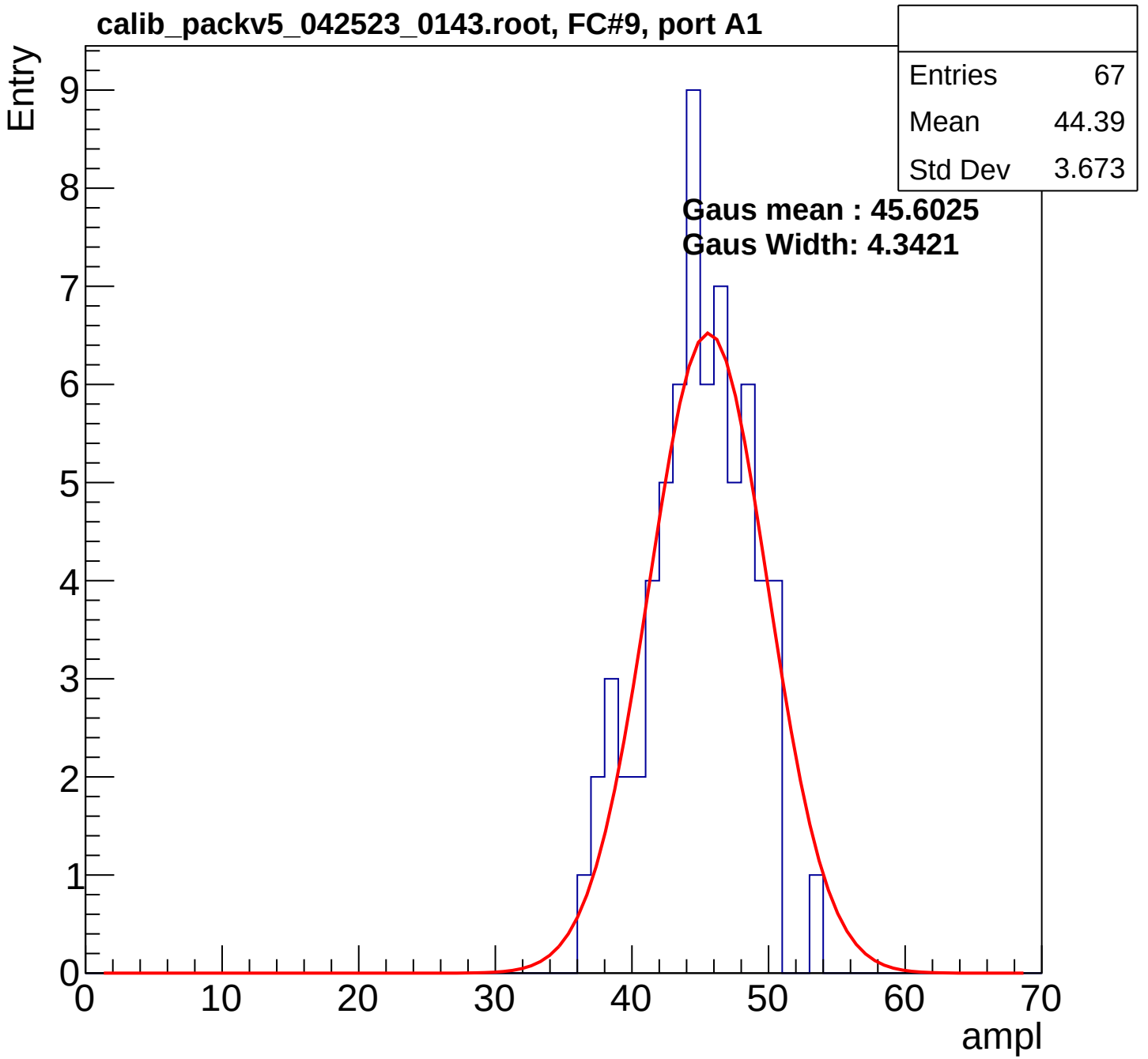

B0L001S, U12-ch115, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 26
Mean 60.81
Std Dev 2.02
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

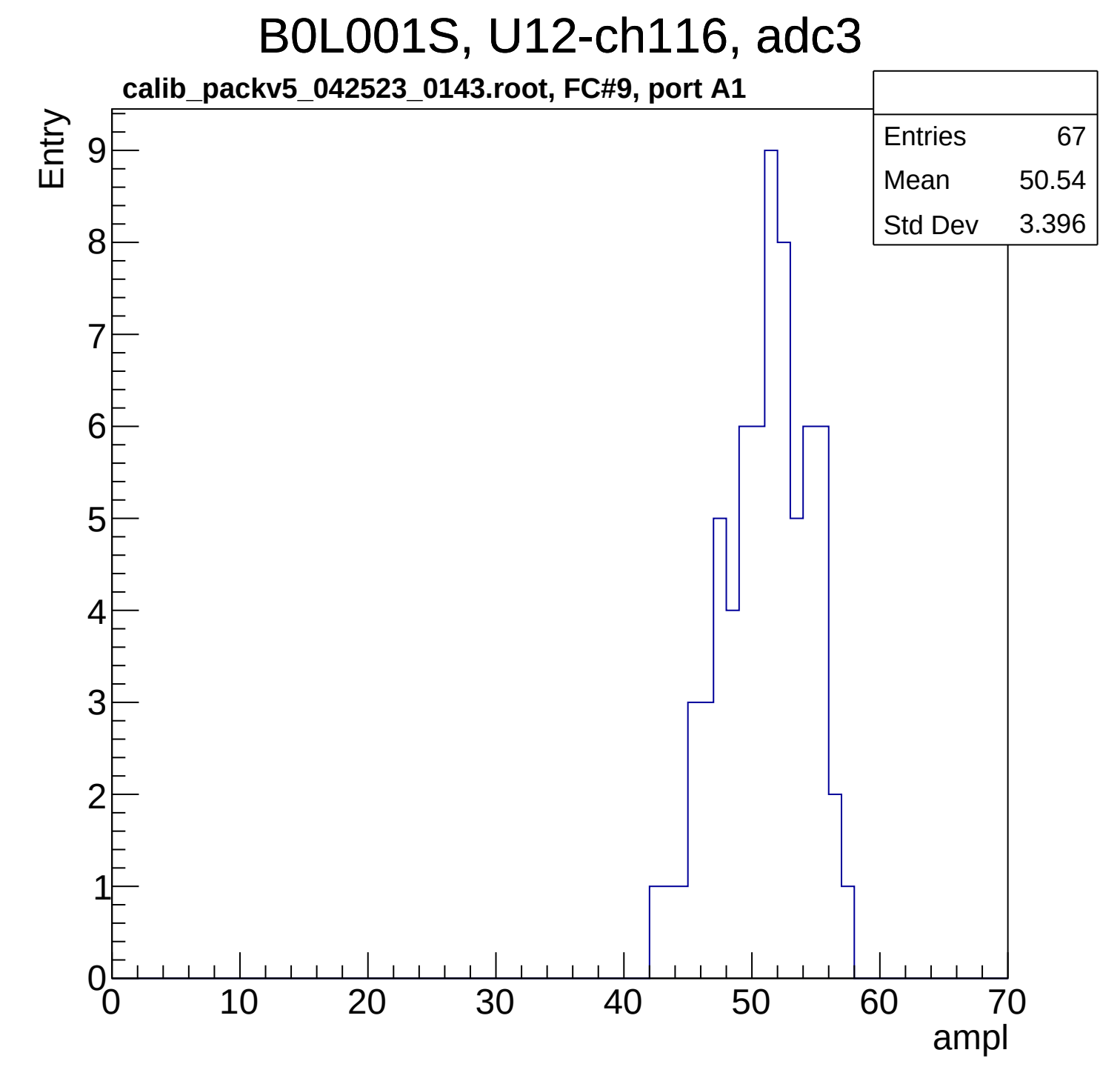

B0L001S, U12-ch115, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

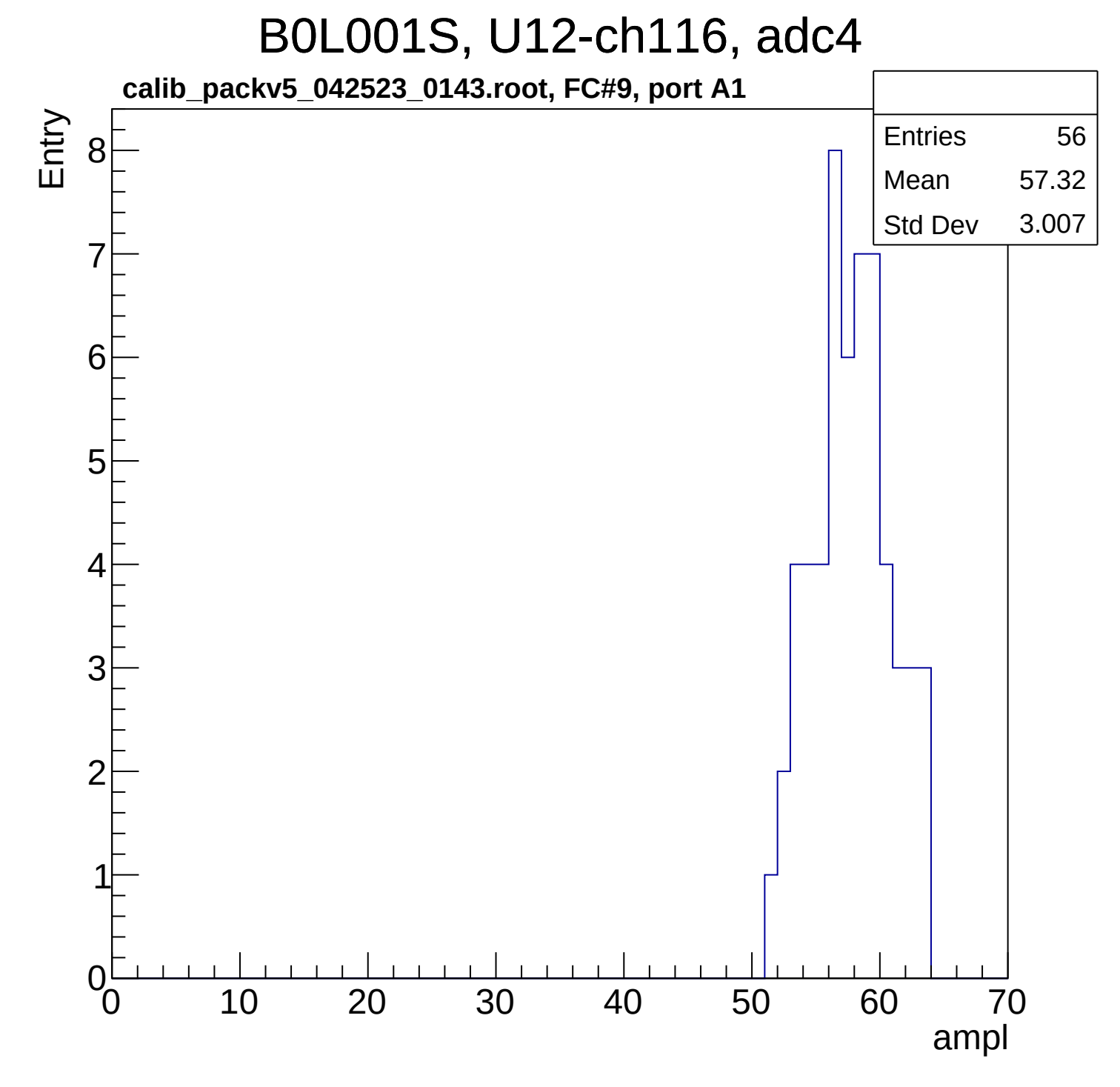

B0L001S, U12-ch115, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

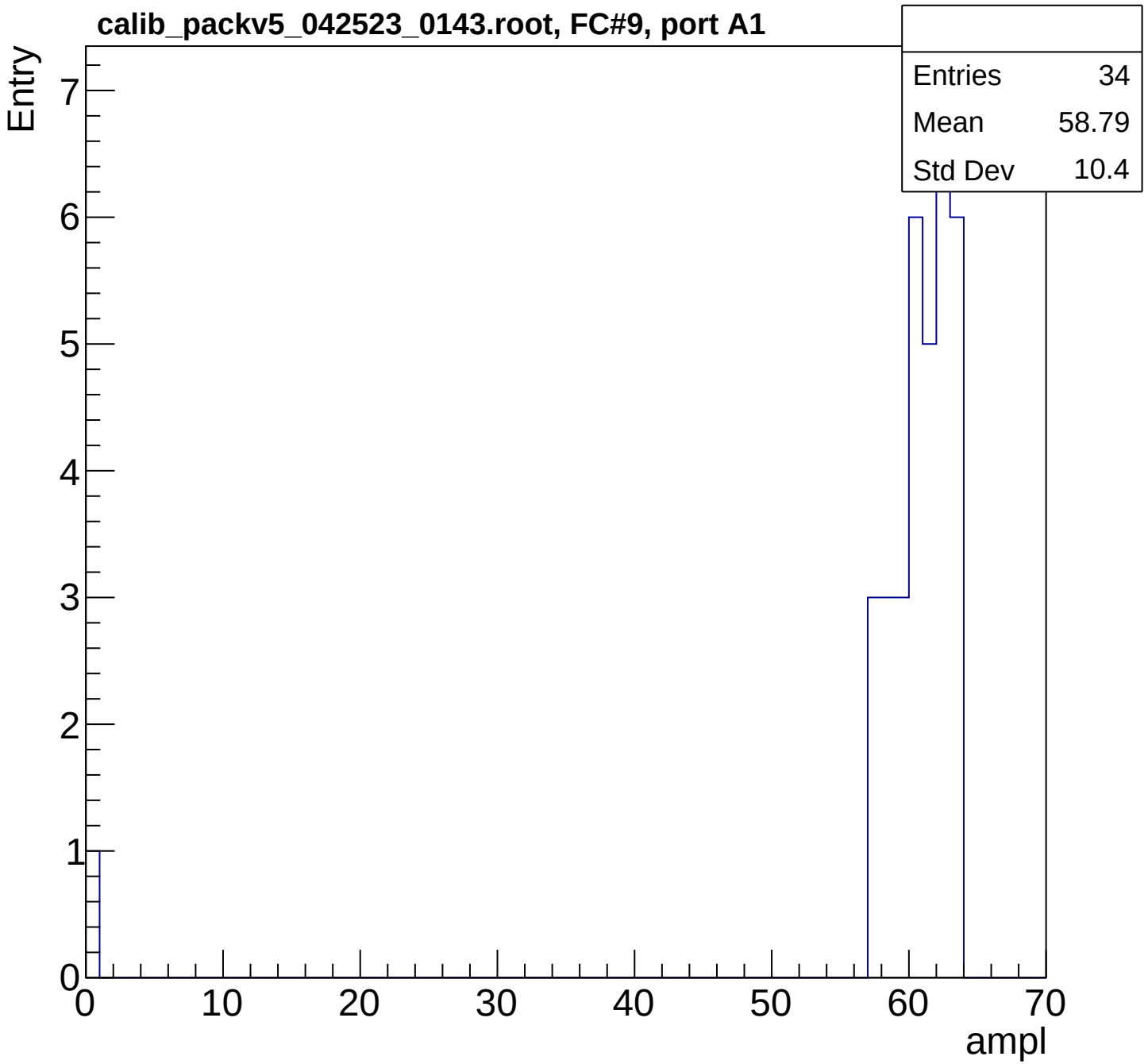

B0L001S, U12-ch116, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 92
Mean 30.62
Std Dev 4.408
Gaus mean : 31.4840
Gaus Width: 5.1577
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

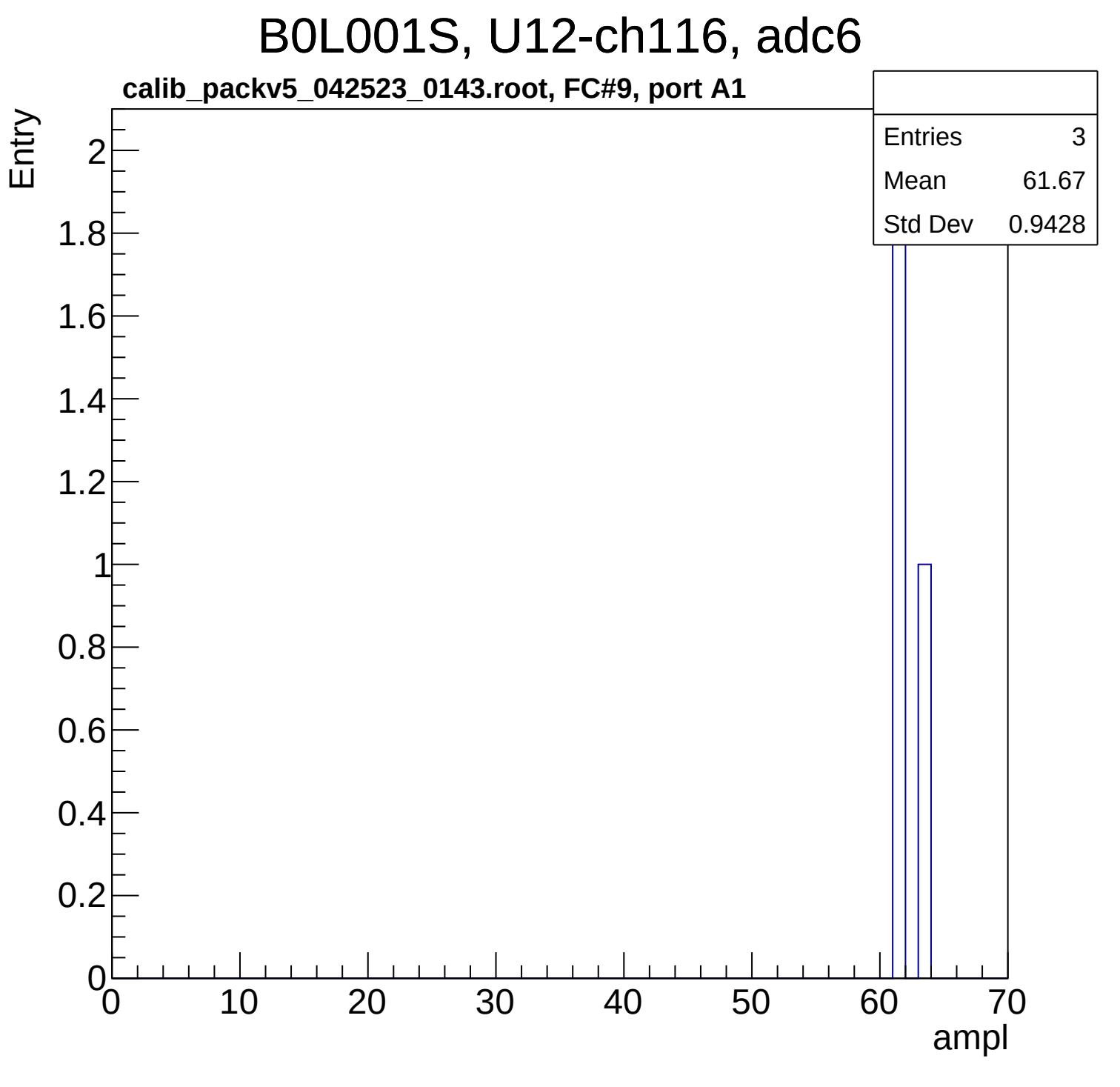

B0L001S, U12-ch116, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 56
Mean 37.84
Std Dev 3.484
Gaus mean : 38.9217
Gaus Width: 4.1364
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

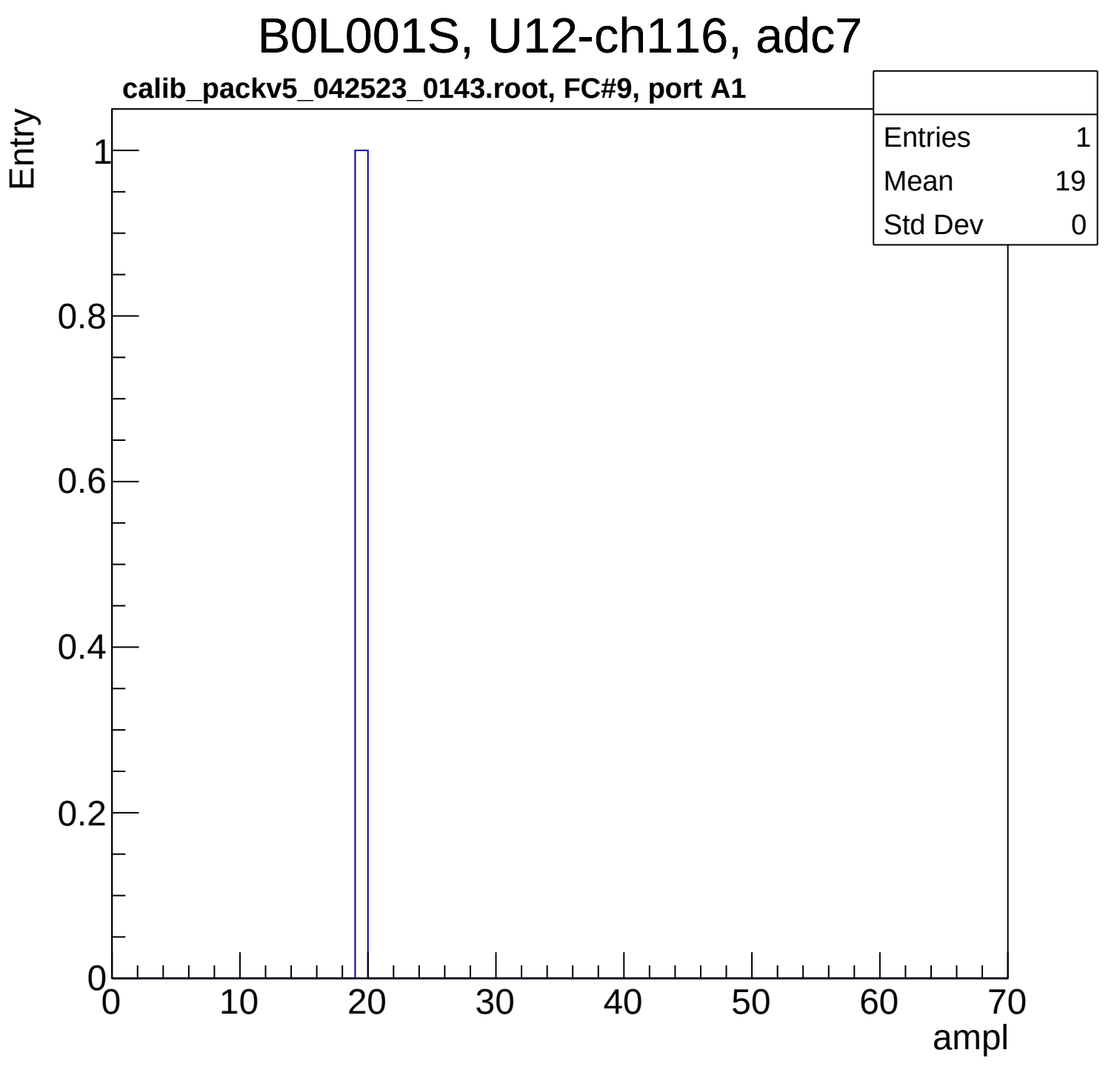

B0L001S, U12-ch116, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 67
Mean 44.39
Std Dev 3.673
Gaus mean : 45.6025
Gaus Width: 4.3421
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

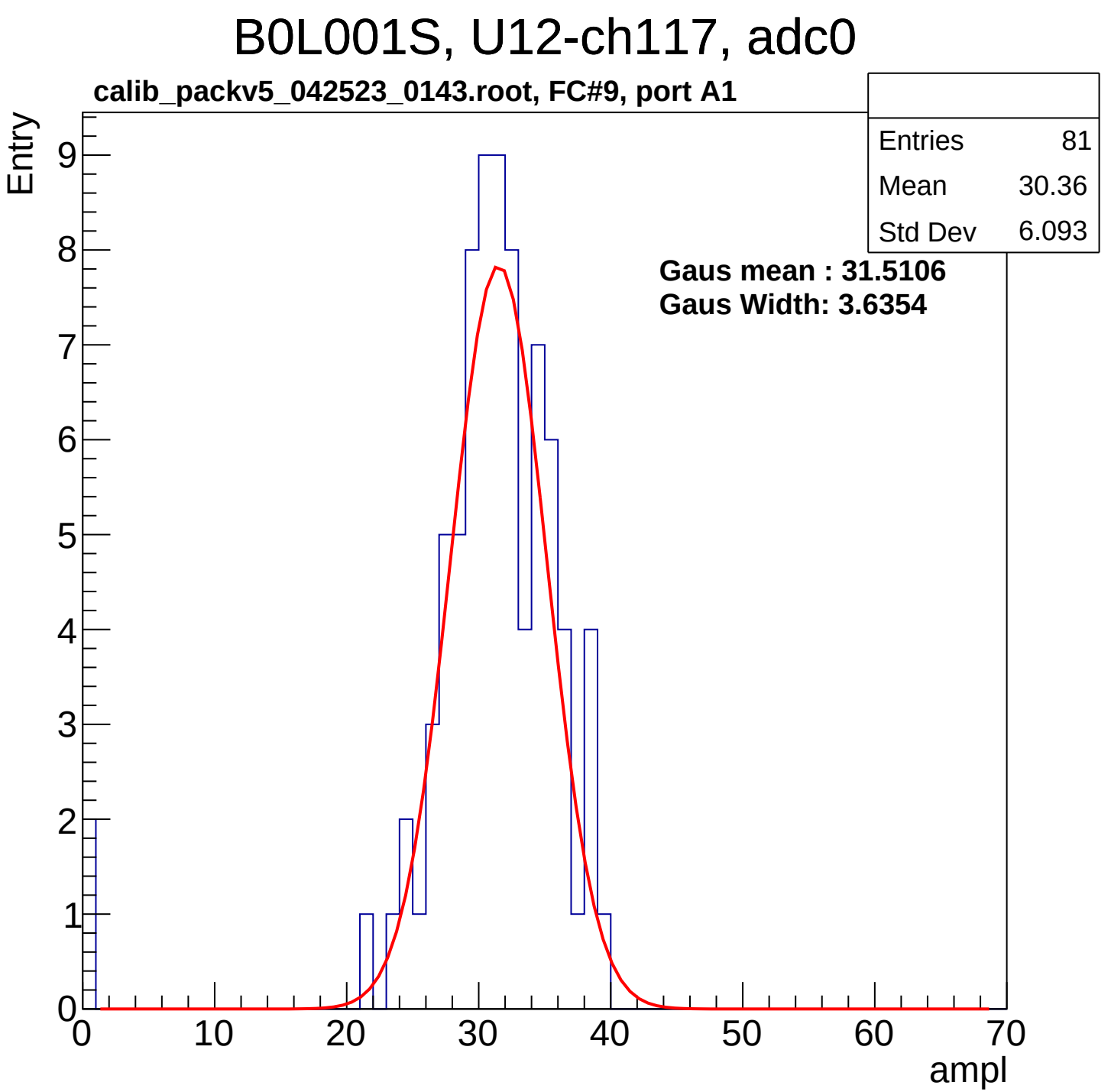

B0L001S, U12-ch116, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 67
Mean 50.54
Std Dev 3.396
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

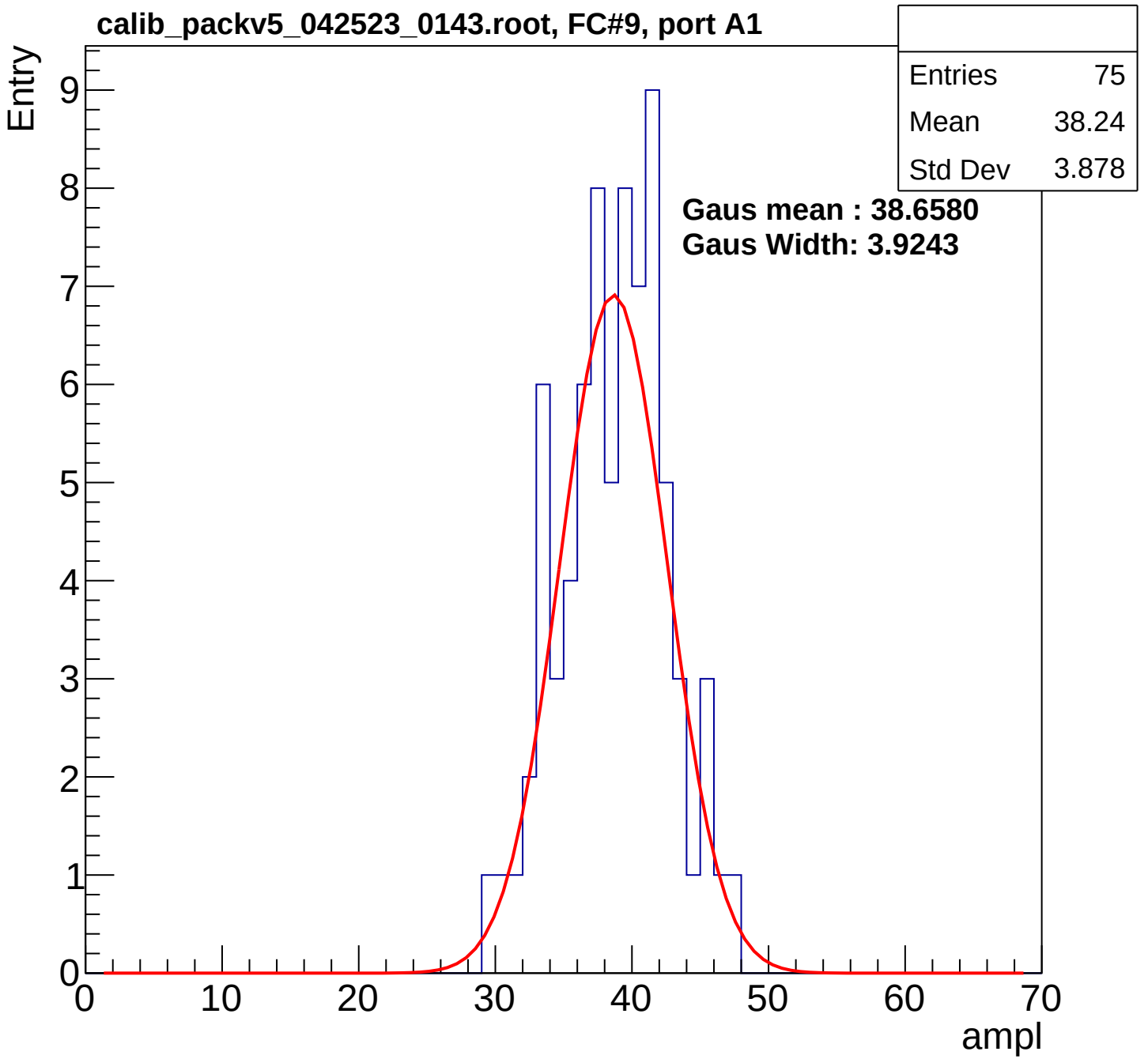

B0L001S, U12-ch116, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 56
Mean 57.32
Std Dev 3.007
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

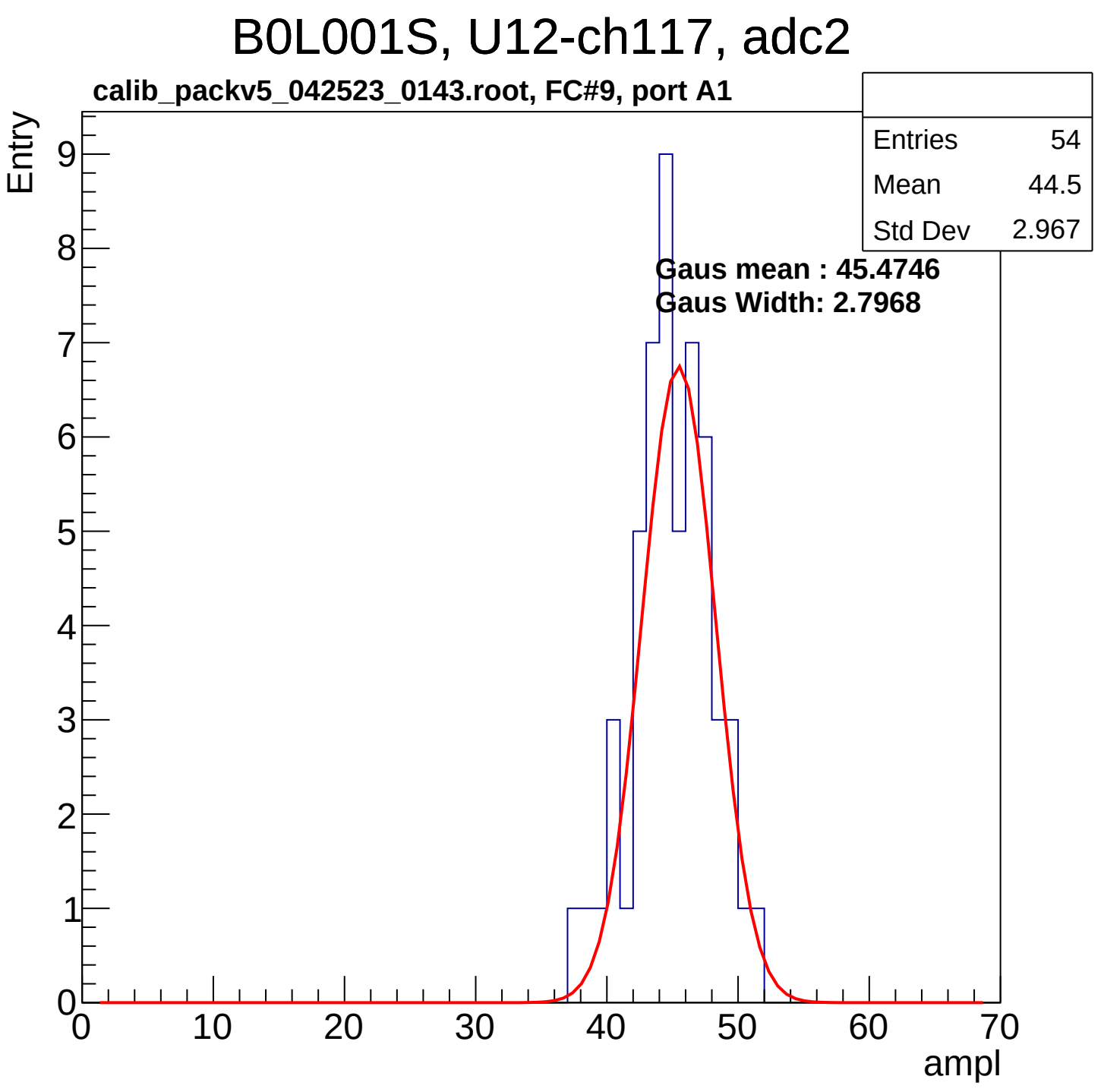

B0L001S, U12-ch116, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 34
Mean 58.79
Std Dev 10.4
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

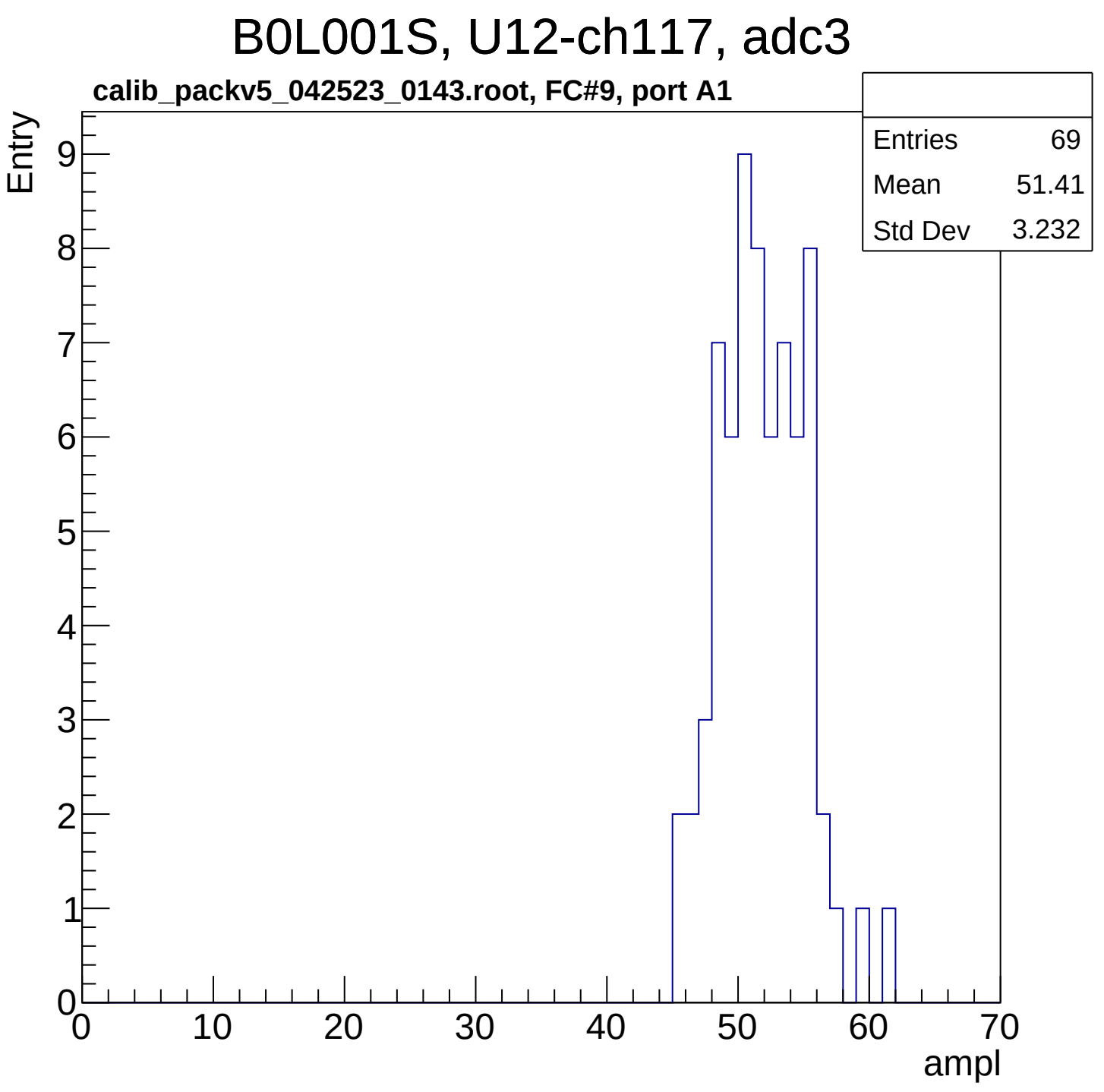

B0L001S, U12-ch116, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 3
Mean 61.67
Std Dev 0.9428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

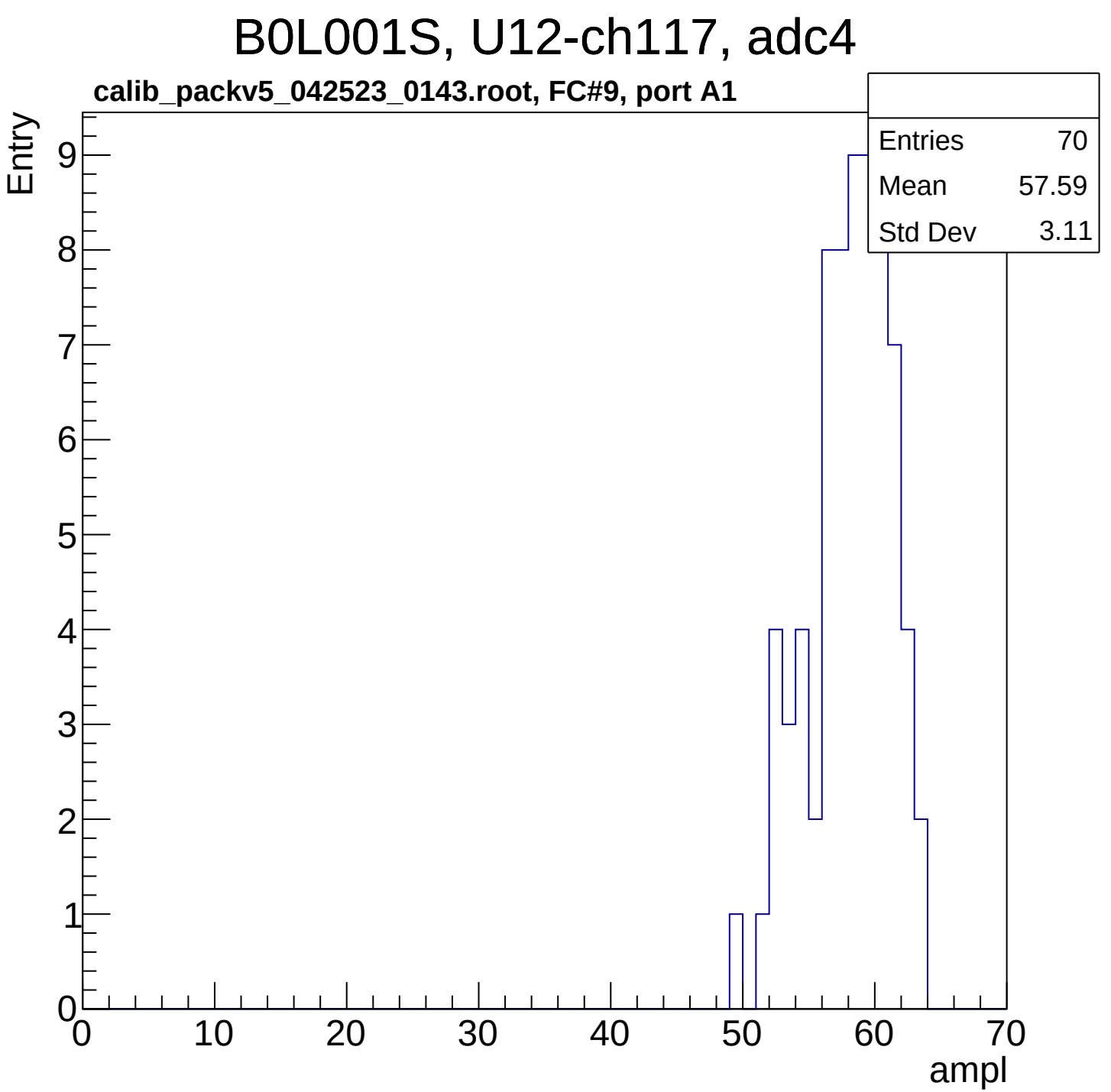

B0L001S, U12-ch116, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 19
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

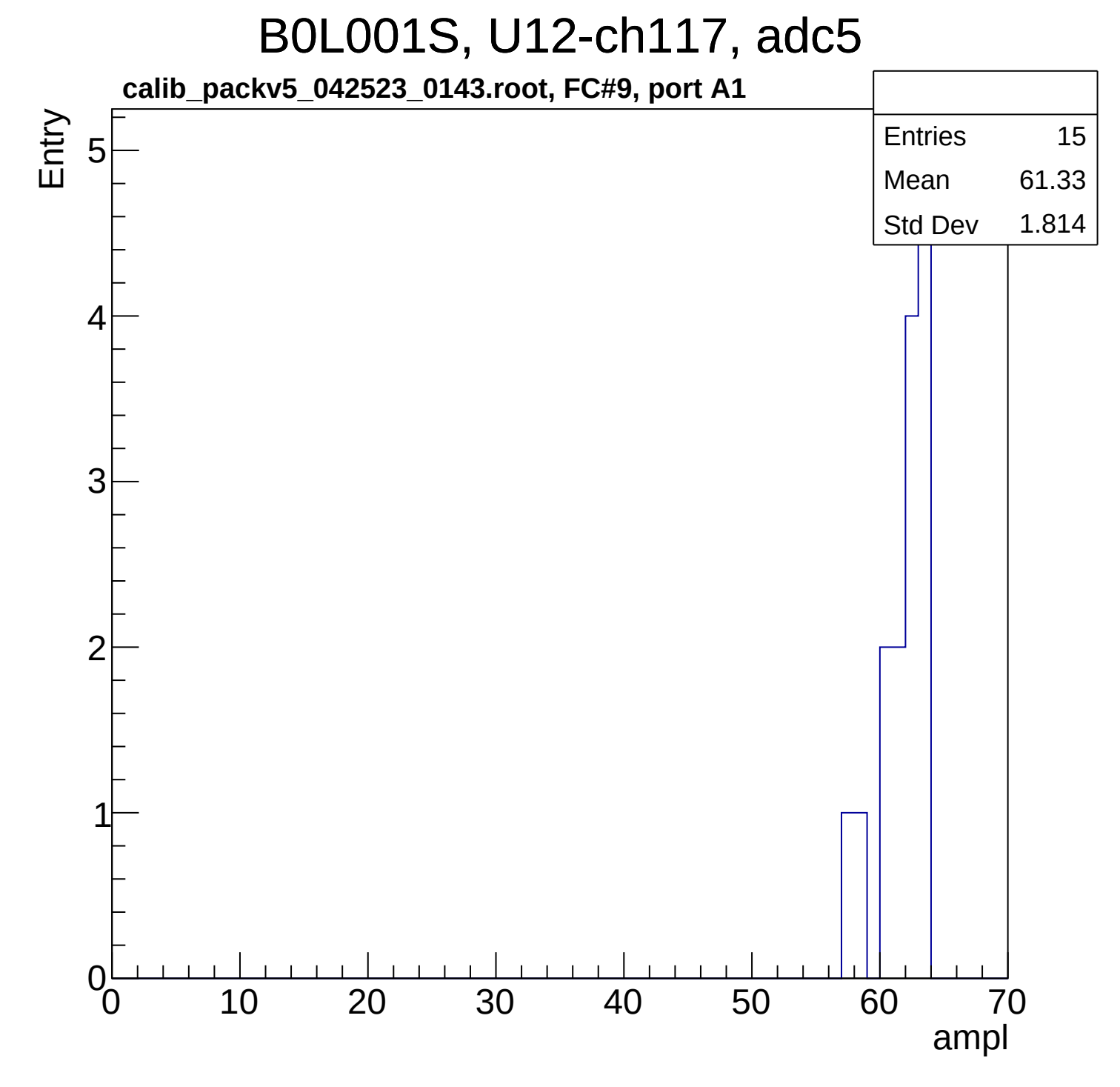

B0L001S, U12-ch117, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 81
Mean 30.36
Std Dev 6.093
Gaus mean : 31.5106
Gaus Width: 3.6354
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

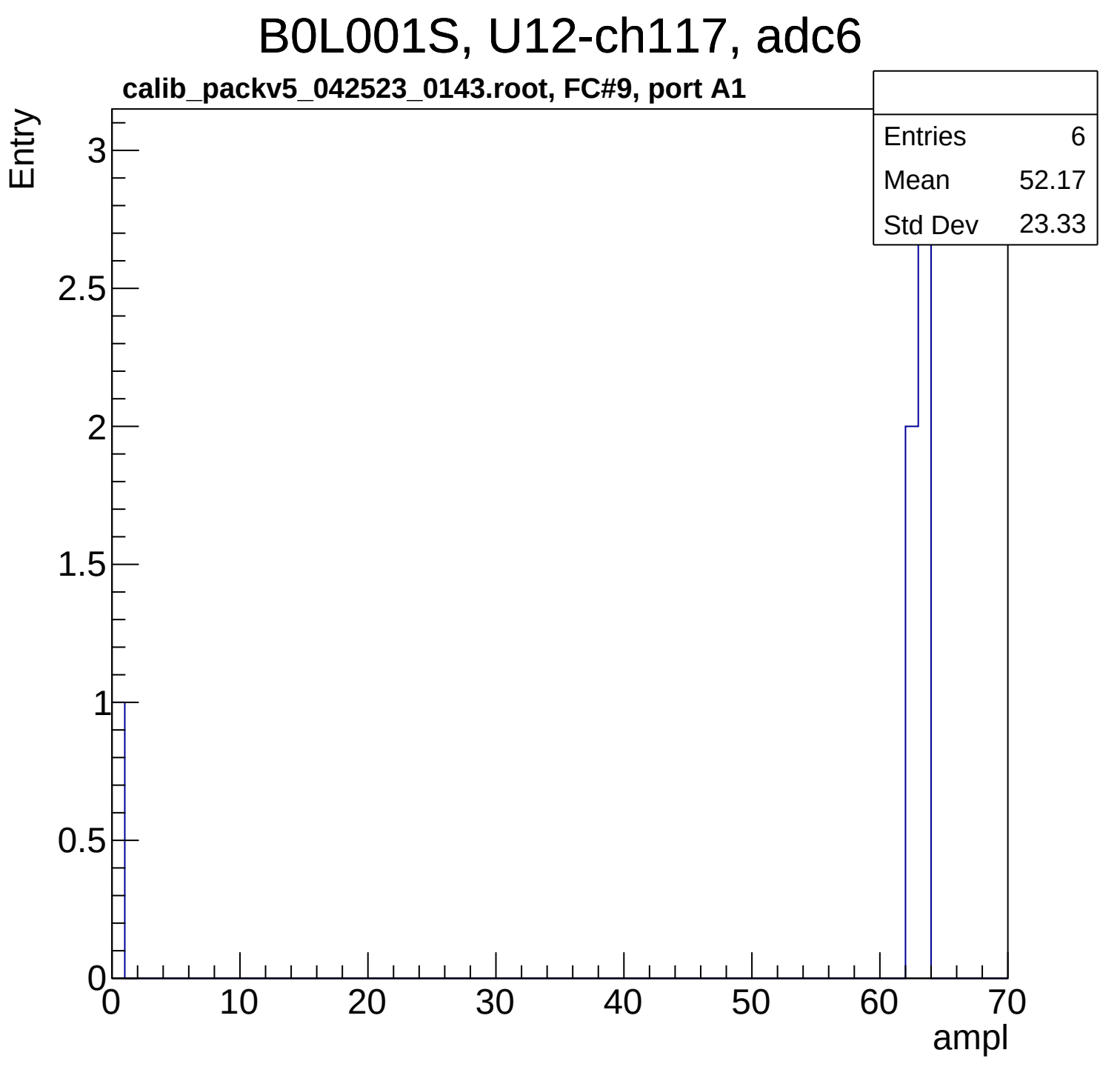

B0L001S, U12-ch117, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 75
Mean 38.24
Std Dev 3.878
Gaus mean : 38.6580
Gaus Width: 3.9243
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

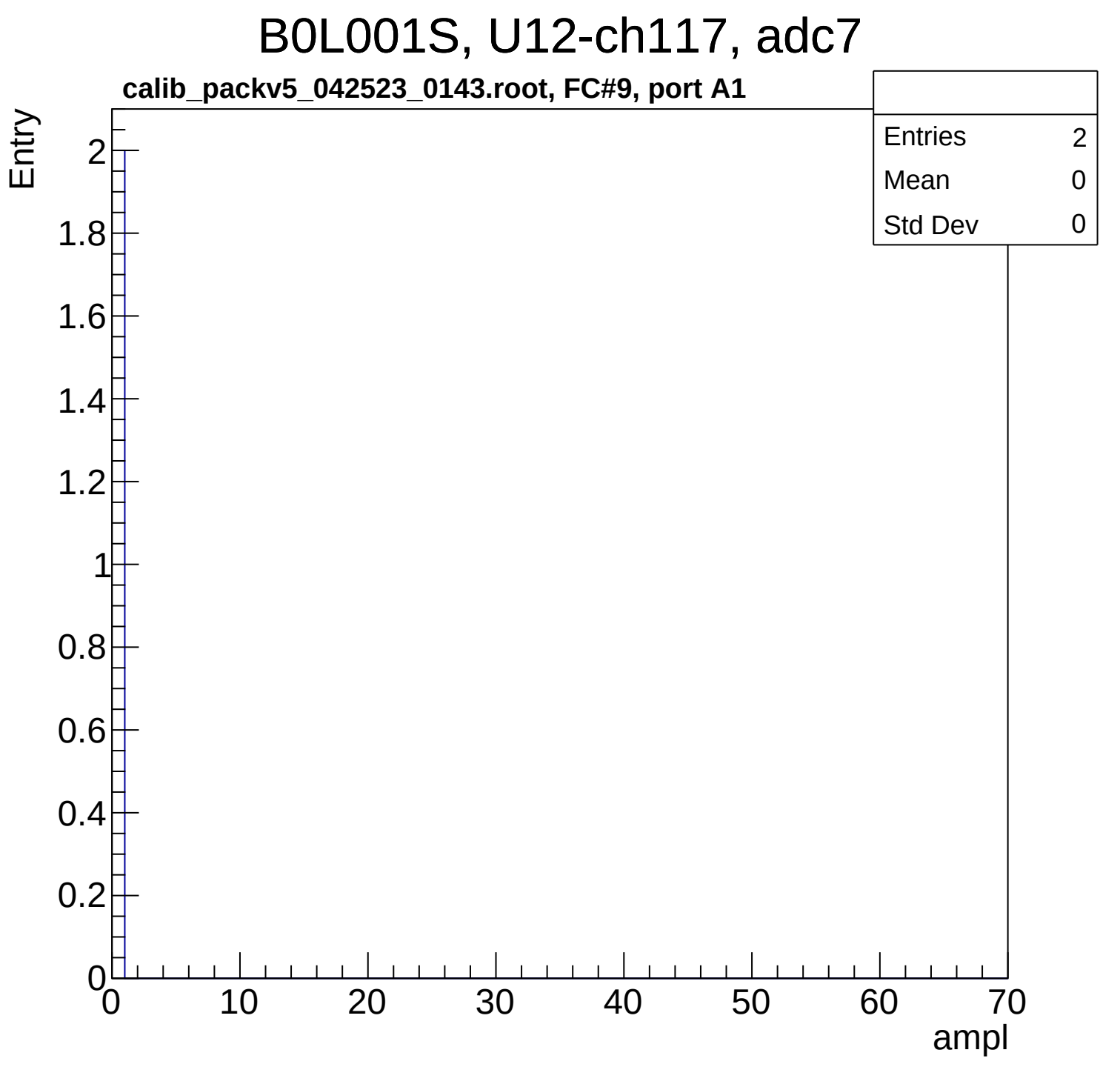

B0L001S, U12-ch117, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 54
Mean 44.5
Std Dev 2.967
Gaus mean : 45.4746
Gaus Width: 2.7968
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

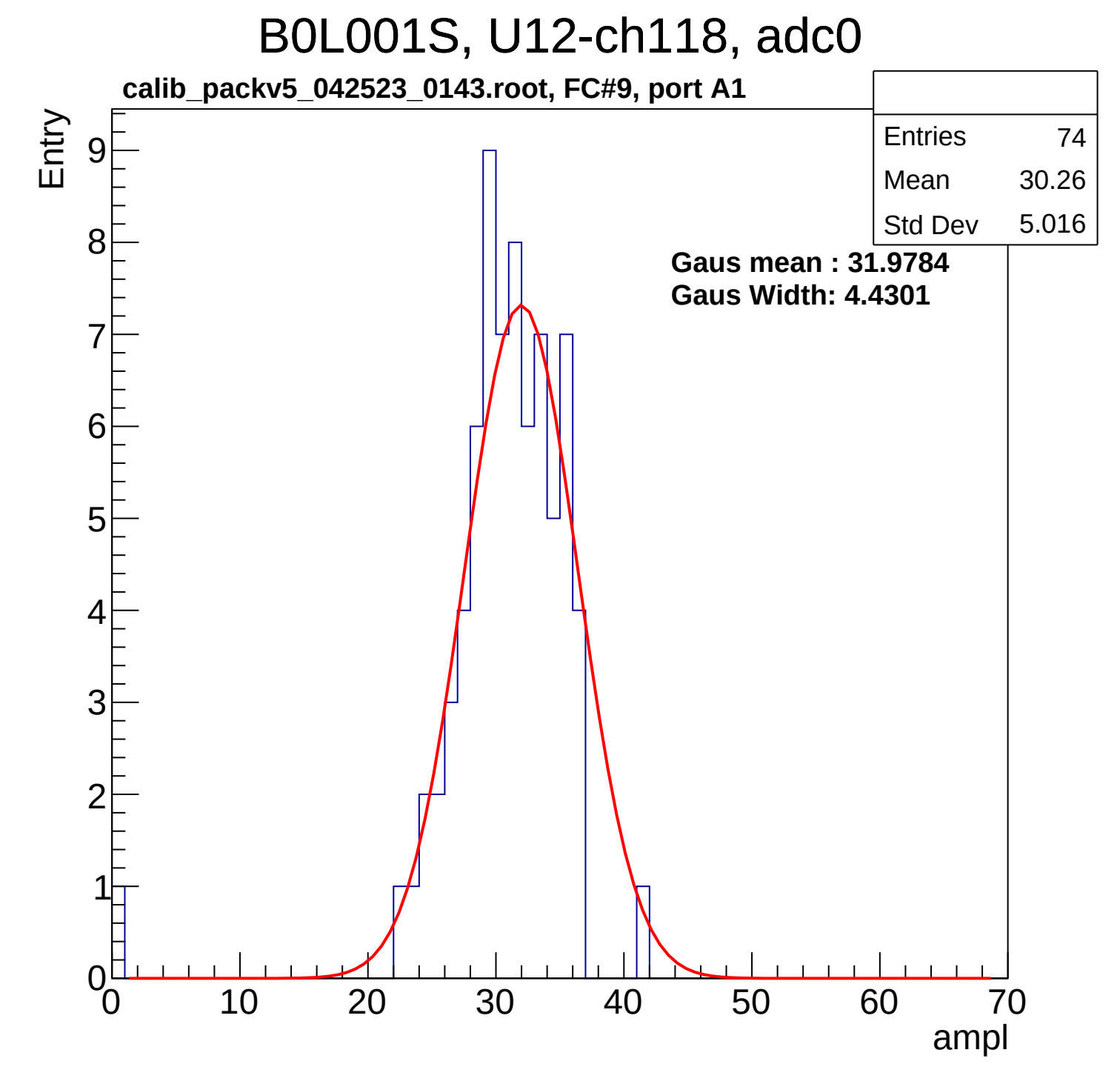

B0L001S, U12-ch117, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 69
Mean 51.41
Std Dev 3.232
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch117, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 70
Mean 57.59
Std Dev 3.11
Entry
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch117, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 15
Mean 61.33
Std Dev 1.814
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch117, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 6
Mean 52.17
Std Dev 23.33
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B0L001S, U12-ch117, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L001S, U12-ch118, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 74
Mean 30.26
Std Dev 5.016
Gaus mean : 31.9784
Gaus Width: 4.4301
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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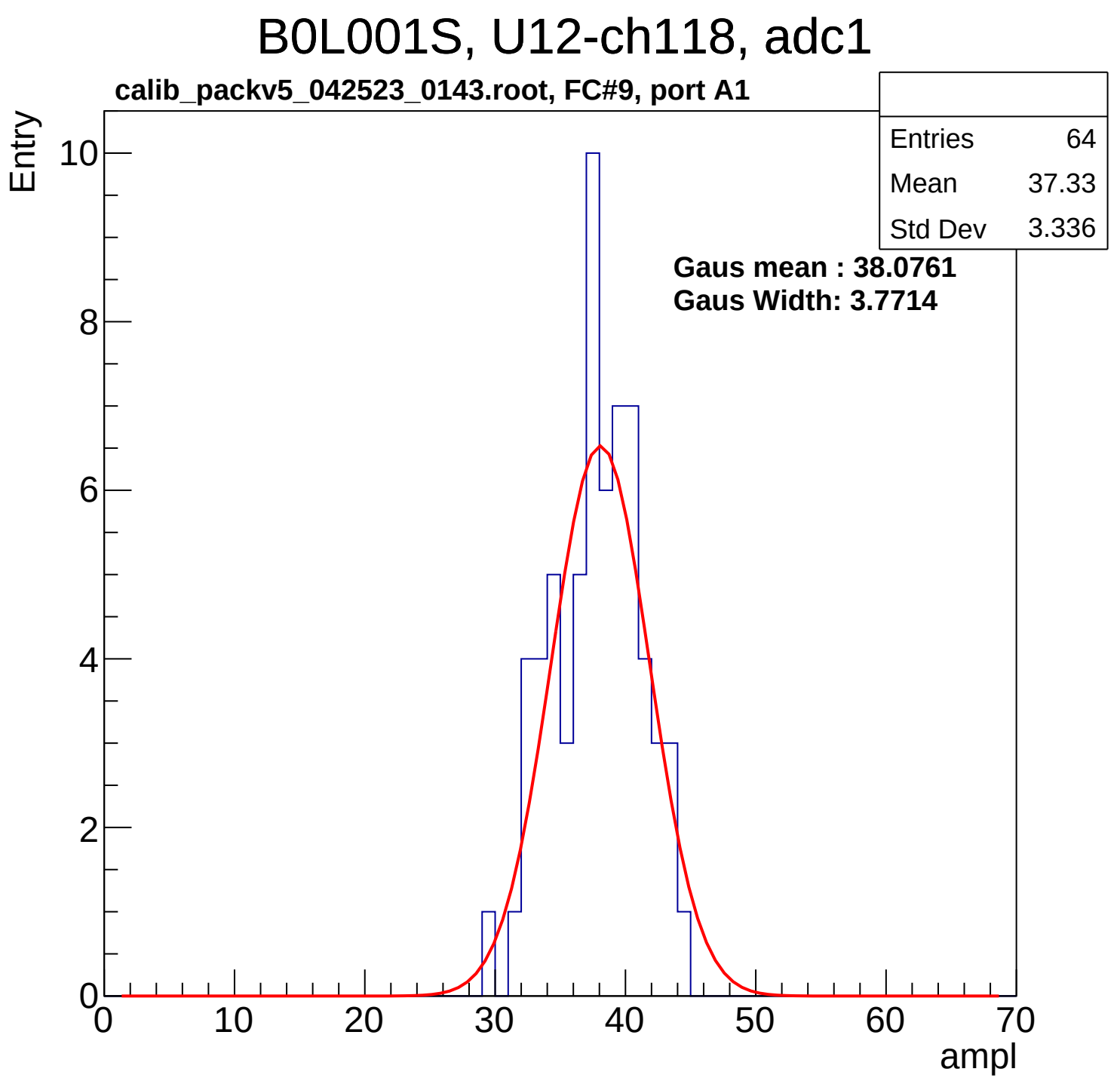
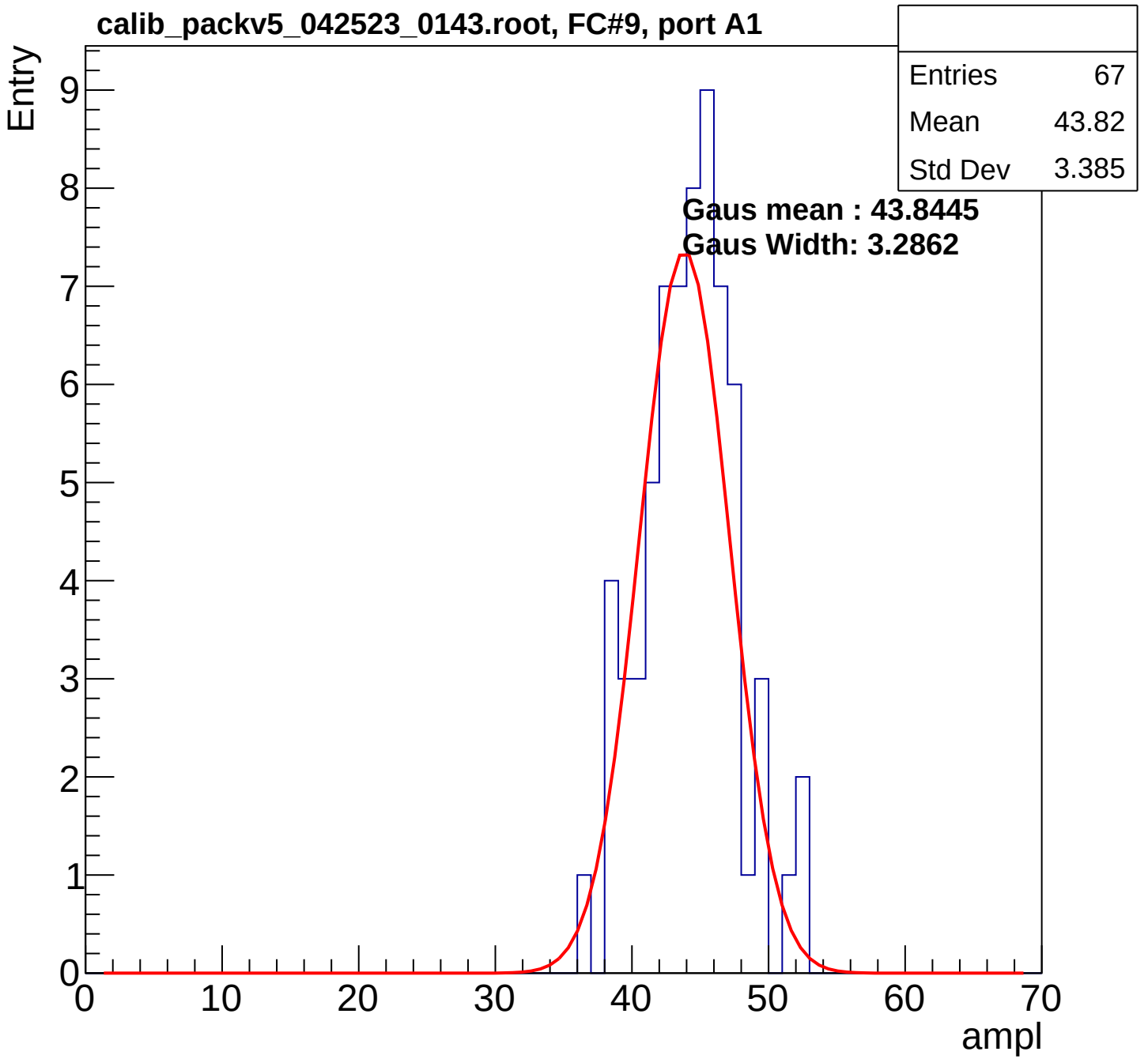
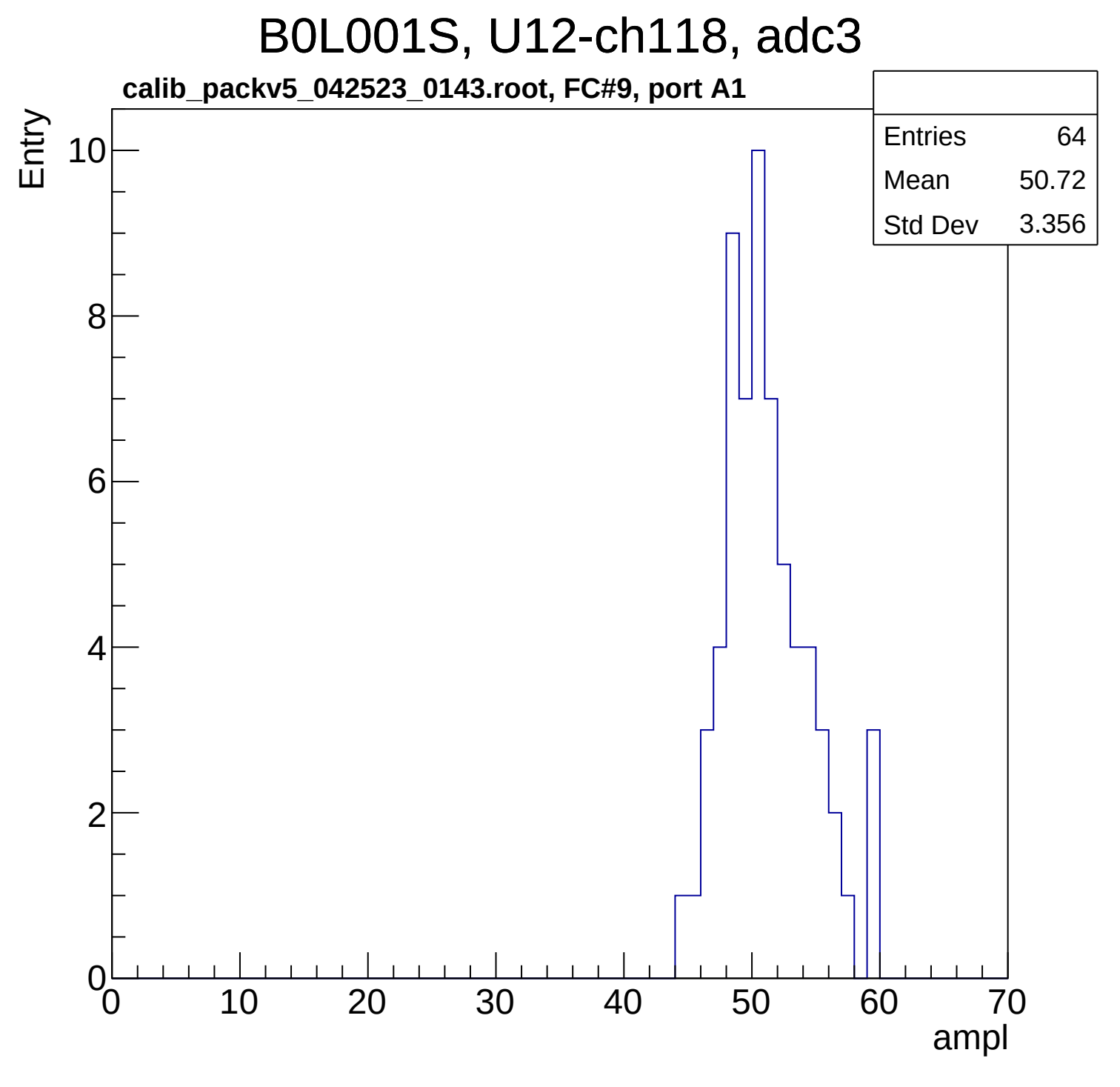
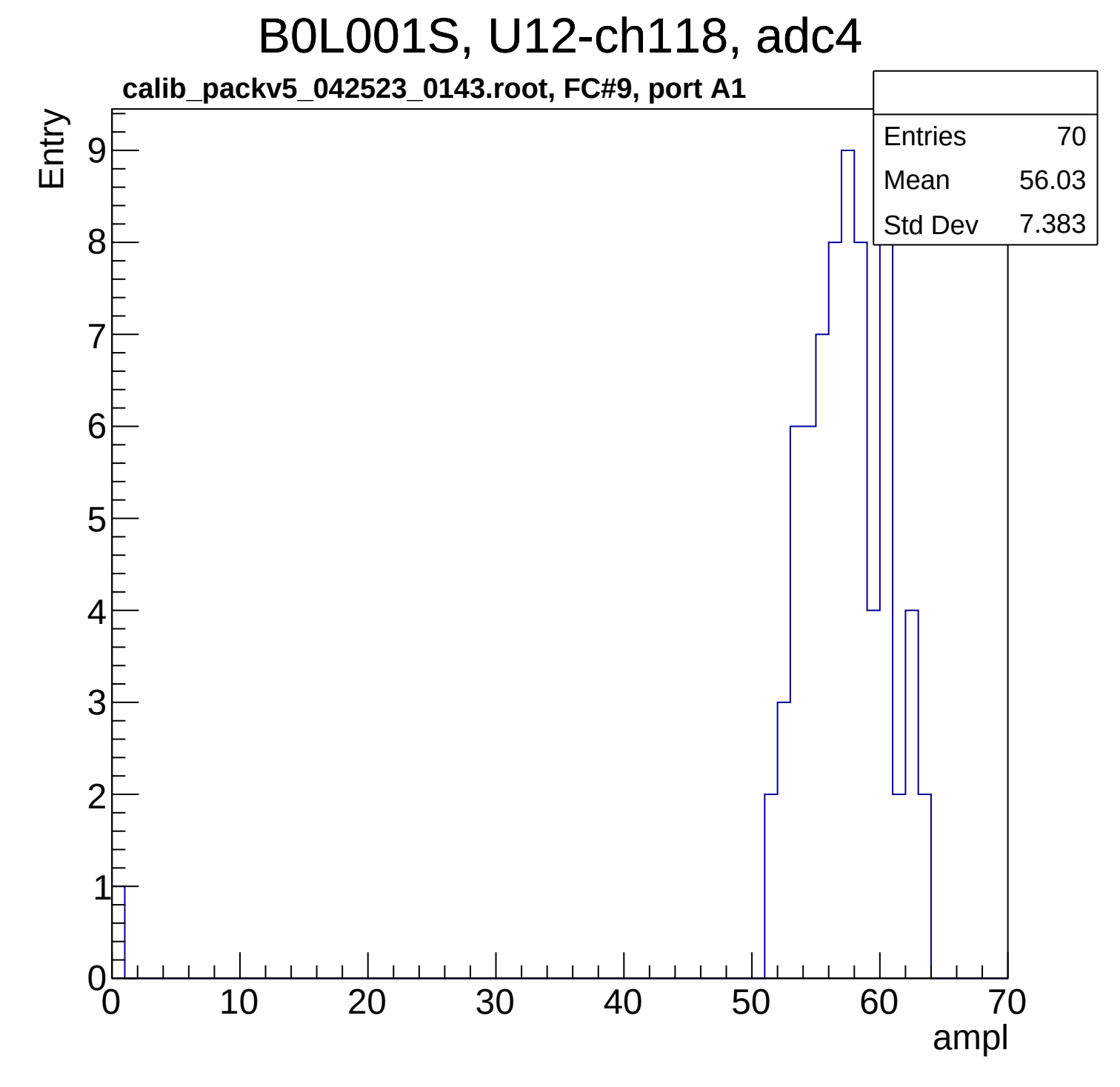
40
50
60
70


B0L001S, U12-ch118, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 64
Mean 37.33
Std Dev 3.336
Gaus mean : 38.0761
Gaus Width: 3.7714
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch118, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 67
Mean 43.82
Std Dev 3.385
Gaus mean : 43.8445
Gaus Width: 3.2862
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch118, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 64
Mean 50.72
Std Dev 3.356
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch118, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 70
Mean 56.03
Std Dev 7.383
Entry
ampl
0
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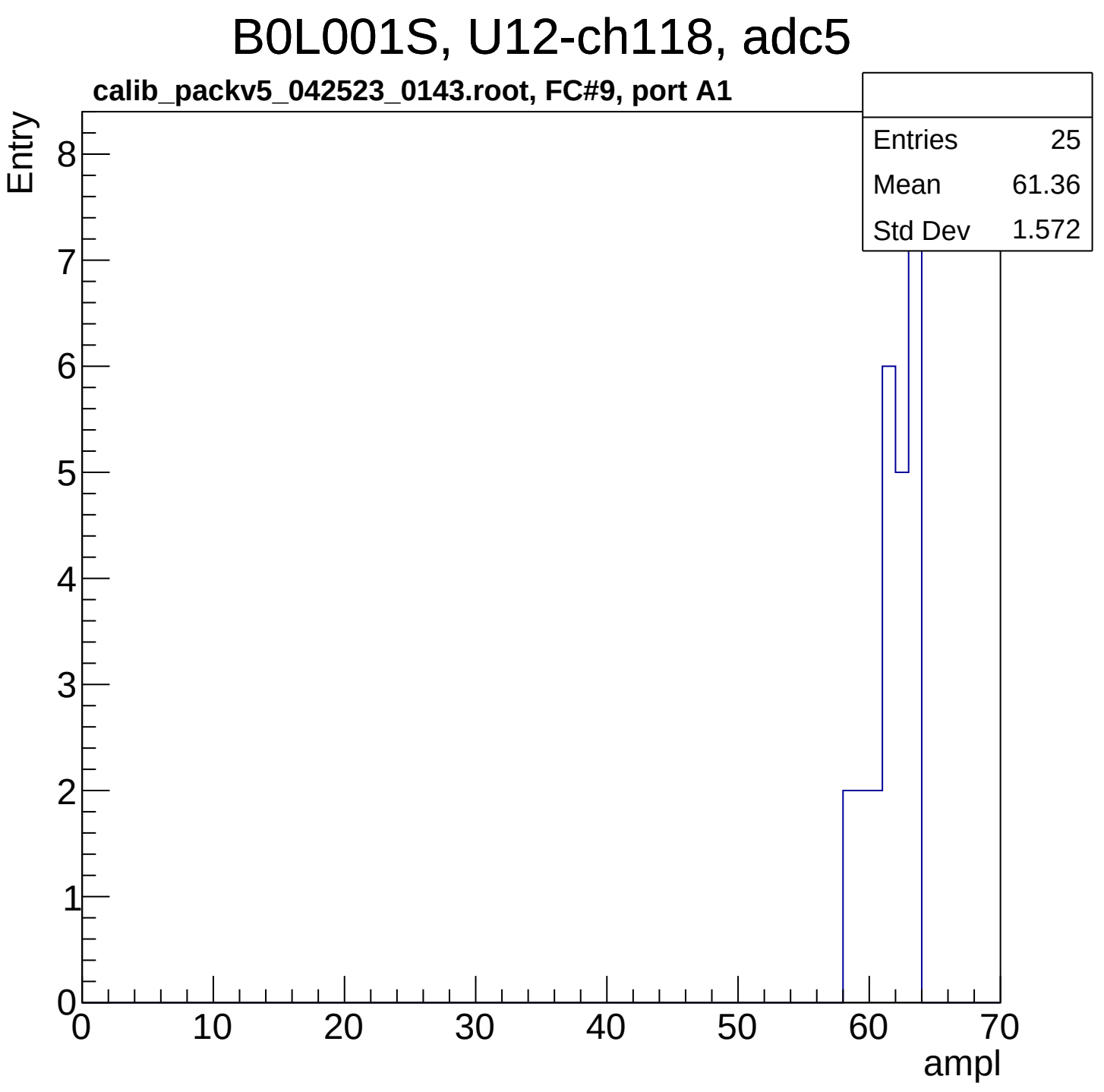
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch118, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 25
Mean 61.36
Std Dev 1.572
Entry
ampl
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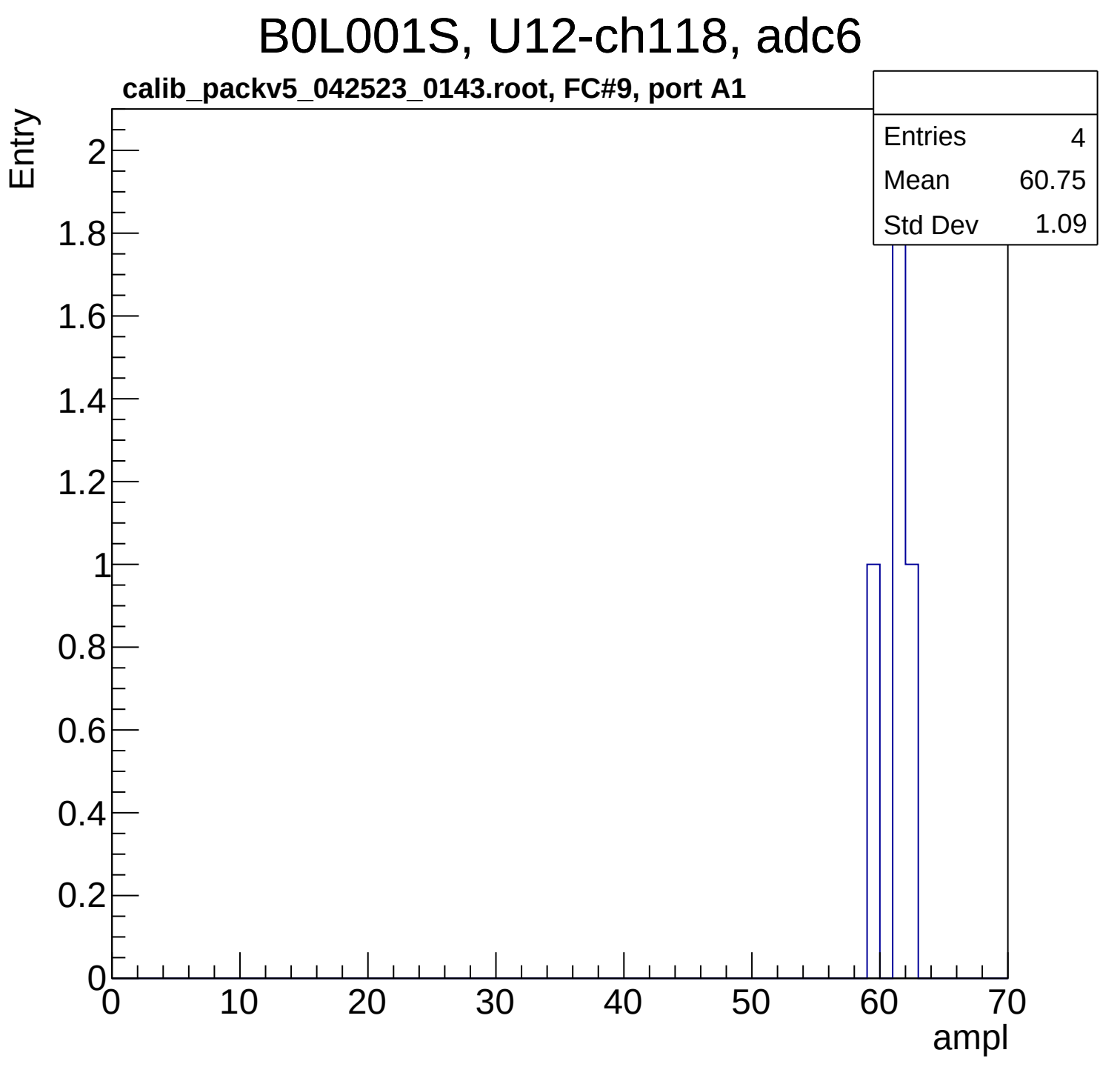
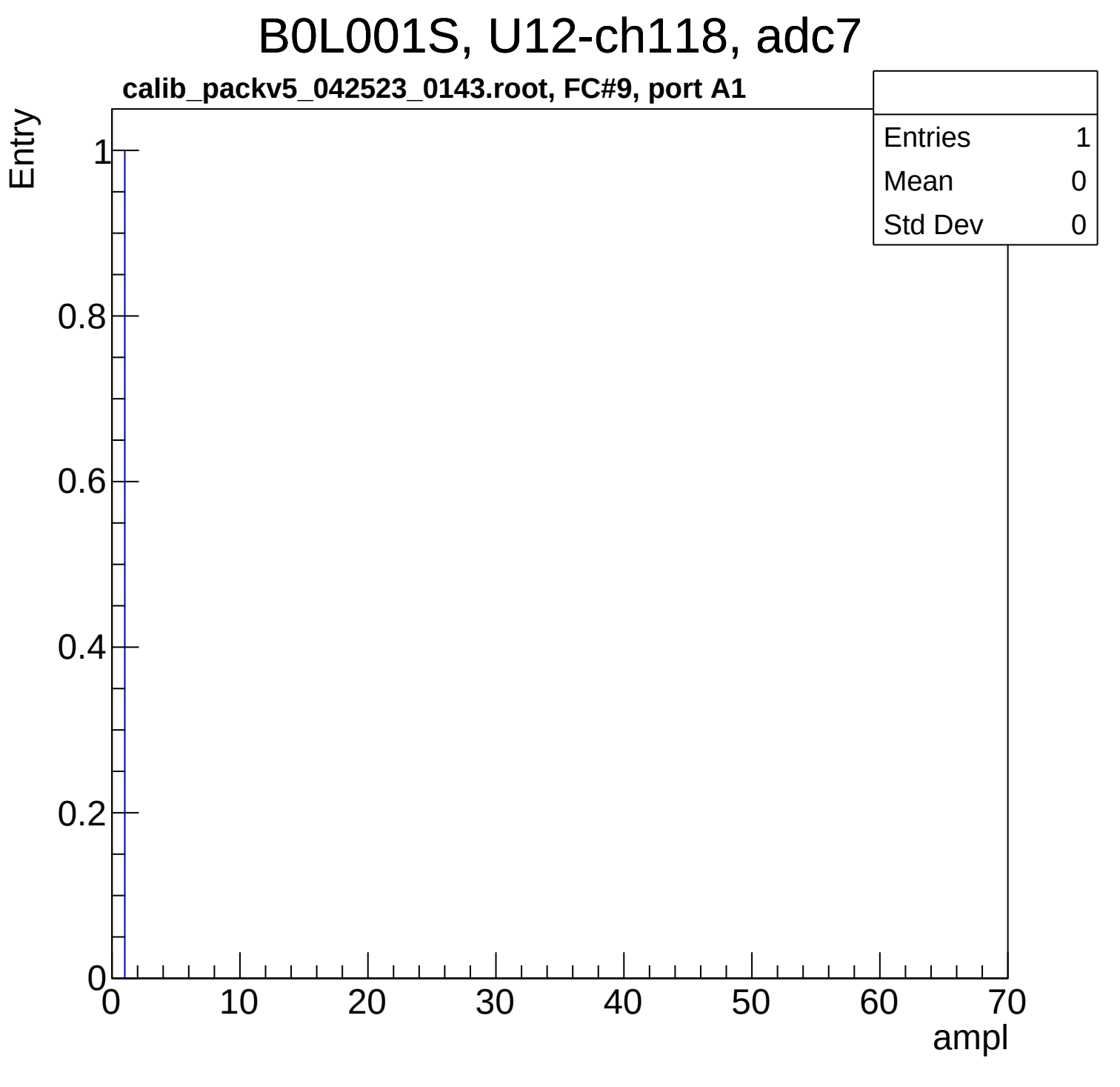
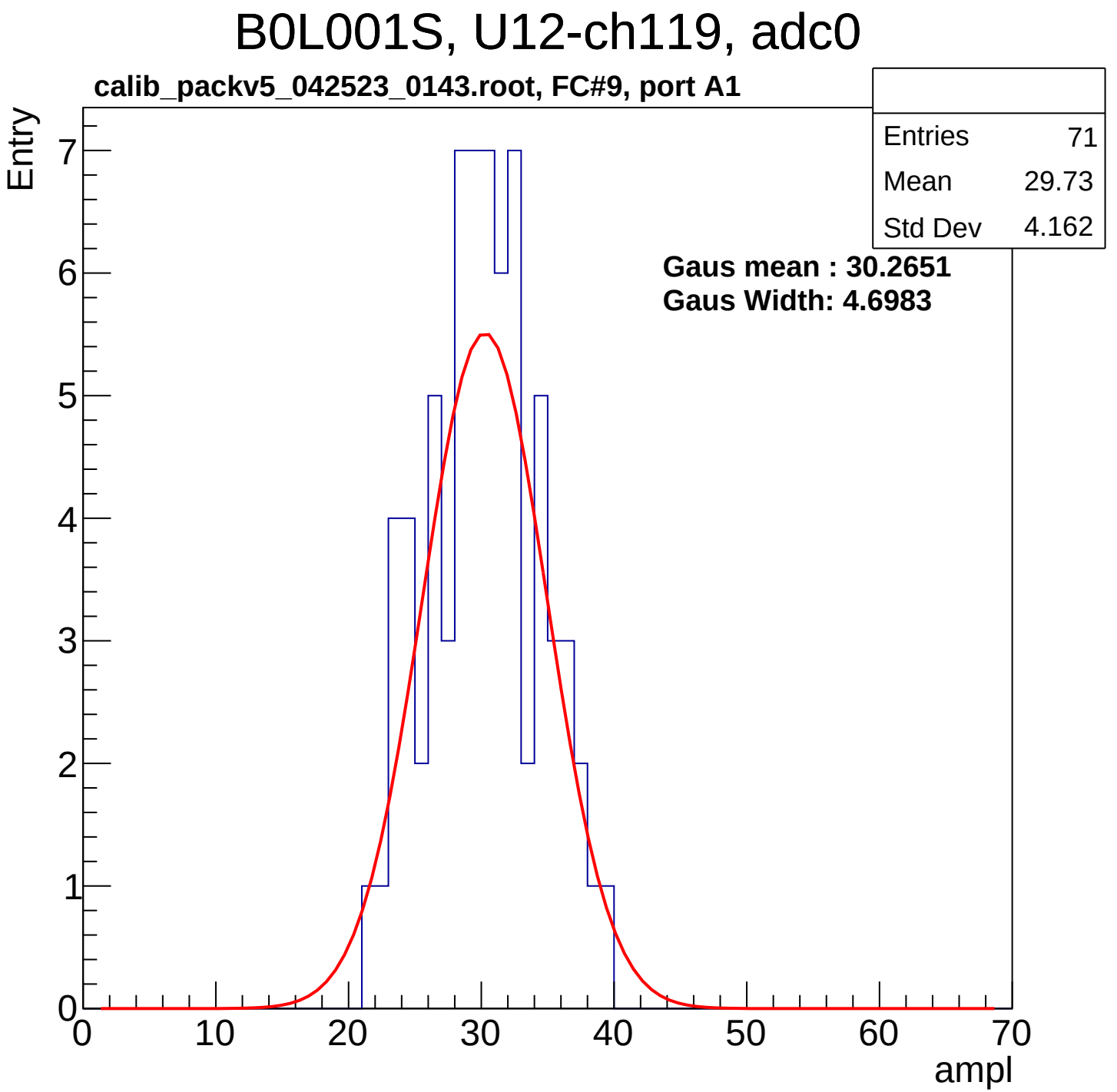
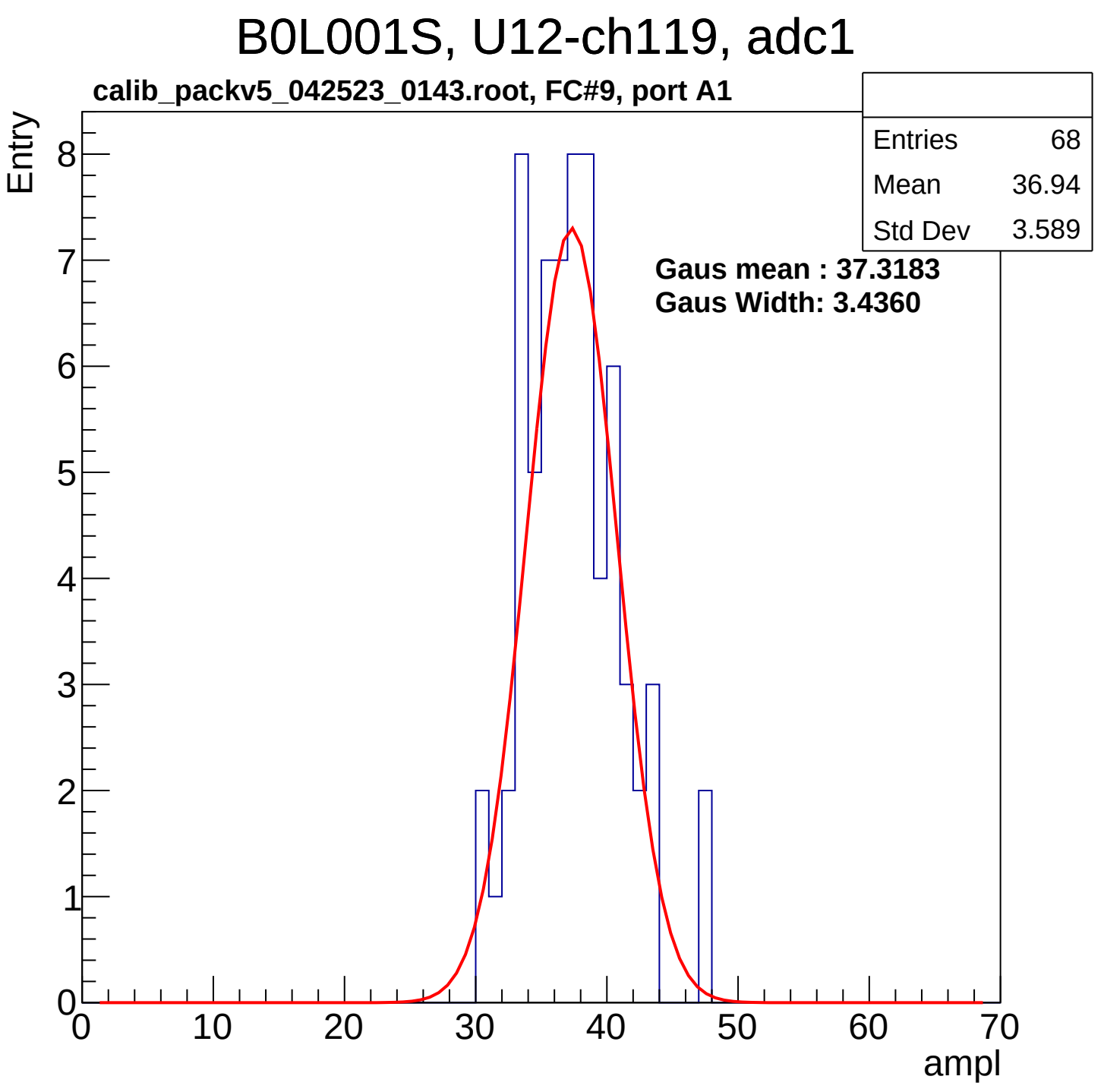
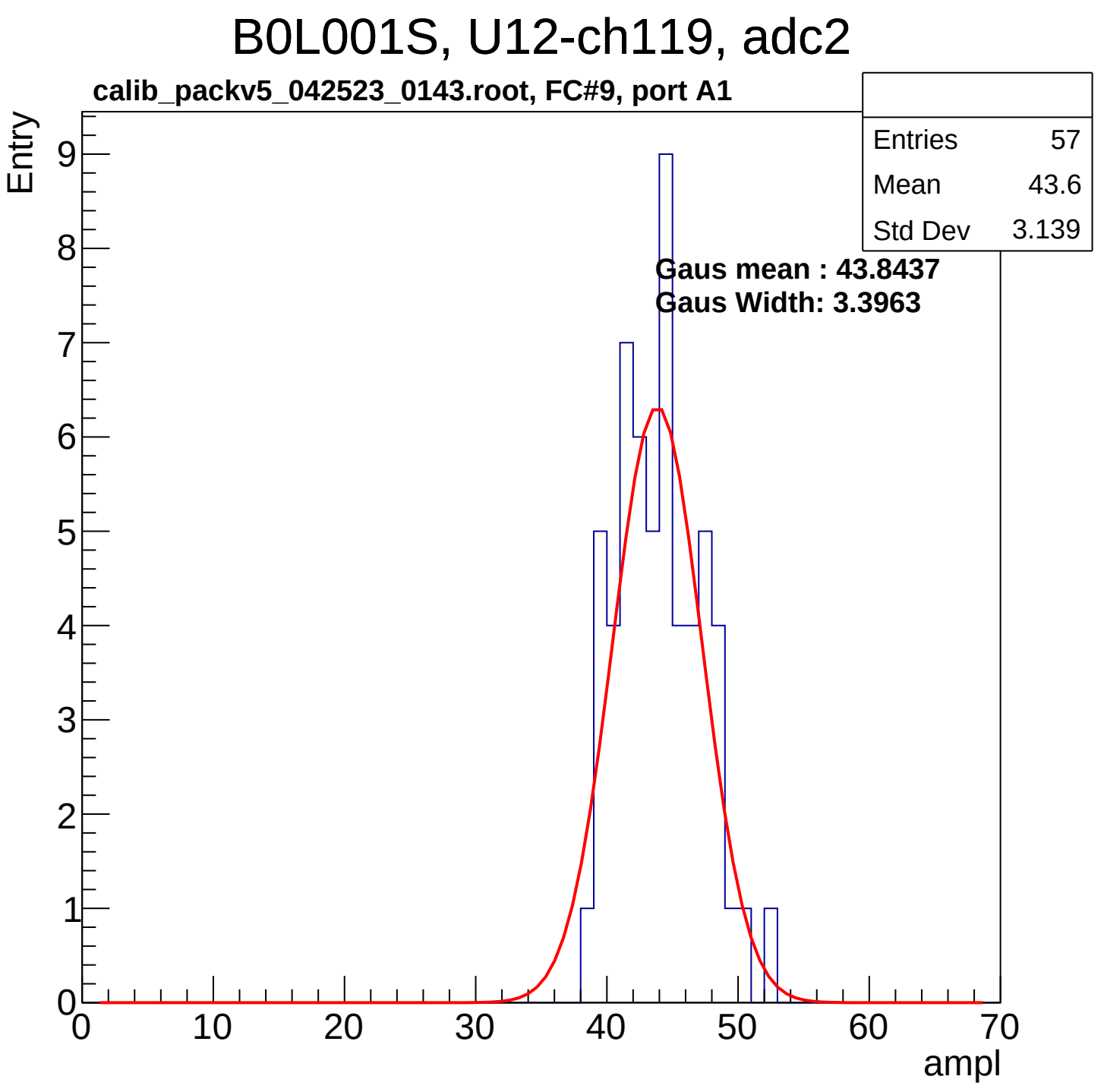
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

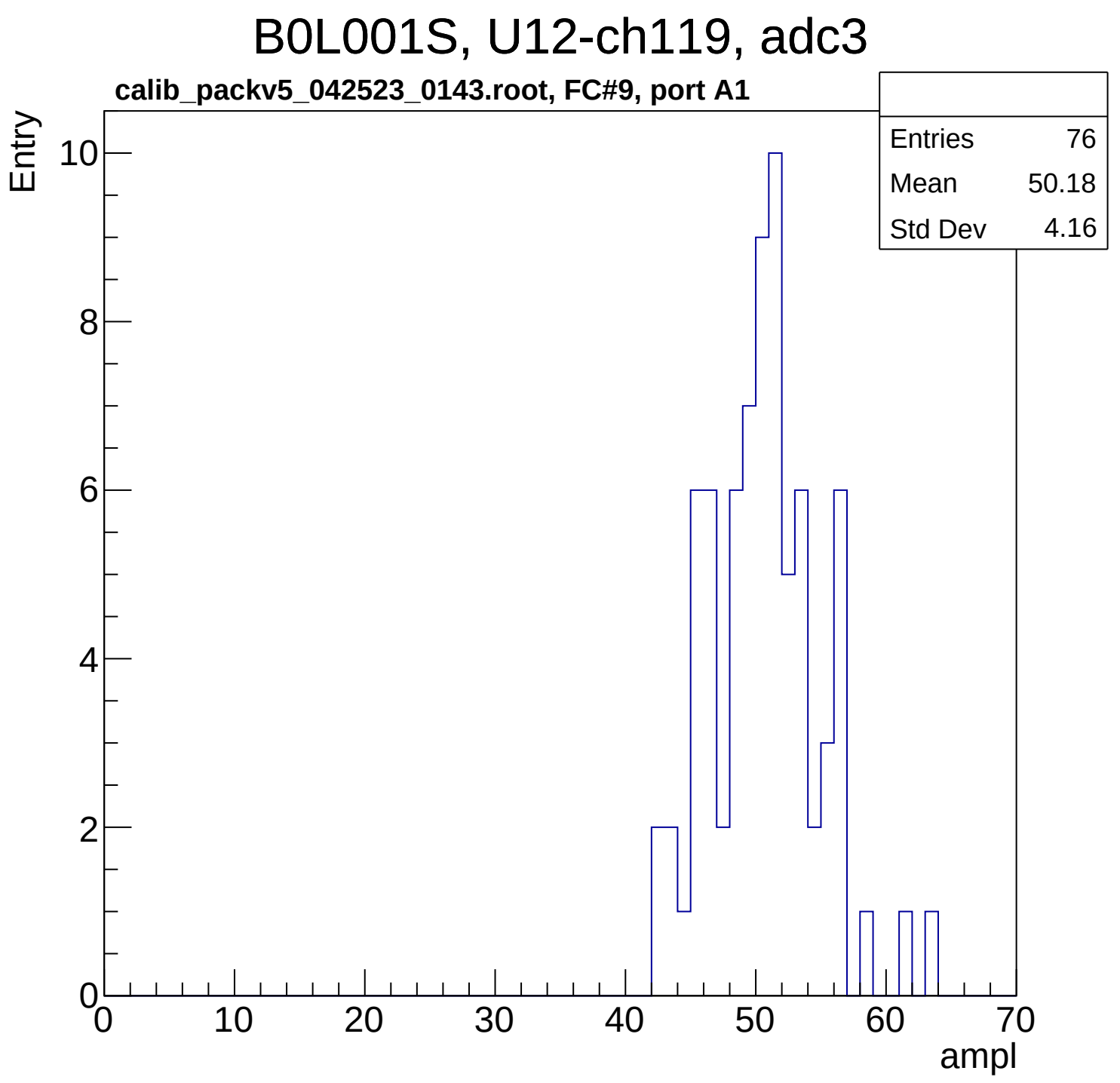

B0L001S, U12-ch118, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 4
Mean 60.75
Std Dev 1.09
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

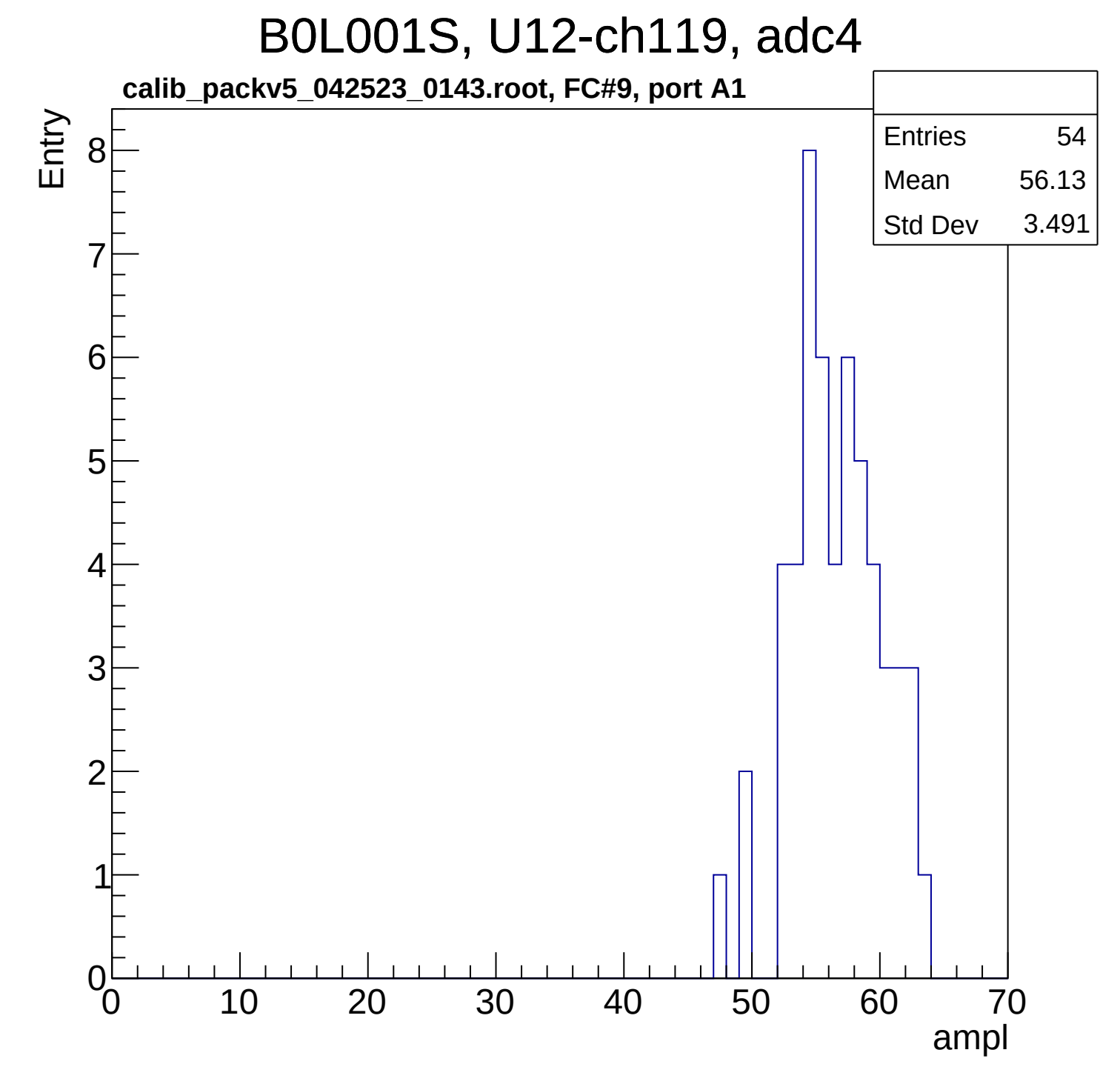

B0L001S, U12-ch118, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch119, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 71
Mean 29.73
Std Dev 4.162
Gaus mean : 30.2651
Gaus Width: 4.6983
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B0L001S, U12-ch119, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 68
Mean 36.94
Std Dev 3.589
Gaus mean : 37.3183
Gaus Width: 3.4360
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch119, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 57
Mean 43.6
Std Dev 3.139
Gaus mean : 43.8437
Gaus Width: 3.3963
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch119, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 76
Mean 50.18
Std Dev 4.16
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch119, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 54
Mean 56.13
Std Dev 3.491
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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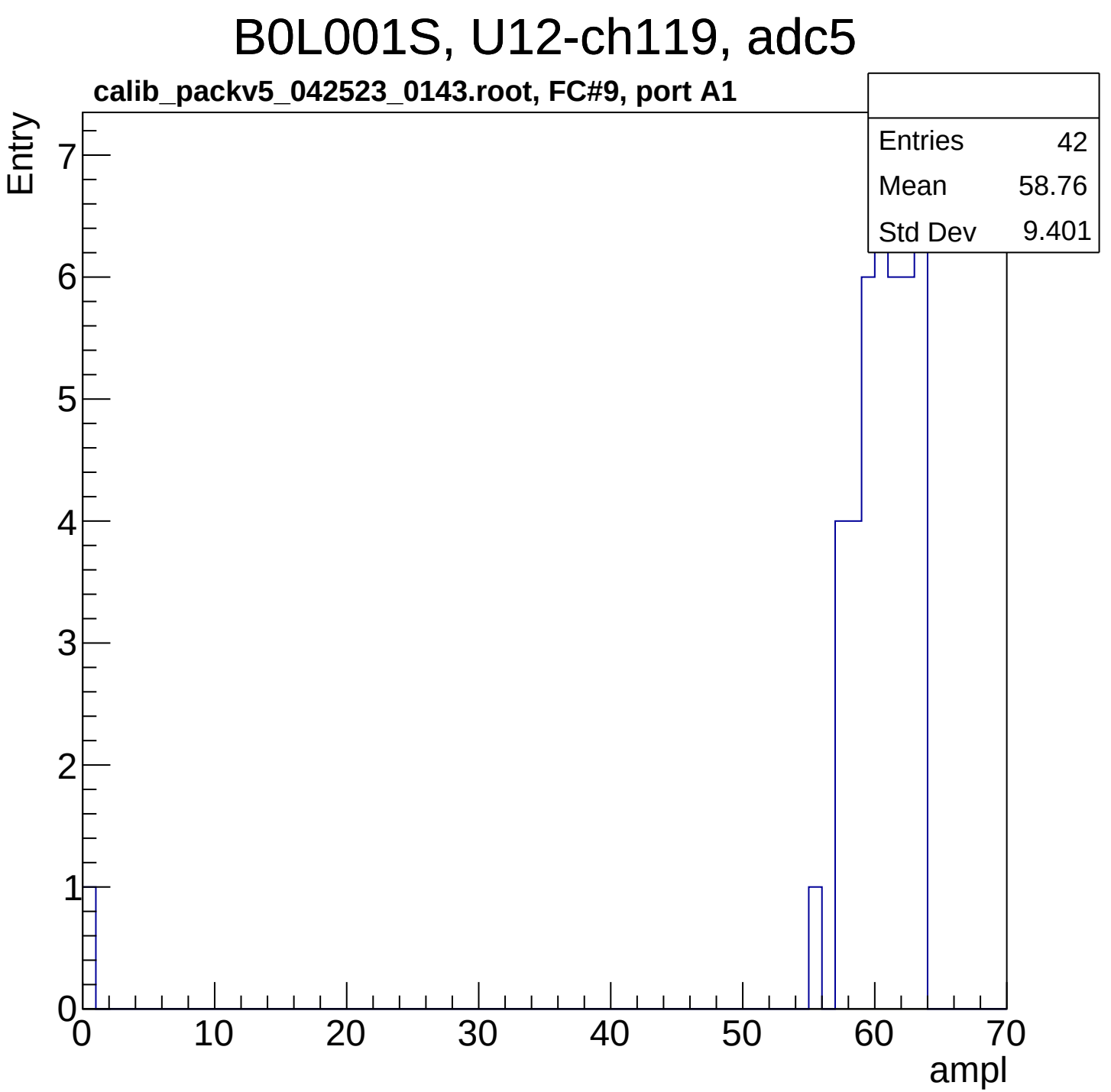
B0L001S, U12-ch119, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 42
Mean 58.76
Std Dev 9.401
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
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60
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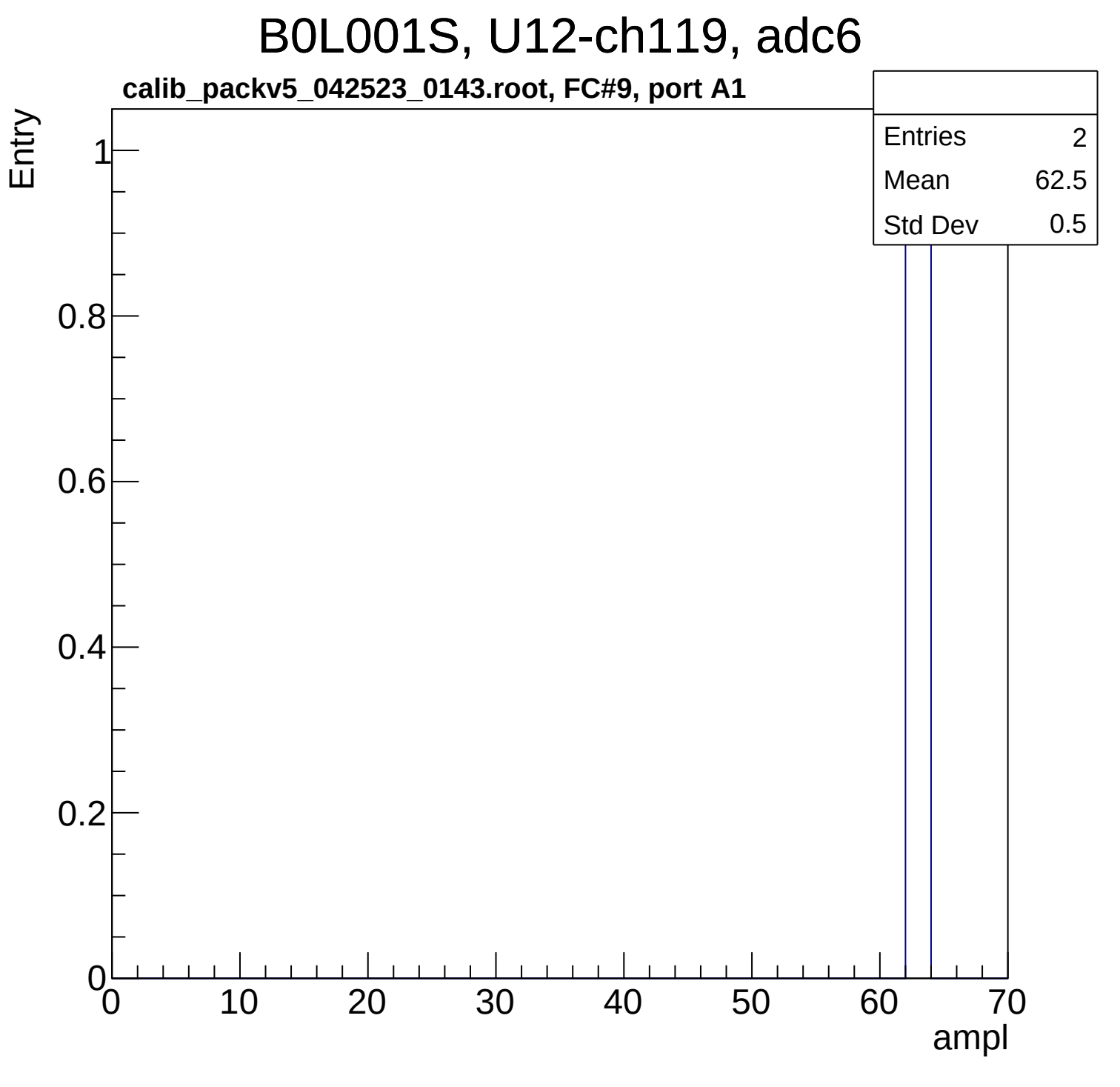
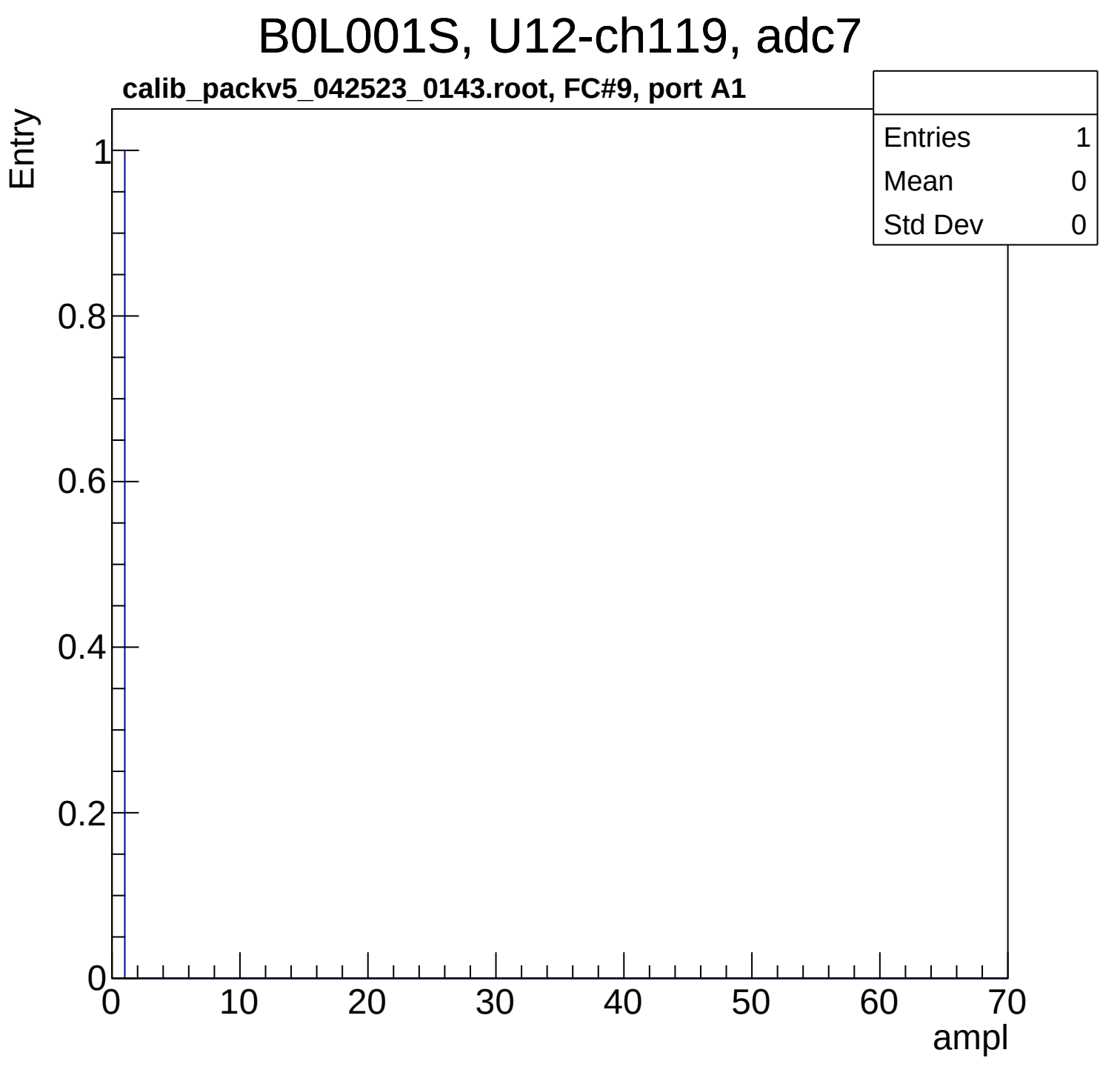
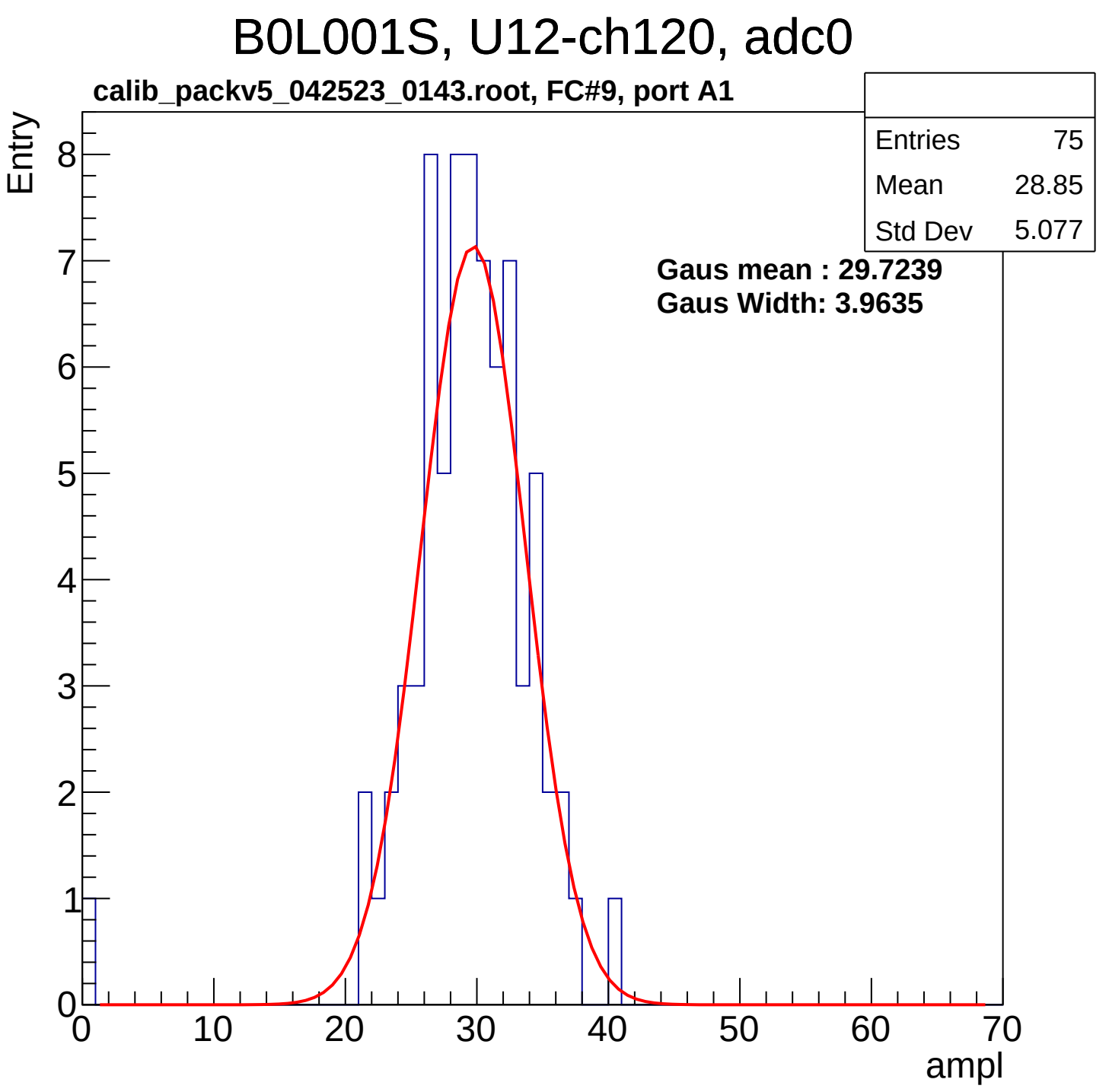
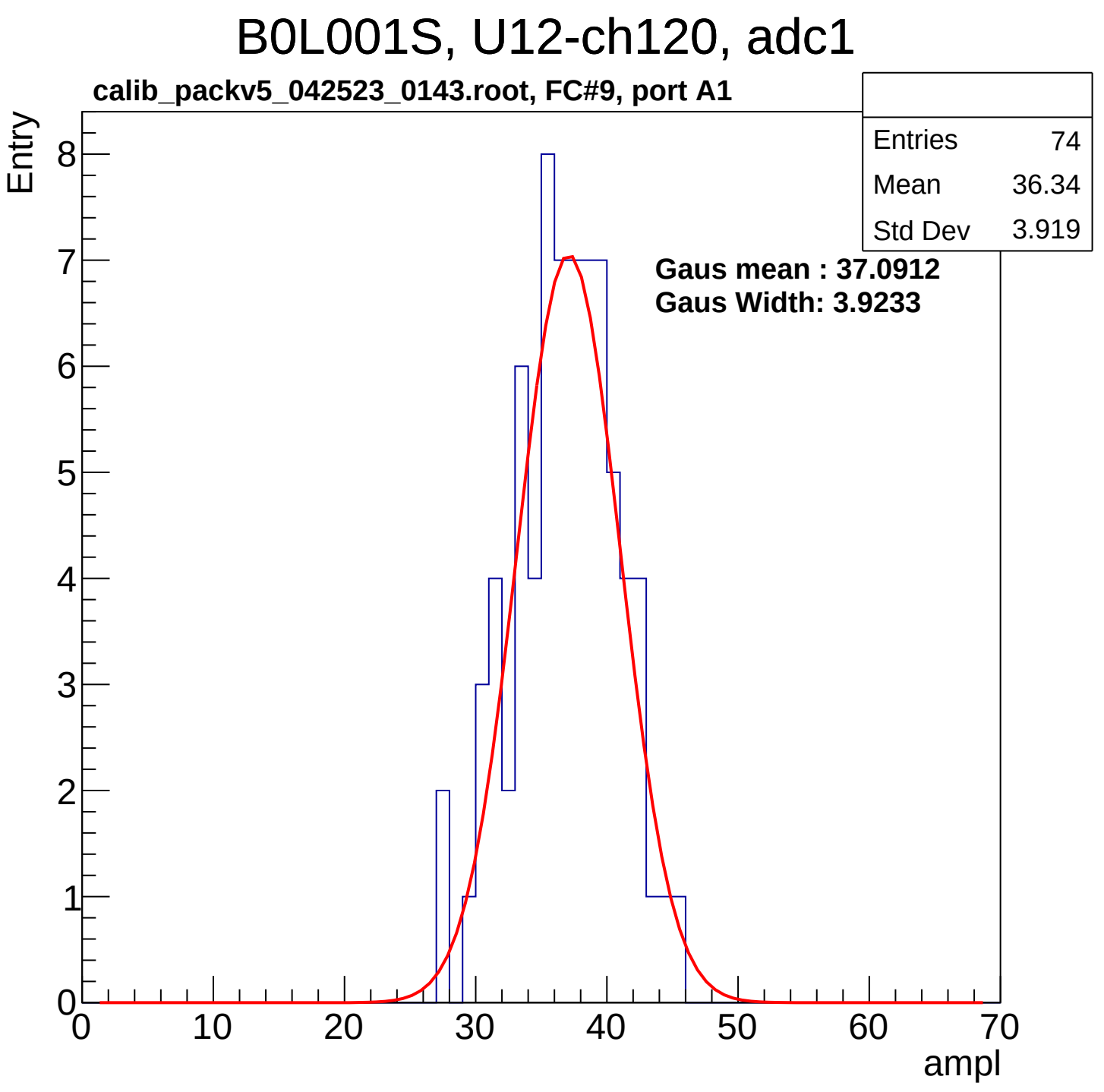

B0L001S, U12-ch119, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch119, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch120, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 75
Mean 28.85
Std Dev 5.077
Gaus mean : 29.7239
Gaus Width: 3.9635
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch120, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 74
Mean 36.34
Std Dev 3.919
Gaus mean : 37.0912
Gaus Width: 3.9233
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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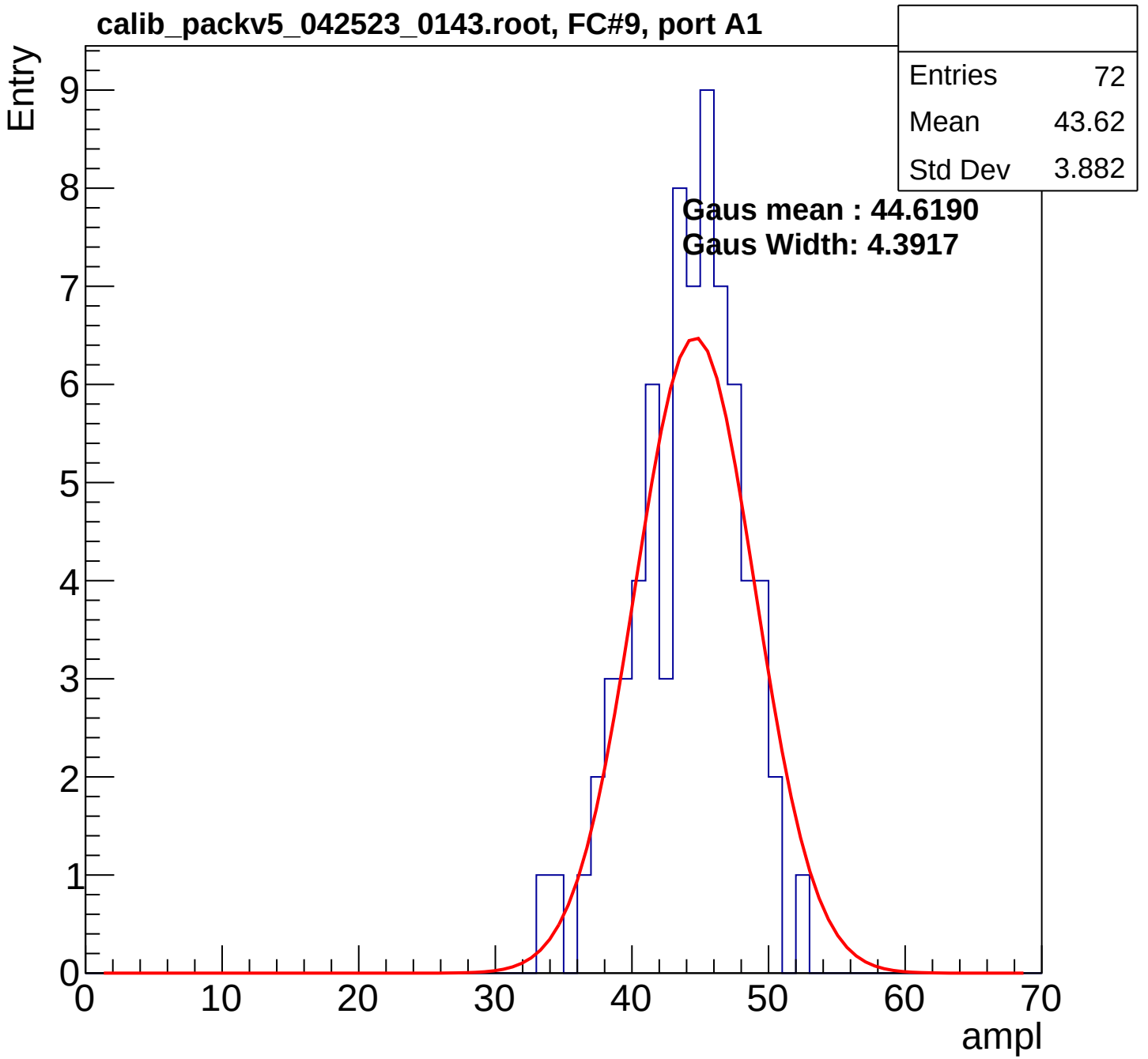
B0L001S, U12-ch120, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 72
Mean 43.62
Std Dev 3.882
Gaus mean : 44.6190
Gaus Width: 4.3917
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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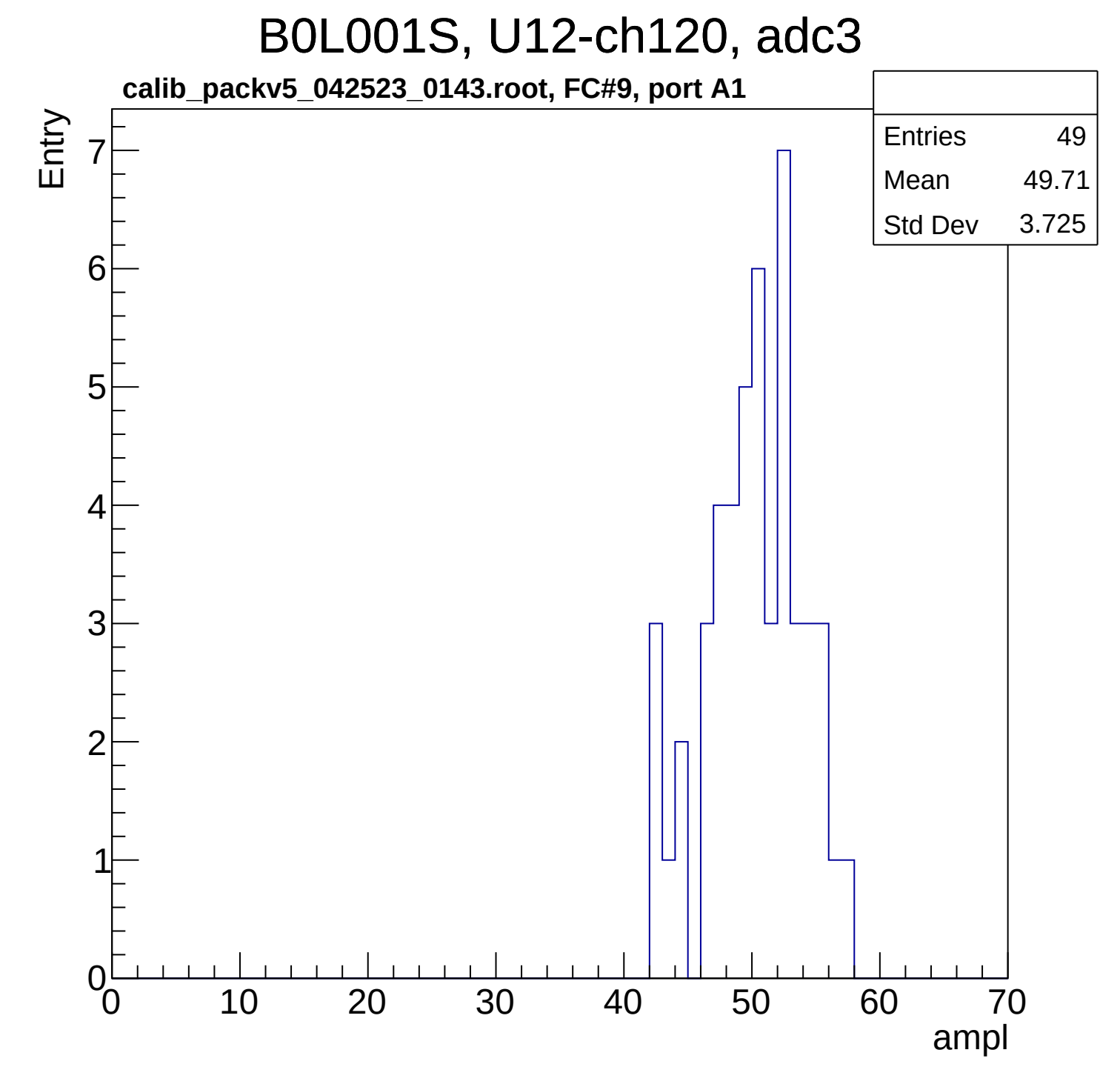
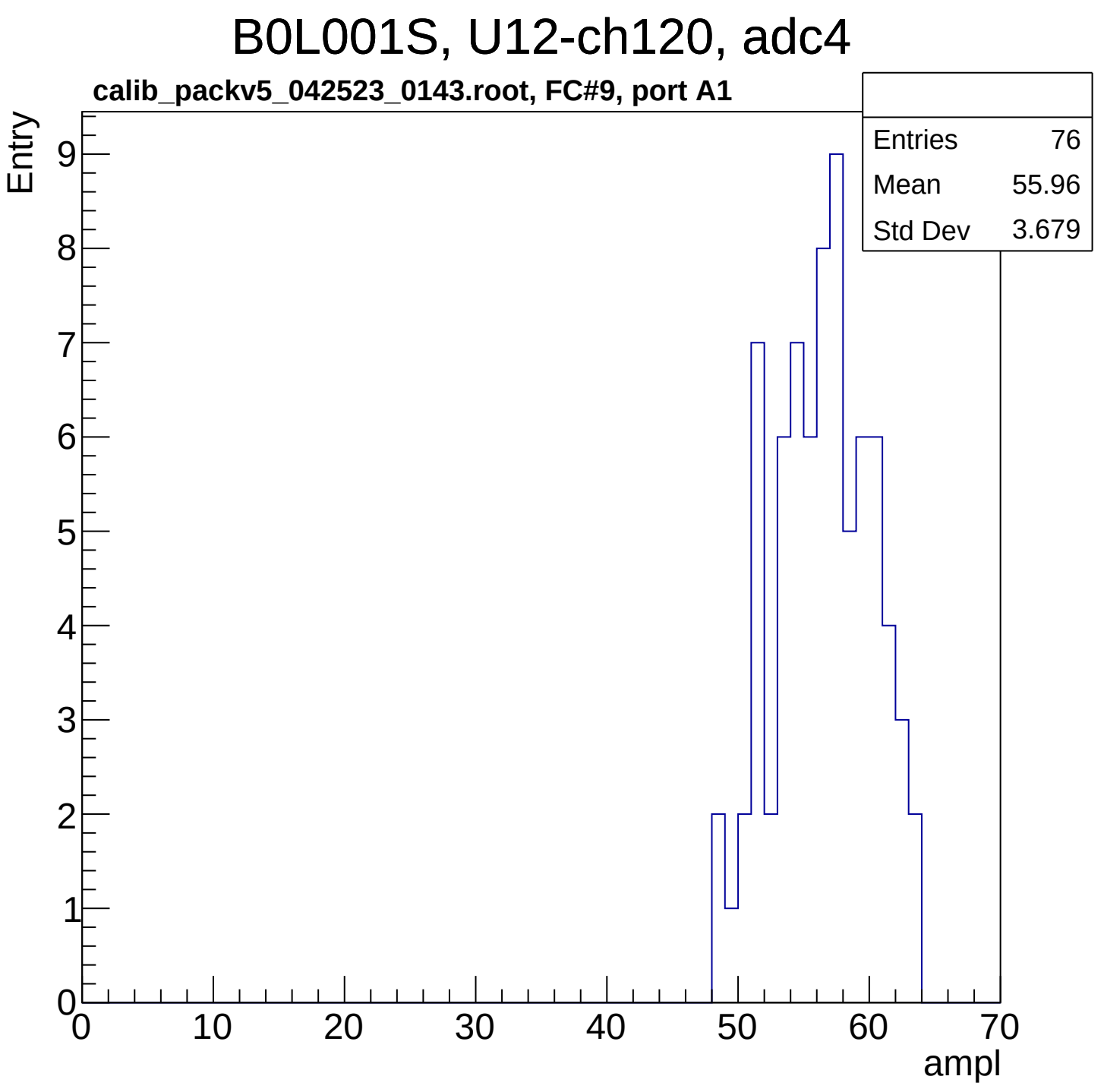
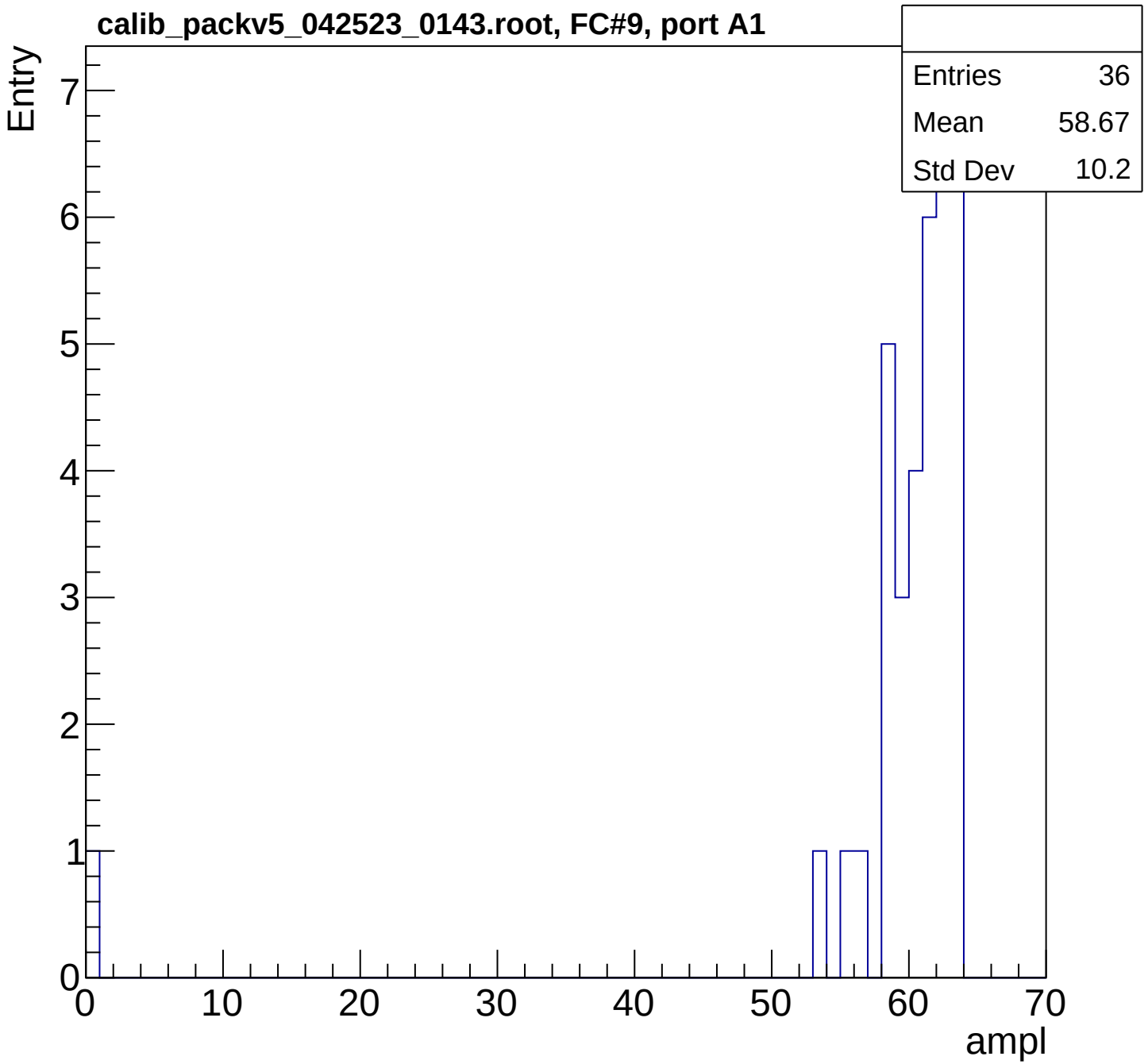
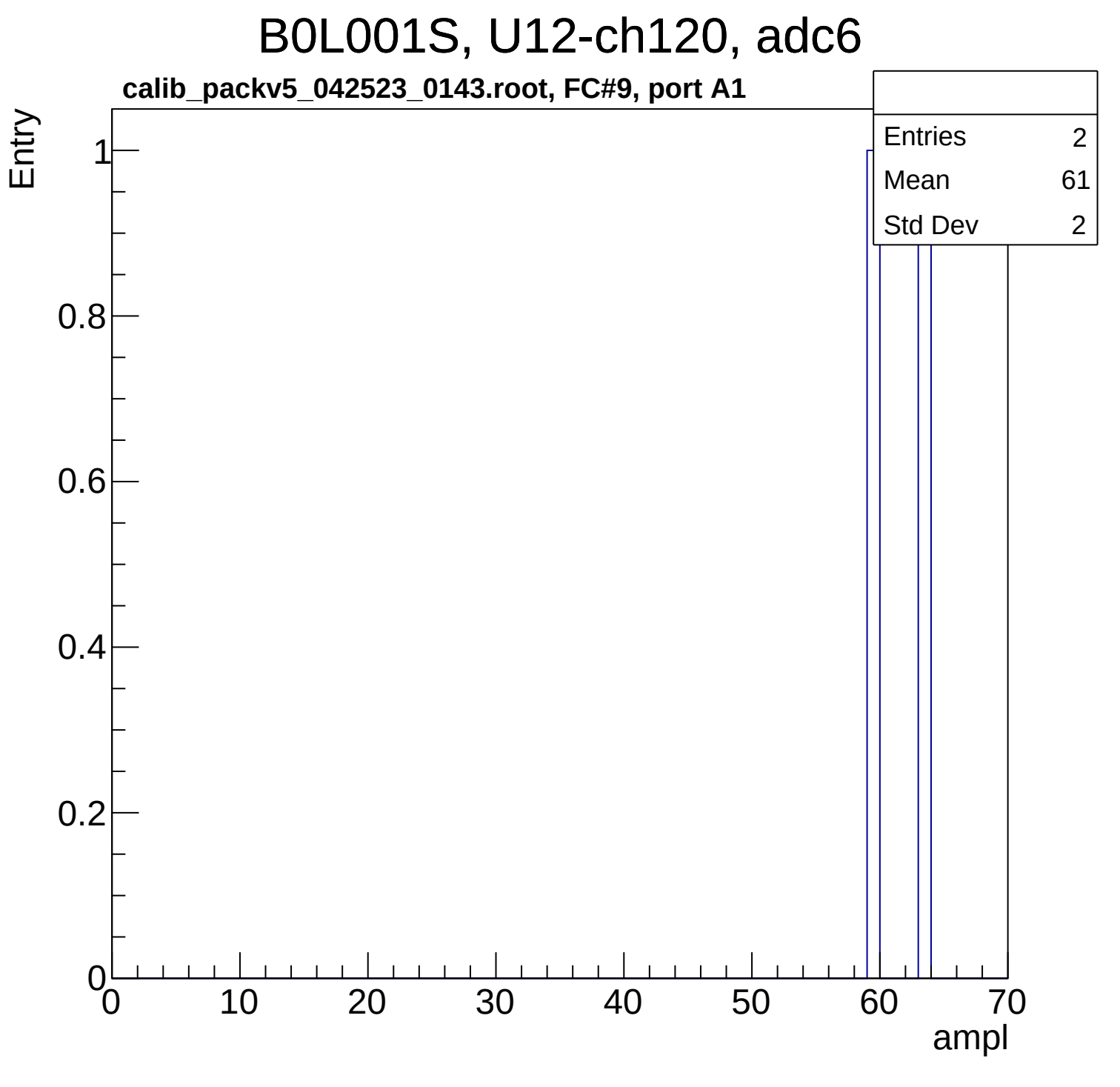
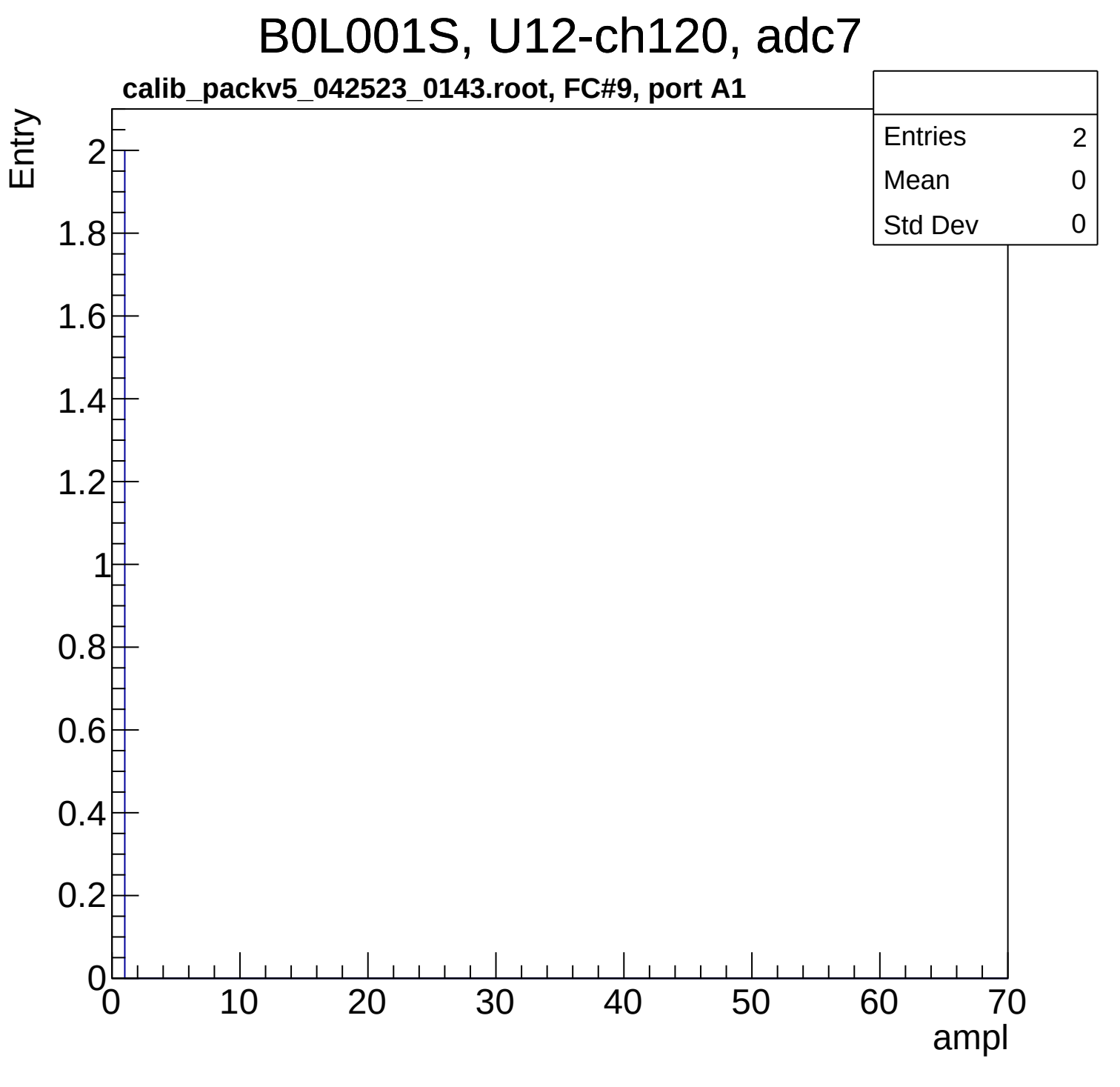
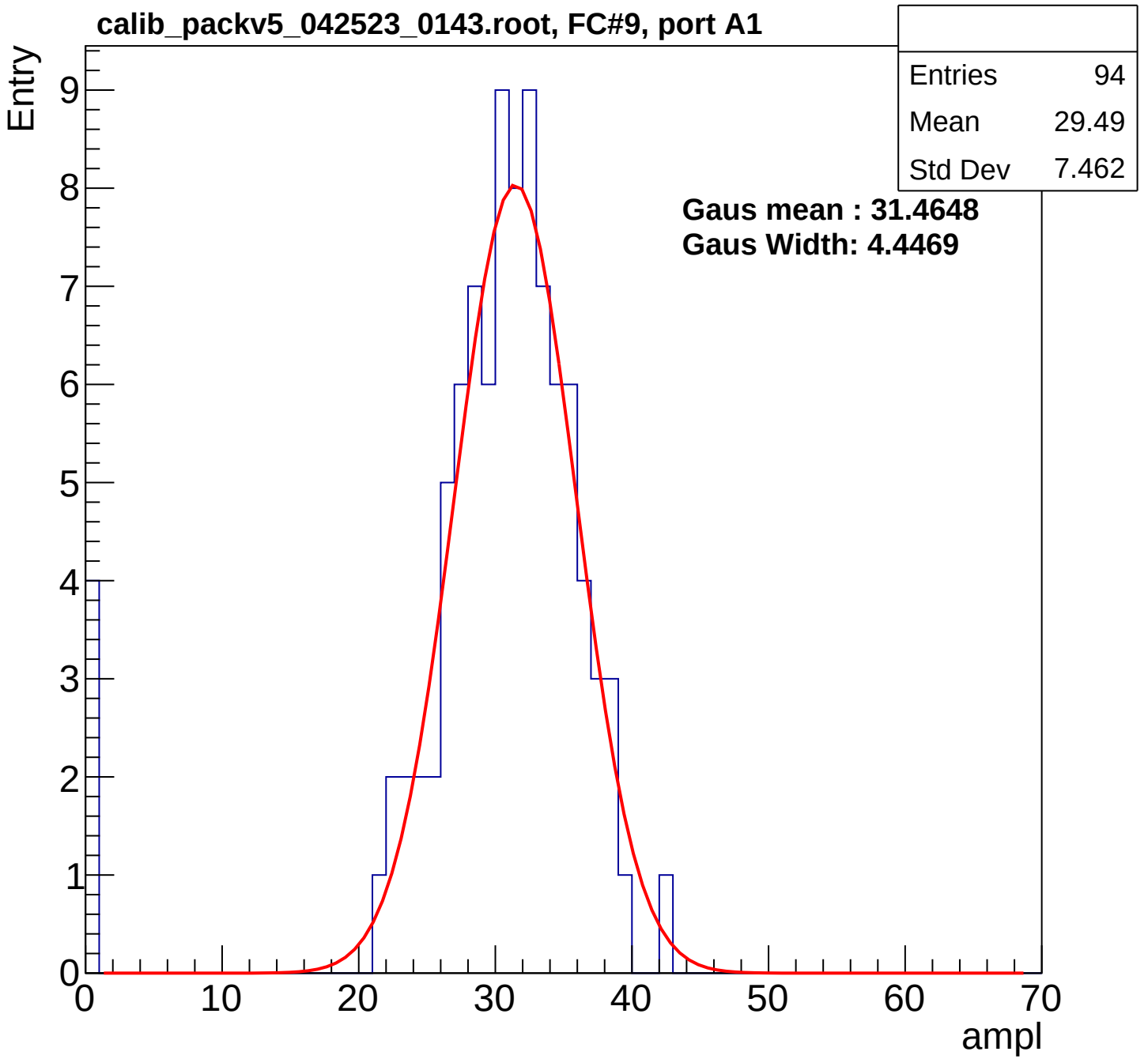

B0L001S, U12-ch120, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 49
Mean 49.71
Std Dev 3.725
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

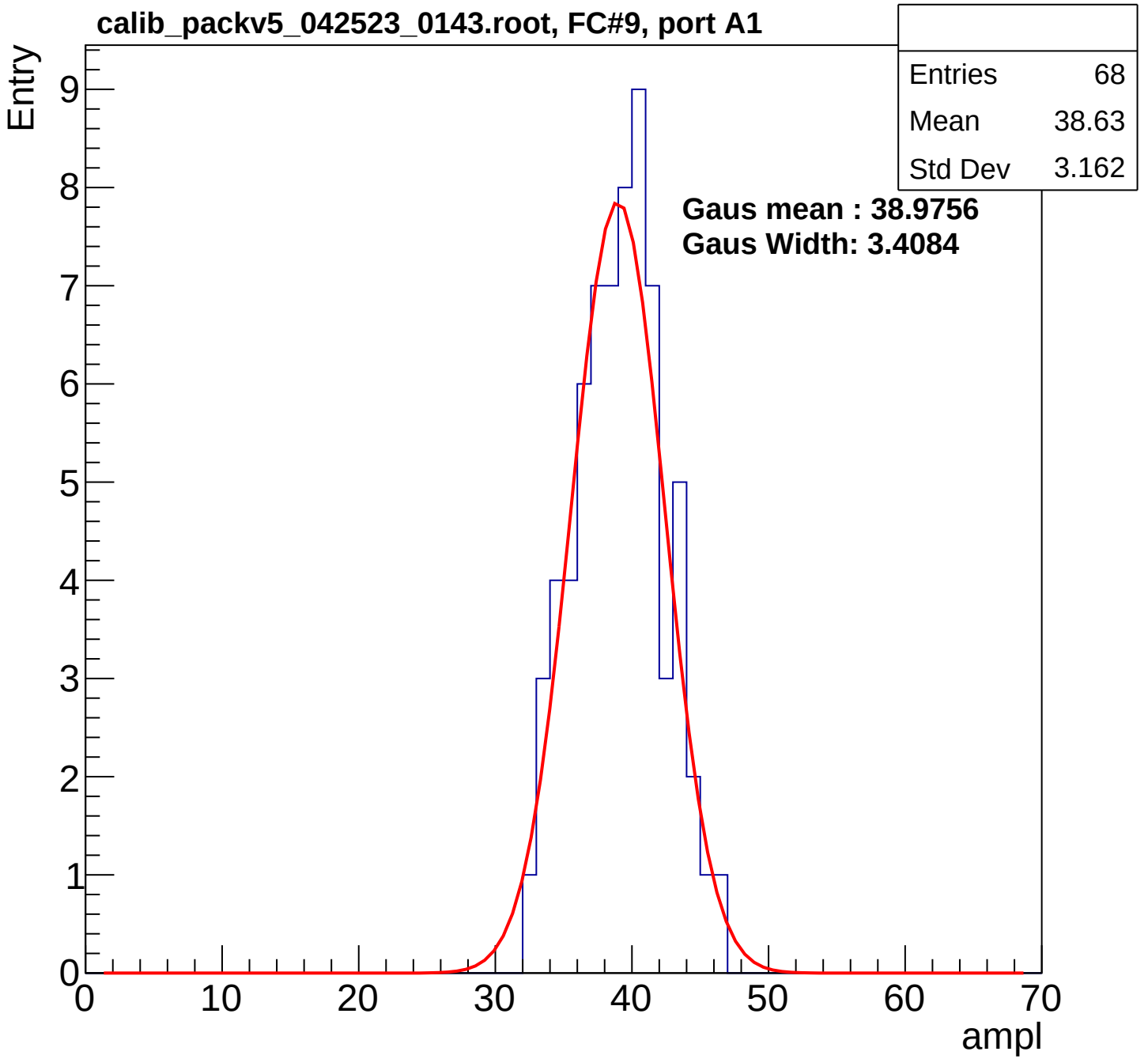

B0L001S, U12-ch120, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 76
Mean 55.96
Std Dev 3.679
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

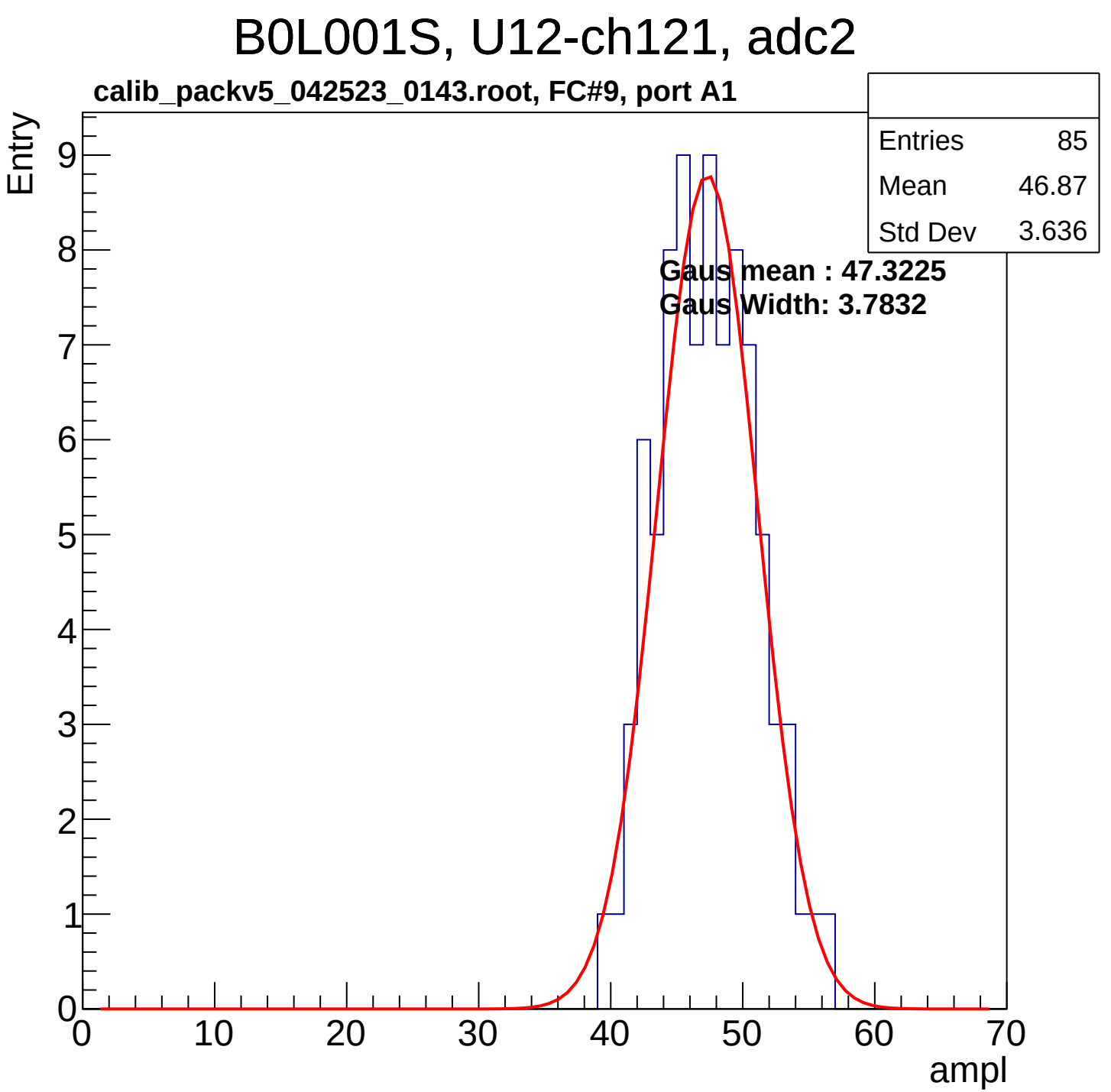

B0L001S, U12-ch120, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 36
Mean 58.67
Std Dev 10.2
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

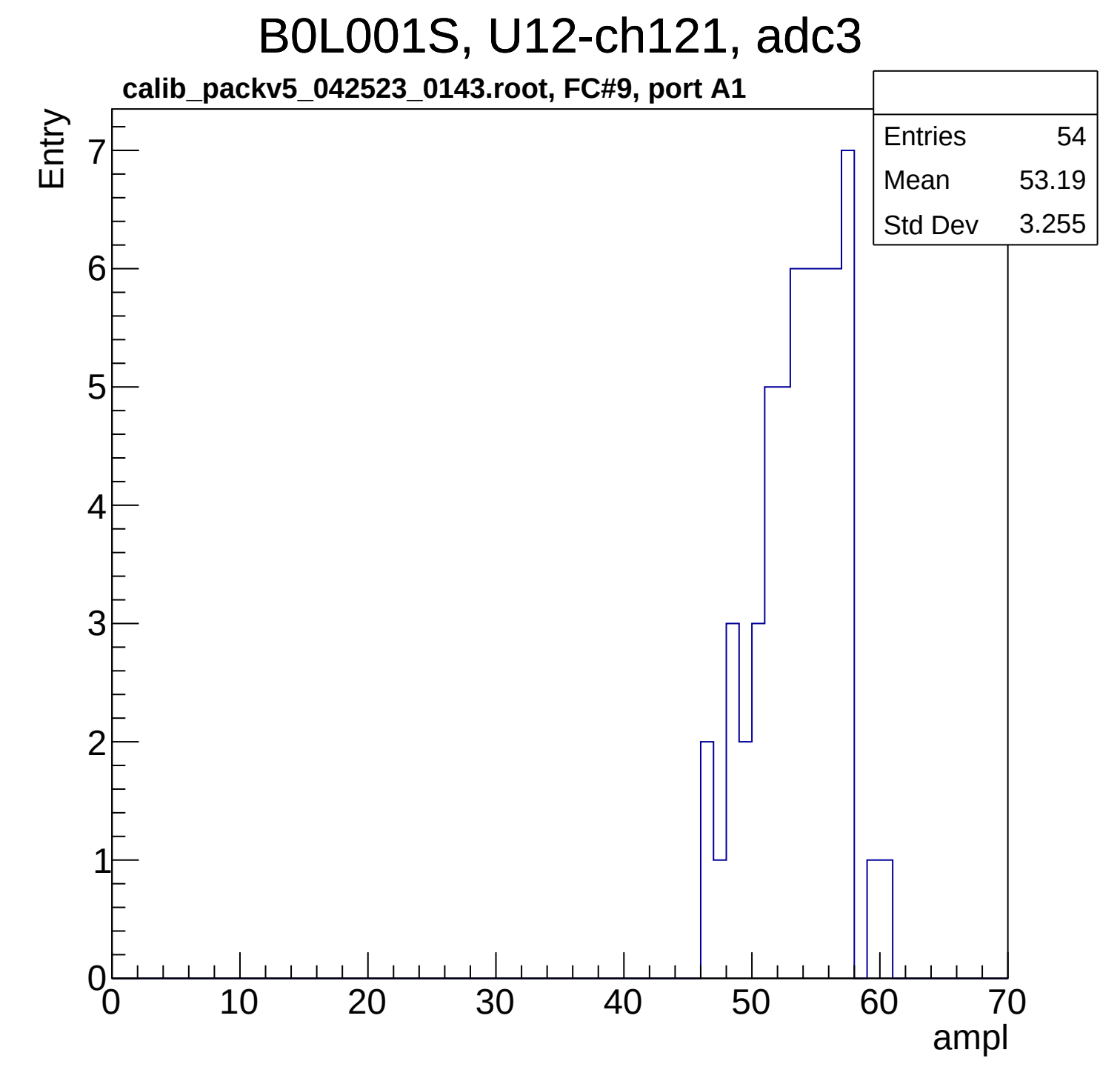

B0L001S, U12-ch120, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 61
Std Dev 2
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

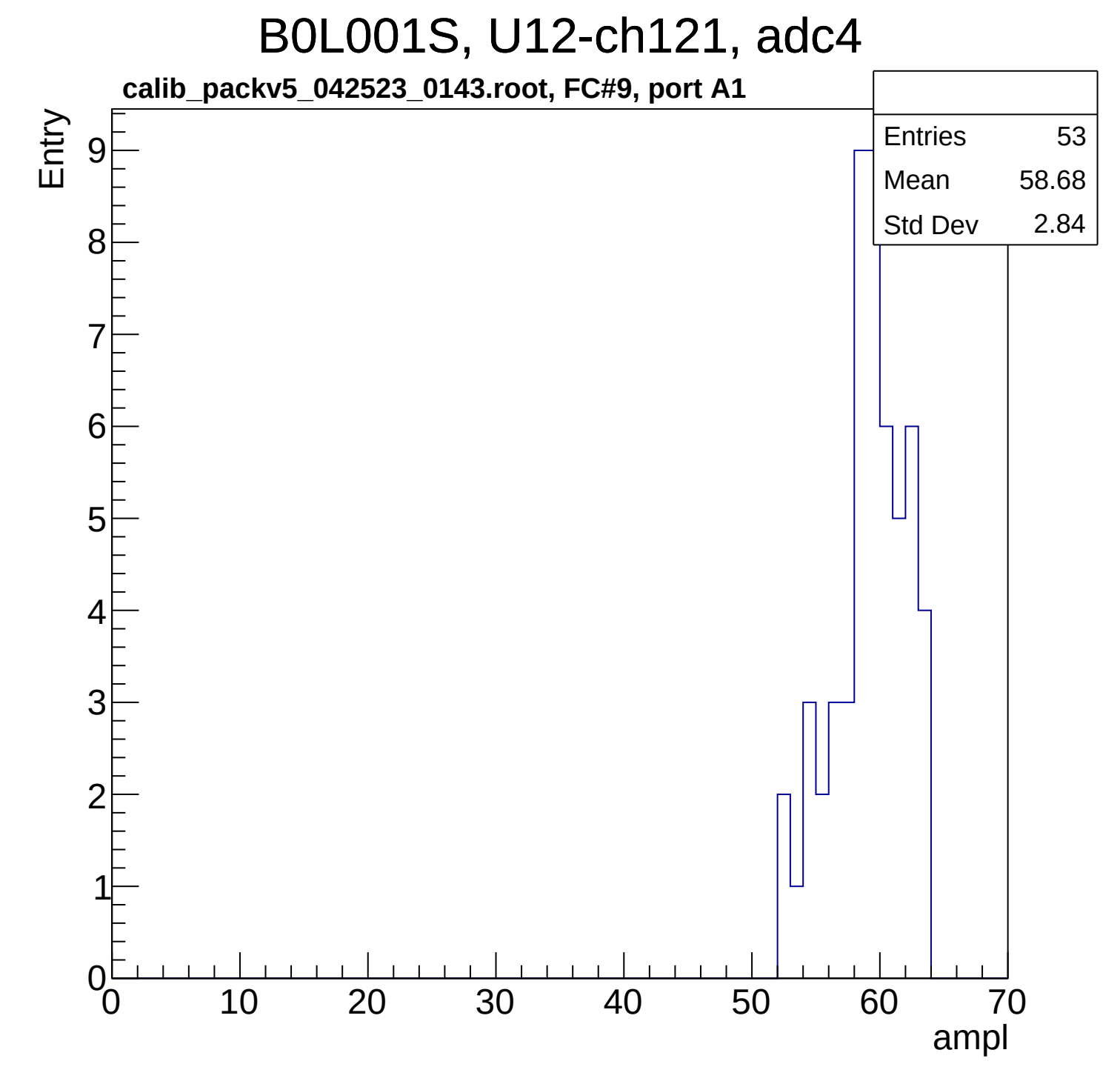

B0L001S, U12-ch120, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

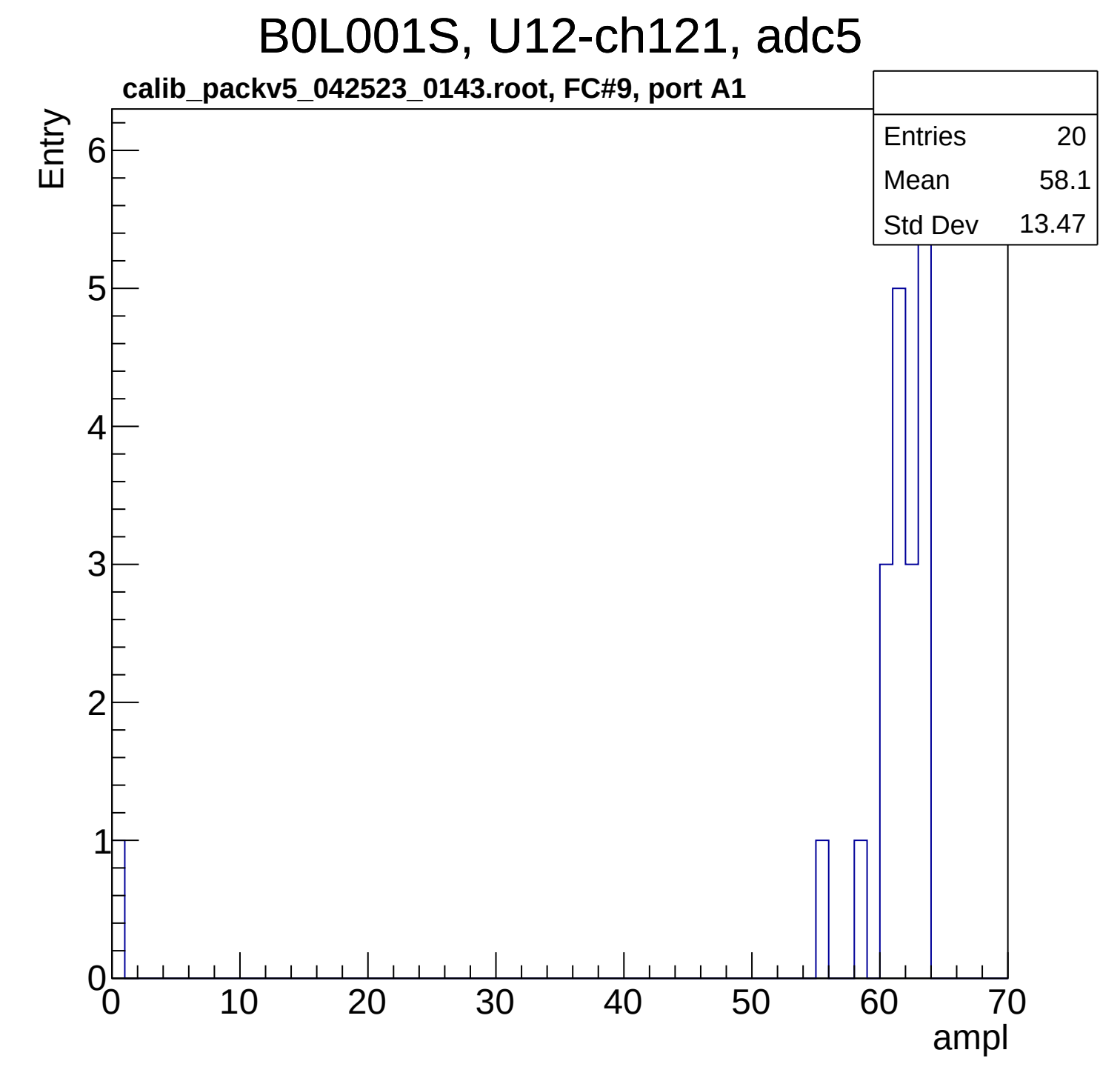

B0L001S, U12-ch121, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 94
Mean 29.49
Std Dev 7.462
Gaus mean : 31.4648
Gaus Width: 4.4469
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

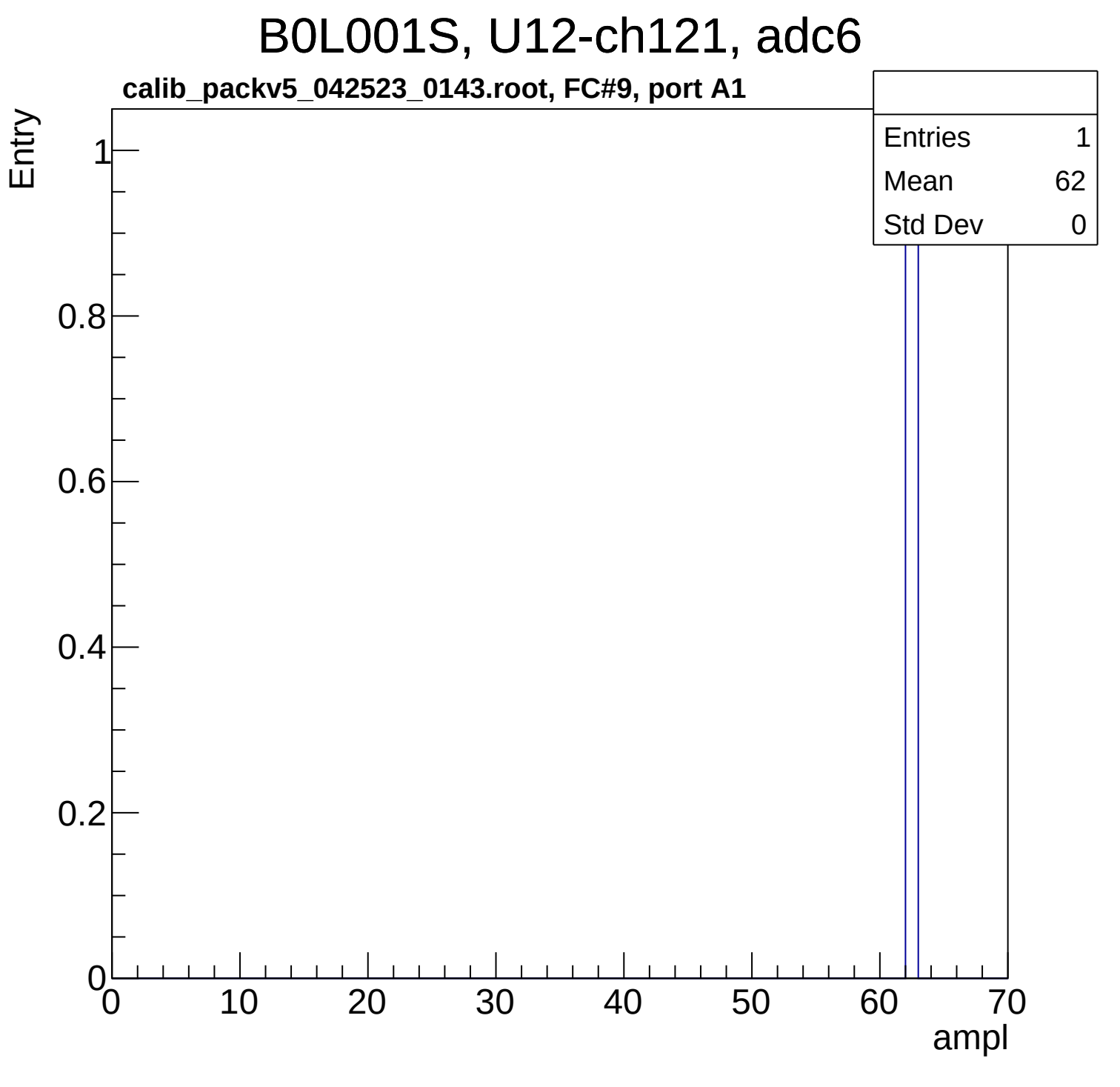

B0L001S, U12-ch121, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 68
Mean 38.63
Std Dev 3.162
Gaus mean : 38.9756
Gaus Width: 3.4084
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

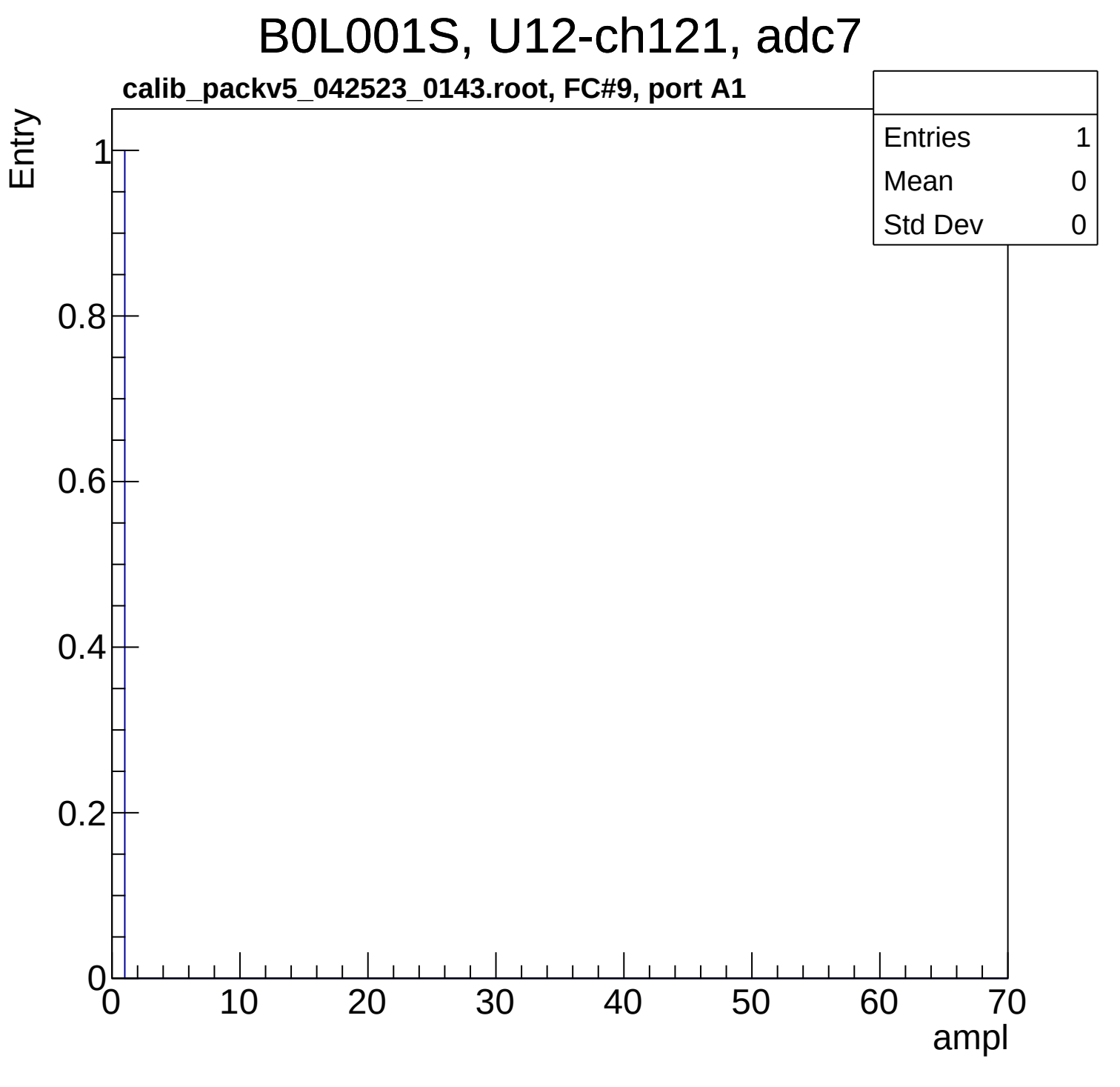

B0L001S, U12-ch121, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 85
Mean 46.87
Std Dev 3.636
Gaus mean : 47.3225
Gaus Width: 3.7832
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

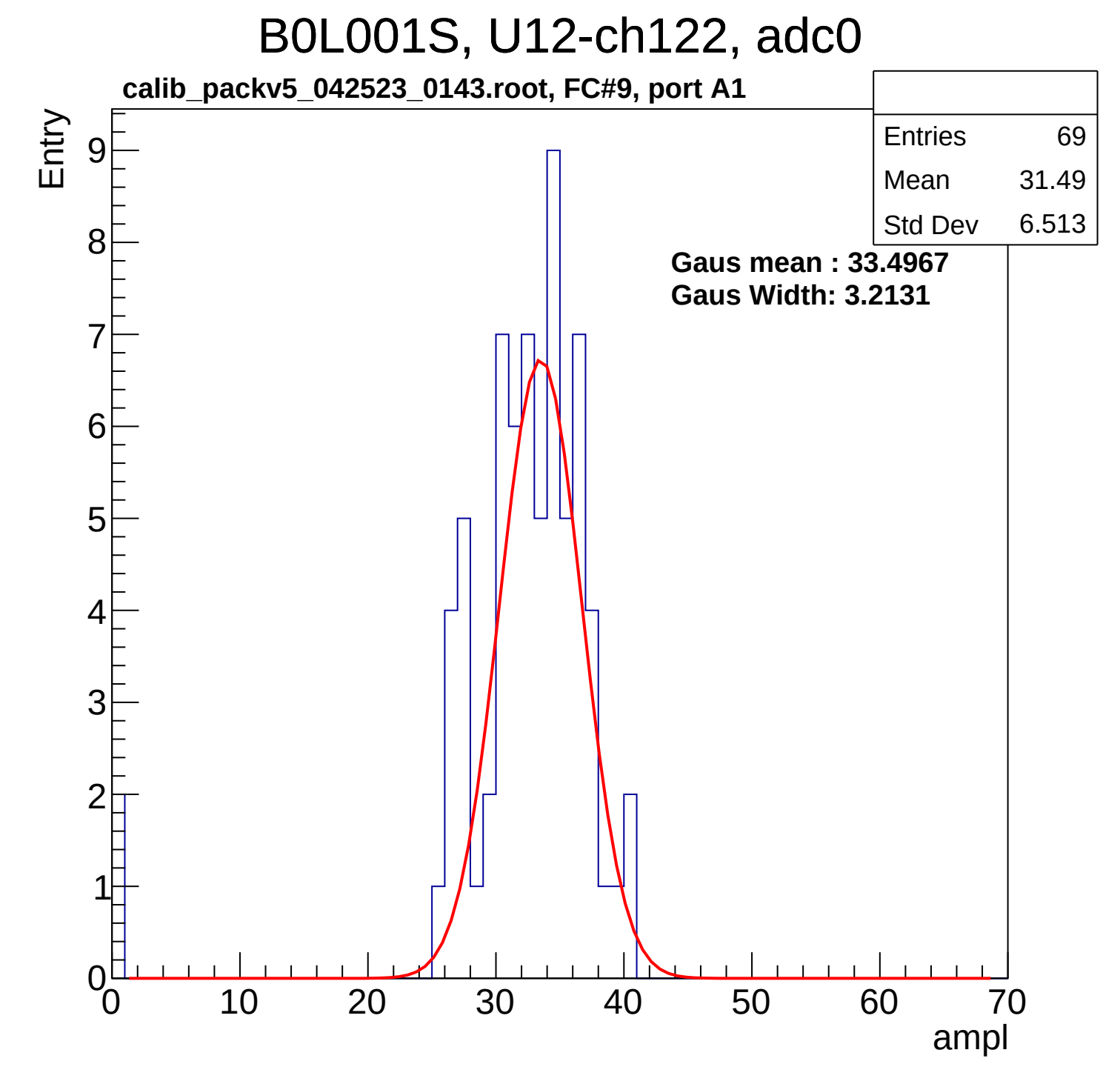

B0L001S, U12-ch121, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 54
Mean 53.19
Std Dev 3.255
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

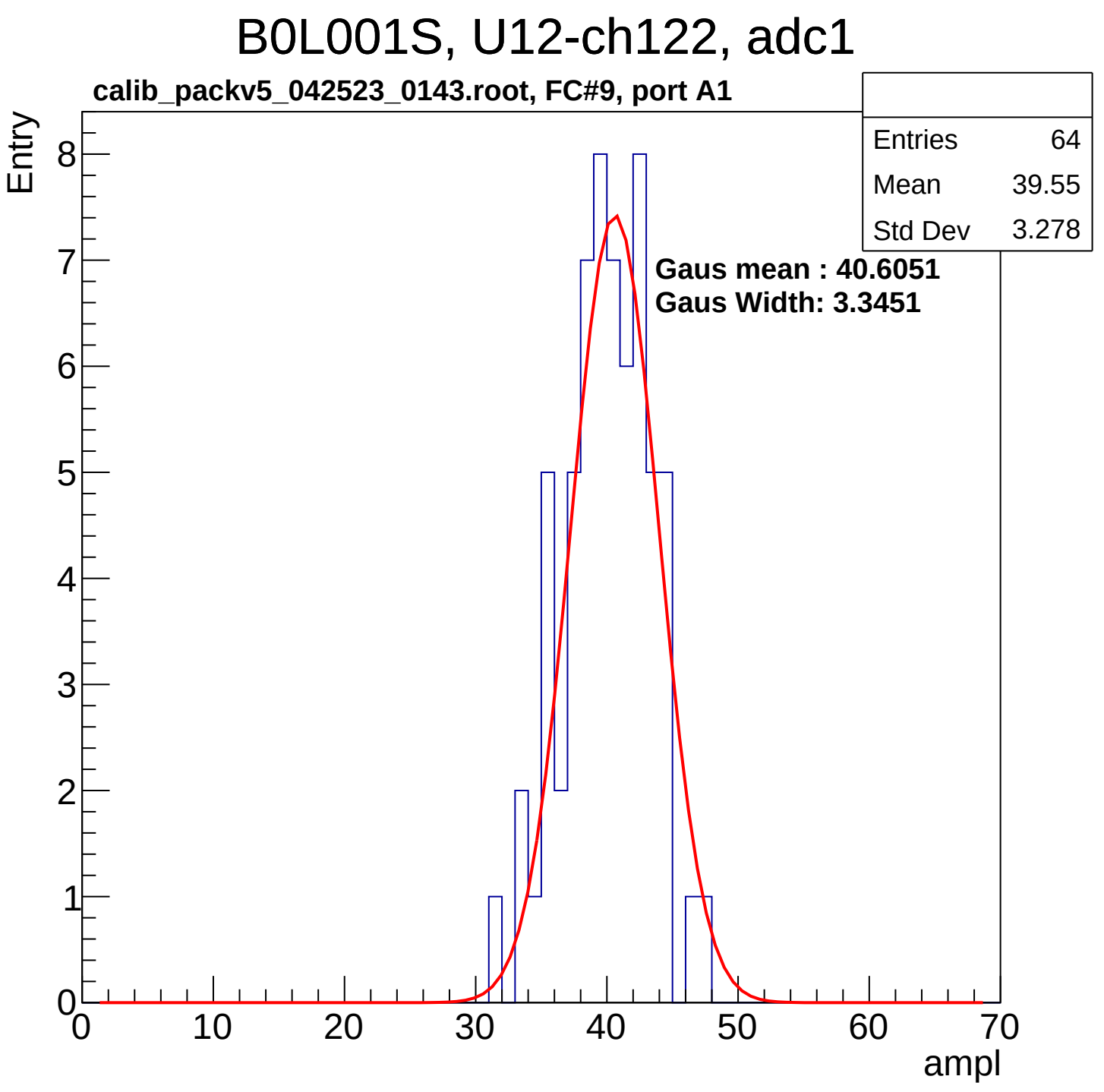

B0L001S, U12-ch121, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 53
Mean 58.68
Std Dev 2.84
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

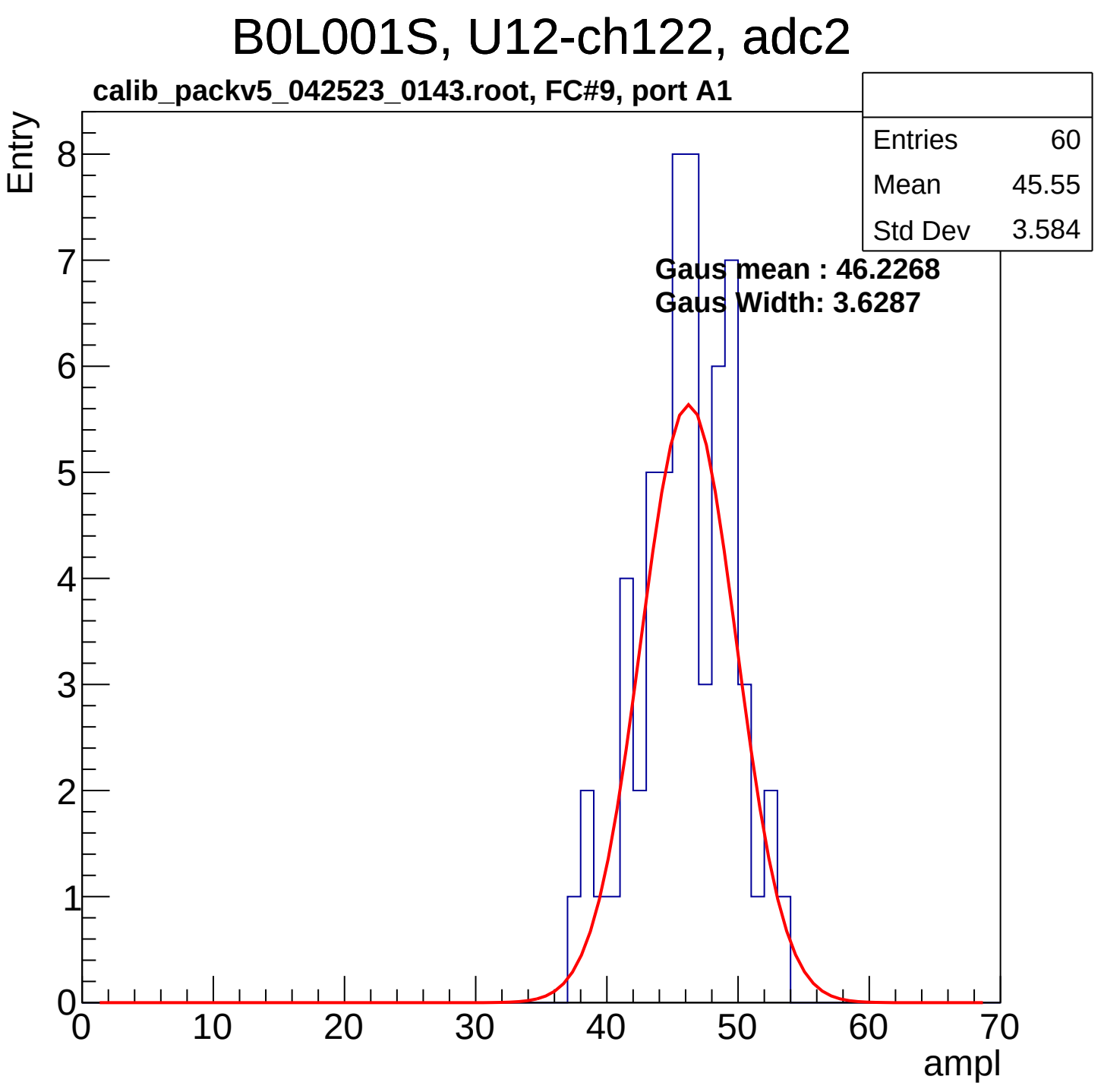

B0L001S, U12-ch121, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 20
Mean 58.1
Std Dev 13.47
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

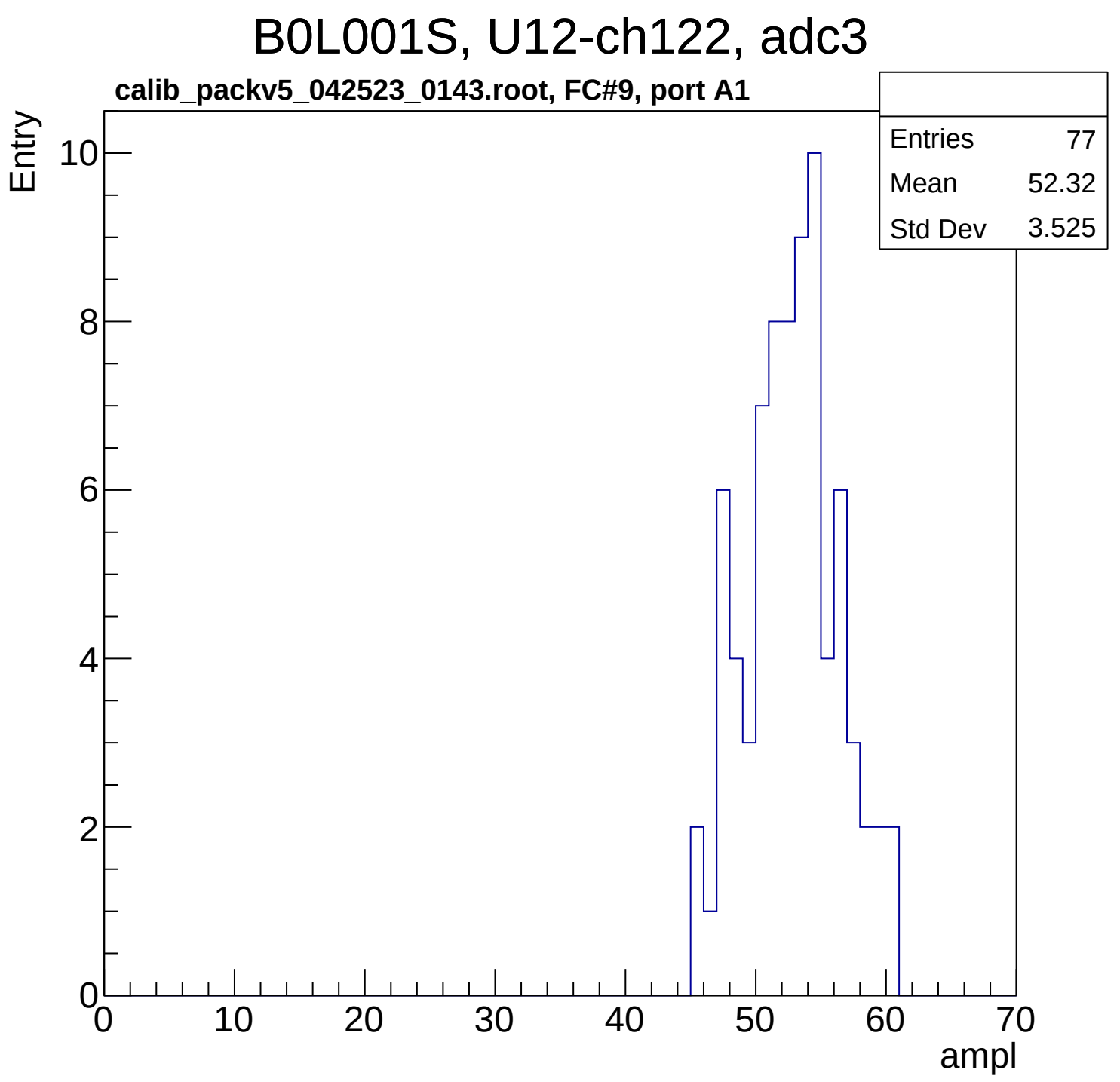

B0L001S, U12-ch121, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

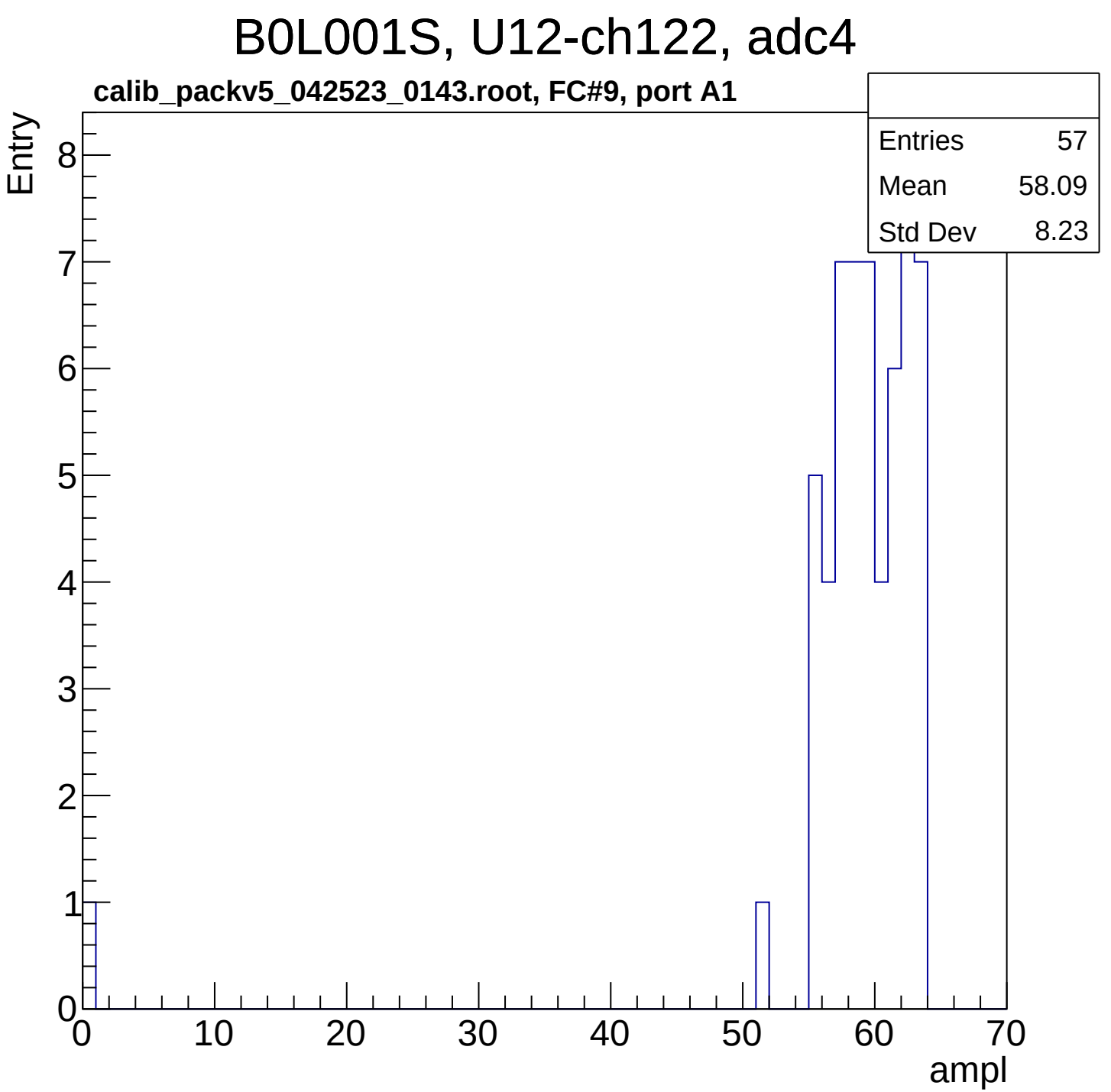

B0L001S, U12-ch121, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch122, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 69
Mean 31.49
Std Dev 6.513
Gaus mean : 33.4967
Gaus Width: 3.2131
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch122, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 64
Mean 39.55
Std Dev 3.278
Gaus mean : 40.6051
Gaus Width: 3.3451
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch122, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 60
Mean 45.55
Std Dev 3.584
Gaus mean : 46.2268
Gaus Width: 3.6287
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch122, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 77
Mean 52.32
Std Dev 3.525
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch122, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 57
Mean 58.09
Std Dev 8.23
Entry
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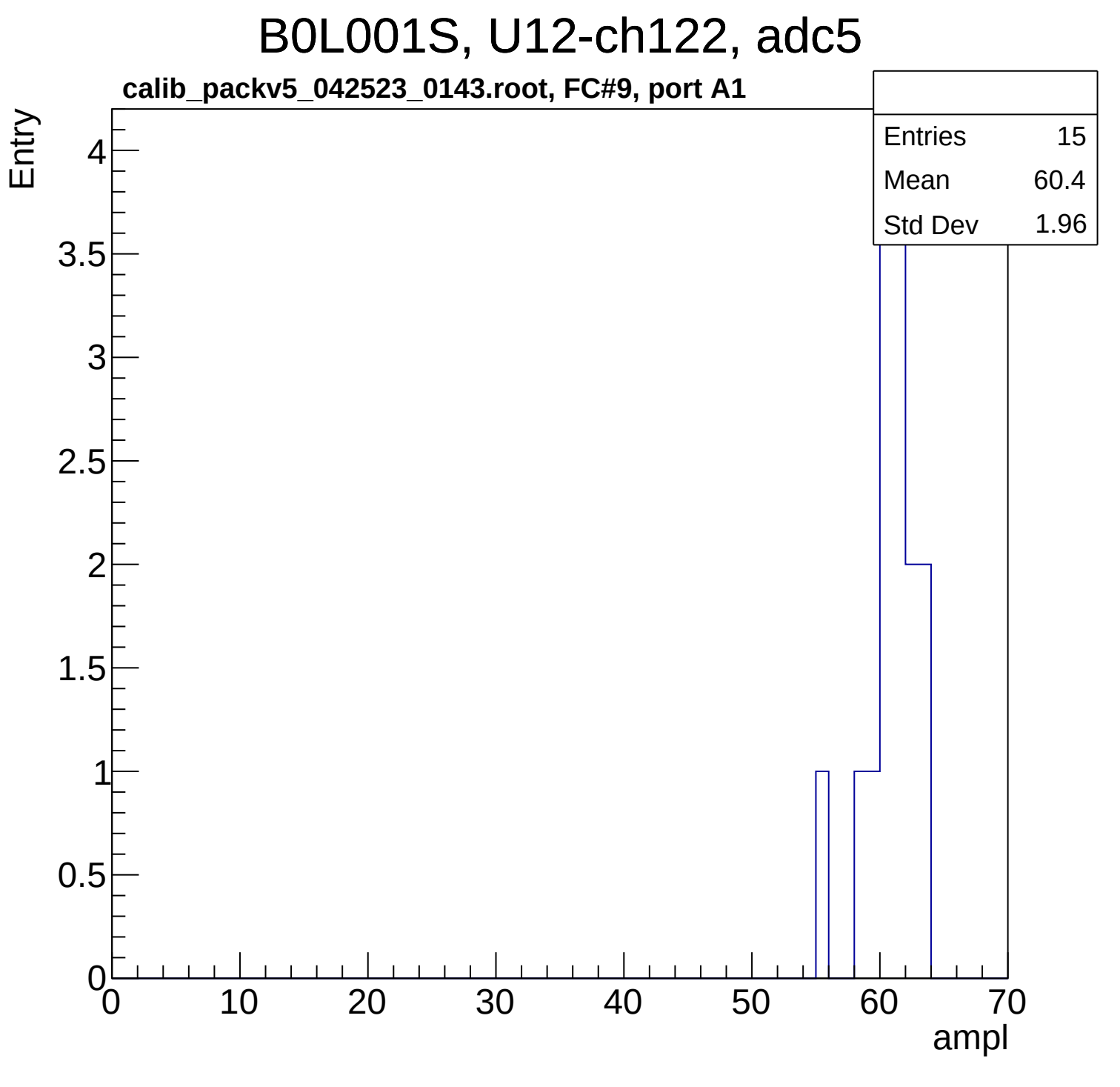
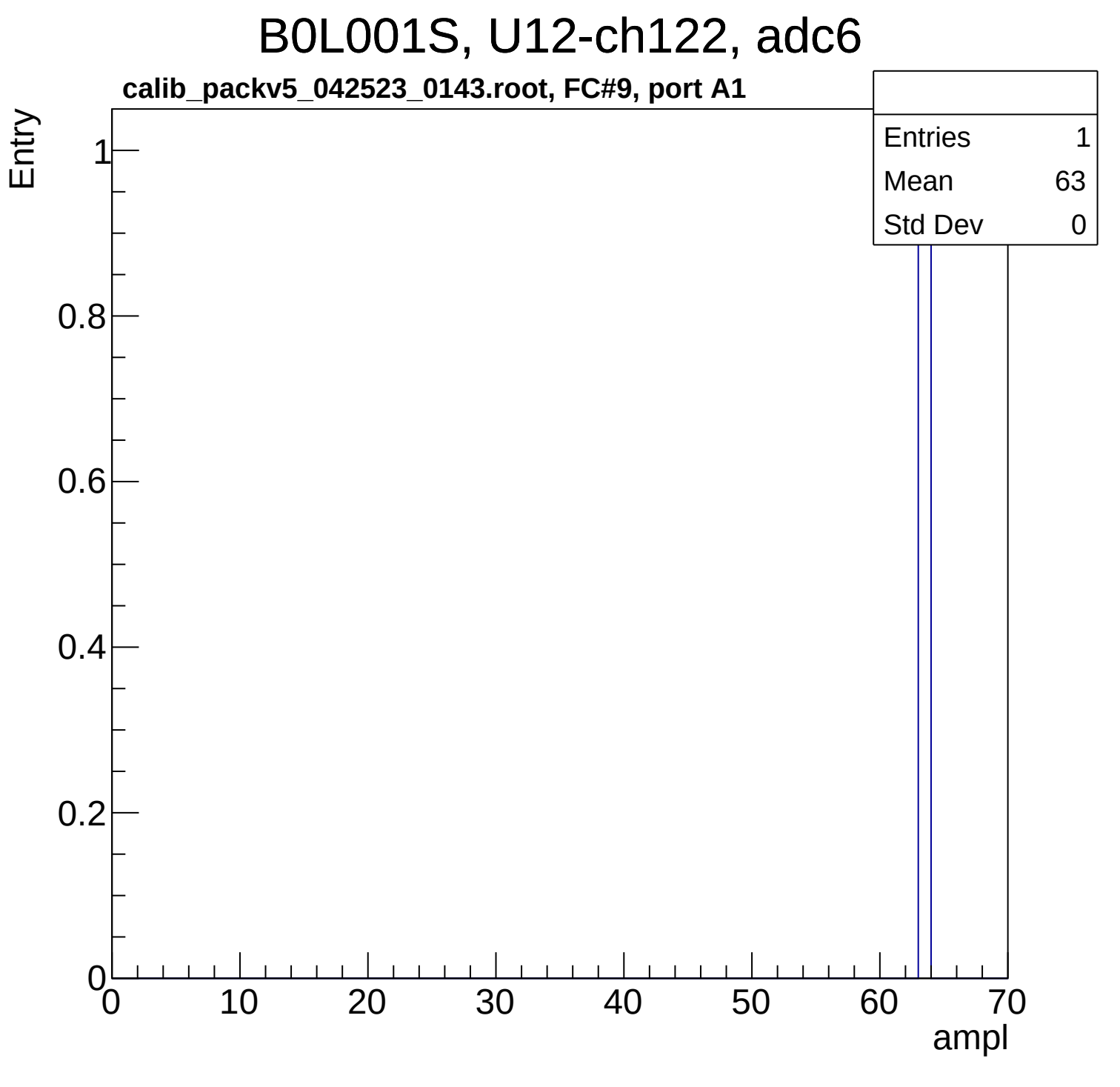
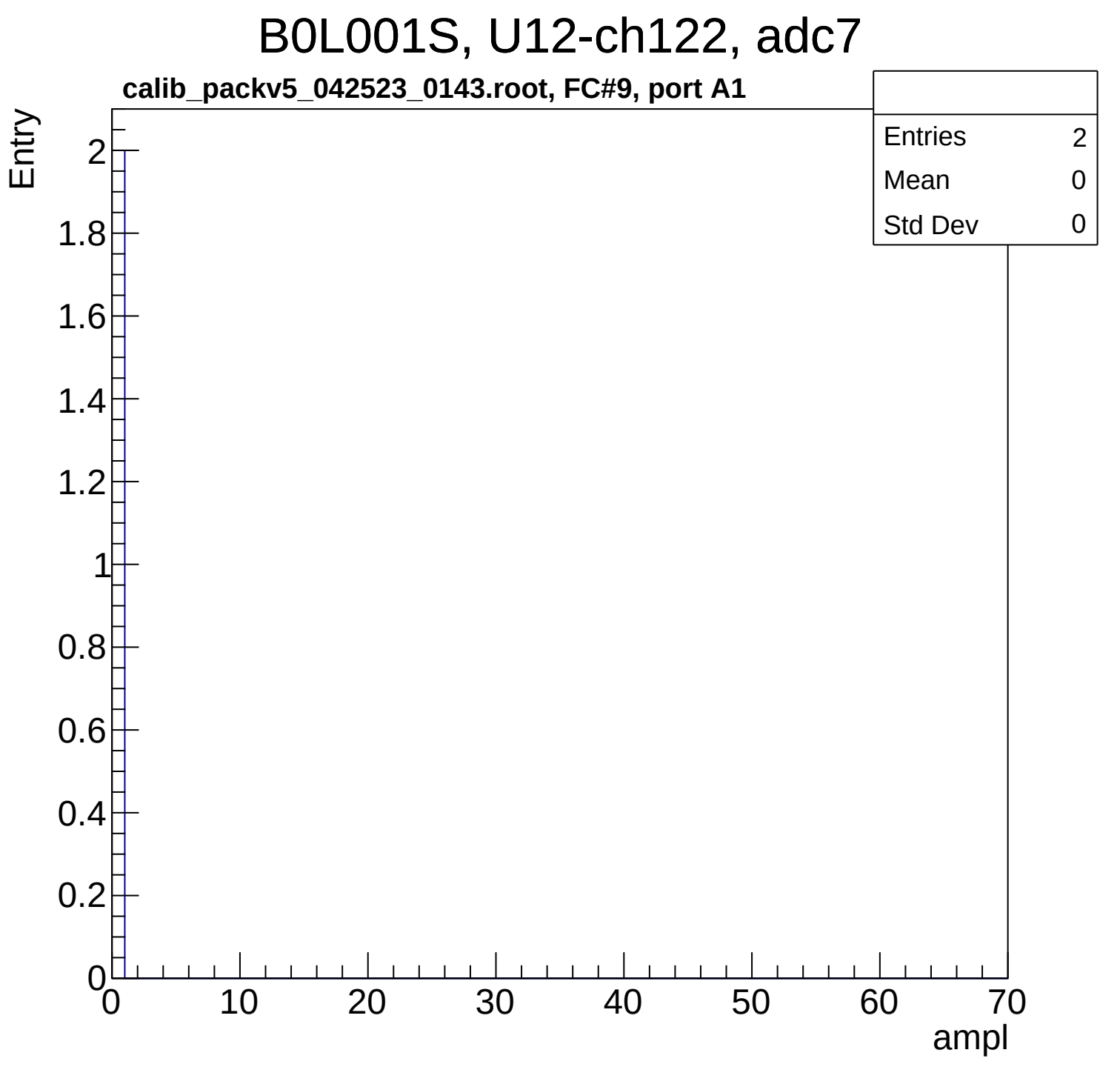
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch122, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 15
Mean 60.4
Std Dev 1.96
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B0L001S, U12-ch122, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch122, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
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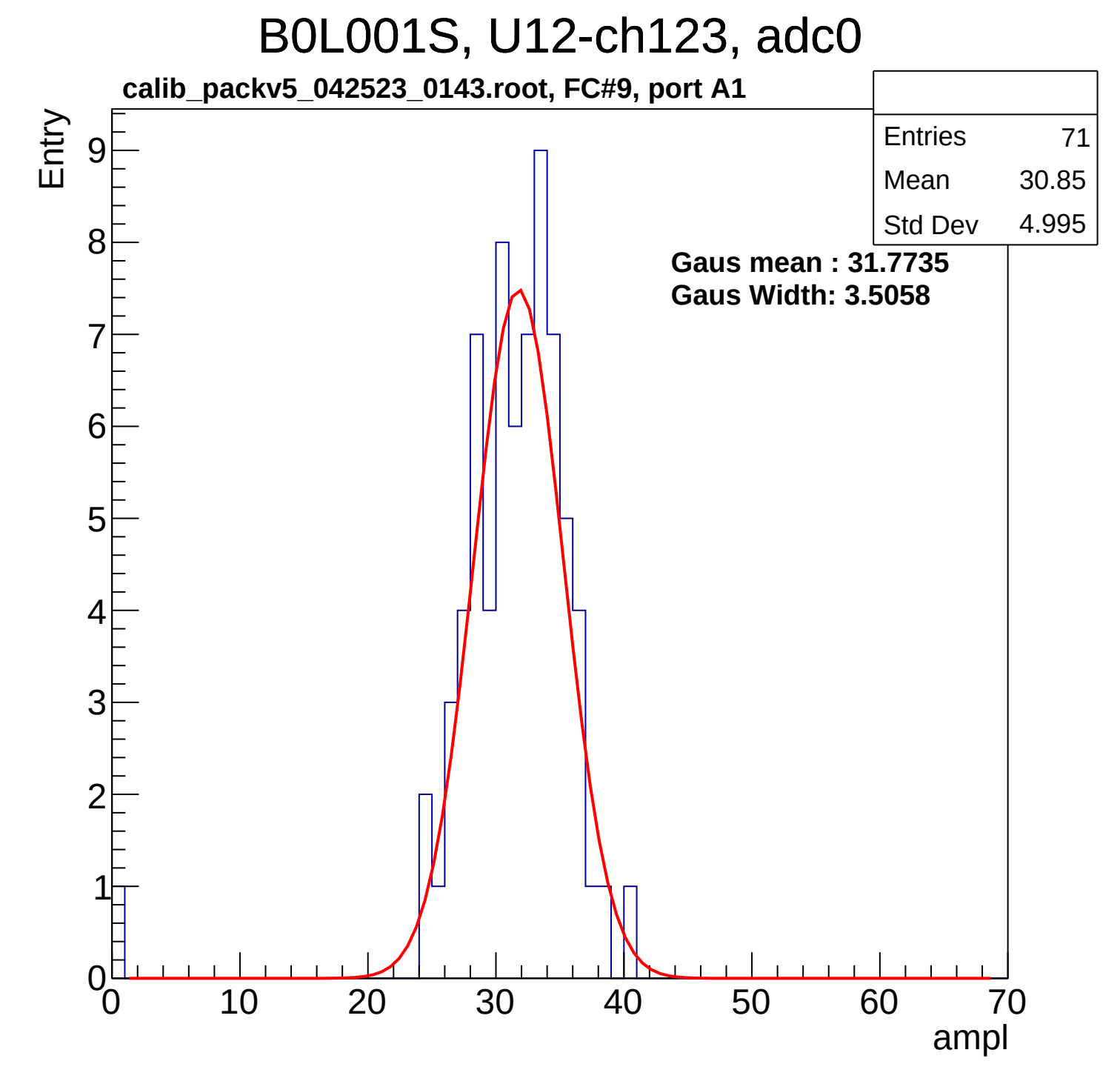
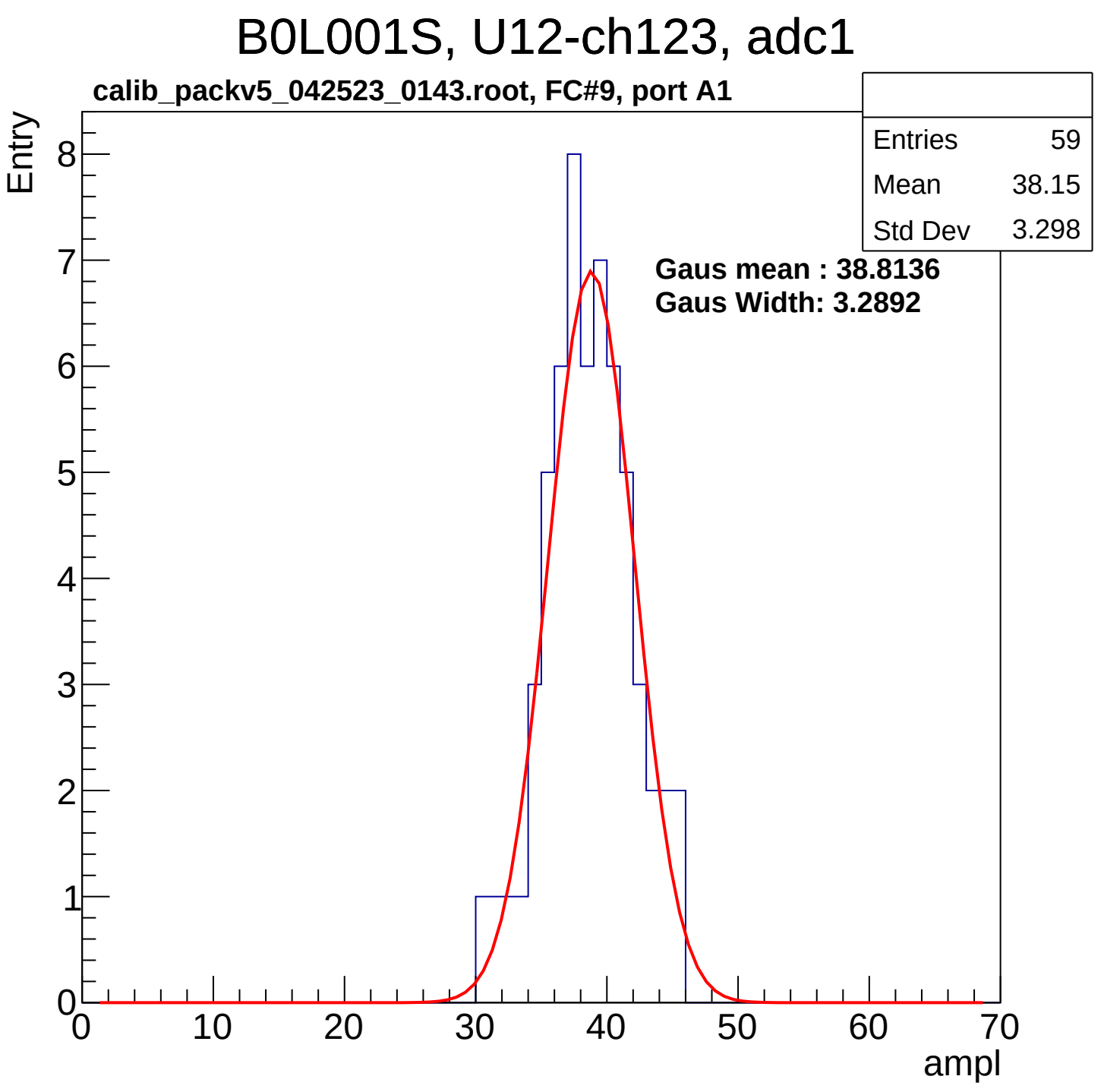
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch123, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 71
Mean 30.85
Std Dev 4.995
Gaus mean : 31.7735
Gaus Width: 3.5058
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch123, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 59
Mean 38.15
Std Dev 3.298
Gaus mean : 38.8136
Gaus Width: 3.2892
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
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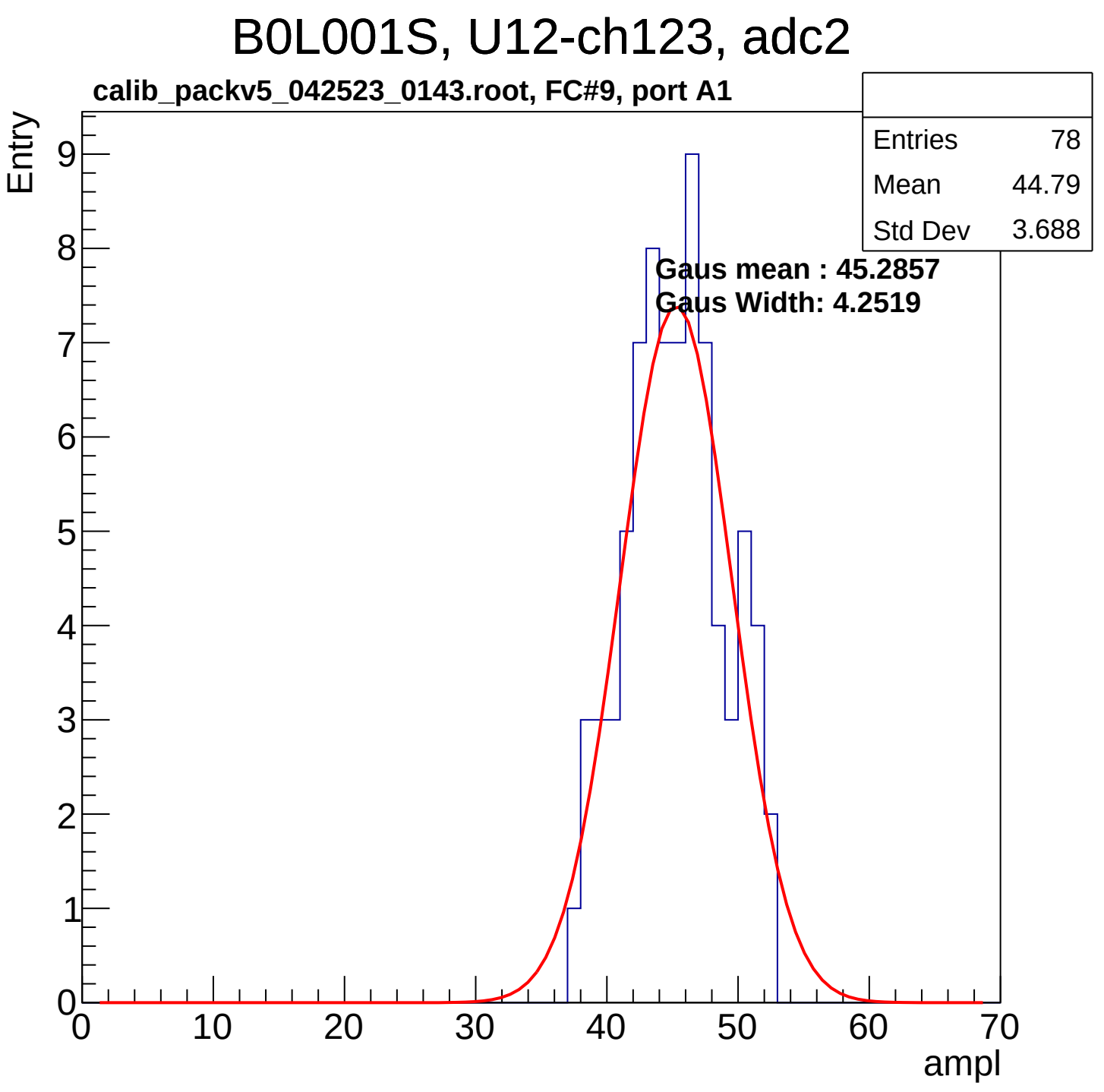
B0L001S, U12-ch123, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 78
Mean 44.79
Std Dev 3.688
Gaus mean : 45.2857
Gaus Width: 4.2519
Entry
ampl
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2
3
4
5
6
7
8
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0
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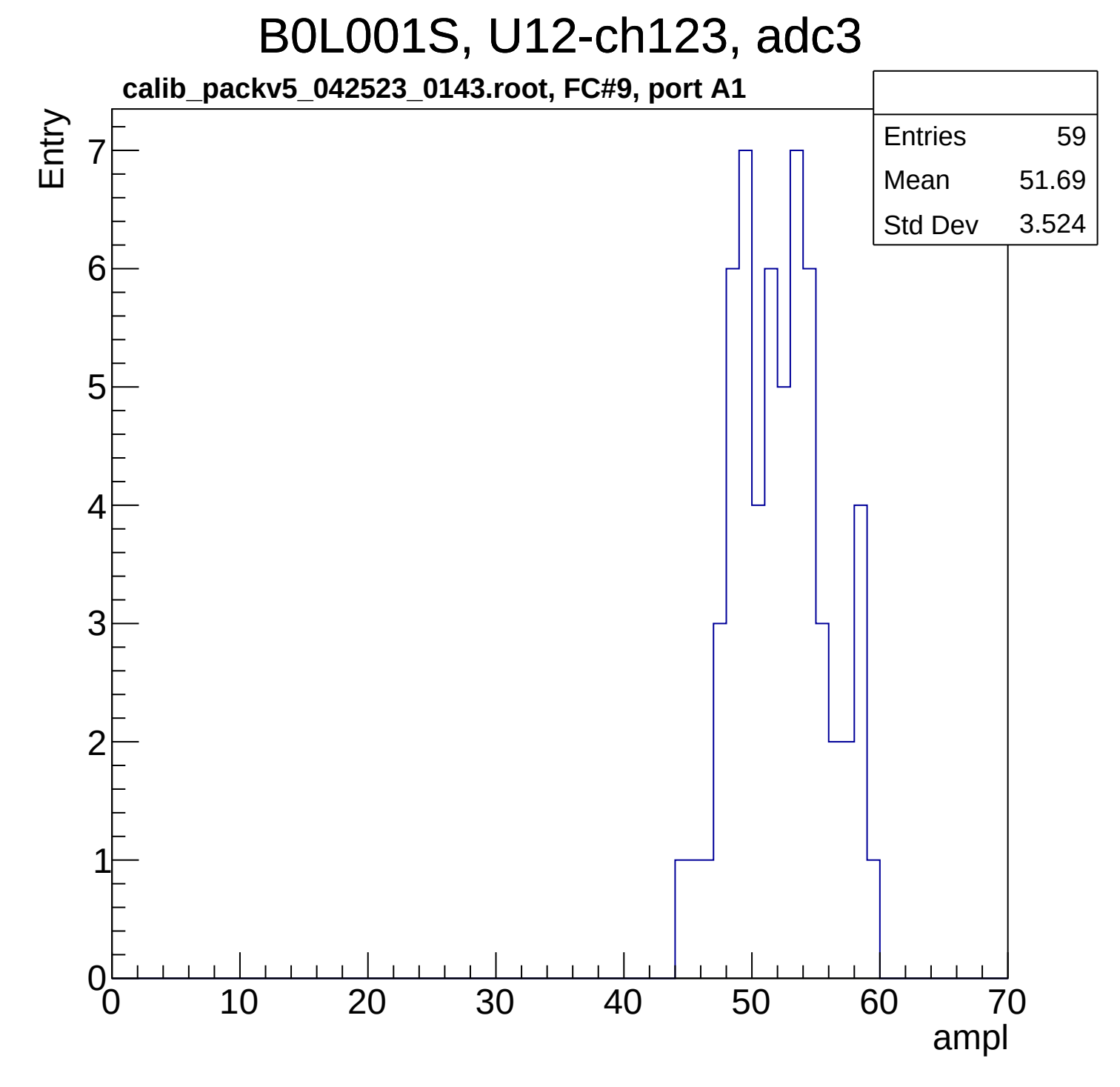
B0L001S, U12-ch123, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 59
Mean 51.69
Std Dev 3.524
Entry
ampl
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4
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0
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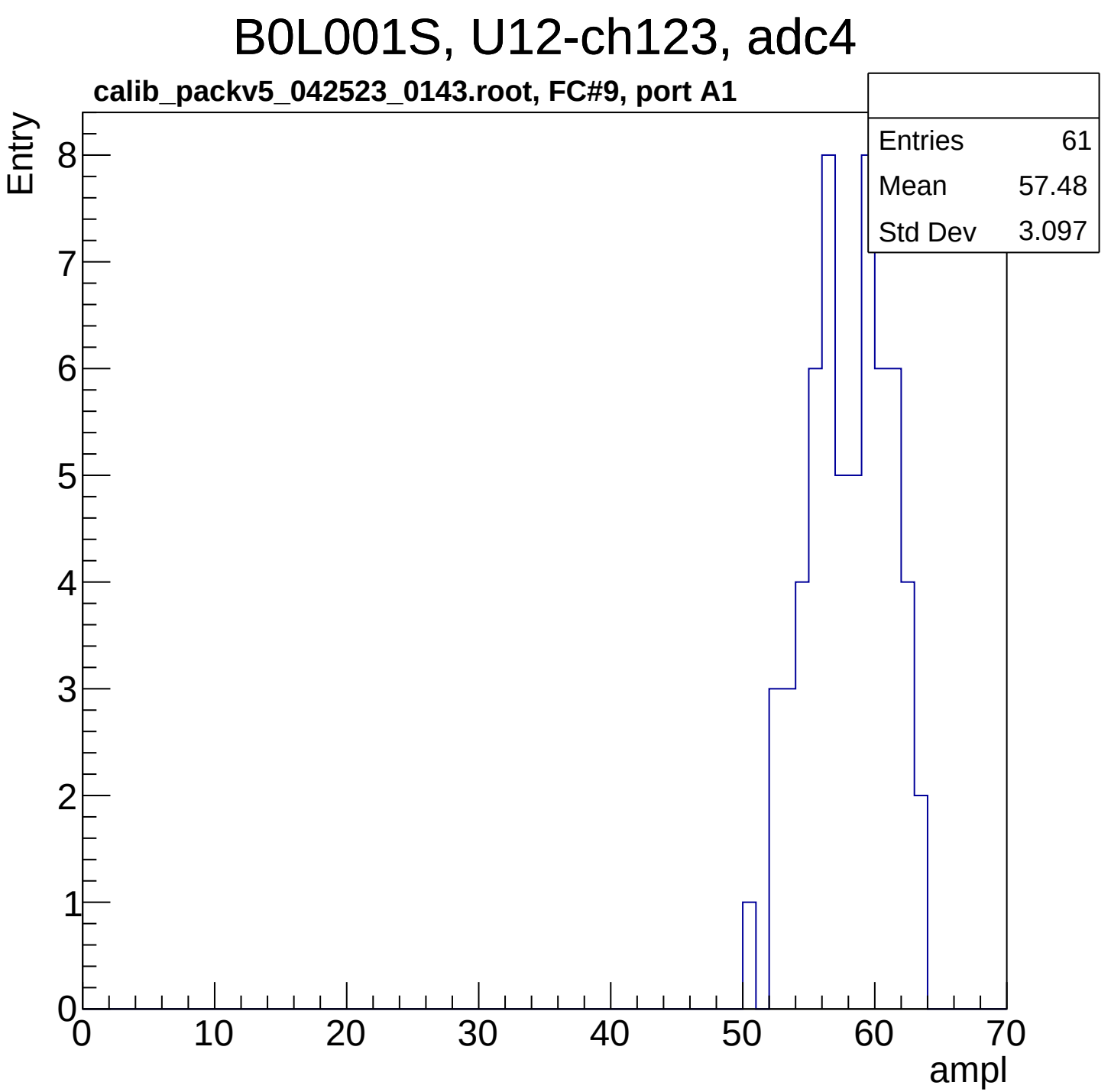
B0L001S, U12-ch123, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 61
Mean 57.48
Std Dev 3.097
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
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40
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60
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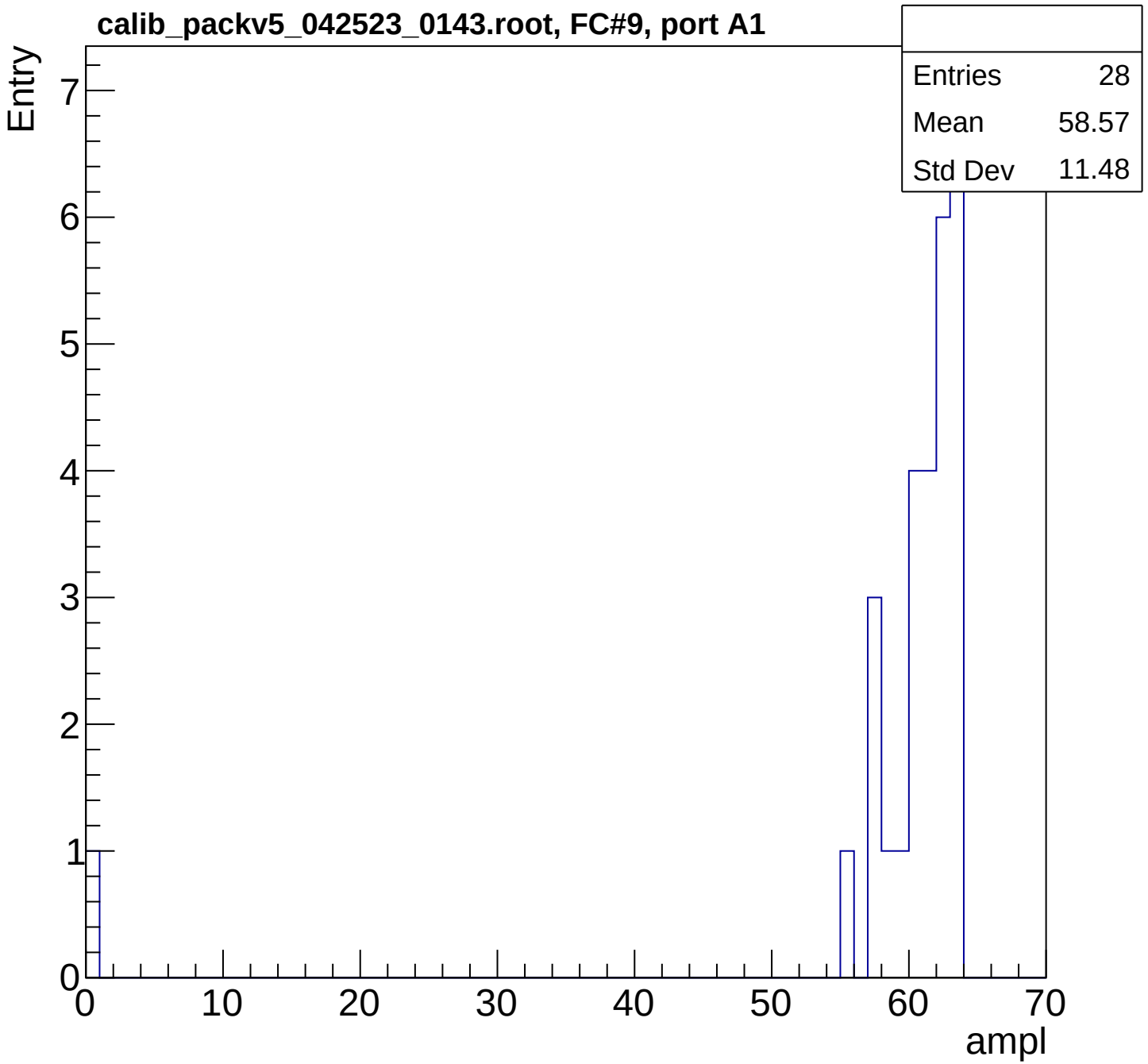
B0L001S, U12-ch123, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 28
Mean 58.57
Std Dev 11.48
Entry
0
1
2
3
4
5
6
7
0
10
20
30
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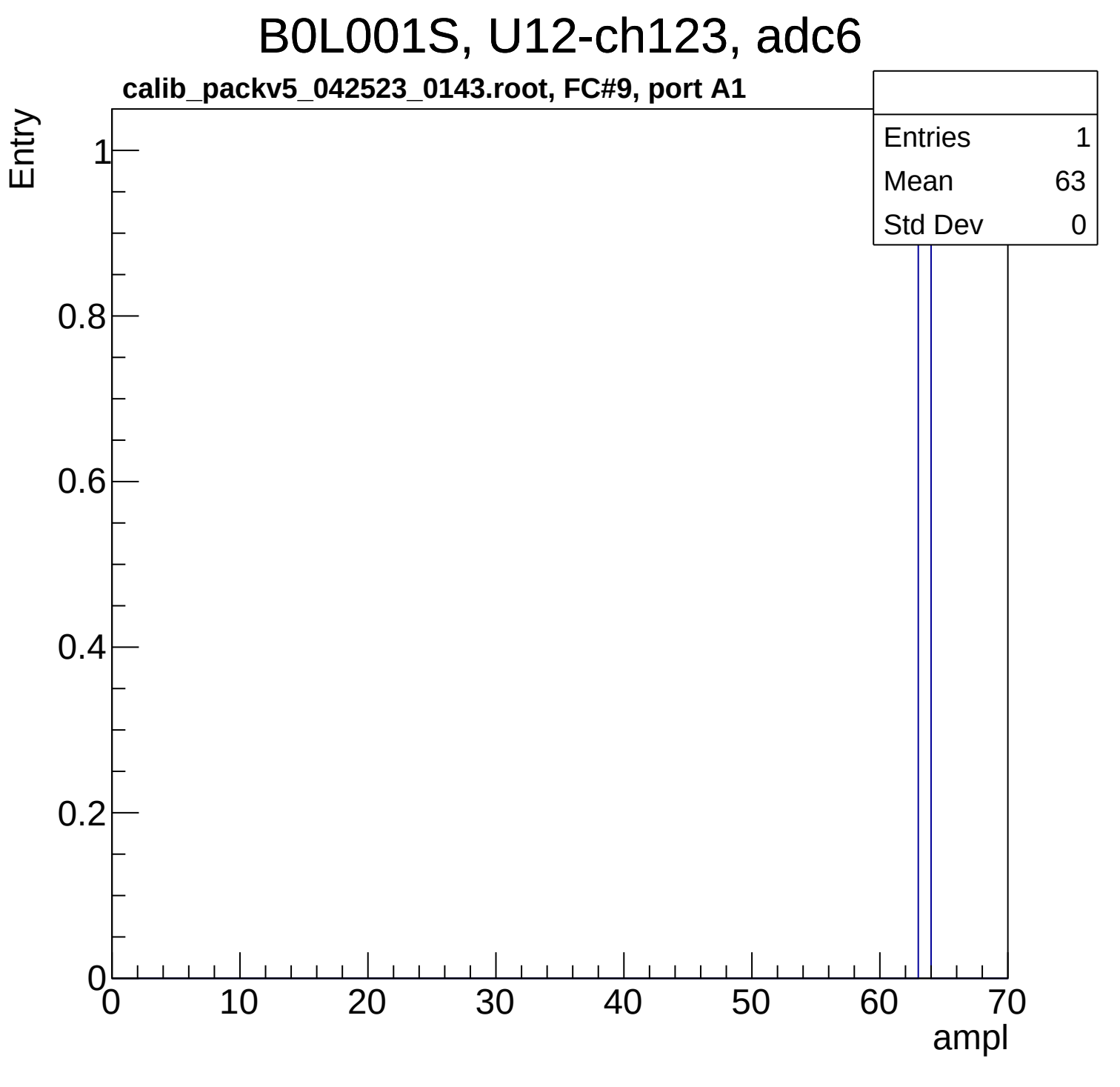
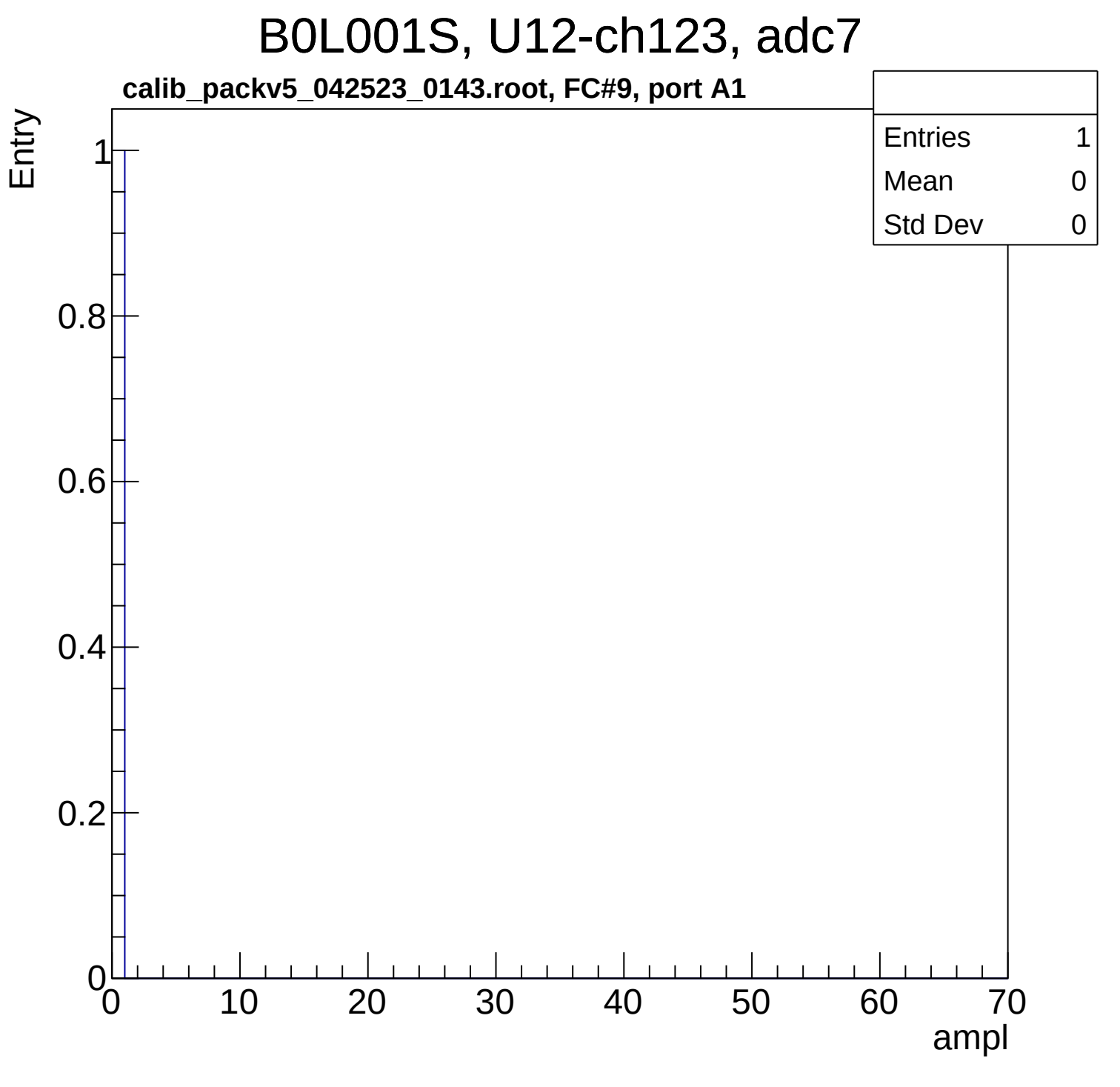
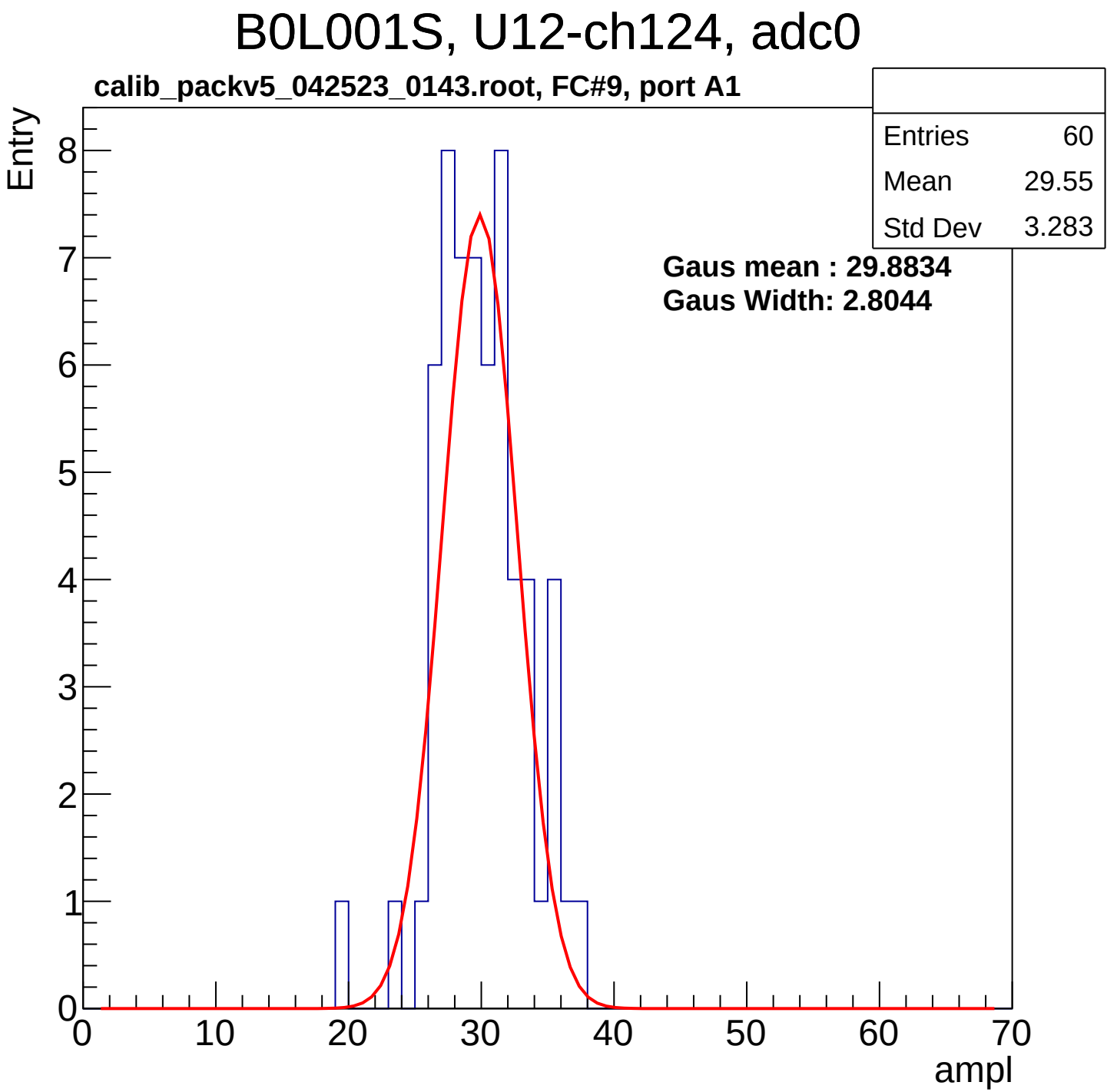
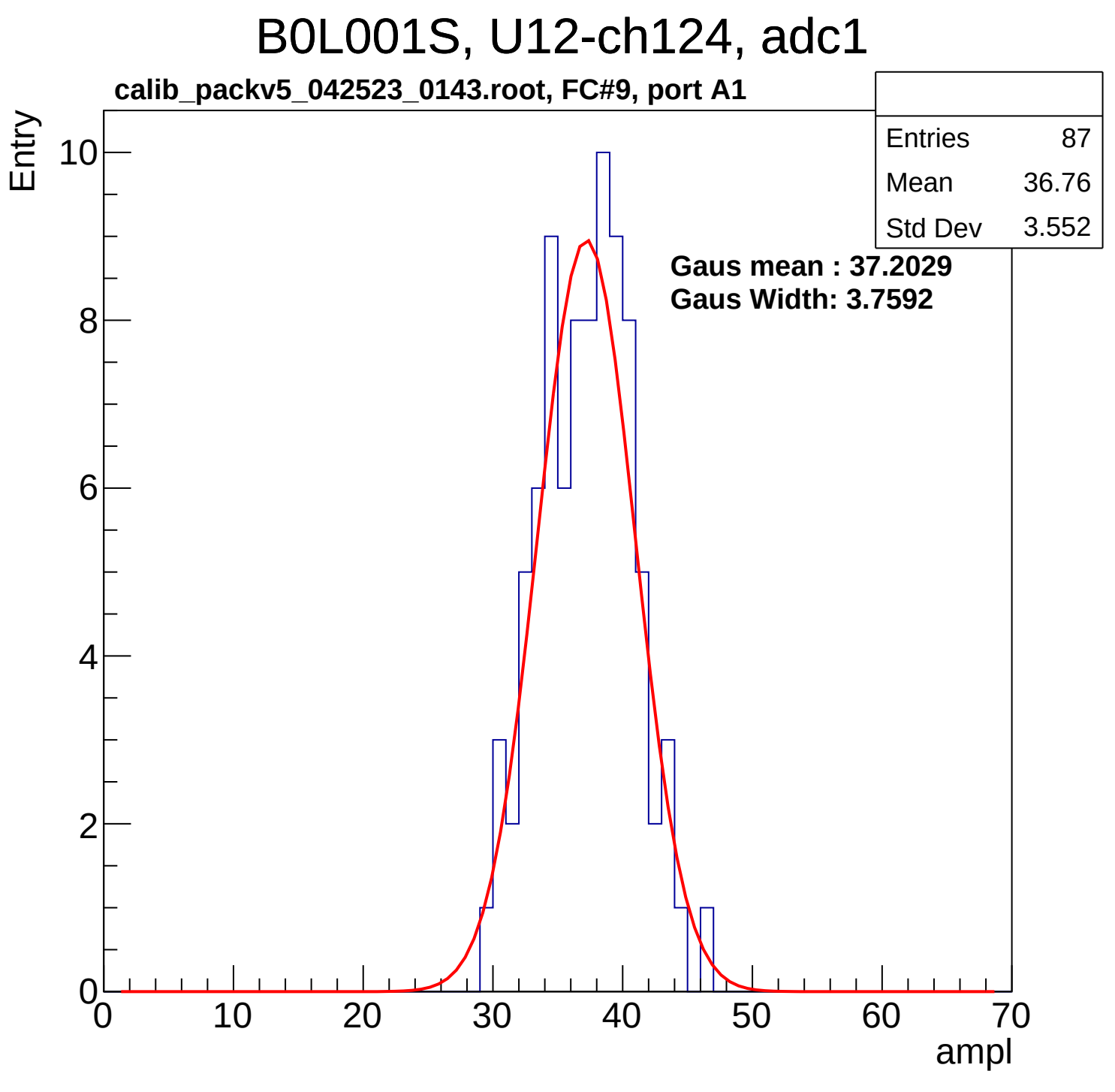
50
60
70
ampl


B0L001S, U12-ch123, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch123, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch124, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 60
Mean 29.55
Std Dev 3.283
Gaus mean : 29.8834
Gaus Width: 2.8044
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch124, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 87
Mean 36.76
Std Dev 3.552
Gaus mean : 37.2029
Gaus Width: 3.7592
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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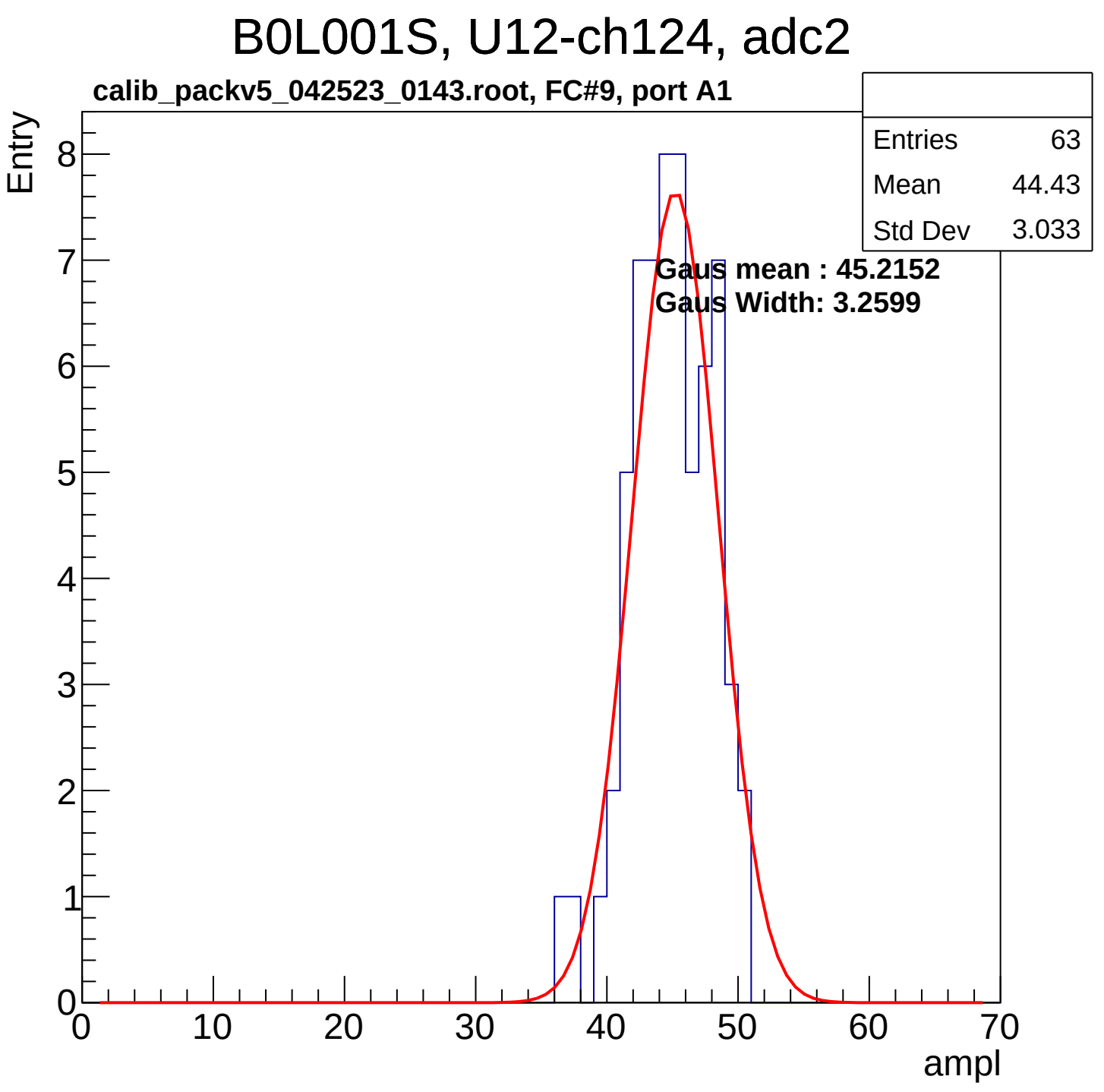
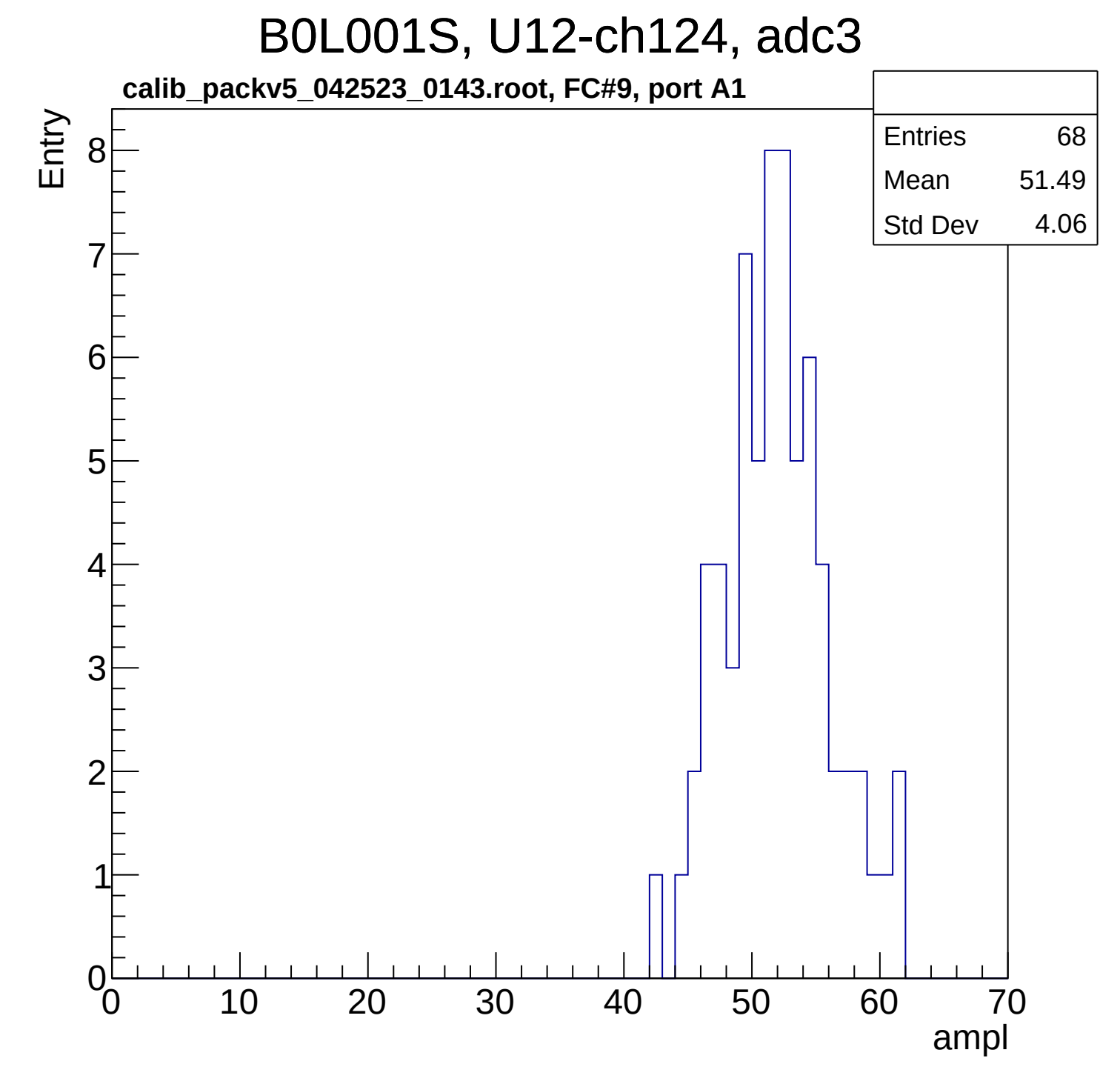
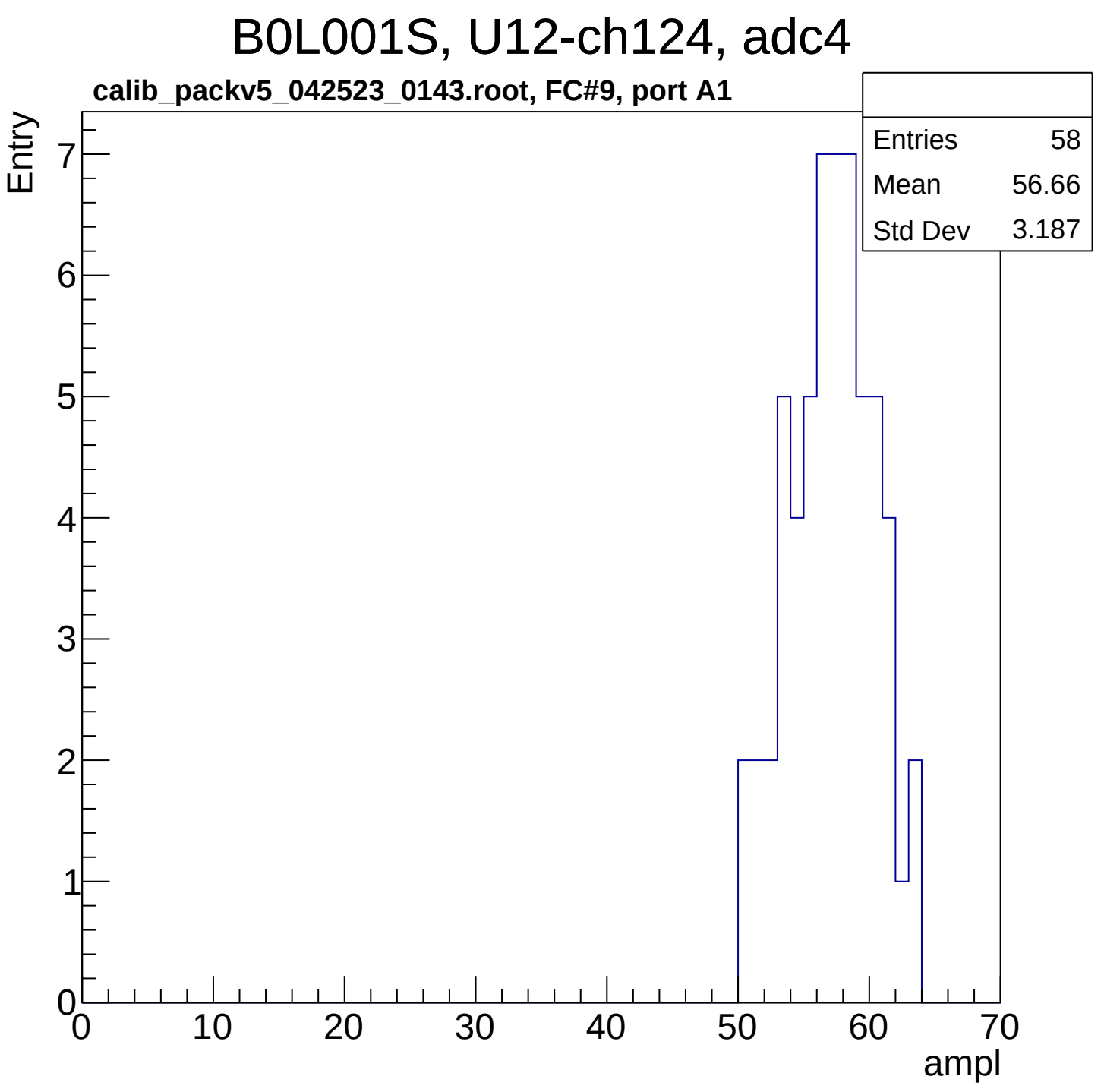

B0L001S, U12-ch124, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 63
Mean 44.43
Std Dev 3.033
Gaus mean : 45.2152
Gaus Width: 3.2599
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch124, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 68
Mean 51.49
Std Dev 4.06
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch124, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 58
Mean 56.66
Std Dev 3.187
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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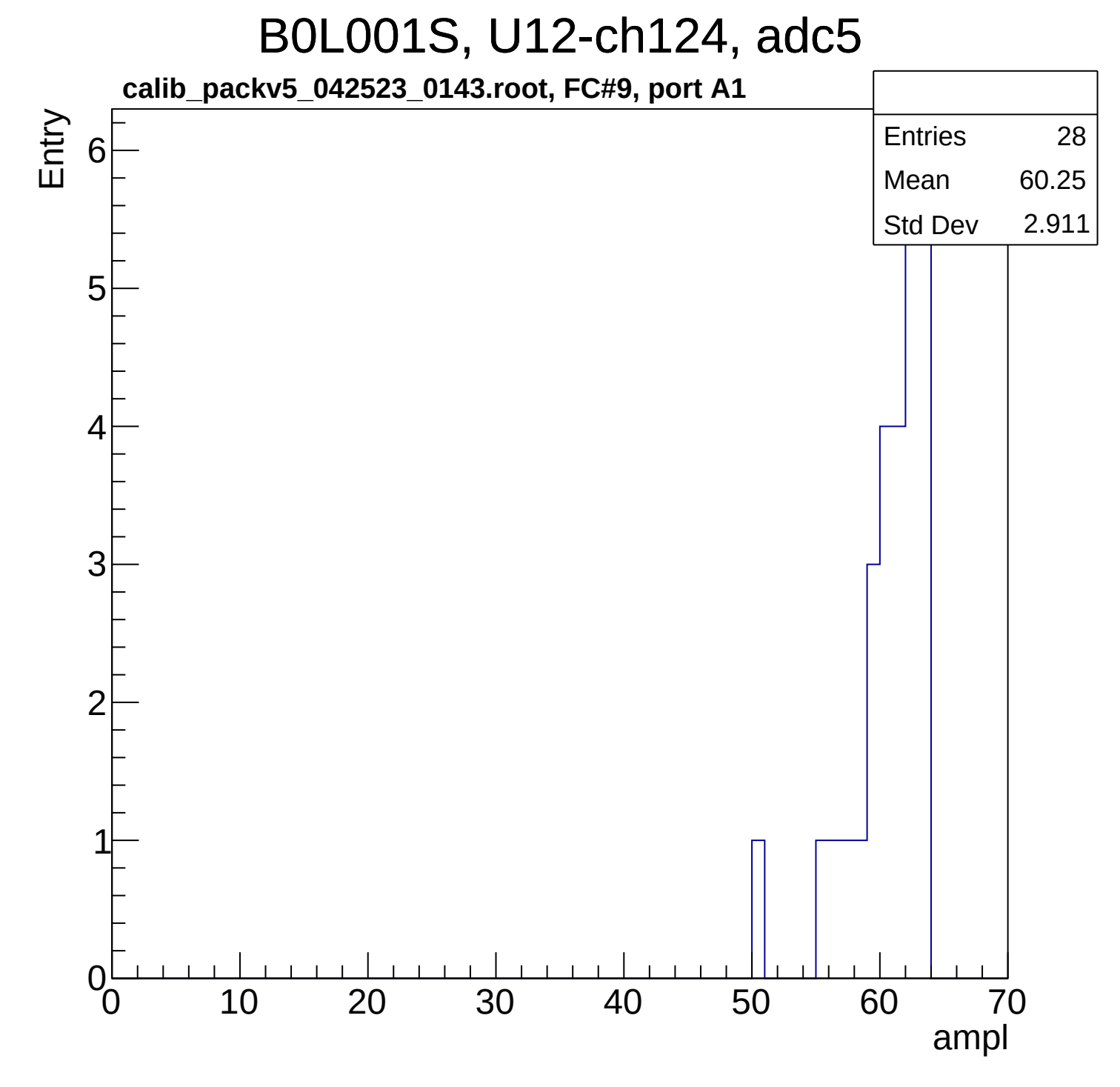
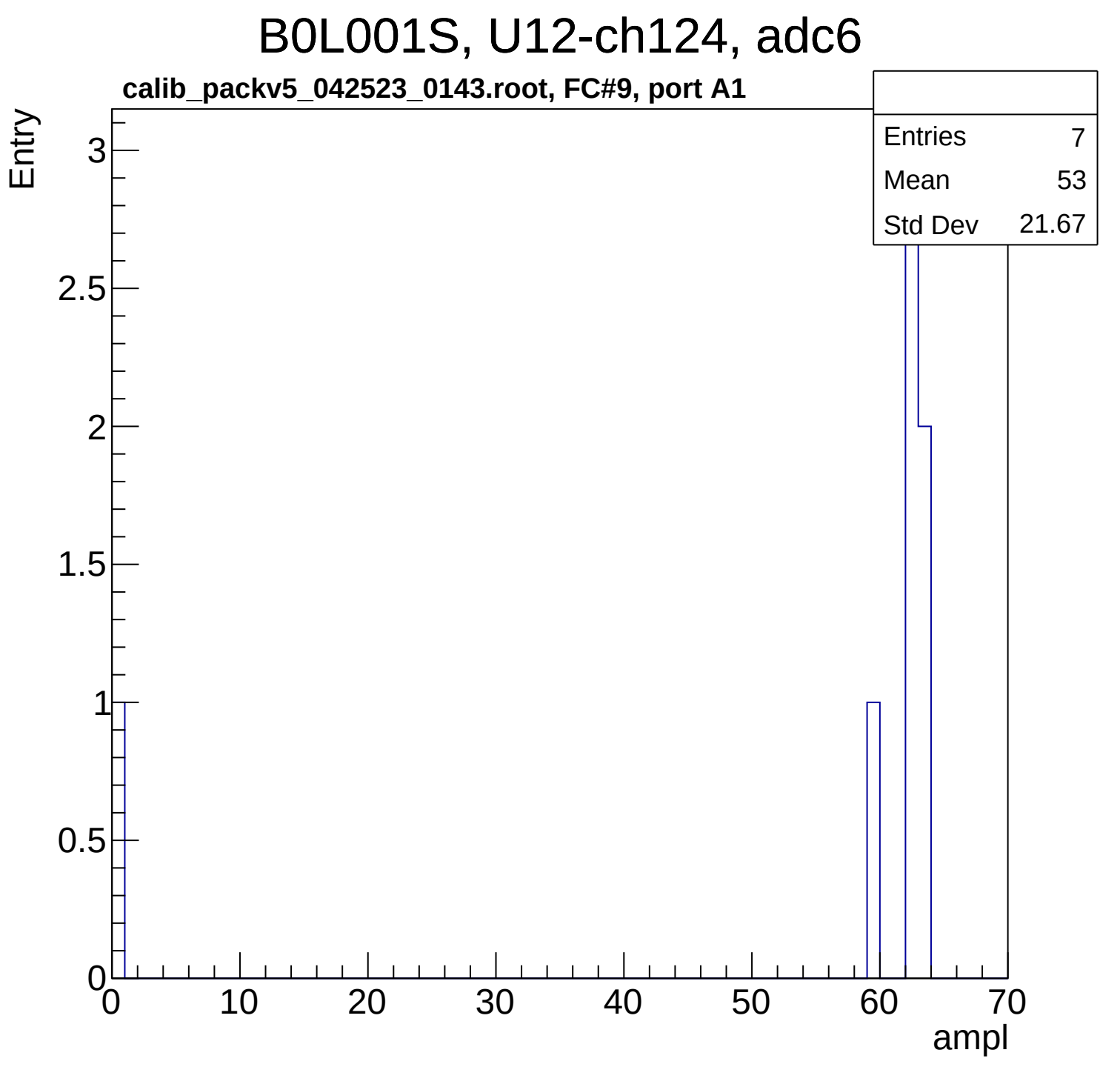

B0L001S, U12-ch124, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 28
Mean 60.25
Std Dev 2.911
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch124, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 7
Mean 53
Std Dev 21.67
Entry
ampl
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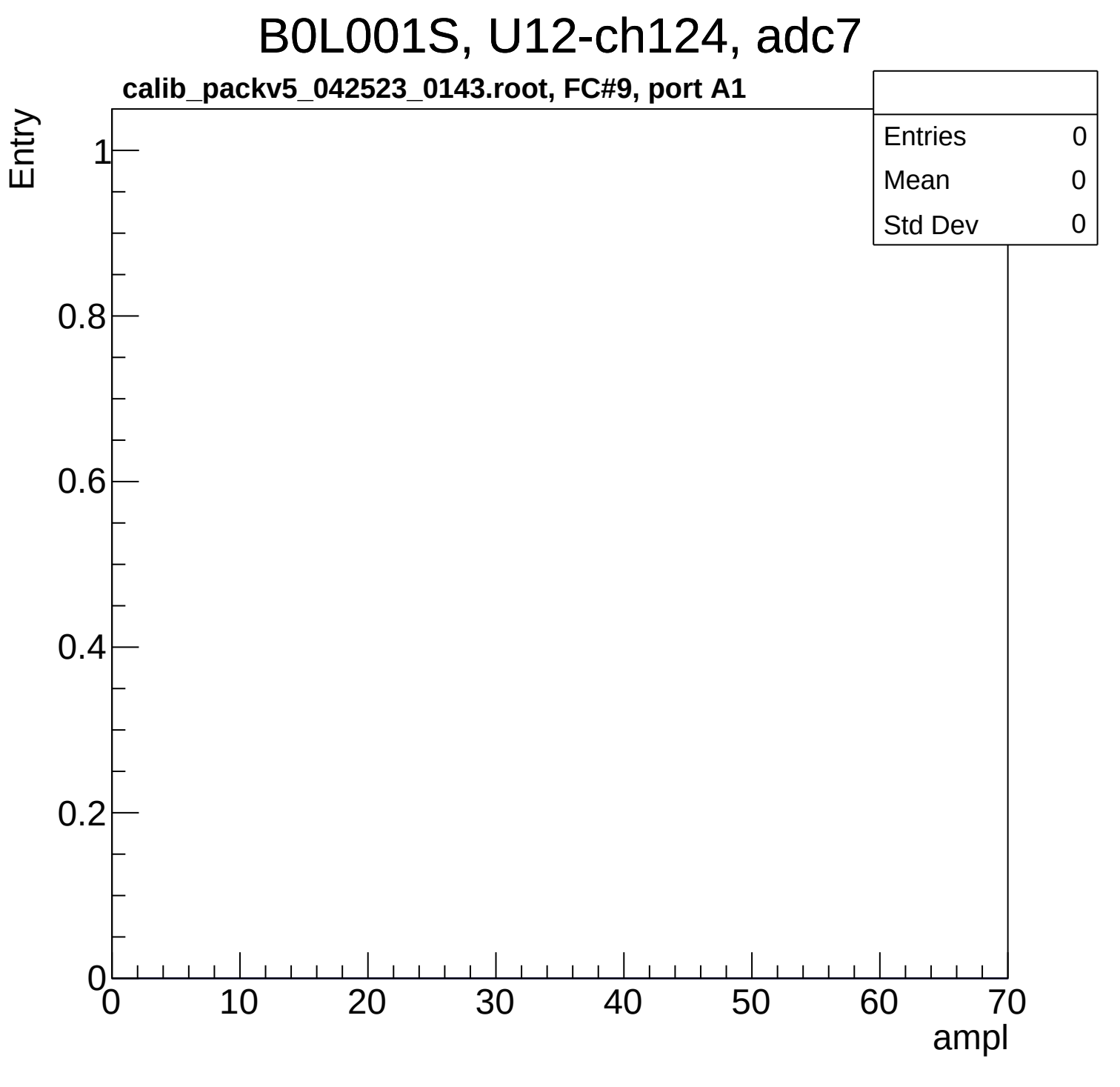
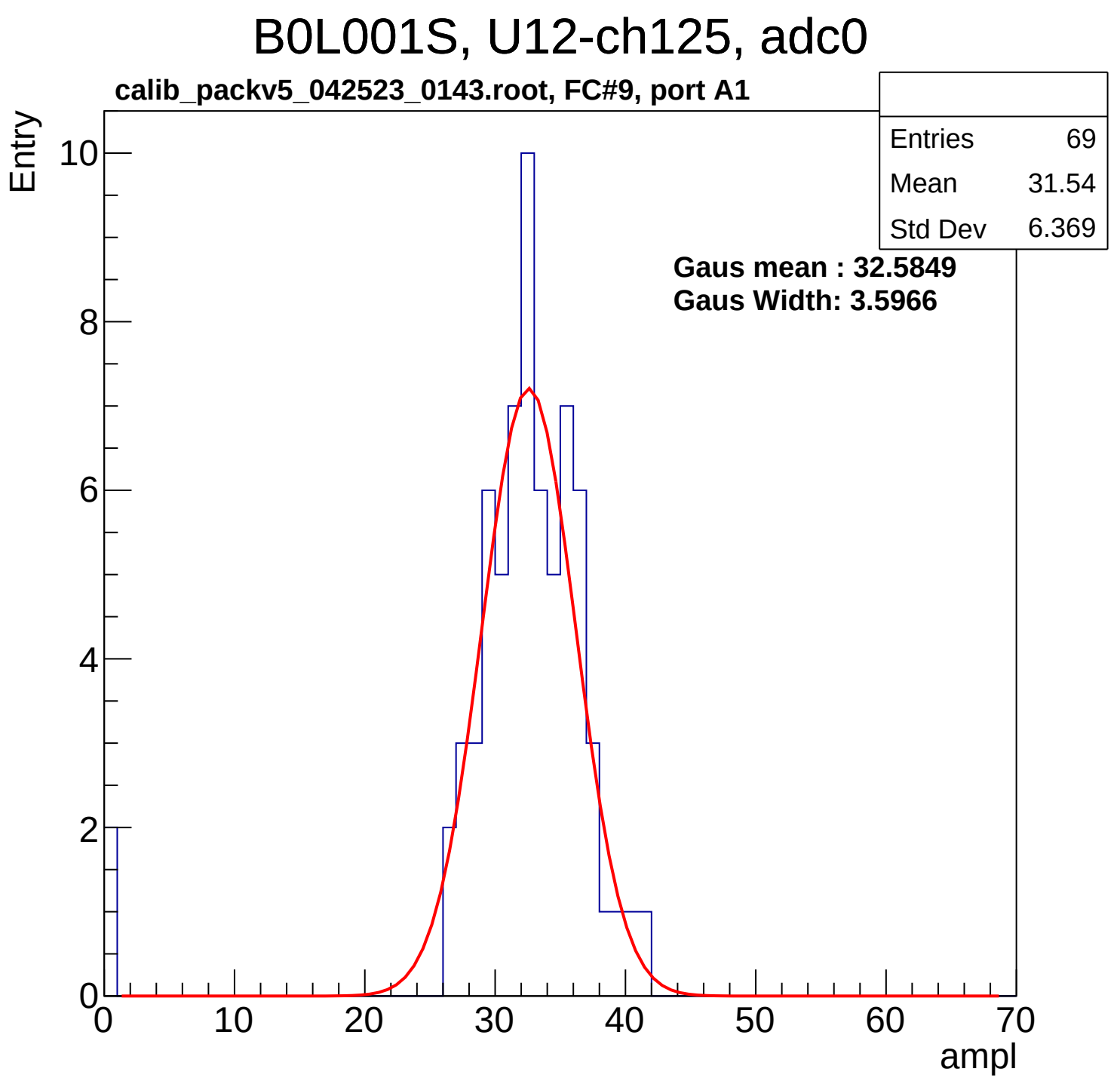
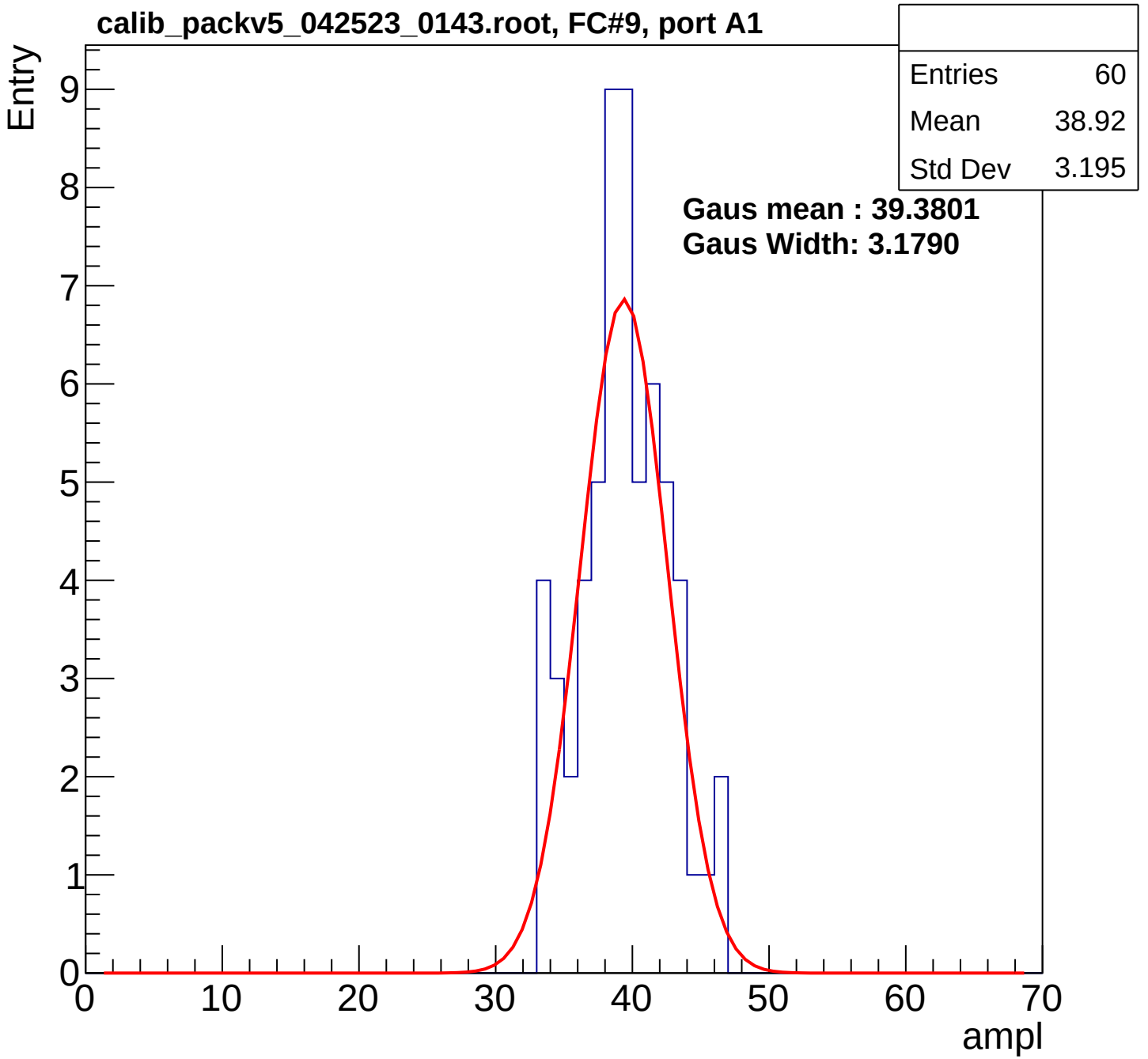
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B0L001S, U12-ch124, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch125, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 69
Mean 31.54
Std Dev 6.369
Gaus mean : 32.5849
Gaus Width: 3.5966
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B0L001S, U12-ch125, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 60
Mean 38.92
Std Dev 3.195
Gaus mean : 39.3801
Gaus Width: 3.1790
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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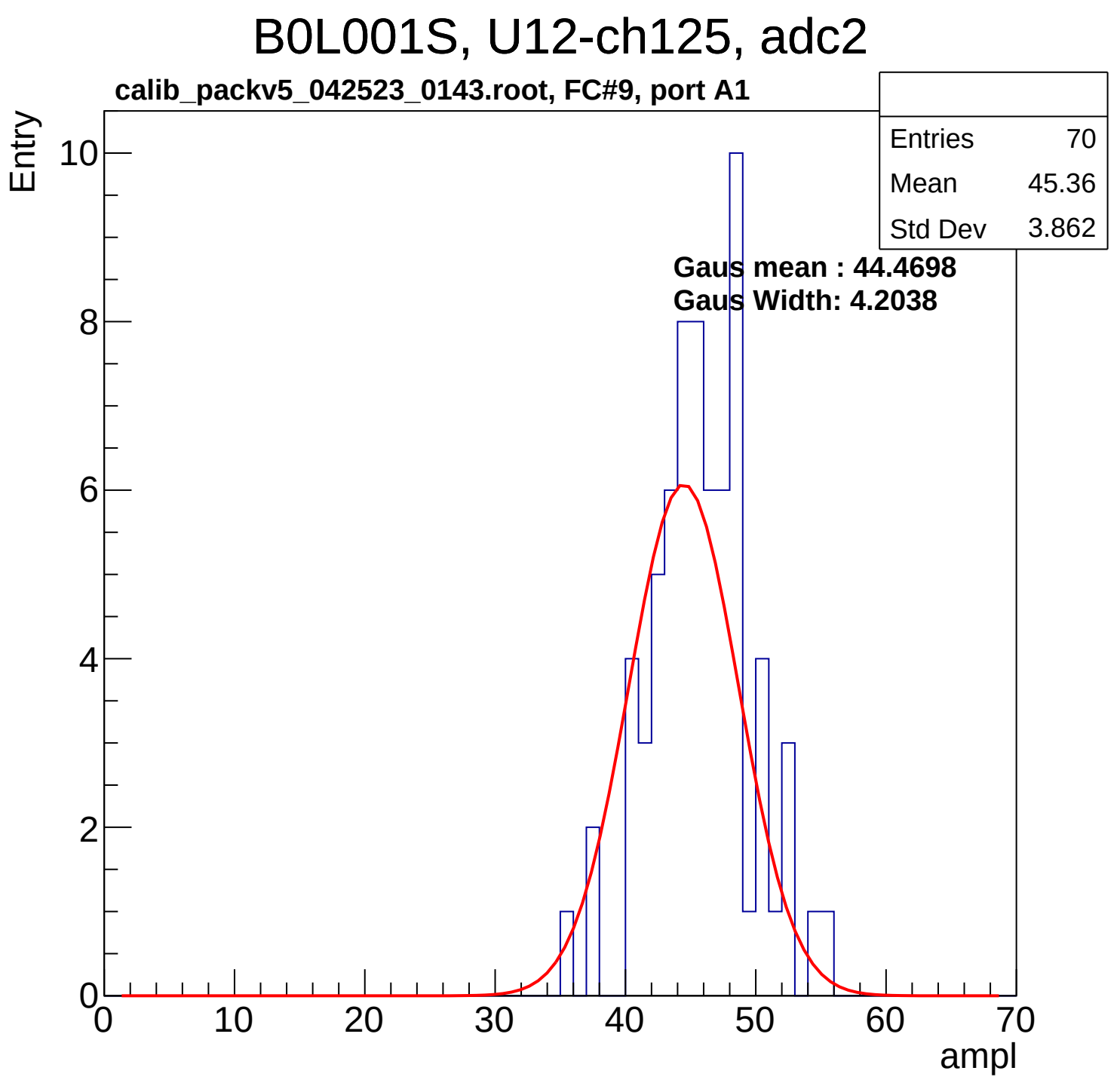
B0L001S, U12-ch125, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 70
Mean 45.36
Std Dev 3.862
Gaus mean : 44.4698
Gaus Width: 4.2038
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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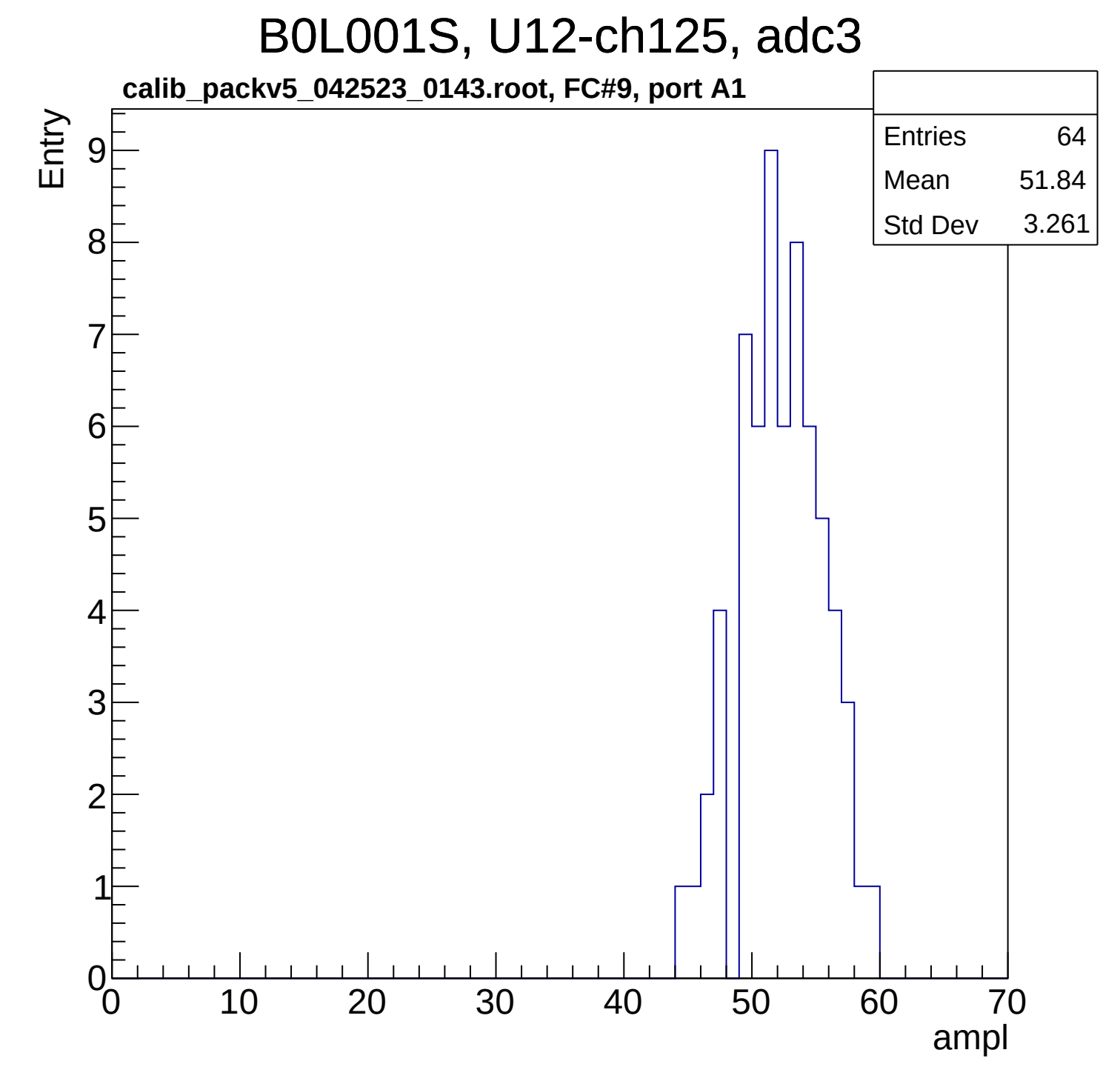
B0L001S, U12-ch125, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 64
Mean 51.84
Std Dev 3.261
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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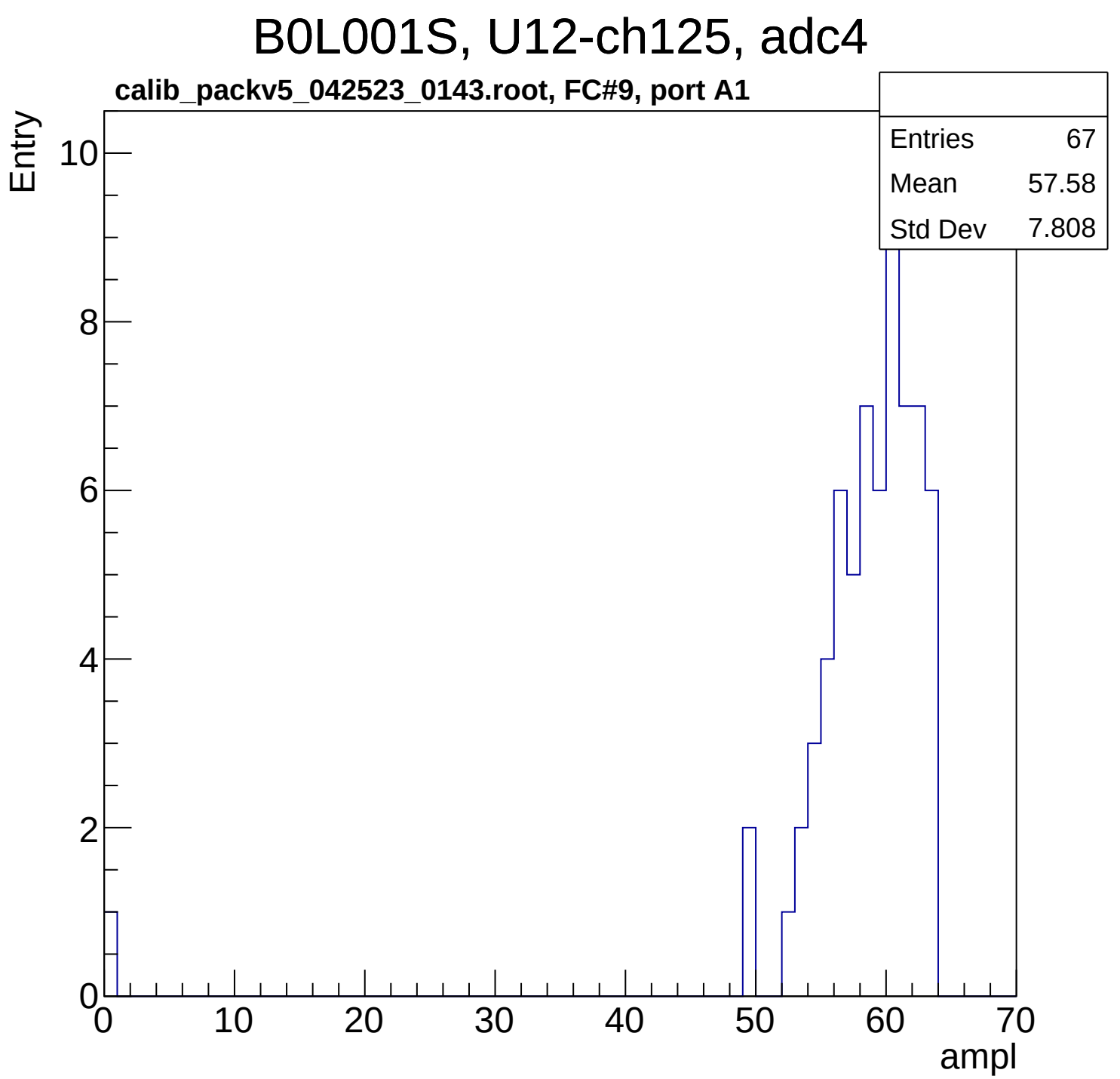
B0L001S, U12-ch125, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 67
Mean 57.58
Std Dev 7.808
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
50
60
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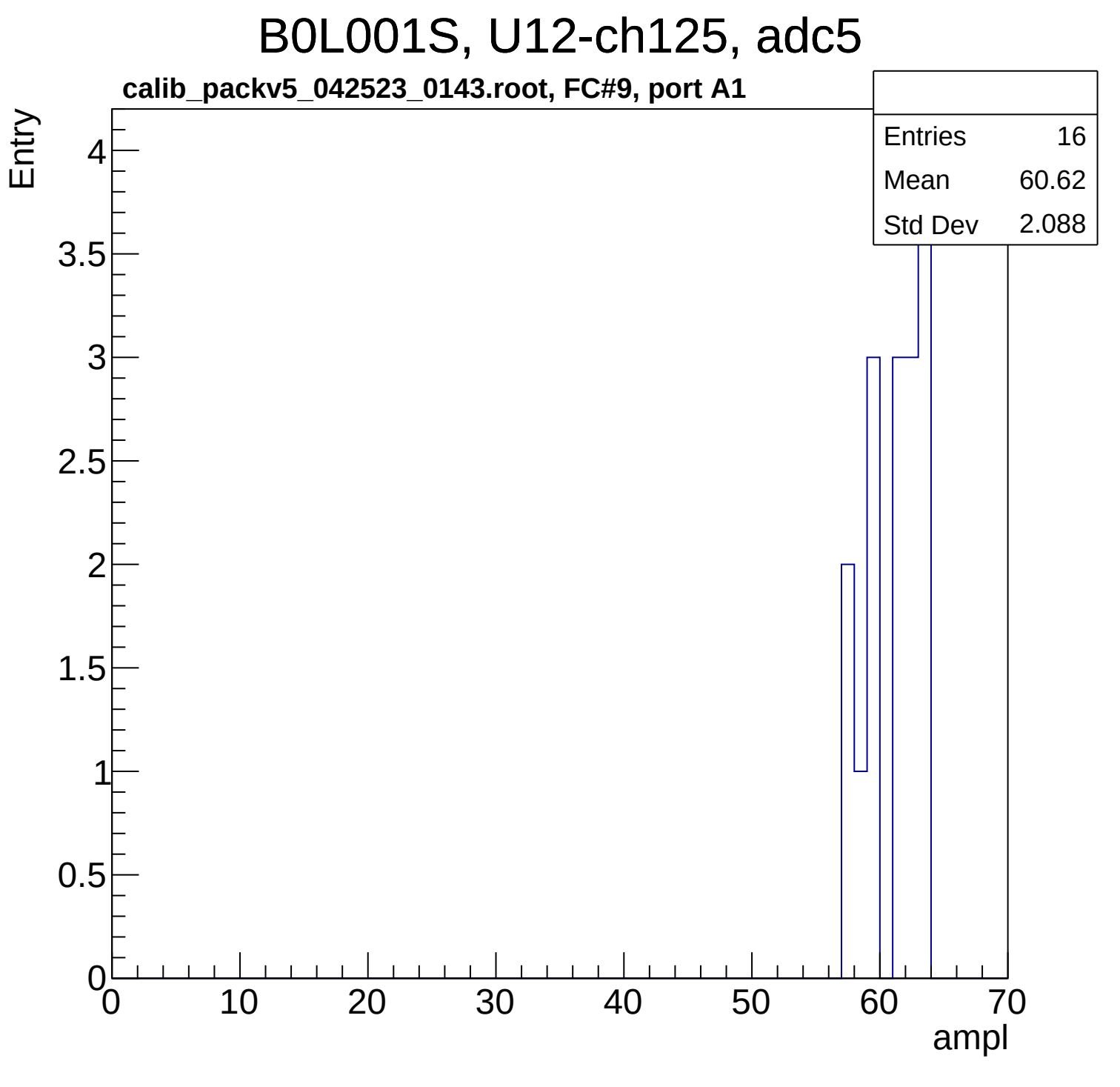
B0L001S, U12-ch125, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 16
Mean 60.62
Std Dev 2.088
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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60
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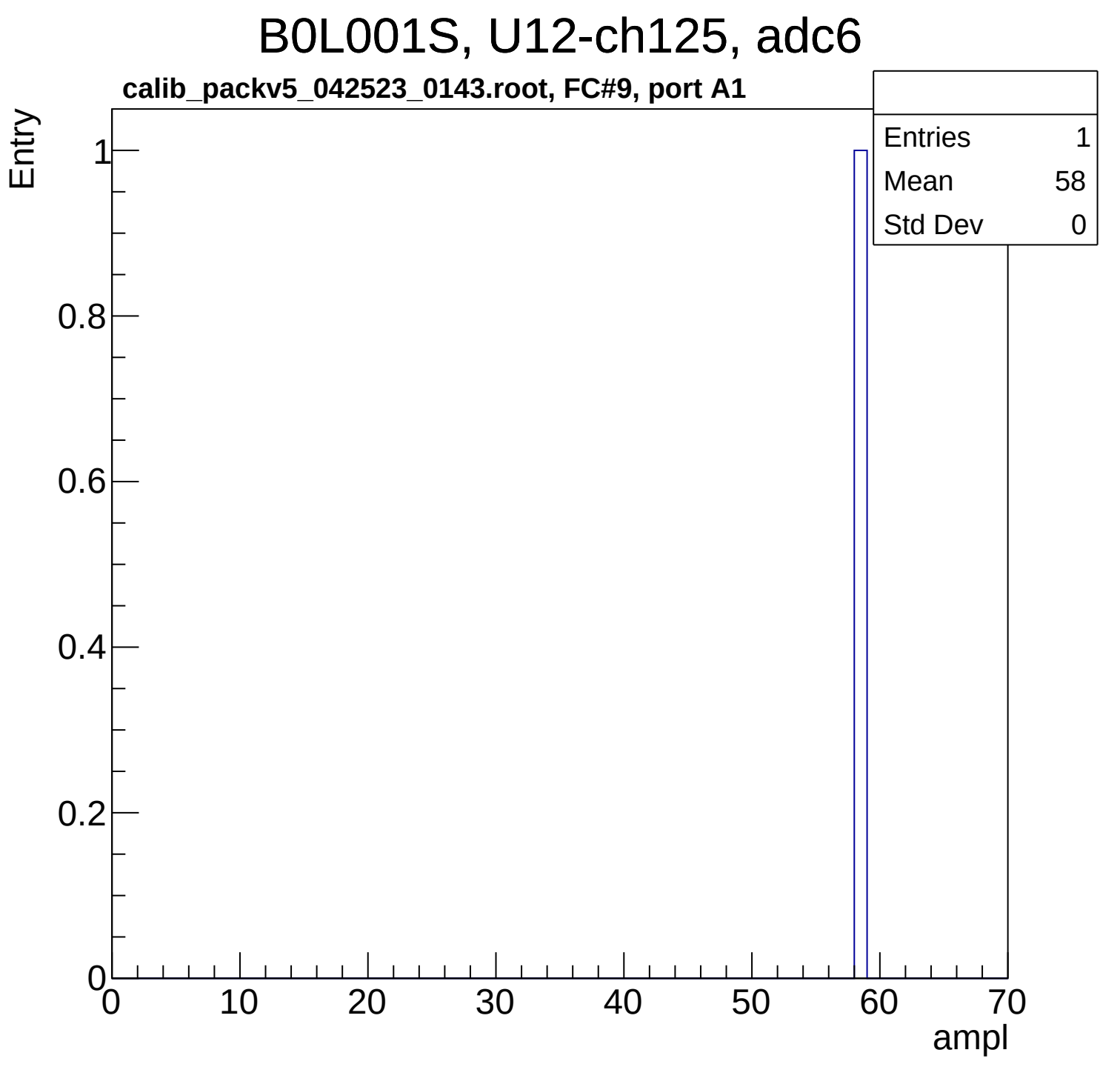
B0L001S, U12-ch125, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 58
Std Dev 0
Entry
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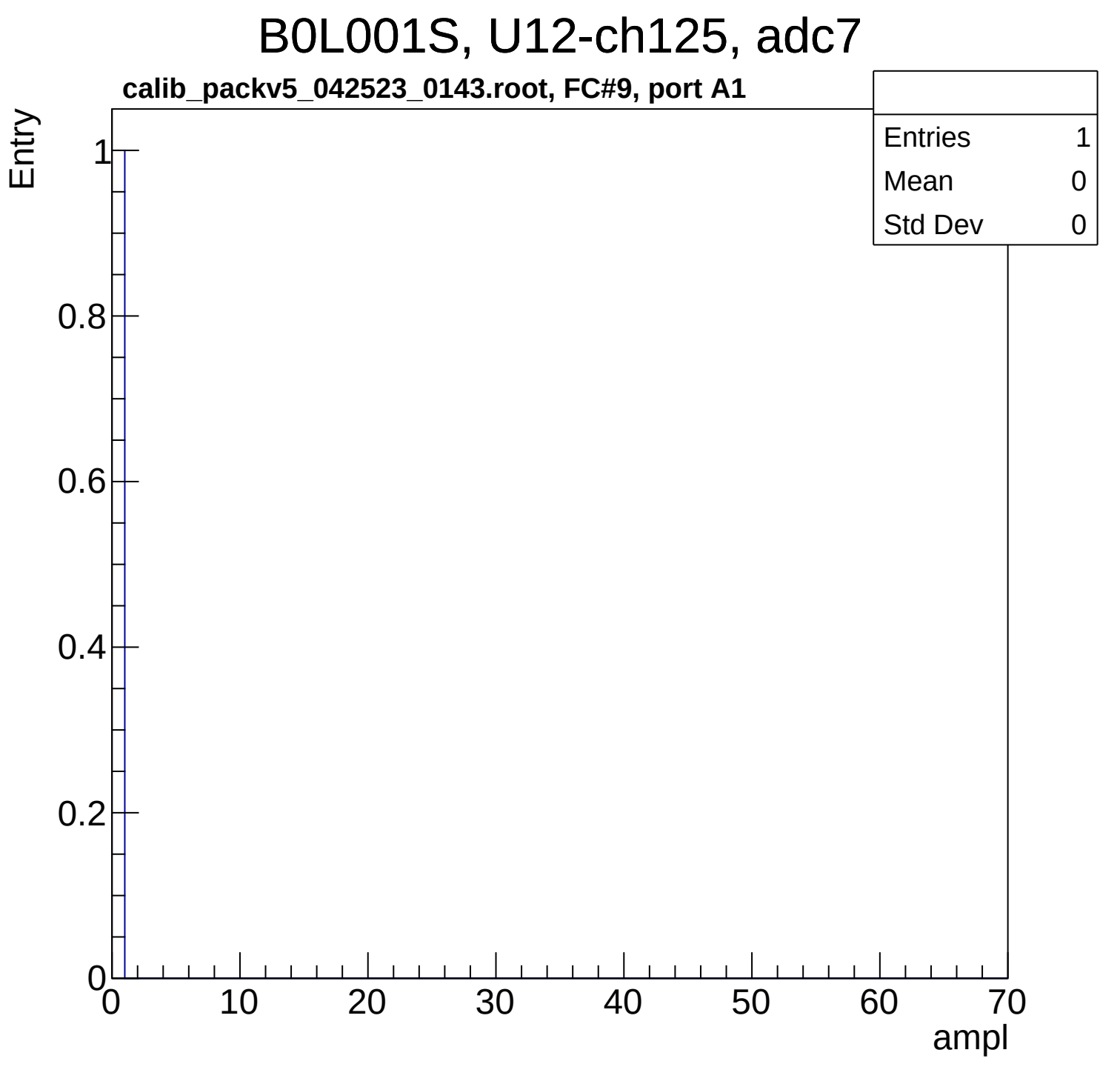
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch125, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 1
Mean 0
Std Dev 0
Entry
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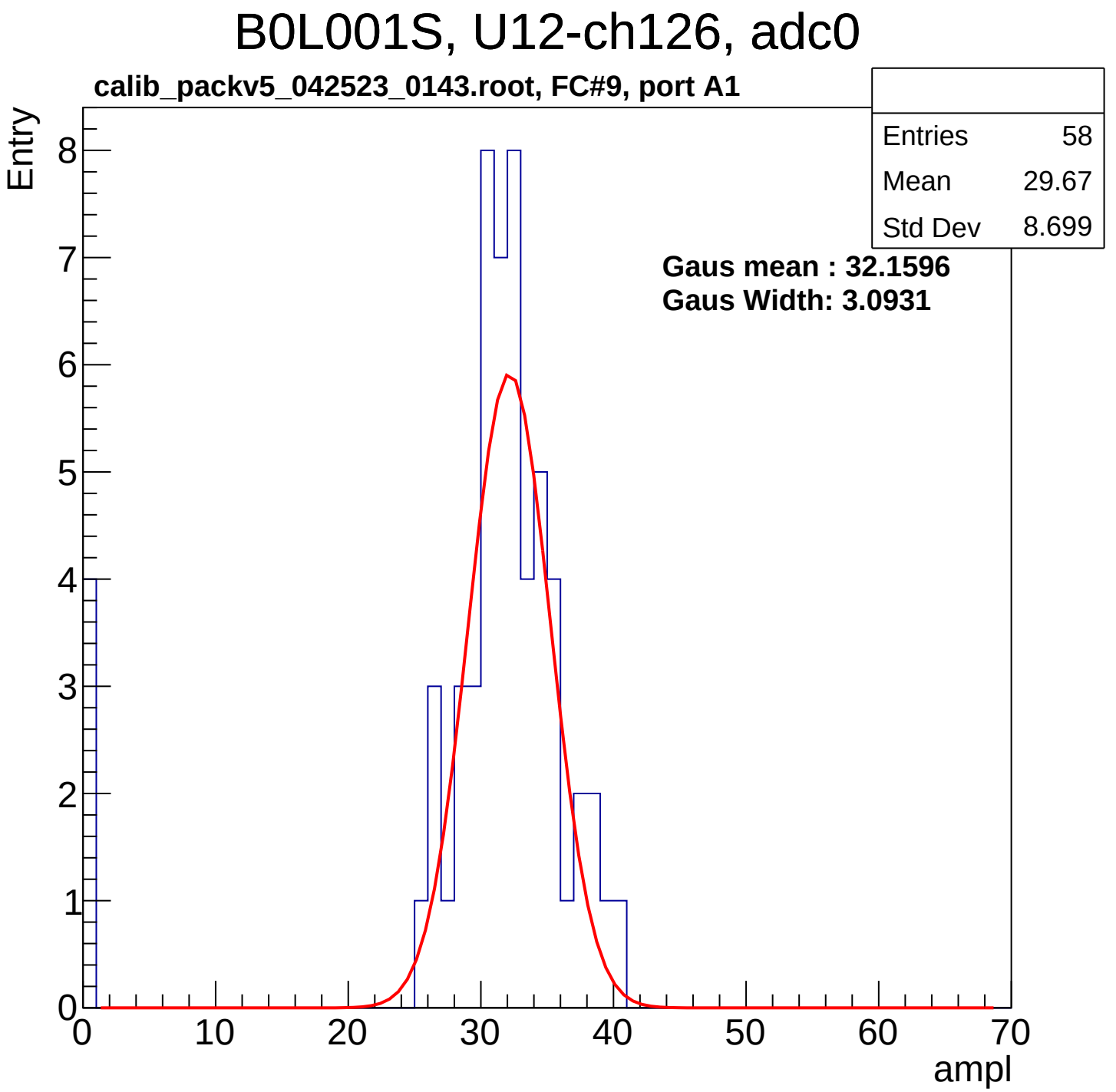
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch126, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 58
Mean 29.67
Std Dev 8.699
Gaus mean : 32.1596
Gaus Width: 3.0931
Entry
ampl
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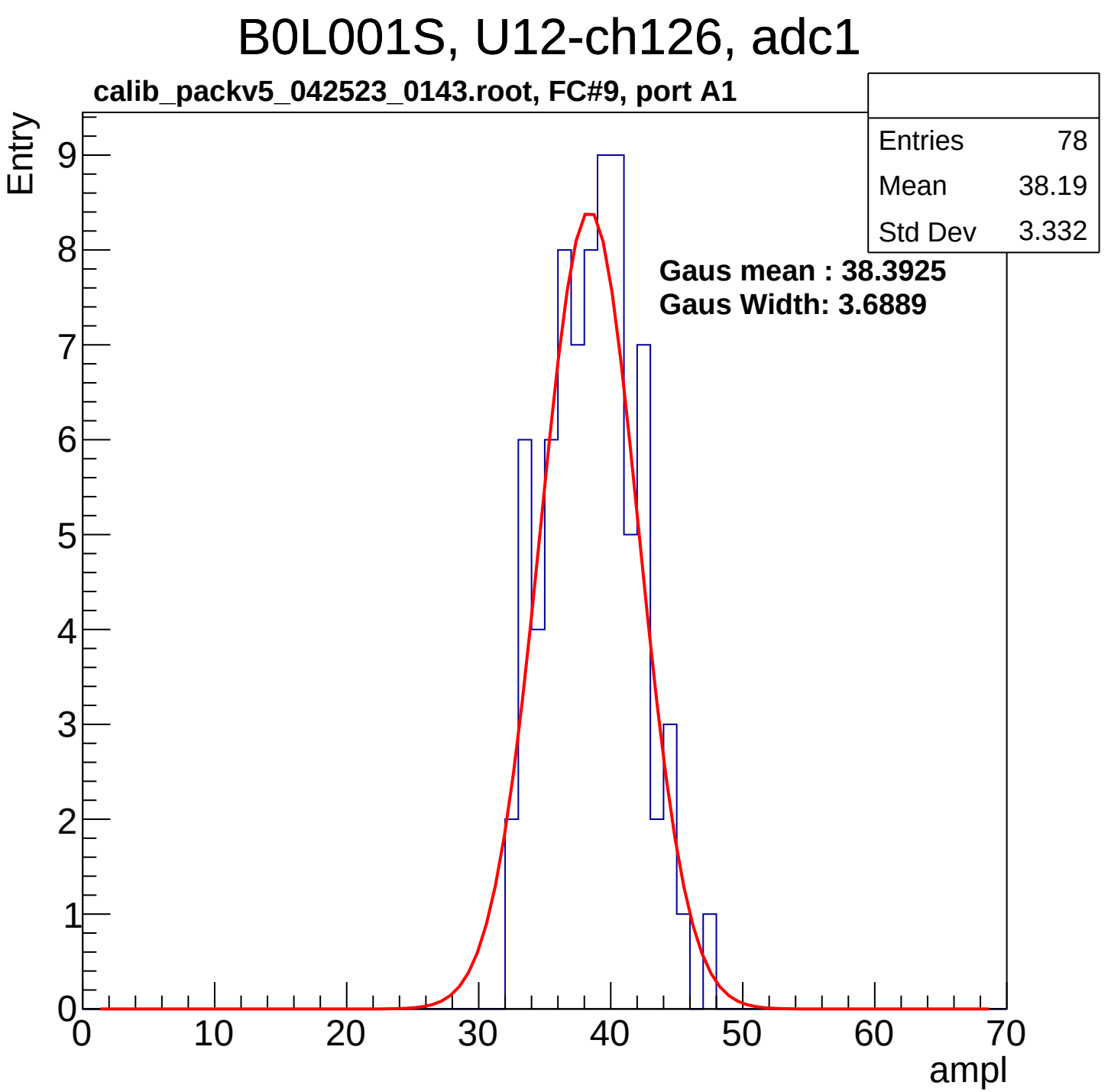
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch126, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 78
Mean 38.19
Std Dev 3.332
Gaus mean : 38.3925
Gaus Width: 3.6889
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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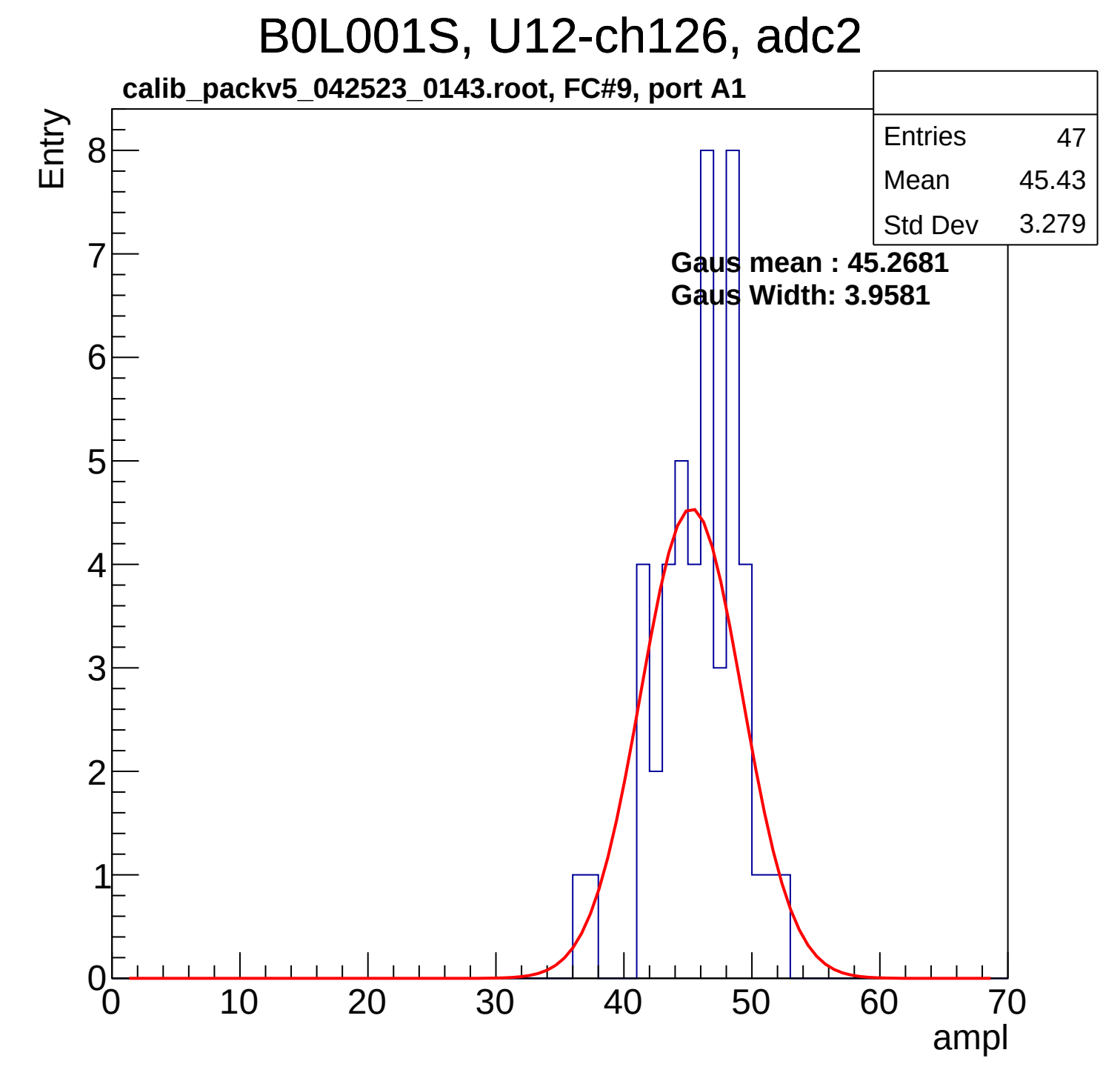
40
50
60
70


B0L001S, U12-ch126, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 47
Mean 45.43
Std Dev 3.279
Gaus mean : 45.2681
Gaus Width: 3.9581
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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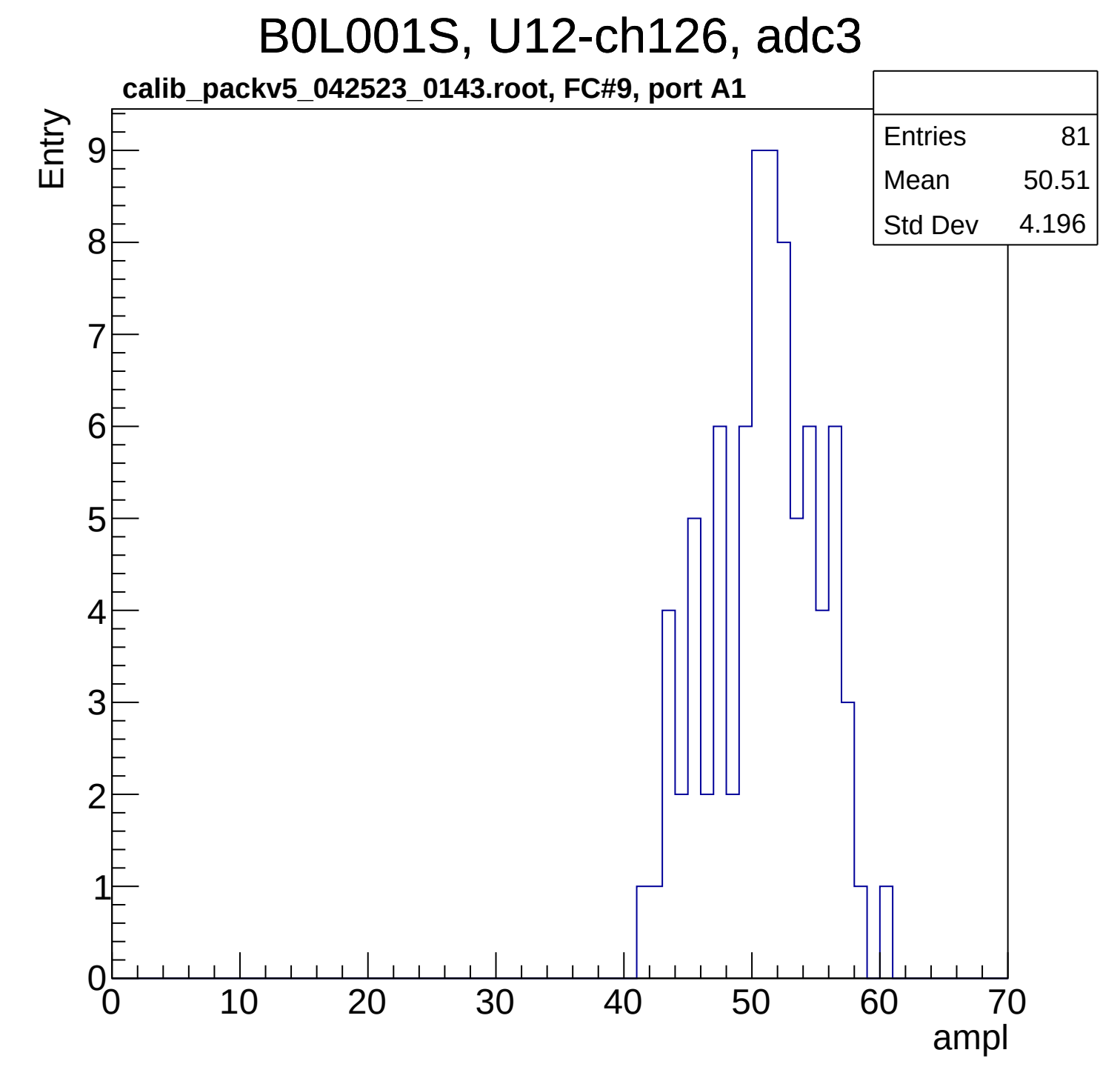
B0L001S, U12-ch126, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 81
Mean 50.51
Std Dev 4.196
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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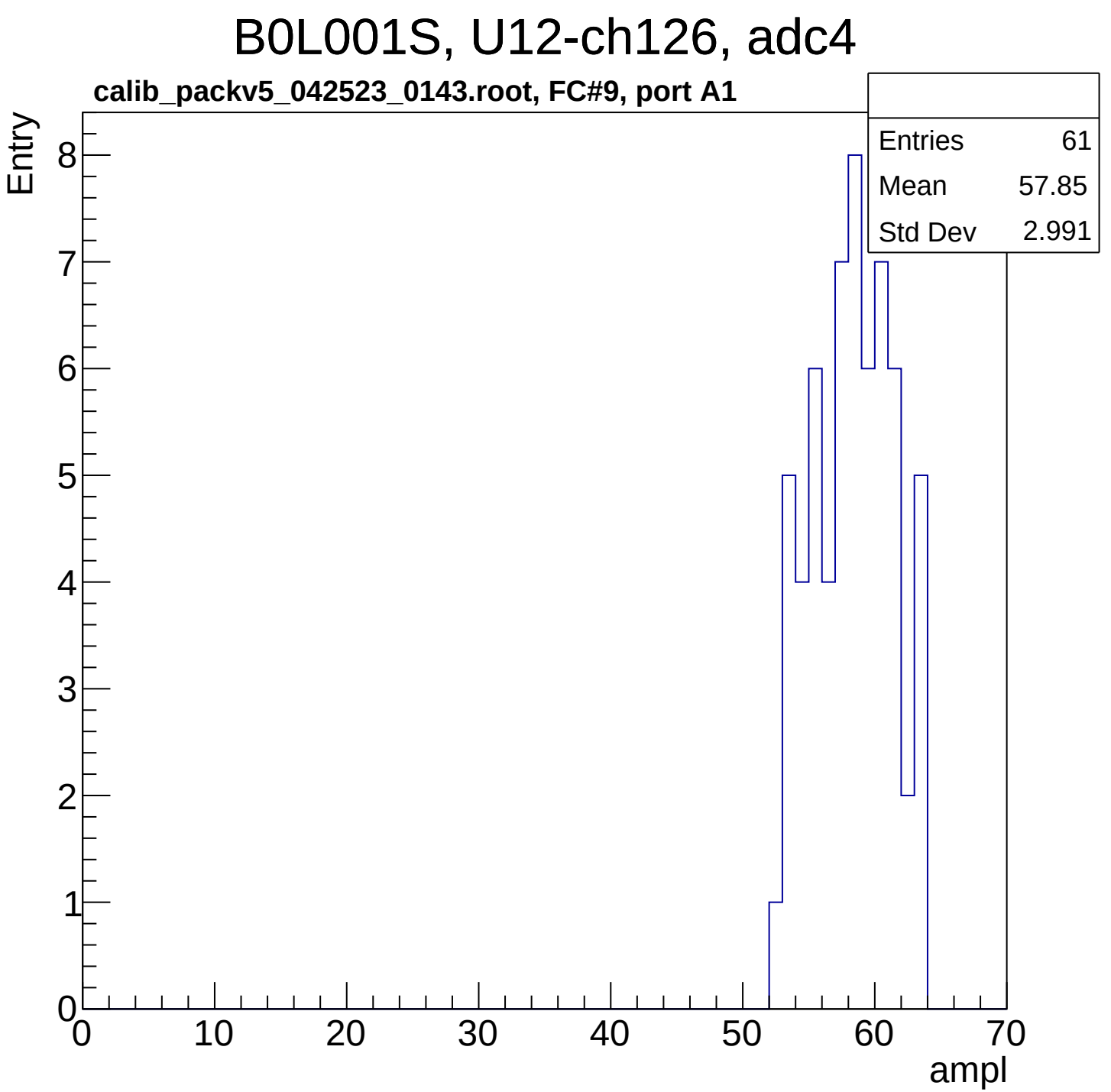
B0L001S, U12-ch126, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 61
Mean 57.85
Std Dev 2.991
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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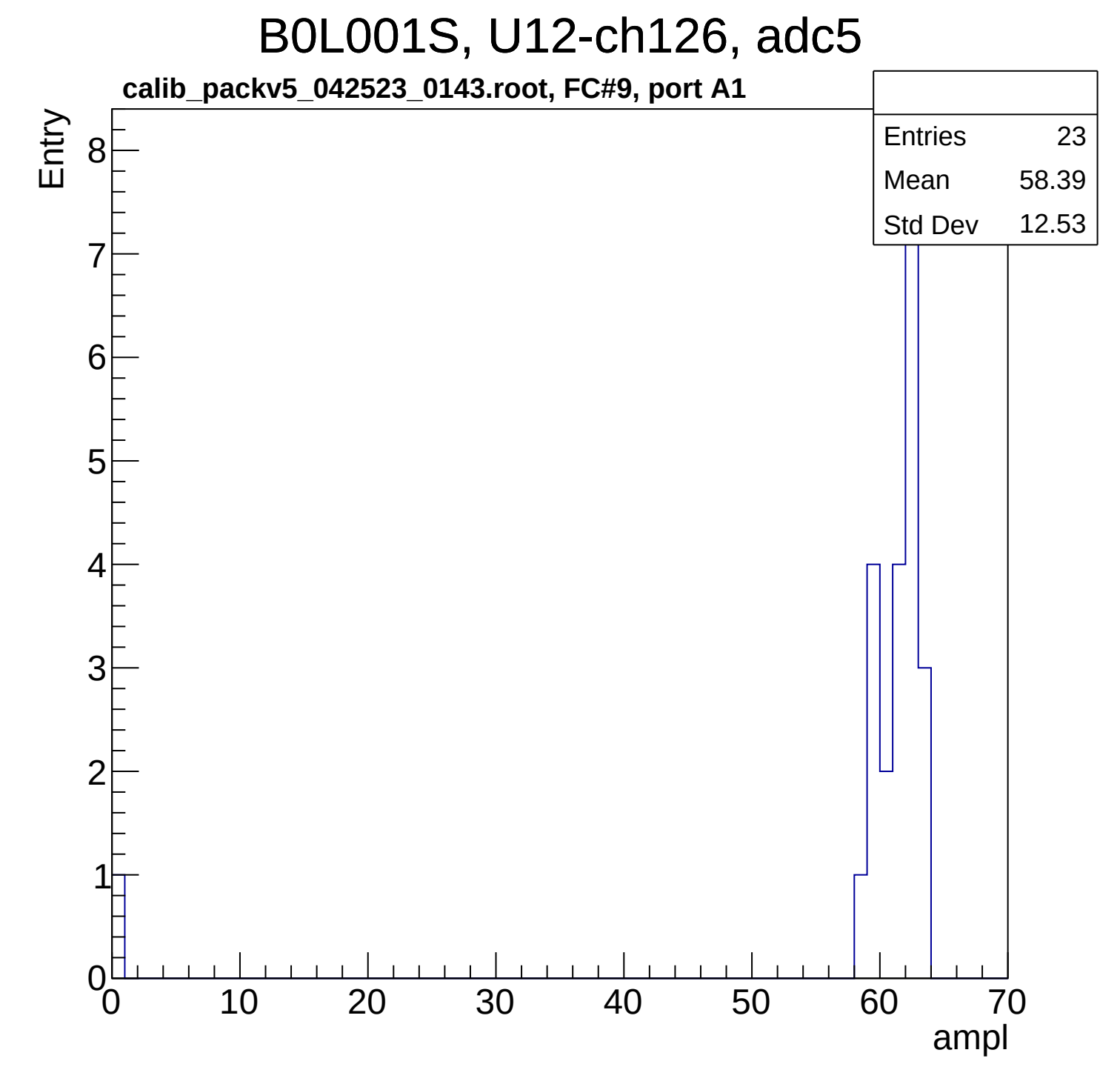
B0L001S, U12-ch126, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 23
Mean 58.39
Std Dev 12.53
Entry
ampl
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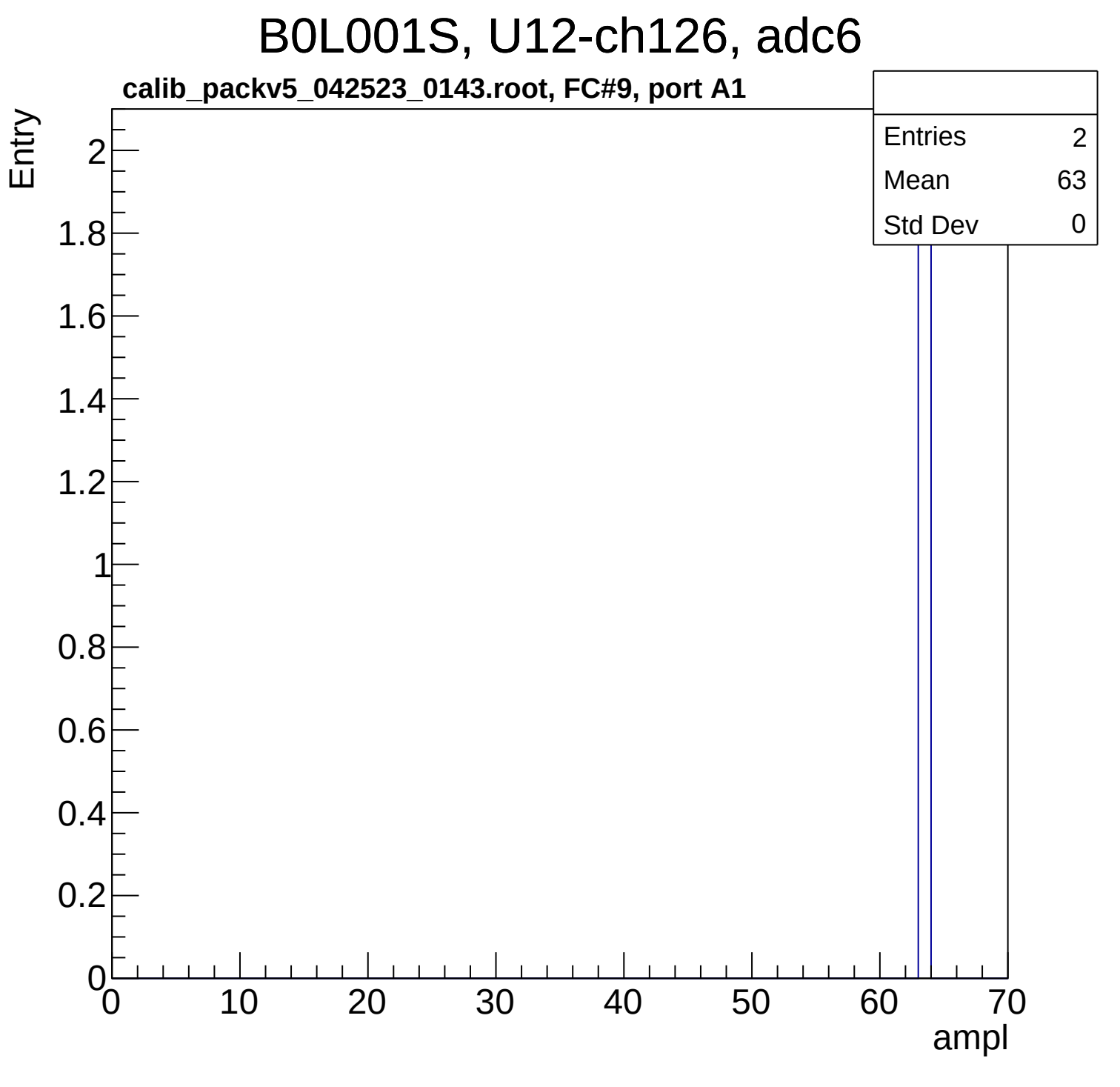
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch126, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
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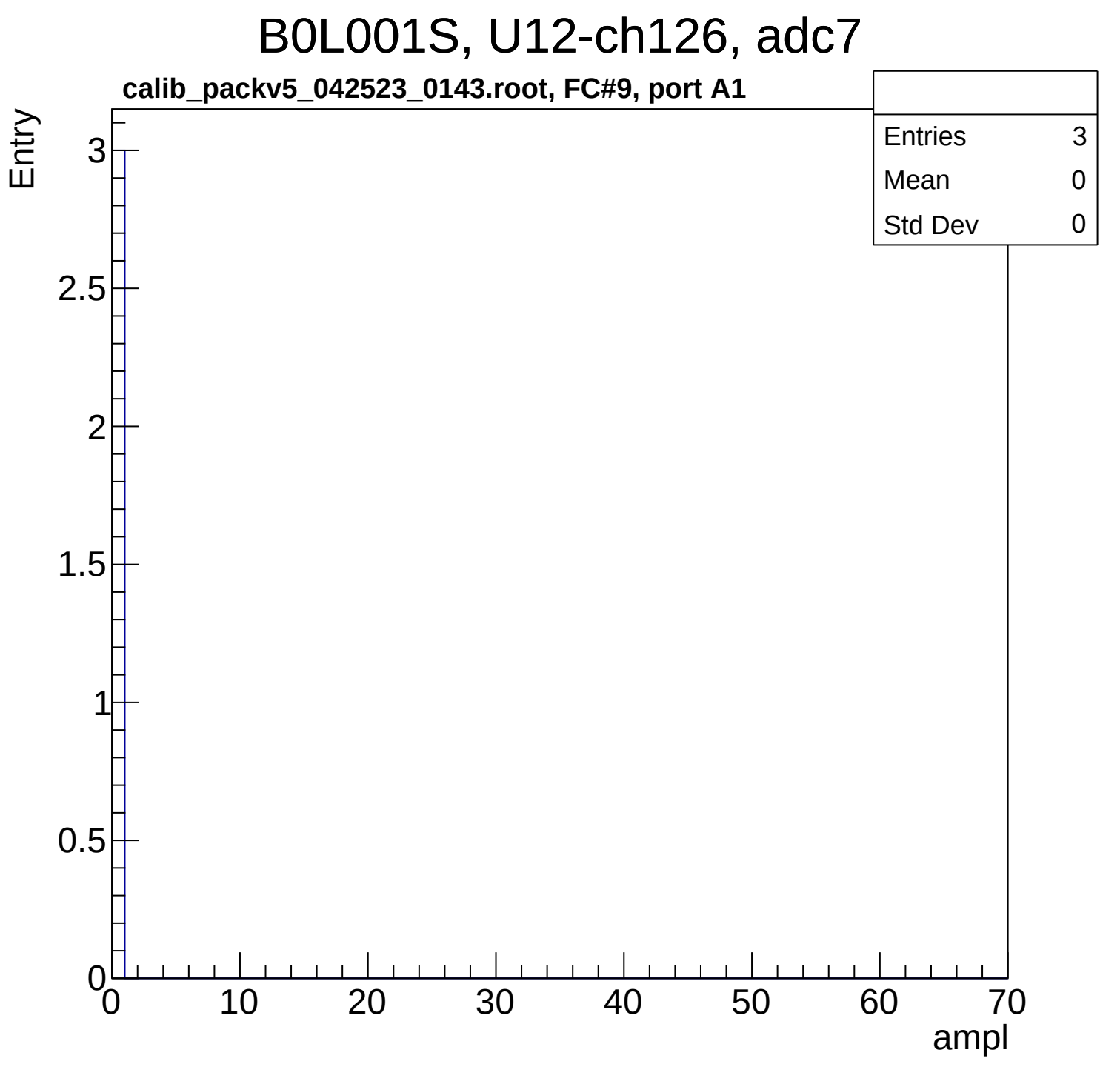
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L001S, U12-ch126, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 3
Mean 0
Std Dev 0
Entry
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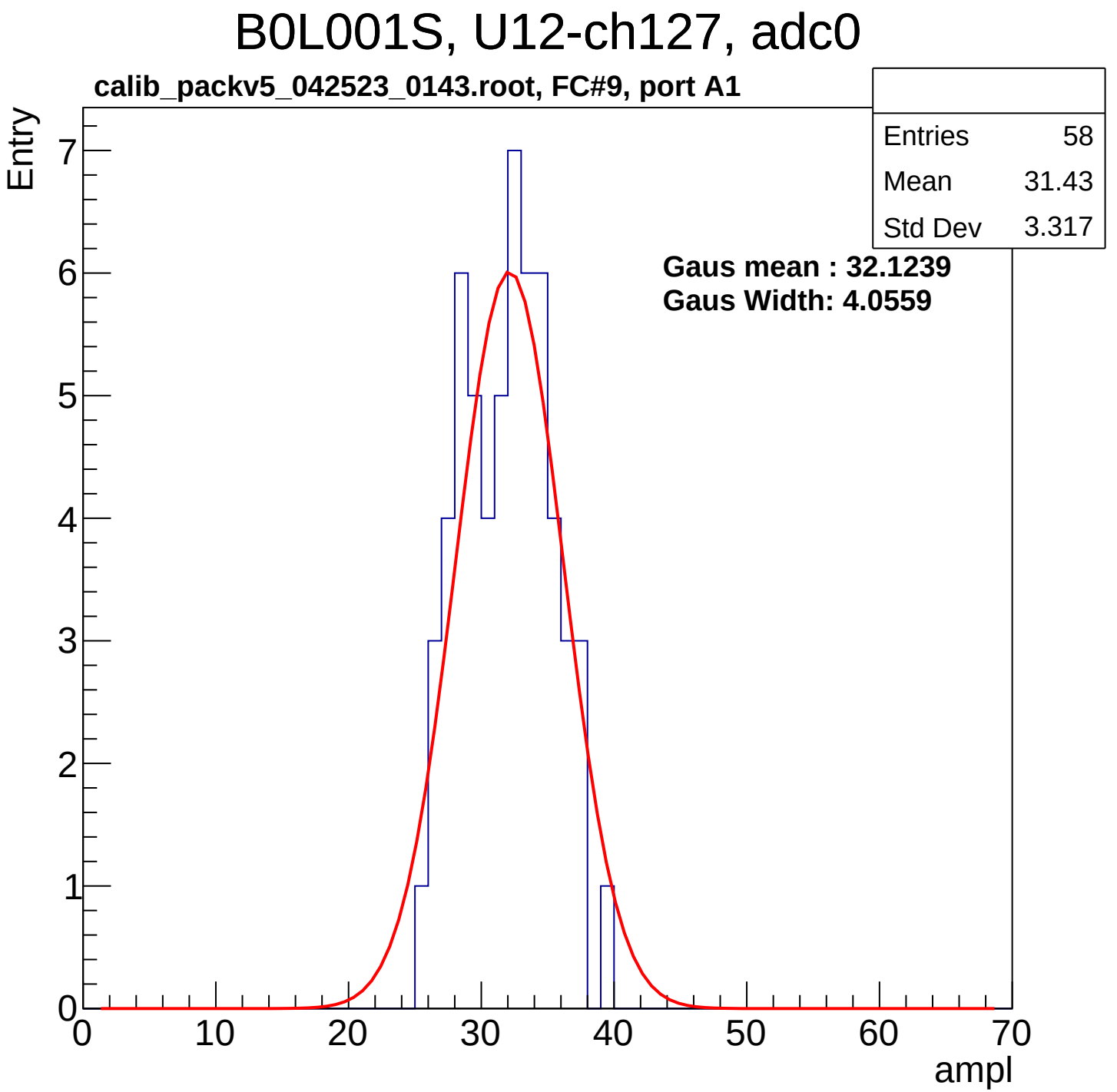
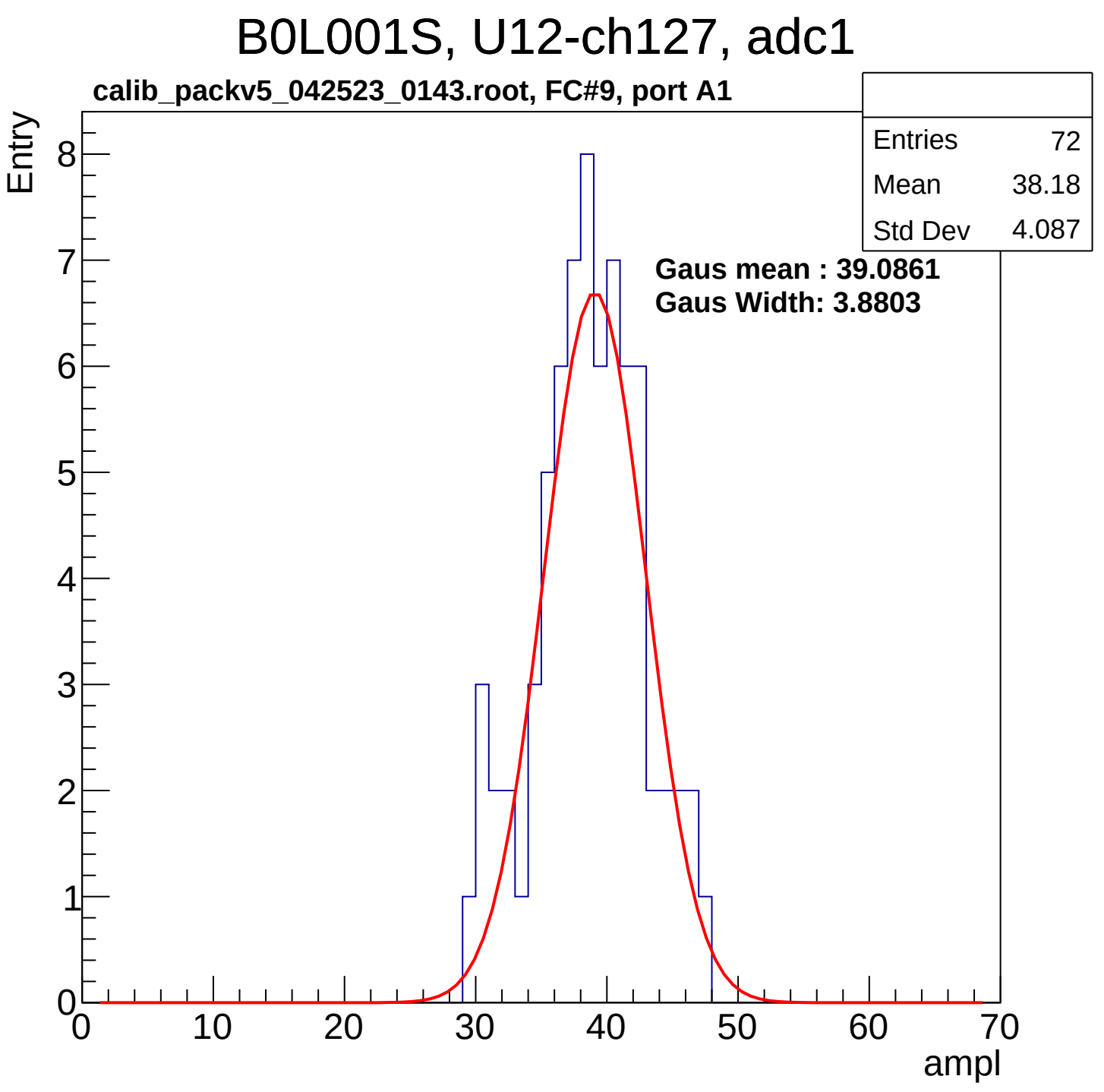
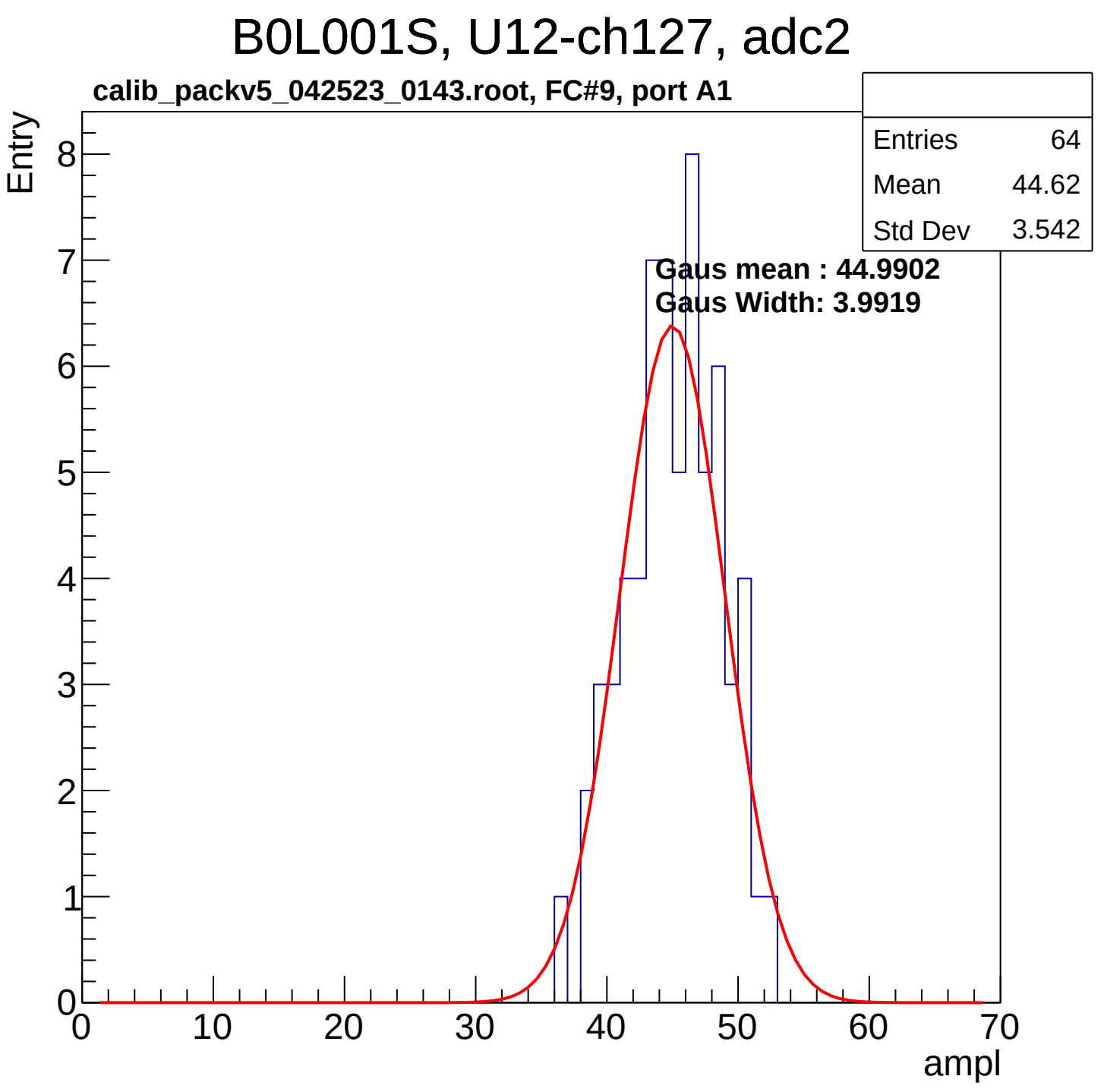
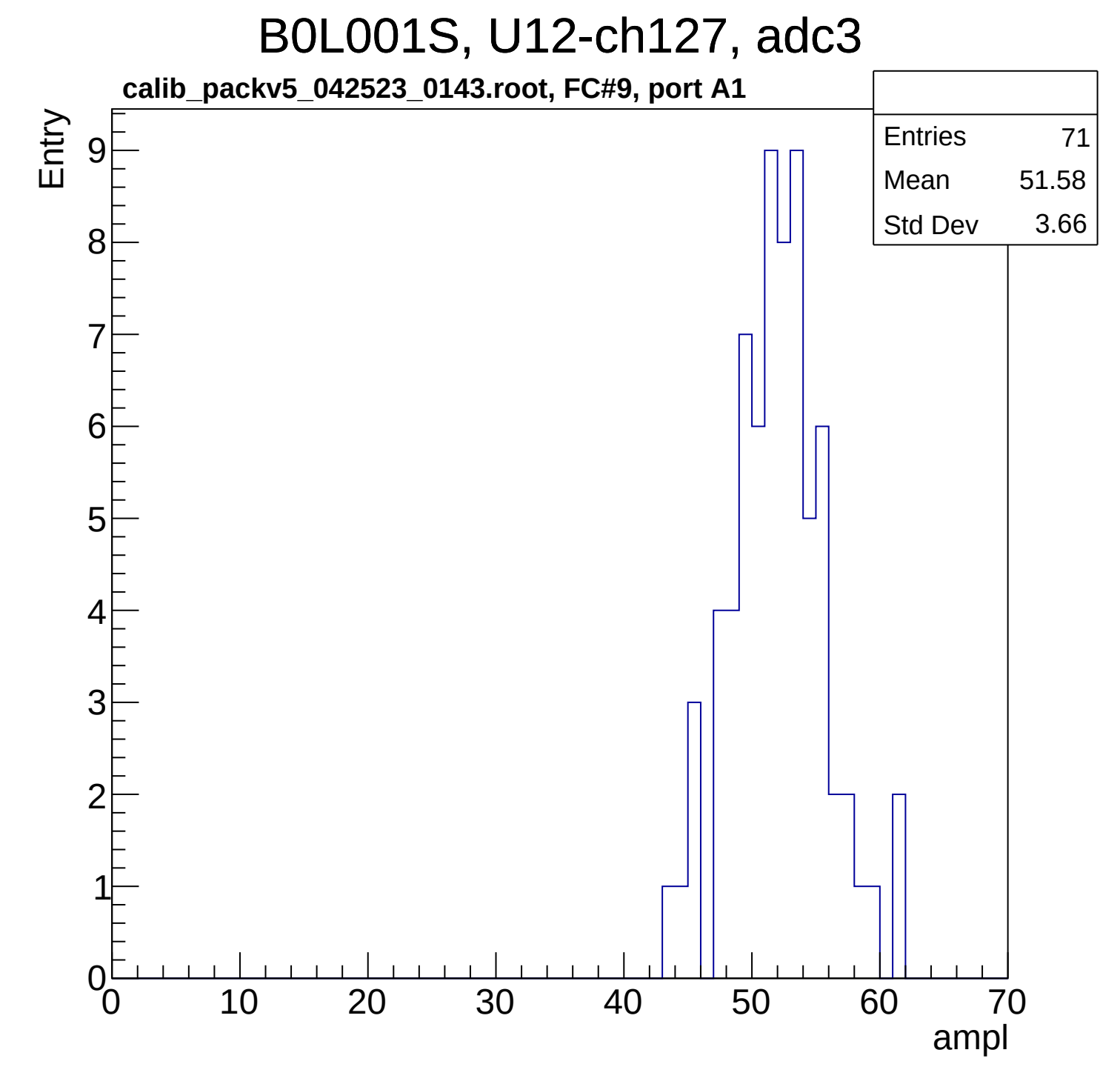
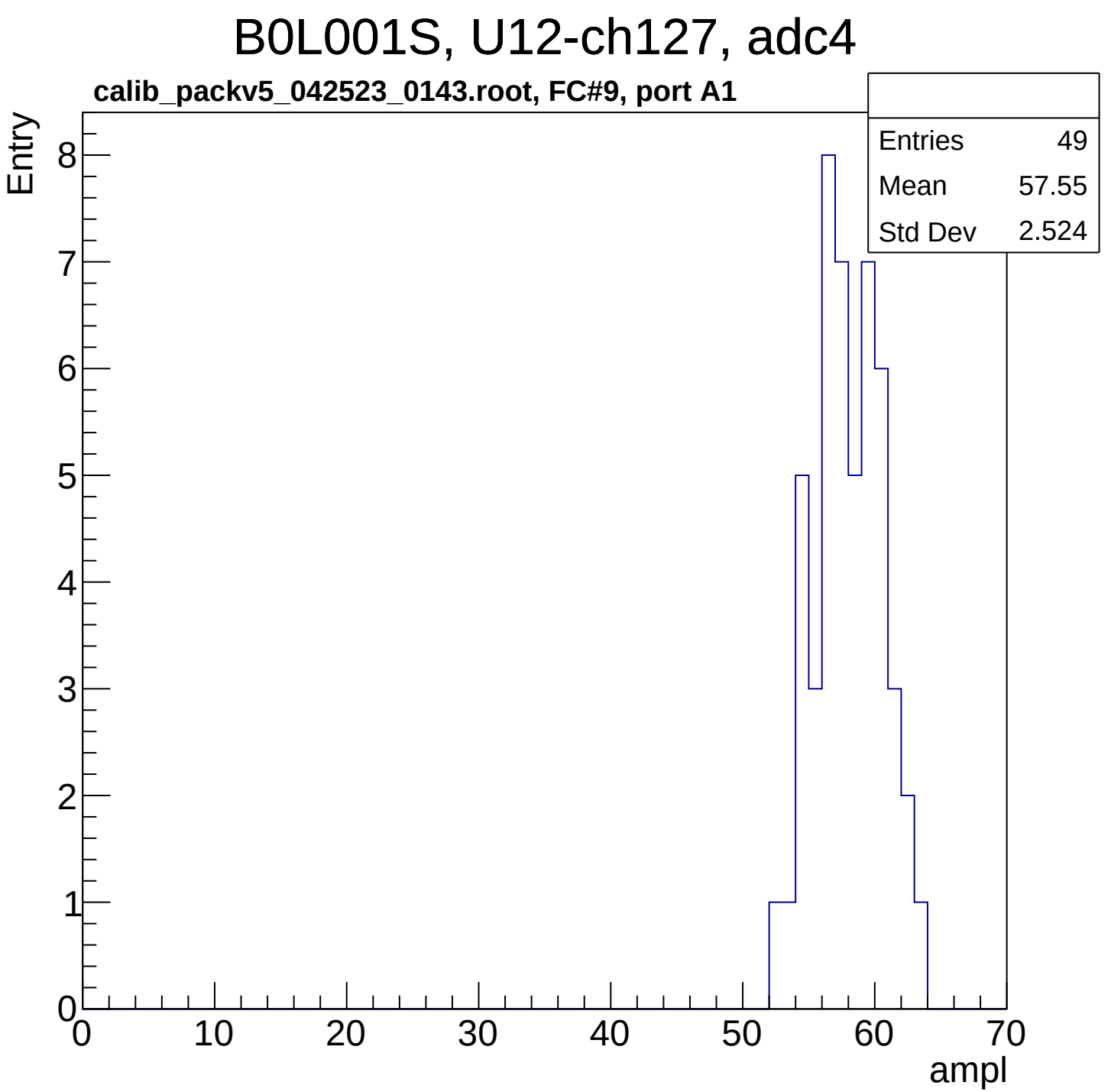
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl

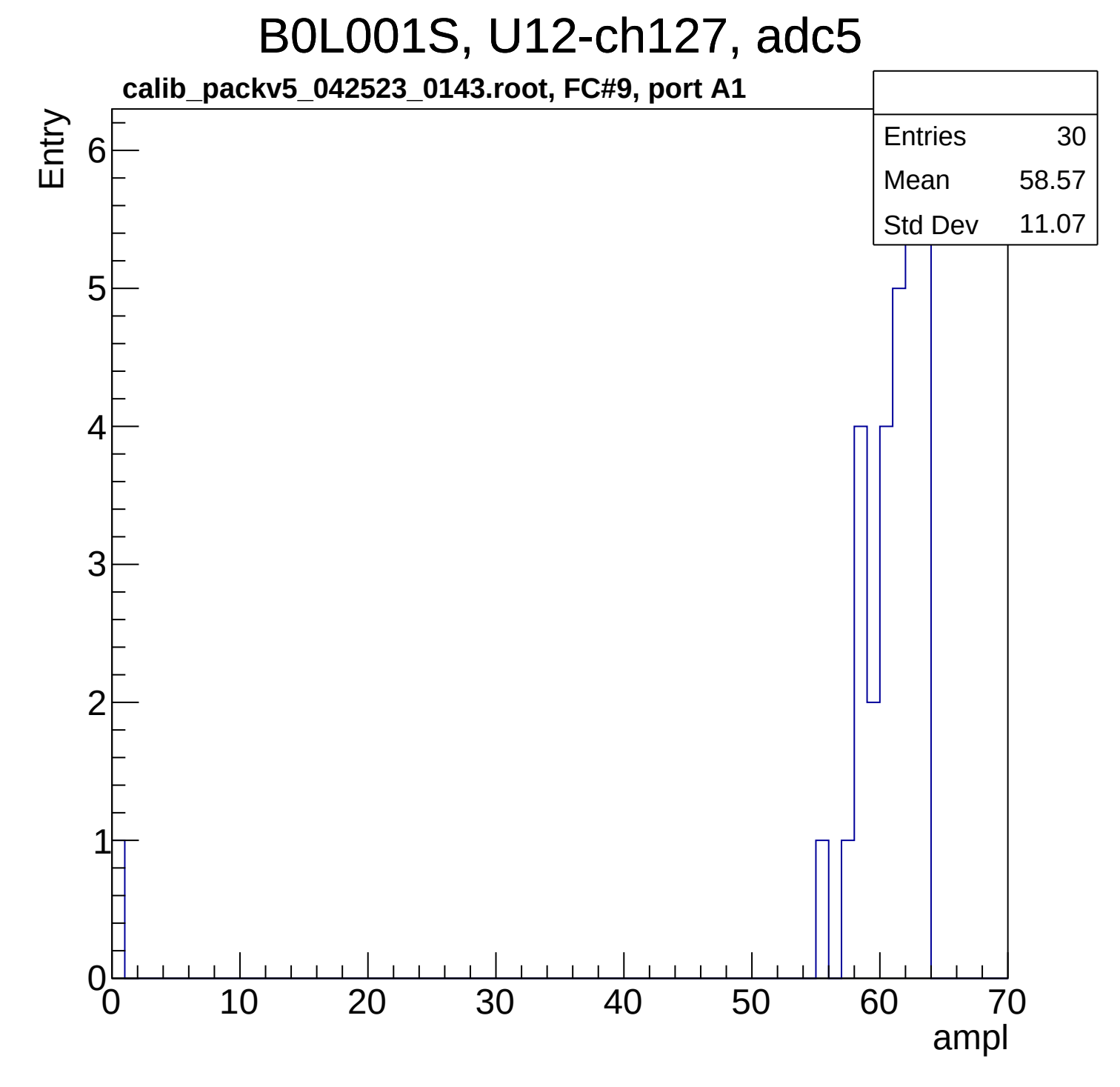

B0L001S, U12-ch127, adc0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 58
Mean 31.43
Std Dev 3.317
Gaus mean : 32.1239
Gaus Width: 4.0559
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

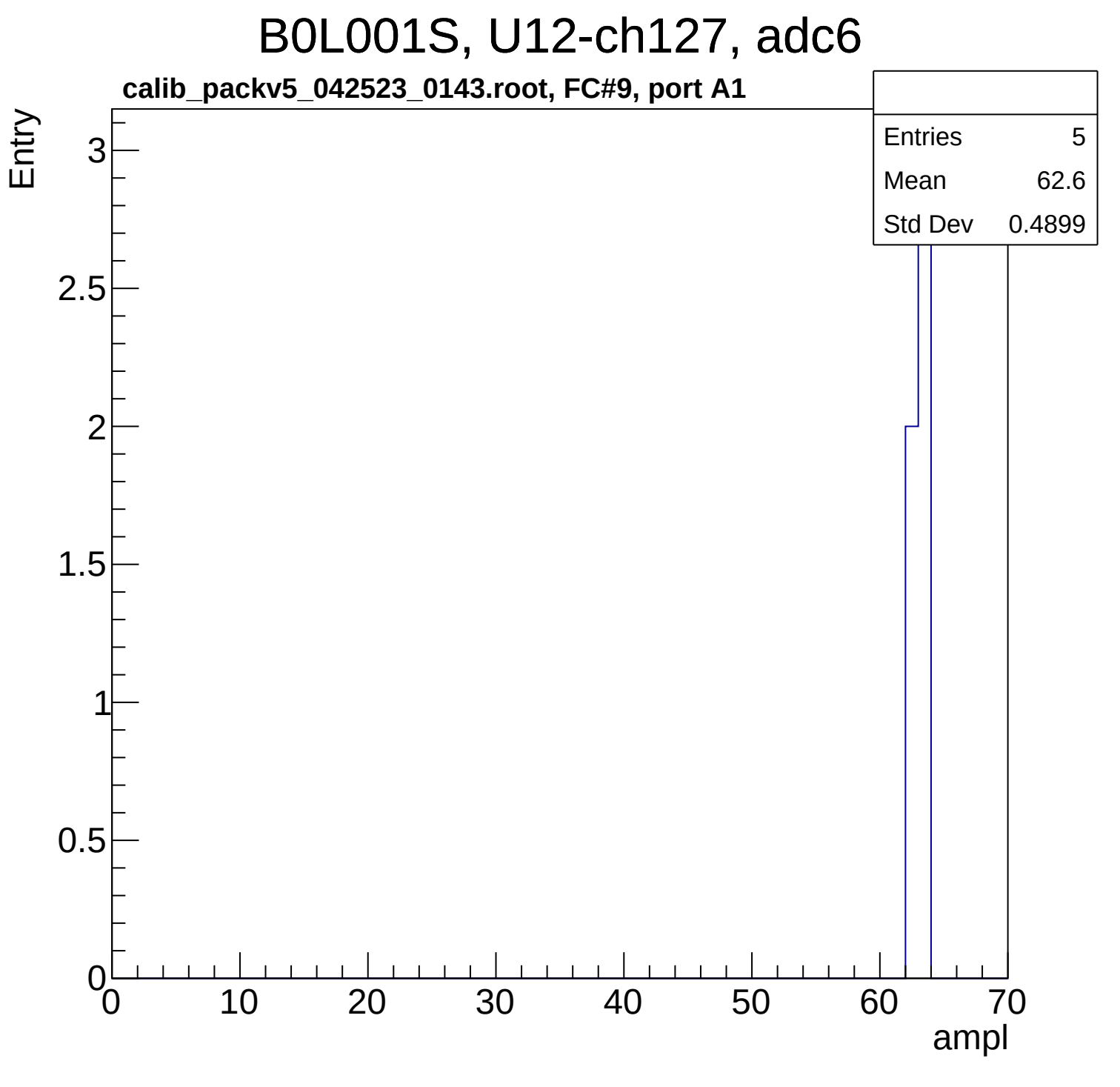

B0L001S, U12-ch127, adc1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 72
Mean 38.18
Std Dev 4.087
Gaus mean : 39.0861
Gaus Width: 3.8803
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

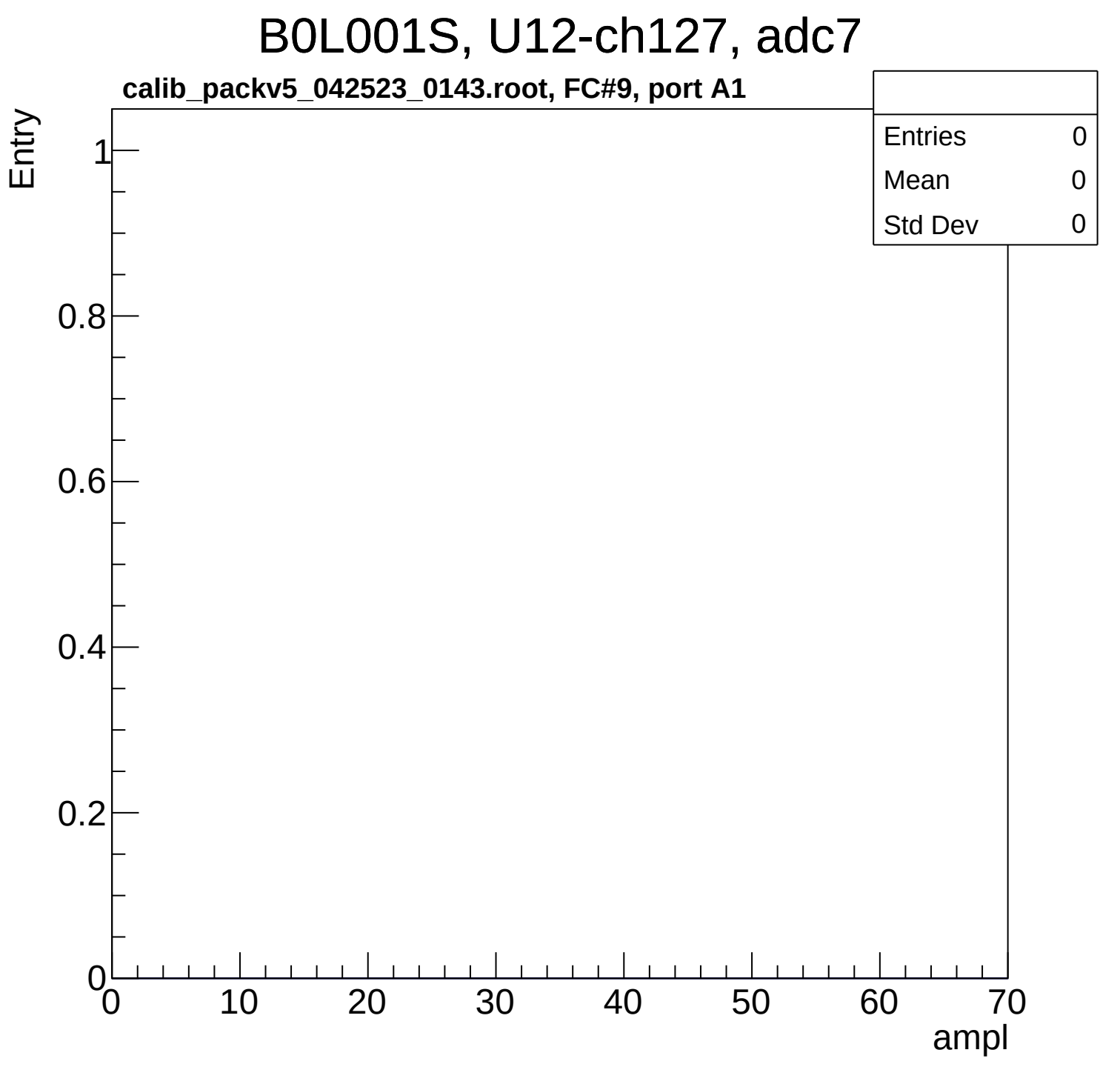

B0L001S, U12-ch127, adc2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 64
Mean 44.62
Std Dev 3.542
Gaus mean : 44.9902
Gaus Width: 3.9919
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

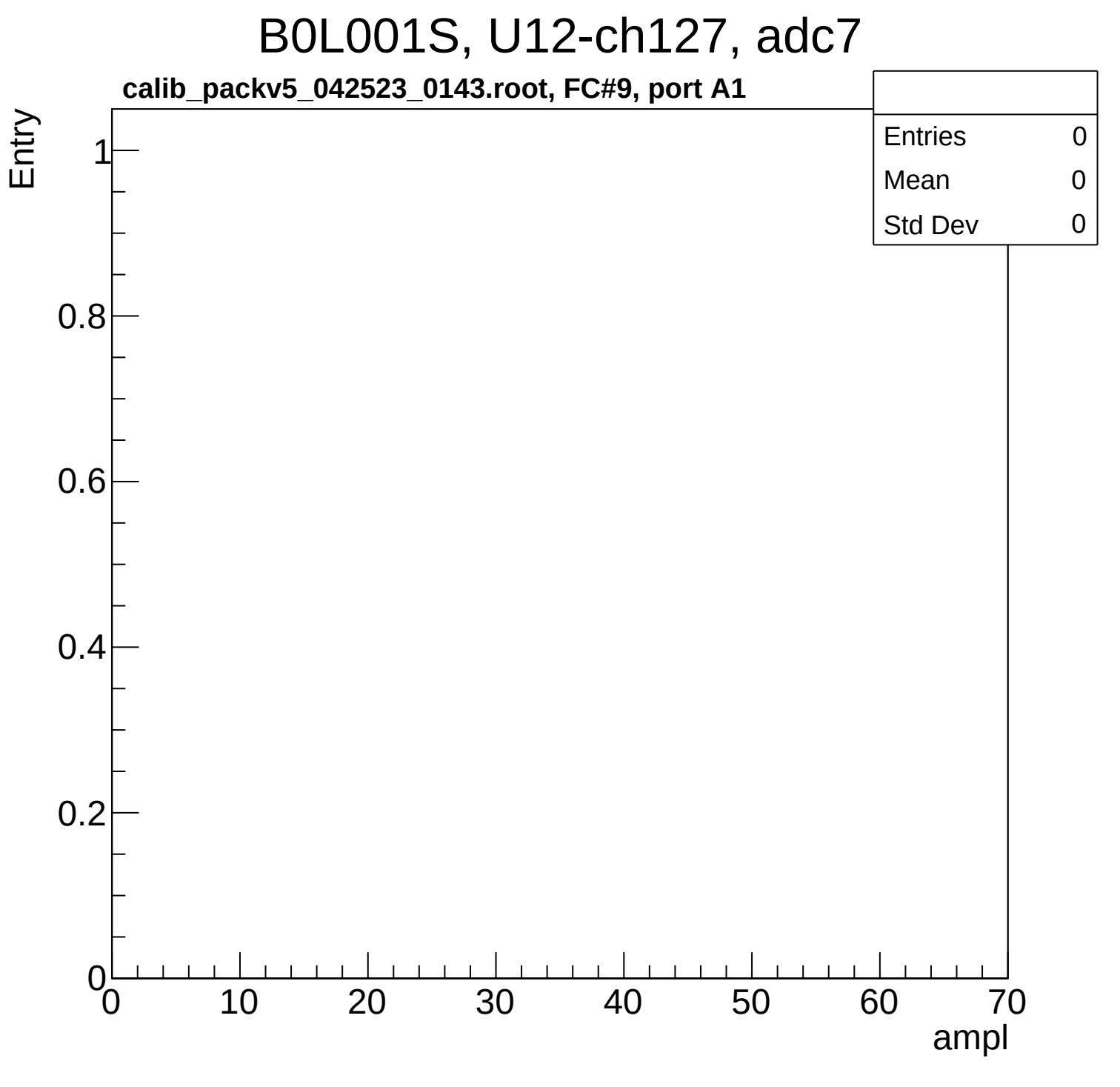

B0L001S, U12-ch127, adc3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 71
Mean 51.58
Std Dev 3.66
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B0L001S, U12-ch127, adc4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 49
Mean 57.55
Std Dev 2.524
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B0L001S, U12-ch127, adc5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 30
Mean 58.57
Std Dev 11.07
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch127, adc6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 5
Mean 62.6
Std Dev 0.4899
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B0L001S, U12-ch127, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L001S, U12-ch127, adc7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl