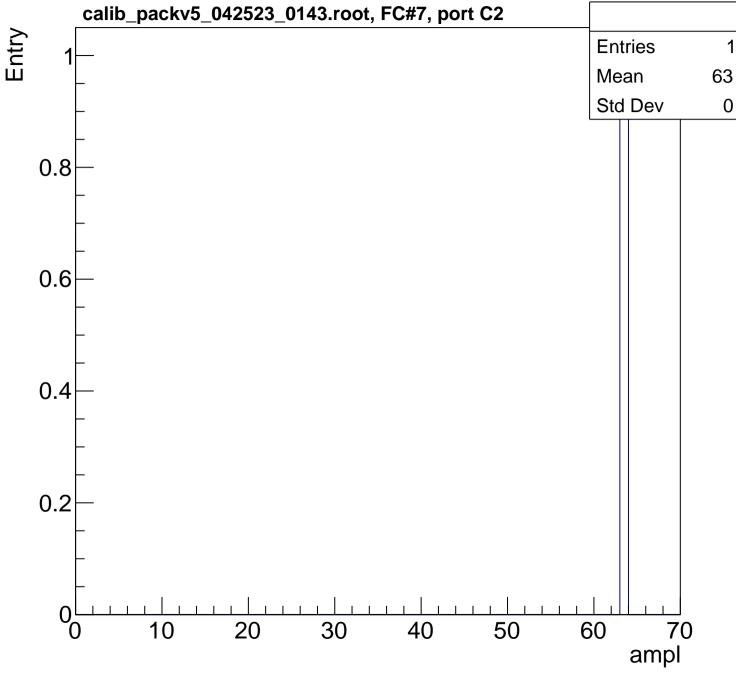
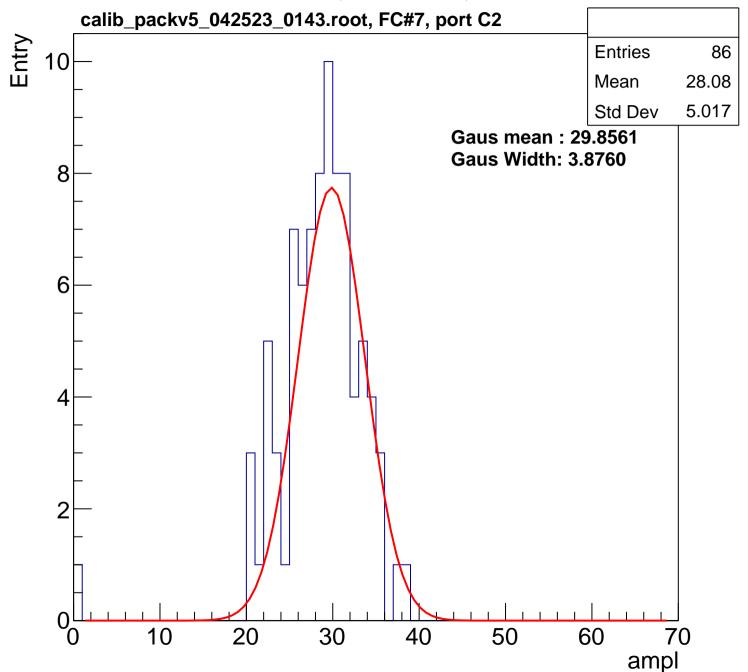
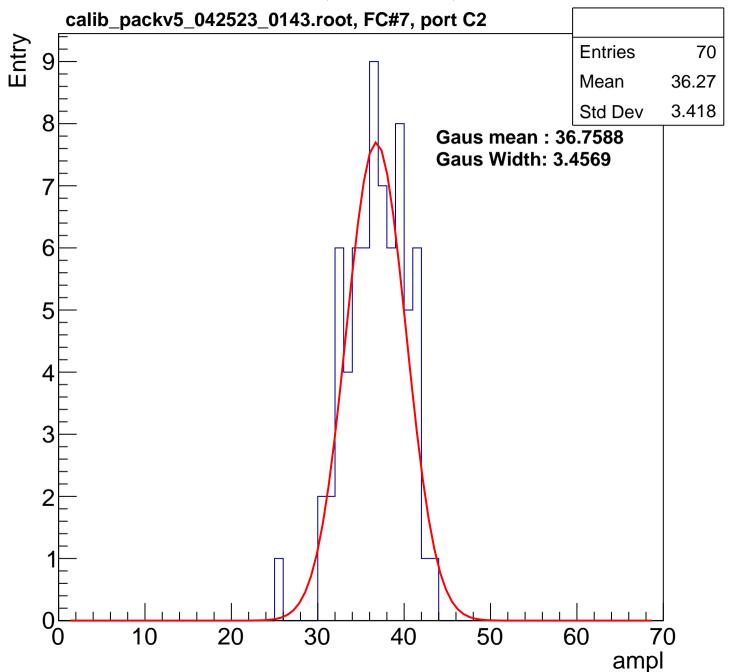
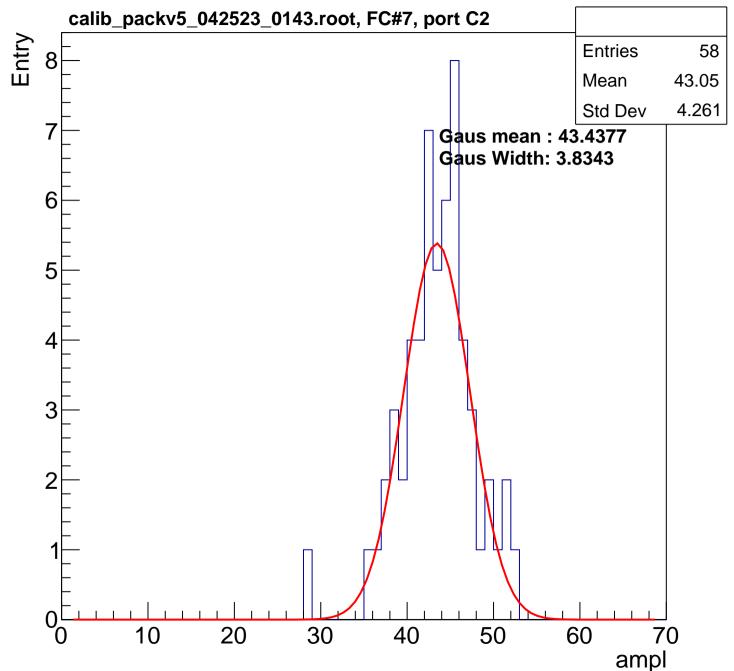


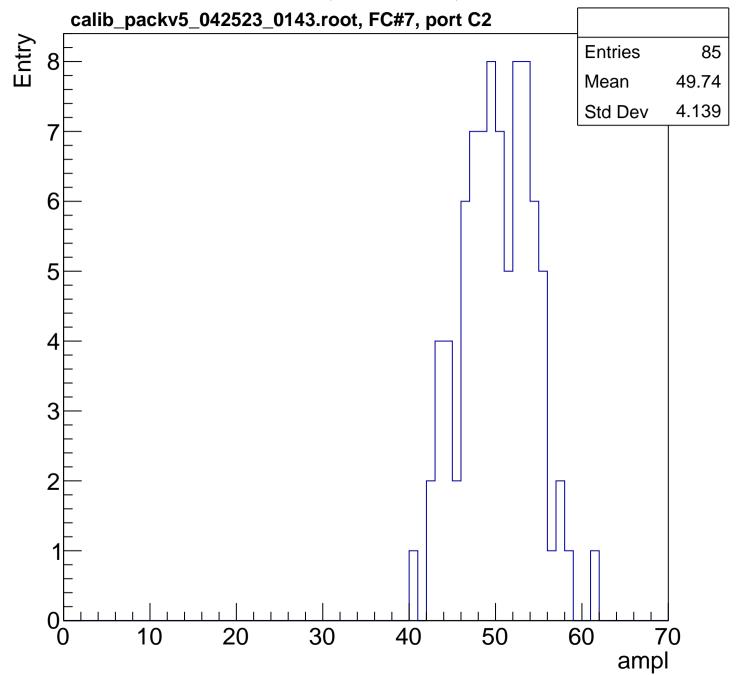
0

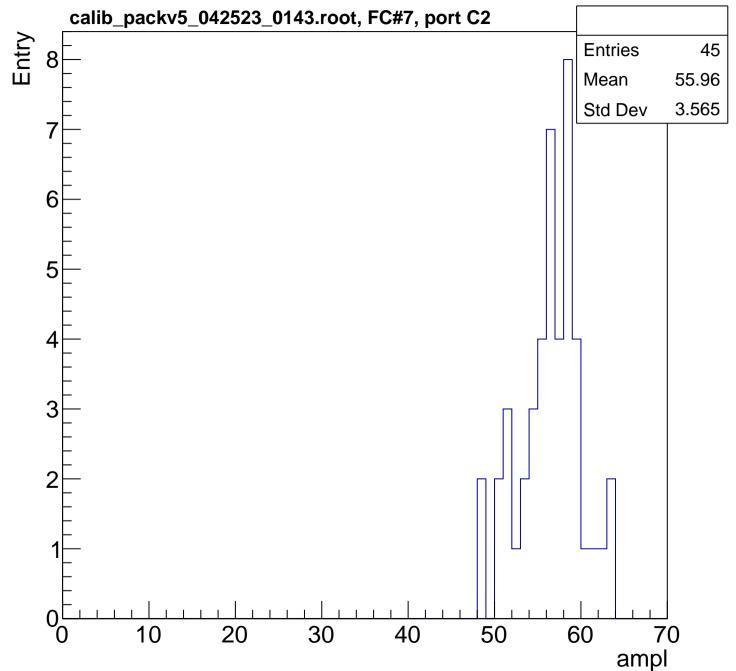


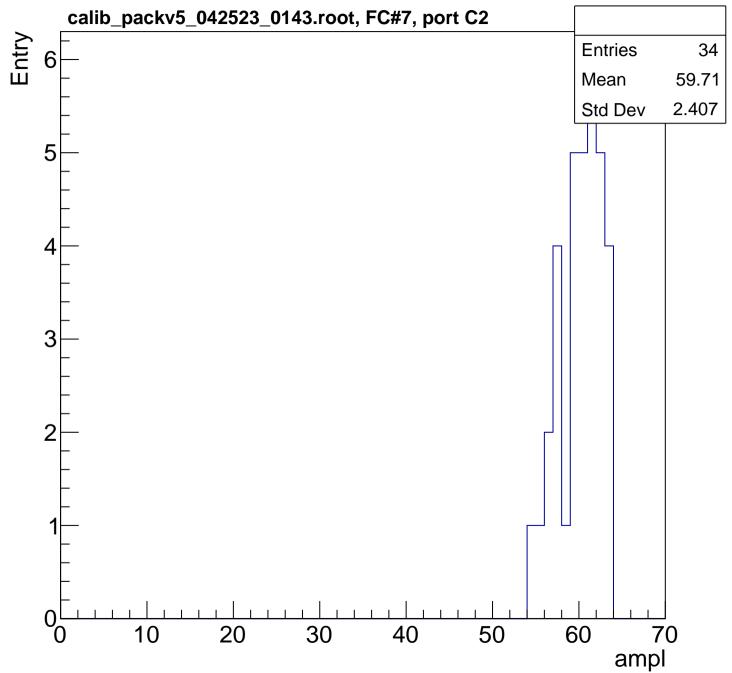


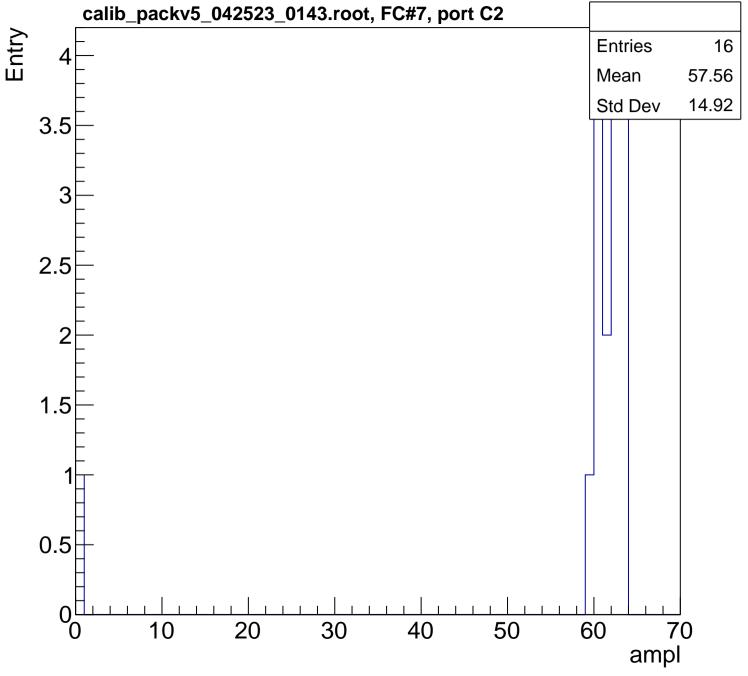


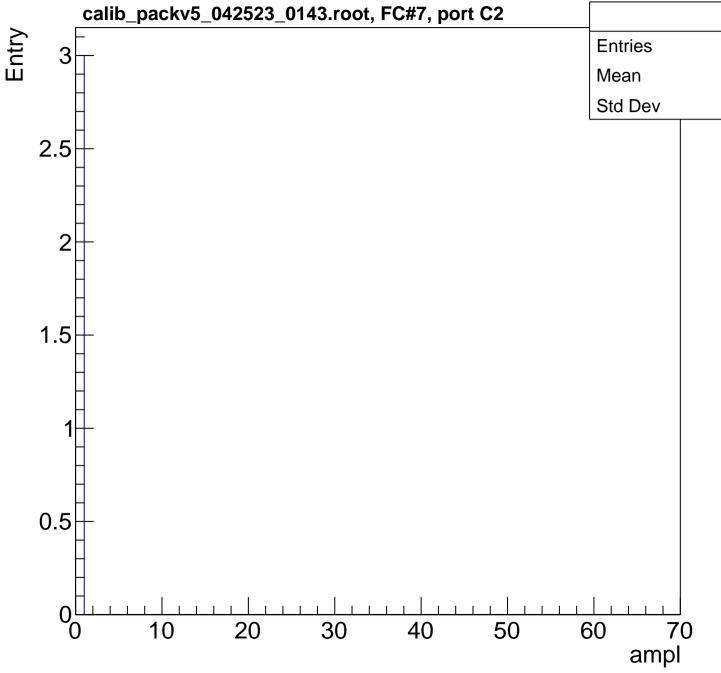


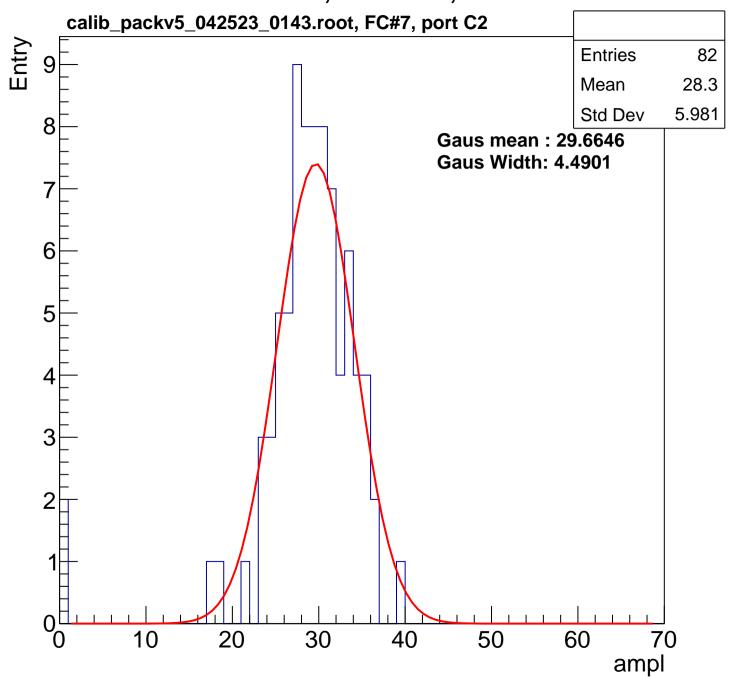


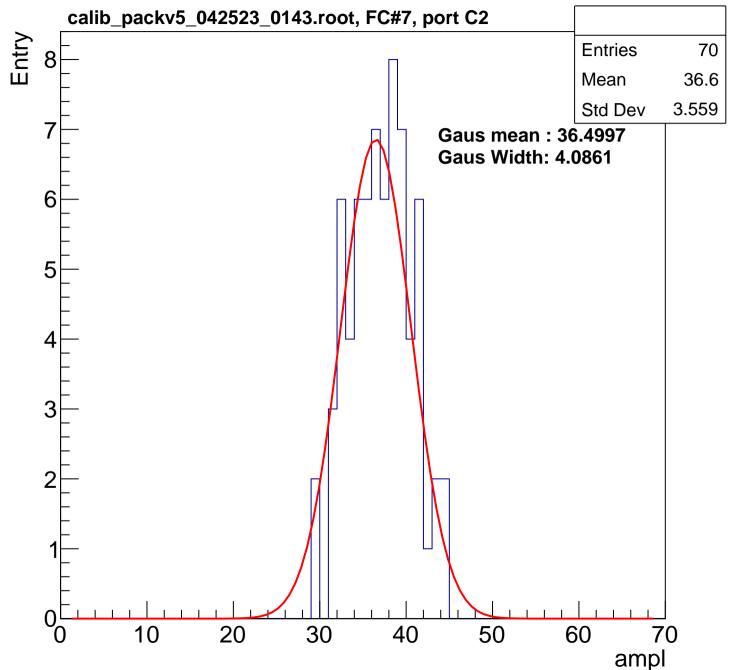


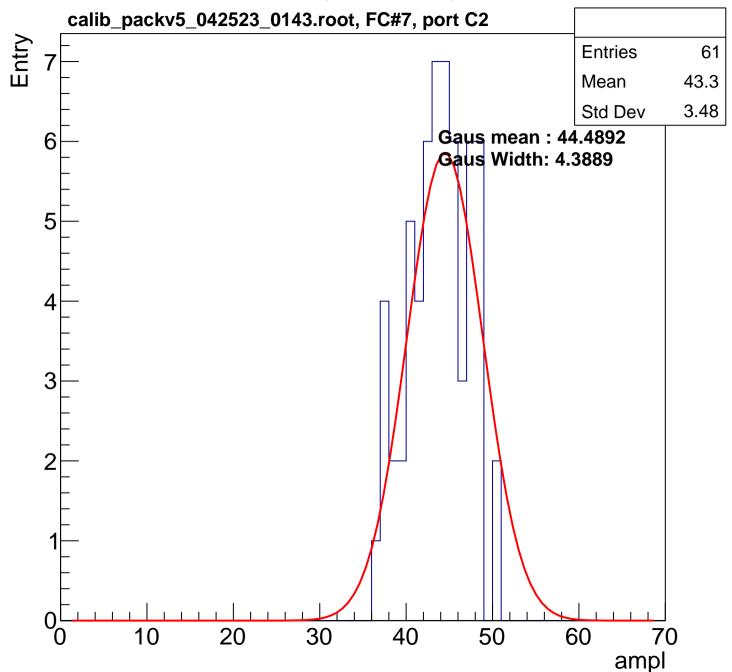


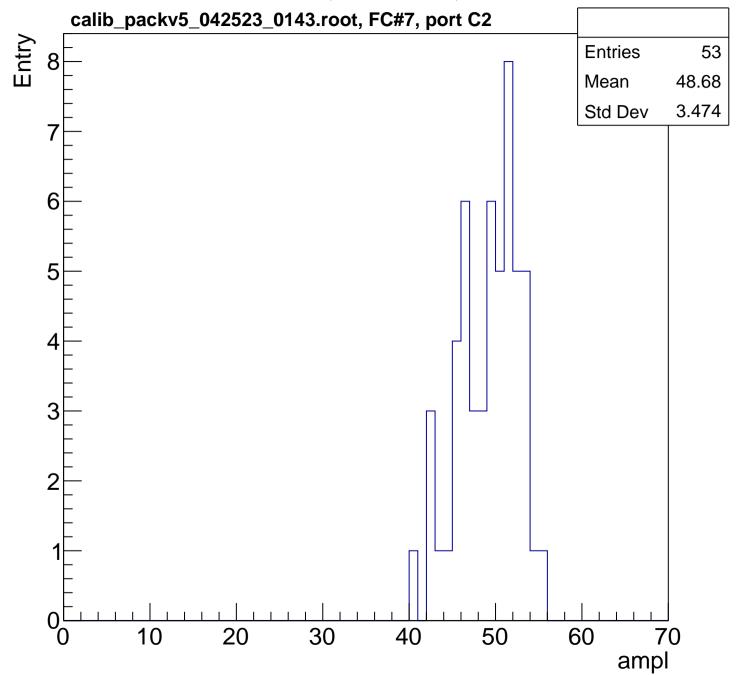


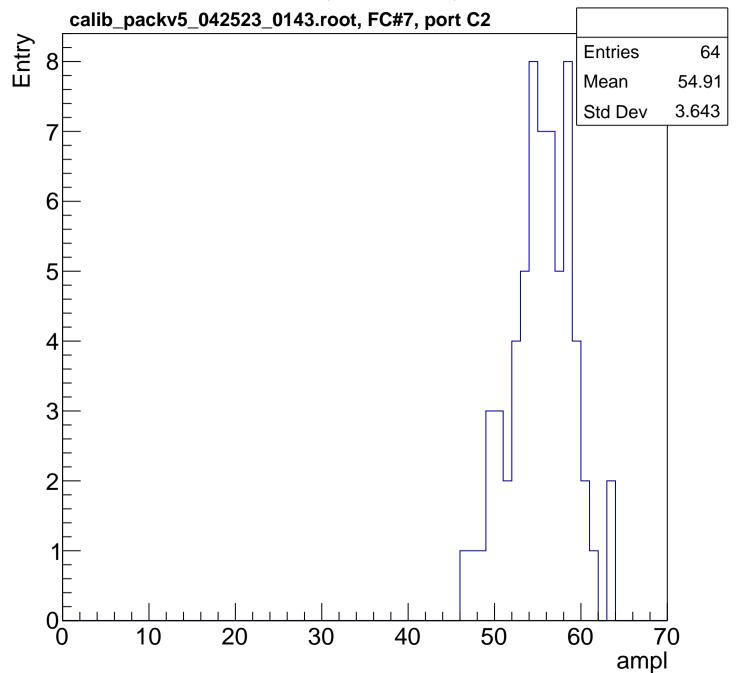


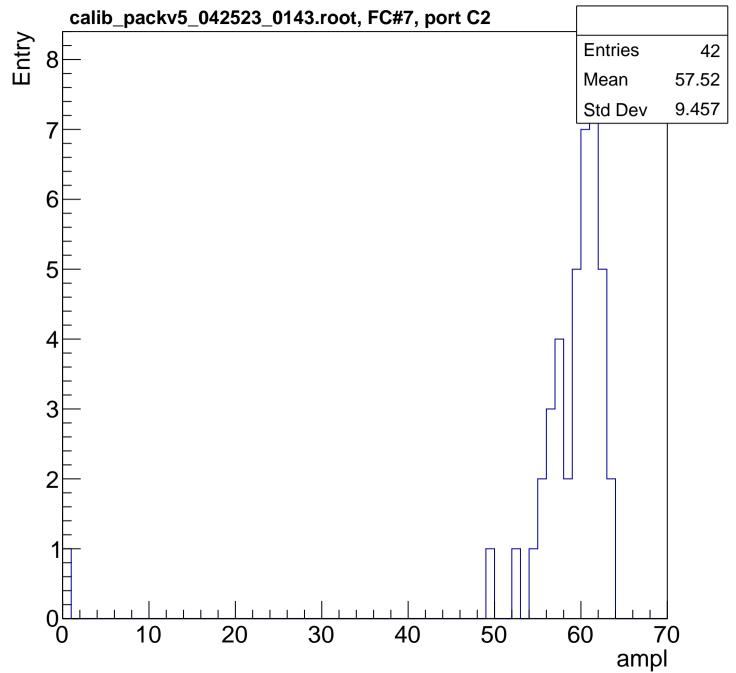


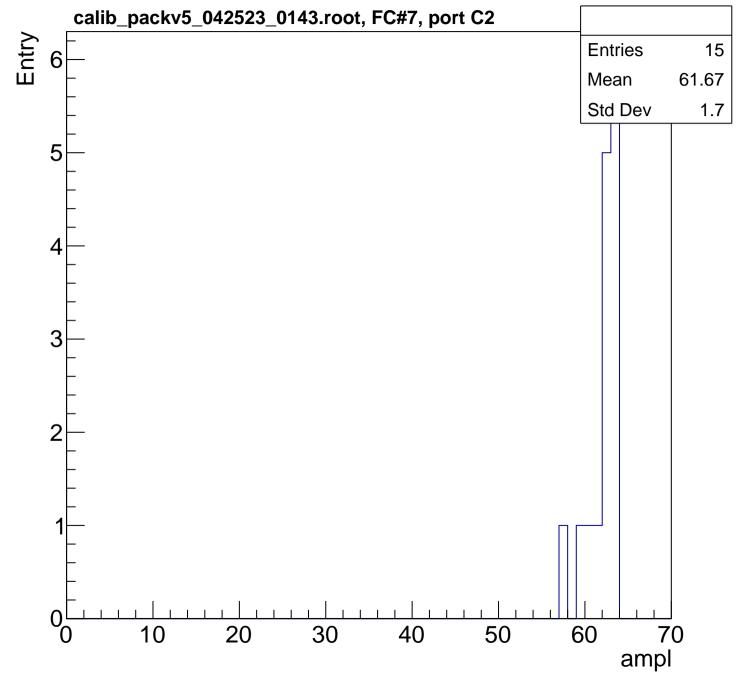


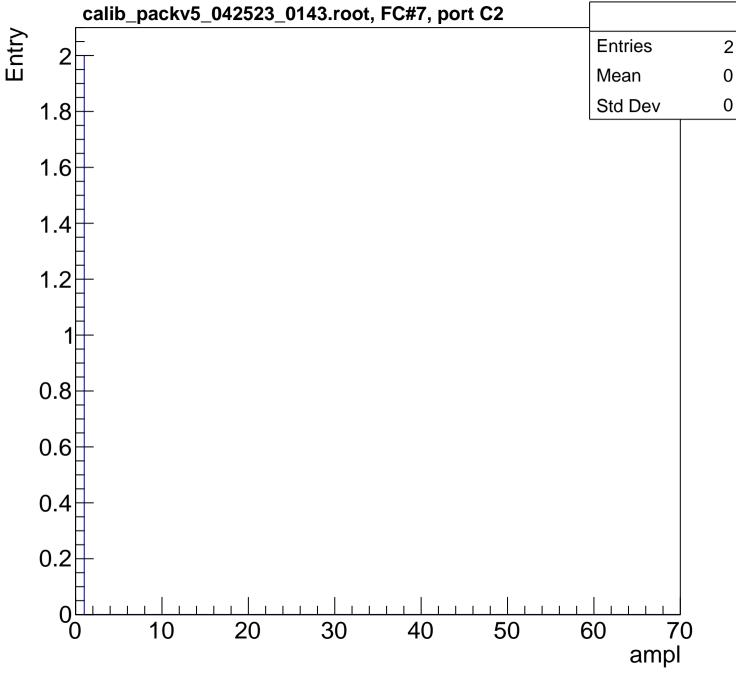


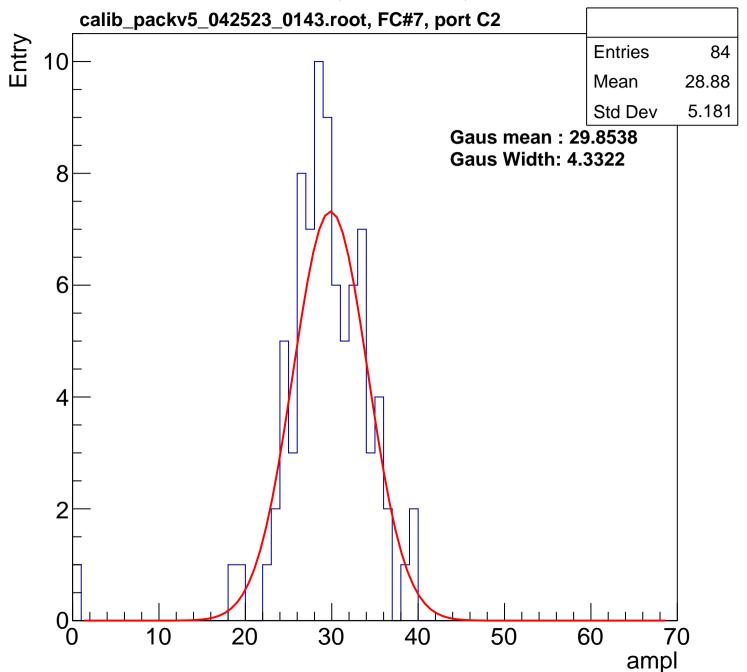


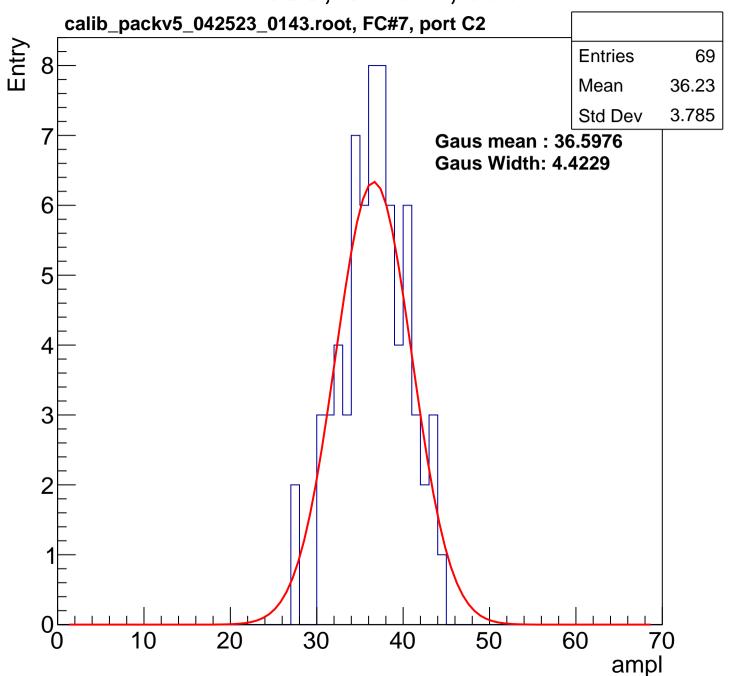


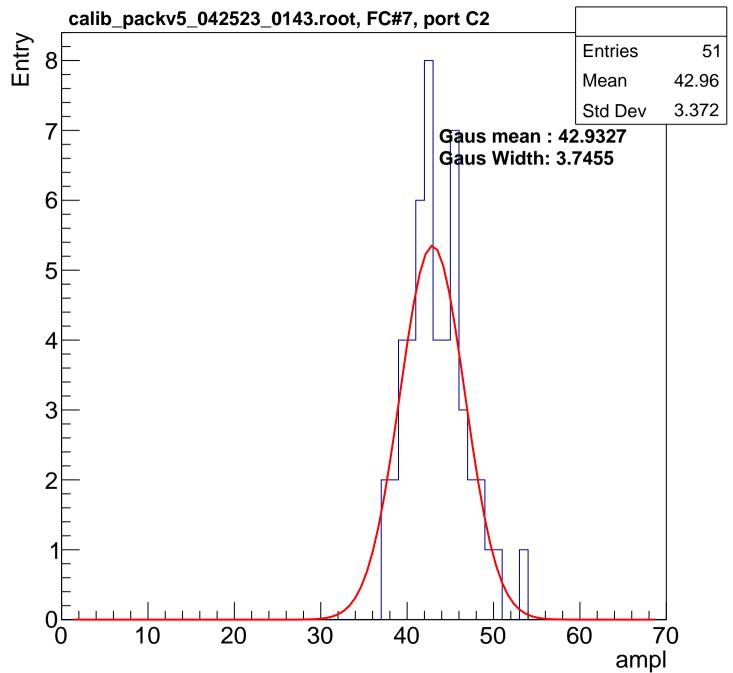


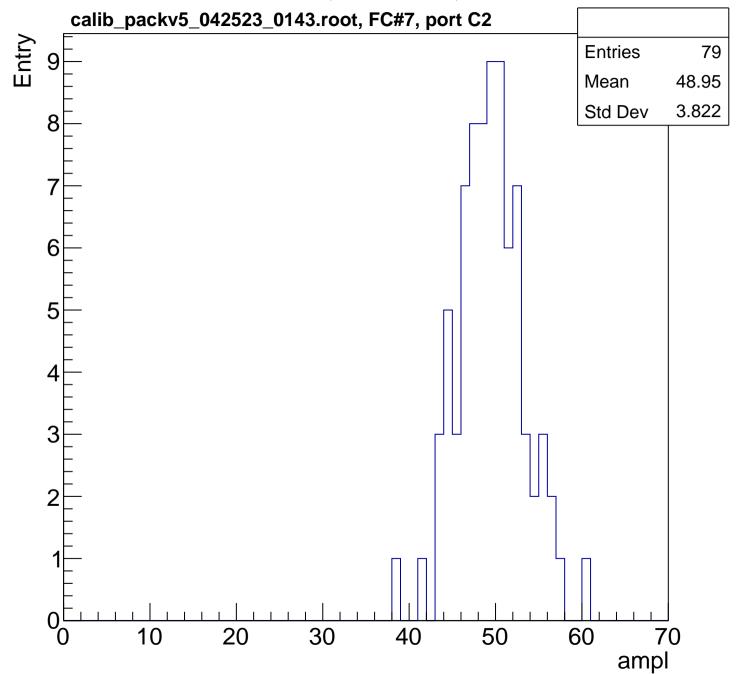


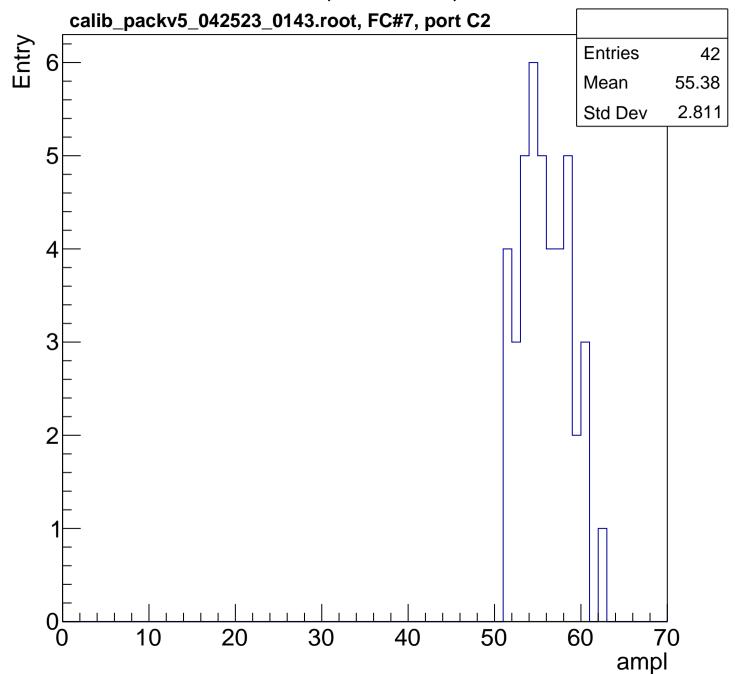


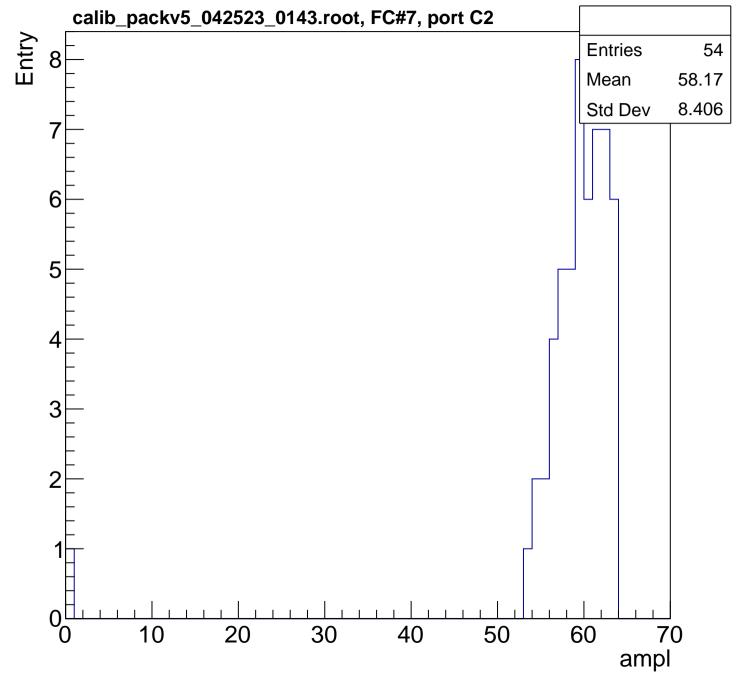


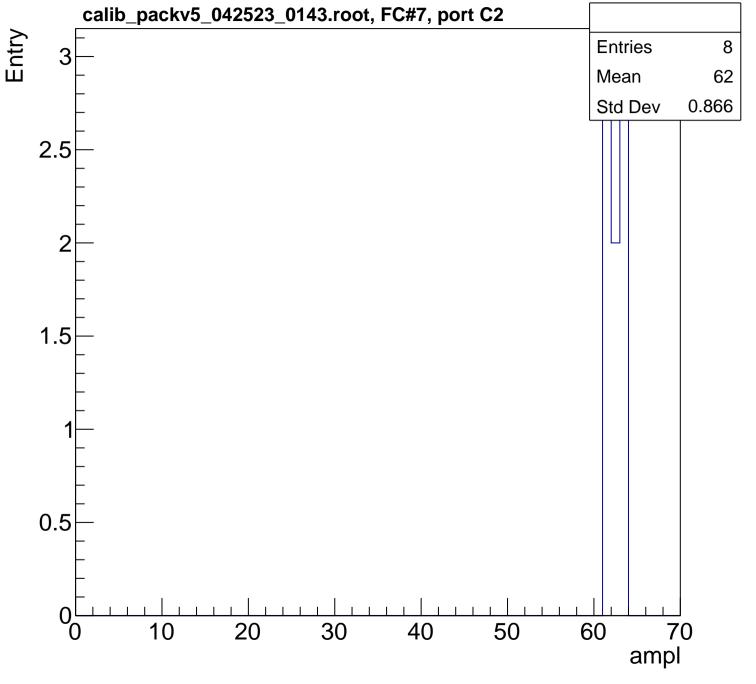


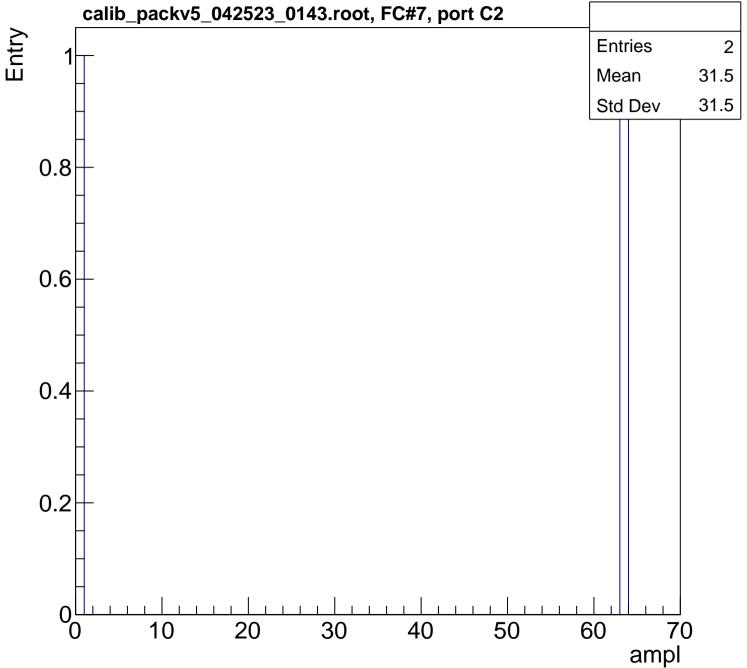


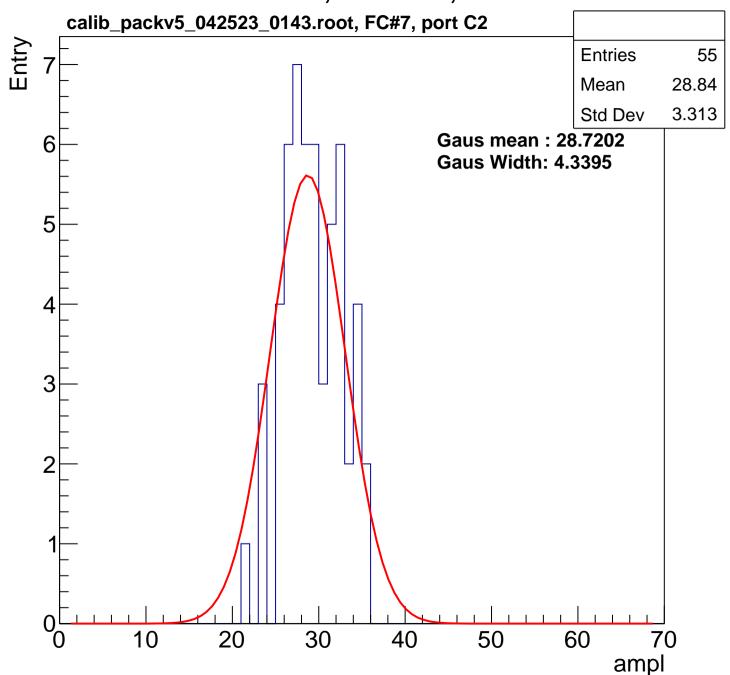


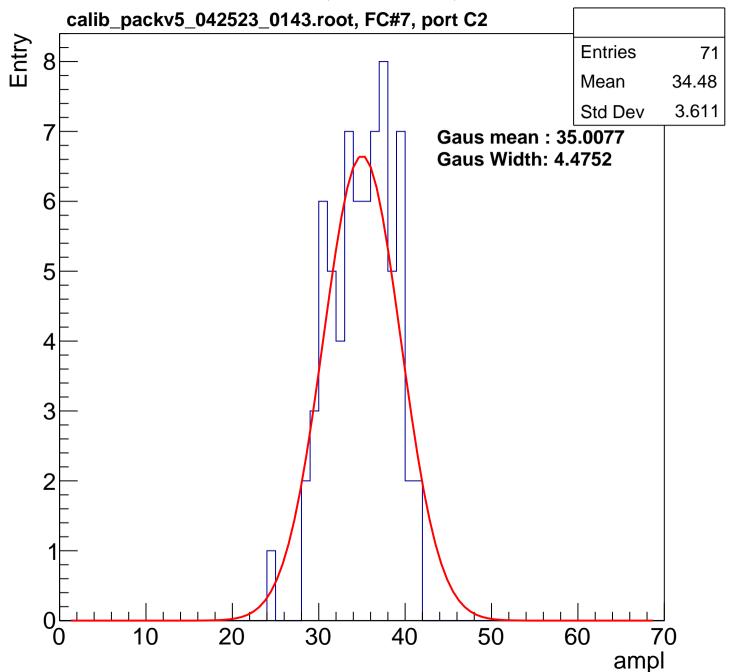


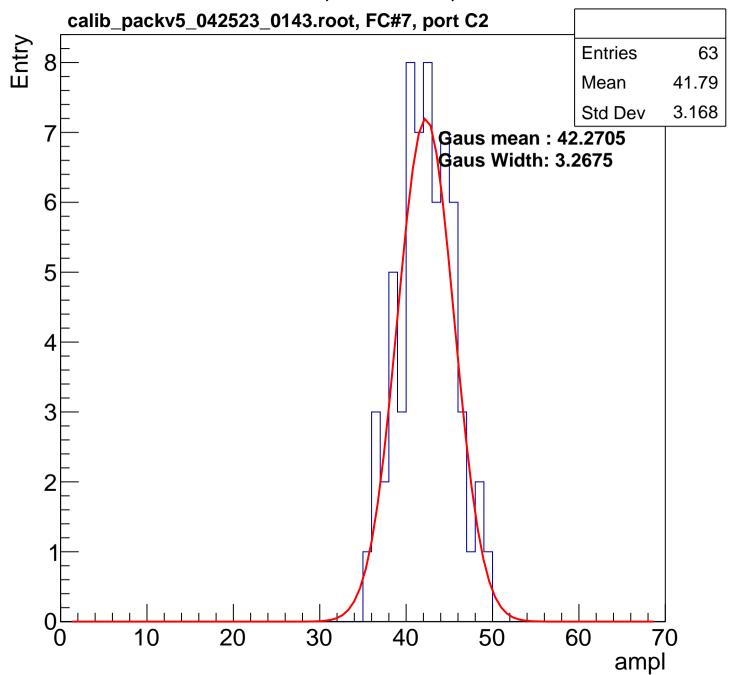


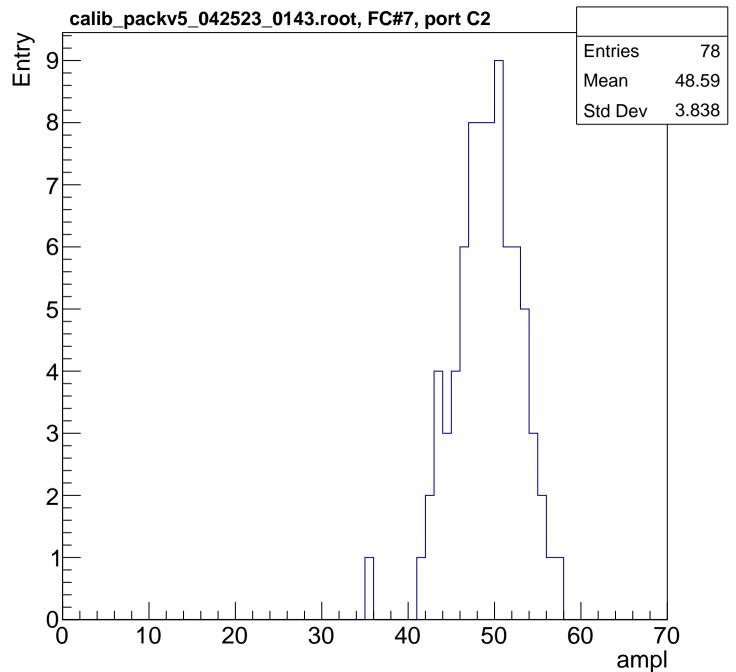


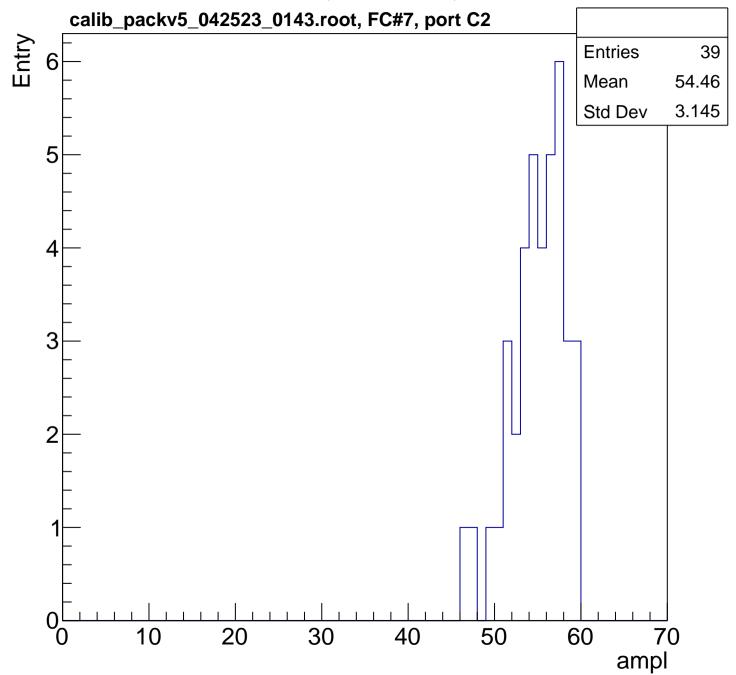


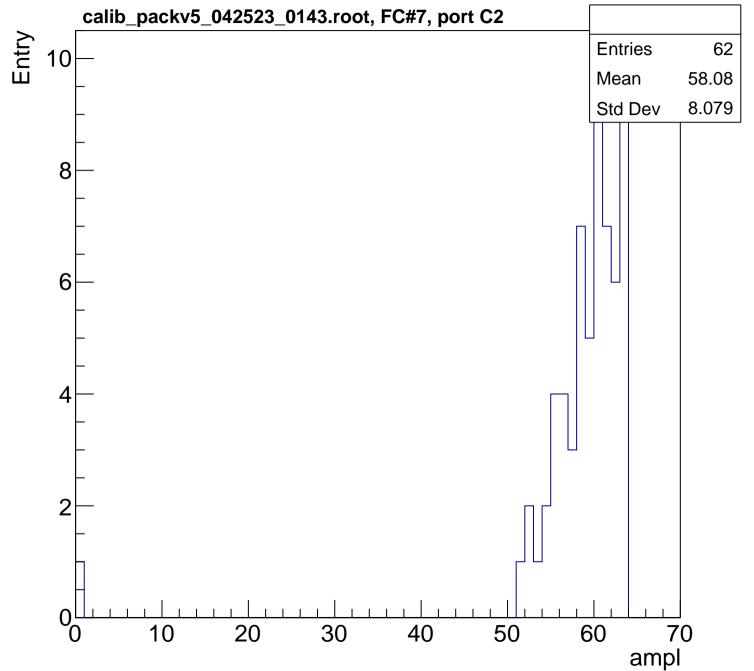


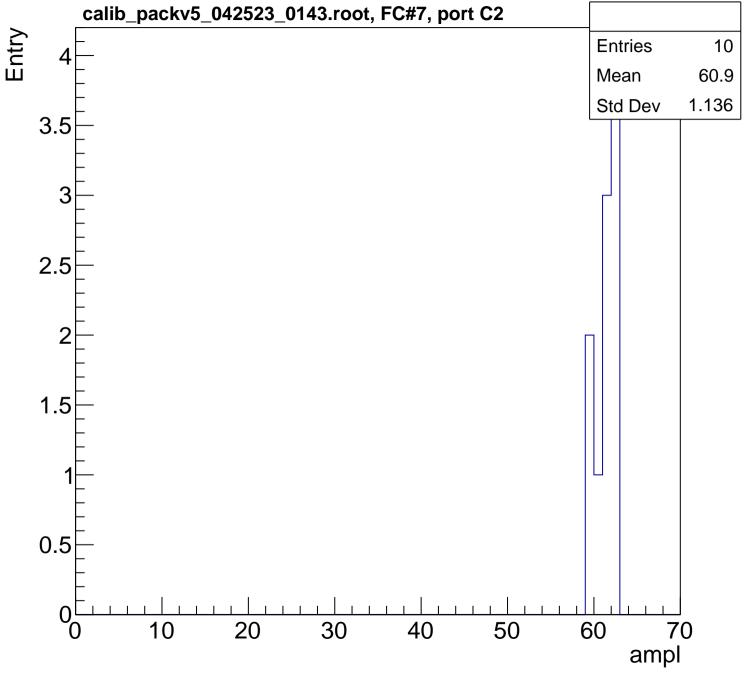




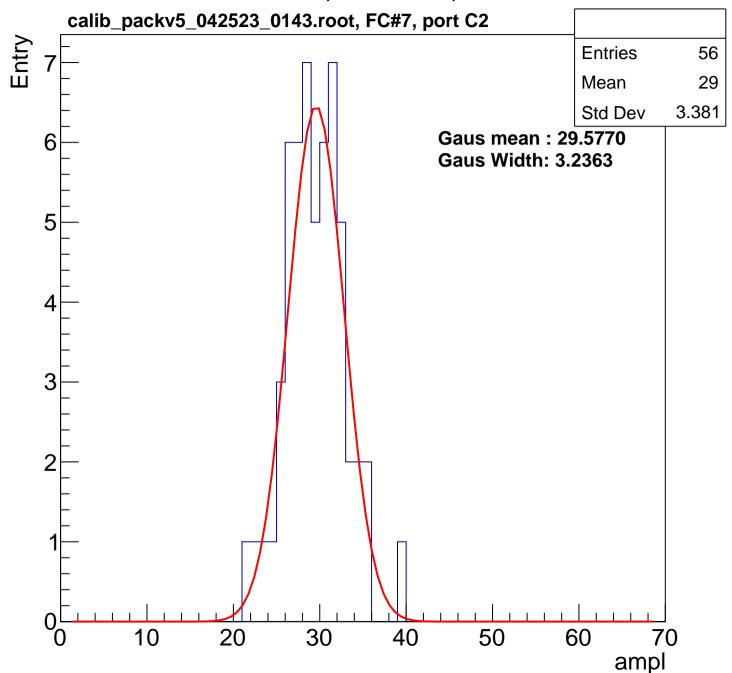


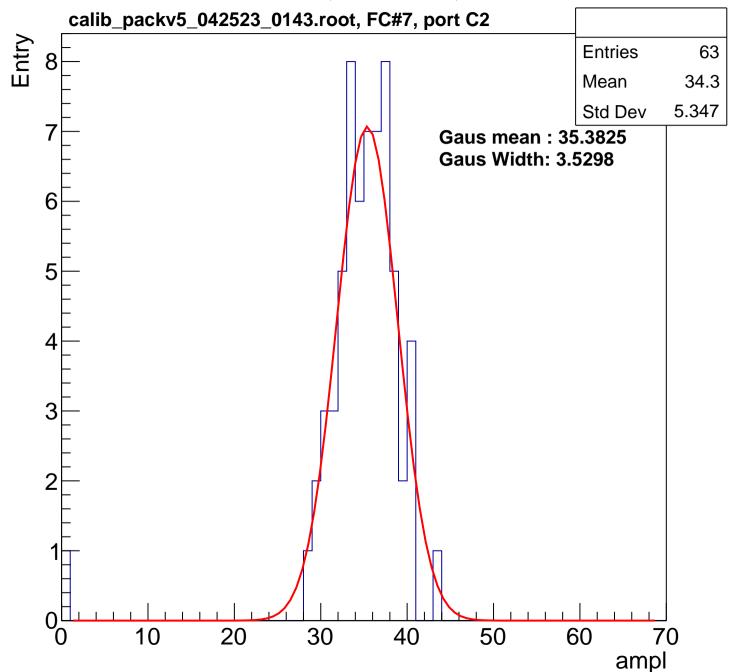


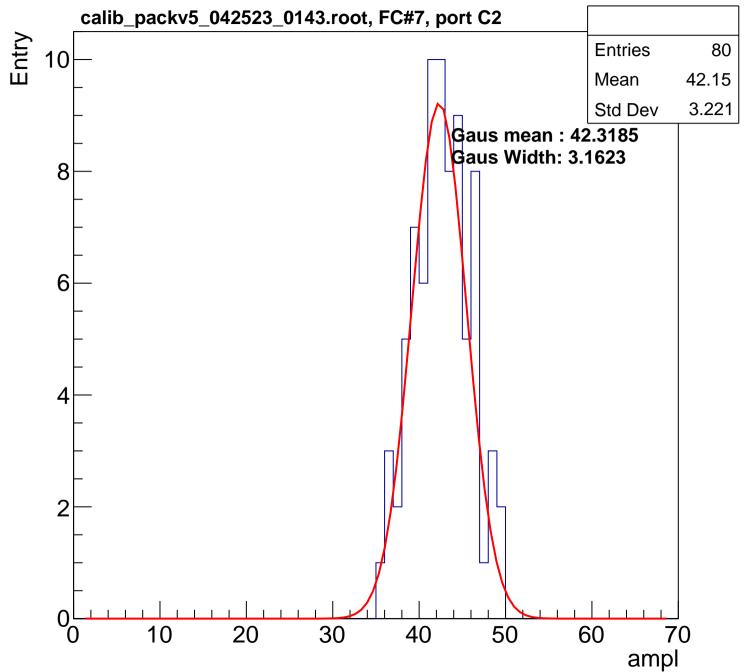


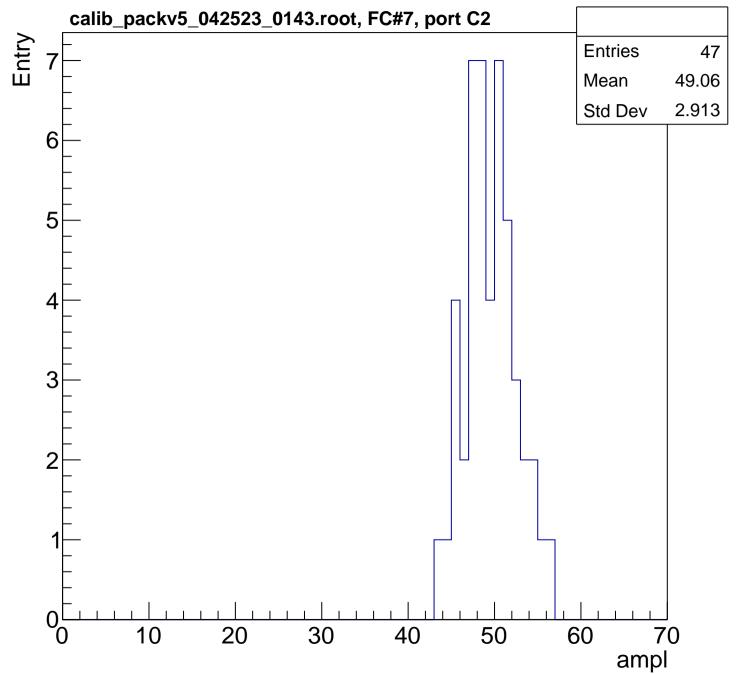


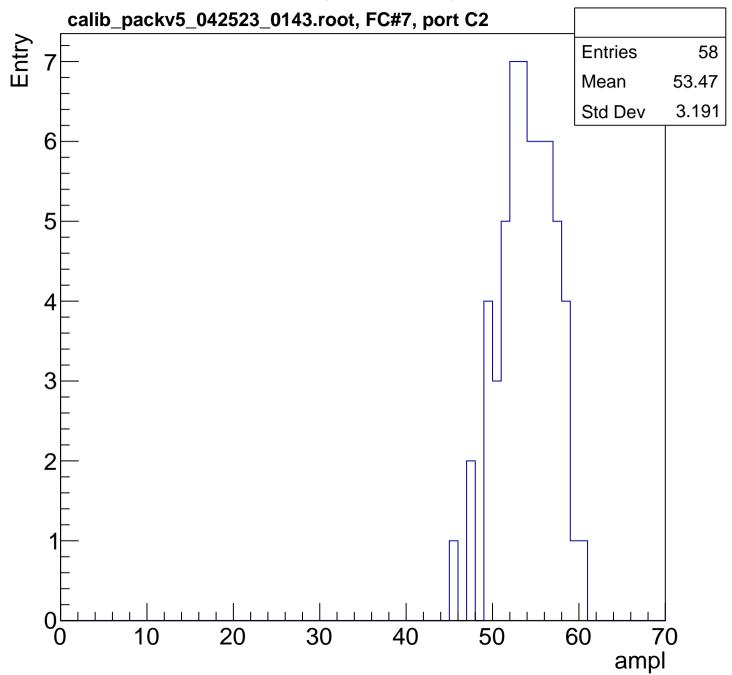
B1L103S, U4-ch5, adc7 calib_packv5_042523_0143.root, FC#7, port C2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

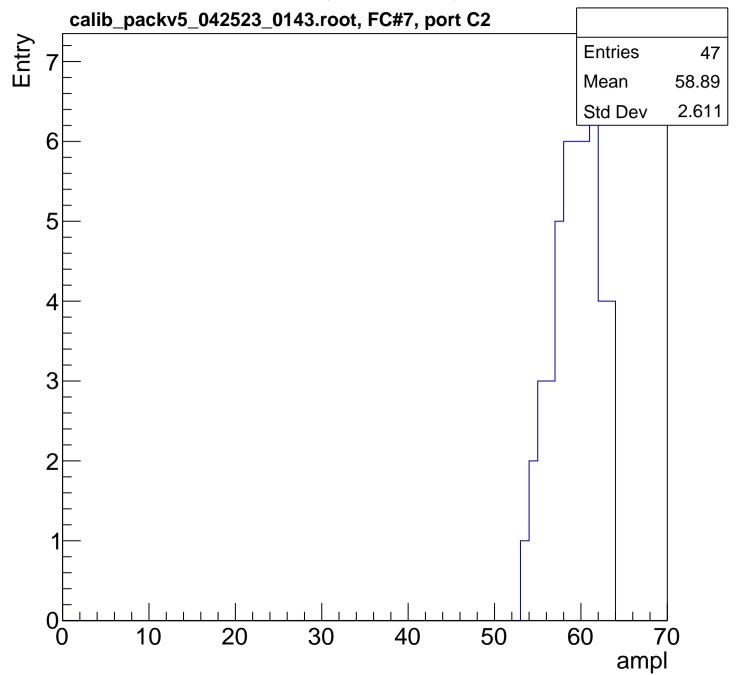


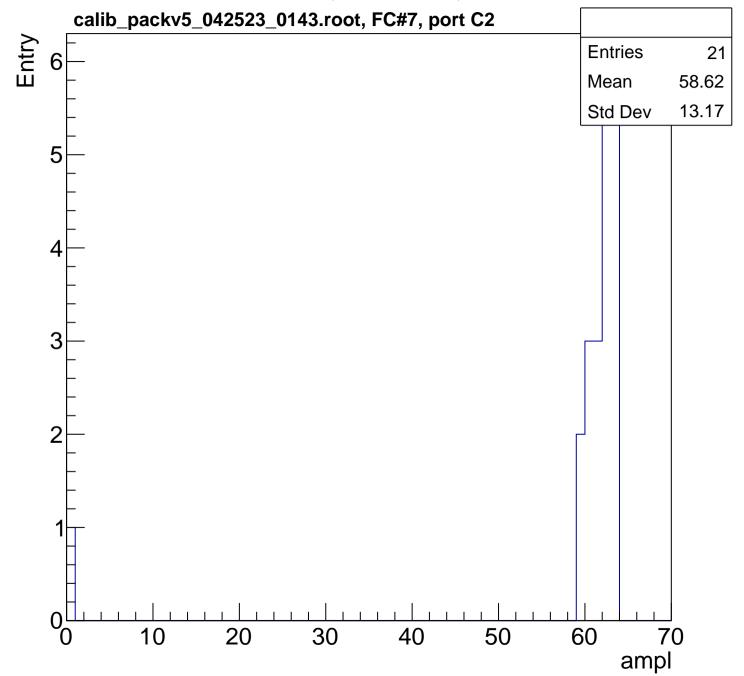


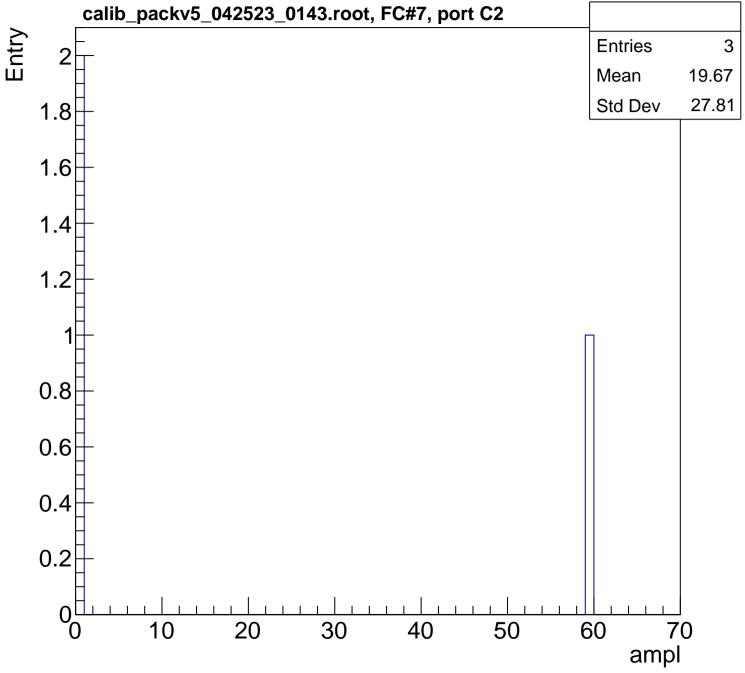


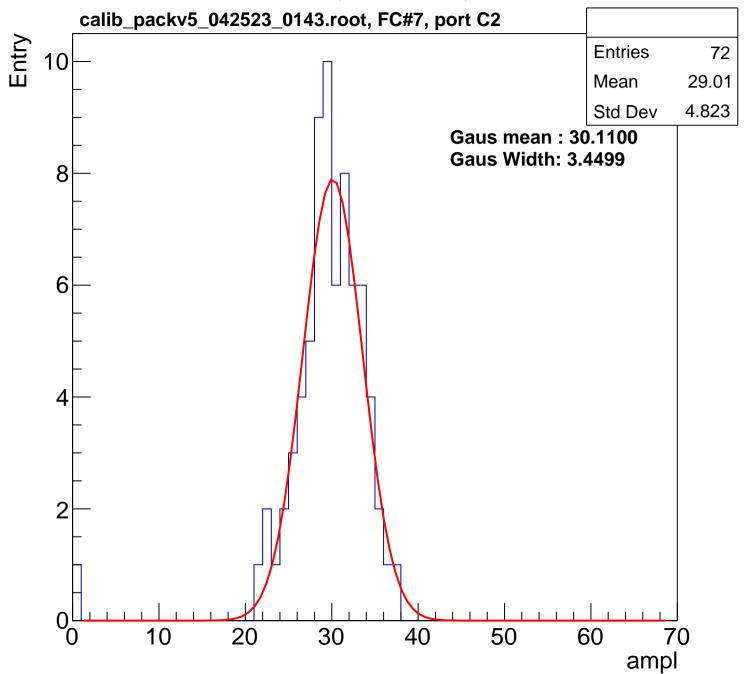


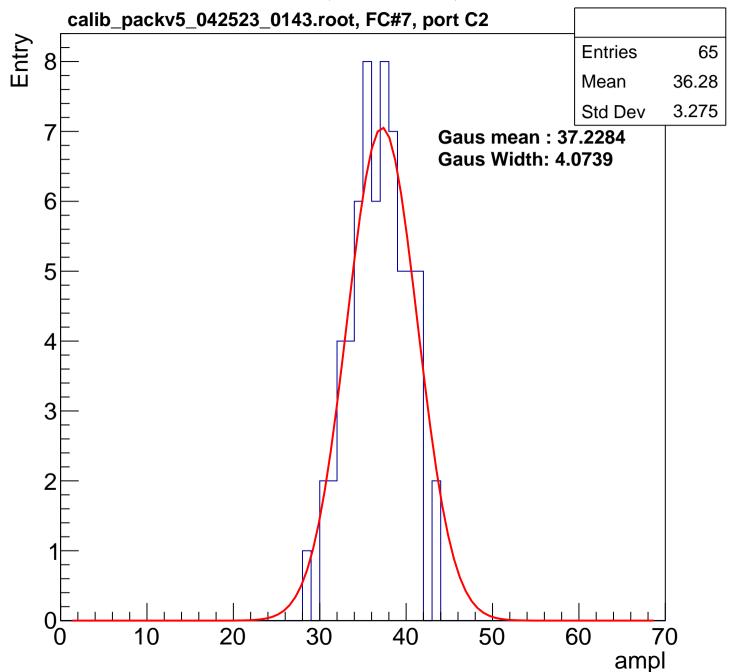


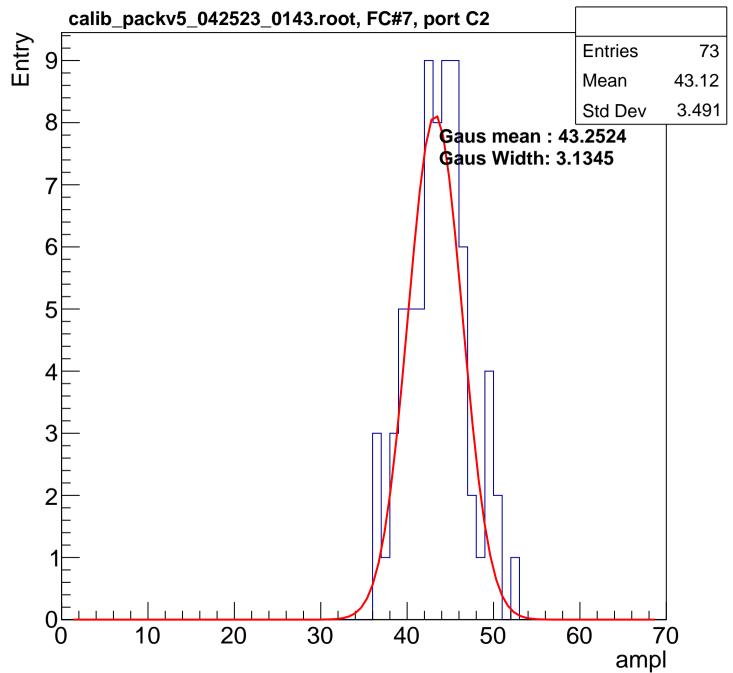


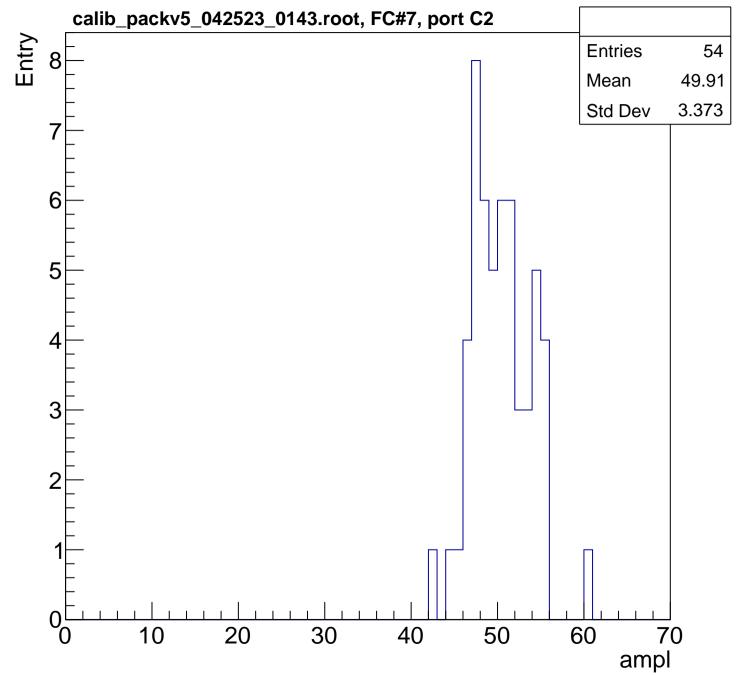


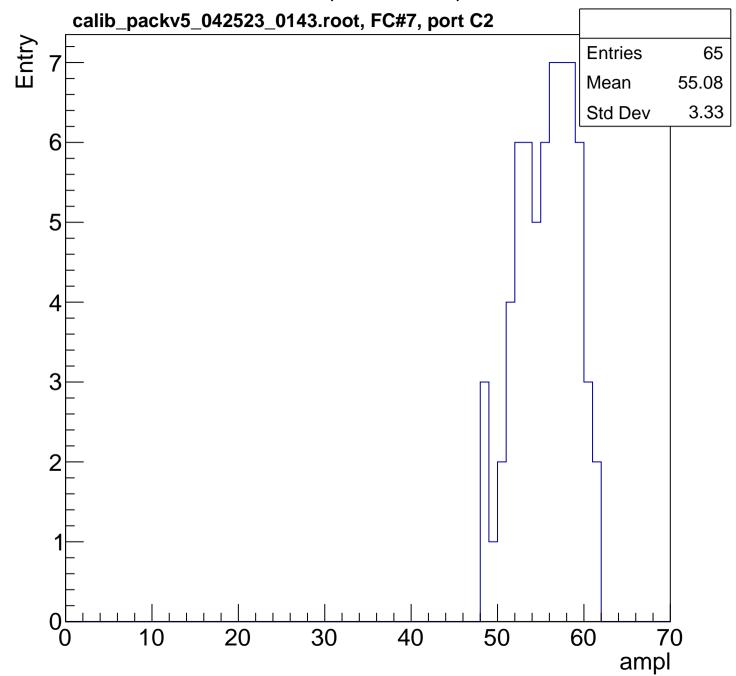


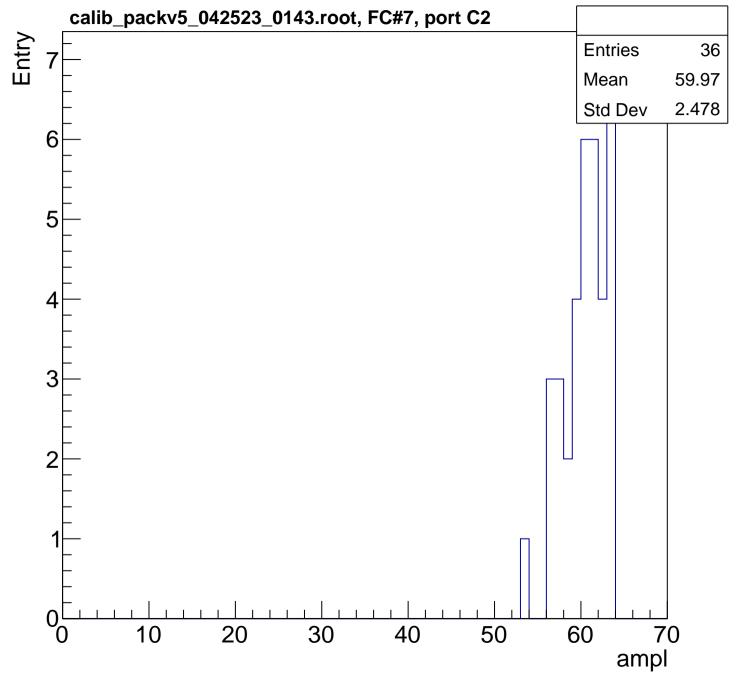


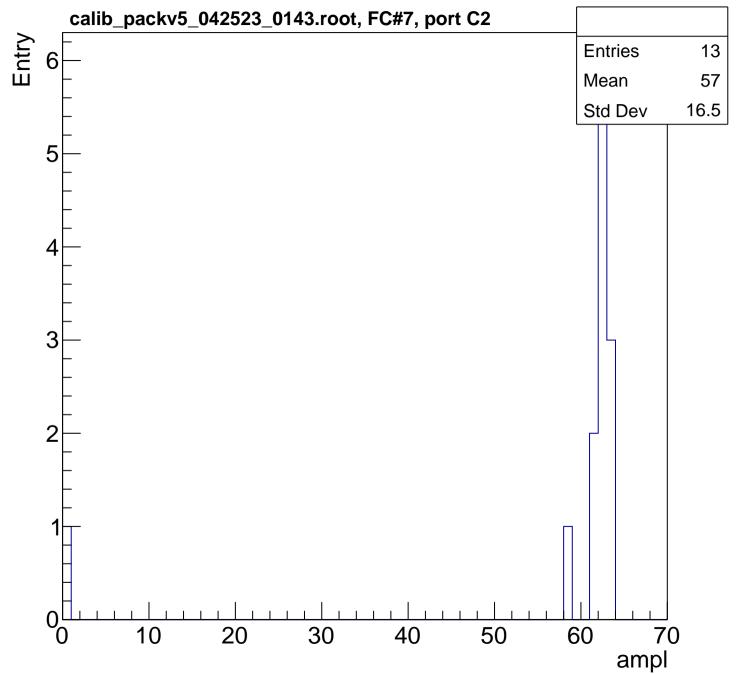




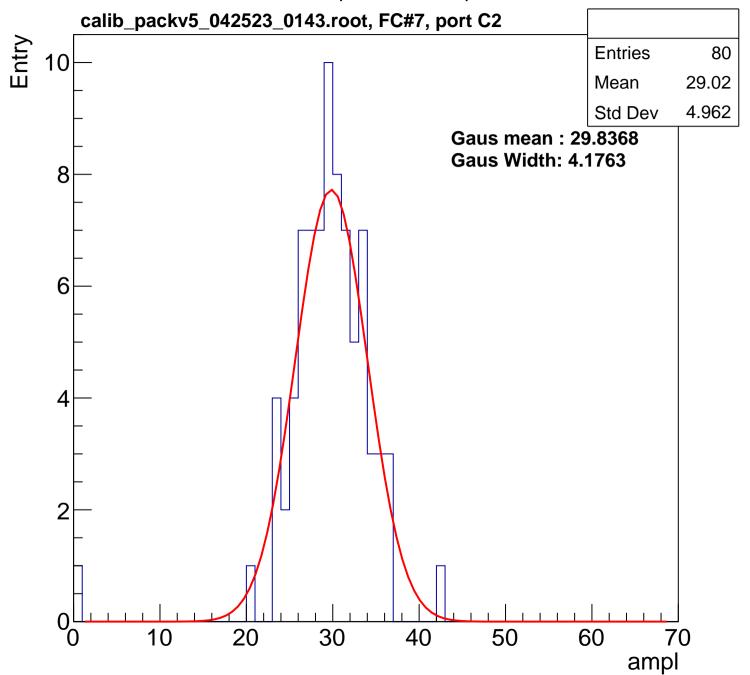


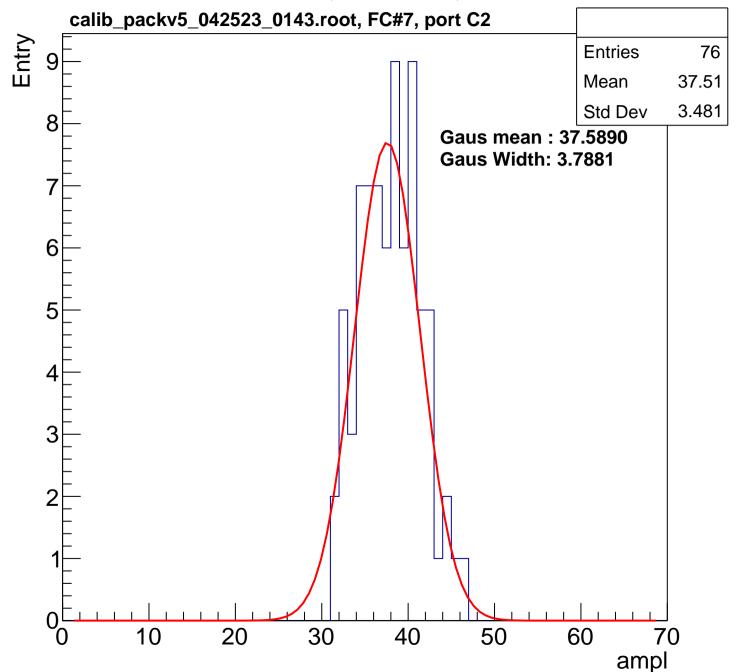


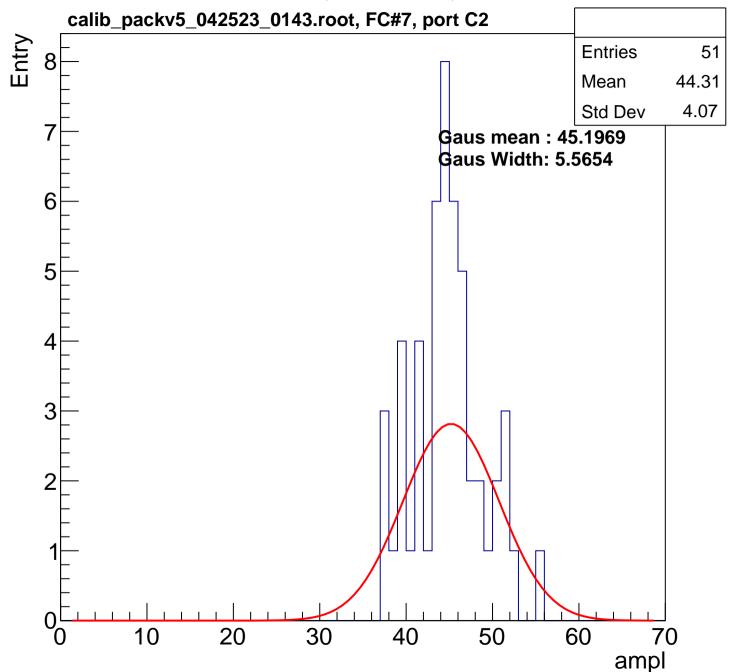


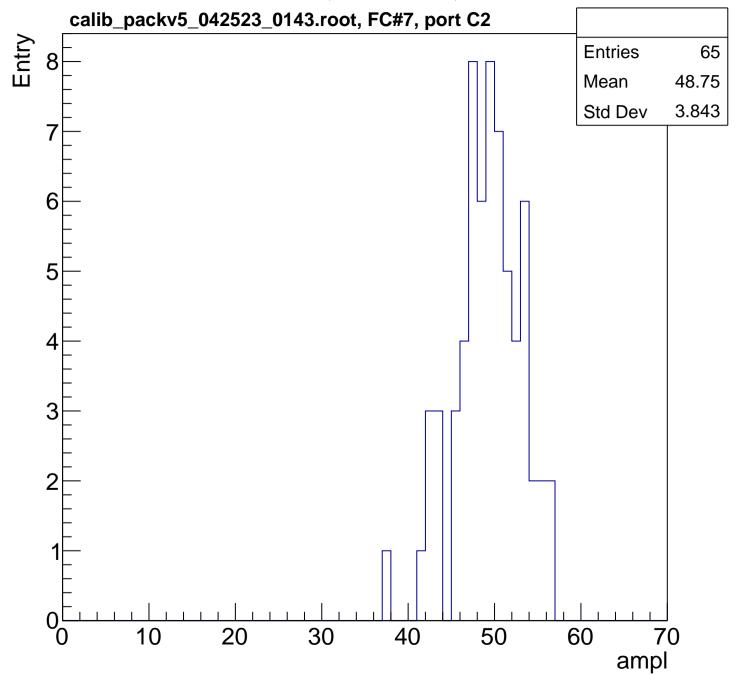


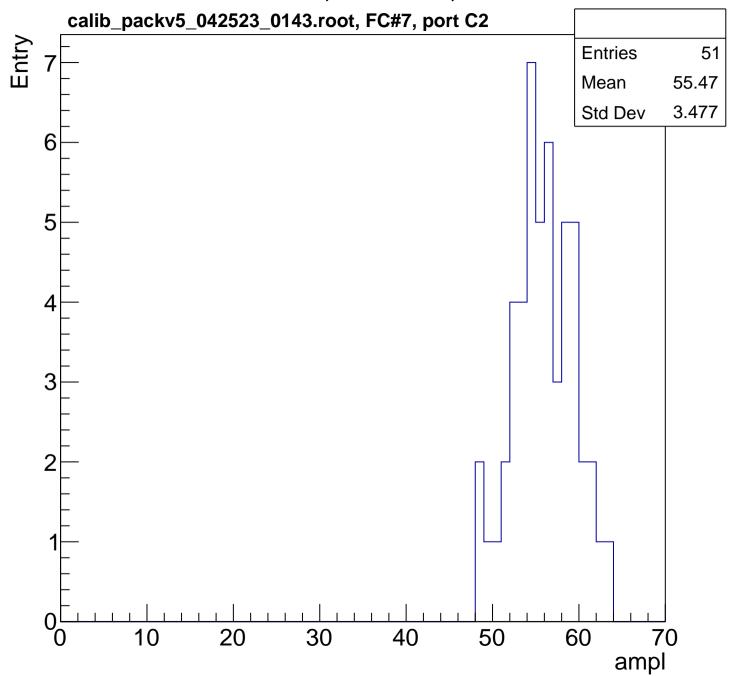
B1L103S, U4-ch7, adc7 calib_packv5_042523_0143.root, FC#7, port C2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

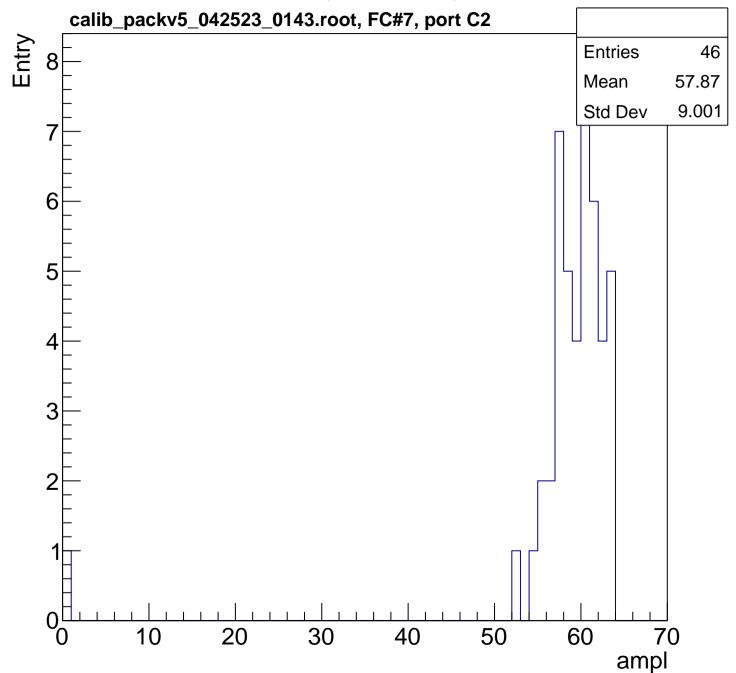


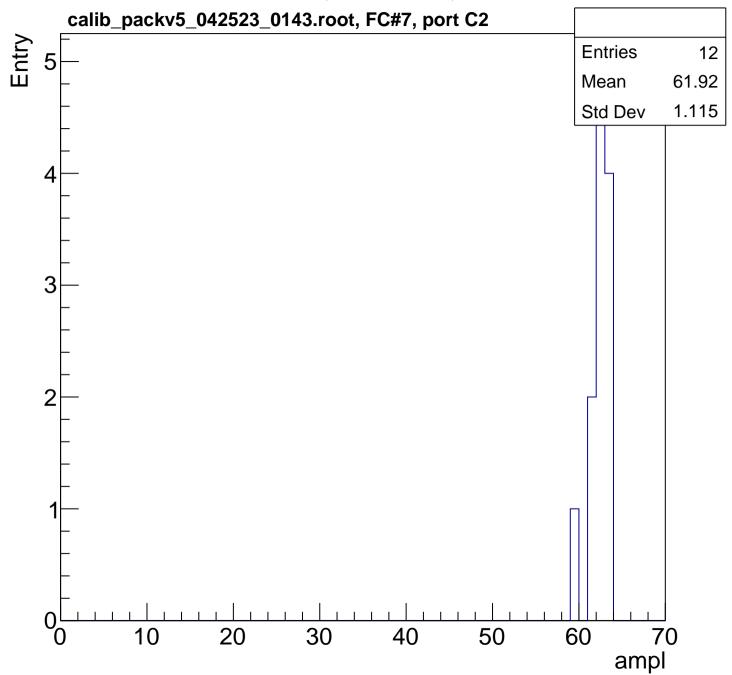




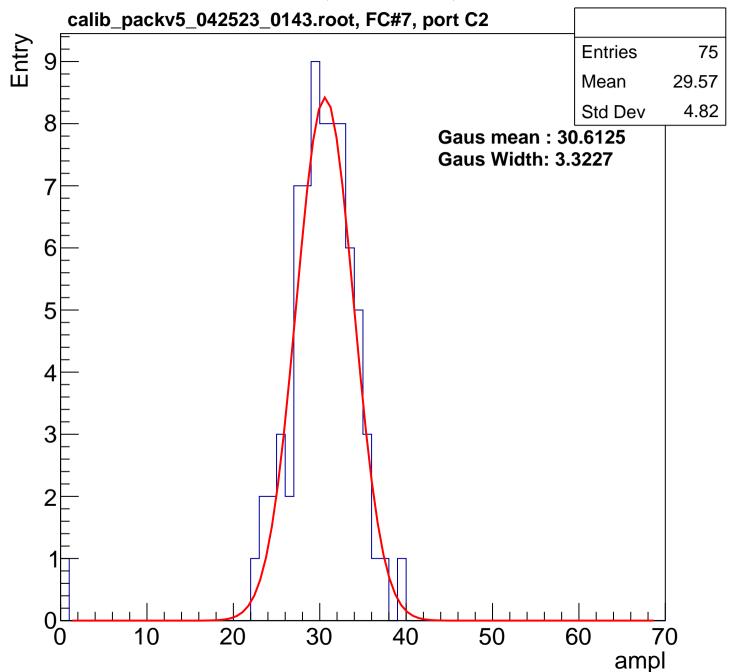


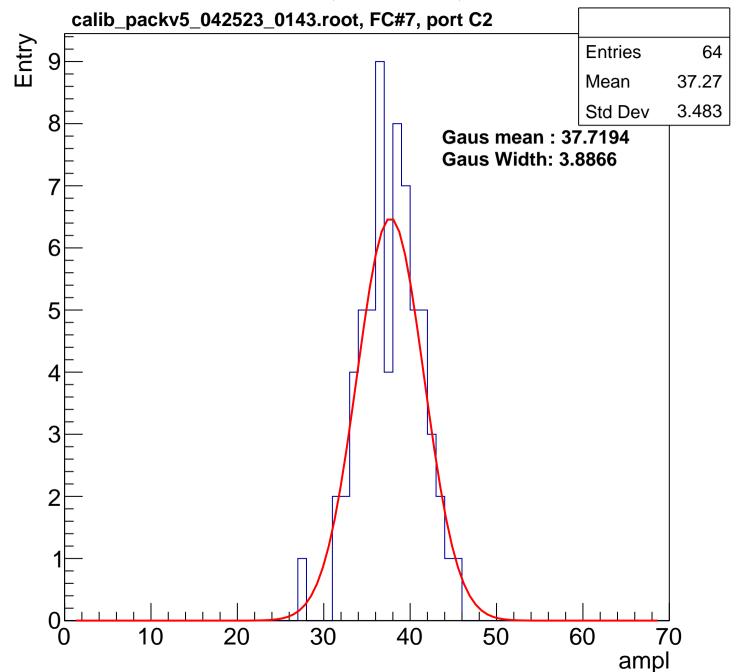


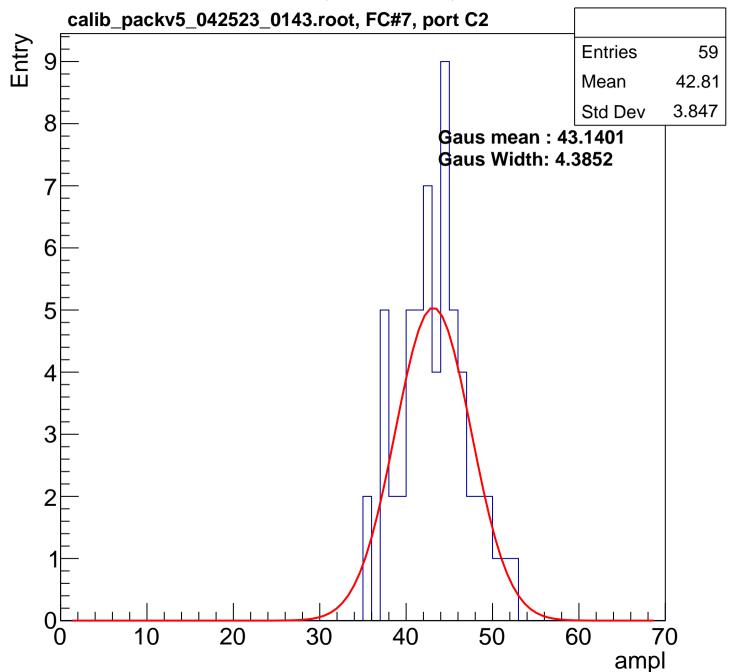


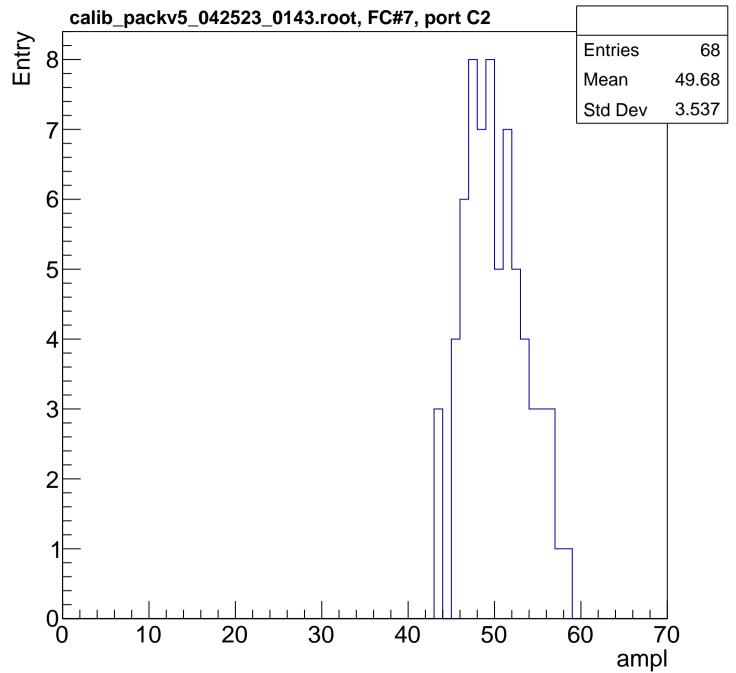


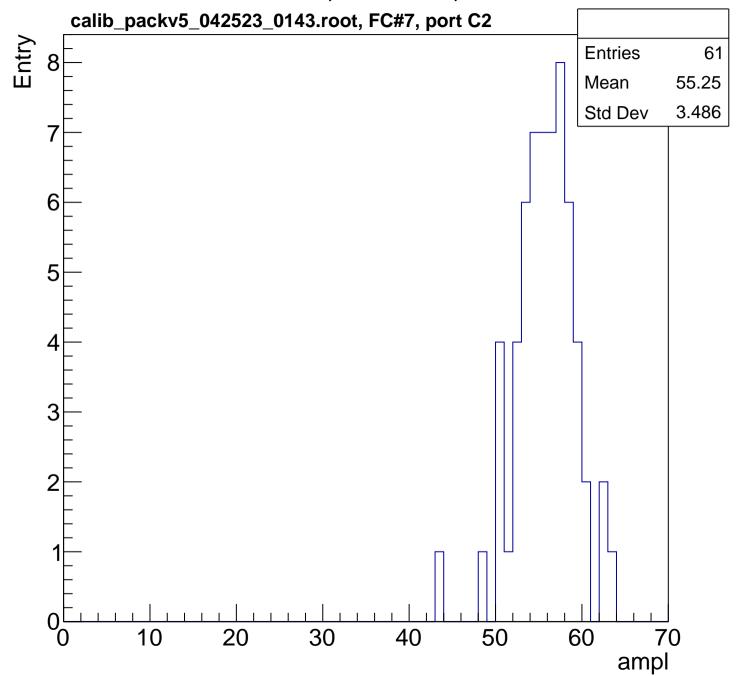
B1L103S, U4-ch8, adc7 calib_packv5_042523_0143.root, FC#7, port C2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

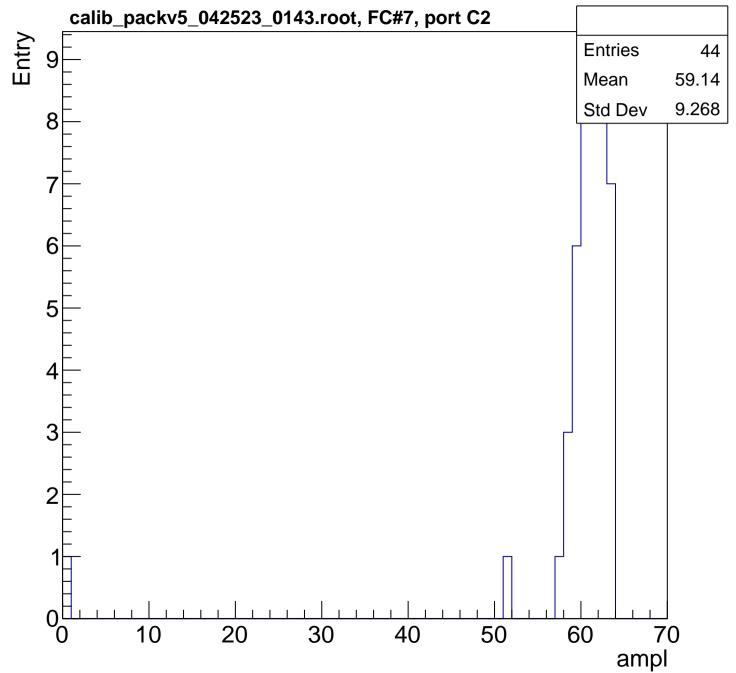


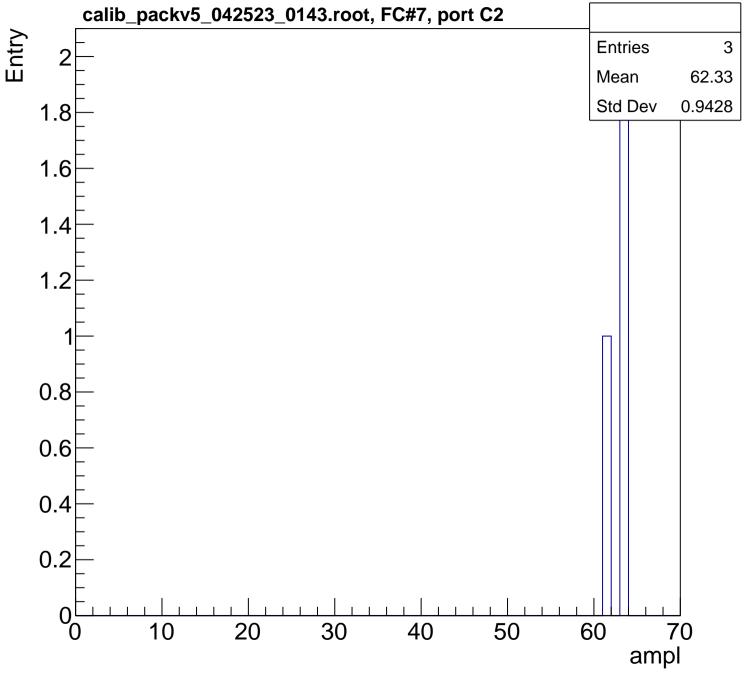


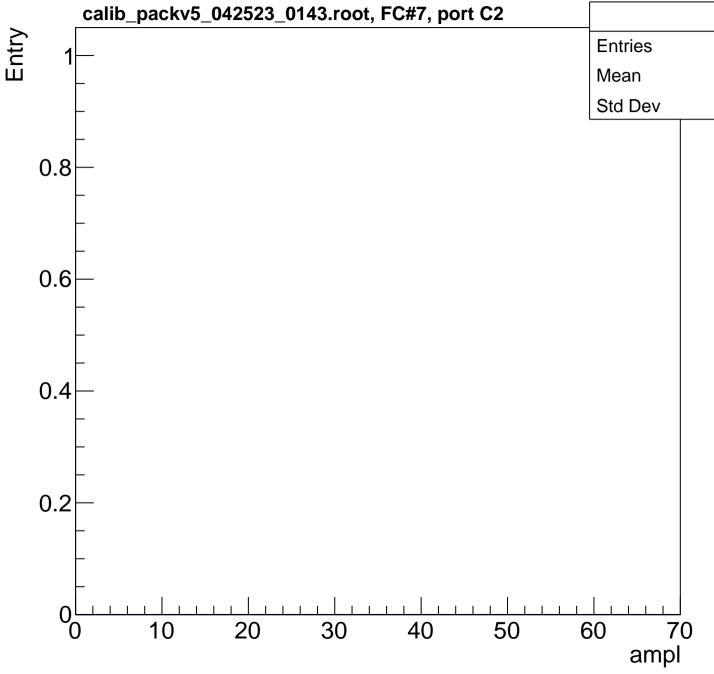


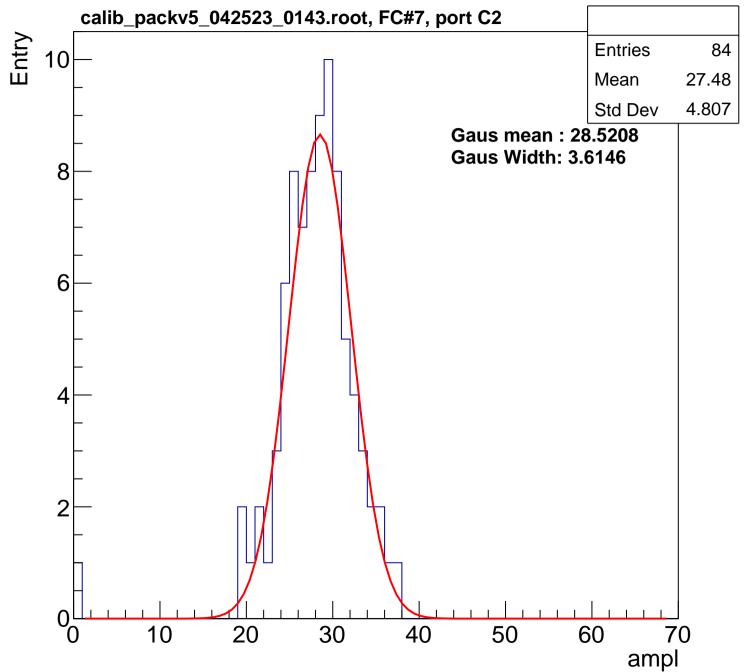


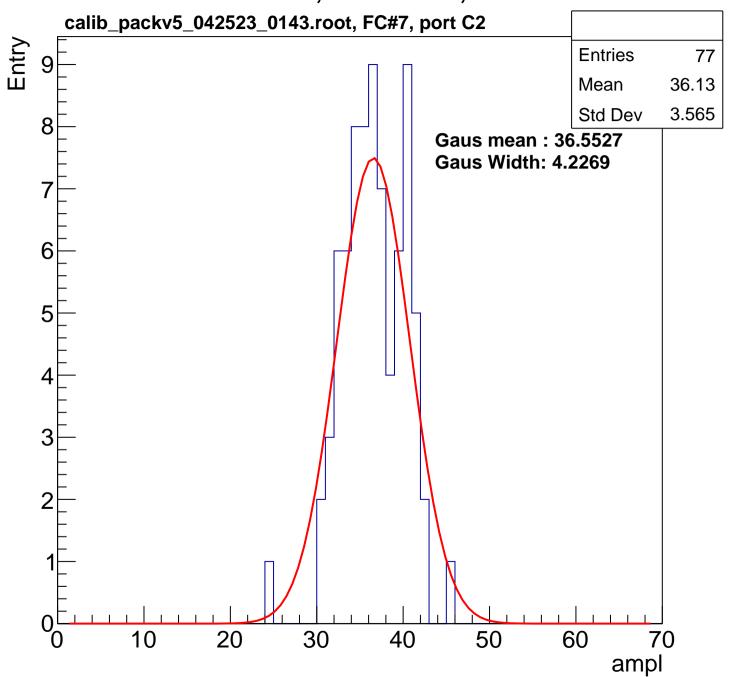


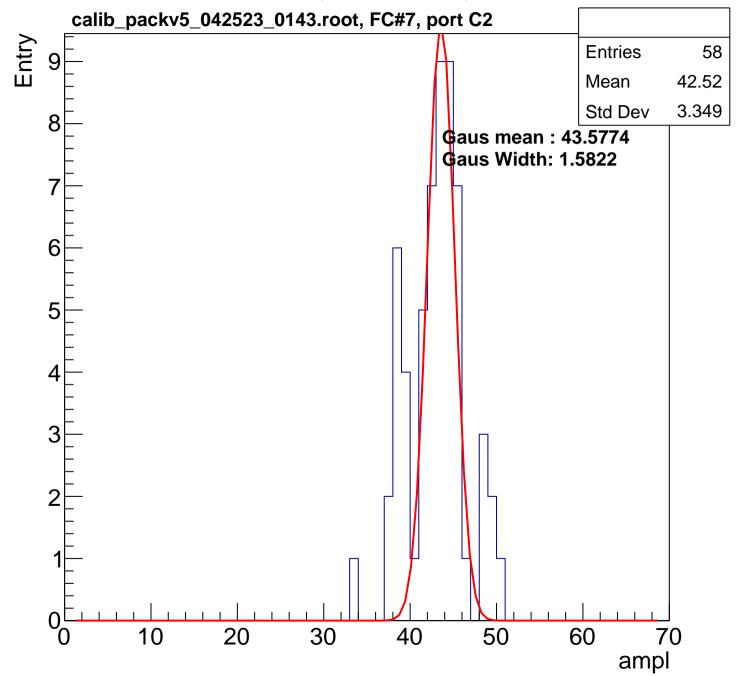


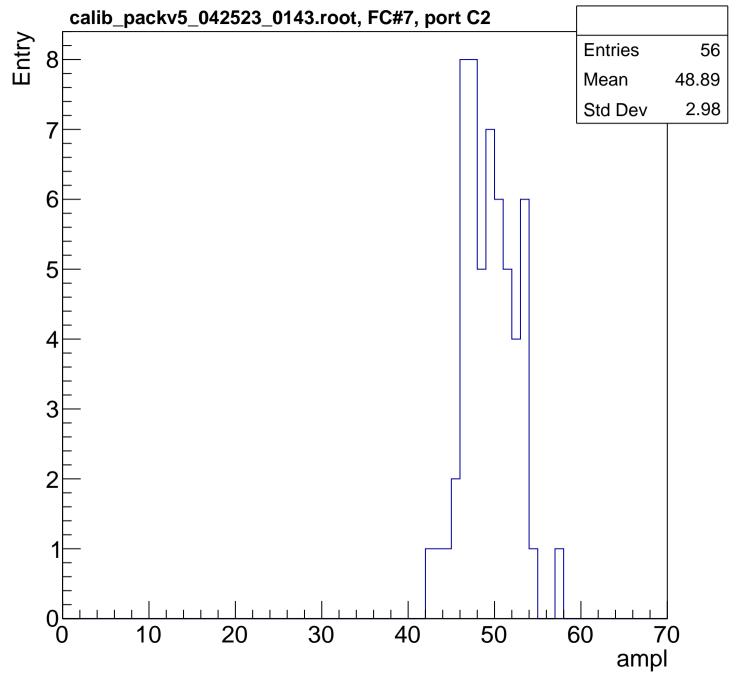


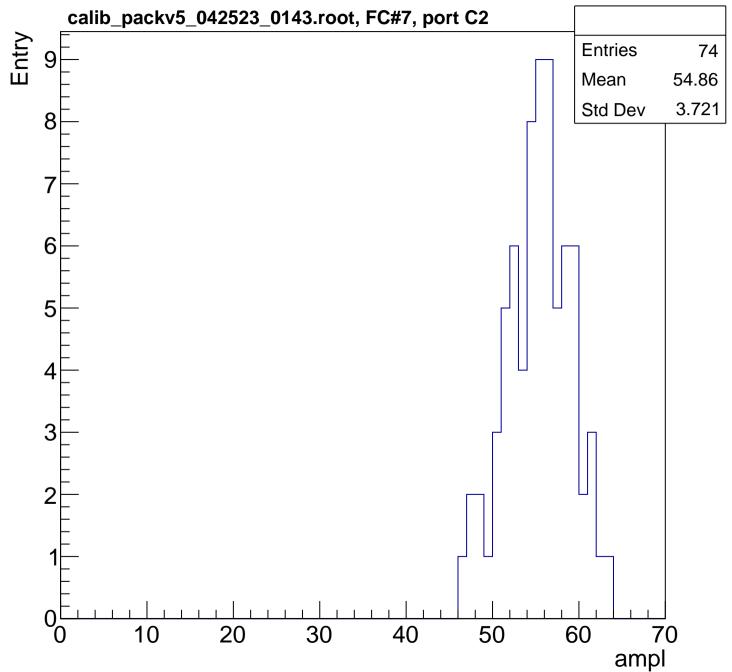


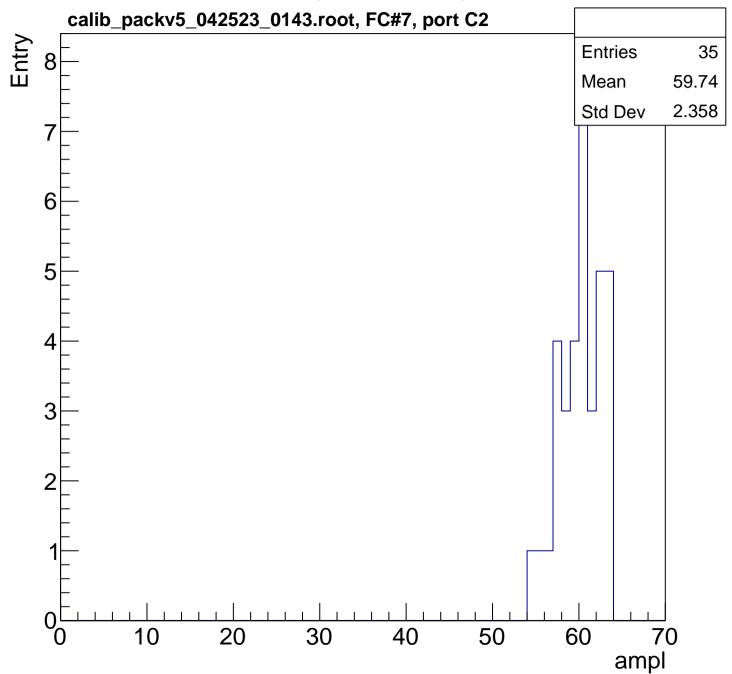


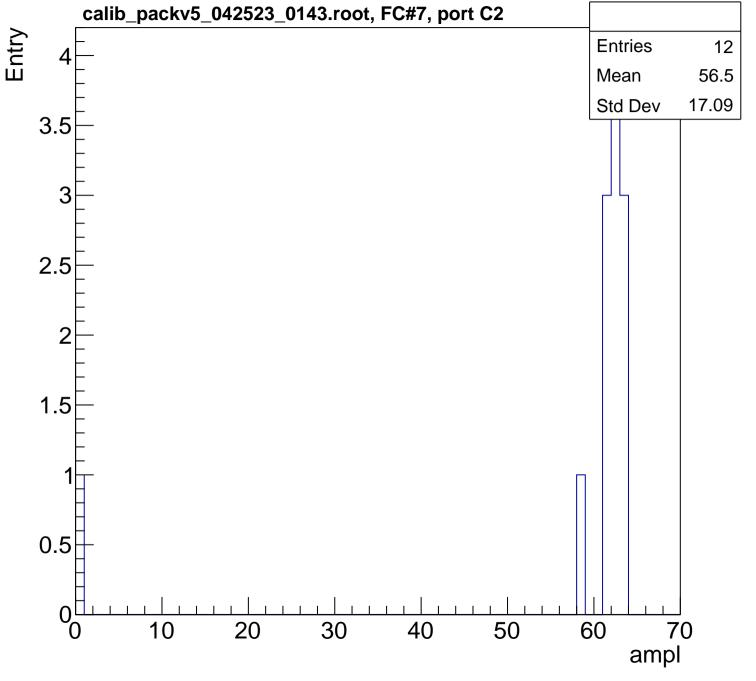


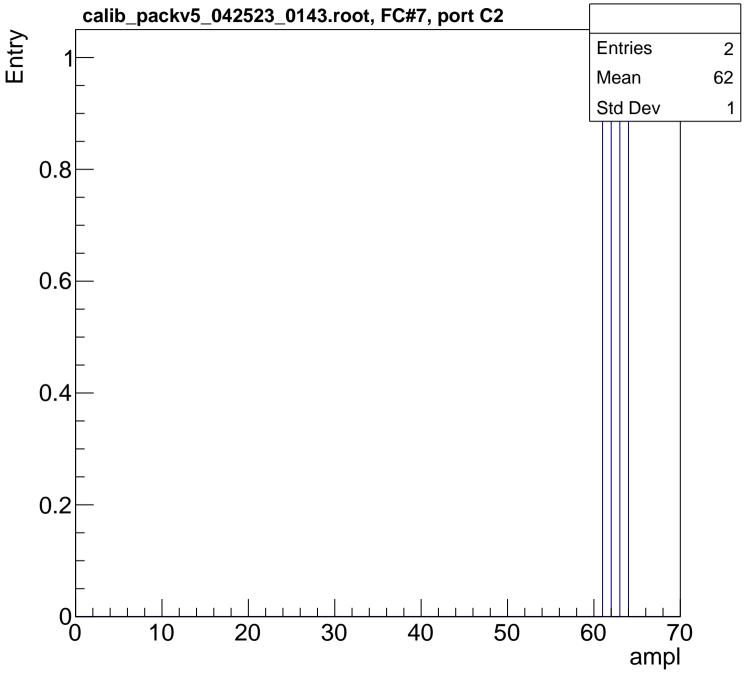


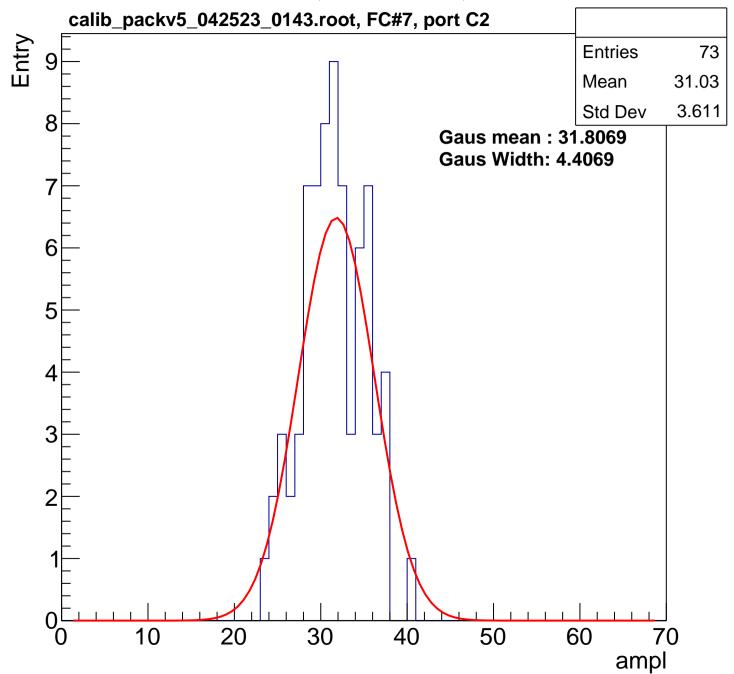


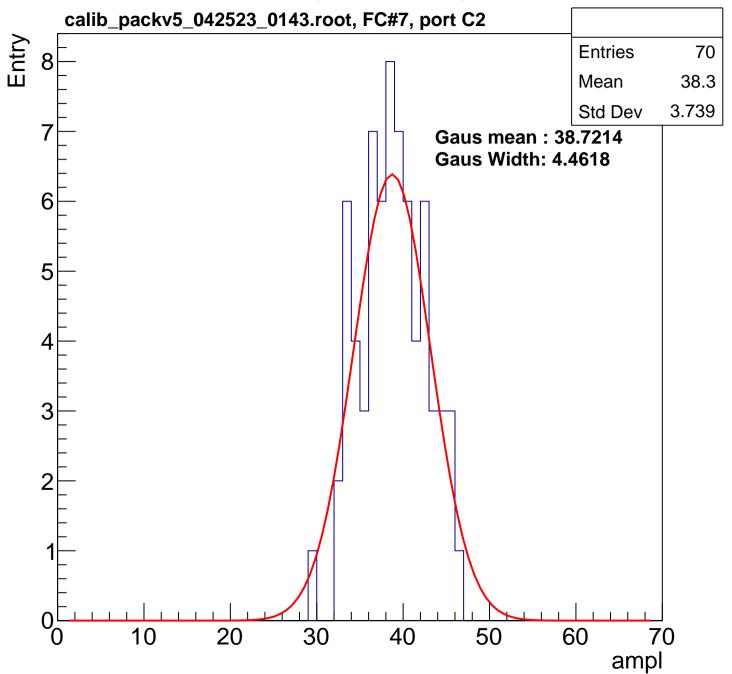


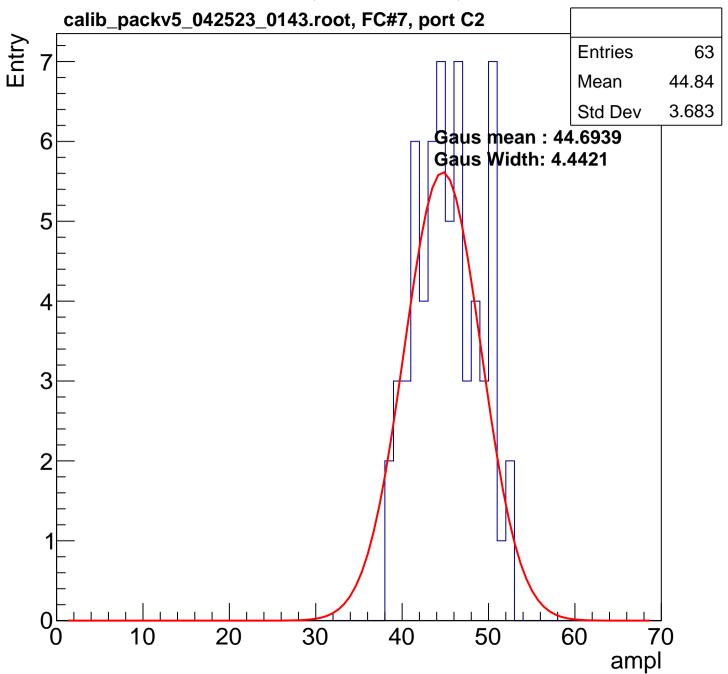


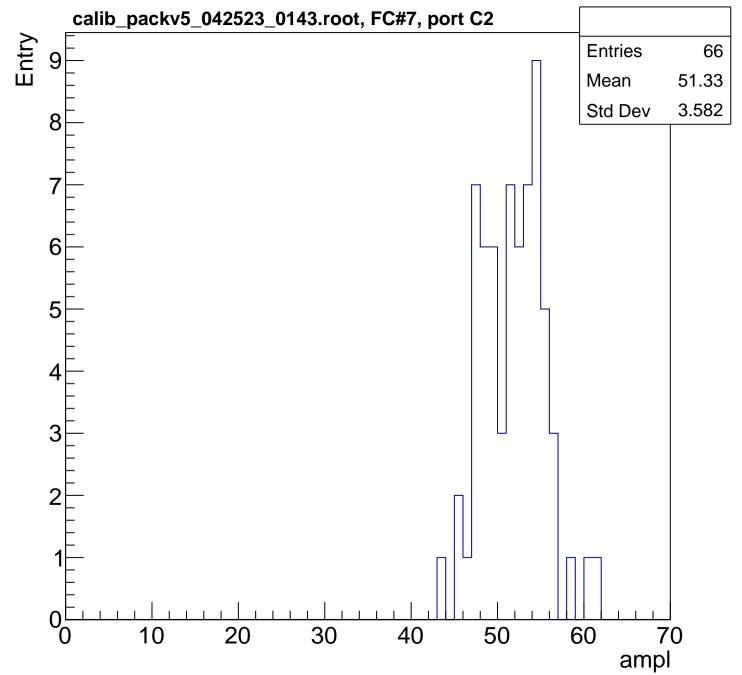


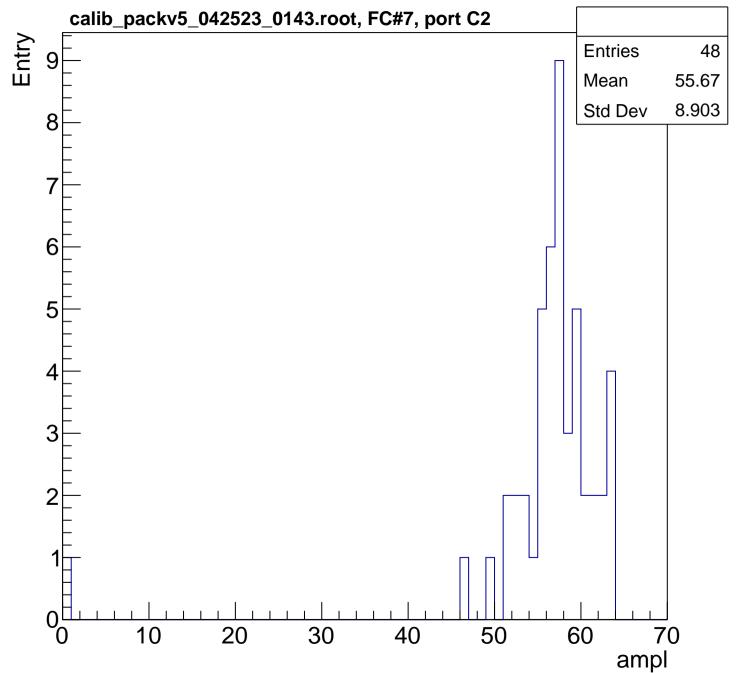


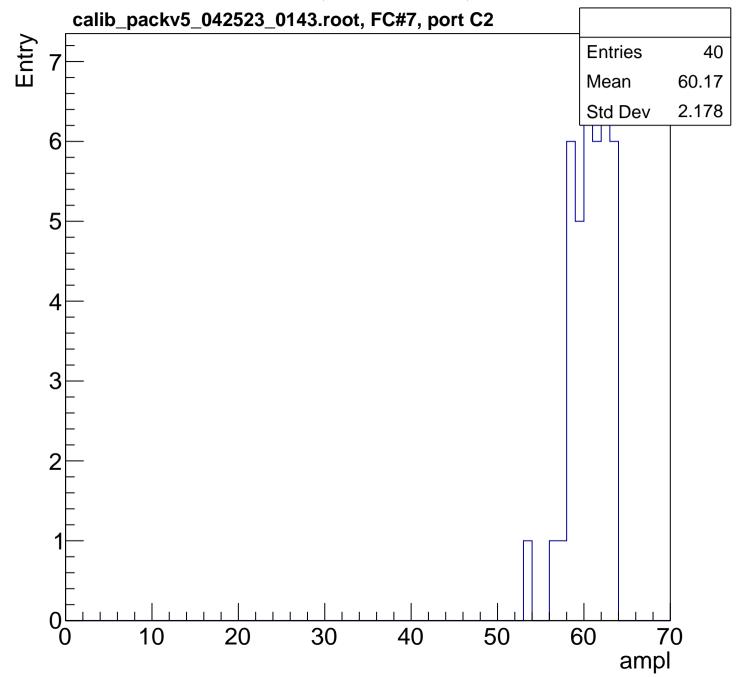


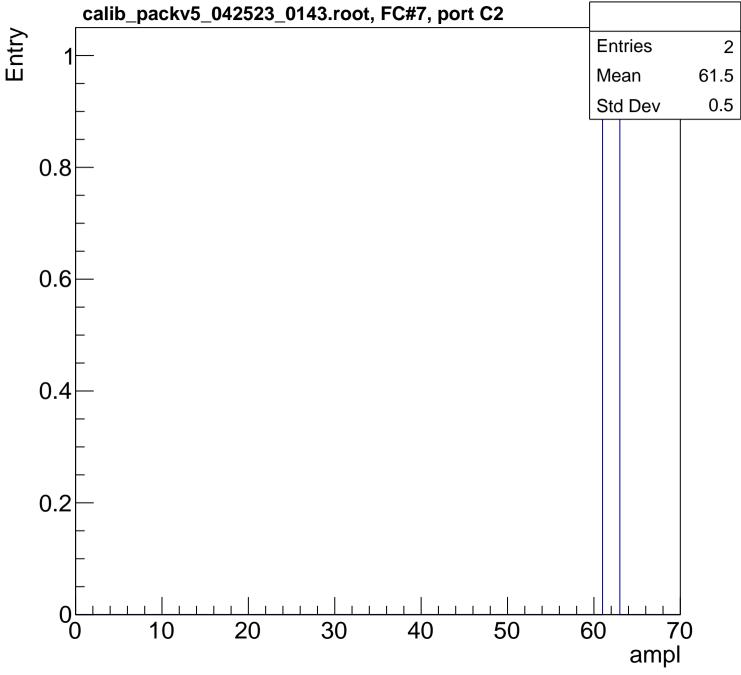




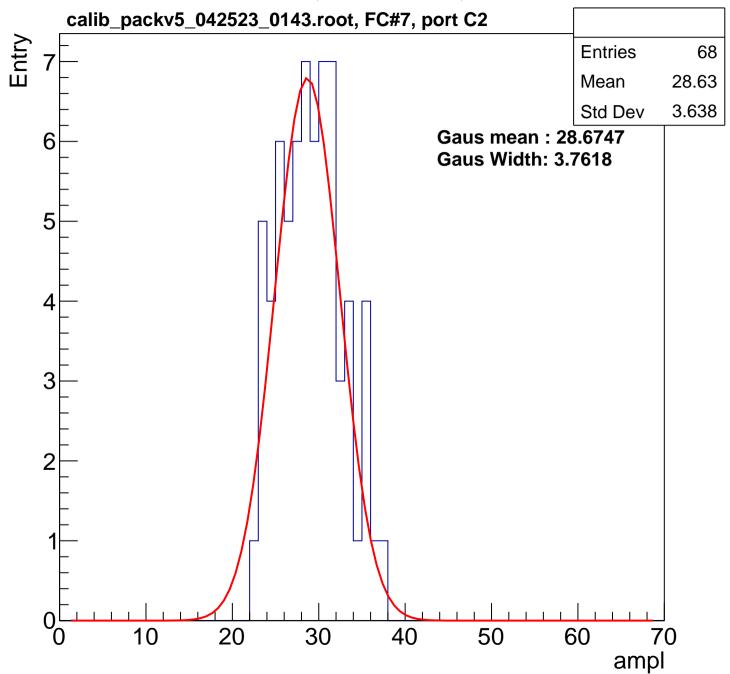


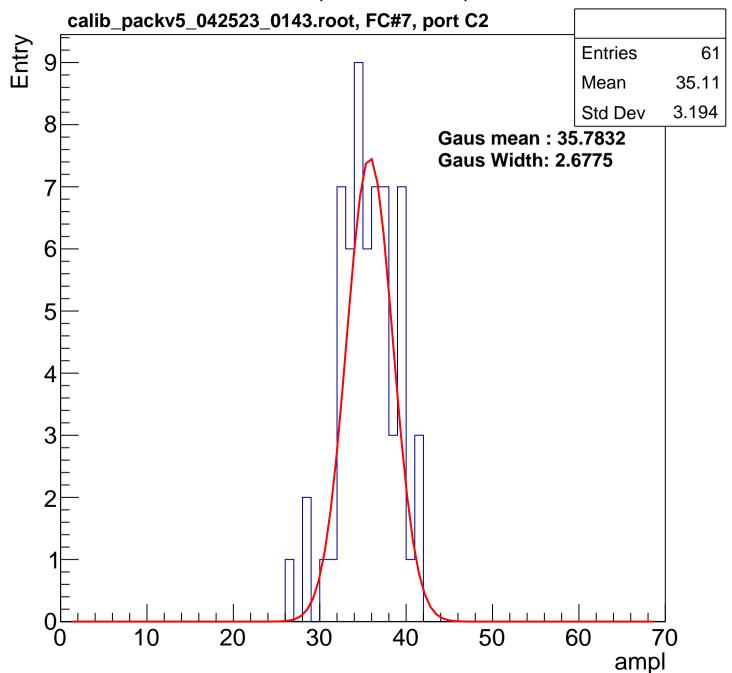


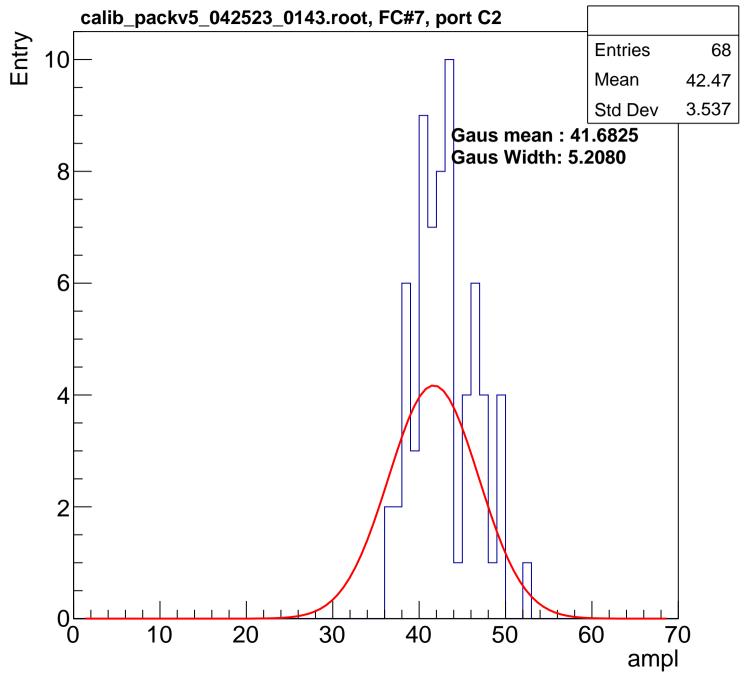


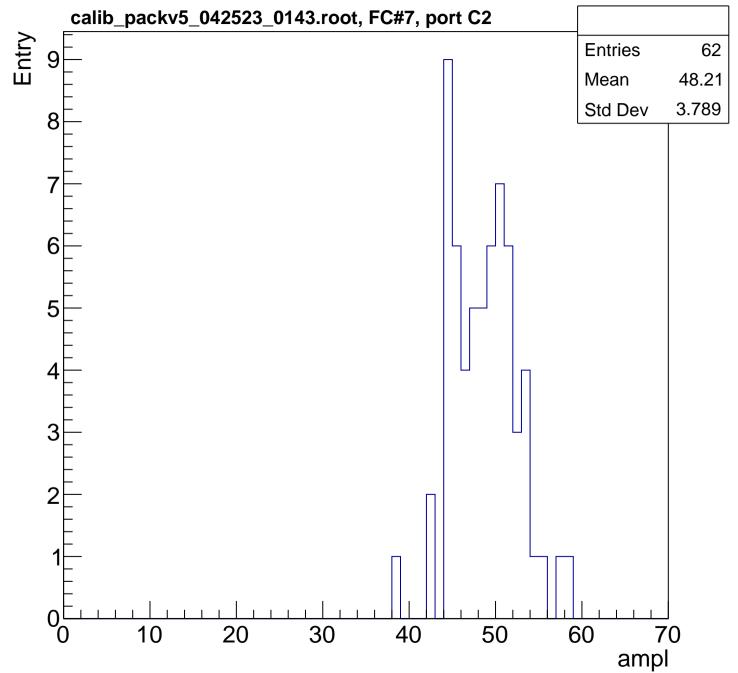


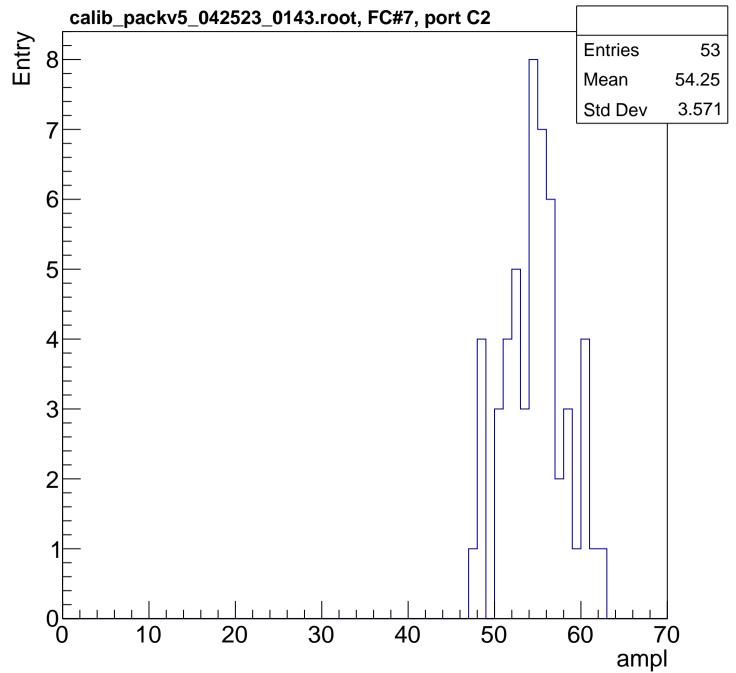
B1L103S, U4-ch11, adc7 calib_packv5_042523_0143.root, FC#7, port C2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

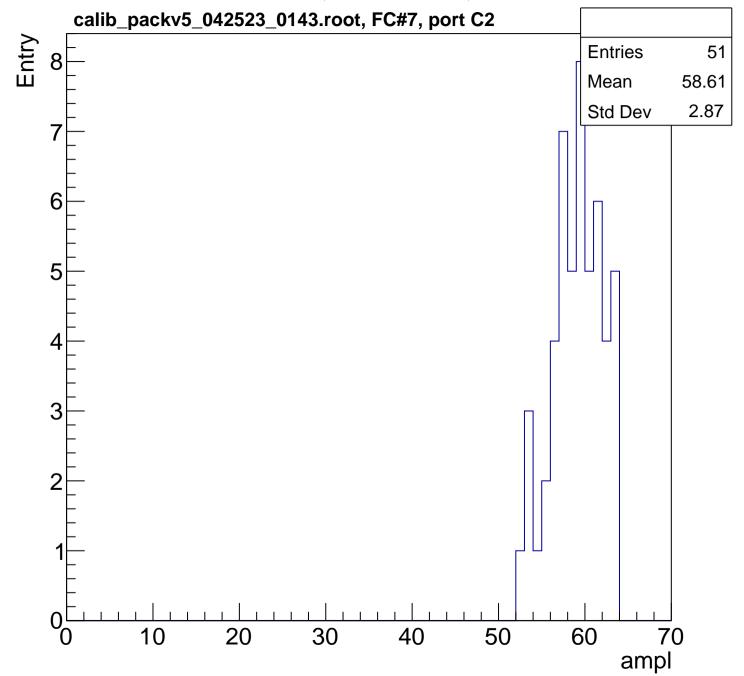


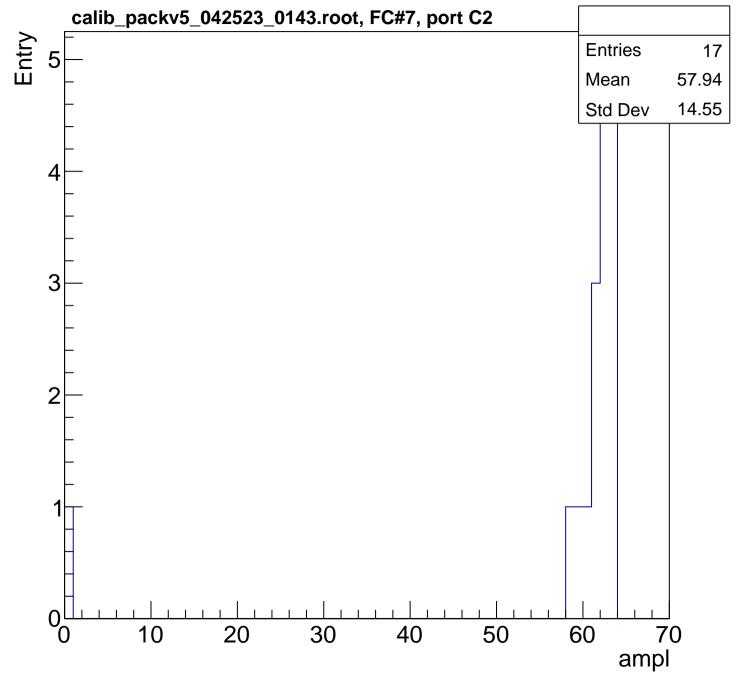


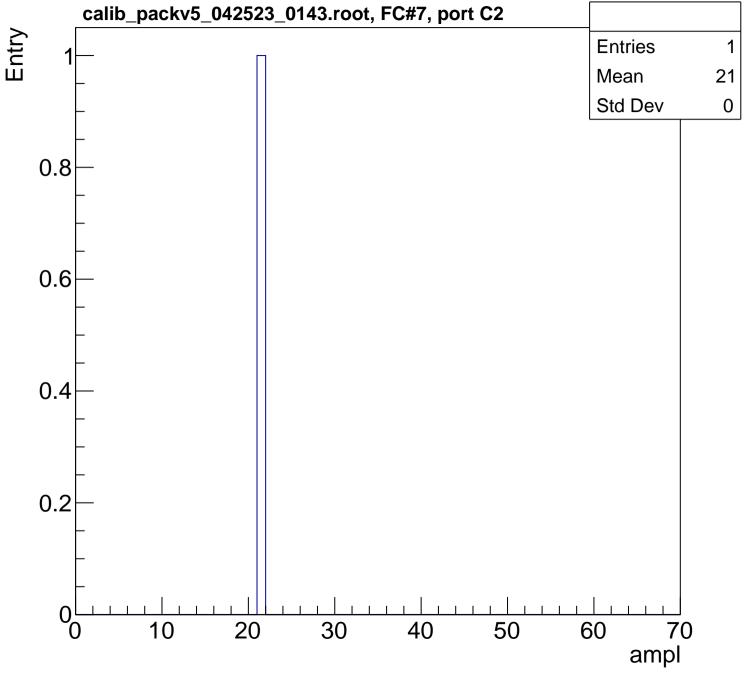


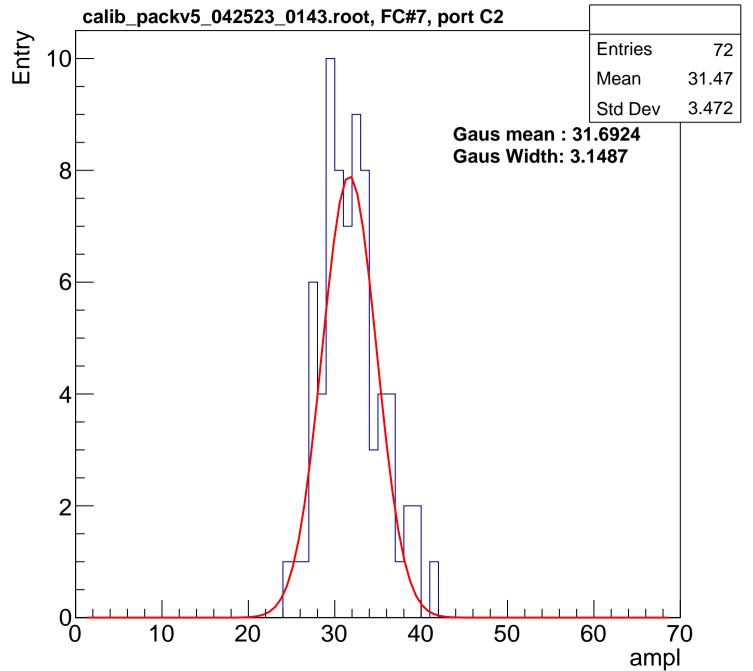


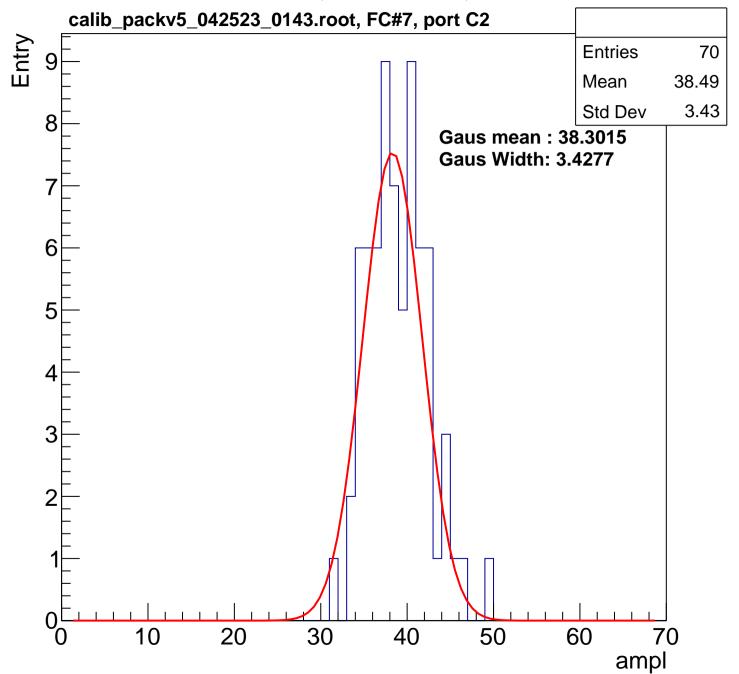


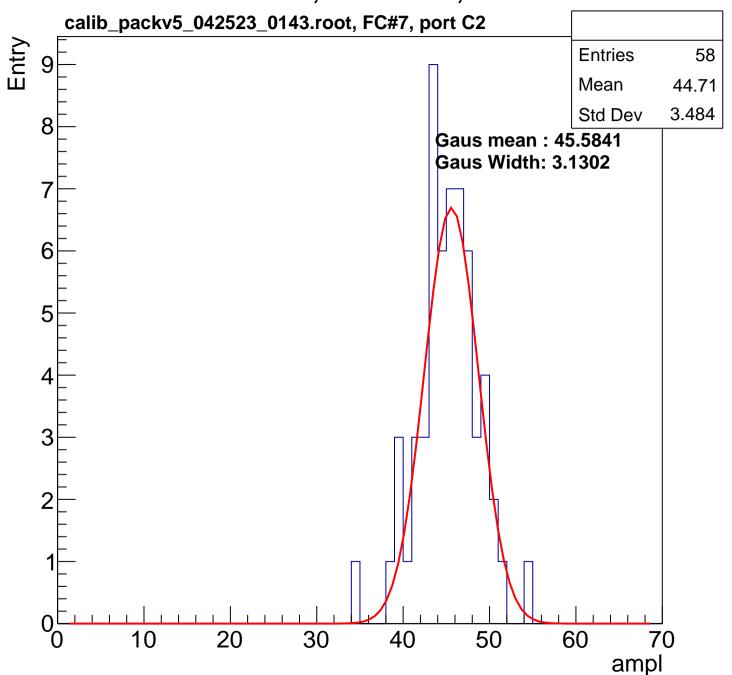


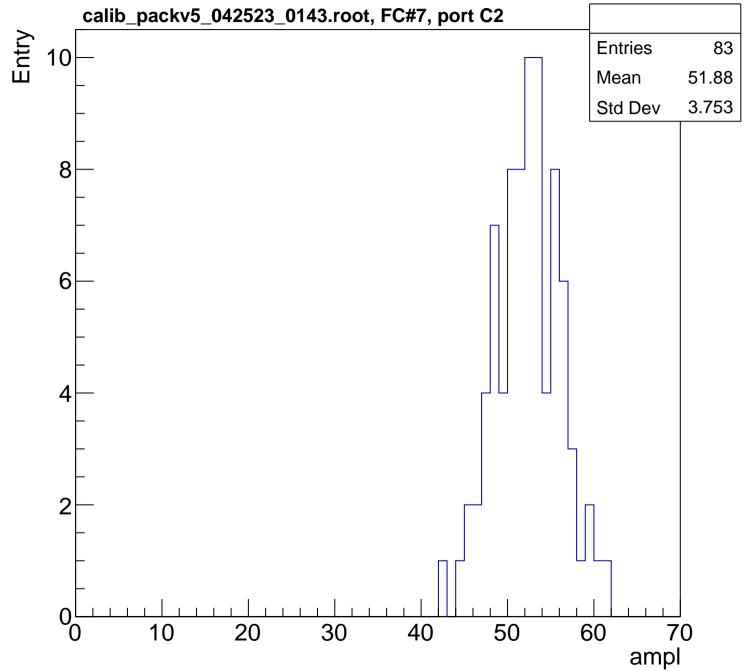


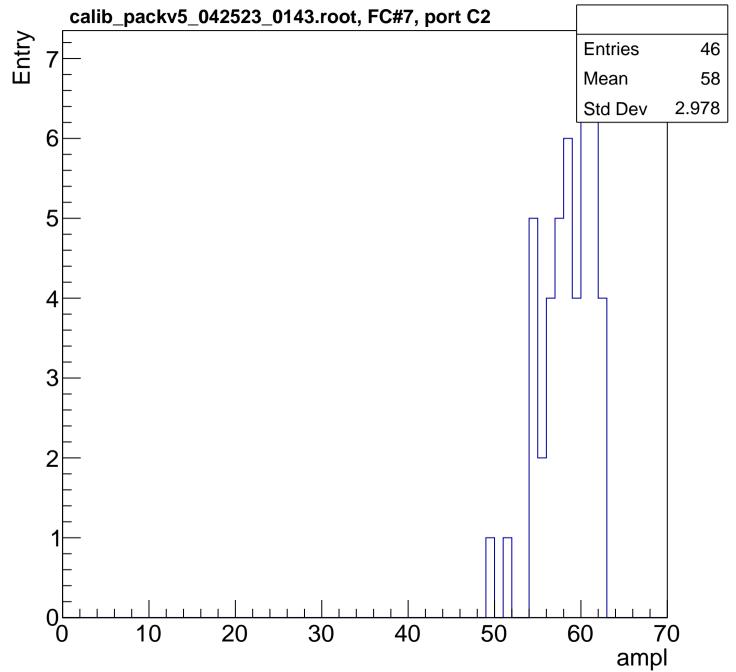


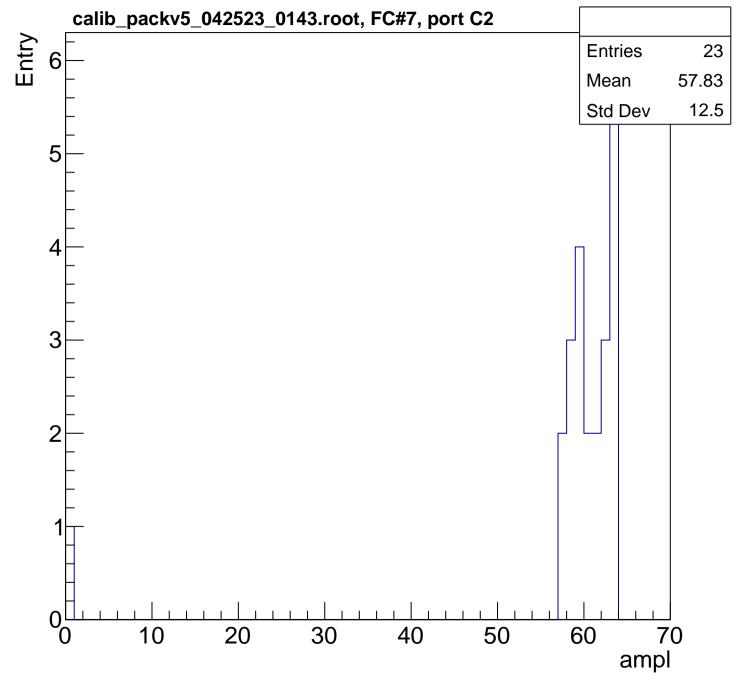


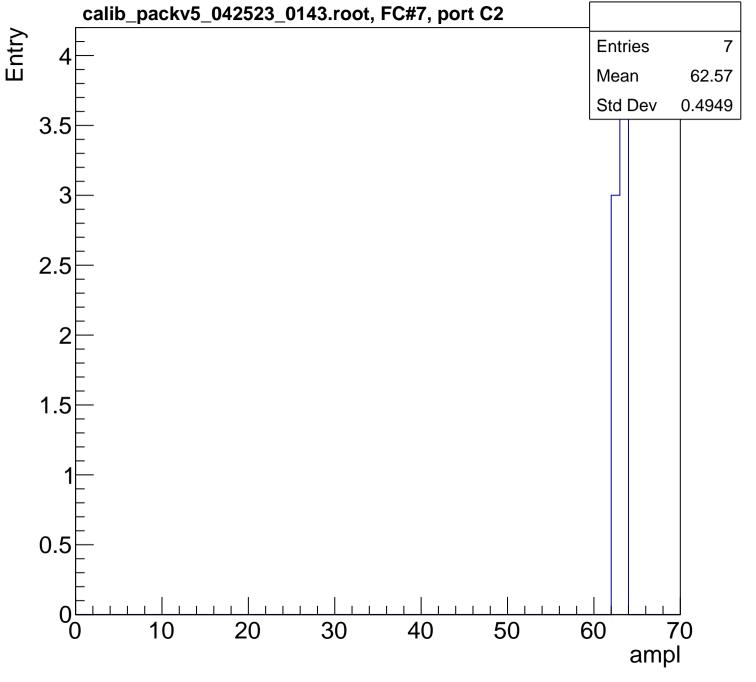




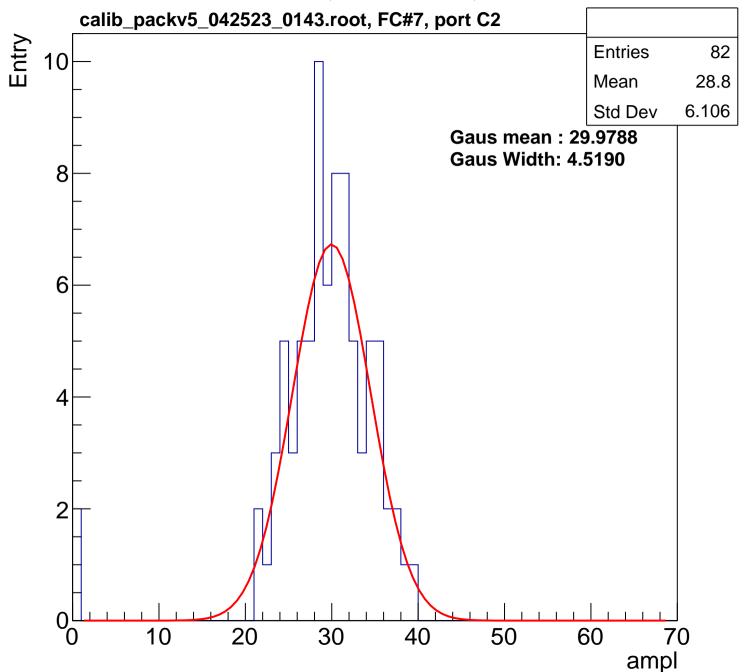


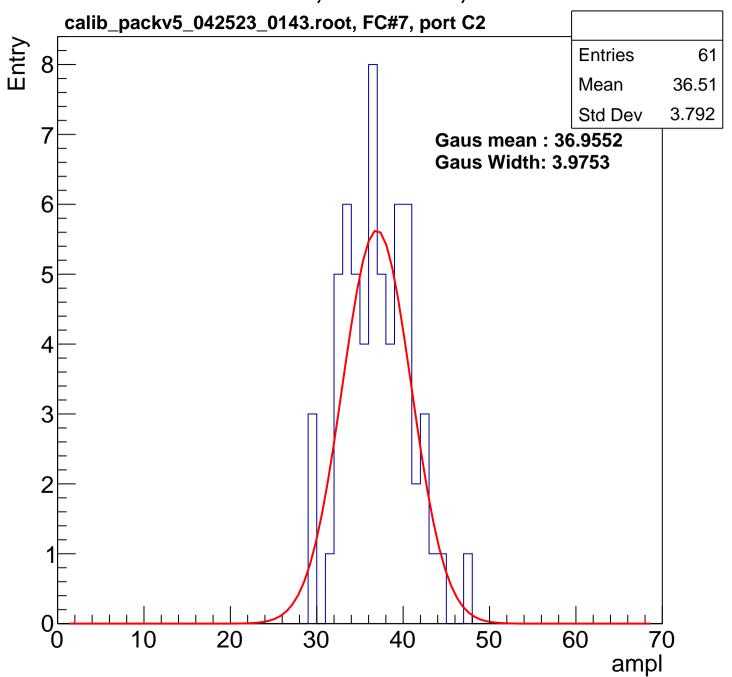


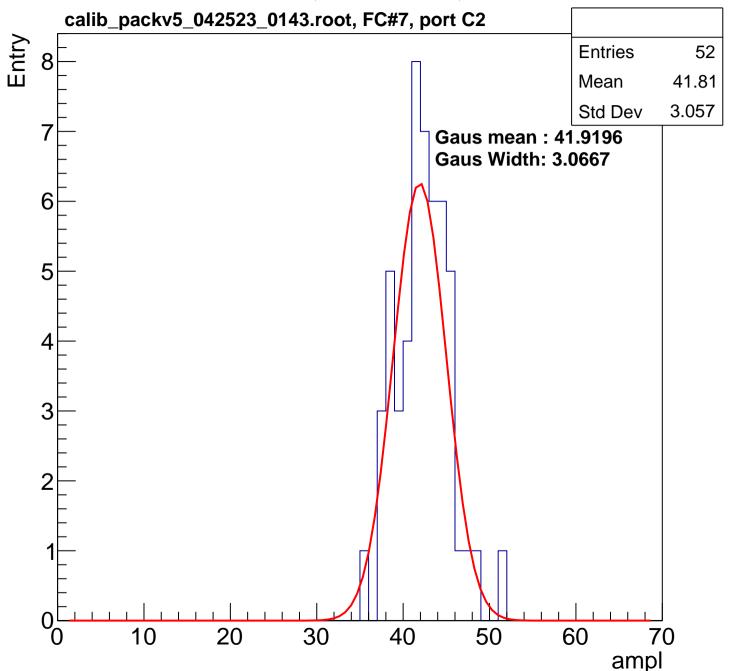


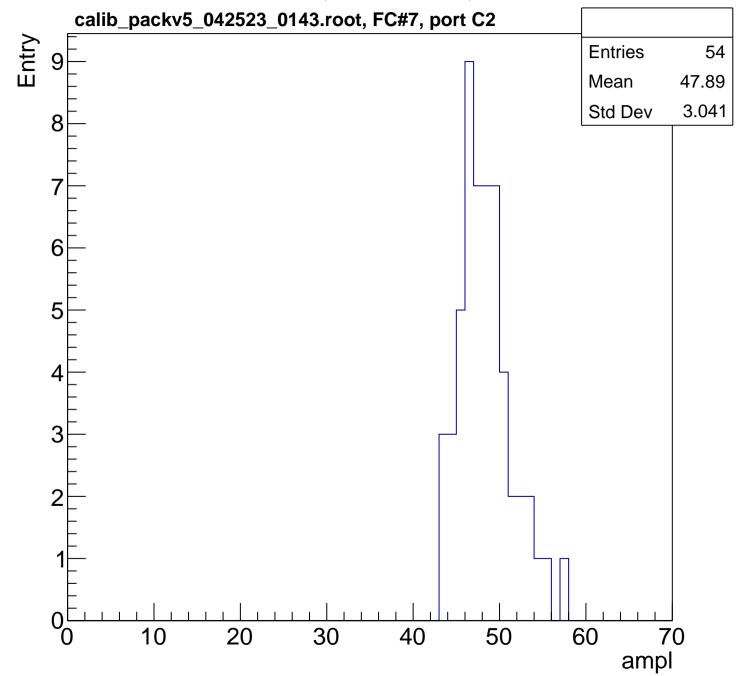


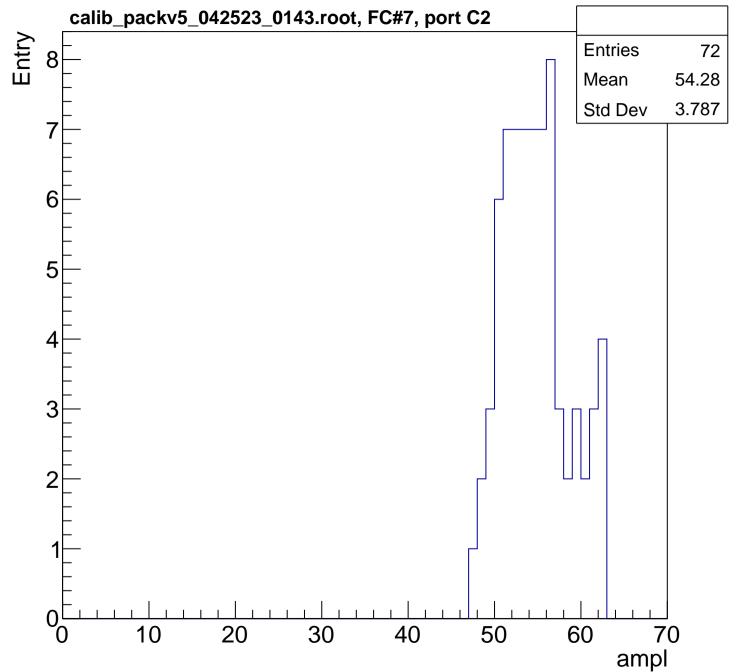
B1L103S, U4-ch13, adc7 calib_packv5_042523_0143.root, FC#7, port C2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

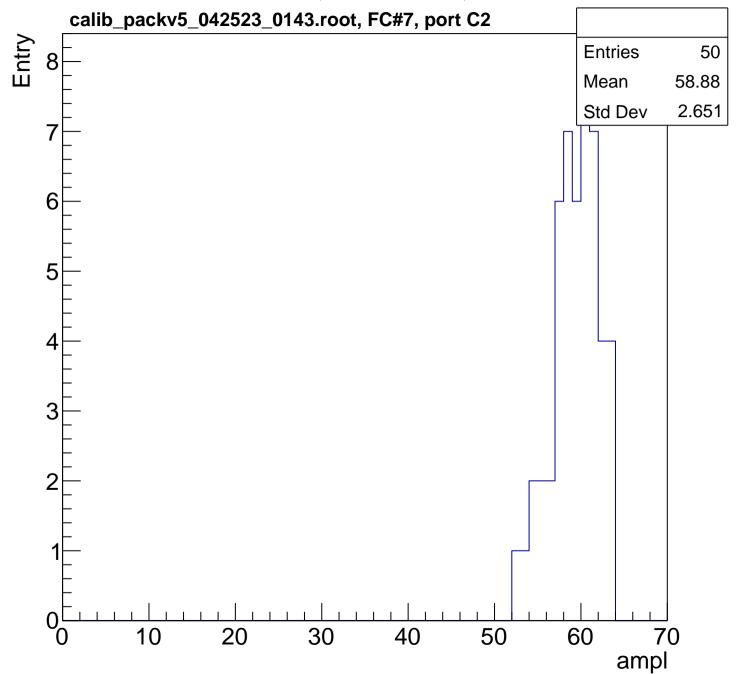


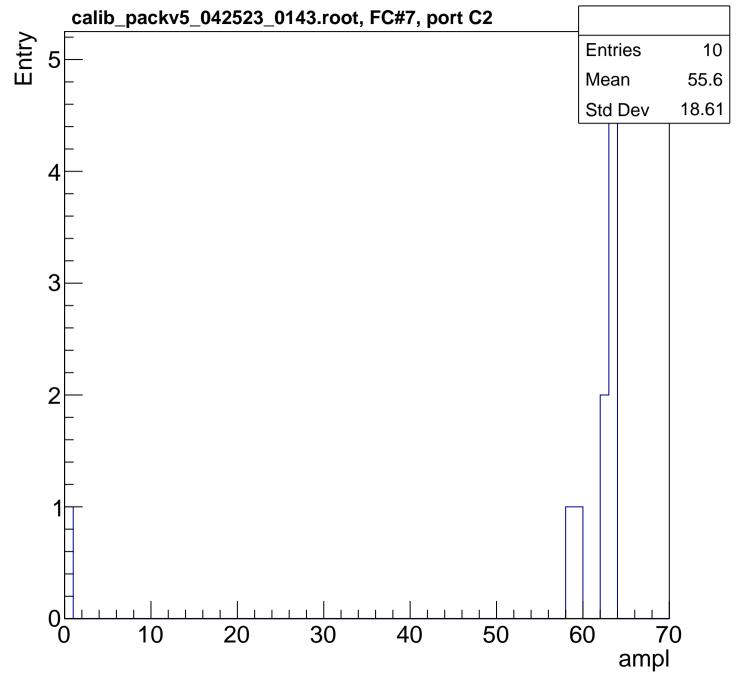


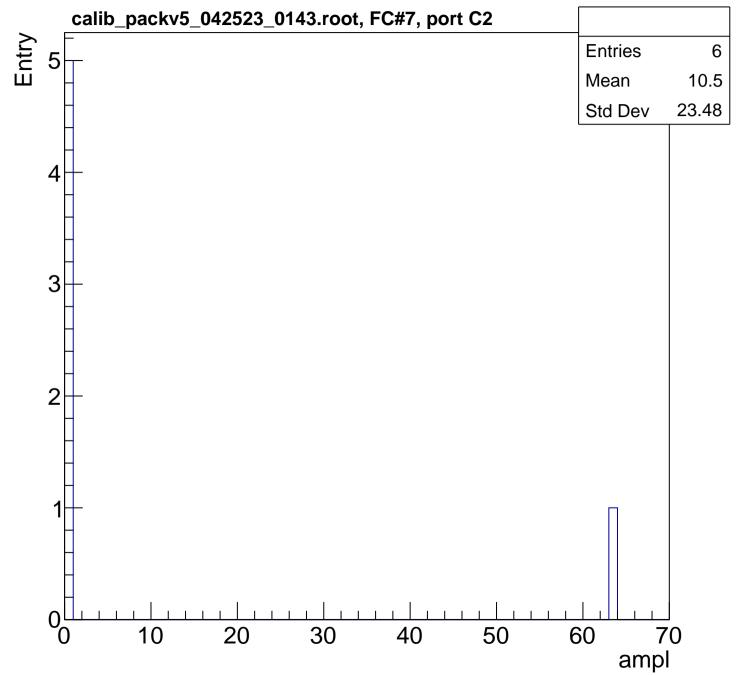


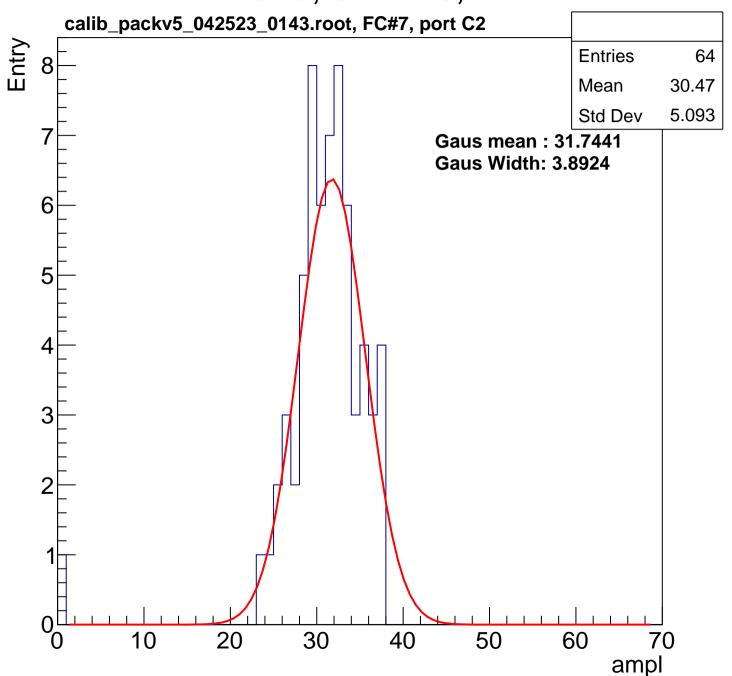


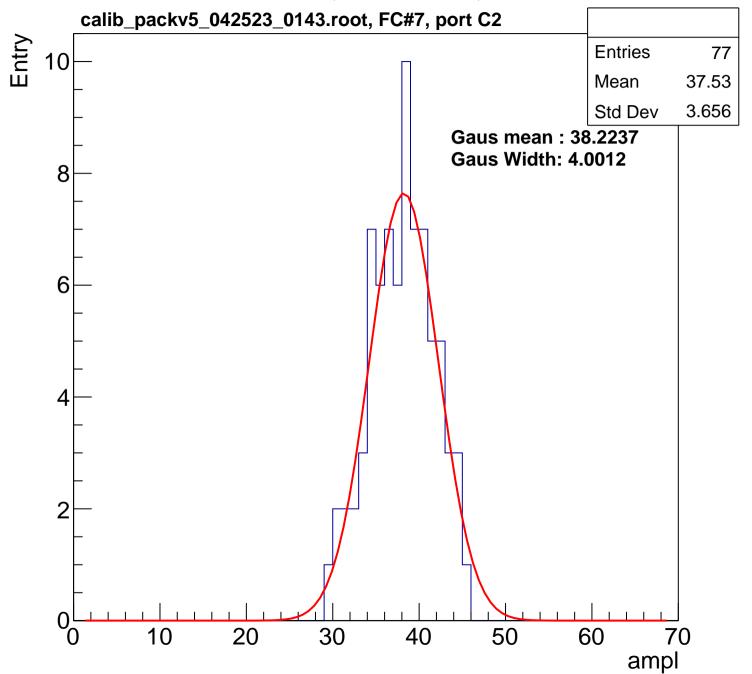


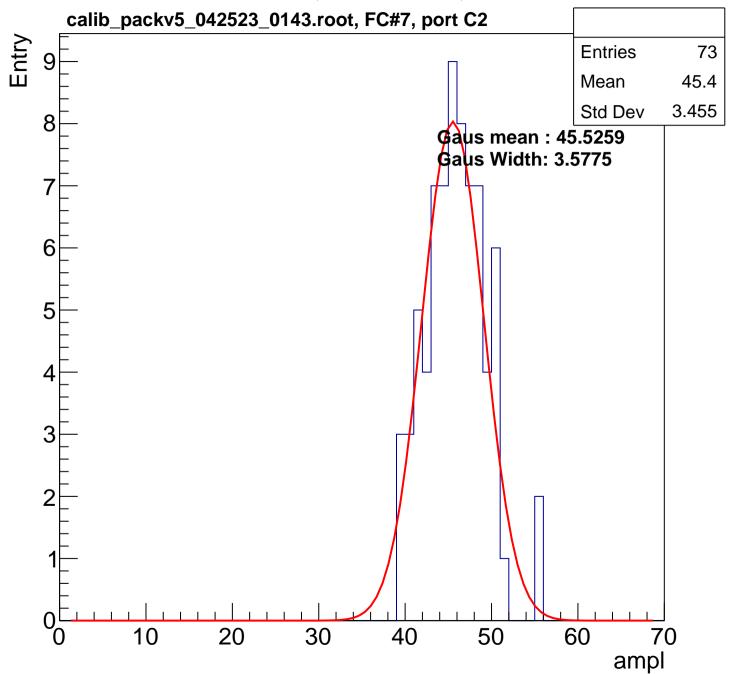


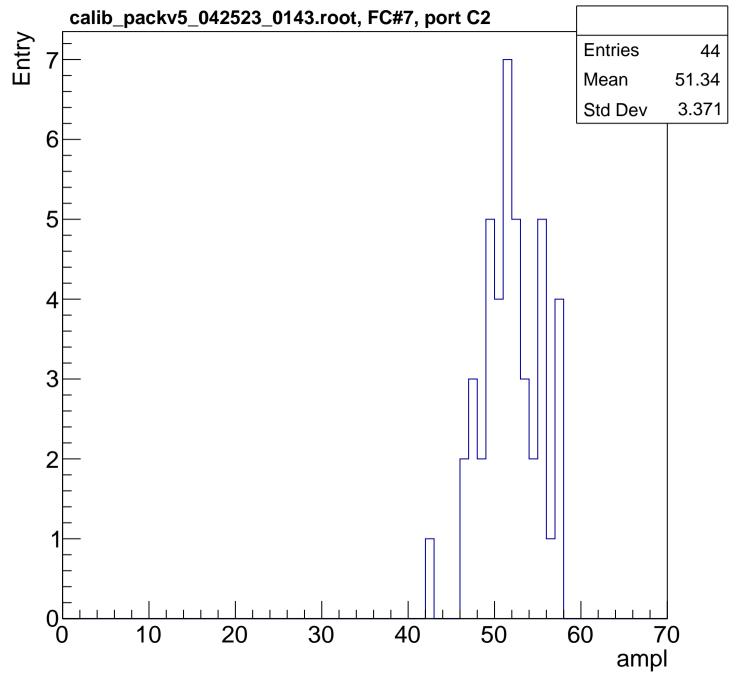


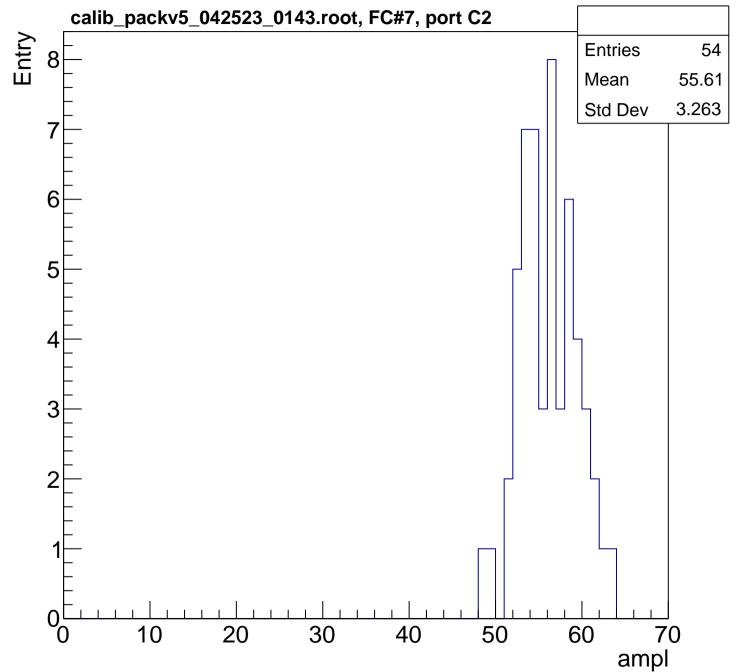


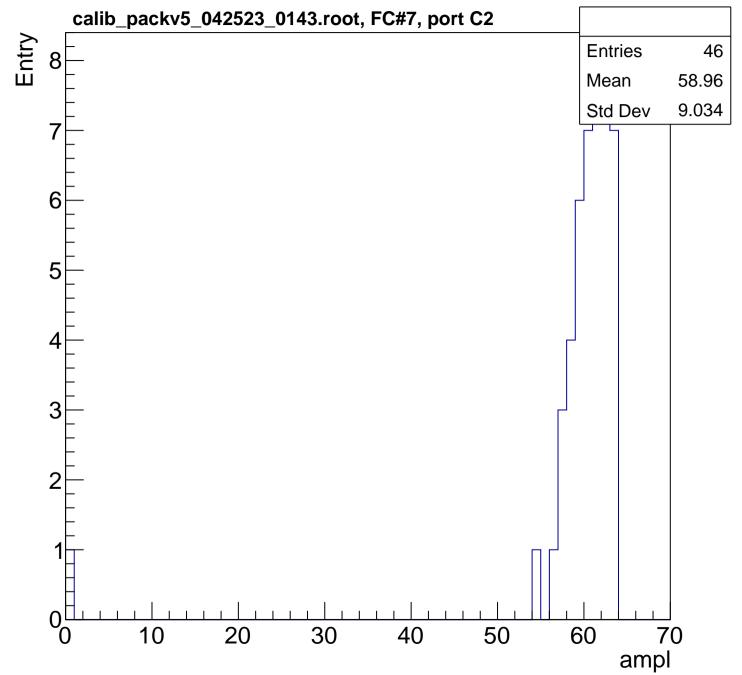


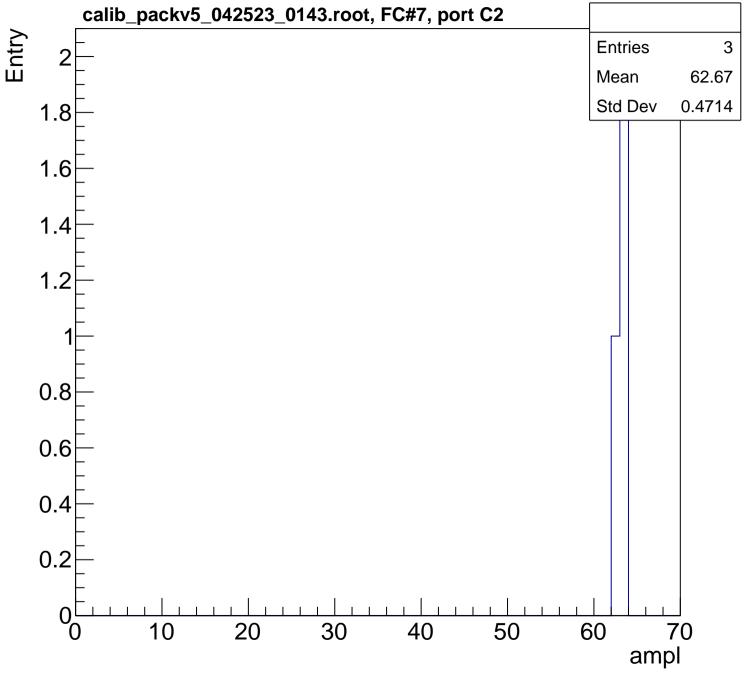


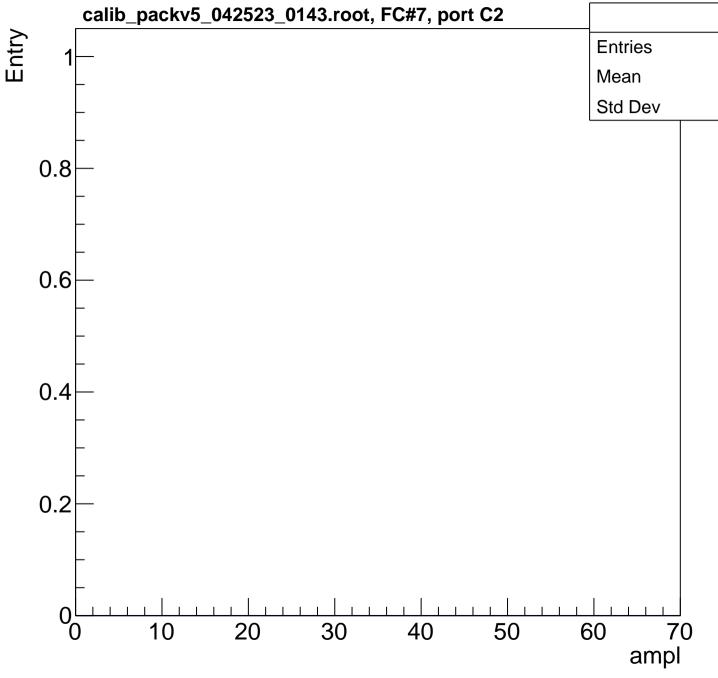


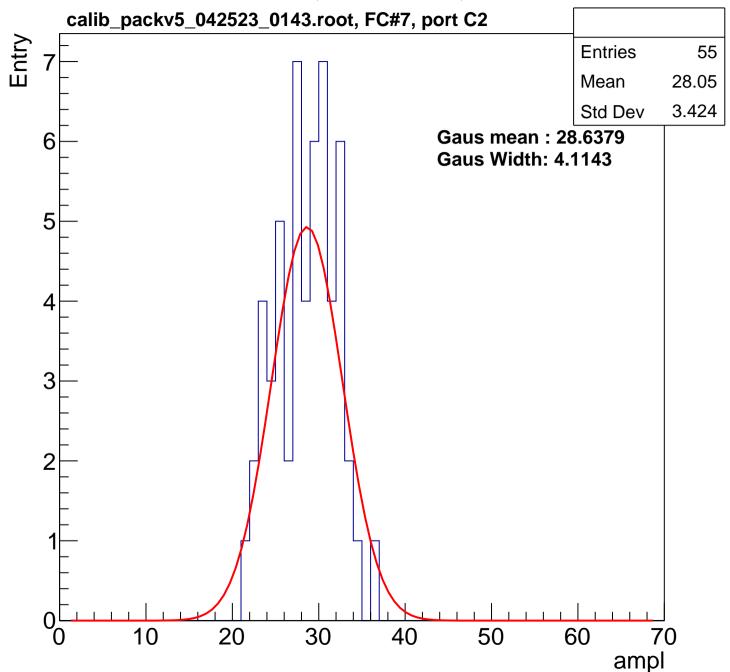


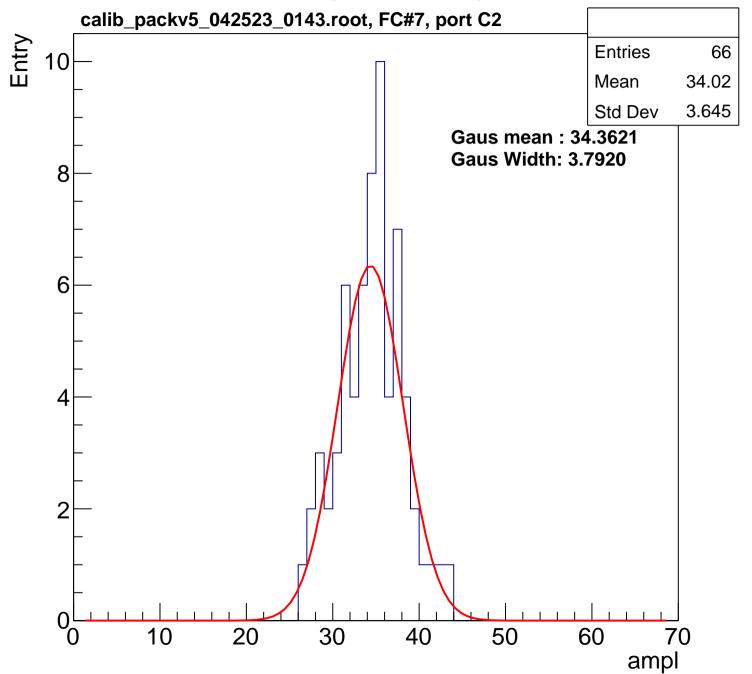


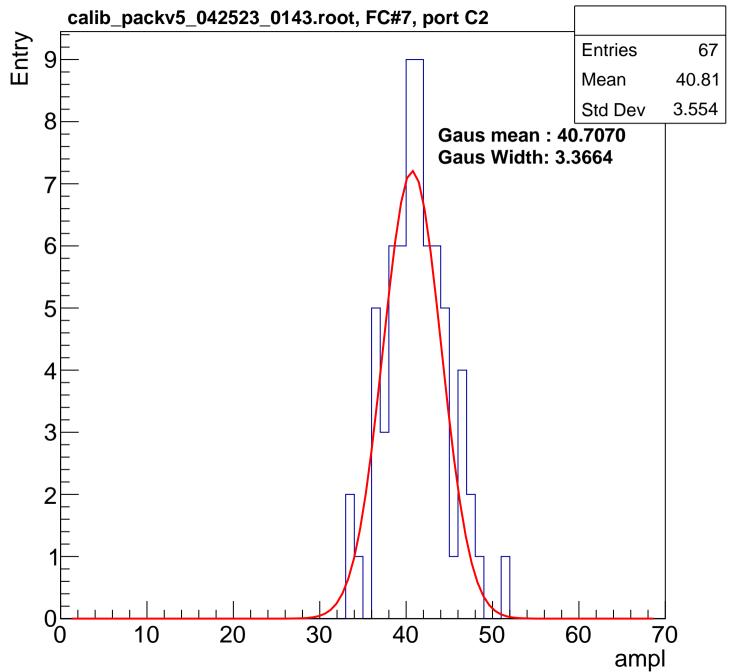


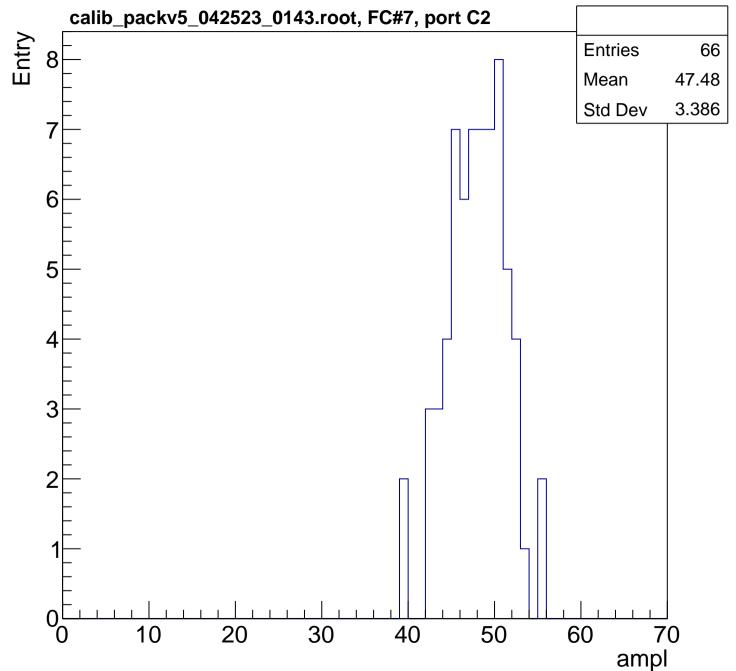


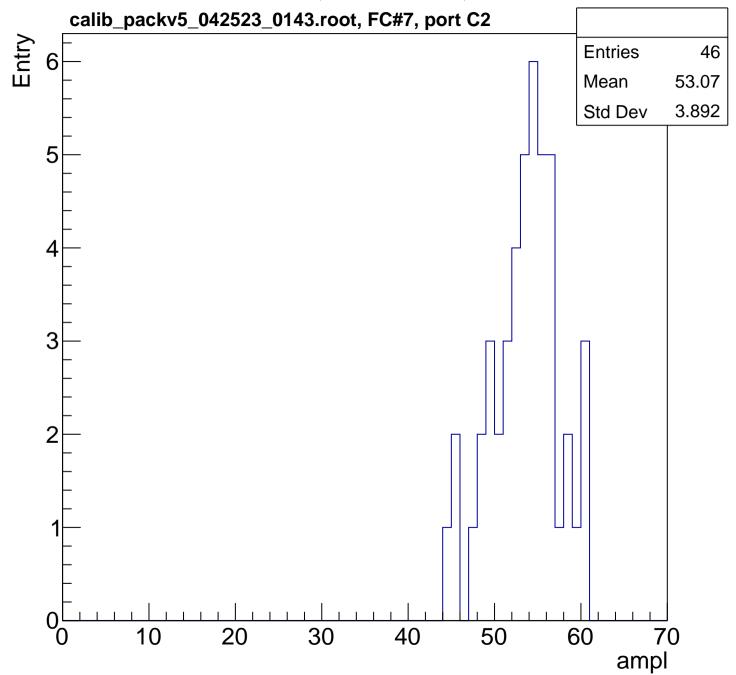


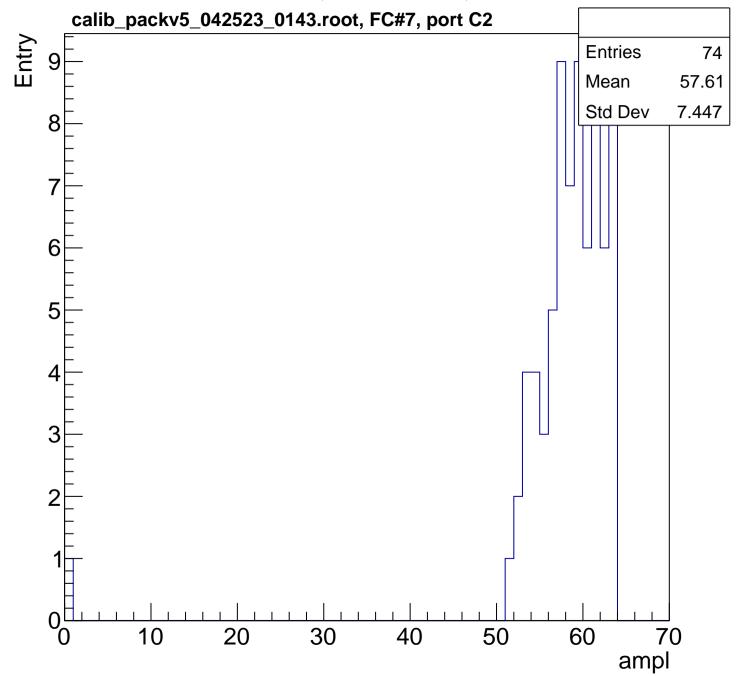


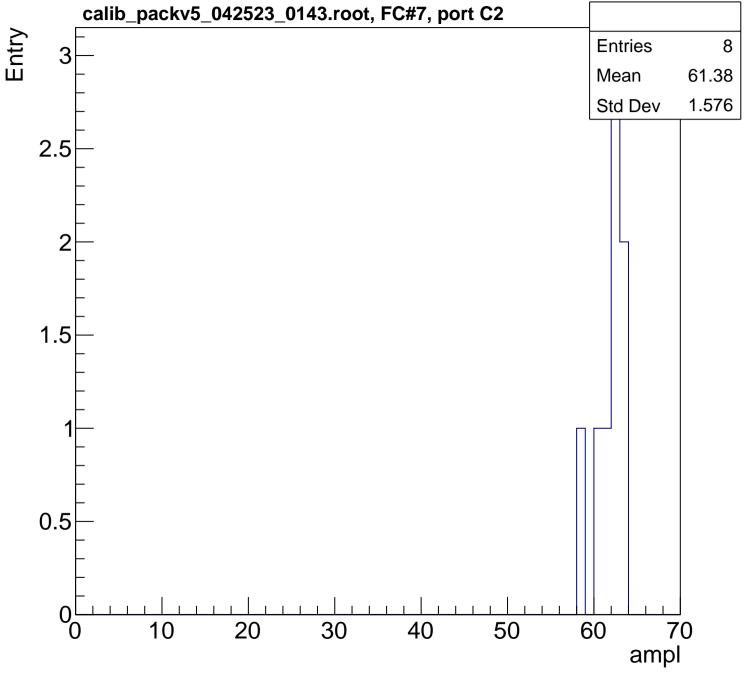


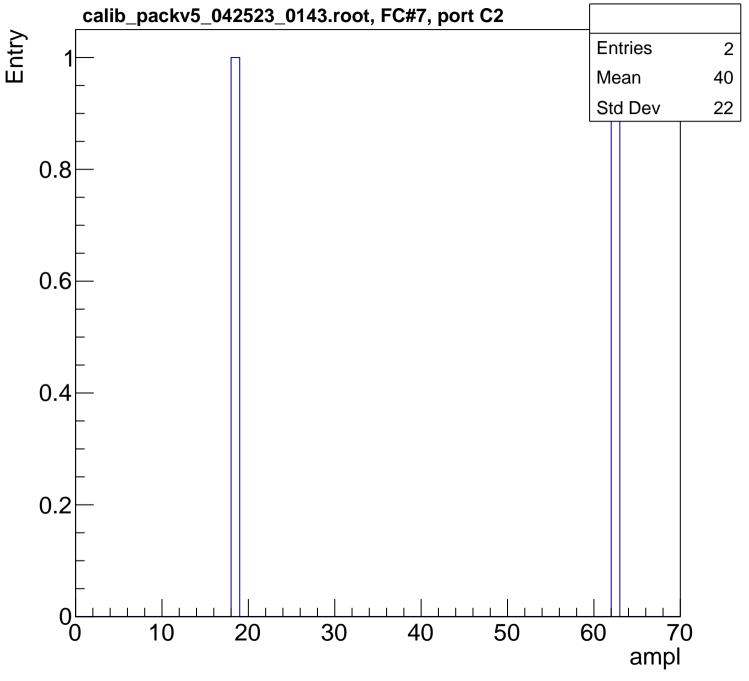


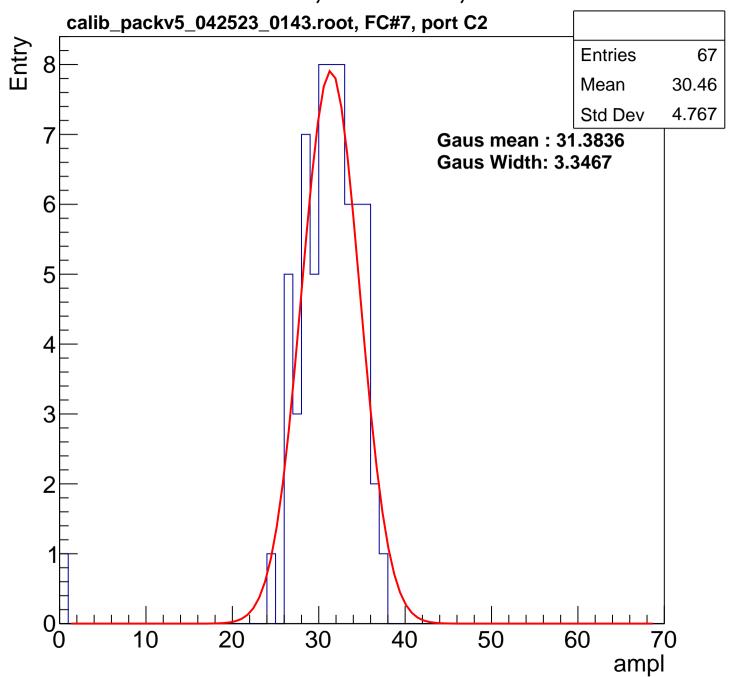


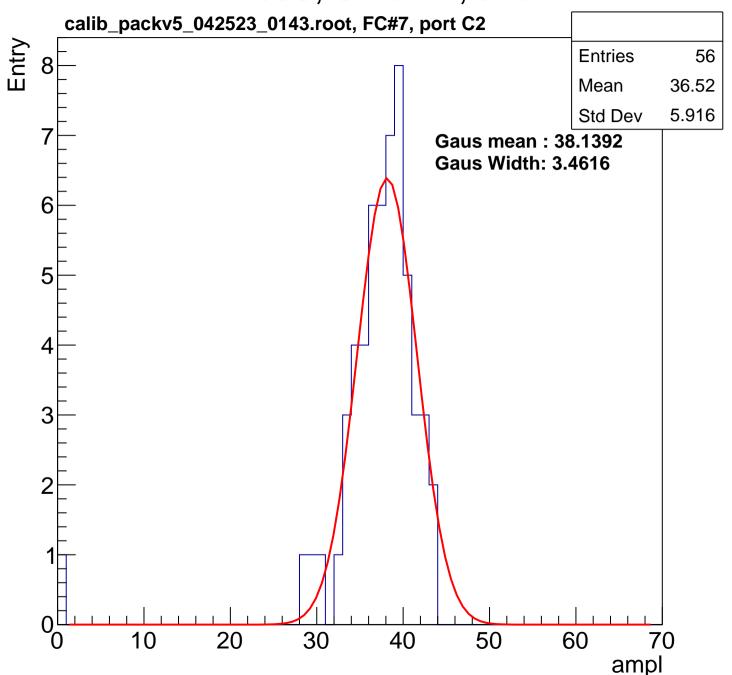


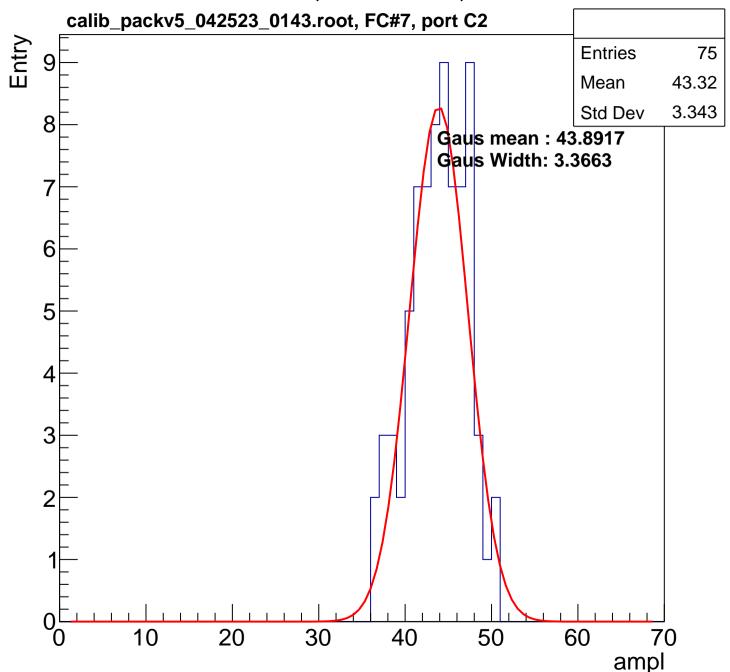


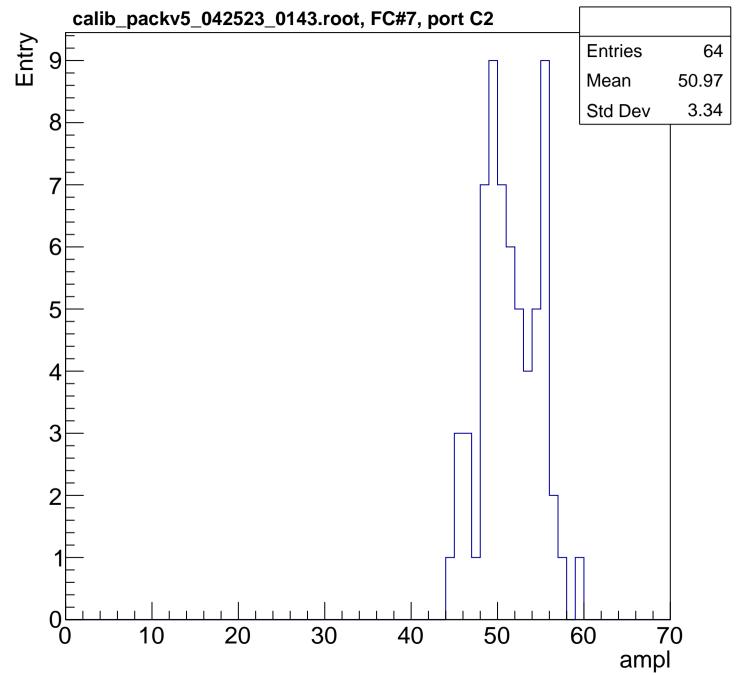


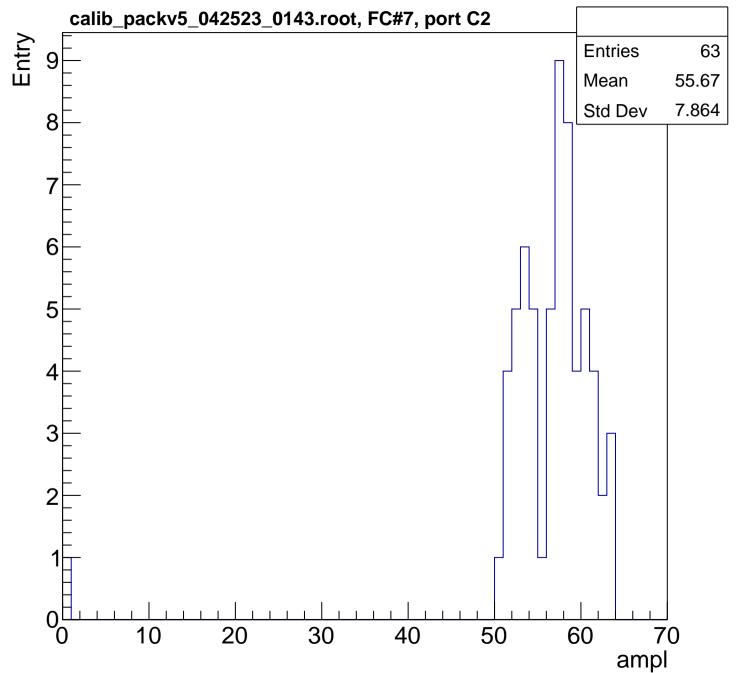


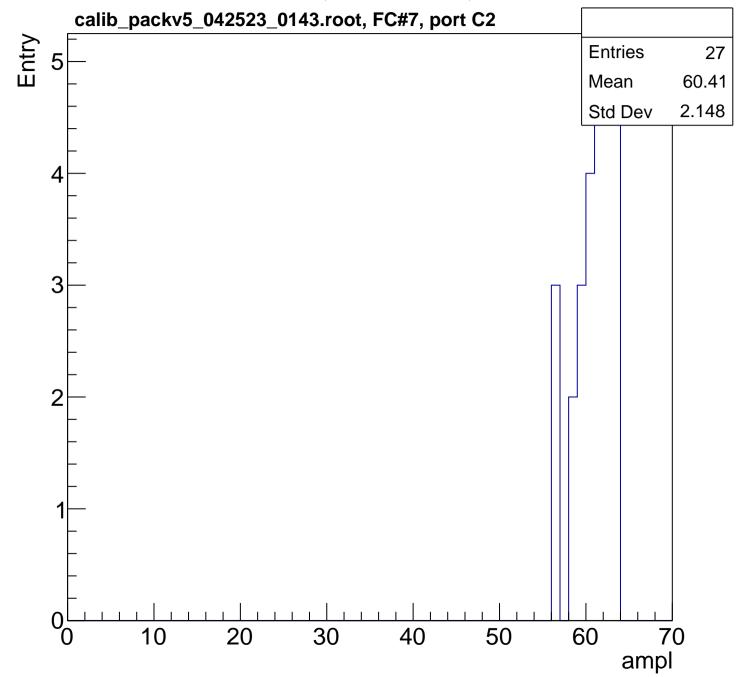


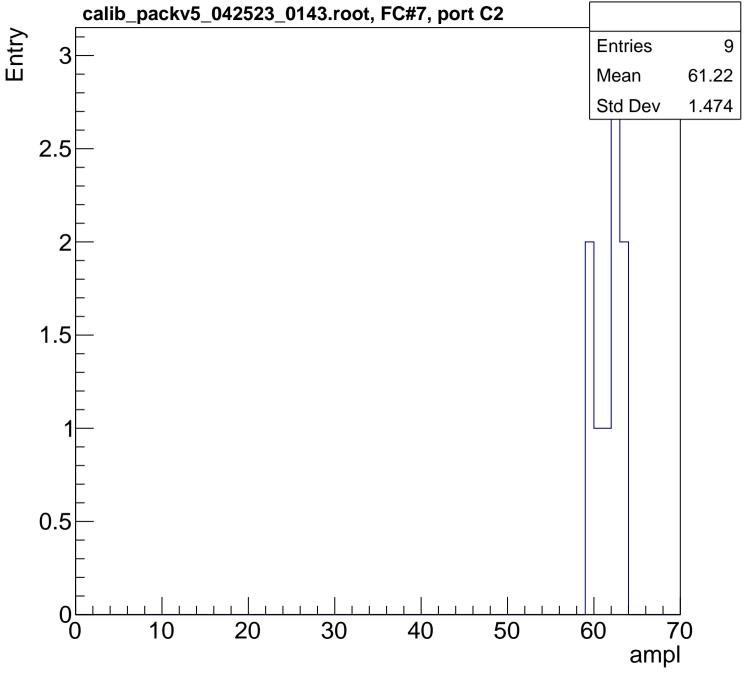


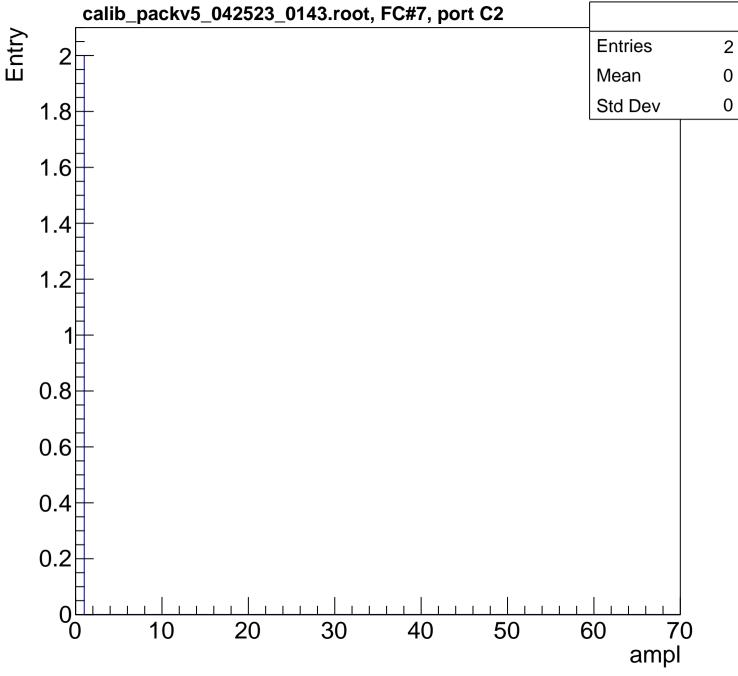


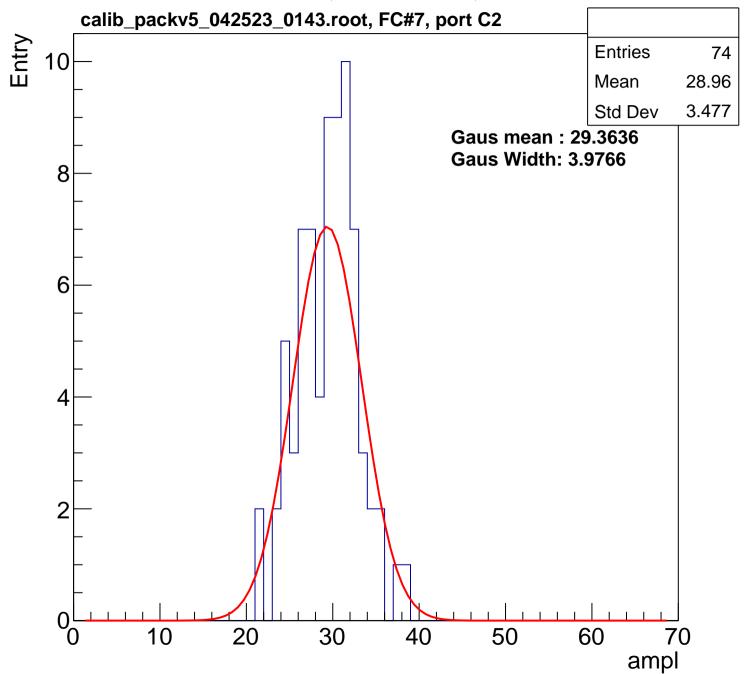


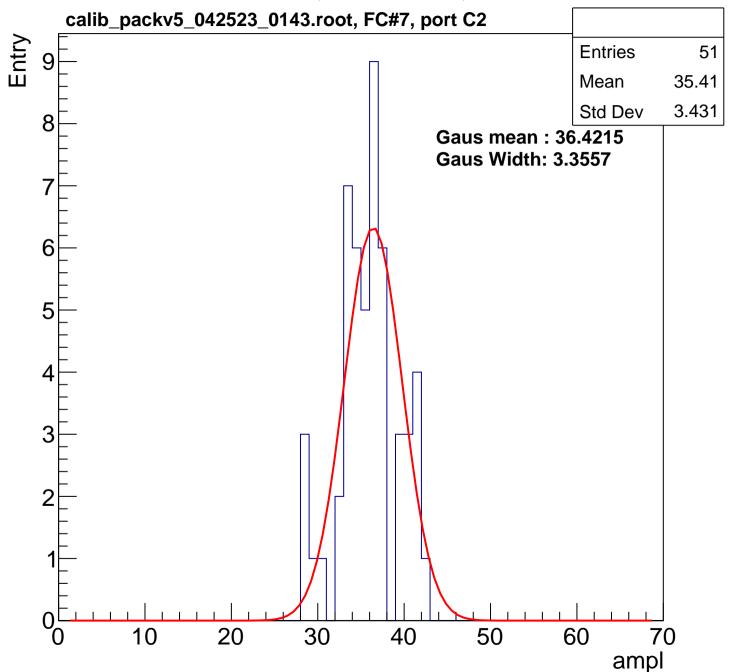


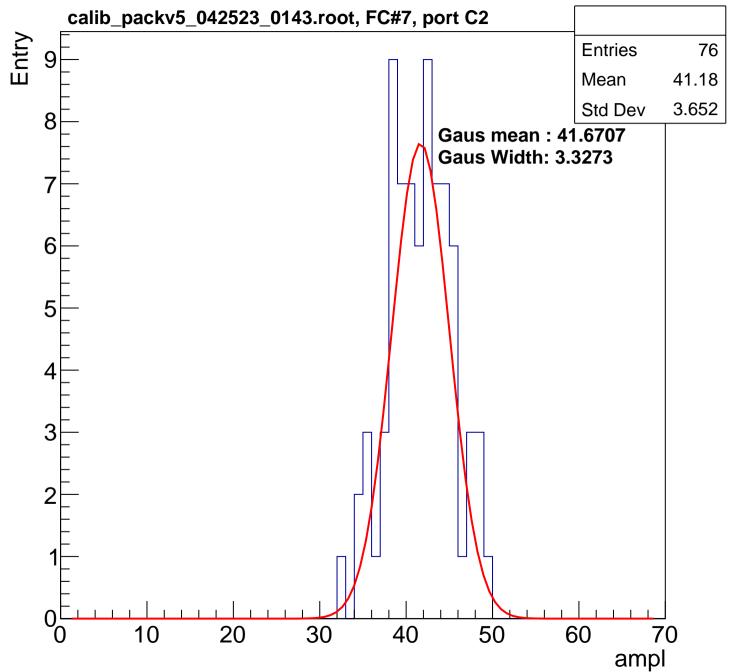


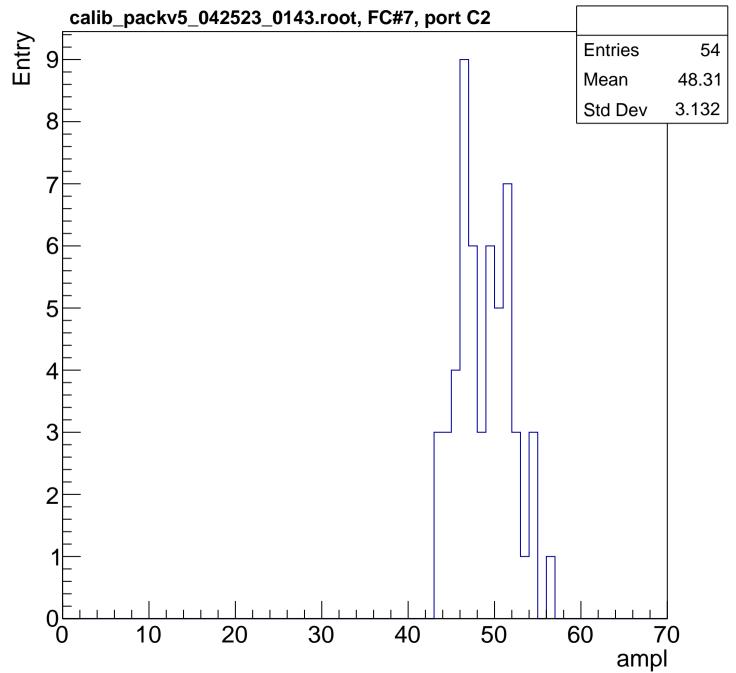


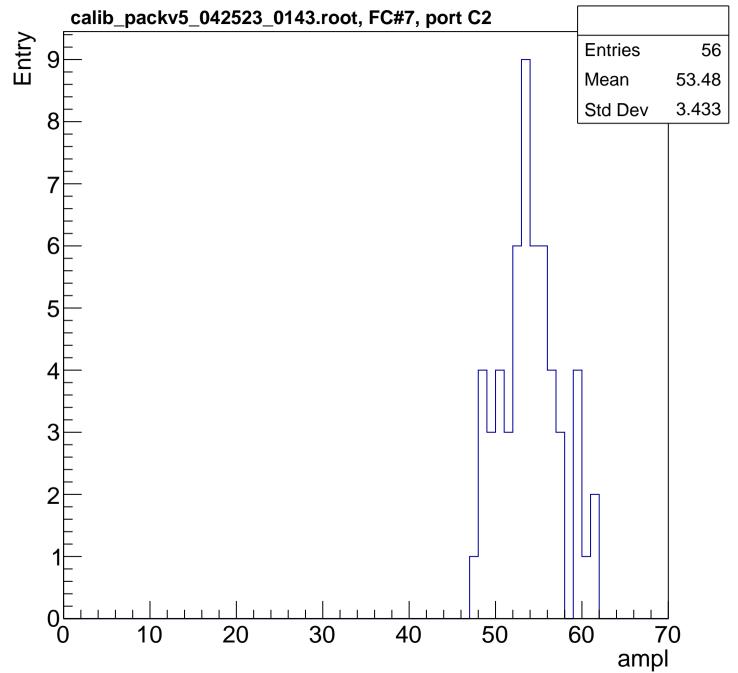


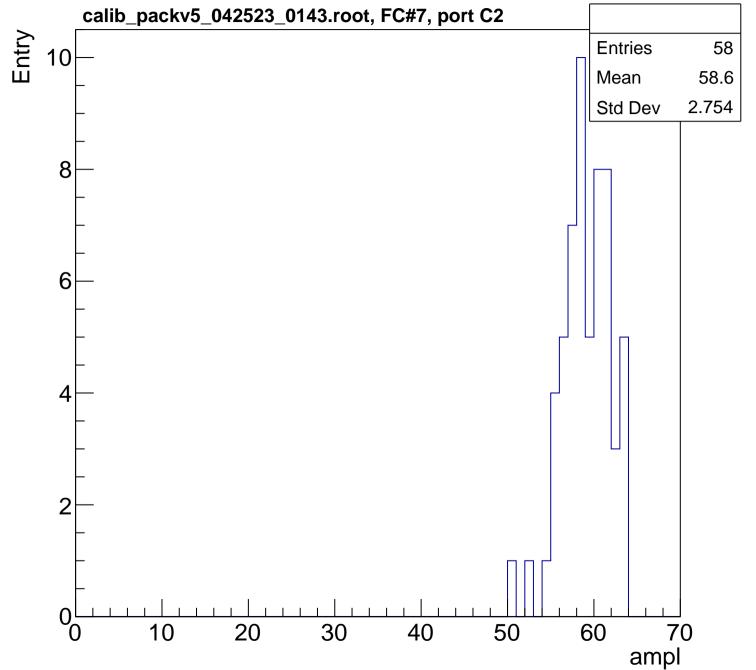


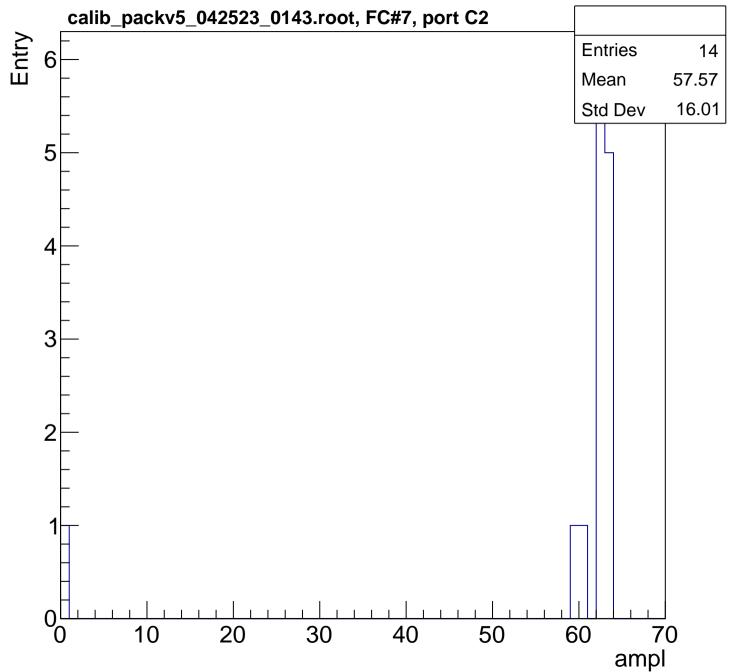


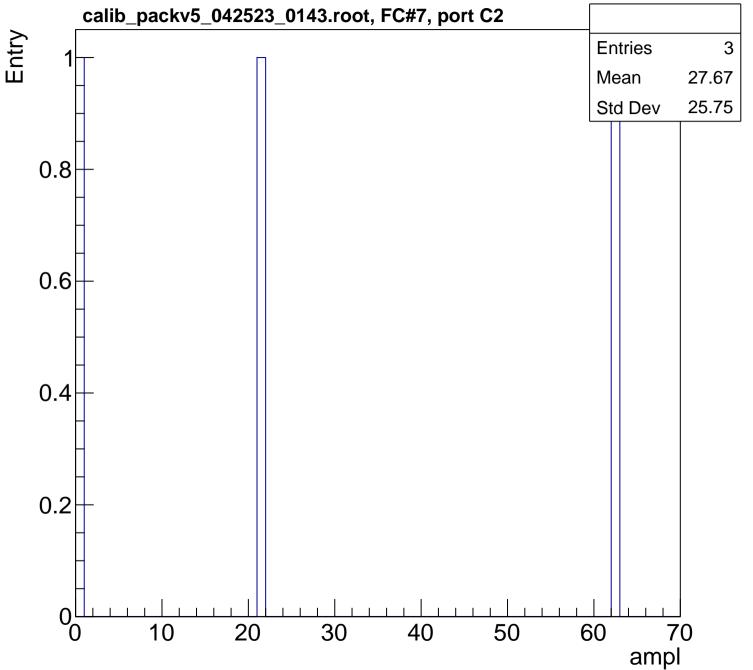


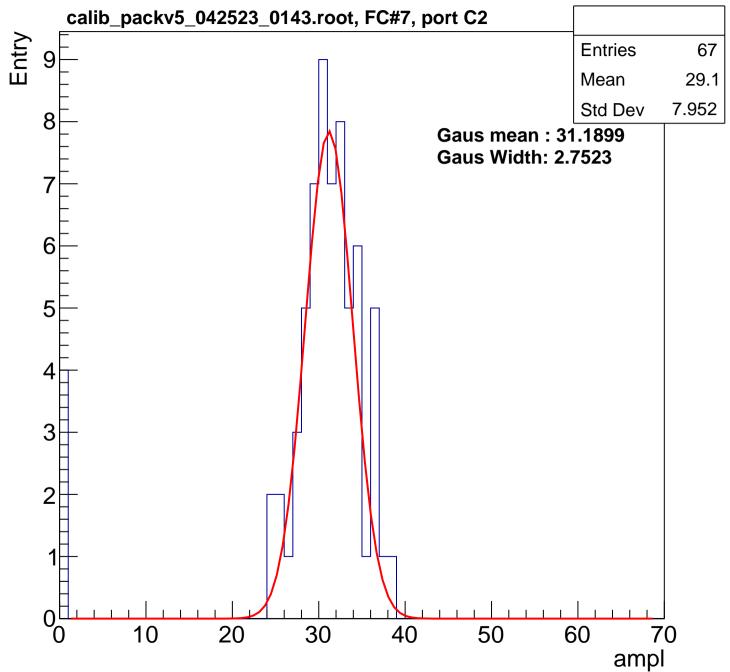


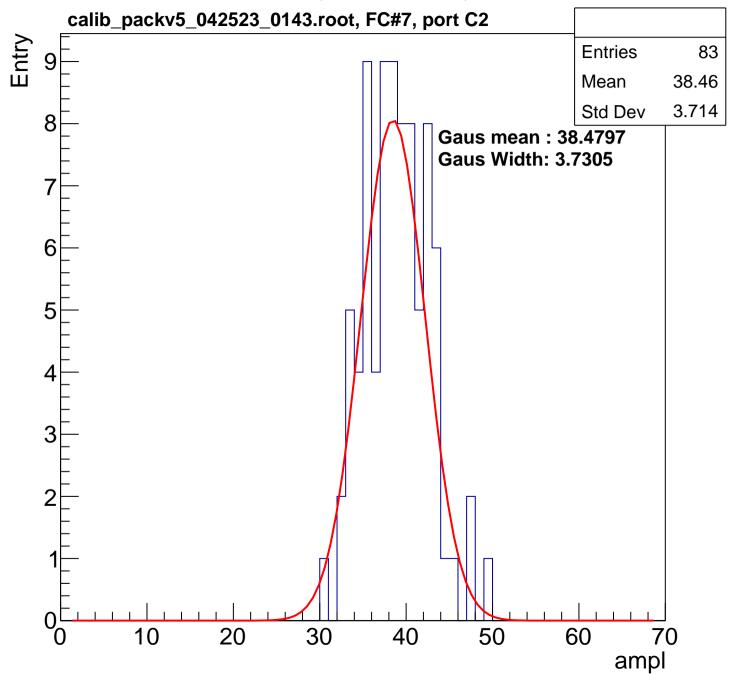


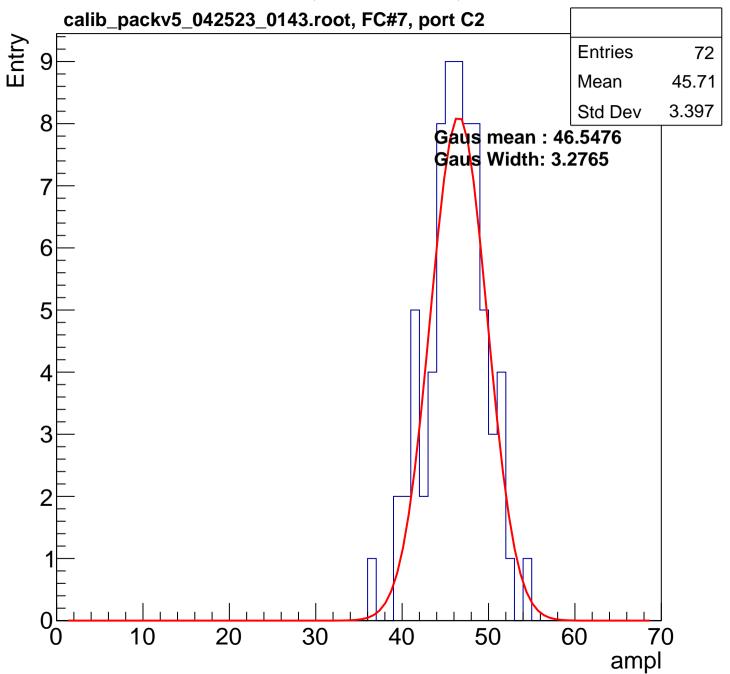


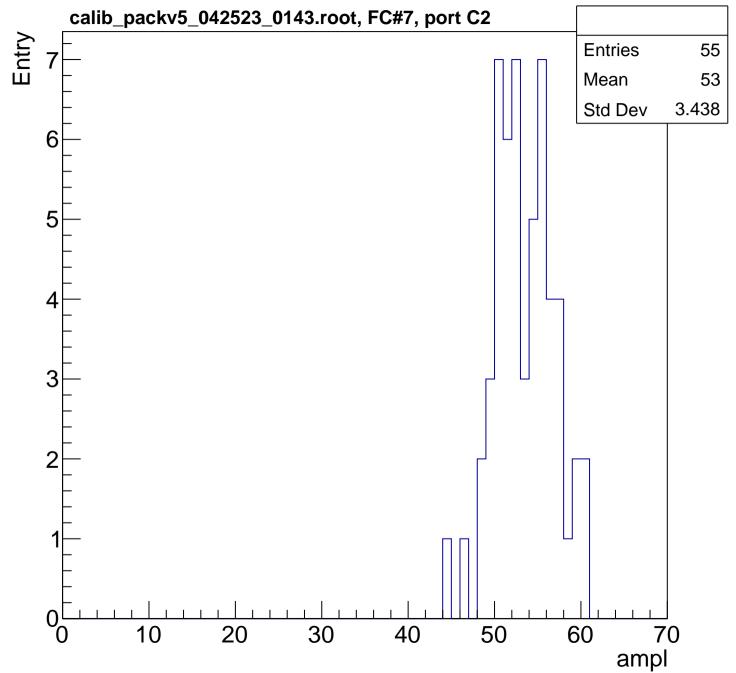


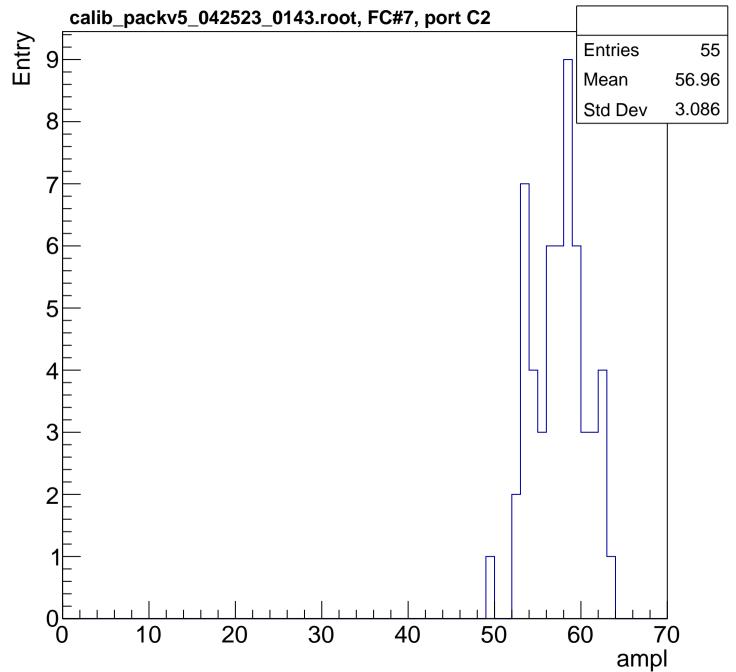


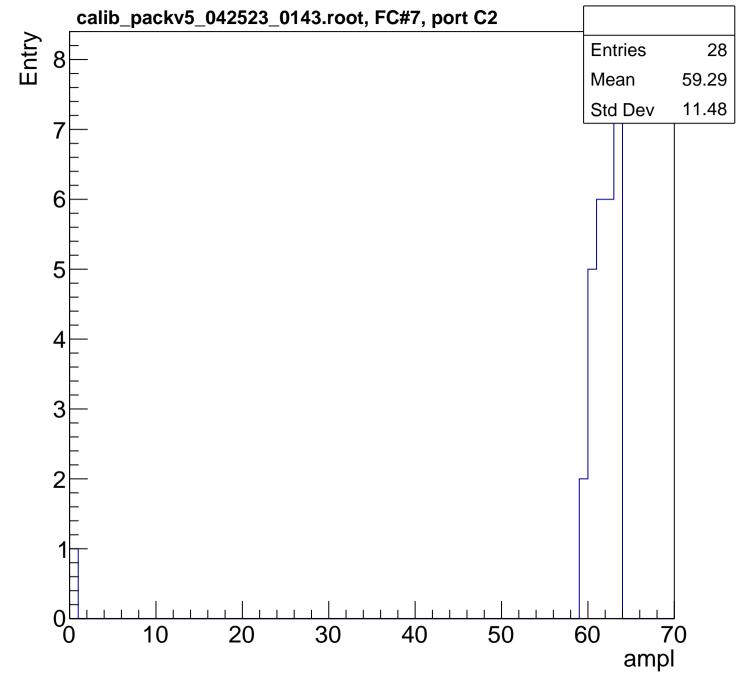


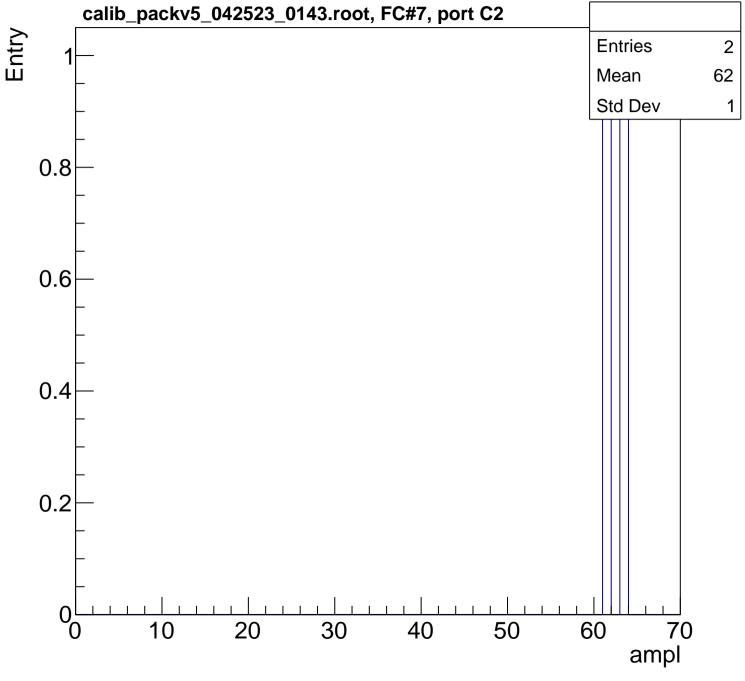




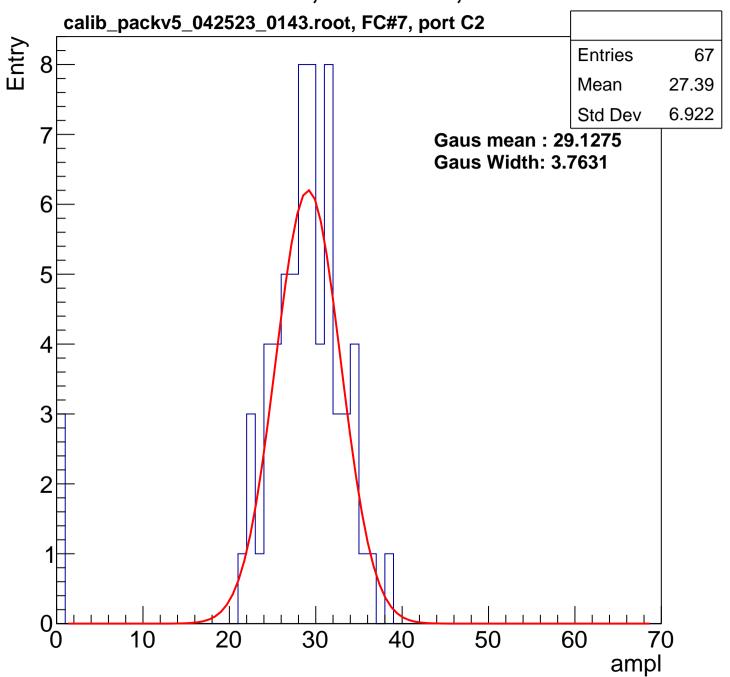


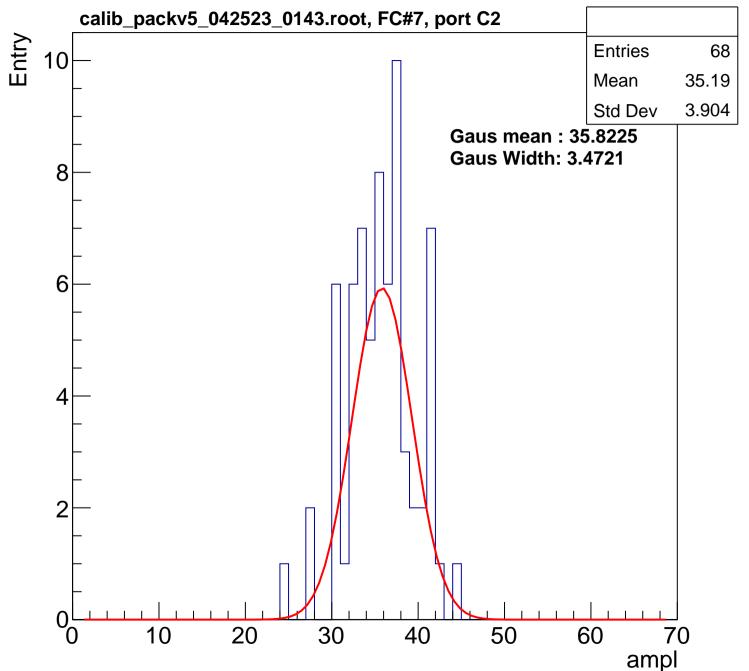


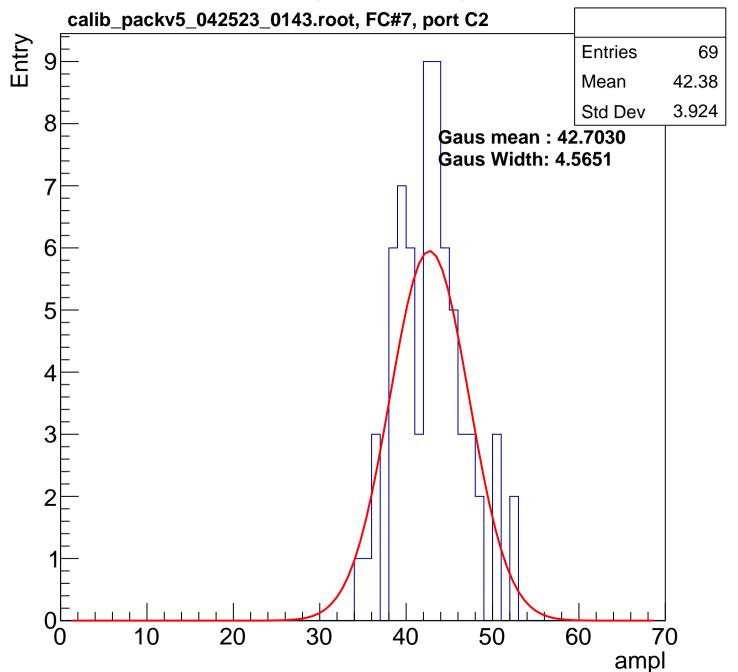


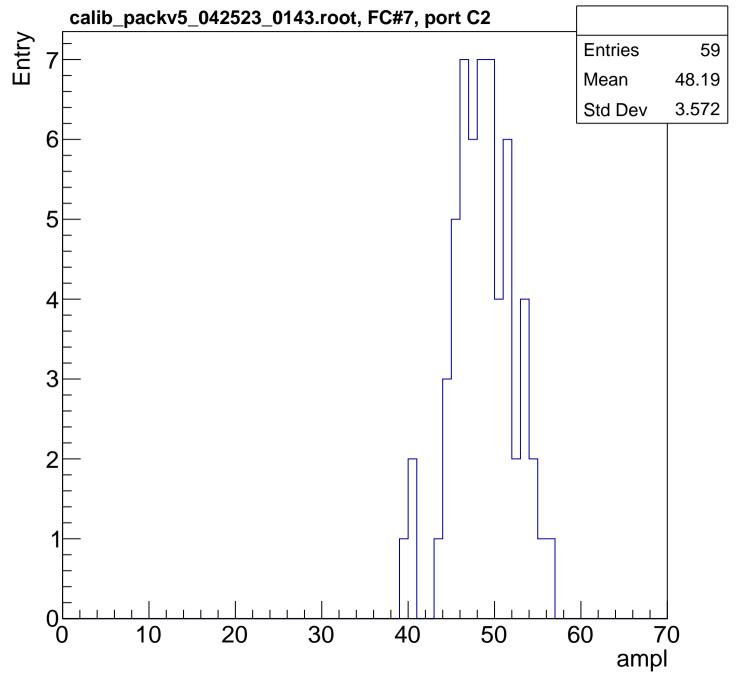


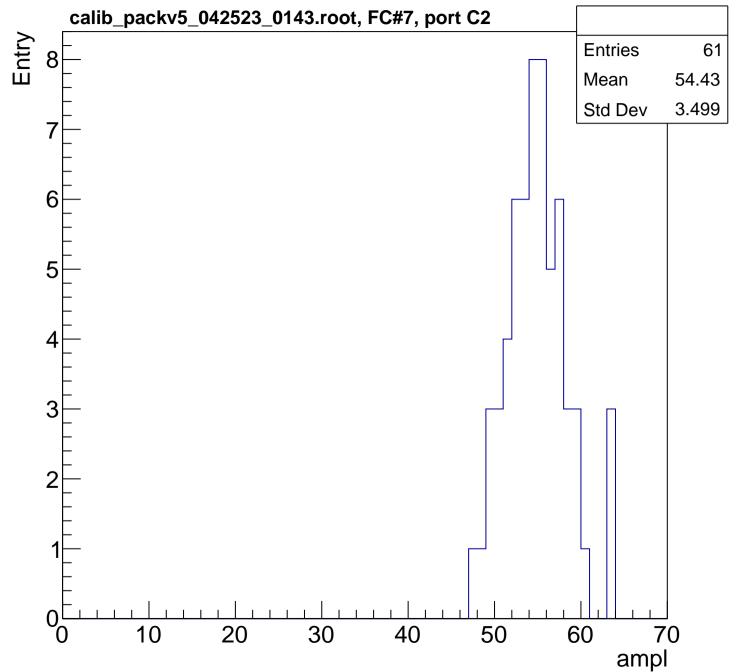
B1L103S, U4-ch19, adc7 calib_packv5_042523_0143.root, FC#7, port C2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

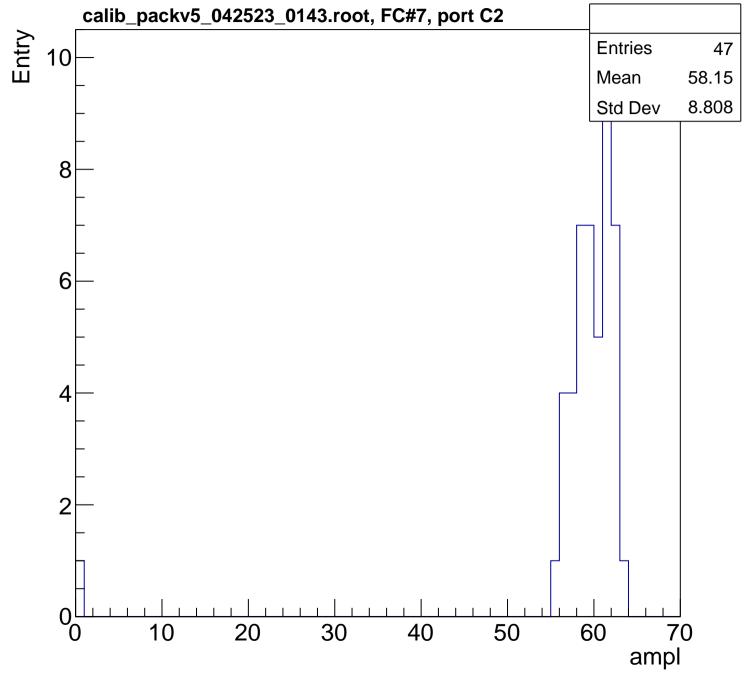


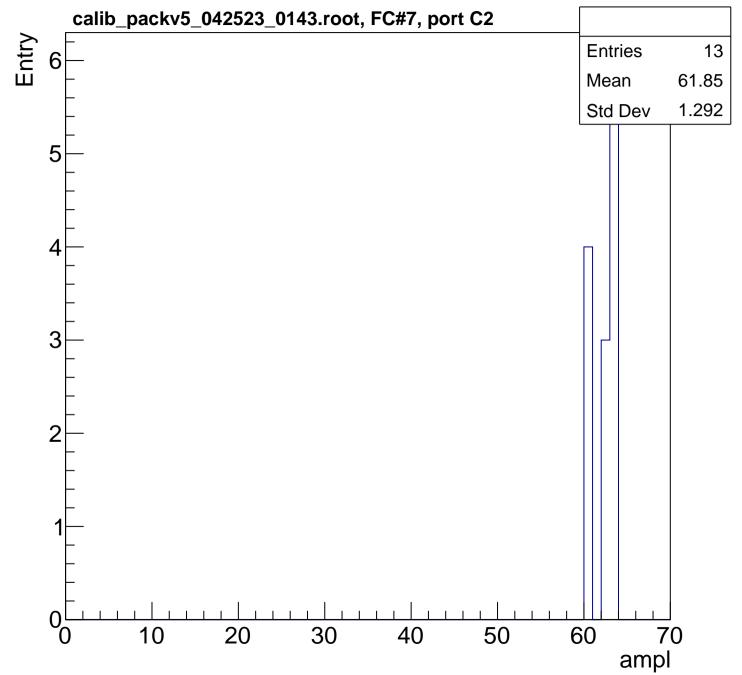


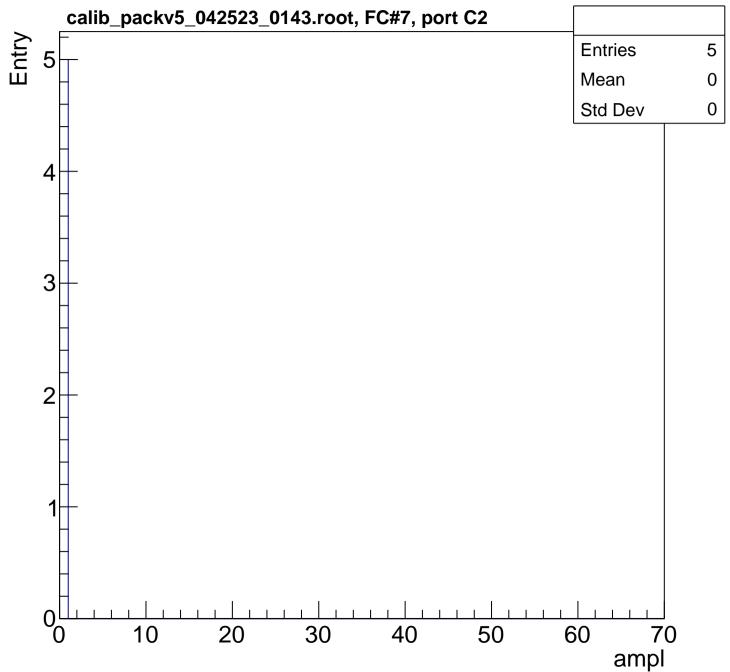


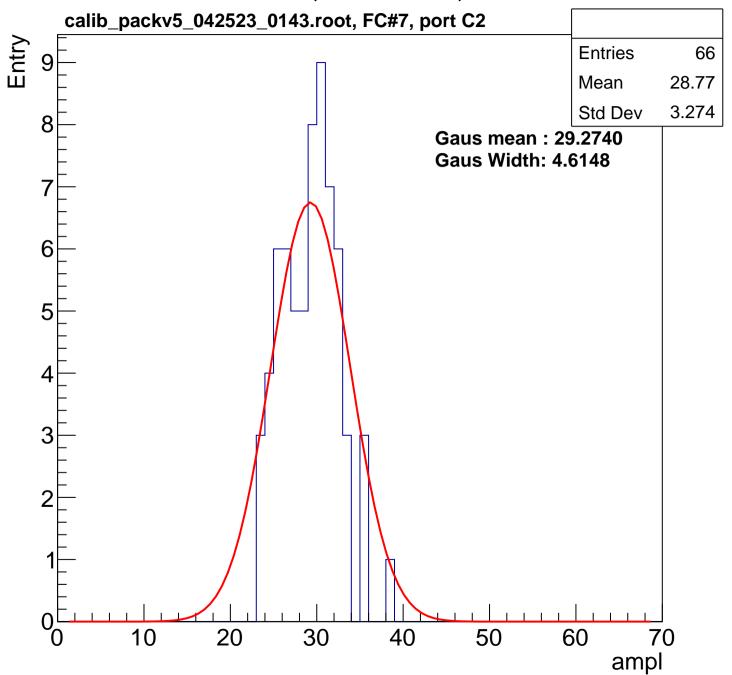


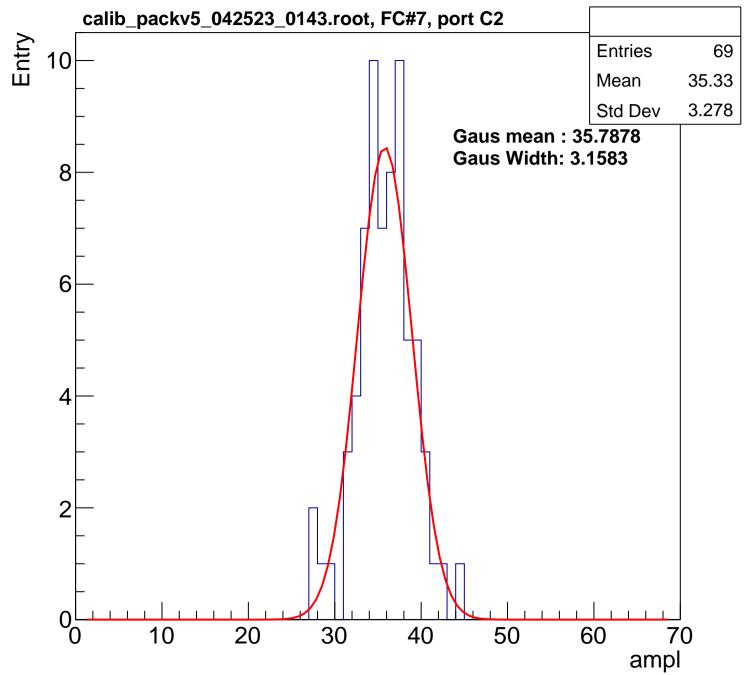


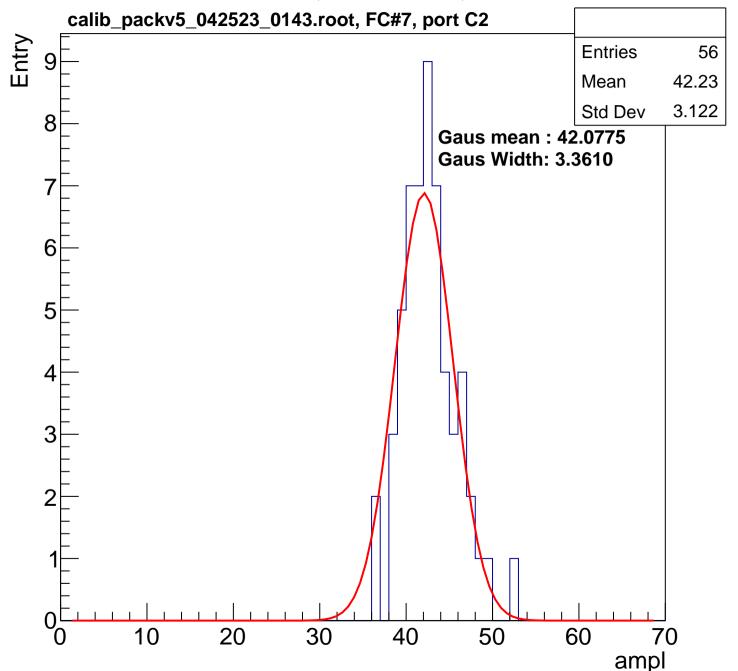


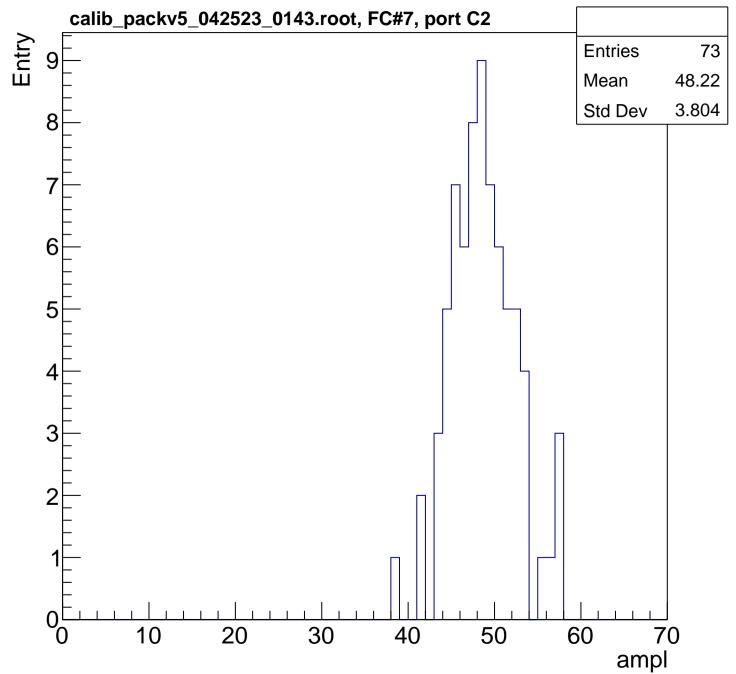


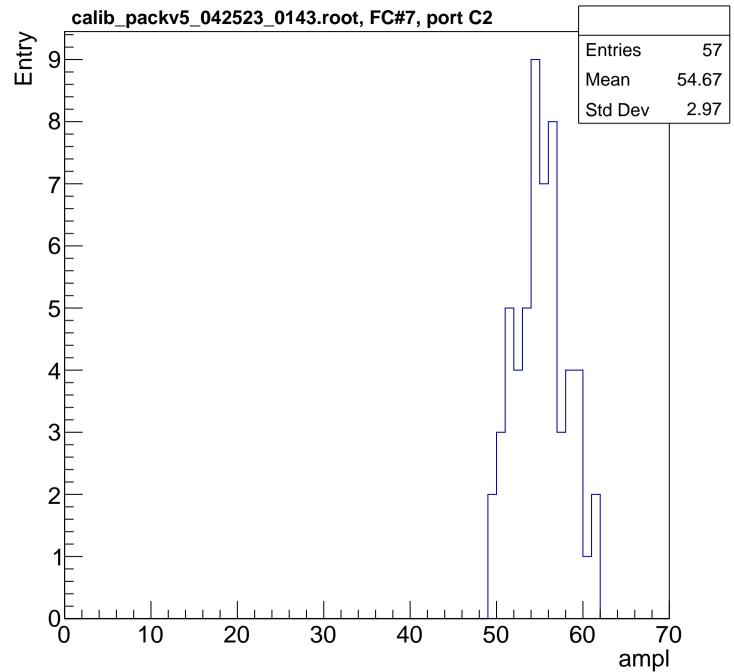


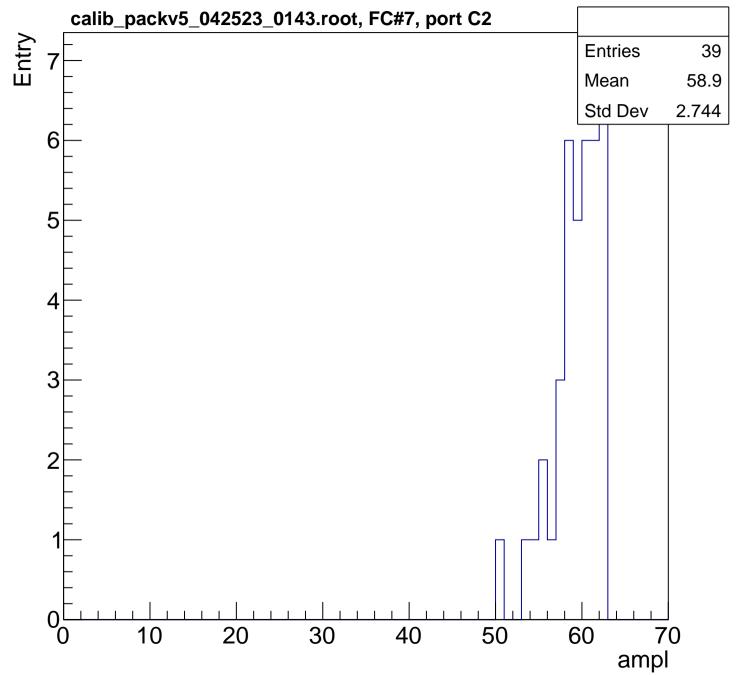


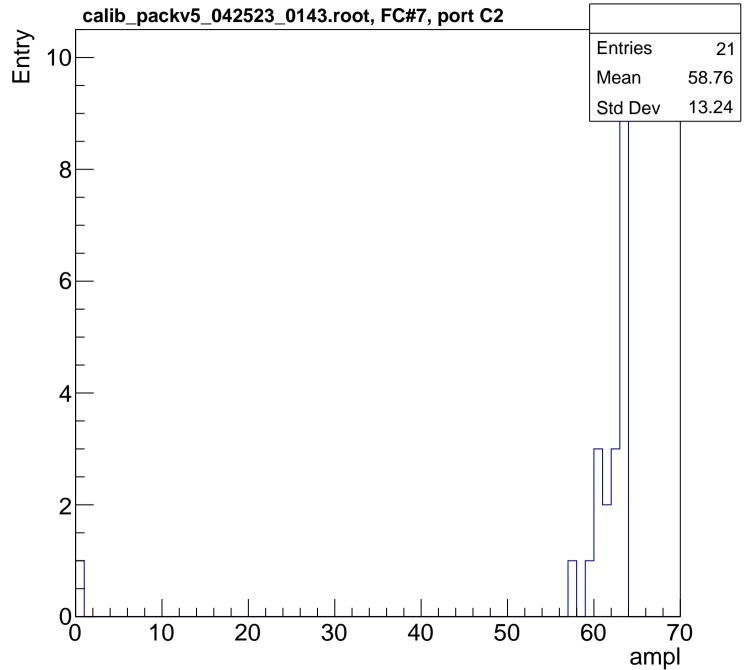


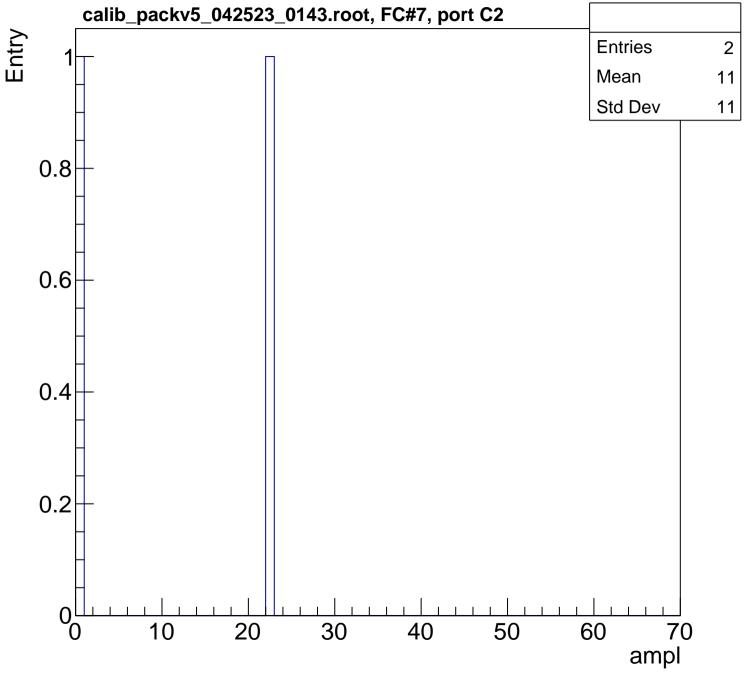


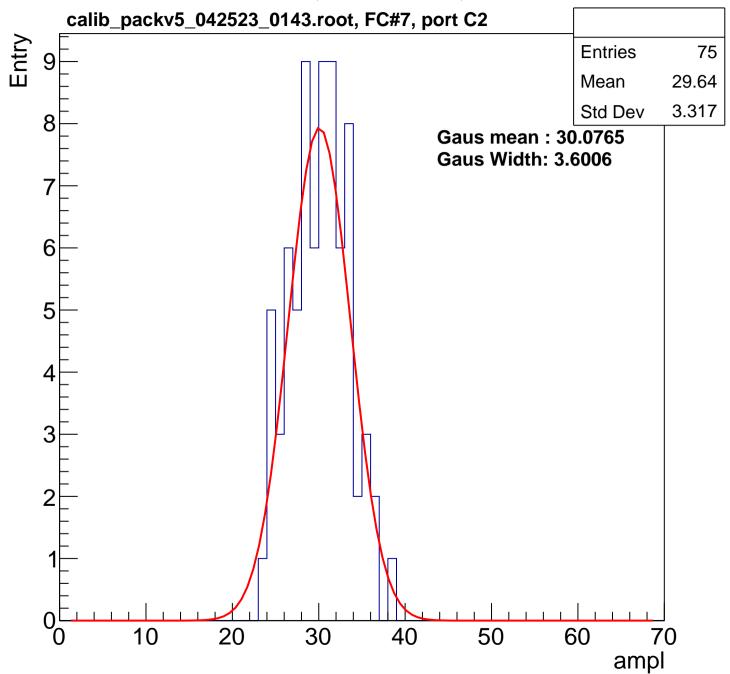


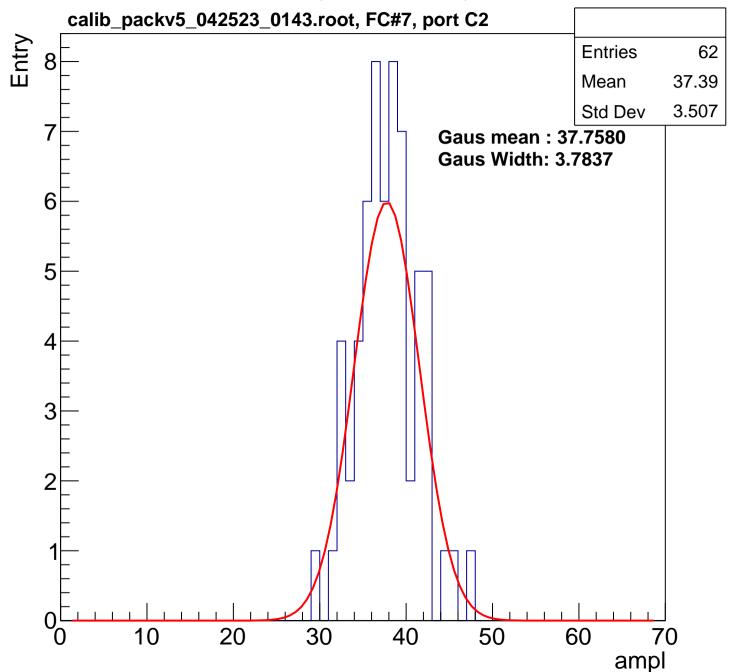


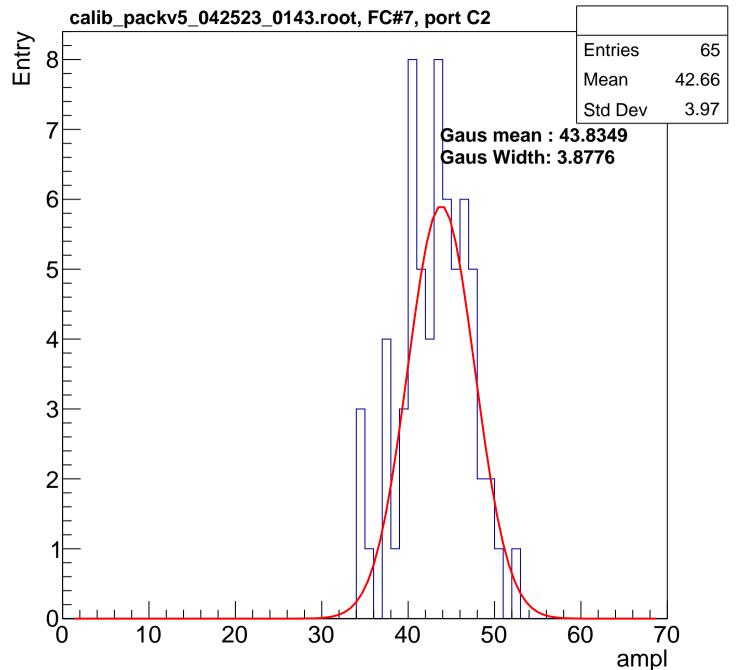


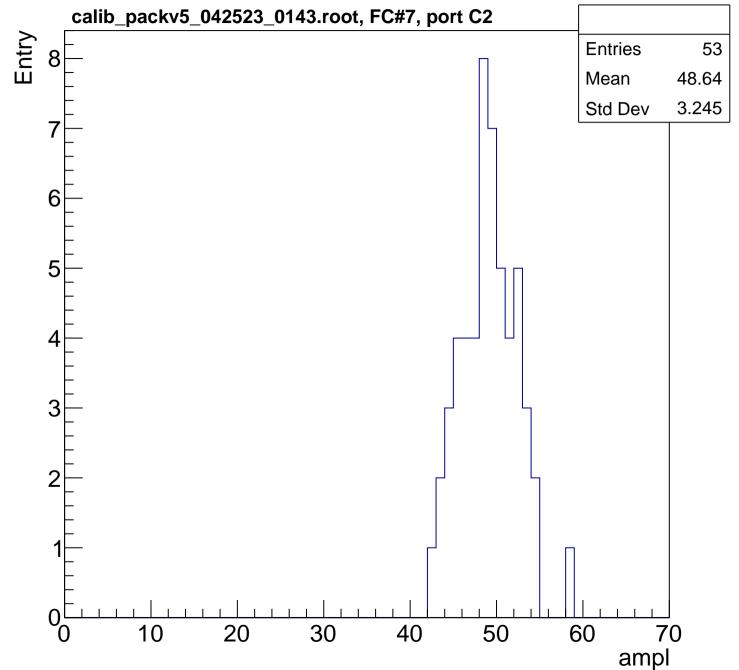


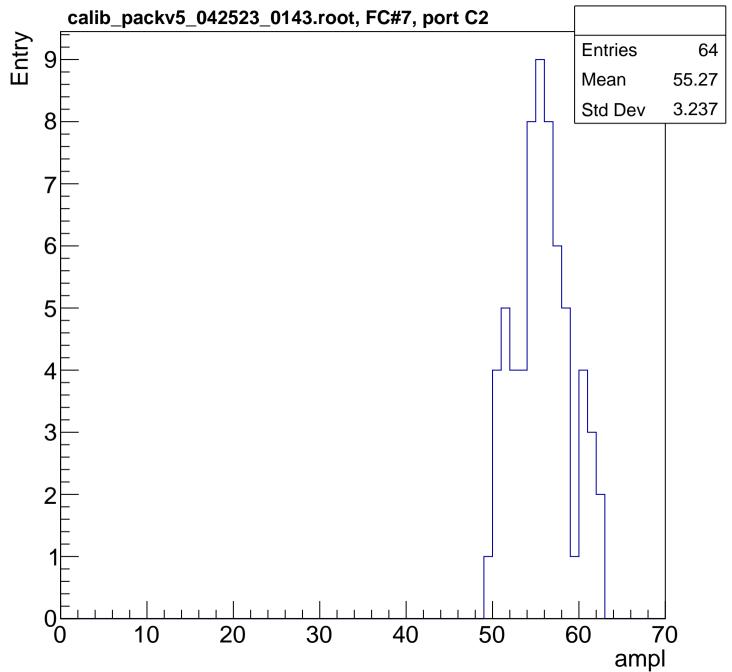


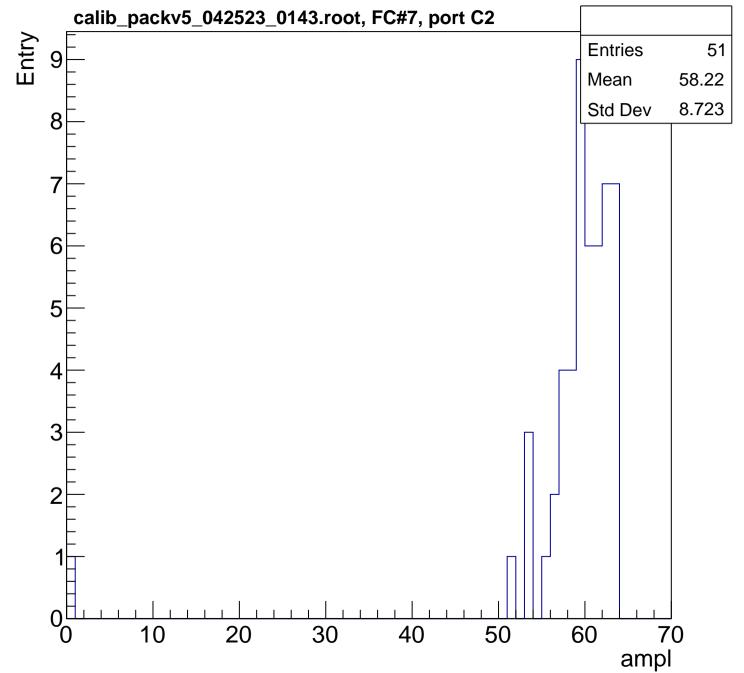


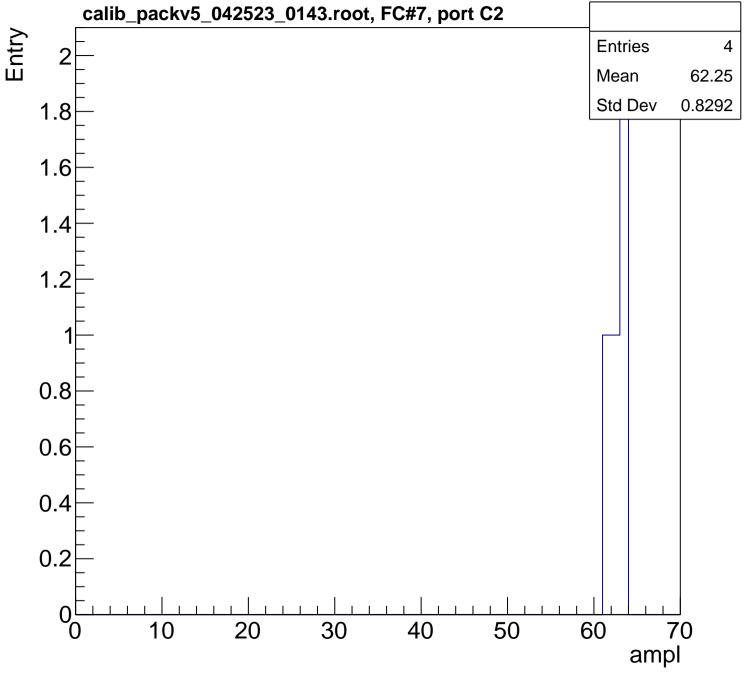




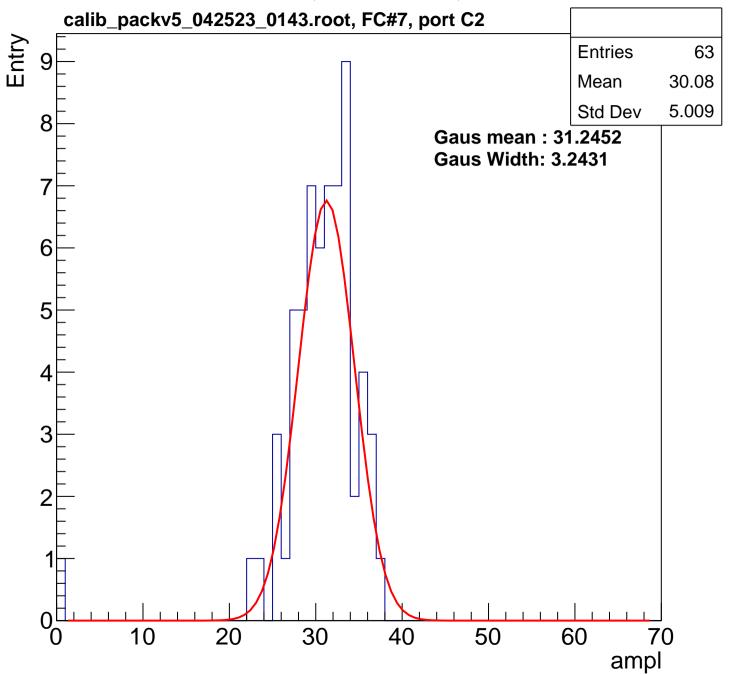


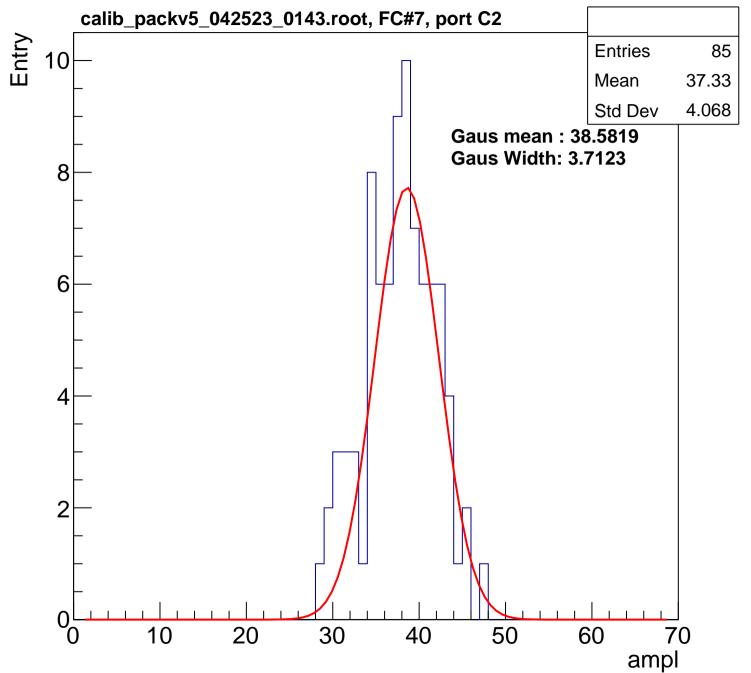


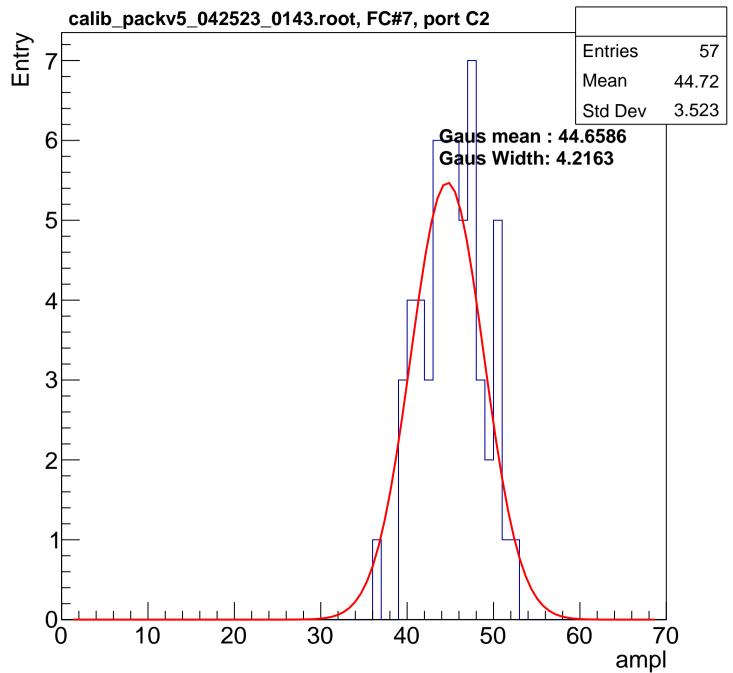


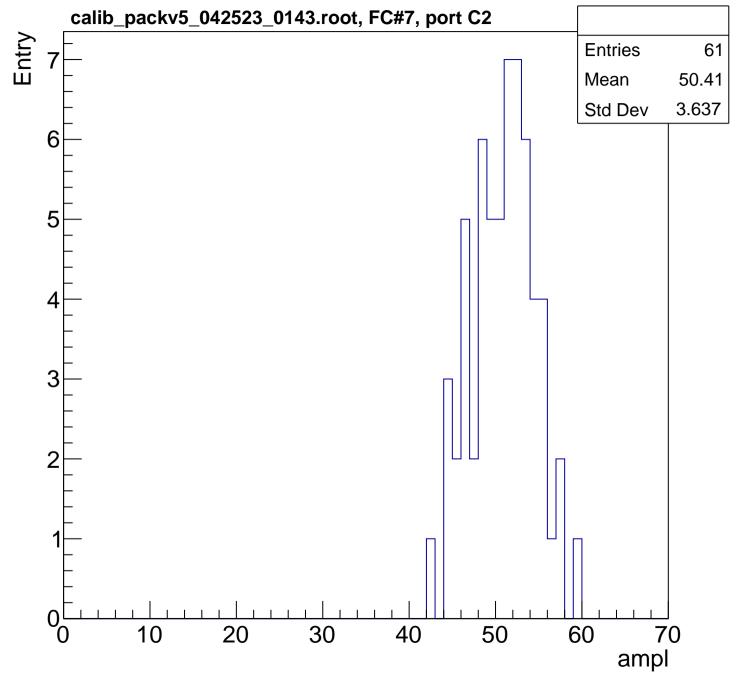


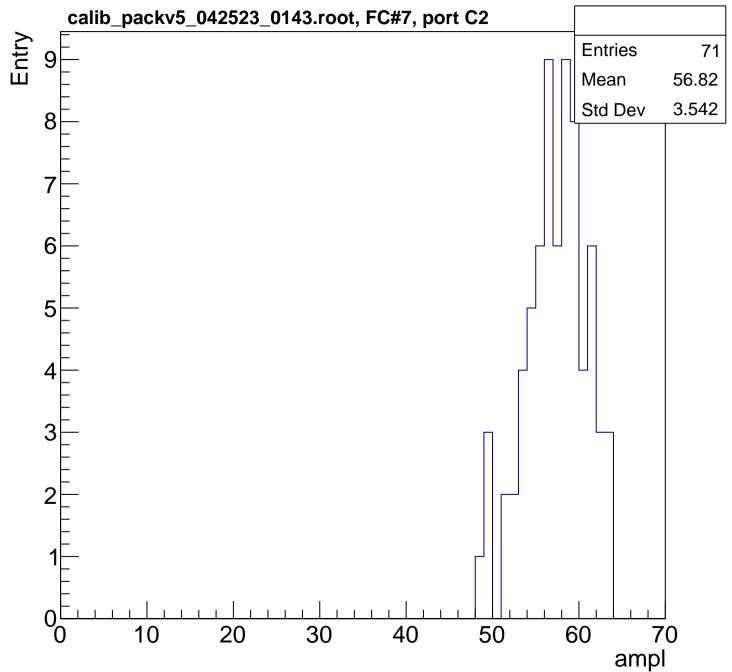


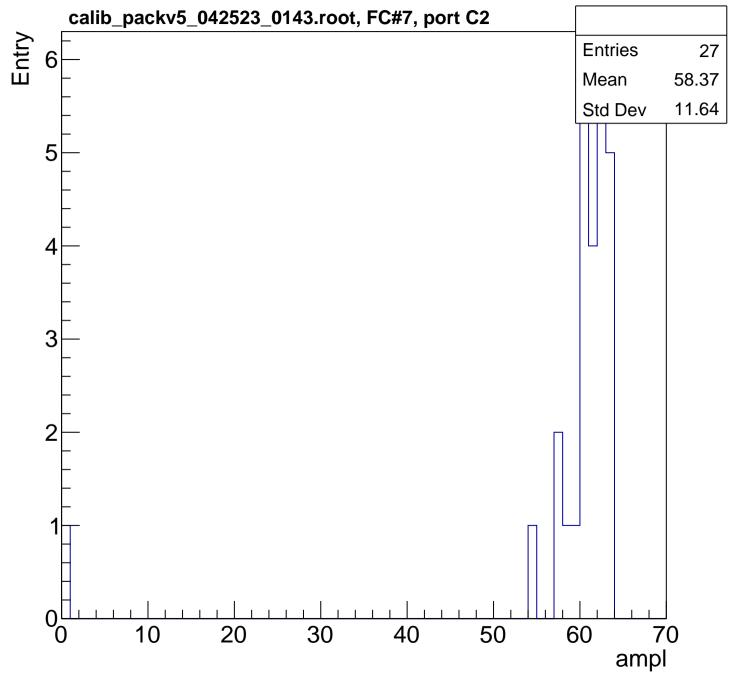


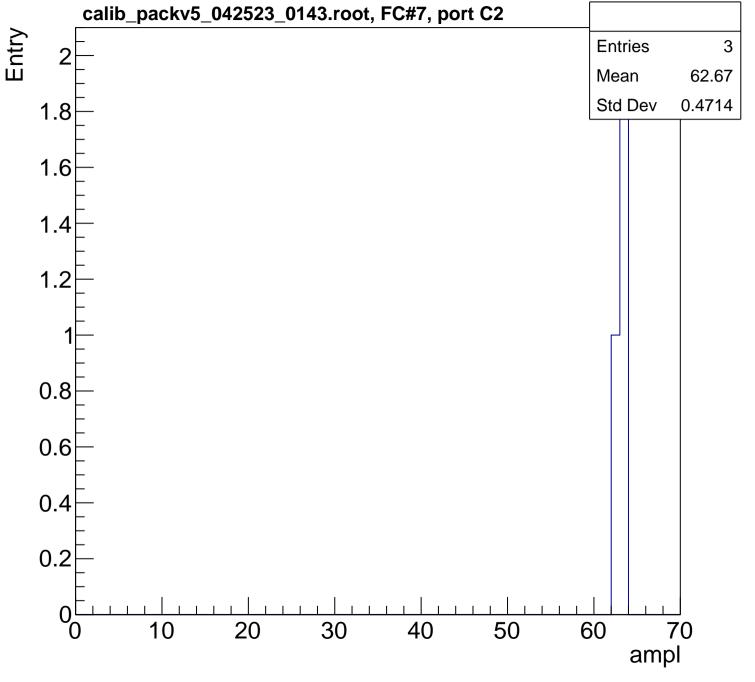




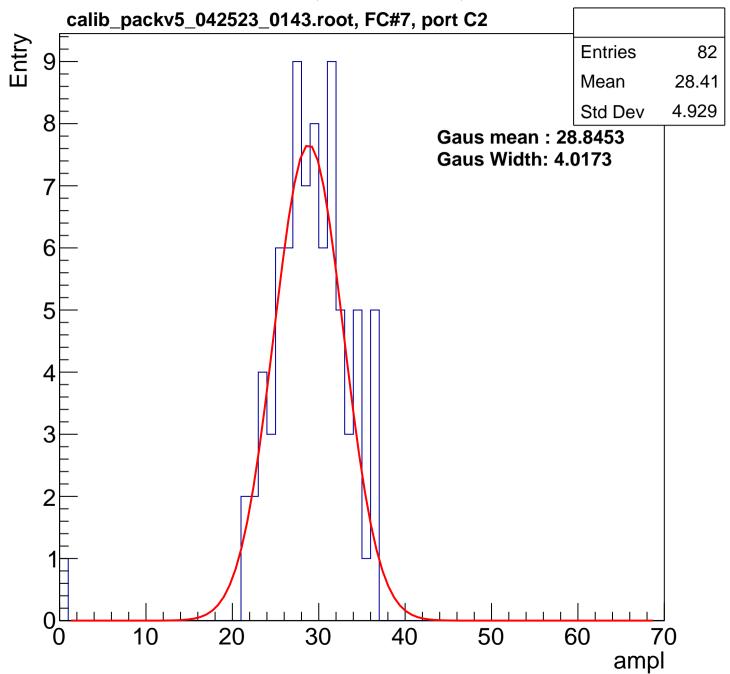


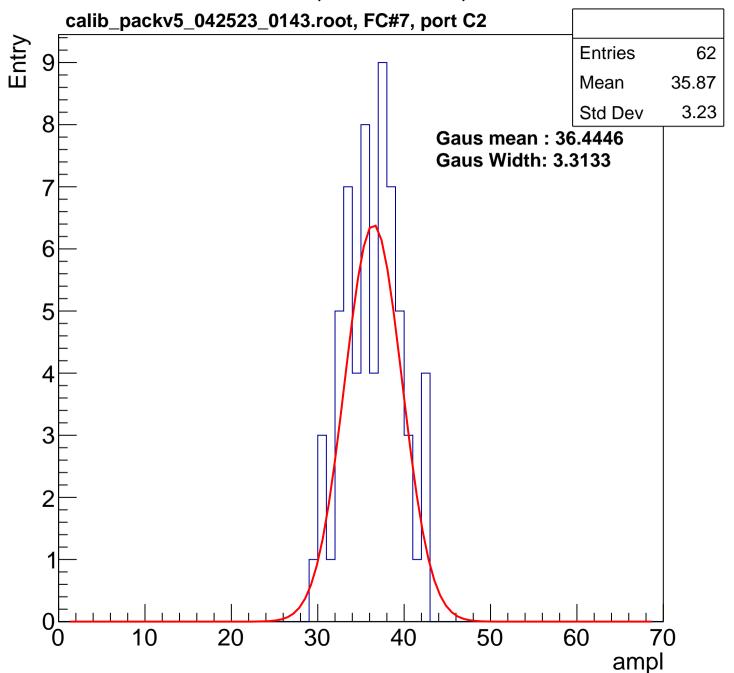


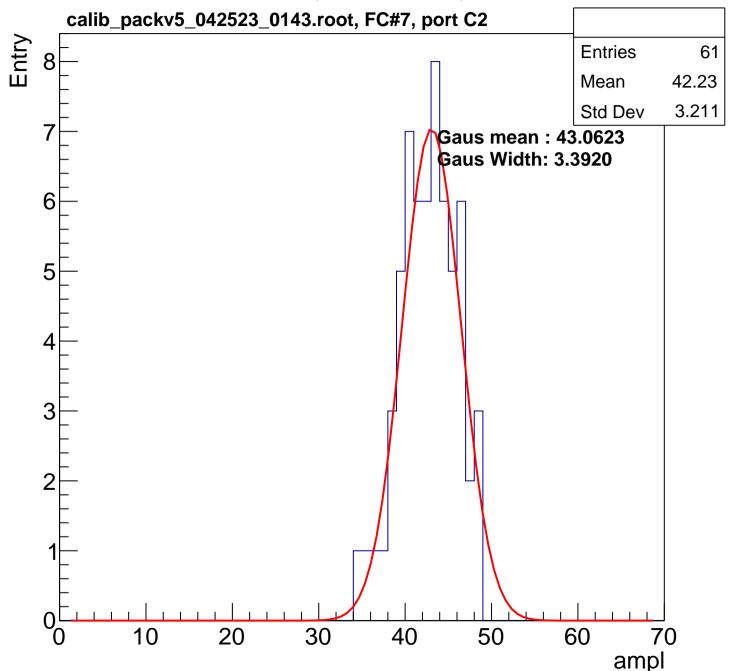


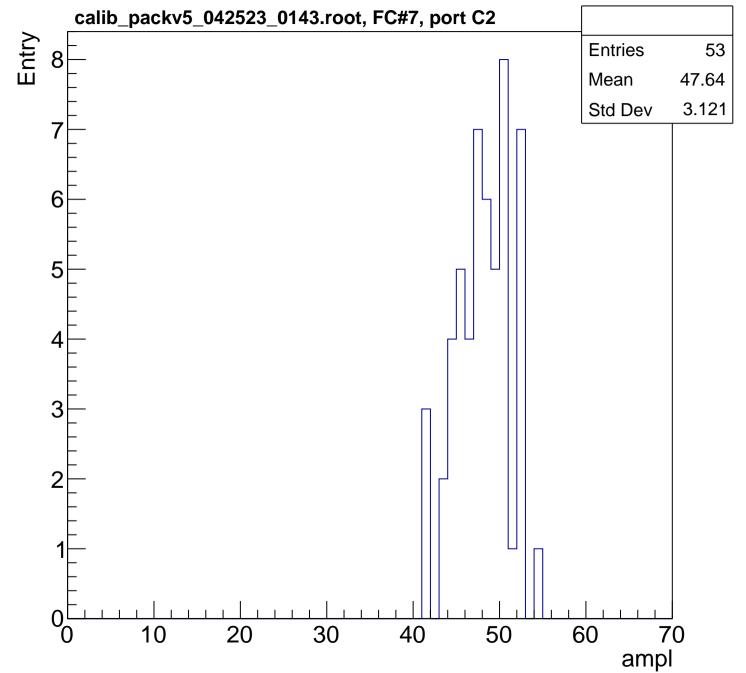


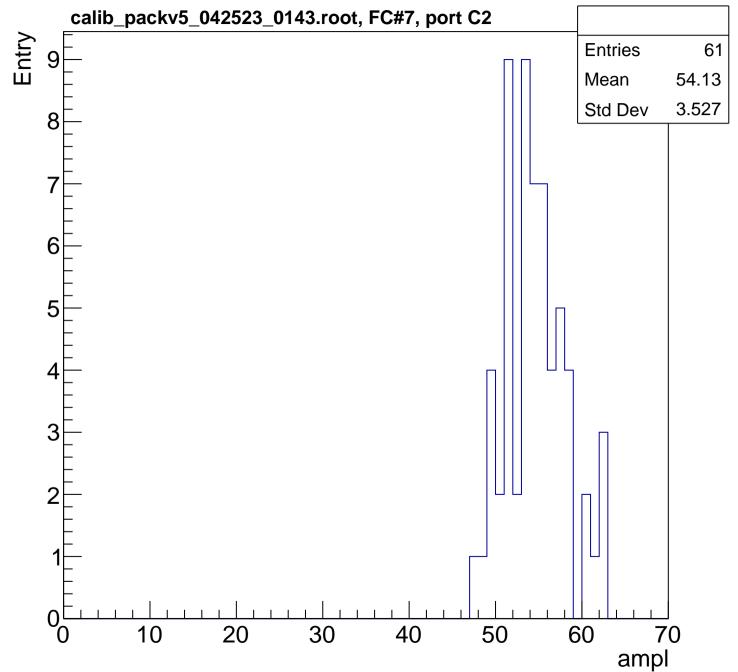


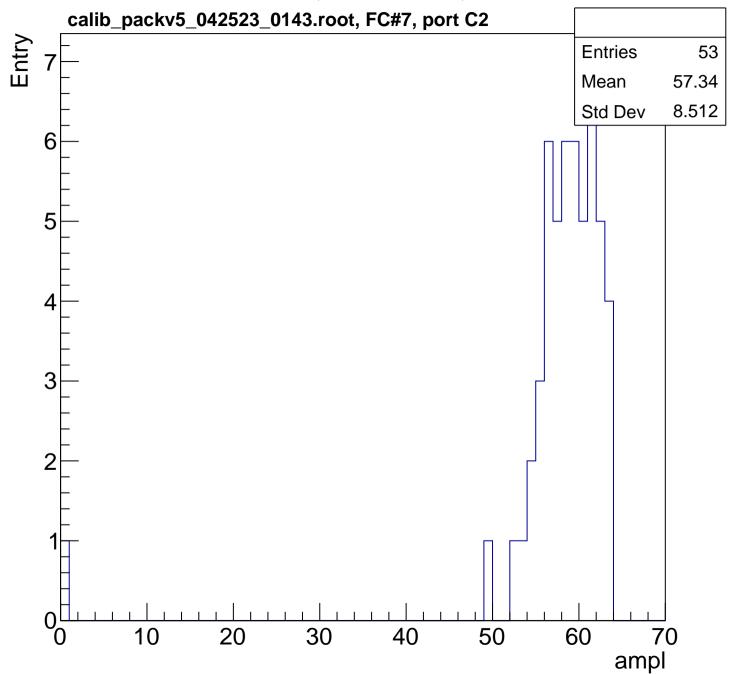


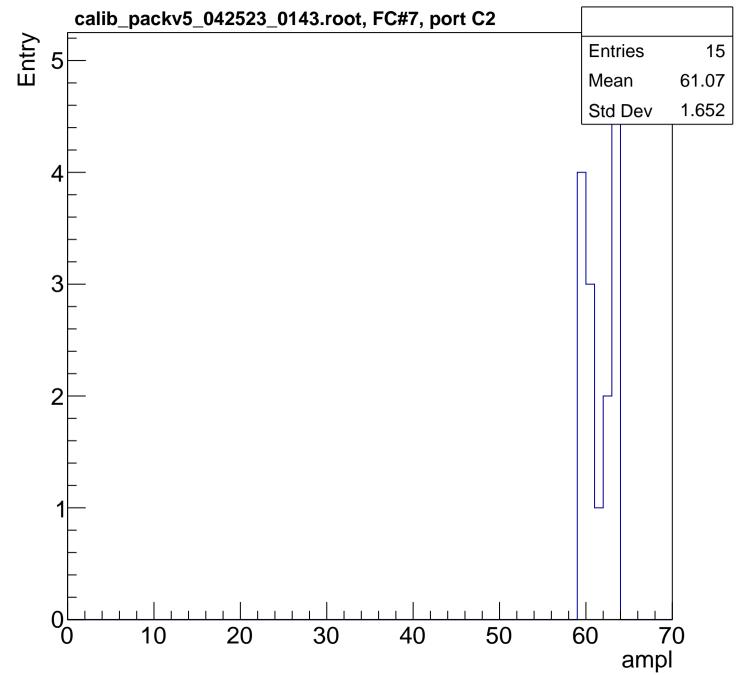


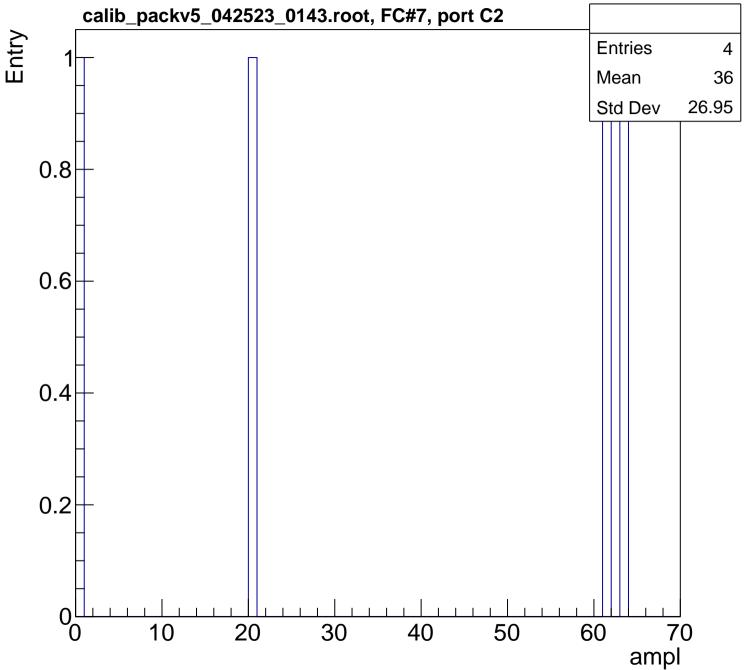


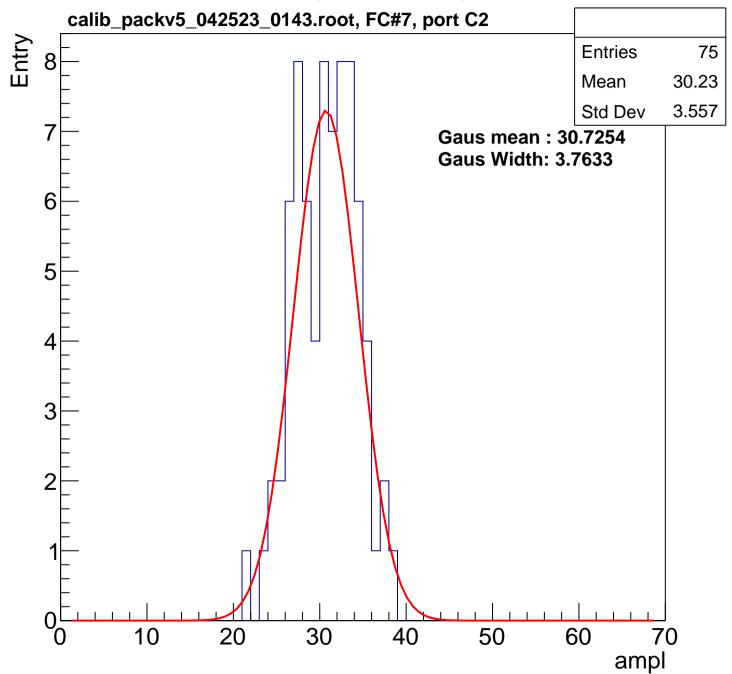


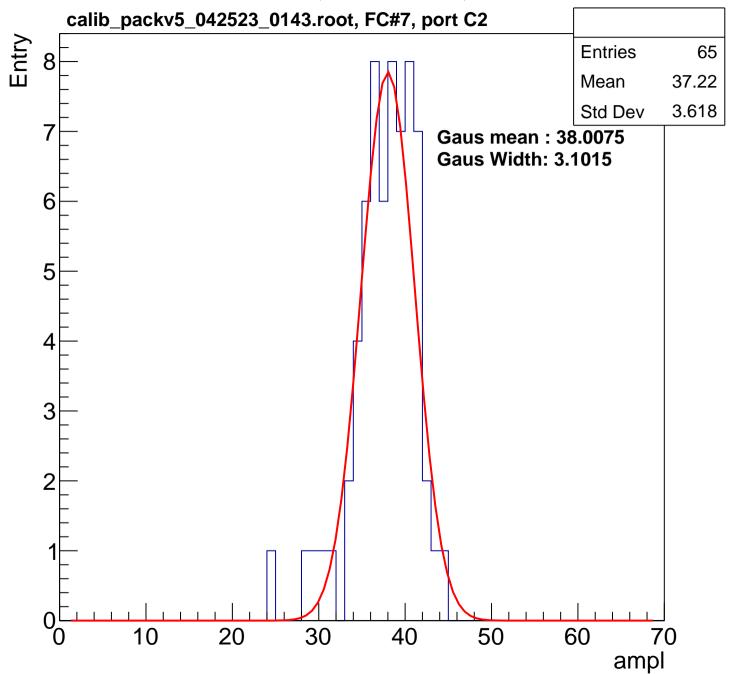


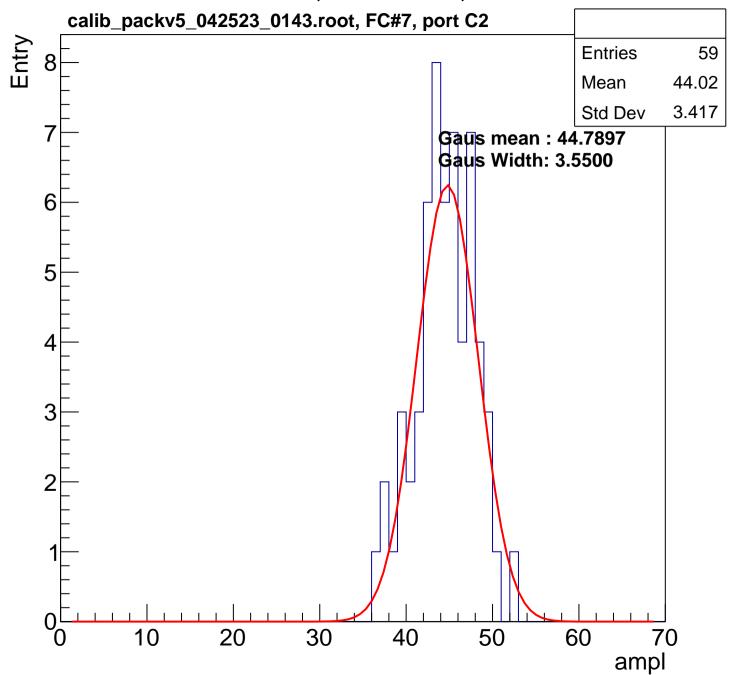


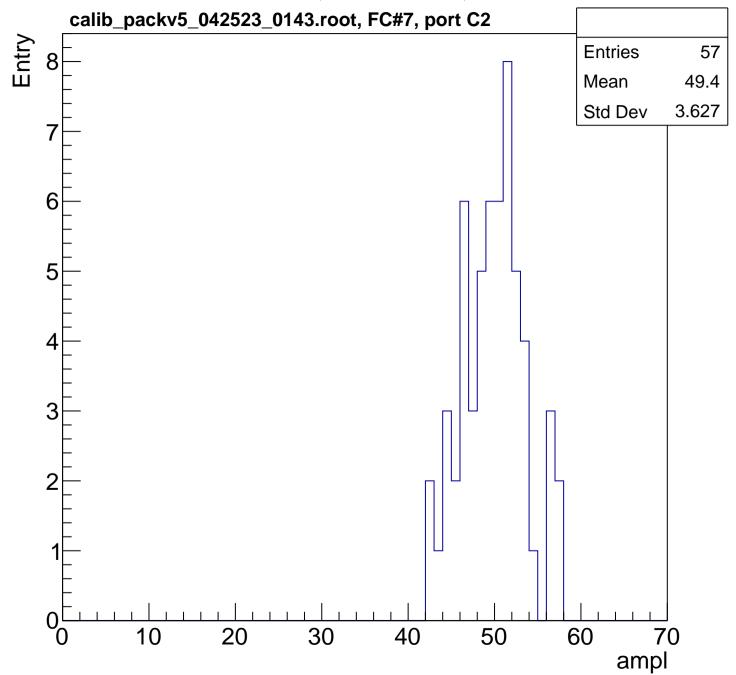


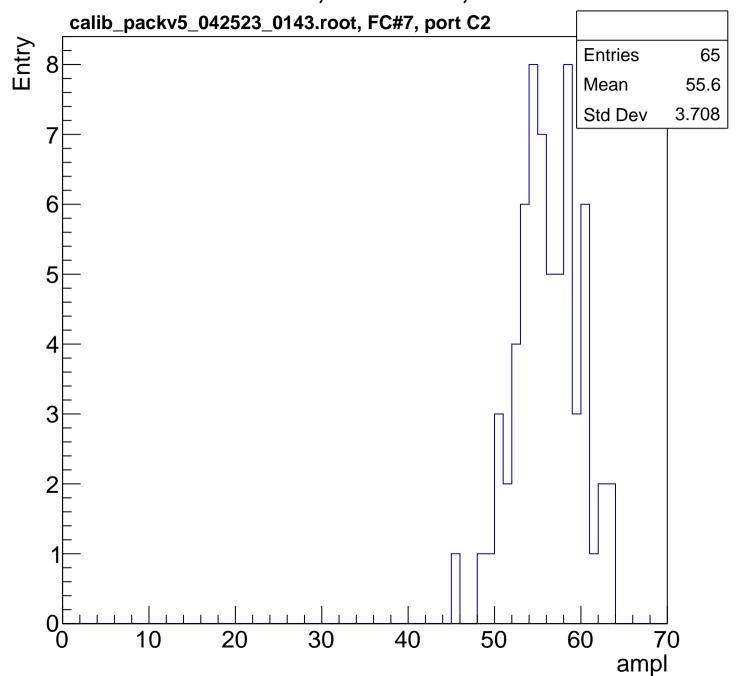


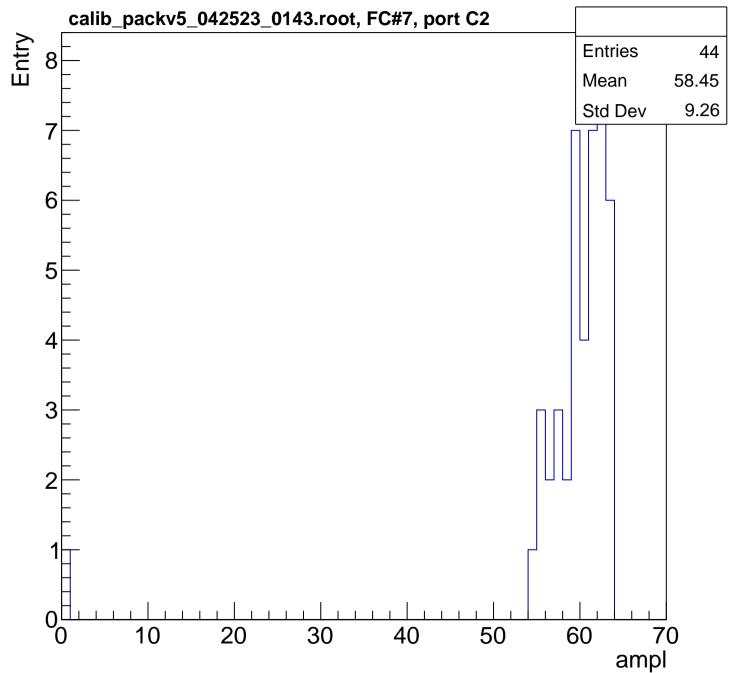


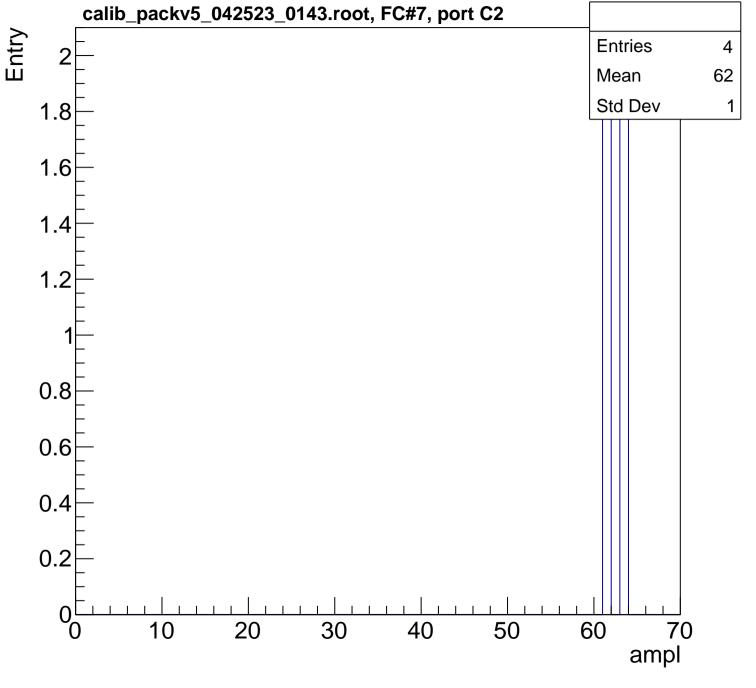








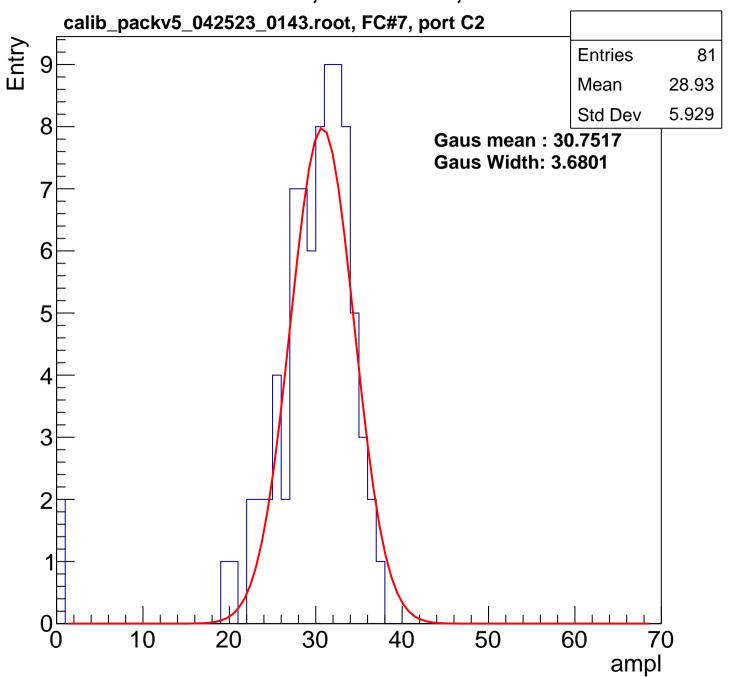


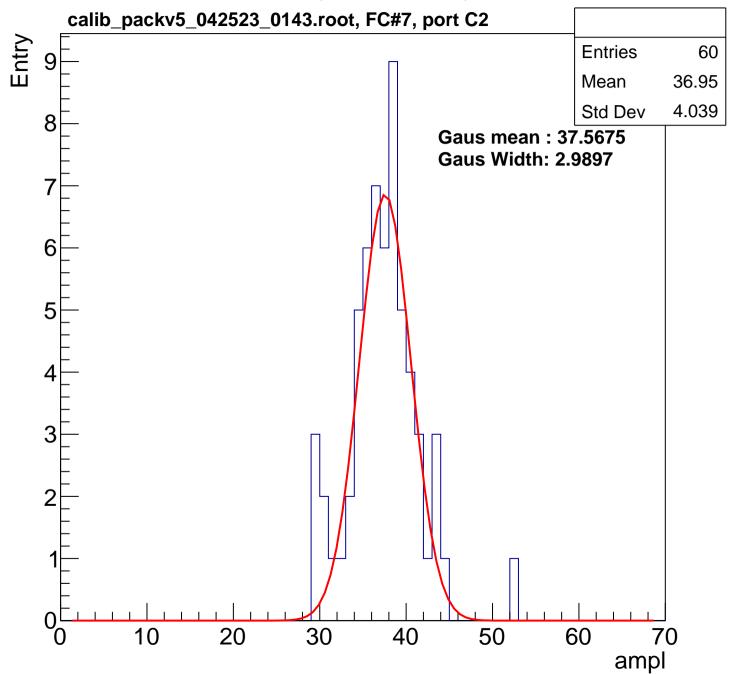


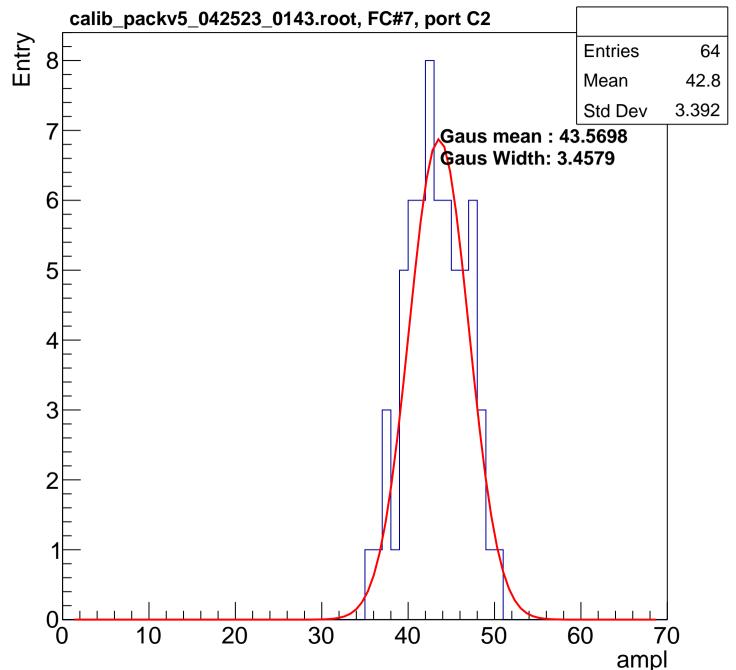
B1L103S, U4-ch25, adc7 calib_packv5_042523_0143.root, FC#7, port C2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60

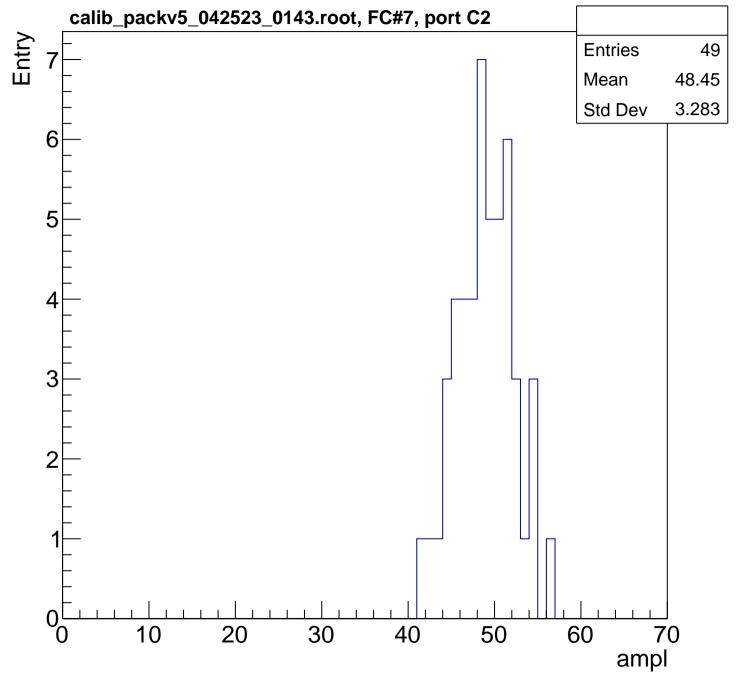
70

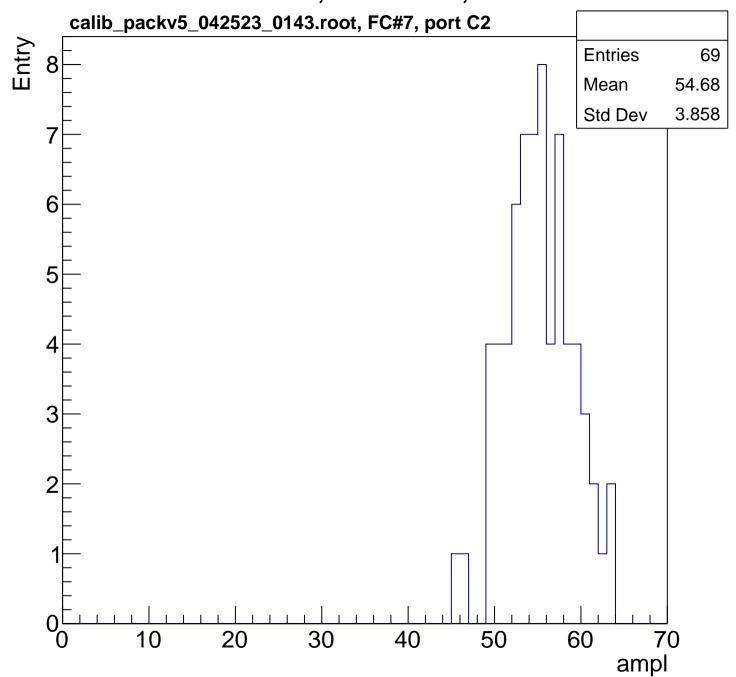
ampl

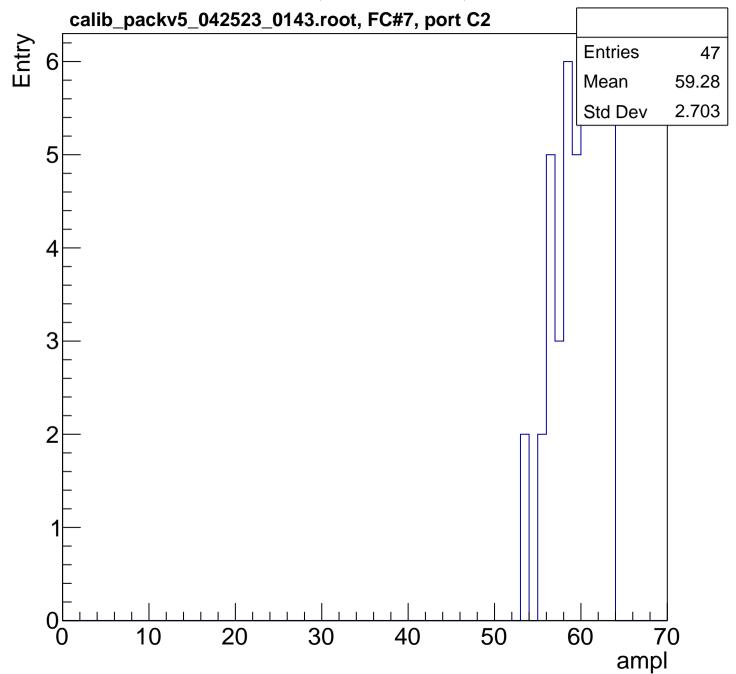


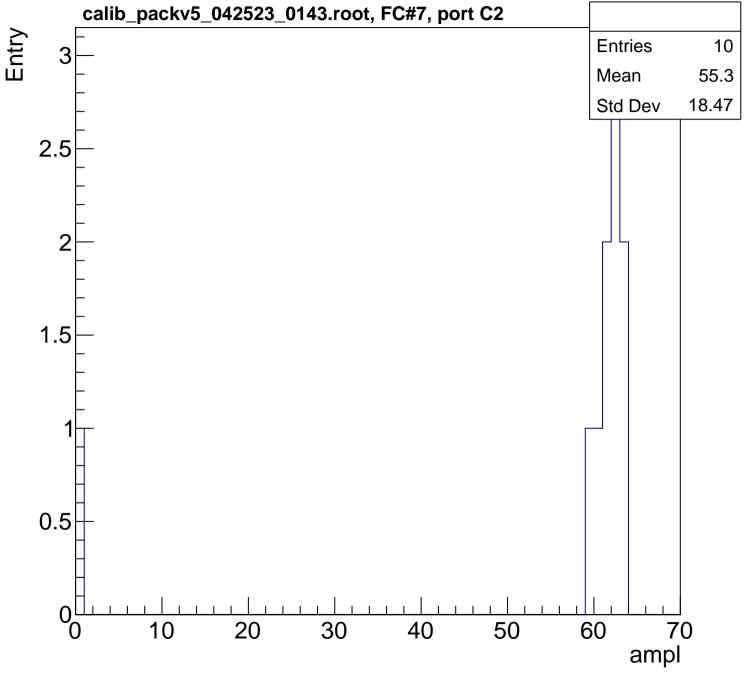




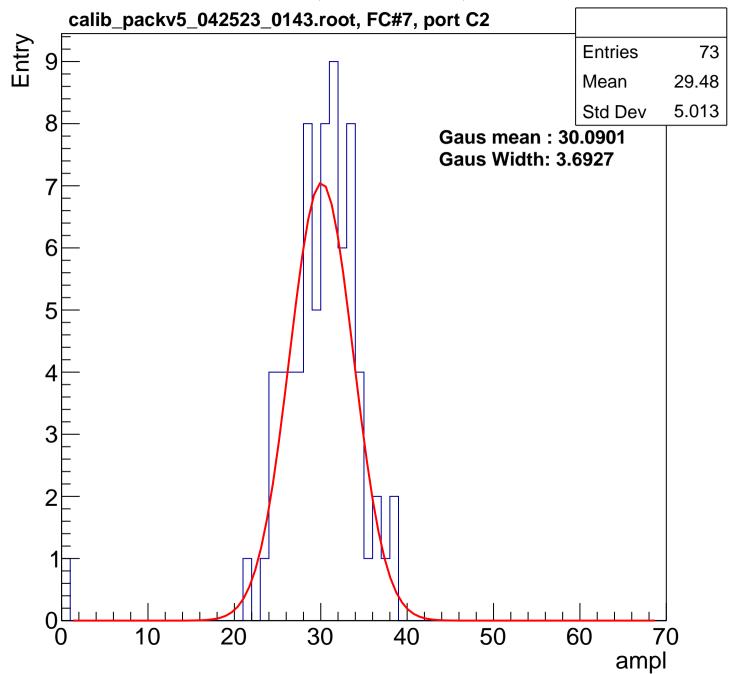


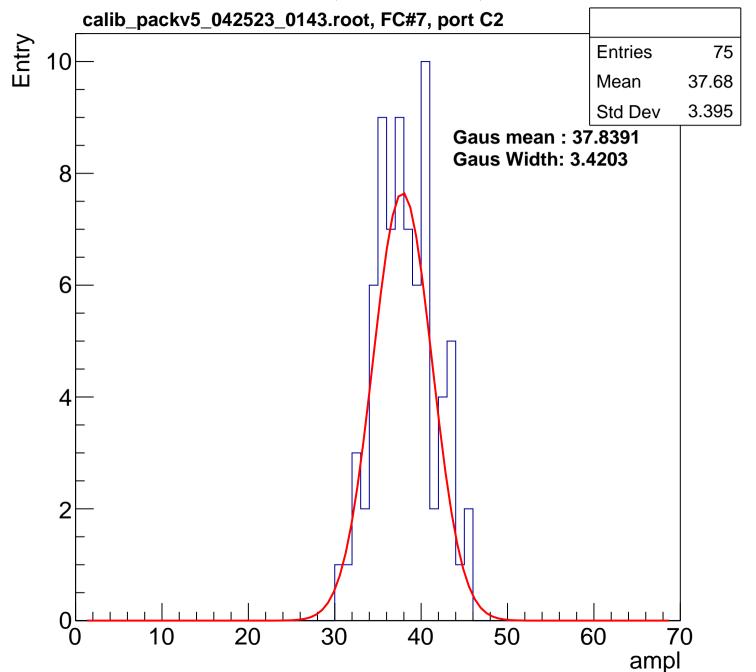


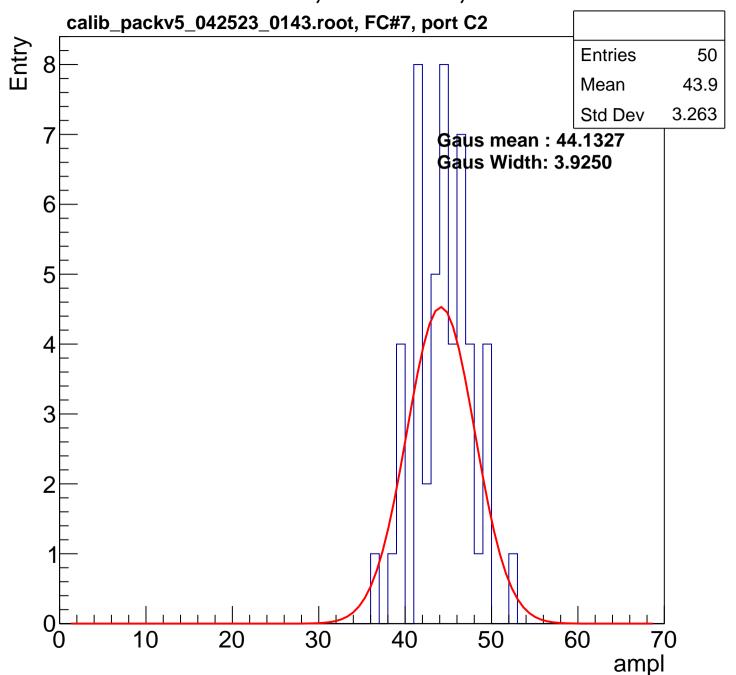




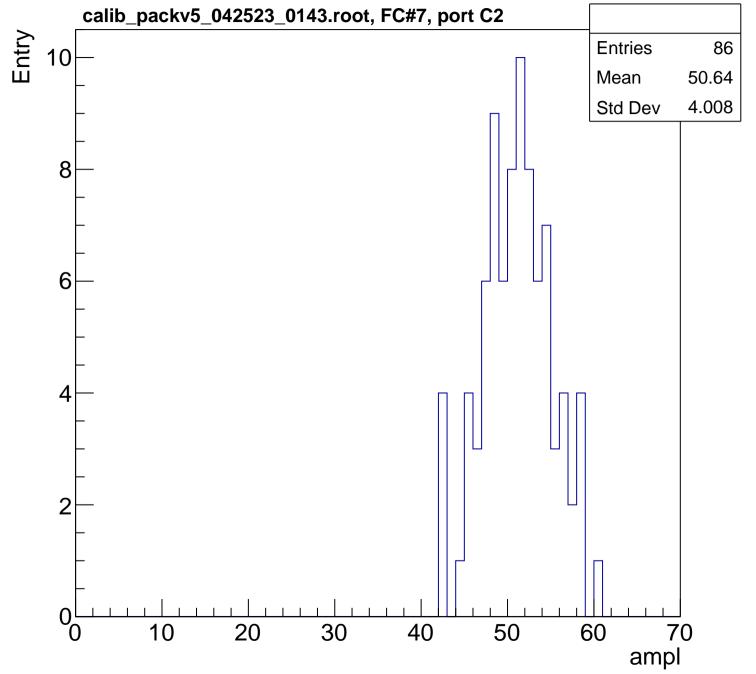


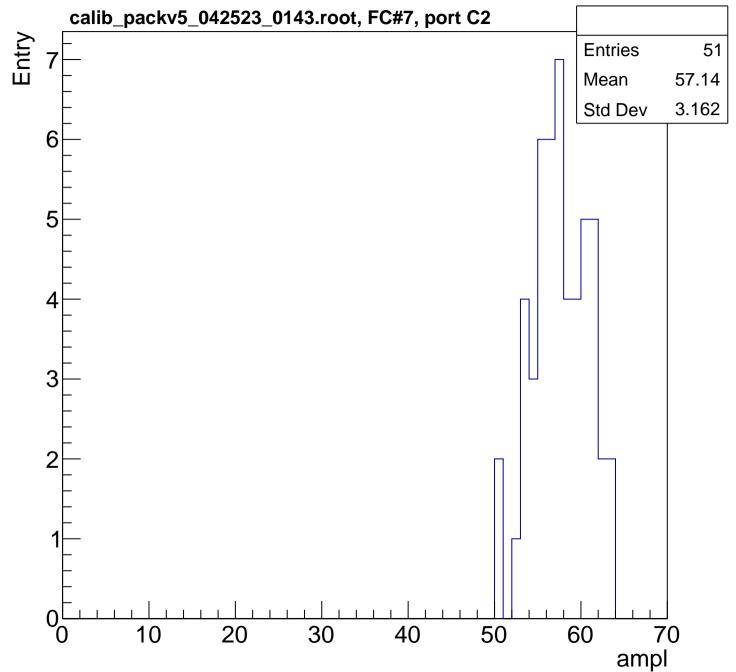


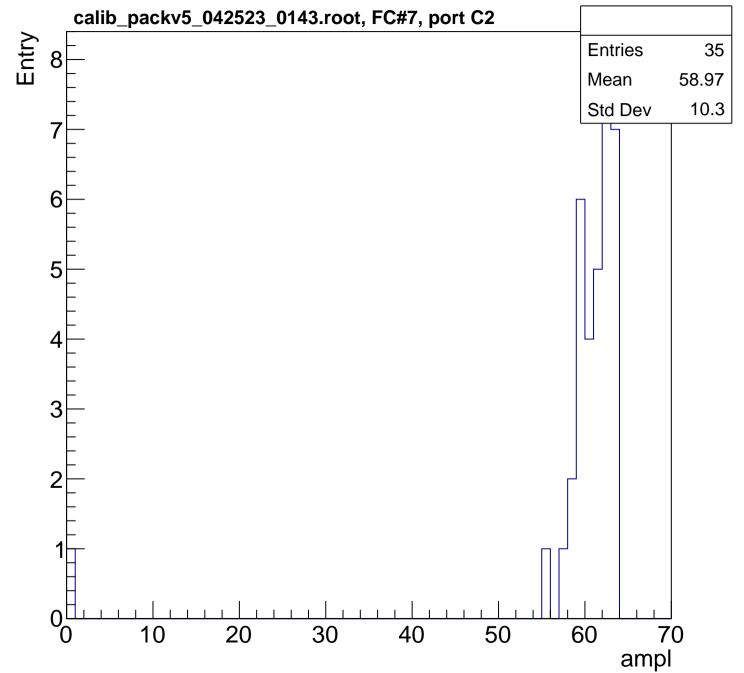


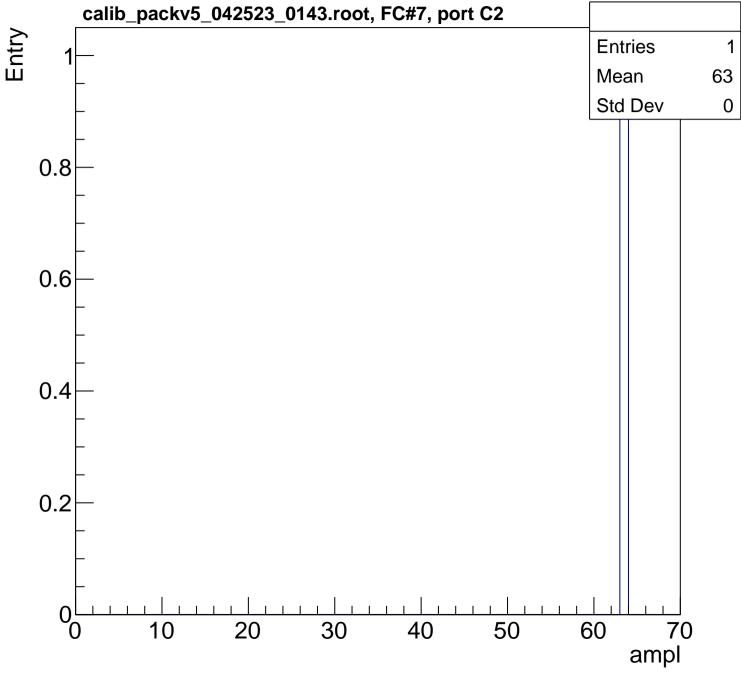


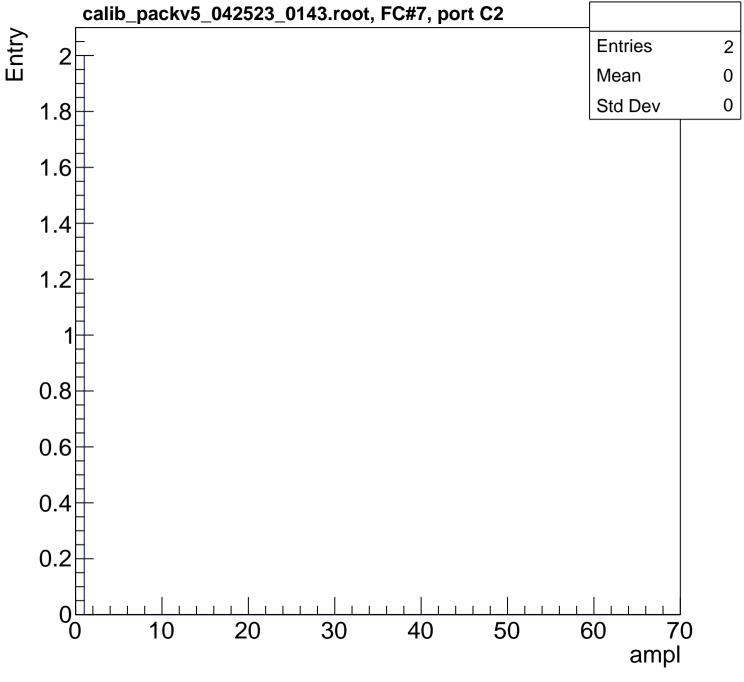
B1L103S, U4-ch27, adc3

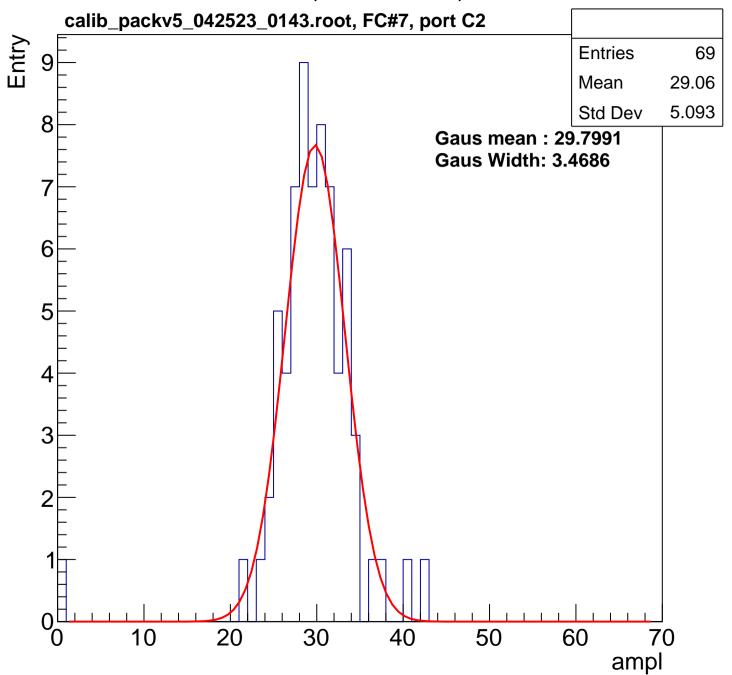


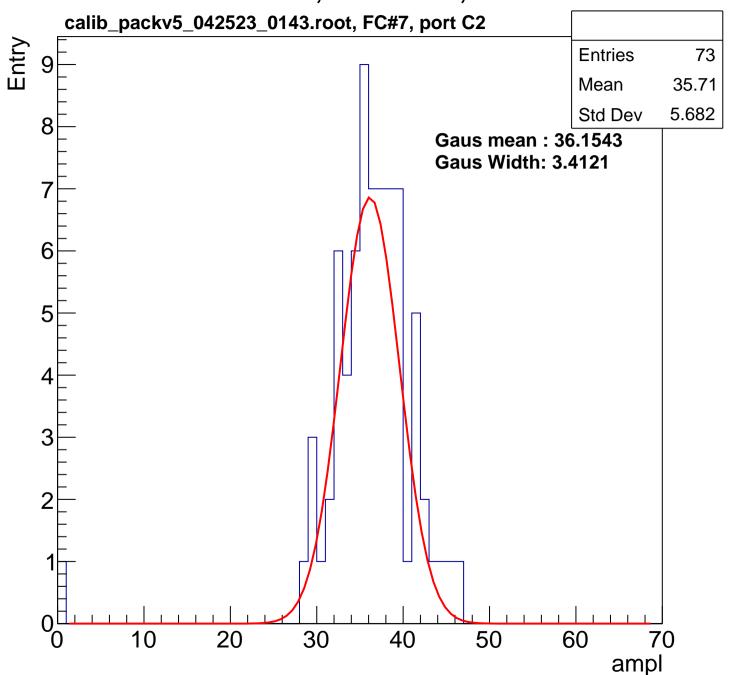


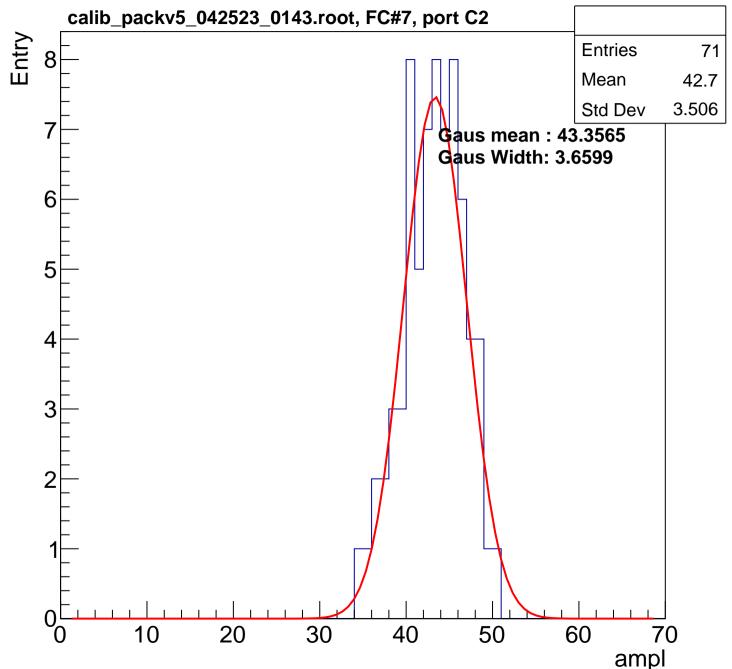


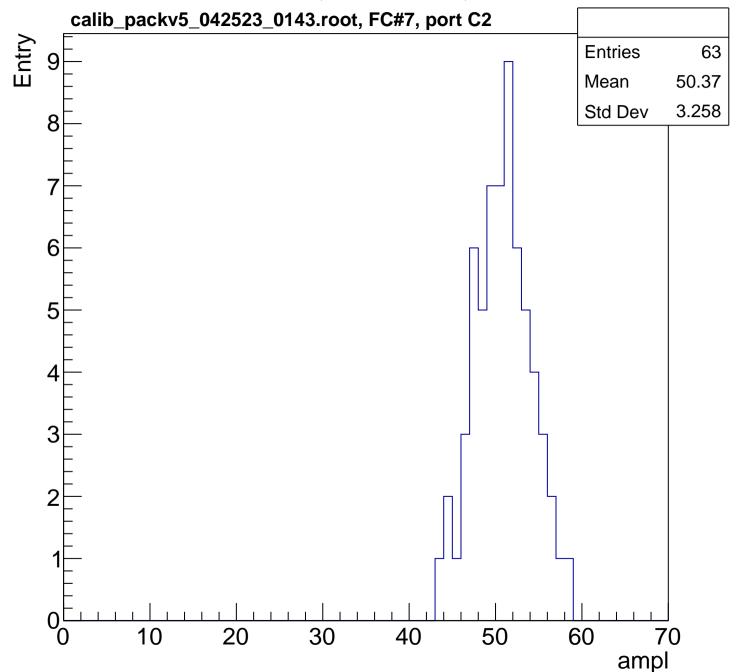


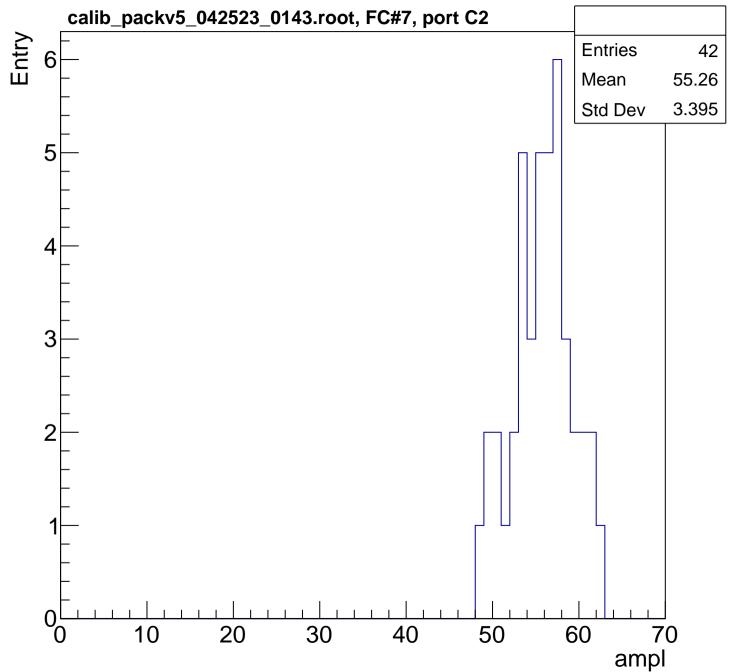


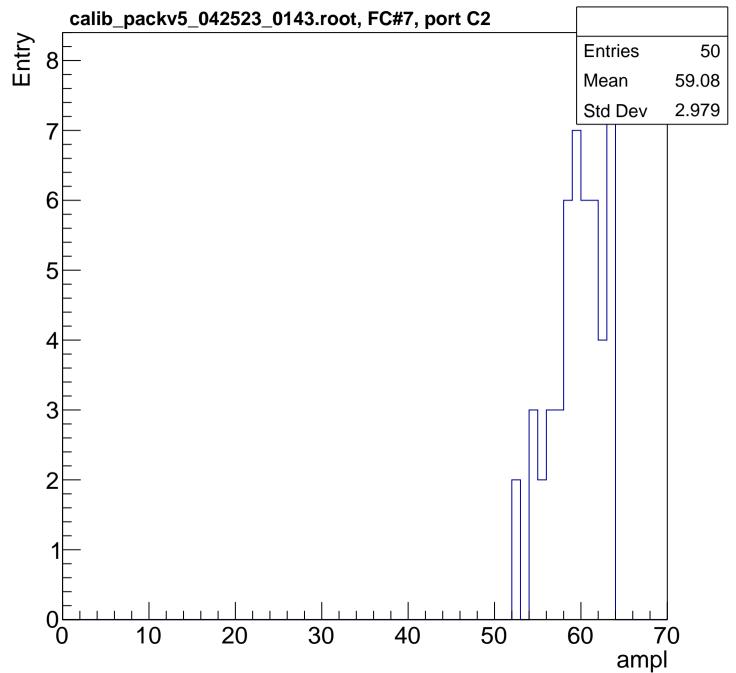


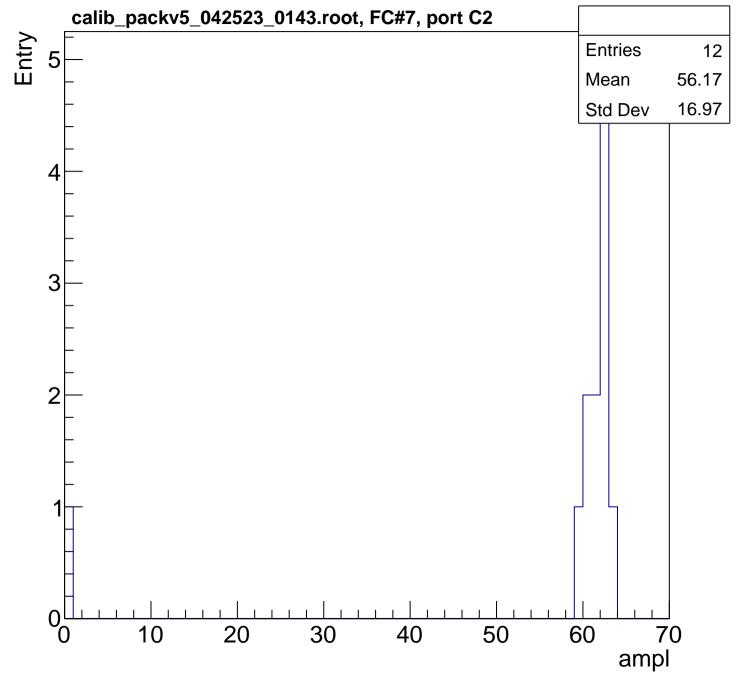


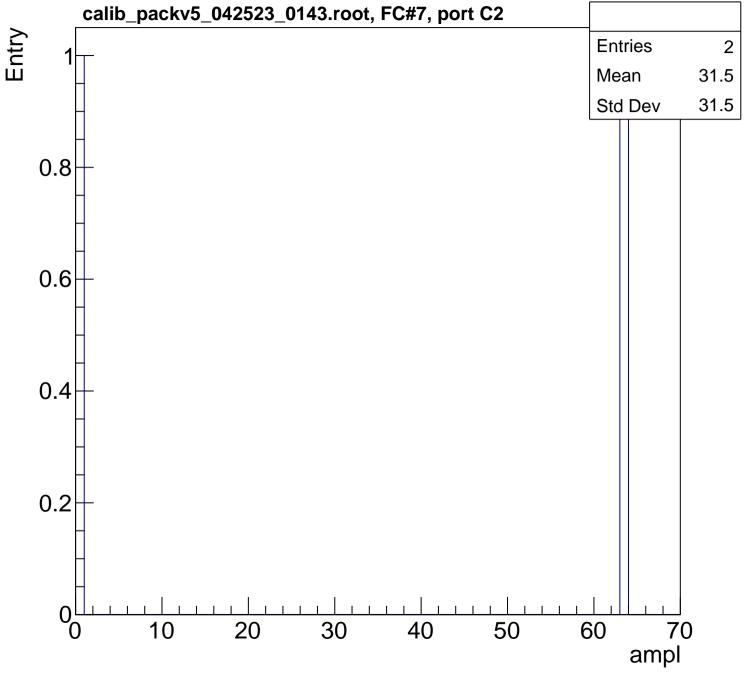


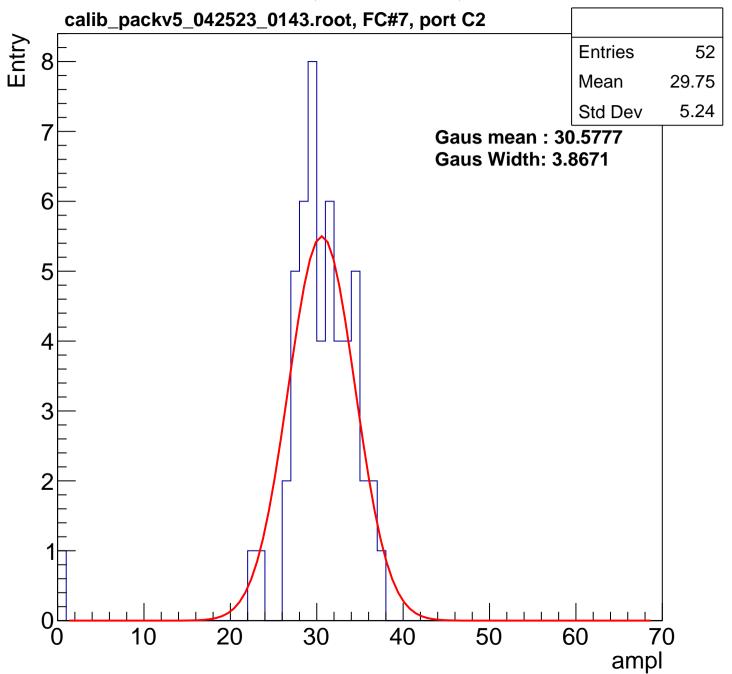


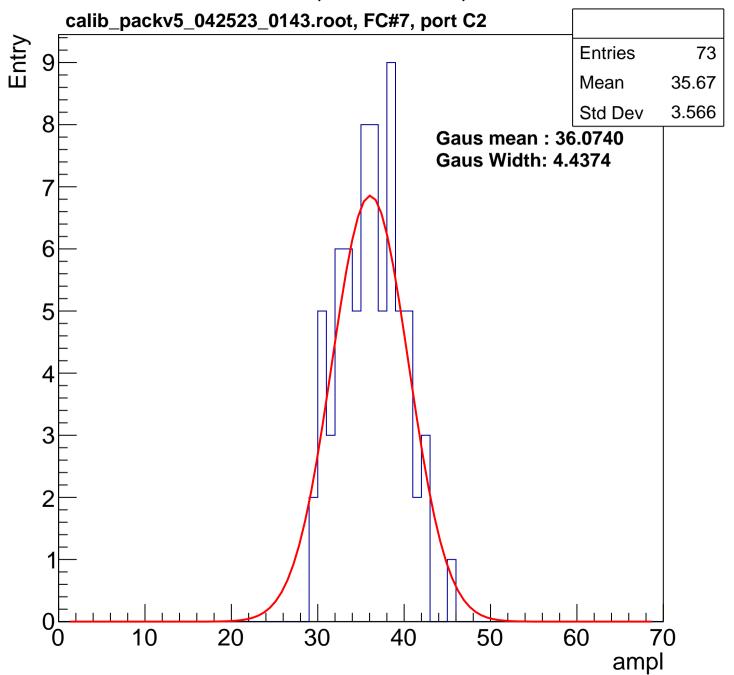


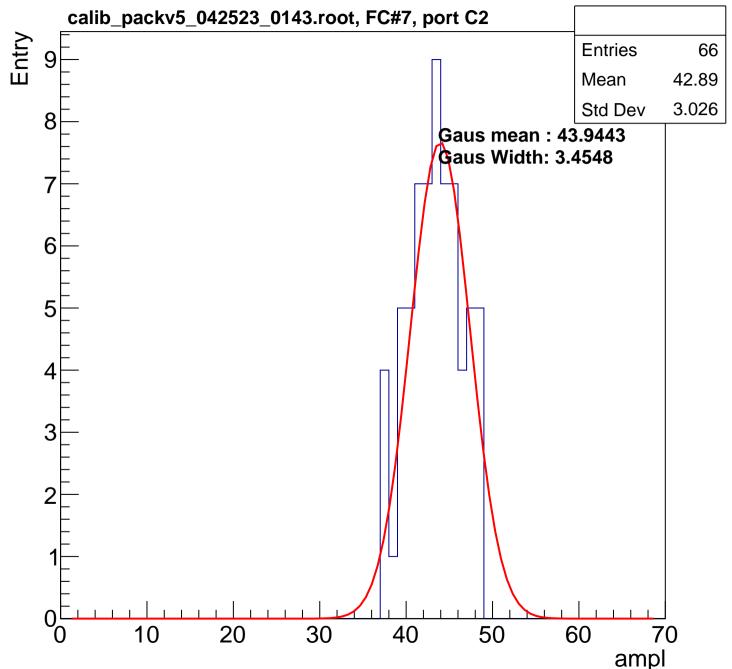


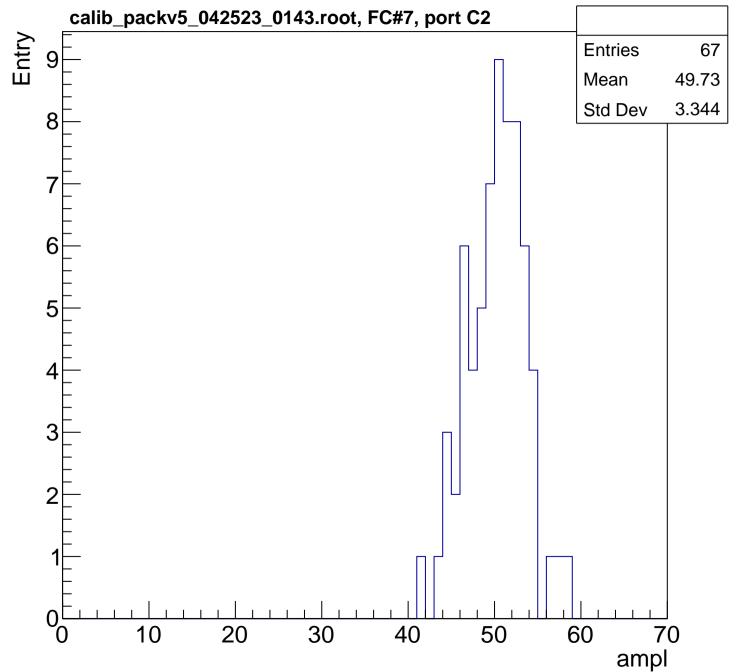


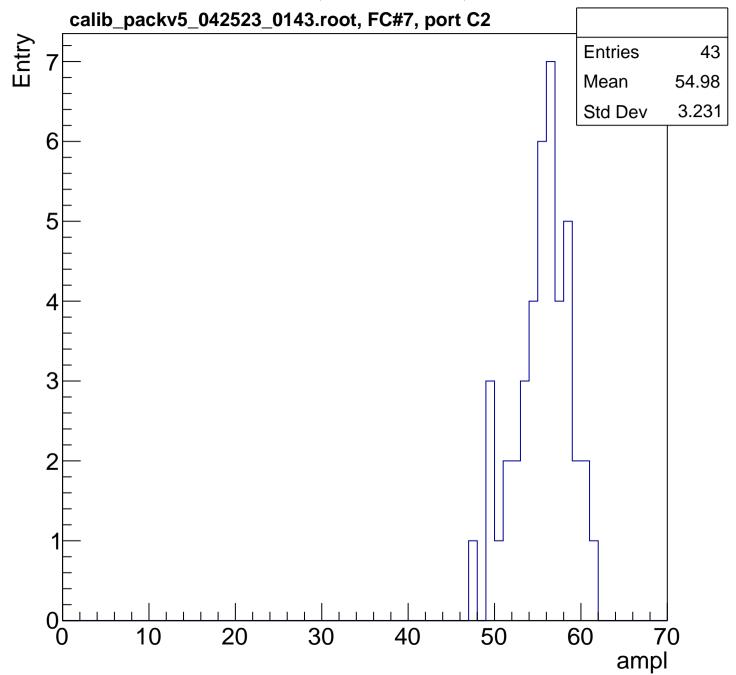


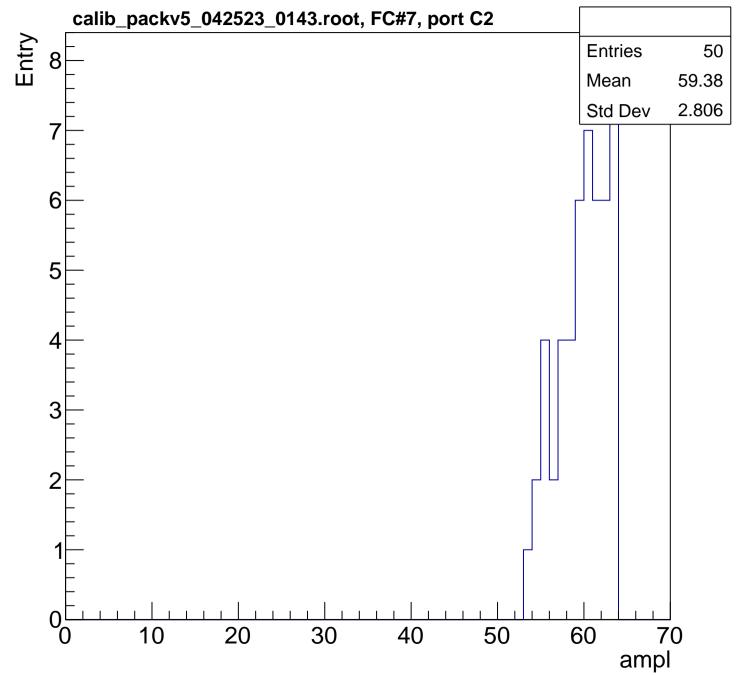


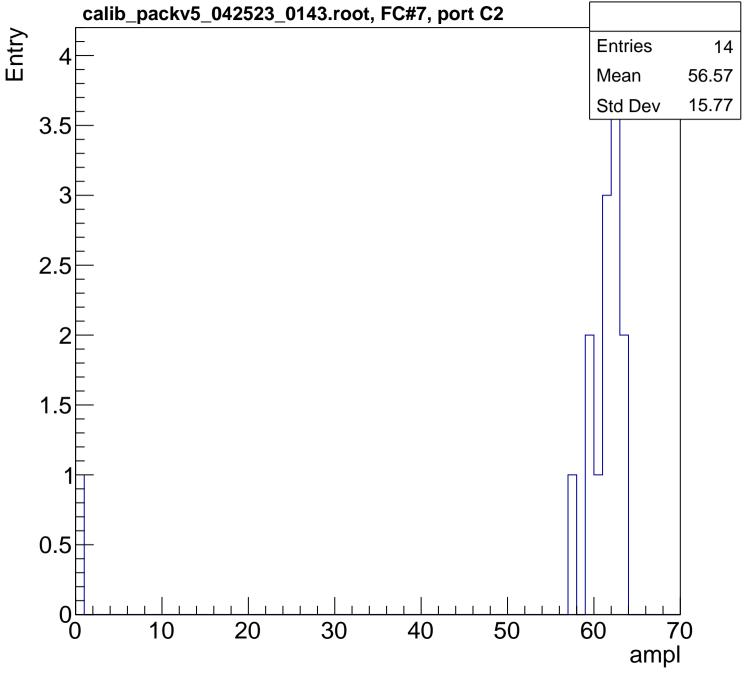


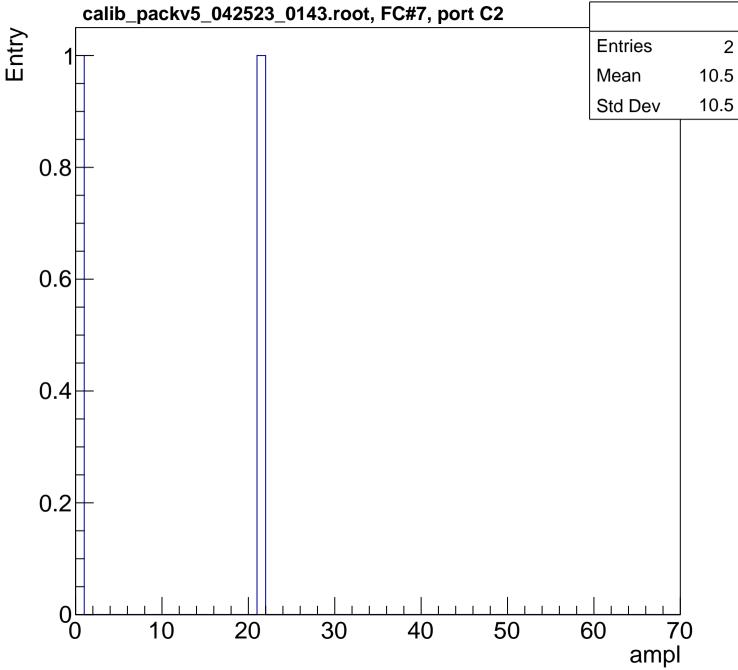


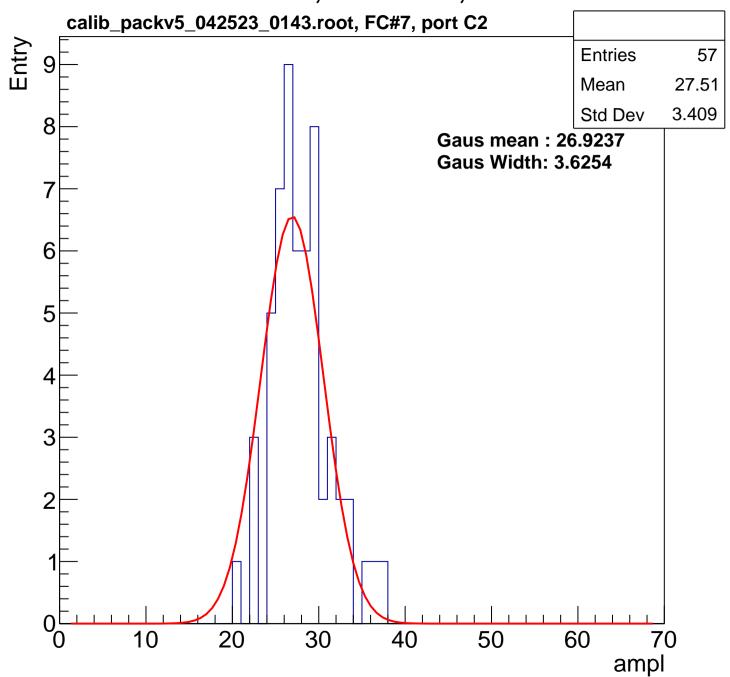


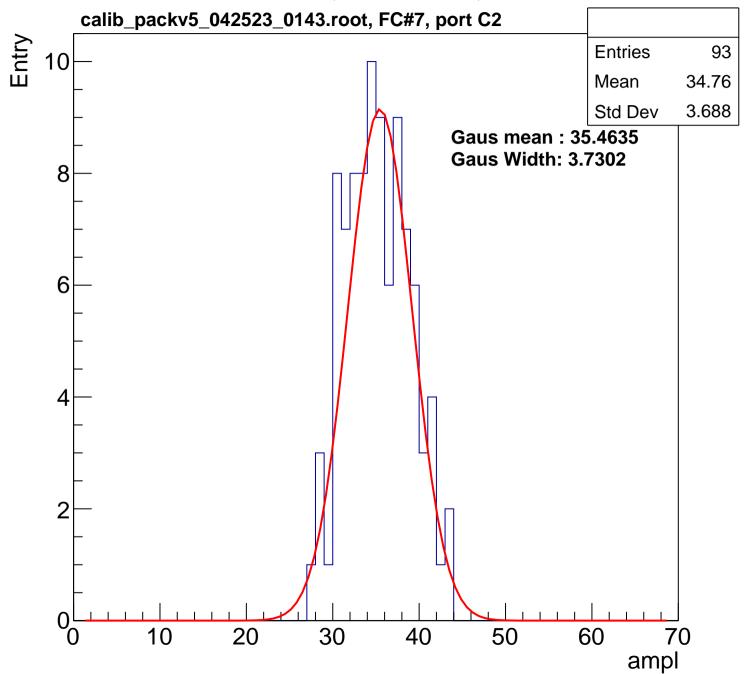


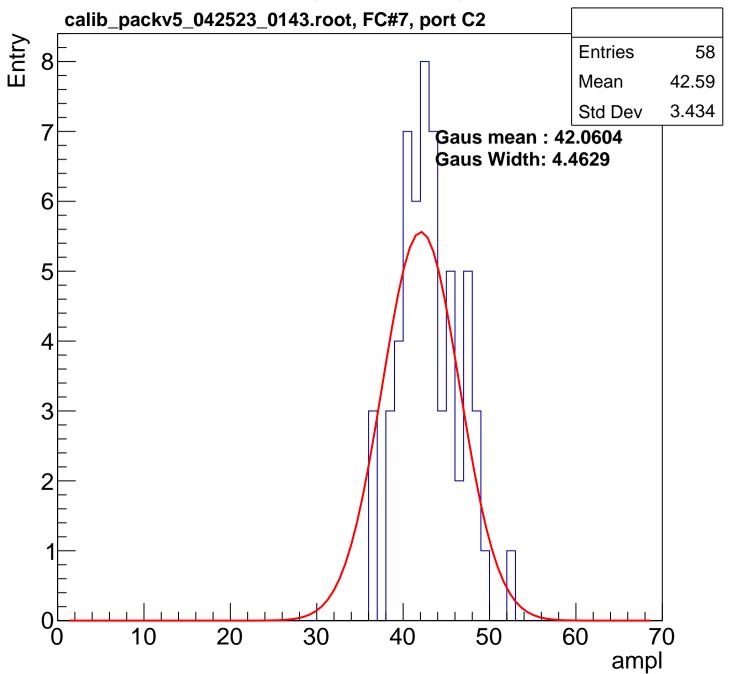


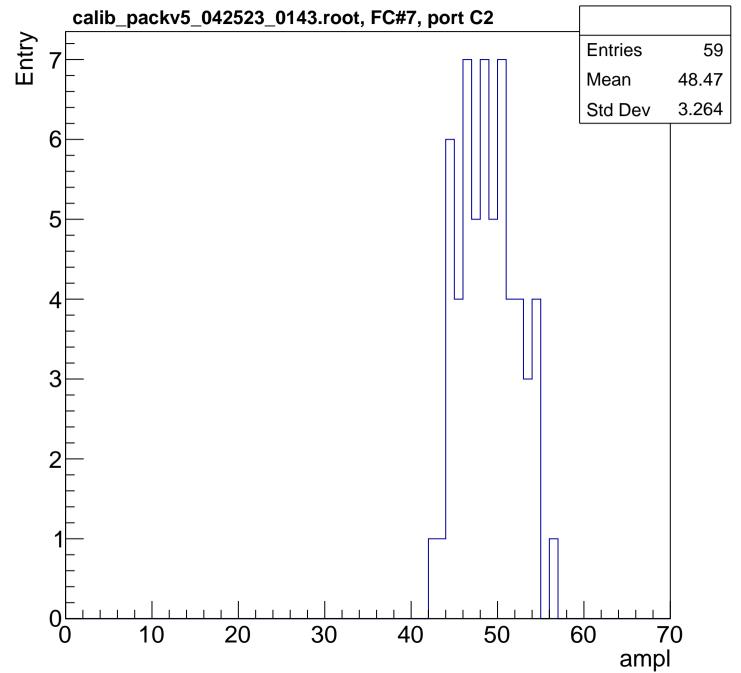


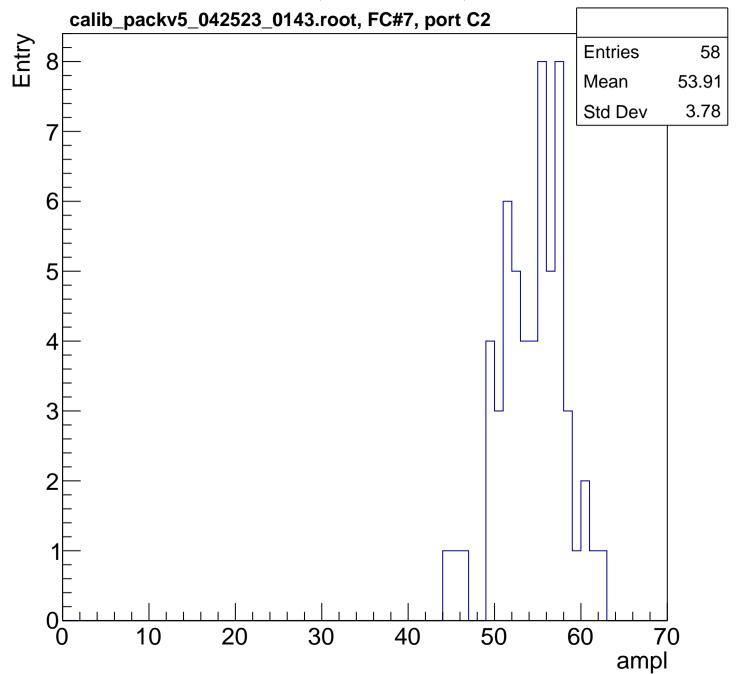


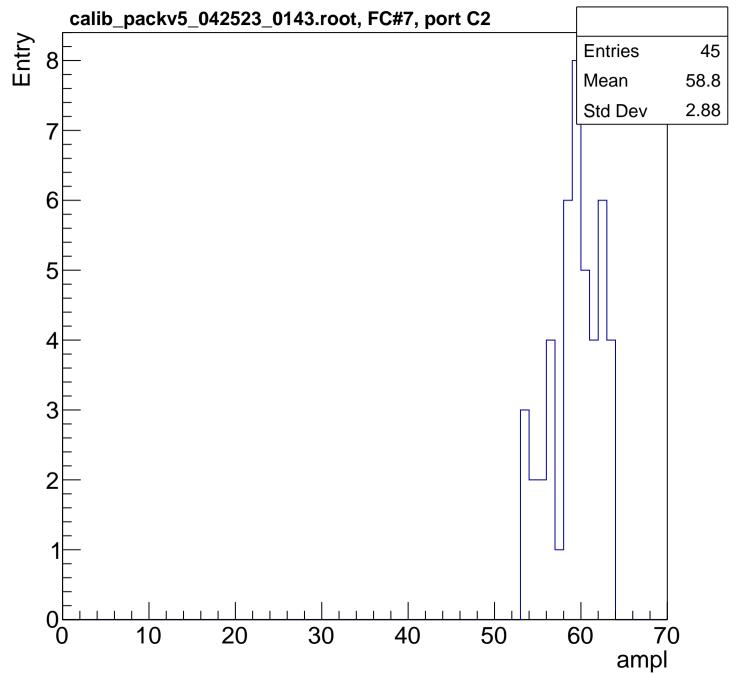


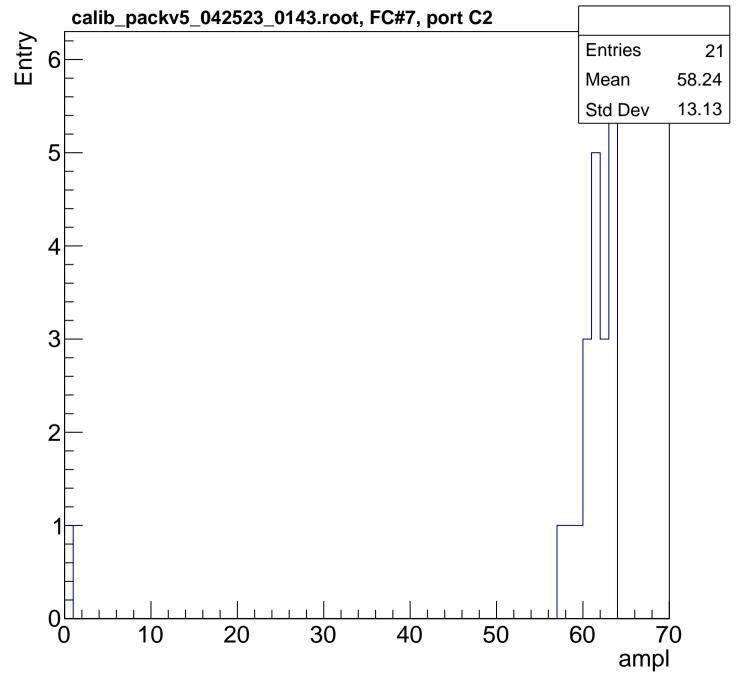


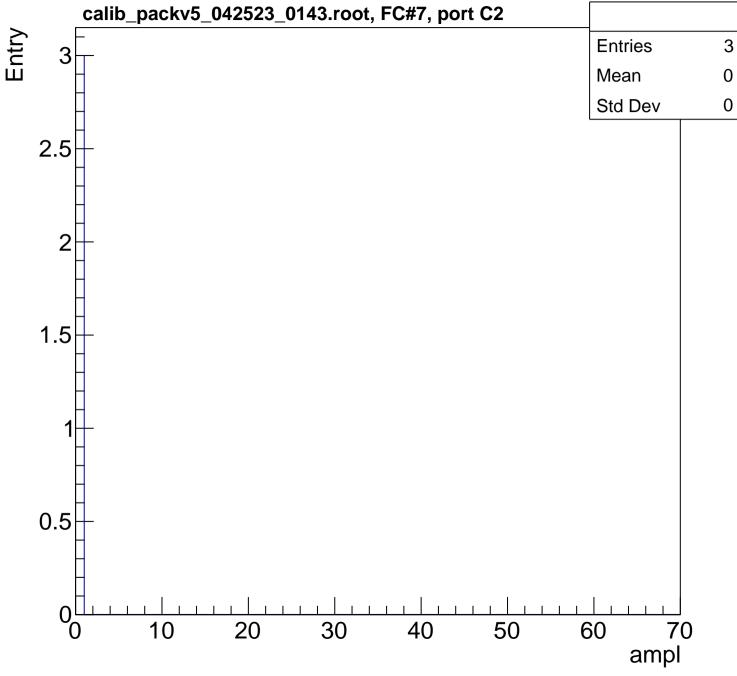


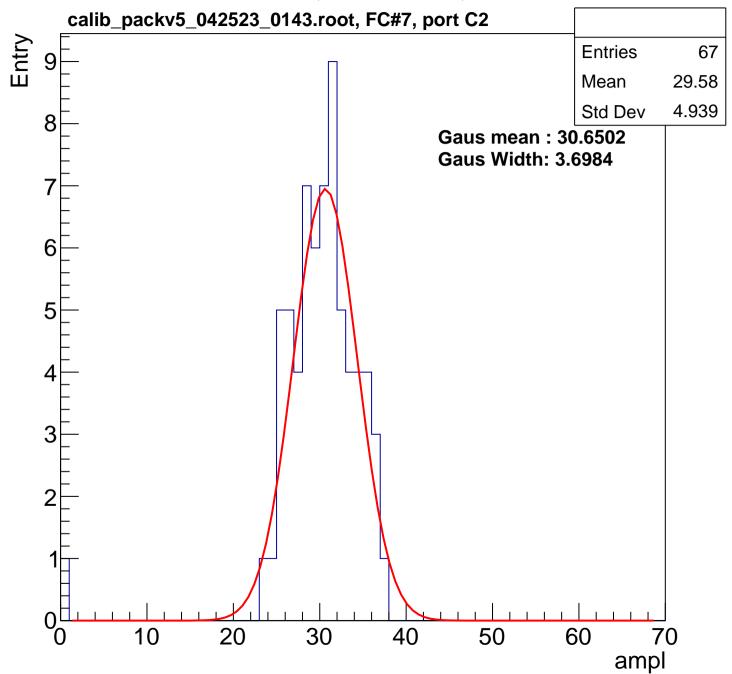


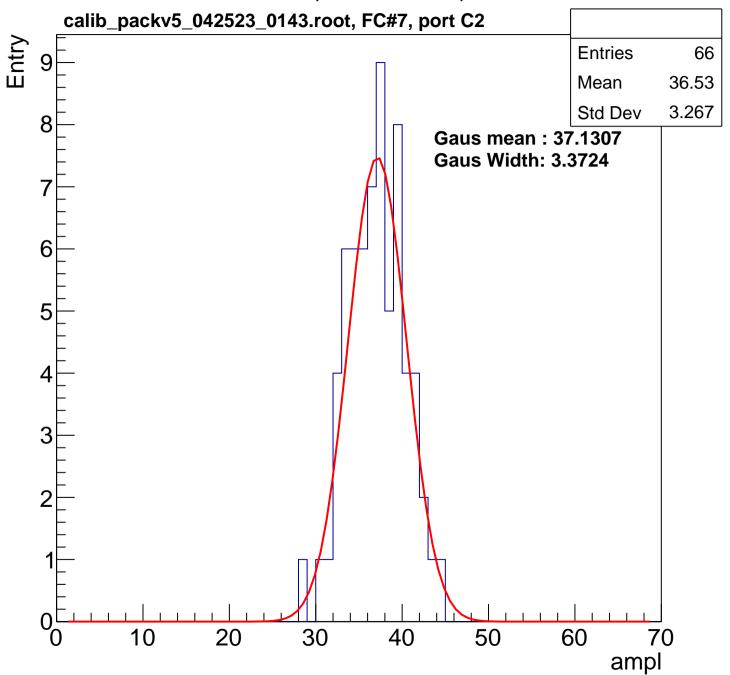


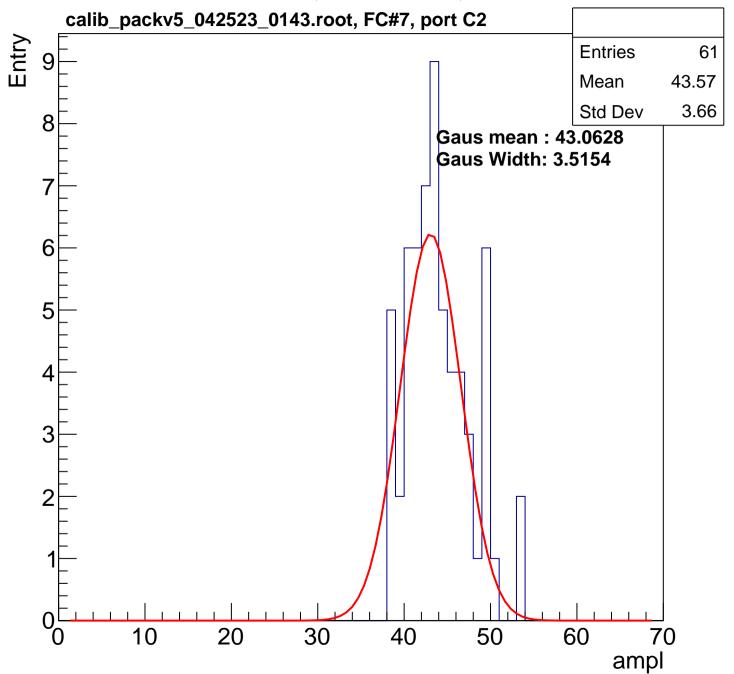


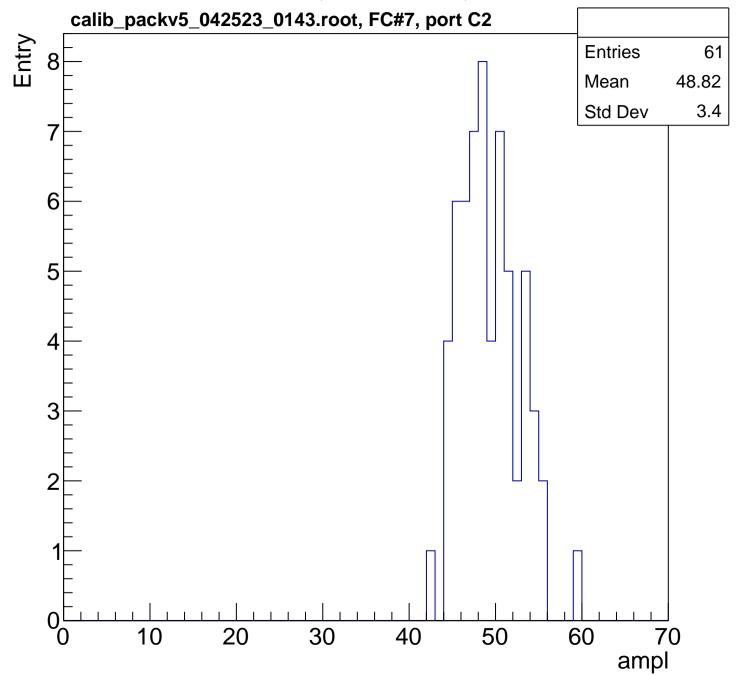


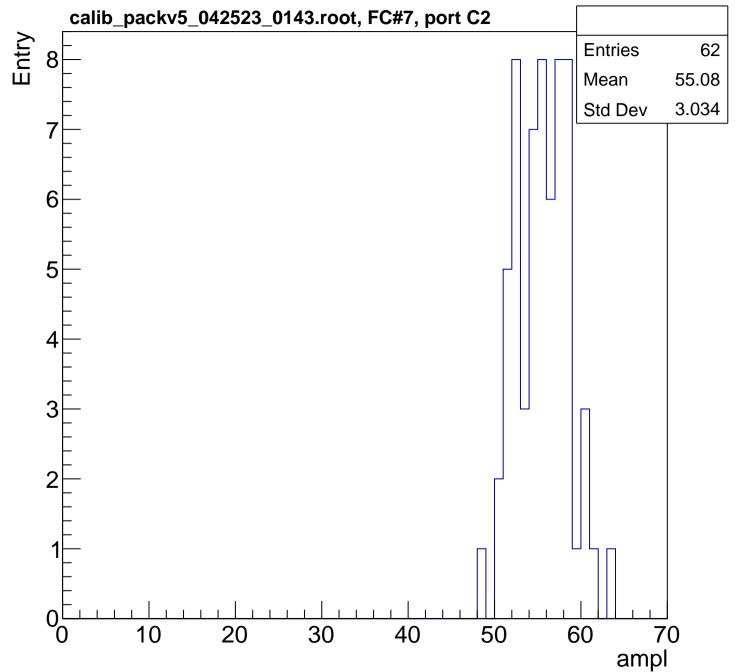


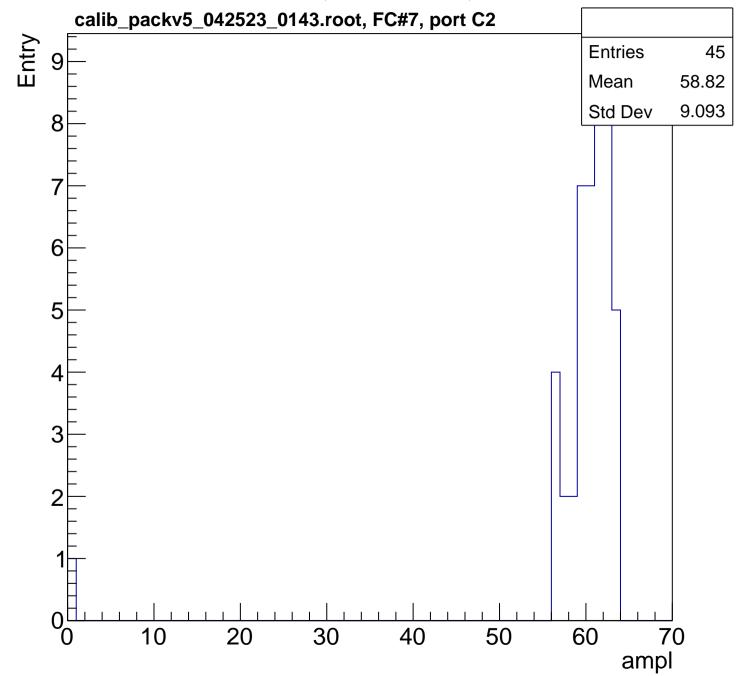


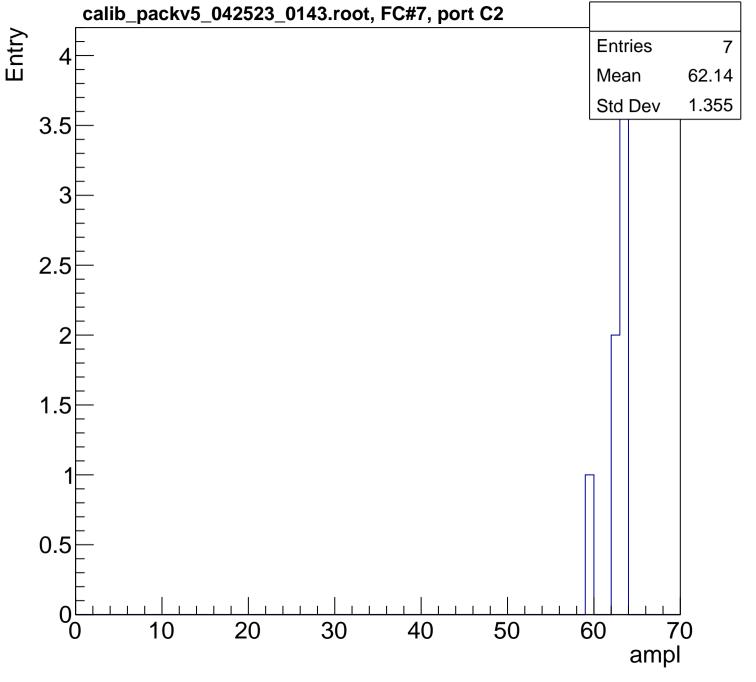






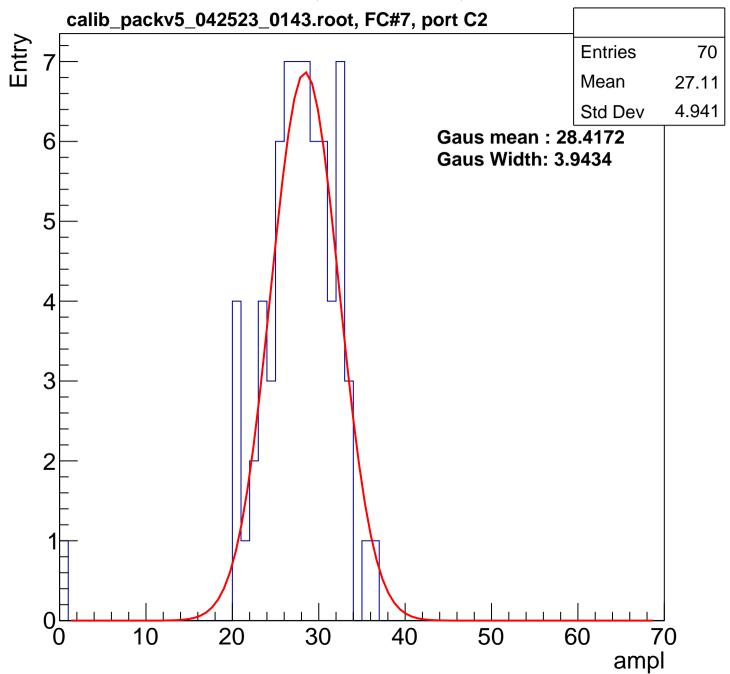


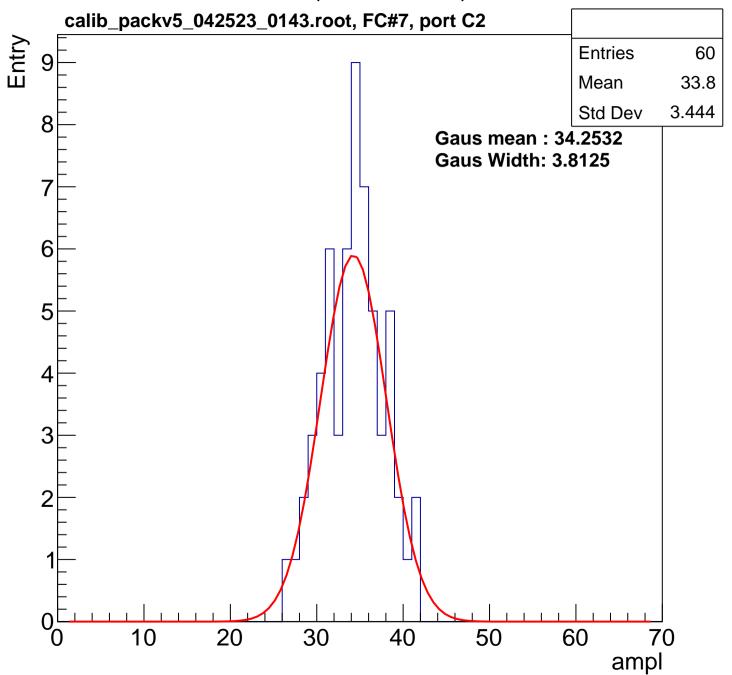


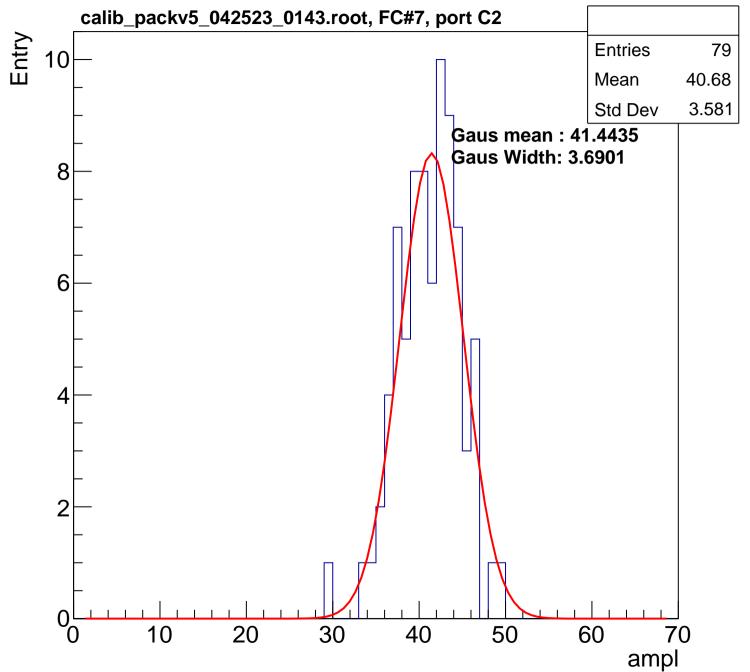


B1L103S, U4-ch31, adc7 calib_packv5_042523_0143.root, FC#7, port C2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70

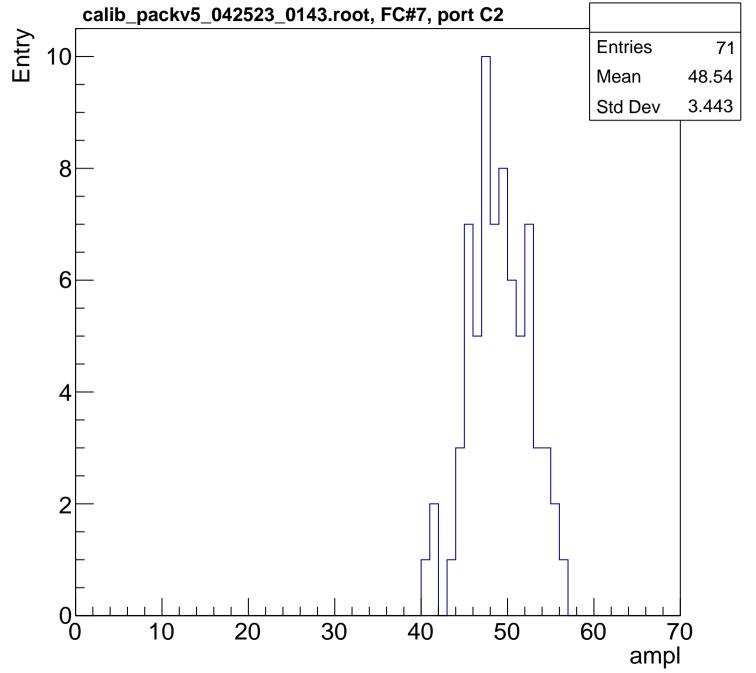
ampl

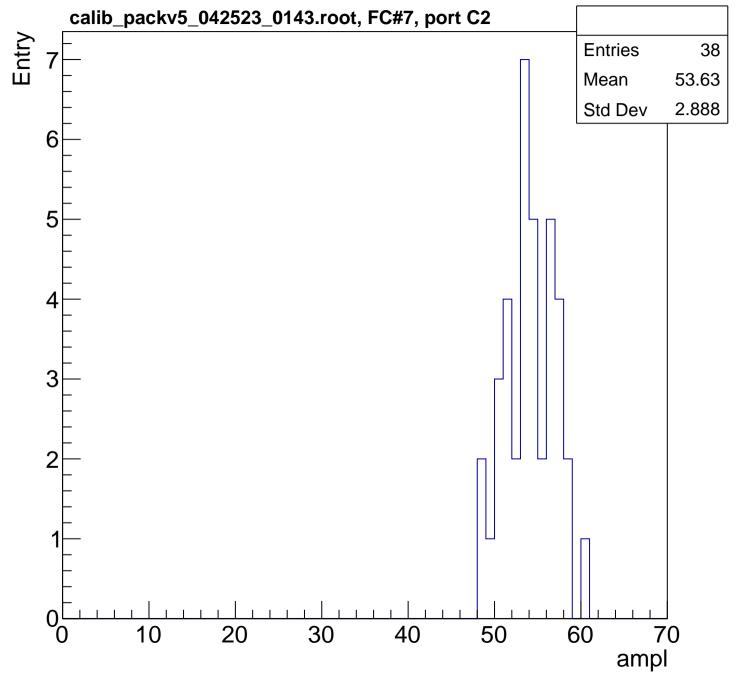


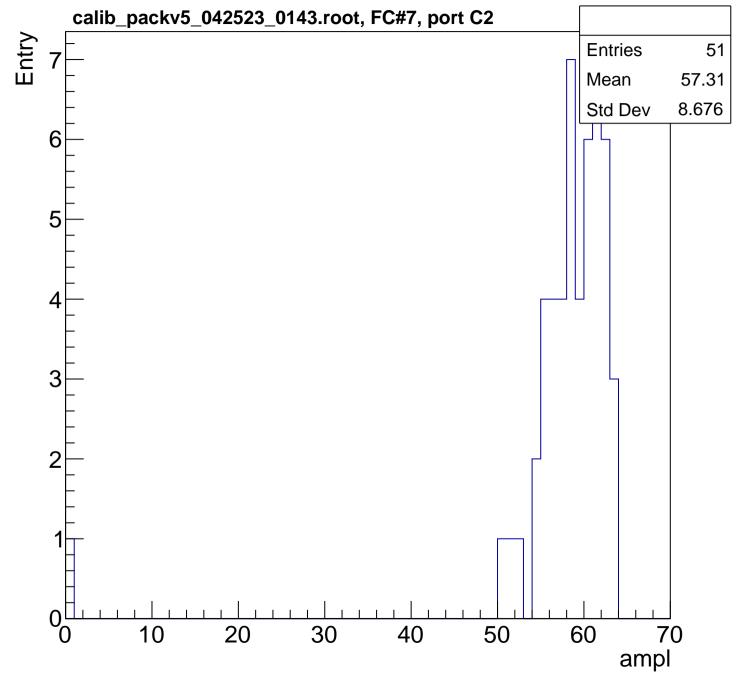


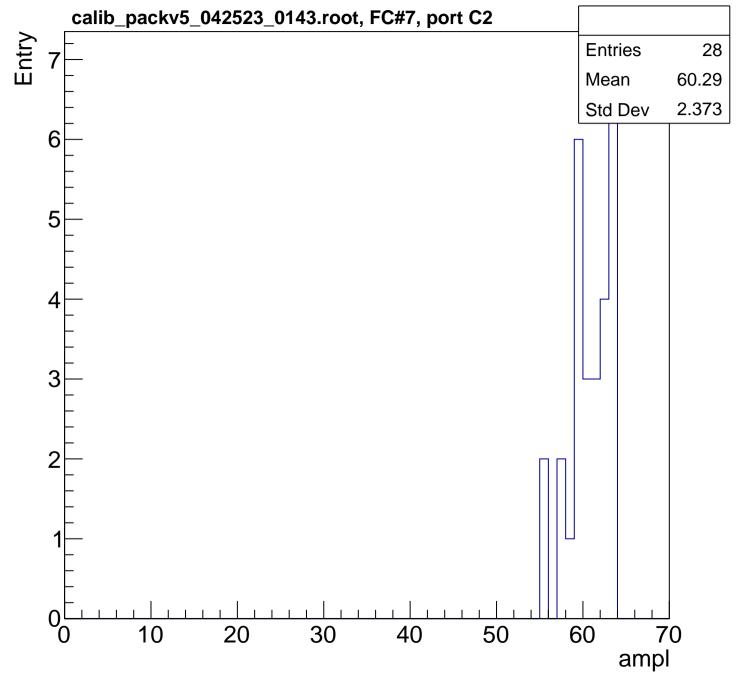


B1L103S, U4-ch32, adc3

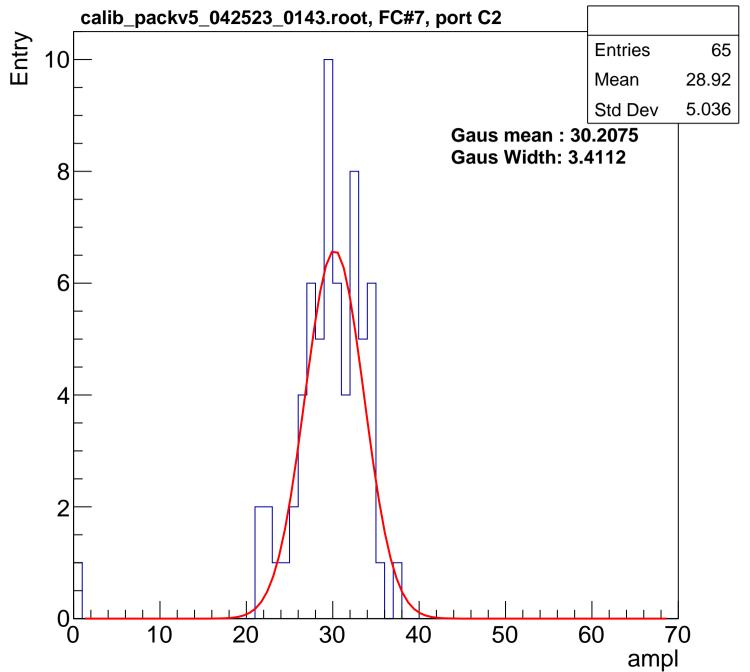


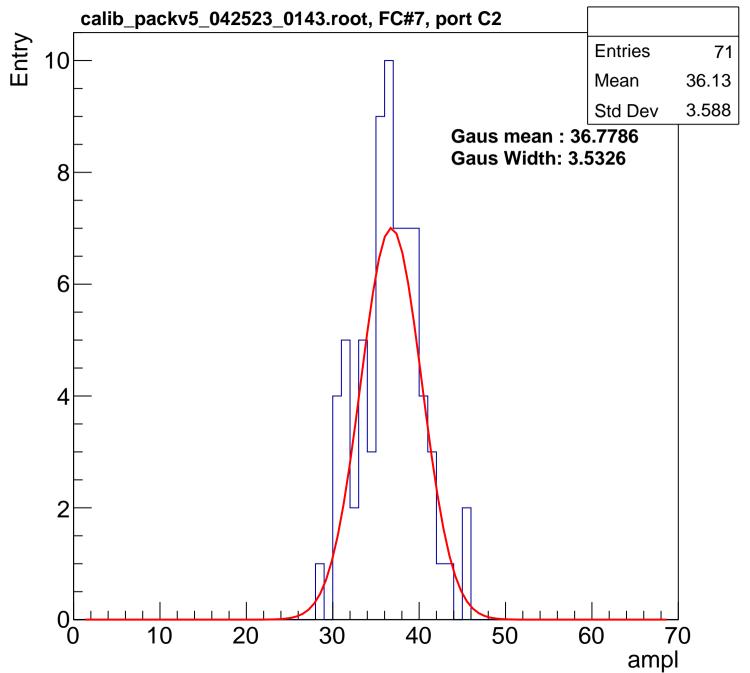


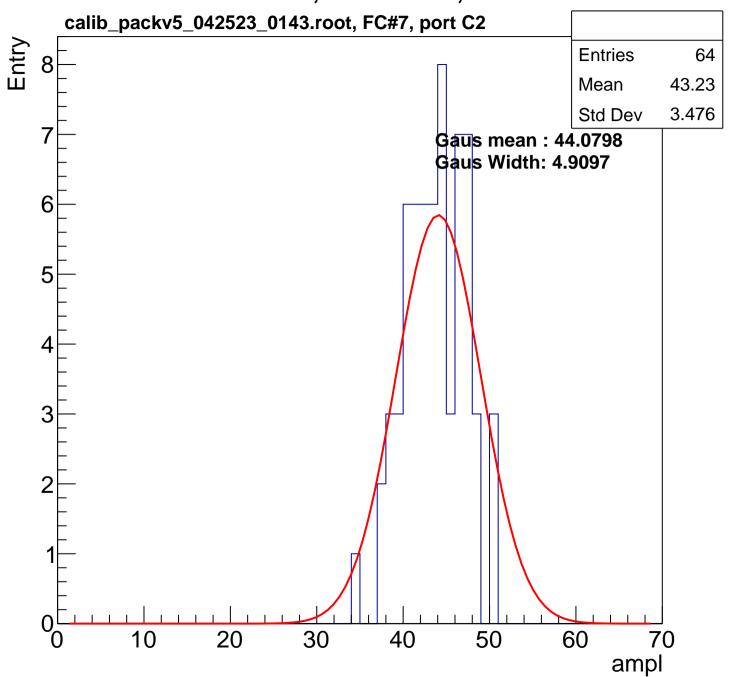


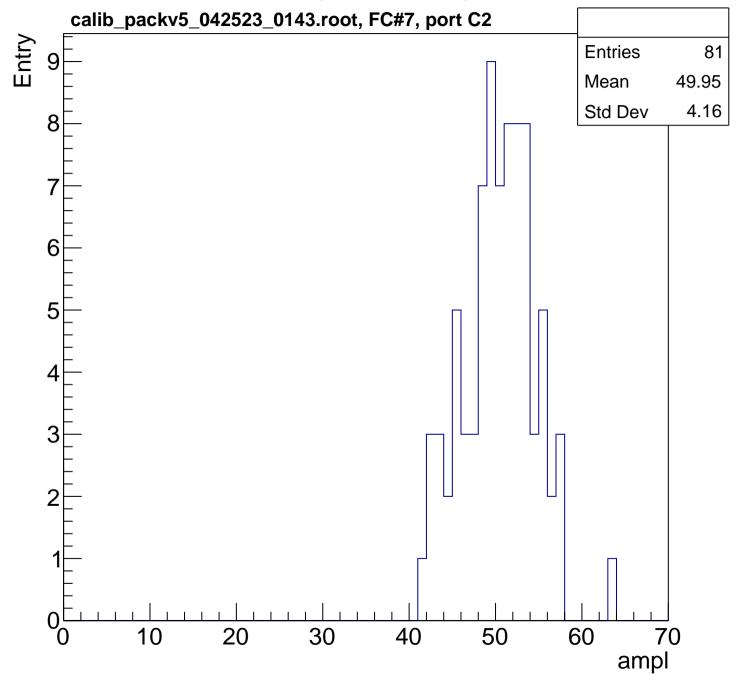


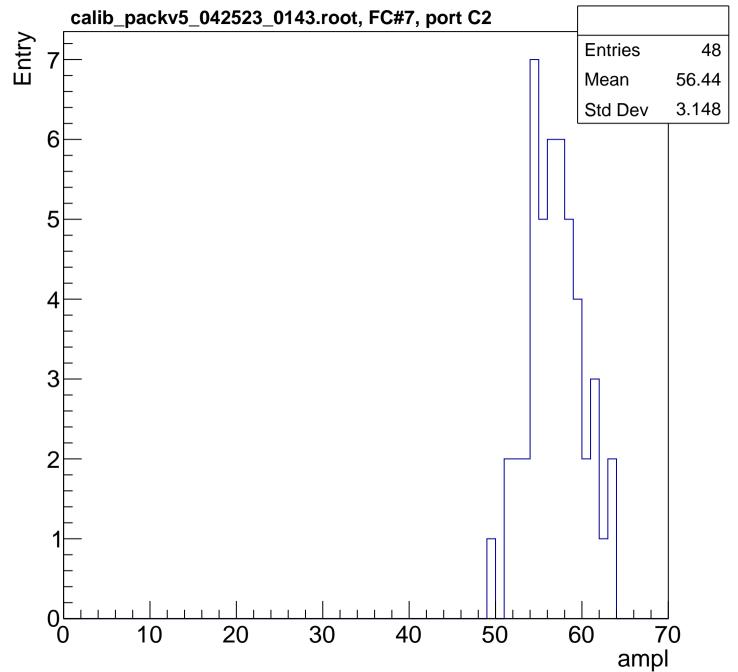
B1L103S, U4-ch32, adc7 calib_packv5_042523_0143.root, FC#7, port C2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

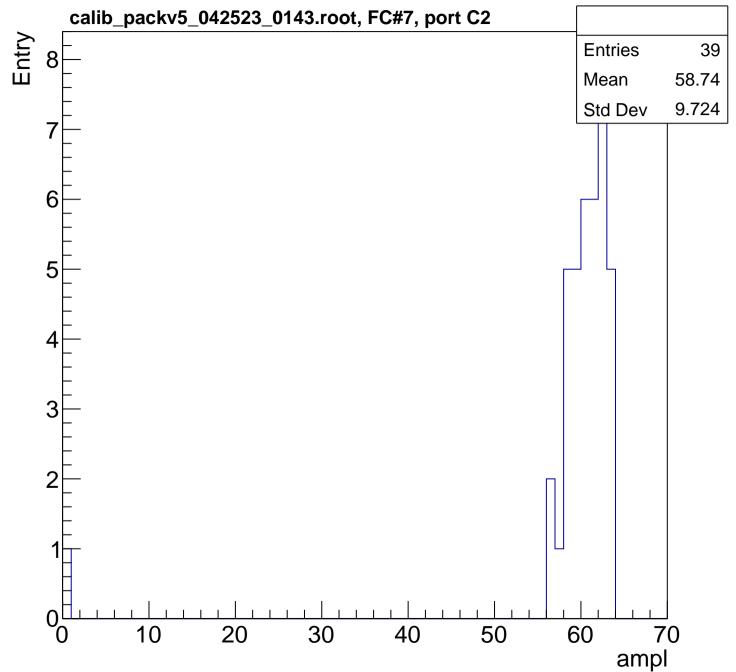


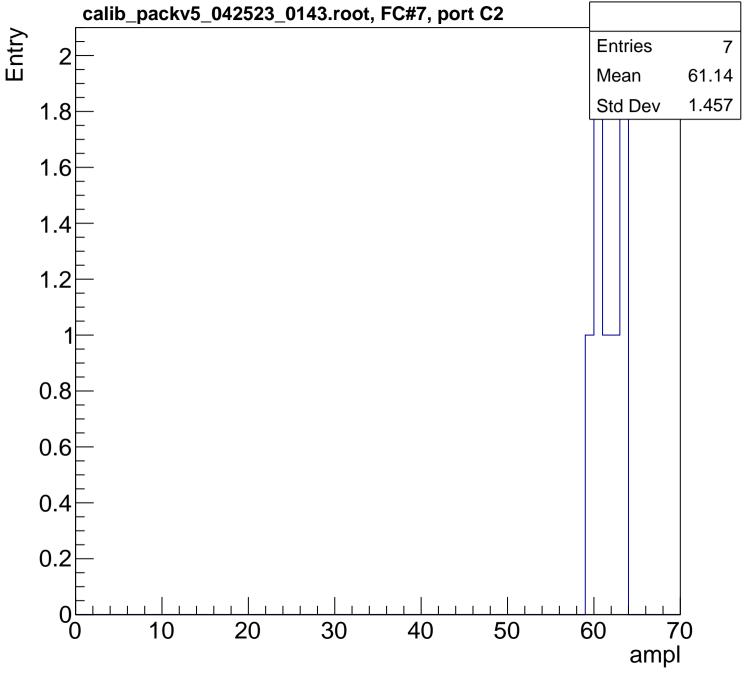




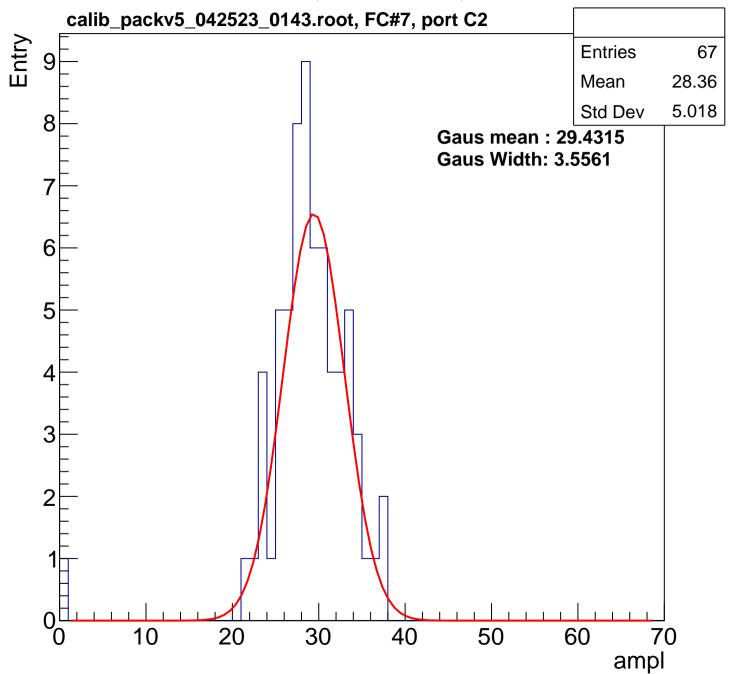


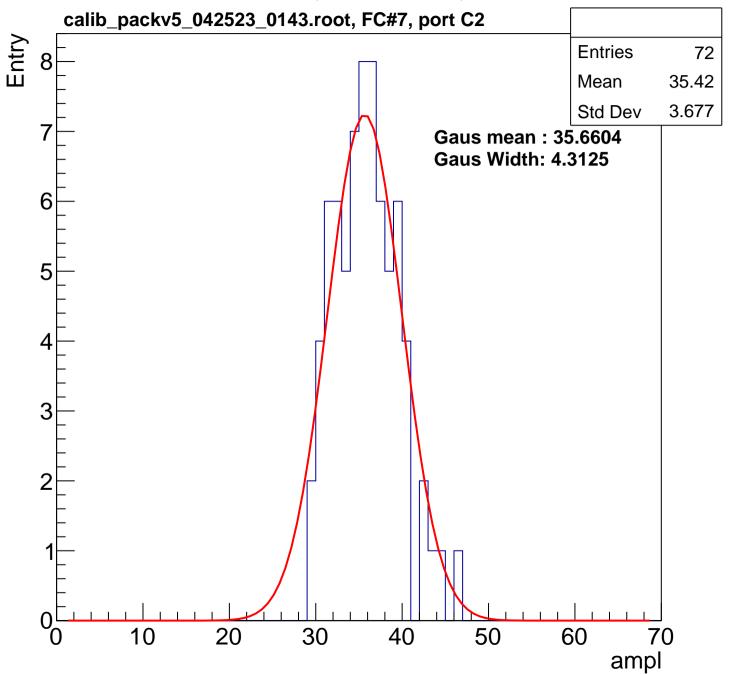


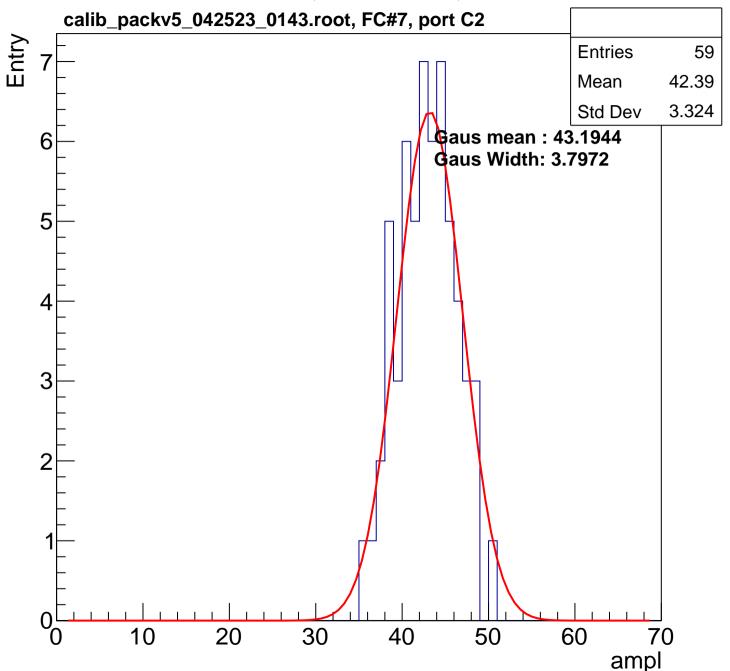


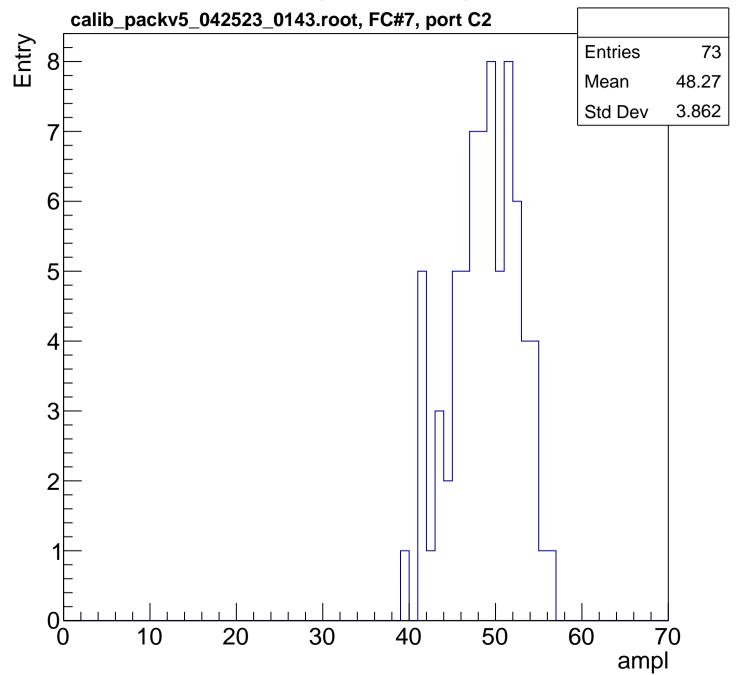


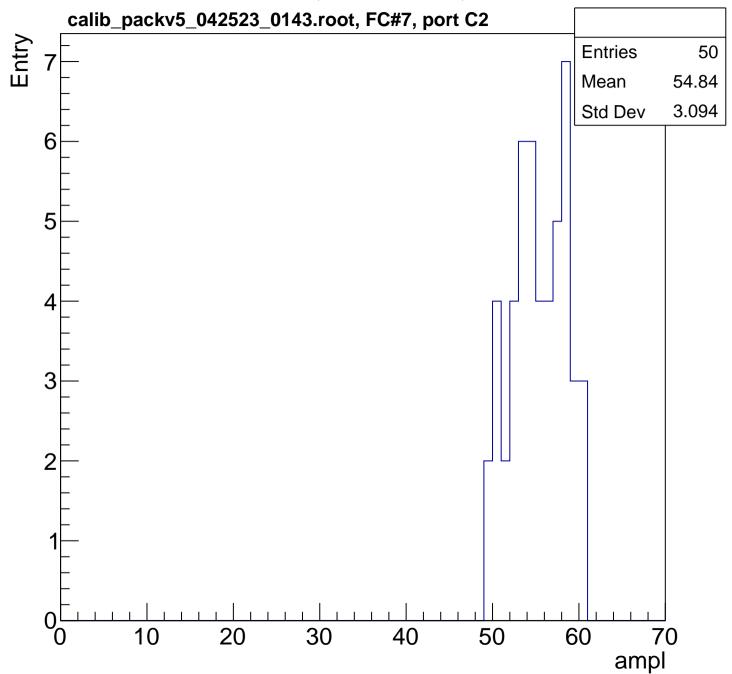
B1L103S, U4-ch33, adc7 calib_packv5_042523_0143.root, FC#7, port C2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

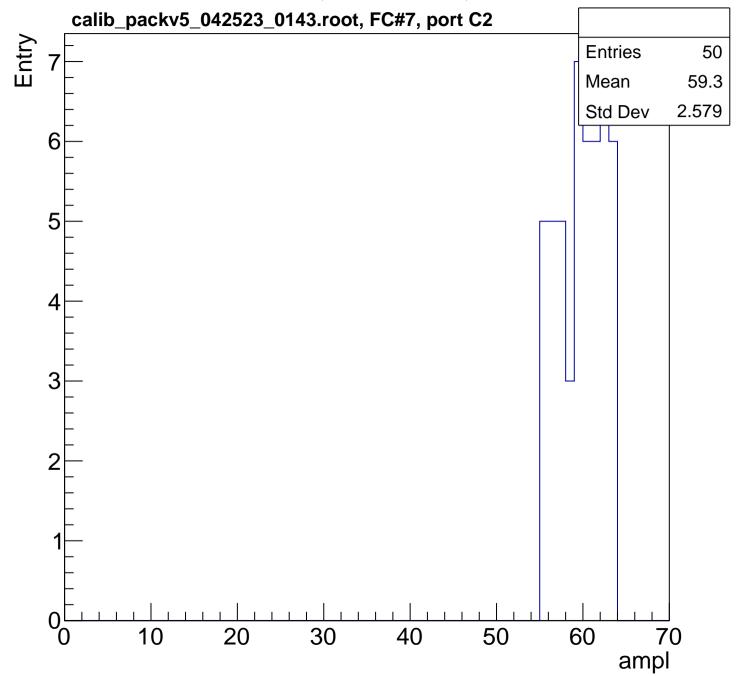


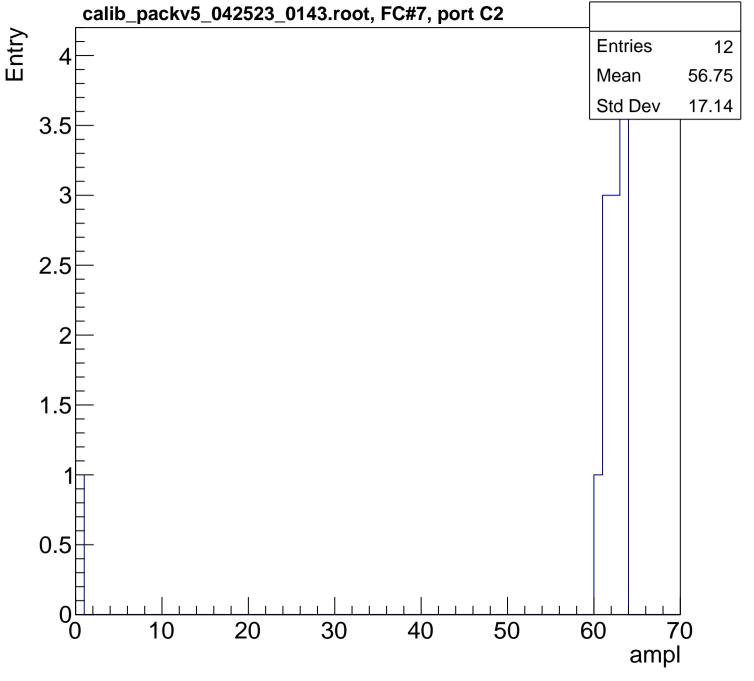


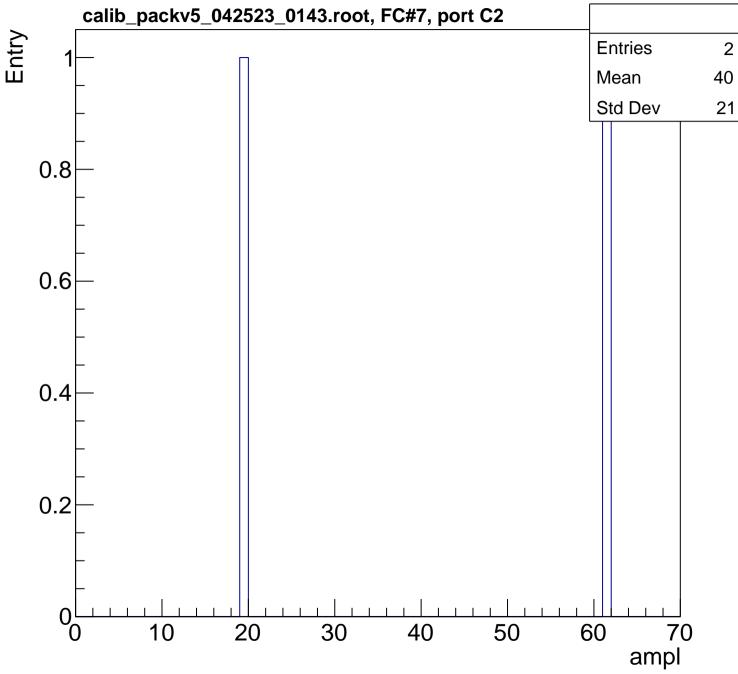


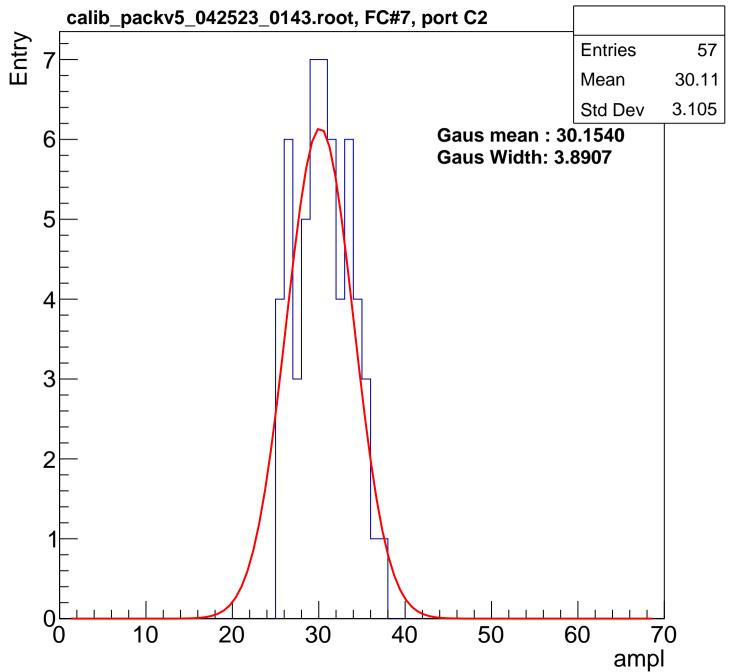


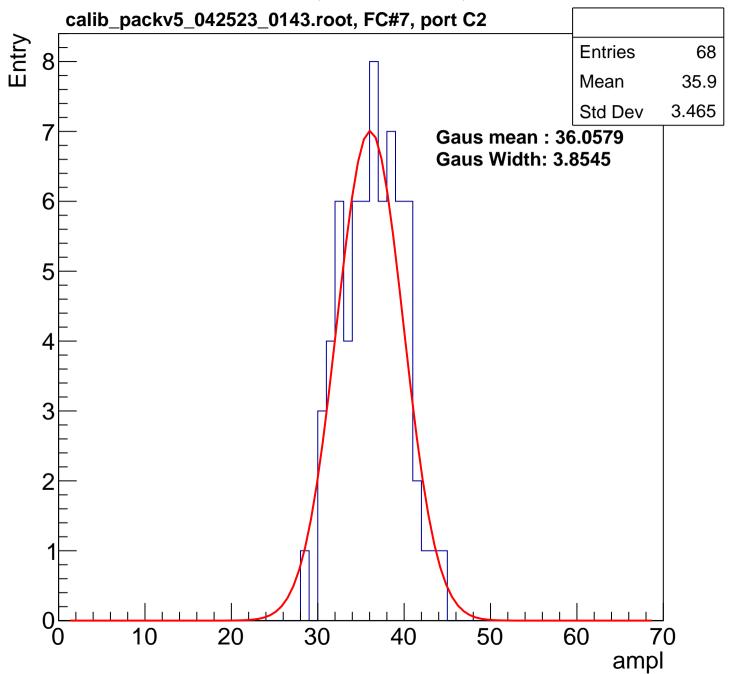


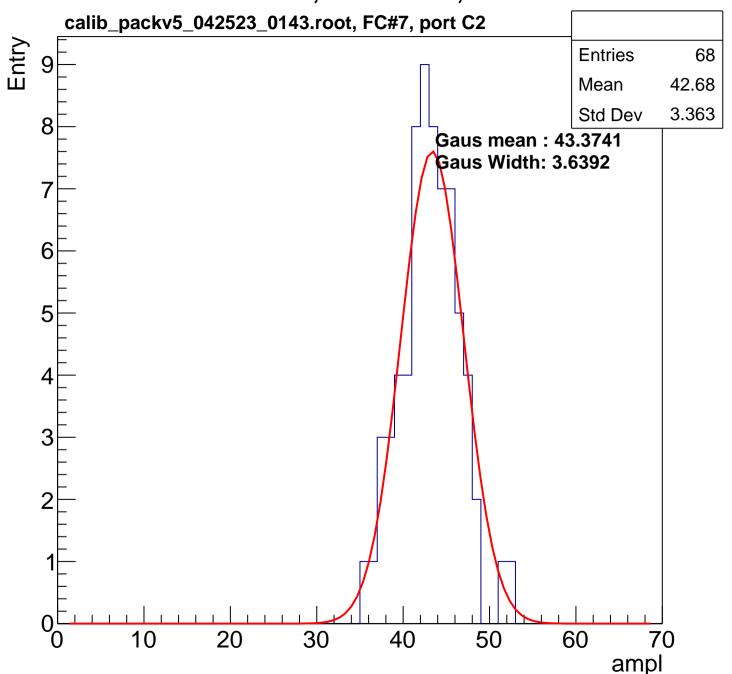


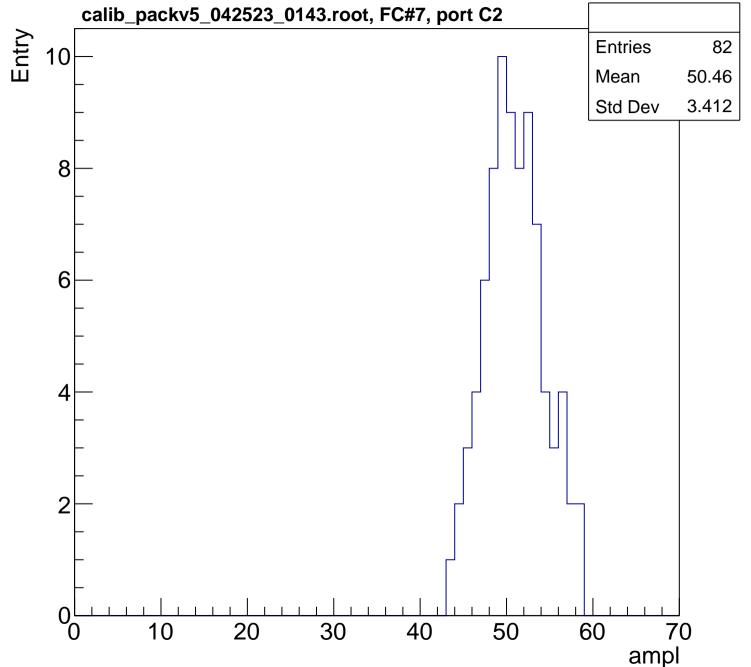


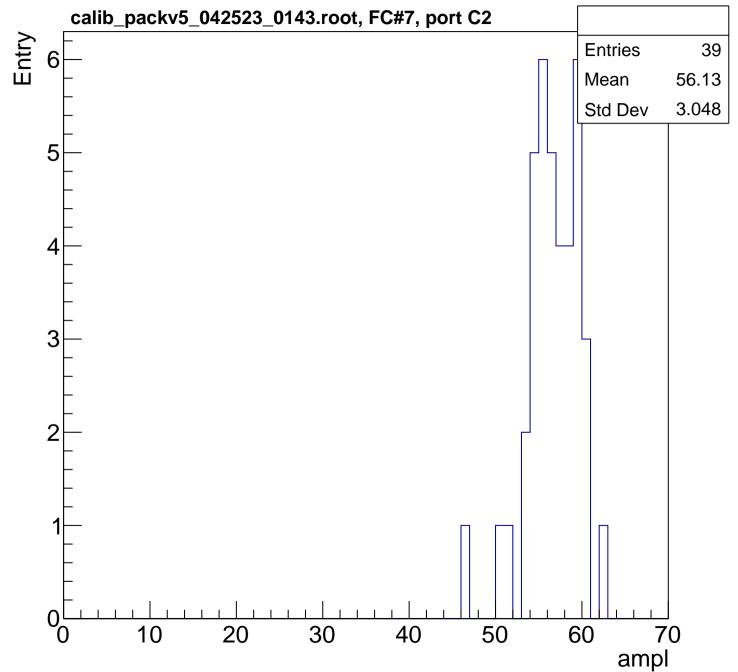


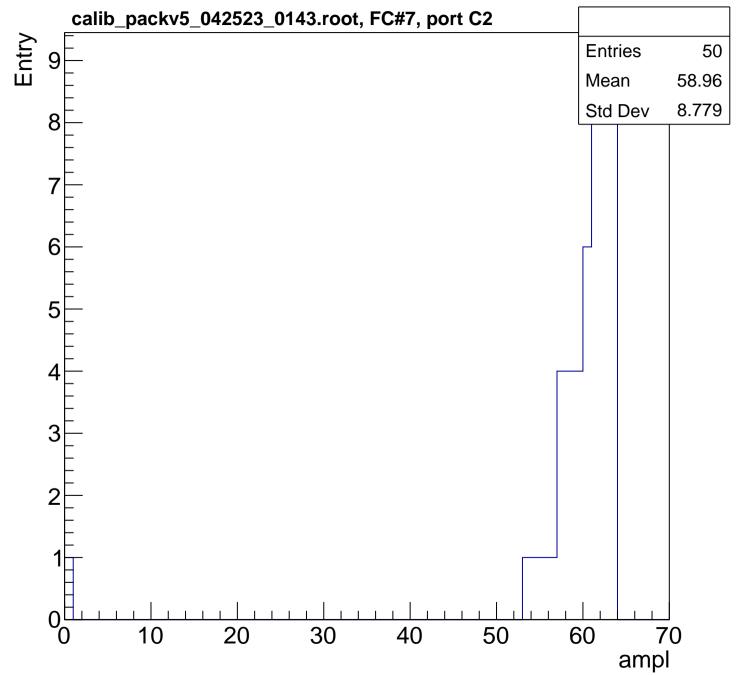


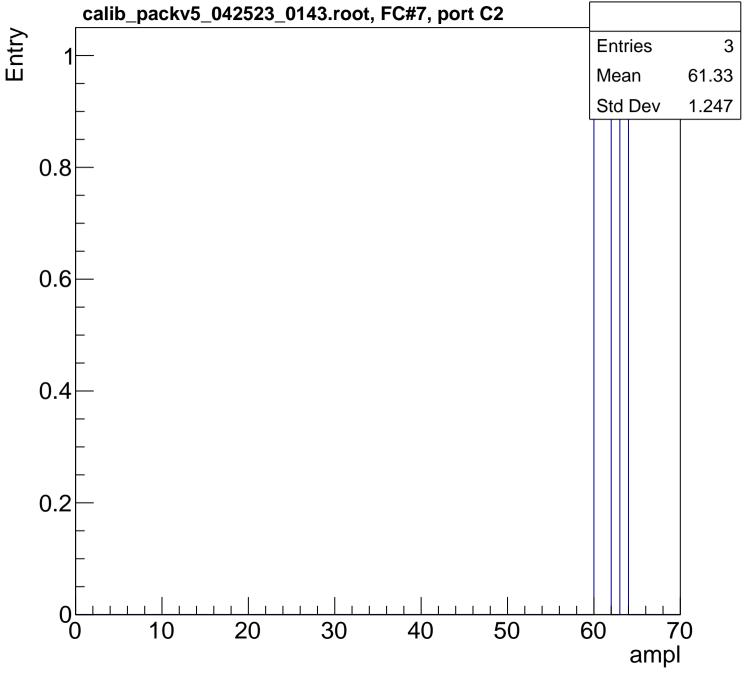


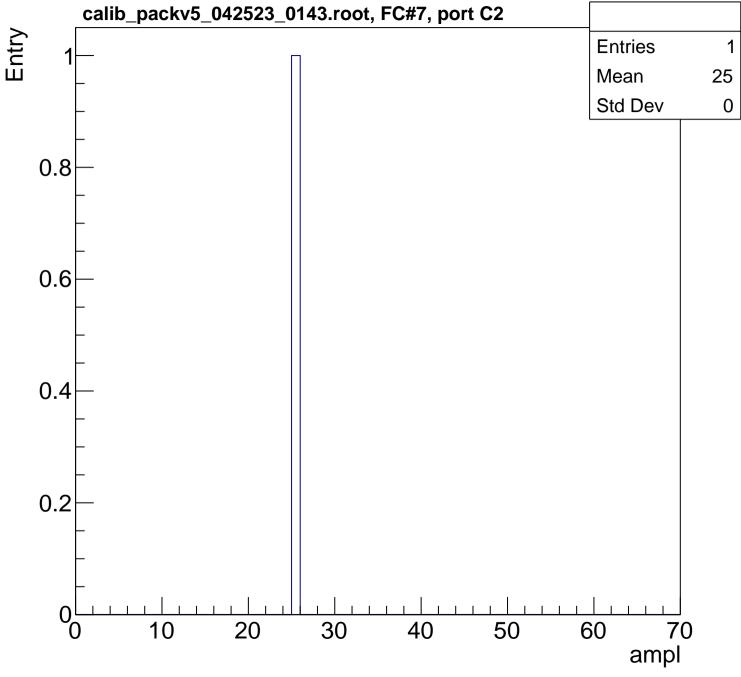


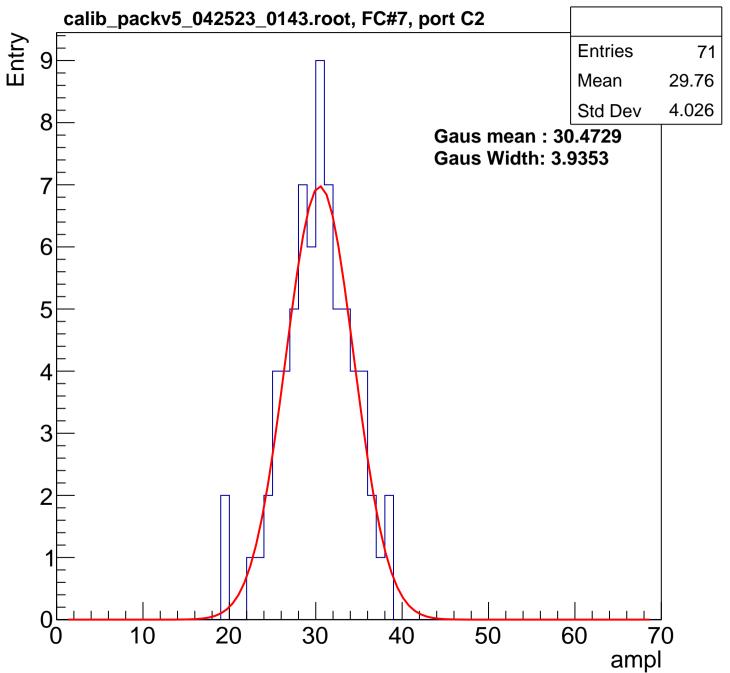


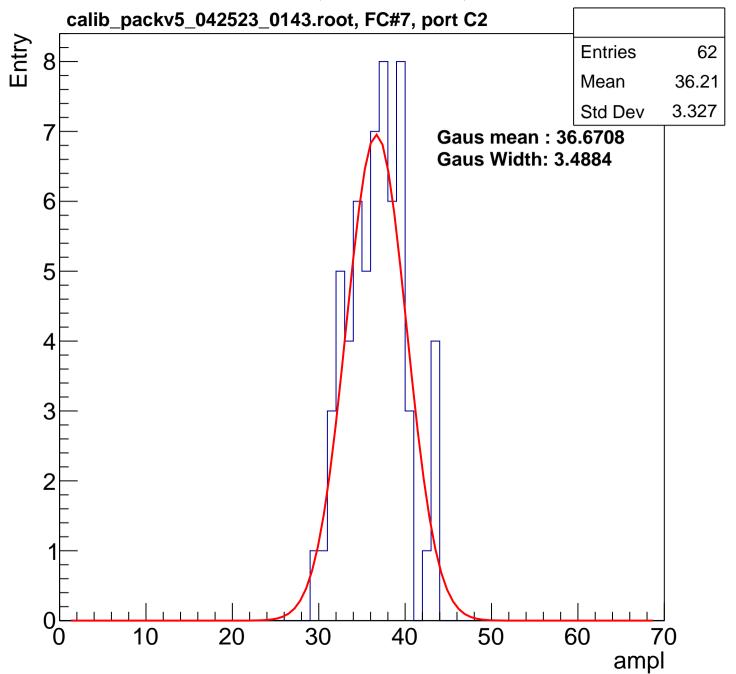


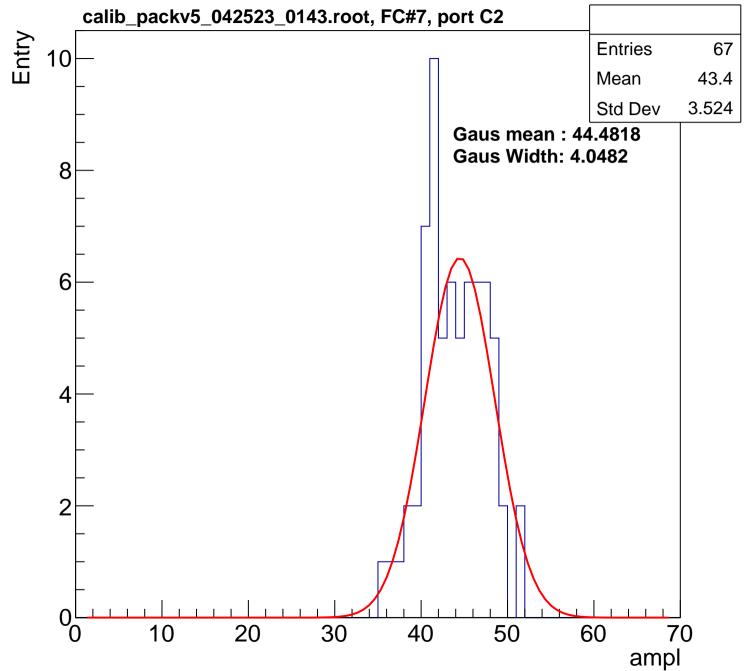


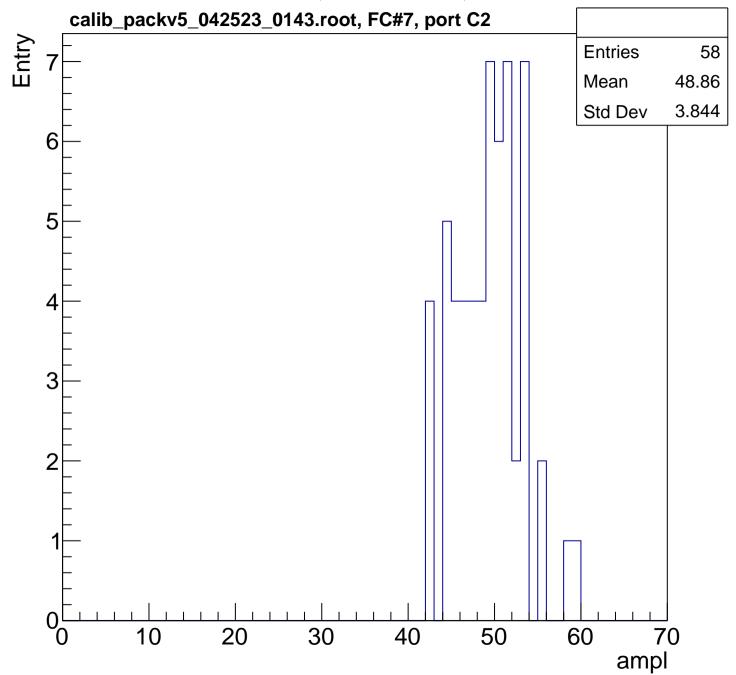


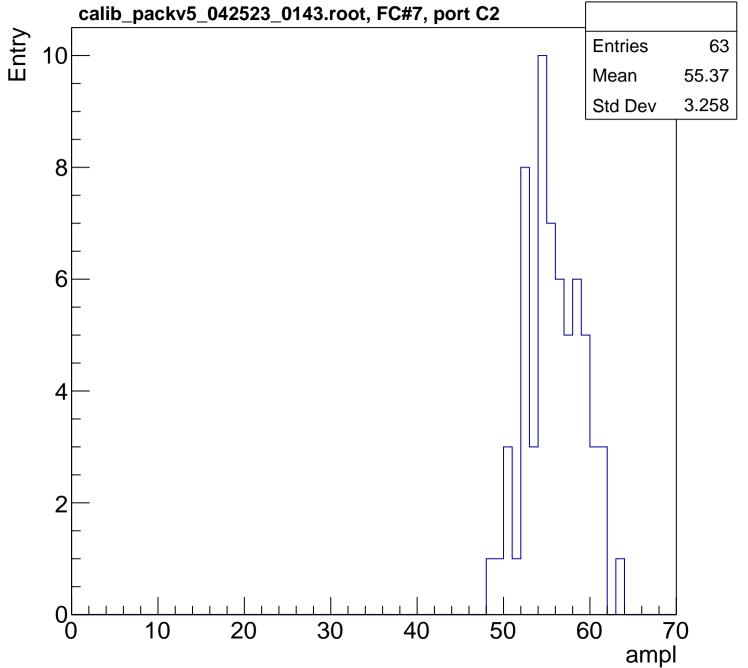


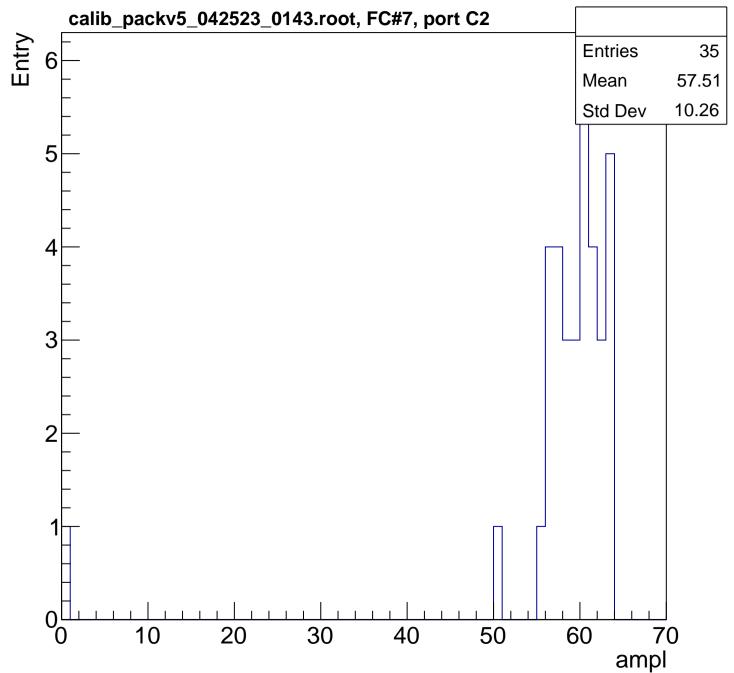


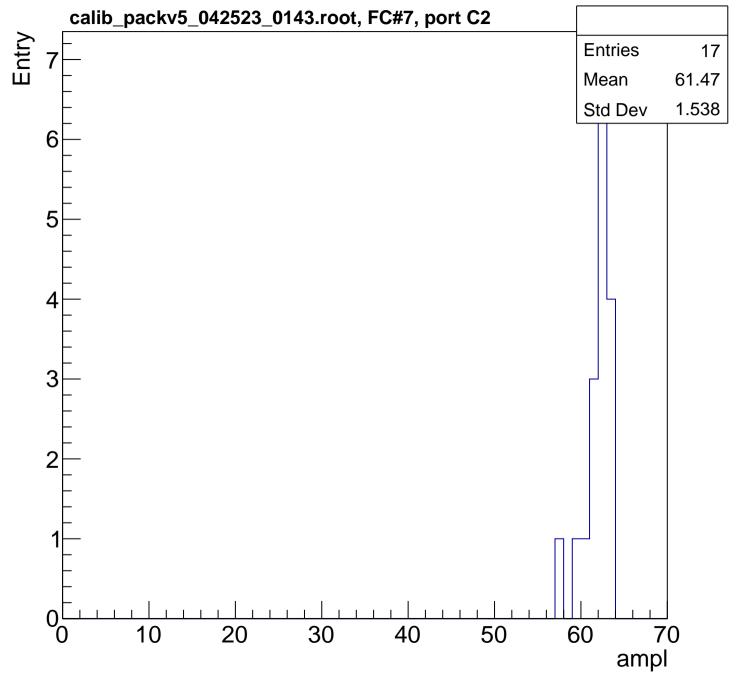


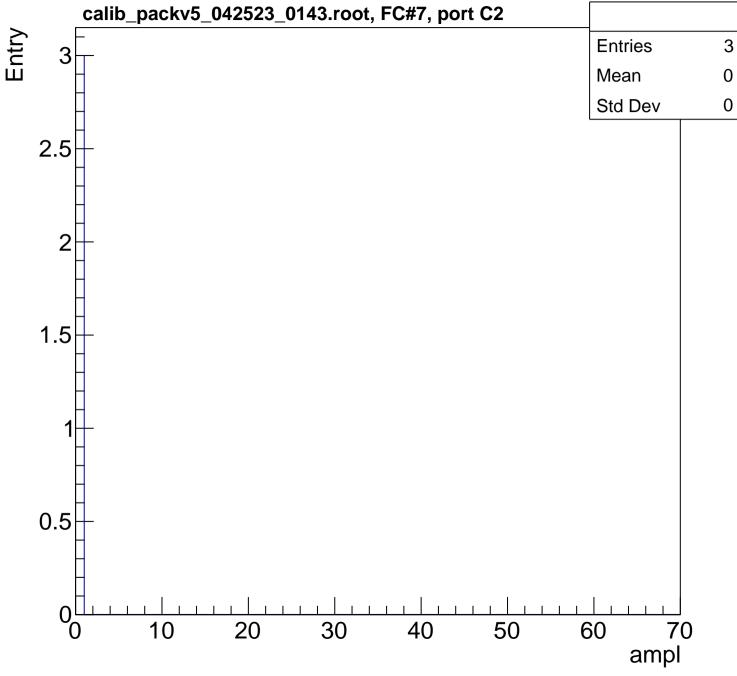


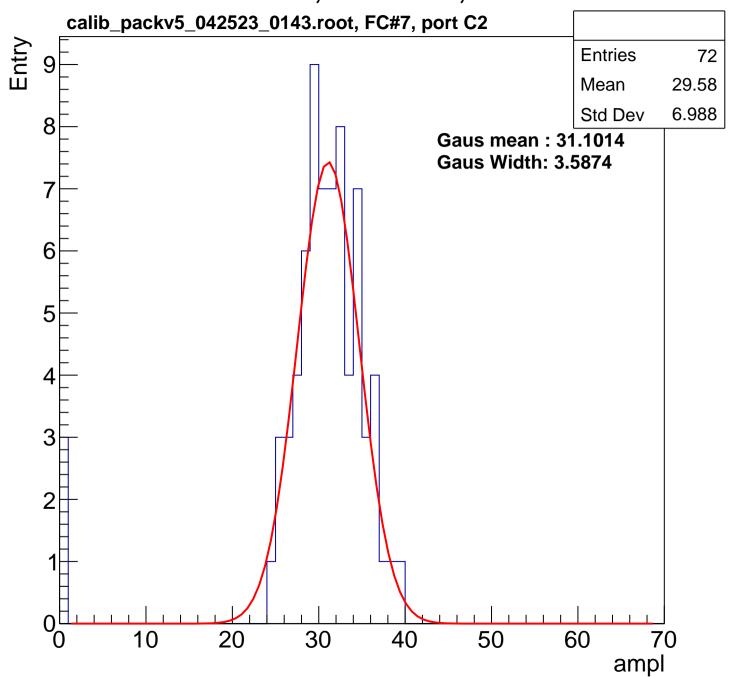


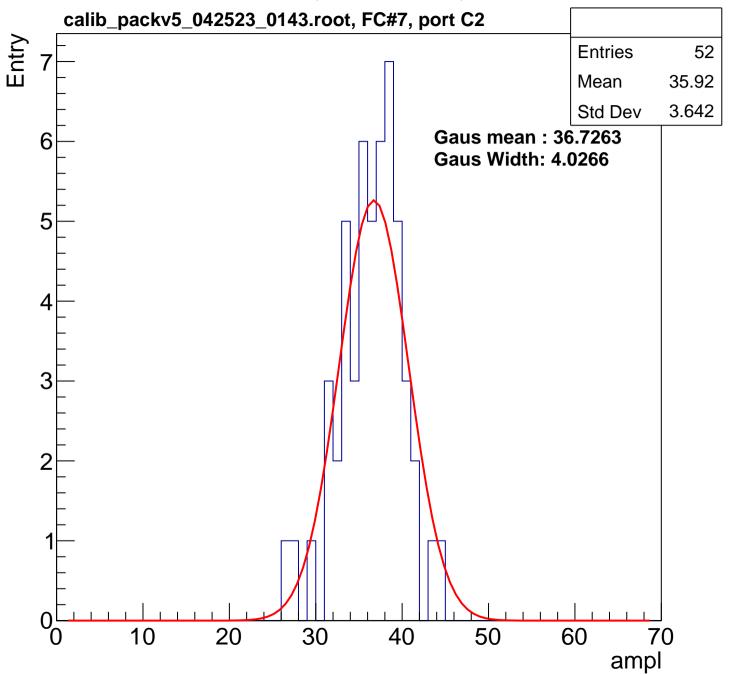


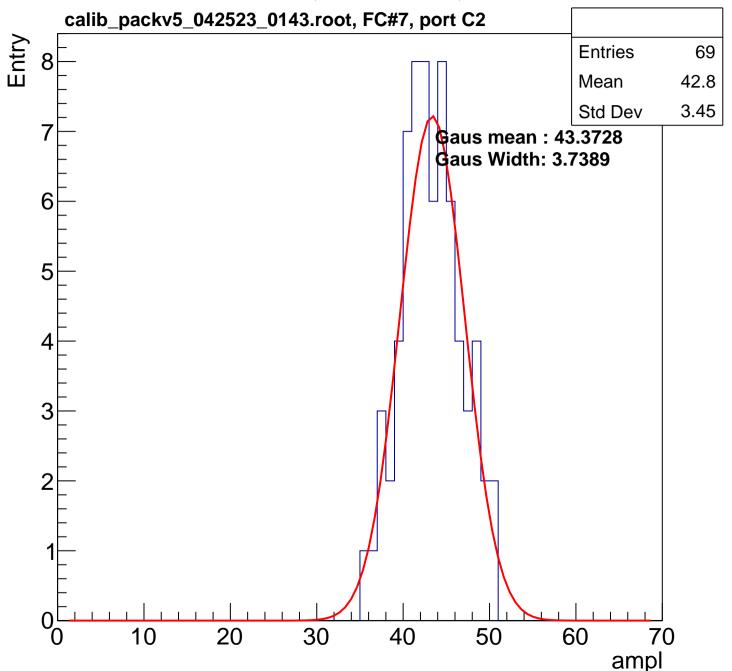


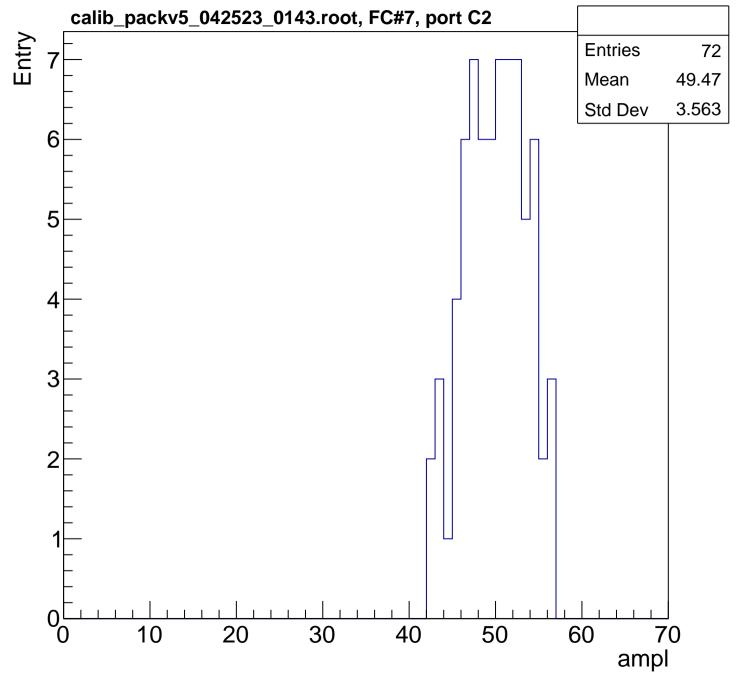


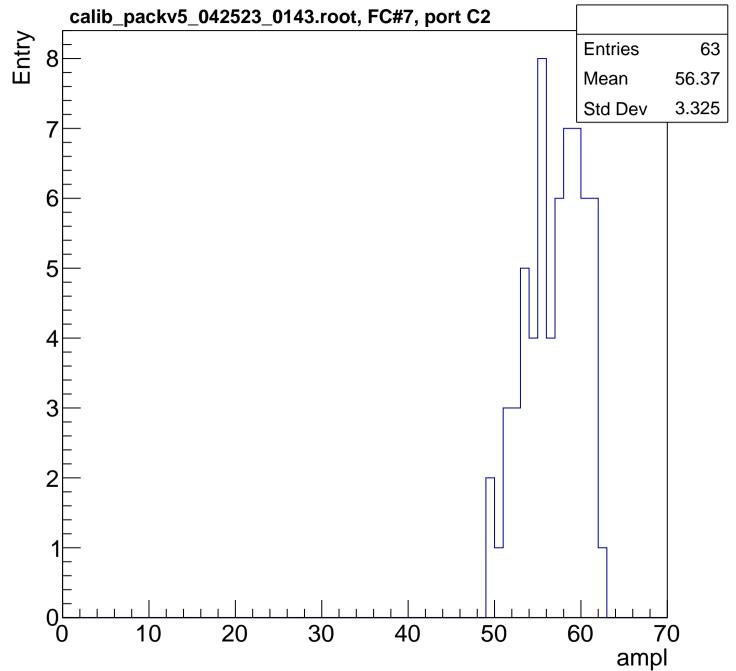


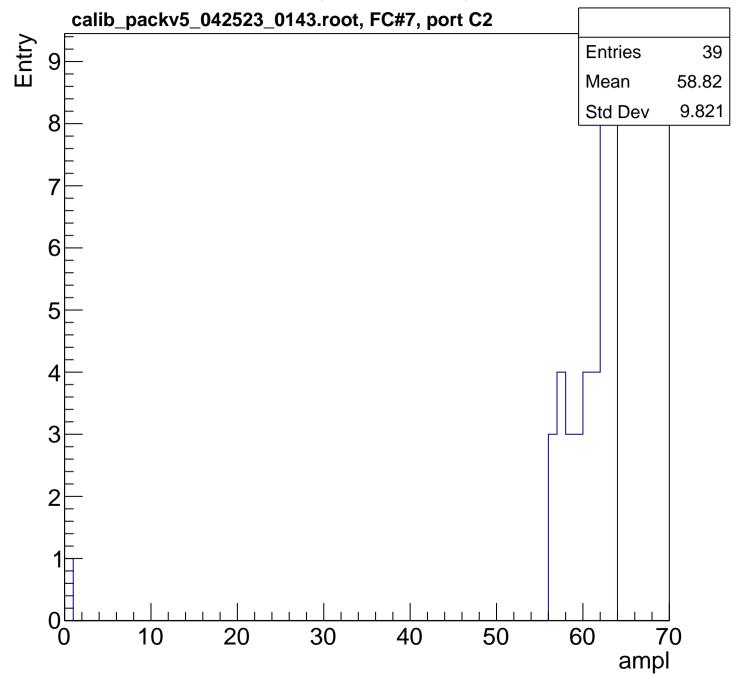


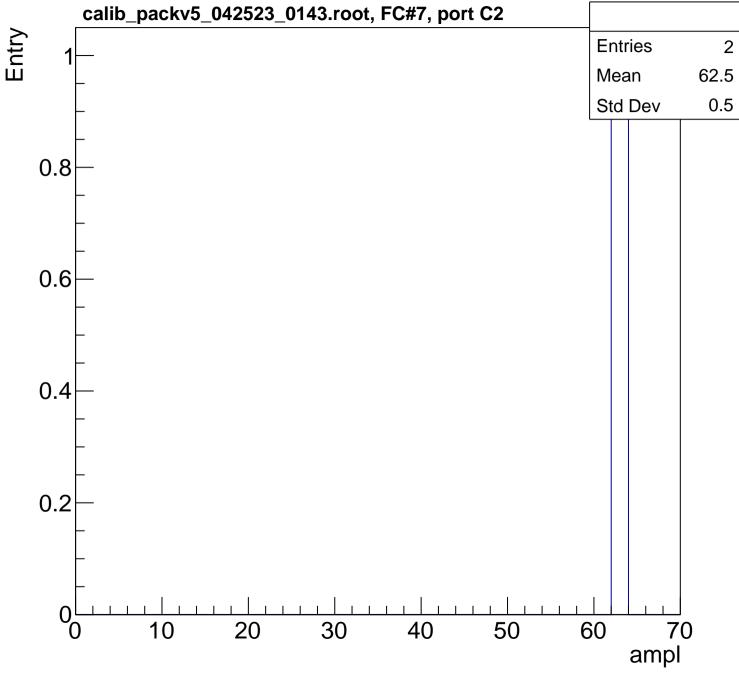




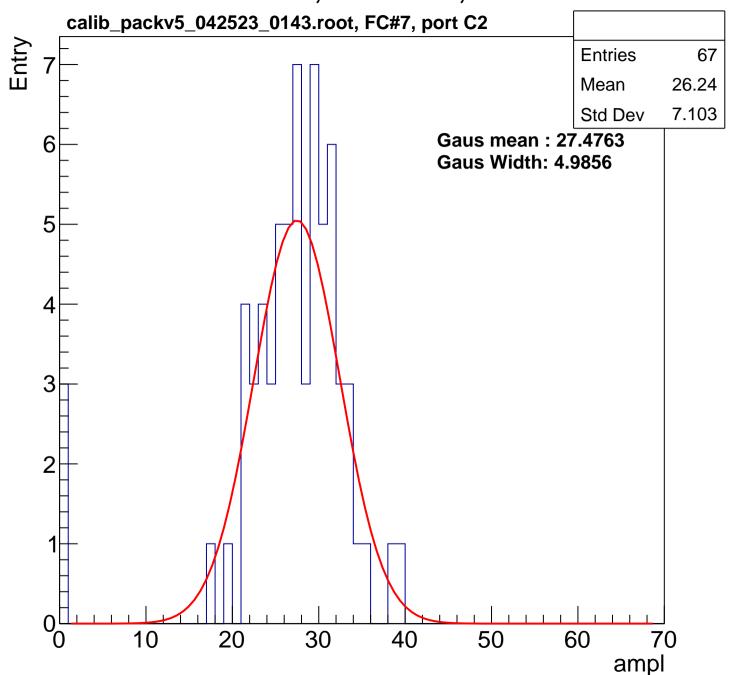


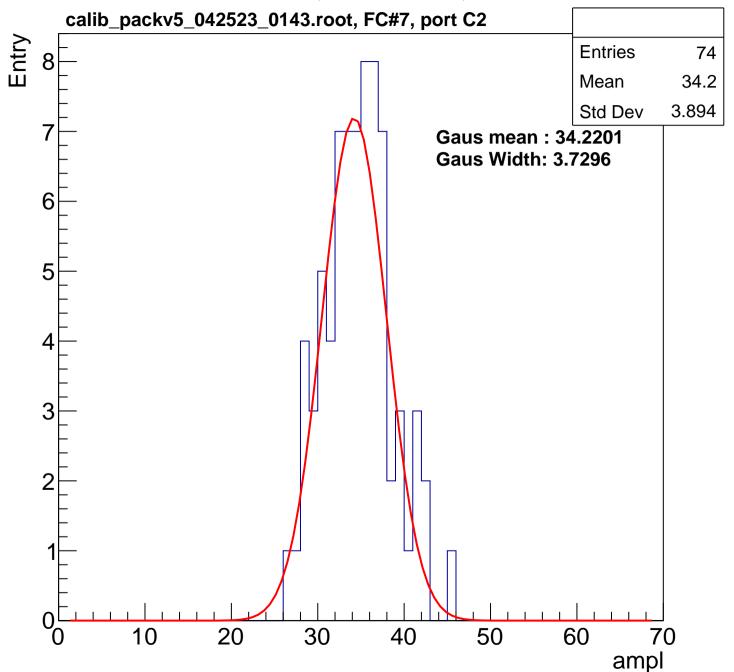


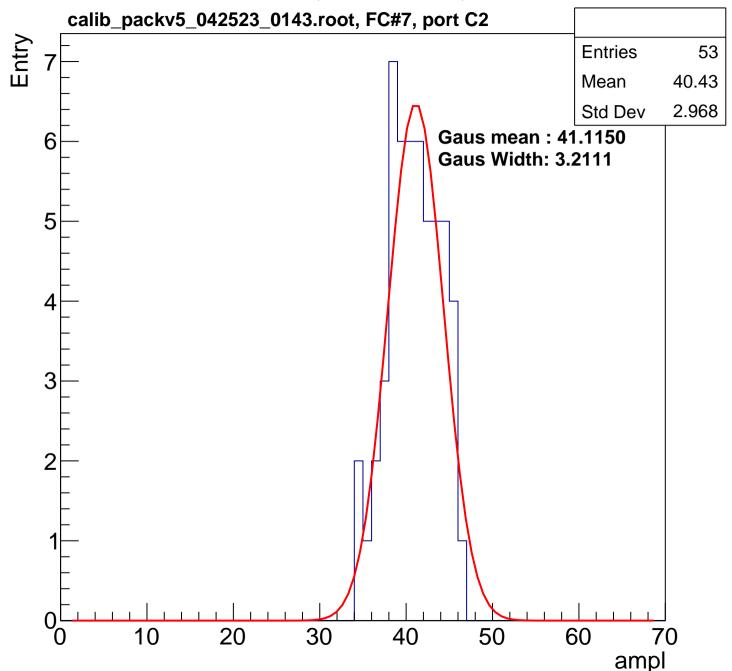


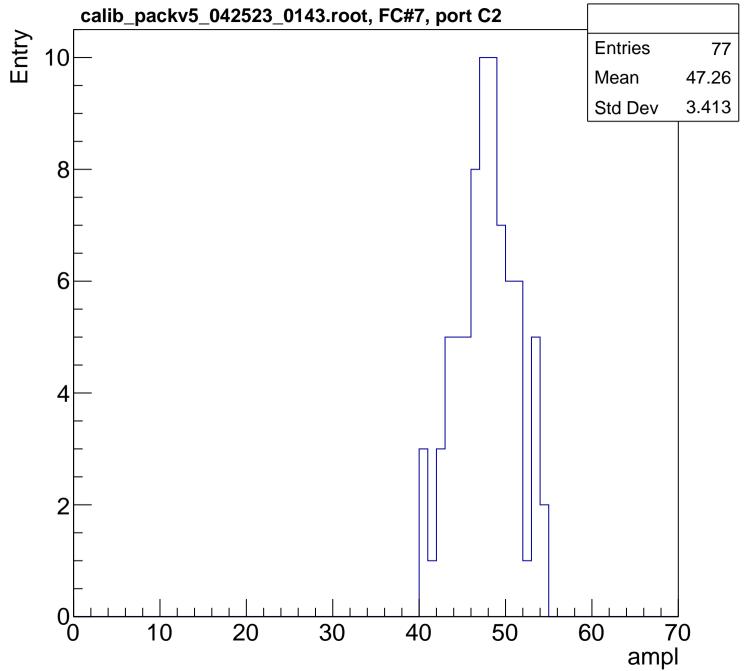


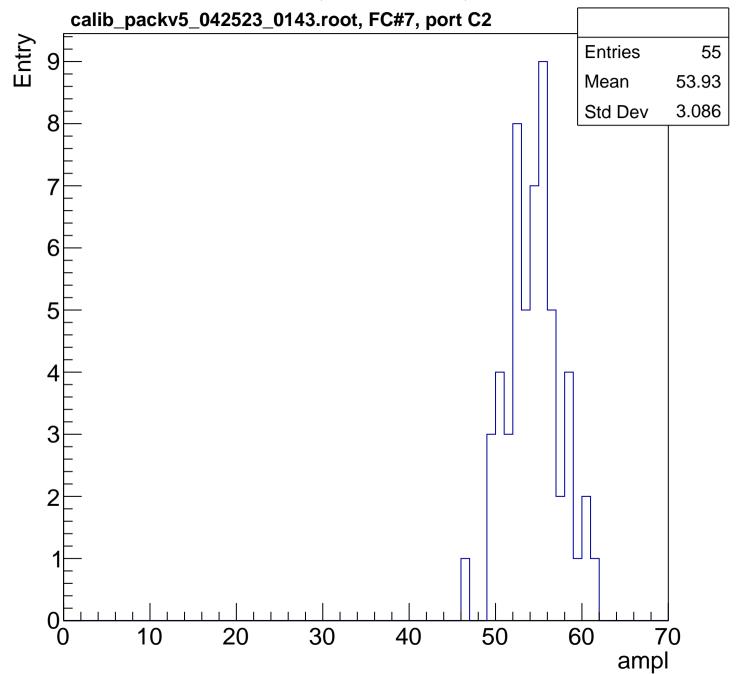
B1L103S, U4-ch37, adc7 calib_packv5_042523_0143.root, FC#7, port C2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

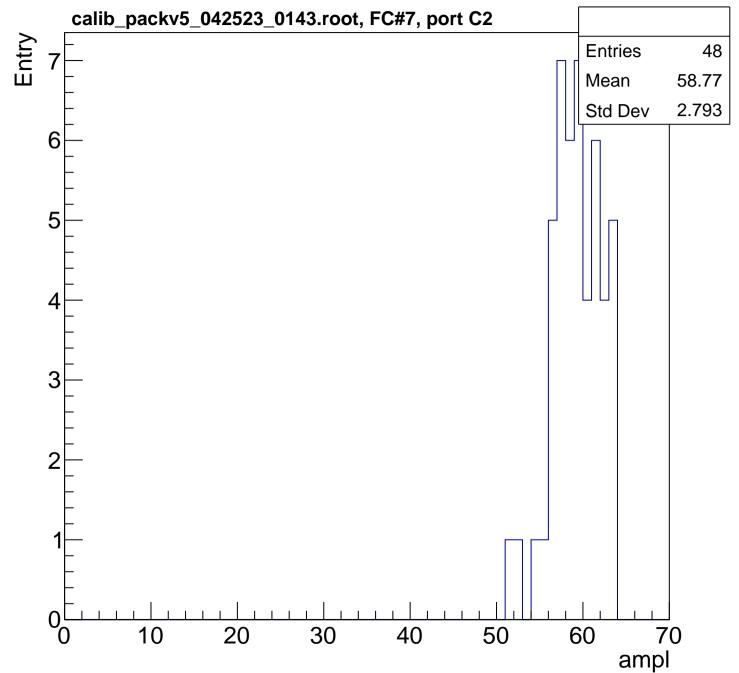


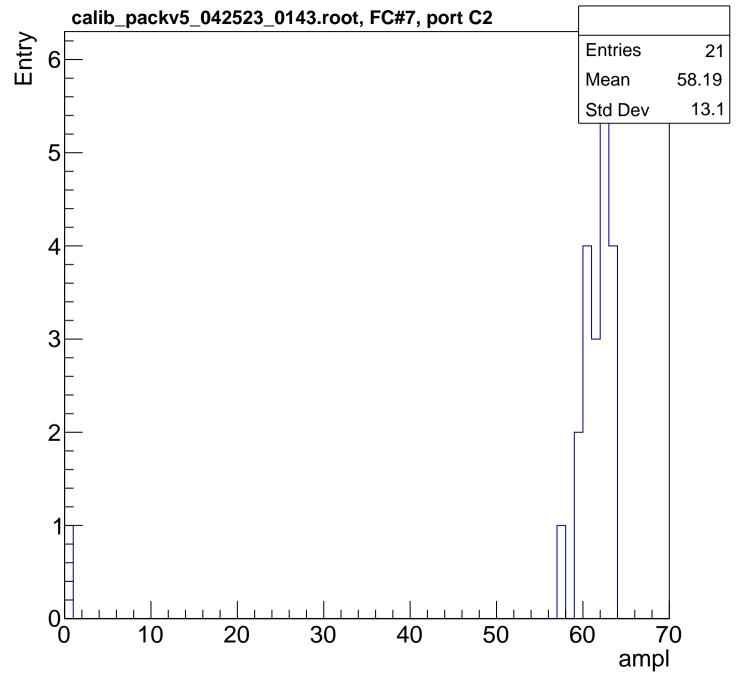


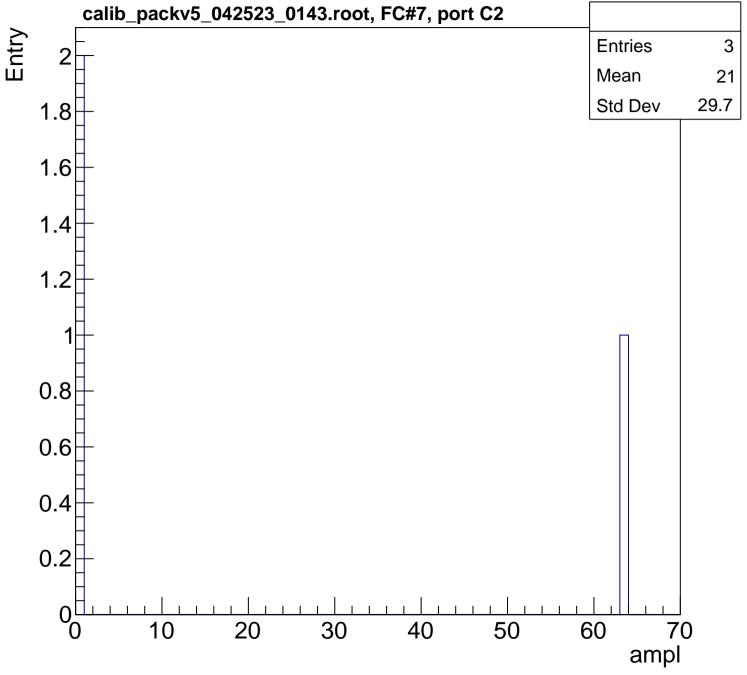


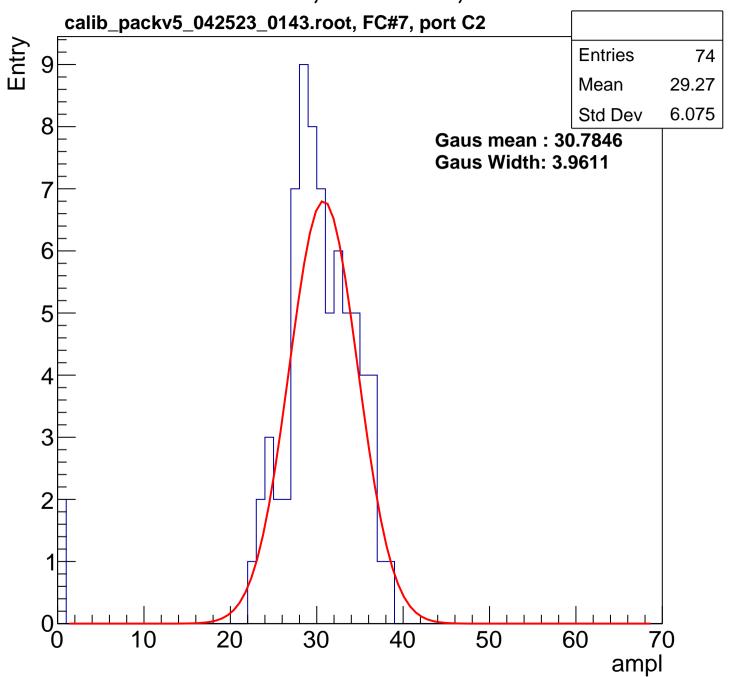


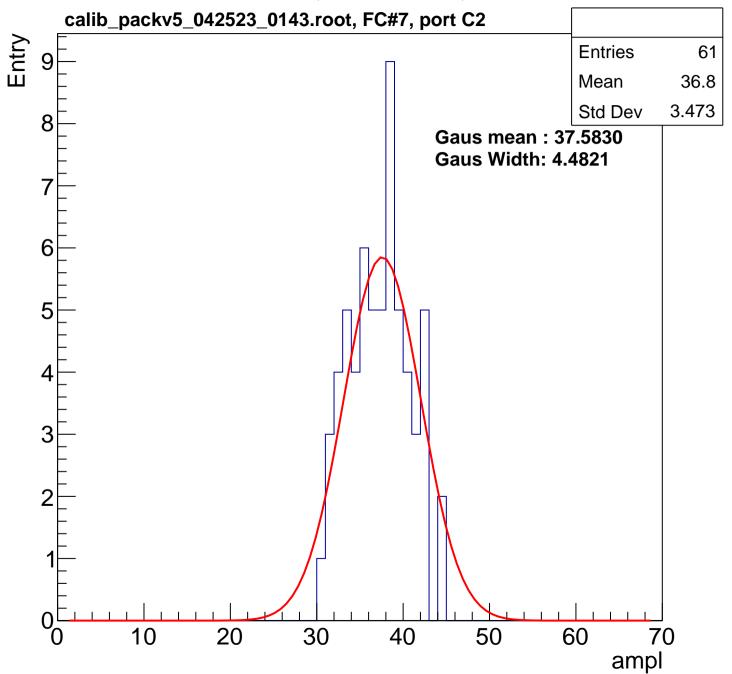


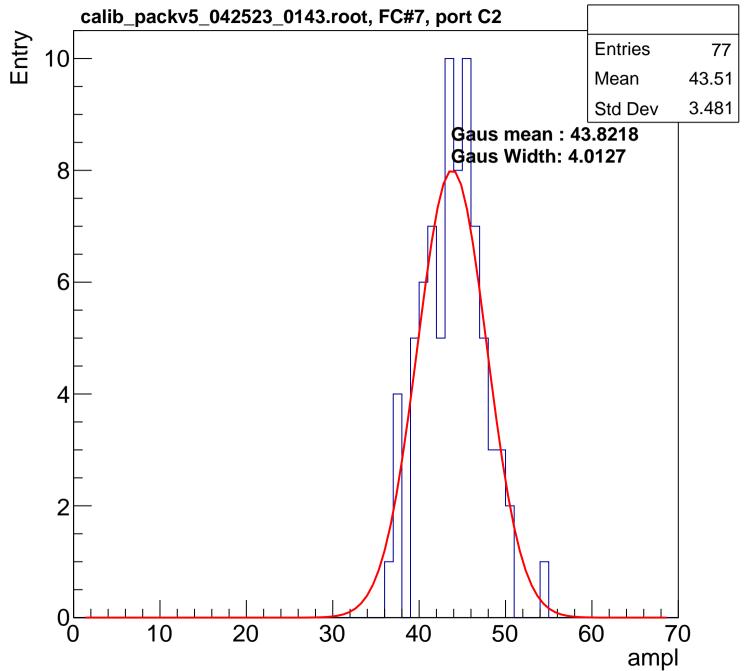


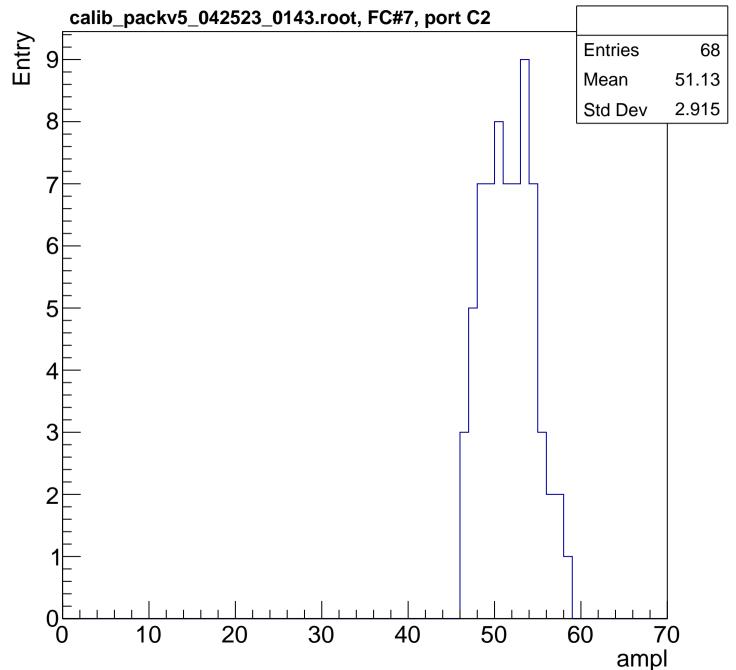


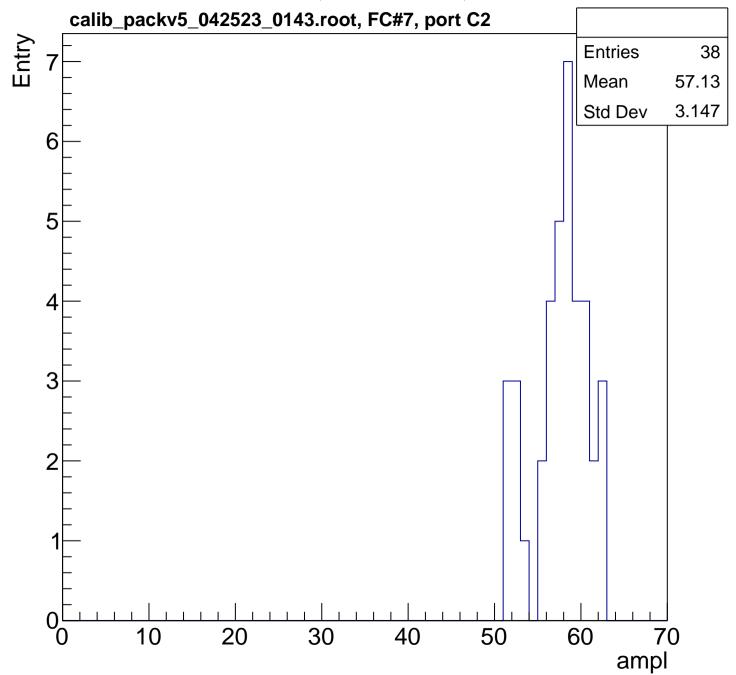


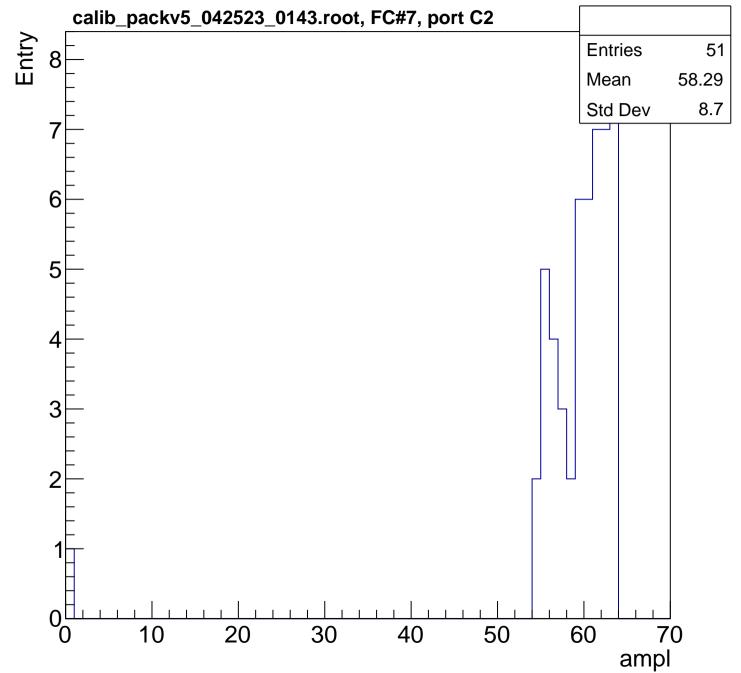


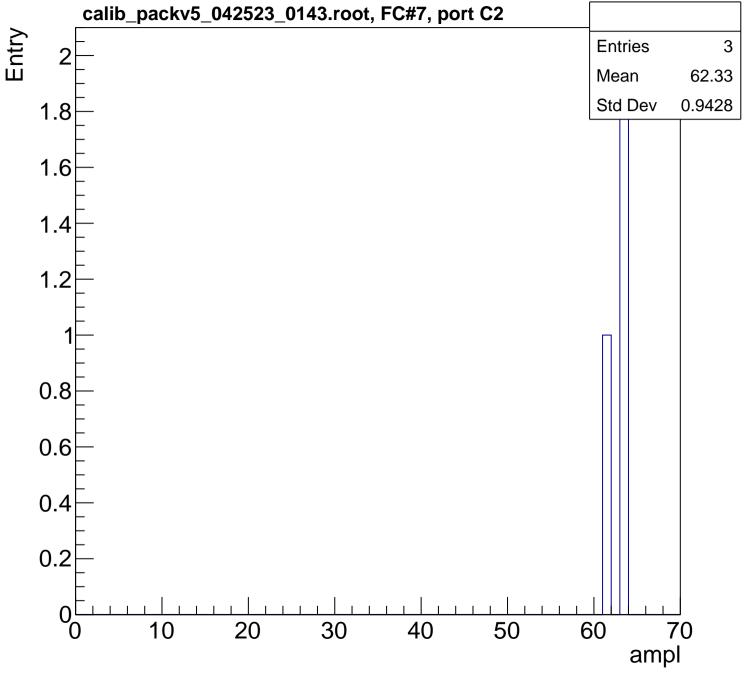




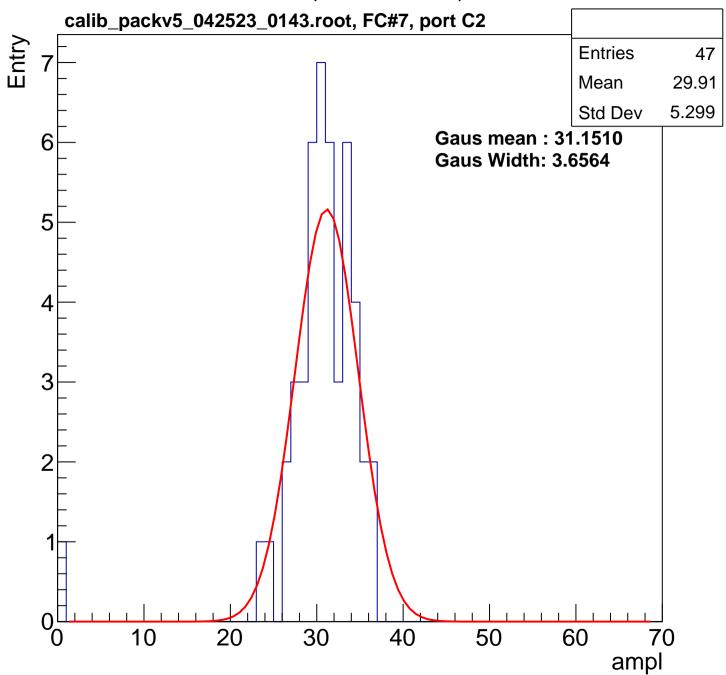


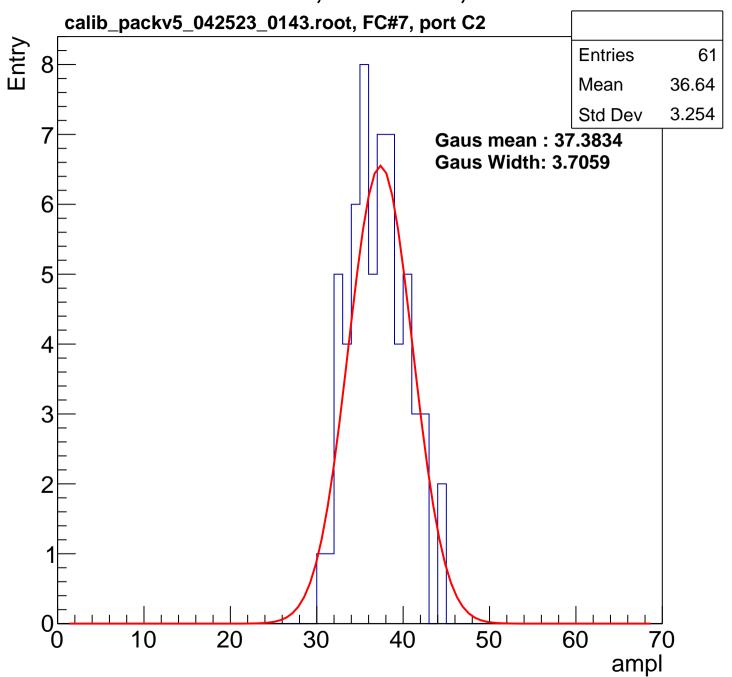


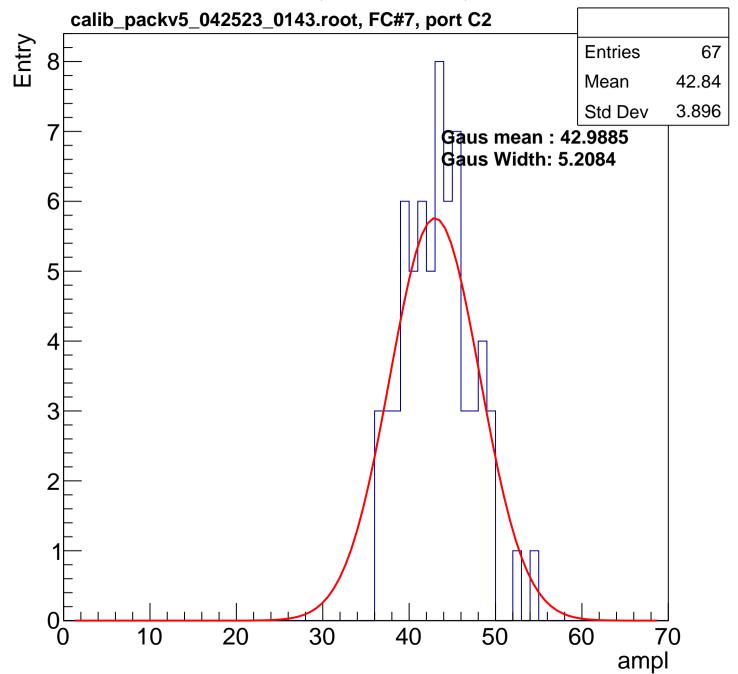


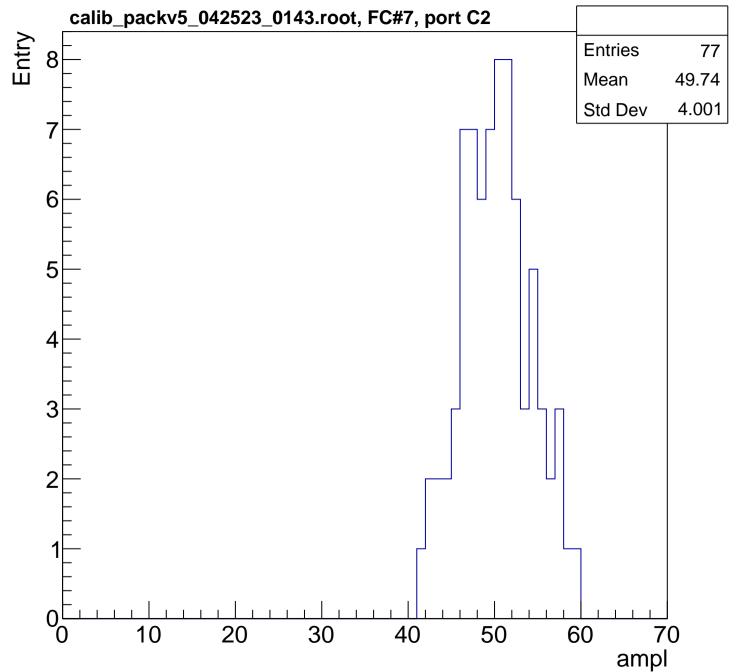


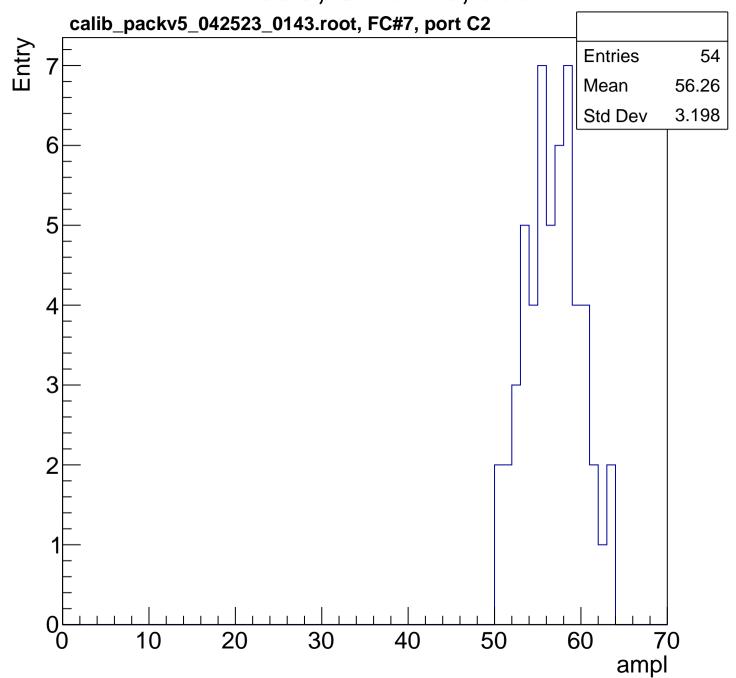


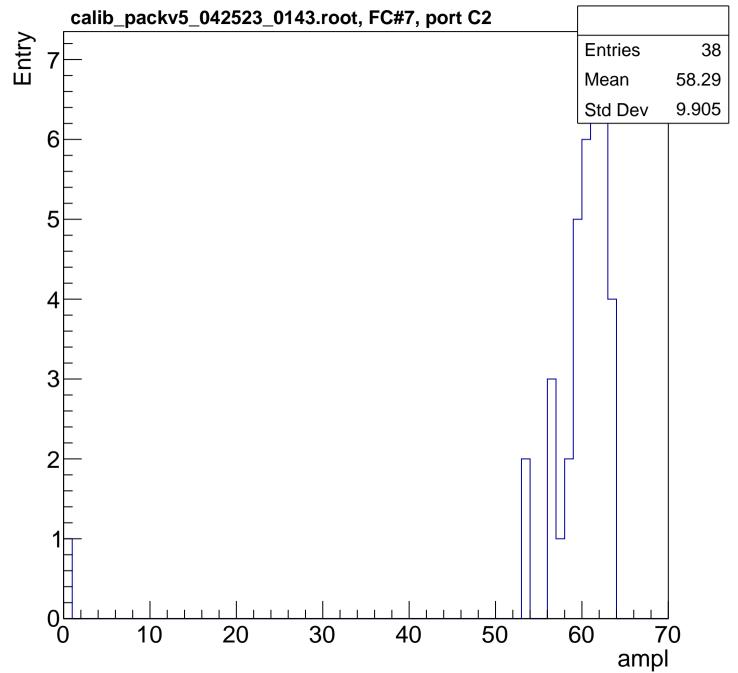


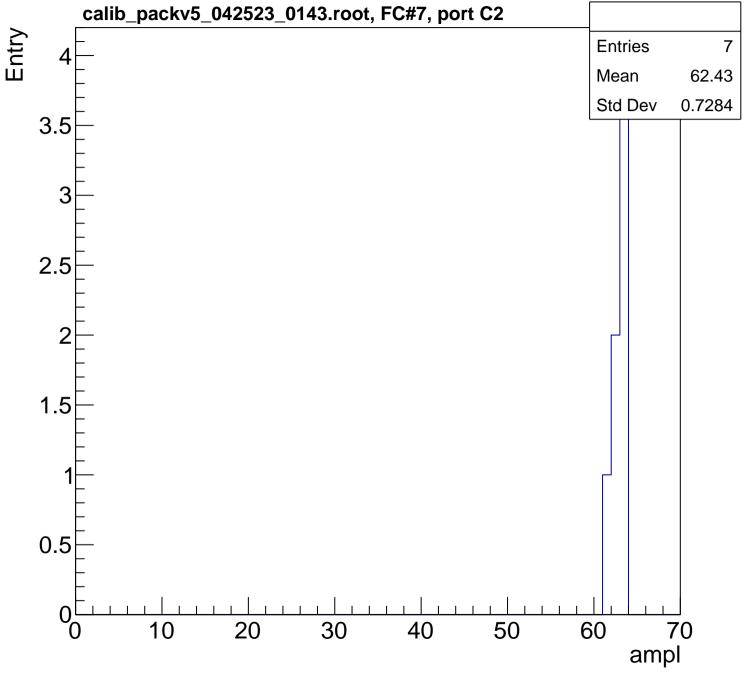


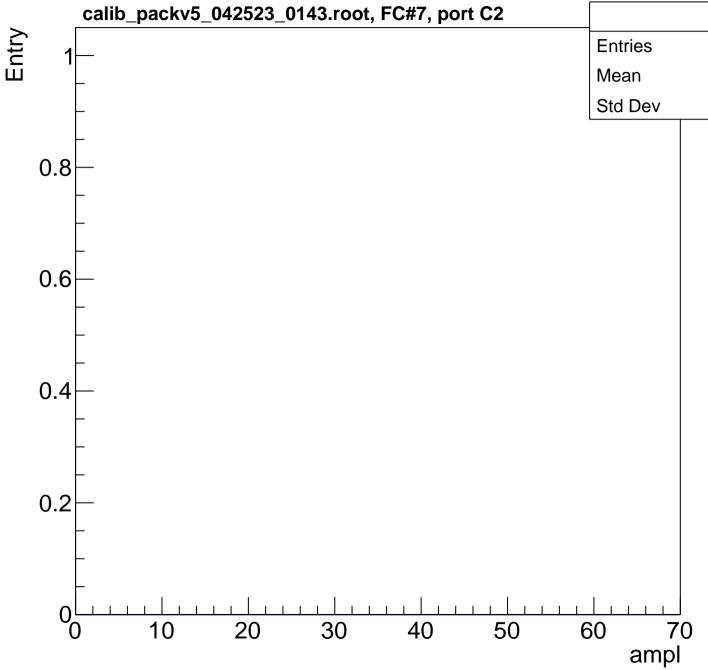


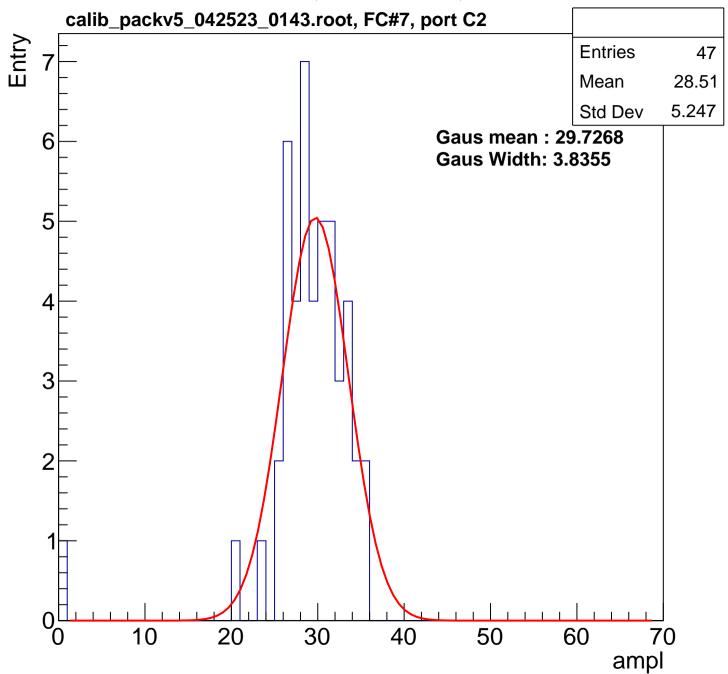


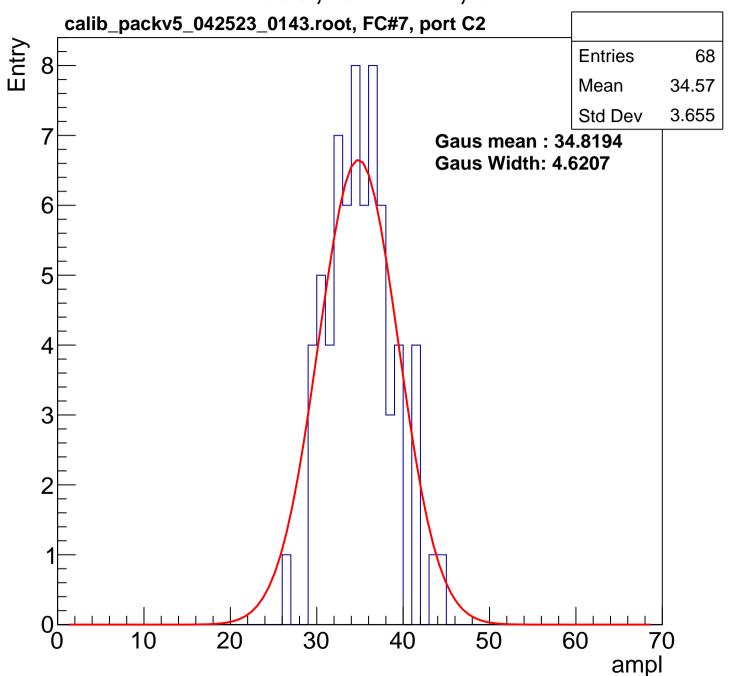


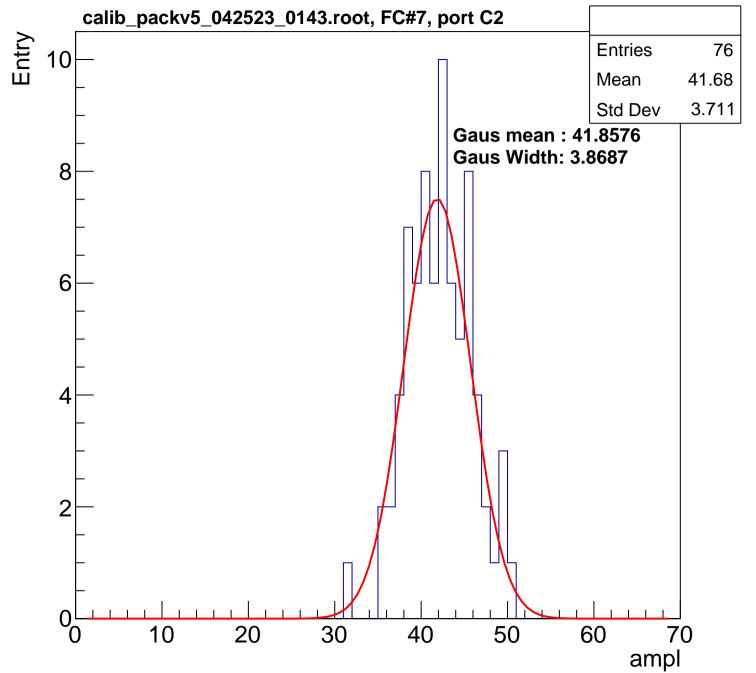


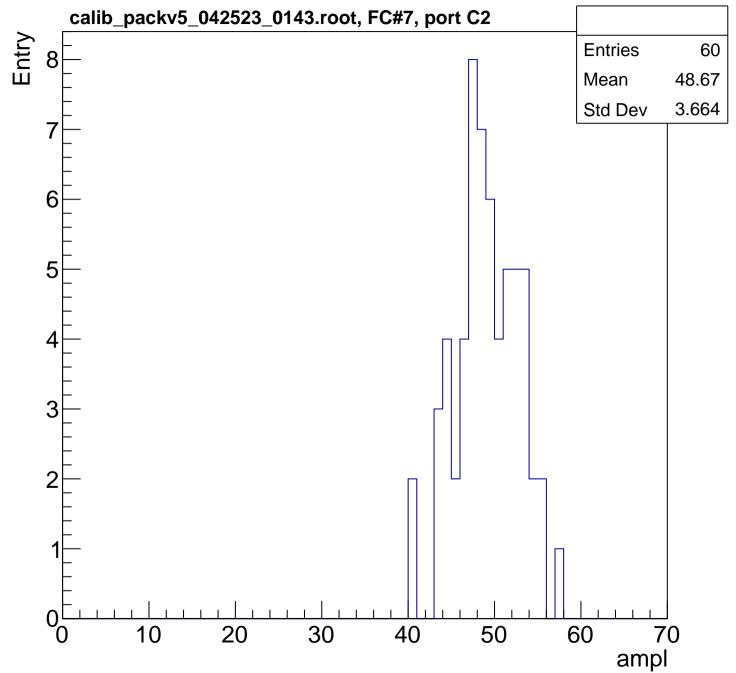


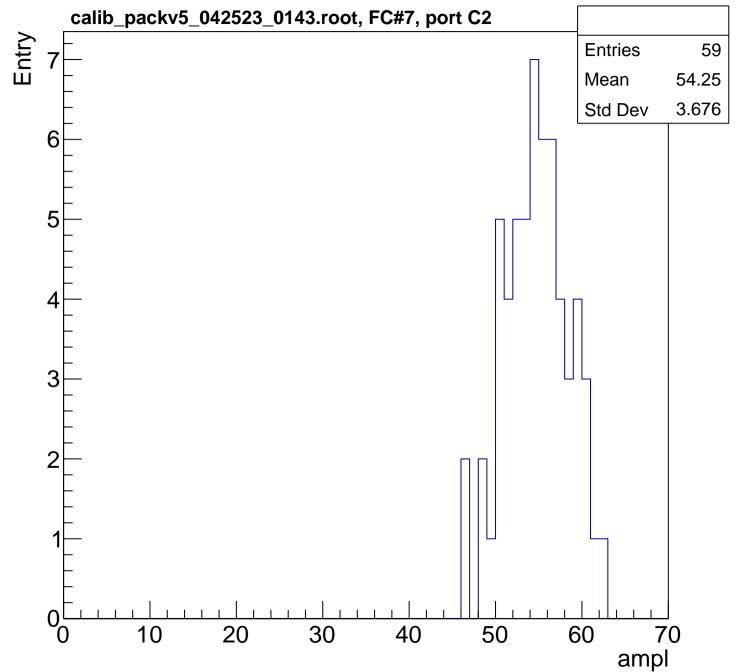


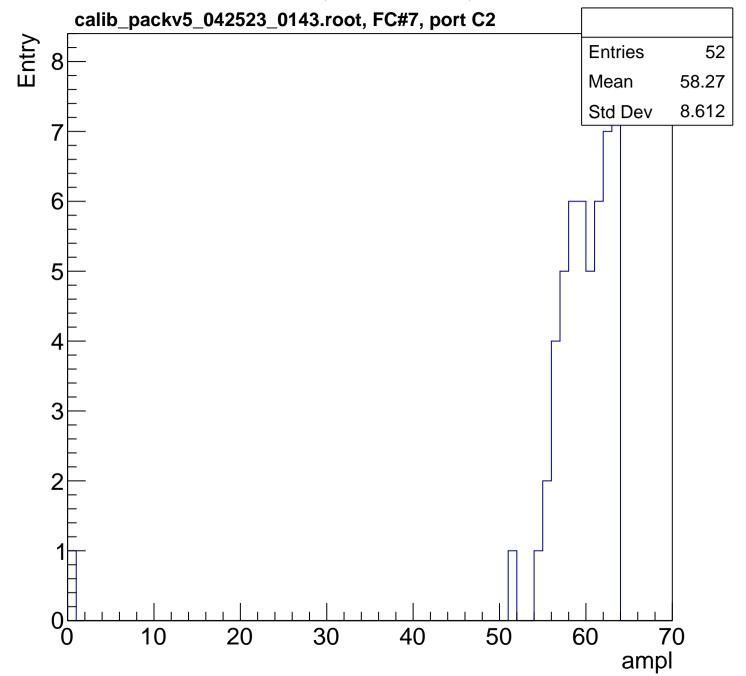


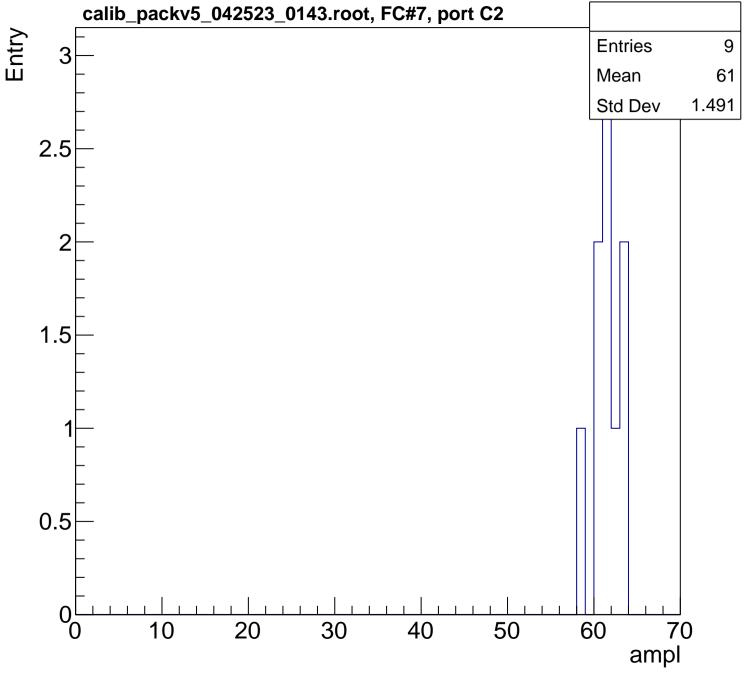


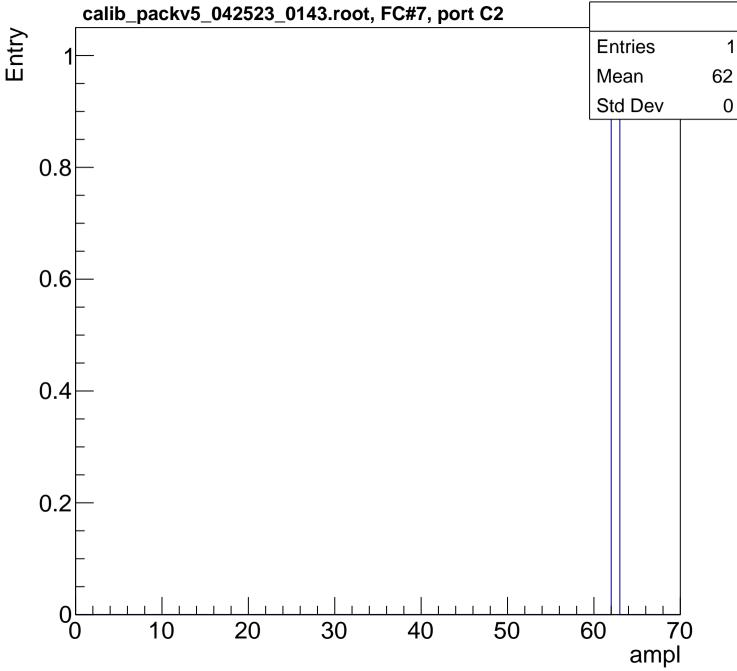


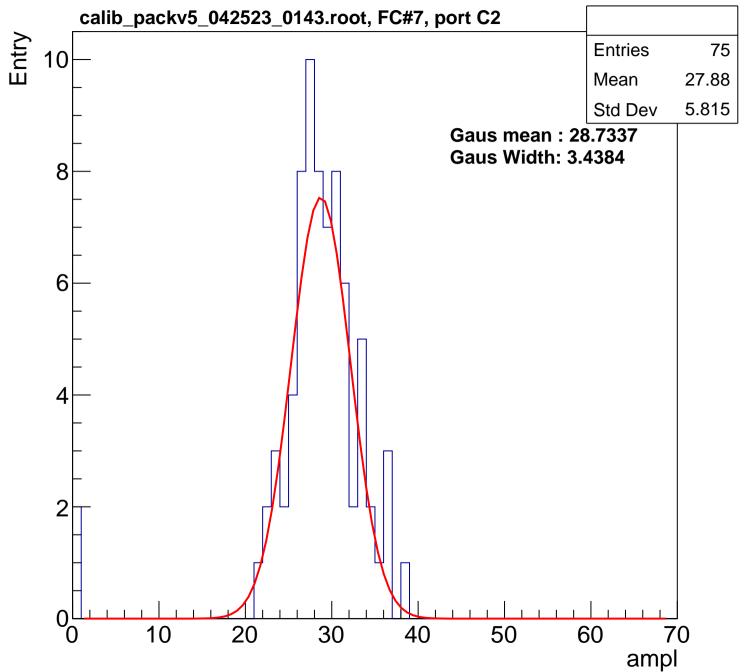


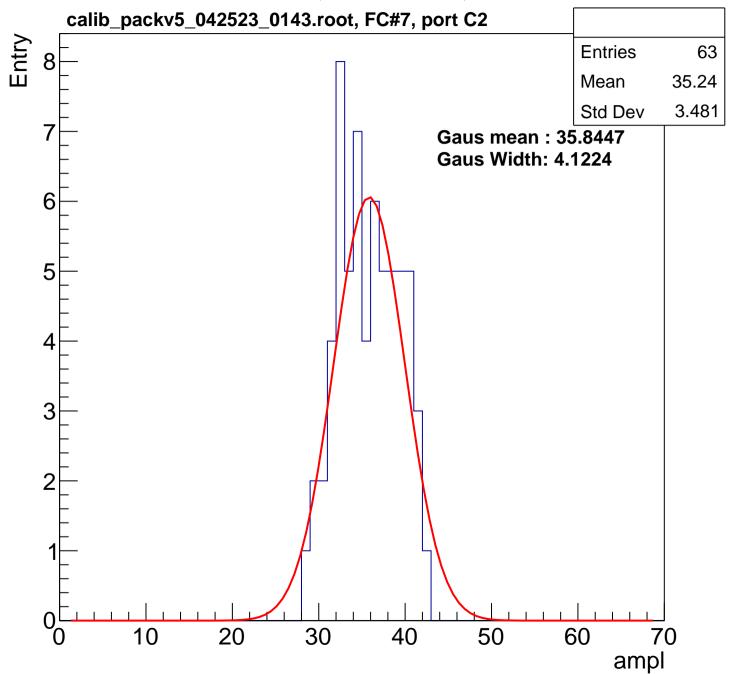


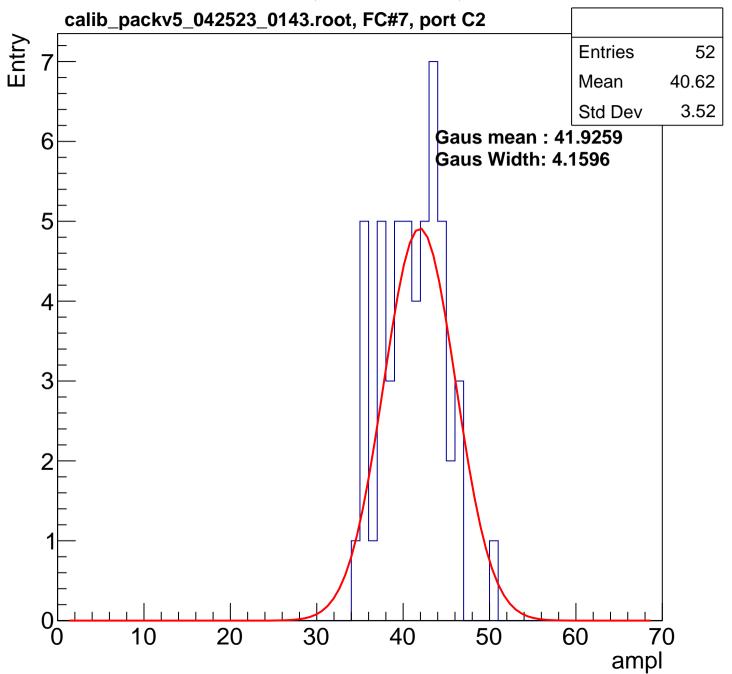


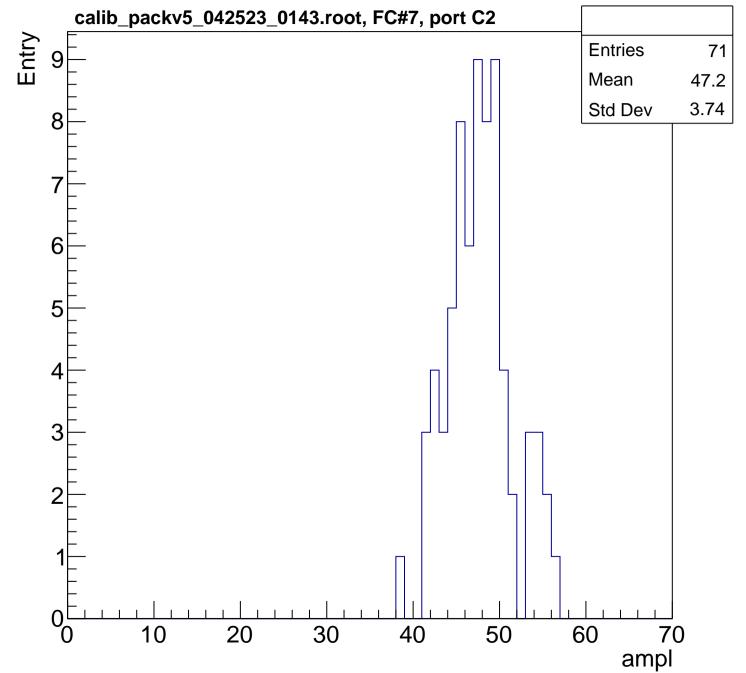


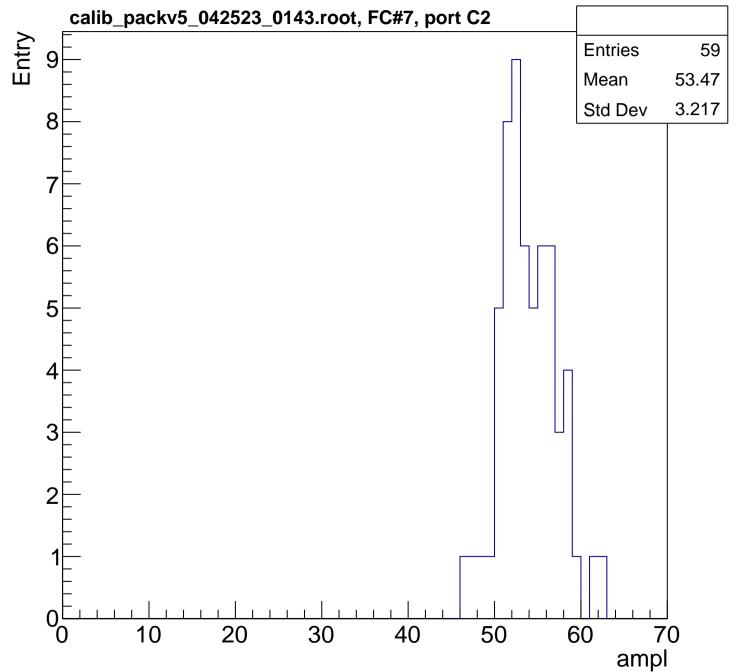


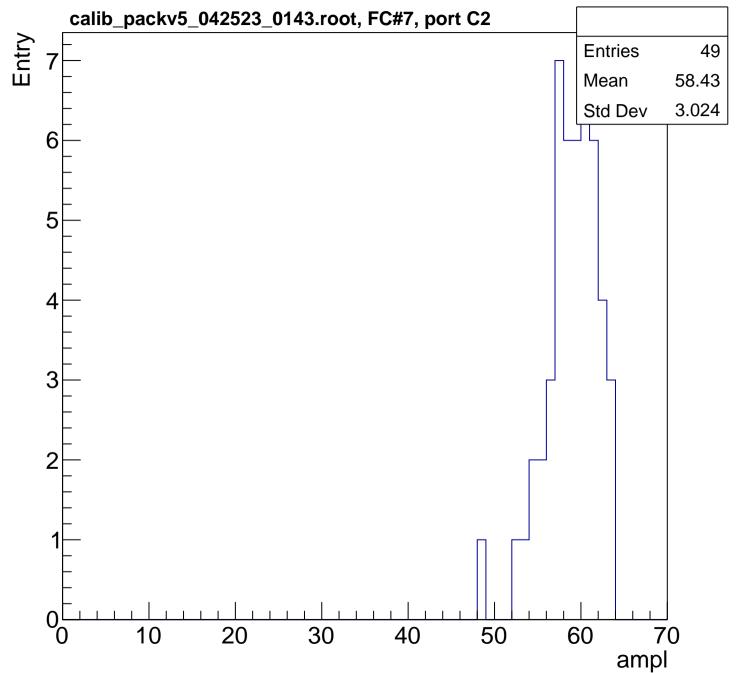


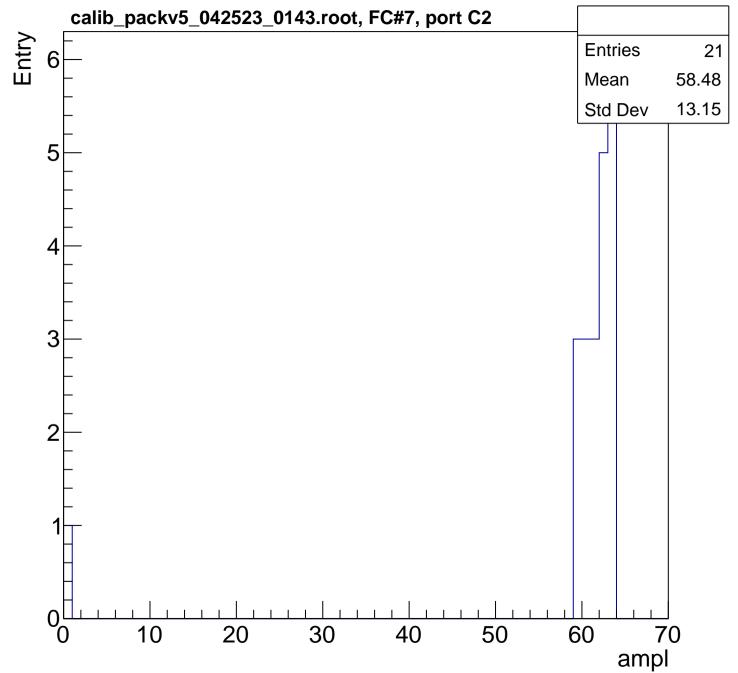


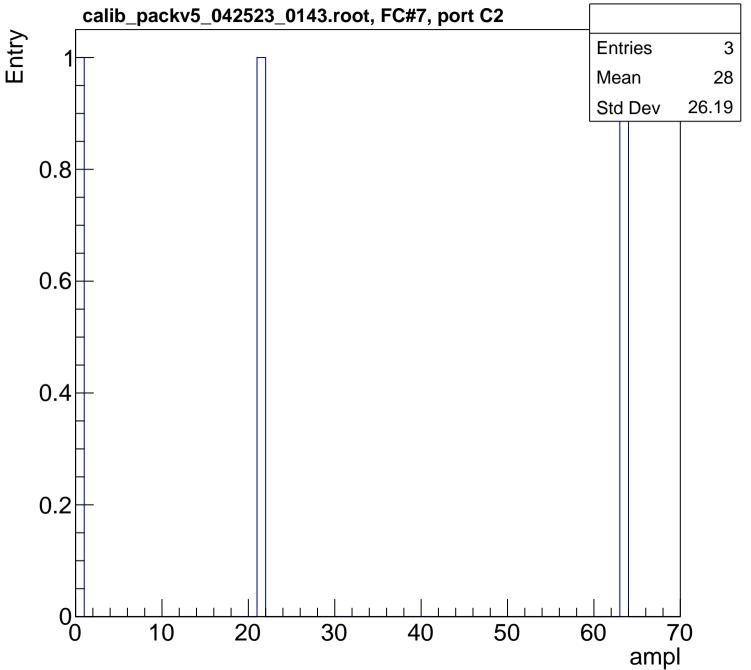


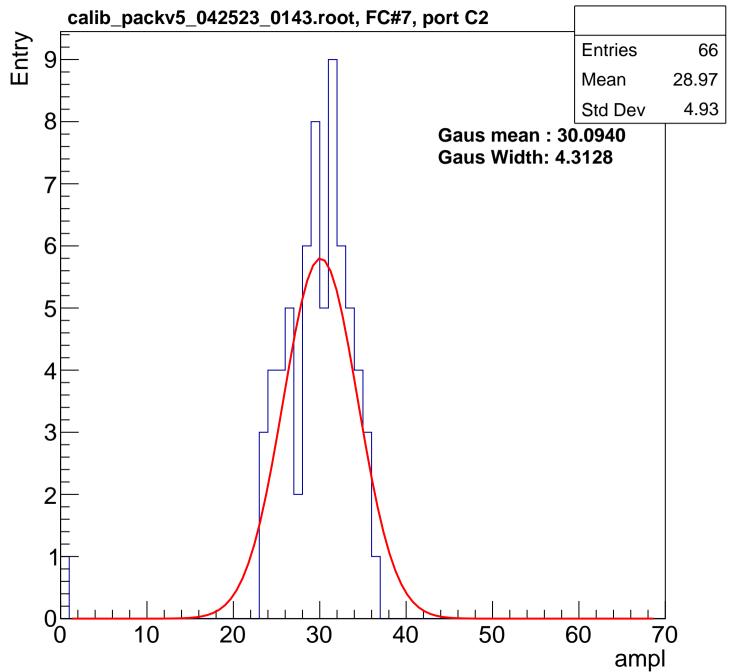


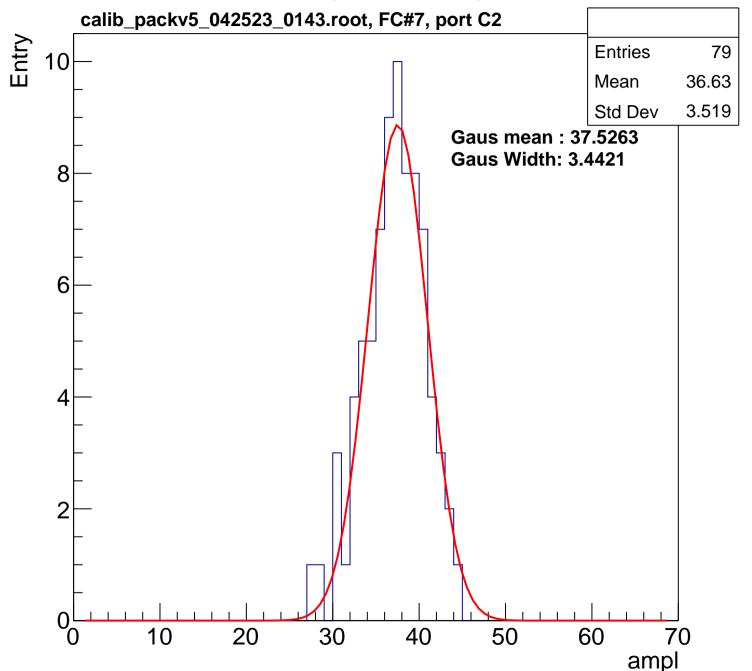


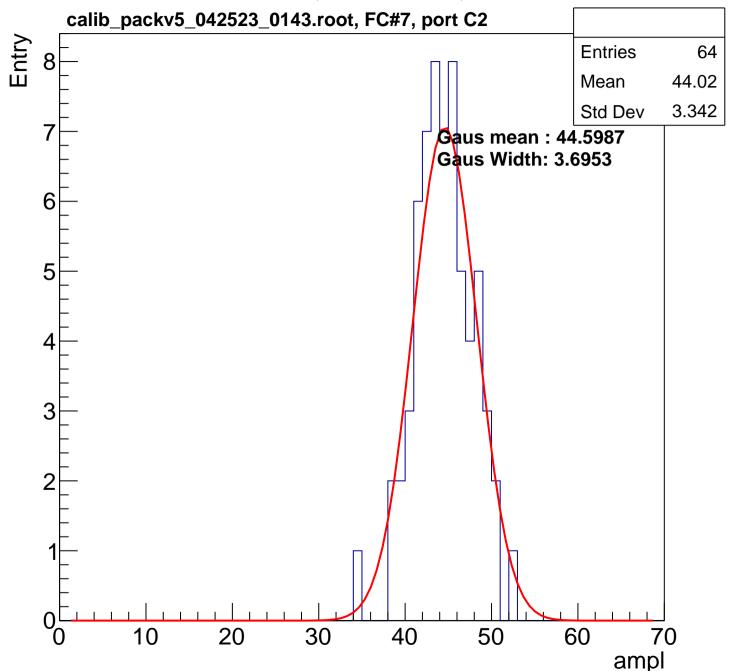


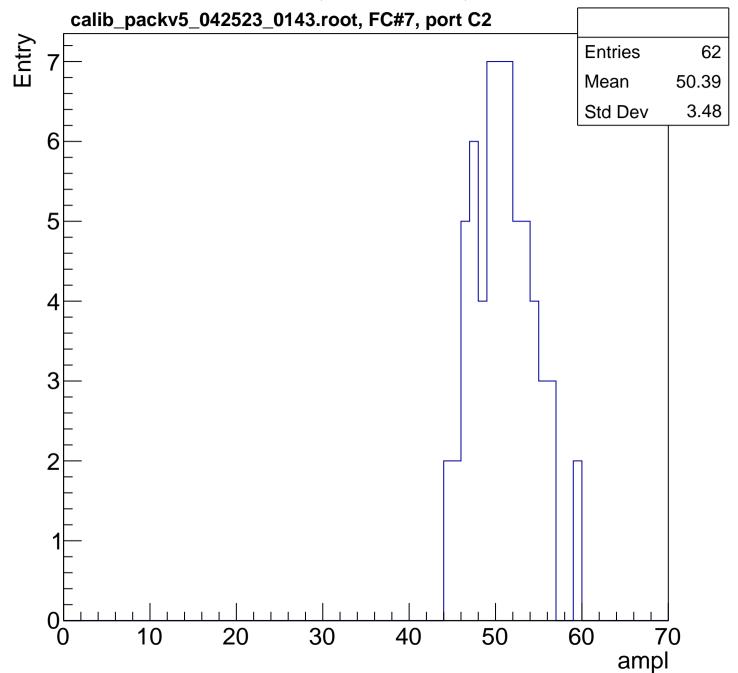


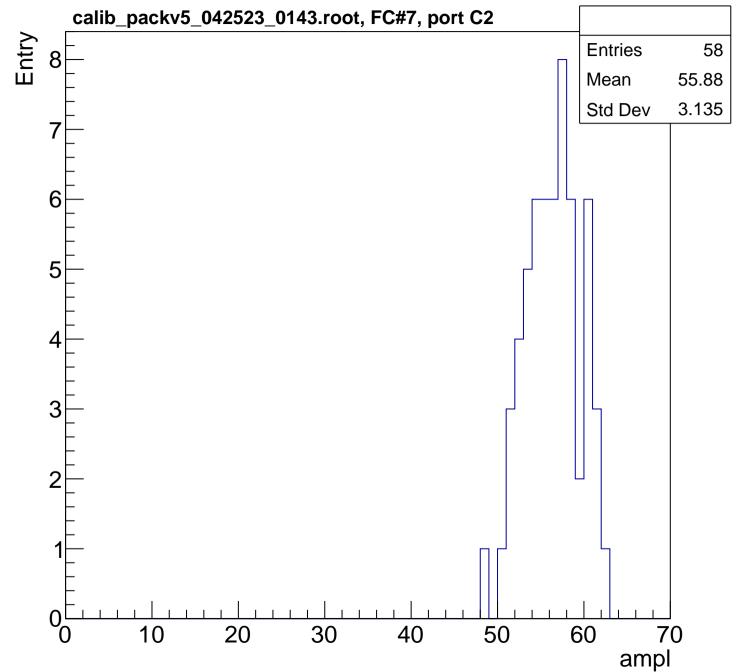


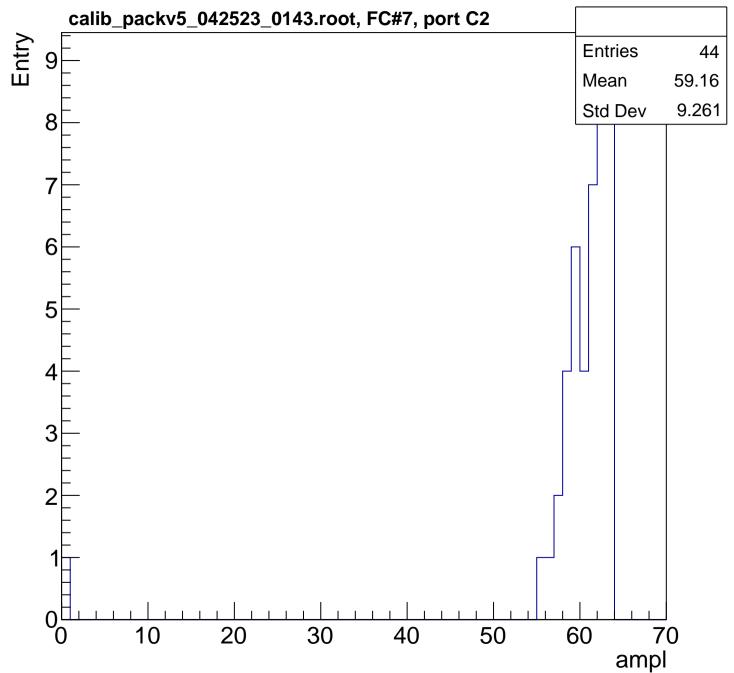


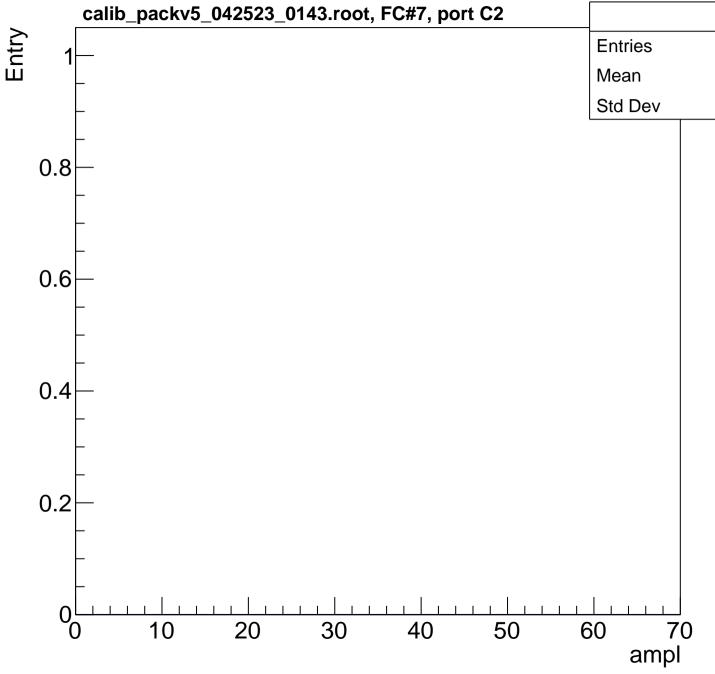


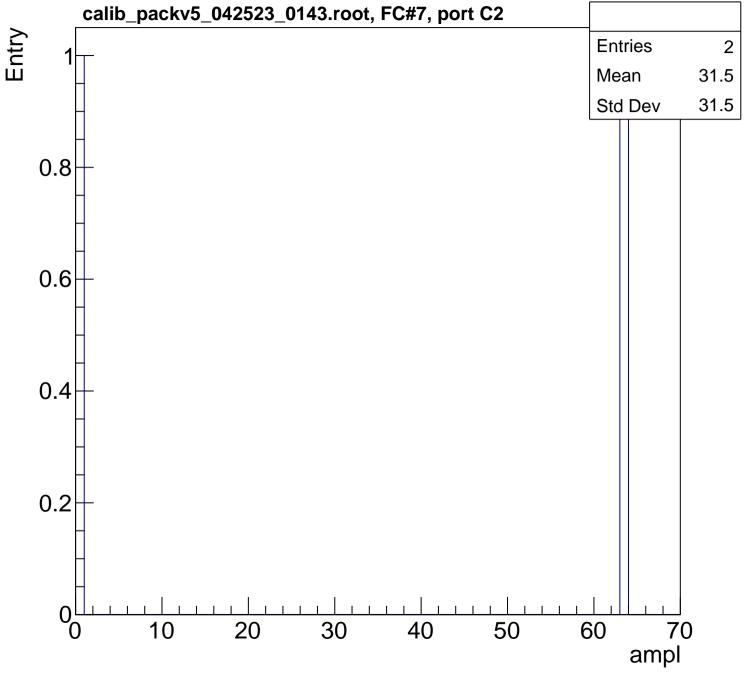


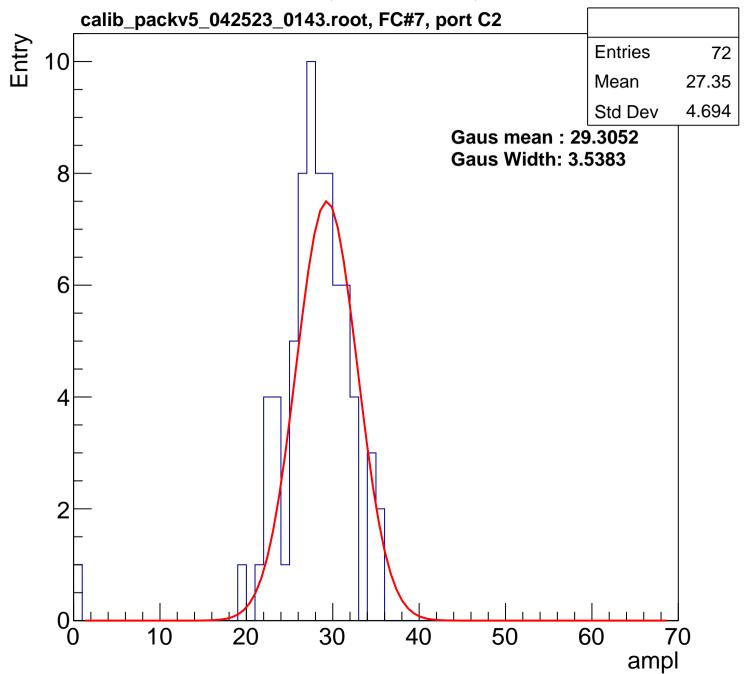


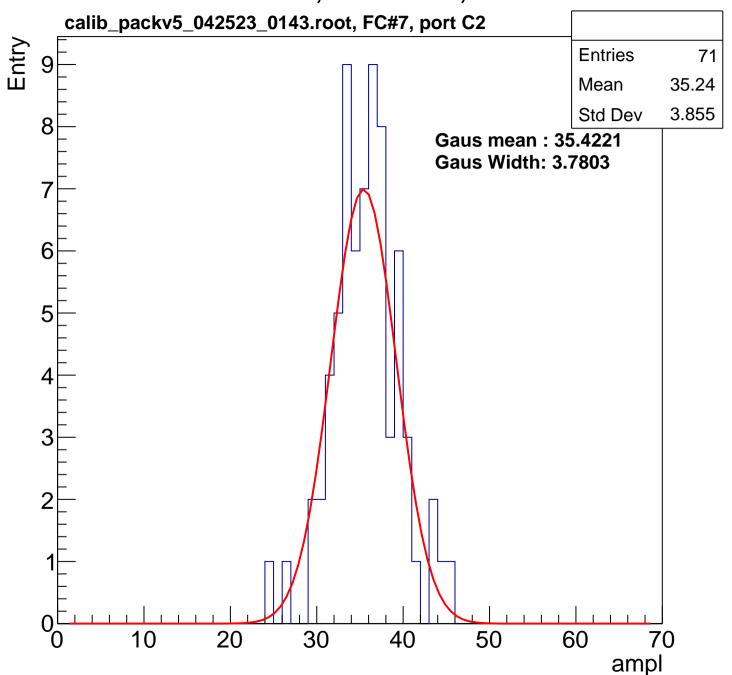


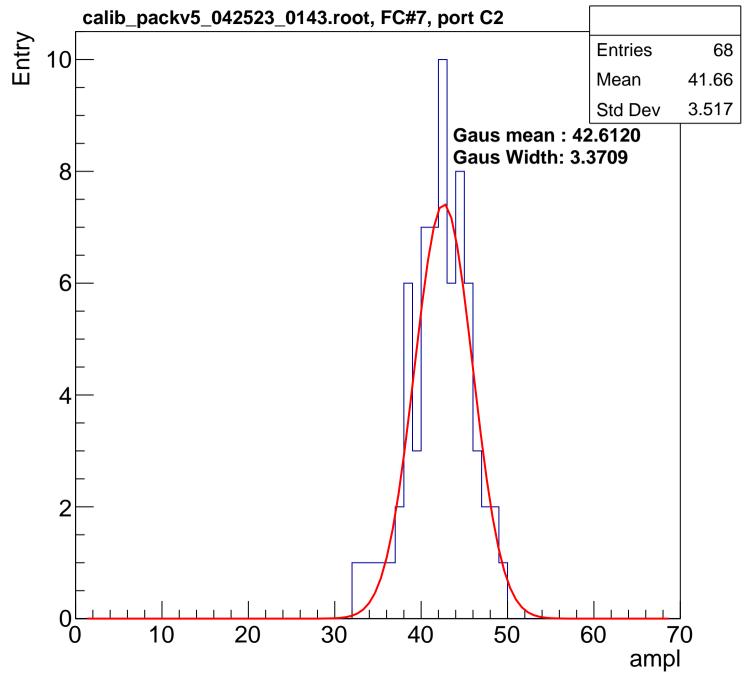


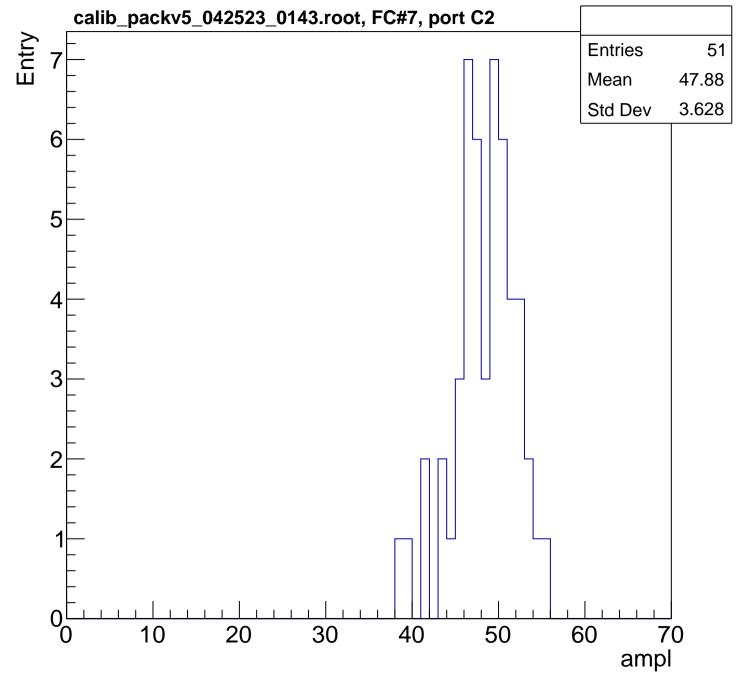


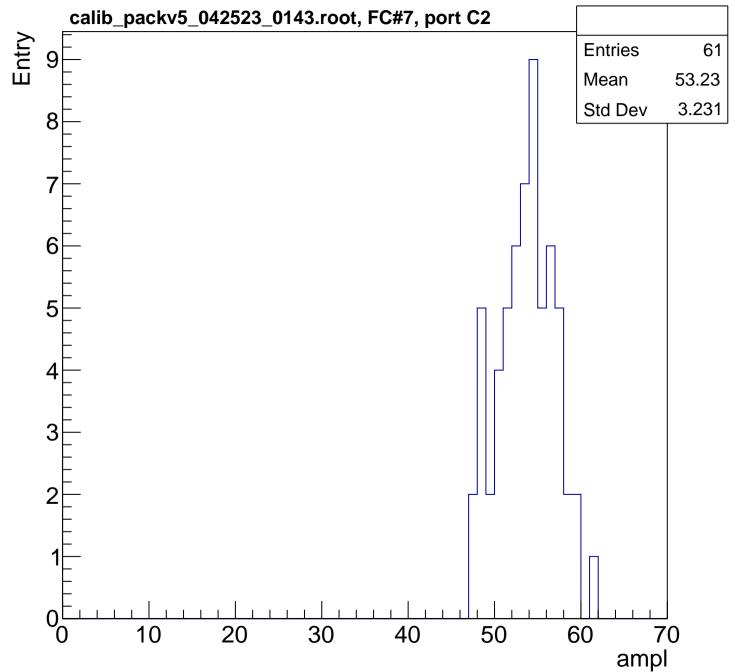


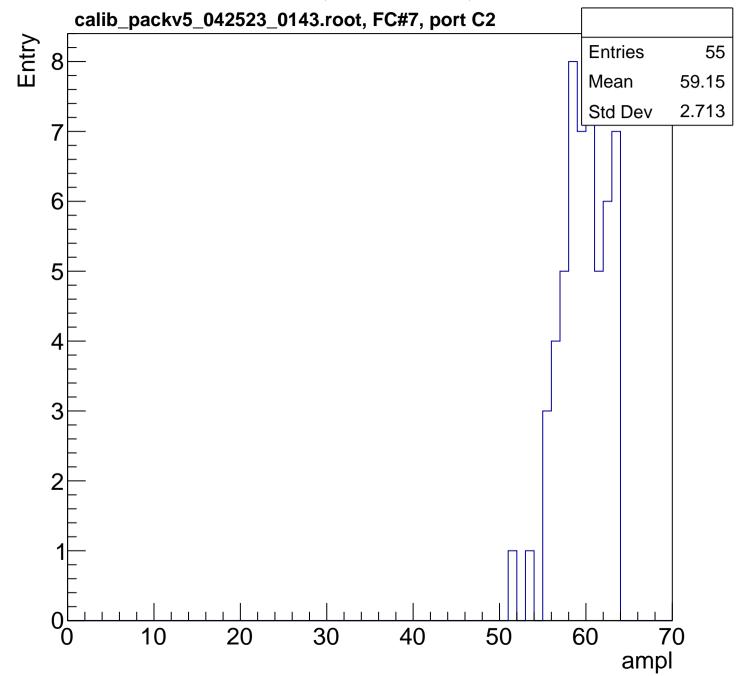


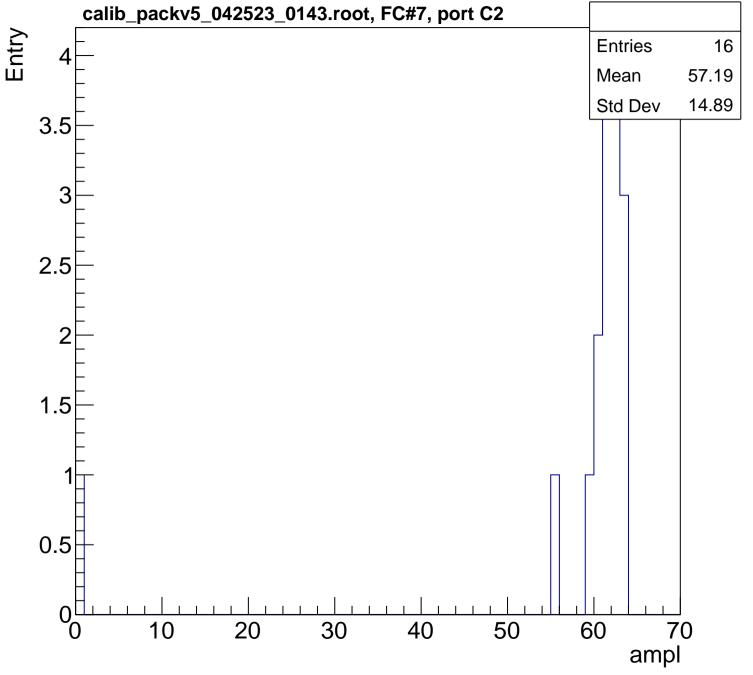




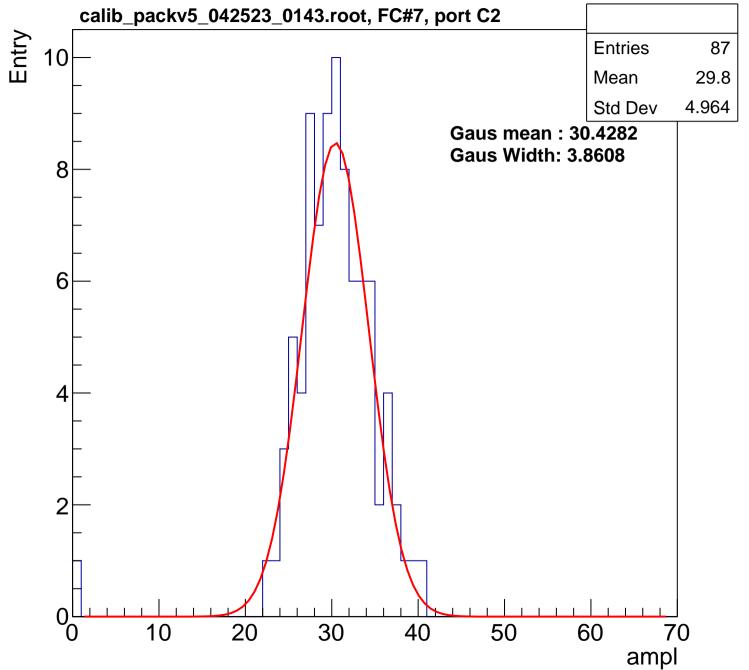


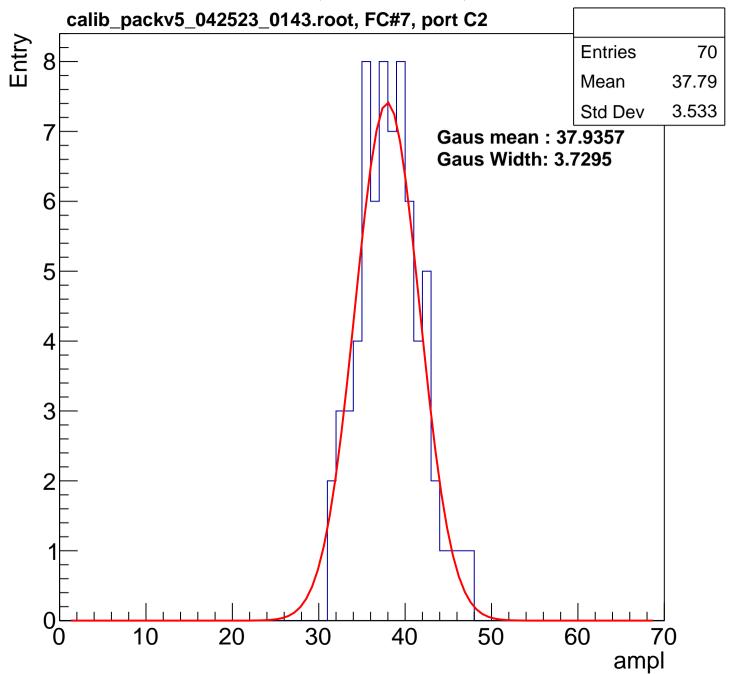


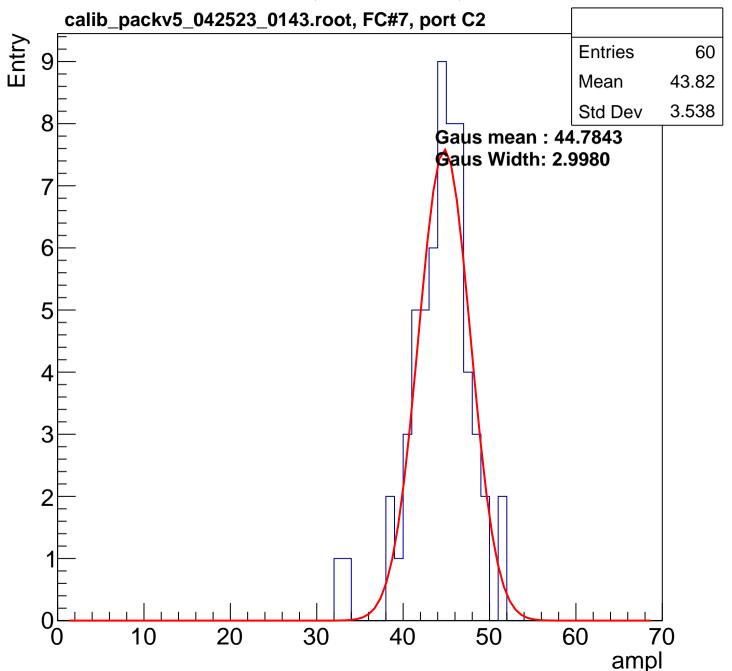


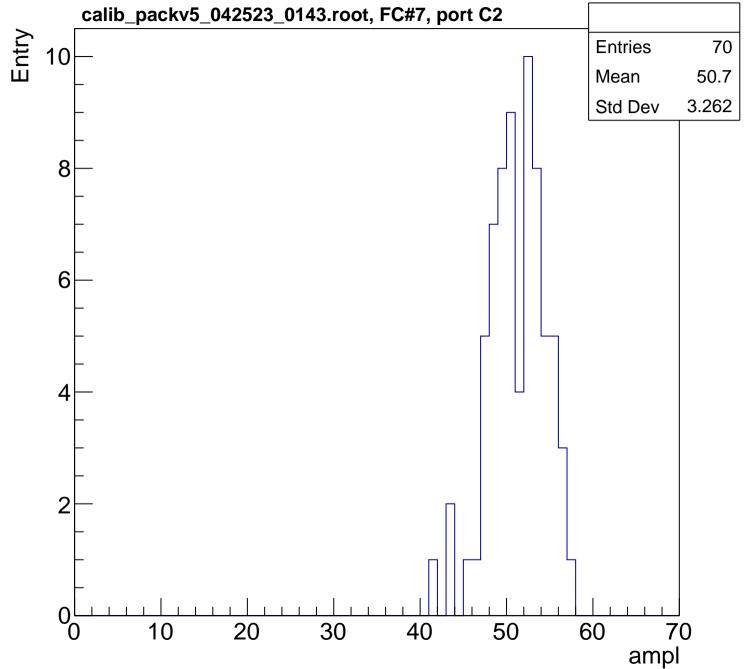


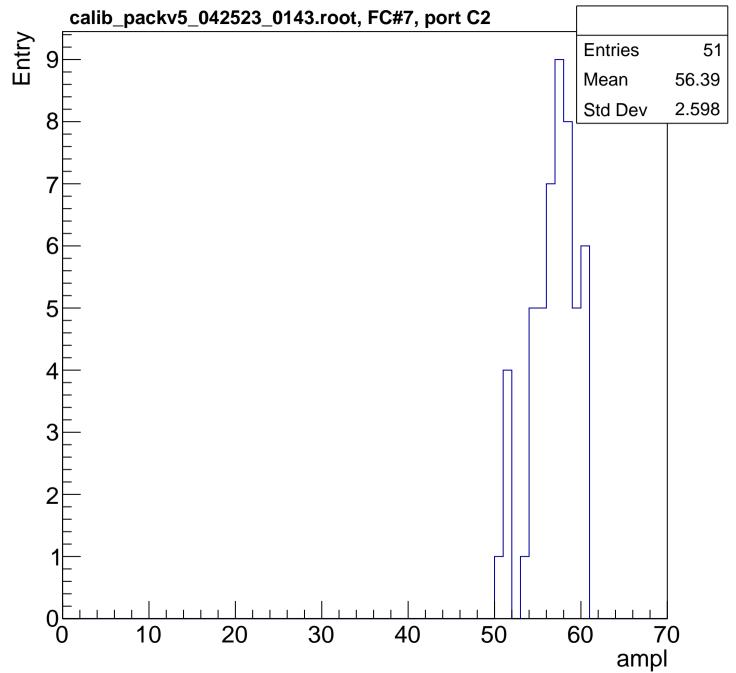
B1L103S, U4-ch44, adc7 calib_packv5_042523_0143.root, FC#7, port C2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

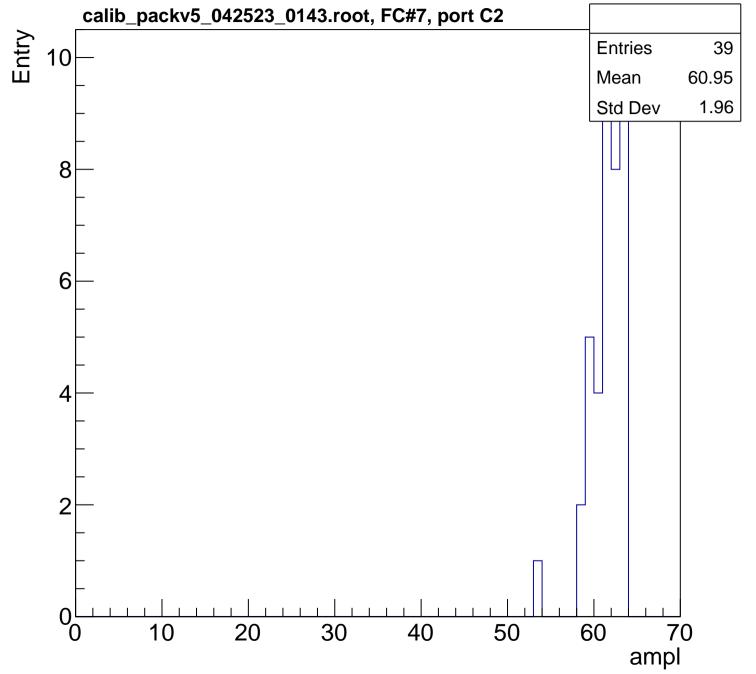


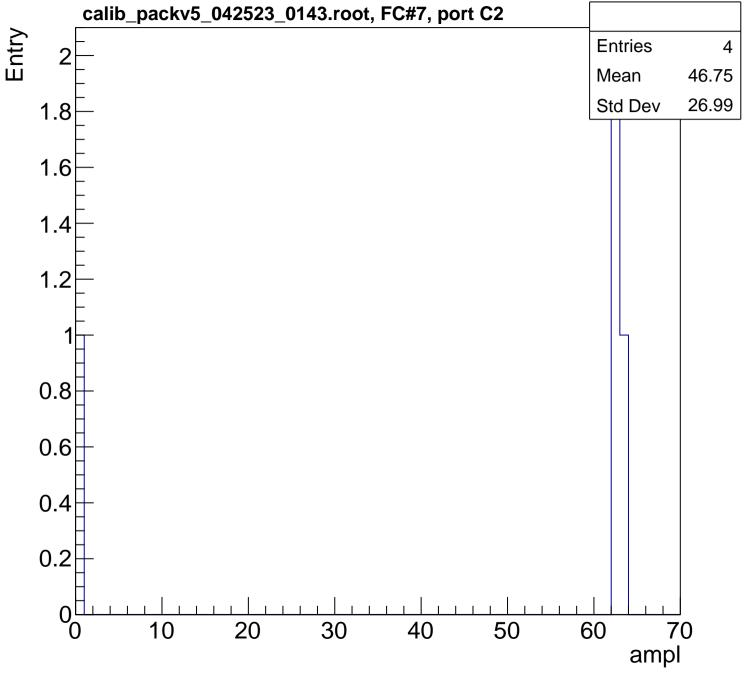


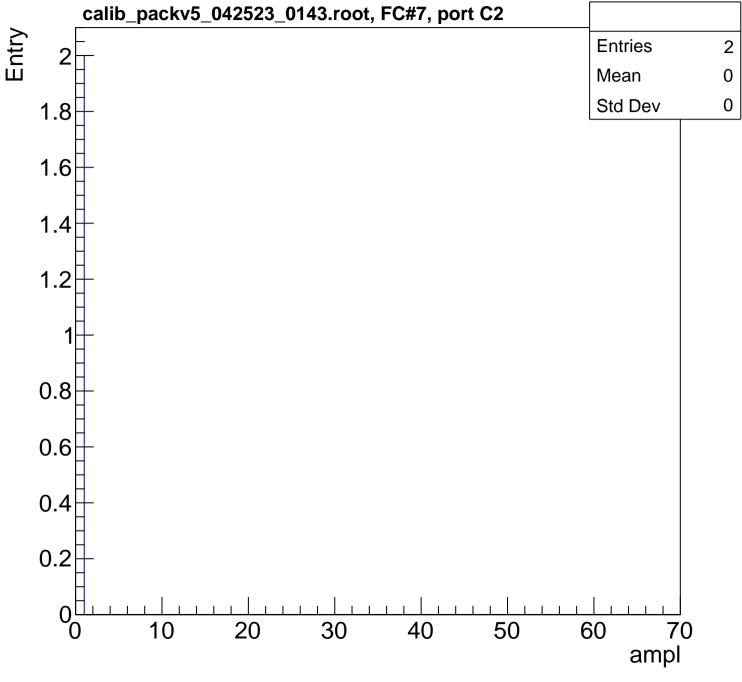


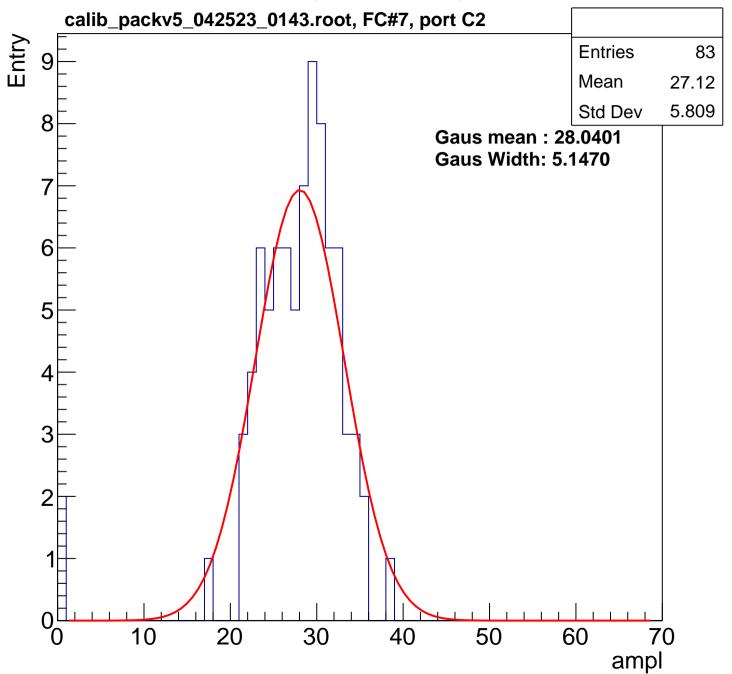


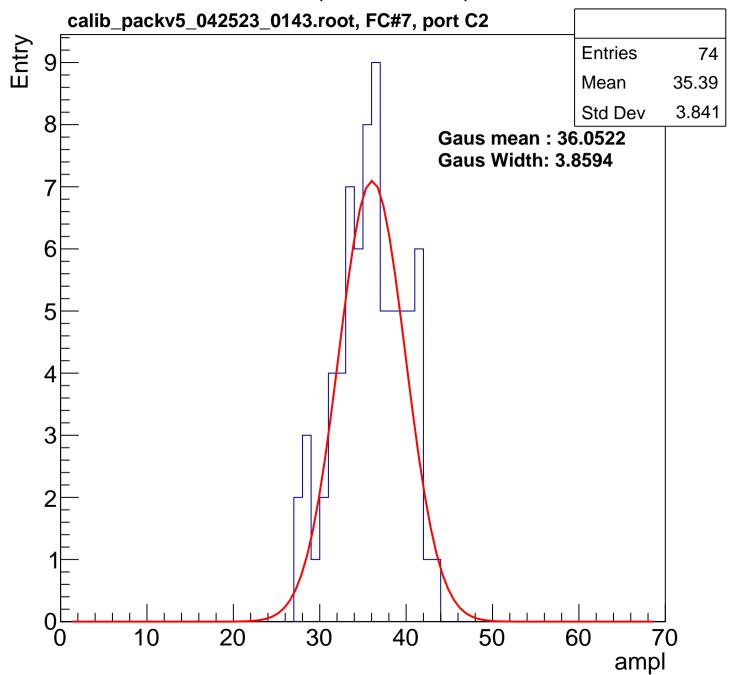


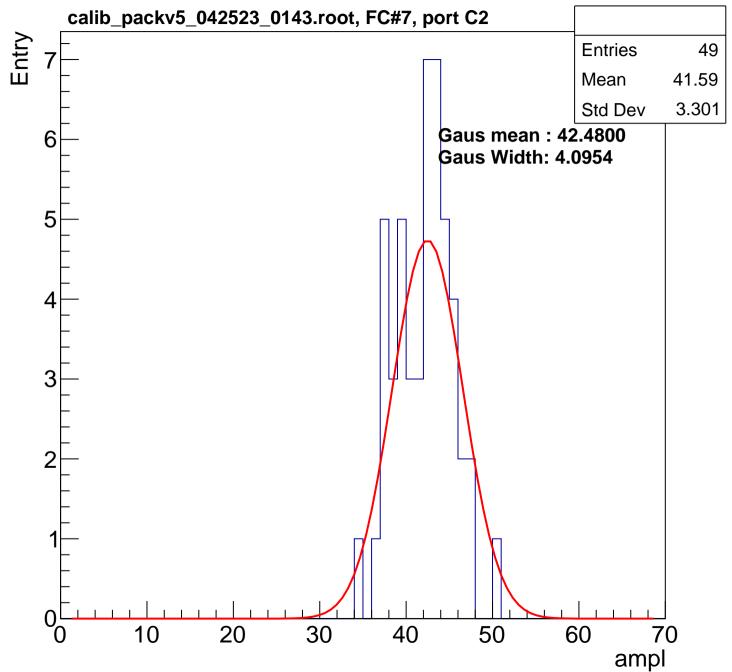


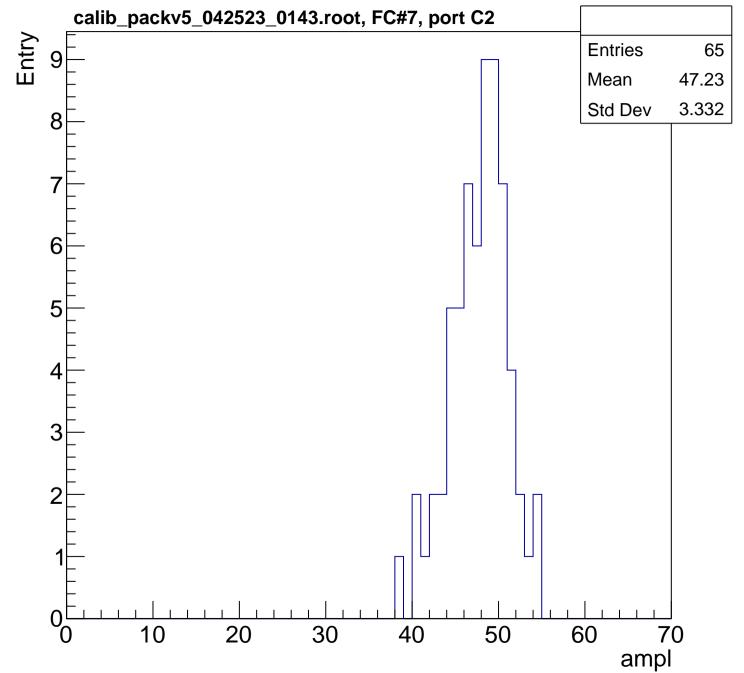


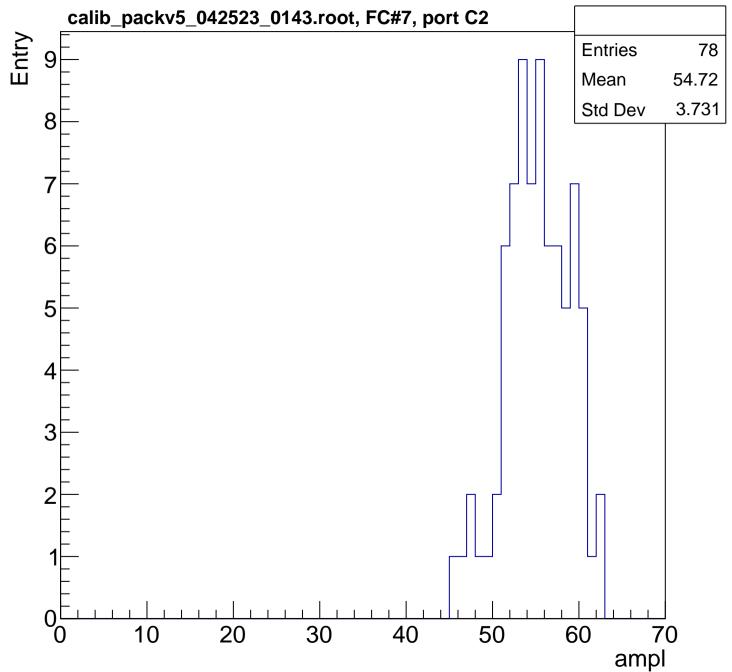


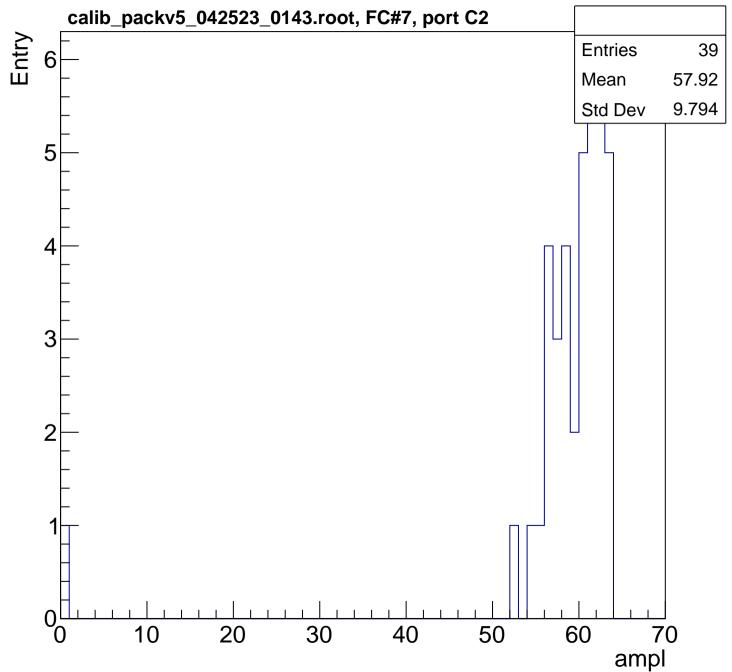


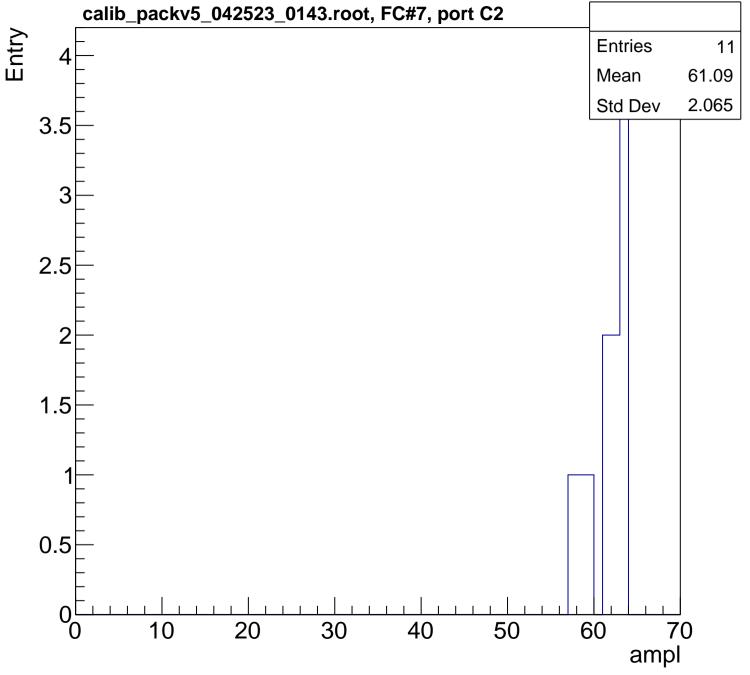


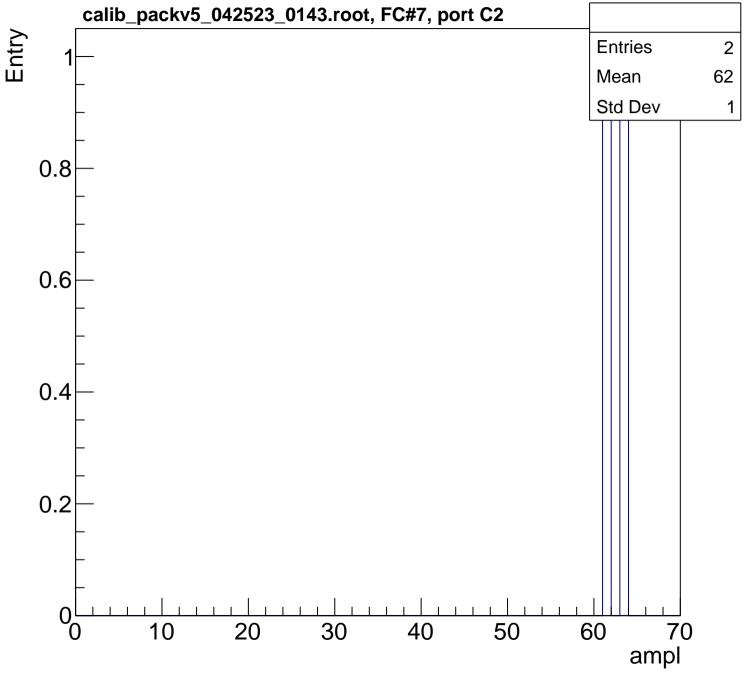


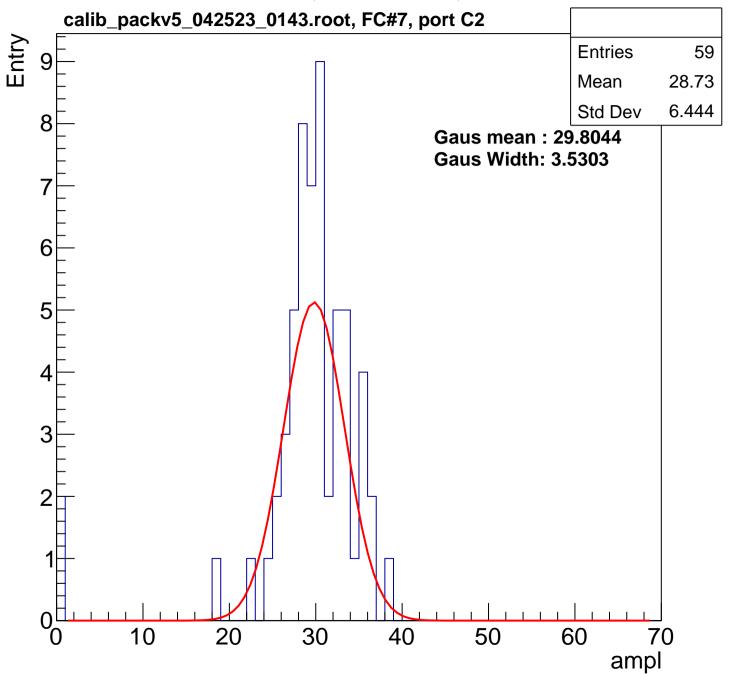


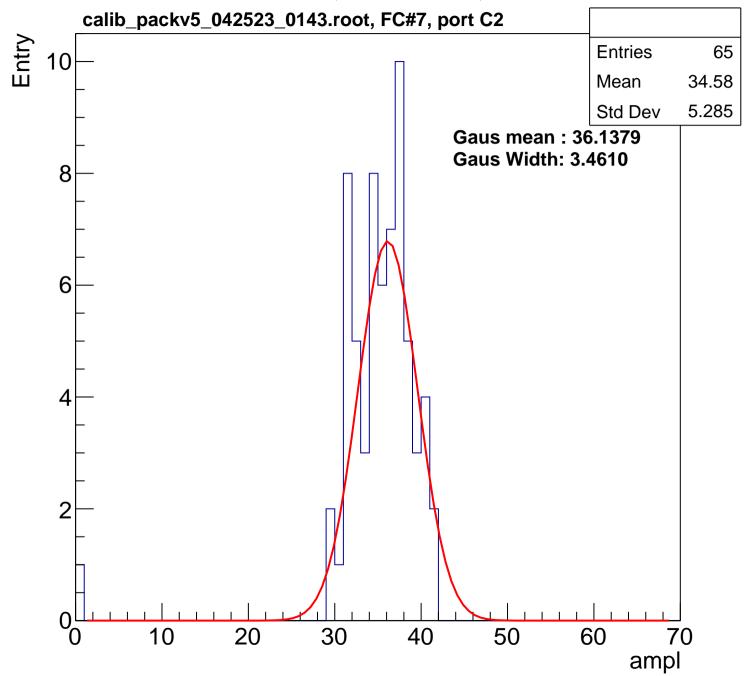


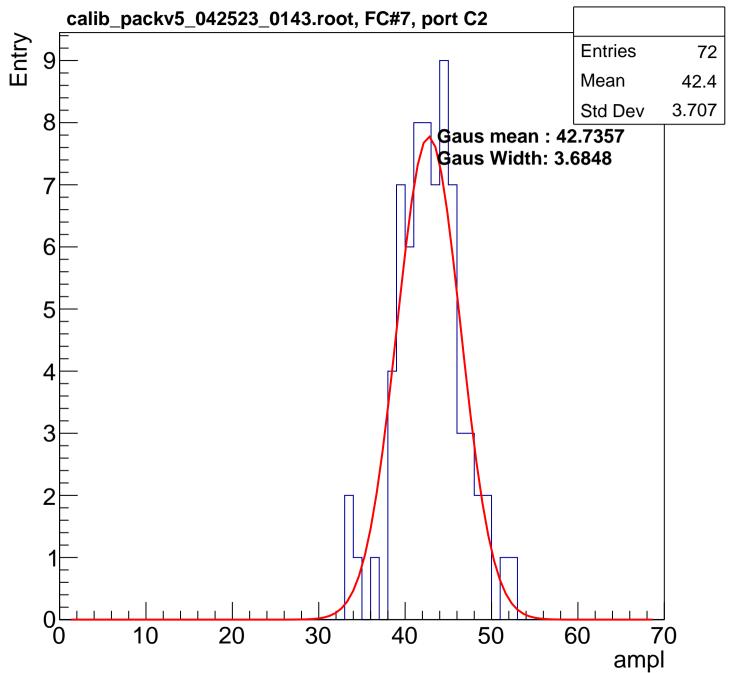


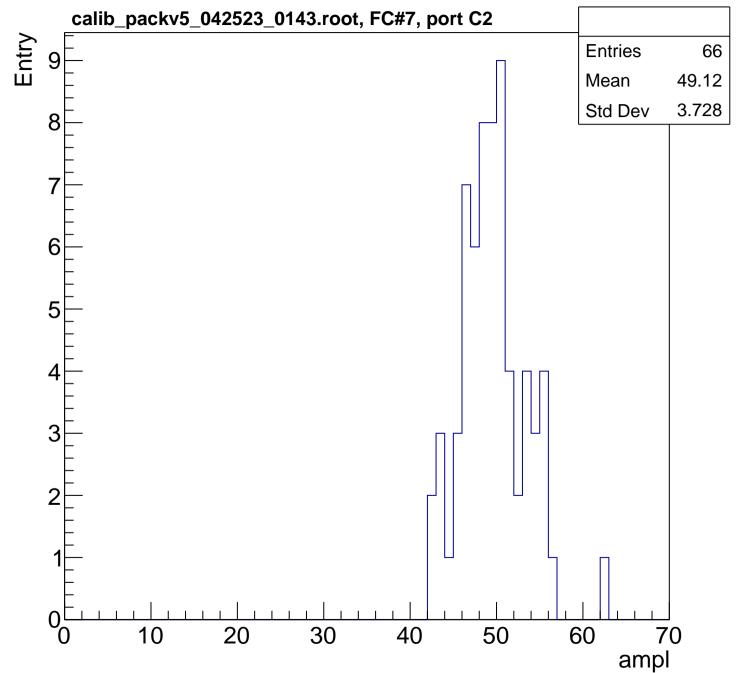


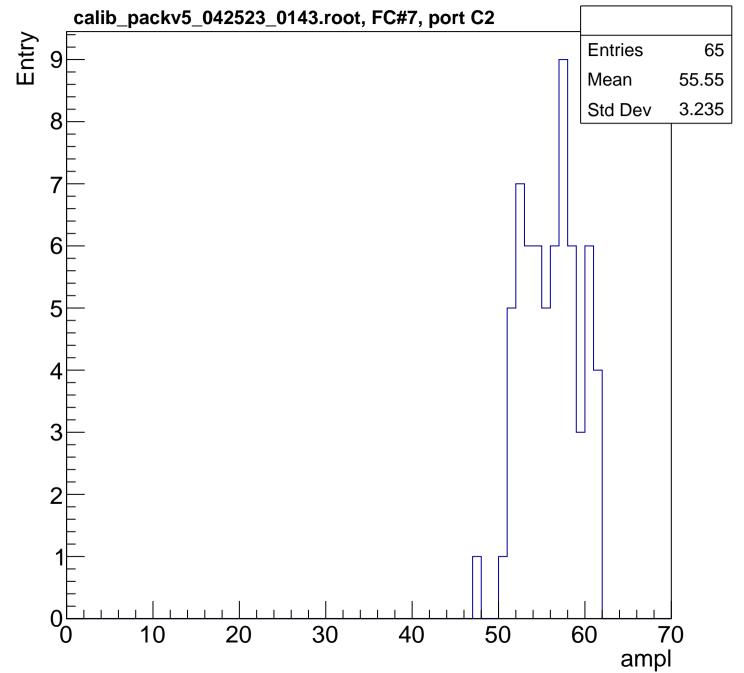


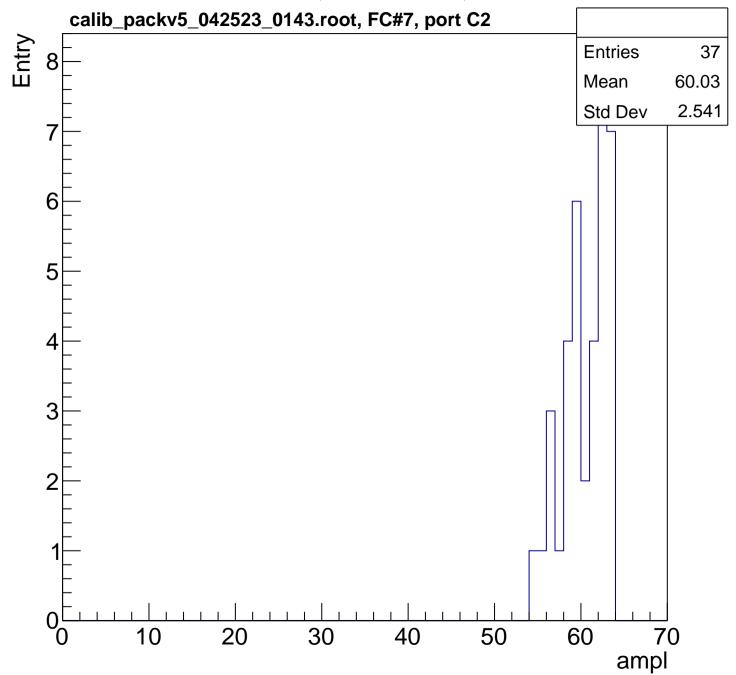


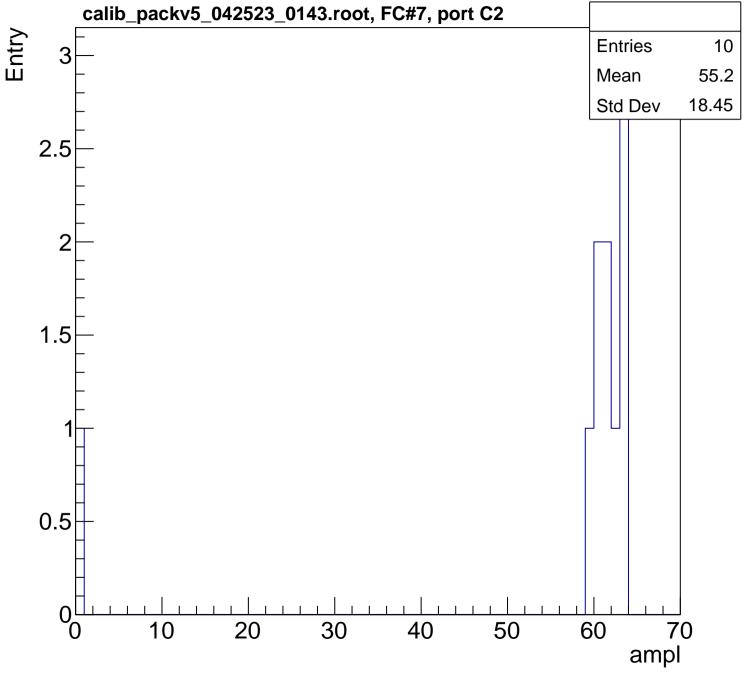


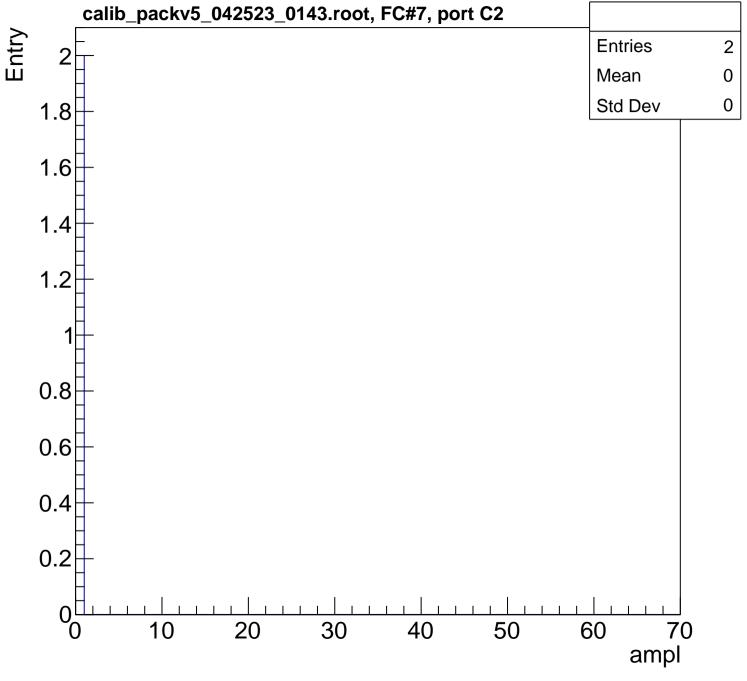


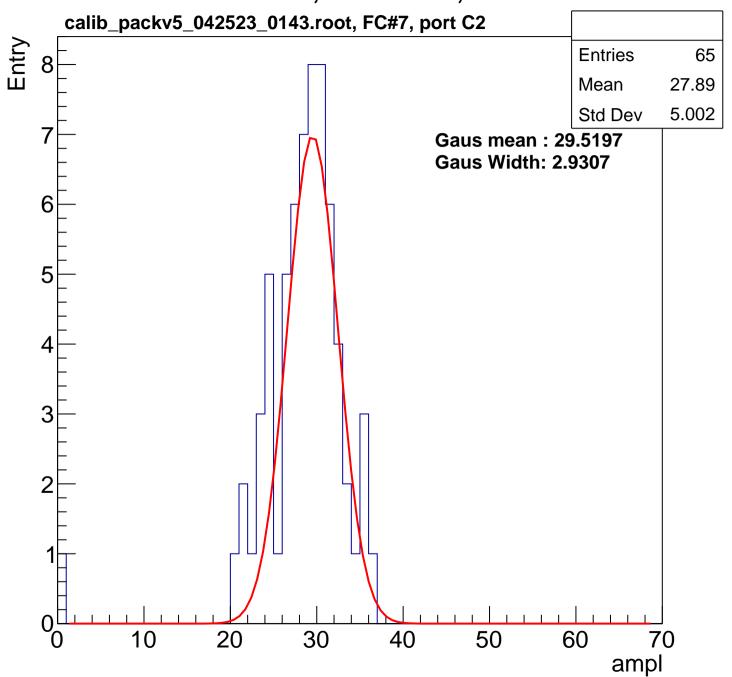


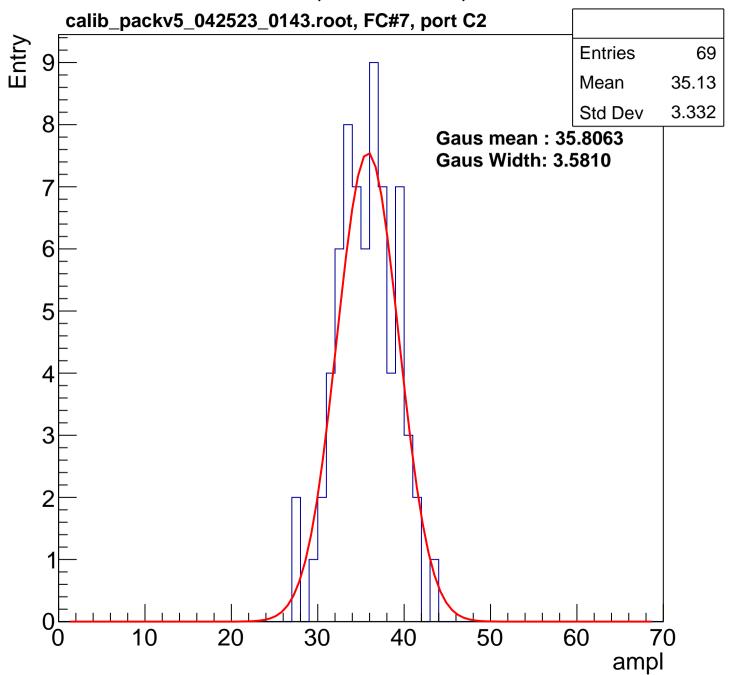


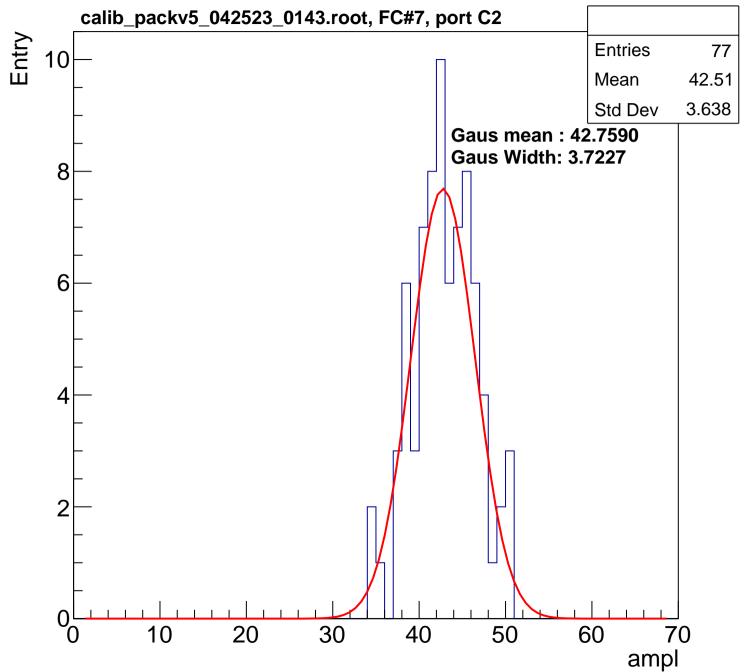


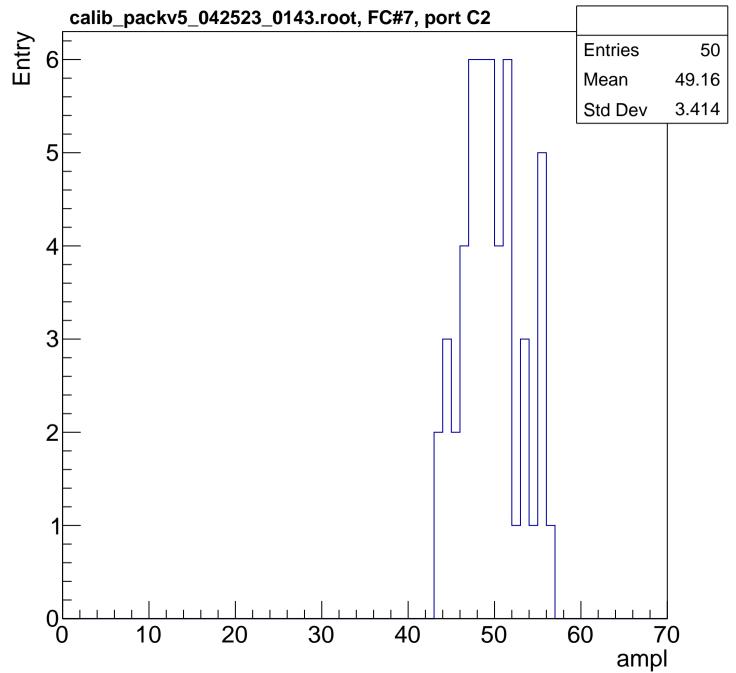


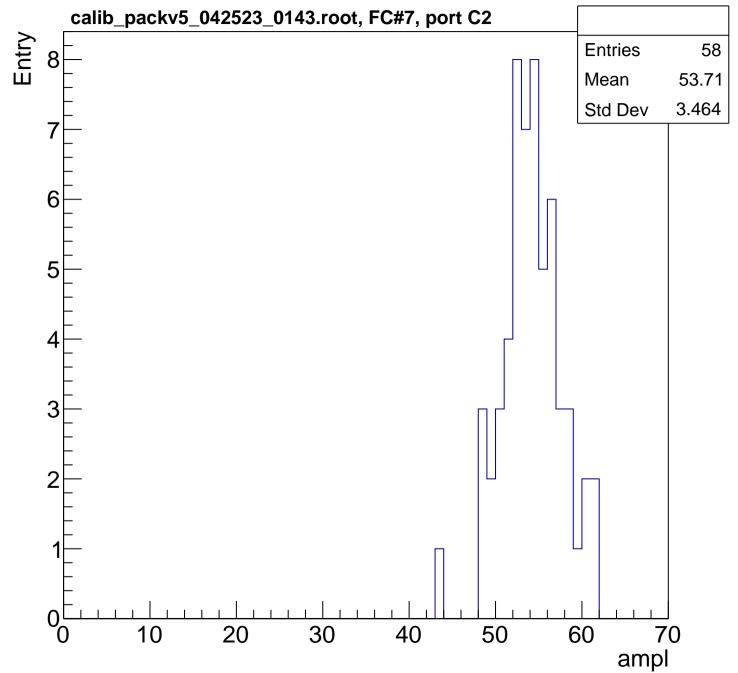


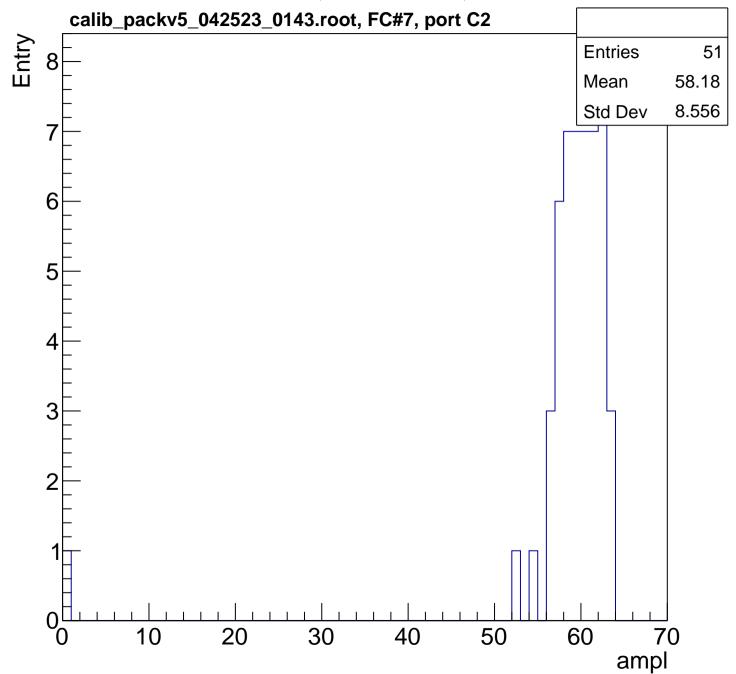


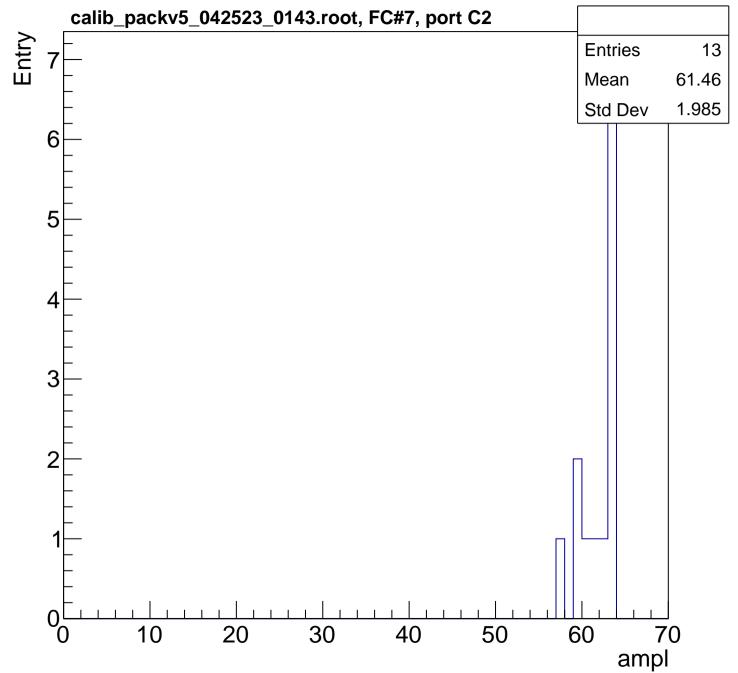


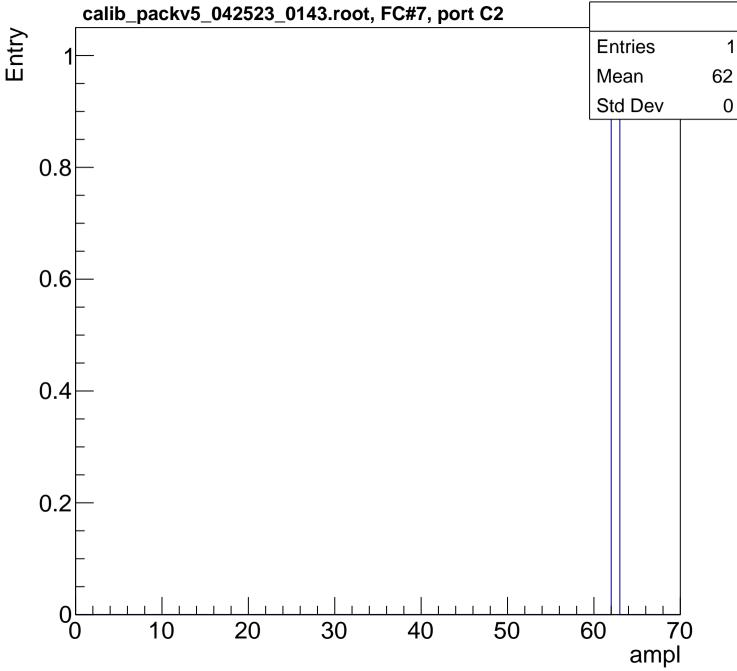


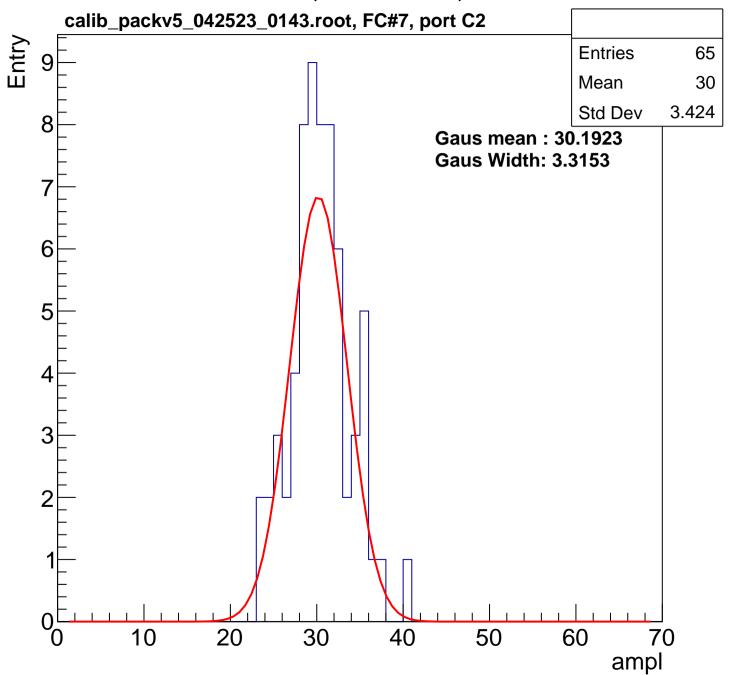


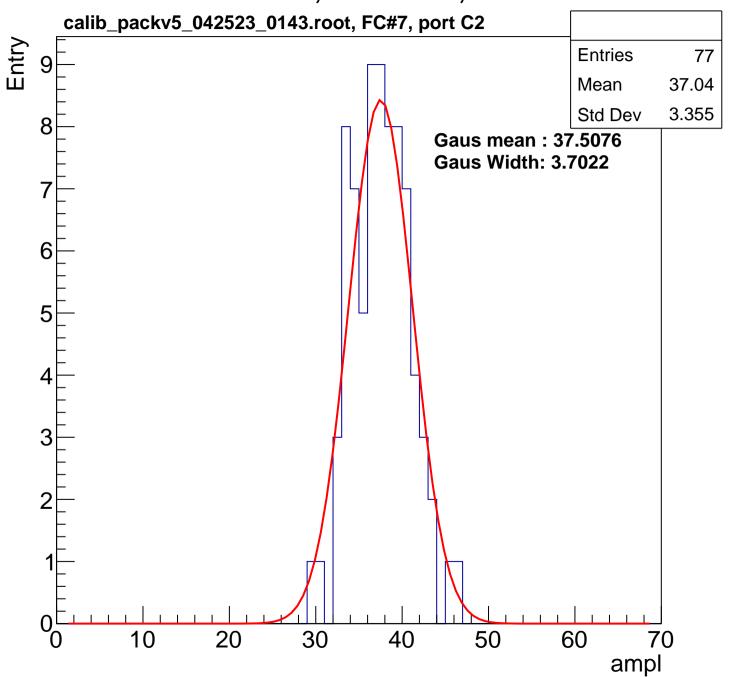


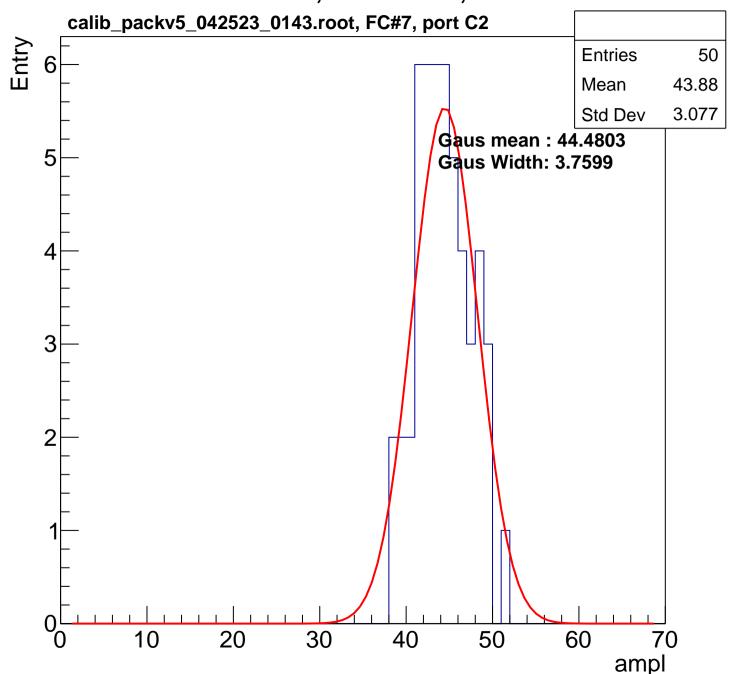


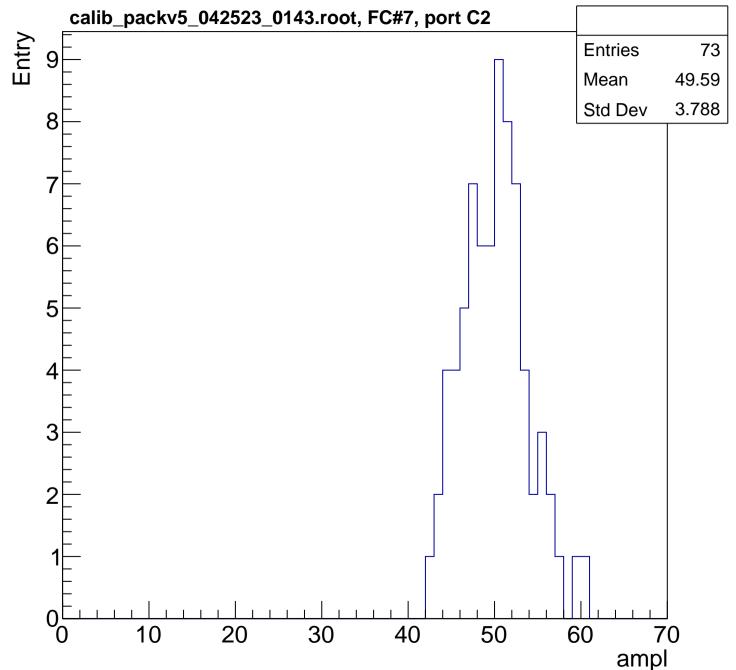


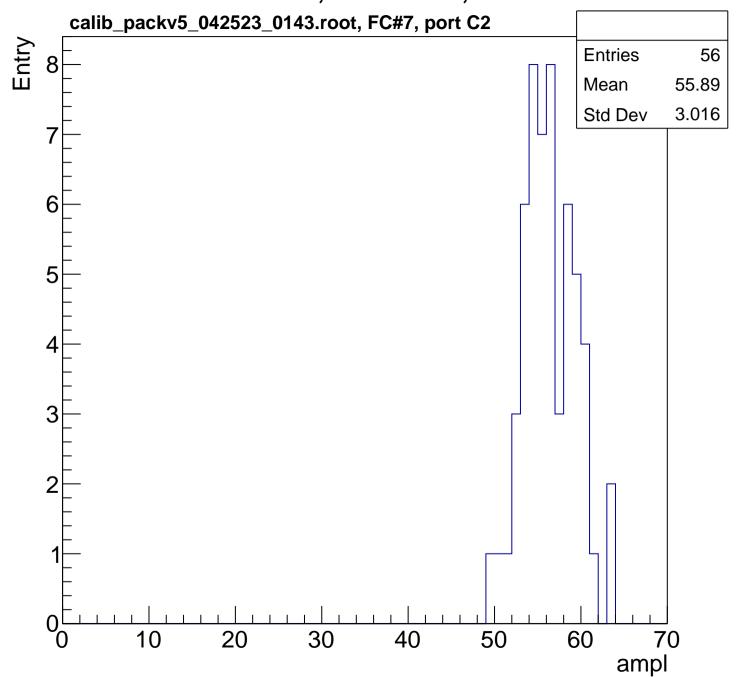


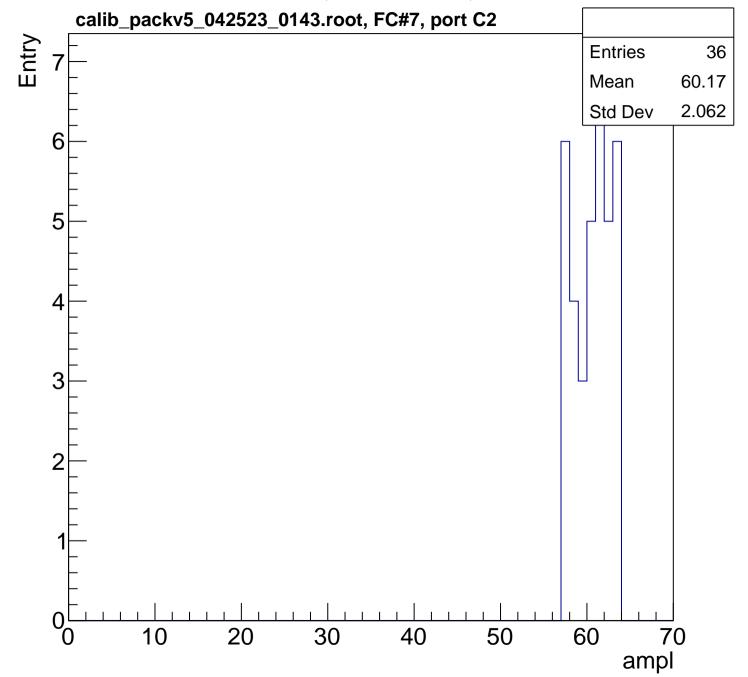


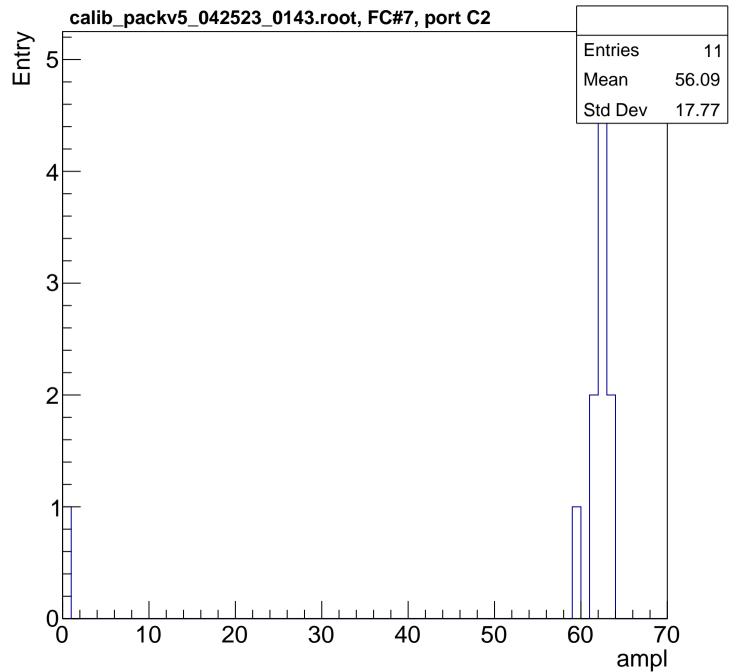


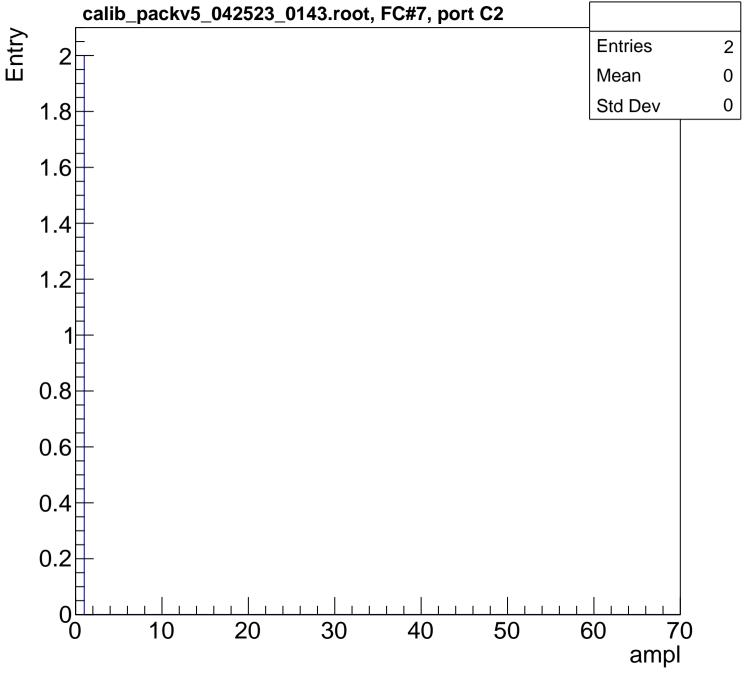


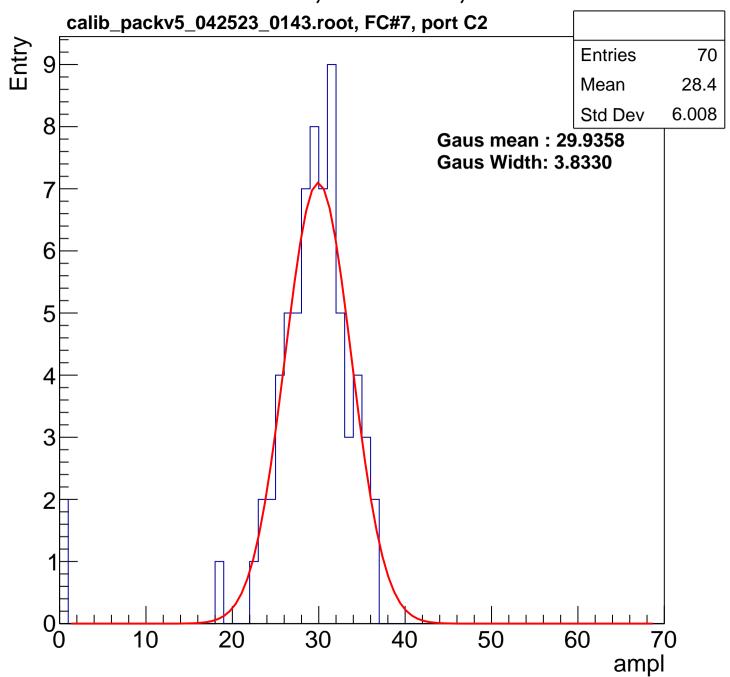


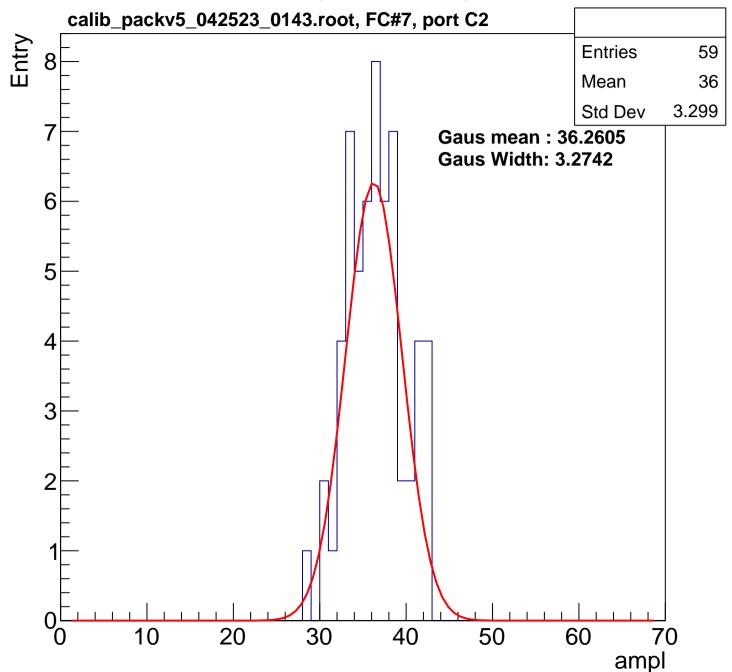


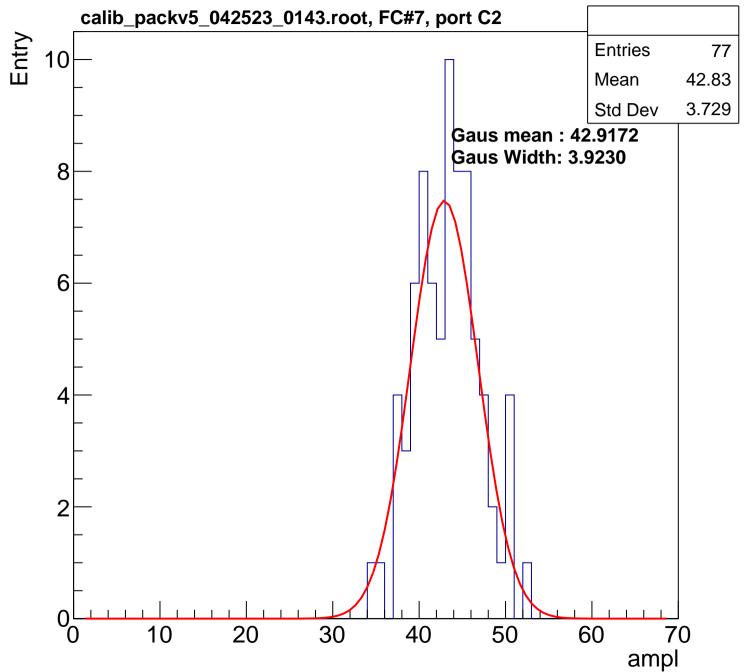


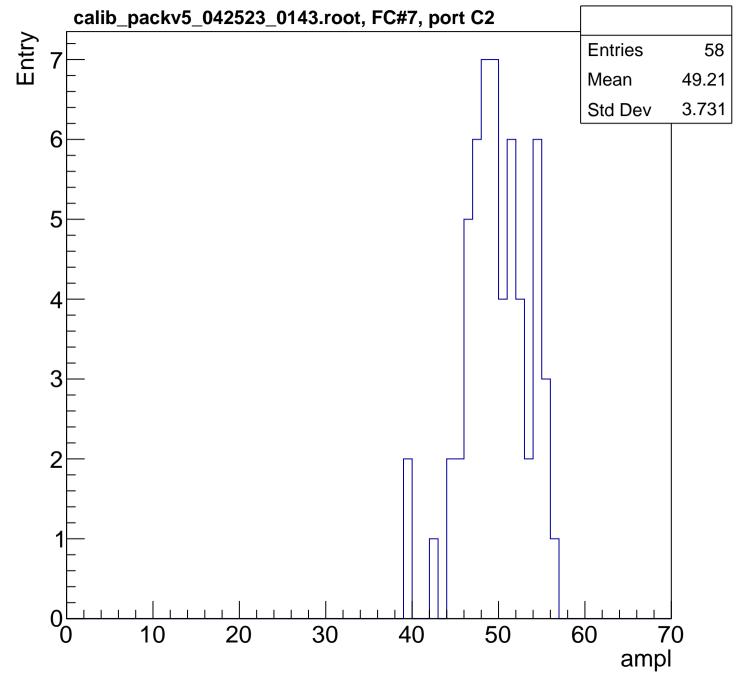


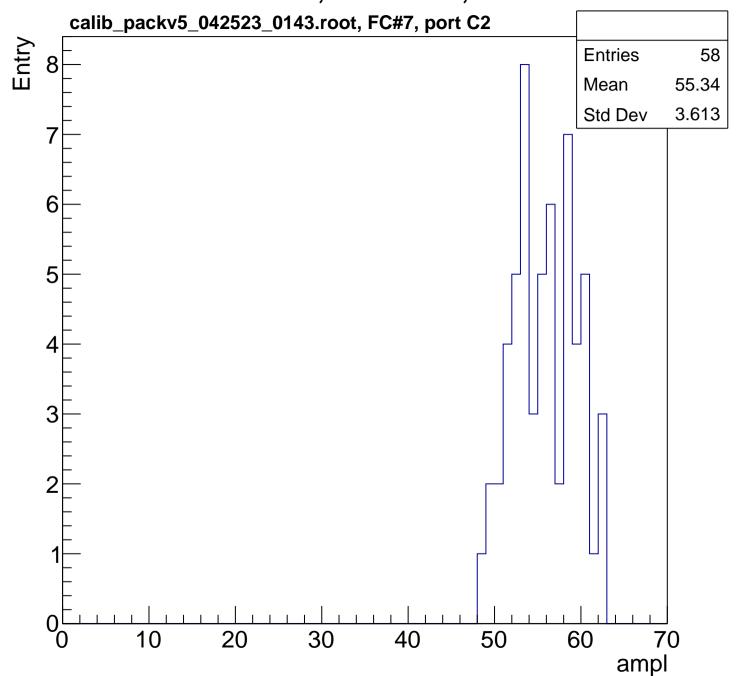


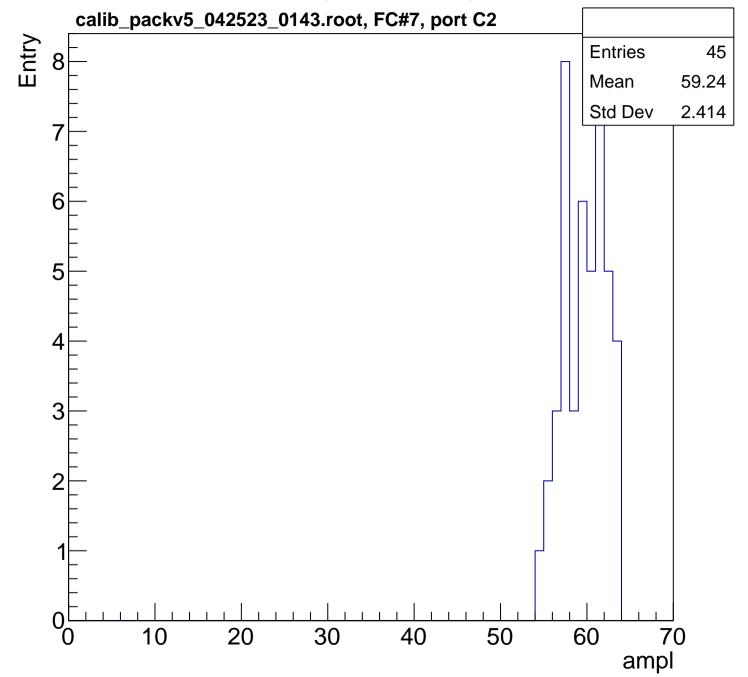


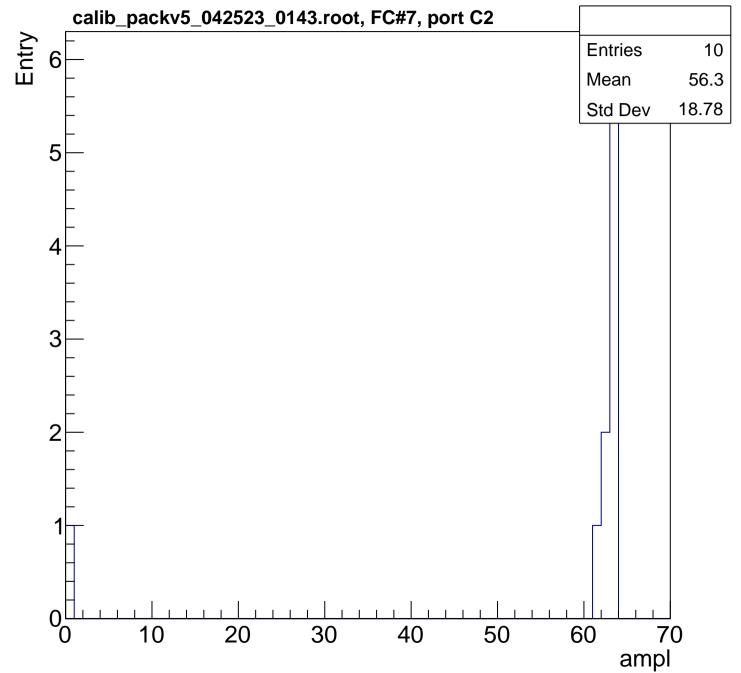


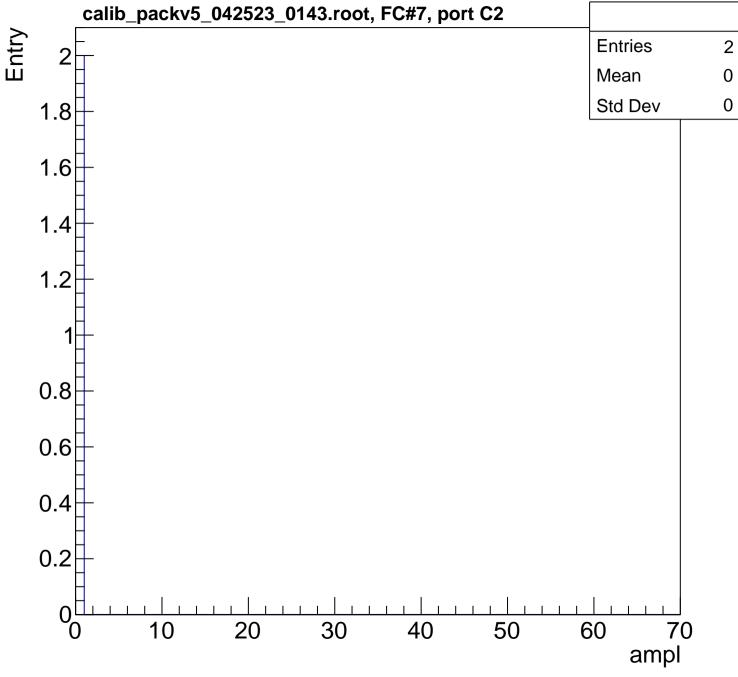


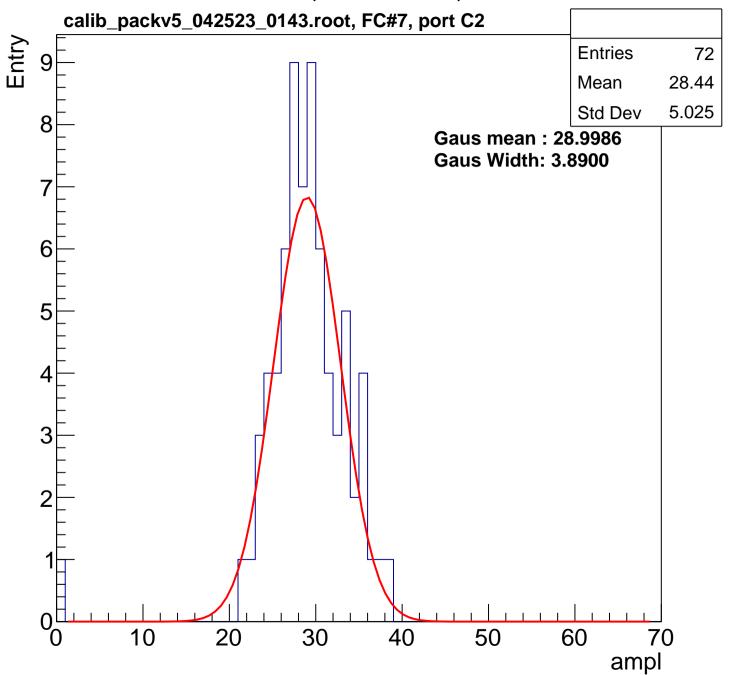


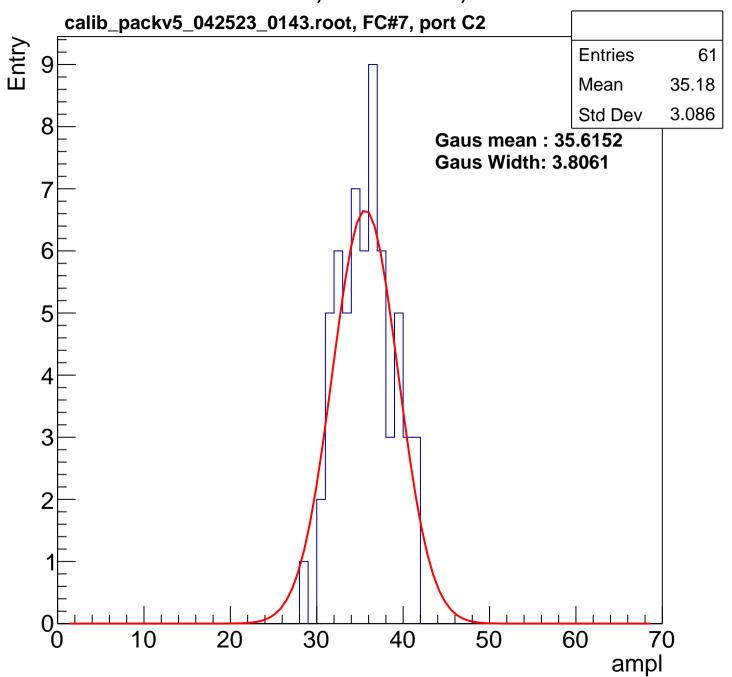


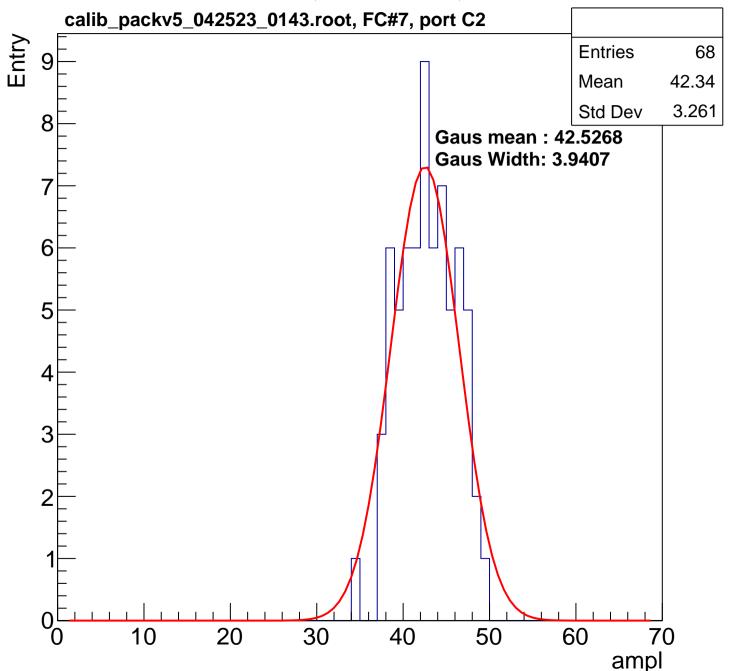


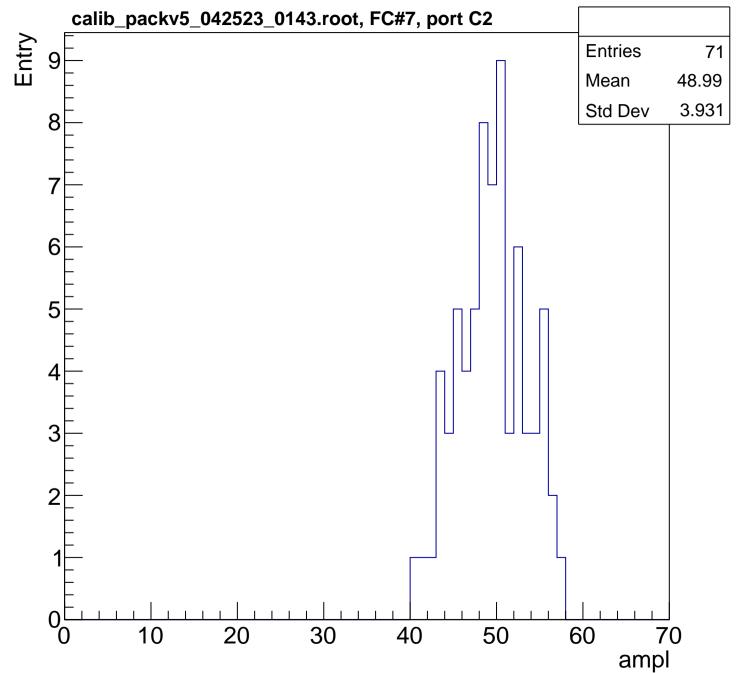


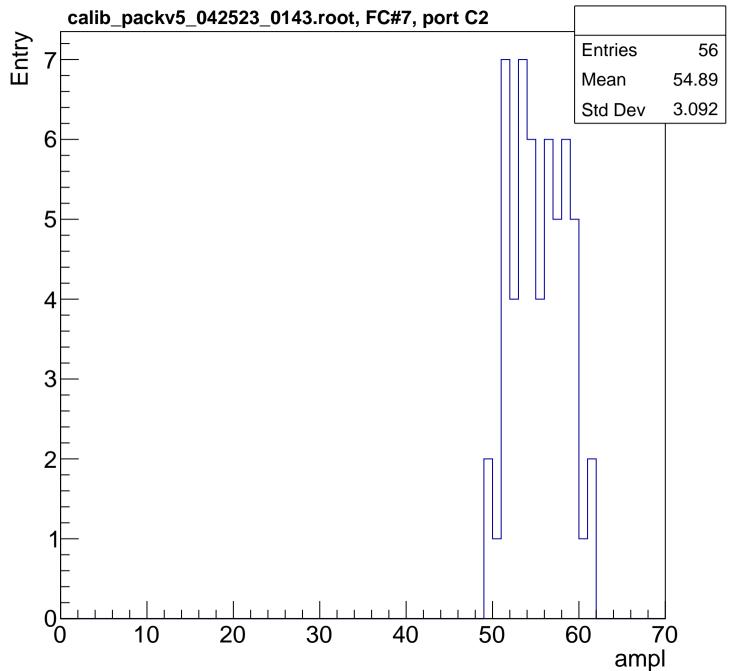


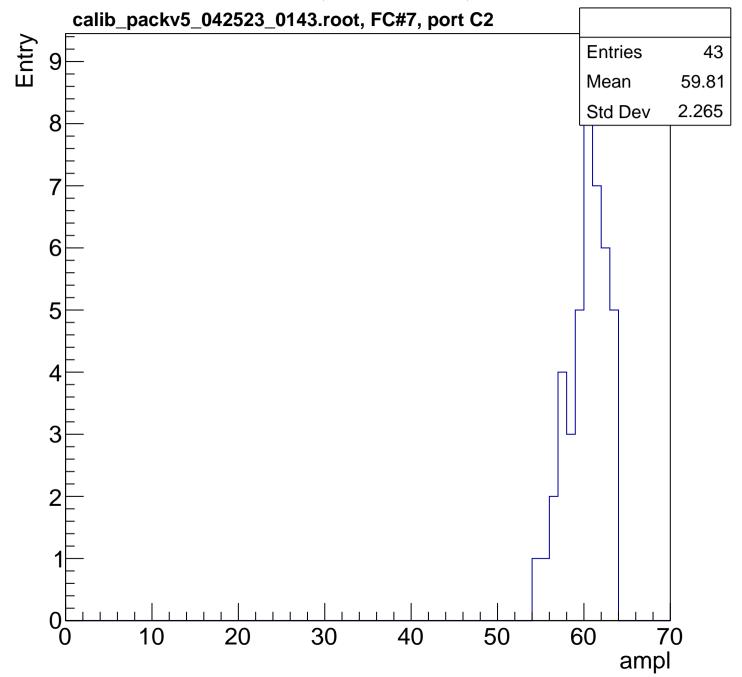


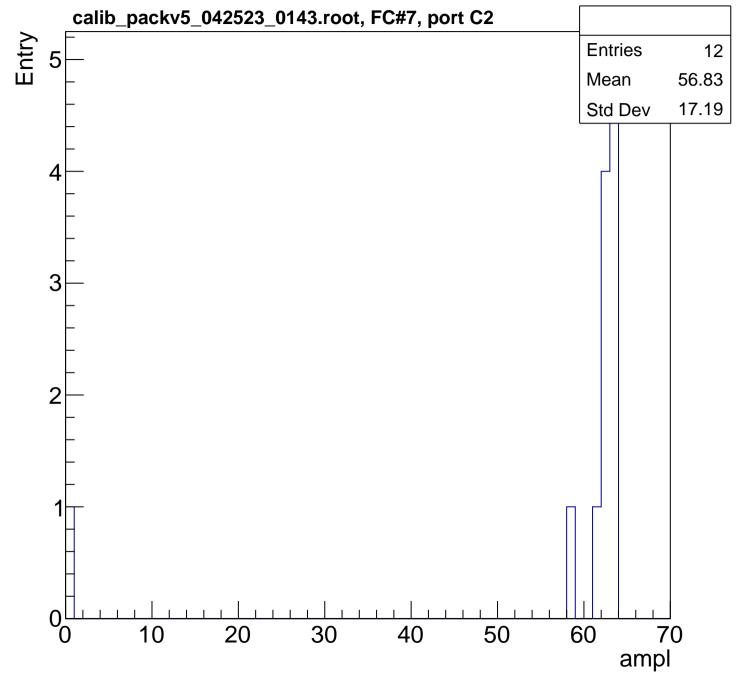


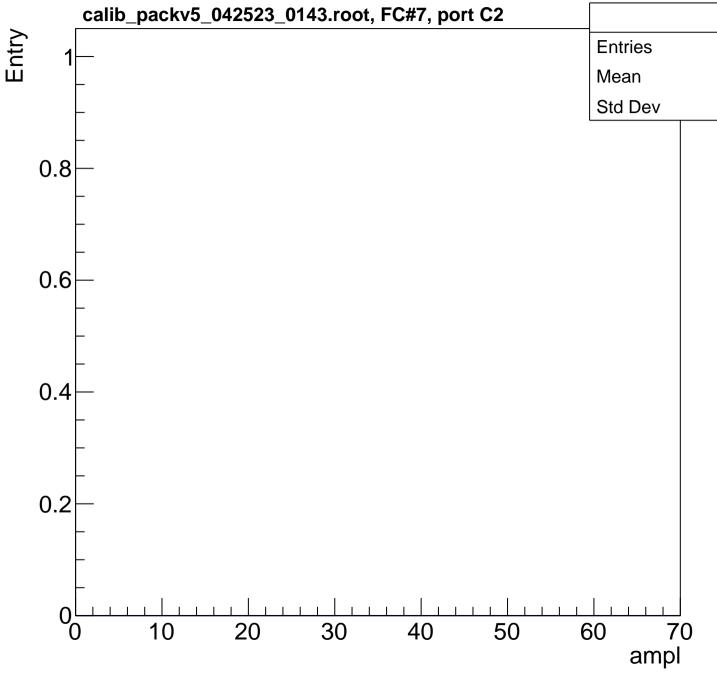


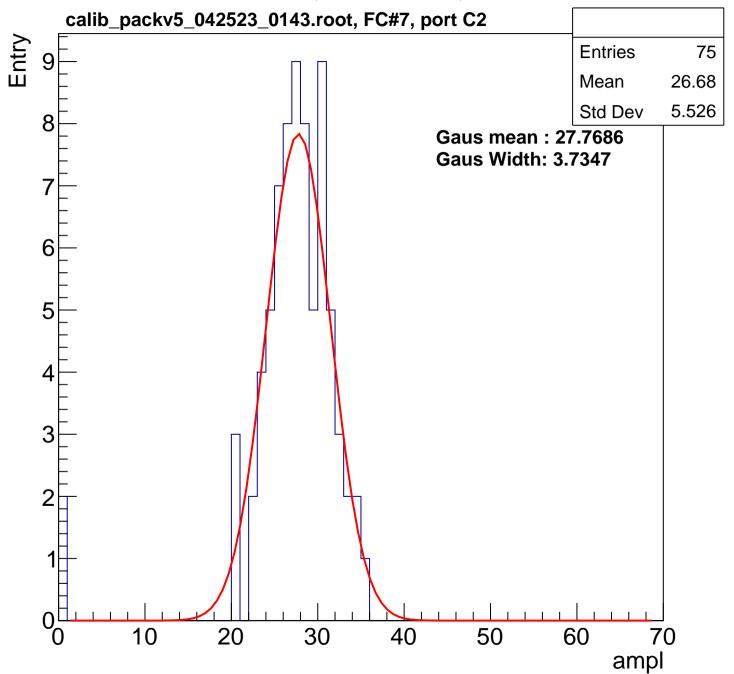


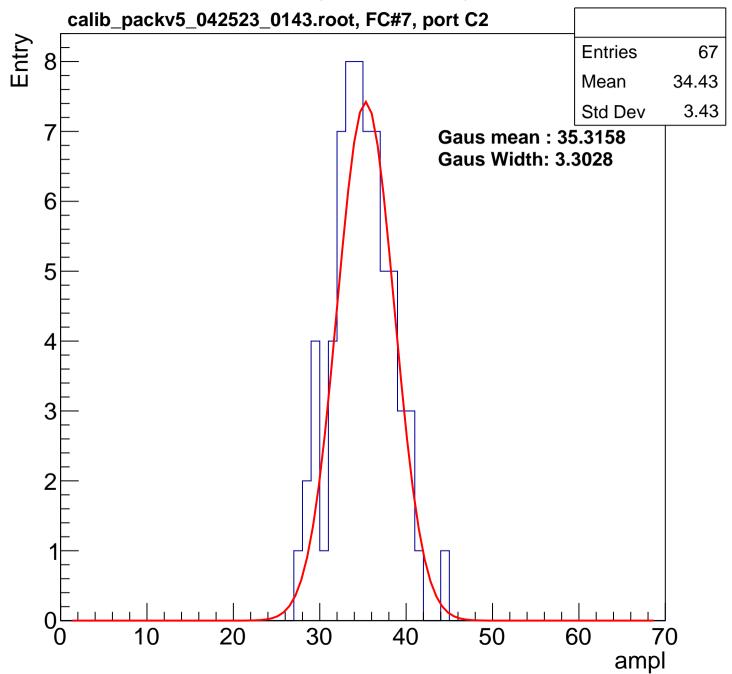


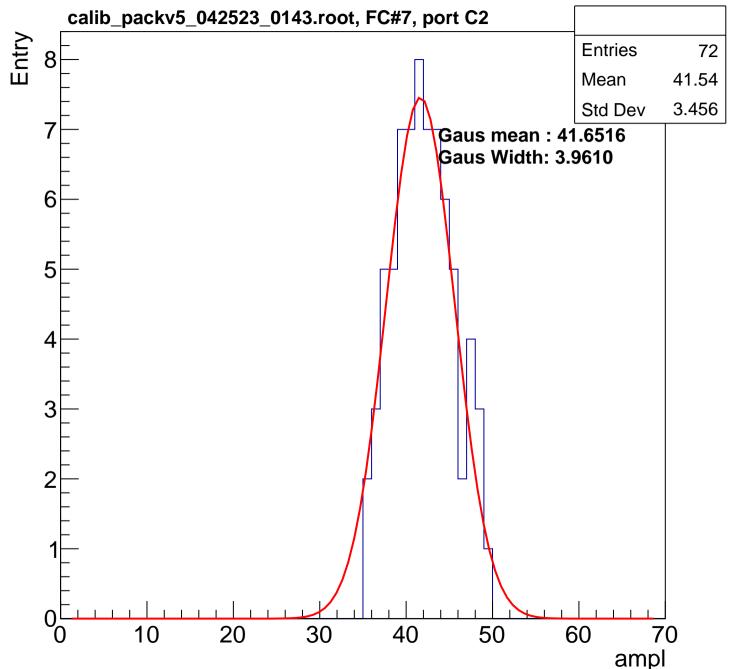


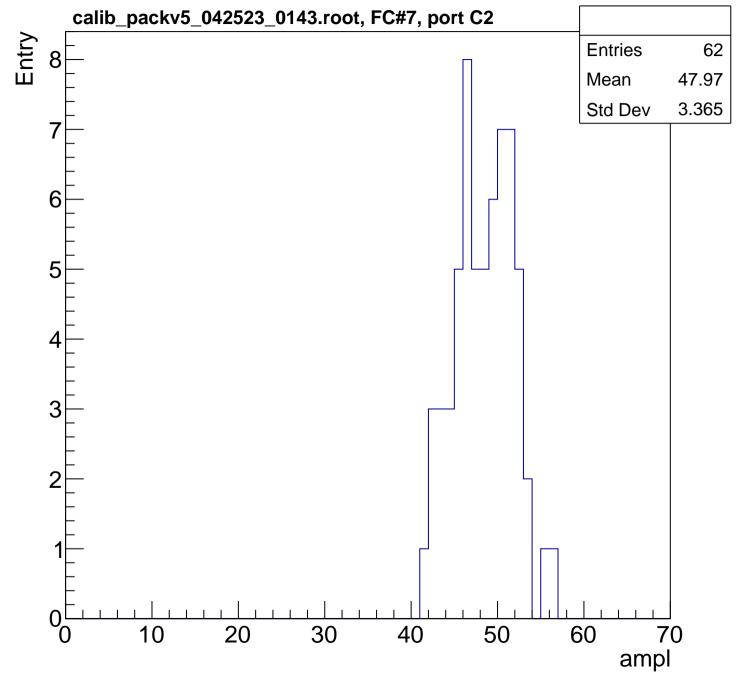


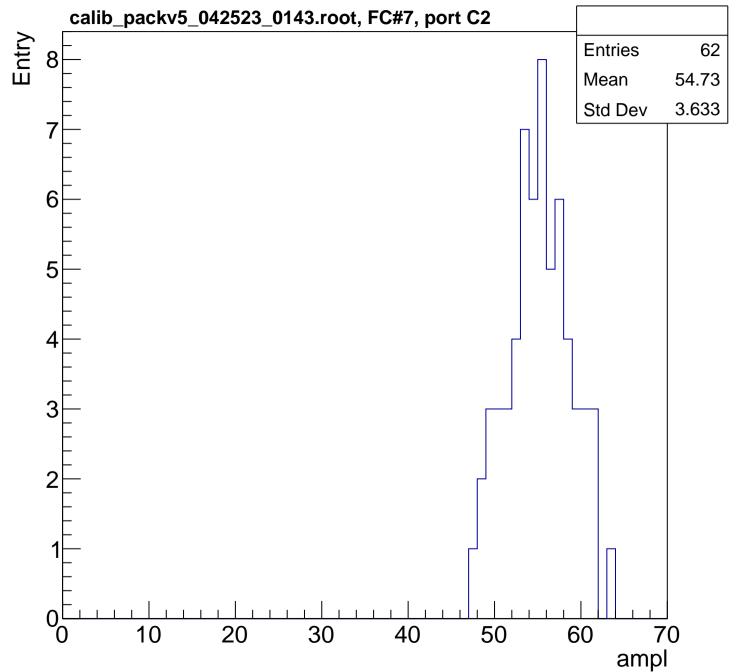


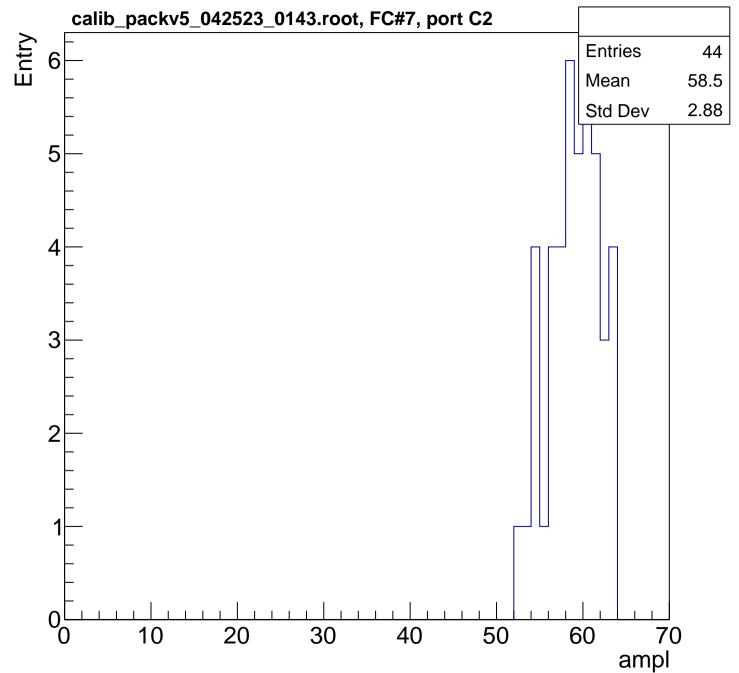


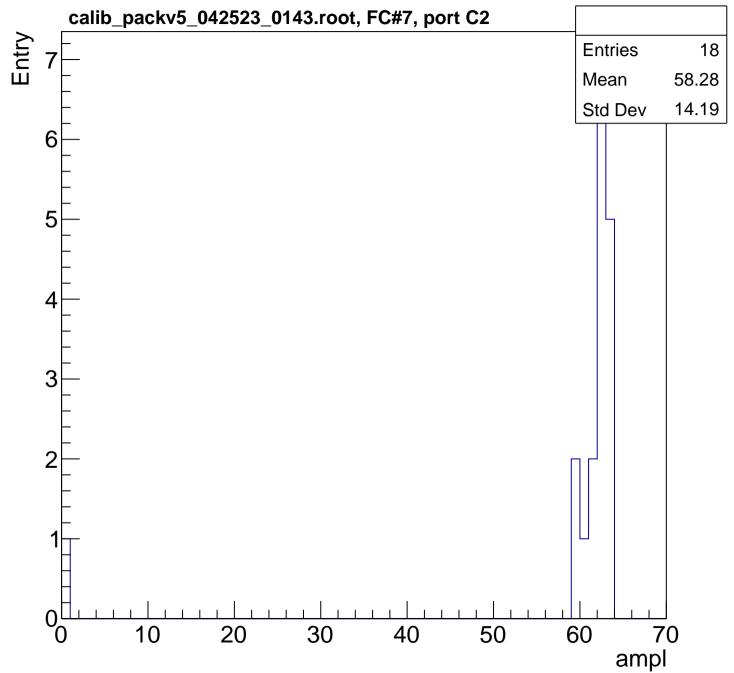












B1L103S, U4-ch52, adc7 calib_packv5_042523_0143.root, FC#7, port C2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2

30

40

50

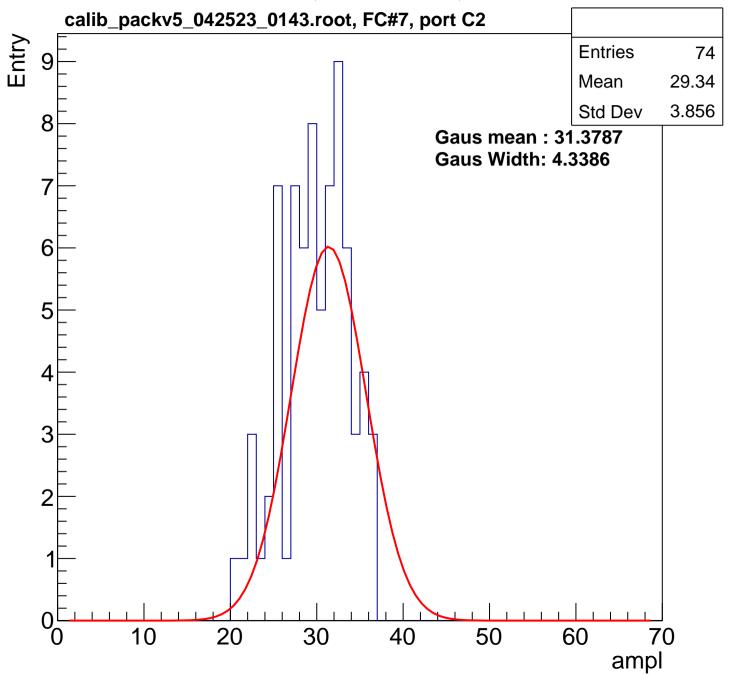
60

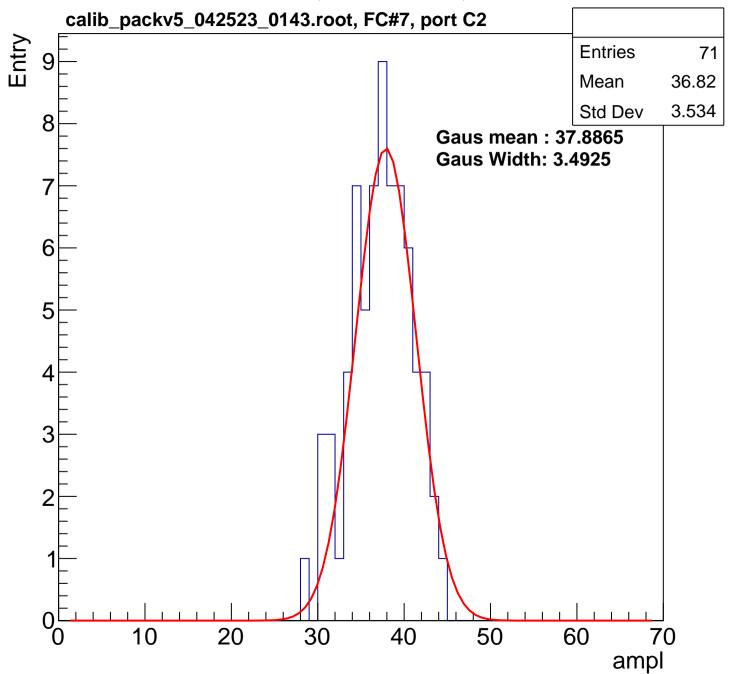
70

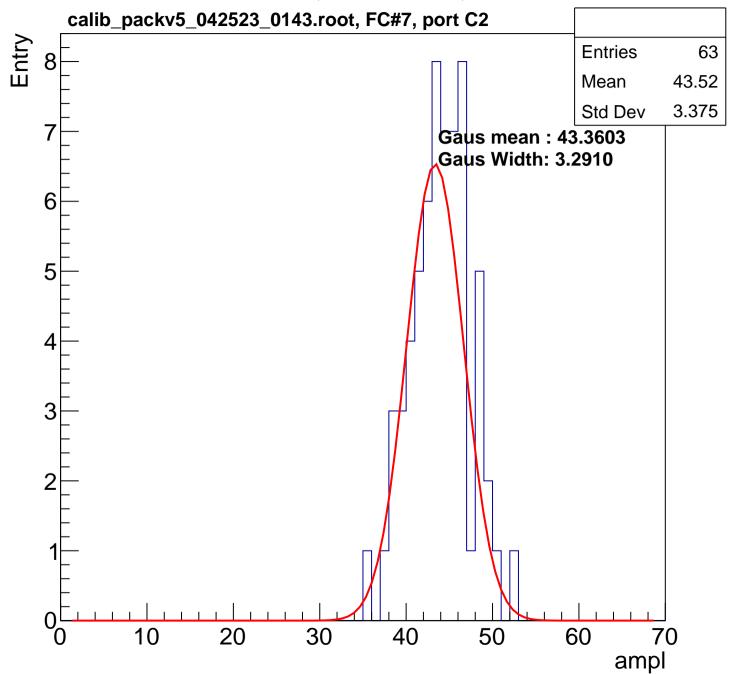
ampl

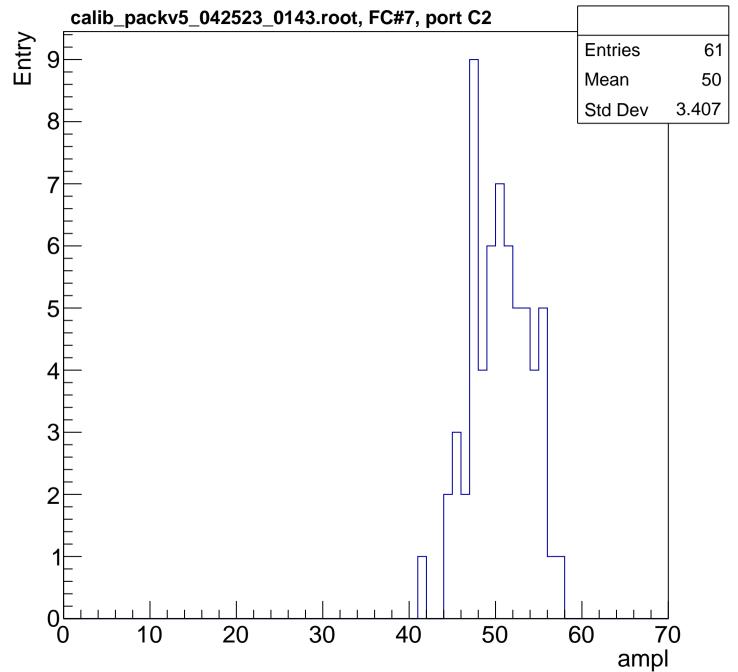
10

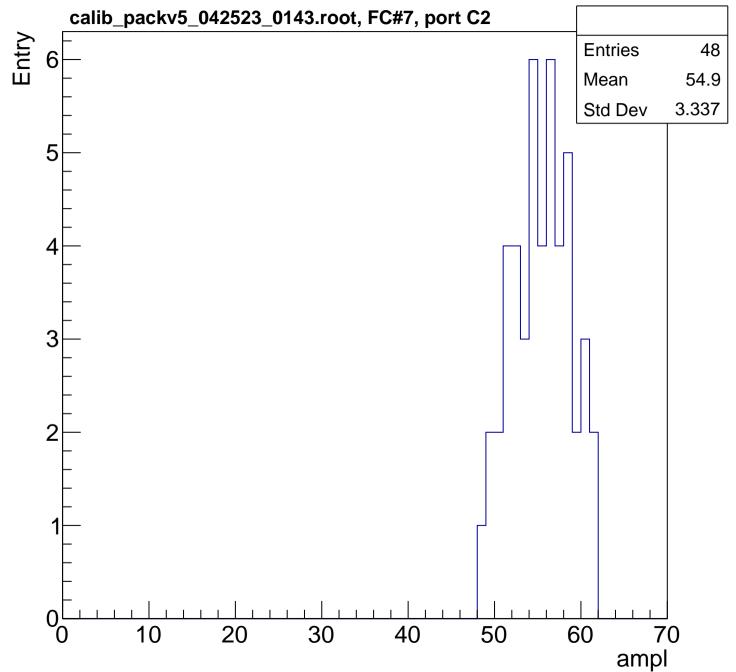
20

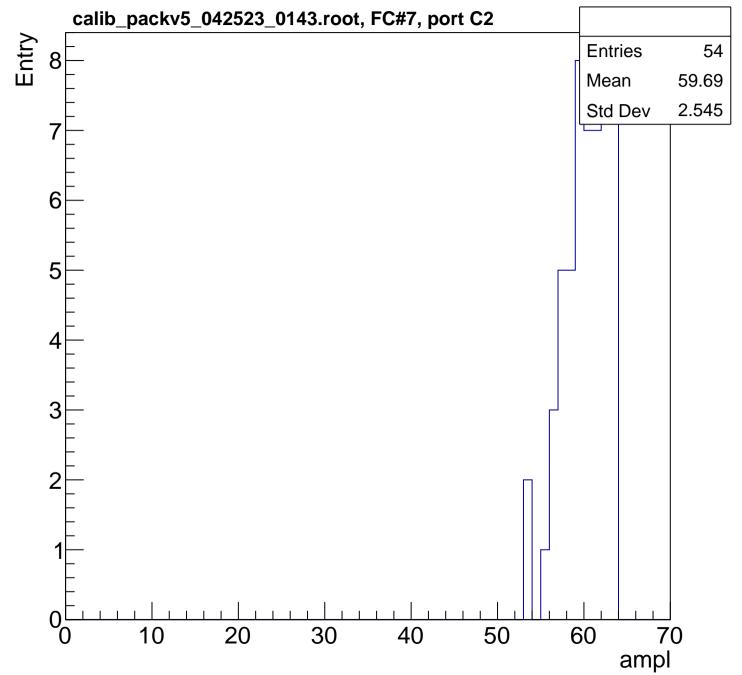


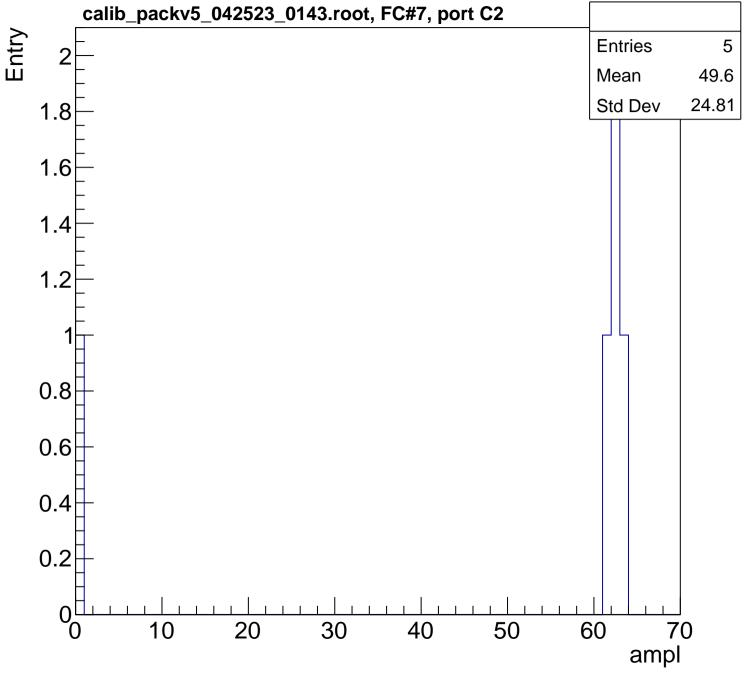




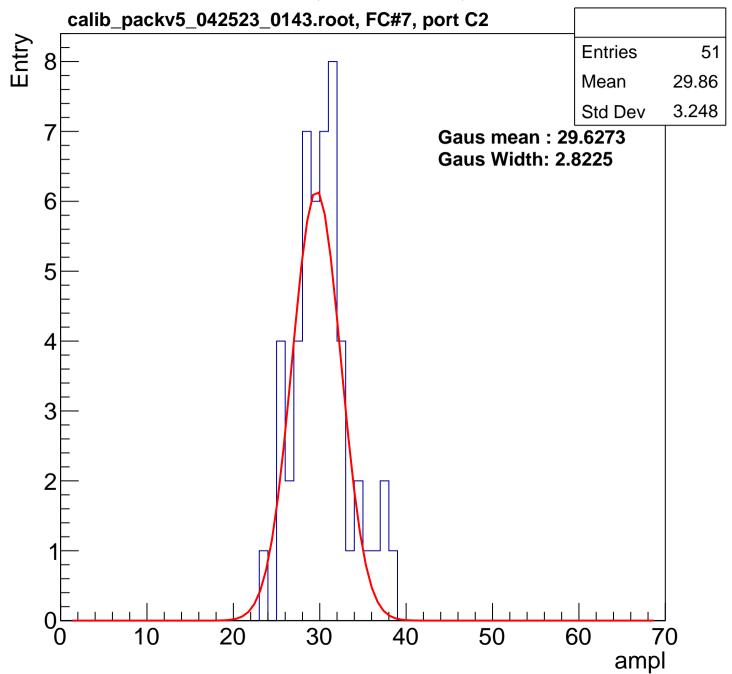


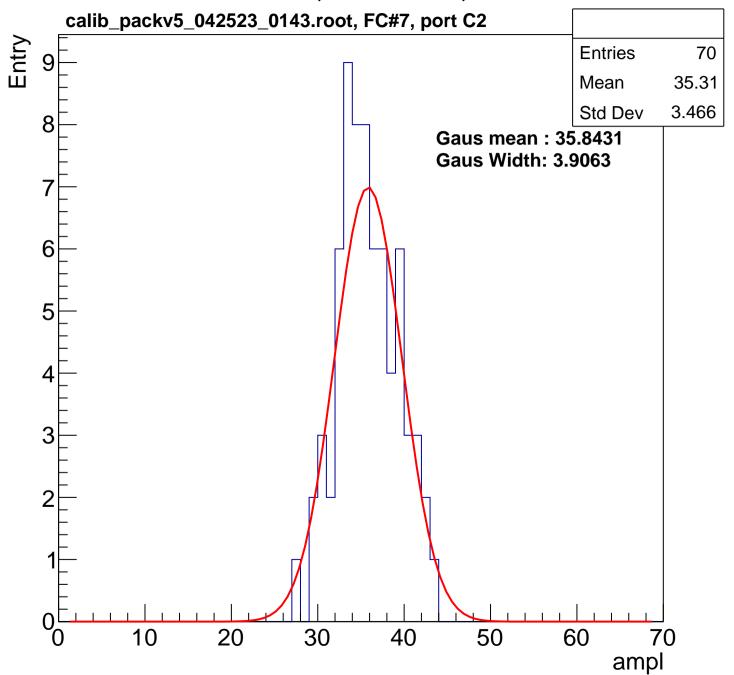


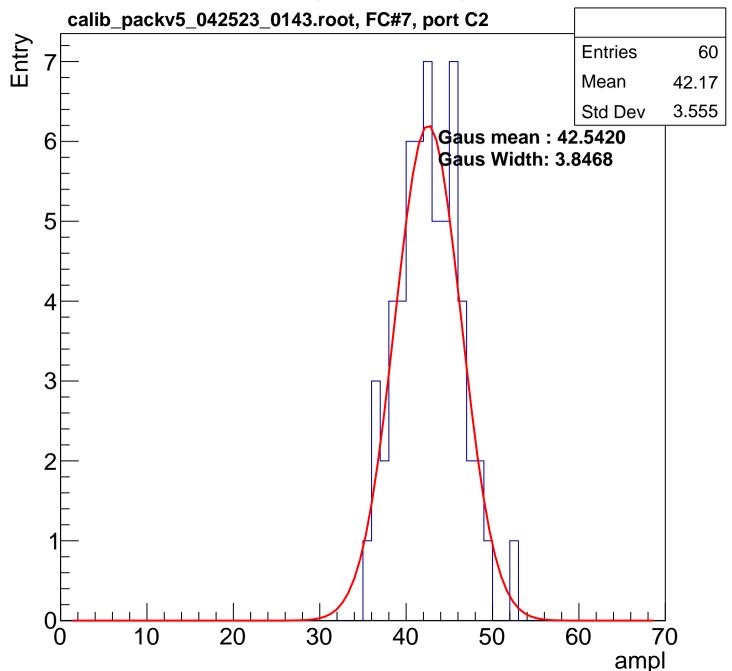


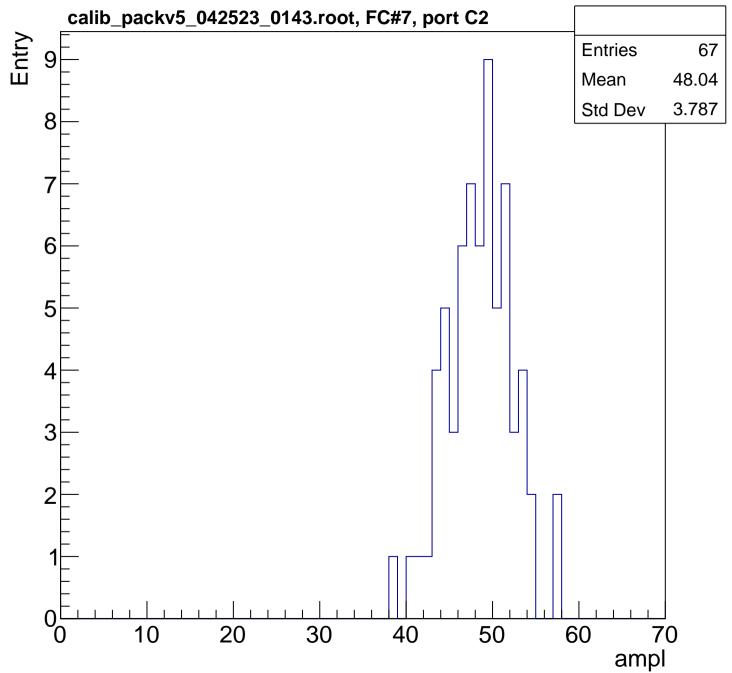


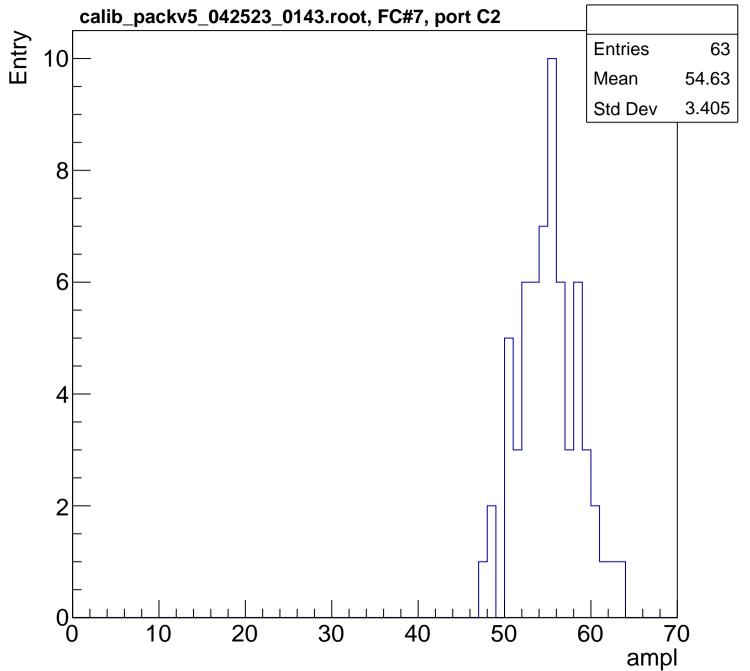


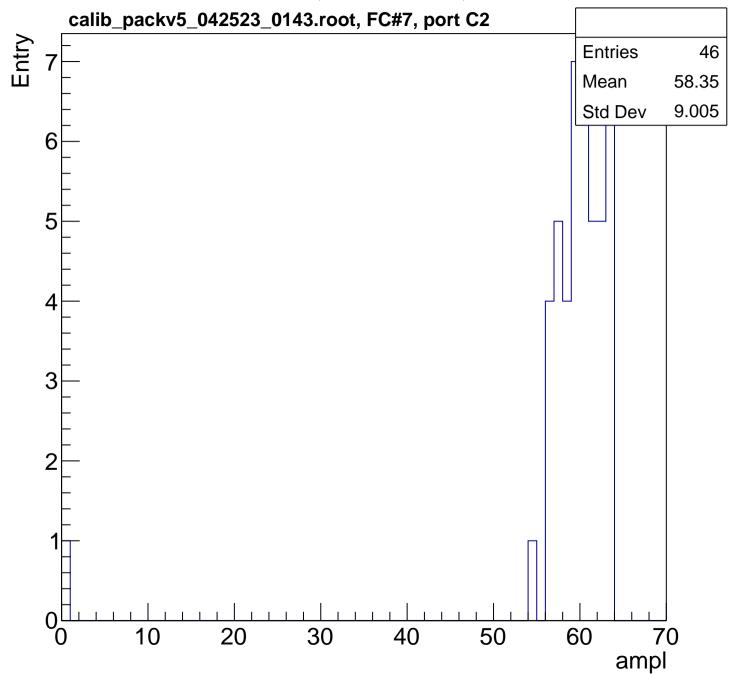


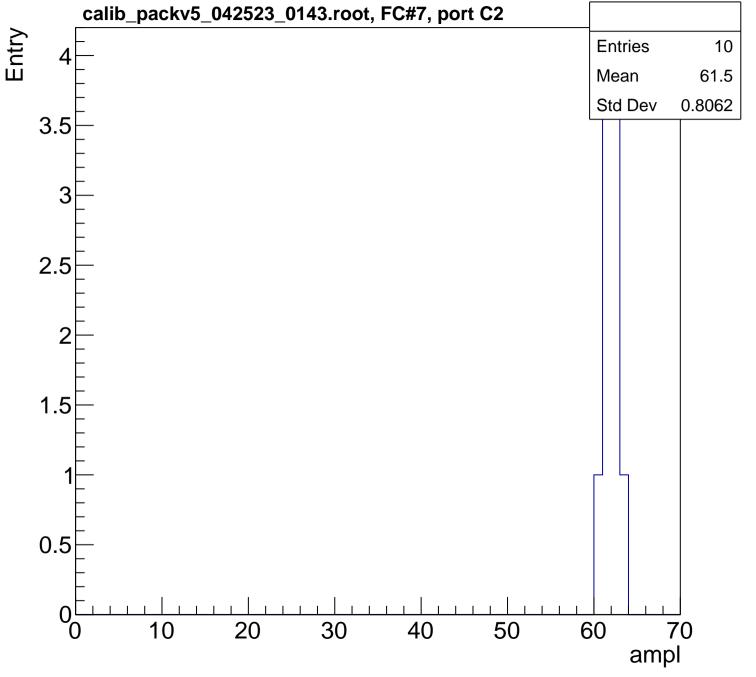


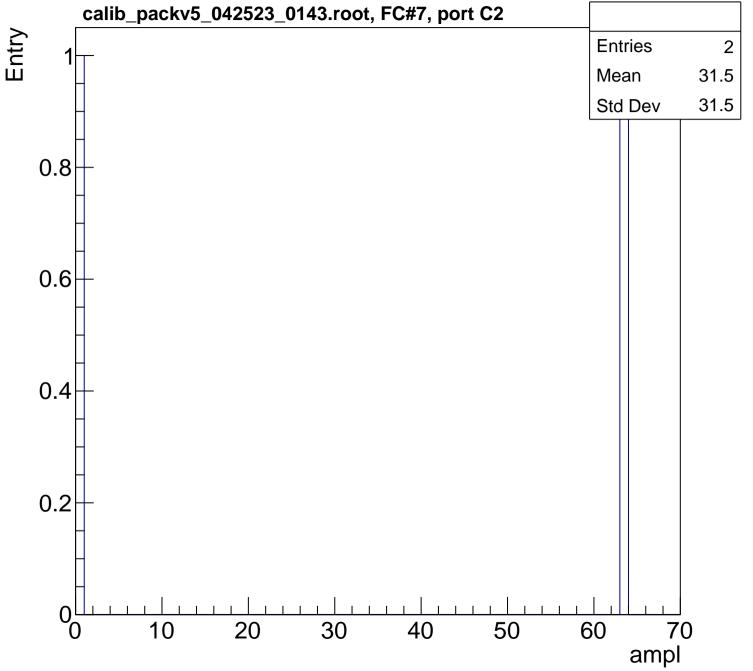


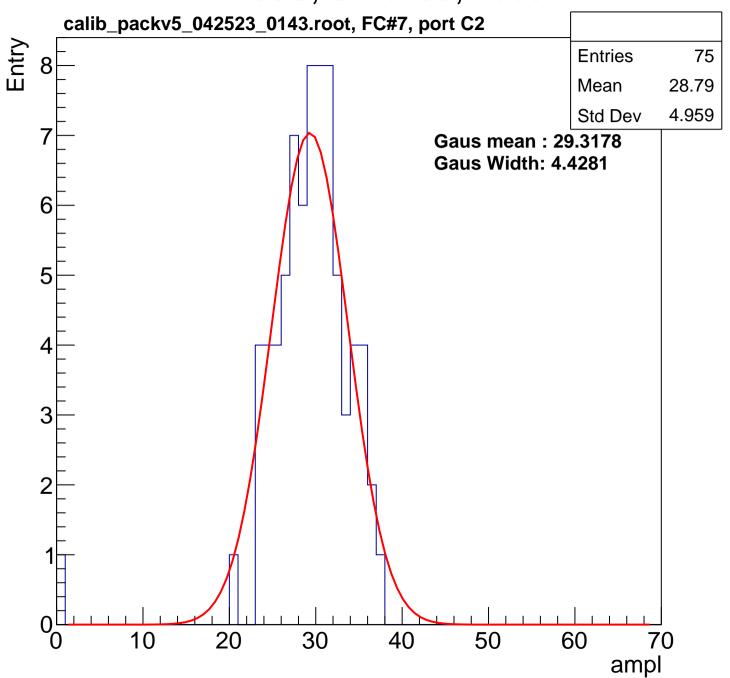


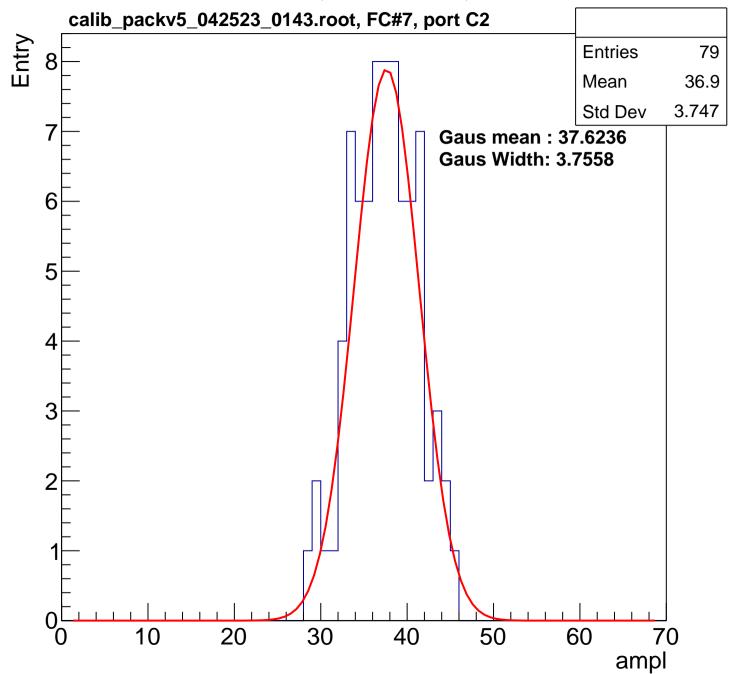


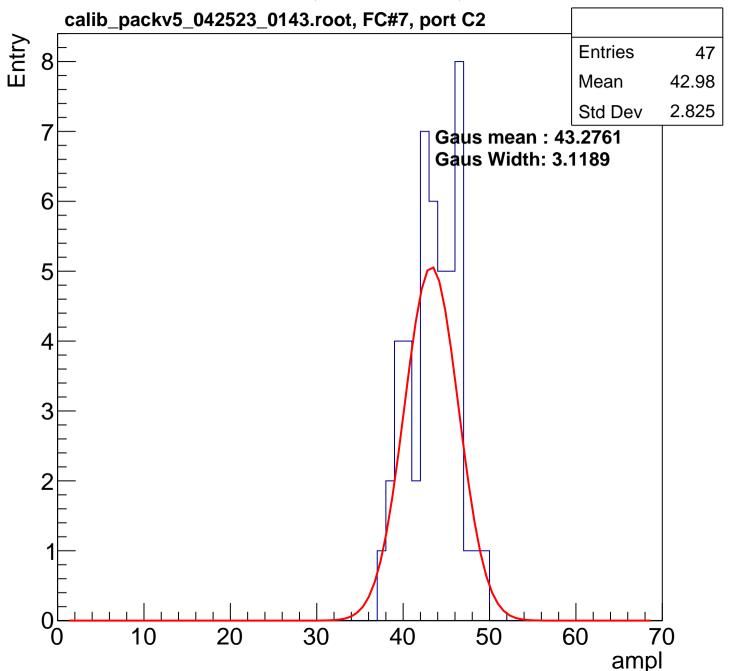


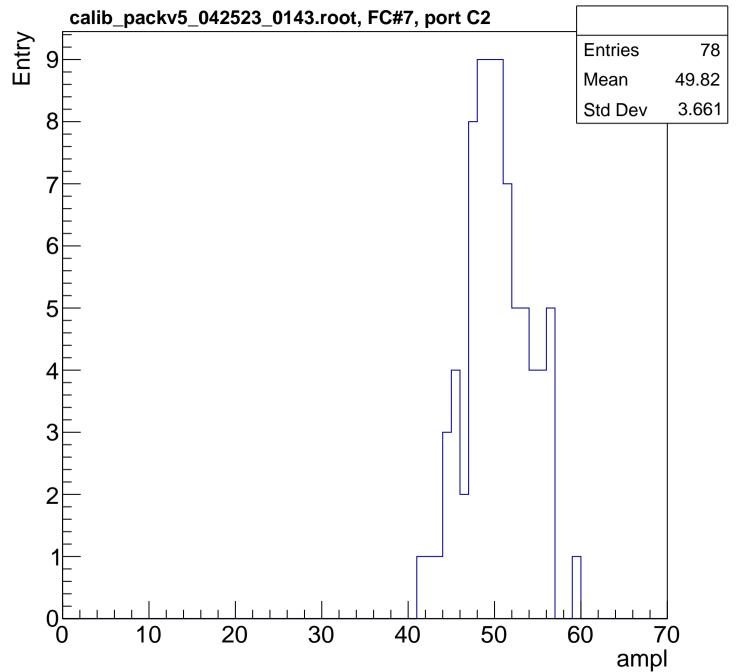


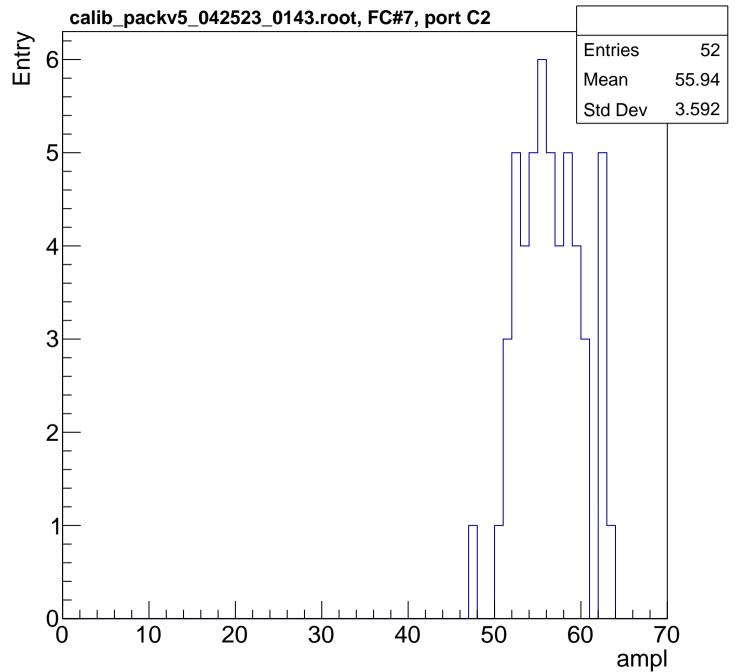


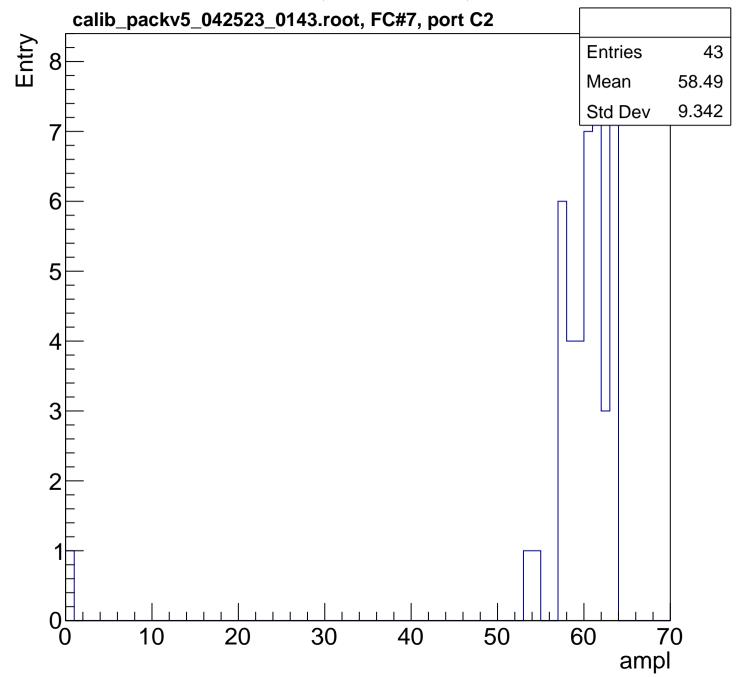


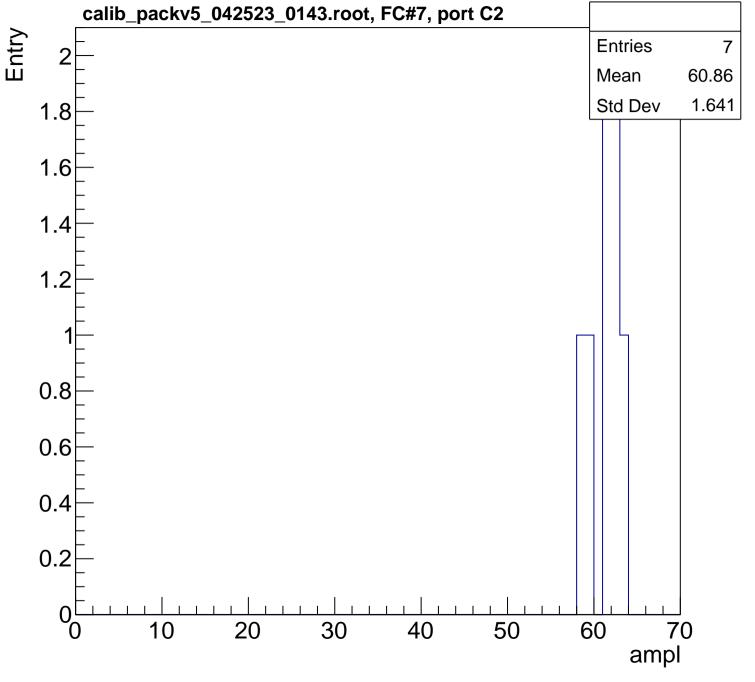


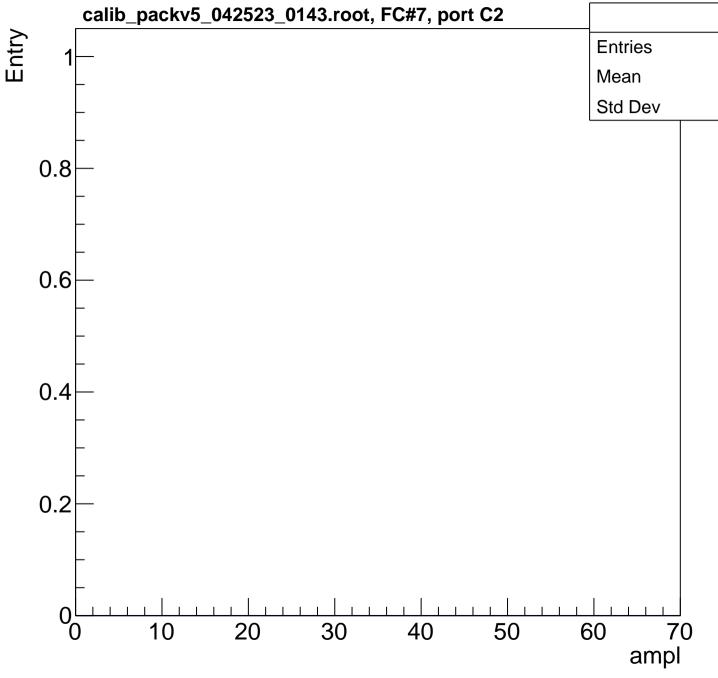


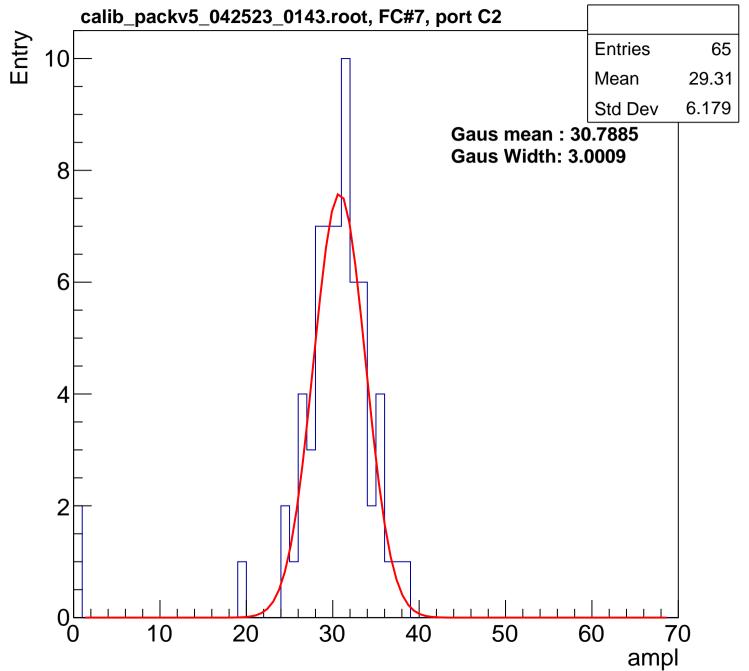


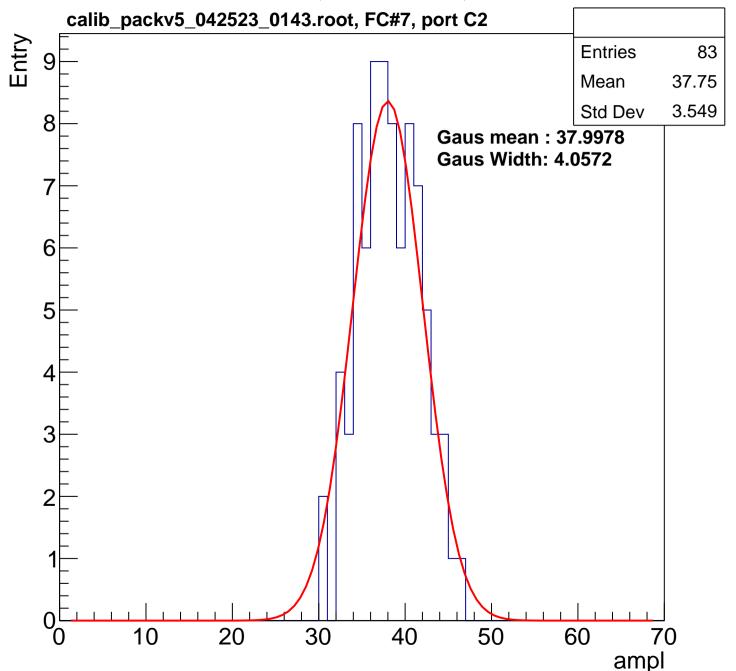


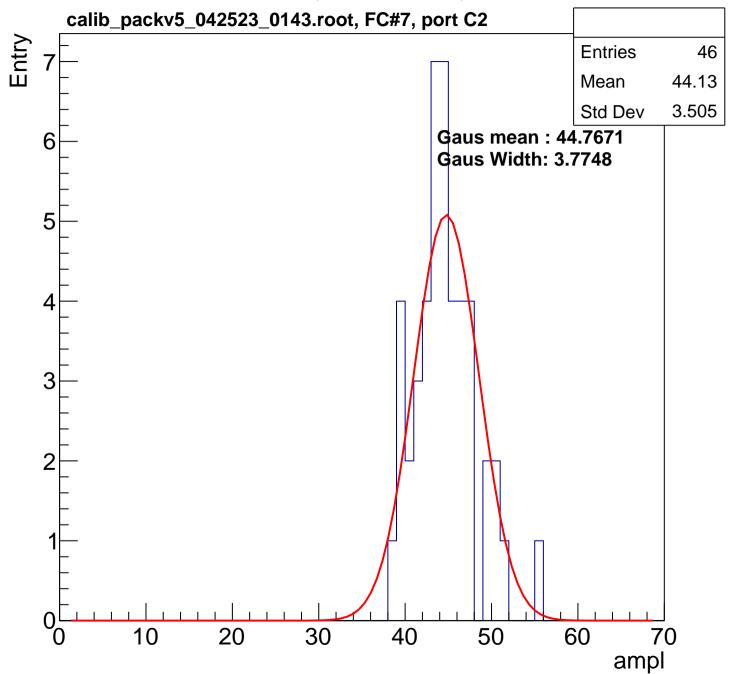


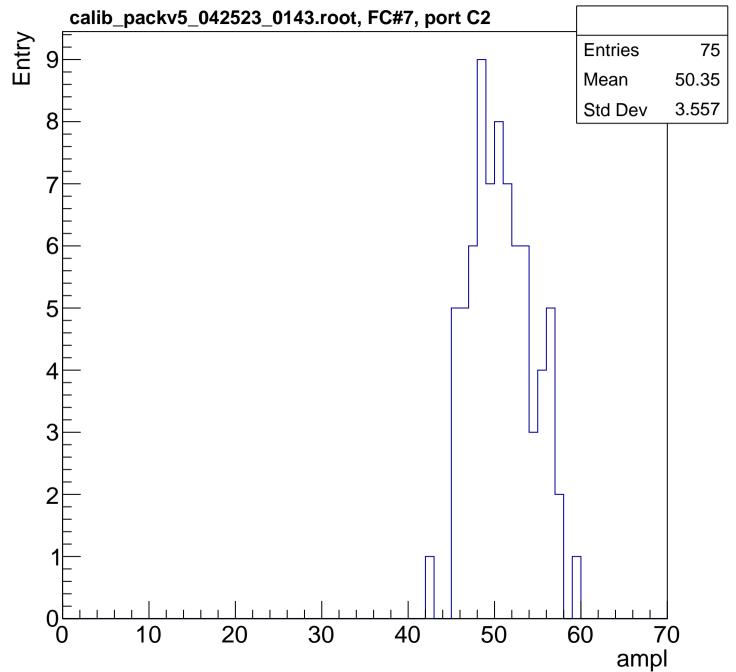


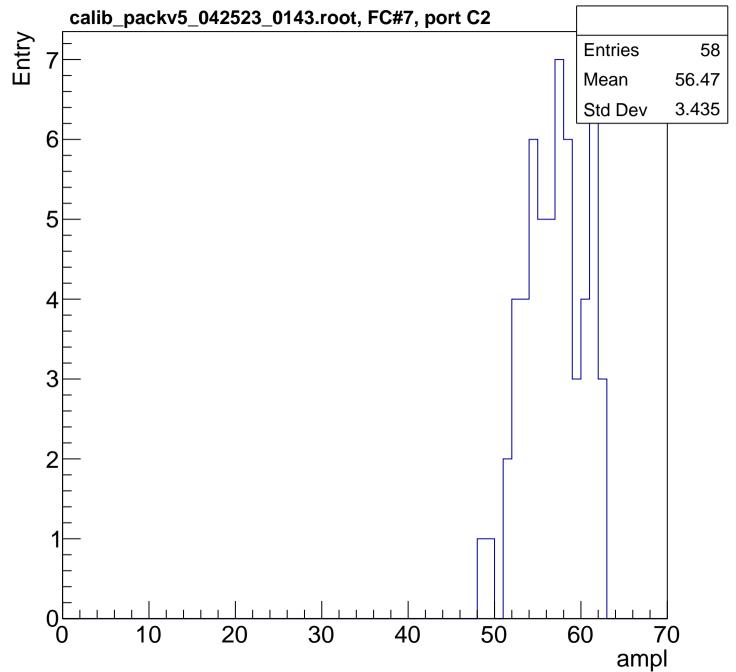


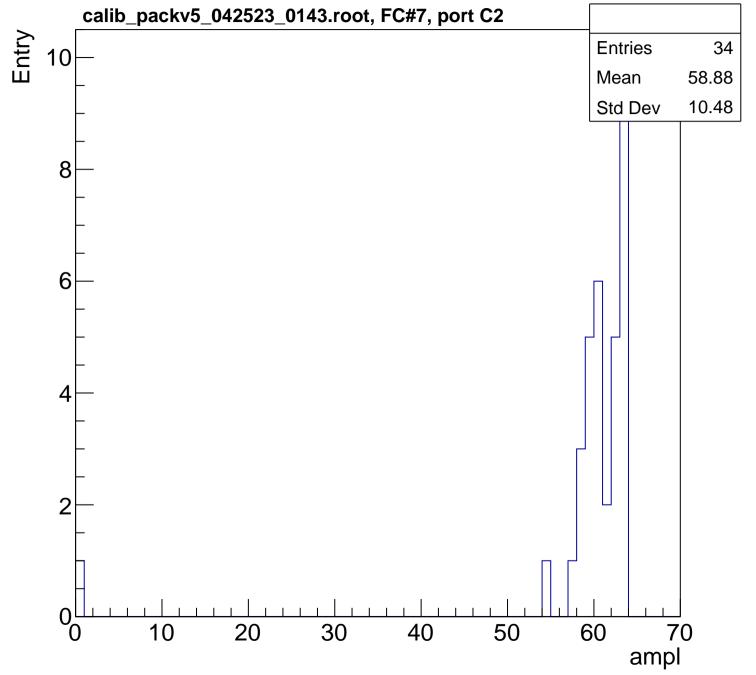


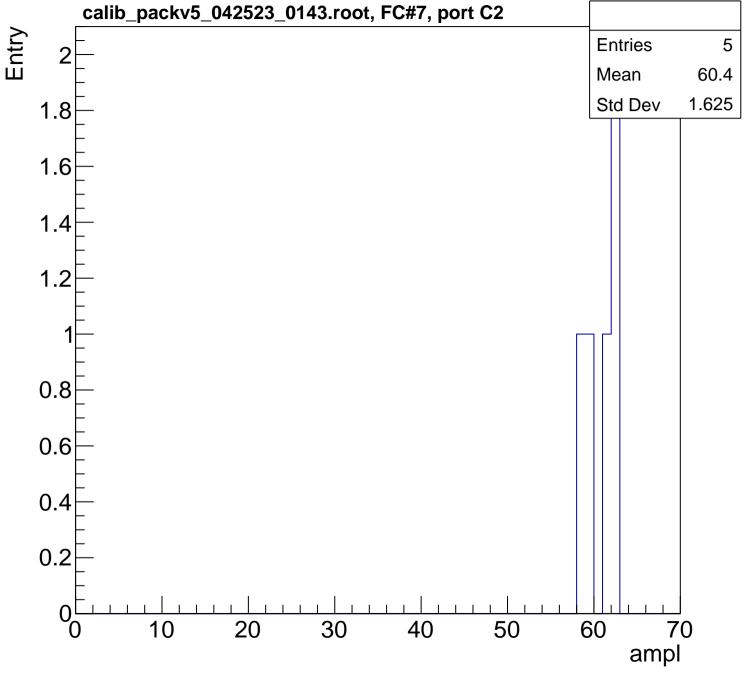


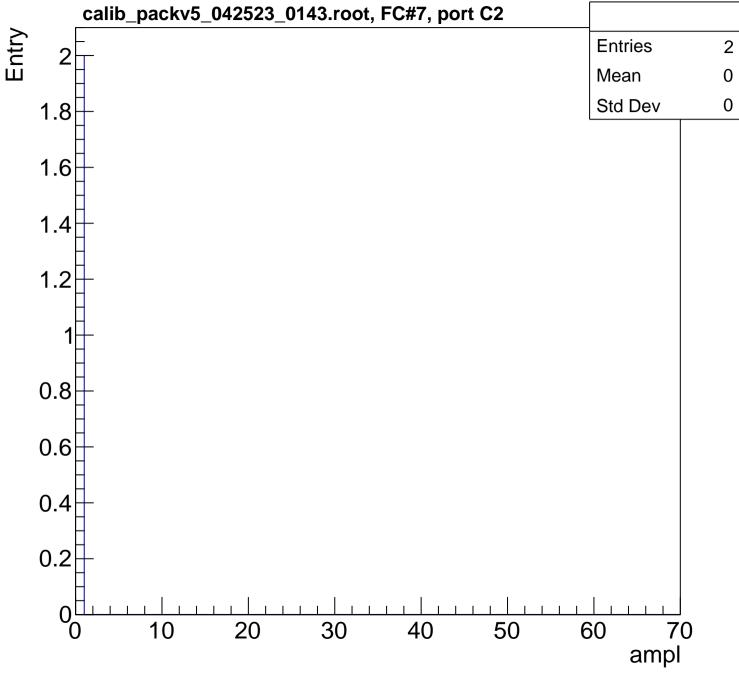


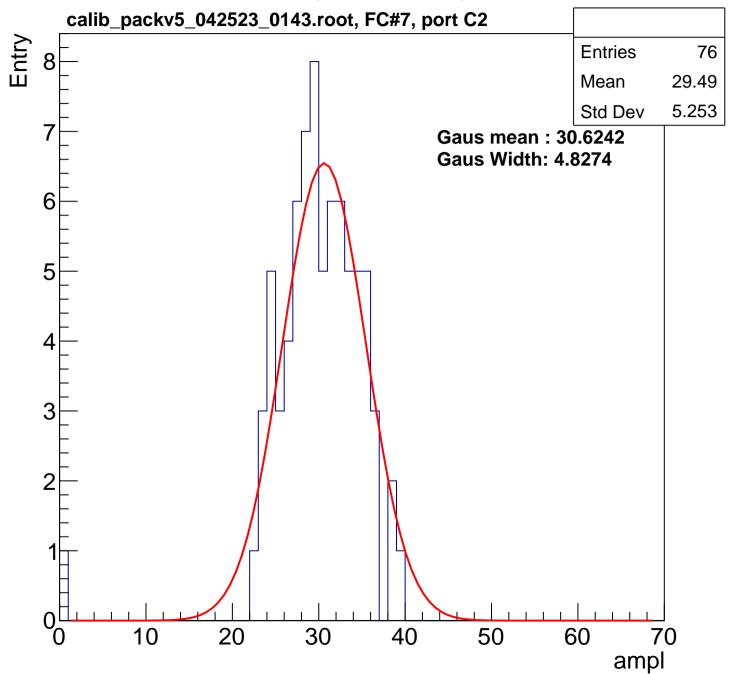


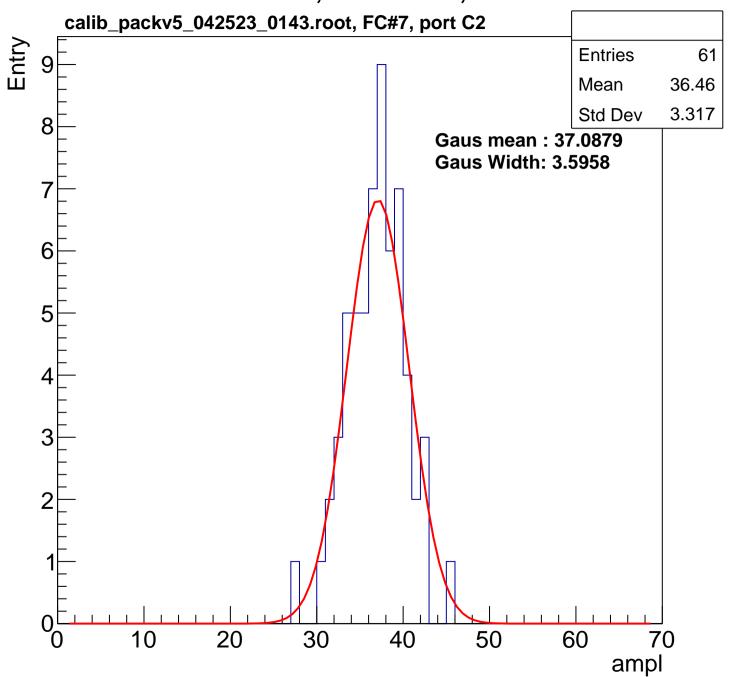


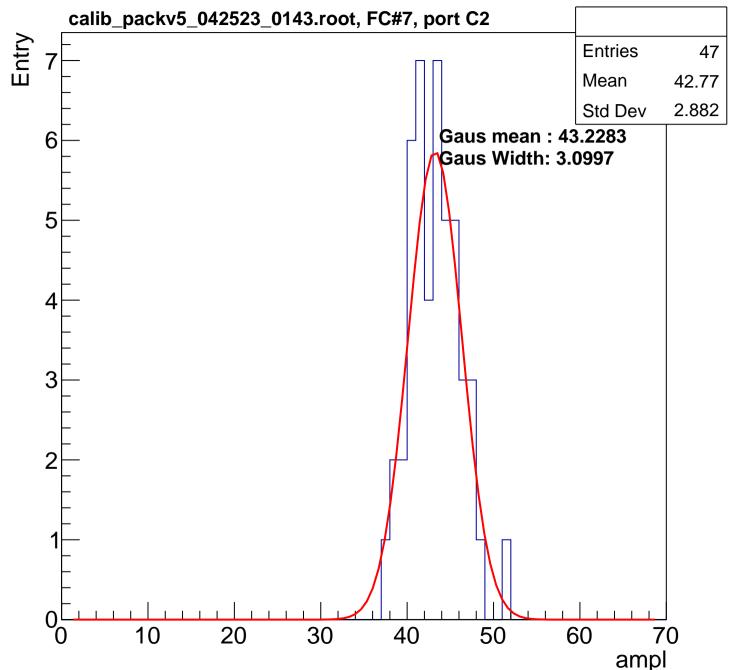


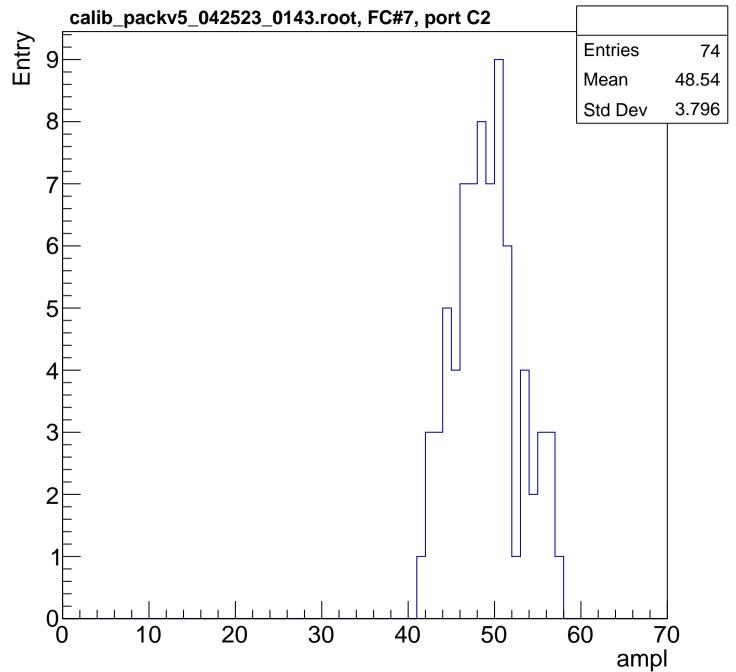


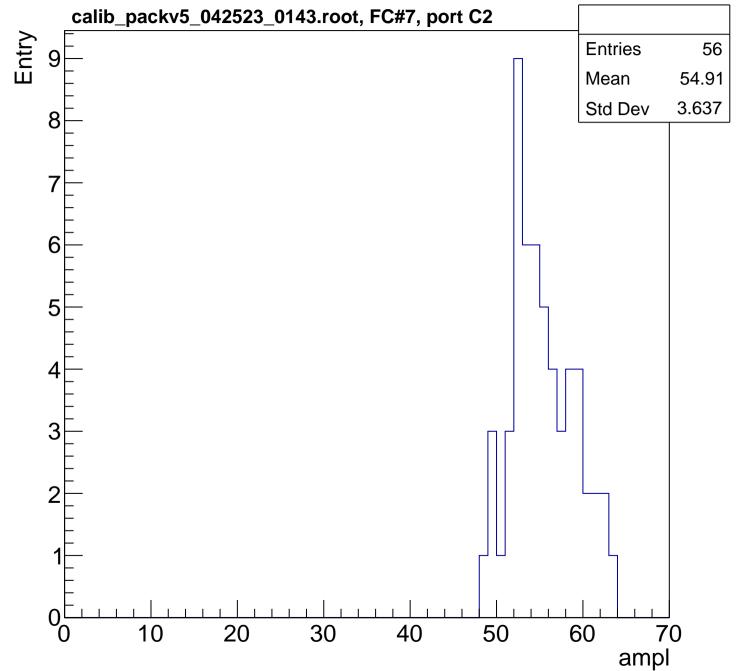


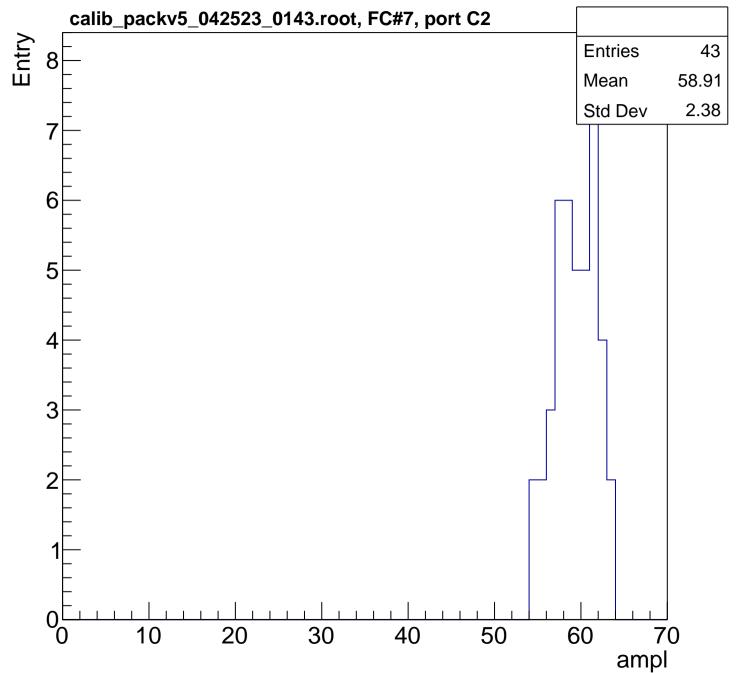


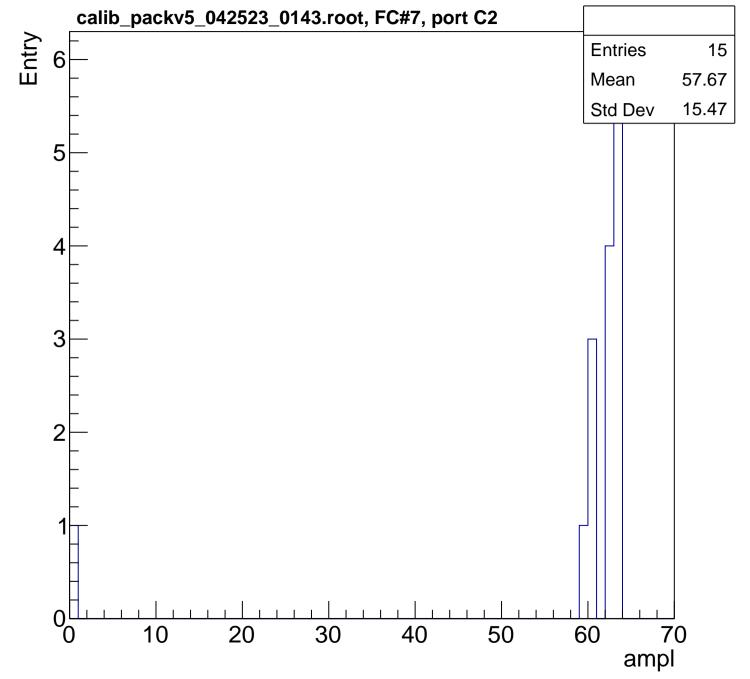


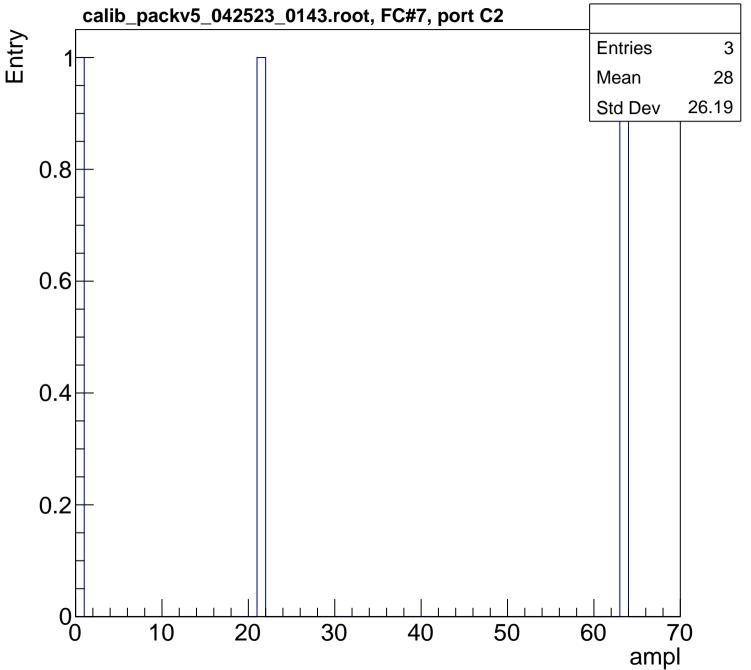


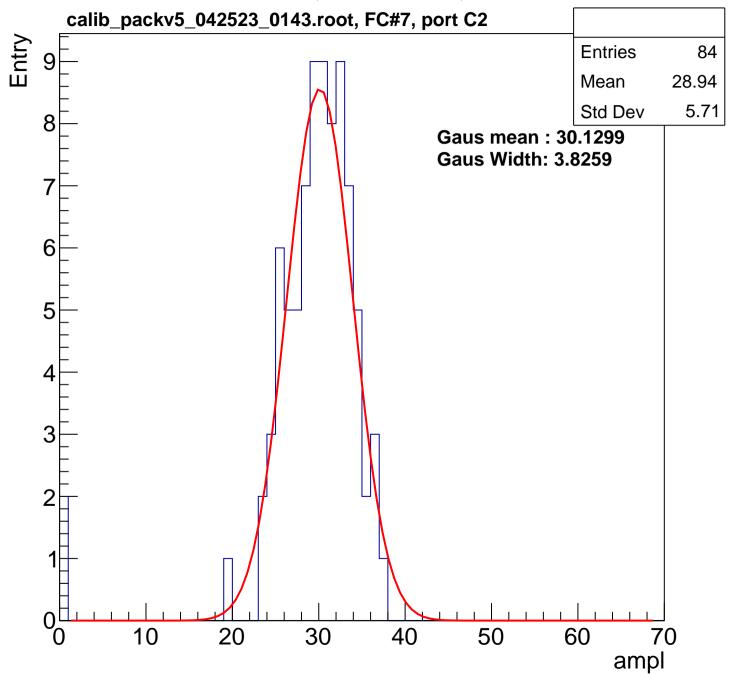


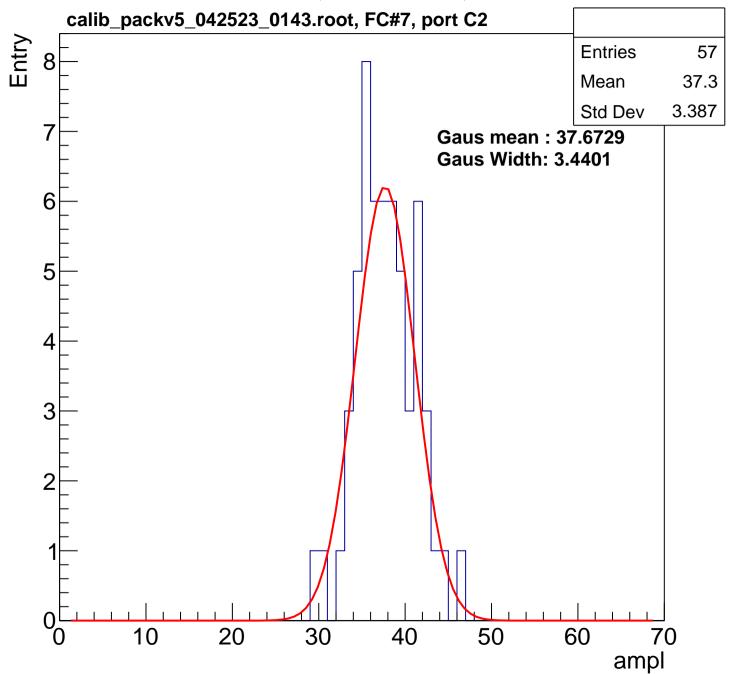


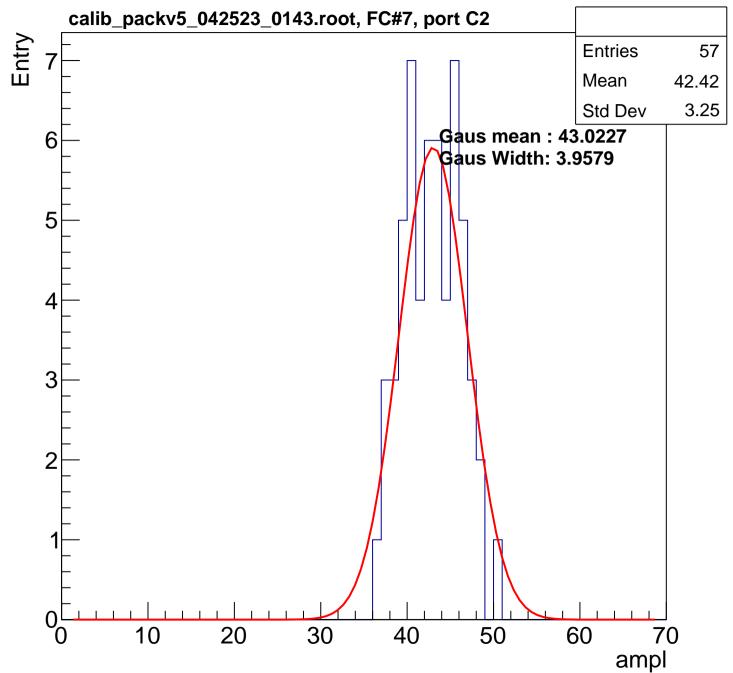


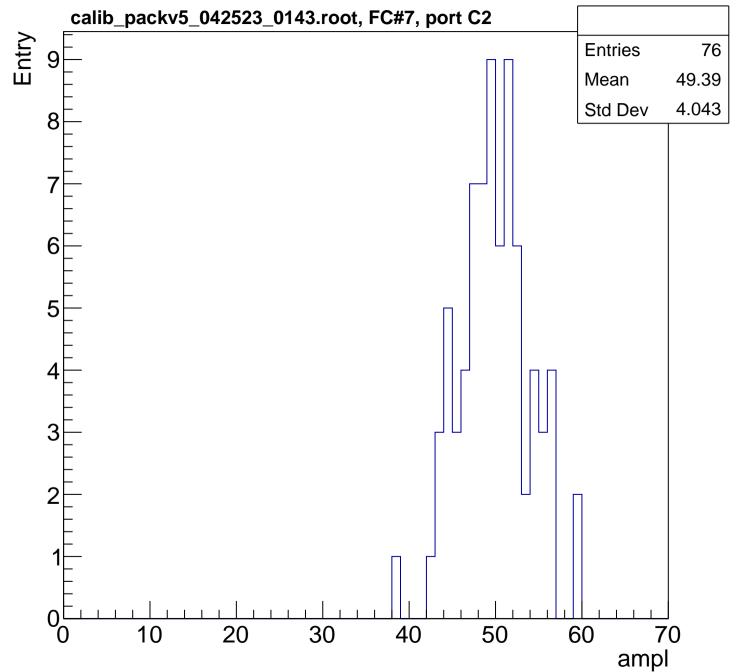


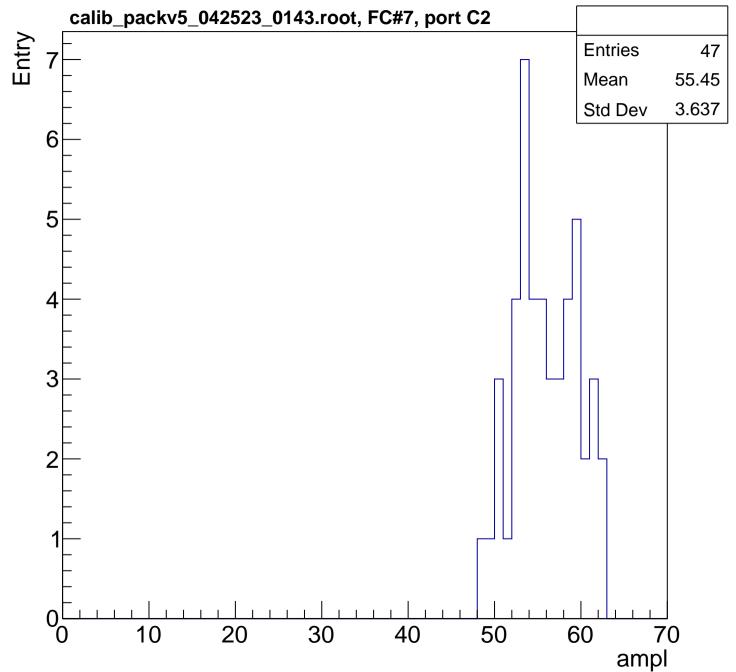


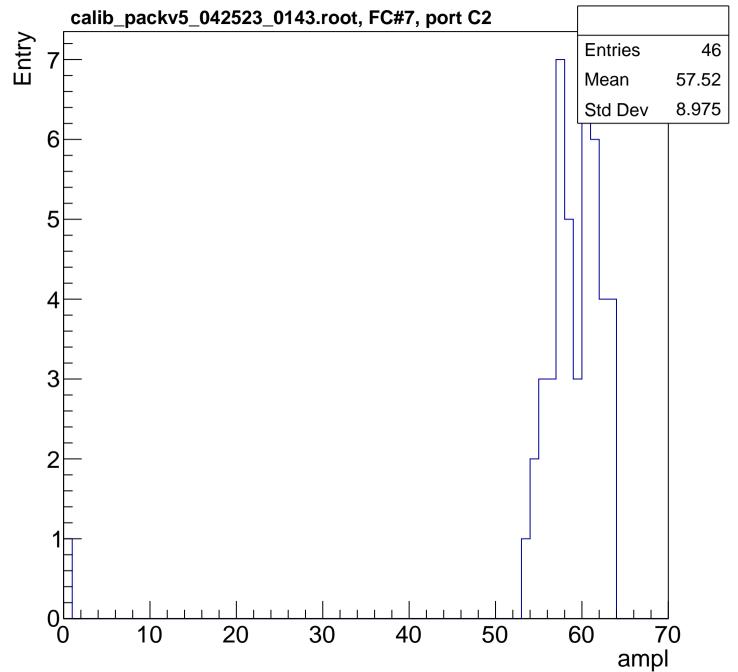


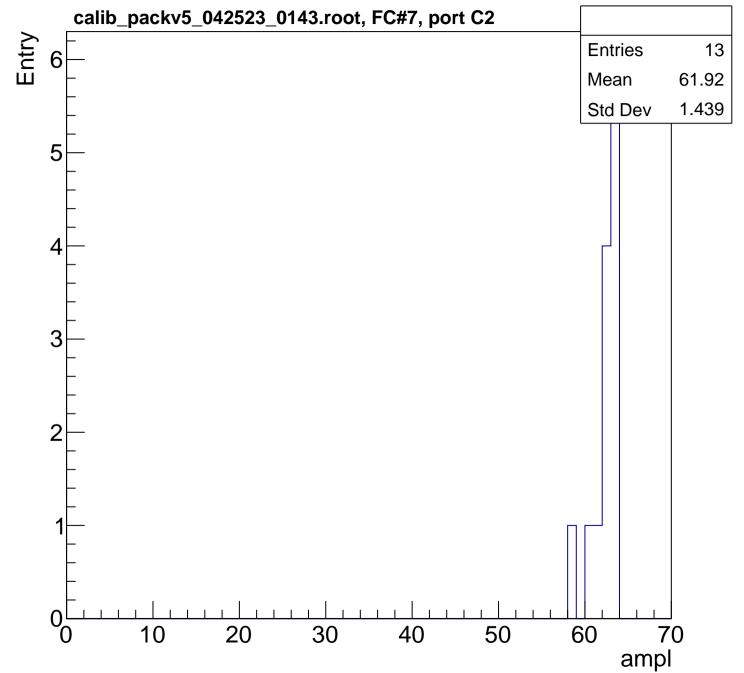












B1L103S, U4-ch58, adc7 calib_packv5_042523_0143.root, FC#7, port C2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30

40

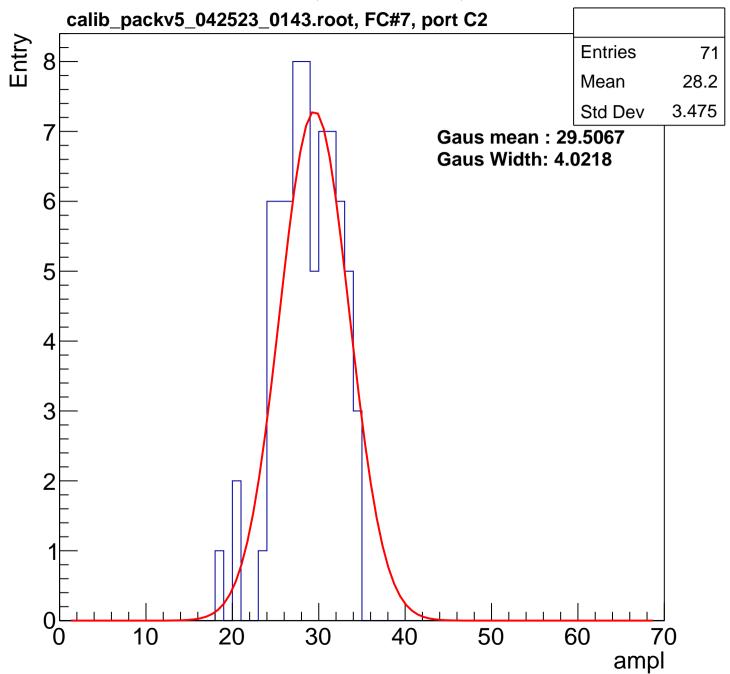
50

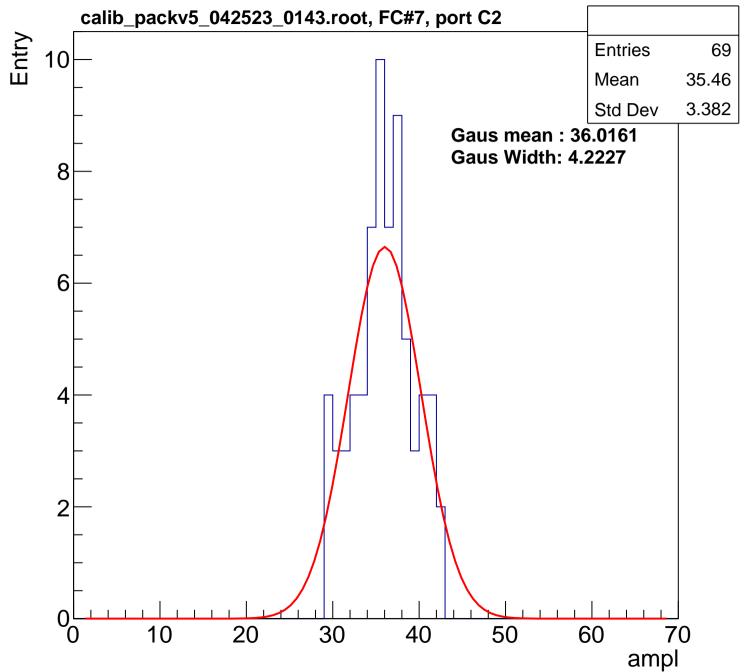
60

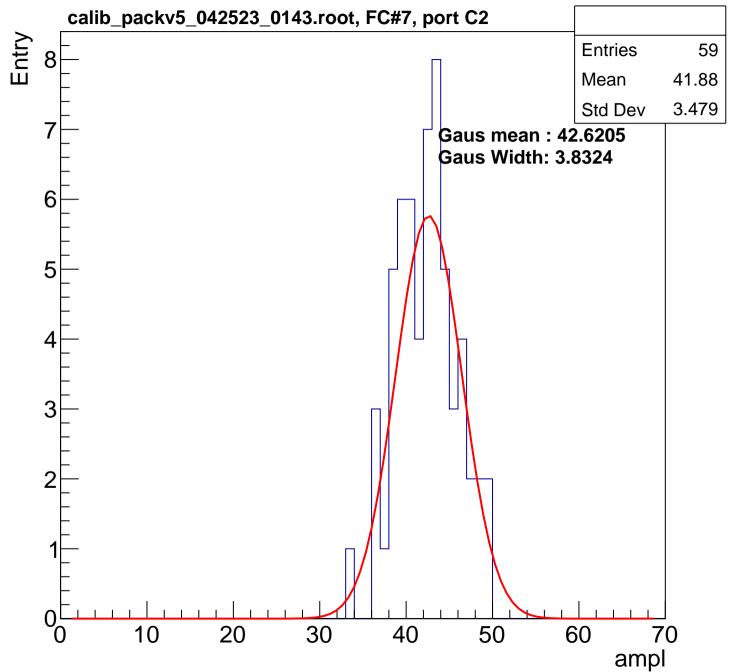
70

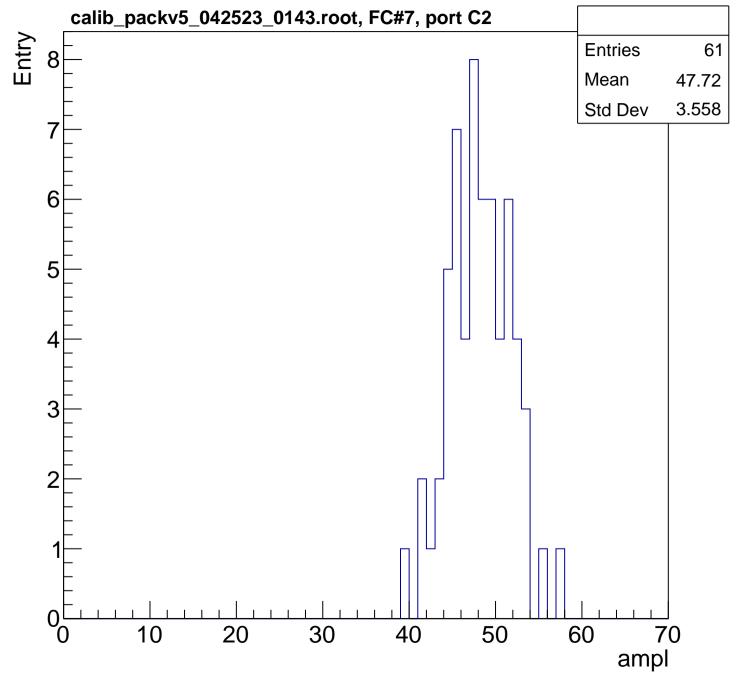
ampl

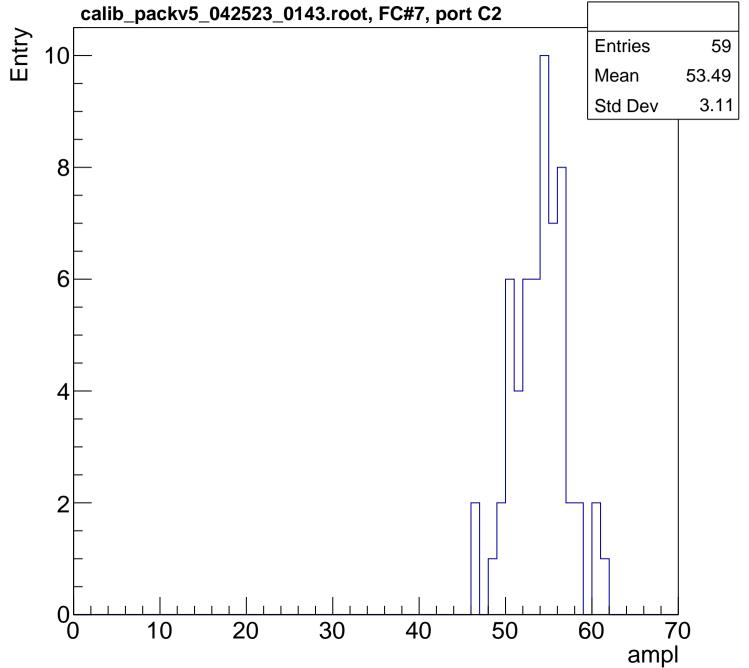
20

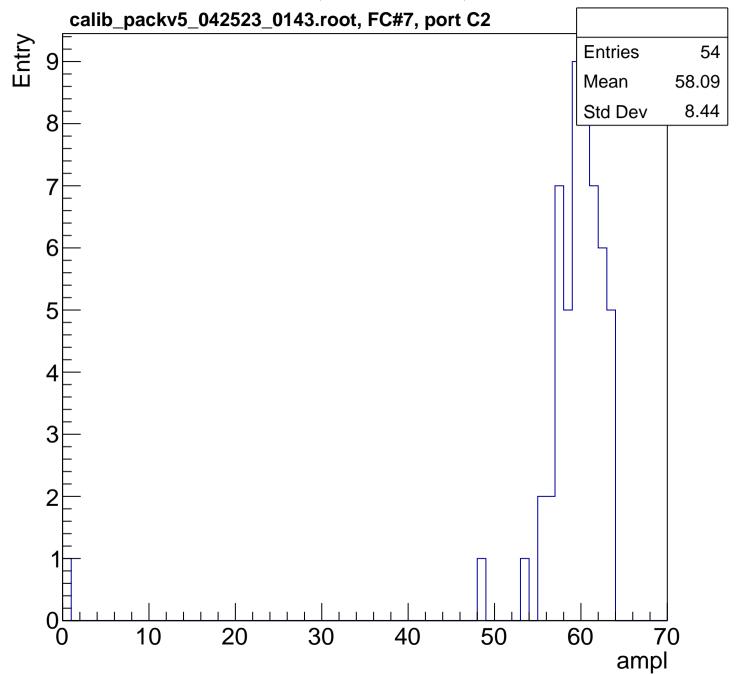


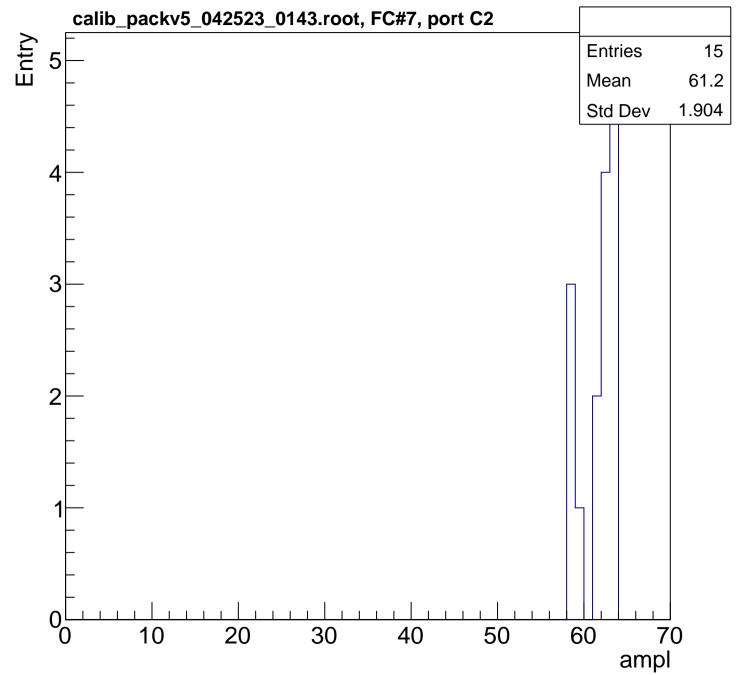


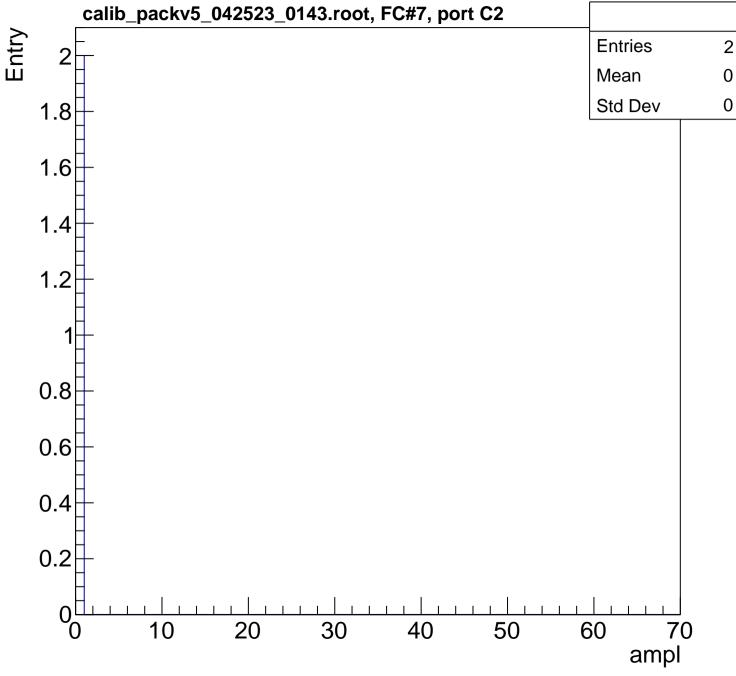


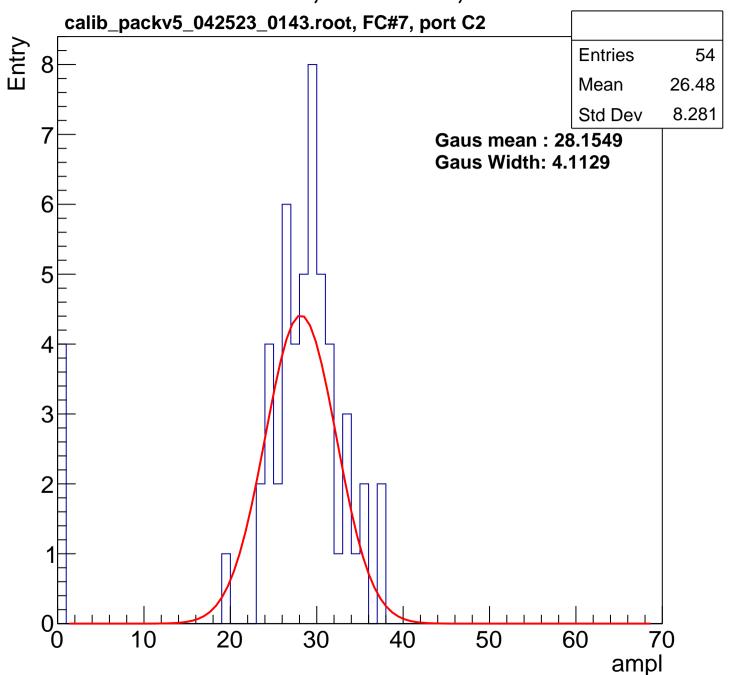


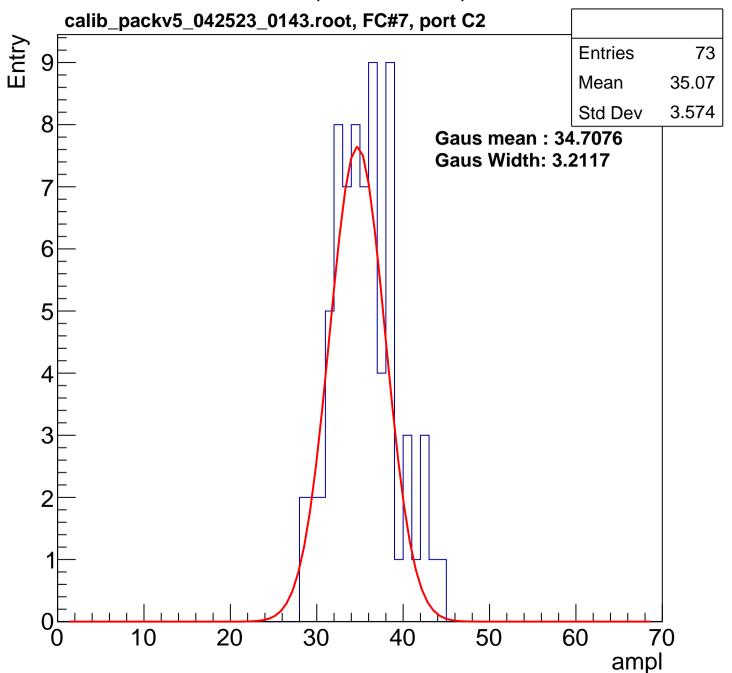


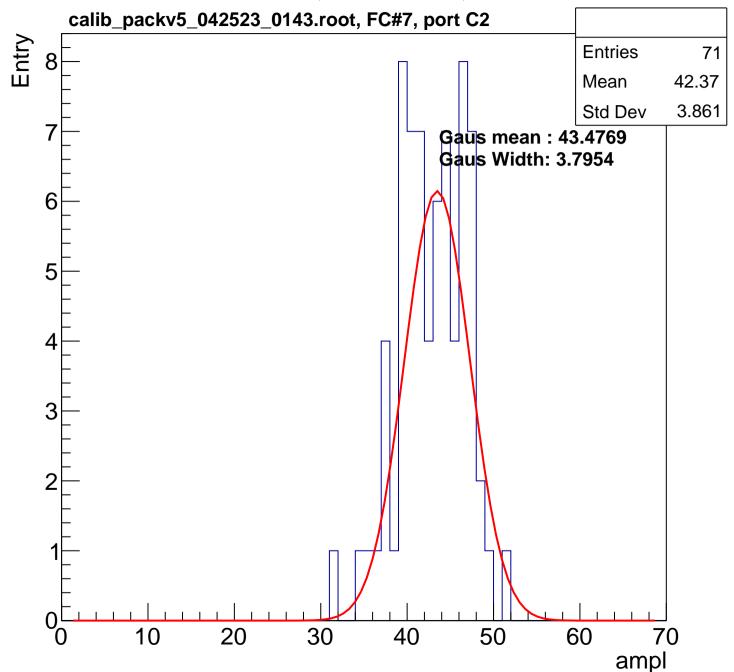


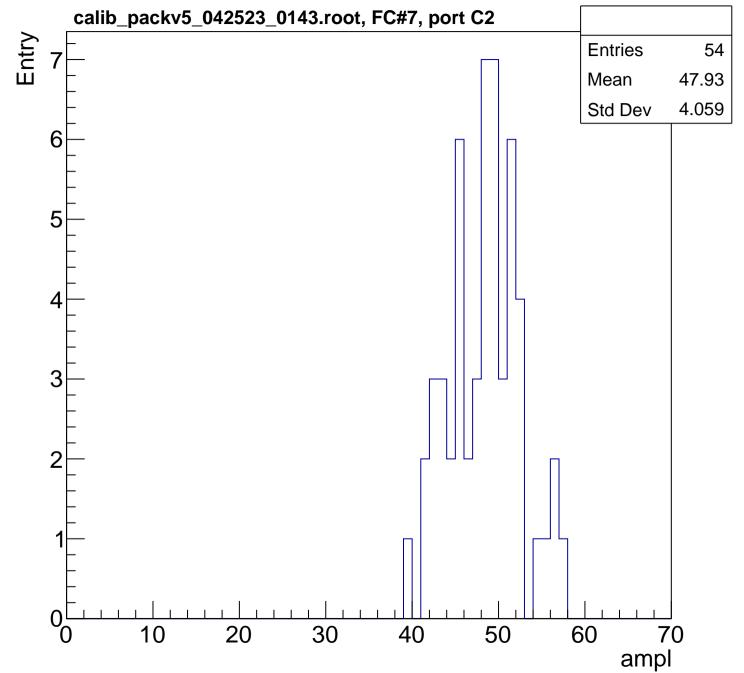


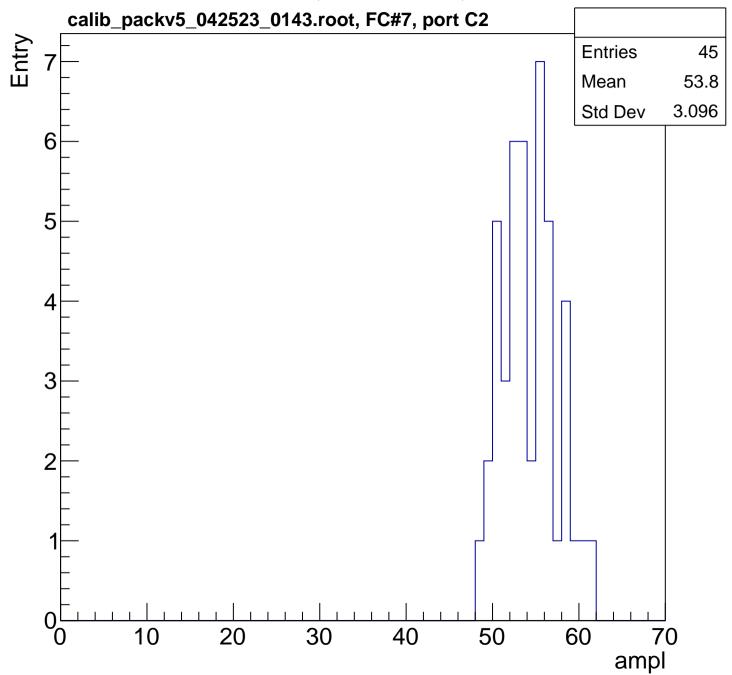


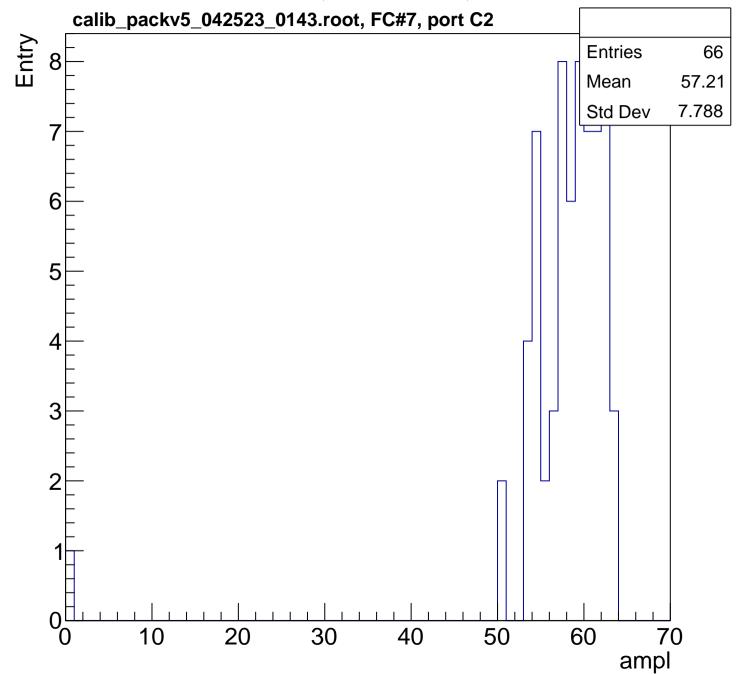


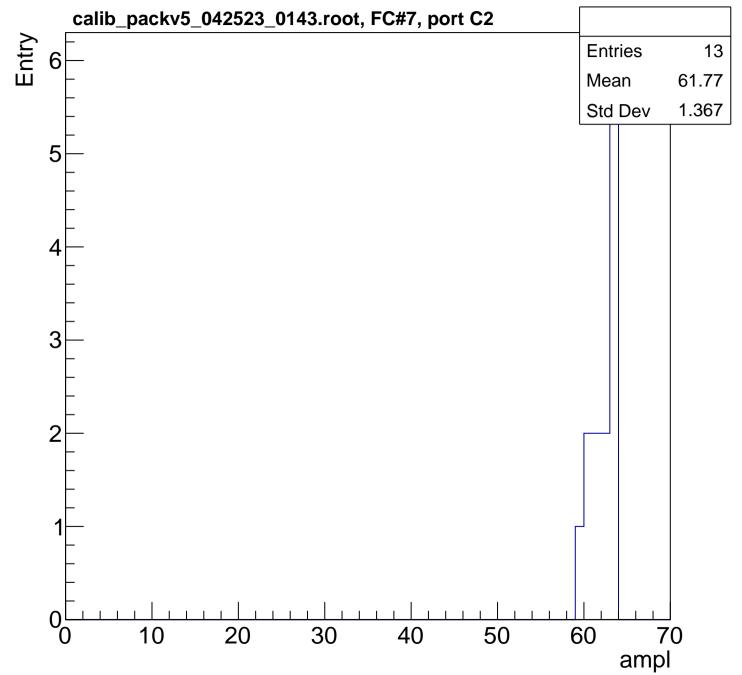


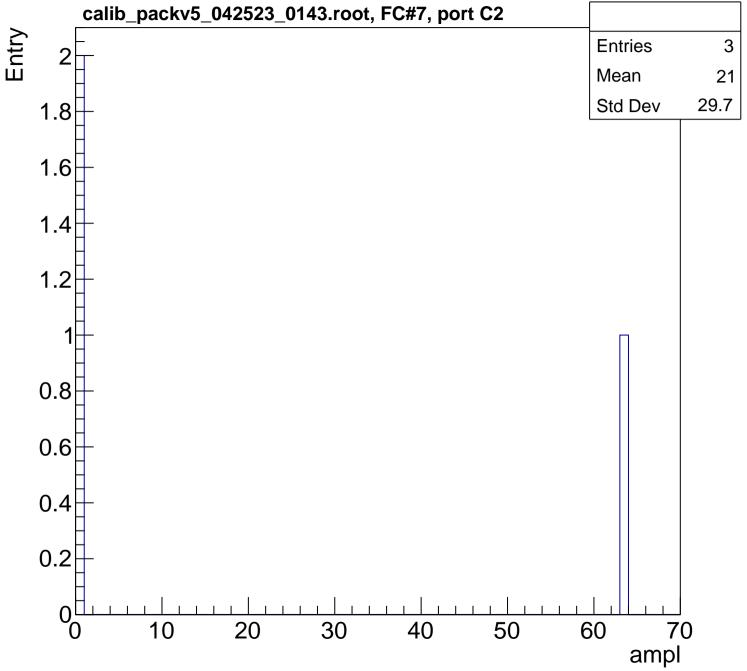


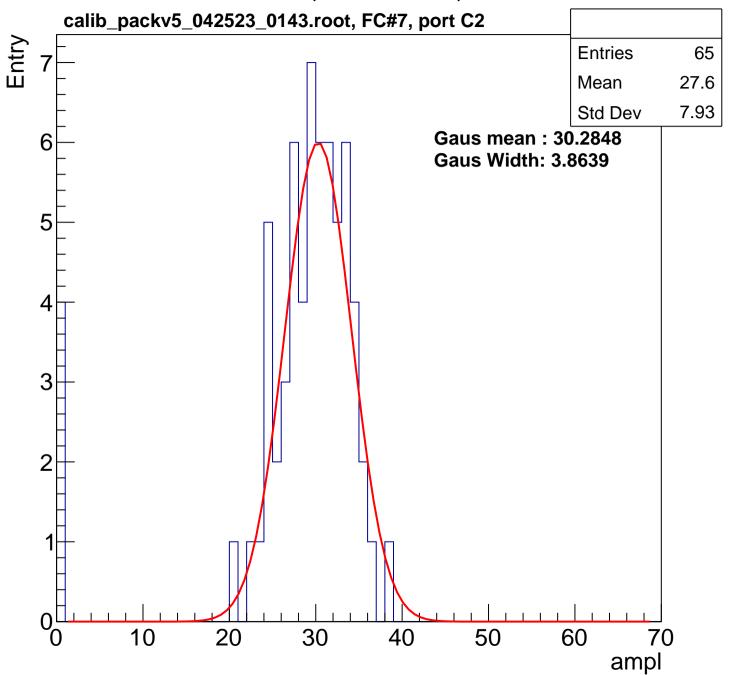


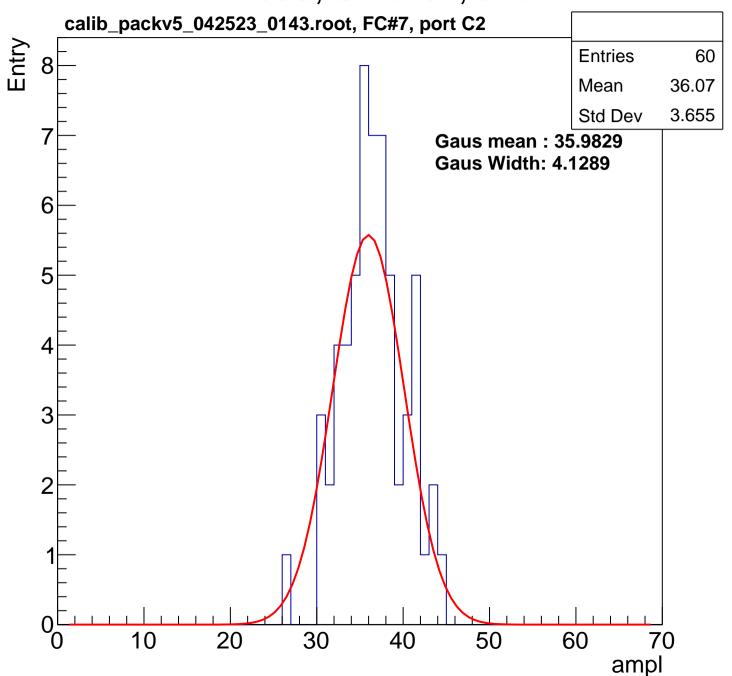


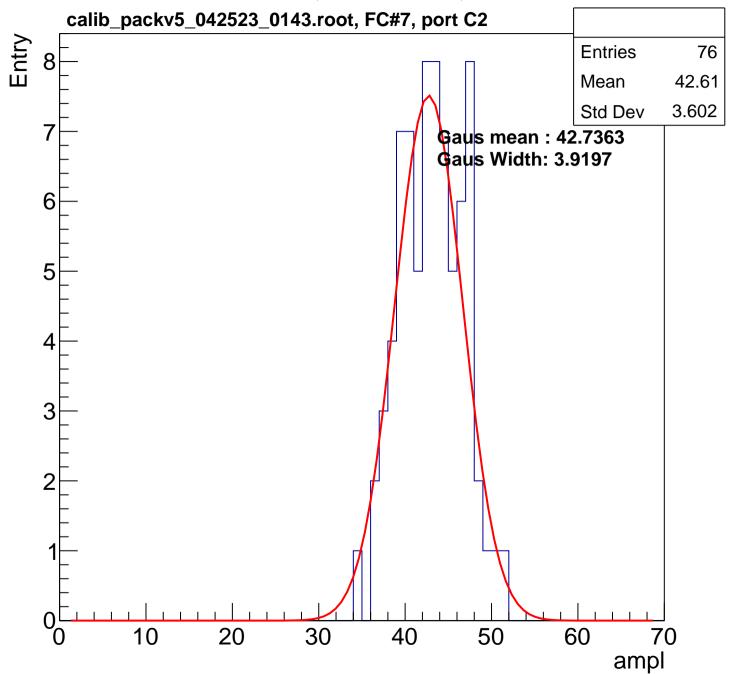


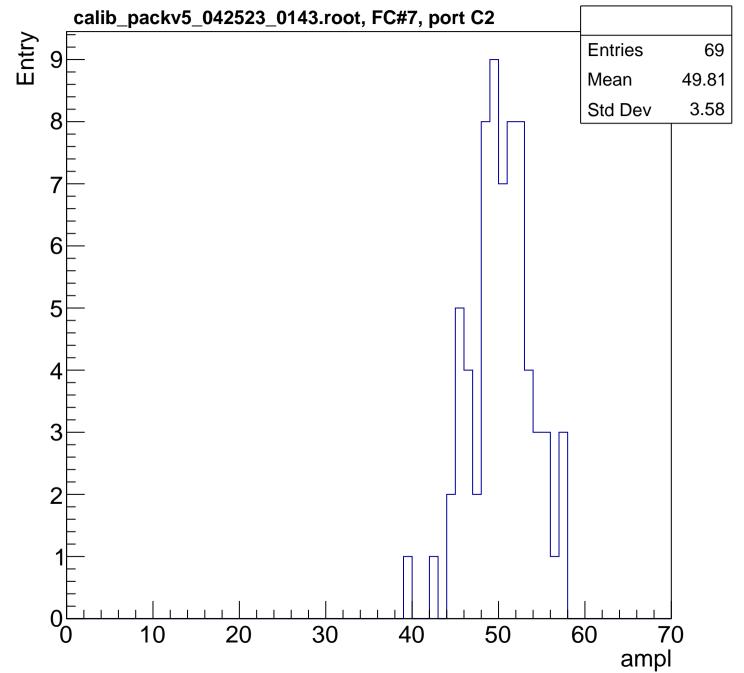


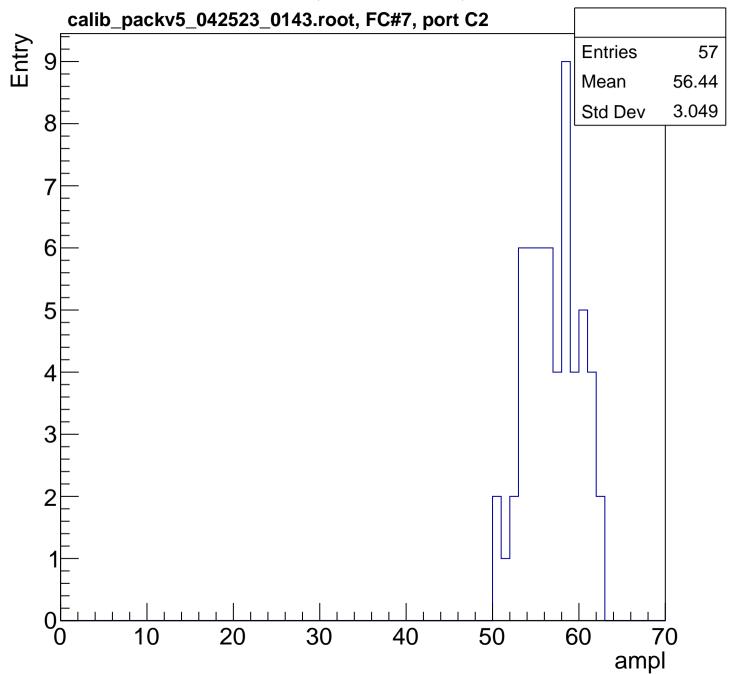


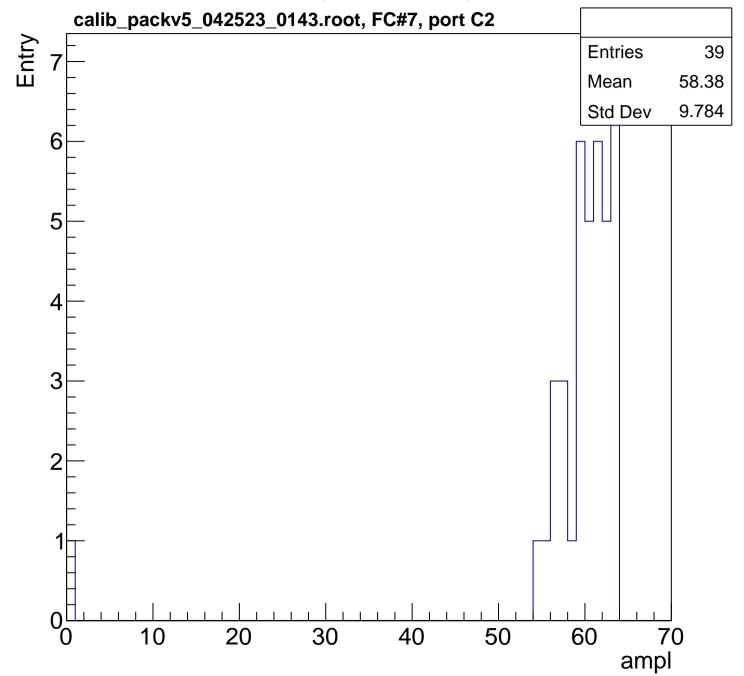


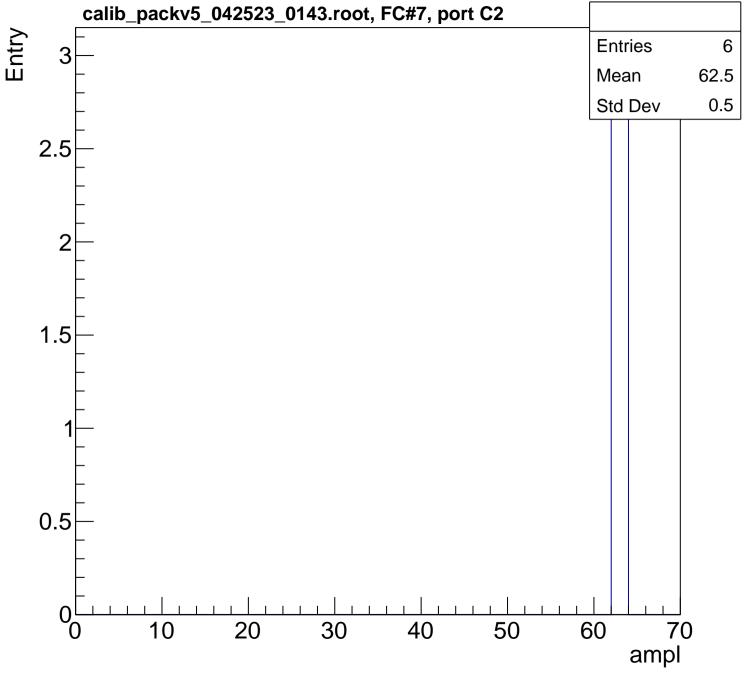


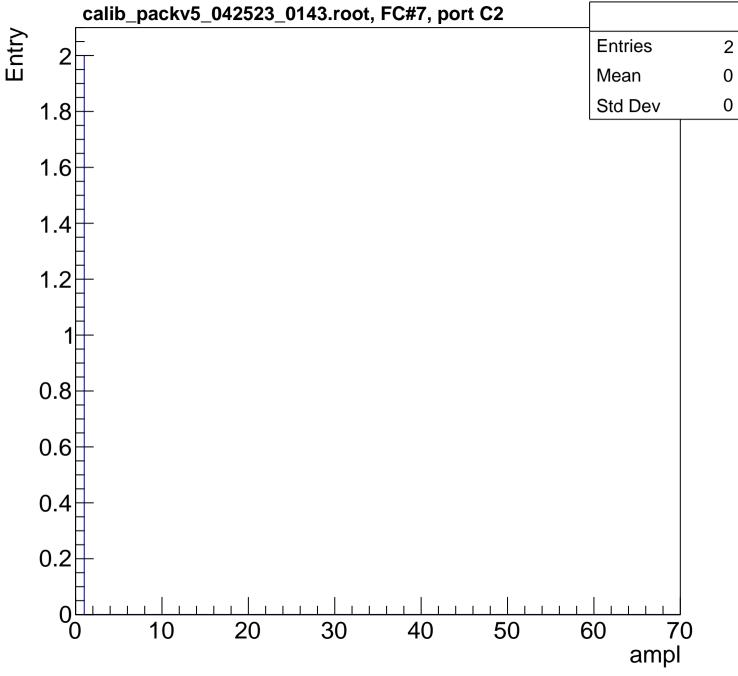


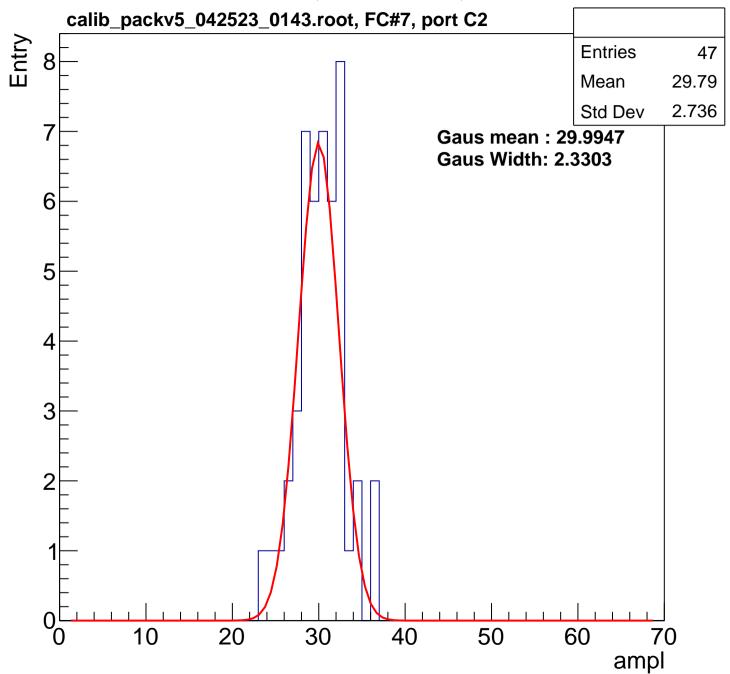


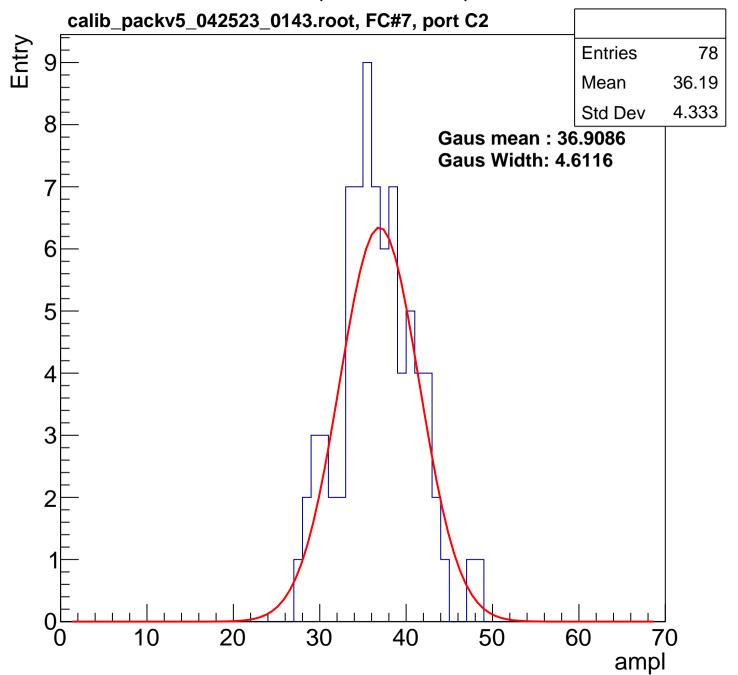


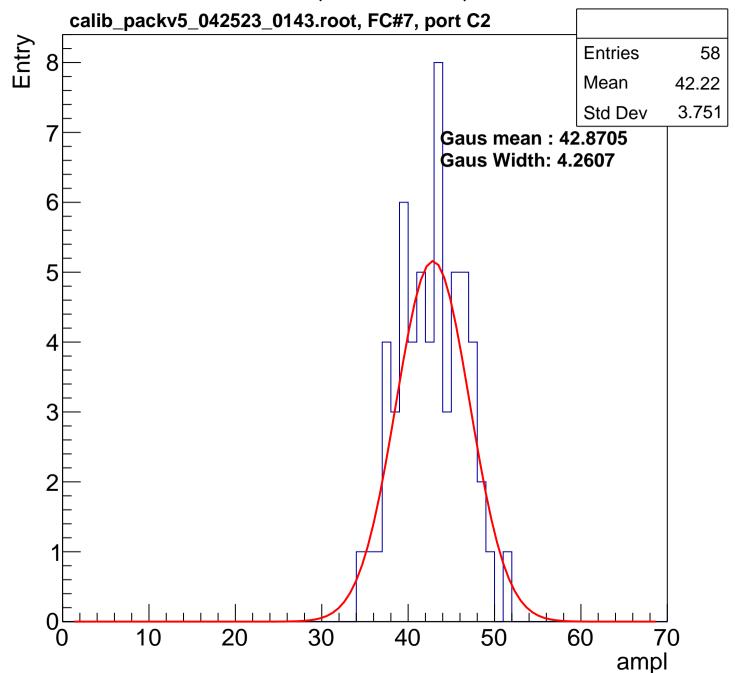


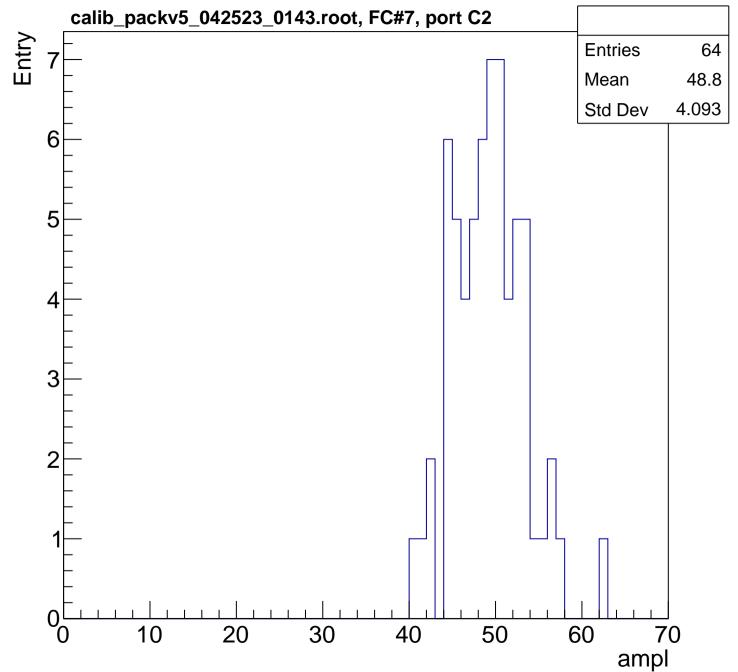


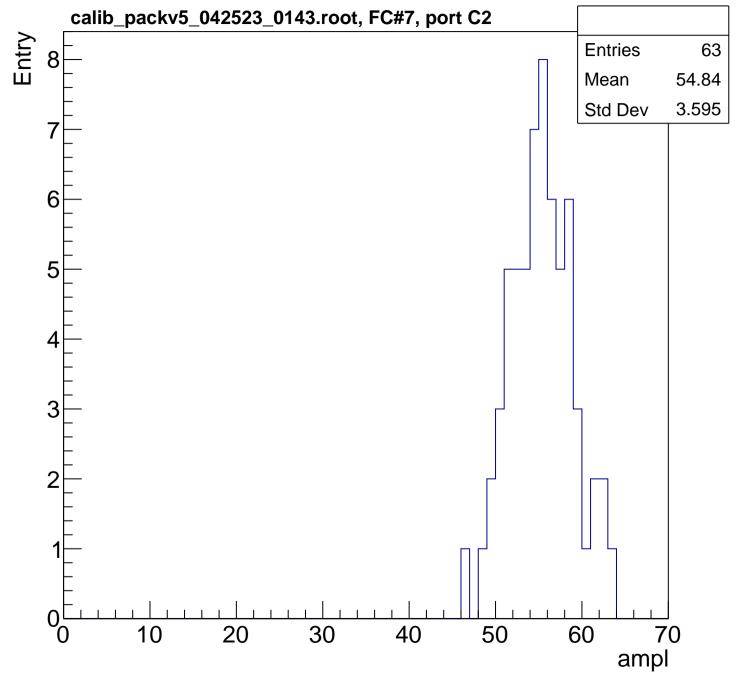


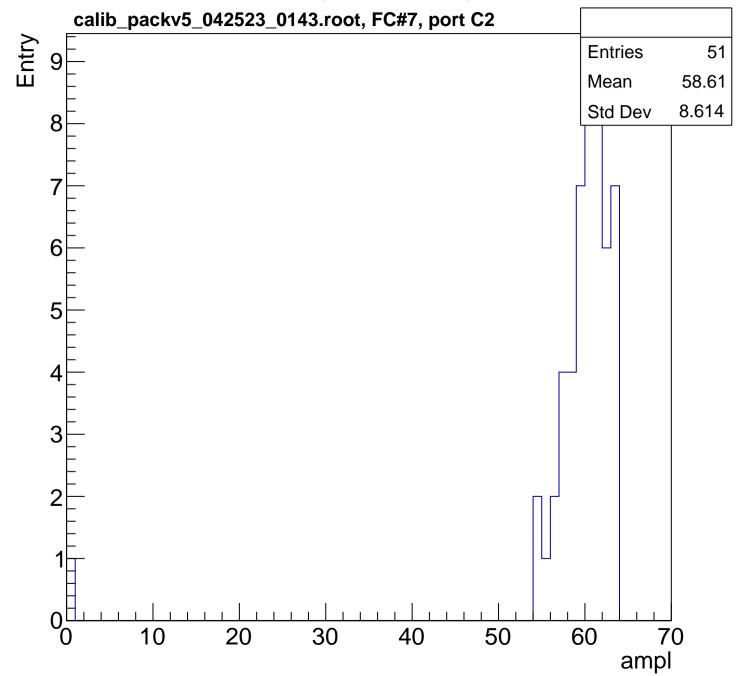


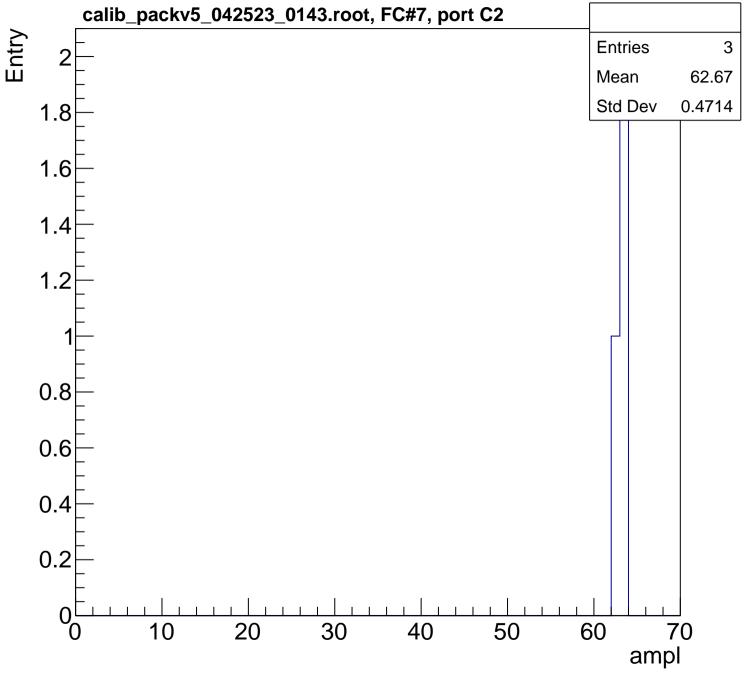


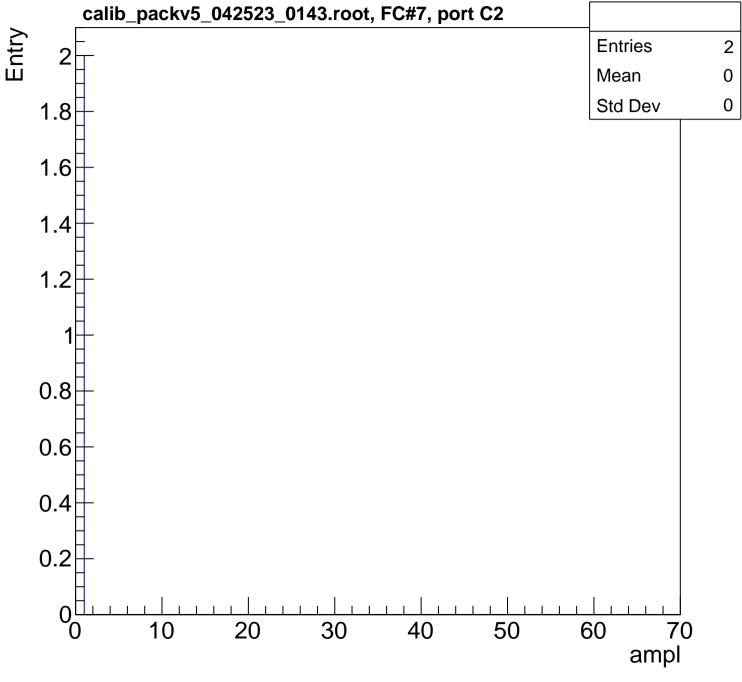


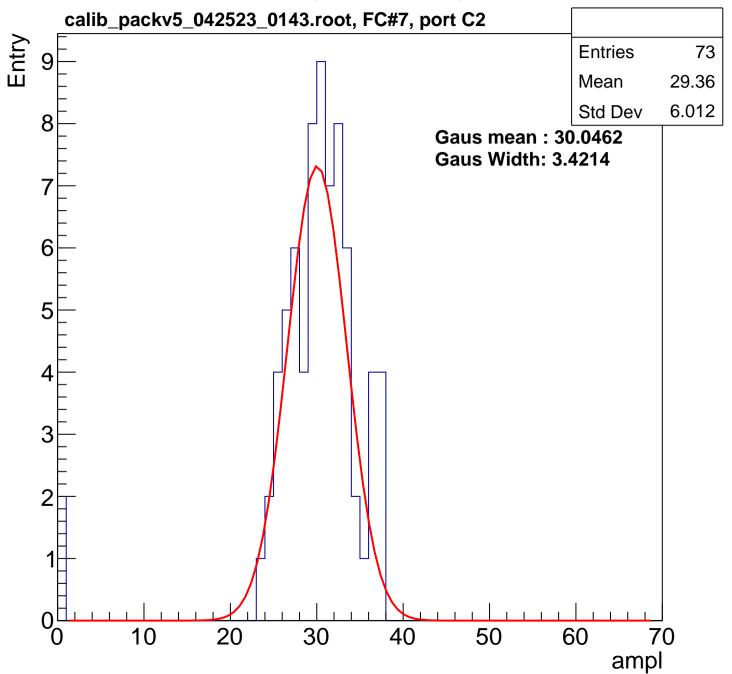


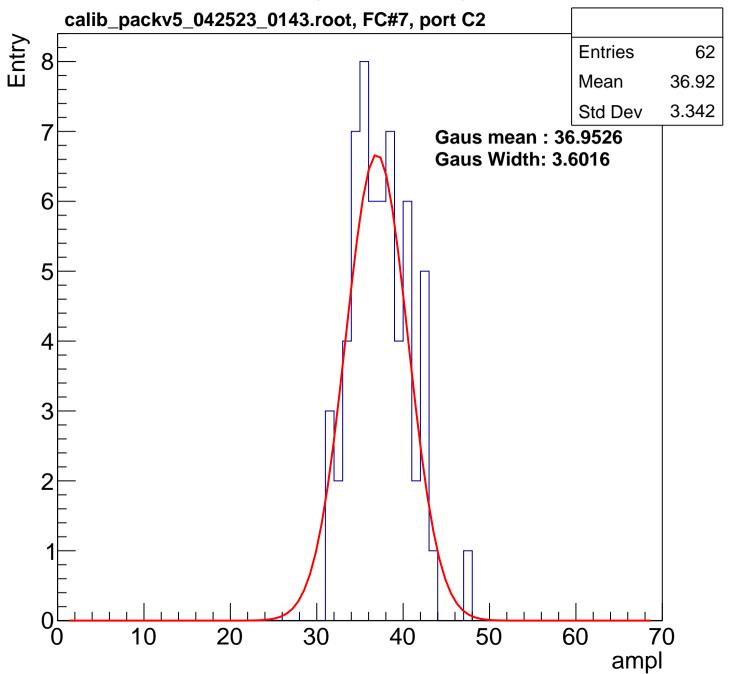


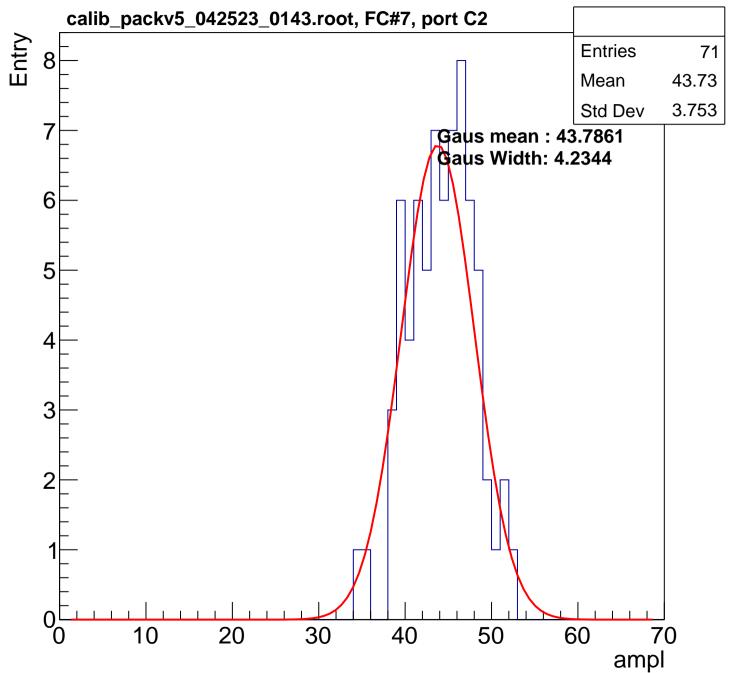


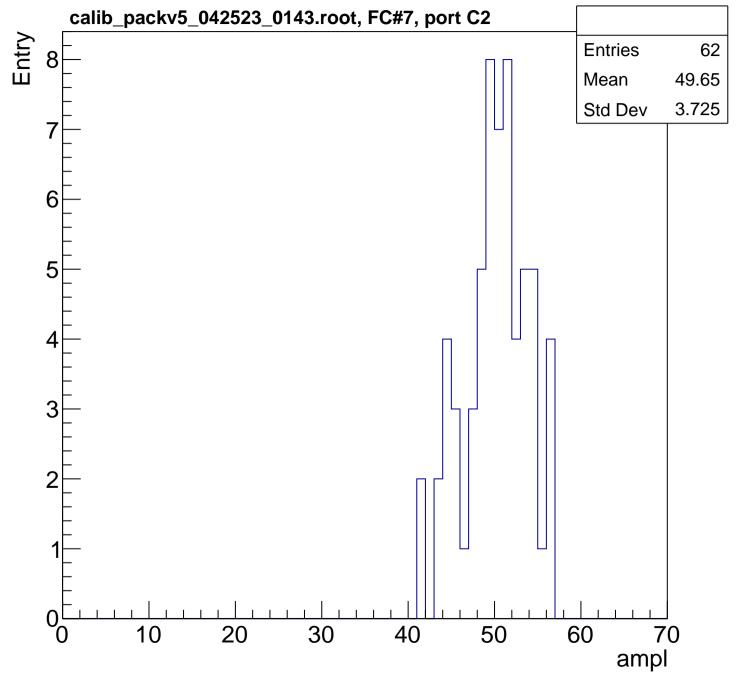


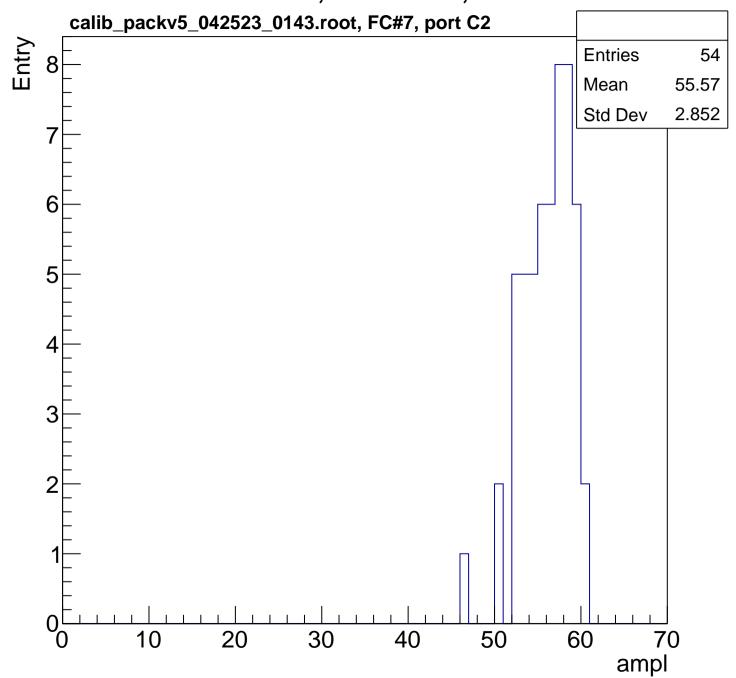


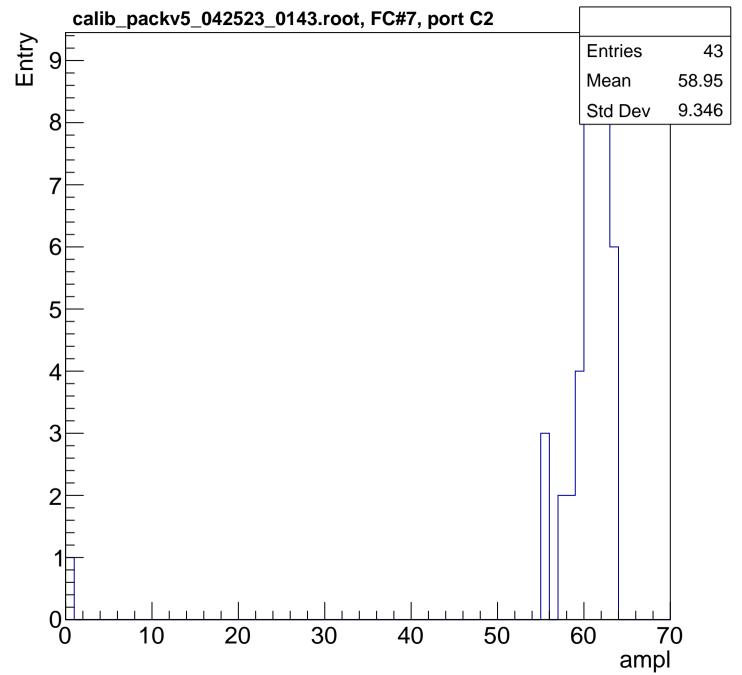


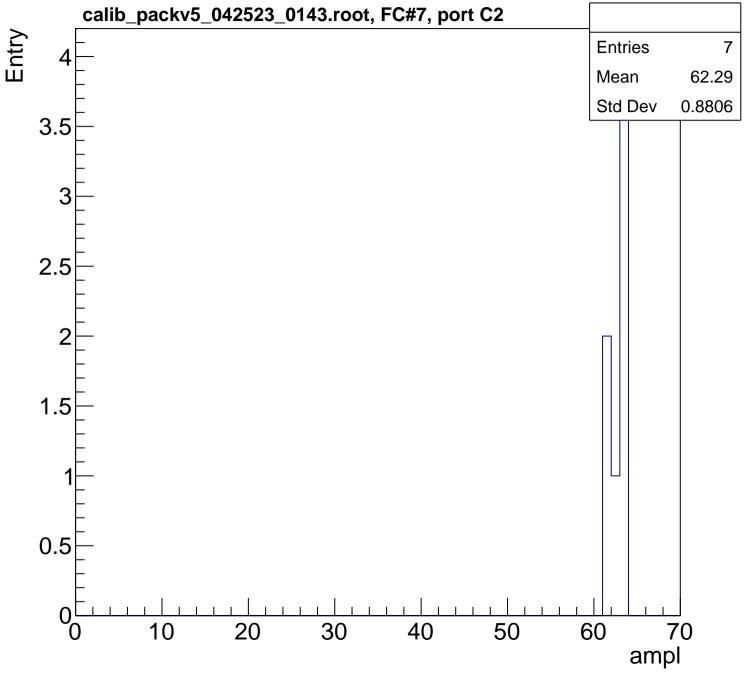




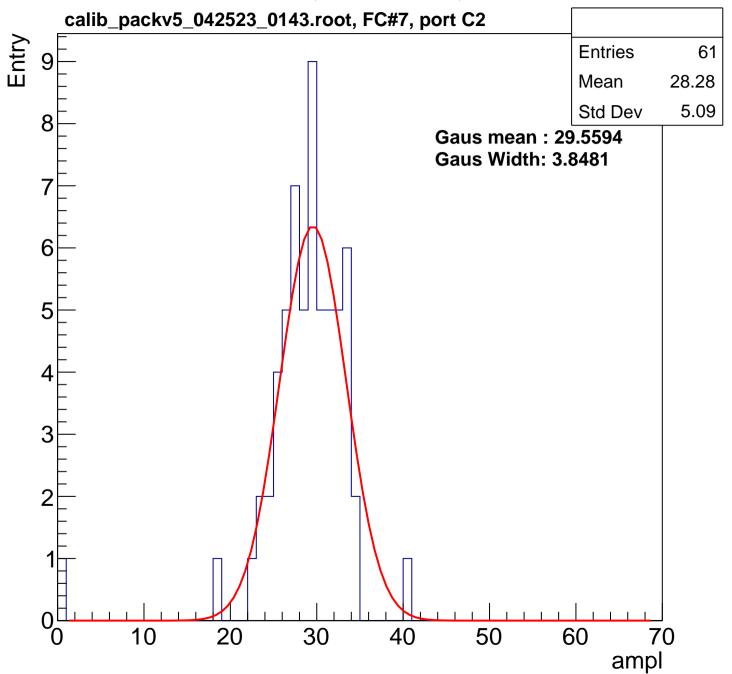


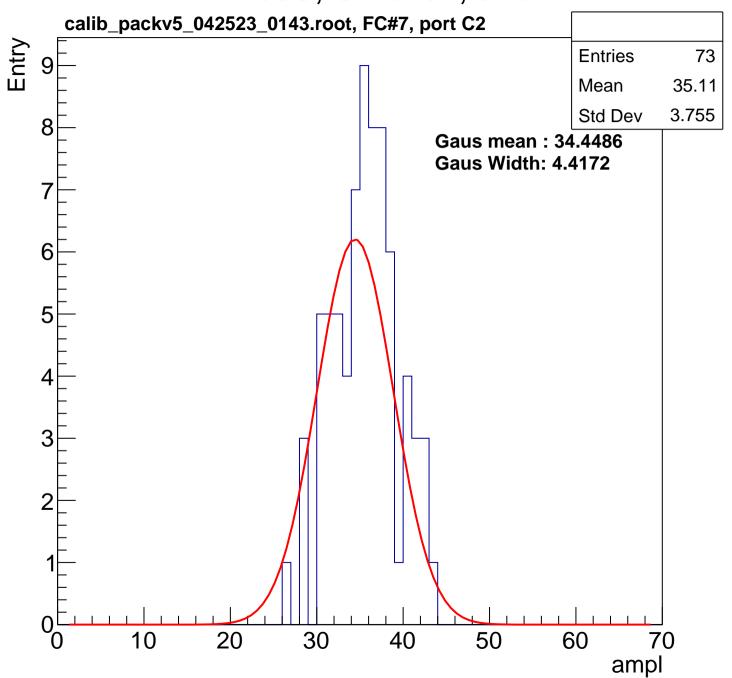


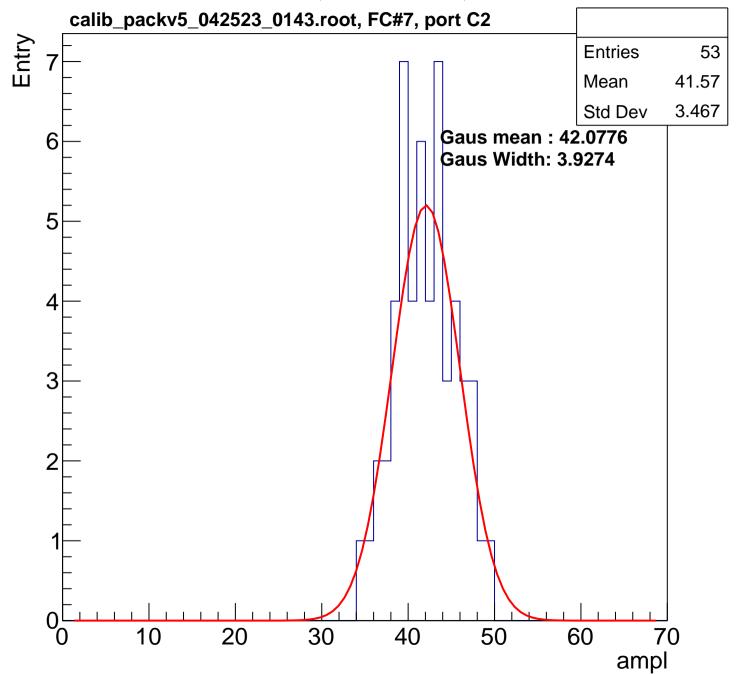


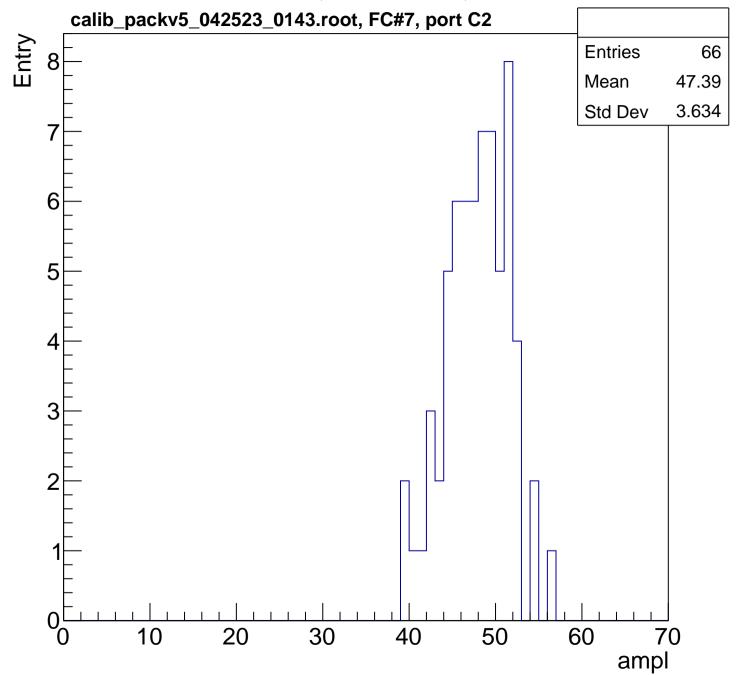


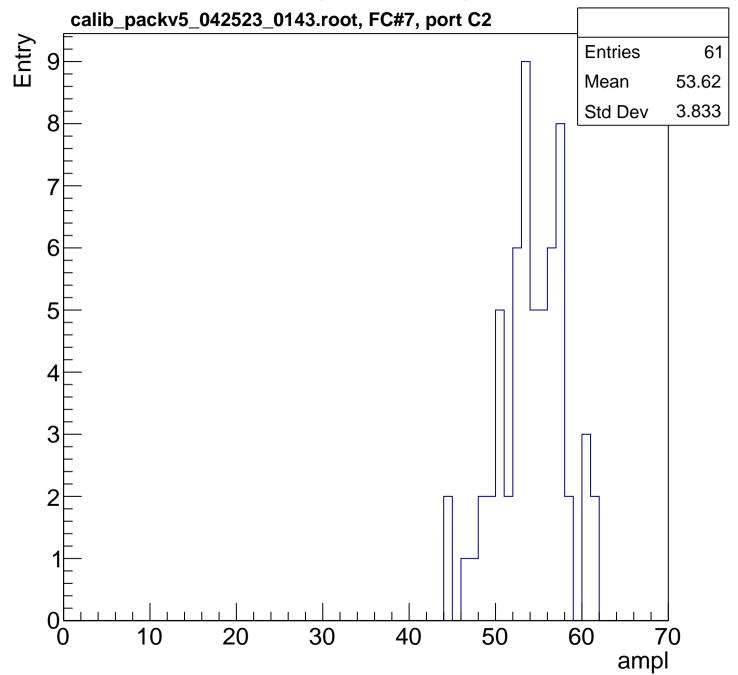
B1L103S, U4-ch63, adc7 calib_packv5_042523_0143.root, FC#7, port C2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

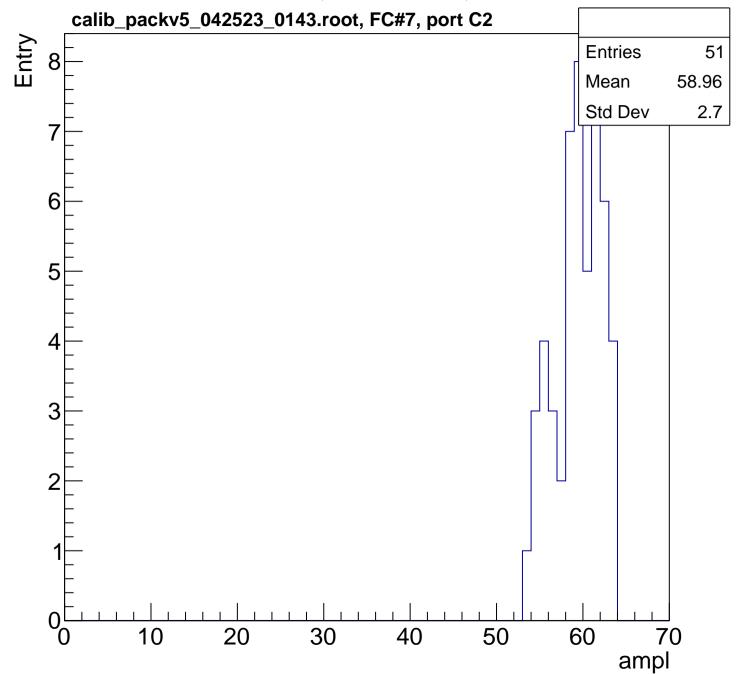


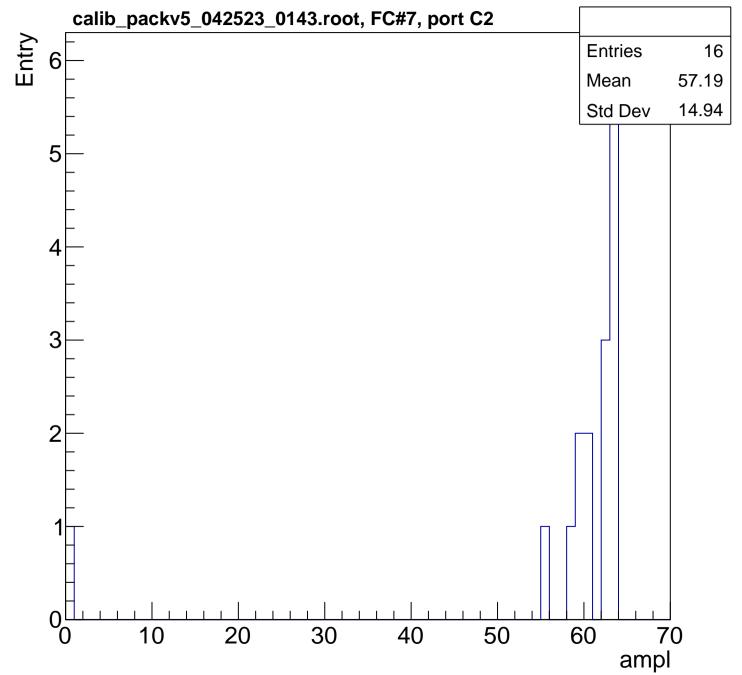


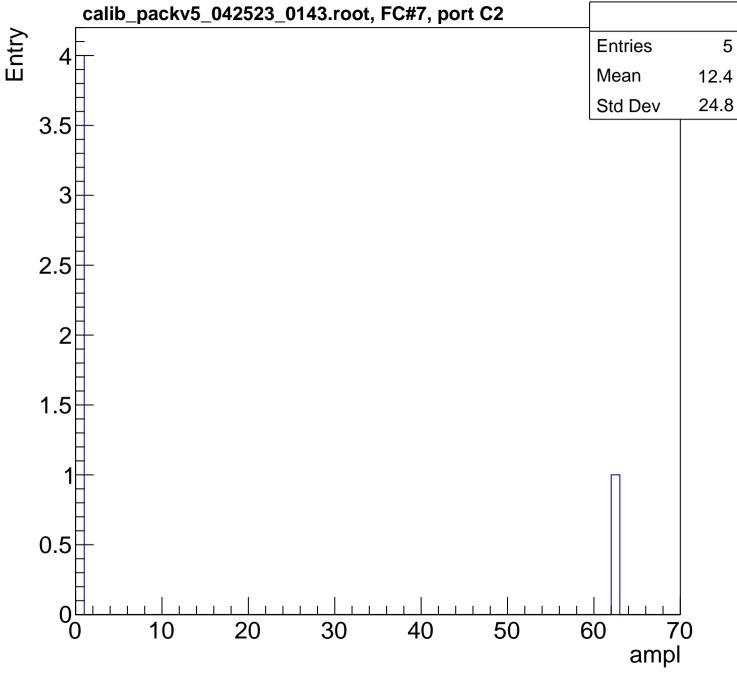


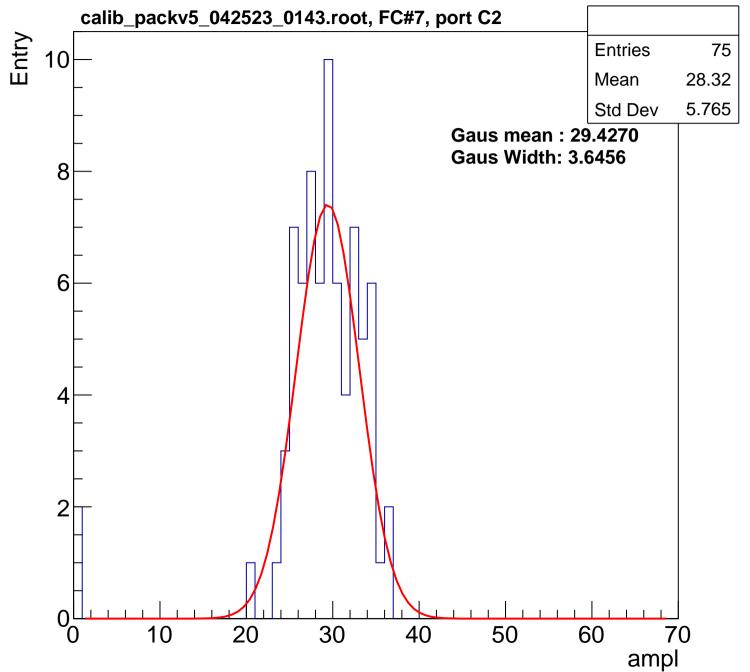


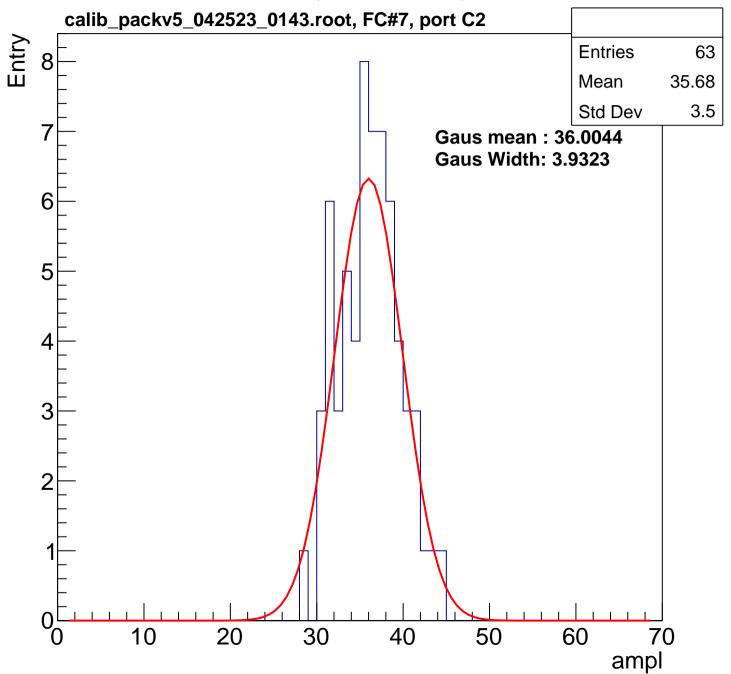


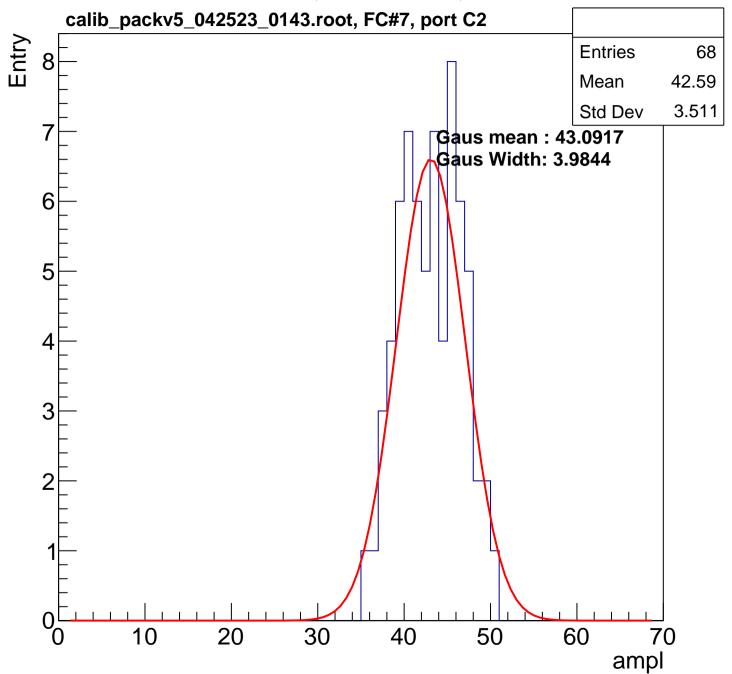


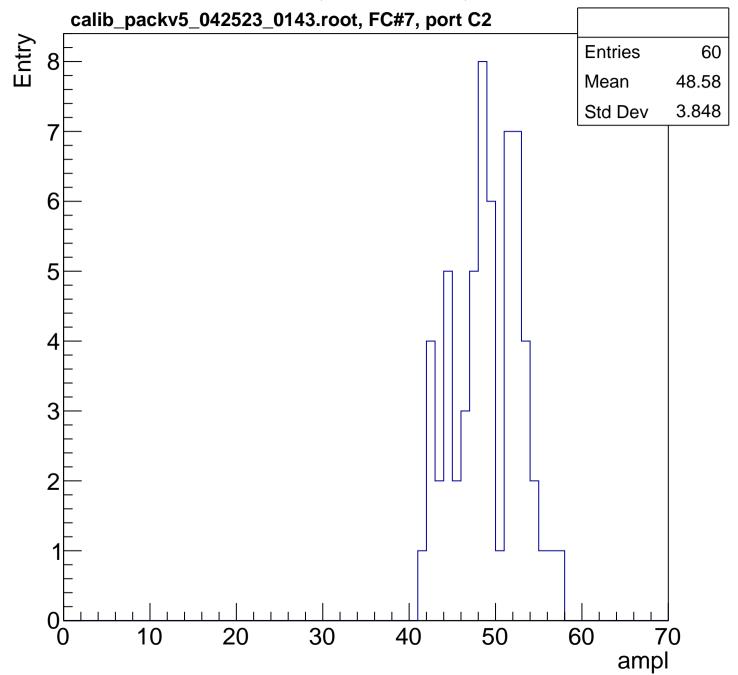


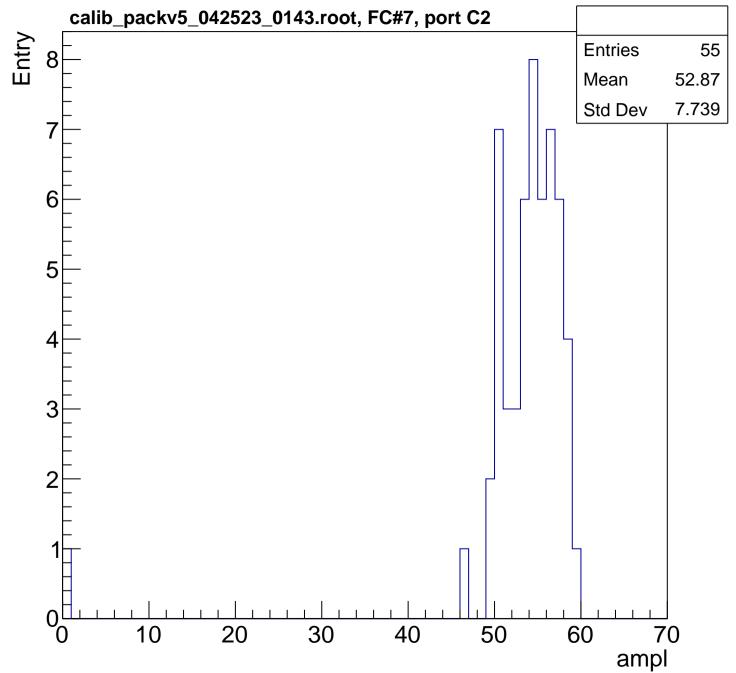


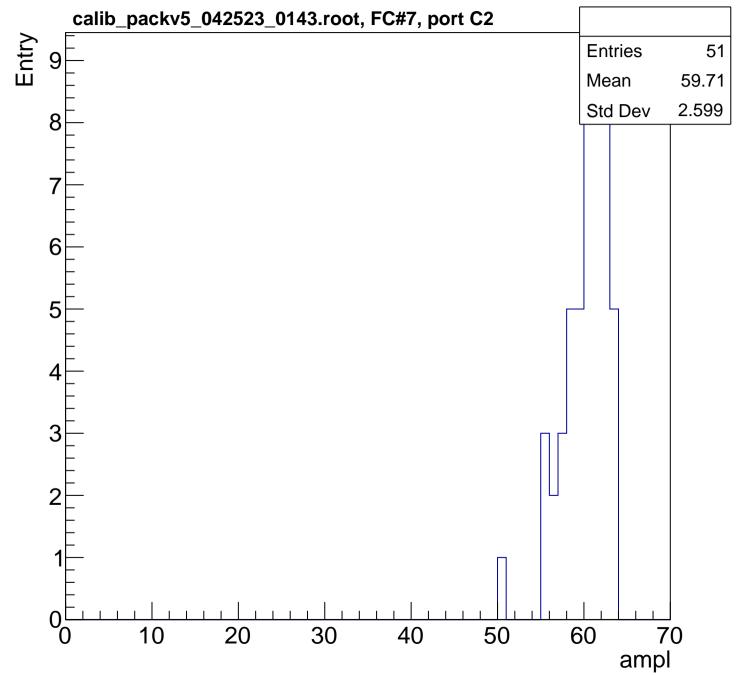


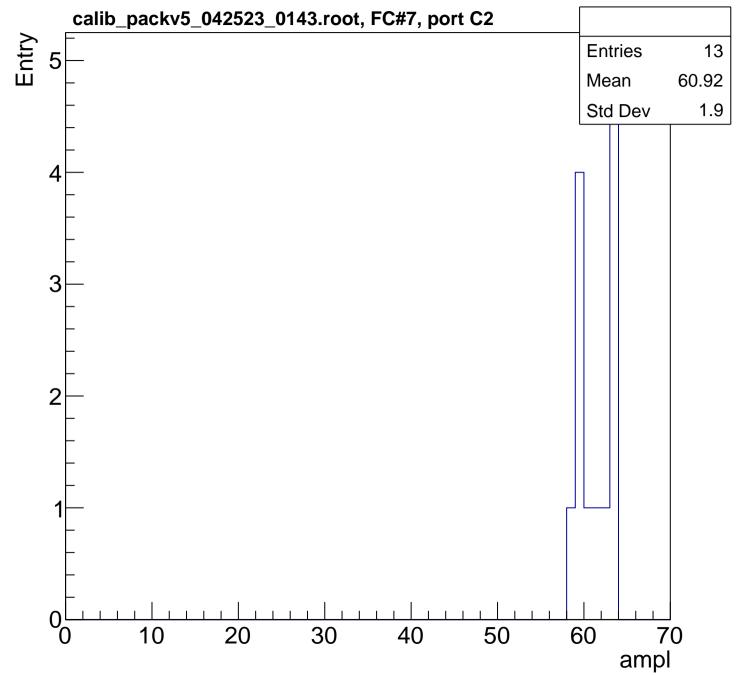




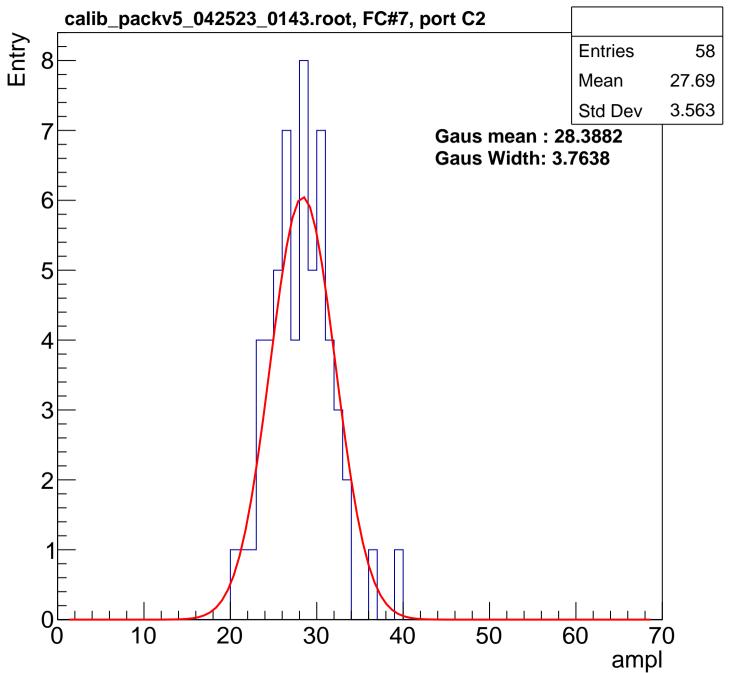


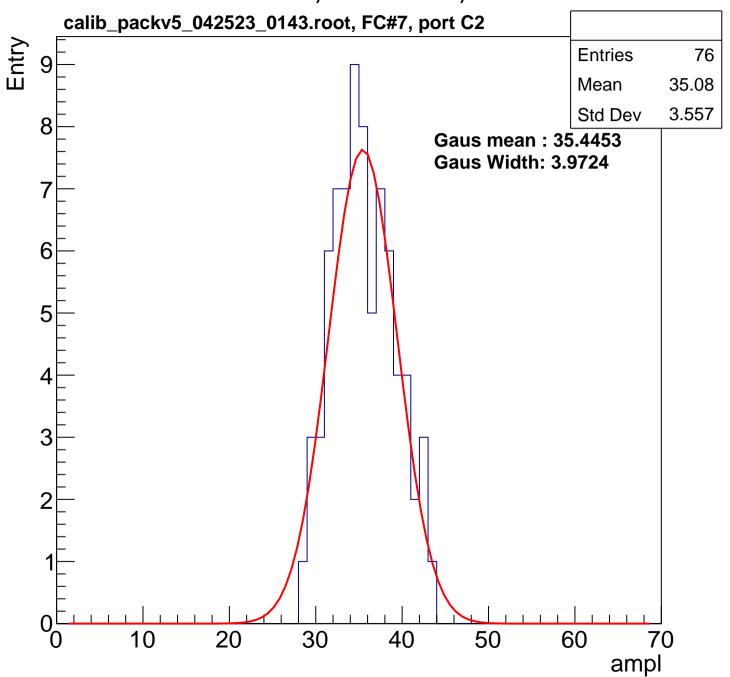


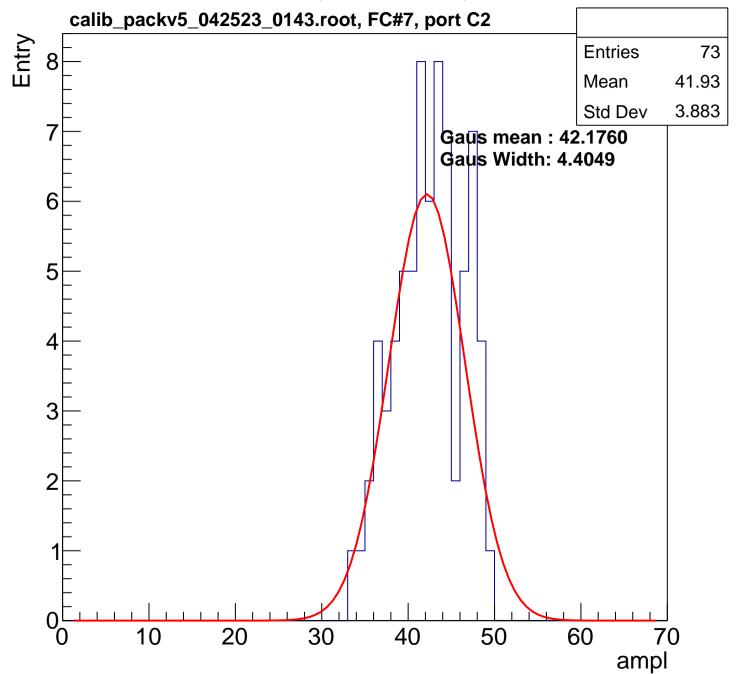


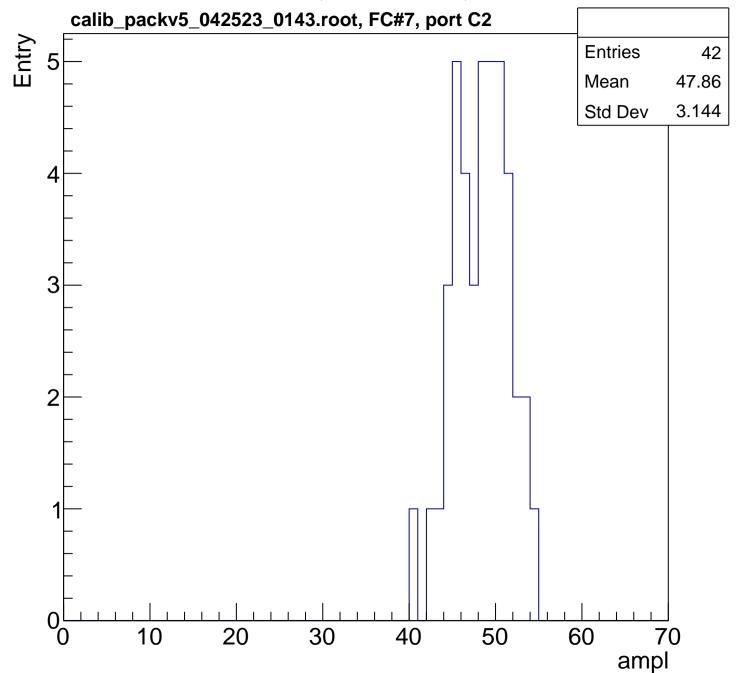


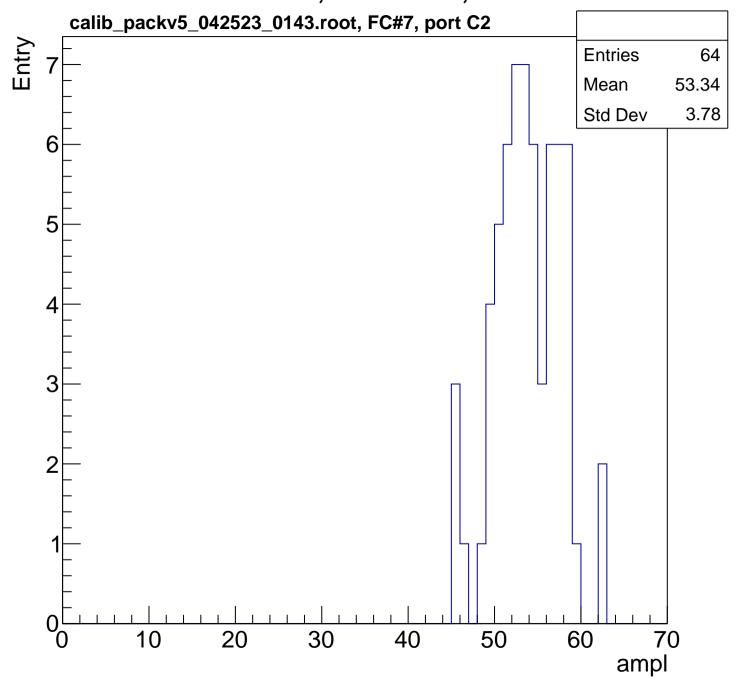


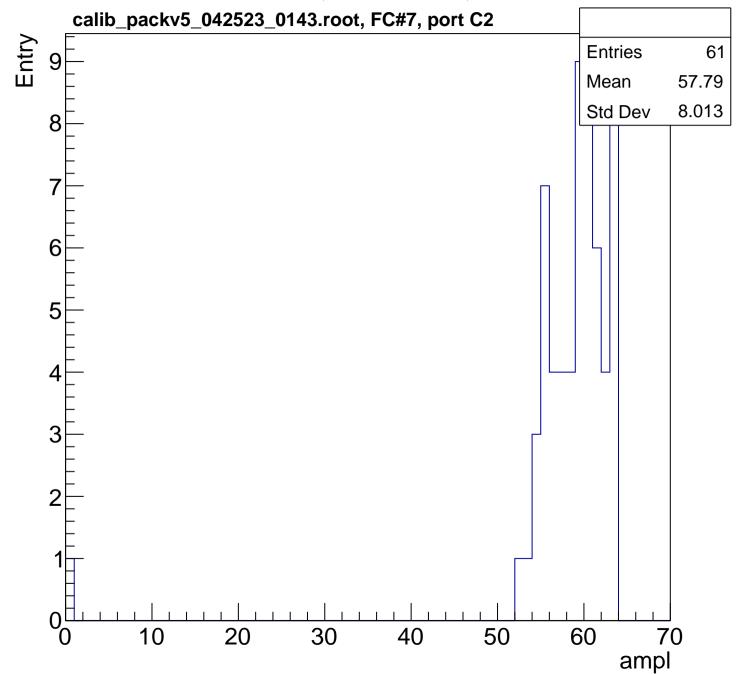


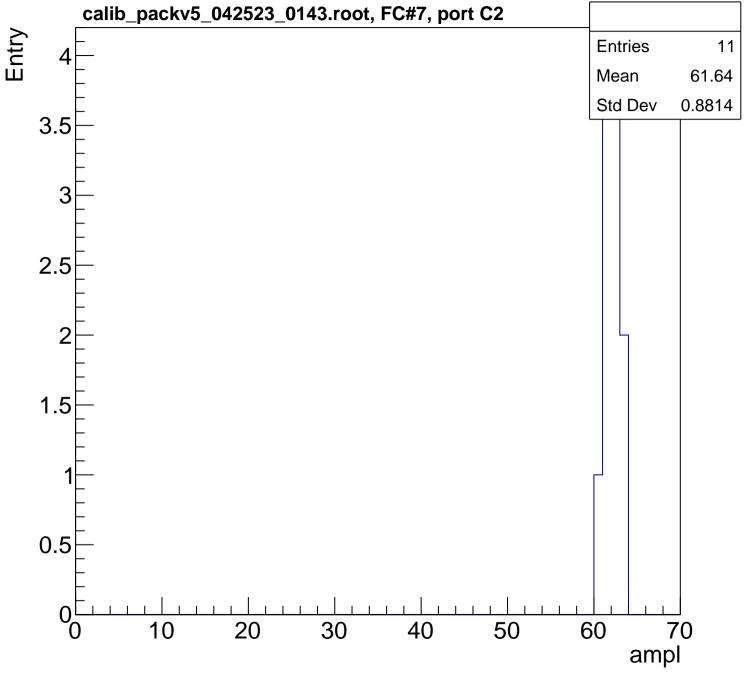


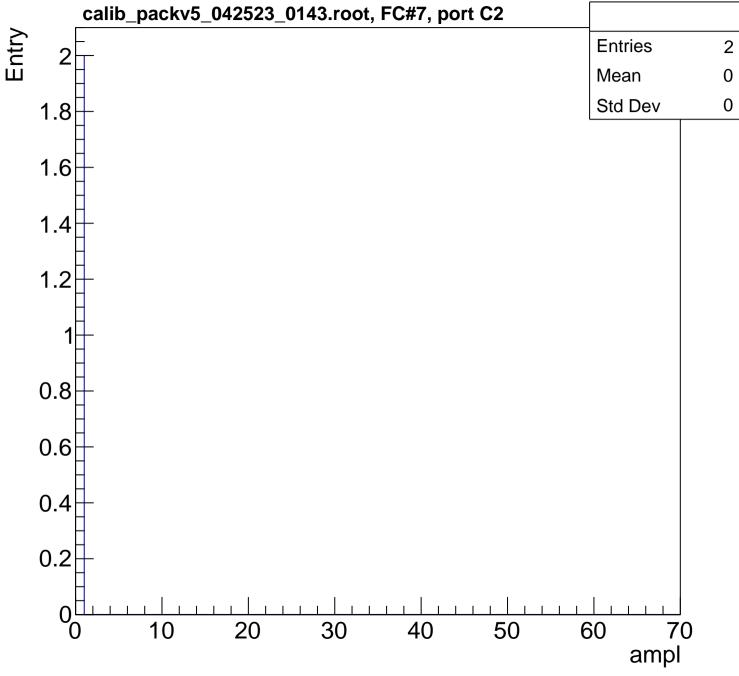


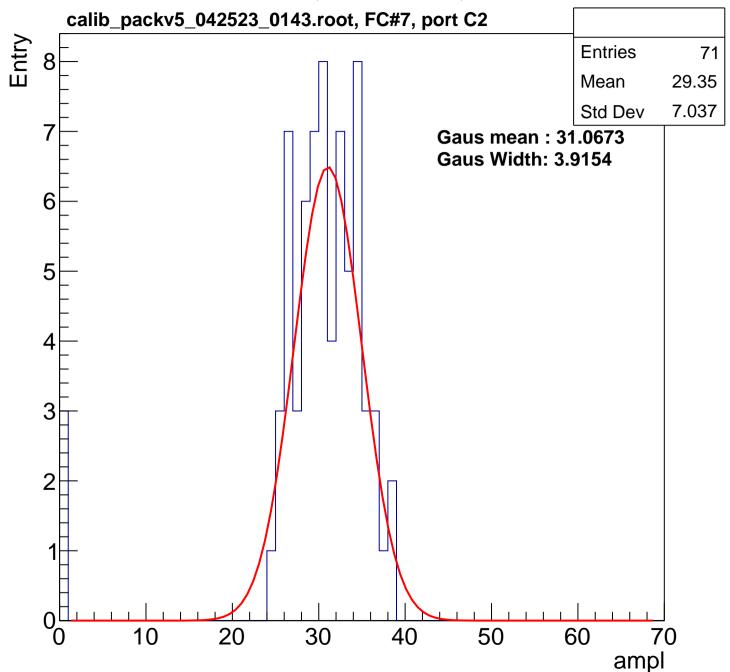


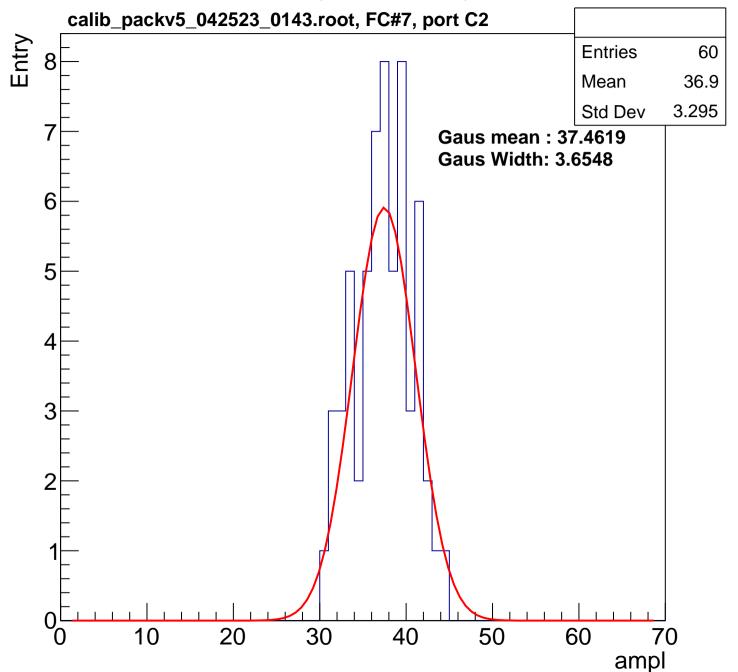


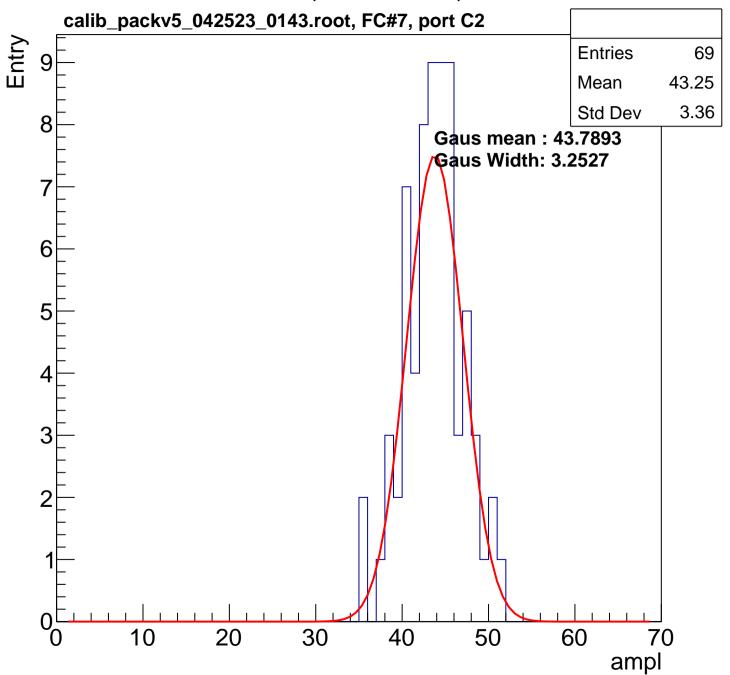


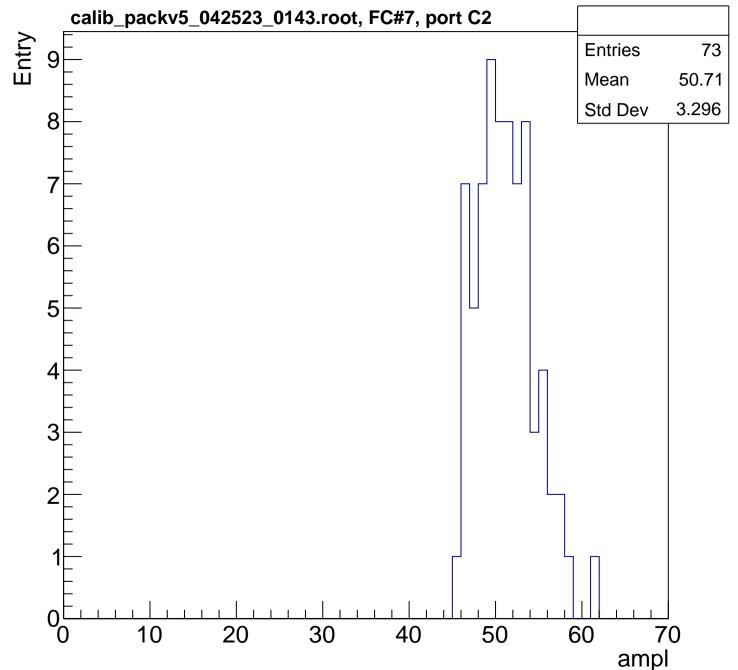


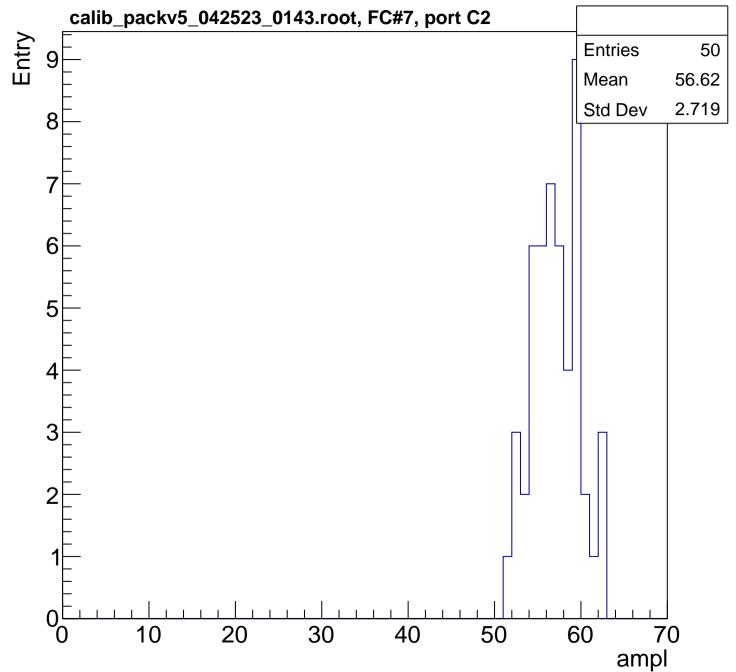


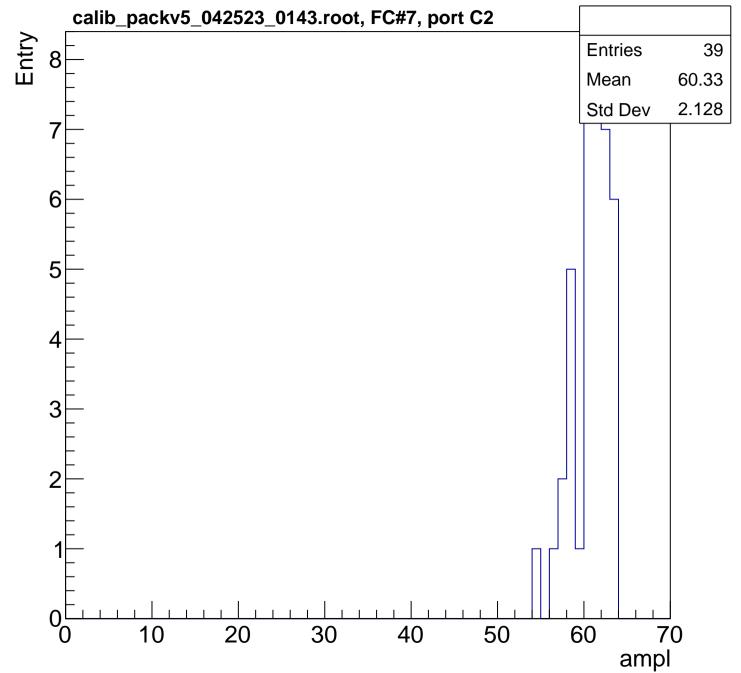


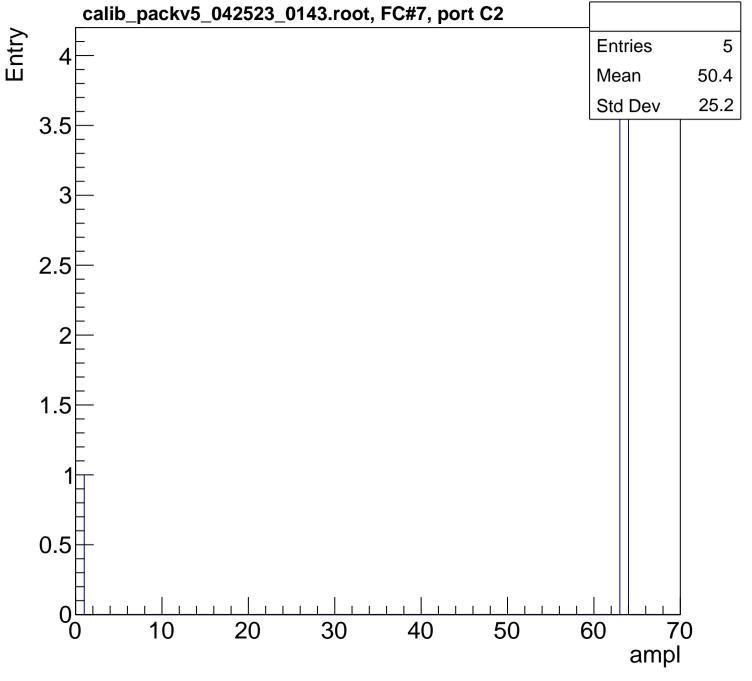




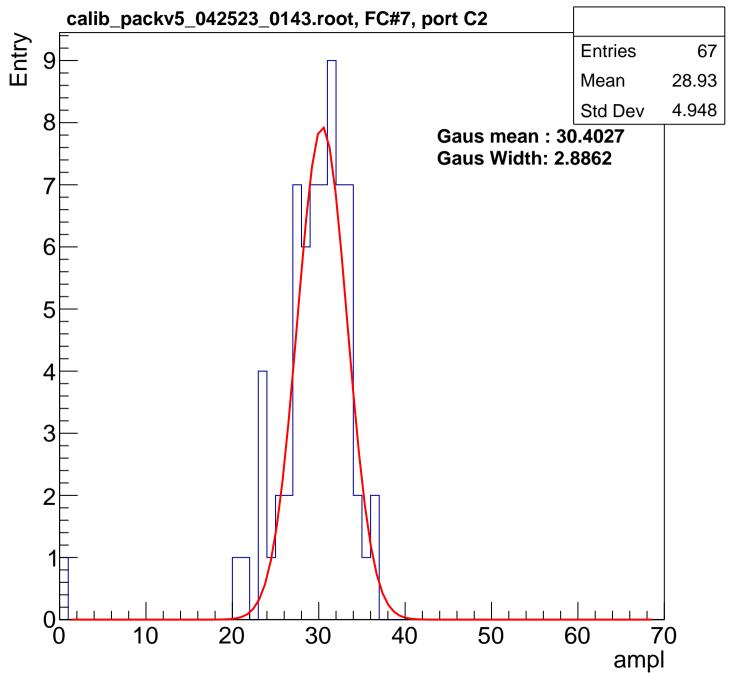


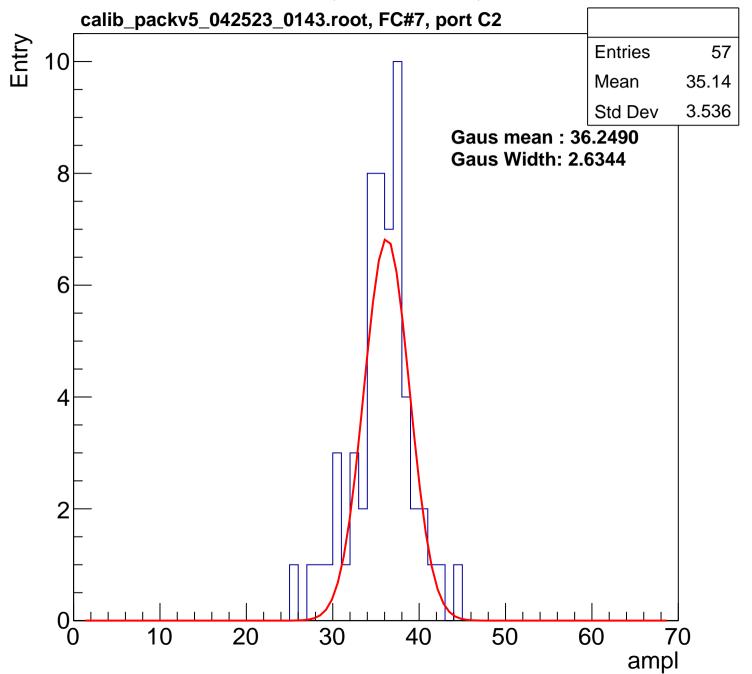


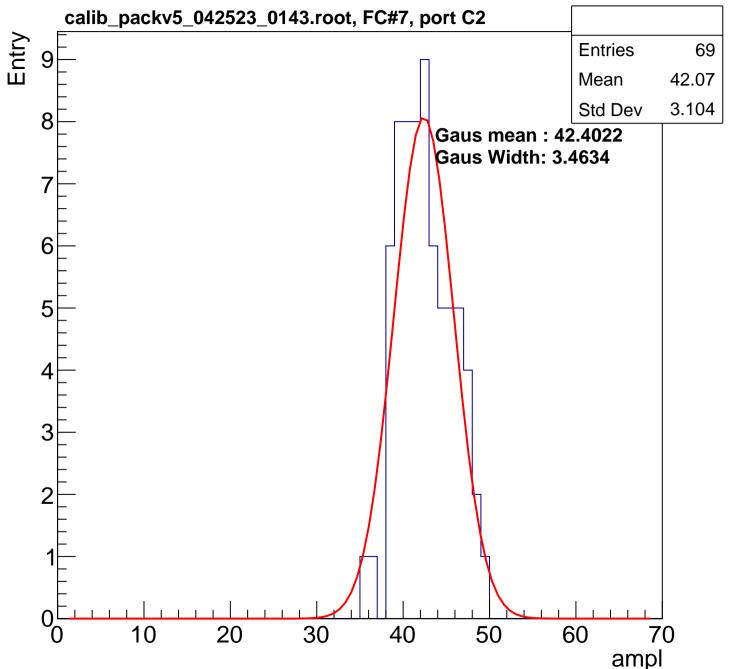


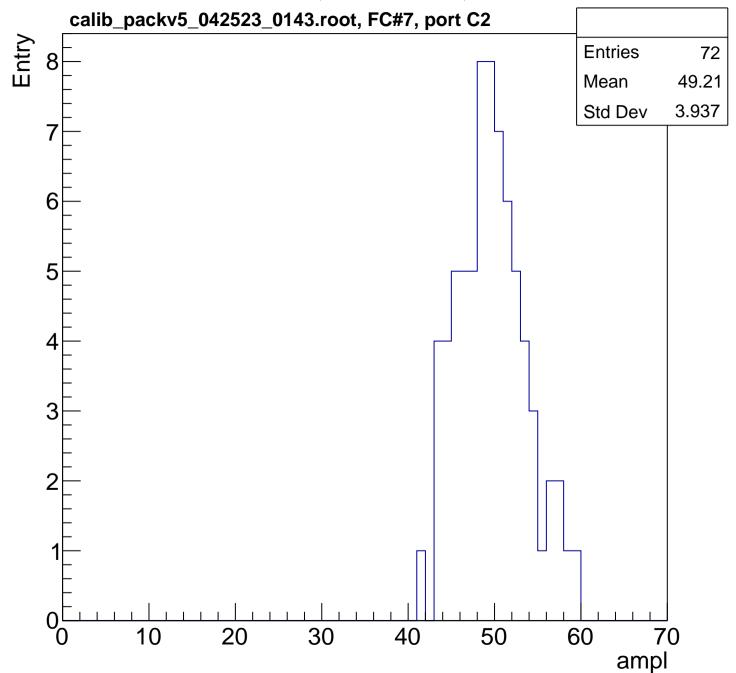


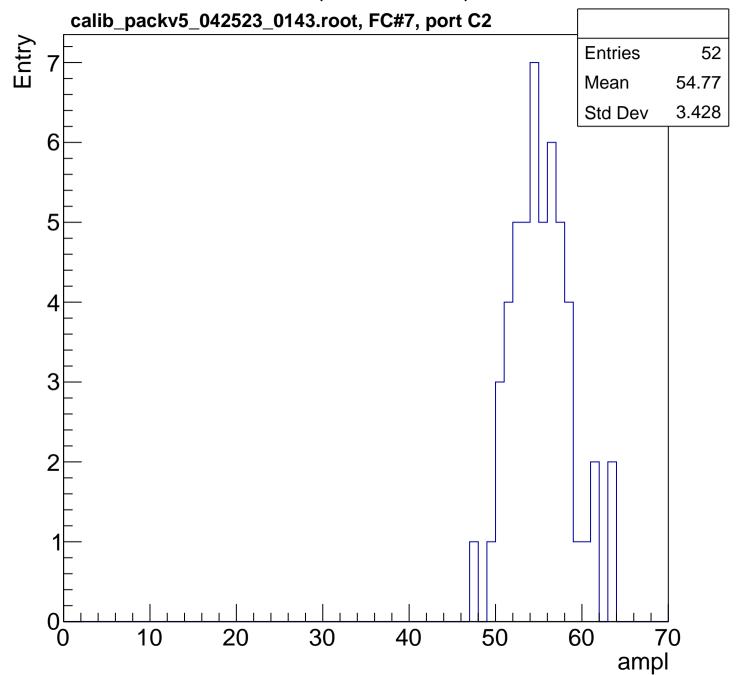
B1L103S, U4-ch67, adc7 calib_packv5_042523_0143.root, FC#7, port C2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

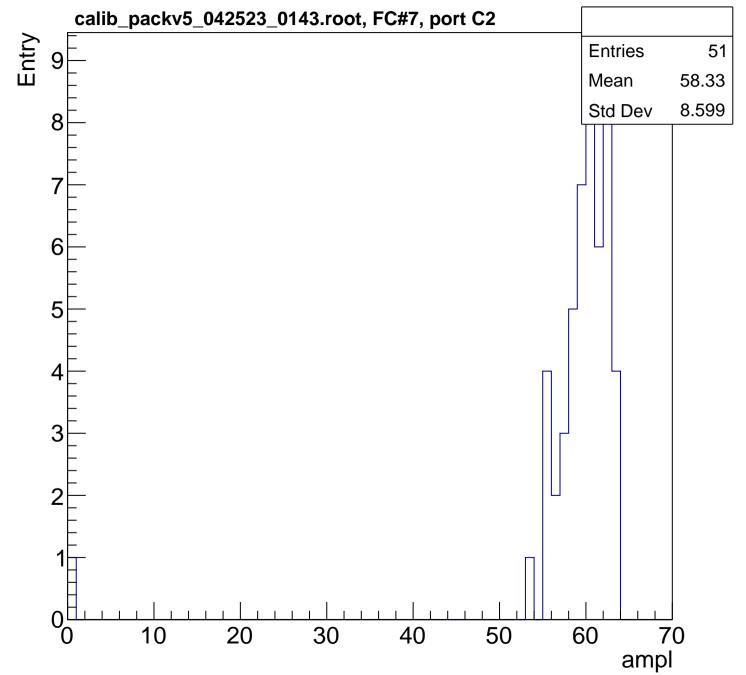


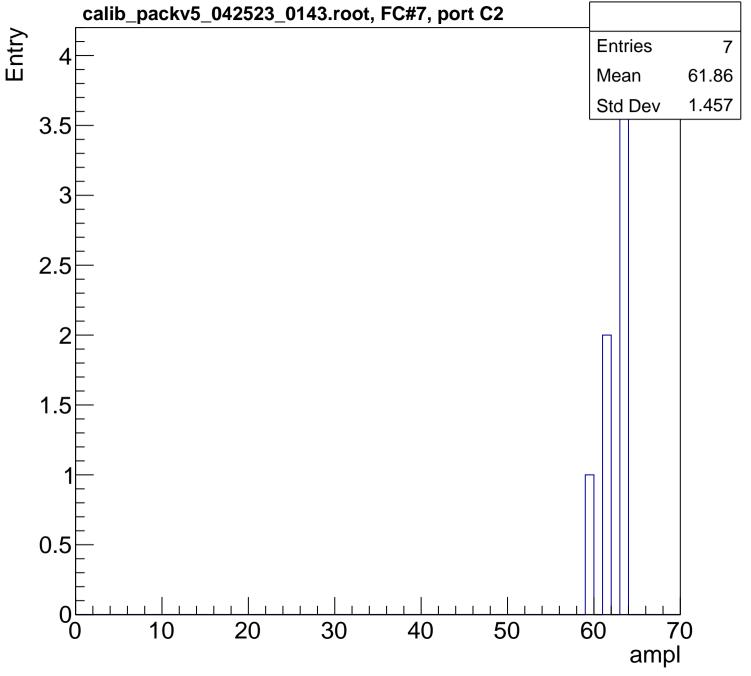


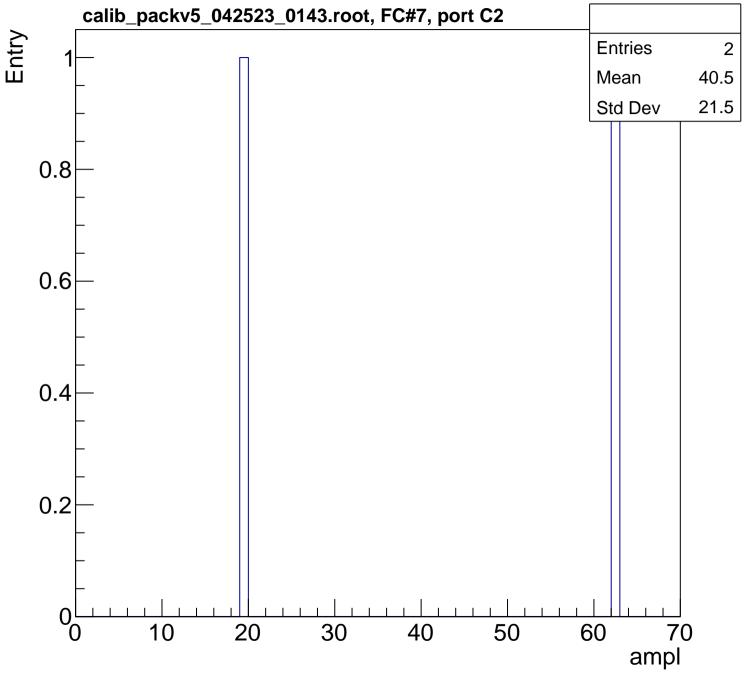


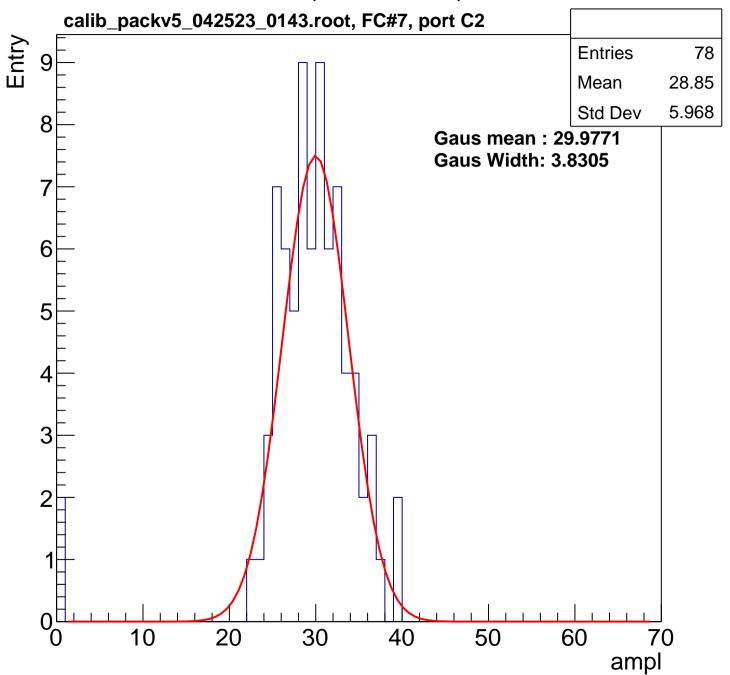


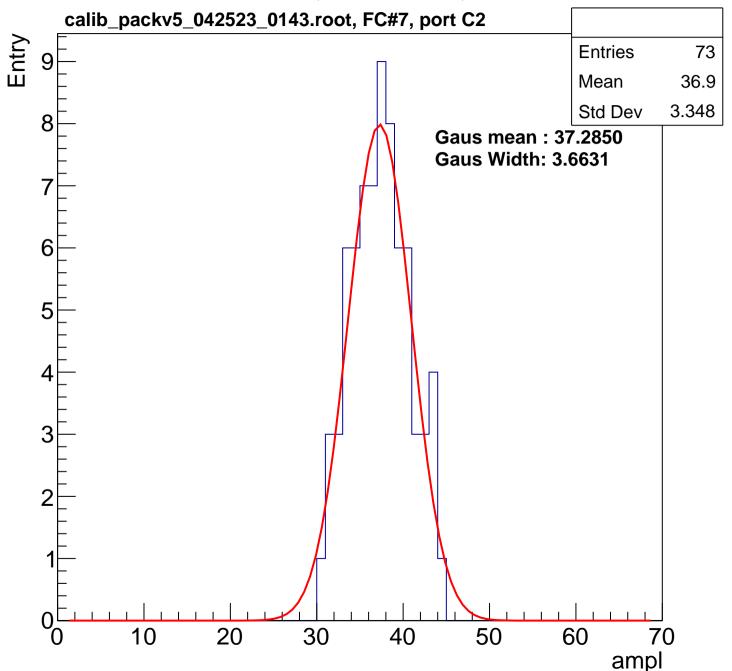


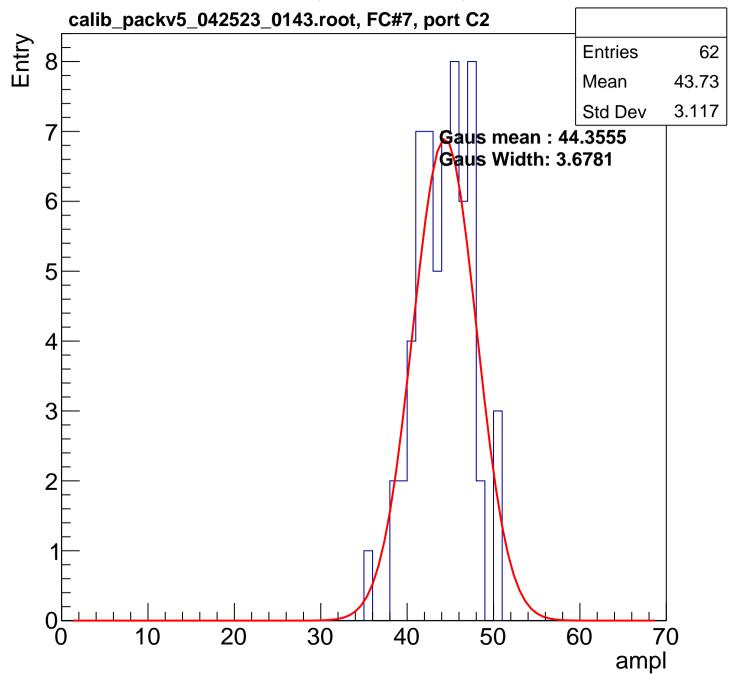




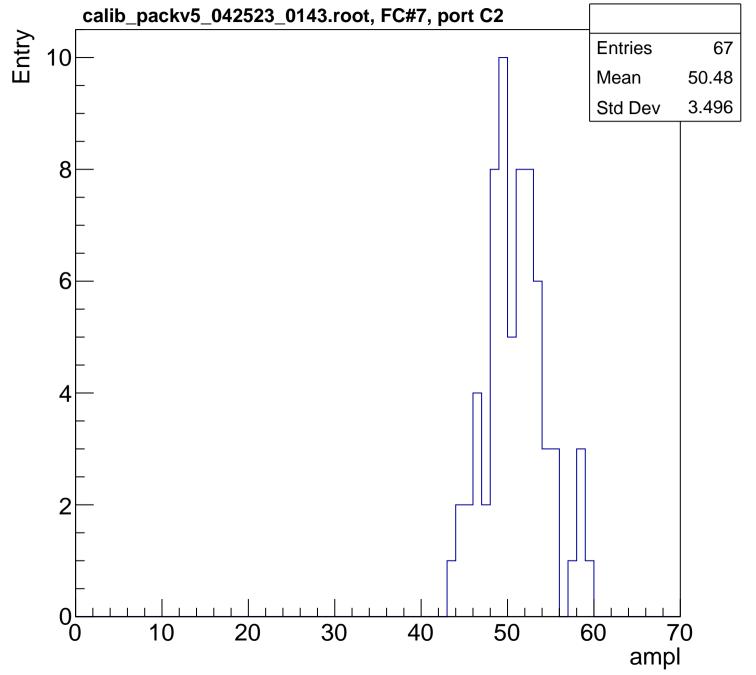


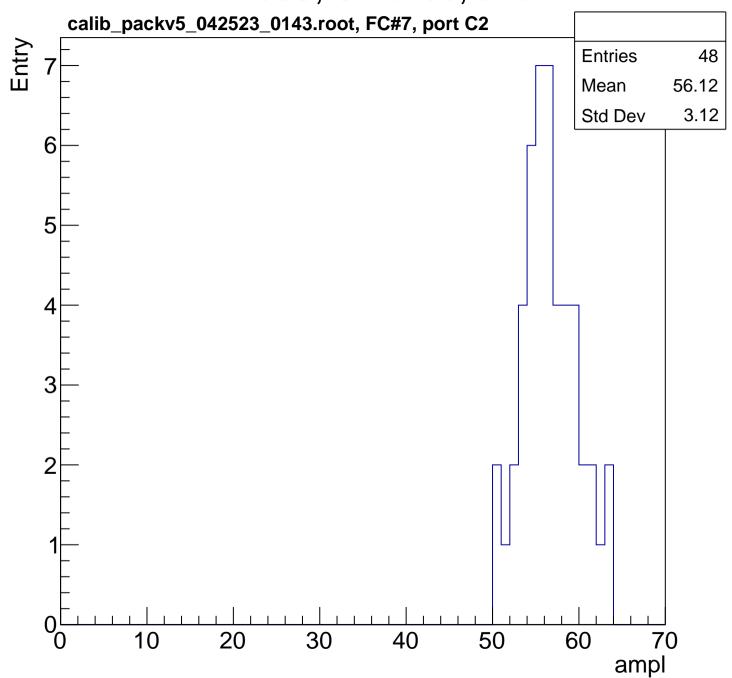


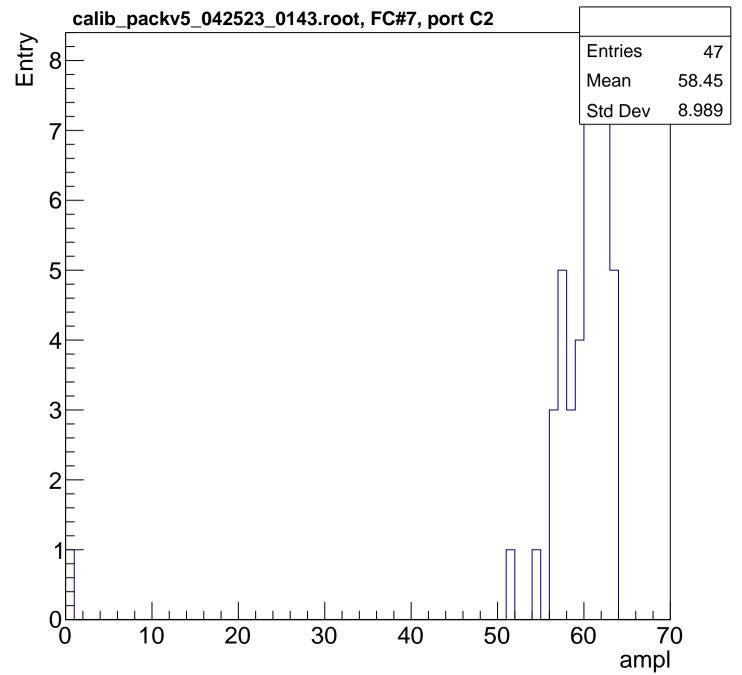


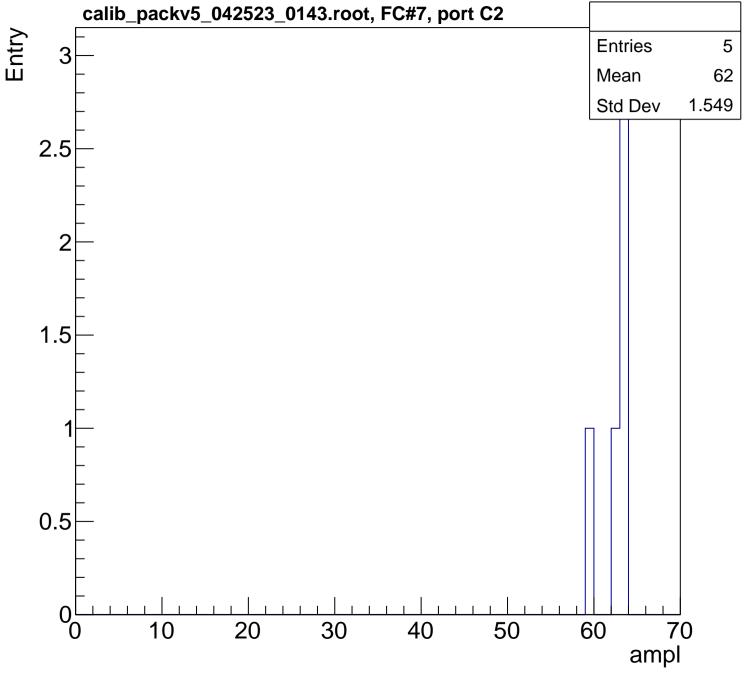


B1L103S, U4-ch69, adc3

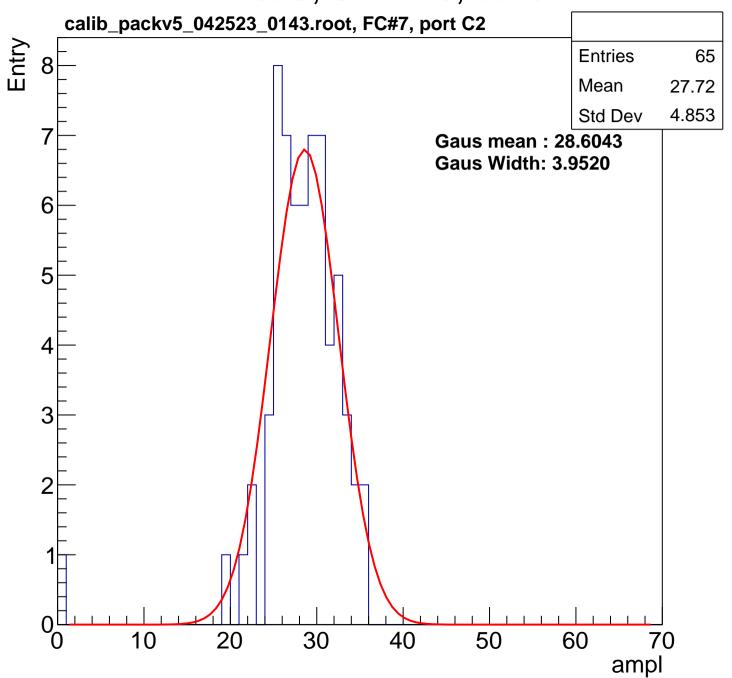


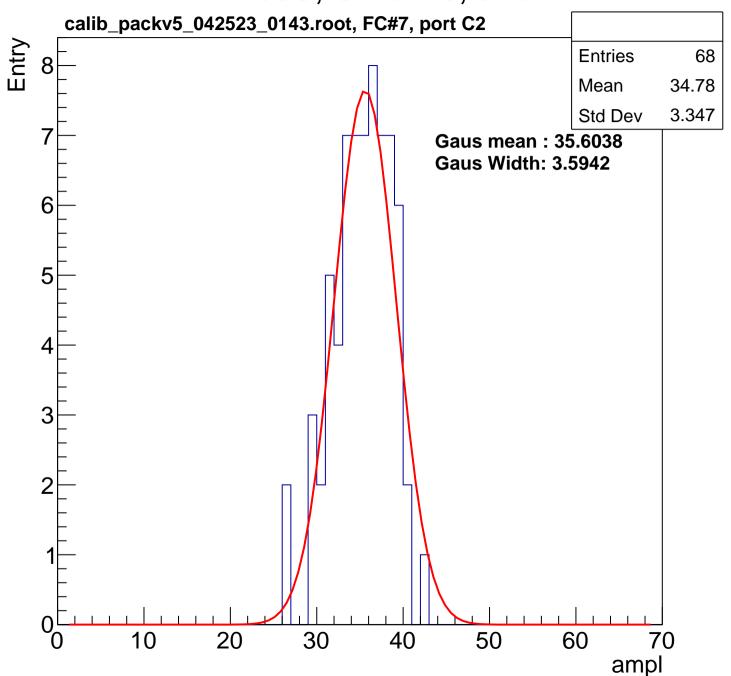


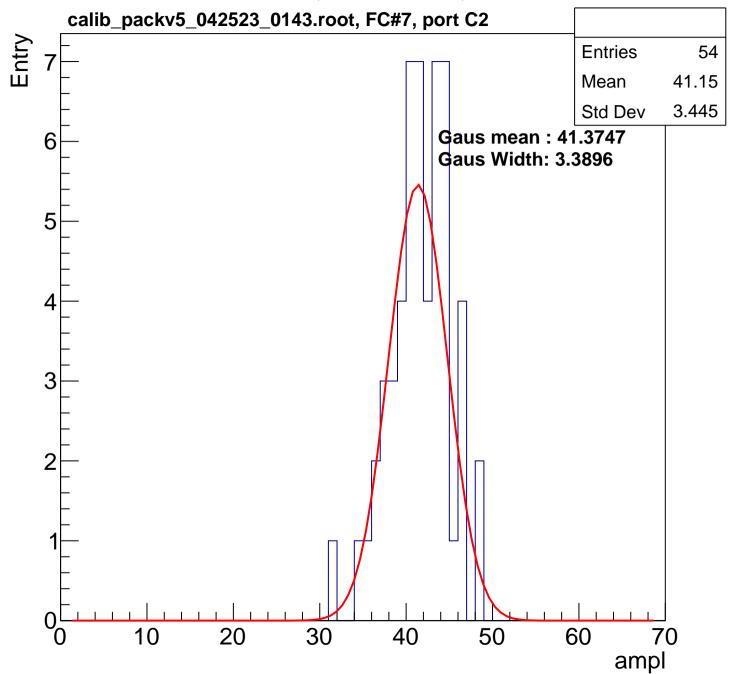




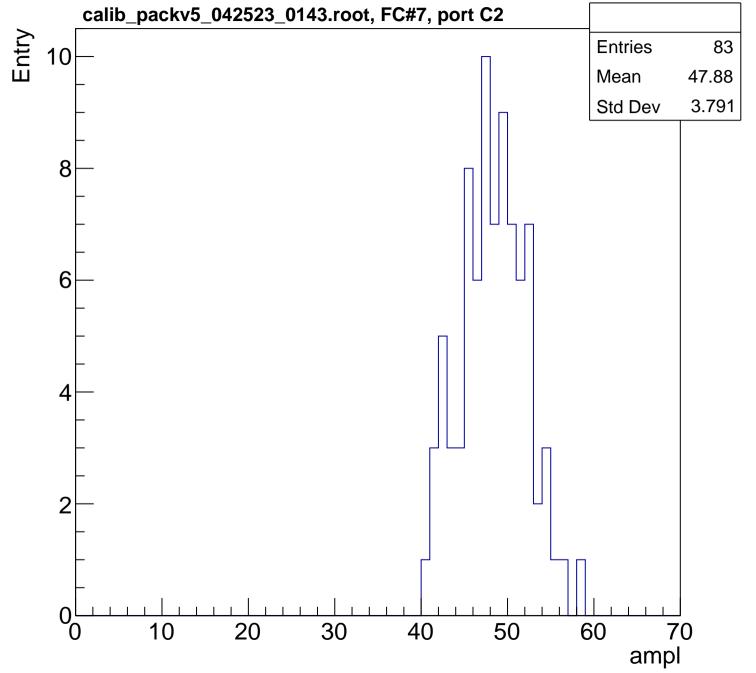
B1L103S, U4-ch69, adc7 calib_packv5_042523_0143.root, FC#7, port C2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

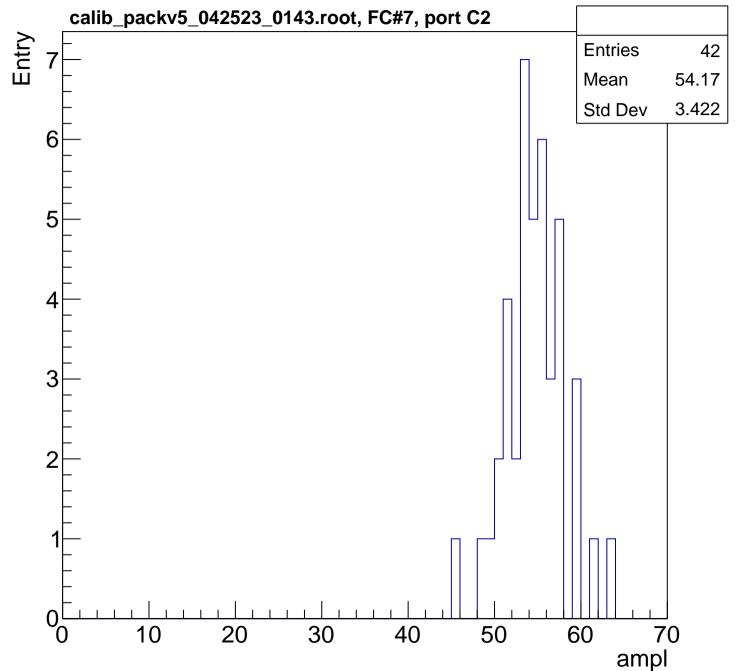


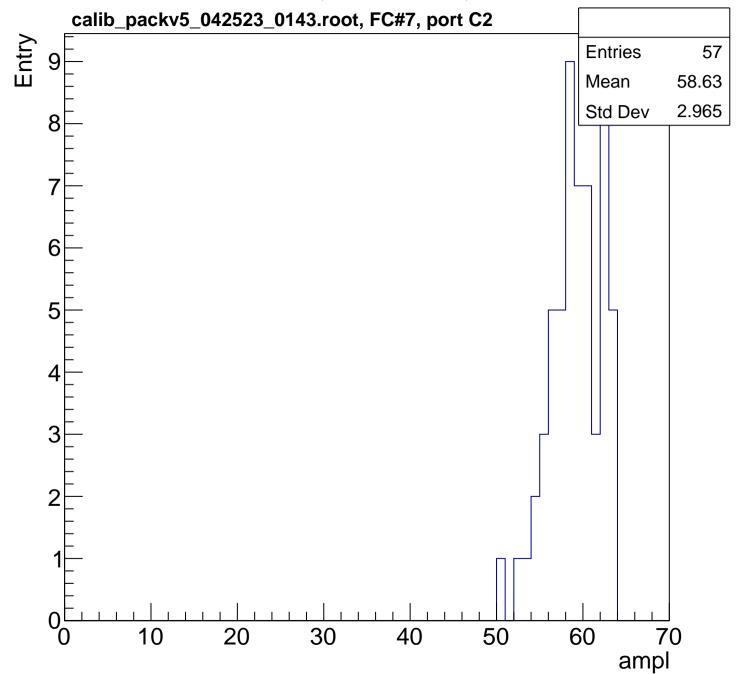


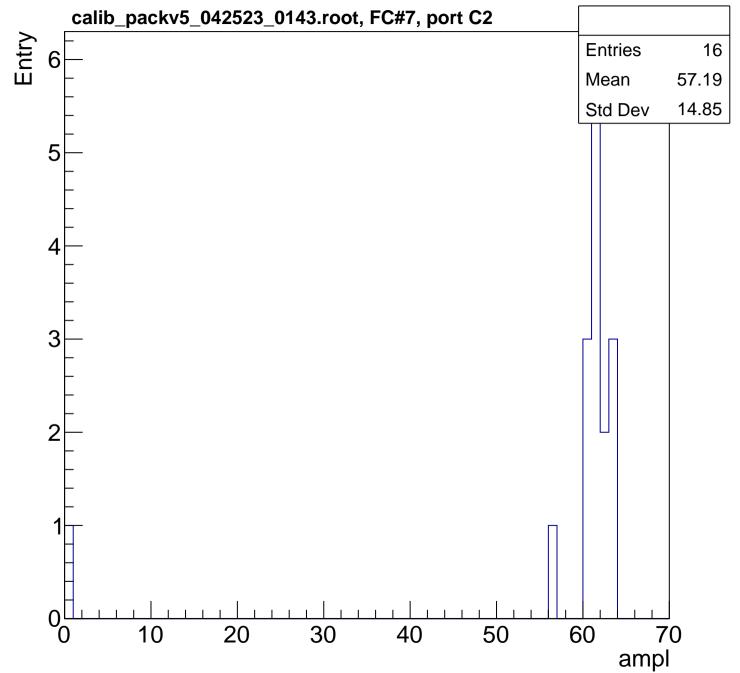


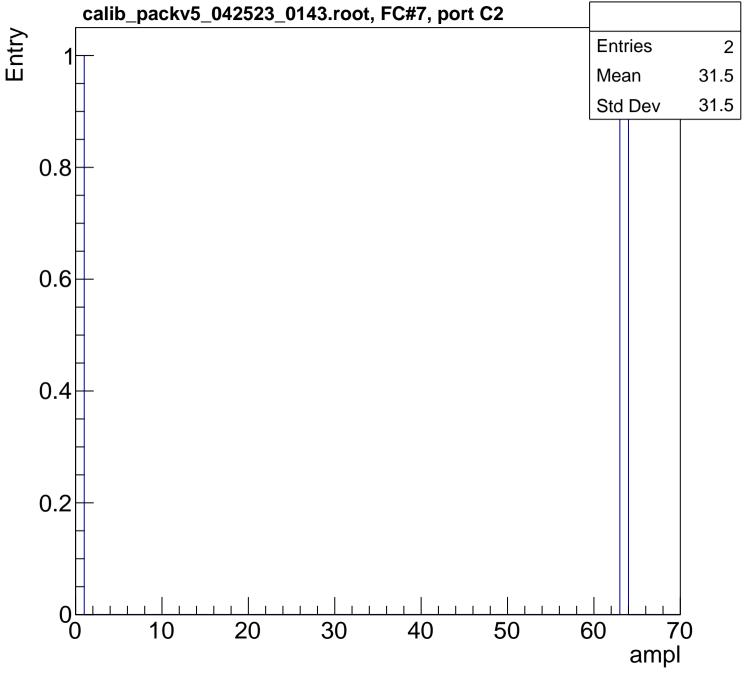
B1L103S, U4-ch70, adc3

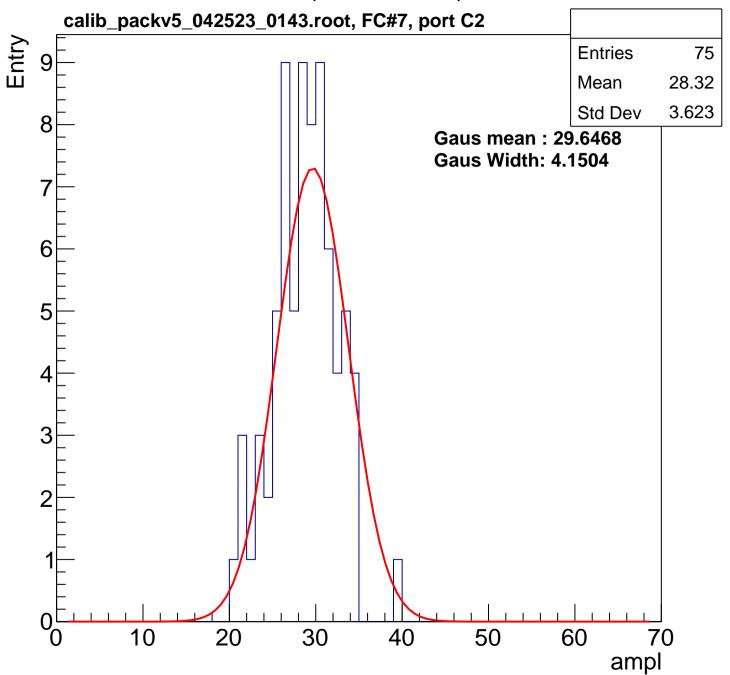


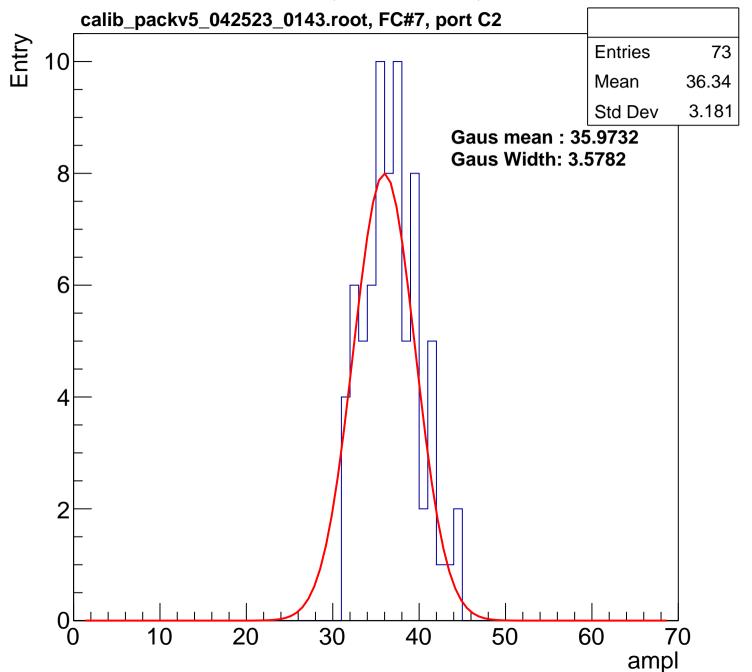


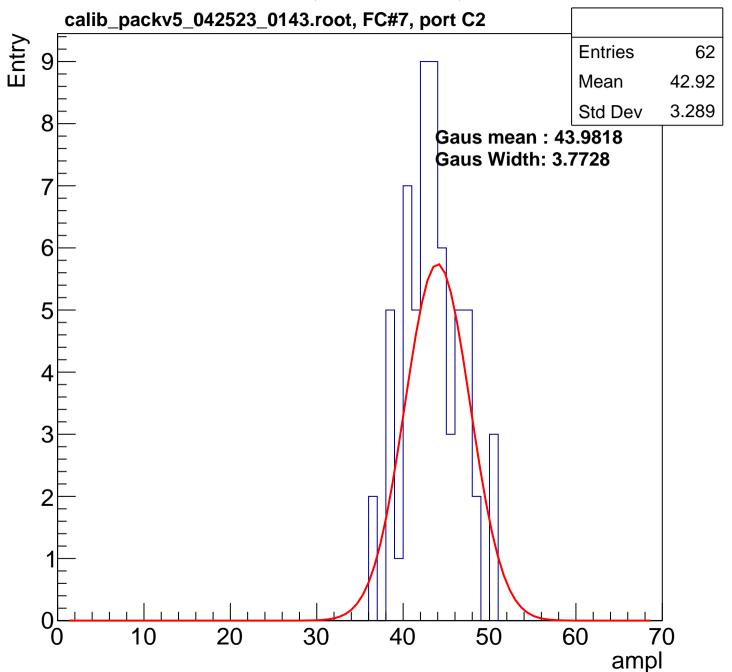


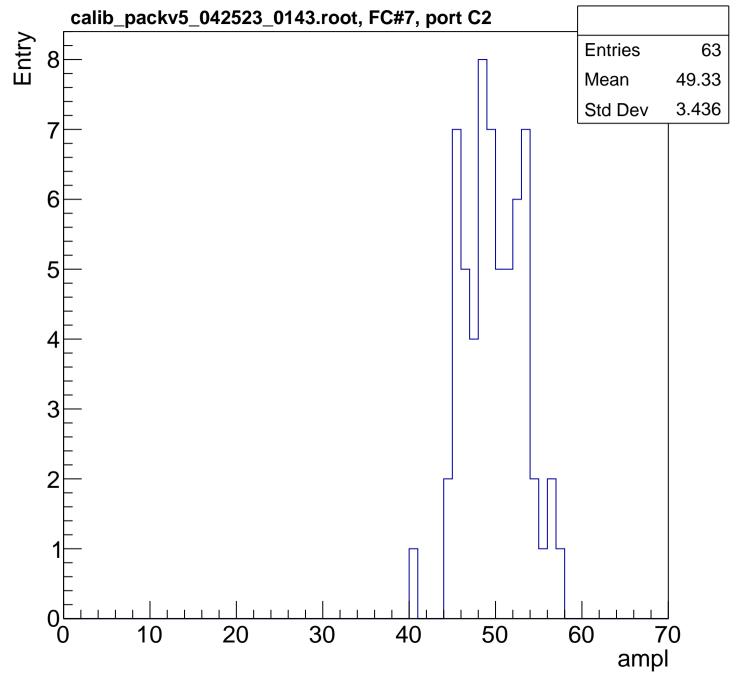


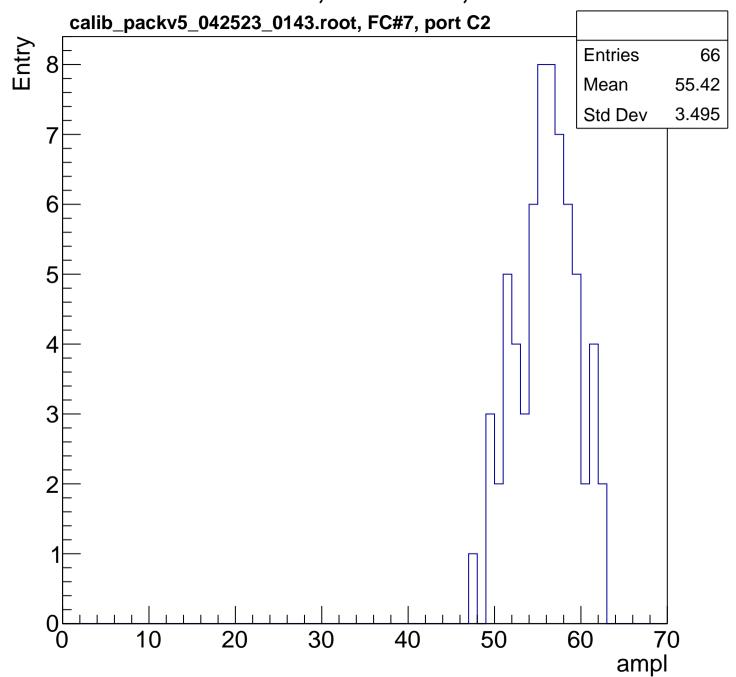


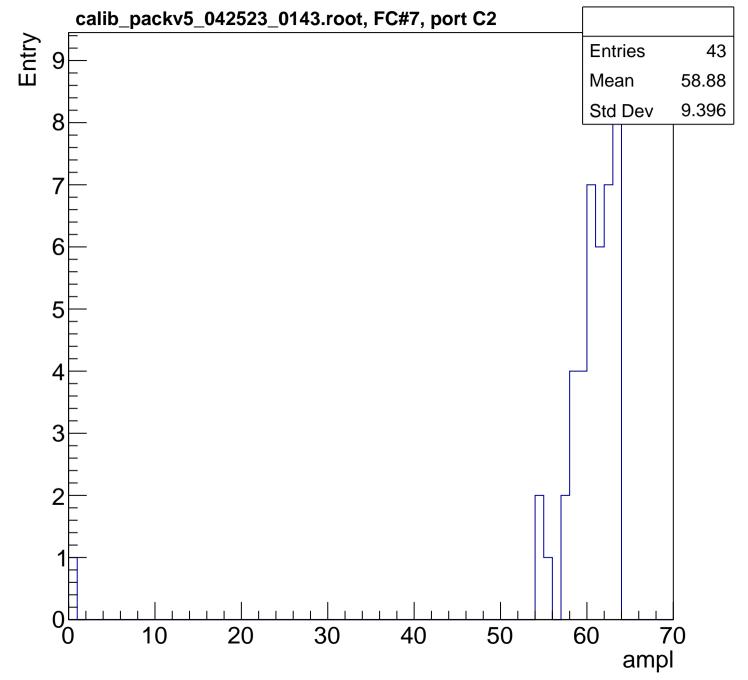


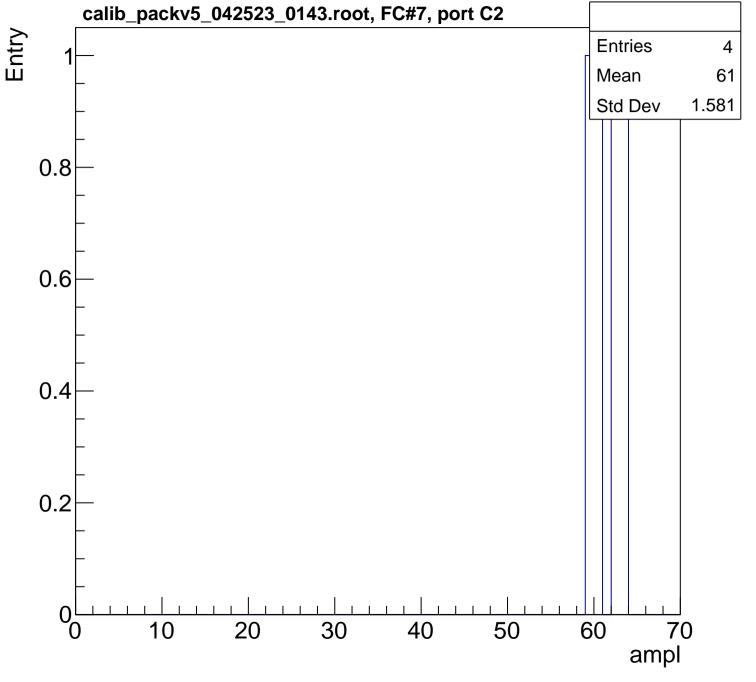




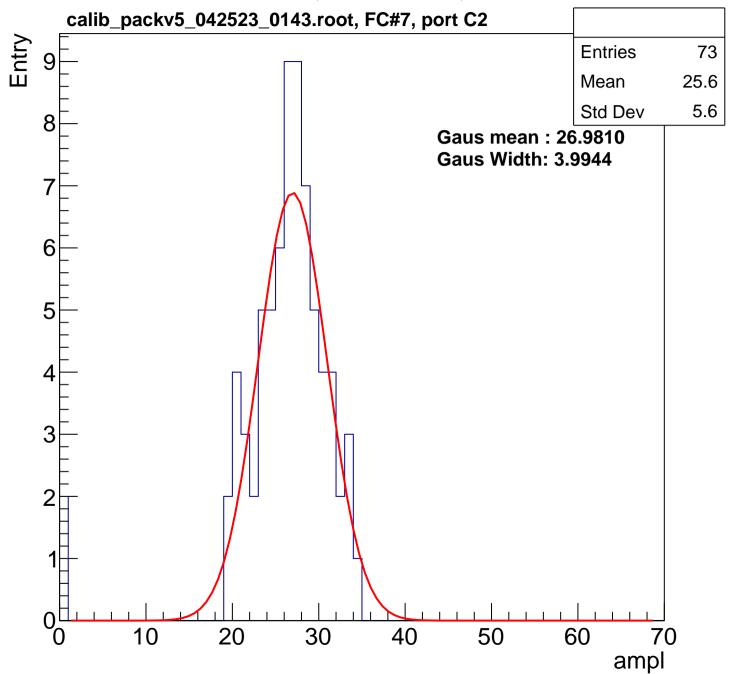


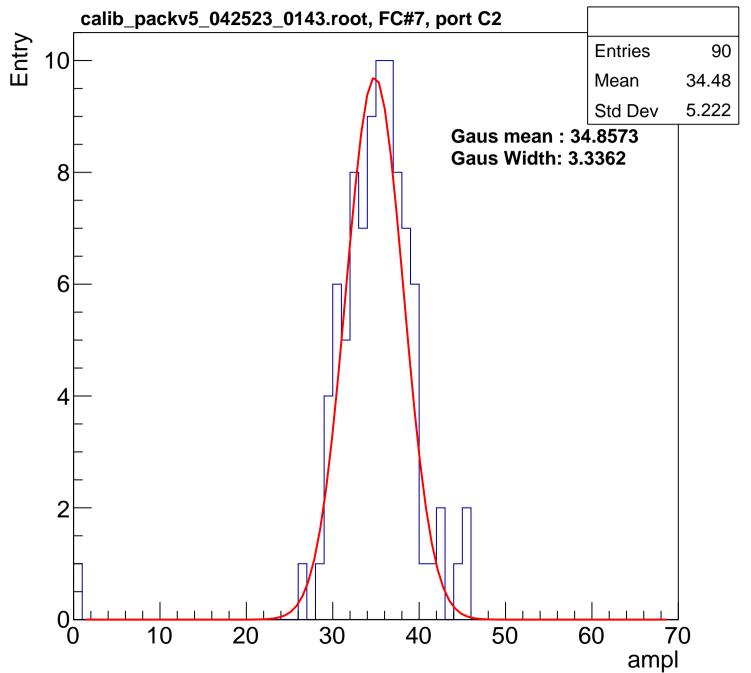


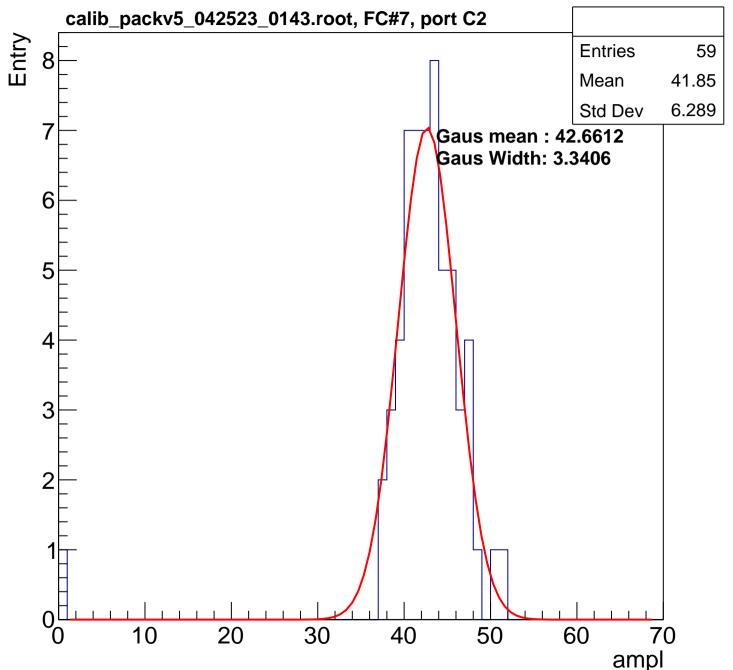


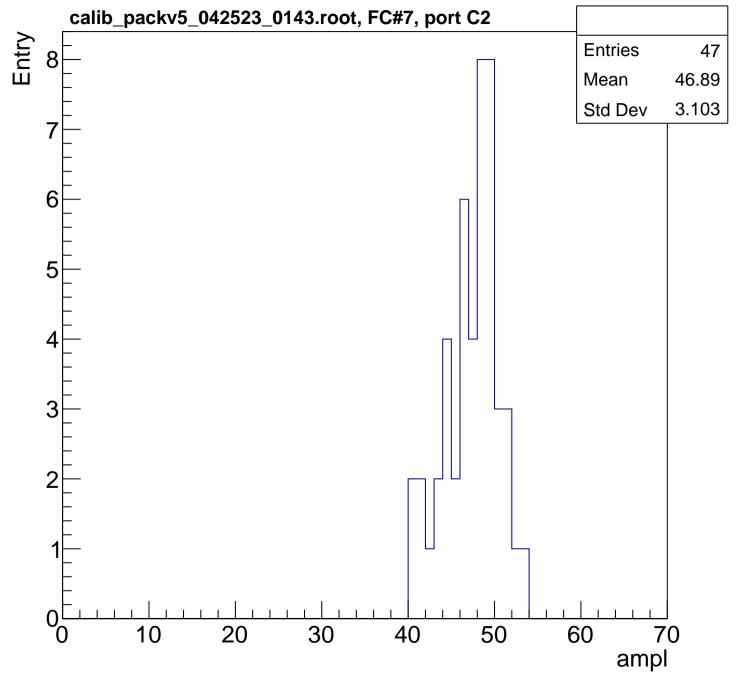


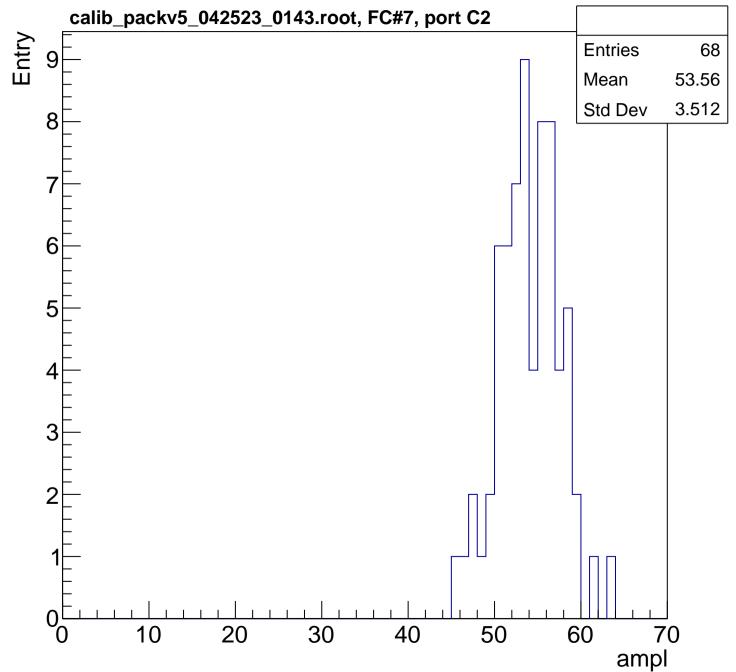


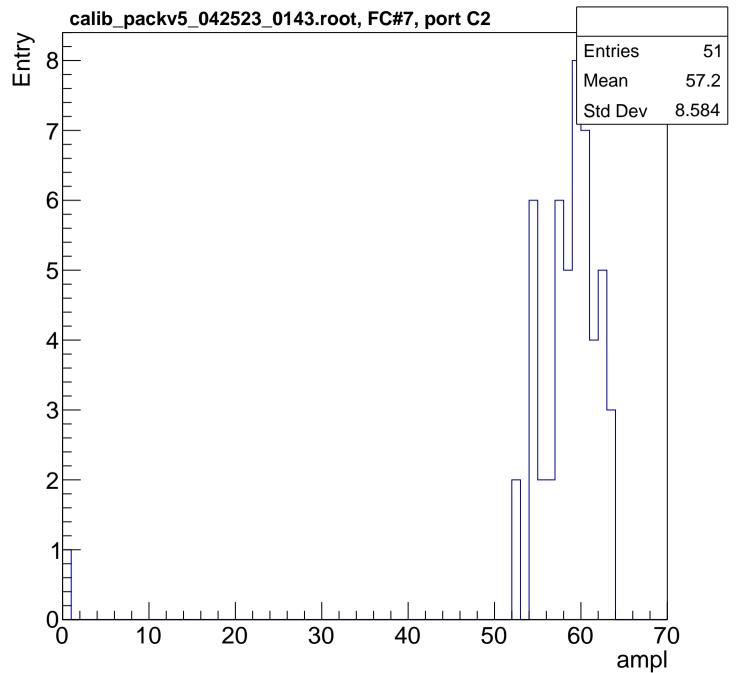


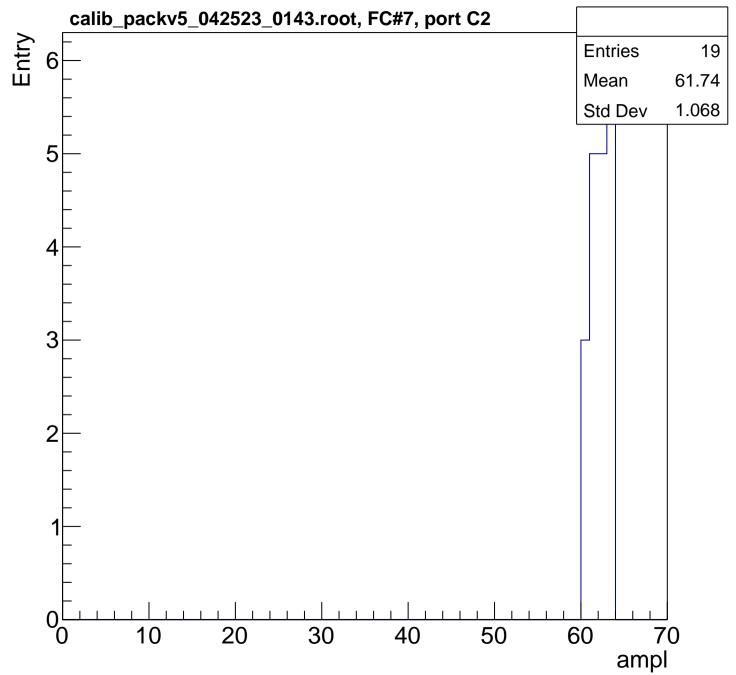




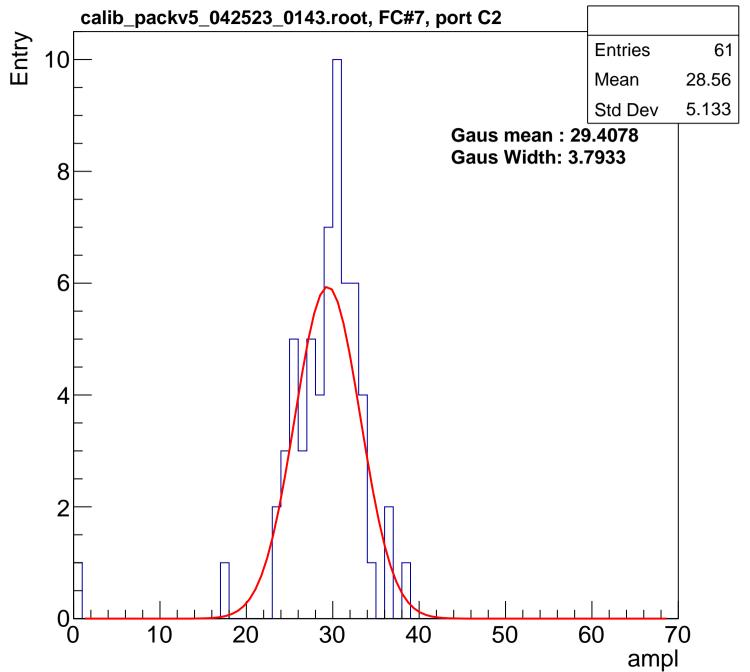


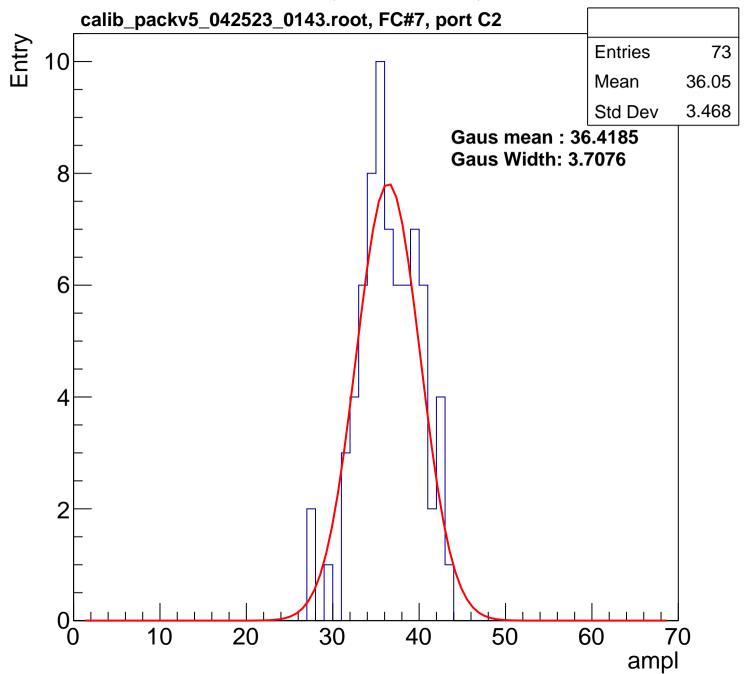


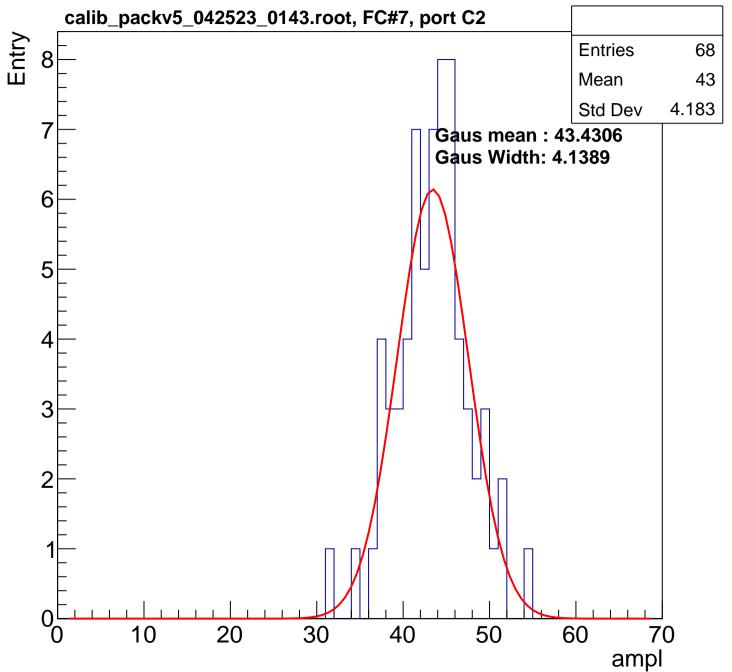


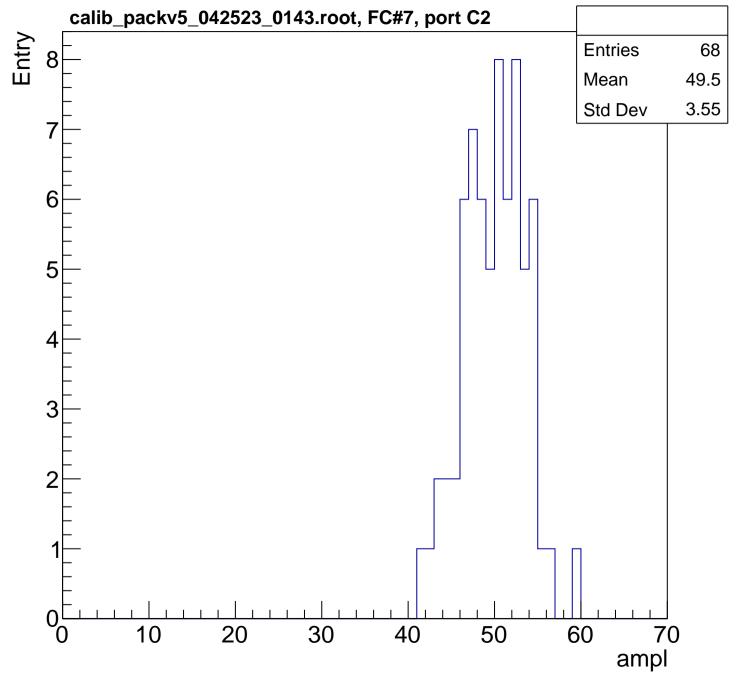


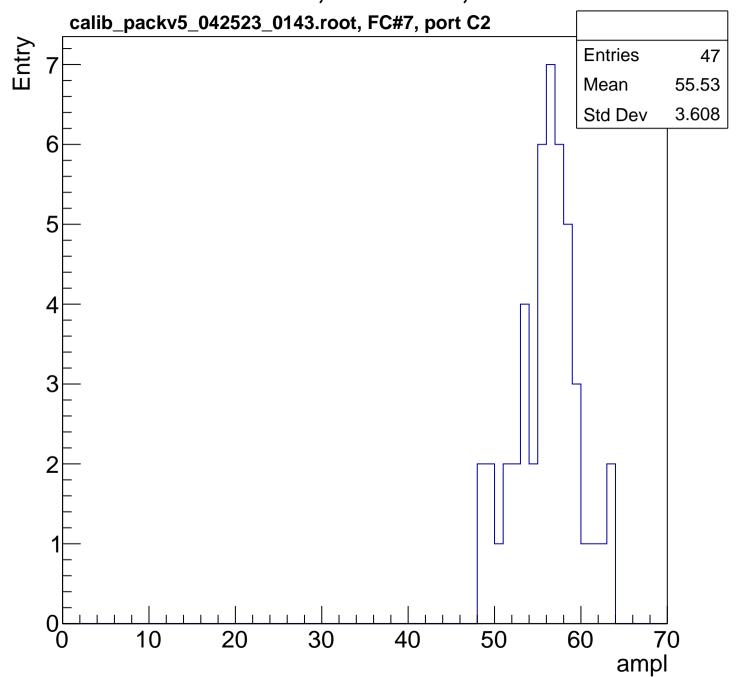
B1L103S, U4-ch72, adc7 calib_packv5_042523_0143.root, FC#7, port C2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

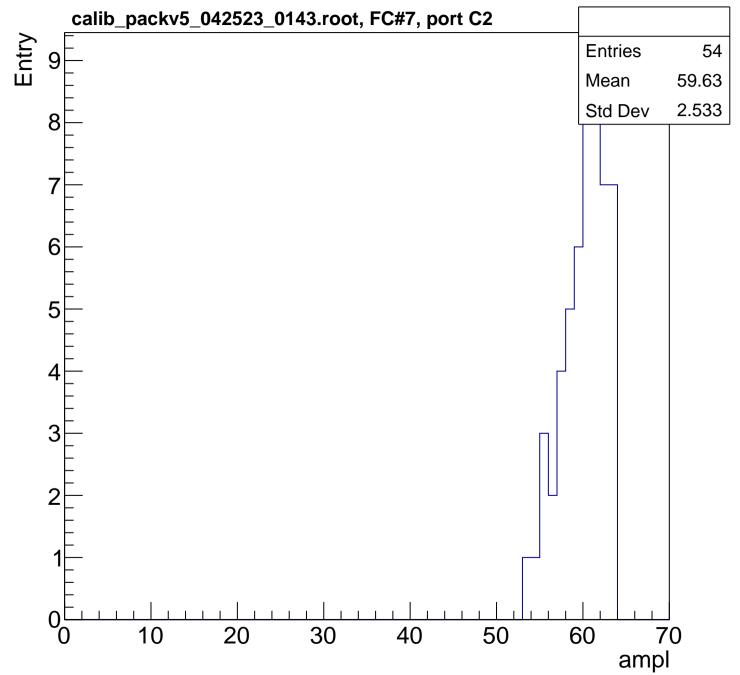


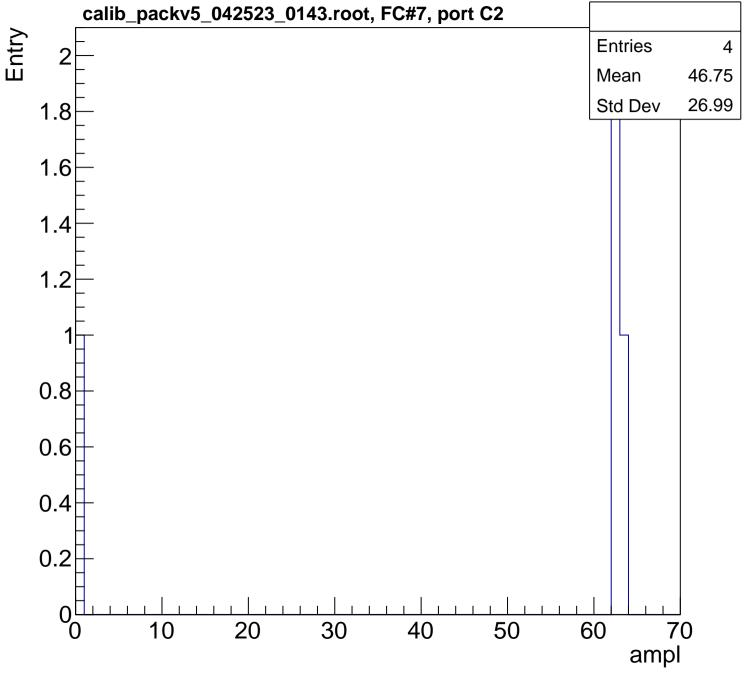




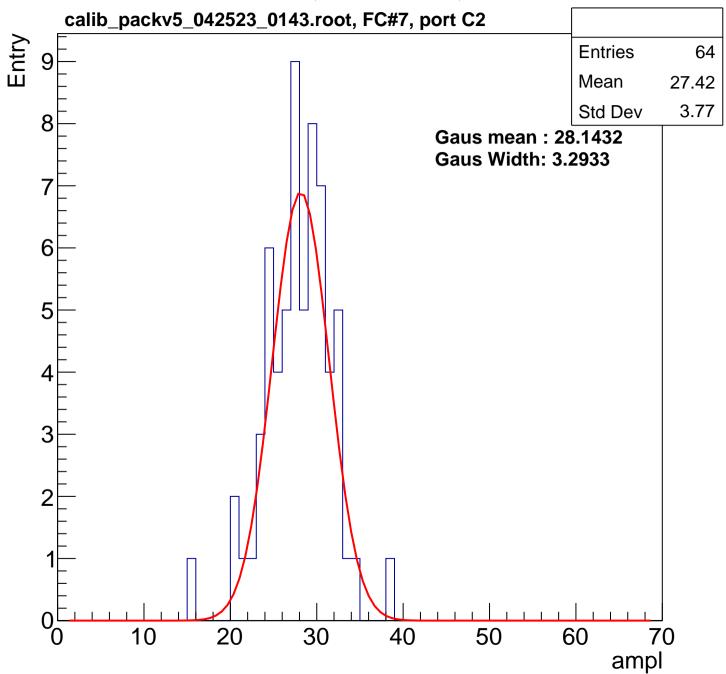


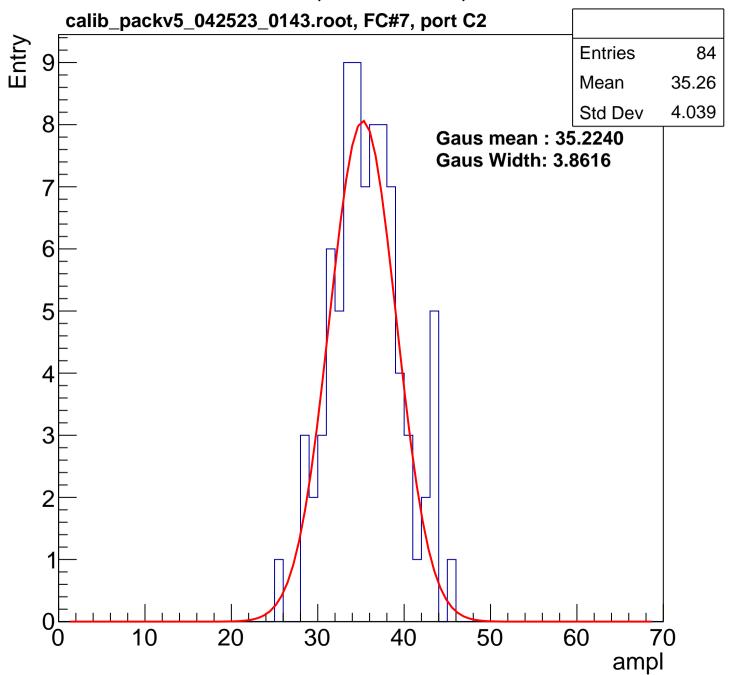


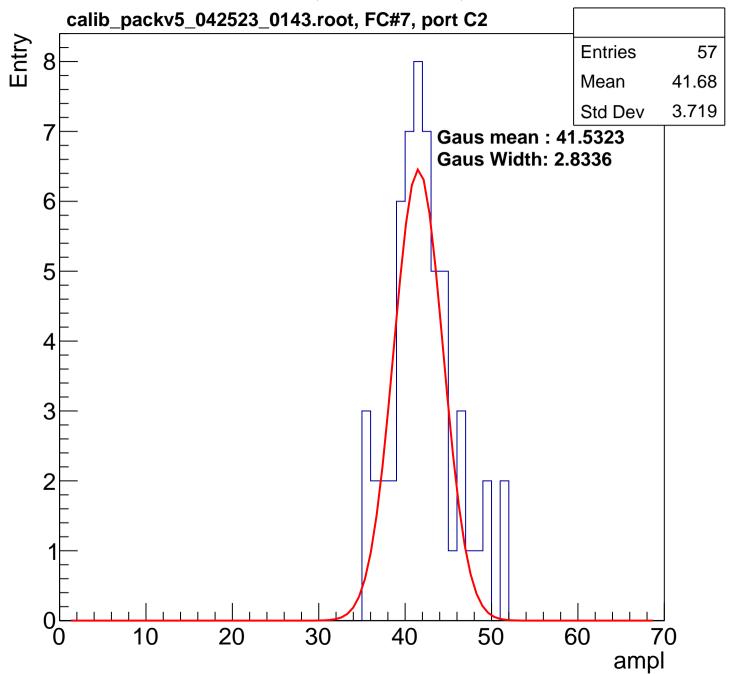


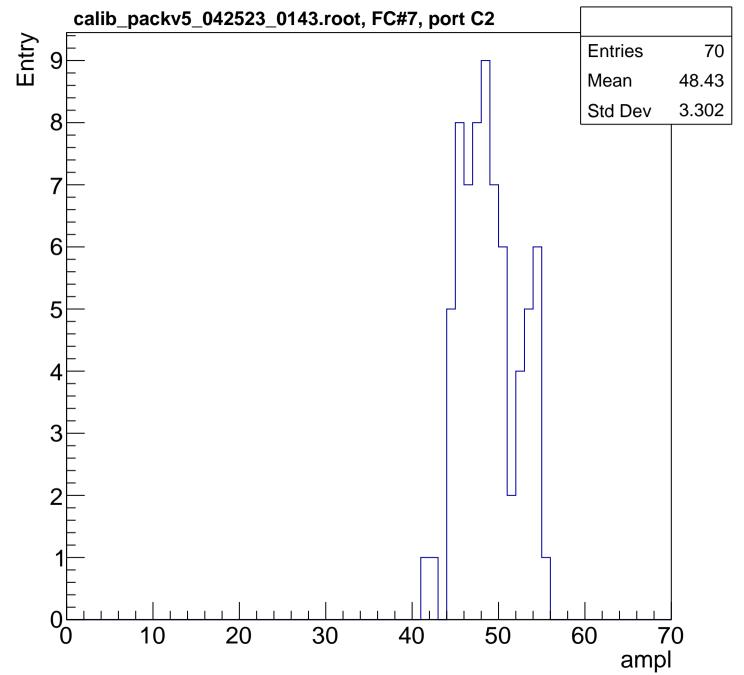


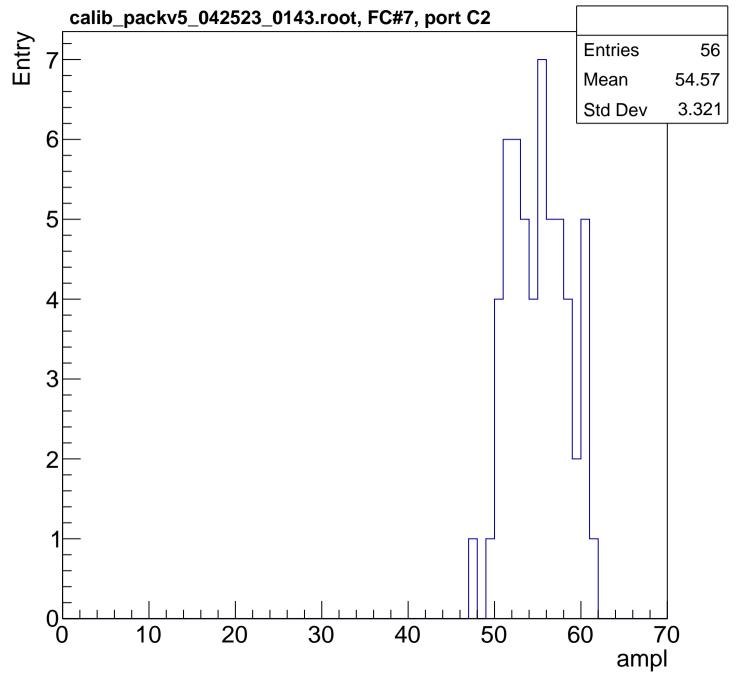
B1L103S, U4-ch73, adc7 calib_packv5_042523_0143.root, FC#7, port C2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

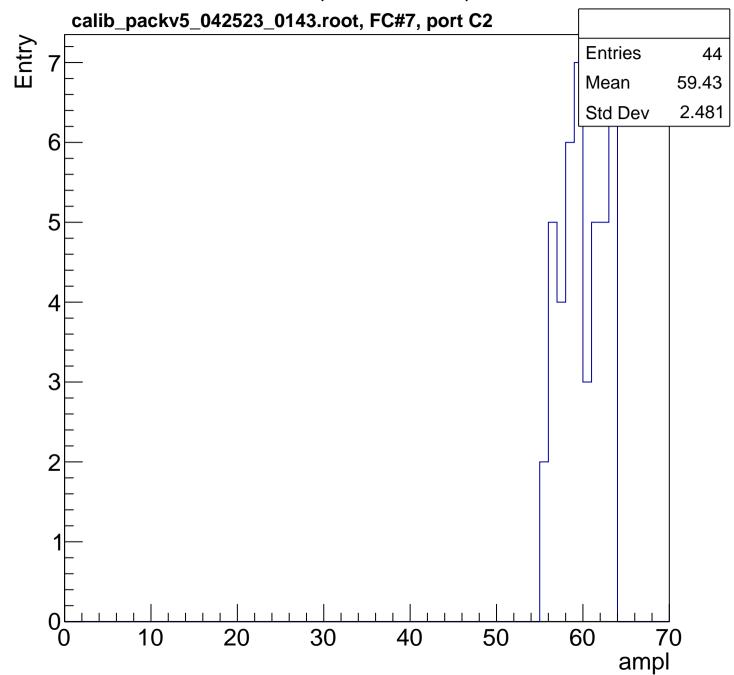


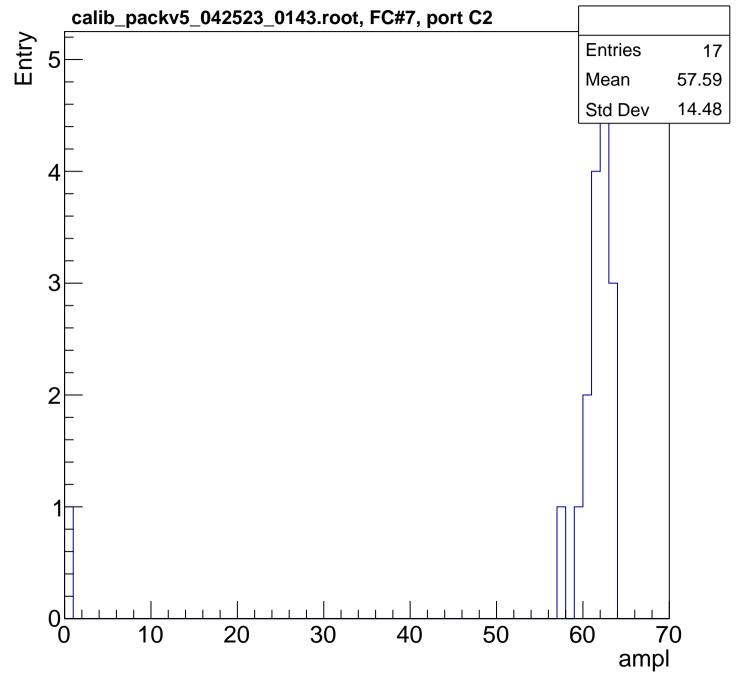


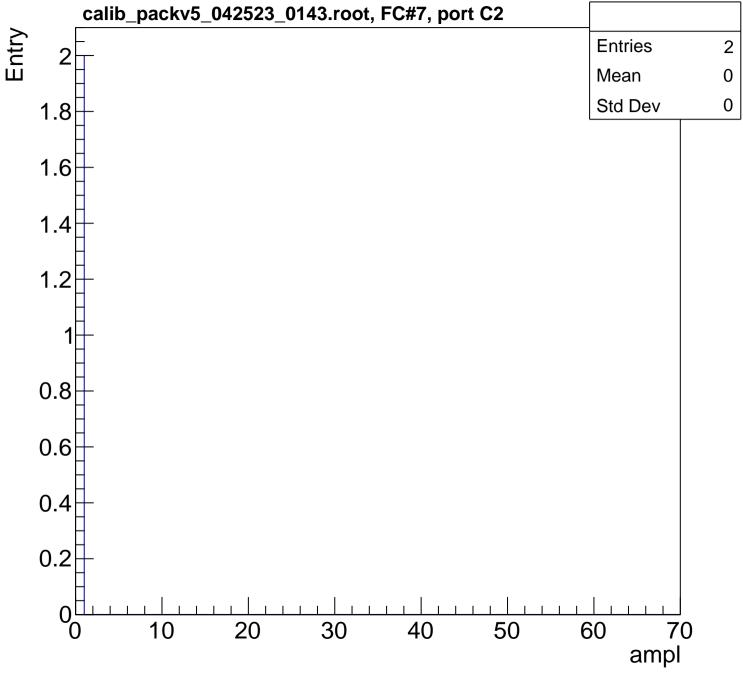


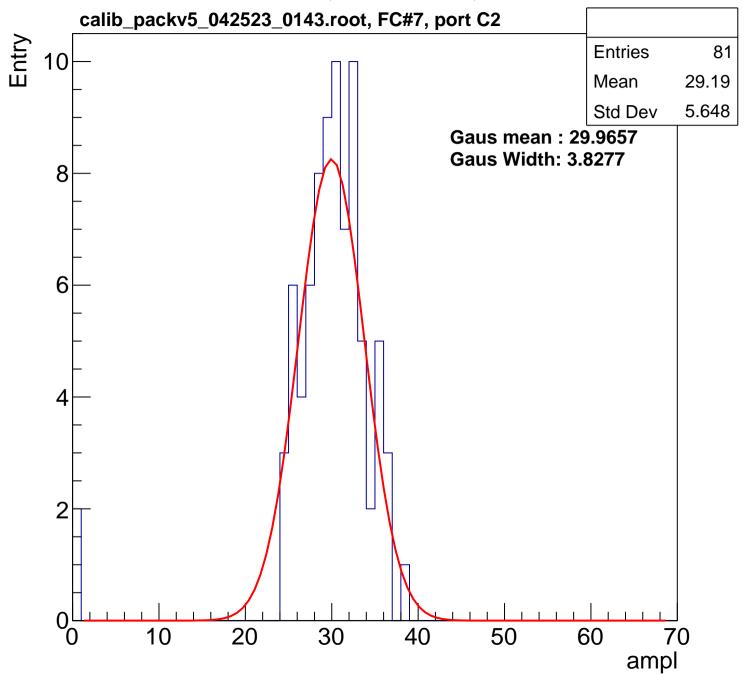


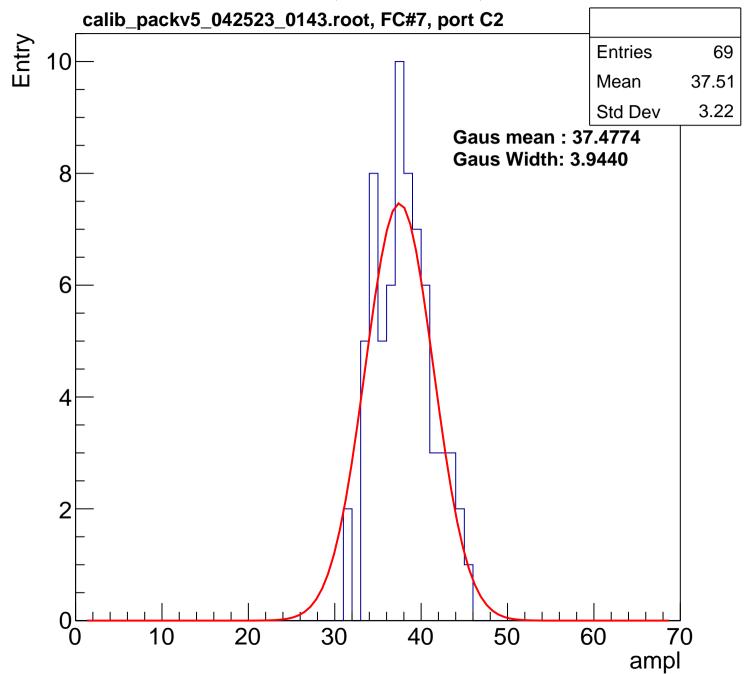


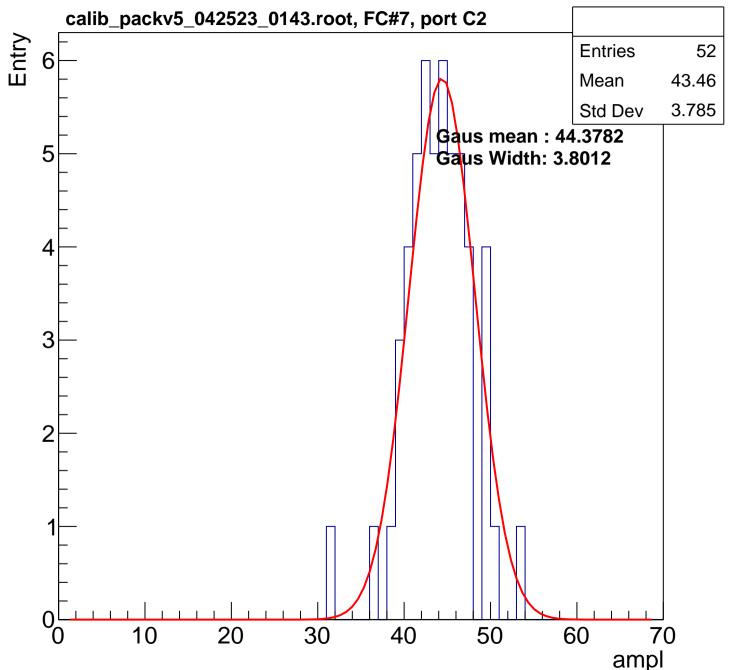




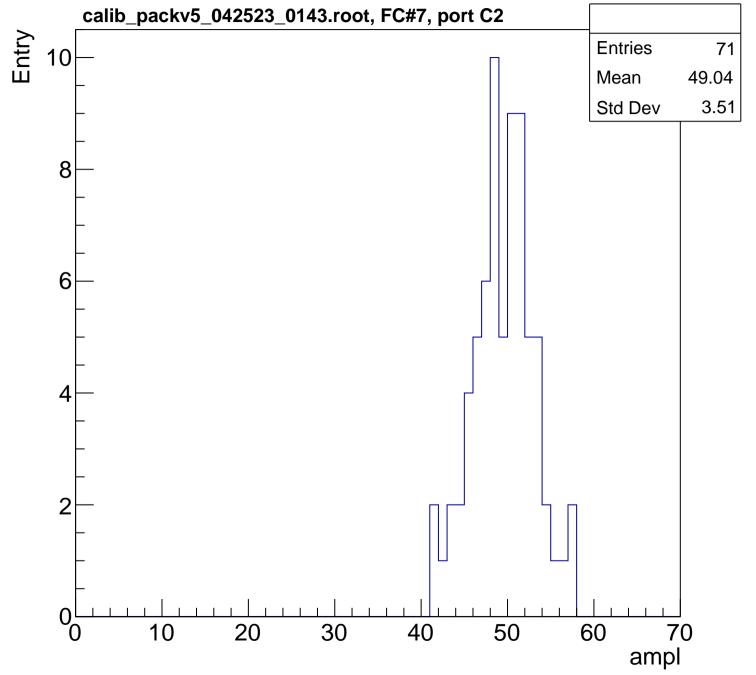


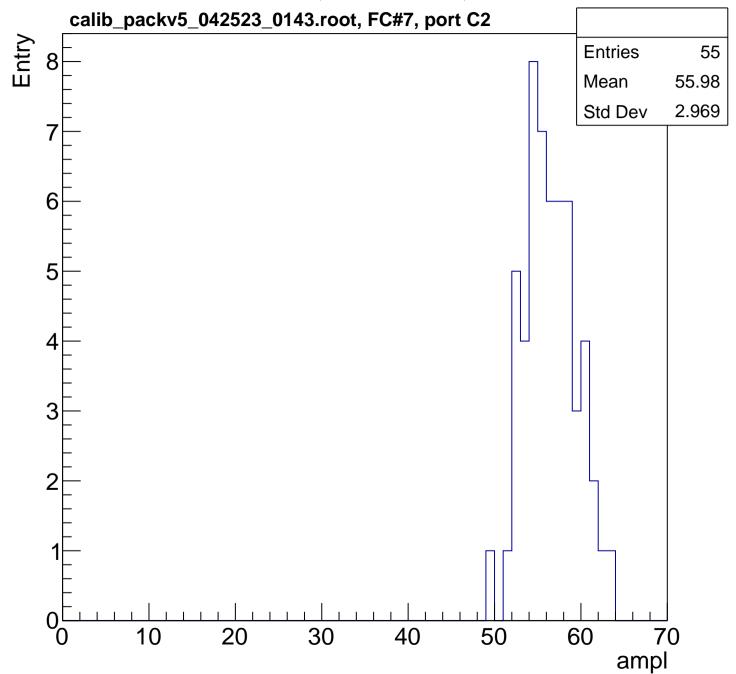


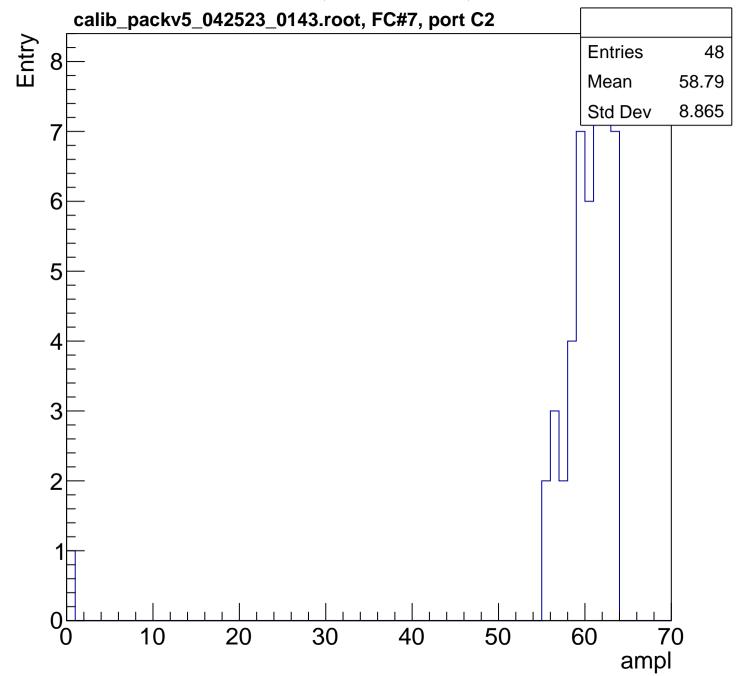


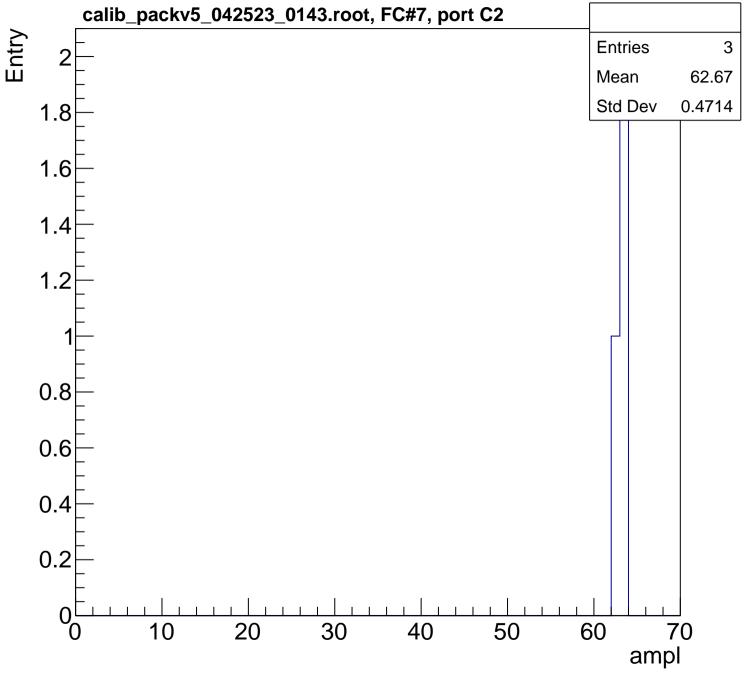


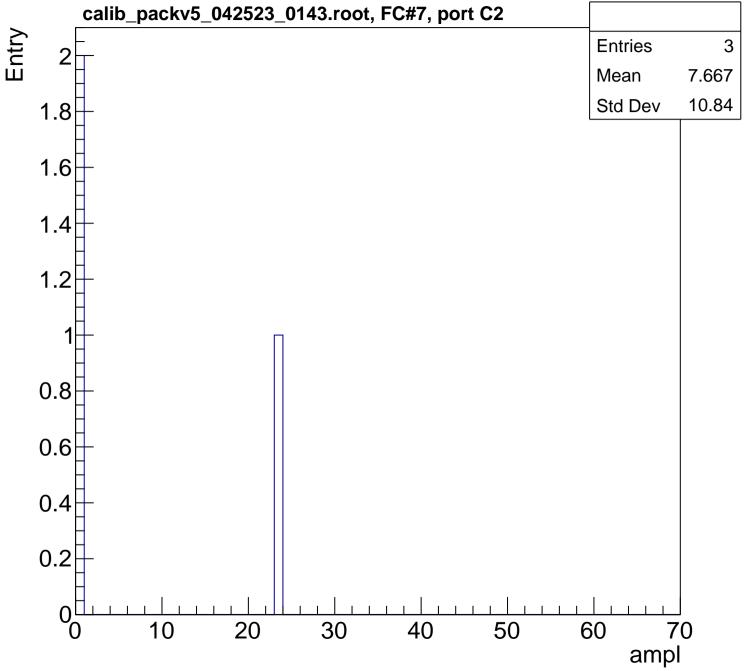
B1L103S, U4-ch75, adc3

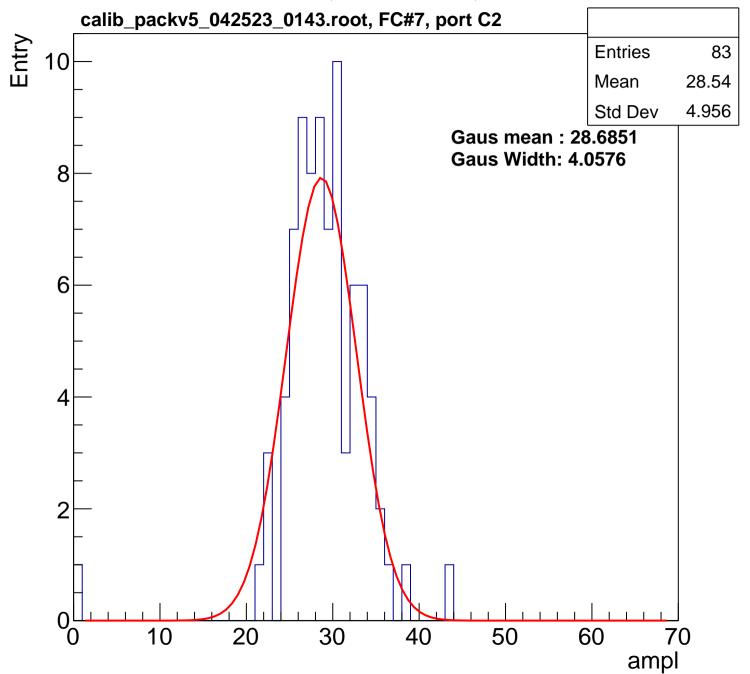


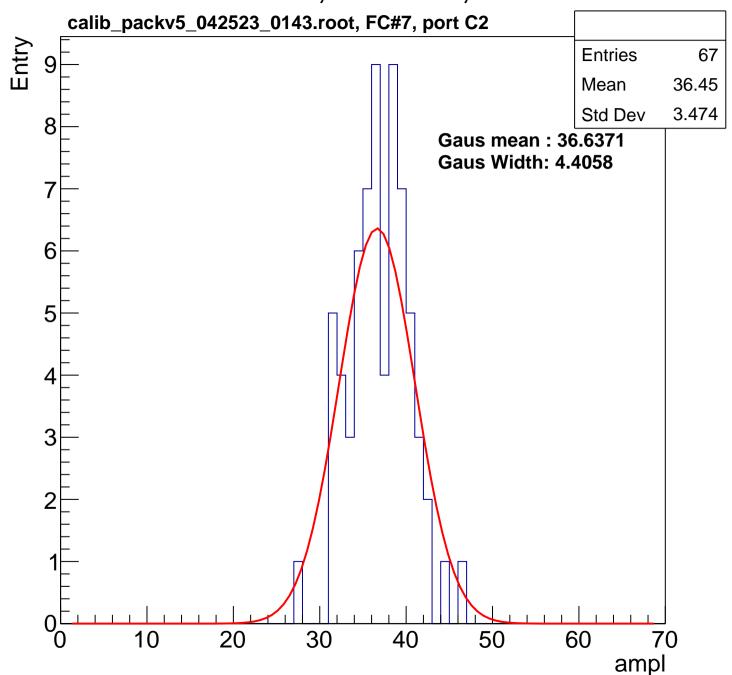


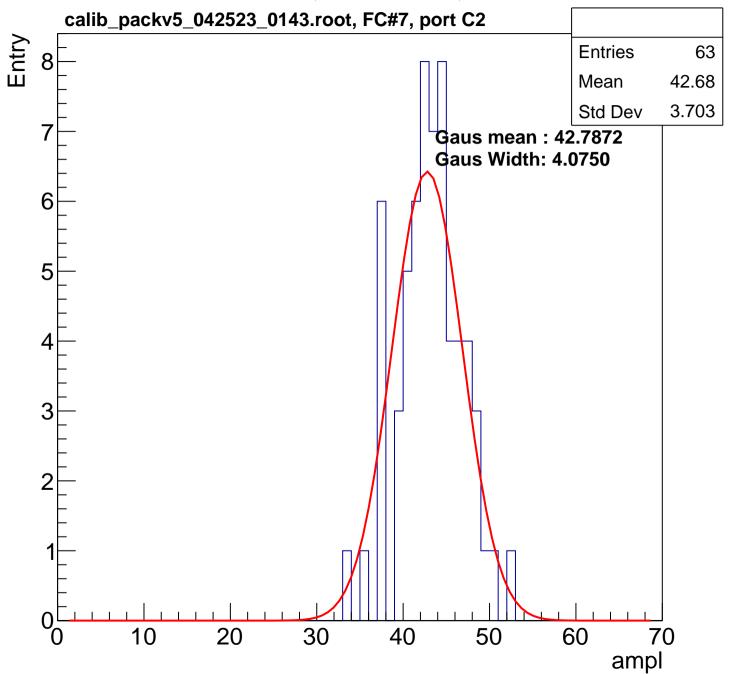


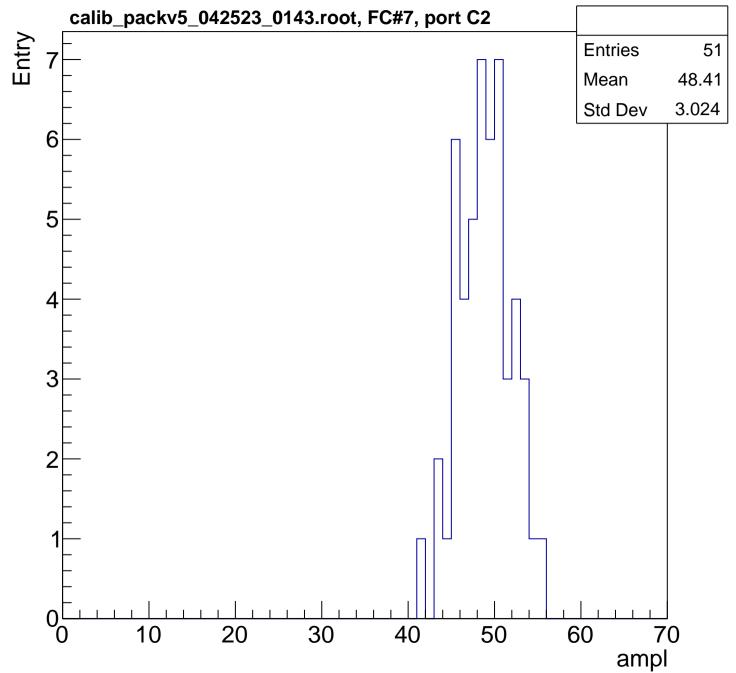


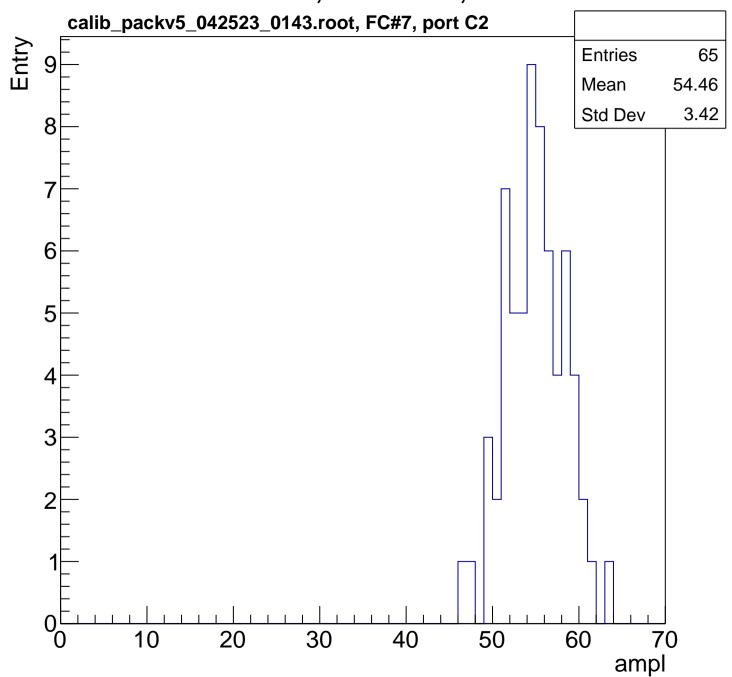


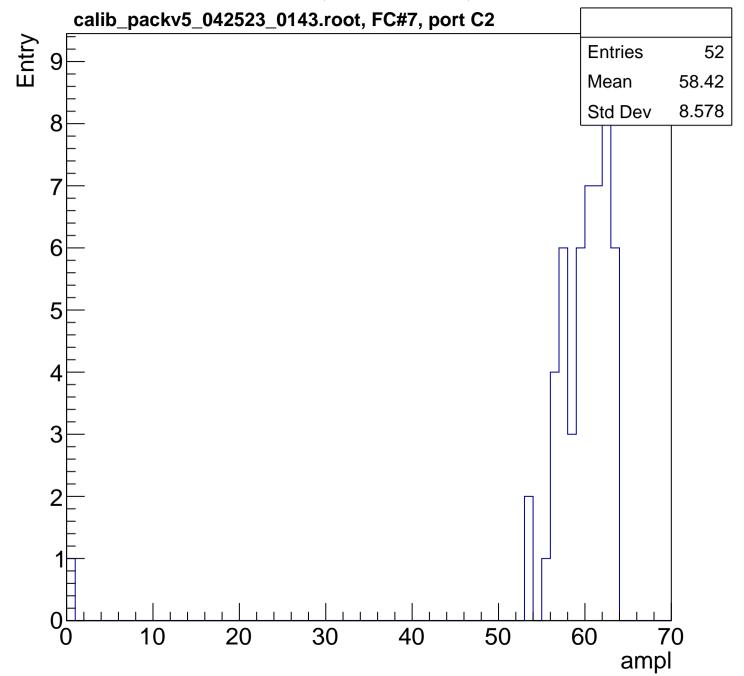


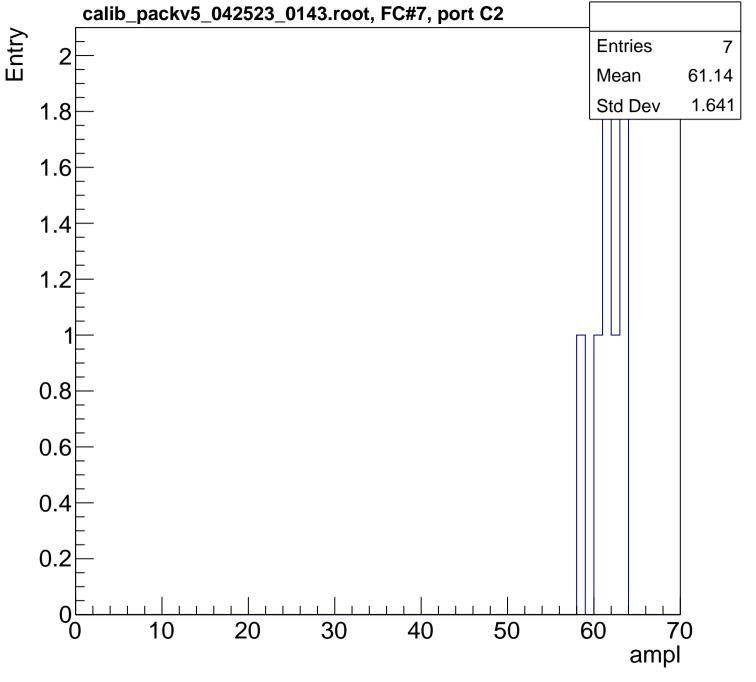


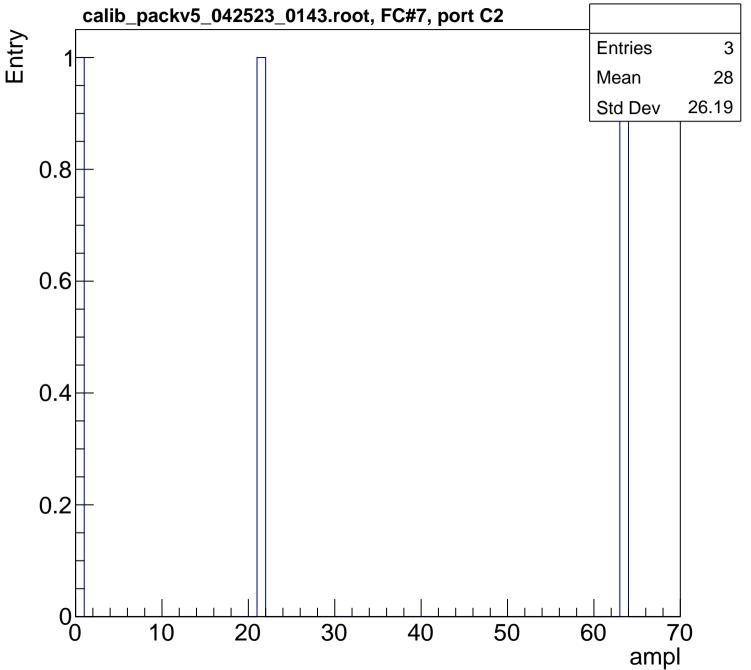


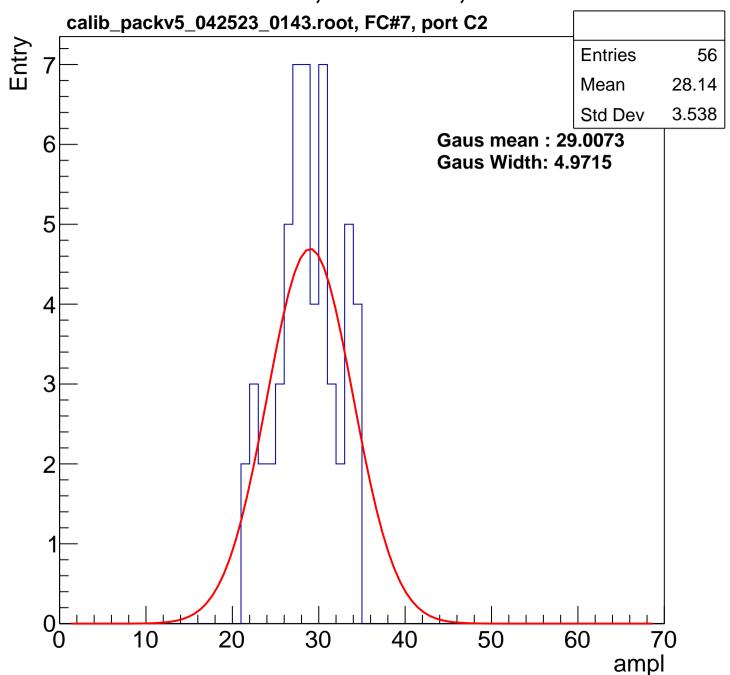


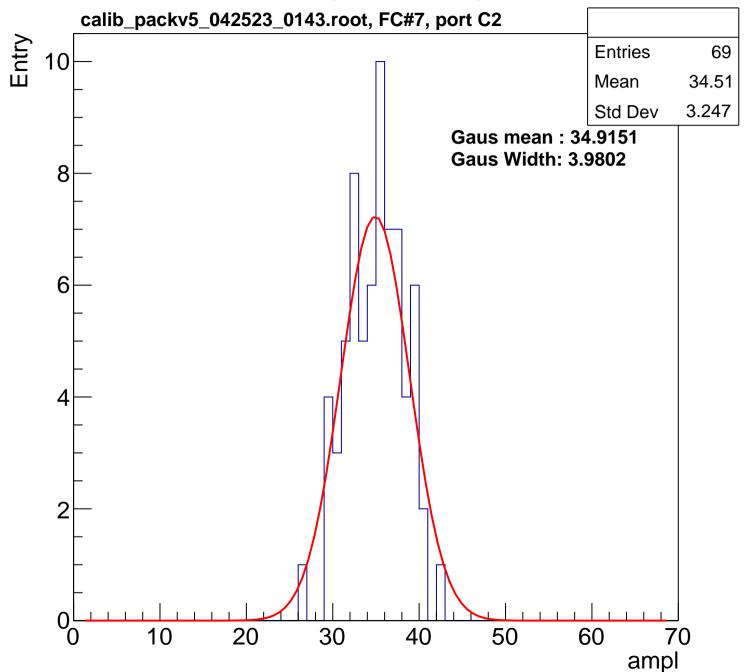


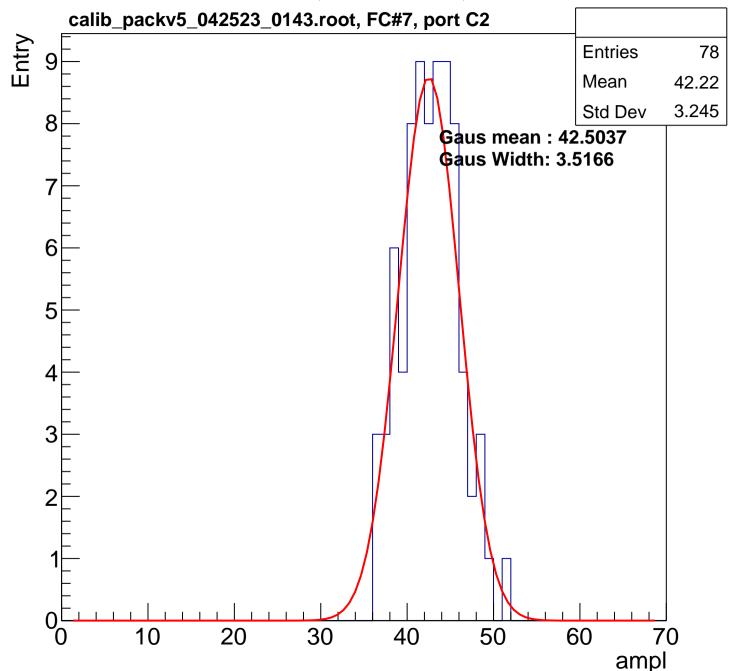


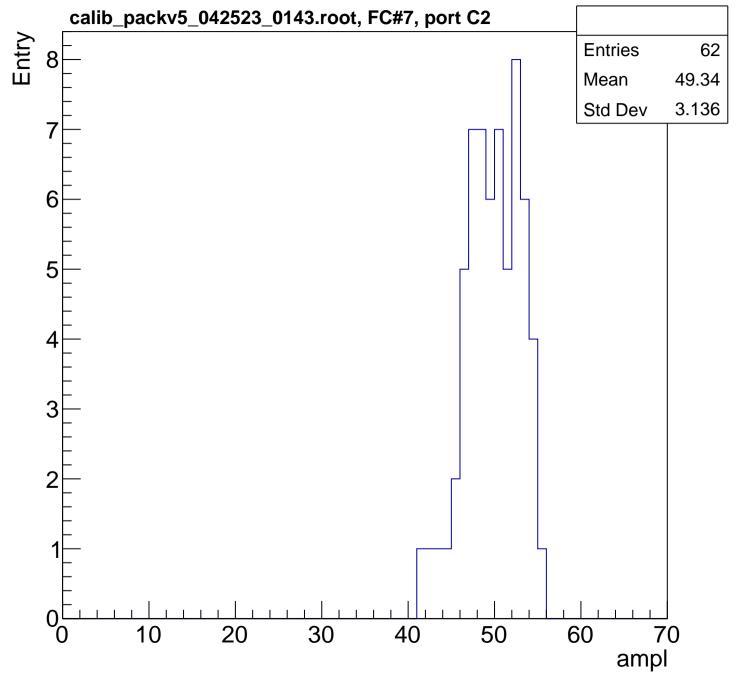


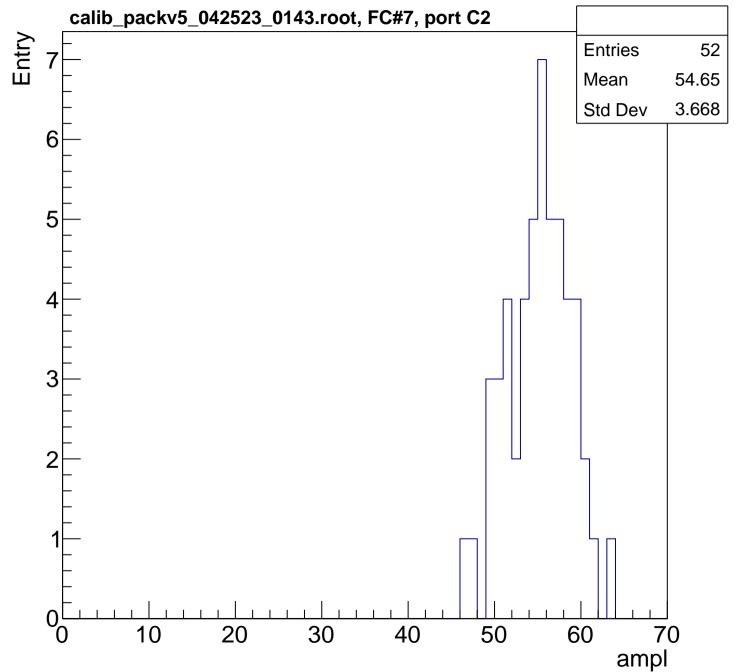


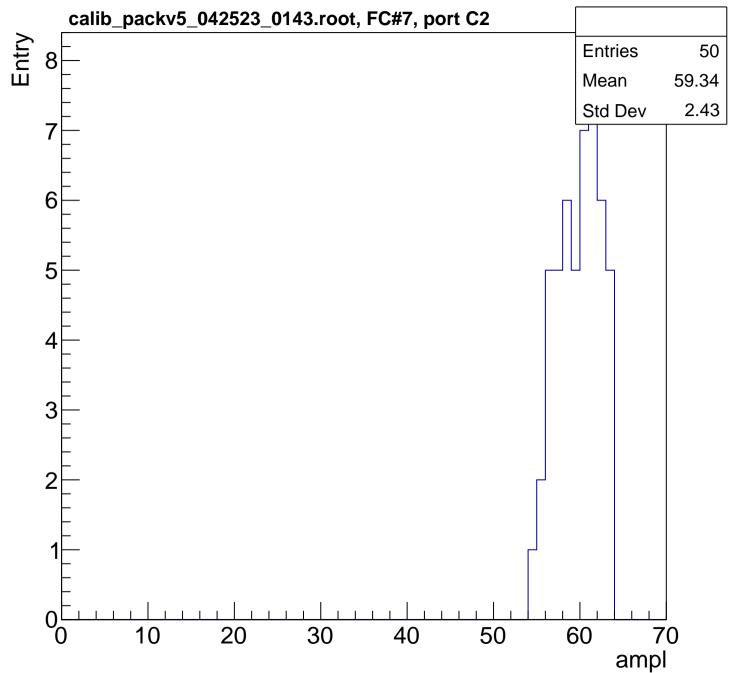


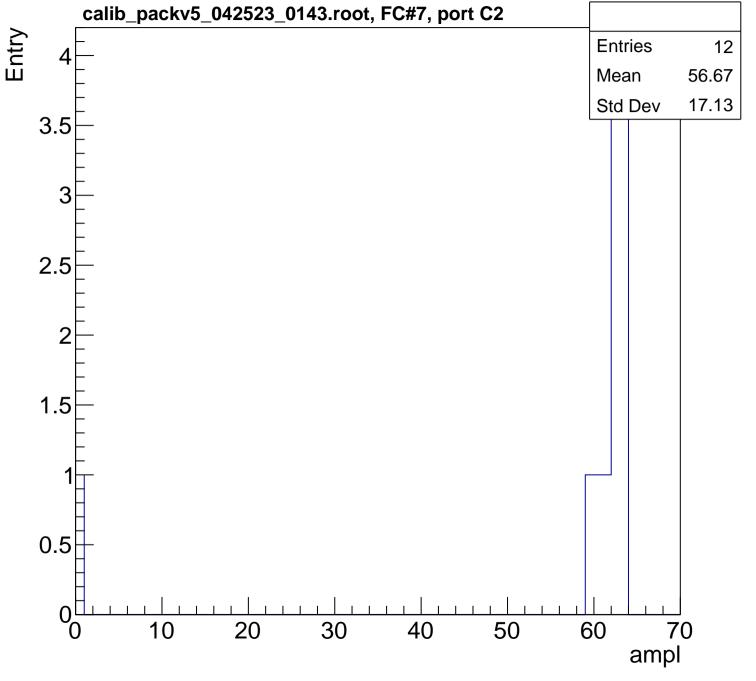


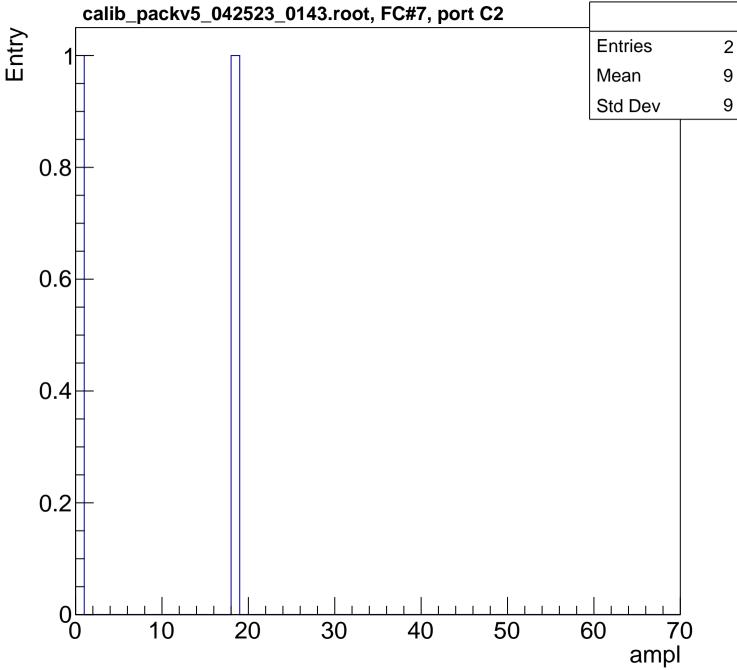


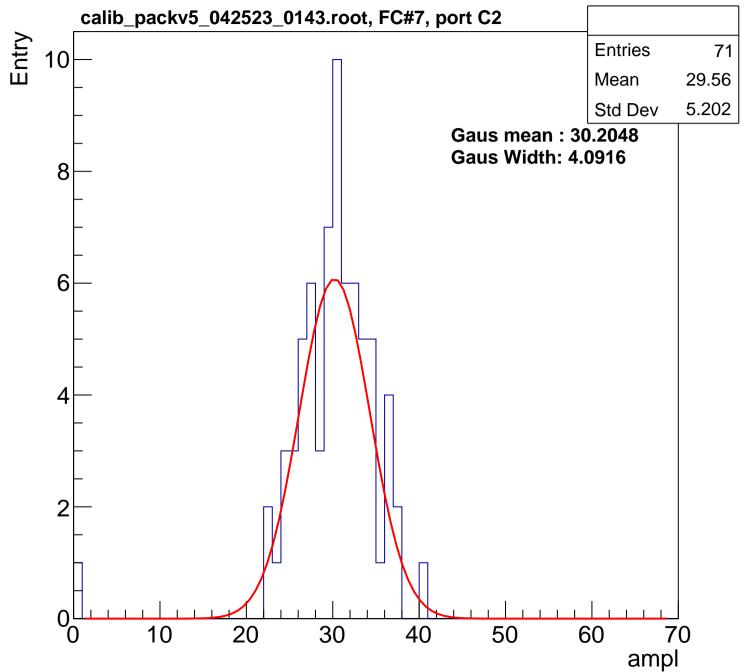


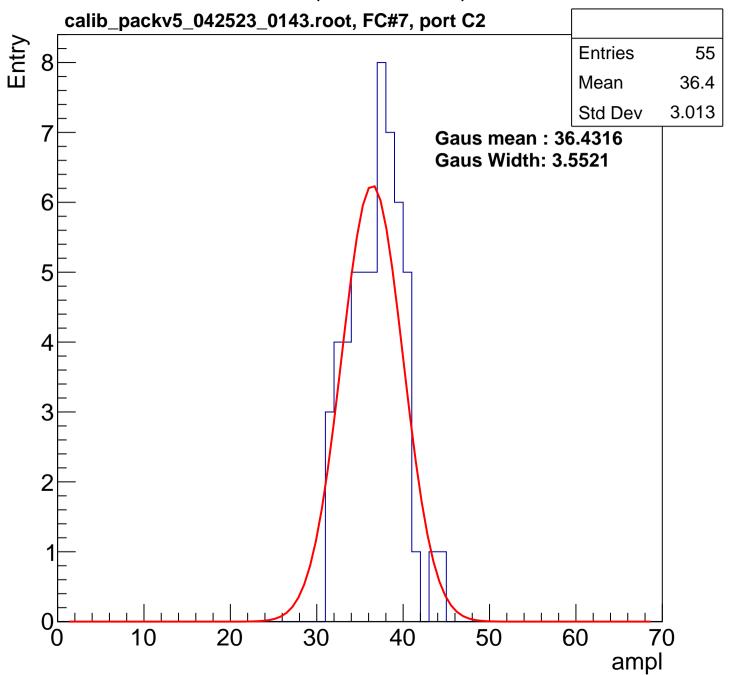


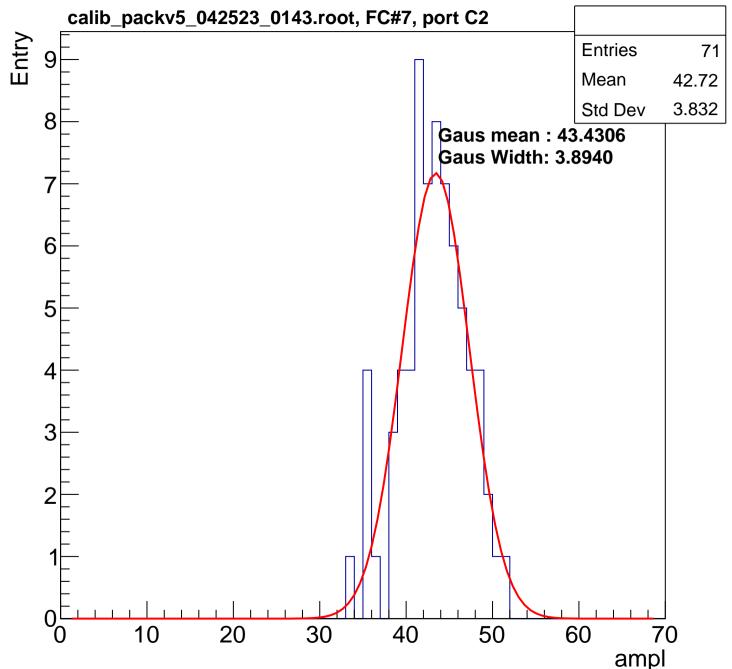


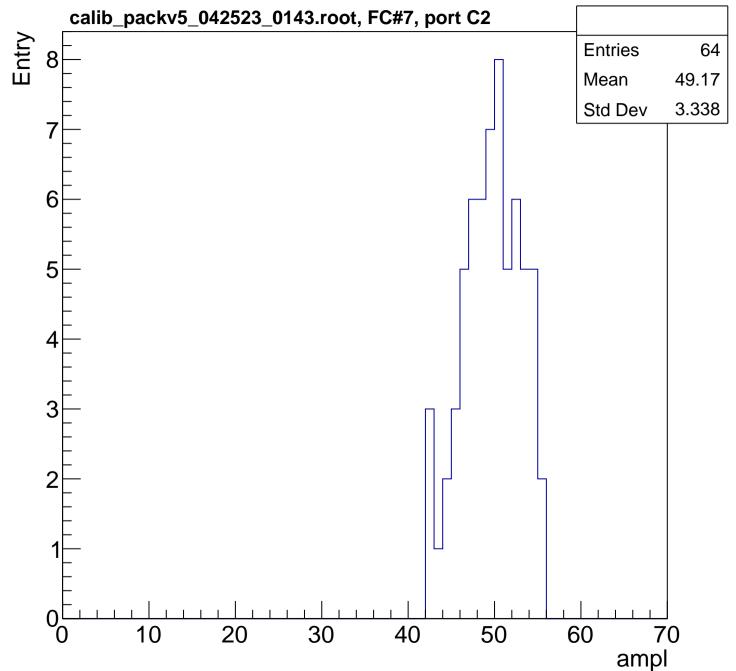


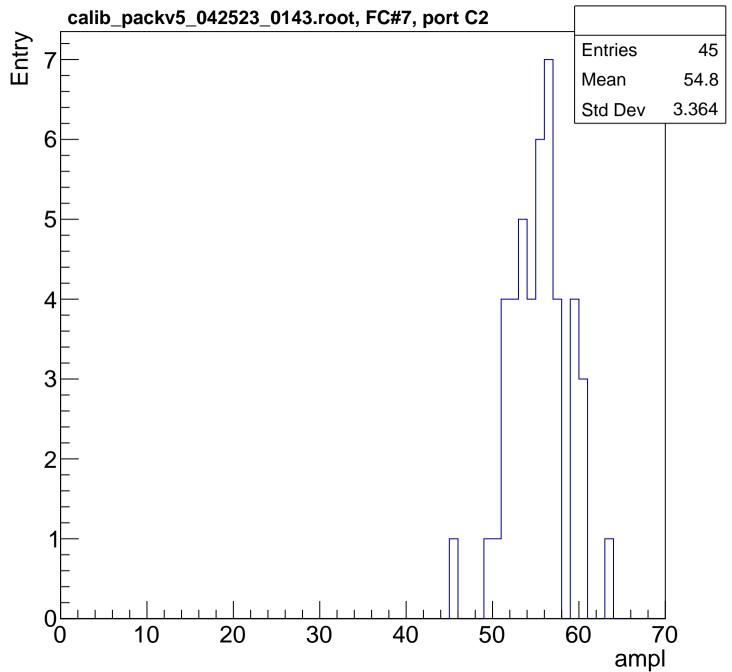


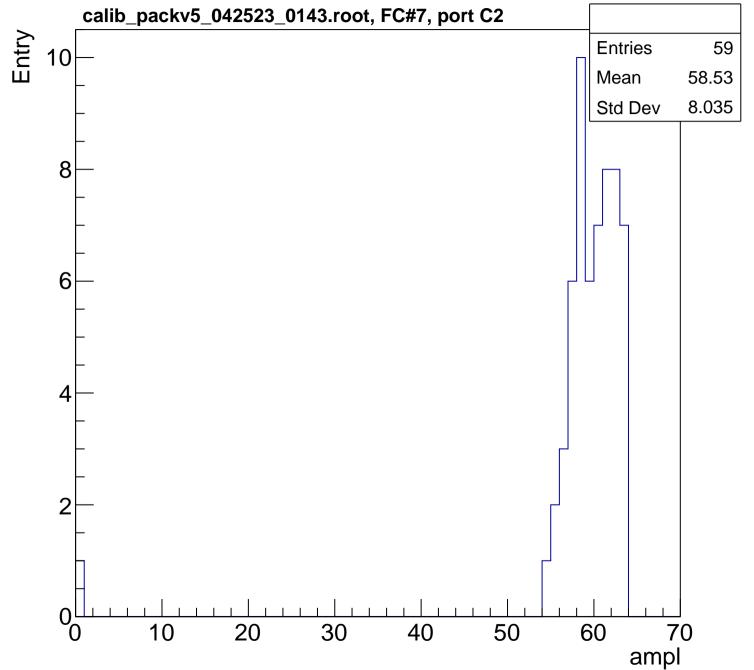


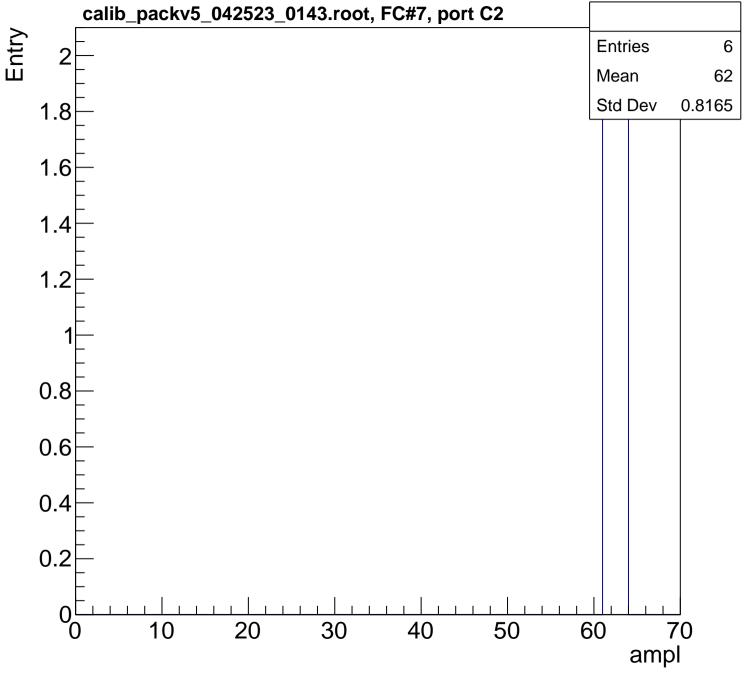




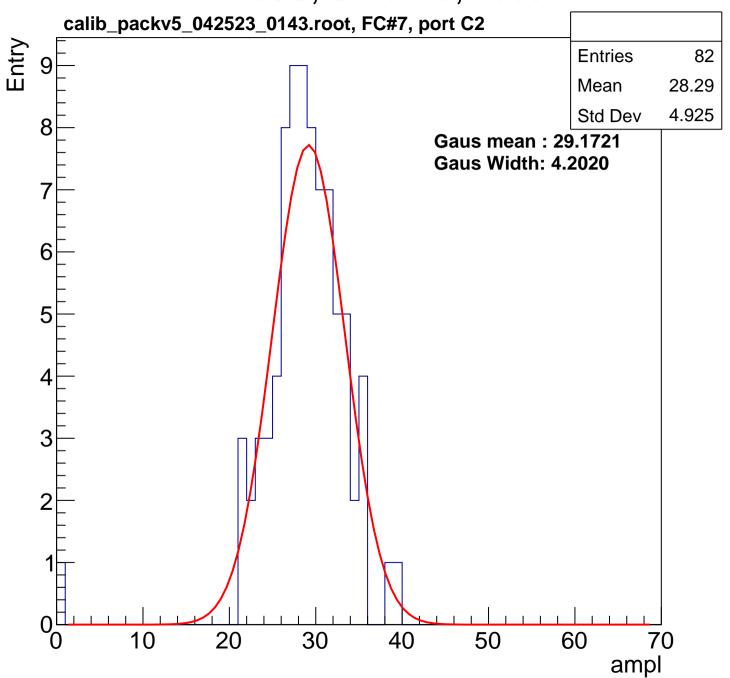


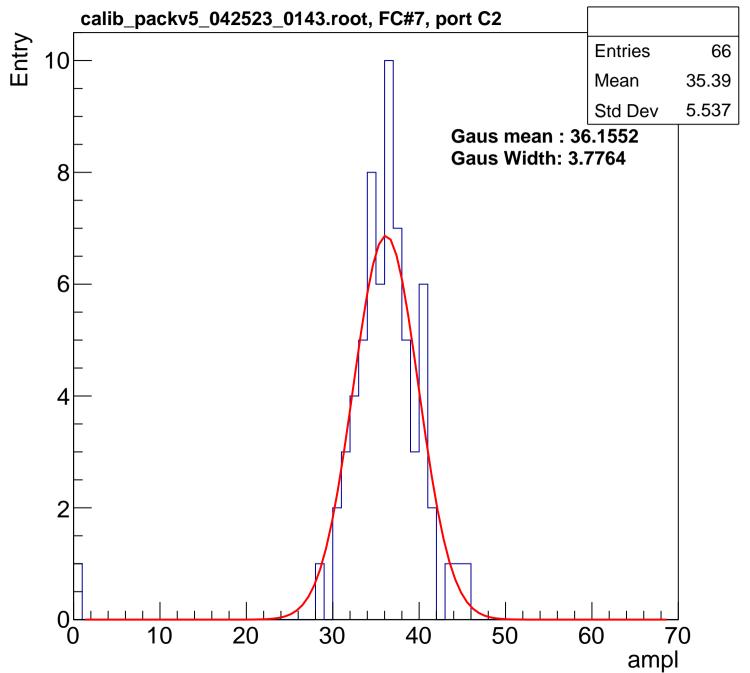


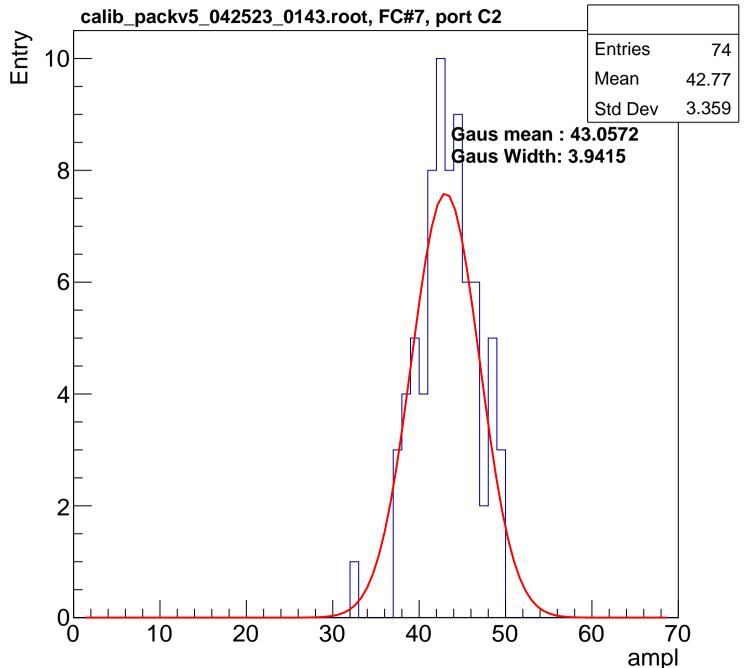


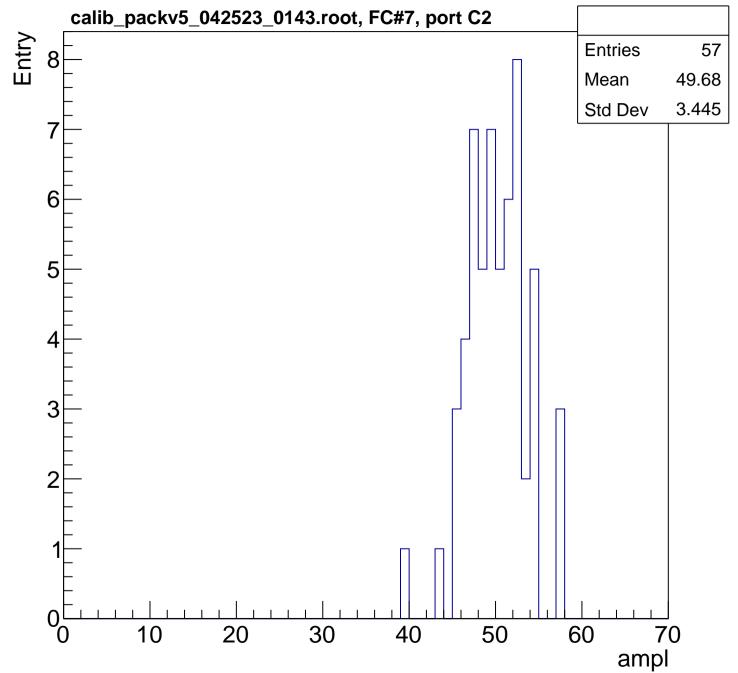


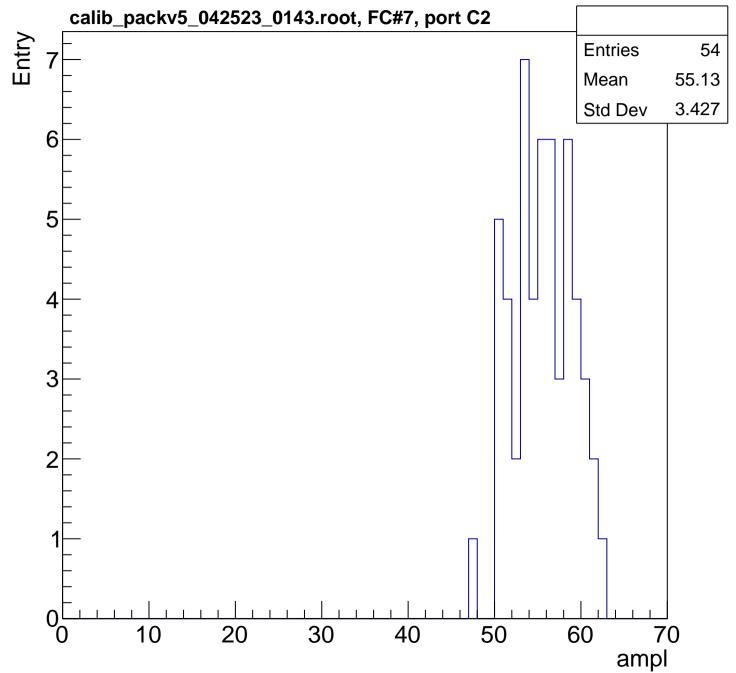
B1L103S, U4-ch78, adc7 calib_packv5_042523_0143.root, FC#7, port C2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

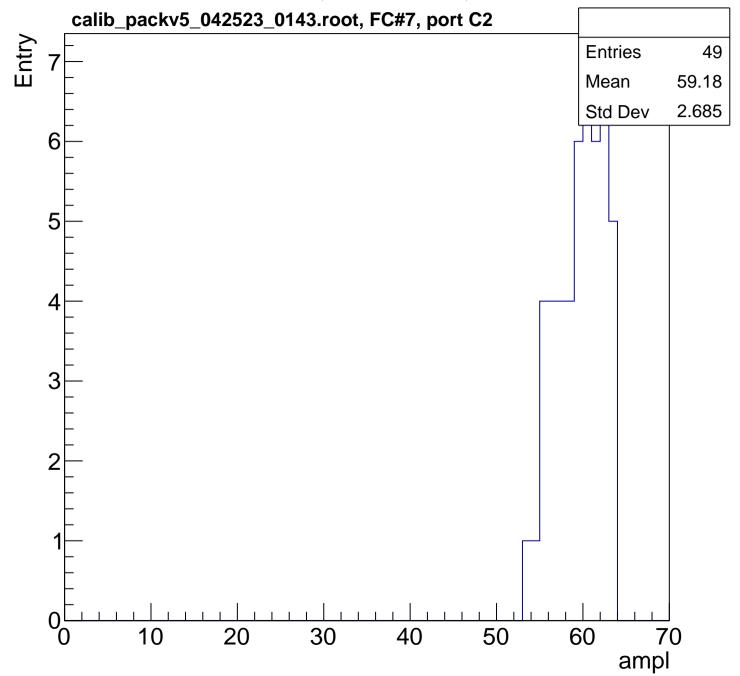


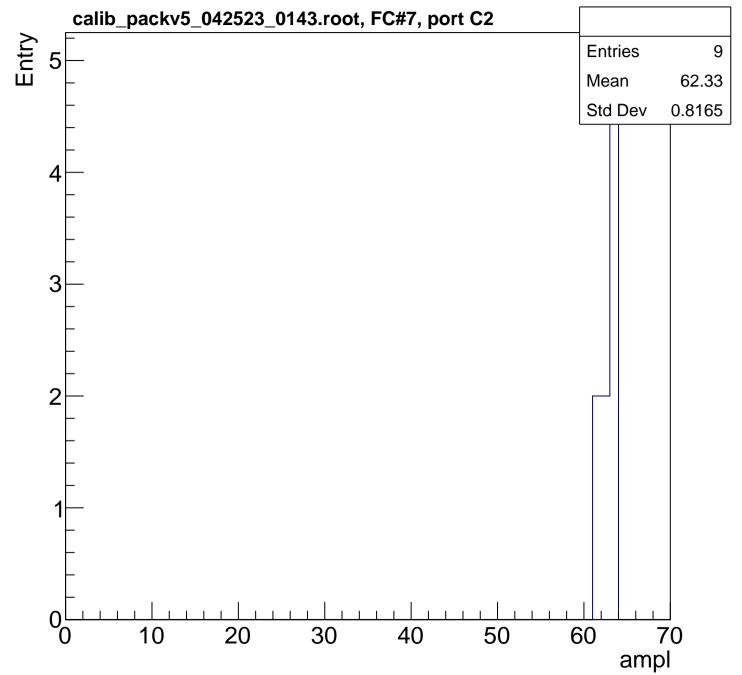


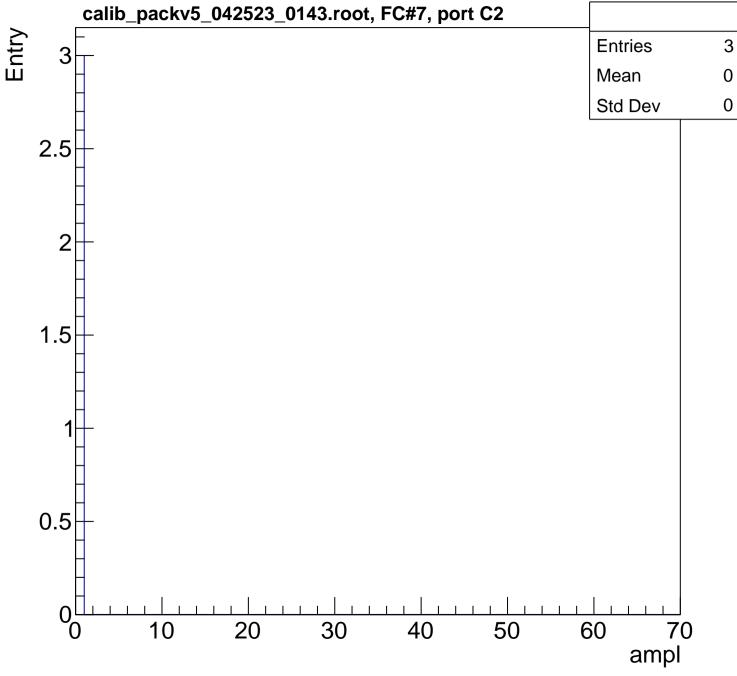


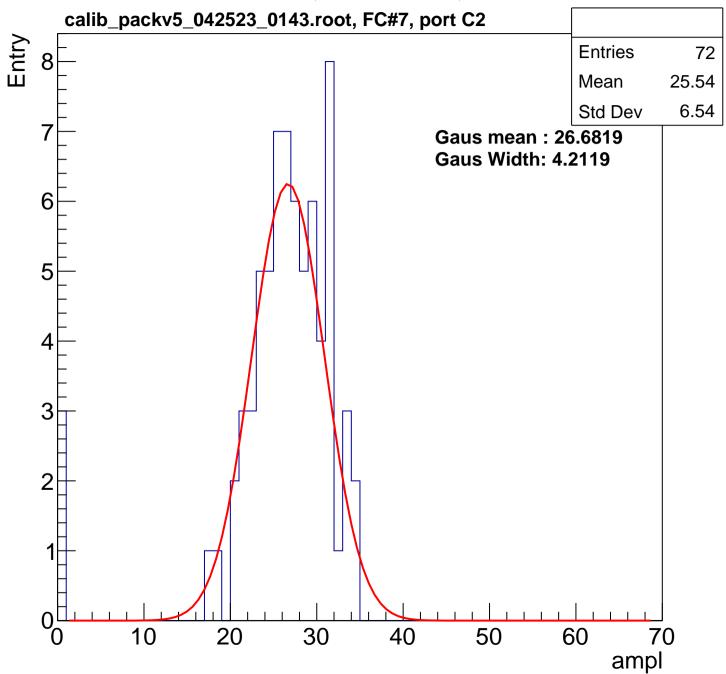


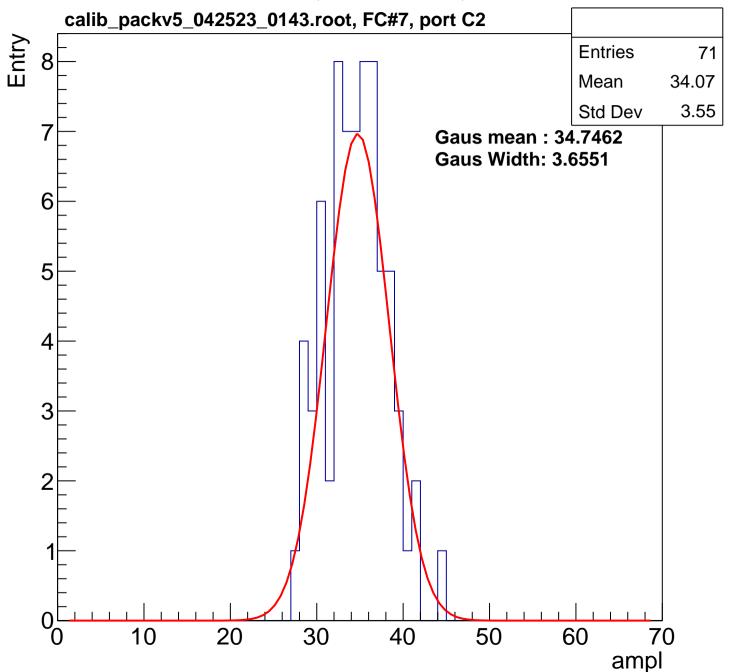


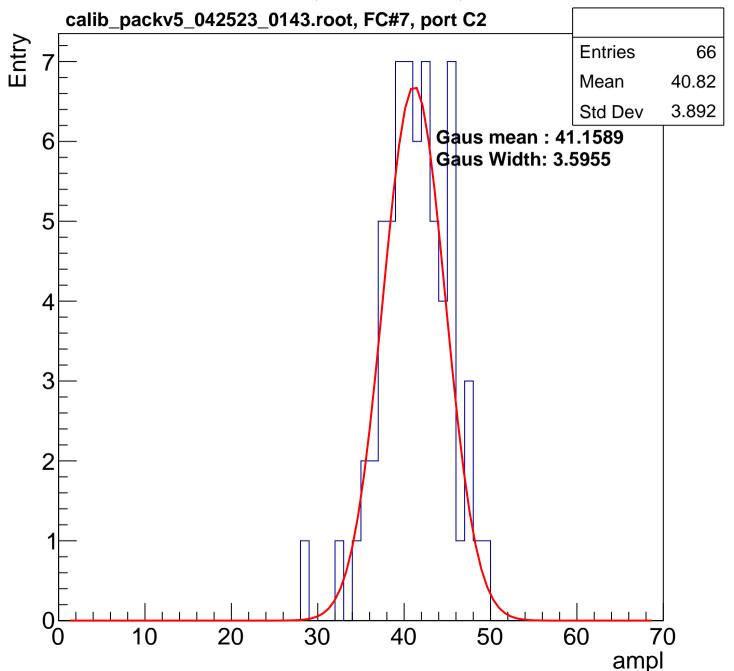


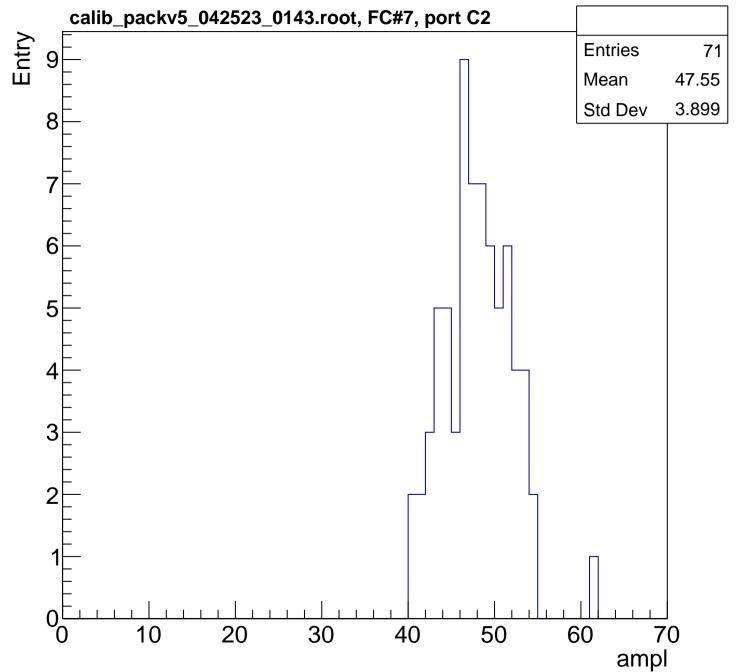


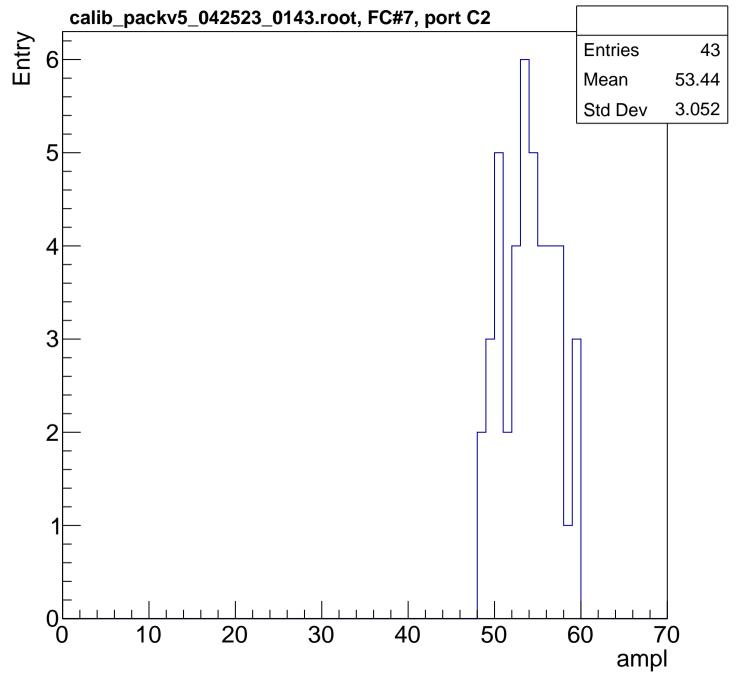


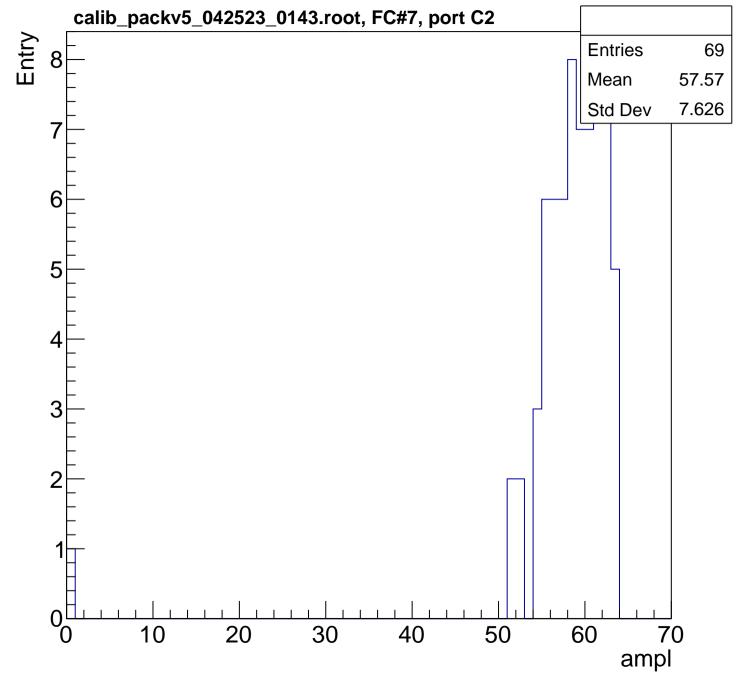


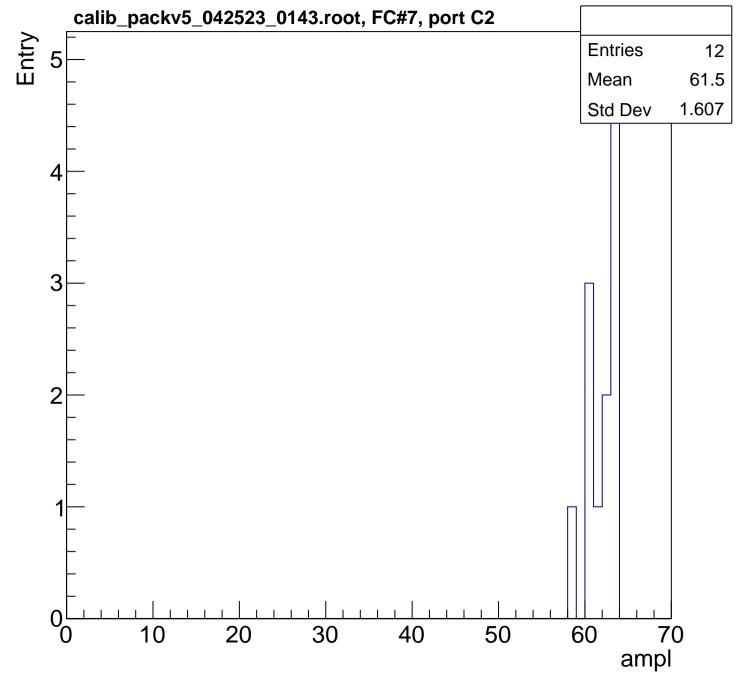


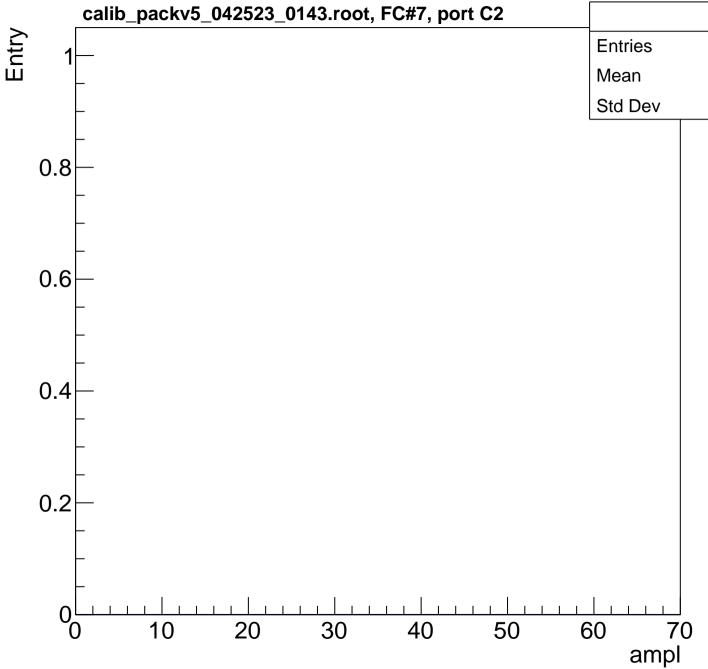


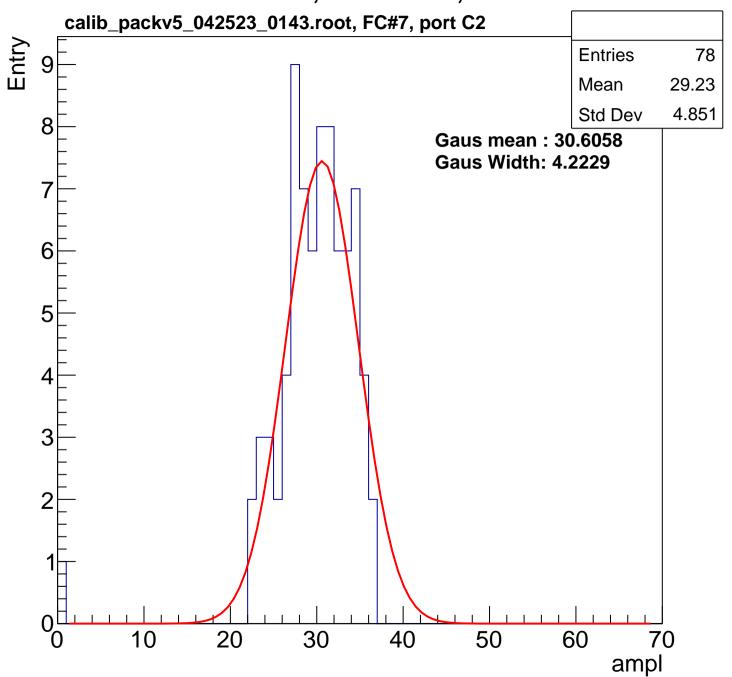


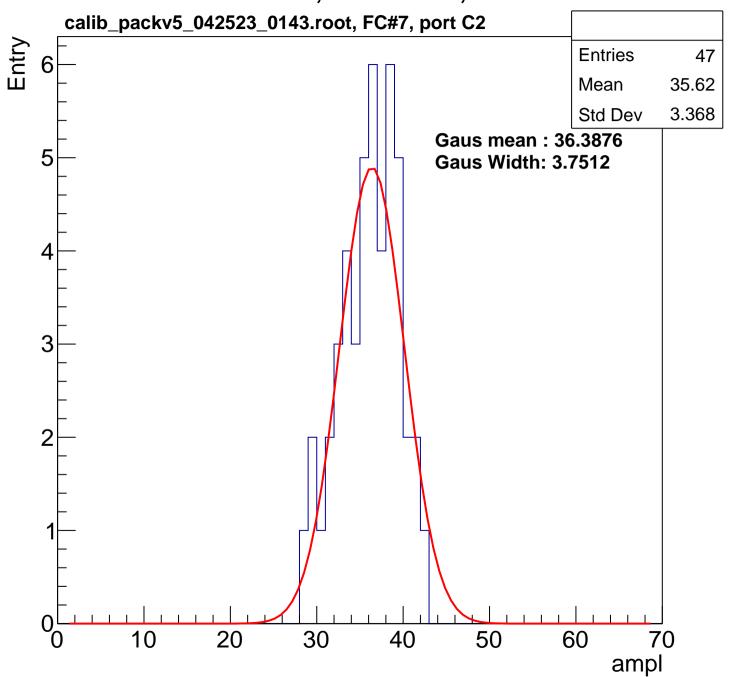


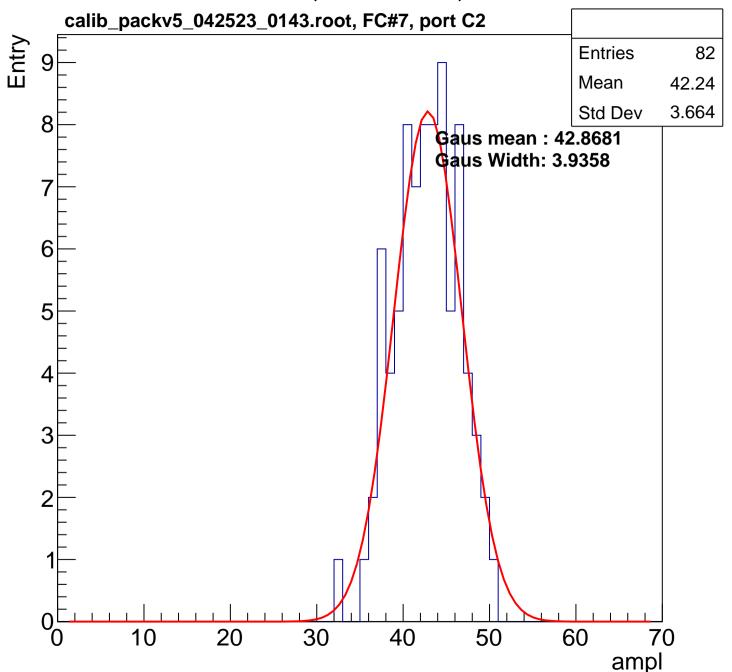


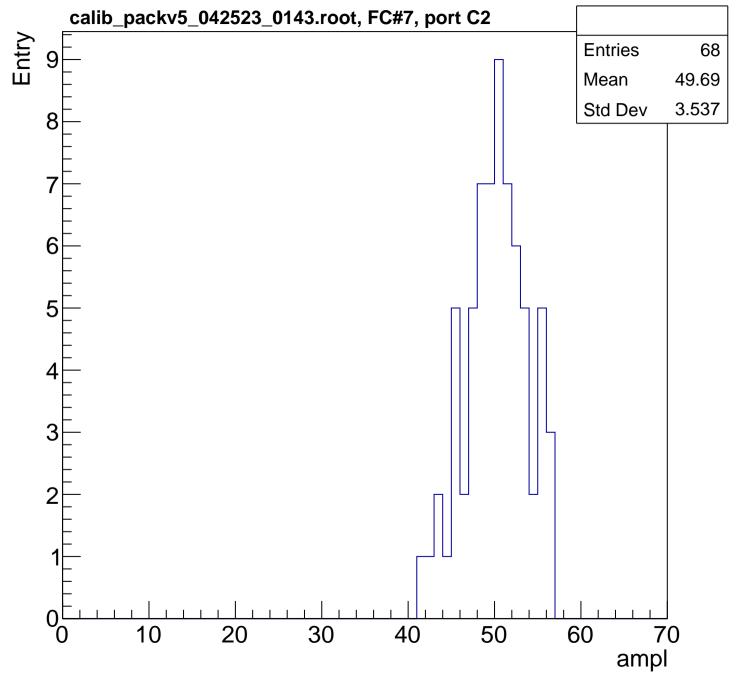


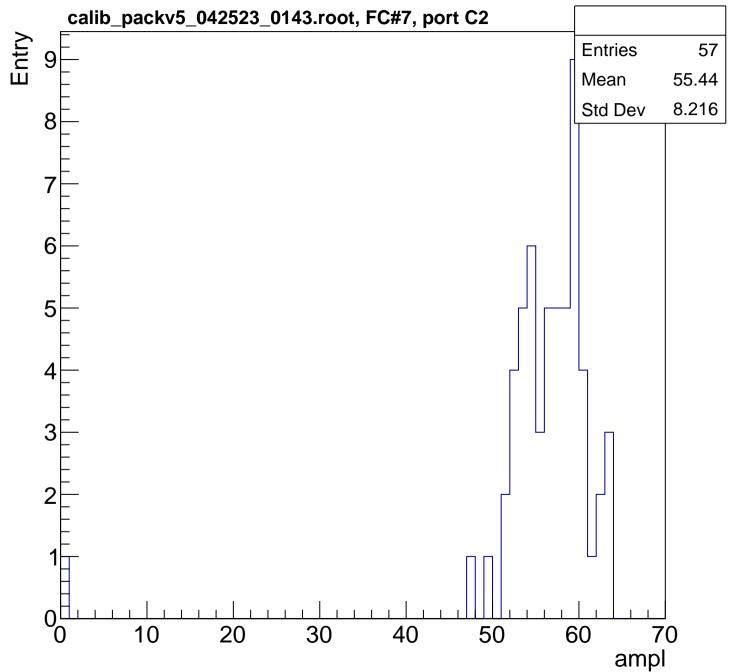


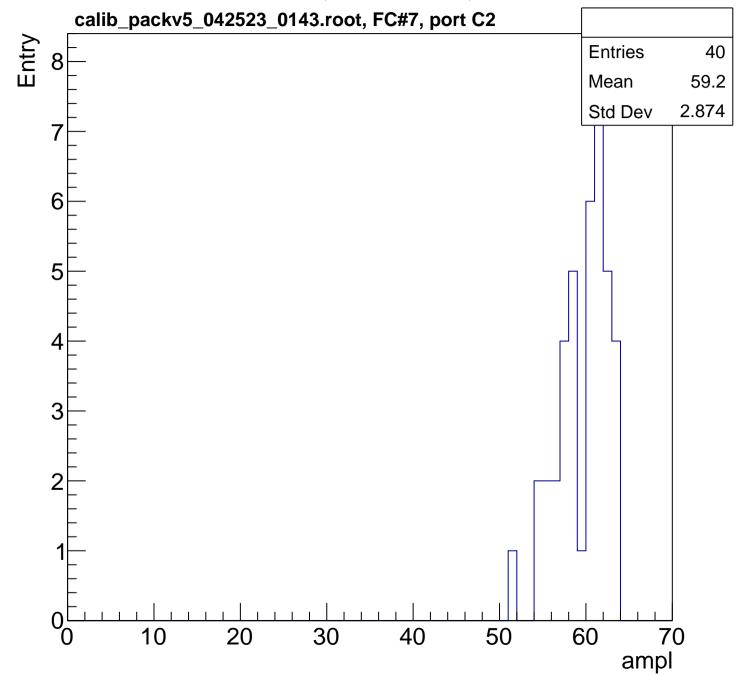


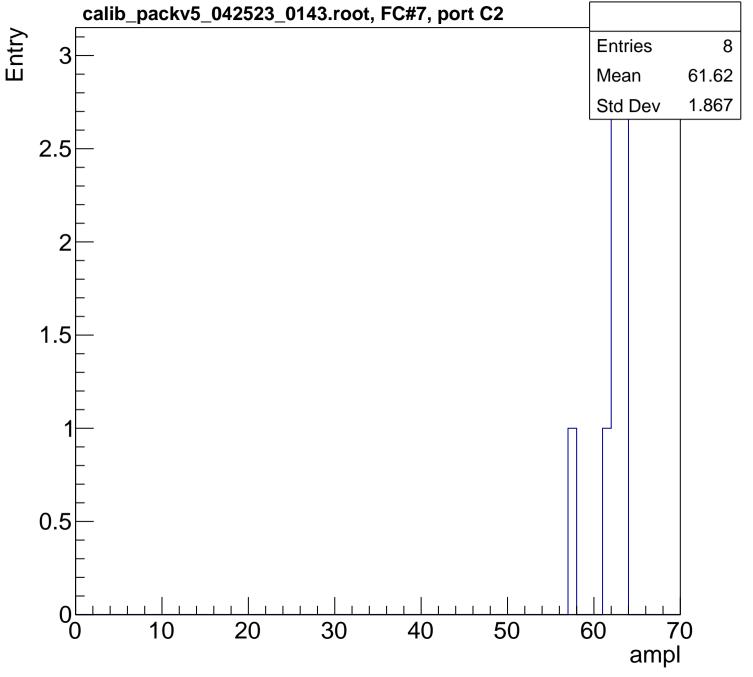


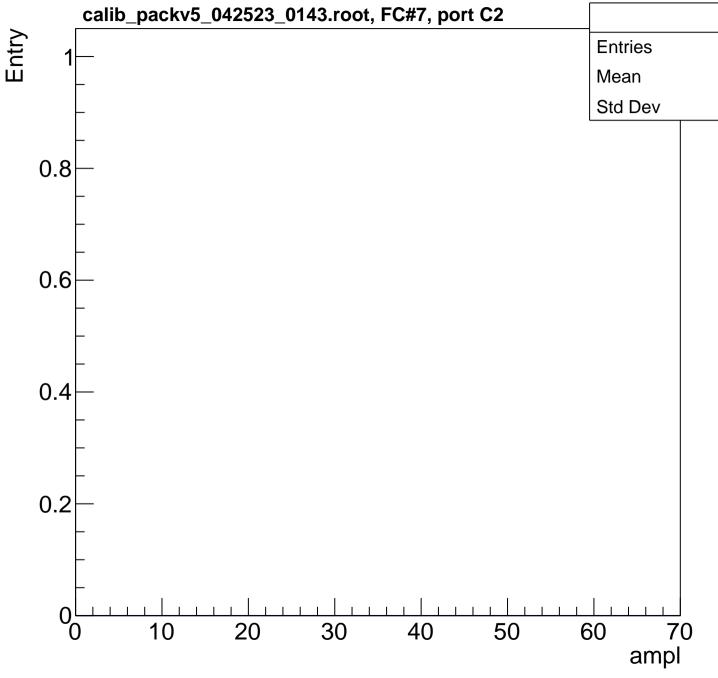


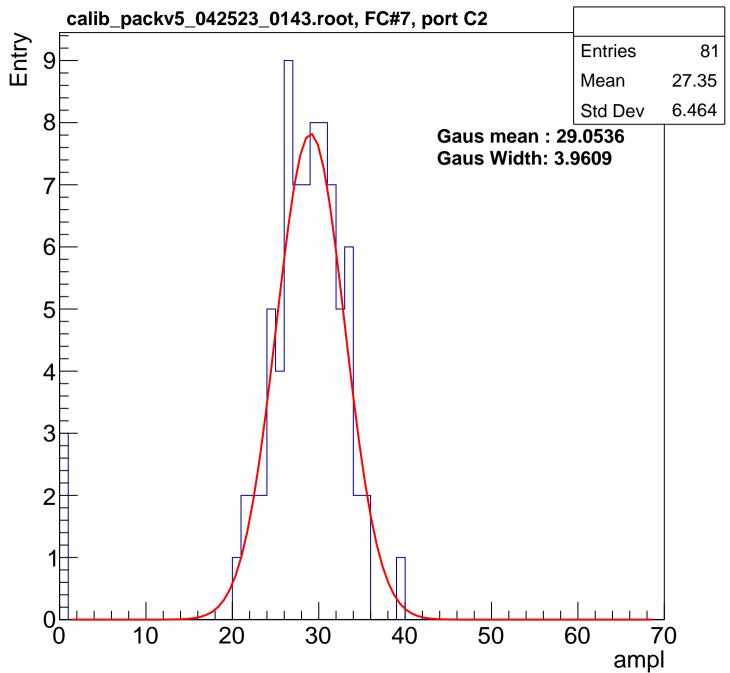


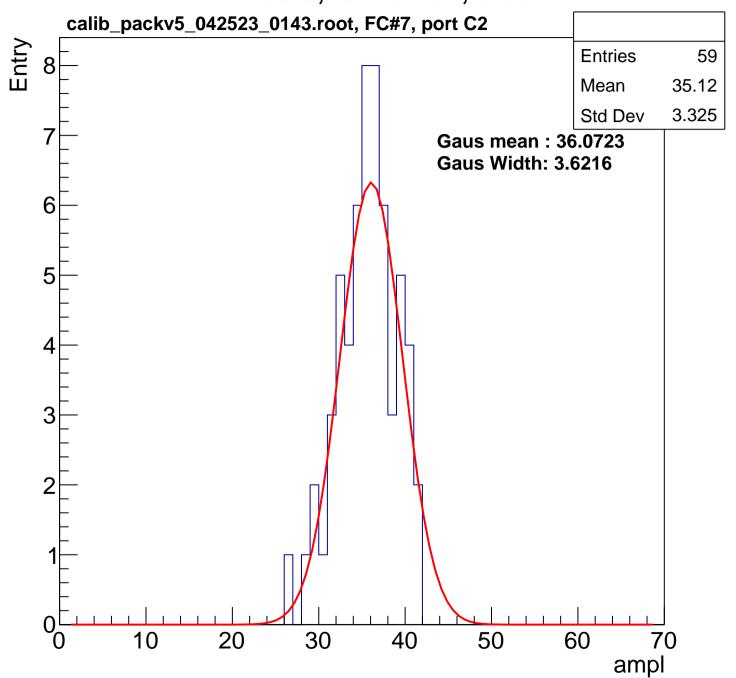


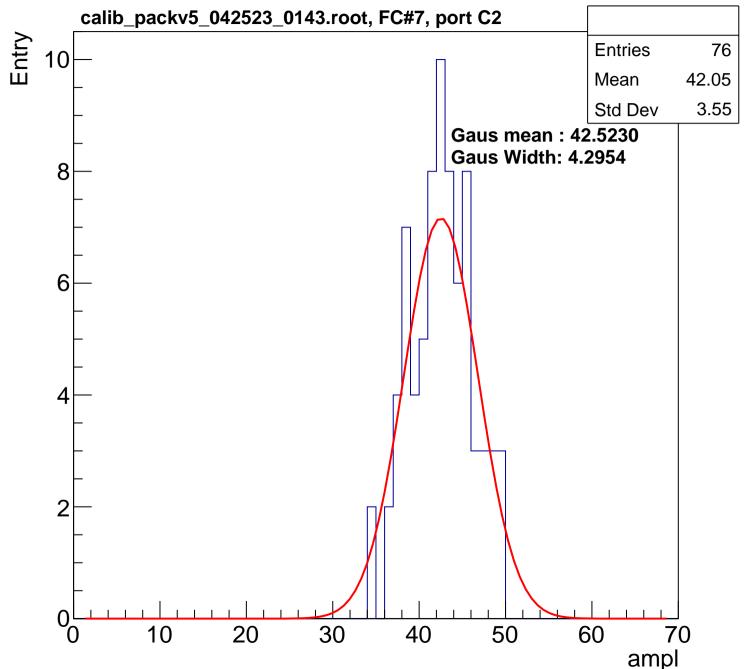


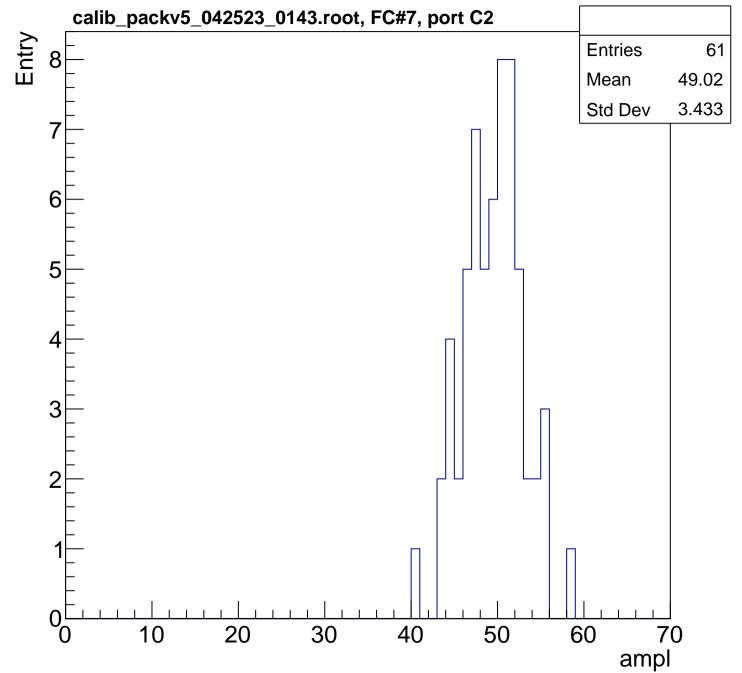


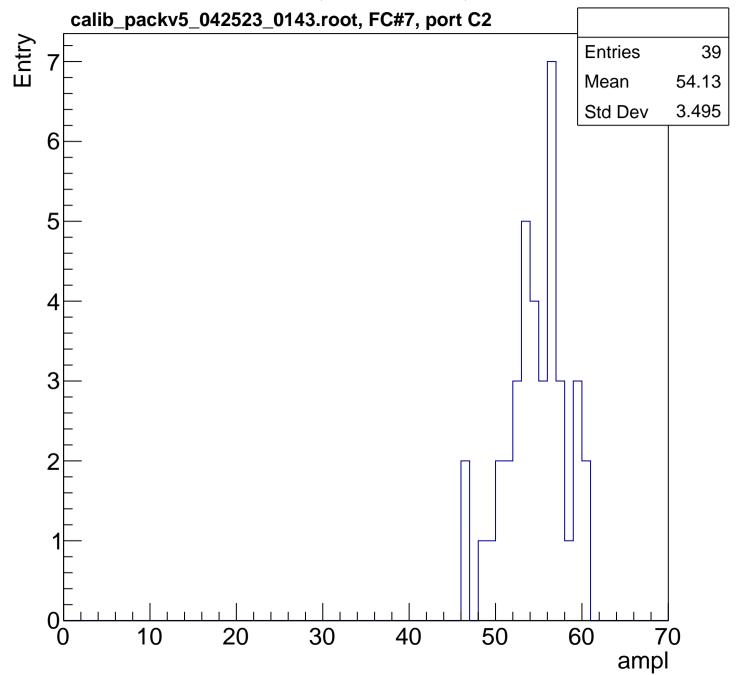


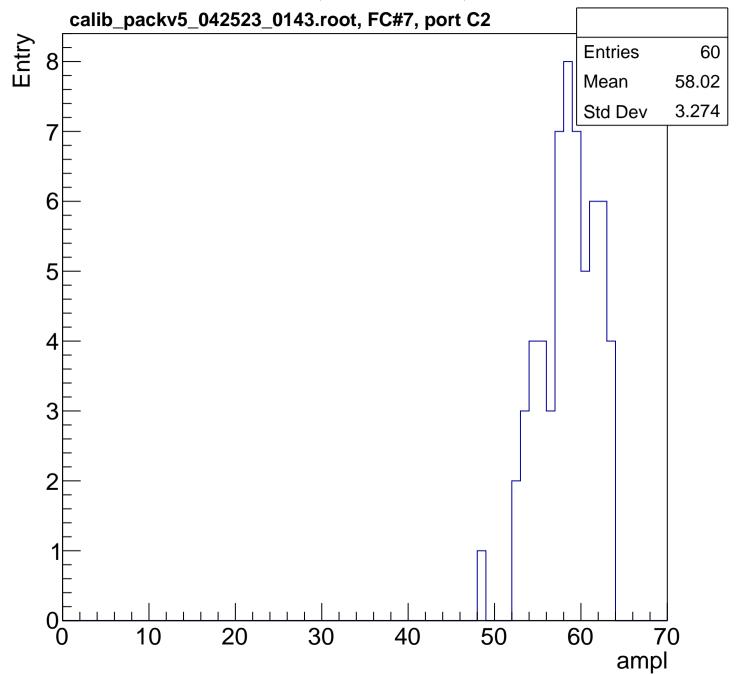


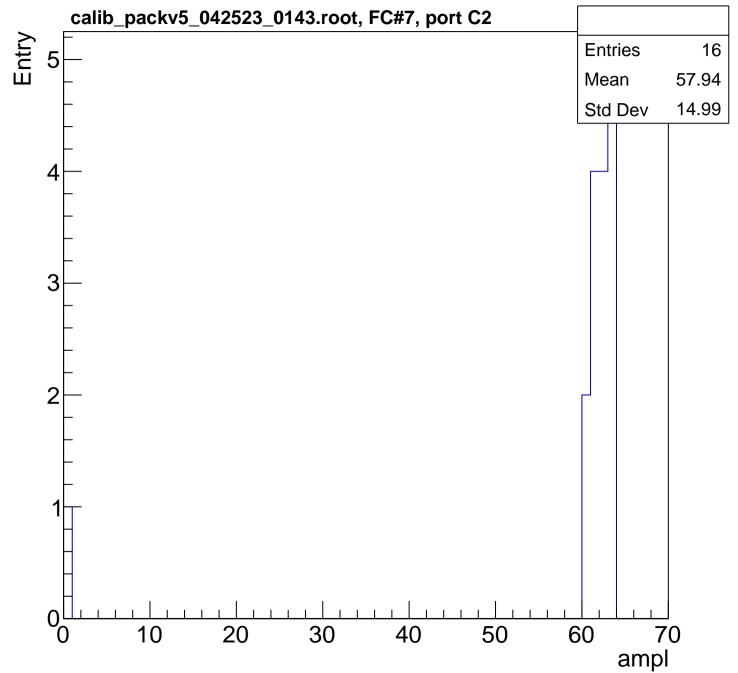


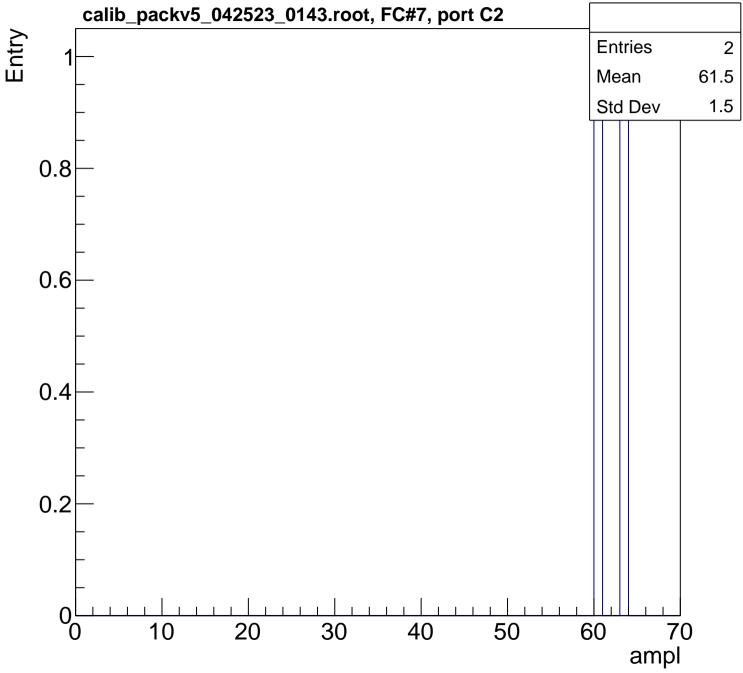


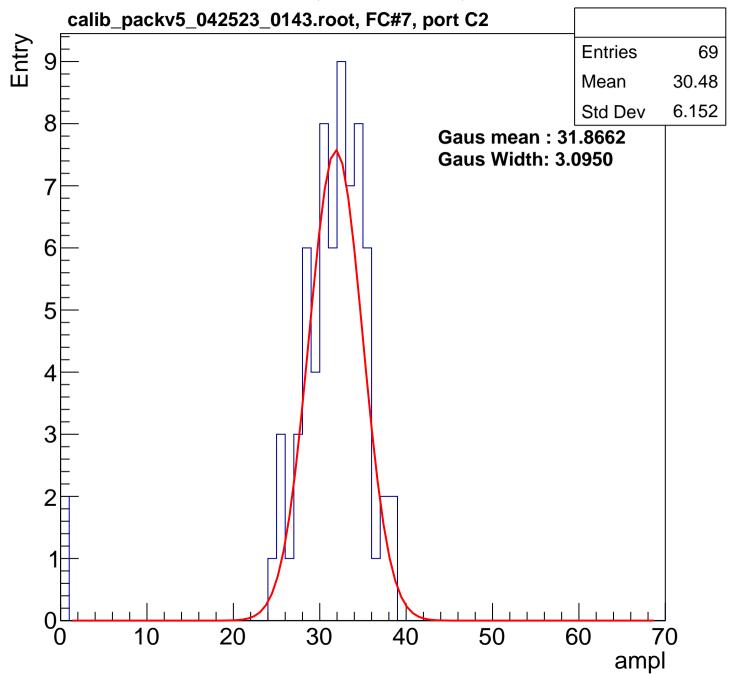


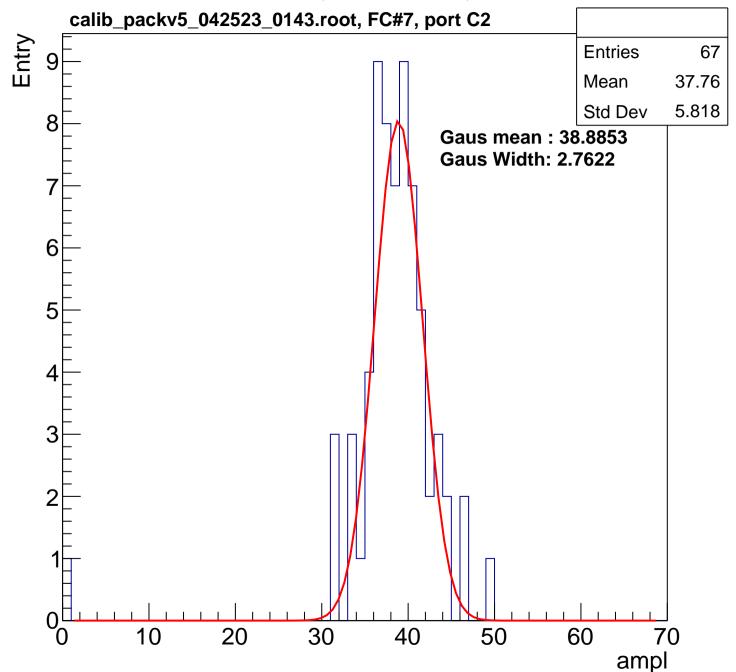


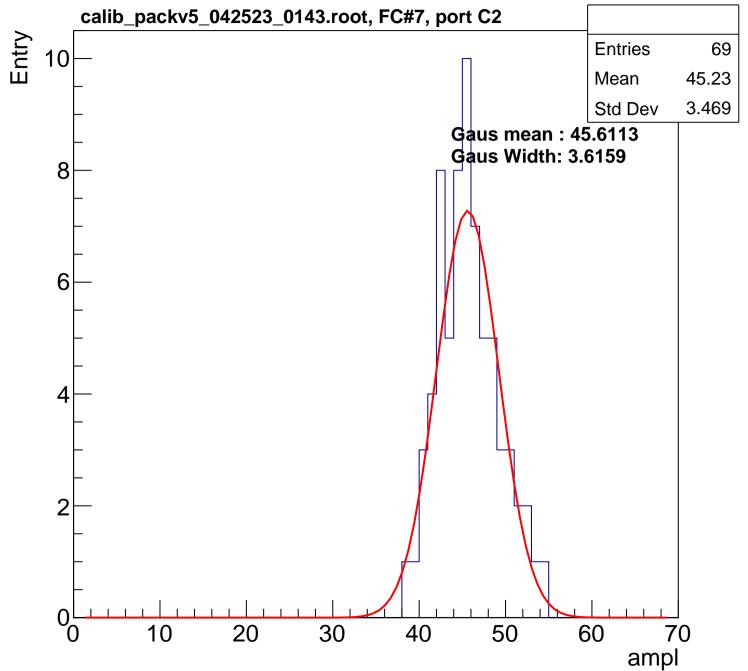


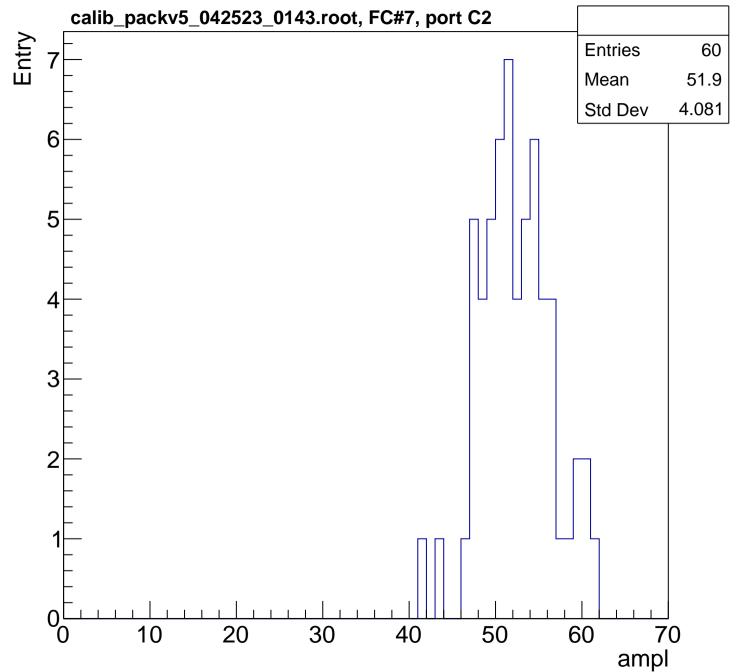


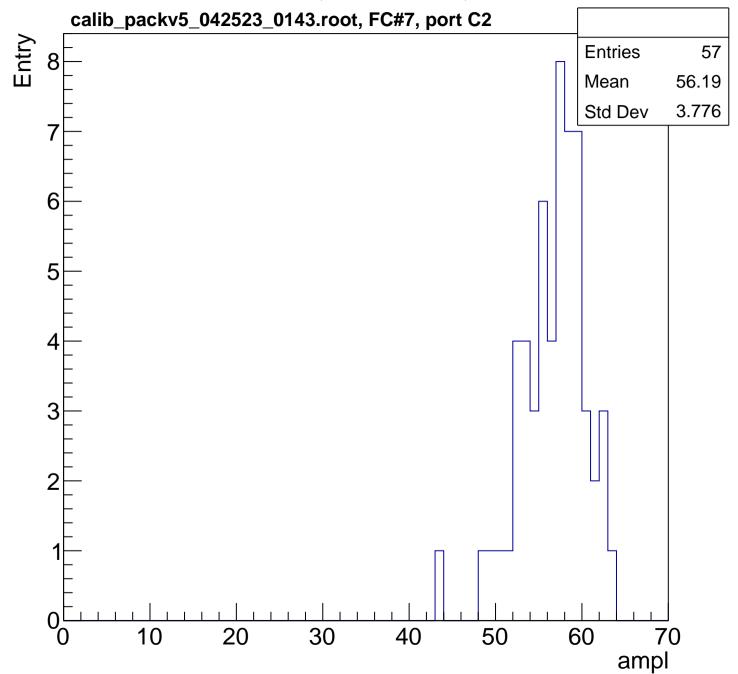


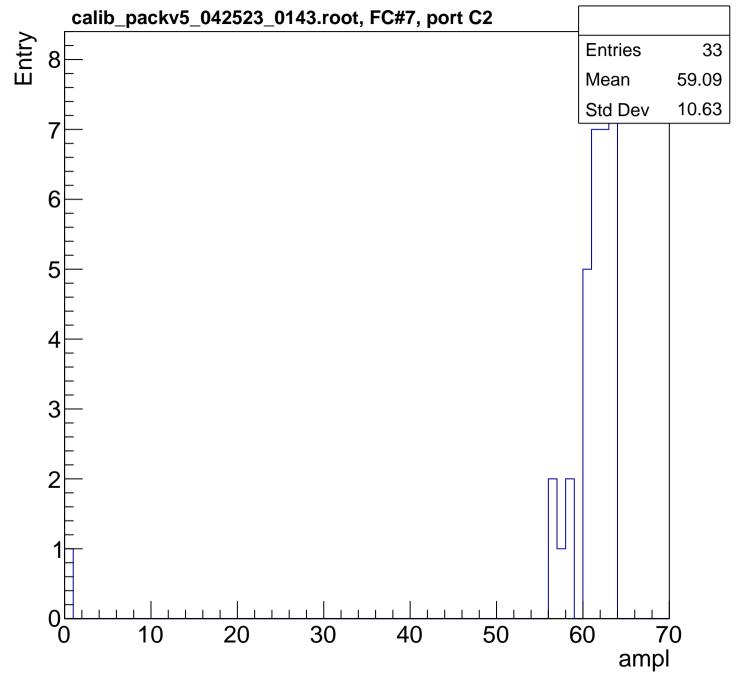


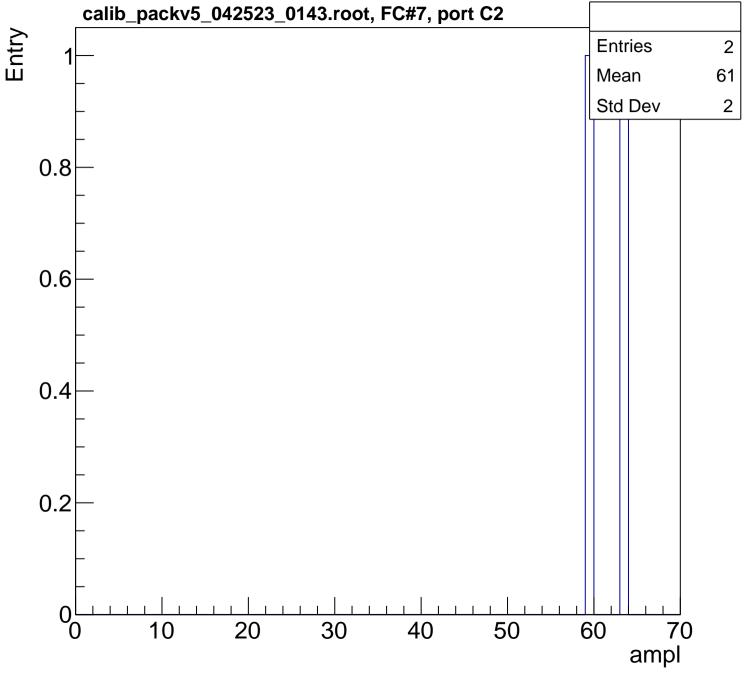


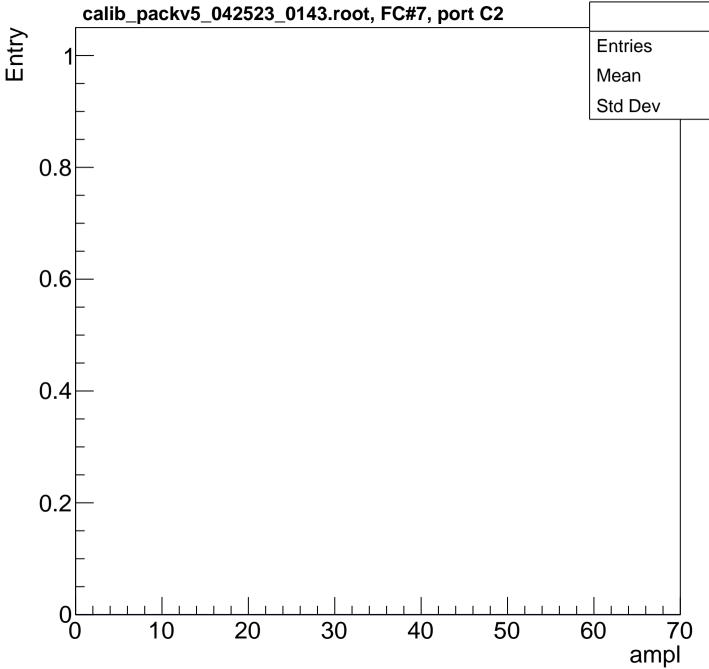


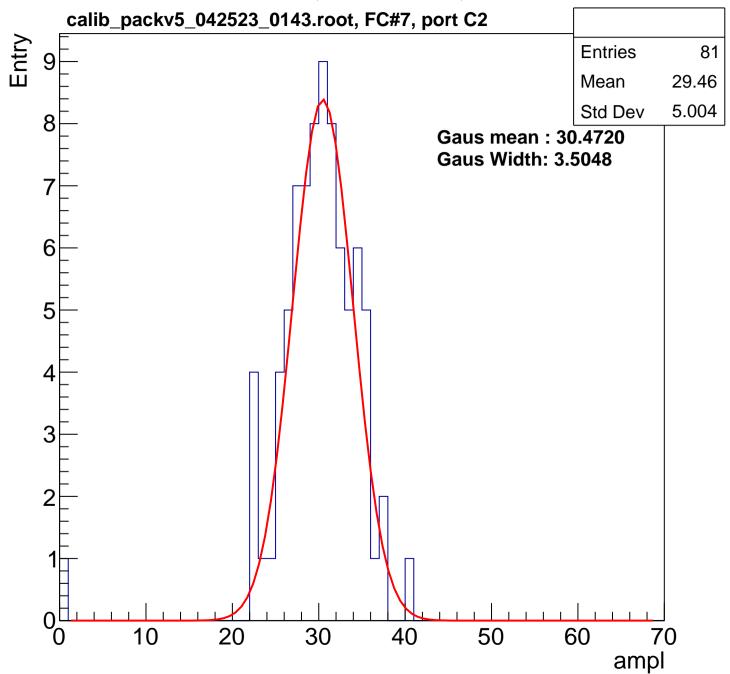


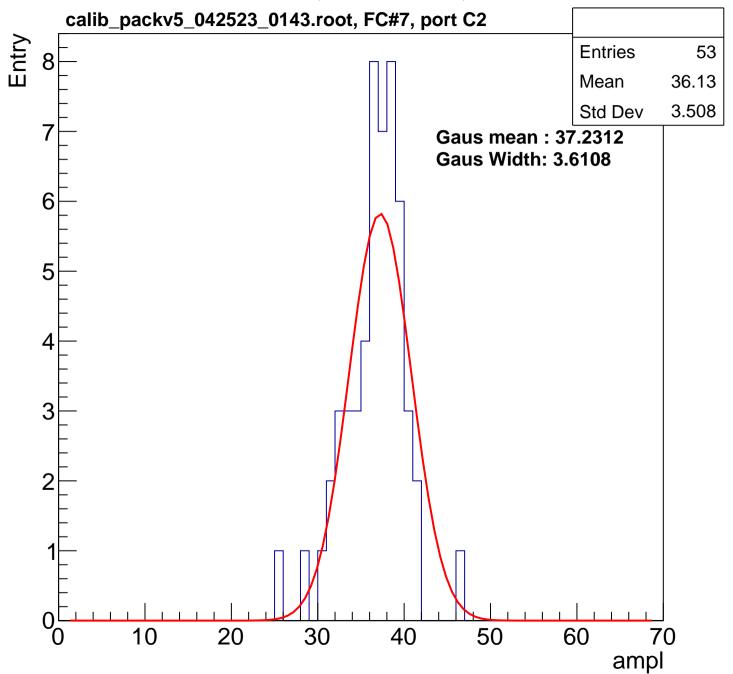


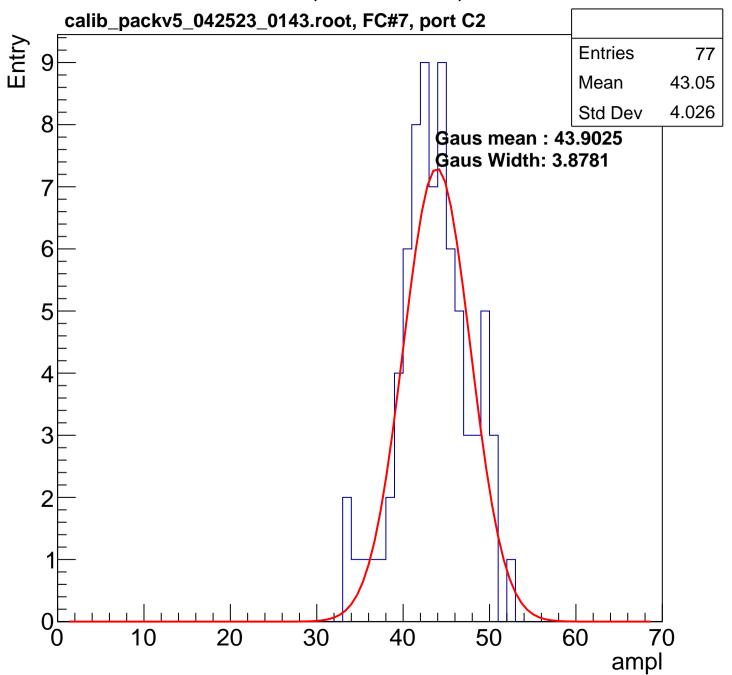


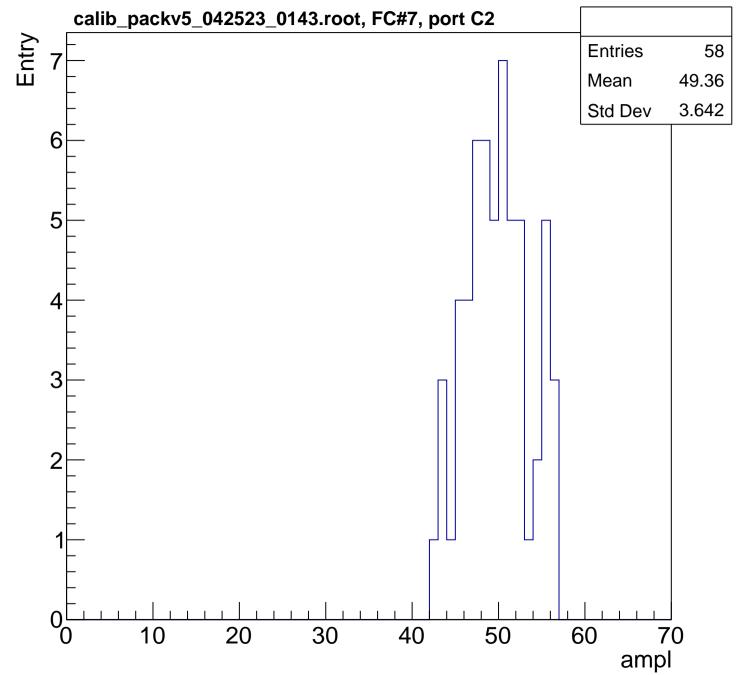


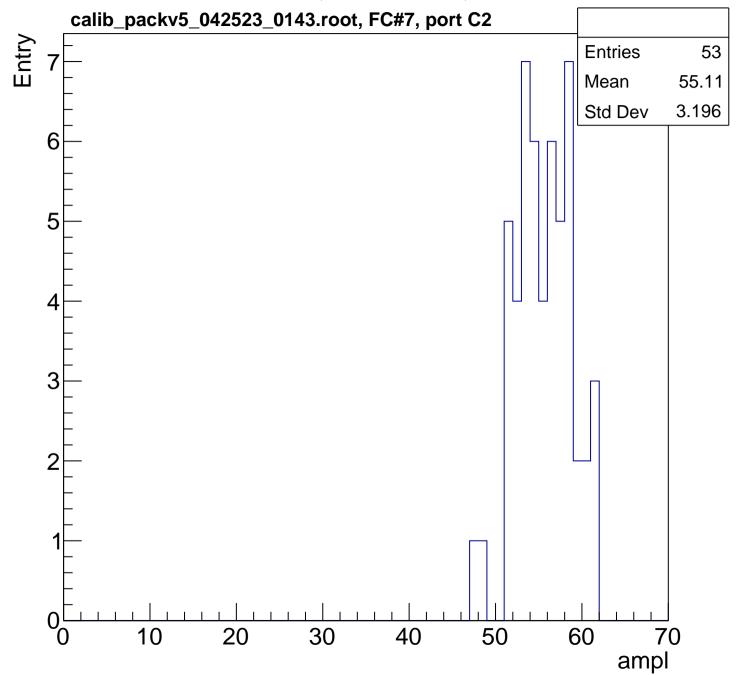


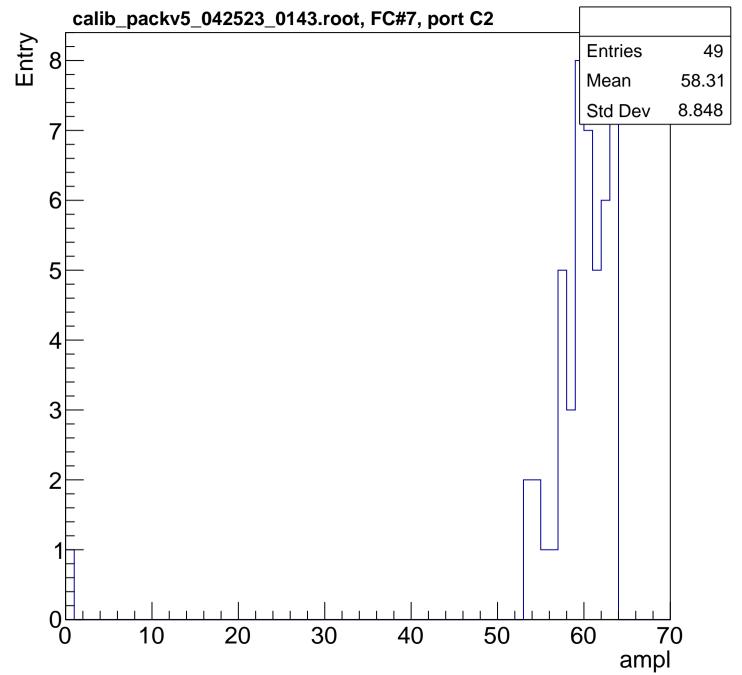


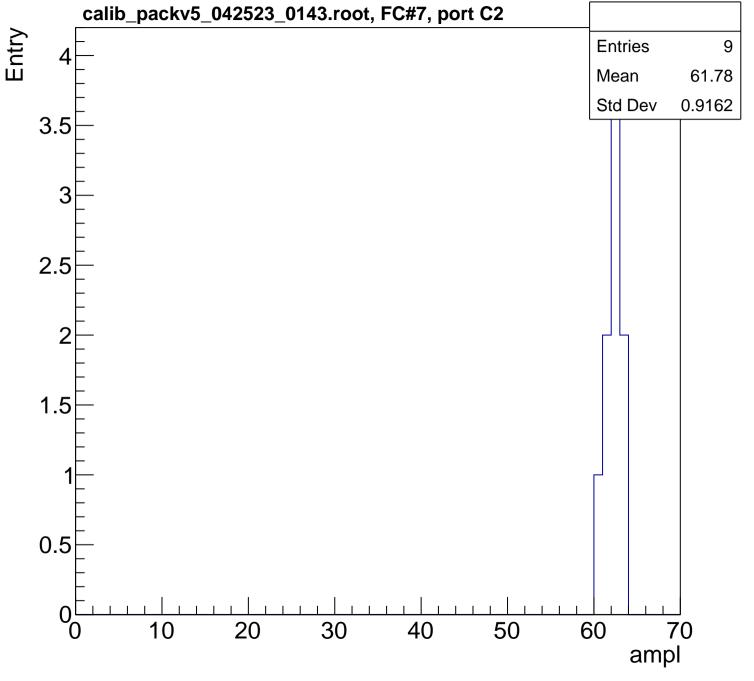


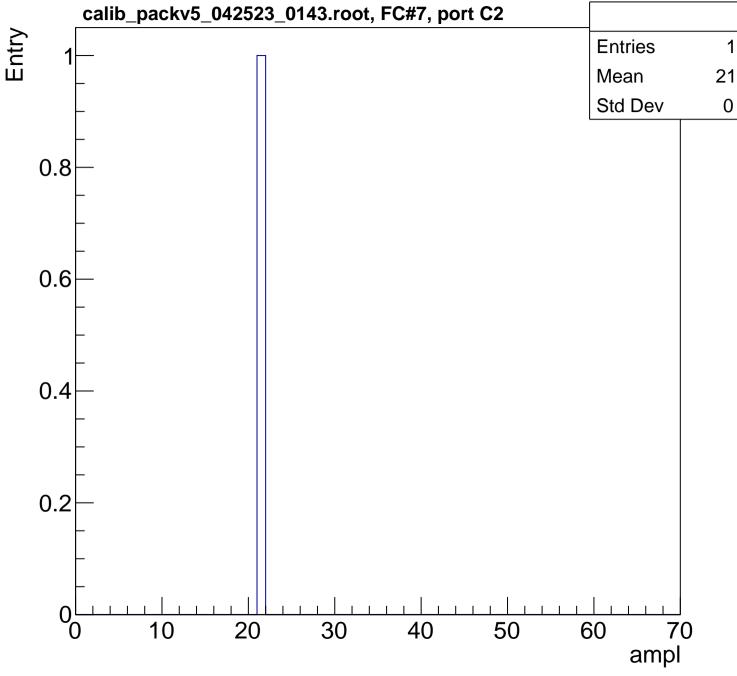


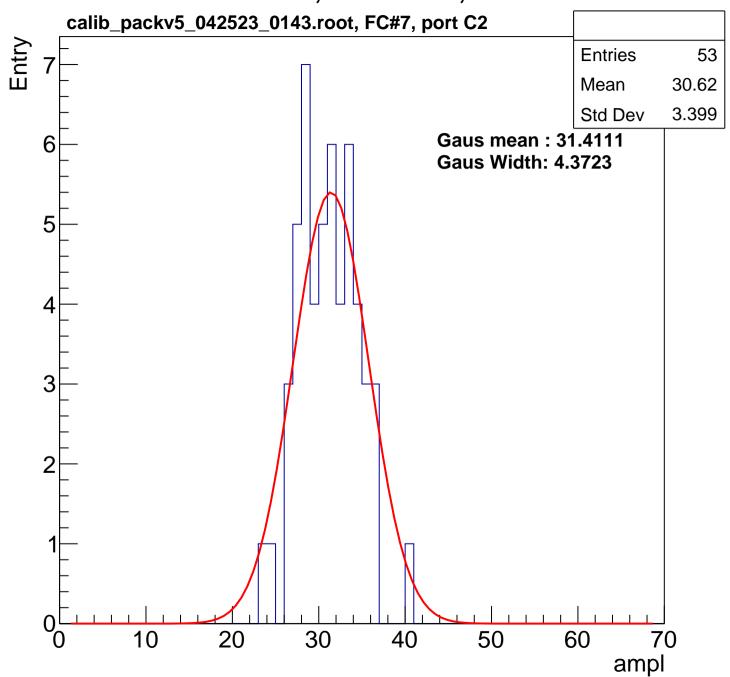


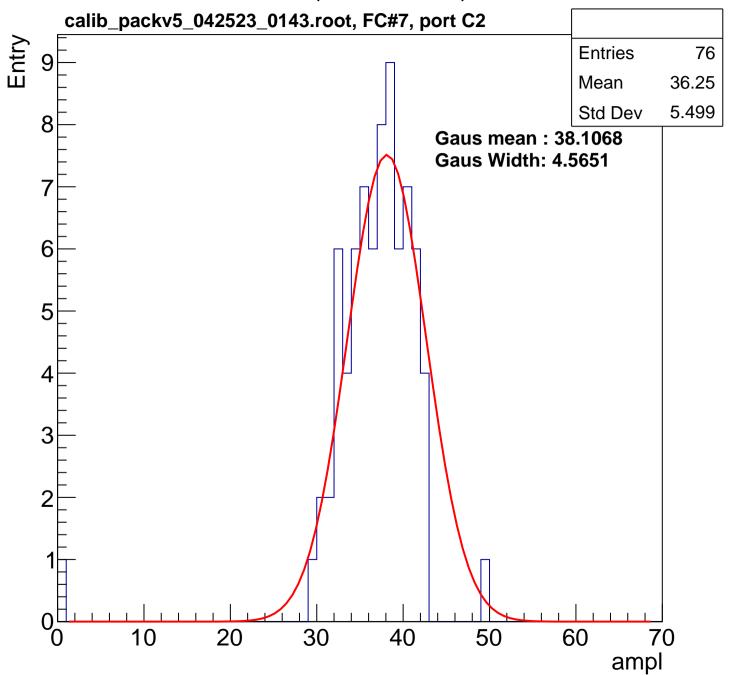


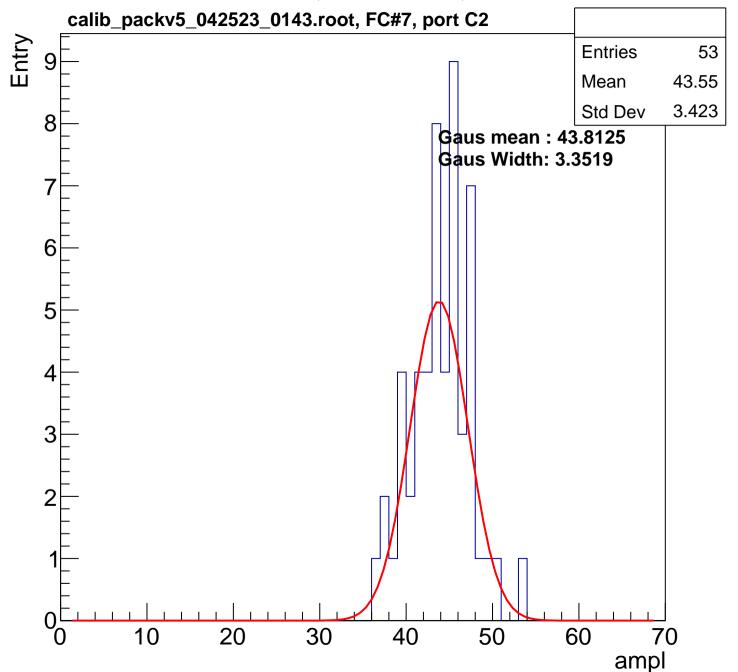


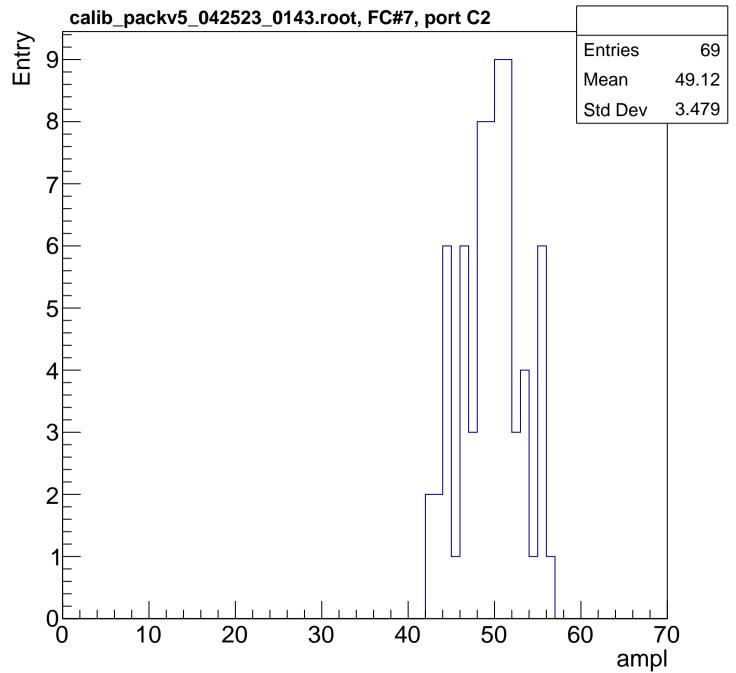


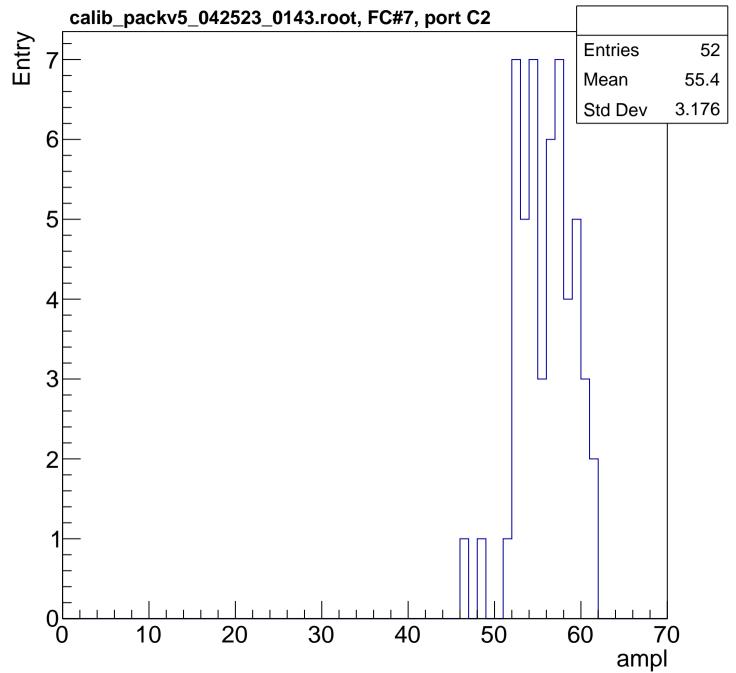


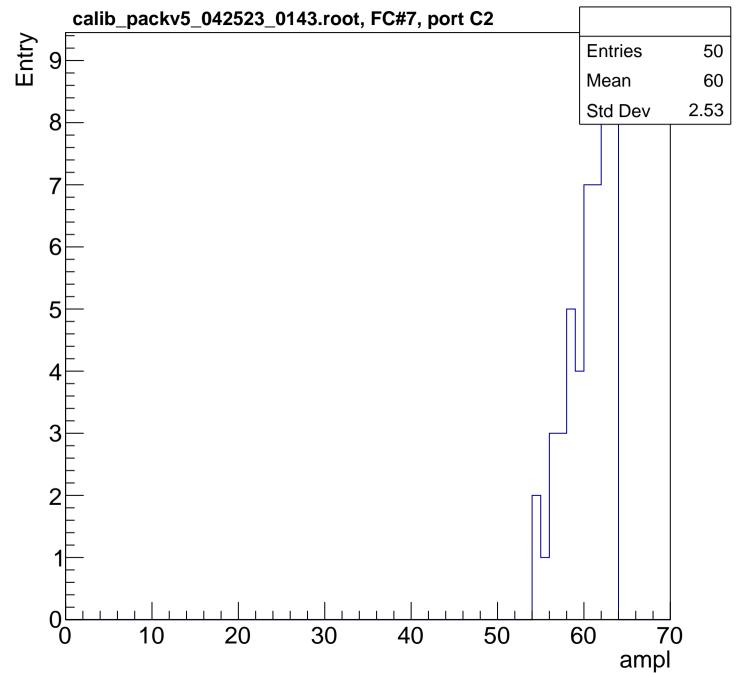


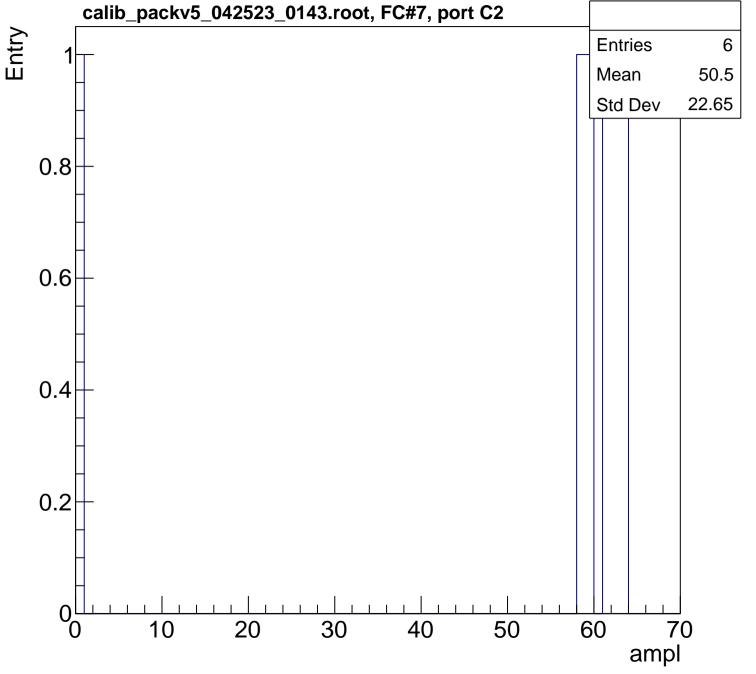




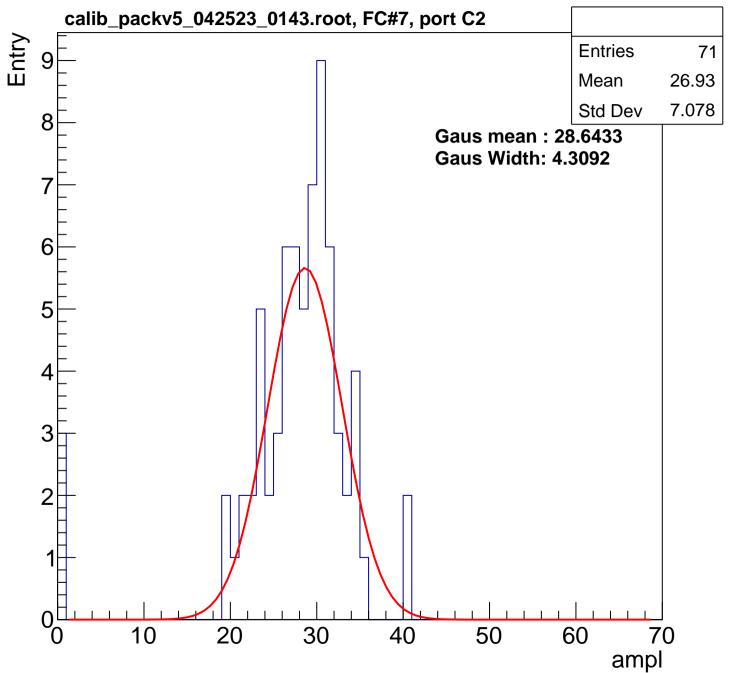


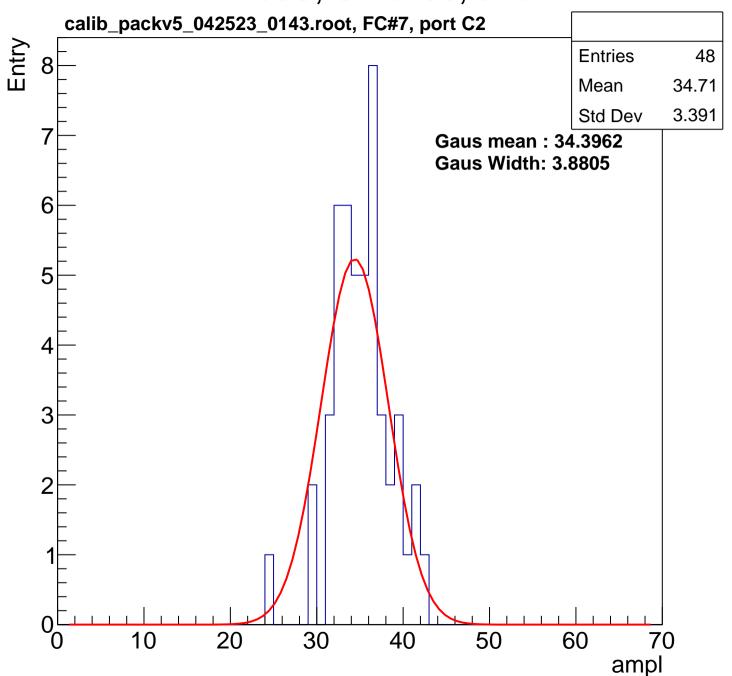


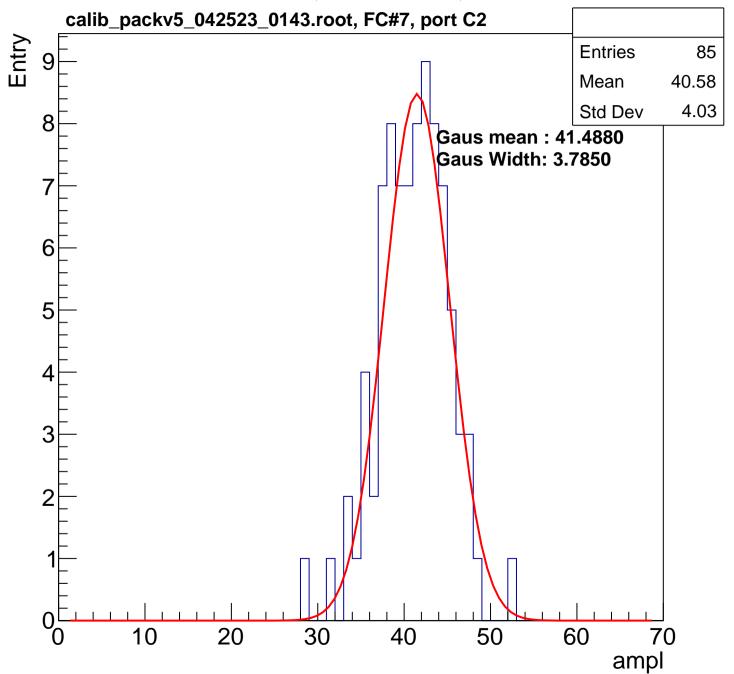


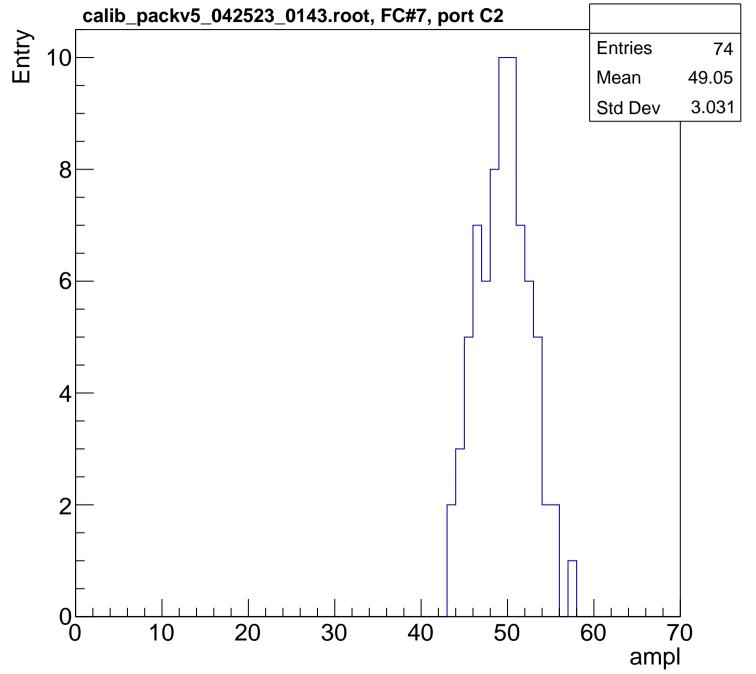


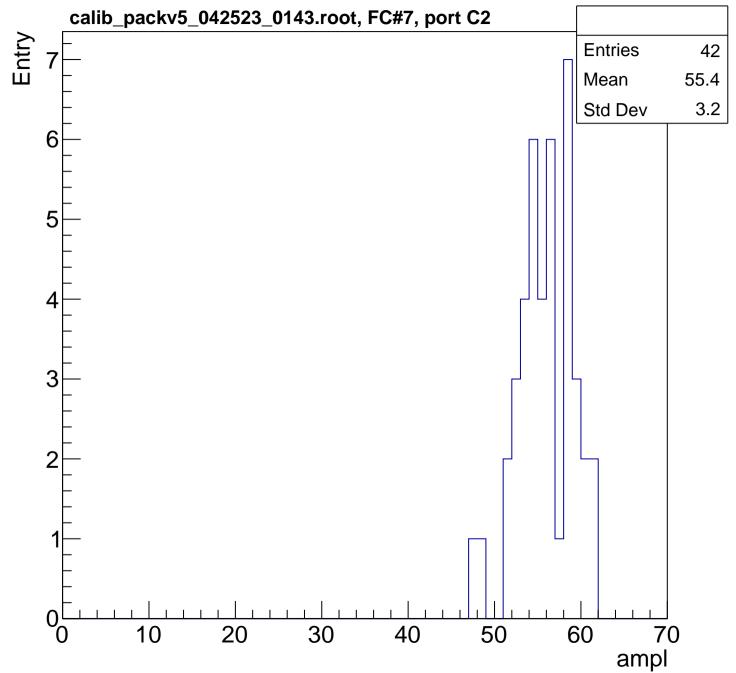
B1L103S, U4-ch85, adc7 calib_packv5_042523_0143.root, FC#7, port C2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

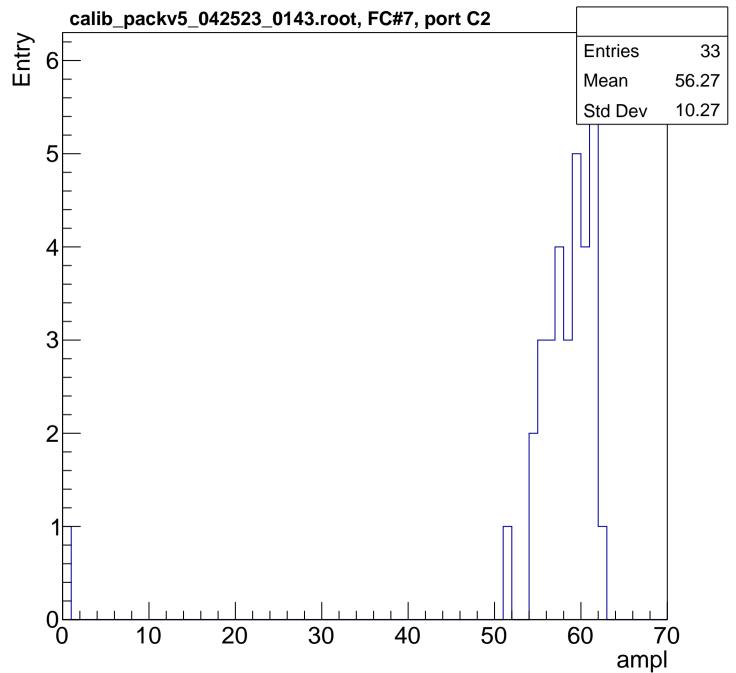




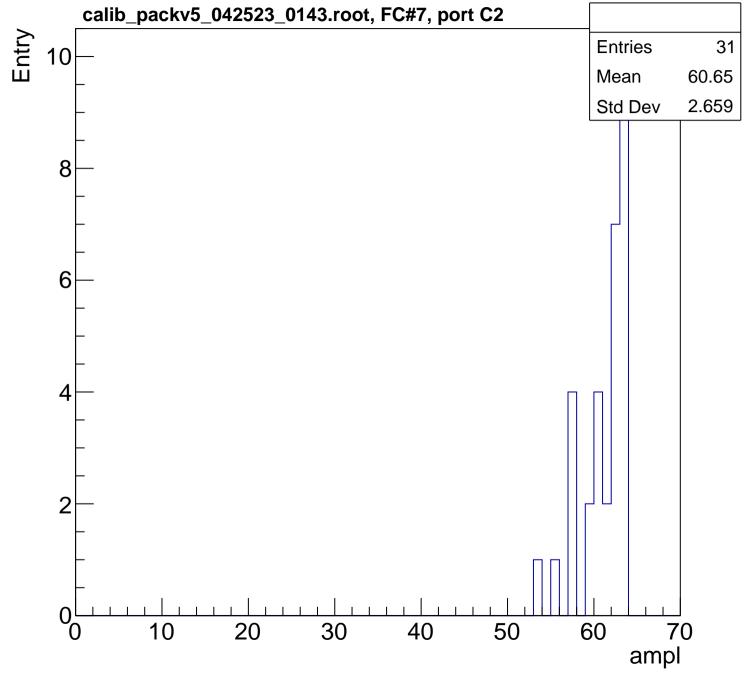


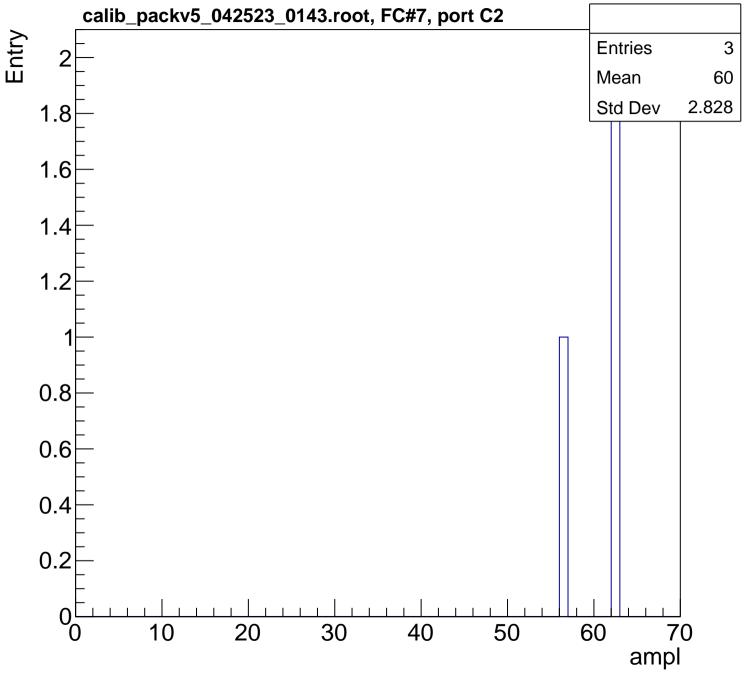


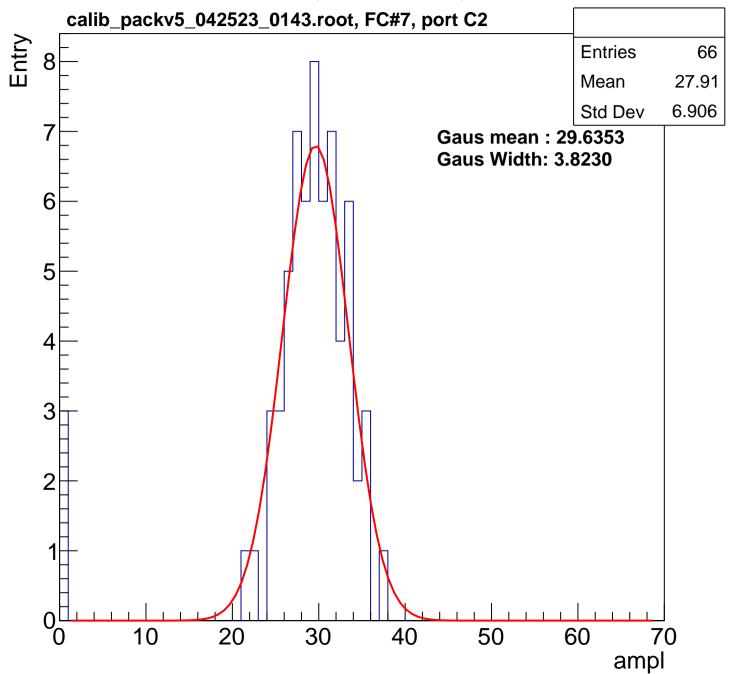


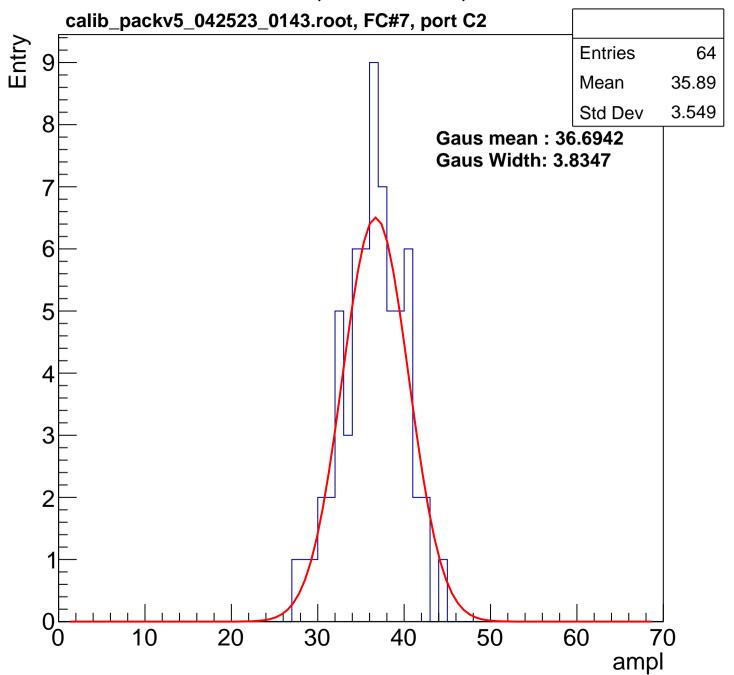


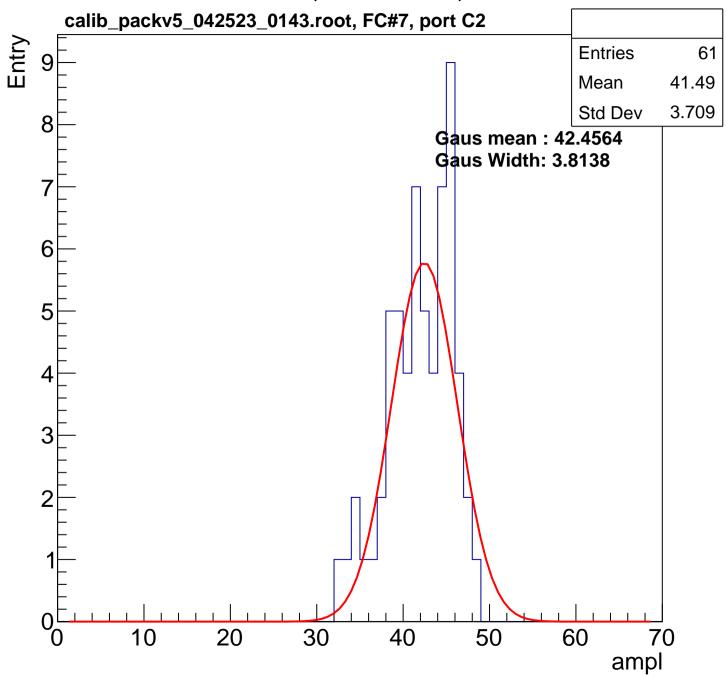
B1L103S, U4-ch86, adc6

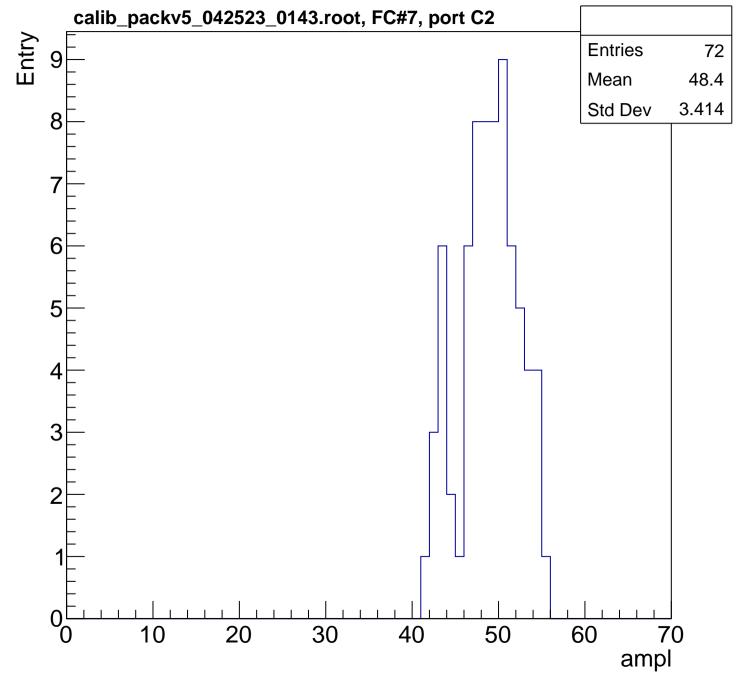


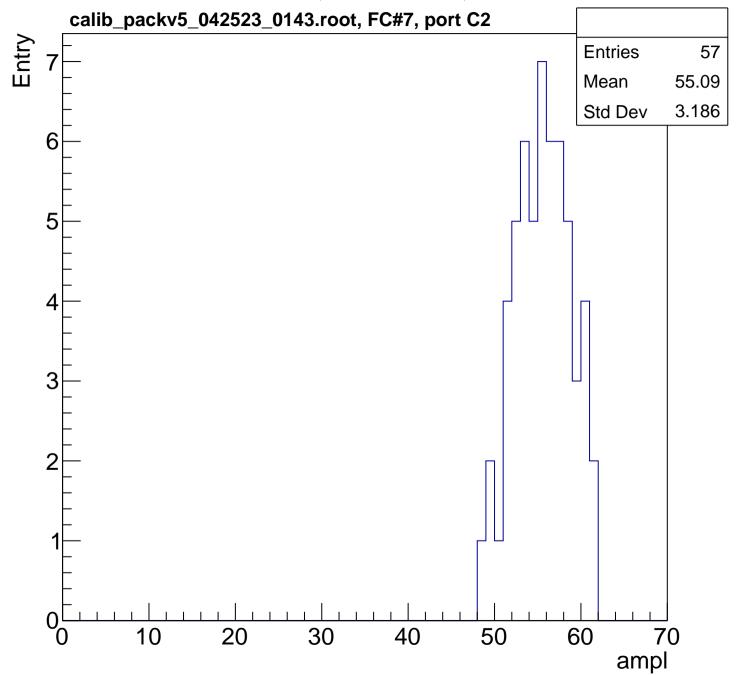


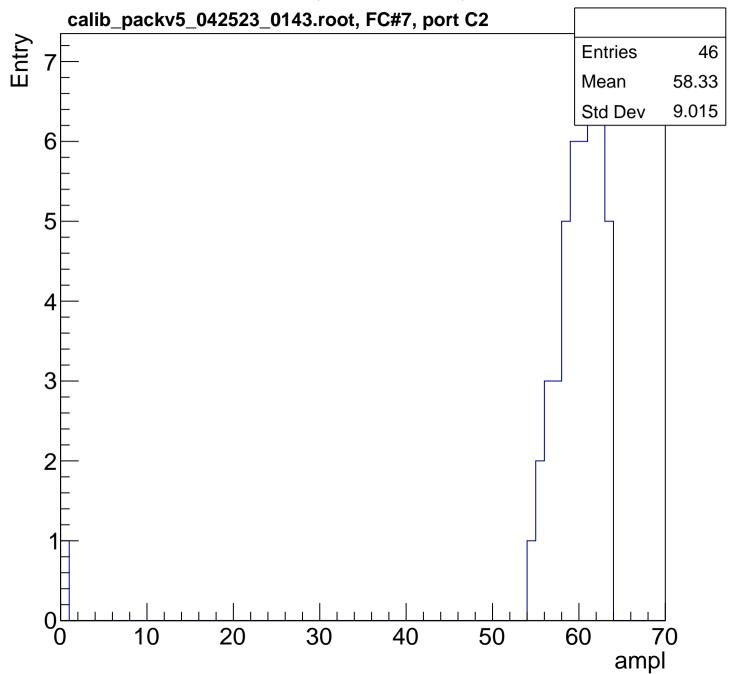


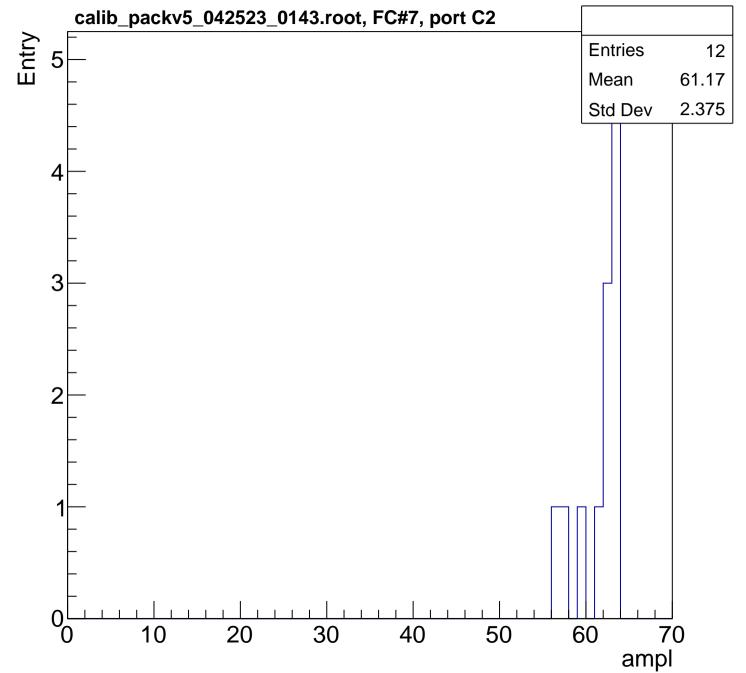


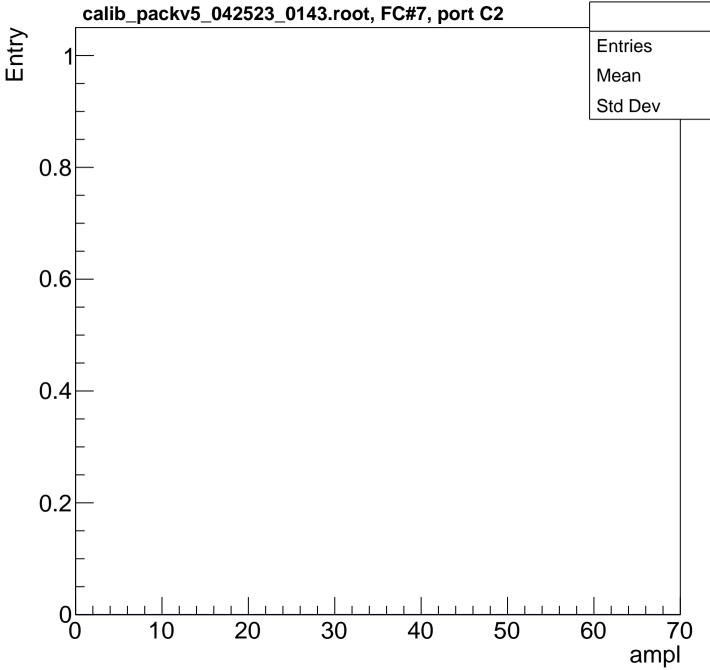


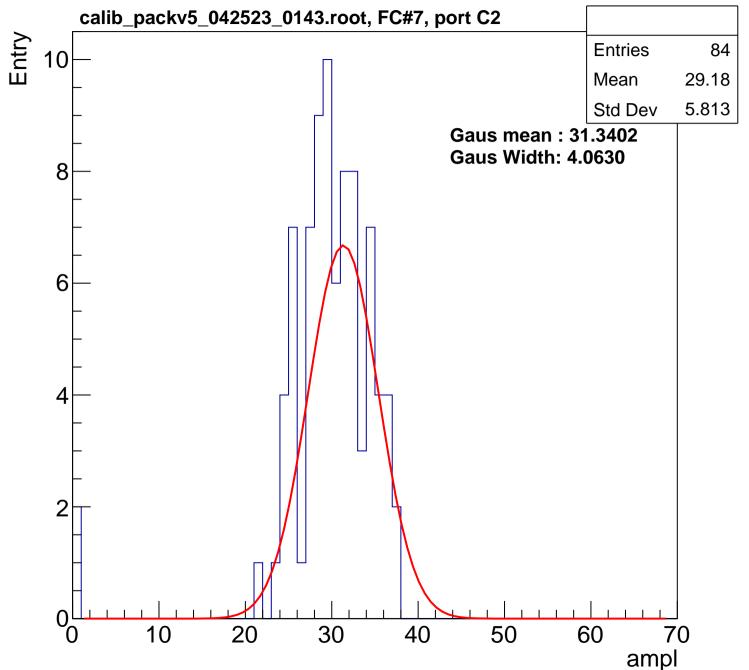


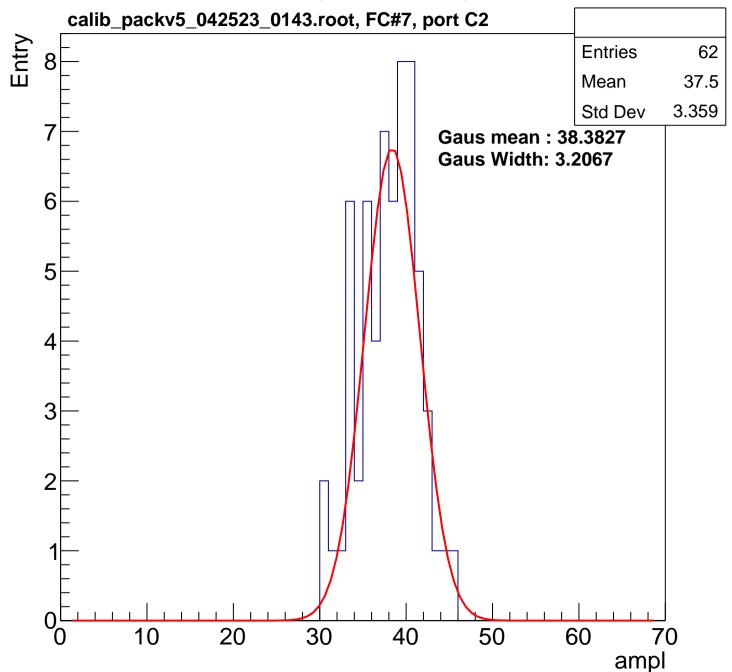


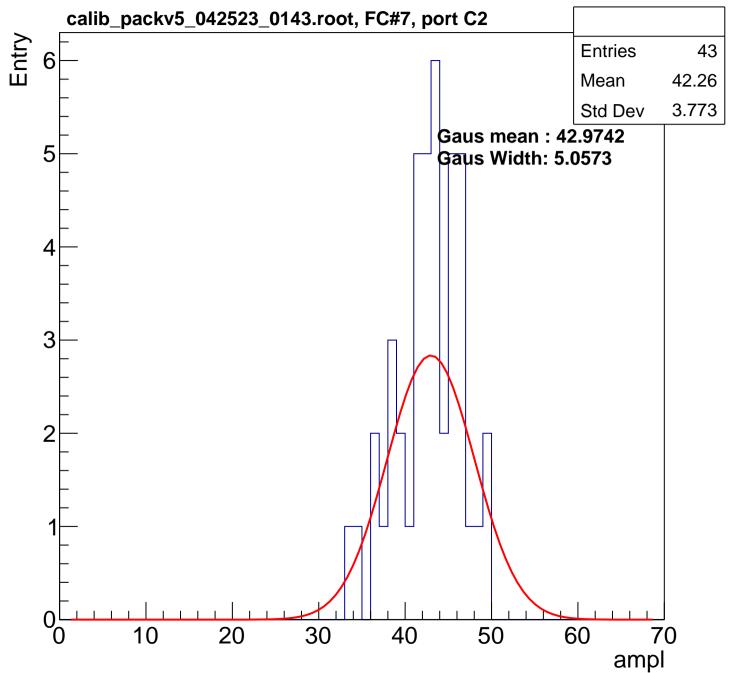


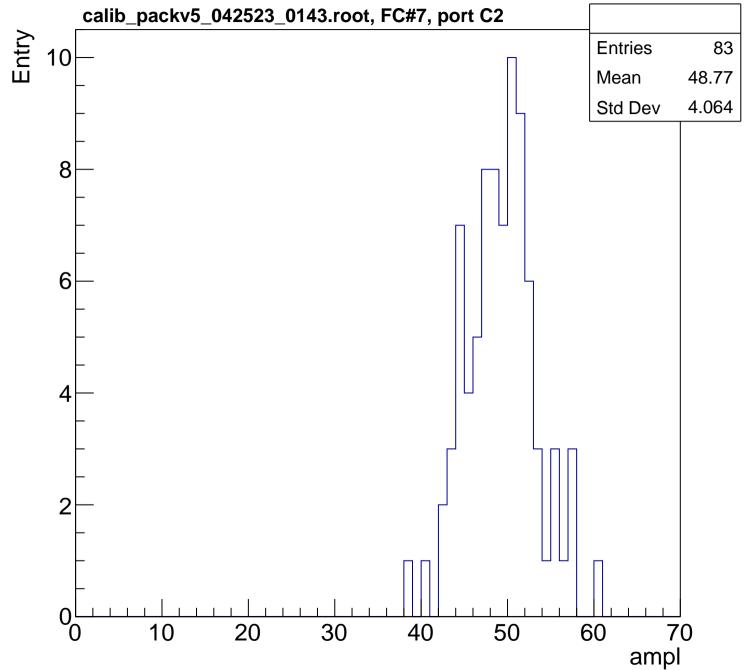


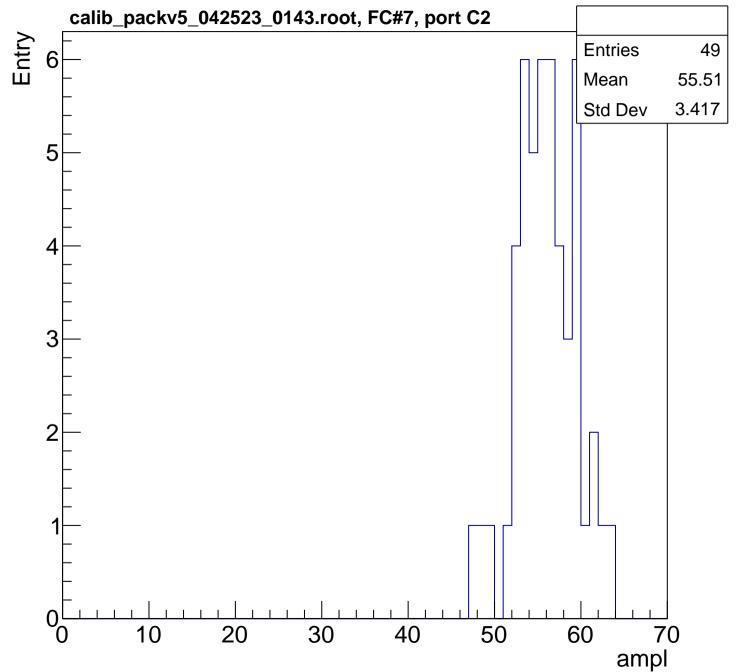


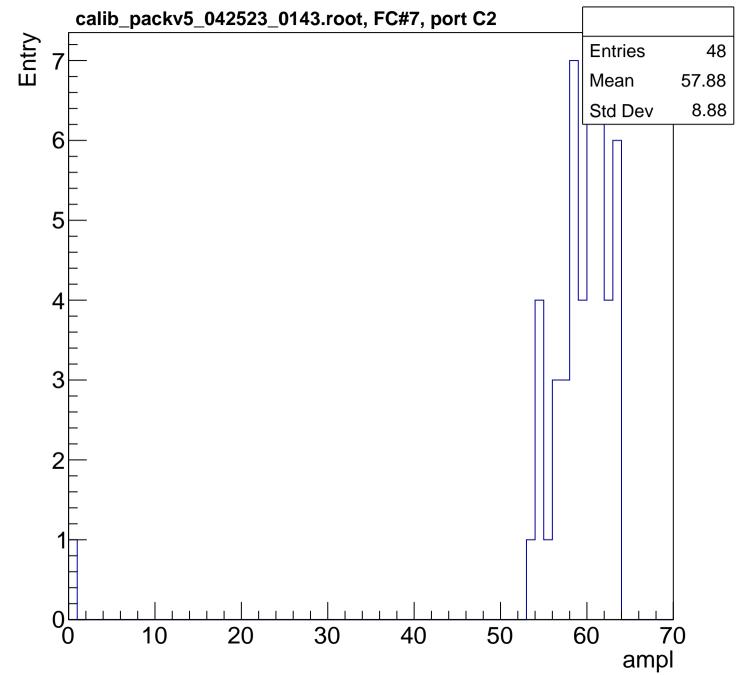


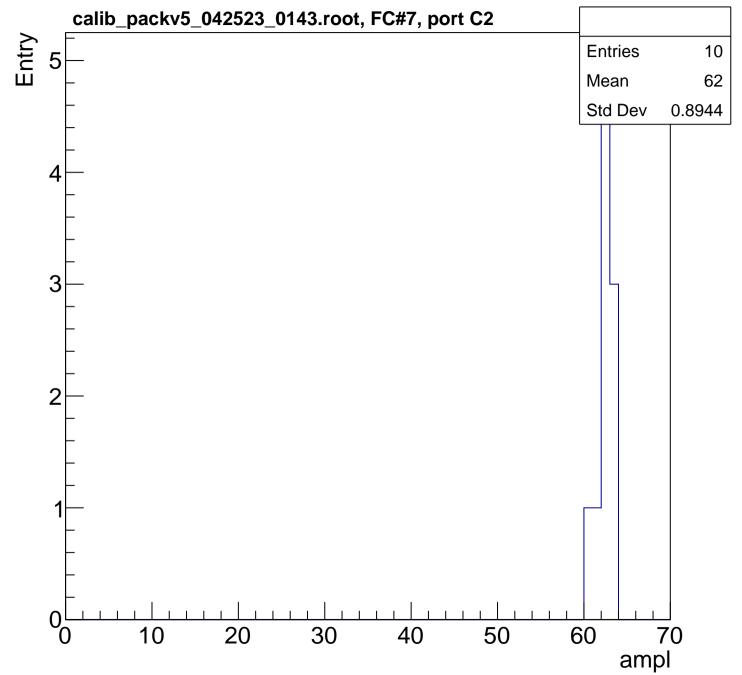




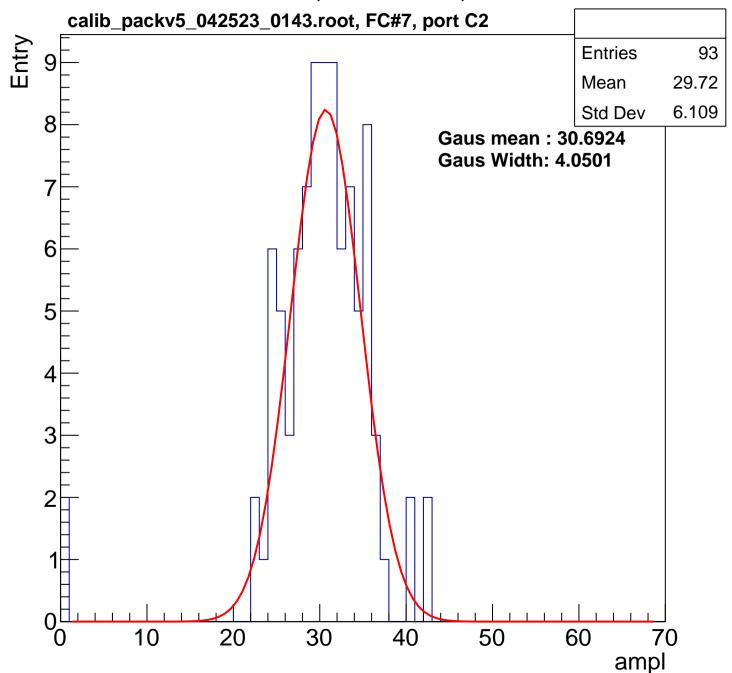


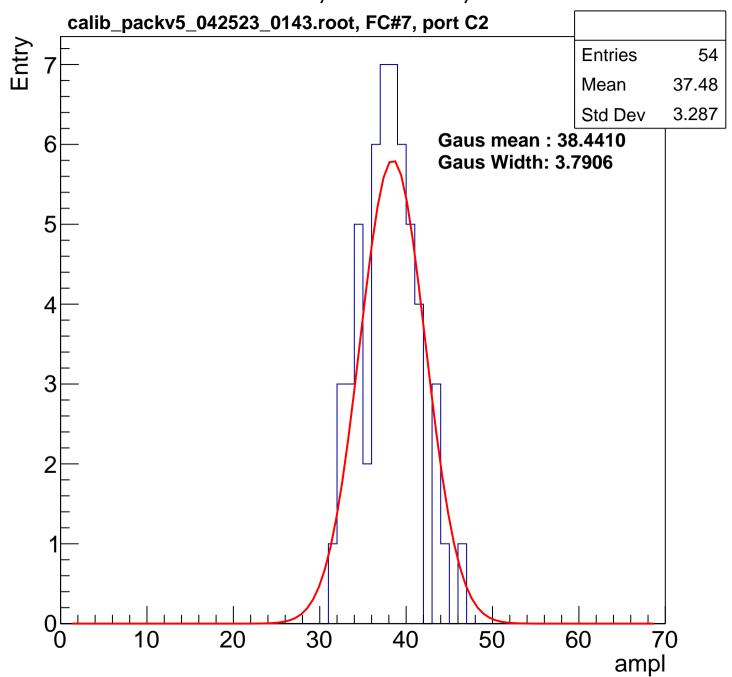


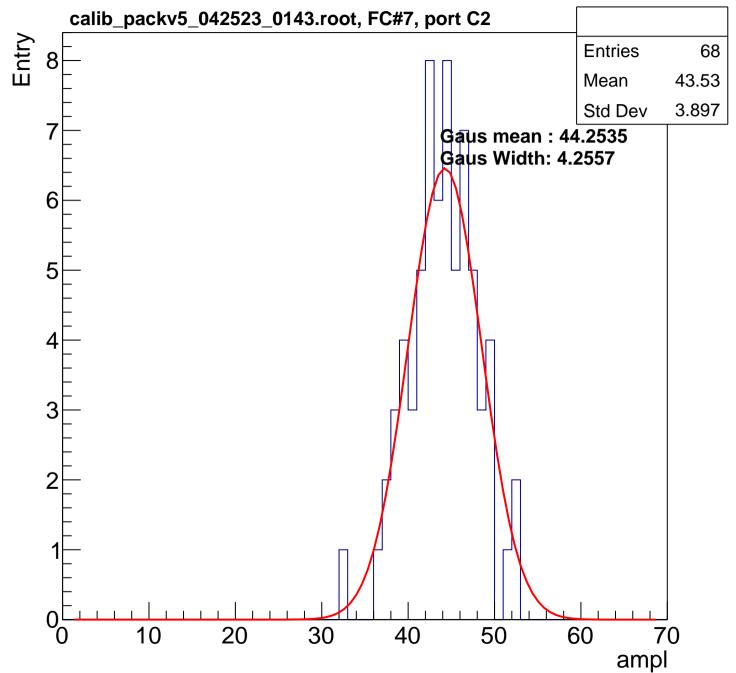


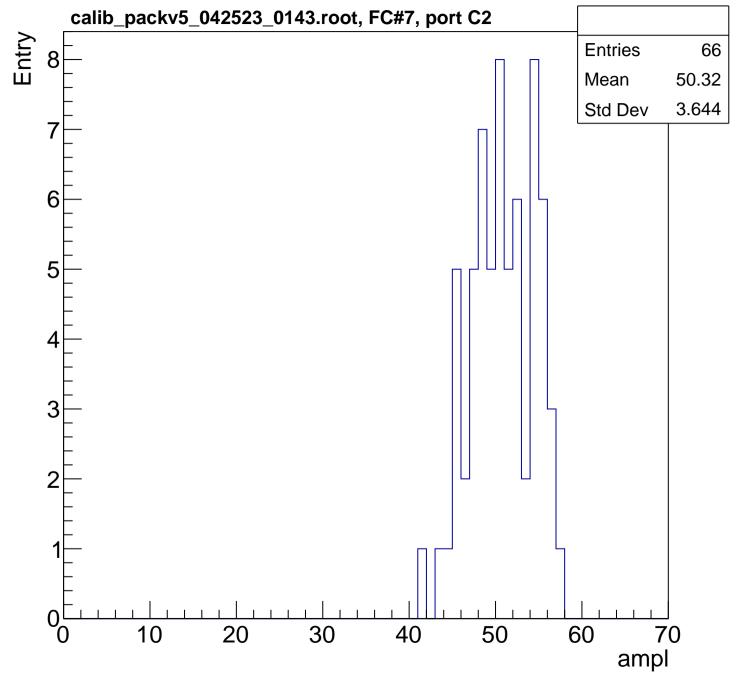


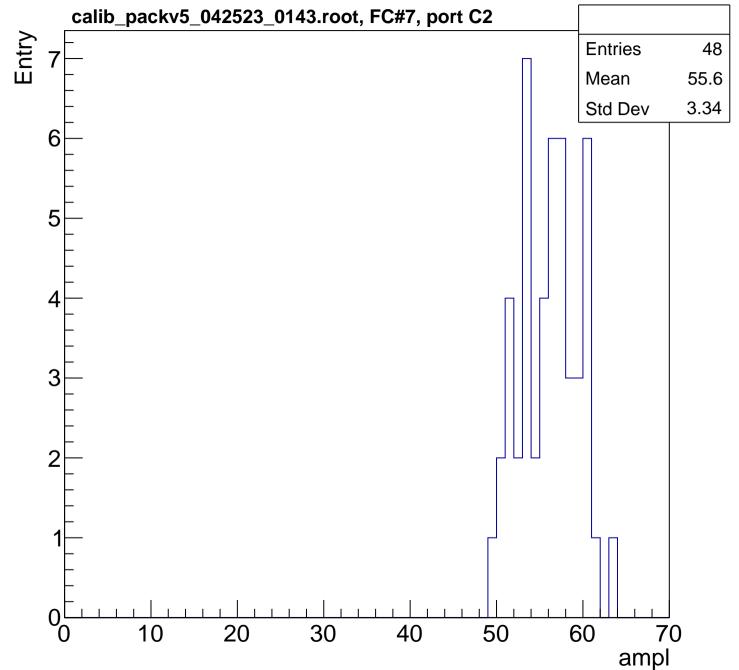
B1L103S, U4-ch88, adc7 calib_packv5_042523_0143.root, FC#7, port C2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

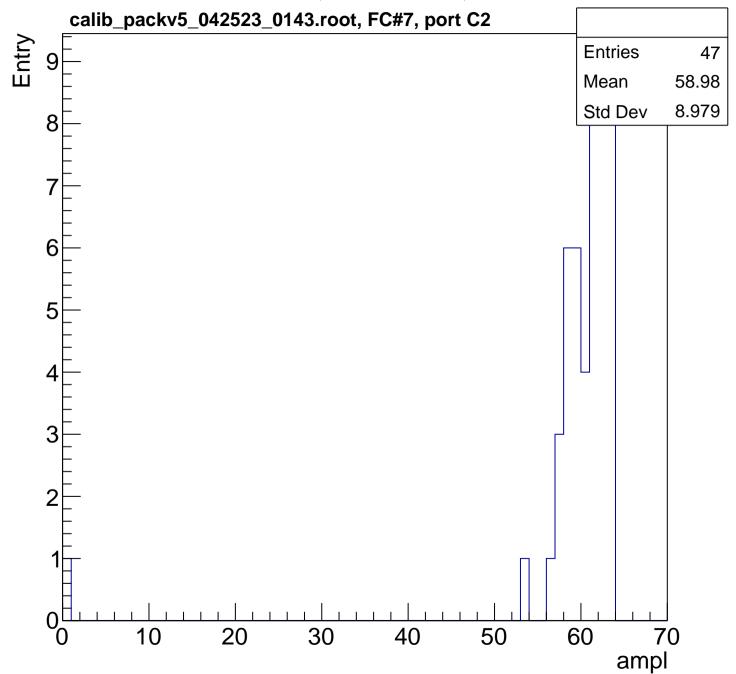


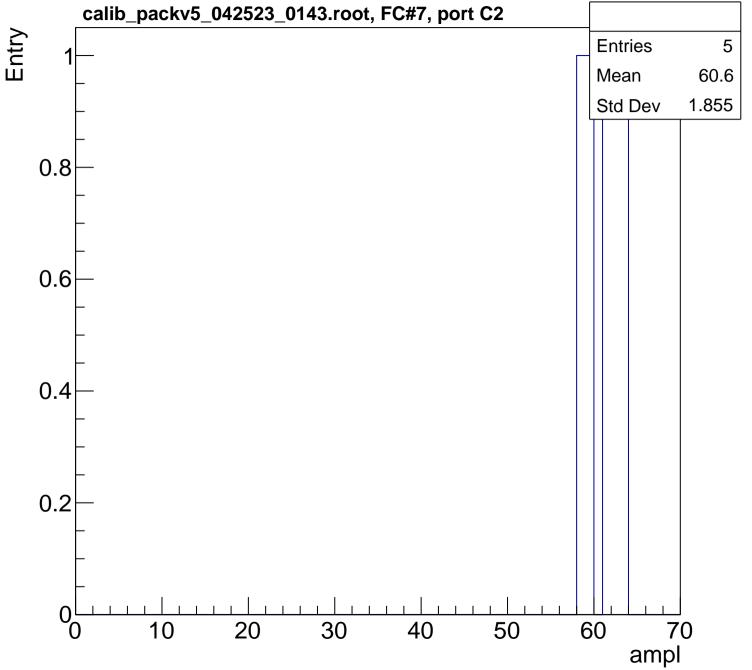




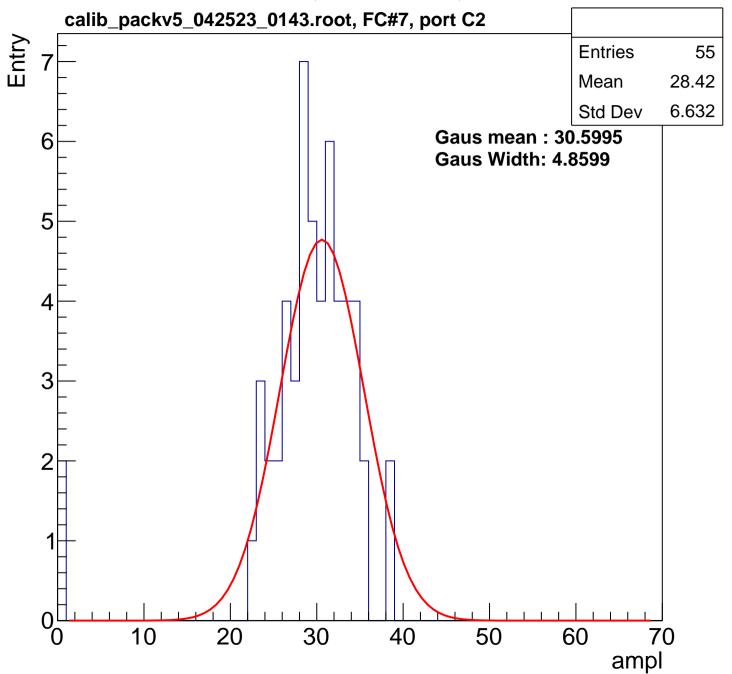


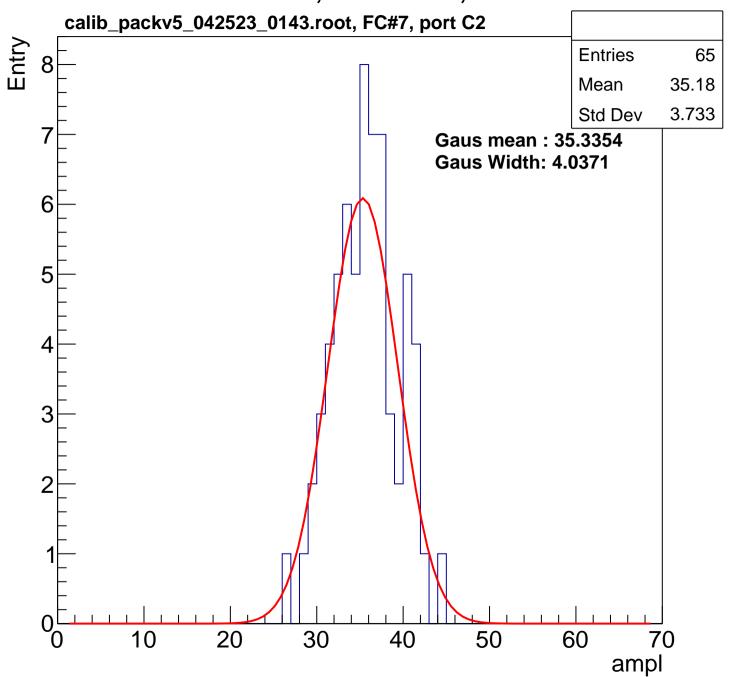


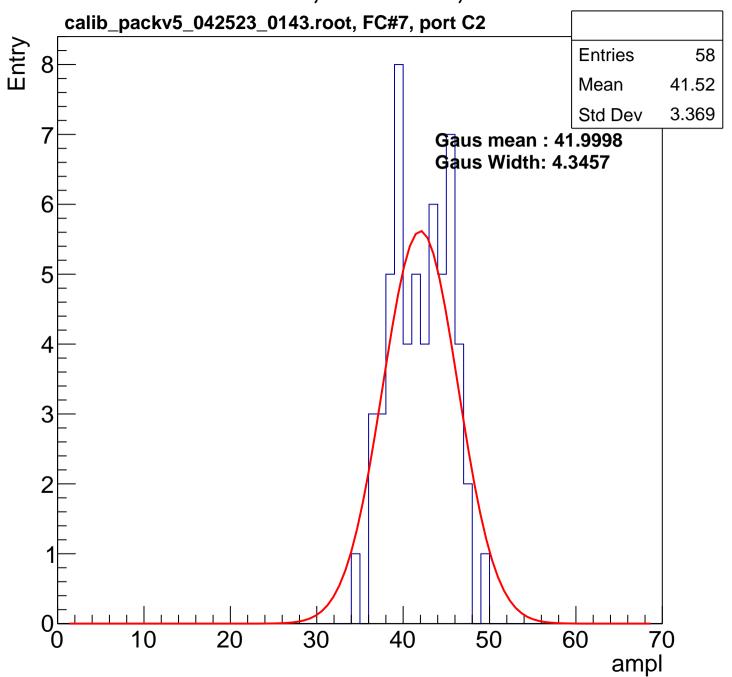


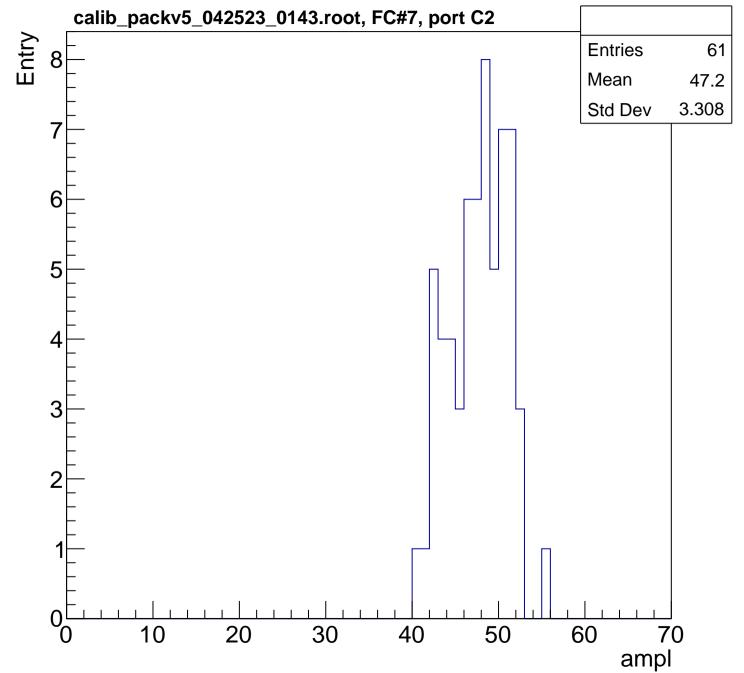


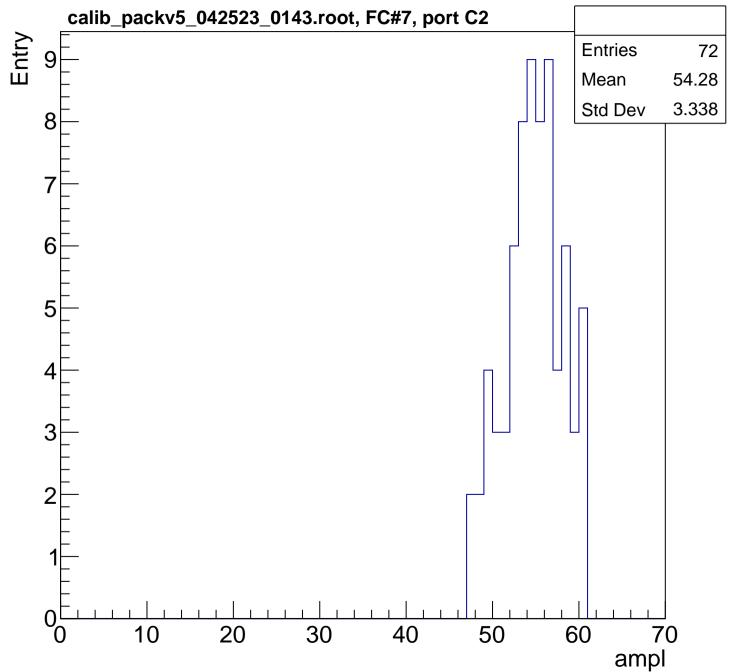
B1L103S, U4-ch89, adc7 calib_packv5_042523_0143.root, FC#7, port C2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2 10 30 20 40 50 60 70 ampl

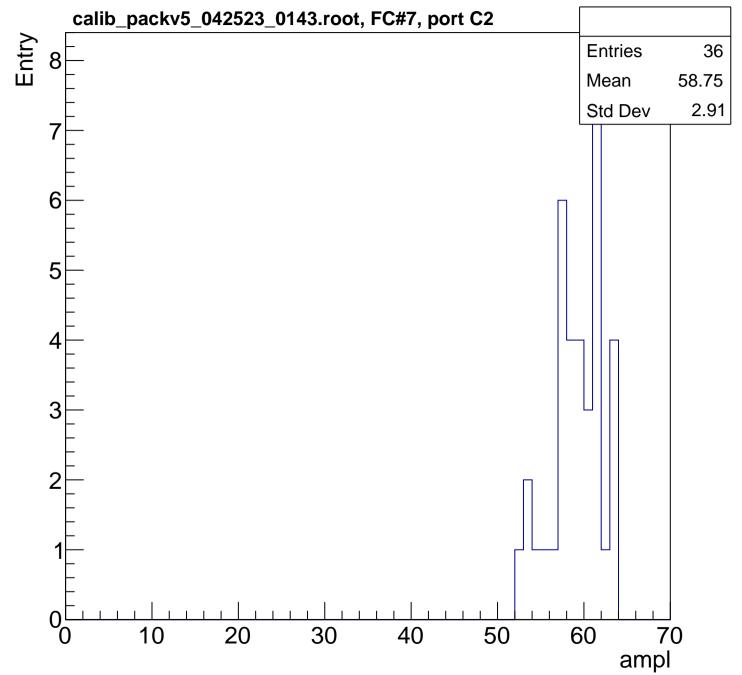


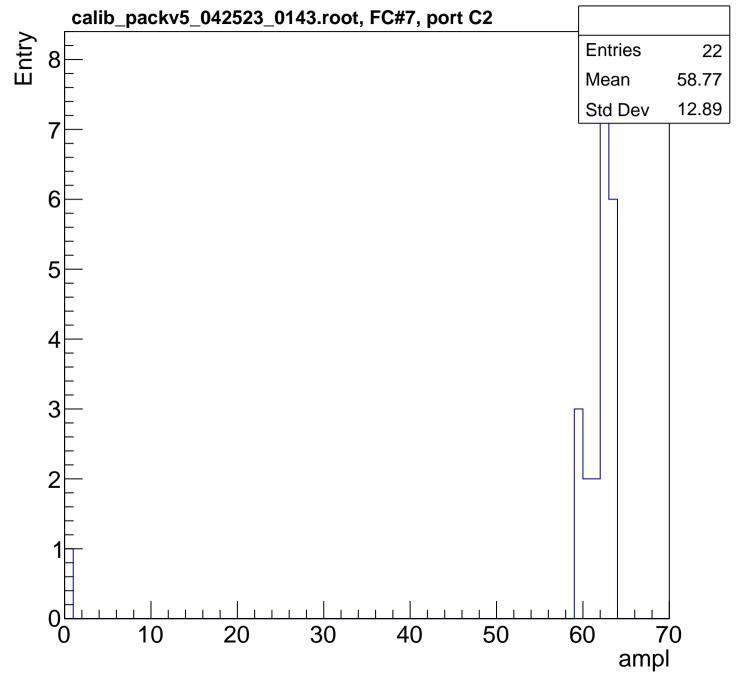


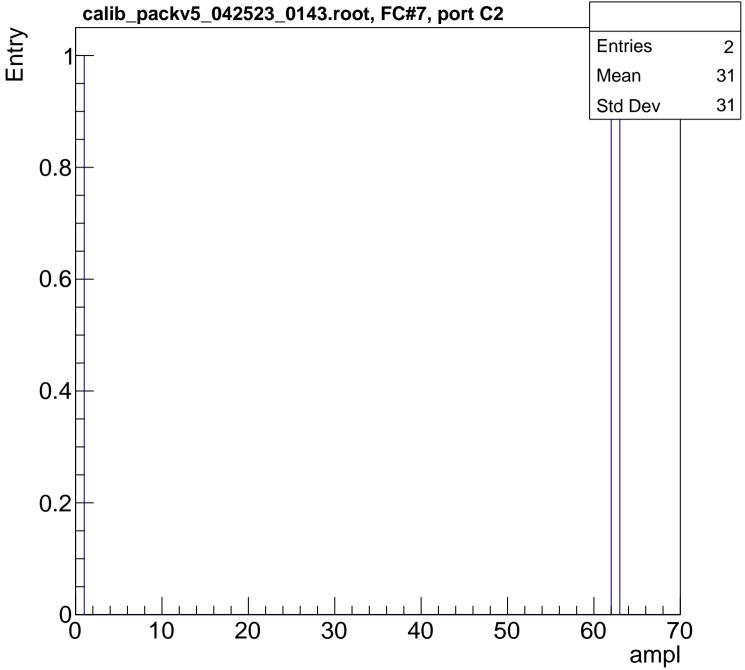


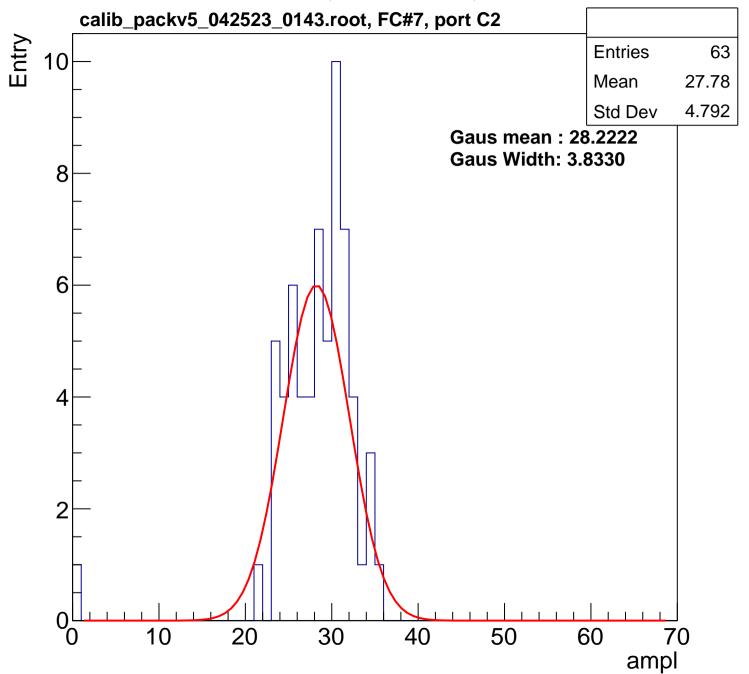


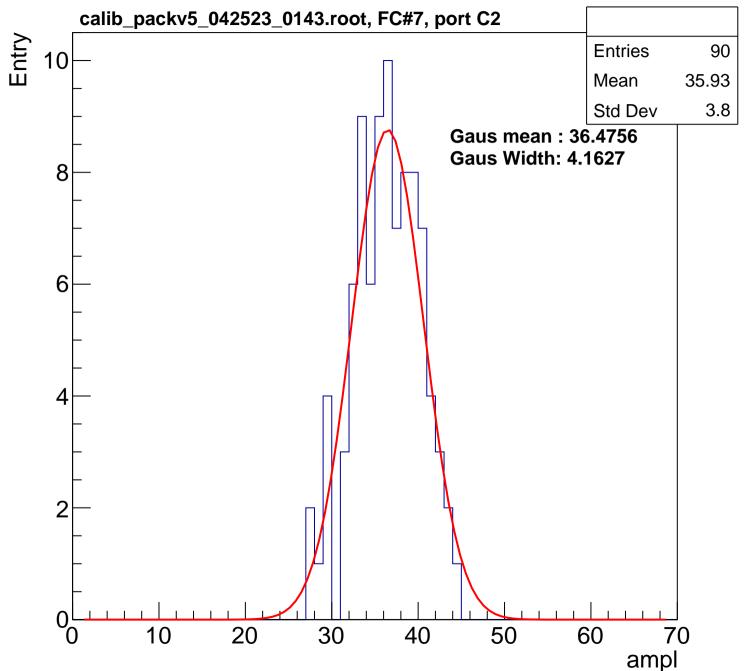


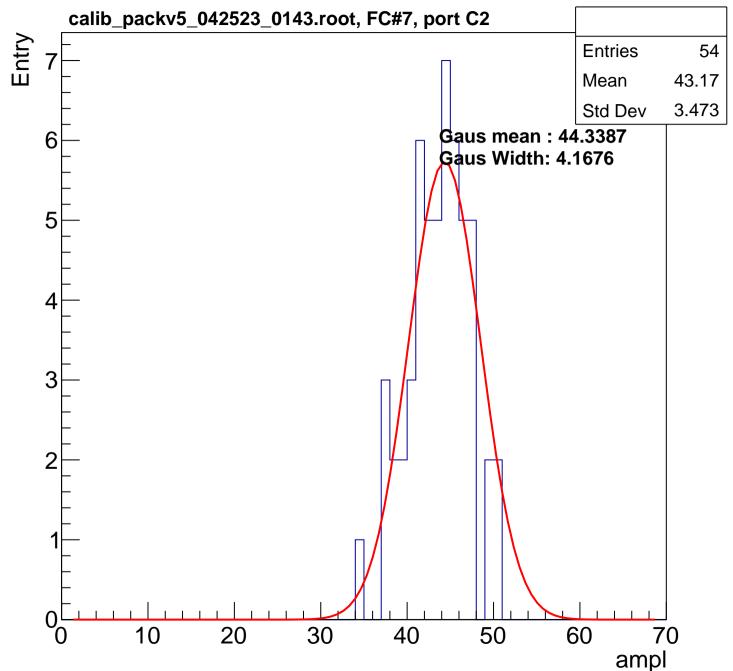


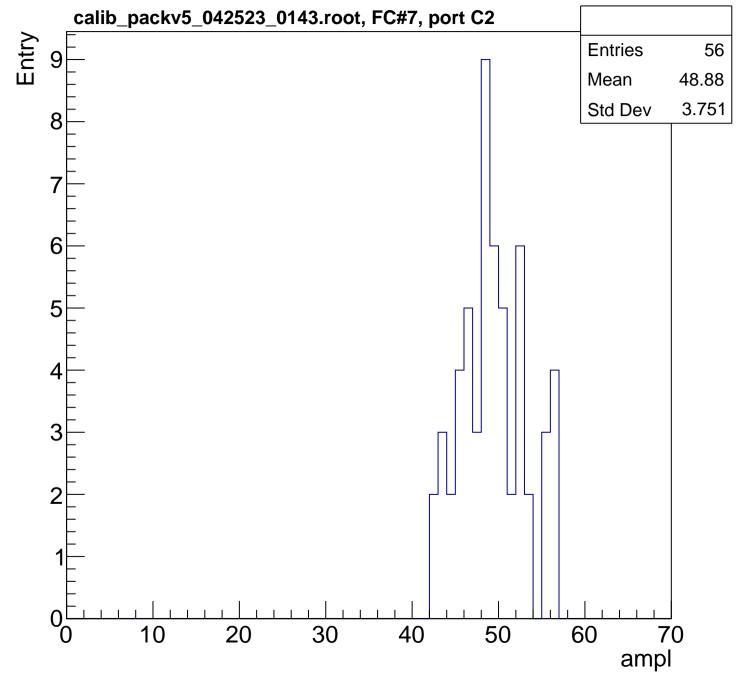


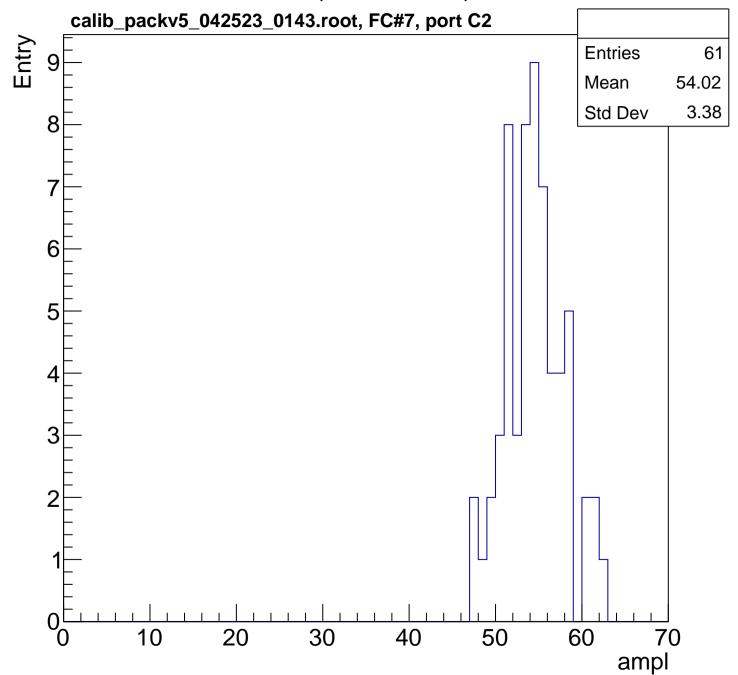


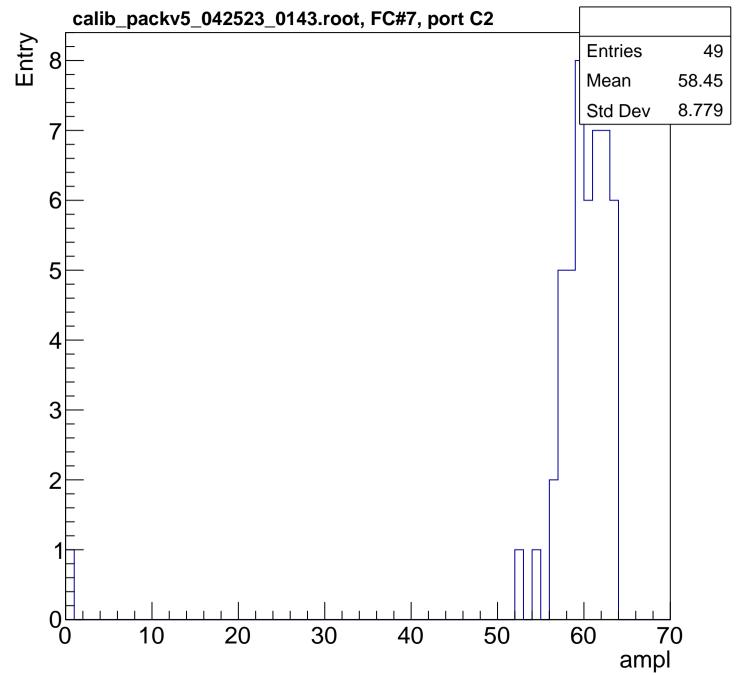


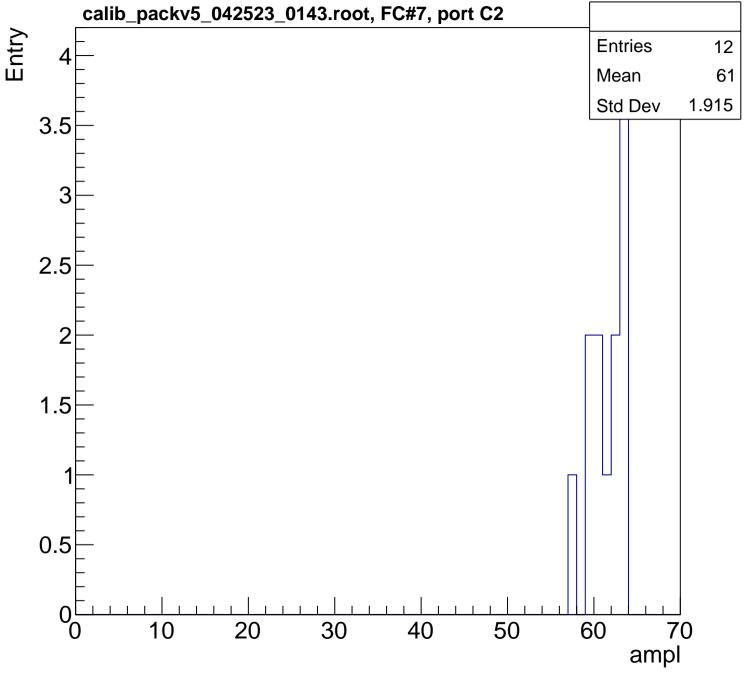




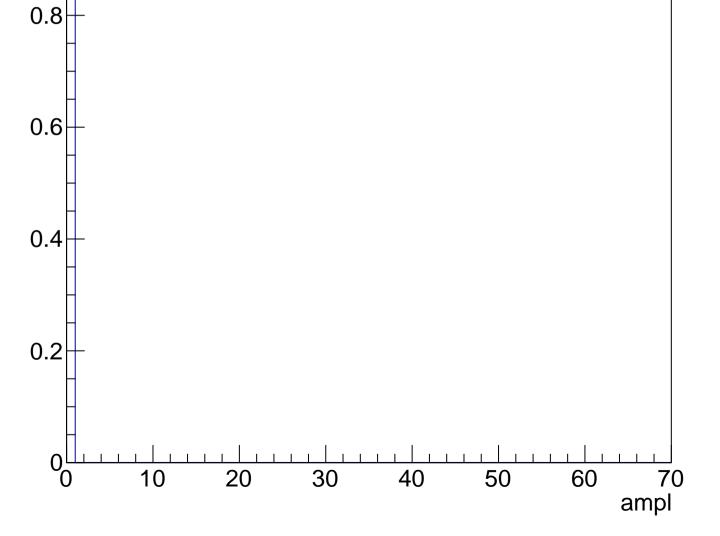


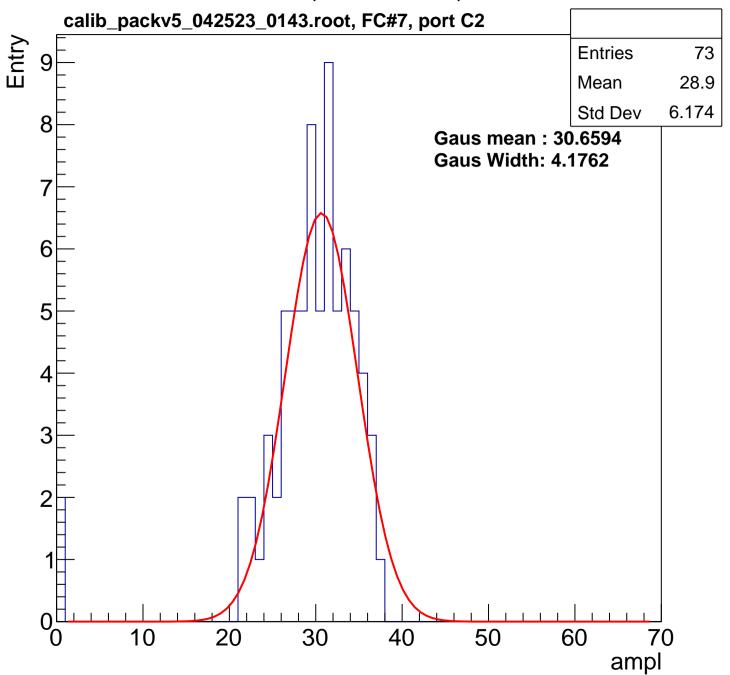


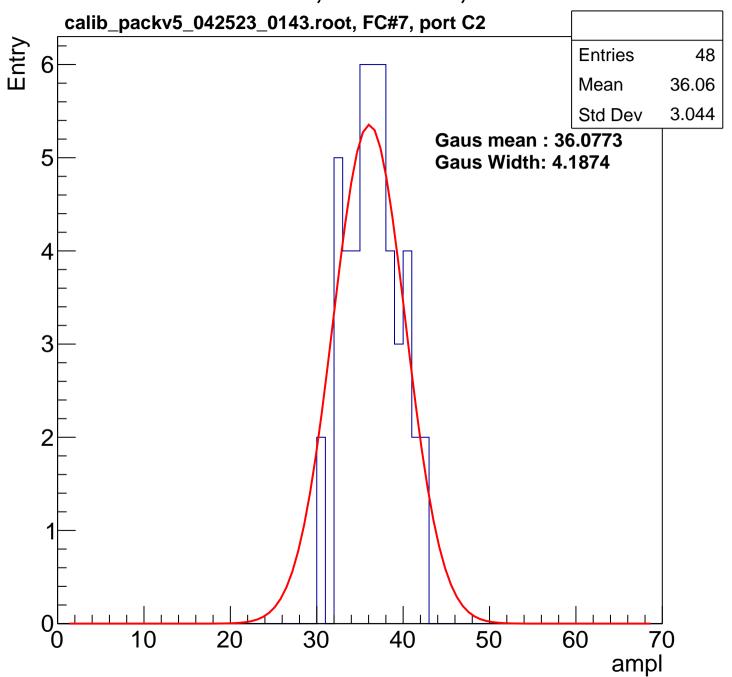


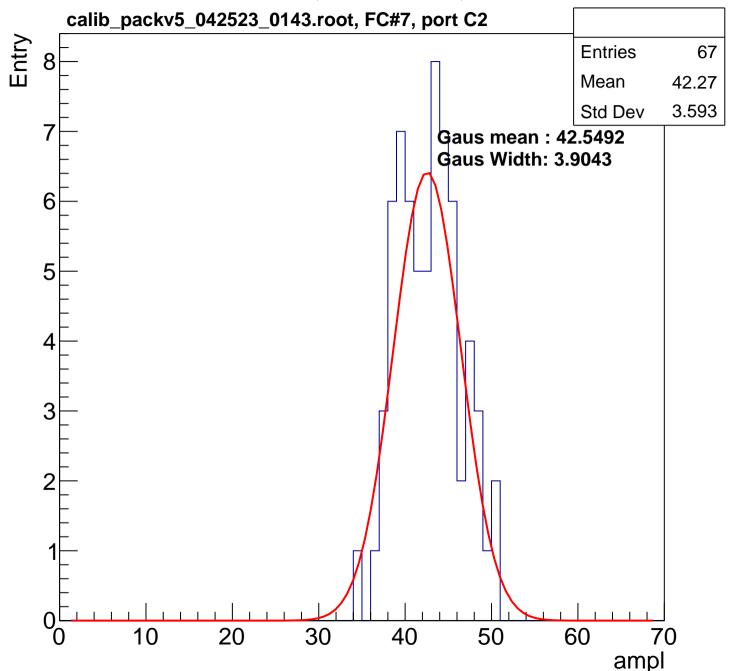


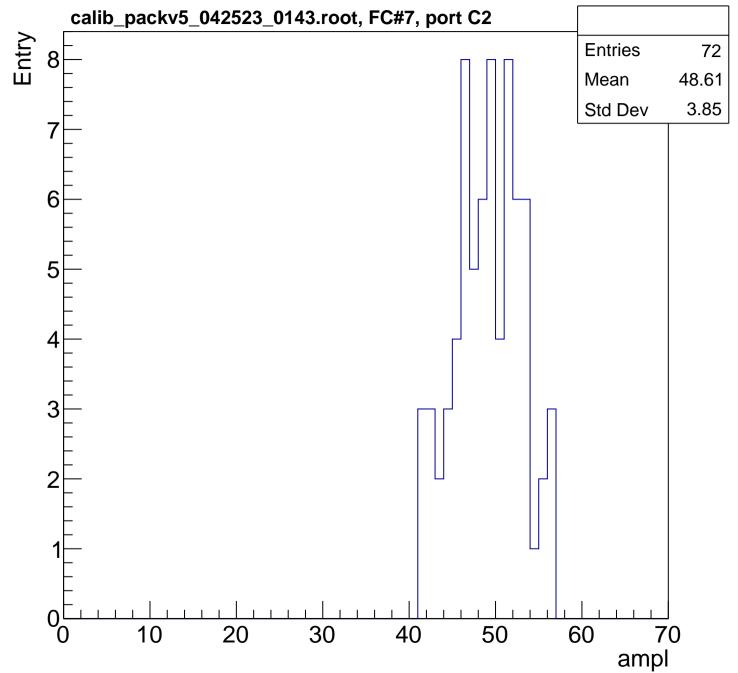
B1L103S, U4-ch91, adc7 calib_packv5_042523_0143.root, FC#7, port C2 Entry **Entries** 1 Mean 0 Std Dev 0 8.0 0.6 0.4 0.2

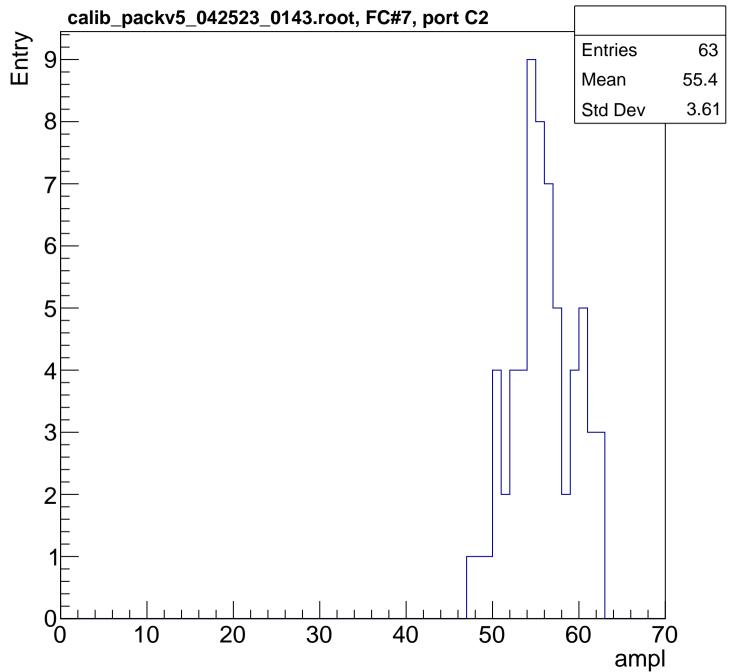


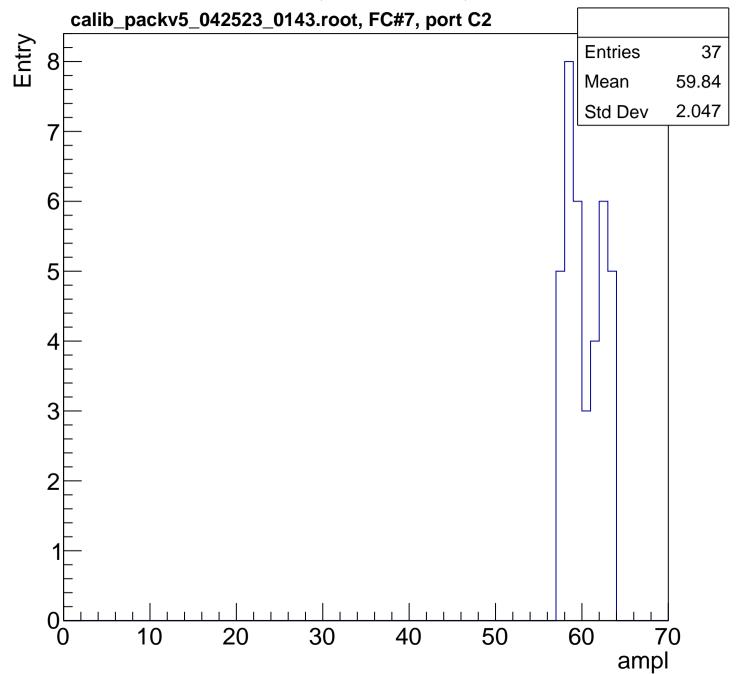


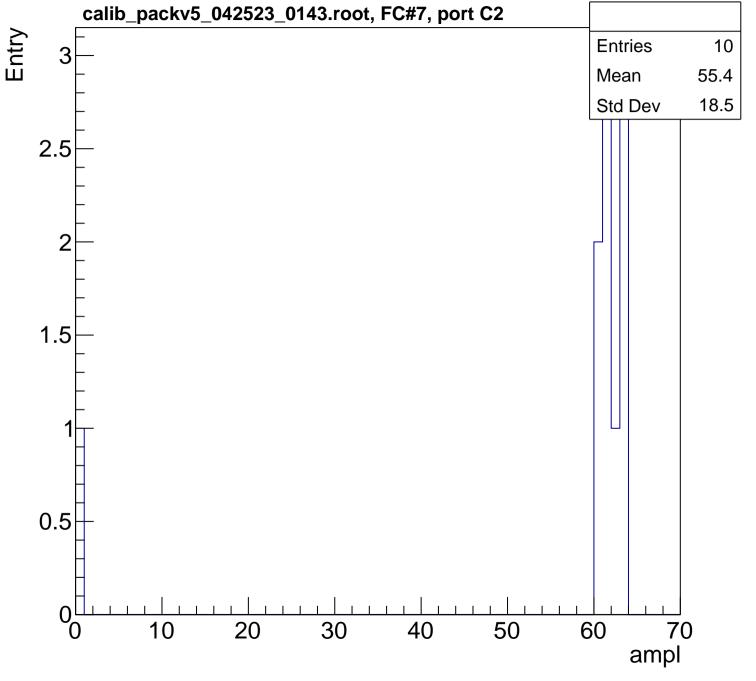


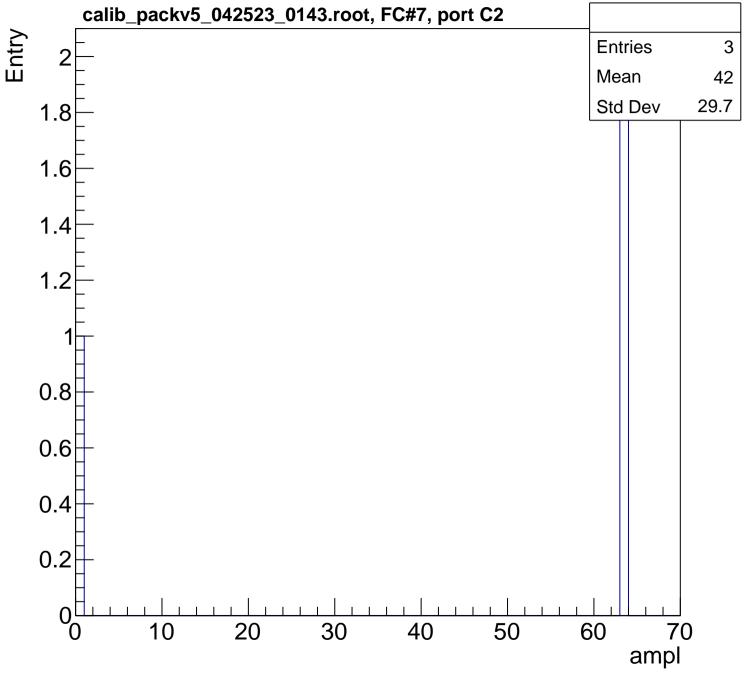


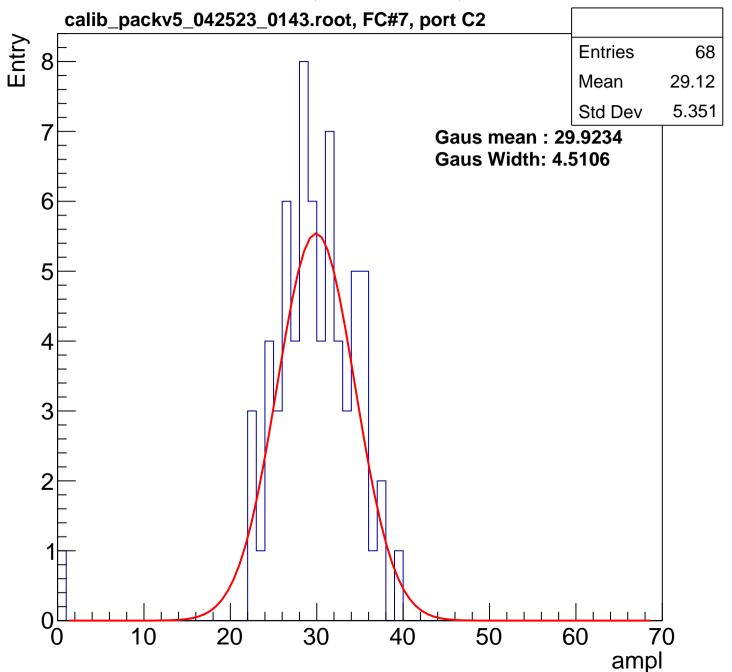


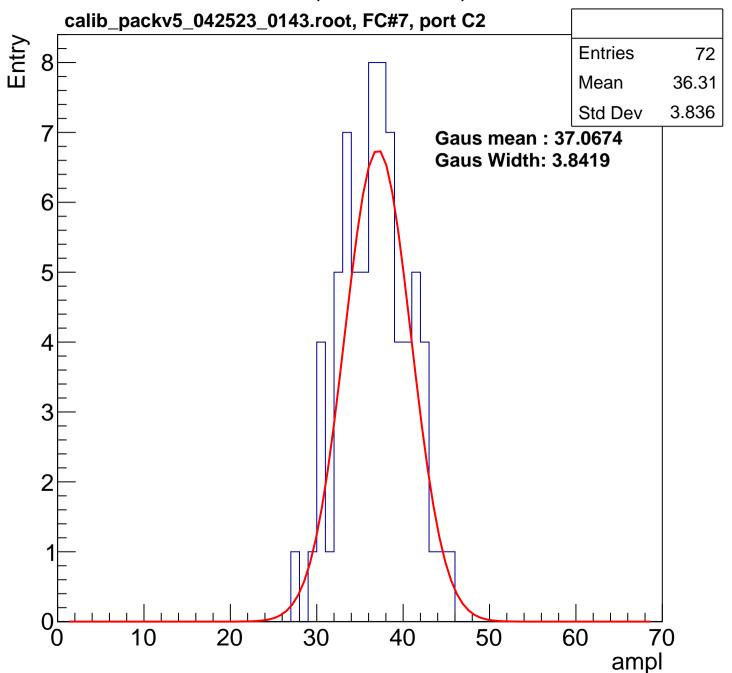


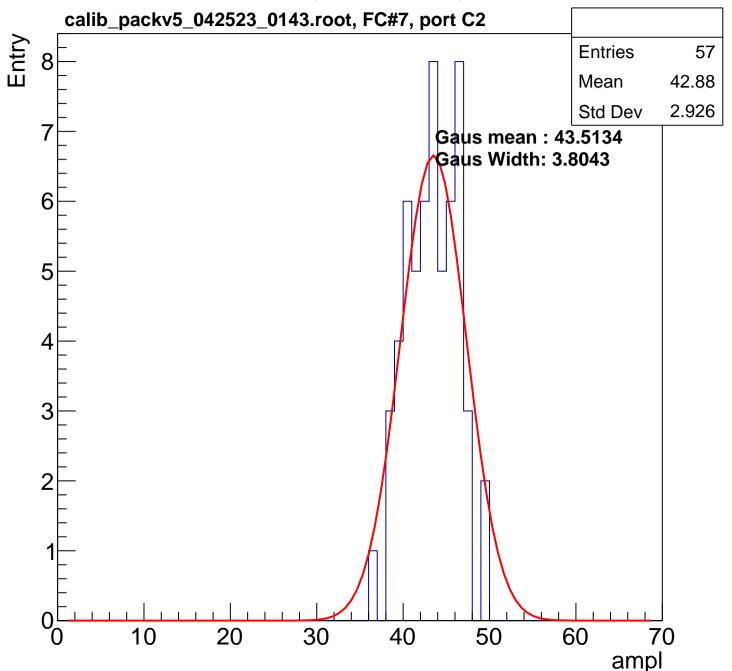


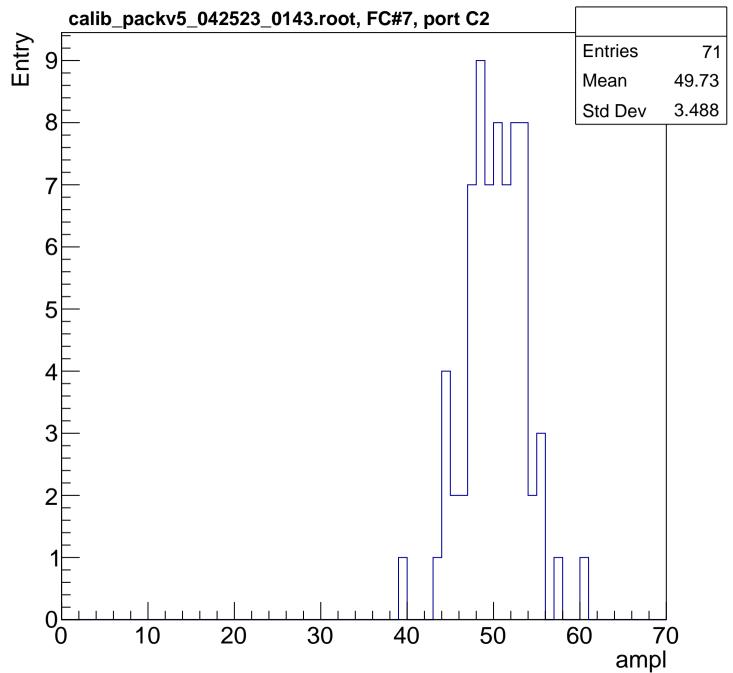


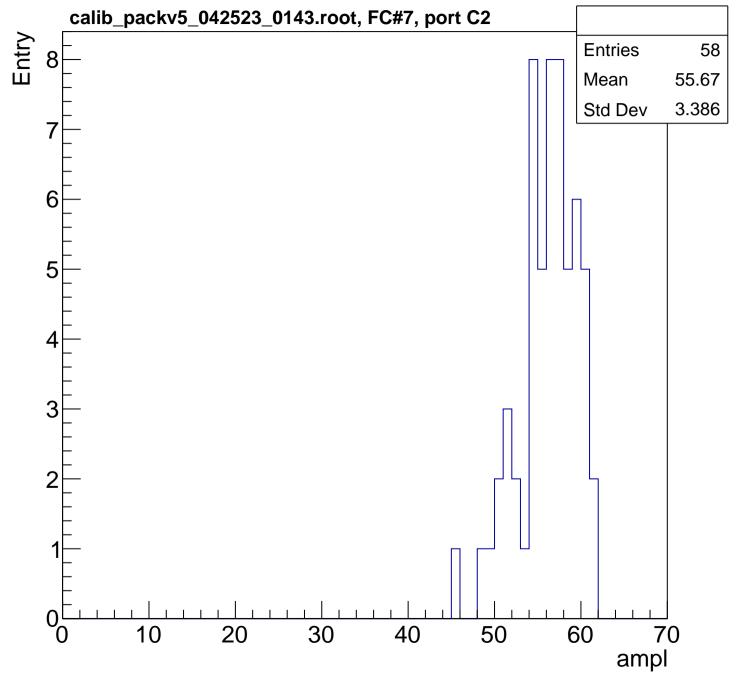


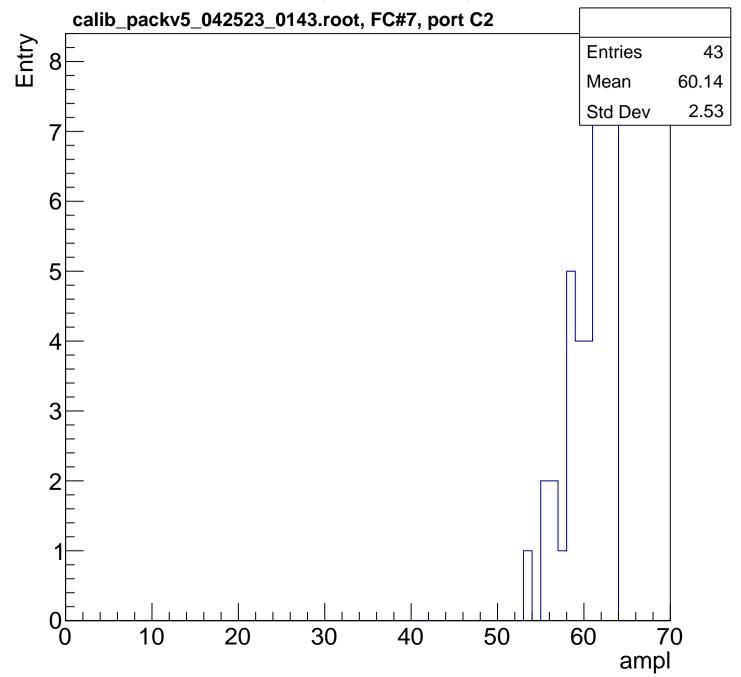


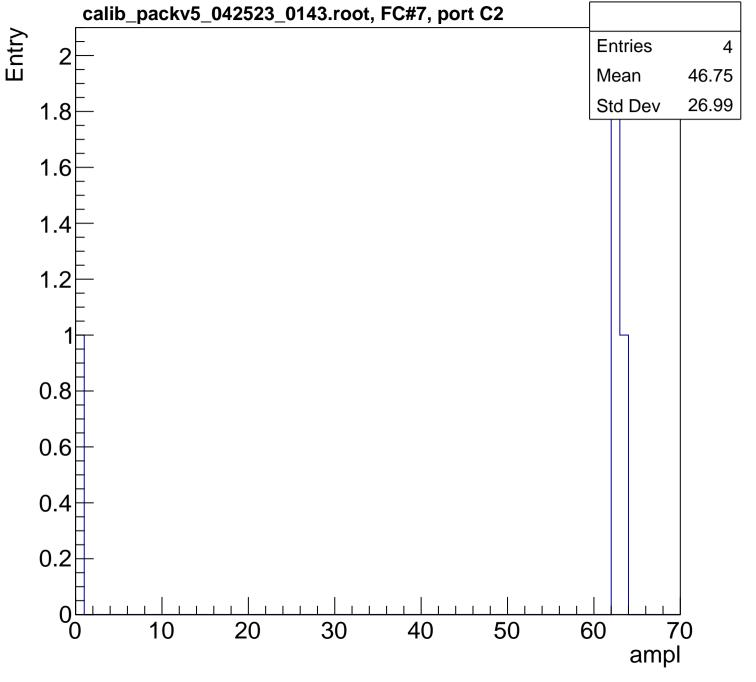




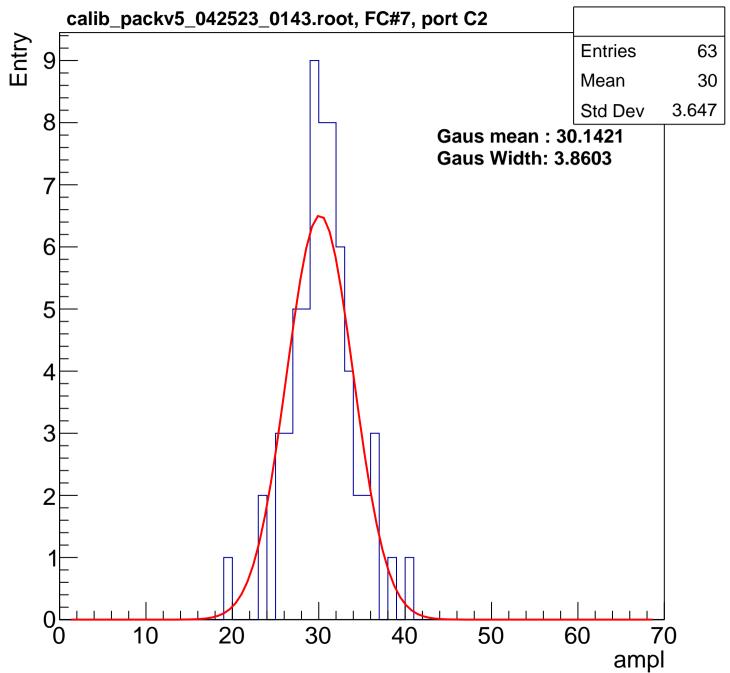


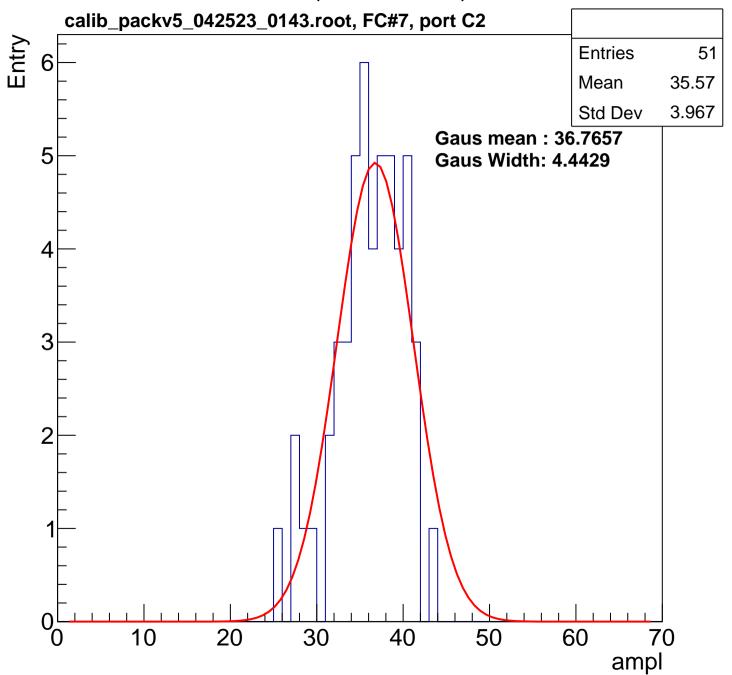


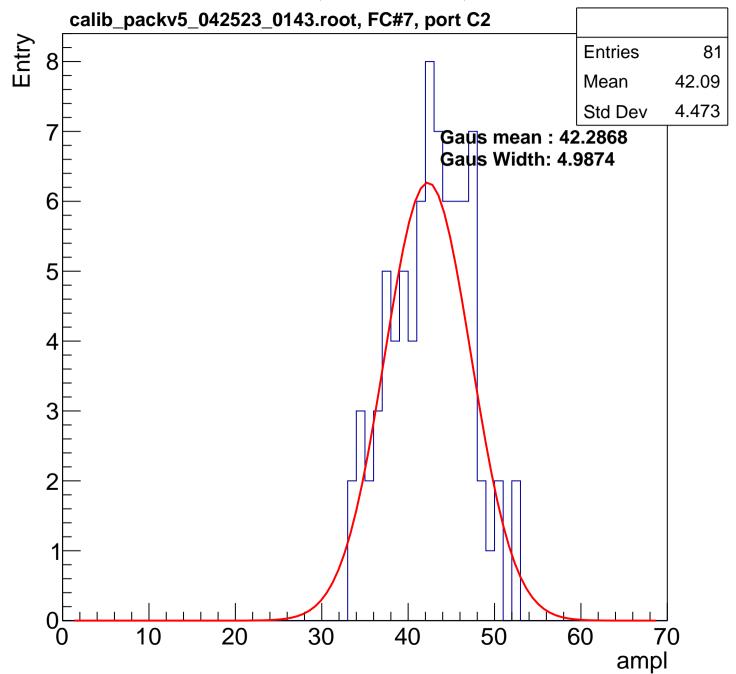


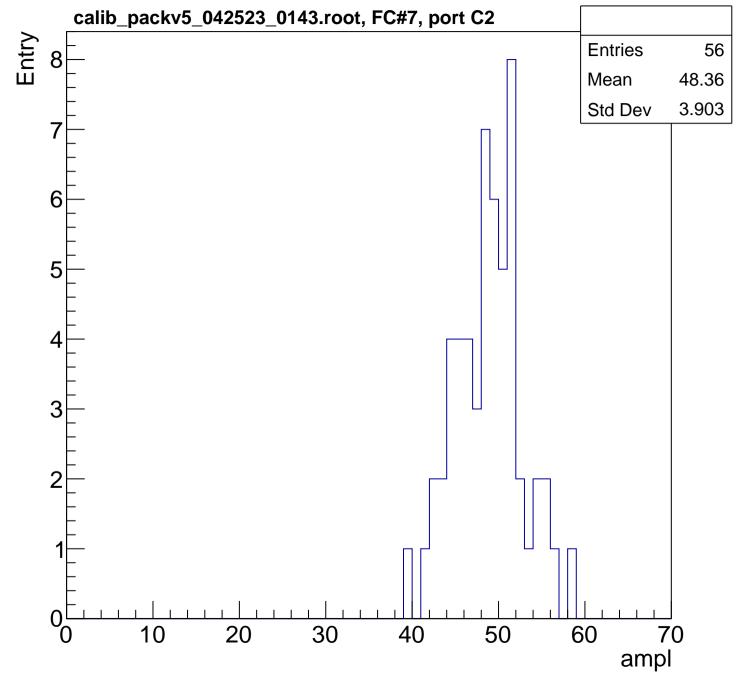


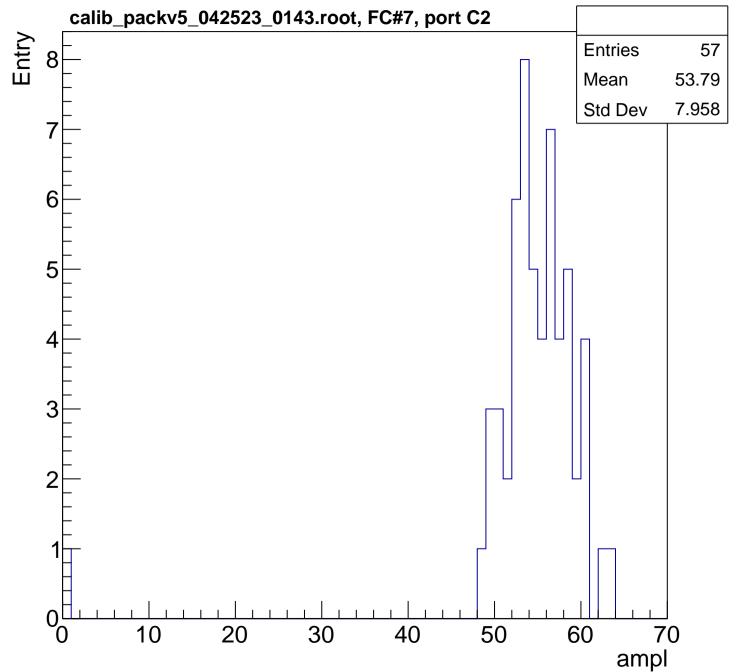


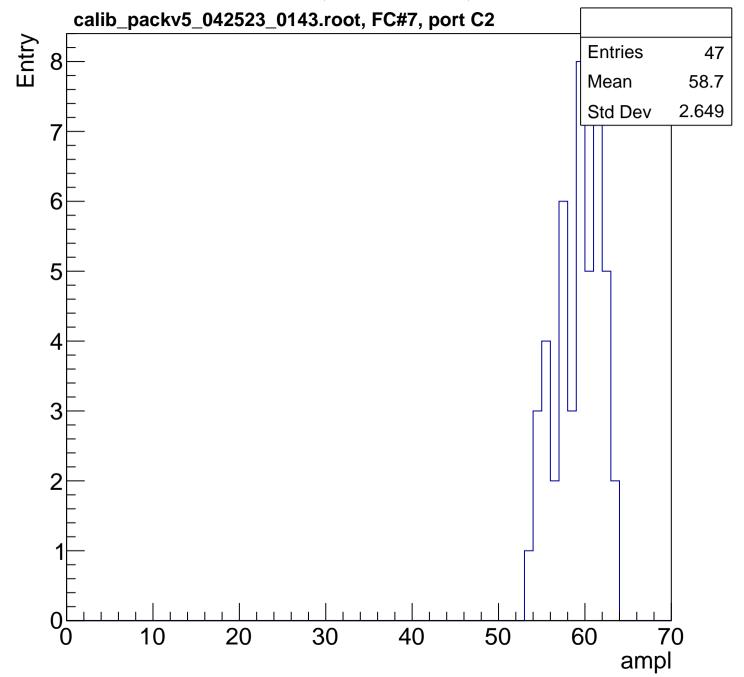


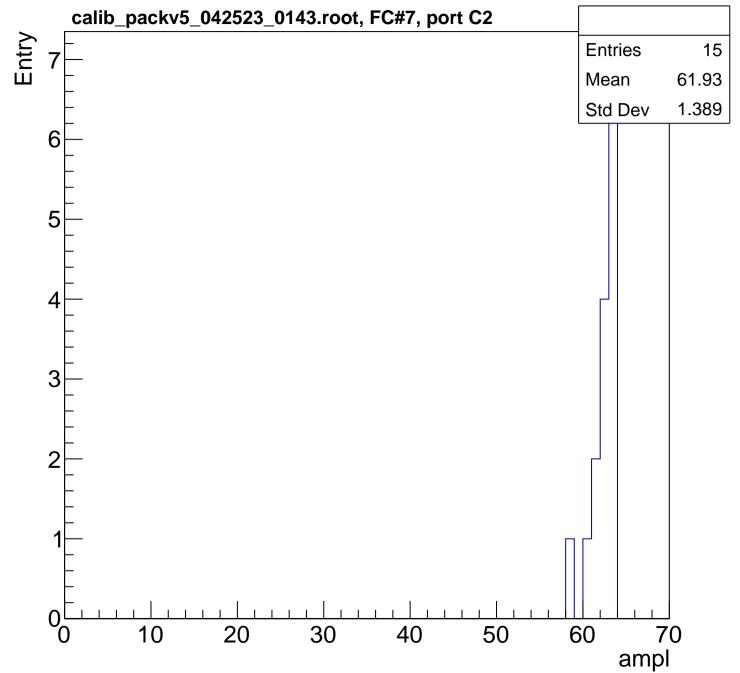


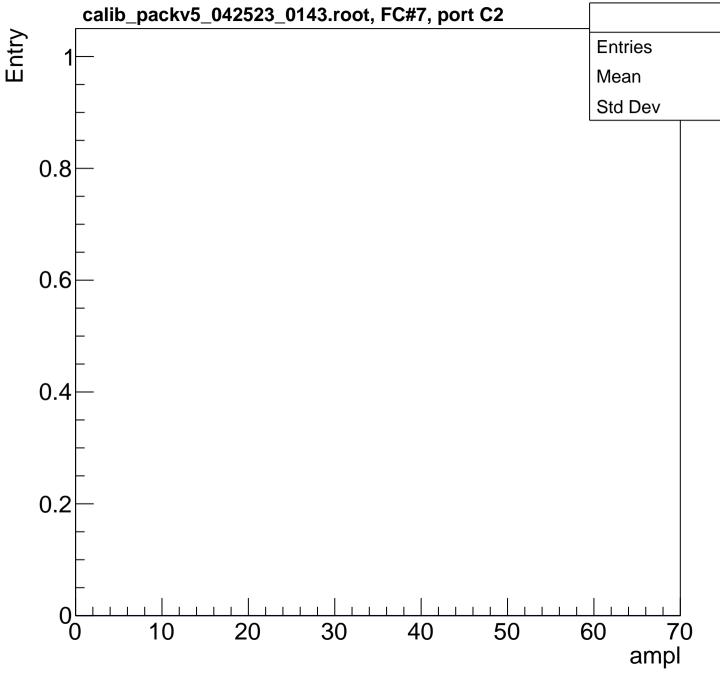


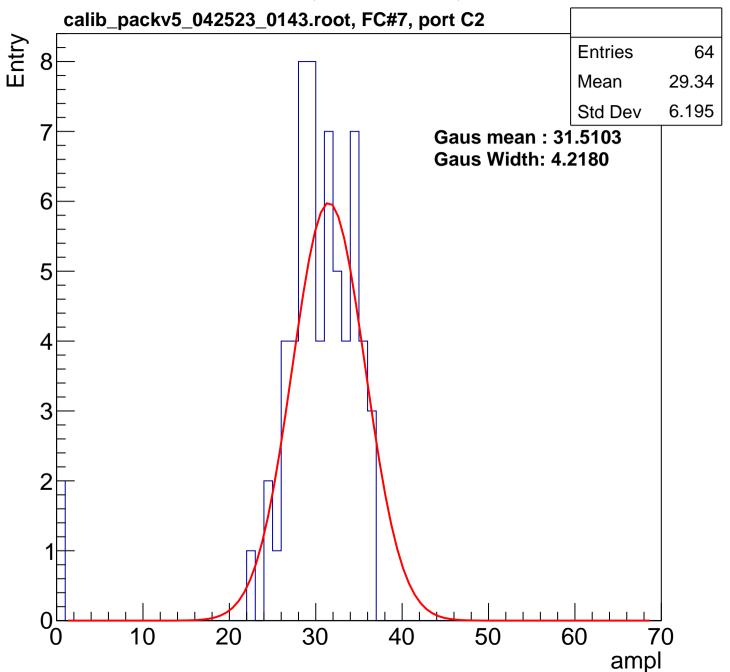


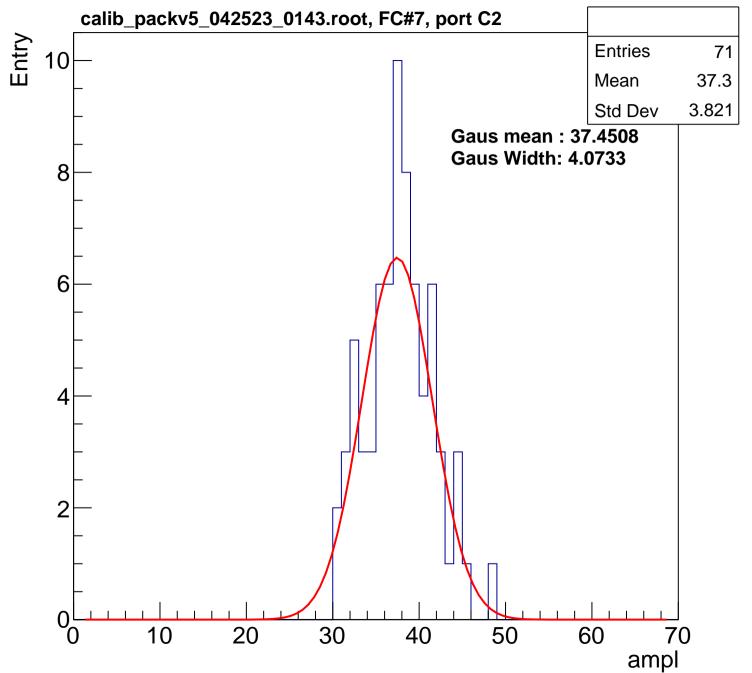


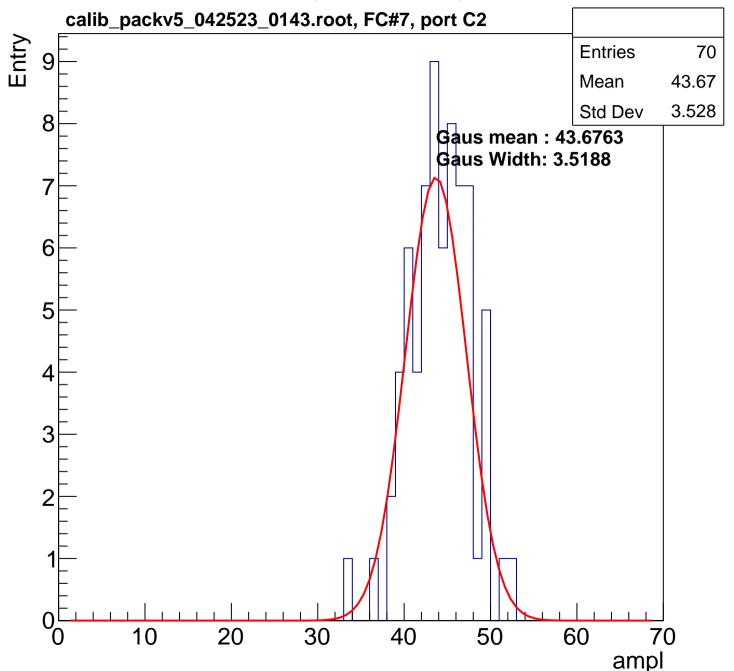


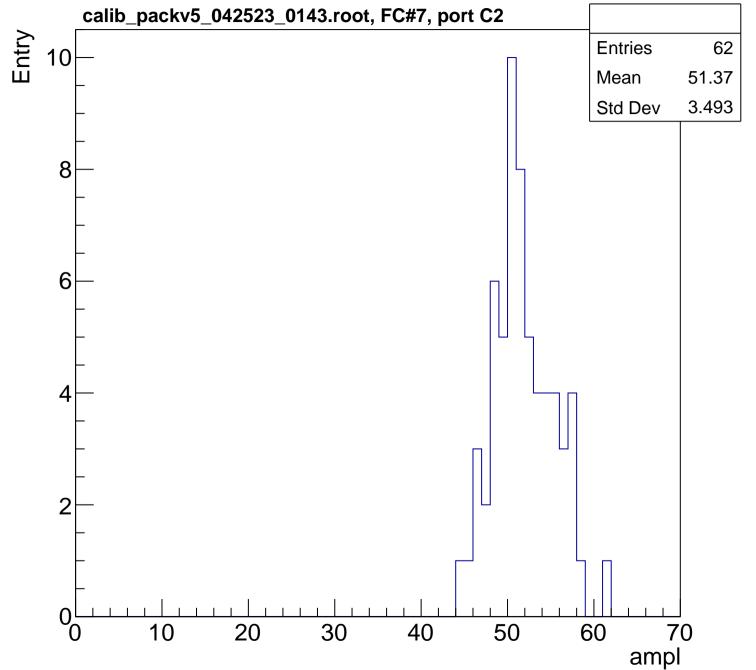


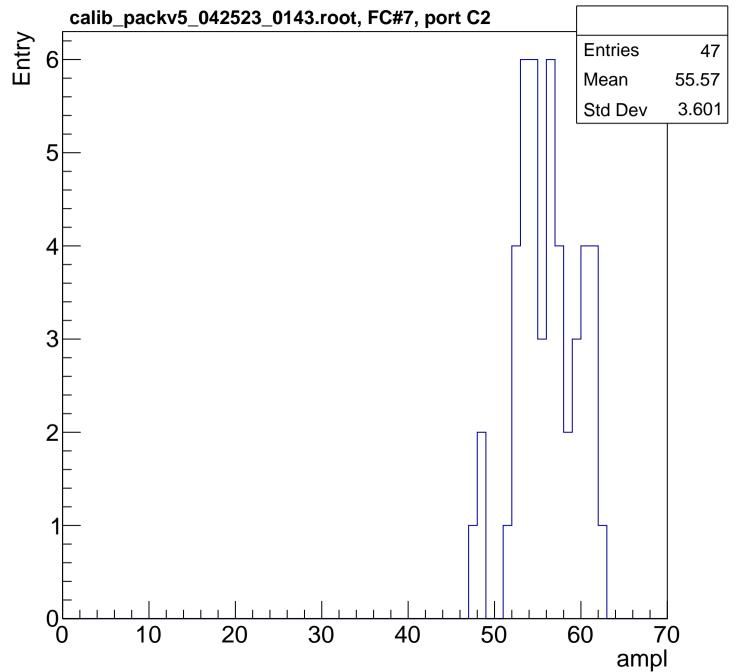


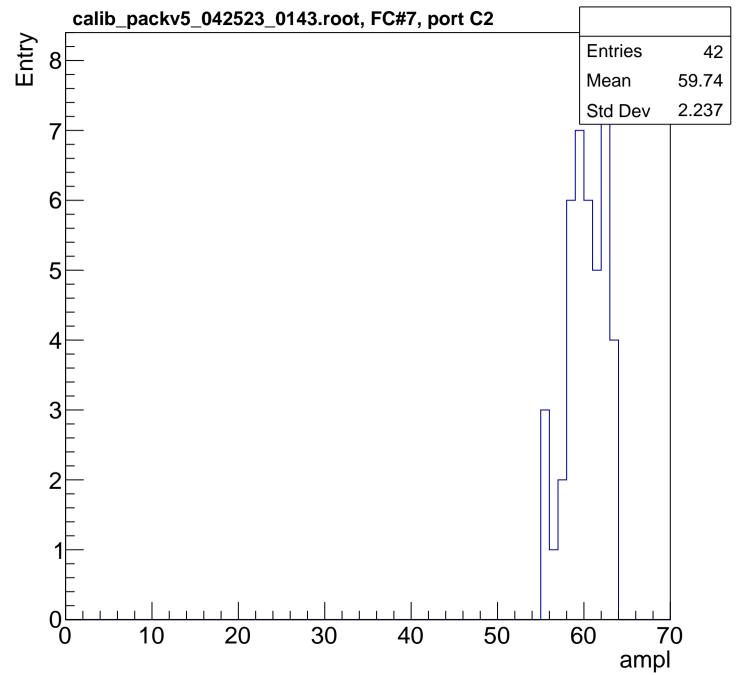


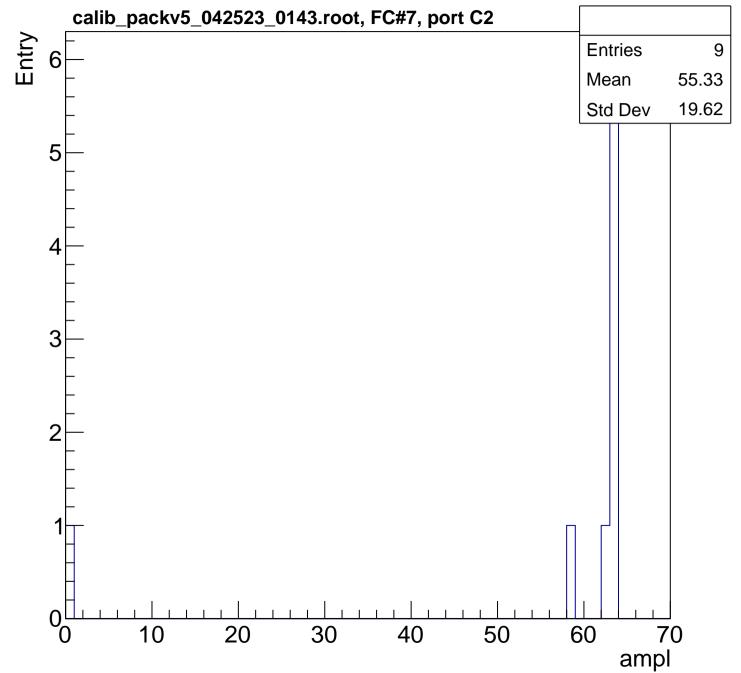


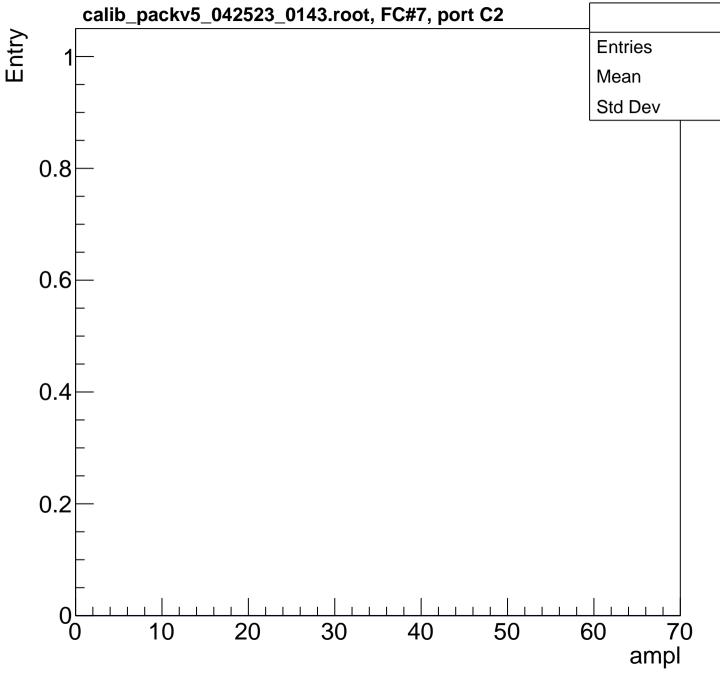


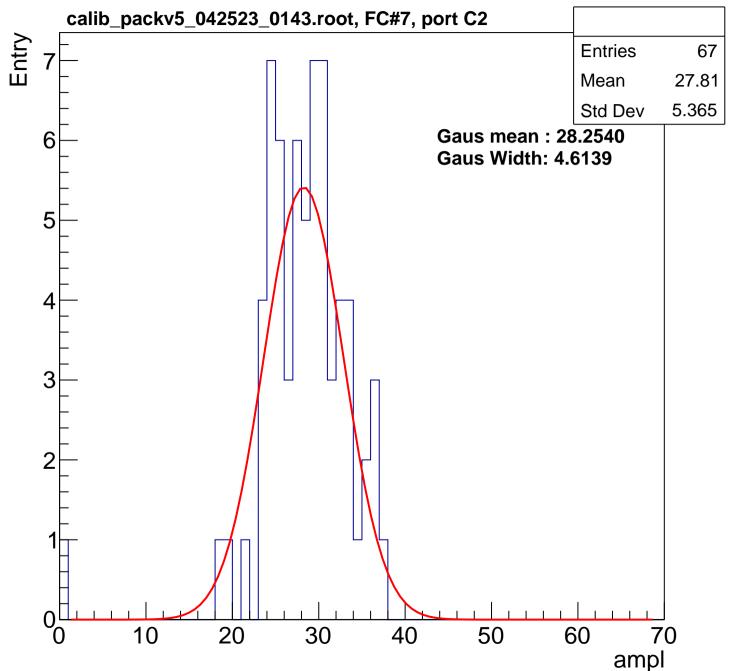


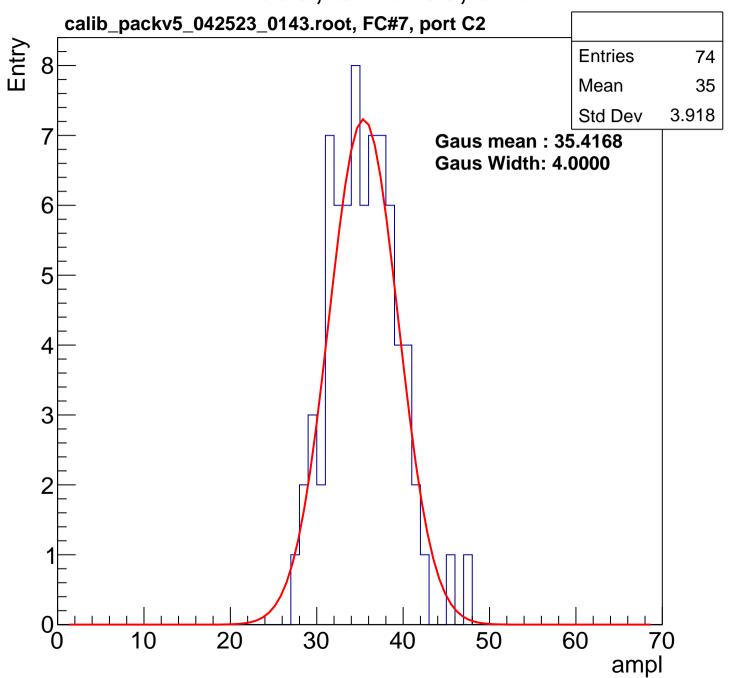


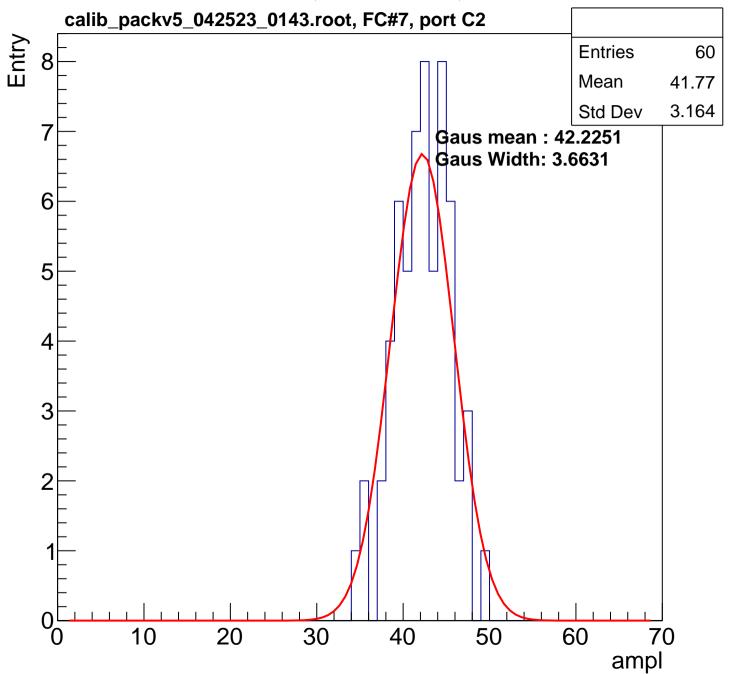


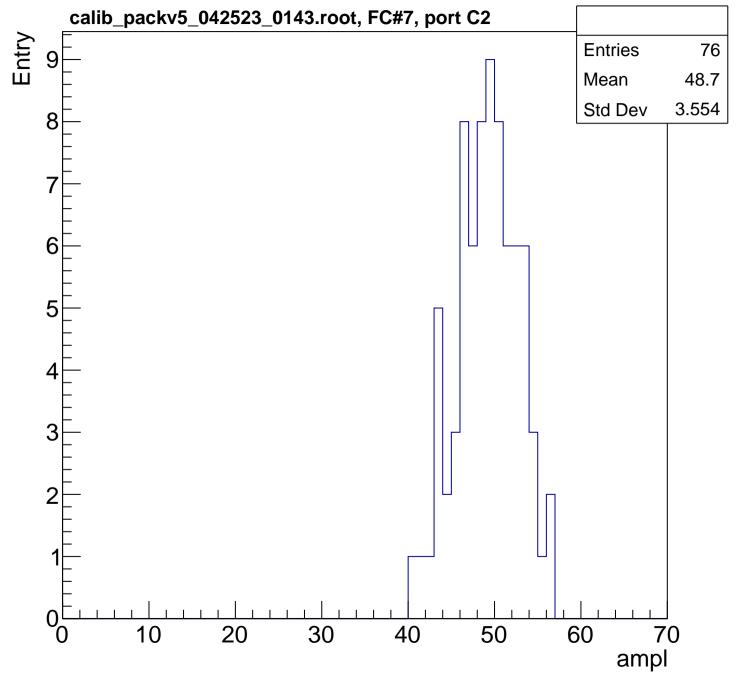


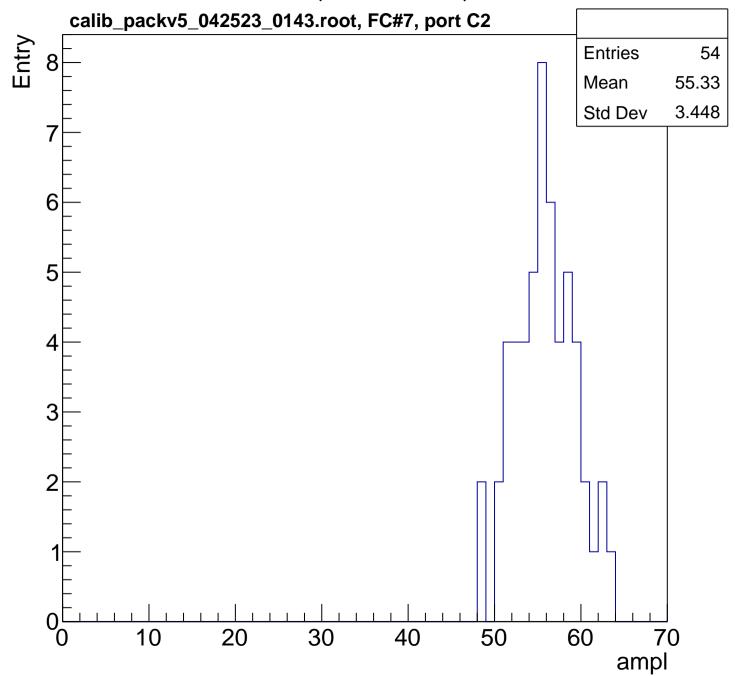


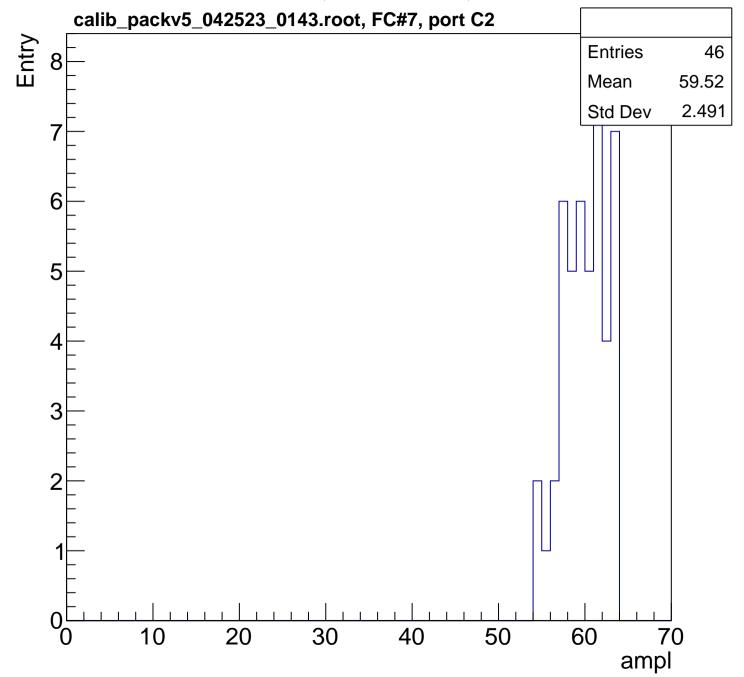


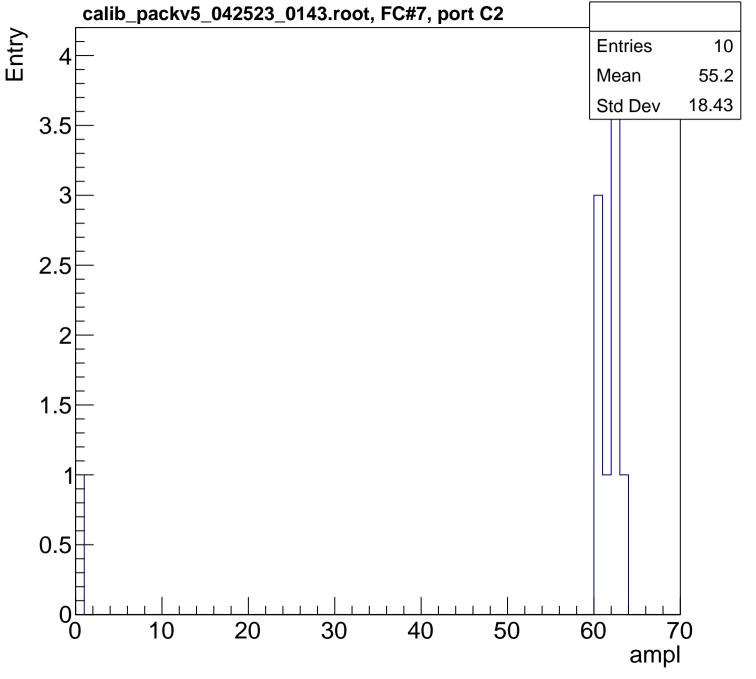


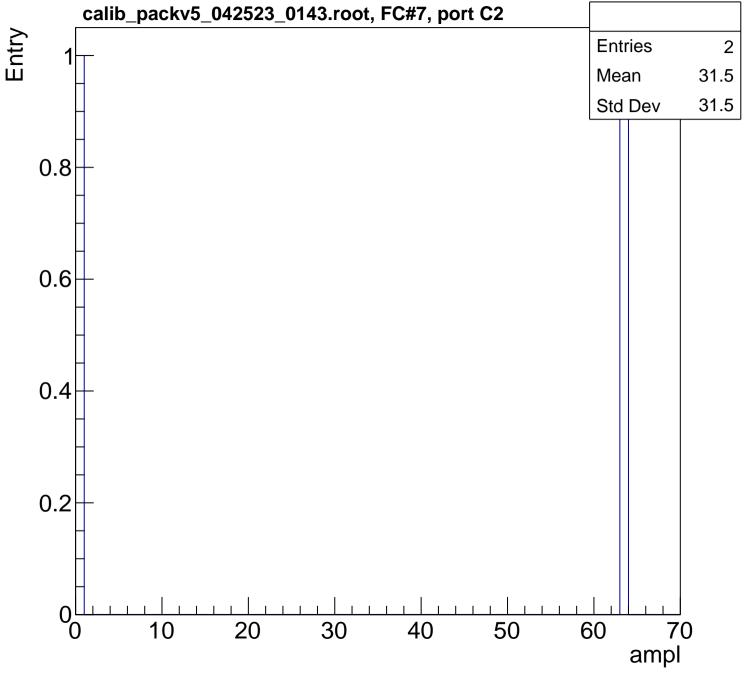


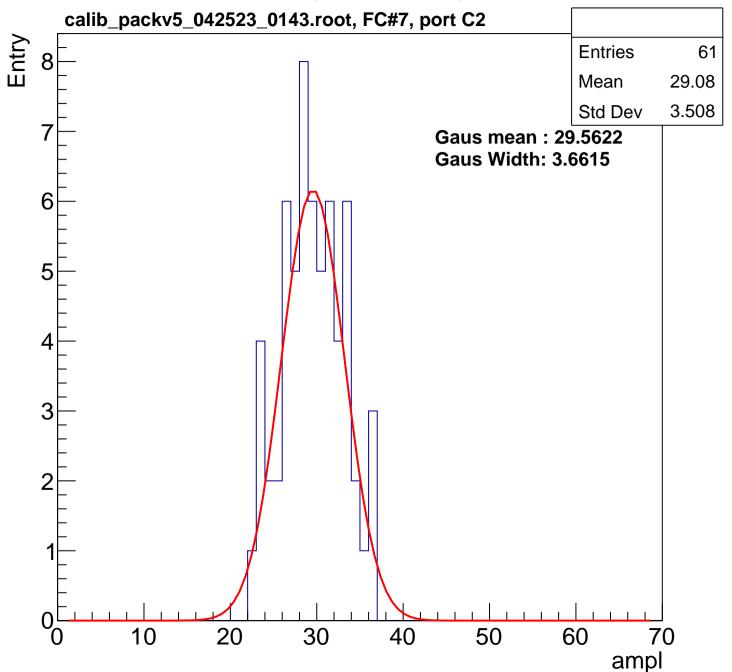


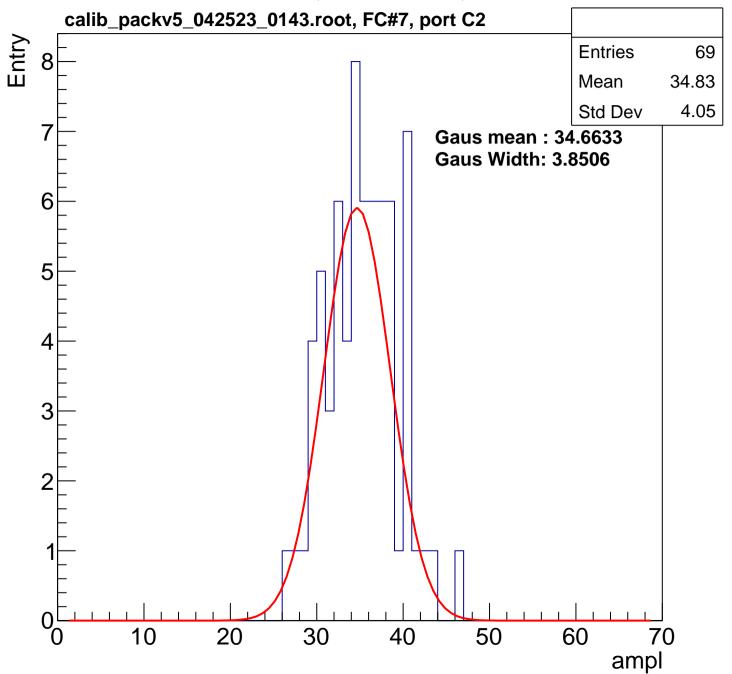


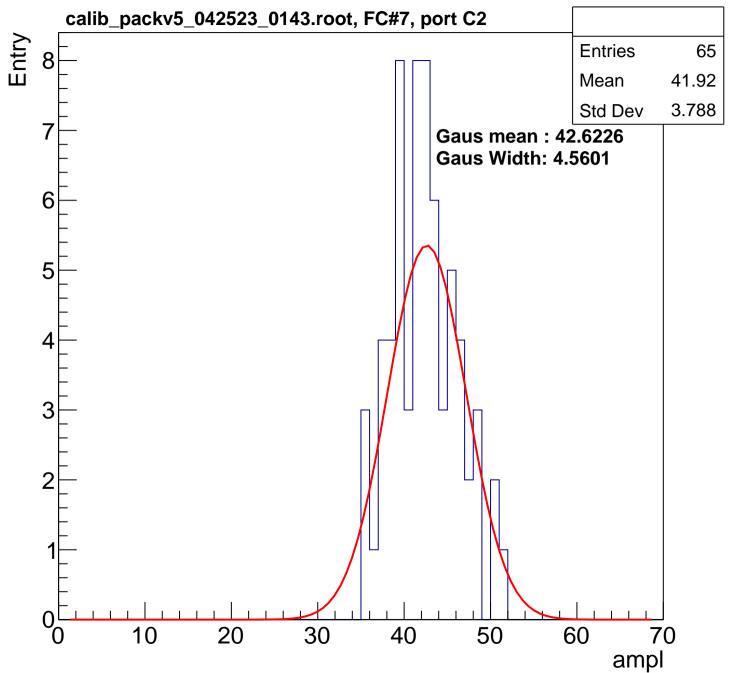




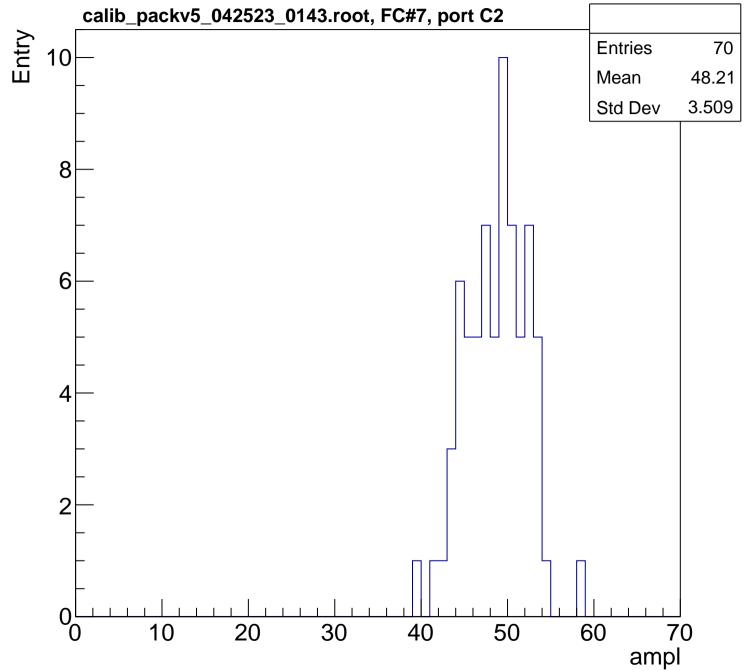


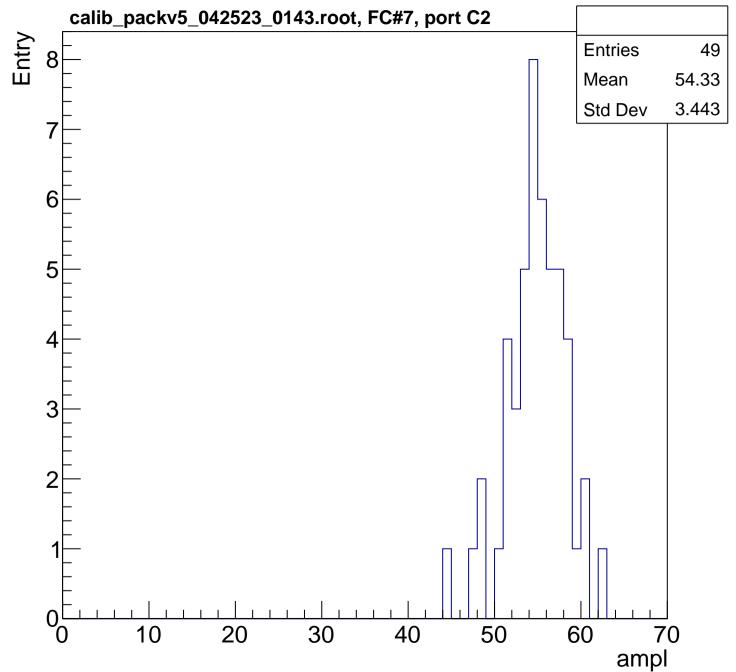


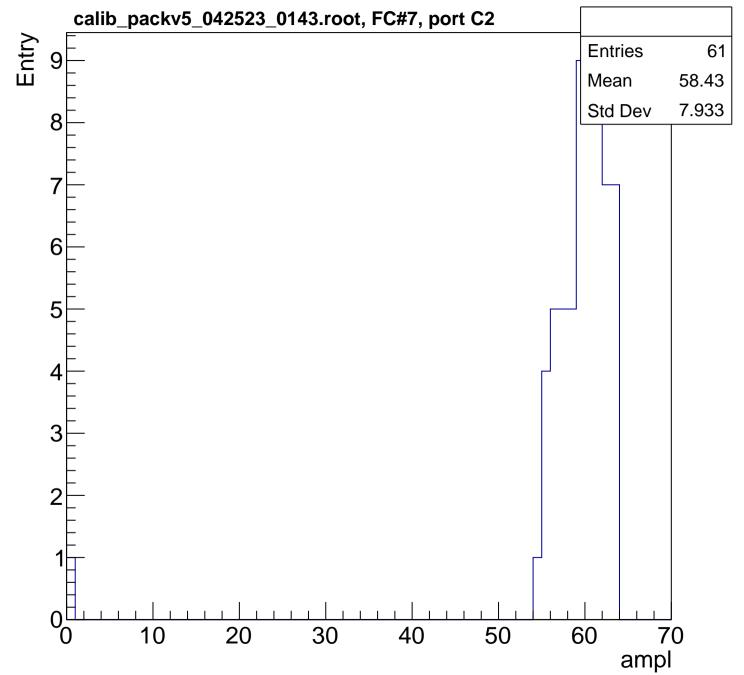


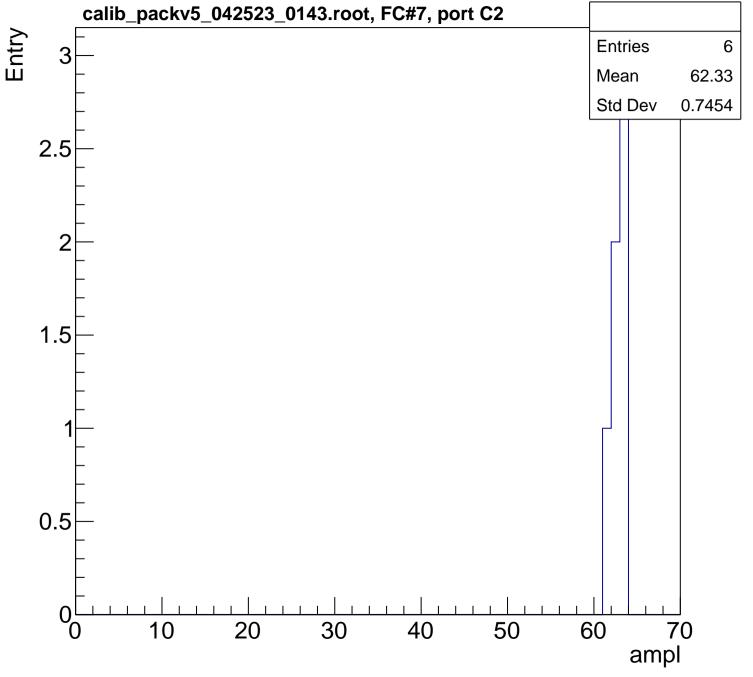


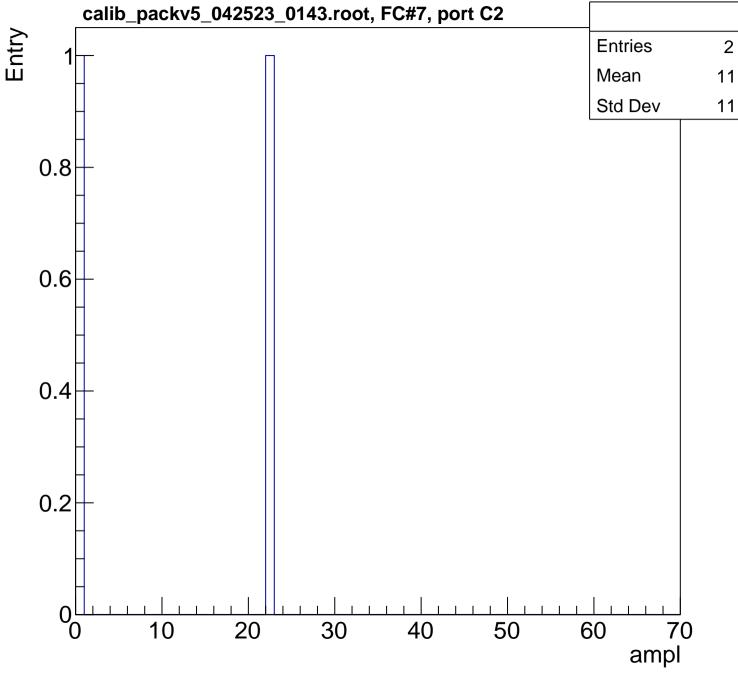
B1L103S, U4-ch97, adc3

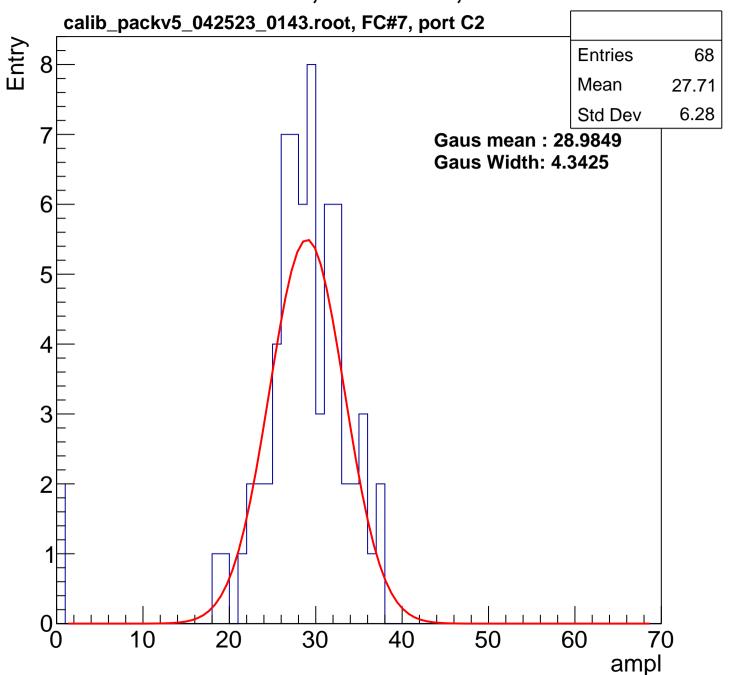


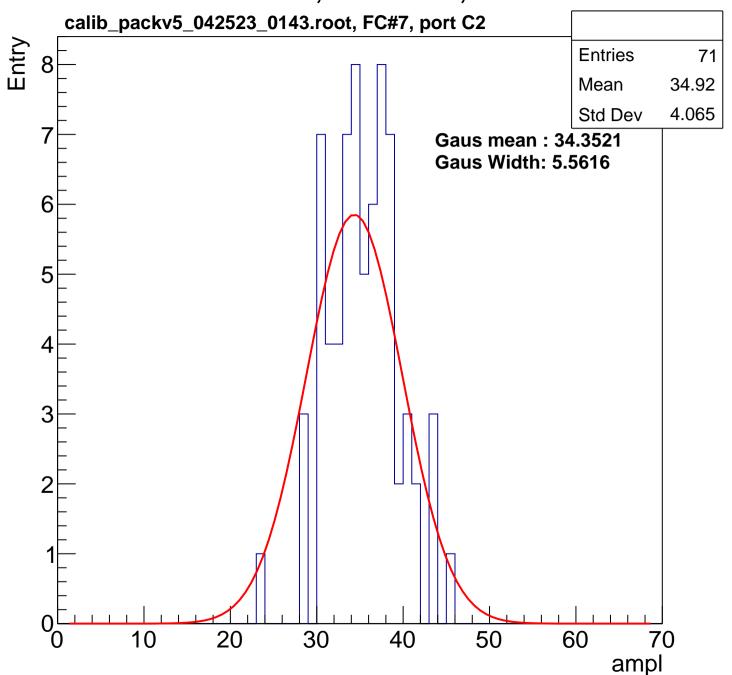


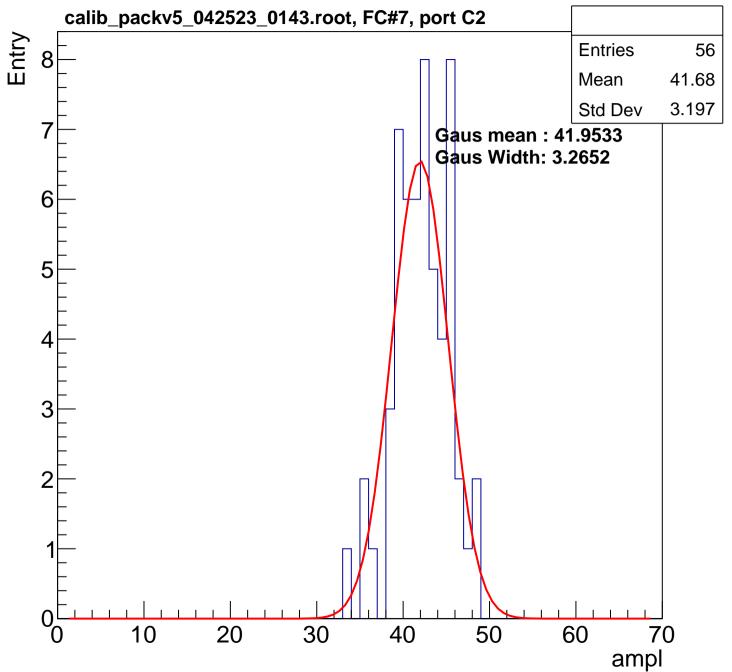


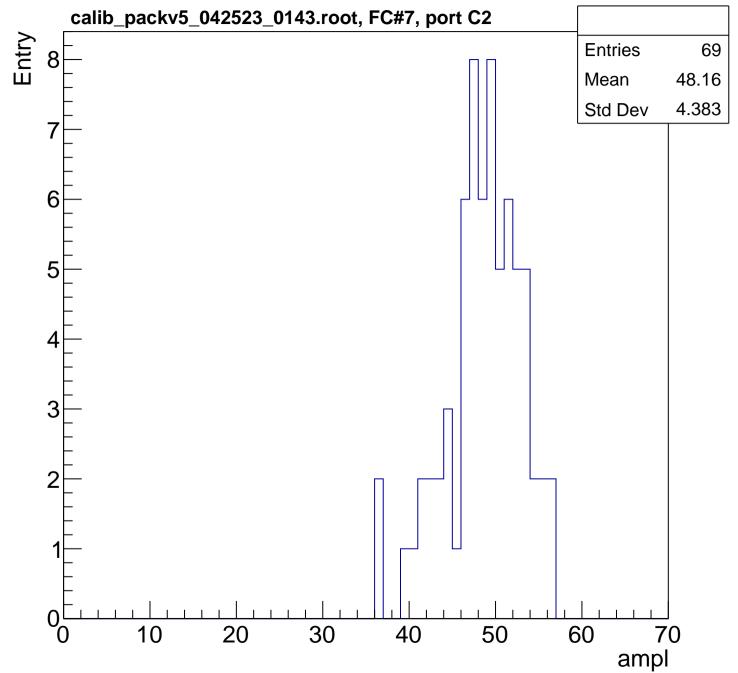


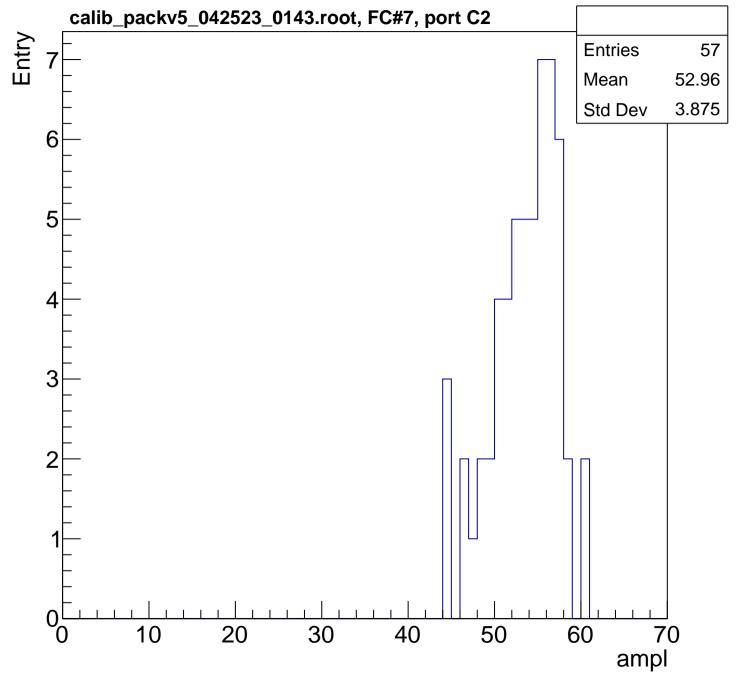


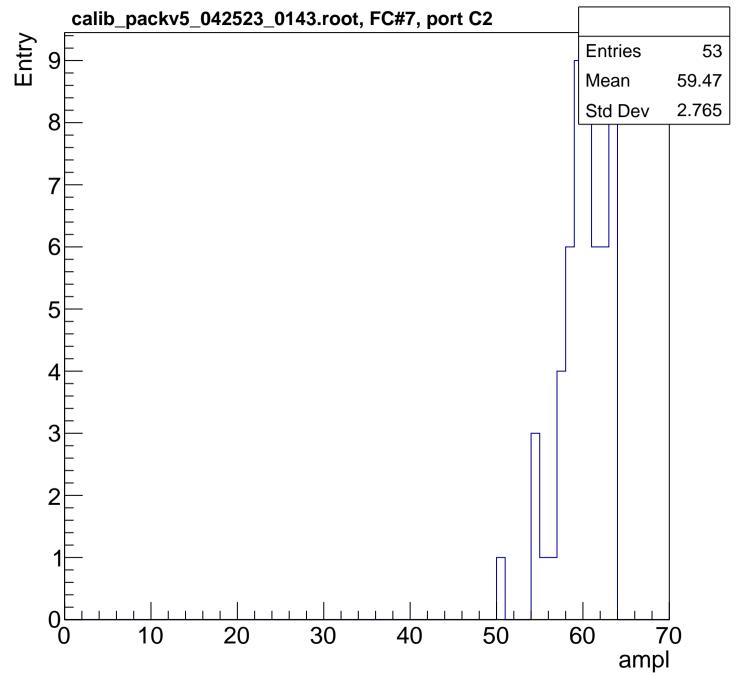


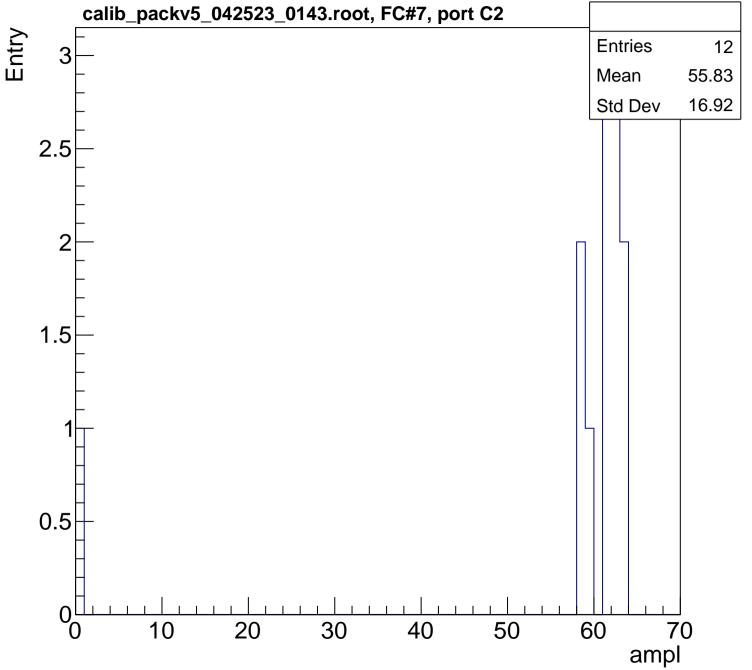


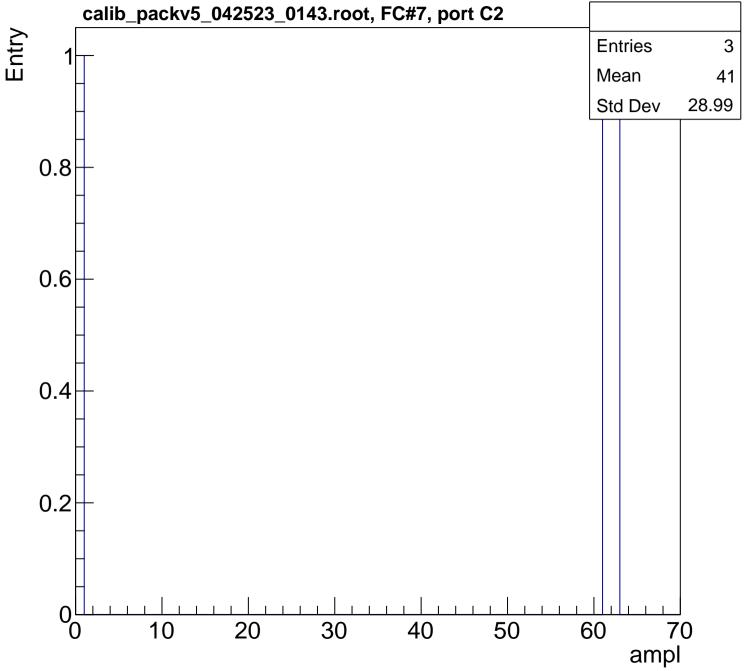


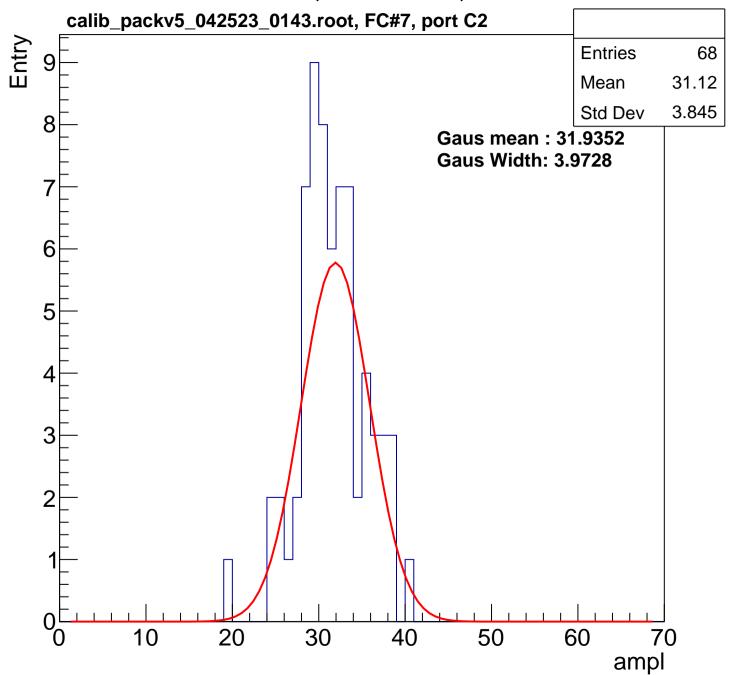


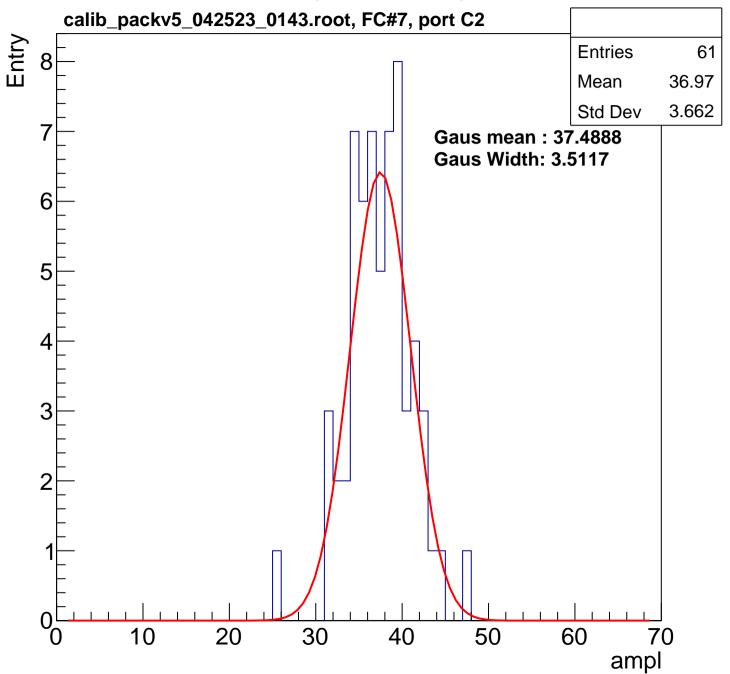


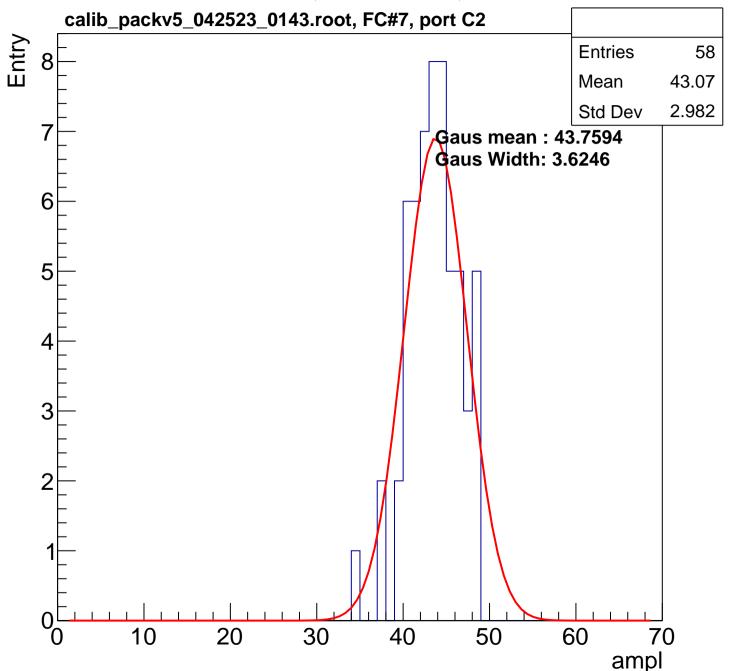


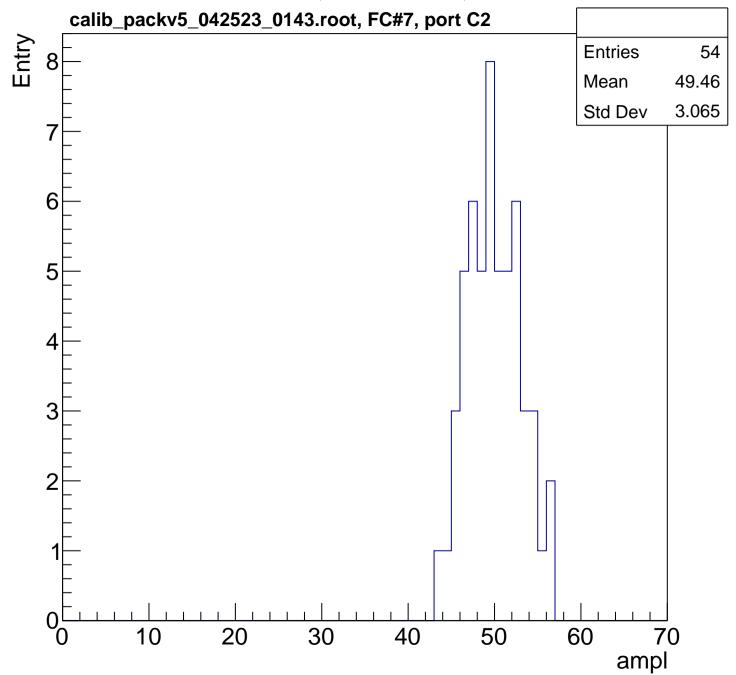


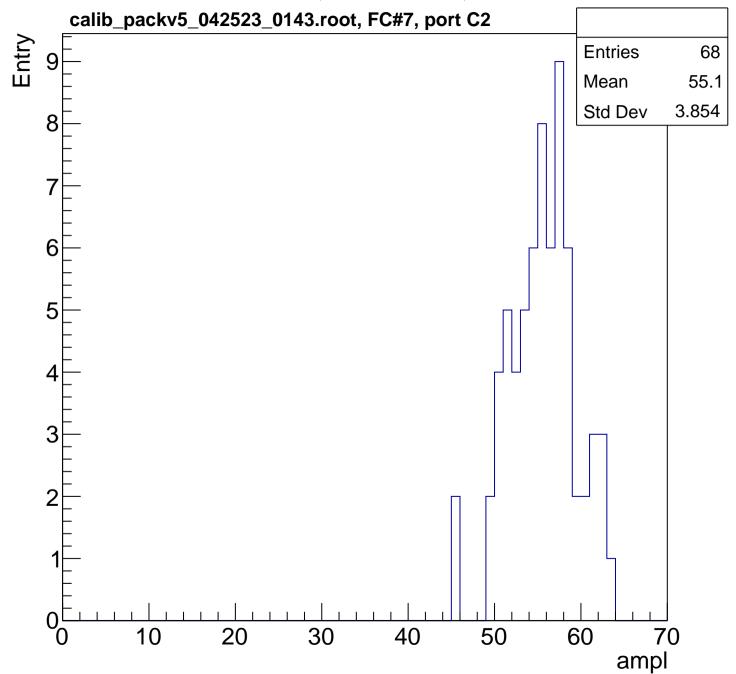


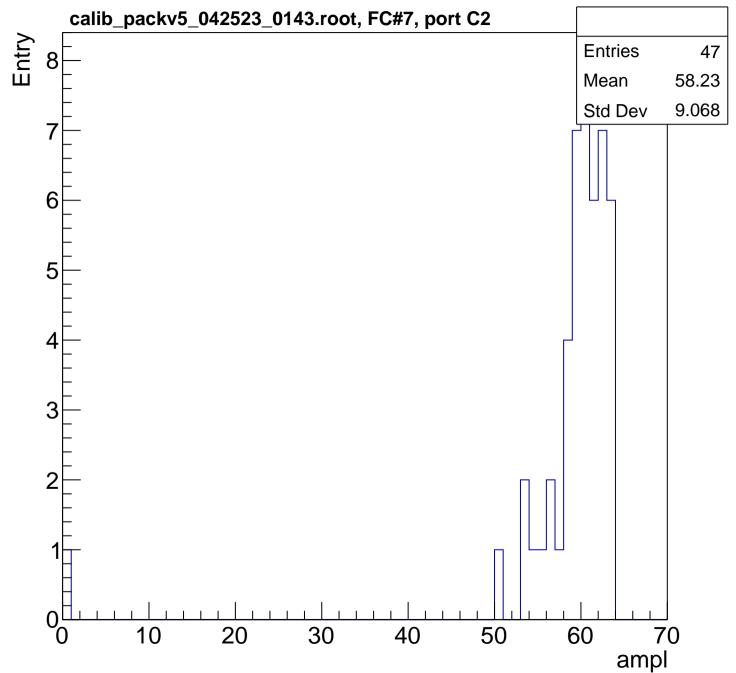


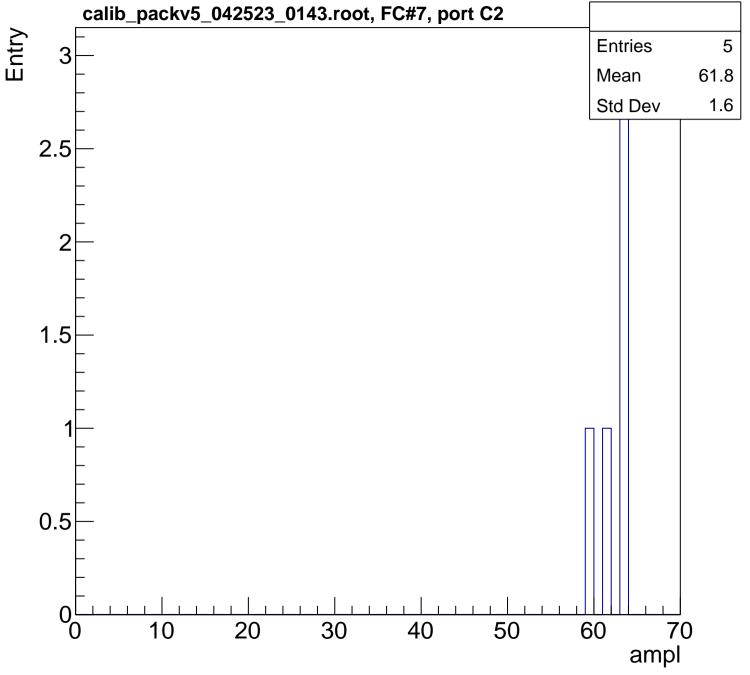


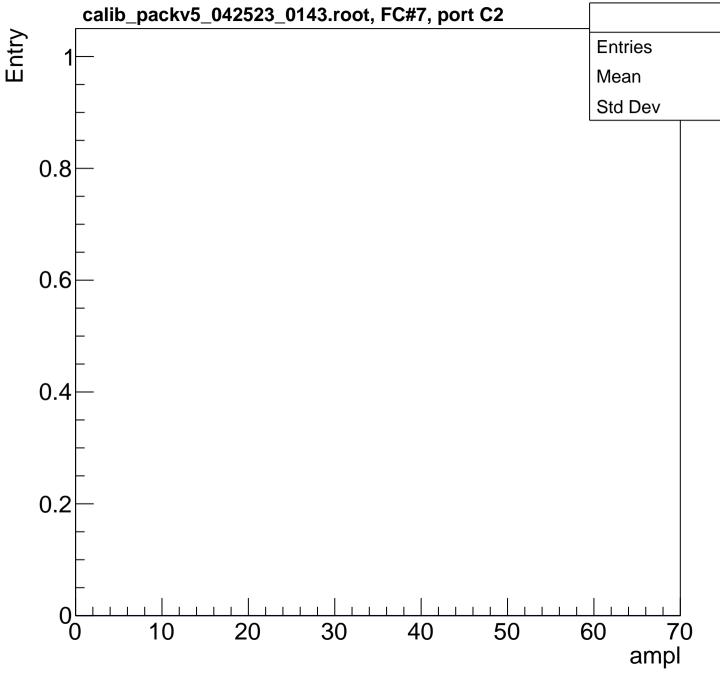


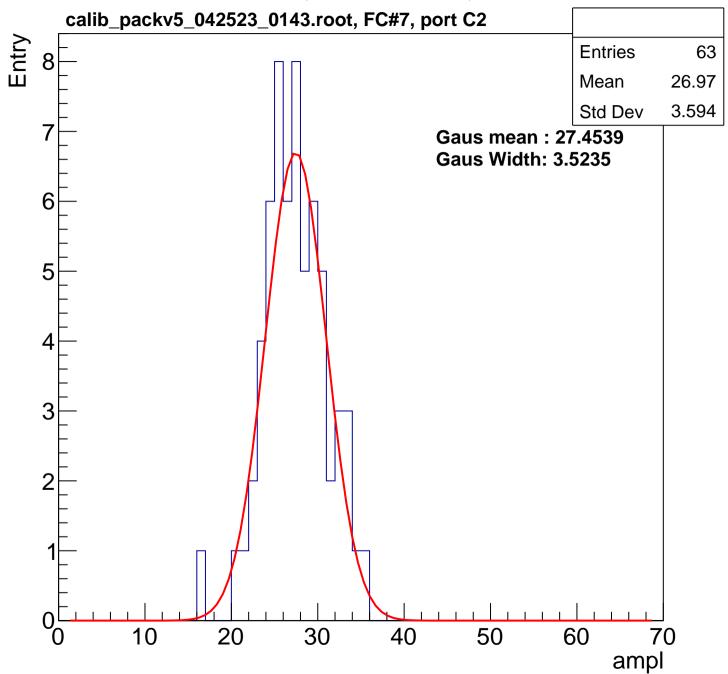


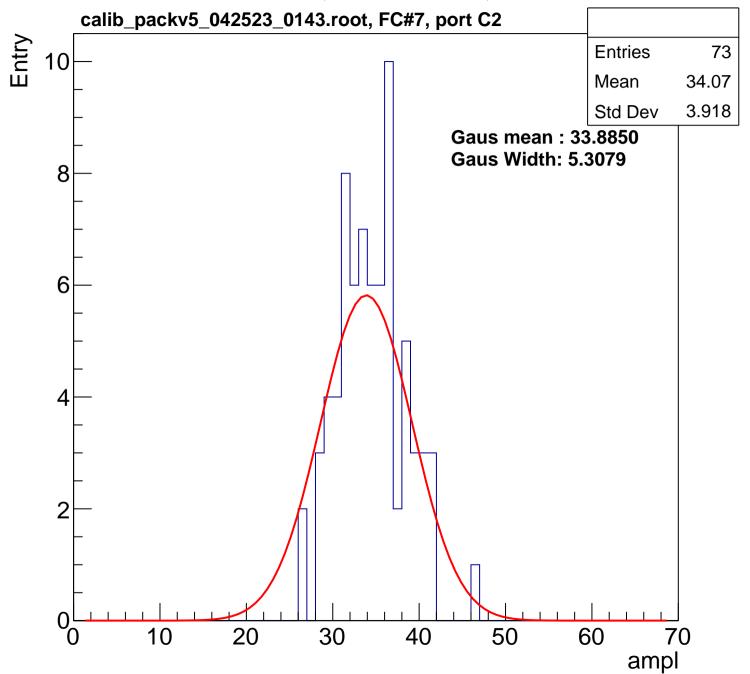


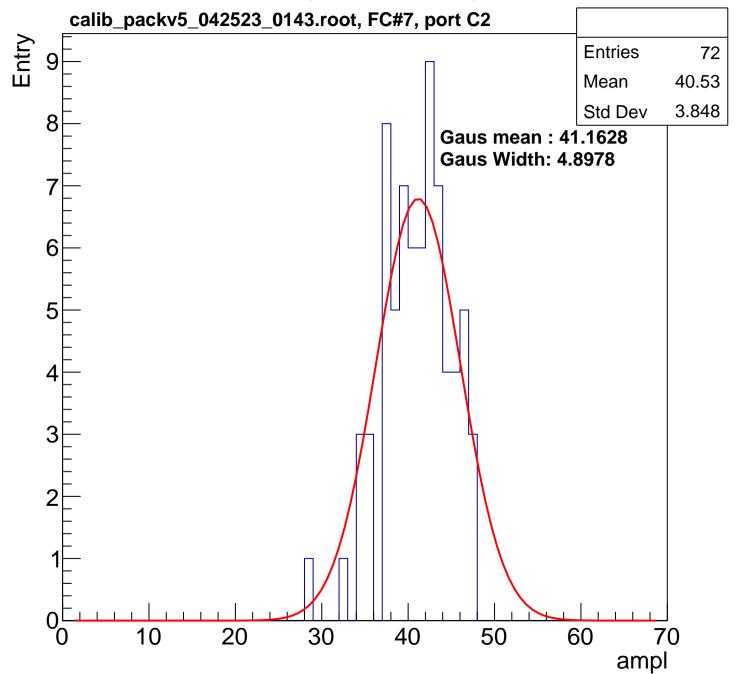


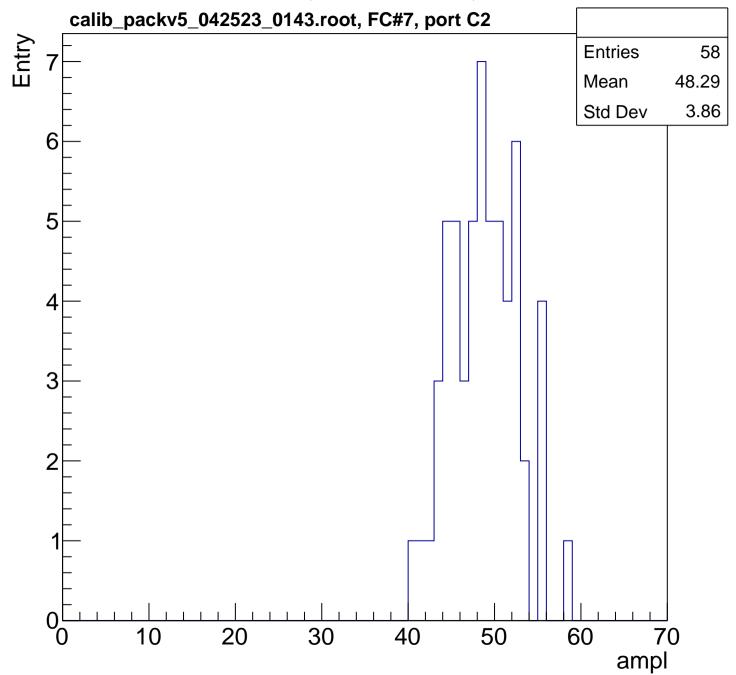


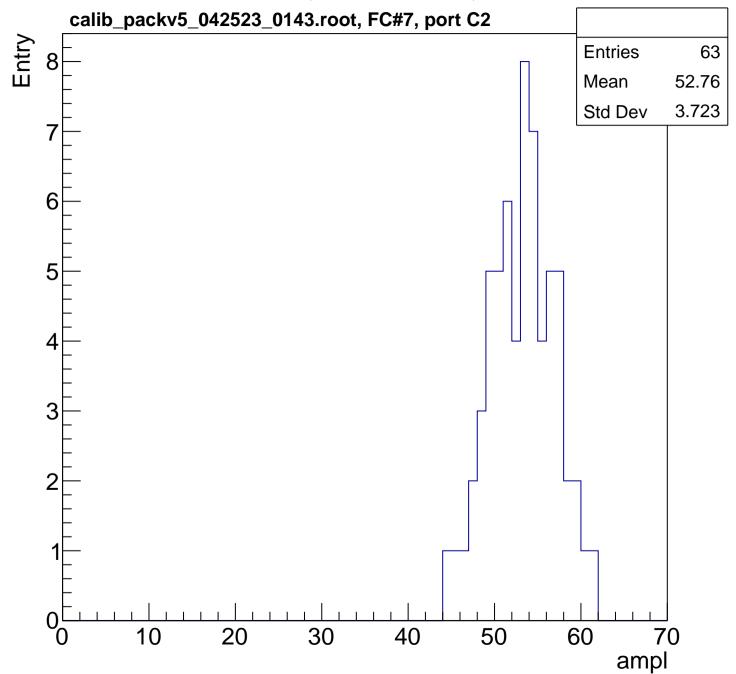


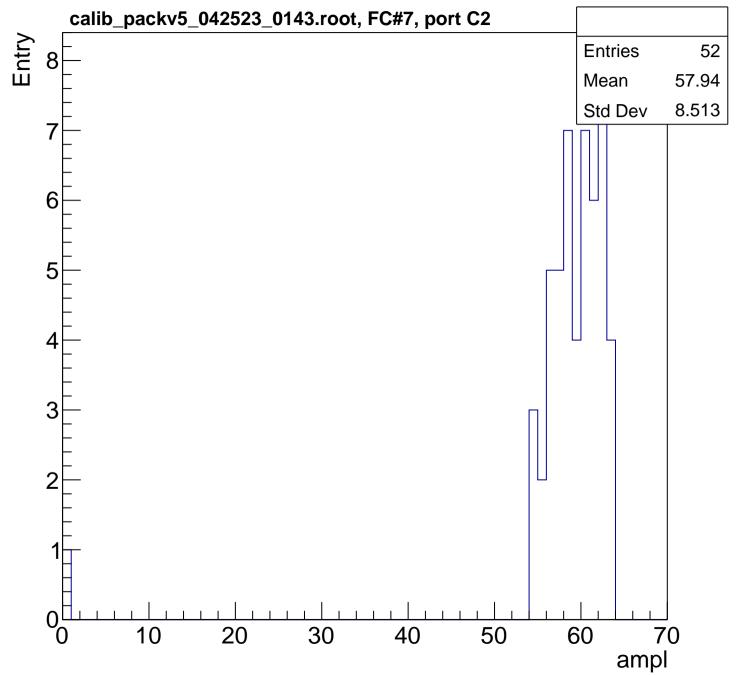


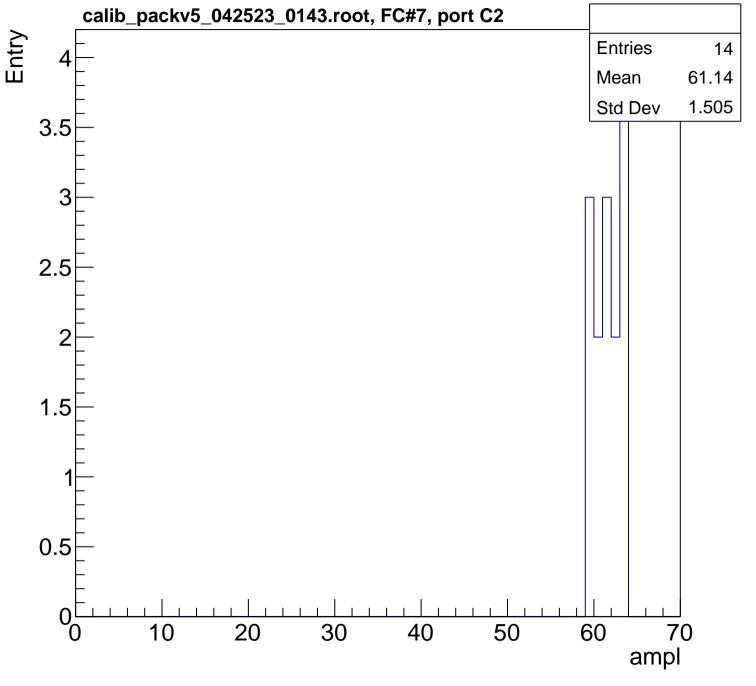


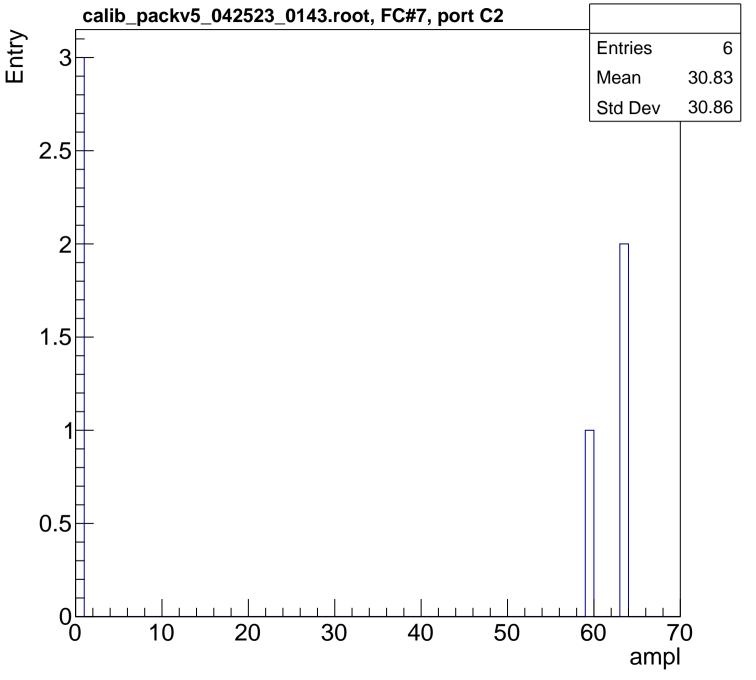


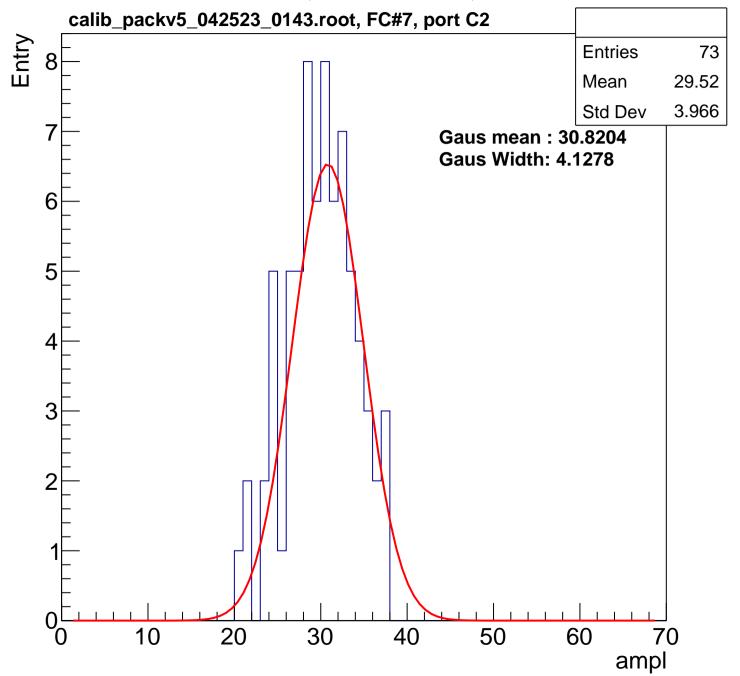


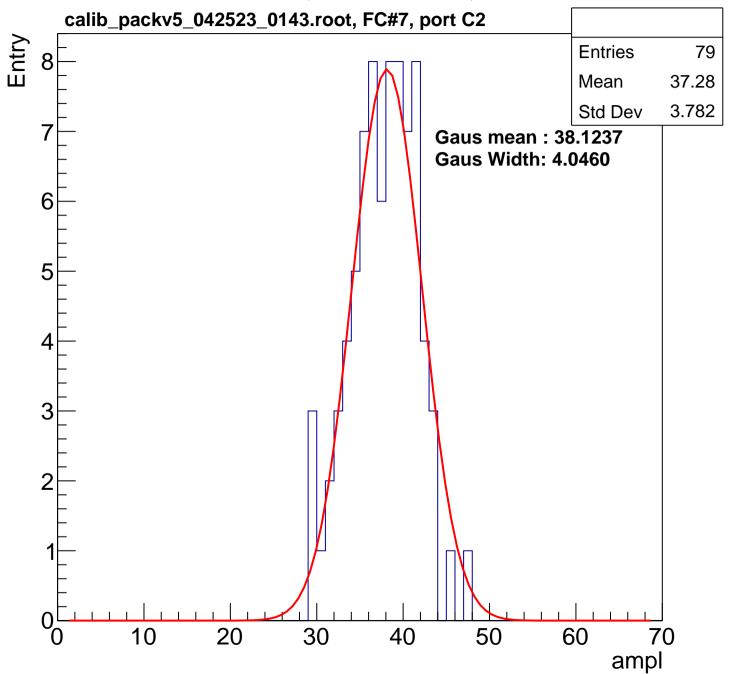


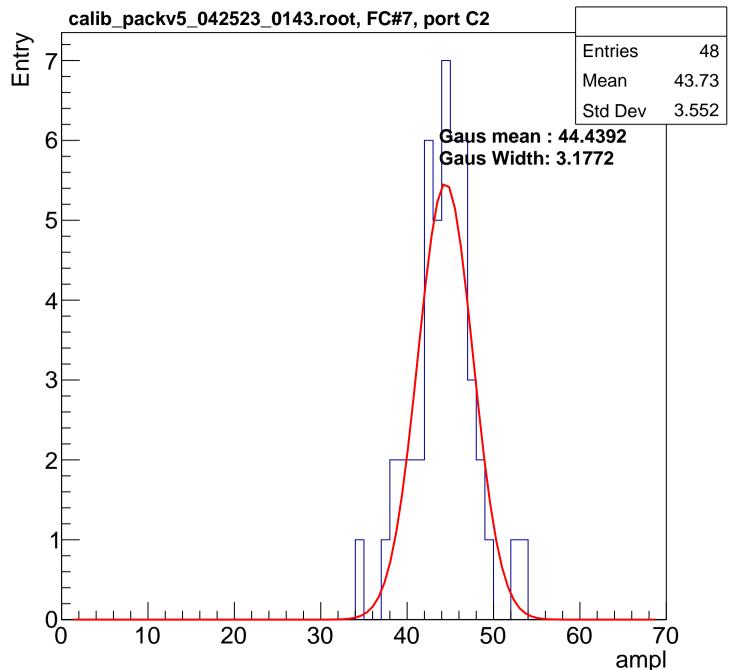


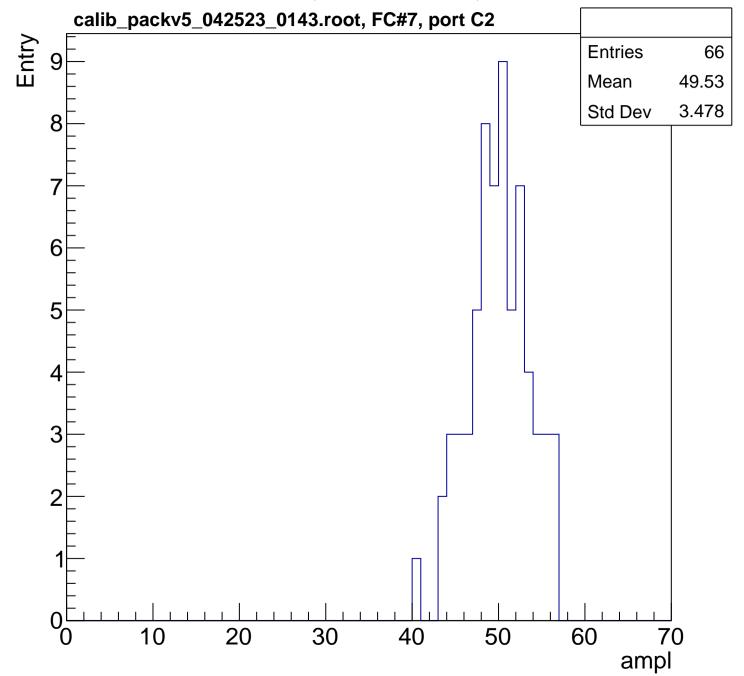


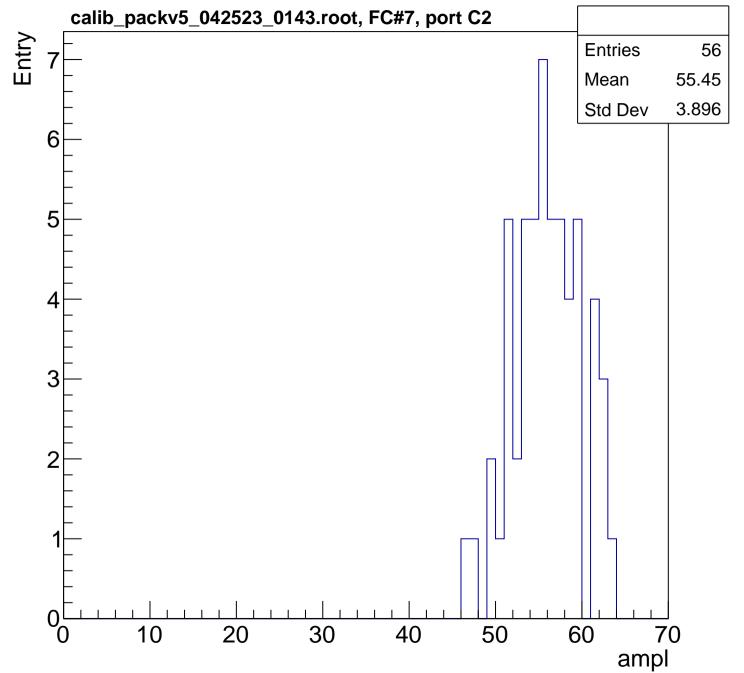


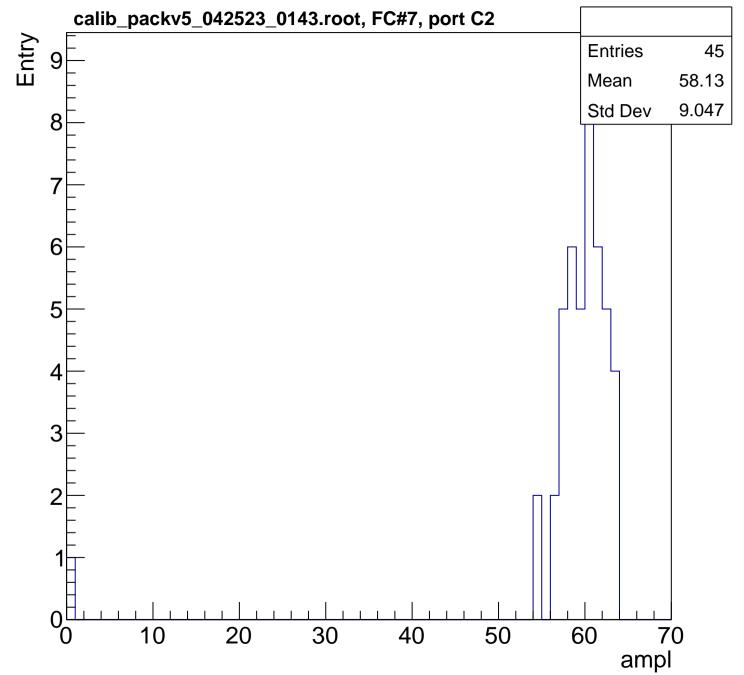


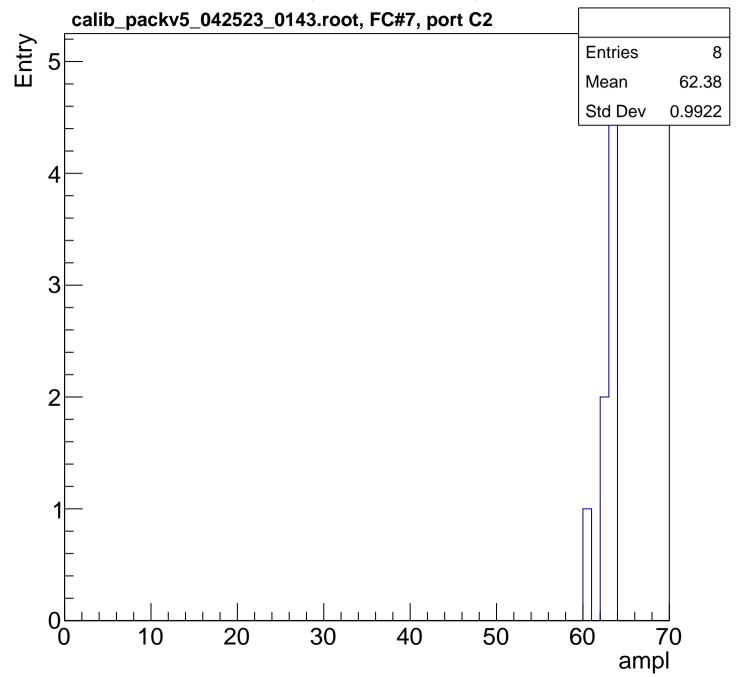


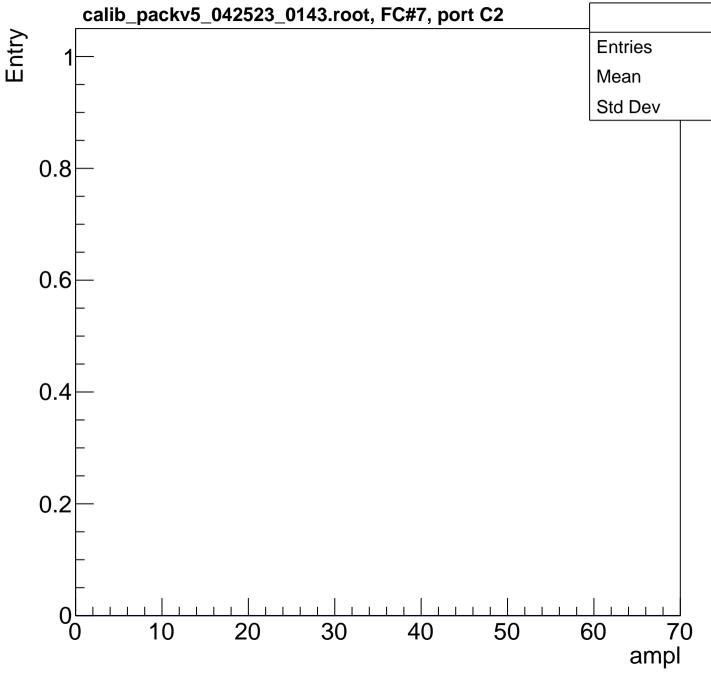


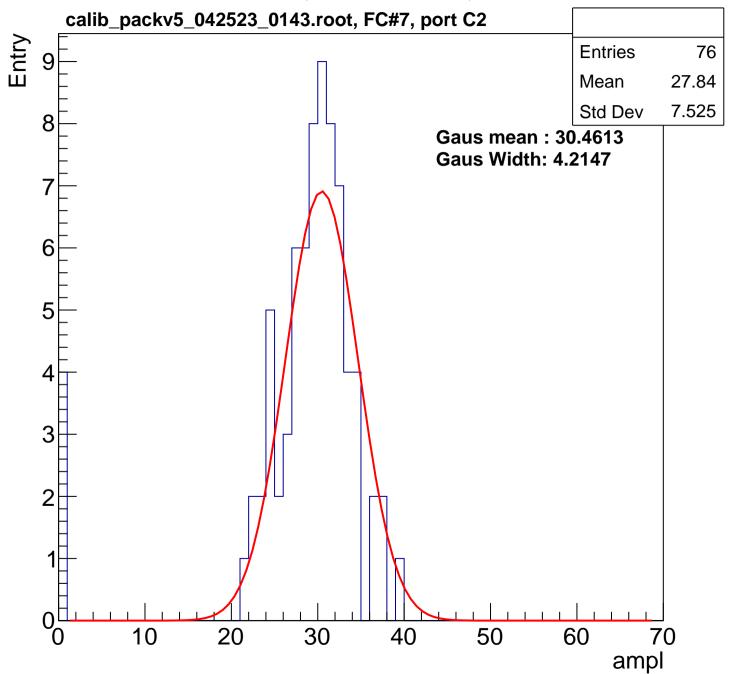


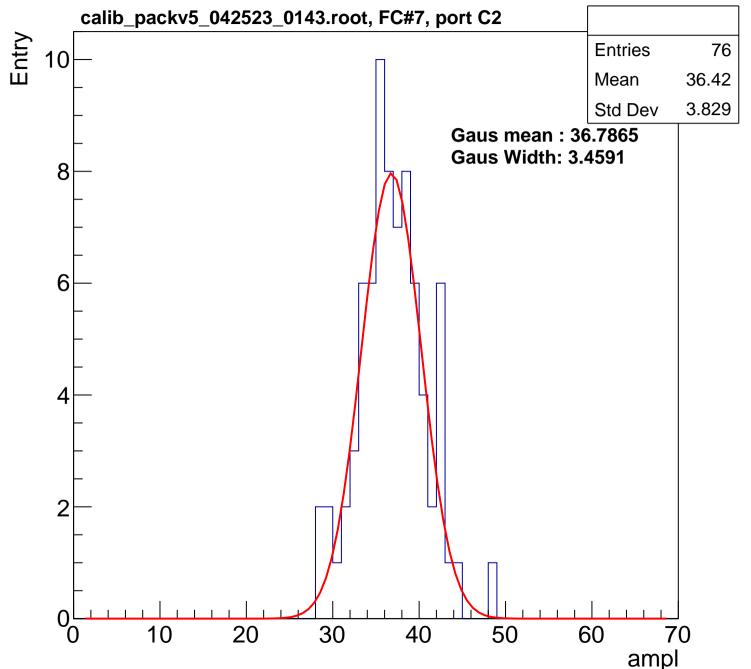


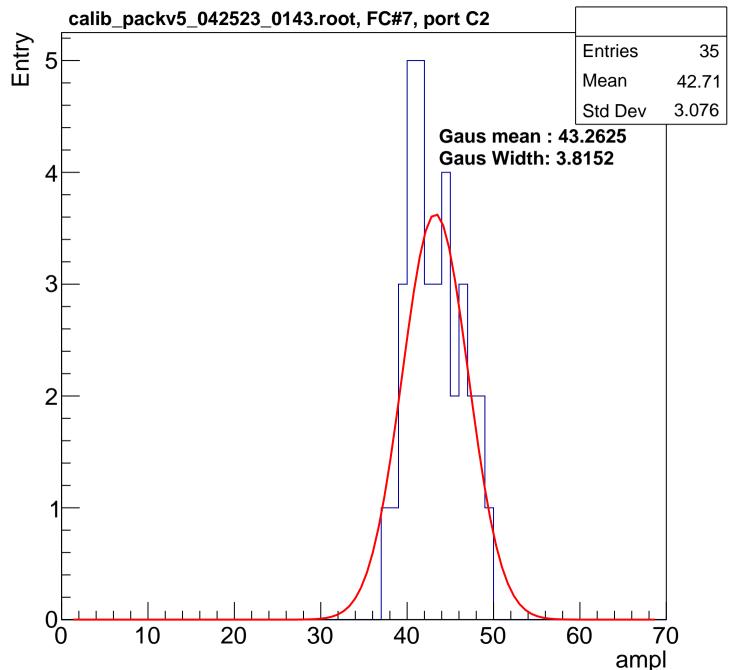


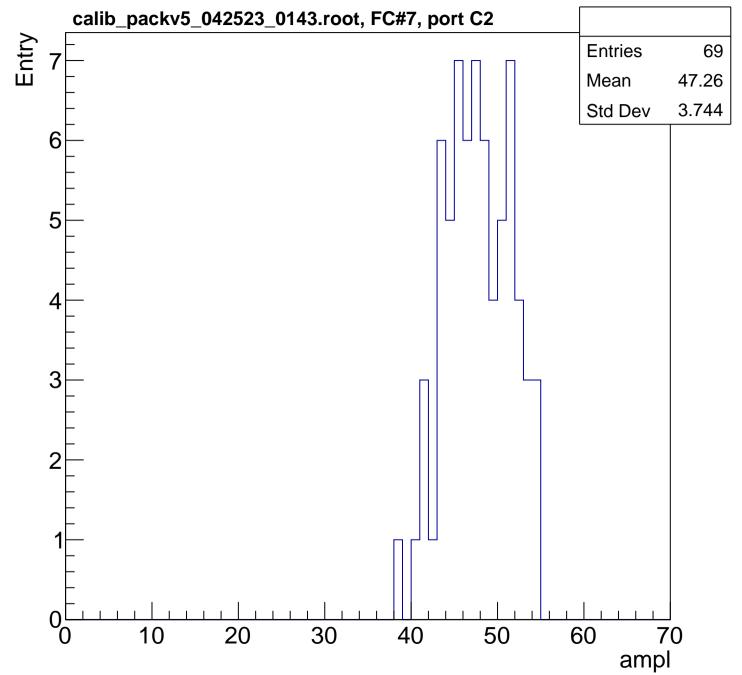


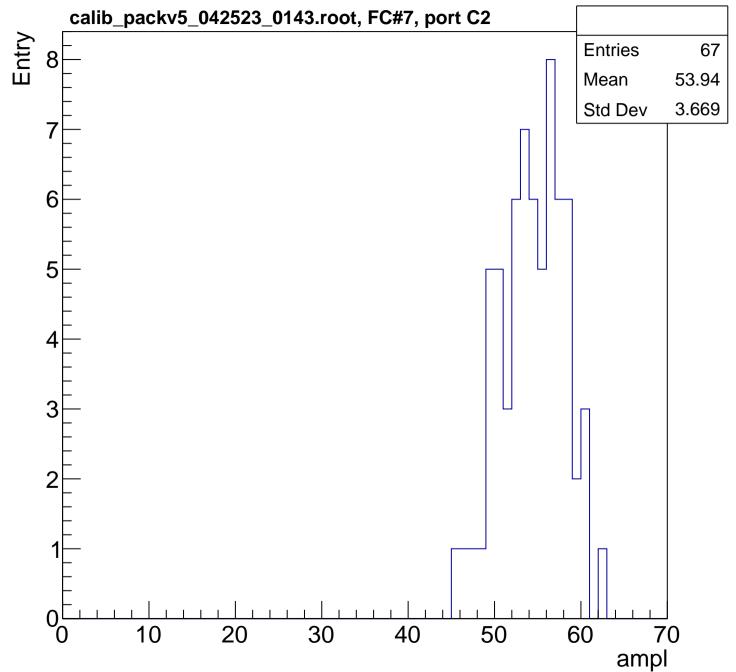


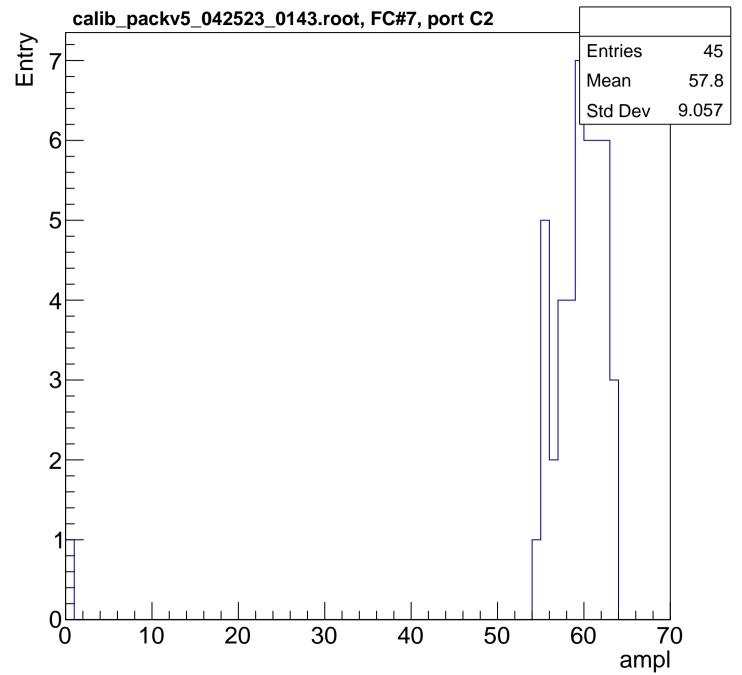


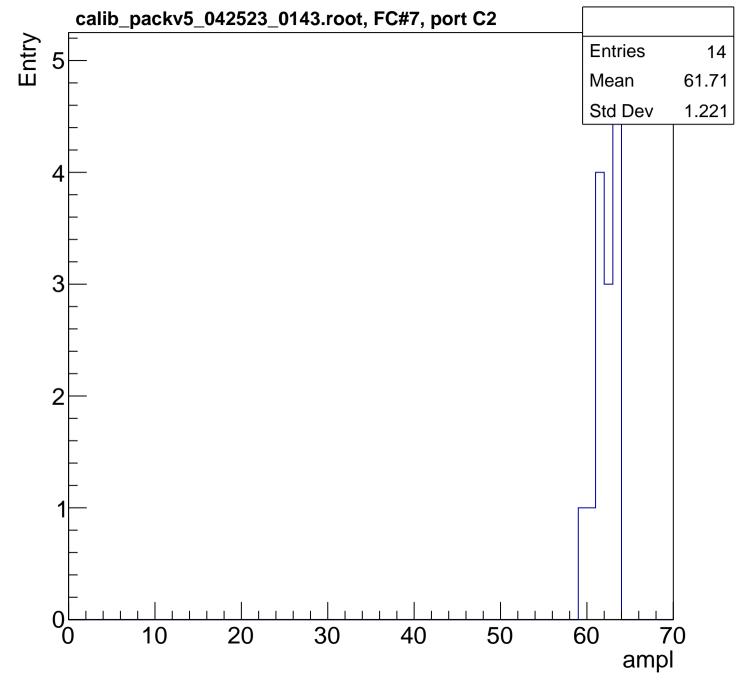


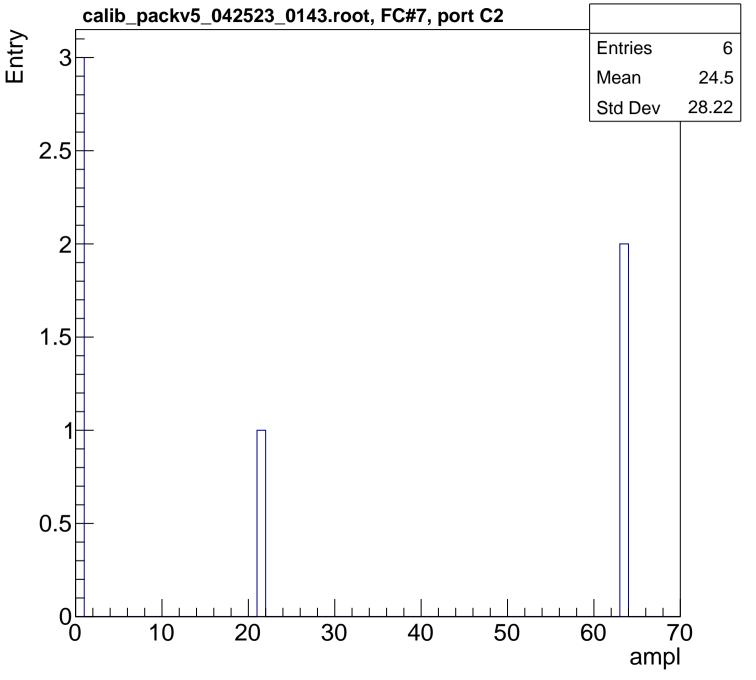


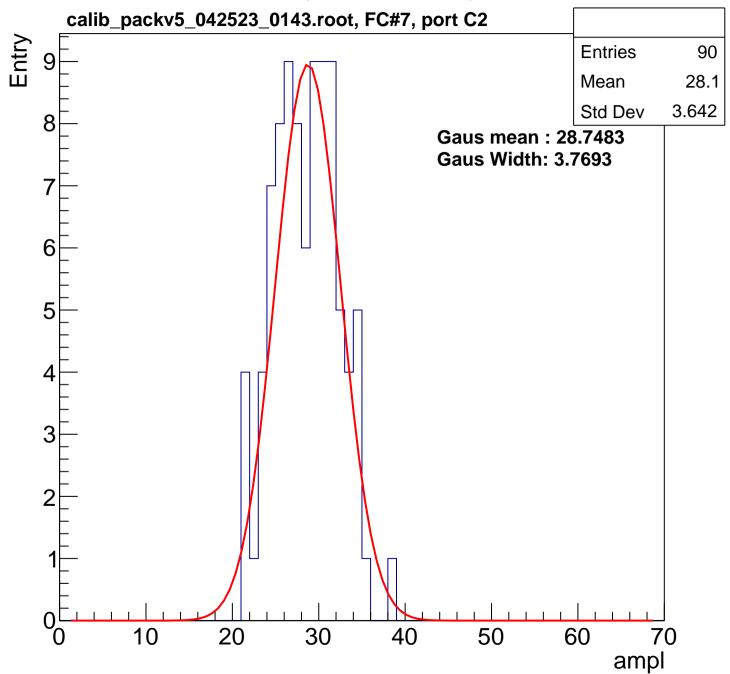


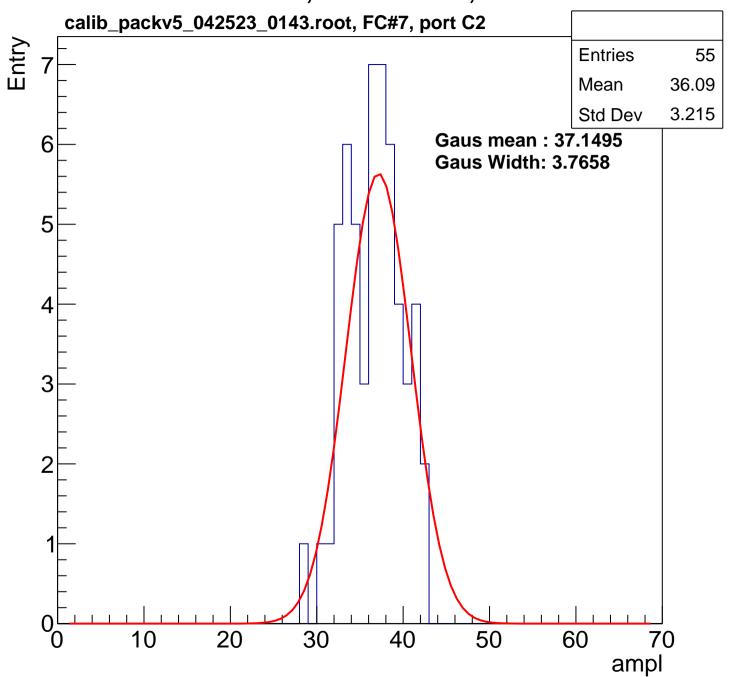


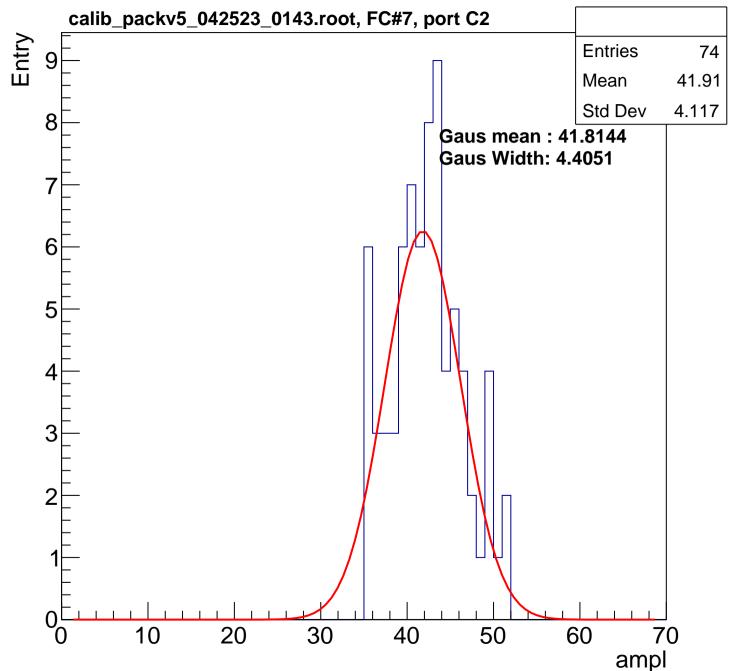


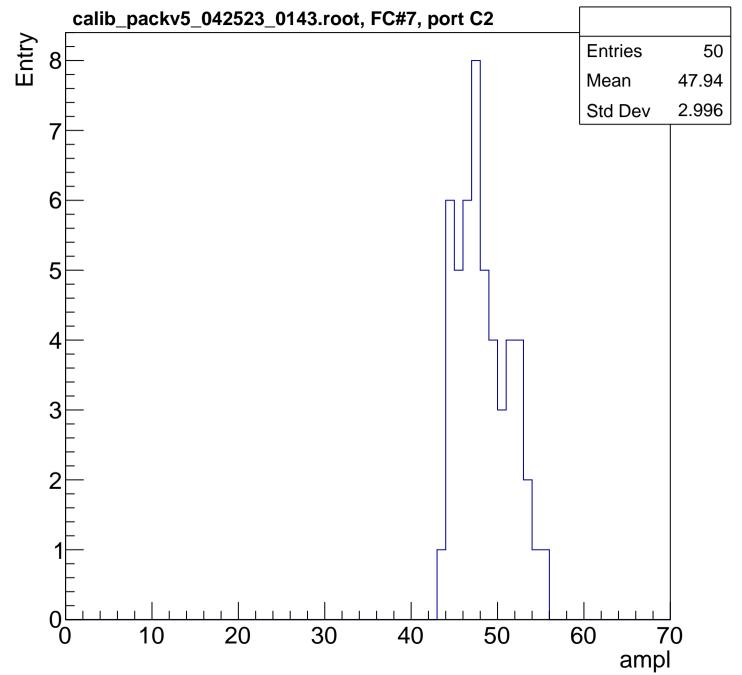


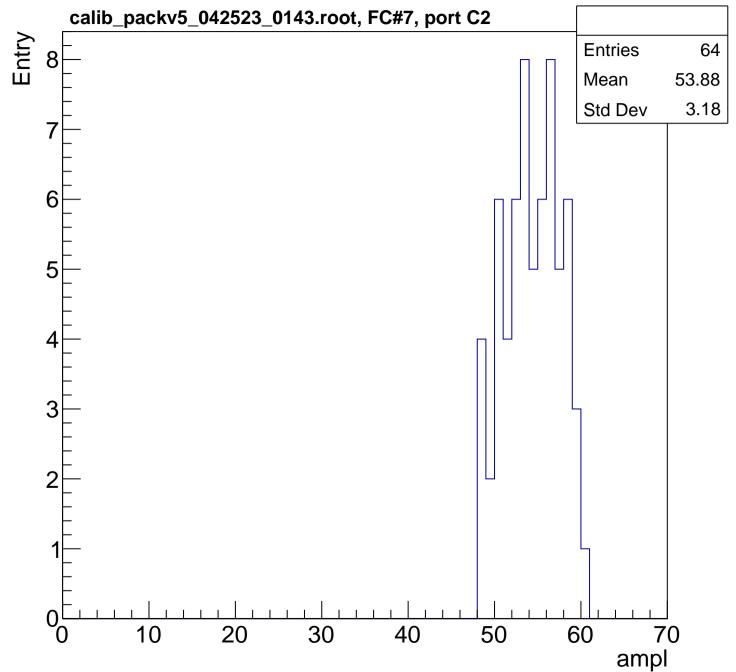


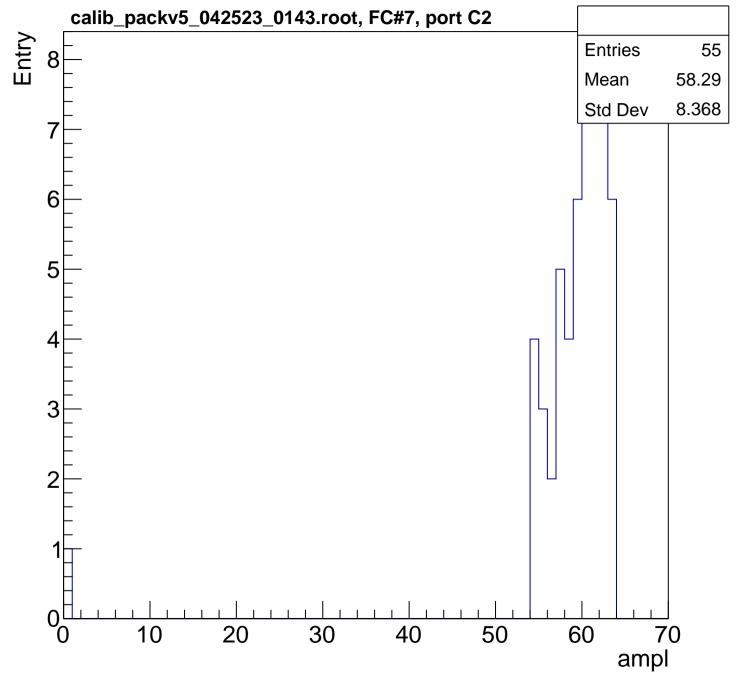


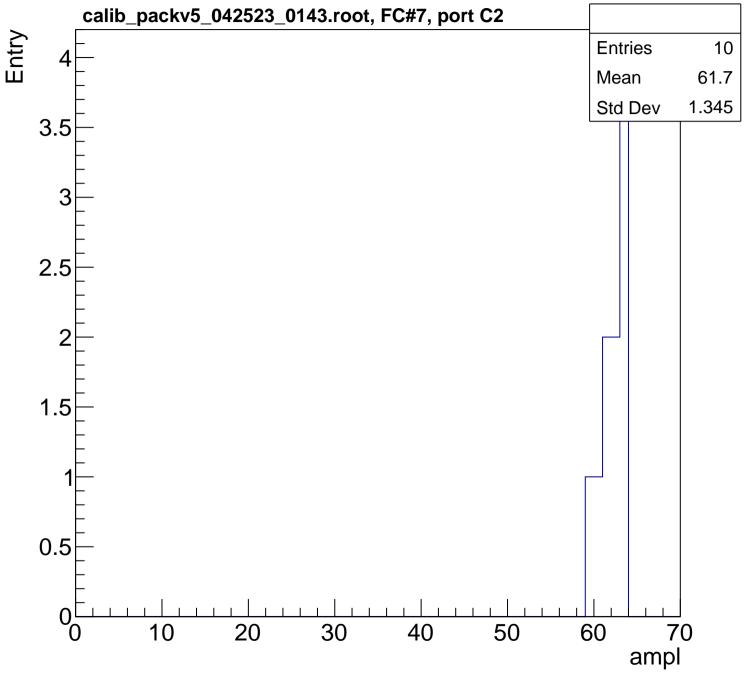


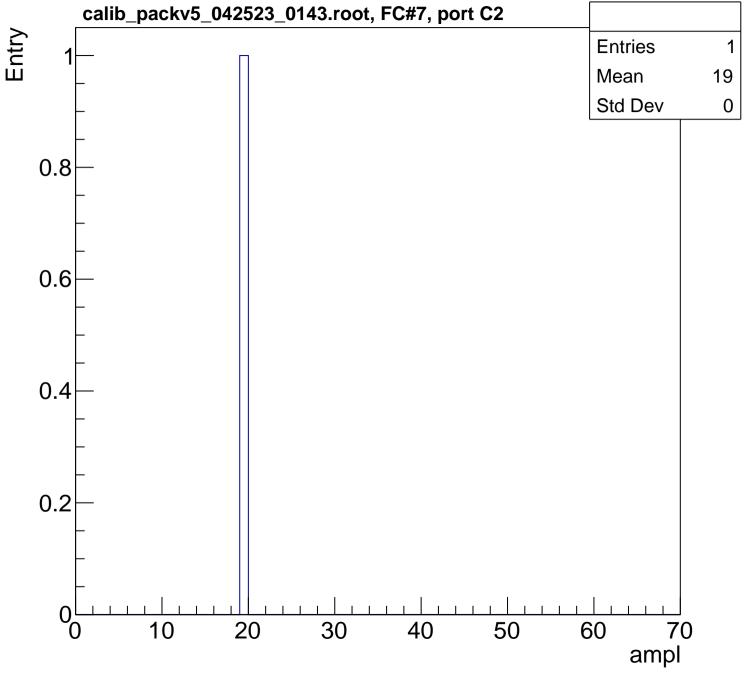


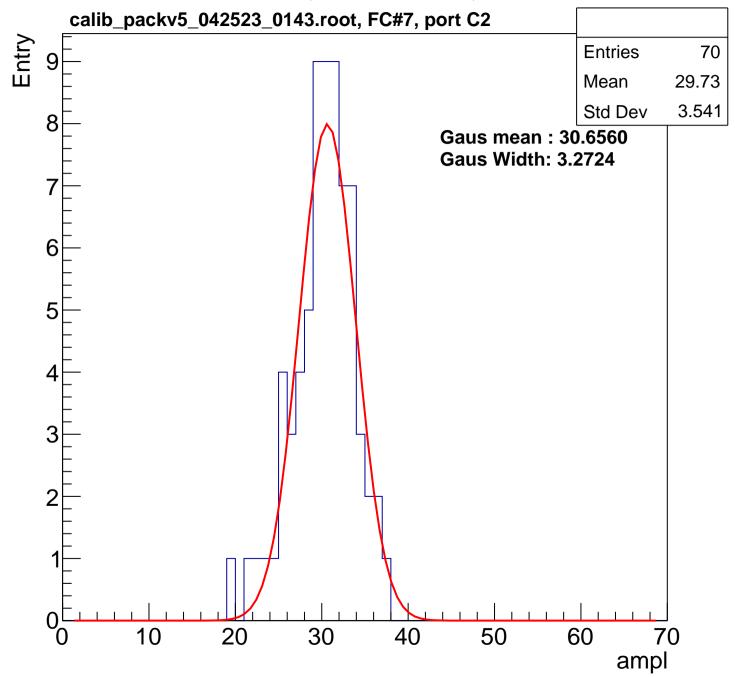


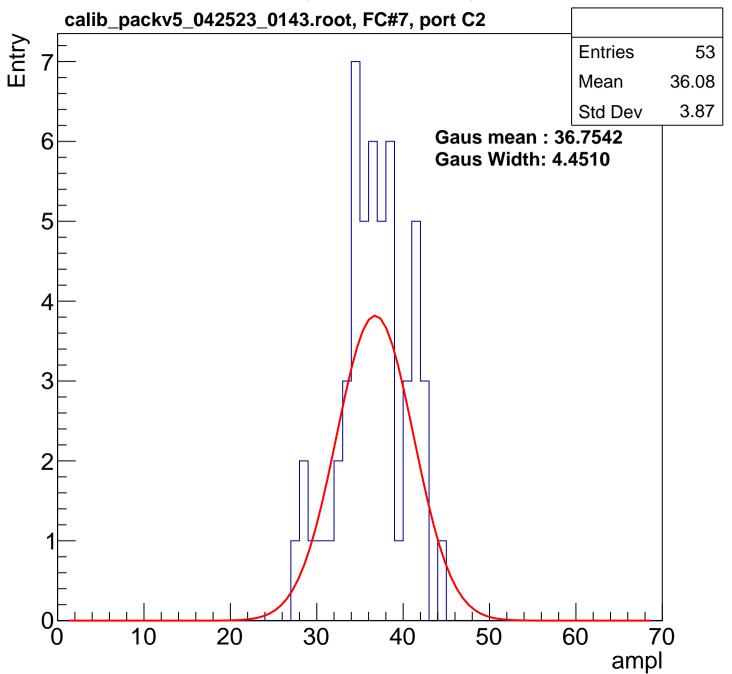


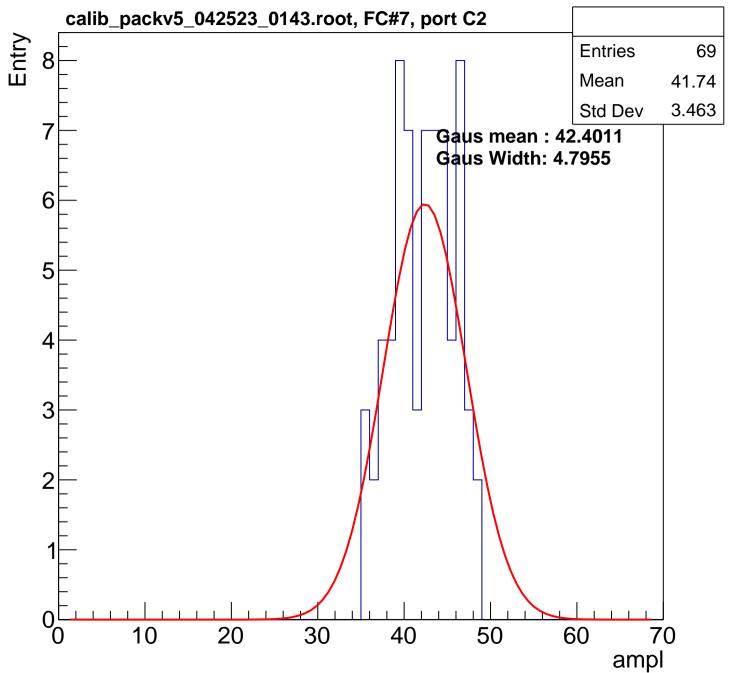


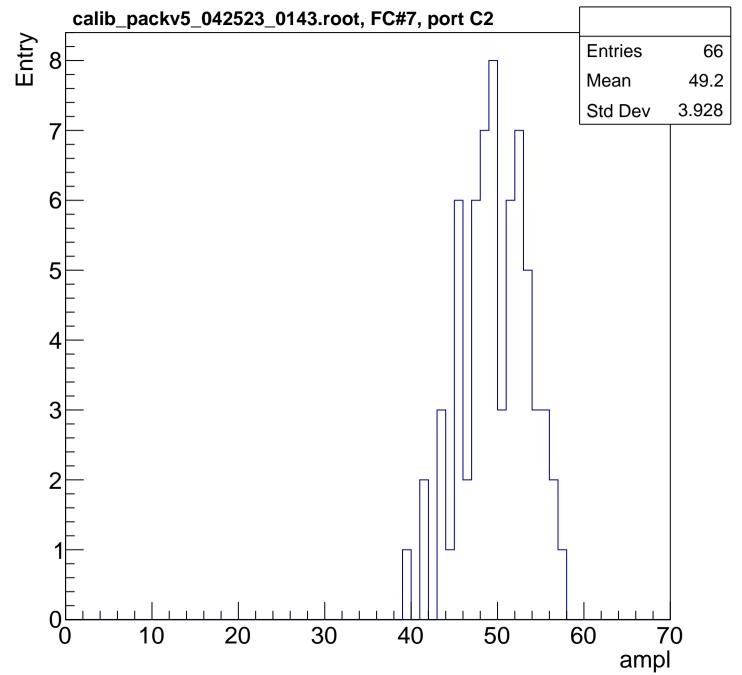


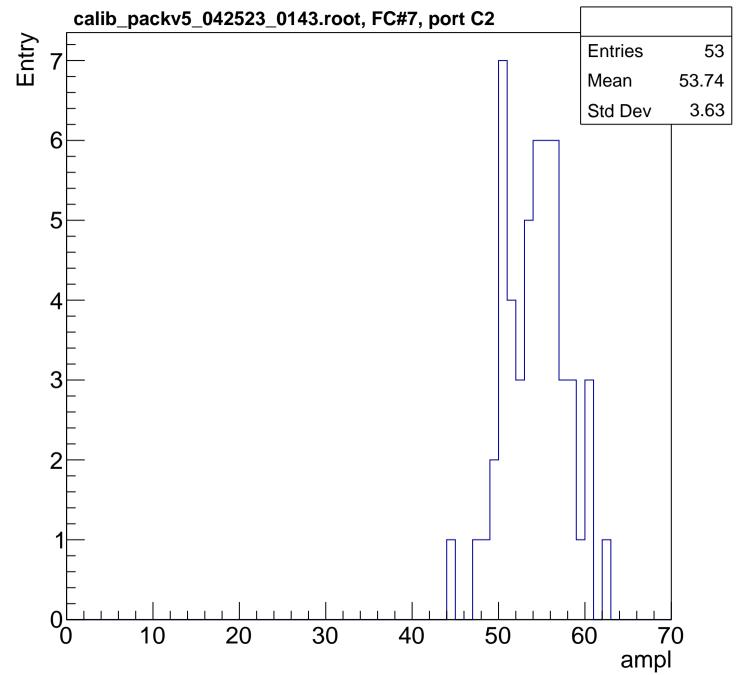


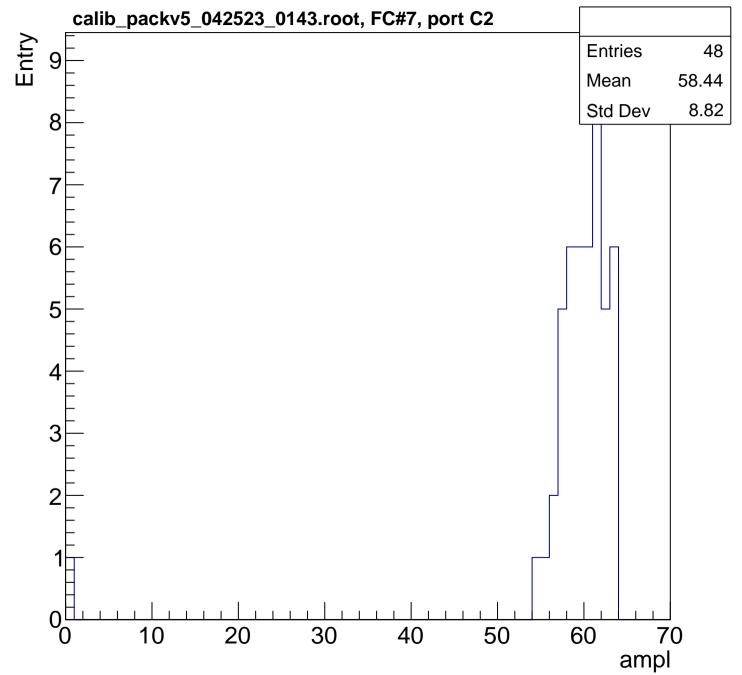


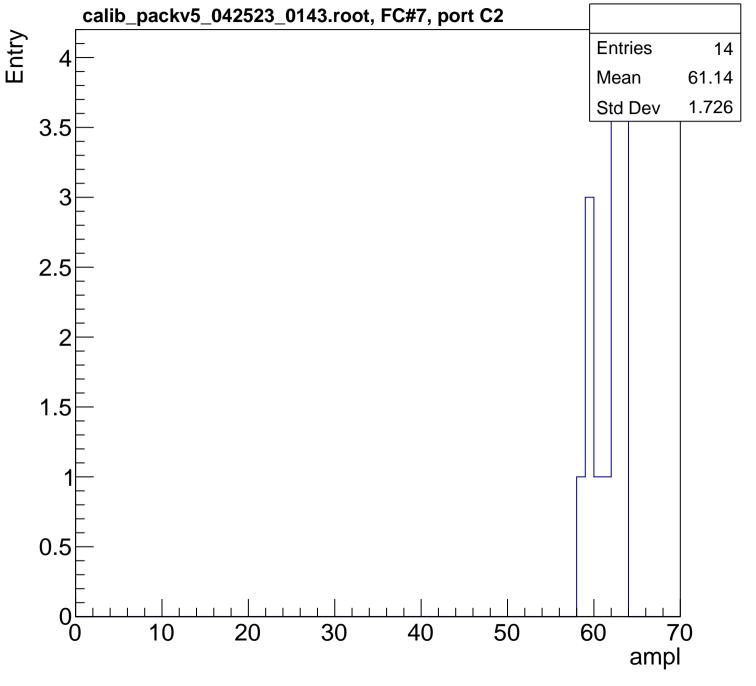


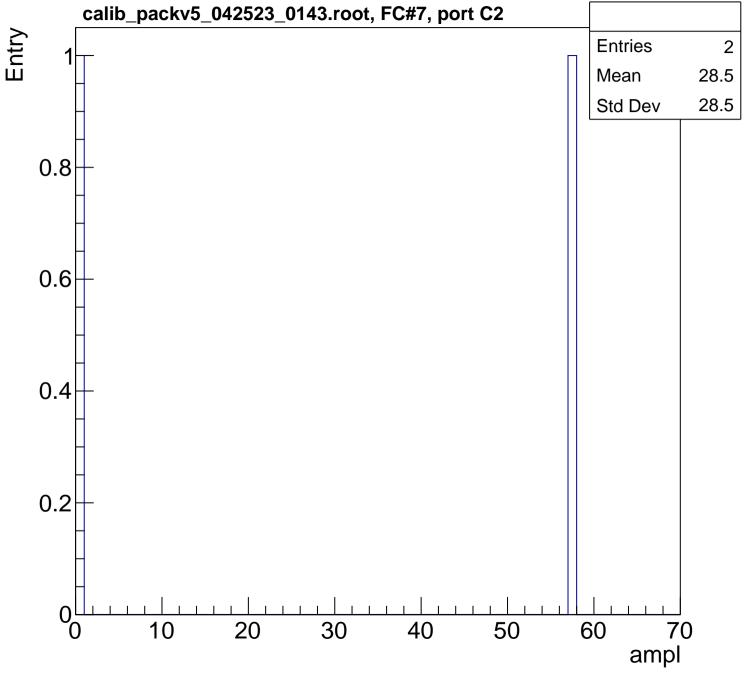


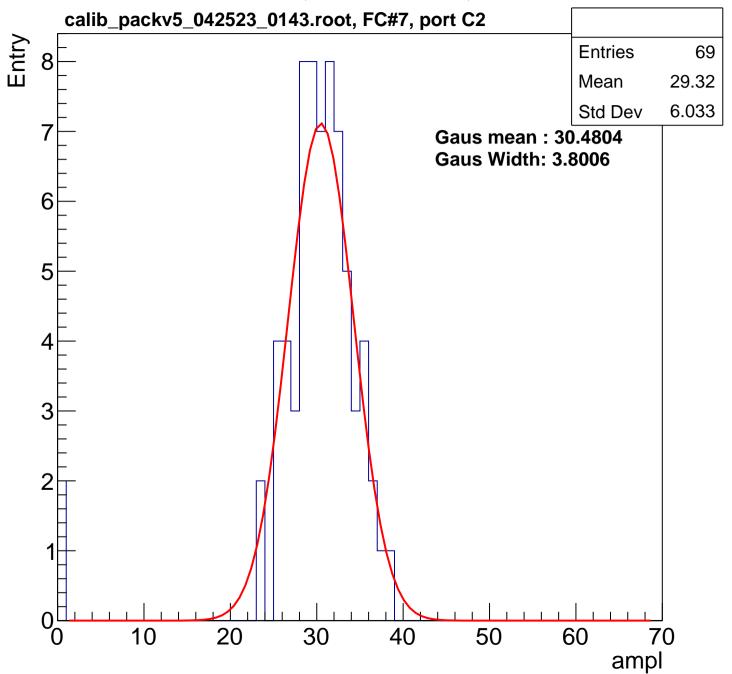


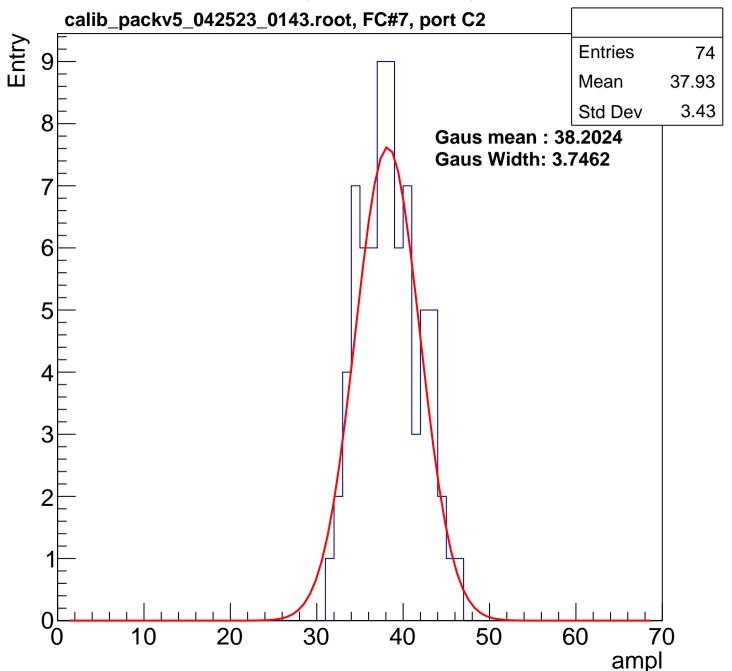


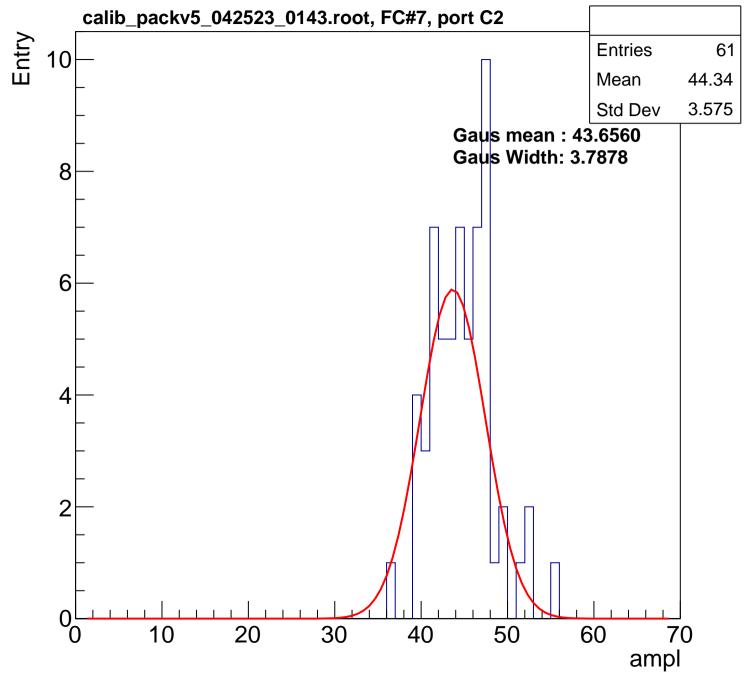


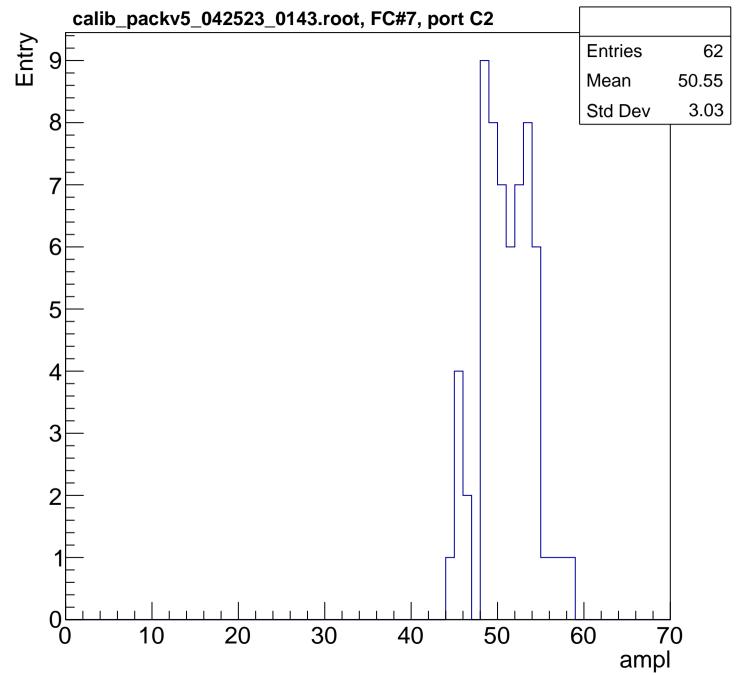


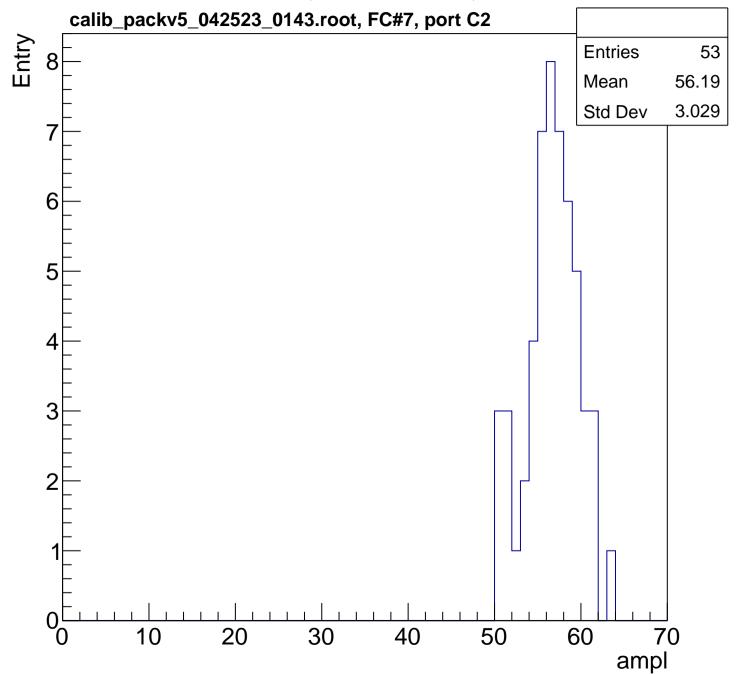


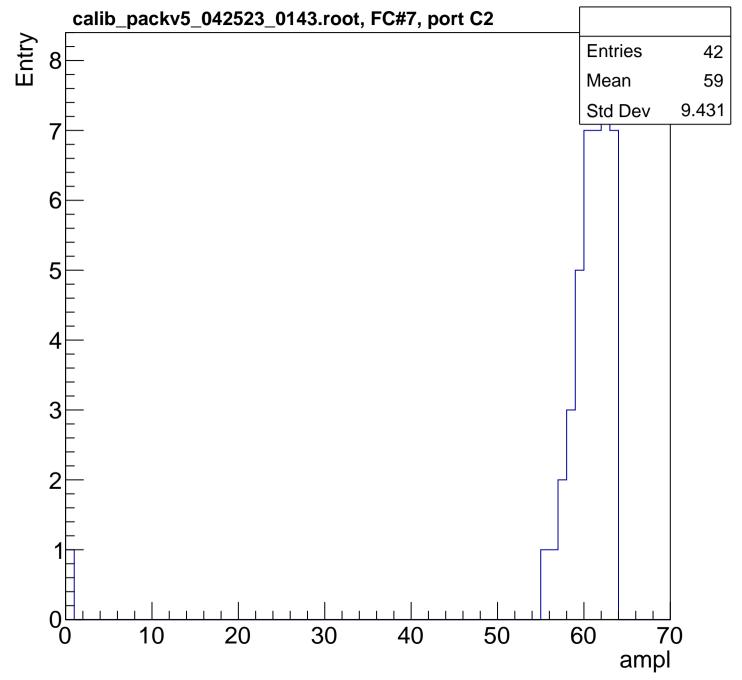


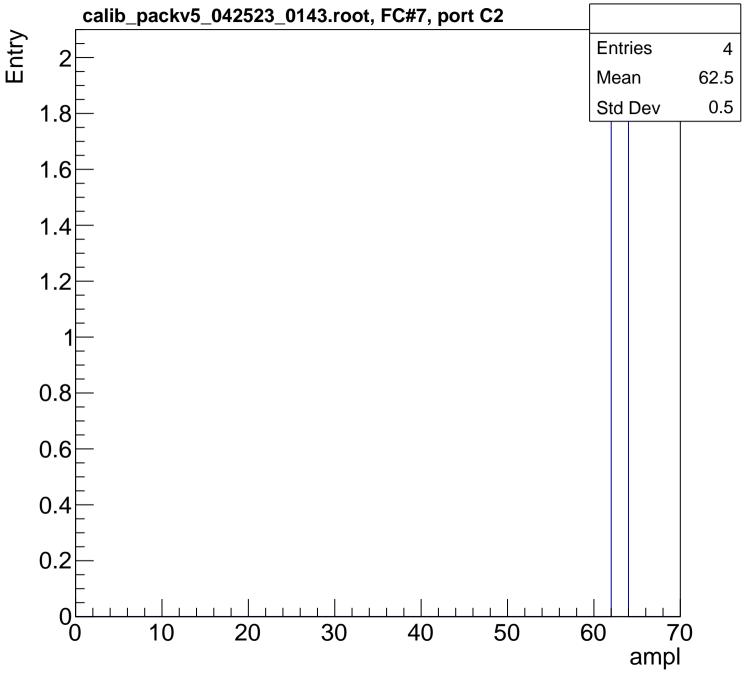


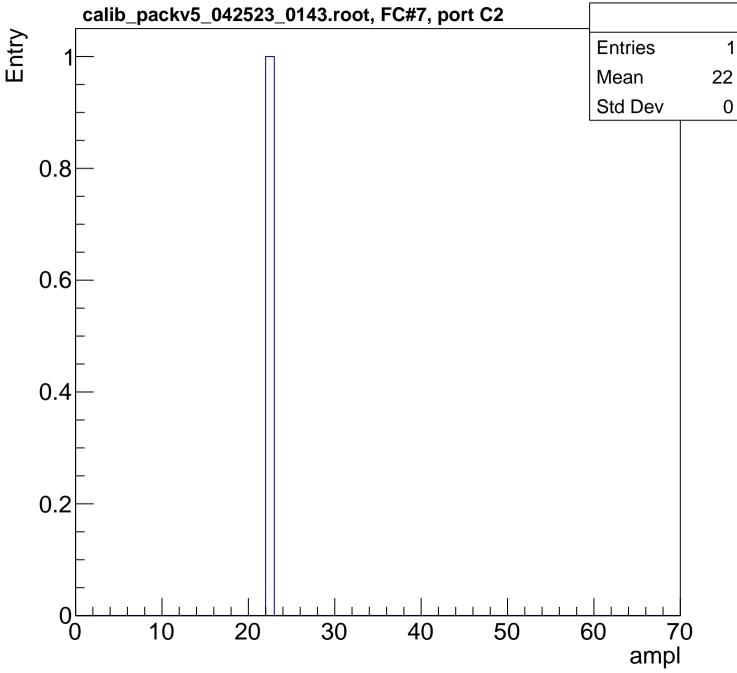


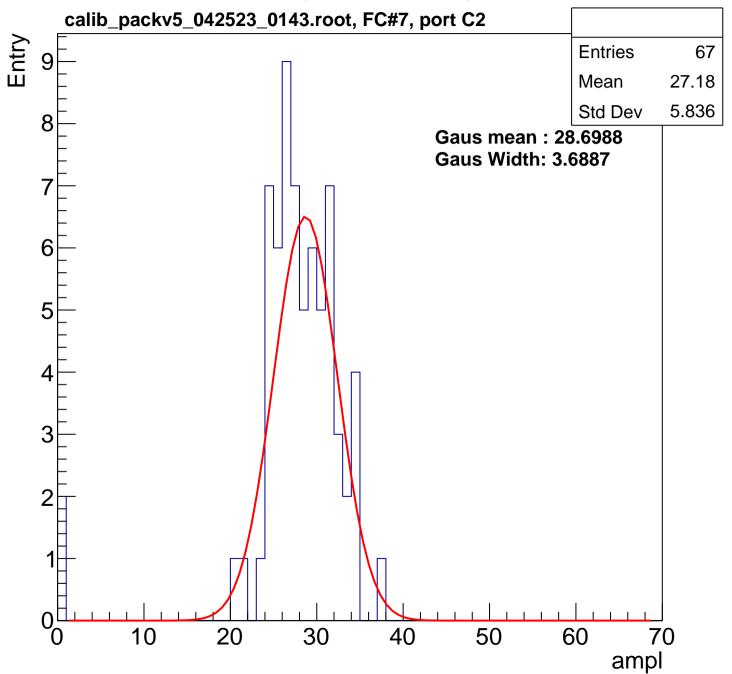


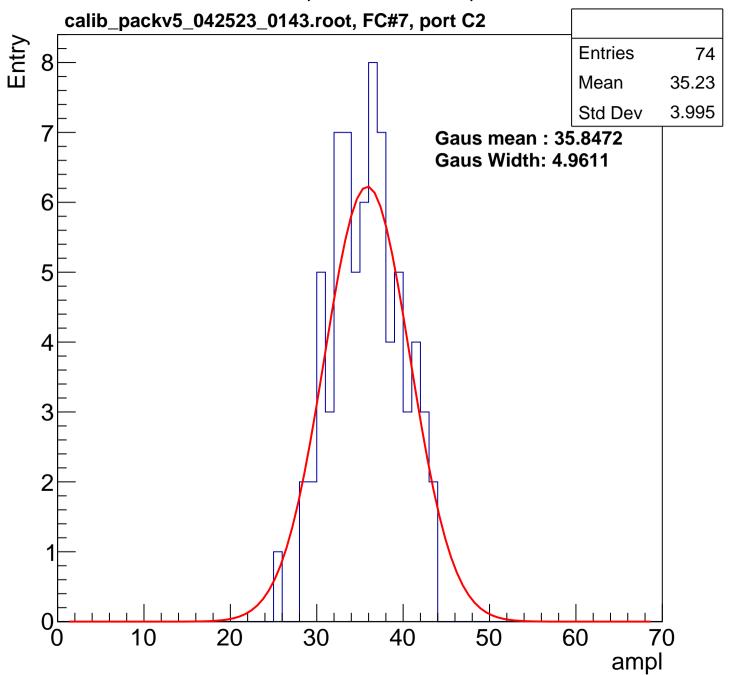


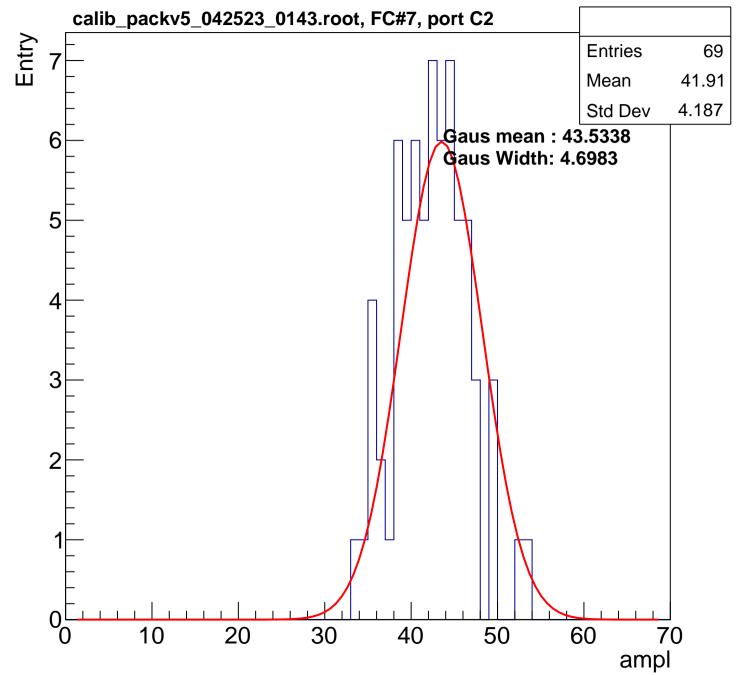




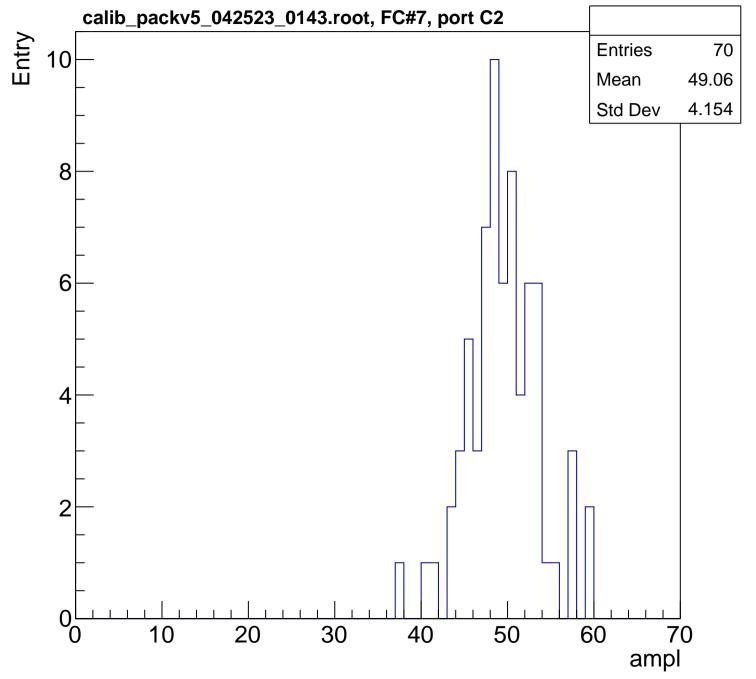


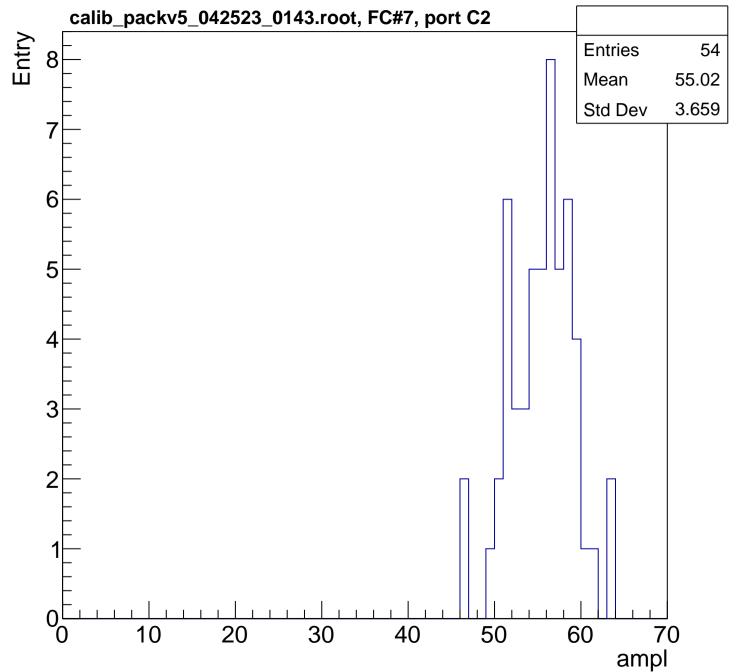


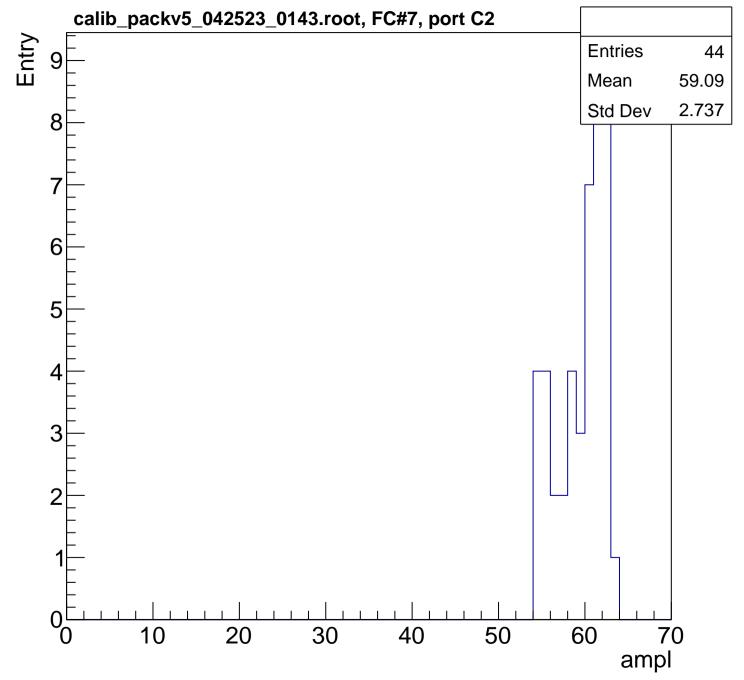


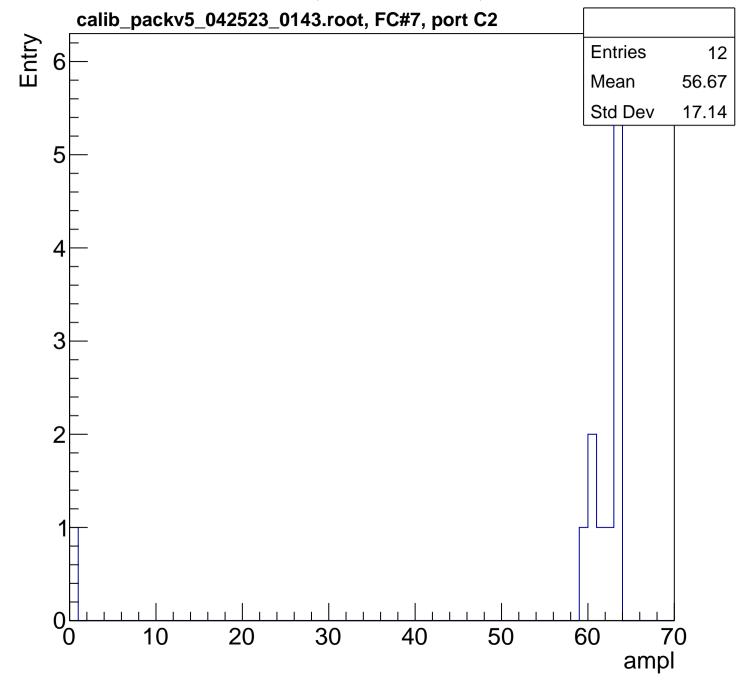


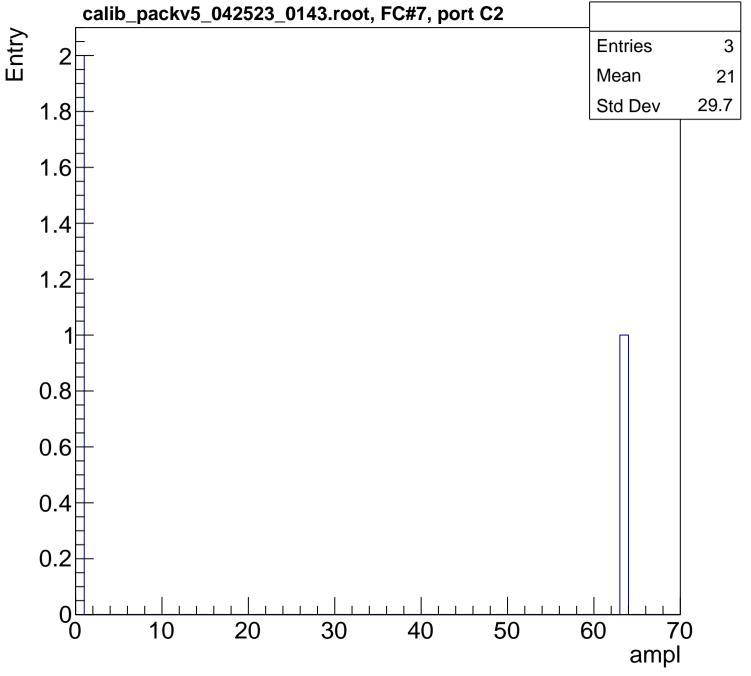
B1L103S, U4-ch106, adc3

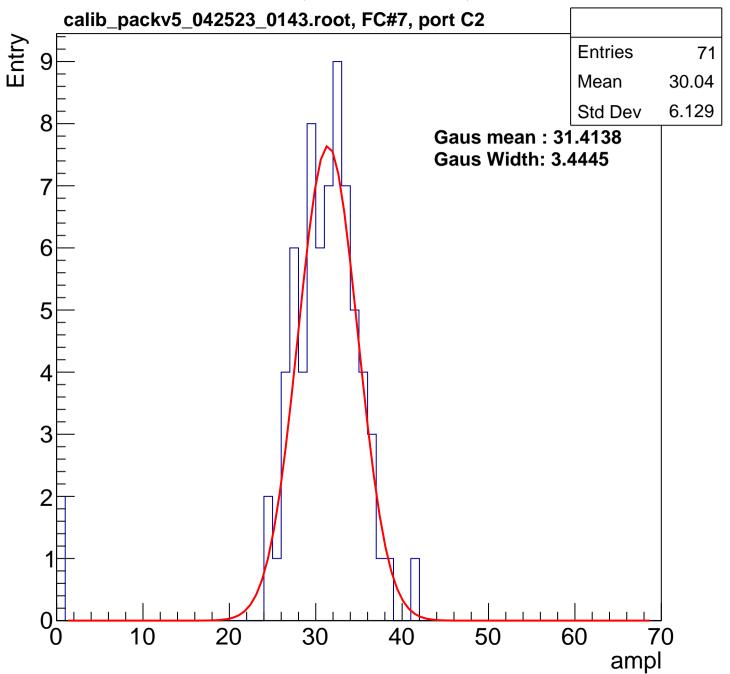


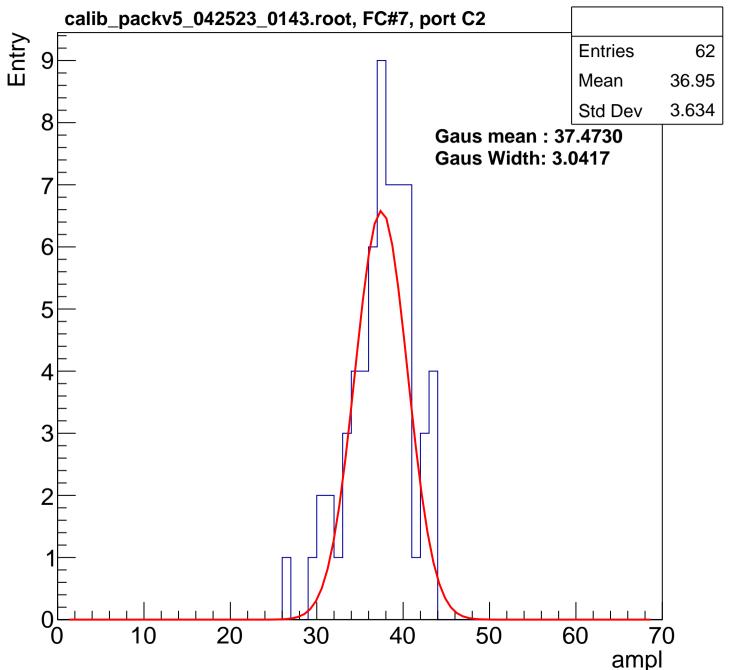


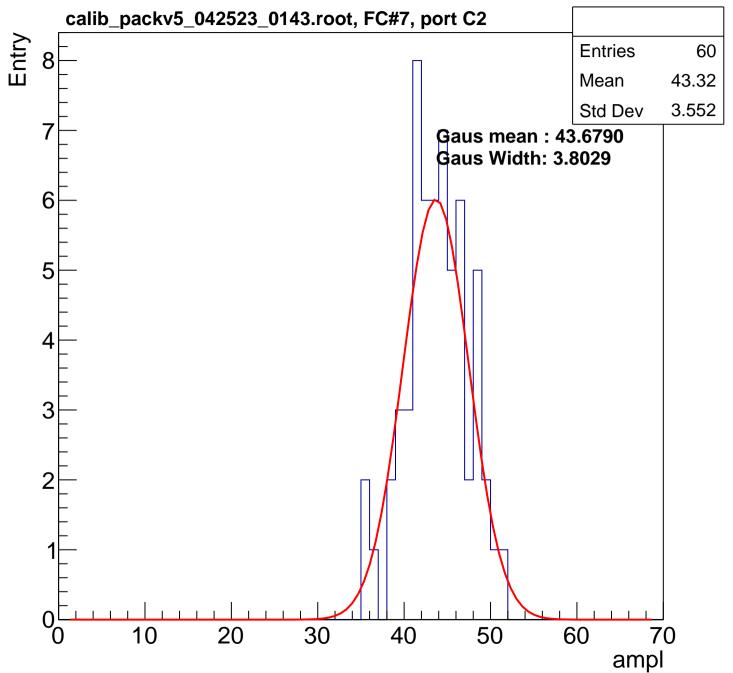


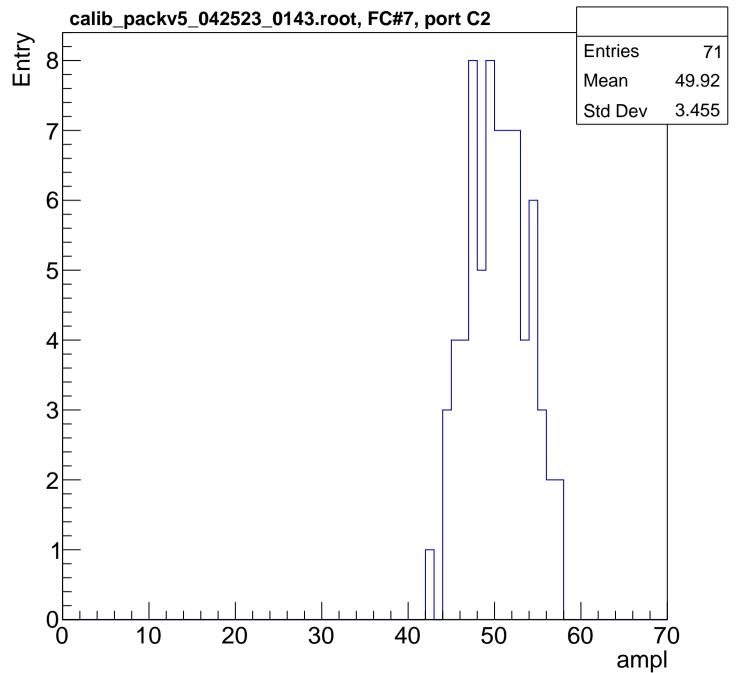


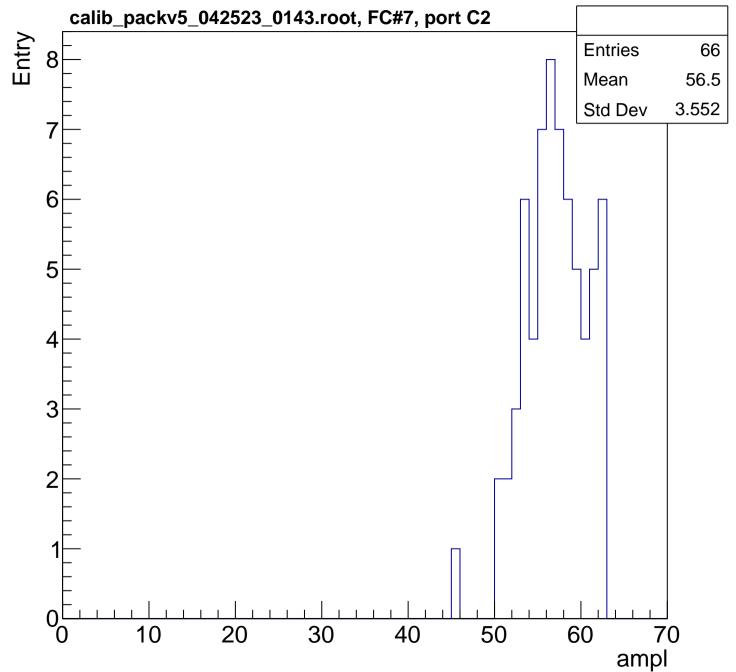


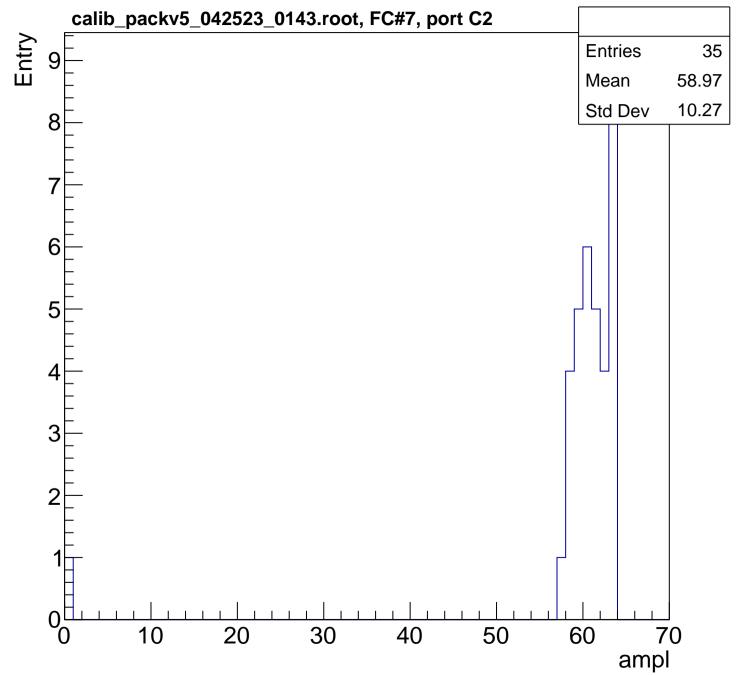


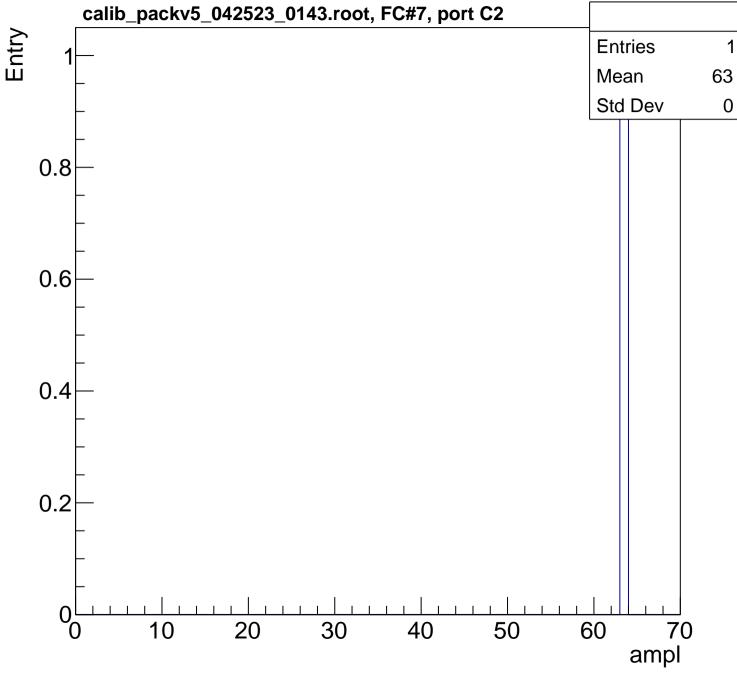


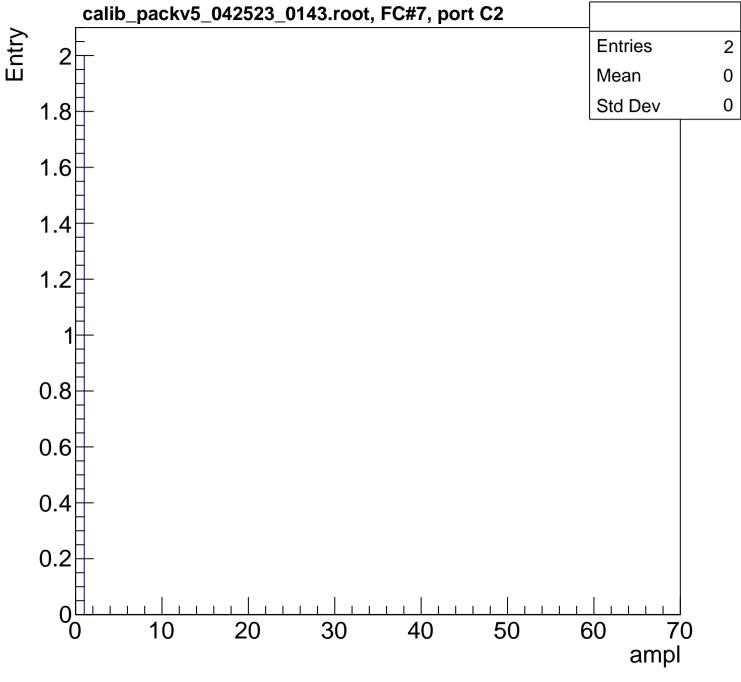


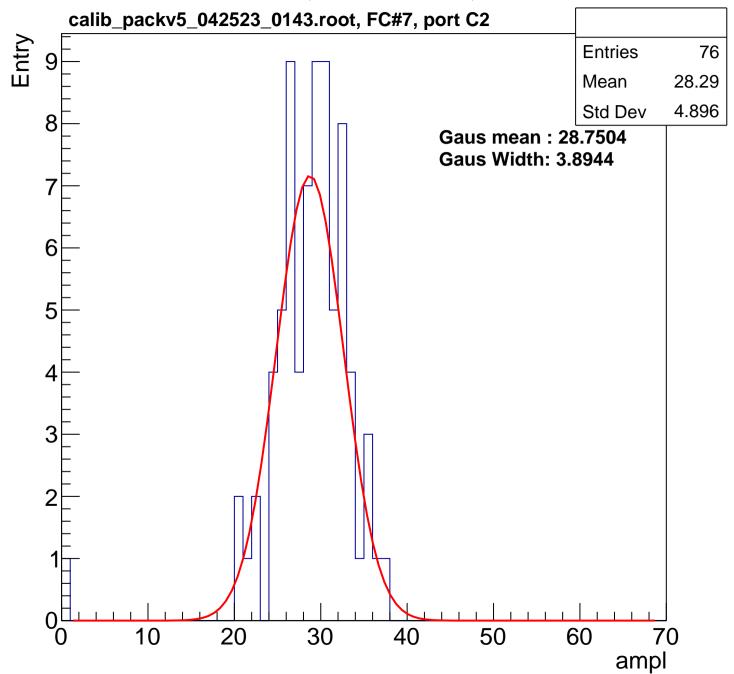


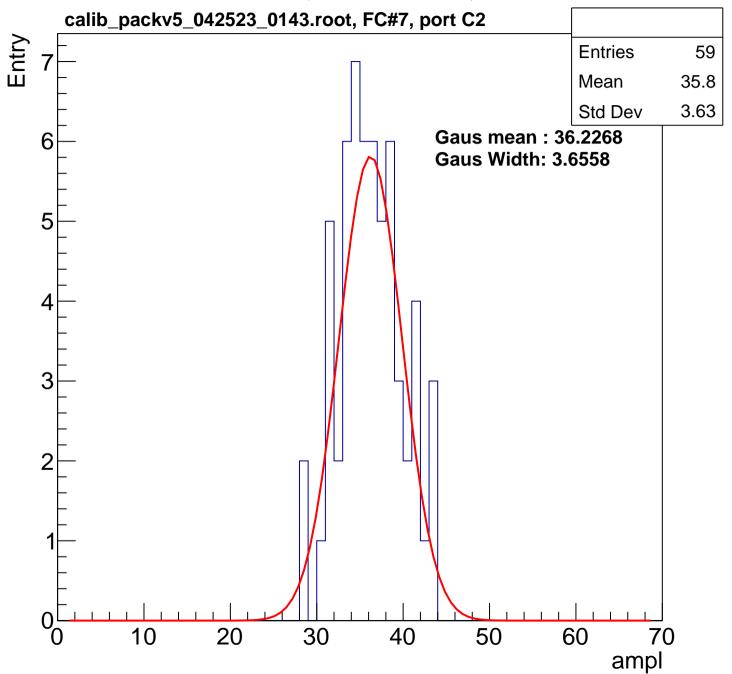


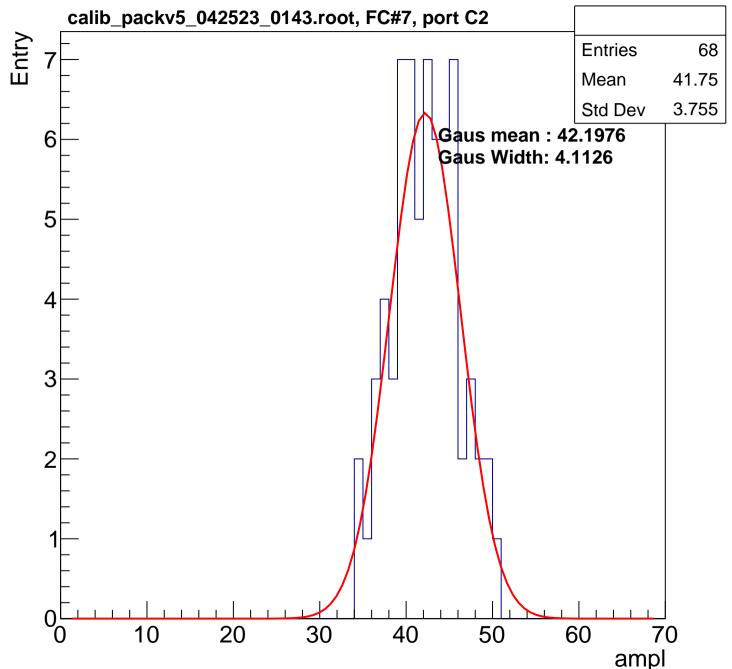


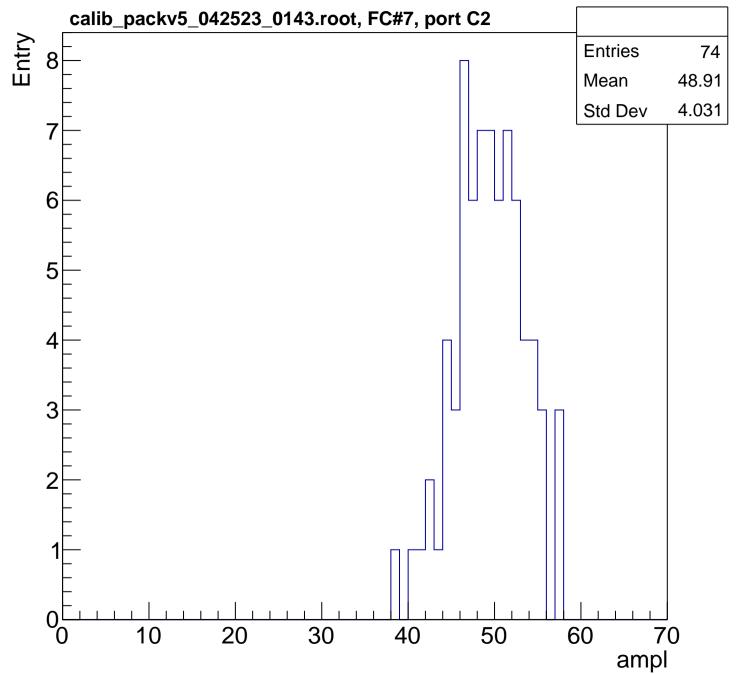


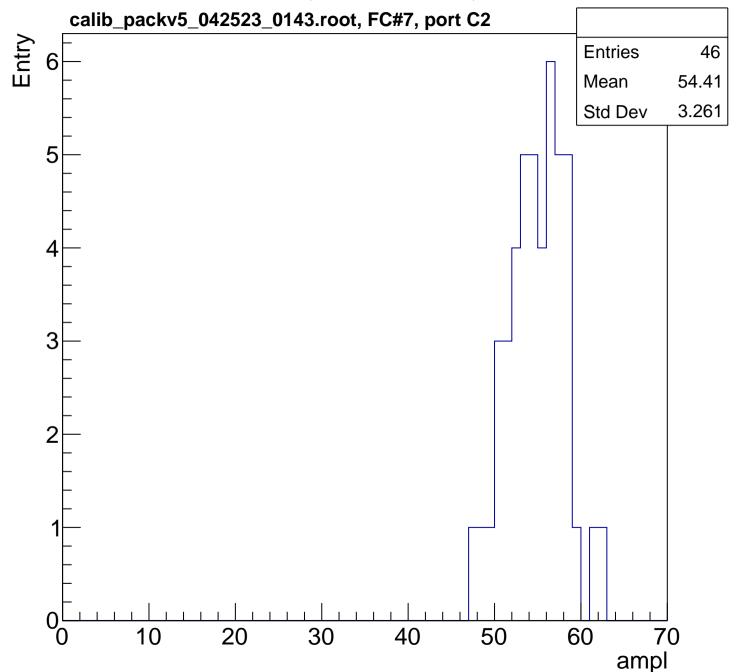


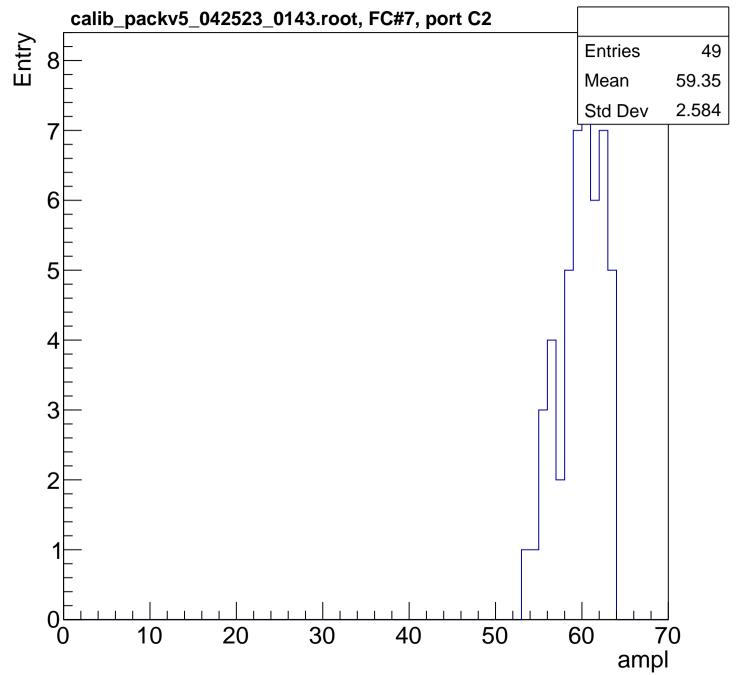


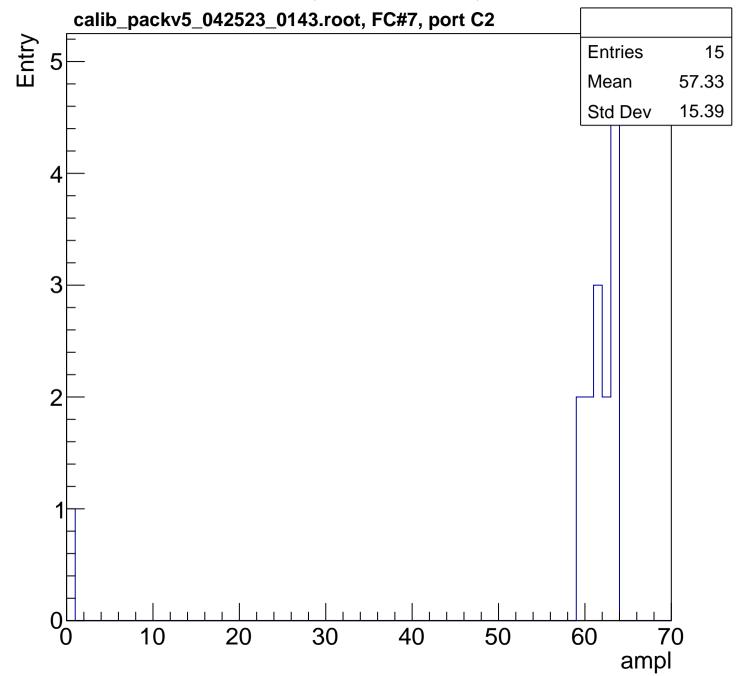


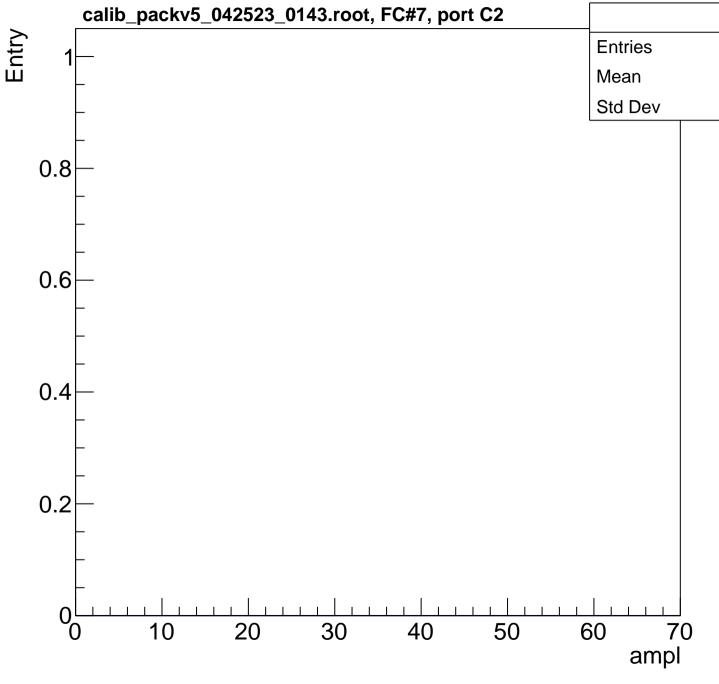


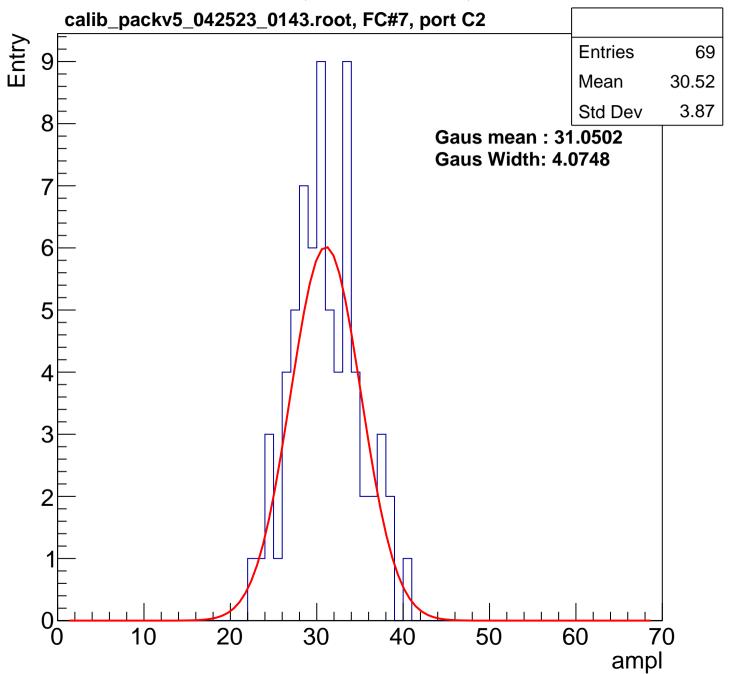


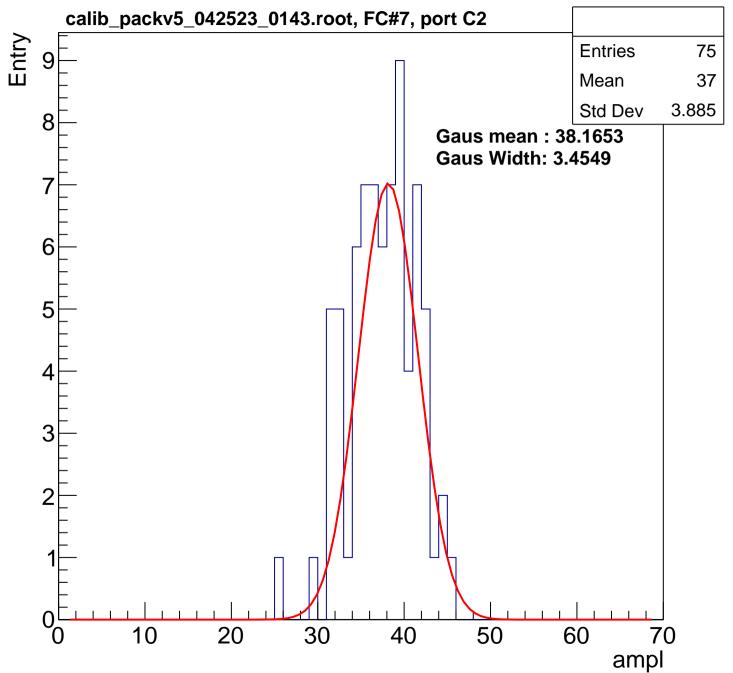


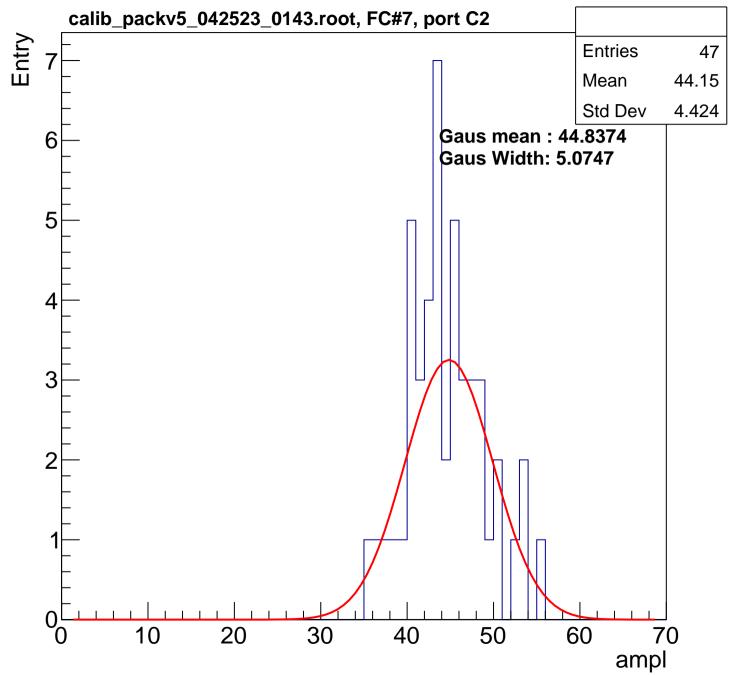


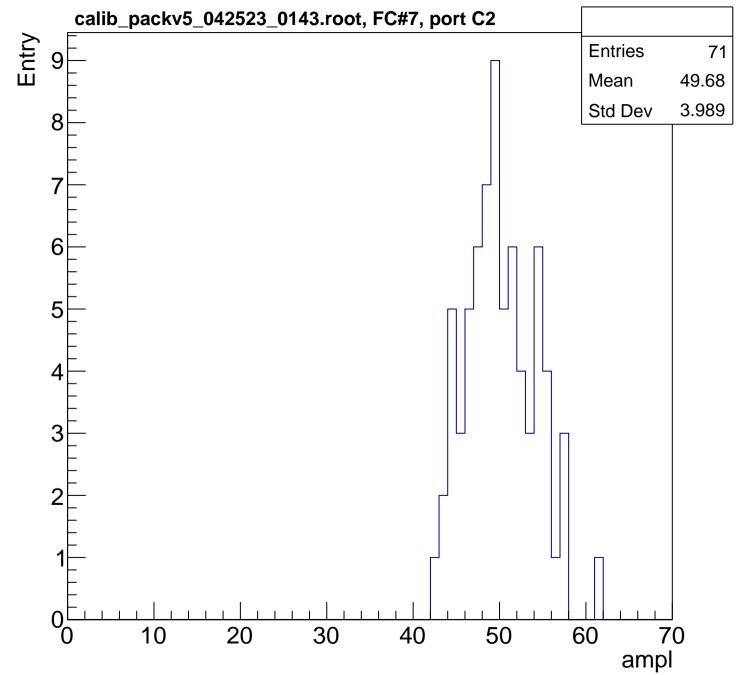


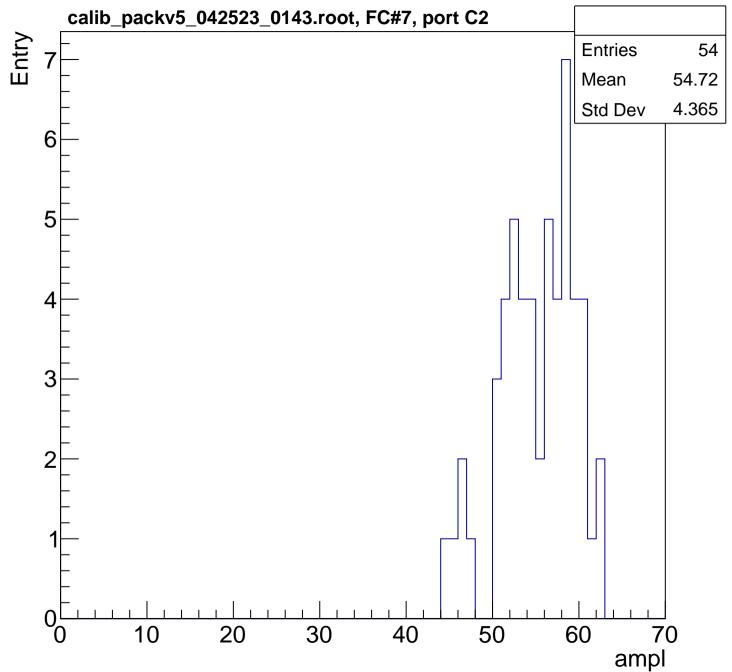


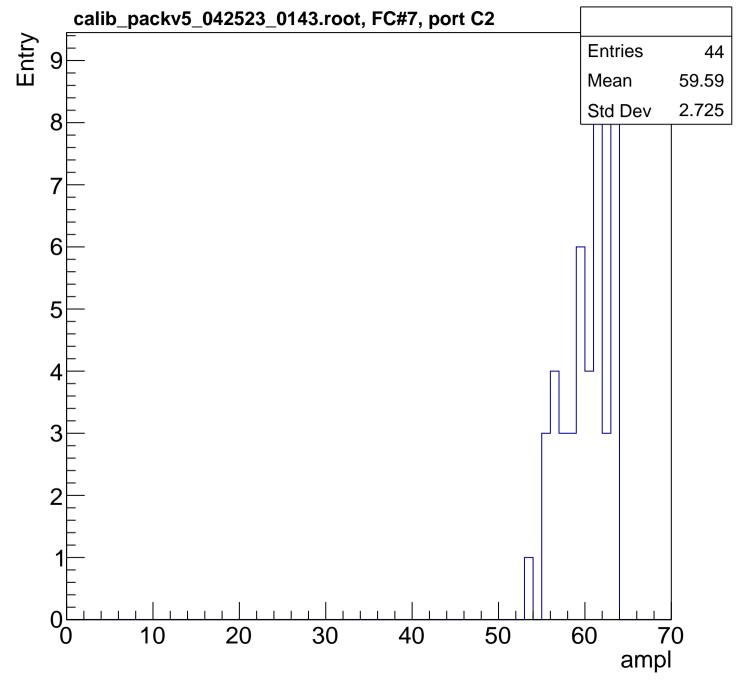


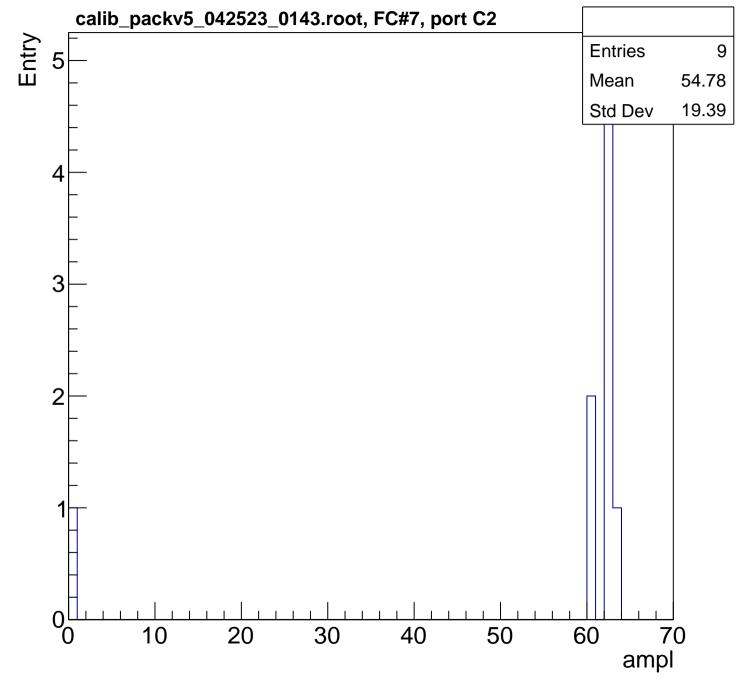


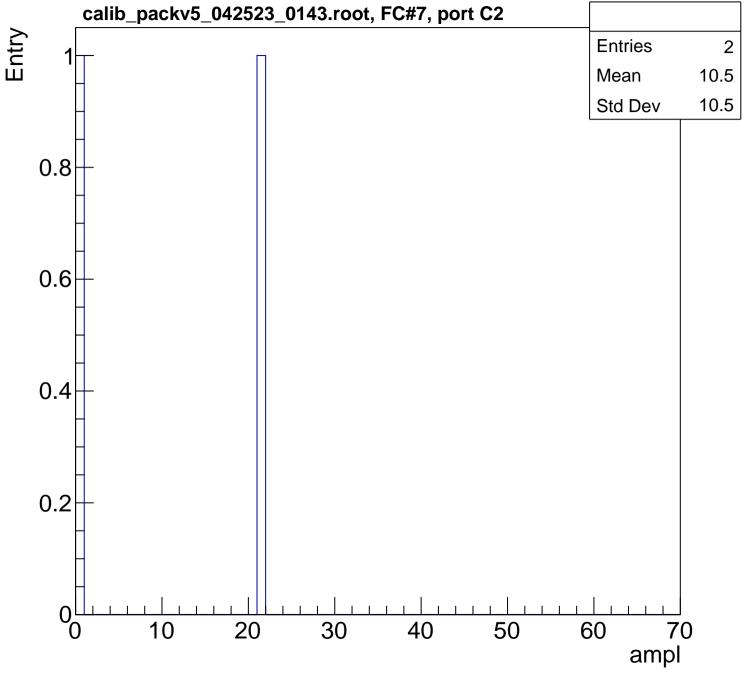


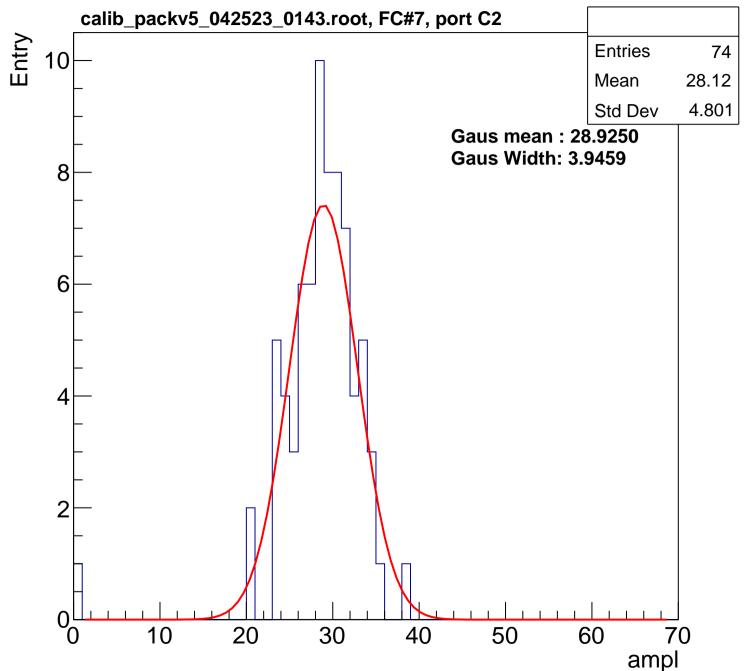


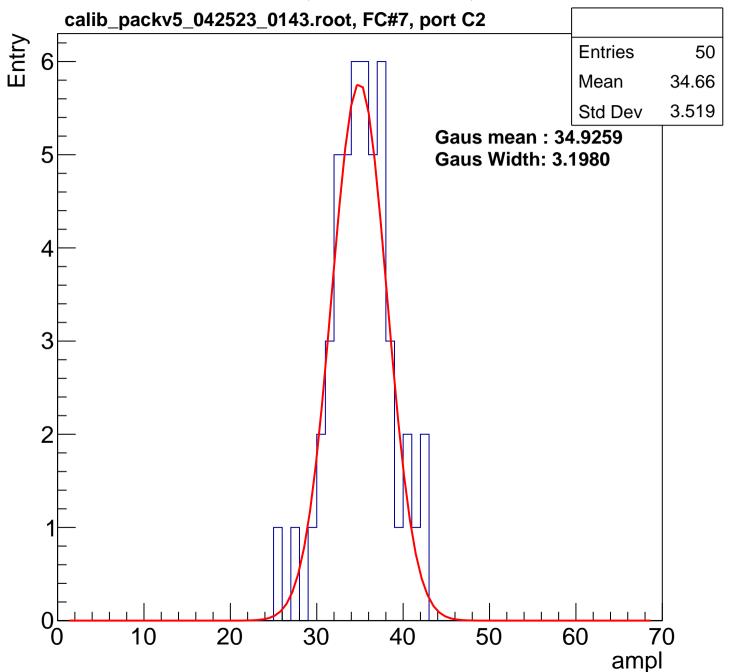


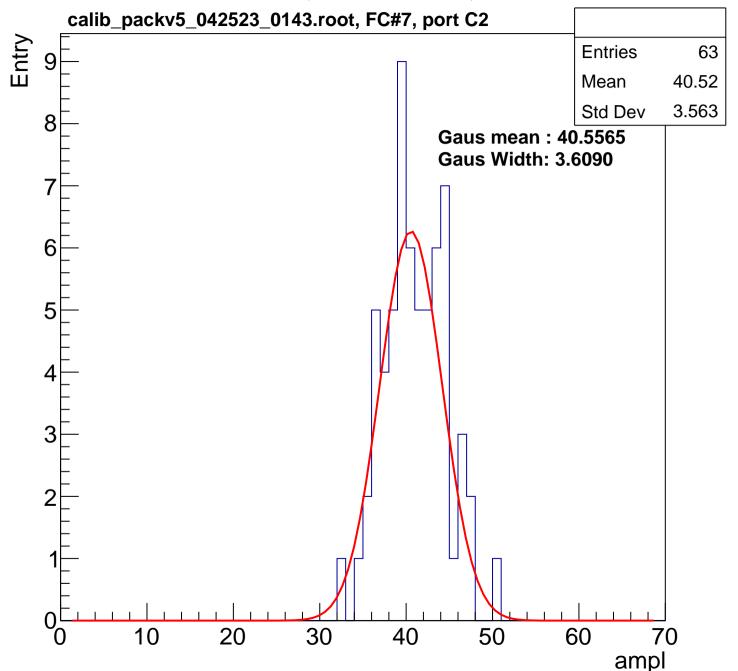


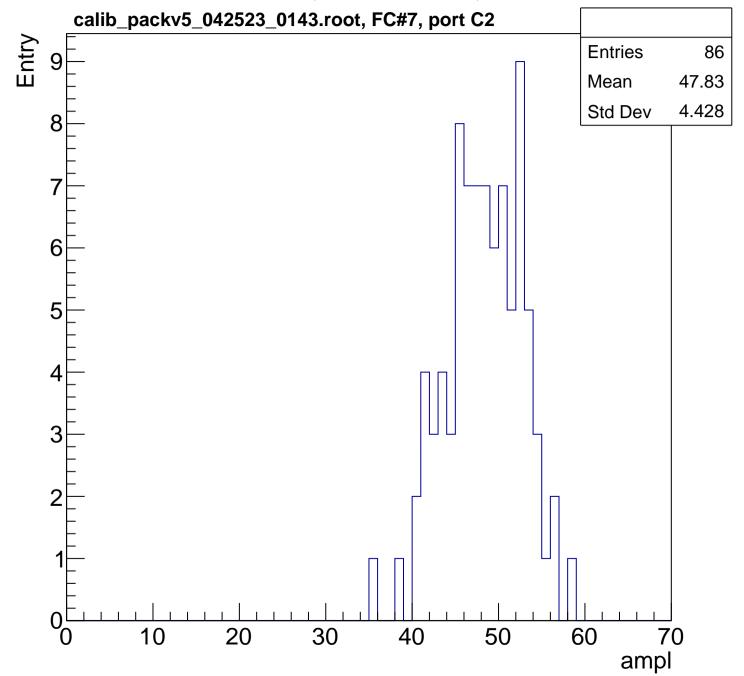


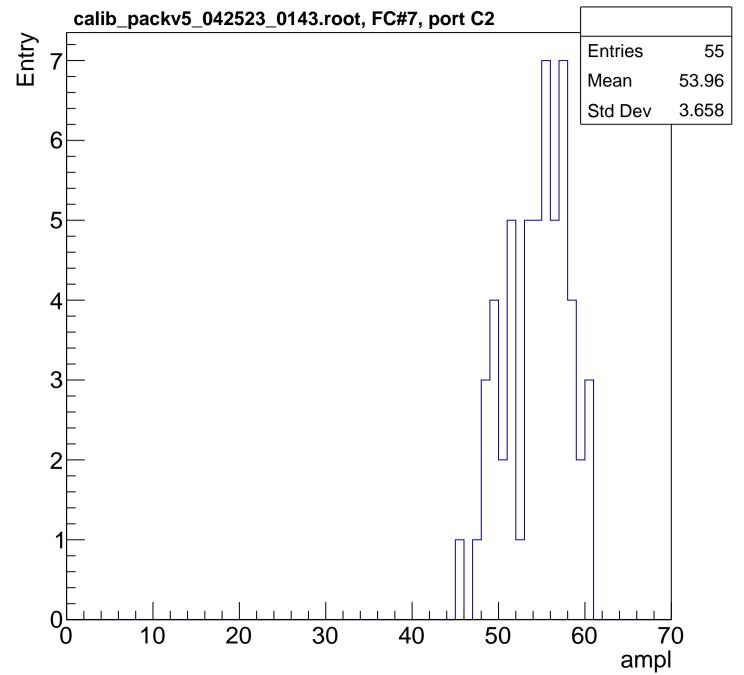


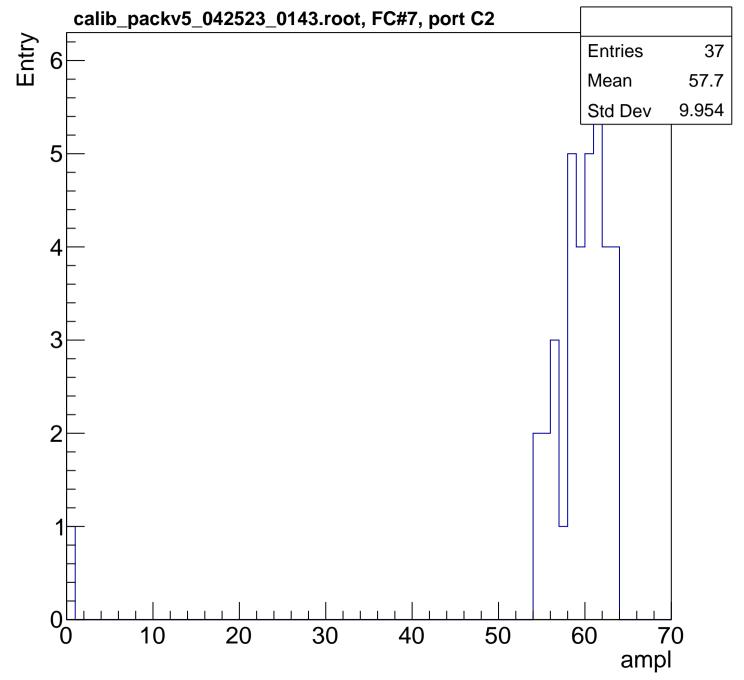


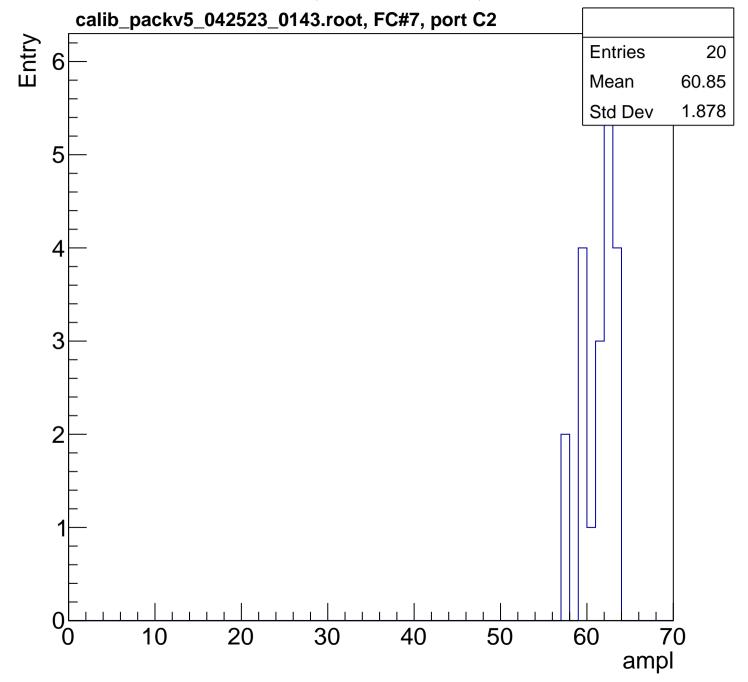


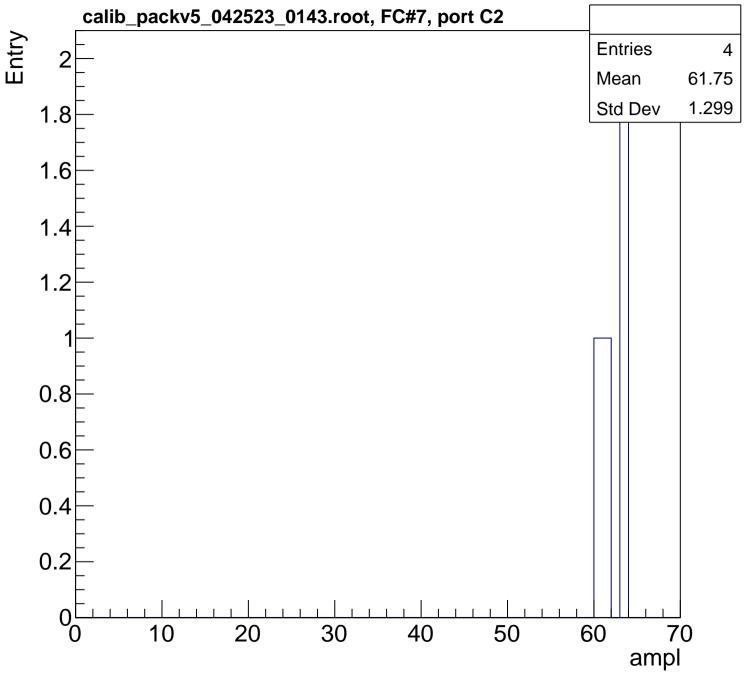


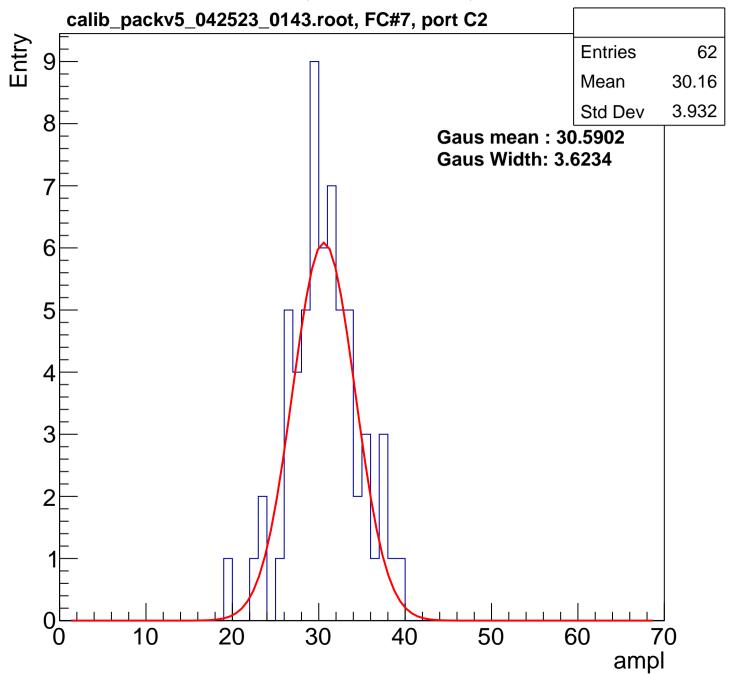


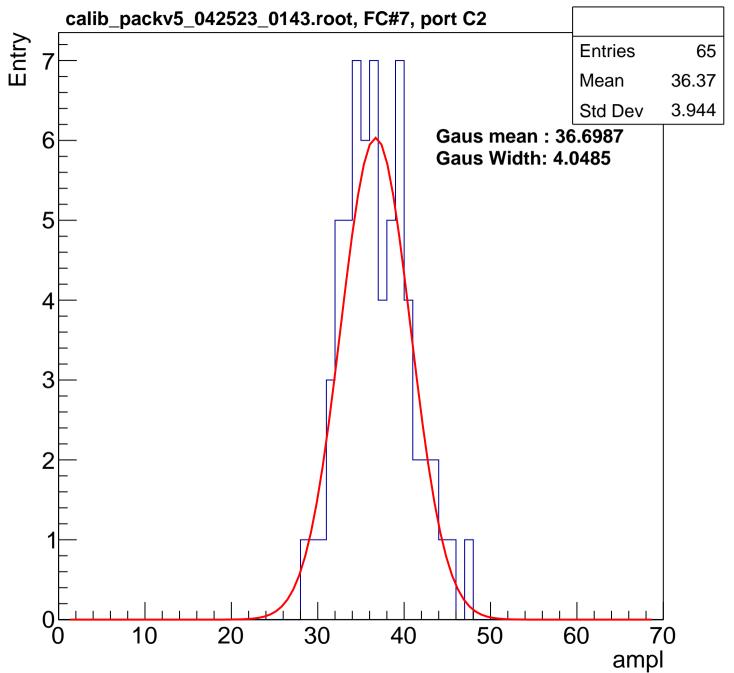


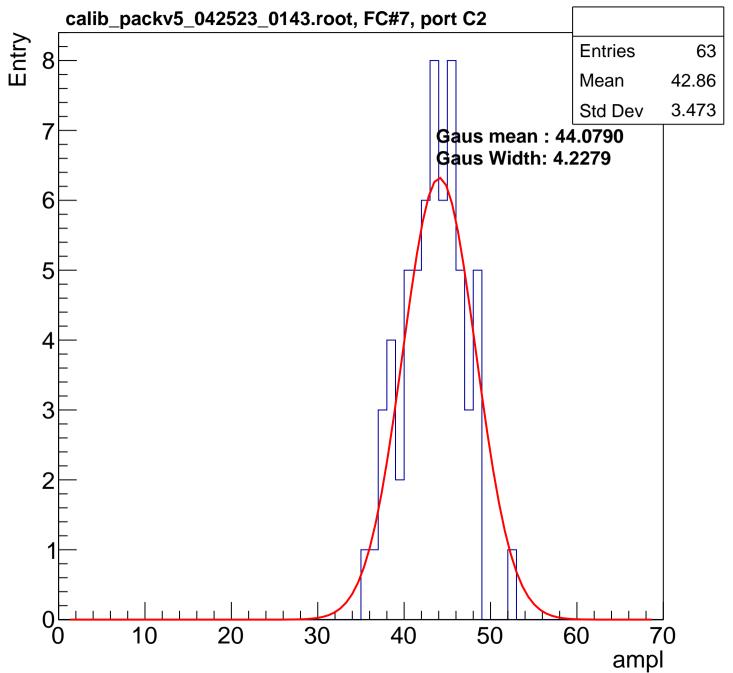


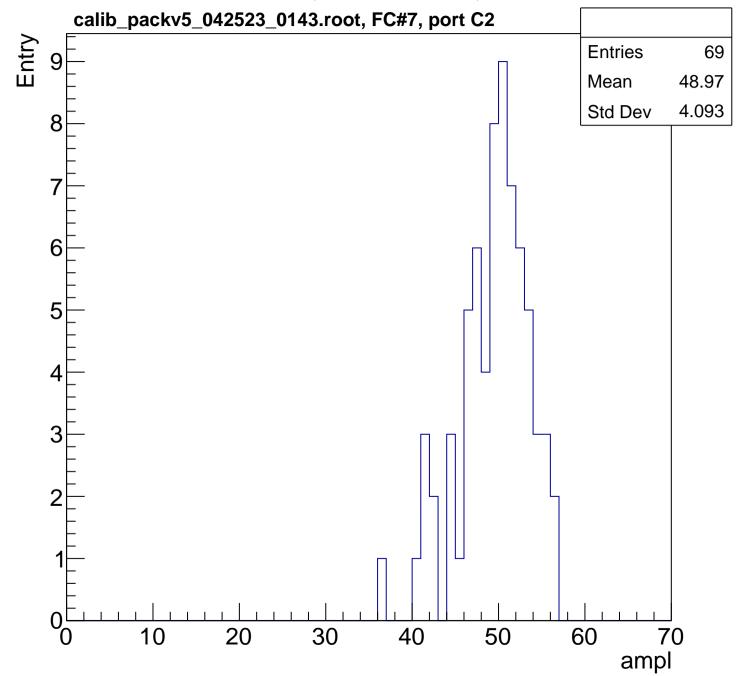


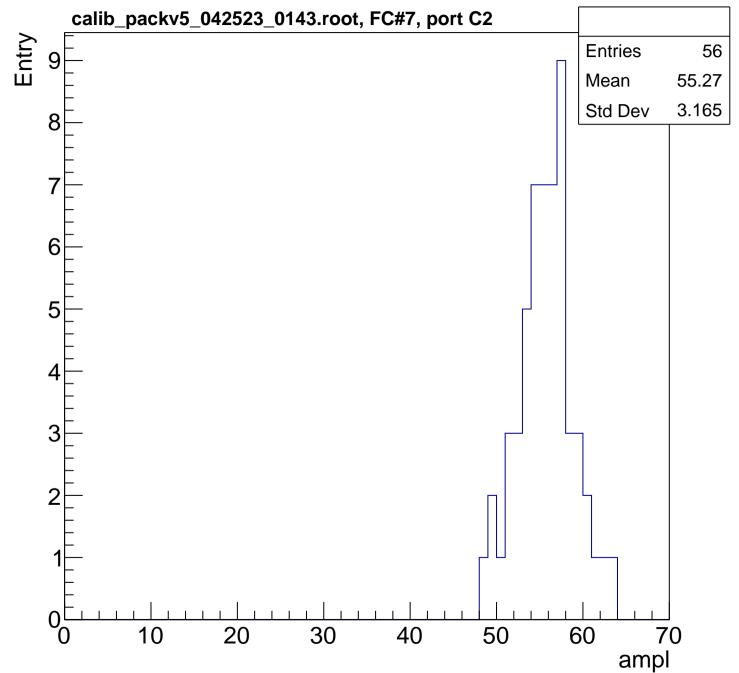


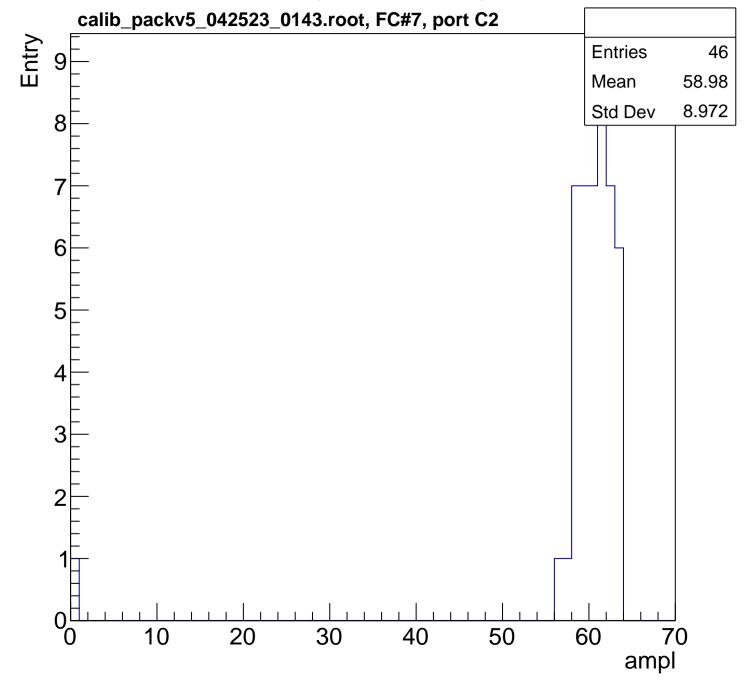


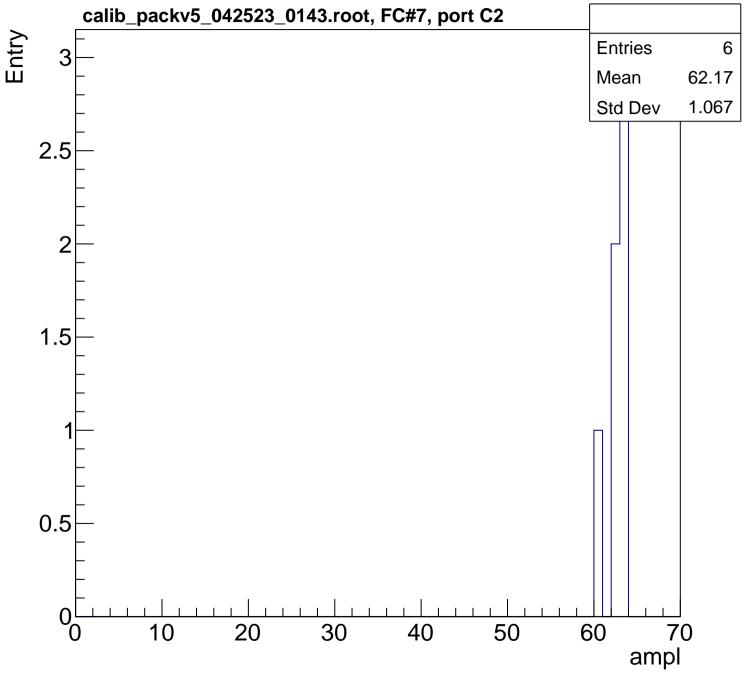


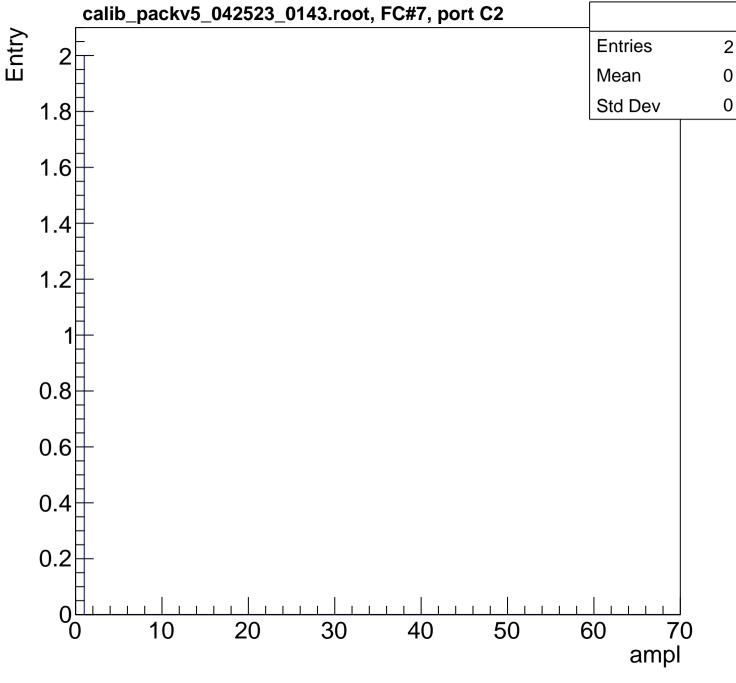


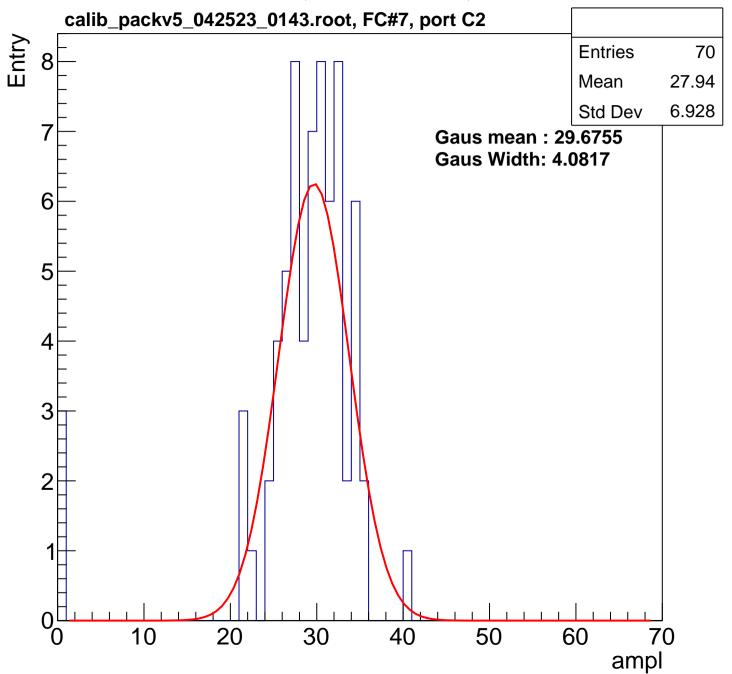


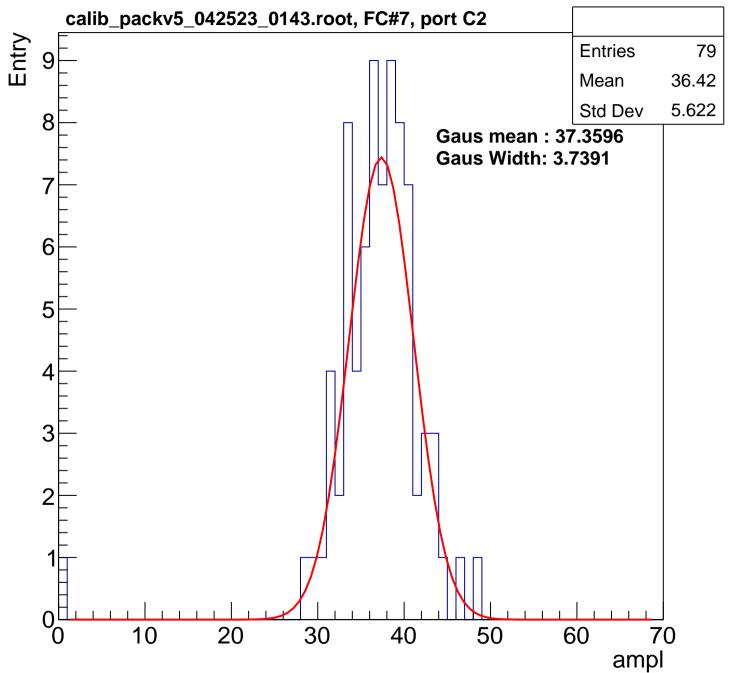


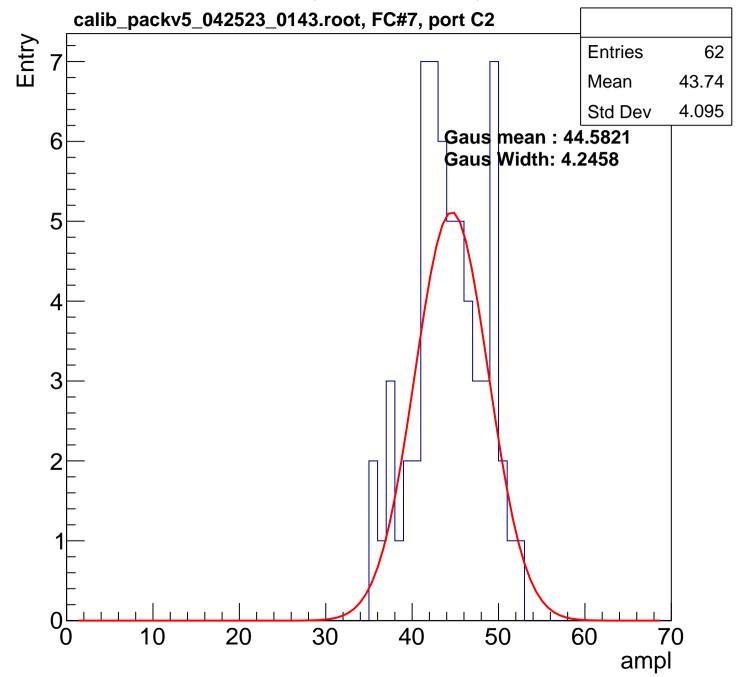


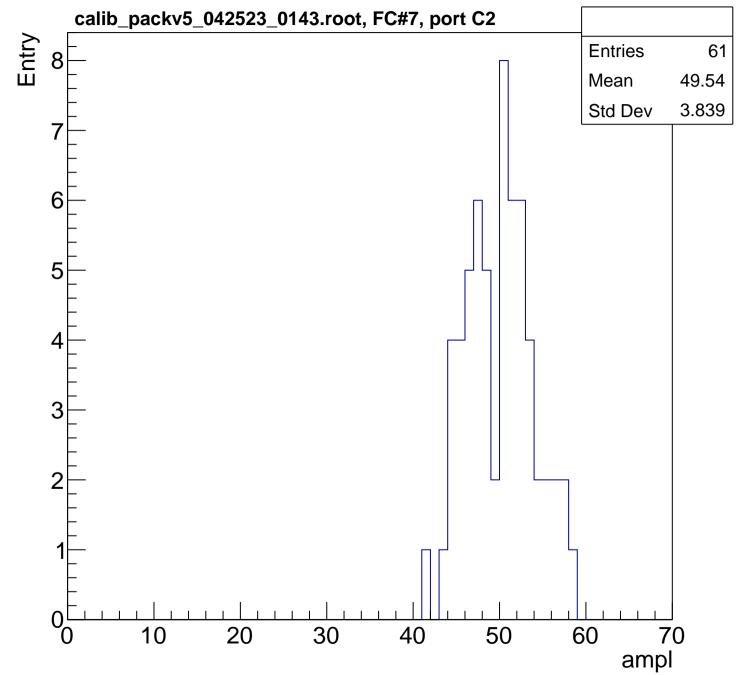


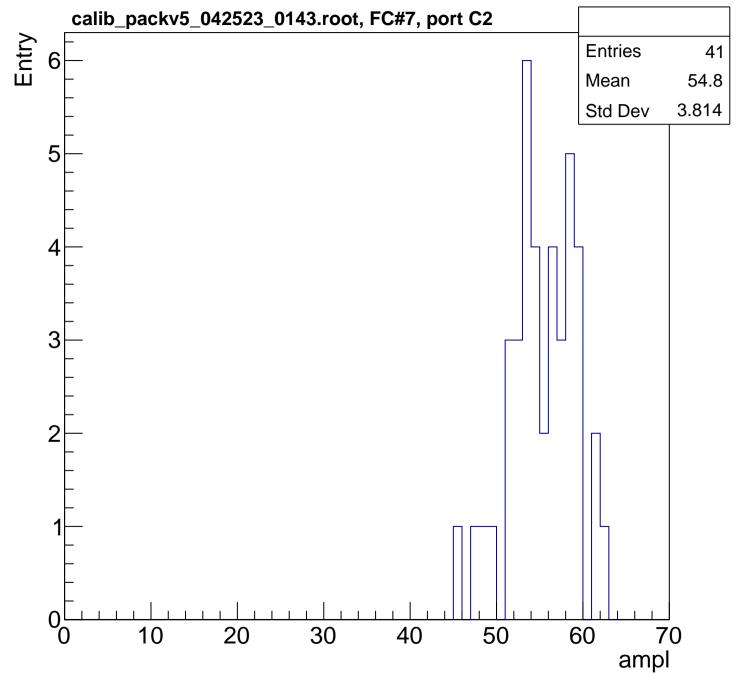


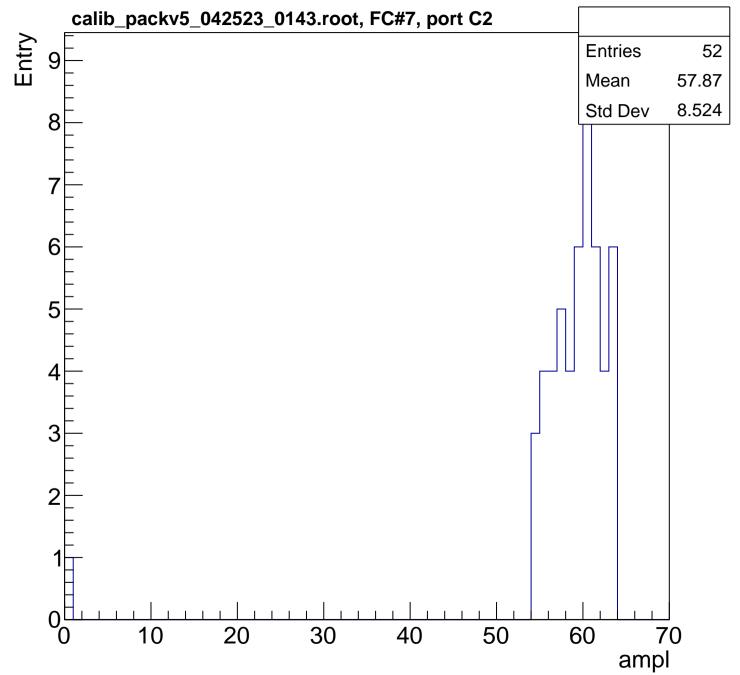


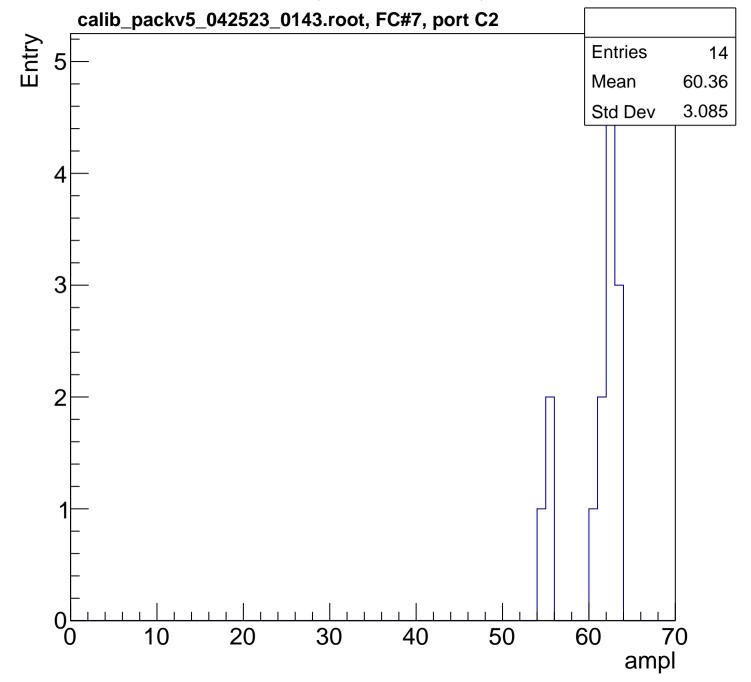


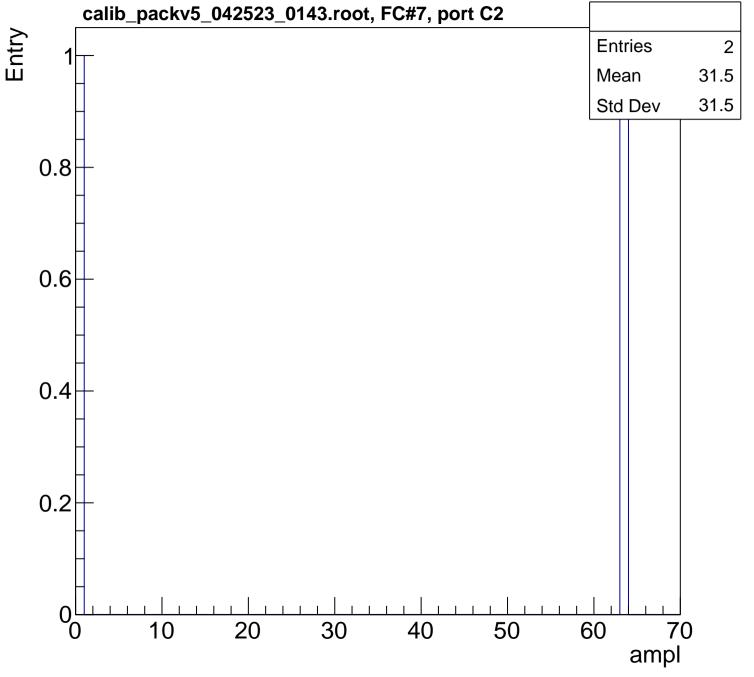


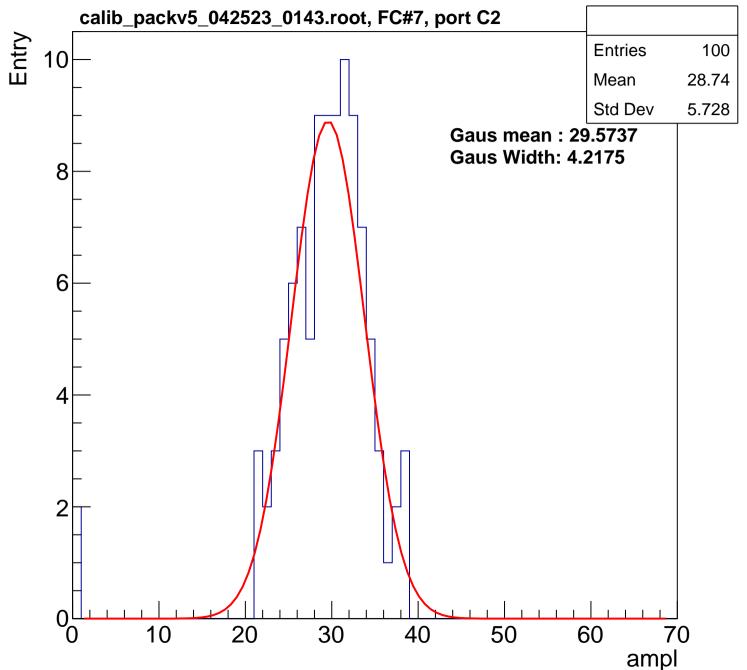


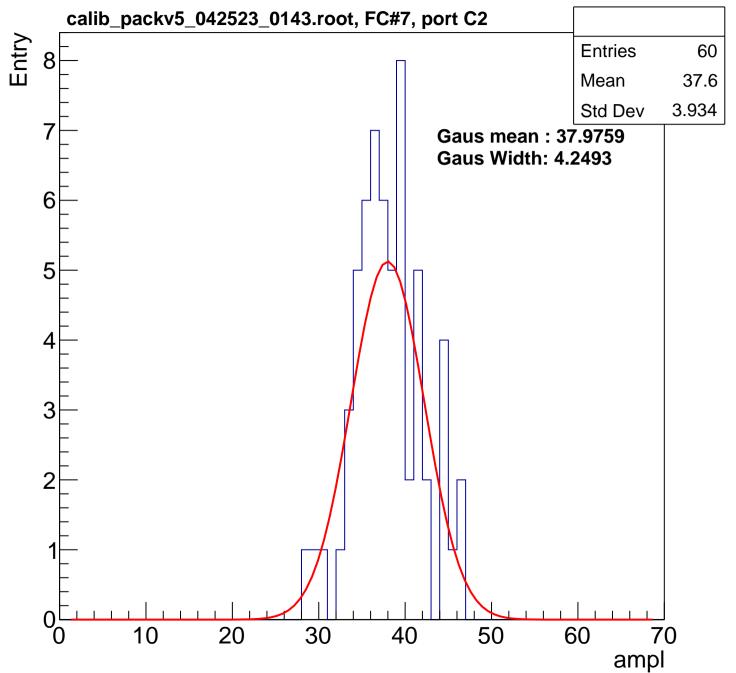


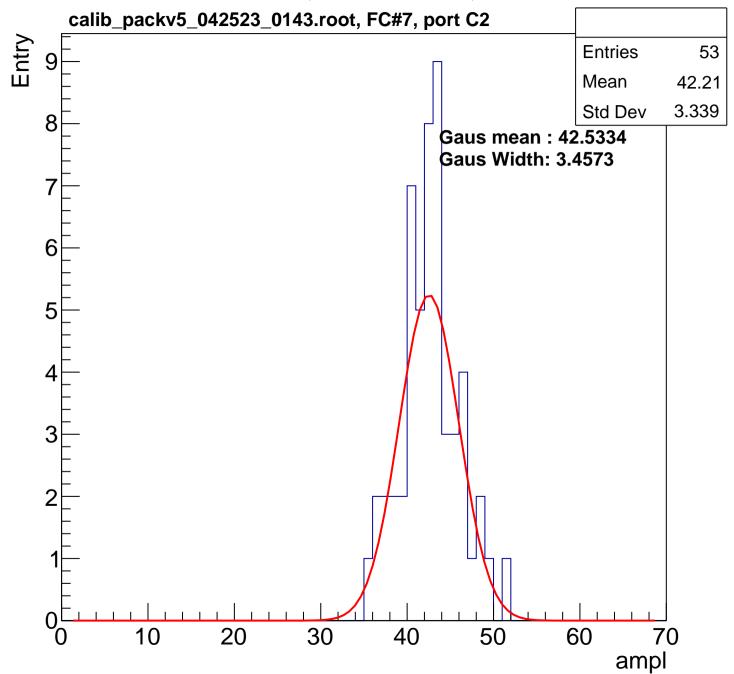


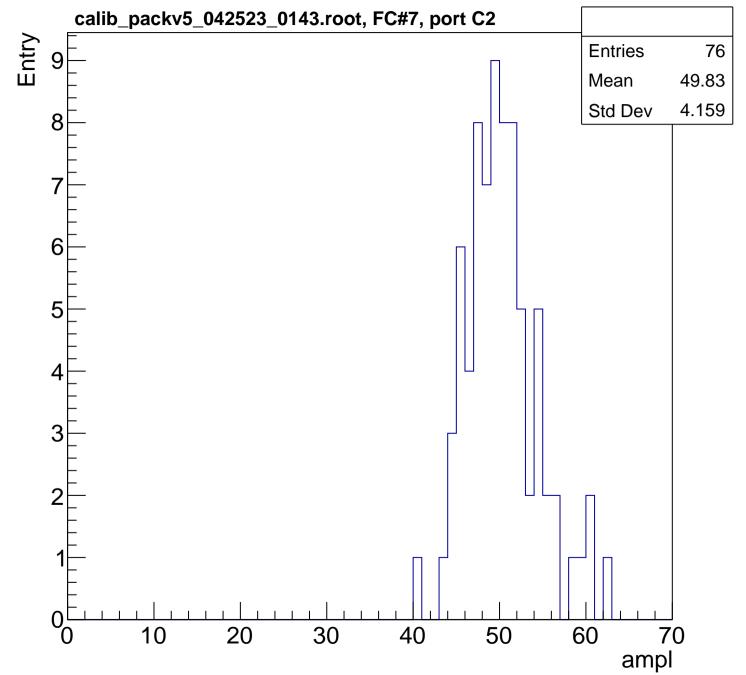


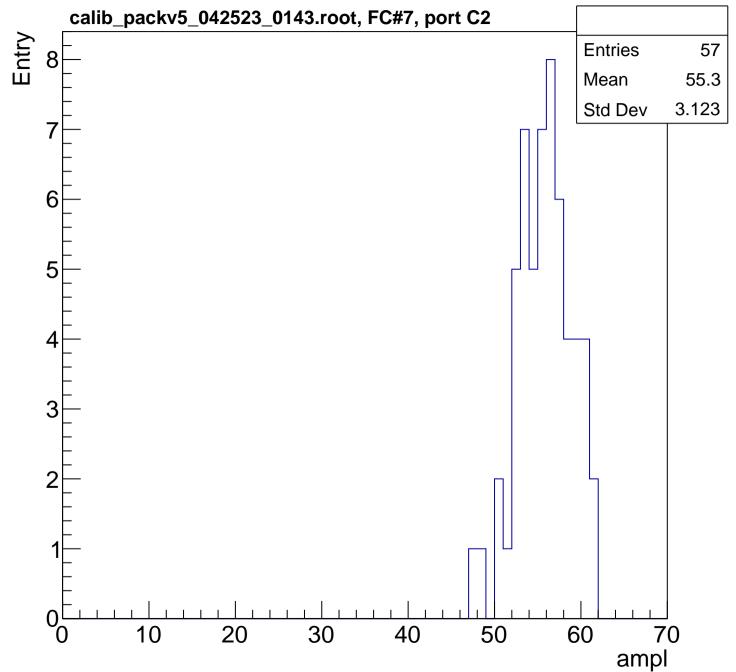


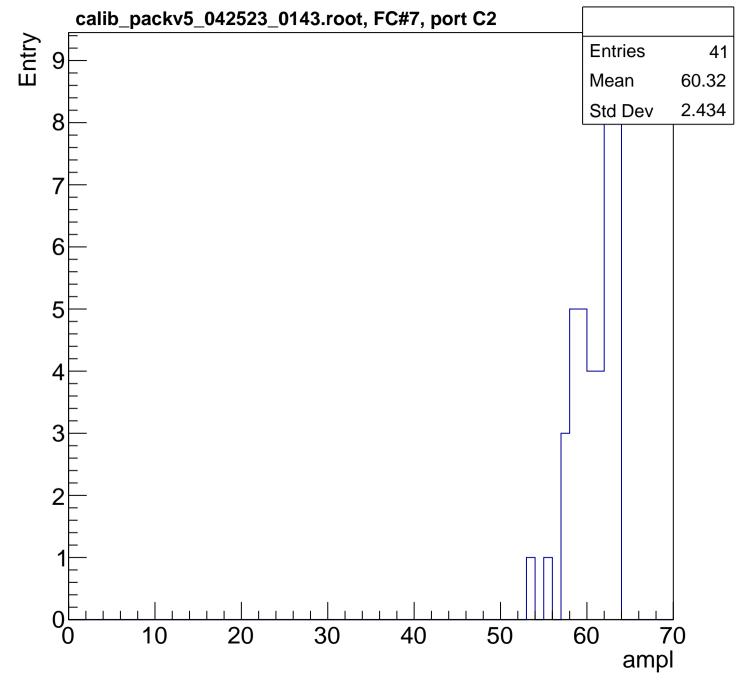


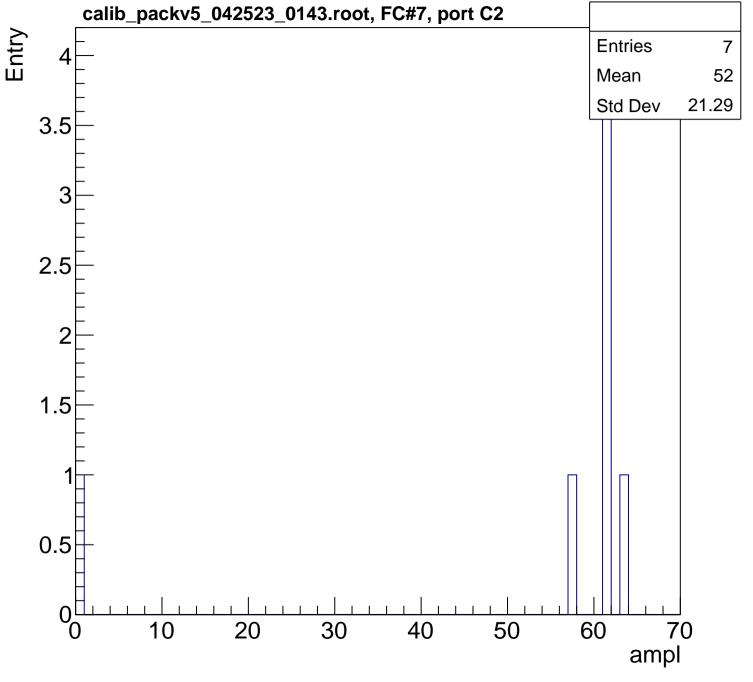


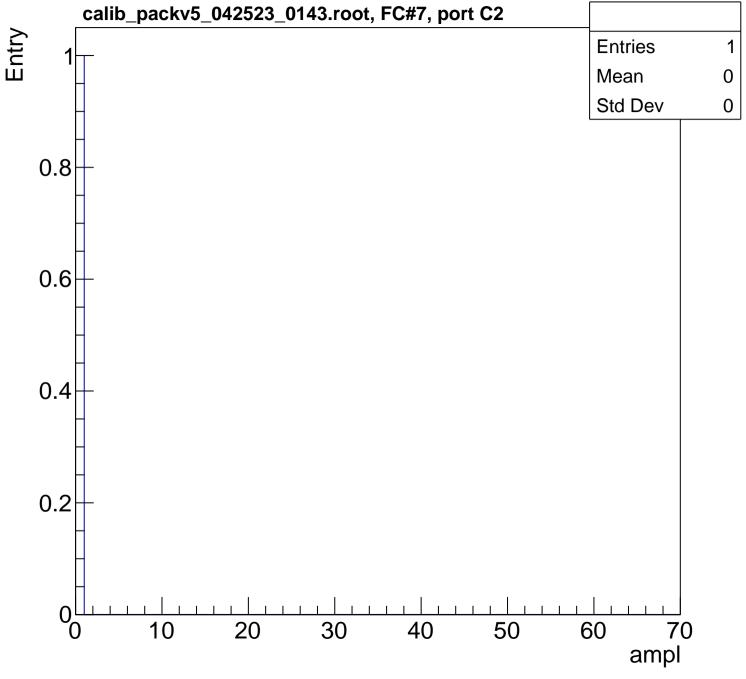


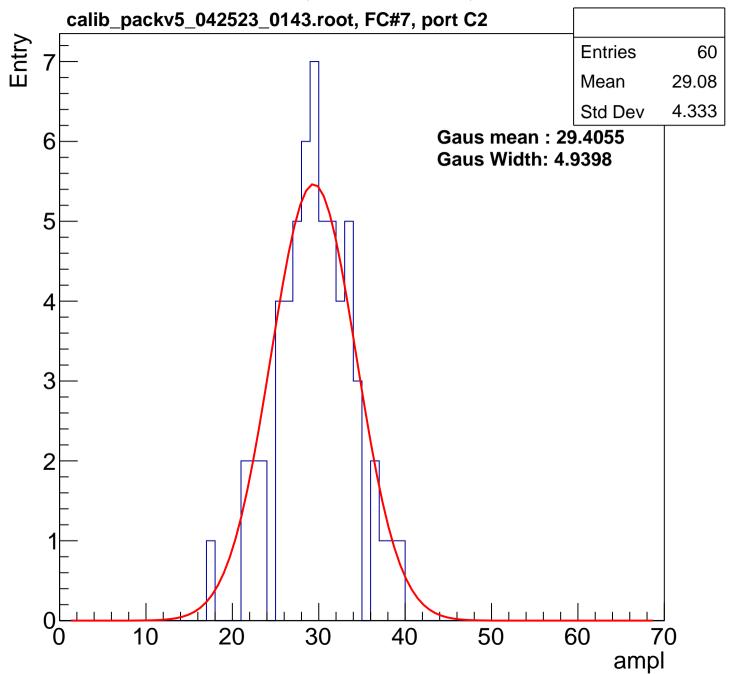


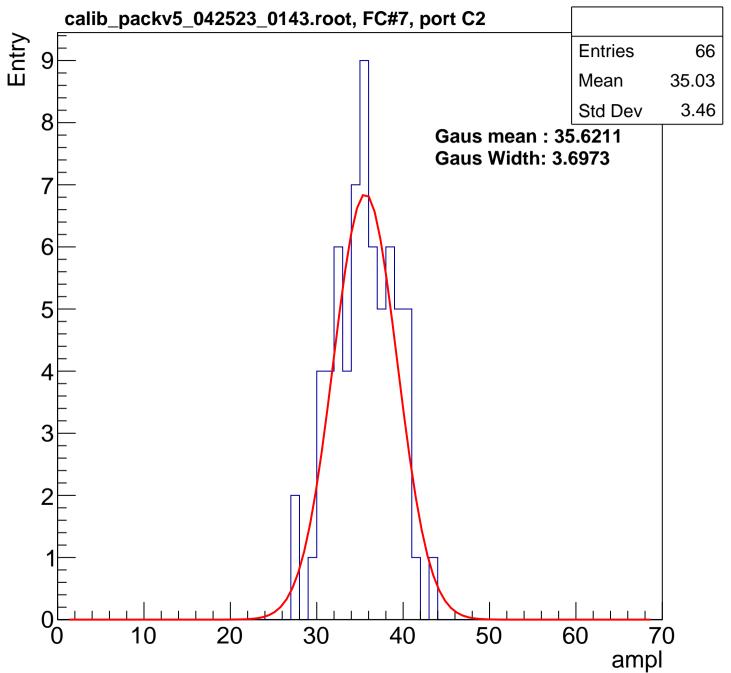


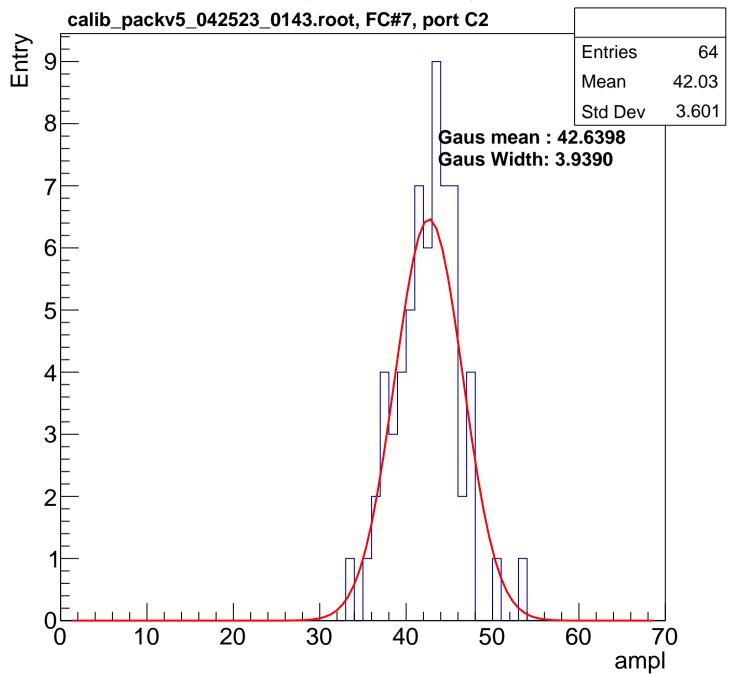


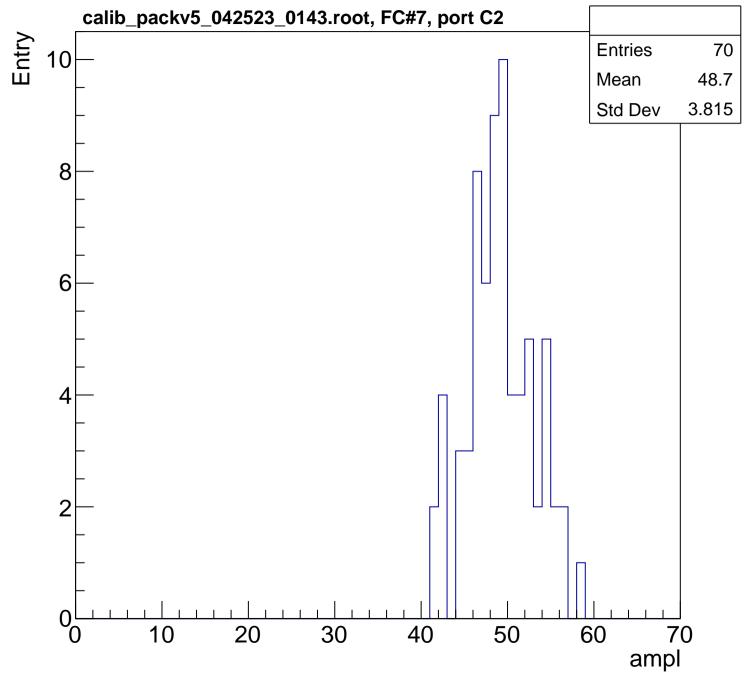


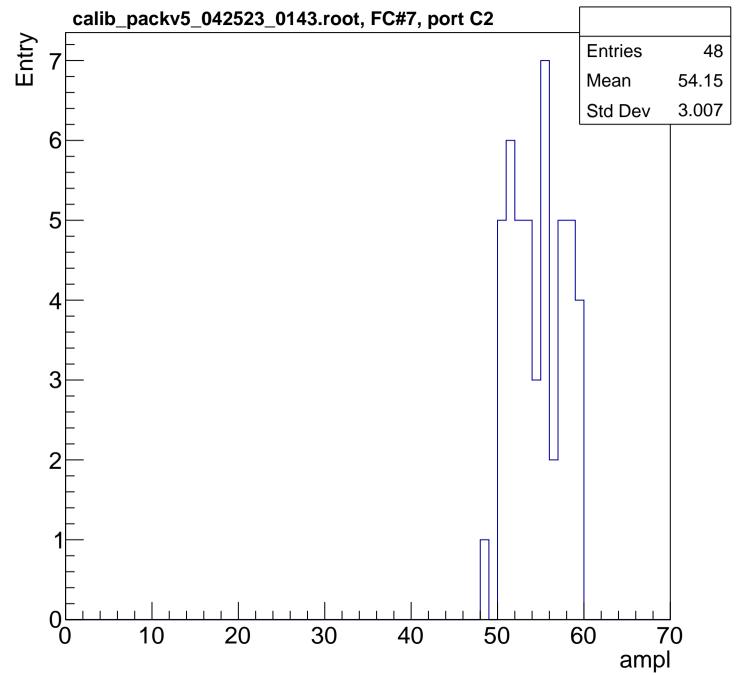


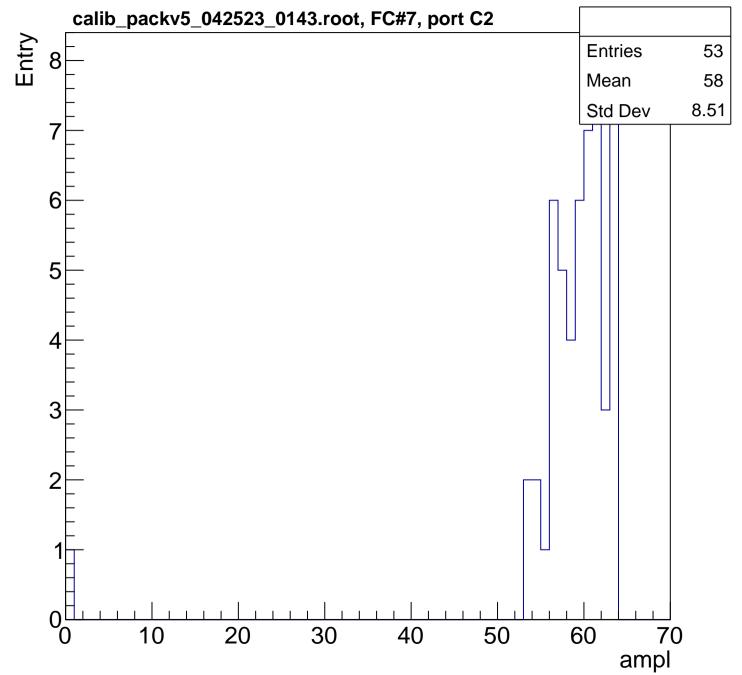


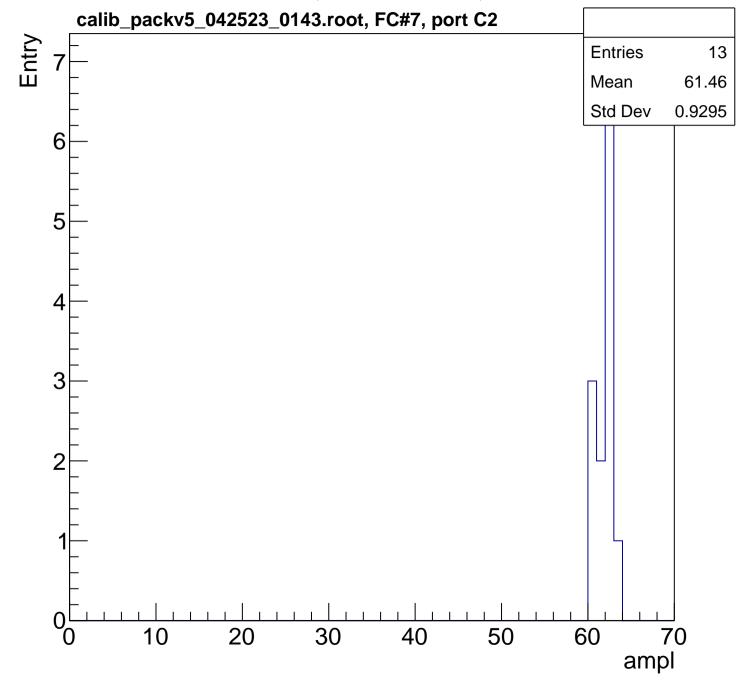


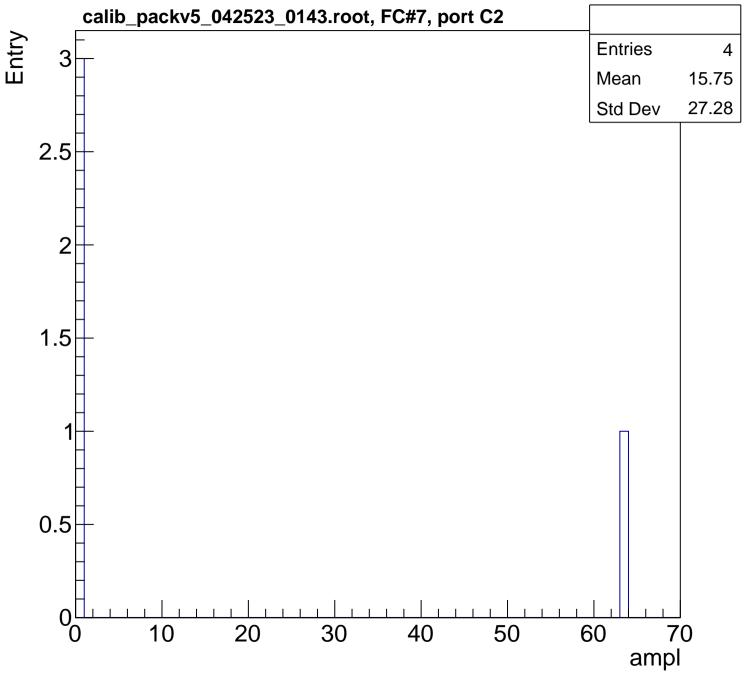


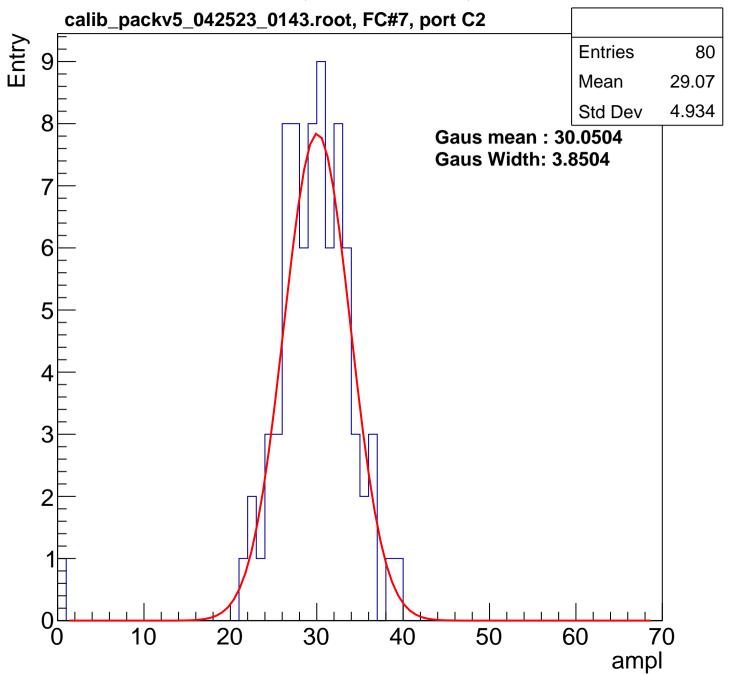


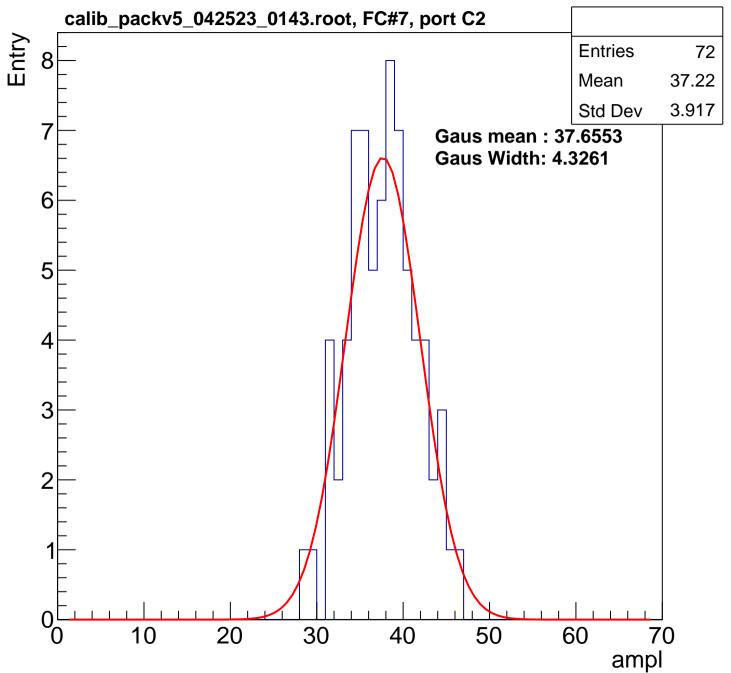


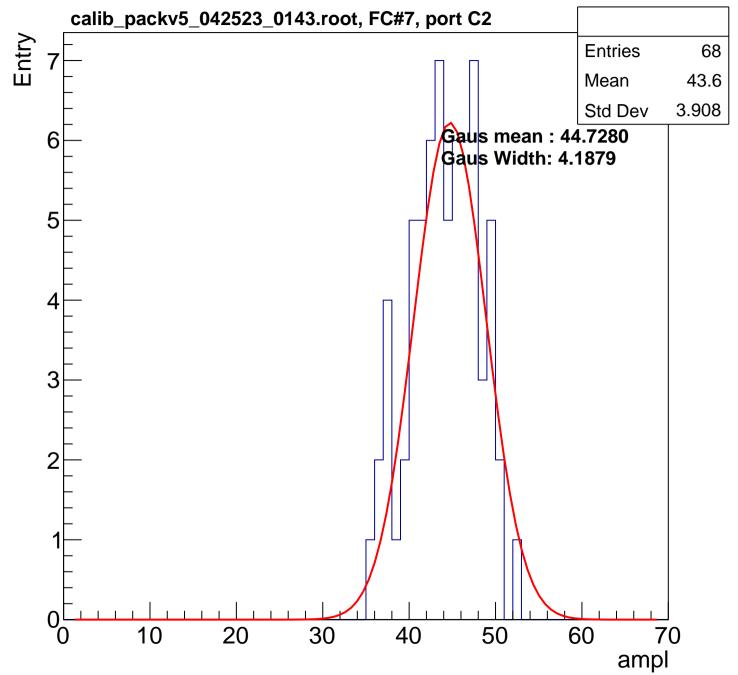


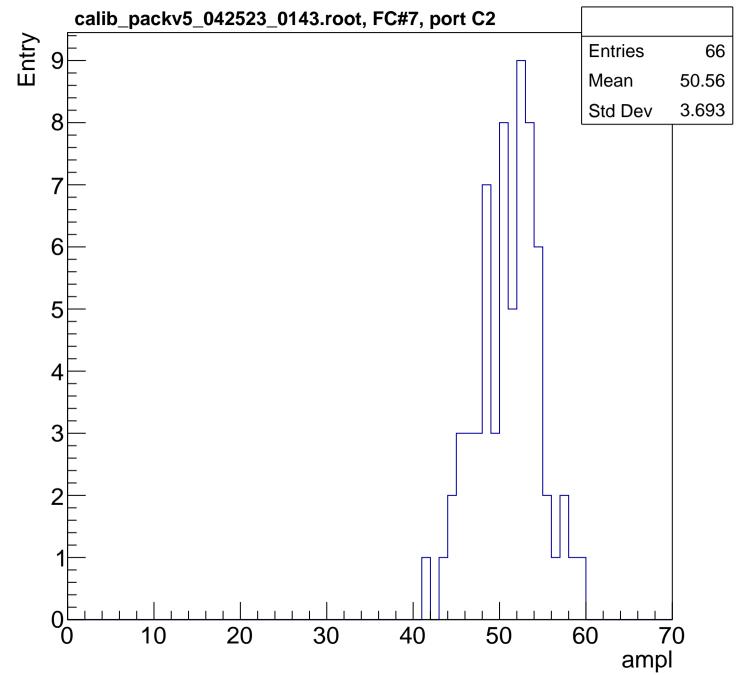


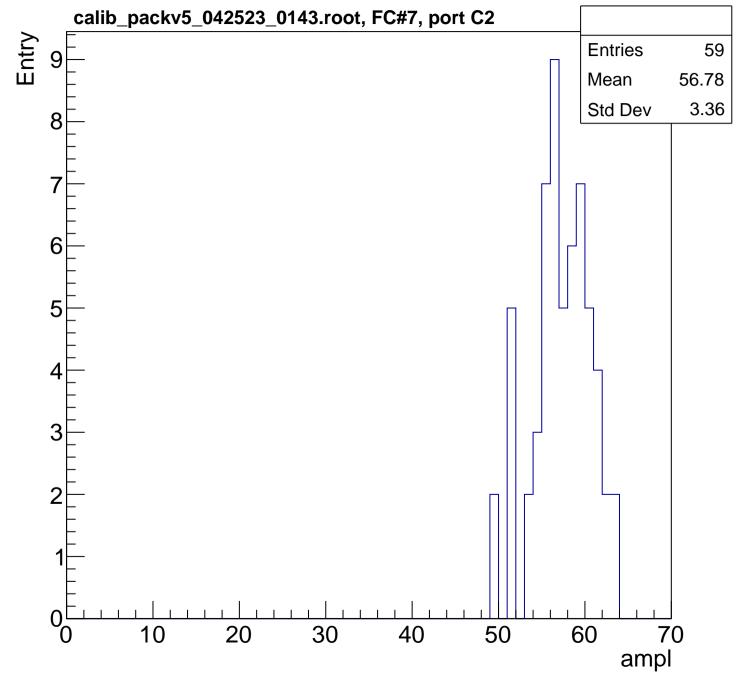


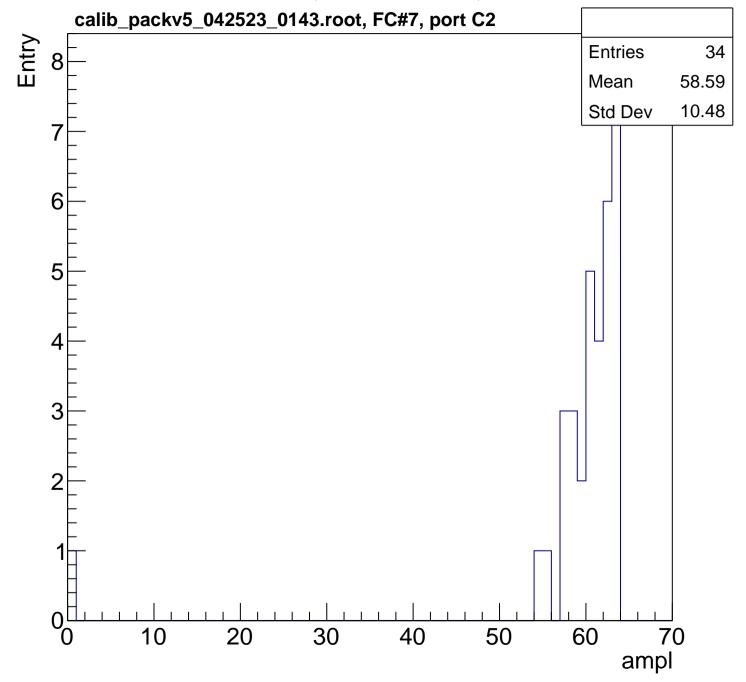


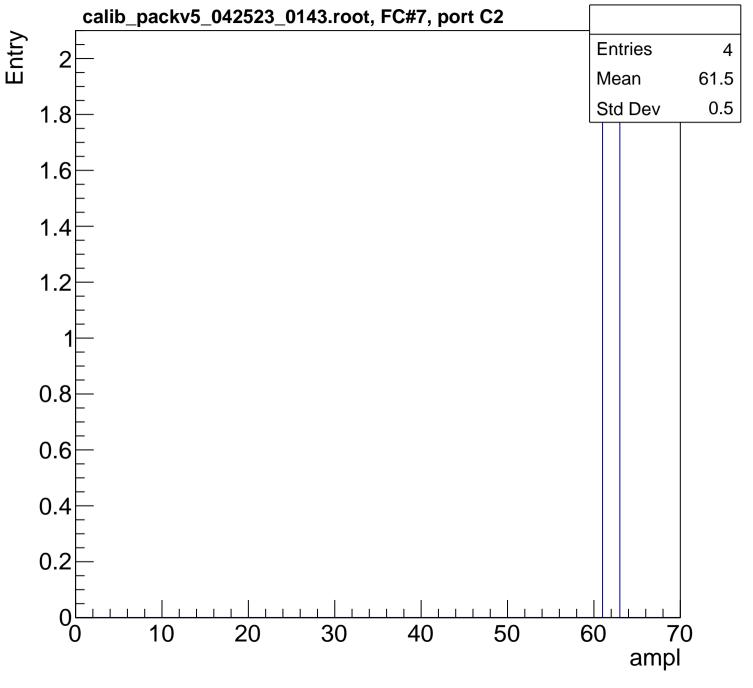


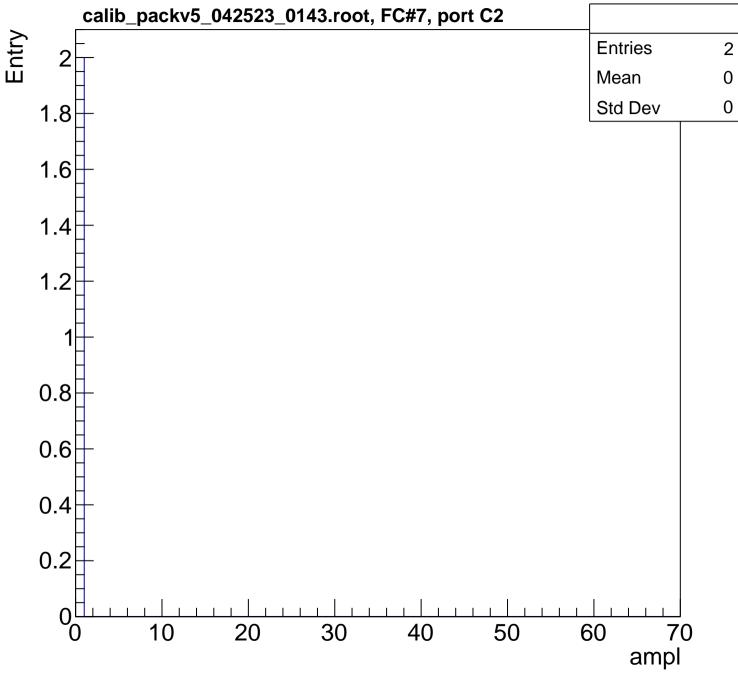


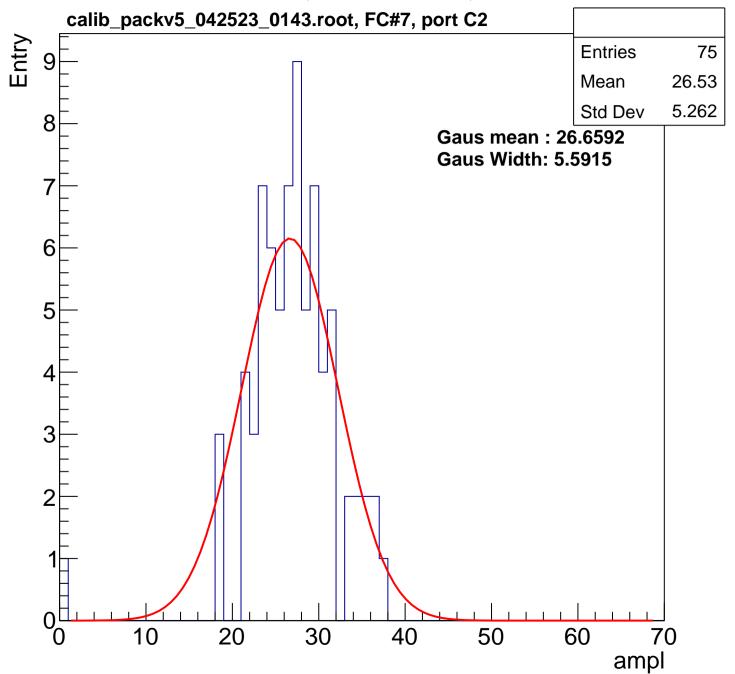


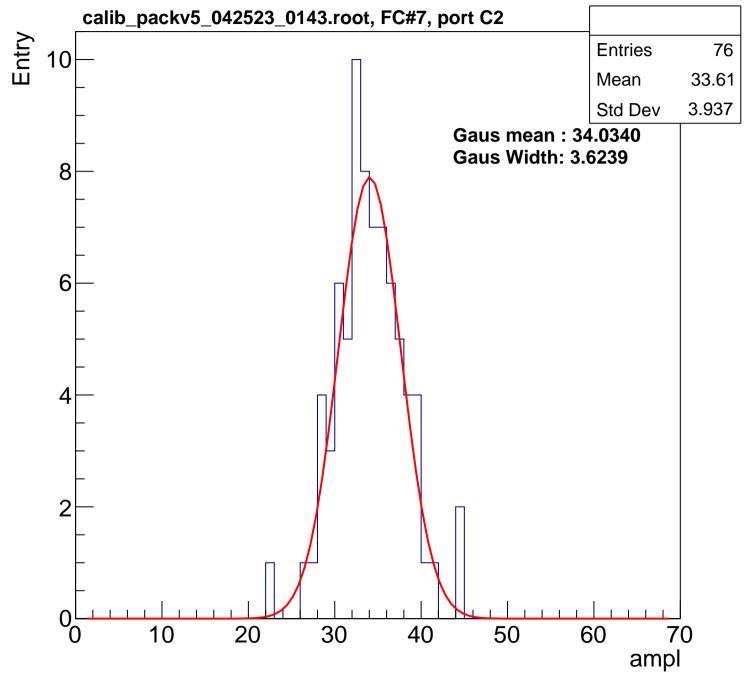


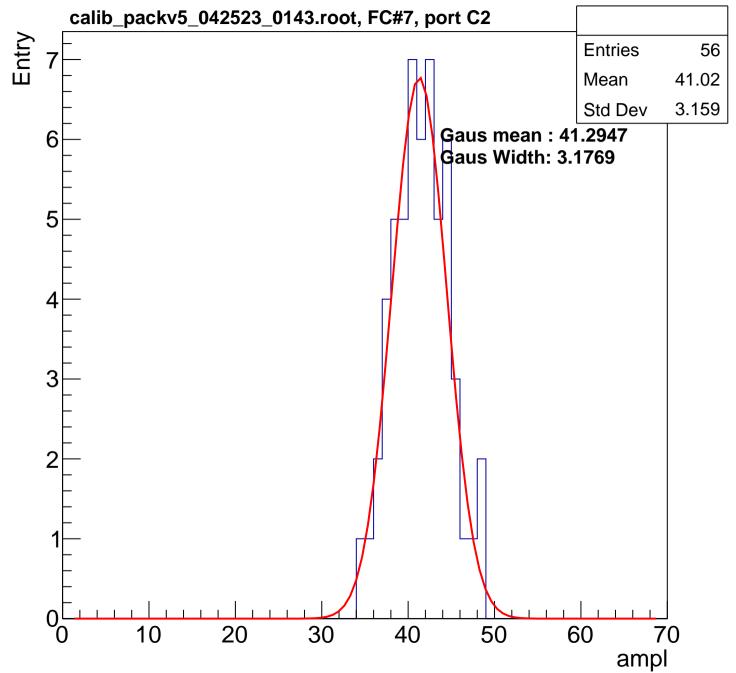


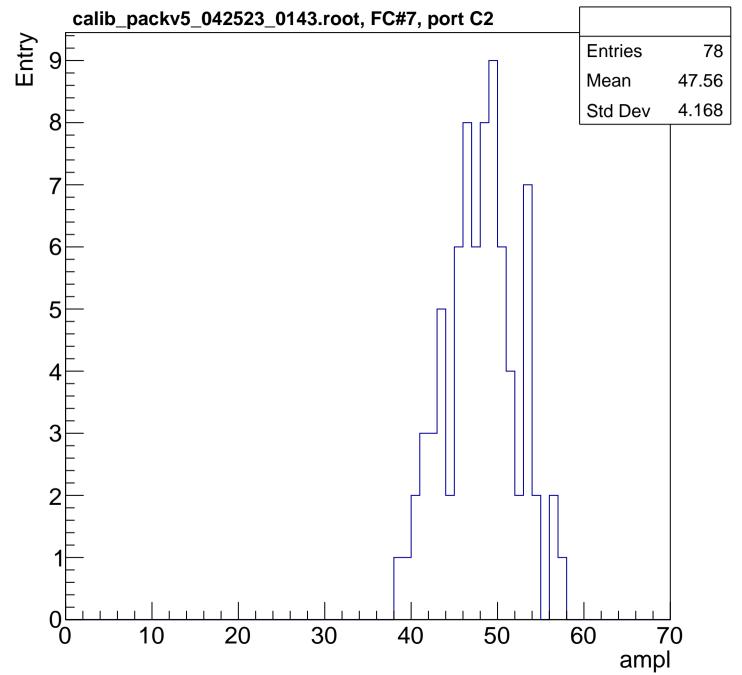


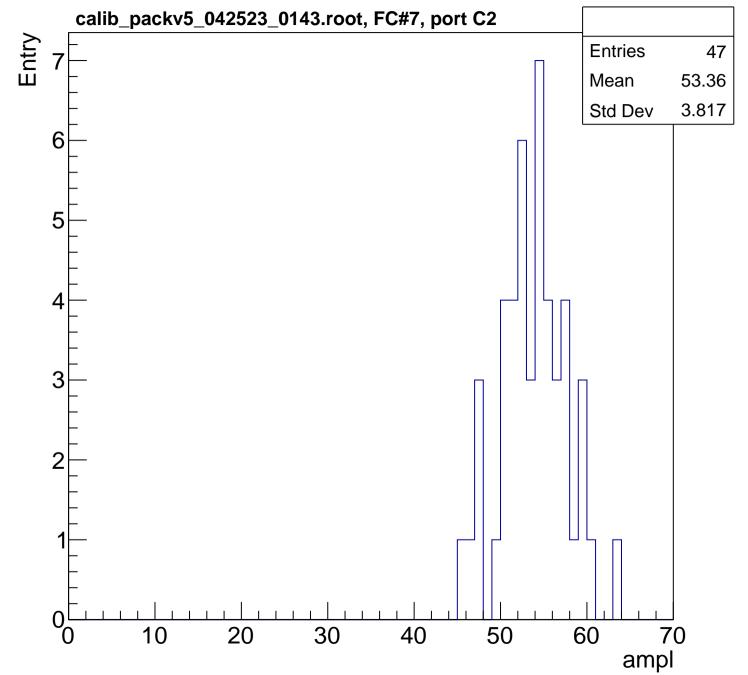


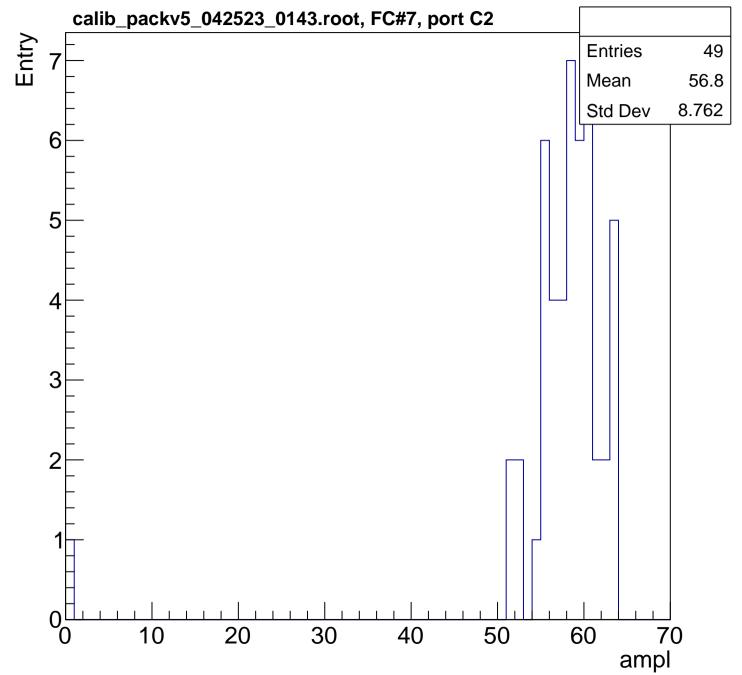


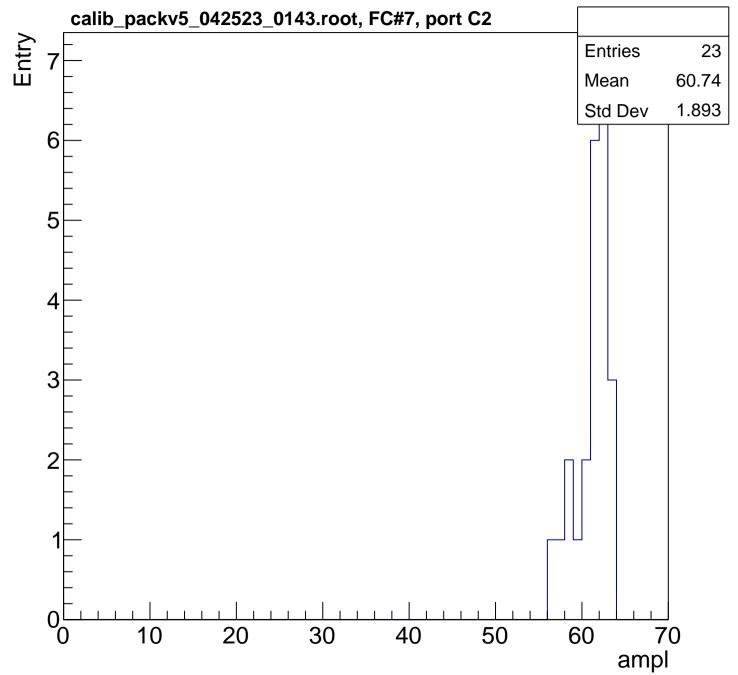


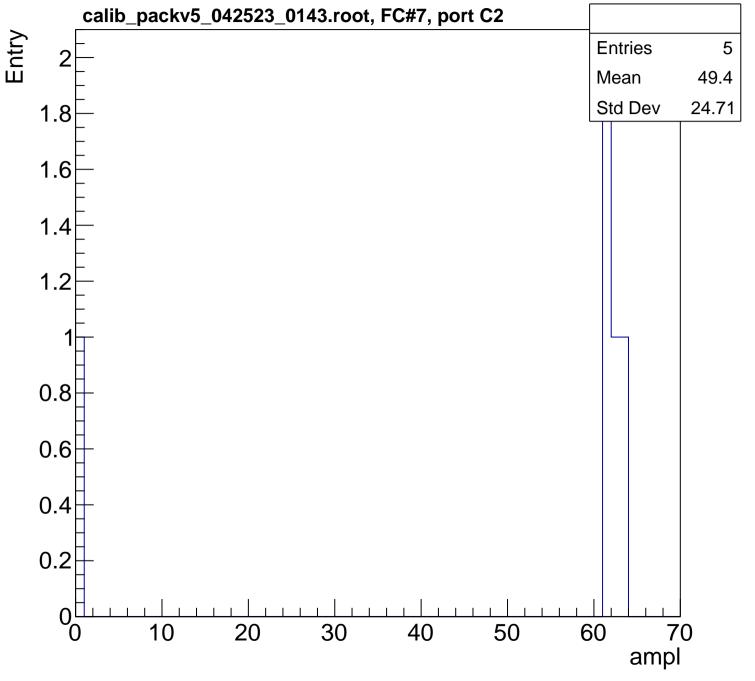


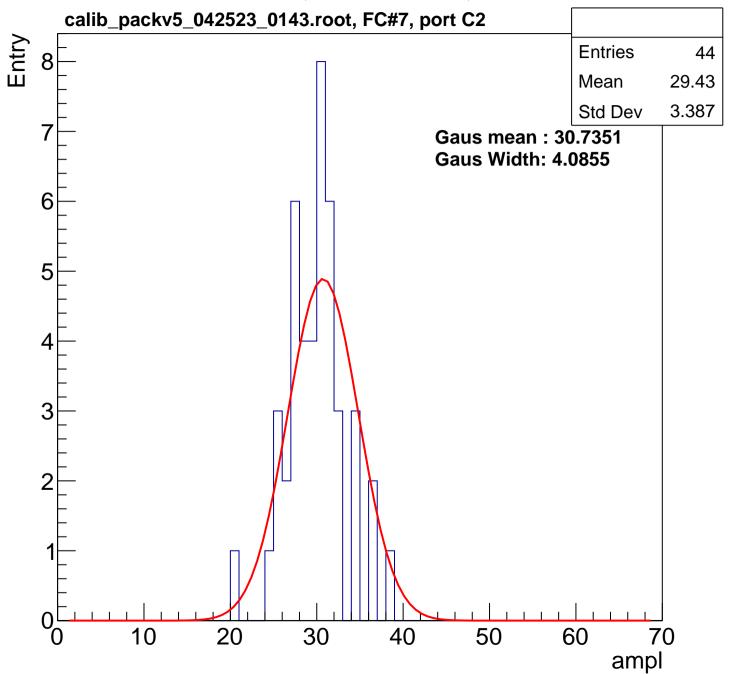


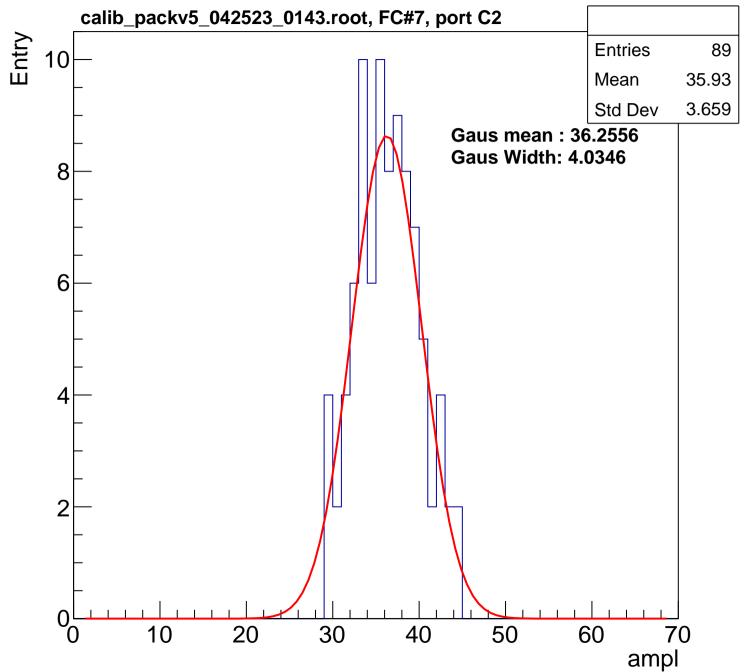


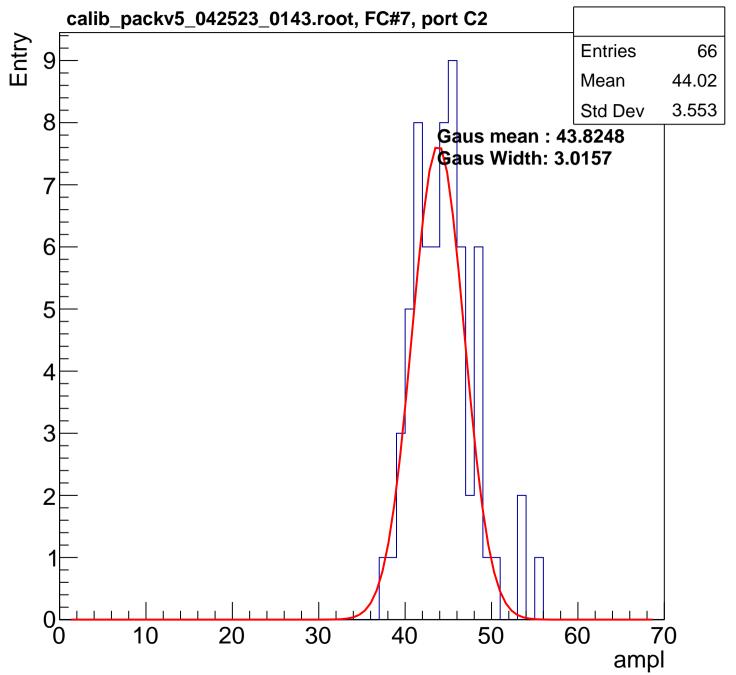


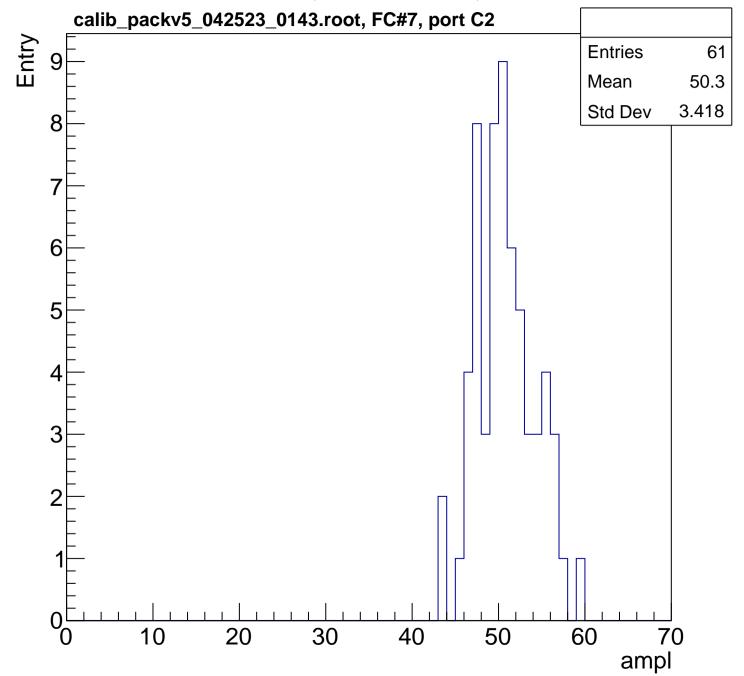


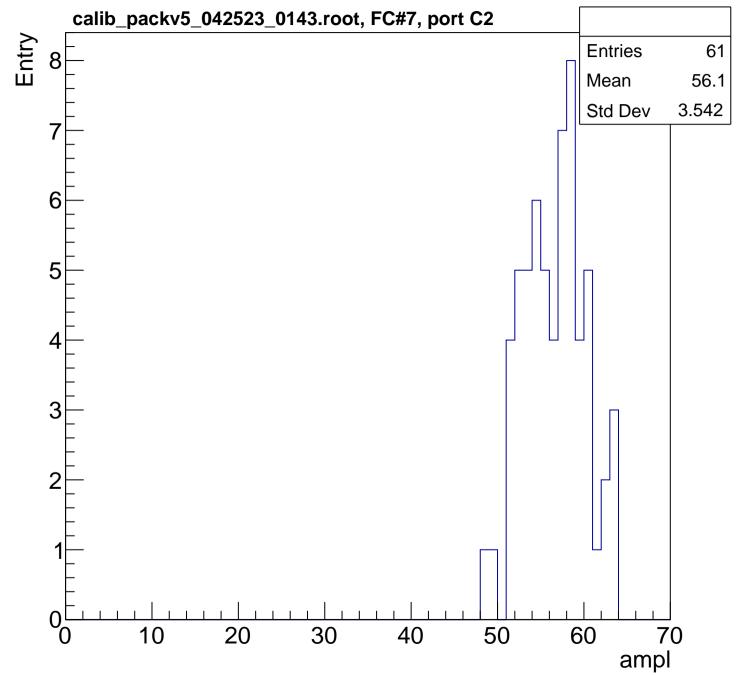


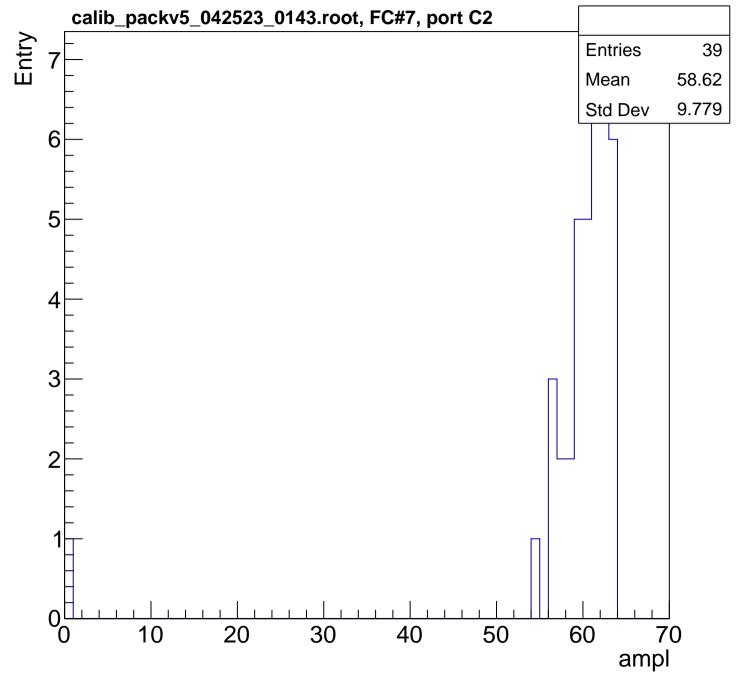


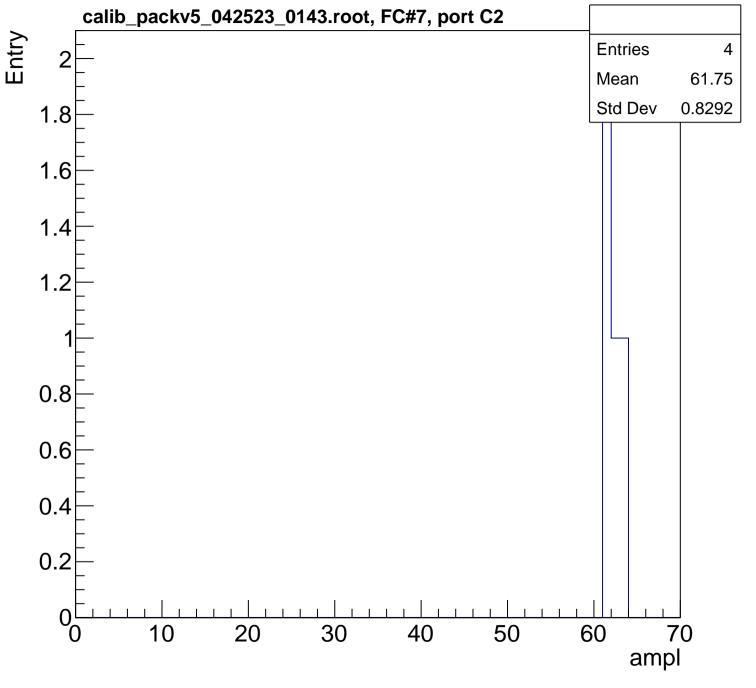




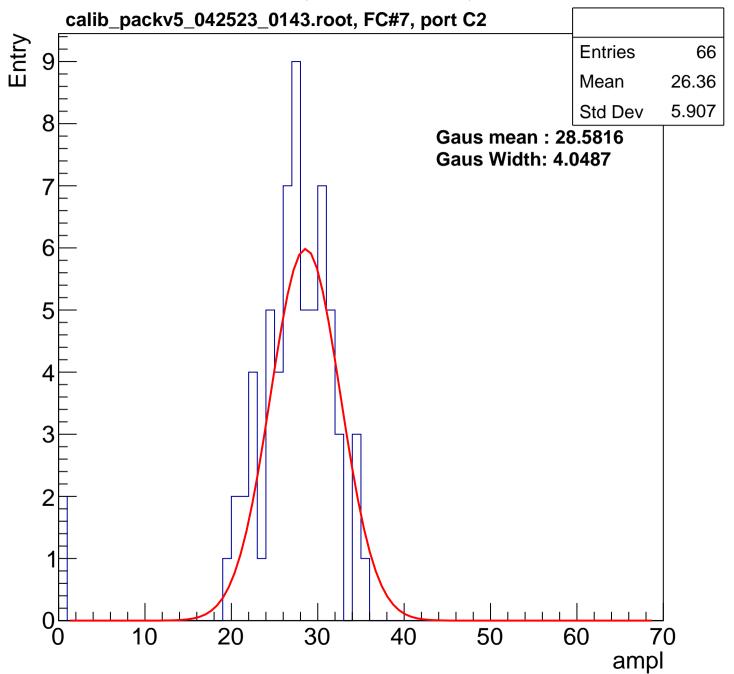


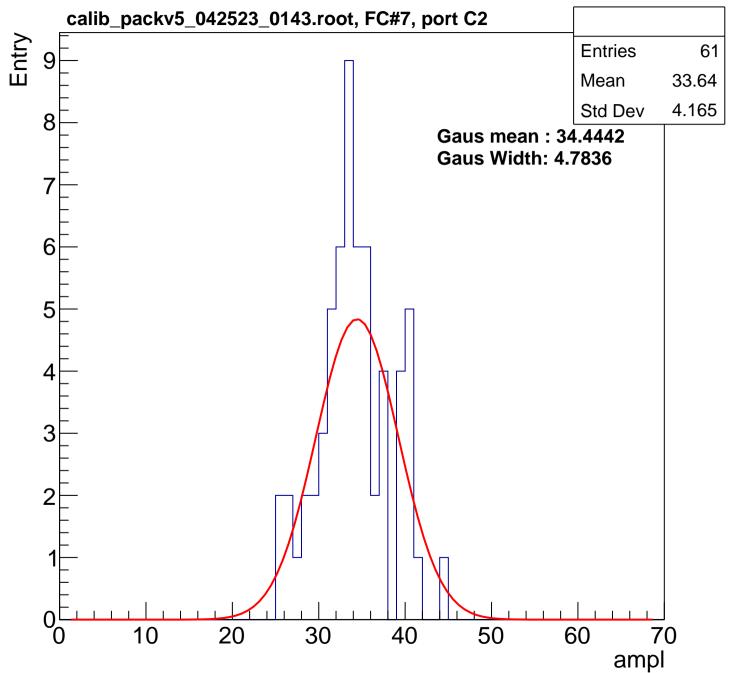


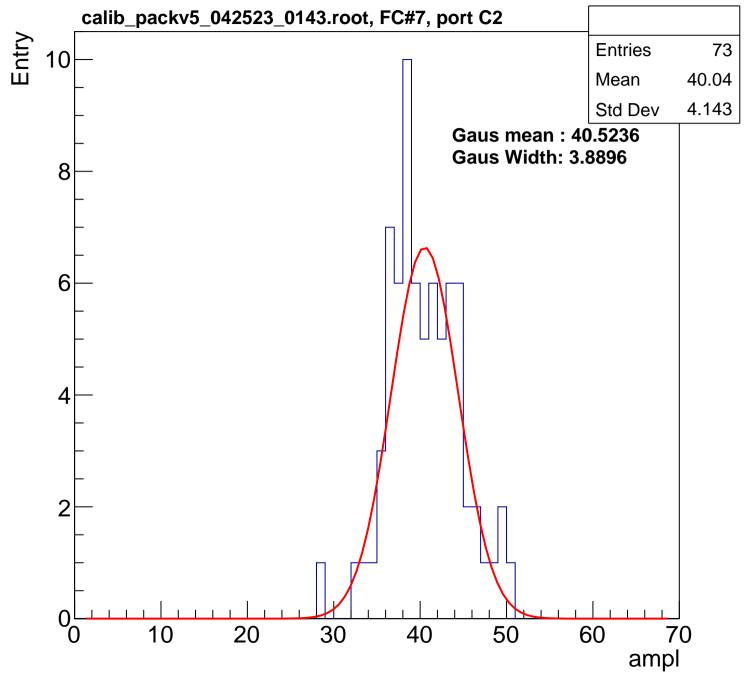


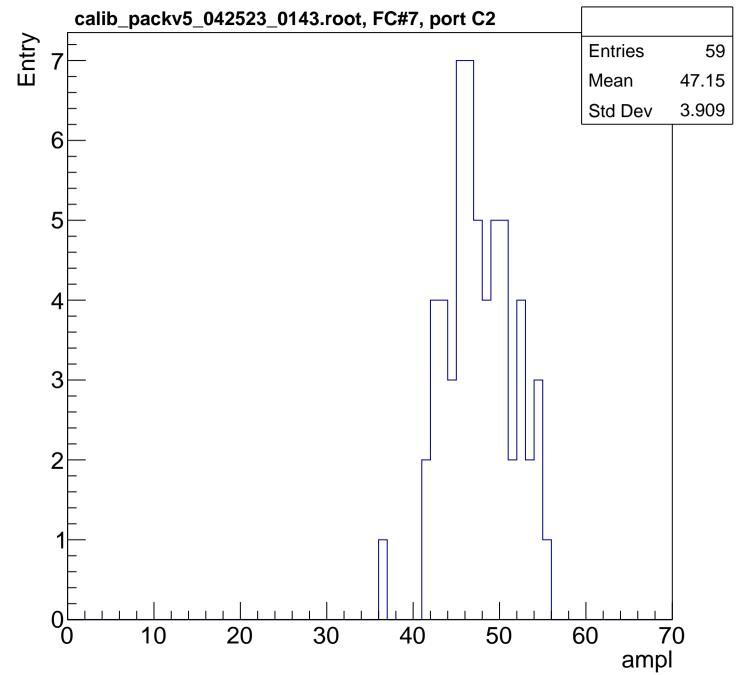


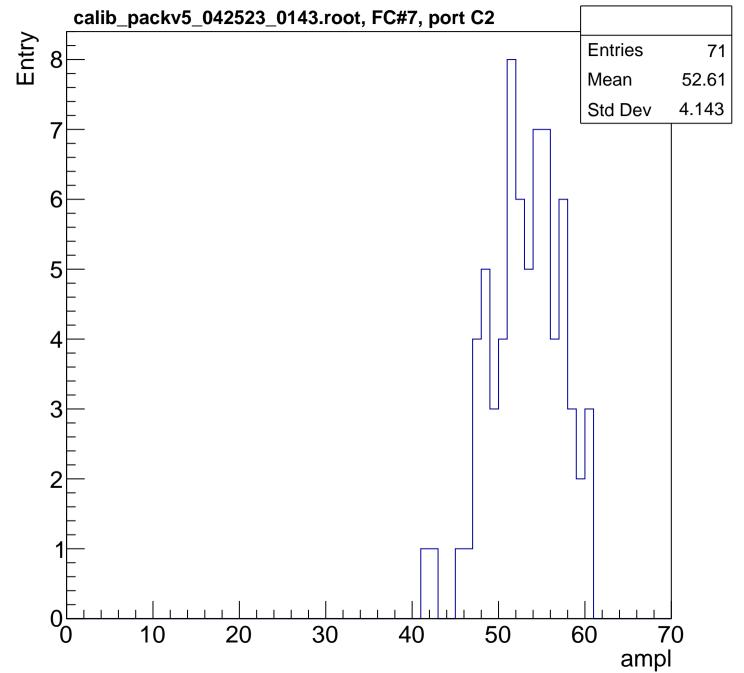


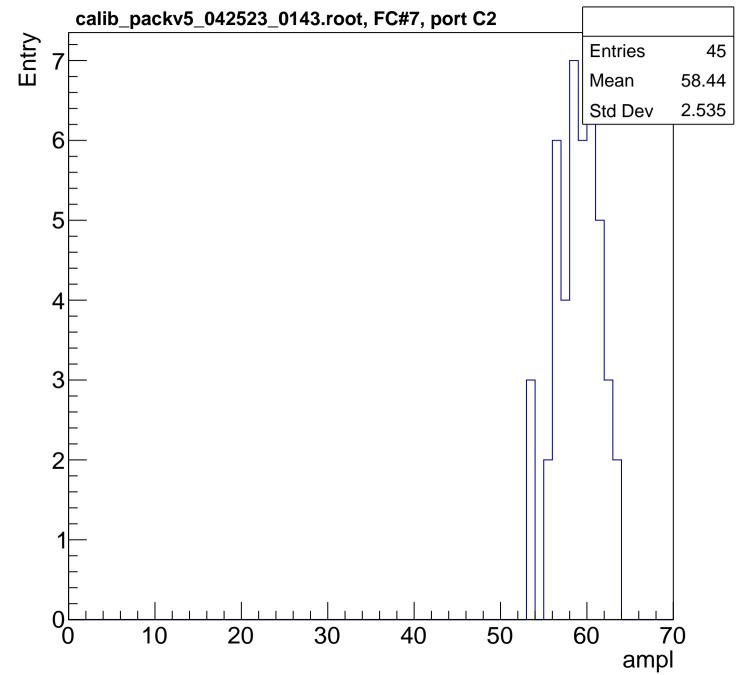


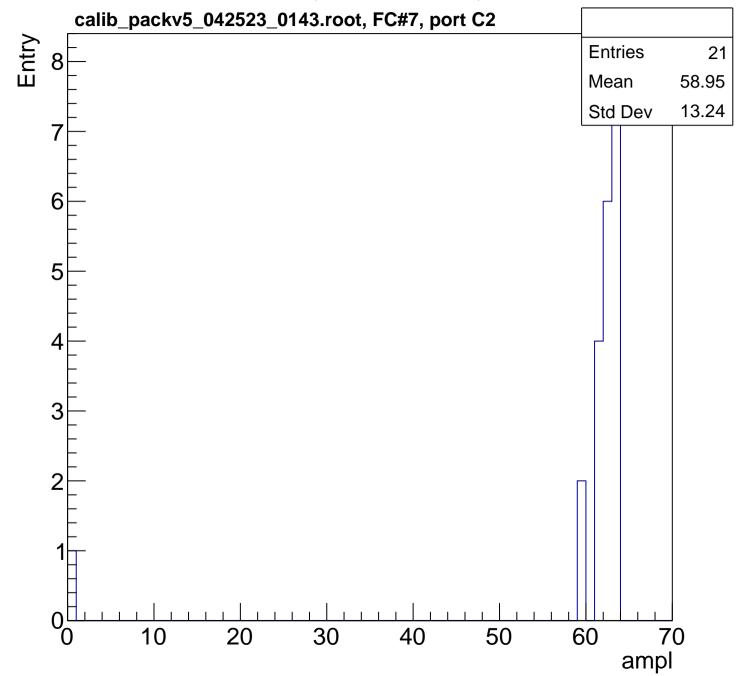


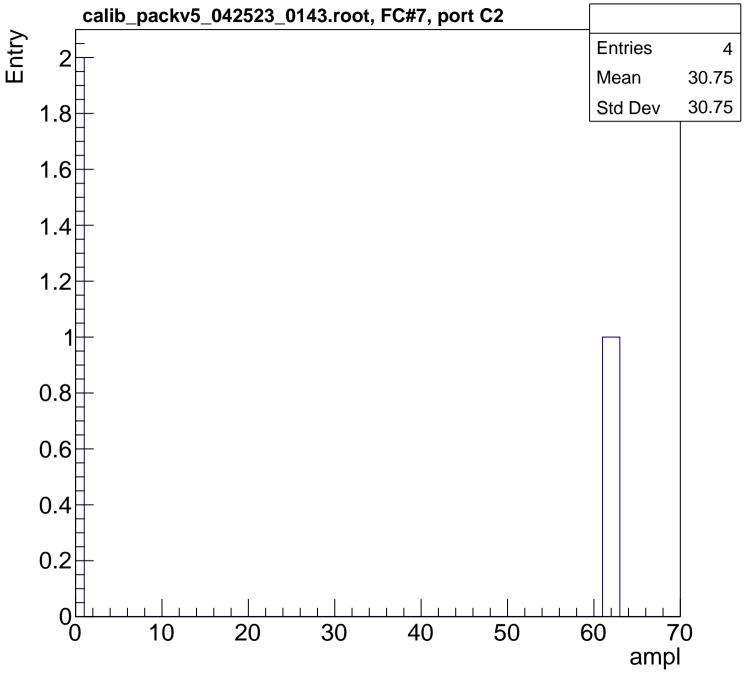


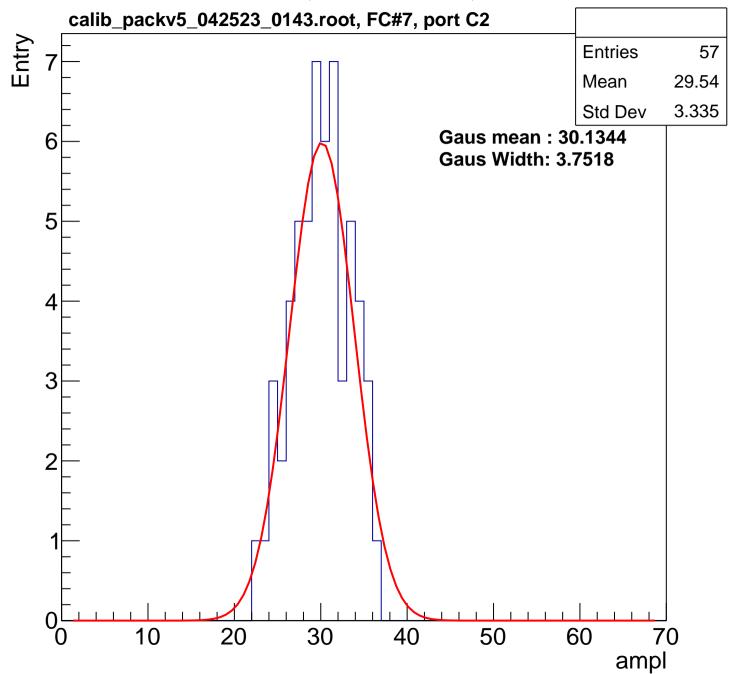


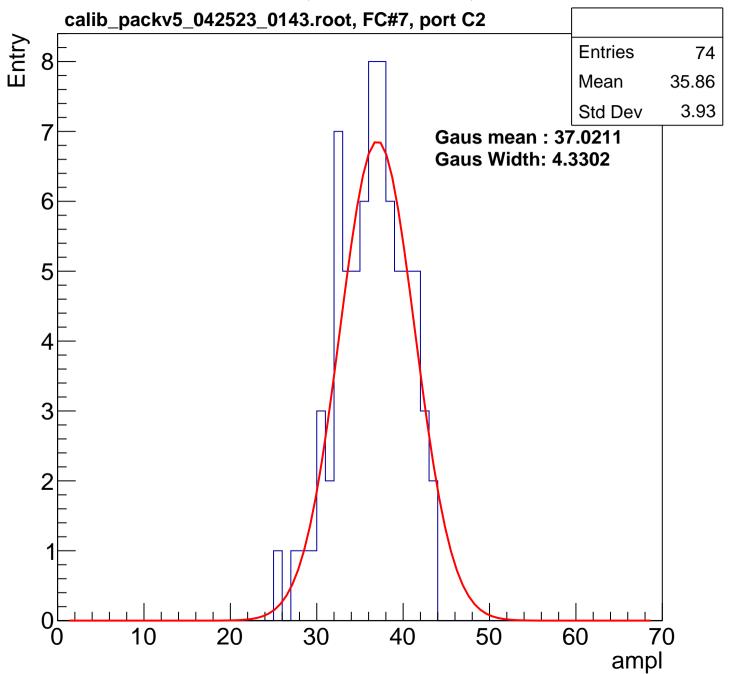


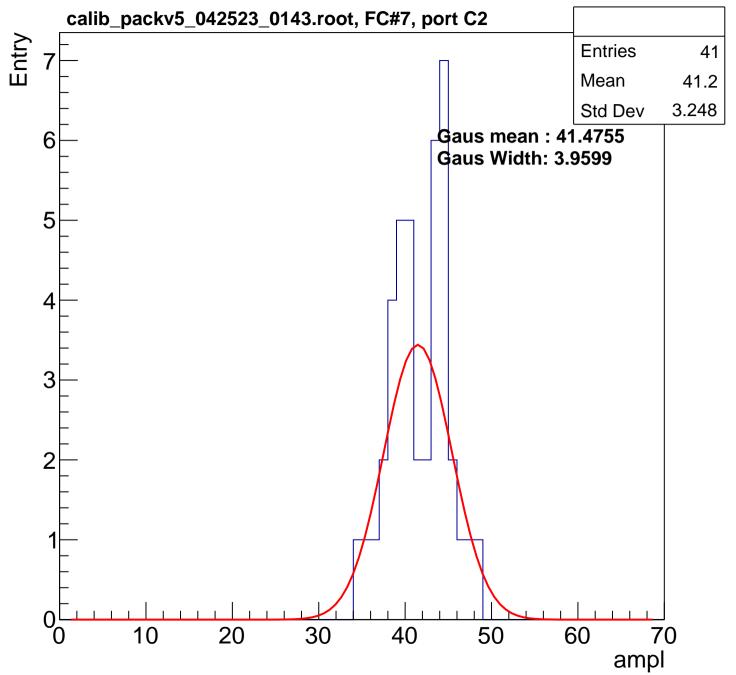


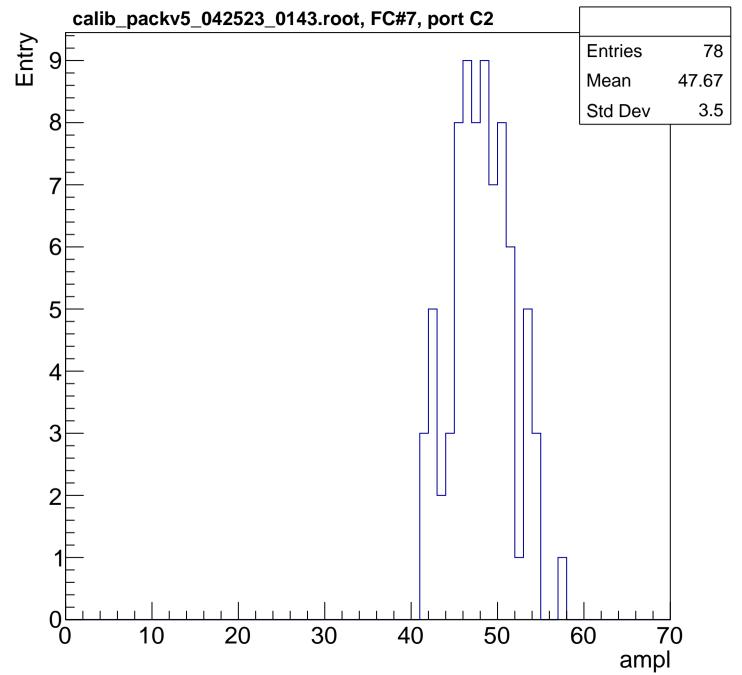




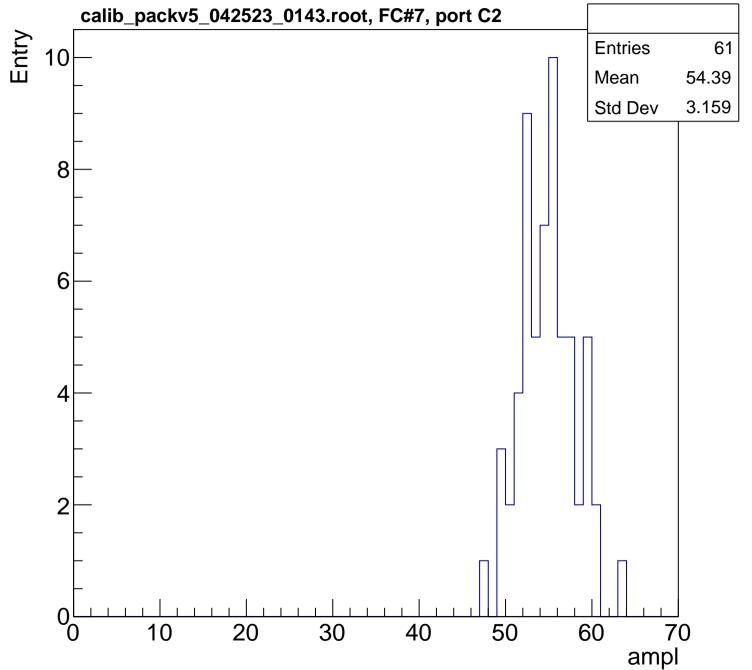


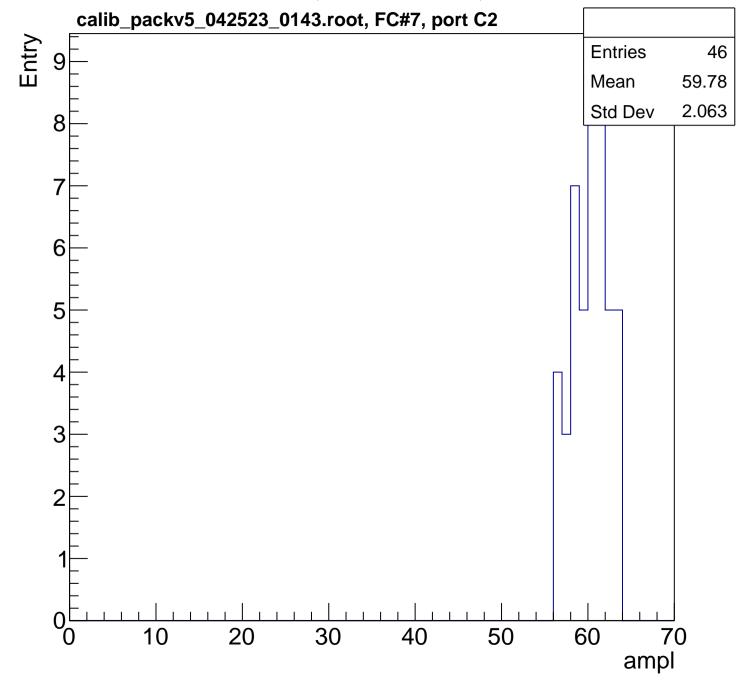


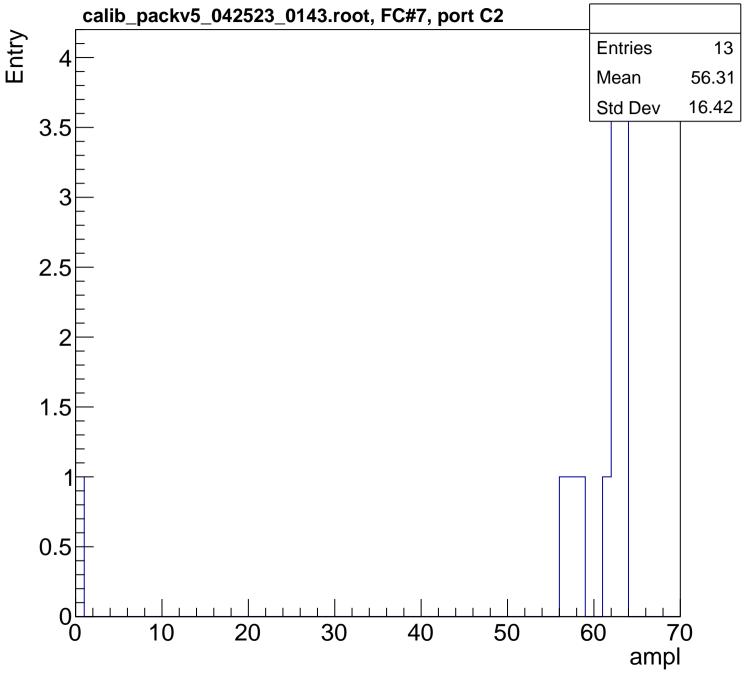


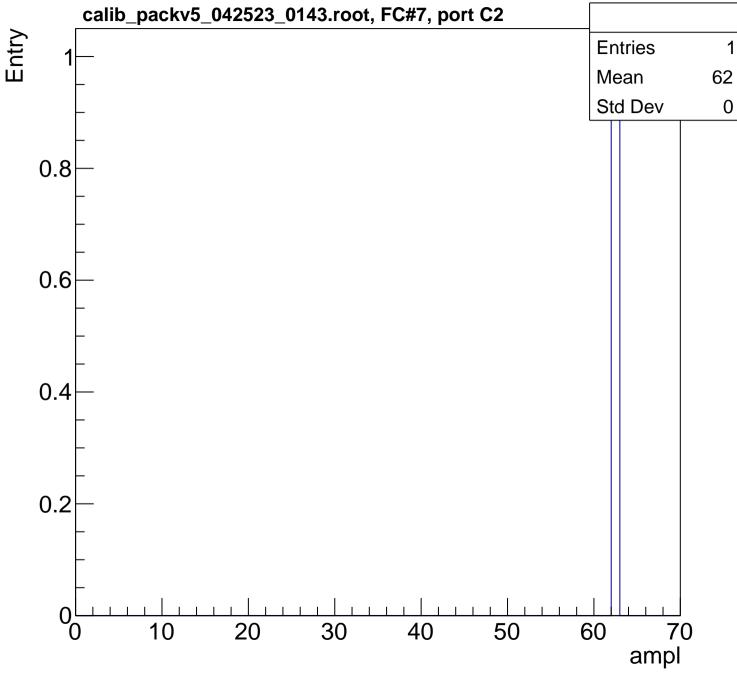


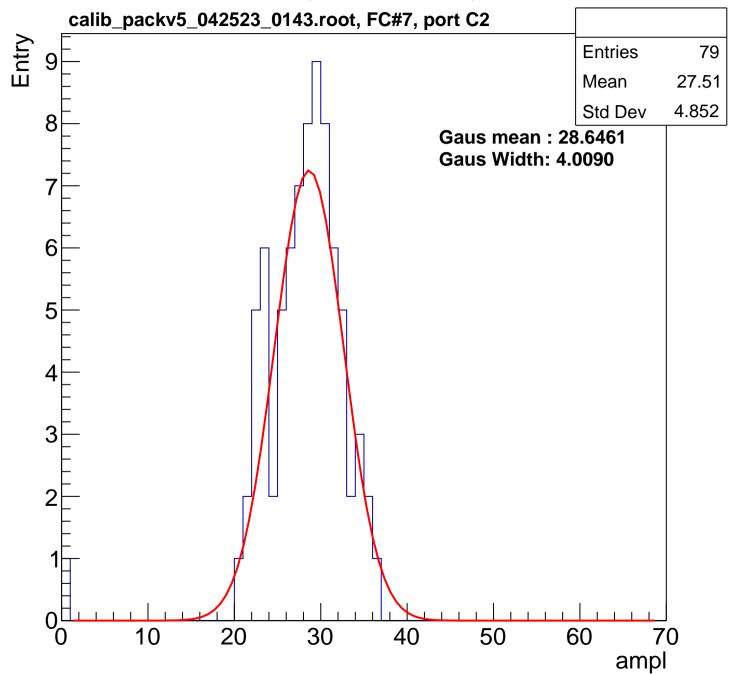
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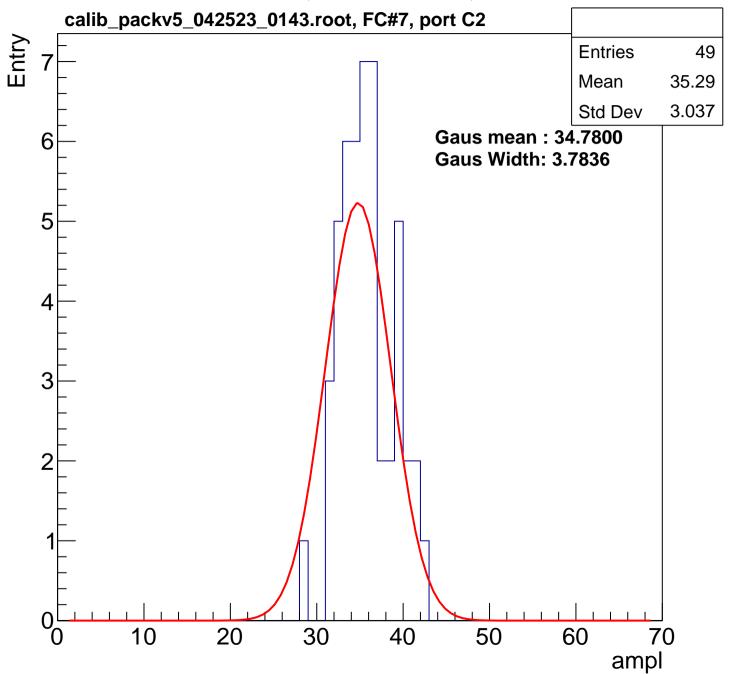


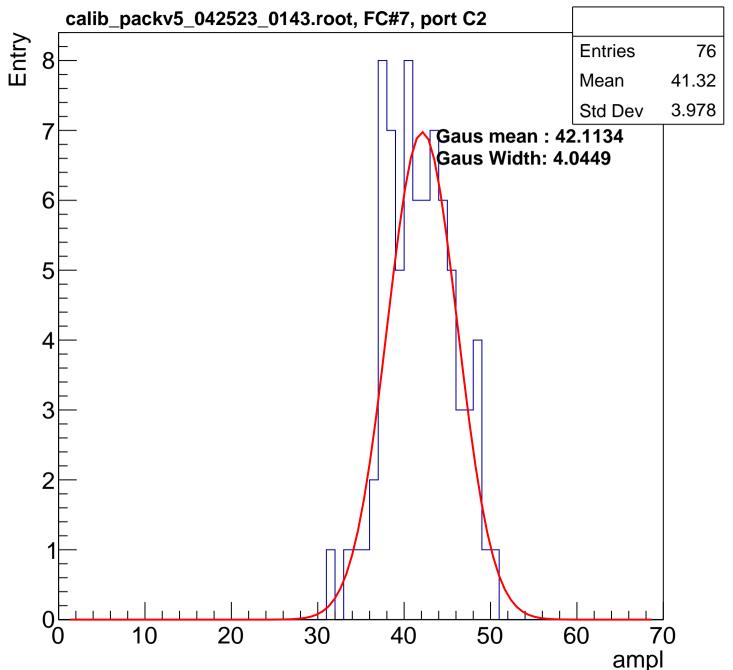


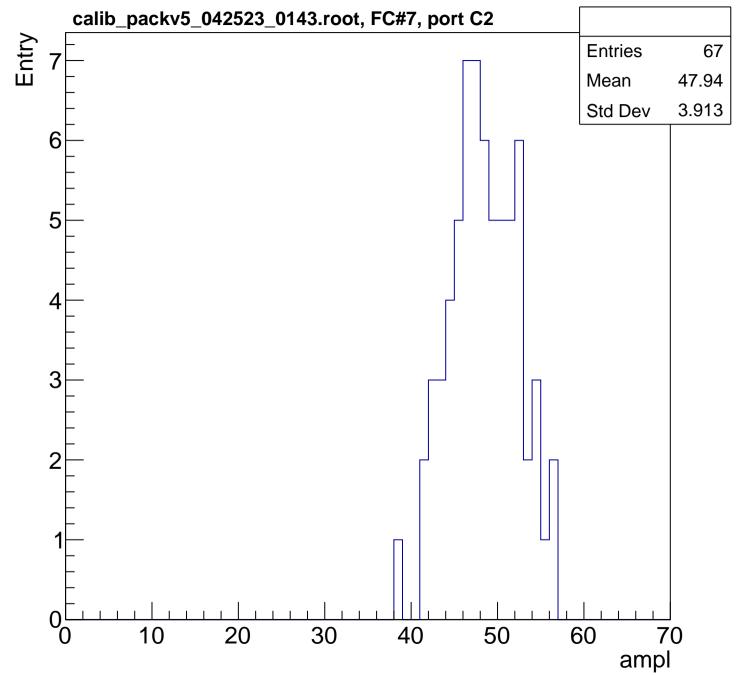


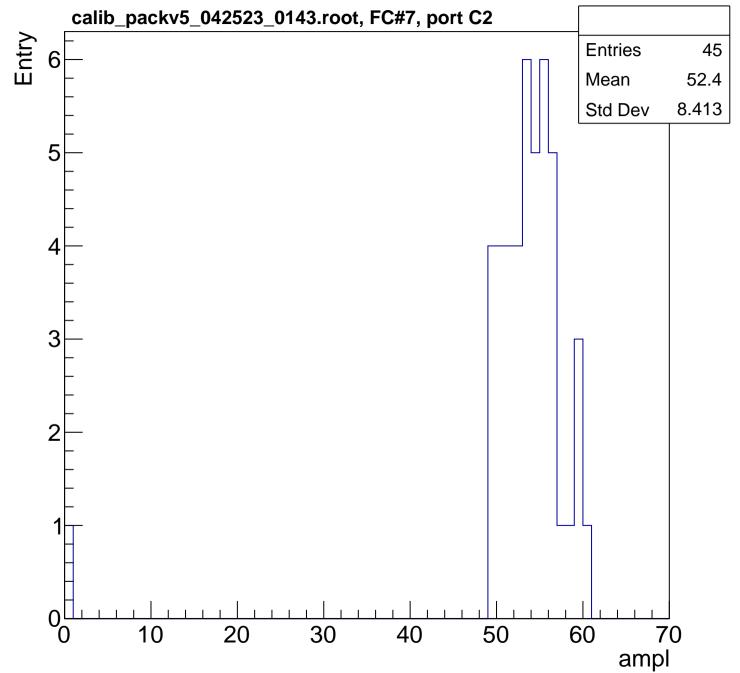


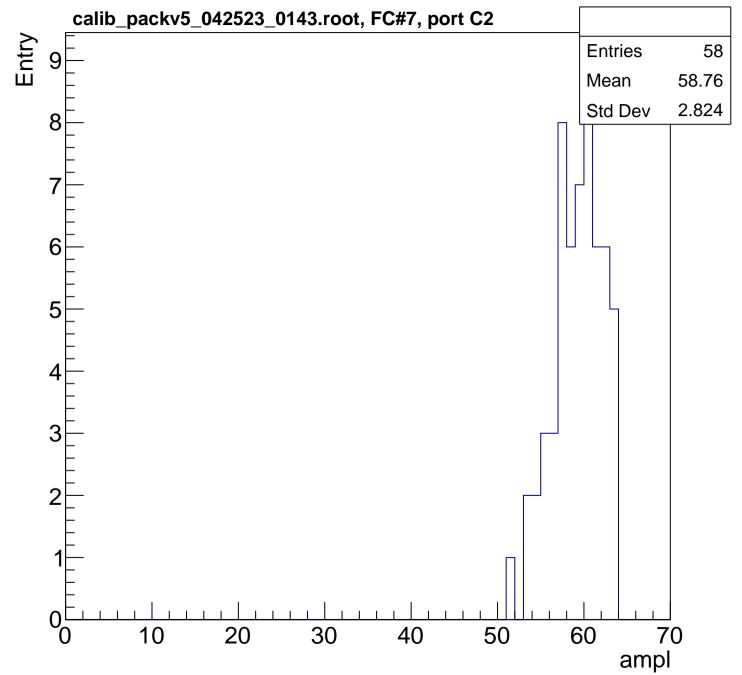


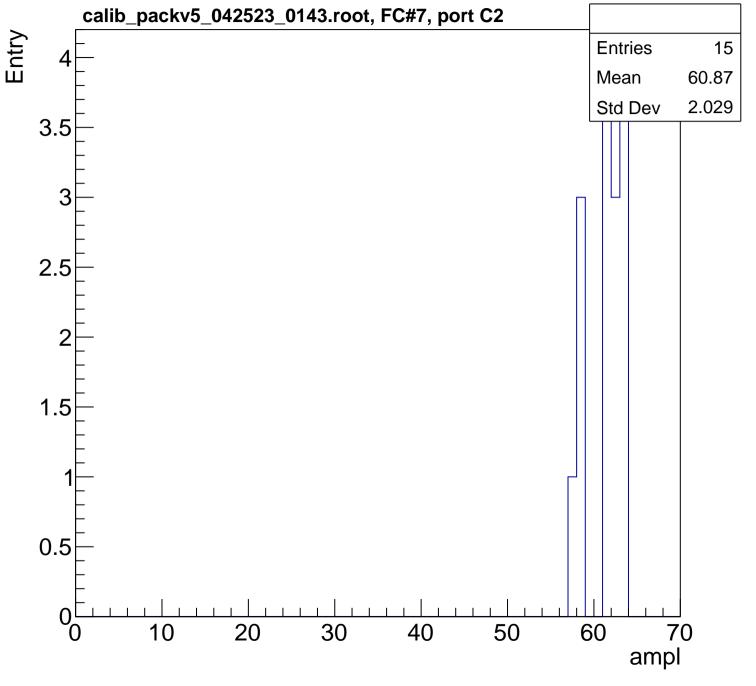


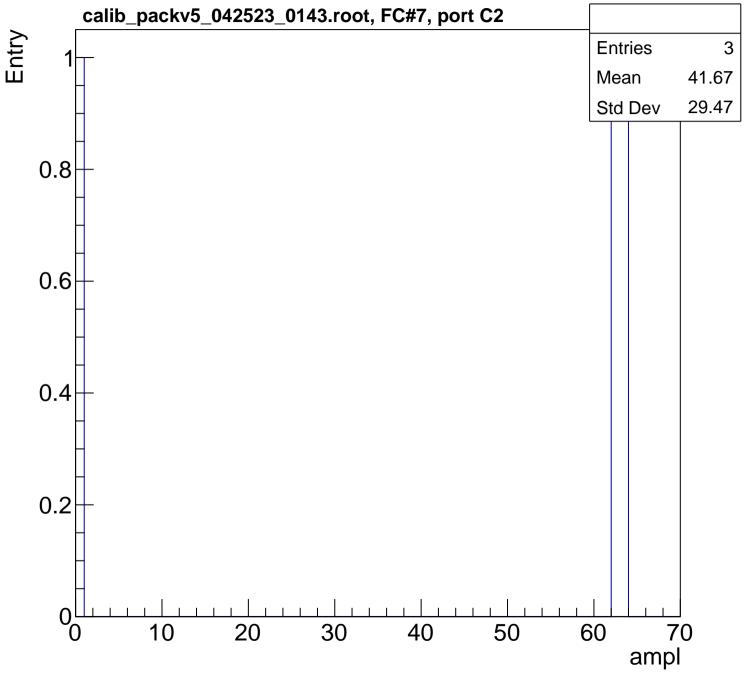


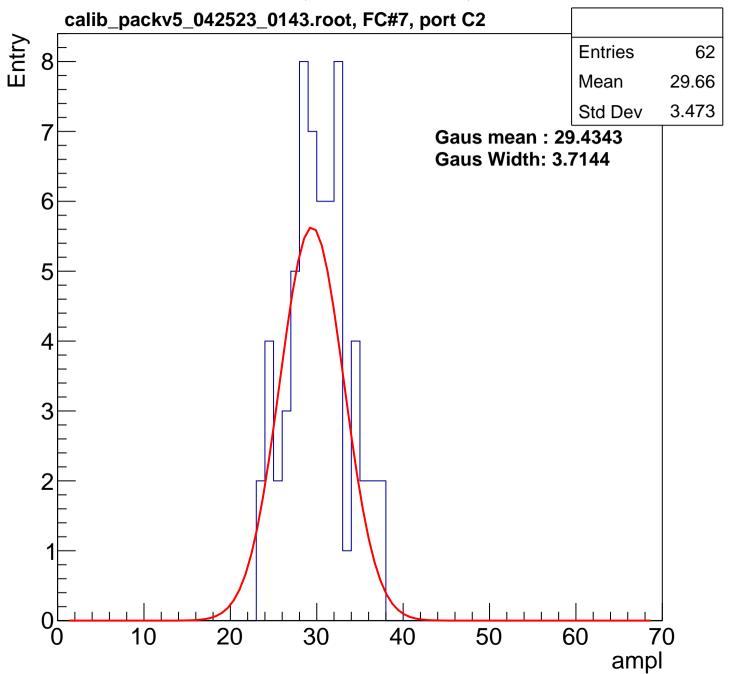


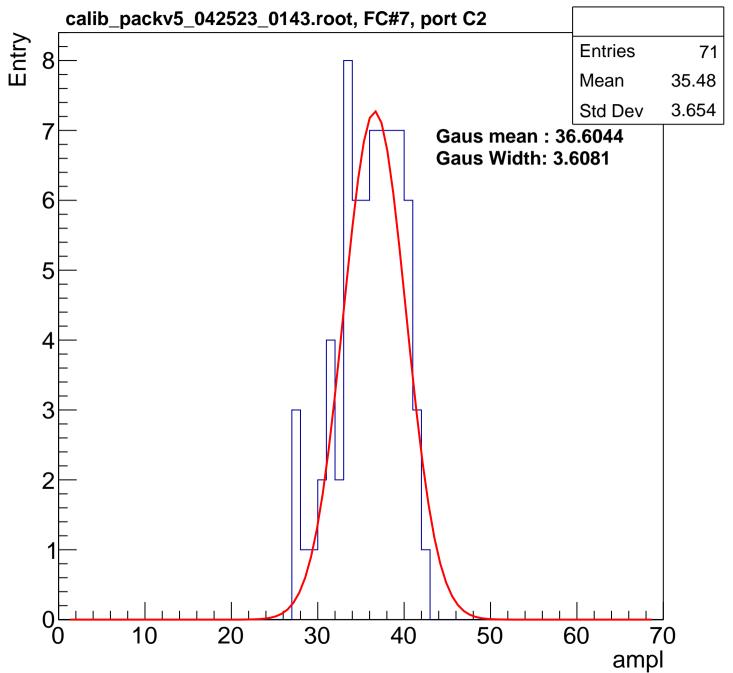


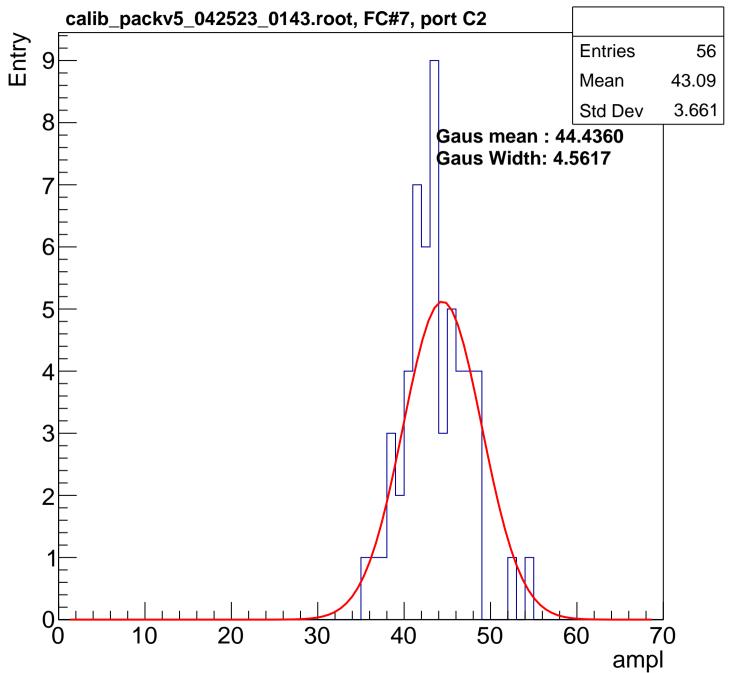


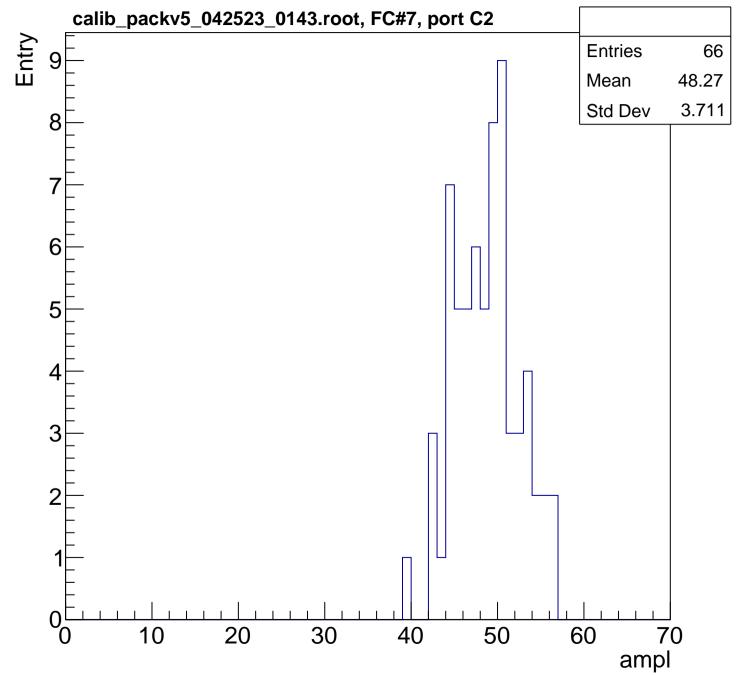


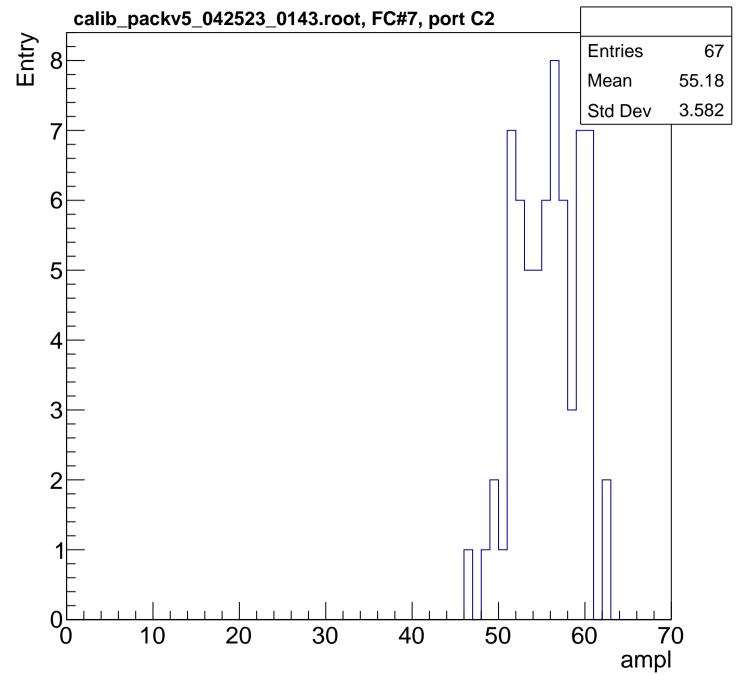


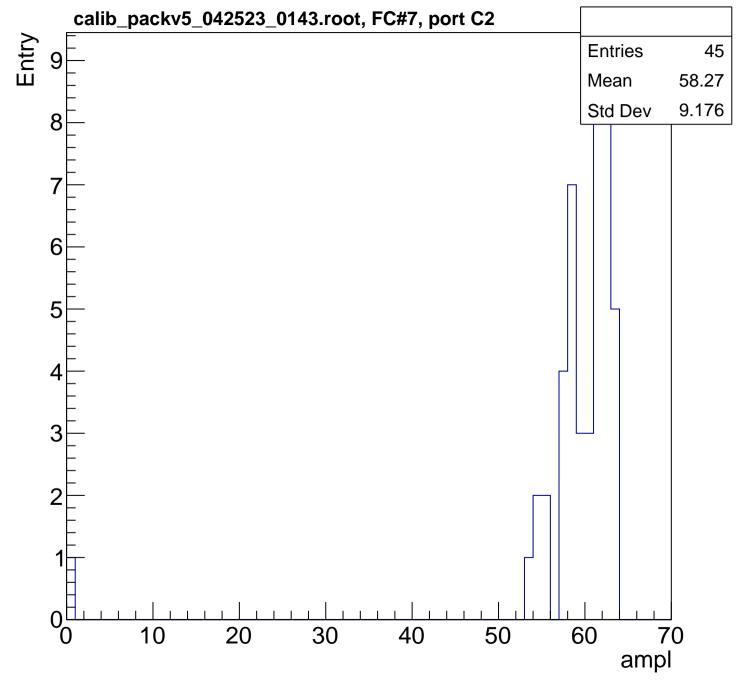


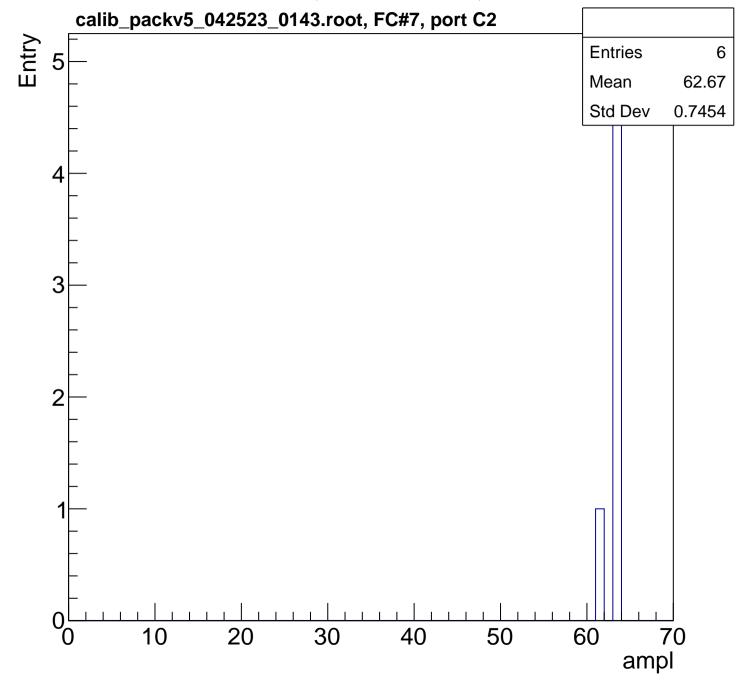


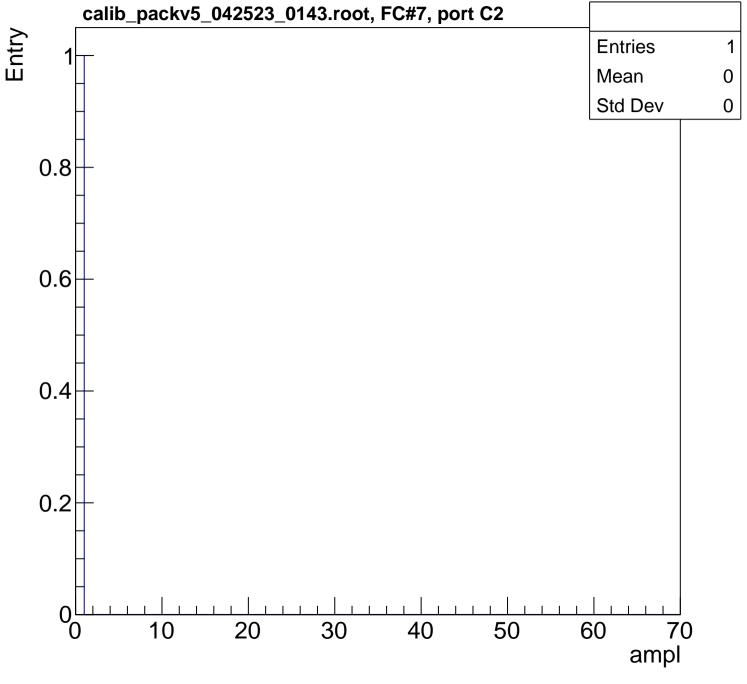


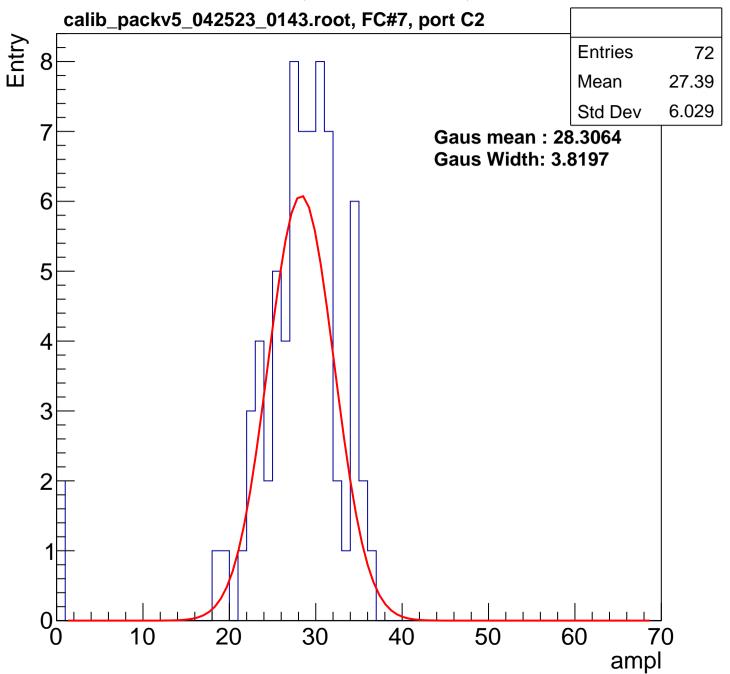


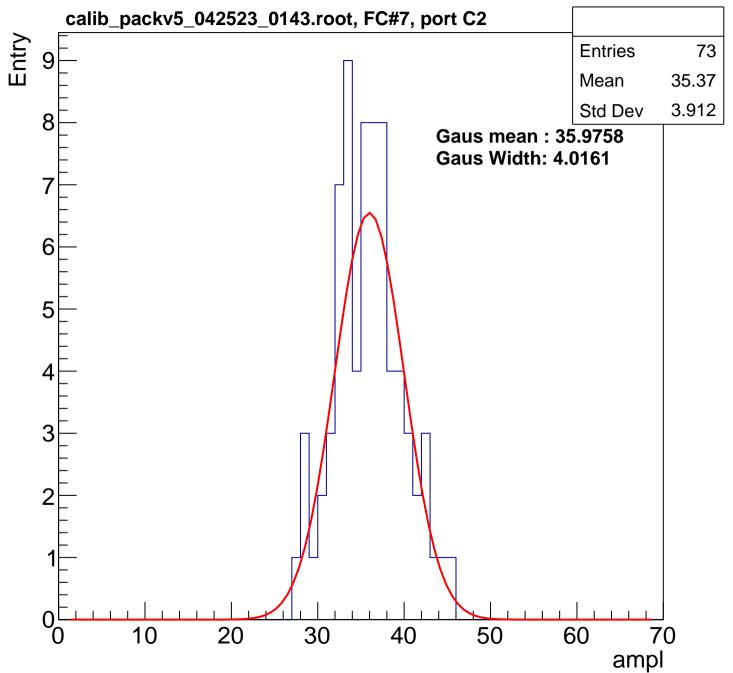


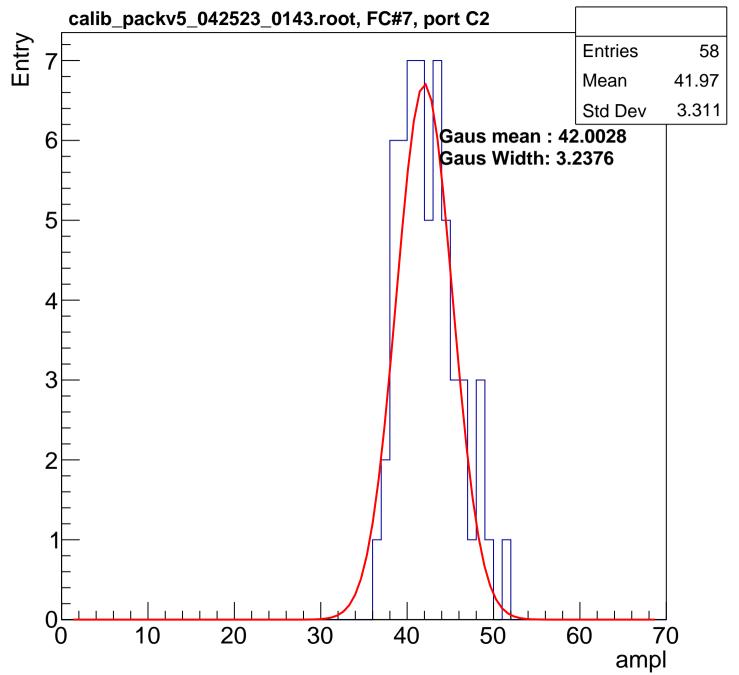


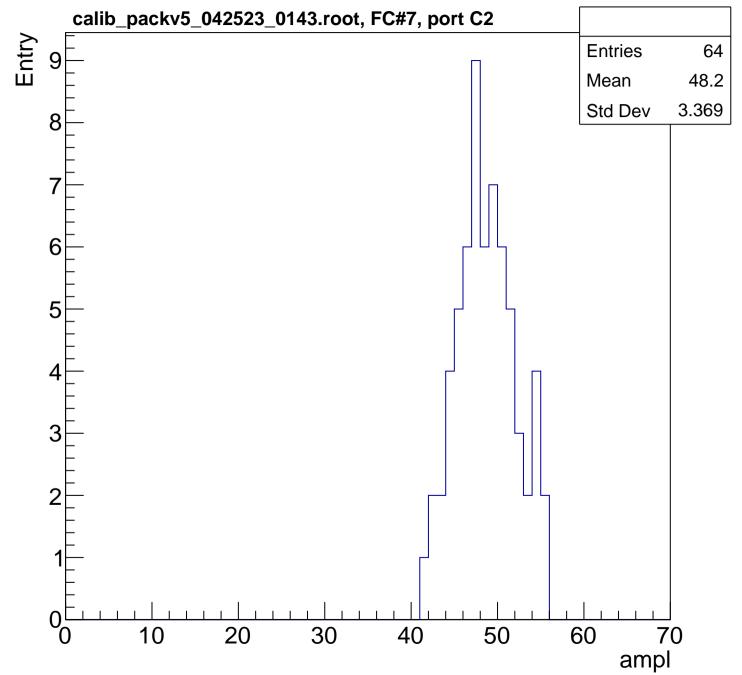


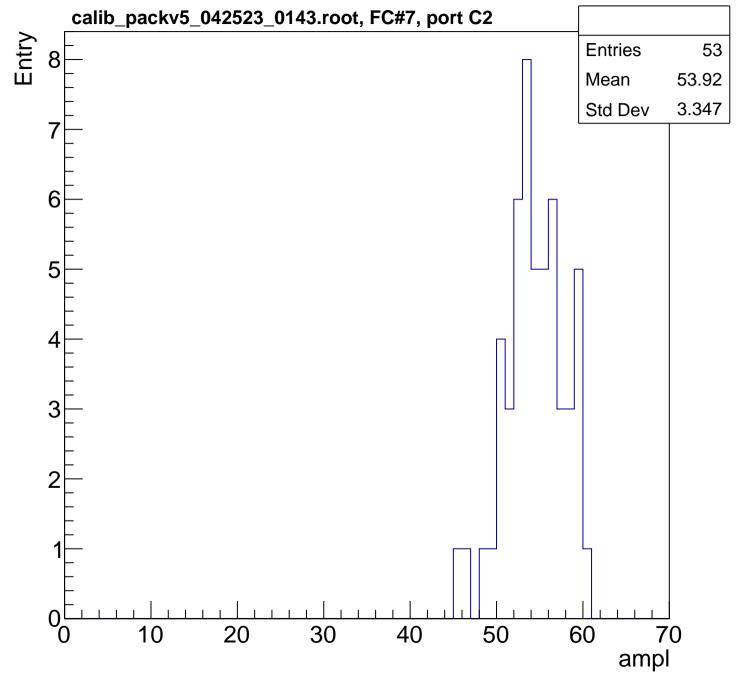


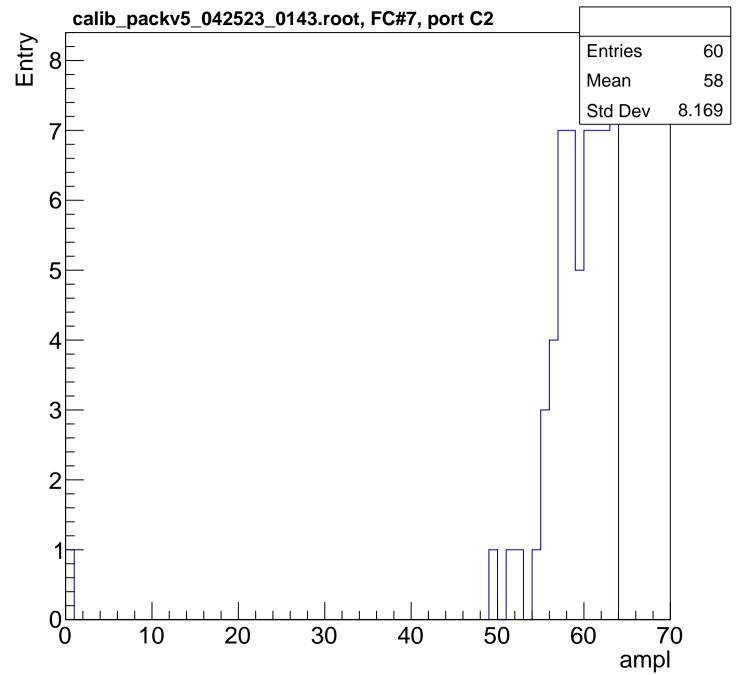


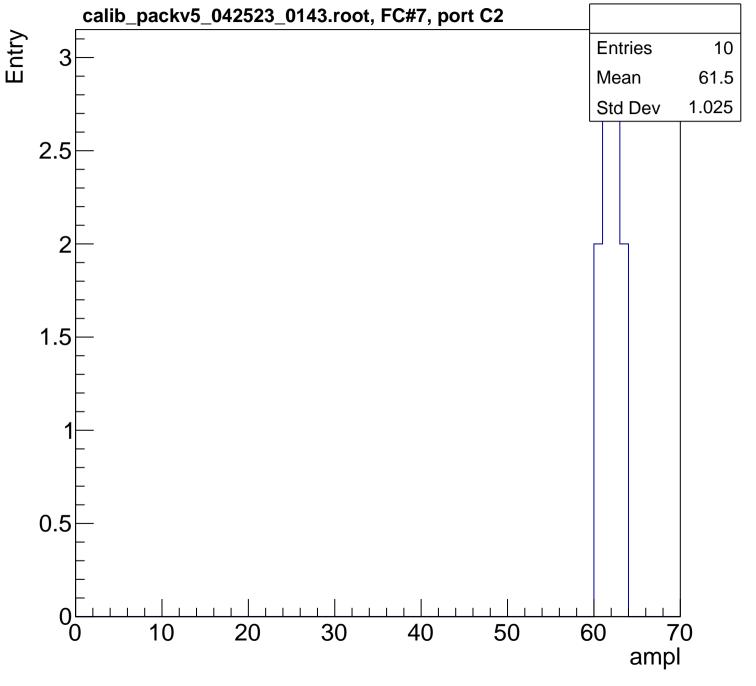


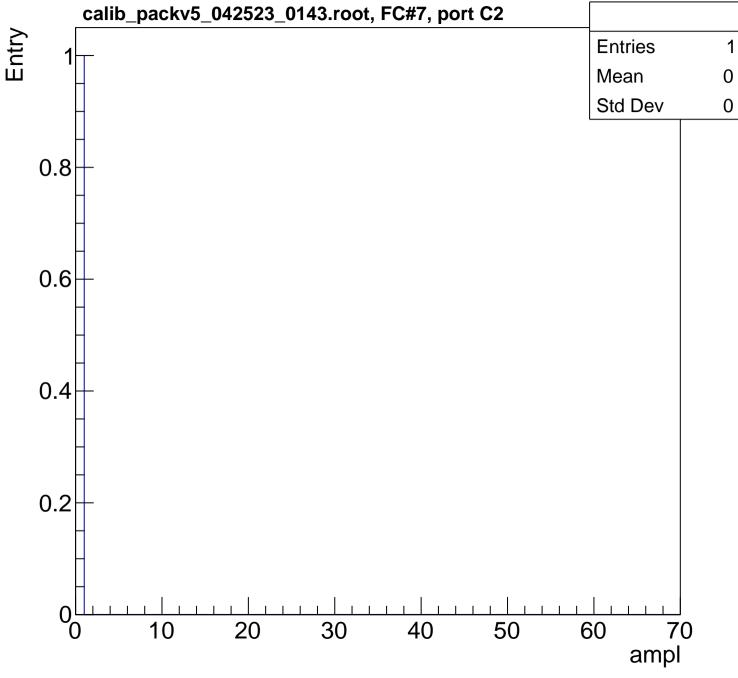


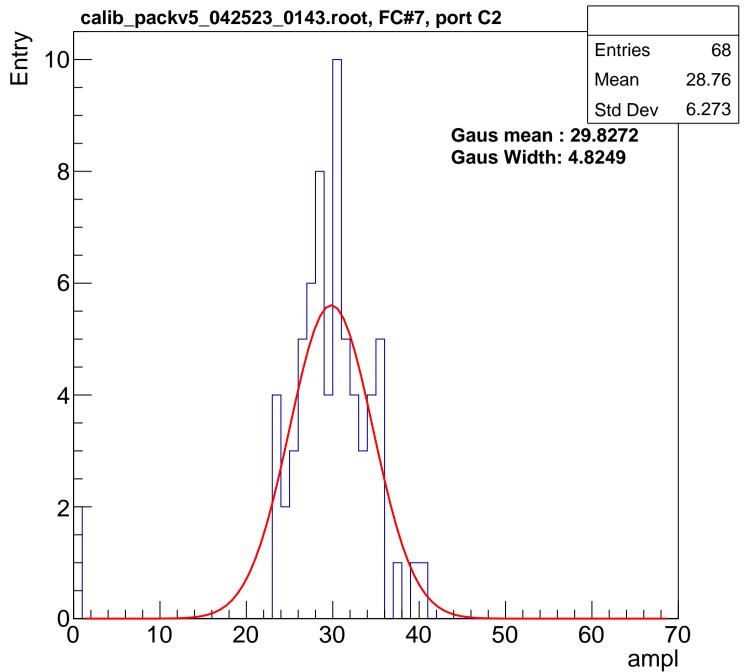


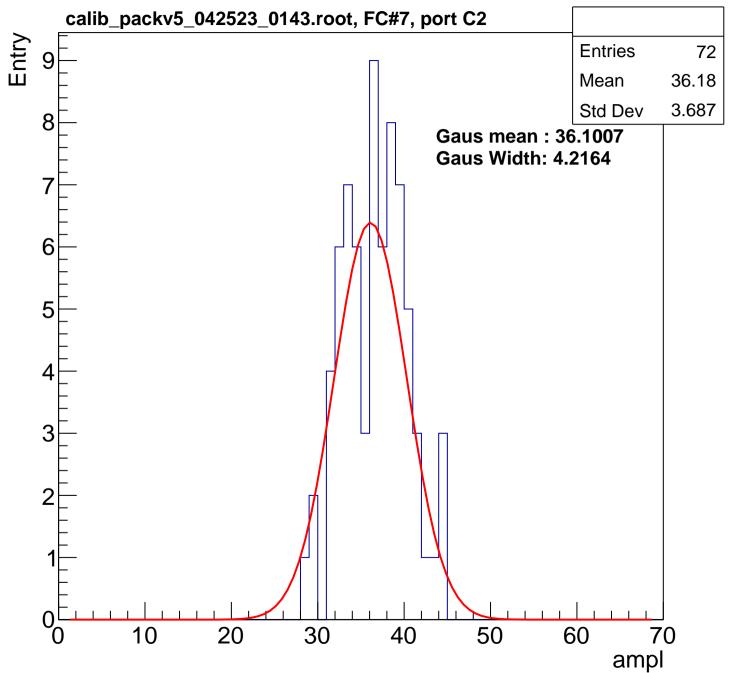


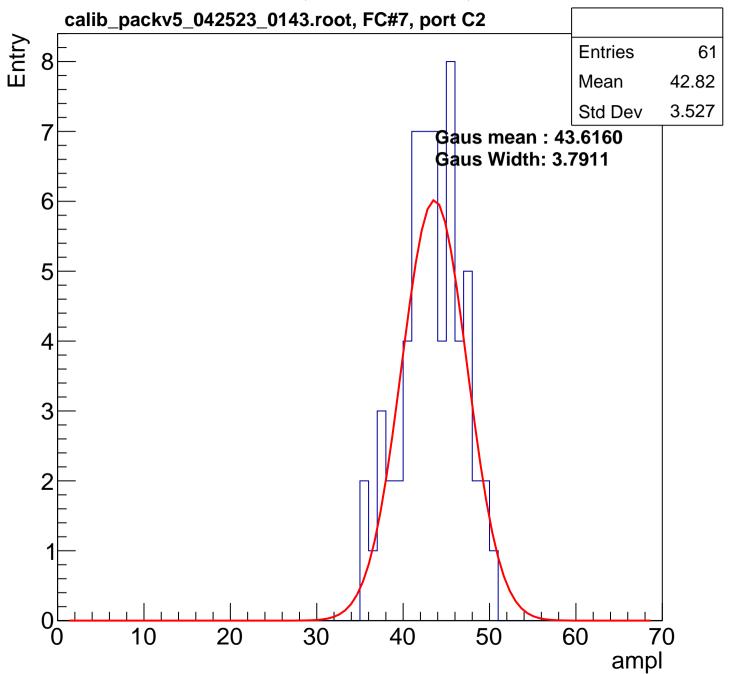


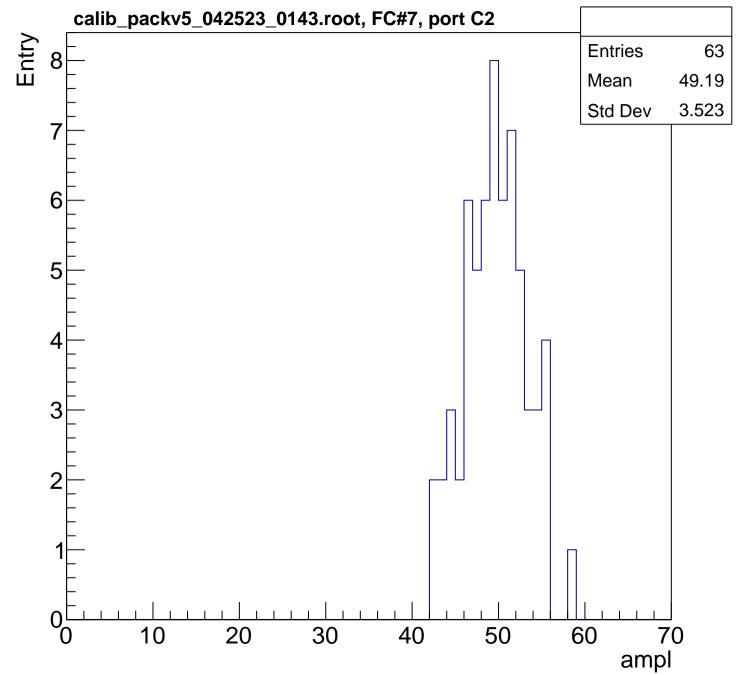












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