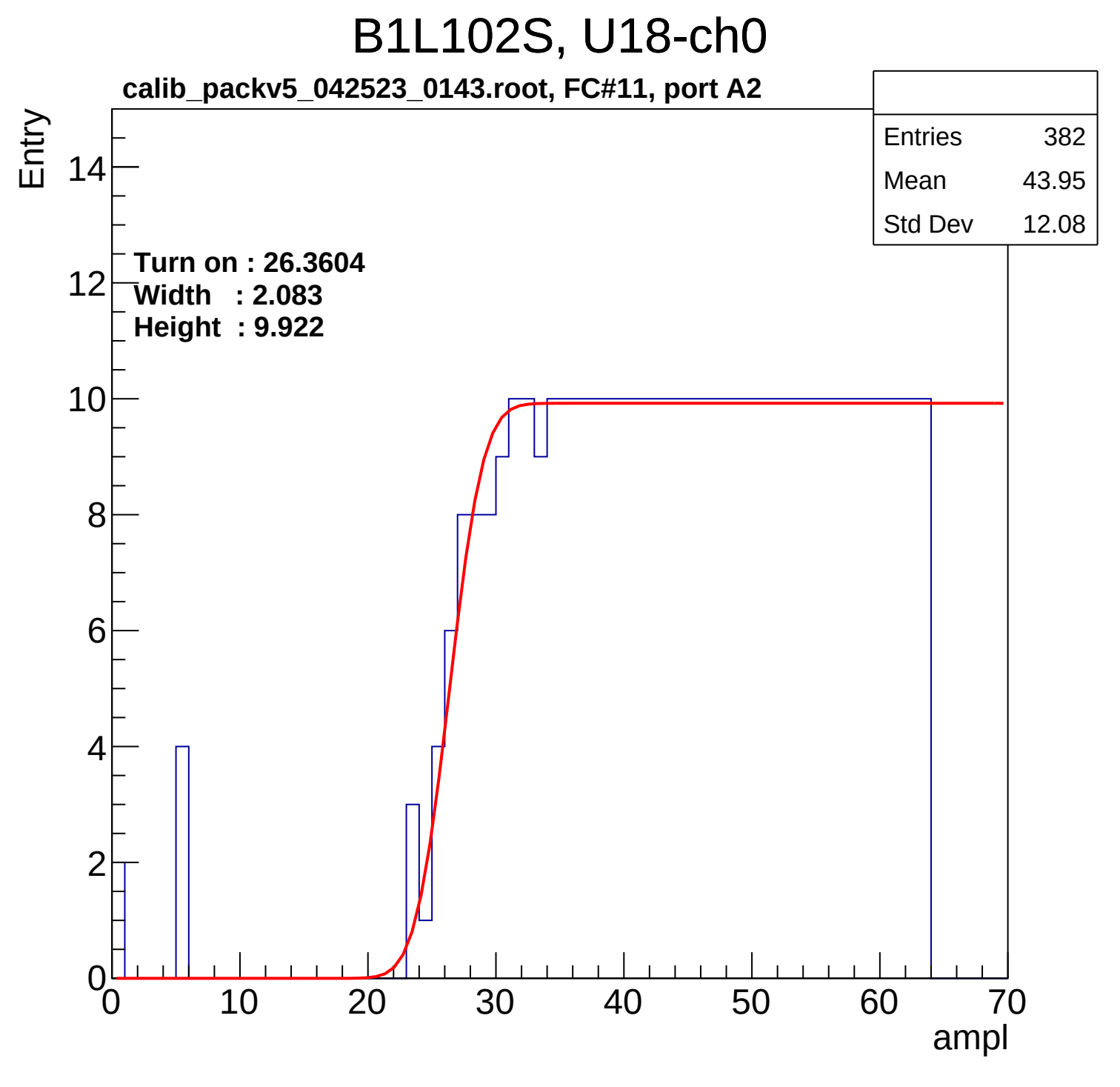
B1L102S, U18-ch0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 43.95
Std Dev 12.08
Turn on : 26.3604
Width : 2.083
Height : 9.922
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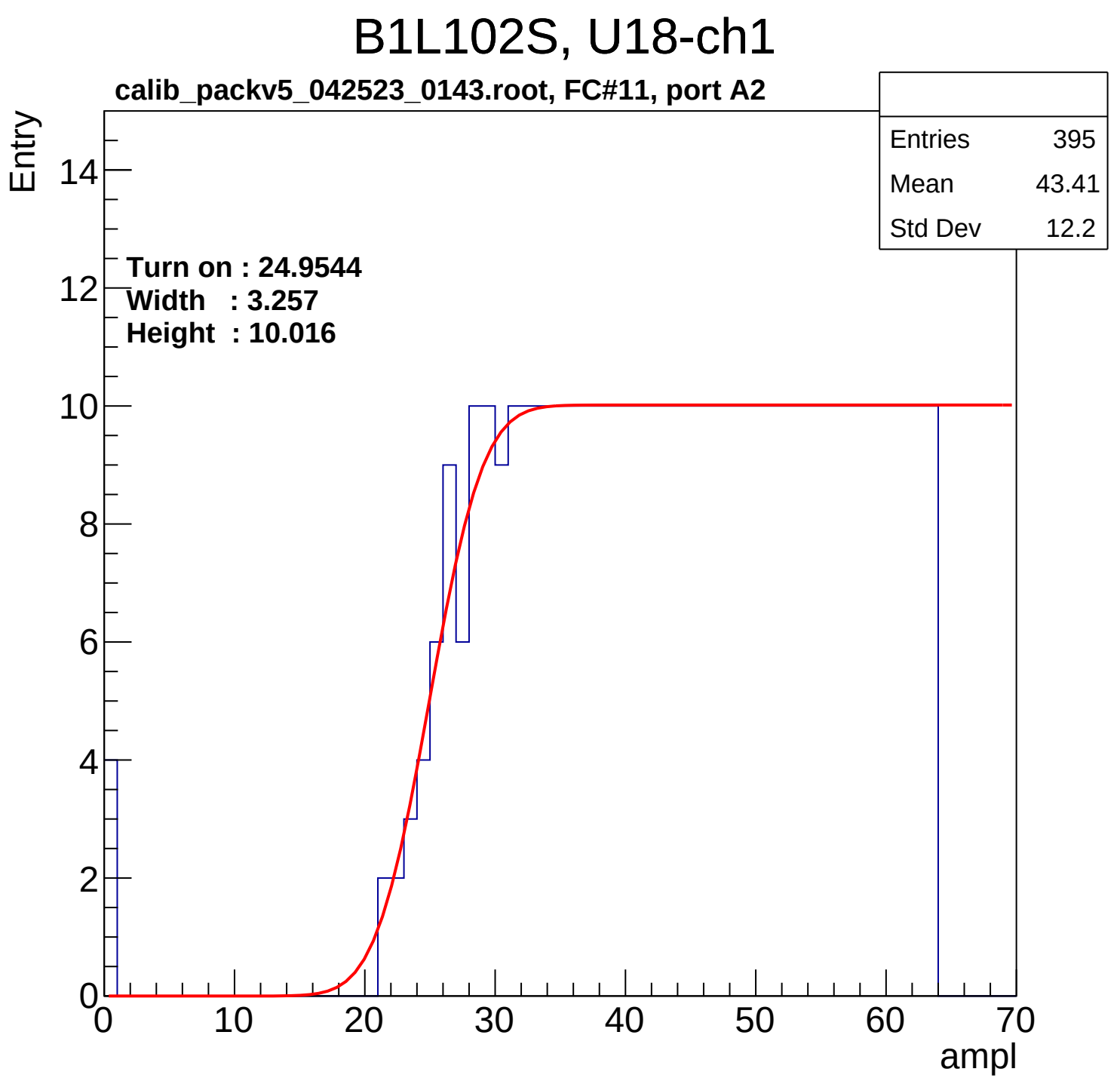
B1L102S, U18-ch1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 395
Mean 43.41
Std Dev 12.2
Turn on : 24.9544
Width : 3.257
Height : 10.016
Entry
ampl
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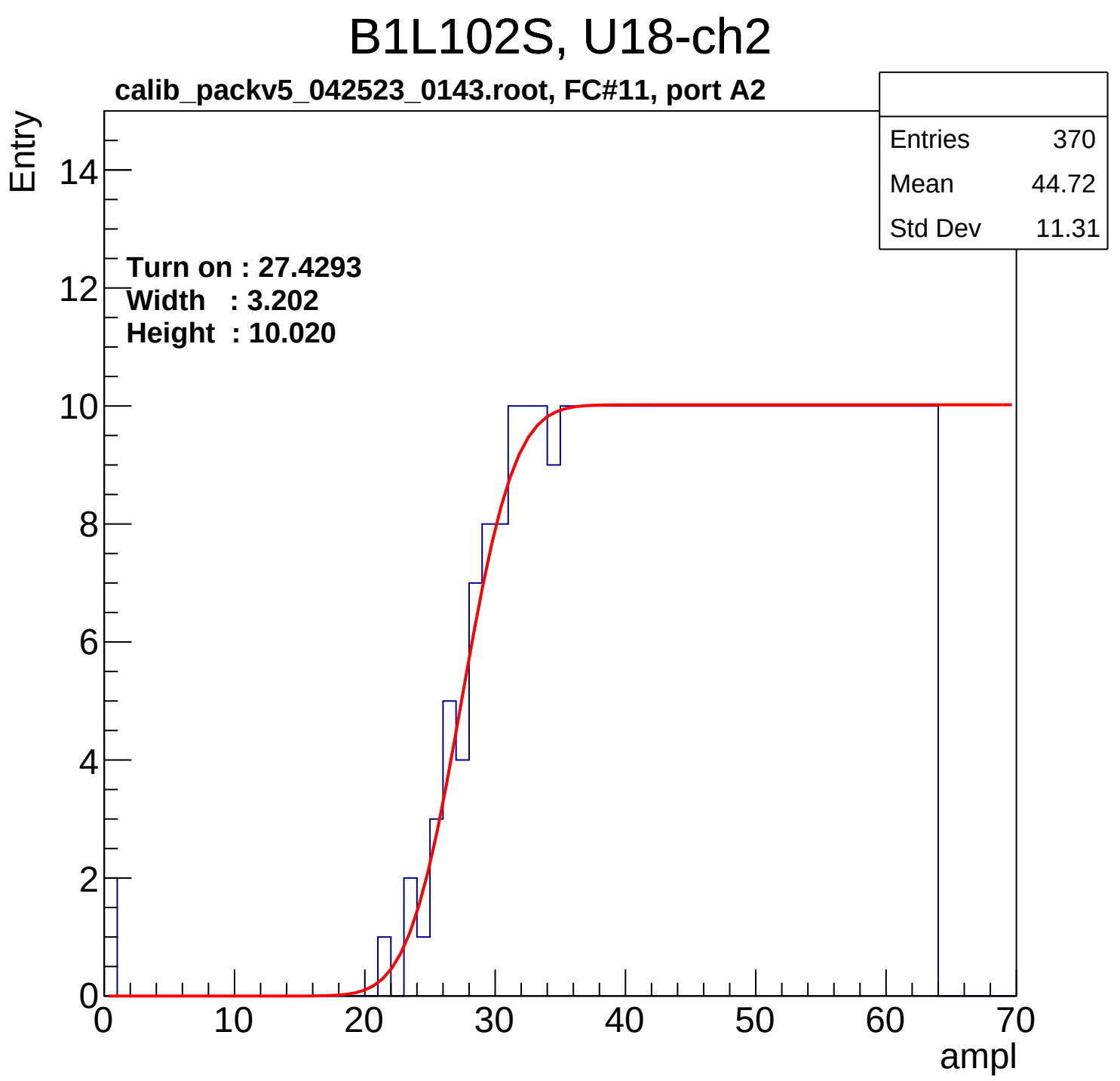
B1L102S, U18-ch2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 370
Mean 44.72
Std Dev 11.31
Turn on : 27.4293
Width : 3.202
Height : 10.020
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ampl
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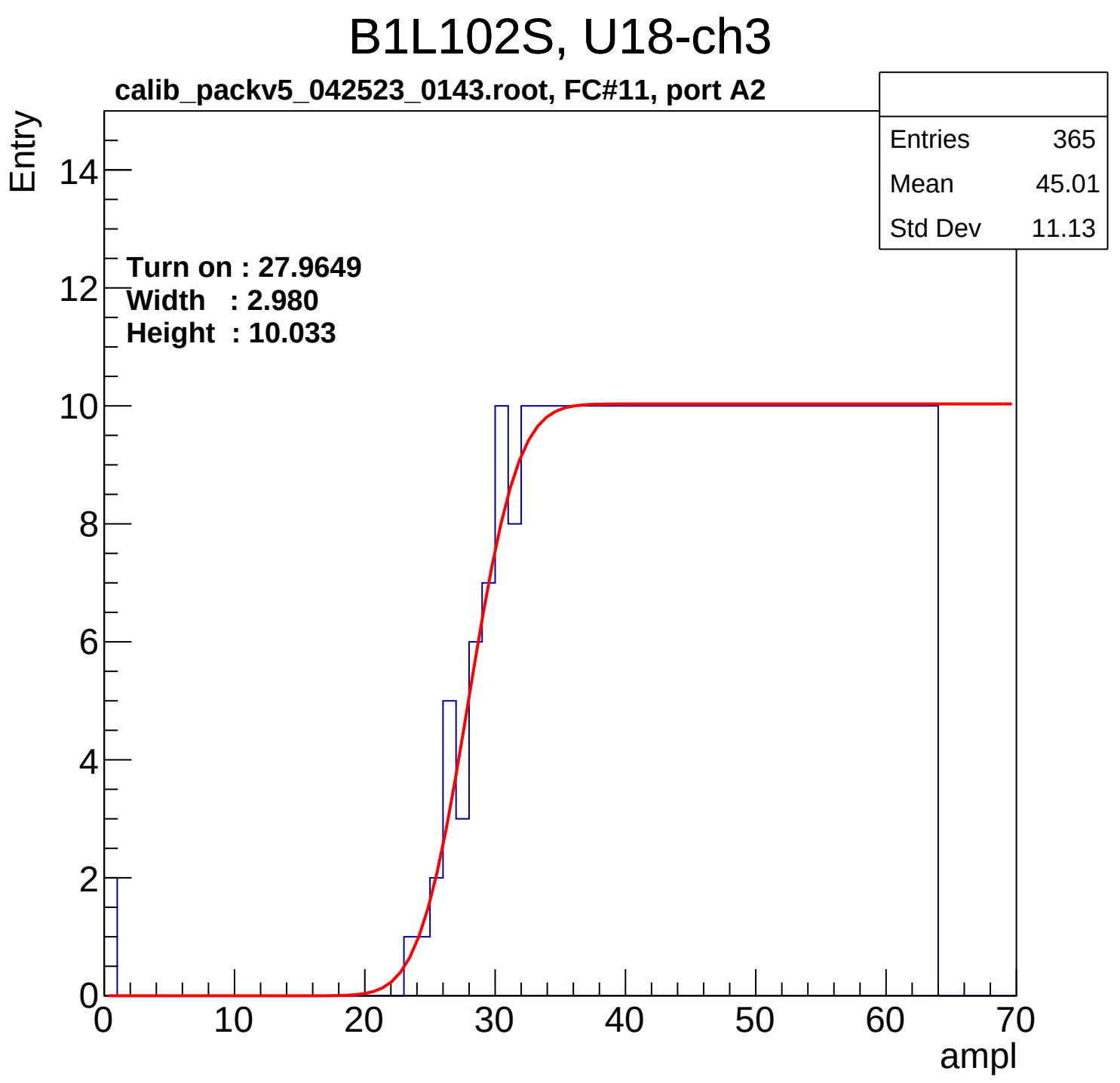
B1L102S, U18-ch3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 365
Mean 45.01
Std Dev 11.13
Turn on : 27.9649
Width : 2.980
Height : 10.033
Entry
ampl
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4
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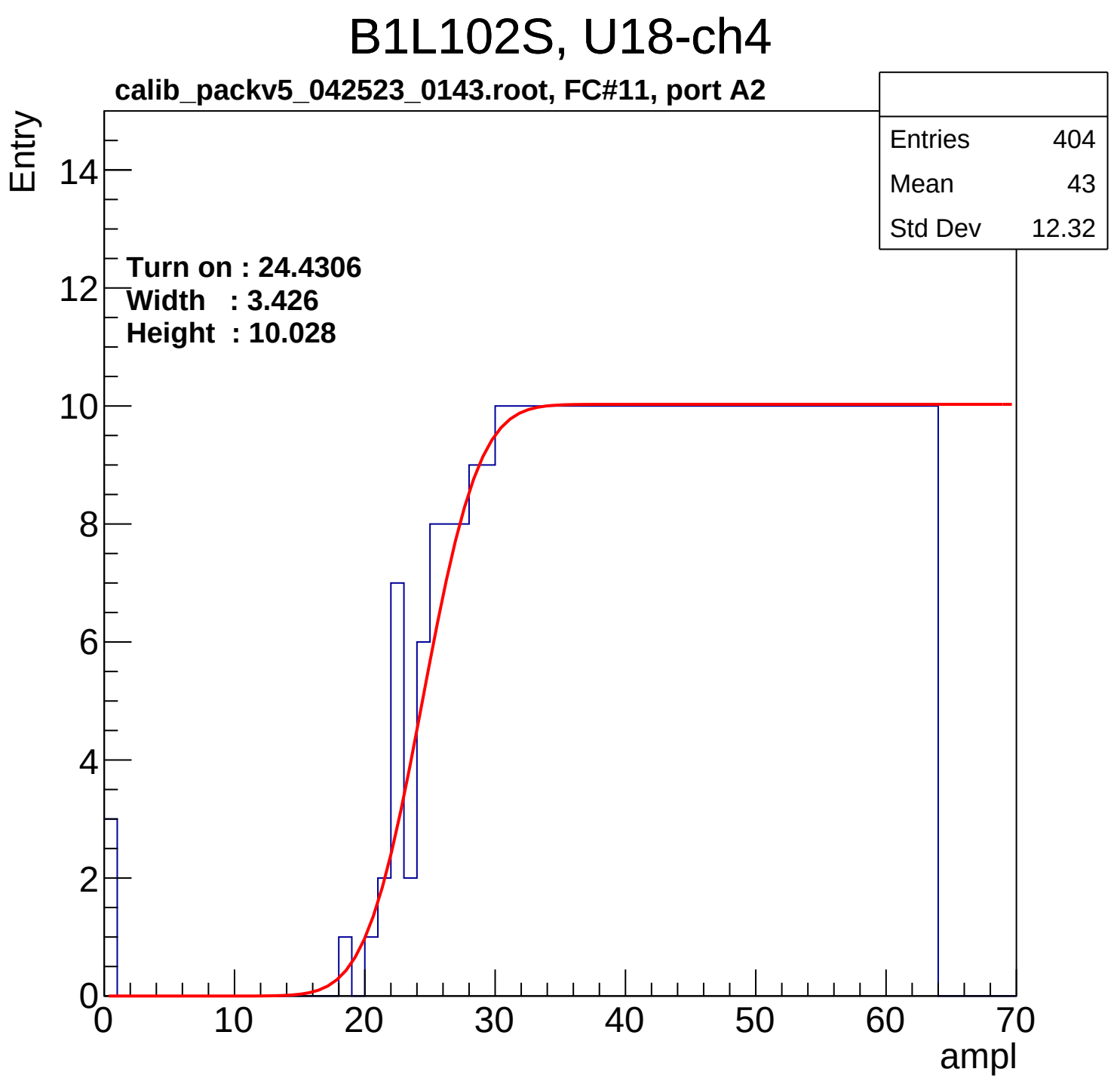
B1L102S, U18-ch4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 404
Mean 43
Std Dev 12.32
Turn on : 24.4306
Width : 3.426
Height : 10.028
Entry
ampl
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8
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0
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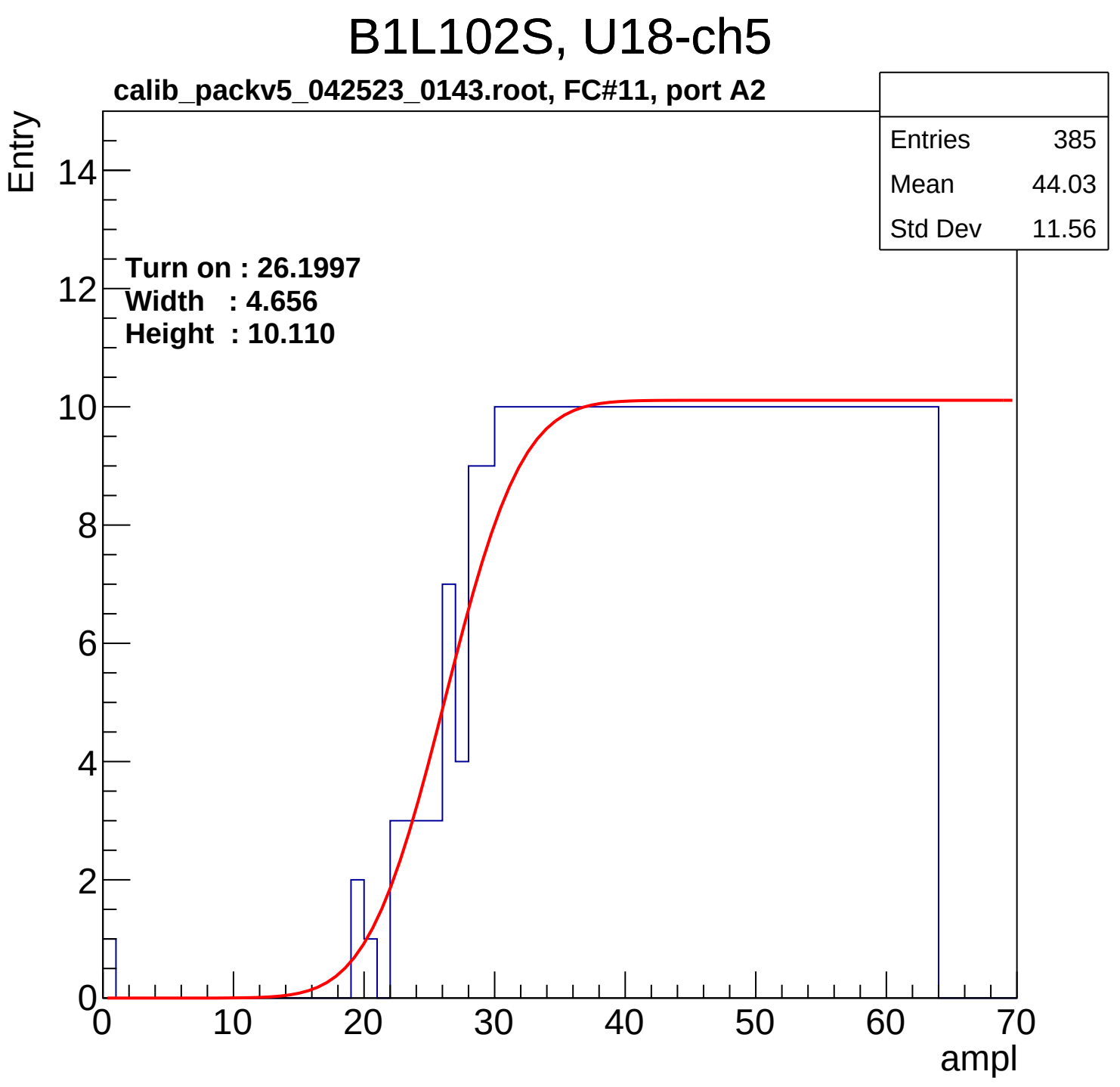
B1L102S, U18-ch5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 44.03
Std Dev 11.56
Turn on : 26.1997
Width : 4.656
Height : 10.110
Entry
ampl
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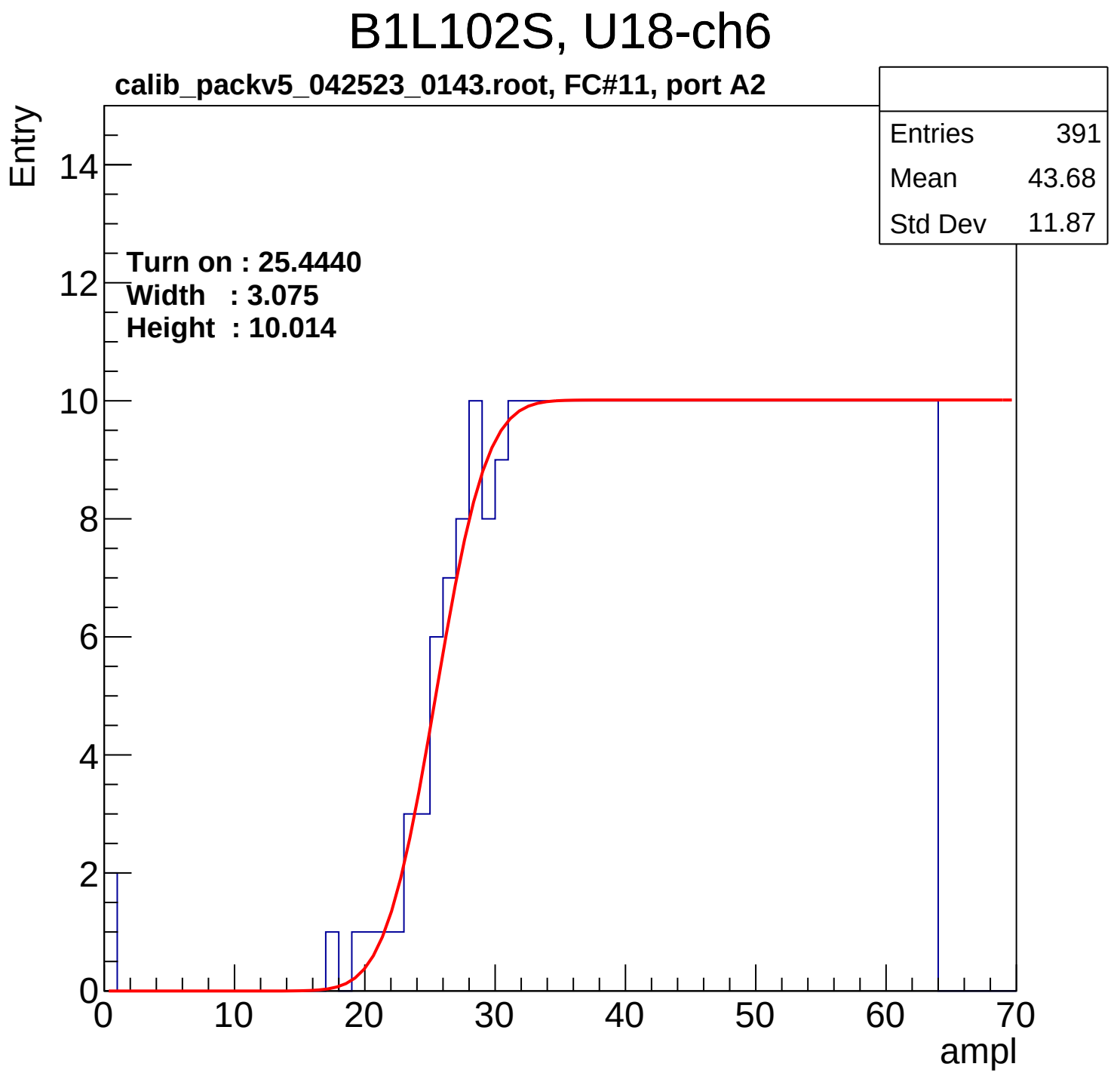
B1L102S, U18-ch6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.68
Std Dev 11.87
Turn on : 25.4440
Width : 3.075
Height : 10.014
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ampl
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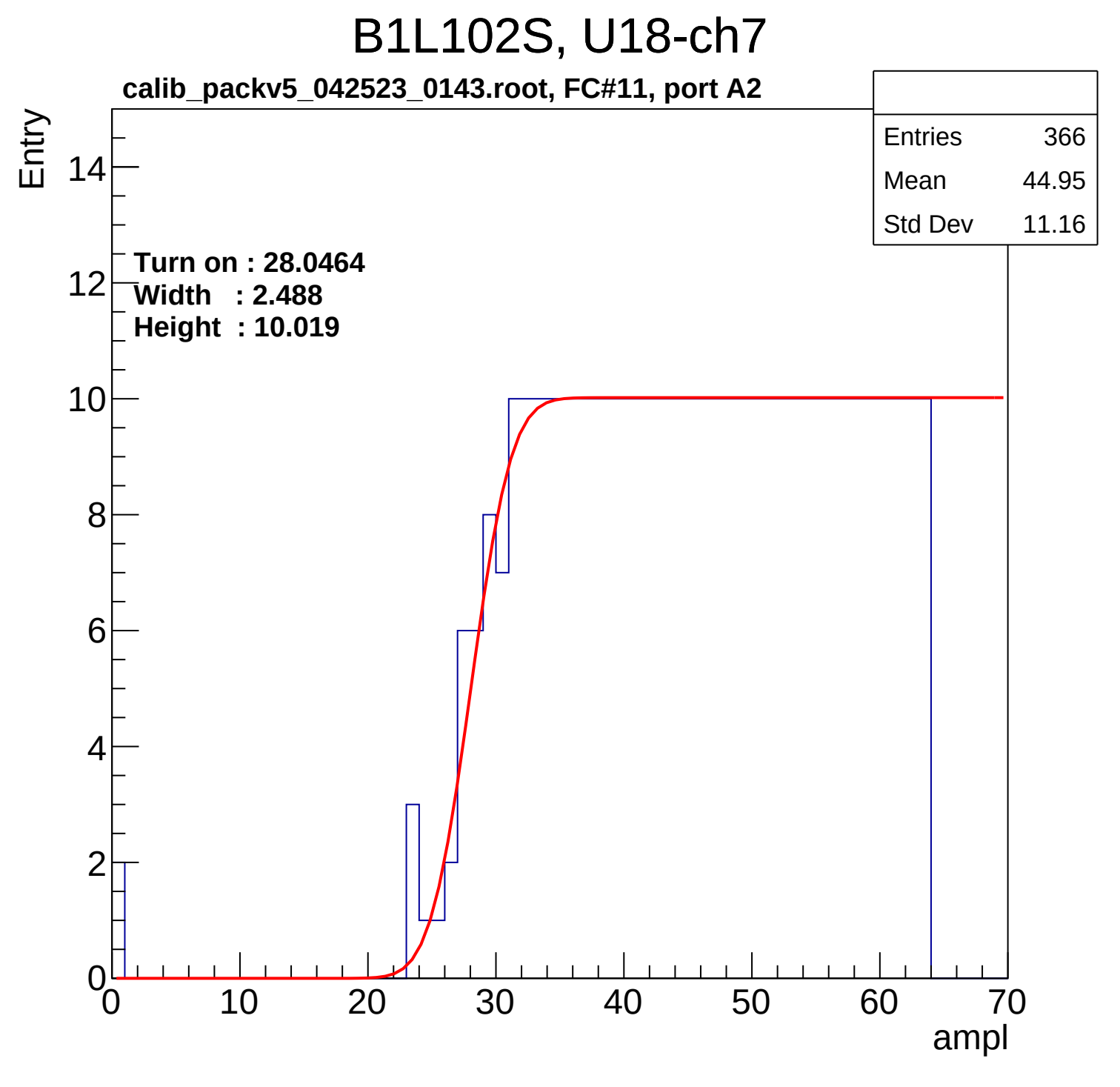
B1L102S, U18-ch7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 366
Mean 44.95
Std Dev 11.16
Turn on : 28.0464
Width : 2.488
Height : 10.019
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ampl
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8
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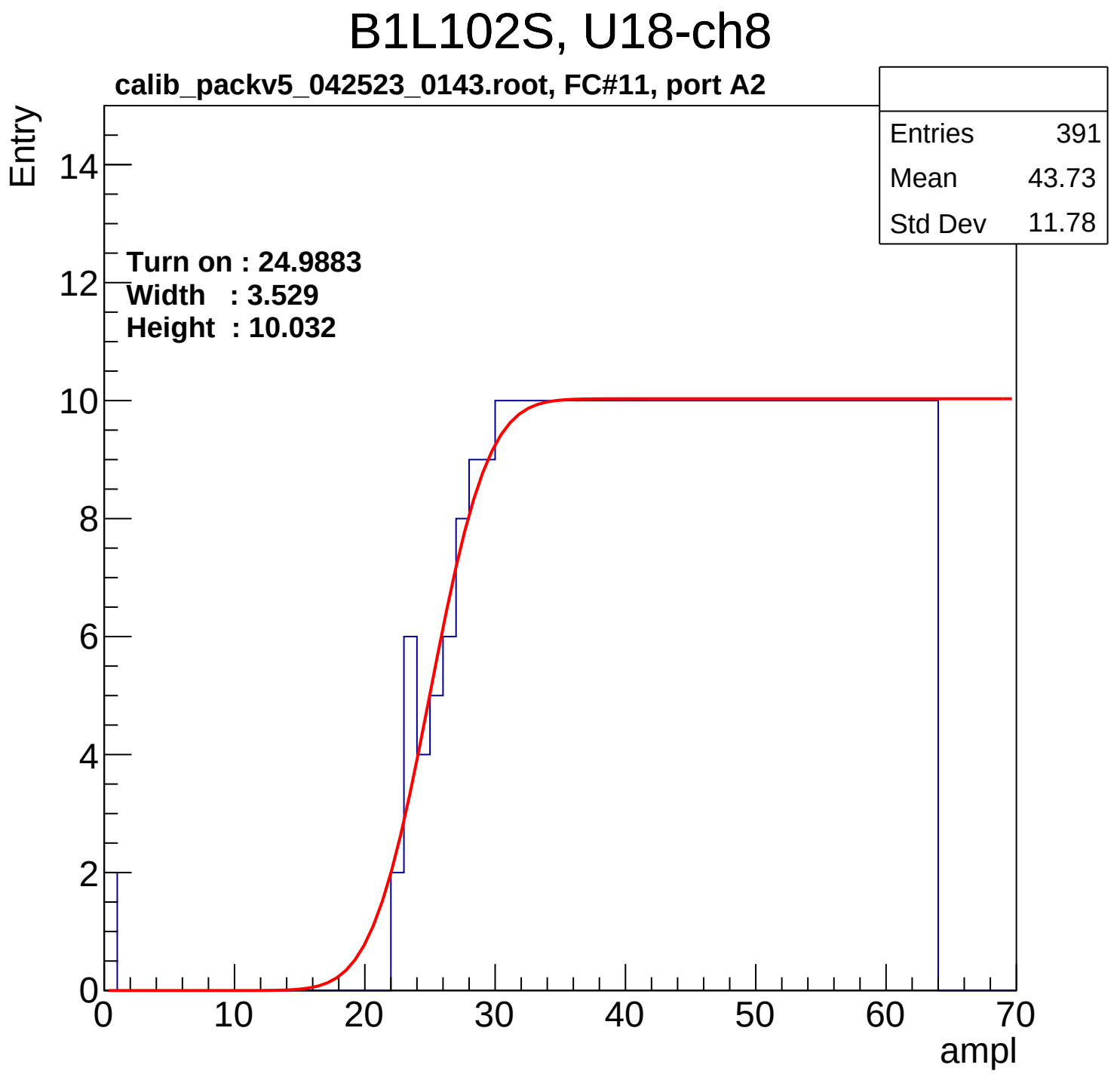
B1L102S, U18-ch8
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.73
Std Dev 11.78
Turn on : 24.9883
Width : 3.529
Height : 10.032
Entry
ampl
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8
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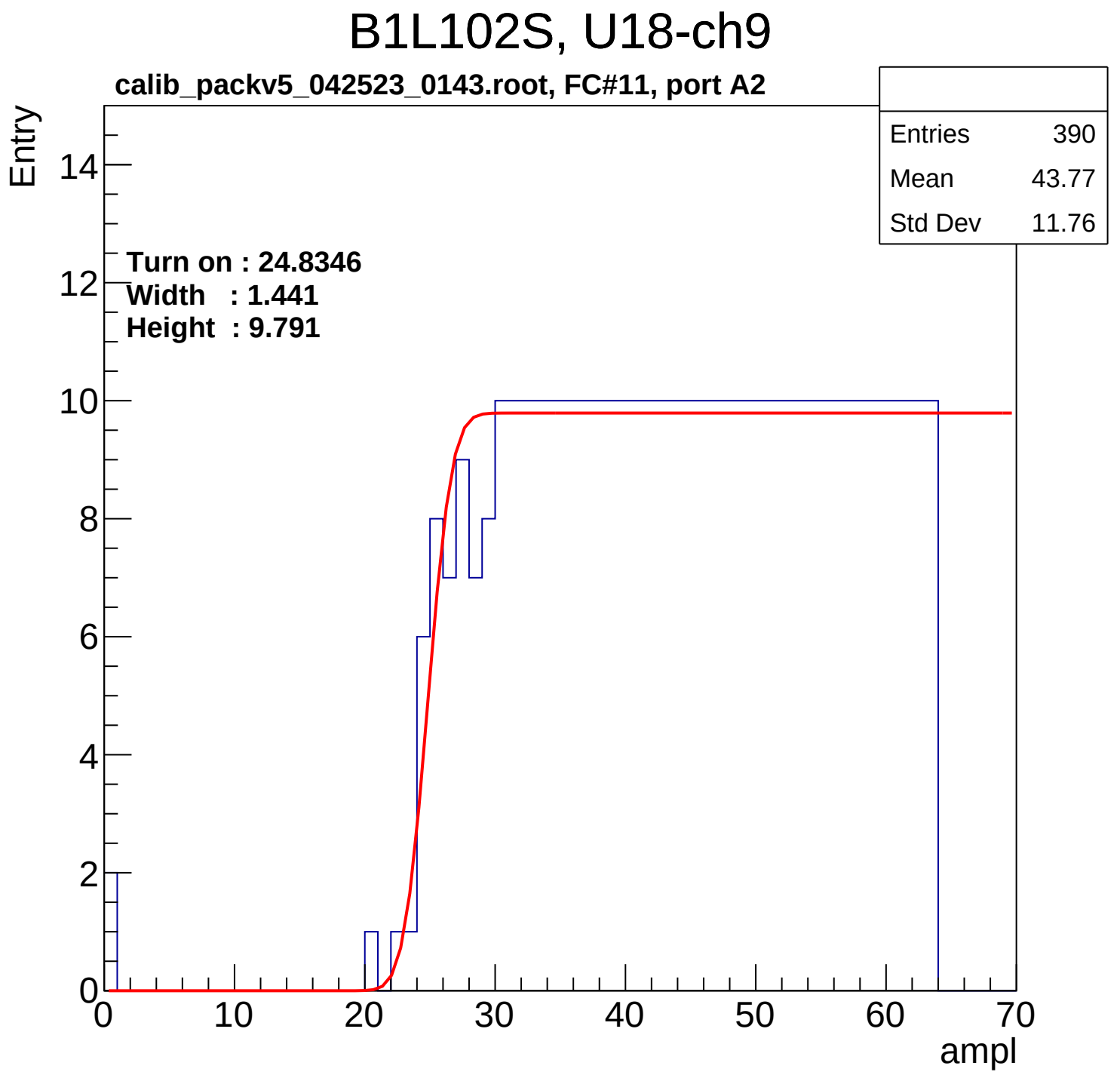
B1L102S, U18-ch9
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.77
Std Dev 11.76
Turn on : 24.8346
Width : 1.441
Height : 9.791
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ampl
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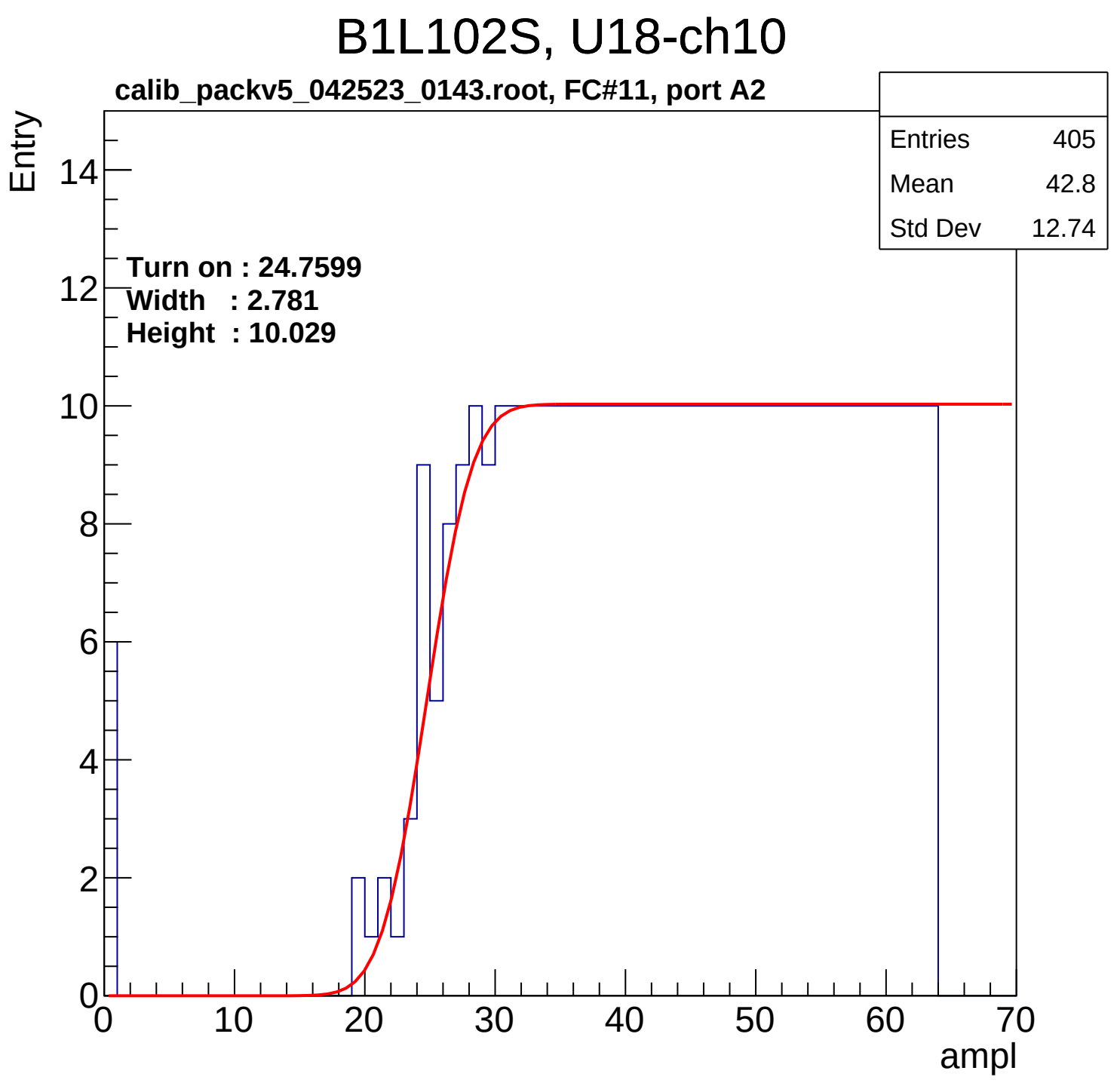
B1L102S, U18-ch10
calib_packv5_042523_0143.root, FC#11, port A2
Entries 405
Mean 42.8
Std Dev 12.74
Turn on : 24.7599
Width : 2.781
Height : 10.029
Entry
ampl
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6
8
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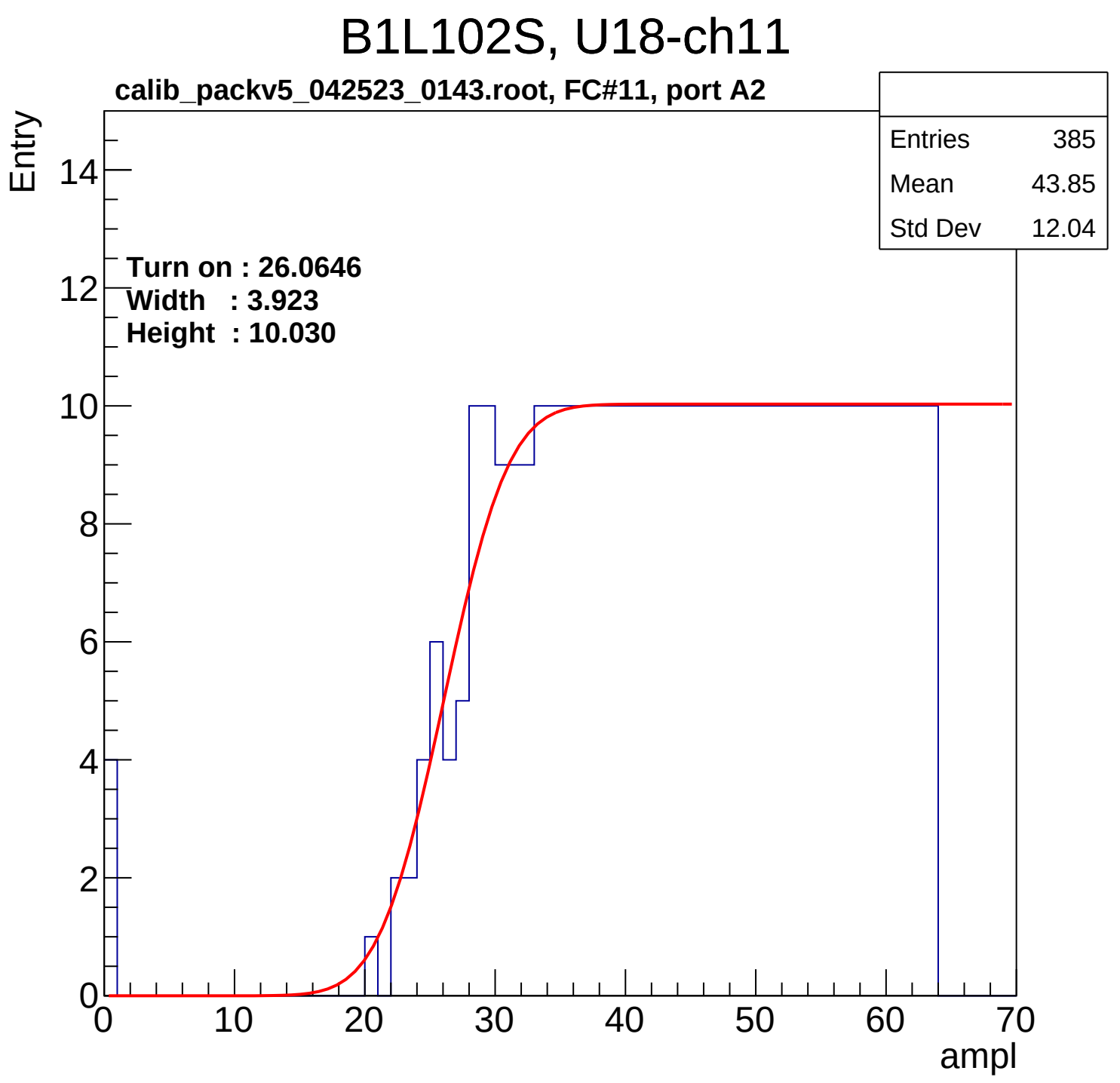
B1L102S, U18-ch11
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.85
Std Dev 12.04
Turn on : 26.0646
Width : 3.923
Height : 10.030
Entry
ampl
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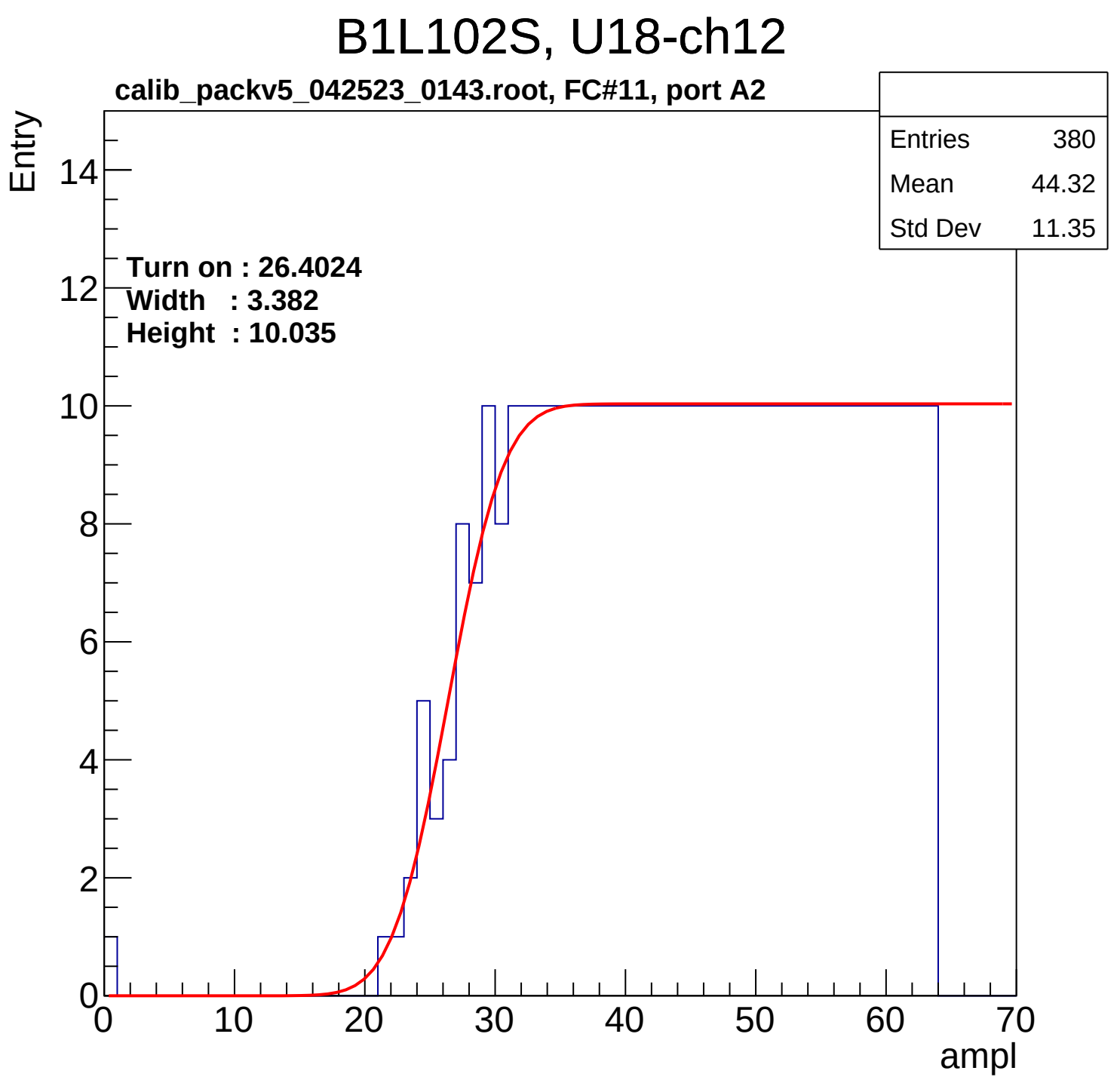
B1L102S, U18-ch12
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.32
Std Dev 11.35
Turn on : 26.4024
Width : 3.382
Height : 10.035
Entry
ampl
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6
8
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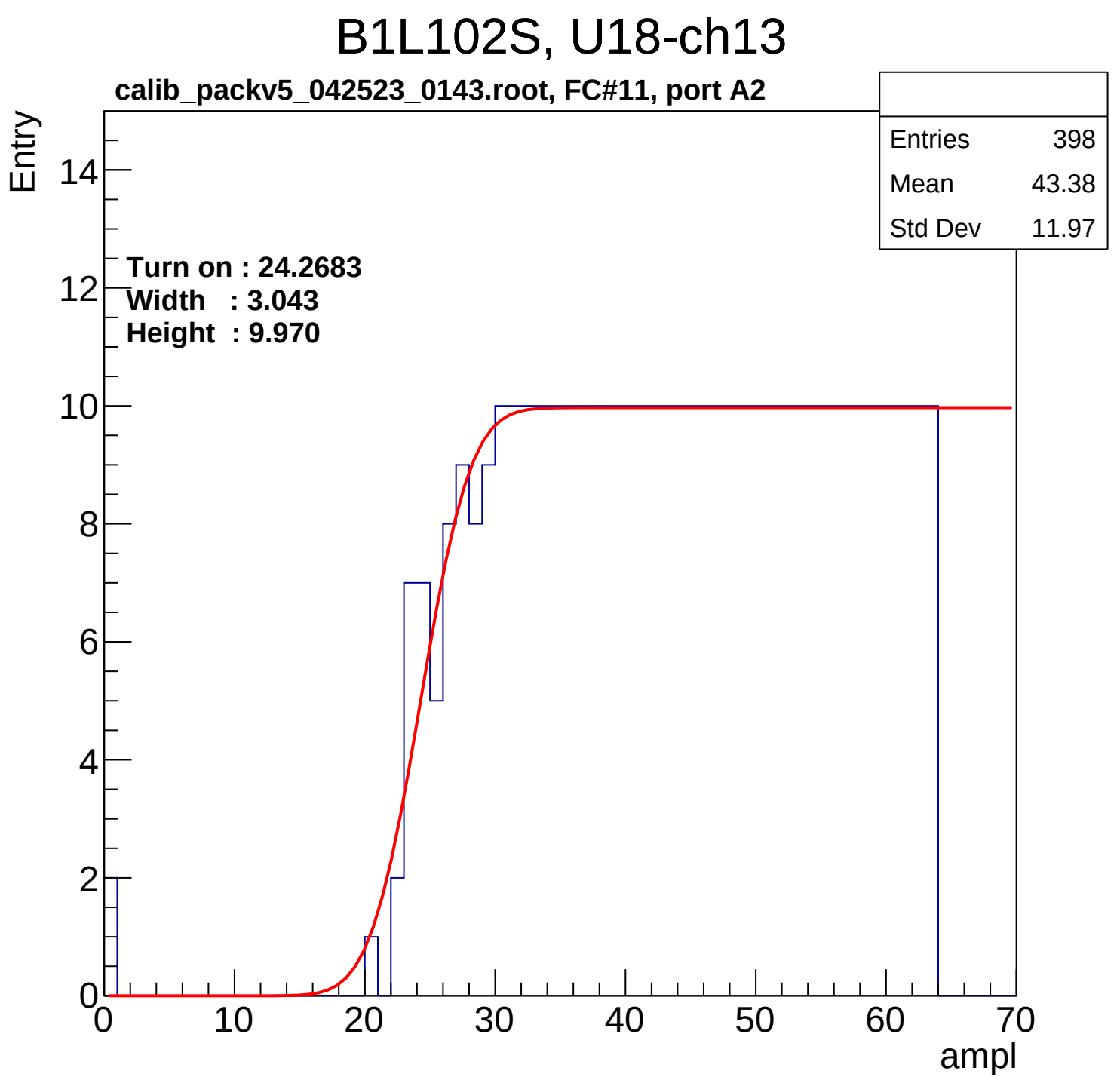
B1L102S, U18-ch13
calib_packv5_042523_0143.root, FC#11, port A2
Entries 398
Mean 43.38
Std Dev 11.97
Turn on : 24.2683
Width : 3.043
Height : 9.970
Entry
ampl
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6
8
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0
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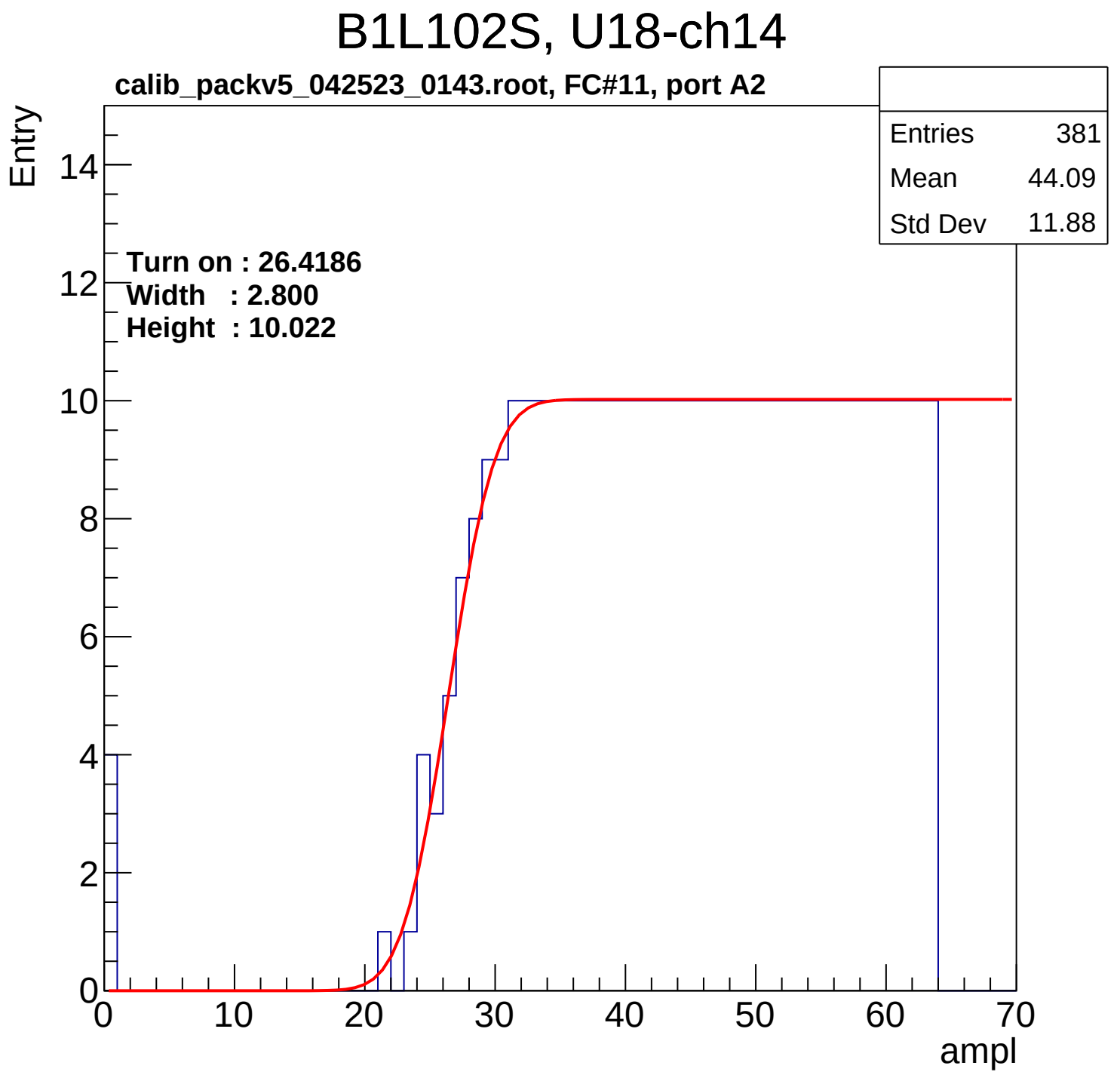
B1L102S, U18-ch14
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.09
Std Dev 11.88
Turn on : 26.4186
Width : 2.800
Height : 10.022
Entry
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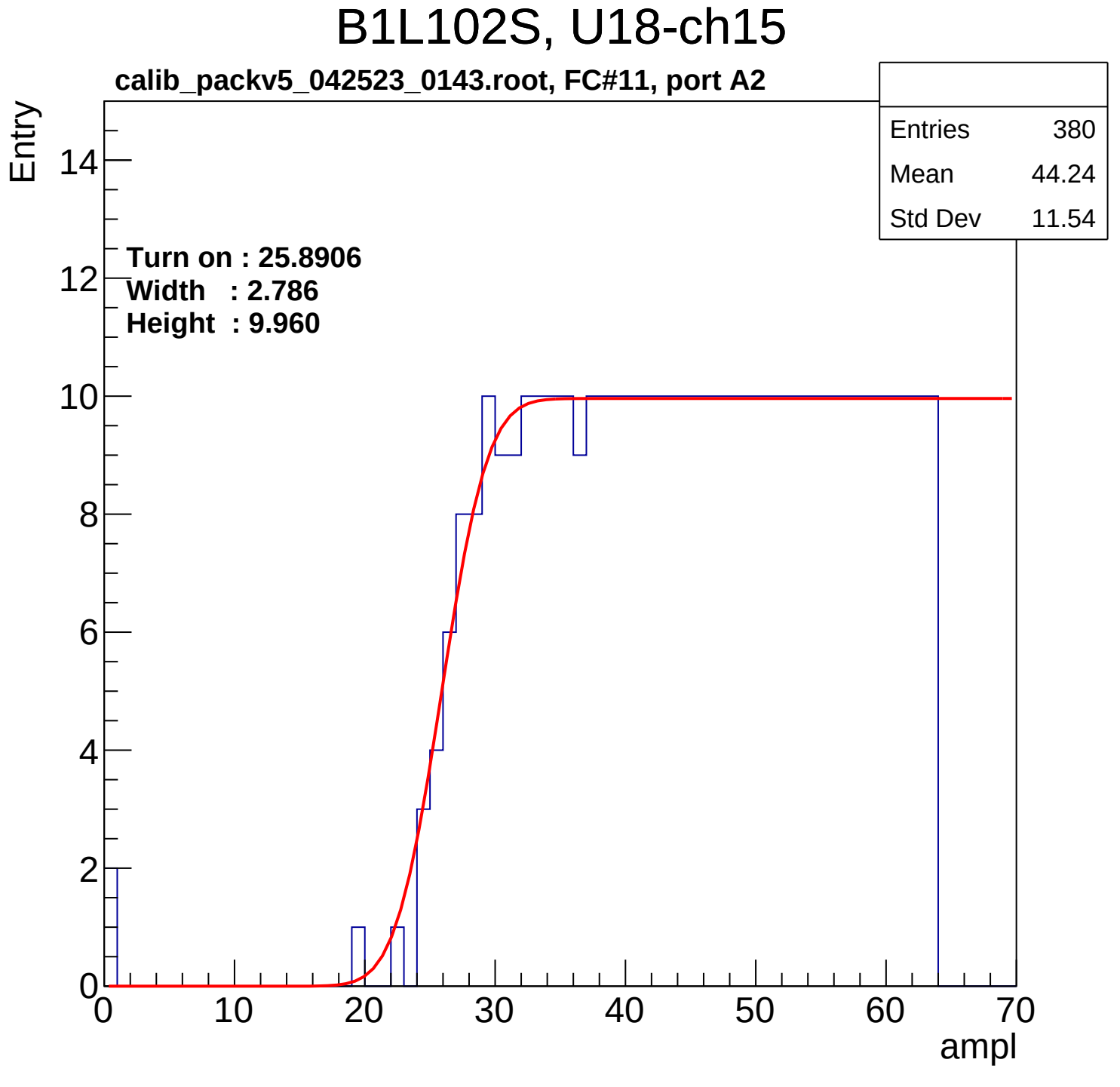
B1L102S, U18-ch15
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.24
Std Dev 11.54
Turn on : 25.8906
Width : 2.786
Height : 9.960
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ampl
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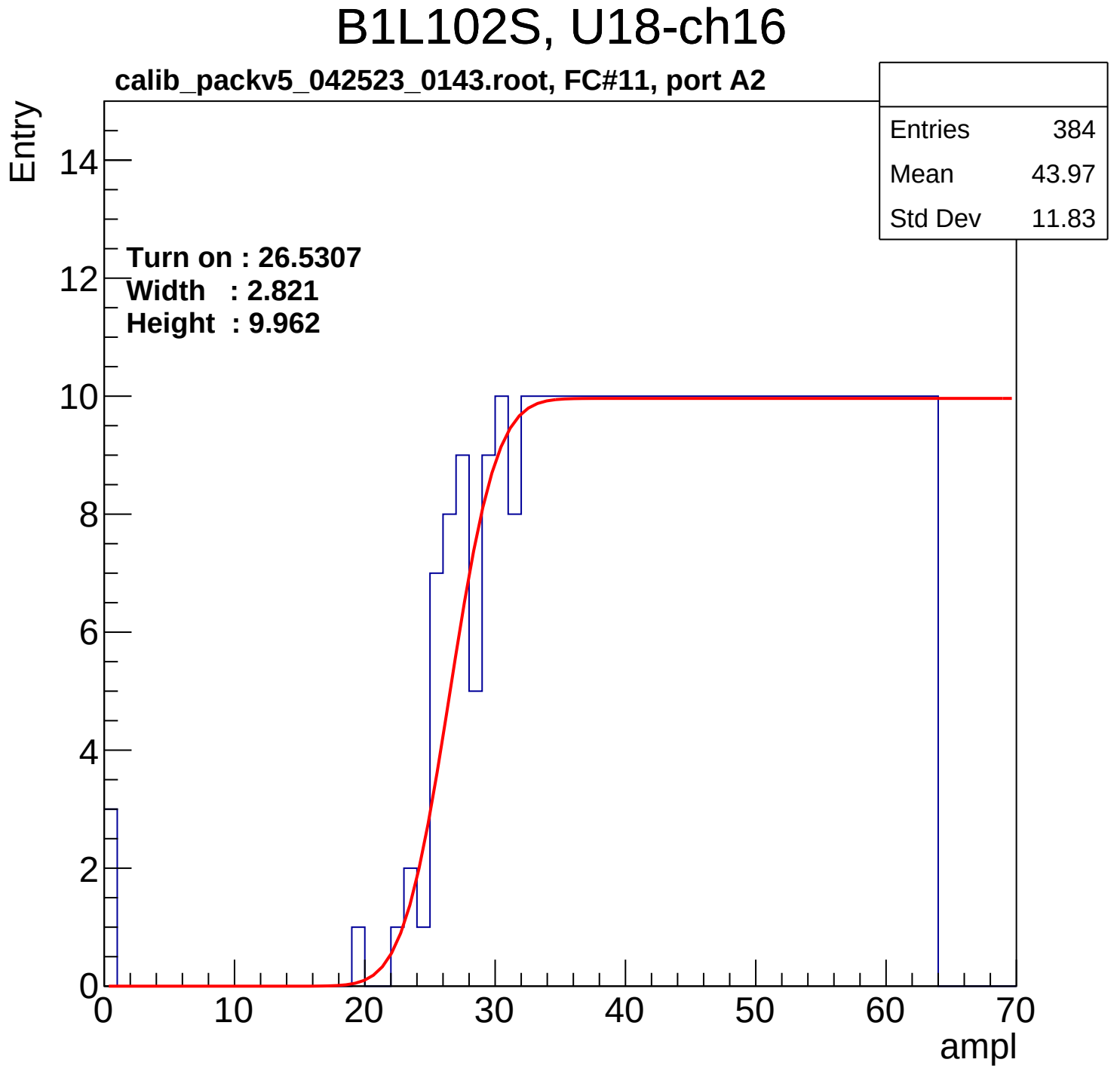
B1L102S, U18-ch16
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 43.97
Std Dev 11.83
Turn on : 26.5307
Width : 2.821
Height : 9.962
Entry
ampl
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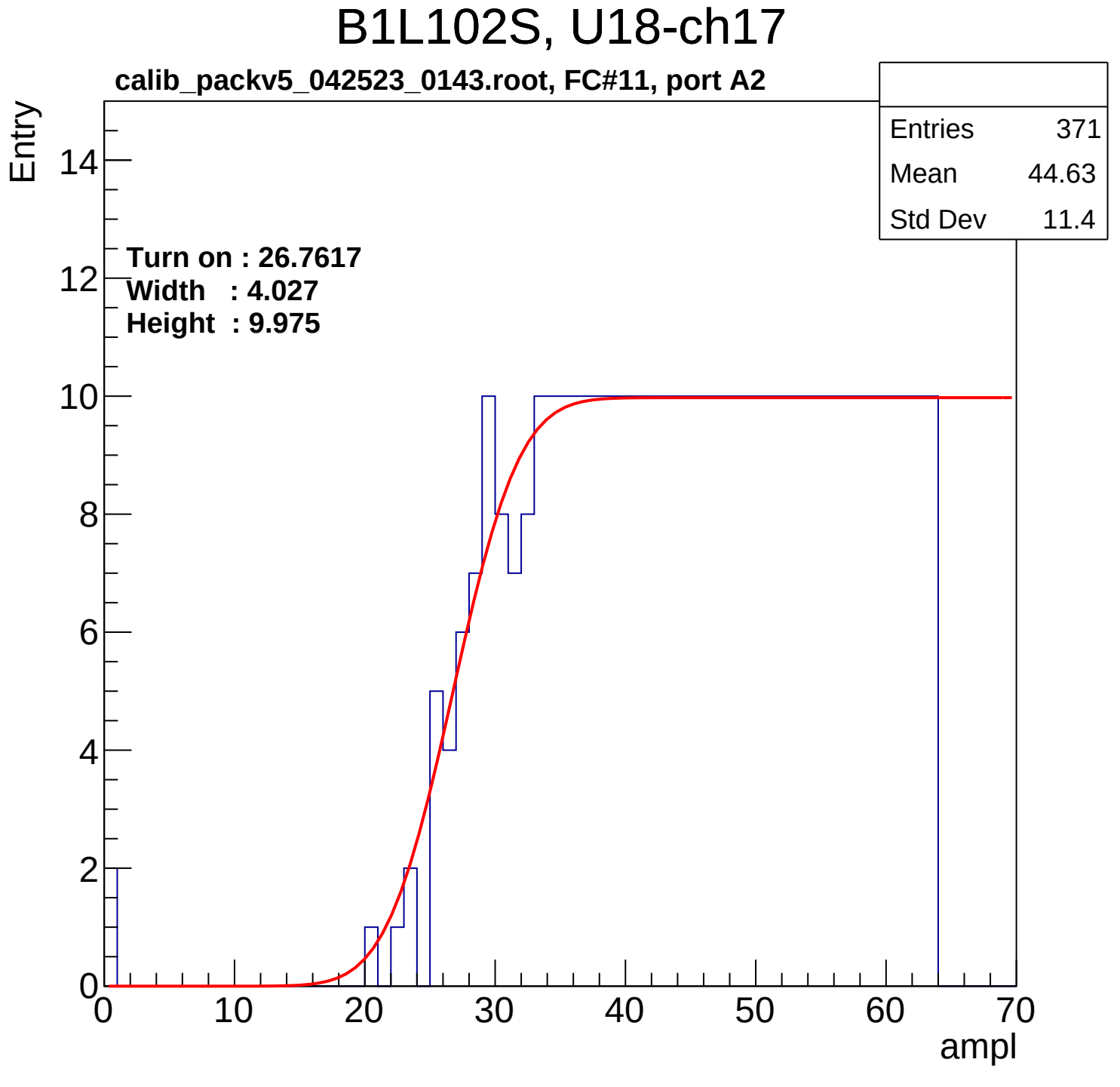
B1L102S, U18-ch17
calib_packv5_042523_0143.root, FC#11, port A2
Entries 371
Mean 44.63
Std Dev 11.4
Turn on : 26.7617
Width : 4.027
Height : 9.975
Entry
ampl
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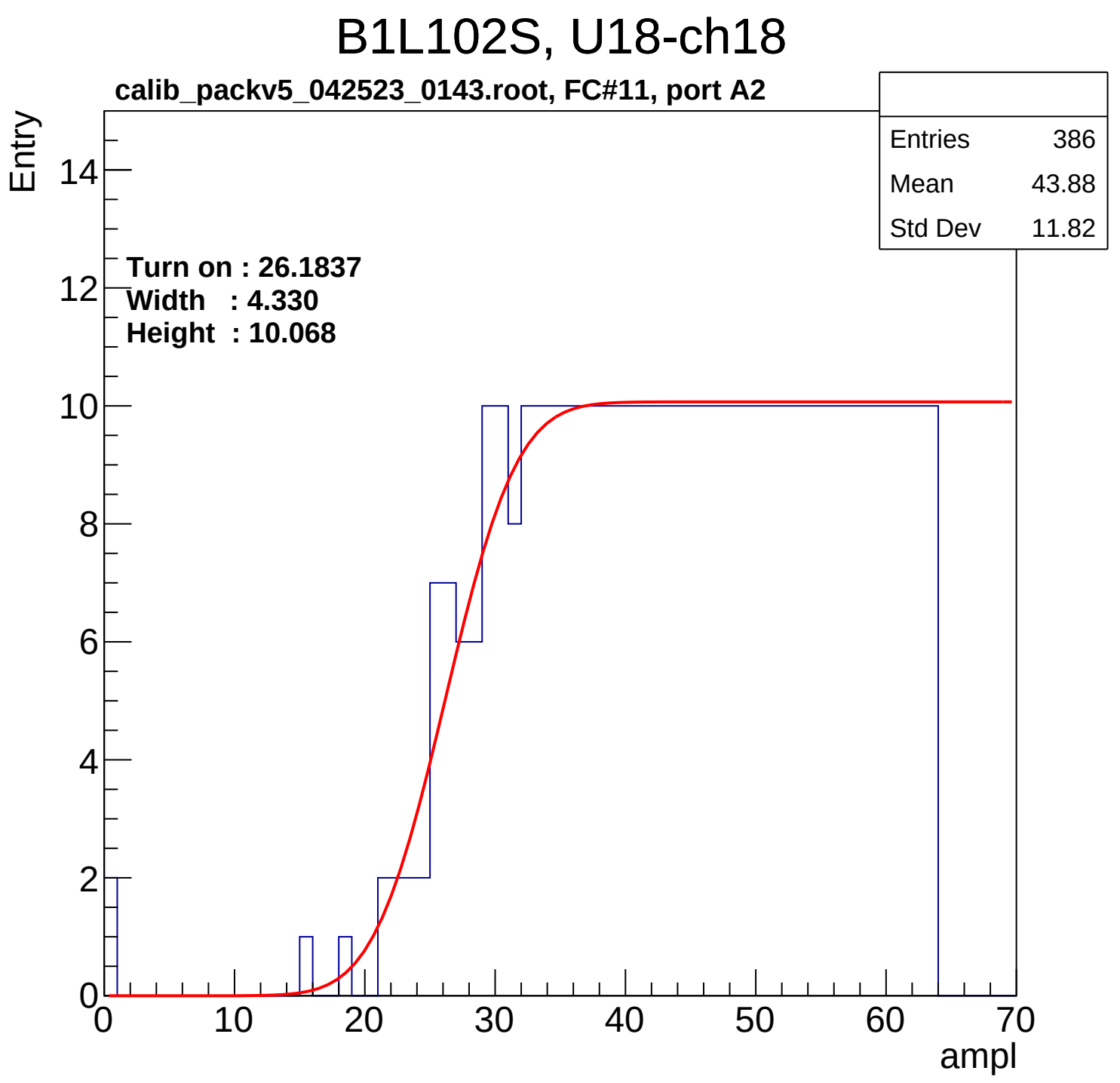
B1L102S, U18-ch18
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.88
Std Dev 11.82
Turn on : 26.1837
Width : 4.330
Height : 10.068
Entry
ampl
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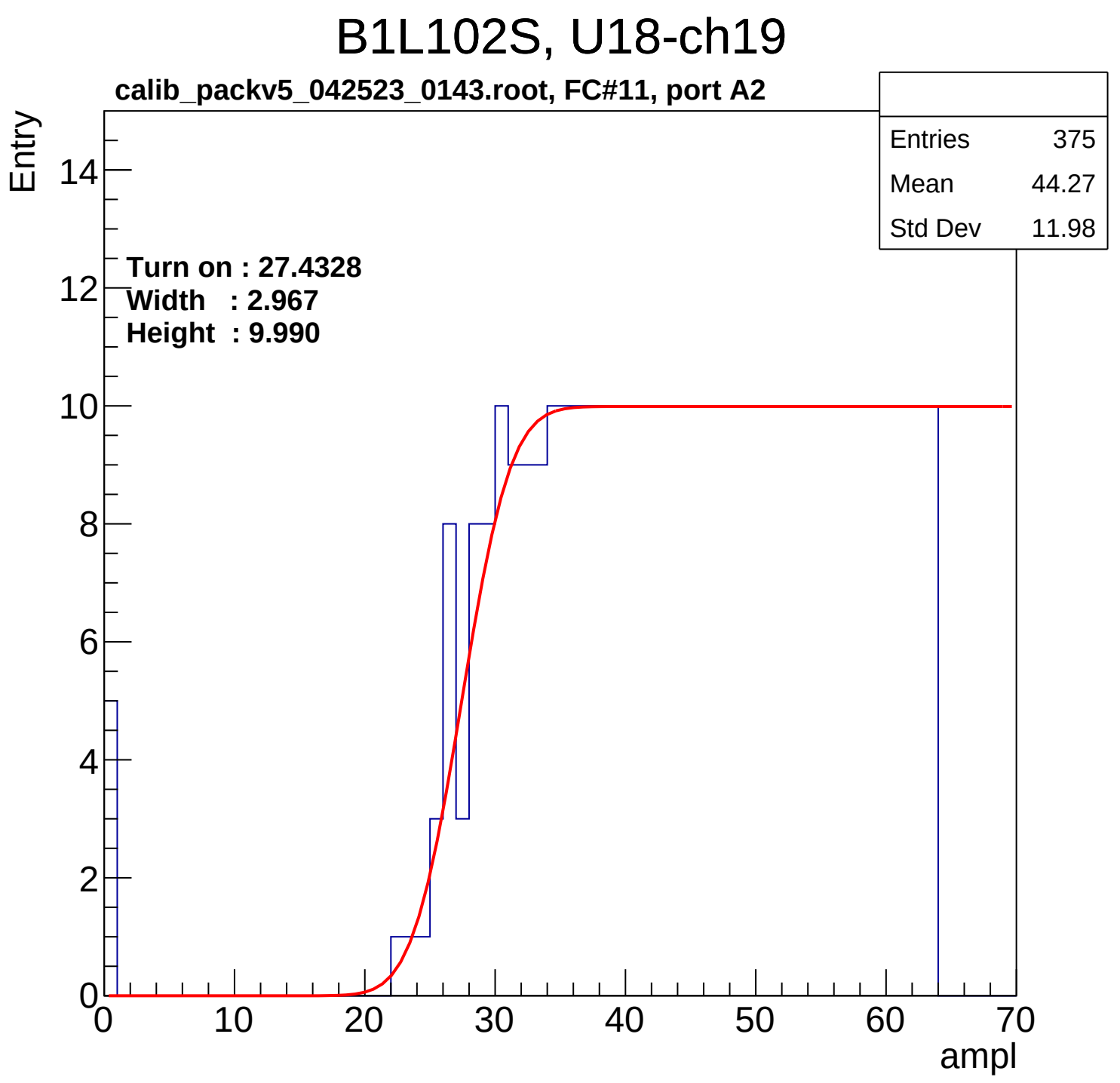
B1L102S, U18-ch19
calib_packv5_042523_0143.root, FC#11, port A2
Entries 375
Mean 44.27
Std Dev 11.98
Turn on : 27.4328
Width : 2.967
Height : 9.990
Entry
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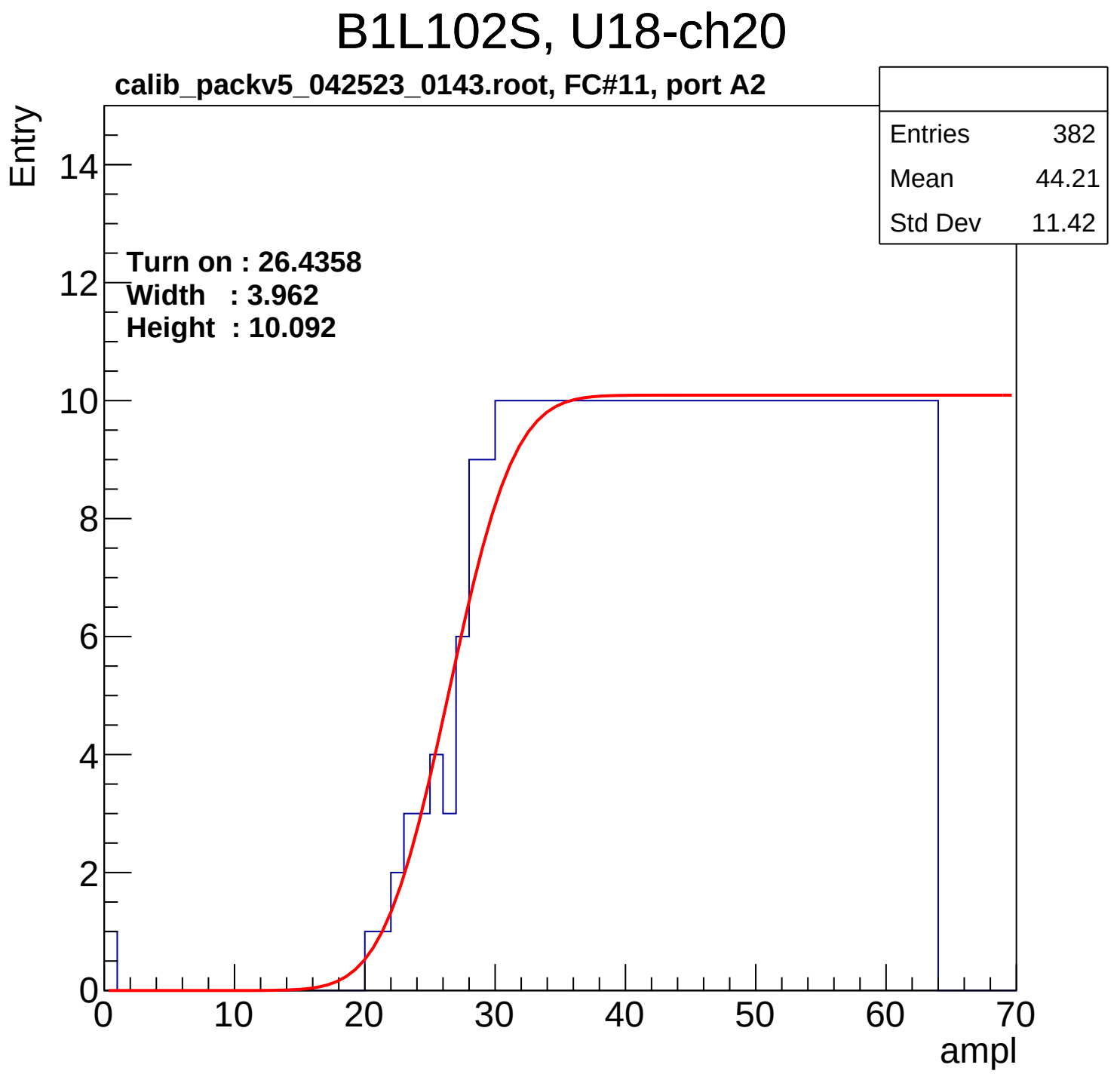
B1L102S, U18-ch20
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.21
Std Dev 11.42
Turn on : 26.4358
Width : 3.962
Height : 10.092
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ampl
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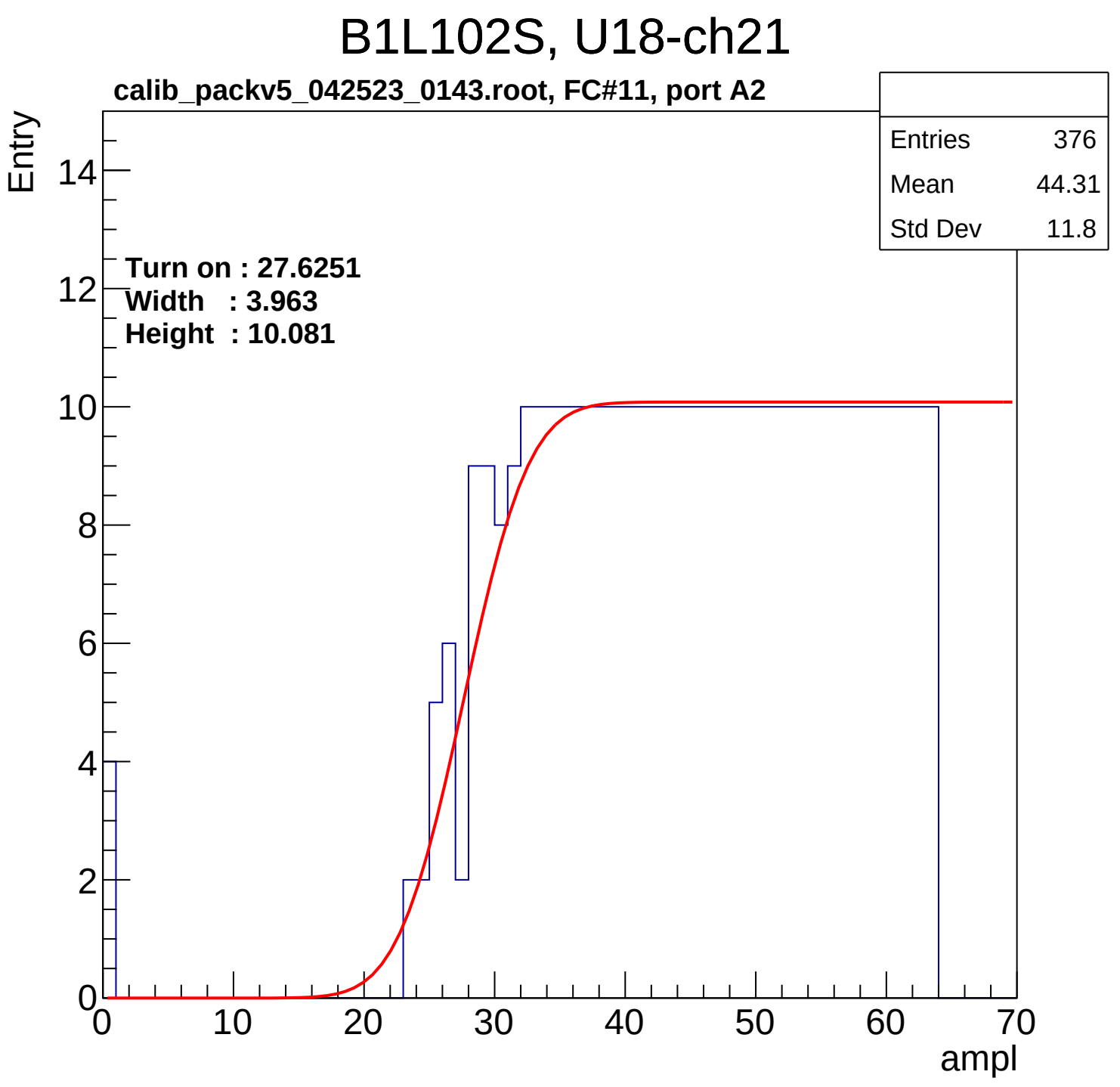
B1L102S, U18-ch21
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.31
Std Dev 11.8
Turn on : 27.6251
Width : 3.963
Height : 10.081
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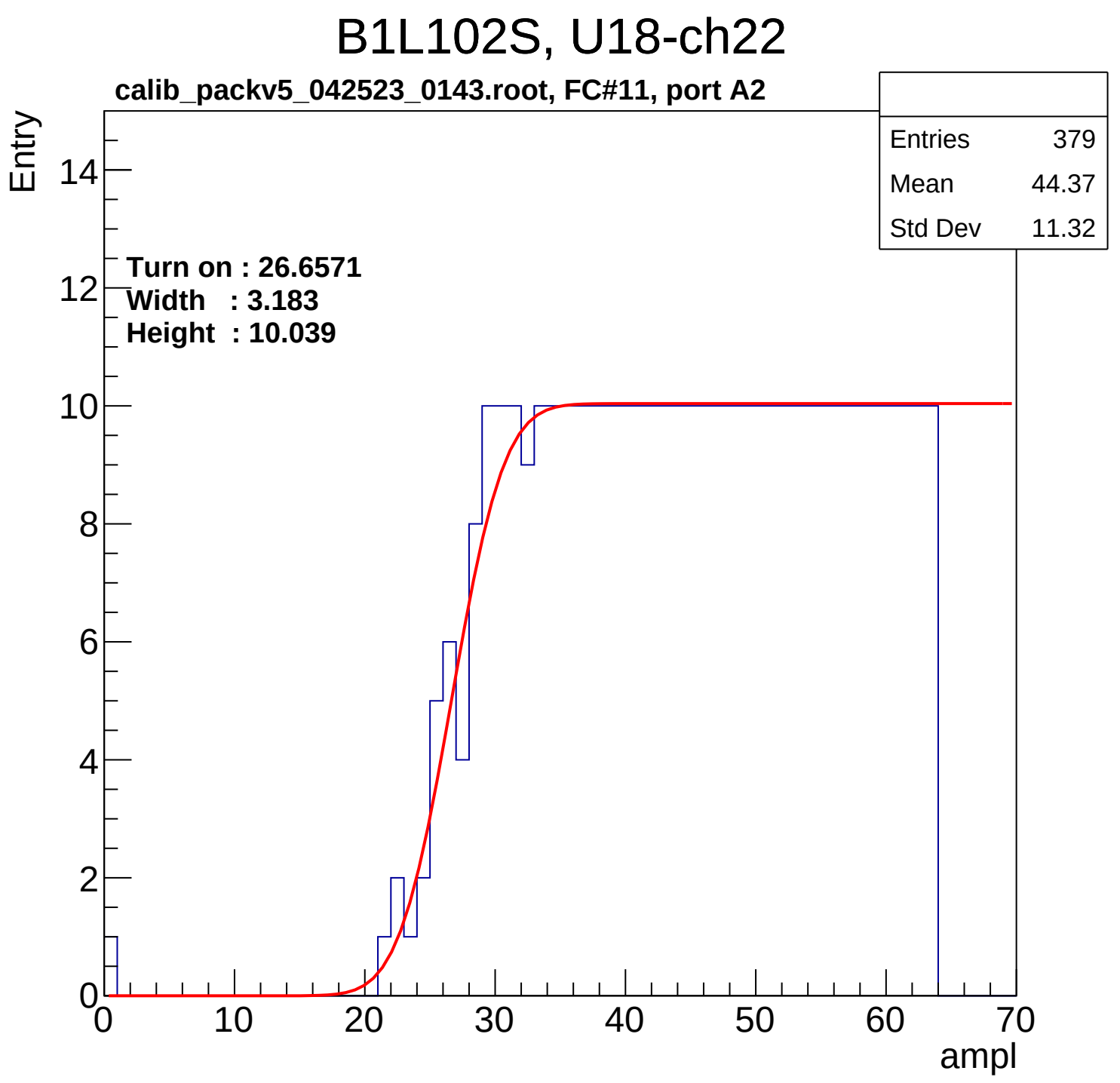
B1L102S, U18-ch22
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.37
Std Dev 11.32
Turn on : 26.6571
Width : 3.183
Height : 10.039
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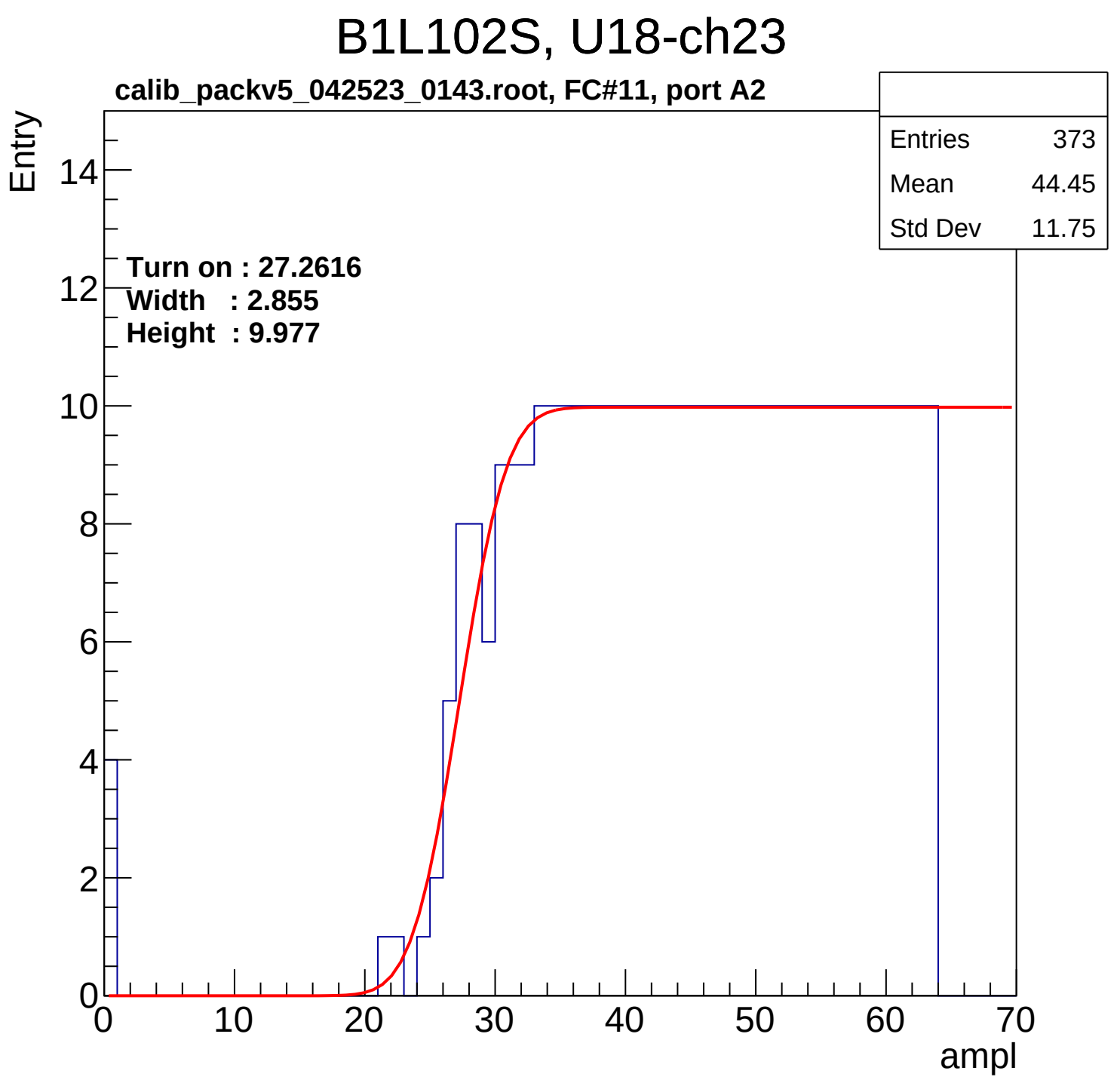
B1L102S, U18-ch23
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.45
Std Dev 11.75
Turn on : 27.2616
Width : 2.855
Height : 9.977
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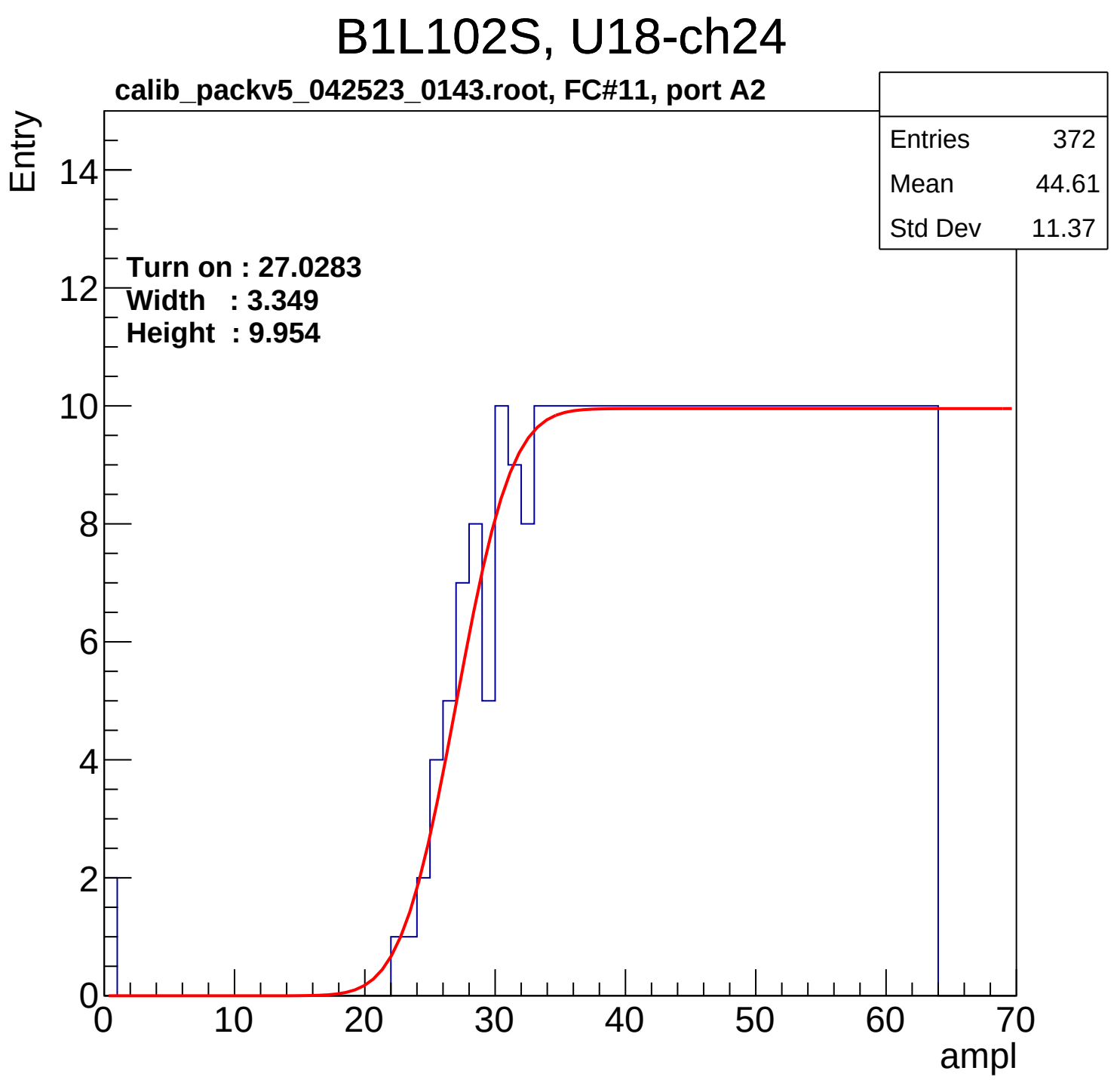
B1L102S, U18-ch24
calib_packv5_042523_0143.root, FC#11, port A2
Entries 372
Mean 44.61
Std Dev 11.37
Turn on : 27.0283
Width : 3.349
Height : 9.954
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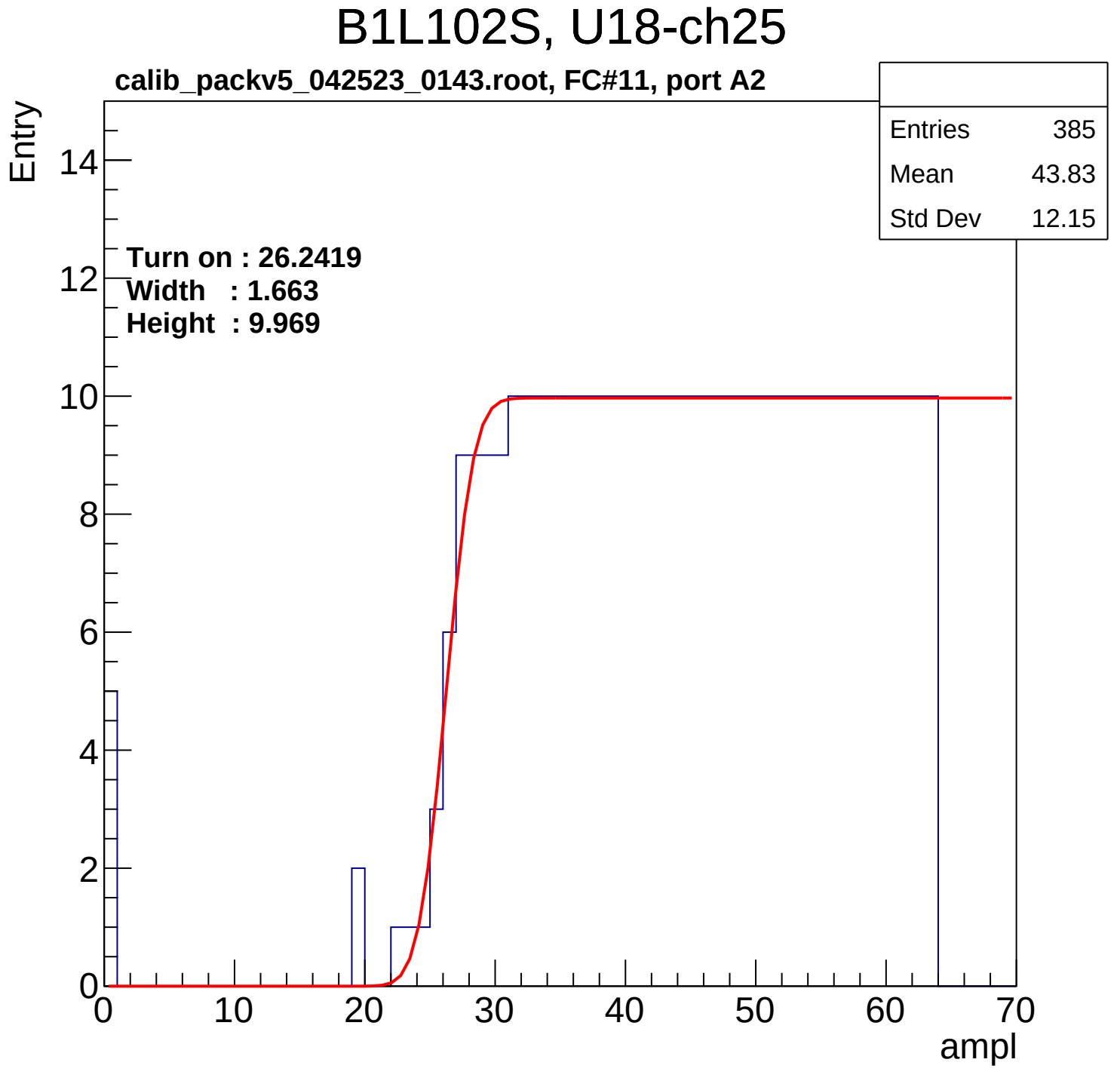
B1L102S, U18-ch25
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.83
Std Dev 12.15
Turn on : 26.2419
Width : 1.663
Height : 9.969
Entry
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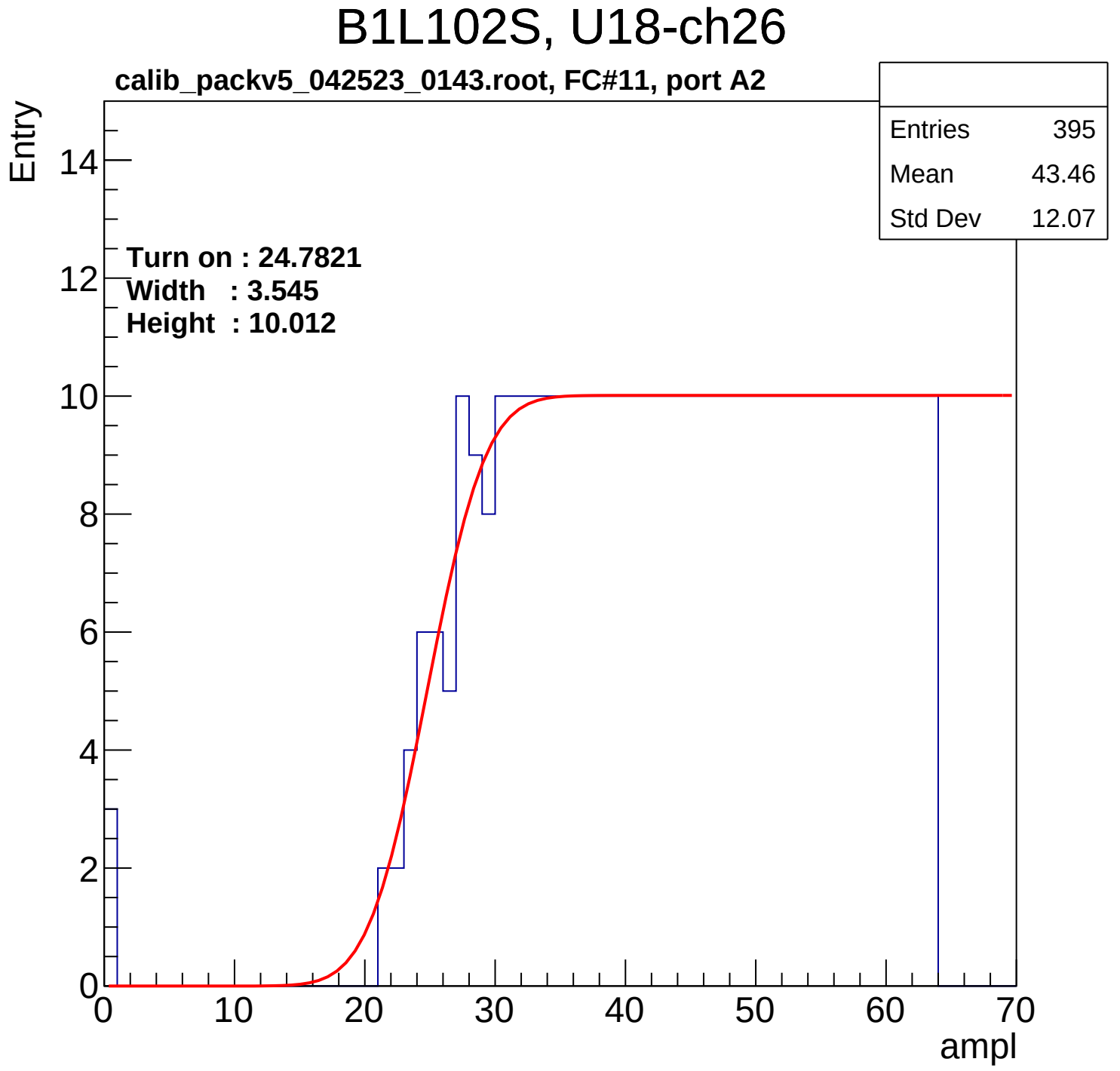
B1L102S, U18-ch26
calib_packv5_042523_0143.root, FC#11, port A2
Entries 395
Mean 43.46
Std Dev 12.07
Turn on : 24.7821
Width : 3.545
Height : 10.012
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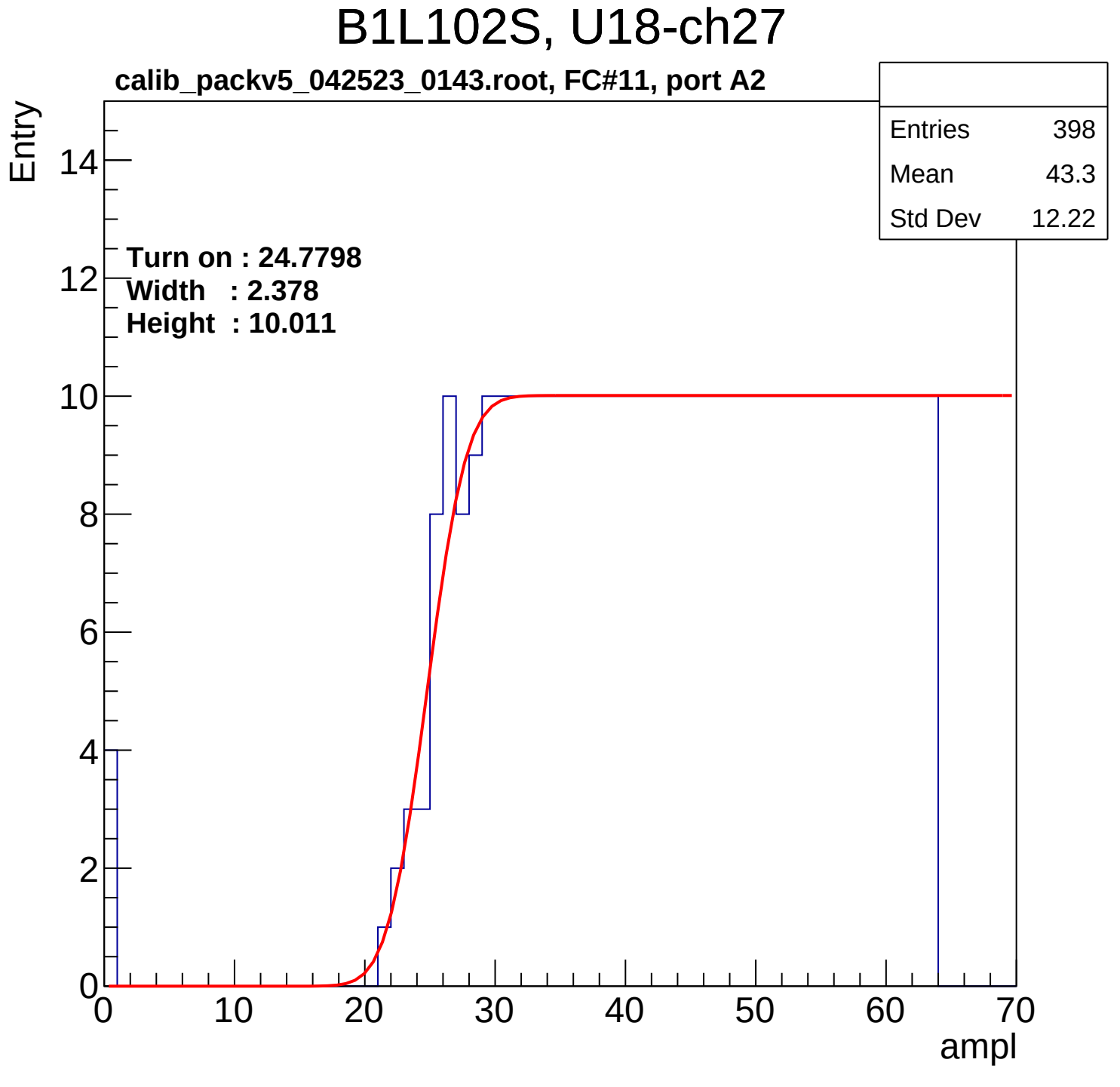
B1L102S, U18-ch27
calib_packv5_042523_0143.root, FC#11, port A2
Entries 398
Mean 43.3
Std Dev 12.22
Turn on : 24.7798
Width : 2.378
Height : 10.011
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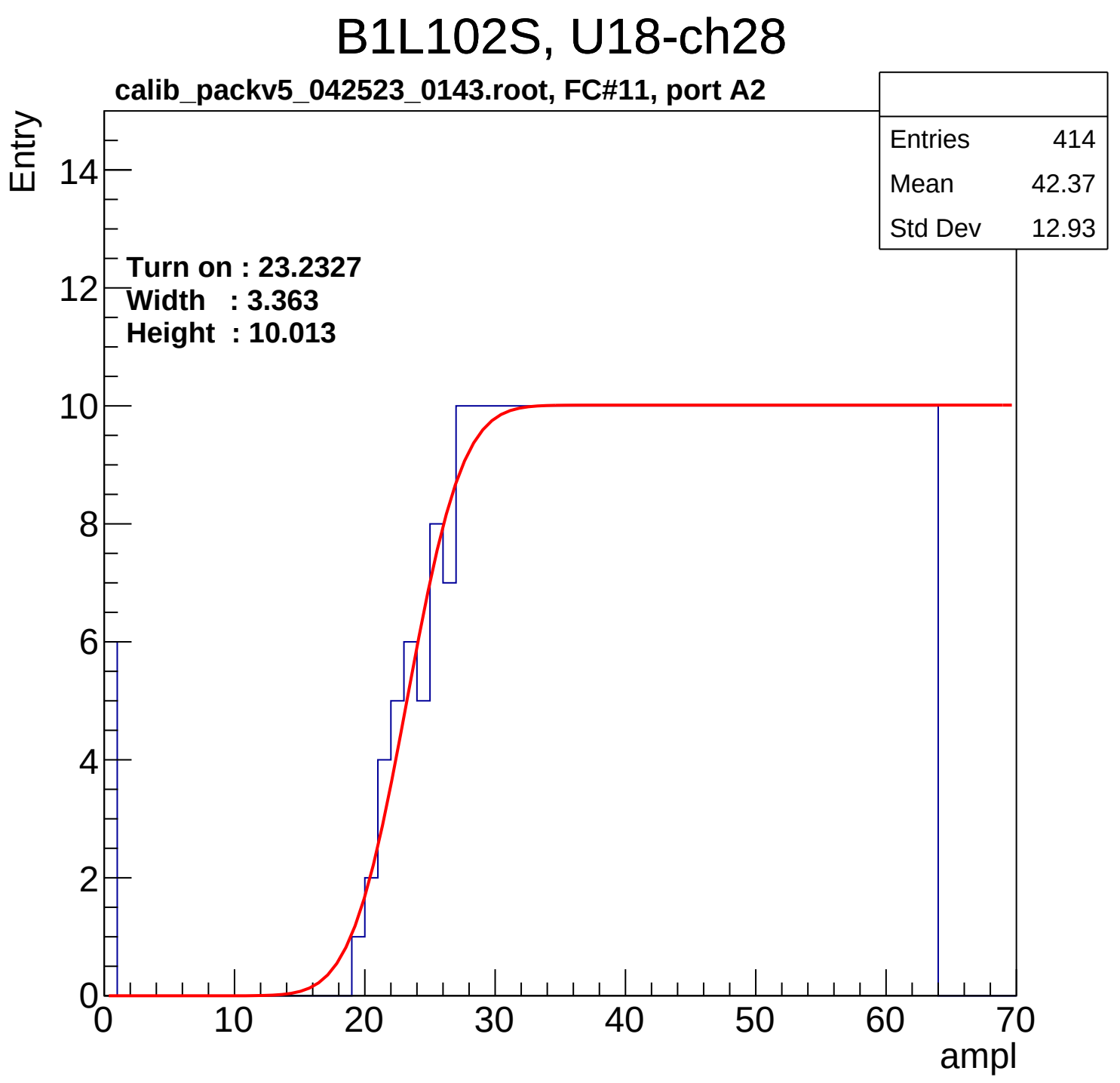
B1L102S, U18-ch28
calib_packv5_042523_0143.root, FC#11, port A2
Entries 414
Mean 42.37
Std Dev 12.93
Turn on : 23.2327
Width : 3.363
Height : 10.013
Entry
ampl
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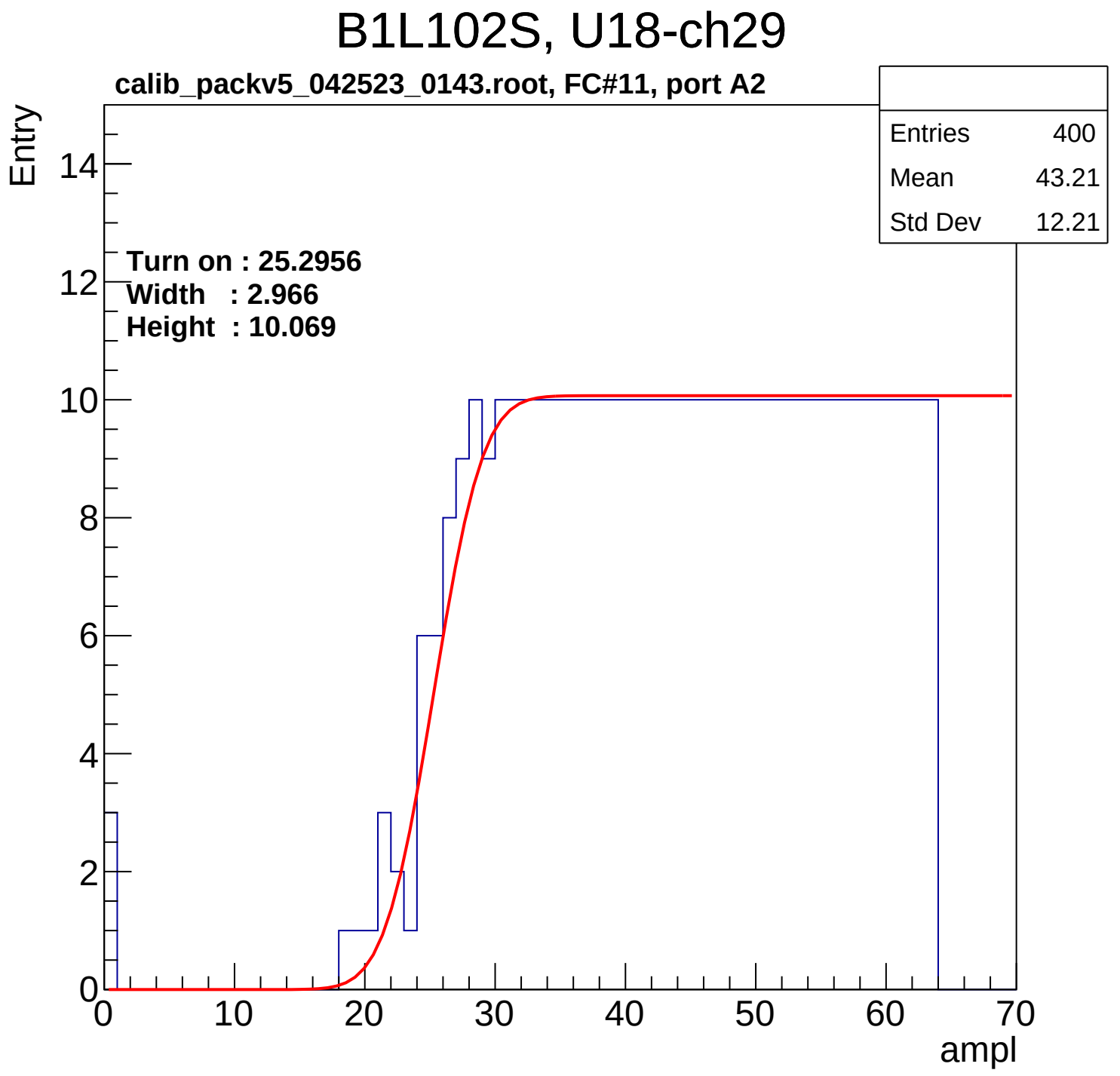
B1L102S, U18-ch29
calib_packv5_042523_0143.root, FC#11, port A2
Entries 400
Mean 43.21
Std Dev 12.21
Turn on : 25.2956
Width : 2.966
Height : 10.069
Entry
ampl
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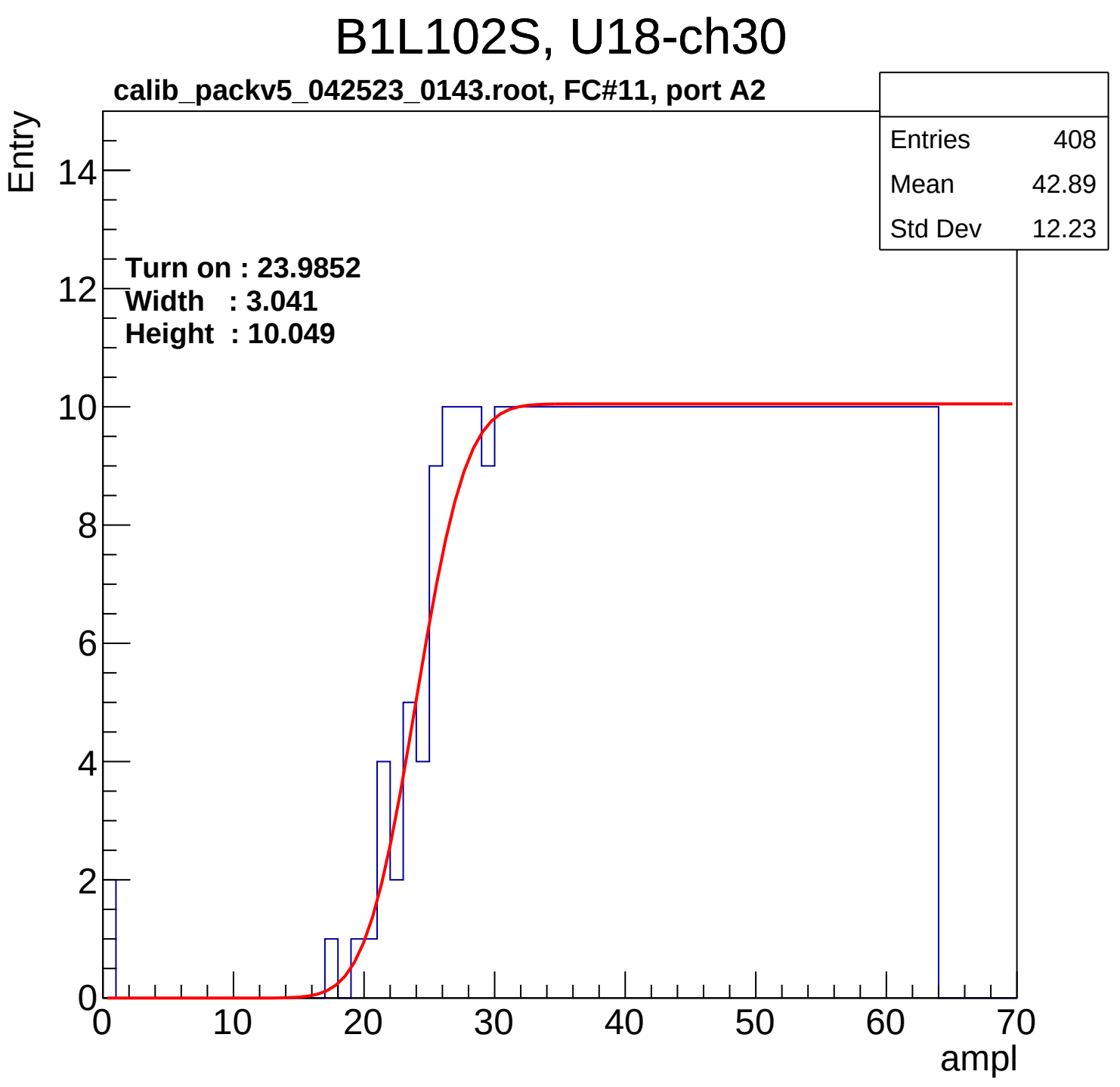
B1L102S, U18-ch30
calib_packv5_042523_0143.root, FC#11, port A2
Entries 408
Mean 42.89
Std Dev 12.23
Turn on : 23.9852
Width : 3.041
Height : 10.049
Entry
ampl
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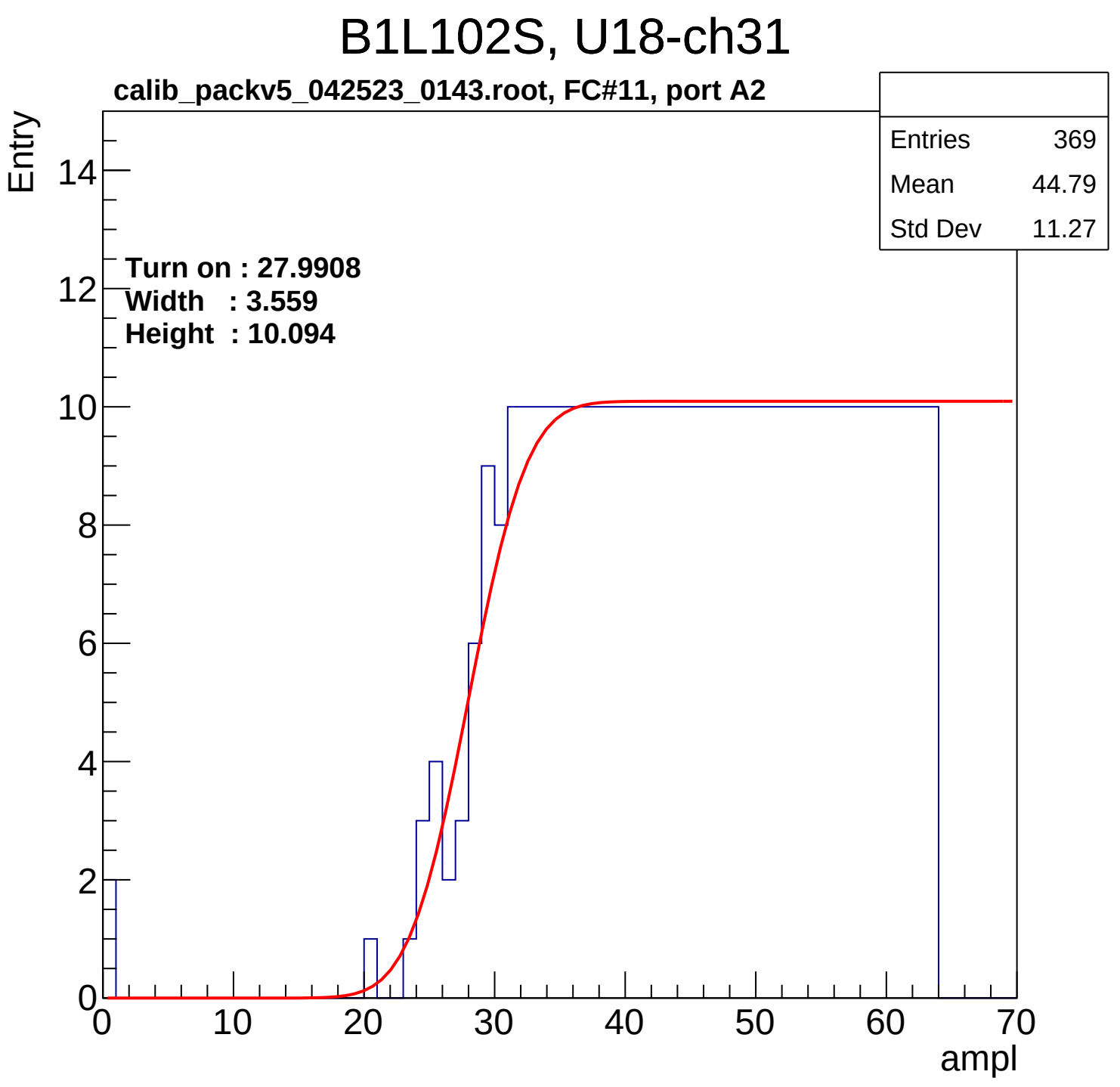
B1L102S, U18-ch31
calib_packv5_042523_0143.root, FC#11, port A2
Entries 369
Mean 44.79
Std Dev 11.27
Turn on : 27.9908
Width : 3.559
Height : 10.094
Entry
ampl
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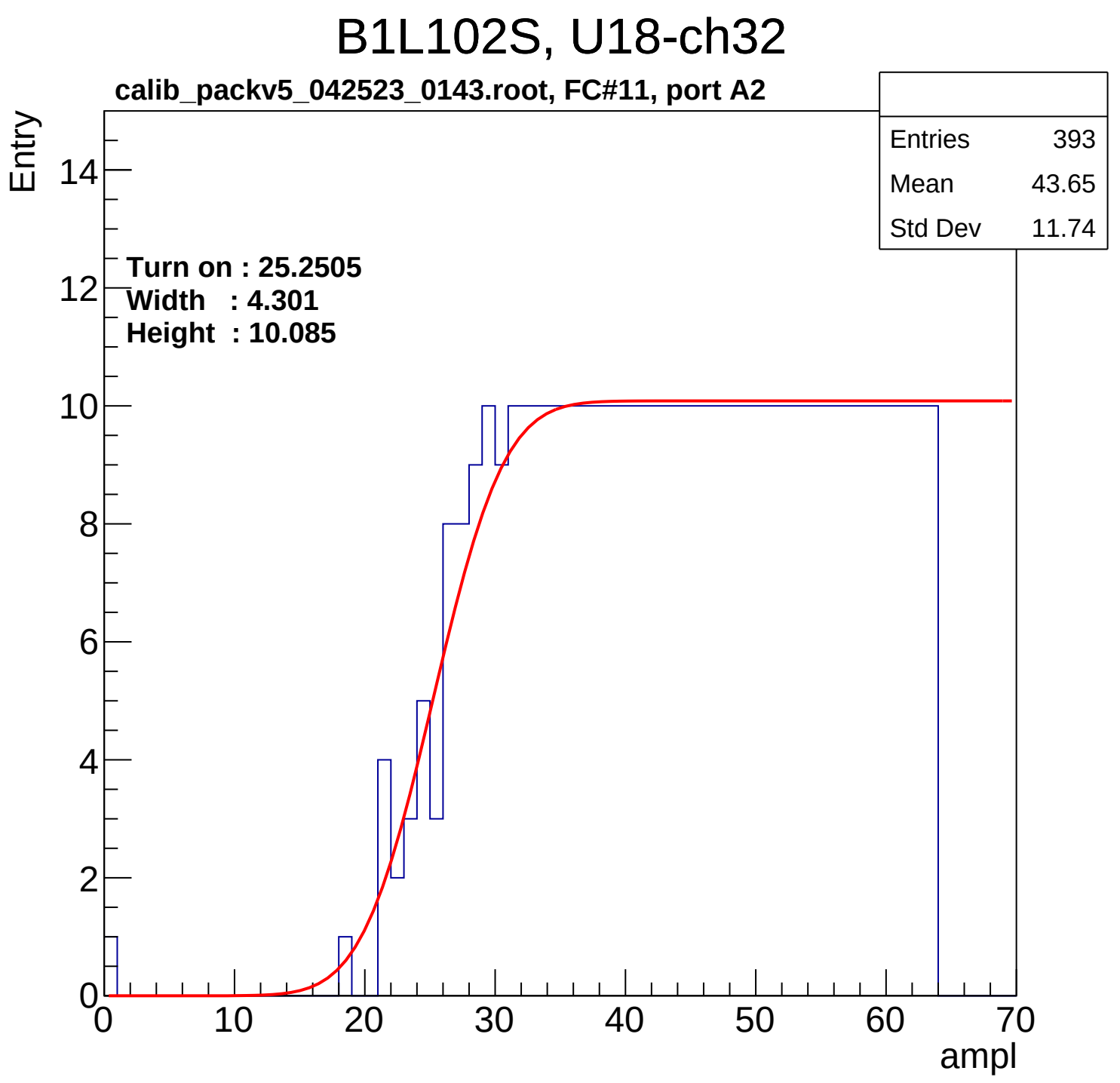
B1L102S, U18-ch32
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.65
Std Dev 11.74
Turn on : 25.2505
Width : 4.301
Height : 10.085
Entry
ampl
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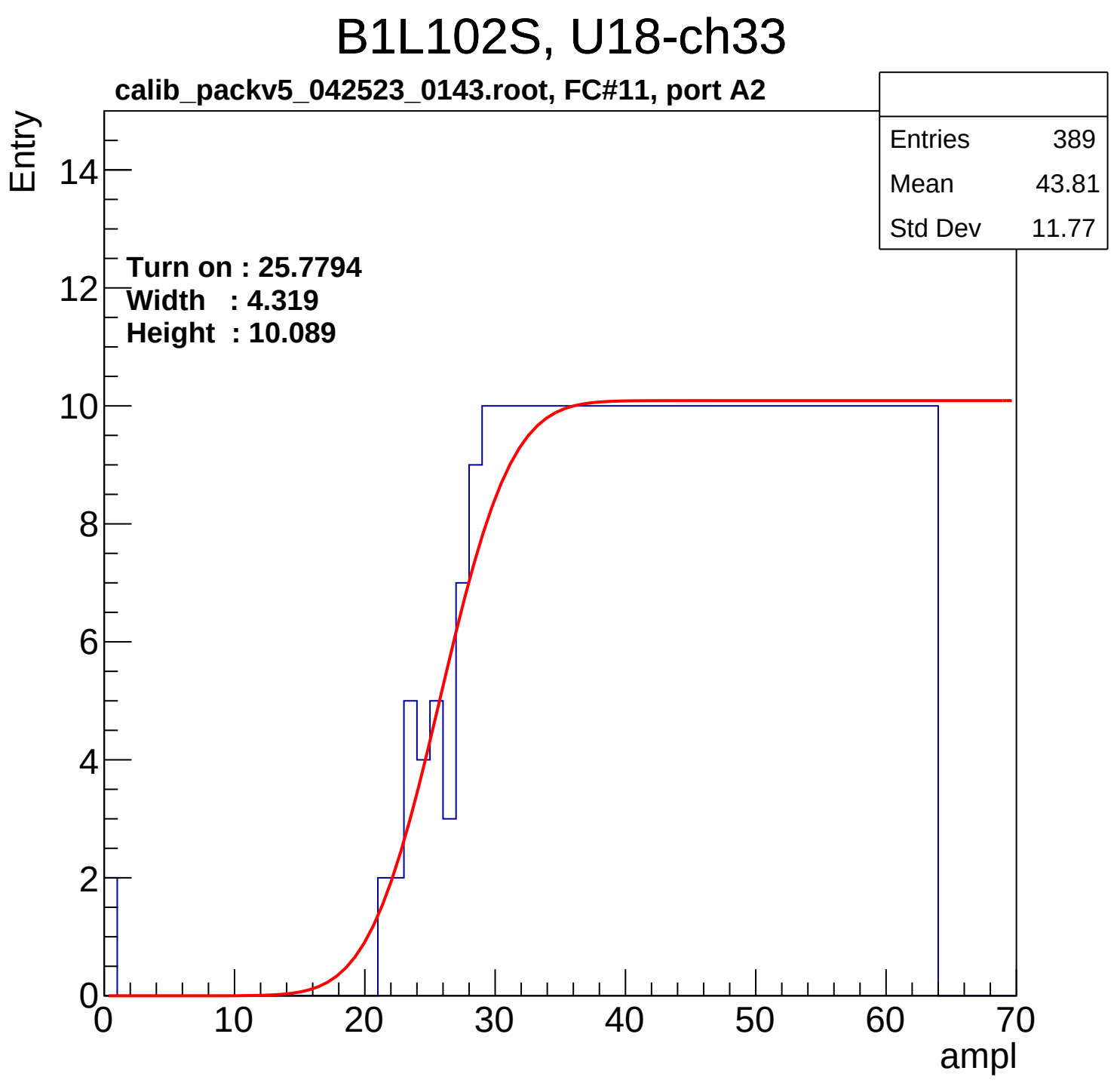
B1L102S, U18-ch33
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.81
Std Dev 11.77
Turn on : 25.7794
Width : 4.319
Height : 10.089
Entry
ampl
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2
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6
8
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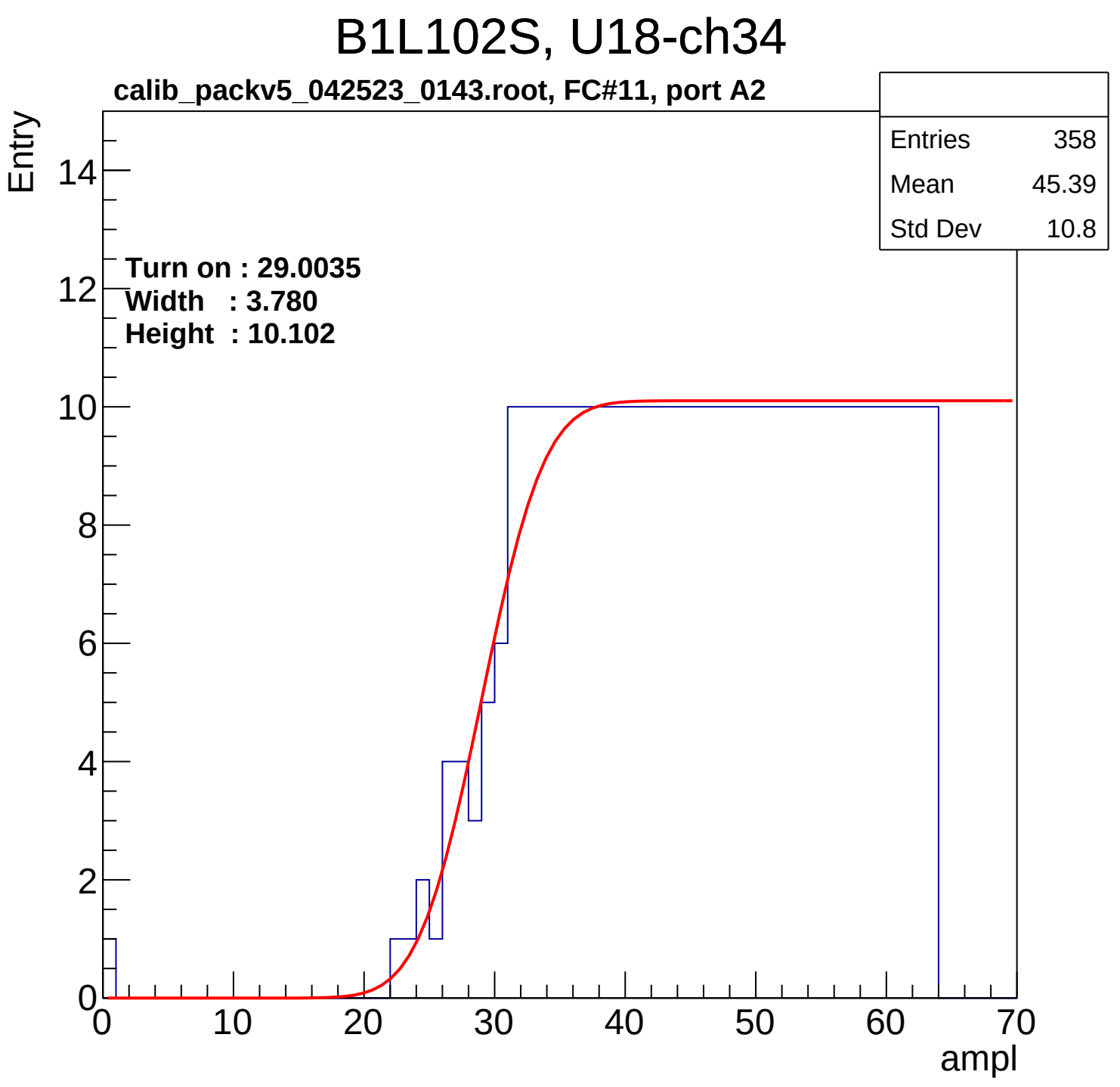
B1L102S, U18-ch34
calib_packv5_042523_0143.root, FC#11, port A2
Entries 358
Mean 45.39
Std Dev 10.8
Turn on : 29.0035
Width : 3.780
Height : 10.102
Entry
ampl
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2
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6
8
10
12
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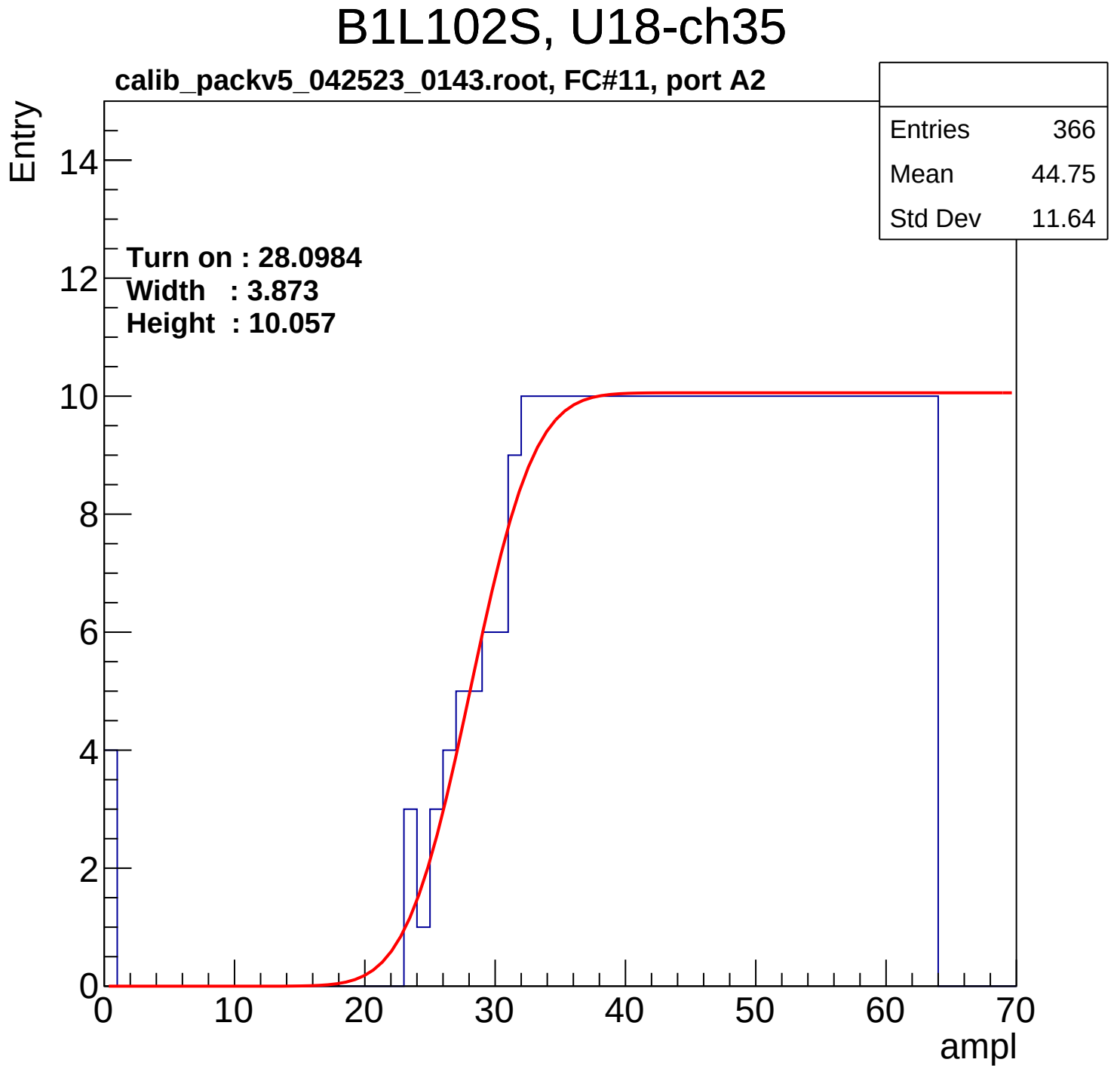
B1L102S, U18-ch35
calib_packv5_042523_0143.root, FC#11, port A2
Entries 366
Mean 44.75
Std Dev 11.64
Turn on : 28.0984
Width : 3.873
Height : 10.057
Entry
ampl
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8
10
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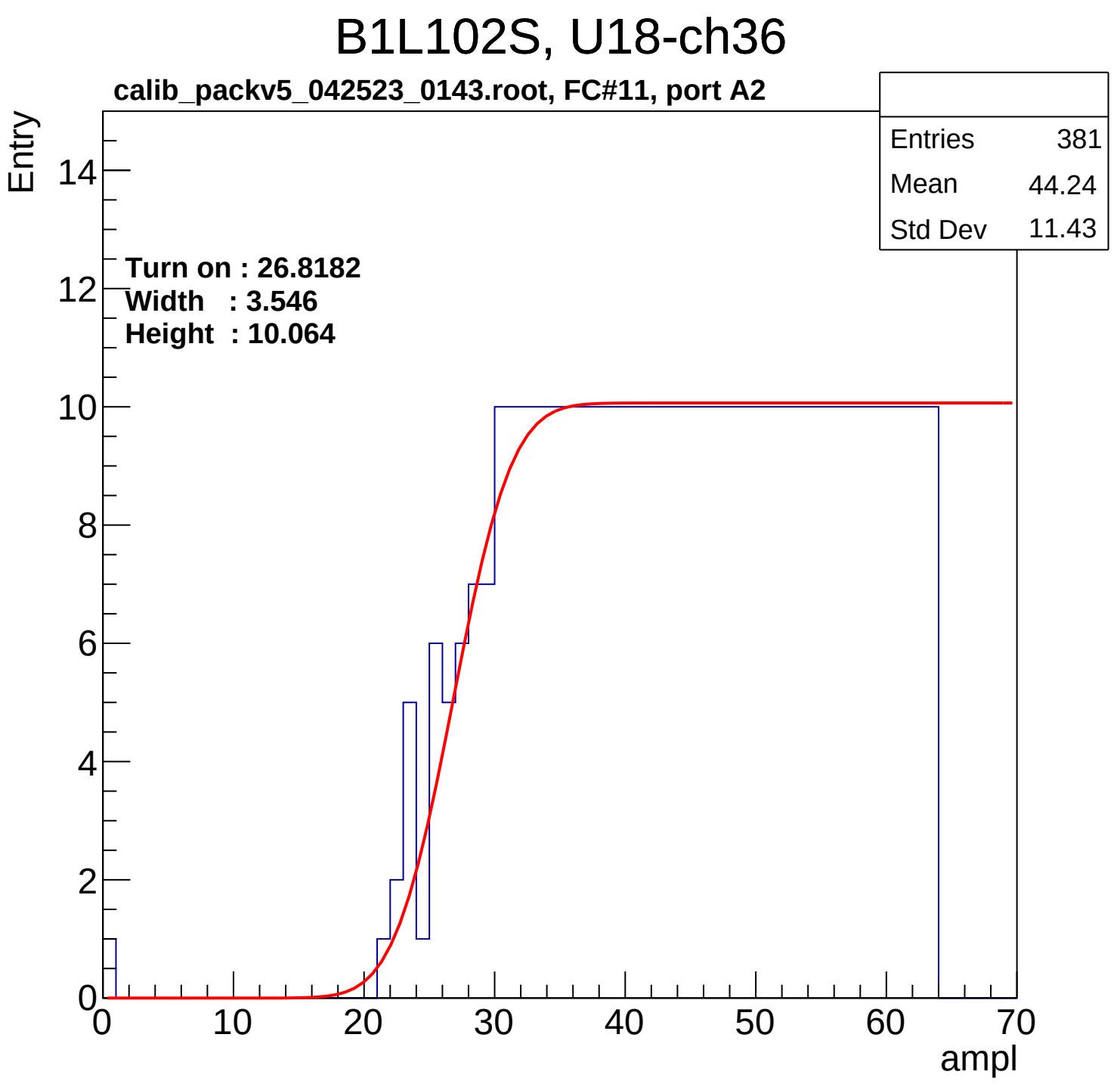
B1L102S, U18-ch36
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.24
Std Dev 11.43
Turn on : 26.8182
Width : 3.546
Height : 10.064
Entry
ampl
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4
6
8
10
12
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0
10
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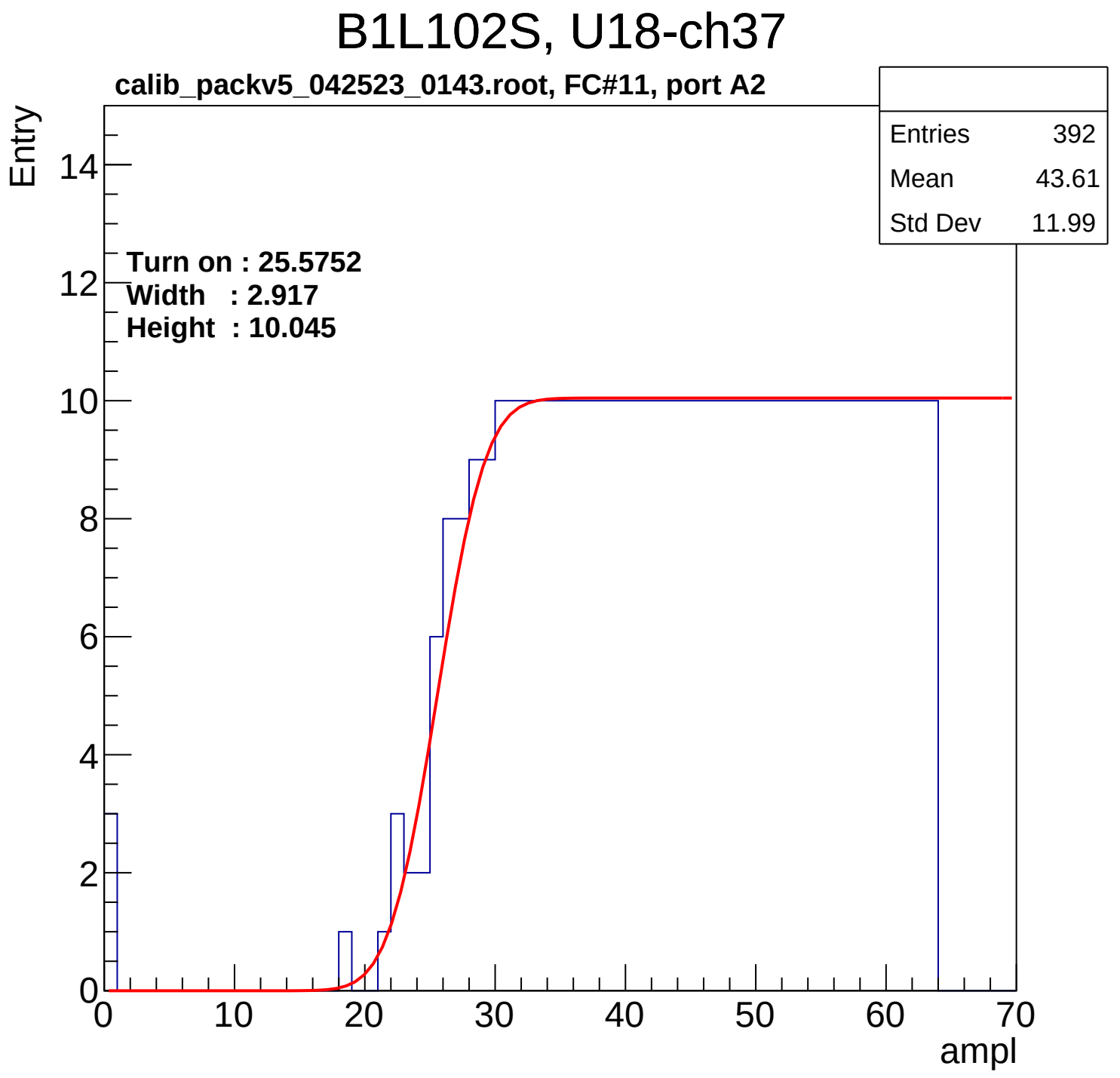
B1L102S, U18-ch37
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.61
Std Dev 11.99
Turn on : 25.5752
Width : 2.917
Height : 10.045
Entry
ampl
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2
4
6
8
10
12
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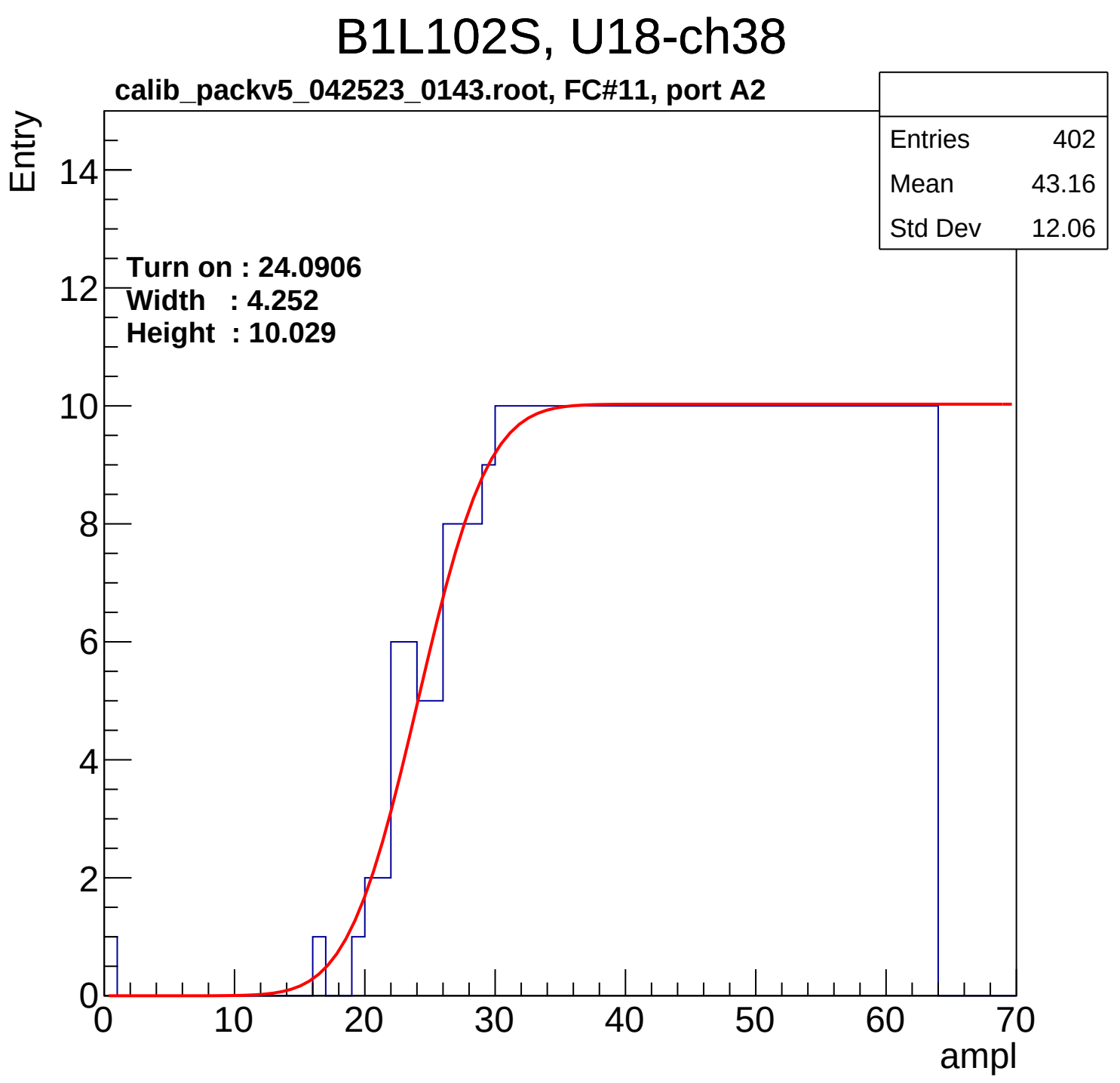
B1L102S, U18-ch38
calib_packv5_042523_0143.root, FC#11, port A2
Entries 402
Mean 43.16
Std Dev 12.06
Turn on : 24.0906
Width : 4.252
Height : 10.029
Entry
ampl
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6
8
10
12
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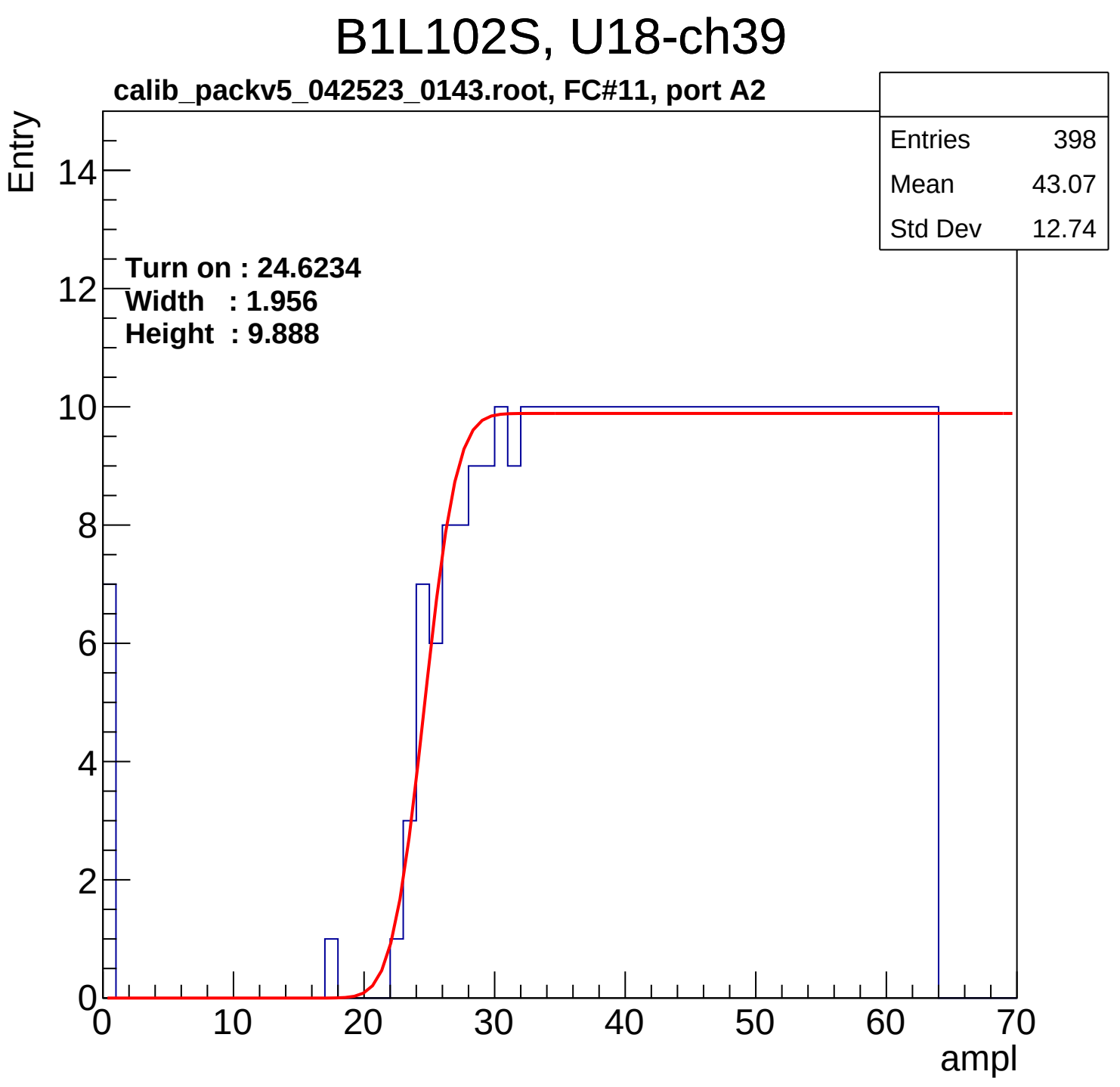
B1L102S, U18-ch39
calib_packv5_042523_0143.root, FC#11, port A2
Entries 398
Mean 43.07
Std Dev 12.74
Turn on : 24.6234
Width : 1.956
Height : 9.888
Entry
ampl
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6
8
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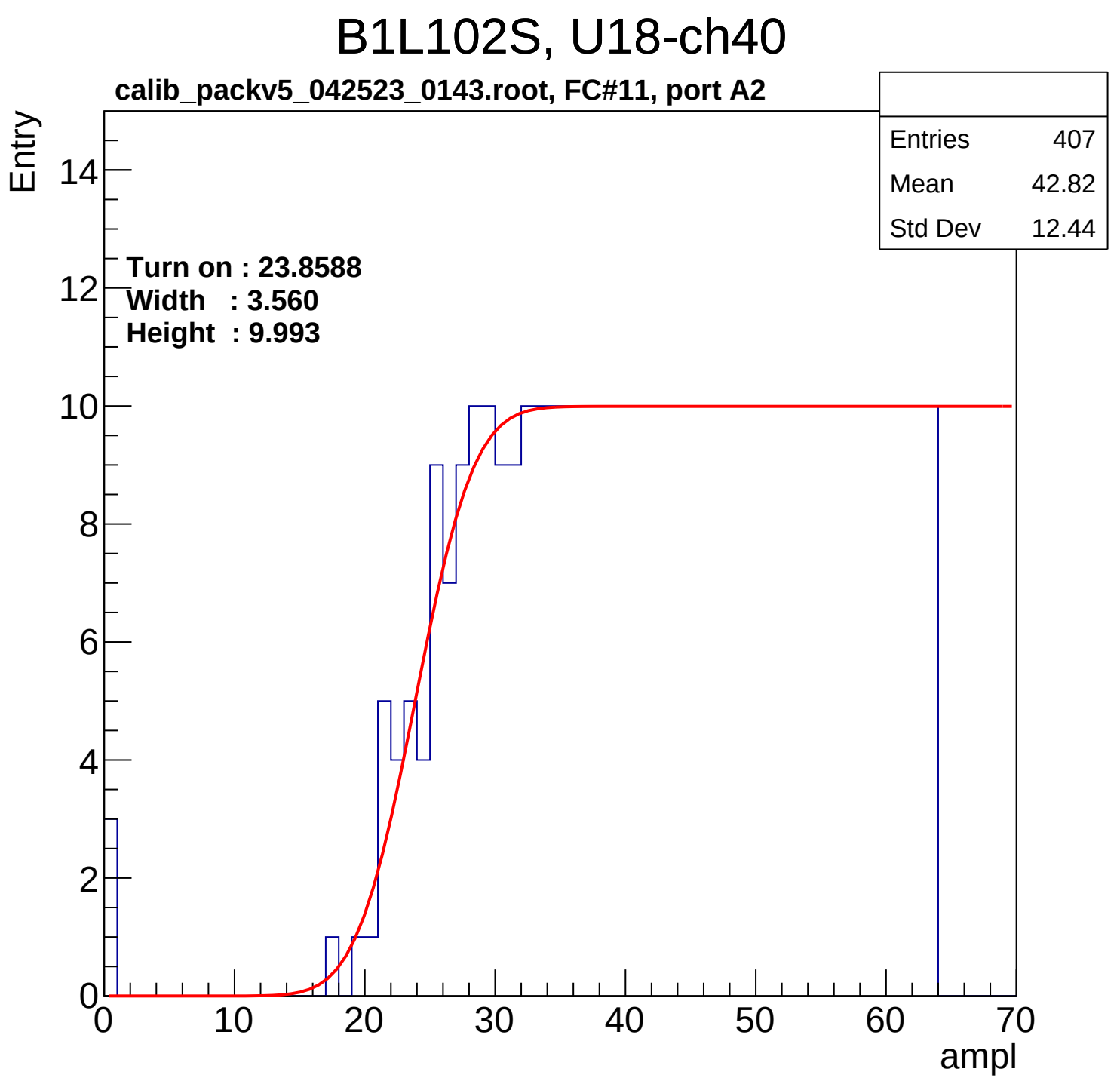
B1L102S, U18-ch40
calib_packv5_042523_0143.root, FC#11, port A2
Entries 407
Mean 42.82
Std Dev 12.44
Turn on : 23.8588
Width : 3.560
Height : 9.993
Entry
ampl
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6
8
10
12
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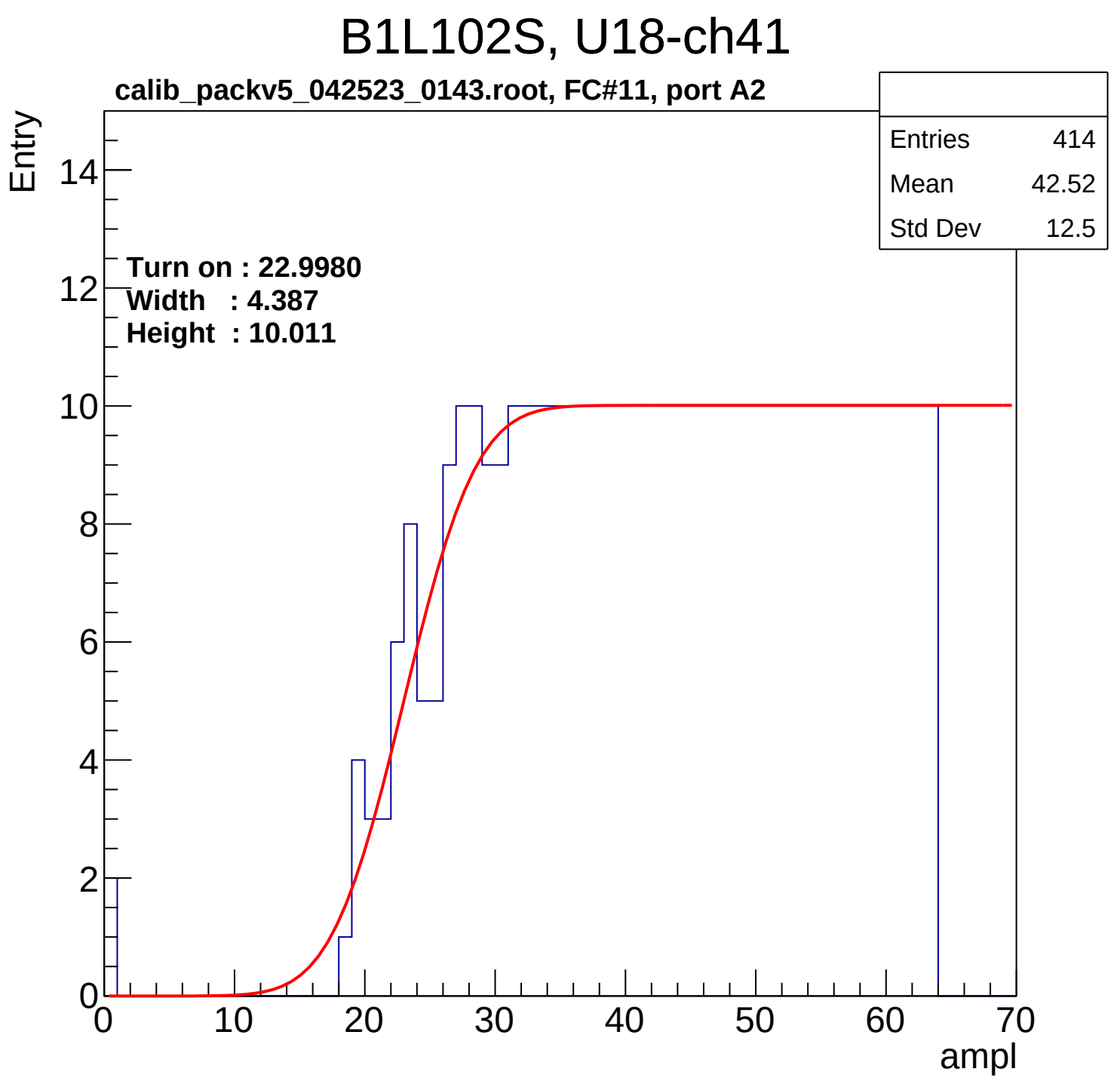
B1L102S, U18-ch41
calib_packv5_042523_0143.root, FC#11, port A2
Entries 414
Mean 42.52
Std Dev 12.5
Turn on : 22.9980
Width : 4.387
Height : 10.011
Entry
ampl
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6
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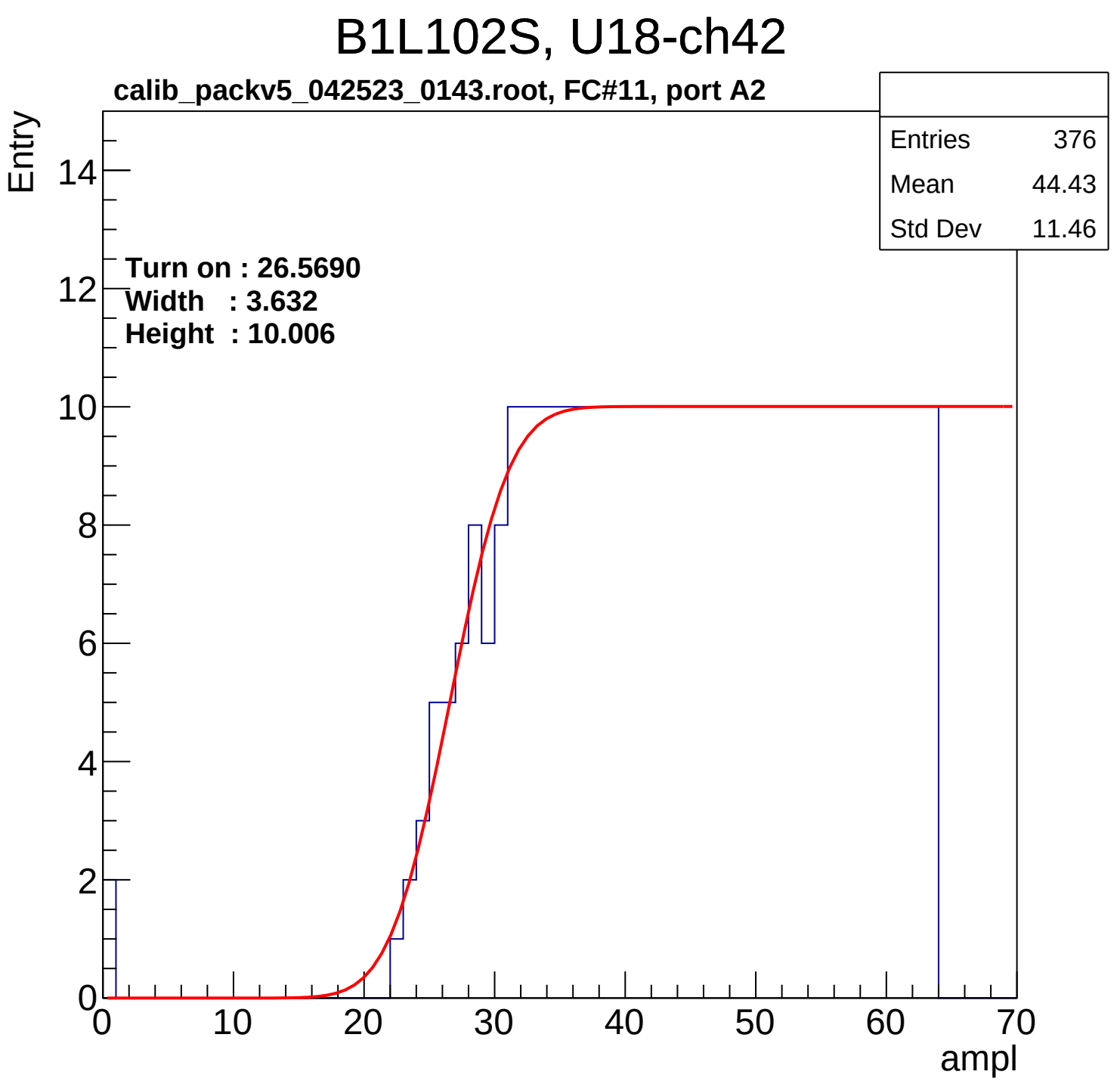
B1L102S, U18-ch42
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.43
Std Dev 11.46
Turn on : 26.5690
Width : 3.632
Height : 10.006
Entry
ampl
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6
8
10
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0
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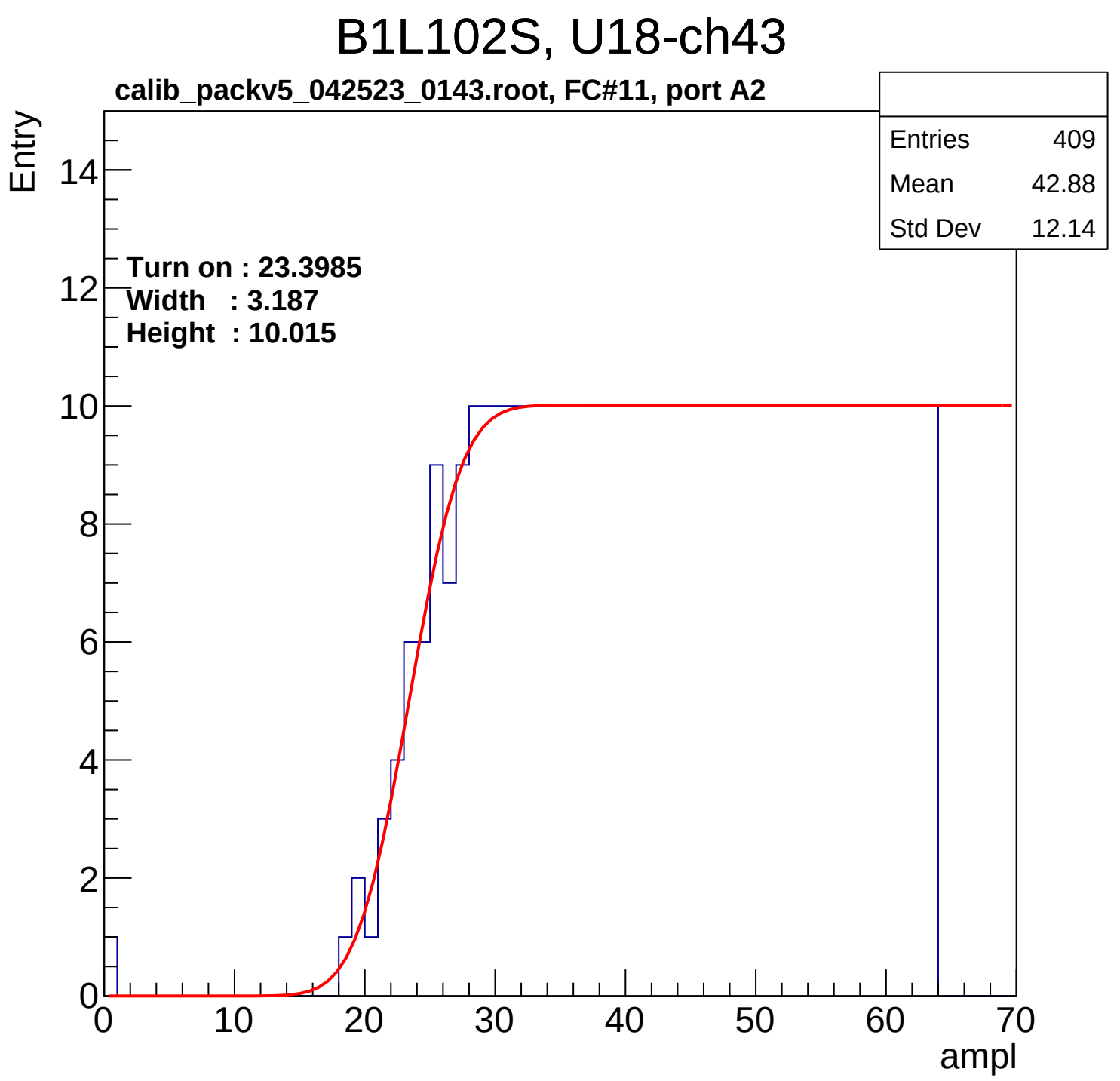
B1L102S, U18-ch43
calib_packv5_042523_0143.root, FC#11, port A2
Entries 409
Mean 42.88
Std Dev 12.14
Turn on : 23.3985
Width : 3.187
Height : 10.015
Entry
ampl
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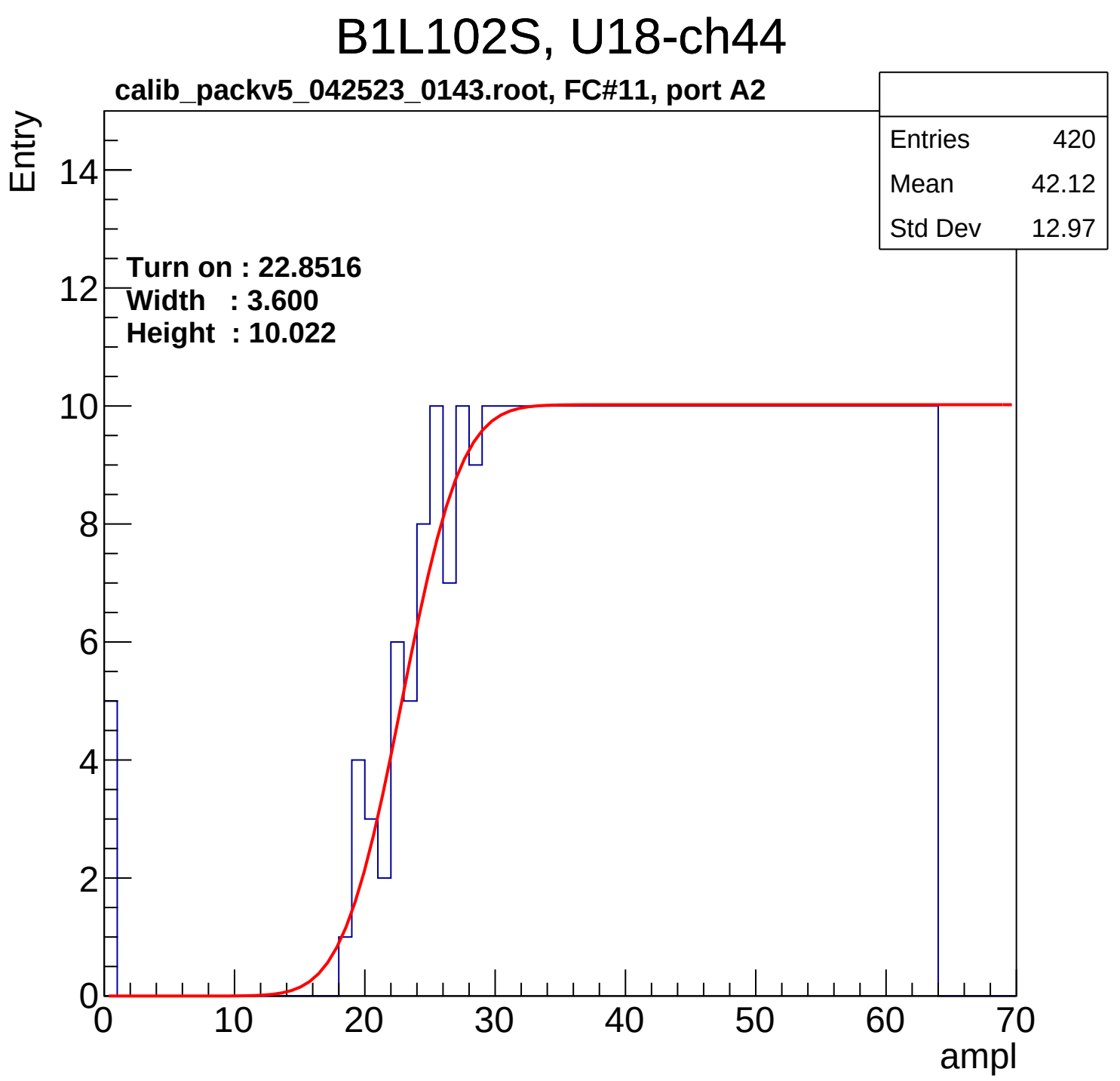
B1L102S, U18-ch44
calib_packv5_042523_0143.root, FC#11, port A2
Entries 420
Mean 42.12
Std Dev 12.97
Turn on : 22.8516
Width : 3.600
Height : 10.022
Entry
ampl
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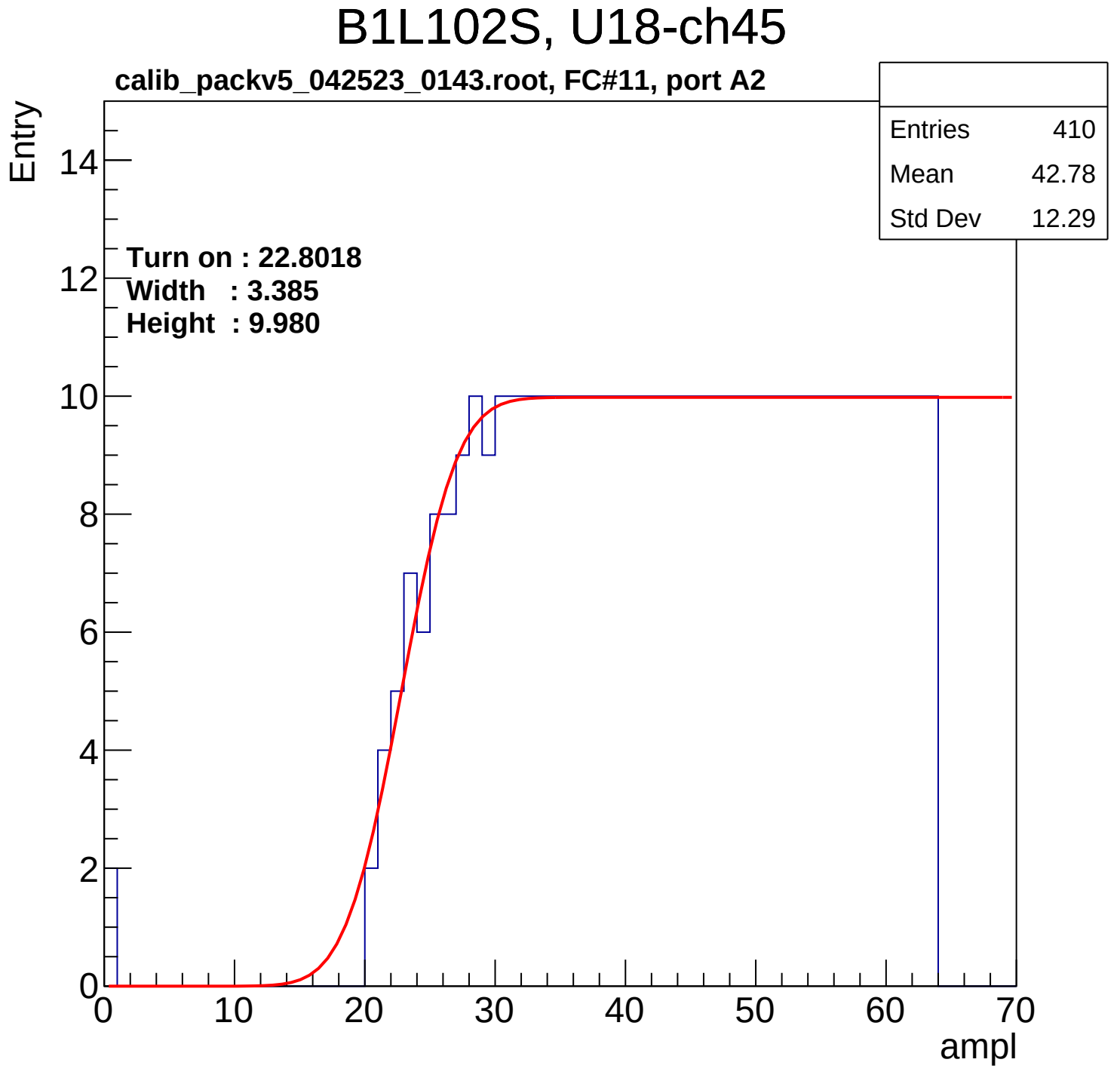
B1L102S, U18-ch45
calib_packv5_042523_0143.root, FC#11, port A2
Entries 410
Mean 42.78
Std Dev 12.29
Turn on : 22.8018
Width : 3.385
Height : 9.980
Entry
ampl
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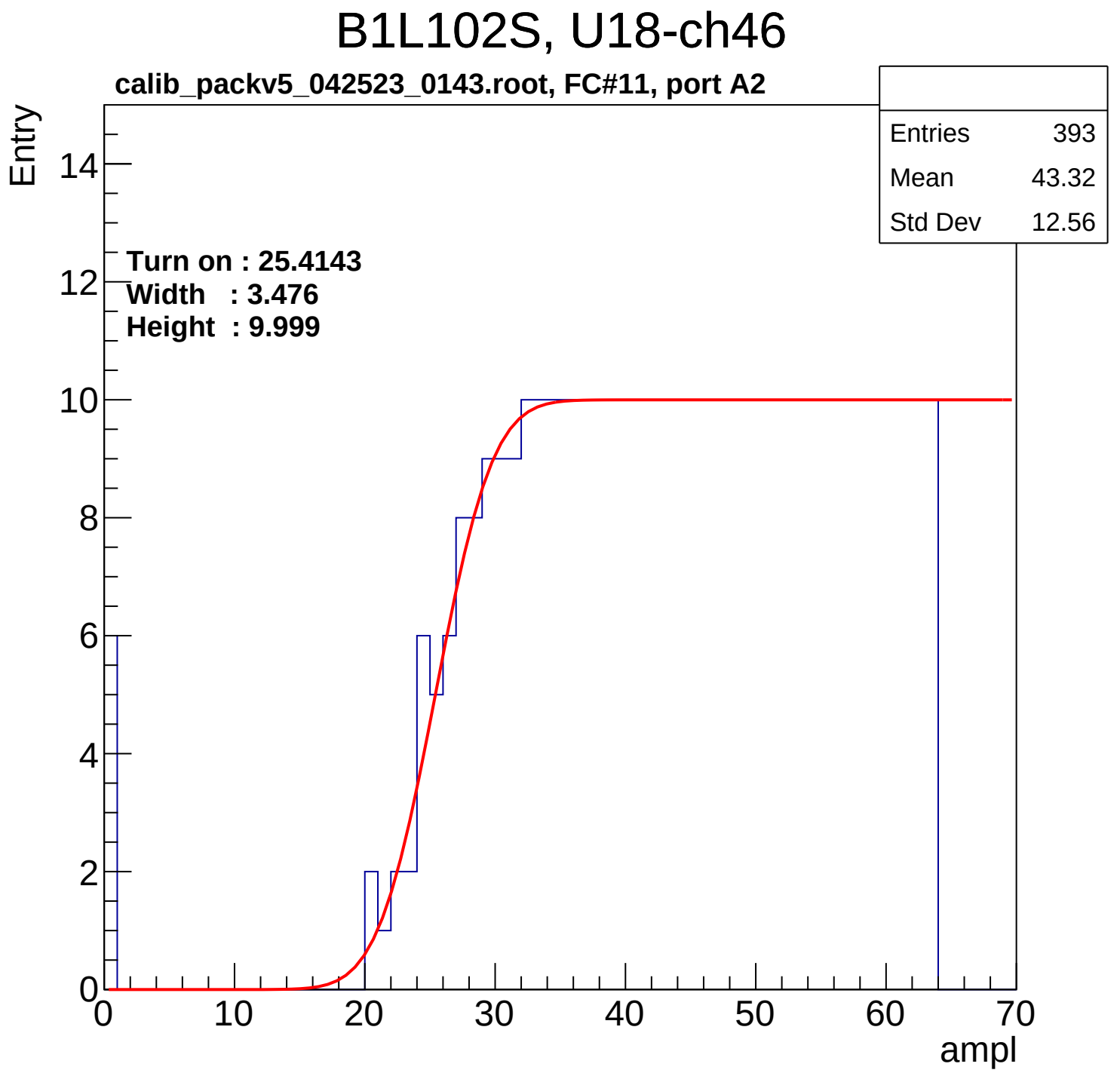
B1L102S, U18-ch46
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.32
Std Dev 12.56
Turn on : 25.4143
Width : 3.476
Height : 9.999
Entry
ampl
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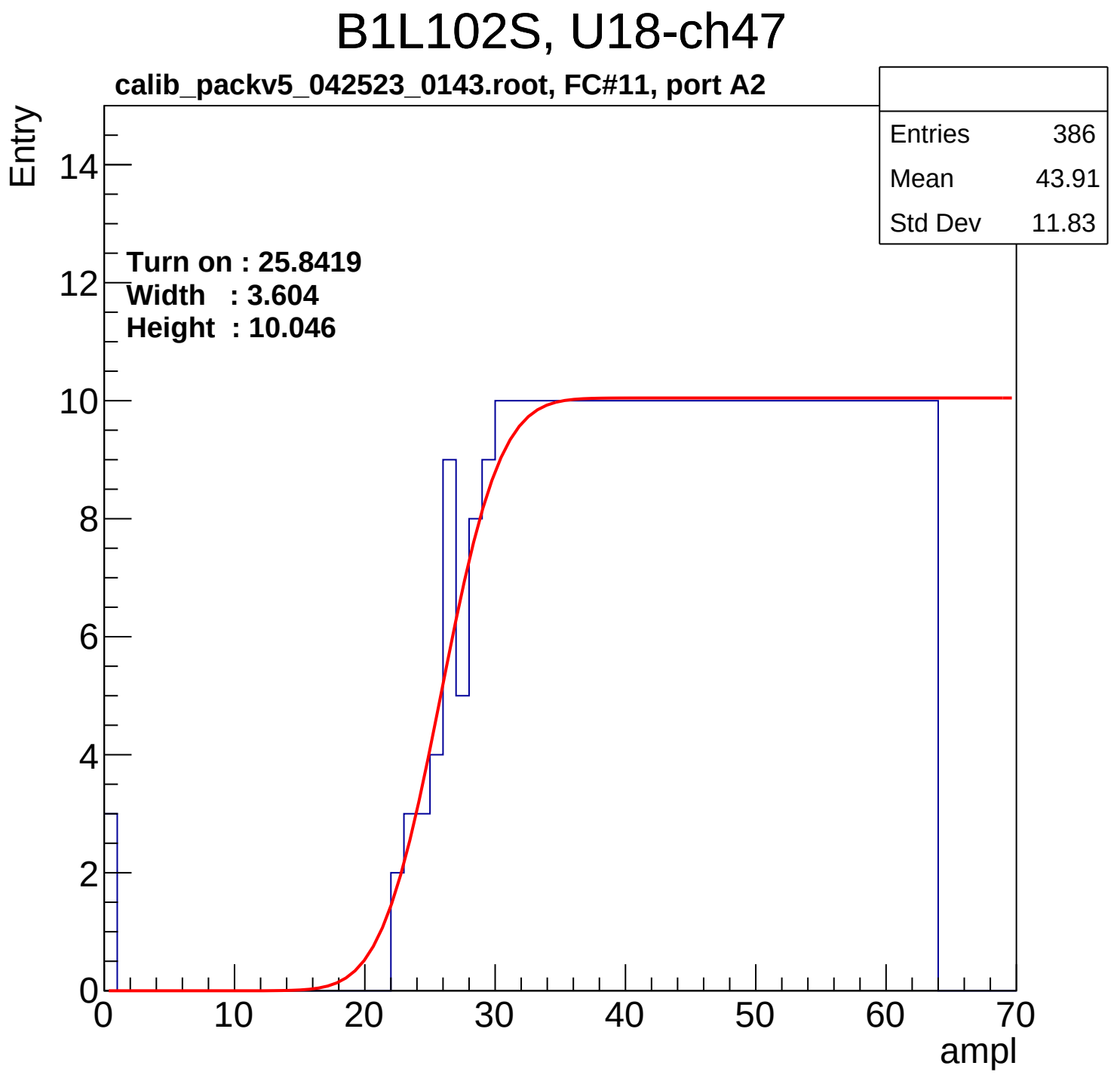
B1L102S, U18-ch47
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.91
Std Dev 11.83
Turn on : 25.8419
Width : 3.604
Height : 10.046
Entry
ampl
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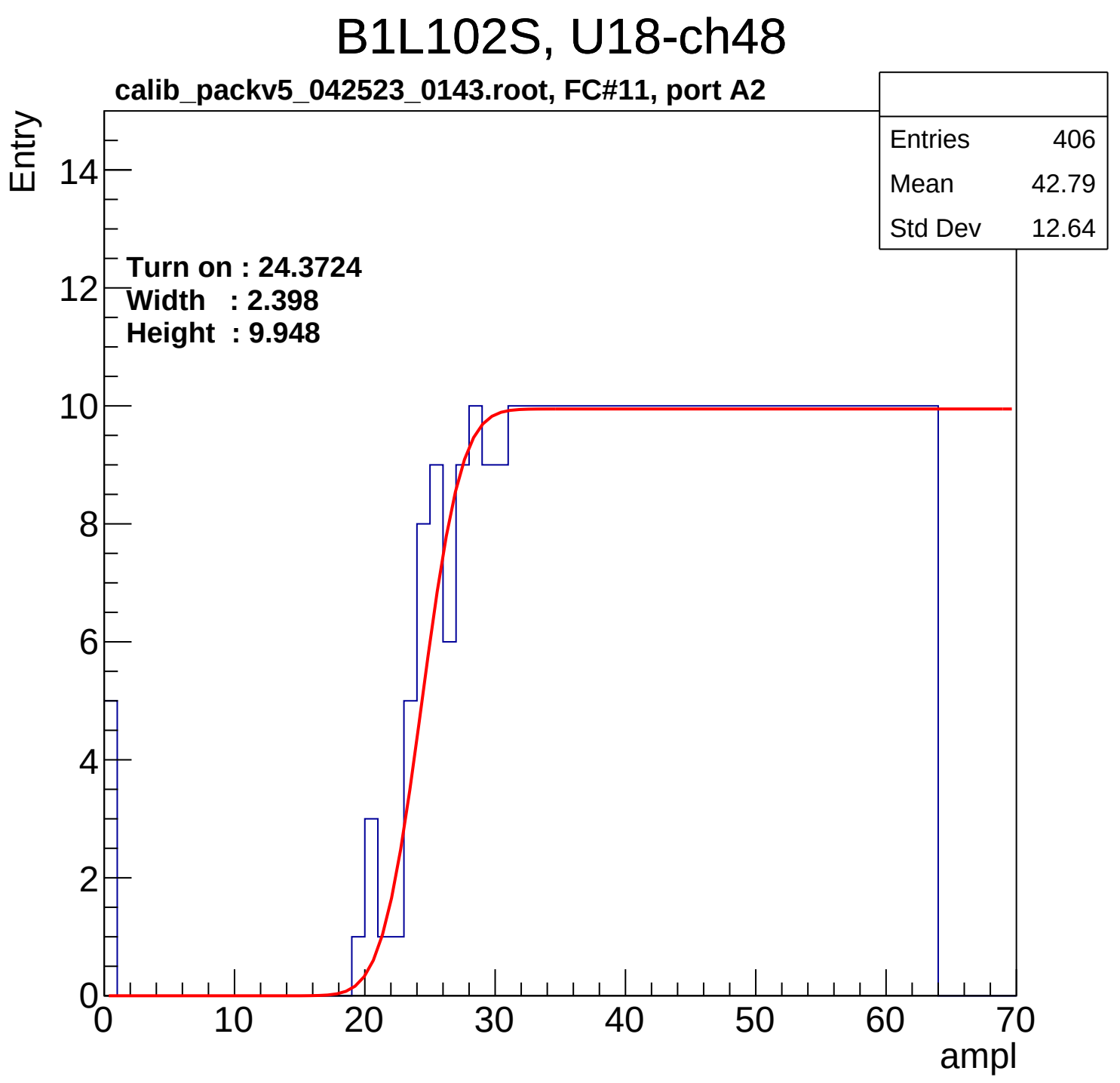
B1L102S, U18-ch48
calib_packv5_042523_0143.root, FC#11, port A2
Entries 406
Mean 42.79
Std Dev 12.64
Turn on : 24.3724
Width : 2.398
Height : 9.948
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ampl
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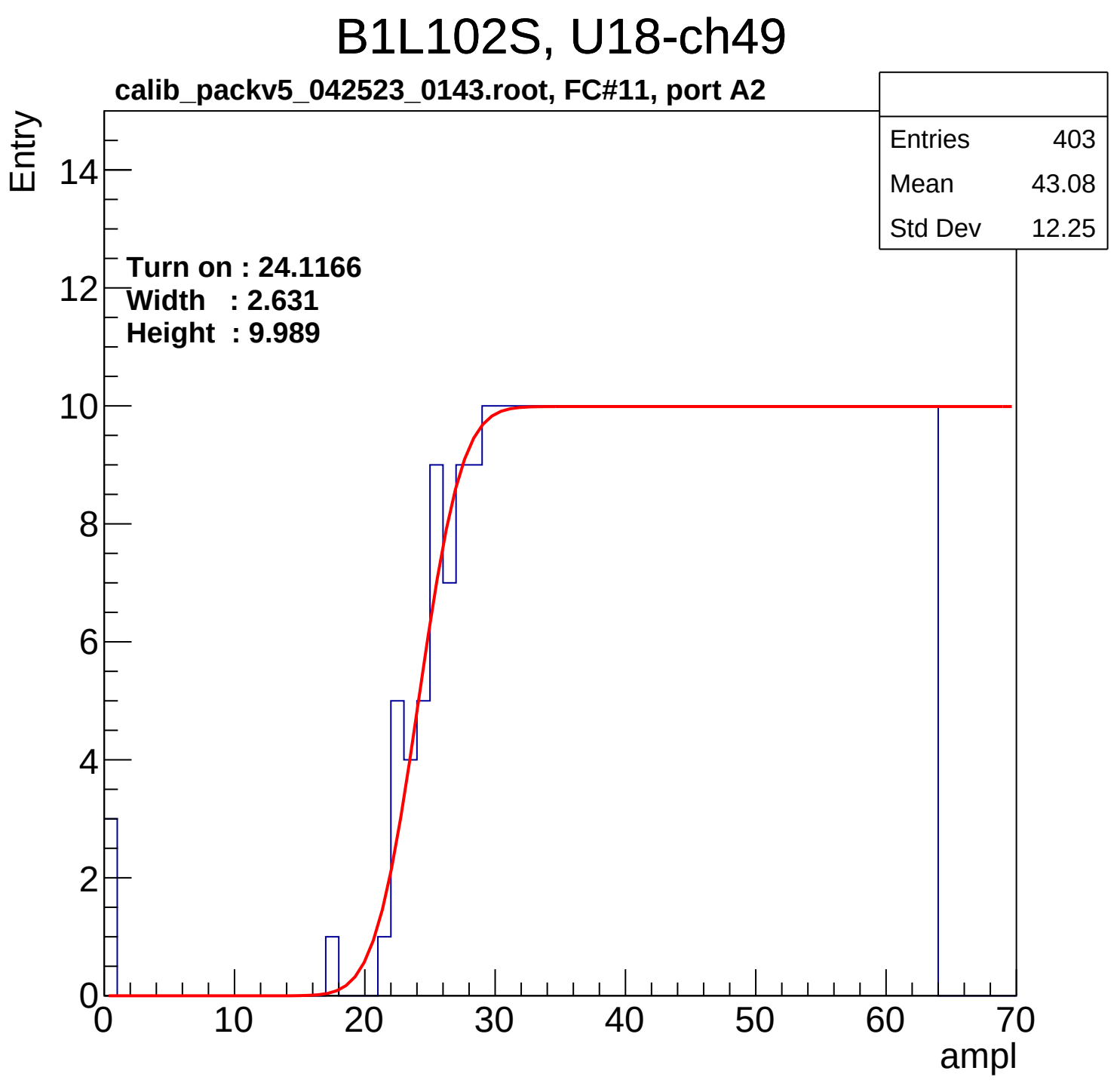
B1L102S, U18-ch49
calib_packv5_042523_0143.root, FC#11, port A2
Entries 403
Mean 43.08
Std Dev 12.25
Turn on : 24.1166
Width : 2.631
Height : 9.989
Entry
ampl
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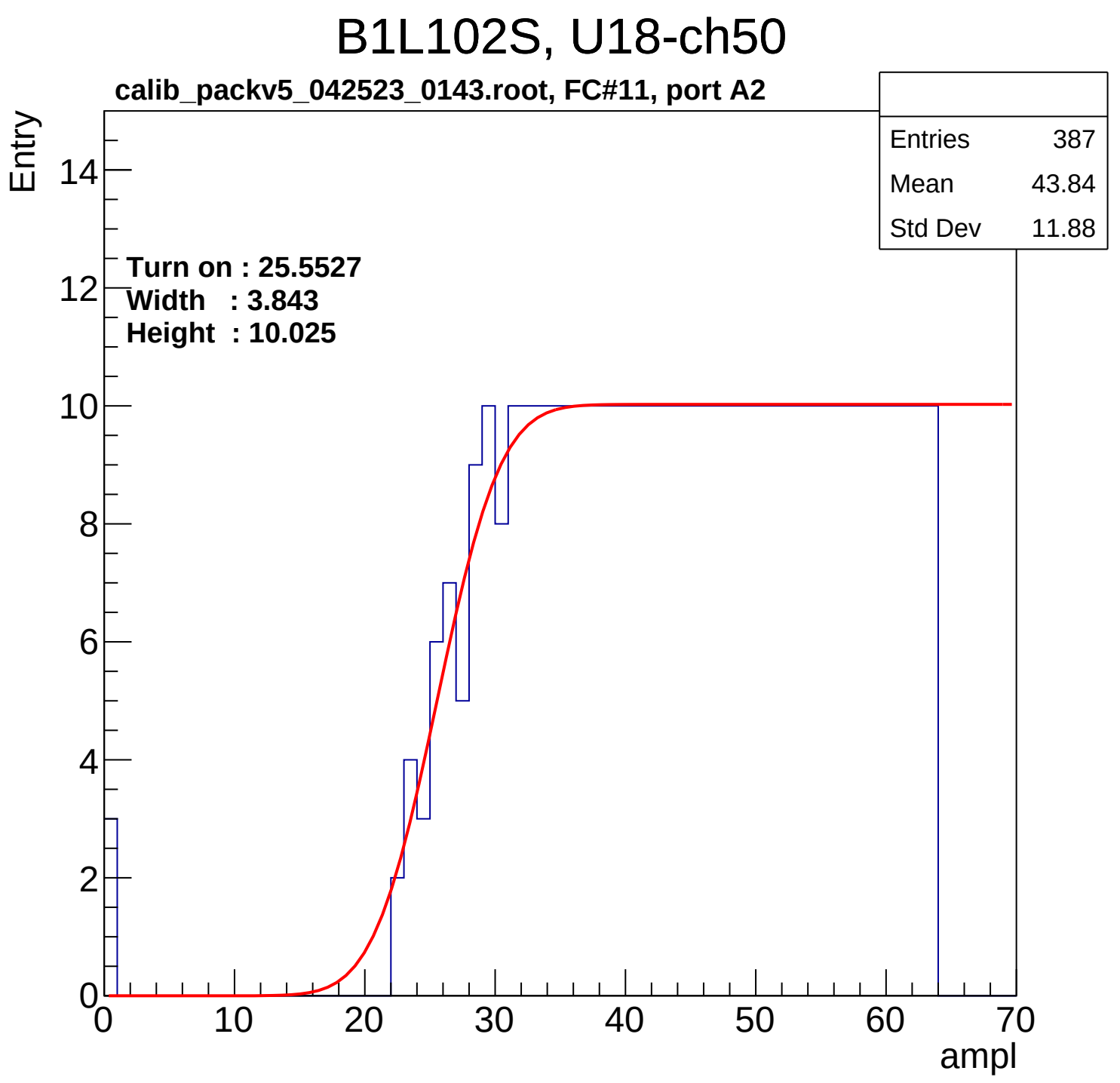
B1L102S, U18-ch50
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.84
Std Dev 11.88
Turn on : 25.5527
Width : 3.843
Height : 10.025
Entry
ampl
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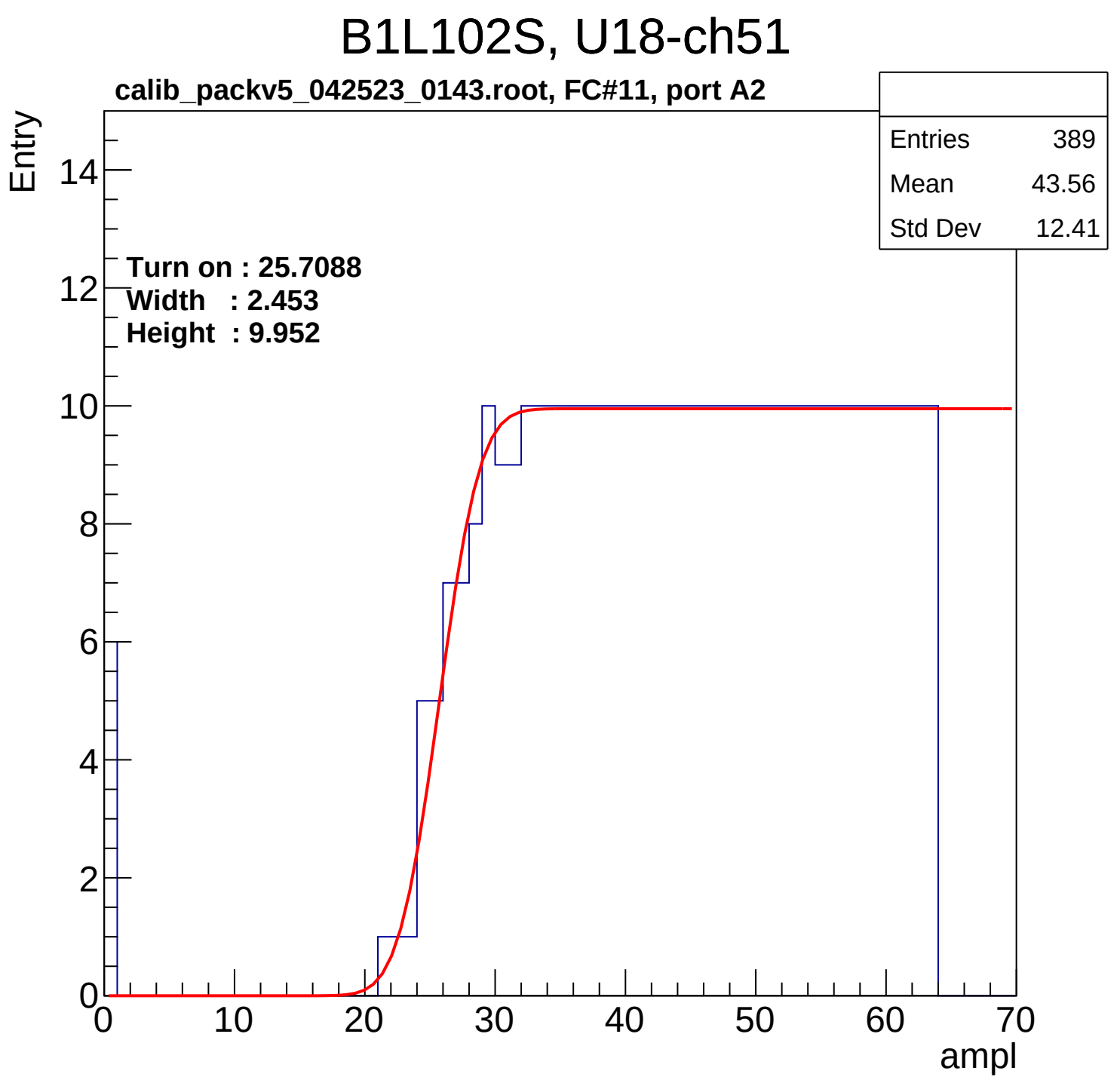
B1L102S, U18-ch51
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.56
Std Dev 12.41
Turn on : 25.7088
Width : 2.453
Height : 9.952
Entry
ampl
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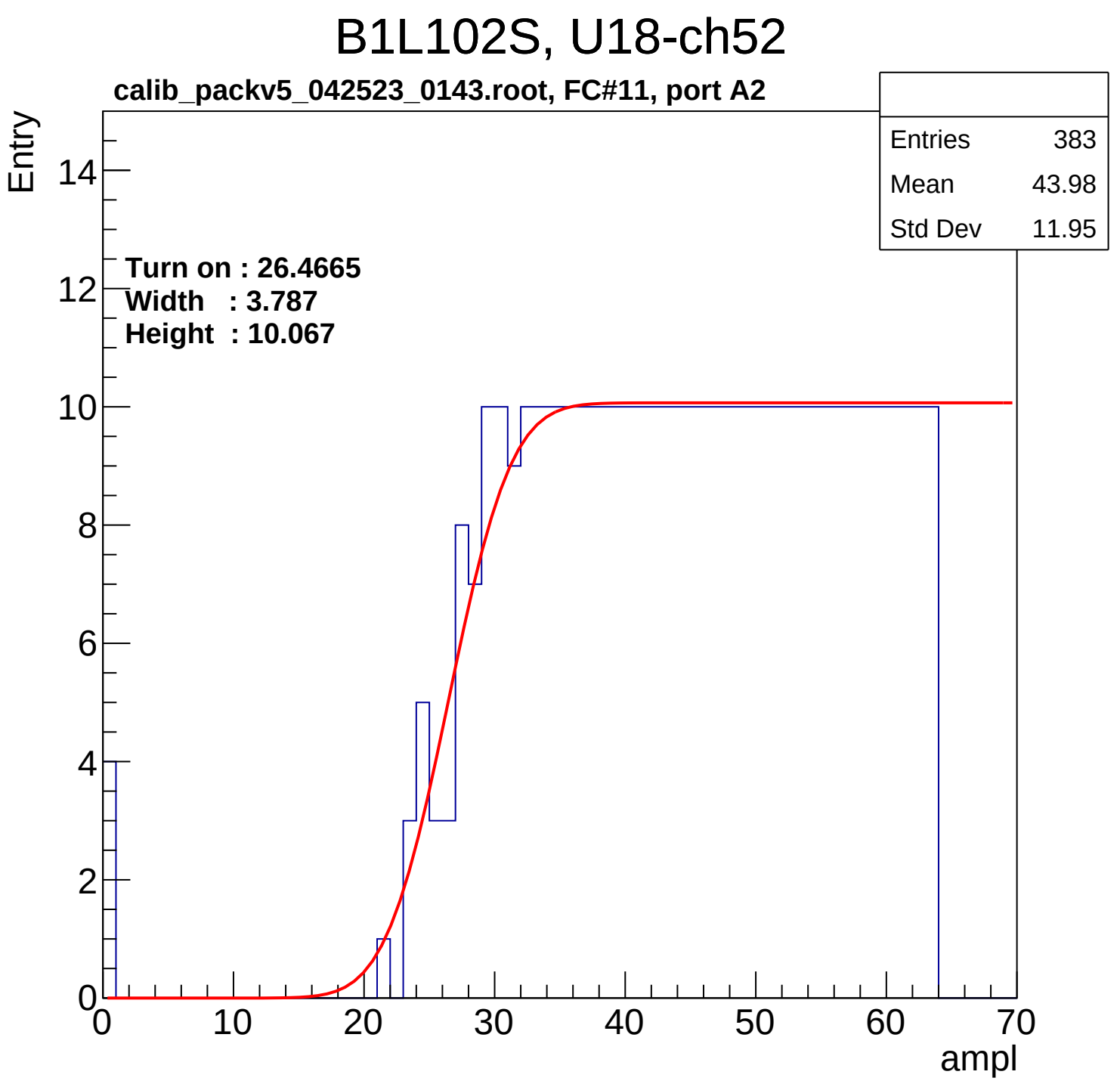
B1L102S, U18-ch52
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 43.98
Std Dev 11.95
Turn on : 26.4665
Width : 3.787
Height : 10.067
Entry
ampl
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6
8
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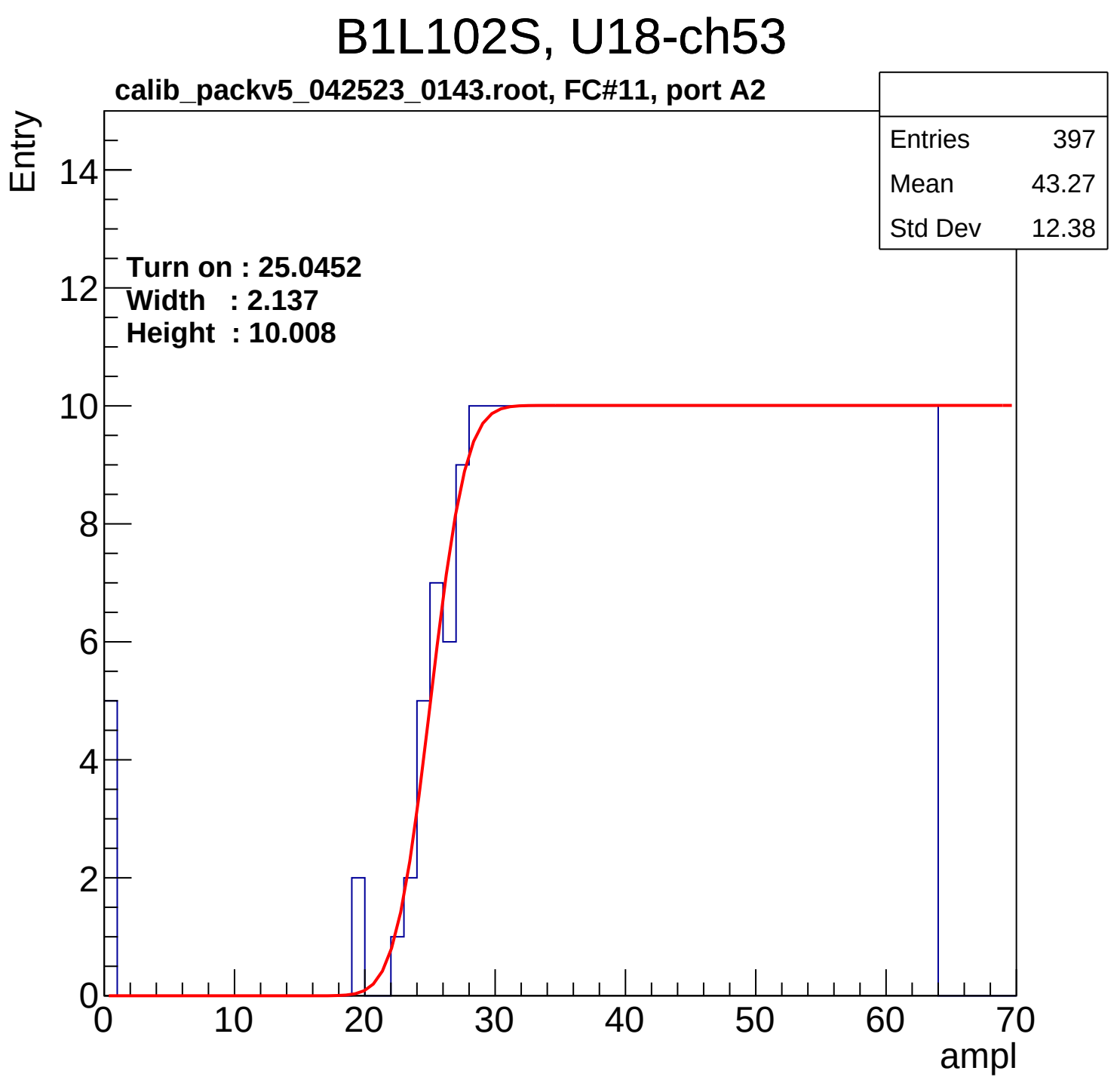
B1L102S, U18-ch53
calib_packv5_042523_0143.root, FC#11, port A2
Entries 397
Mean 43.27
Std Dev 12.38
Turn on : 25.0452
Width : 2.137
Height : 10.008
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ampl
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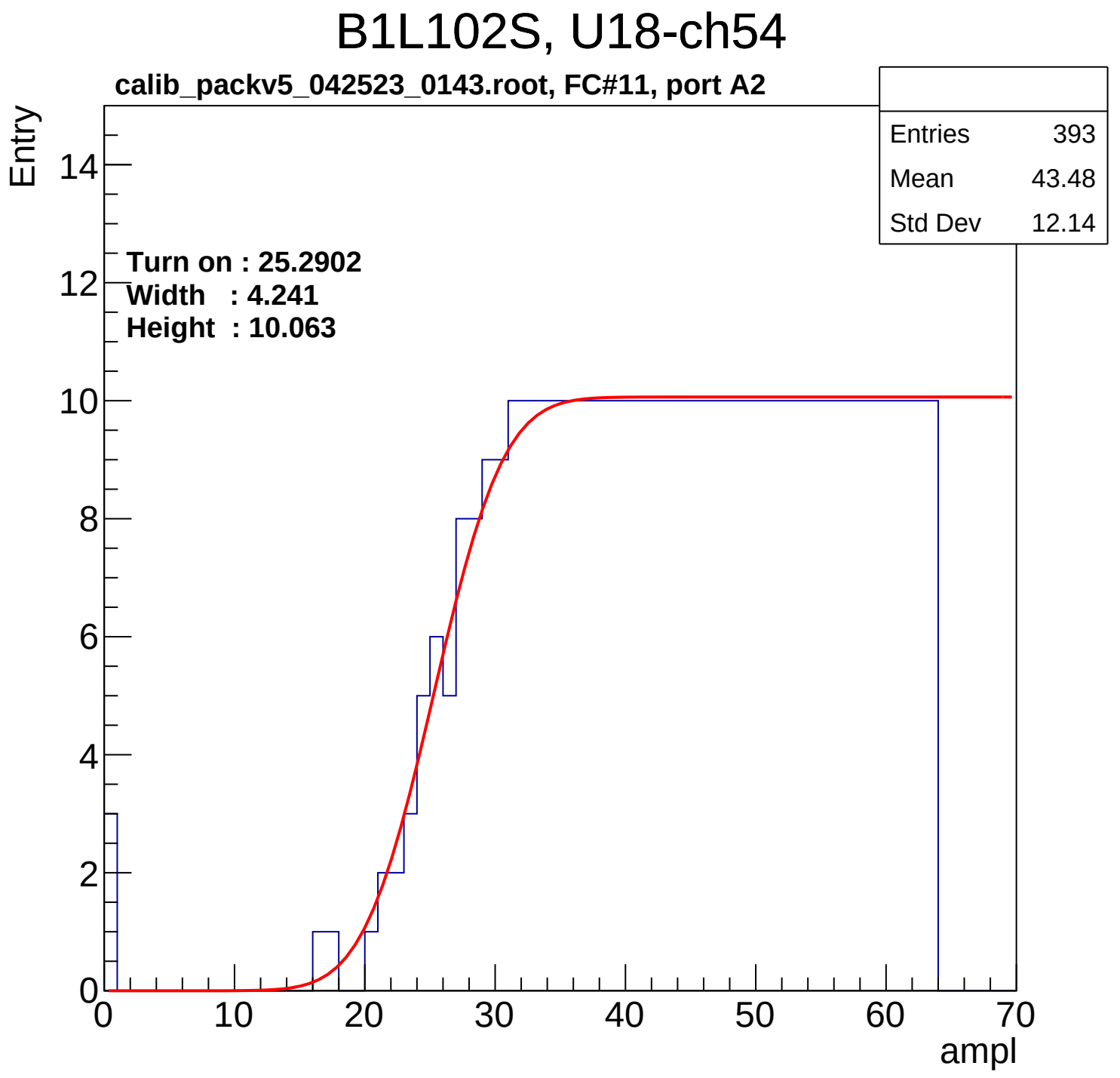
B1L102S, U18-ch54
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.48
Std Dev 12.14
Turn on : 25.2902
Width : 4.241
Height : 10.063
Entry
ampl
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6
8
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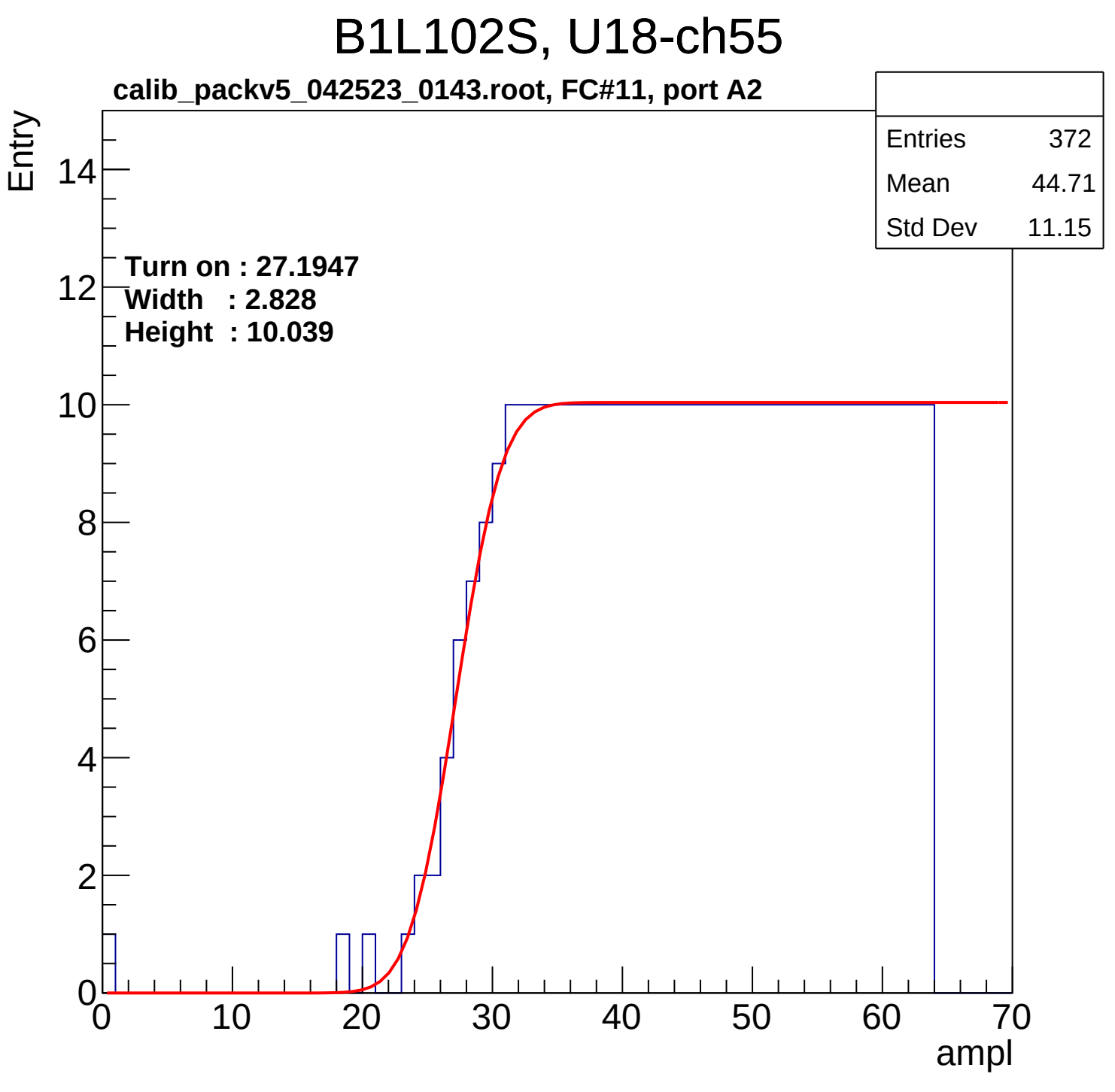
B1L102S, U18-ch55
calib_packv5_042523_0143.root, FC#11, port A2
Entries 372
Mean 44.71
Std Dev 11.15
Turn on : 27.1947
Width : 2.828
Height : 10.039
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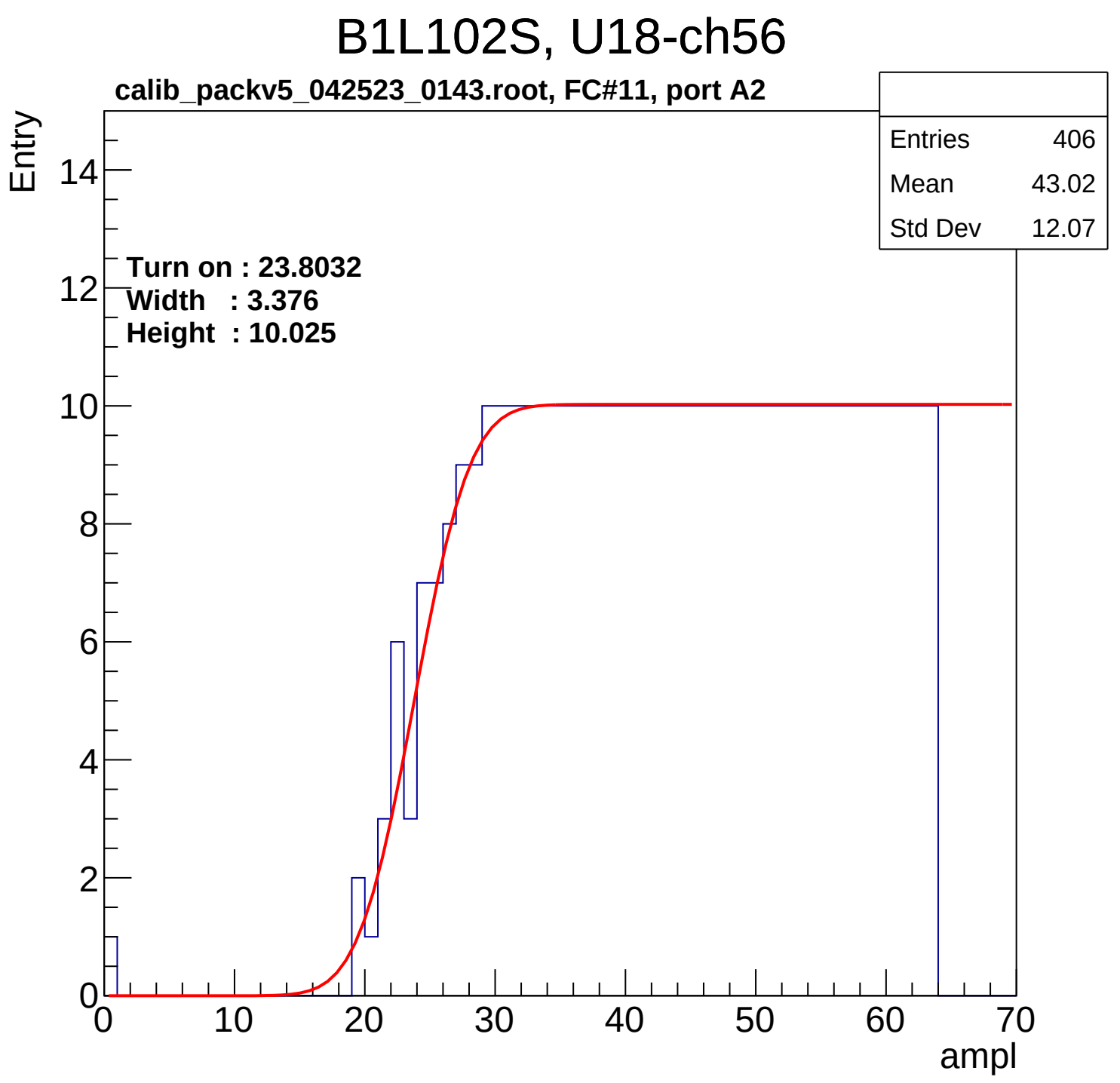
B1L102S, U18-ch56
calib_packv5_042523_0143.root, FC#11, port A2
Entries 406
Mean 43.02
Std Dev 12.07
Turn on : 23.8032
Width : 3.376
Height : 10.025
Entry
ampl
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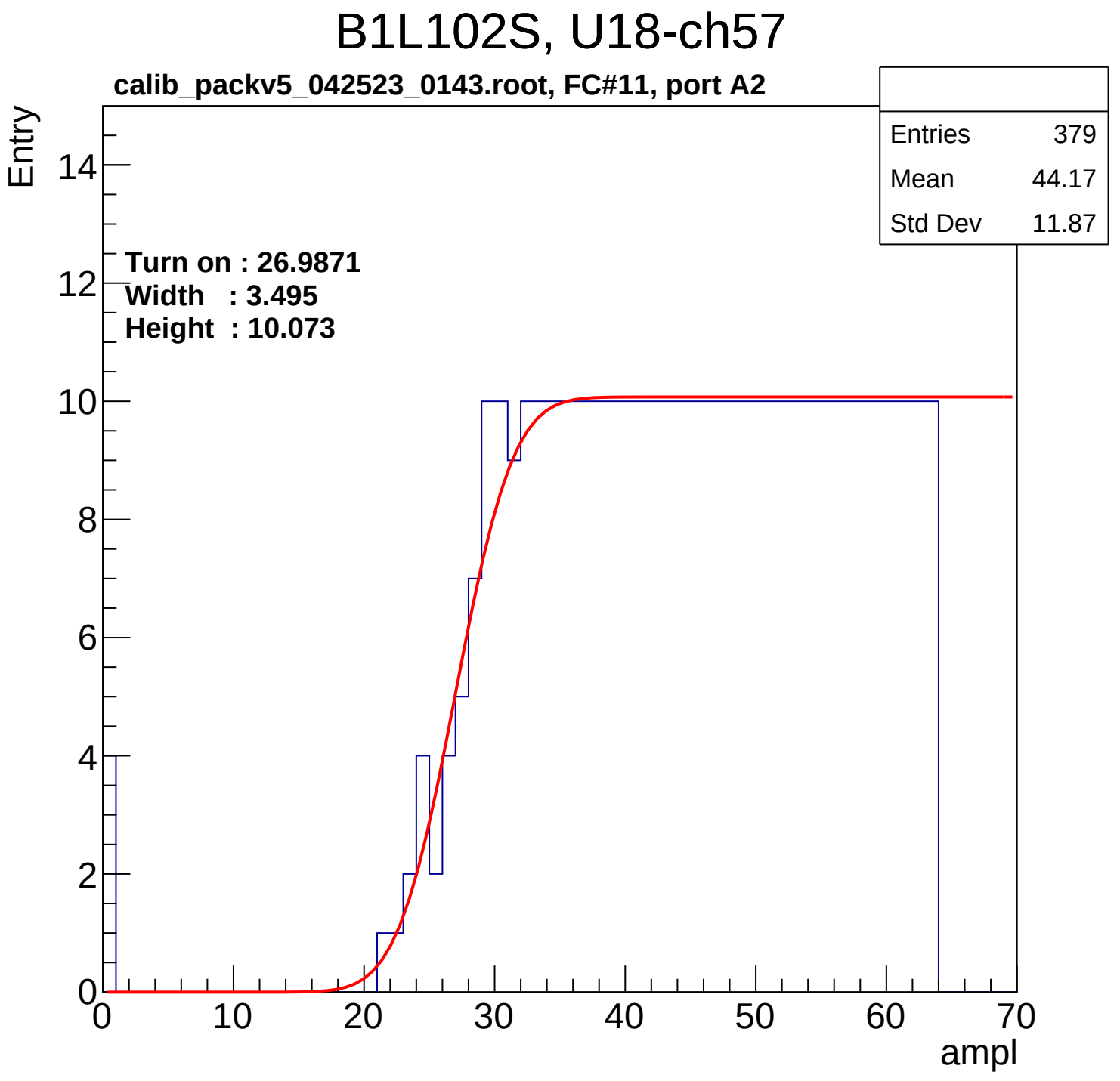
B1L102S, U18-ch57
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.17
Std Dev 11.87
Turn on : 26.9871
Width : 3.495
Height : 10.073
Entry
ampl
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4
6
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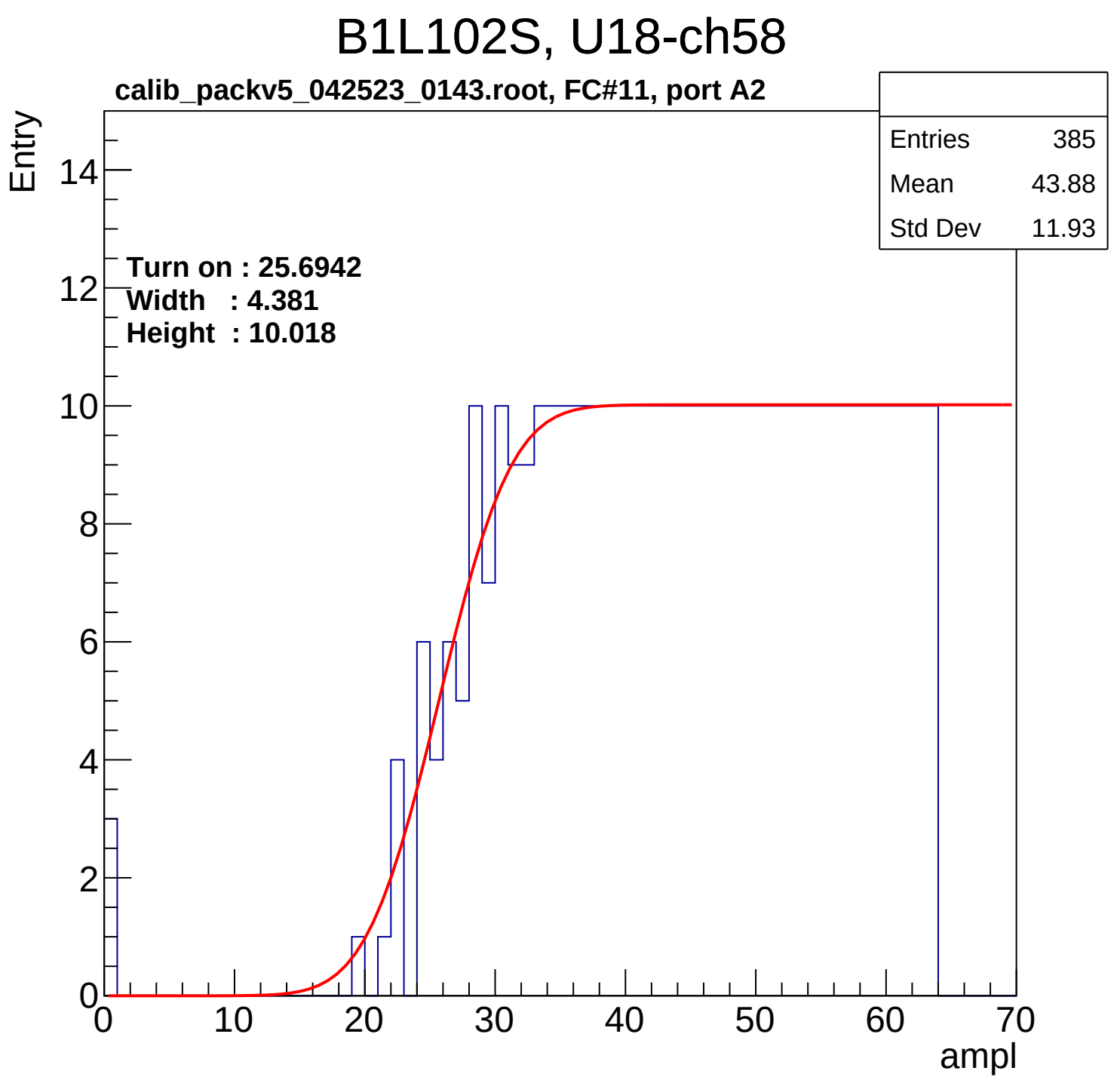
B1L102S, U18-ch58
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.88
Std Dev 11.93
Turn on : 25.6942
Width : 4.381
Height : 10.018
Entry
ampl
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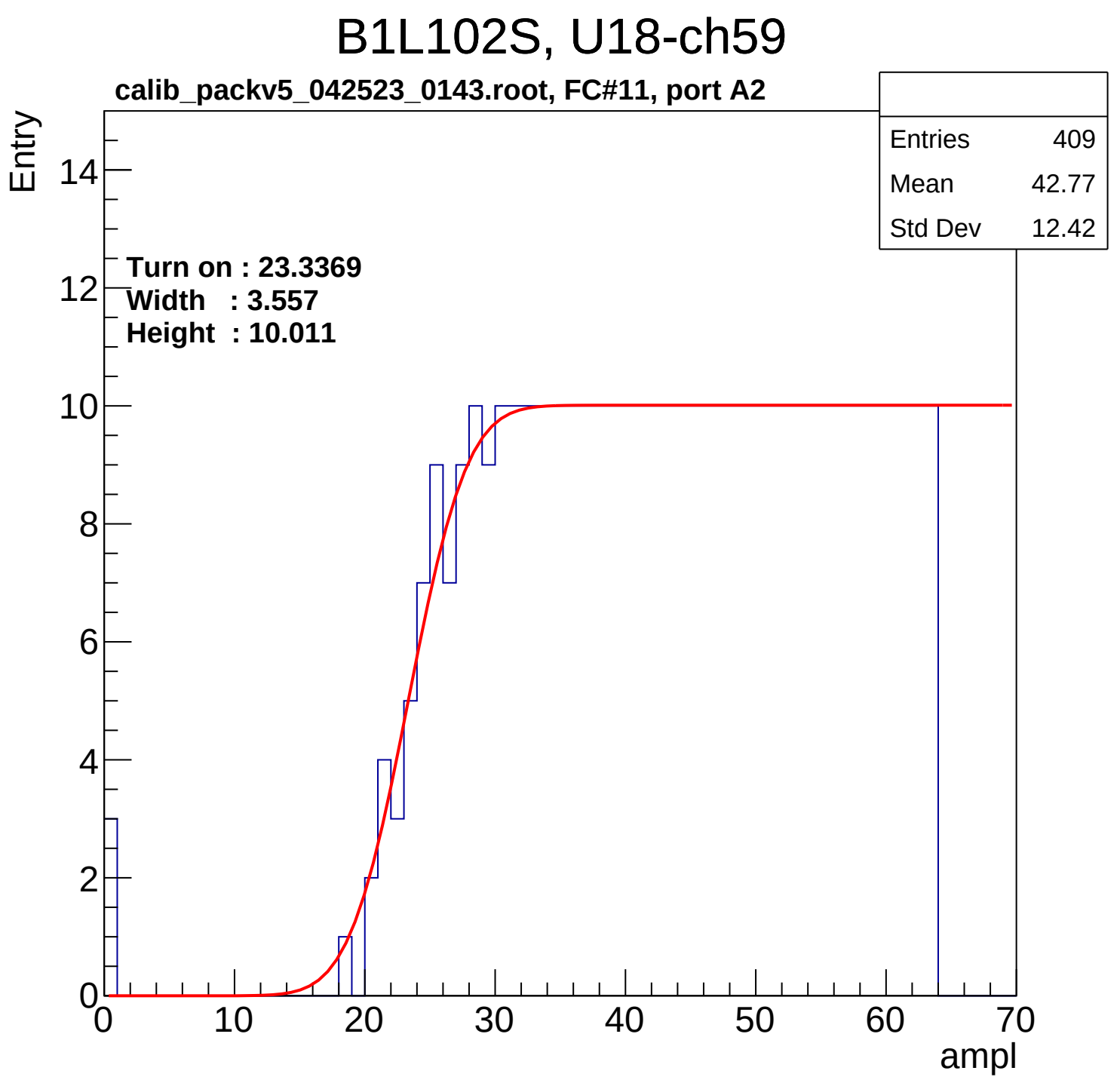
B1L102S, U18-ch59
calib_packv5_042523_0143.root, FC#11, port A2
Entries 409
Mean 42.77
Std Dev 12.42
Turn on : 23.3369
Width : 3.557
Height : 10.011
Entry
ampl
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2
4
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8
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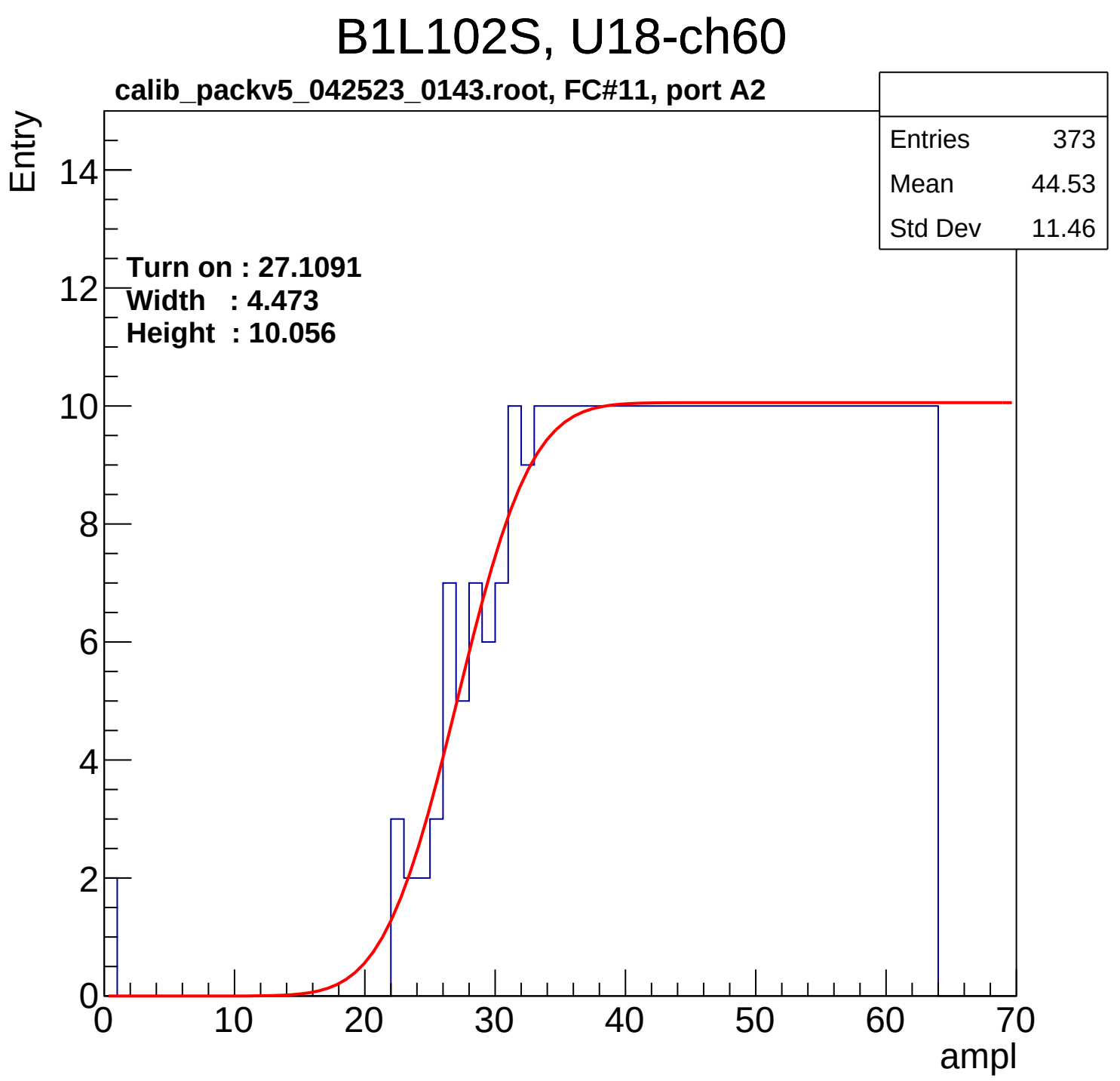
B1L102S, U18-ch60
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.53
Std Dev 11.46
Turn on : 27.1091
Width : 4.473
Height : 10.056
Entry
ampl
0
2
4
6
8
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0
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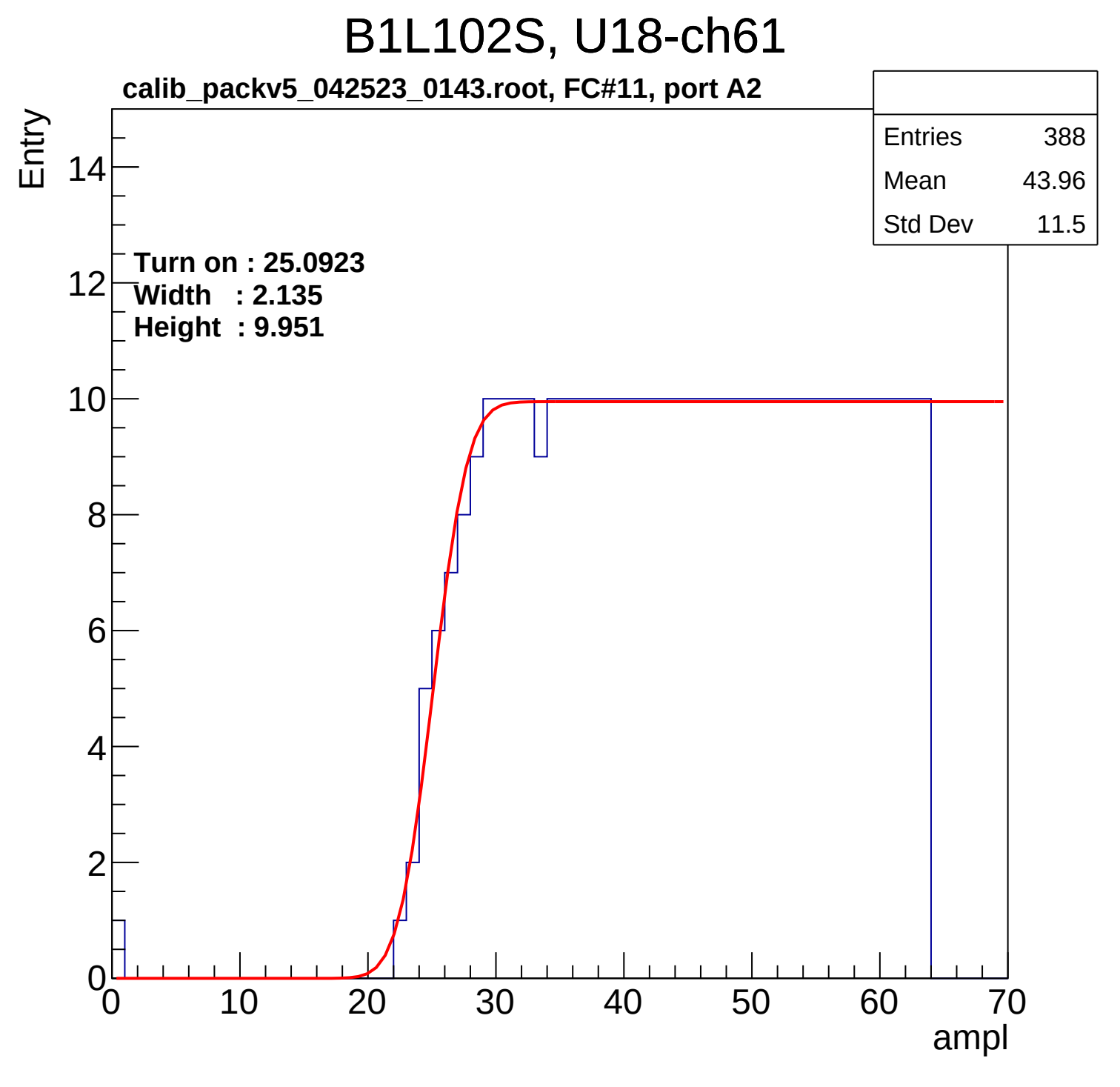
B1L102S, U18-ch61
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.96
Std Dev 11.5
Turn on : 25.0923
Width : 2.135
Height : 9.951
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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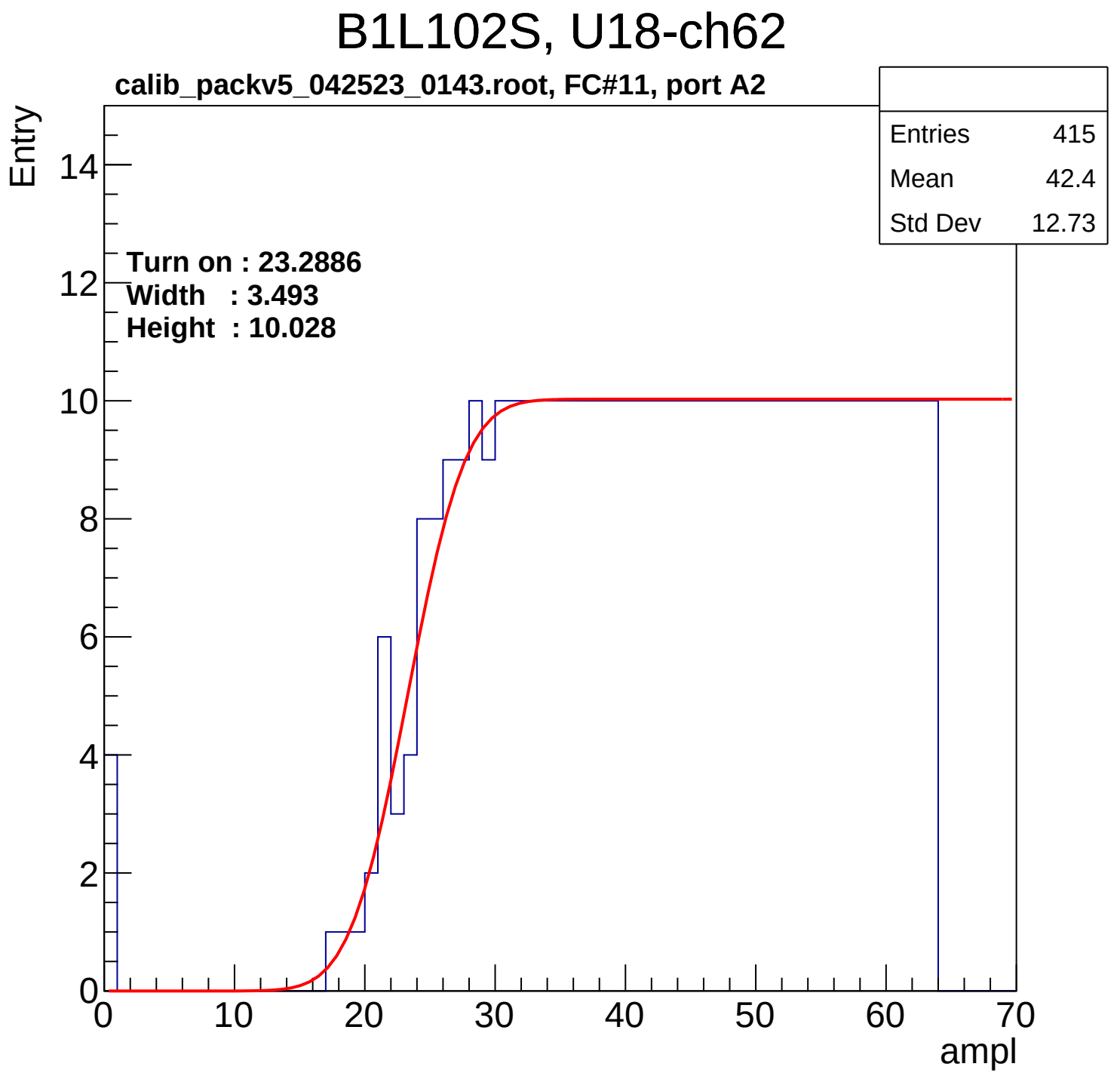
B1L102S, U18-ch62
calib_packv5_042523_0143.root, FC#11, port A2
Entries 415
Mean 42.4
Std Dev 12.73
Turn on : 23.2886
Width : 3.493
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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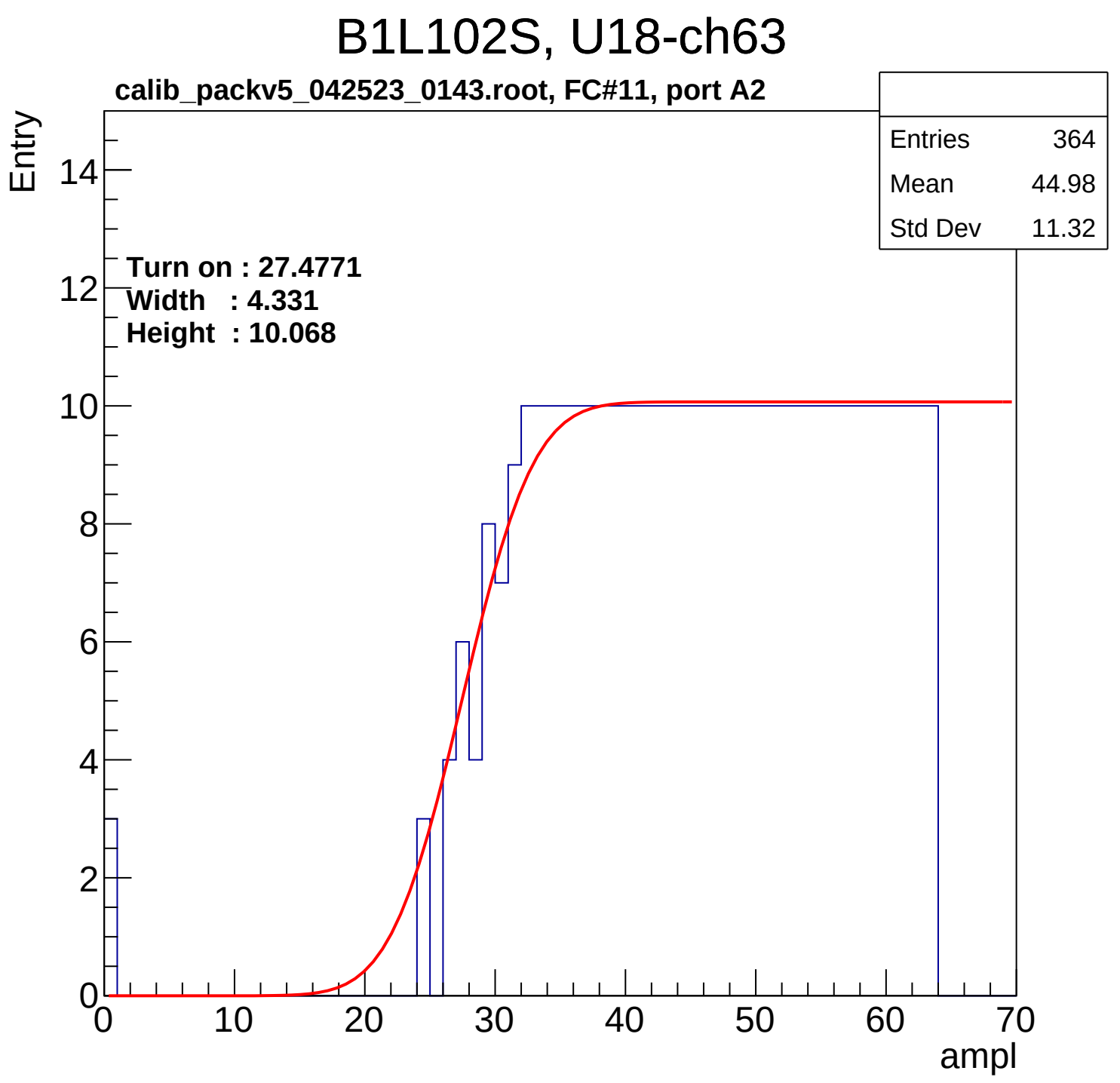
B1L102S, U18-ch63
calib_packv5_042523_0143.root, FC#11, port A2
Entries 364
Mean 44.98
Std Dev 11.32
Turn on : 27.4771
Width : 4.331
Height : 10.068
Entry
ampl
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2
4
6
8
10
12
14
0
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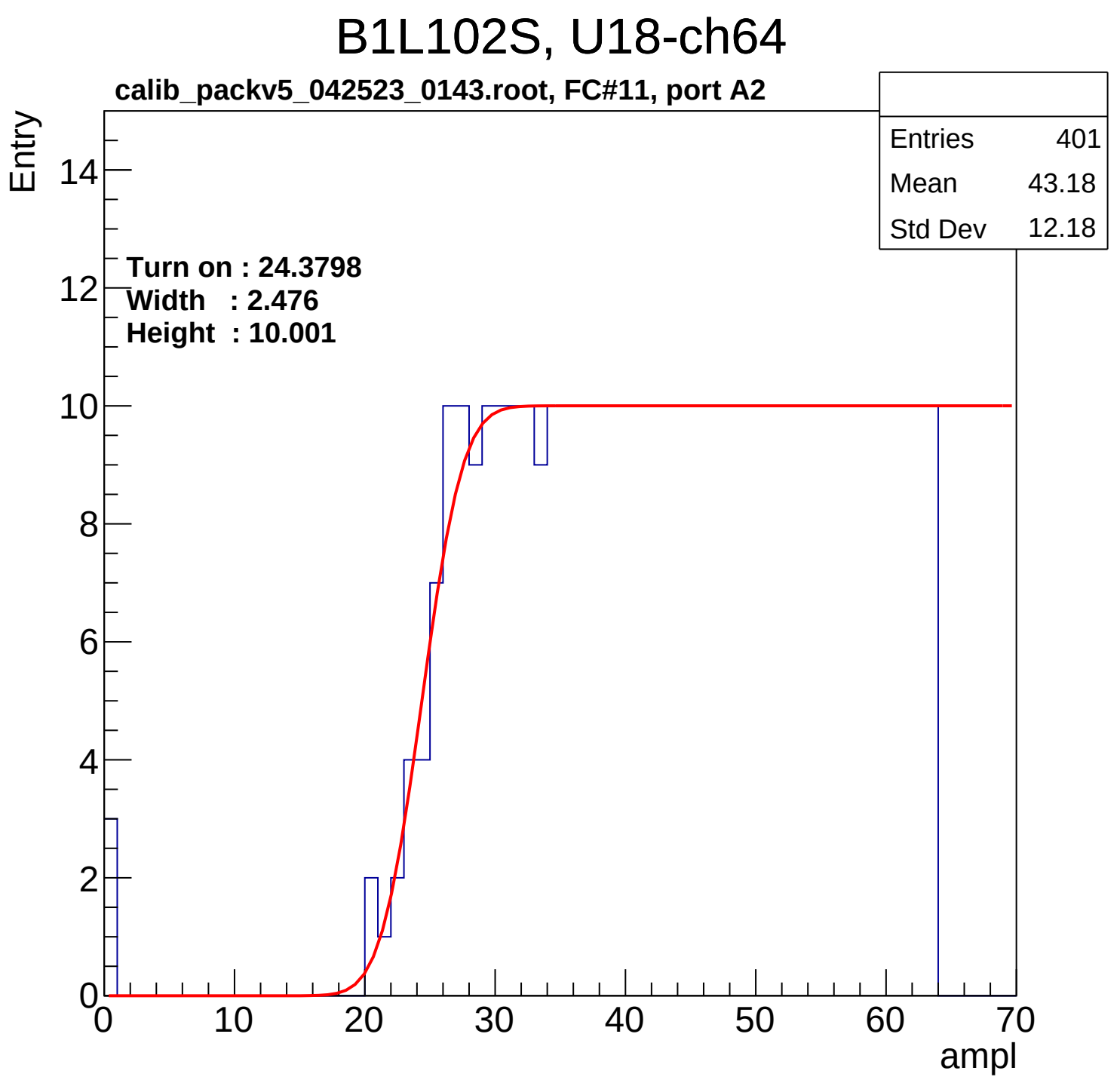
B1L102S, U18-ch64
calib_packv5_042523_0143.root, FC#11, port A2
Entries 401
Mean 43.18
Std Dev 12.18
Turn on : 24.3798
Width : 2.476
Height : 10.001
Entry
ampl
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4
6
8
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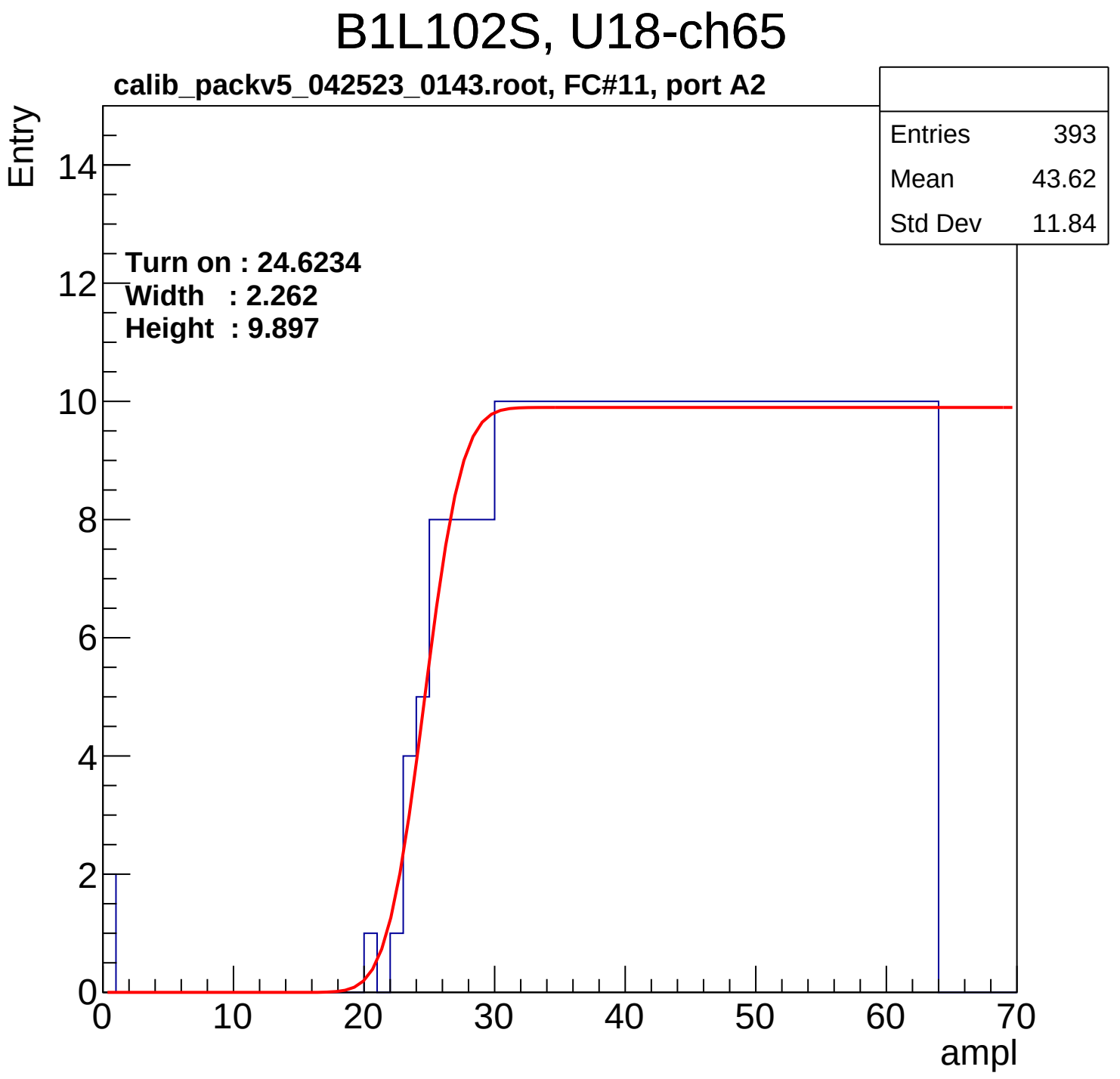
B1L102S, U18-ch65
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.62
Std Dev 11.84
Turn on : 24.6234
Width : 2.262
Height : 9.897
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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60
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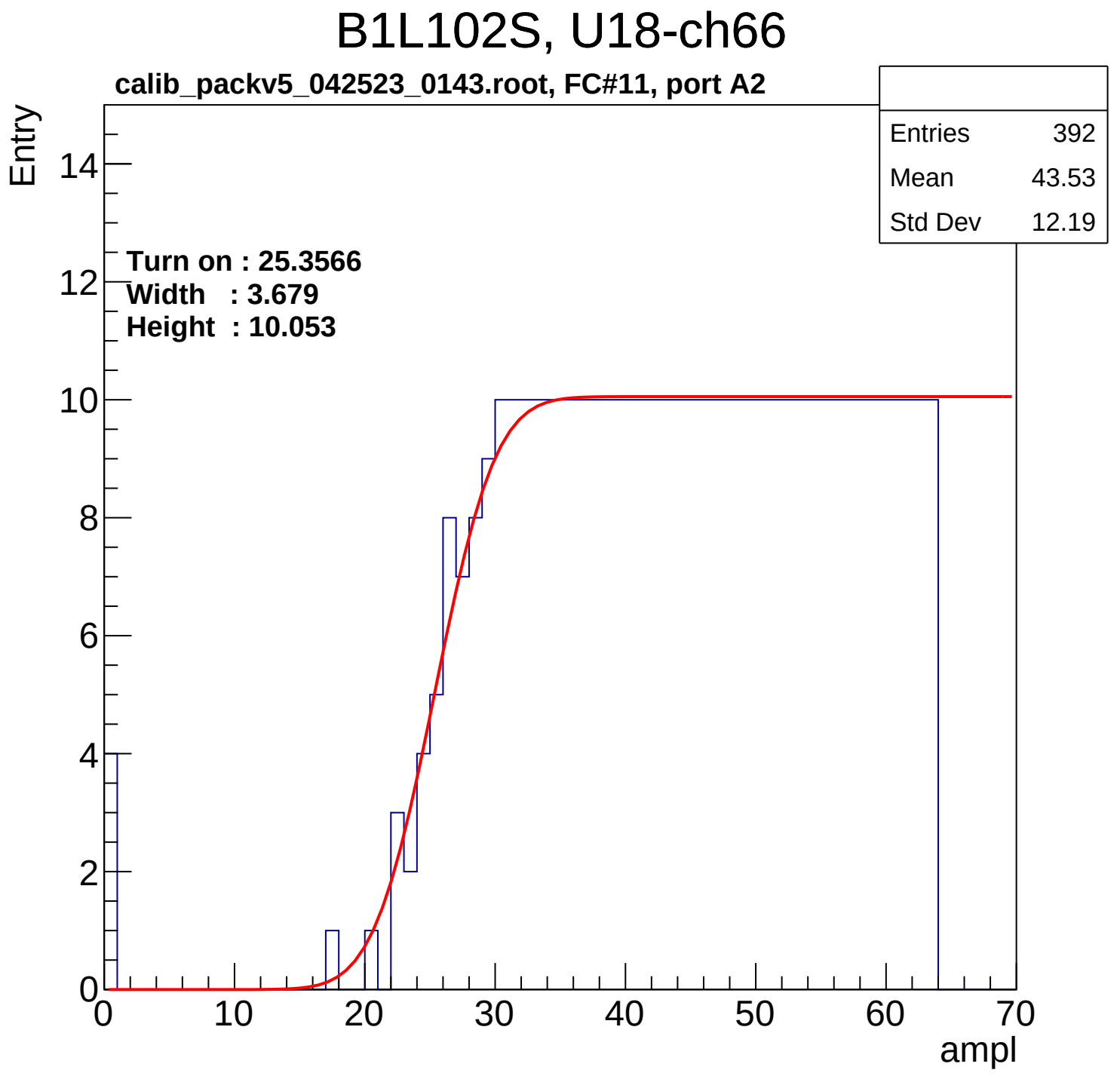
B1L102S, U18-ch66
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.53
Std Dev 12.19
Turn on : 25.3566
Width : 3.679
Height : 10.053
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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60
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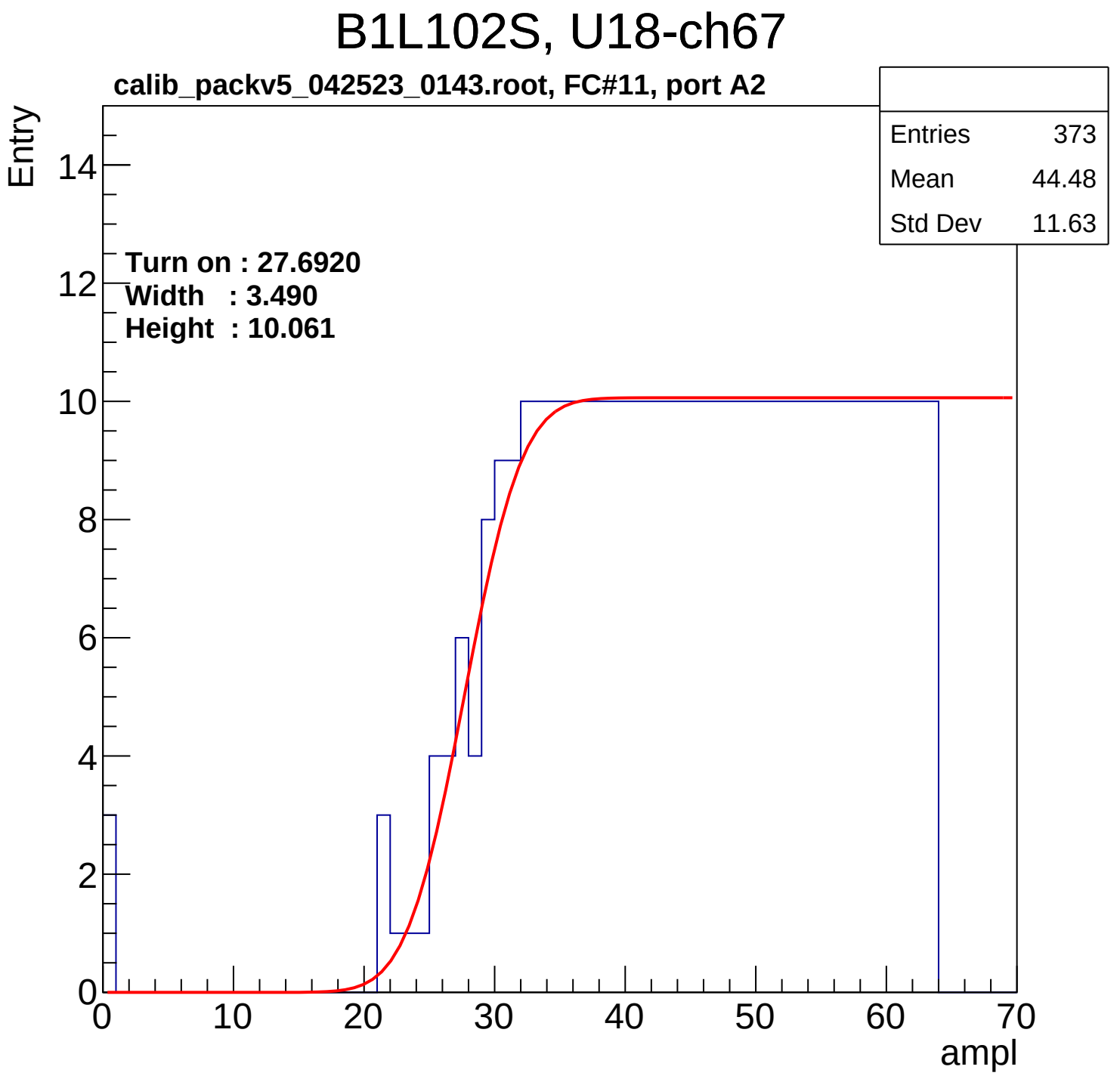
B1L102S, U18-ch67
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.48
Std Dev 11.63
Turn on : 27.6920
Width : 3.490
Height : 10.061
Entry
ampl
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4
6
8
10
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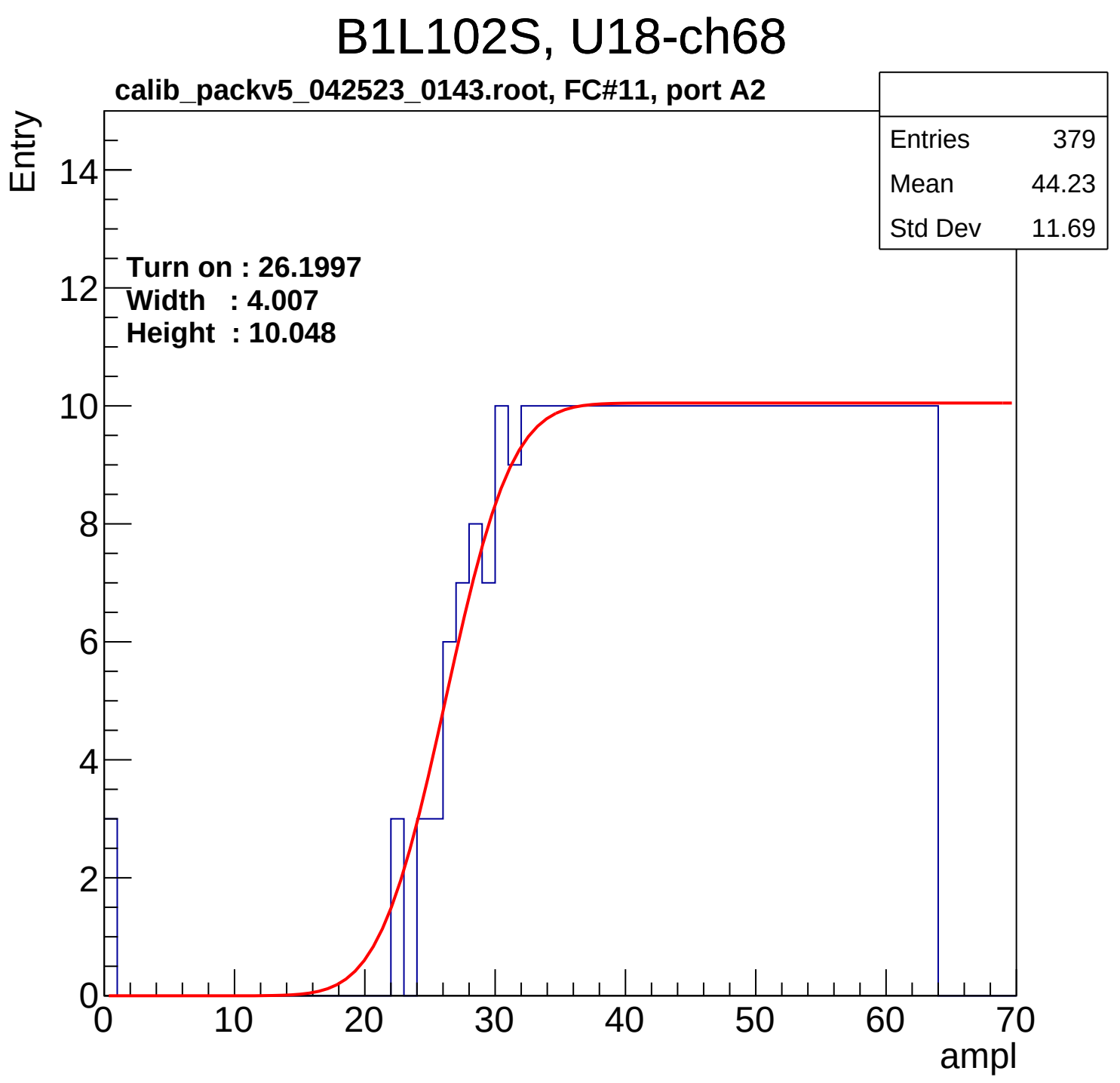
B1L102S, U18-ch68
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.23
Std Dev 11.69
Turn on : 26.1997
Width : 4.007
Height : 10.048
Entry
ampl
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2
4
6
8
10
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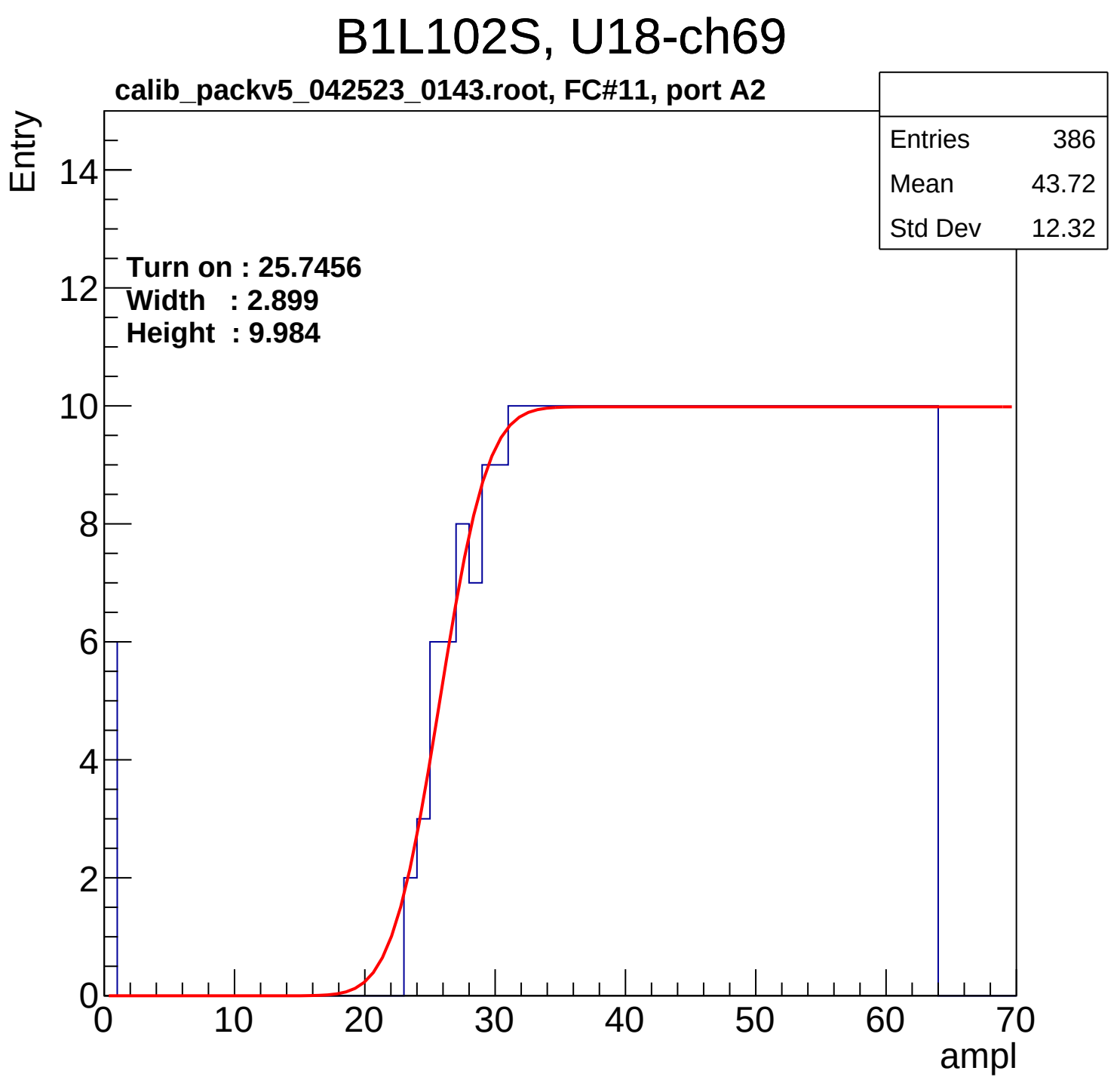
B1L102S, U18-ch69
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.72
Std Dev 12.32
Turn on : 25.7456
Width : 2.899
Height : 9.984
Entry
ampl
0
2
4
6
8
10
12
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0
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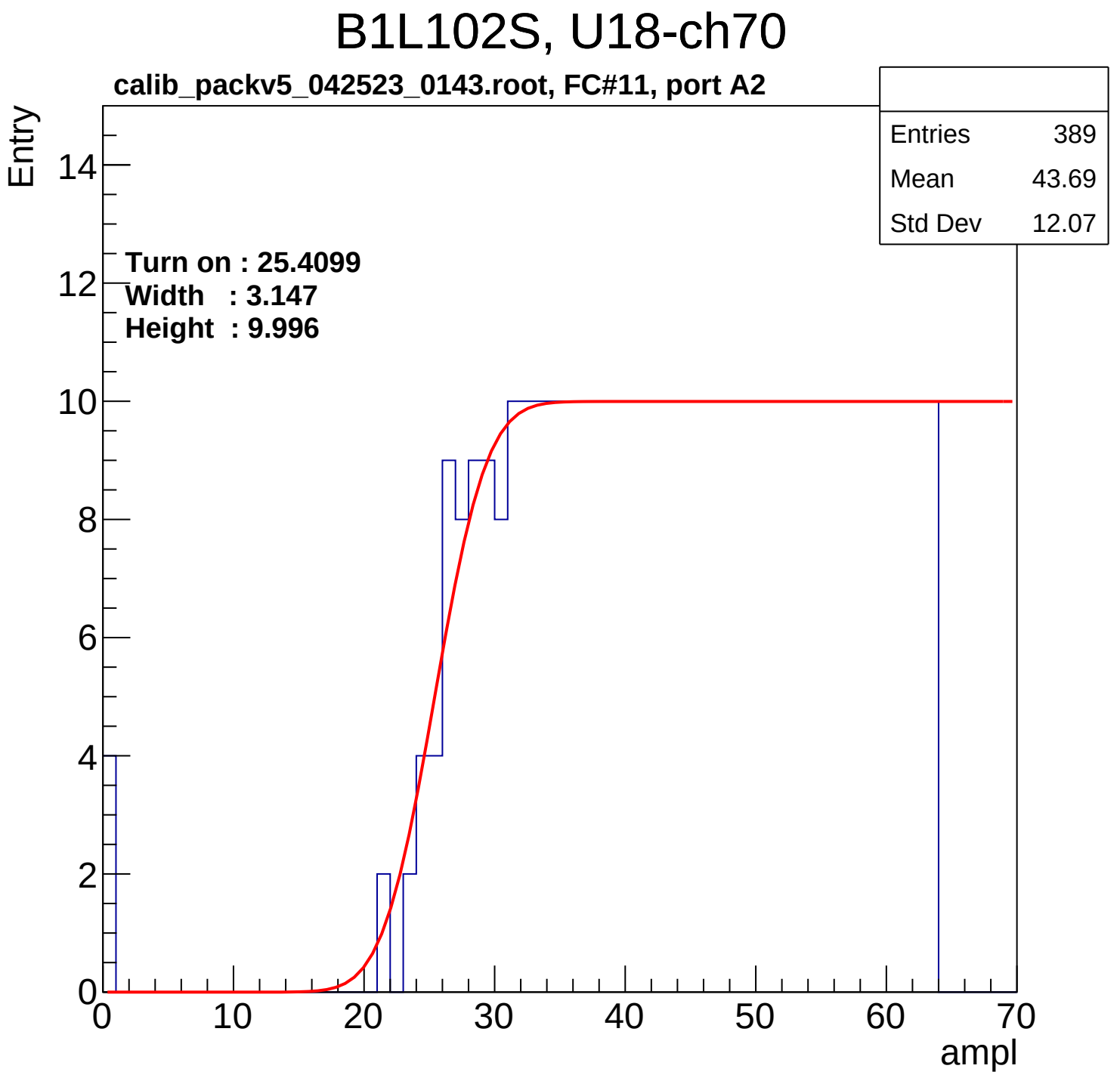
B1L102S, U18-ch70
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.69
Std Dev 12.07
Turn on : 25.4099
Width : 3.147
Height : 9.996
Entry
ampl
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2
4
6
8
10
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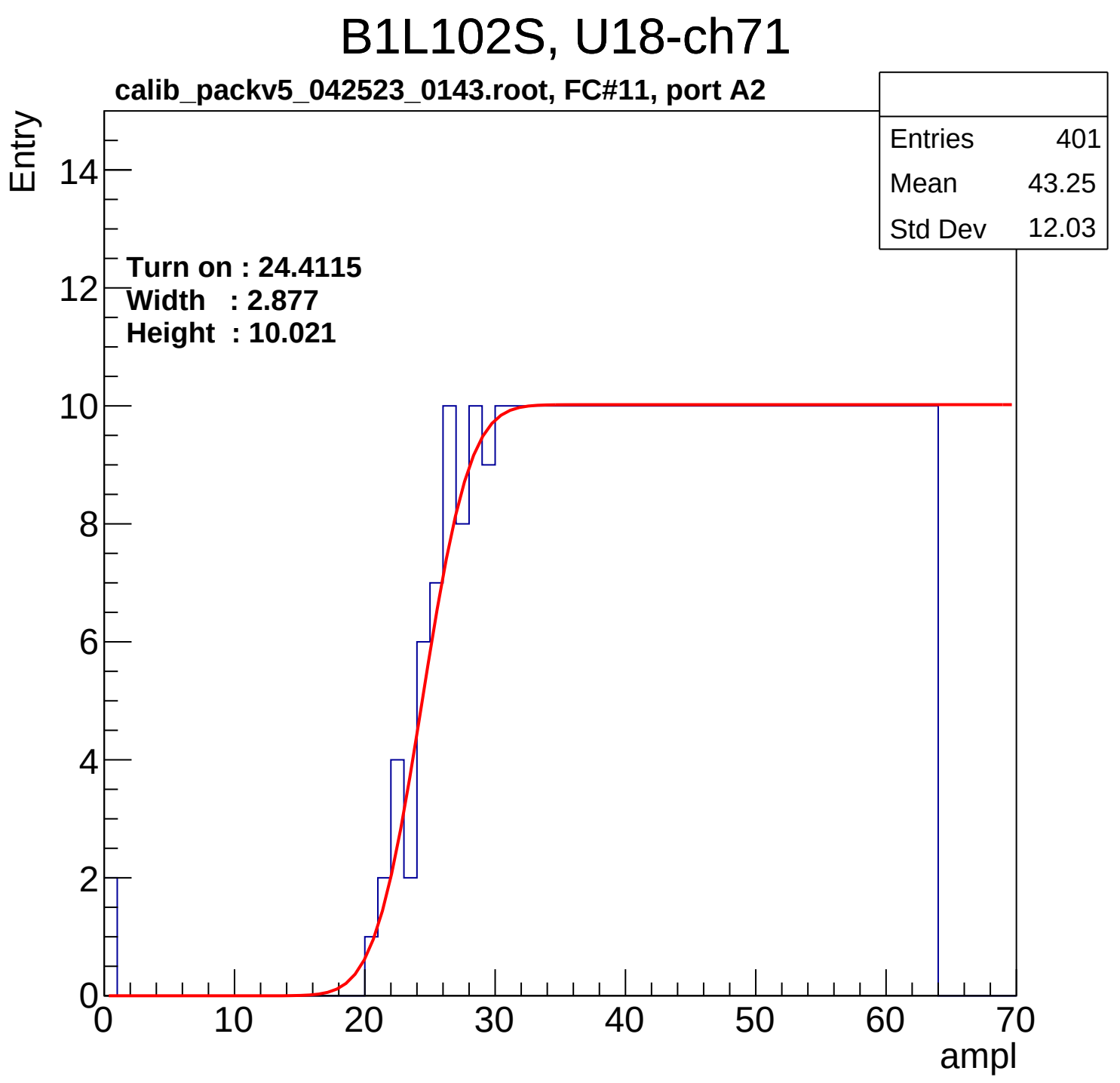
B1L102S, U18-ch71
calib_packv5_042523_0143.root, FC#11, port A2
Entries 401
Mean 43.25
Std Dev 12.03
Turn on : 24.4115
Width : 2.877
Height : 10.021
Entry
ampl
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2
4
6
8
10
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0
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60
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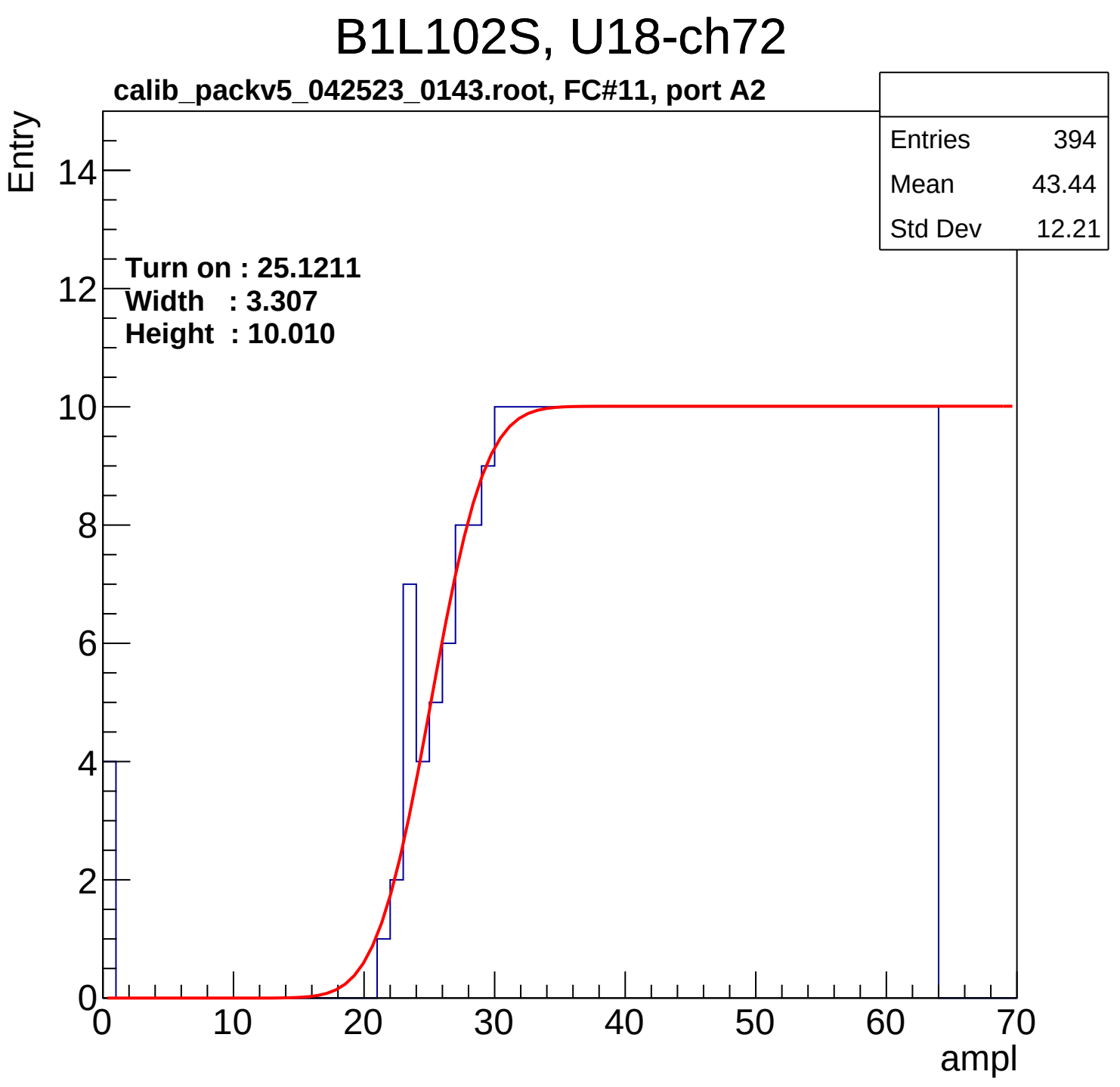
B1L102S, U18-ch72
calib_packv5_042523_0143.root, FC#11, port A2
Entries 394
Mean 43.44
Std Dev 12.21
Turn on : 25.1211
Width : 3.307
Height : 10.010
Entry
ampl
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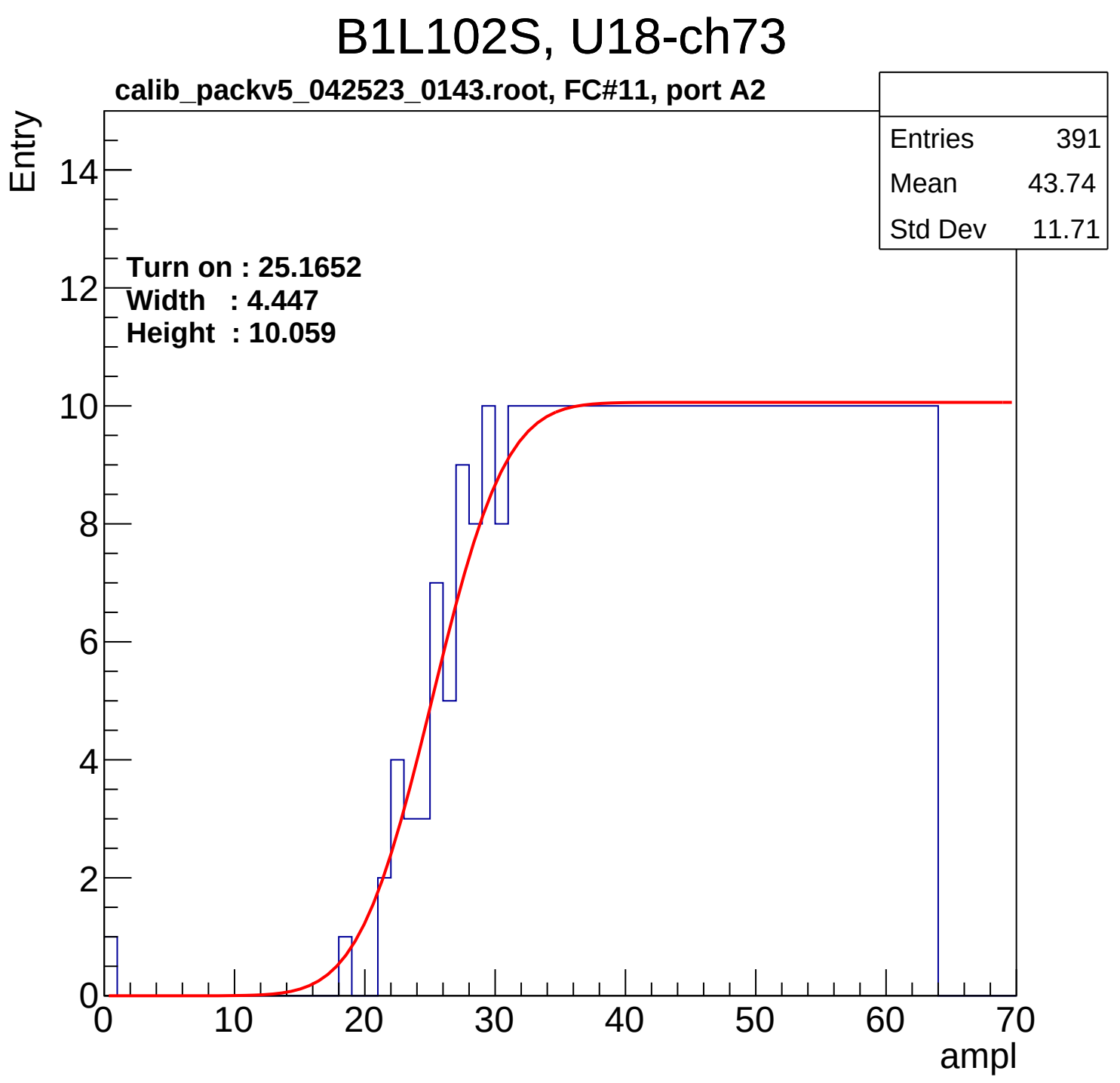
B1L102S, U18-ch73
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.74
Std Dev 11.71
Turn on : 25.1652
Width : 4.447
Height : 10.059
Entry
ampl
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6
8
10
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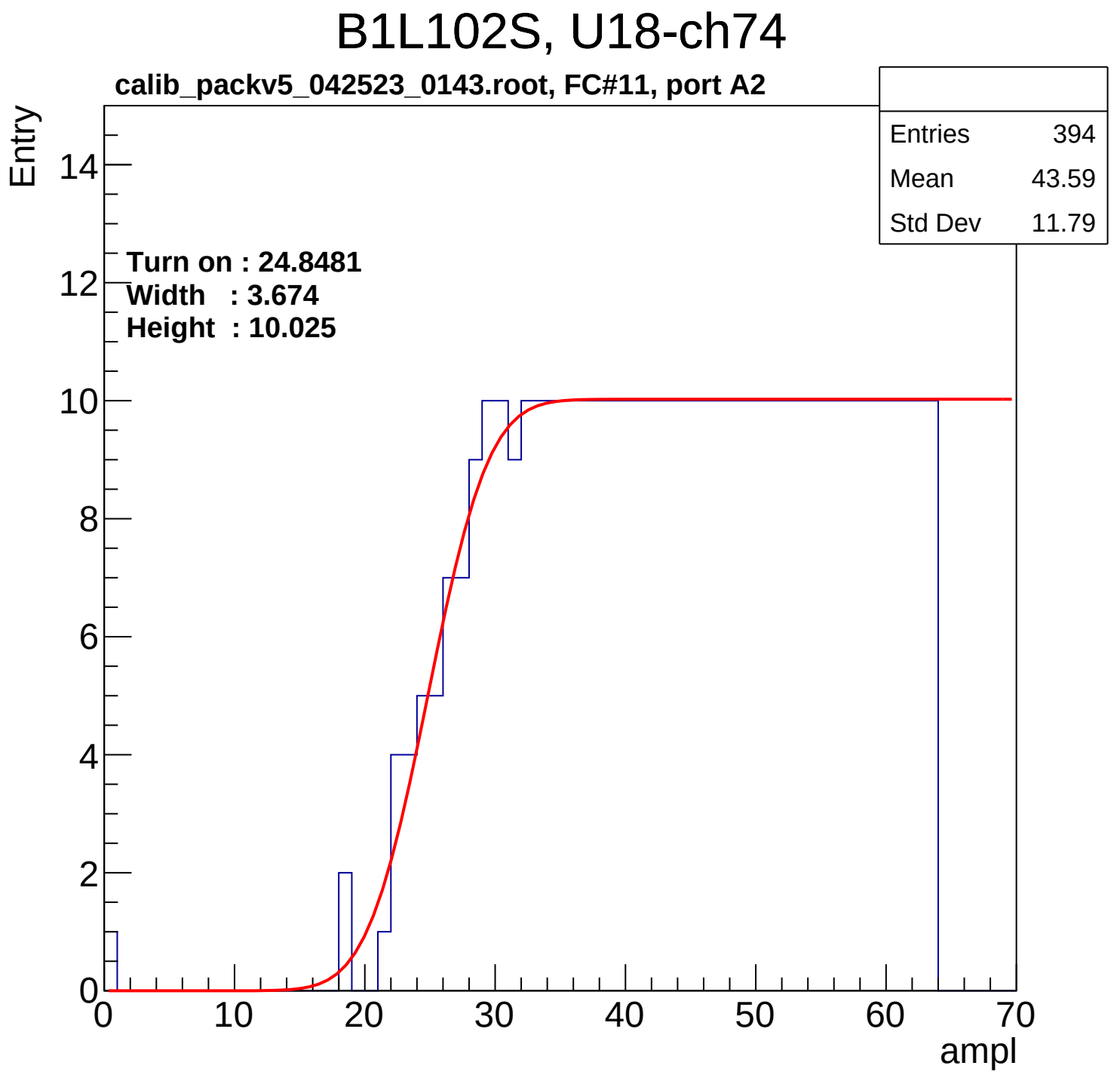
B1L102S, U18-ch74
calib_packv5_042523_0143.root, FC#11, port A2
Entries 394
Mean 43.59
Std Dev 11.79
Turn on : 24.8481
Width : 3.674
Height : 10.025
Entry
ampl
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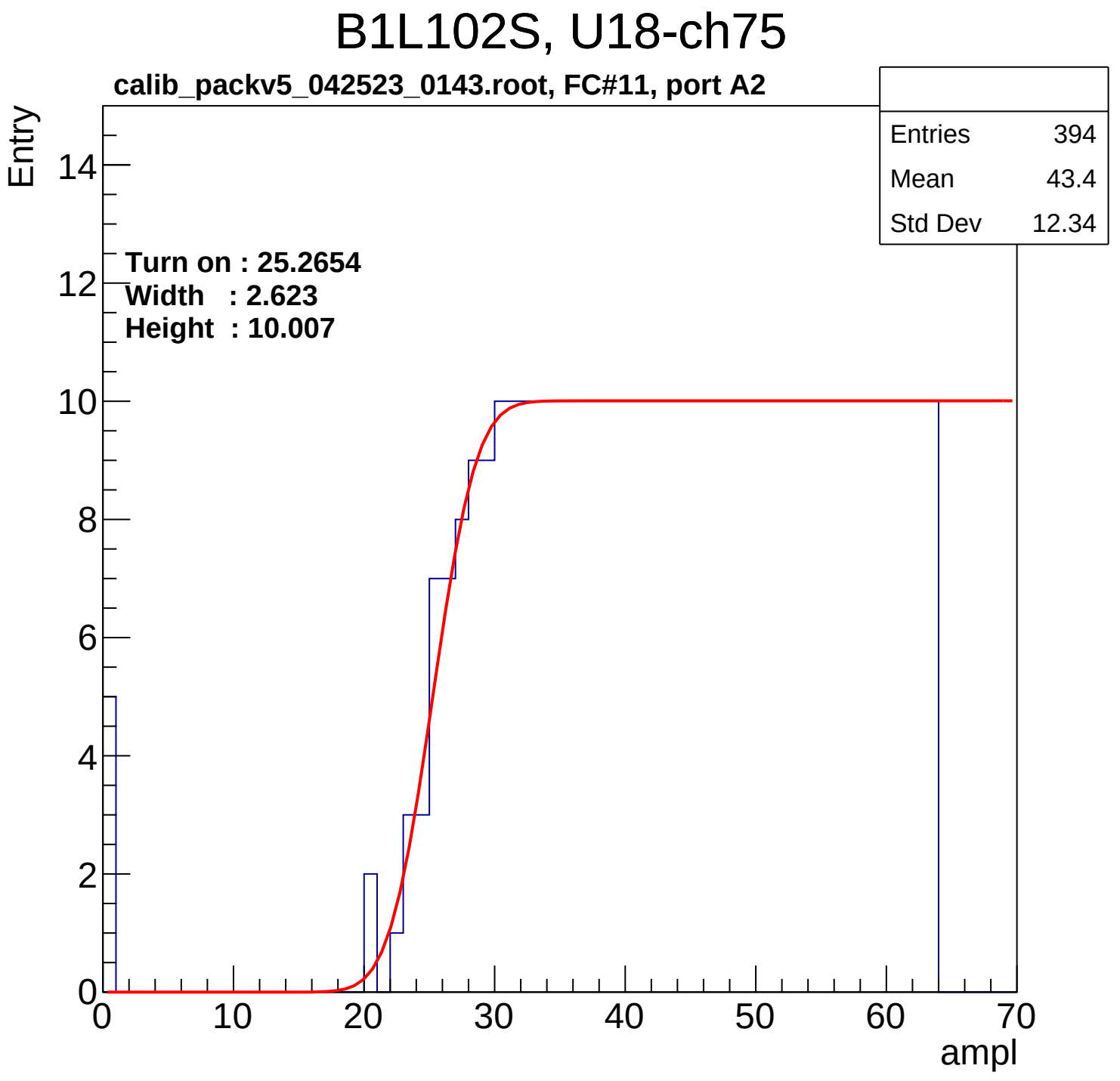
B1L102S, U18-ch75
calib_packv5_042523_0143.root, FC#11, port A2
Entries 394
Mean 43.4
Std Dev 12.34
Turn on : 25.2654
Width : 2.623
Height : 10.007
Entry
ampl
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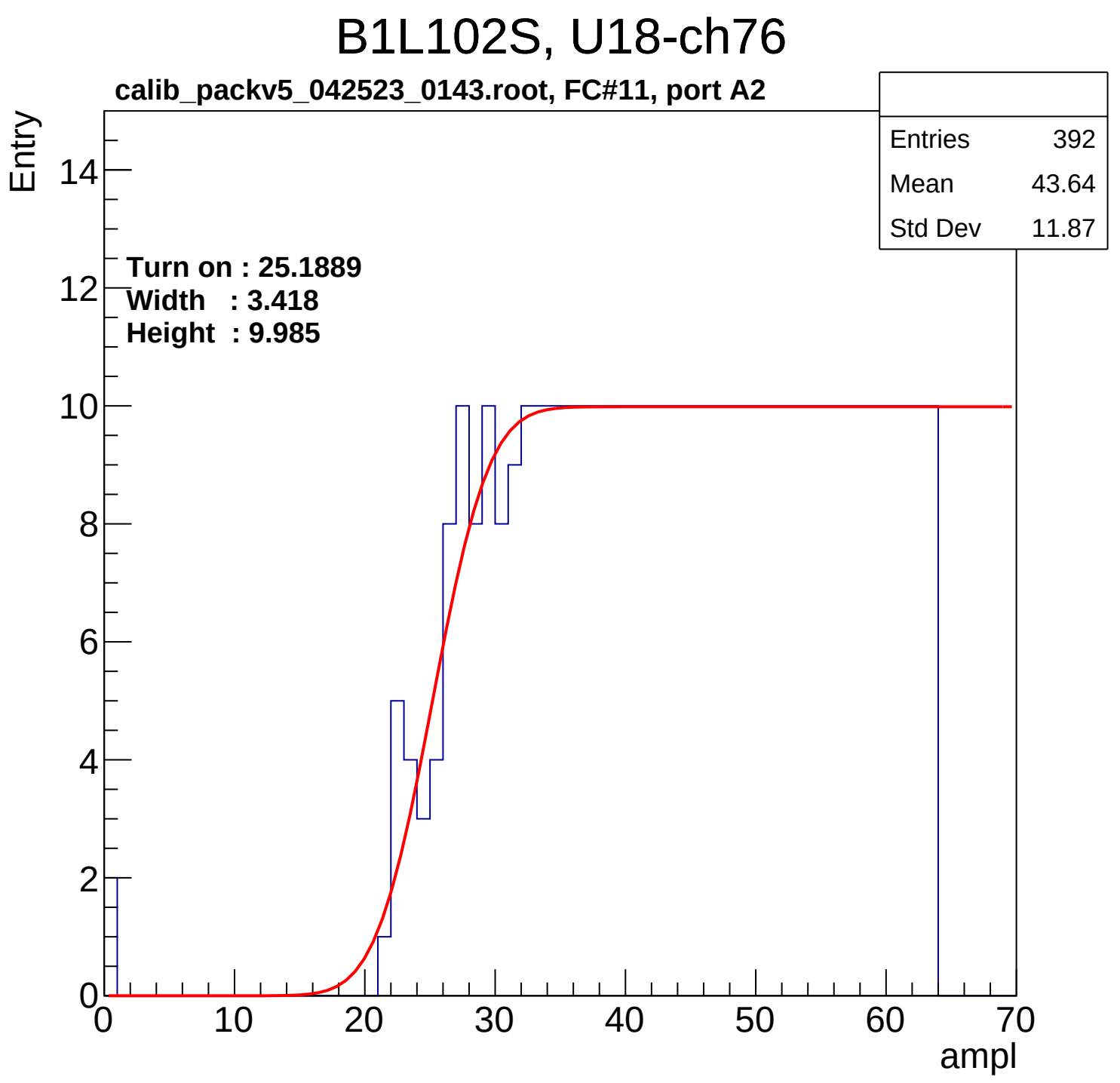
B1L102S, U18-ch76
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.64
Std Dev 11.87
Turn on : 25.1889
Width : 3.418
Height : 9.985
Entry
ampl
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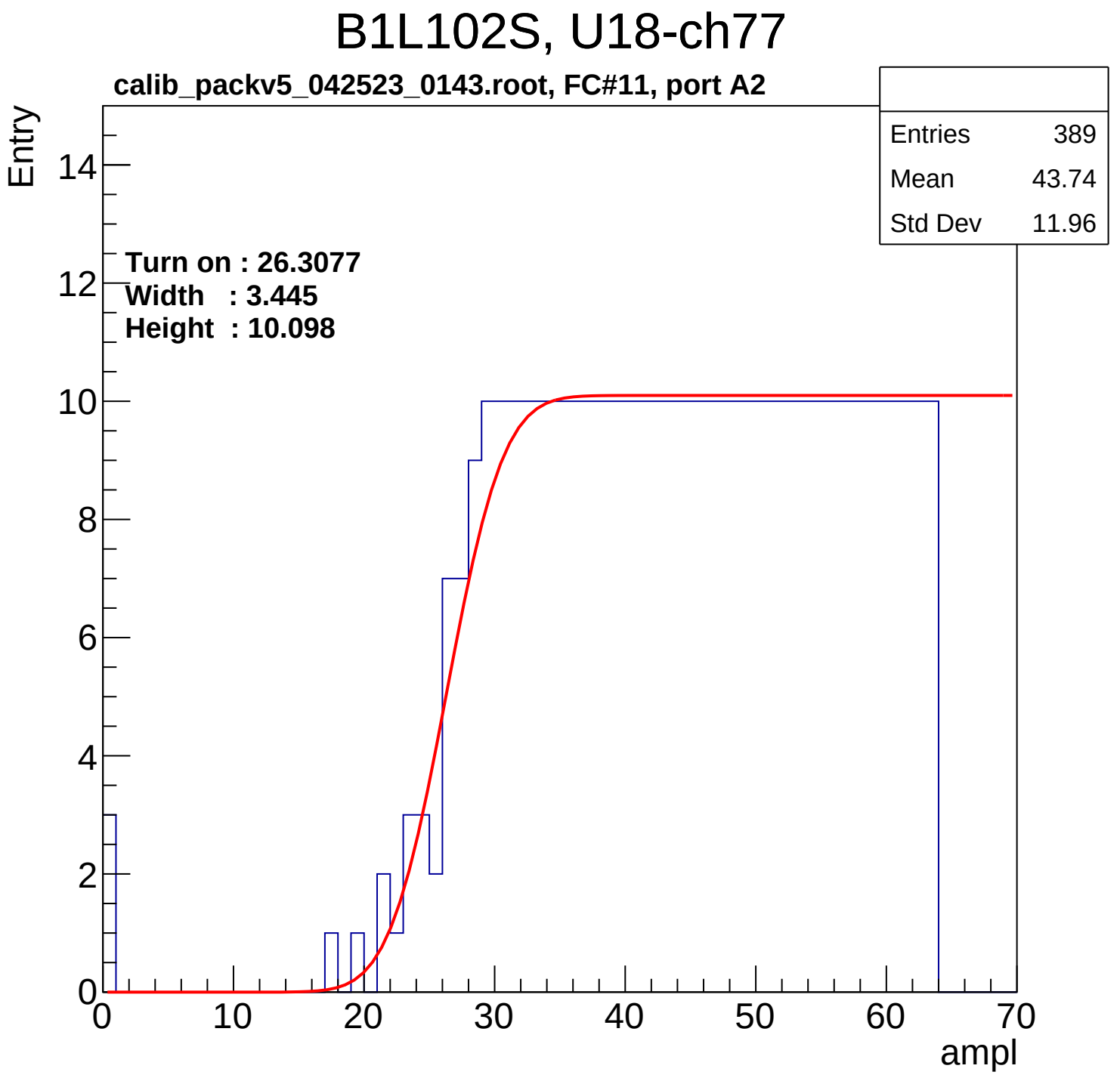
B1L102S, U18-ch77
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.74
Std Dev 11.96
Turn on : 26.3077
Width : 3.445
Height : 10.098
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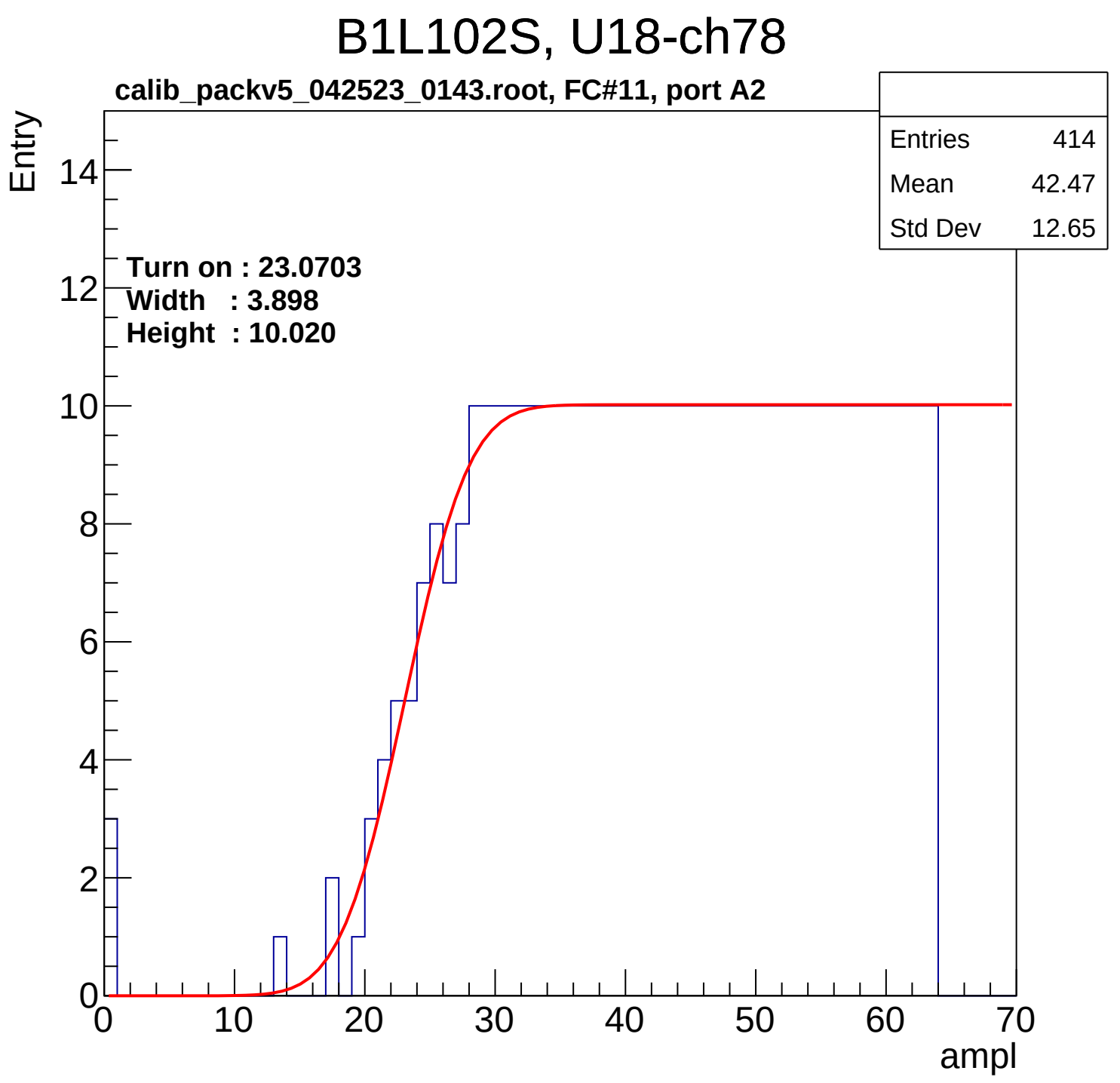
B1L102S, U18-ch78
calib_packv5_042523_0143.root, FC#11, port A2
Entries 414
Mean 42.47
Std Dev 12.65
Turn on : 23.0703
Width : 3.898
Height : 10.020
Entry
ampl
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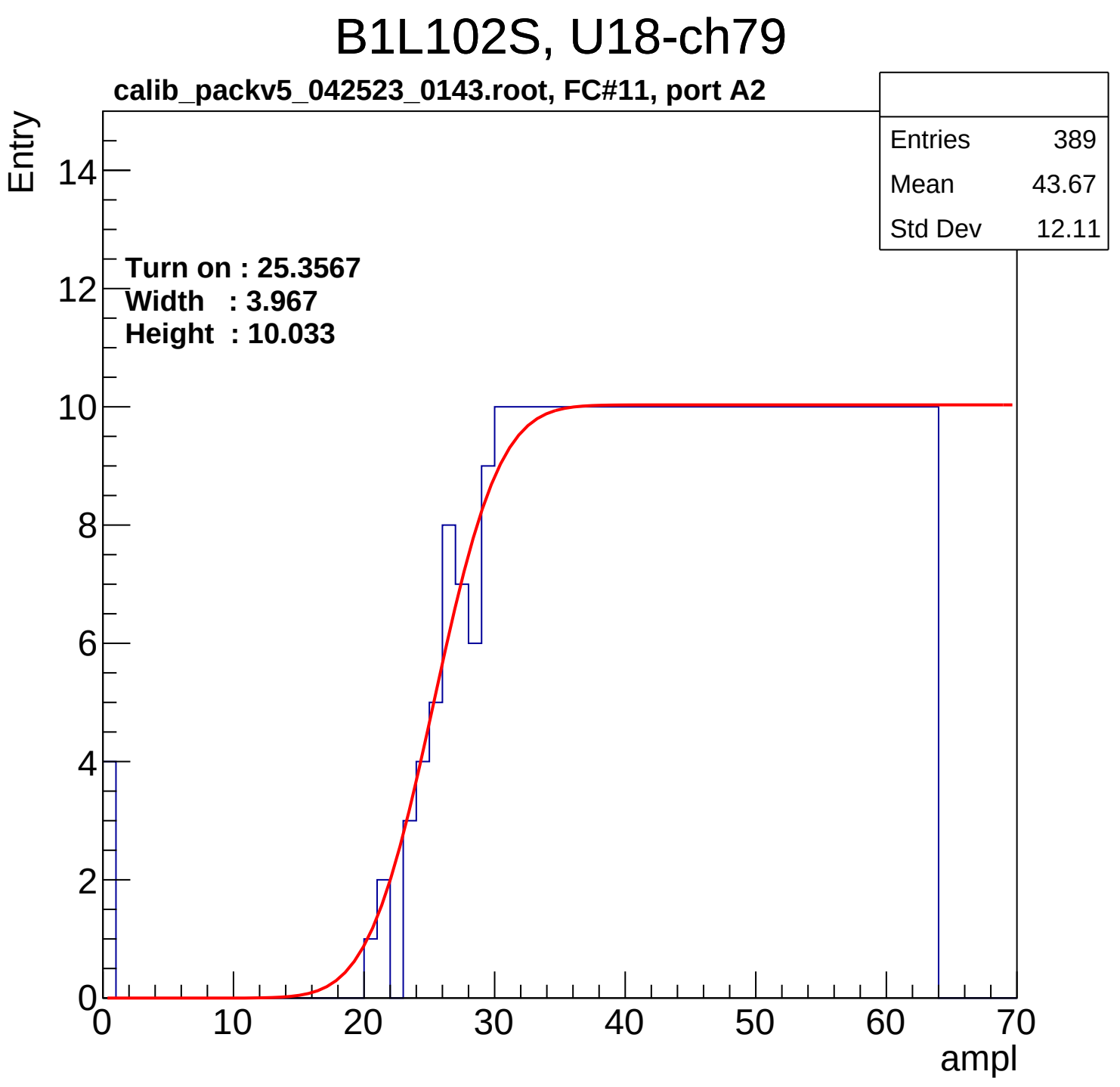
B1L102S, U18-ch79
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.67
Std Dev 12.11
Turn on : 25.3567
Width : 3.967
Height : 10.033
Entry
ampl
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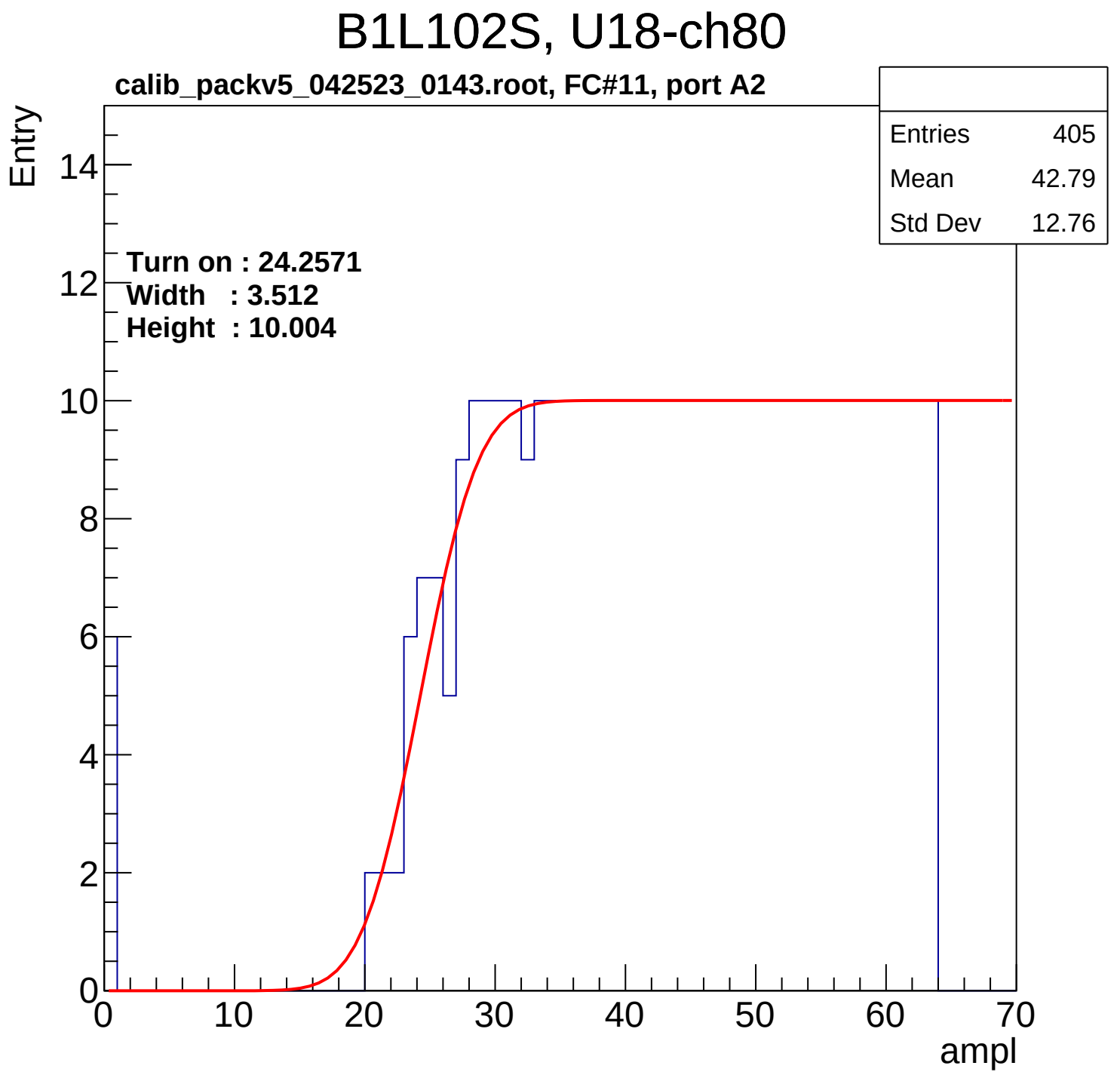
B1L102S, U18-ch80
calib_packv5_042523_0143.root, FC#11, port A2
Entries 405
Mean 42.79
Std Dev 12.76
Turn on : 24.2571
Width : 3.512
Height : 10.004
Entry
ampl
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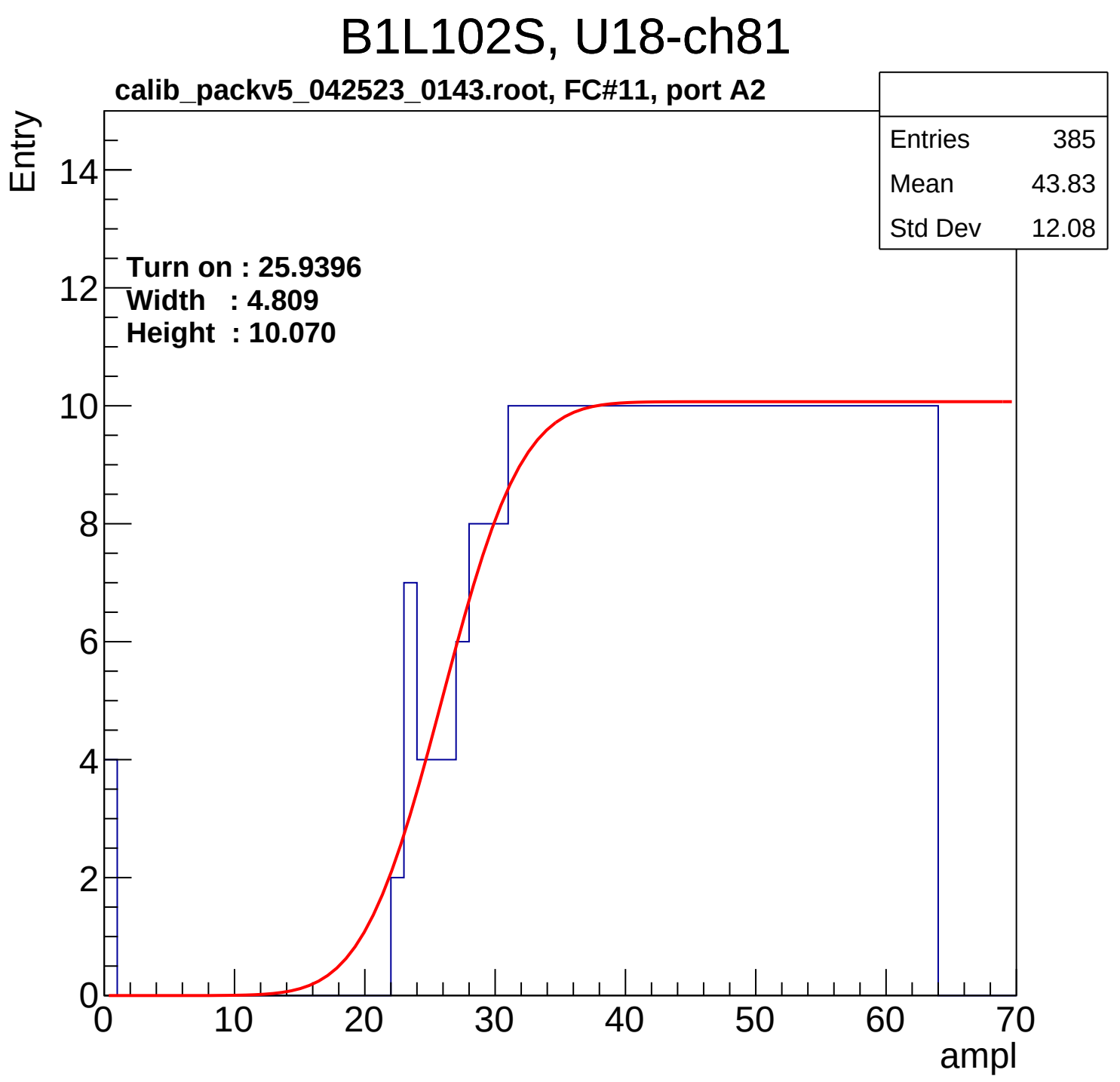
B1L102S, U18-ch81
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.83
Std Dev 12.08
Turn on : 25.9396
Width : 4.809
Height : 10.070
Entry
ampl
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2
4
6
8
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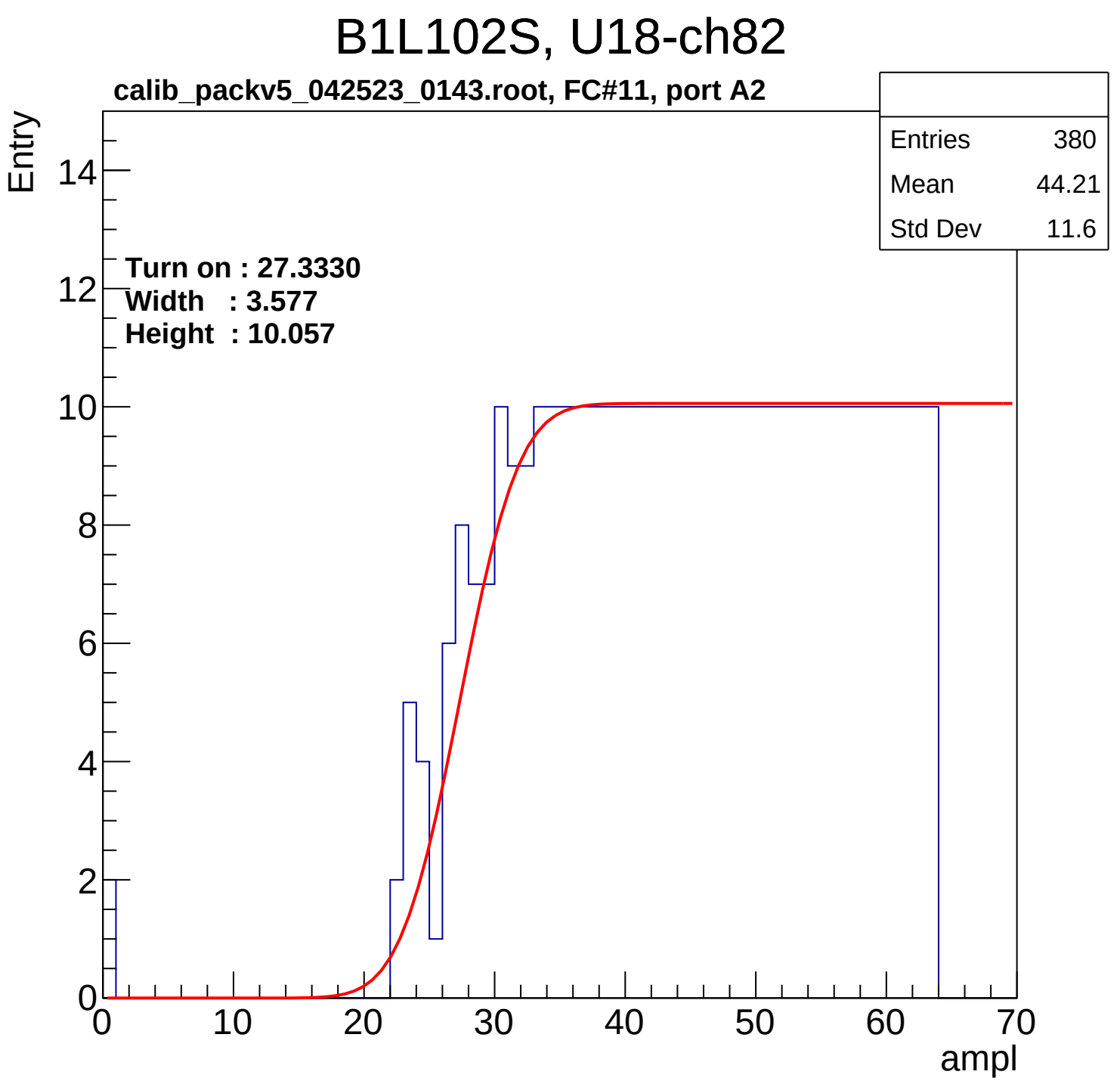
B1L102S, U18-ch82
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.21
Std Dev 11.6
Turn on : 27.3330
Width : 3.577
Height : 10.057
Entry
ampl
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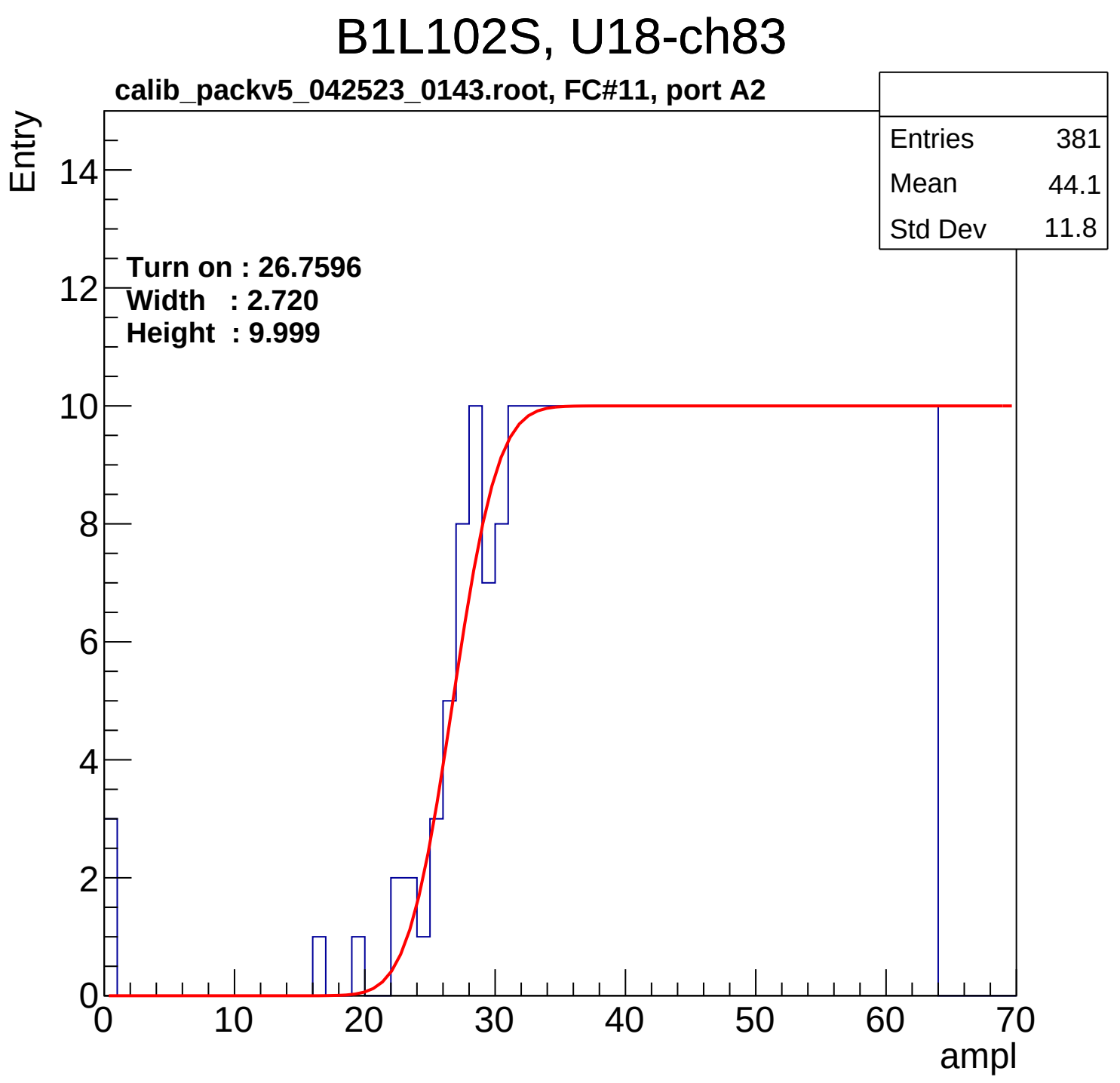
B1L102S, U18-ch83
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.1
Std Dev 11.8
Turn on : 26.7596
Width : 2.720
Height : 9.999
Entry
ampl
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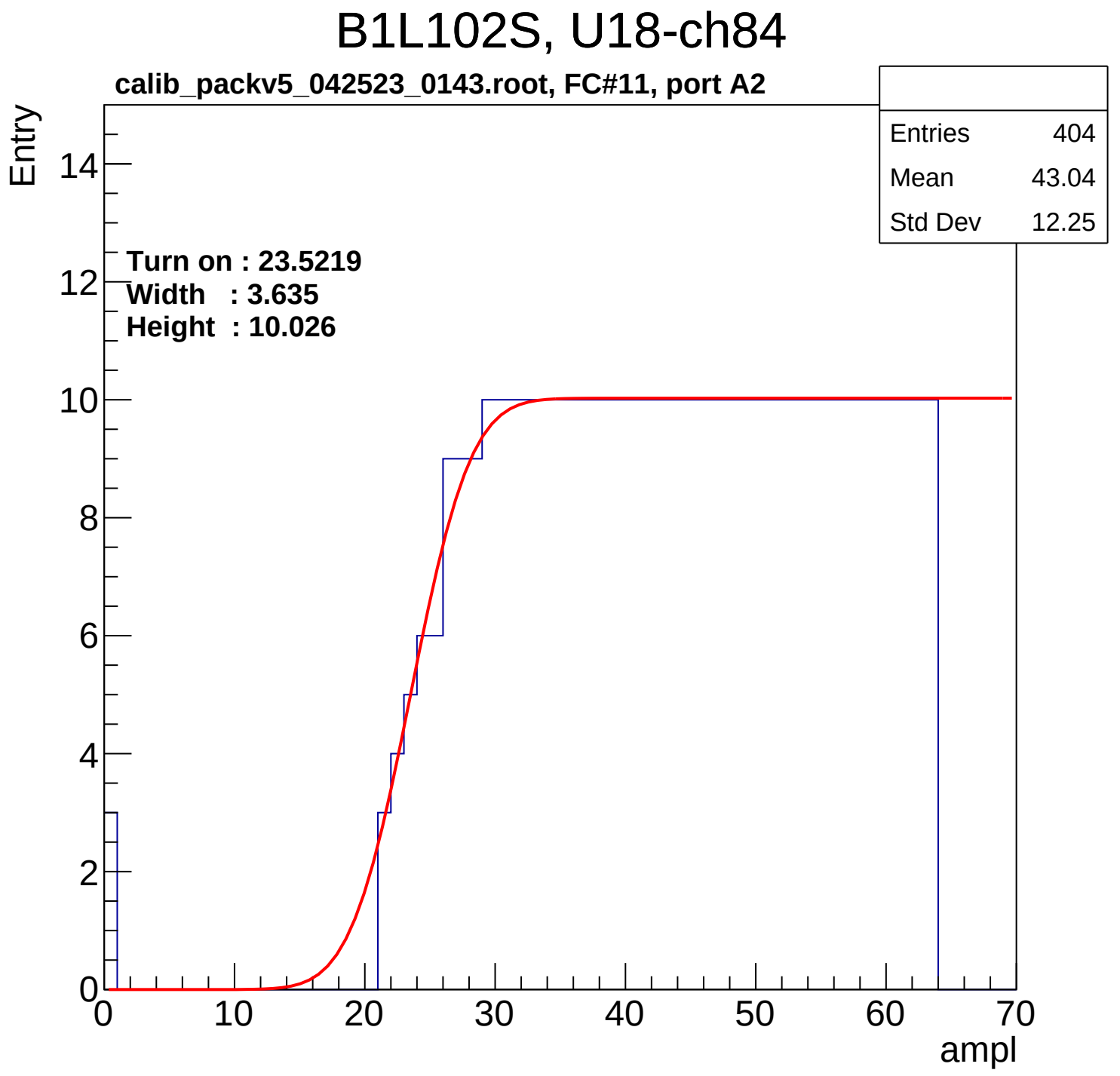
B1L102S, U18-ch84
calib_packv5_042523_0143.root, FC#11, port A2
Entries 404
Mean 43.04
Std Dev 12.25
Turn on : 23.5219
Width : 3.635
Height : 10.026
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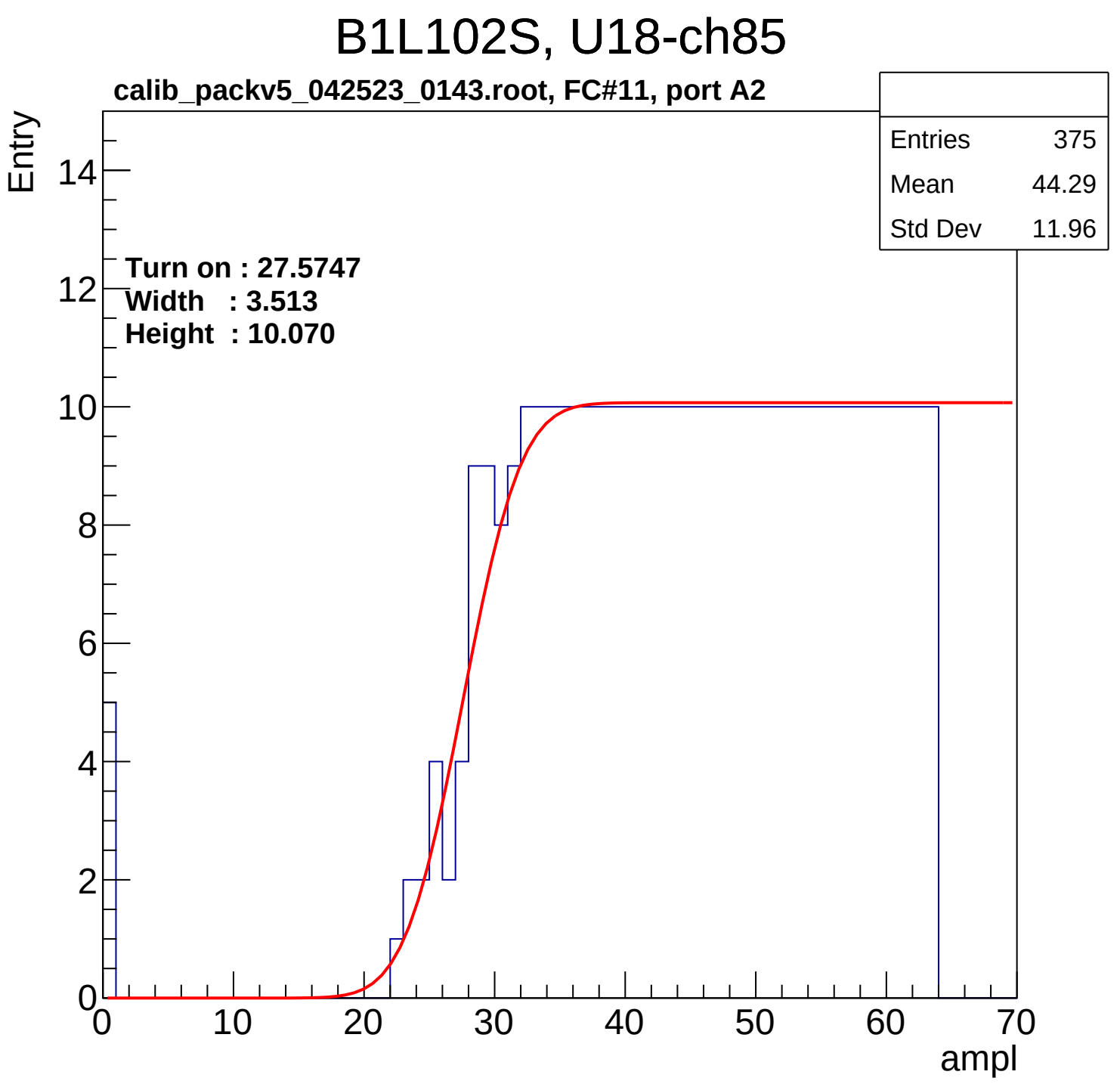
B1L102S, U18-ch85
calib_packv5_042523_0143.root, FC#11, port A2
Entries 375
Mean 44.29
Std Dev 11.96
Turn on : 27.5747
Width : 3.513
Height : 10.070
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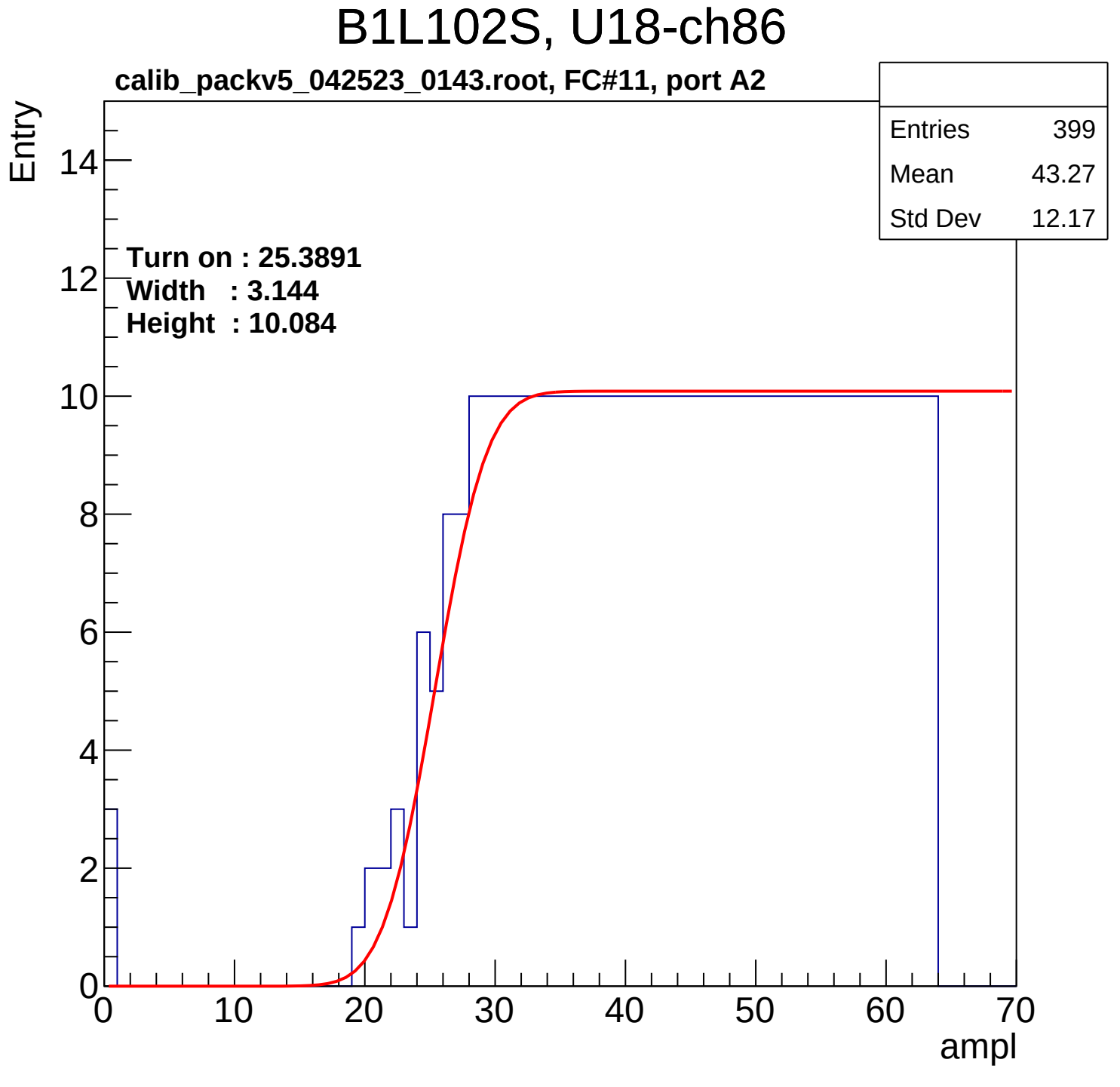
B1L102S, U18-ch86
calib_packv5_042523_0143.root, FC#11, port A2
Entries 399
Mean 43.27
Std Dev 12.17
Turn on : 25.3891
Width : 3.144
Height : 10.084
Entry
ampl
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6
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10
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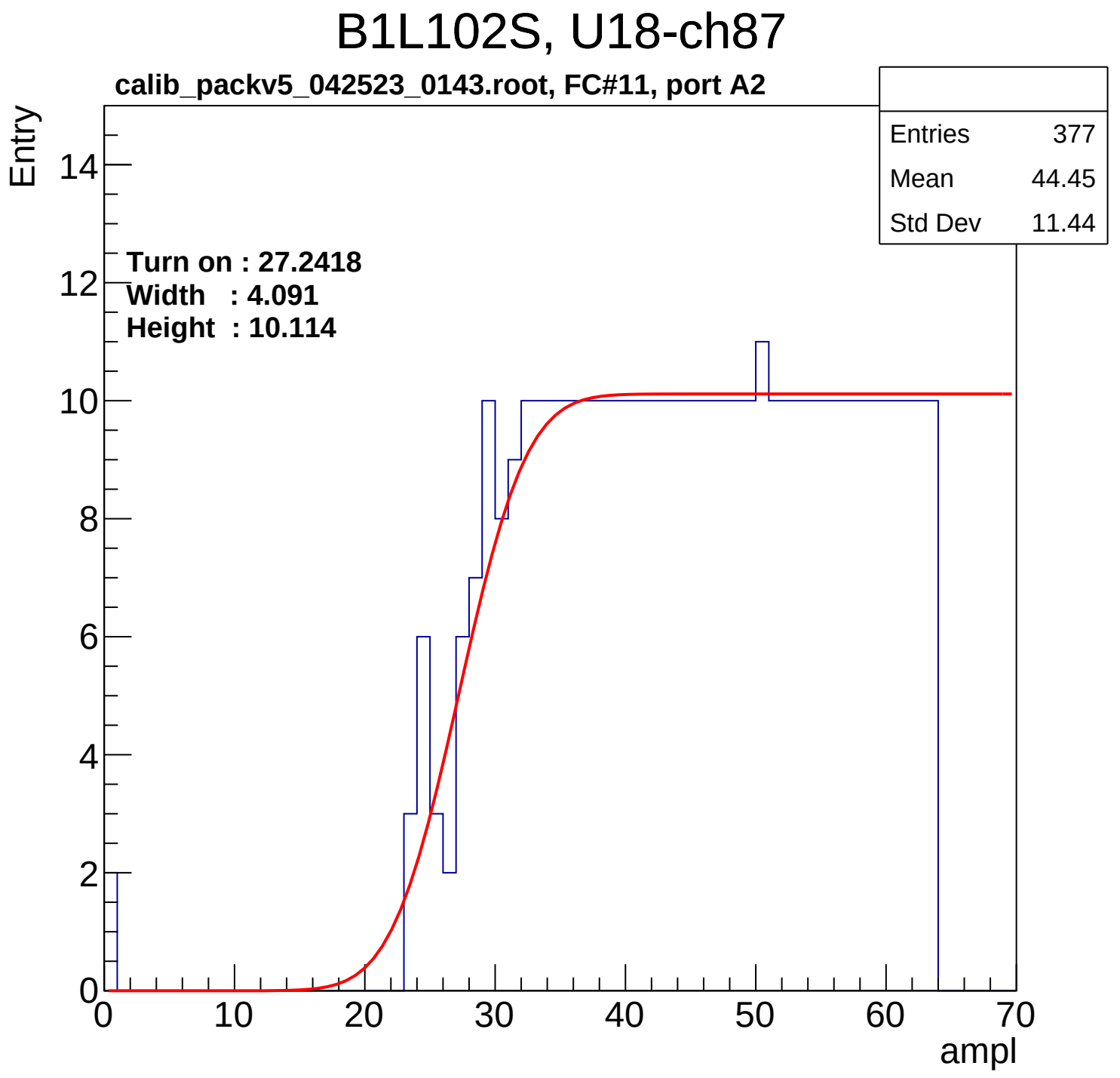
B1L102S, U18-ch87
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.45
Std Dev 11.44
Turn on : 27.2418
Width : 4.091
Height : 10.114
Entry
ampl
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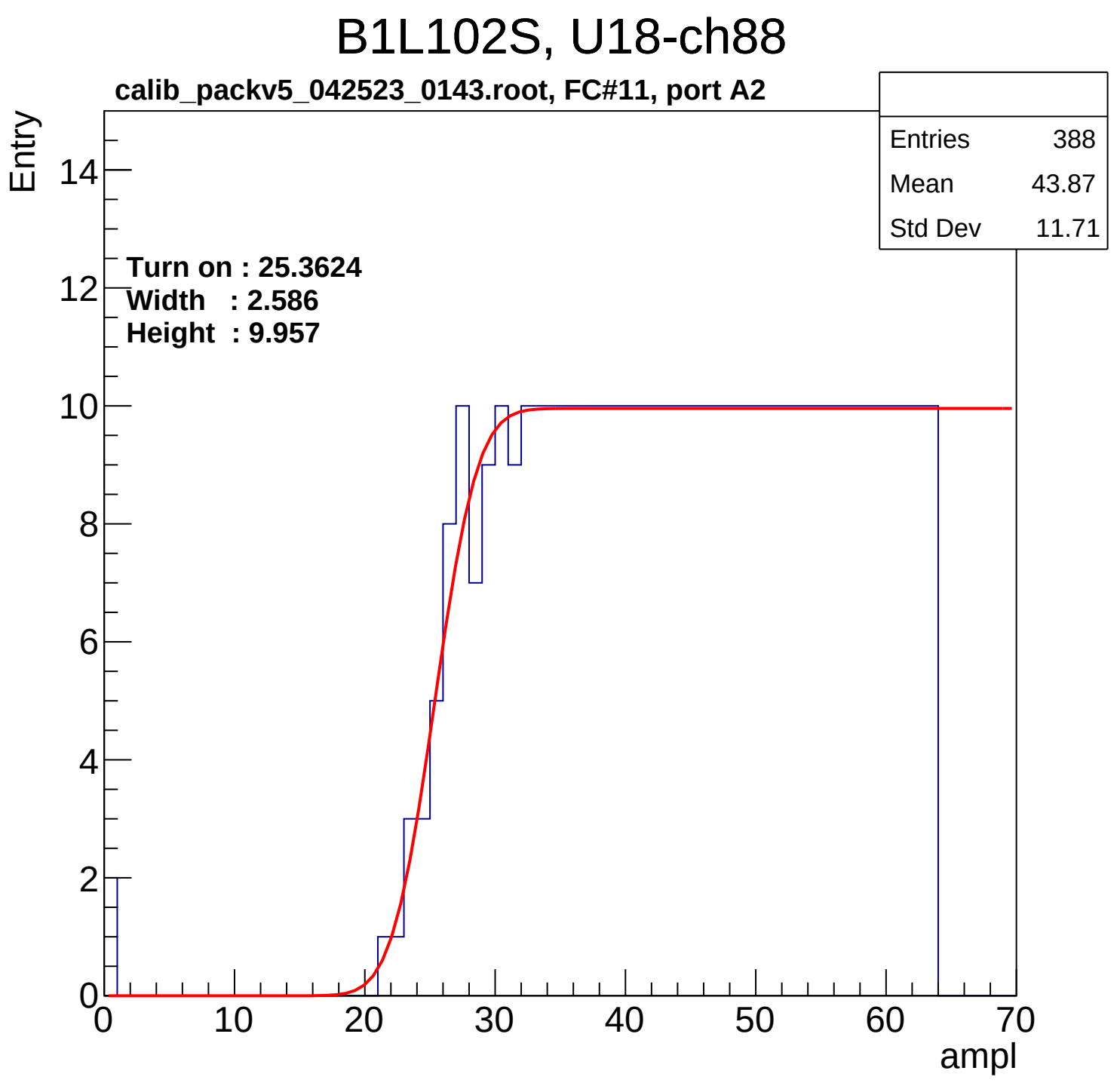
B1L102S, U18-ch88
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.87
Std Dev 11.71
Turn on : 25.3624
Width : 2.586
Height : 9.957
Entry
ampl
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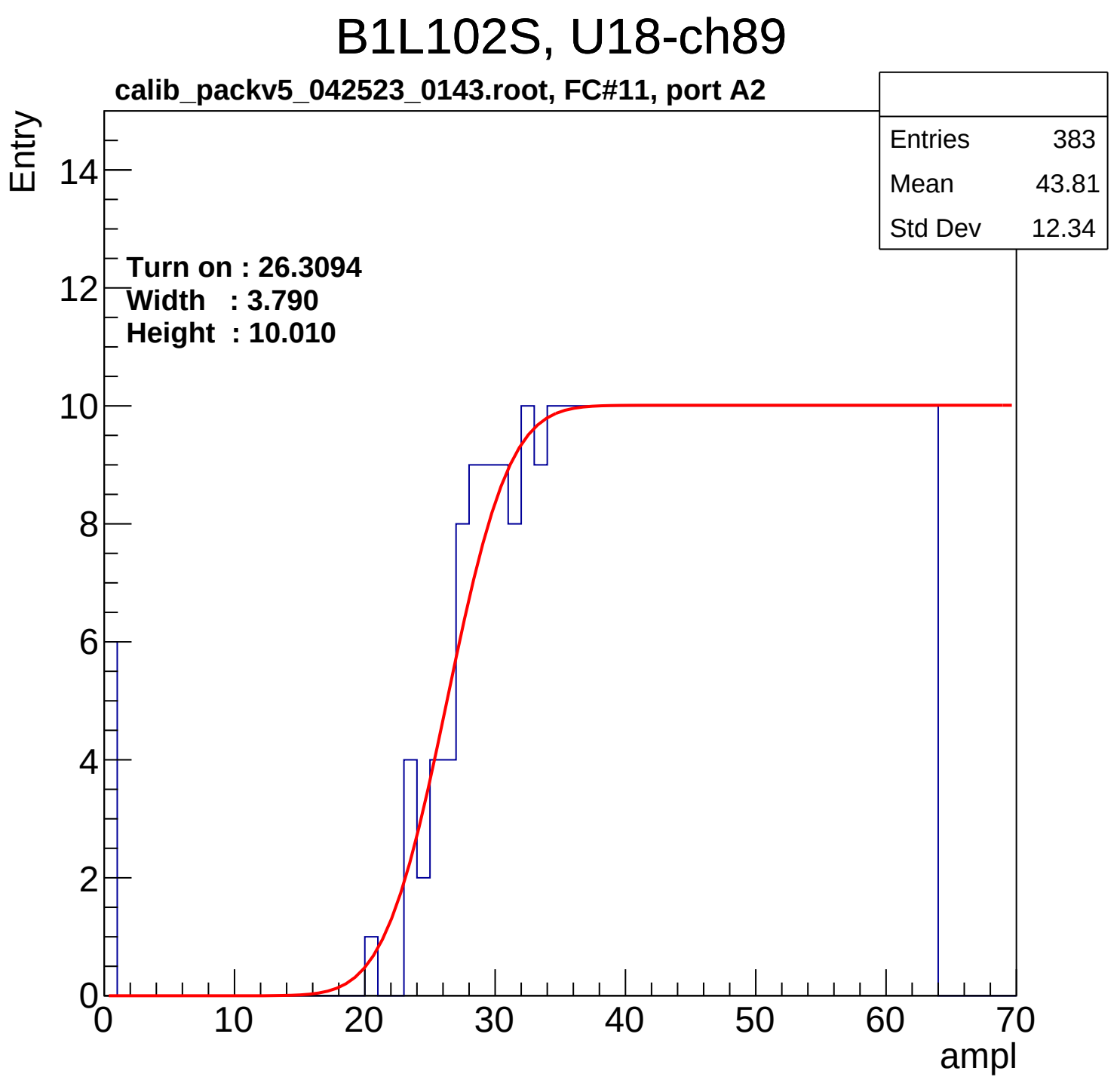
B1L102S, U18-ch89
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 43.81
Std Dev 12.34
Turn on : 26.3094
Width : 3.790
Height : 10.010
Entry
ampl
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8
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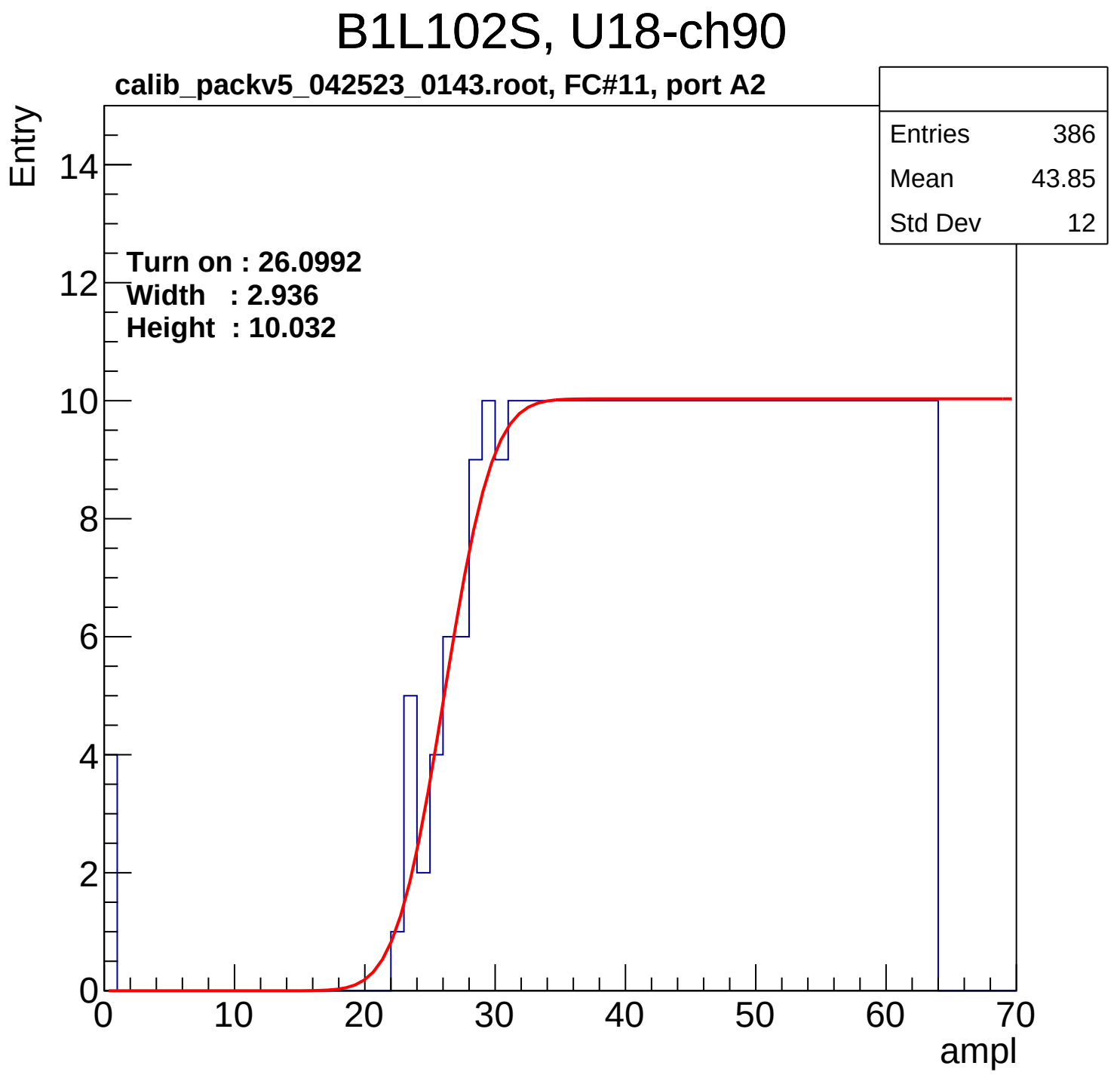
B1L102S, U18-ch90
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.85
Std Dev 12
Turn on : 26.0992
Width : 2.936
Height : 10.032
Entry
ampl
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6
8
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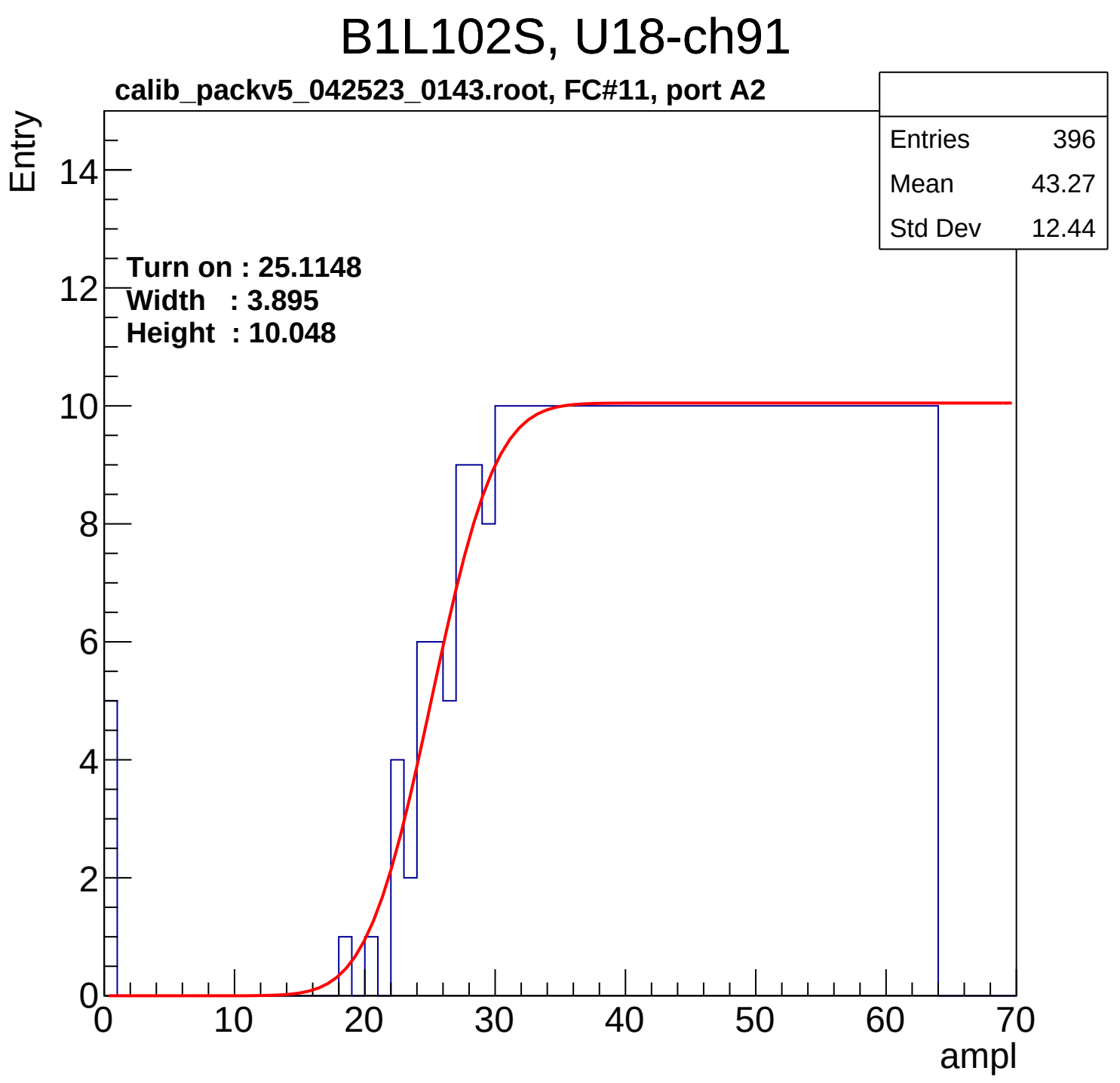
B1L102S, U18-ch91
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.27
Std Dev 12.44
Turn on : 25.1148
Width : 3.895
Height : 10.048
Entry
ampl
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8
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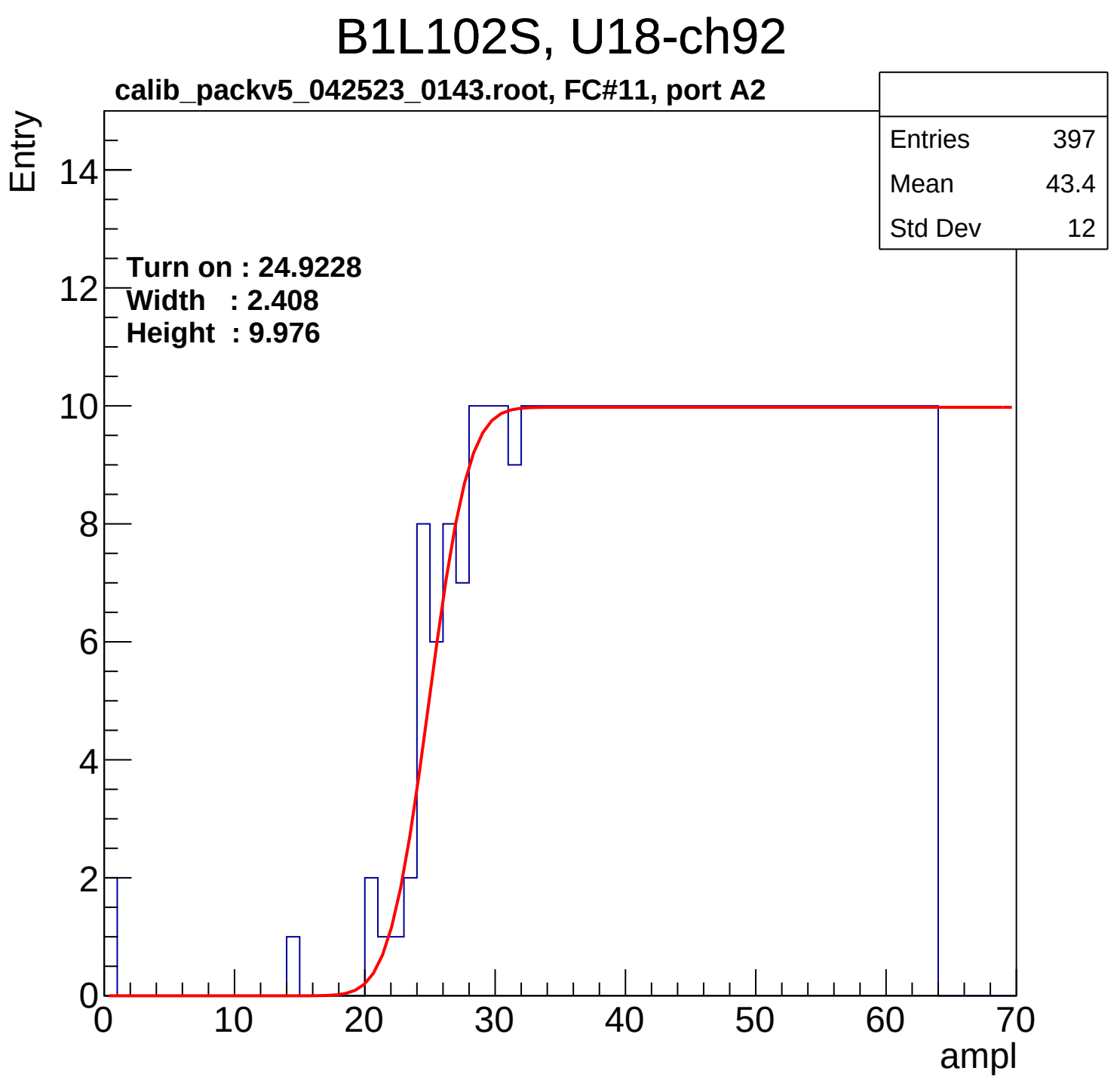
B1L102S, U18-ch92
calib_packv5_042523_0143.root, FC#11, port A2
Entries 397
Mean 43.4
Std Dev 12
Turn on : 24.9228
Width : 2.408
Height : 9.976
Entry
ampl
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8
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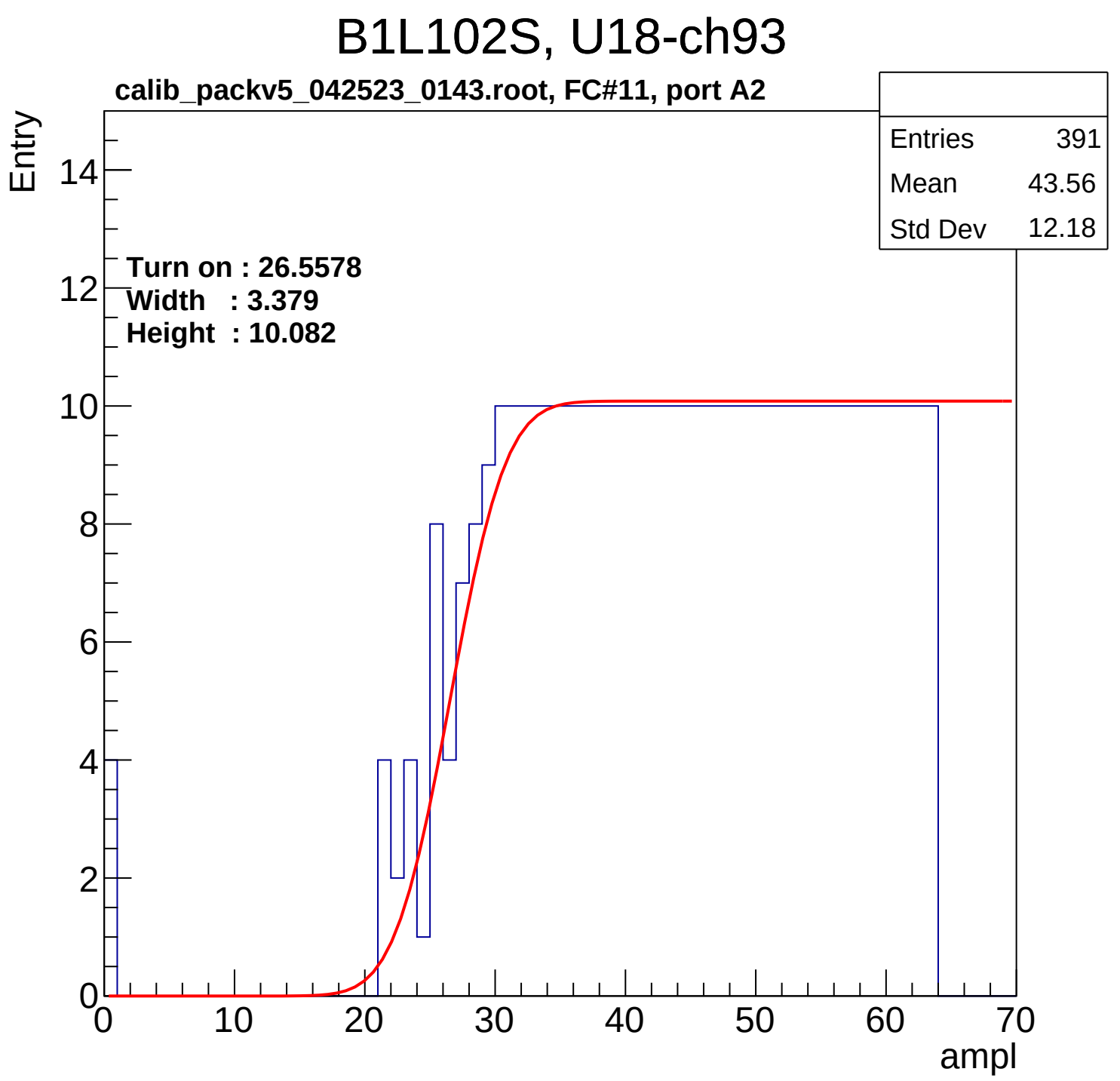
B1L102S, U18-ch93
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.56
Std Dev 12.18
Turn on : 26.5578
Width : 3.379
Height : 10.082
Entry
ampl
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8
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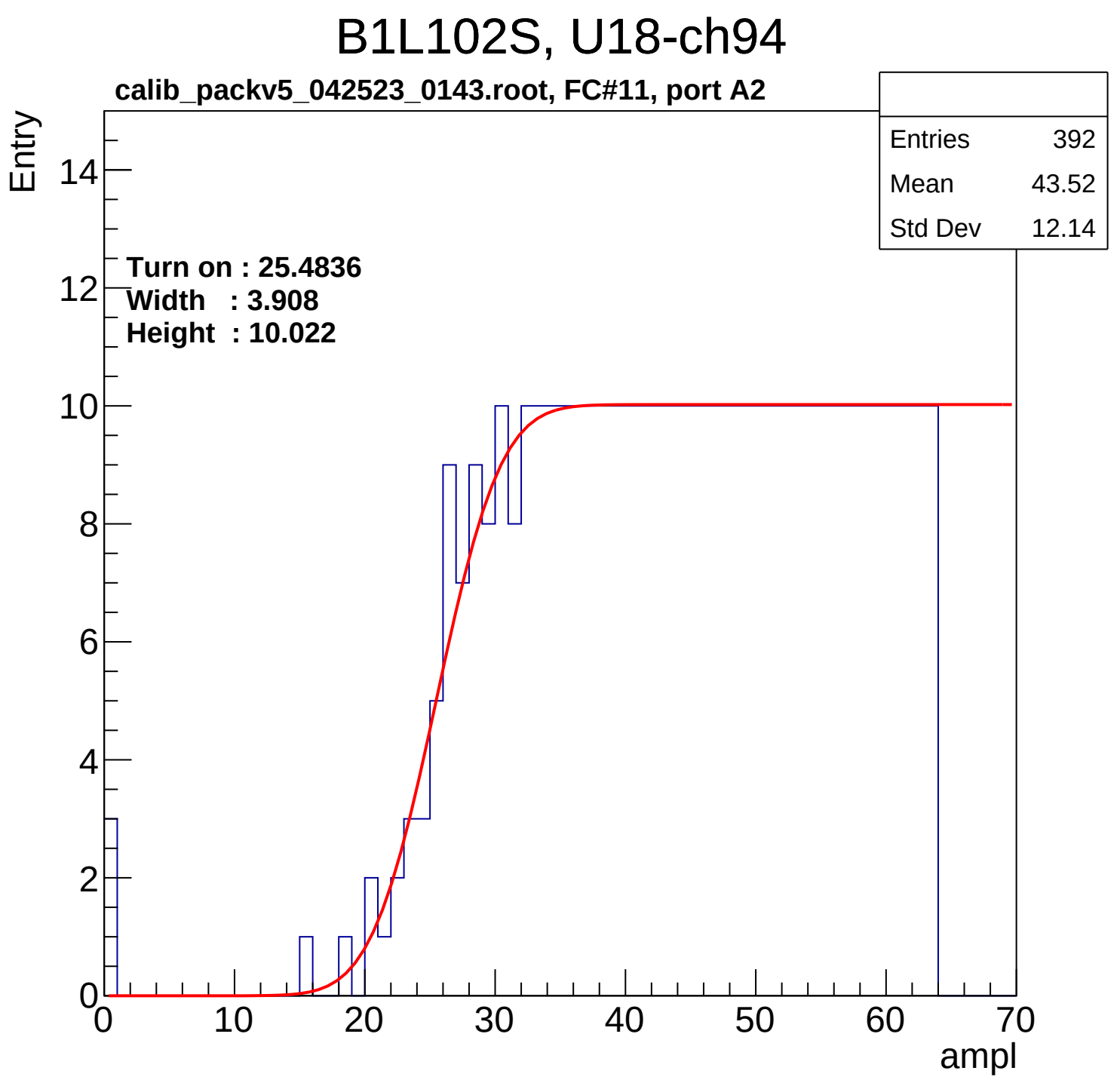
B1L102S, U18-ch94
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.52
Std Dev 12.14
Turn on : 25.4836
Width : 3.908
Height : 10.022
Entry
ampl
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4
6
8
10
12
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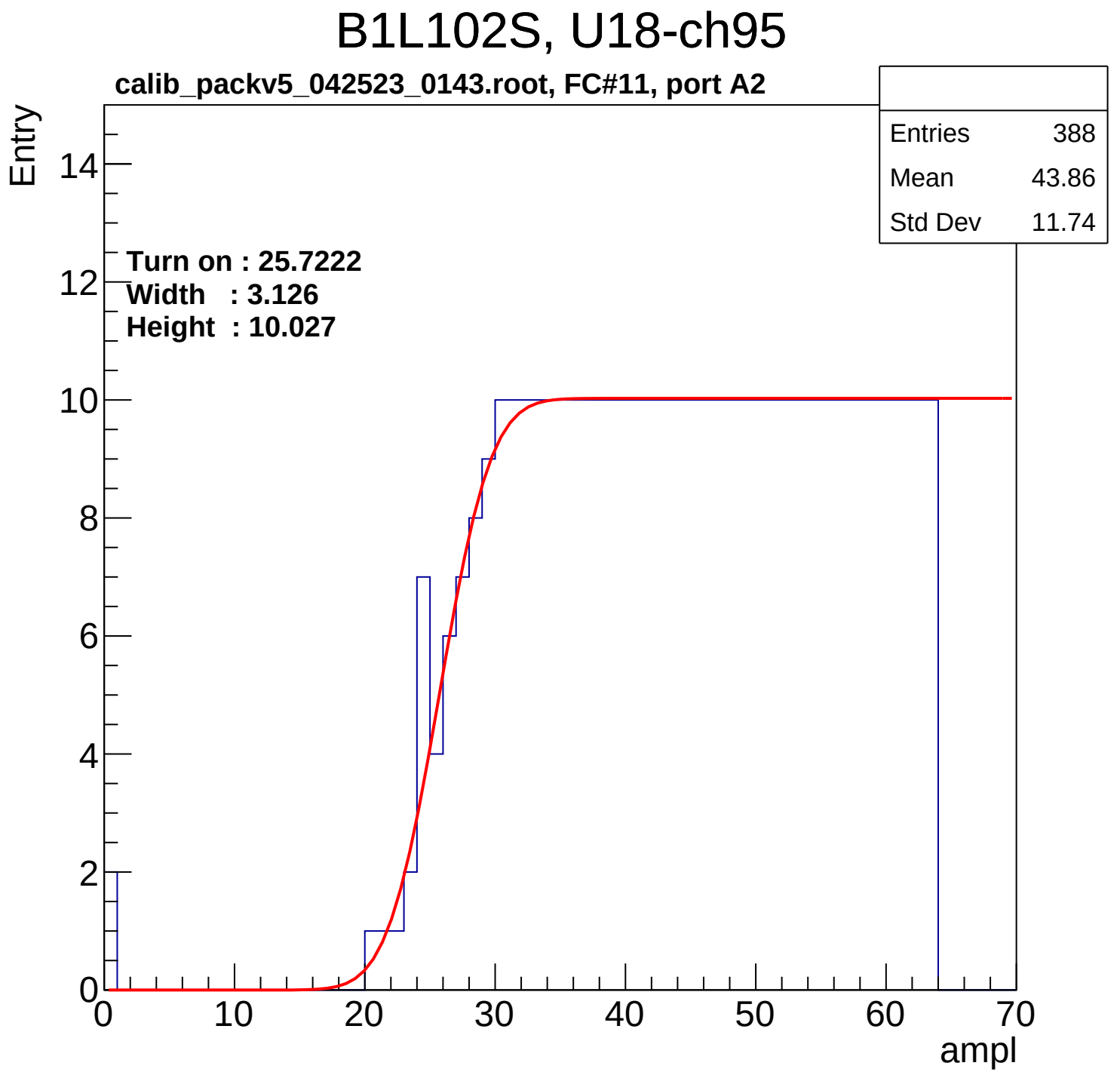
B1L102S, U18-ch95
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.86
Std Dev 11.74
Turn on : 25.7222
Width : 3.126
Height : 10.027
Entry
ampl
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6
8
10
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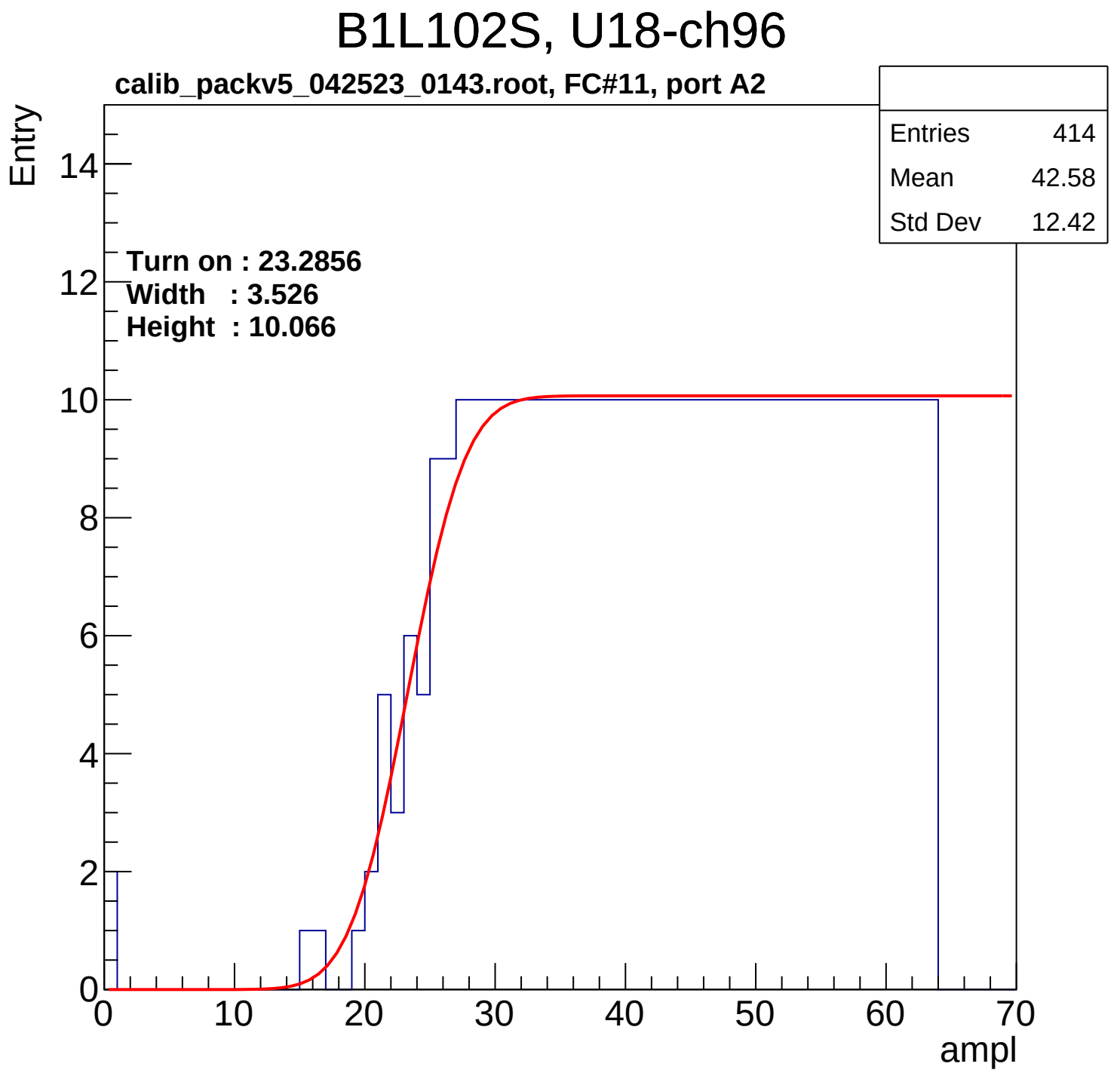
B1L102S, U18-ch96
calib_packv5_042523_0143.root, FC#11, port A2
Entries 414
Mean 42.58
Std Dev 12.42
Turn on : 23.2856
Width : 3.526
Height : 10.066
Entry
ampl
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6
8
10
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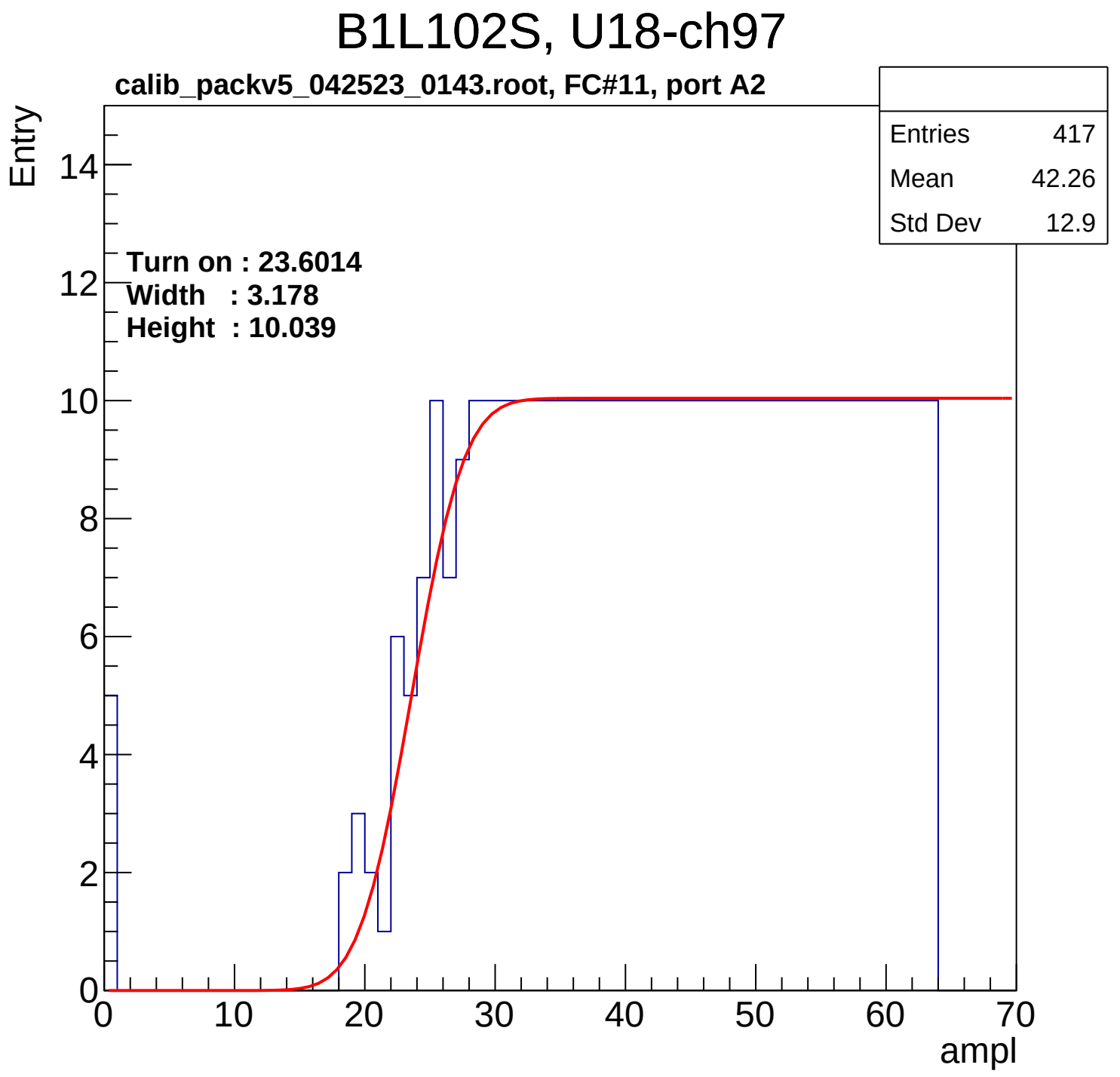
B1L102S, U18-ch97
calib_packv5_042523_0143.root, FC#11, port A2
Entries 417
Mean 42.26
Std Dev 12.9
Turn on : 23.6014
Width : 3.178
Height : 10.039
Entry
ampl
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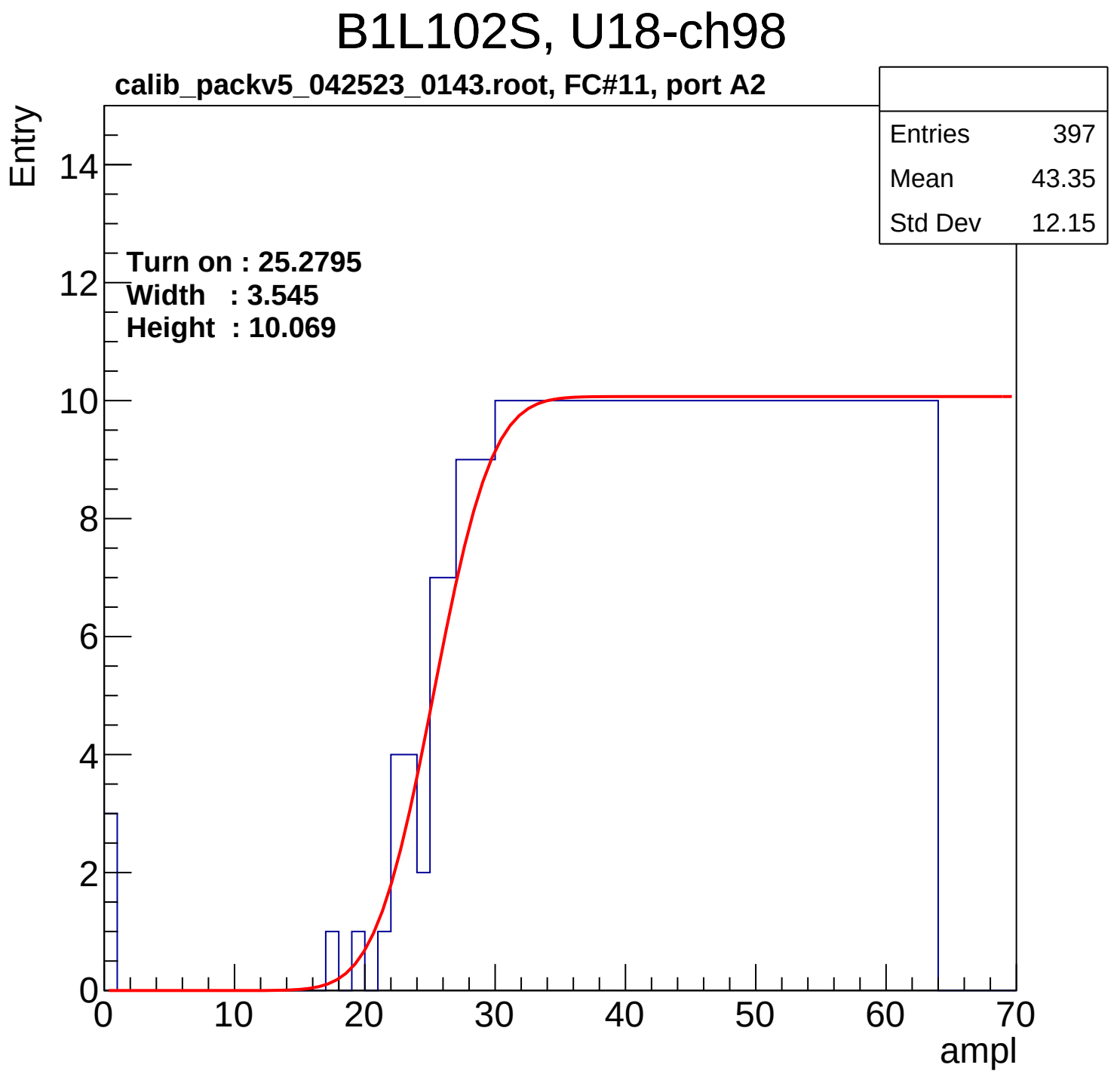
B1L102S, U18-ch98
calib_packv5_042523_0143.root, FC#11, port A2
Entries 397
Mean 43.35
Std Dev 12.15
Turn on : 25.2795
Width : 3.545
Height : 10.069
Entry
ampl
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4
6
8
10
12
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0
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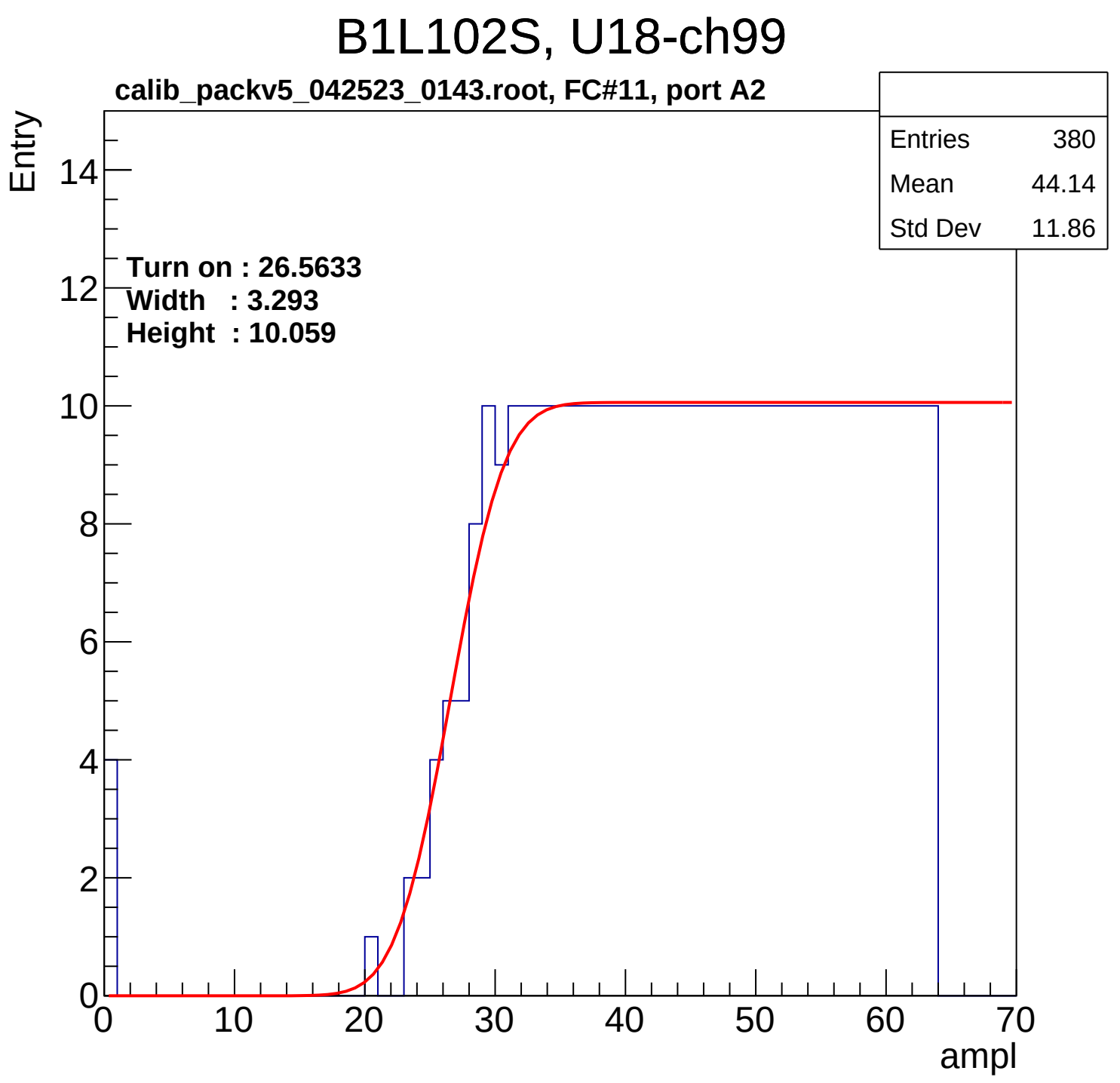
B1L102S, U18-ch99
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.14
Std Dev 11.86
Turn on : 26.5633
Width : 3.293
Height : 10.059
Entry
ampl
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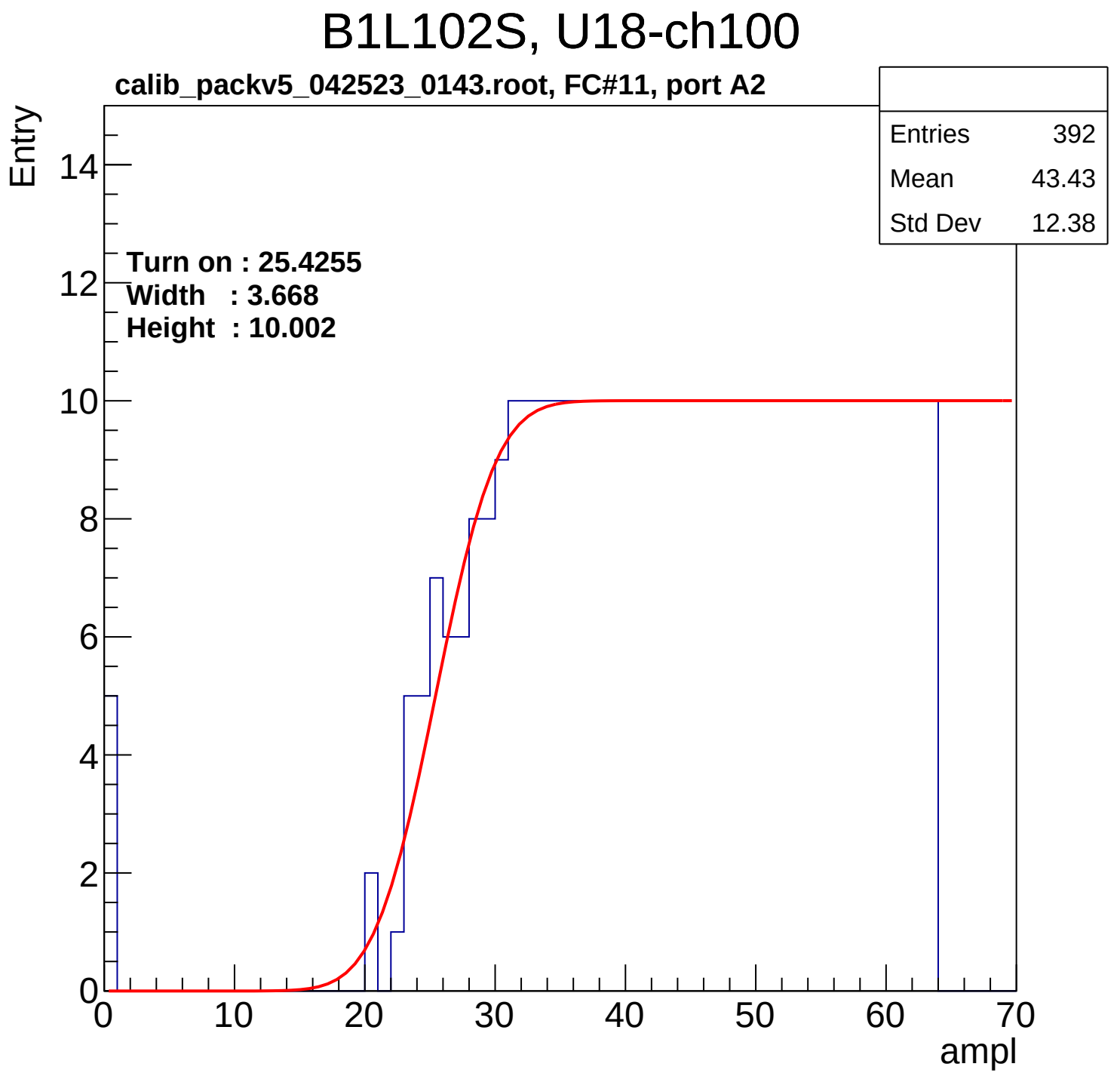
B1L102S, U18-ch100
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.43
Std Dev 12.38
Turn on : 25.4255
Width : 3.668
Height : 10.002
Entry
ampl
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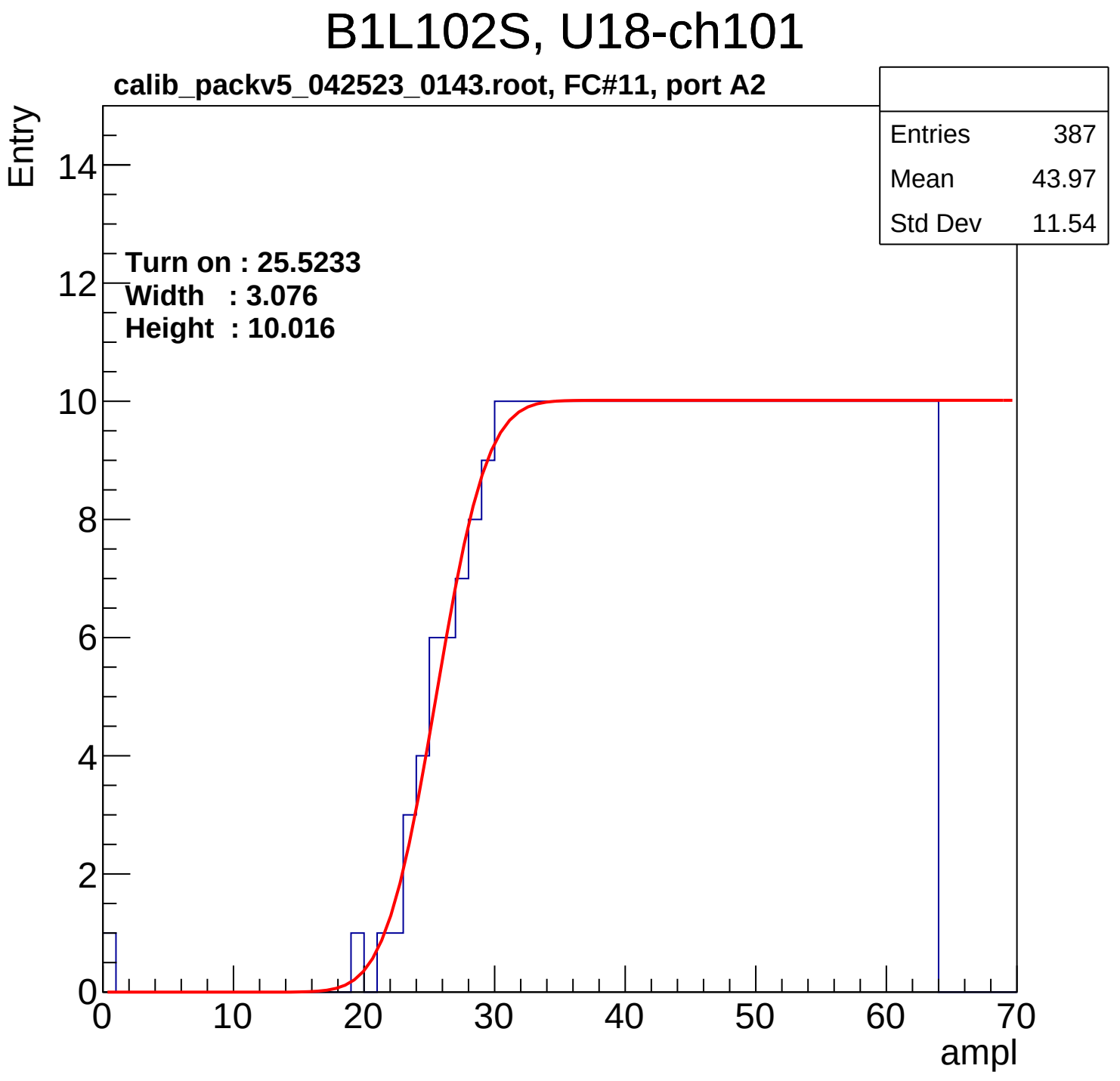
B1L102S, U18-ch101
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.97
Std Dev 11.54
Turn on : 25.5233
Width : 3.076
Height : 10.016
Entry
ampl
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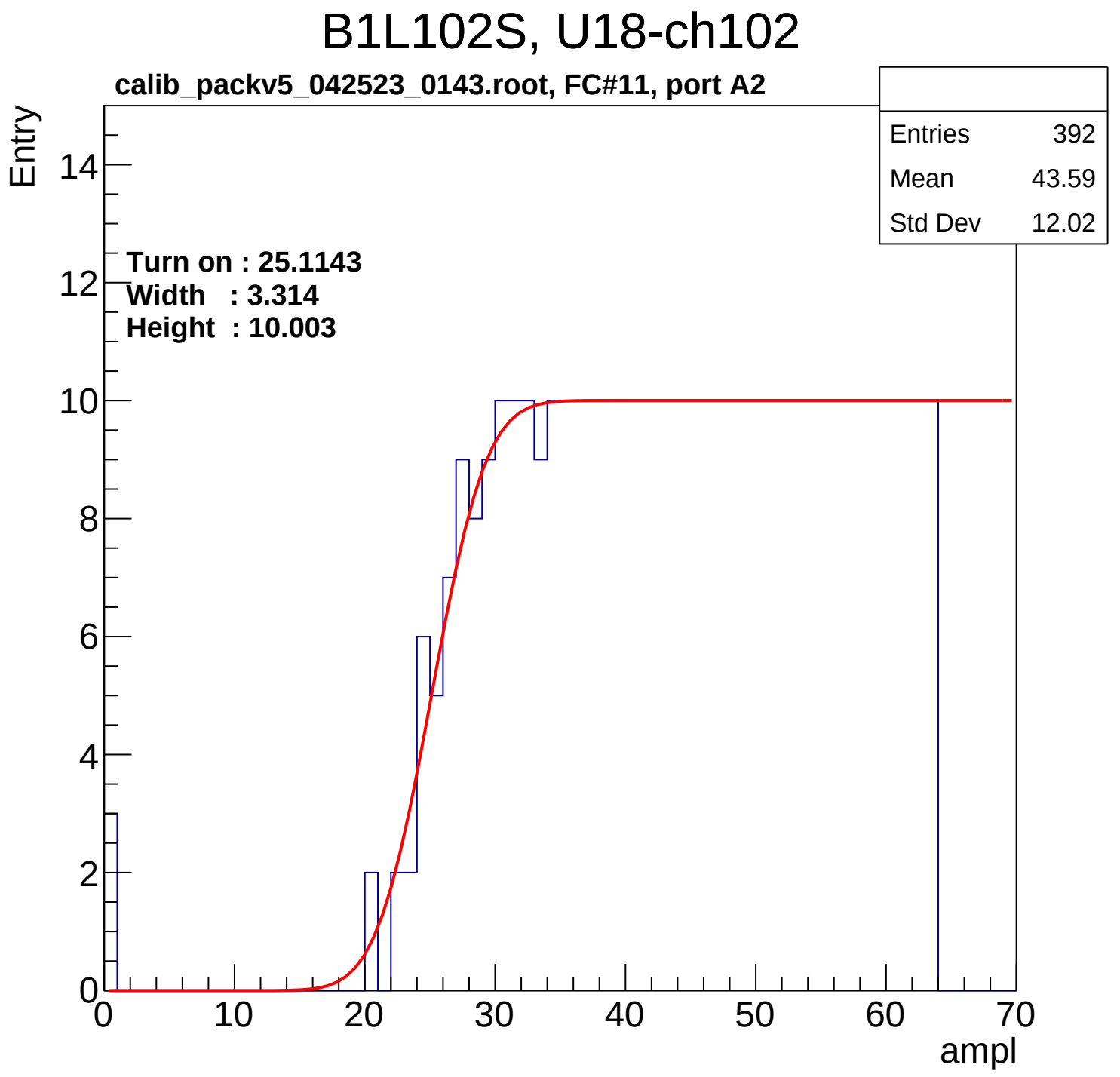
B1L102S, U18-ch102
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.59
Std Dev 12.02
Turn on : 25.1143
Width : 3.314
Height : 10.003
Entry
ampl
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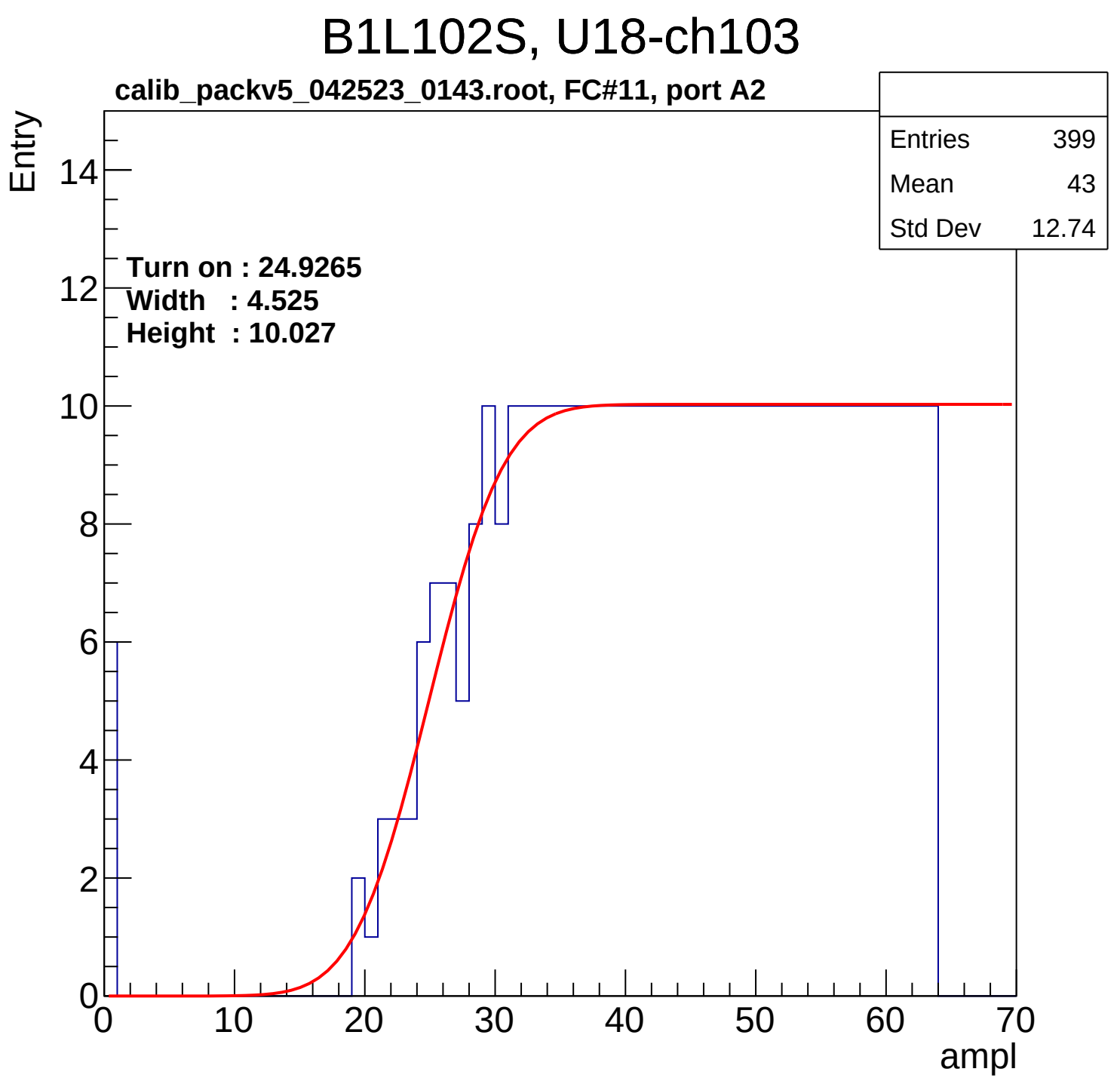
B1L102S, U18-ch103
calib_packv5_042523_0143.root, FC#11, port A2
Entries 399
Mean 43
Std Dev 12.74
Turn on : 24.9265
Width : 4.525
Height : 10.027
Entry
ampl
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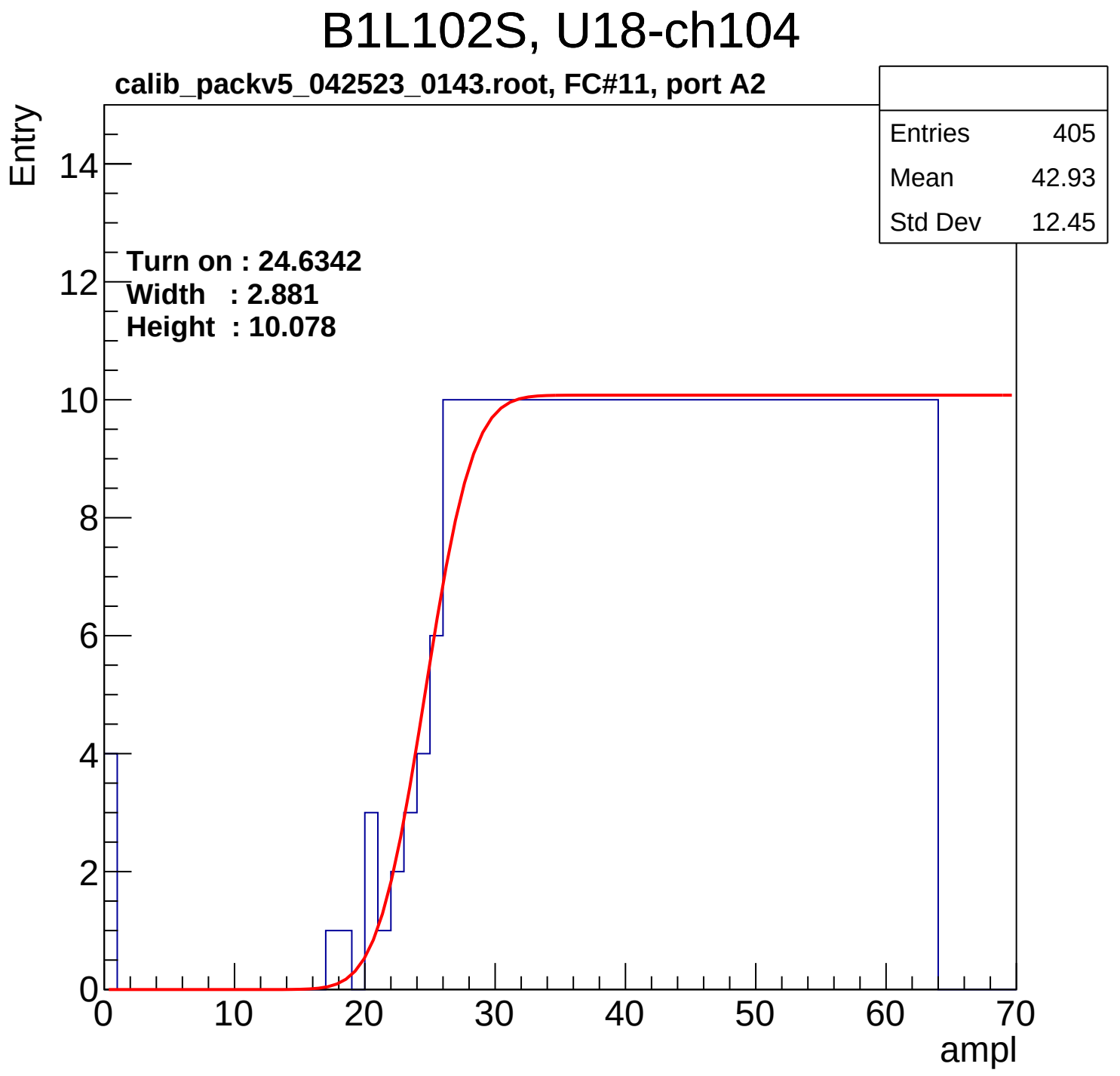
B1L102S, U18-ch104
calib_packv5_042523_0143.root, FC#11, port A2
Entries 405
Mean 42.93
Std Dev 12.45
Turn on : 24.6342
Width : 2.881
Height : 10.078
Entry
ampl
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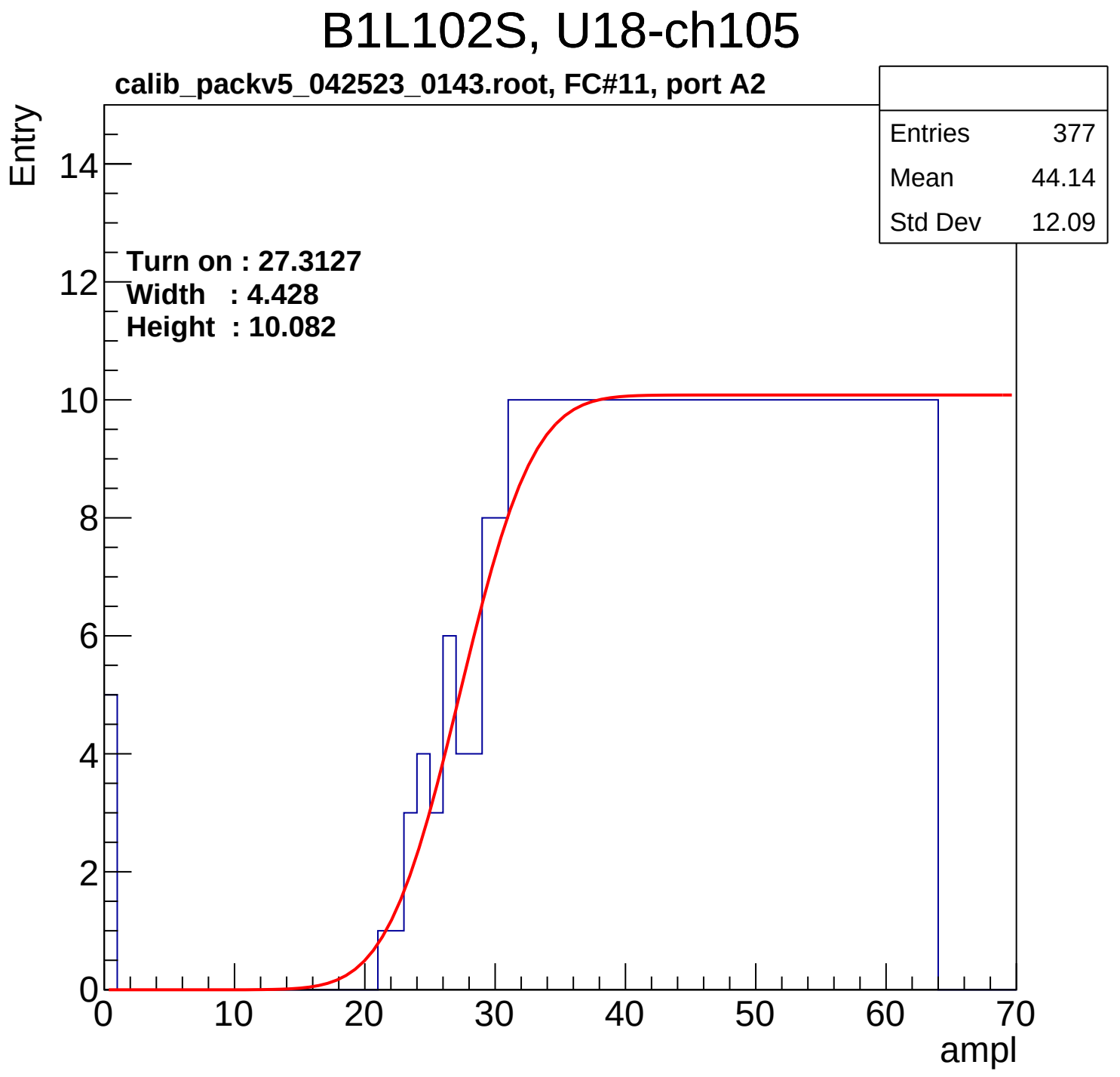
B1L102S, U18-ch105
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.14
Std Dev 12.09
Turn on : 27.3127
Width : 4.428
Height : 10.082
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ampl
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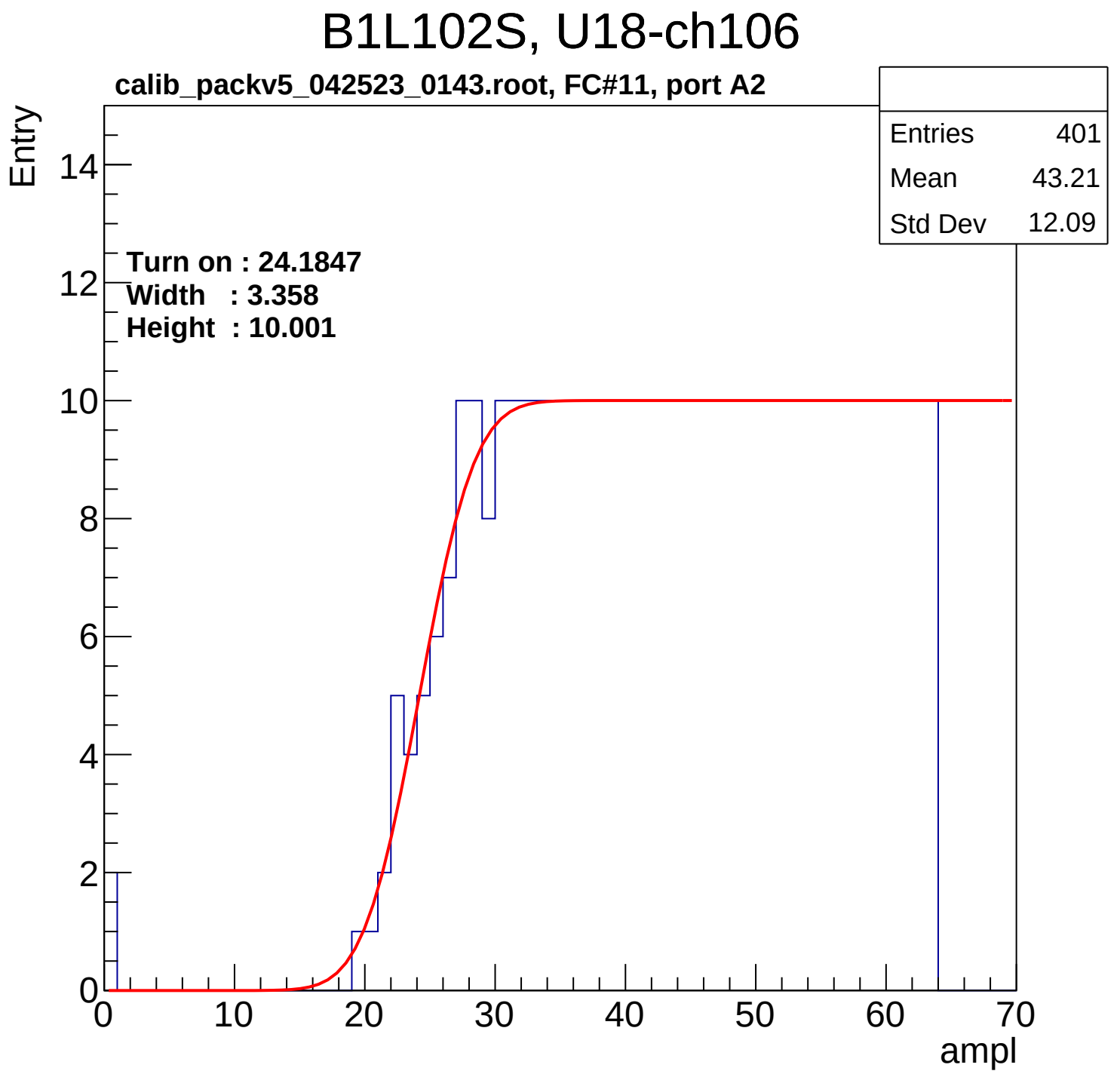
B1L102S, U18-ch106
calib_packv5_042523_0143.root, FC#11, port A2
Entries 401
Mean 43.21
Std Dev 12.09
Turn on : 24.1847
Width : 3.358
Height : 10.001
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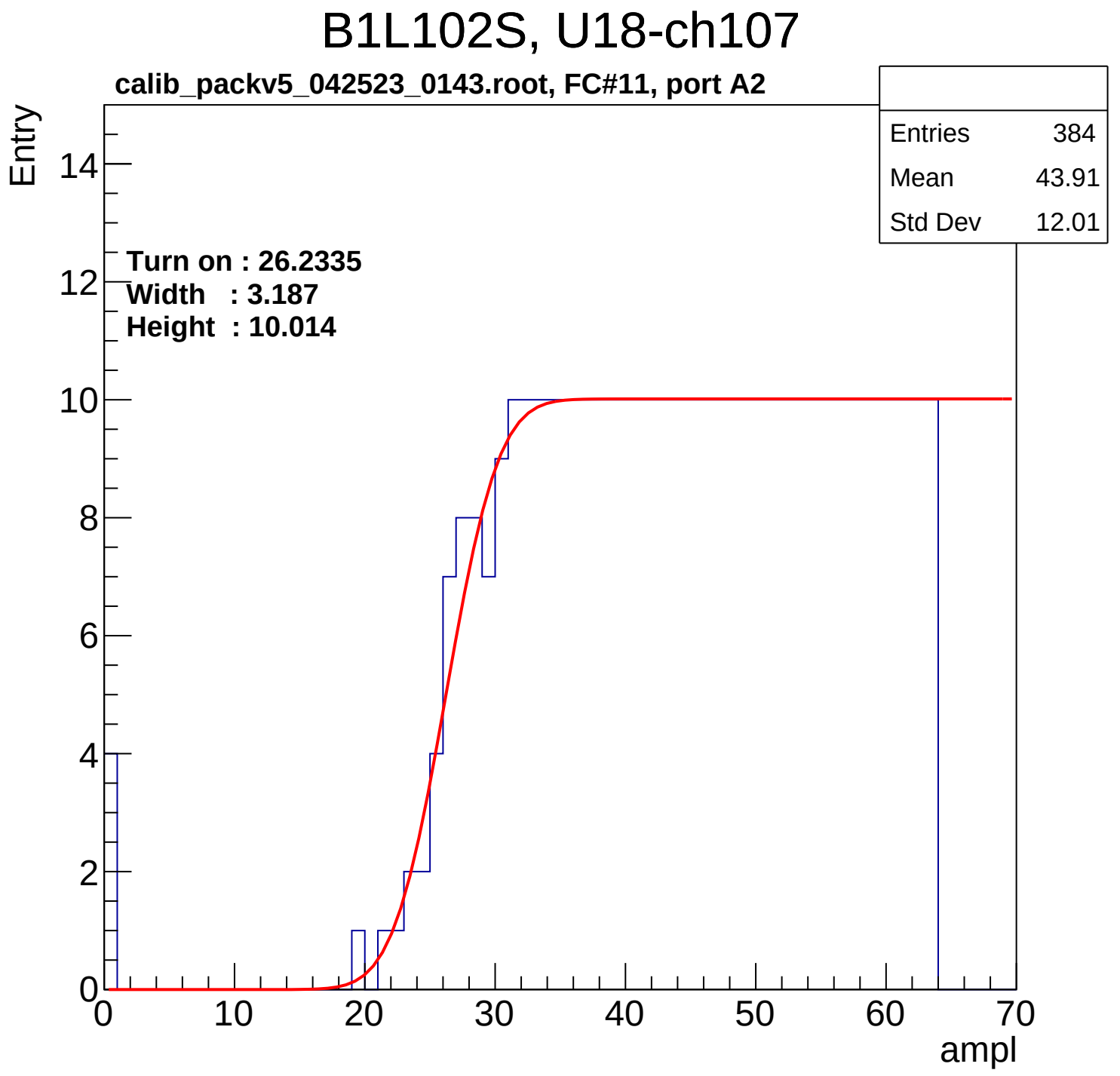
B1L102S, U18-ch107
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 43.91
Std Dev 12.01
Turn on : 26.2335
Width : 3.187
Height : 10.014
Entry
ampl
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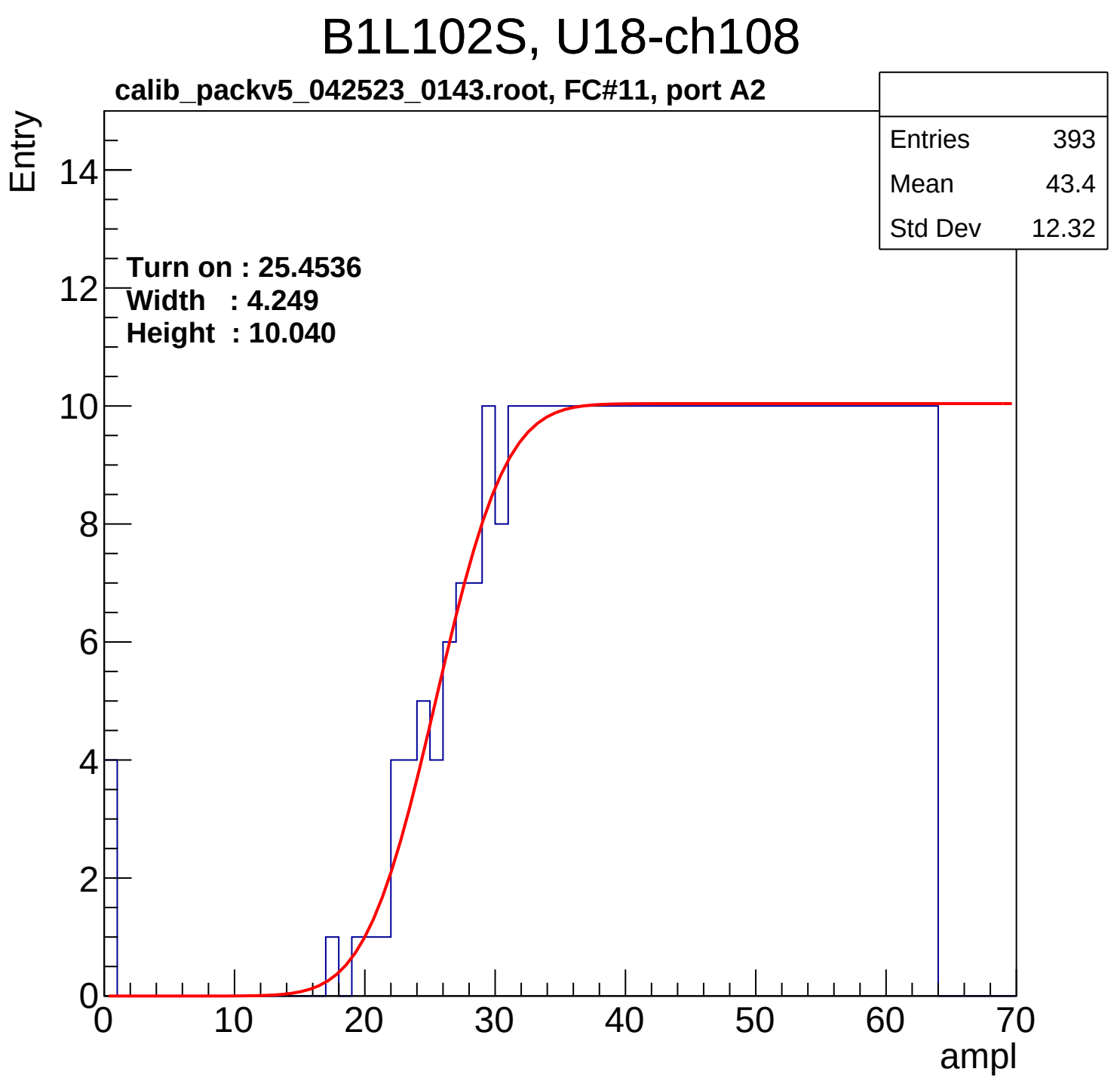
B1L102S, U18-ch108
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.4
Std Dev 12.32
Turn on : 25.4536
Width : 4.249
Height : 10.040
Entry
ampl
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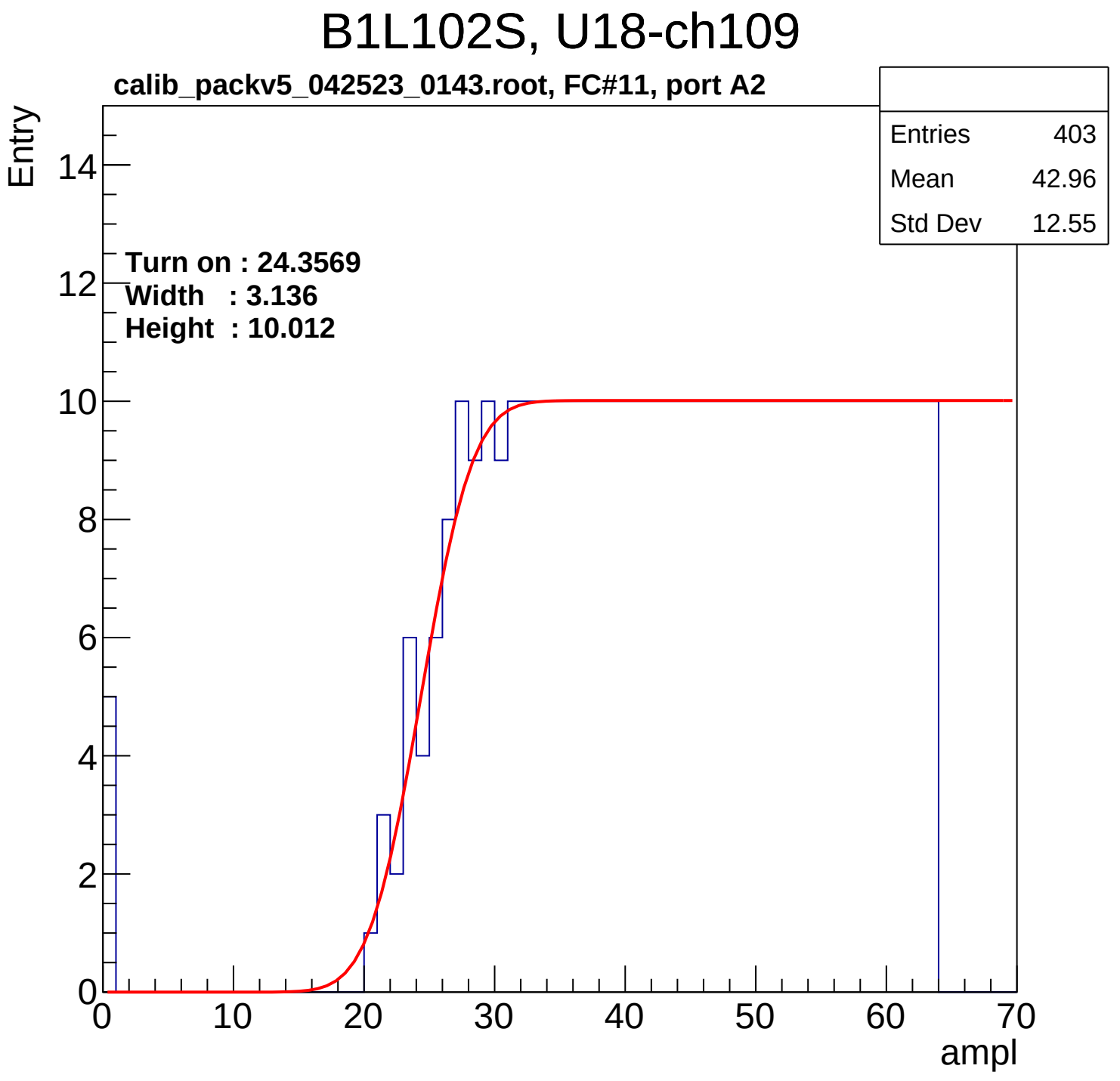
B1L102S, U18-ch109
calib_packv5_042523_0143.root, FC#11, port A2
Entries 403
Mean 42.96
Std Dev 12.55
Turn on : 24.3569
Width : 3.136
Height : 10.012
Entry
ampl
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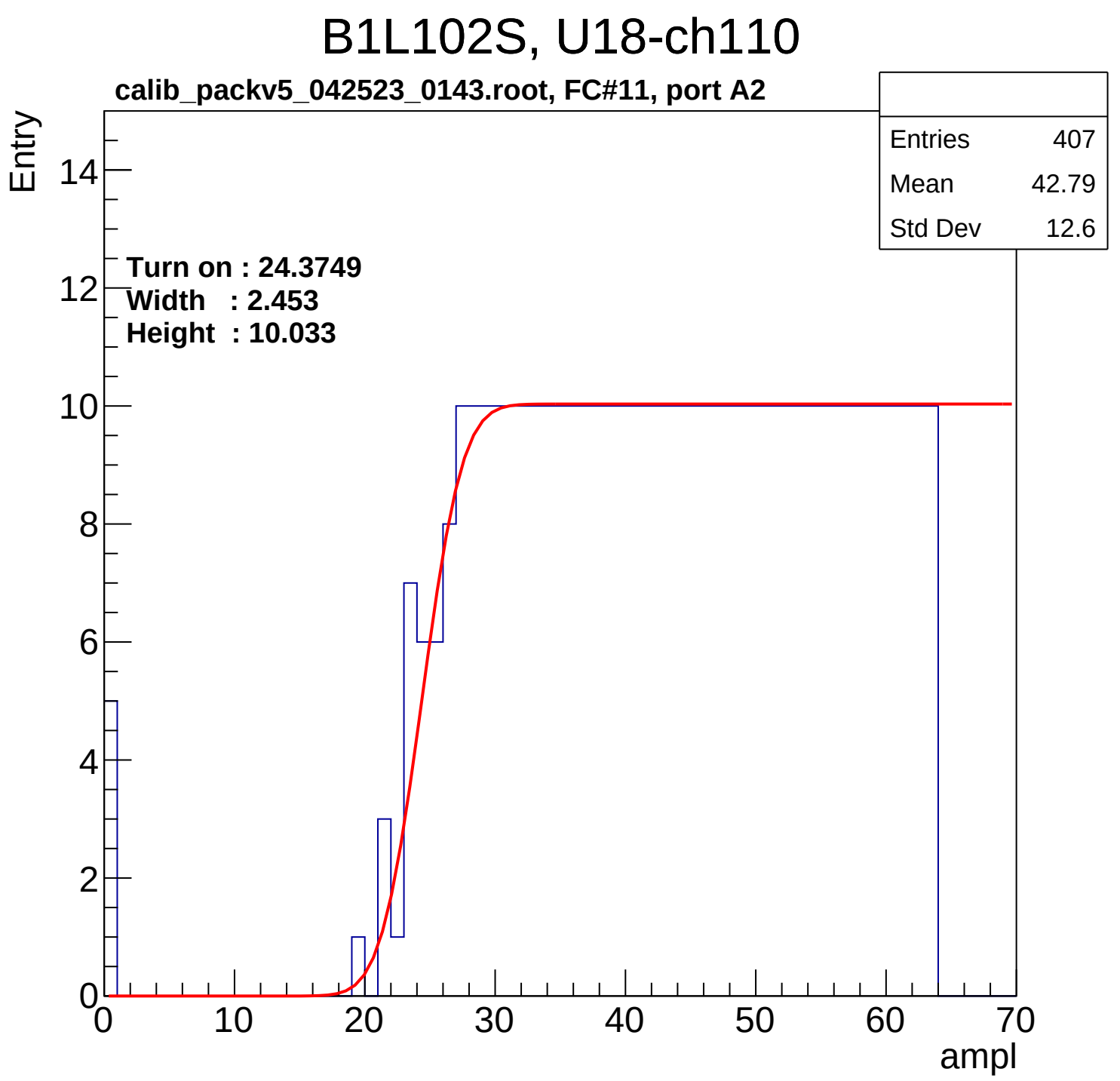
B1L102S, U18-ch110
calib_packv5_042523_0143.root, FC#11, port A2
Entries 407
Mean 42.79
Std Dev 12.6
Turn on : 24.3749
Width : 2.453
Height : 10.033
Entry
ampl
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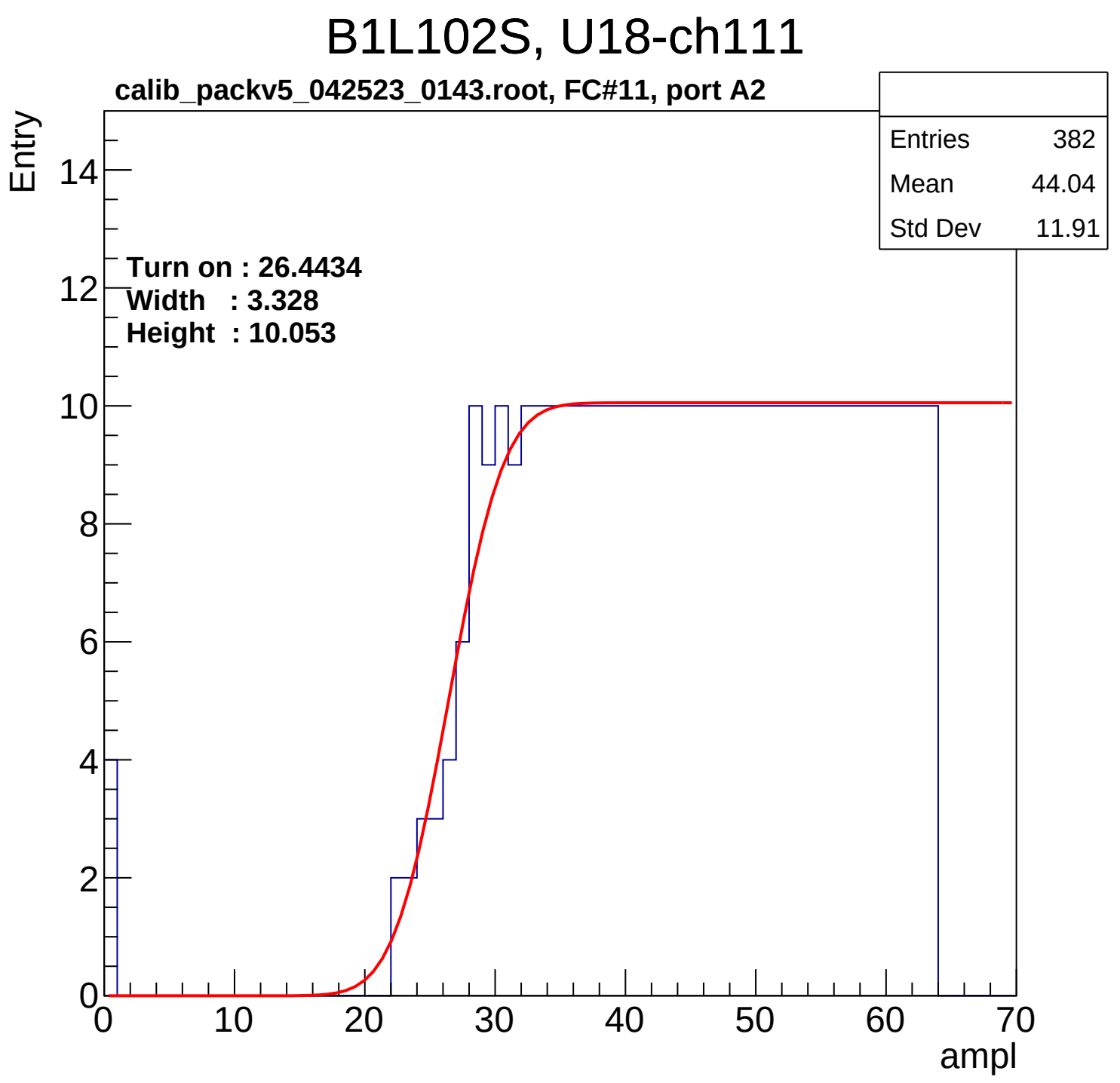
B1L102S, U18-ch111
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.04
Std Dev 11.91
Turn on : 26.4434
Width : 3.328
Height : 10.053
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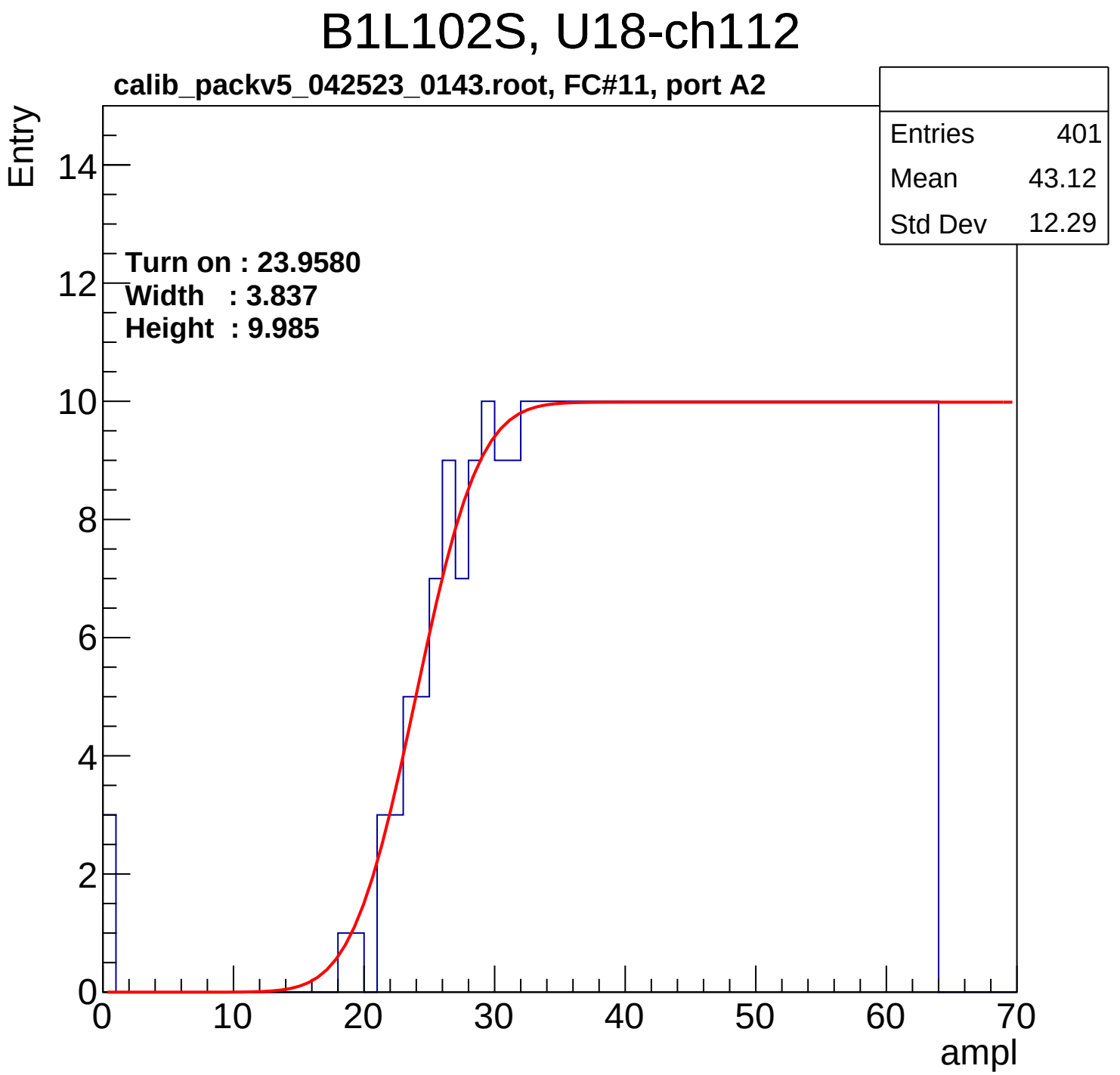
B1L102S, U18-ch112
calib_packv5_042523_0143.root, FC#11, port A2
Entries 401
Mean 43.12
Std Dev 12.29
Turn on : 23.9580
Width : 3.837
Height : 9.985
Entry
ampl
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8
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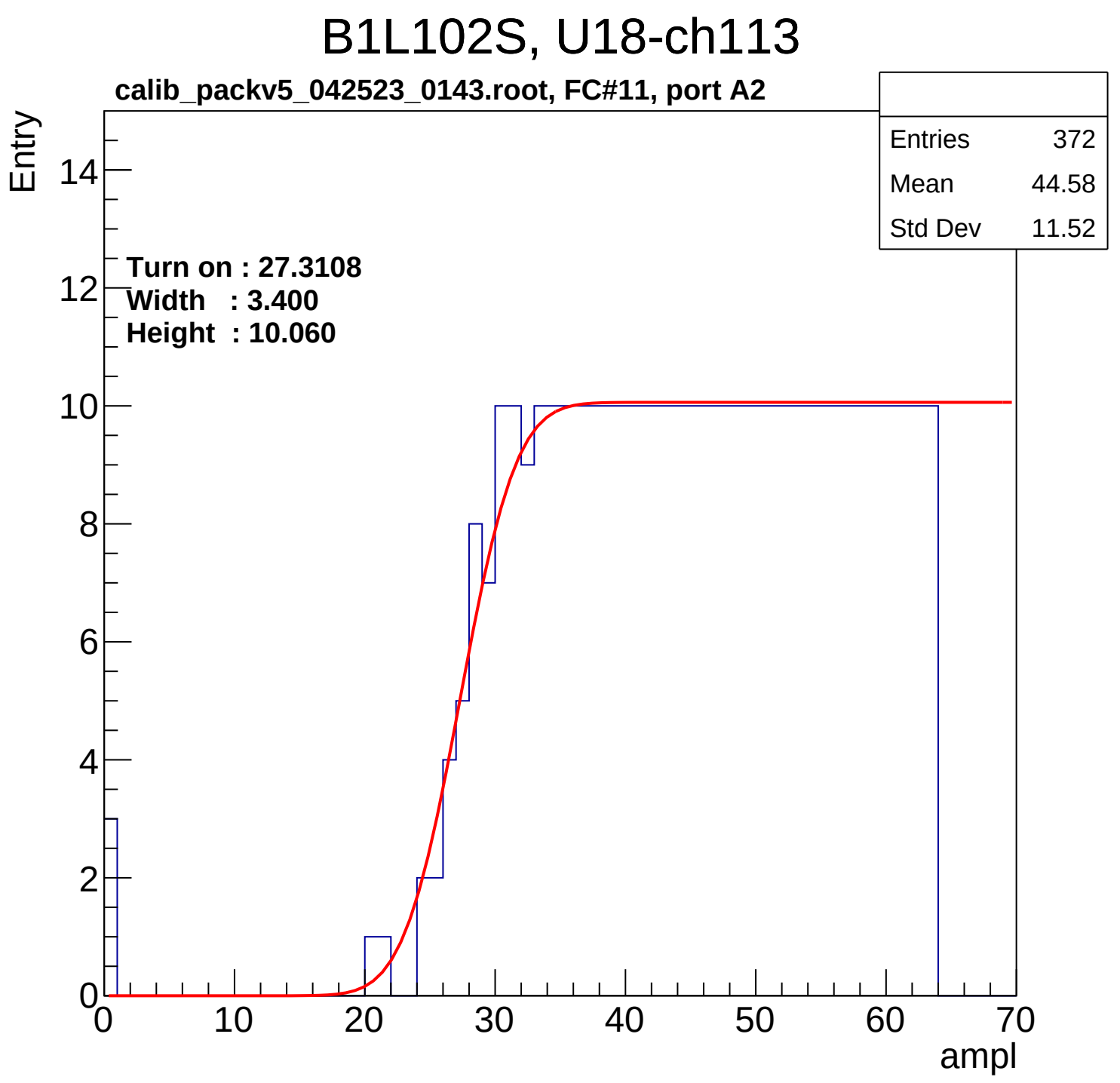
B1L102S, U18-ch113
calib_packv5_042523_0143.root, FC#11, port A2
Entries 372
Mean 44.58
Std Dev 11.52
Turn on : 27.3108
Width : 3.400
Height : 10.060
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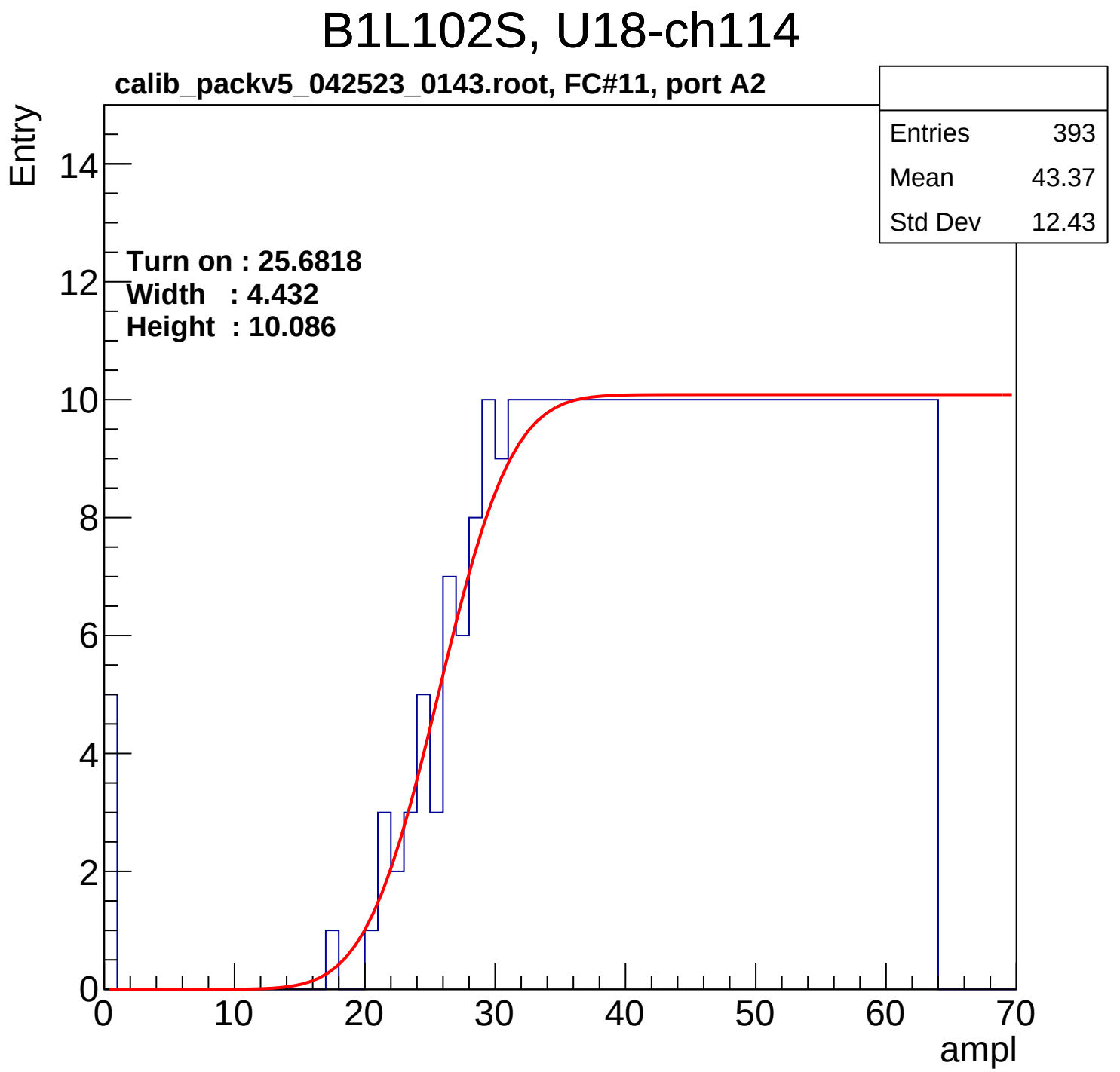
B1L102S, U18-ch114
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.37
Std Dev 12.43
Turn on : 25.6818
Width : 4.432
Height : 10.086
Entry
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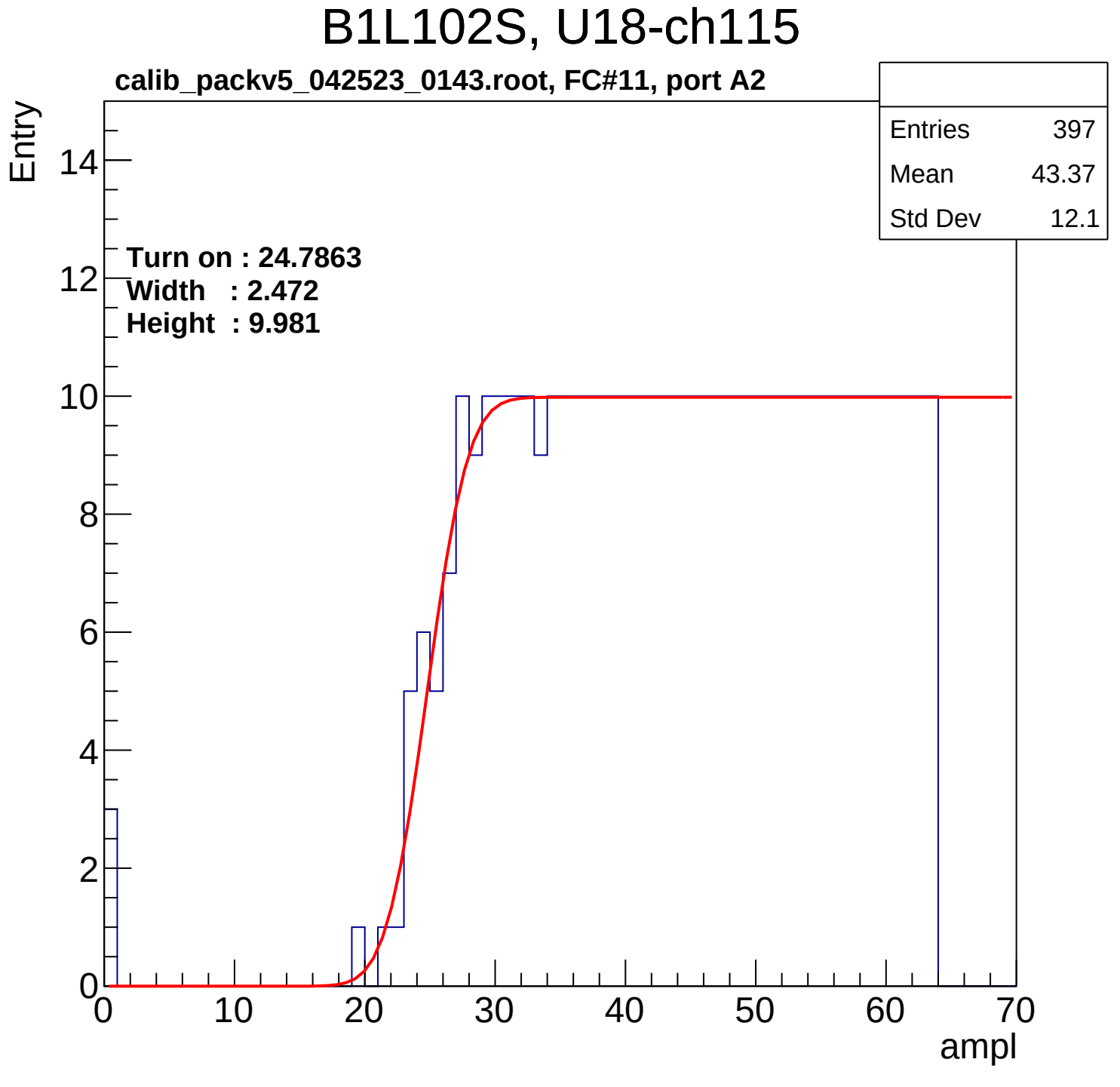
B1L102S, U18-ch115
calib_packv5_042523_0143.root, FC#11, port A2
Entries 397
Mean 43.37
Std Dev 12.1
Turn on : 24.7863
Width : 2.472
Height : 9.981
Entry
ampl
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6
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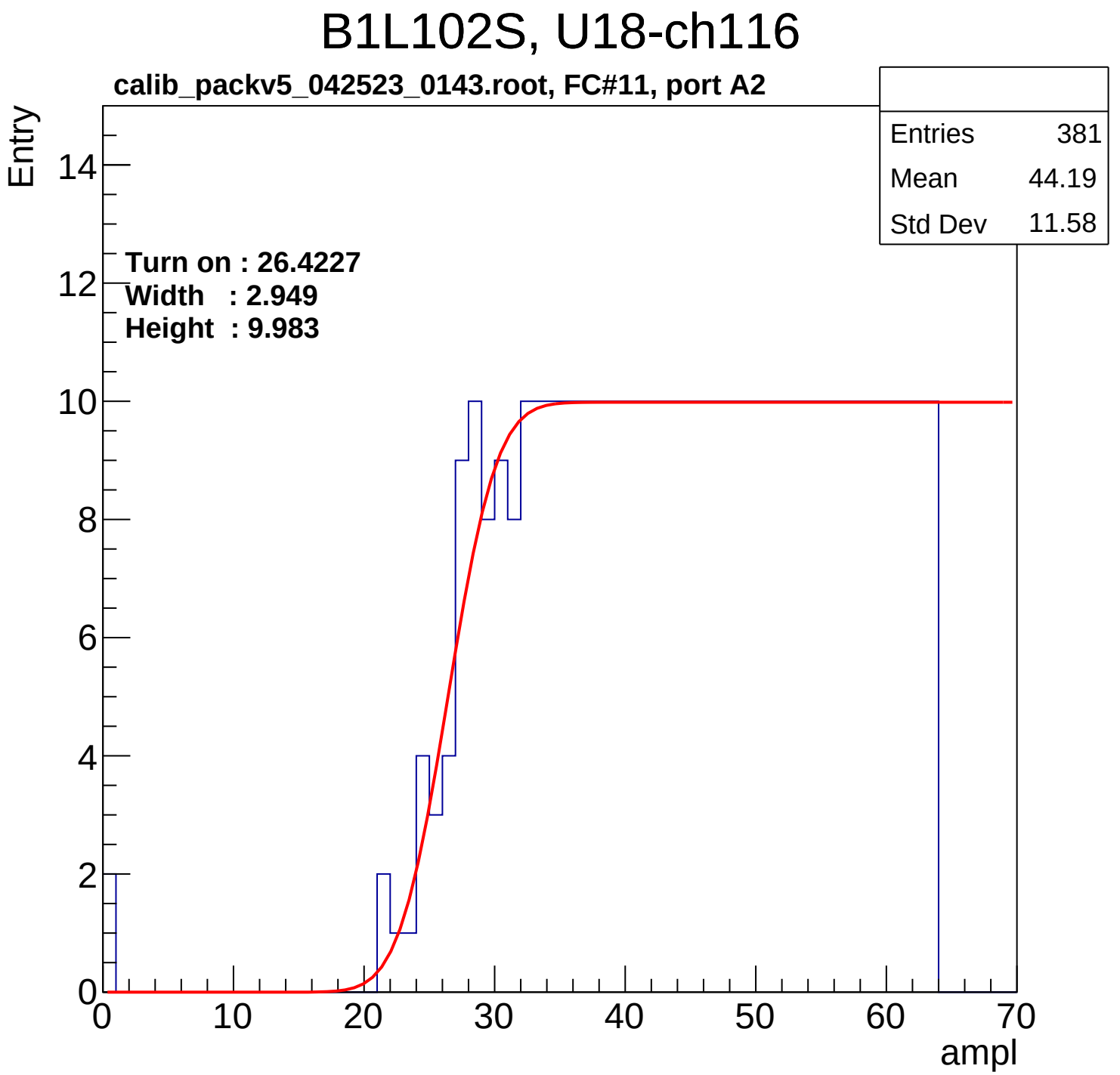
B1L102S, U18-ch116
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.19
Std Dev 11.58
Turn on : 26.4227
Width : 2.949
Height : 9.983
Entry
ampl
0
2
4
6
8
10
12
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0
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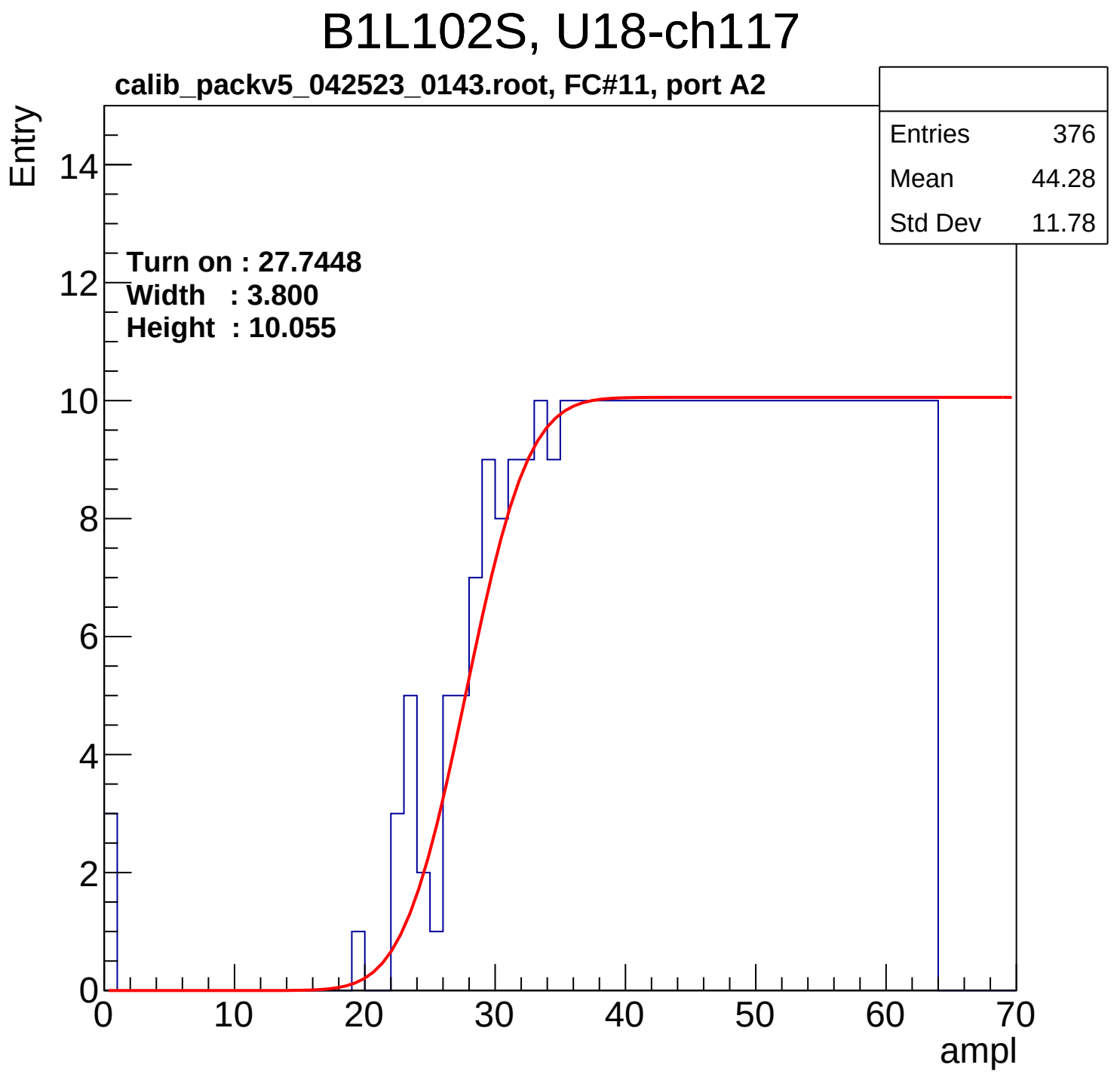
B1L102S, U18-ch117
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.28
Std Dev 11.78
Turn on : 27.7448
Width : 3.800
Height : 10.055
Entry
ampl
0
2
4
6
8
10
12
14
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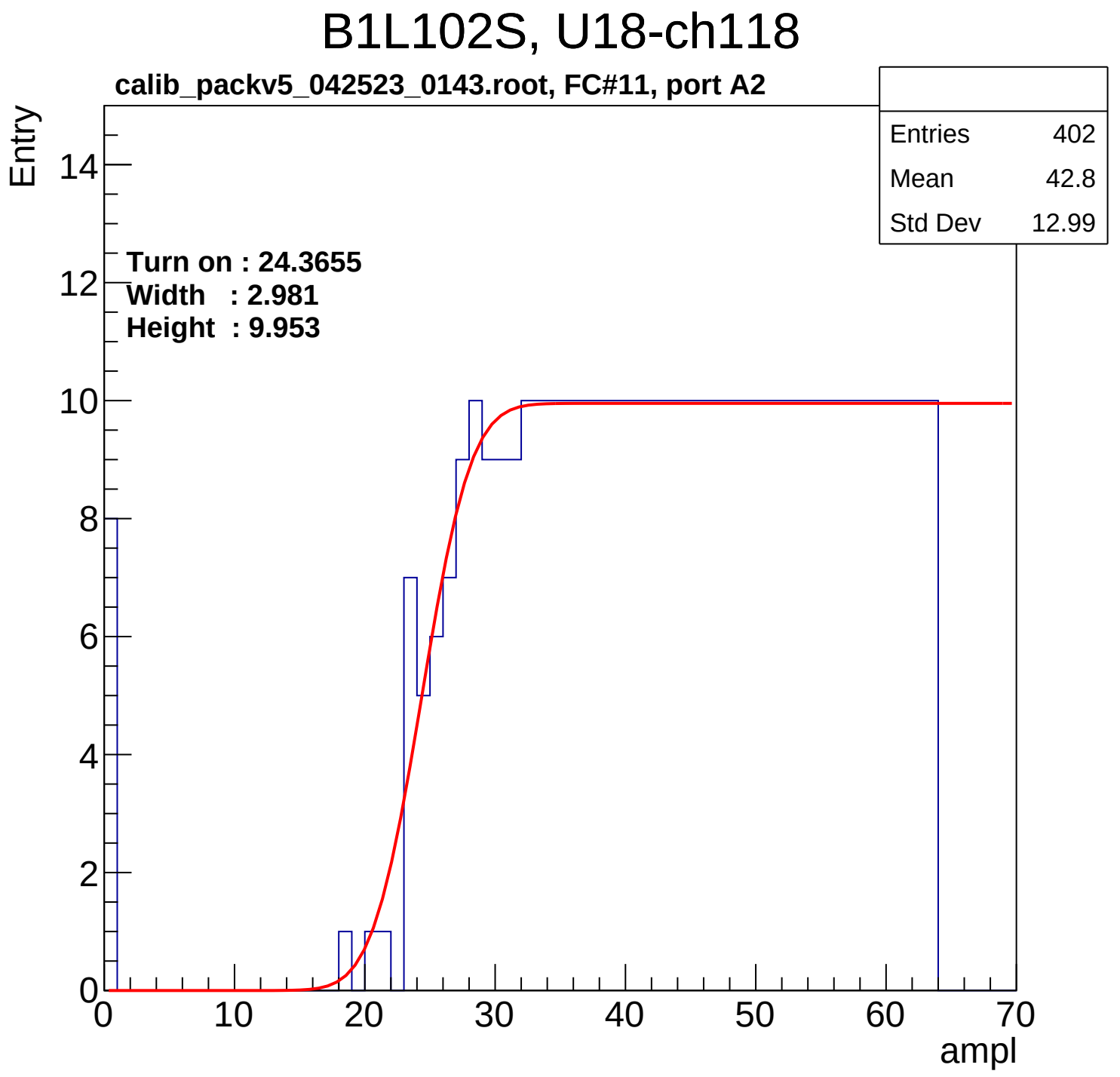
B1L102S, U18-ch118
calib_packv5_042523_0143.root, FC#11, port A2
Entries 402
Mean 42.8
Std Dev 12.99
Turn on : 24.3655
Width : 2.981
Height : 9.953
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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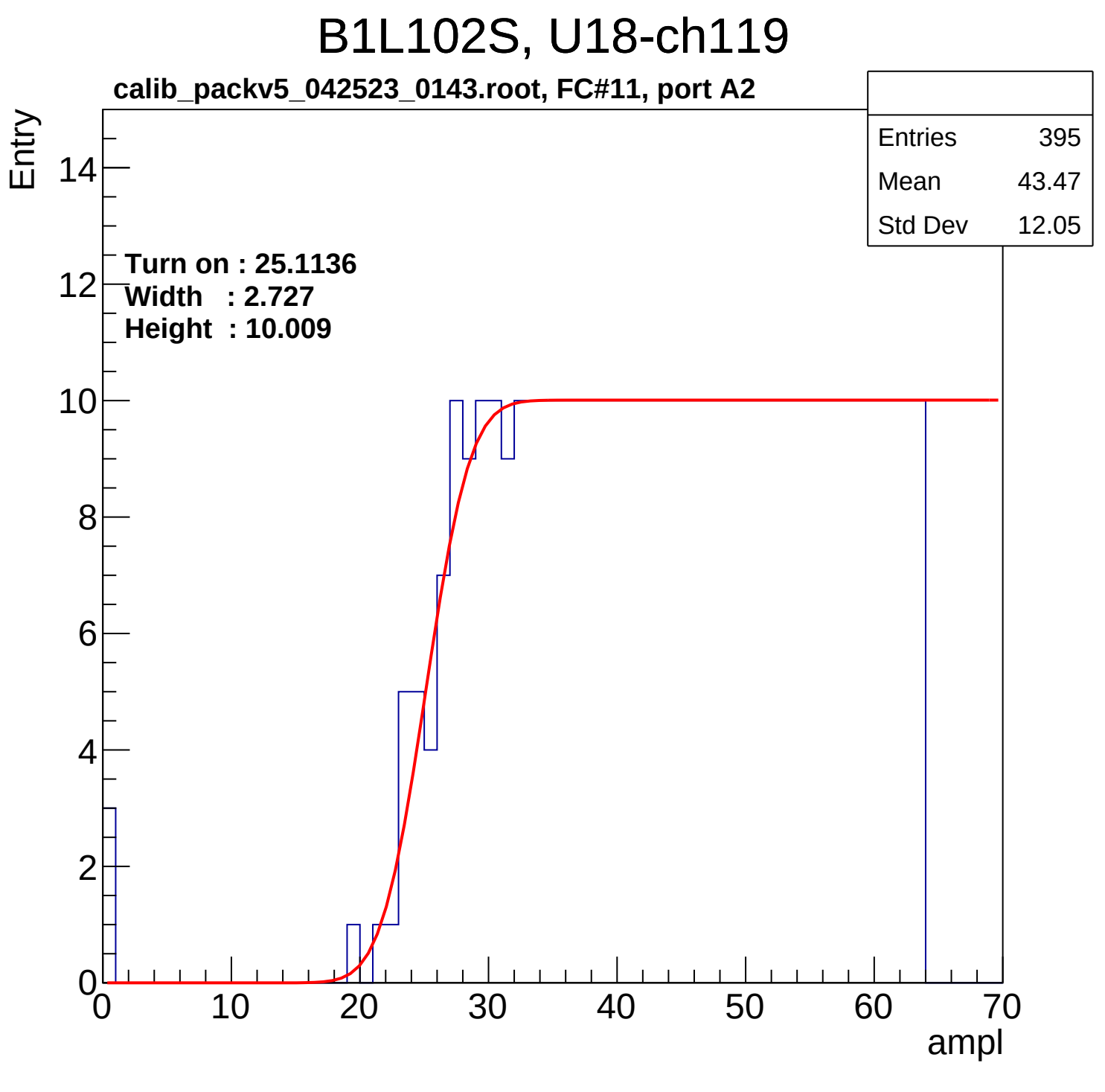
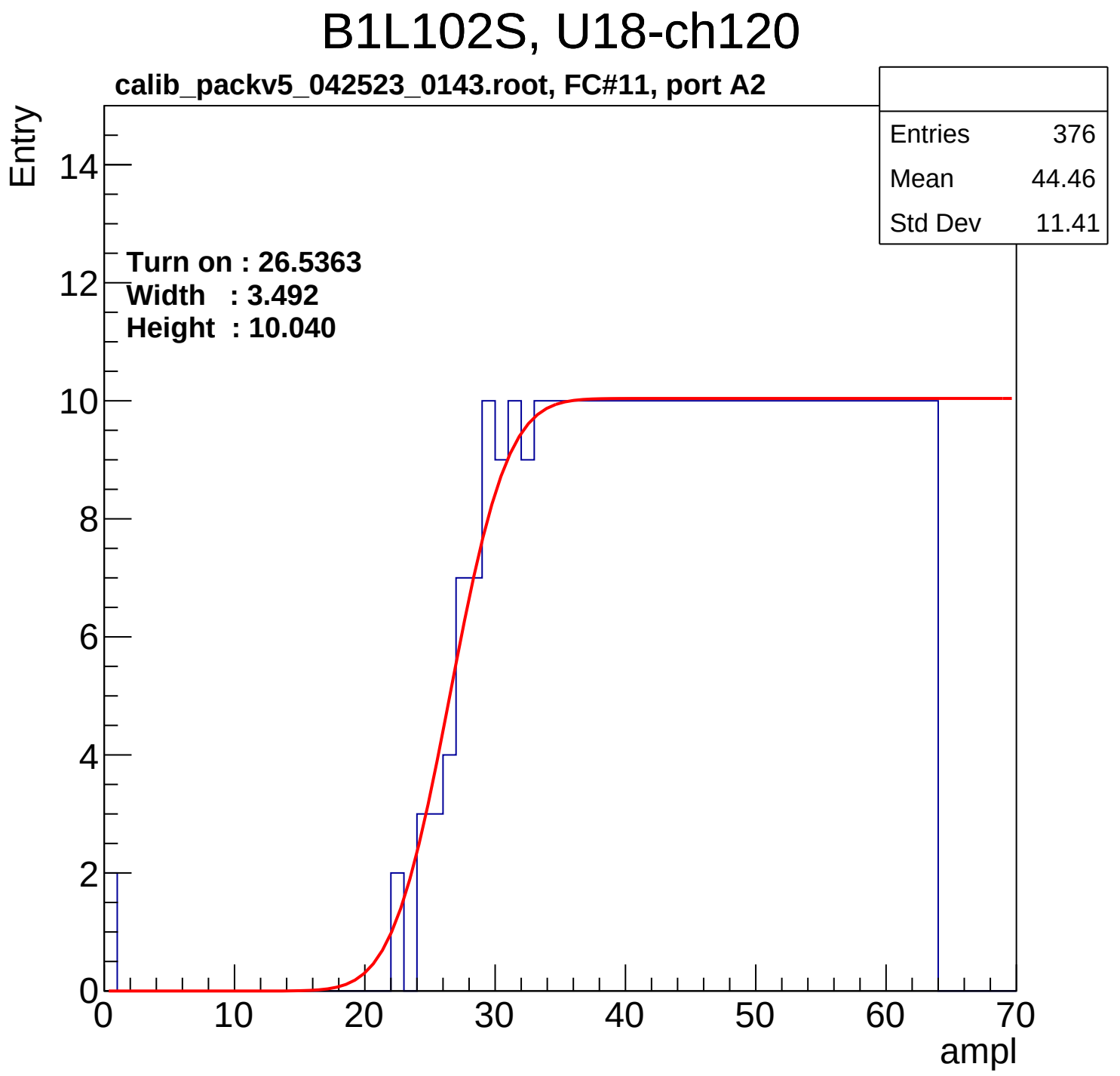

B1L102S, U18-ch119
calib_packv5_042523_0143.root, FC#11, port A2
Entries 395
Mean 43.47
Std Dev 12.05
Turn on : 25.1136
Width : 2.727
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U18-ch120
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.46
Std Dev 11.41
Turn on : 26.5363
Width : 3.492
Height : 10.040
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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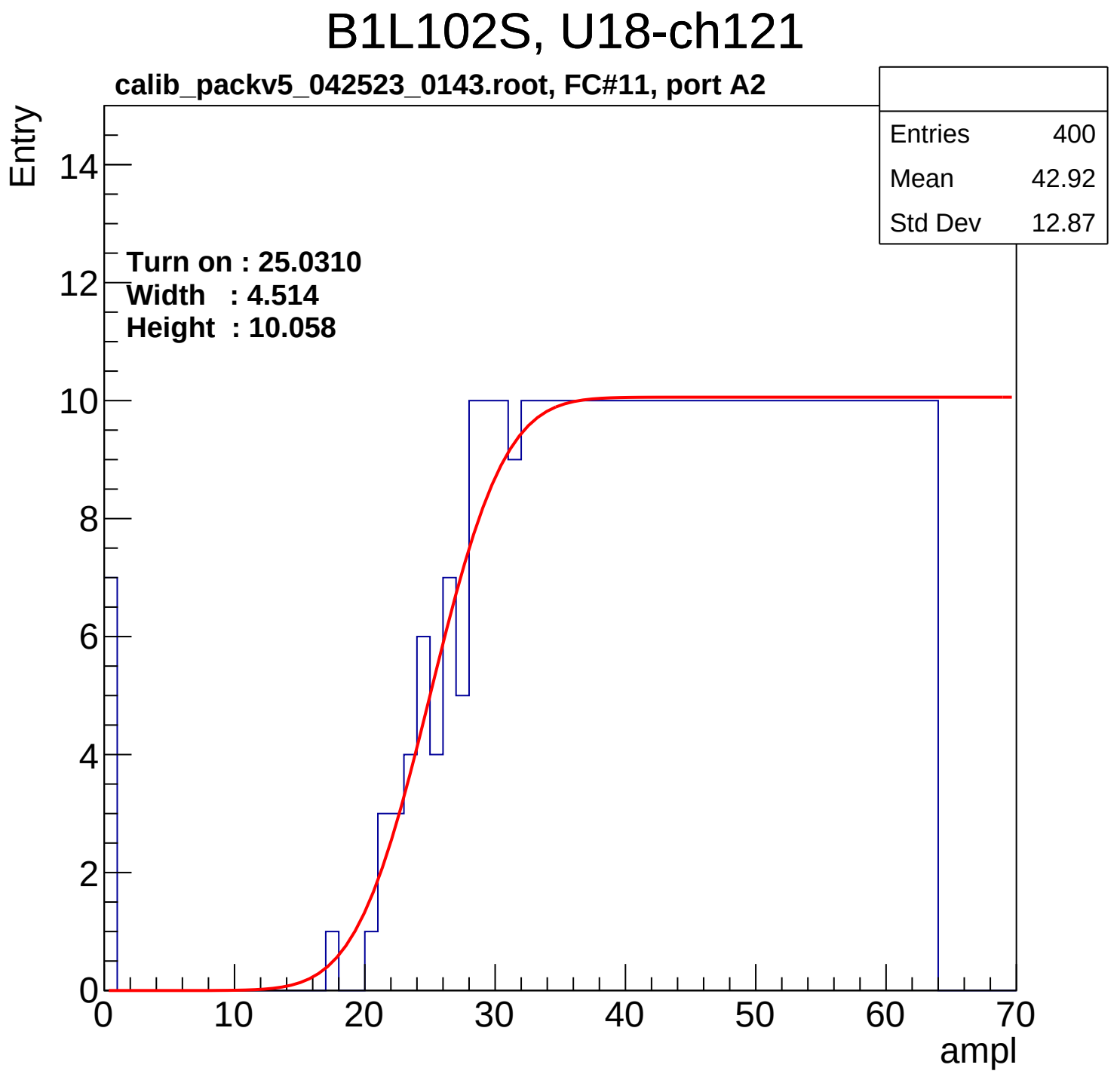
B1L102S, U18-ch121
calib_packv5_042523_0143.root, FC#11, port A2
Entries 400
Mean 42.92
Std Dev 12.87
Turn on : 25.0310
Width : 4.514
Height : 10.058
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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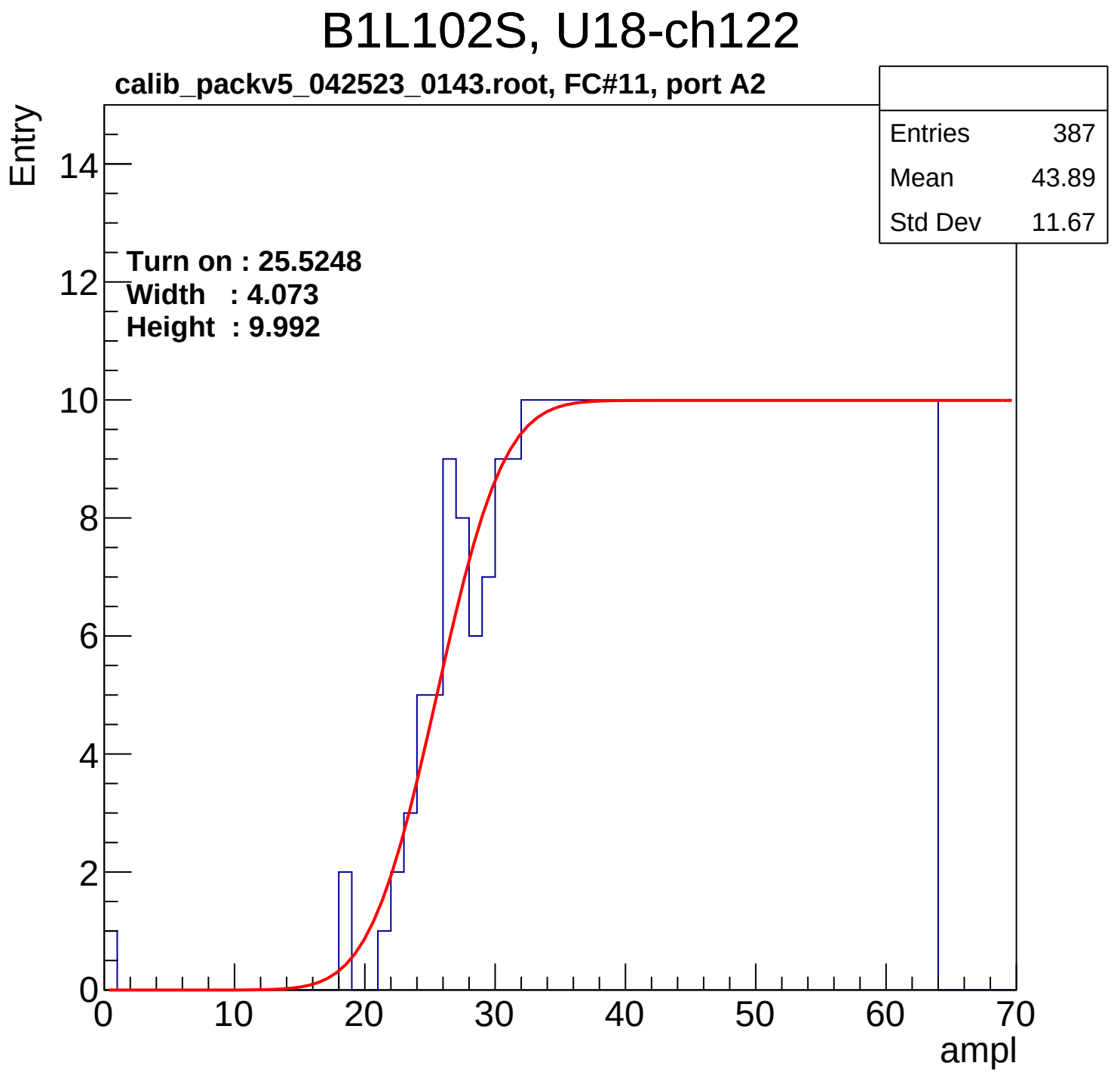
B1L102S, U18-ch122
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.89
Std Dev 11.67
Turn on : 25.5248
Width : 4.073
Height : 9.992
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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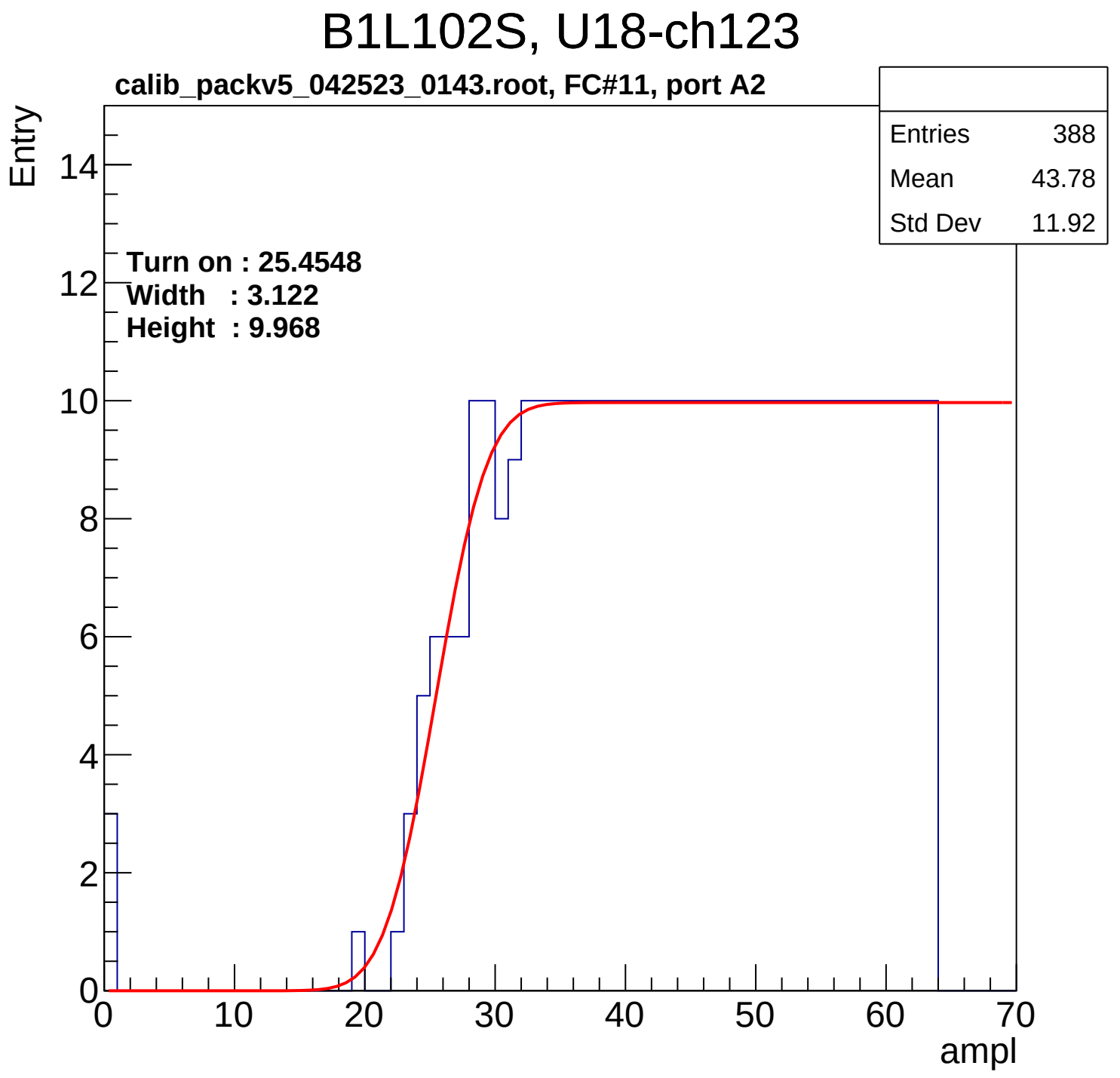
B1L102S, U18-ch123
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.78
Std Dev 11.92
Turn on : 25.4548
Width : 3.122
Height : 9.968
Entry
ampl
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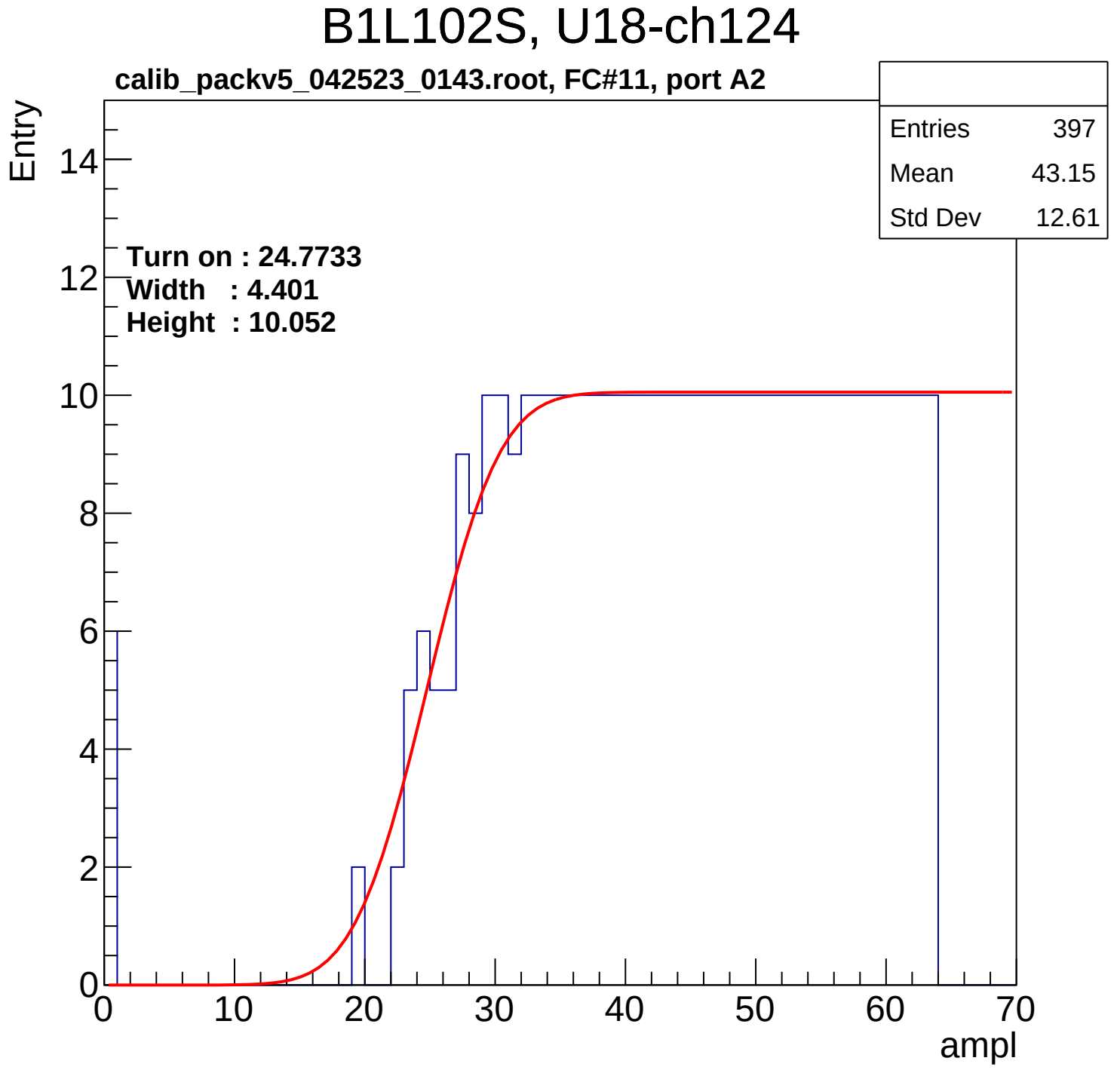
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U18-ch124
calib_packv5_042523_0143.root, FC#11, port A2
Entries 397
Mean 43.15
Std Dev 12.61
Turn on : 24.7733
Width : 4.401
Height : 10.052
Entry
ampl
0
2
4
6
8
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12
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20
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40
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60
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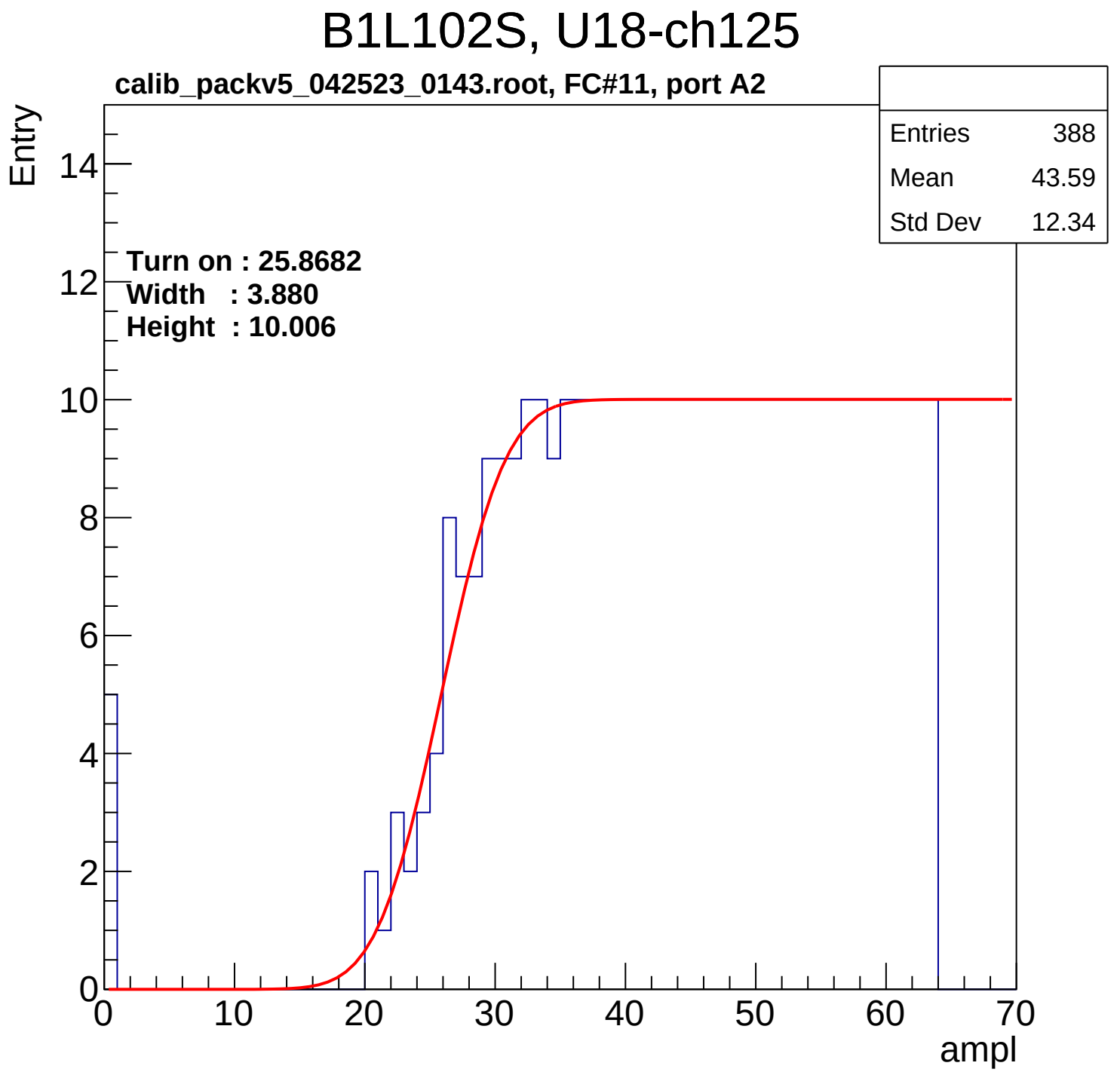
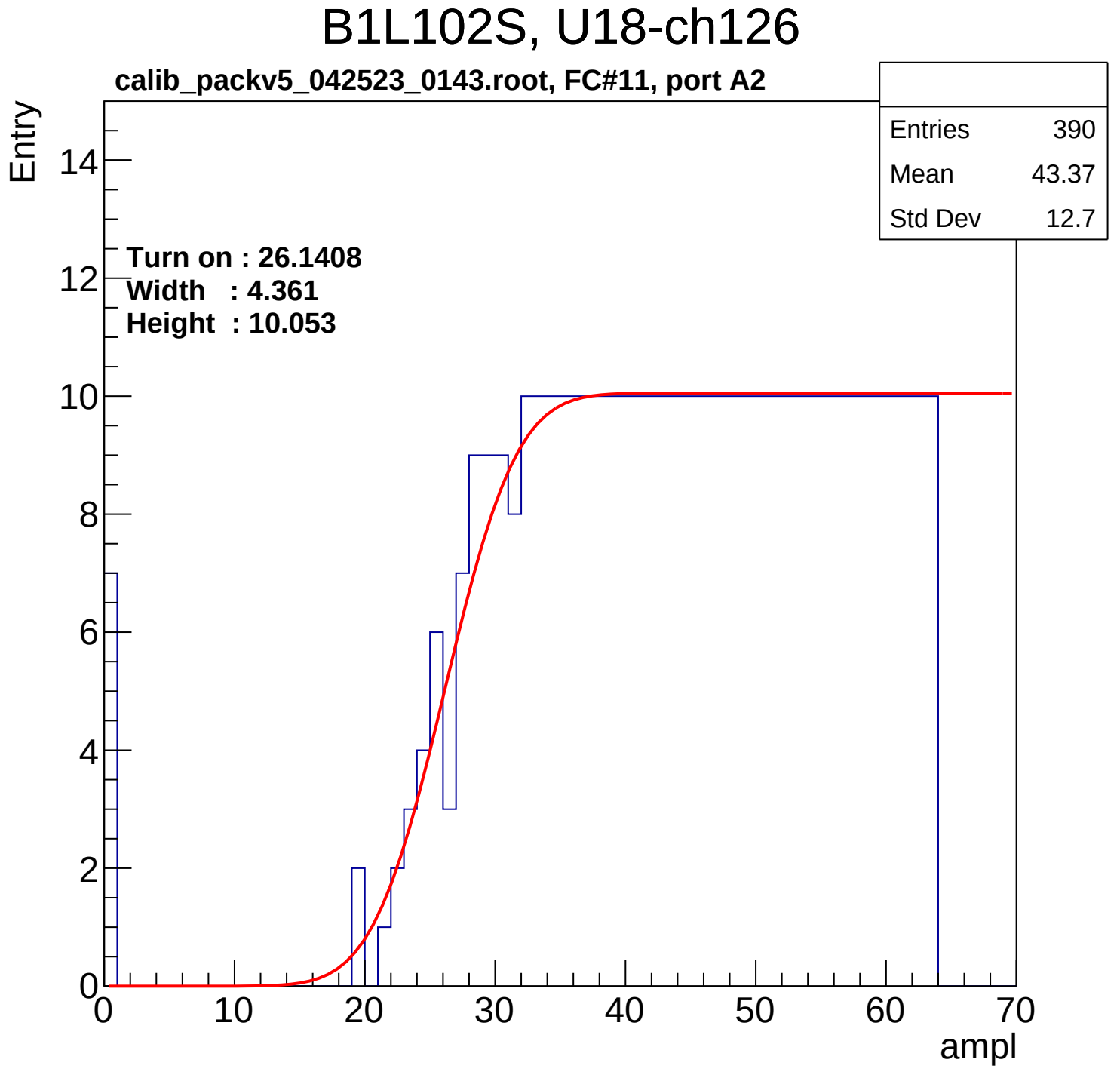

B1L102S, U18-ch125
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.59
Std Dev 12.34
Turn on : 25.8682
Width : 3.880
Height : 10.006
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U18-ch126
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.37
Std Dev 12.7
Turn on : 26.1408
Width : 4.361
Height : 10.053
Entry
ampl
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2
4
6
8
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0
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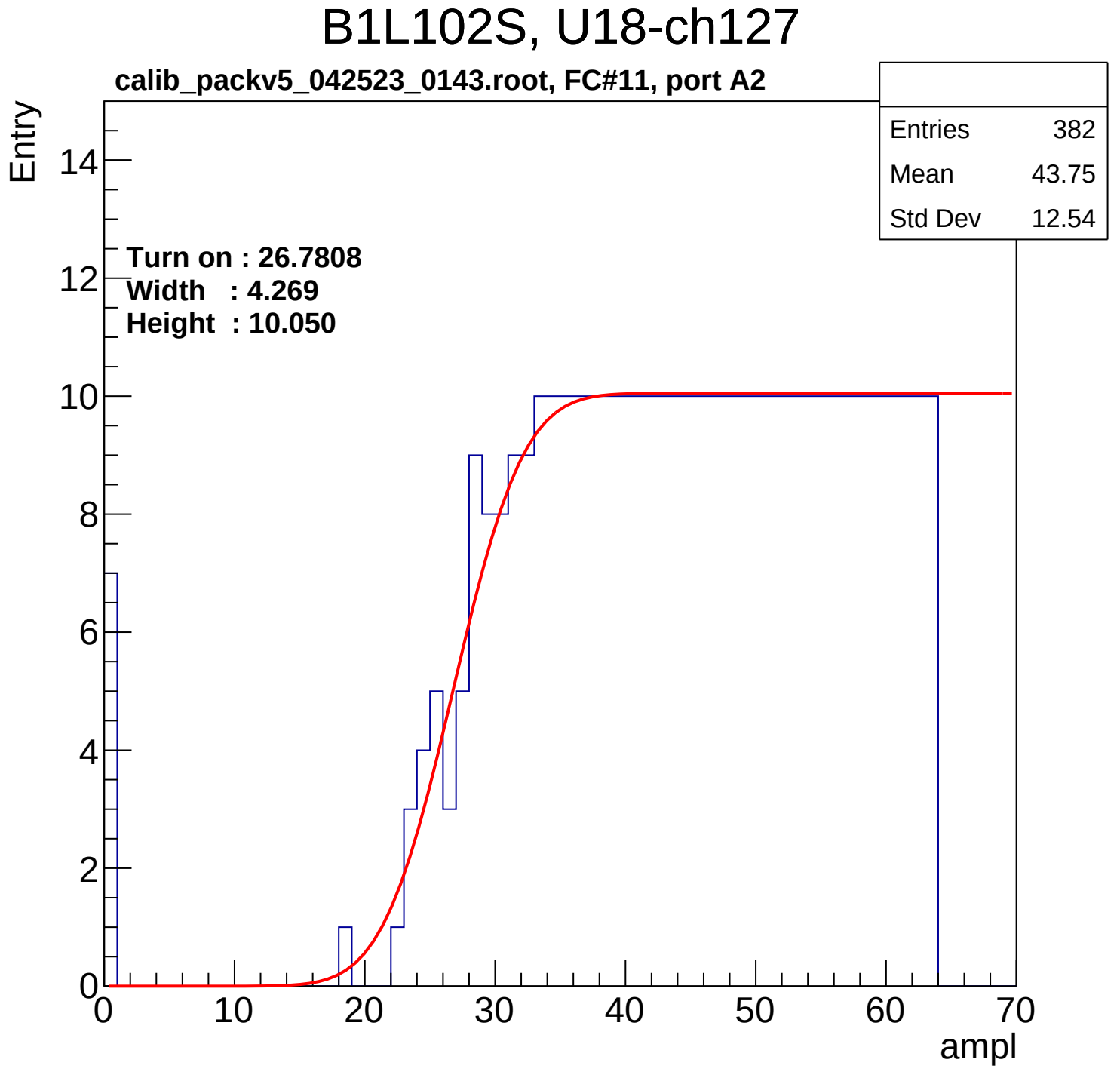
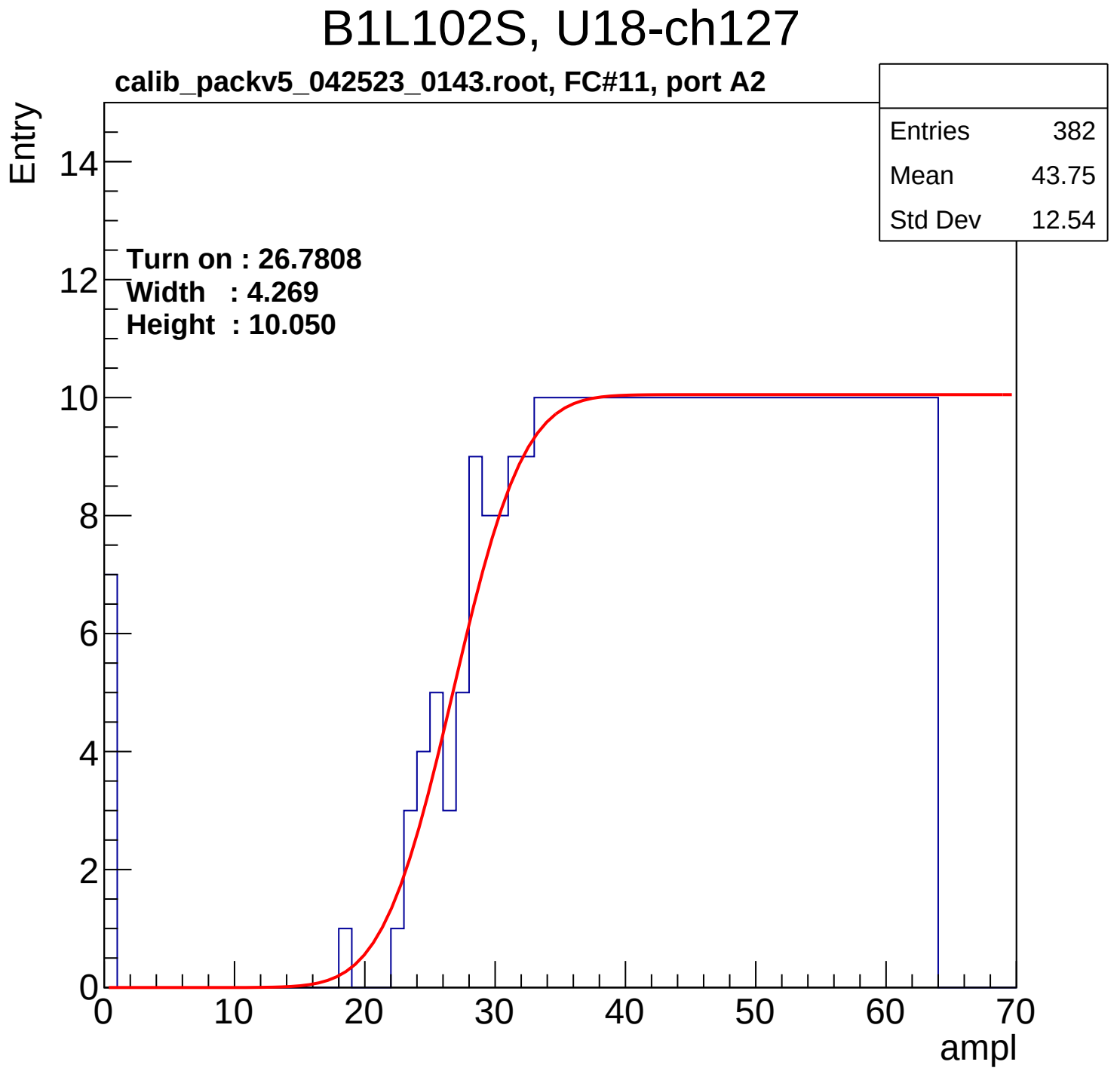

B1L102S, U18-ch127
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 43.75
Std Dev 12.54
Turn on : 26.7808
Width : 4.269
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U18-ch127
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 43.75
Std Dev 12.54
Turn on : 26.7808
Width : 4.269
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70