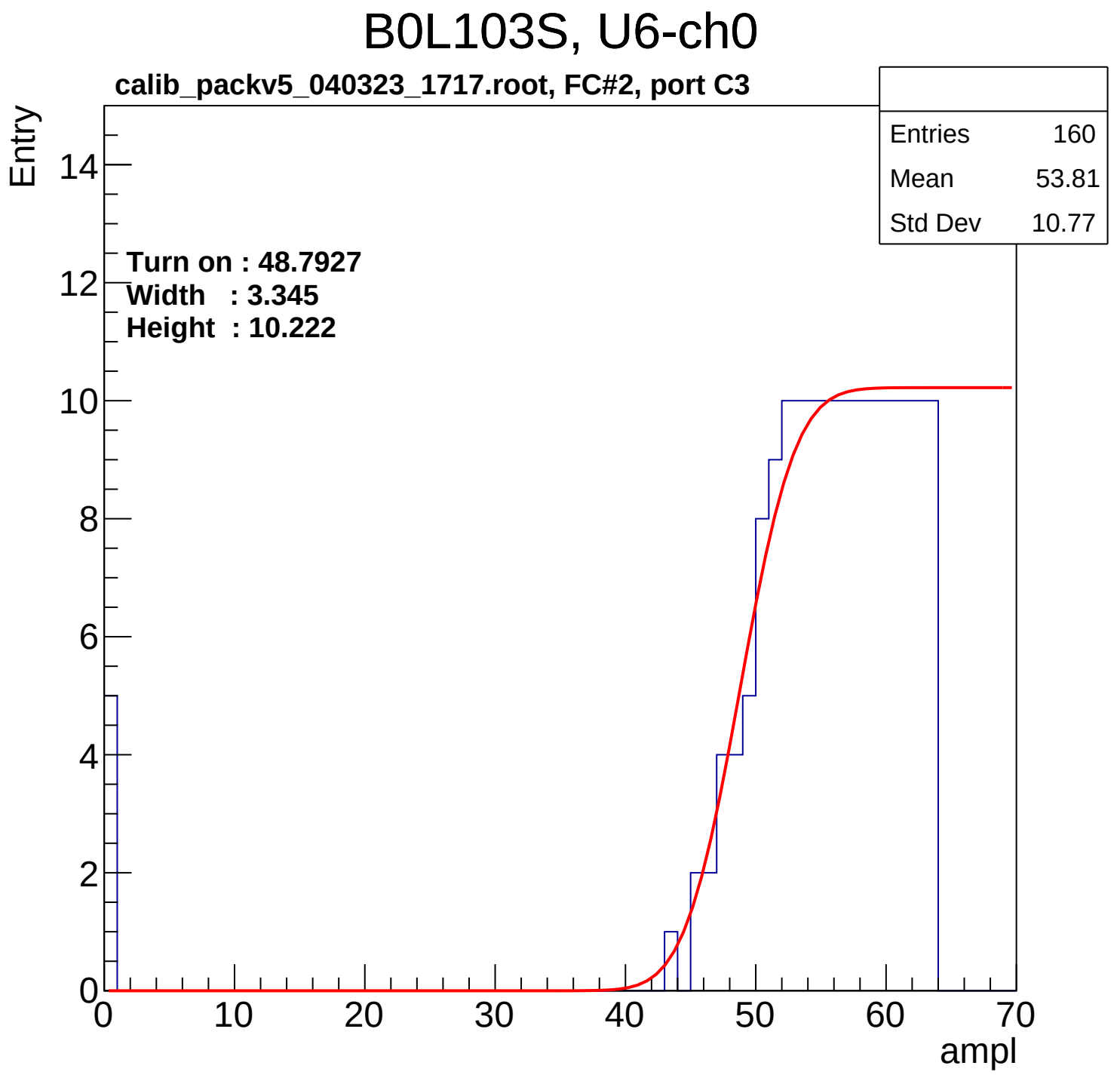
B0L103S, U6-ch0
calib_packv5_040323_1717.root, FC#2, port C3
Entries 160
Mean 53.81
Std Dev 10.77
Turn on : 48.7927
Width : 3.345
Height : 10.222
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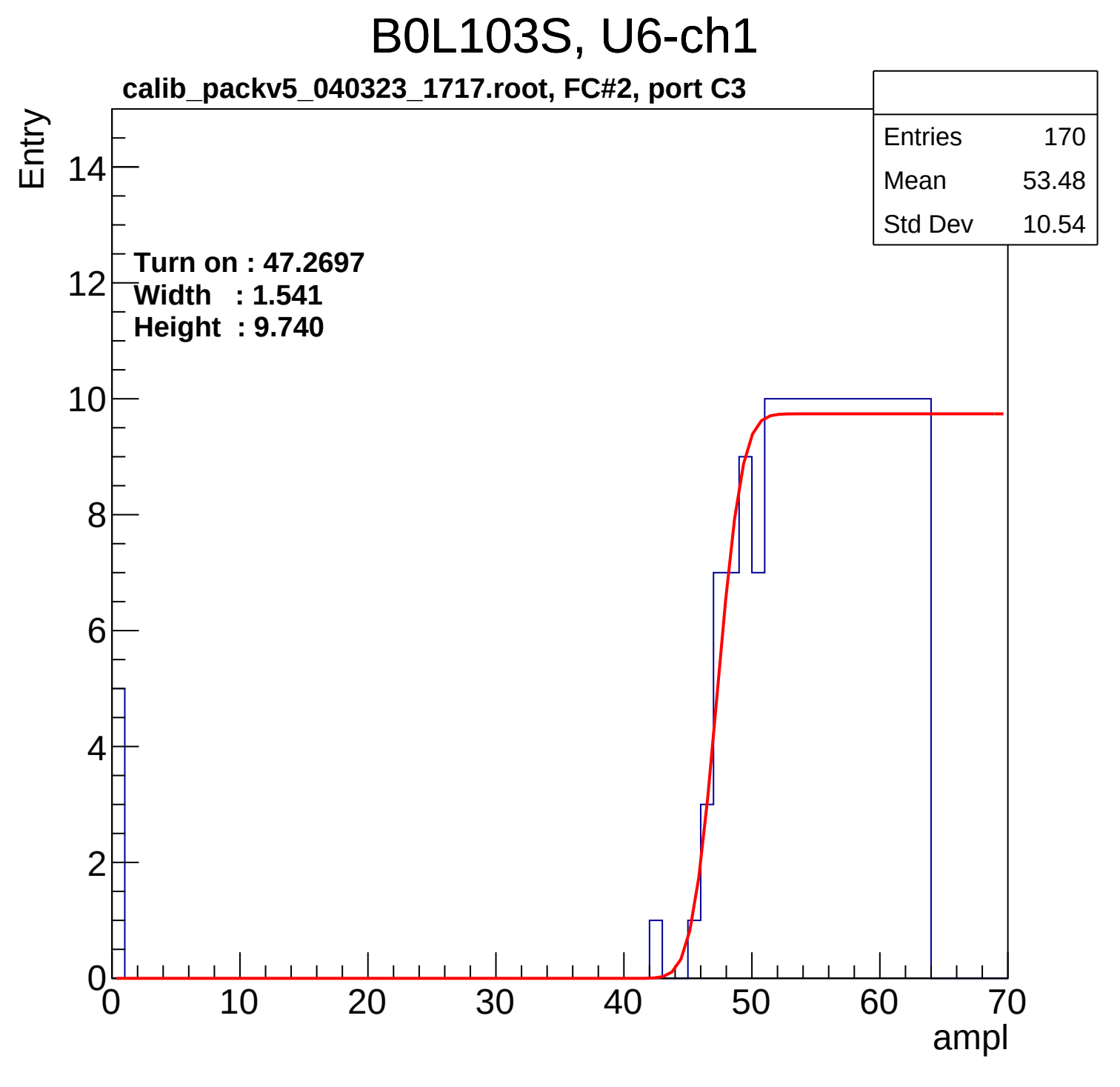
B0L103S, U6-ch1
calib_packv5_040323_1717.root, FC#2, port C3
Entries 170
Mean 53.48
Std Dev 10.54
Turn on : 47.2697
Width : 1.541
Height : 9.740
Entry
ampl
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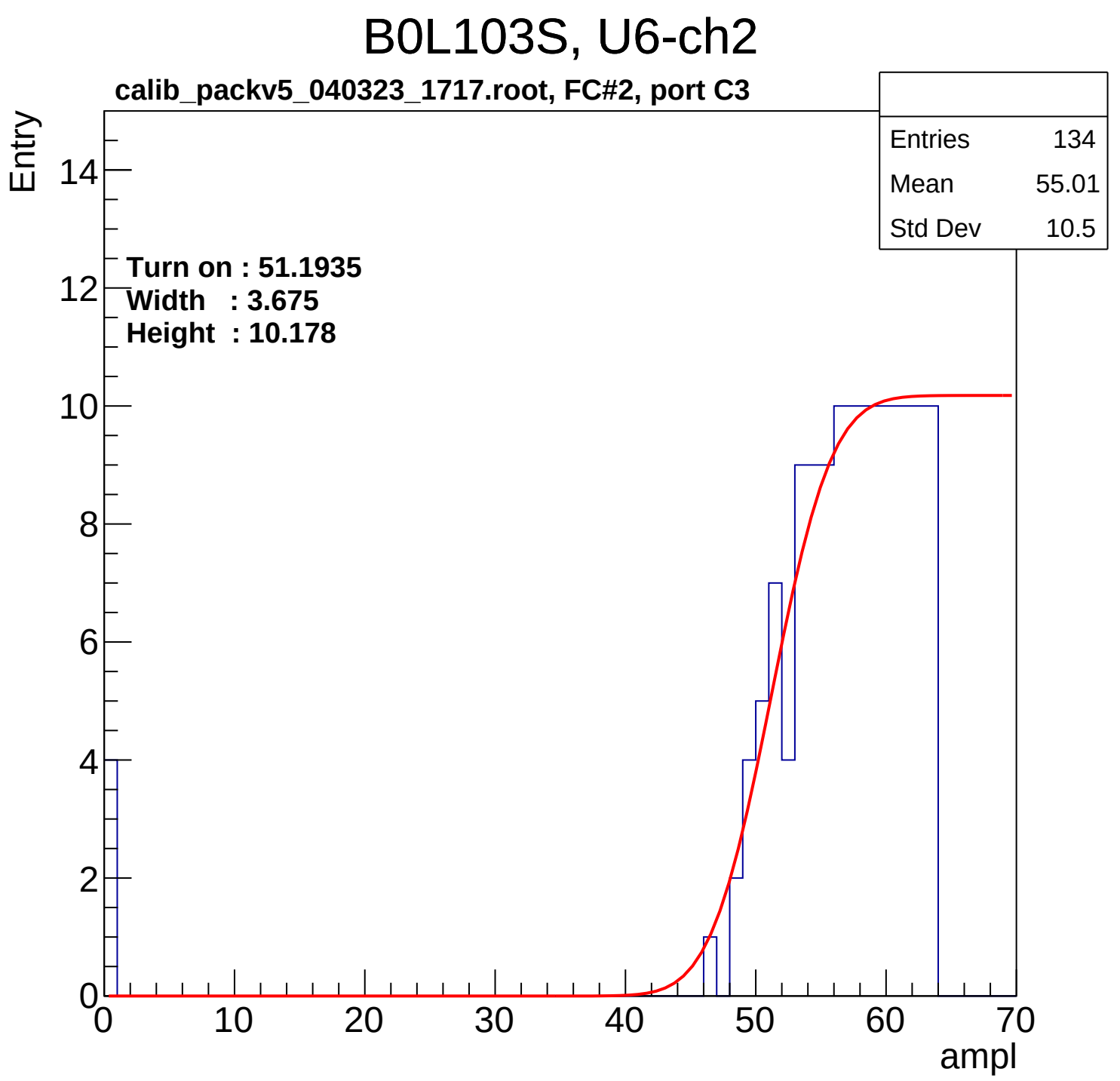
B0L103S, U6-ch2
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 55.01
Std Dev 10.5
Turn on : 51.1935
Width : 3.675
Height : 10.178
Entry
ampl
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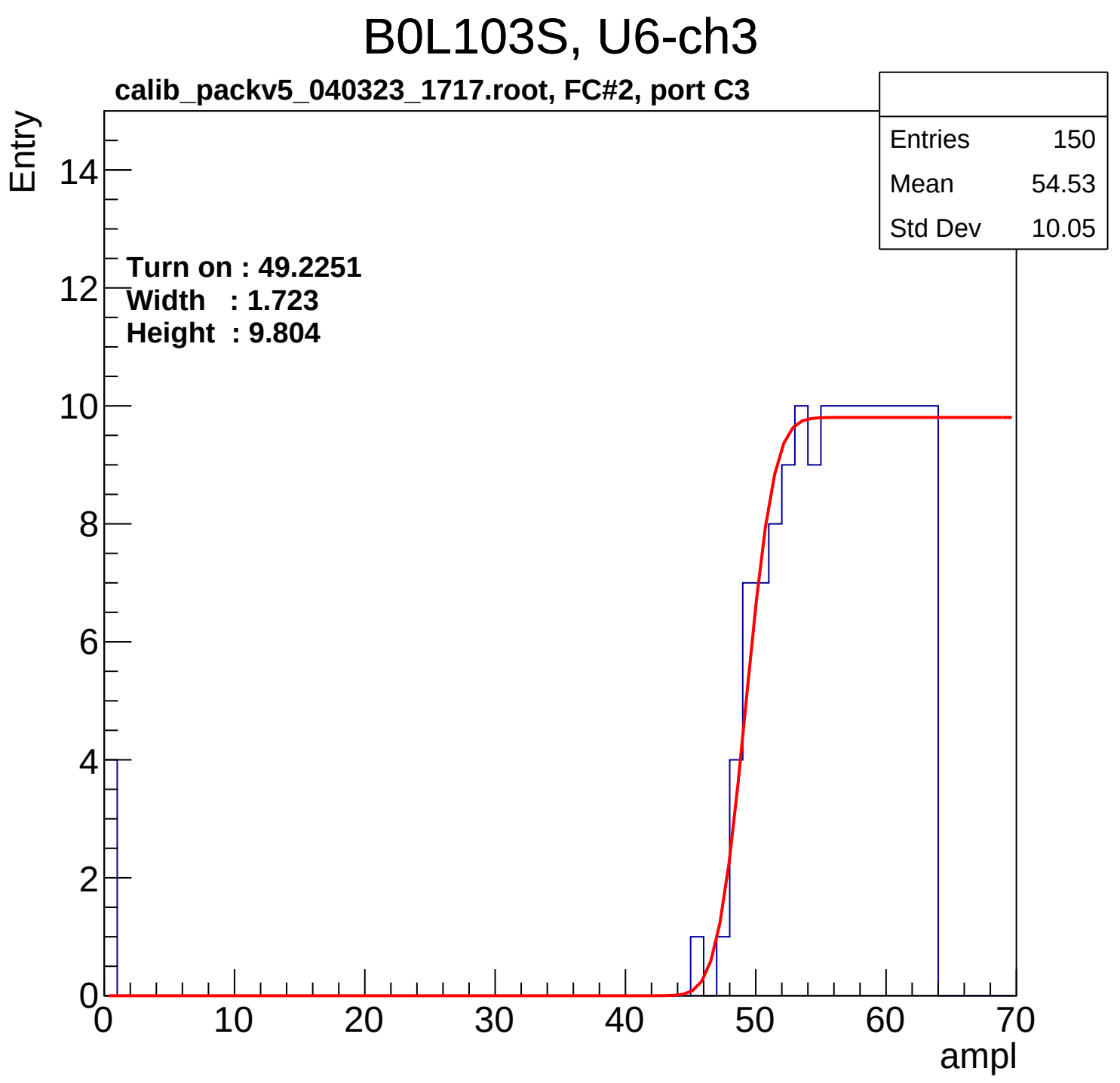
B0L103S, U6-ch3
calib_packv5_040323_1717.root, FC#2, port C3
Entries 150
Mean 54.53
Std Dev 10.05
Turn on : 49.2251
Width : 1.723
Height : 9.804
Entry
ampl
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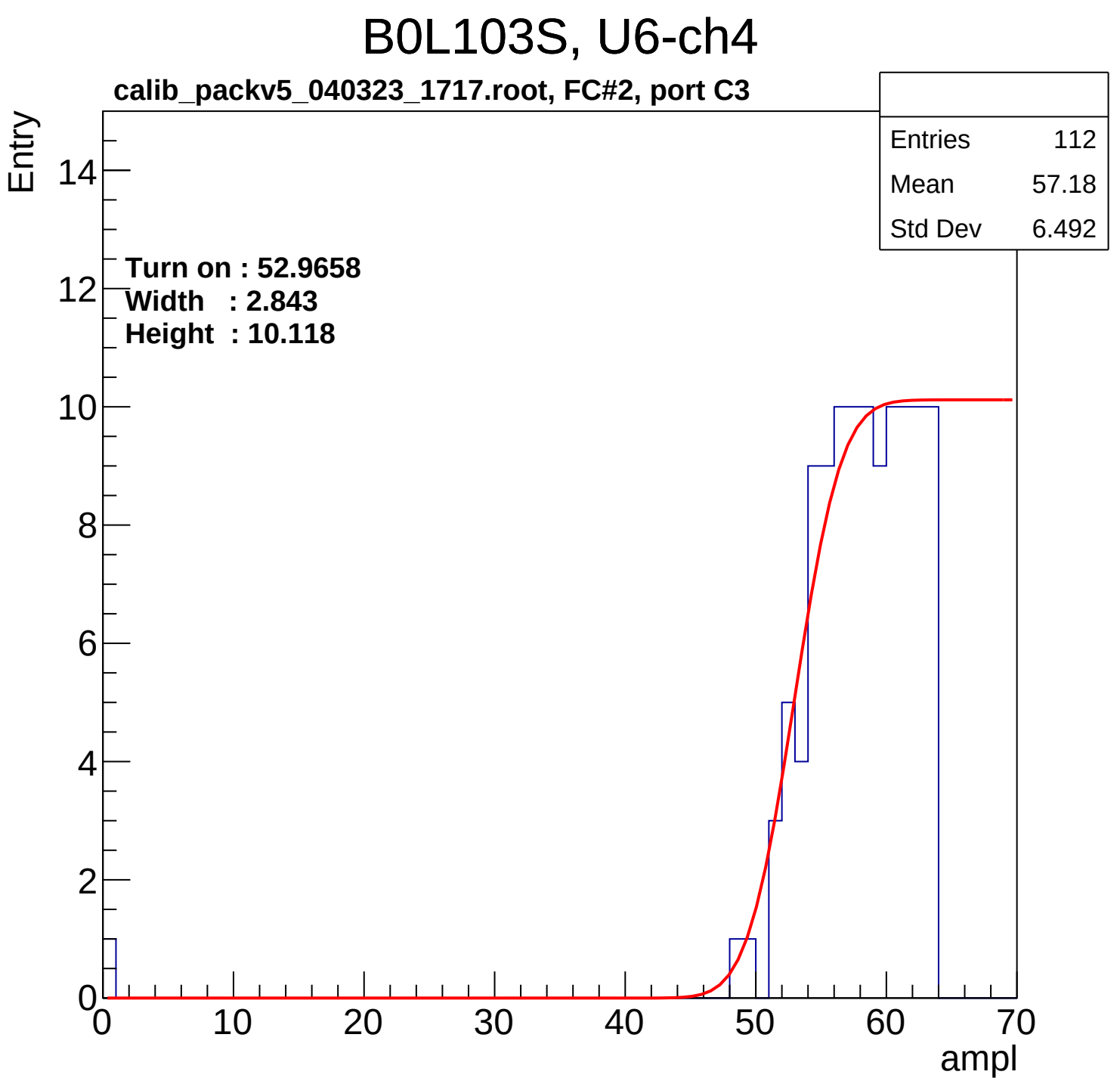
B0L103S, U6-ch4
calib_packv5_040323_1717.root, FC#2, port C3
Entries 112
Mean 57.18
Std Dev 6.492
Turn on : 52.9658
Width : 2.843
Height : 10.118
Entry
ampl
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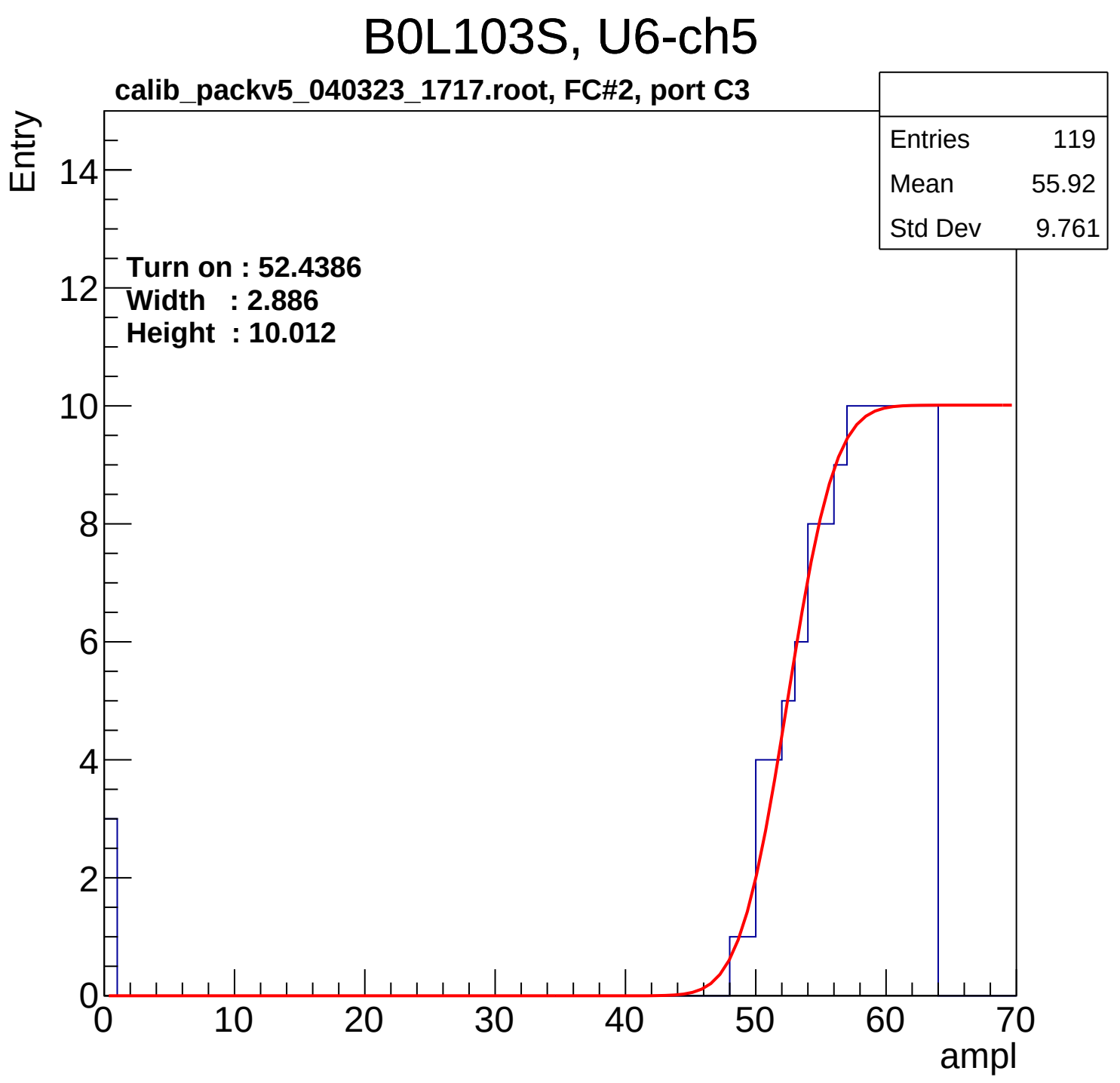
B0L103S, U6-ch5
calib_packv5_040323_1717.root, FC#2, port C3
Entries 119
Mean 55.92
Std Dev 9.761
Turn on : 52.4386
Width : 2.886
Height : 10.012
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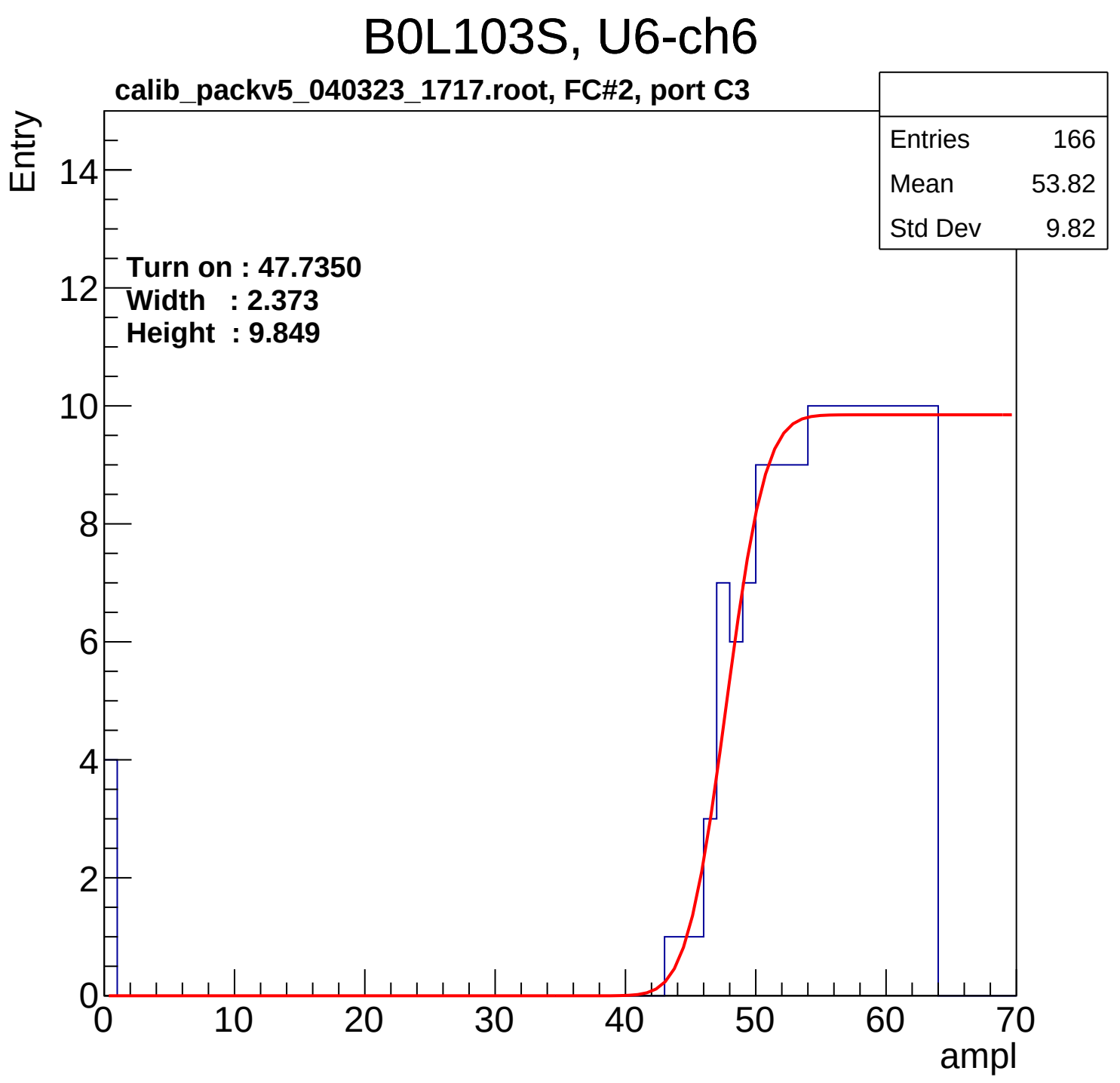
B0L103S, U6-ch6
calib_packv5_040323_1717.root, FC#2, port C3
Entries 166
Mean 53.82
Std Dev 9.82
Turn on : 47.7350
Width : 2.373
Height : 9.849
Entry
ampl
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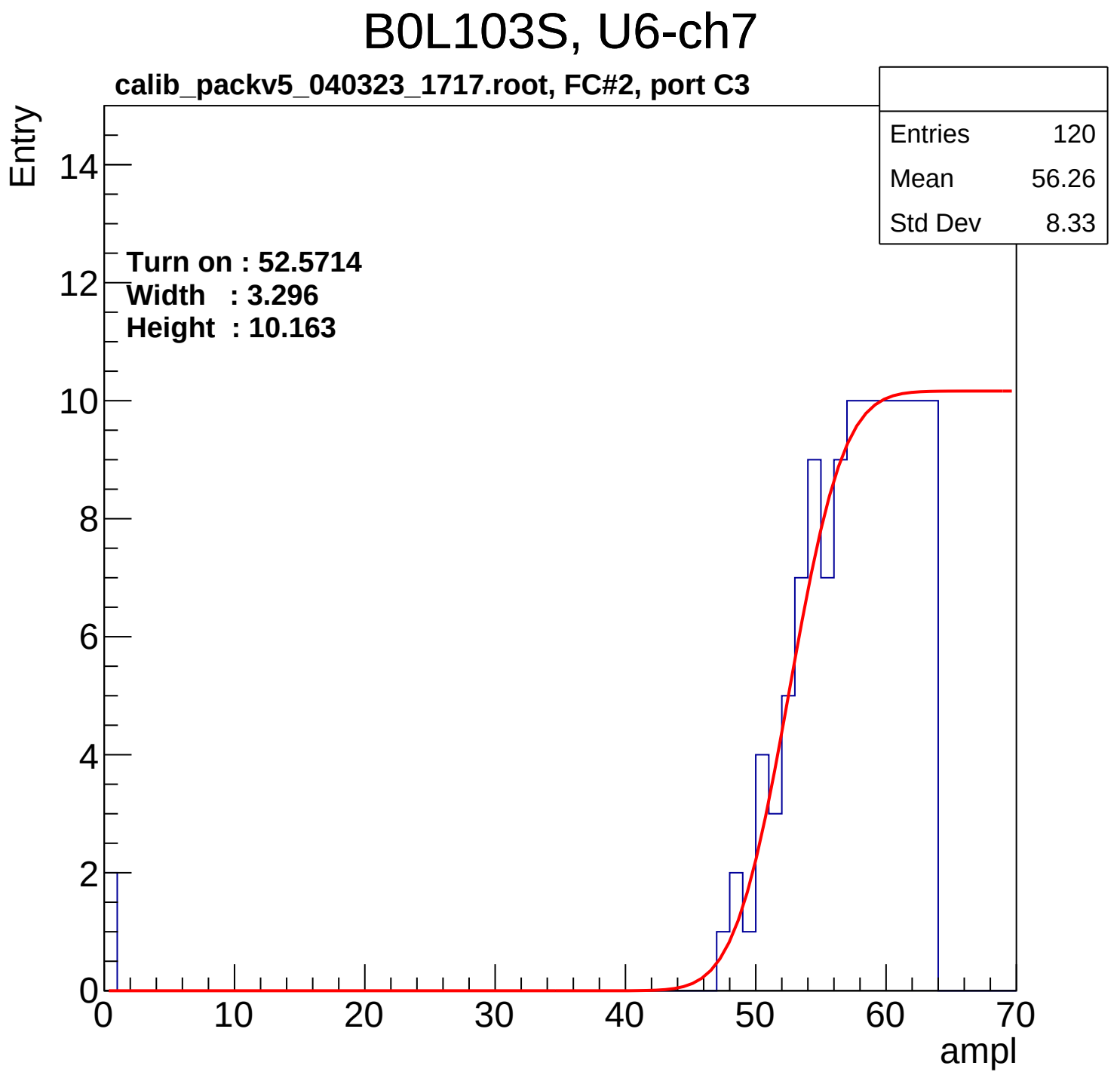
B0L103S, U6-ch7
calib_packv5_040323_1717.root, FC#2, port C3
Entries 120
Mean 56.26
Std Dev 8.33
Turn on : 52.5714
Width : 3.296
Height : 10.163
Entry
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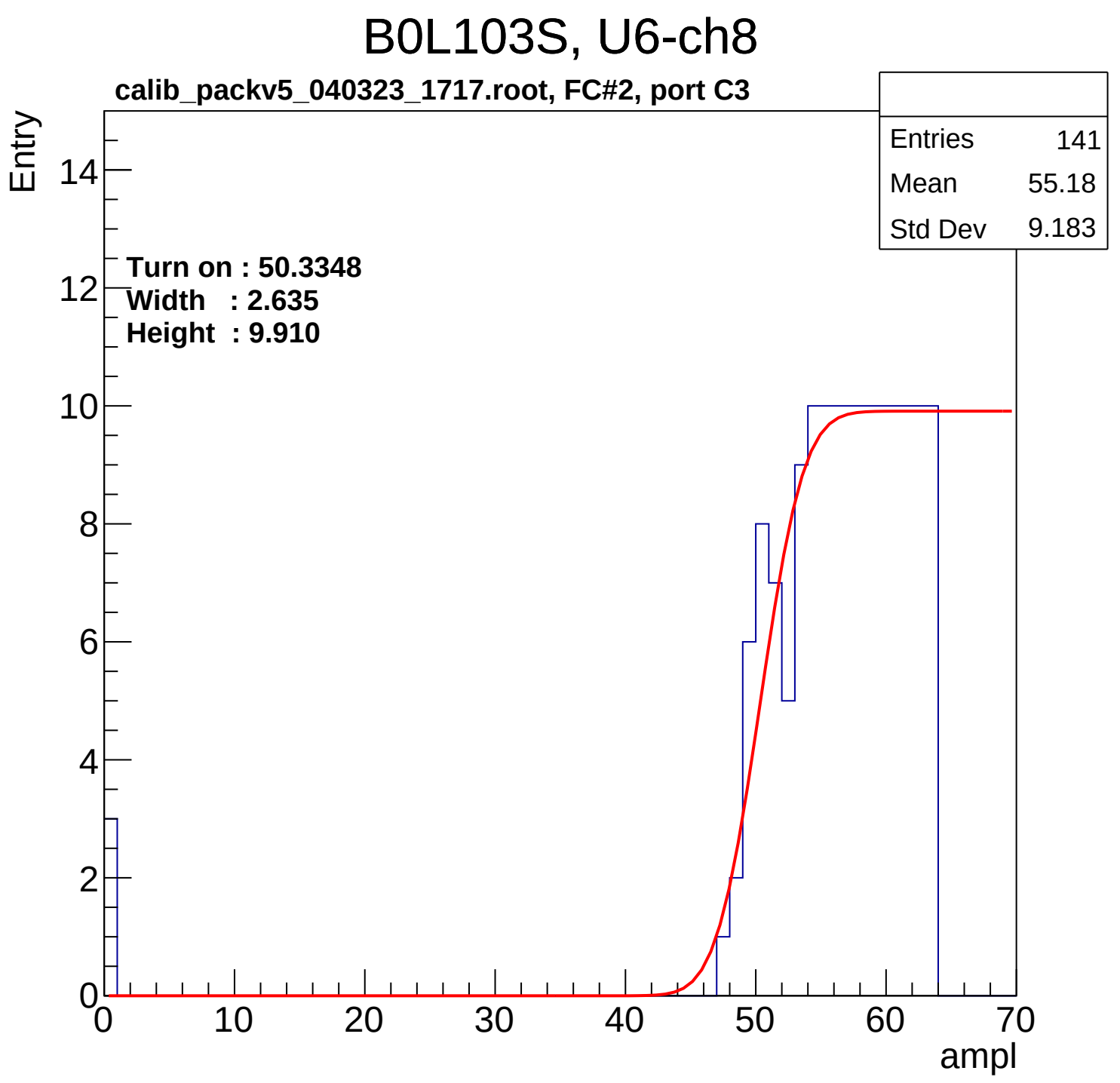
B0L103S, U6-ch8
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 55.18
Std Dev 9.183
Turn on : 50.3348
Width : 2.635
Height : 9.910
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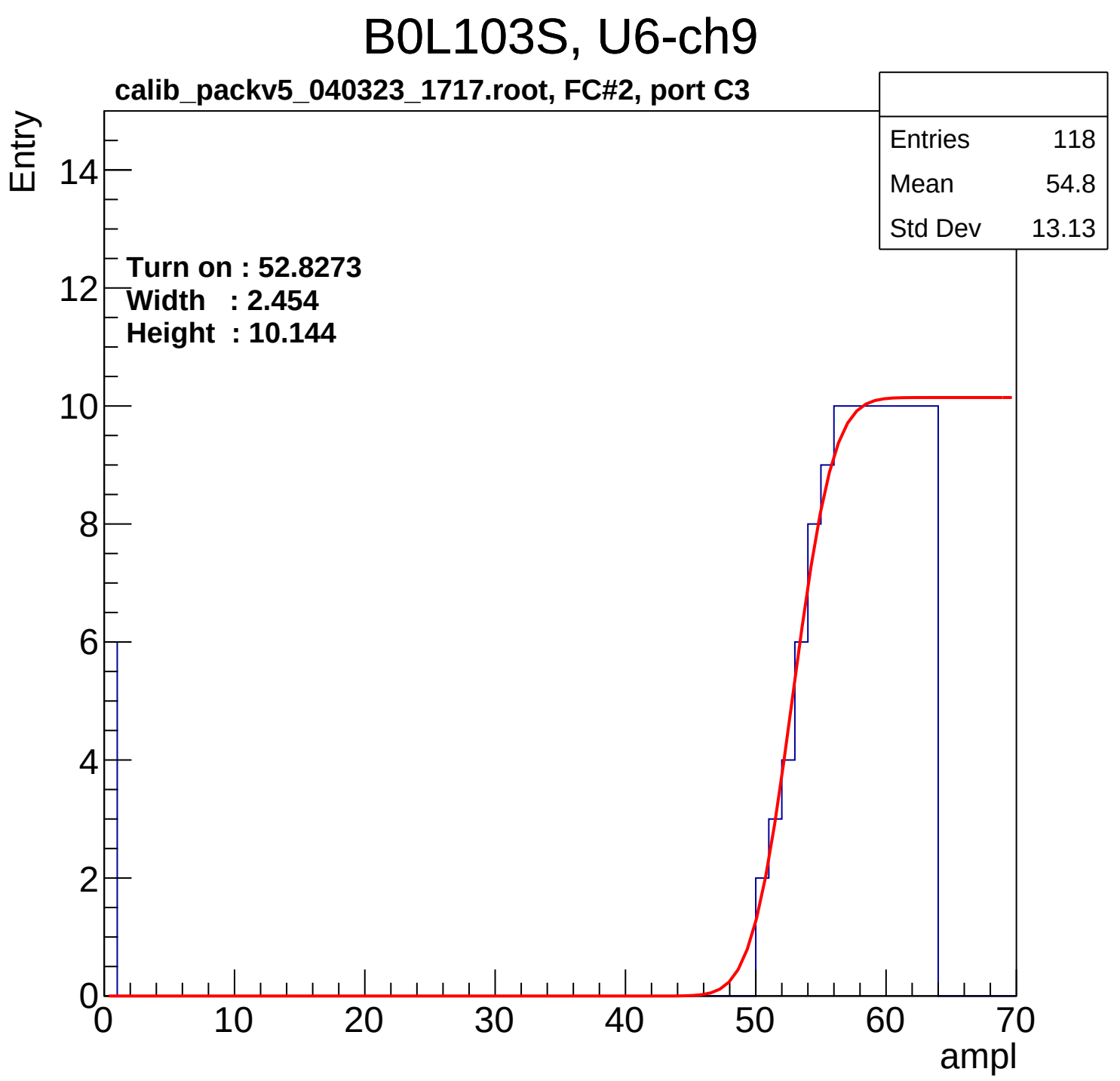
B0L103S, U6-ch9
calib_packv5_040323_1717.root, FC#2, port C3
Entries 118
Mean 54.8
Std Dev 13.13
Turn on : 52.8273
Width : 2.454
Height : 10.144
Entry
ampl
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8
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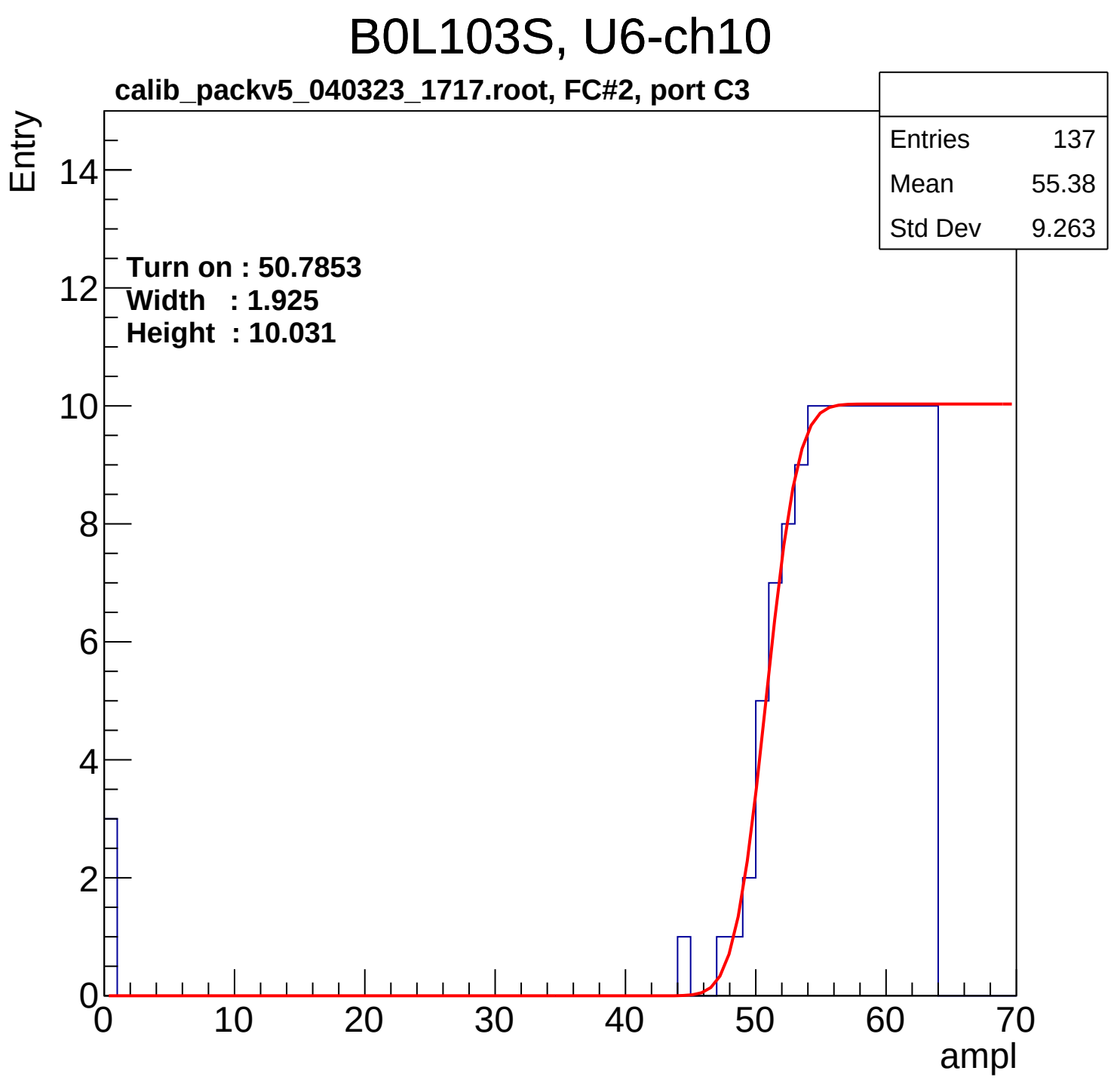
B0L103S, U6-ch10
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 55.38
Std Dev 9.263
Turn on : 50.7853
Width : 1.925
Height : 10.031
Entry
ampl
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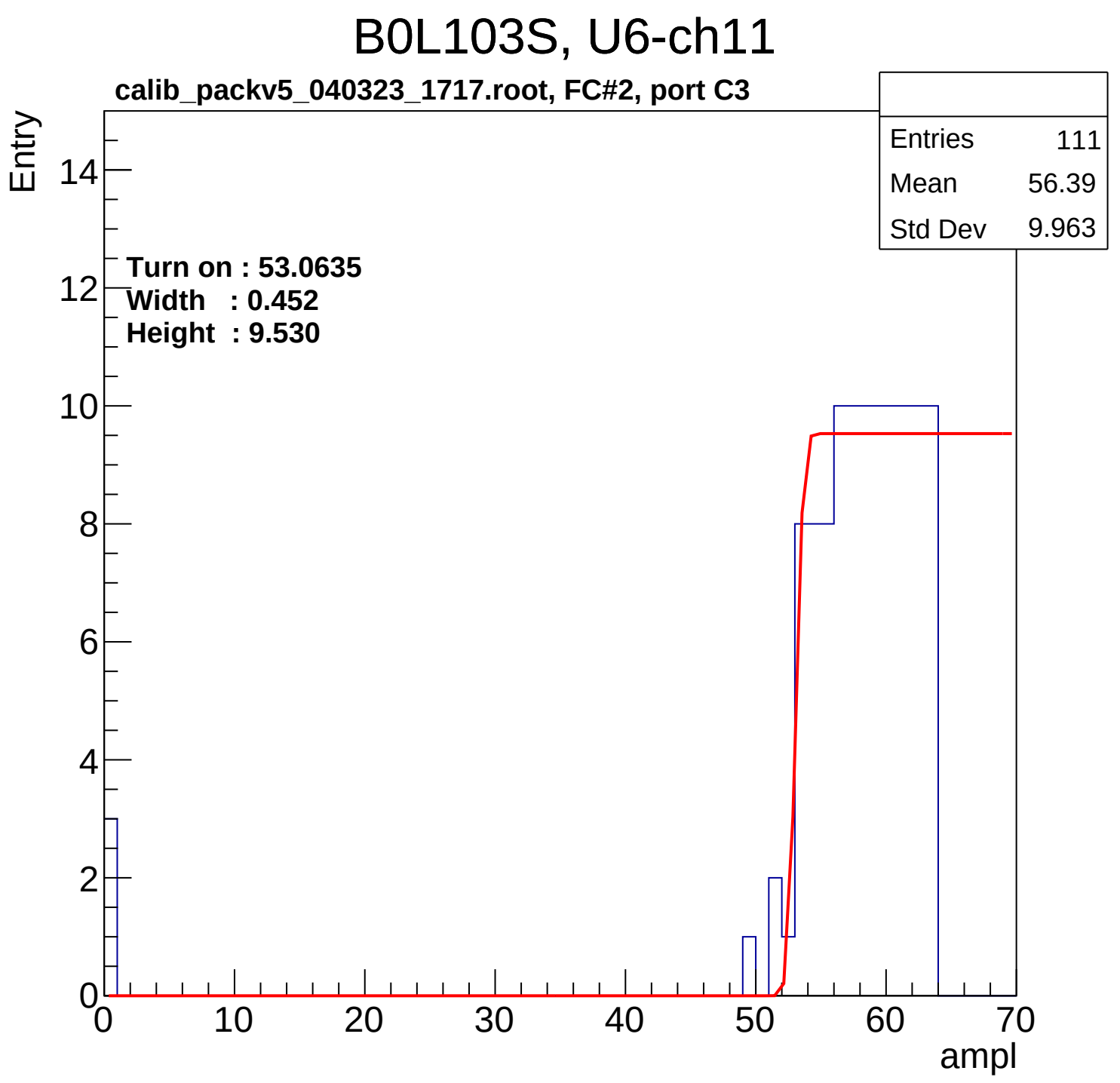
B0L103S, U6-ch11
calib_packv5_040323_1717.root, FC#2, port C3
Entries 111
Mean 56.39
Std Dev 9.963
Turn on : 53.0635
Width : 0.452
Height : 9.530
Entry
ampl
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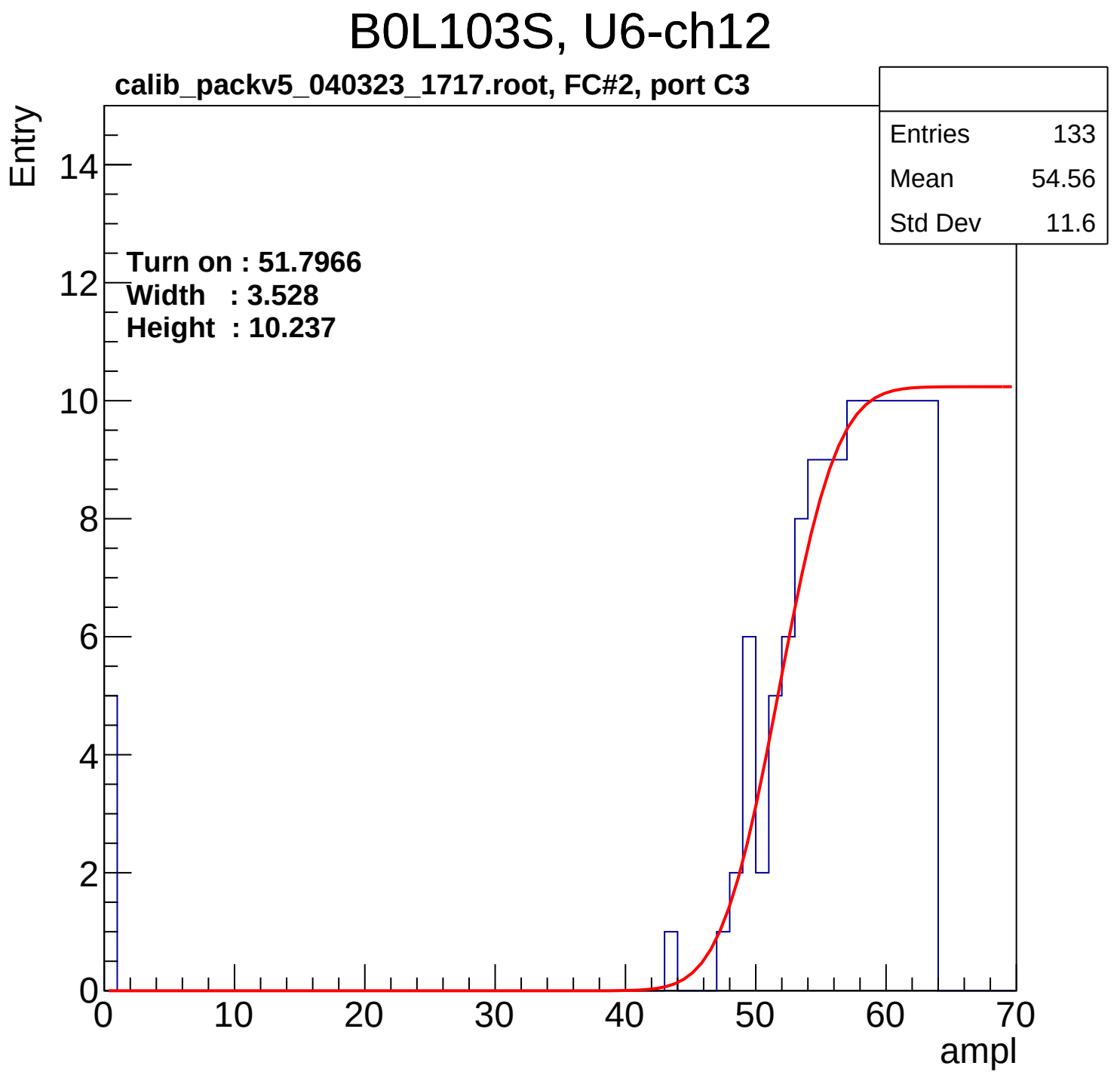
B0L103S, U6-ch12
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 54.56
Std Dev 11.6
Turn on : 51.7966
Width : 3.528
Height : 10.237
Entry
ampl
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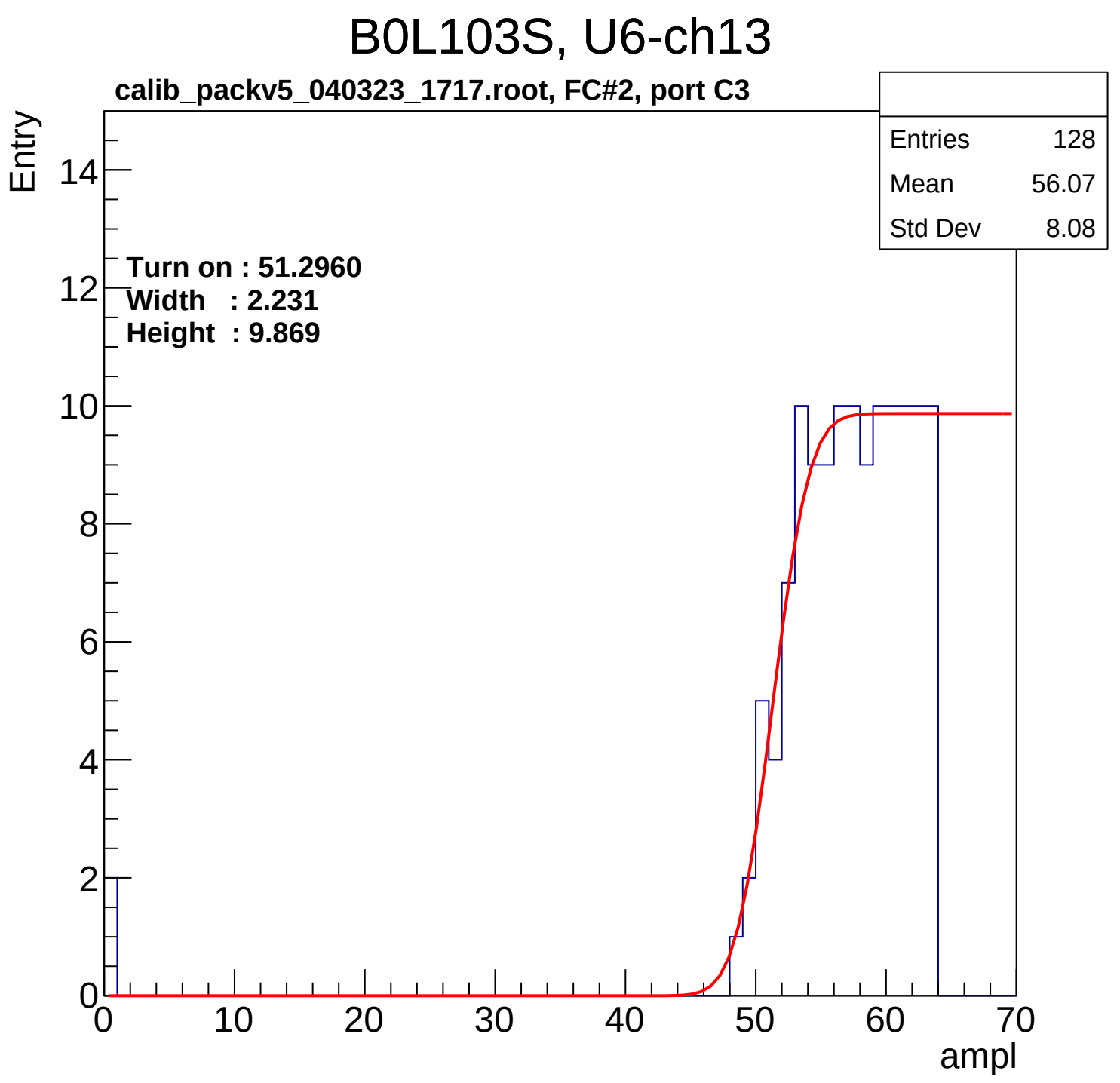
B0L103S, U6-ch13
calib_packv5_040323_1717.root, FC#2, port C3
Entries 128
Mean 56.07
Std Dev 8.08
Turn on : 51.2960
Width : 2.231
Height : 9.869
Entry
ampl
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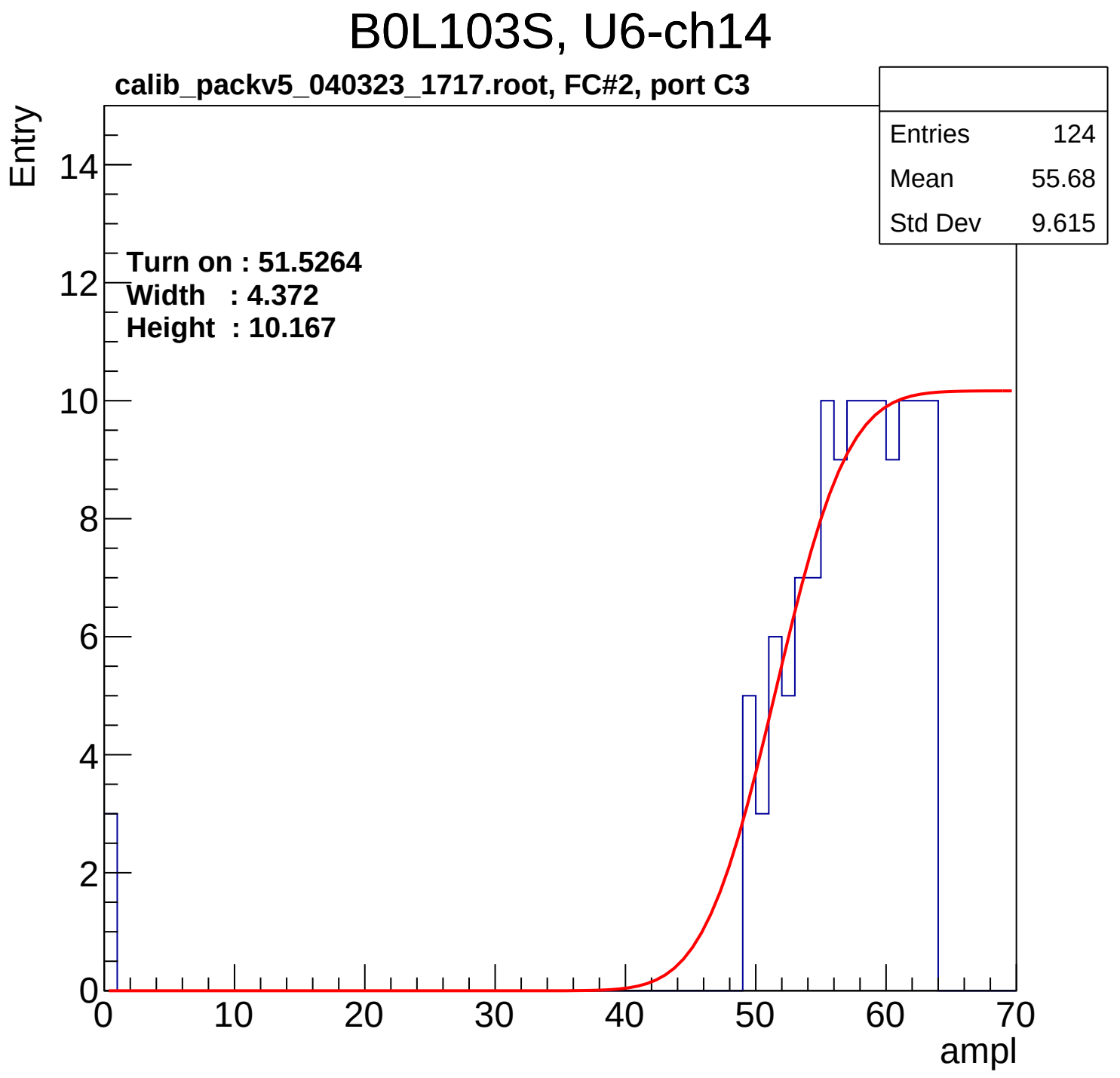
B0L103S, U6-ch14
calib_packv5_040323_1717.root, FC#2, port C3
Entries 124
Mean 55.68
Std Dev 9.615
Turn on : 51.5264
Width : 4.372
Height : 10.167
Entry
ampl
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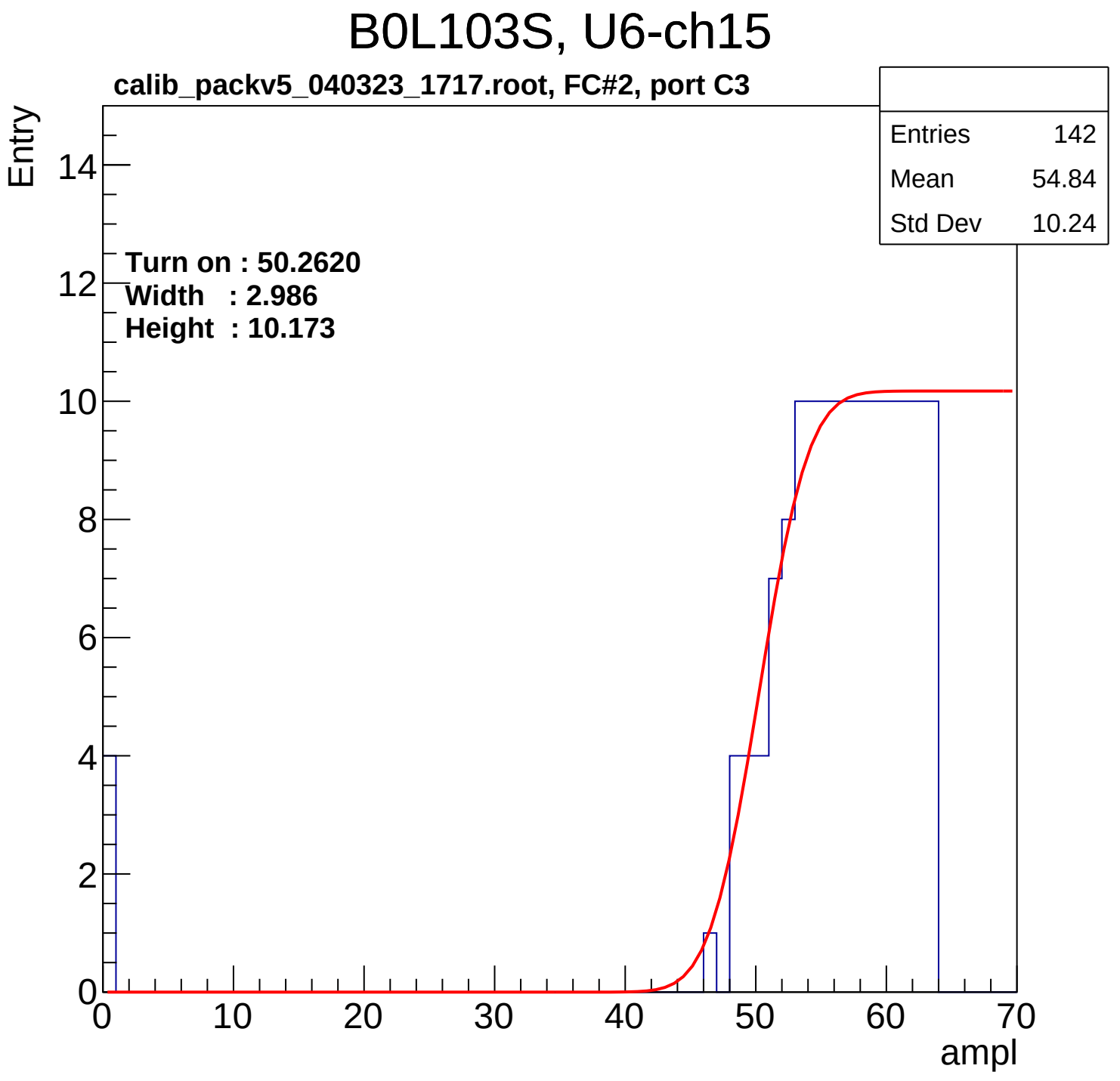
B0L103S, U6-ch15
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 54.84
Std Dev 10.24
Turn on : 50.2620
Width : 2.986
Height : 10.173
Entry
ampl
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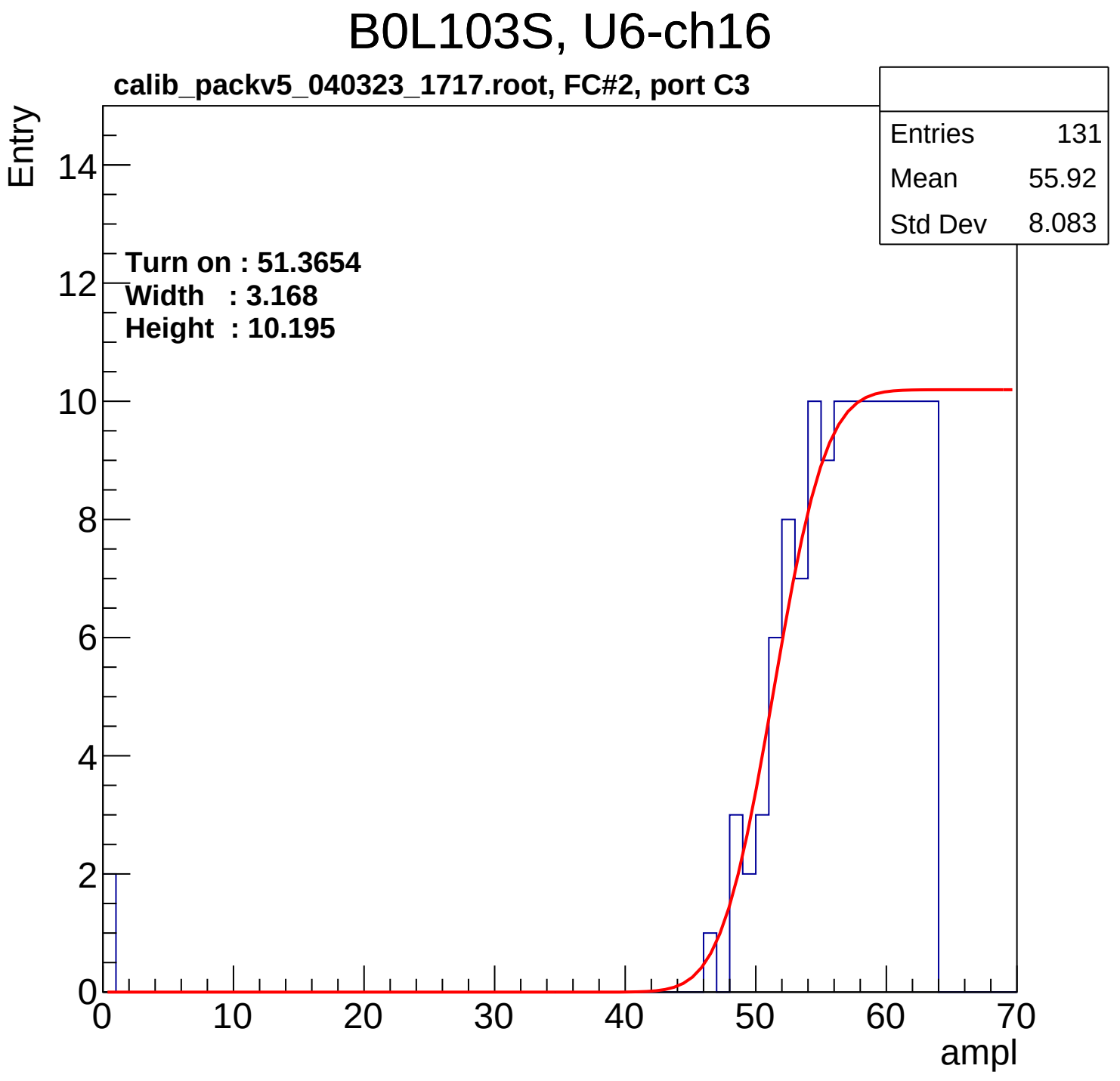
B0L103S, U6-ch16
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 55.92
Std Dev 8.083
Turn on : 51.3654
Width : 3.168
Height : 10.195
Entry
ampl
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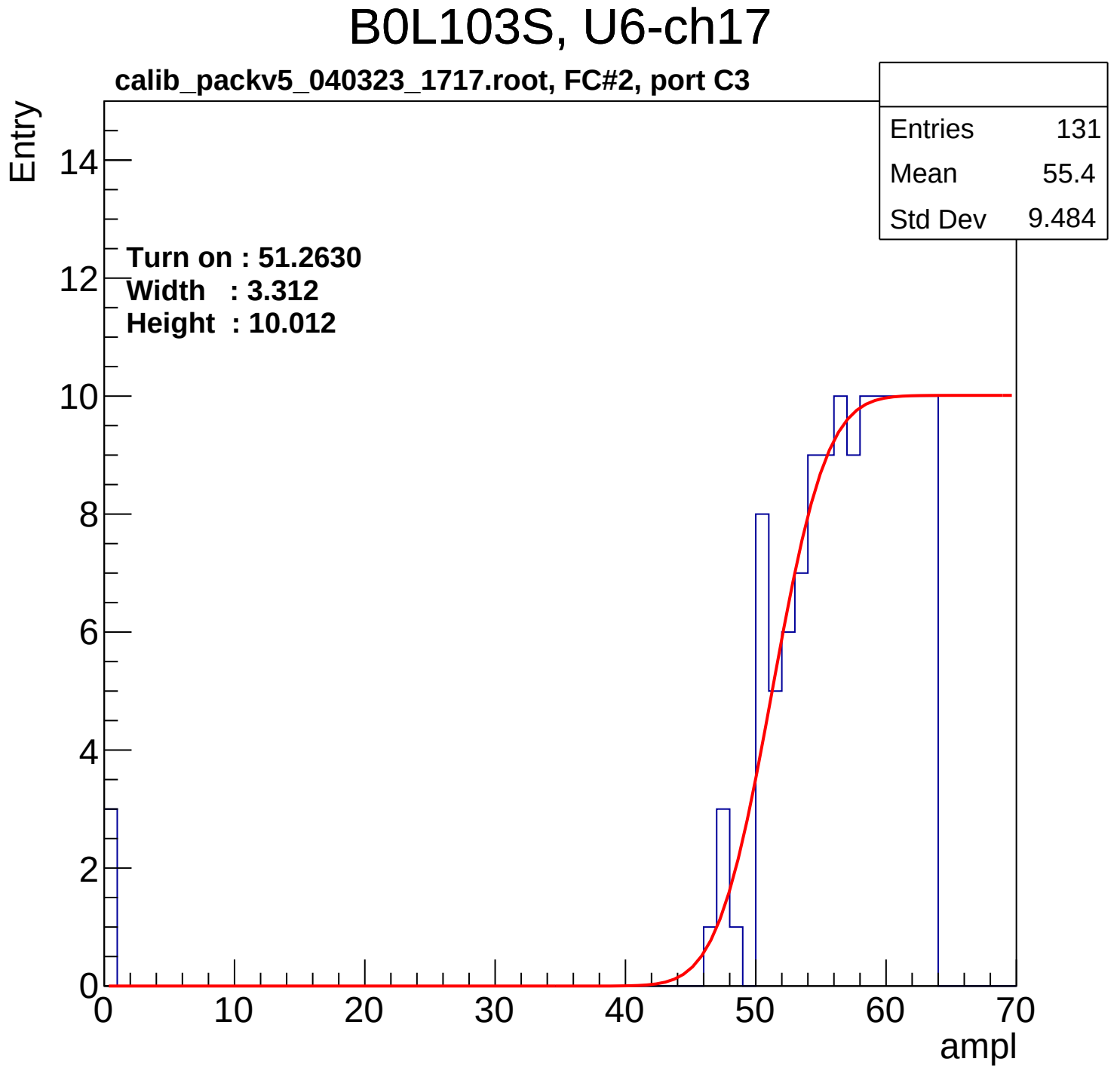
B0L103S, U6-ch17
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 55.4
Std Dev 9.484
Turn on : 51.2630
Width : 3.312
Height : 10.012
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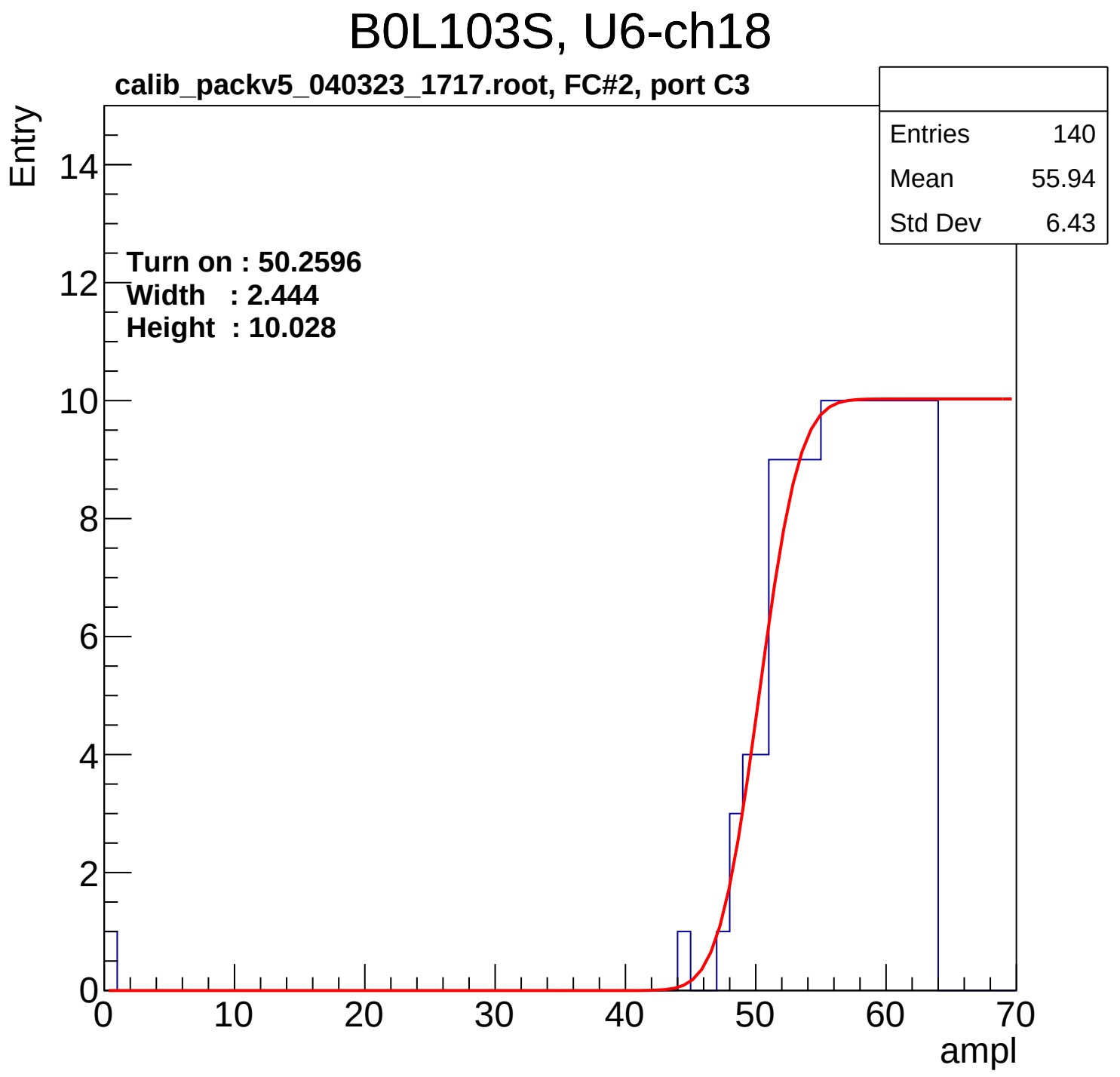
B0L103S, U6-ch18
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 55.94
Std Dev 6.43
Turn on : 50.2596
Width : 2.444
Height : 10.028
Entry
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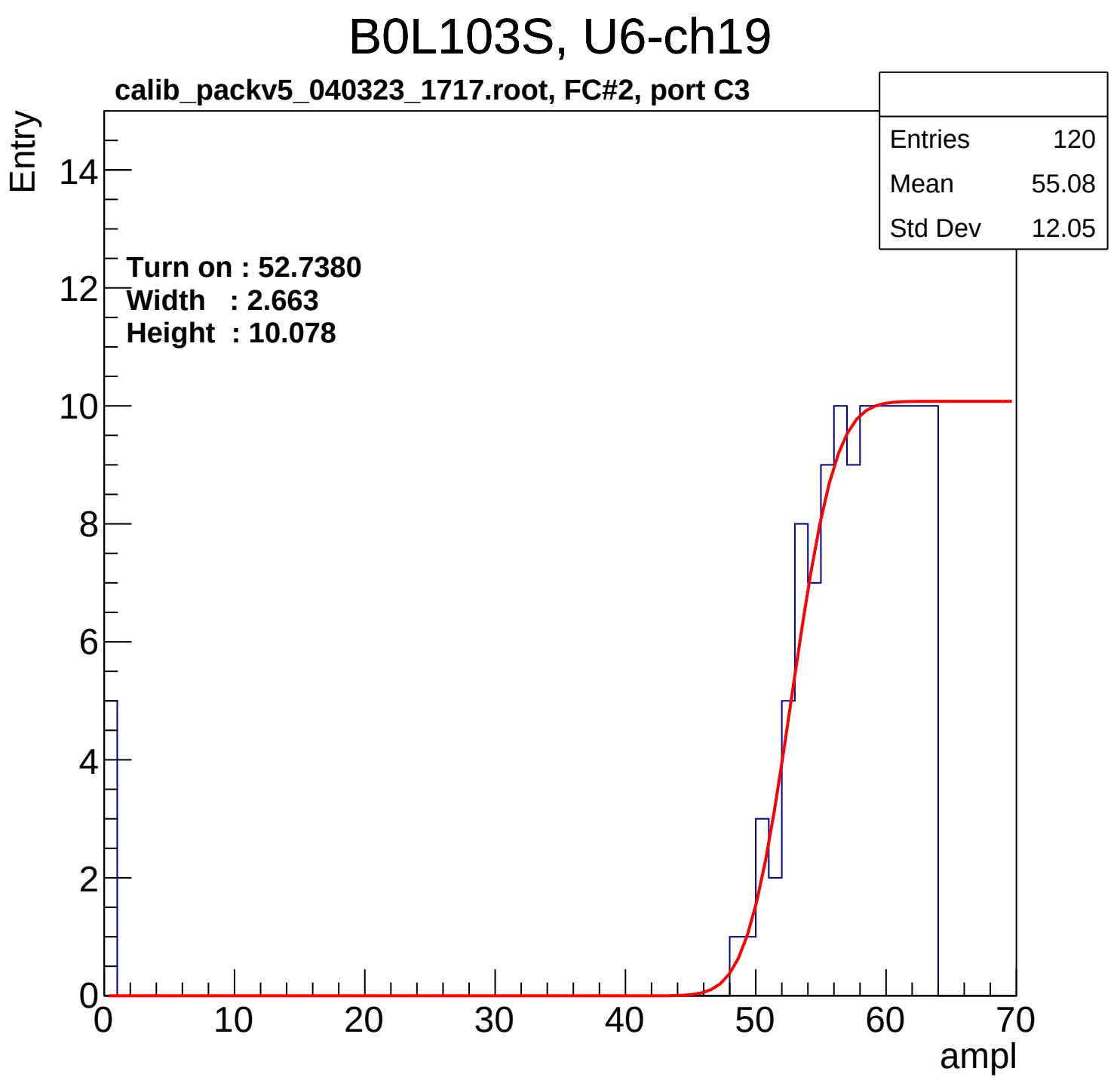
B0L103S, U6-ch19
calib_packv5_040323_1717.root, FC#2, port C3
Entries 120
Mean 55.08
Std Dev 12.05
Turn on : 52.7380
Width : 2.663
Height : 10.078
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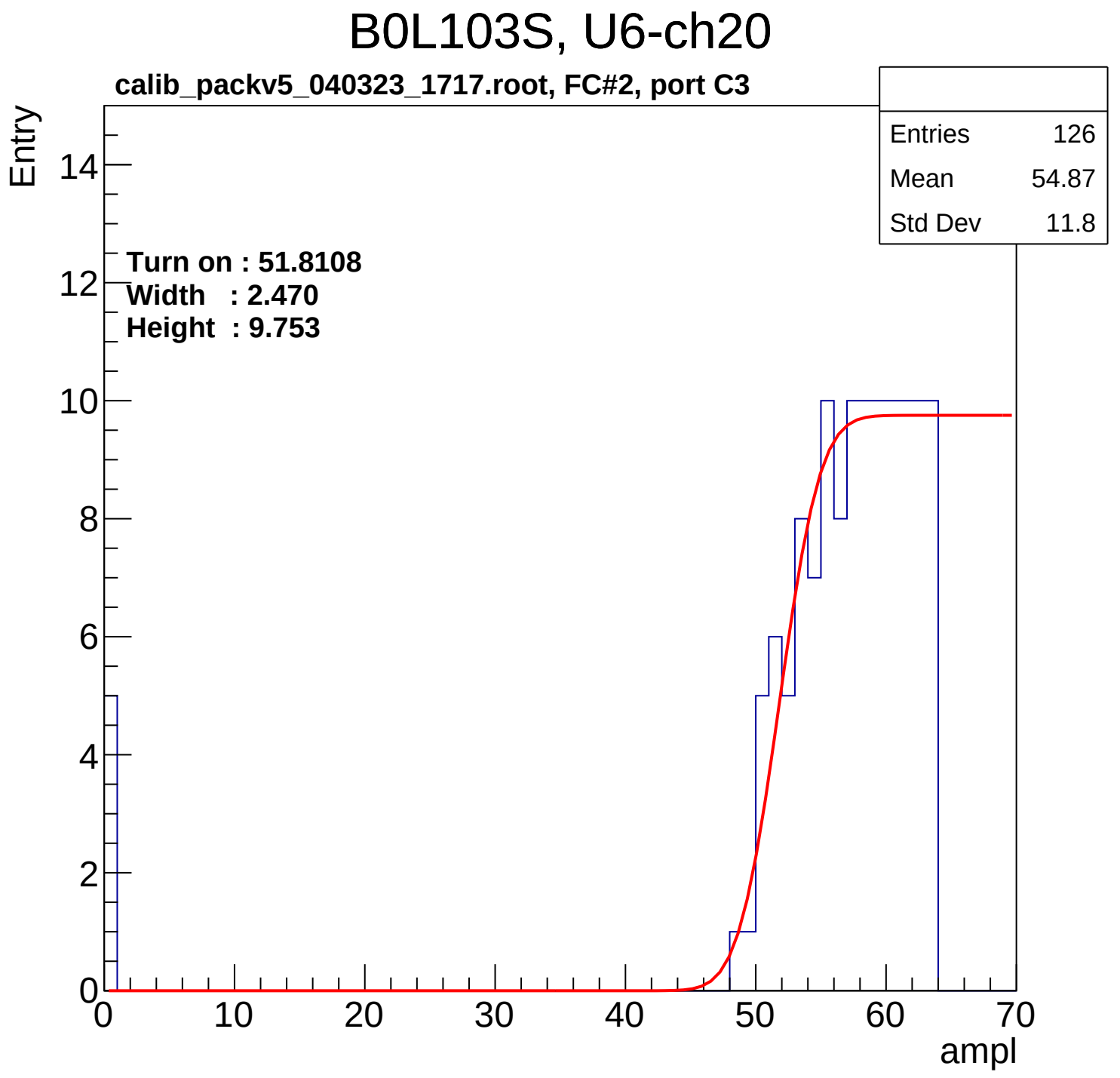
B0L103S, U6-ch20
calib_packv5_040323_1717.root, FC#2, port C3
Entries 126
Mean 54.87
Std Dev 11.8
Turn on : 51.8108
Width : 2.470
Height : 9.753
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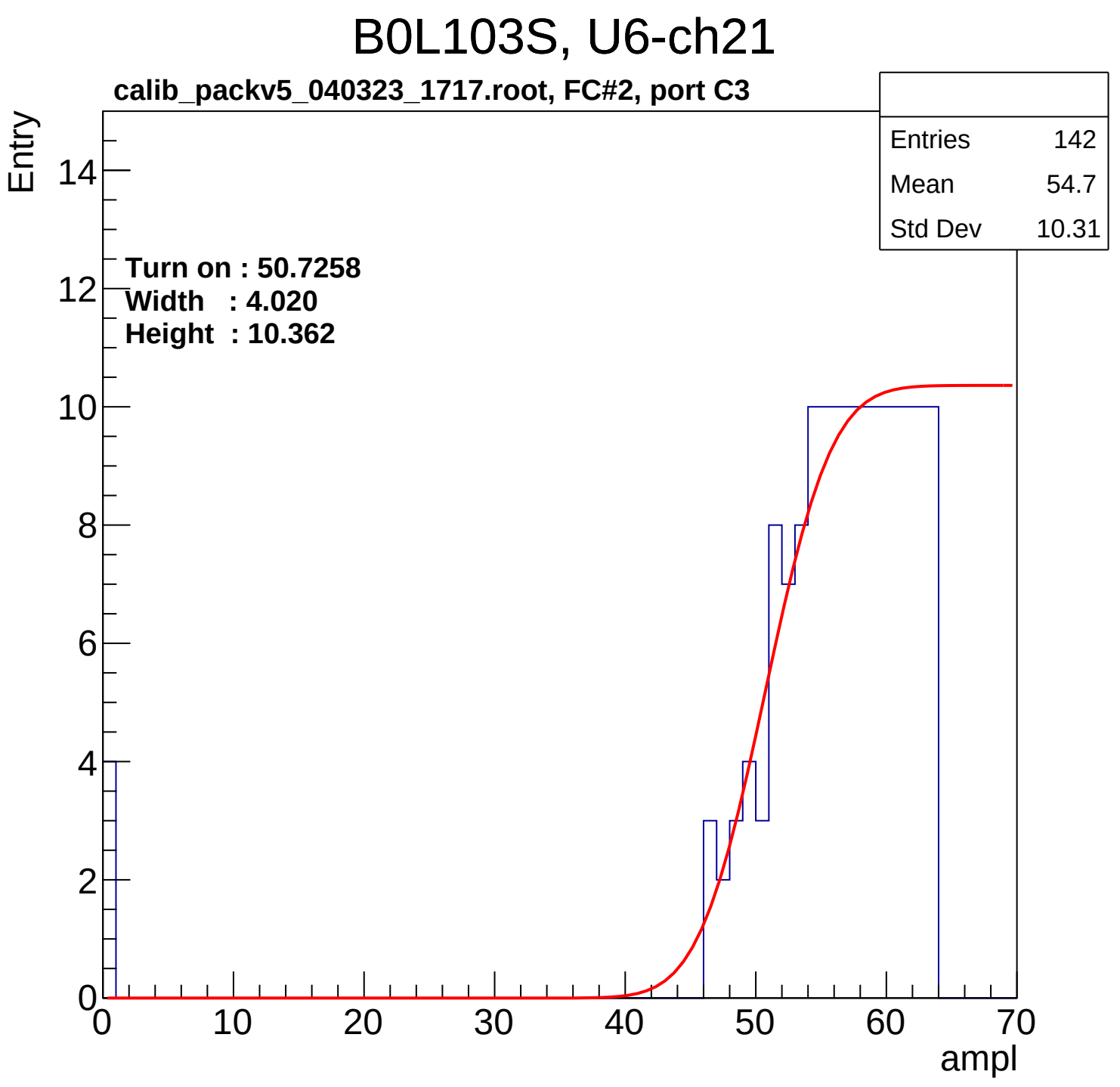
B0L103S, U6-ch21
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 54.7
Std Dev 10.31
Turn on : 50.7258
Width : 4.020
Height : 10.362
Entry
ampl
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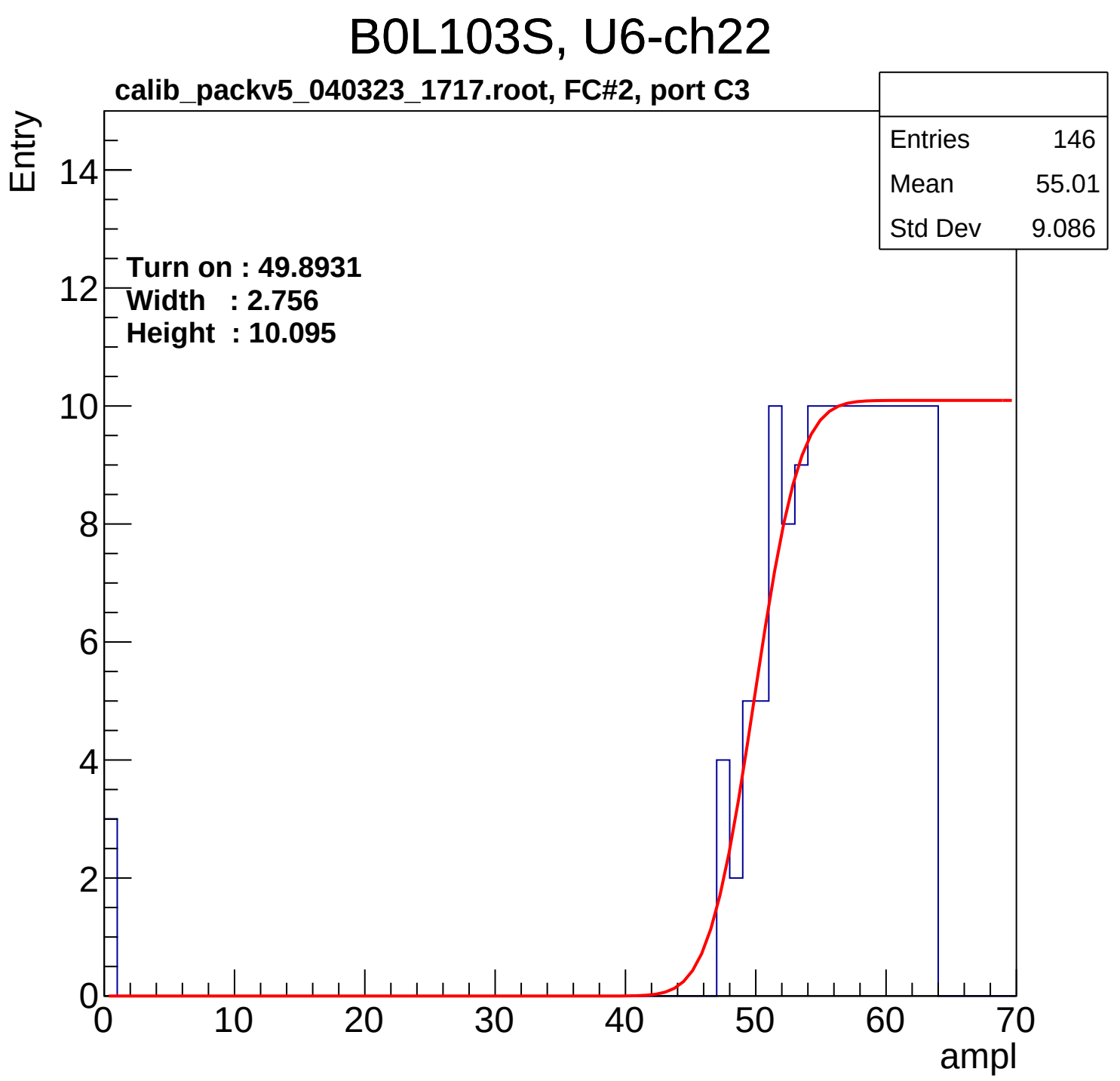
B0L103S, U6-ch22
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 55.01
Std Dev 9.086
Turn on : 49.8931
Width : 2.756
Height : 10.095
Entry
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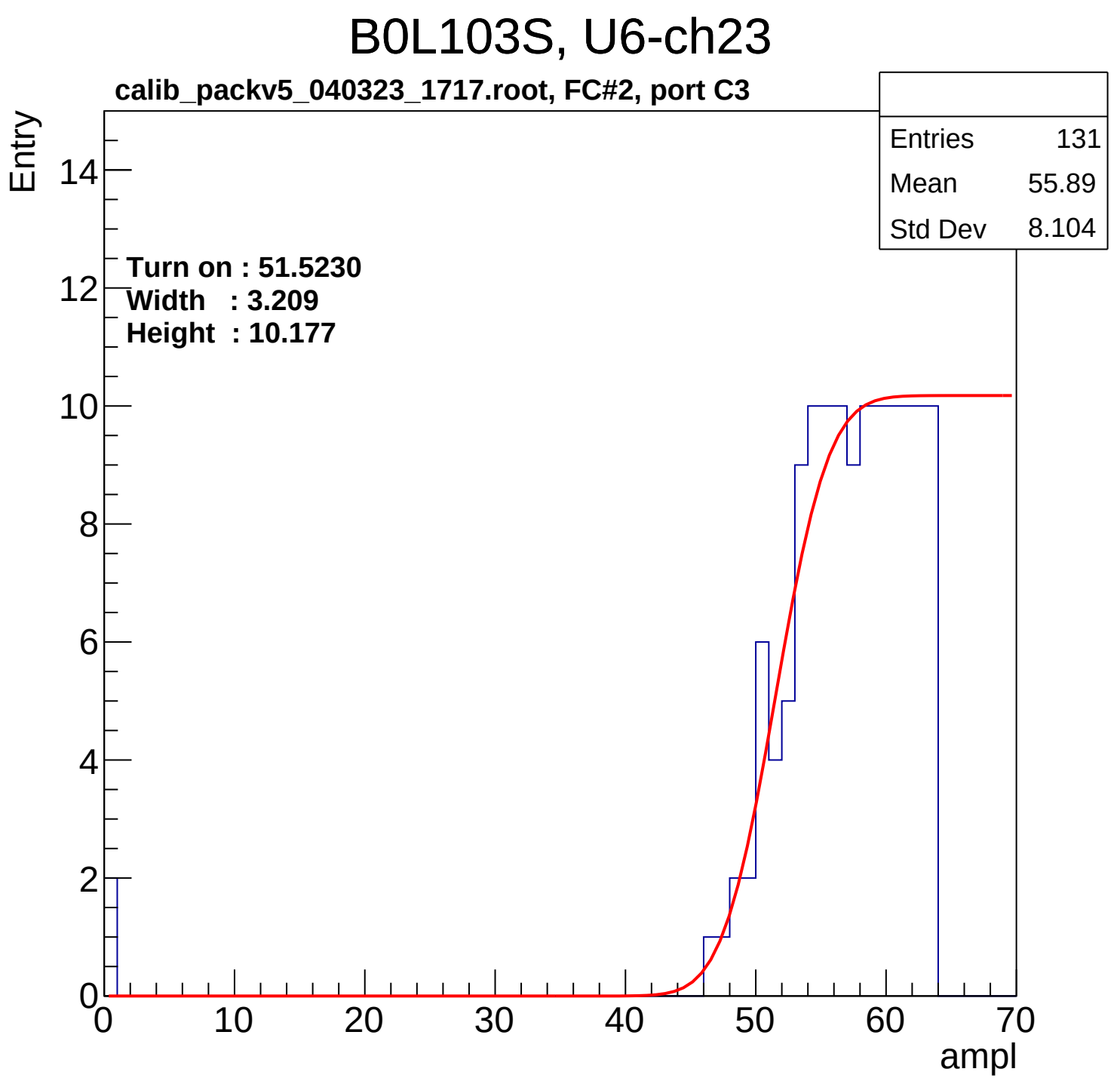
B0L103S, U6-ch23
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 55.89
Std Dev 8.104
Turn on : 51.5230
Width : 3.209
Height : 10.177
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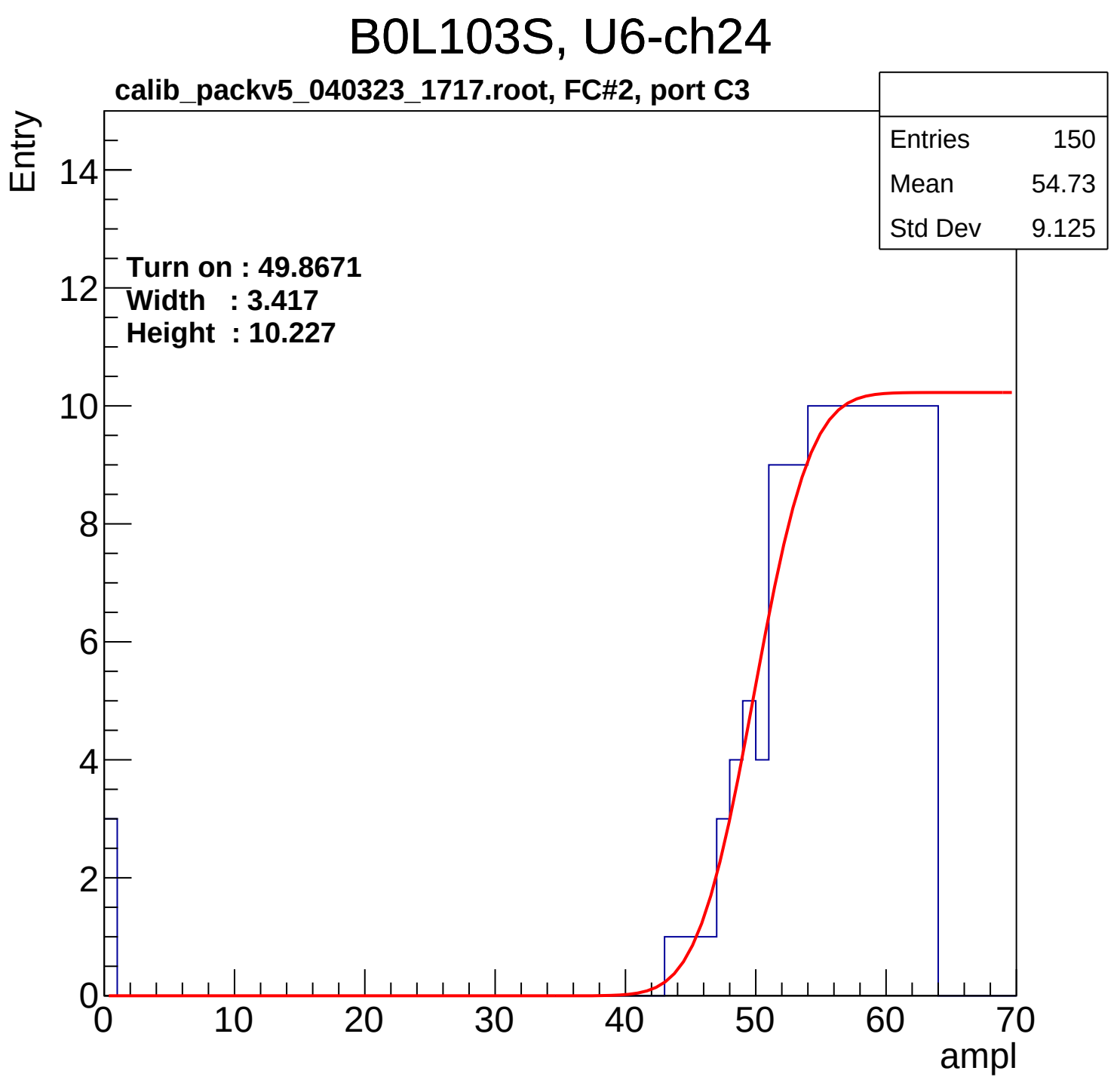
B0L103S, U6-ch24
calib_packv5_040323_1717.root, FC#2, port C3
Entries 150
Mean 54.73
Std Dev 9.125
Turn on : 49.8671
Width : 3.417
Height : 10.227
Entry
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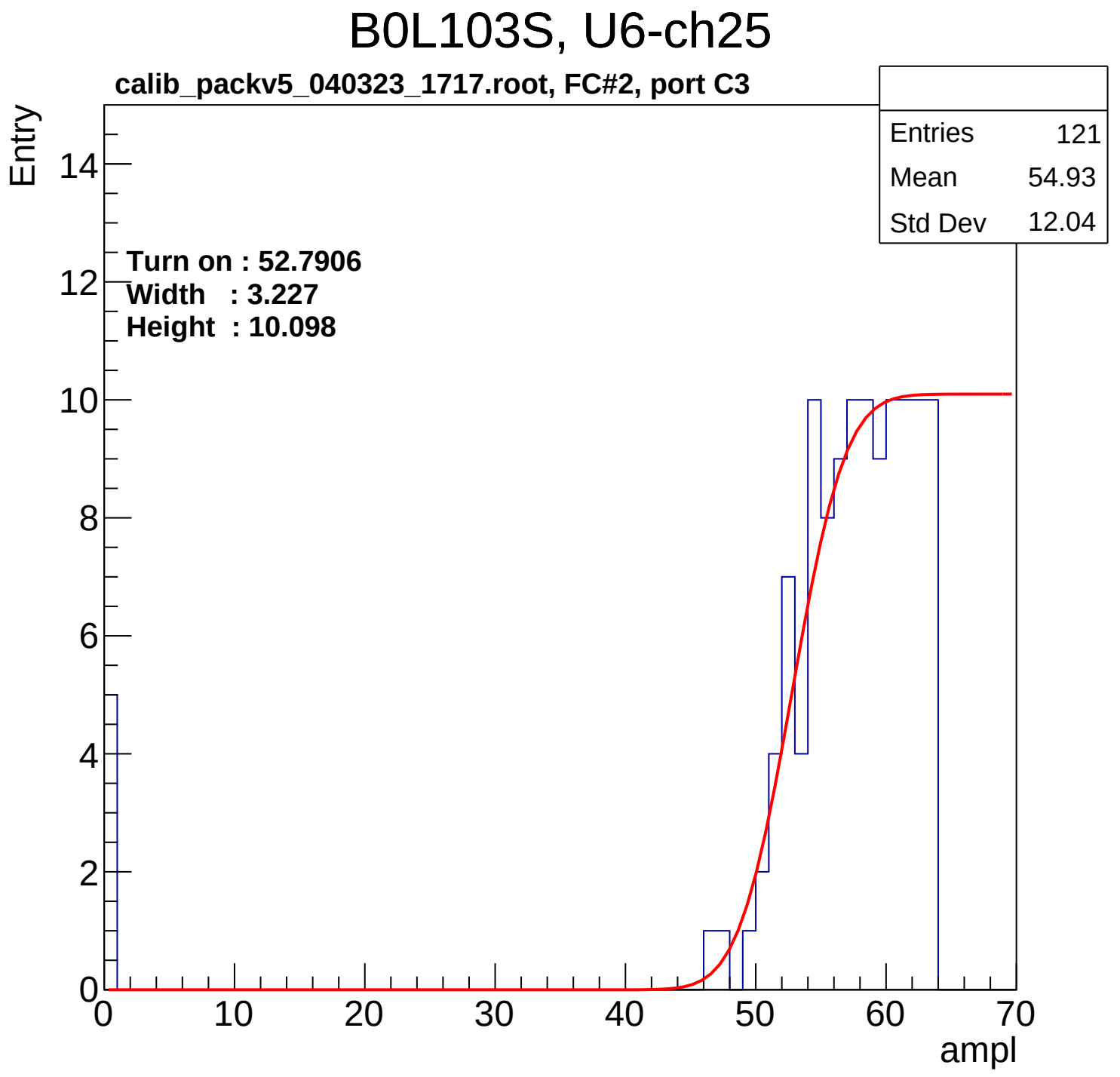
B0L103S, U6-ch25
calib_packv5_040323_1717.root, FC#2, port C3
Entries 121
Mean 54.93
Std Dev 12.04
Turn on : 52.7906
Width : 3.227
Height : 10.098
Entry
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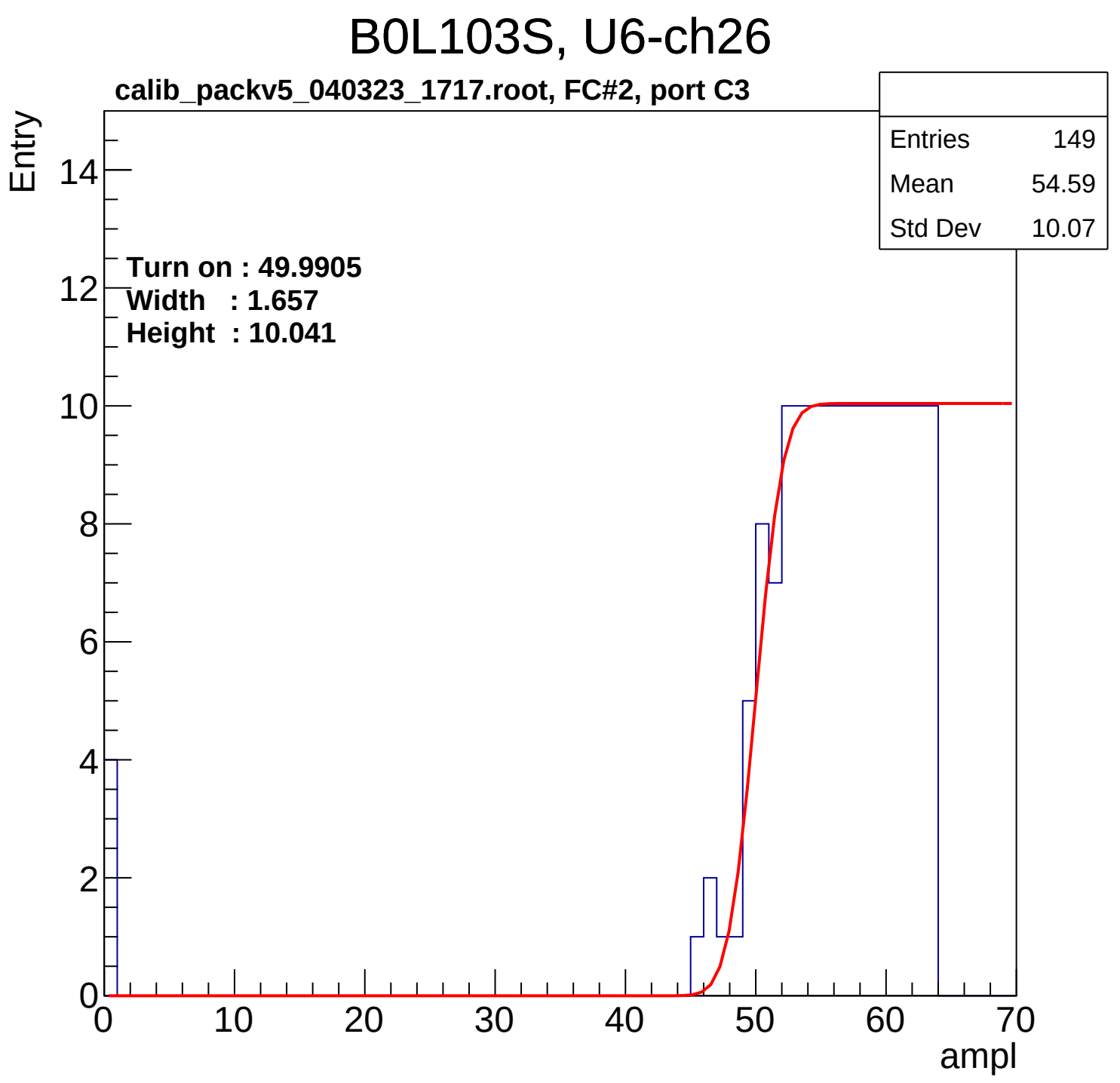
B0L103S, U6-ch26
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 54.59
Std Dev 10.07
Turn on : 49.9905
Width : 1.657
Height : 10.041
Entry
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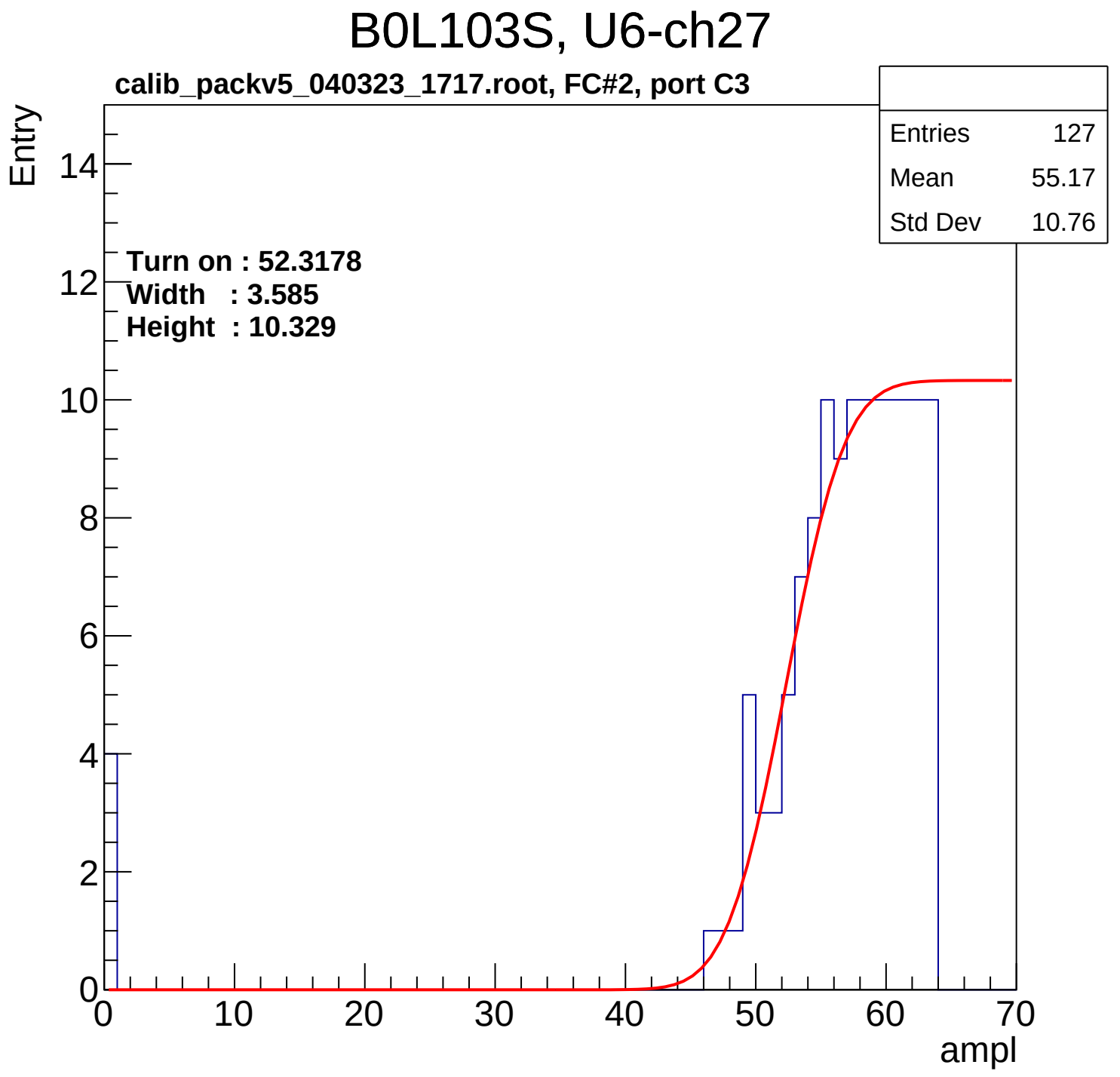
B0L103S, U6-ch27
calib_packv5_040323_1717.root, FC#2, port C3
Entries 127
Mean 55.17
Std Dev 10.76
Turn on : 52.3178
Width : 3.585
Height : 10.329
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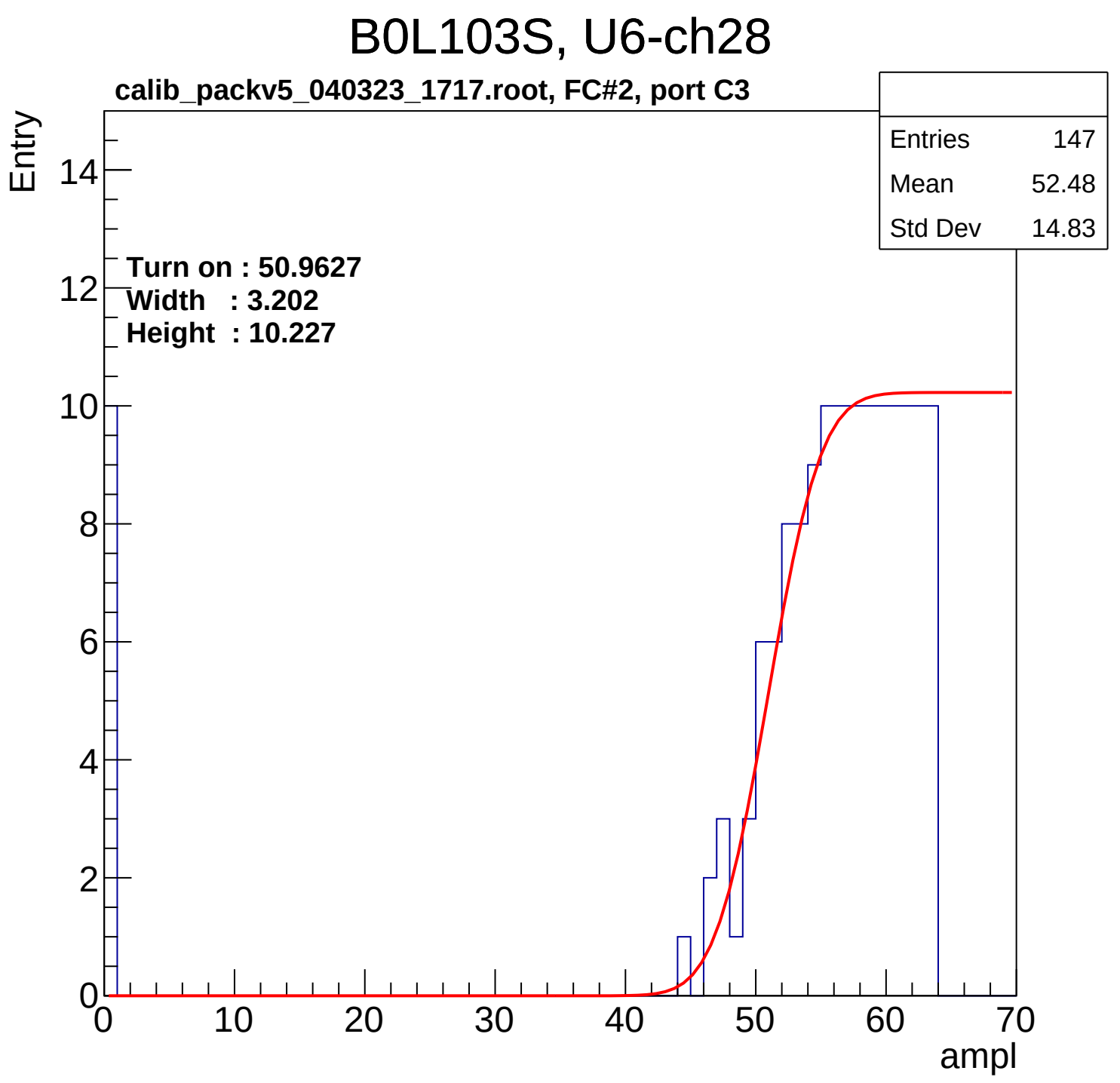
B0L103S, U6-ch28
calib_packv5_040323_1717.root, FC#2, port C3
Entries 147
Mean 52.48
Std Dev 14.83
Turn on : 50.9627
Width : 3.202
Height : 10.227
Entry
ampl
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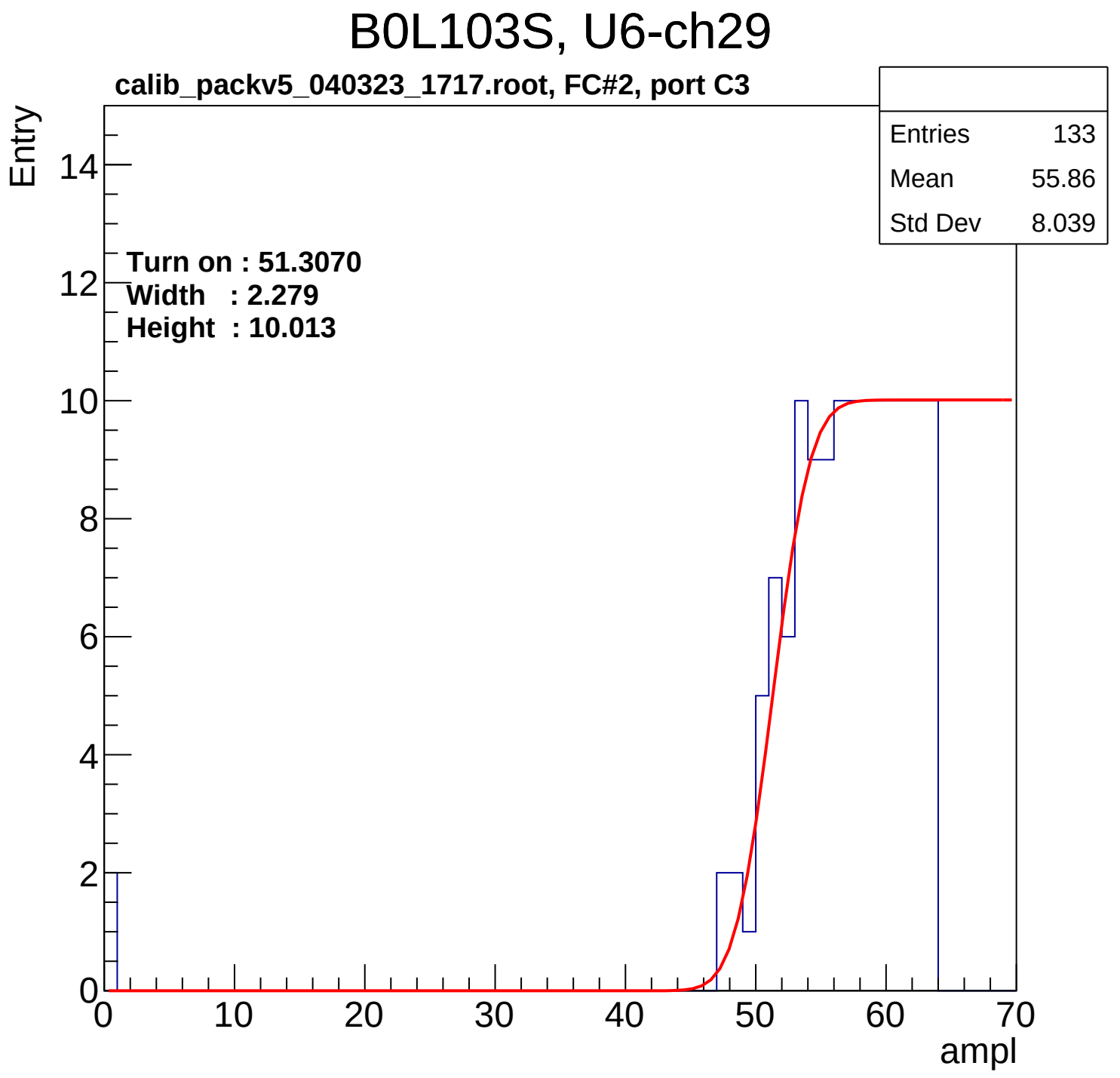
B0L103S, U6-ch29
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 55.86
Std Dev 8.039
Turn on : 51.3070
Width : 2.279
Height : 10.013
Entry
ampl
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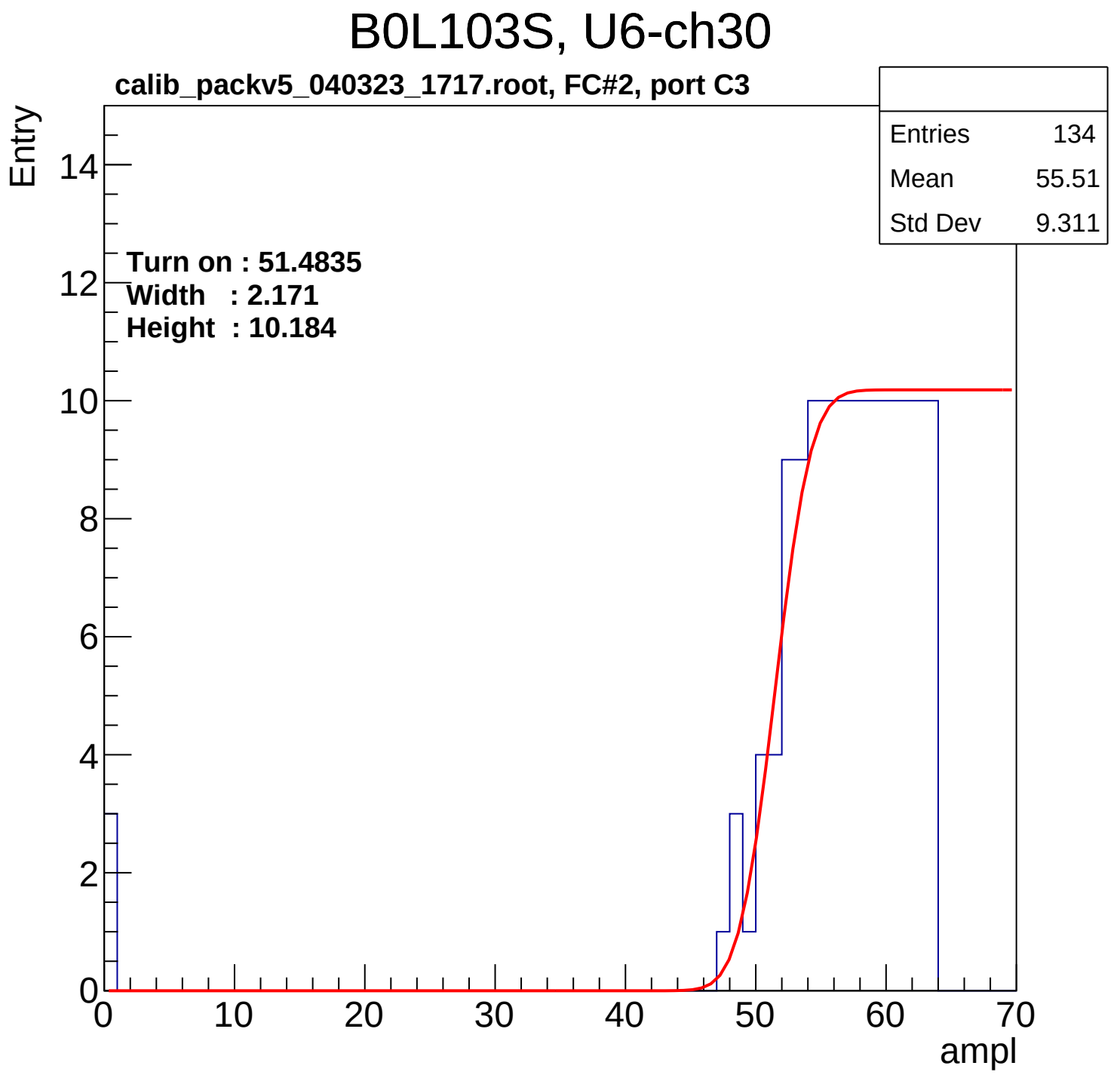
B0L103S, U6-ch30
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 55.51
Std Dev 9.311
Turn on : 51.4835
Width : 2.171
Height : 10.184
Entry
ampl
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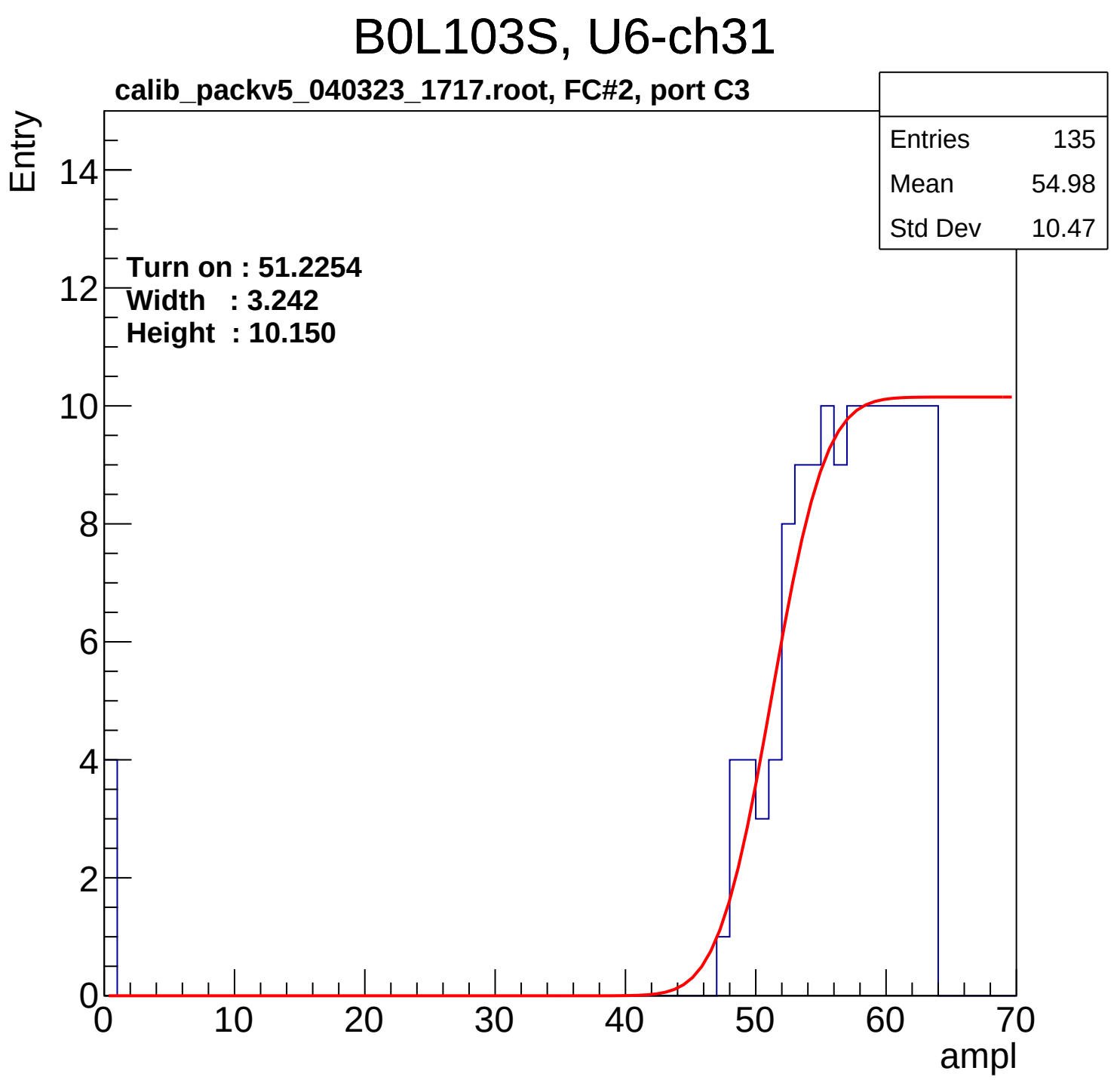
B0L103S, U6-ch31
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 54.98
Std Dev 10.47
Turn on : 51.2254
Width : 3.242
Height : 10.150
Entry
ampl
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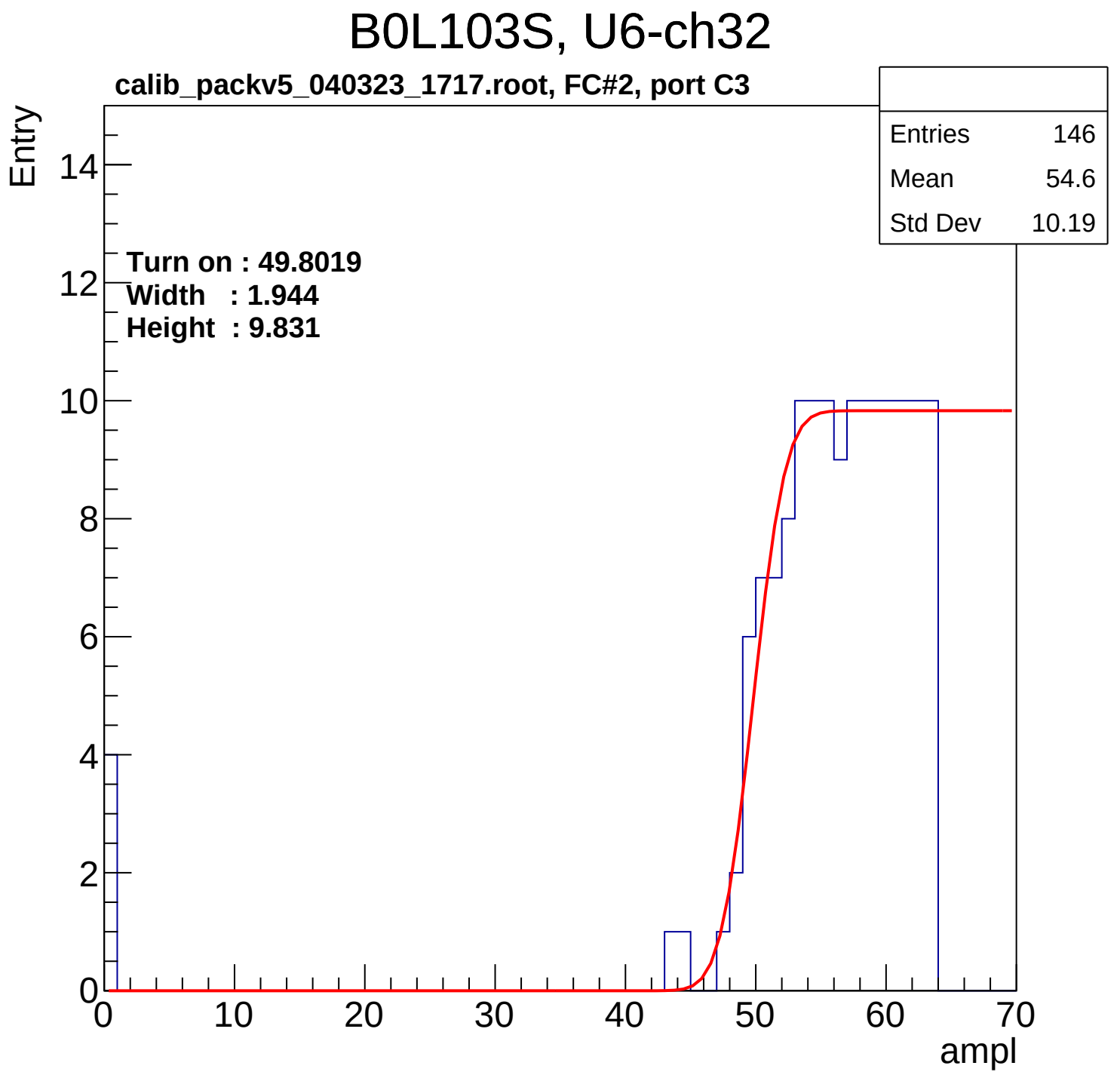
B0L103S, U6-ch32
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 54.6
Std Dev 10.19
Turn on : 49.8019
Width : 1.944
Height : 9.831
Entry
ampl
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4
6
8
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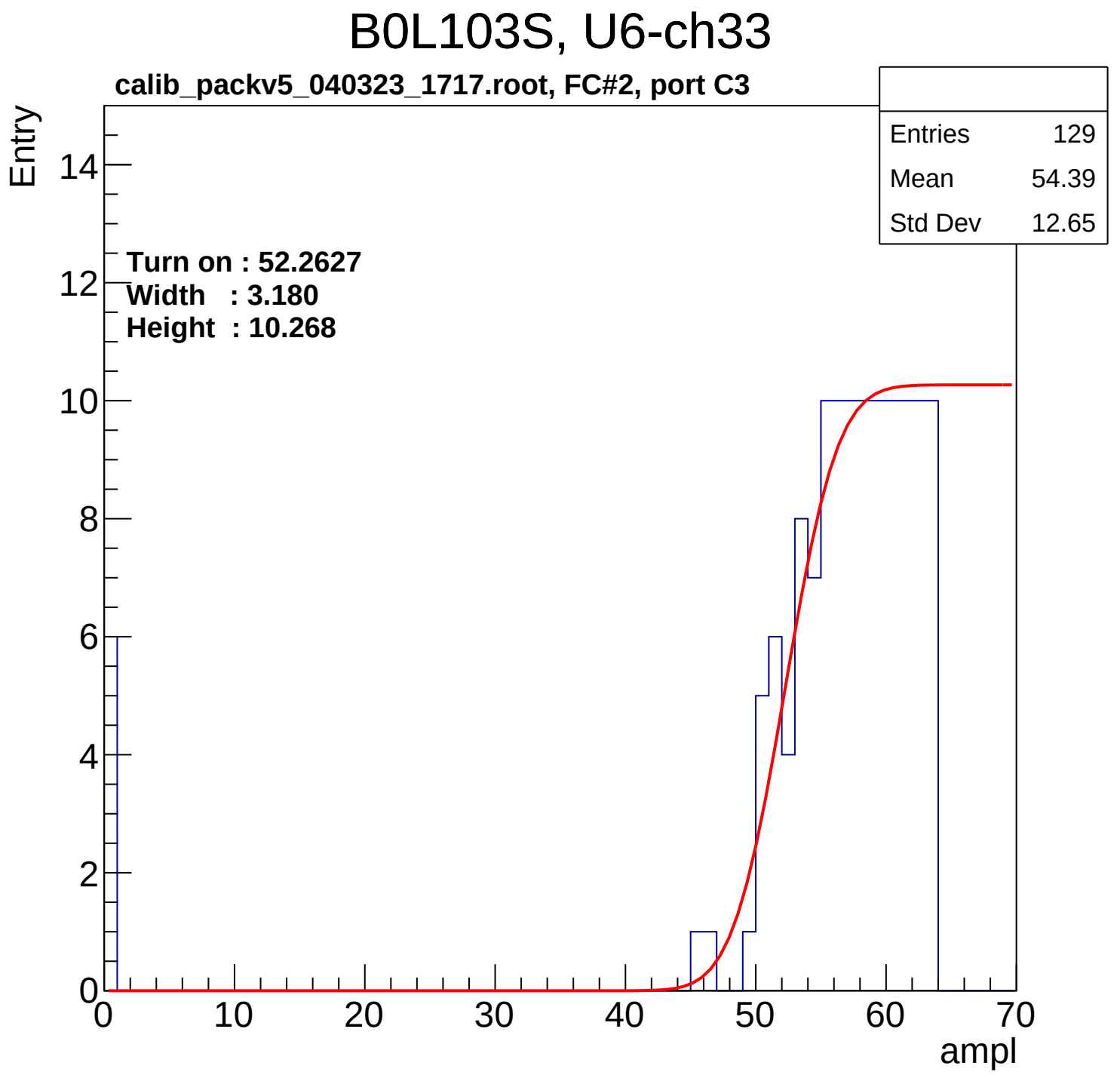
B0L103S, U6-ch33
calib_packv5_040323_1717.root, FC#2, port C3
Entries 129
Mean 54.39
Std Dev 12.65
Turn on : 52.2627
Width : 3.180
Height : 10.268
Entry
ampl
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8
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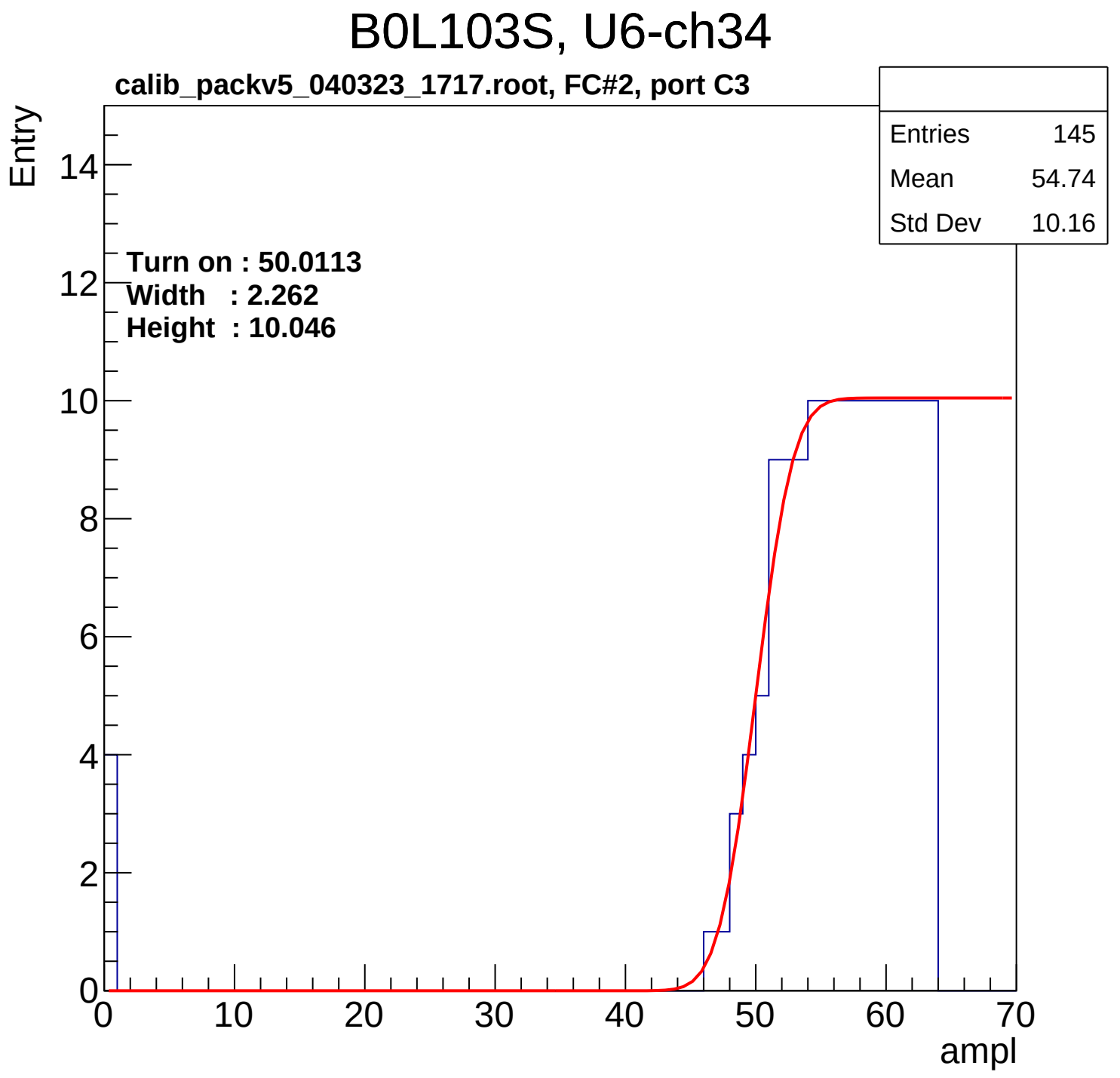
B0L103S, U6-ch34
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 54.74
Std Dev 10.16
Turn on : 50.0113
Width : 2.262
Height : 10.046
Entry
ampl
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2
4
6
8
10
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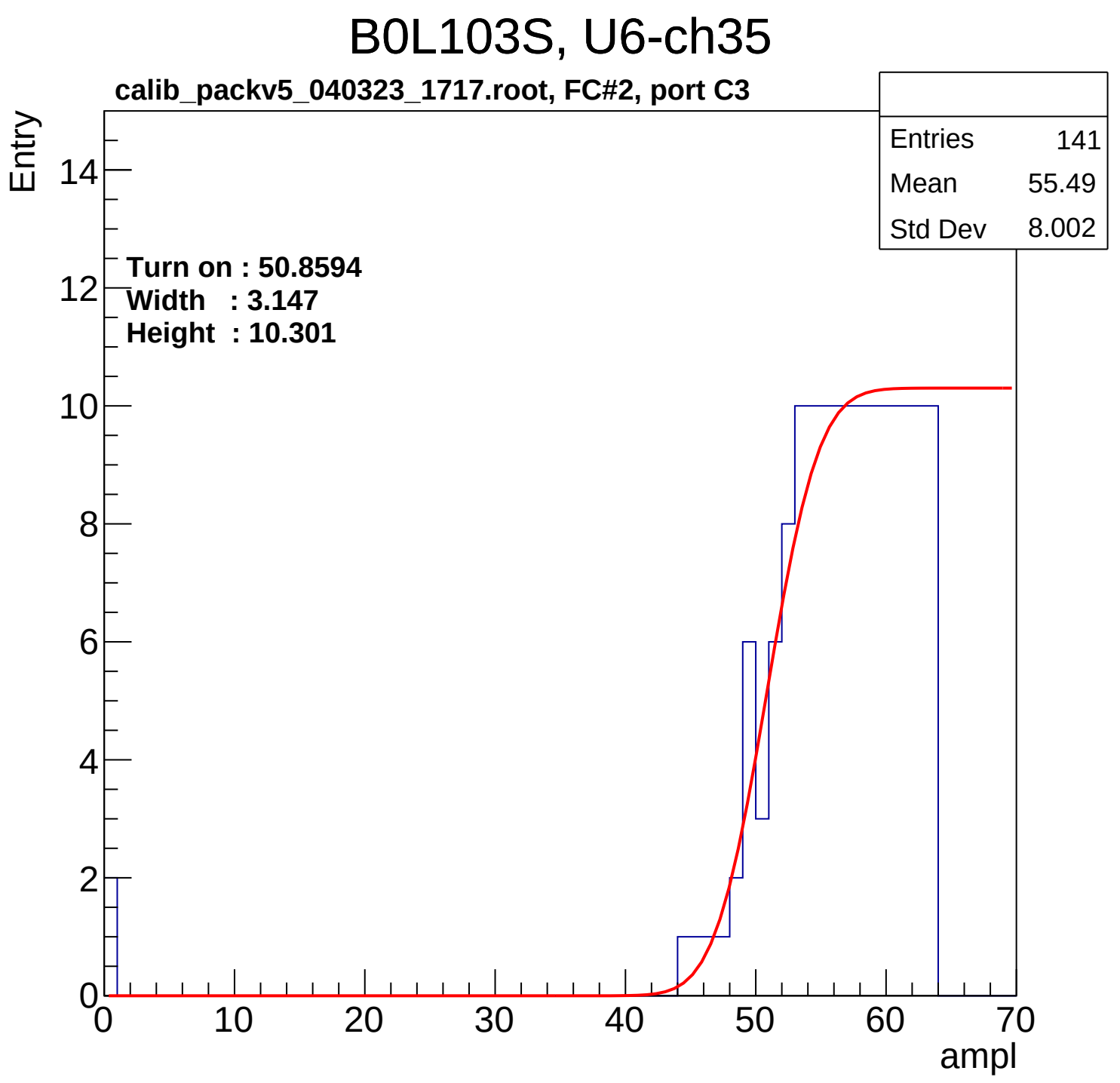
B0L103S, U6-ch35
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 55.49
Std Dev 8.002
Turn on : 50.8594
Width : 3.147
Height : 10.301
Entry
ampl
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6
8
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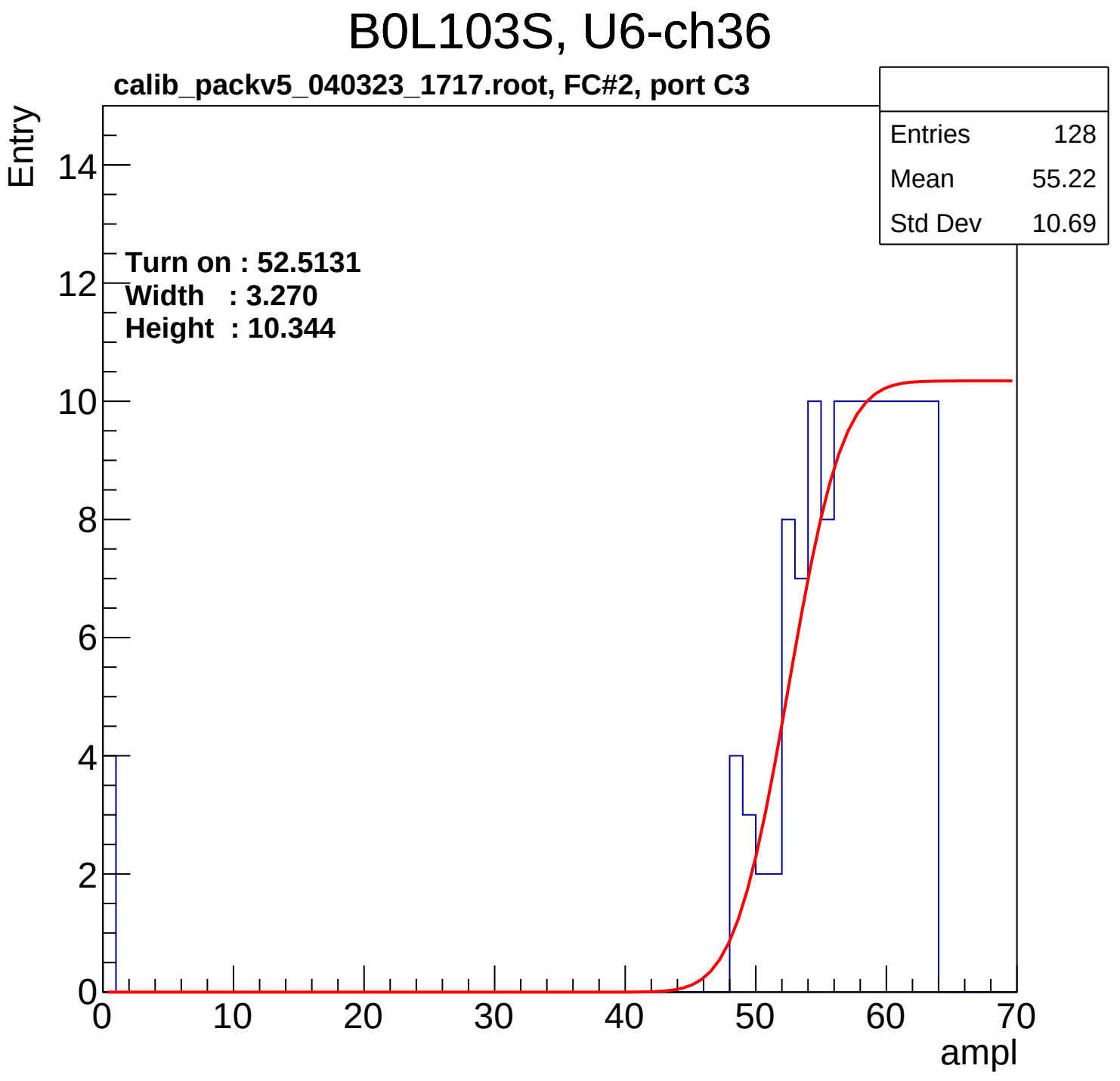
B0L103S, U6-ch36
calib_packv5_040323_1717.root, FC#2, port C3
Entries 128
Mean 55.22
Std Dev 10.69
Turn on : 52.5131
Width : 3.270
Height : 10.344
Entry
ampl
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6
8
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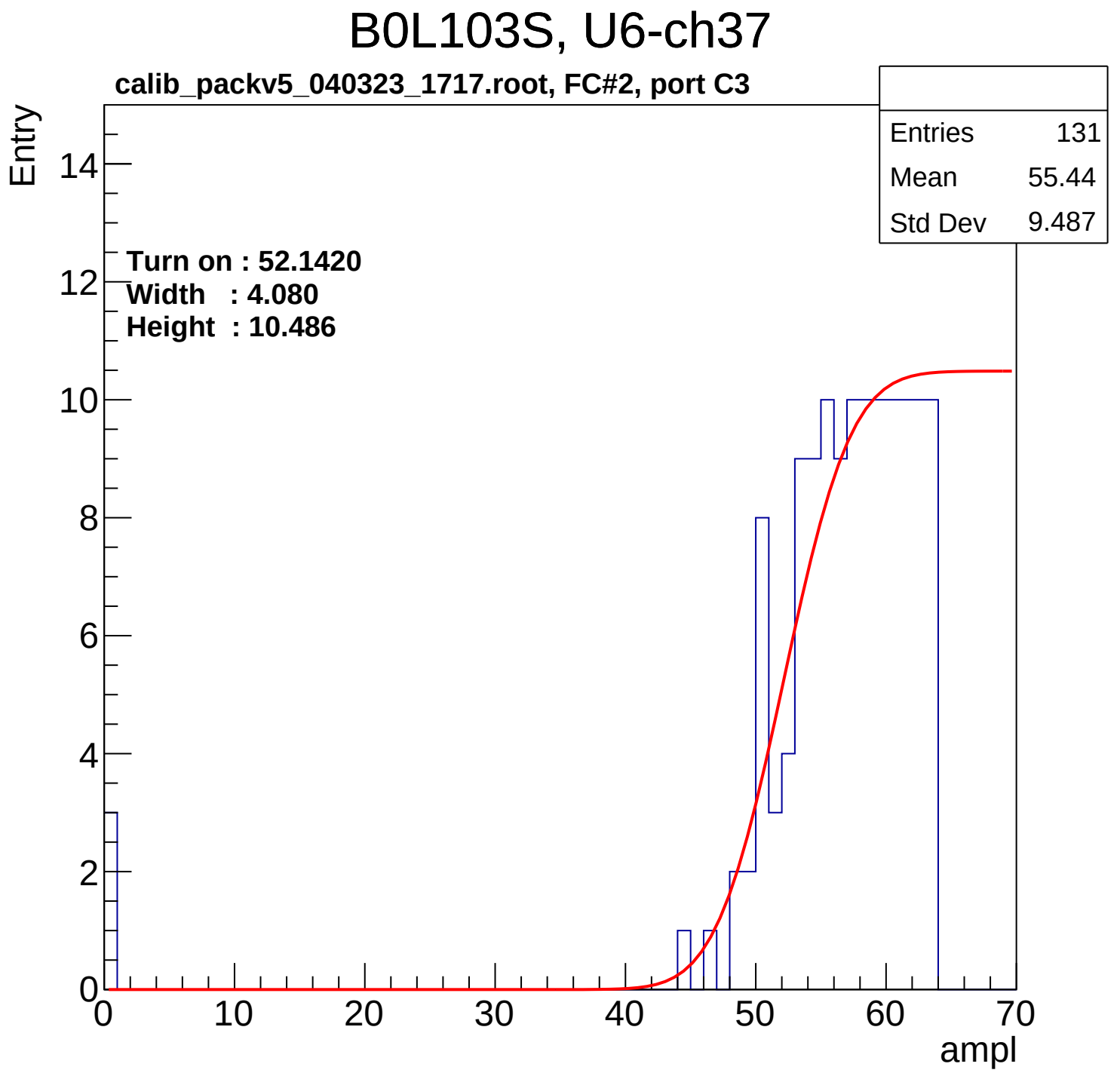
B0L103S, U6-ch37
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 55.44
Std Dev 9.487
Turn on : 52.1420
Width : 4.080
Height : 10.486
Entry
ampl
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8
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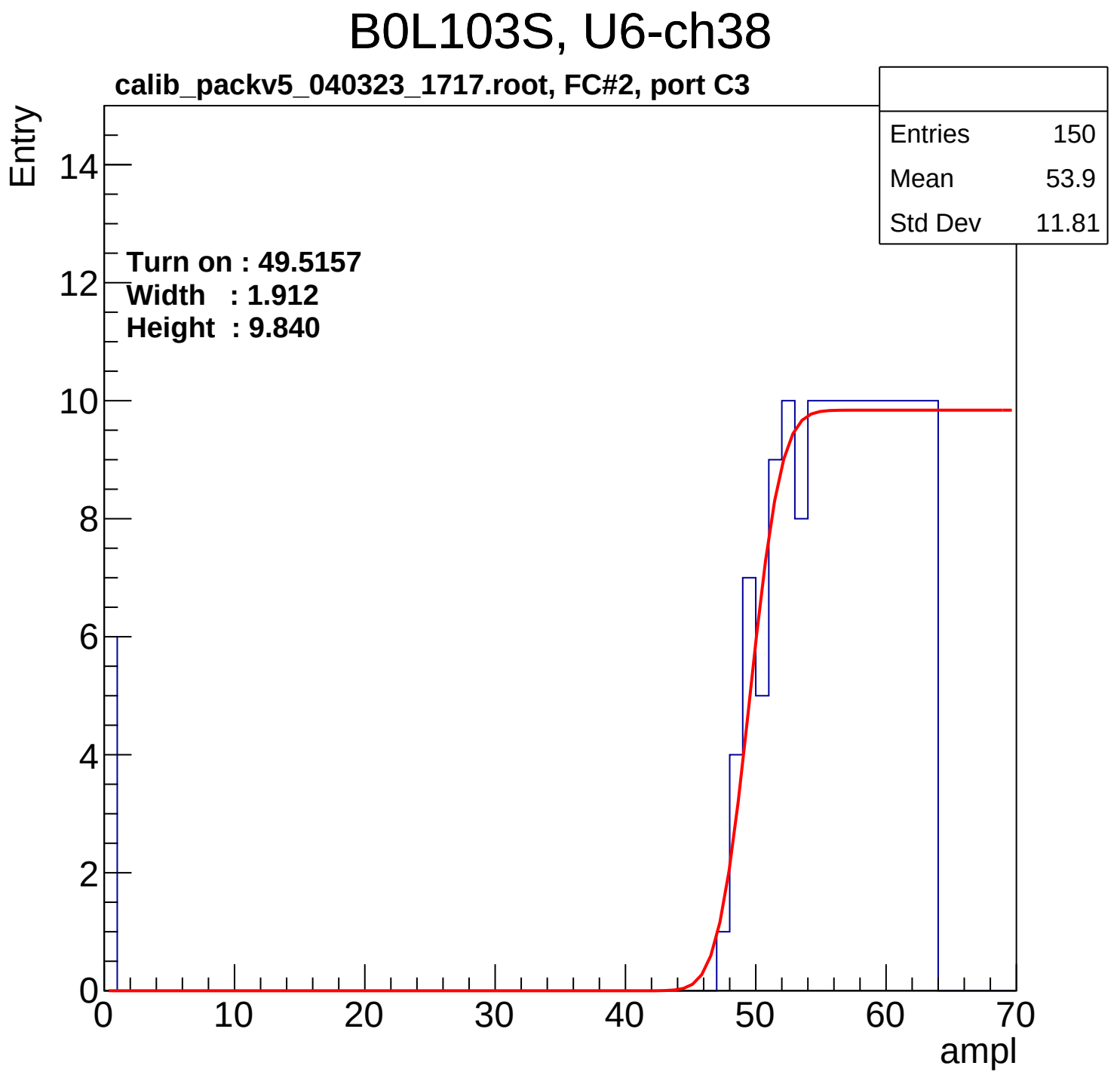
B0L103S, U6-ch38
calib_packv5_040323_1717.root, FC#2, port C3
Entries 150
Mean 53.9
Std Dev 11.81
Turn on : 49.5157
Width : 1.912
Height : 9.840
Entry
ampl
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6
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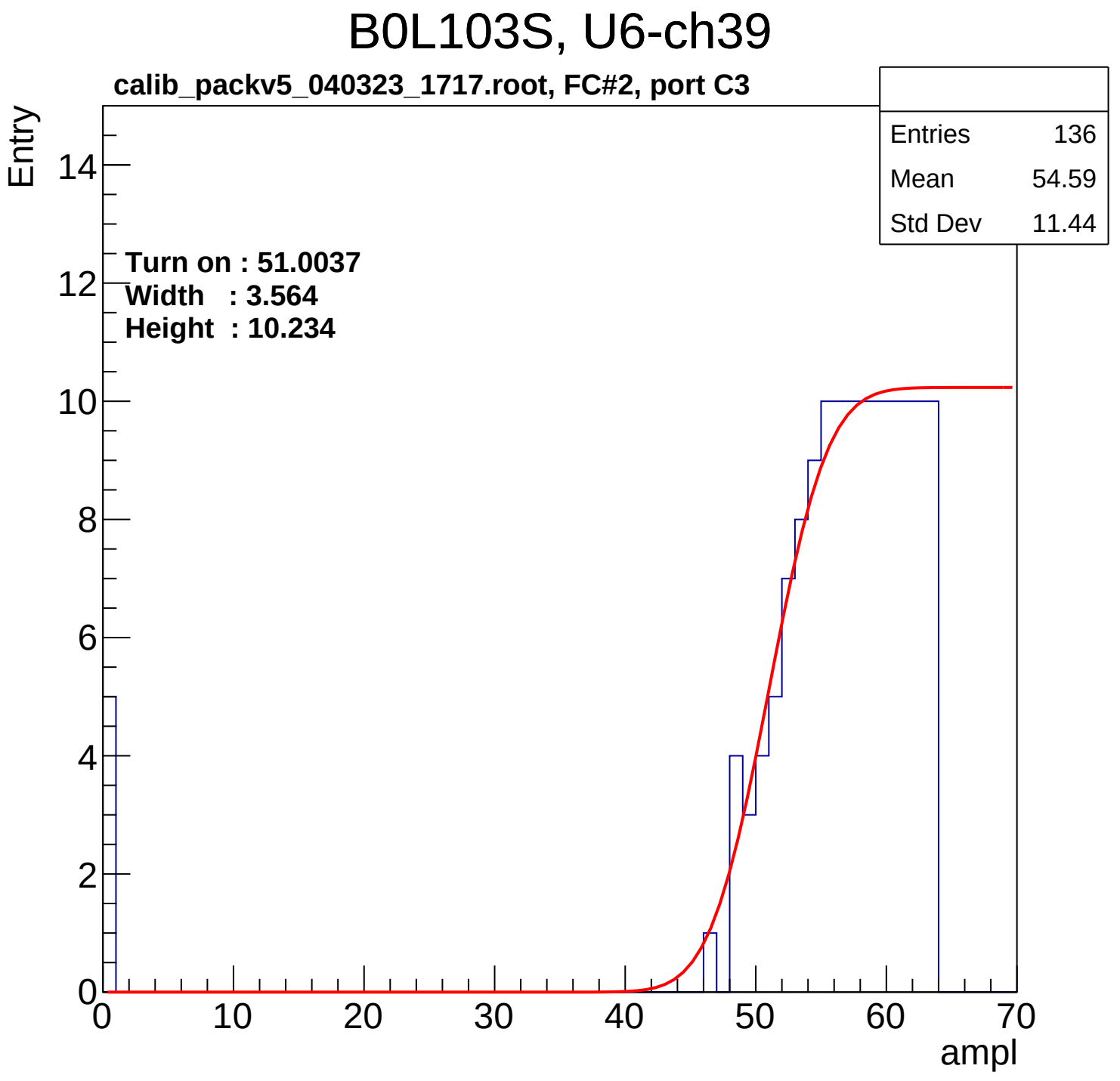
B0L103S, U6-ch39
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 54.59
Std Dev 11.44
Turn on : 51.0037
Width : 3.564
Height : 10.234
Entry
ampl
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8
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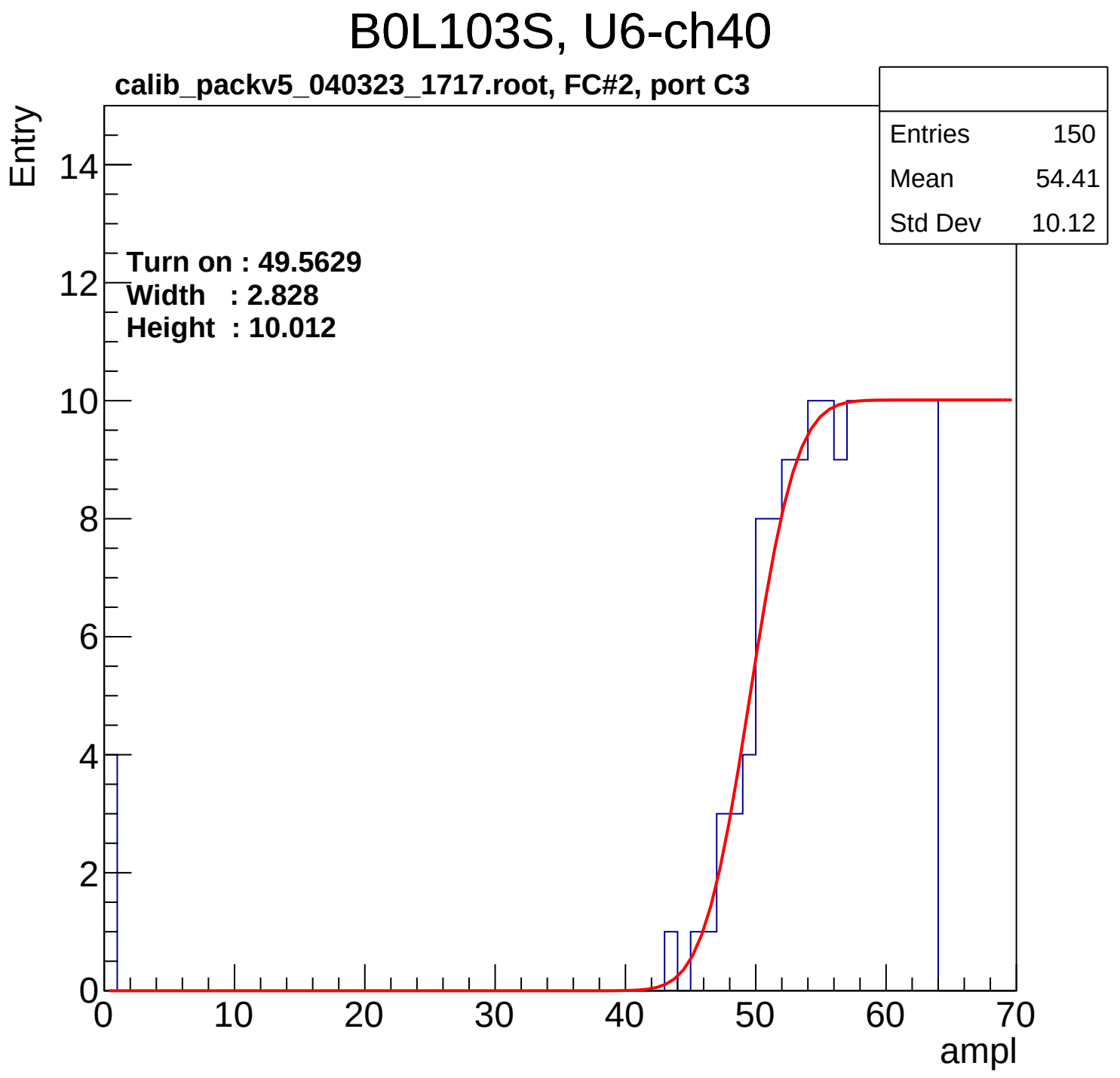
B0L103S, U6-ch40
calib_packv5_040323_1717.root, FC#2, port C3
Entries 150
Mean 54.41
Std Dev 10.12
Turn on : 49.5629
Width : 2.828
Height : 10.012
Entry
ampl
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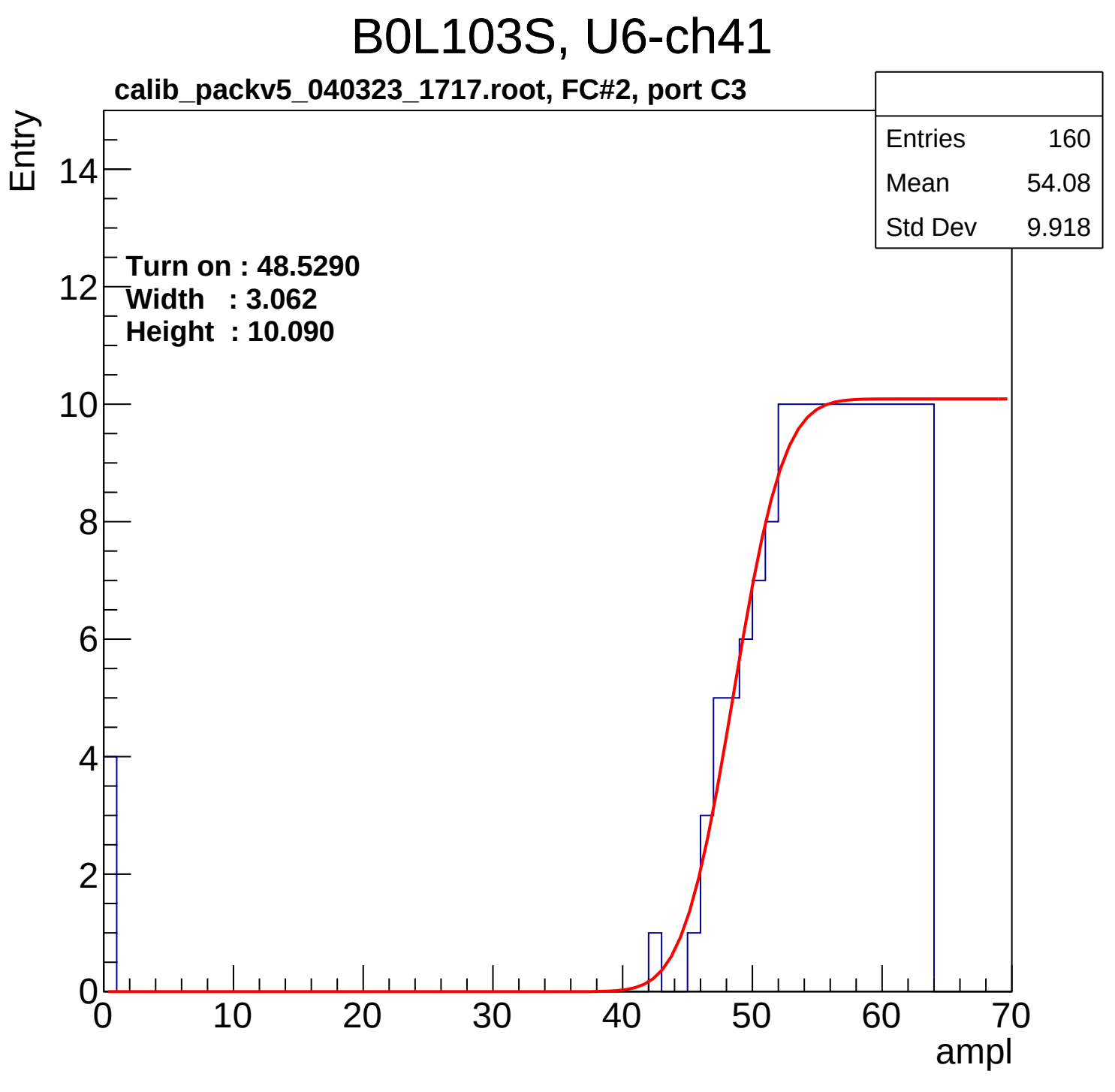
B0L103S, U6-ch41
calib_packv5_040323_1717.root, FC#2, port C3
Entries 160
Mean 54.08
Std Dev 9.918
Turn on : 48.5290
Width : 3.062
Height : 10.090
Entry
ampl
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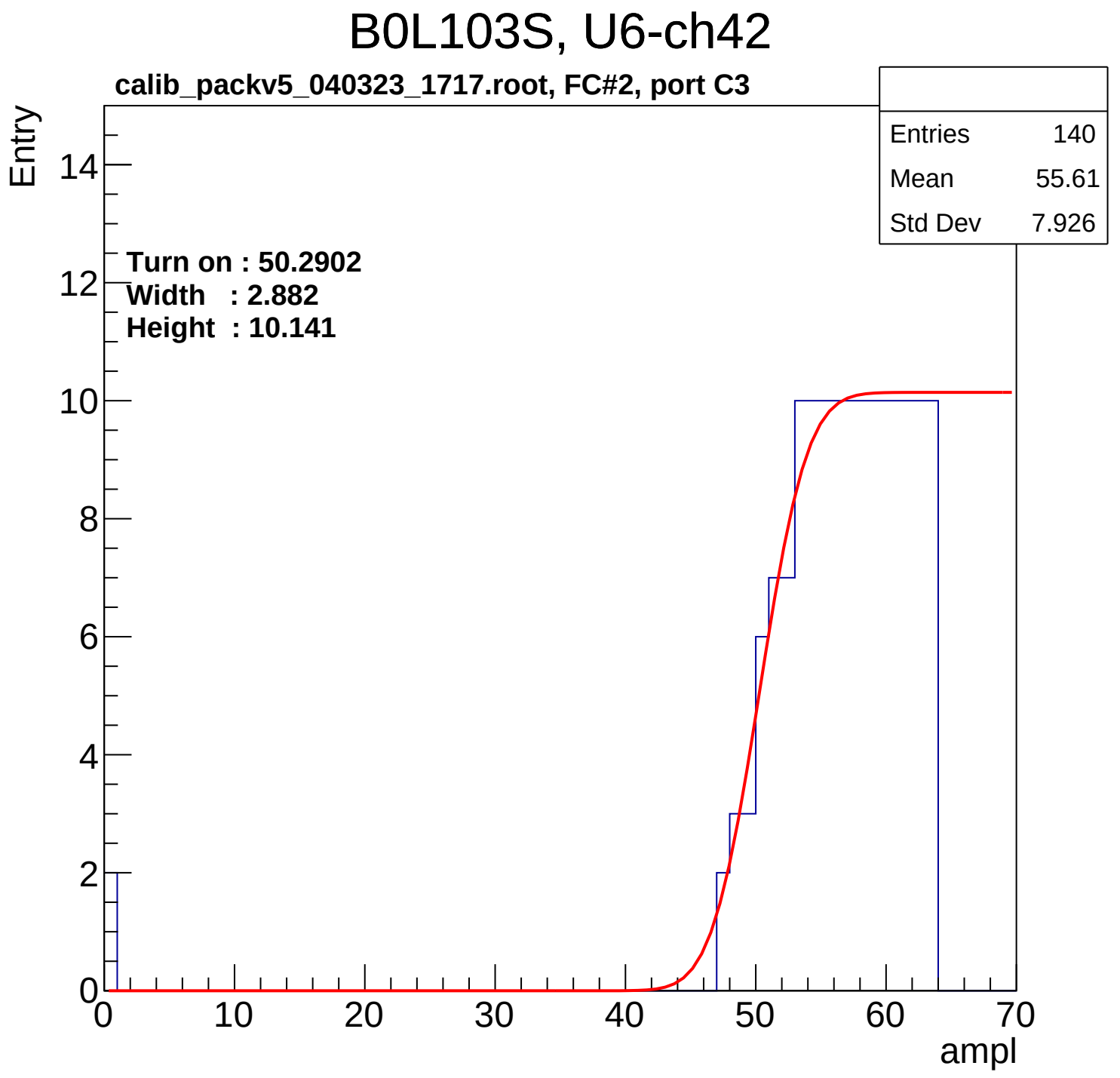
B0L103S, U6-ch42
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 55.61
Std Dev 7.926
Turn on : 50.2902
Width : 2.882
Height : 10.141
Entry
ampl
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8
10
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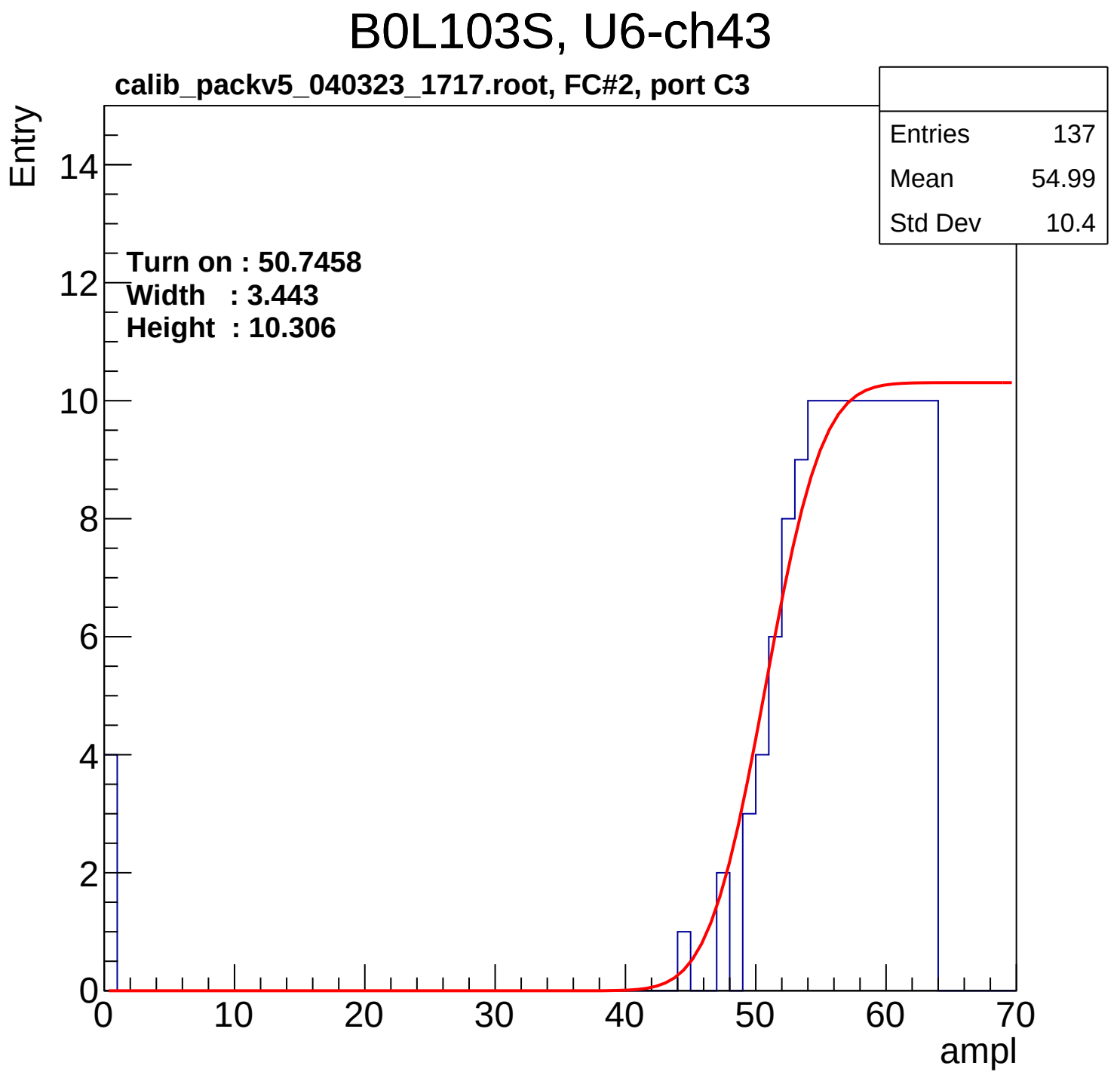
B0L103S, U6-ch43
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 54.99
Std Dev 10.4
Turn on : 50.7458
Width : 3.443
Height : 10.306
Entry
ampl
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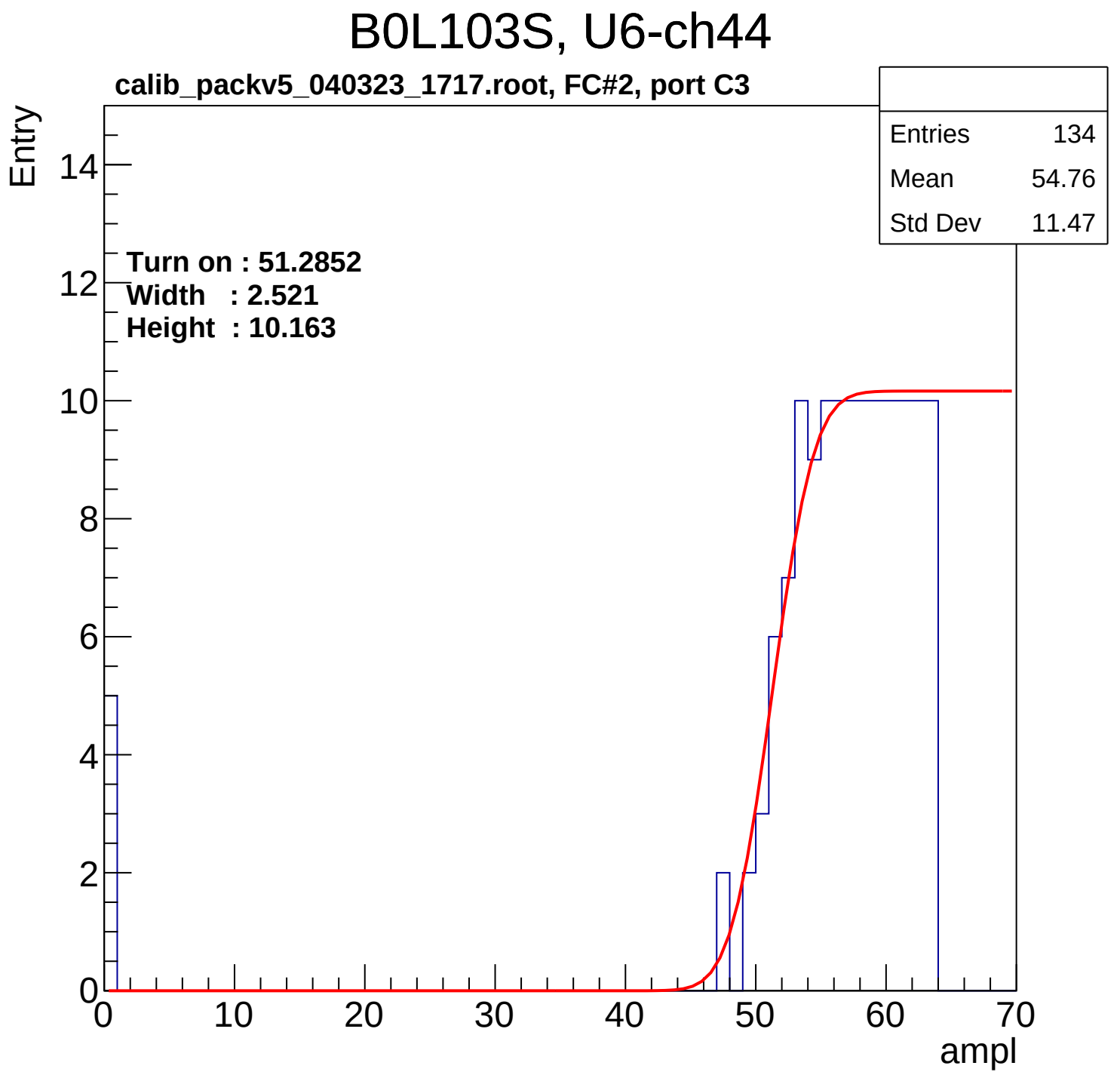
B0L103S, U6-ch44
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 54.76
Std Dev 11.47
Turn on : 51.2852
Width : 2.521
Height : 10.163
Entry
ampl
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10
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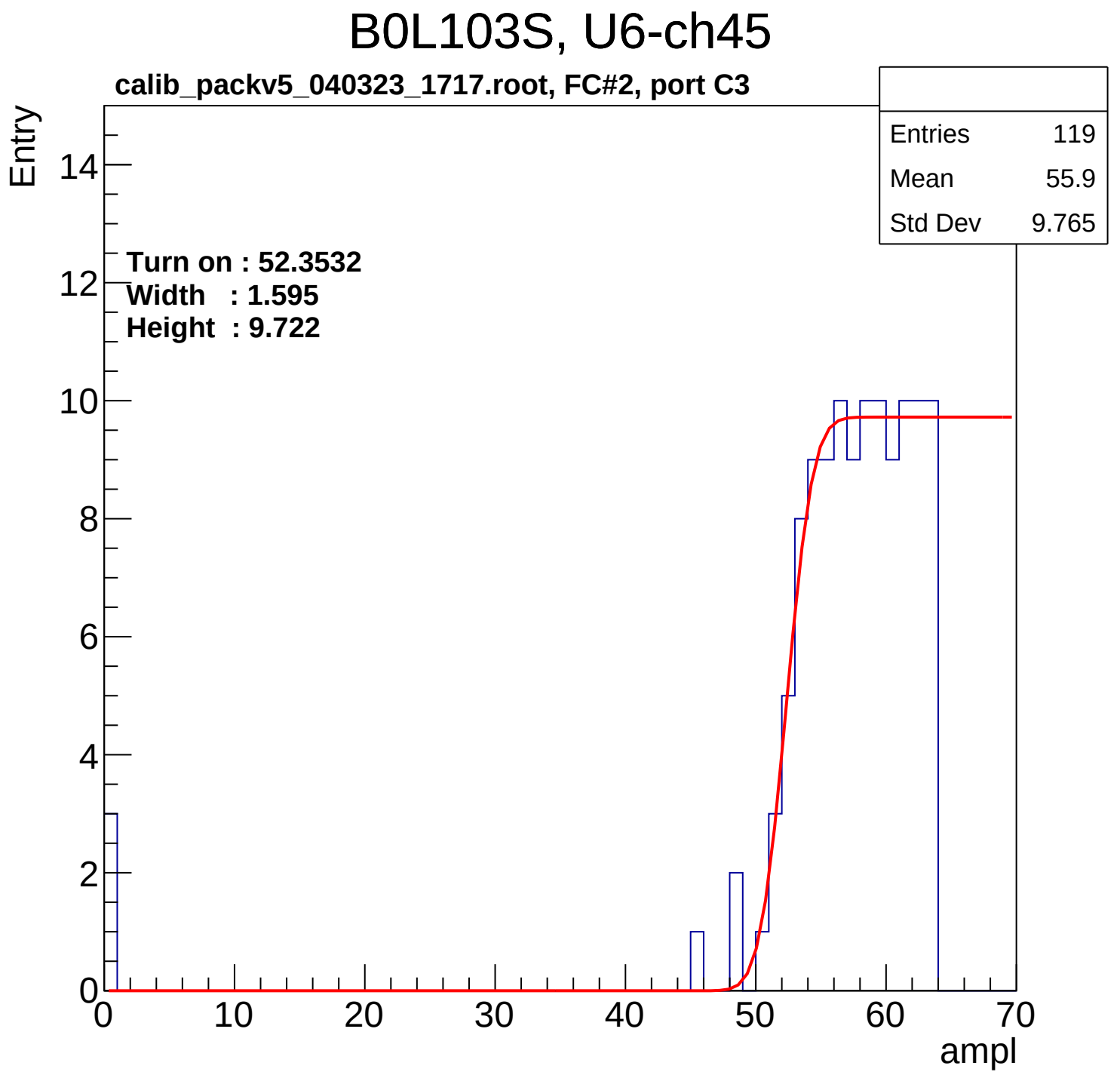
B0L103S, U6-ch45
calib_packv5_040323_1717.root, FC#2, port C3
Entries 119
Mean 55.9
Std Dev 9.765
Turn on : 52.3532
Width : 1.595
Height : 9.722
Entry
ampl
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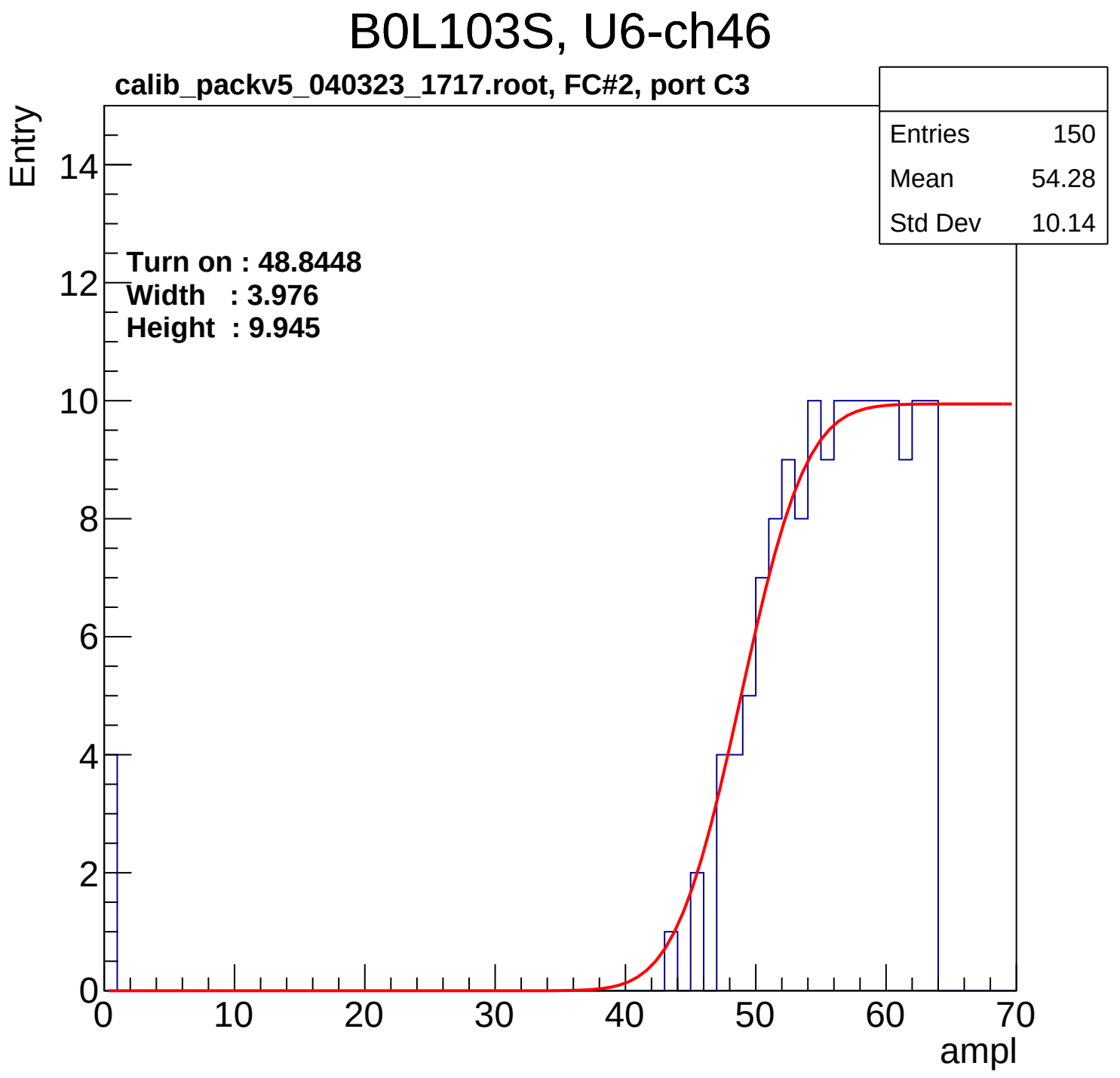
B0L103S, U6-ch46
calib_packv5_040323_1717.root, FC#2, port C3
Entries 150
Mean 54.28
Std Dev 10.14
Turn on : 48.8448
Width : 3.976
Height : 9.945
Entry
ampl
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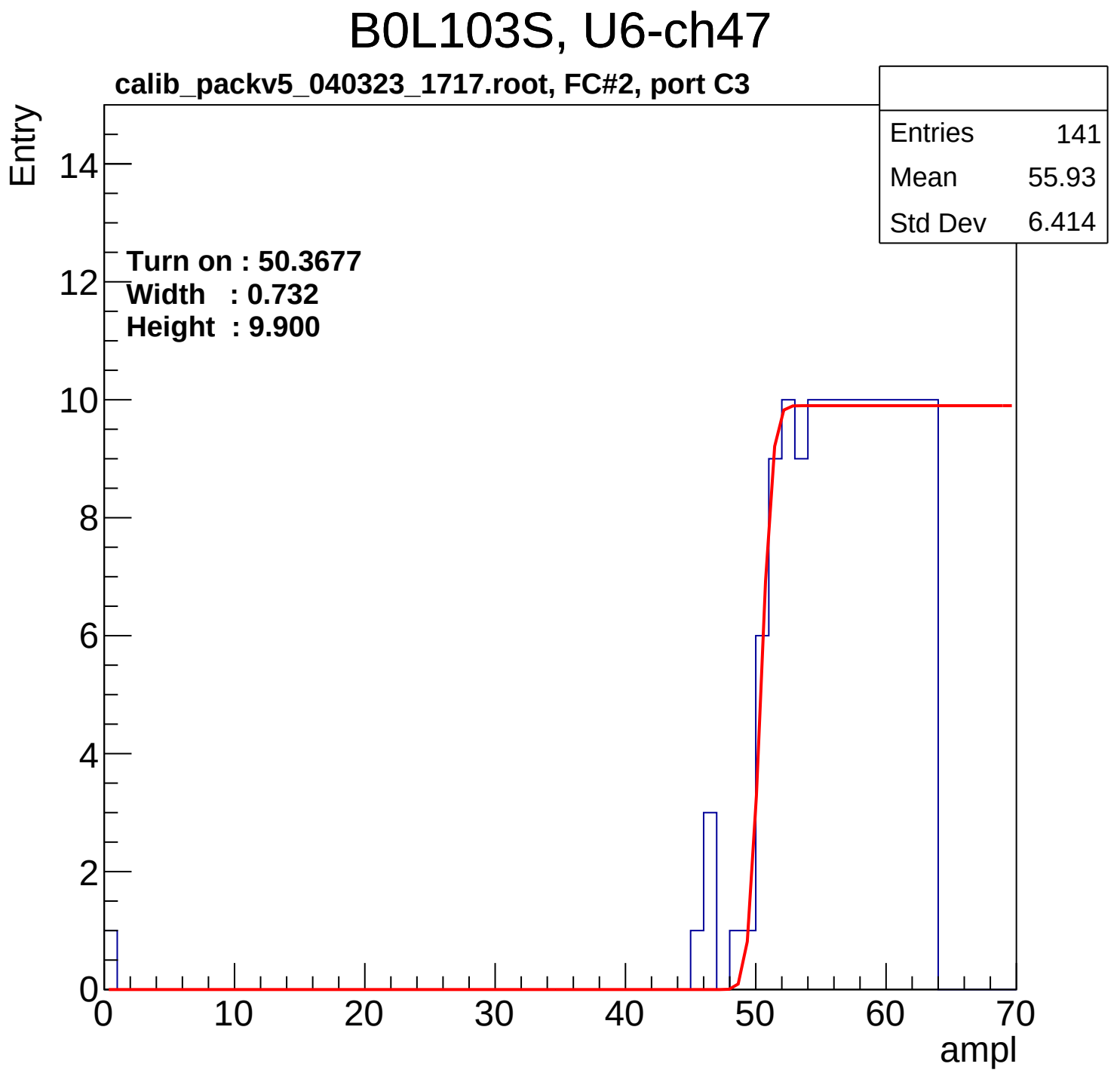
B0L103S, U6-ch47
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 55.93
Std Dev 6.414
Turn on : 50.3677
Width : 0.732
Height : 9.900
Entry
ampl
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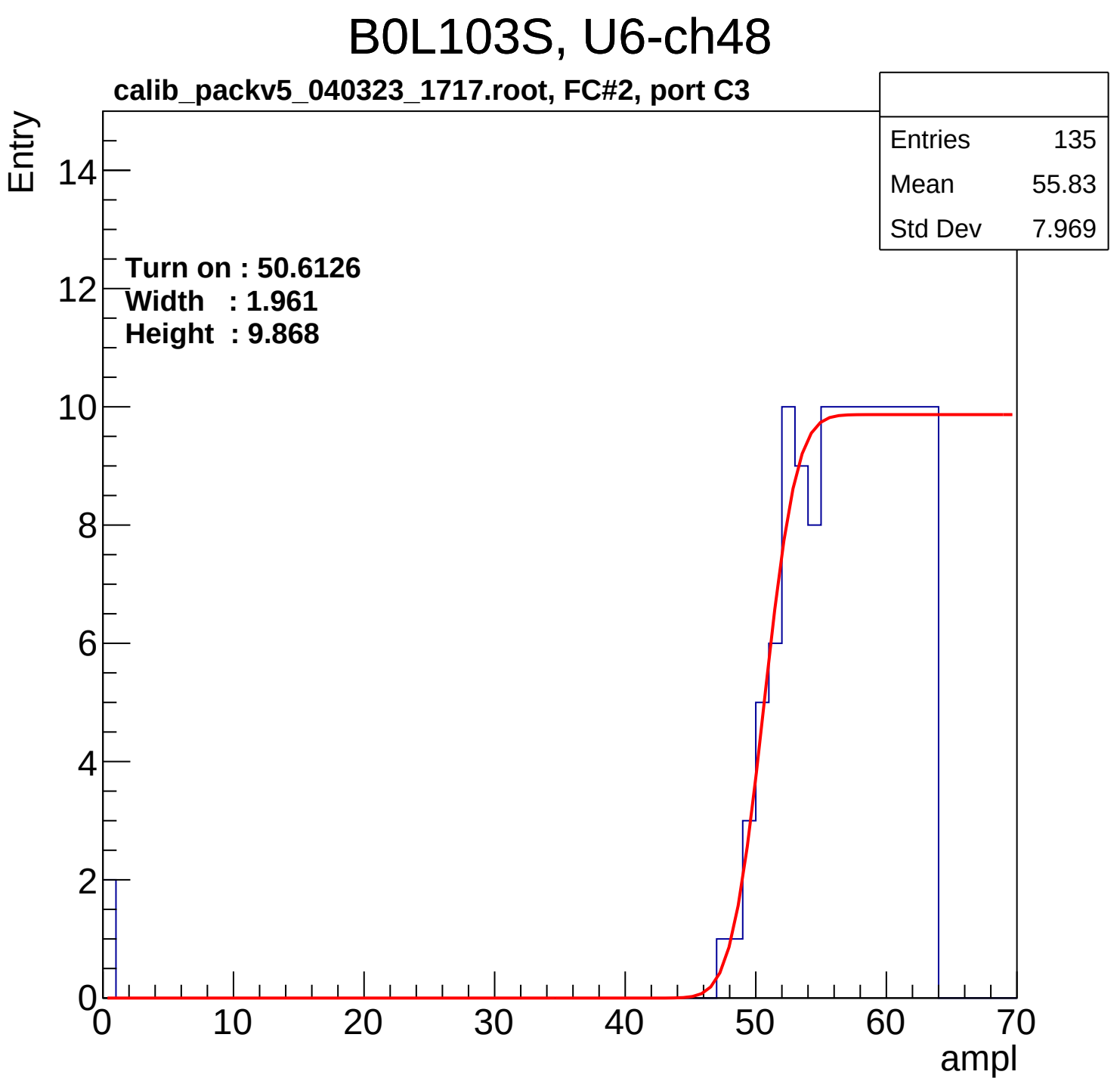
B0L103S, U6-ch48
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 55.83
Std Dev 7.969
Turn on : 50.6126
Width : 1.961
Height : 9.868
Entry
ampl
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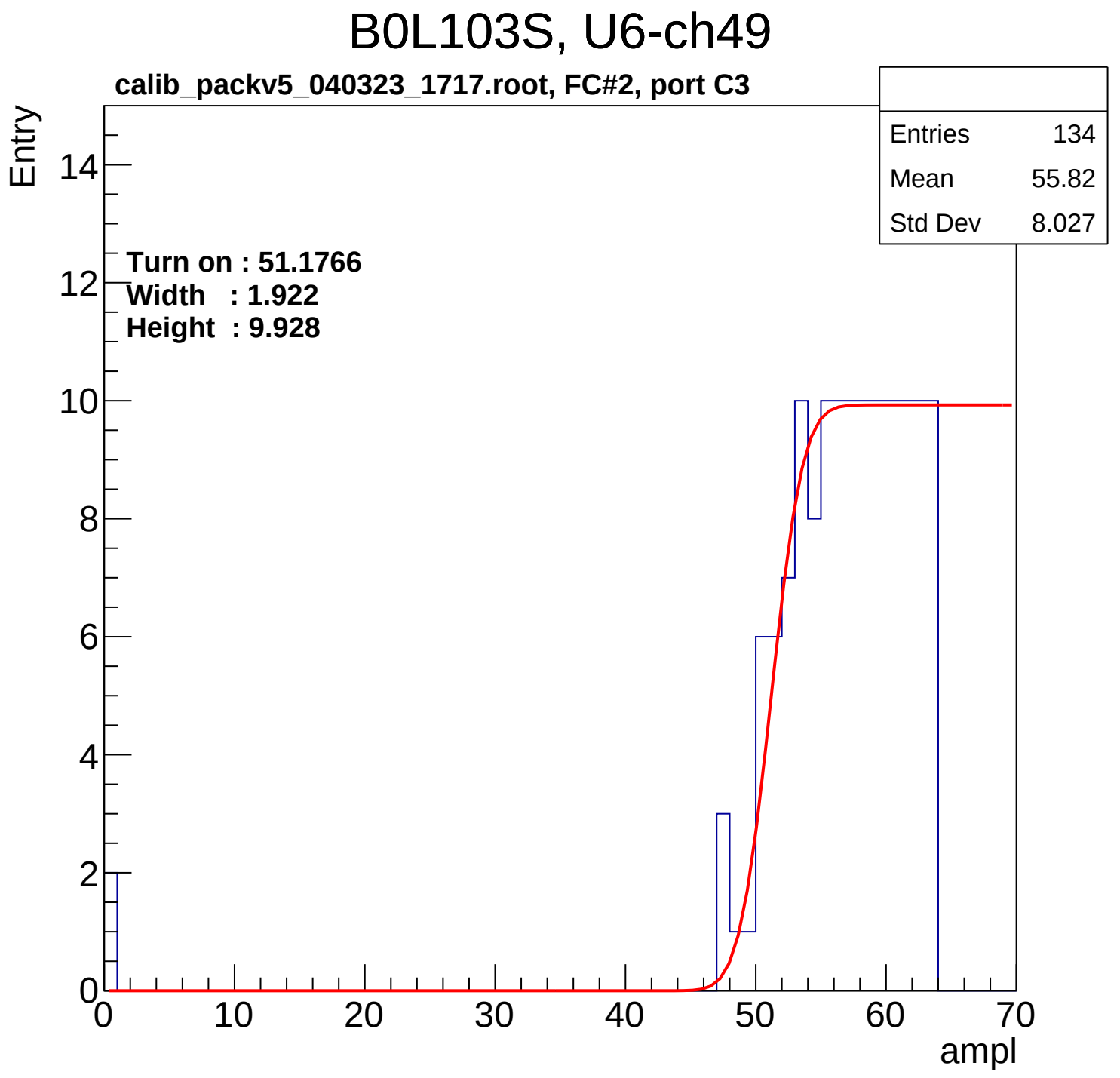
B0L103S, U6-ch49
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 55.82
Std Dev 8.027
Turn on : 51.1766
Width : 1.922
Height : 9.928
Entry
ampl
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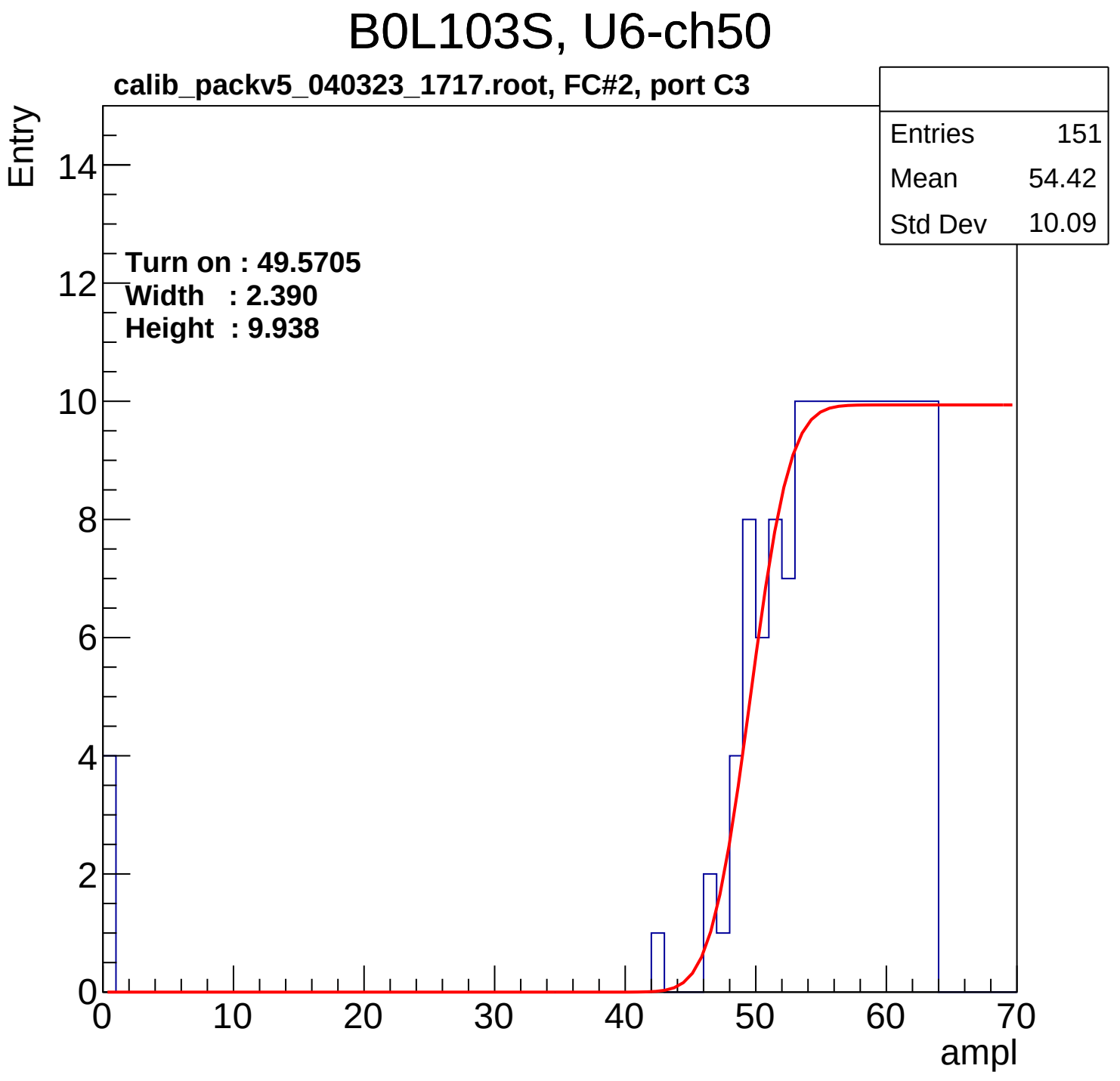
B0L103S, U6-ch50
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 54.42
Std Dev 10.09
Turn on : 49.5705
Width : 2.390
Height : 9.938
Entry
ampl
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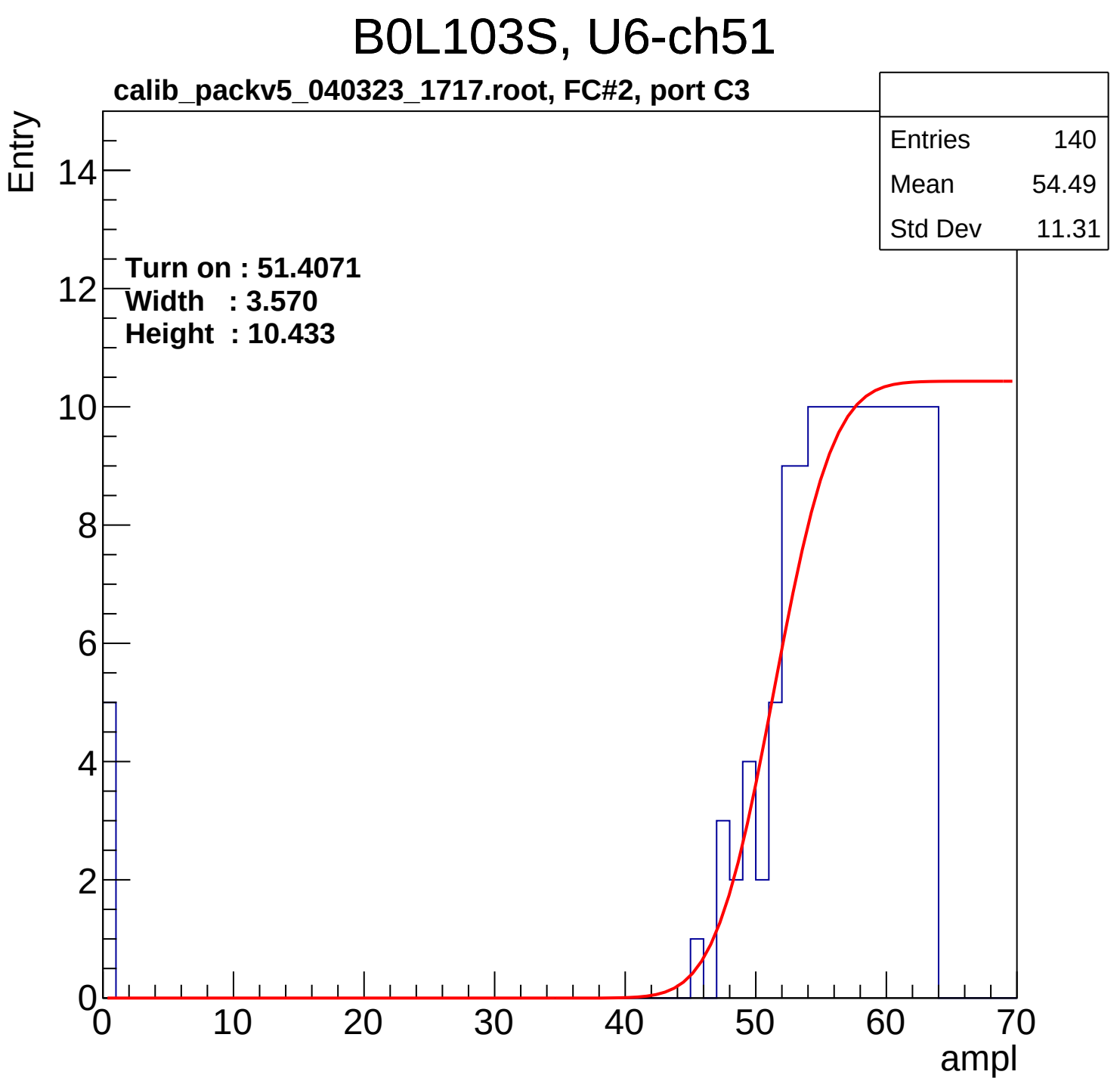
B0L103S, U6-ch51
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 54.49
Std Dev 11.31
Turn on : 51.4071
Width : 3.570
Height : 10.433
Entry
ampl
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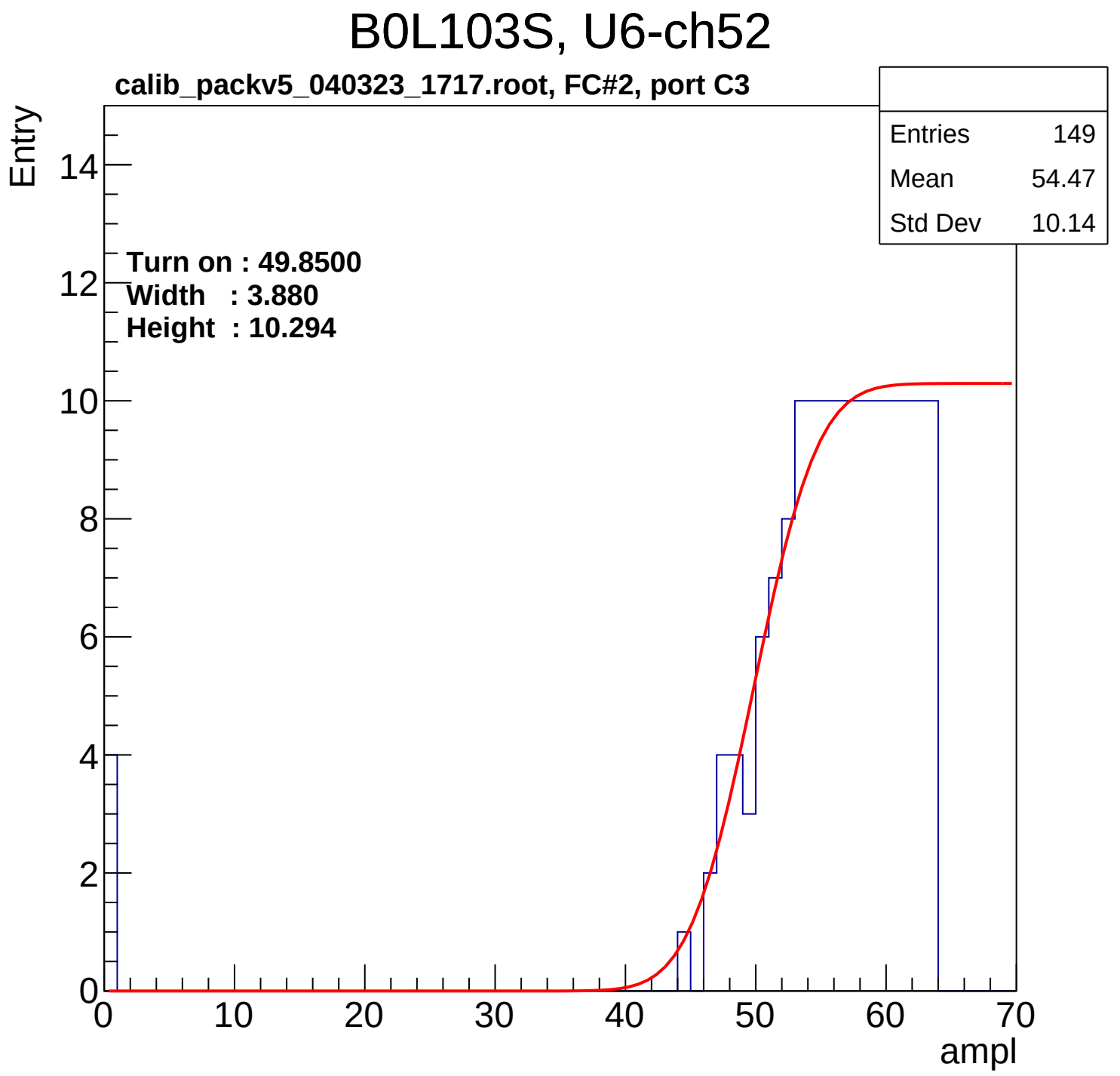
B0L103S, U6-ch52
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 54.47
Std Dev 10.14
Turn on : 49.8500
Width : 3.880
Height : 10.294
Entry
ampl
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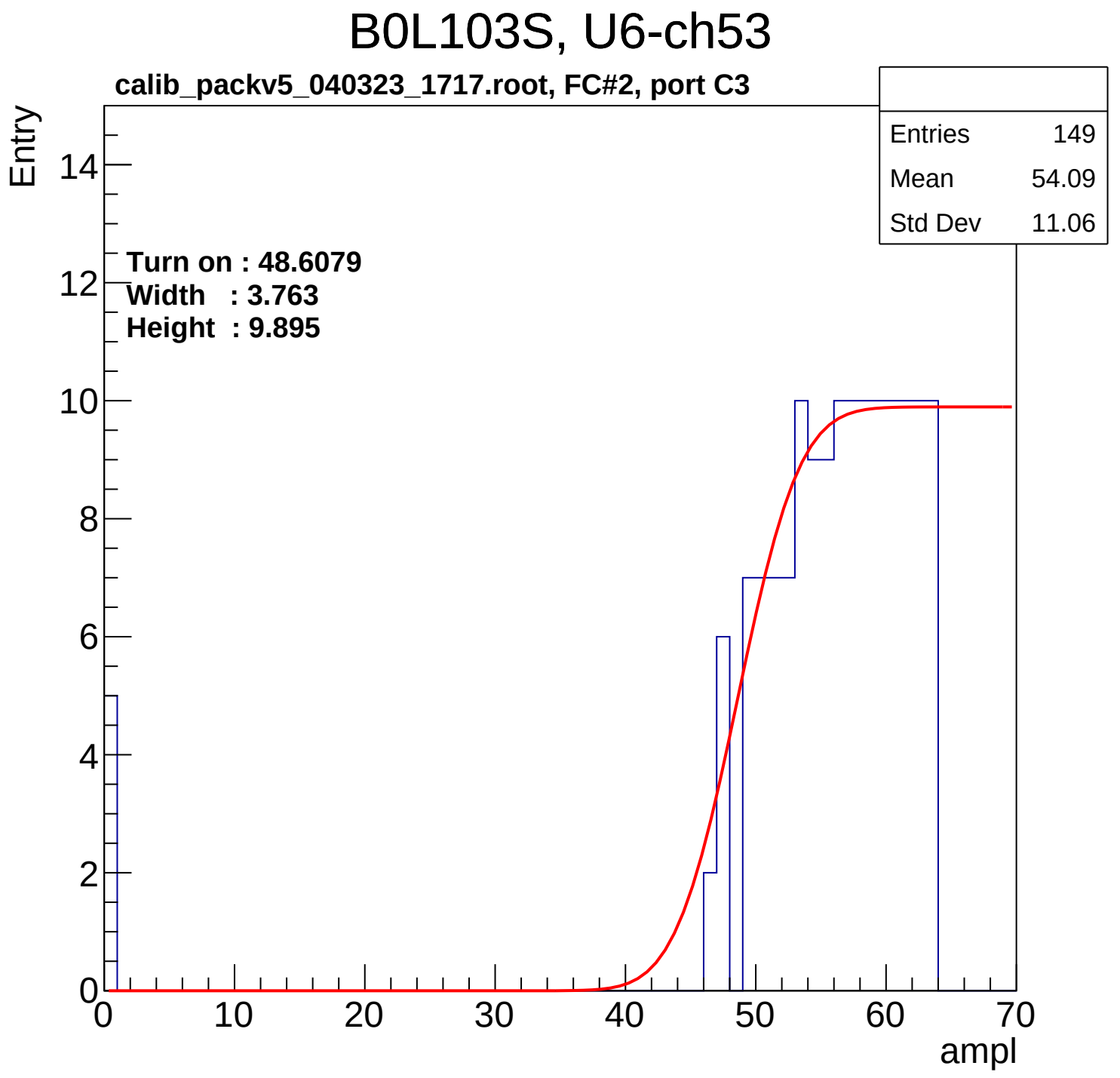
B0L103S, U6-ch53
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 54.09
Std Dev 11.06
Turn on : 48.6079
Width : 3.763
Height : 9.895
Entry
ampl
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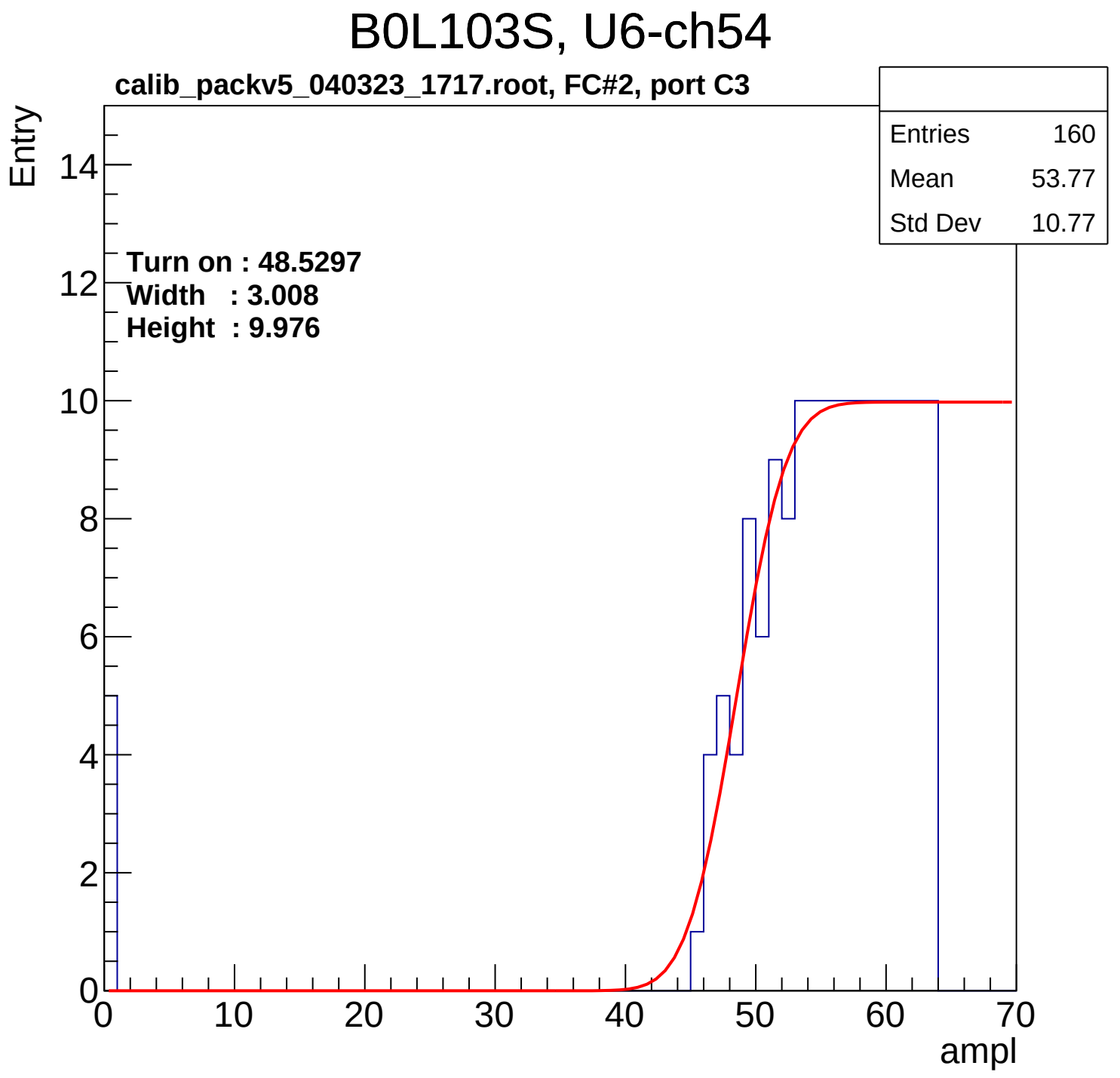
B0L103S, U6-ch54
calib_packv5_040323_1717.root, FC#2, port C3
Entries 160
Mean 53.77
Std Dev 10.77
Turn on : 48.5297
Width : 3.008
Height : 9.976
Entry
ampl
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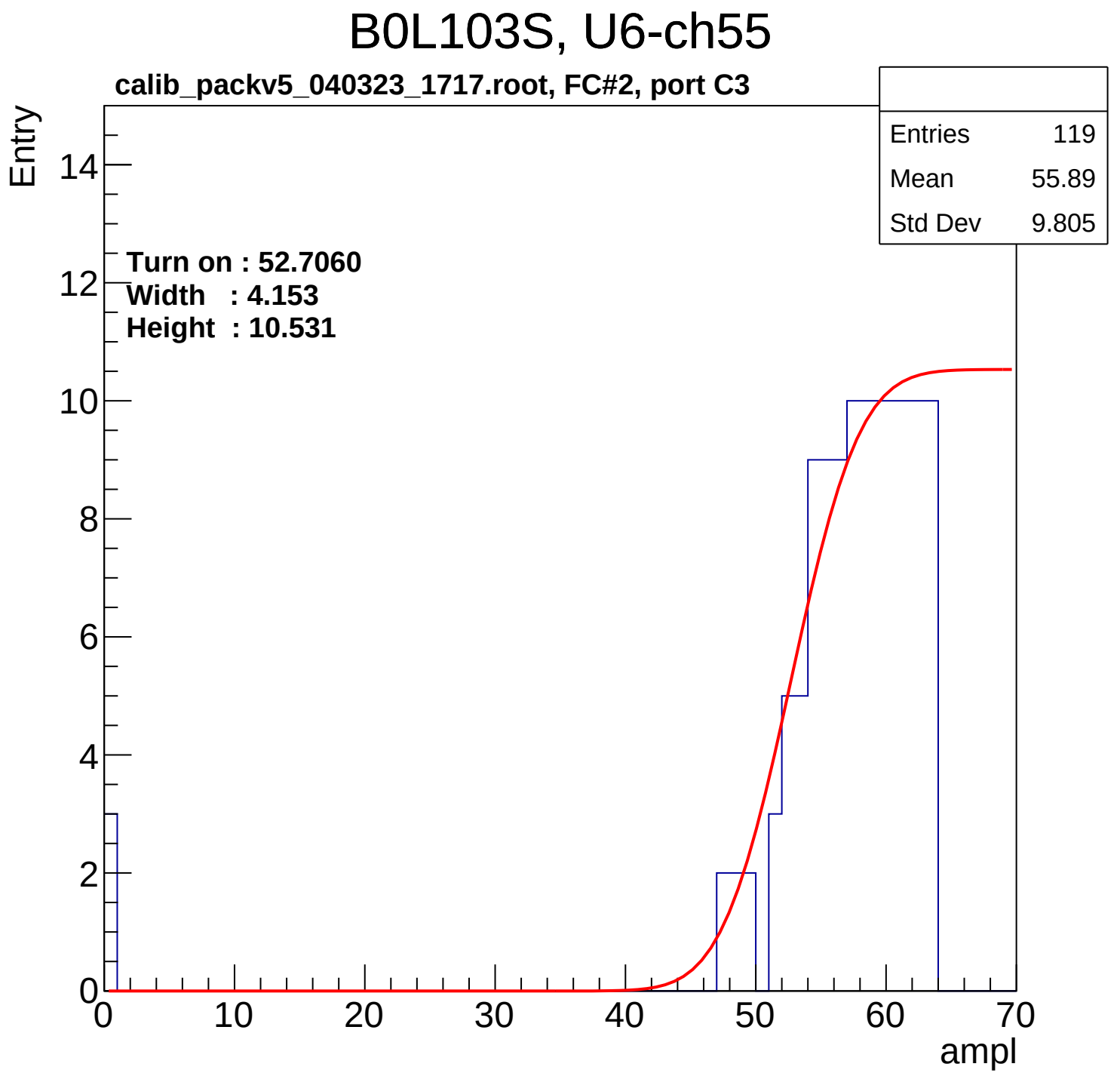
B0L103S, U6-ch55
calib_packv5_040323_1717.root, FC#2, port C3
Entries 119
Mean 55.89
Std Dev 9.805
Turn on : 52.7060
Width : 4.153
Height : 10.531
Entry
ampl
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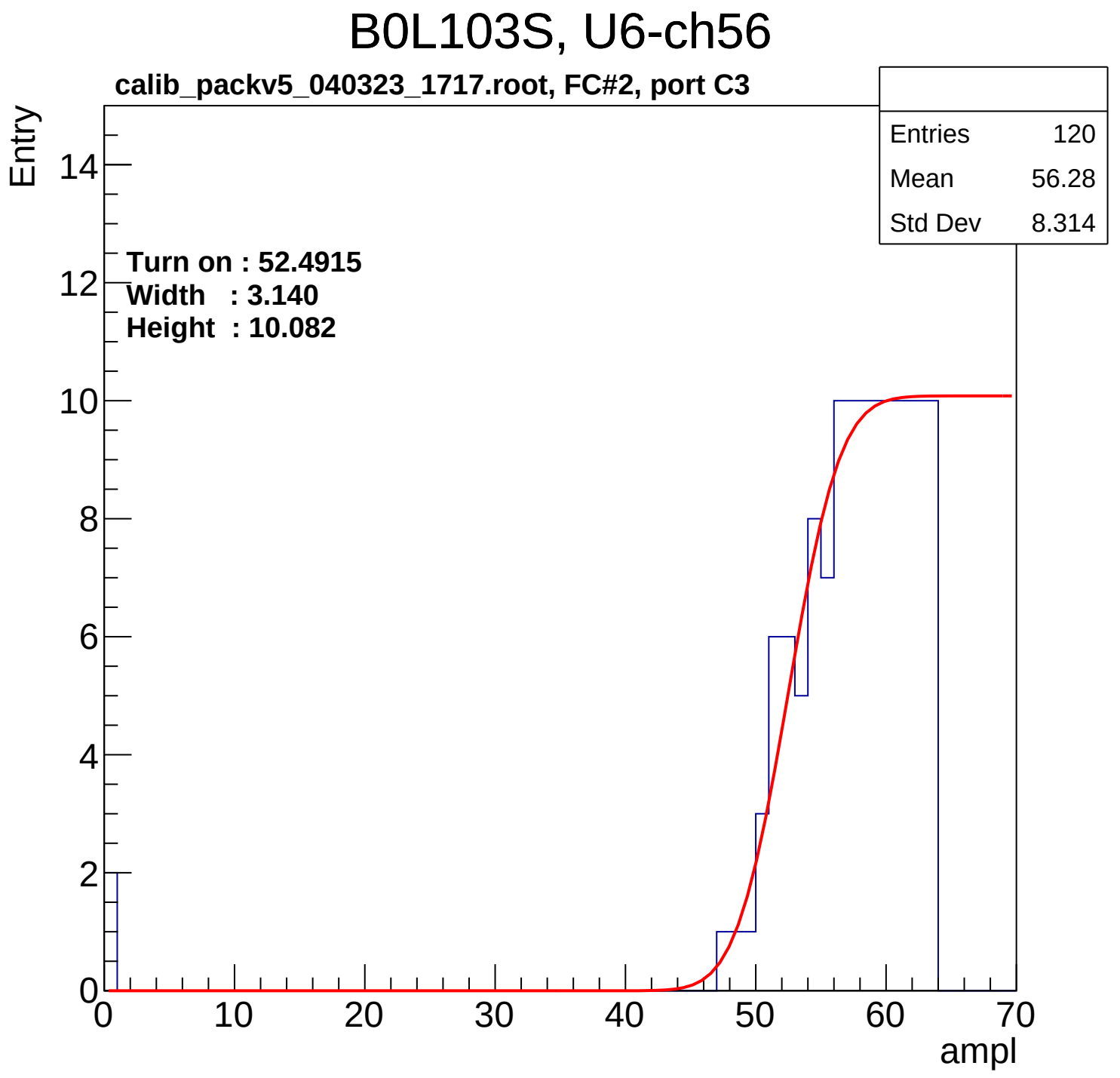
B0L103S, U6-ch56
calib_packv5_040323_1717.root, FC#2, port C3
Entries 120
Mean 56.28
Std Dev 8.314
Turn on : 52.4915
Width : 3.140
Height : 10.082
Entry
ampl
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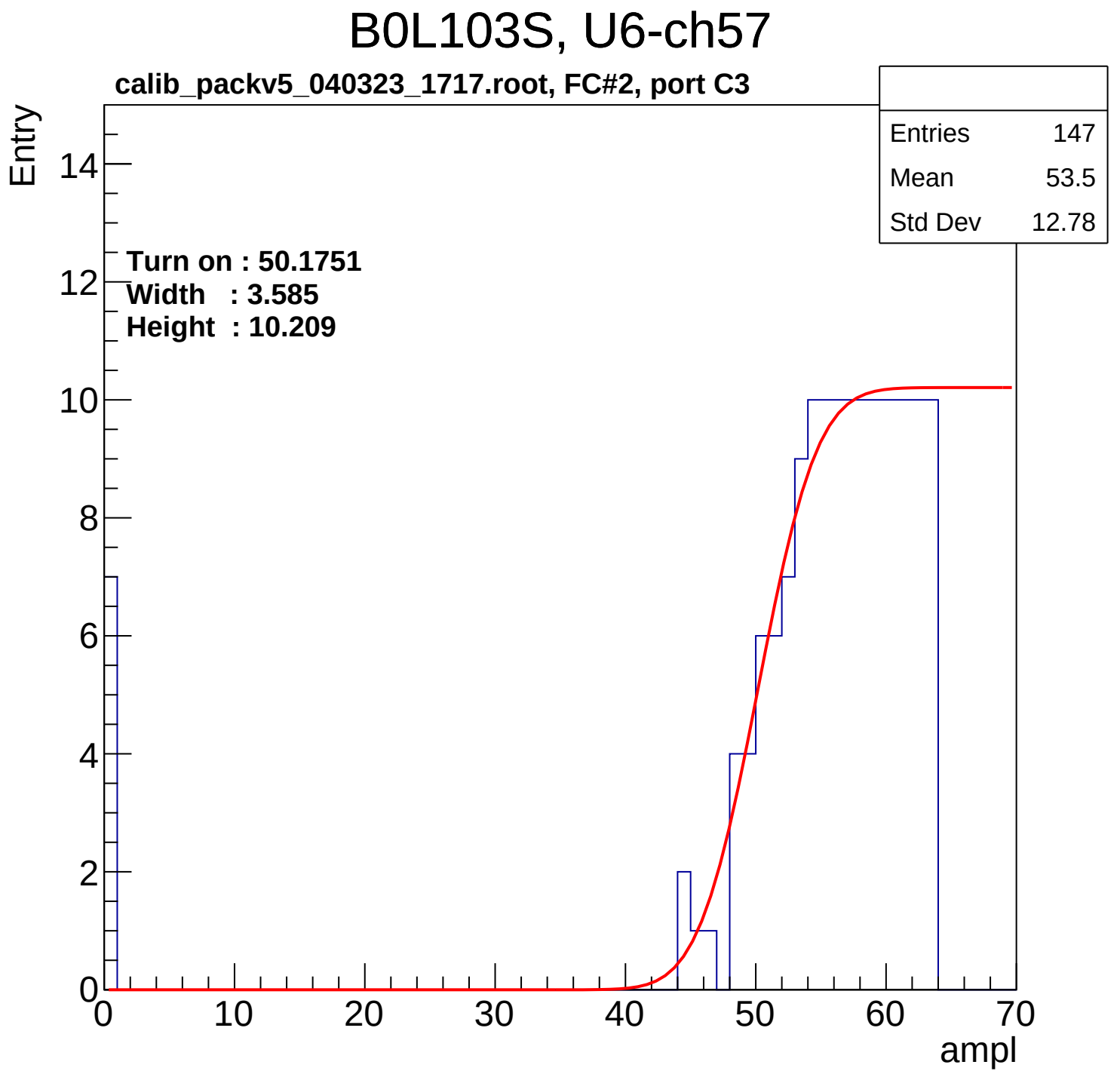
B0L103S, U6-ch57
calib_packv5_040323_1717.root, FC#2, port C3
Entries 147
Mean 53.5
Std Dev 12.78
Turn on : 50.1751
Width : 3.585
Height : 10.209
Entry
ampl
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2
4
6
8
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12
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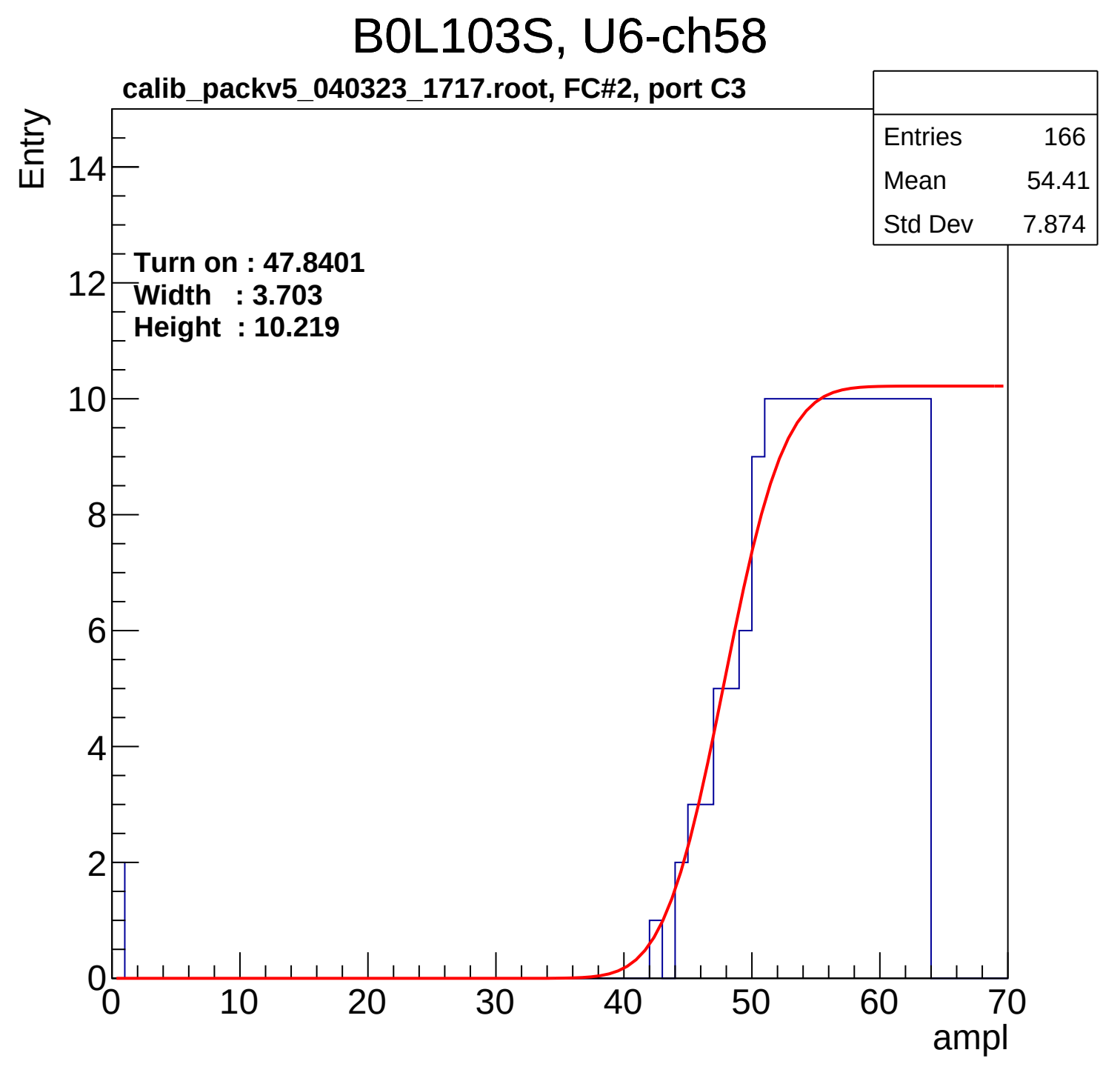
B0L103S, U6-ch58
calib_packv5_040323_1717.root, FC#2, port C3
Entries 166
Mean 54.41
Std Dev 7.874
Turn on : 47.8401
Width : 3.703
Height : 10.219
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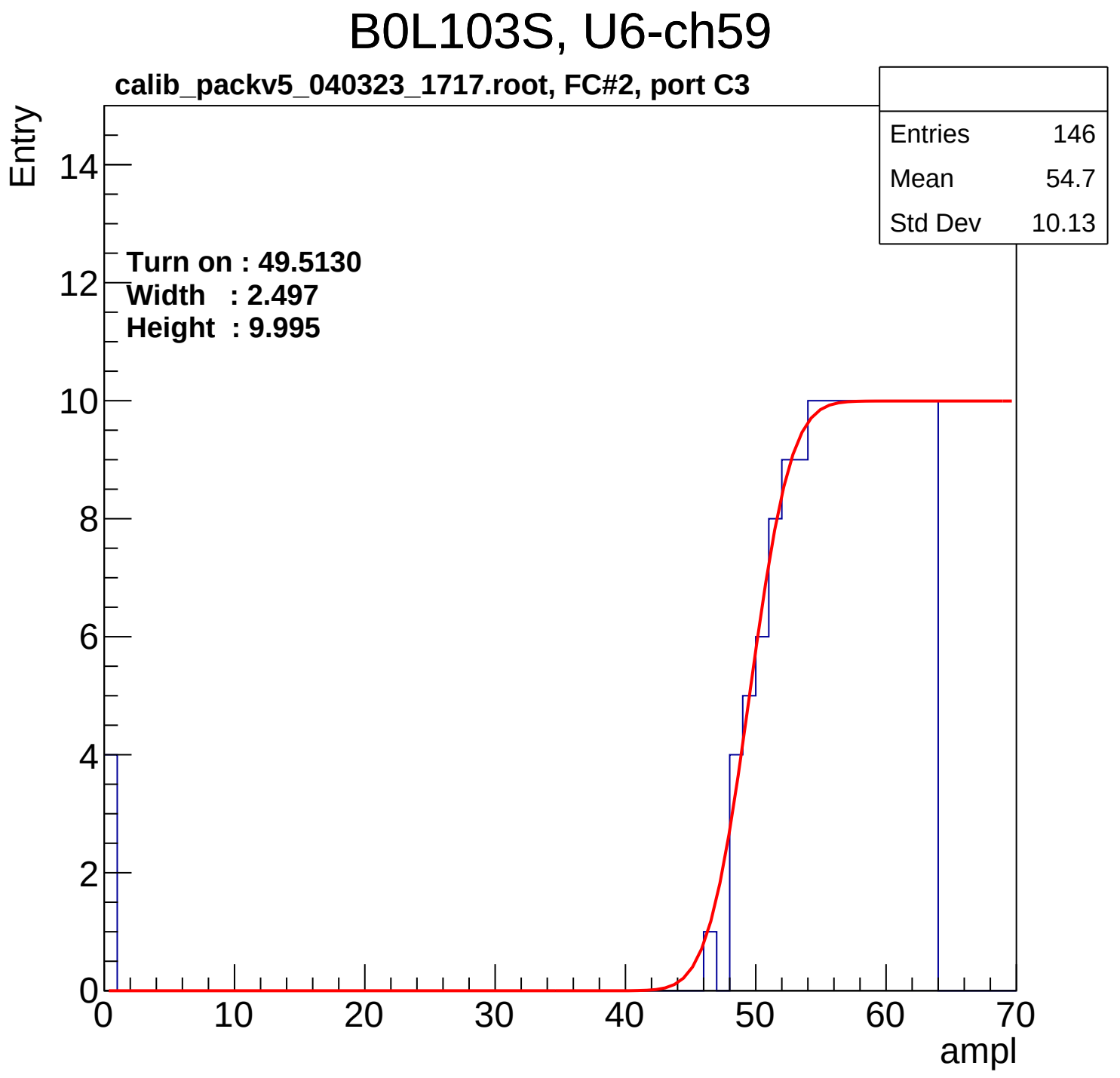
B0L103S, U6-ch59
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 54.7
Std Dev 10.13
Turn on : 49.5130
Width : 2.497
Height : 9.995
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ampl
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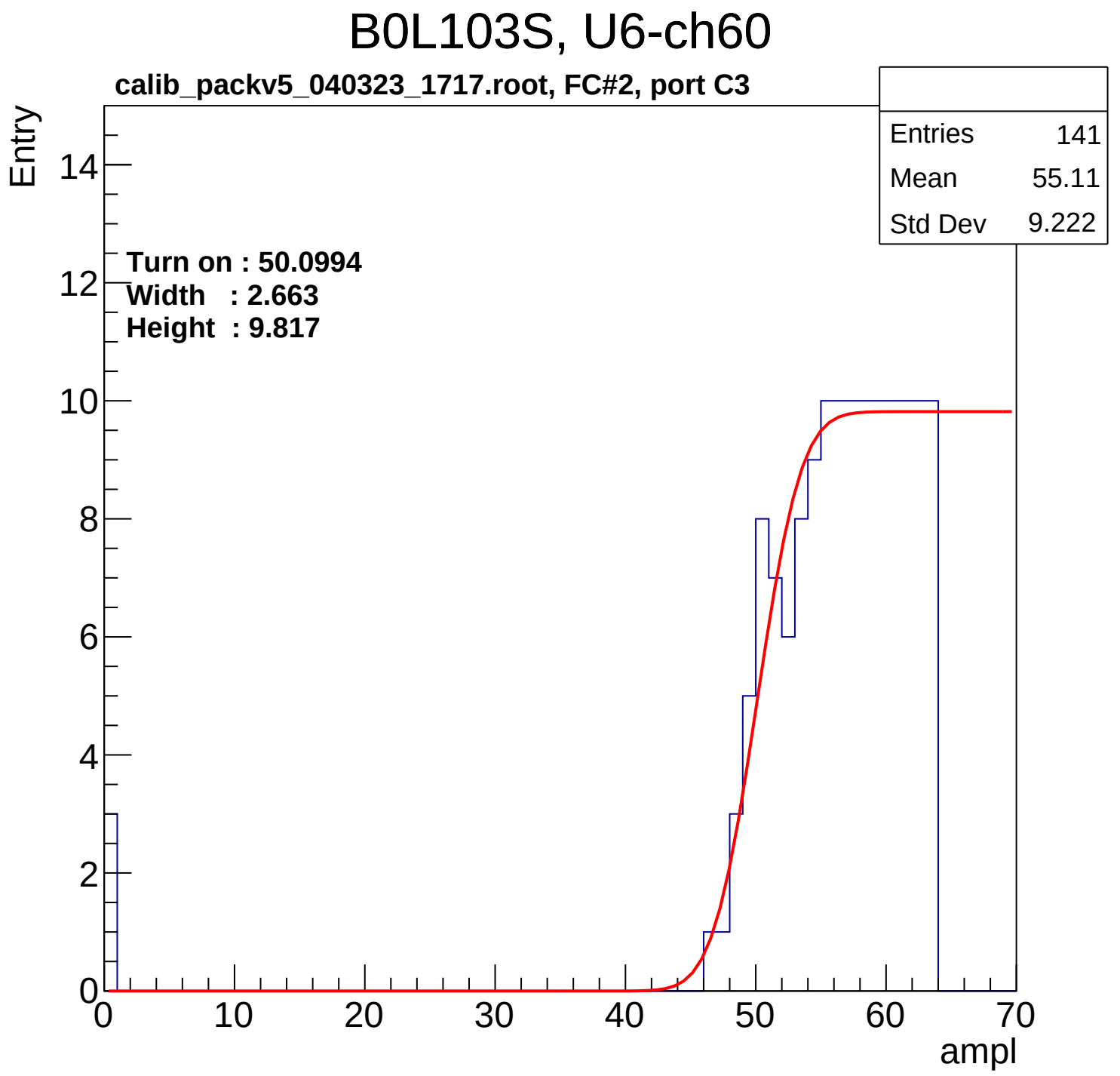
B0L103S, U6-ch60
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 55.11
Std Dev 9.222
Turn on : 50.0994
Width : 2.663
Height : 9.817
Entry
ampl
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8
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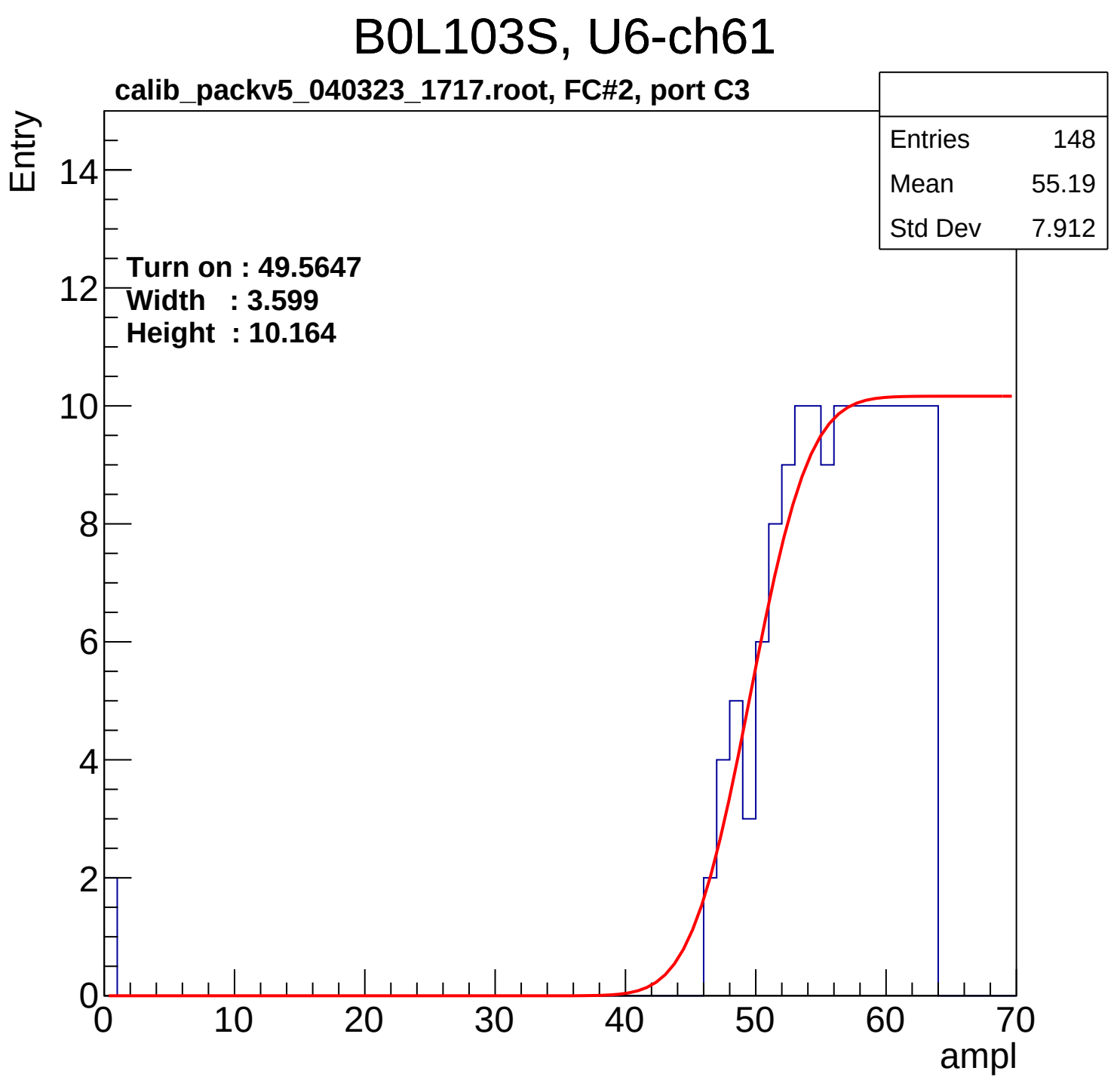
B0L103S, U6-ch61
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 55.19
Std Dev 7.912
Turn on : 49.5647
Width : 3.599
Height : 10.164
Entry
ampl
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6
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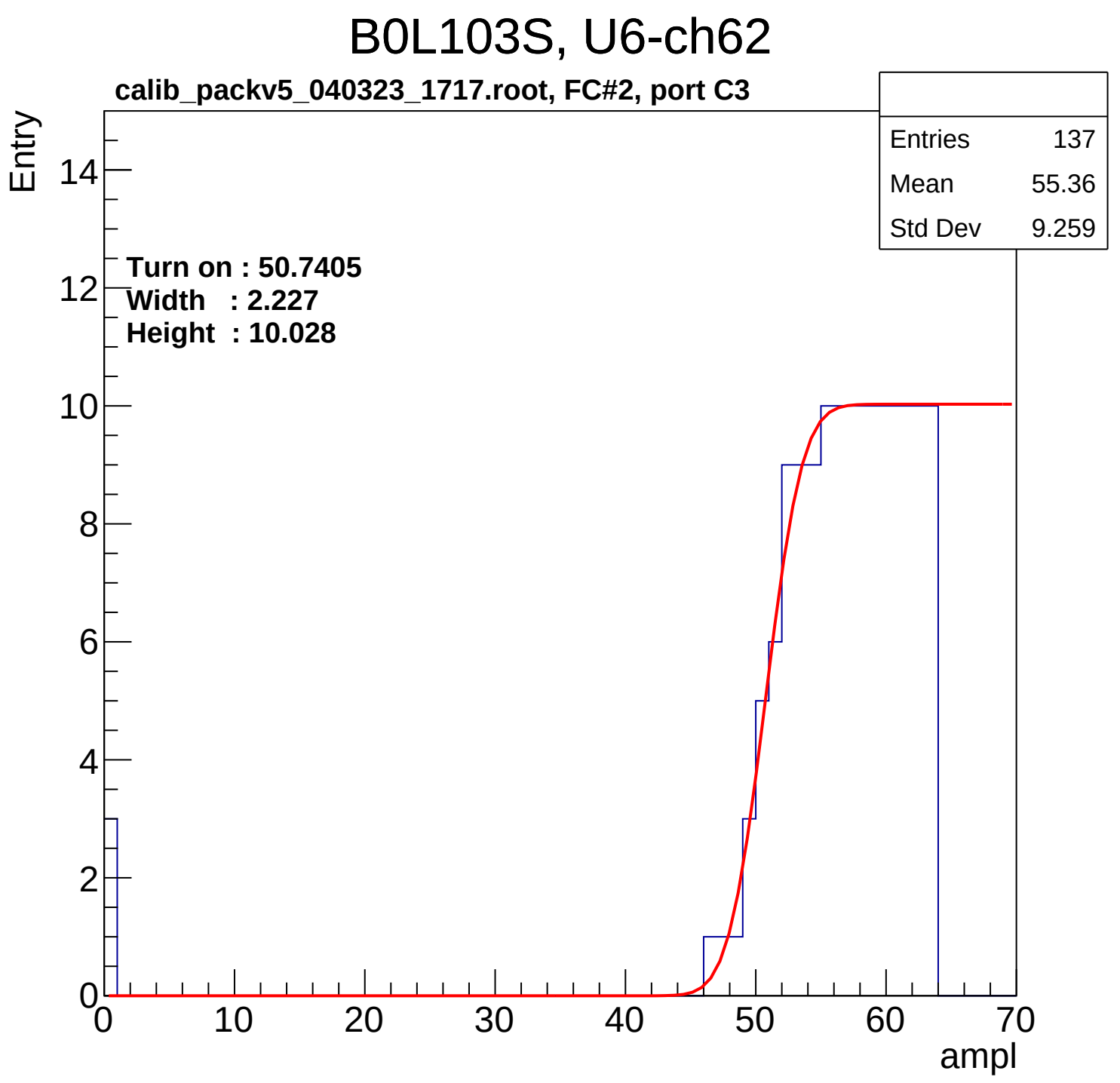
B0L103S, U6-ch62
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 55.36
Std Dev 9.259
Turn on : 50.7405
Width : 2.227
Height : 10.028
Entry
ampl
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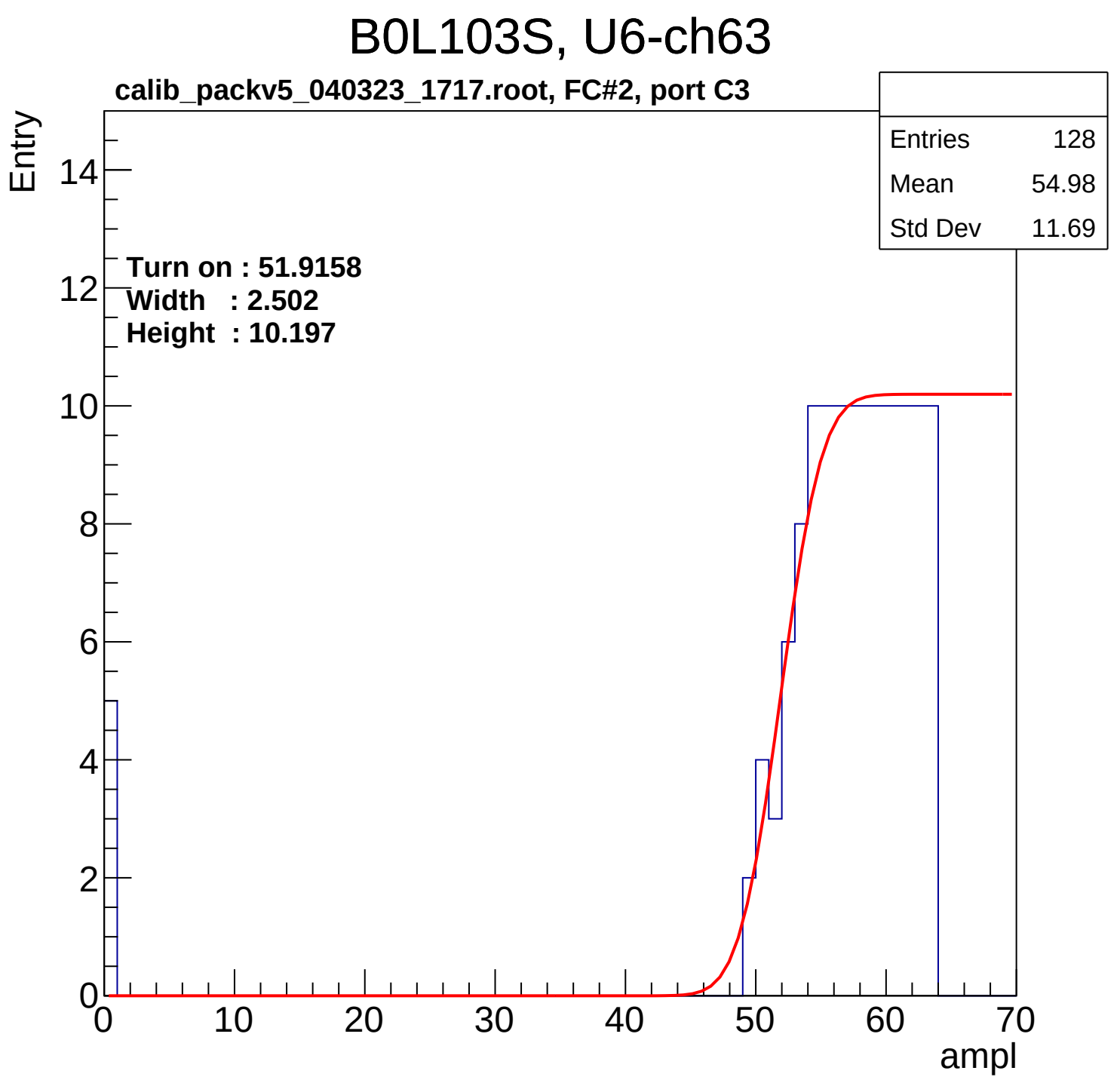
B0L103S, U6-ch63
calib_packv5_040323_1717.root, FC#2, port C3
Entries 128
Mean 54.98
Std Dev 11.69
Turn on : 51.9158
Width : 2.502
Height : 10.197
Entry
ampl
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4
6
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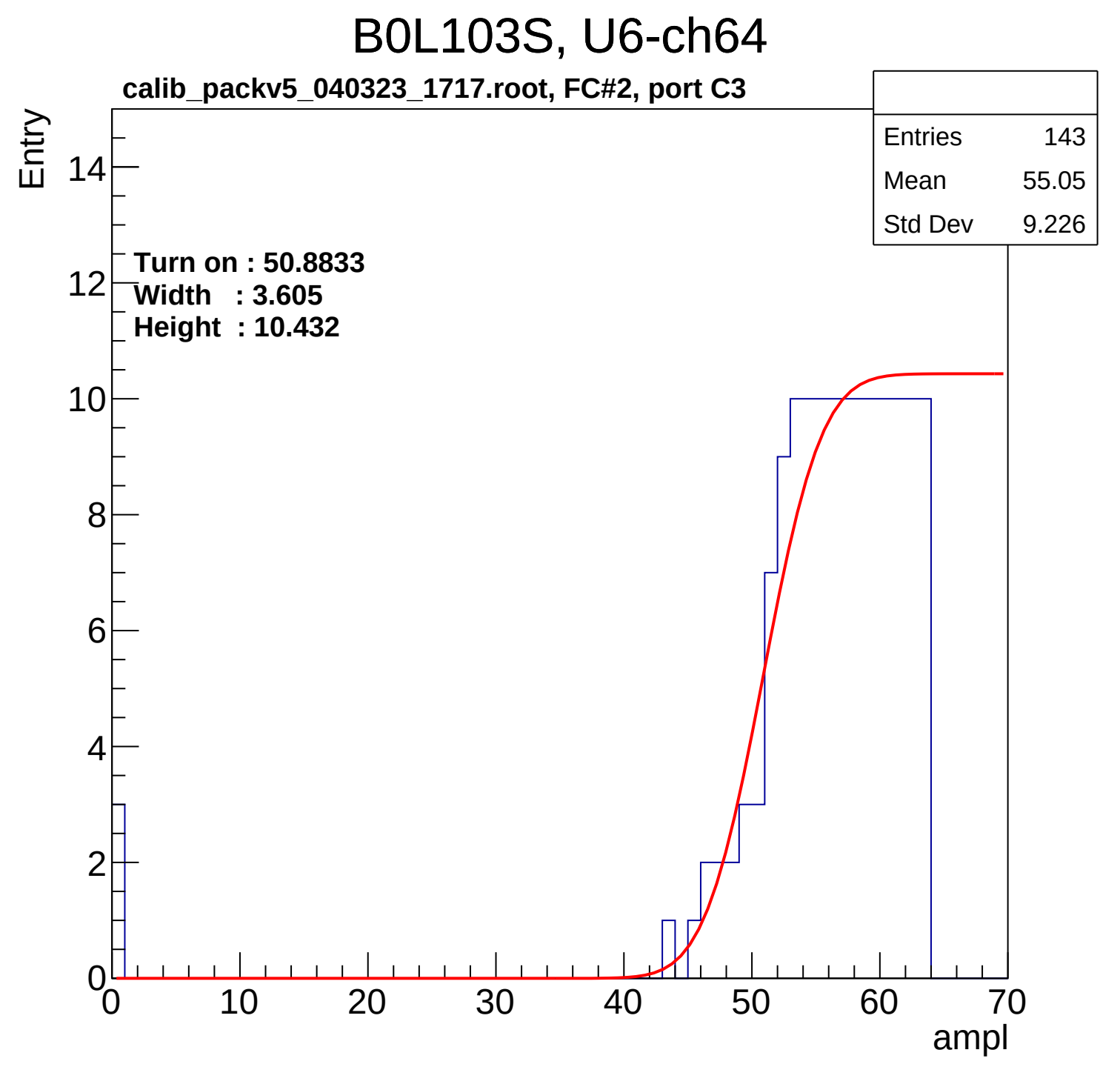
B0L103S, U6-ch64
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 55.05
Std Dev 9.226
Turn on : 50.8833
Width : 3.605
Height : 10.432
Entry
ampl
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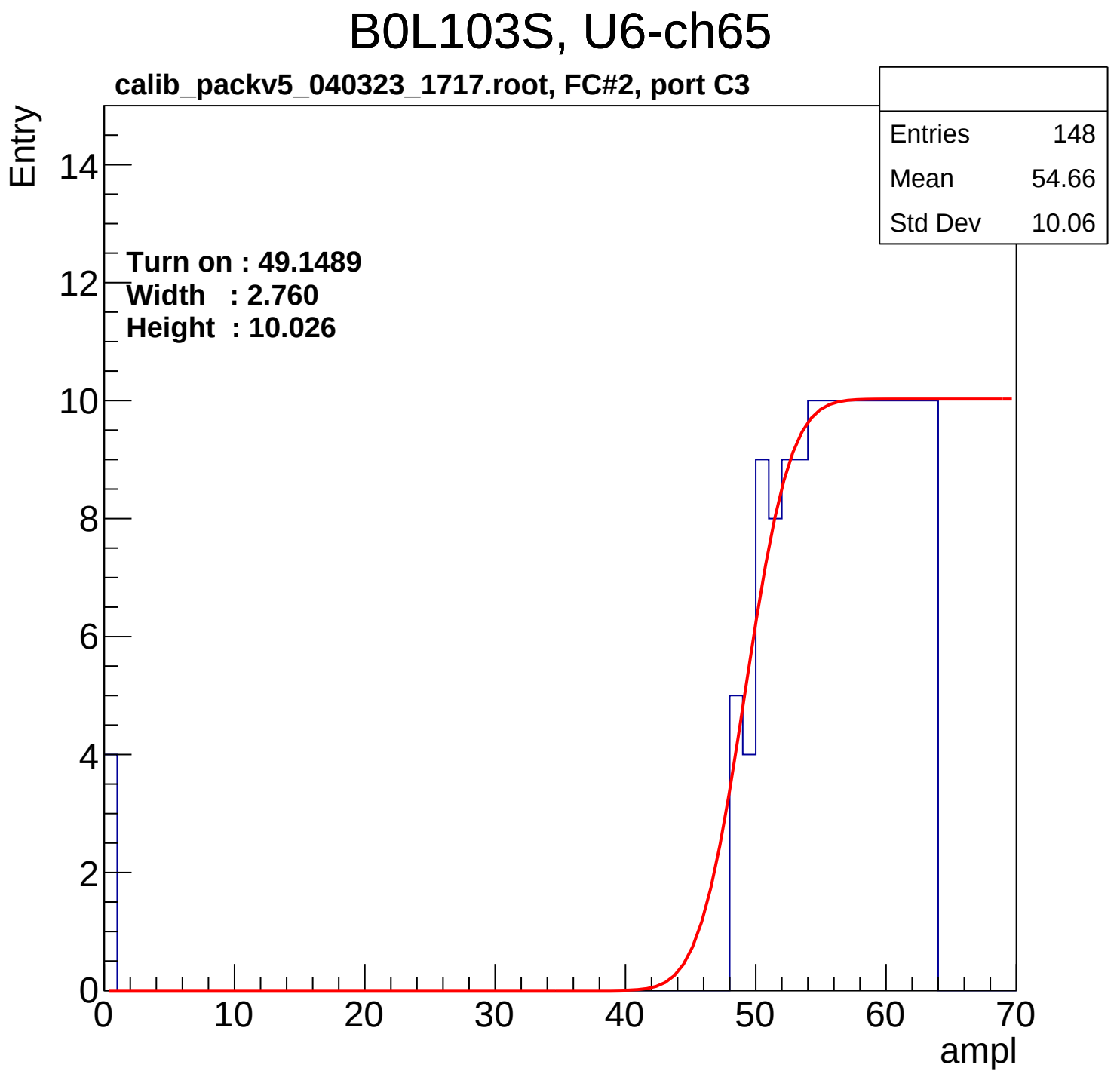
B0L103S, U6-ch65
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 54.66
Std Dev 10.06
Turn on : 49.1489
Width : 2.760
Height : 10.026
Entry
ampl
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6
8
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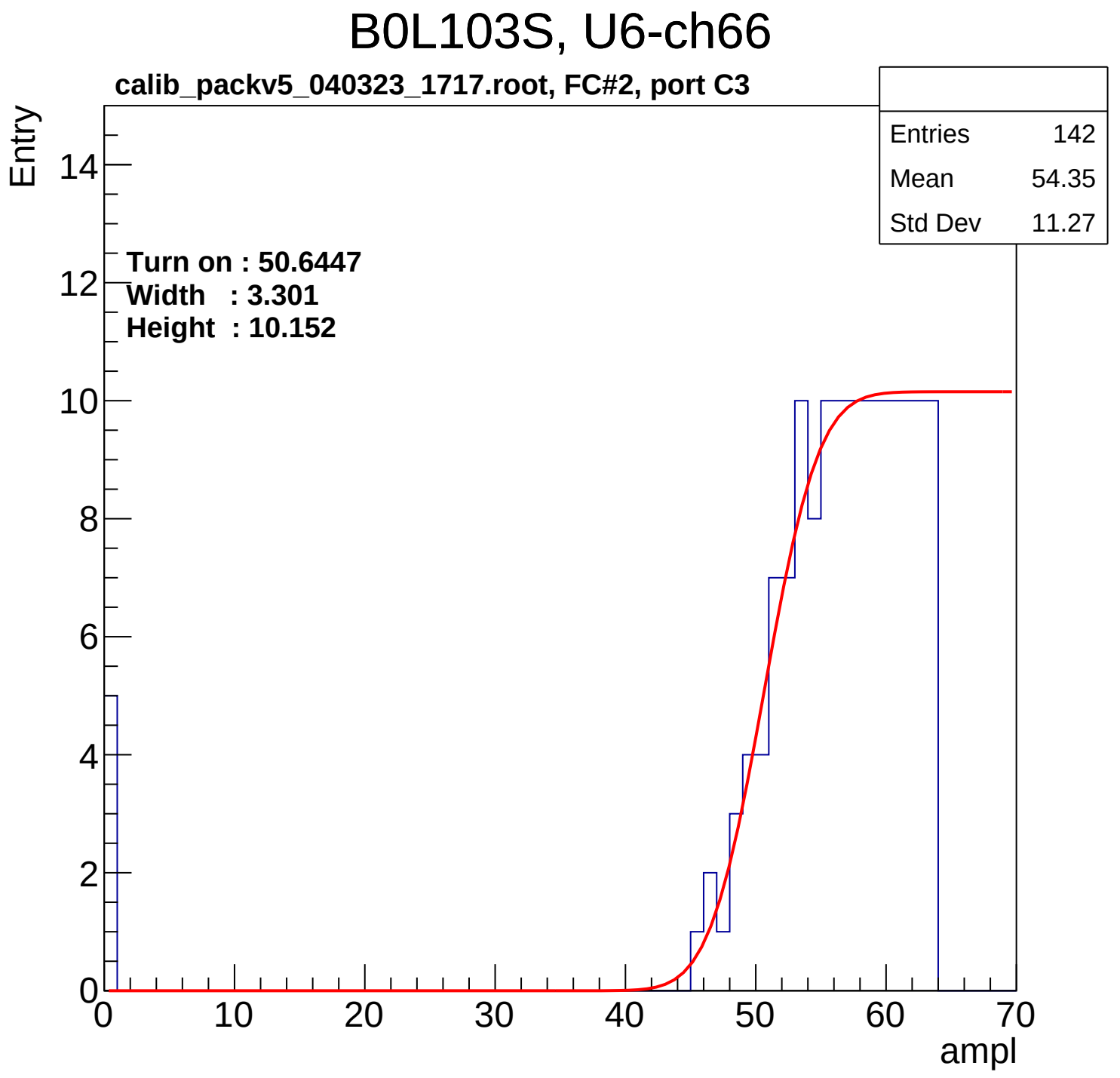
B0L103S, U6-ch66
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 54.35
Std Dev 11.27
Turn on : 50.6447
Width : 3.301
Height : 10.152
Entry
ampl
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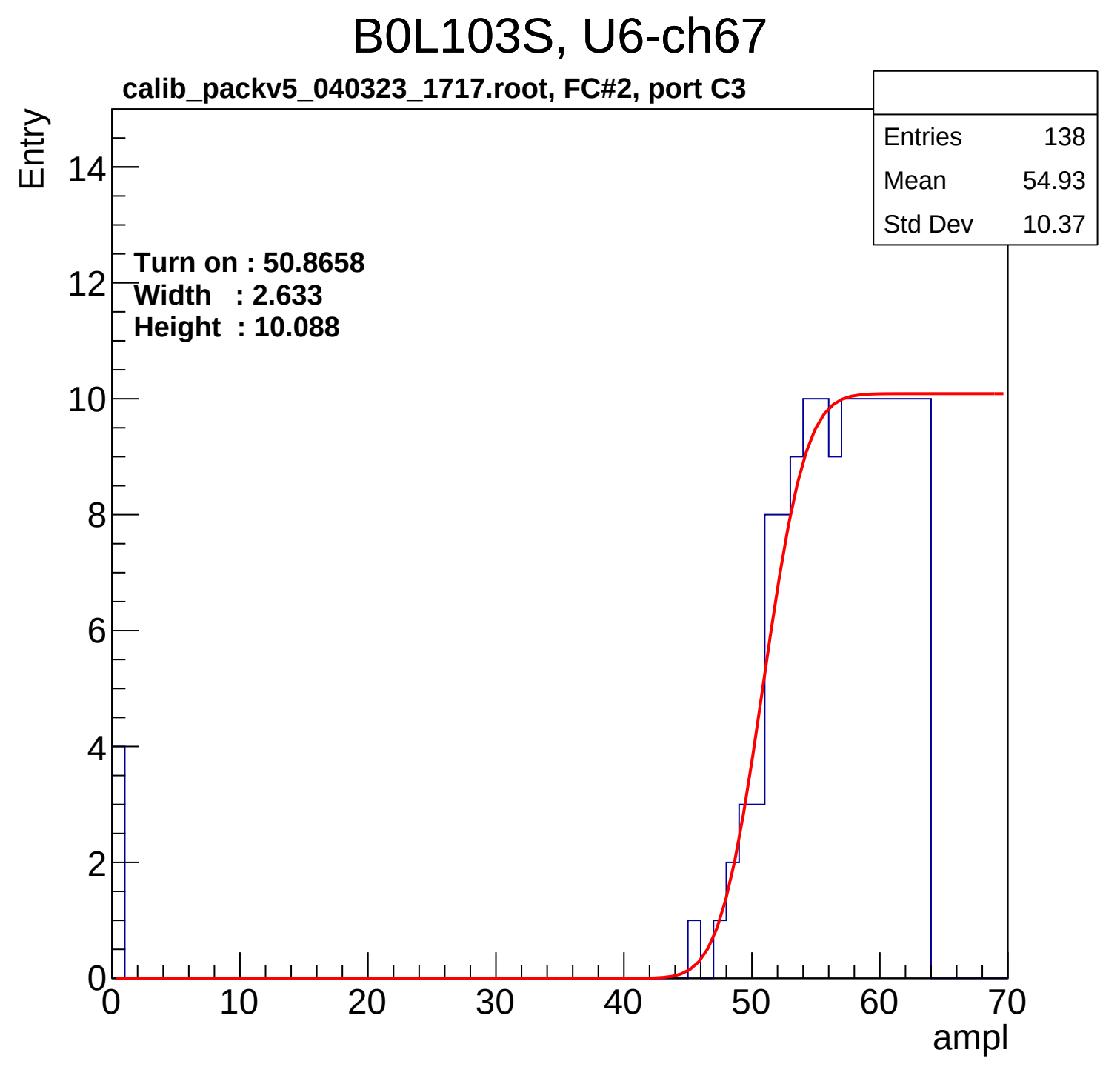
B0L103S, U6-ch67
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 54.93
Std Dev 10.37
Turn on : 50.8658
Width : 2.633
Height : 10.088
Entry
ampl
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2
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6
8
10
12
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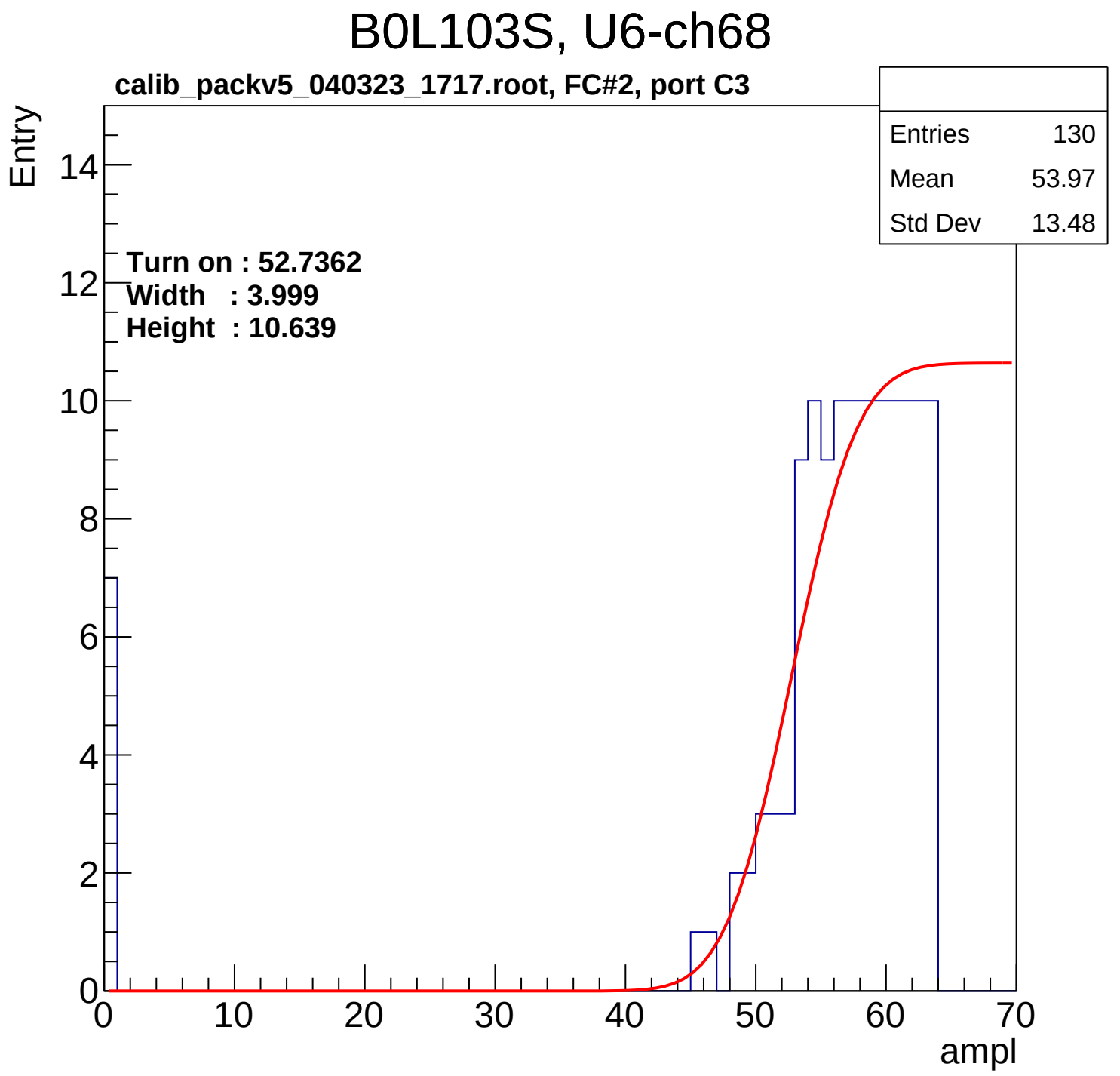
B0L103S, U6-ch68
calib_packv5_040323_1717.root, FC#2, port C3
Entries 130
Mean 53.97
Std Dev 13.48
Turn on : 52.7362
Width : 3.999
Height : 10.639
Entry
ampl
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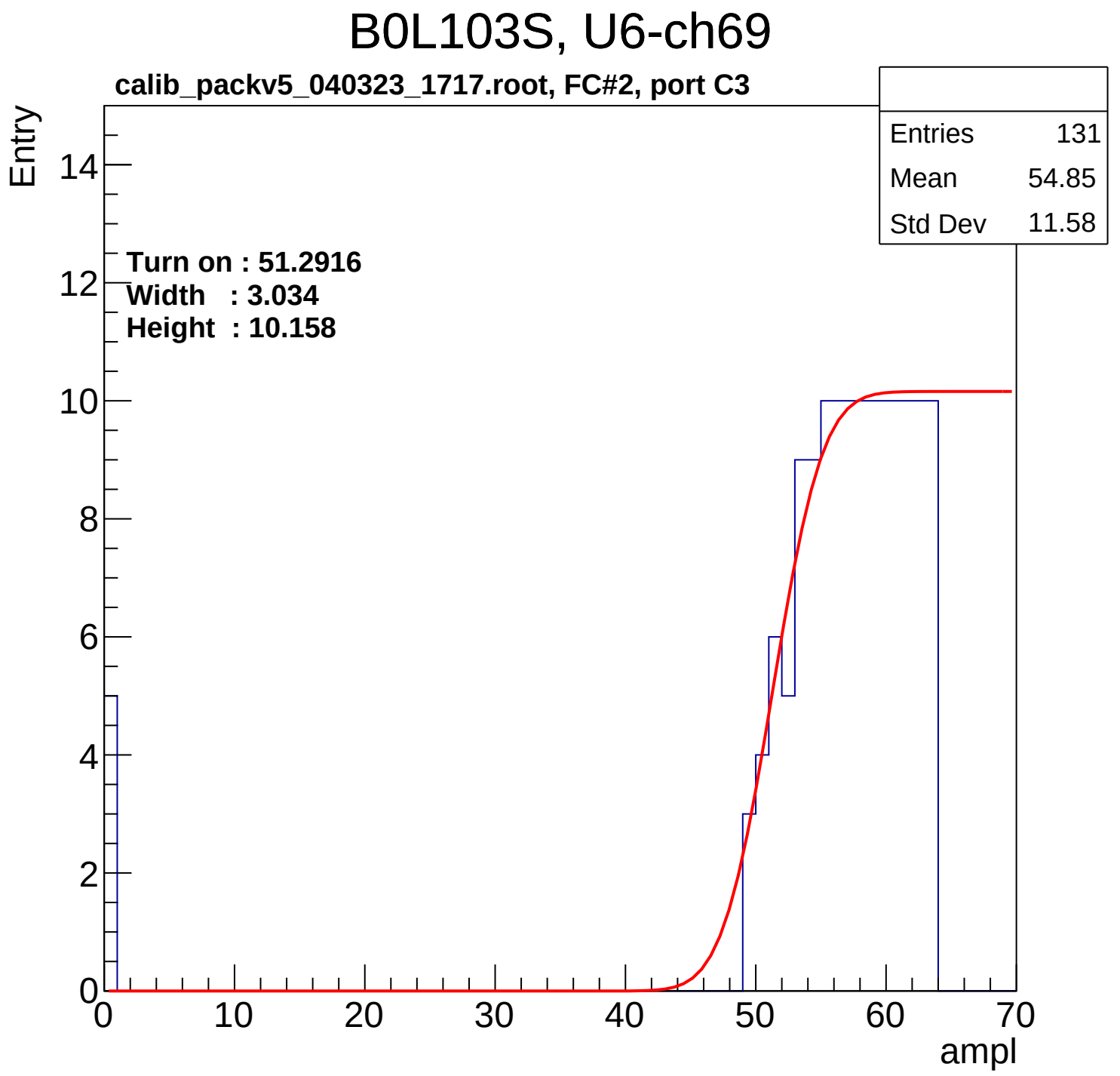
B0L103S, U6-ch69
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 54.85
Std Dev 11.58
Turn on : 51.2916
Width : 3.034
Height : 10.158
Entry
ampl
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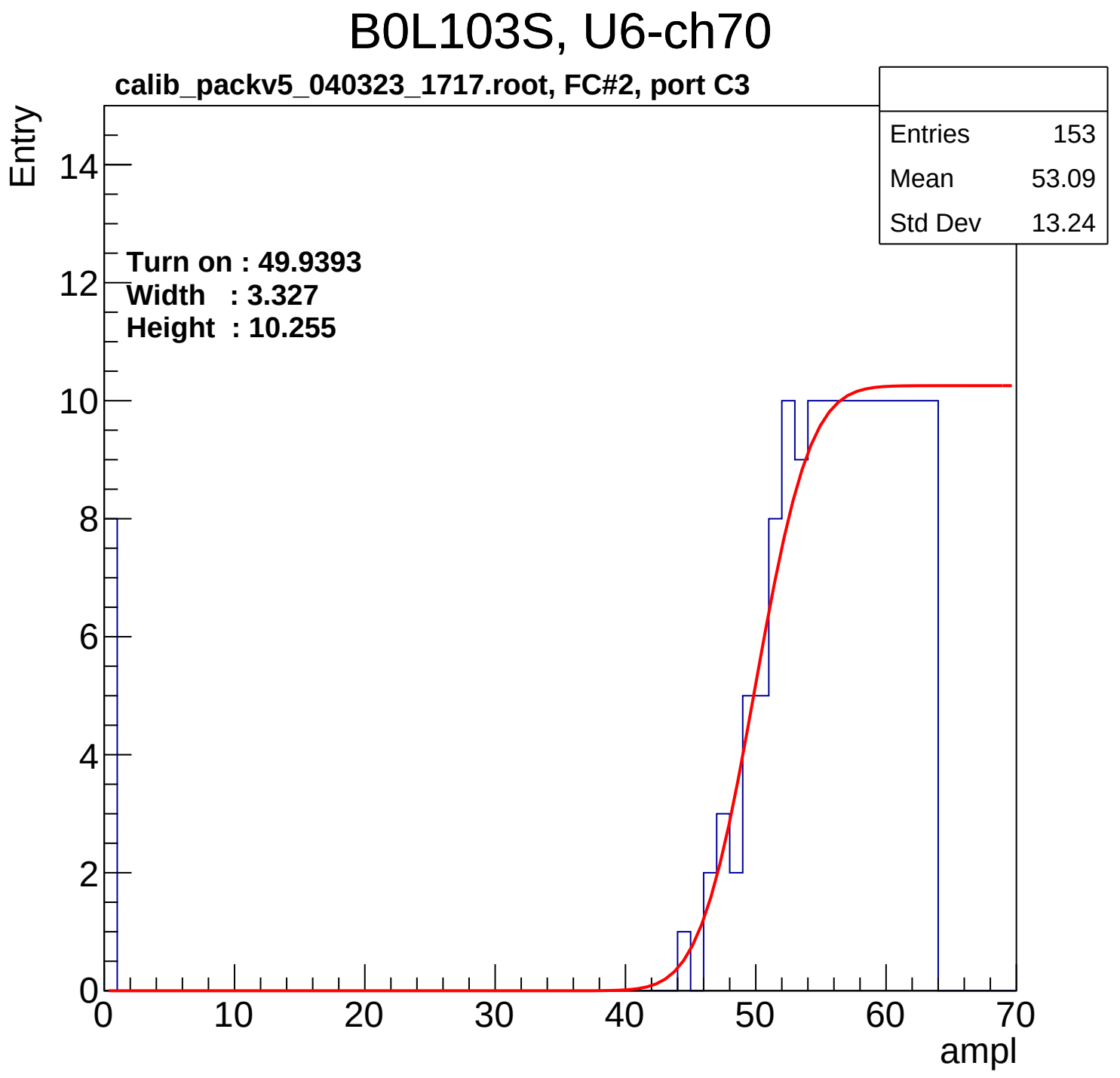
B0L103S, U6-ch70
calib_packv5_040323_1717.root, FC#2, port C3
Entries 153
Mean 53.09
Std Dev 13.24
Turn on : 49.9393
Width : 3.327
Height : 10.255
Entry
ampl
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8
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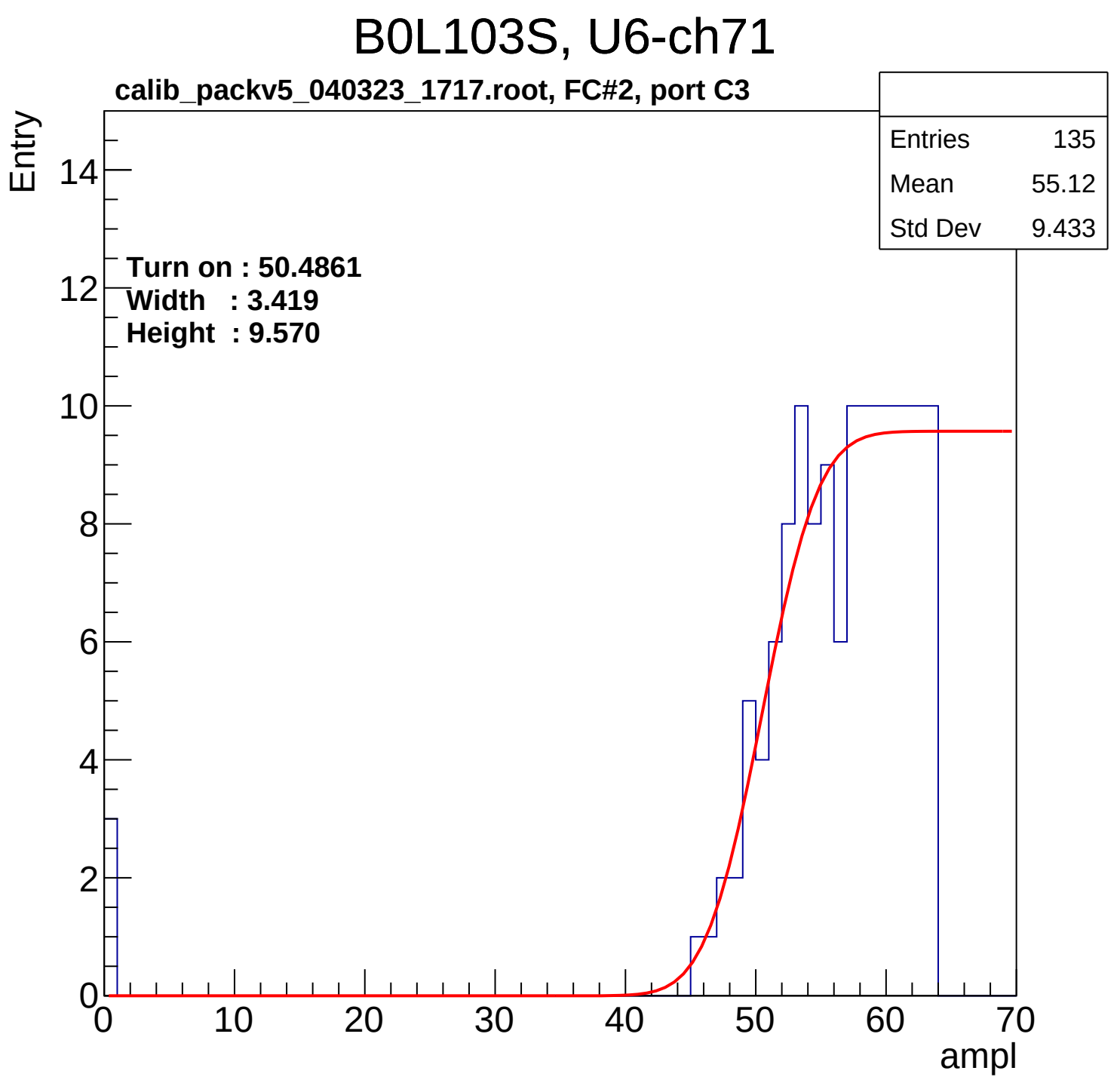
B0L103S, U6-ch71
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 55.12
Std Dev 9.433
Turn on : 50.4861
Width : 3.419
Height : 9.570
Entry
ampl
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6
8
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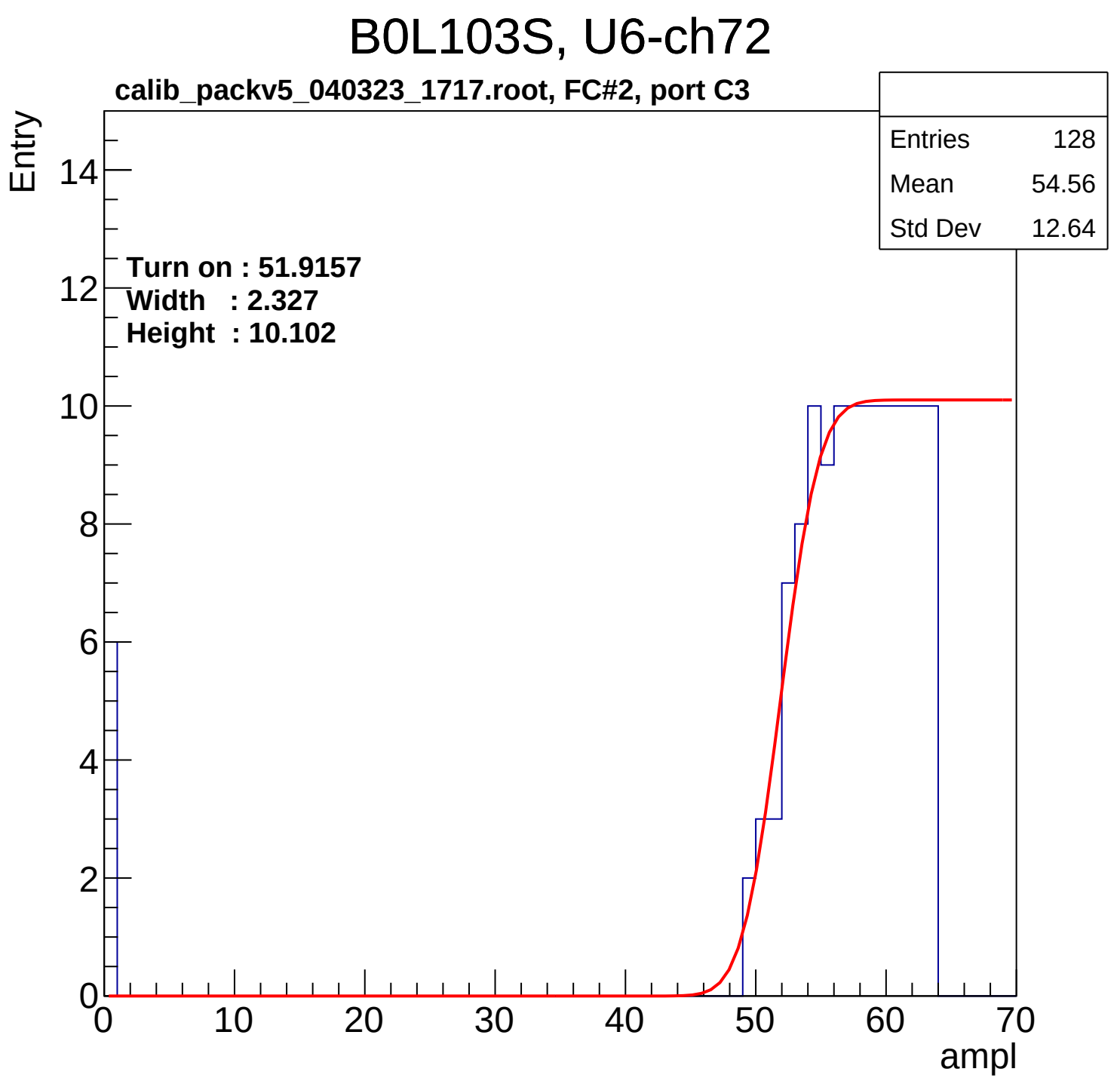
B0L103S, U6-ch72
calib_packv5_040323_1717.root, FC#2, port C3
Entries 128
Mean 54.56
Std Dev 12.64
Turn on : 51.9157
Width : 2.327
Height : 10.102
Entry
ampl
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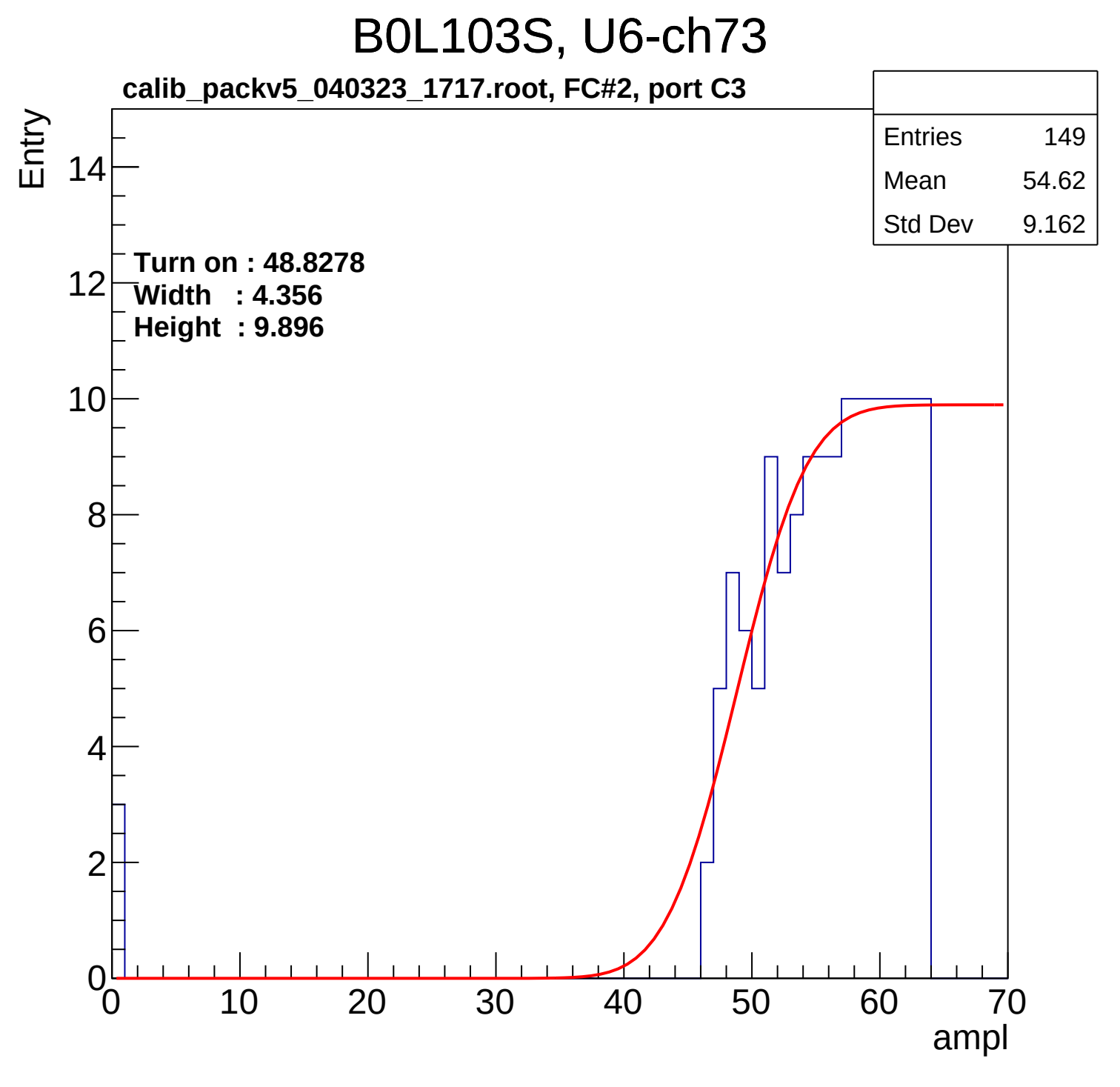
B0L103S, U6-ch73
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 54.62
Std Dev 9.162
Turn on : 48.8278
Width : 4.356
Height : 9.896
Entry
ampl
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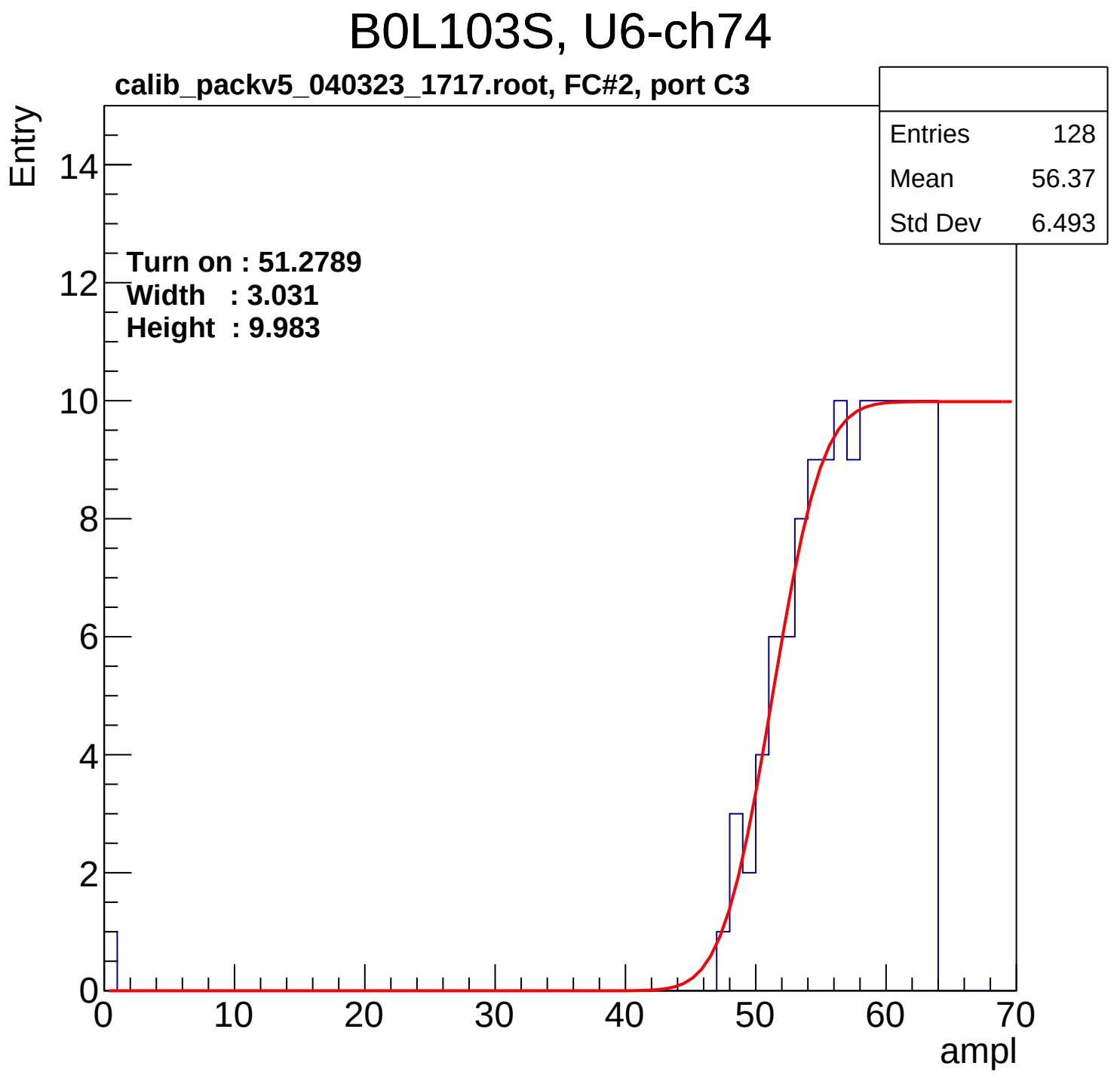
B0L103S, U6-ch74
calib_packv5_040323_1717.root, FC#2, port C3
Entries 128
Mean 56.37
Std Dev 6.493
Turn on : 51.2789
Width : 3.031
Height : 9.983
Entry
ampl
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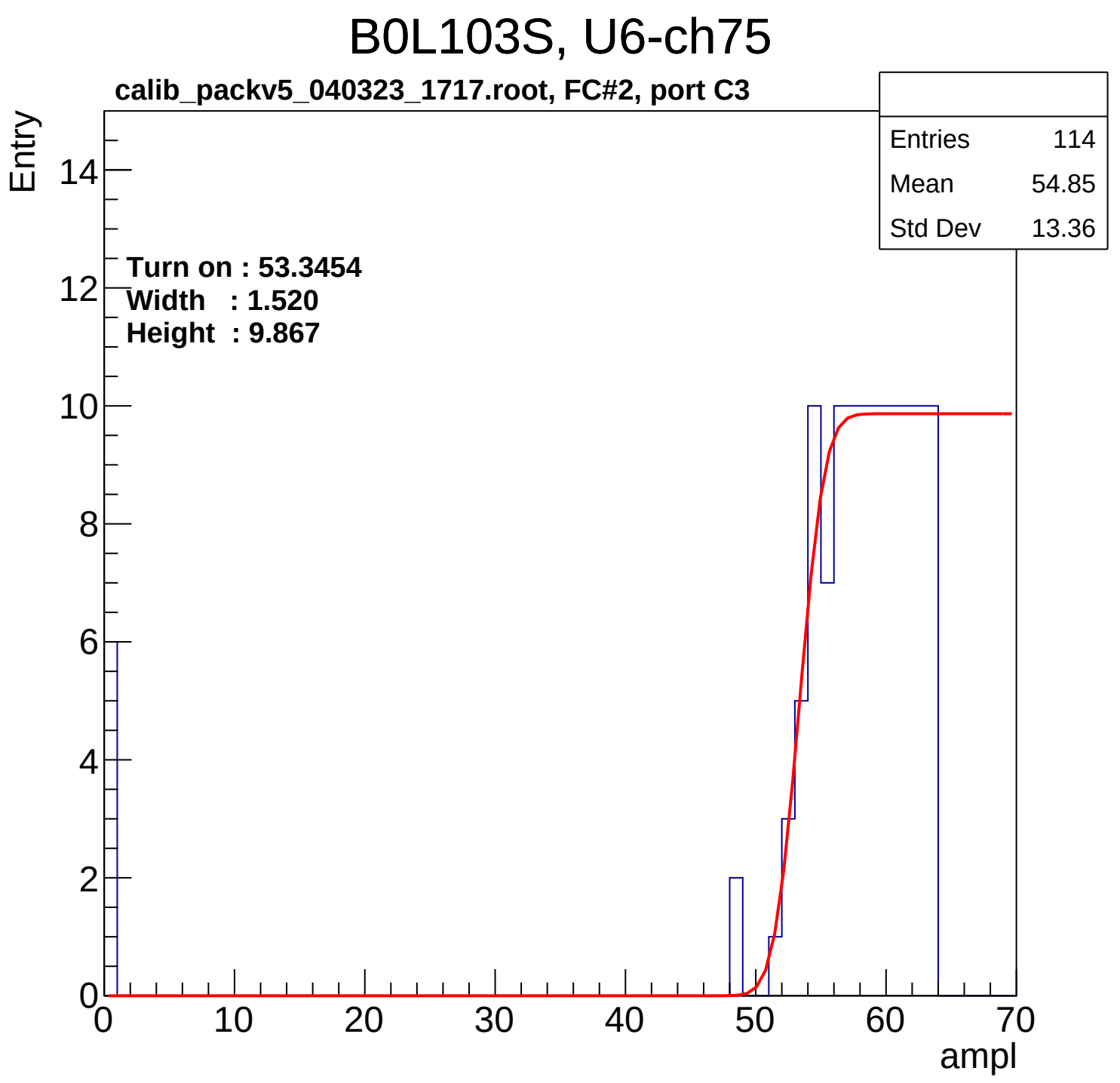
B0L103S, U6-ch75
calib_packv5_040323_1717.root, FC#2, port C3
Entries 114
Mean 54.85
Std Dev 13.36
Turn on : 53.3454
Width : 1.520
Height : 9.867
Entry
ampl
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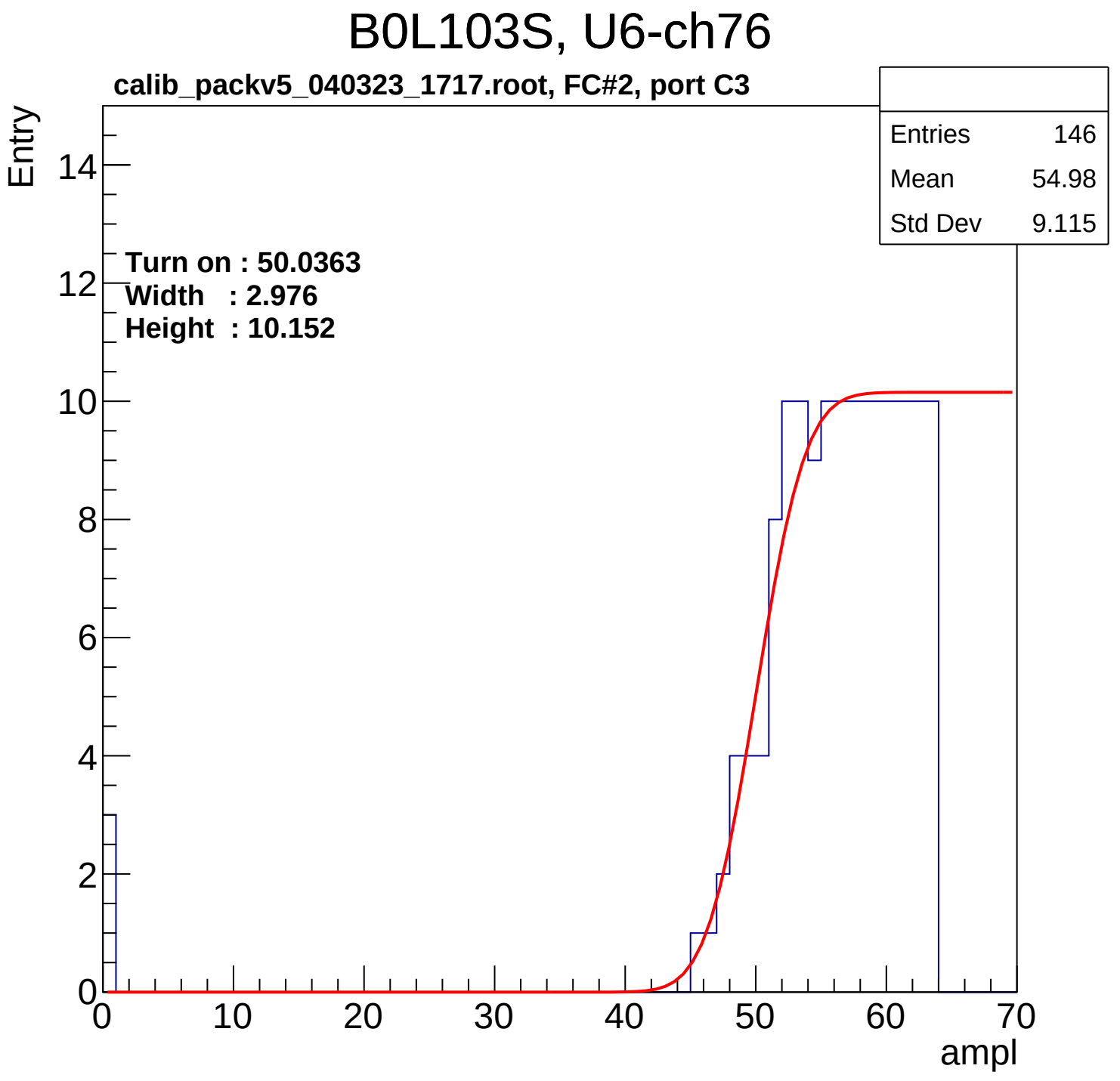
B0L103S, U6-ch76
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 54.98
Std Dev 9.115
Turn on : 50.0363
Width : 2.976
Height : 10.152
Entry
ampl
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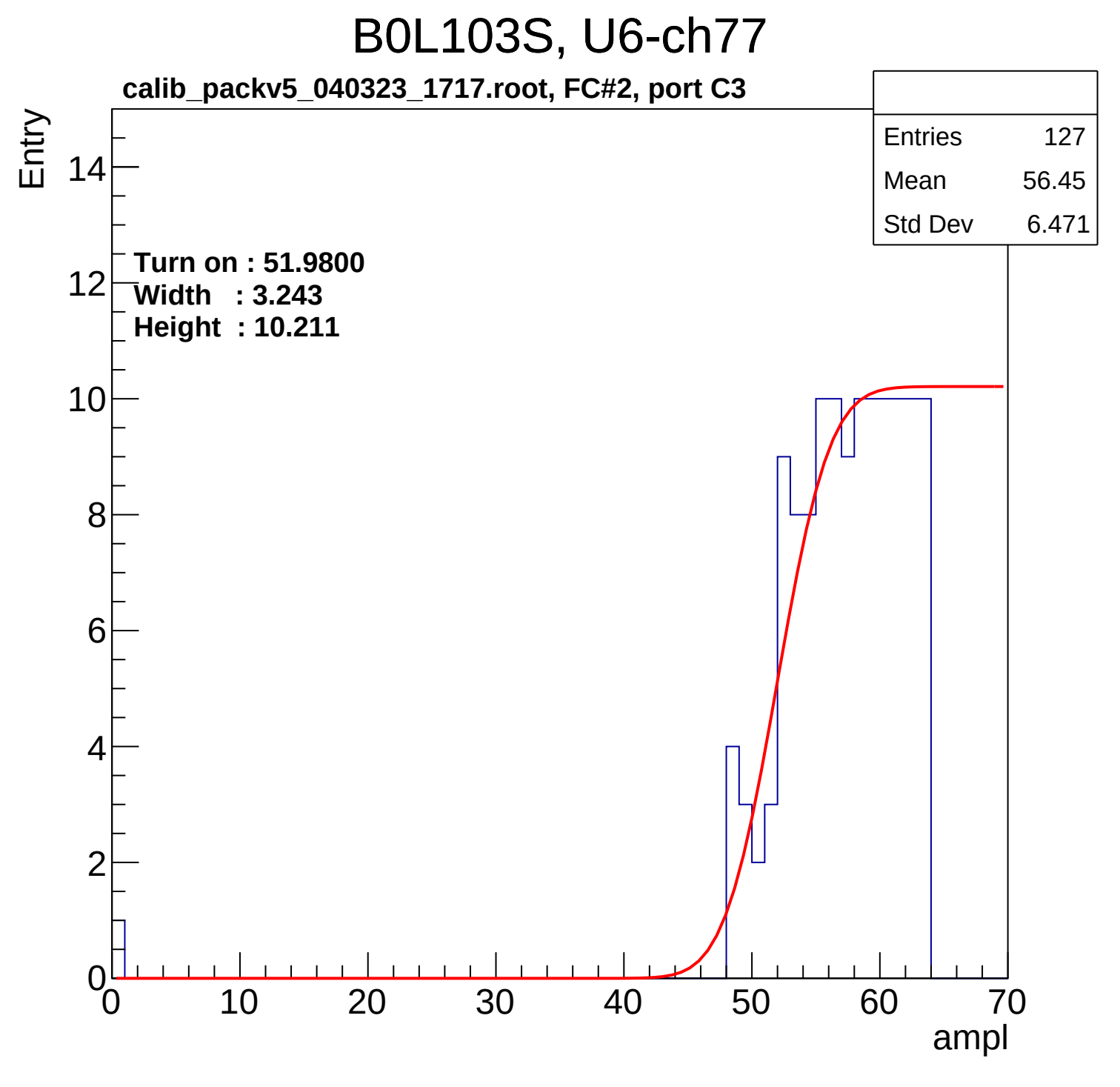
B0L103S, U6-ch77
calib_packv5_040323_1717.root, FC#2, port C3
Entries 127
Mean 56.45
Std Dev 6.471
Turn on : 51.9800
Width : 3.243
Height : 10.211
Entry
ampl
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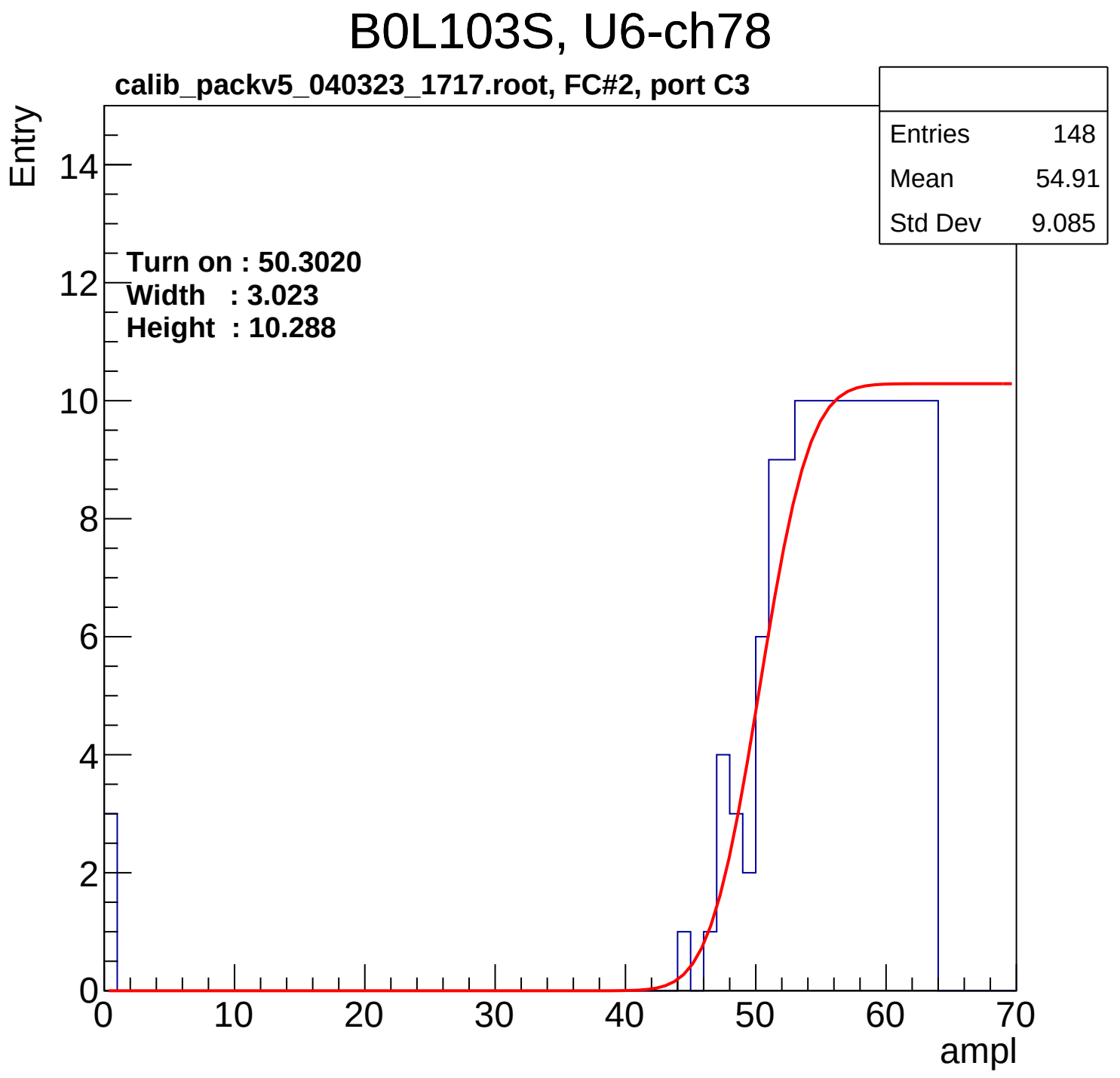
B0L103S, U6-ch78
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 54.91
Std Dev 9.085
Turn on : 50.3020
Width : 3.023
Height : 10.288
Entry
ampl
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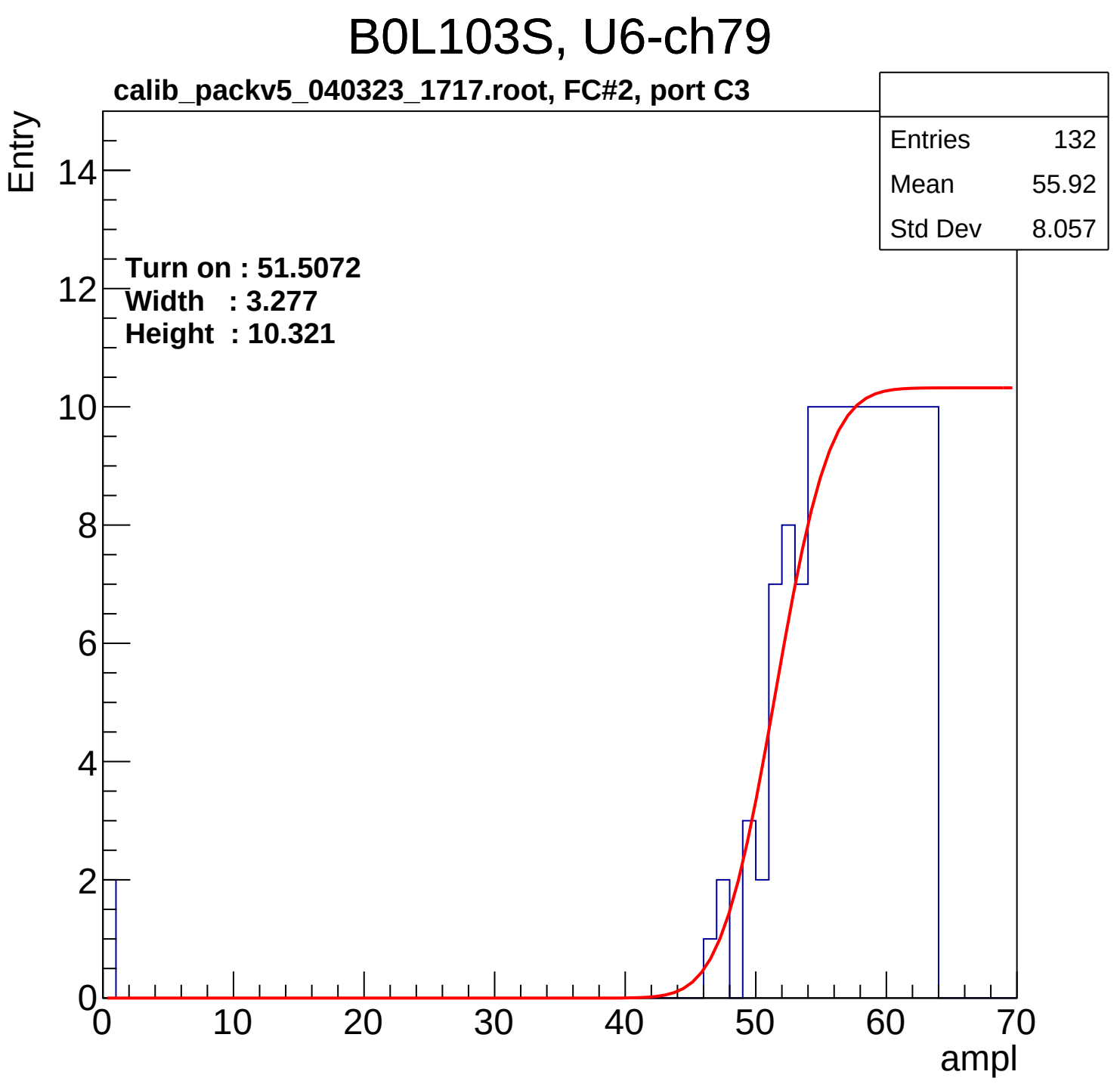
B0L103S, U6-ch79
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 55.92
Std Dev 8.057
Turn on : 51.5072
Width : 3.277
Height : 10.321
Entry
ampl
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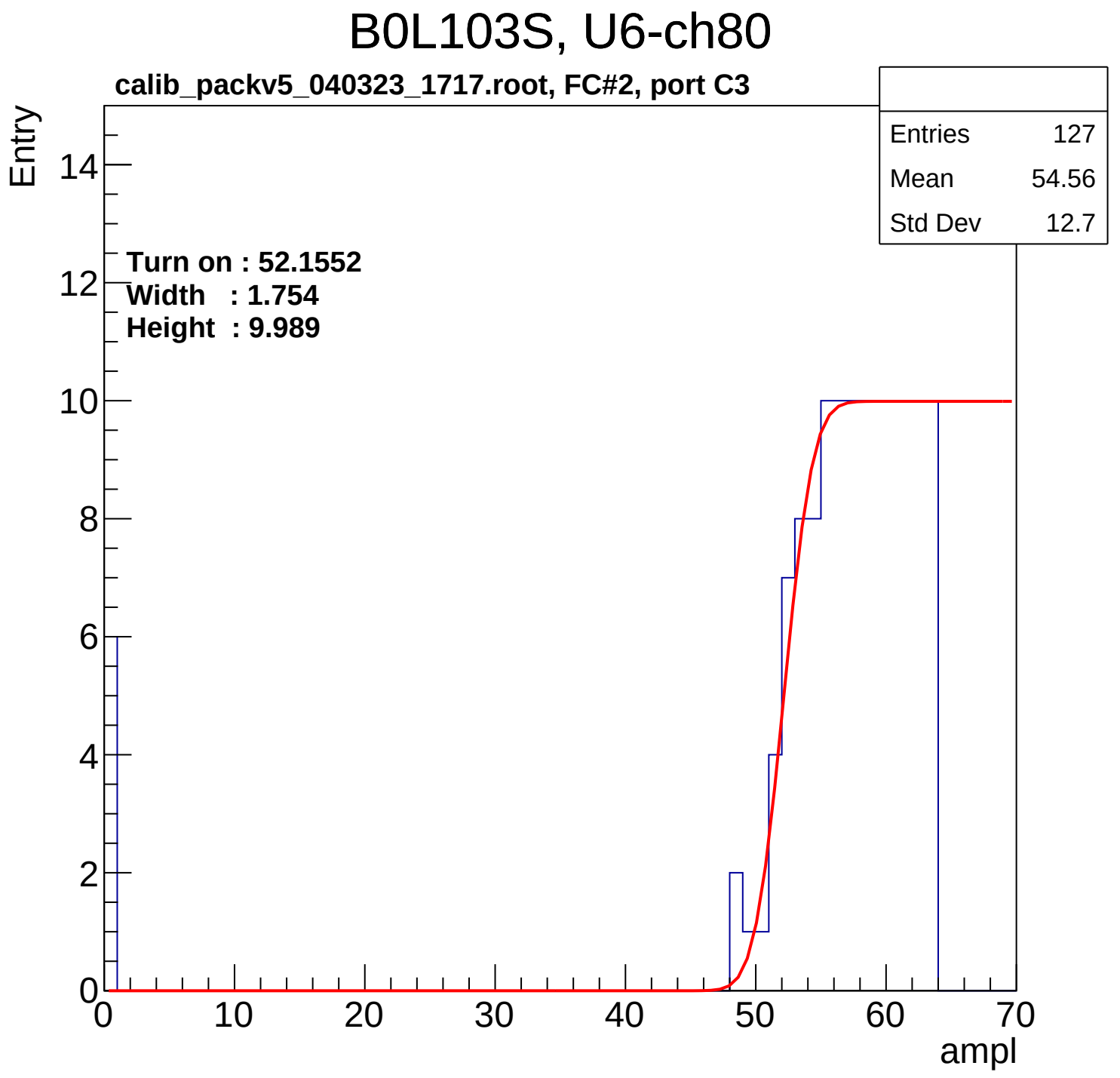
B0L103S, U6-ch80
calib_packv5_040323_1717.root, FC#2, port C3
Entries 127
Mean 54.56
Std Dev 12.7
Turn on : 52.1552
Width : 1.754
Height : 9.989
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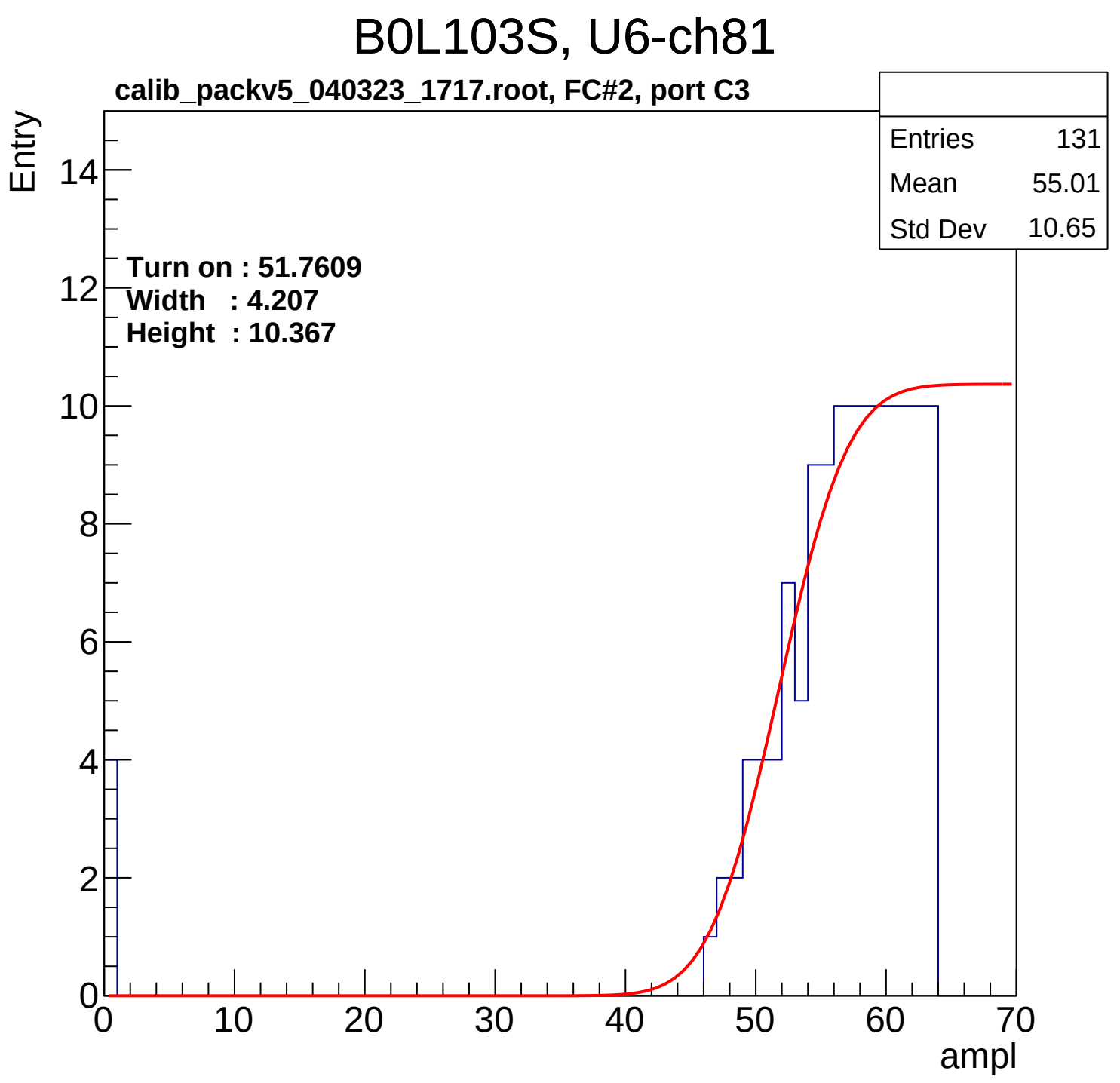
B0L103S, U6-ch81
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 55.01
Std Dev 10.65
Turn on : 51.7609
Width : 4.207
Height : 10.367
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ampl
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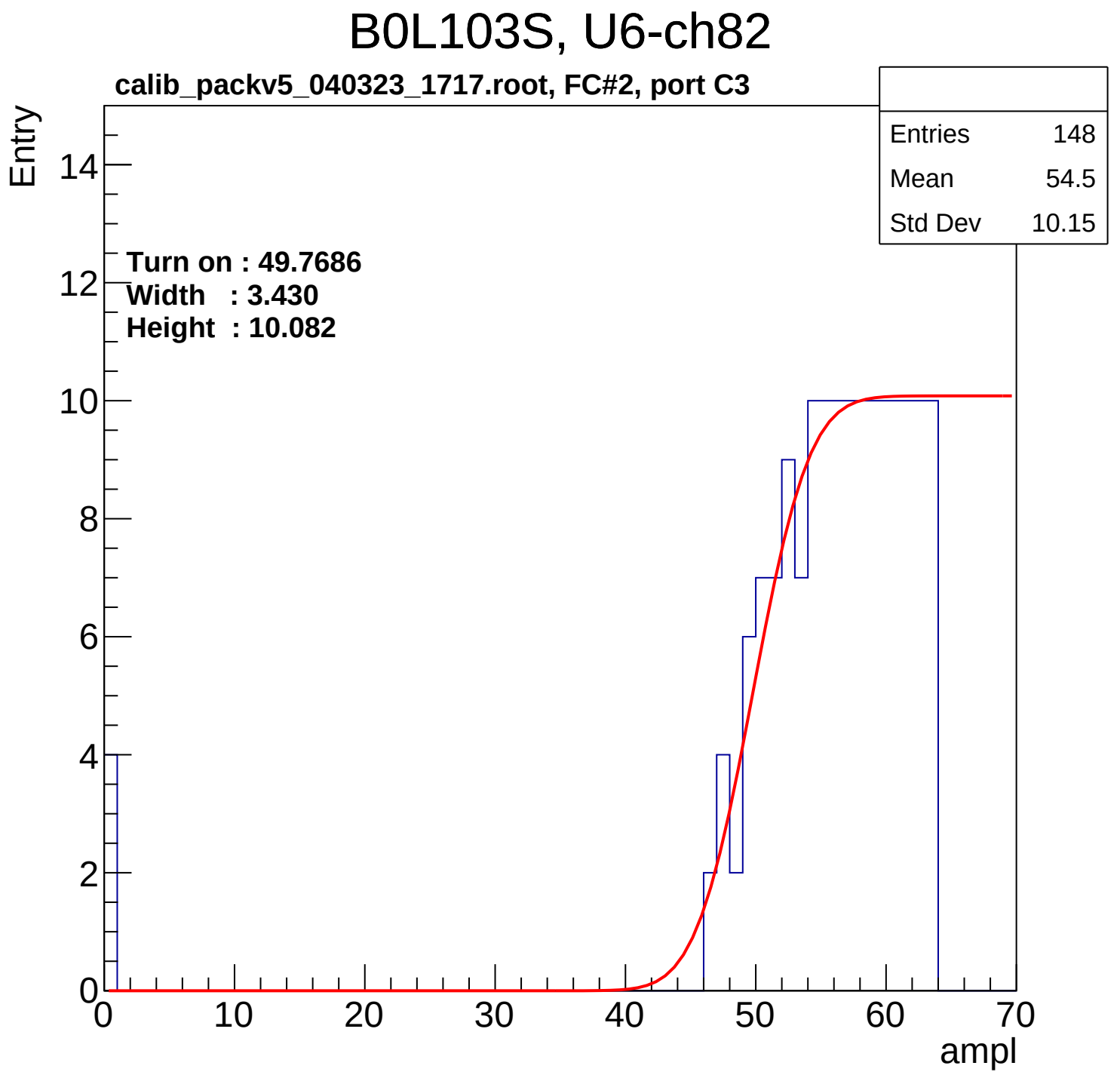
B0L103S, U6-ch82
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 54.5
Std Dev 10.15
Turn on : 49.7686
Width : 3.430
Height : 10.082
Entry
ampl
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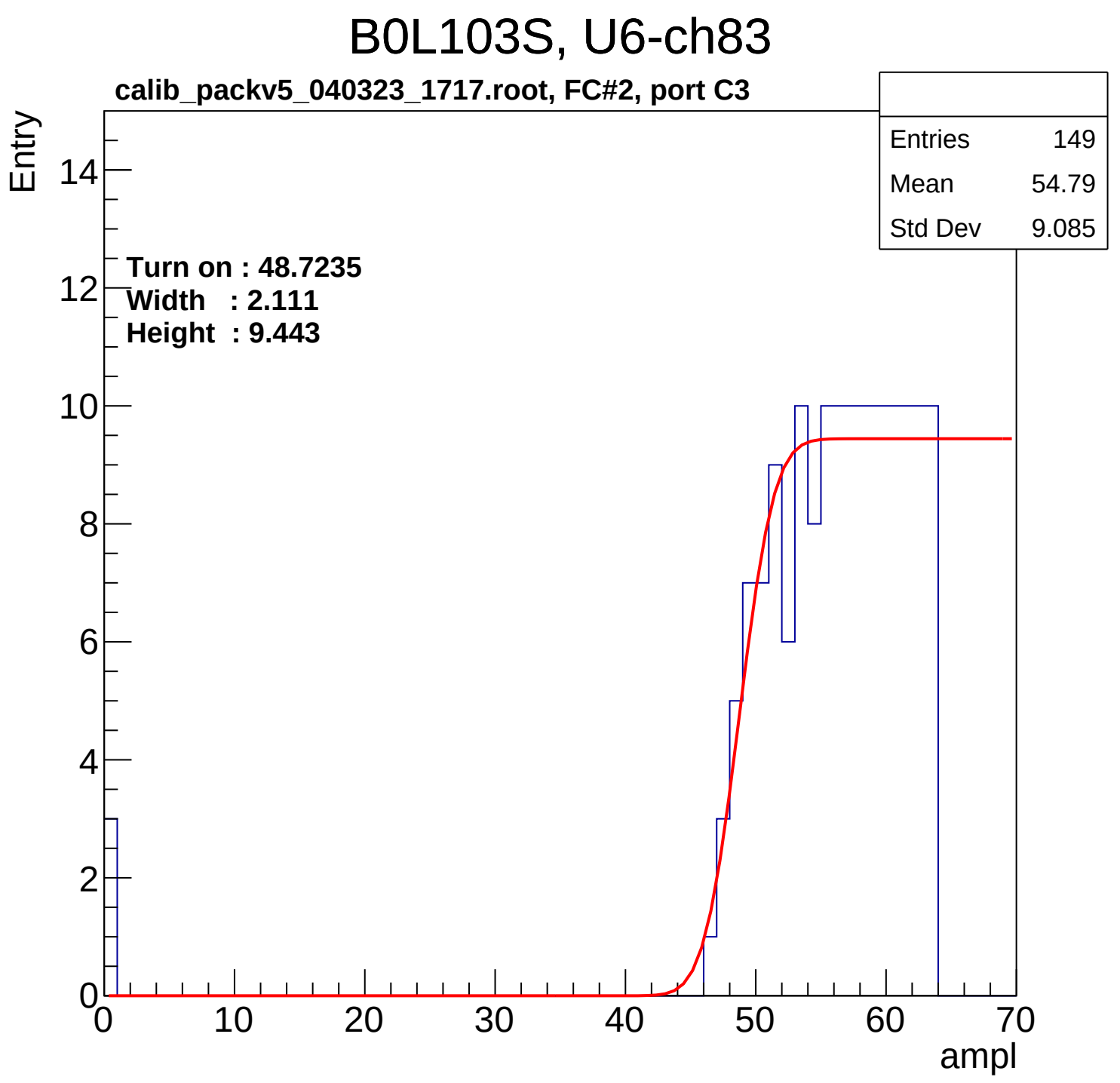
B0L103S, U6-ch83
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 54.79
Std Dev 9.085
Turn on : 48.7235
Width : 2.111
Height : 9.443
Entry
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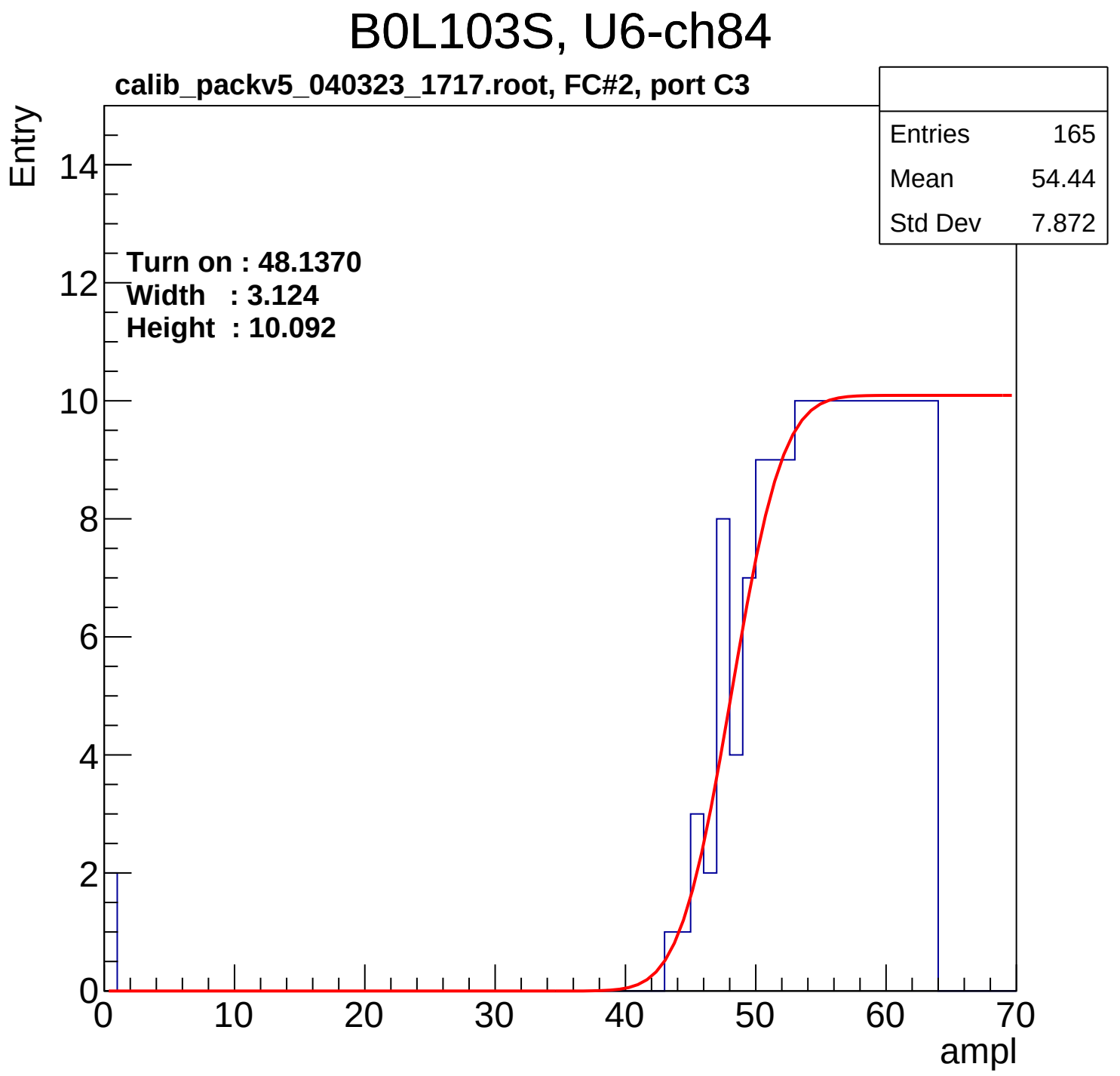
B0L103S, U6-ch84
calib_packv5_040323_1717.root, FC#2, port C3
Entries 165
Mean 54.44
Std Dev 7.872
Turn on : 48.1370
Width : 3.124
Height : 10.092
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ampl
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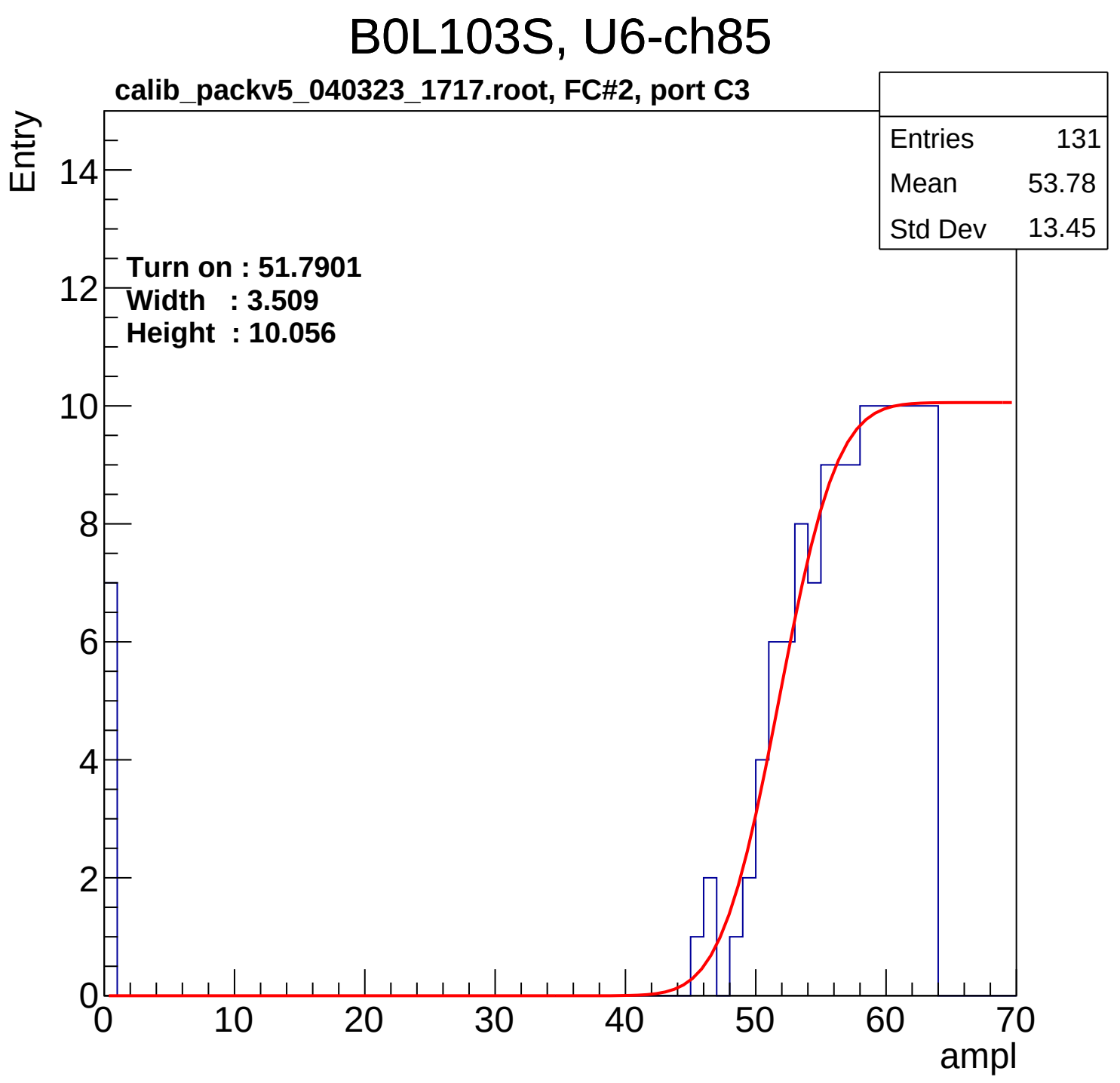
B0L103S, U6-ch85
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 53.78
Std Dev 13.45
Turn on : 51.7901
Width : 3.509
Height : 10.056
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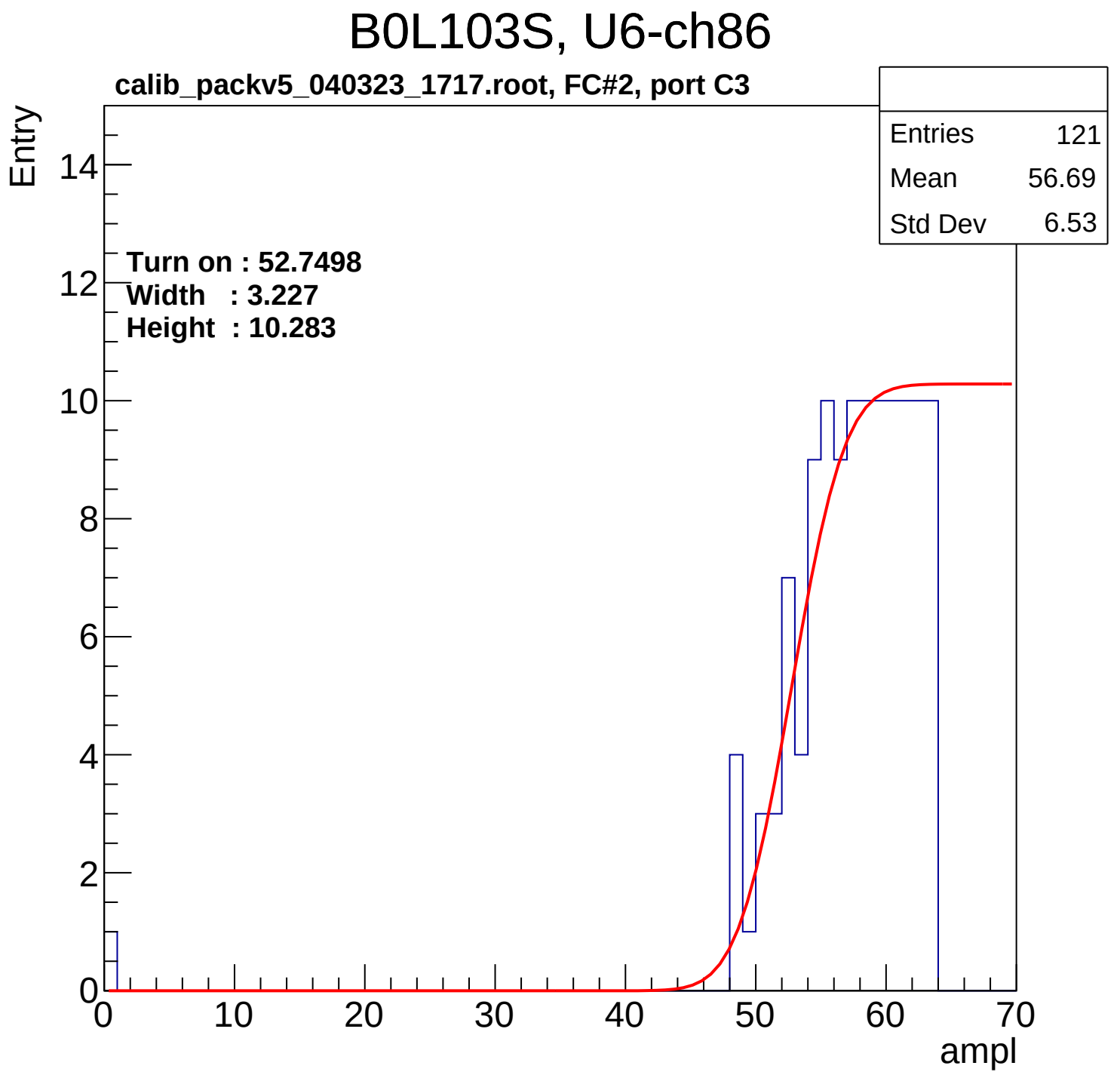
B0L103S, U6-ch86
calib_packv5_040323_1717.root, FC#2, port C3
Entries 121
Mean 56.69
Std Dev 6.53
Turn on : 52.7498
Width : 3.227
Height : 10.283
Entry
ampl
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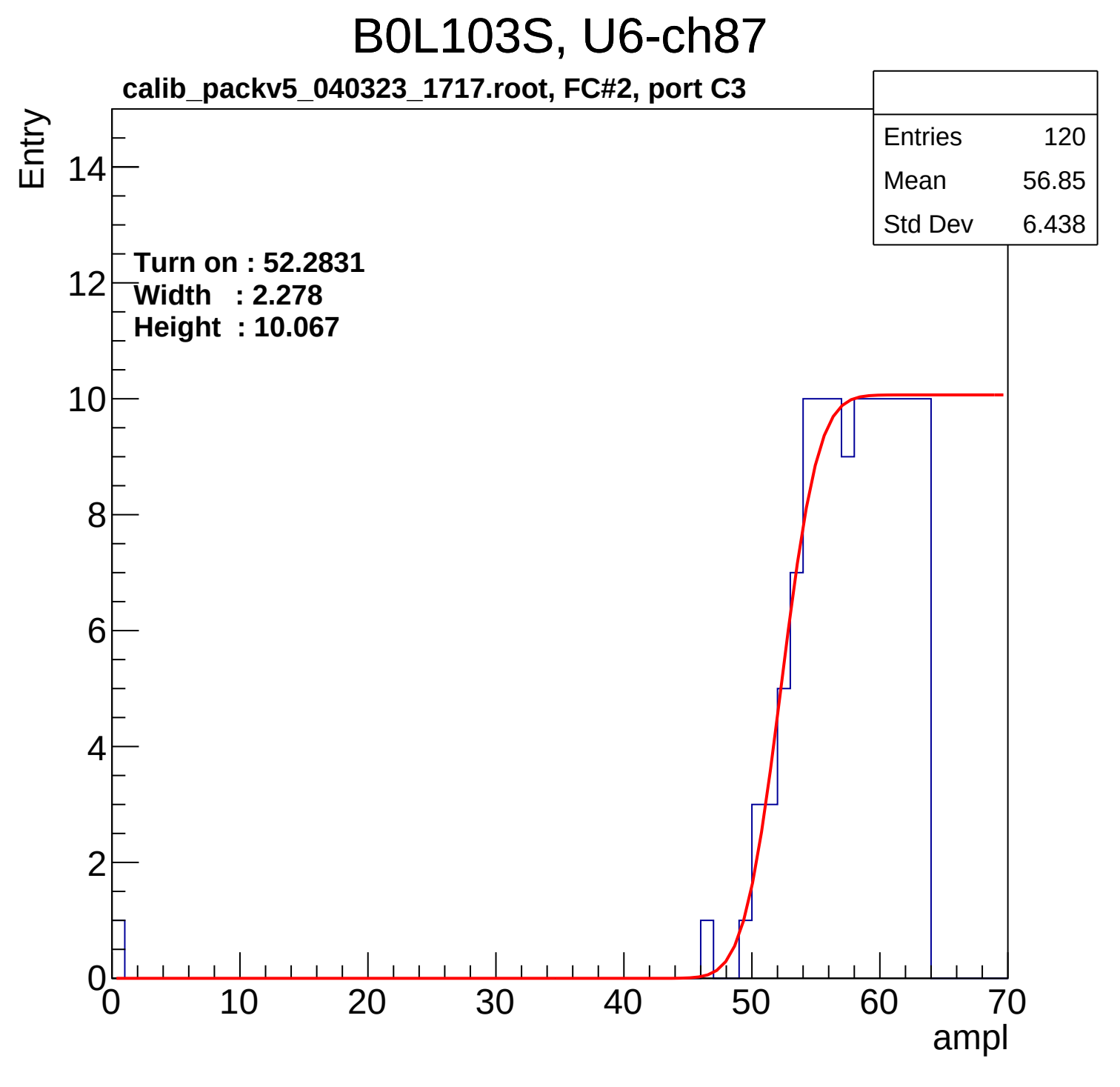
B0L103S, U6-ch87
calib_packv5_040323_1717.root, FC#2, port C3
Entries 120
Mean 56.85
Std Dev 6.438
Turn on : 52.2831
Width : 2.278
Height : 10.067
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ampl
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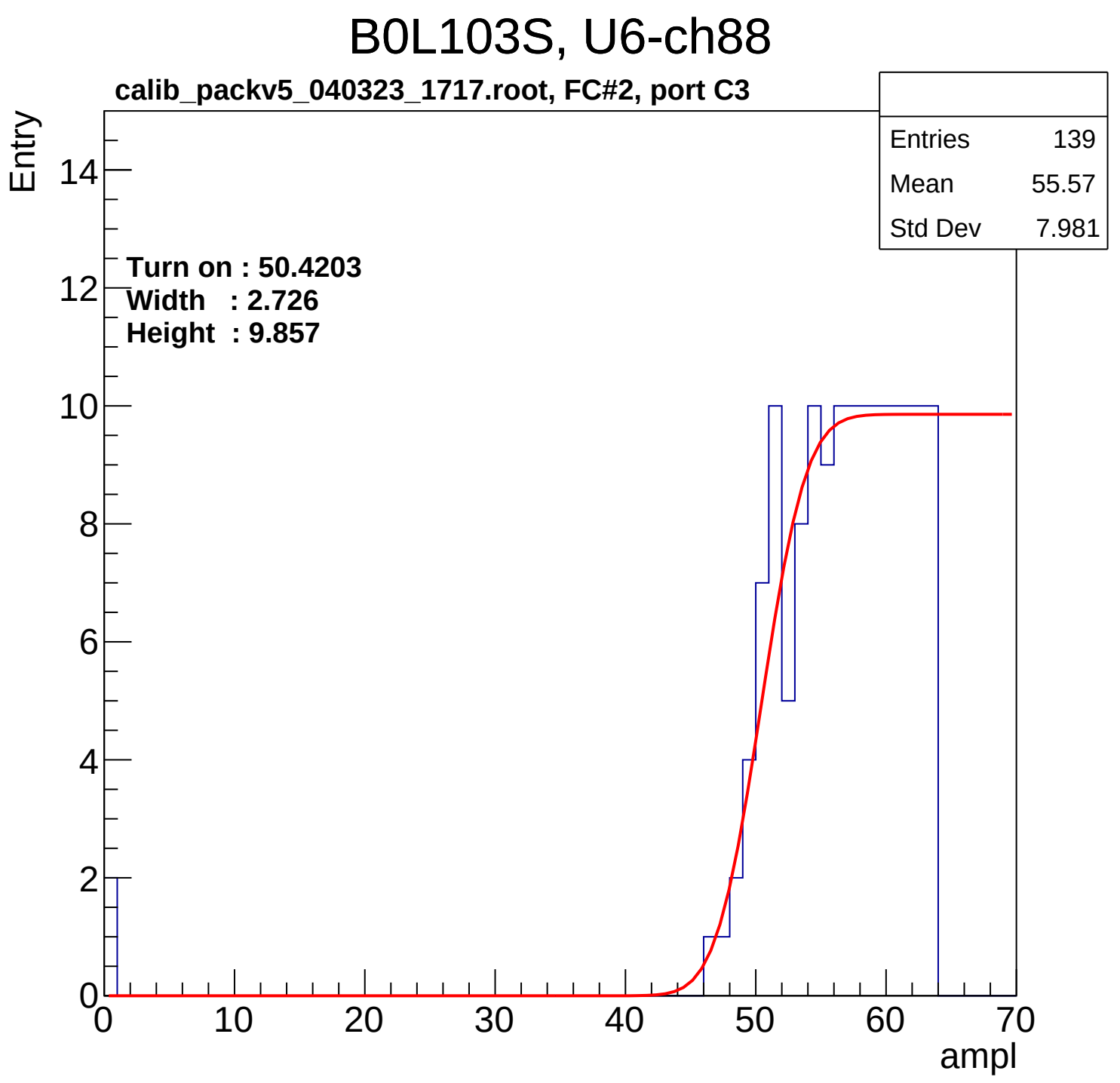
B0L103S, U6-ch88
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 55.57
Std Dev 7.981
Turn on : 50.4203
Width : 2.726
Height : 9.857
Entry
ampl
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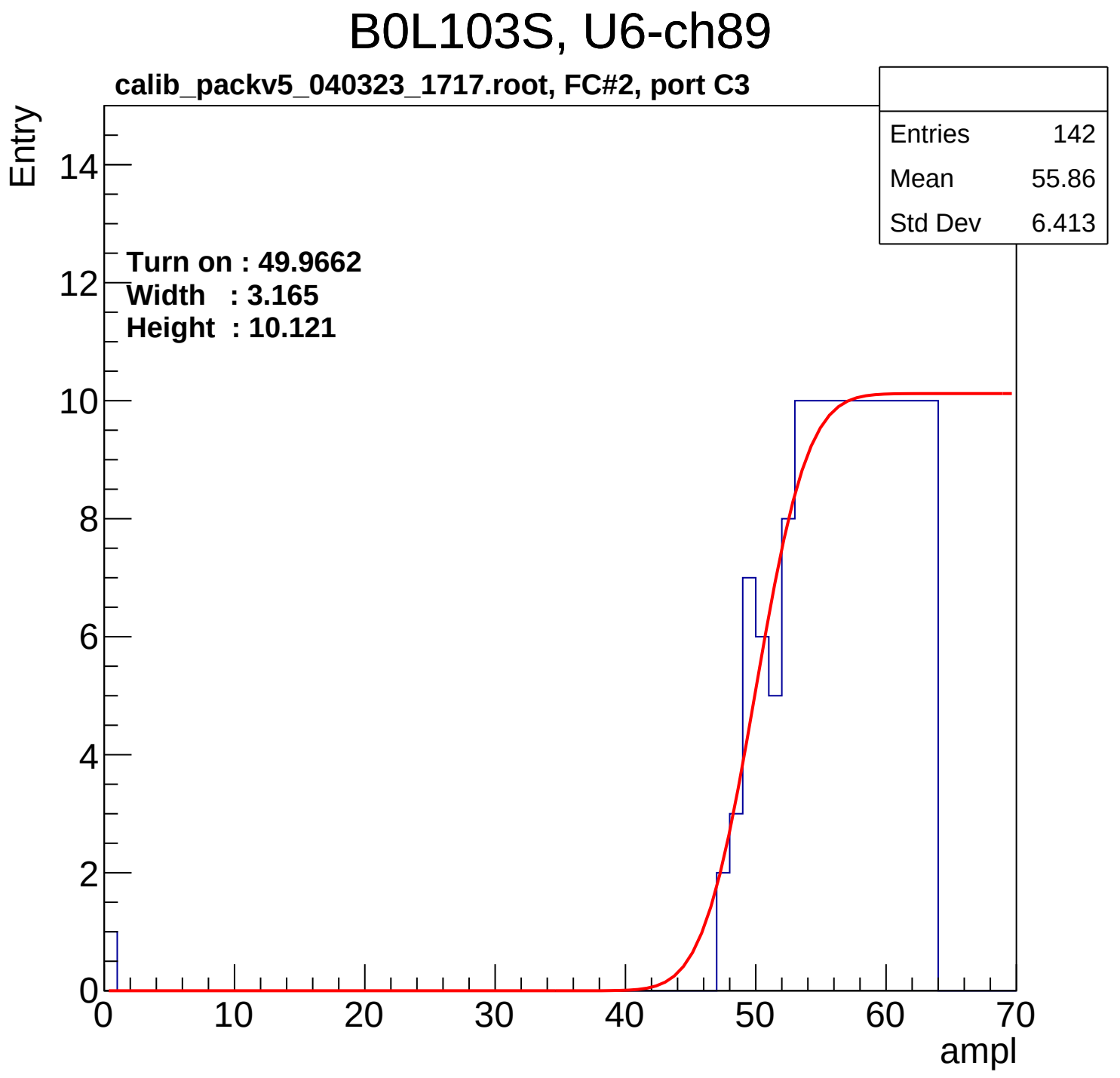
B0L103S, U6-ch89
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 55.86
Std Dev 6.413
Turn on : 49.9662
Width : 3.165
Height : 10.121
Entry
ampl
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2
4
6
8
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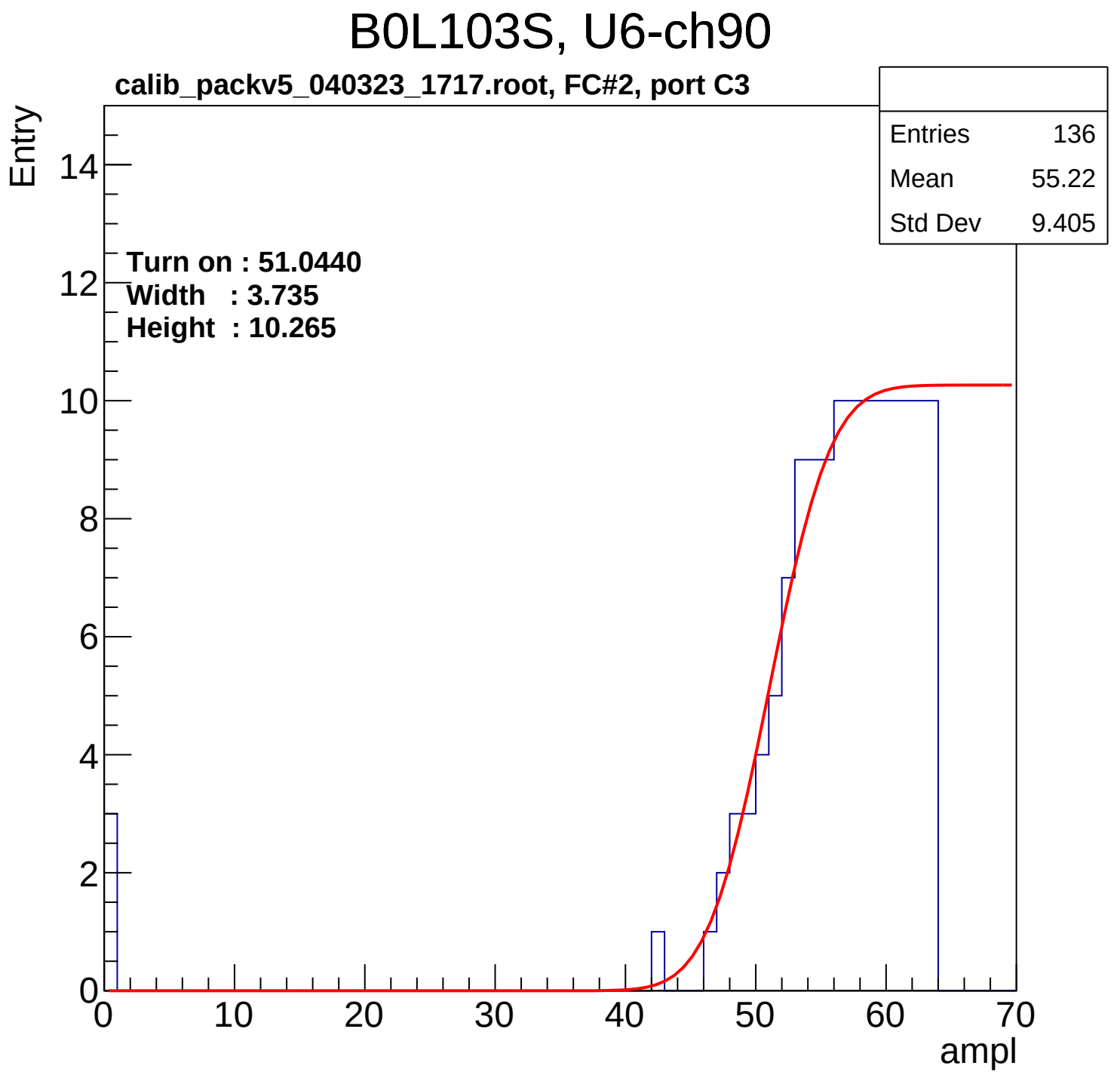
B0L103S, U6-ch90
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 55.22
Std Dev 9.405
Turn on : 51.0440
Width : 3.735
Height : 10.265
Entry
ampl
0
2
4
6
8
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0
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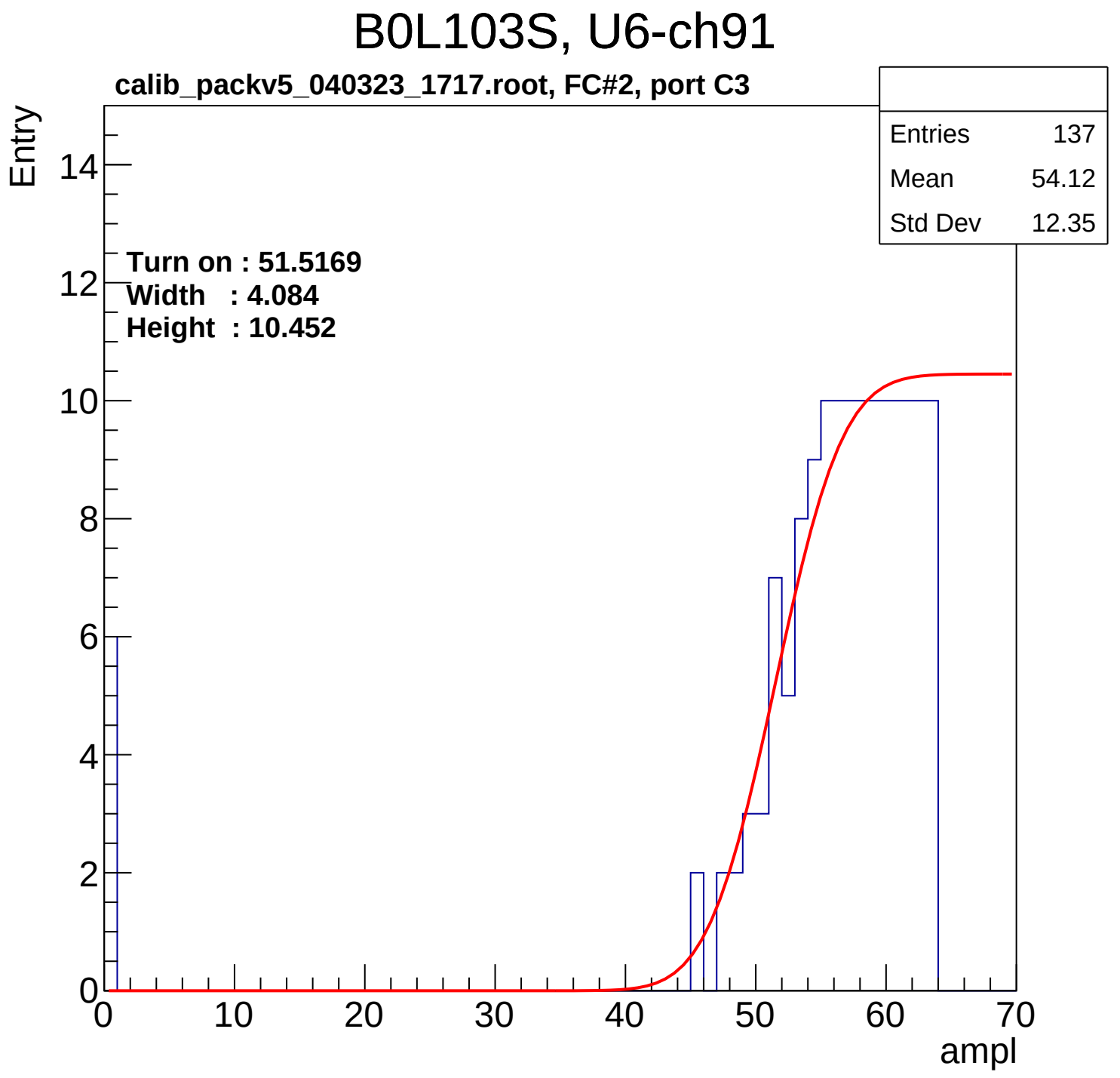
B0L103S, U6-ch91
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 54.12
Std Dev 12.35
Turn on : 51.5169
Width : 4.084
Height : 10.452
Entry
ampl
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2
4
6
8
10
12
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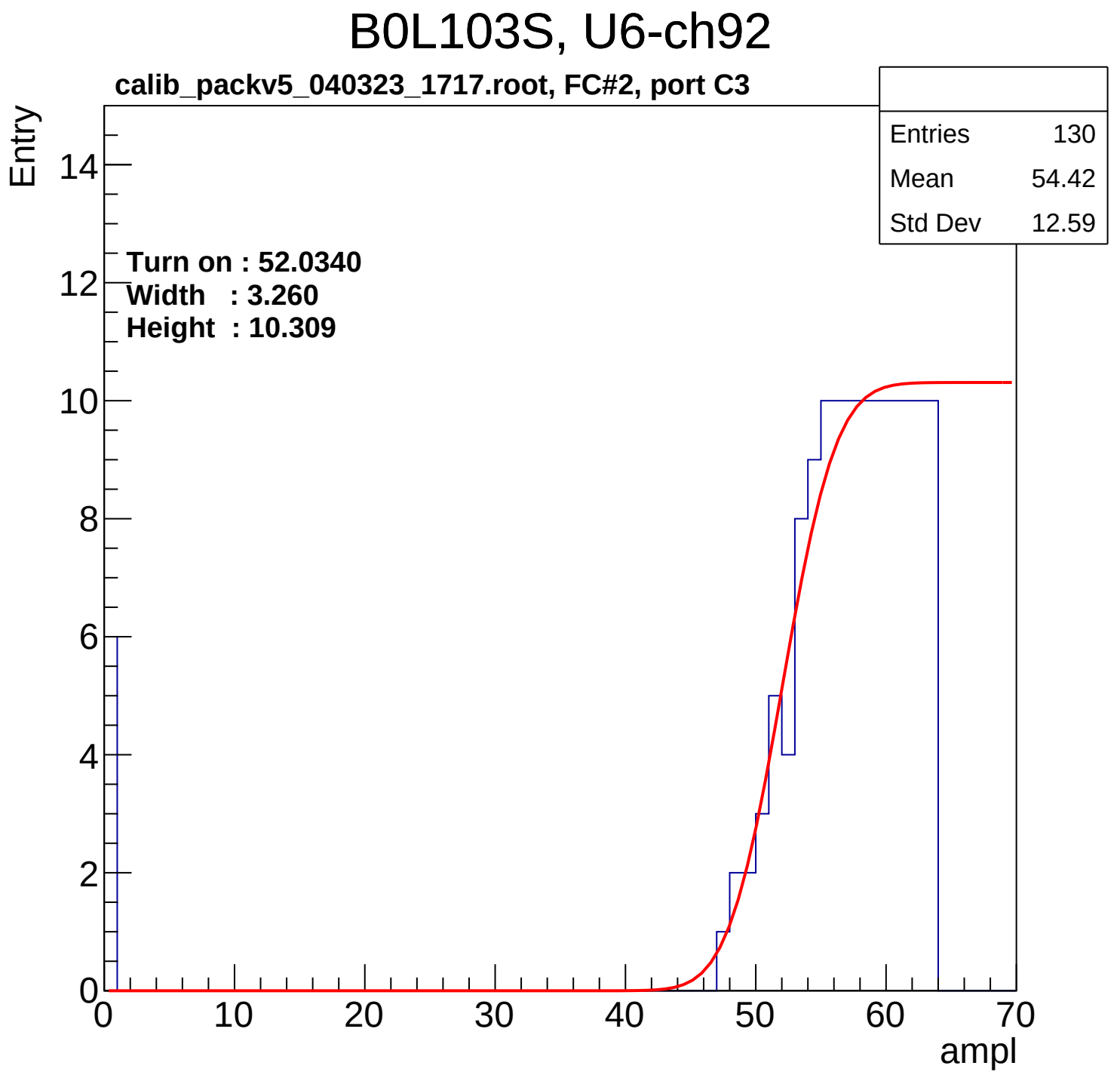
B0L103S, U6-ch92
calib_packv5_040323_1717.root, FC#2, port C3
Entries 130
Mean 54.42
Std Dev 12.59
Turn on : 52.0340
Width : 3.260
Height : 10.309
Entry
ampl
0
2
4
6
8
10
12
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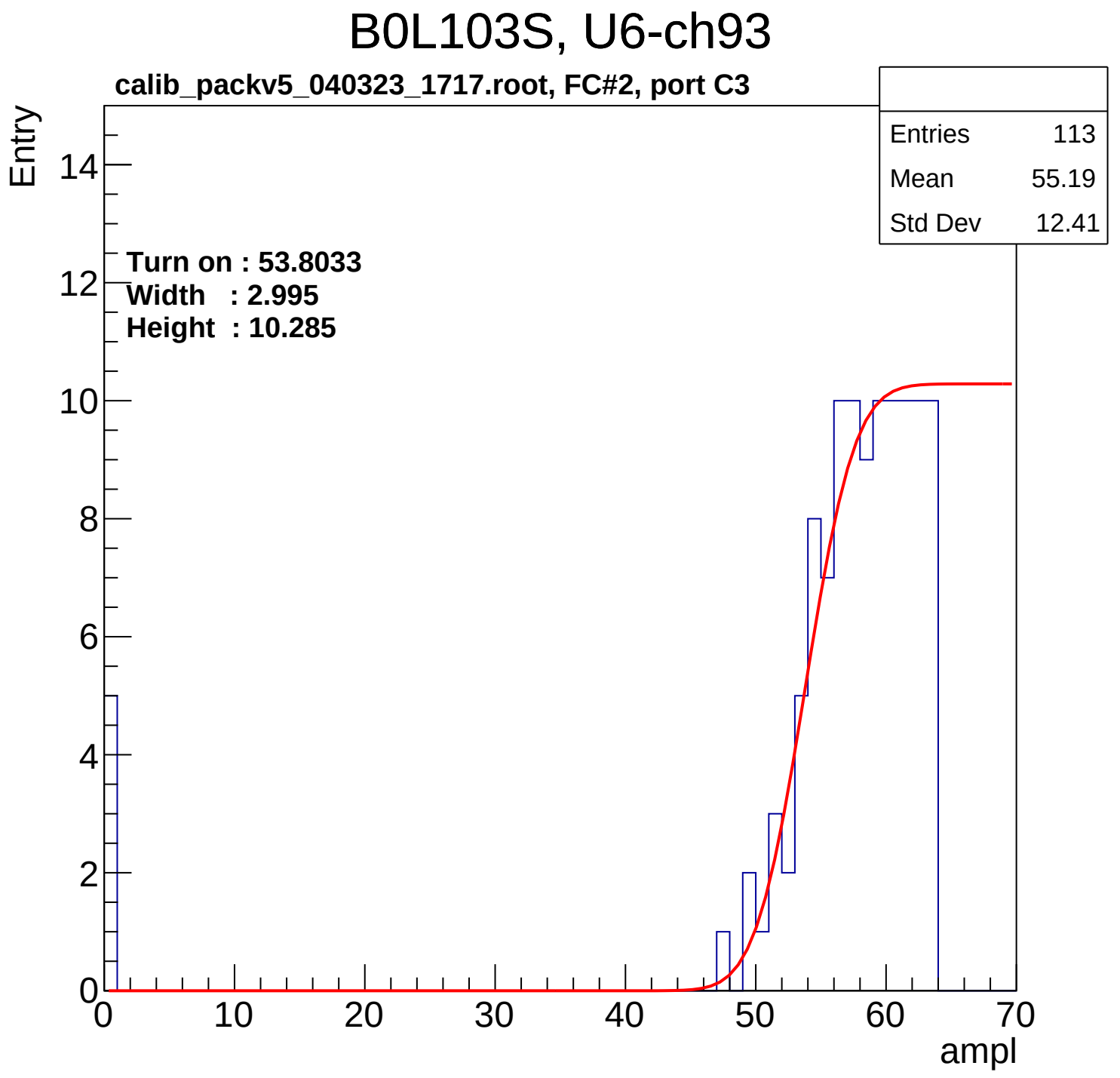
B0L103S, U6-ch93
calib_packv5_040323_1717.root, FC#2, port C3
Entries 113
Mean 55.19
Std Dev 12.41
Turn on : 53.8033
Width : 2.995
Height : 10.285
Entry
ampl
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2
4
6
8
10
12
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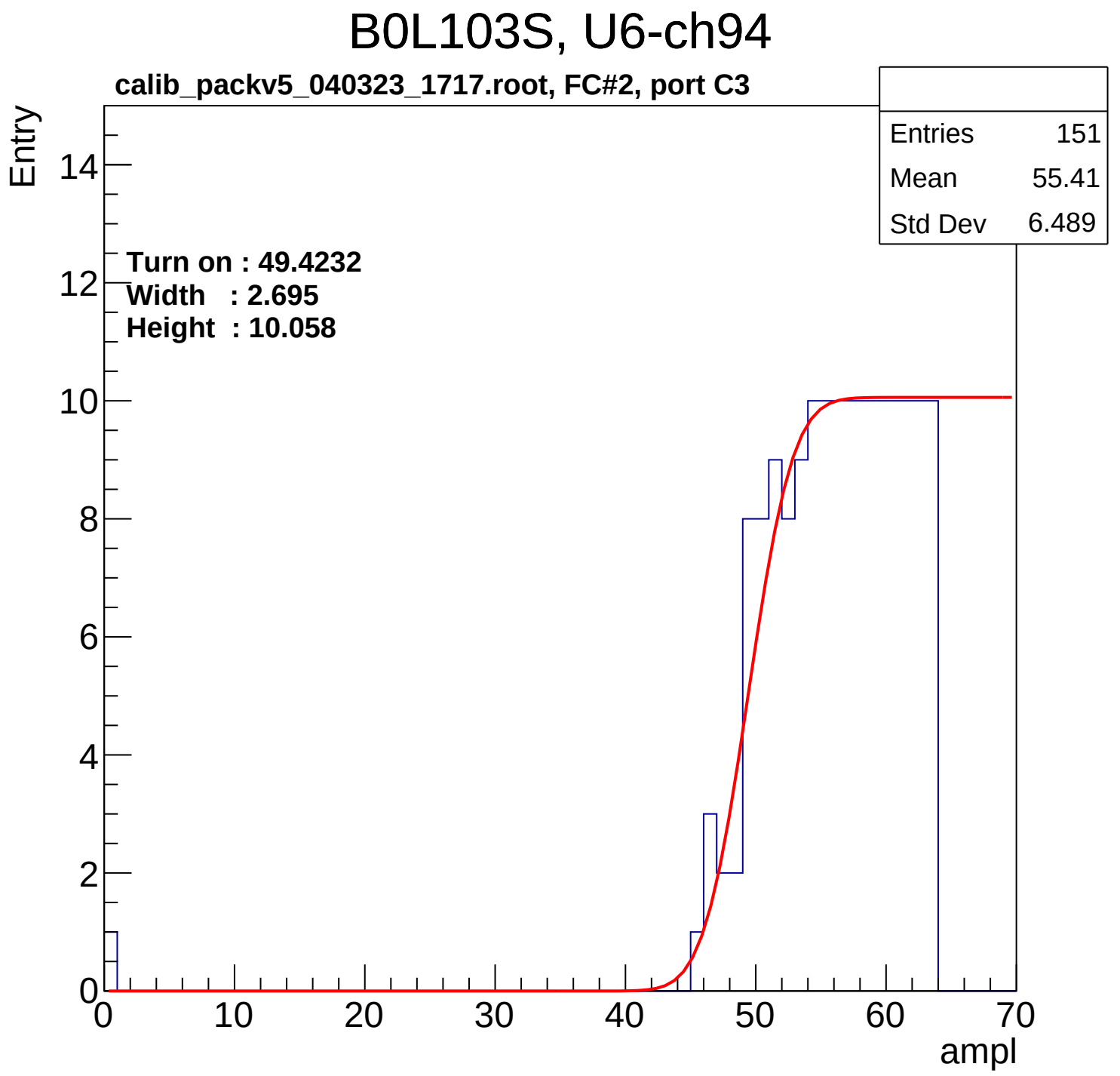
B0L103S, U6-ch94
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 55.41
Std Dev 6.489
Turn on : 49.4232
Width : 2.695
Height : 10.058
Entry
ampl
0
2
4
6
8
10
12
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0
10
20
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40
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60
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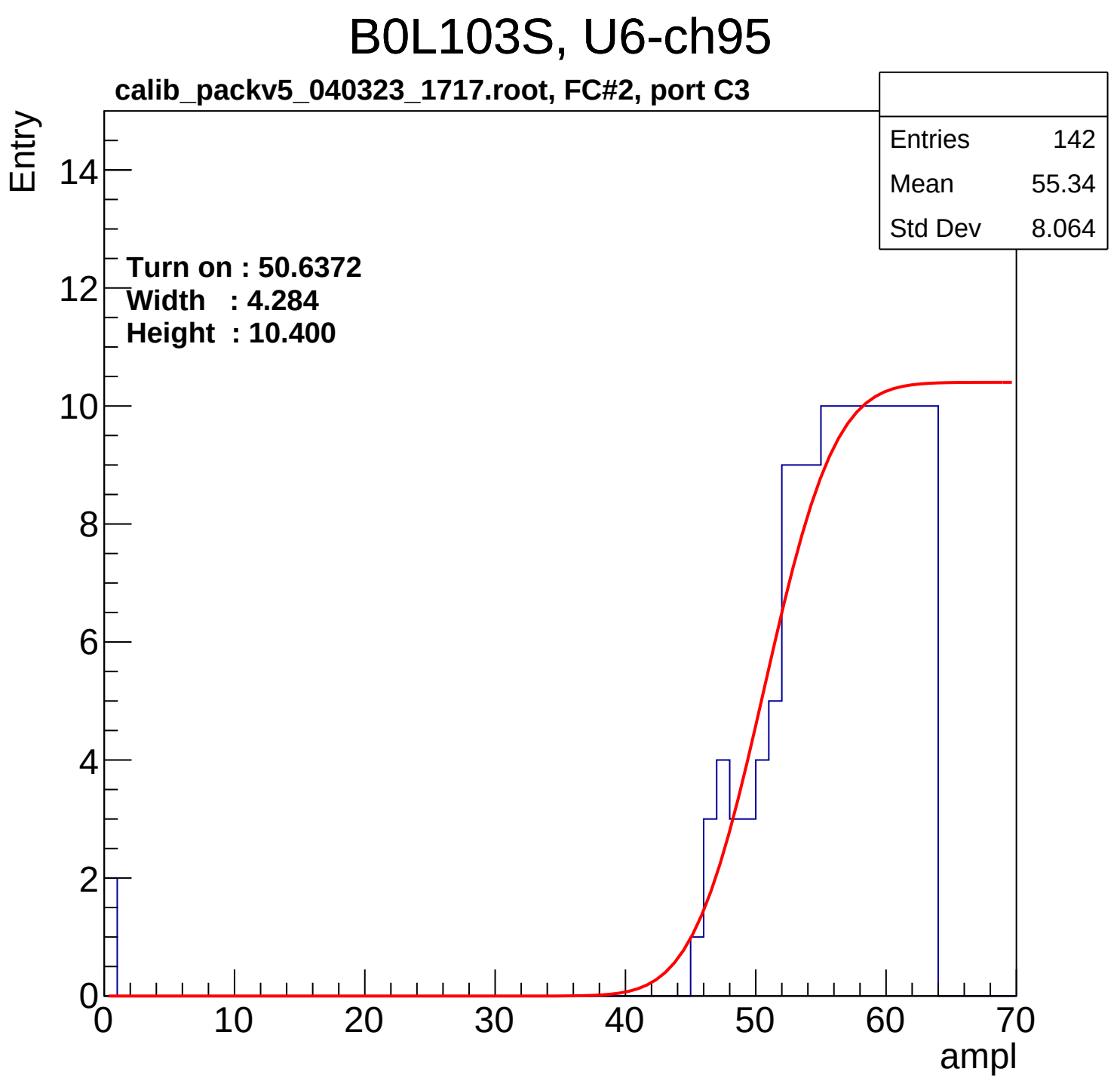
B0L103S, U6-ch95
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 55.34
Std Dev 8.064
Turn on : 50.6372
Width : 4.284
Height : 10.400
Entry
ampl
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2
4
6
8
10
12
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0
10
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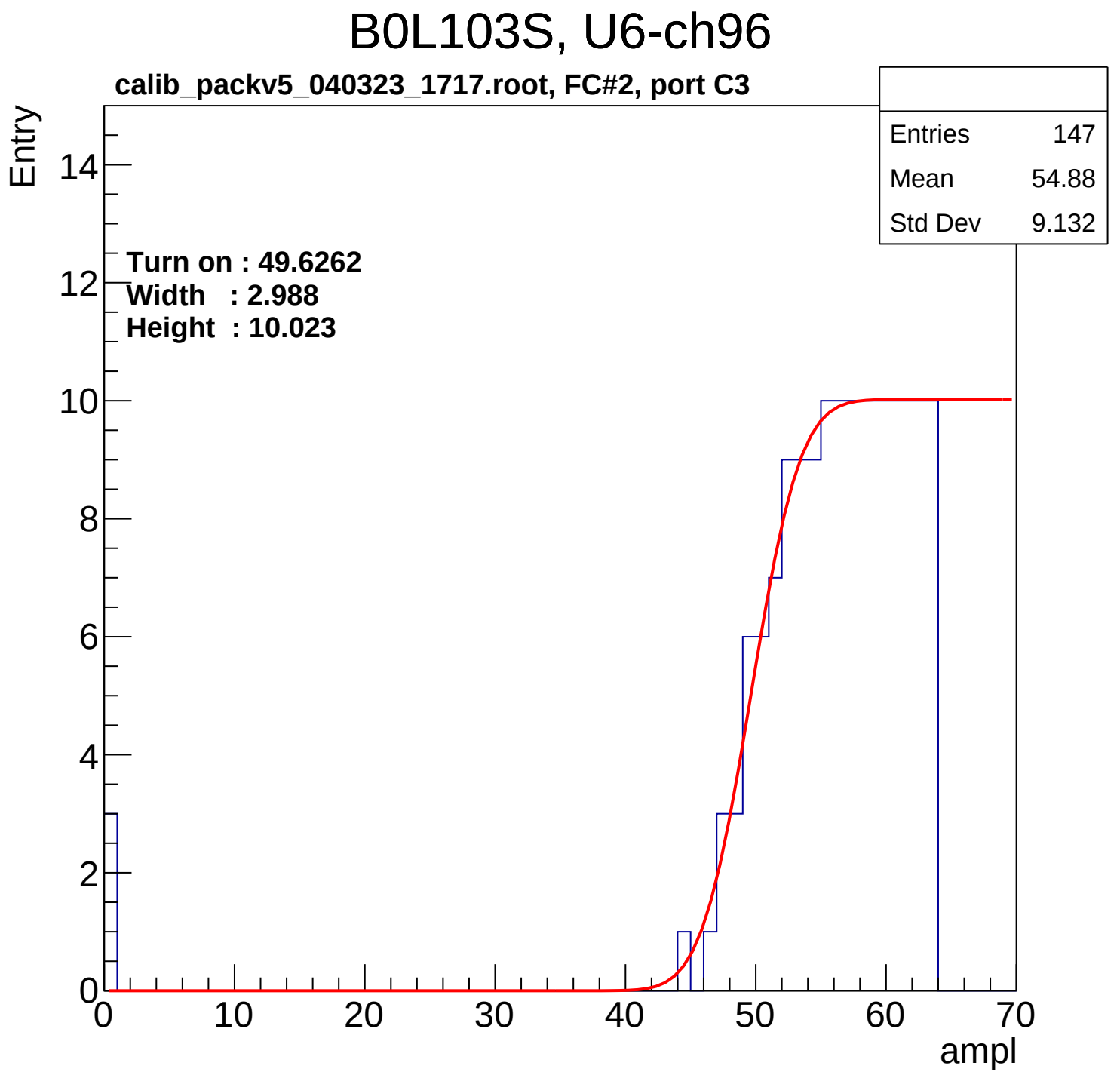
B0L103S, U6-ch96
calib_packv5_040323_1717.root, FC#2, port C3
Entries 147
Mean 54.88
Std Dev 9.132
Turn on : 49.6262
Width : 2.988
Height : 10.023
Entry
ampl
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2
4
6
8
10
12
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10
20
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60
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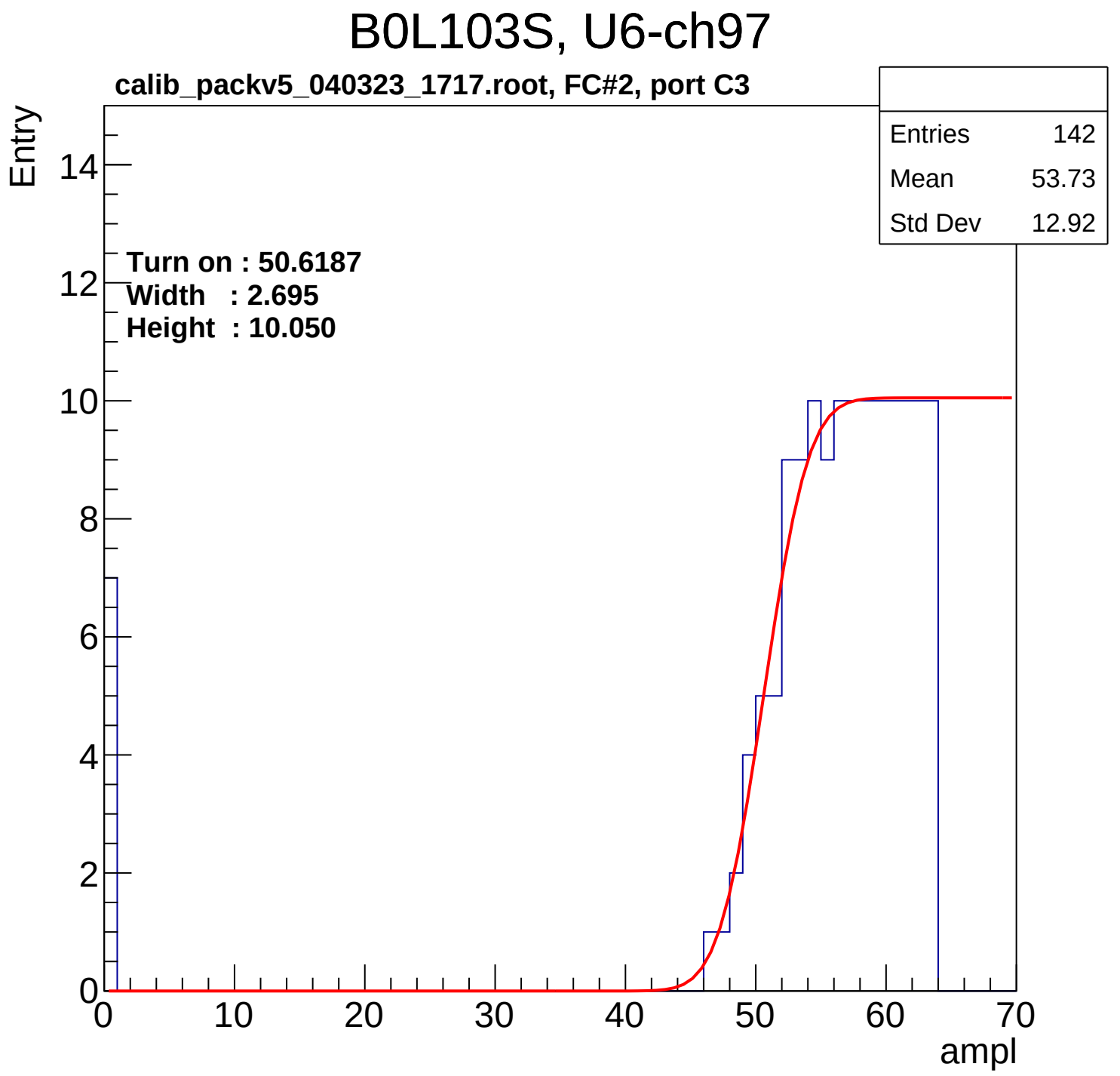
B0L103S, U6-ch97
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 53.73
Std Dev 12.92
Turn on : 50.6187
Width : 2.695
Height : 10.050
Entry
ampl
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6
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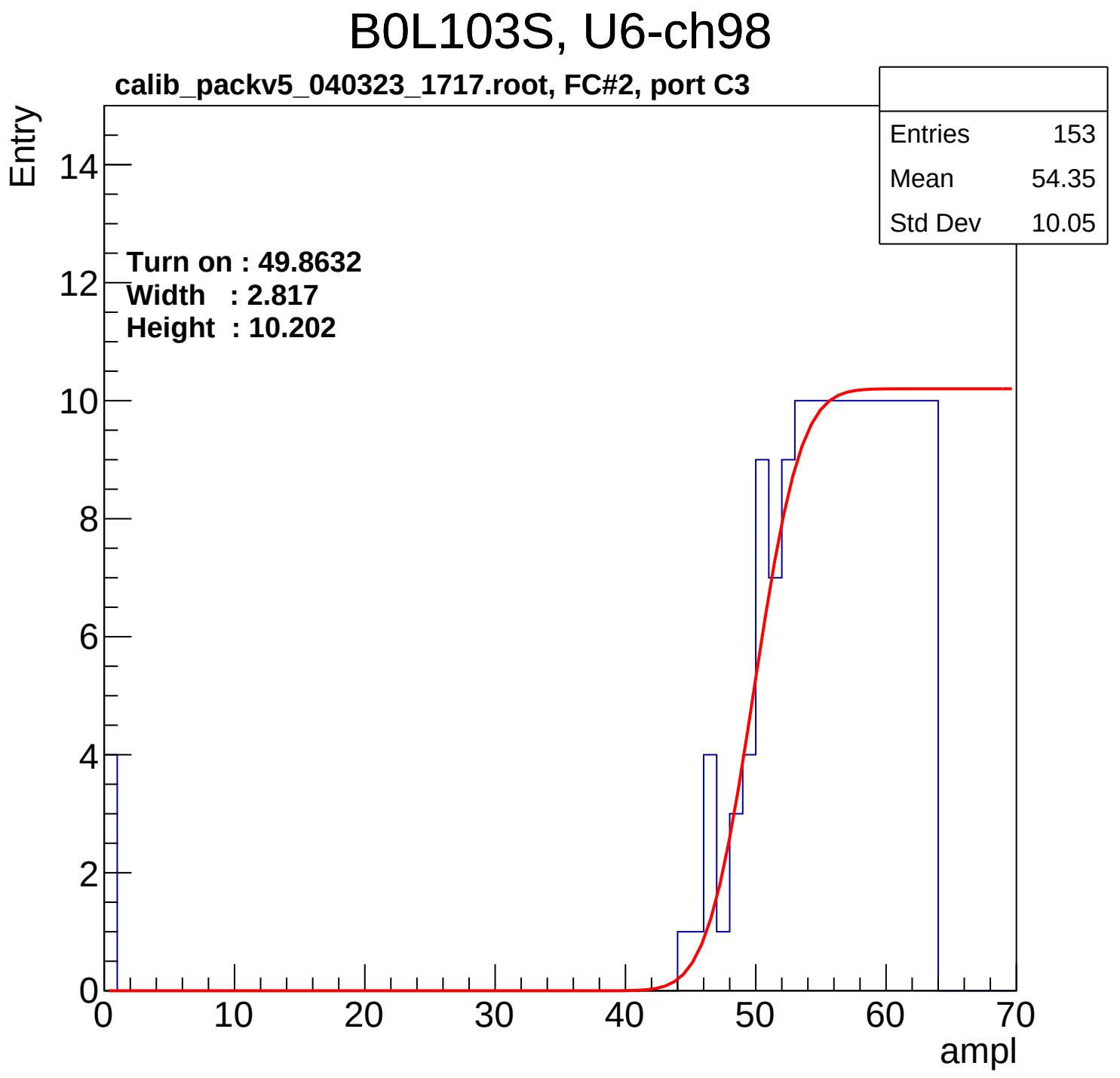
B0L103S, U6-ch98
calib_packv5_040323_1717.root, FC#2, port C3
Entries 153
Mean 54.35
Std Dev 10.05
Turn on : 49.8632
Width : 2.817
Height : 10.202
Entry
ampl
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2
4
6
8
10
12
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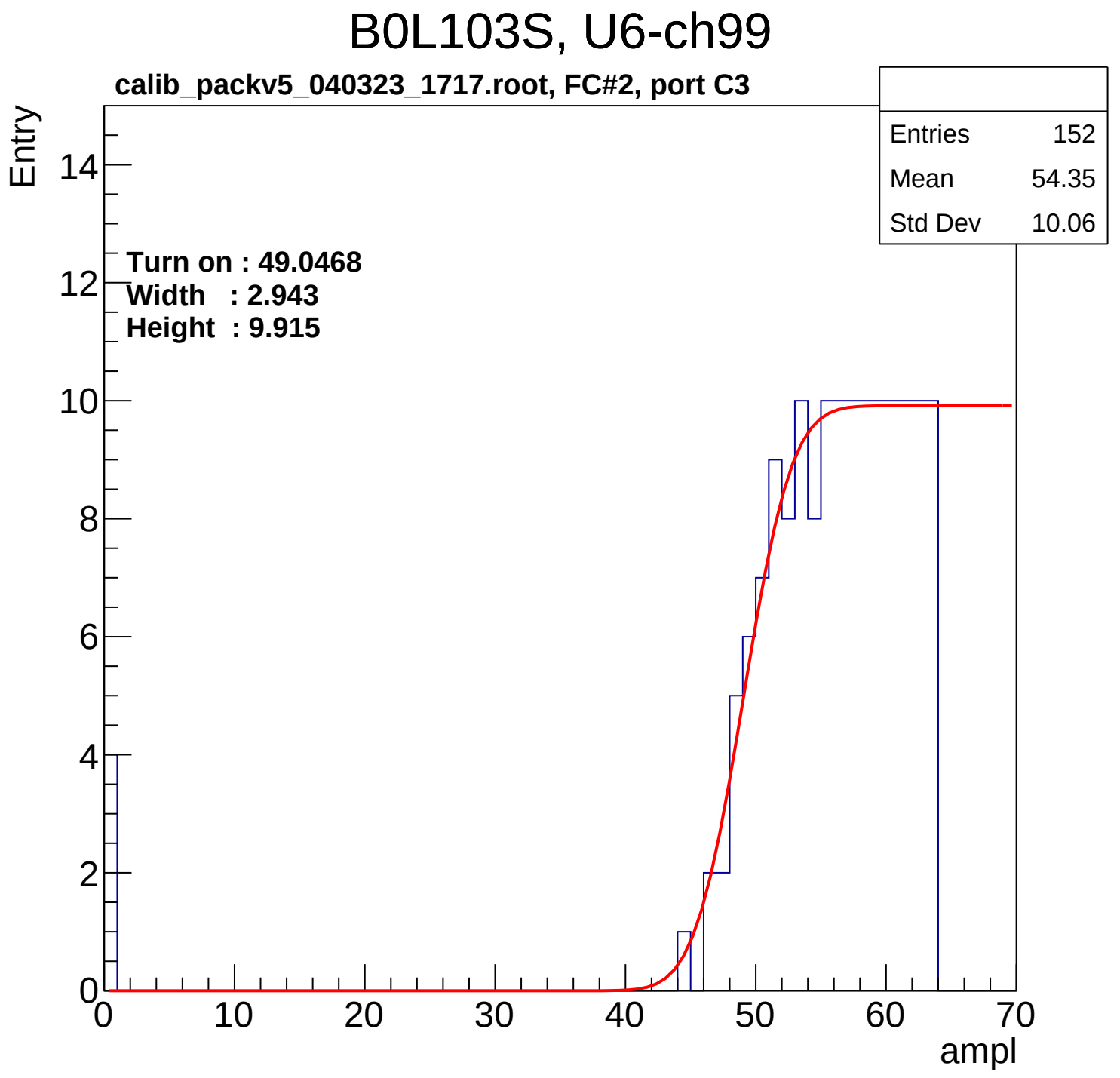
B0L103S, U6-ch99
calib_packv5_040323_1717.root, FC#2, port C3
Entries 152
Mean 54.35
Std Dev 10.06
Turn on : 49.0468
Width : 2.943
Height : 9.915
Entry
ampl
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4
6
8
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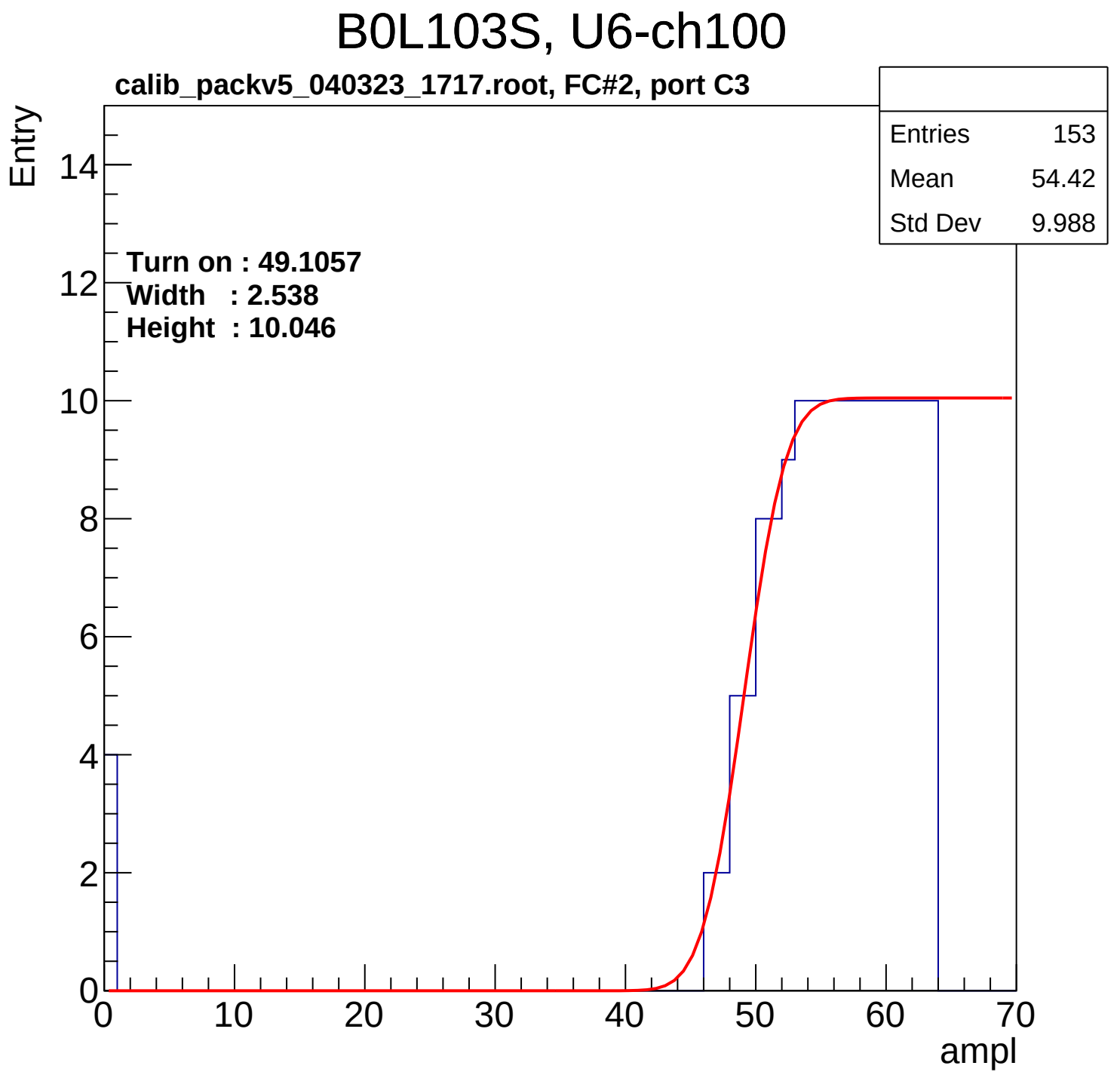
B0L103S, U6-ch100
calib_packv5_040323_1717.root, FC#2, port C3
Entries 153
Mean 54.42
Std Dev 9.988
Turn on : 49.1057
Width : 2.538
Height : 10.046
Entry
ampl
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8
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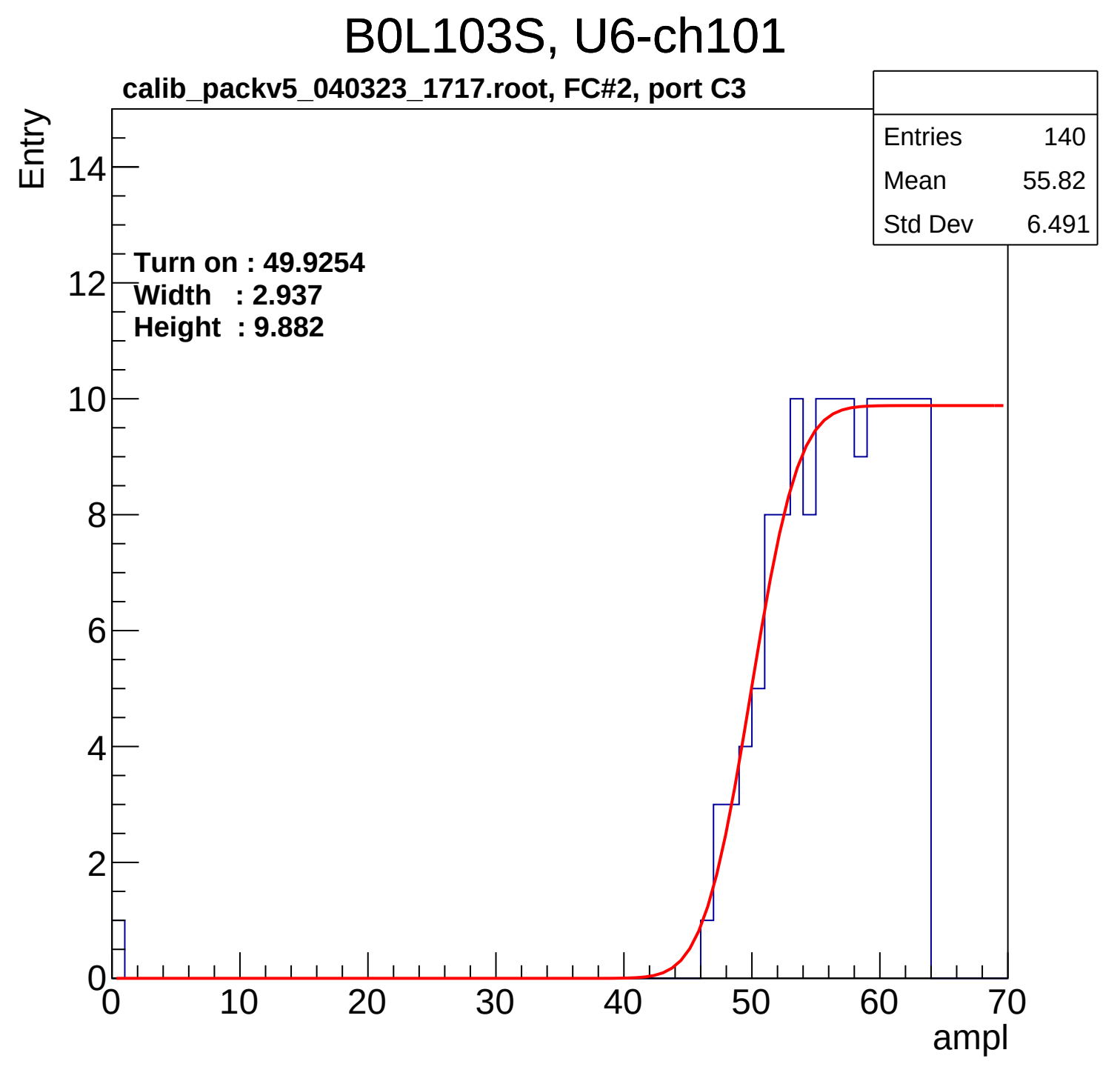
B0L103S, U6-ch101
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 55.82
Std Dev 6.491
Turn on : 49.9254
Width : 2.937
Height : 9.882
Entry
ampl
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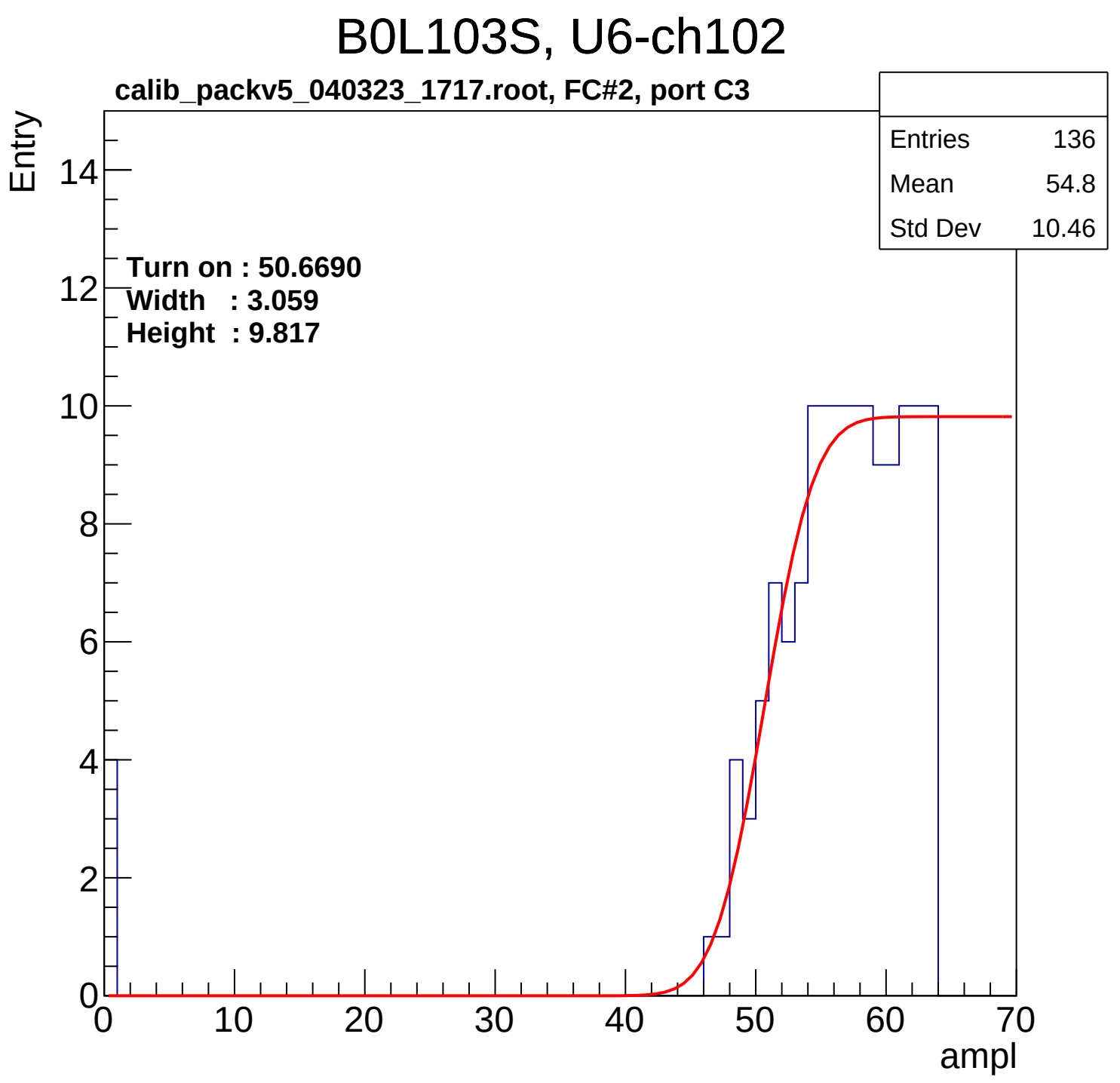
B0L103S, U6-ch102
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 54.8
Std Dev 10.46
Turn on : 50.6690
Width : 3.059
Height : 9.817
Entry
ampl
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6
8
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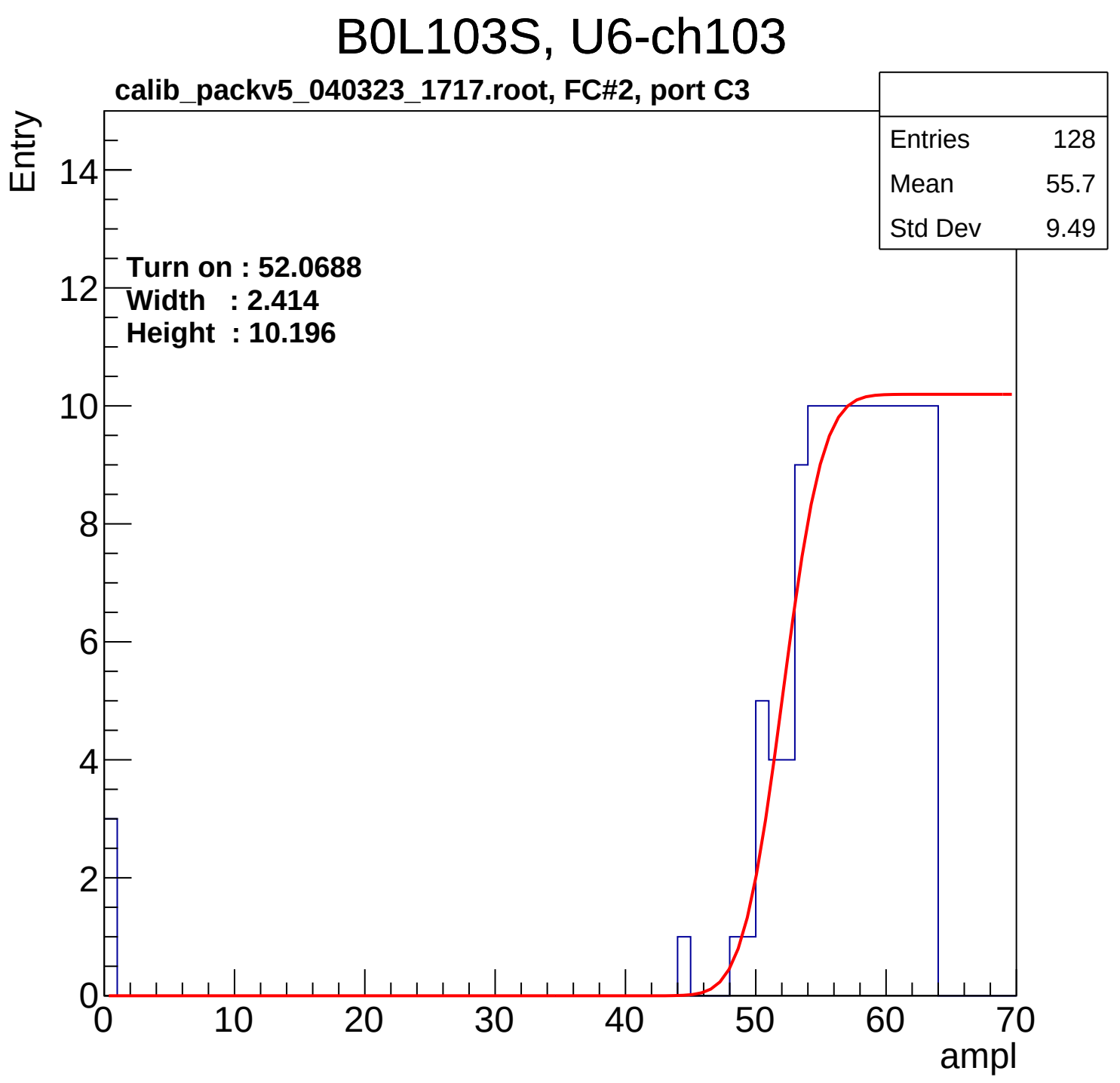
B0L103S, U6-ch103
calib_packv5_040323_1717.root, FC#2, port C3
Entries 128
Mean 55.7
Std Dev 9.49
Turn on : 52.0688
Width : 2.414
Height : 10.196
Entry
ampl
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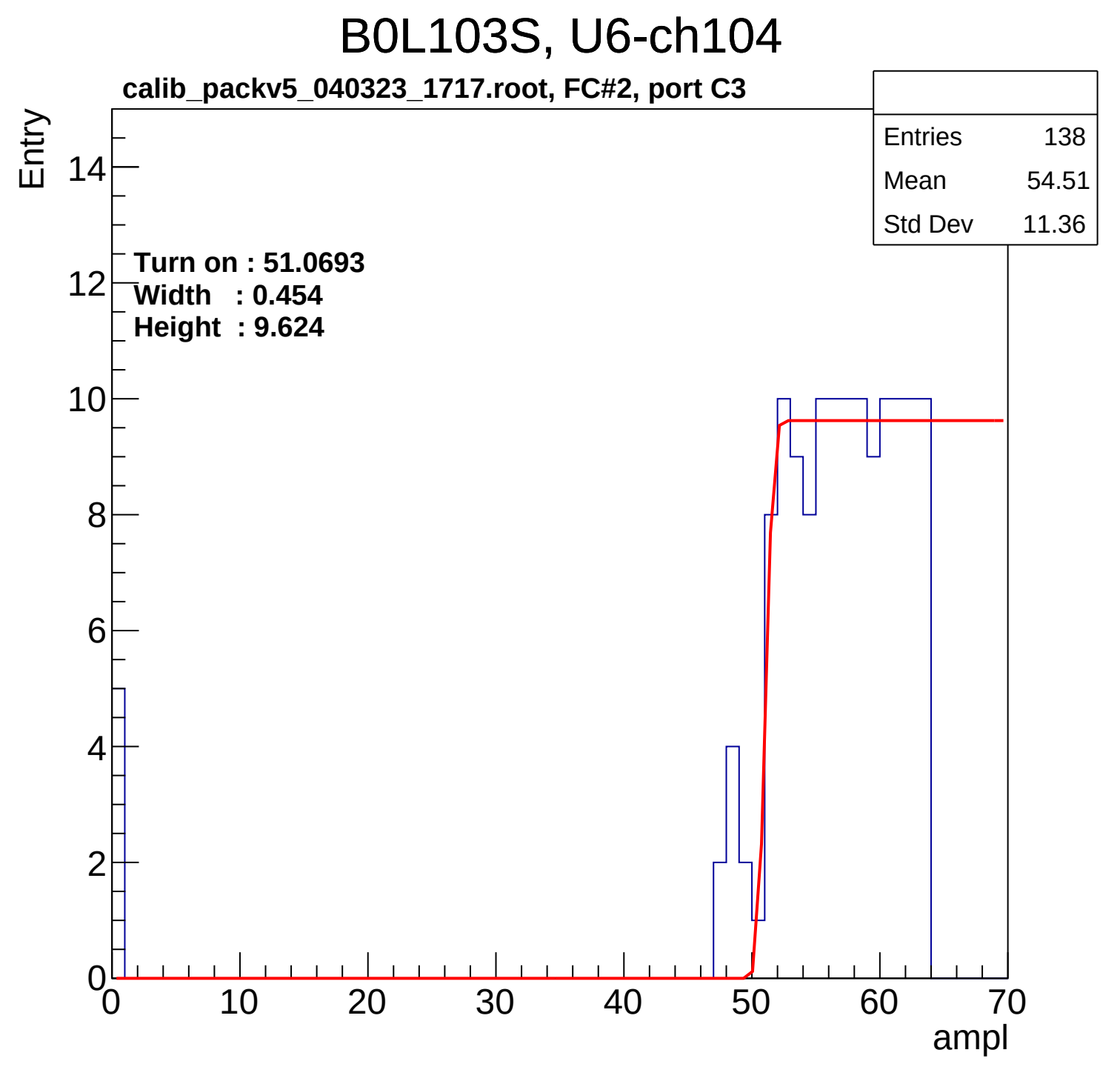
B0L103S, U6-ch104
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 54.51
Std Dev 11.36
Turn on : 51.0693
Width : 0.454
Height : 9.624
Entry
ampl
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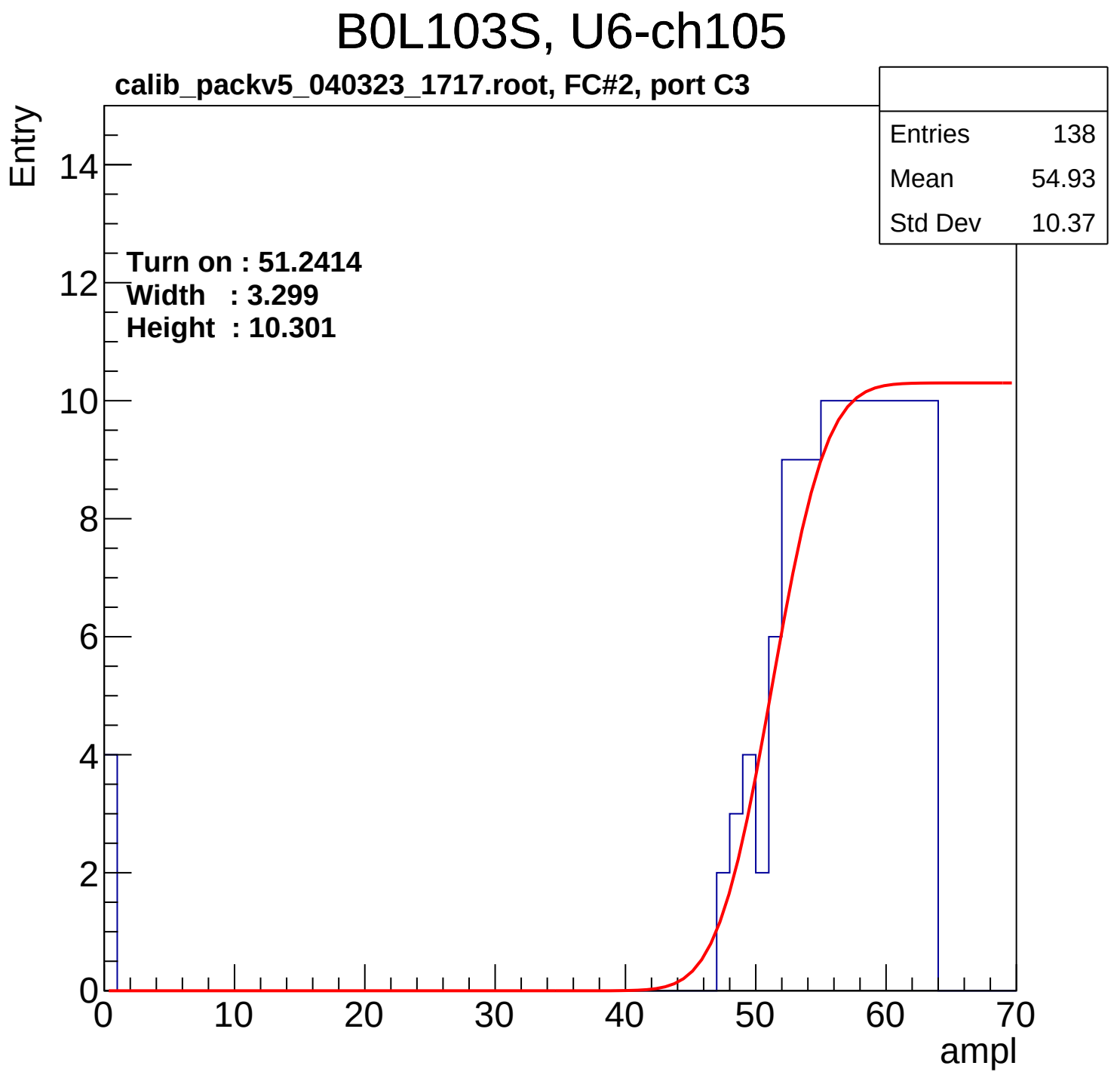
B0L103S, U6-ch105
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 54.93
Std Dev 10.37
Turn on : 51.2414
Width : 3.299
Height : 10.301
Entry
ampl
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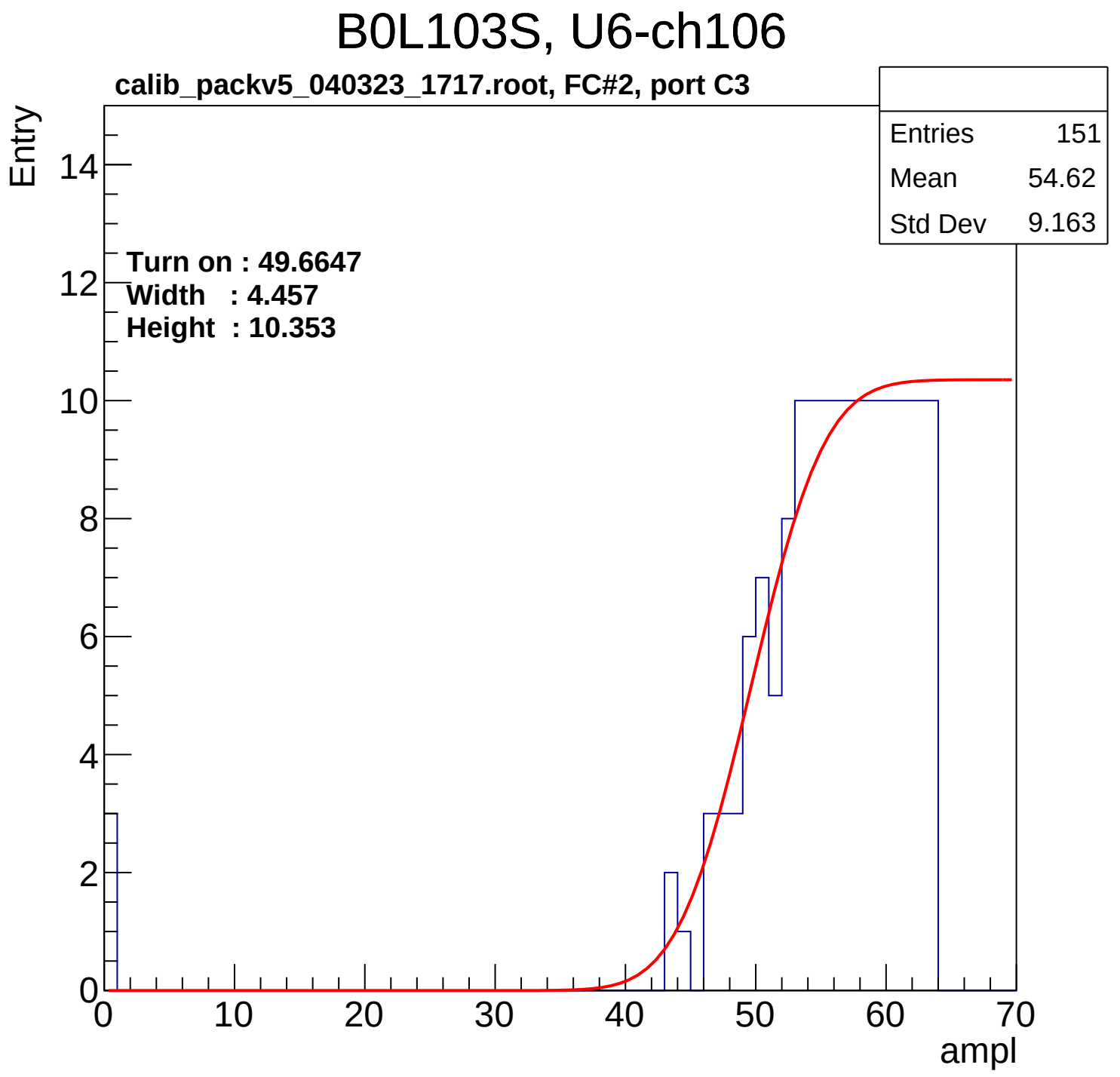
B0L103S, U6-ch106
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 54.62
Std Dev 9.163
Turn on : 49.6647
Width : 4.457
Height : 10.353
Entry
ampl
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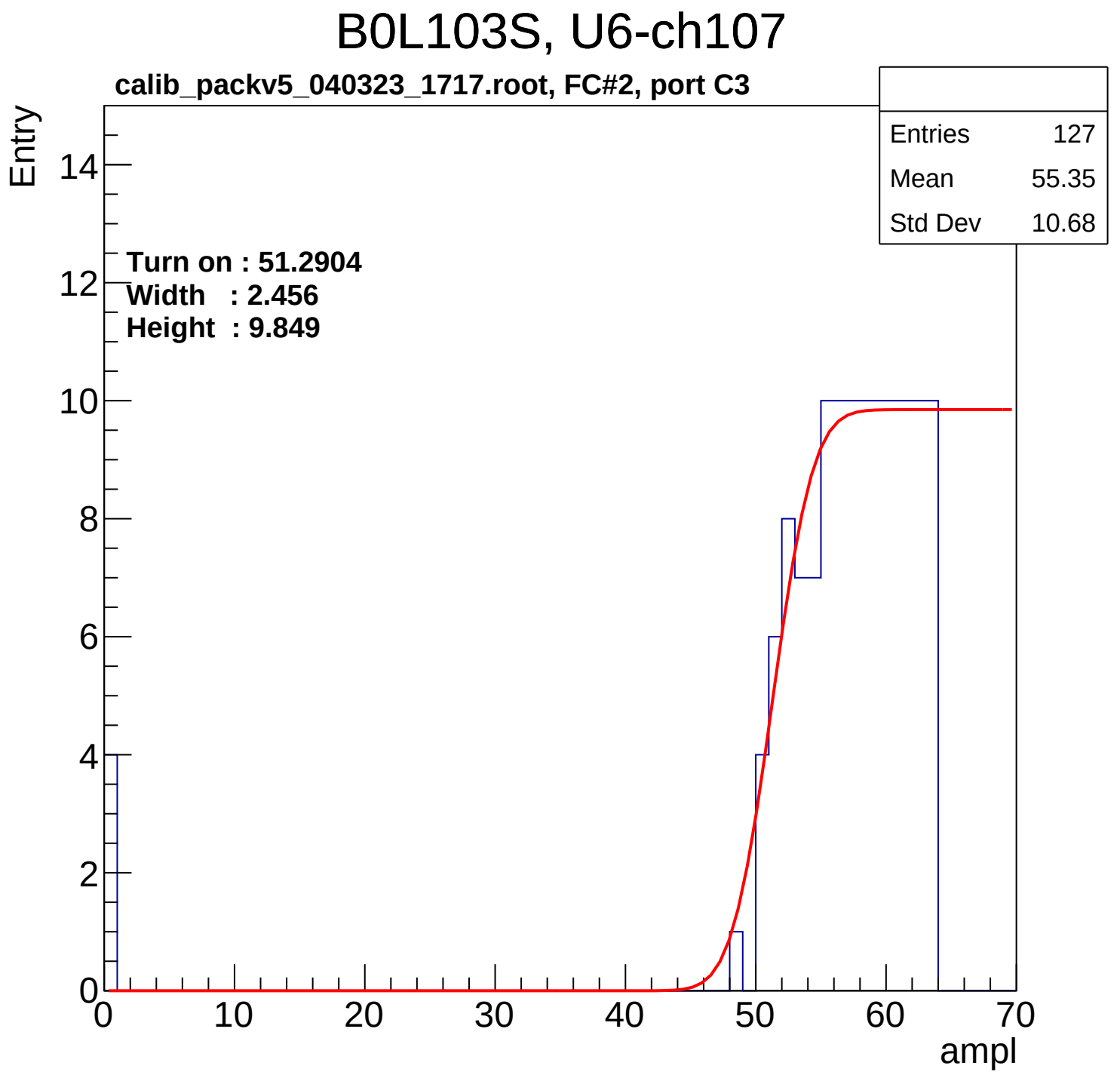
B0L103S, U6-ch107
calib_packv5_040323_1717.root, FC#2, port C3
Entries 127
Mean 55.35
Std Dev 10.68
Turn on : 51.2904
Width : 2.456
Height : 9.849
Entry
ampl
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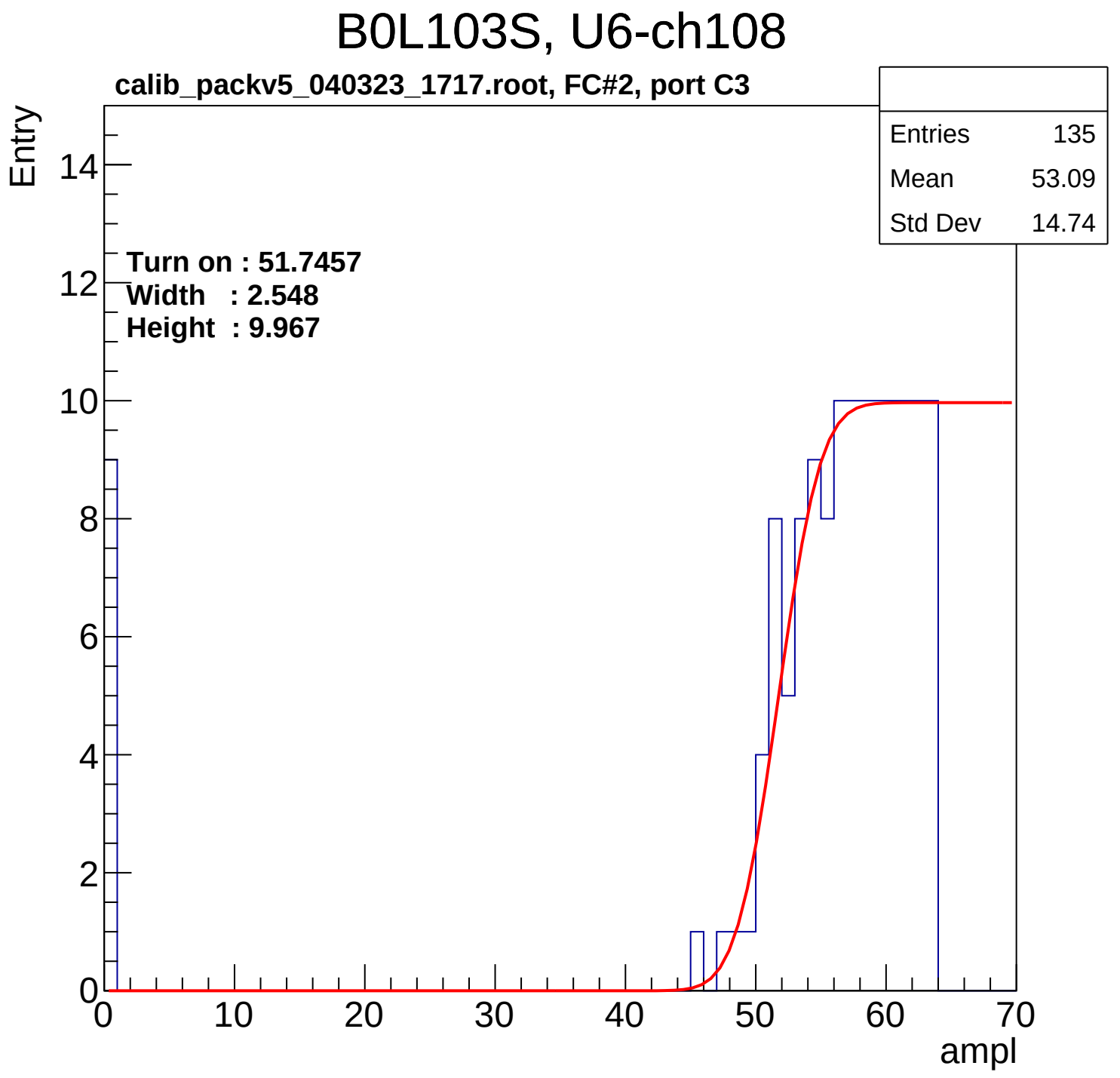
B0L103S, U6-ch108
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 53.09
Std Dev 14.74
Turn on : 51.7457
Width : 2.548
Height : 9.967
Entry
ampl
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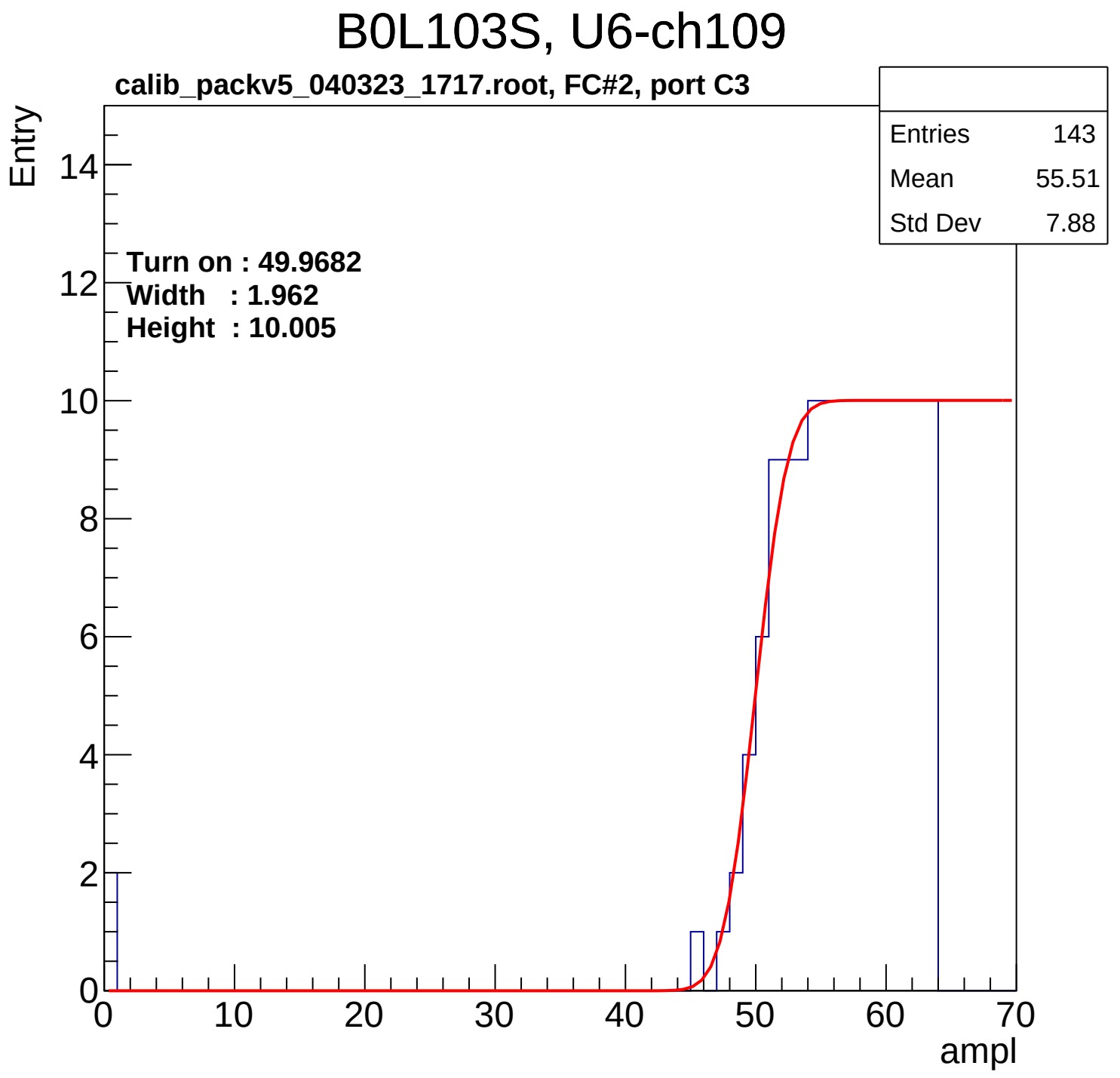
B0L103S, U6-ch109
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 55.51
Std Dev 7.88
Turn on : 49.9682
Width : 1.962
Height : 10.005
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ampl
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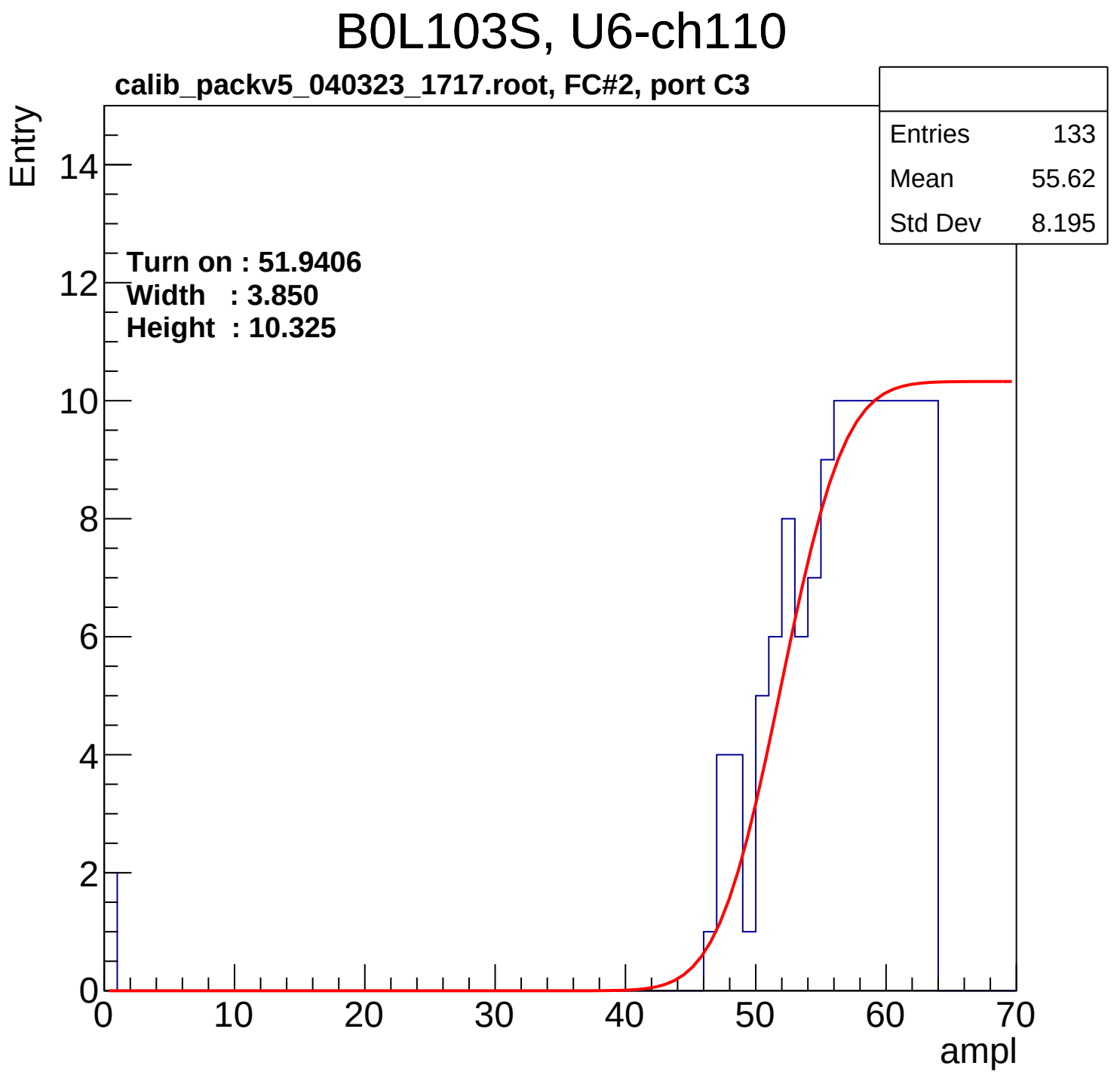
B0L103S, U6-ch110
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 55.62
Std Dev 8.195
Turn on : 51.9406
Width : 3.850
Height : 10.325
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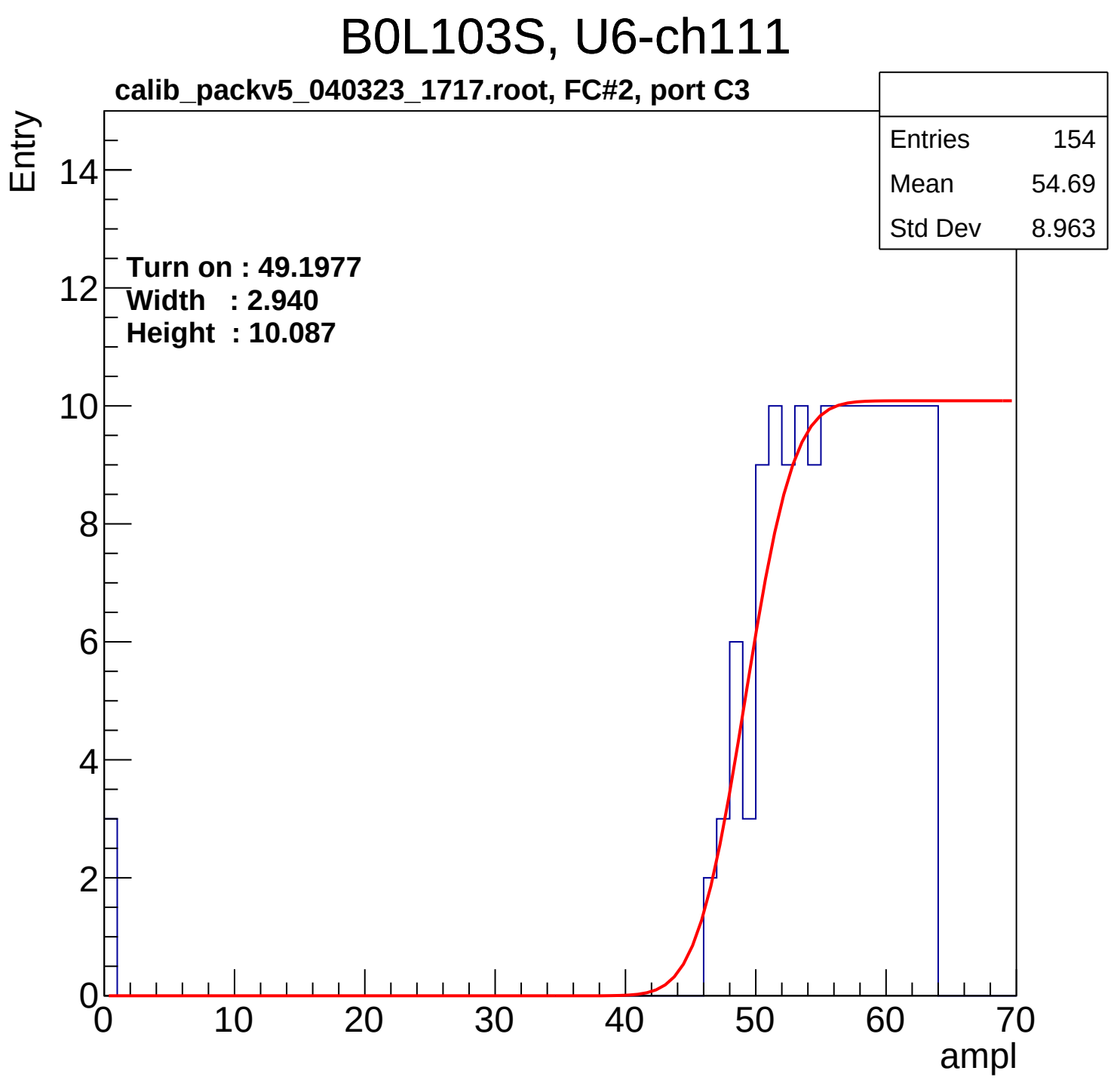
B0L103S, U6-ch111
calib_packv5_040323_1717.root, FC#2, port C3
Entries 154
Mean 54.69
Std Dev 8.963
Turn on : 49.1977
Width : 2.940
Height : 10.087
Entry
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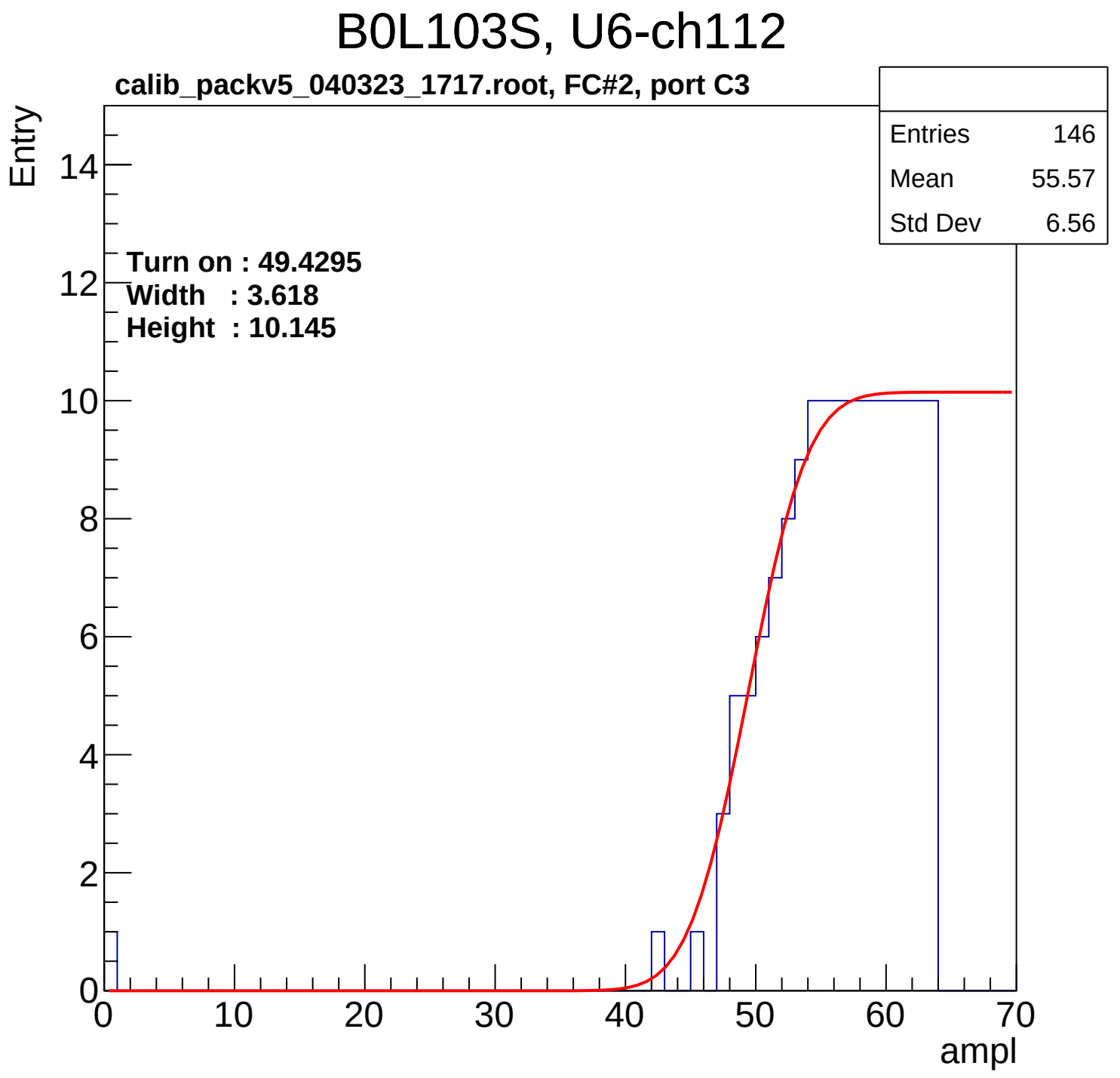
B0L103S, U6-ch112
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 55.57
Std Dev 6.56
Turn on : 49.4295
Width : 3.618
Height : 10.145
Entry
ampl
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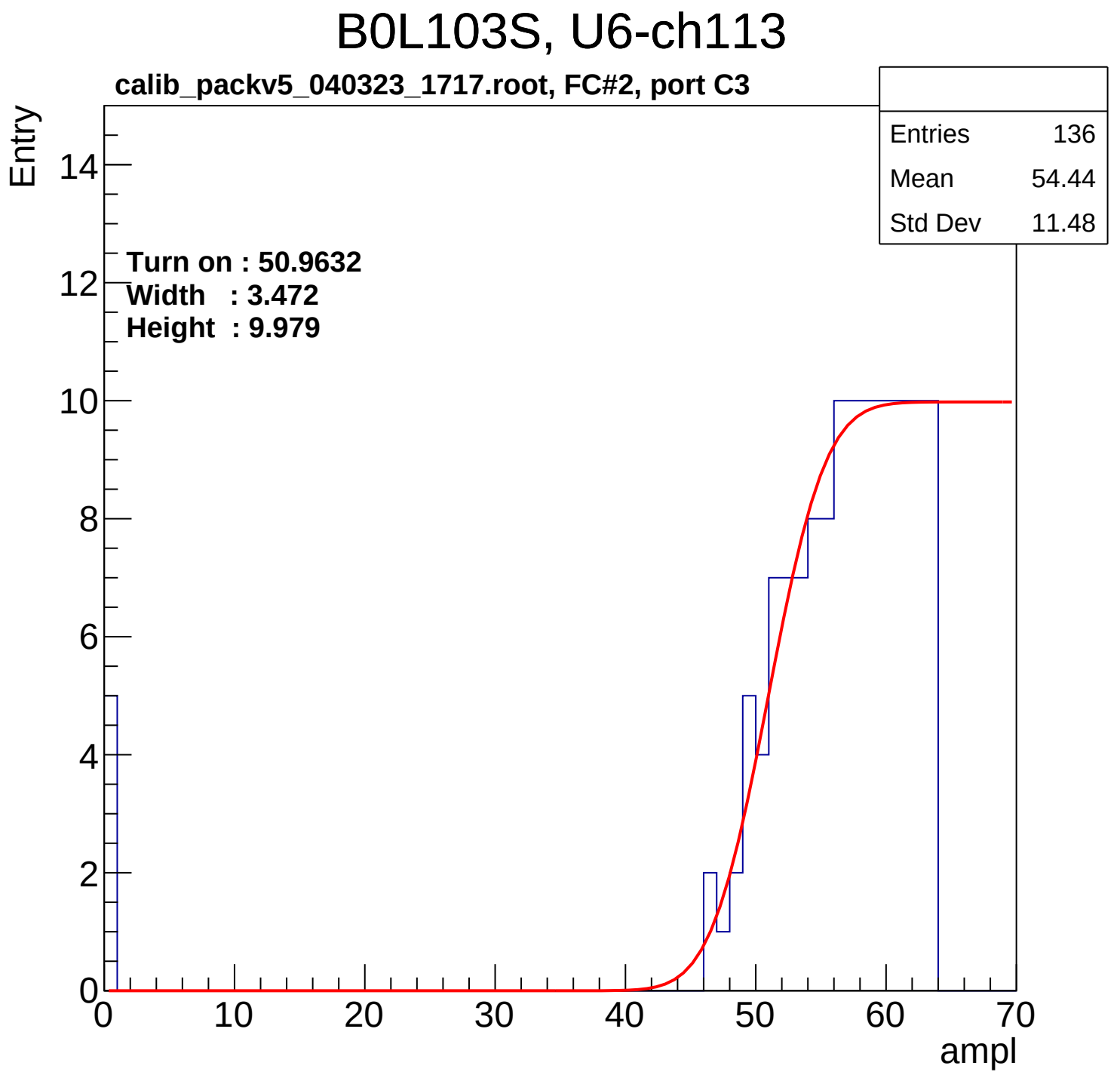
B0L103S, U6-ch113
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 54.44
Std Dev 11.48
Turn on : 50.9632
Width : 3.472
Height : 9.979
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ampl
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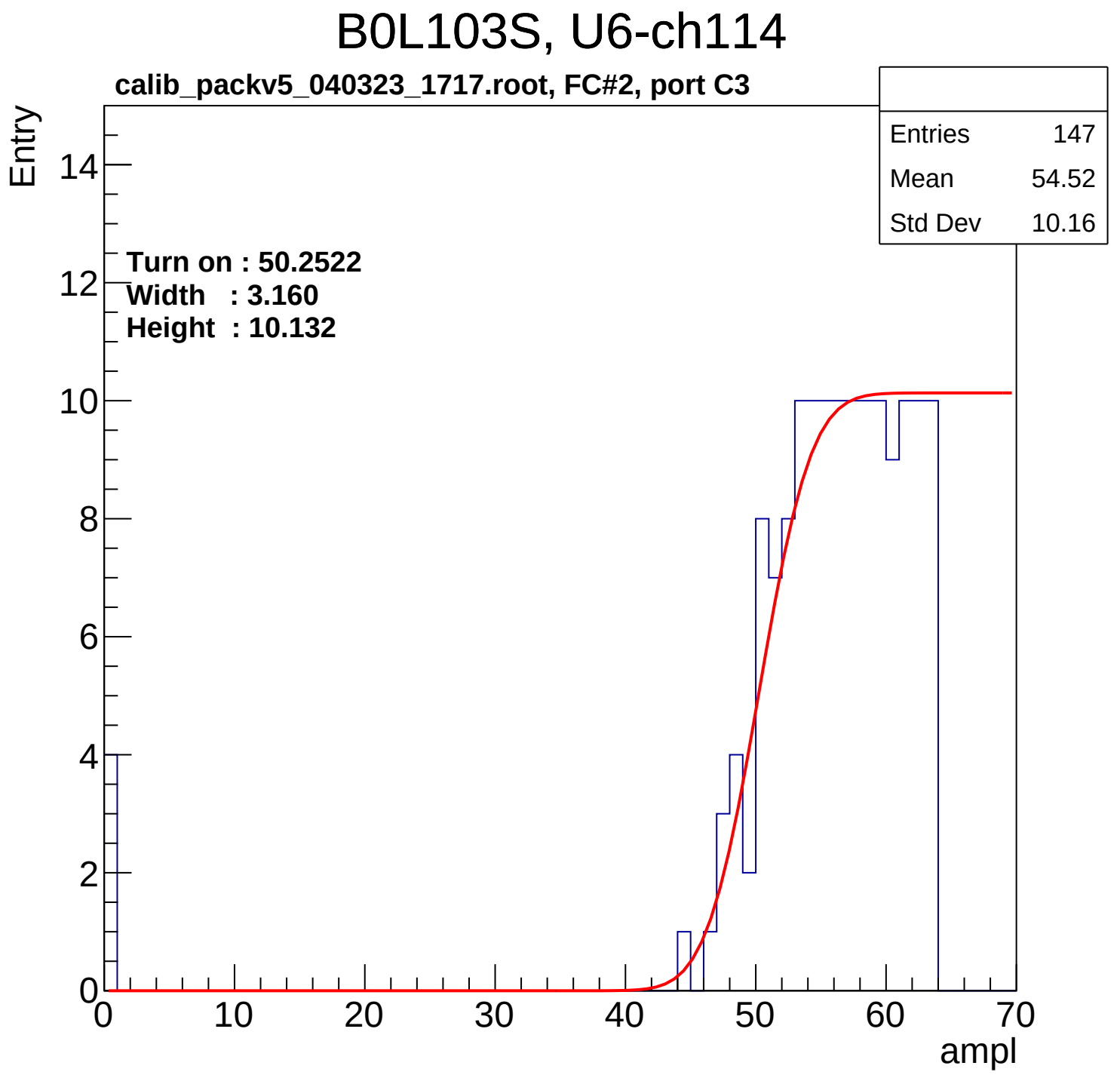
B0L103S, U6-ch114
calib_packv5_040323_1717.root, FC#2, port C3
Entries 147
Mean 54.52
Std Dev 10.16
Turn on : 50.2522
Width : 3.160
Height : 10.132
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ampl
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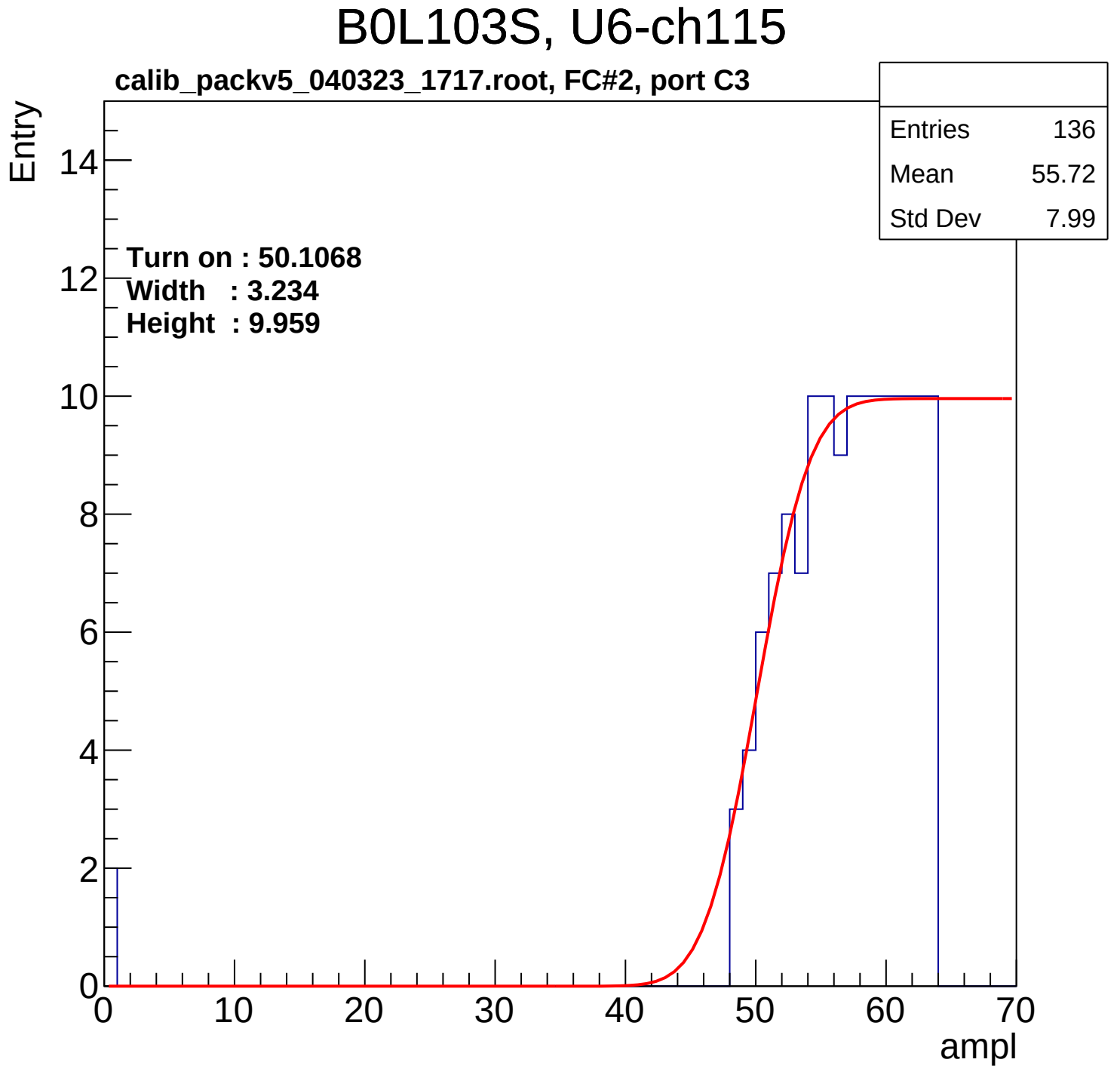
B0L103S, U6-ch115
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 55.72
Std Dev 7.99
Turn on : 50.1068
Width : 3.234
Height : 9.959
Entry
ampl
0
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4
6
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20
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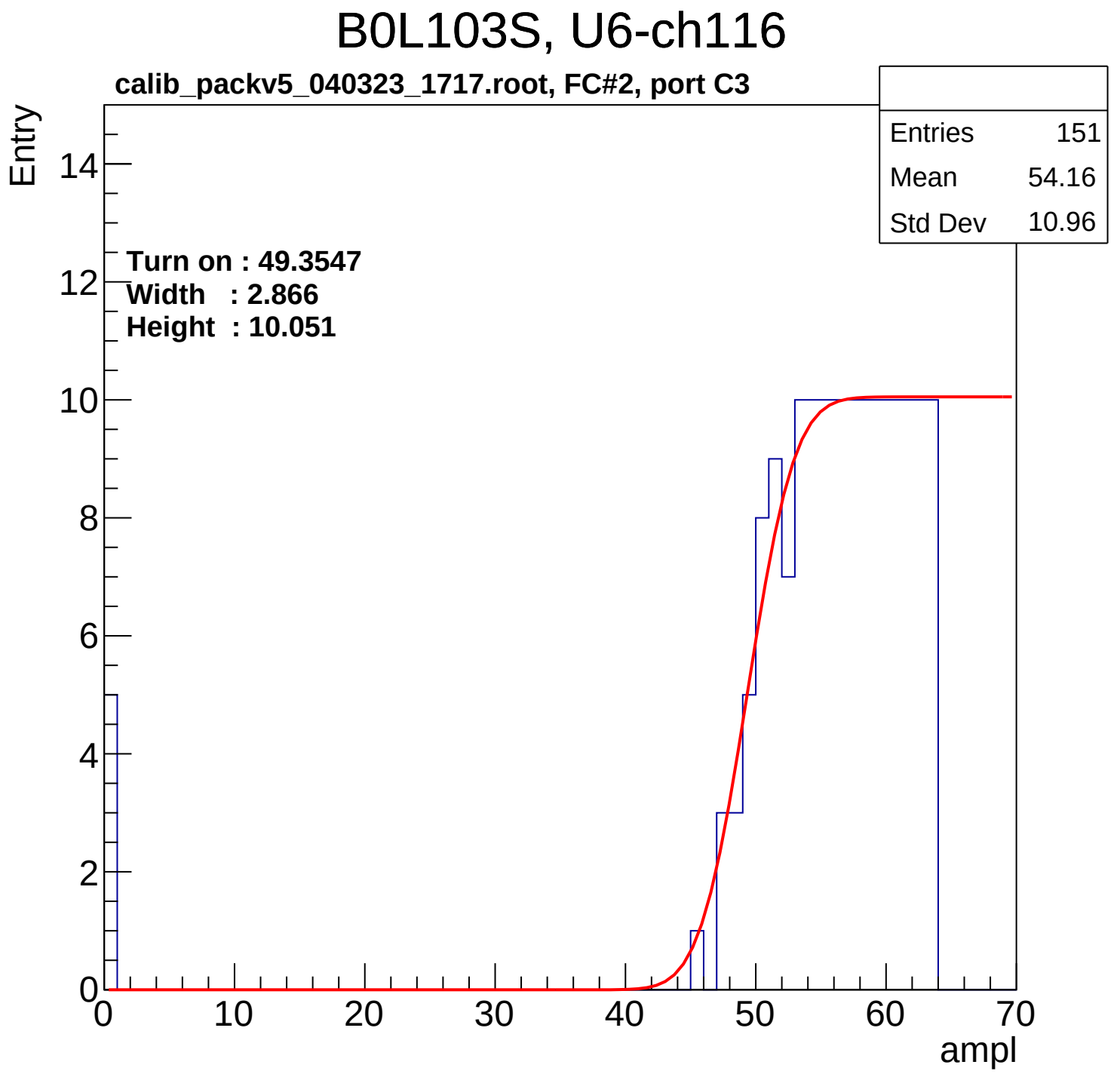
B0L103S, U6-ch116
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 54.16
Std Dev 10.96
Turn on : 49.3547
Width : 2.866
Height : 10.051
Entry
ampl
0
2
4
6
8
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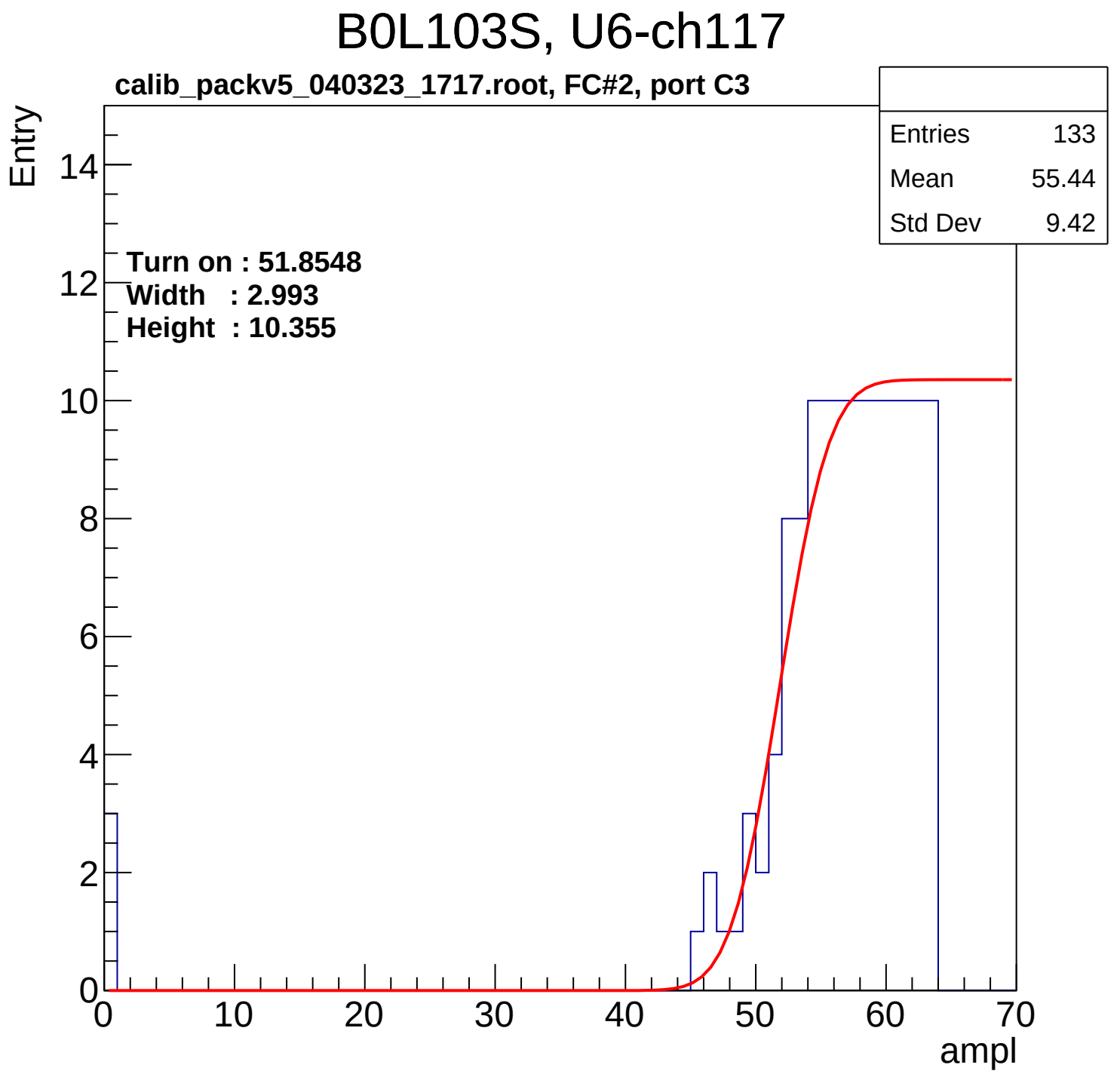
B0L103S, U6-ch117
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 55.44
Std Dev 9.42
Turn on : 51.8548
Width : 2.993
Height : 10.355
Entry
ampl
0
2
4
6
8
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12
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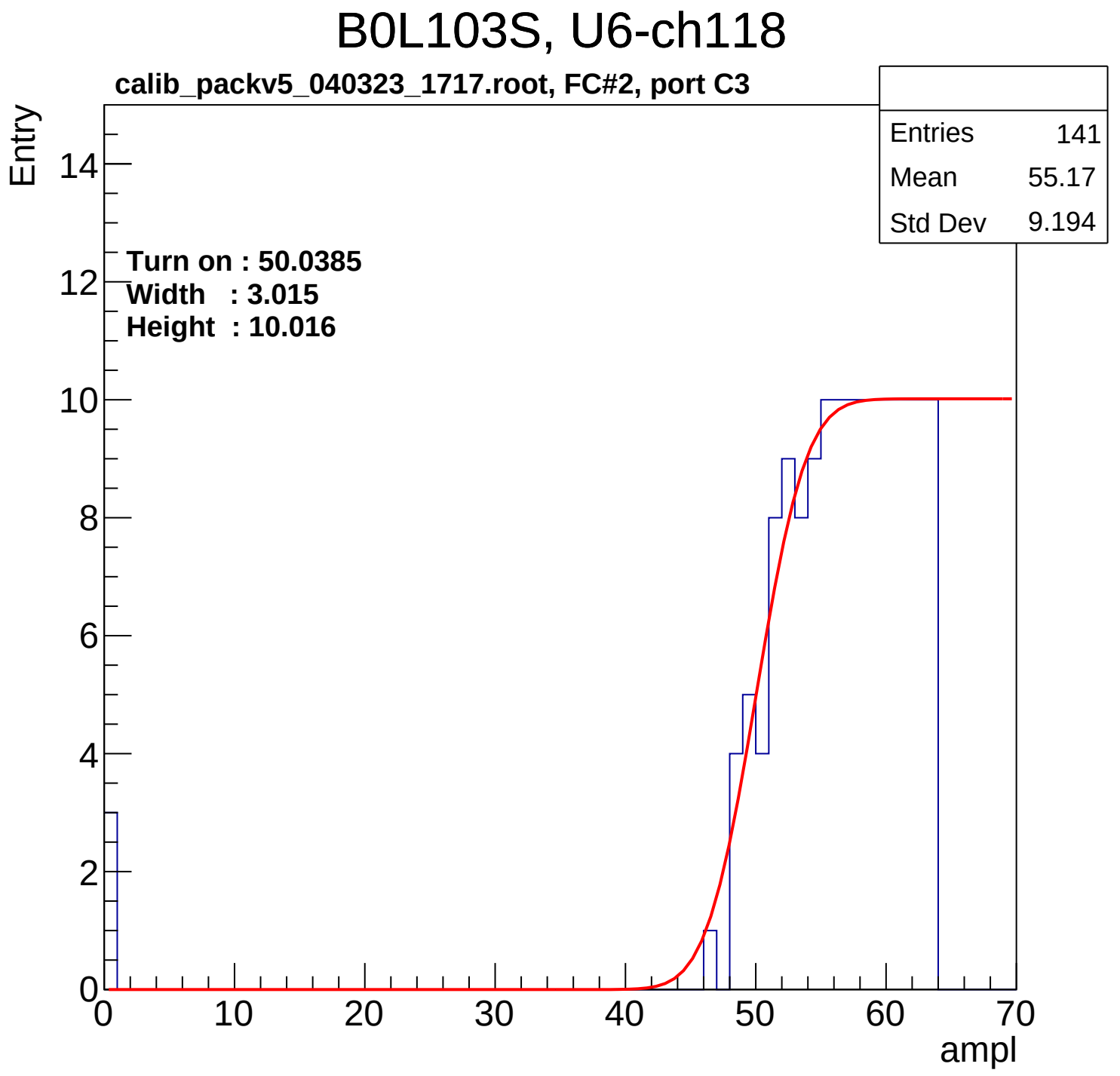
B0L103S, U6-ch118
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 55.17
Std Dev 9.194
Turn on : 50.0385
Width : 3.015
Height : 10.016
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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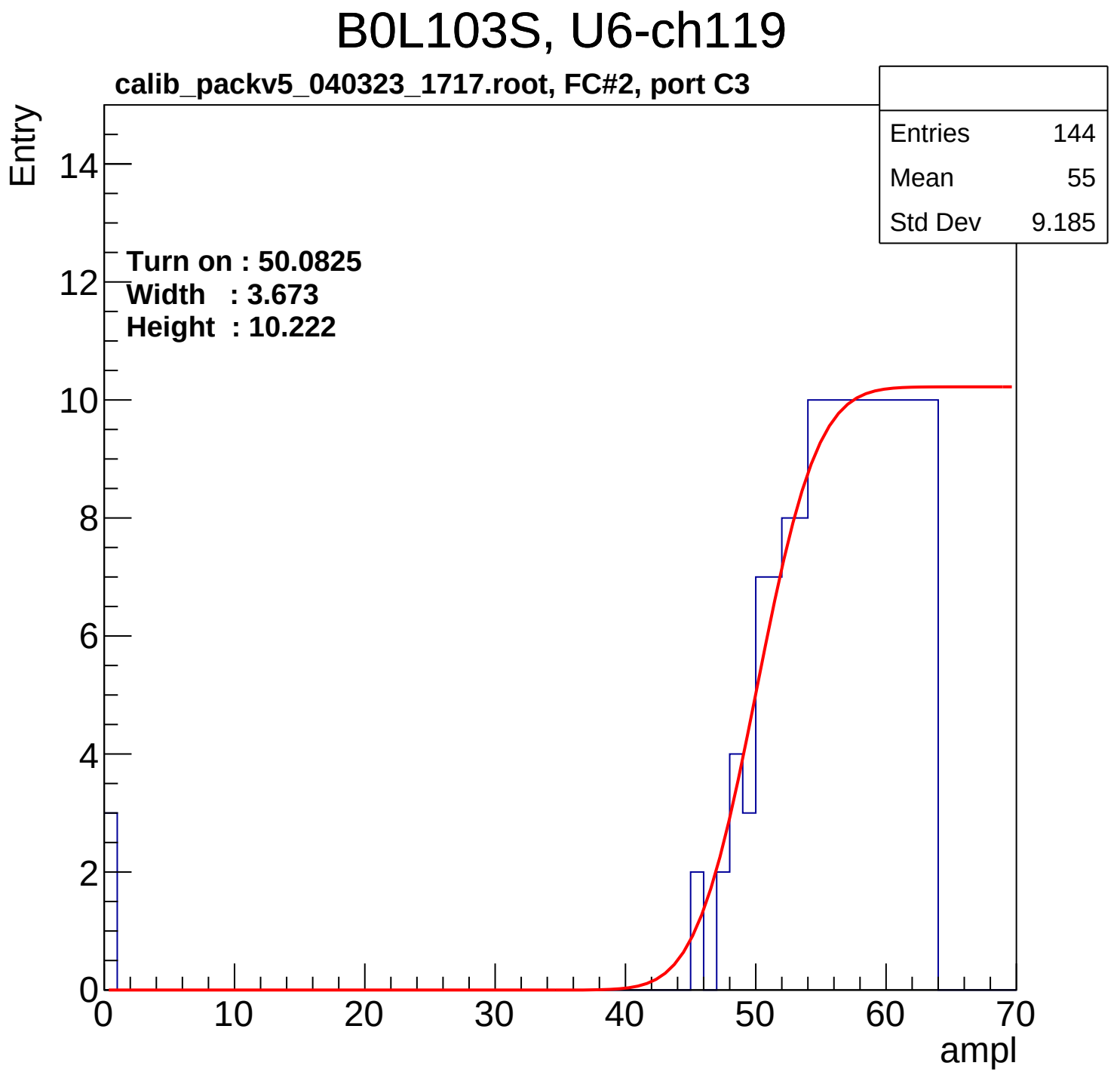
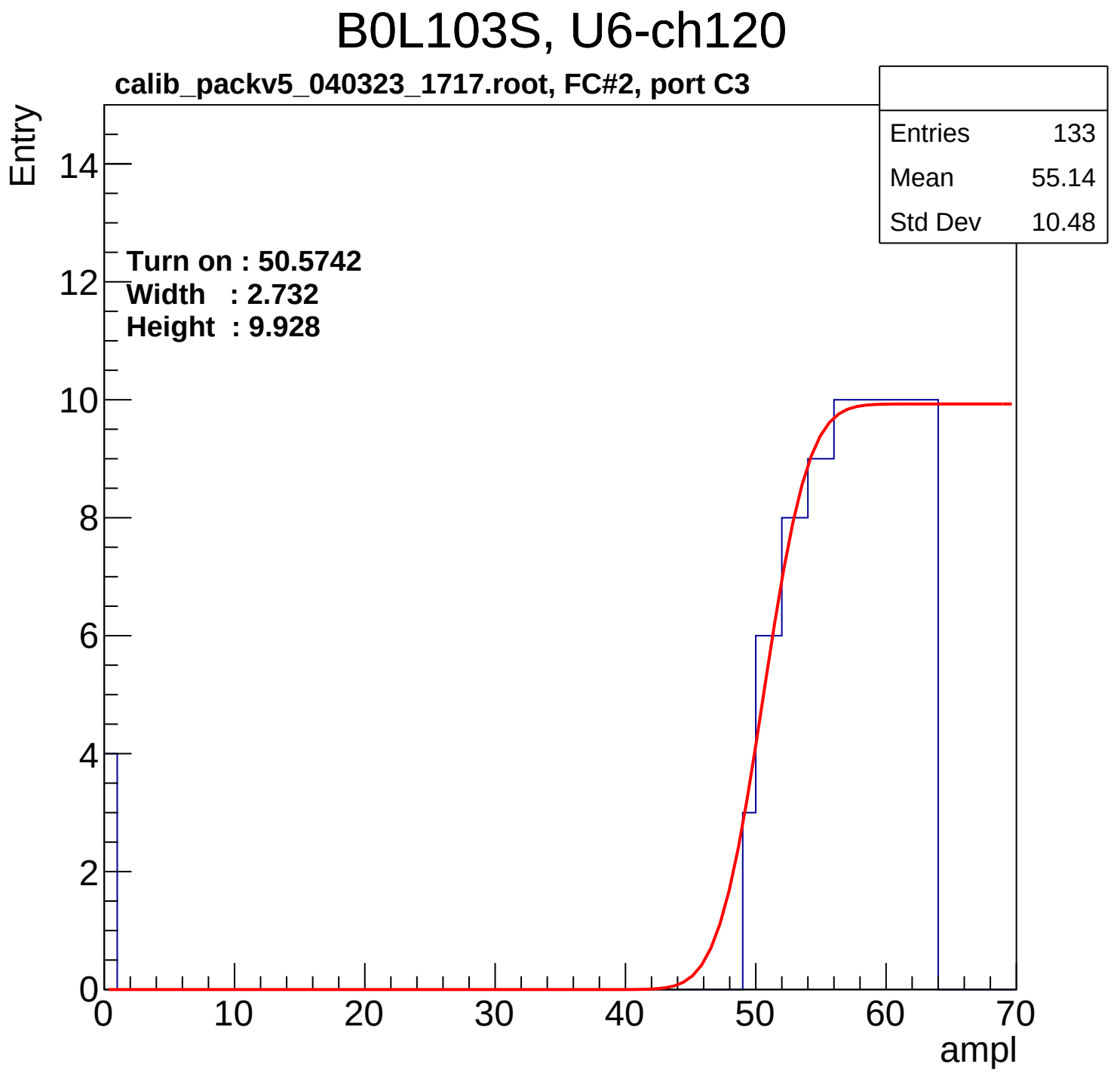

B0L103S, U6-ch119
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 55
Std Dev 9.185
Turn on : 50.0825
Width : 3.673
Height : 10.222
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U6-ch120
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 55.14
Std Dev 10.48
Turn on : 50.5742
Width : 2.732
Height : 9.928
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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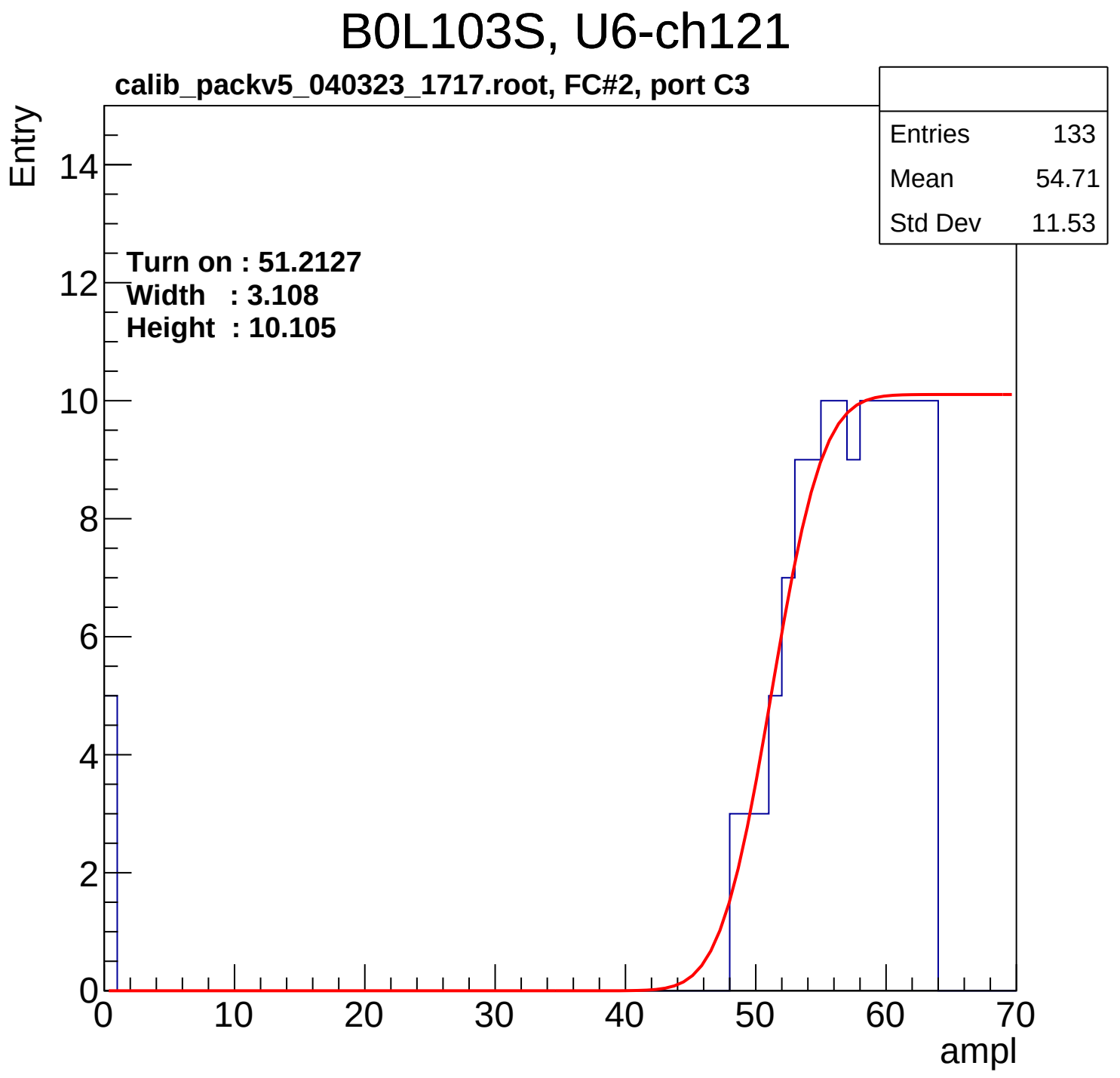
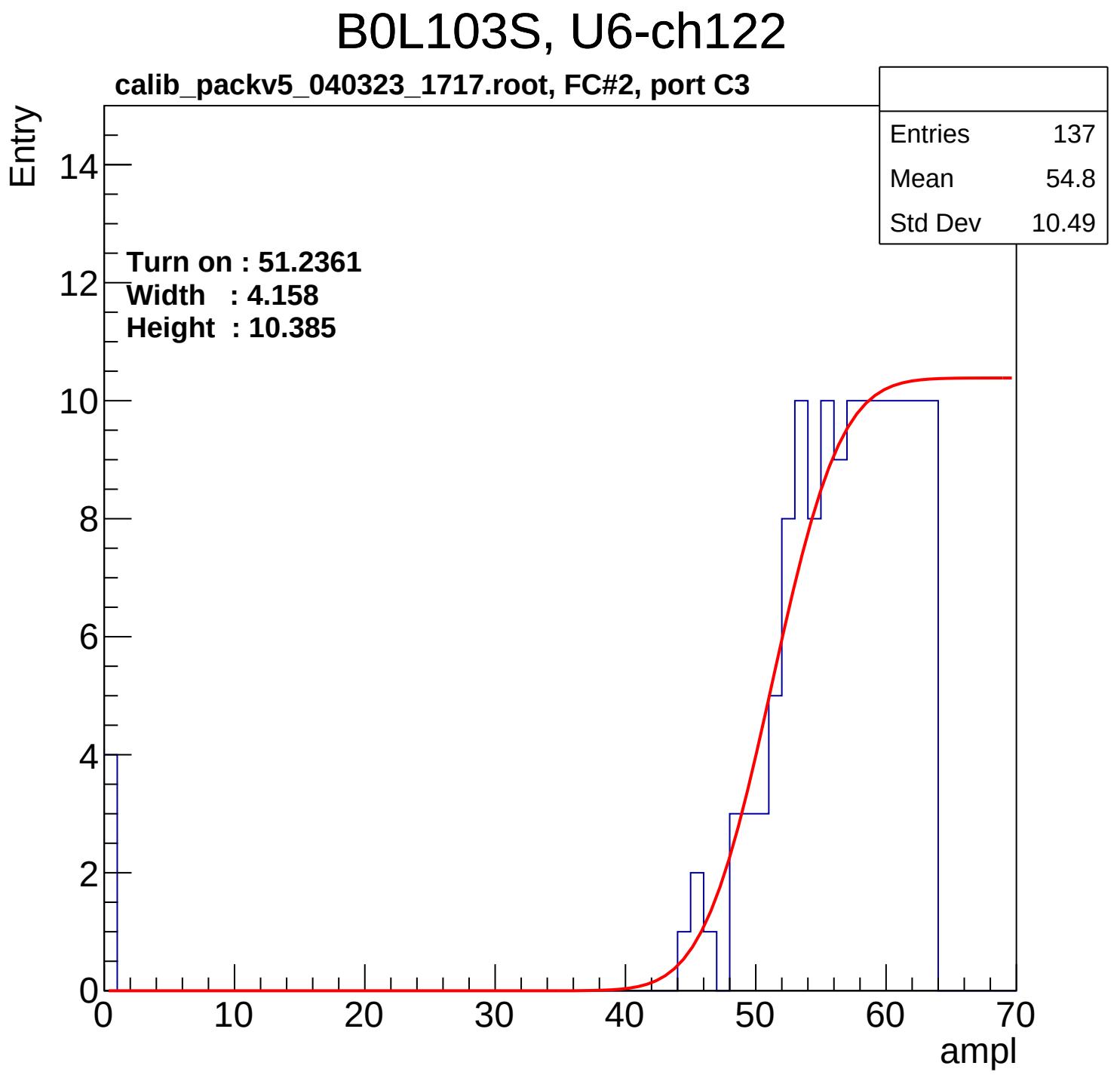

B0L103S, U6-ch121
calib_packv5_040323_1717.root, FC#2, port C3
Entries 133
Mean 54.71
Std Dev 11.53
Turn on : 51.2127
Width : 3.108
Height : 10.105
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U6-ch122
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 54.8
Std Dev 10.49
Turn on : 51.2361
Width : 4.158
Height : 10.385
Entry
ampl
0
2
4
6
8
10
12
14
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10
20
30
40
50
60
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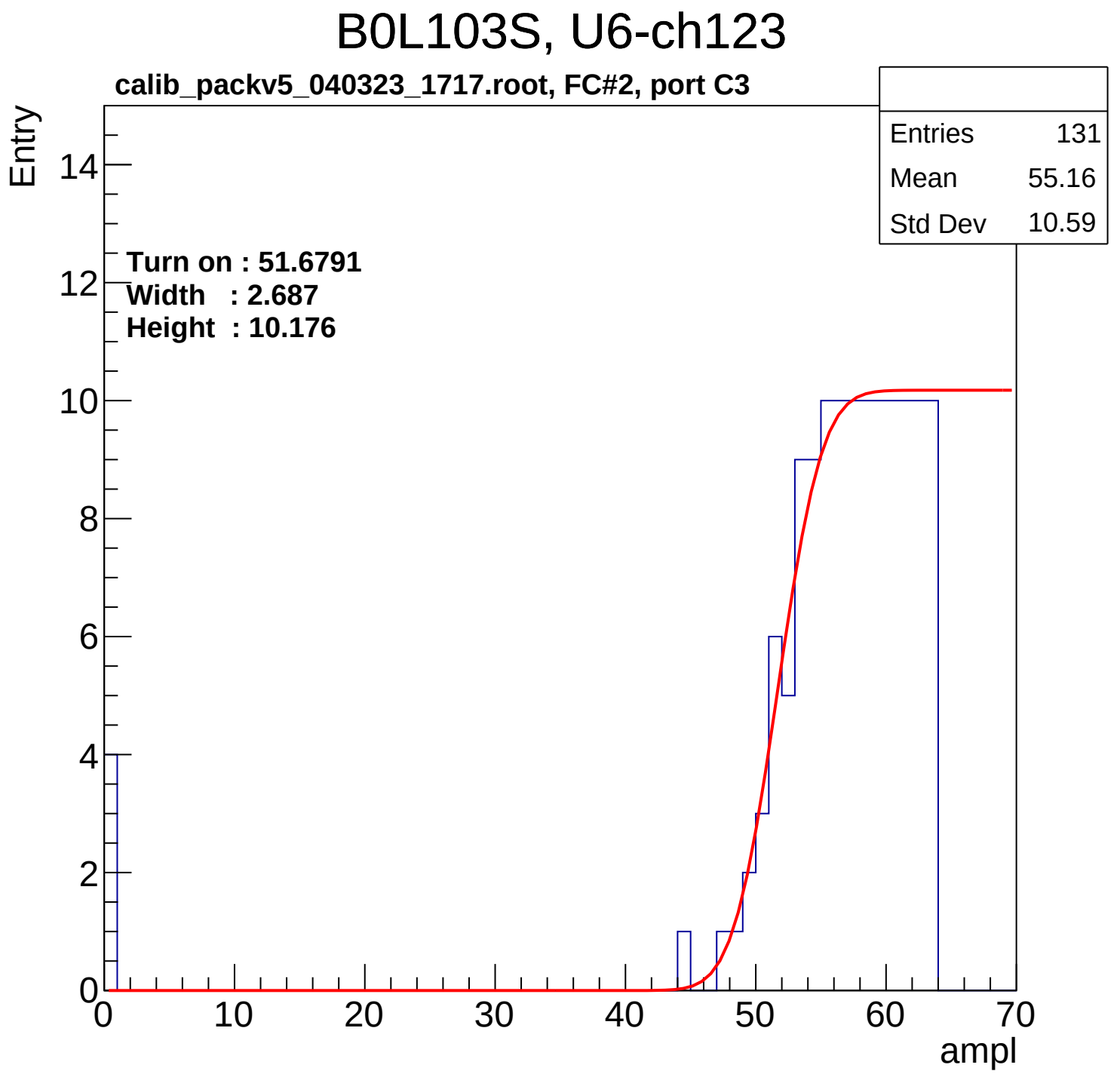
B0L103S, U6-ch123
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 55.16
Std Dev 10.59
Turn on : 51.6791
Width : 2.687
Height : 10.176
Entry
ampl
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2
4
6
8
10
12
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20
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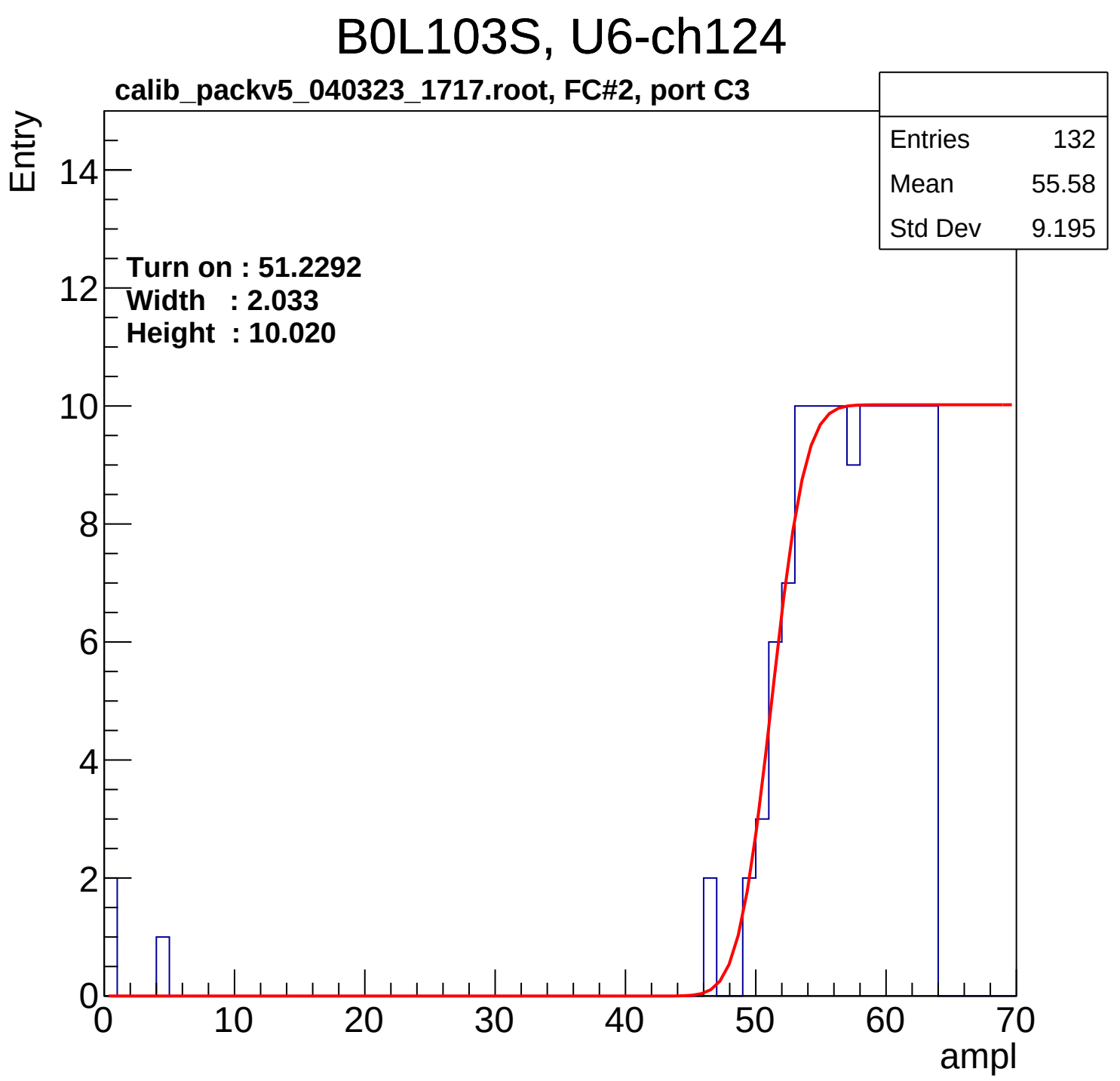
40
50
60
70


B0L103S, U6-ch124
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 55.58
Std Dev 9.195
Turn on : 51.2292
Width : 2.033
Height : 10.020
Entry
ampl
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4
6
8
10
12
14
0
10
20
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40
50
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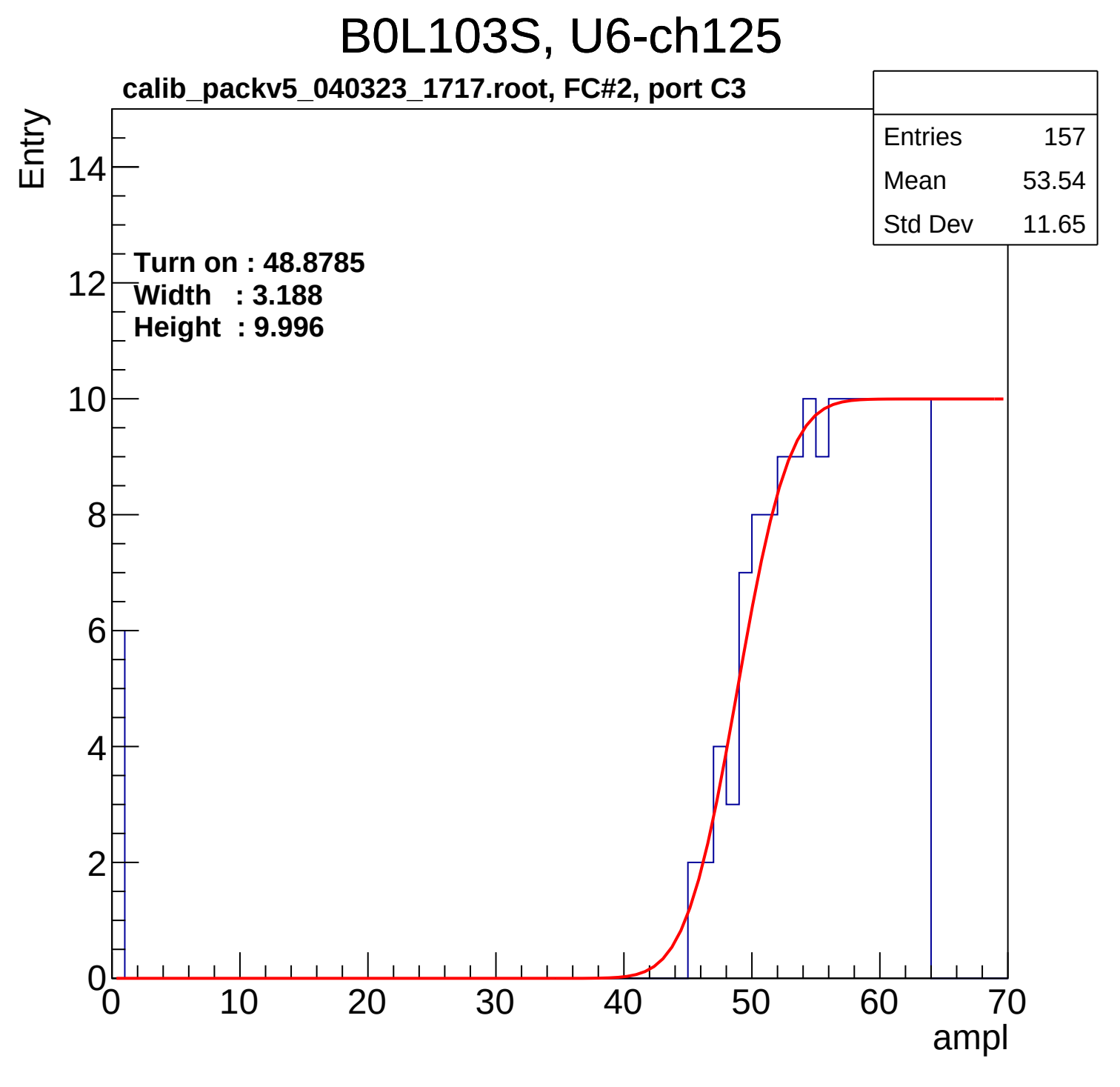
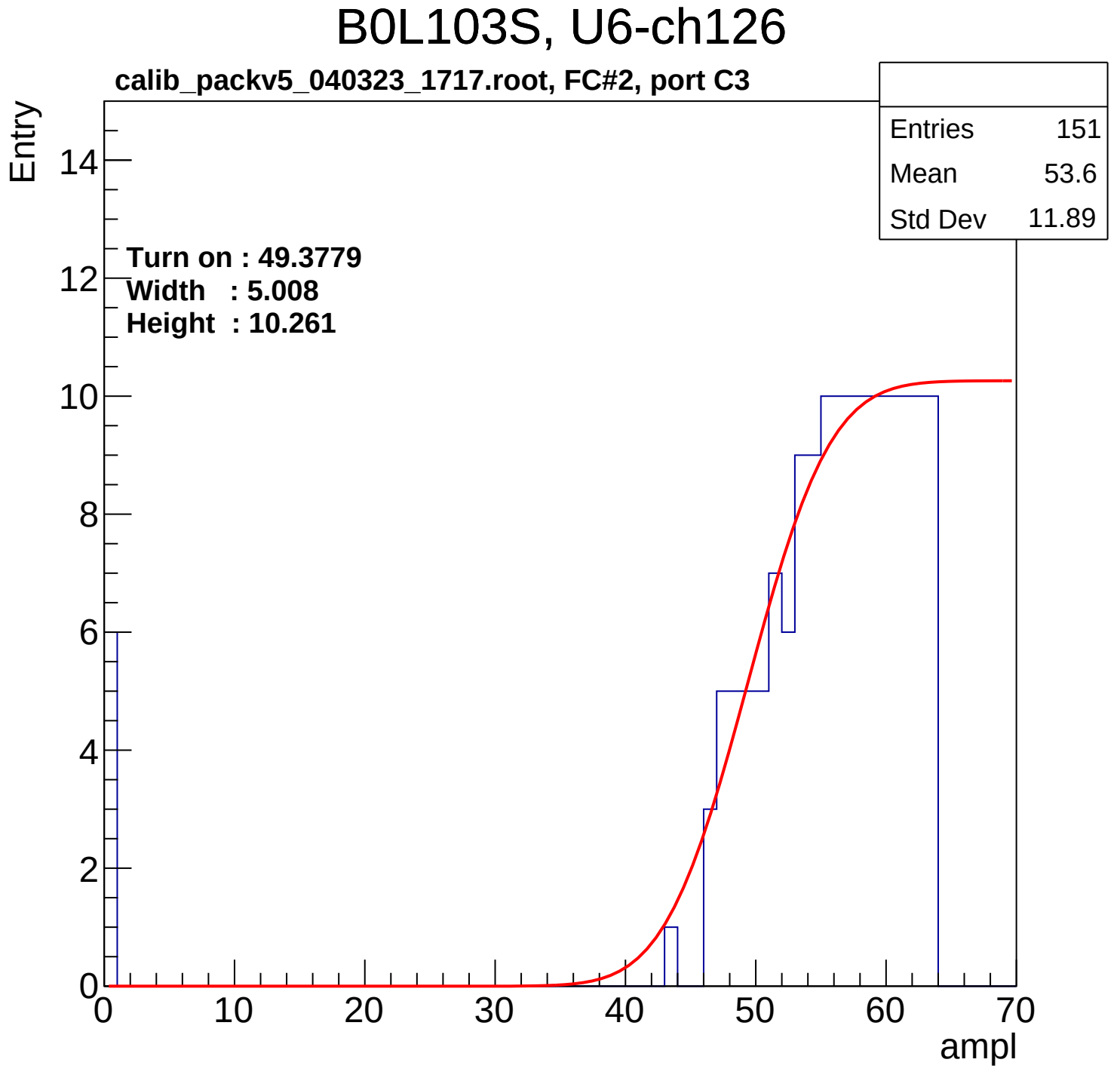

B0L103S, U6-ch125
calib_packv5_040323_1717.root, FC#2, port C3
Entries 157
Mean 53.54
Std Dev 11.65
Turn on : 48.8785
Width : 3.188
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U6-ch126
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 53.6
Std Dev 11.89
Turn on : 49.3779
Width : 5.008
Height : 10.261
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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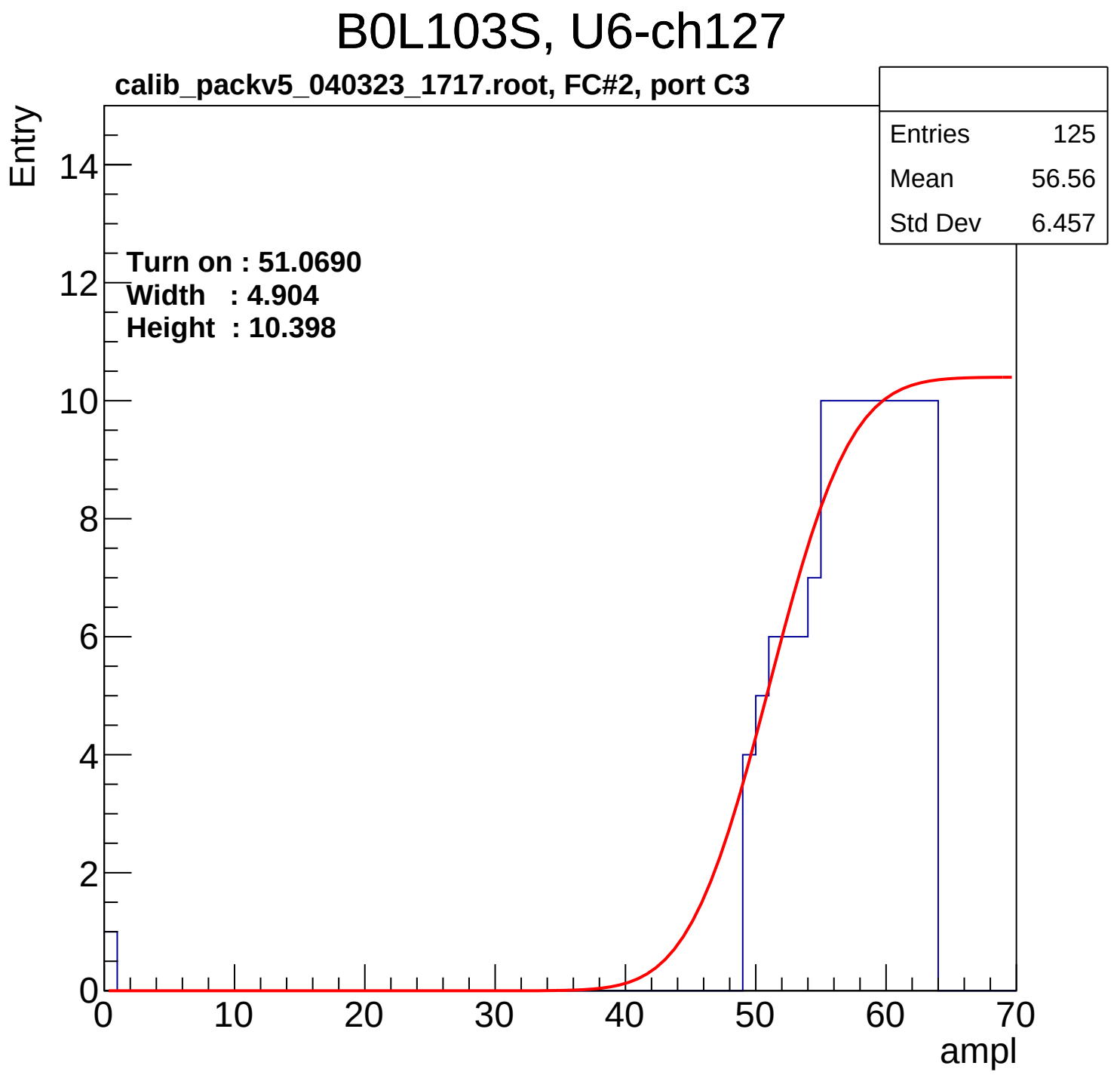
B0L103S, U6-ch127
calib_packv5_040323_1717.root, FC#2, port C3
Entries 125
Mean 56.56
Std Dev 6.457
Turn on : 51.0690
Width : 4.904
Height : 10.398
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
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60
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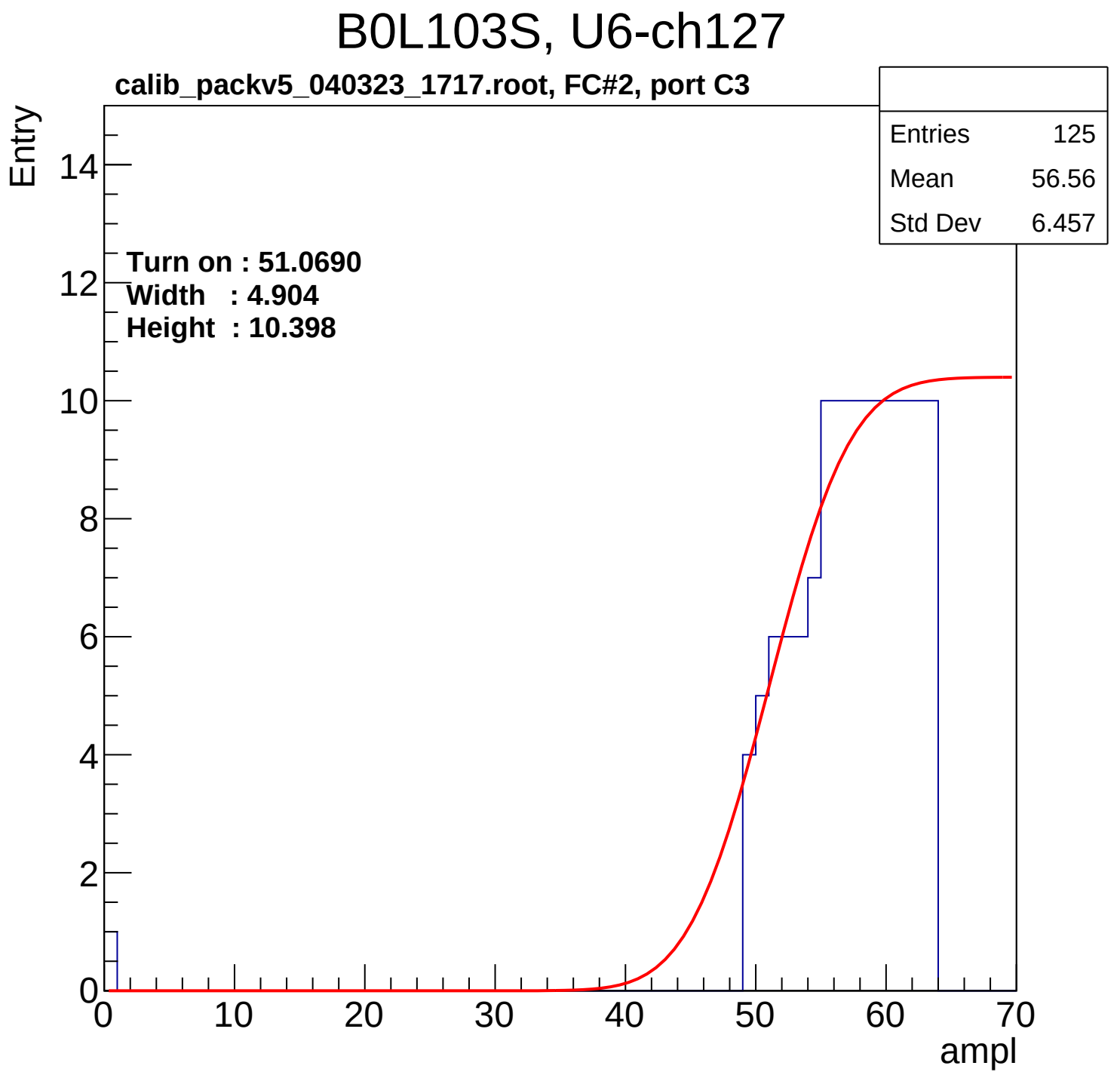
B0L103S, U6-ch127
calib_packv5_040323_1717.root, FC#2, port C3
Entries 125
Mean 56.56
Std Dev 6.457
Turn on : 51.0690
Width : 4.904
Height : 10.398
Entry
ampl
0
2
4
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8
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12
14
0
10
20
30
40
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60
70