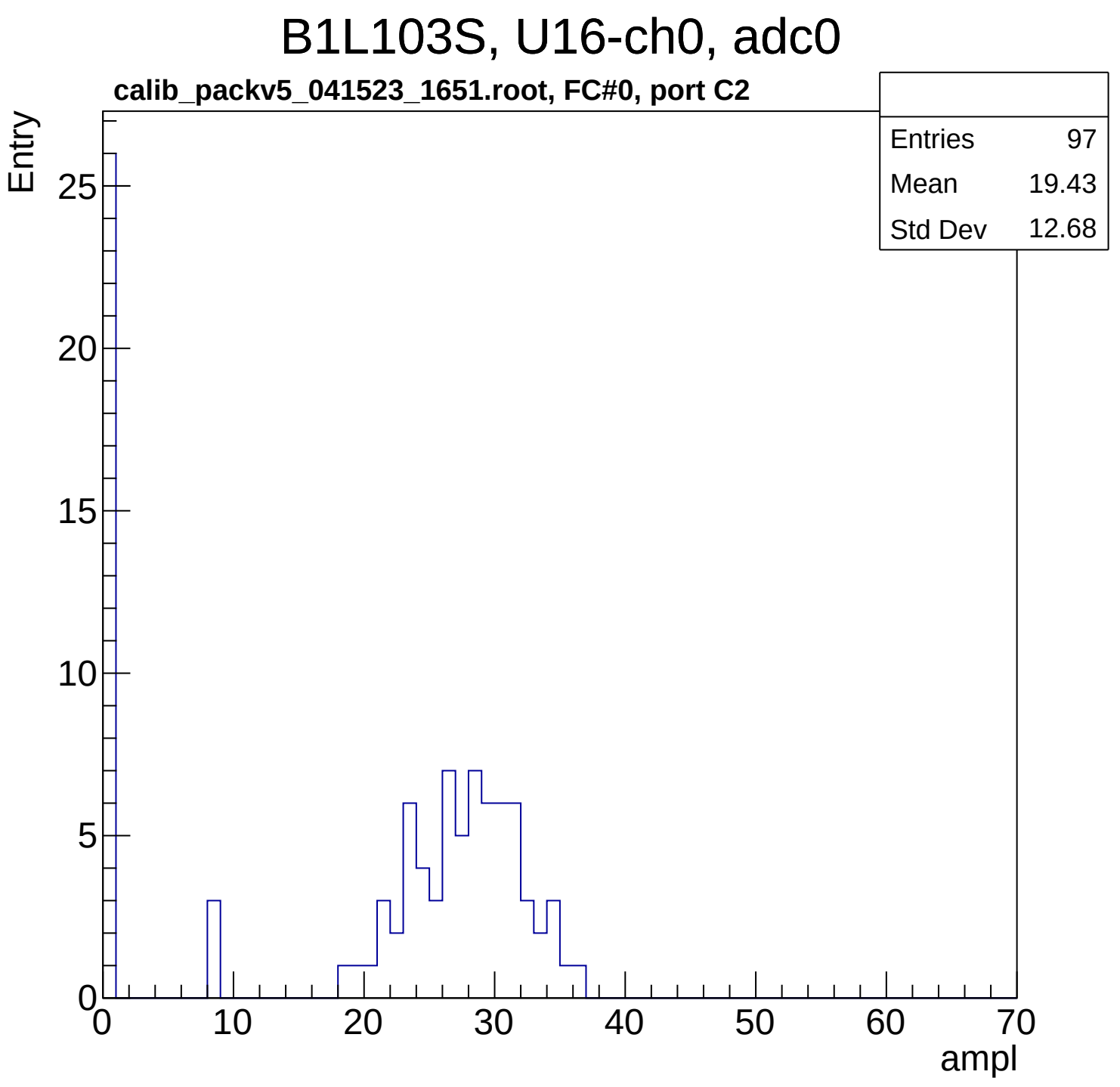
B1L103S, U16-ch0, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 19.43
Std Dev 12.68
Entry
0
5
10
15
20
25
0
10
20
30
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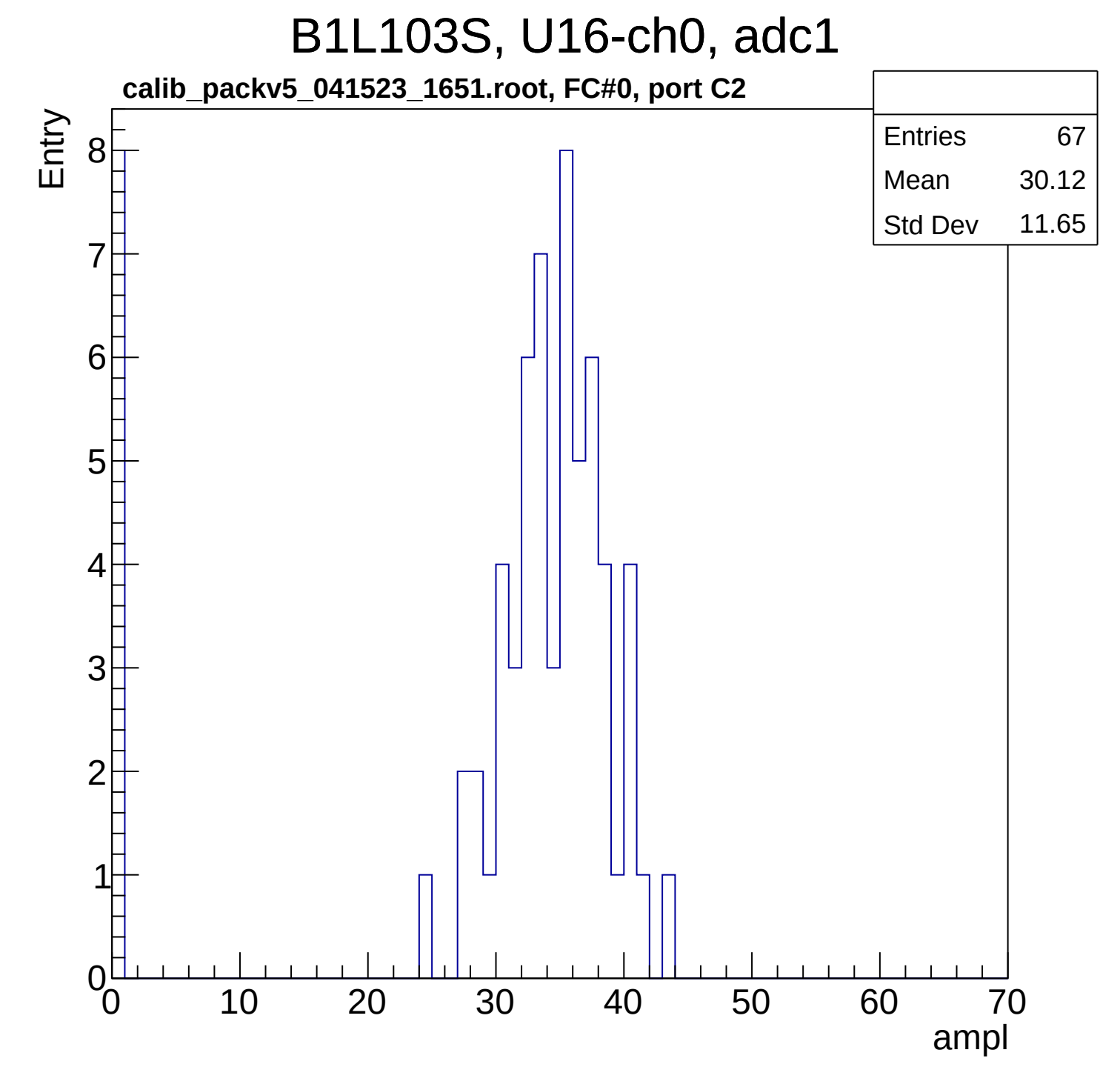
50
60
70
ampl


B1L103S, U16-ch0, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 30.12
Std Dev 11.65
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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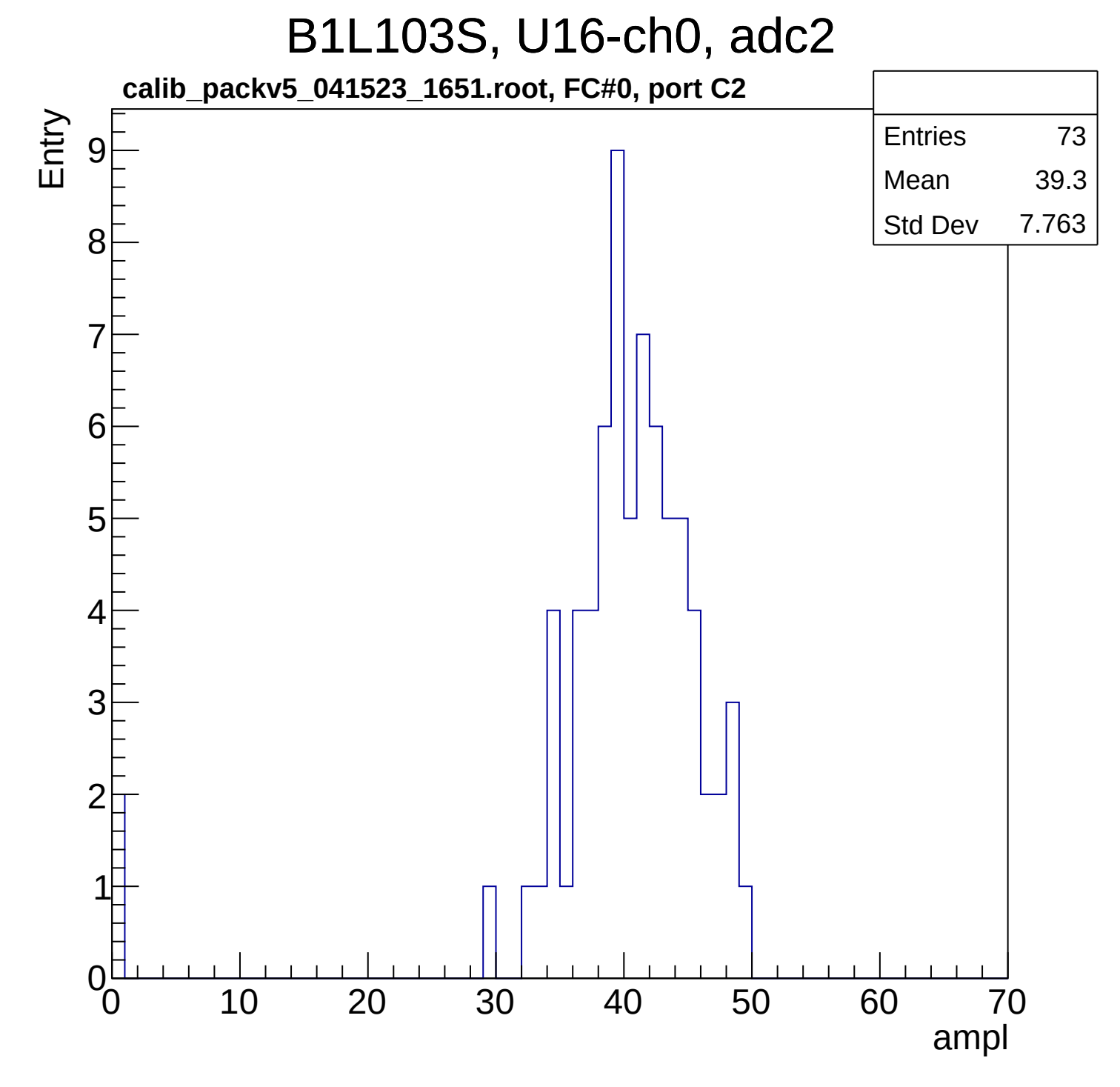
B1L103S, U16-ch0, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 39.3
Std Dev 7.763
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
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40
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60
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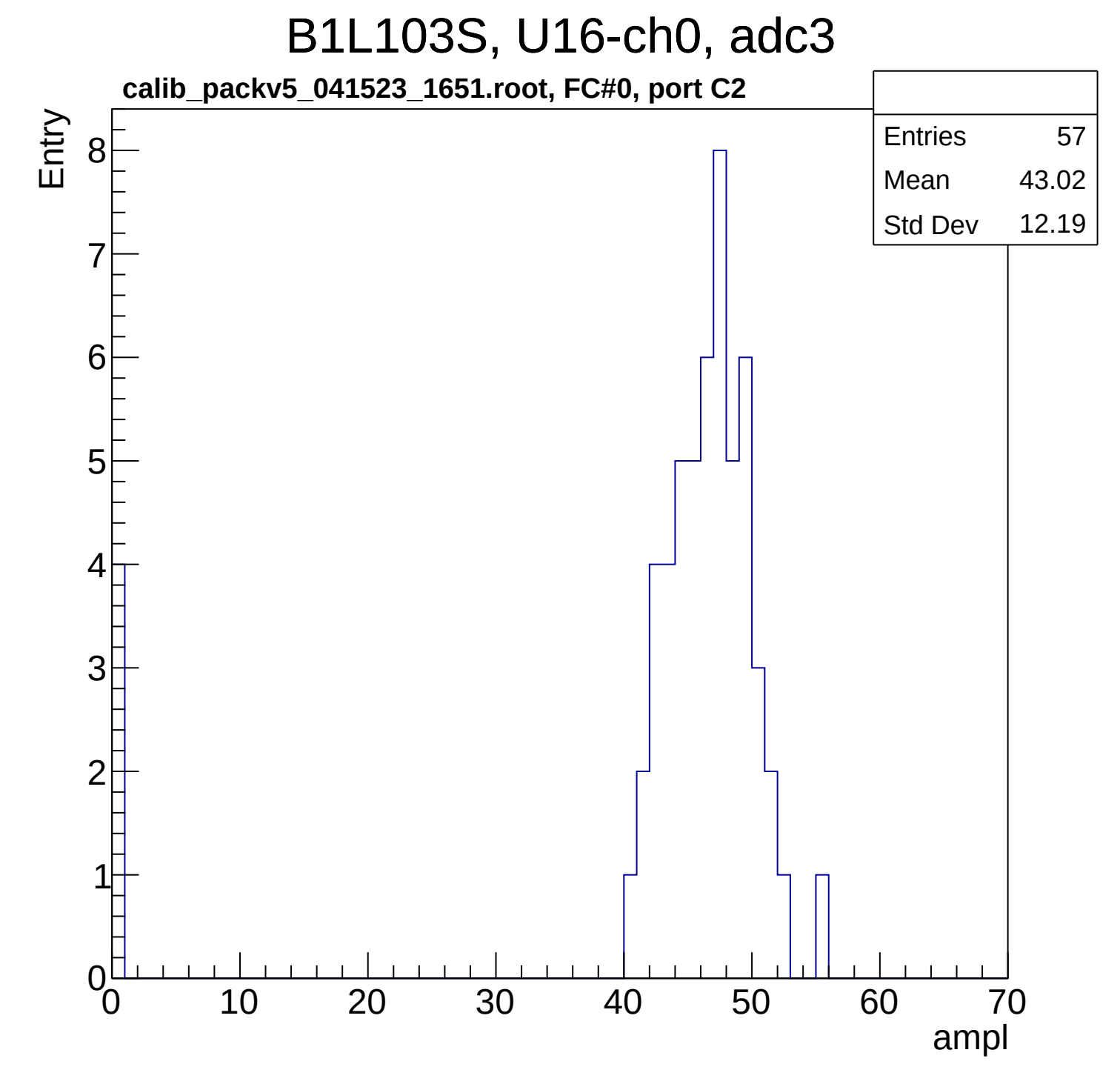
B1L103S, U16-ch0, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 43.02
Std Dev 12.19
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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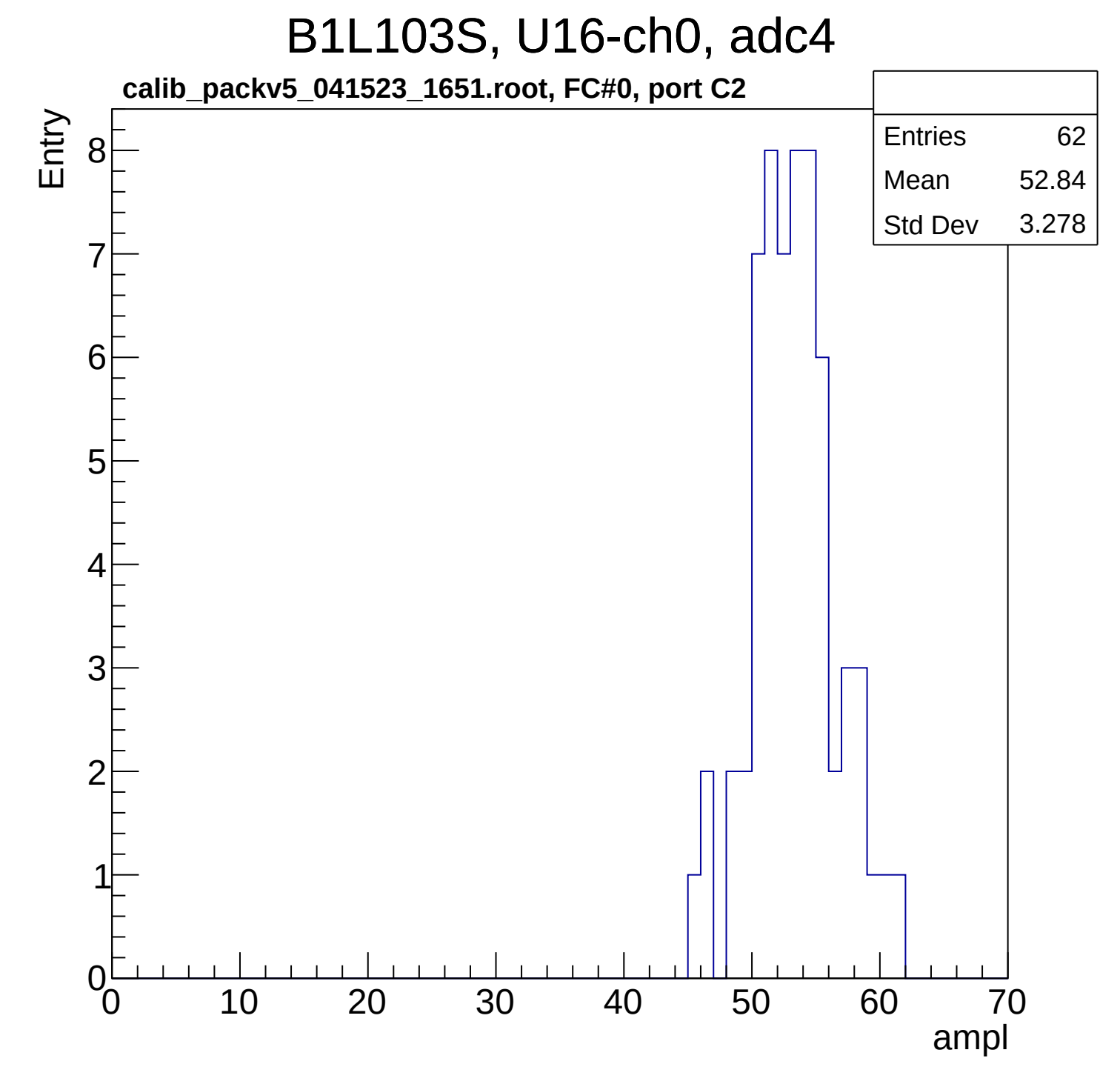
B1L103S, U16-ch0, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 52.84
Std Dev 3.278
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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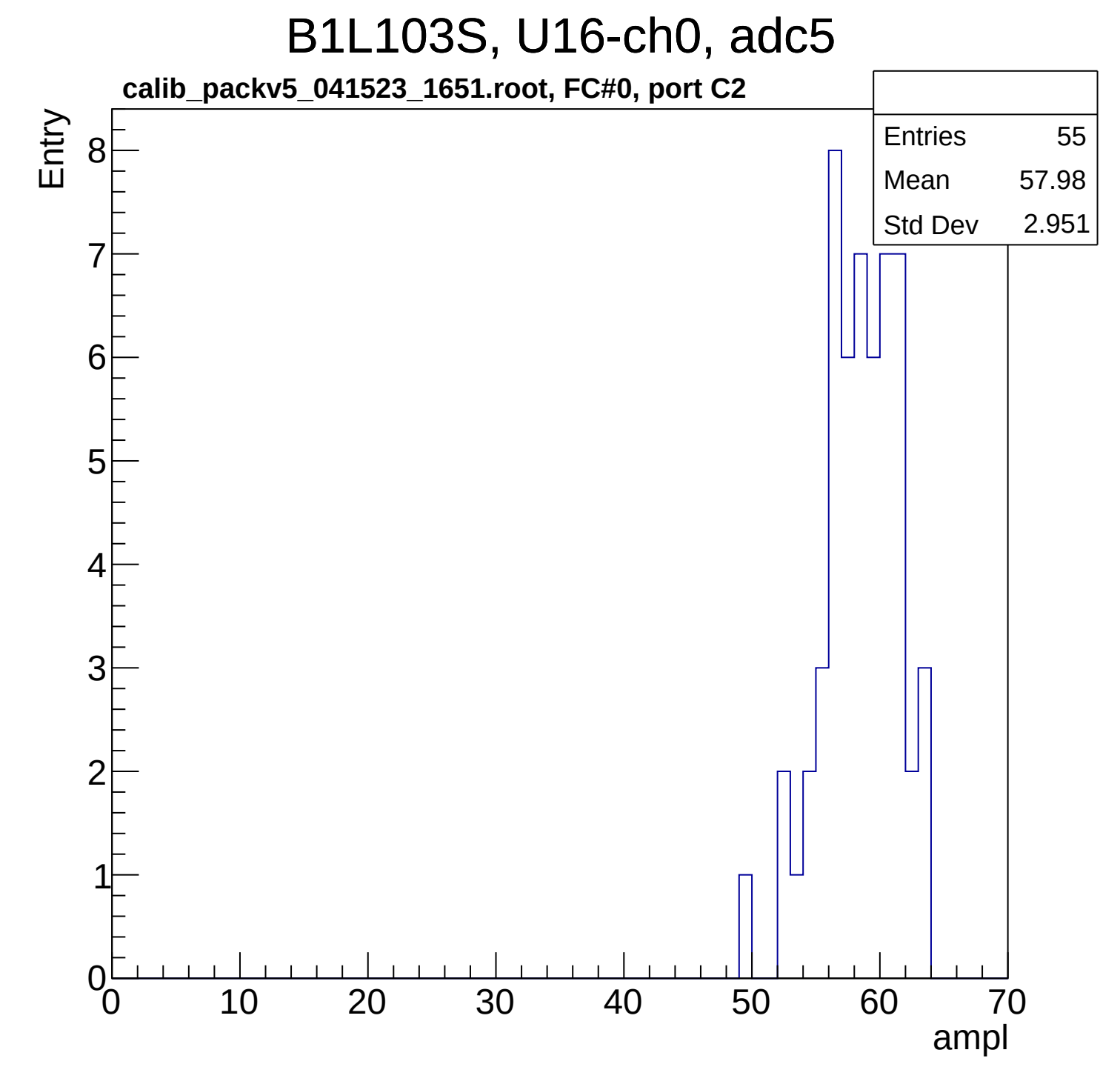
B1L103S, U16-ch0, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.98
Std Dev 2.951
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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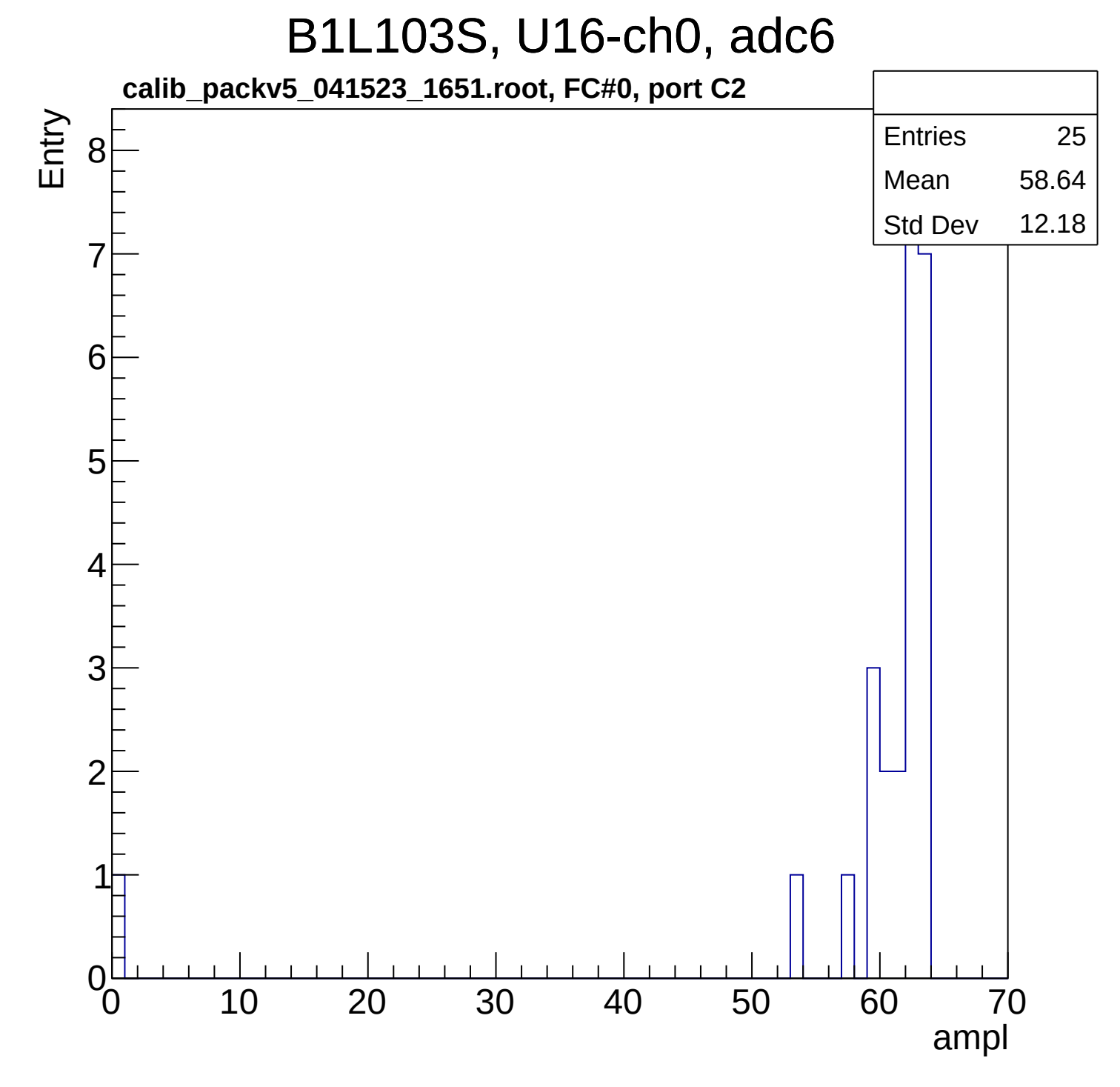
B1L103S, U16-ch0, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 58.64
Std Dev 12.18
Entry
ampl
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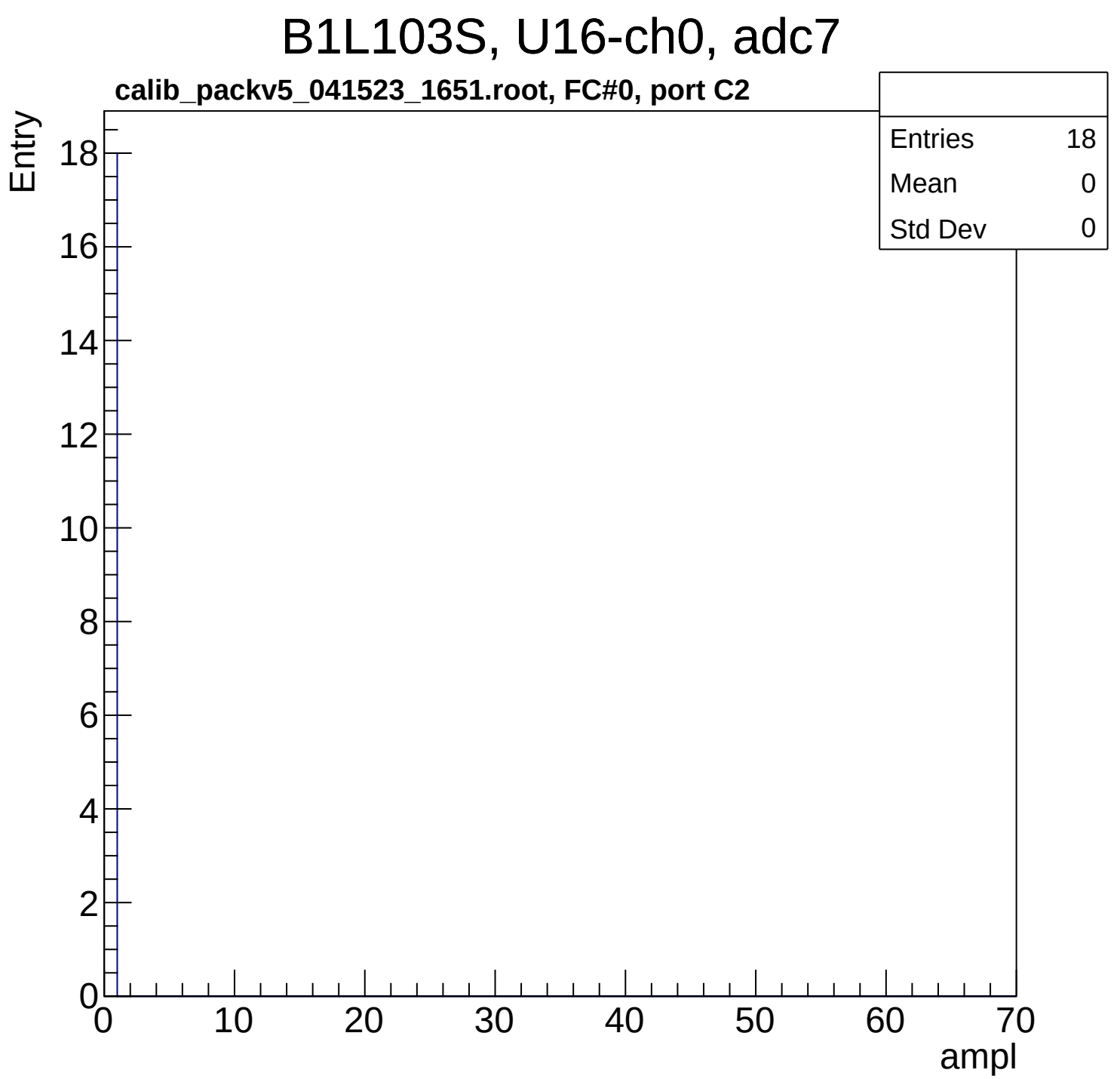
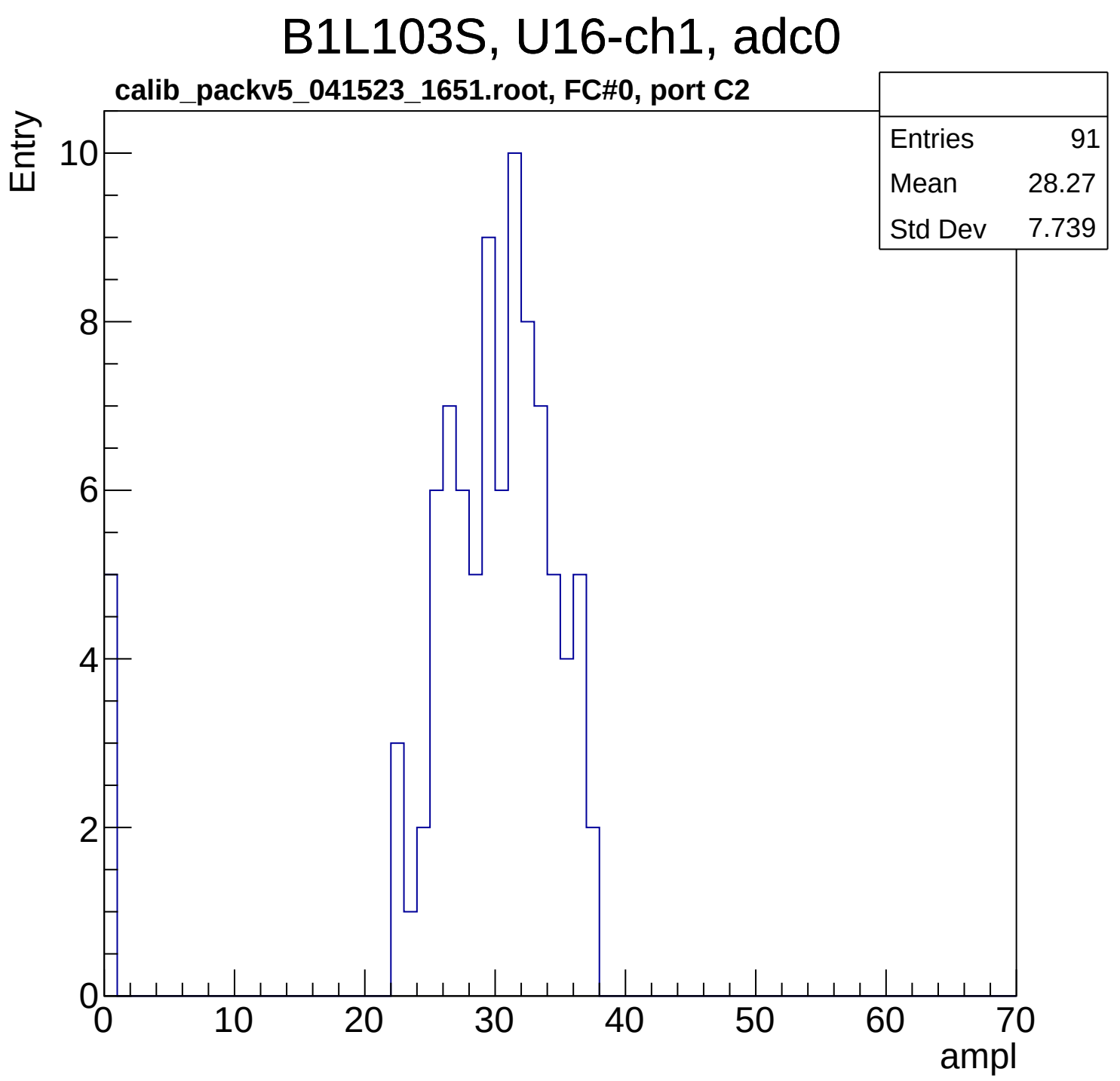
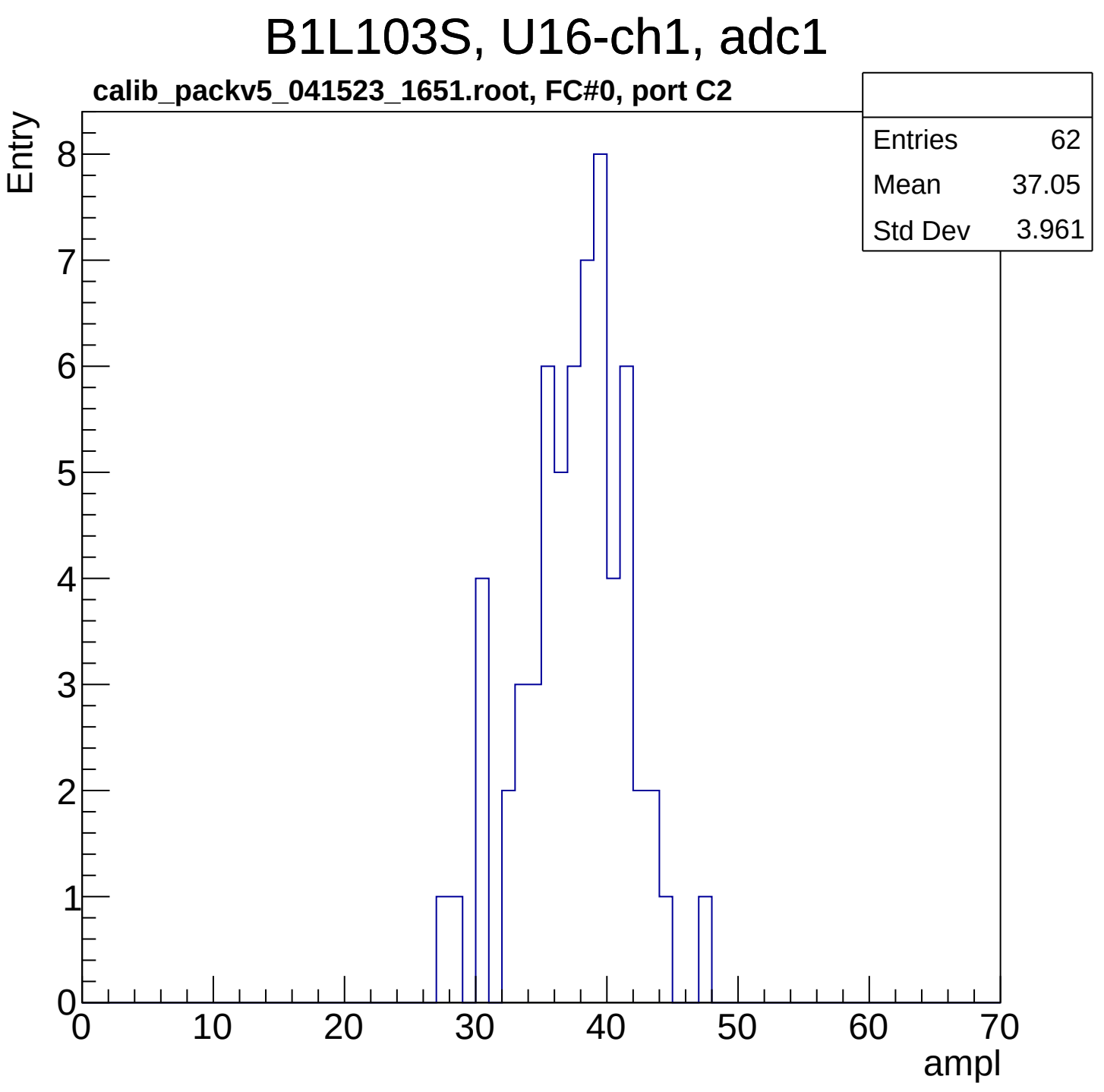
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch0, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch1, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 28.27
Std Dev 7.739
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch1, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 37.05
Std Dev 3.961
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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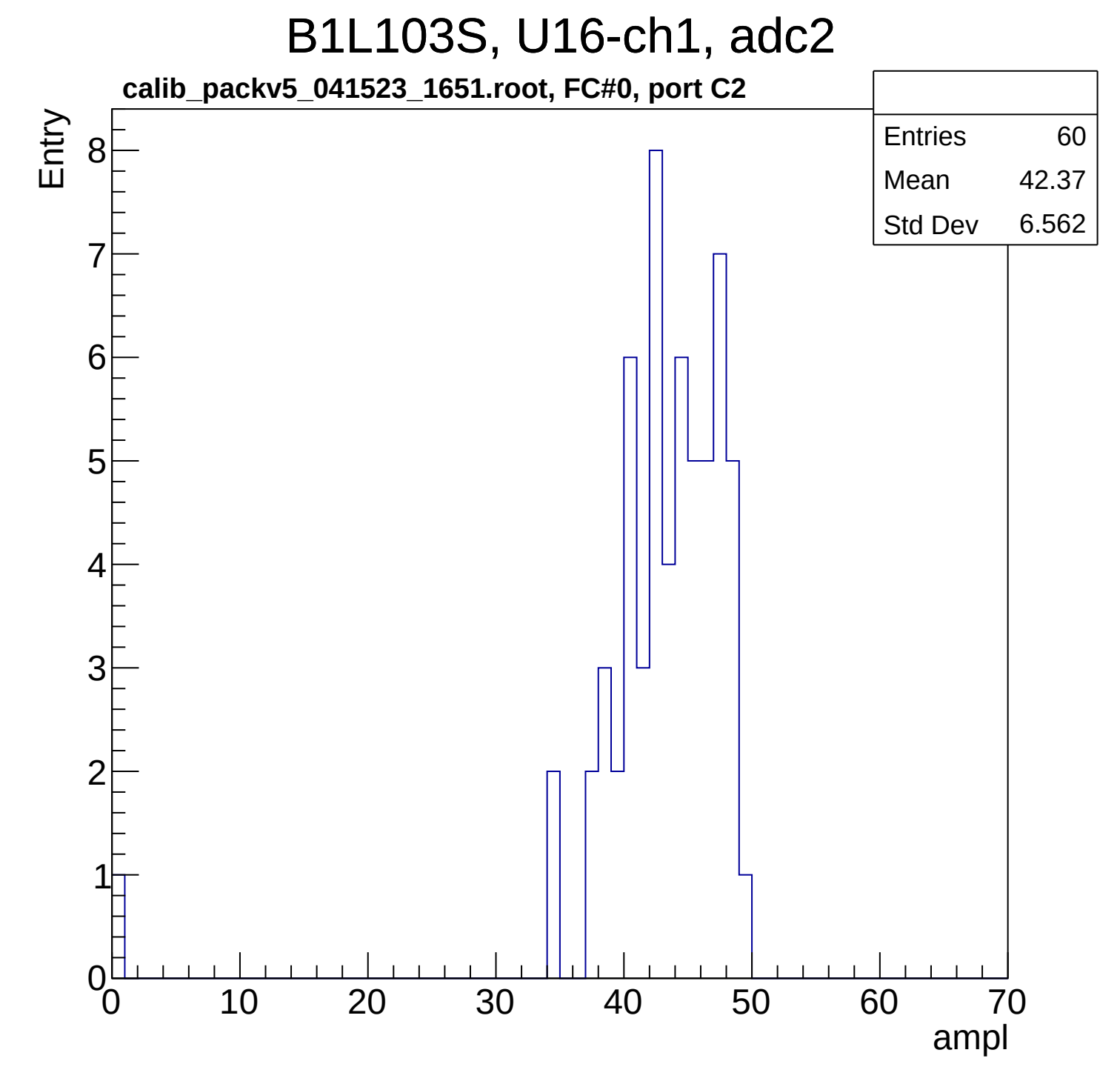
60
70


B1L103S, U16-ch1, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 42.37
Std Dev 6.562
Entry
ampl
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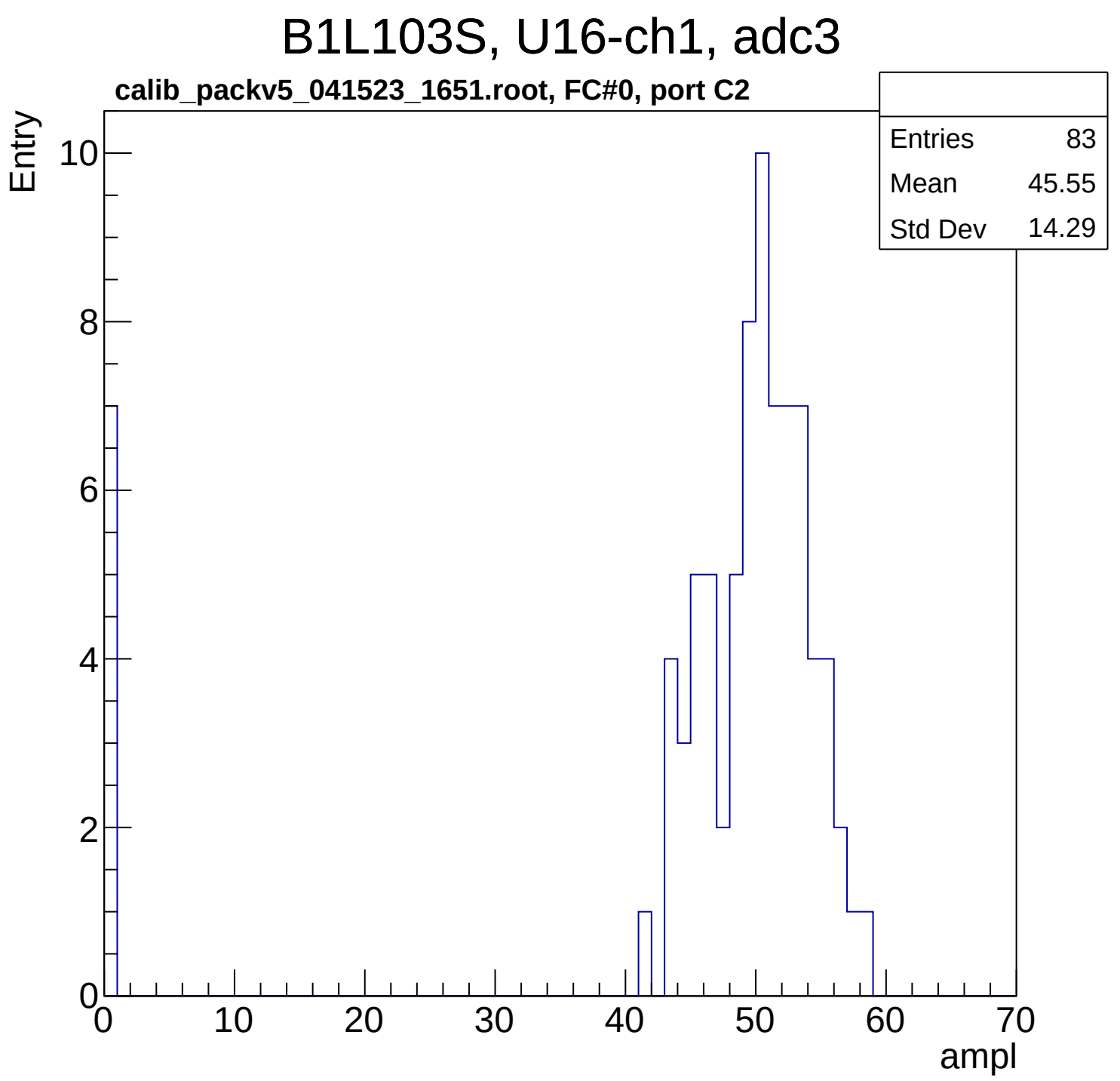
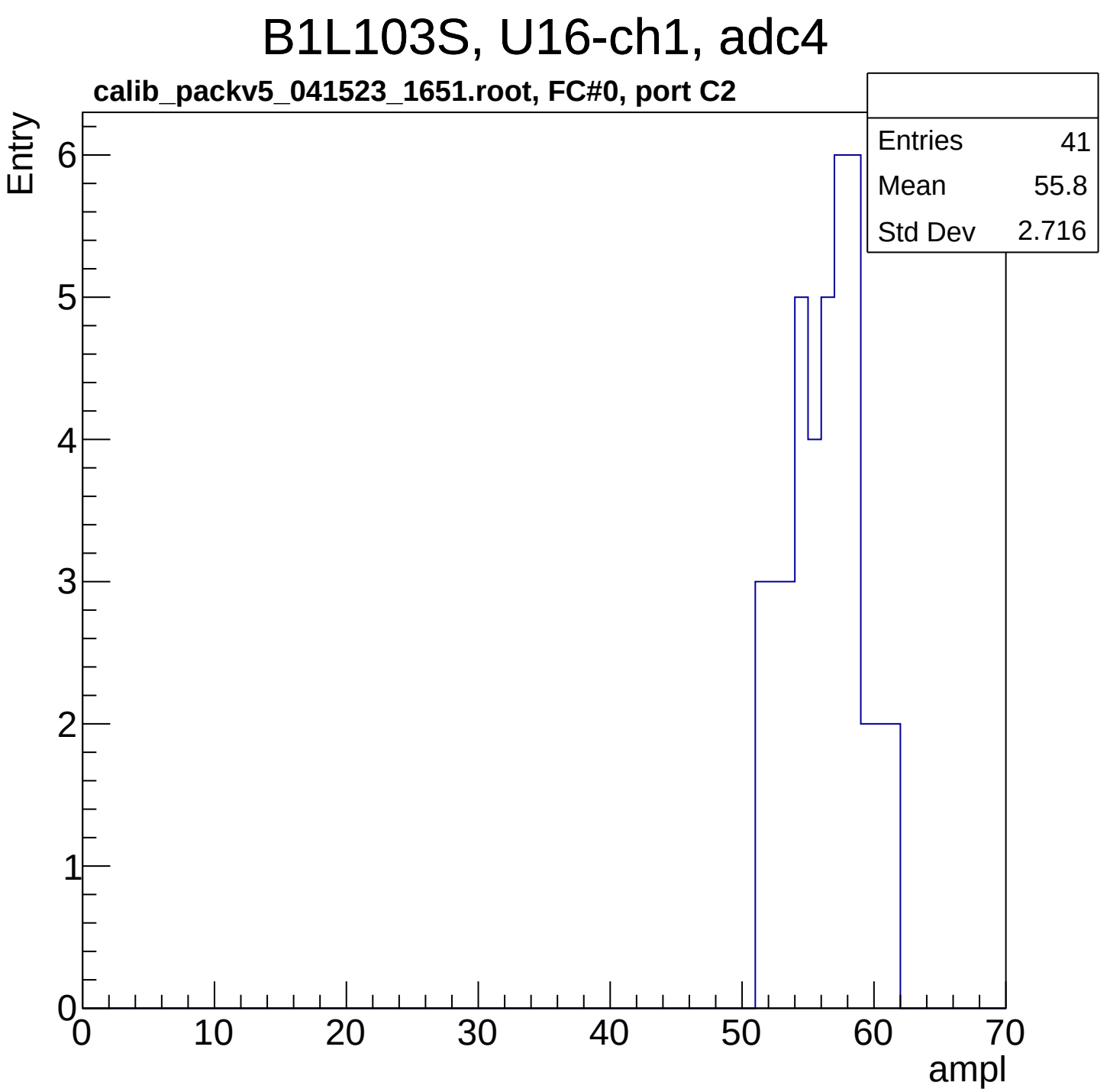
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch1, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 45.55
Std Dev 14.29
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch1, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 55.8
Std Dev 2.716
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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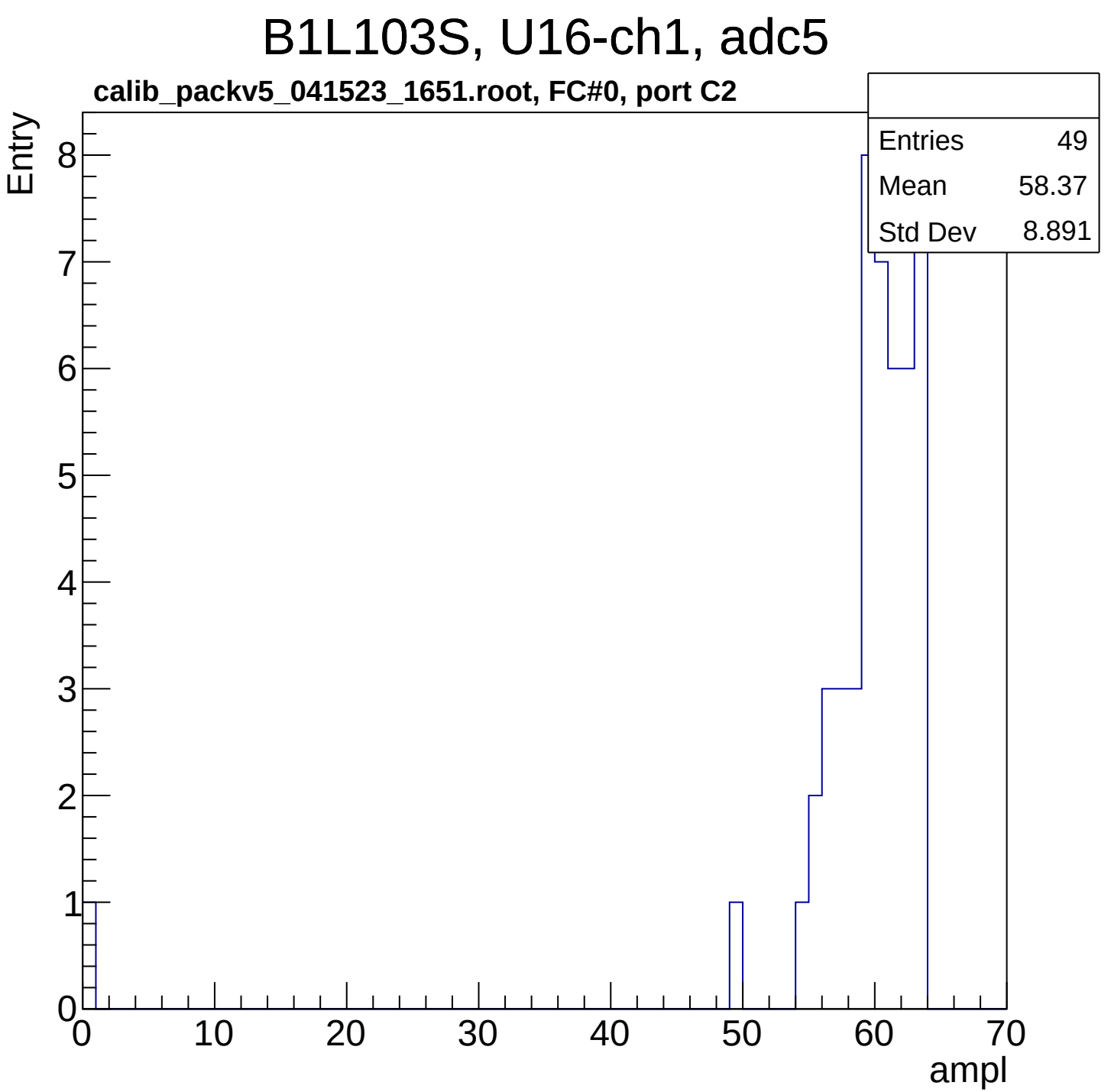
B1L103S, U16-ch1, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.37
Std Dev 8.891
Entry
ampl
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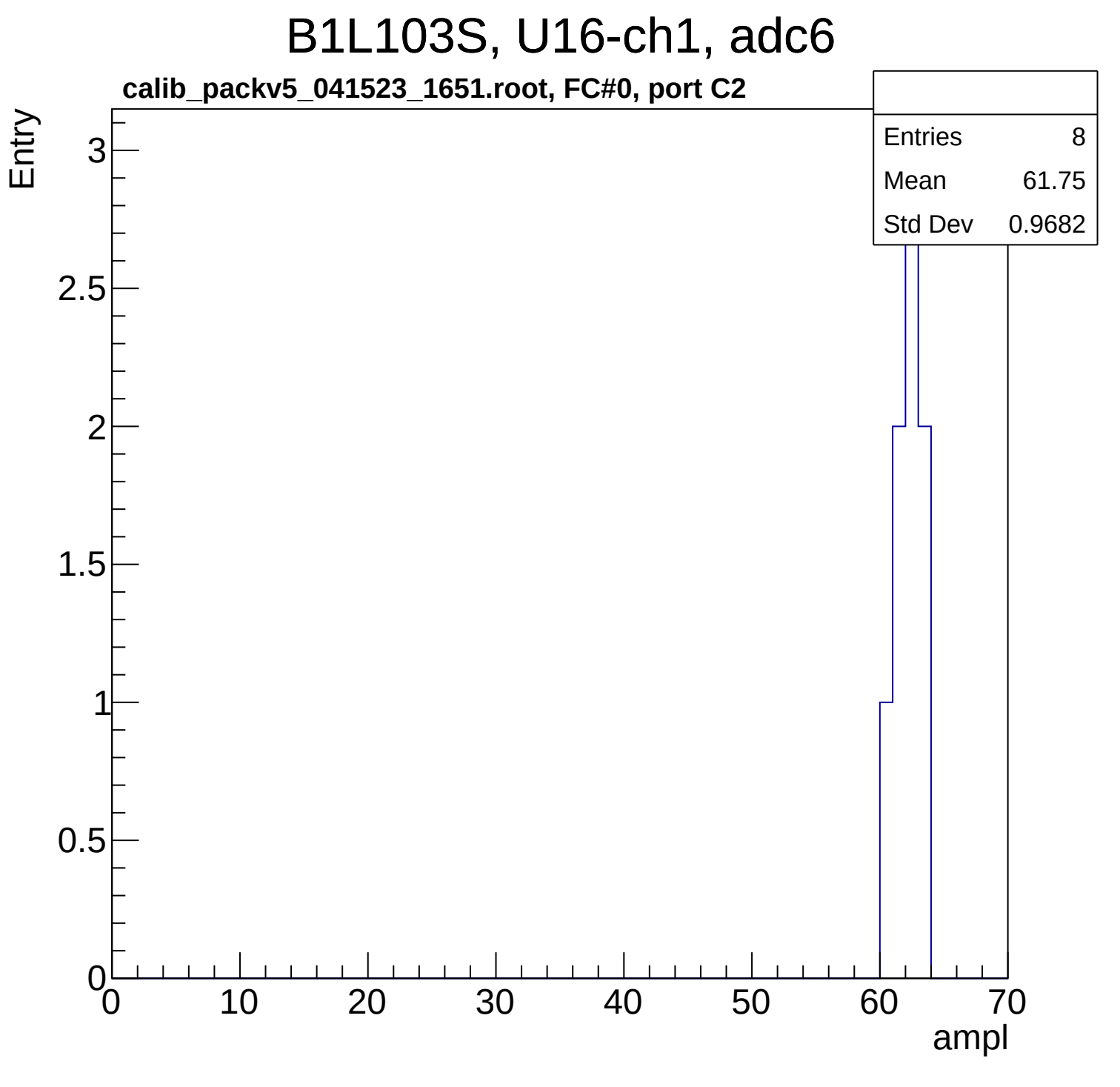
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch1, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.75
Std Dev 0.9682
Entry
ampl
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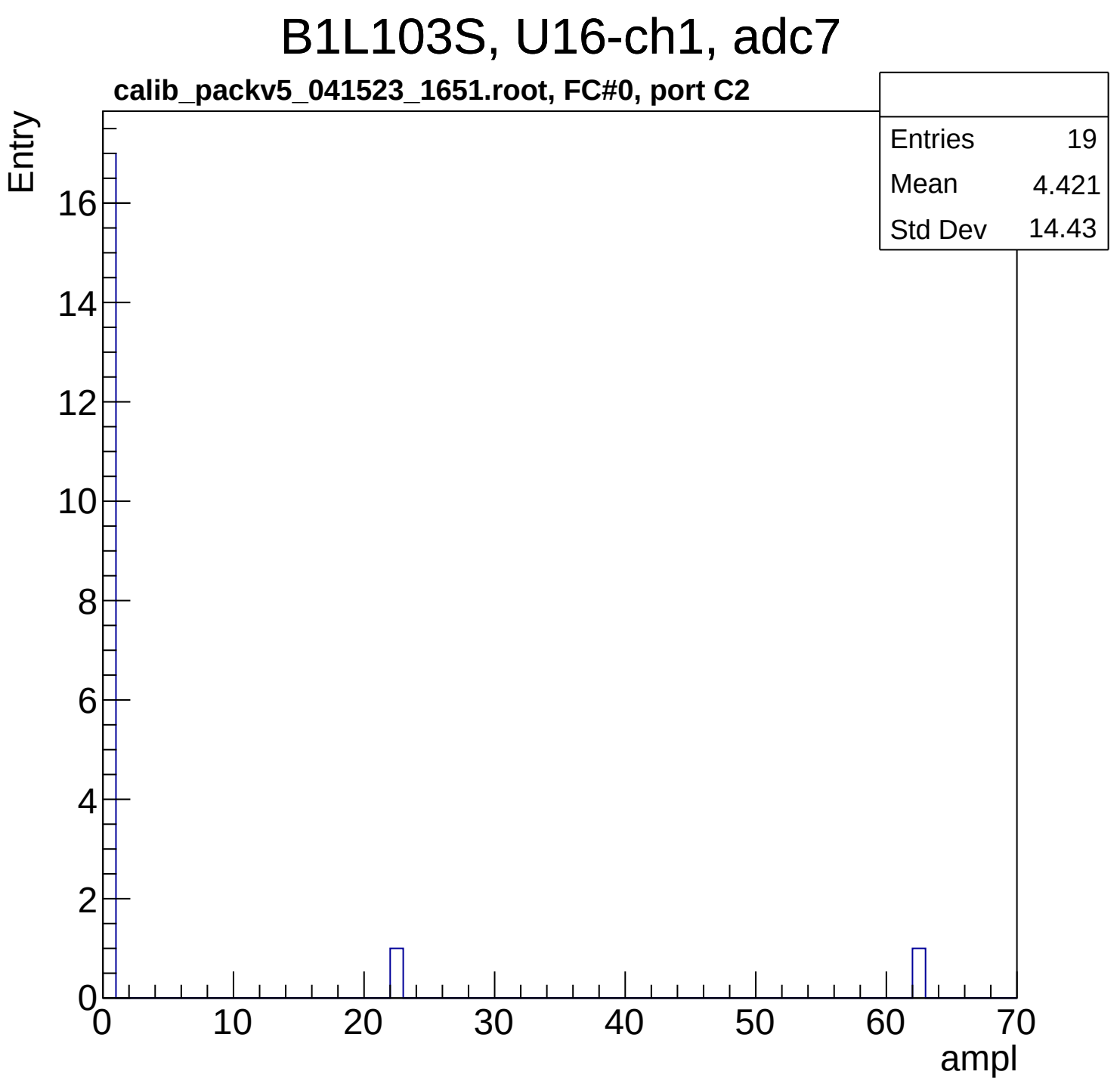
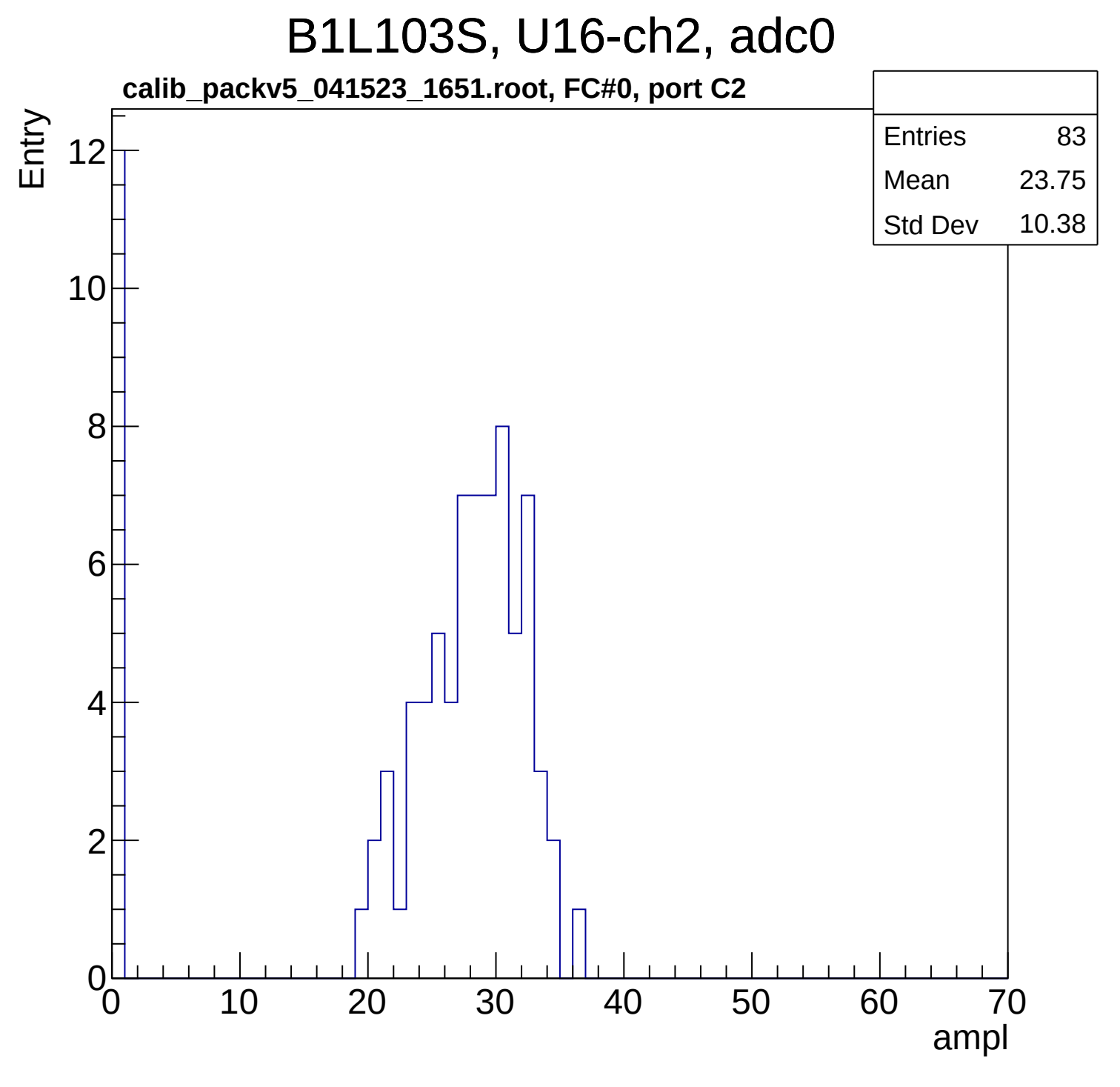
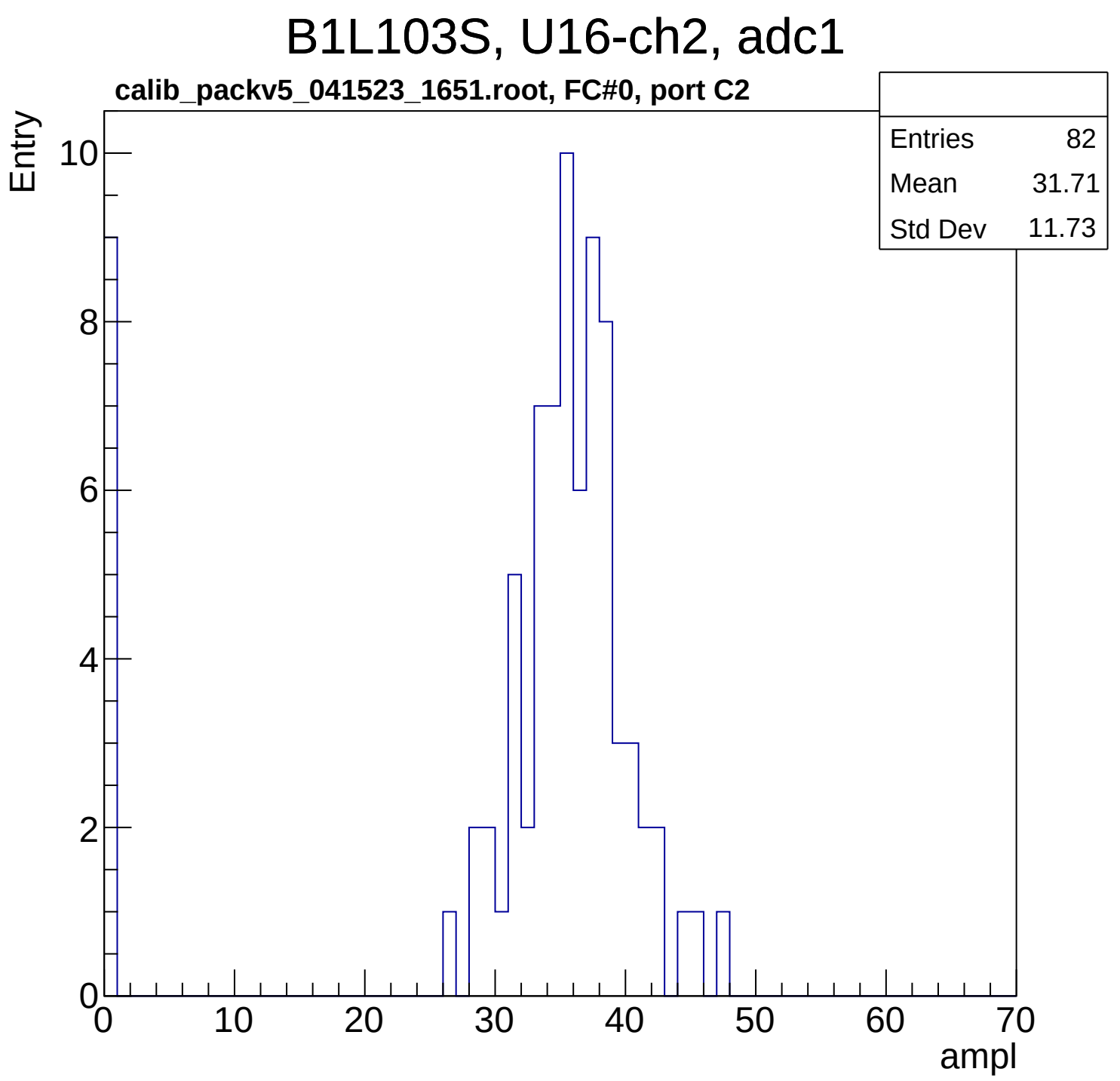
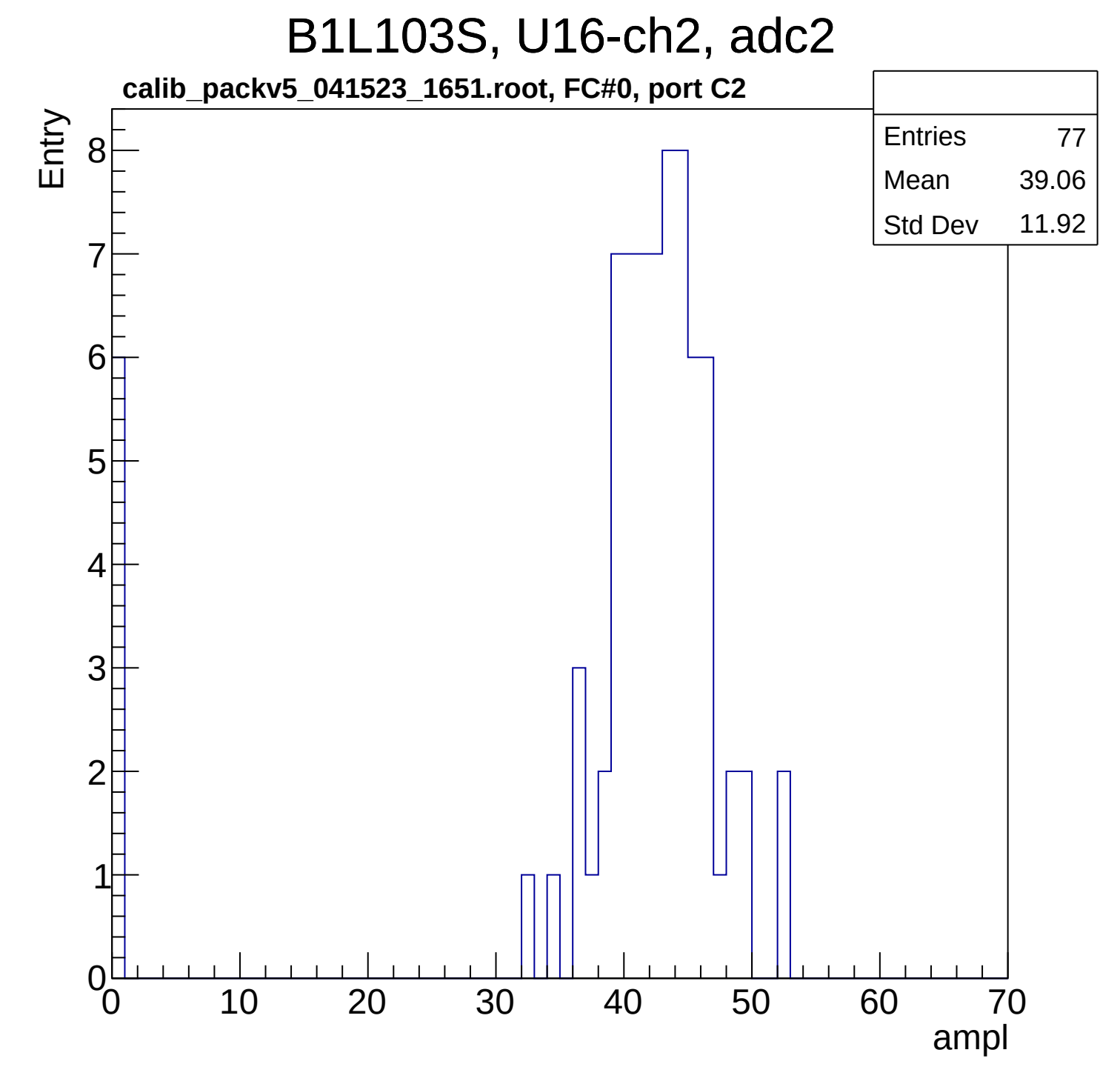
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U16-ch1, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 4.421
Std Dev 14.43
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch2, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 23.75
Std Dev 10.38
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U16-ch2, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 31.71
Std Dev 11.73
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch2, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 39.06
Std Dev 11.92
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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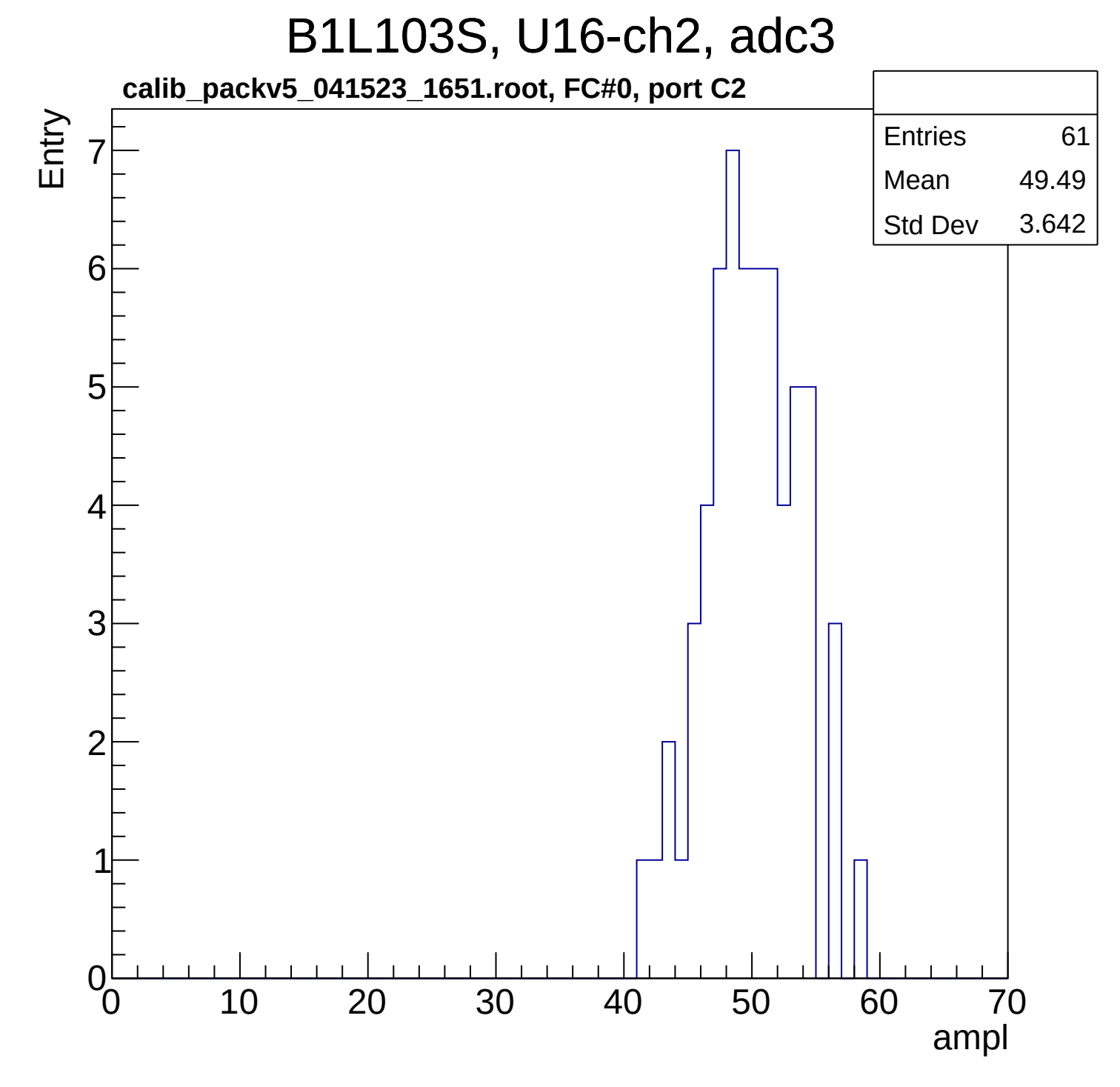
60
70


B1L103S, U16-ch2, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 49.49
Std Dev 3.642
Entry
ampl
0
1
2
3
4
5
6
7
0
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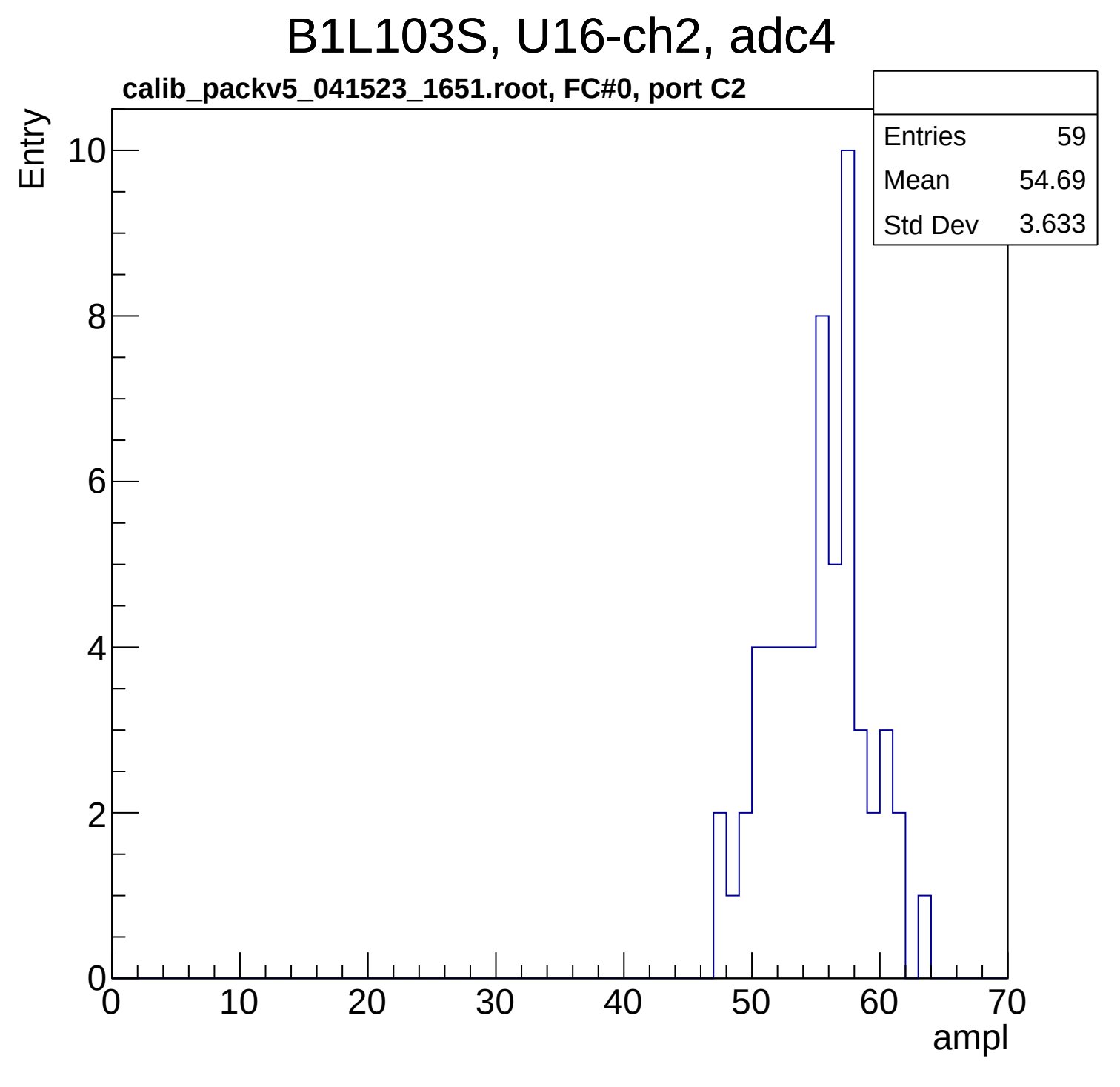
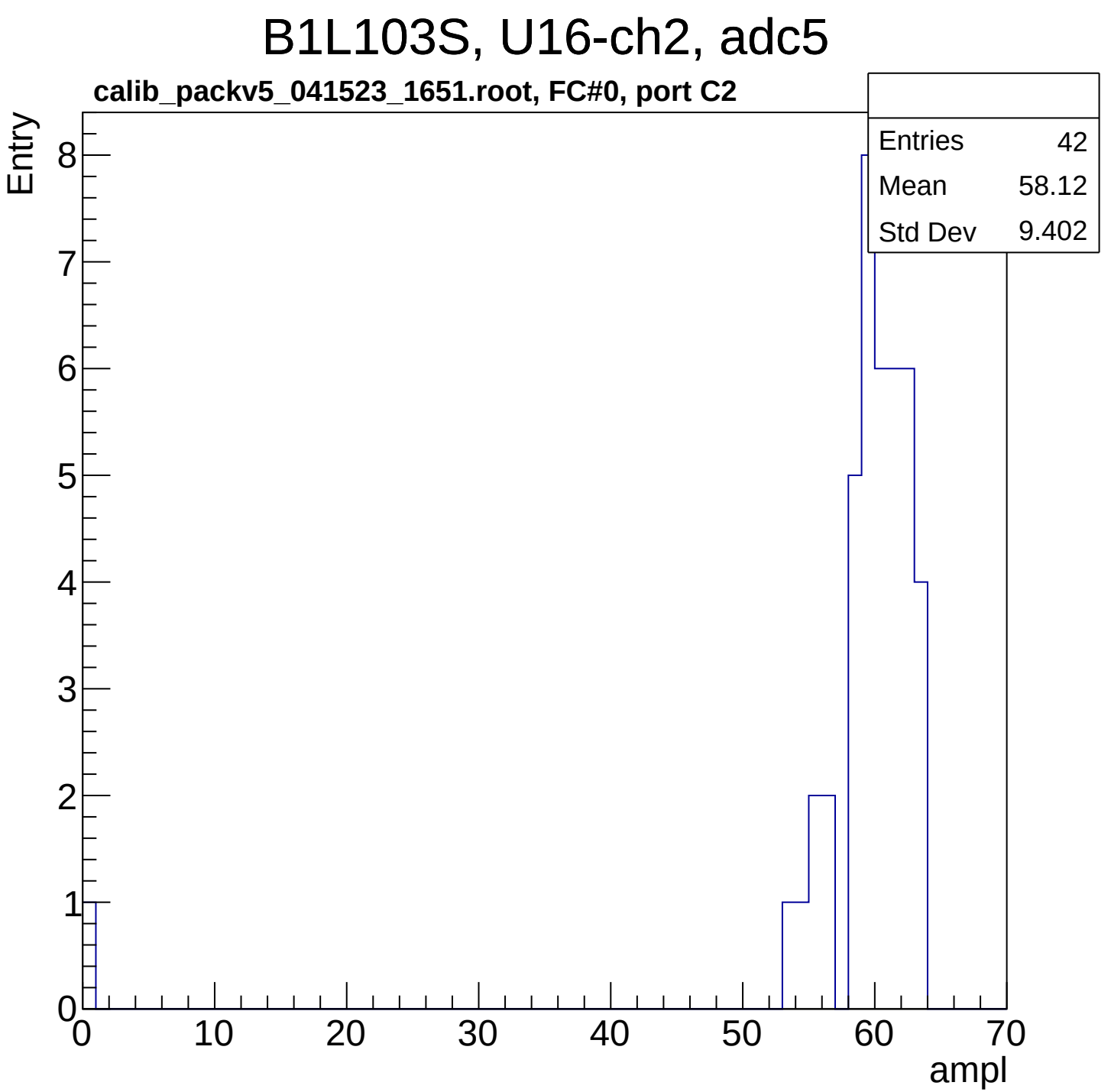
20
30
40
50
60
70


B1L103S, U16-ch2, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.69
Std Dev 3.633
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch2, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 58.12
Std Dev 9.402
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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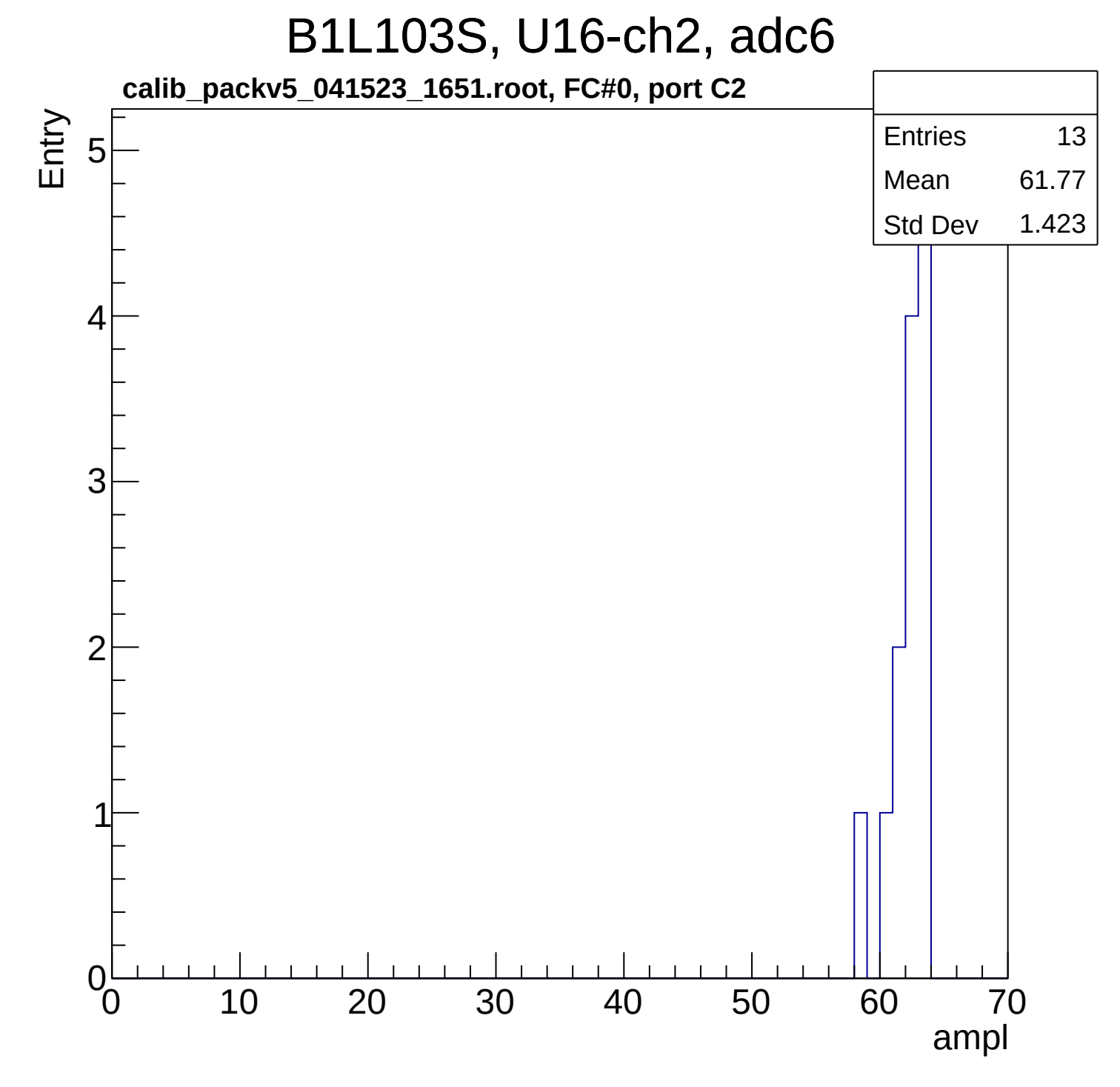
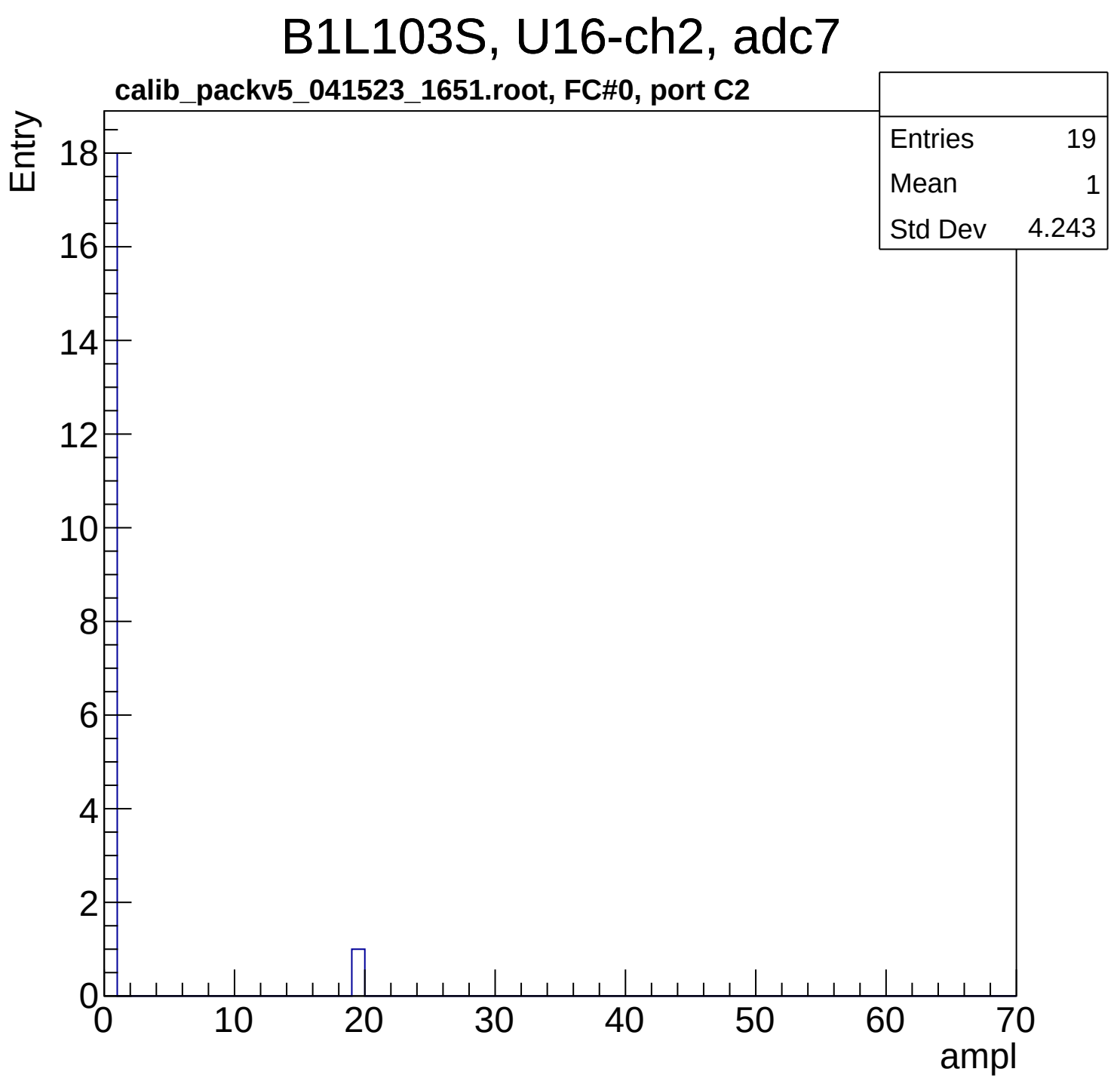
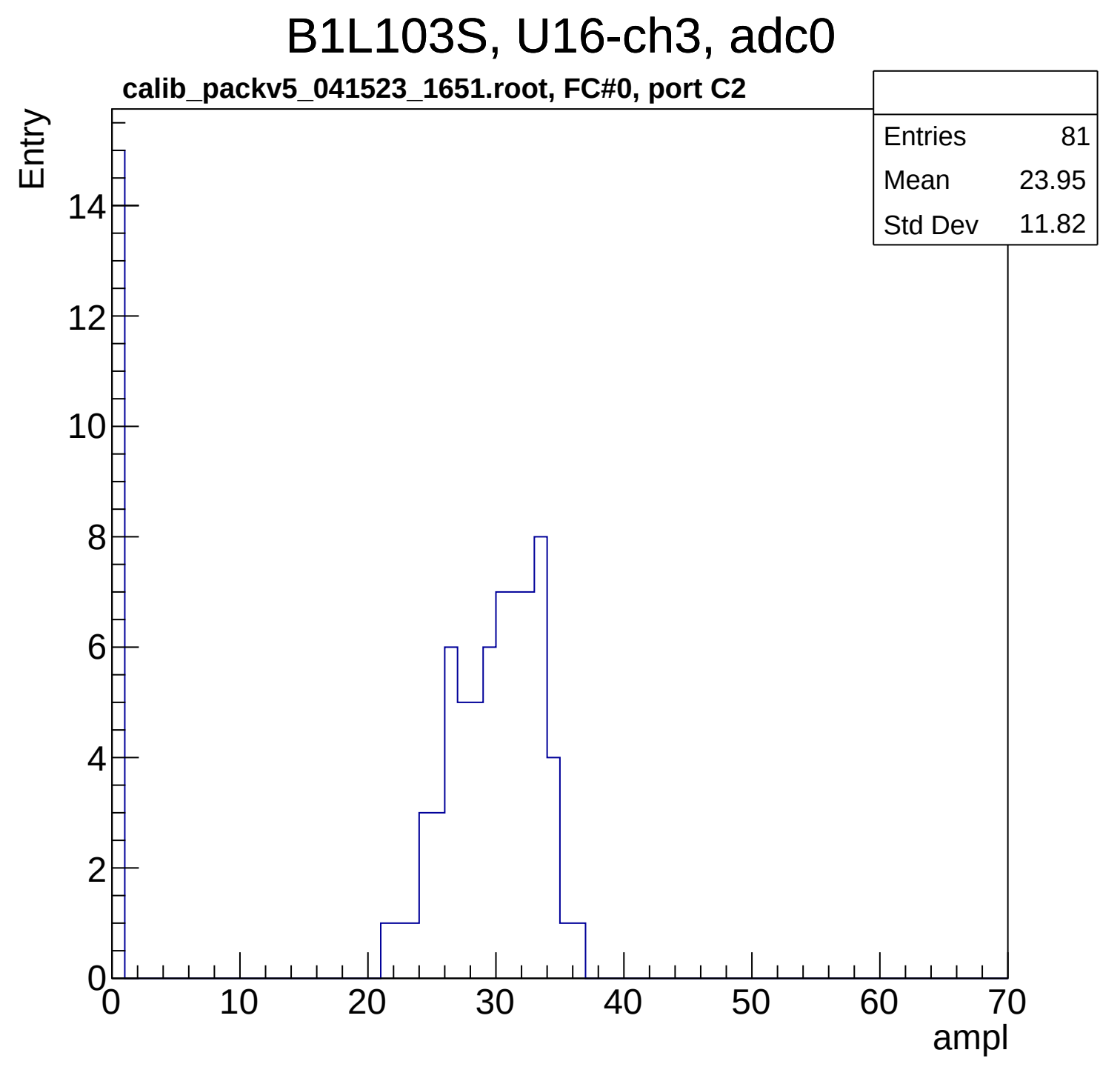
40
50
60
70


B1L103S, U16-ch2, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.77
Std Dev 1.423
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U16-ch2, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1
Std Dev 4.243
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch3, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 23.95
Std Dev 11.82
Entry
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2
4
6
8
10
12
14
0
10
20
30
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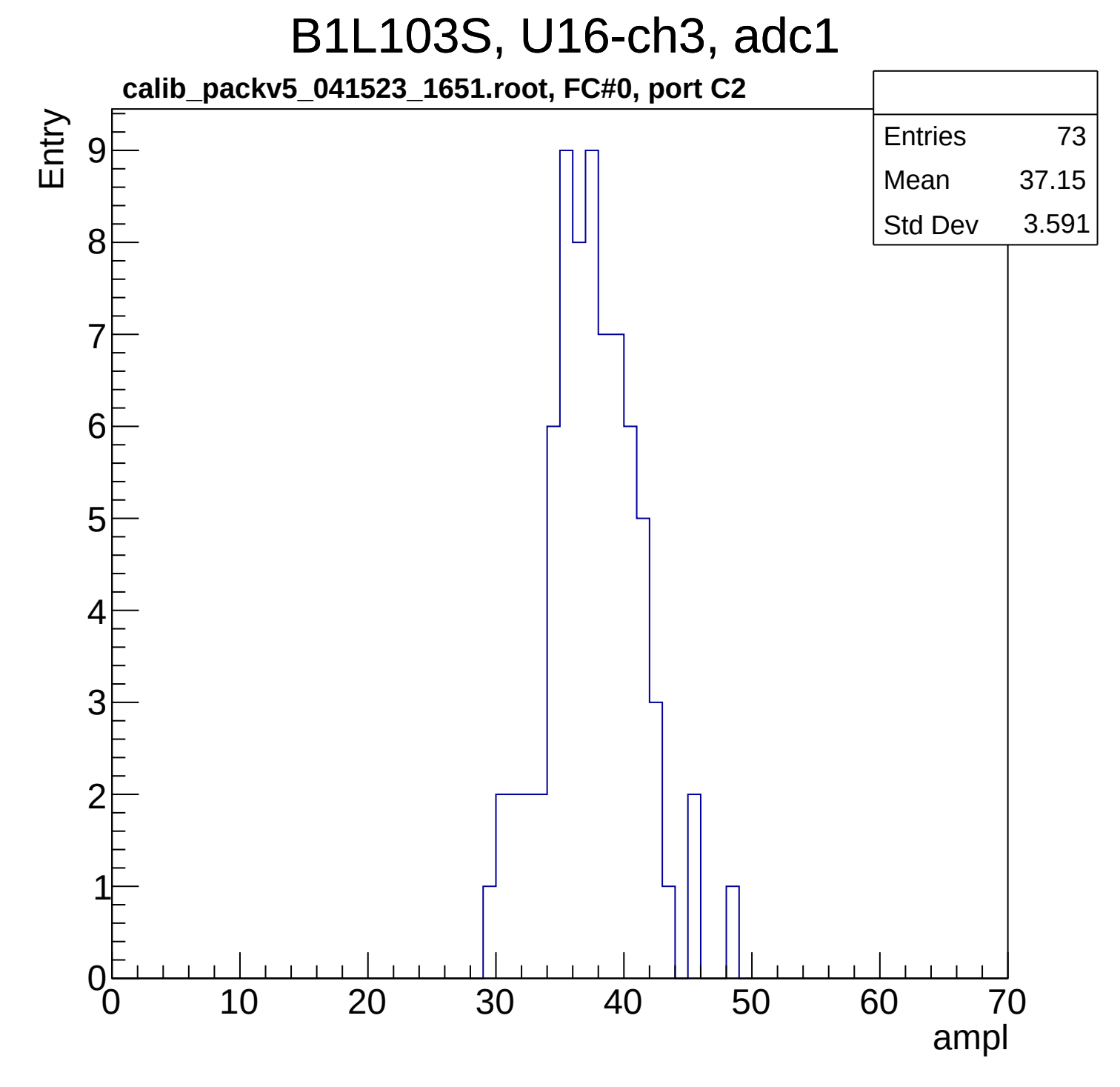
50
60
70
ampl


B1L103S, U16-ch3, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 37.15
Std Dev 3.591
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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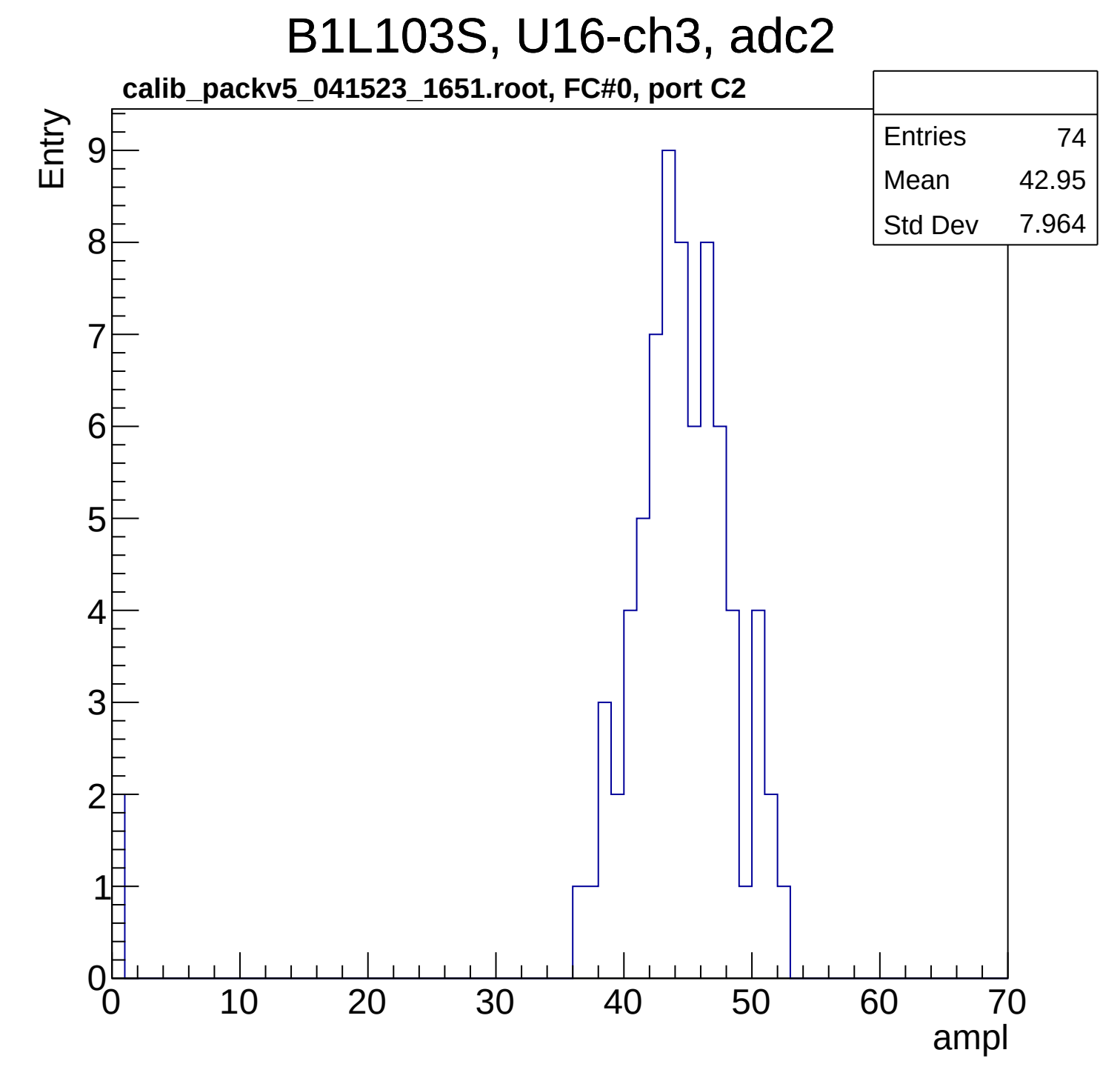
B1L103S, U16-ch3, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 42.95
Std Dev 7.964
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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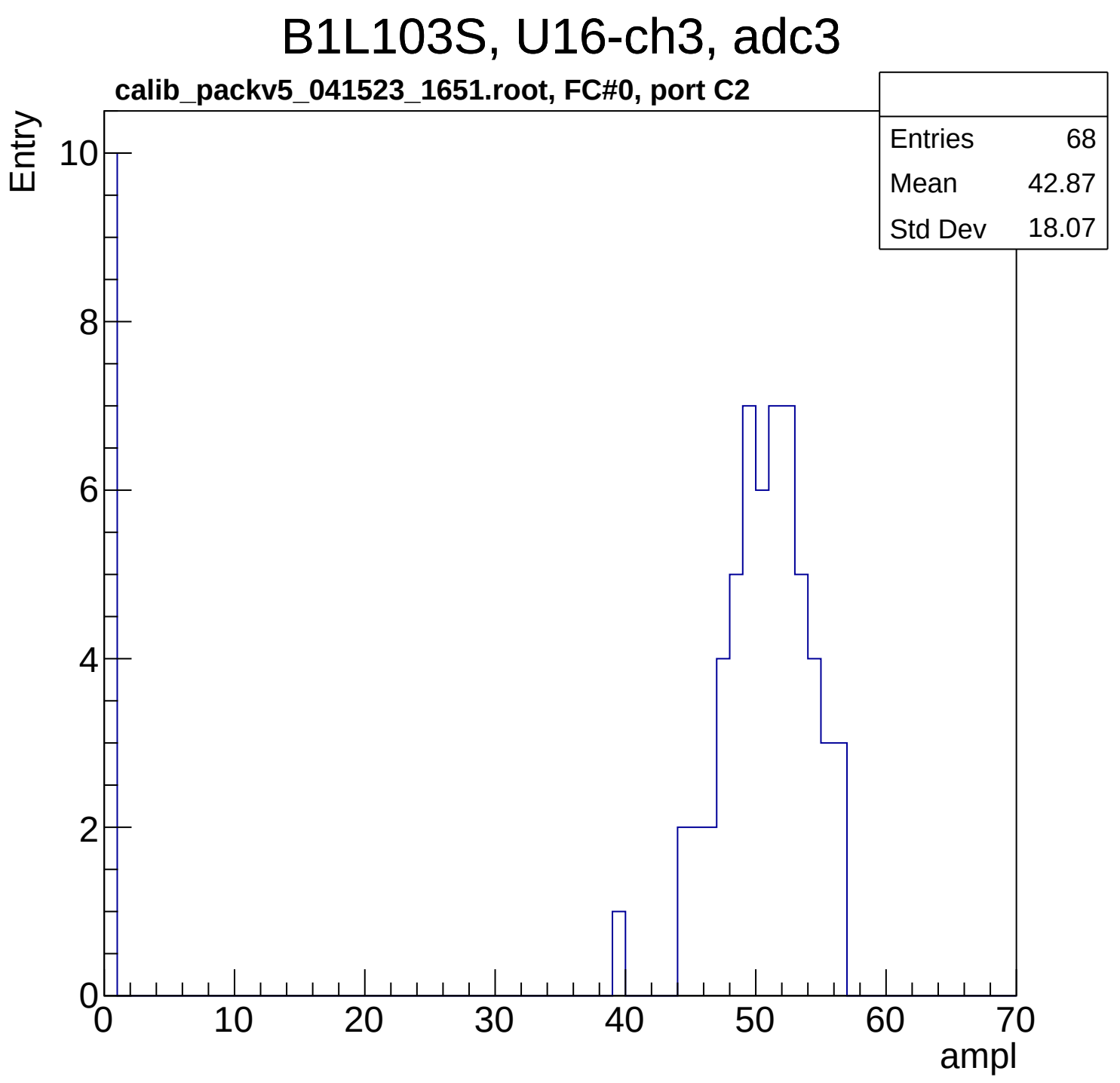
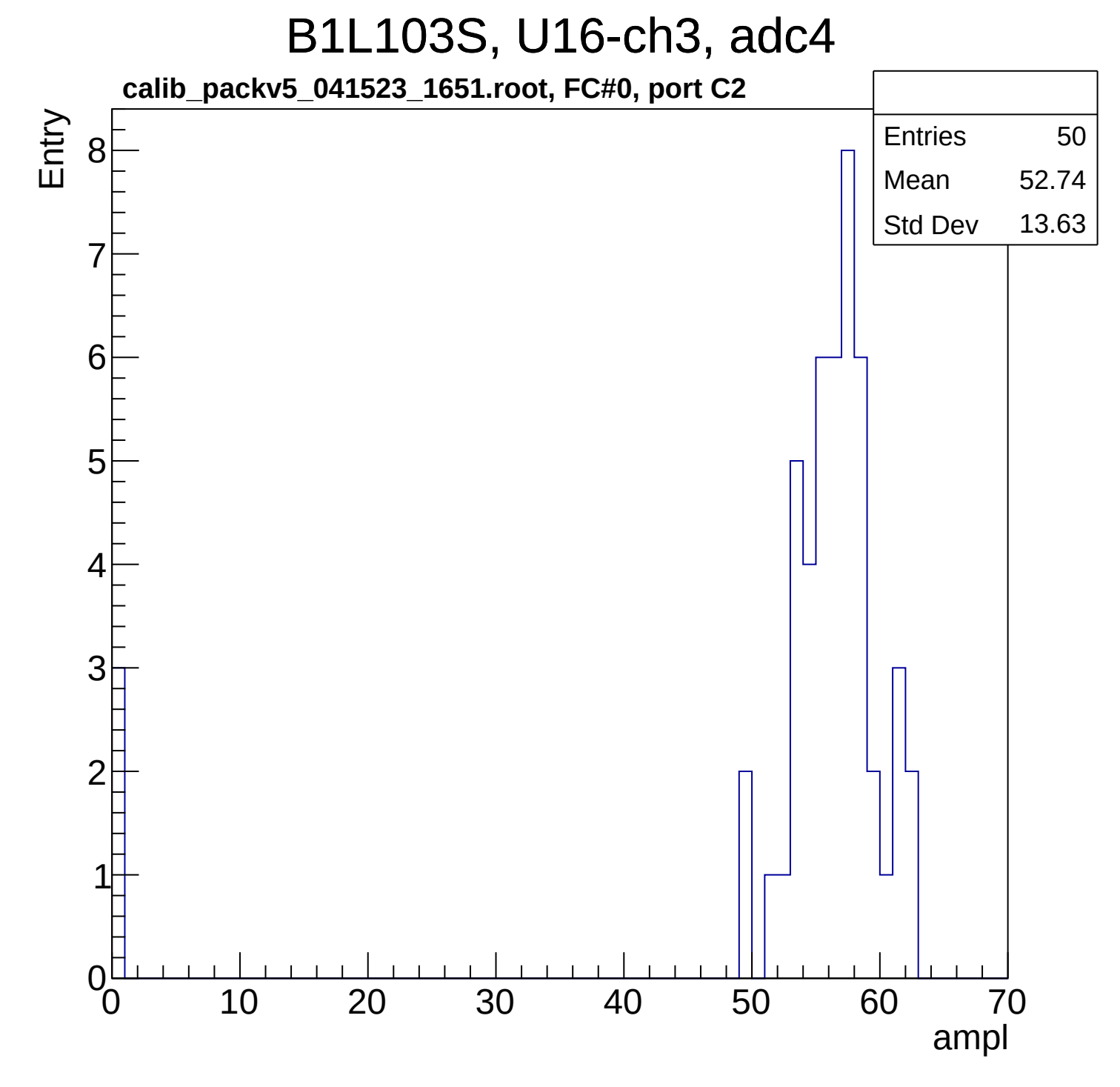
50
60
70


B1L103S, U16-ch3, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 42.87
Std Dev 18.07
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch3, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 52.74
Std Dev 13.63
Entry
ampl
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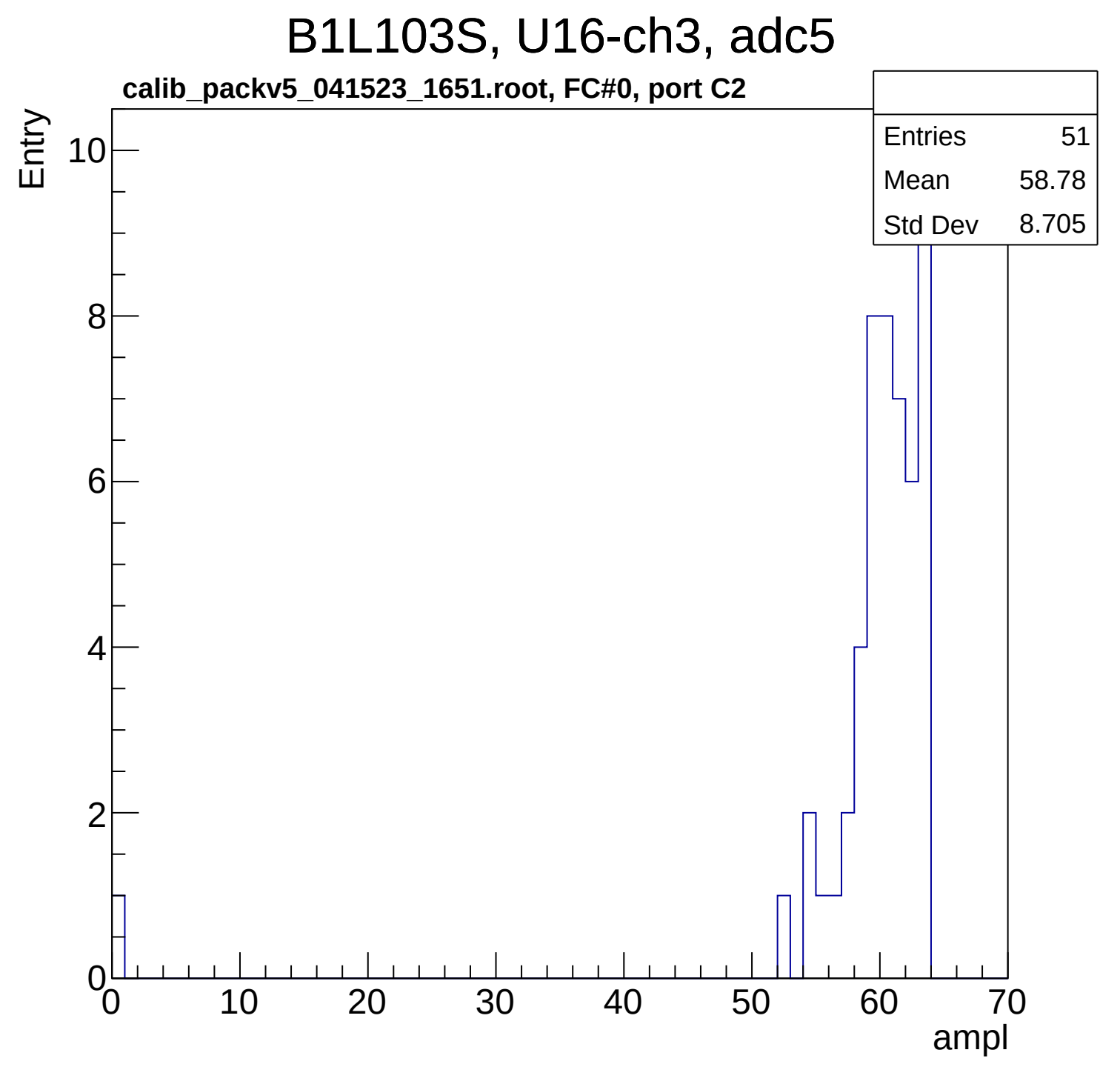
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch3, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.78
Std Dev 8.705
Entry
ampl
0
2
4
6
8
10
0
10
20
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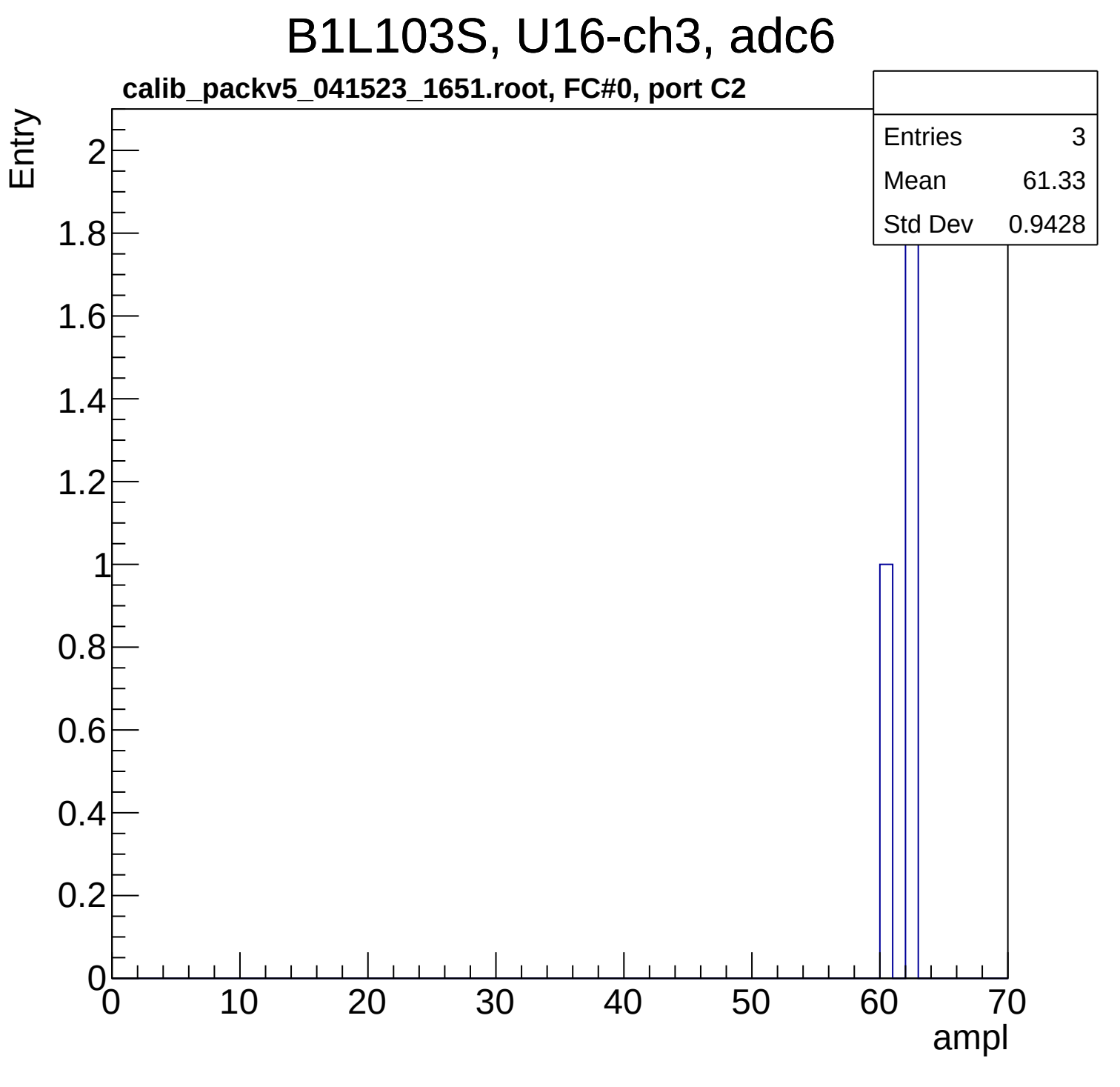
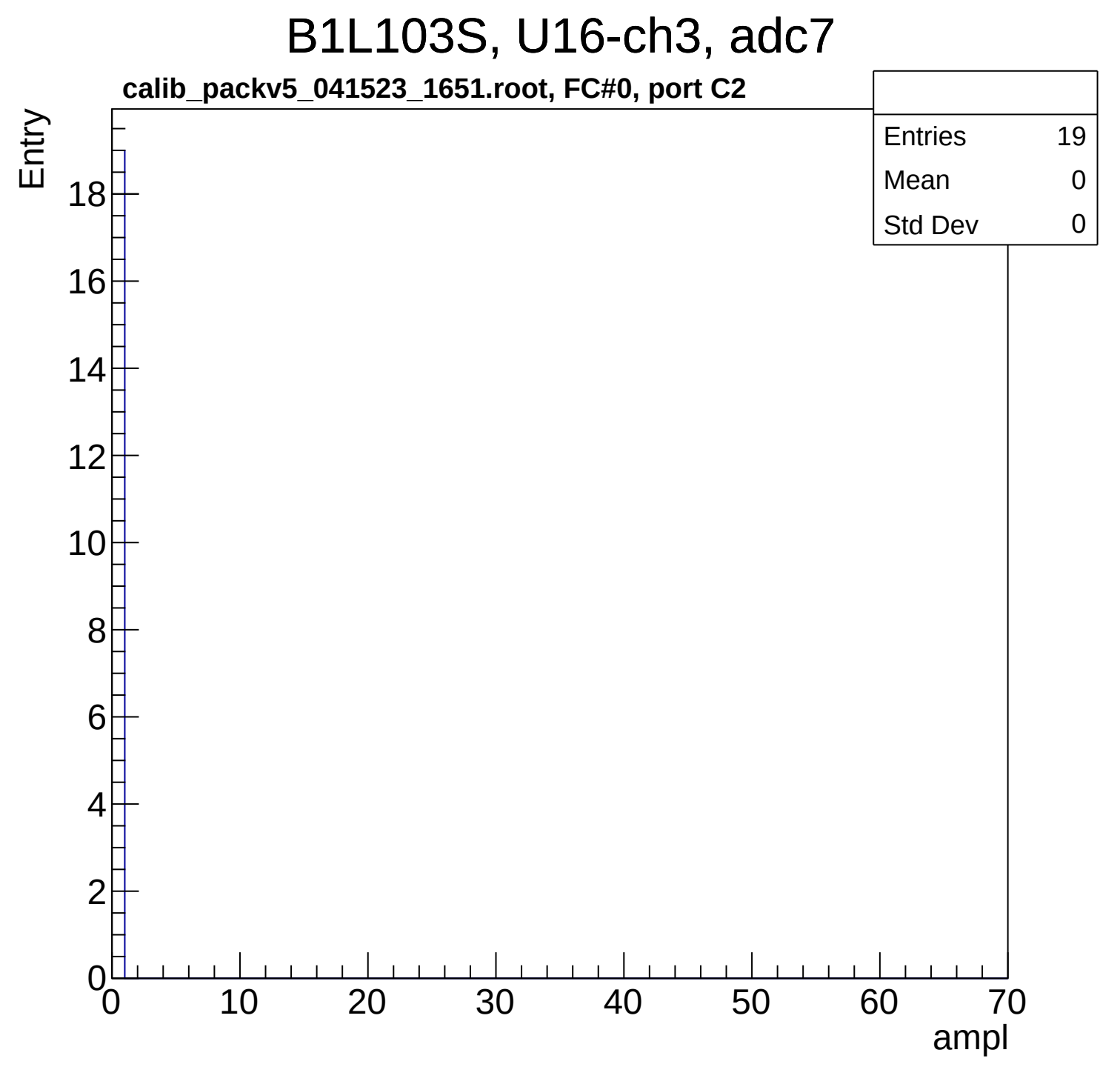
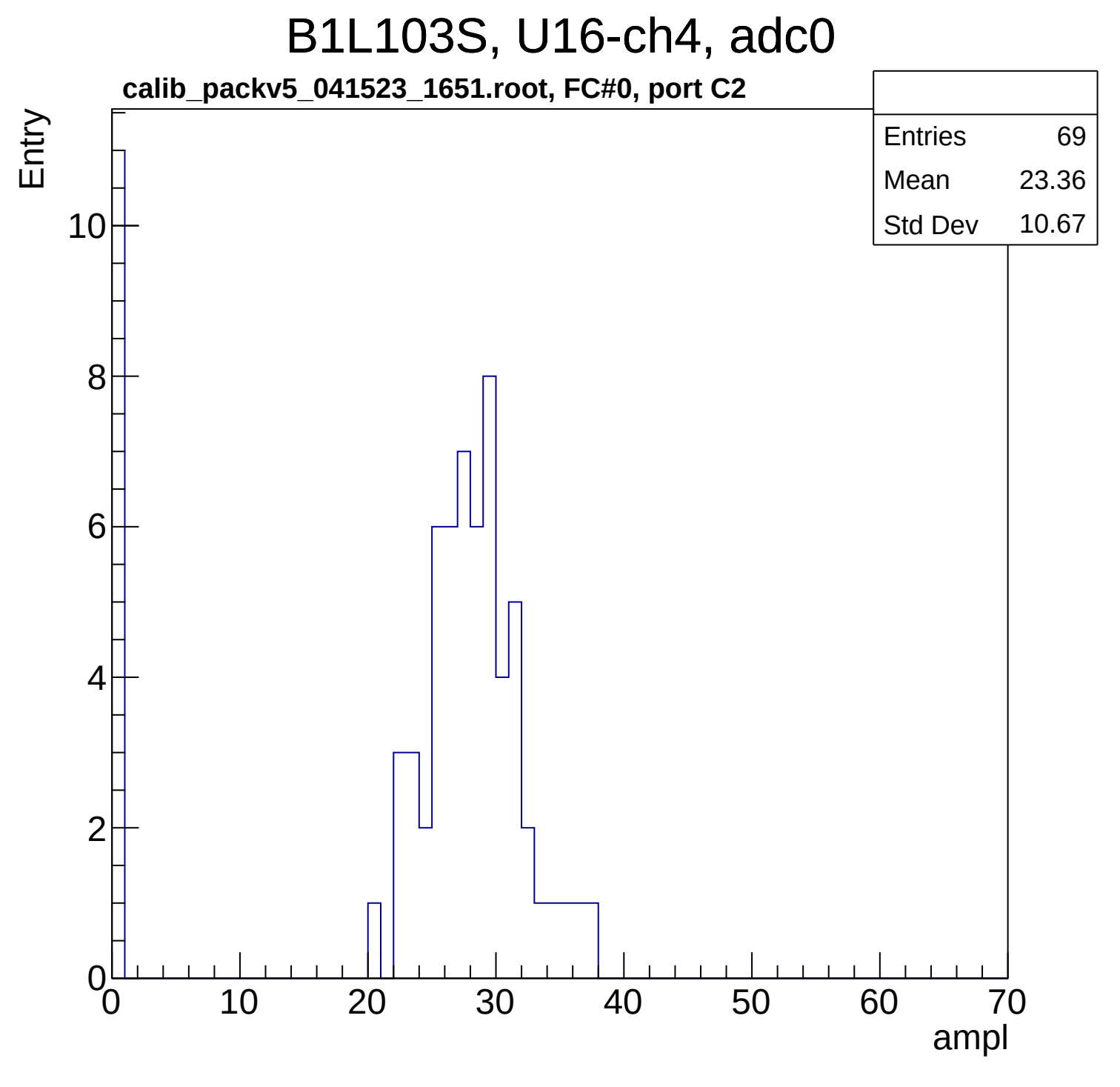
40
50
60
70


B1L103S, U16-ch3, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 61.33
Std Dev 0.9428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U16-ch3, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch4, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 23.36
Std Dev 10.67
Entry
0
2
4
6
8
10
0
10
20
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50
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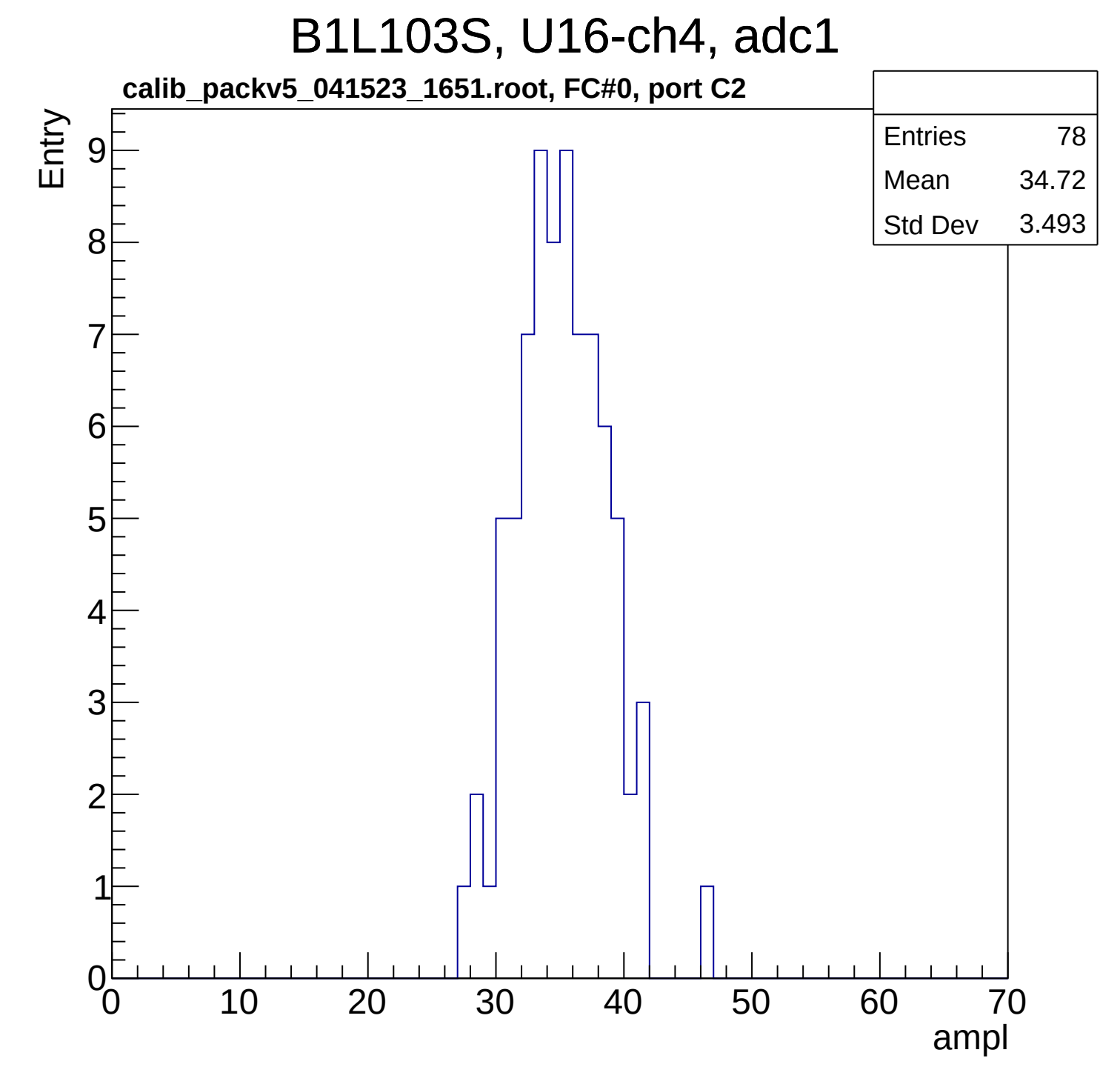
70
ampl


B1L103S, U16-ch4, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 34.72
Std Dev 3.493
Entry
ampl
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3
4
5
6
7
8
9
0
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60
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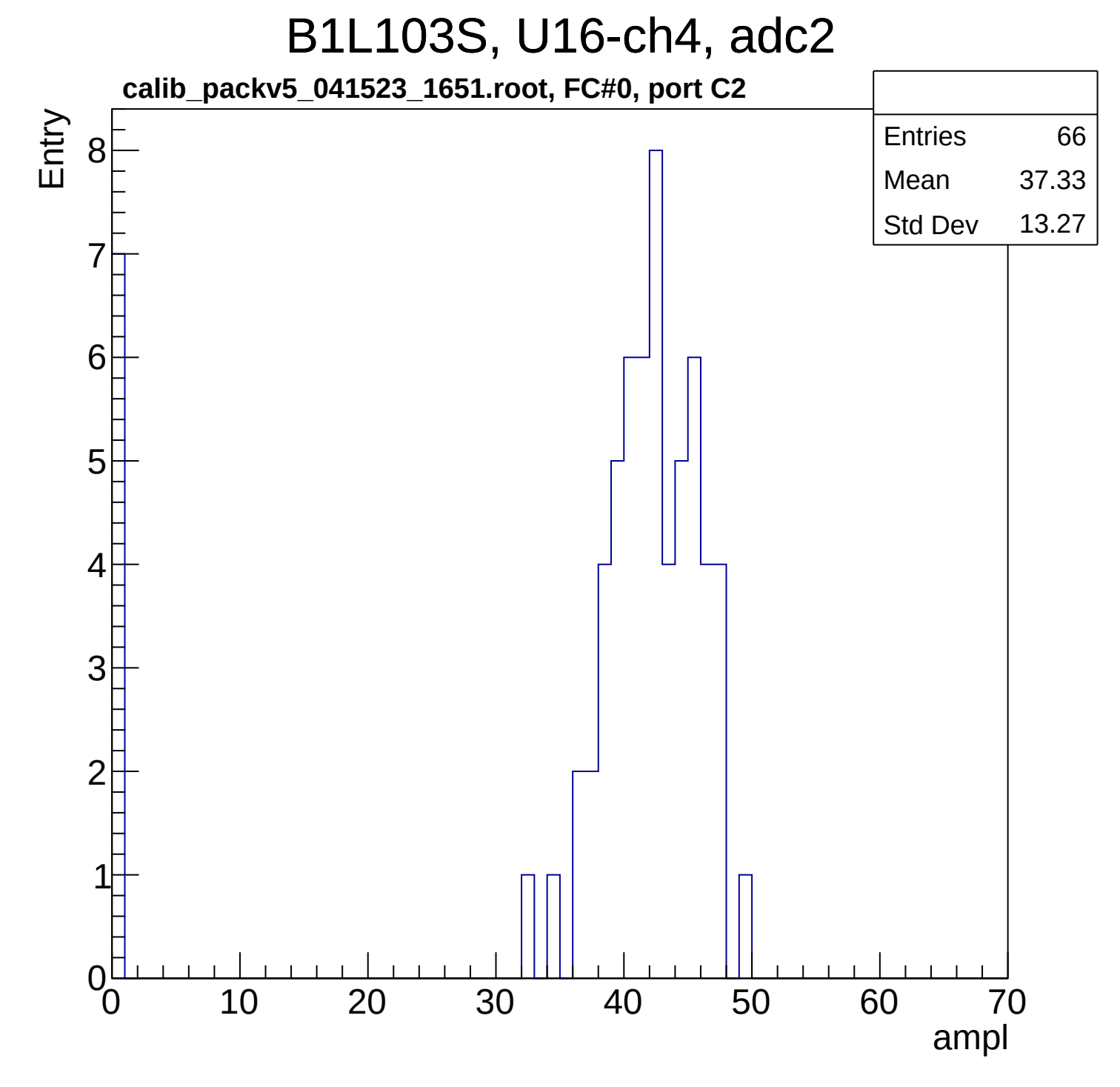
B1L103S, U16-ch4, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 37.33
Std Dev 13.27
Entry
ampl
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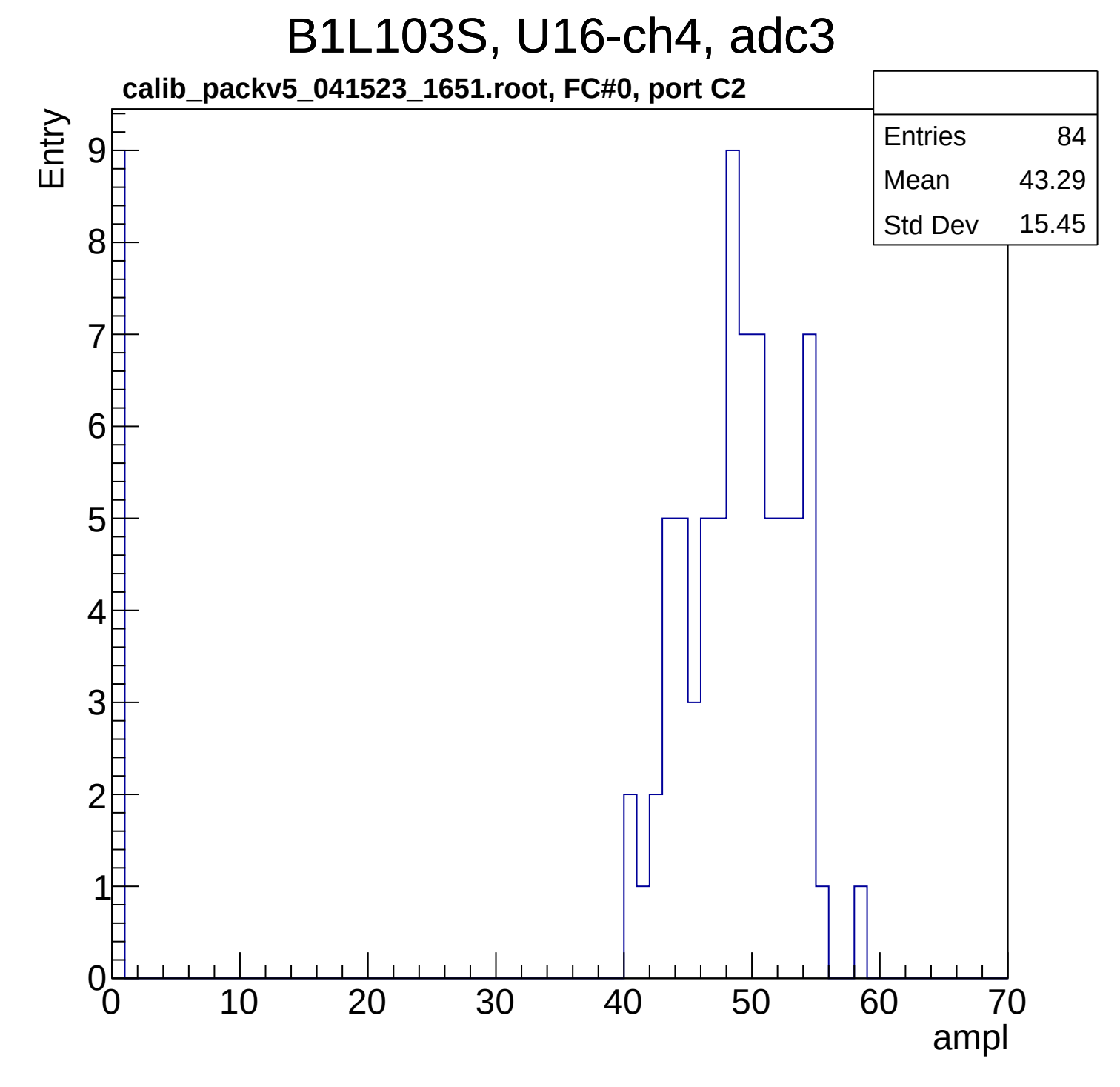
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch4, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 43.29
Std Dev 15.45
Entry
ampl
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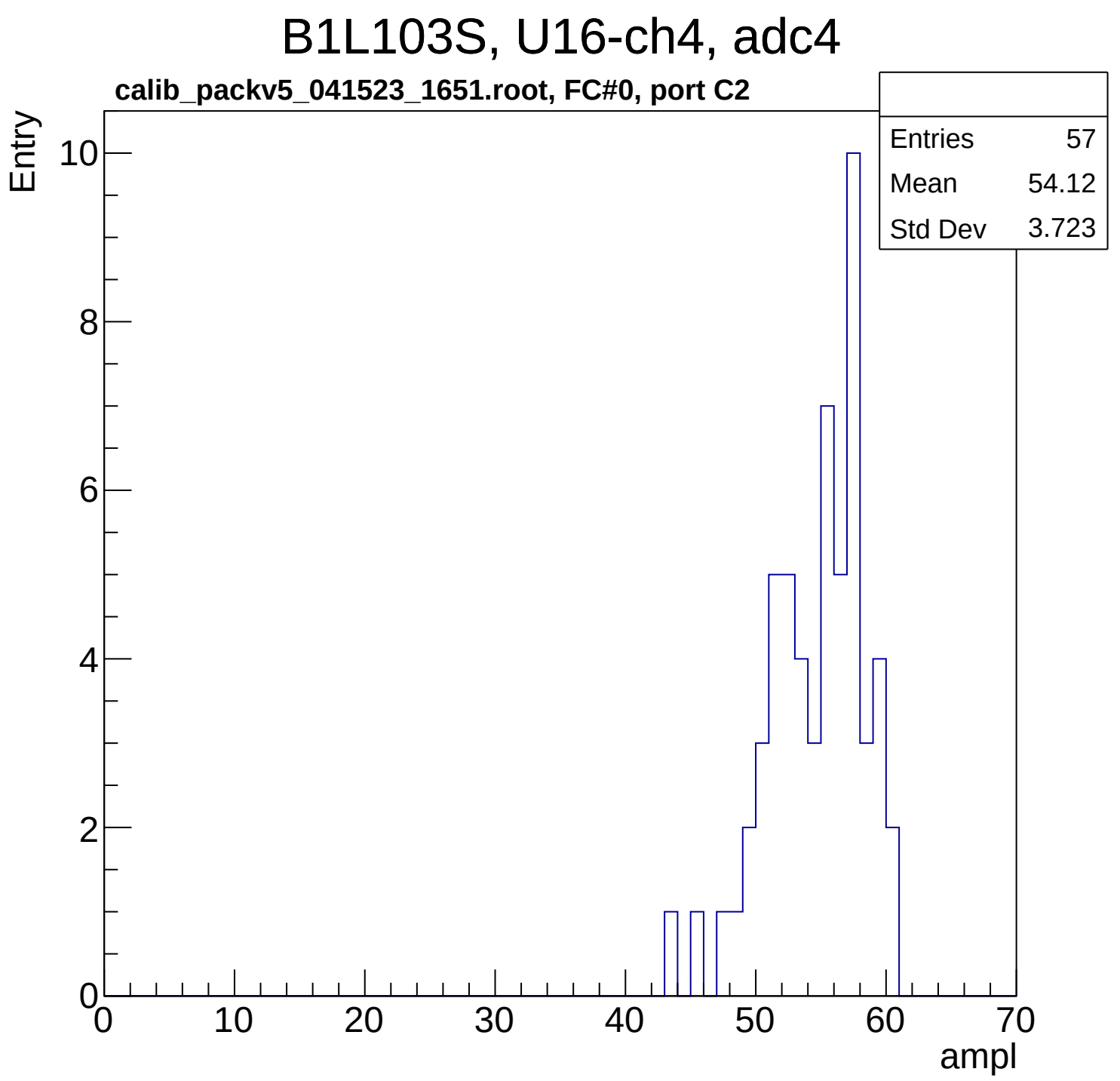
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch4, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 54.12
Std Dev 3.723
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
50
60
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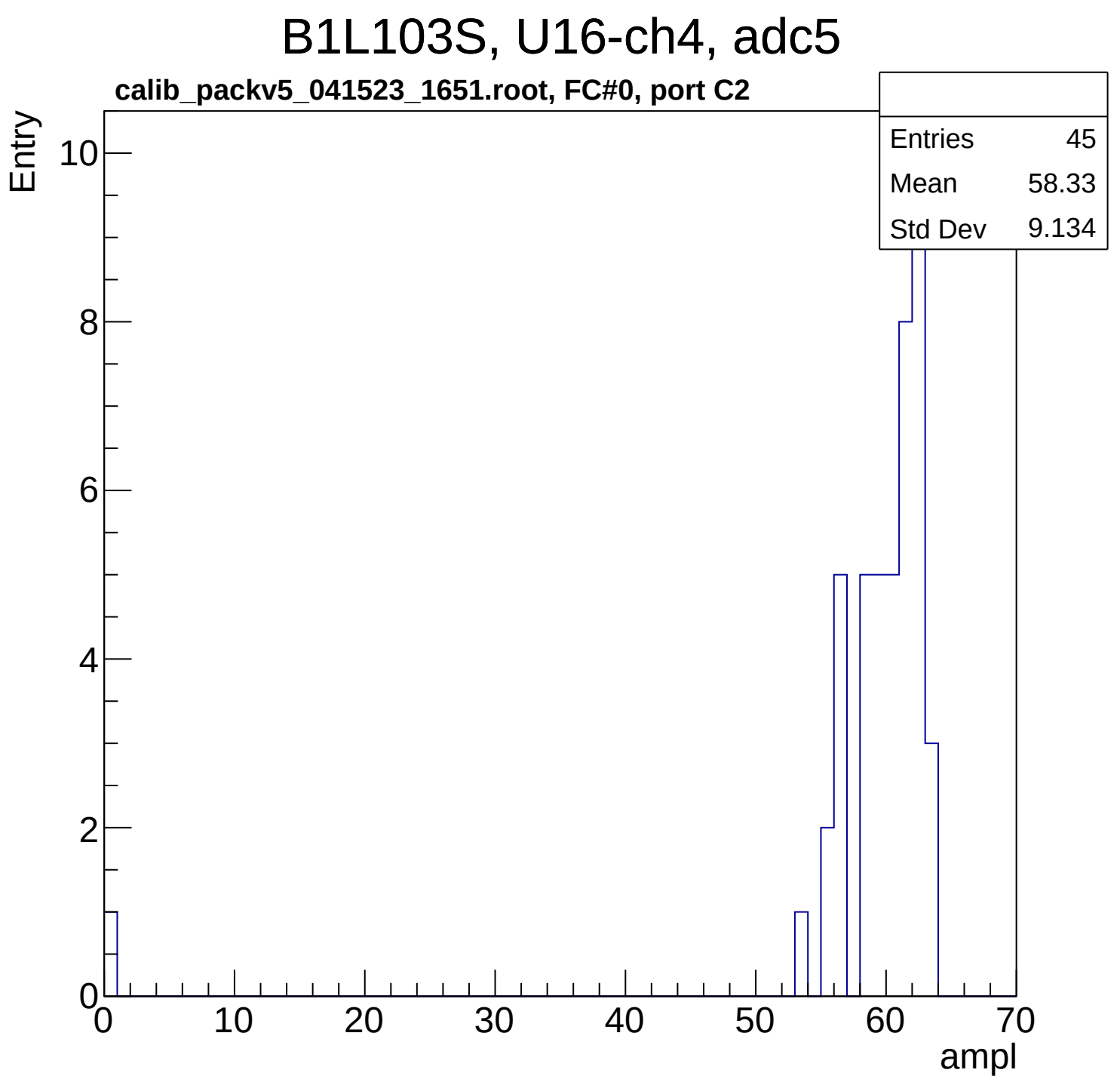
B1L103S, U16-ch4, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.33
Std Dev 9.134
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
50
60
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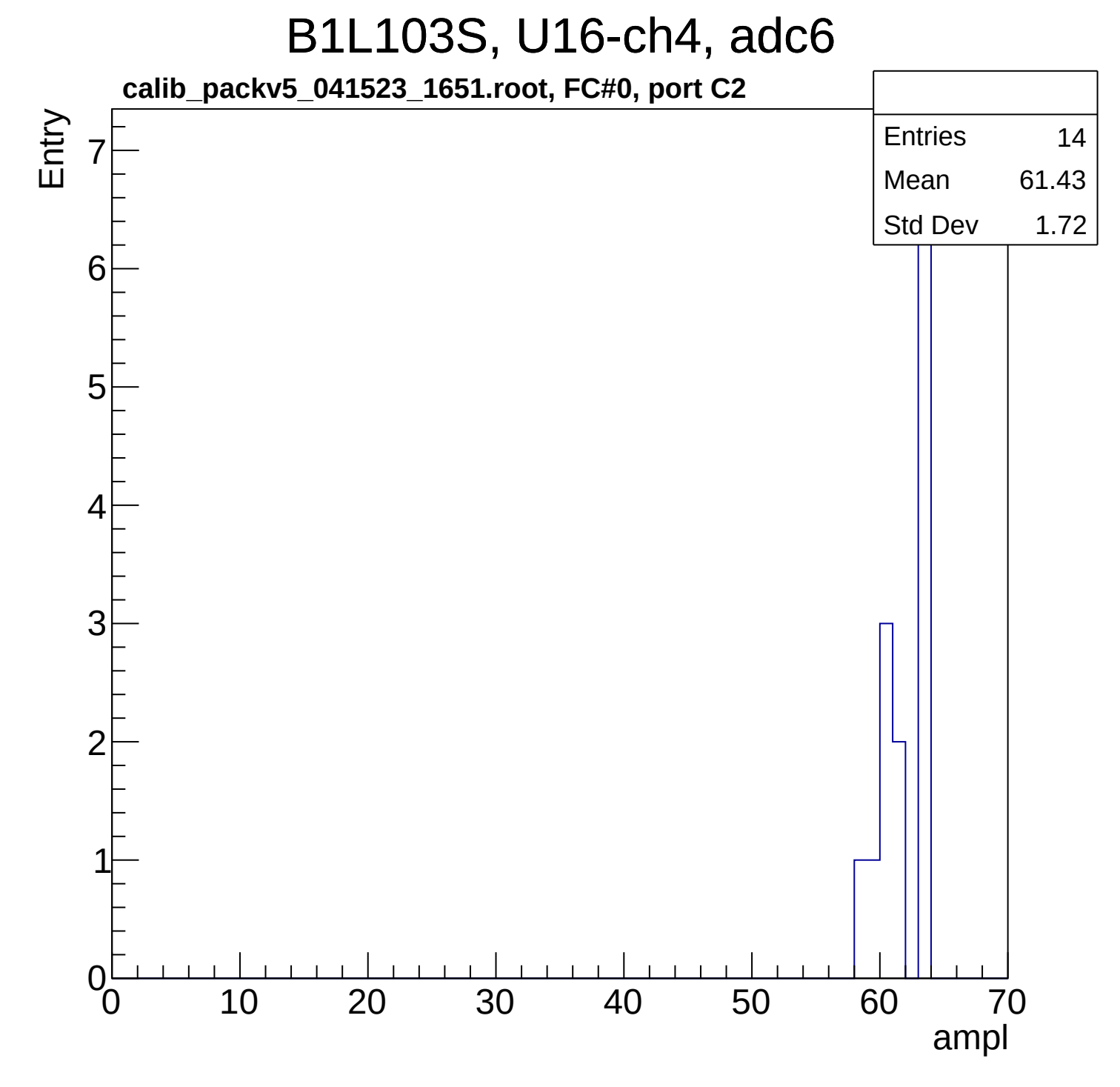
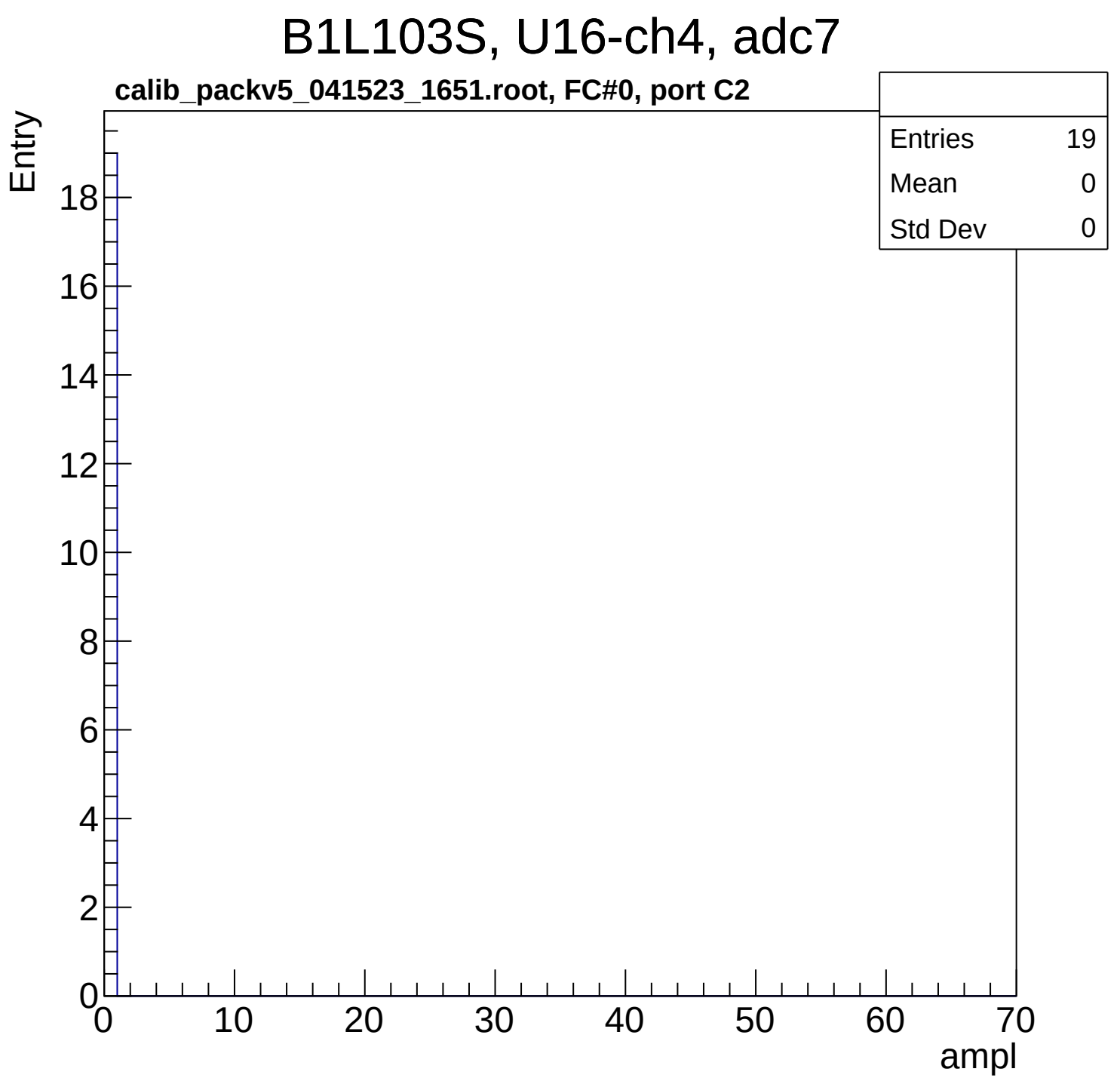
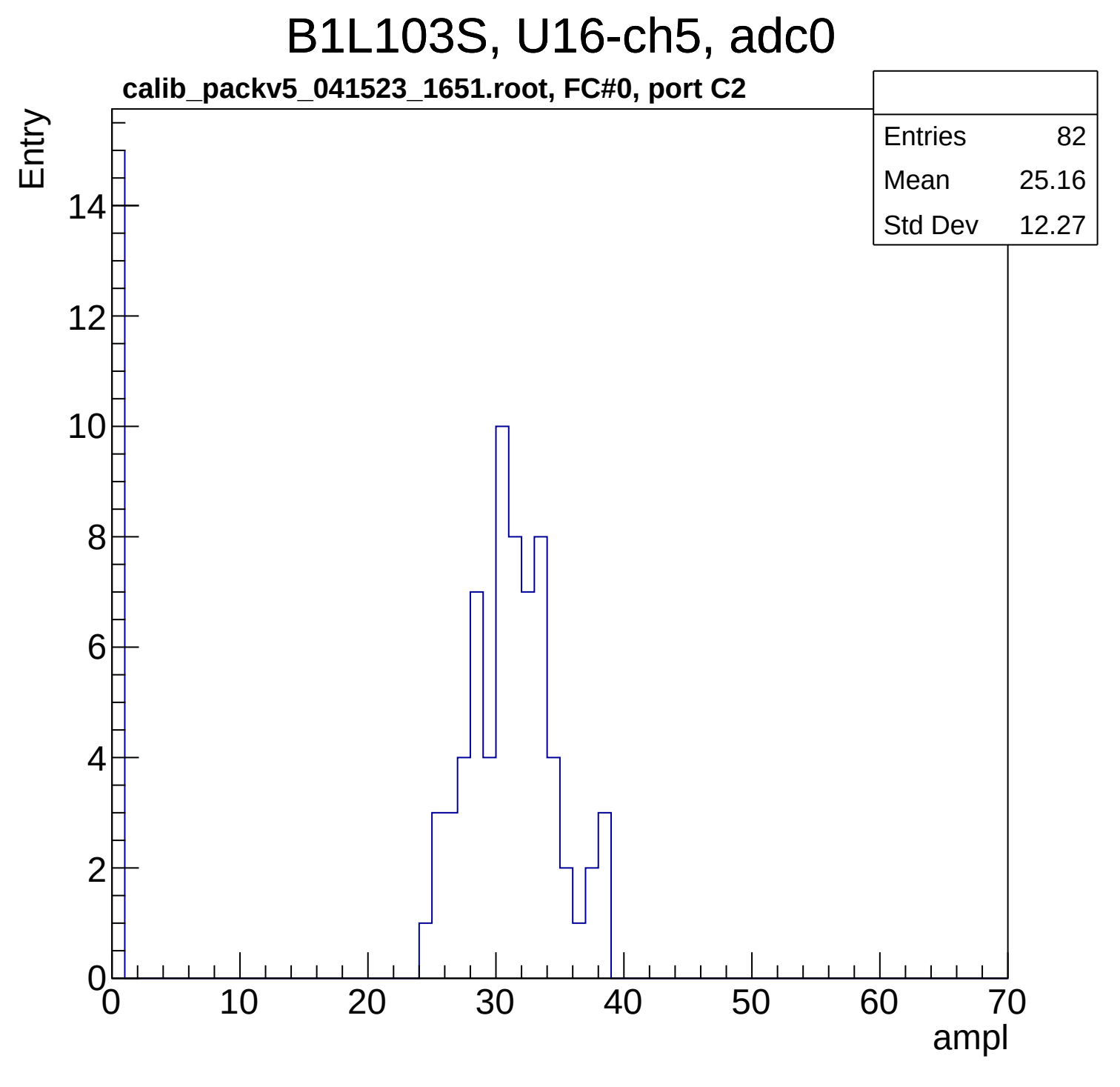
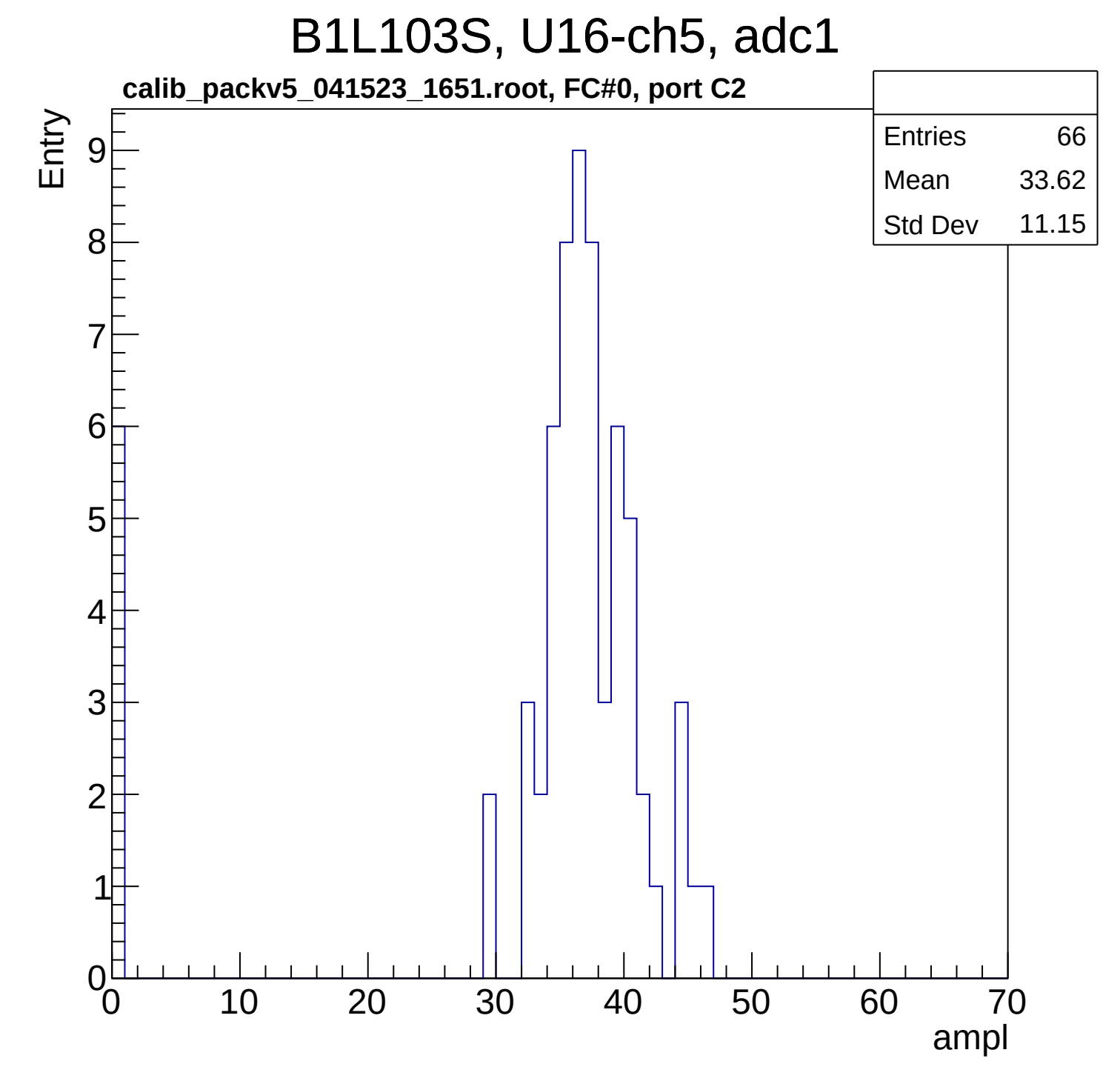
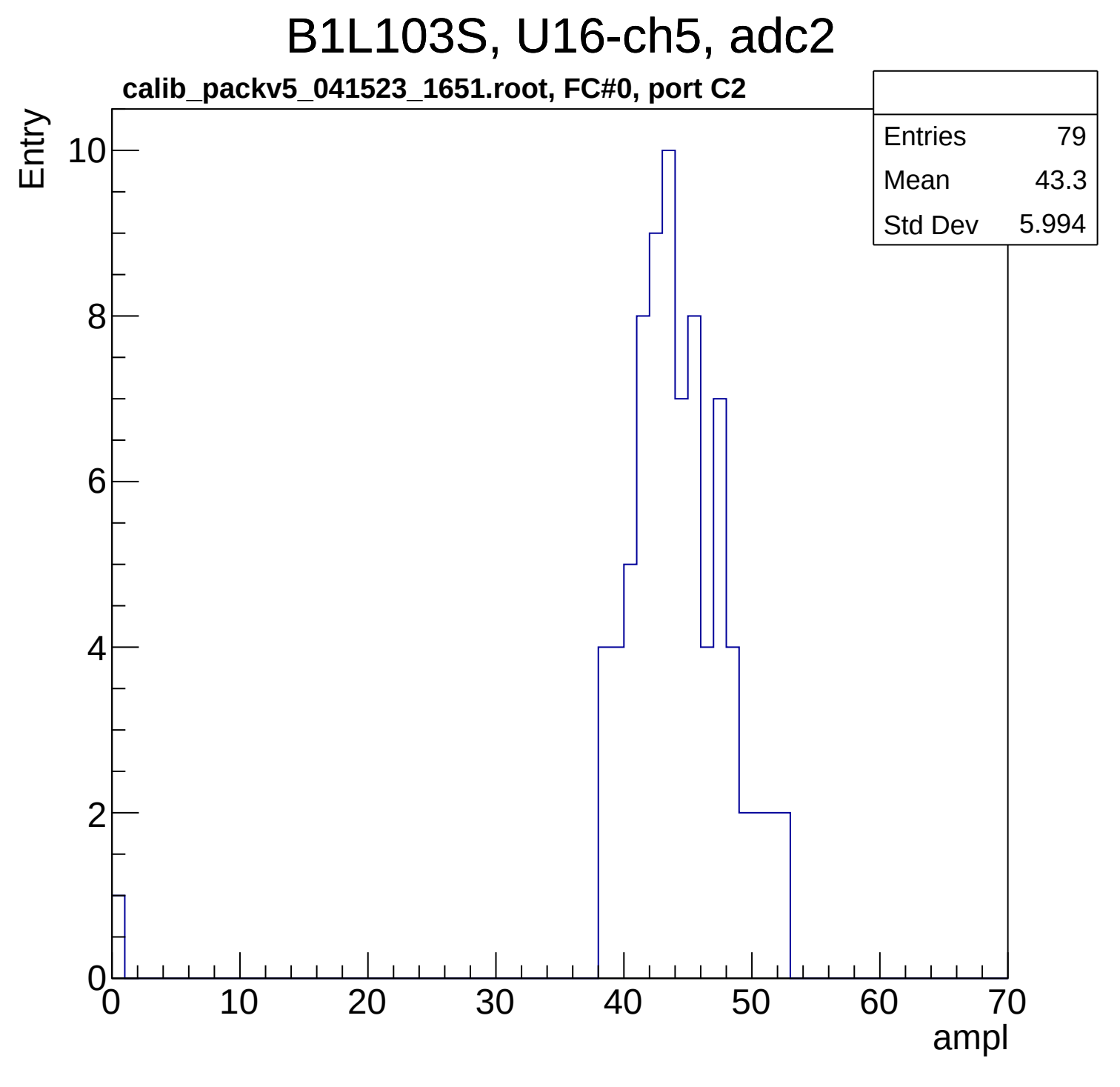
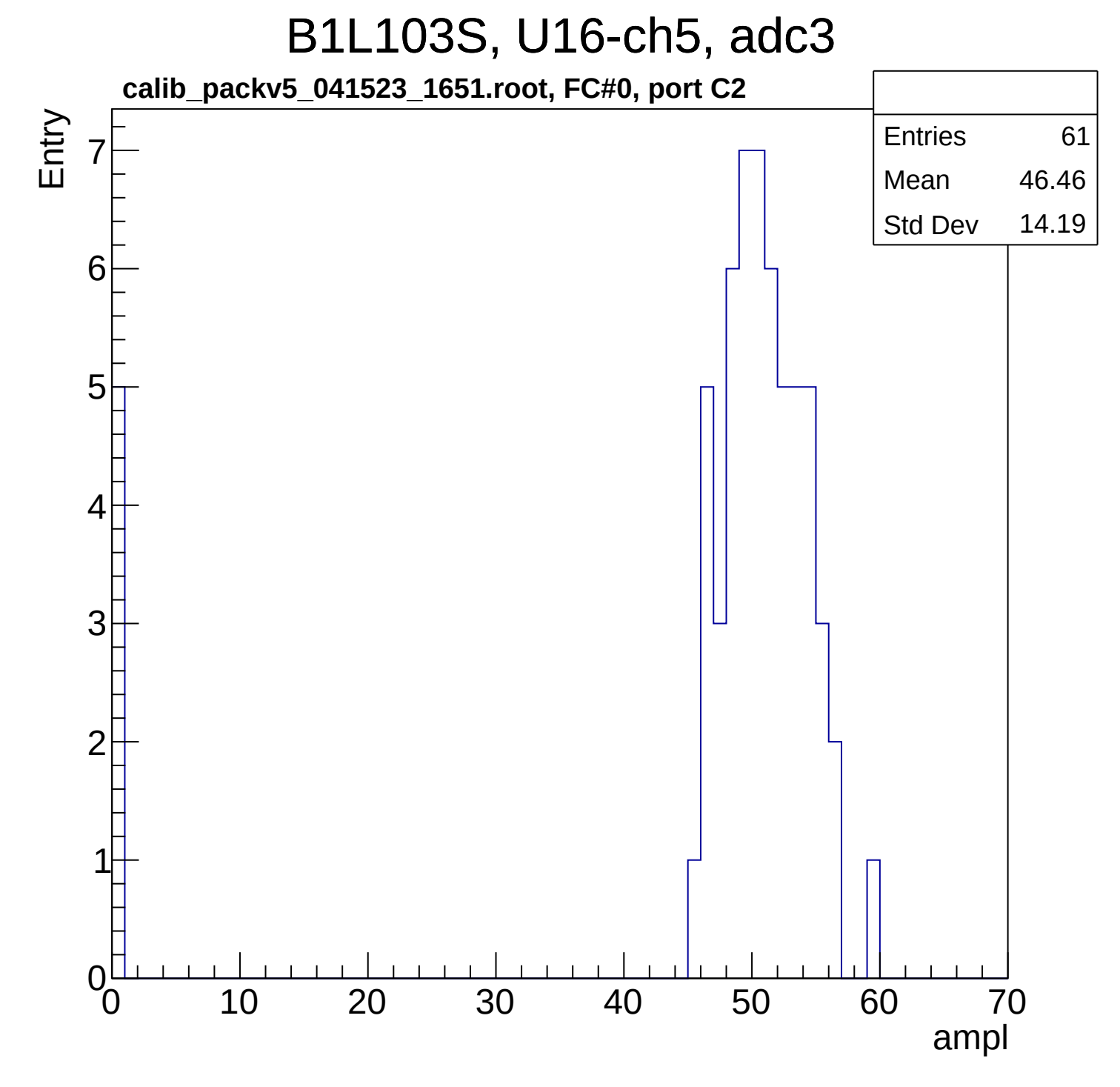

B1L103S, U16-ch4, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.43
Std Dev 1.72
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch4, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch5, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 25.16
Std Dev 12.27
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch5, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 33.62
Std Dev 11.15
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch5, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 43.3
Std Dev 5.994
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch5, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 46.46
Std Dev 14.19
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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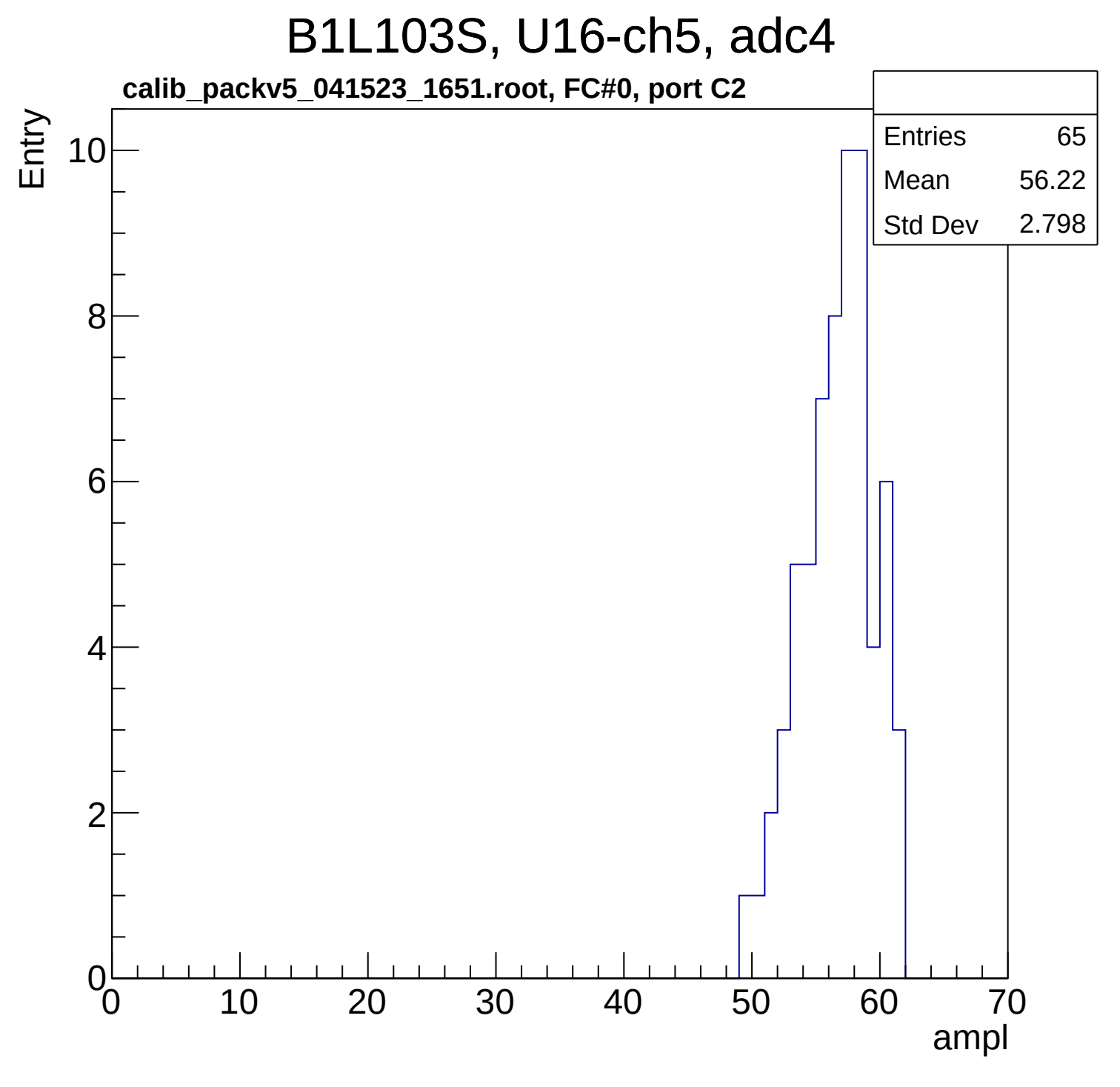
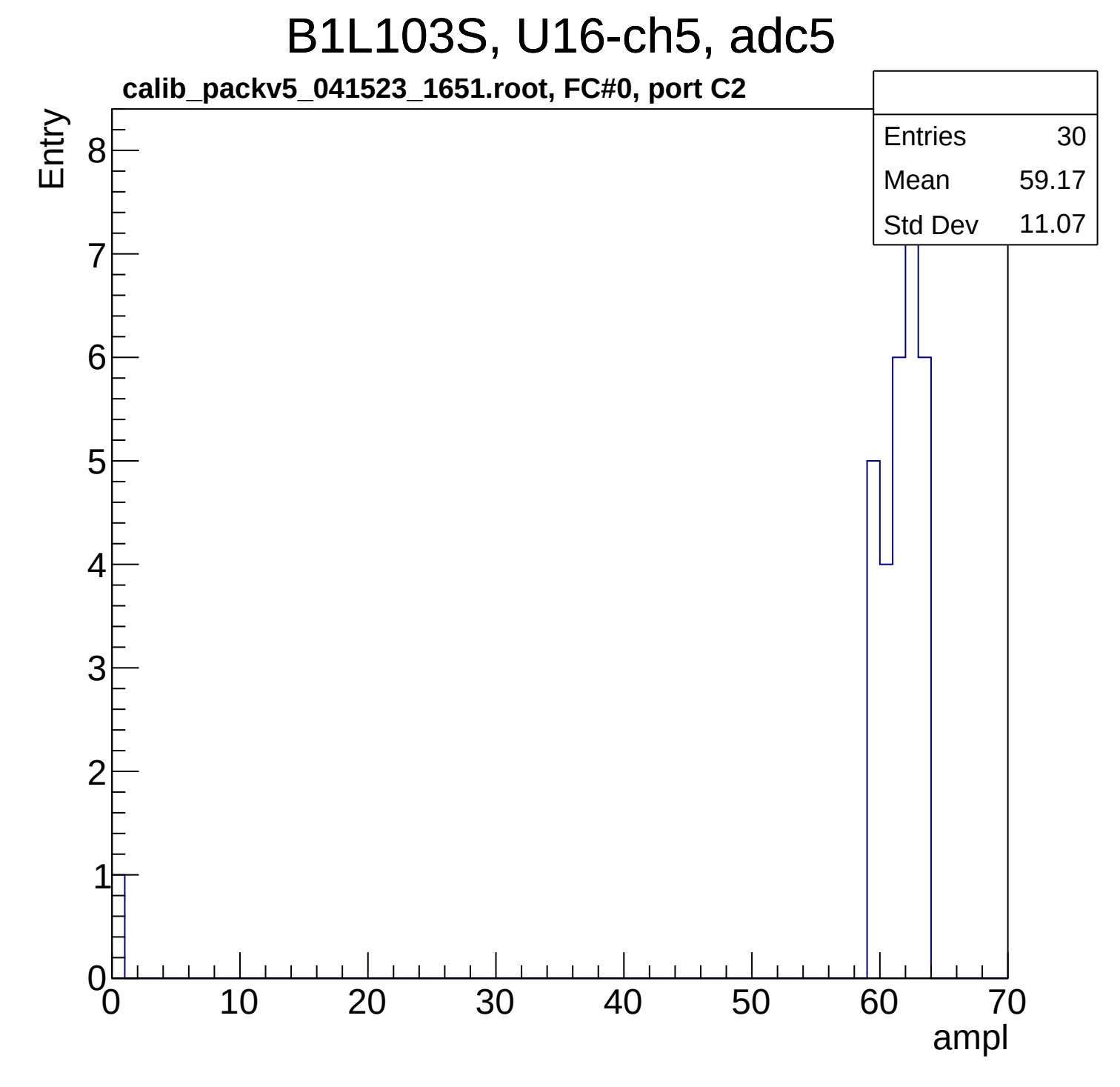
40
50
60
70


B1L103S, U16-ch5, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 56.22
Std Dev 2.798
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch5, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 59.17
Std Dev 11.07
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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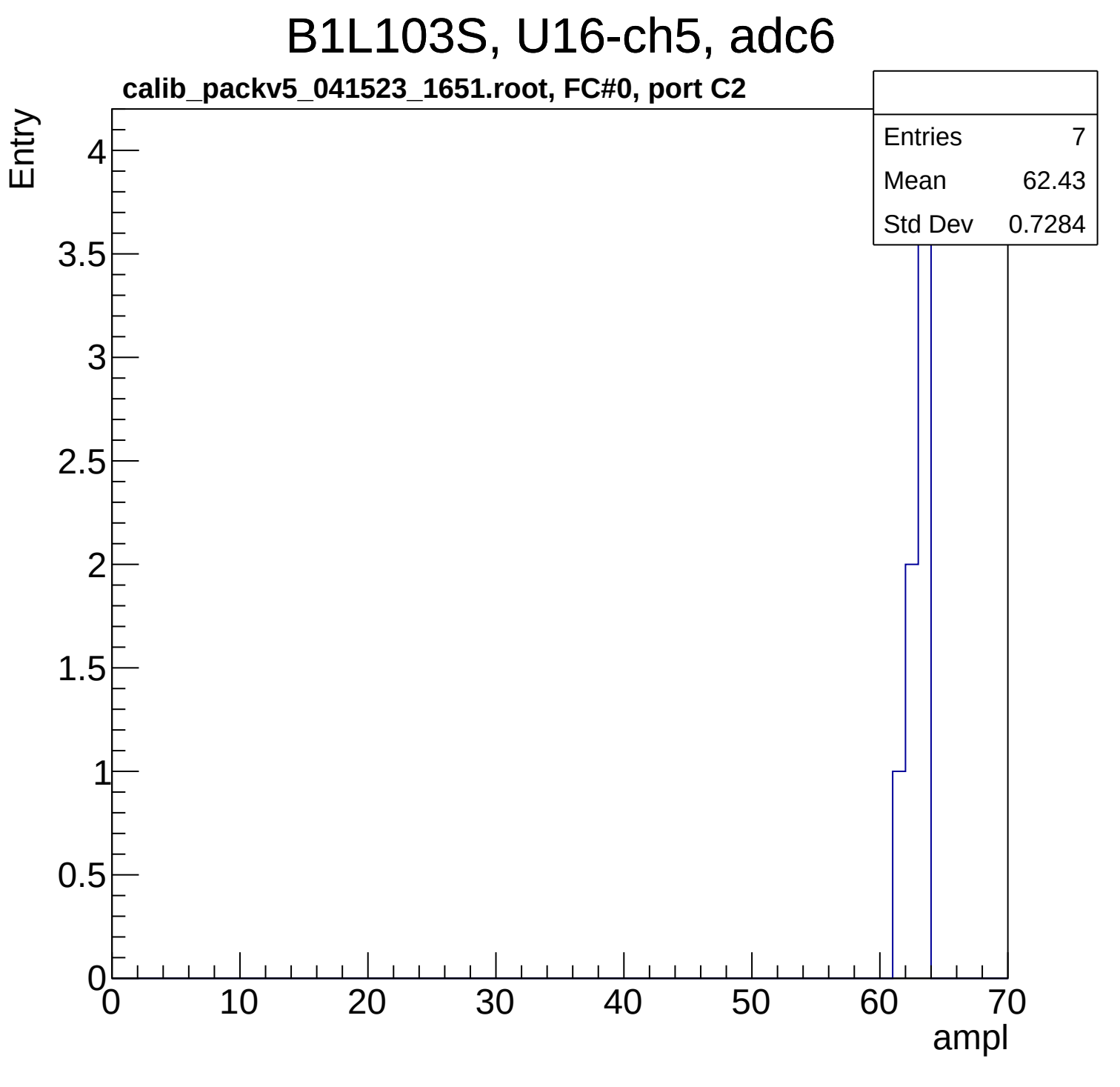
B1L103S, U16-ch5, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62.43
Std Dev 0.7284
Entry
ampl
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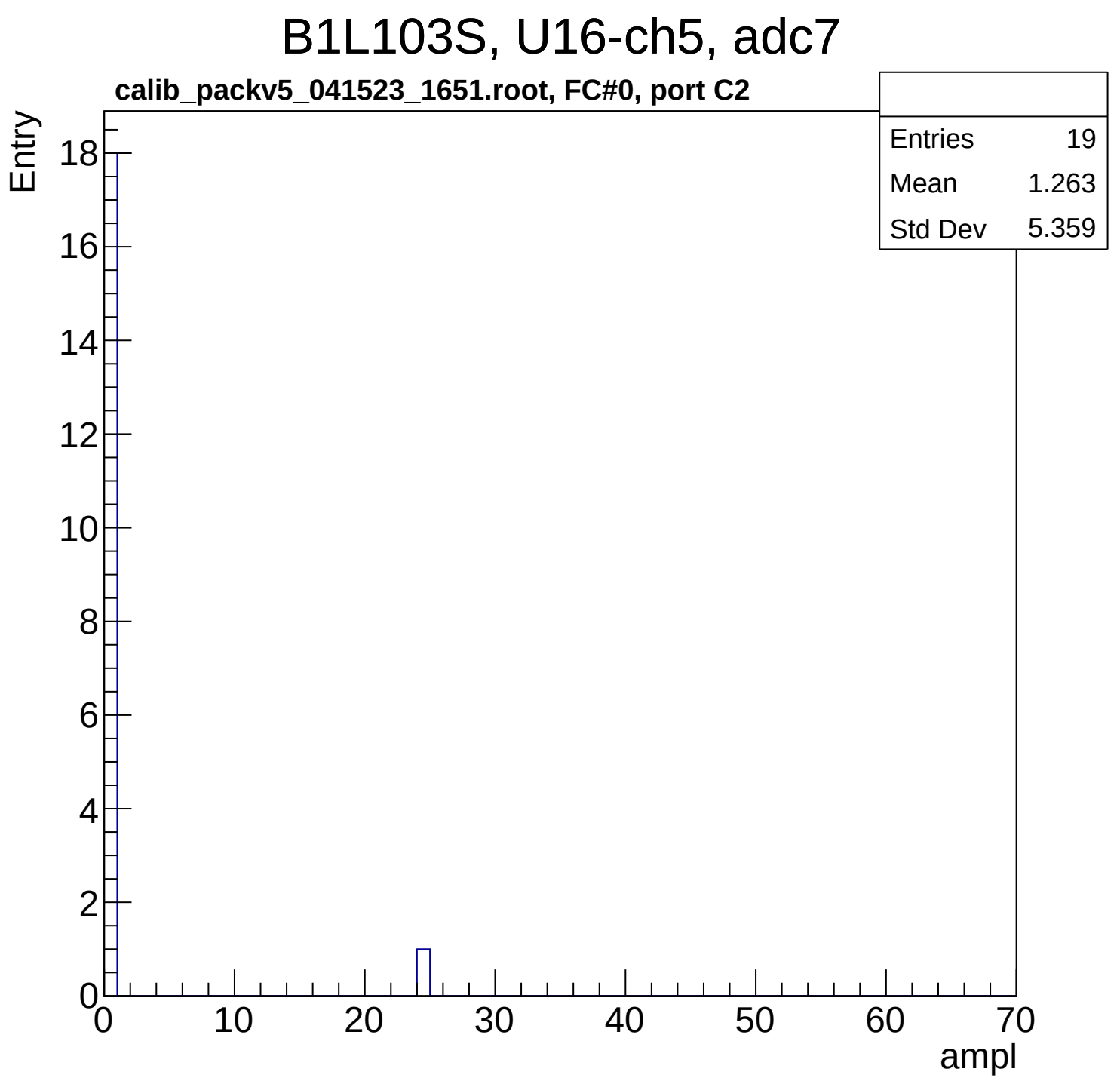
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U16-ch5, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.263
Std Dev 5.359
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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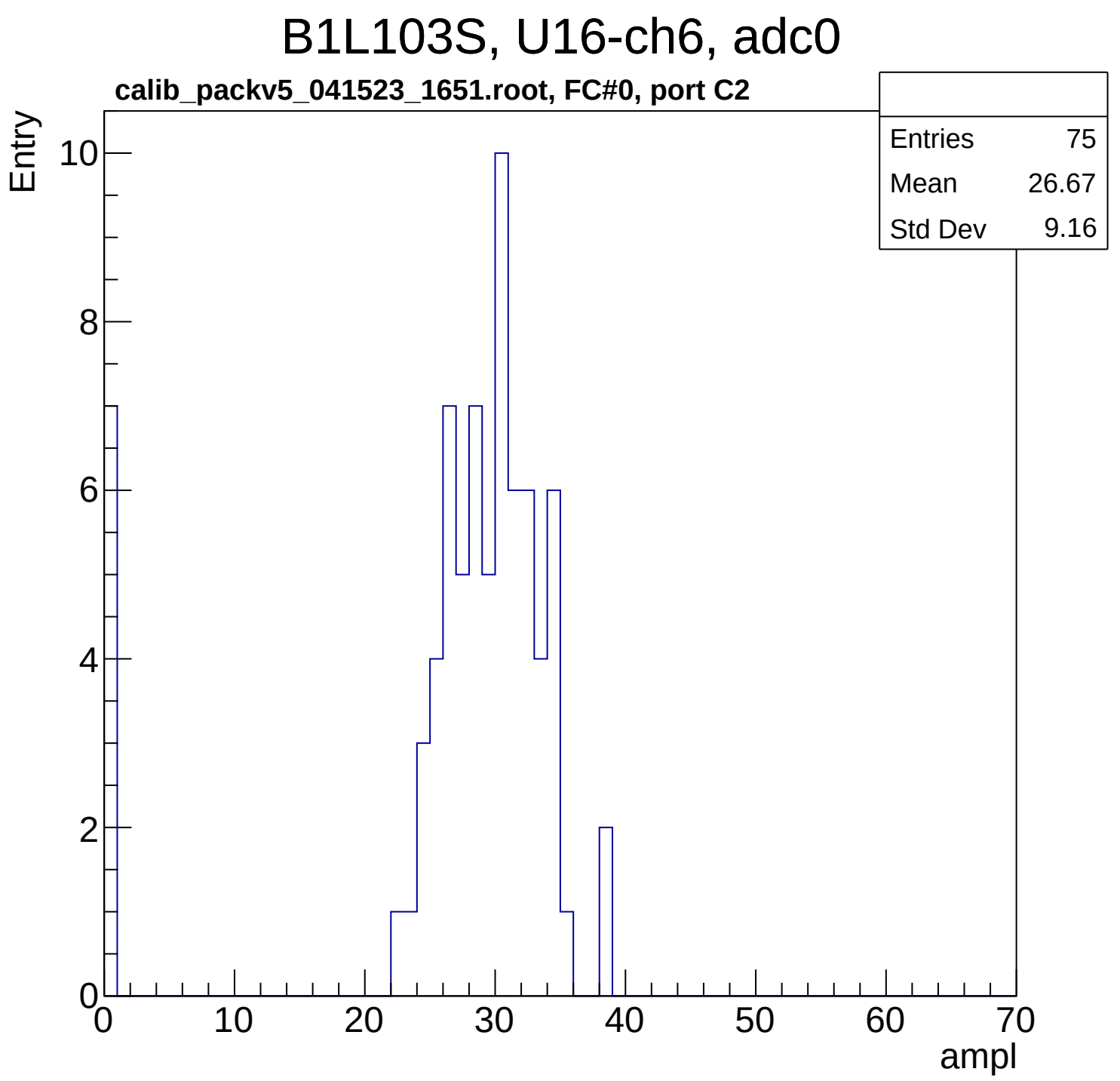
B1L103S, U16-ch6, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 26.67
Std Dev 9.16
Entry
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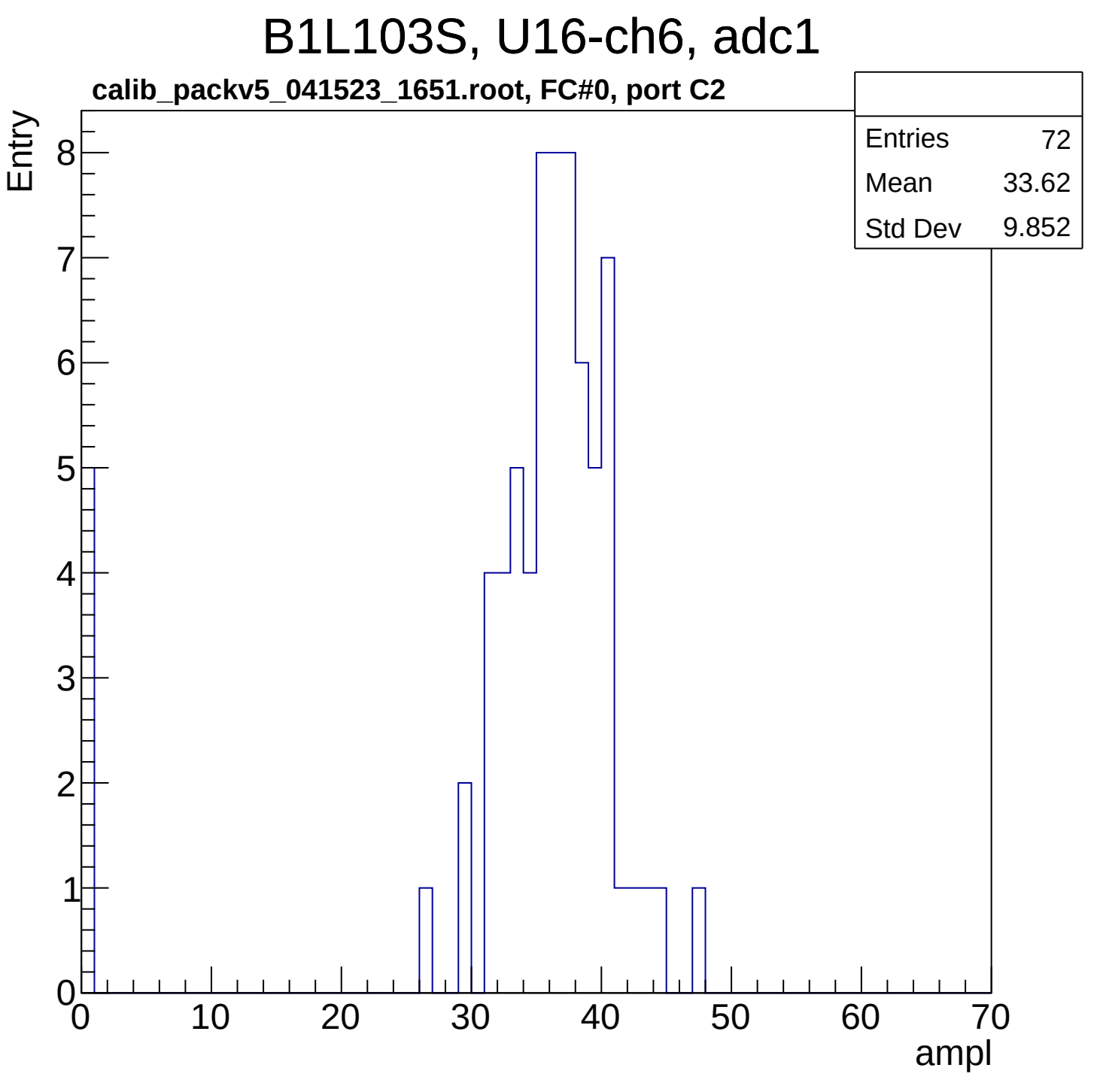
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch6, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 33.62
Std Dev 9.852
Entry
ampl
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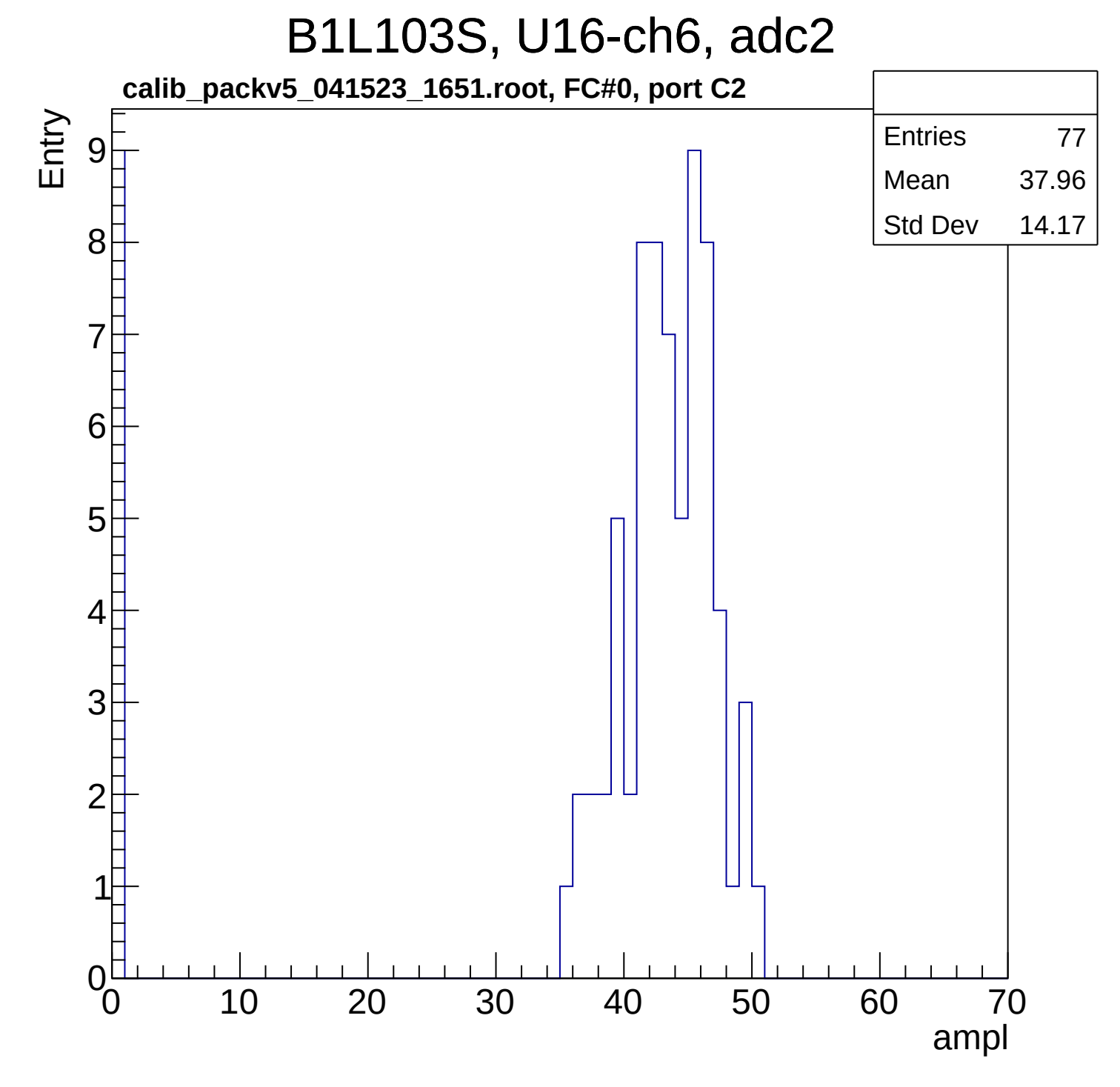
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch6, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 37.96
Std Dev 14.17
Entry
ampl
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2
3
4
5
6
7
8
9
0
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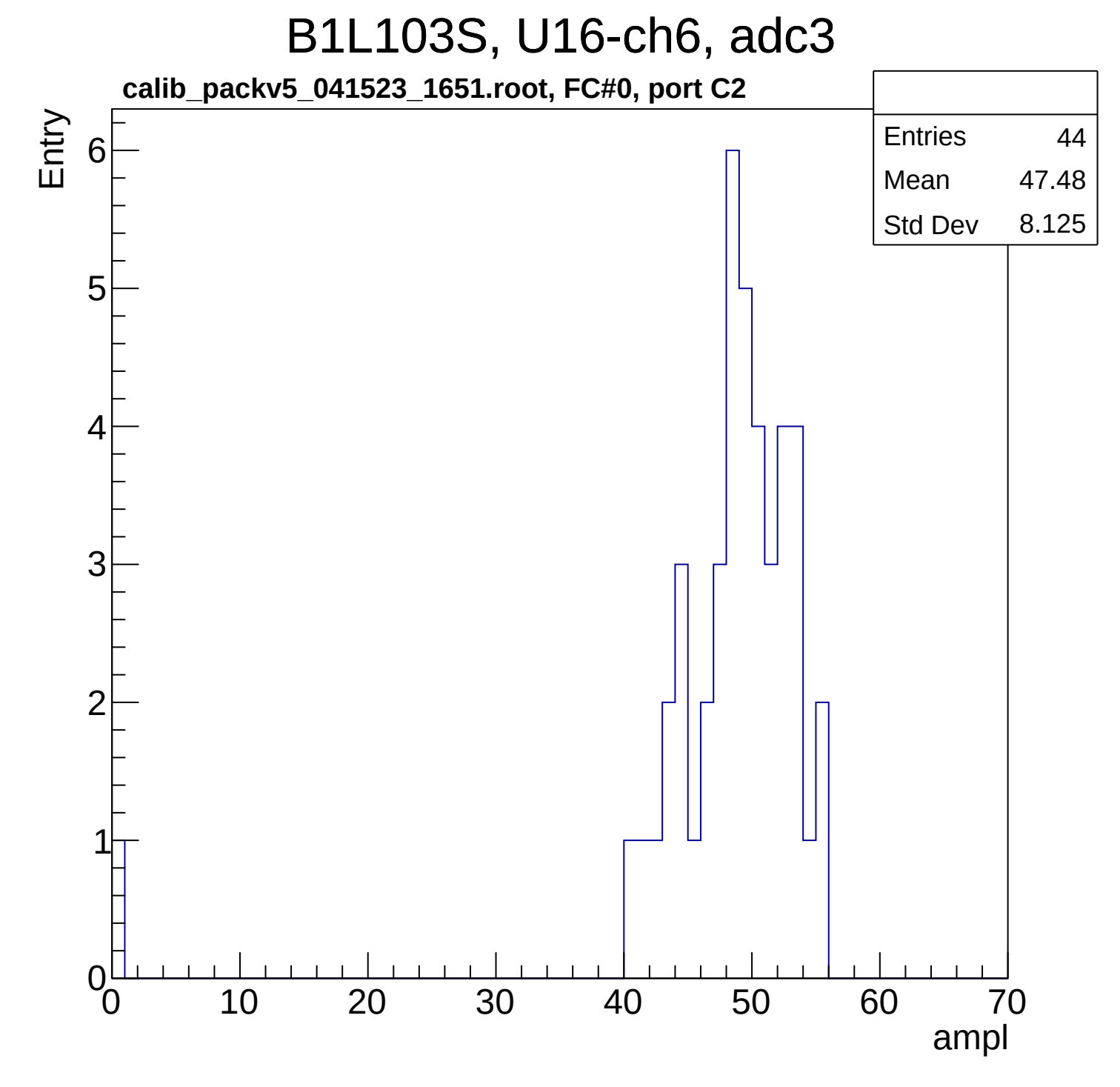
40
50
60
70


B1L103S, U16-ch6, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 47.48
Std Dev 8.125
Entry
ampl
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1
2
3
4
5
6
0
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20
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40
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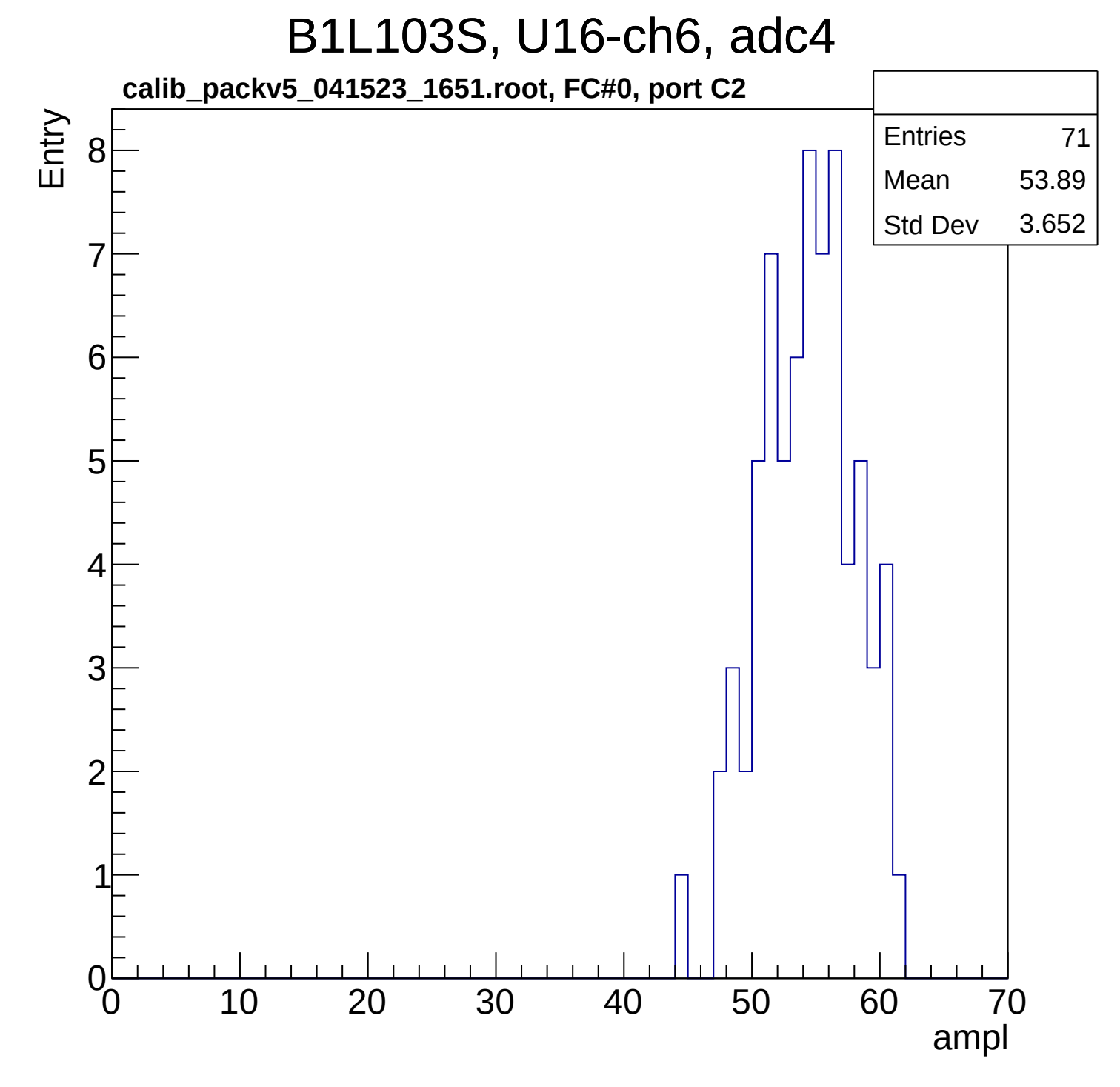
60
70


B1L103S, U16-ch6, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 53.89
Std Dev 3.652
Entry
ampl
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3
4
5
6
7
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0
10
20
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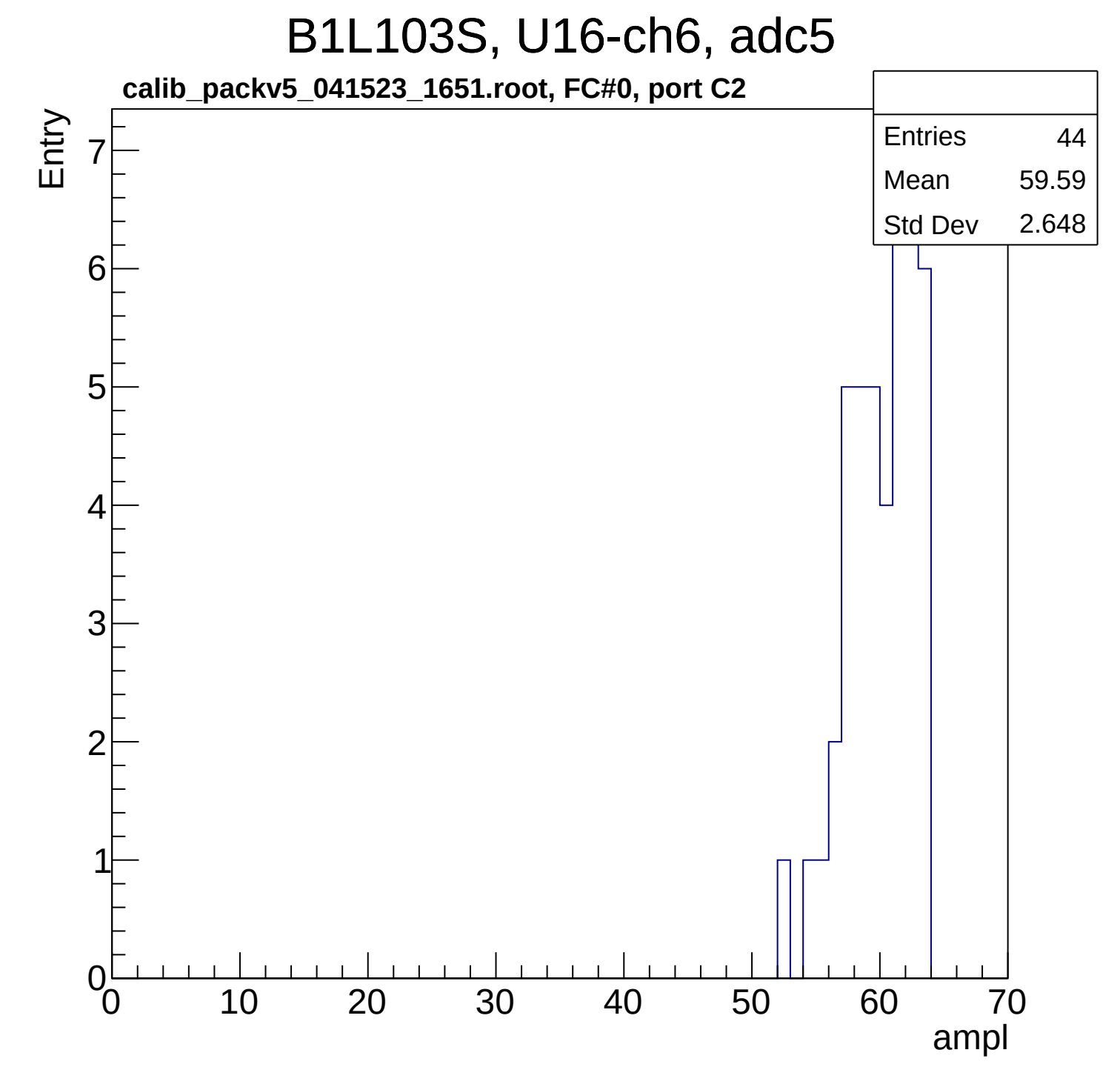
40
50
60
70


B1L103S, U16-ch6, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 59.59
Std Dev 2.648
Entry
ampl
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1
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4
5
6
7
0
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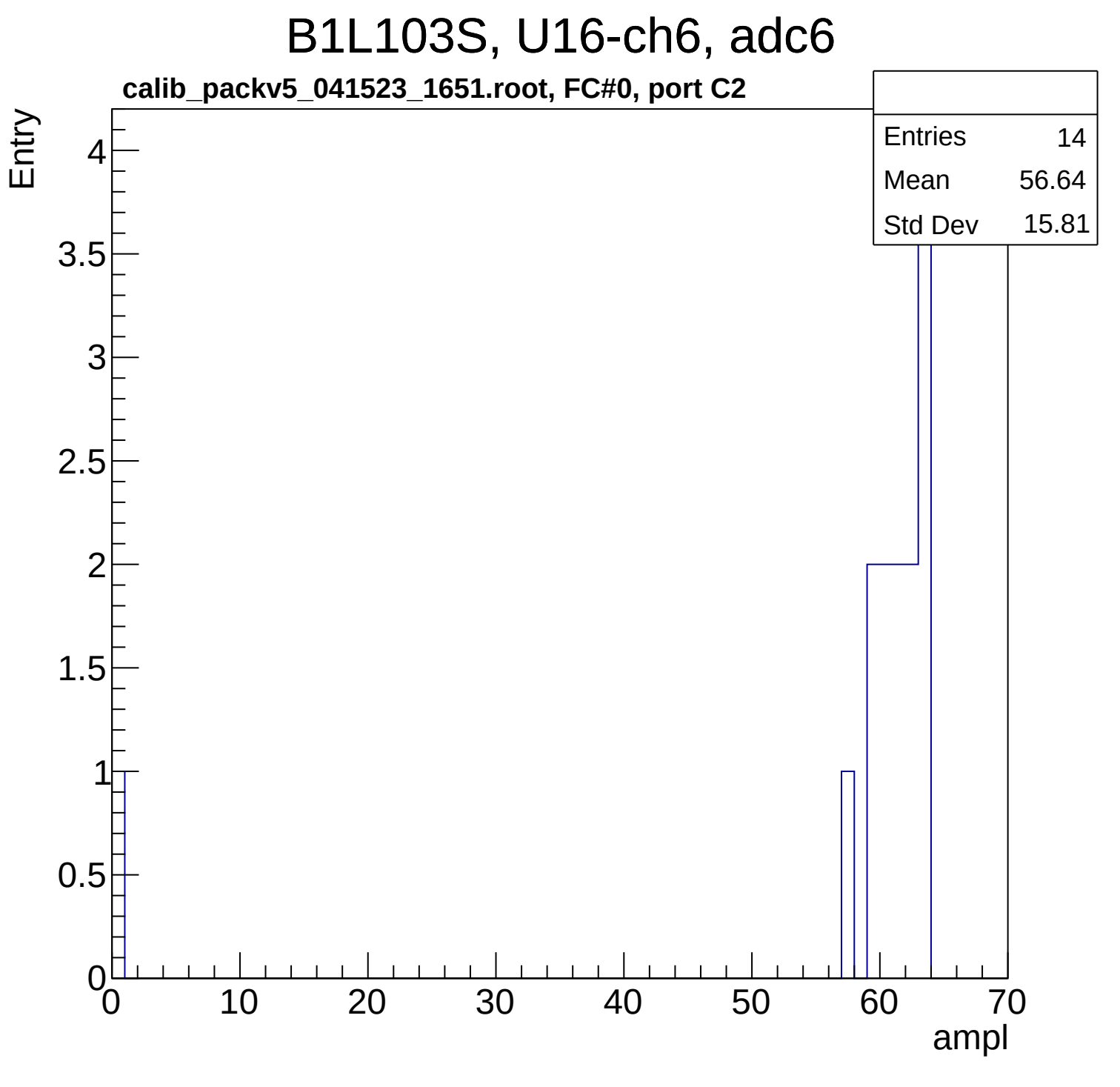
50
60
70


B1L103S, U16-ch6, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 56.64
Std Dev 15.81
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
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20
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40
50
60
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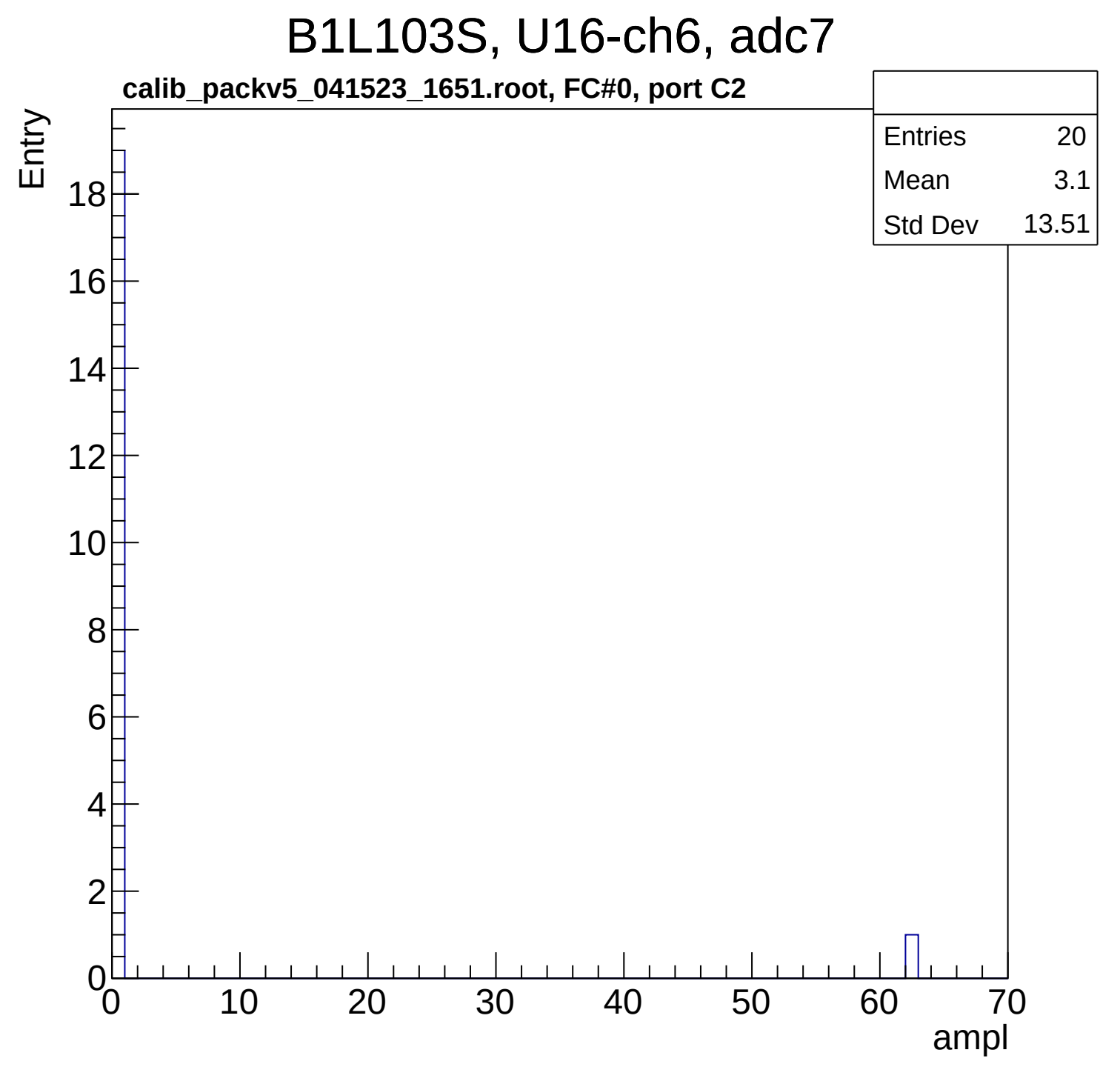
B1L103S, U16-ch6, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
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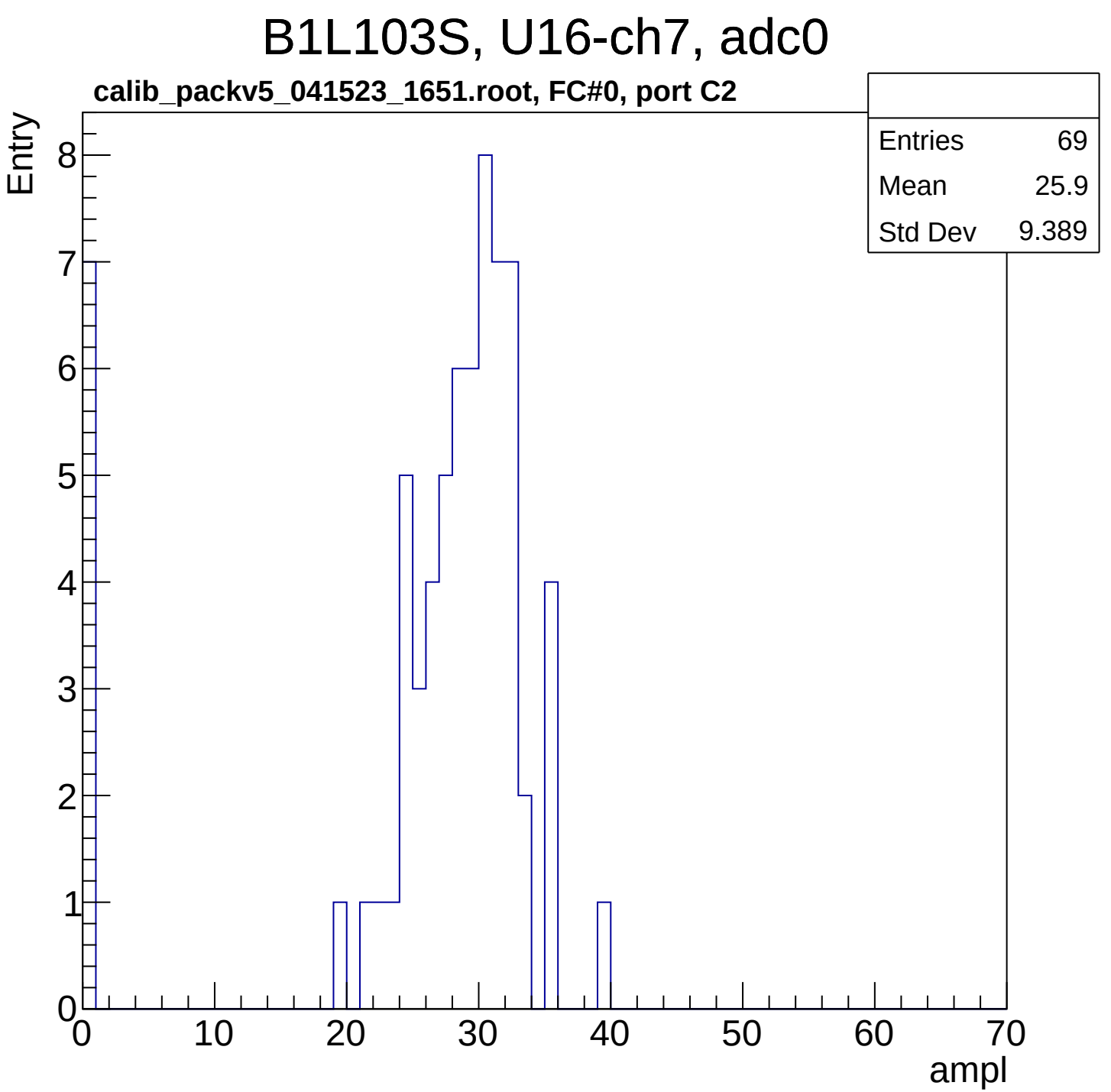
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch7, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 25.9
Std Dev 9.389
Entry
ampl
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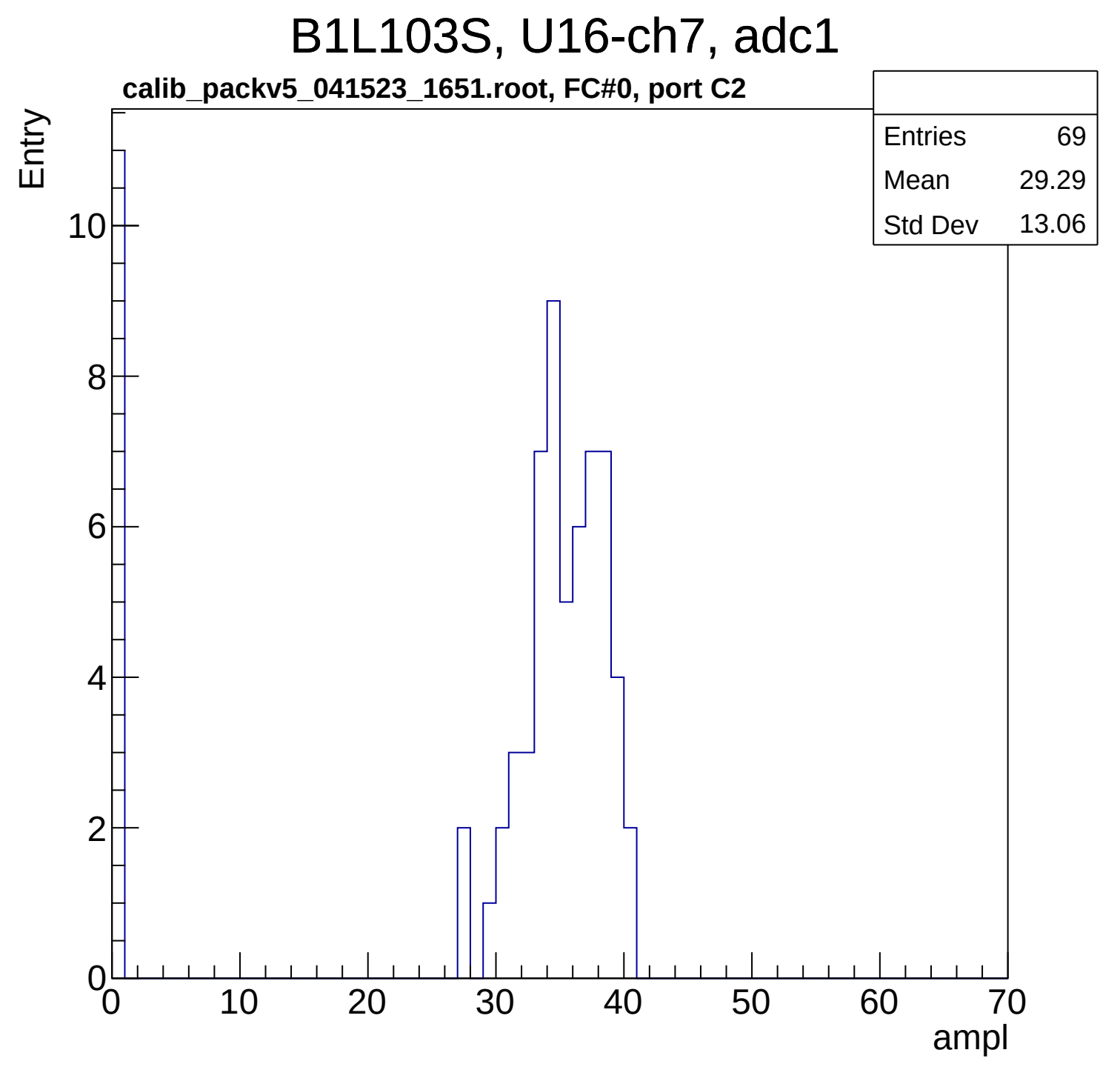
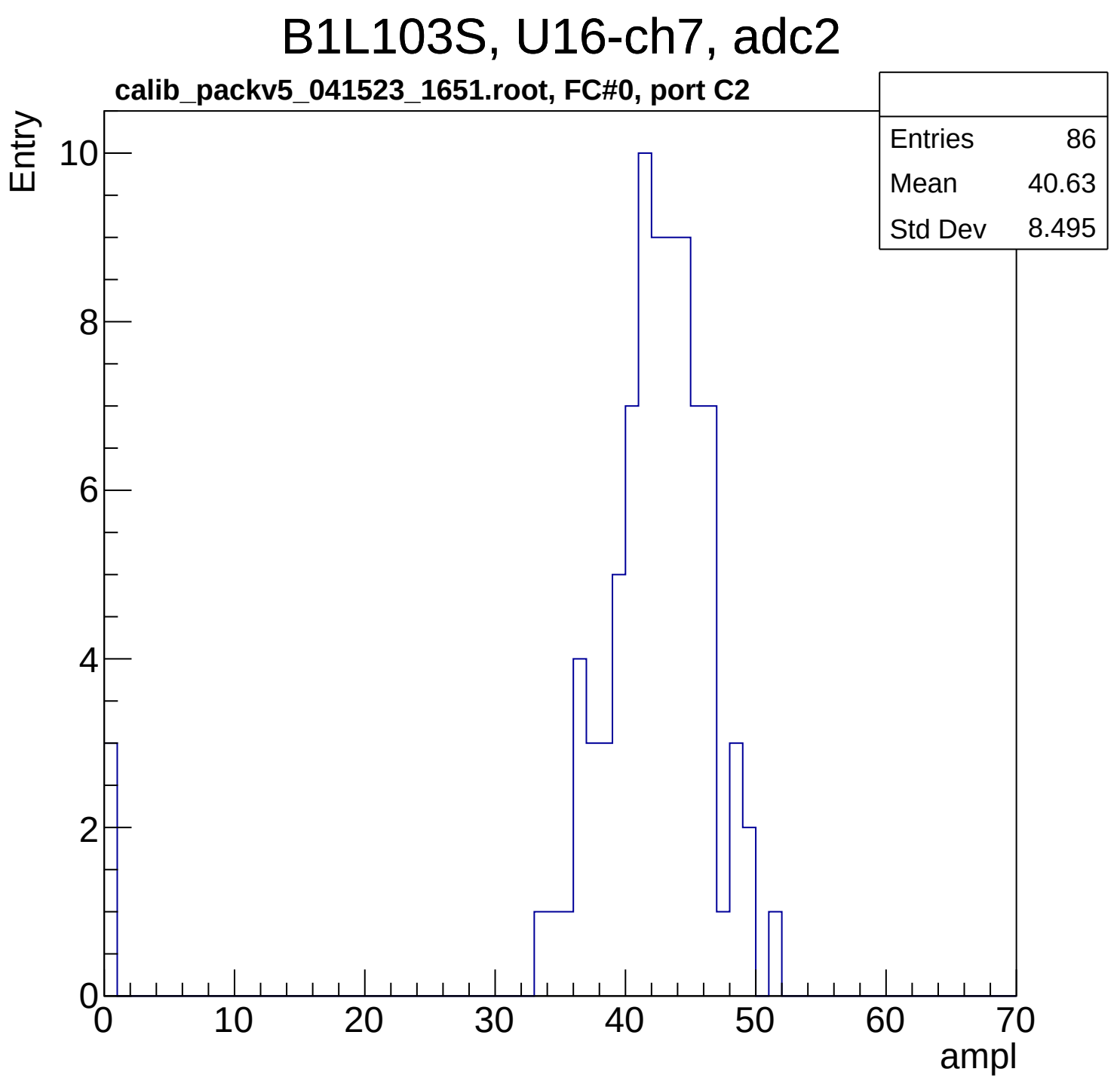
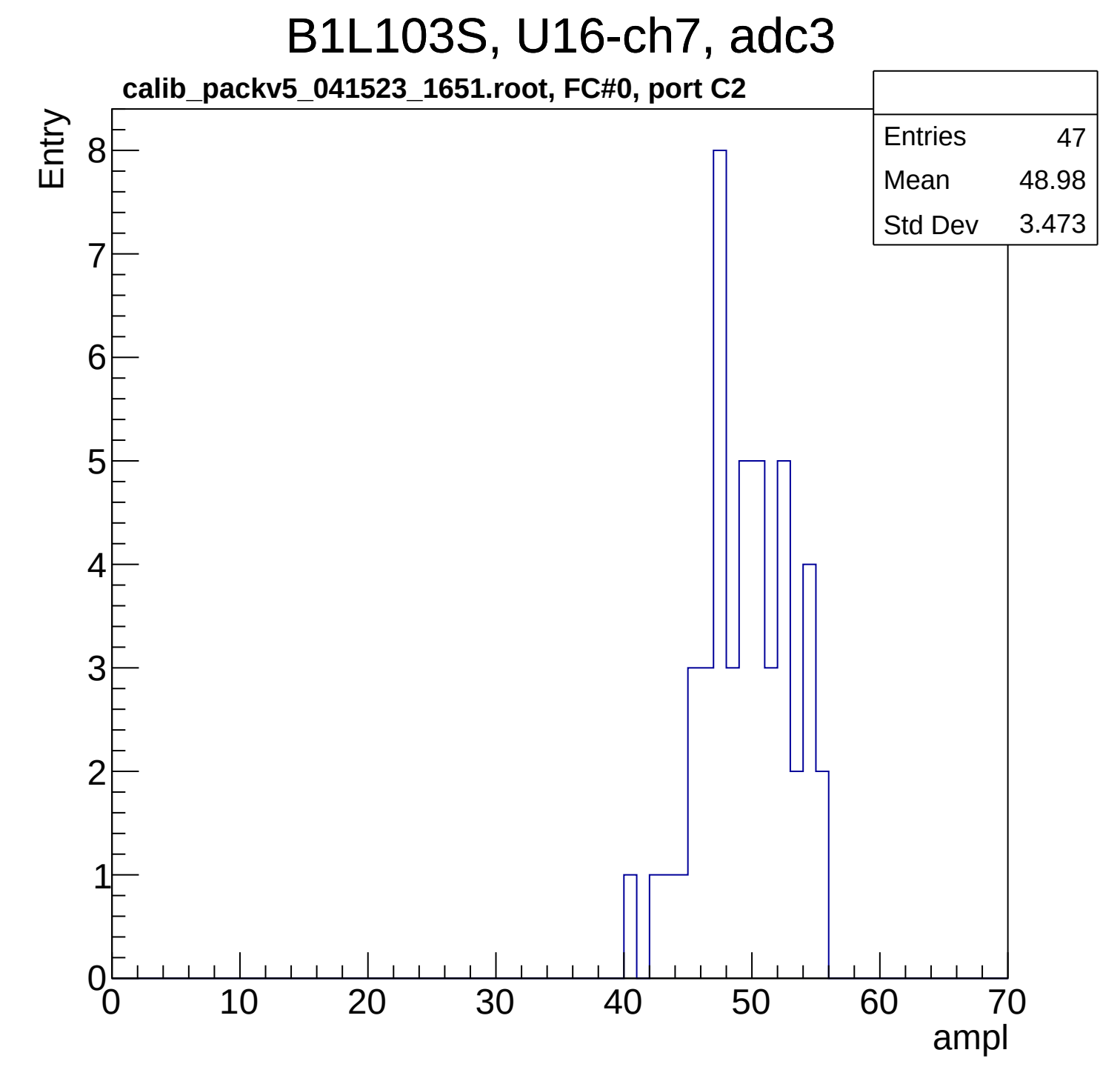
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch7, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 29.29
Std Dev 13.06
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch7, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 40.63
Std Dev 8.495
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch7, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 48.98
Std Dev 3.473
Entry
ampl
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5
6
7
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20
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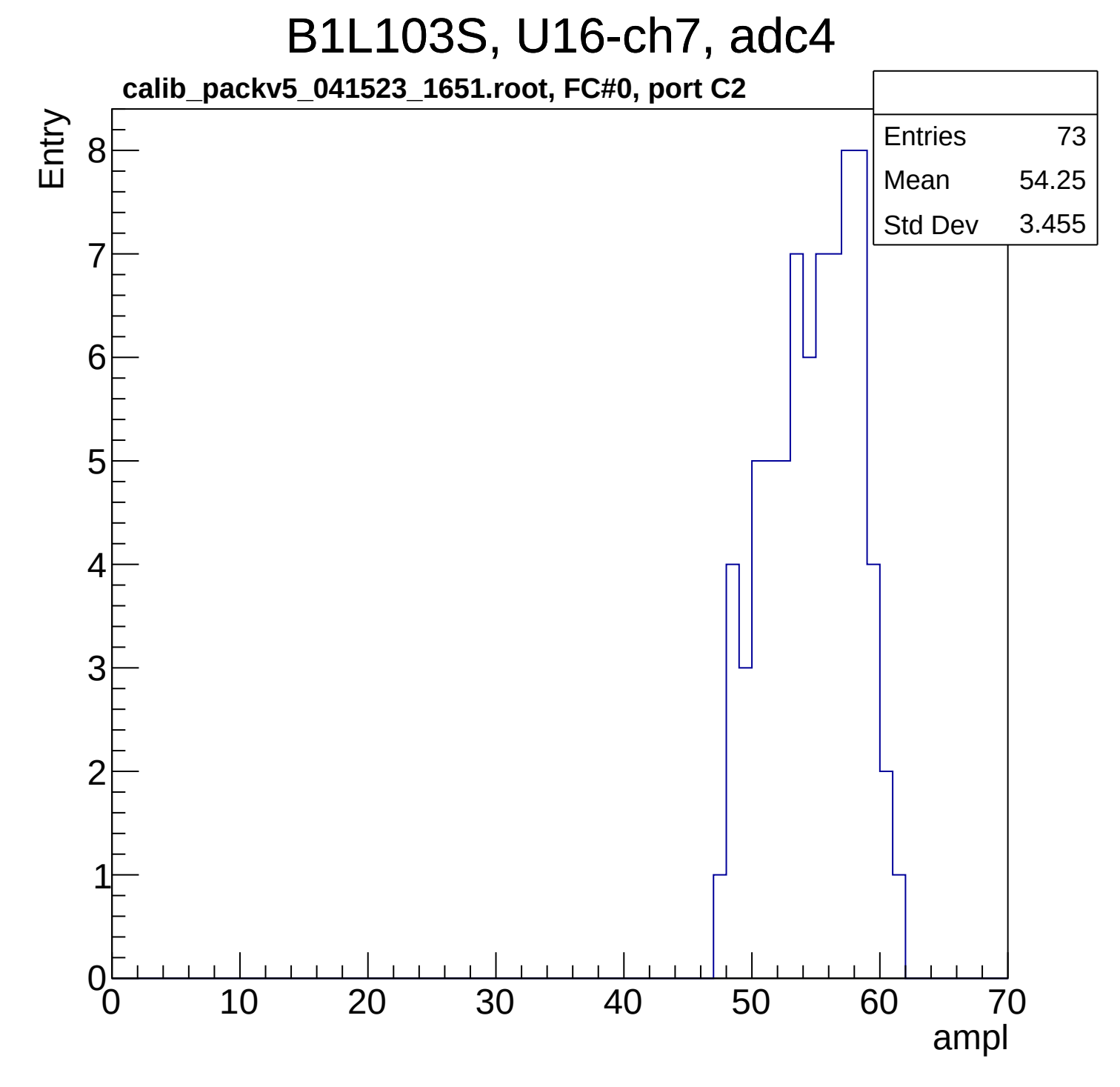
40
50
60
70


B1L103S, U16-ch7, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 54.25
Std Dev 3.455
Entry
ampl
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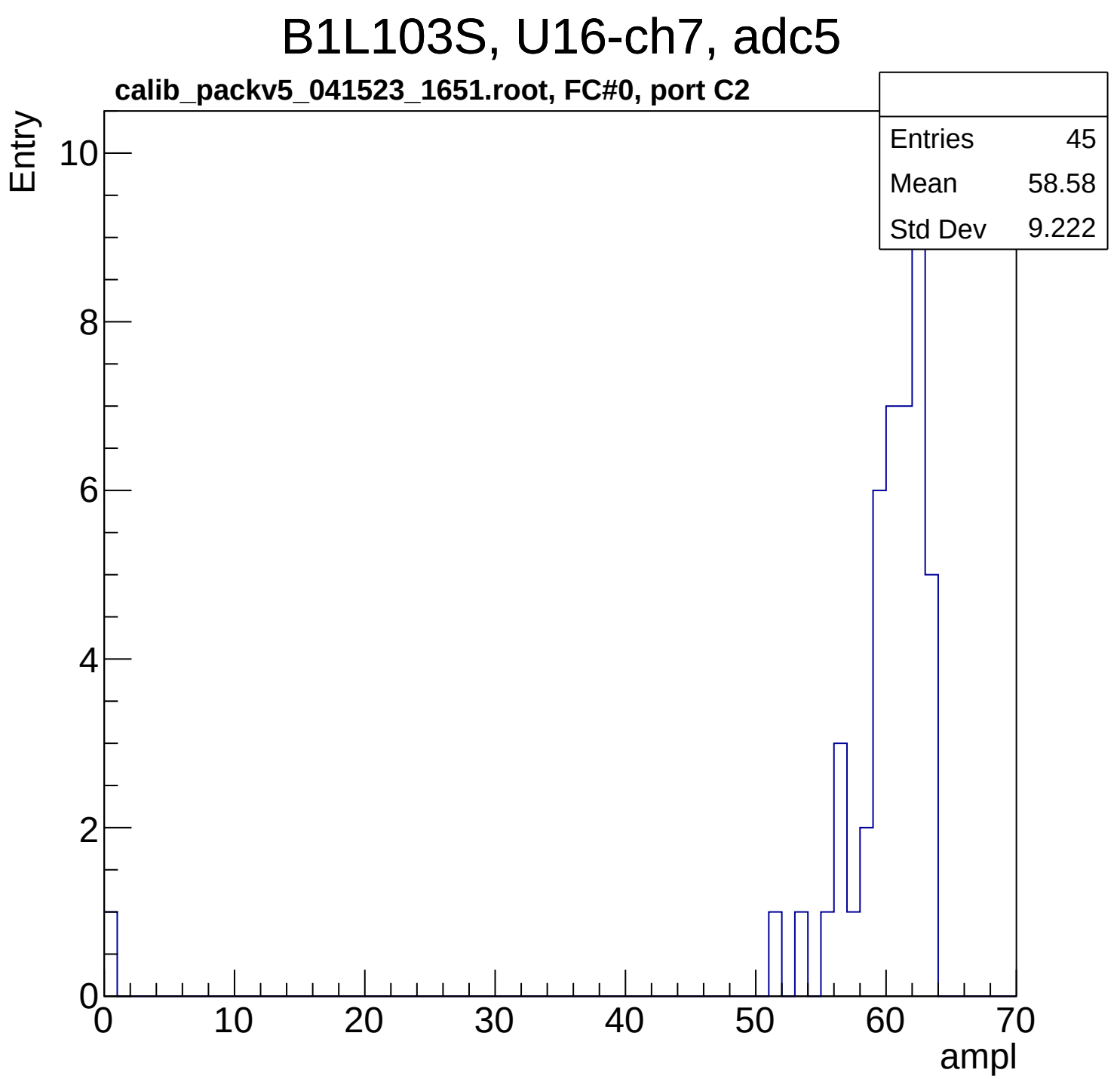
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch7, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.58
Std Dev 9.222
Entry
ampl
0
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4
6
8
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0
10
20
30
40
50
60
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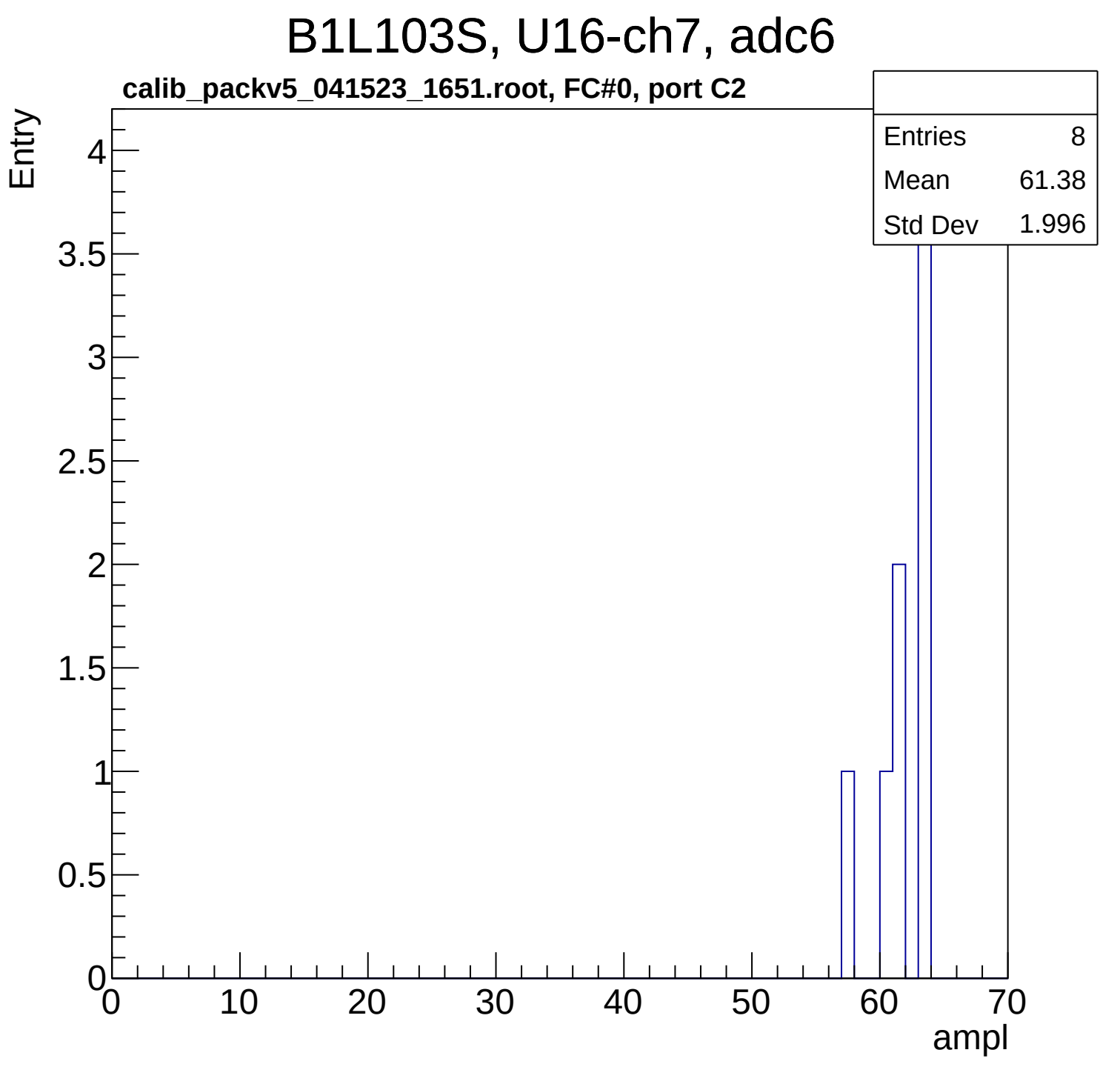
B1L103S, U16-ch7, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.38
Std Dev 1.996
Entry
ampl
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0.5
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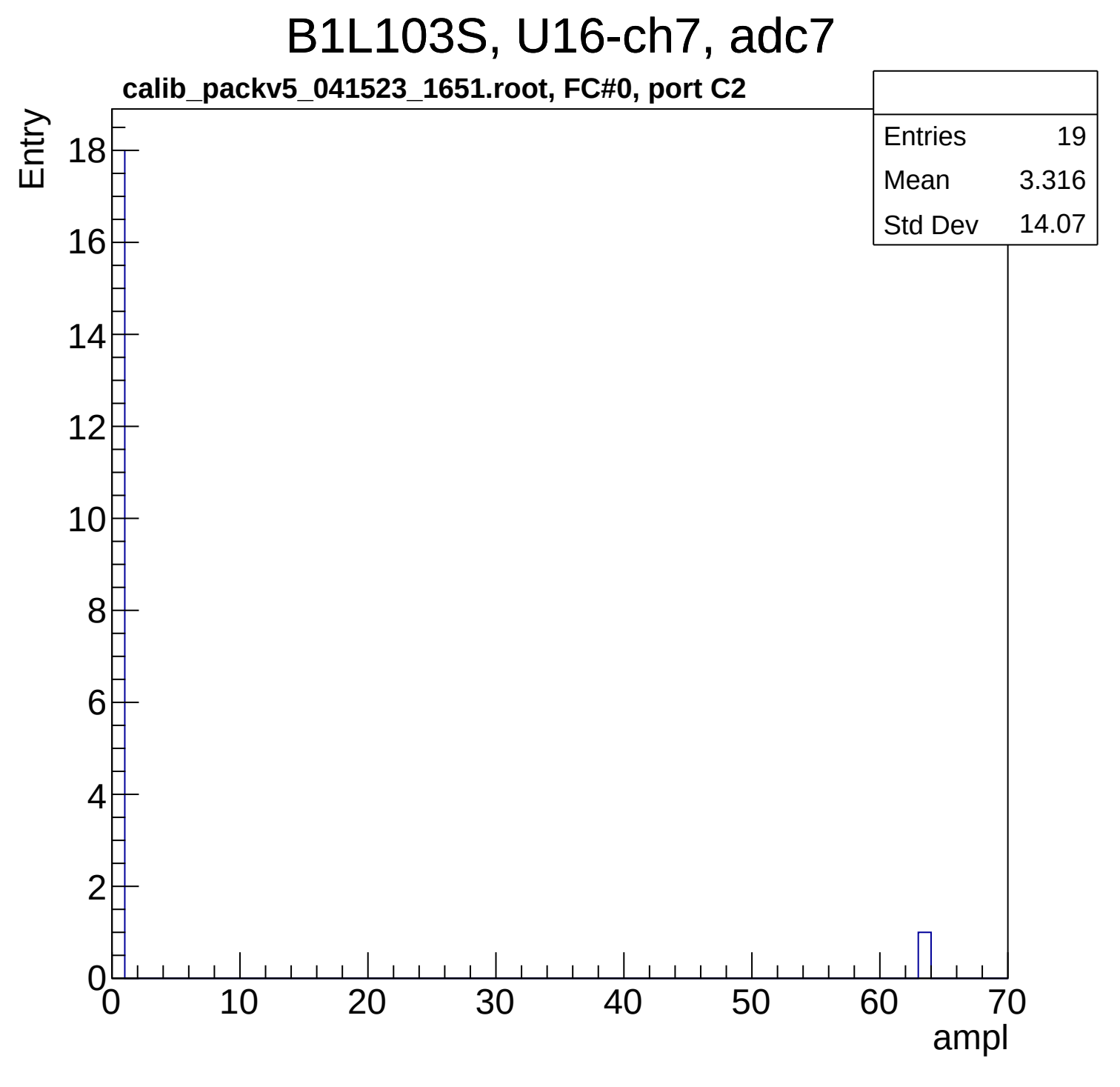
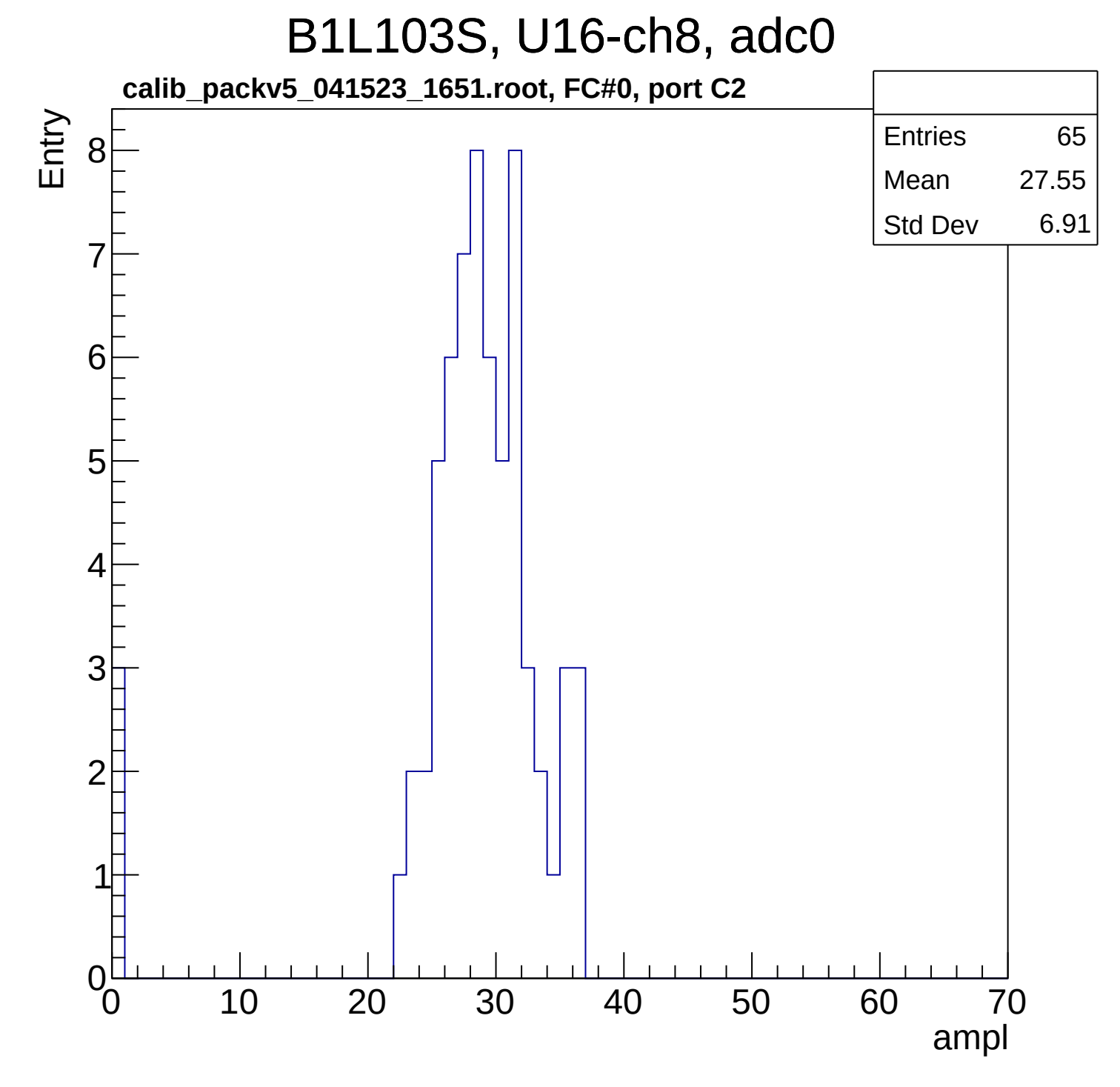
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U16-ch7, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch8, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 27.55
Std Dev 6.91
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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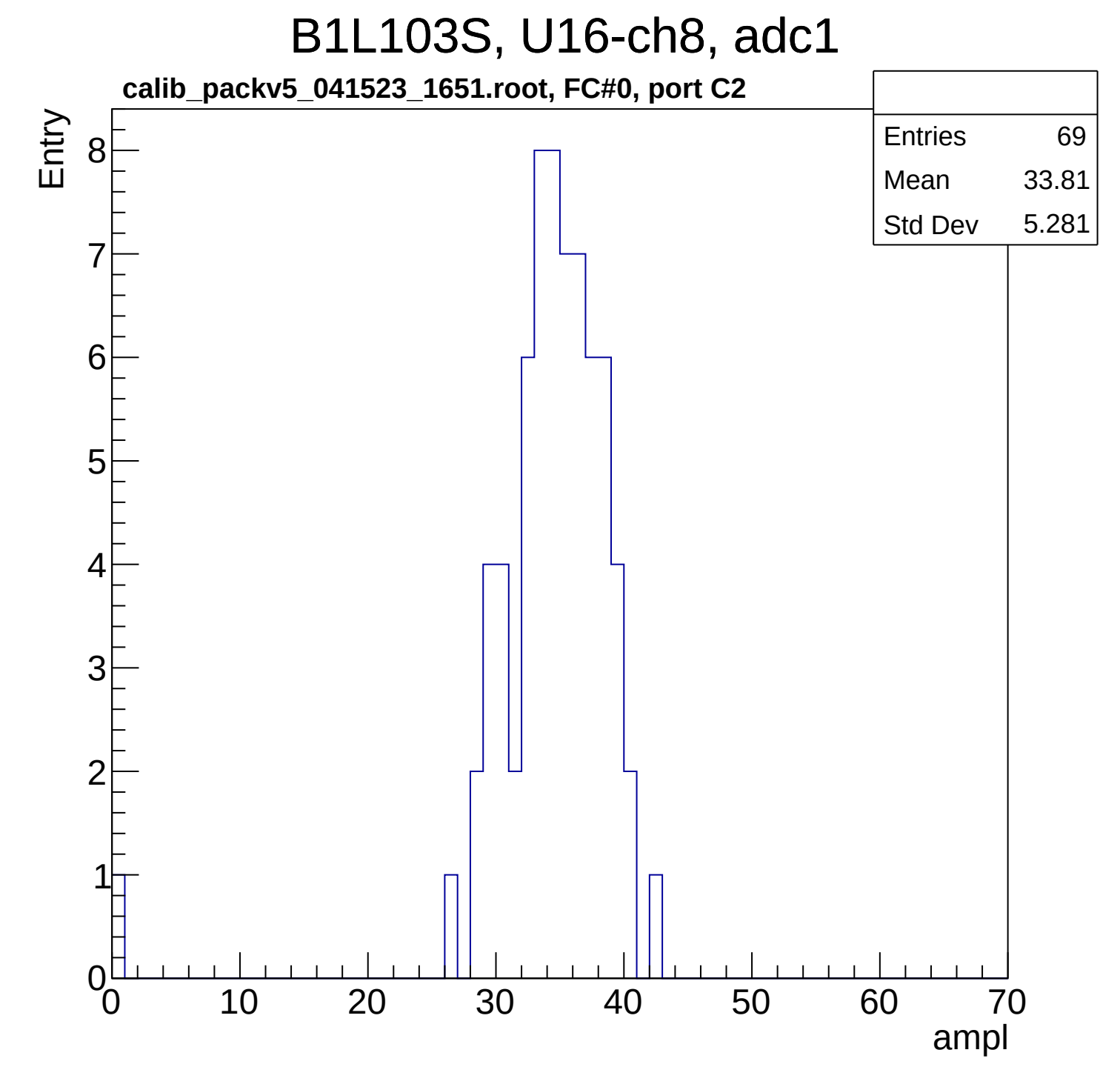
B1L103S, U16-ch8, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 33.81
Std Dev 5.281
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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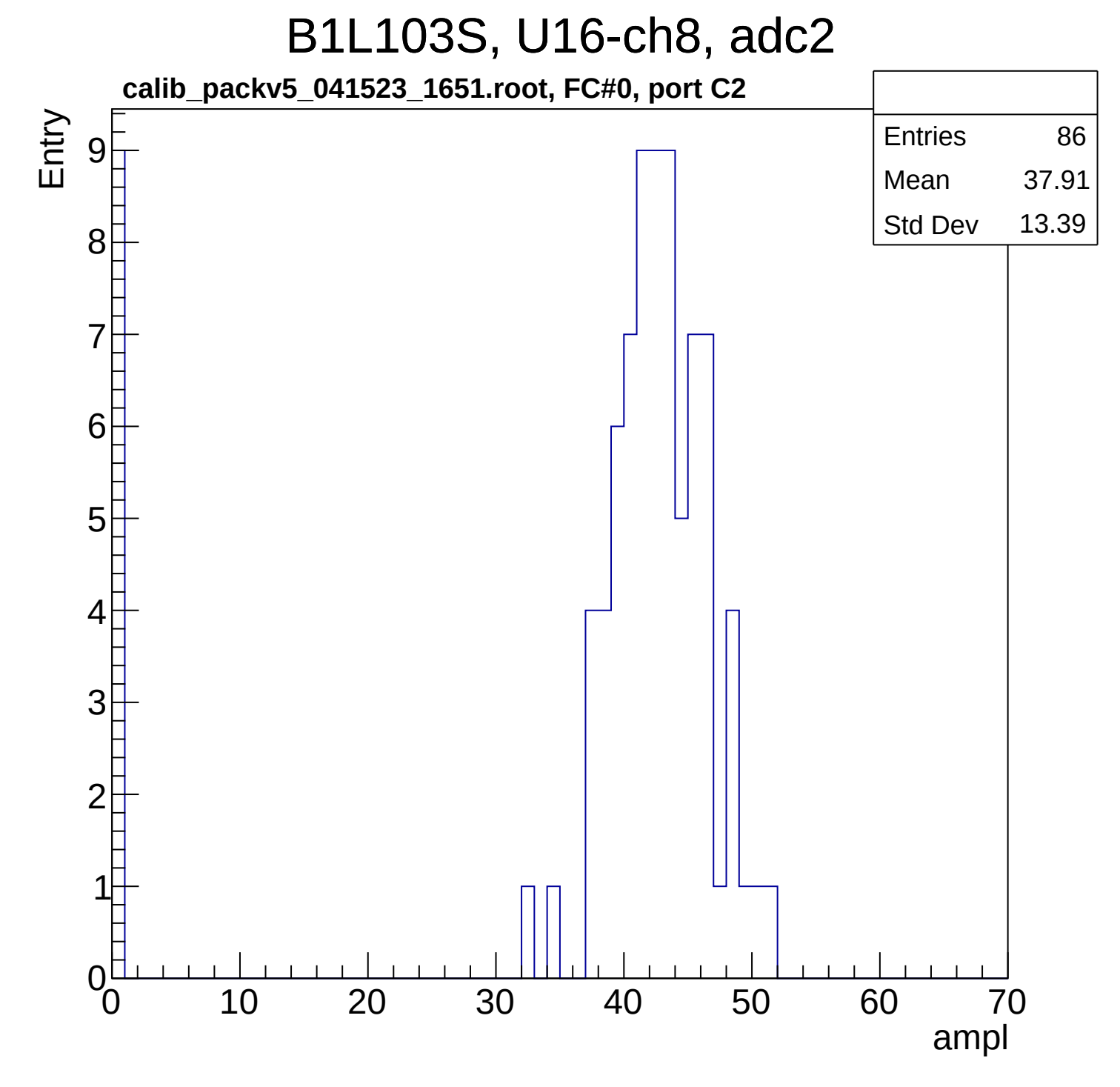
40
50
60
70


B1L103S, U16-ch8, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 37.91
Std Dev 13.39
Entry
ampl
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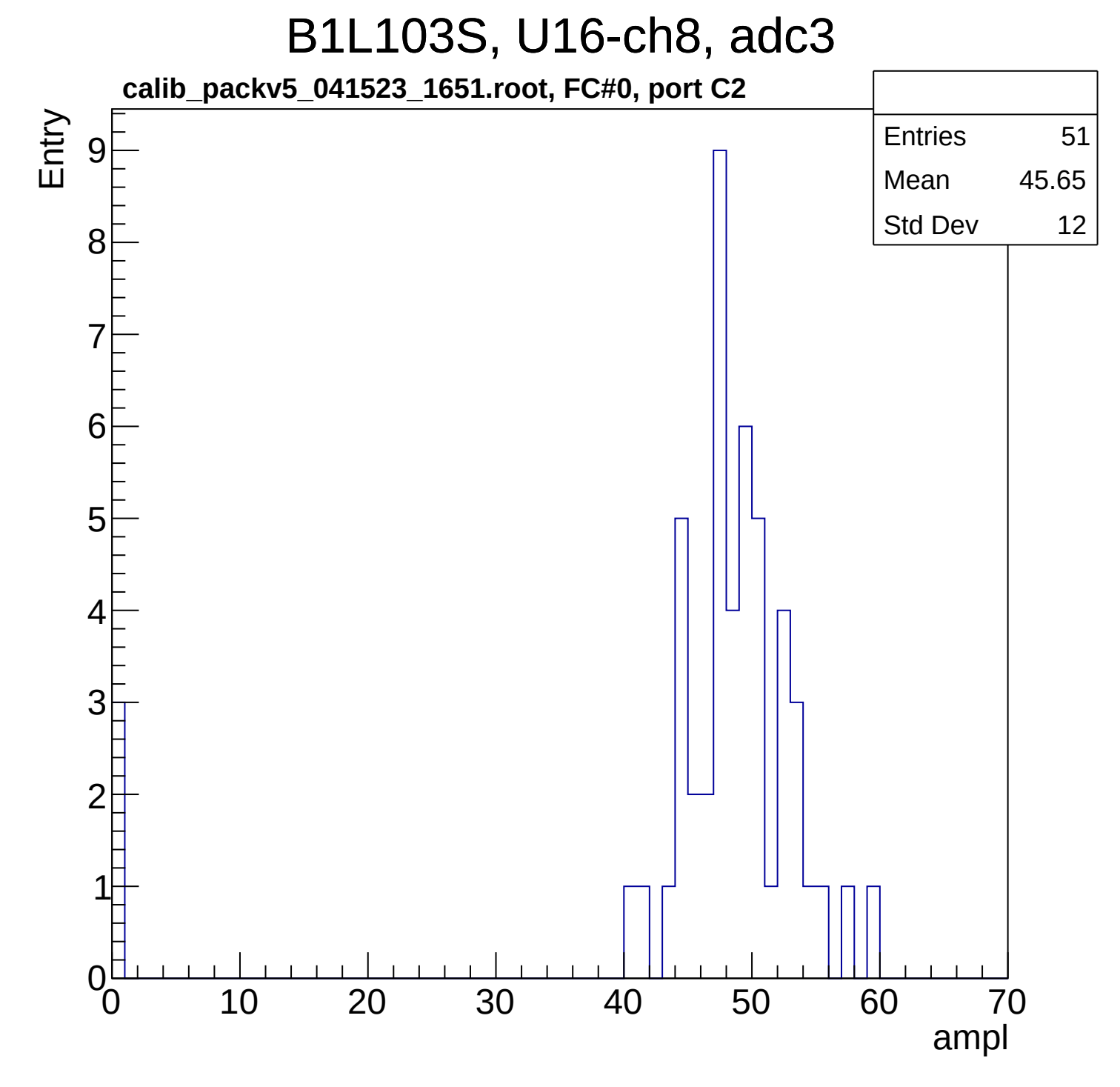
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch8, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 45.65
Std Dev 12
Entry
ampl
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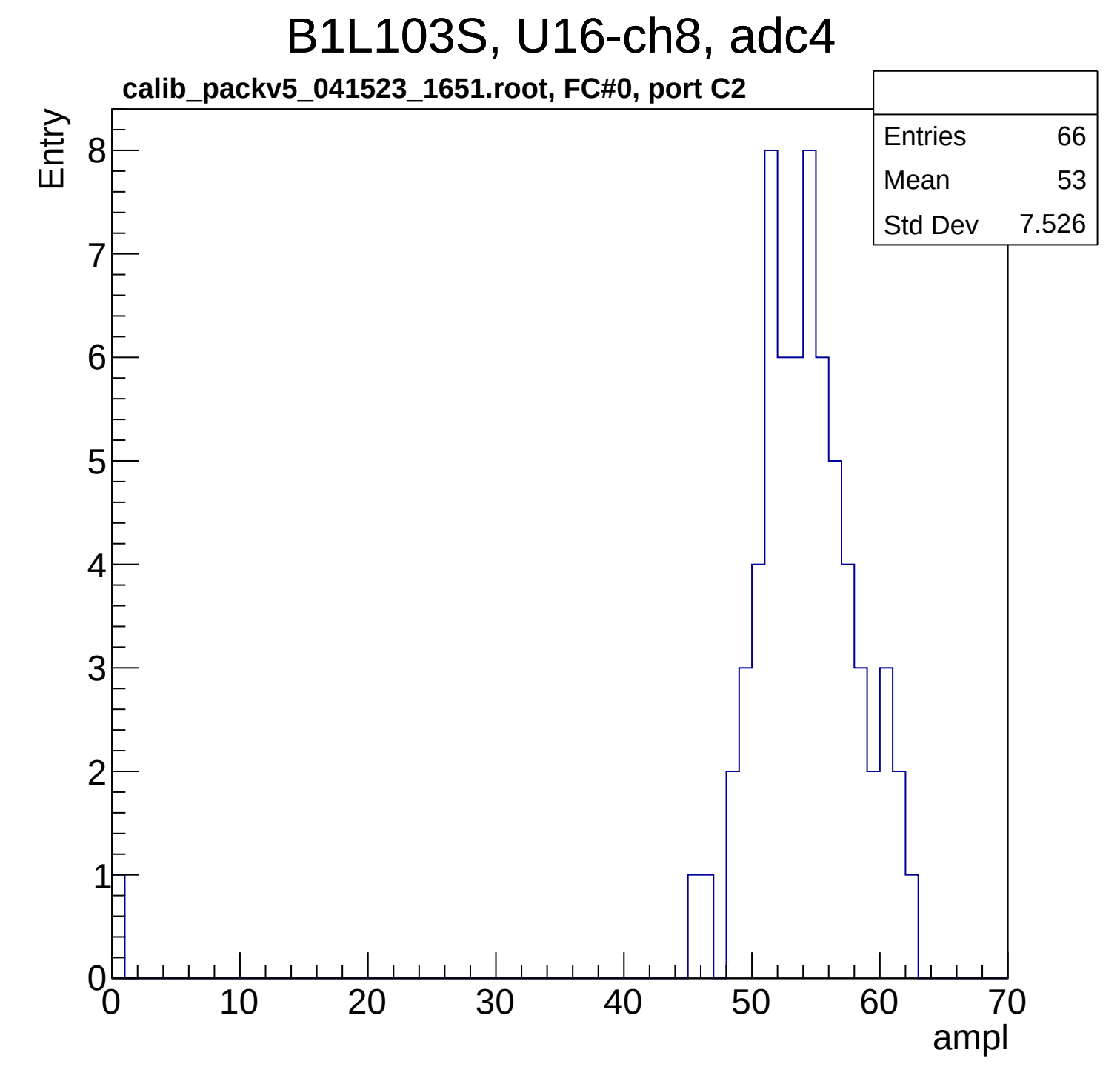
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U16-ch8, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 53
Std Dev 7.526
Entry
ampl
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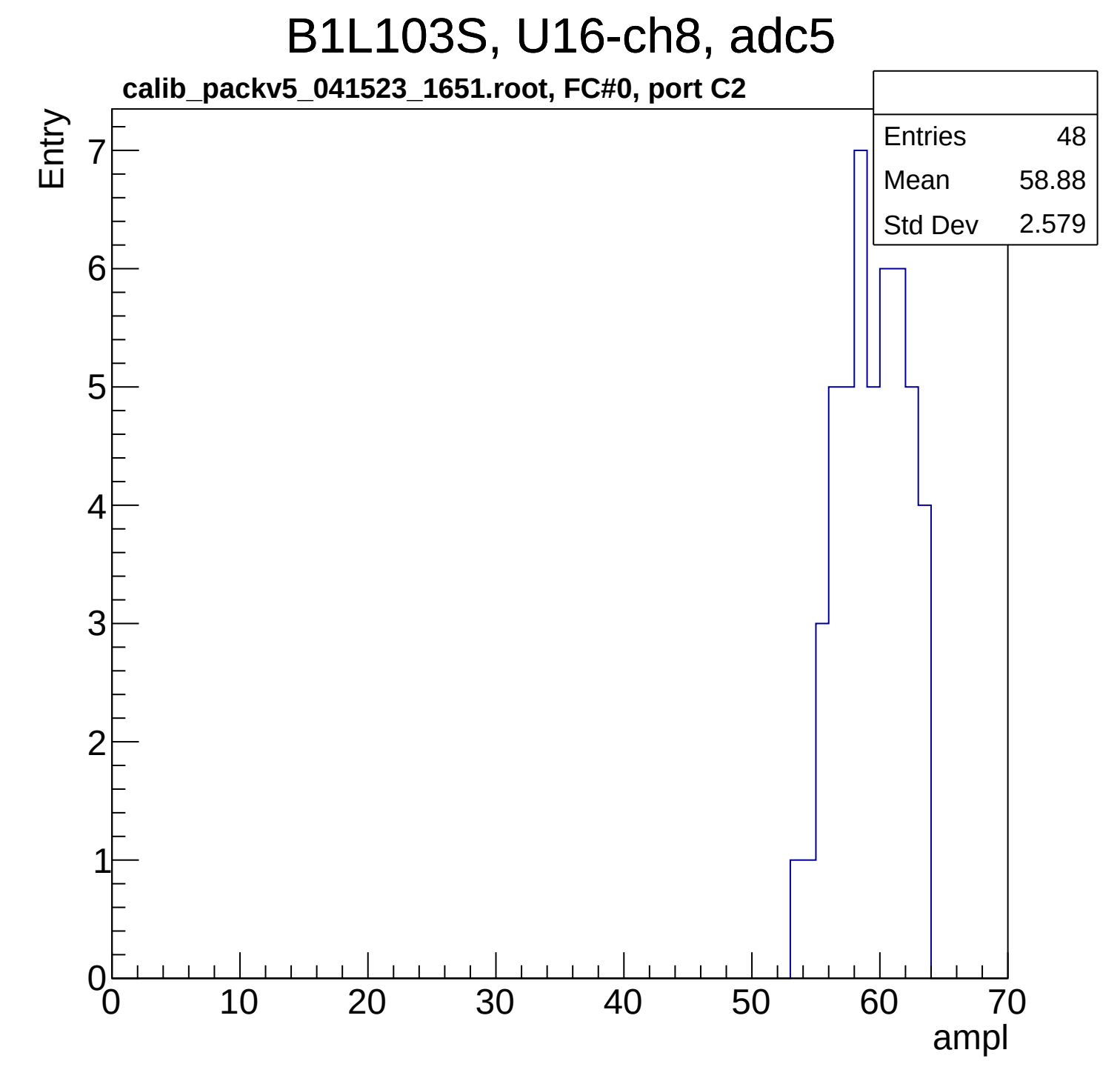
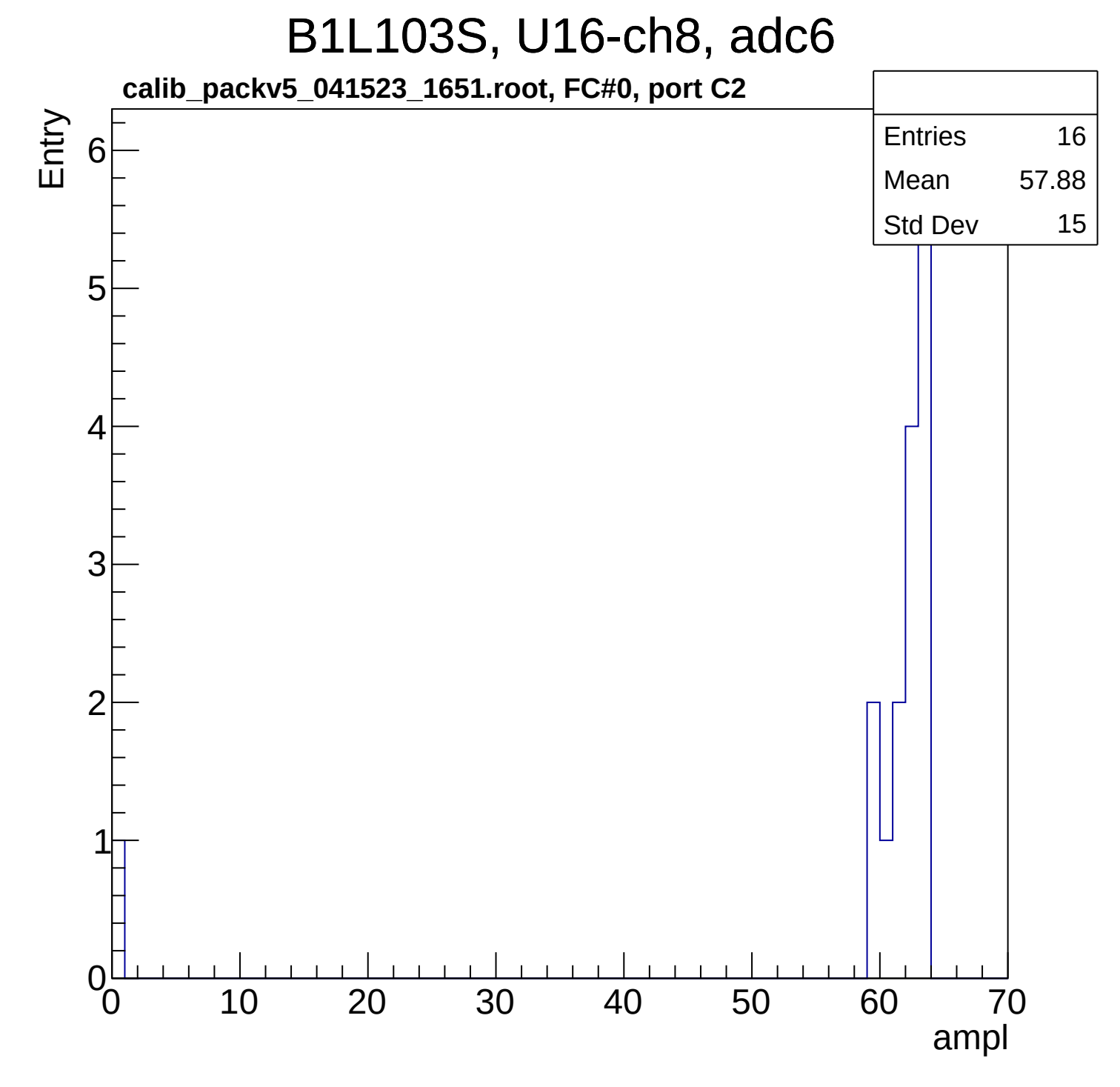
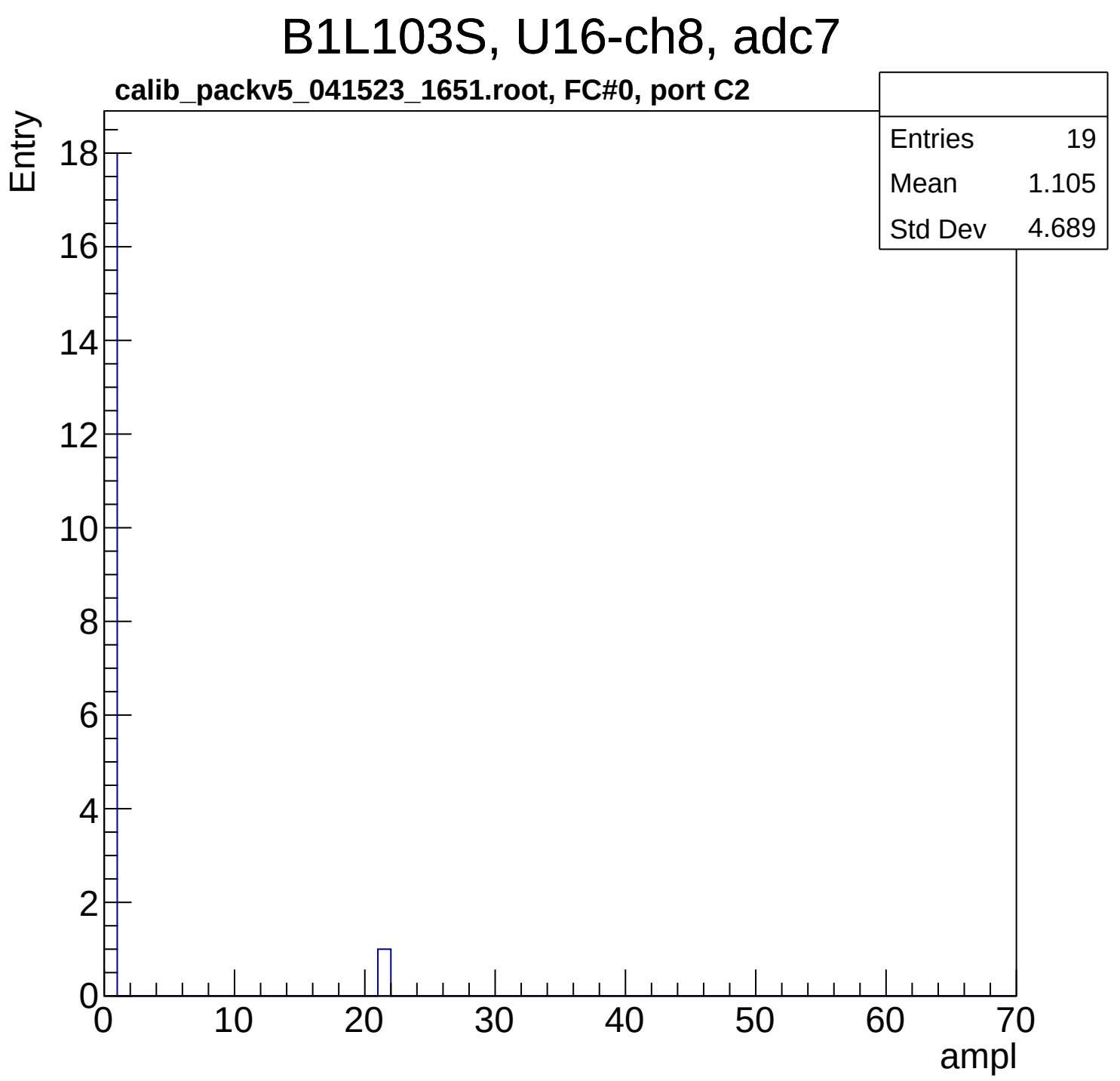
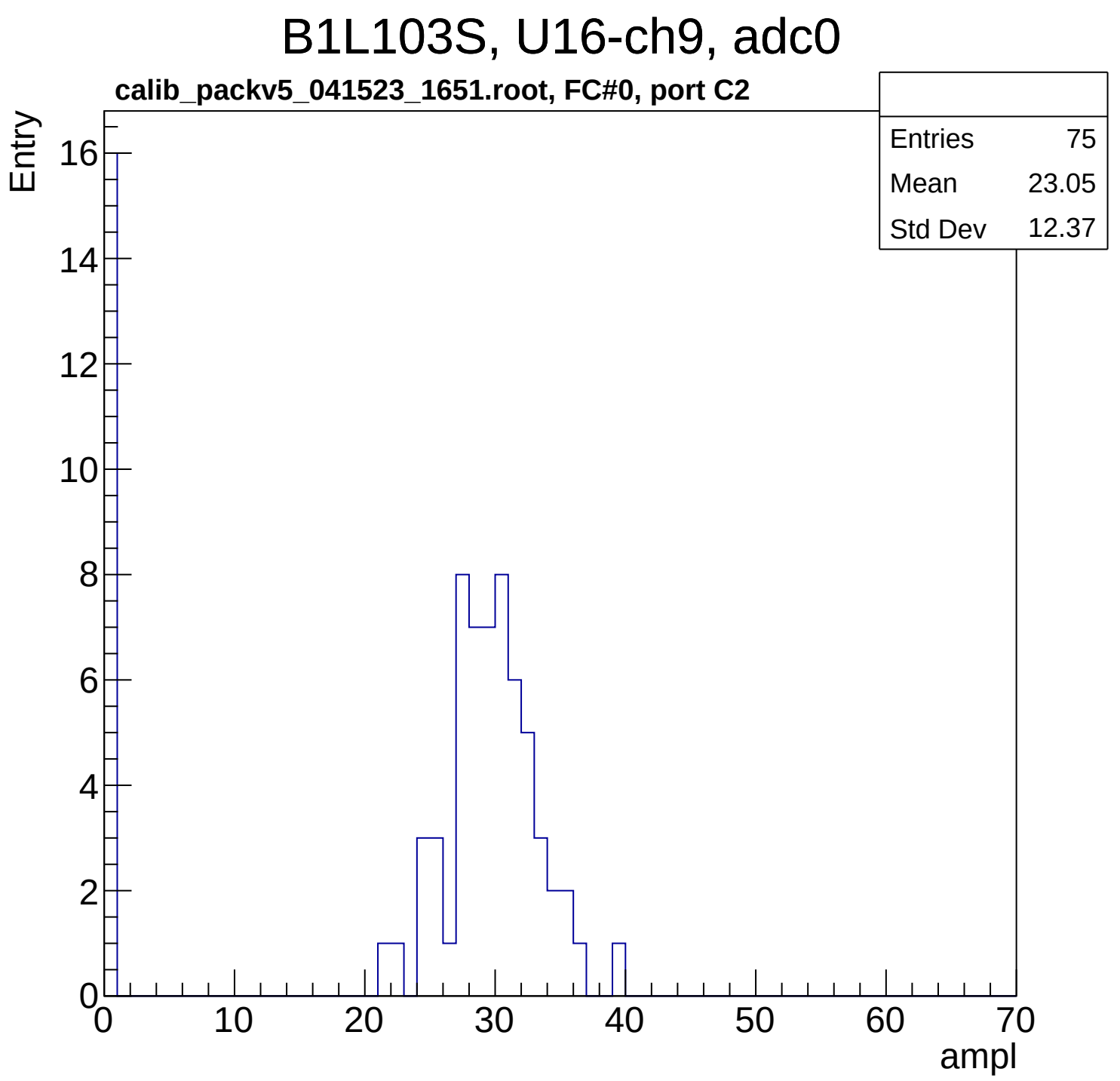
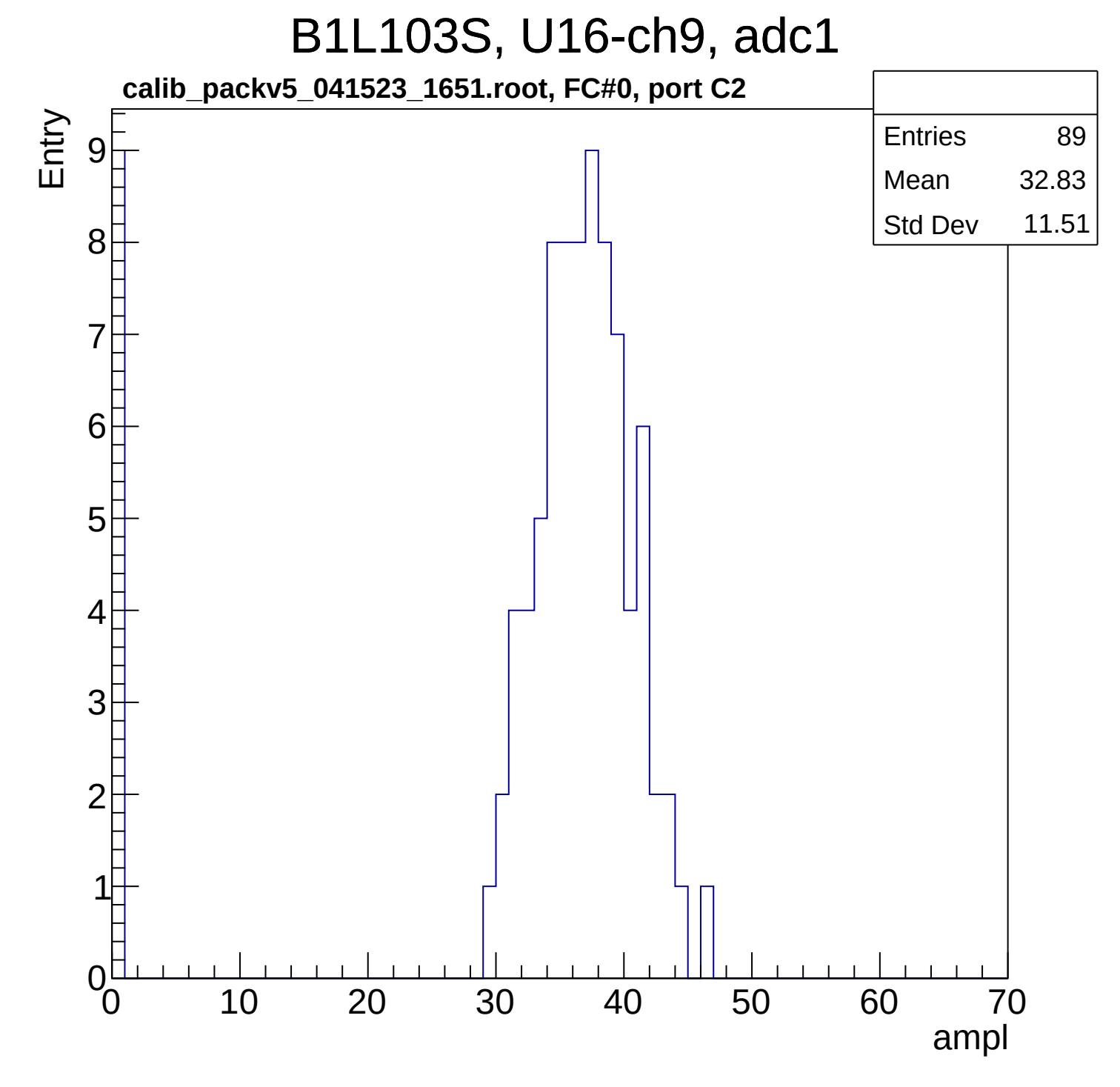
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

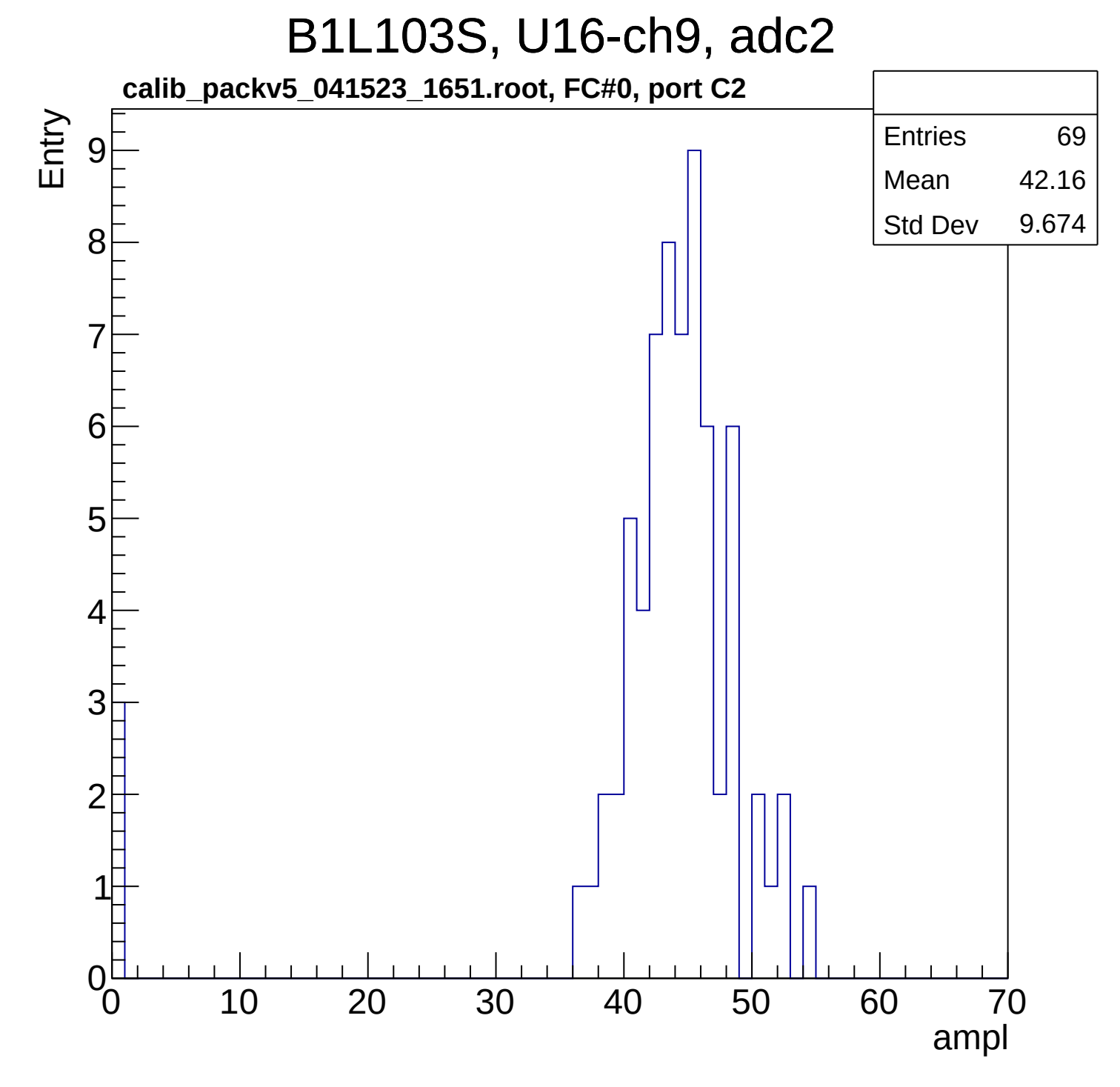

B1L103S, U16-ch8, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.88
Std Dev 2.579
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch8, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.88
Std Dev 15
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U16-ch8, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch9, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 23.05
Std Dev 12.37
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U16-ch9, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 32.83
Std Dev 11.51
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch9, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 42.16
Std Dev 9.674
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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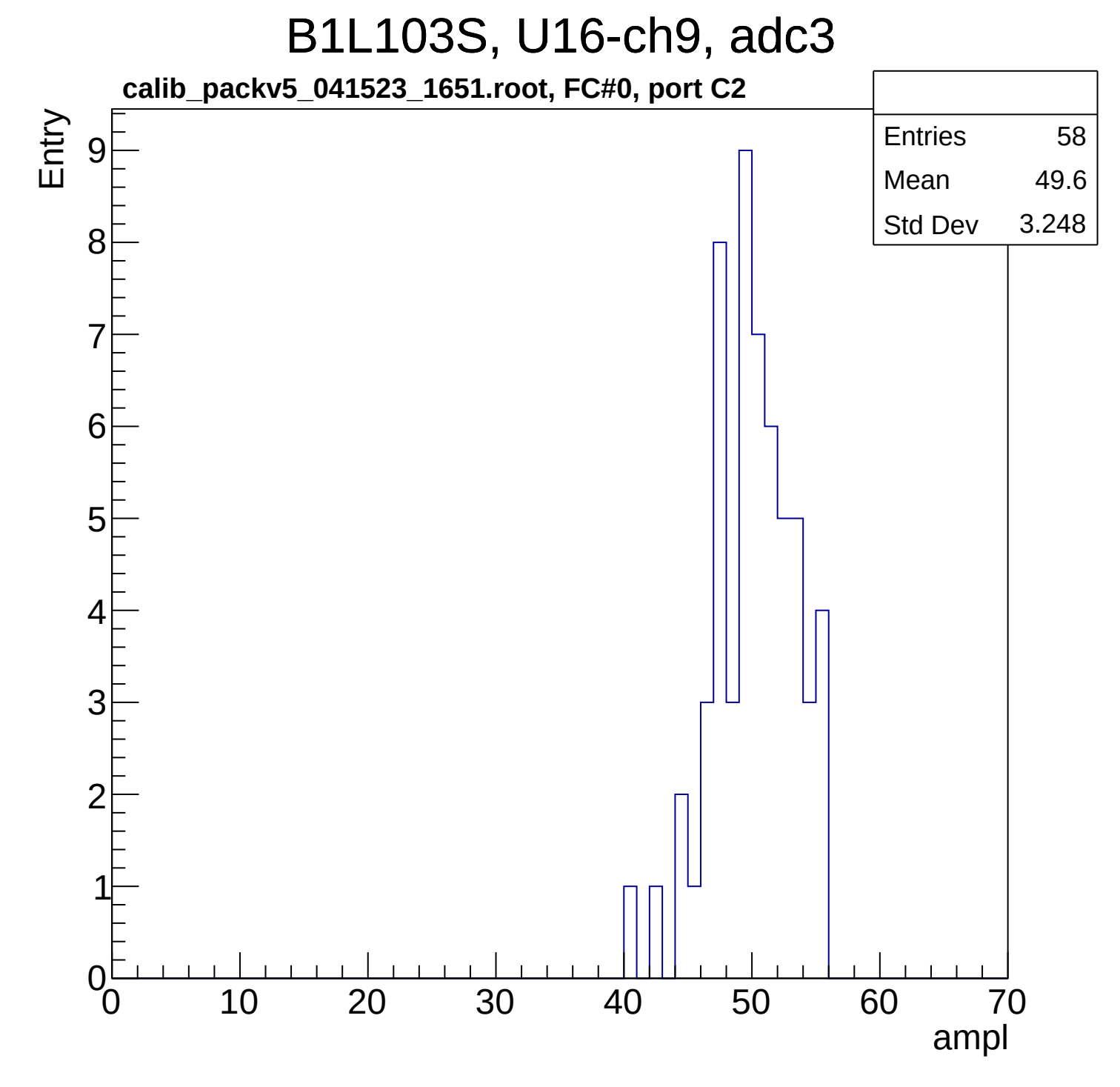
B1L103S, U16-ch9, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 49.6
Std Dev 3.248
Entry
ampl
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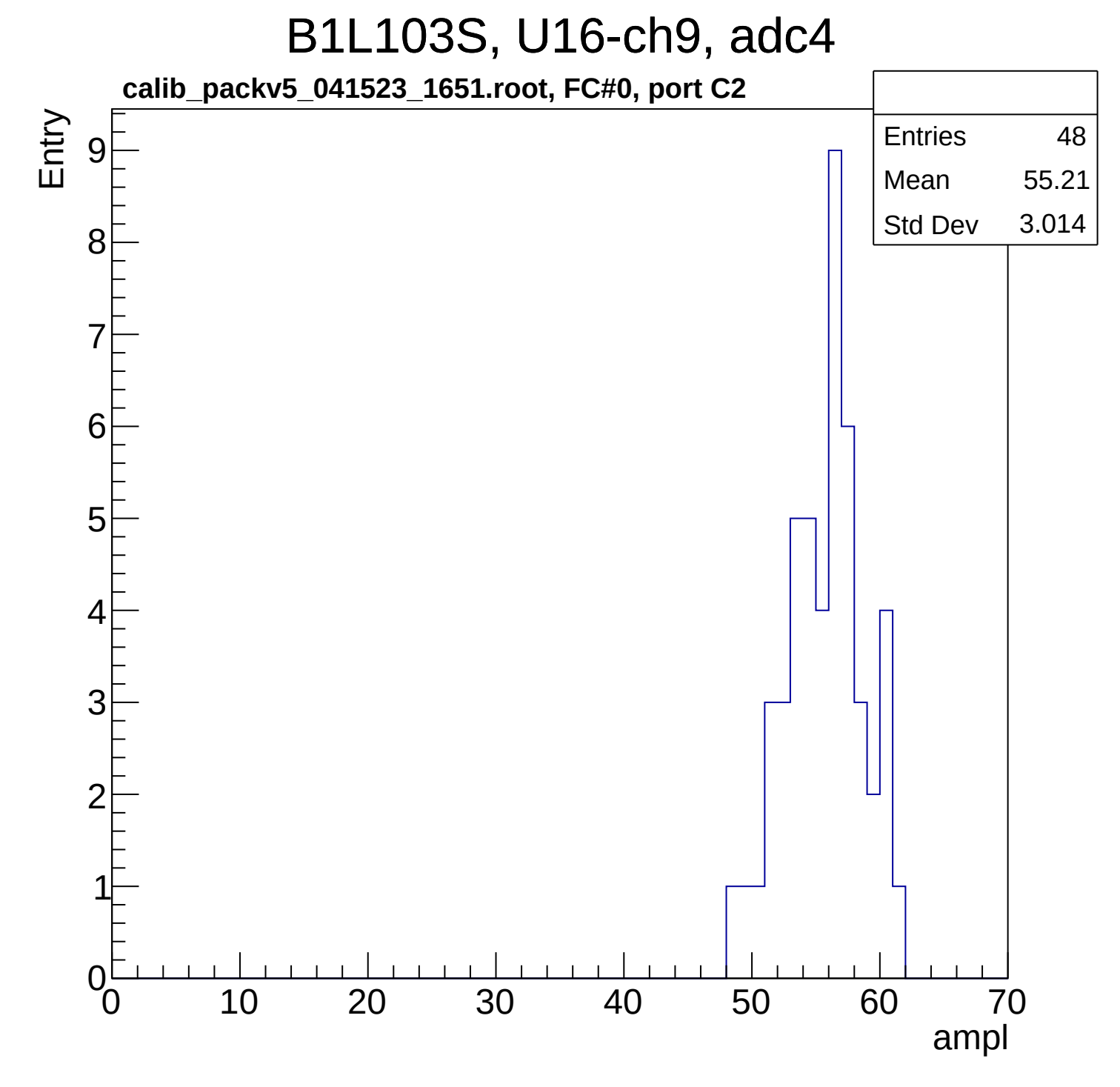
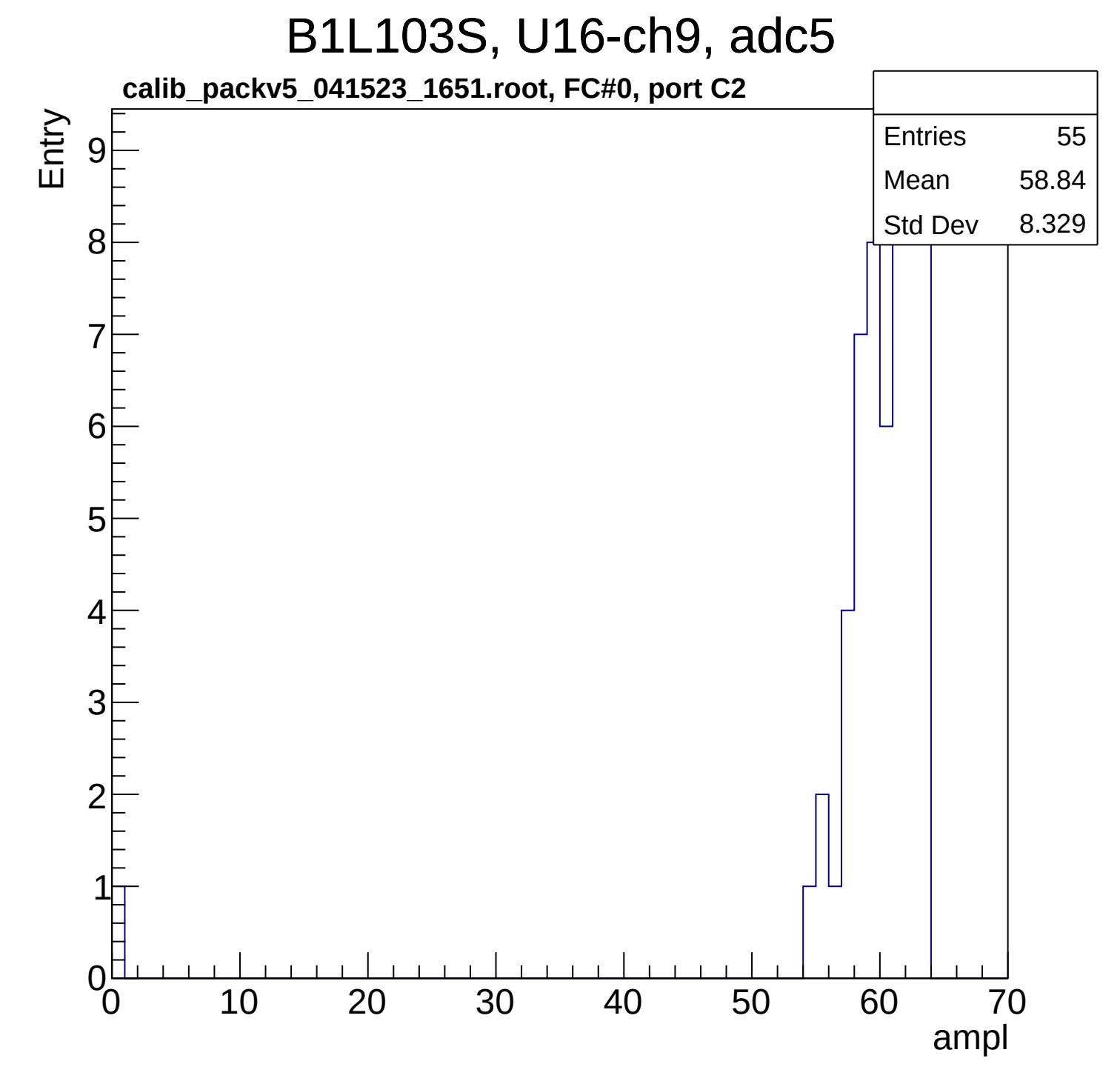
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch9, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 55.21
Std Dev 3.014
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch9, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.84
Std Dev 8.329
Entry
ampl
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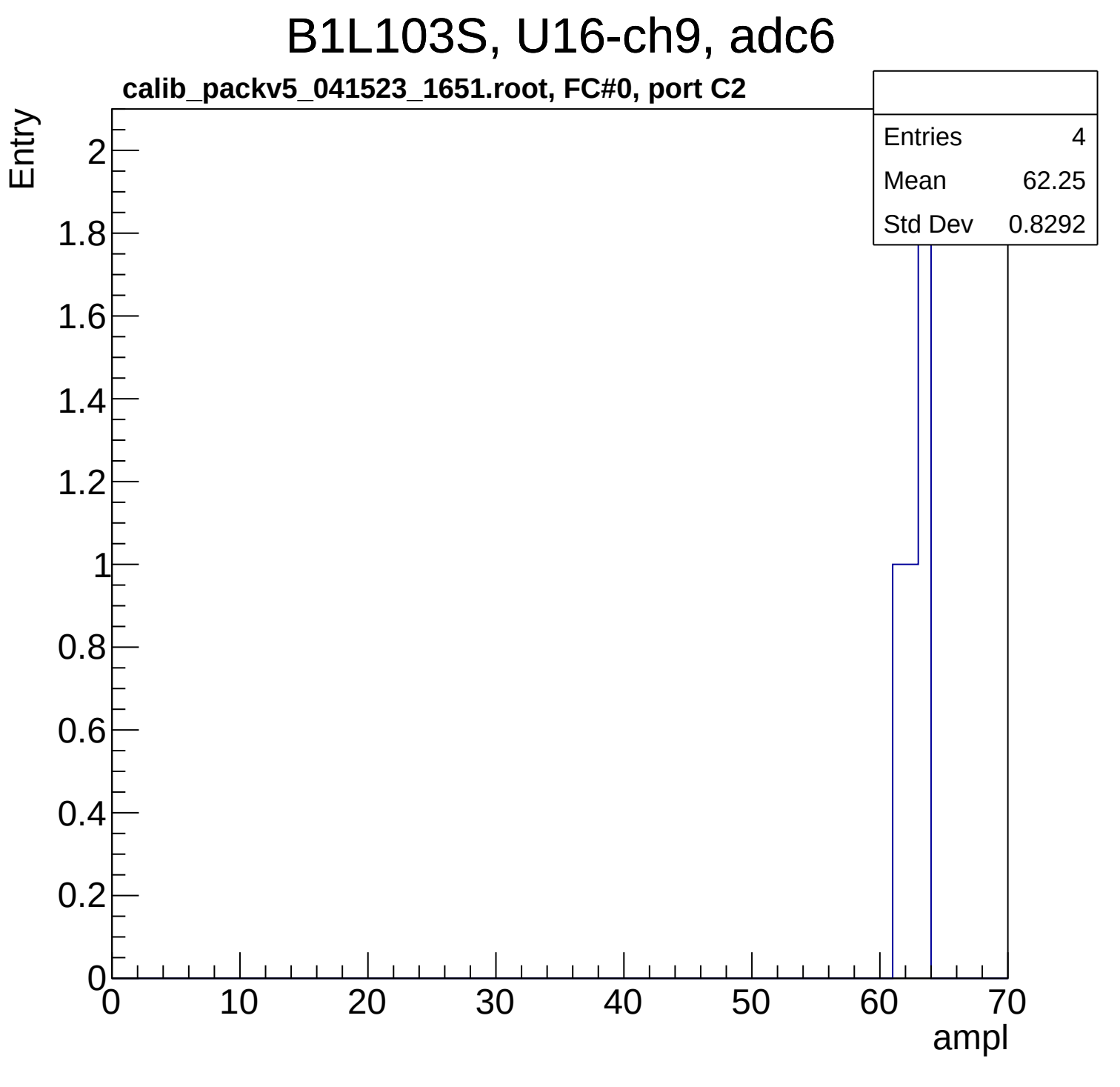
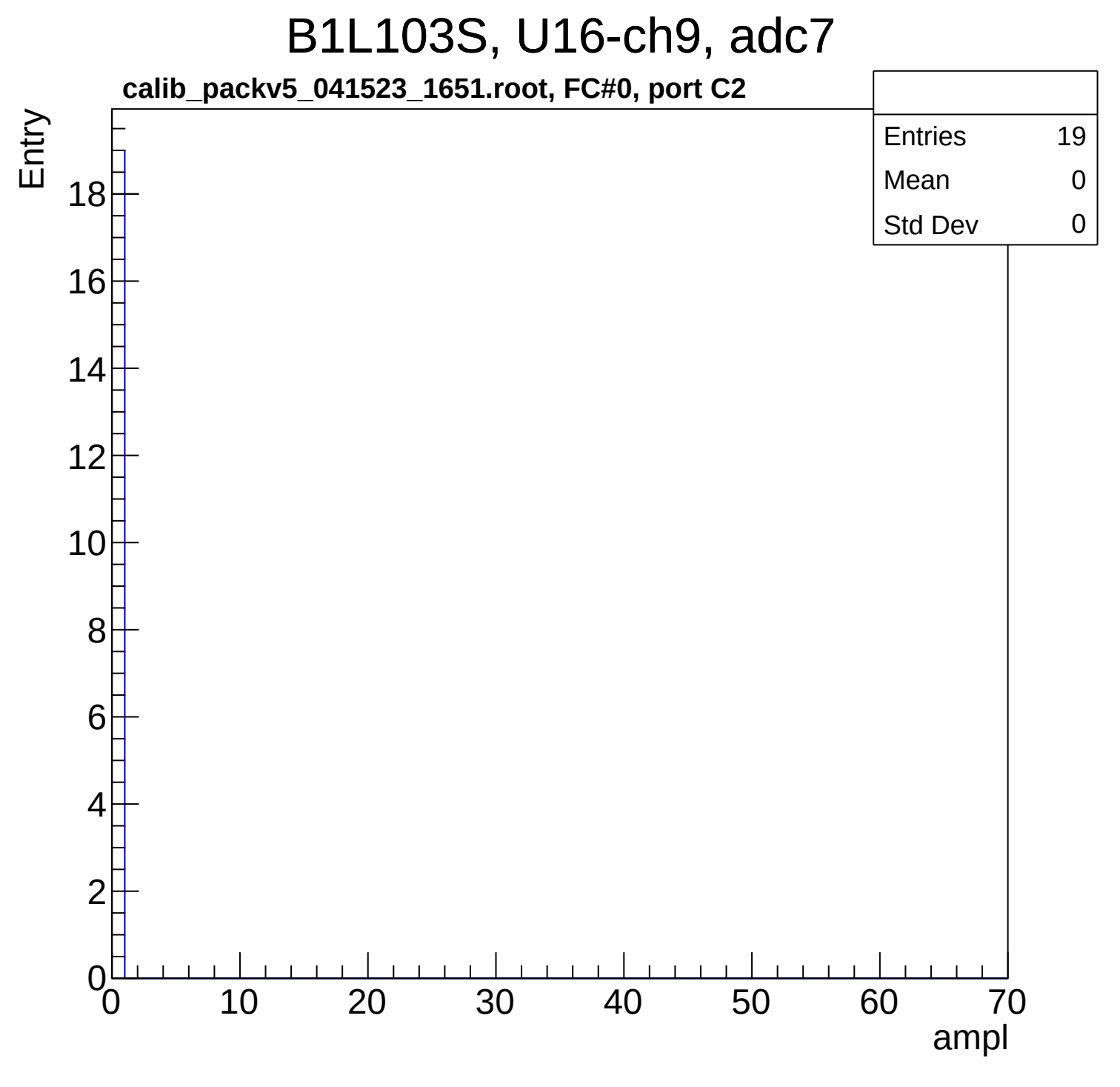
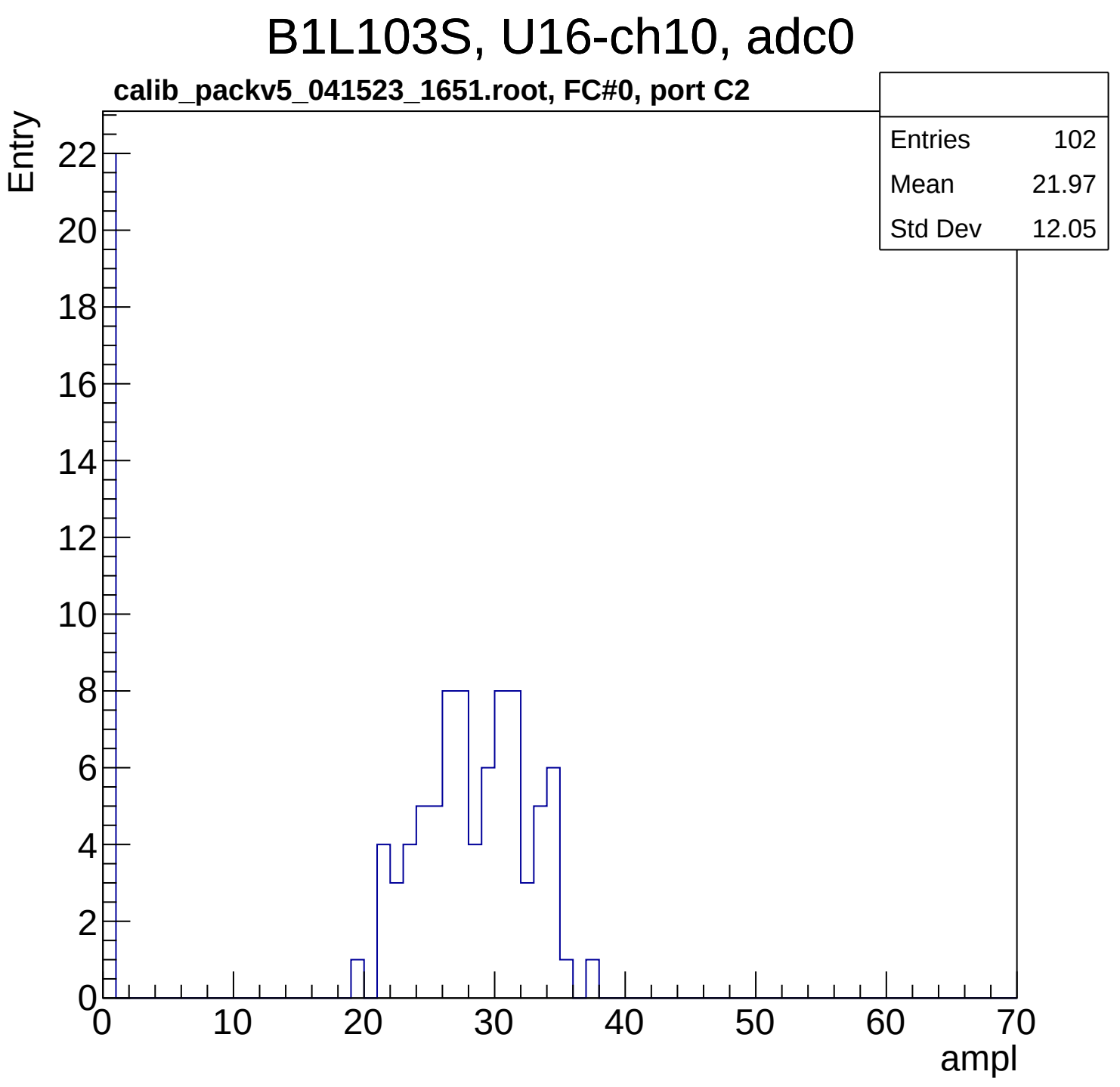
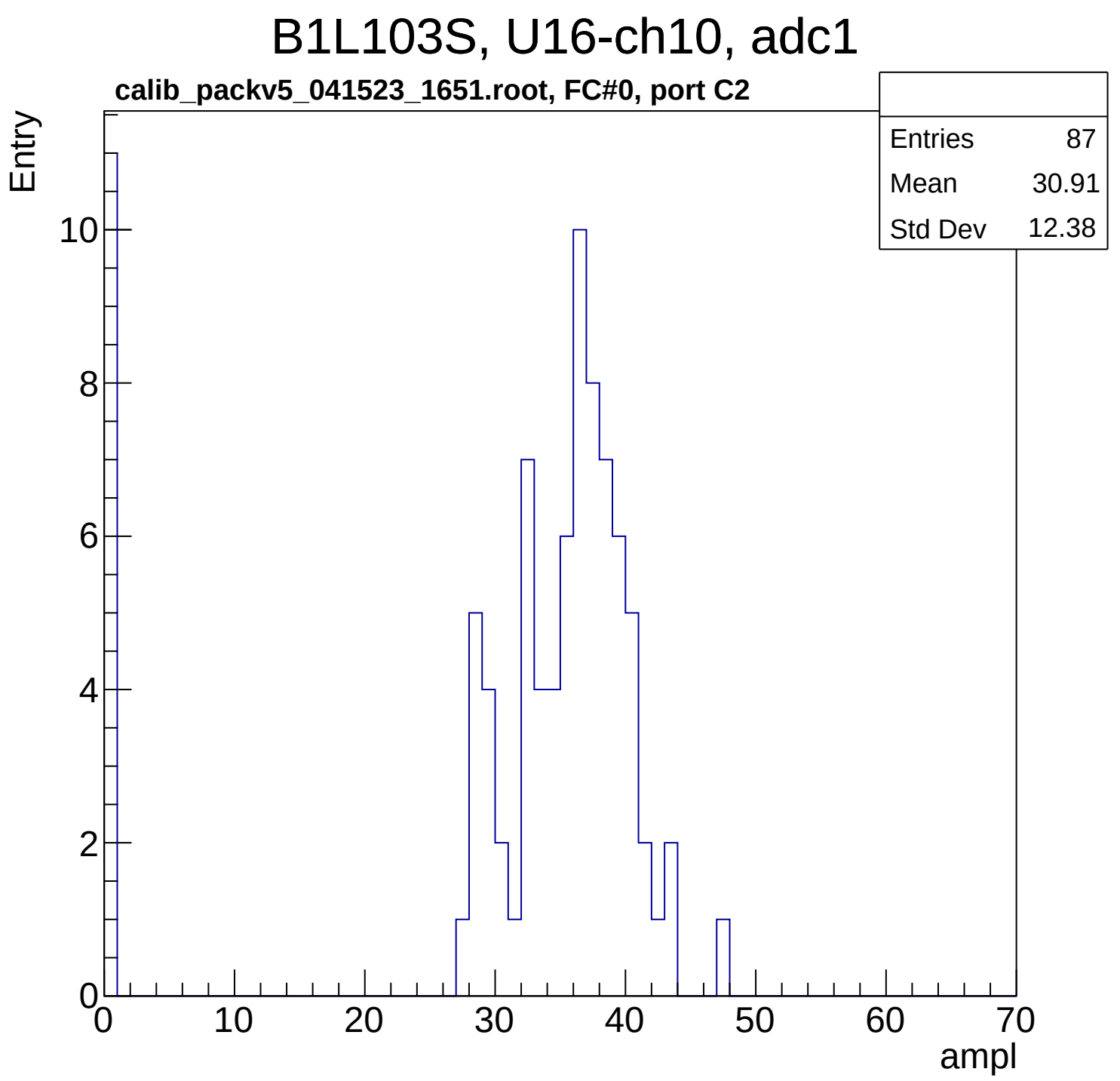
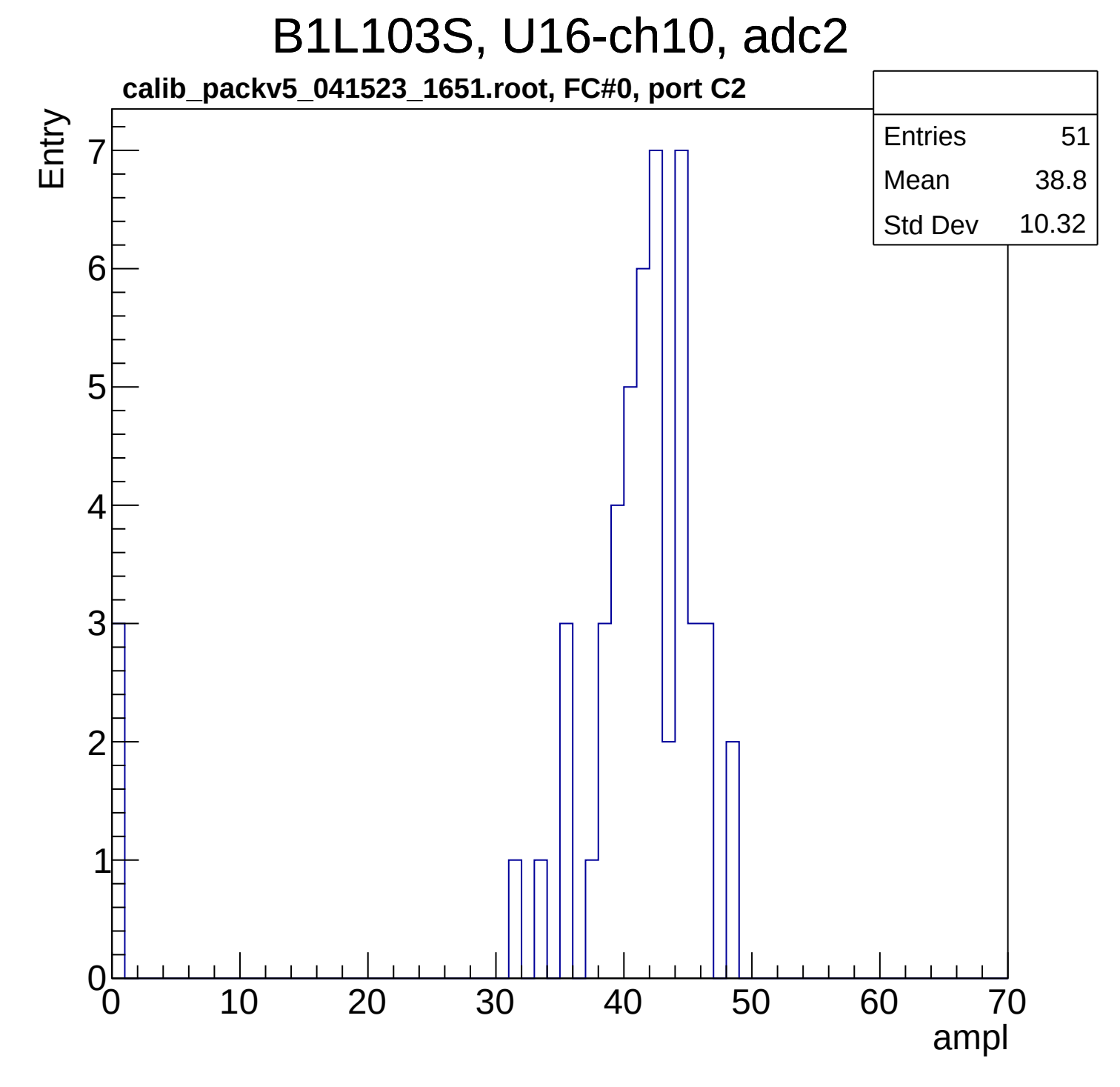
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

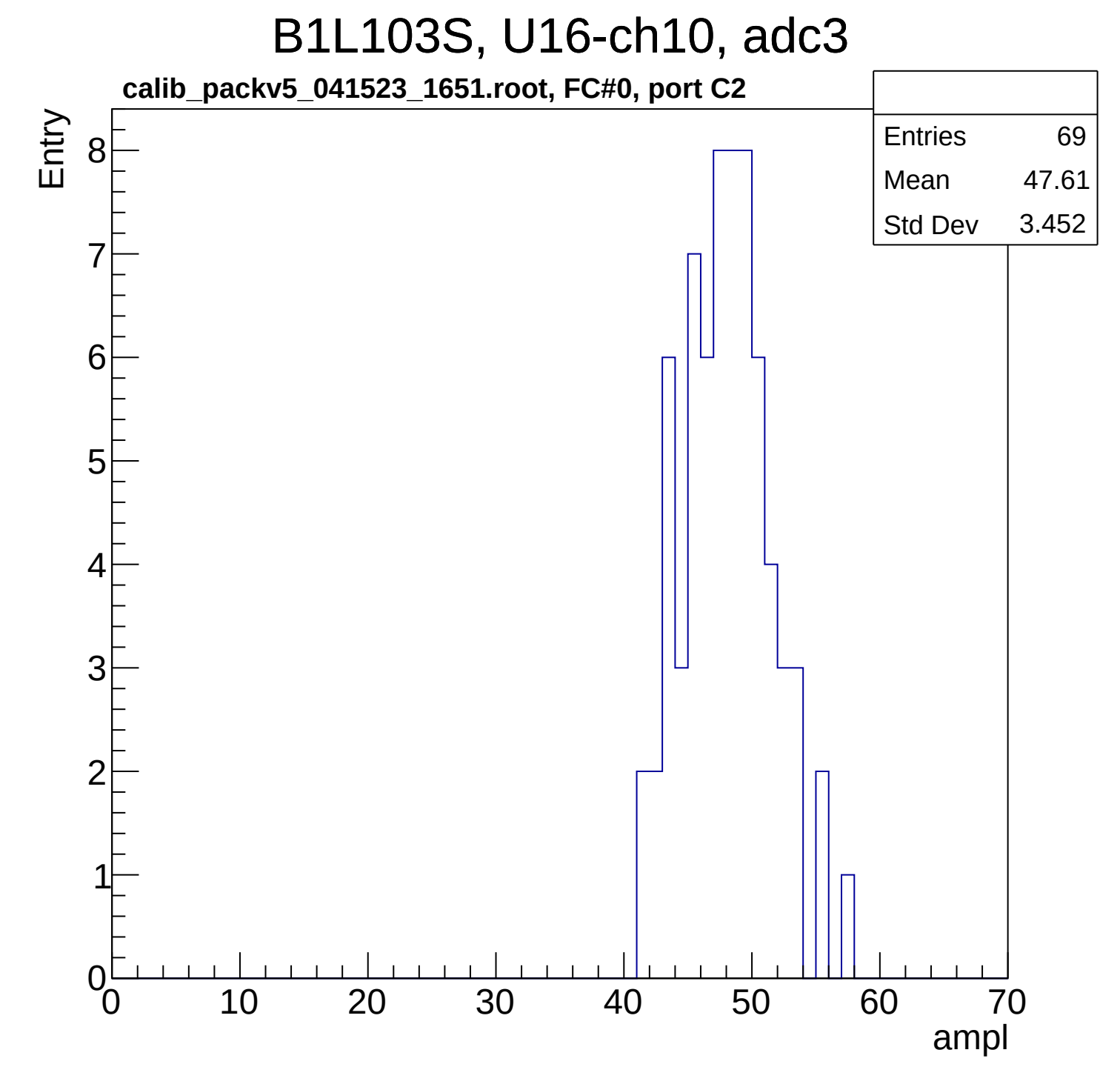

B1L103S, U16-ch9, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U16-ch9, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch10, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 21.97
Std Dev 12.05
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U16-ch10, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 30.91
Std Dev 12.38
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch10, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 38.8
Std Dev 10.32
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch10, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 47.61
Std Dev 3.452
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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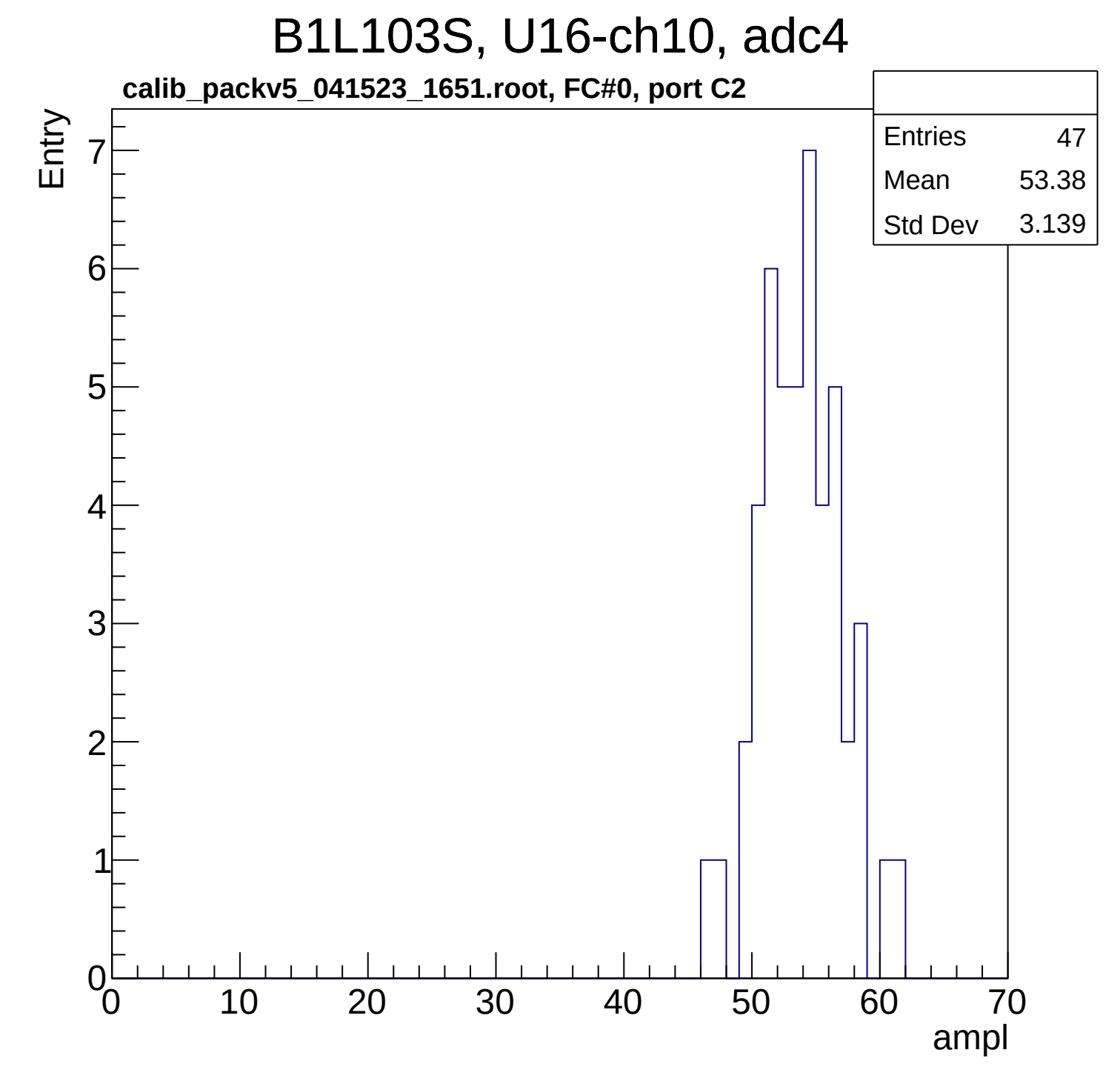
60
70


B1L103S, U16-ch10, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 53.38
Std Dev 3.139
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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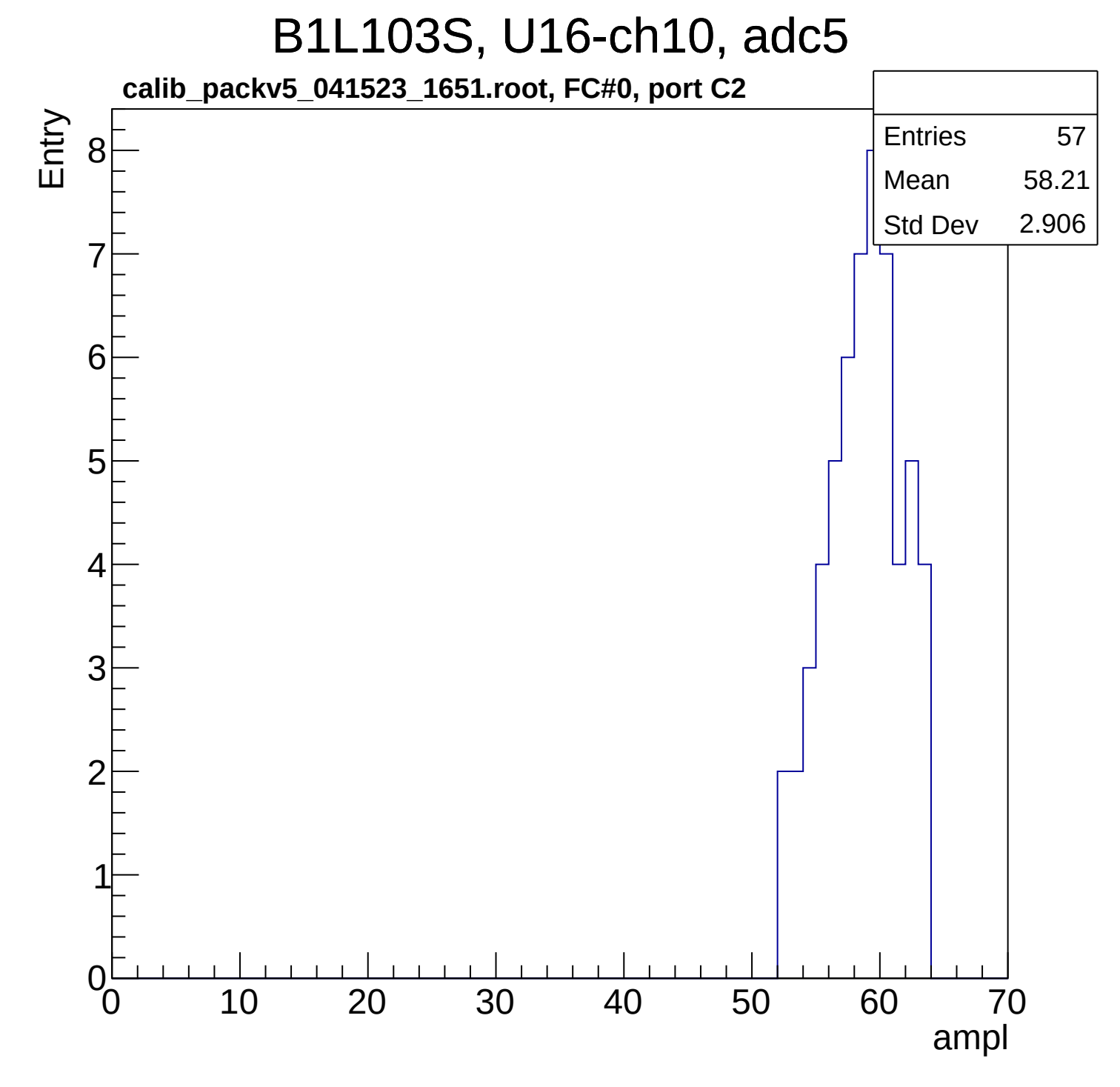
B1L103S, U16-ch10, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.21
Std Dev 2.906
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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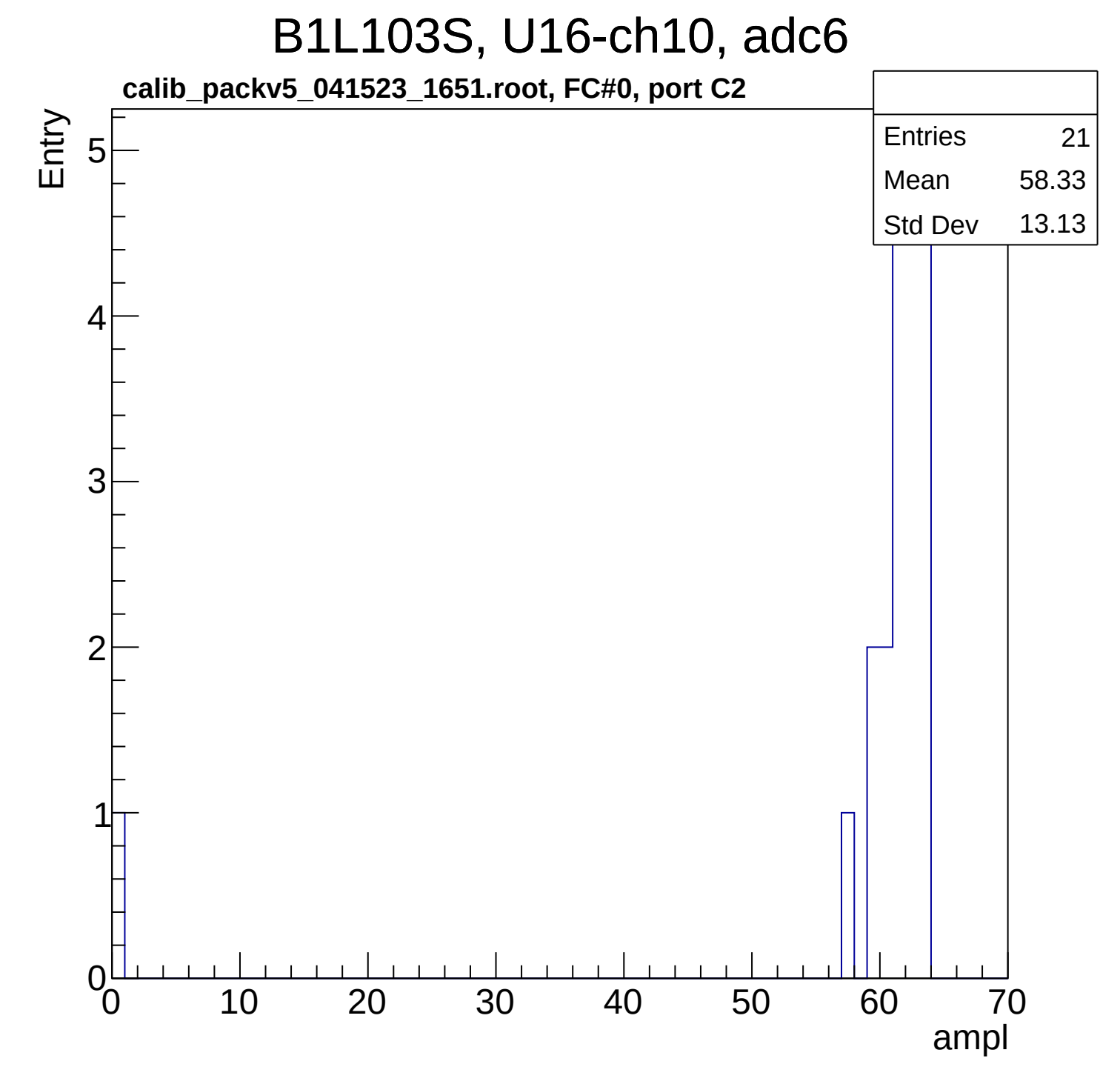
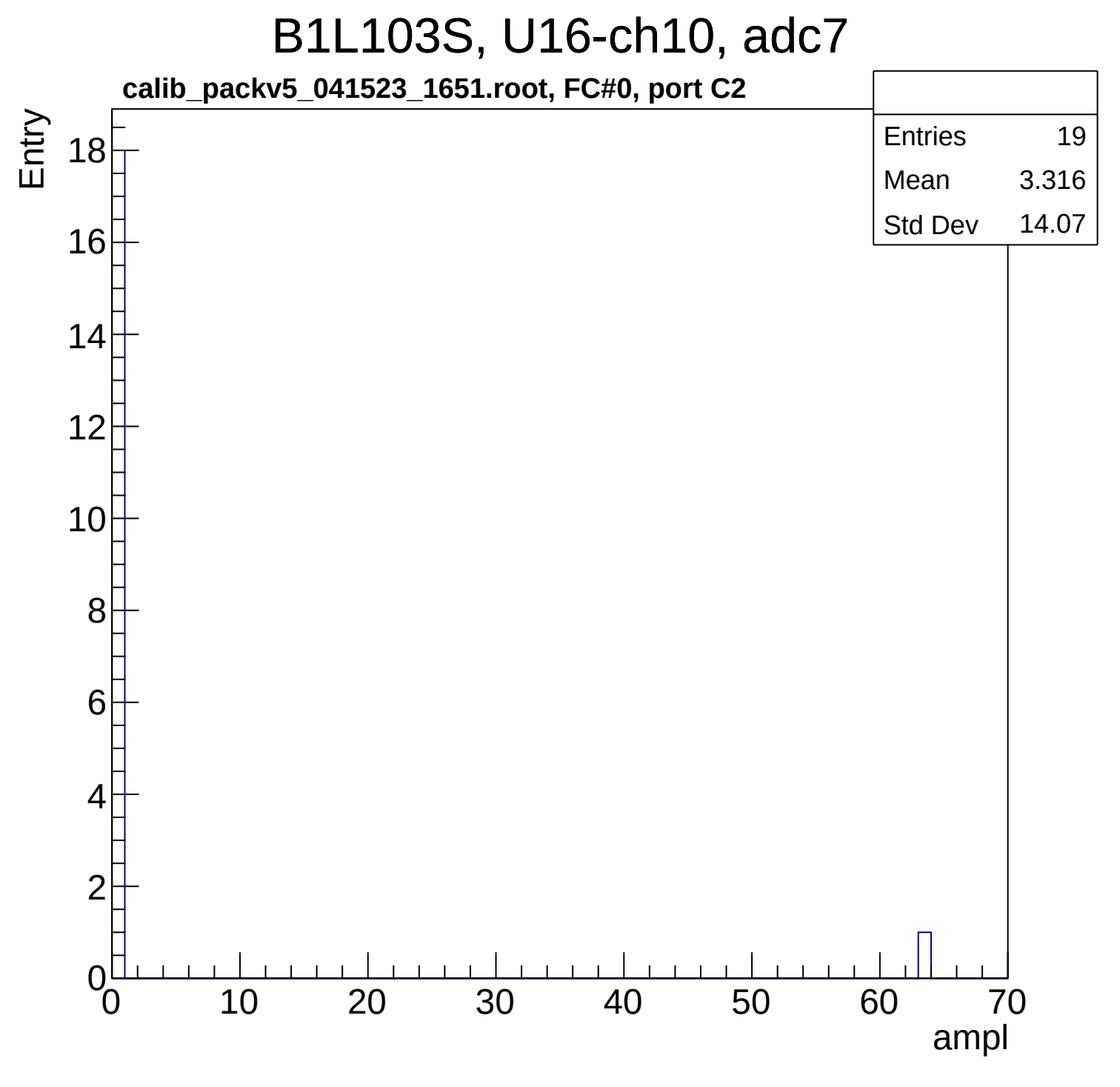
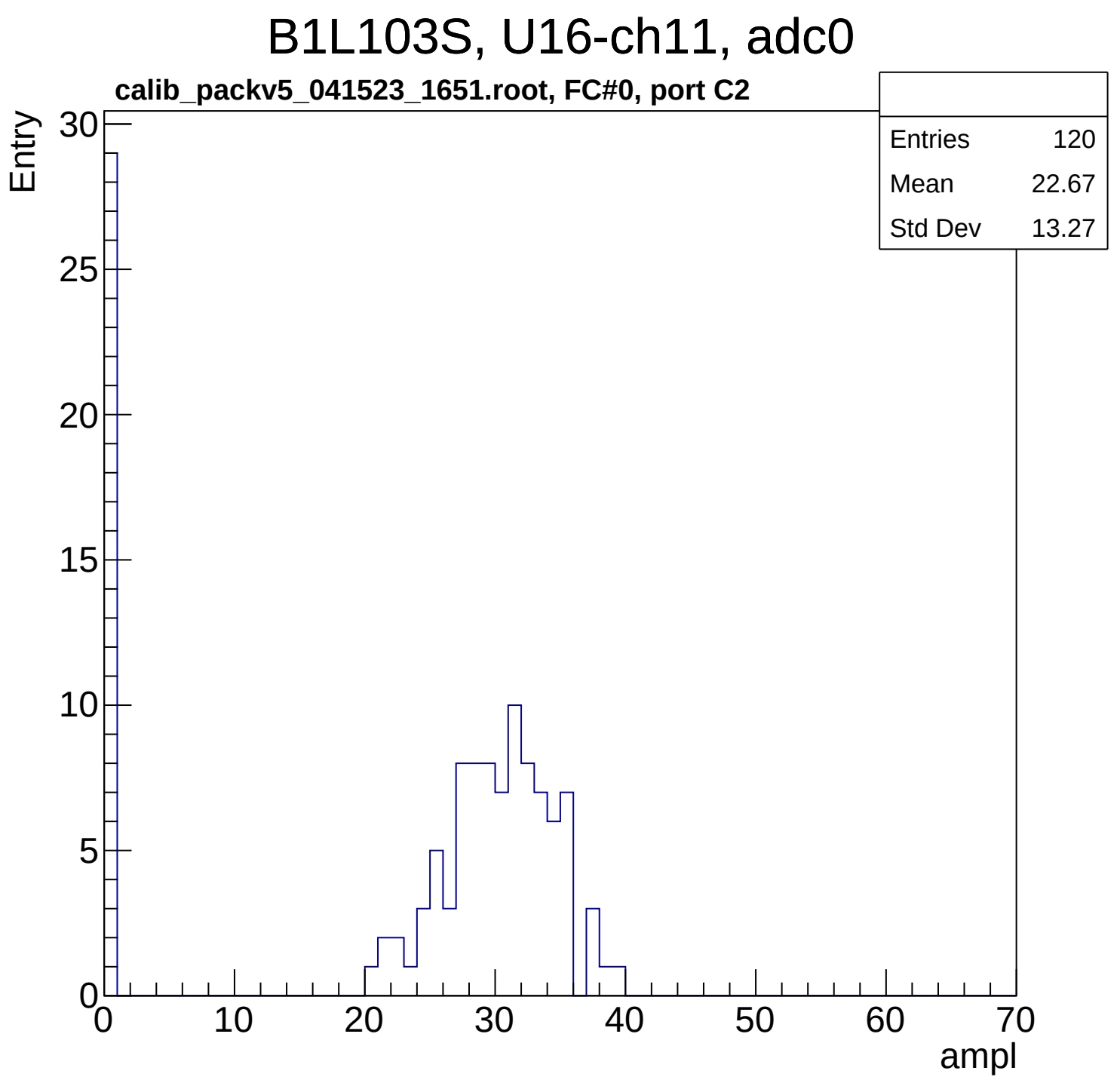
40
50
60
70


B1L103S, U16-ch10, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 58.33
Std Dev 13.13
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U16-ch10, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L103S, U16-ch11, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 120
Mean 22.67
Std Dev 13.27
Entry
ampl
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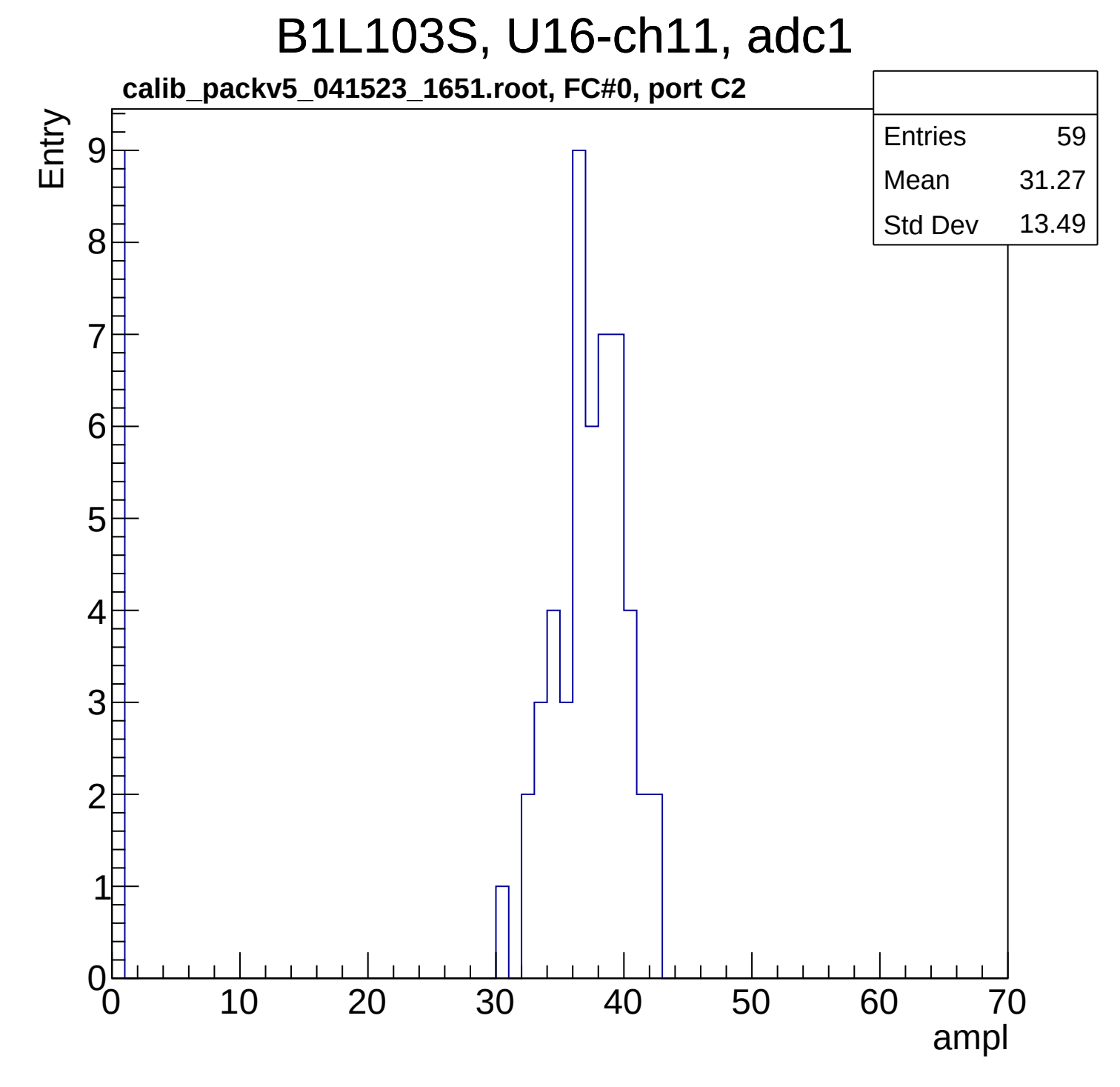
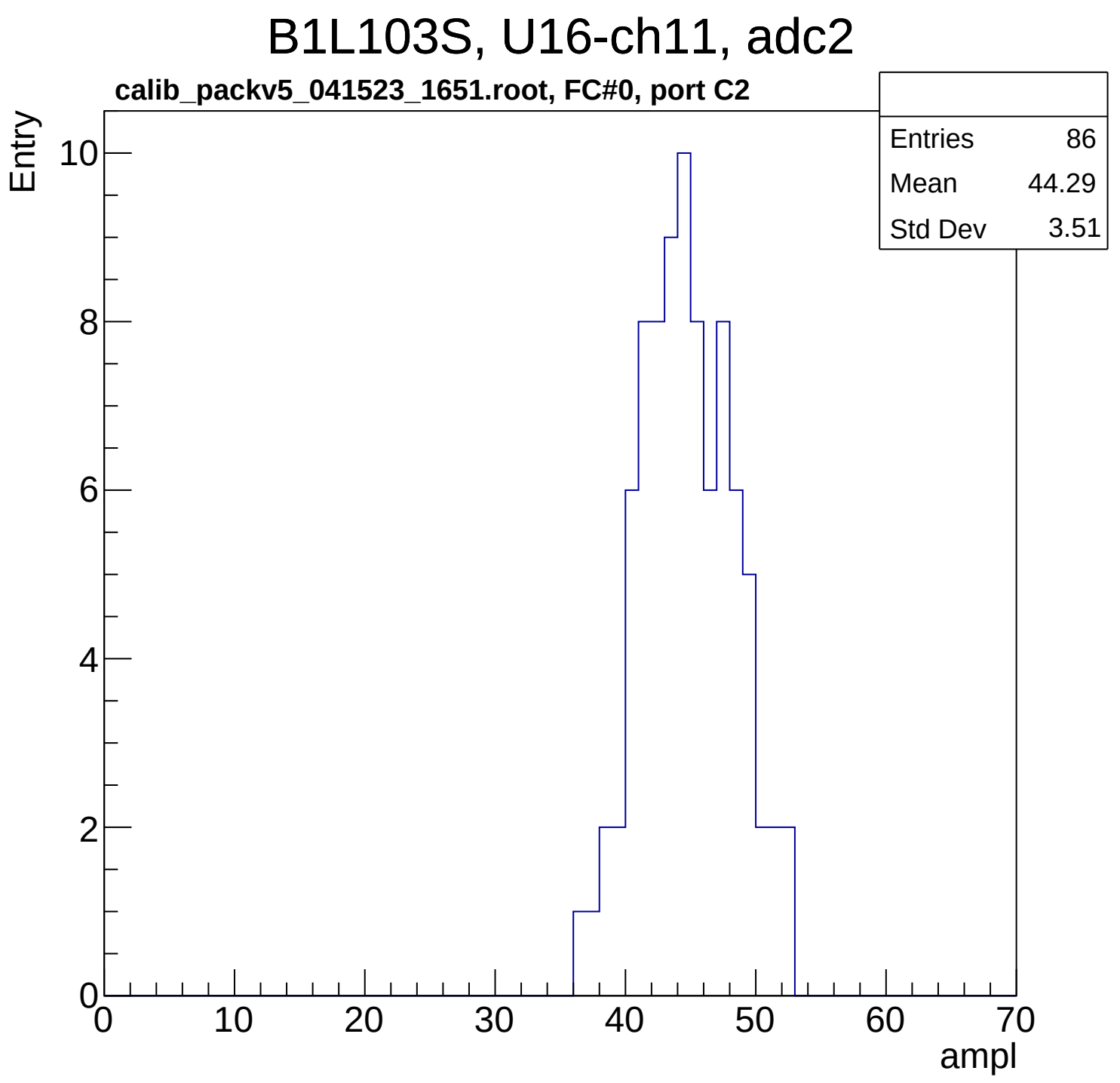
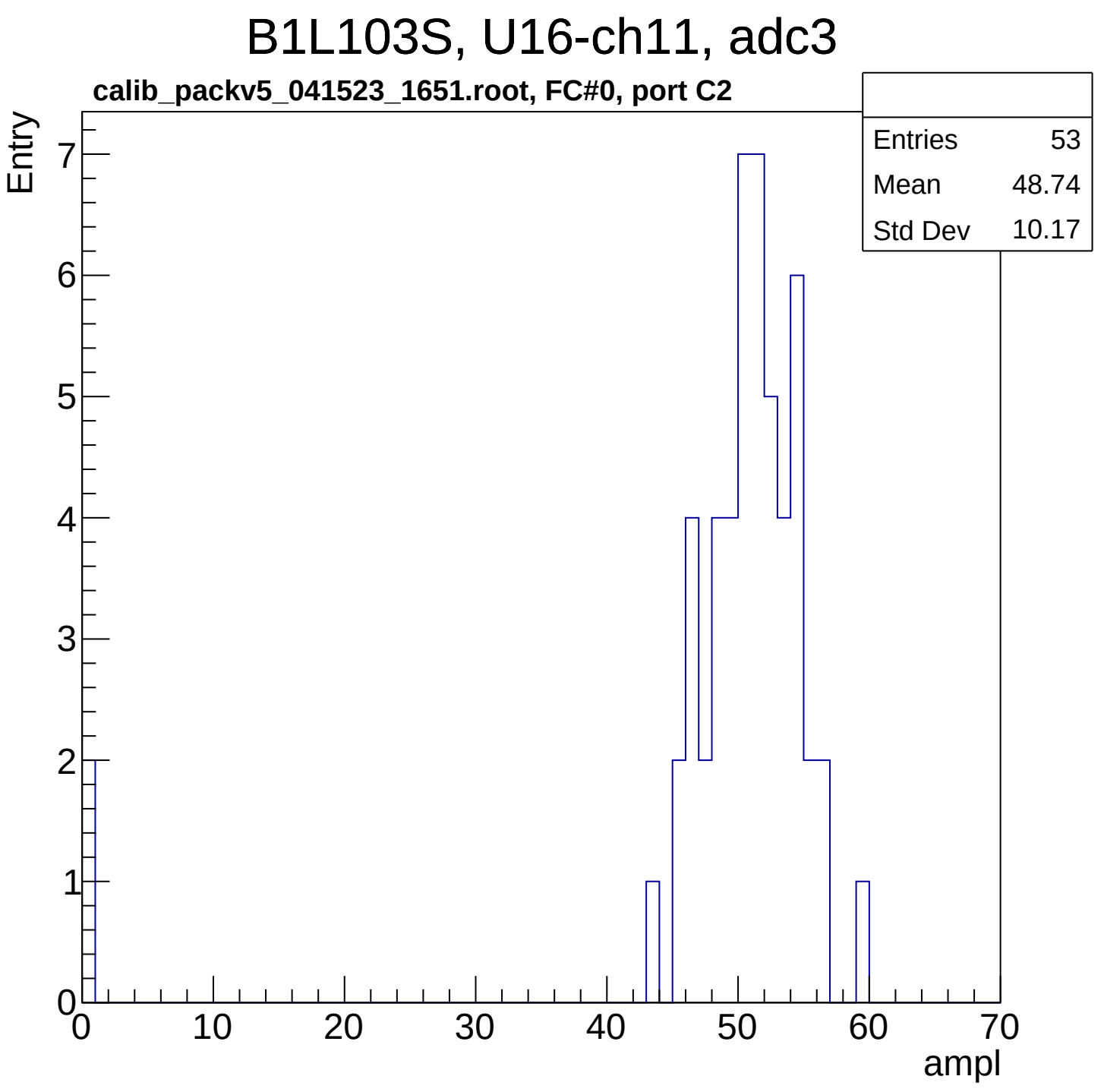
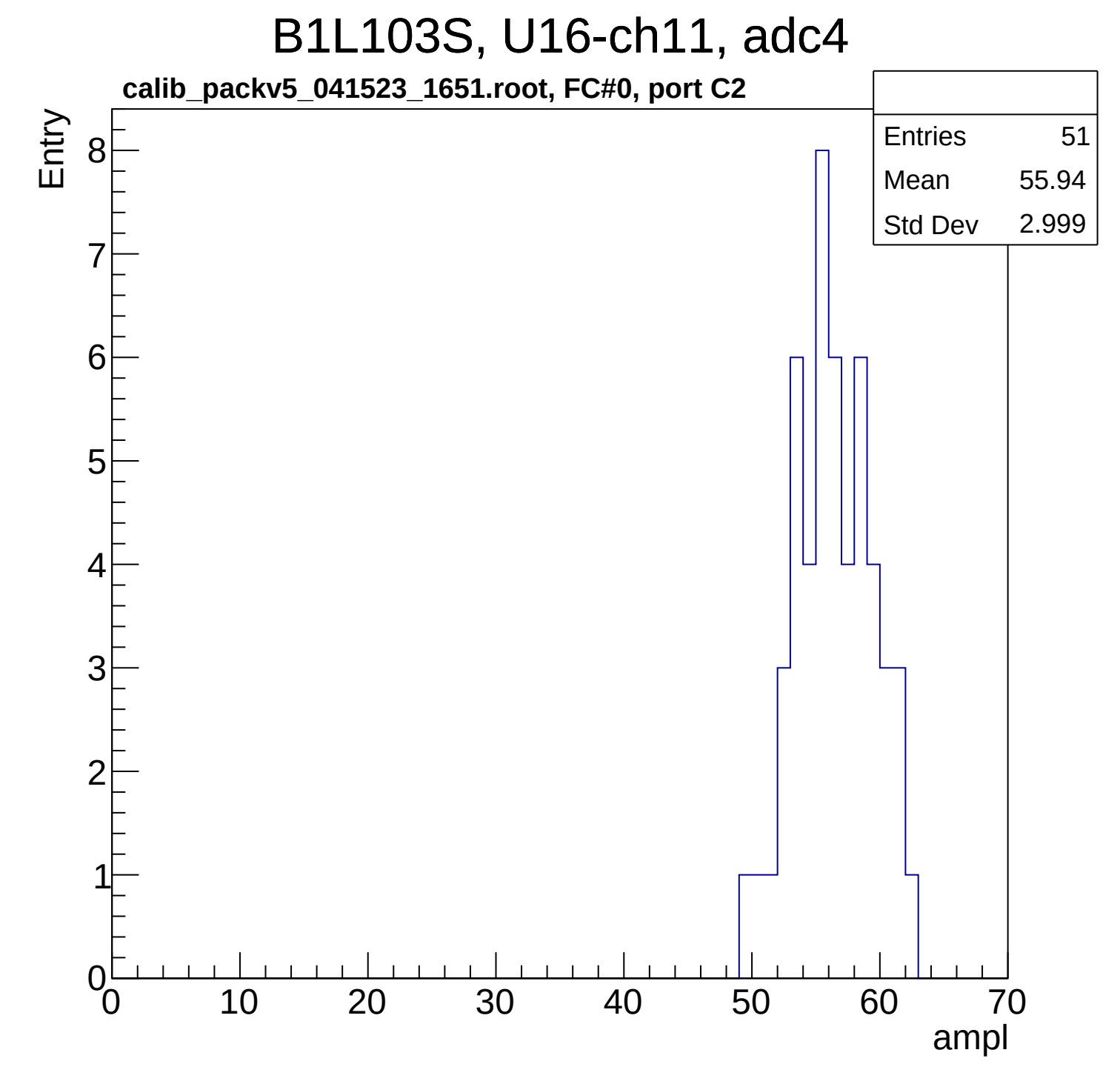
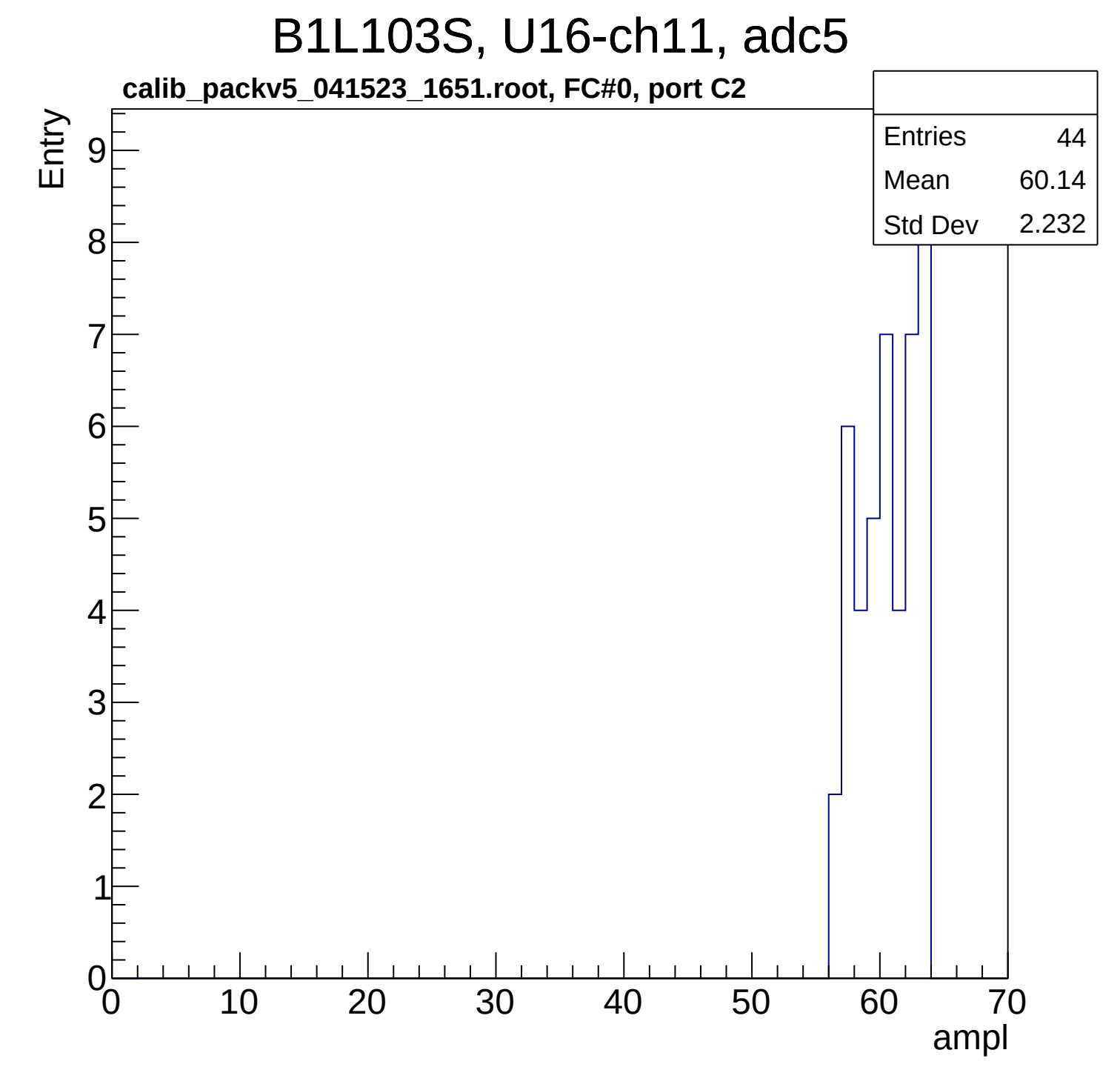
5
10
15
20
25
30
0
10
20
30
40
50
60
70


B1L103S, U16-ch11, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 31.27
Std Dev 13.49
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch11, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 44.29
Std Dev 3.51
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch11, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 48.74
Std Dev 10.17
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch11, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 55.94
Std Dev 2.999
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch11, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 60.14
Std Dev 2.232
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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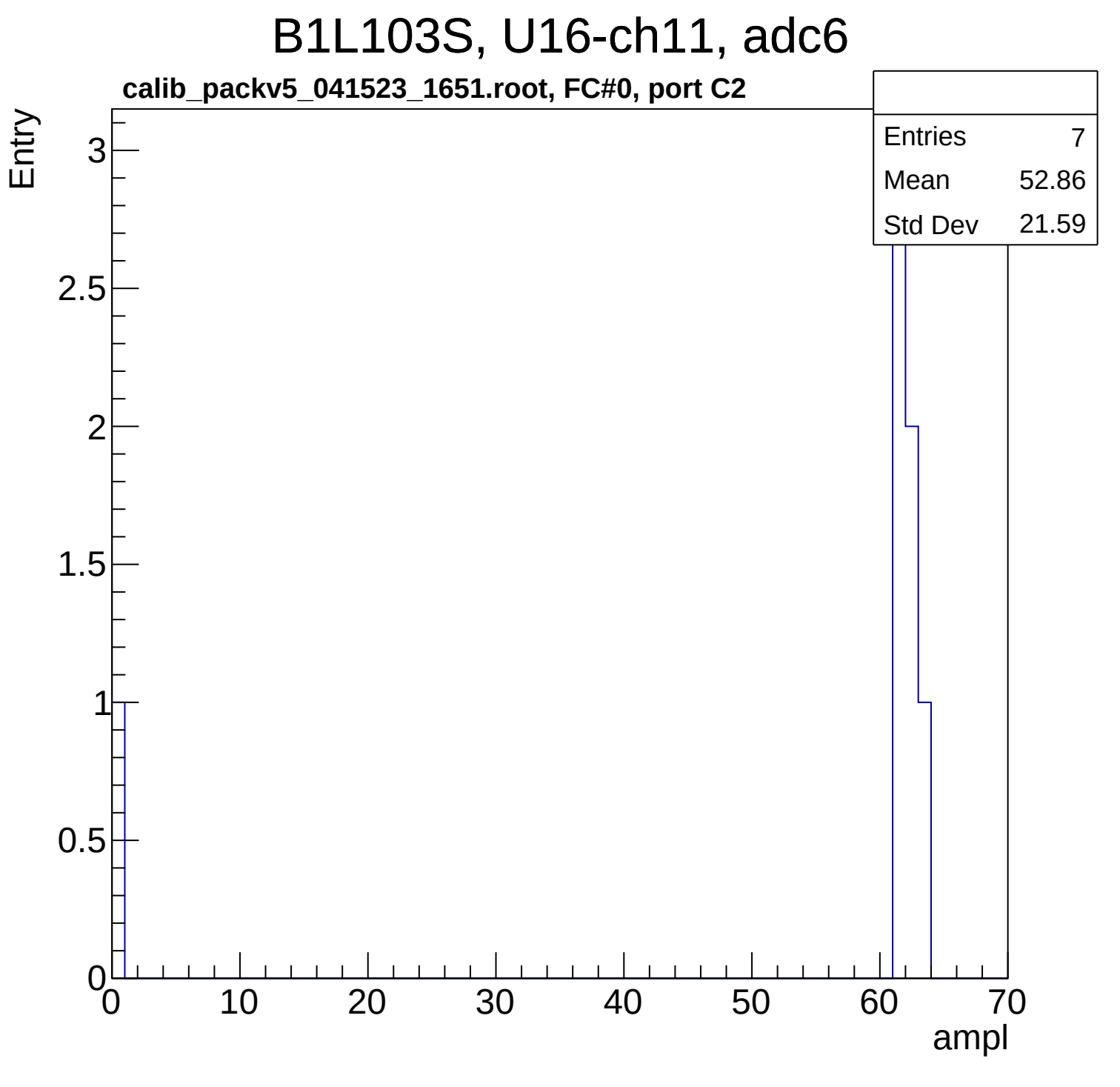
B1L103S, U16-ch11, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 52.86
Std Dev 21.59
Entry
ampl
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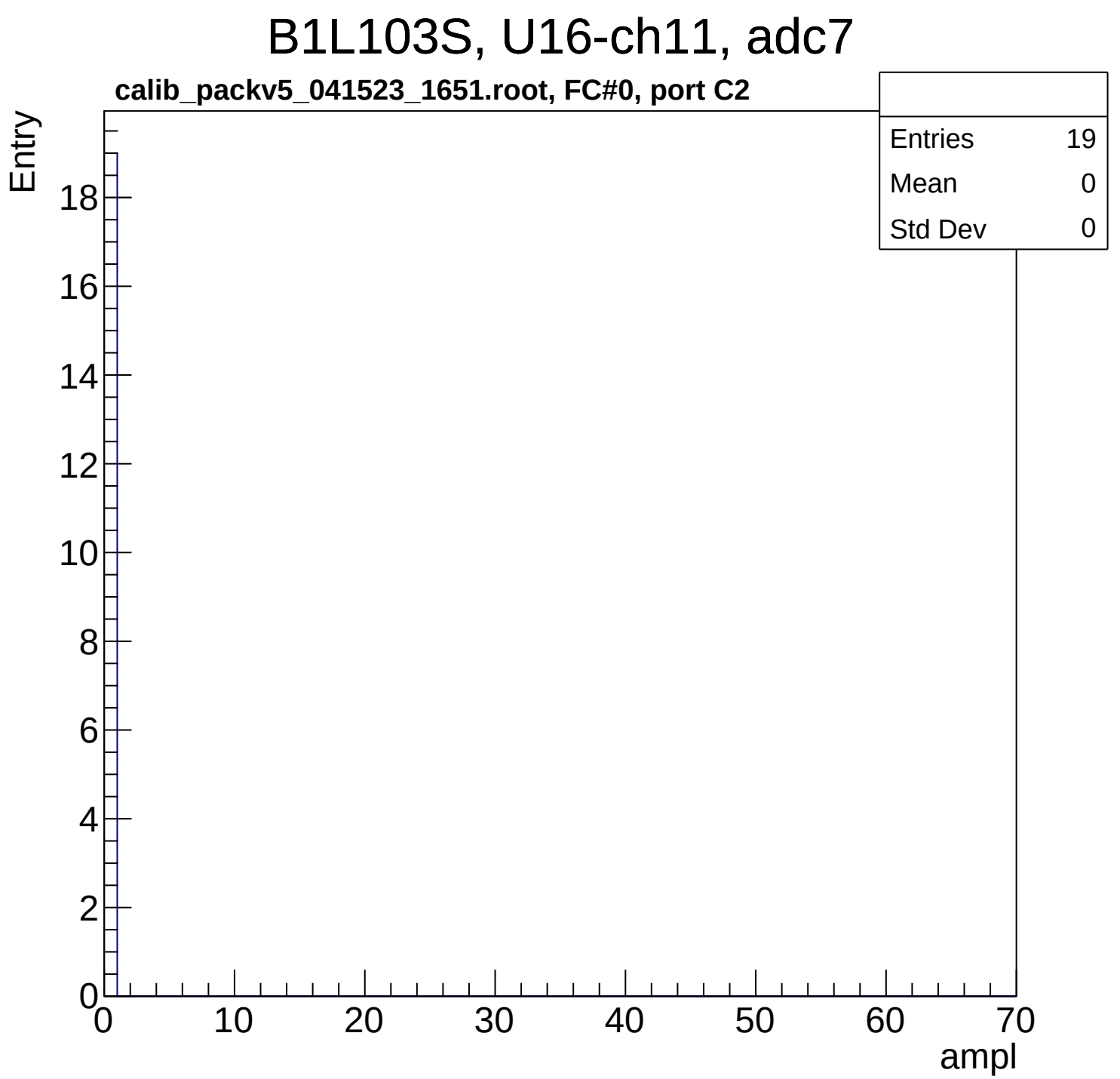
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U16-ch11, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
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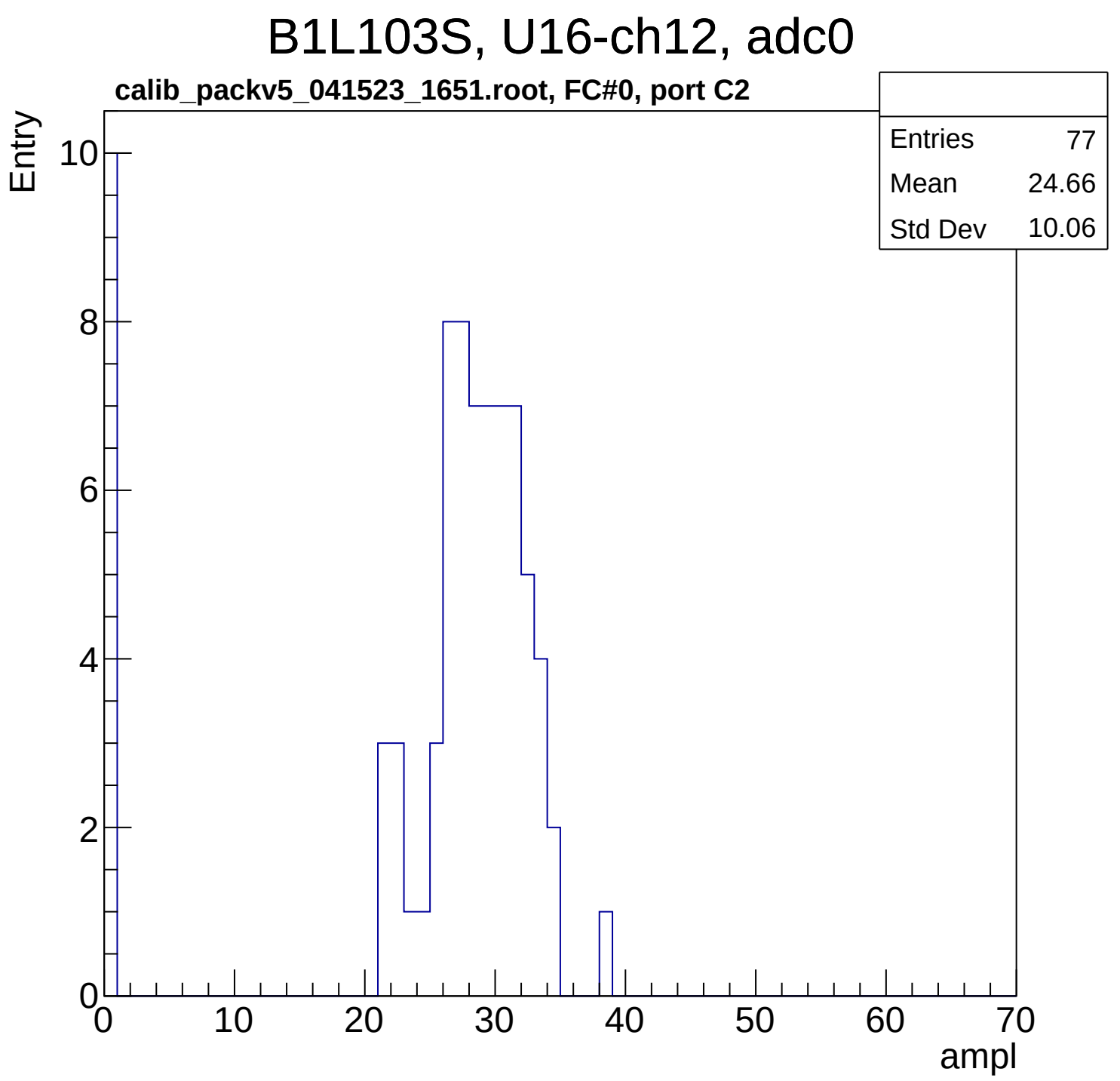
40
50
60
70
ampl


B1L103S, U16-ch12, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 24.66
Std Dev 10.06
Entry
ampl
0
2
4
6
8
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0
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40
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60
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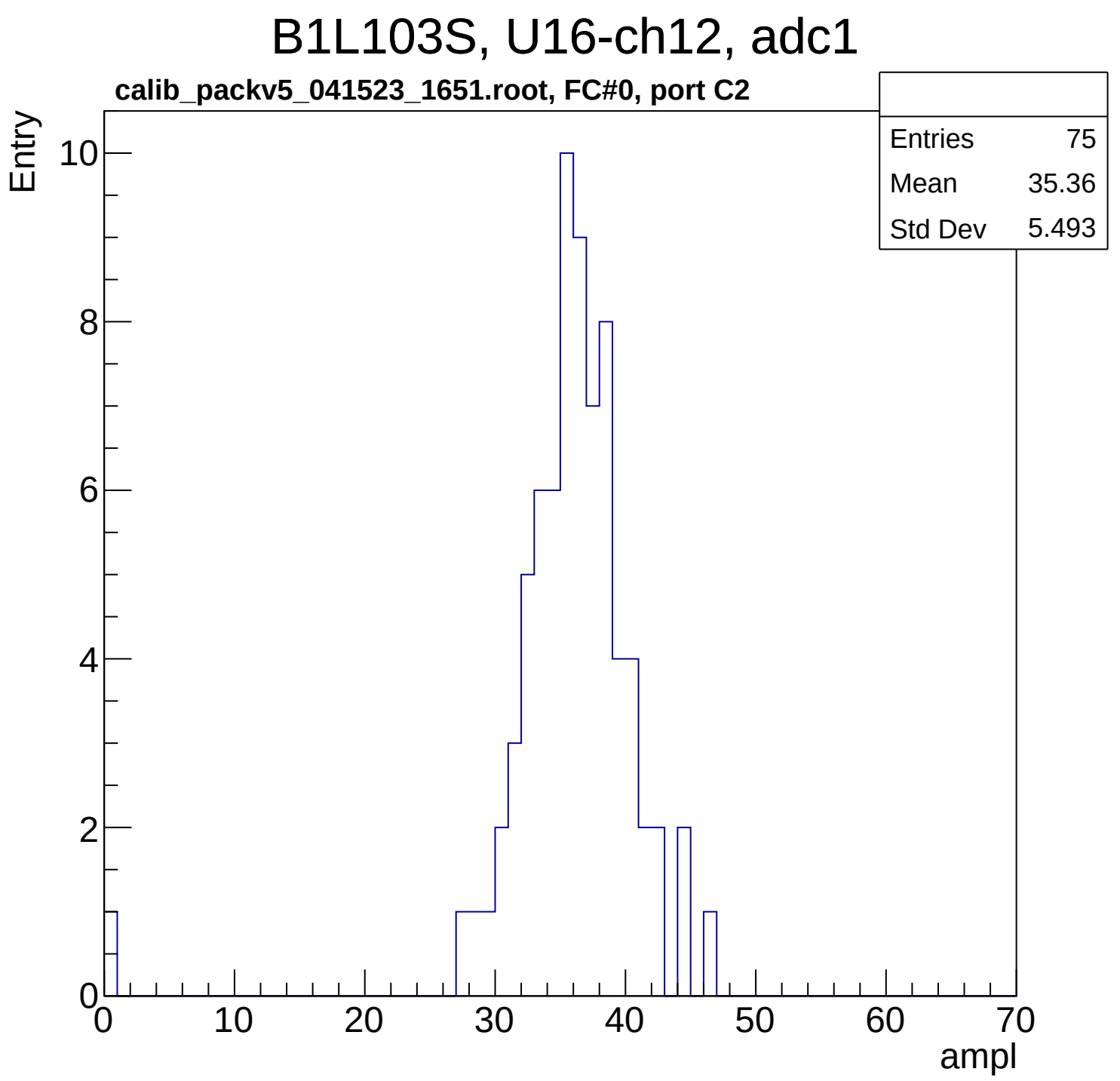
B1L103S, U16-ch12, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 35.36
Std Dev 5.493
Entry
ampl
0
2
4
6
8
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0
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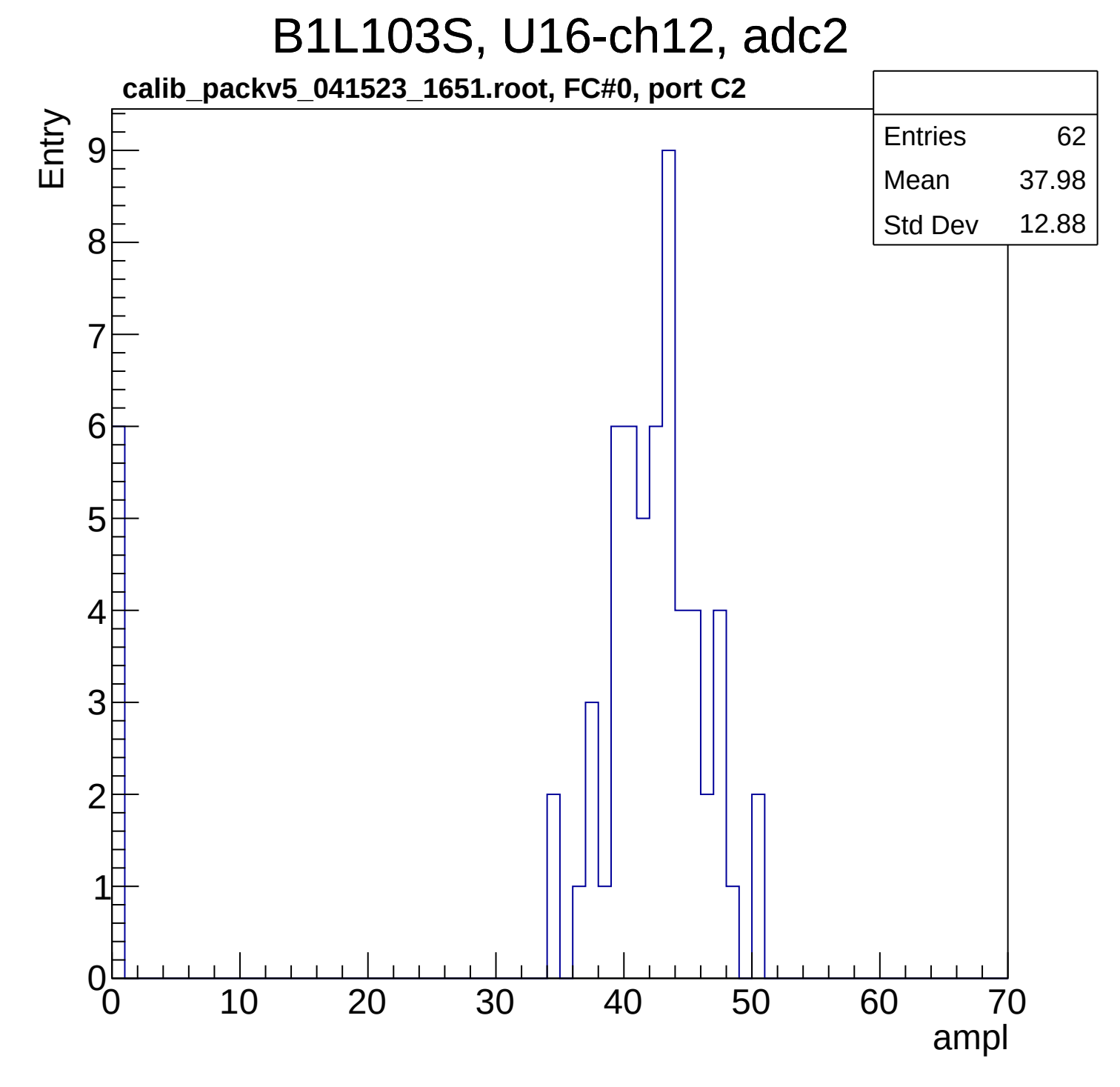
40
50
60
70


B1L103S, U16-ch12, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 37.98
Std Dev 12.88
Entry
ampl
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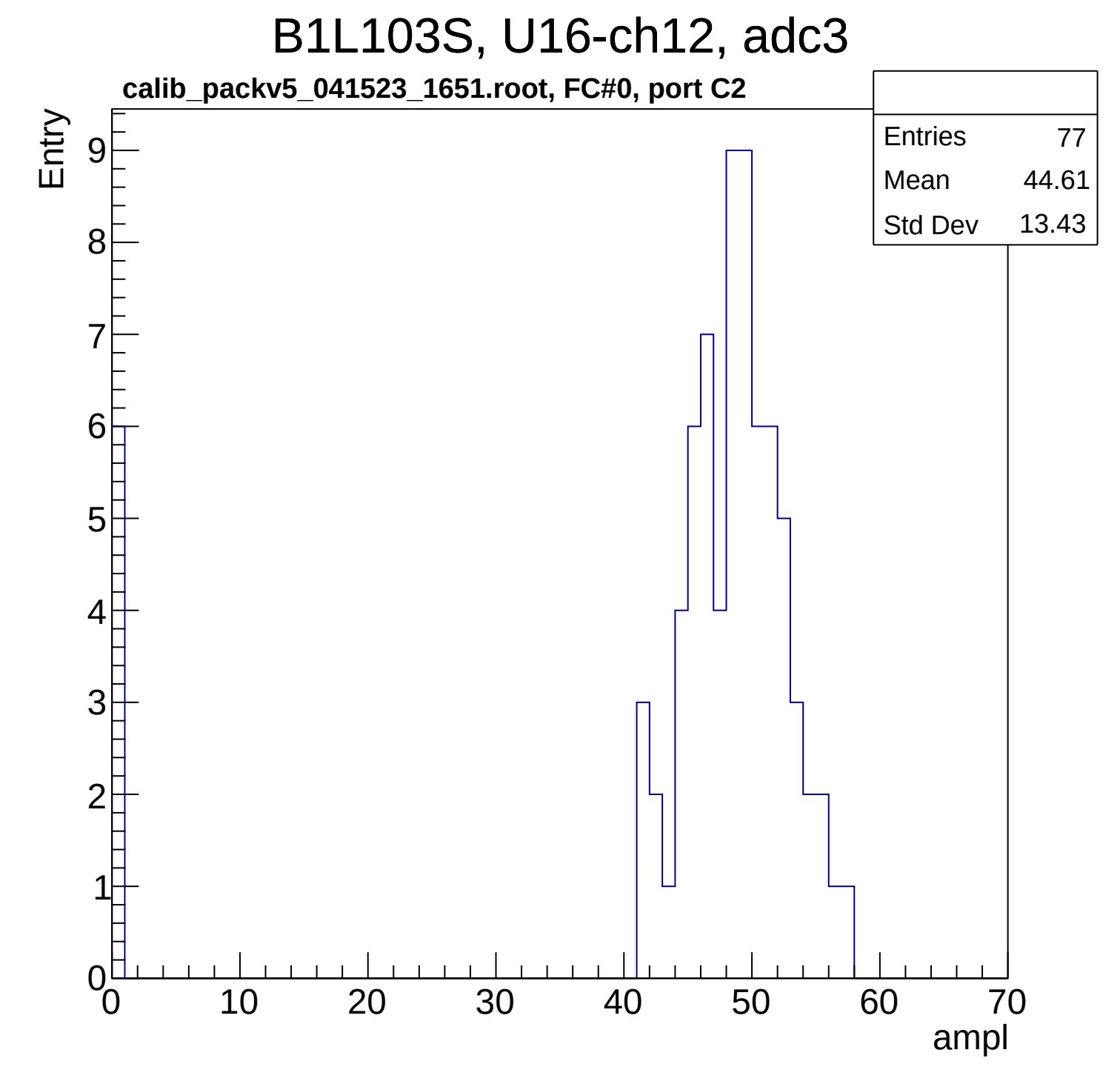
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch12, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 44.61
Std Dev 13.43
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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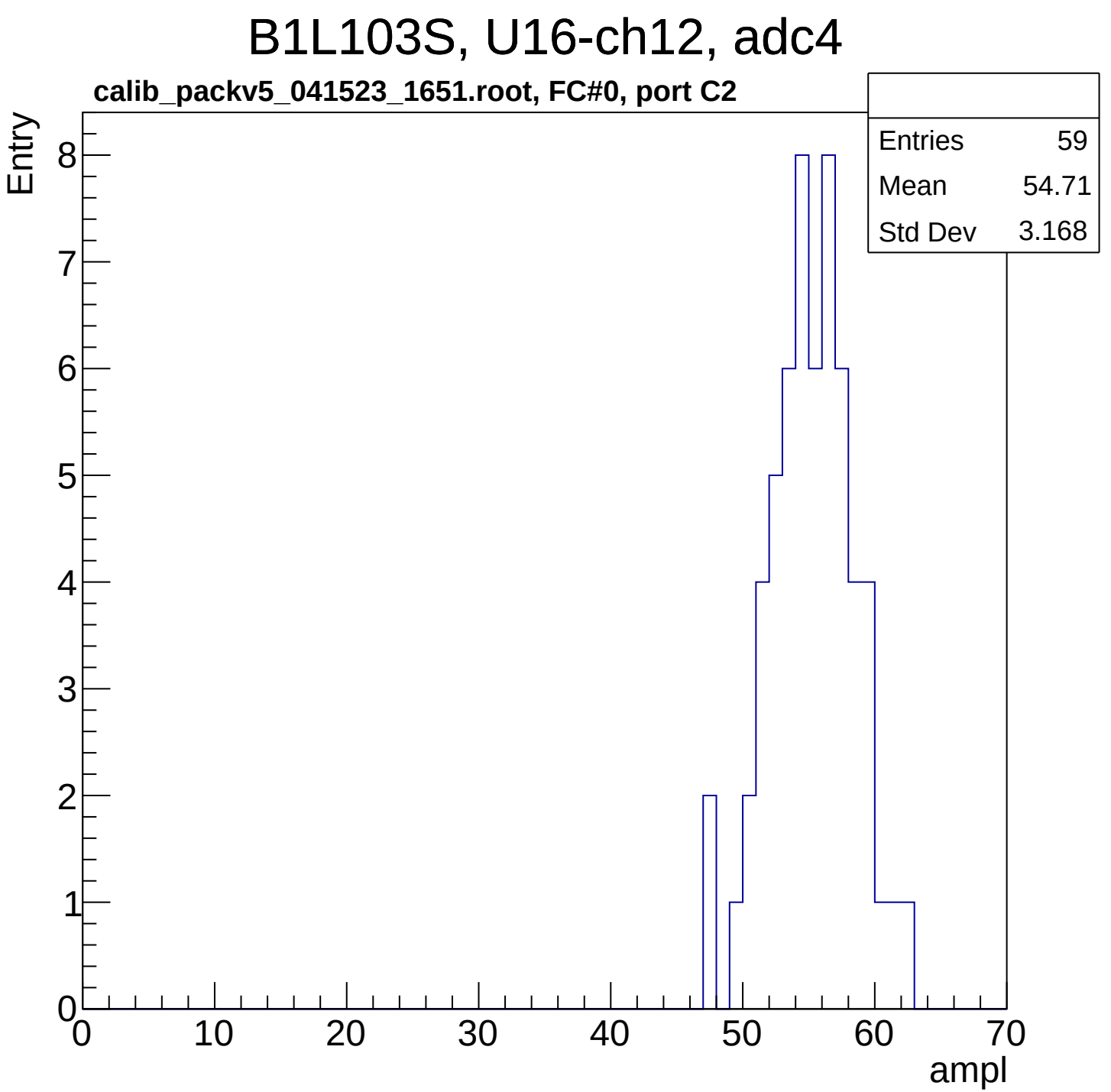
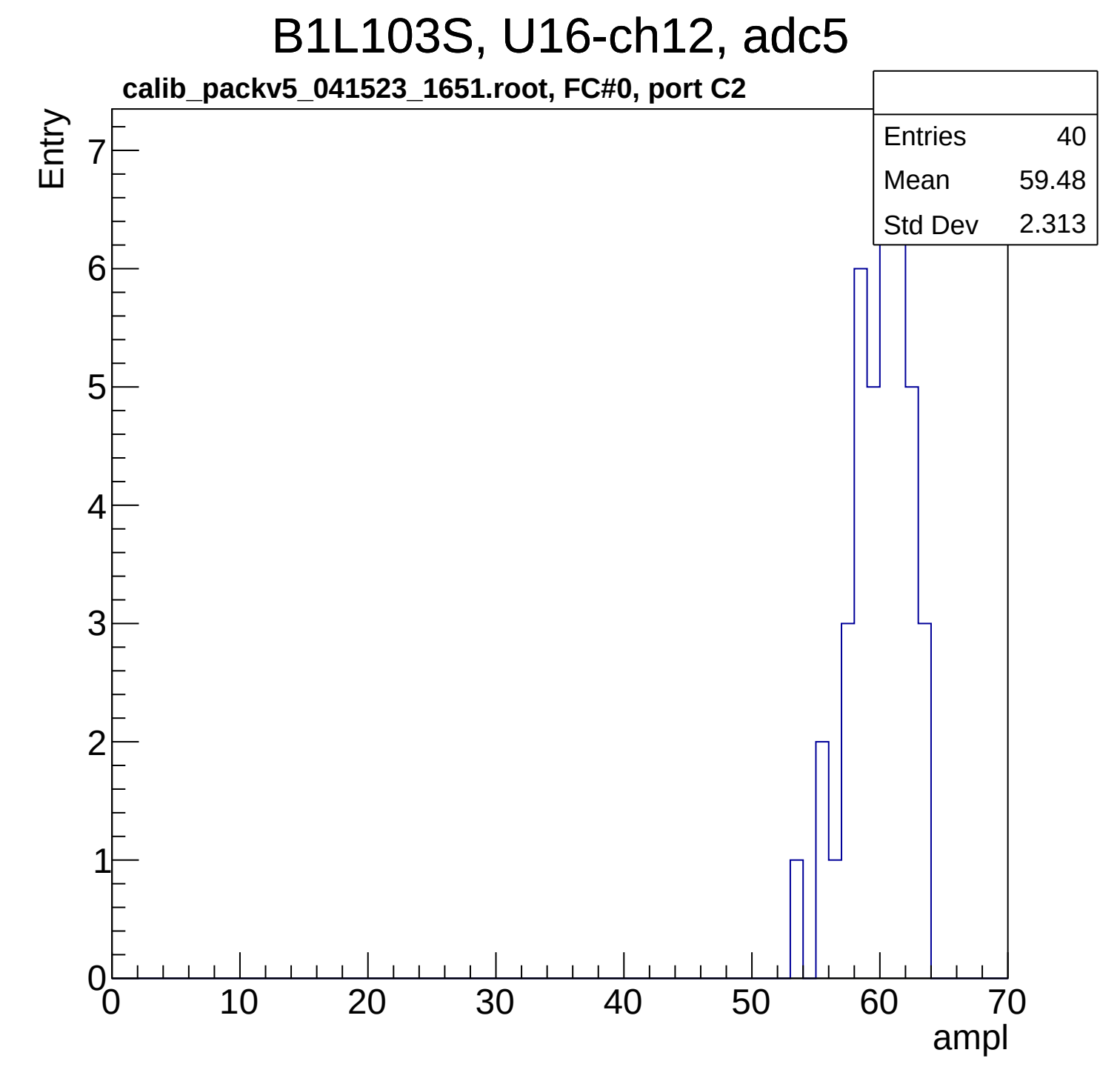
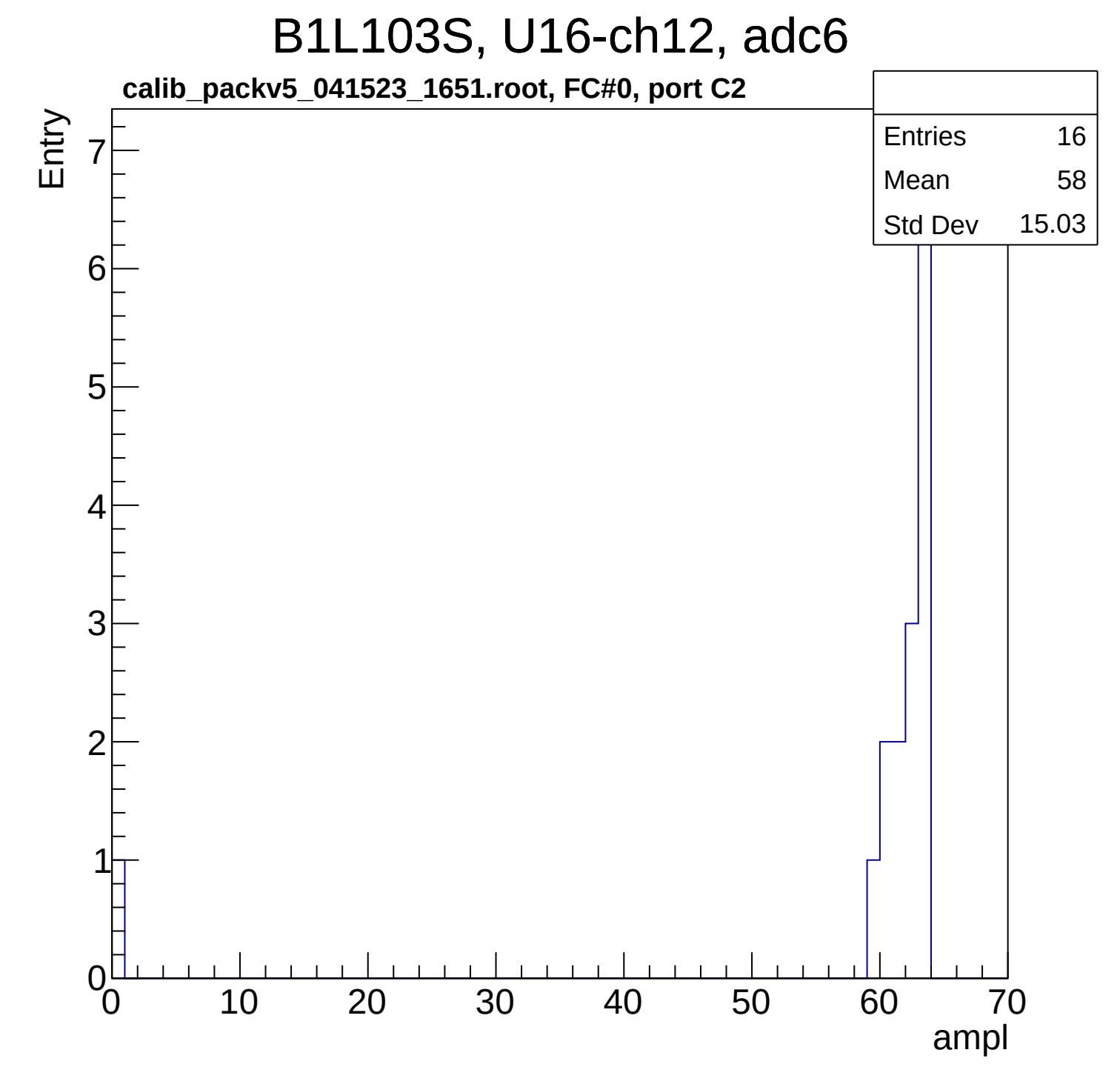
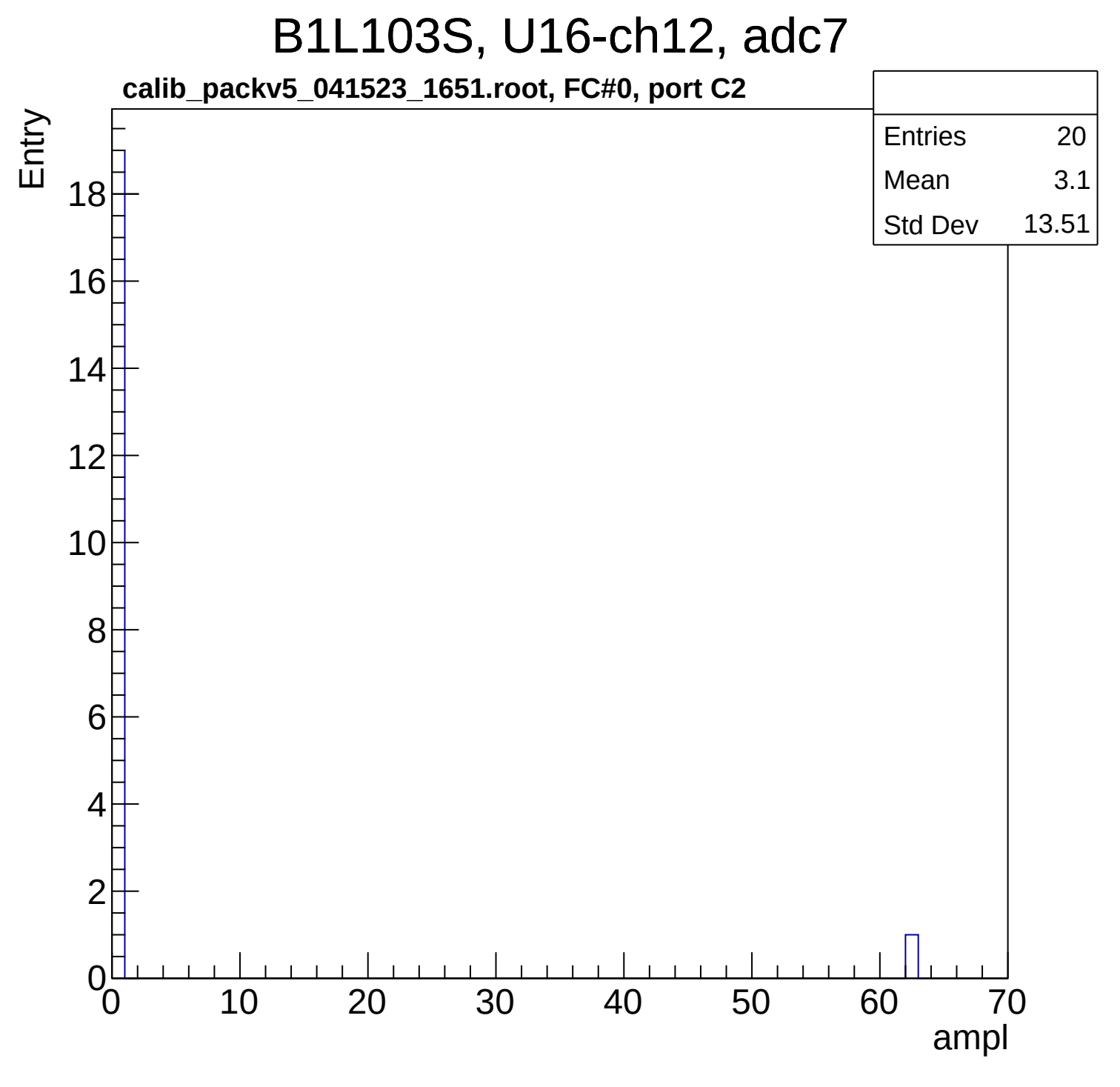
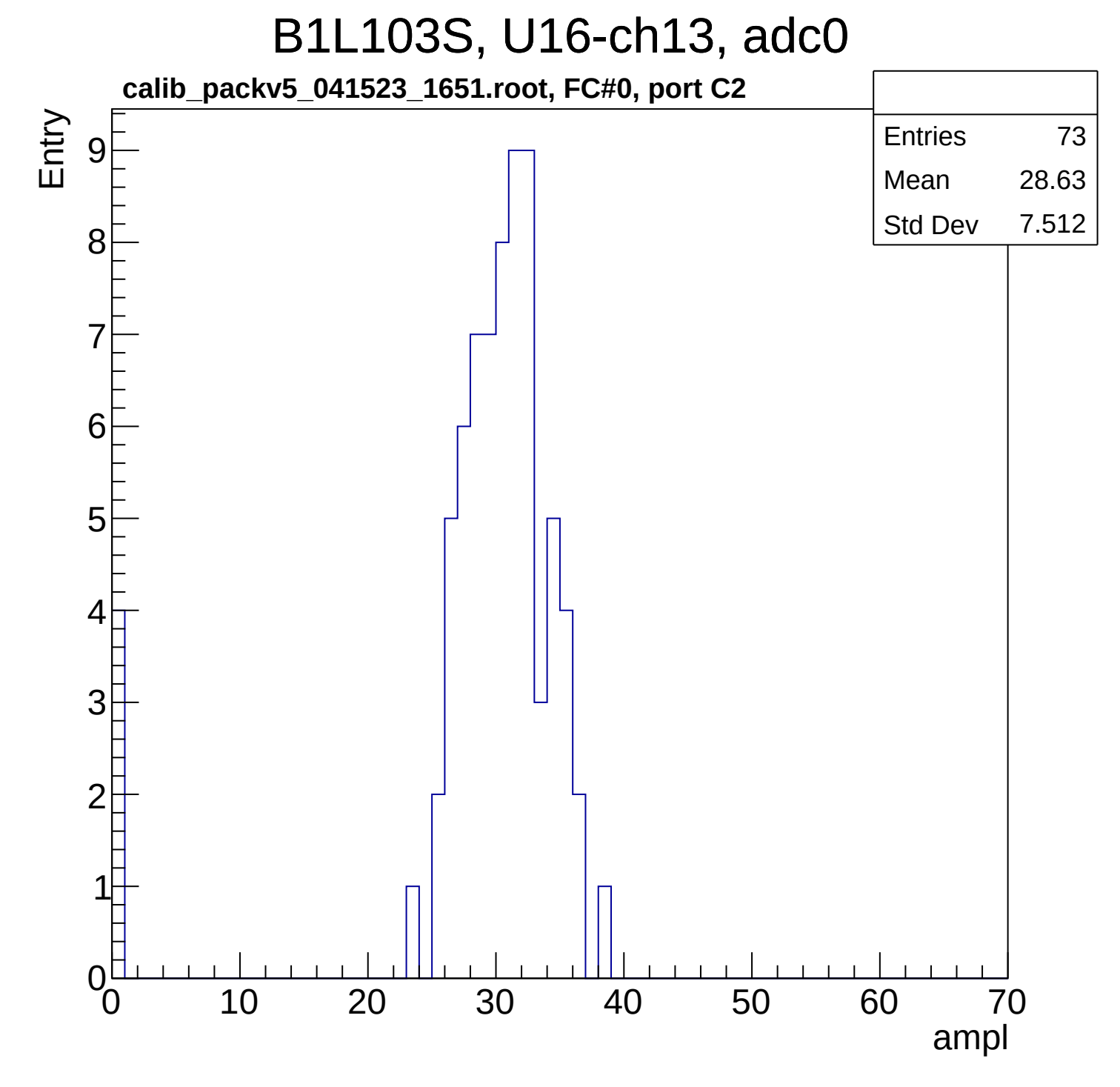
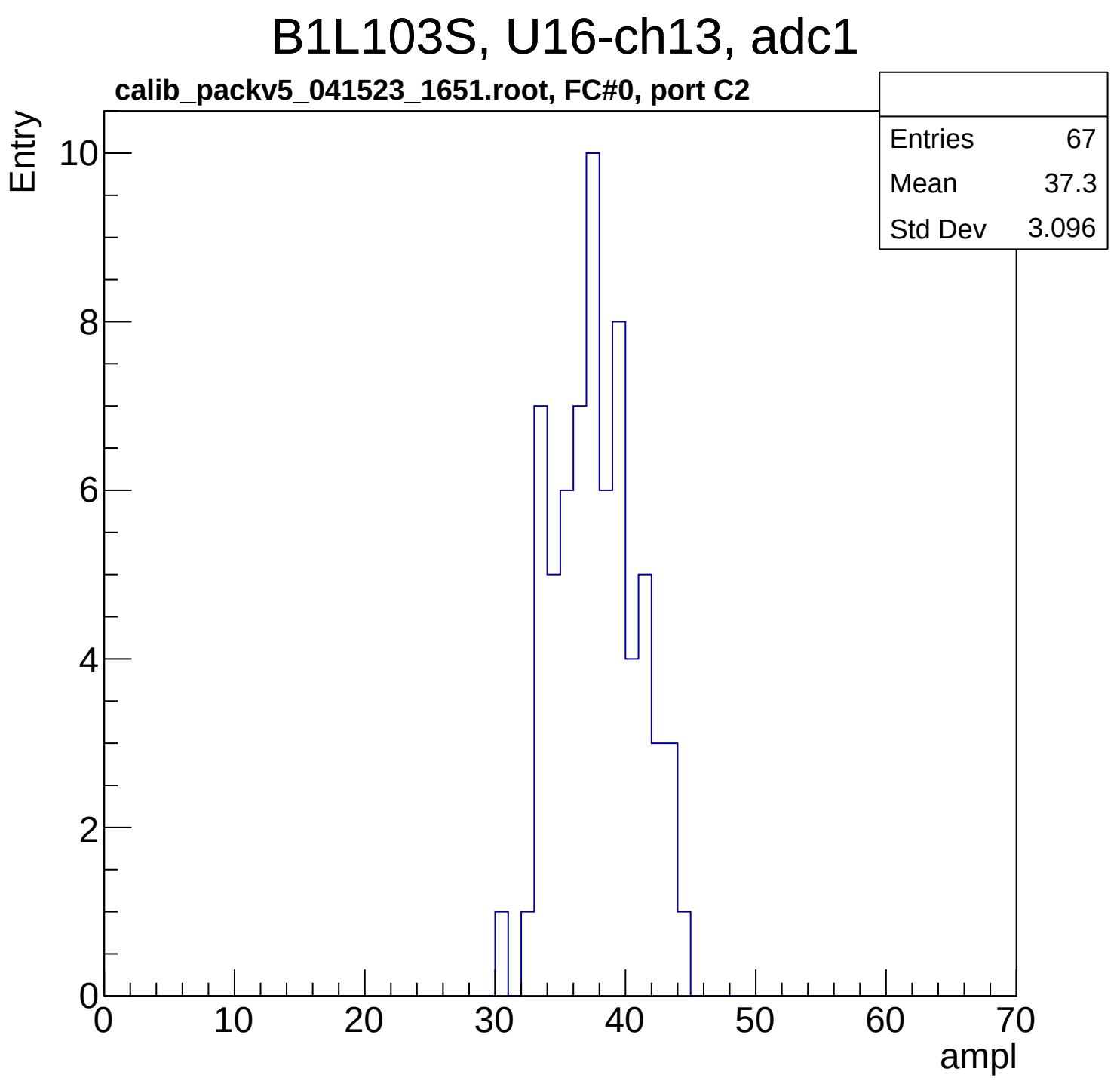

B1L103S, U16-ch12, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.71
Std Dev 3.168
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

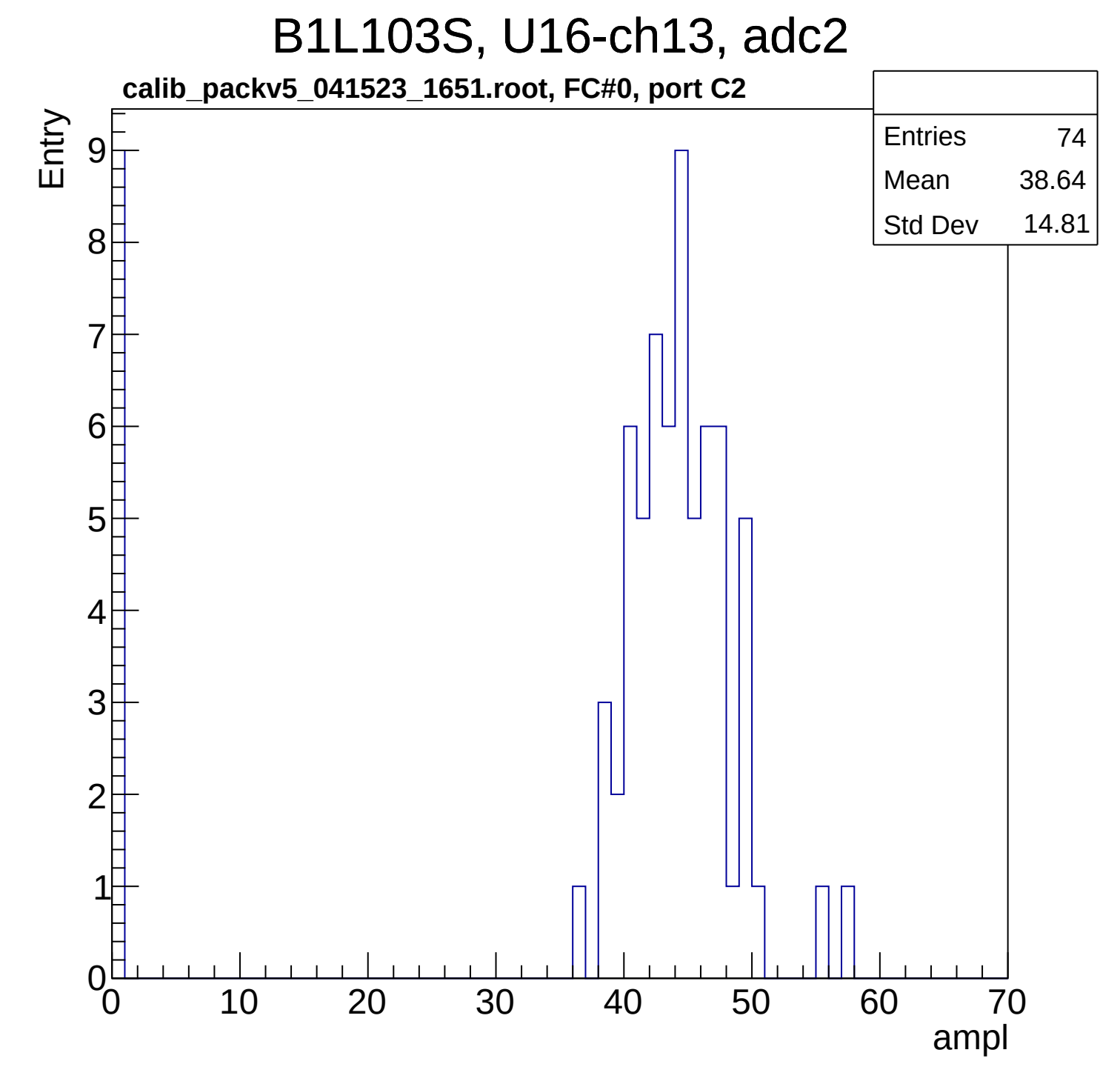

B1L103S, U16-ch12, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 59.48
Std Dev 2.313
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

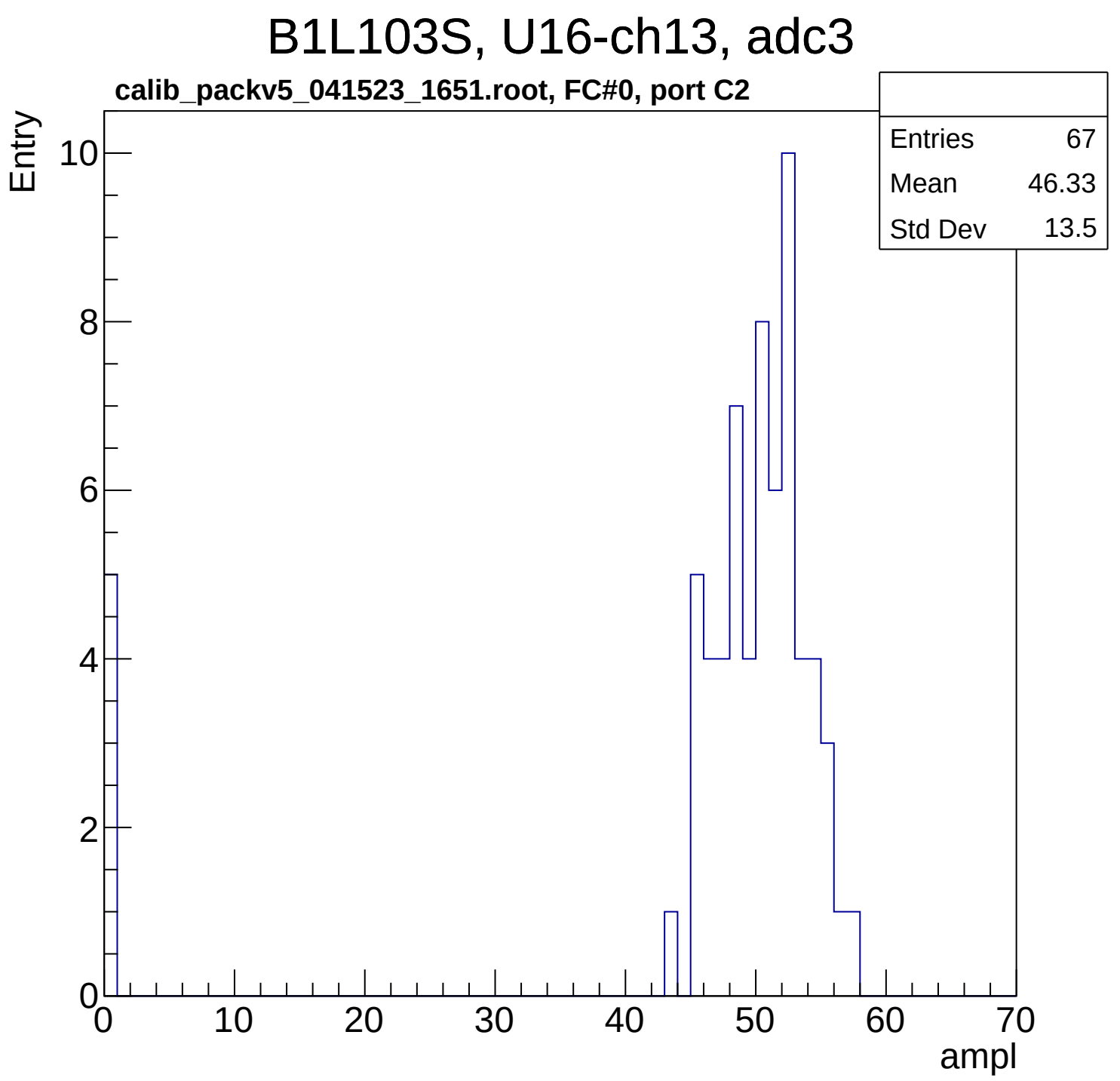

B1L103S, U16-ch12, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 58
Std Dev 15.03
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

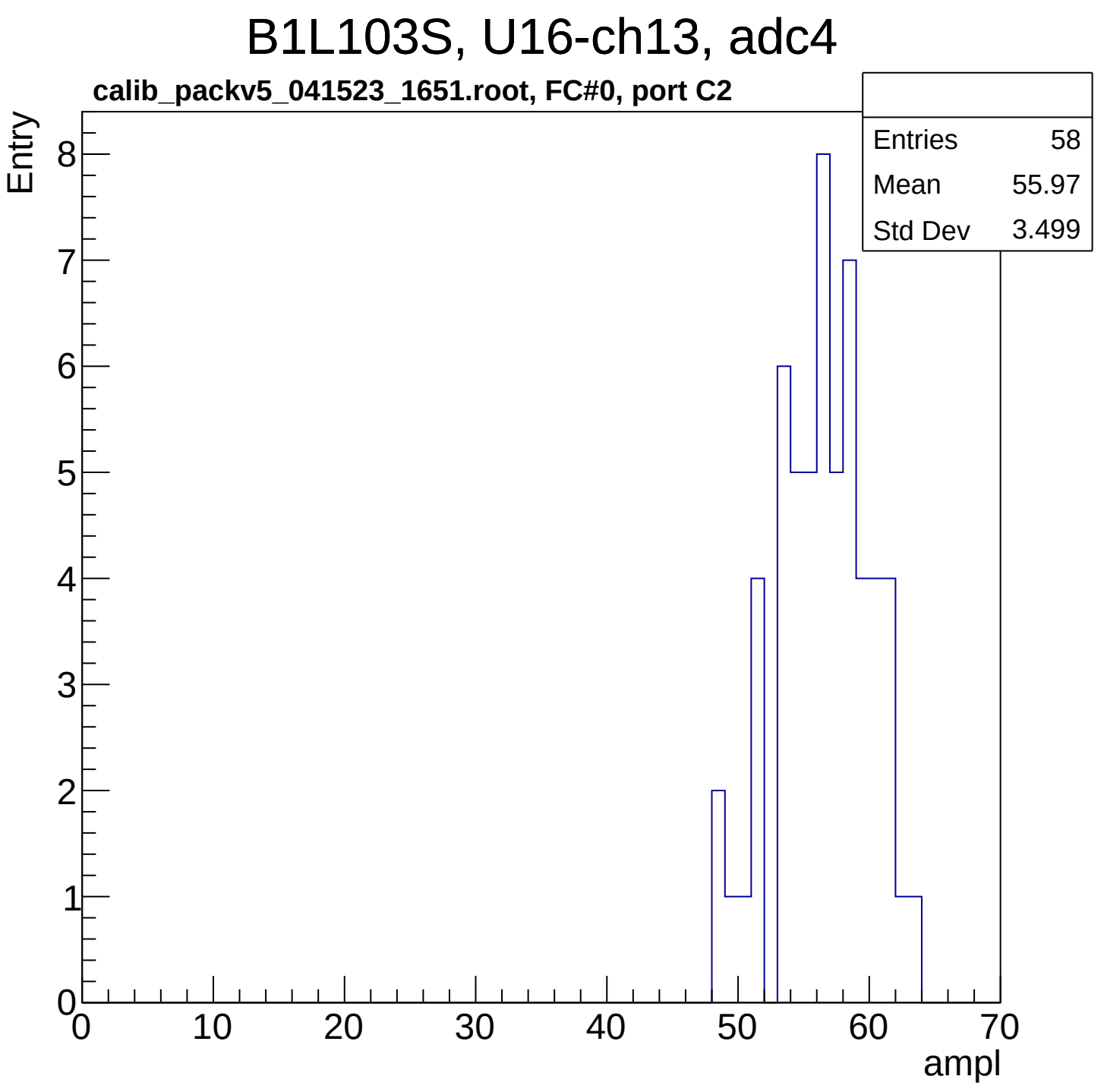

B1L103S, U16-ch12, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

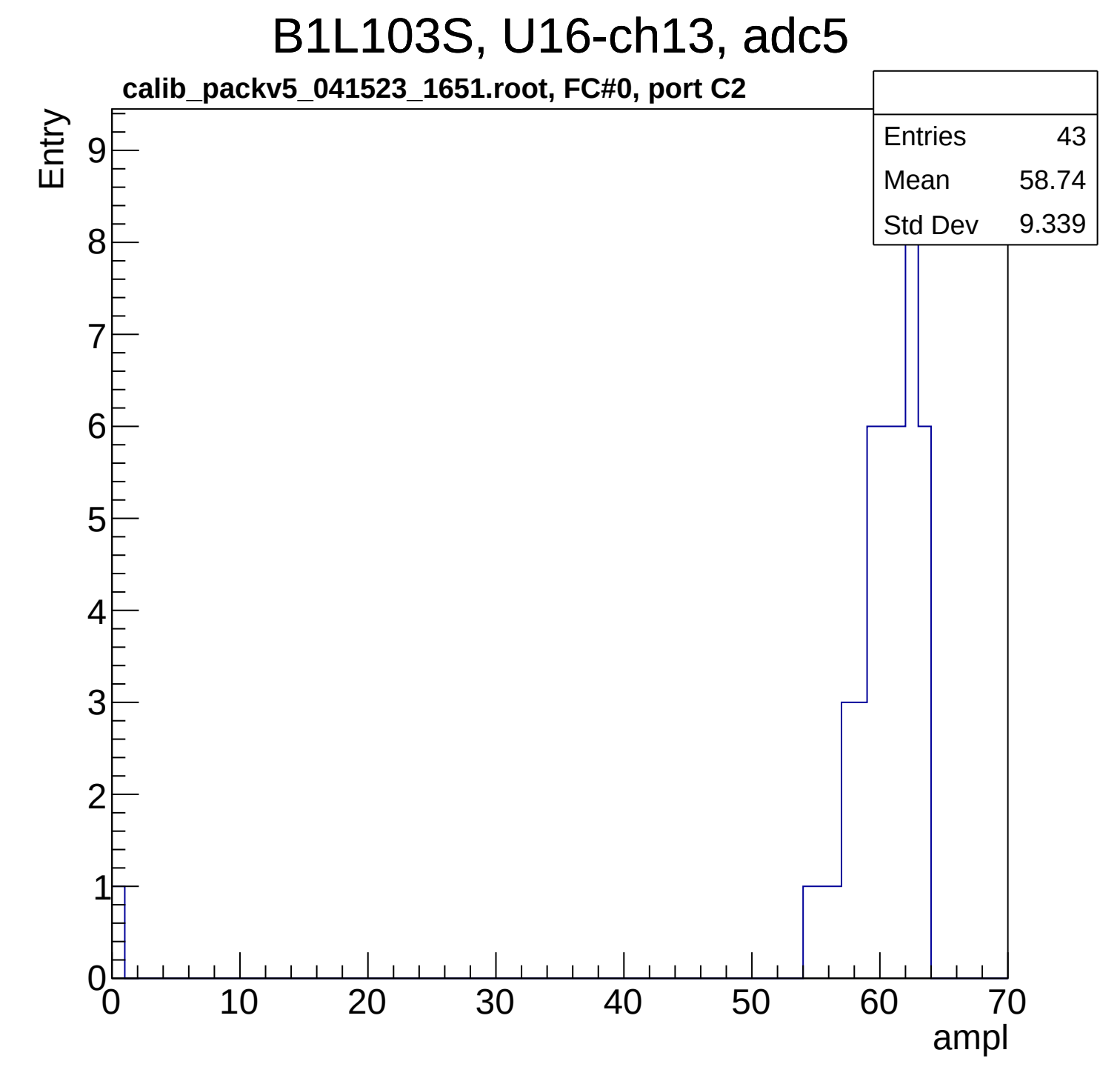

B1L103S, U16-ch13, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 28.63
Std Dev 7.512
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

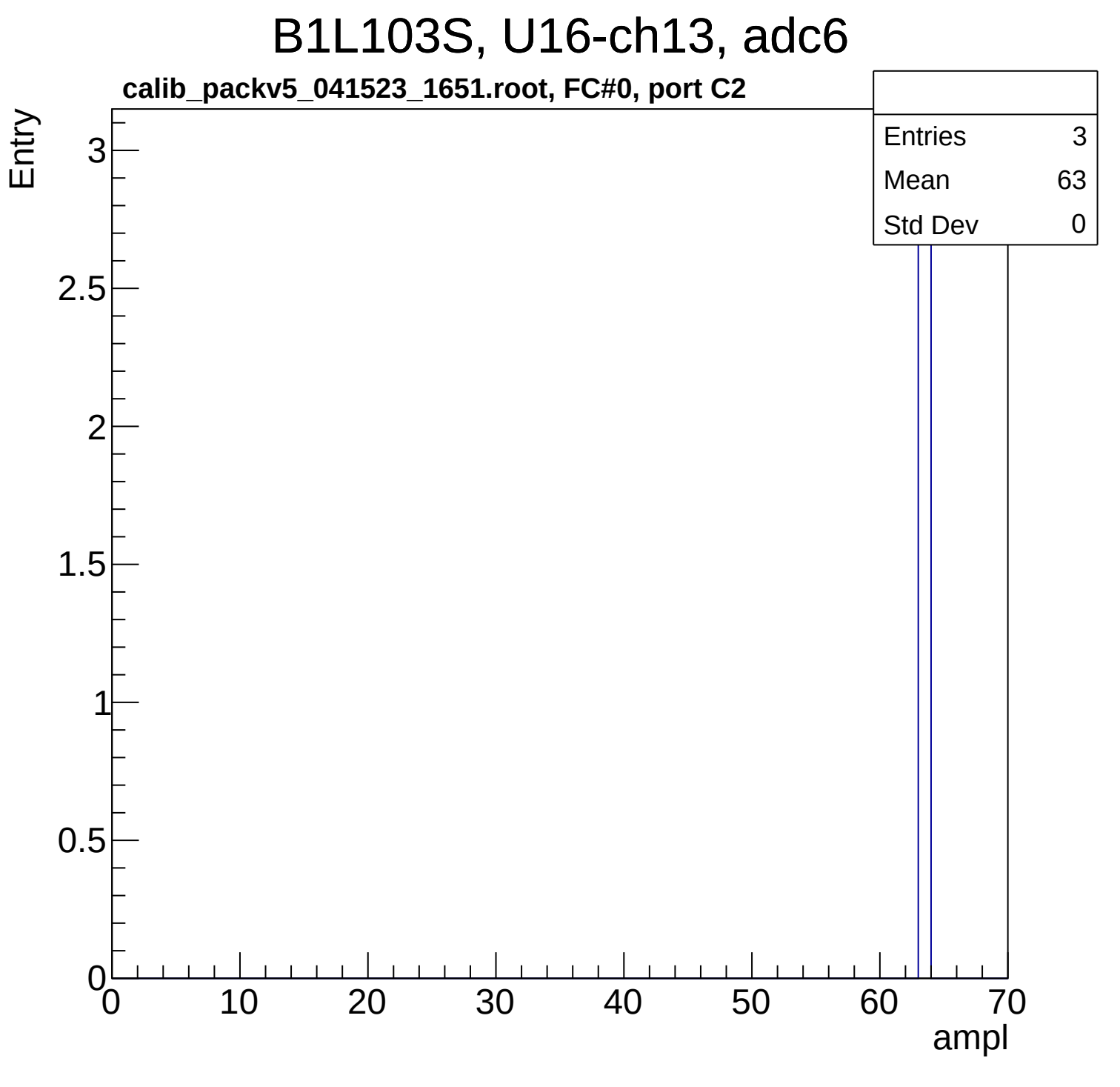

B1L103S, U16-ch13, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 37.3
Std Dev 3.096
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch13, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 38.64
Std Dev 14.81
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch13, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 46.33
Std Dev 13.5
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch13, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 55.97
Std Dev 3.499
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch13, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 58.74
Std Dev 9.339
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch13, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 63
Std Dev 0
Entry
ampl
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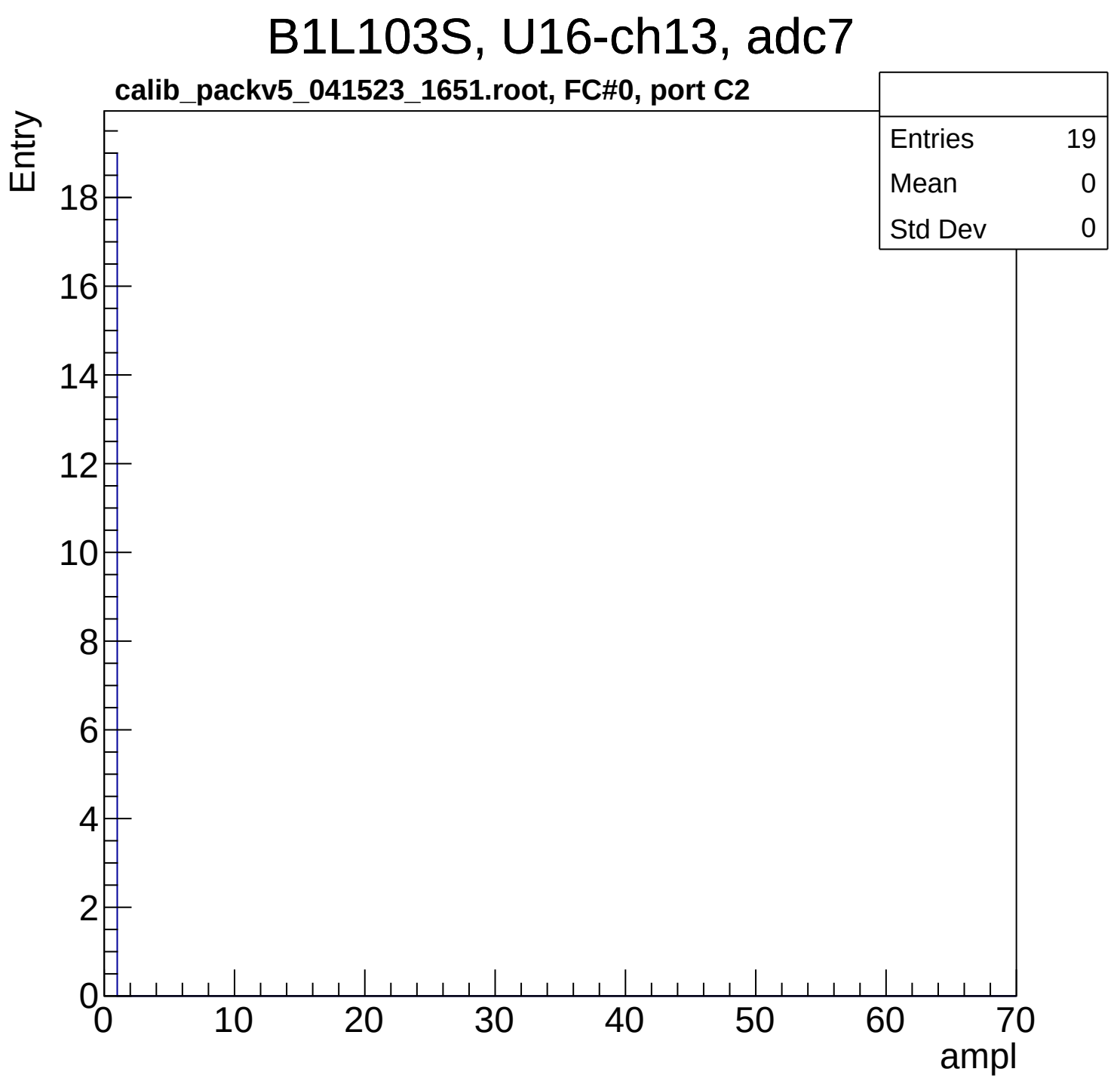
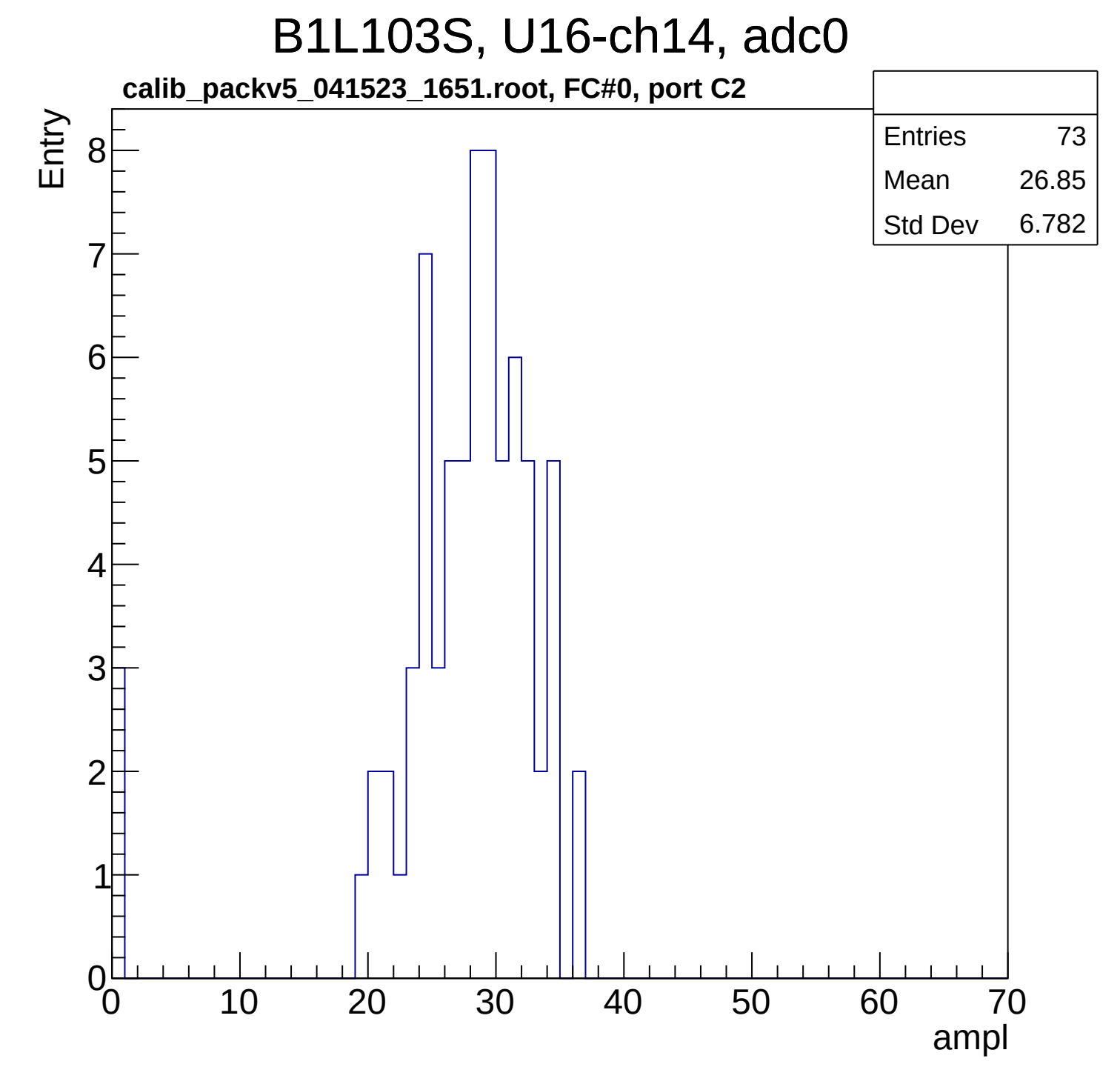
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U16-ch13, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch14, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 26.85
Std Dev 6.782
Entry
ampl
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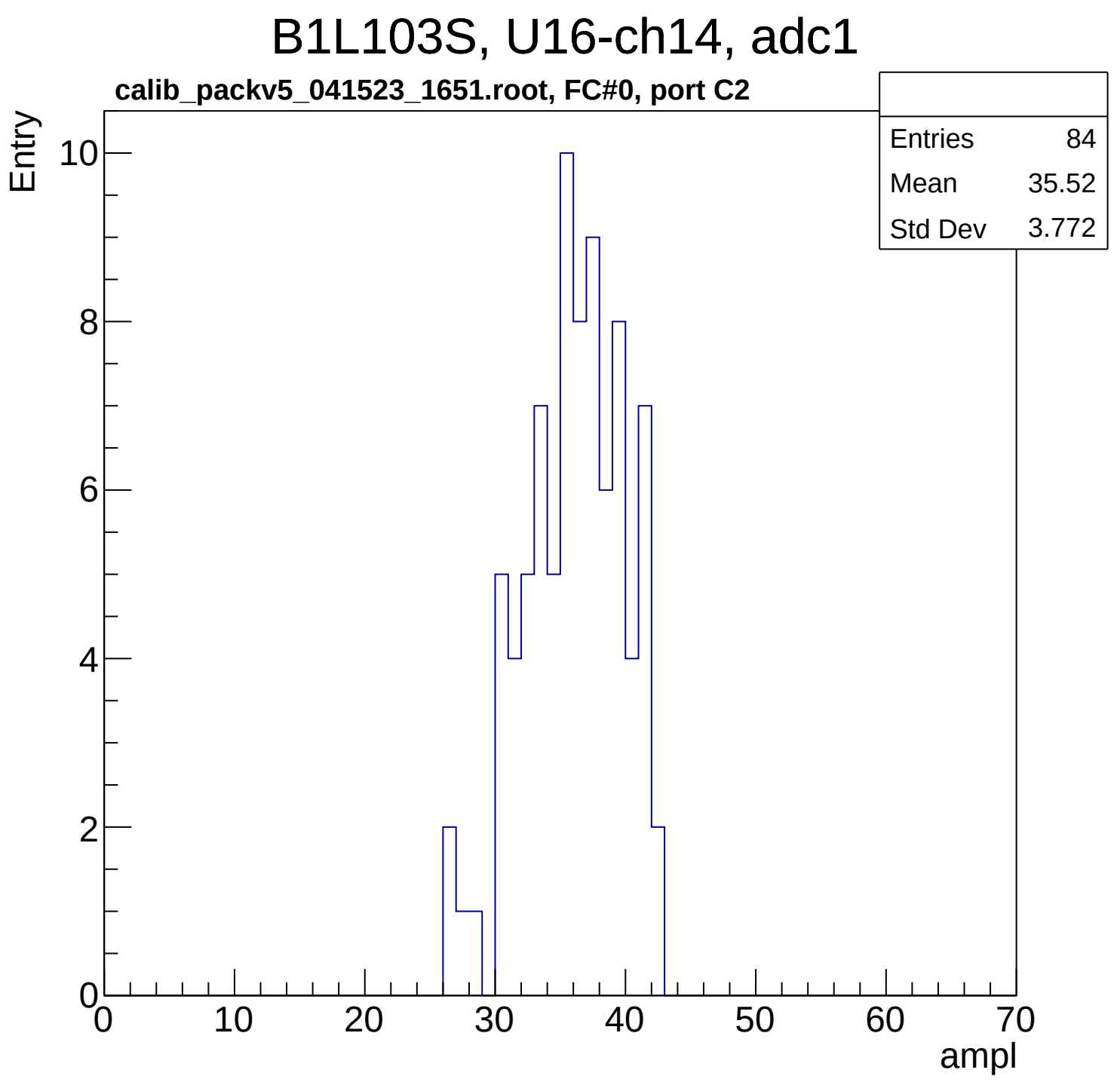
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch14, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 35.52
Std Dev 3.772
Entry
ampl
0
2
4
6
8
10
0
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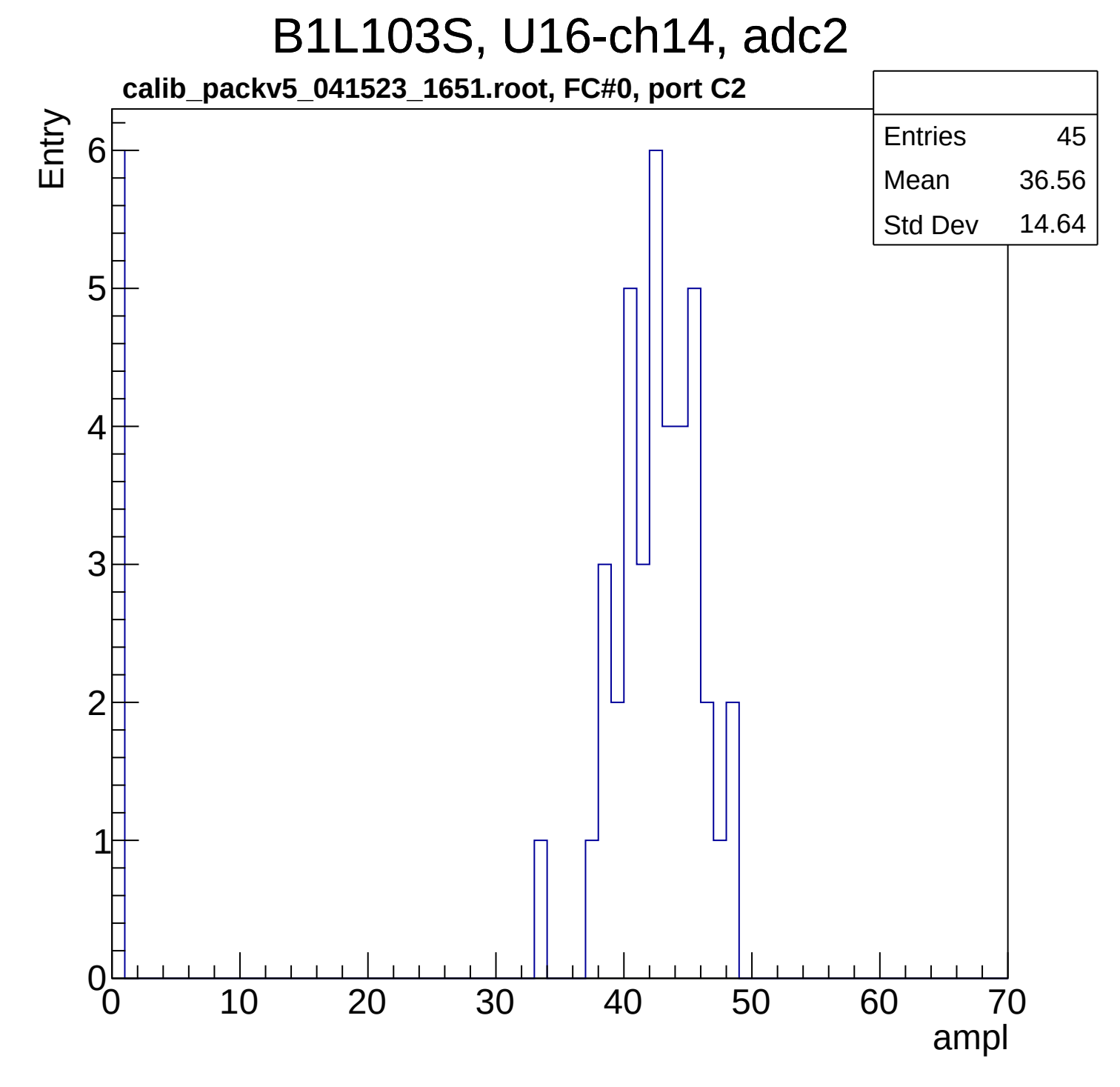
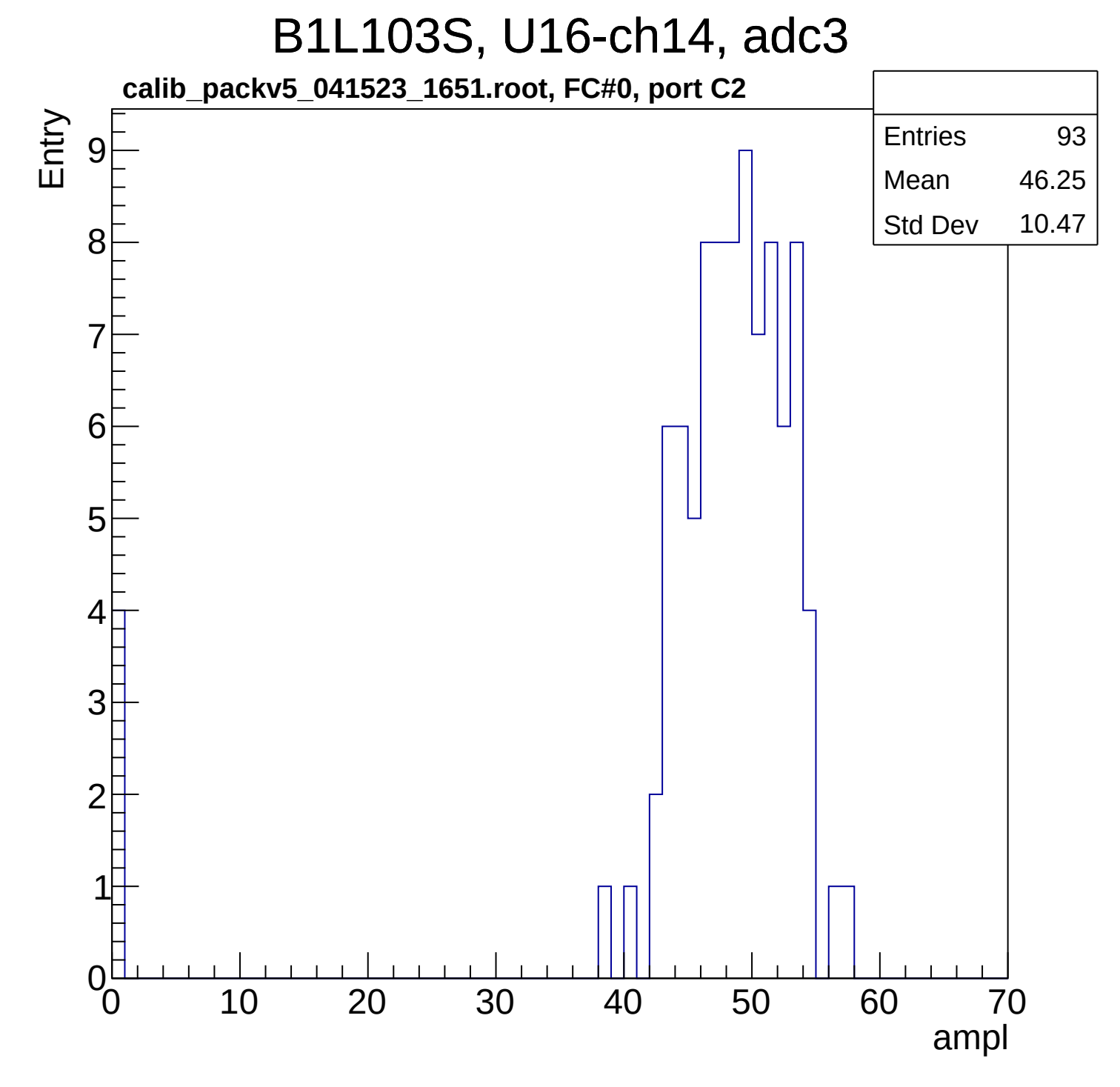
20
30
40
50
60
70


B1L103S, U16-ch14, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 36.56
Std Dev 14.64
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U16-ch14, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 46.25
Std Dev 10.47
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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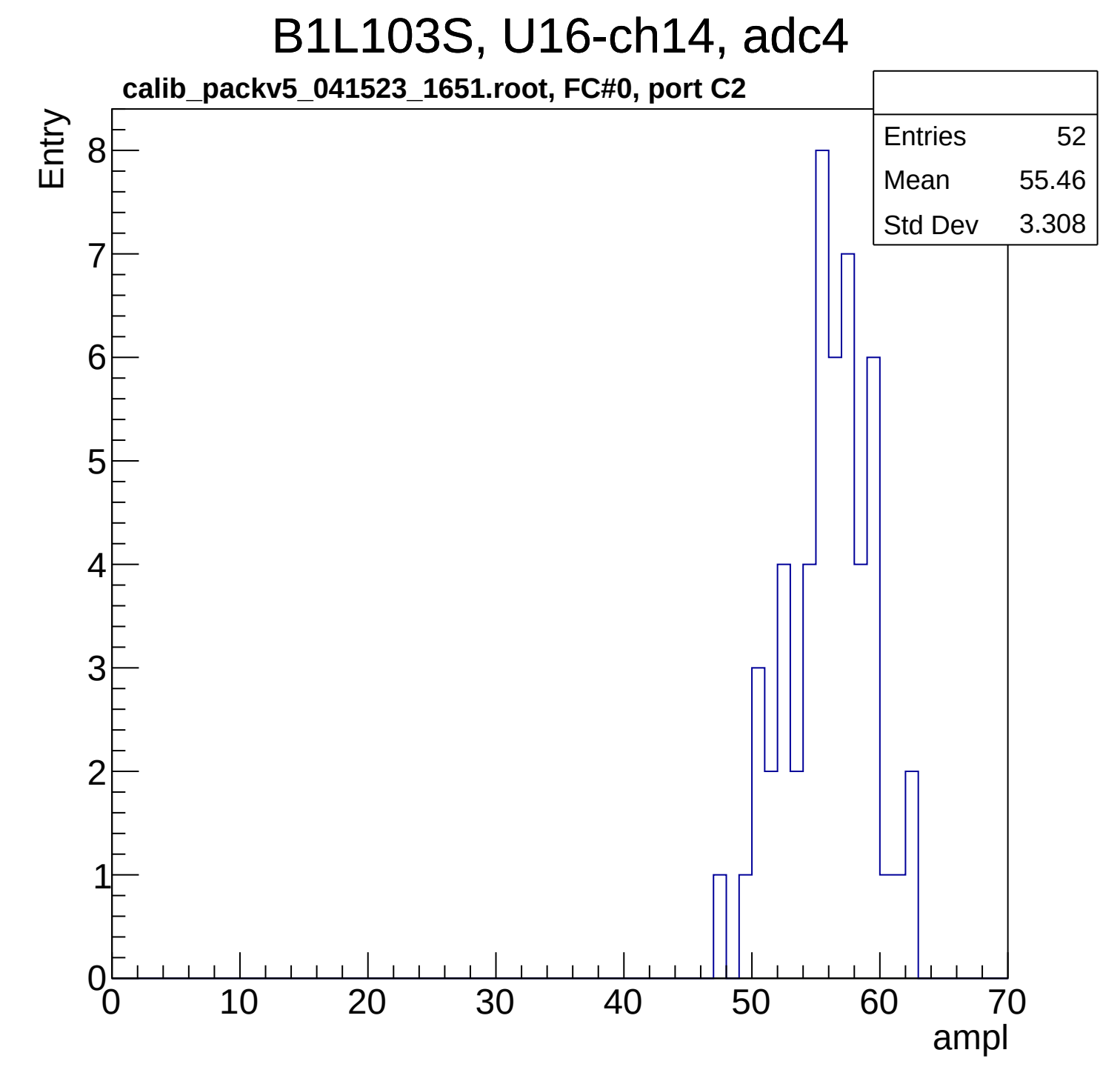
60
70


B1L103S, U16-ch14, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 55.46
Std Dev 3.308
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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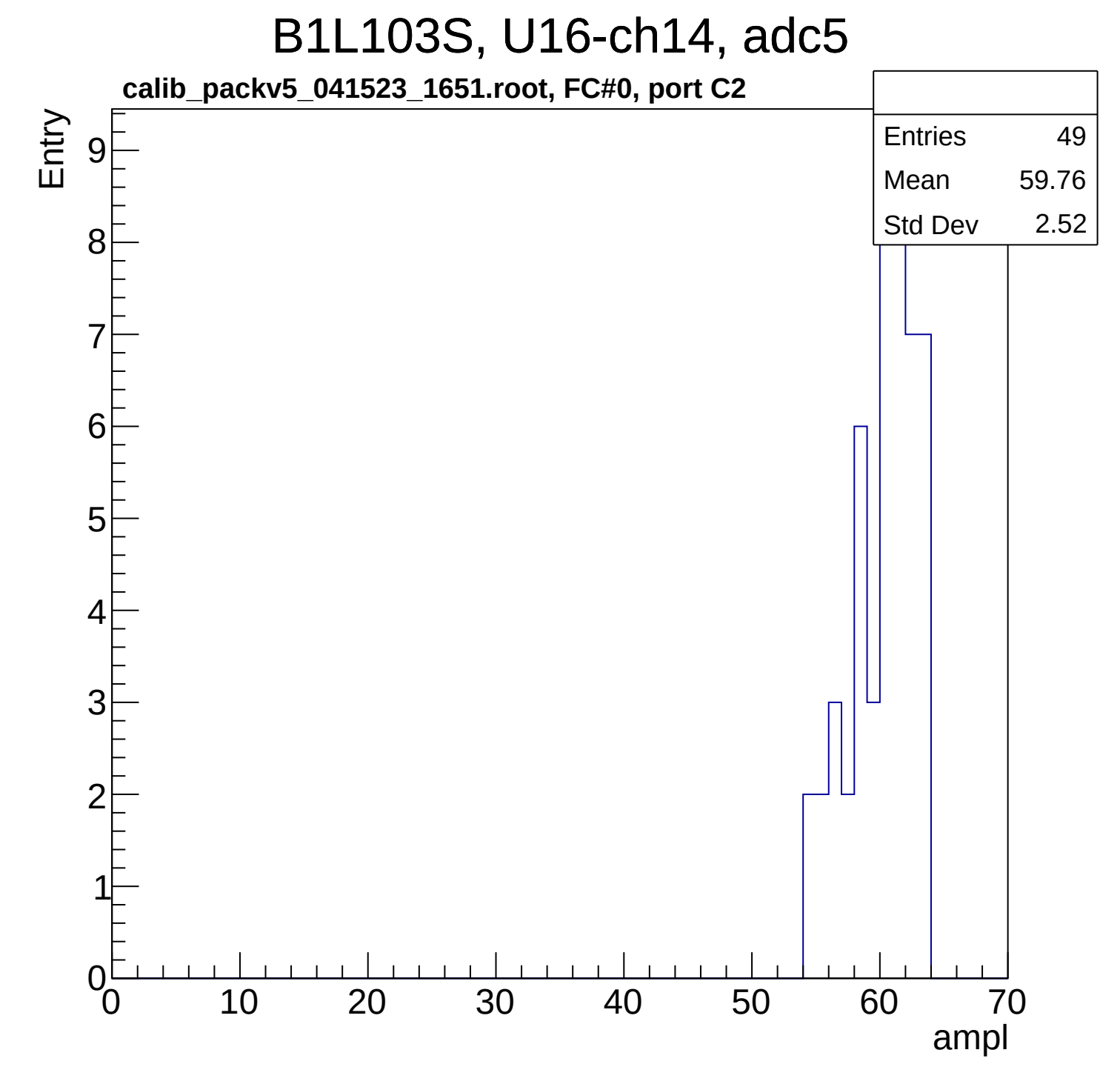
40
50
60
70


B1L103S, U16-ch14, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 59.76
Std Dev 2.52
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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40
50
60
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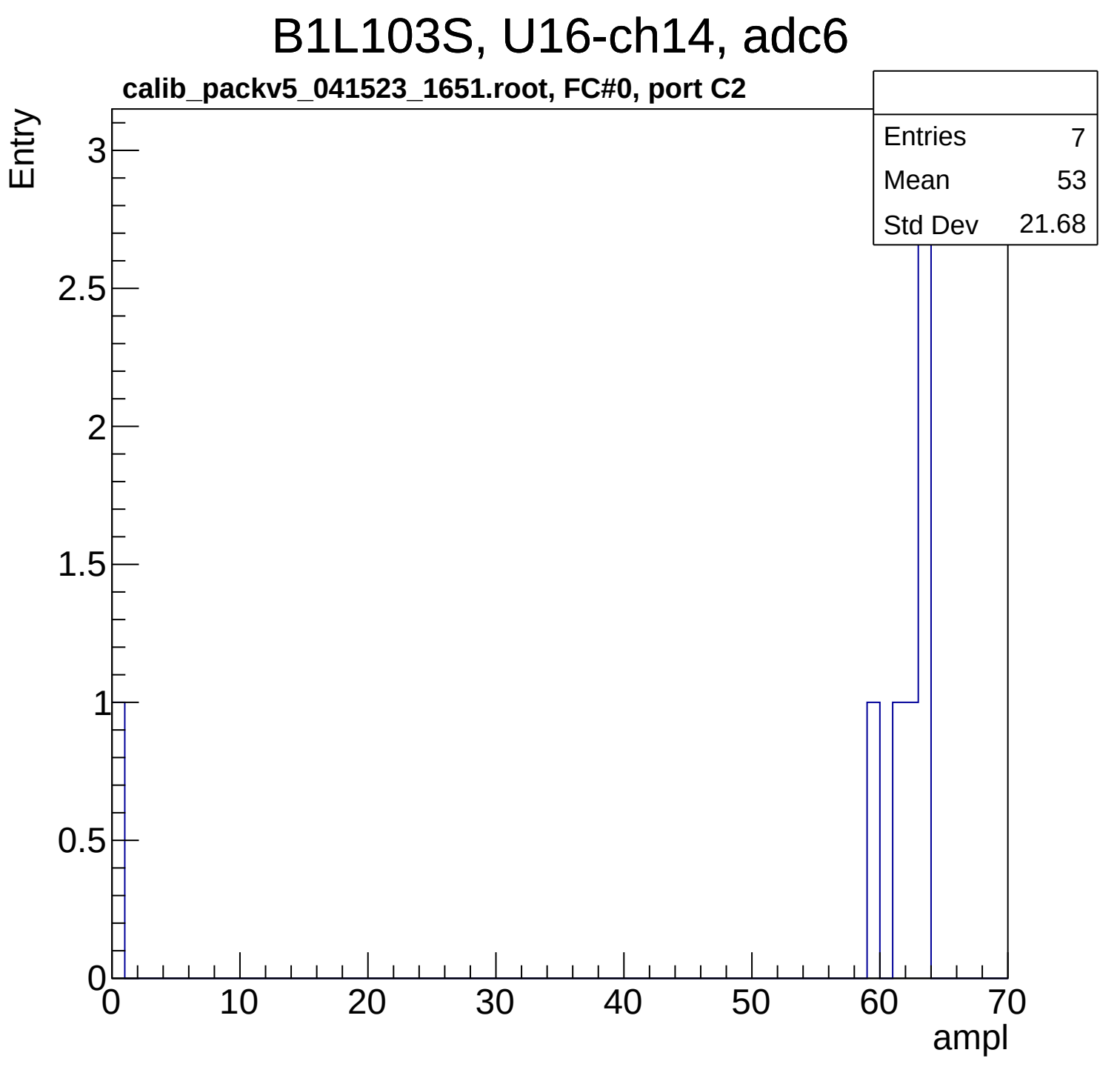
B1L103S, U16-ch14, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 53
Std Dev 21.68
Entry
ampl
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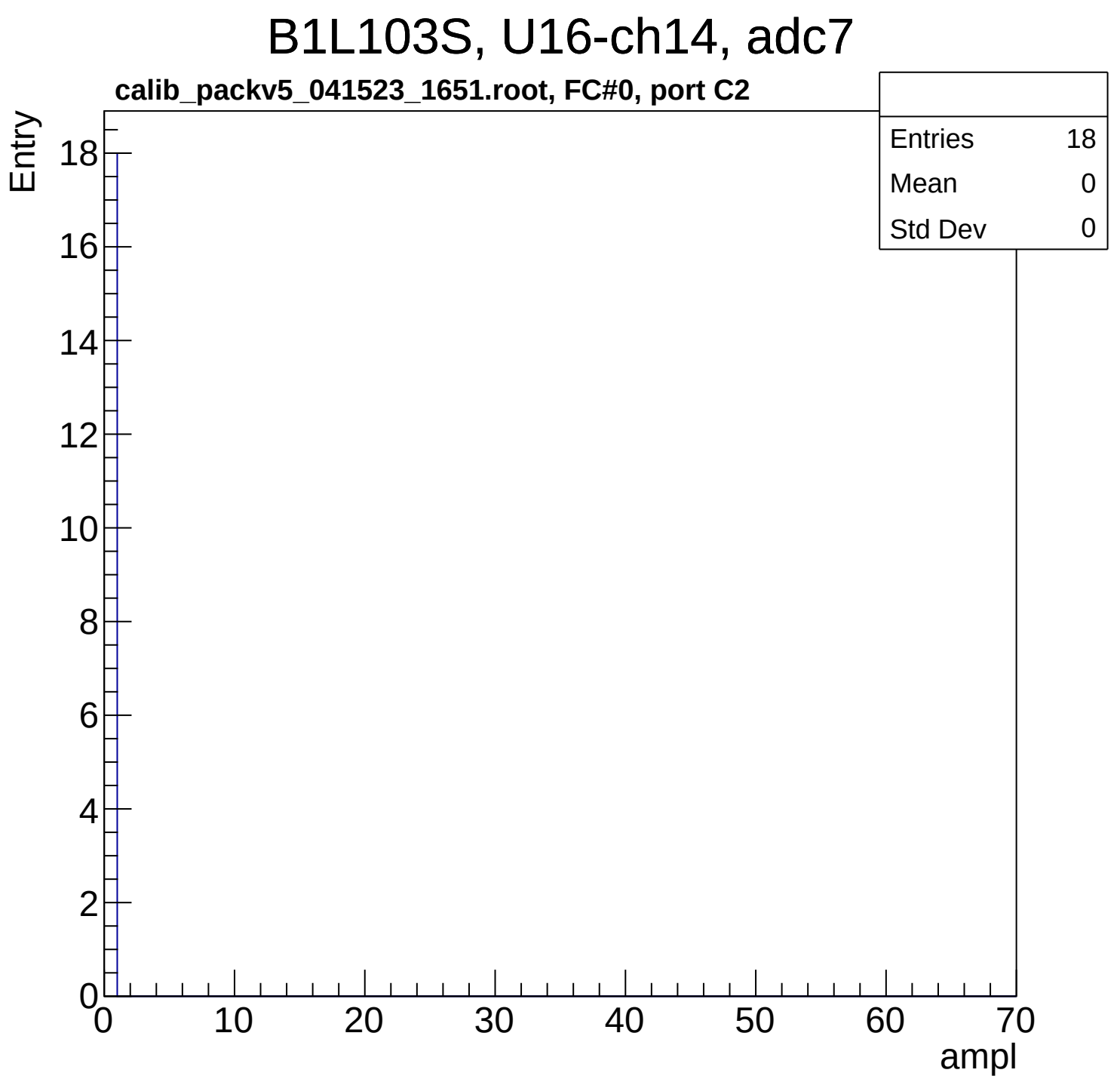
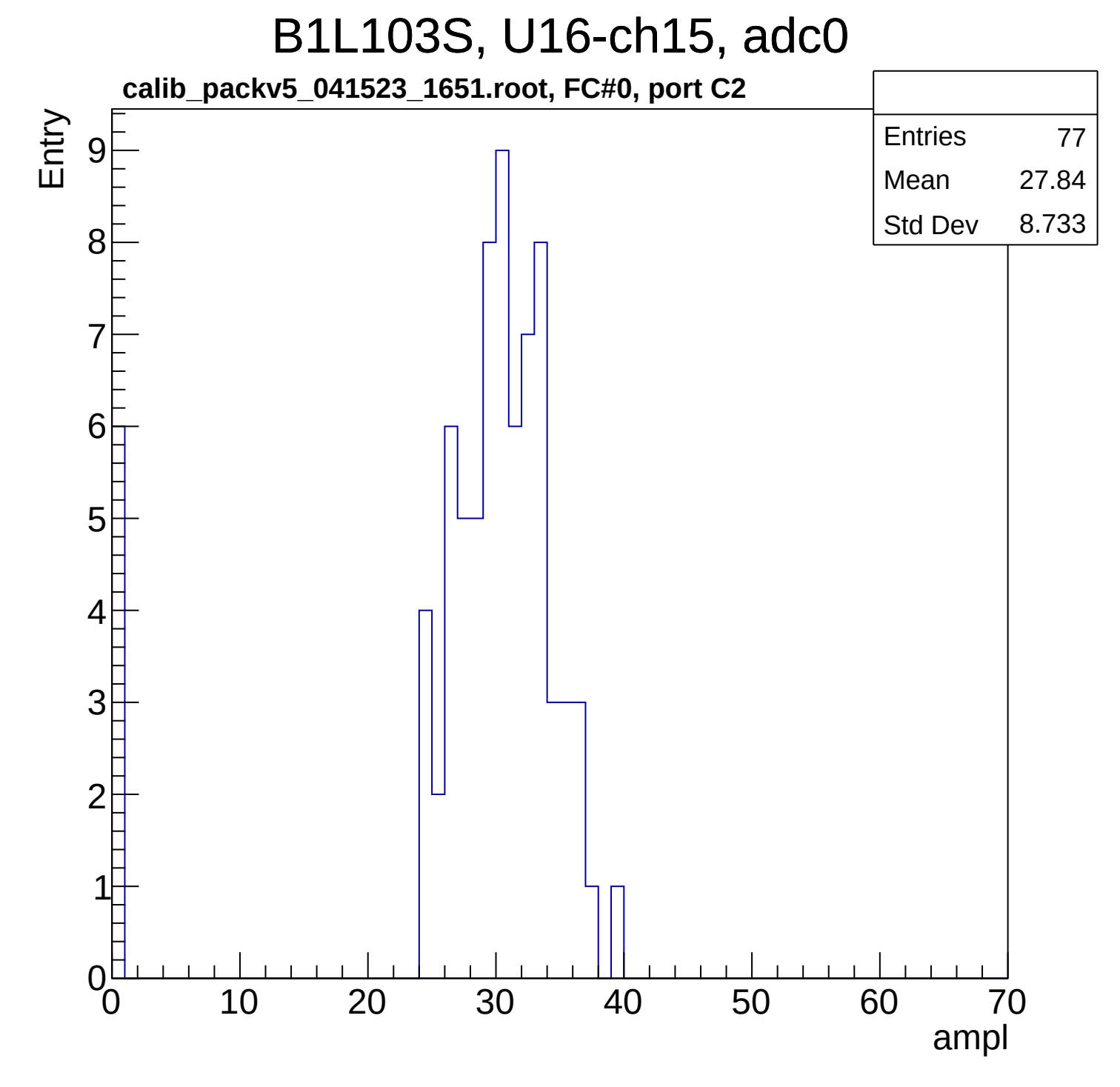
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U16-ch14, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch15, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 27.84
Std Dev 8.733
Entry
ampl
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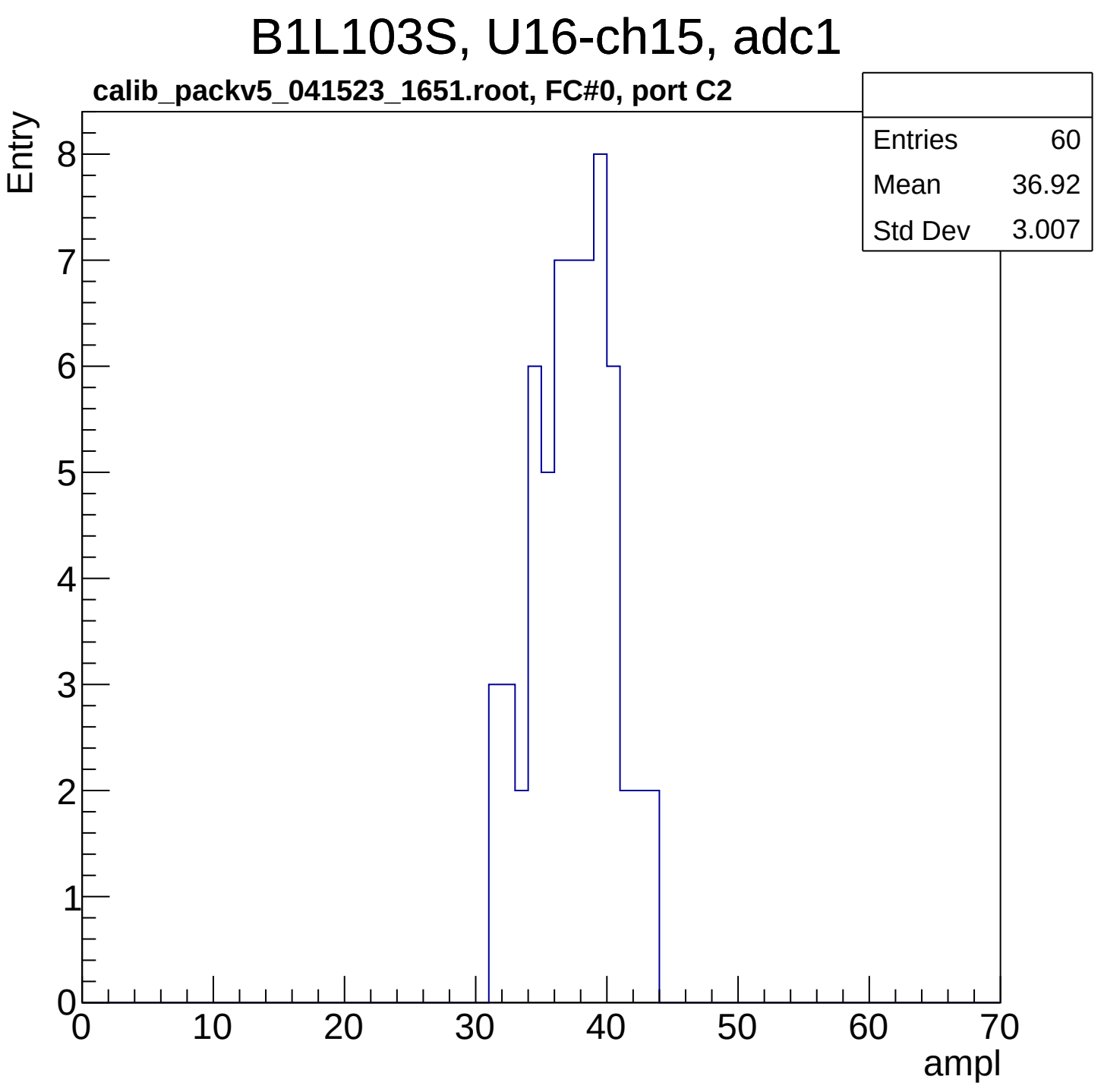
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch15, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 36.92
Std Dev 3.007
Entry
ampl
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2
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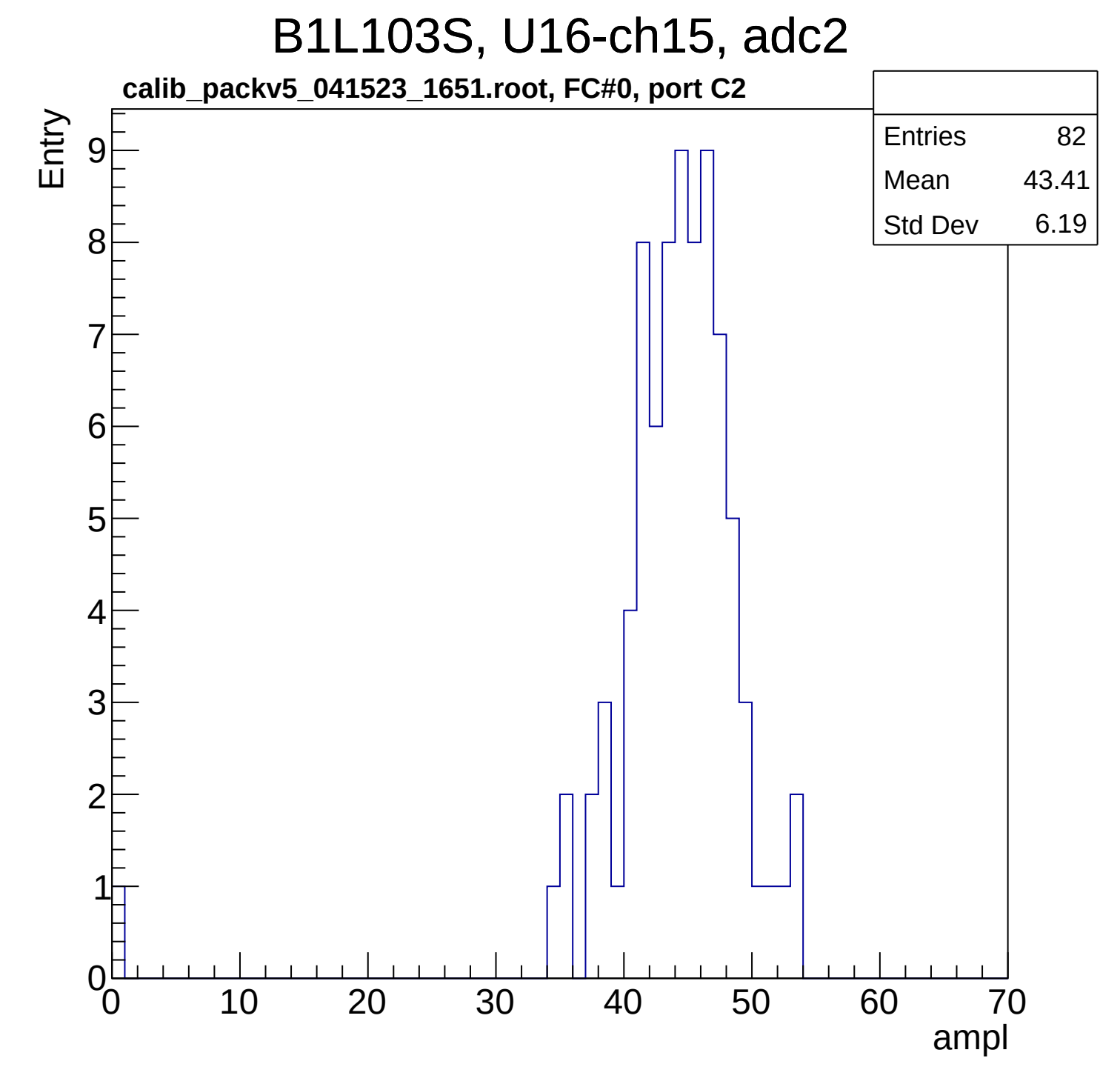
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch15, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 43.41
Std Dev 6.19
Entry
ampl
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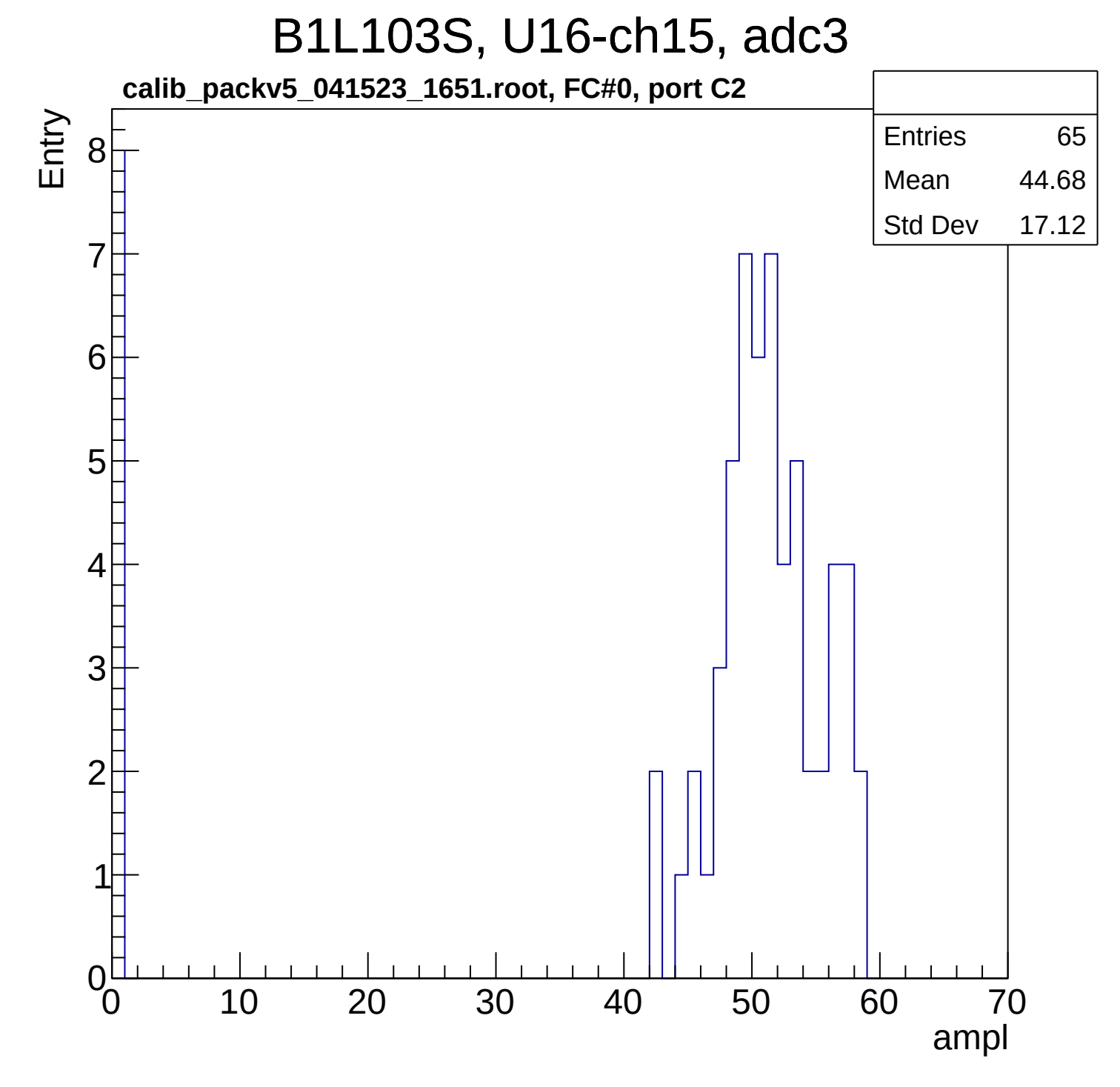
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch15, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 44.68
Std Dev 17.12
Entry
ampl
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1
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3
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5
6
7
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0
10
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40
50
60
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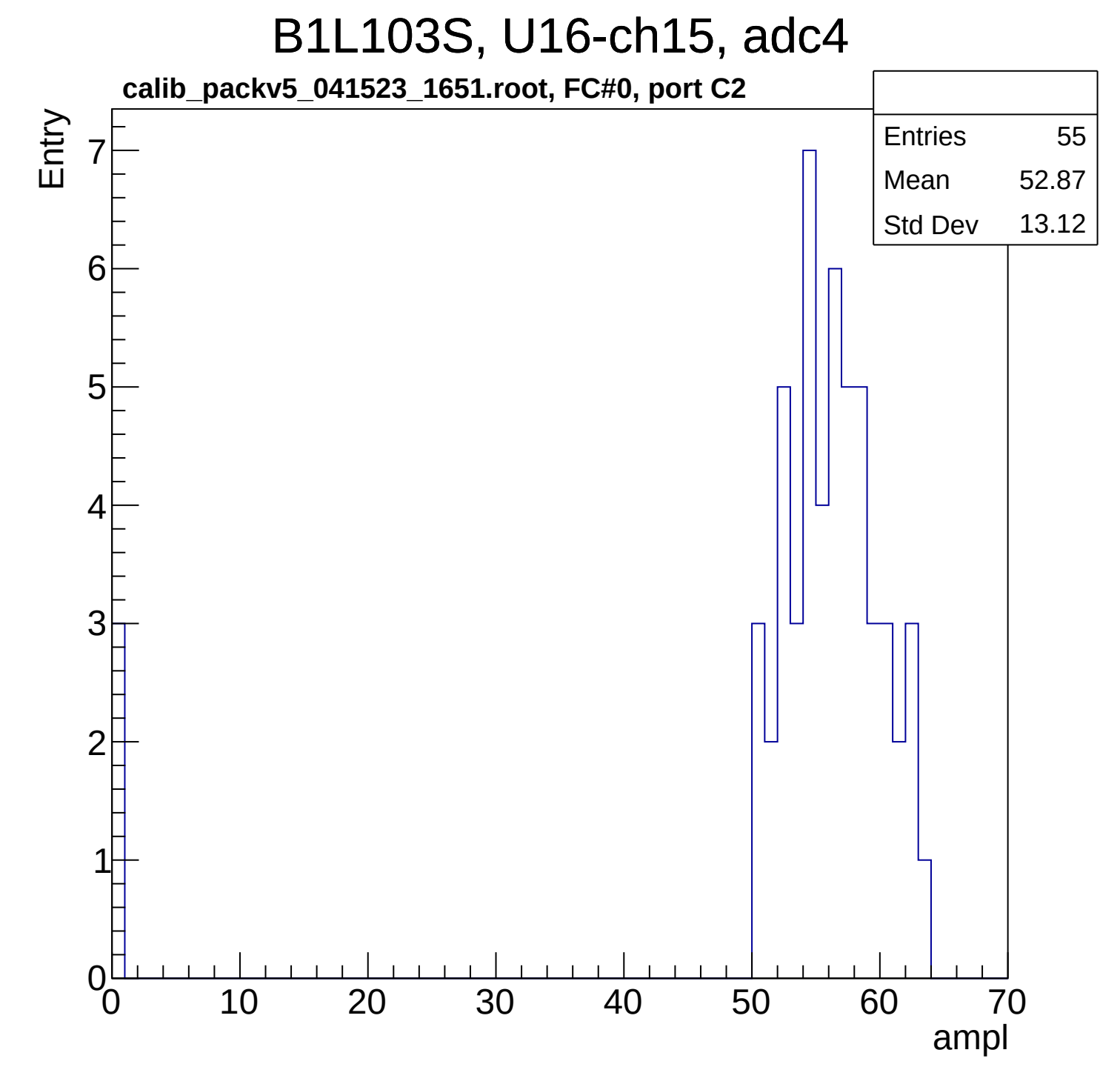
B1L103S, U16-ch15, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 52.87
Std Dev 13.12
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
30
40
50
60
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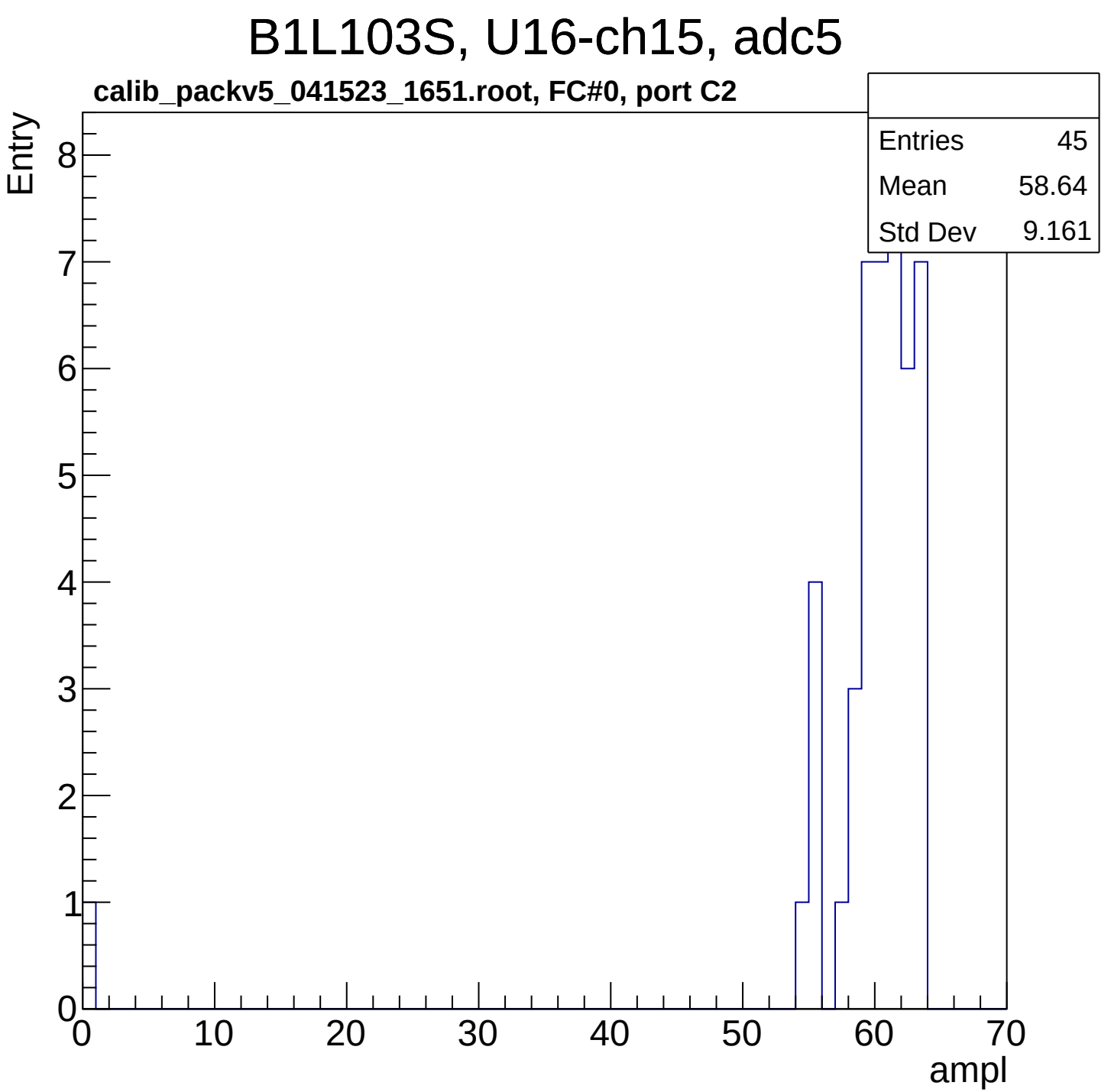
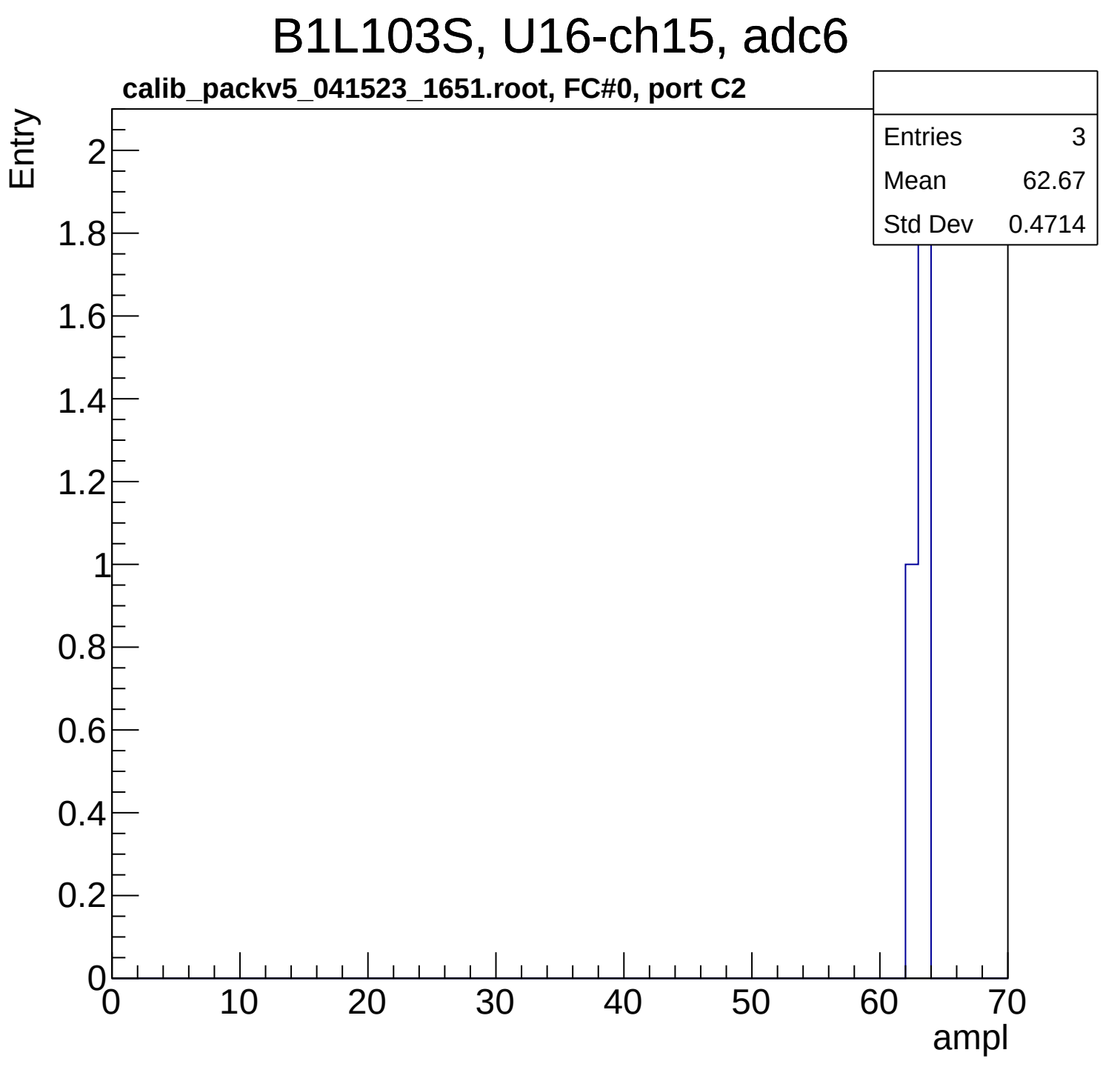
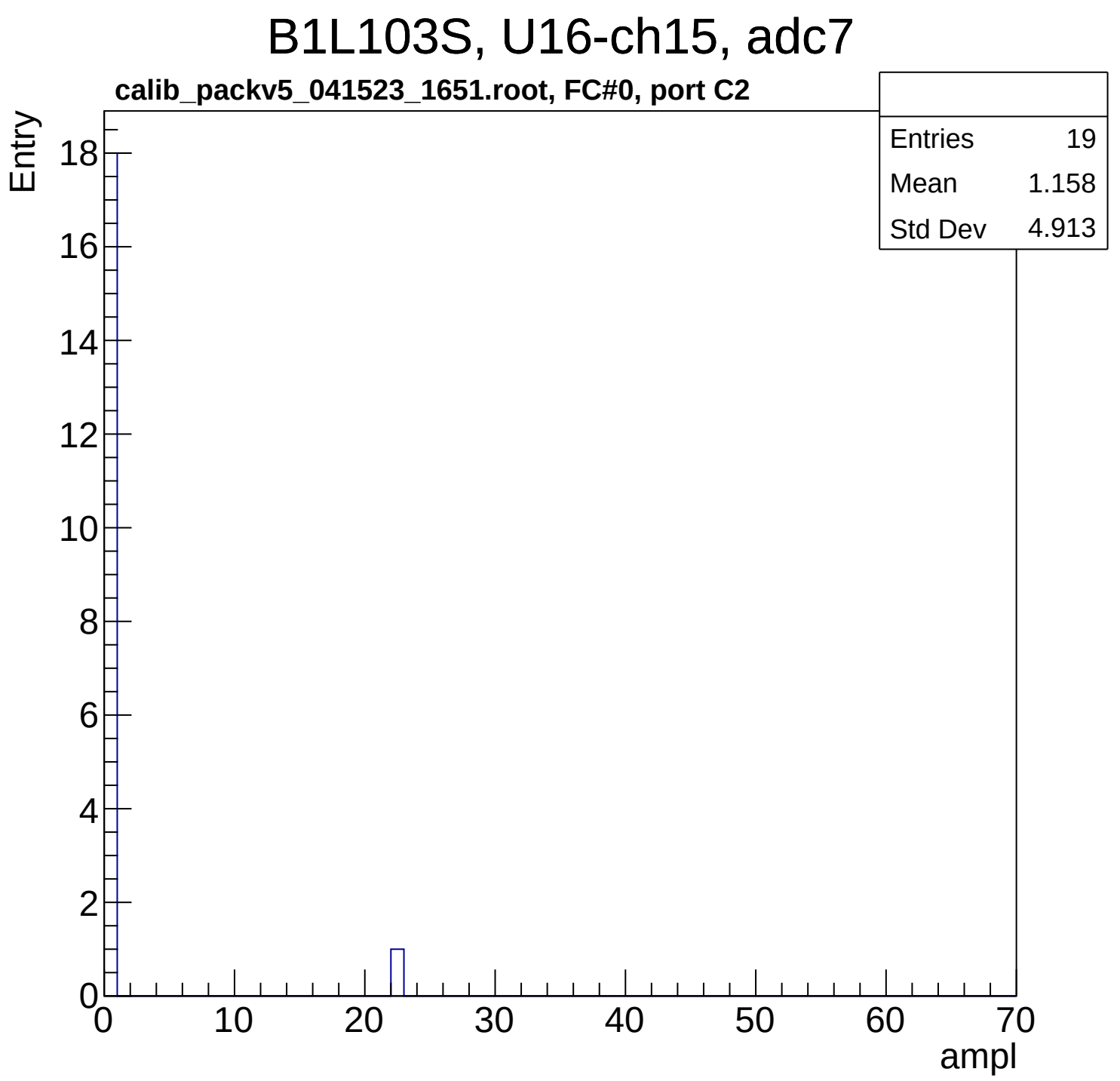
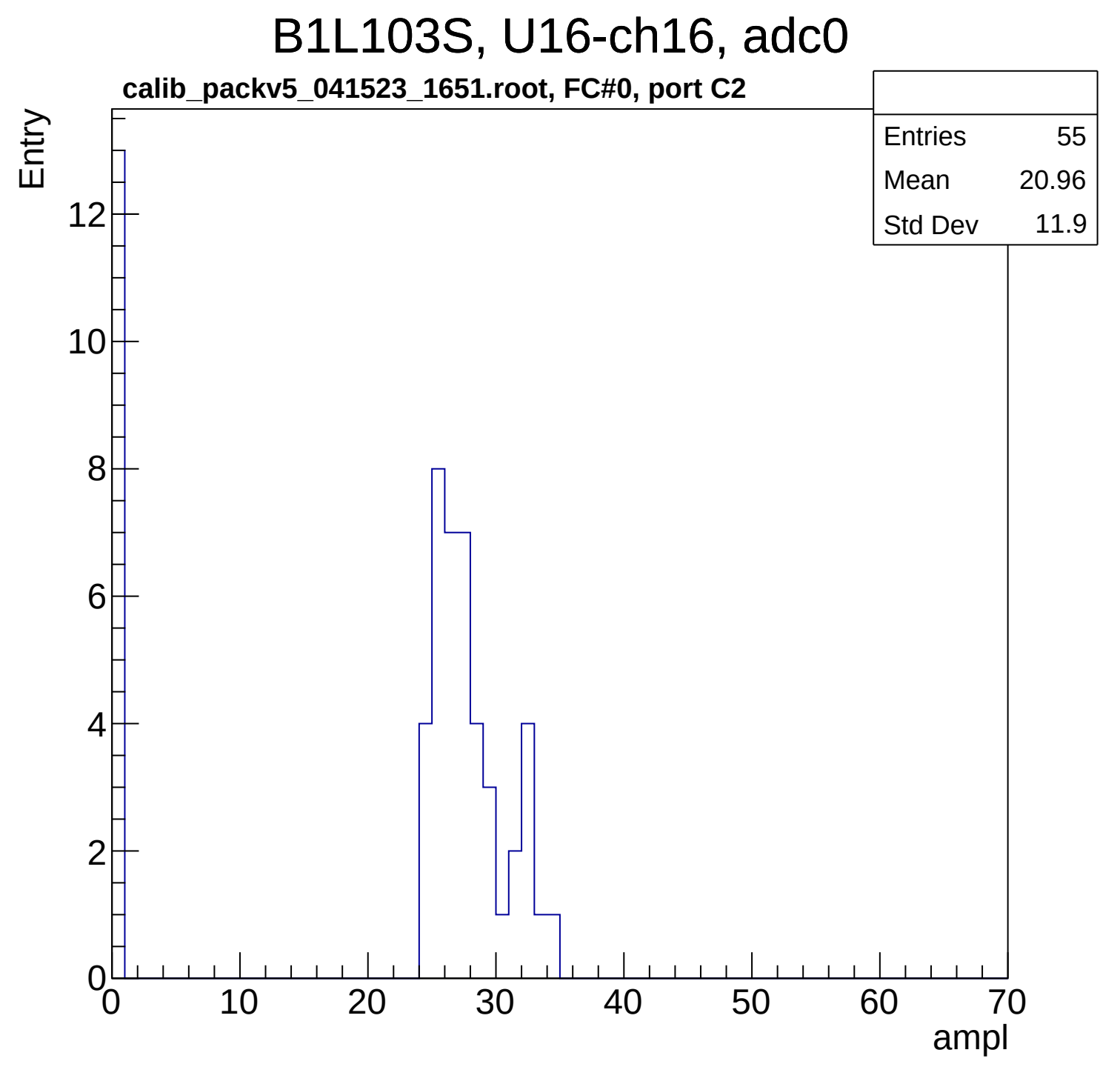

B1L103S, U16-ch15, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.64
Std Dev 9.161
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch15, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U16-ch15, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch16, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 20.96
Std Dev 11.9
Entry
0
2
4
6
8
10
12
0
10
20
30
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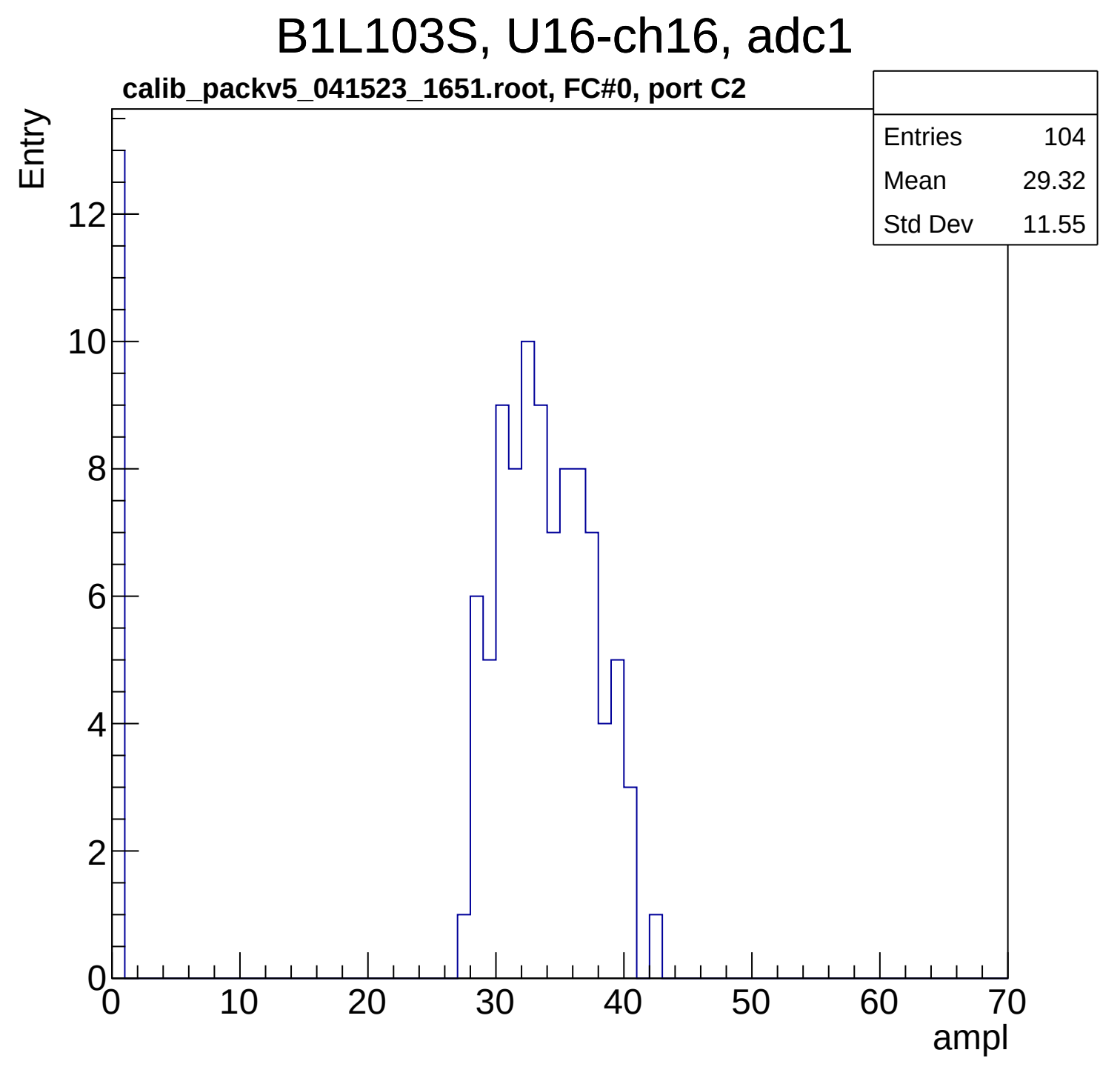
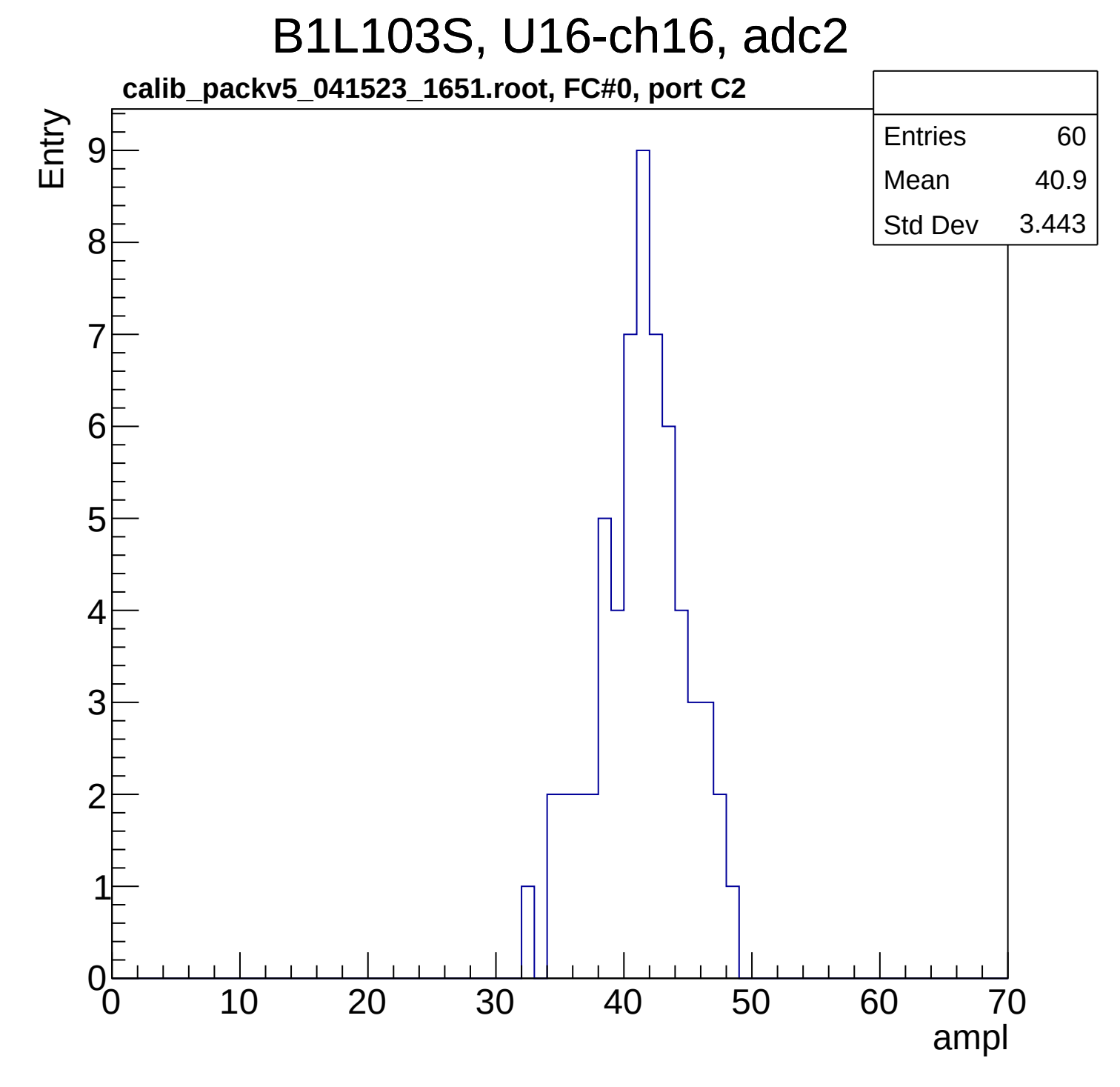
50
60
70
ampl


B1L103S, U16-ch16, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 29.32
Std Dev 11.55
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch16, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 40.9
Std Dev 3.443
Entry
ampl
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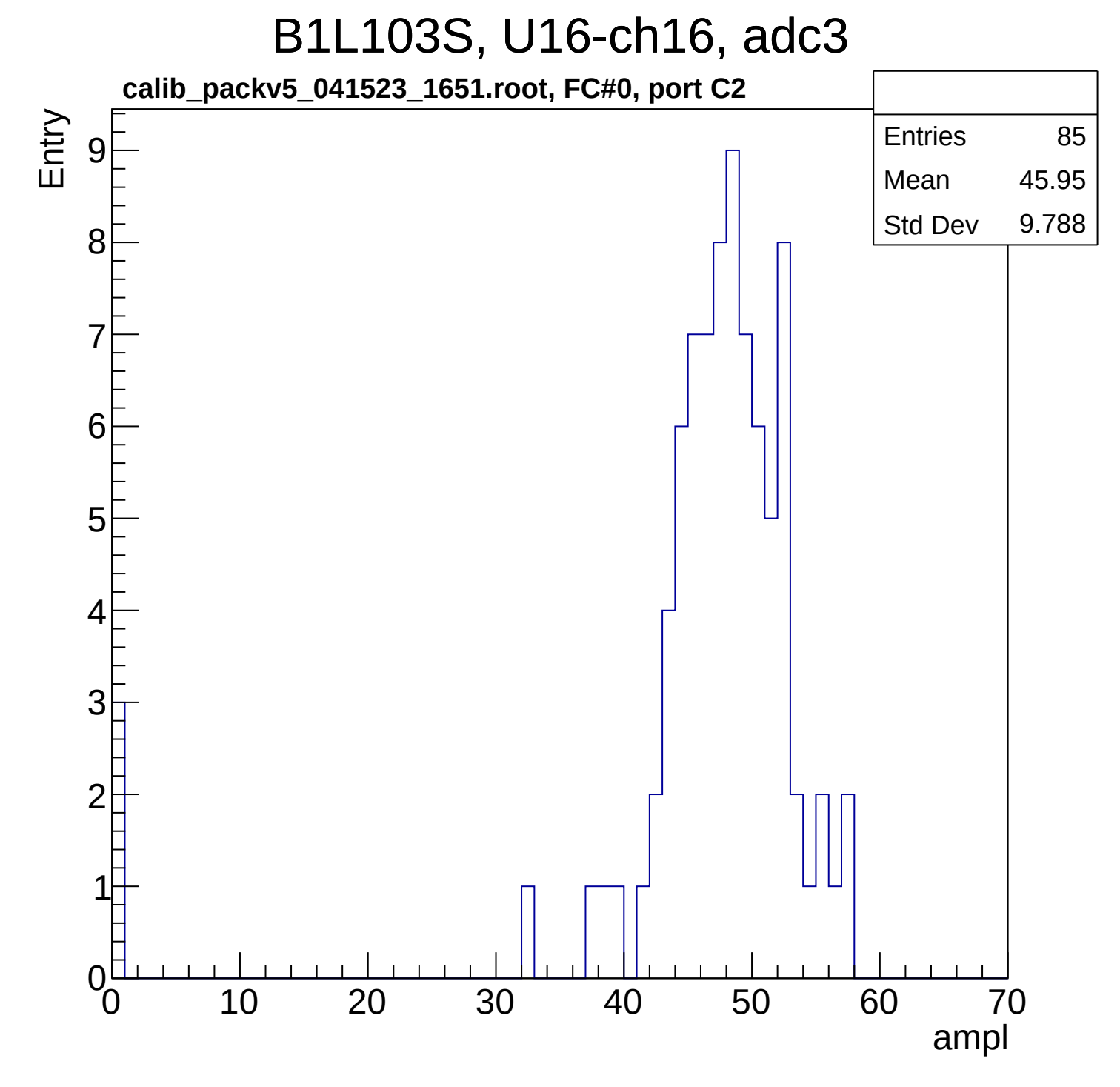
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch16, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 45.95
Std Dev 9.788
Entry
ampl
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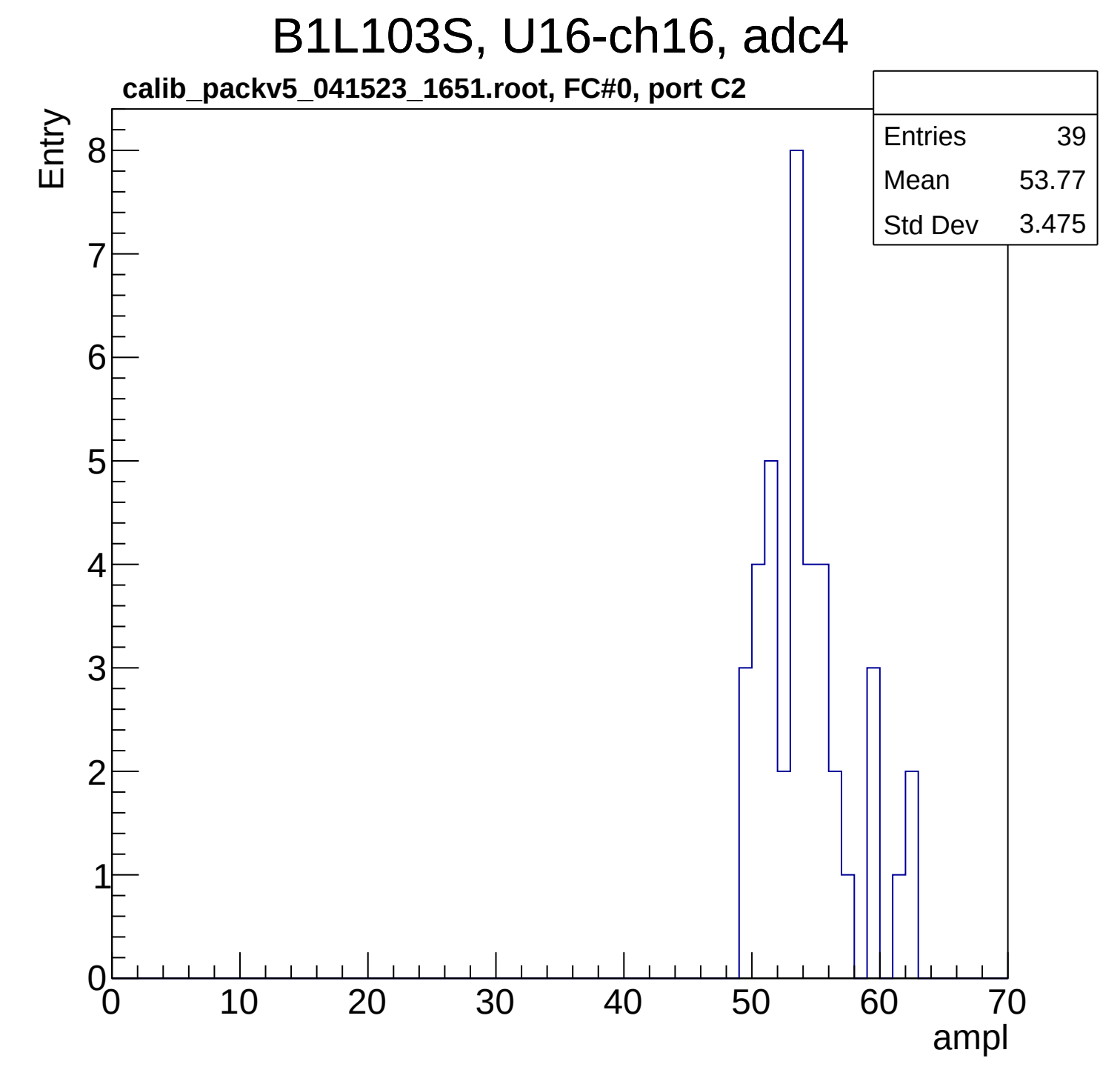
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch16, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 53.77
Std Dev 3.475
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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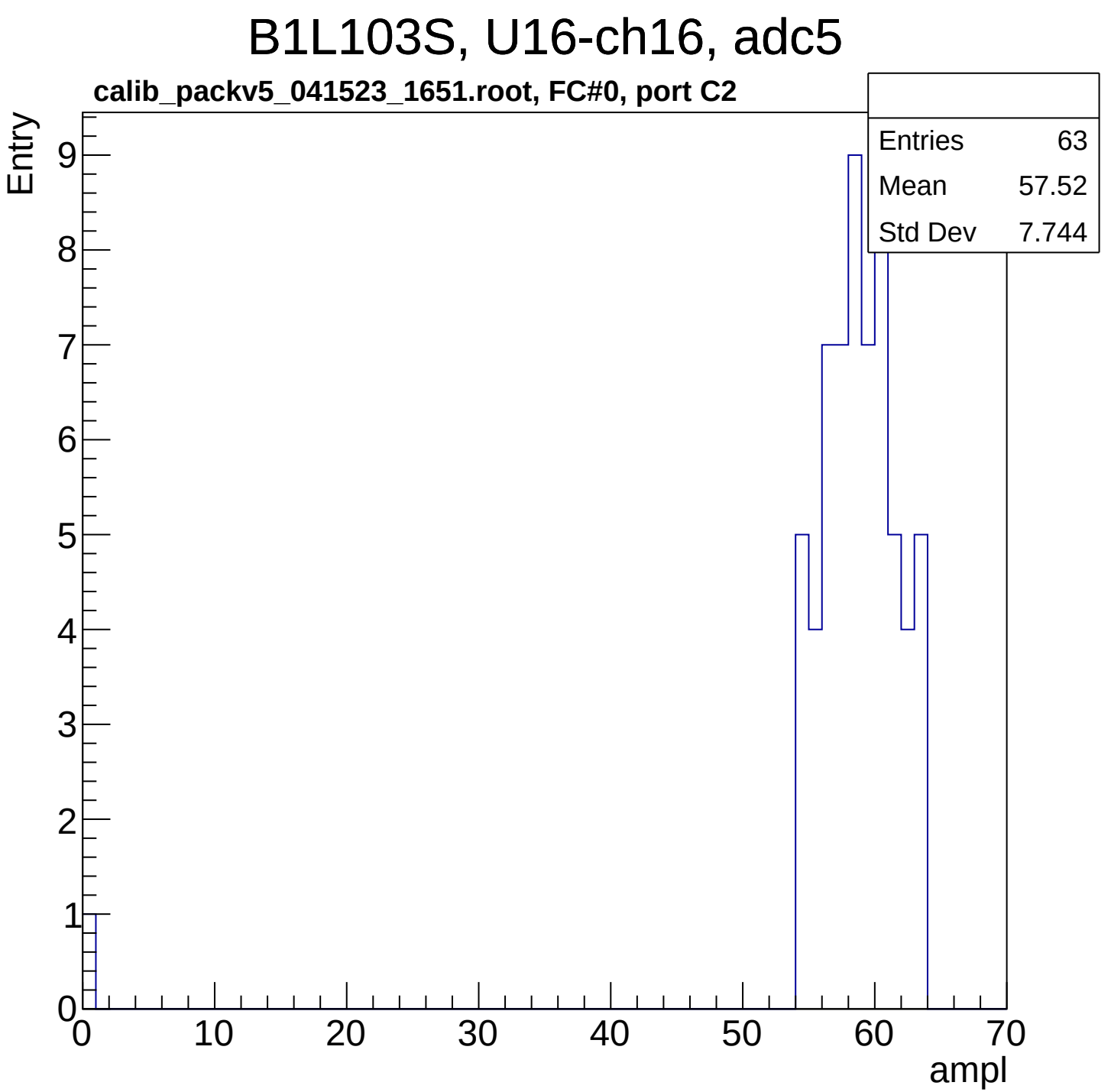
B1L103S, U16-ch16, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 57.52
Std Dev 7.744
Entry
ampl
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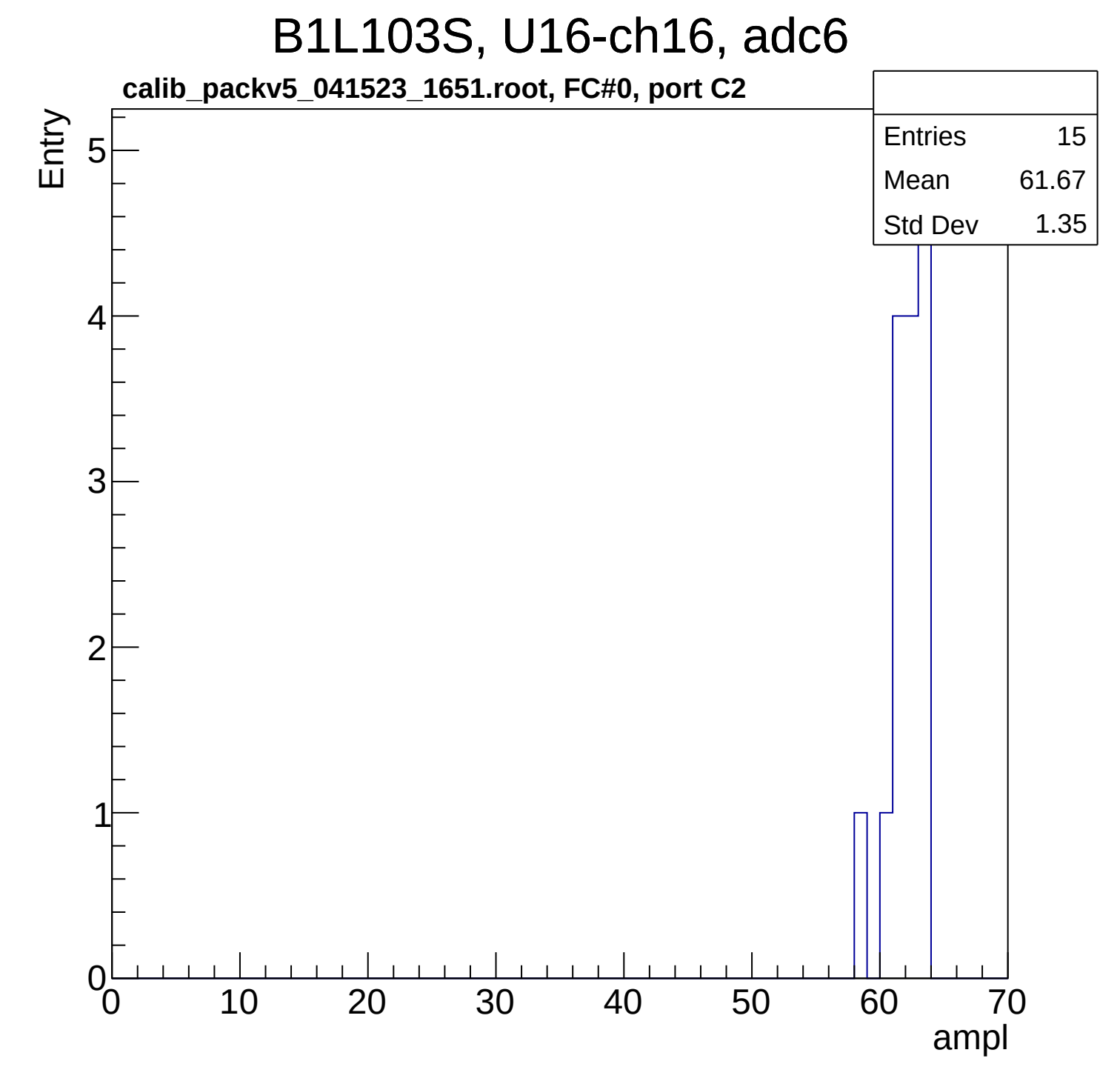
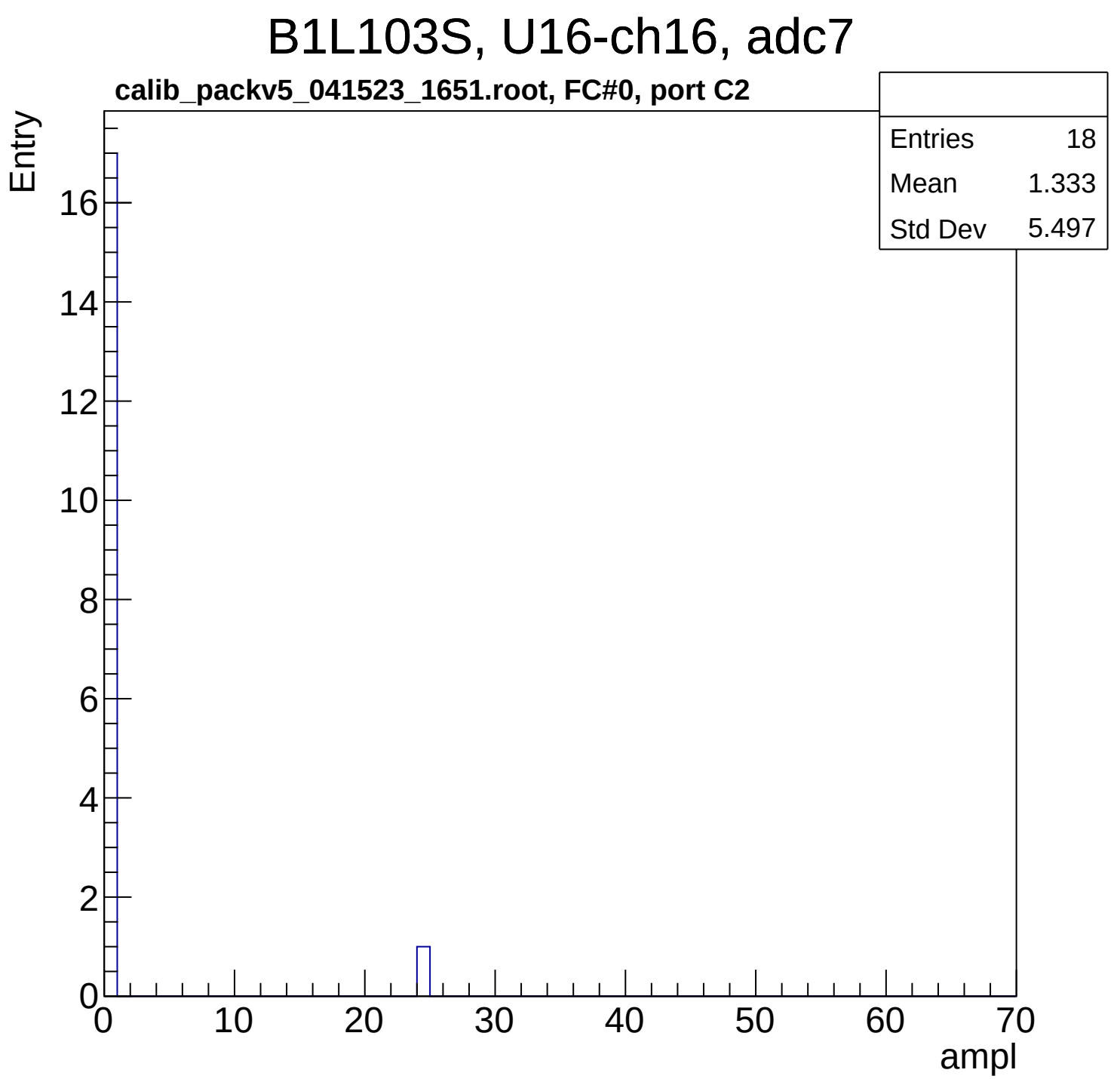
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch16, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.67
Std Dev 1.35
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U16-ch16, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.333
Std Dev 5.497
Entry
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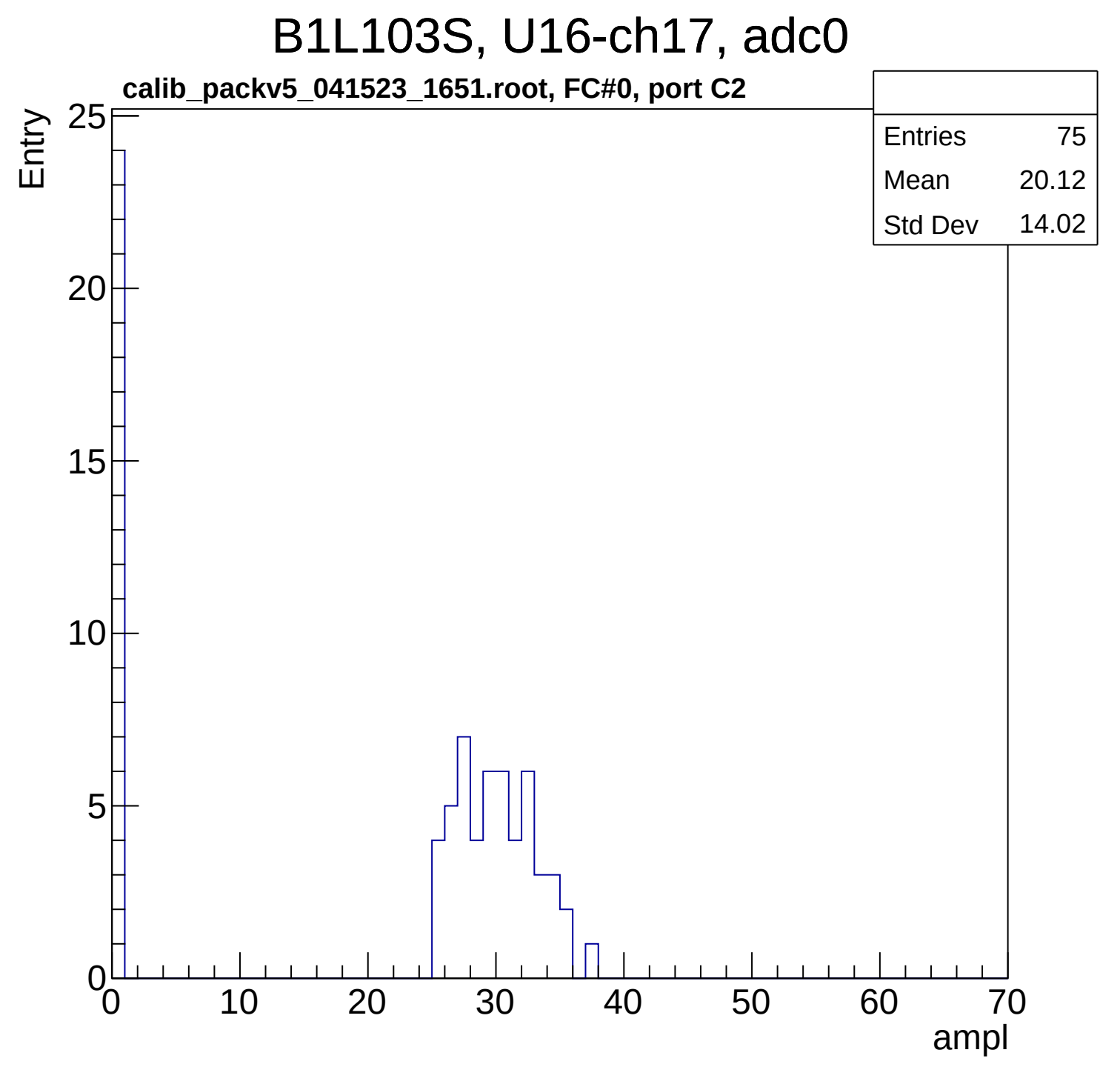
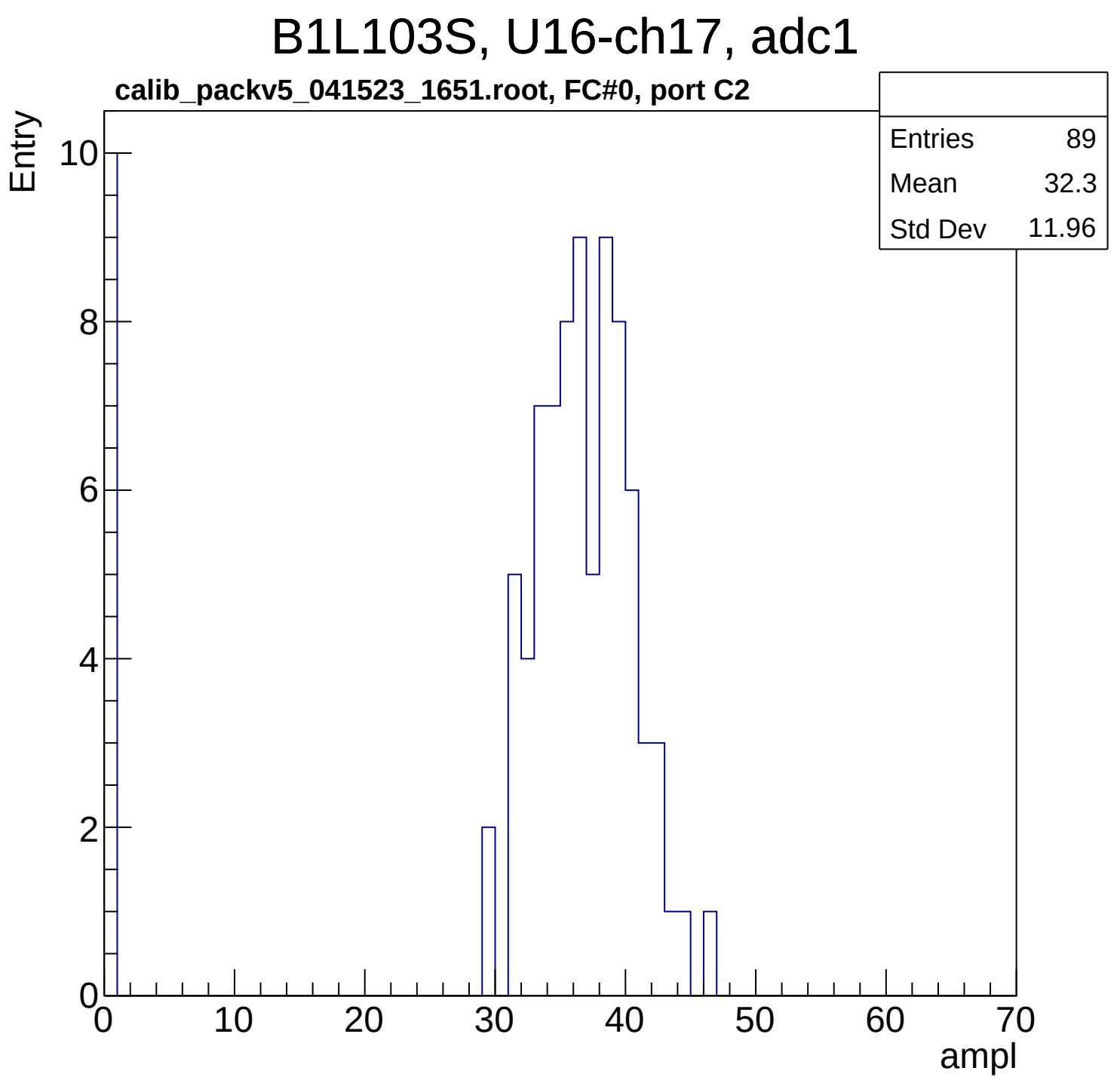
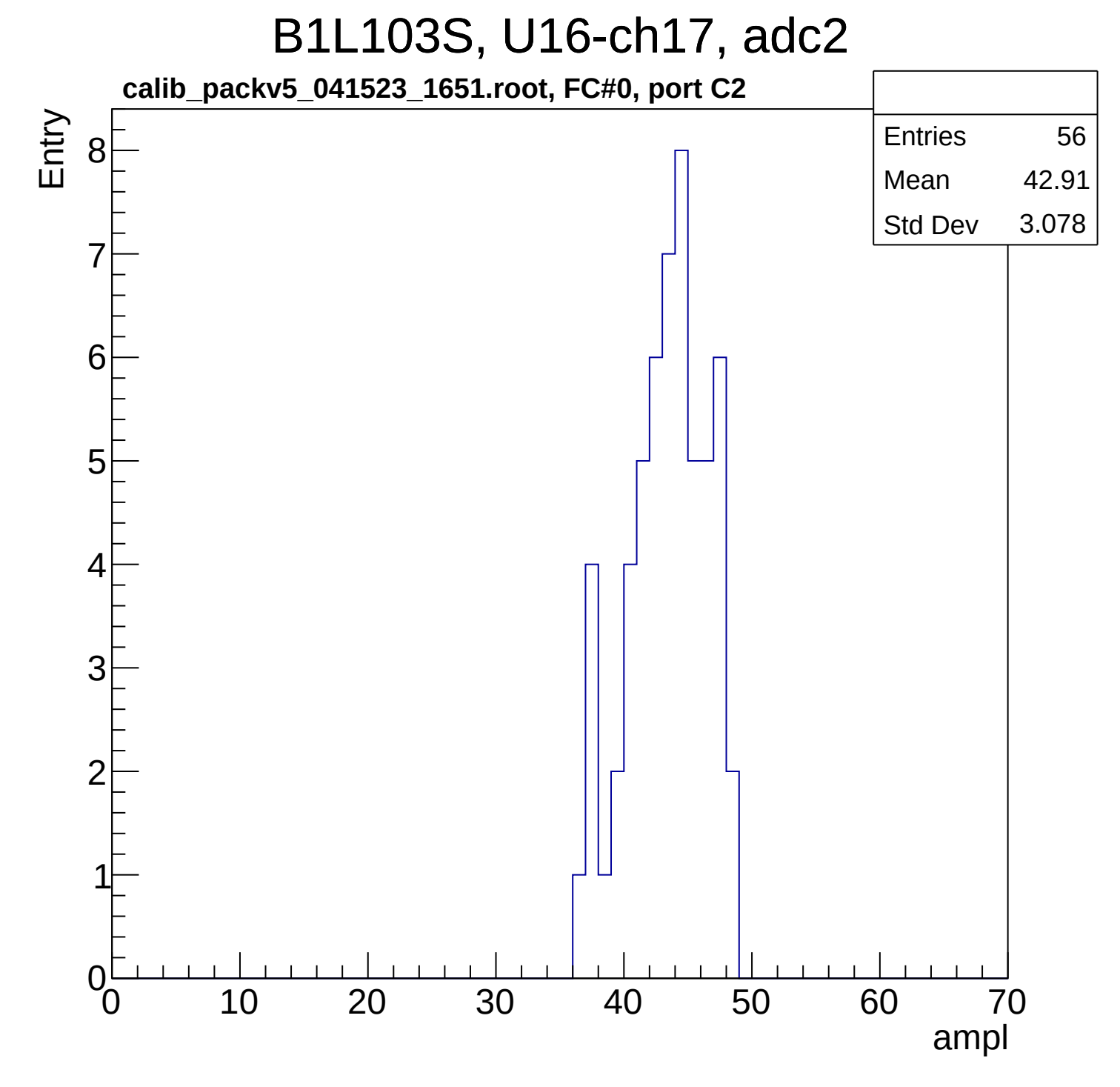
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch17, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 20.12
Std Dev 14.02
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U16-ch17, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 32.3
Std Dev 11.96
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch17, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 42.91
Std Dev 3.078
Entry
ampl
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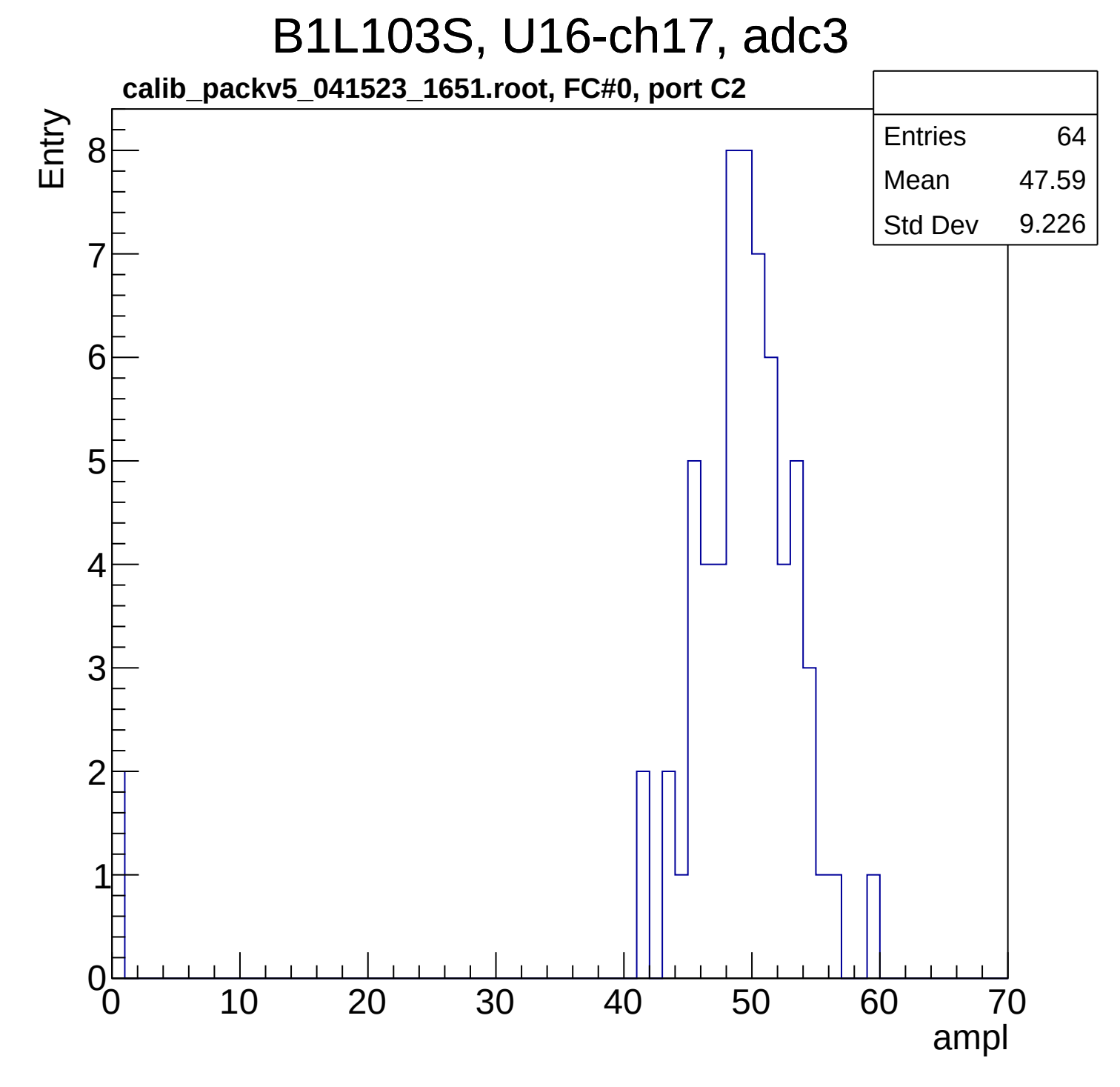
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch17, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 47.59
Std Dev 9.226
Entry
ampl
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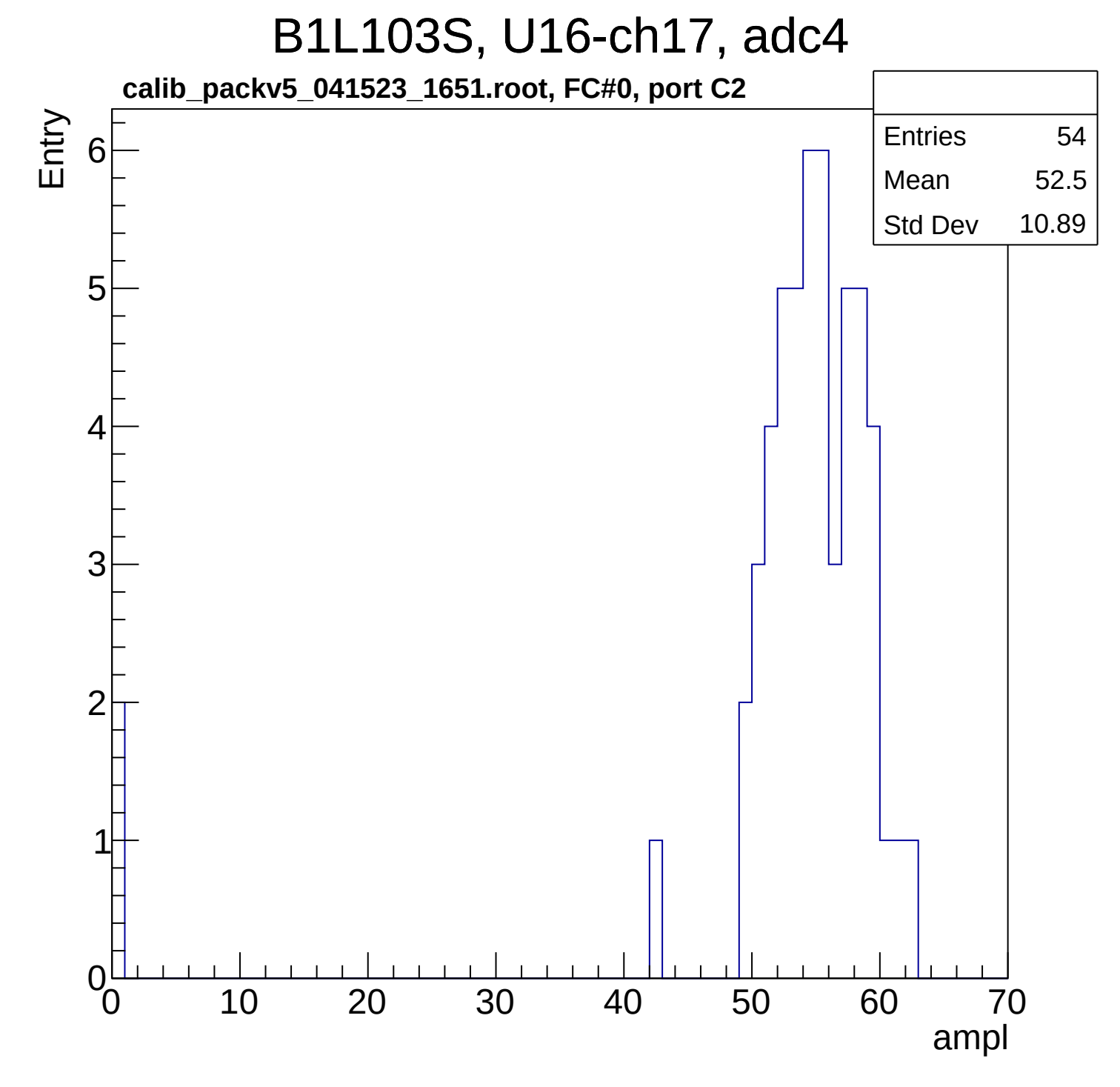
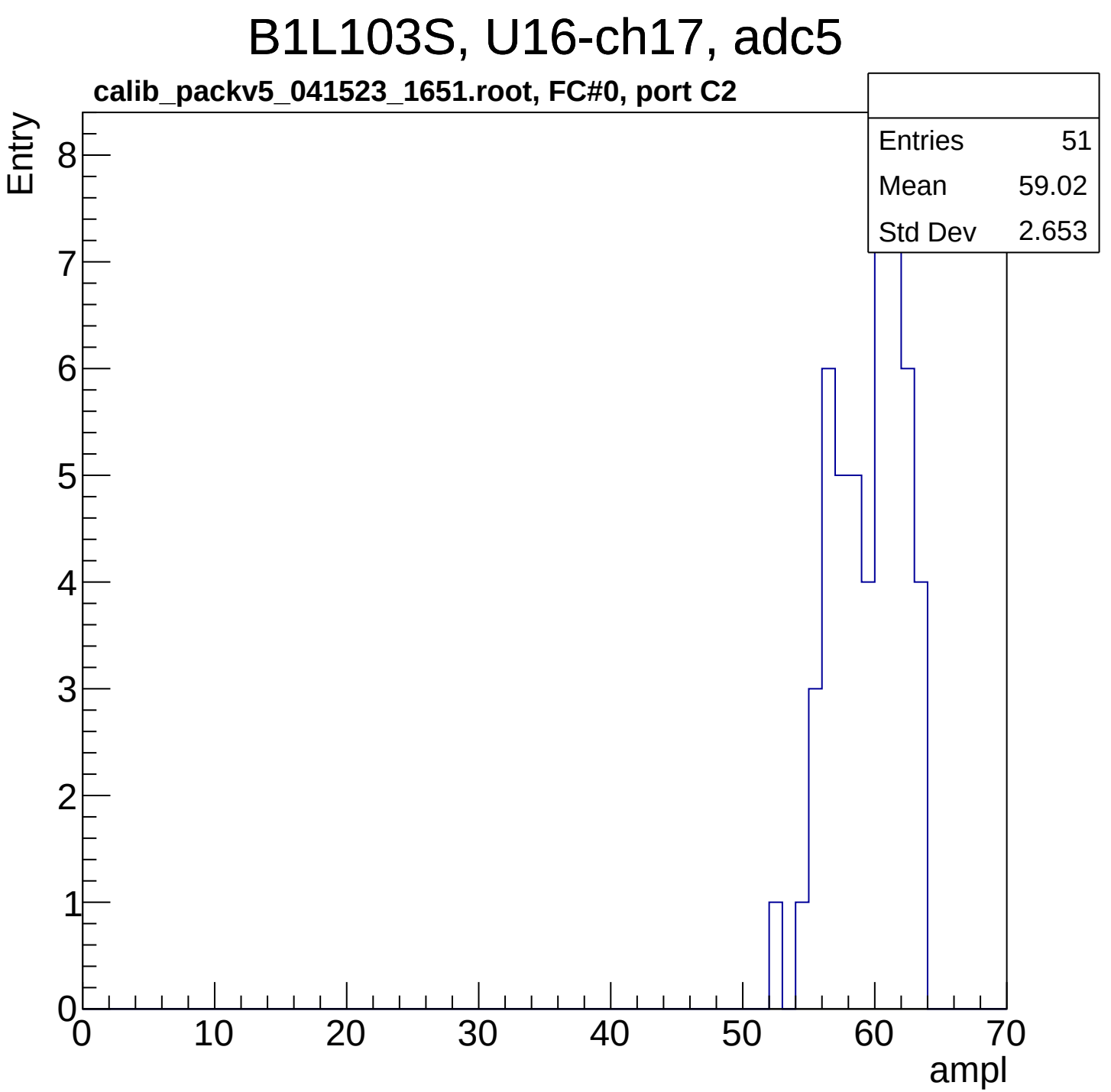
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch17, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 52.5
Std Dev 10.89
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U16-ch17, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 59.02
Std Dev 2.653
Entry
ampl
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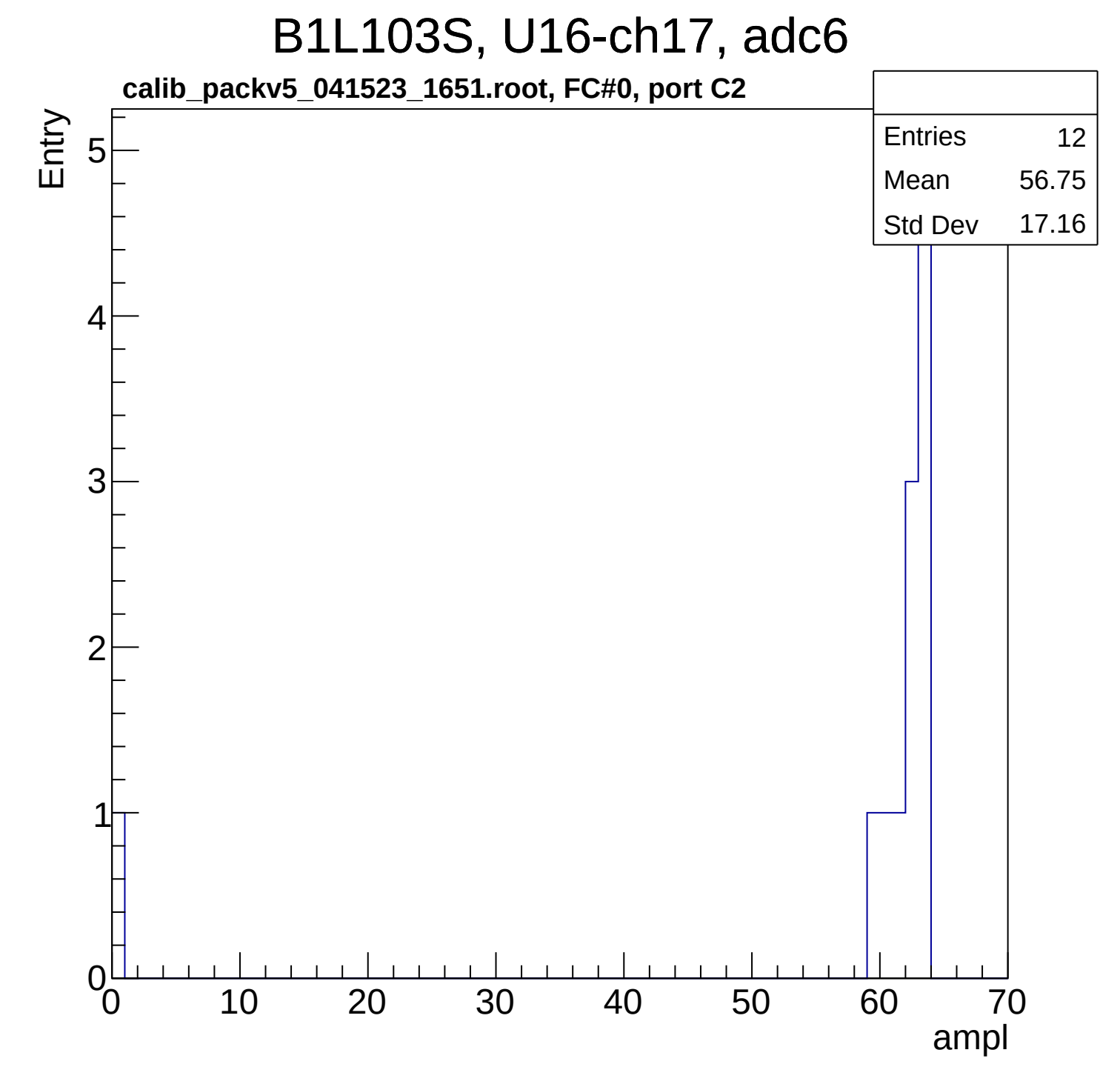
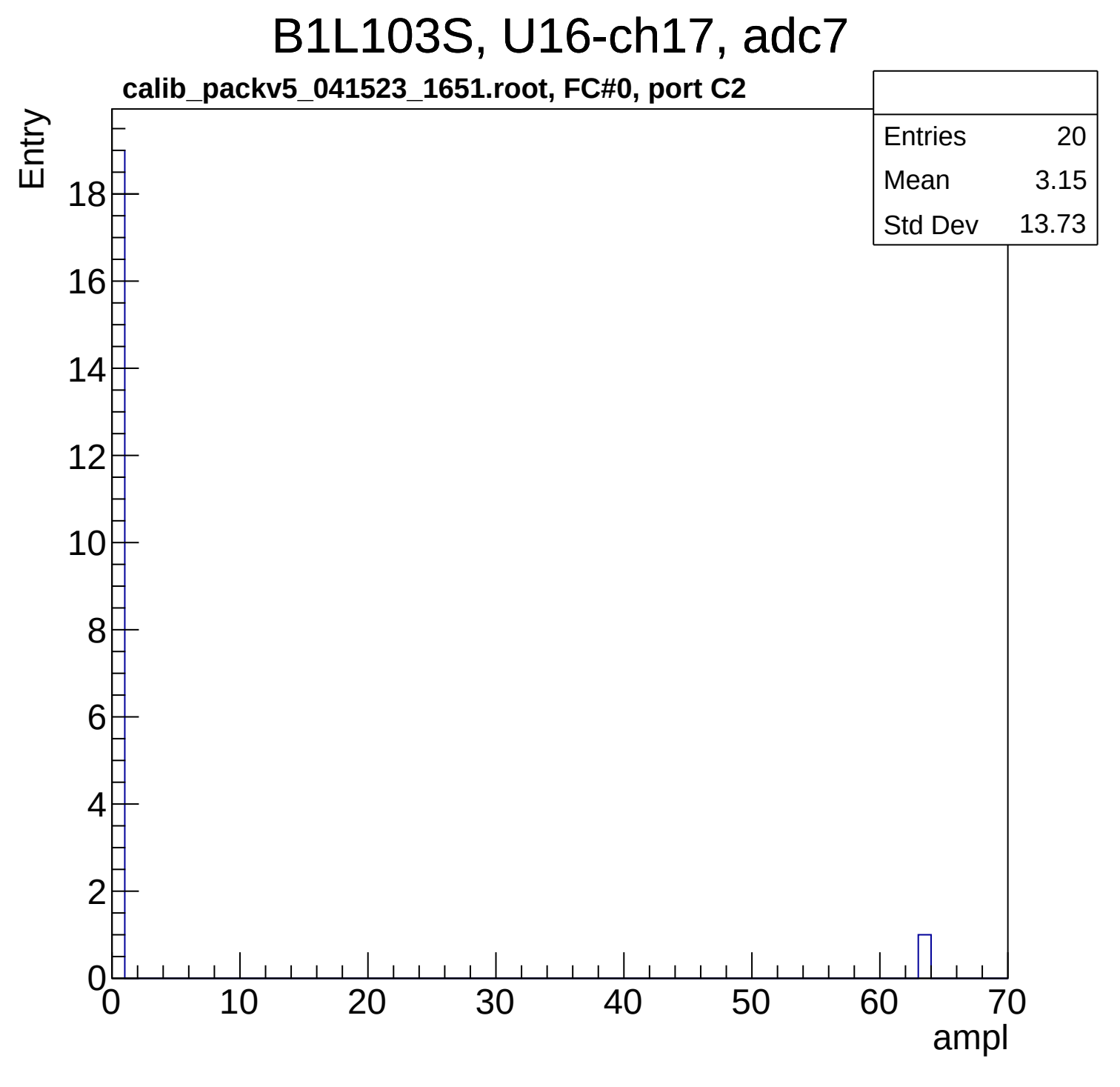
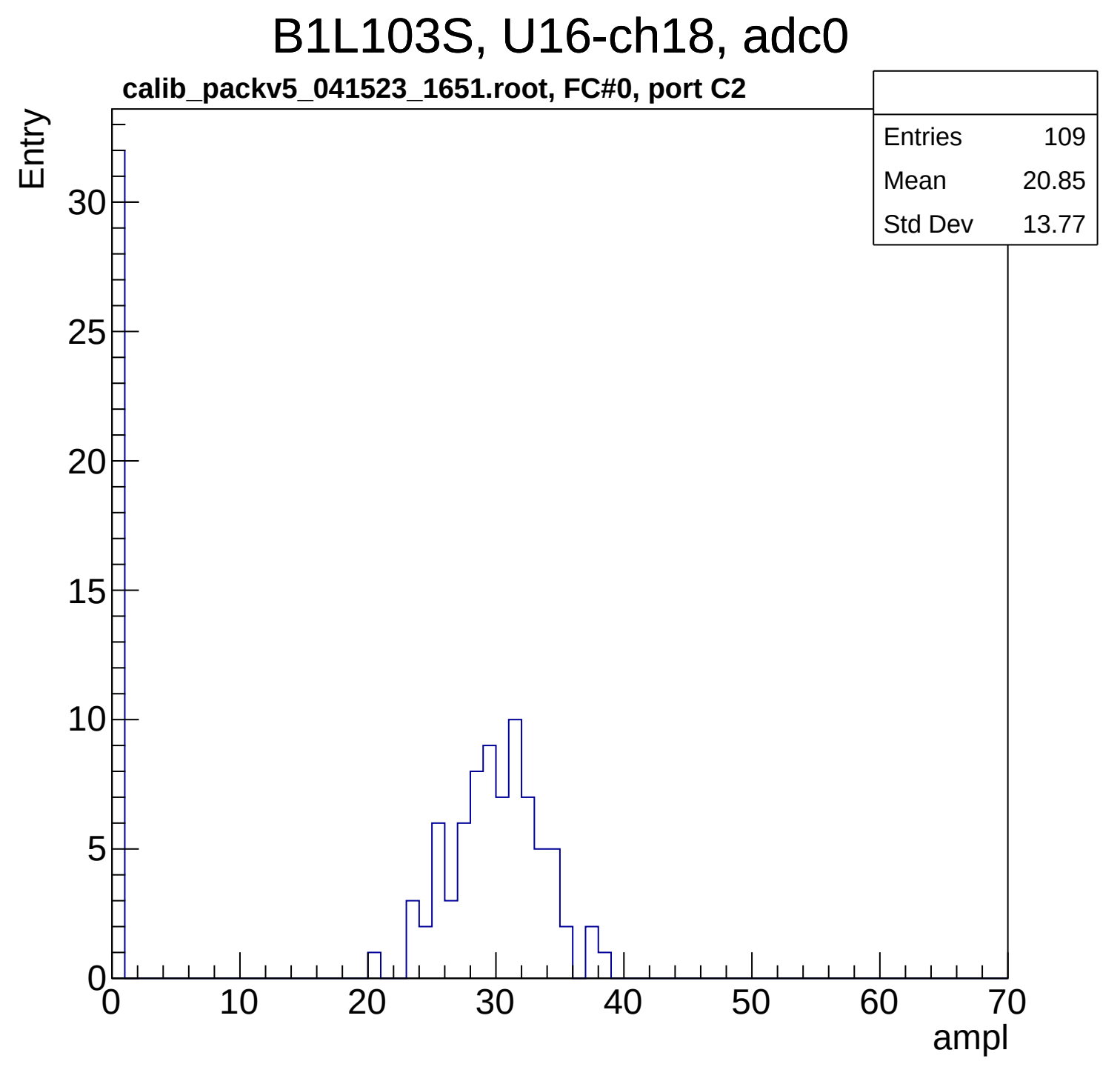
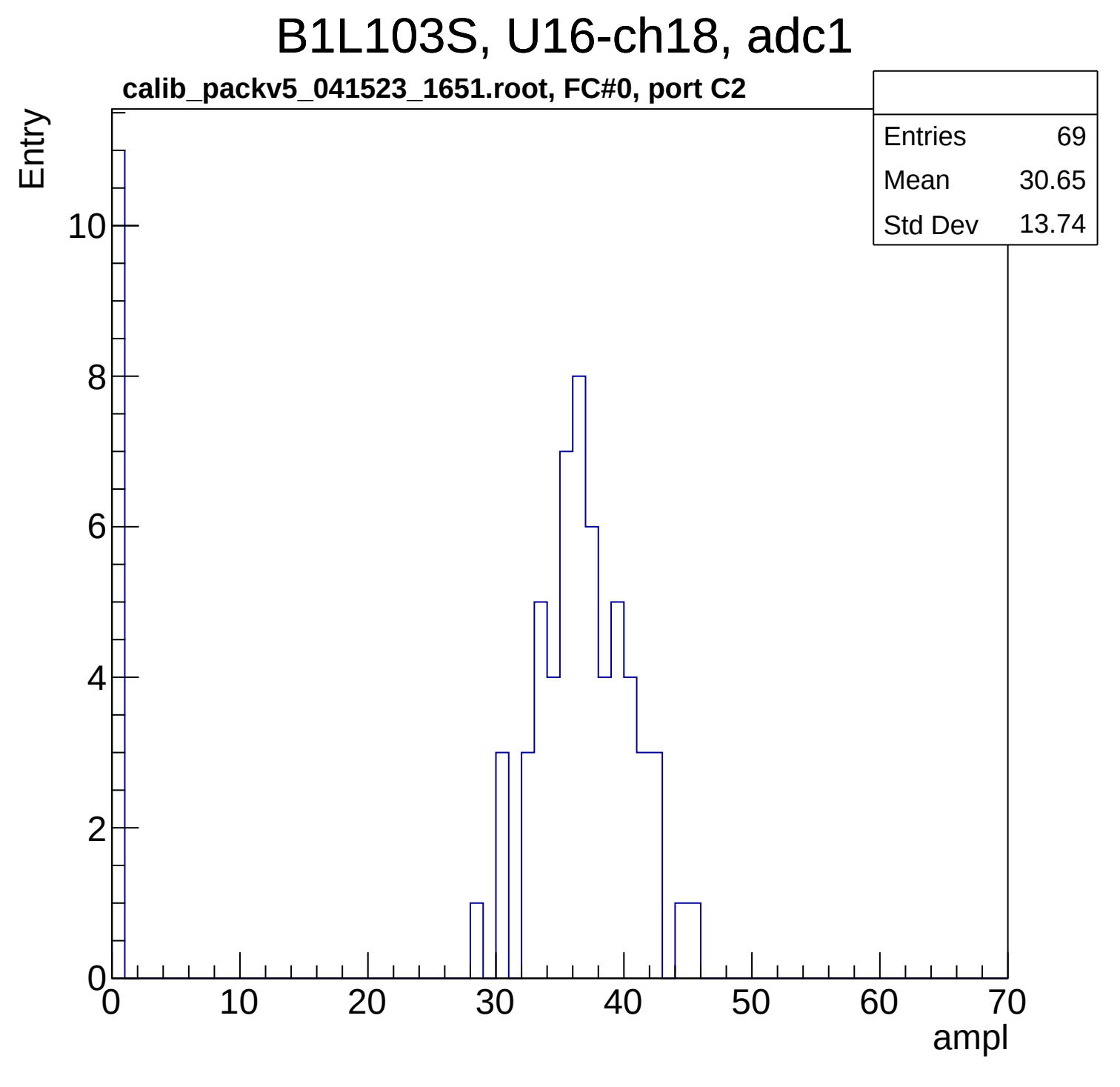
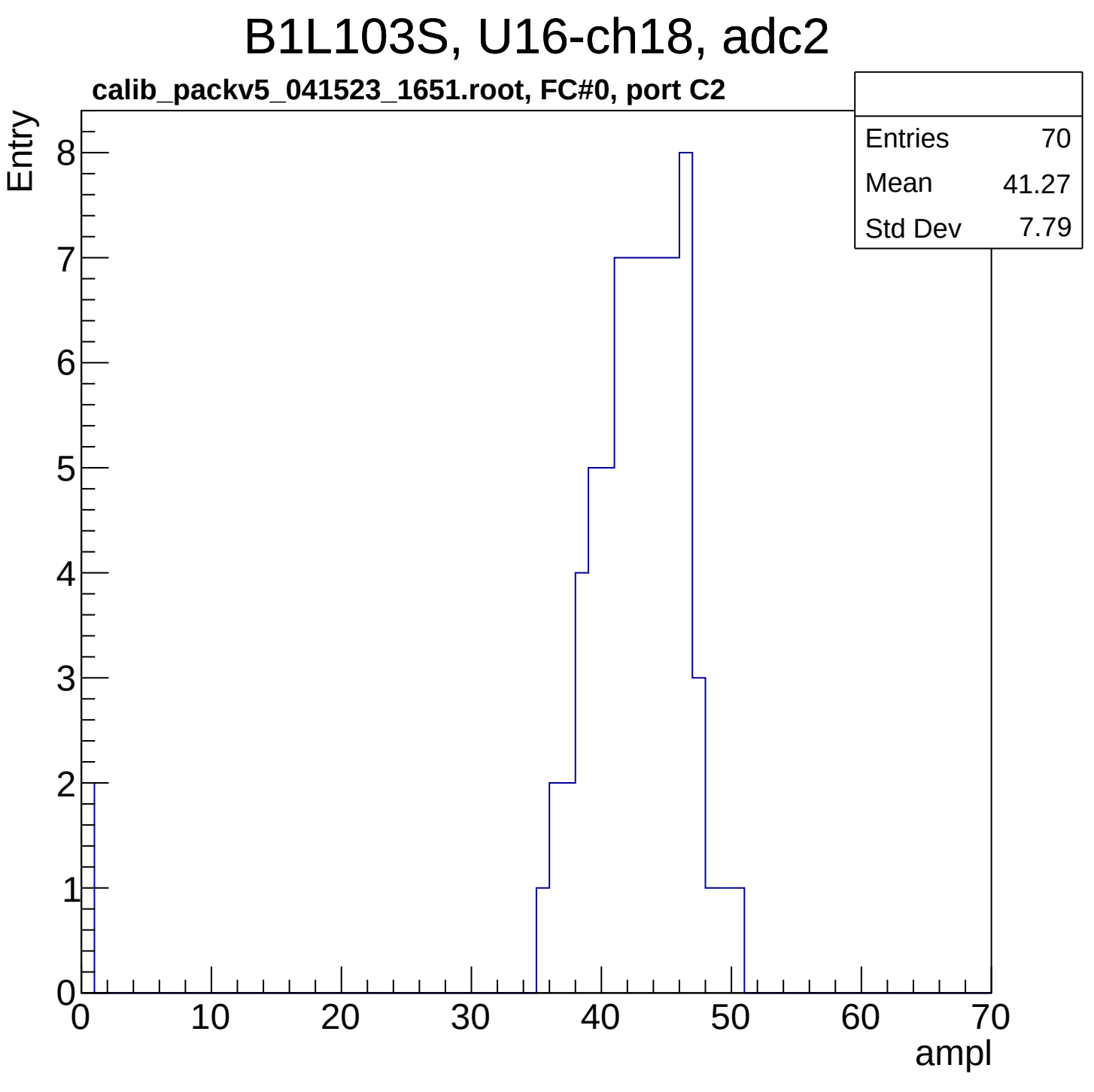
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch17, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.75
Std Dev 17.16
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U16-ch17, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch18, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 109
Mean 20.85
Std Dev 13.77
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch18, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 30.65
Std Dev 13.74
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch18, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 41.27
Std Dev 7.79
Entry
ampl
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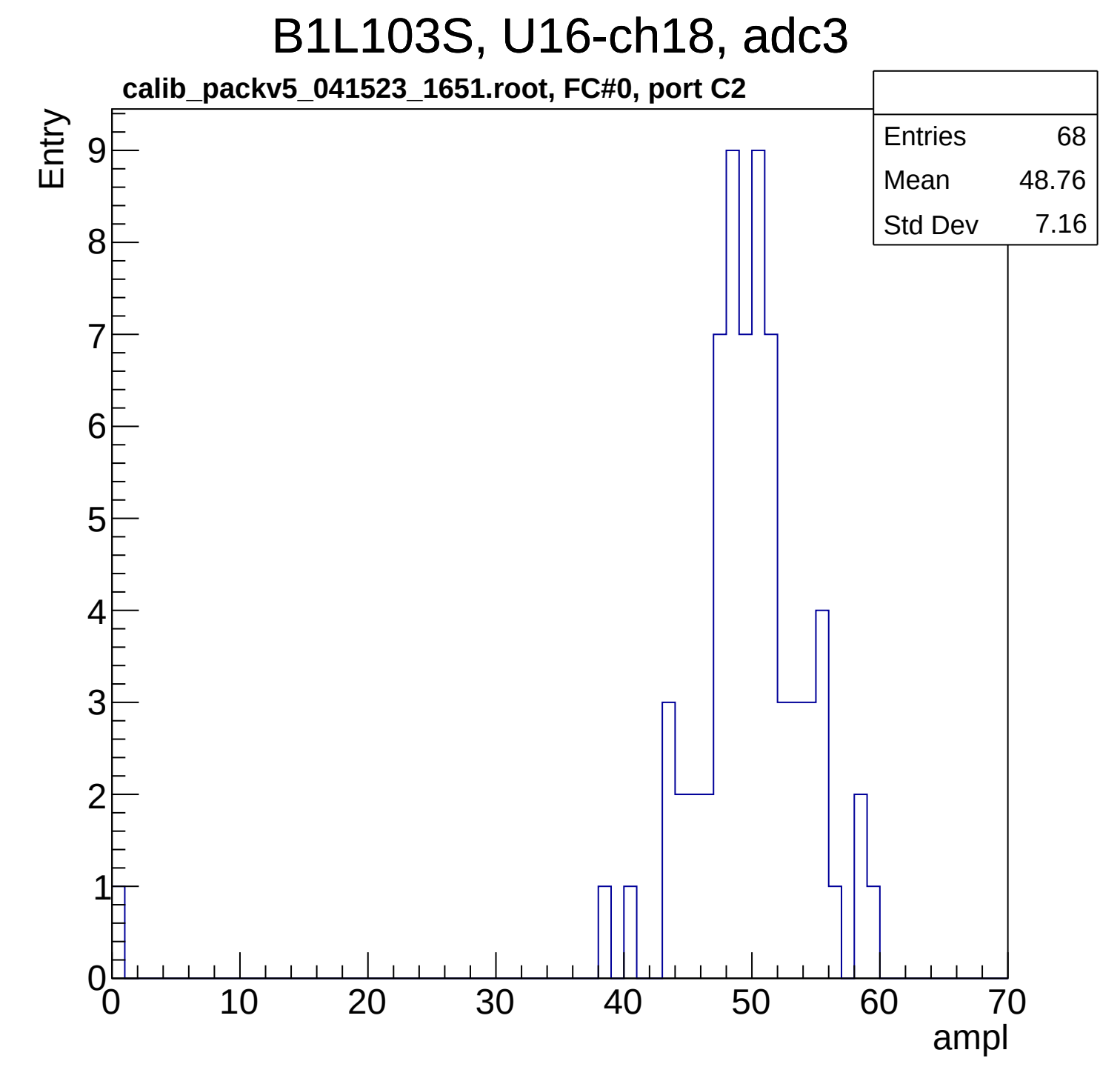
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch18, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 48.76
Std Dev 7.16
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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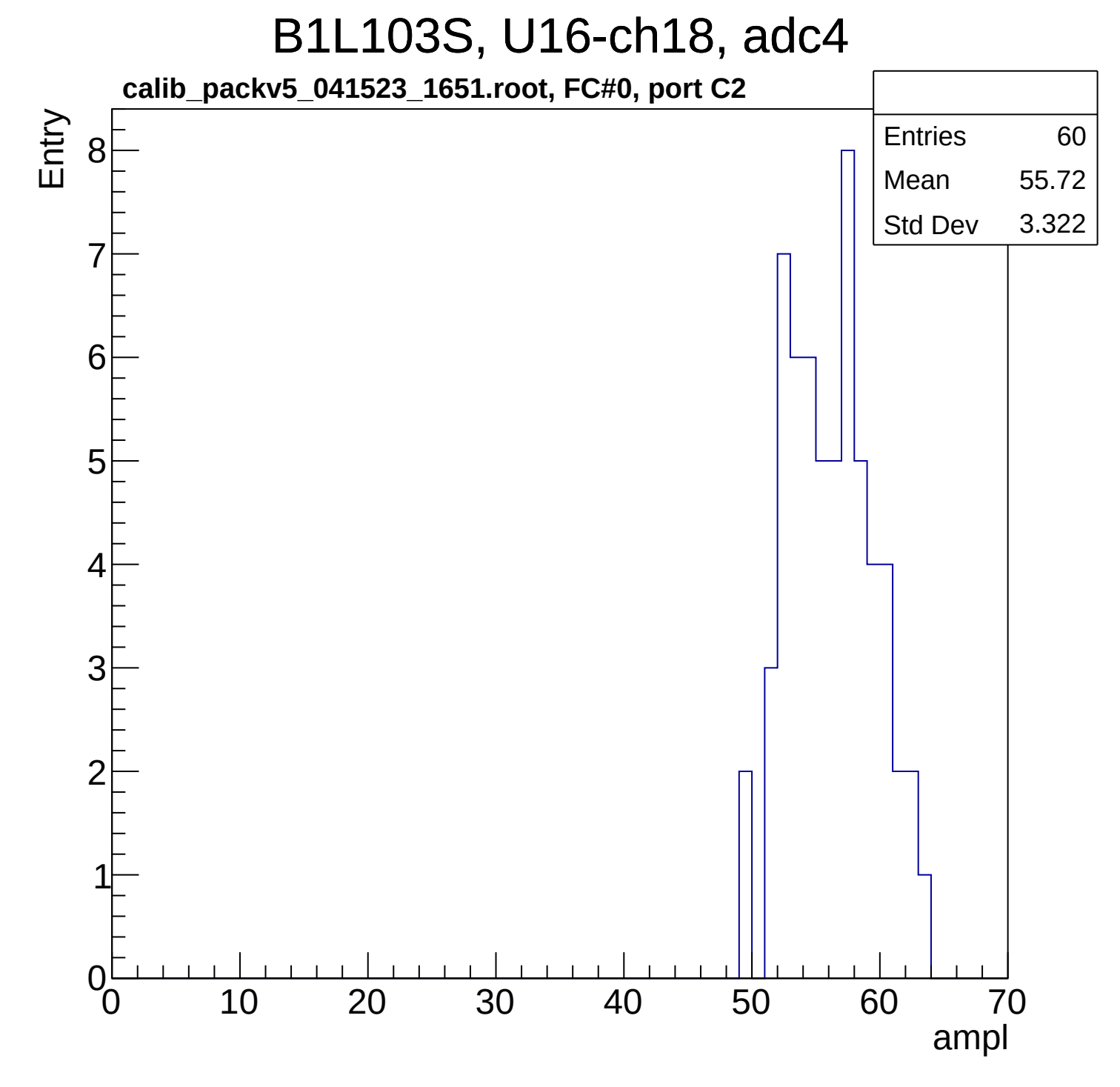
B1L103S, U16-ch18, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 55.72
Std Dev 3.322
Entry
ampl
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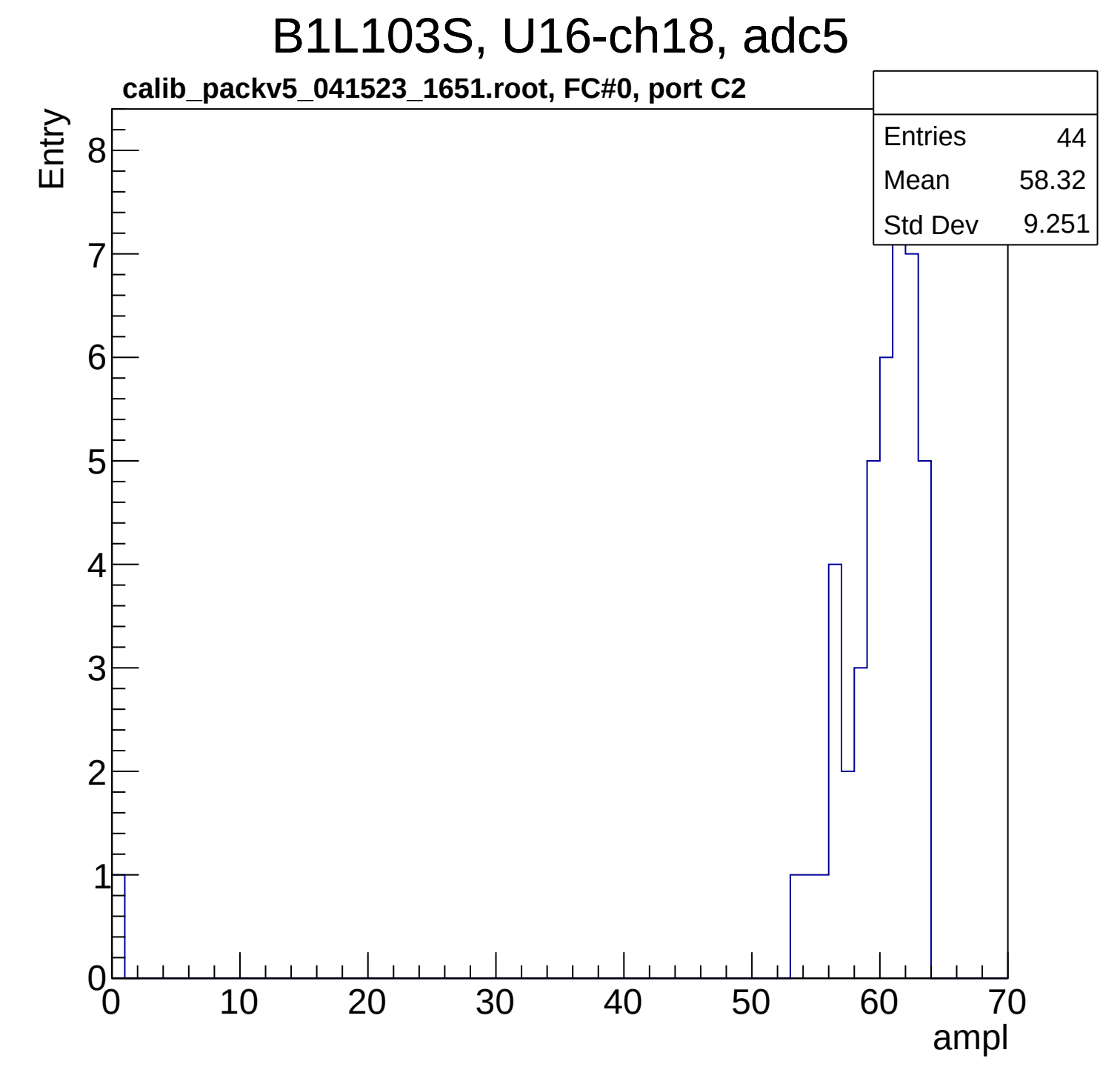
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch18, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 58.32
Std Dev 9.251
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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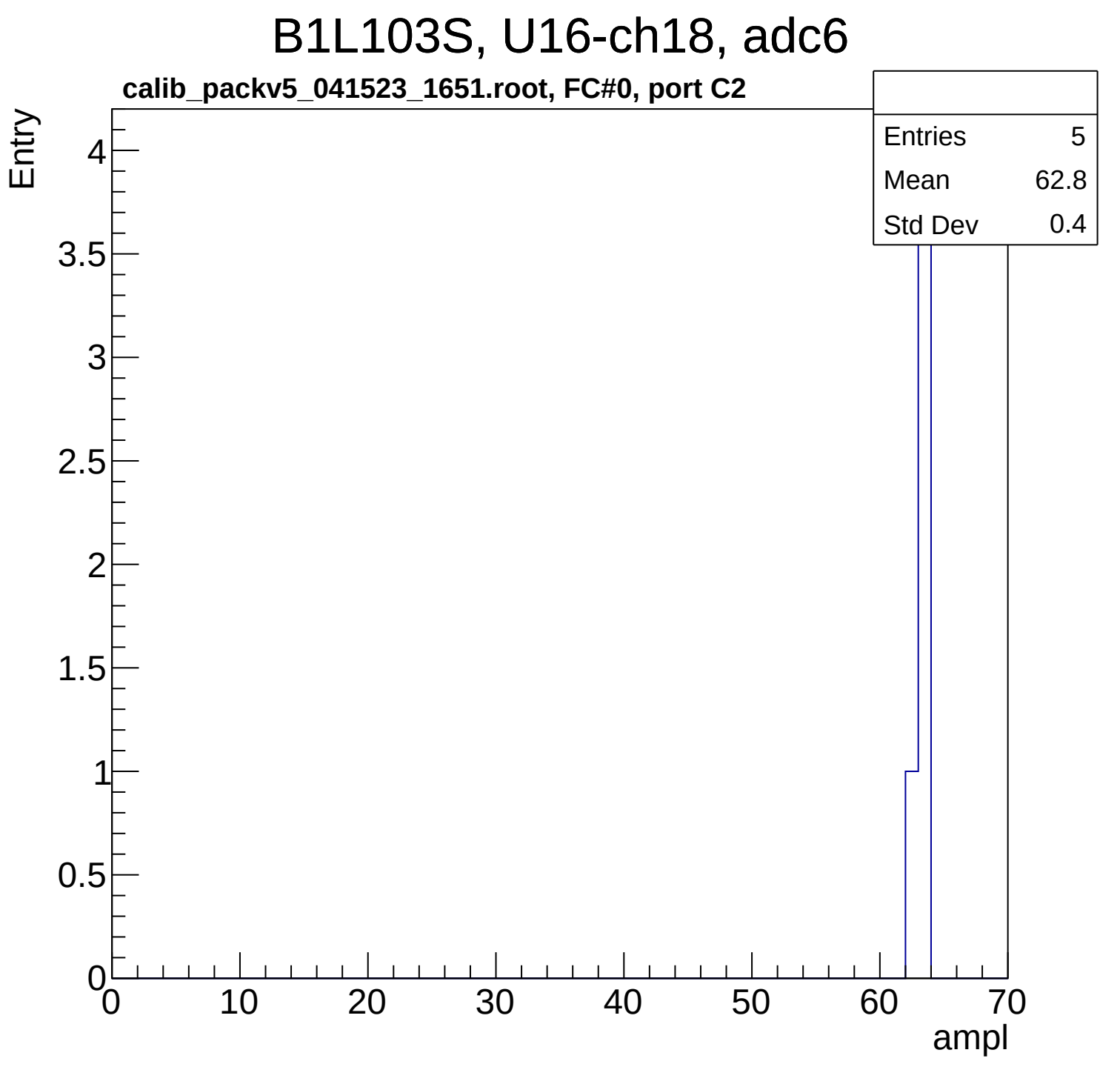
B1L103S, U16-ch18, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.8
Std Dev 0.4
Entry
ampl
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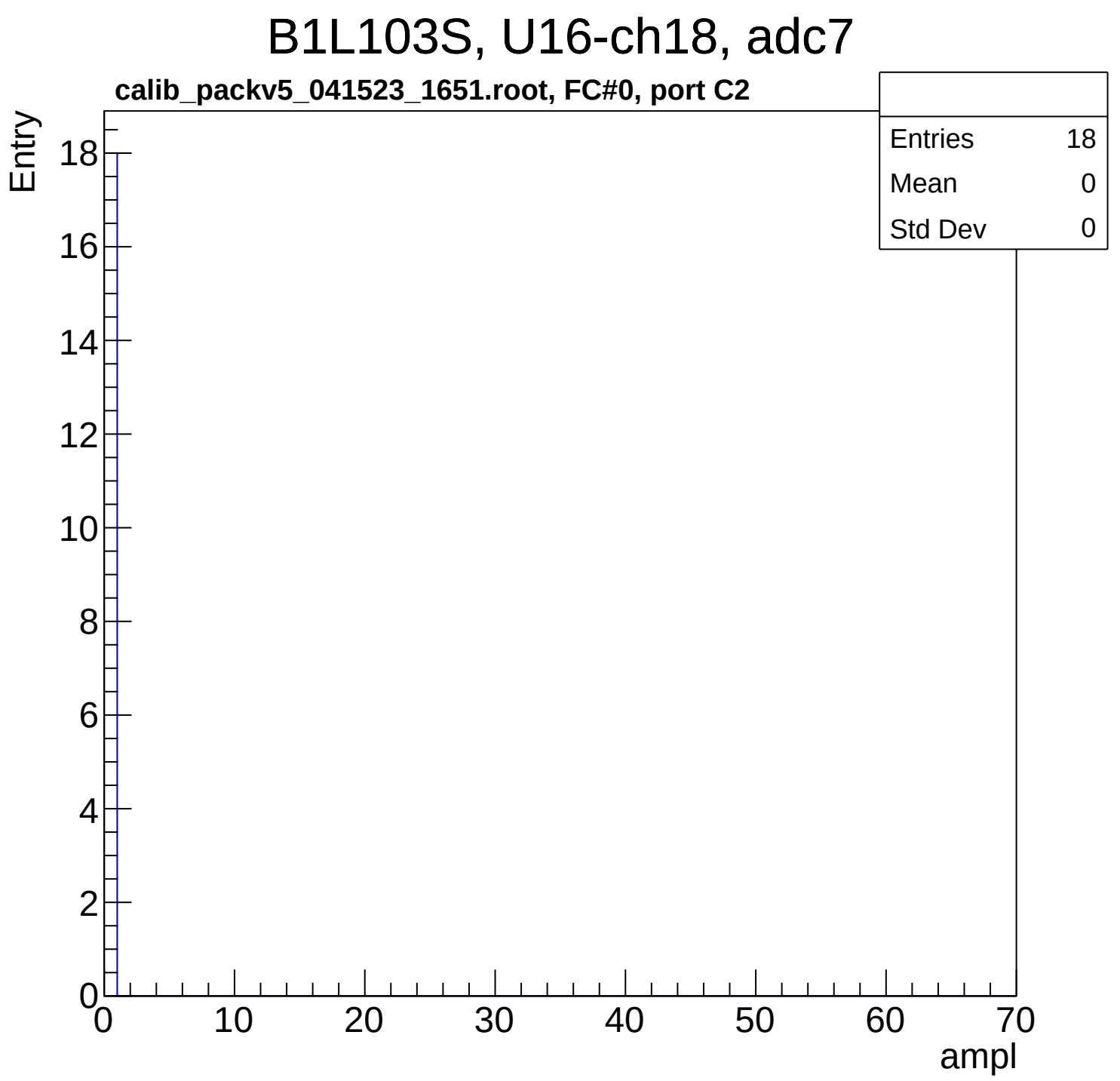
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U16-ch18, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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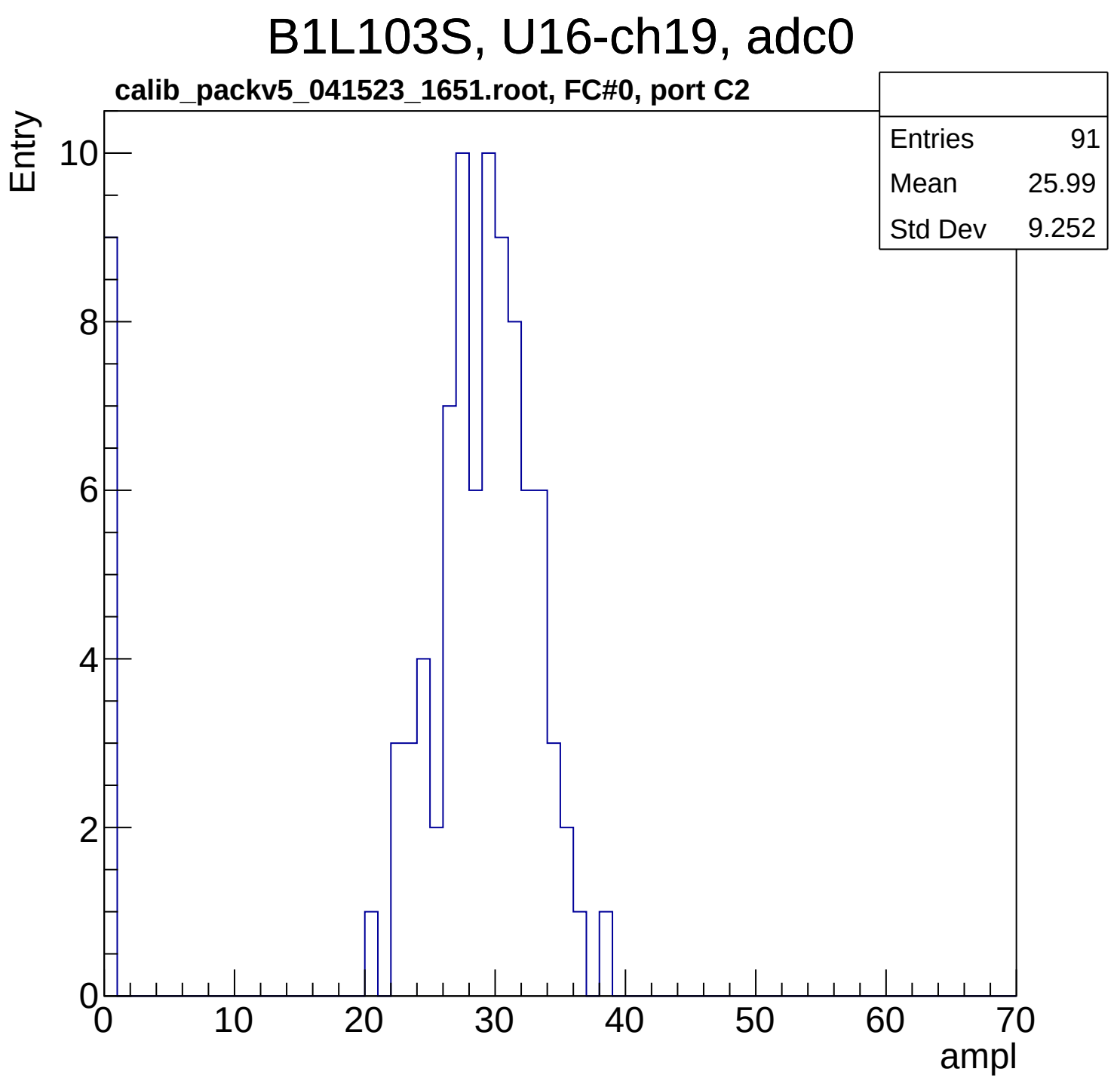
50
60
70
ampl


B1L103S, U16-ch19, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 25.99
Std Dev 9.252
Entry
ampl
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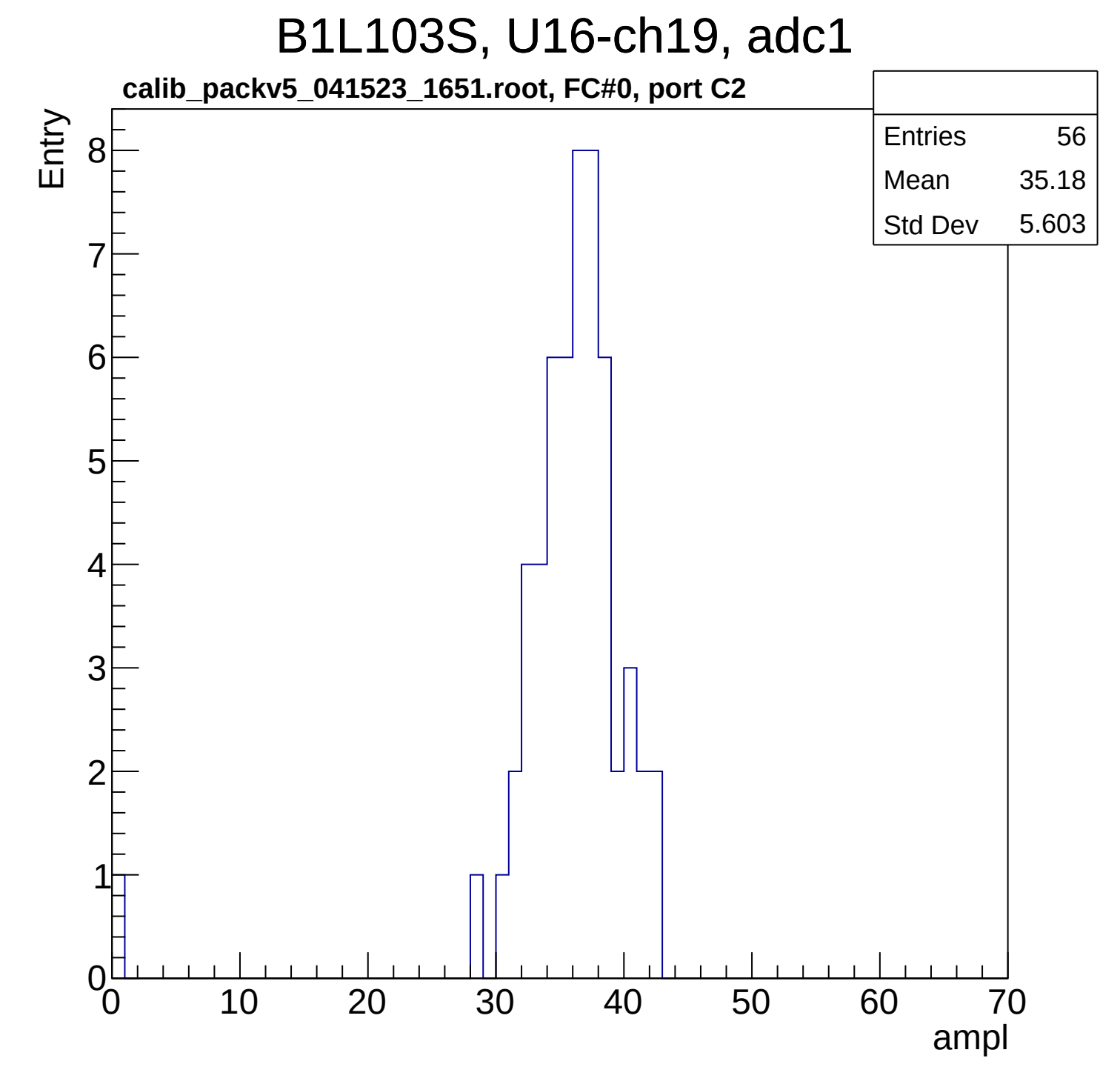
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch19, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 35.18
Std Dev 5.603
Entry
ampl
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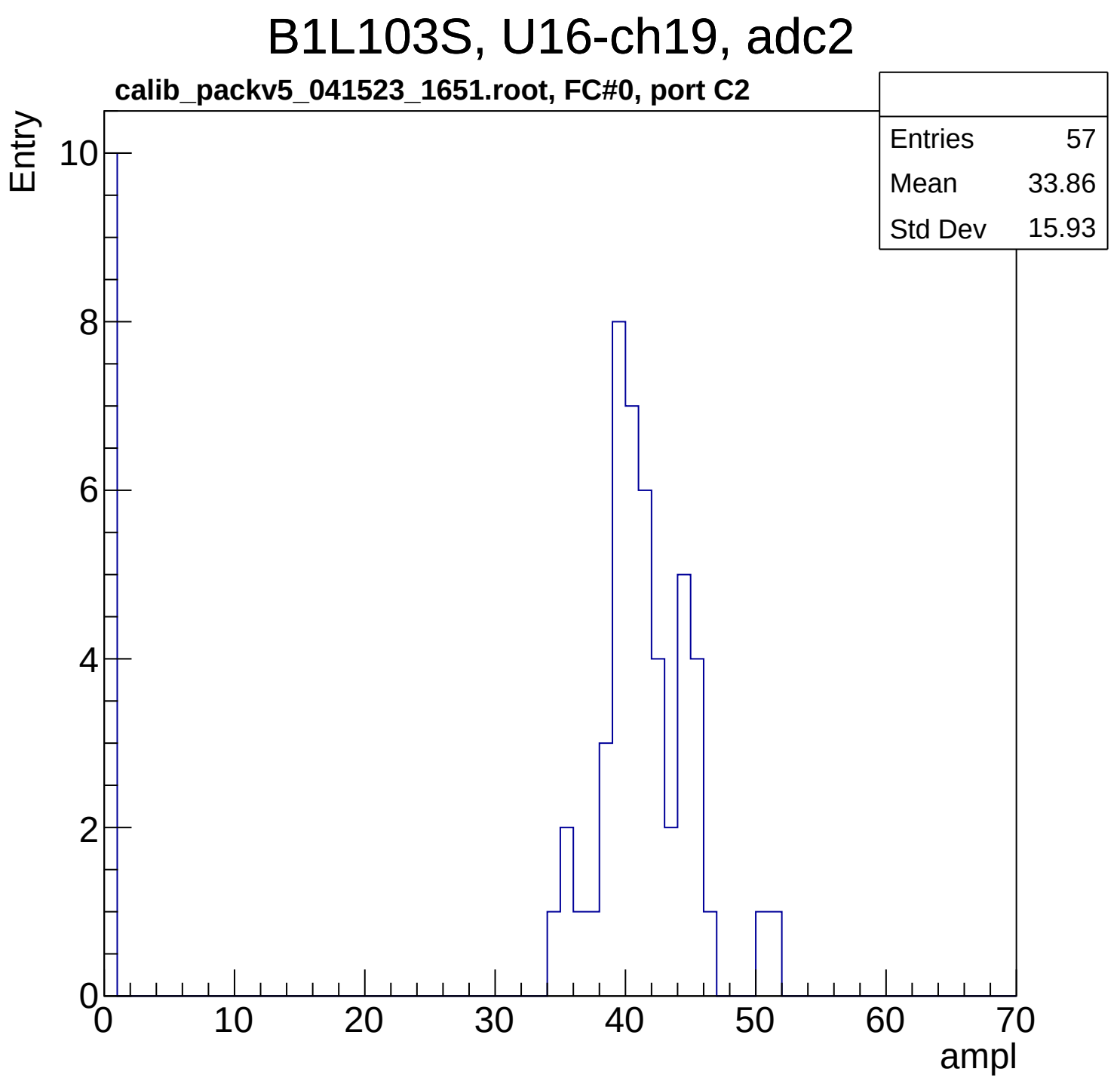
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch19, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 33.86
Std Dev 15.93
Entry
ampl
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4
6
8
10
0
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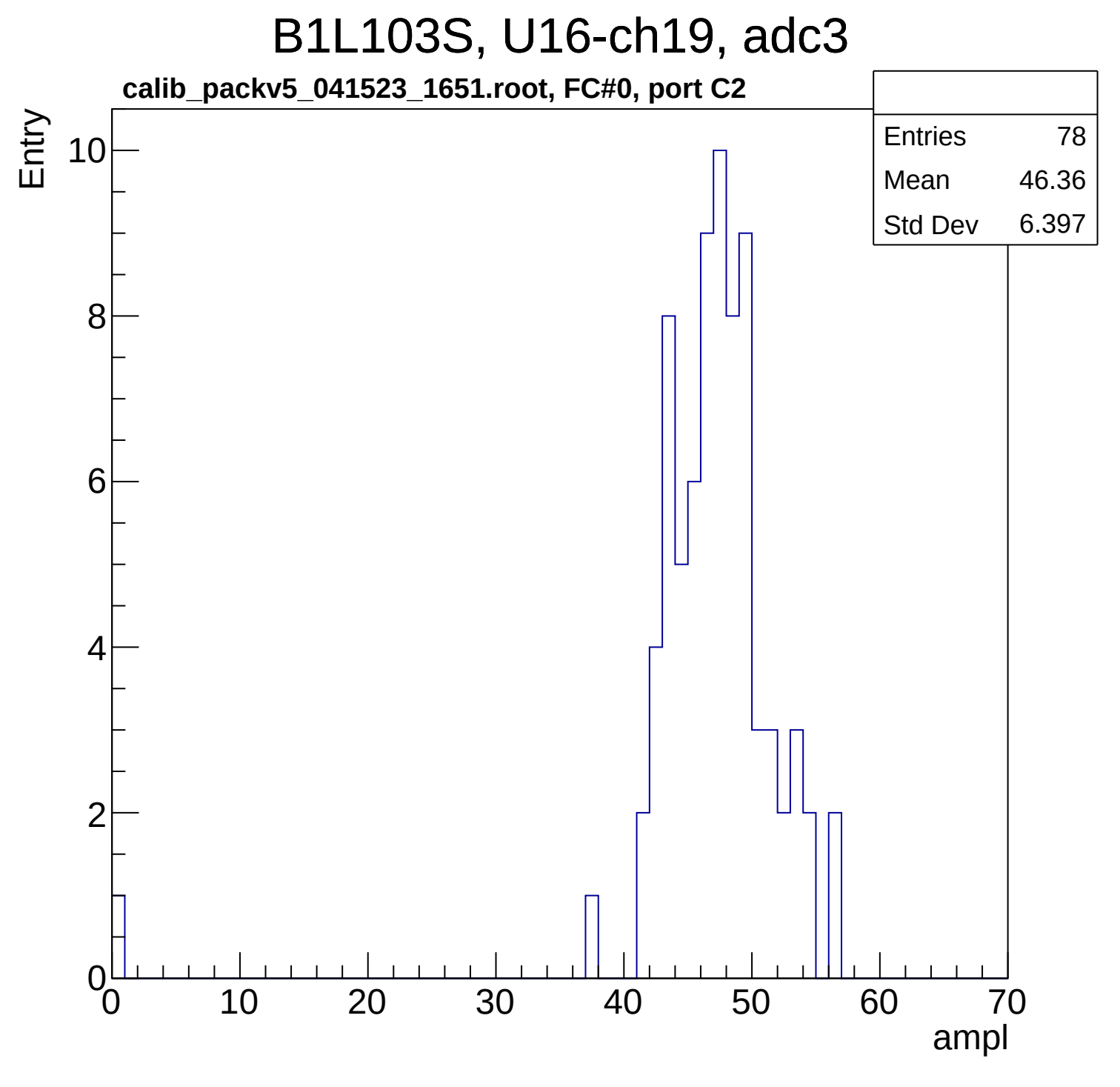
20
30
40
50
60
70


B1L103S, U16-ch19, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 46.36
Std Dev 6.397
Entry
ampl
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4
6
8
10
0
10
20
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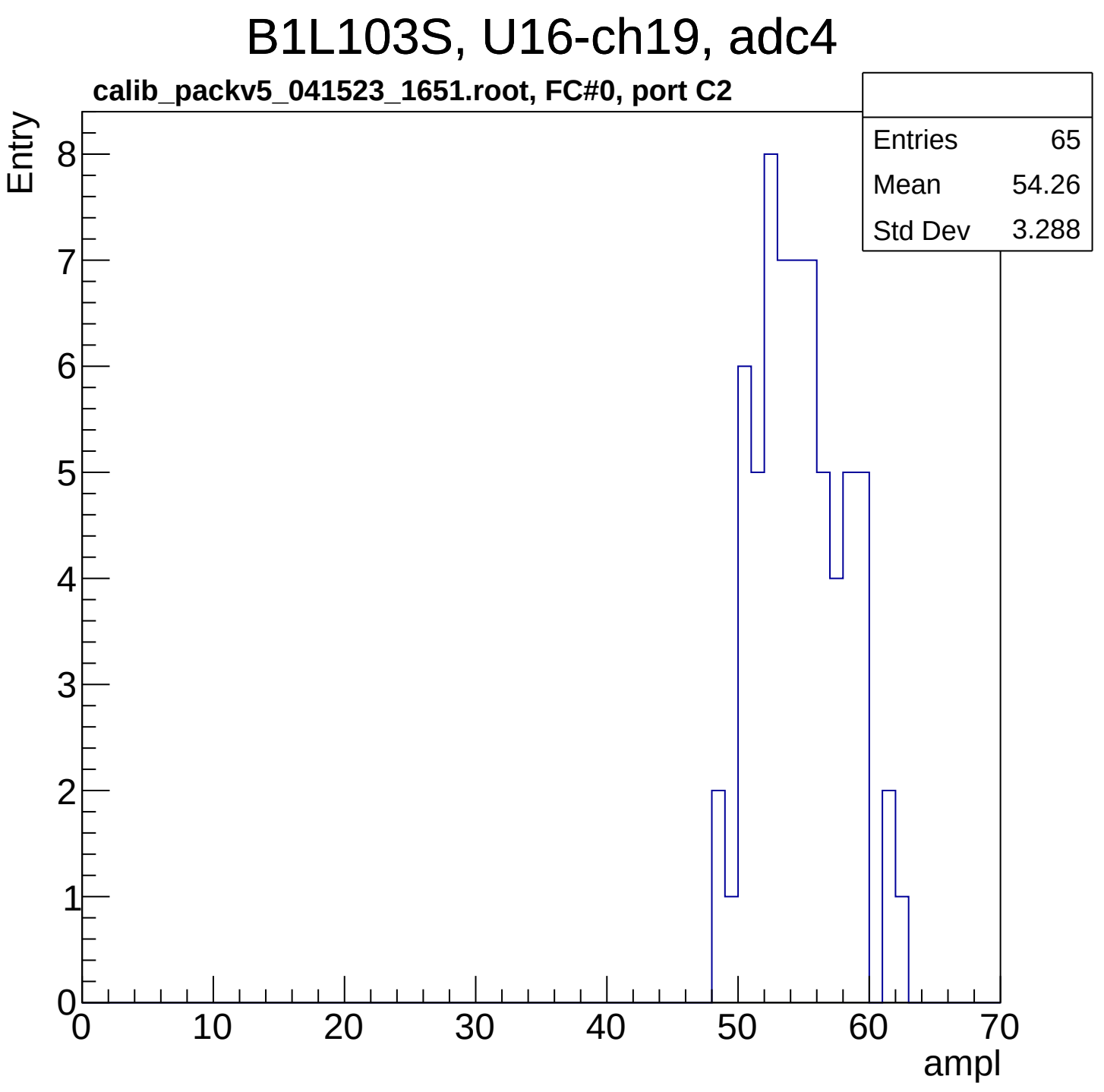
40
50
60
70


B1L103S, U16-ch19, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 54.26
Std Dev 3.288
Entry
ampl
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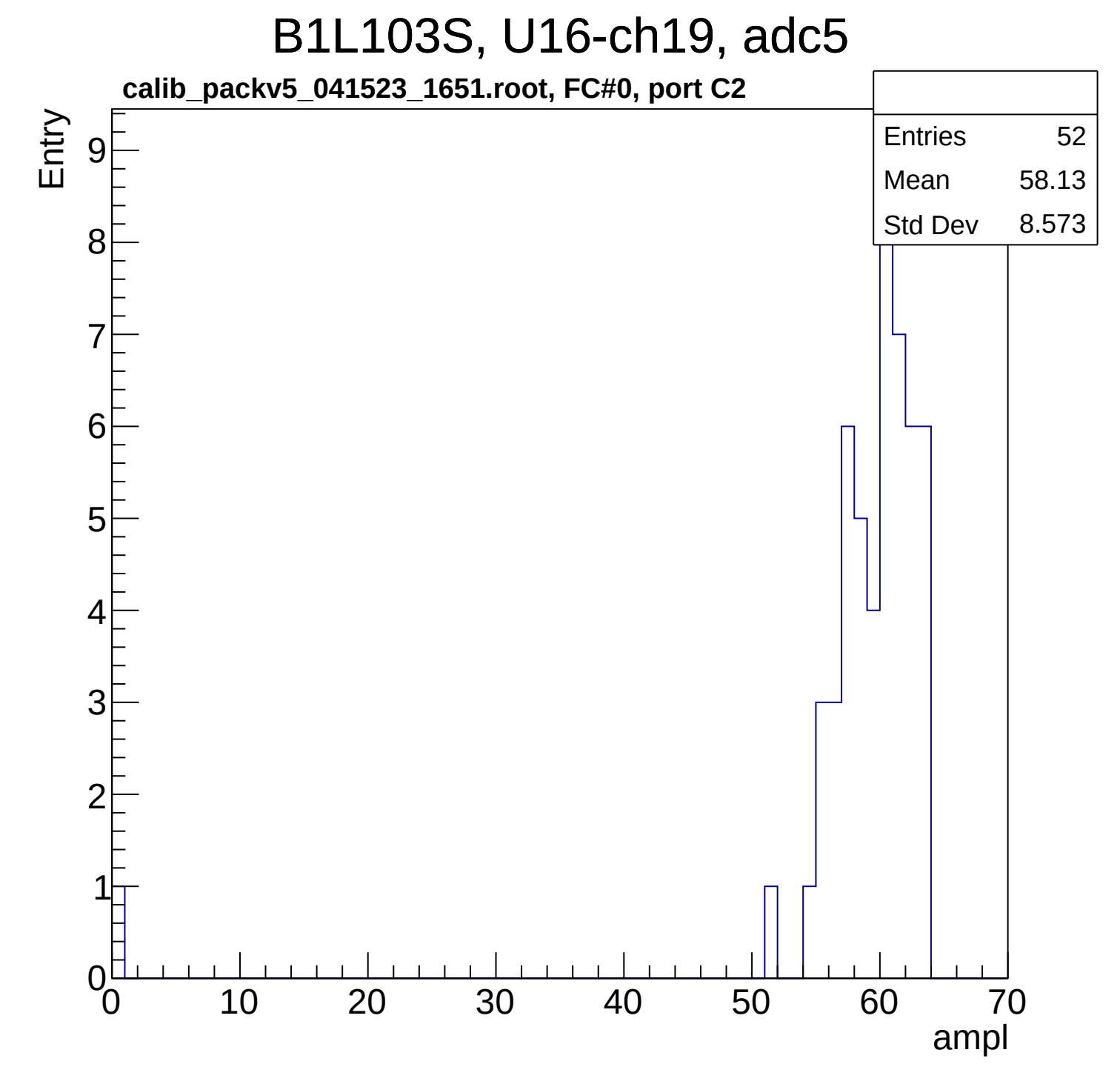
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch19, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.13
Std Dev 8.573
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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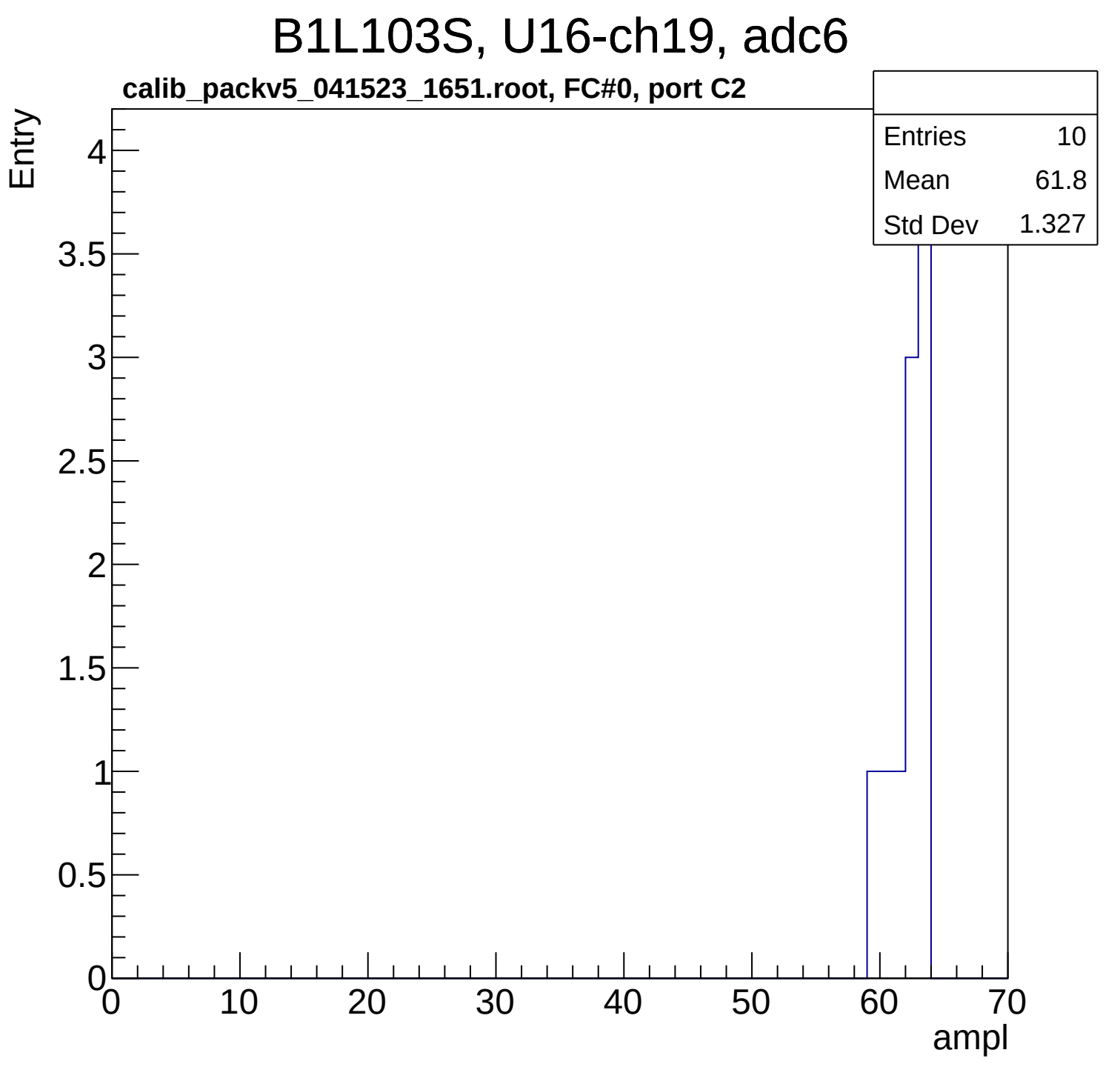
B1L103S, U16-ch19, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.8
Std Dev 1.327
Entry
ampl
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1.5
2
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3
3.5
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0
10
20
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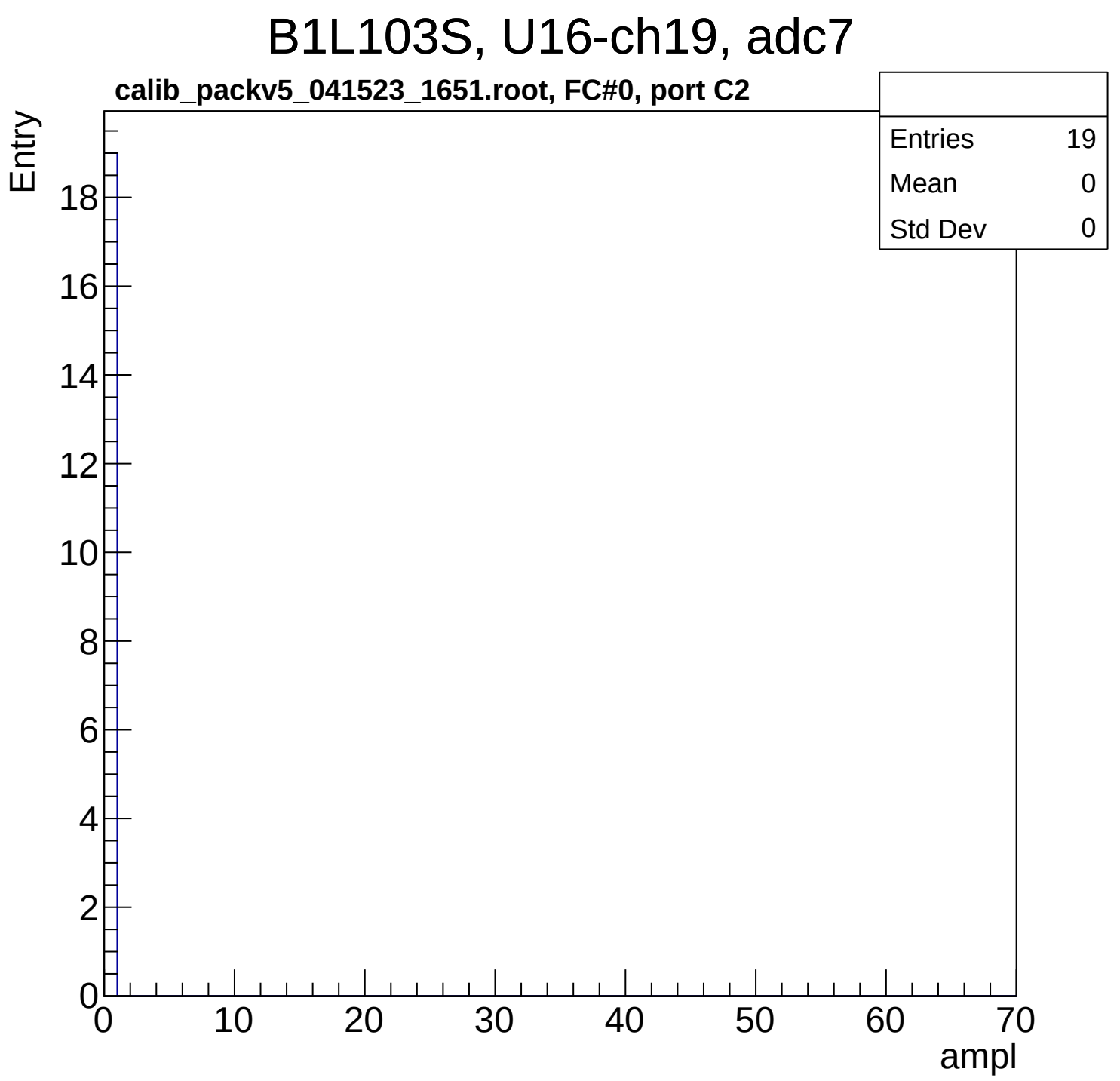
60
70


B1L103S, U16-ch19, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
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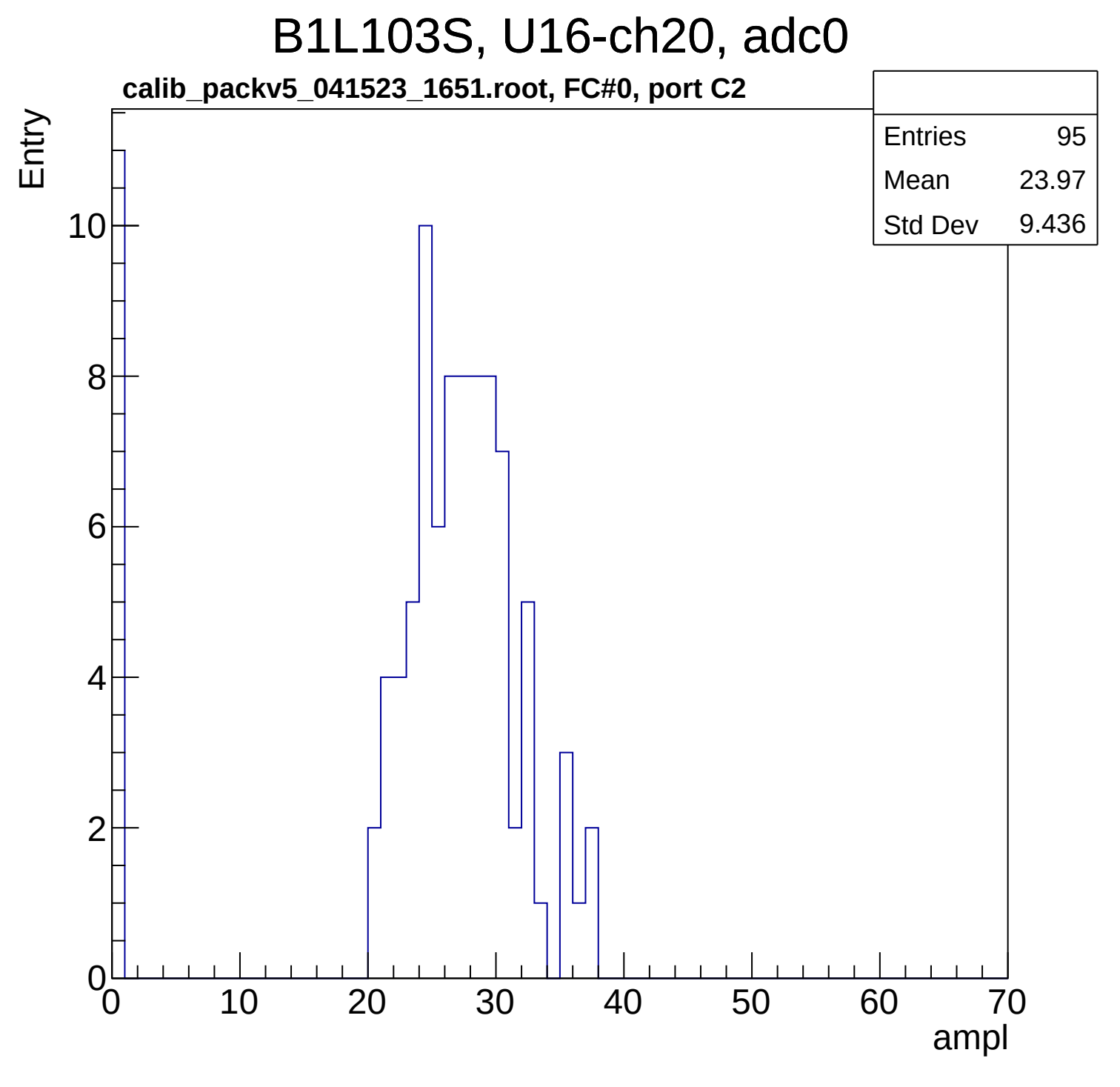
50
60
70
ampl


B1L103S, U16-ch20, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 23.97
Std Dev 9.436
Entry
0
2
4
6
8
10
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10
20
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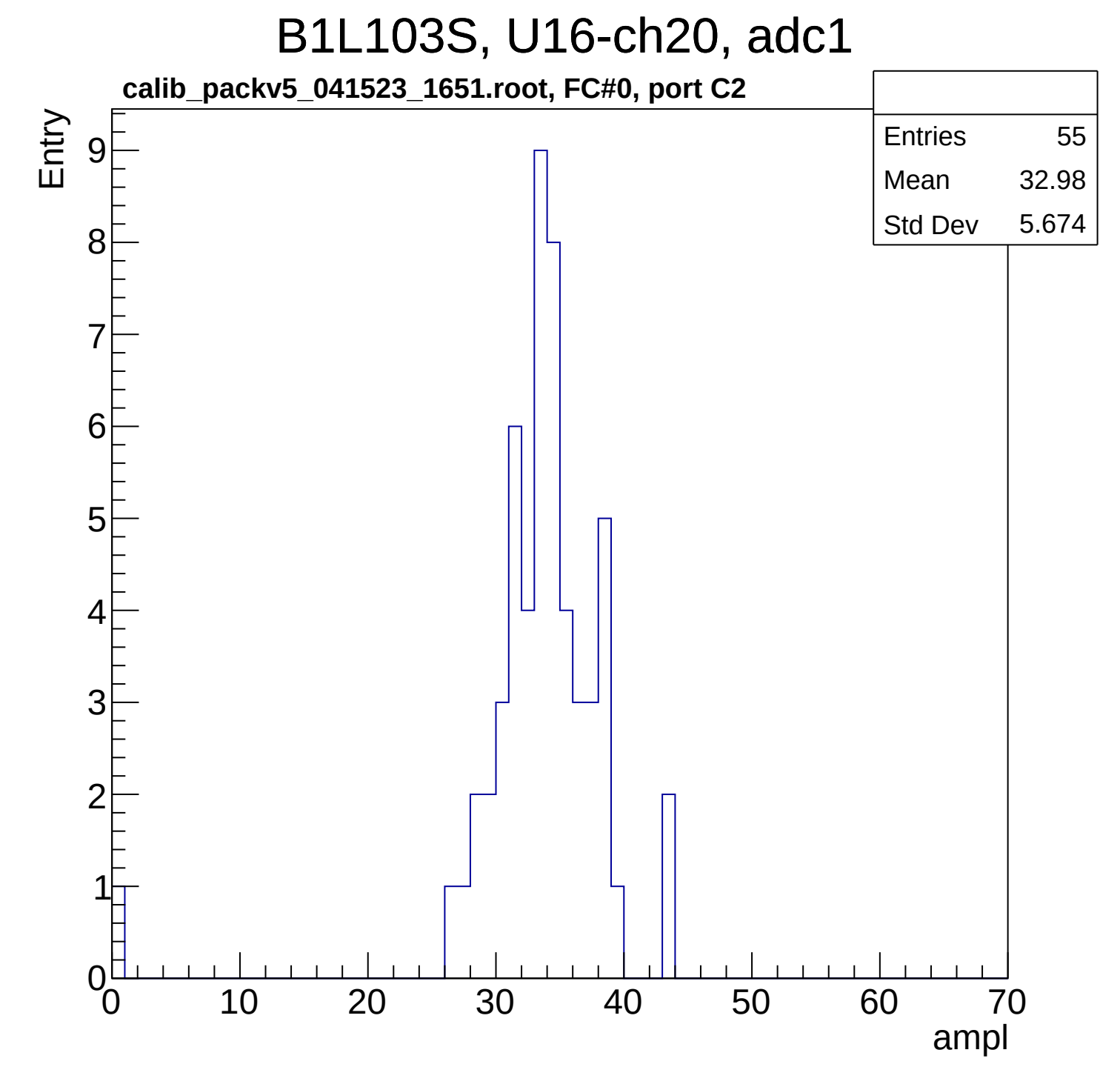
50
60
70
ampl


B1L103S, U16-ch20, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 32.98
Std Dev 5.674
Entry
ampl
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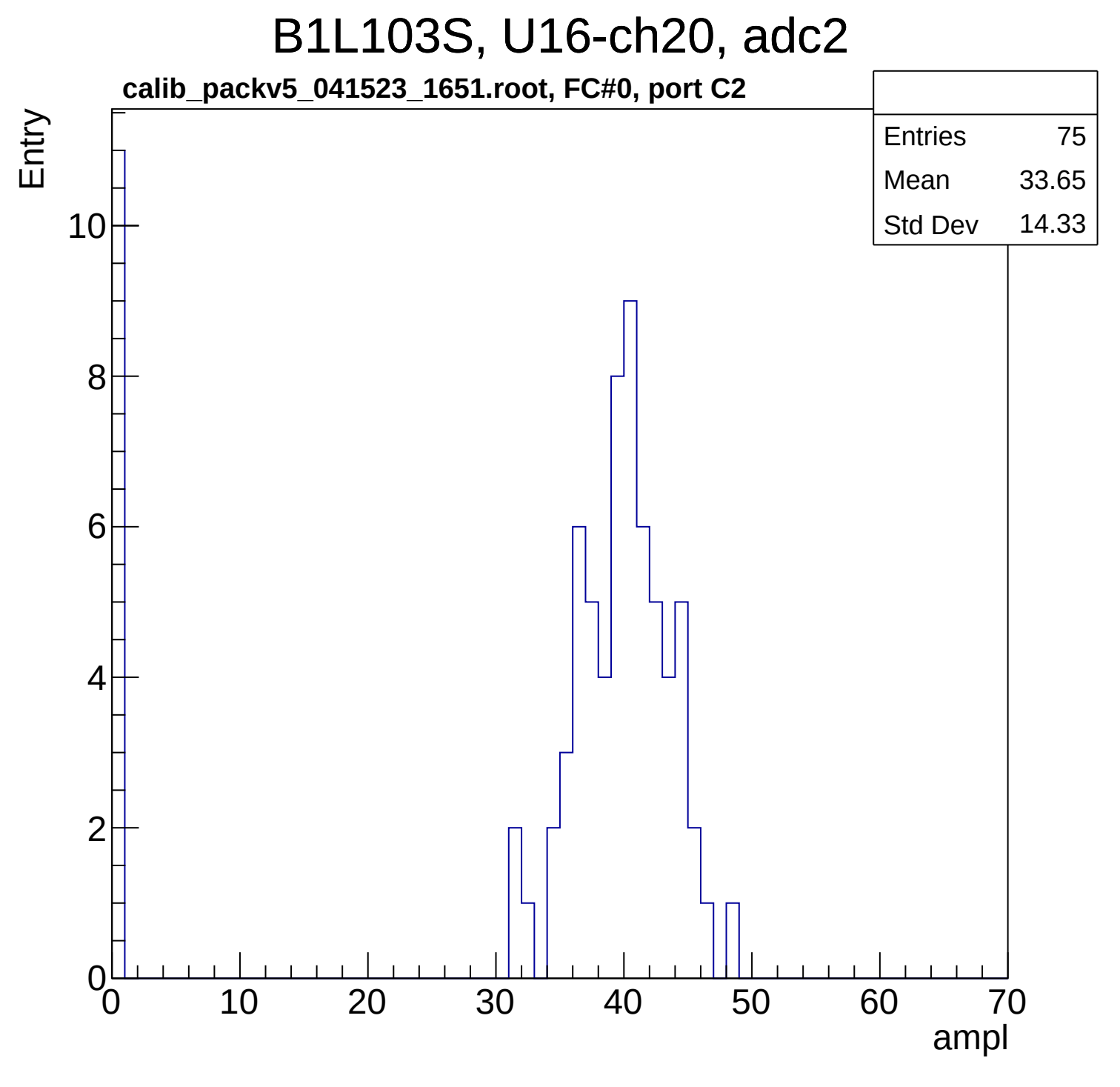
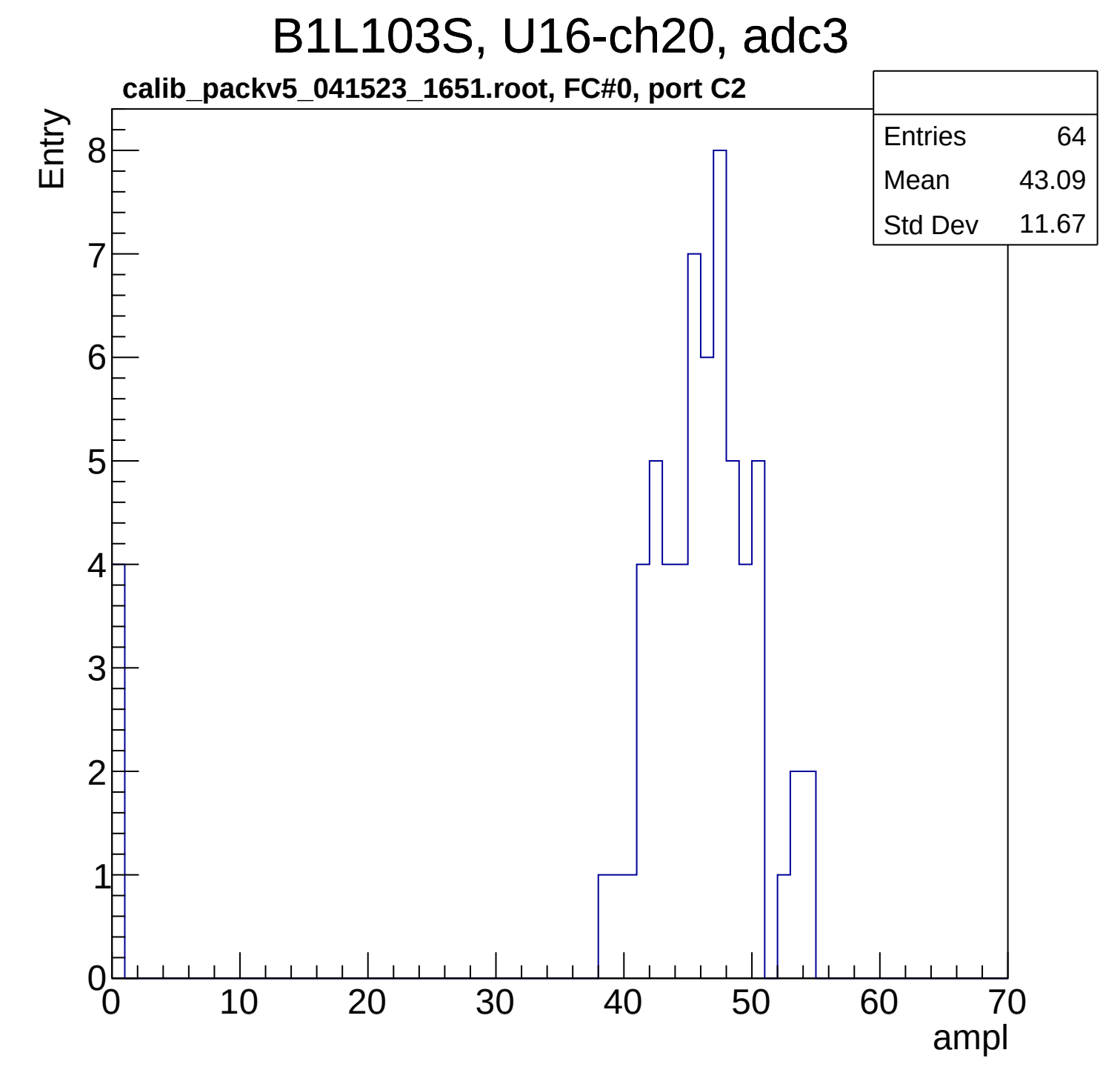
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch20, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 33.65
Std Dev 14.33
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch20, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 43.09
Std Dev 11.67
Entry
ampl
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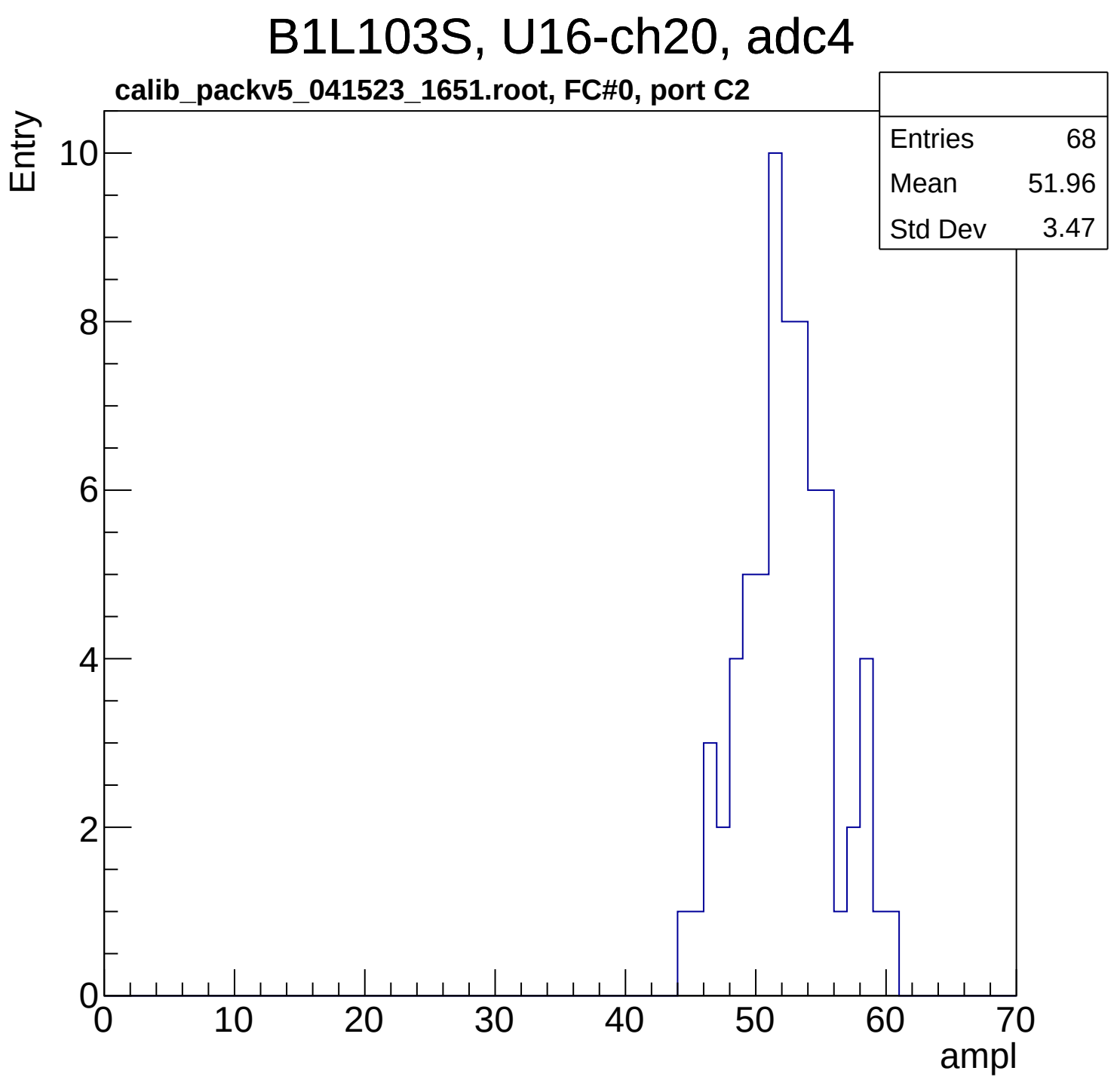
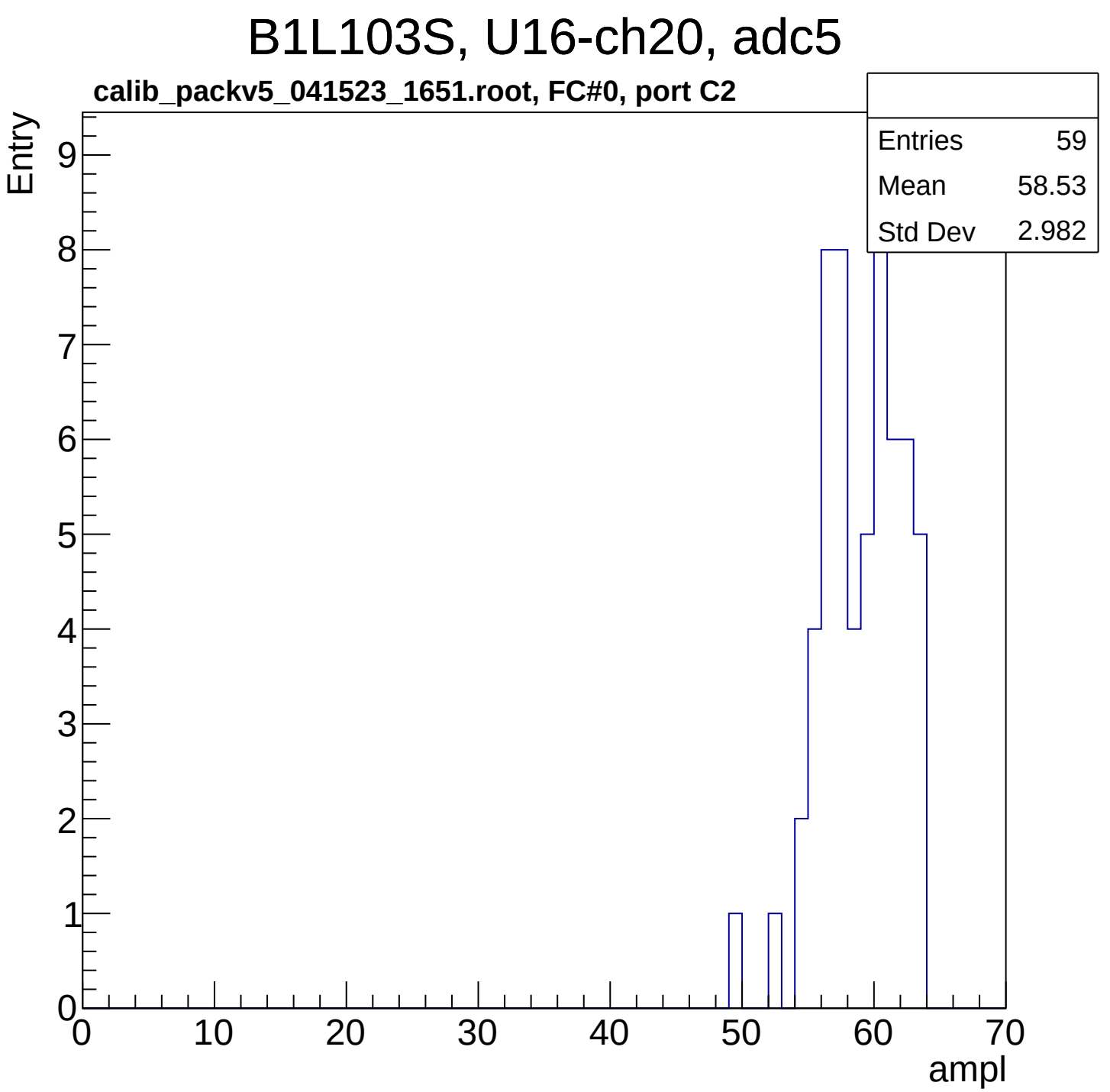
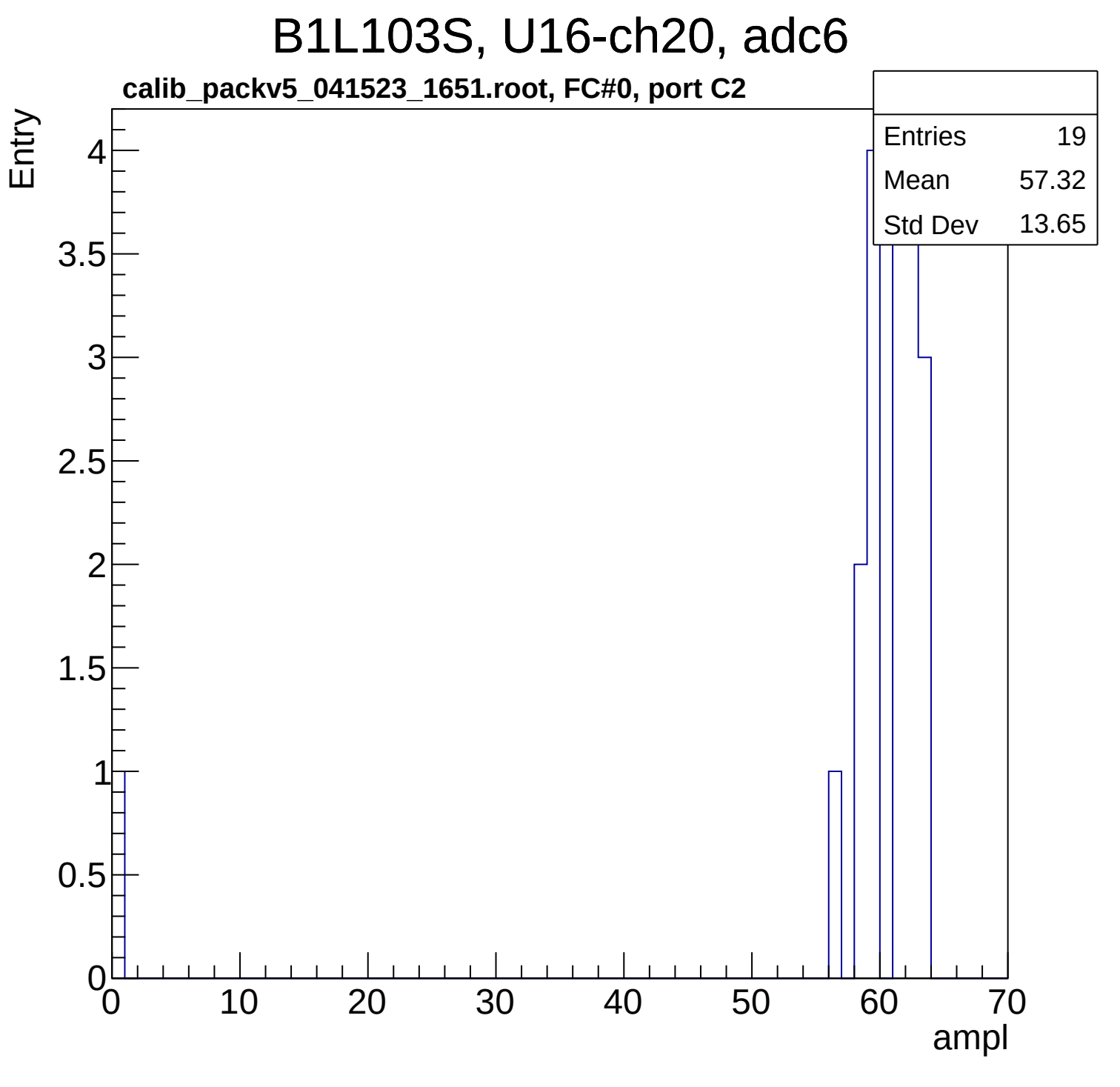
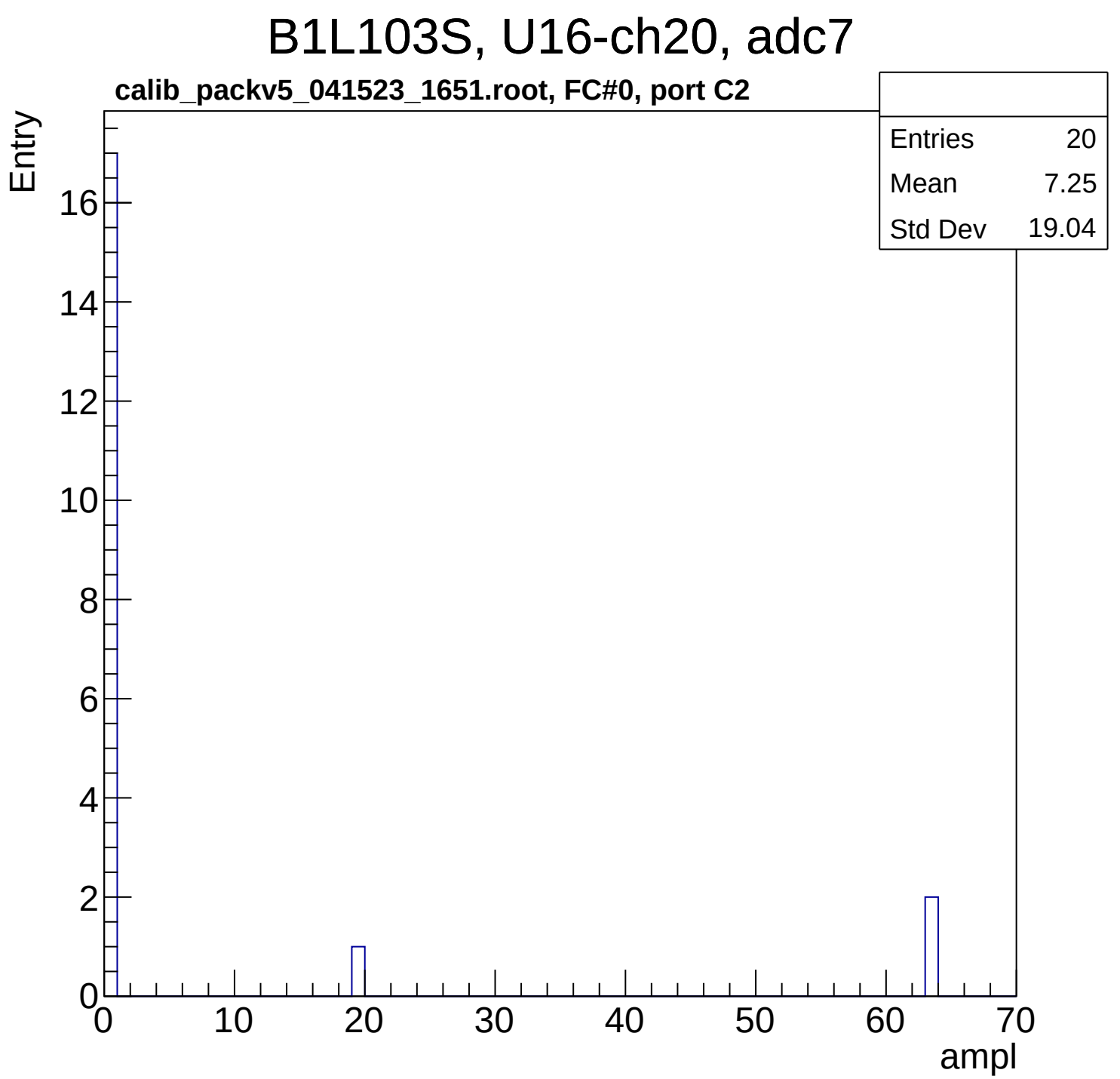
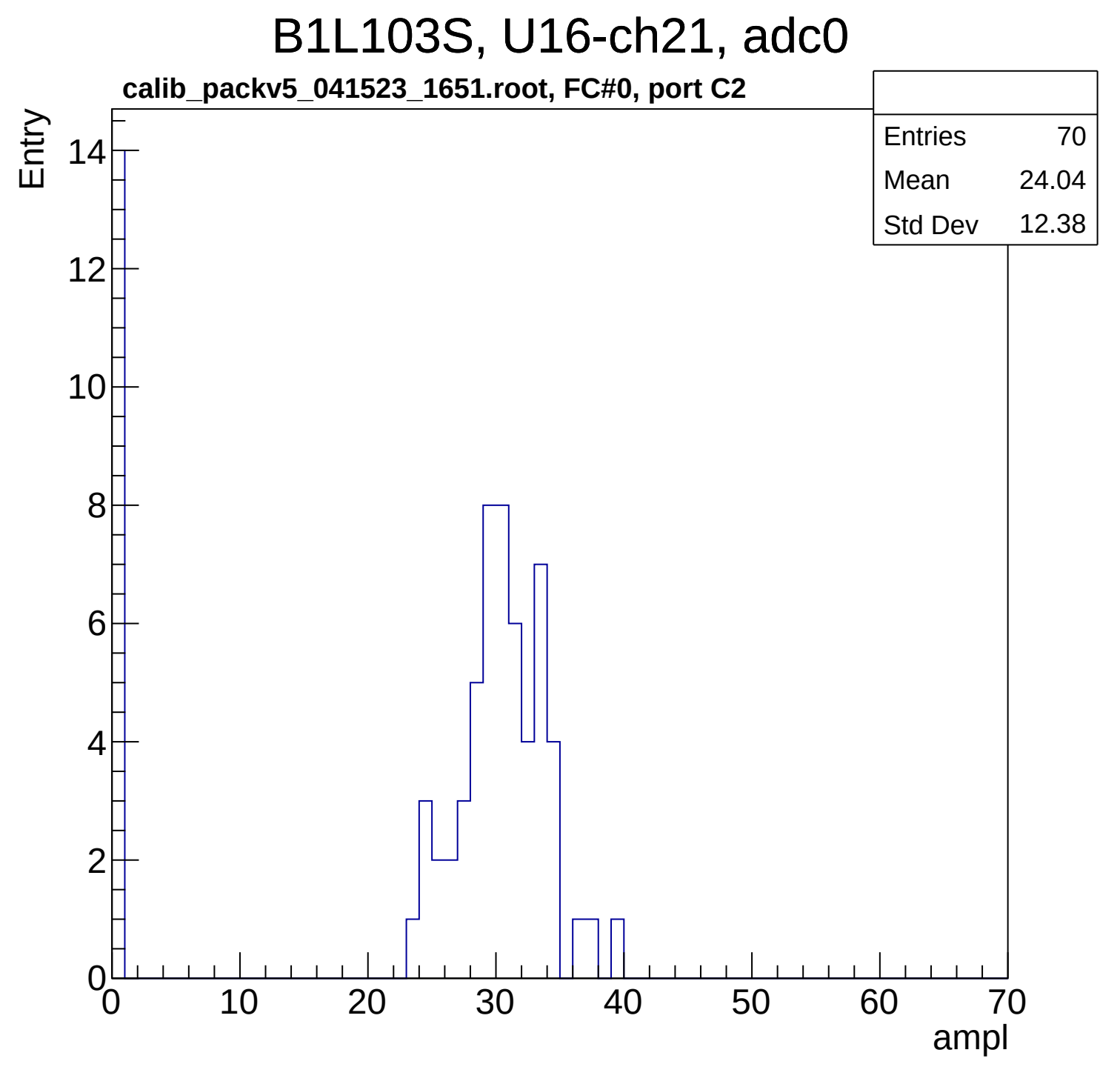
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

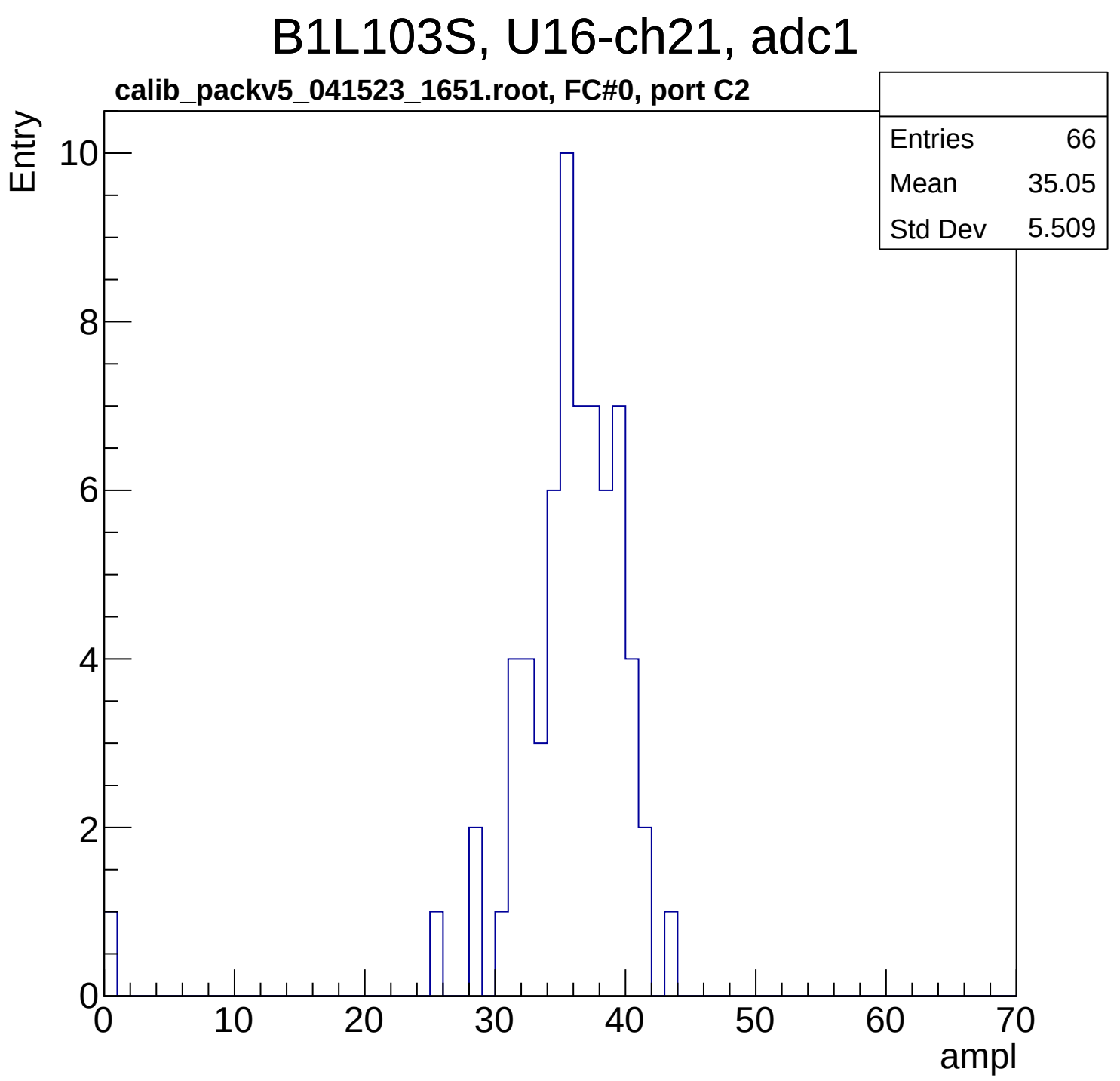

B1L103S, U16-ch20, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 51.96
Std Dev 3.47
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

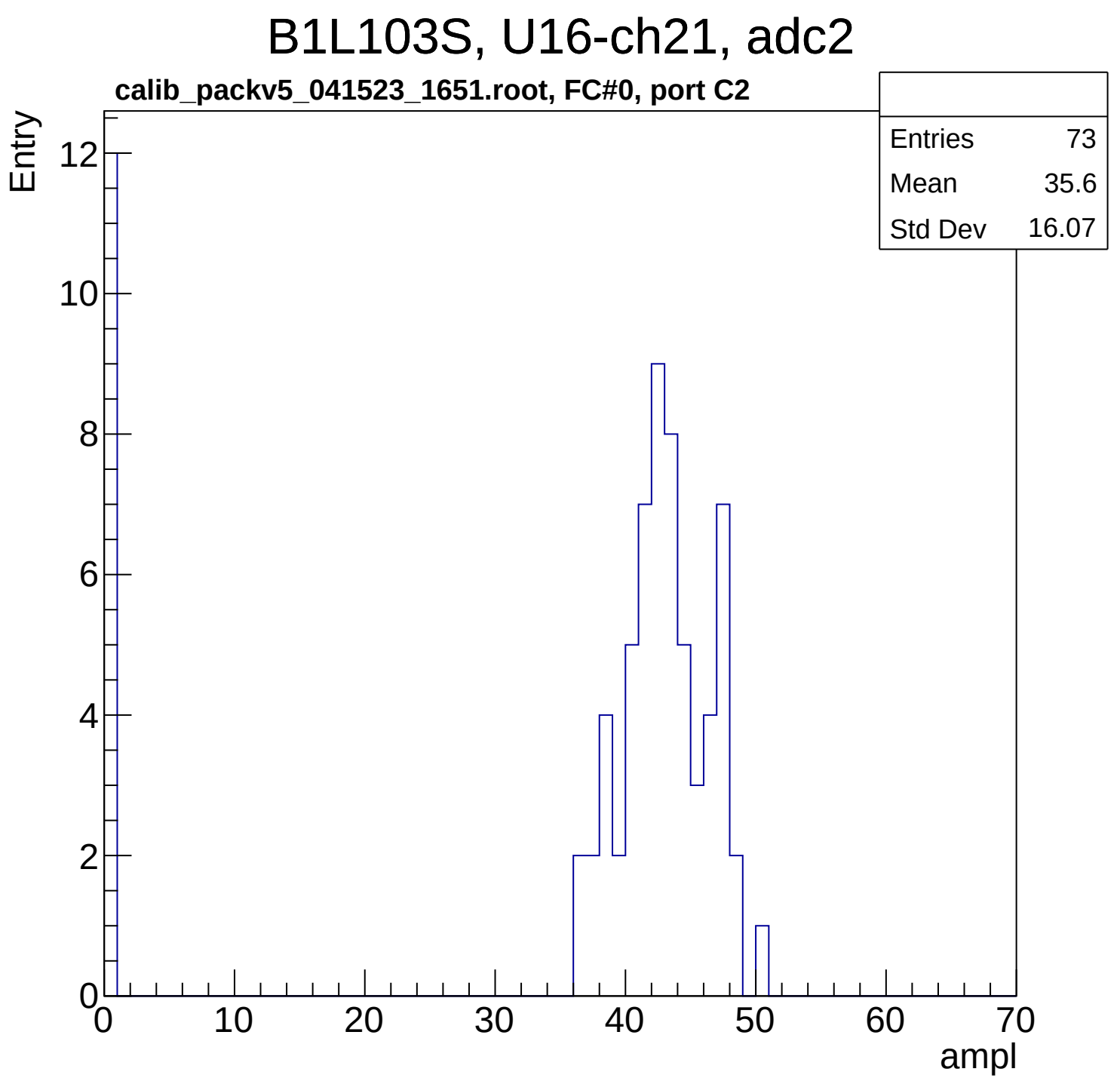

B1L103S, U16-ch20, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 58.53
Std Dev 2.982
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

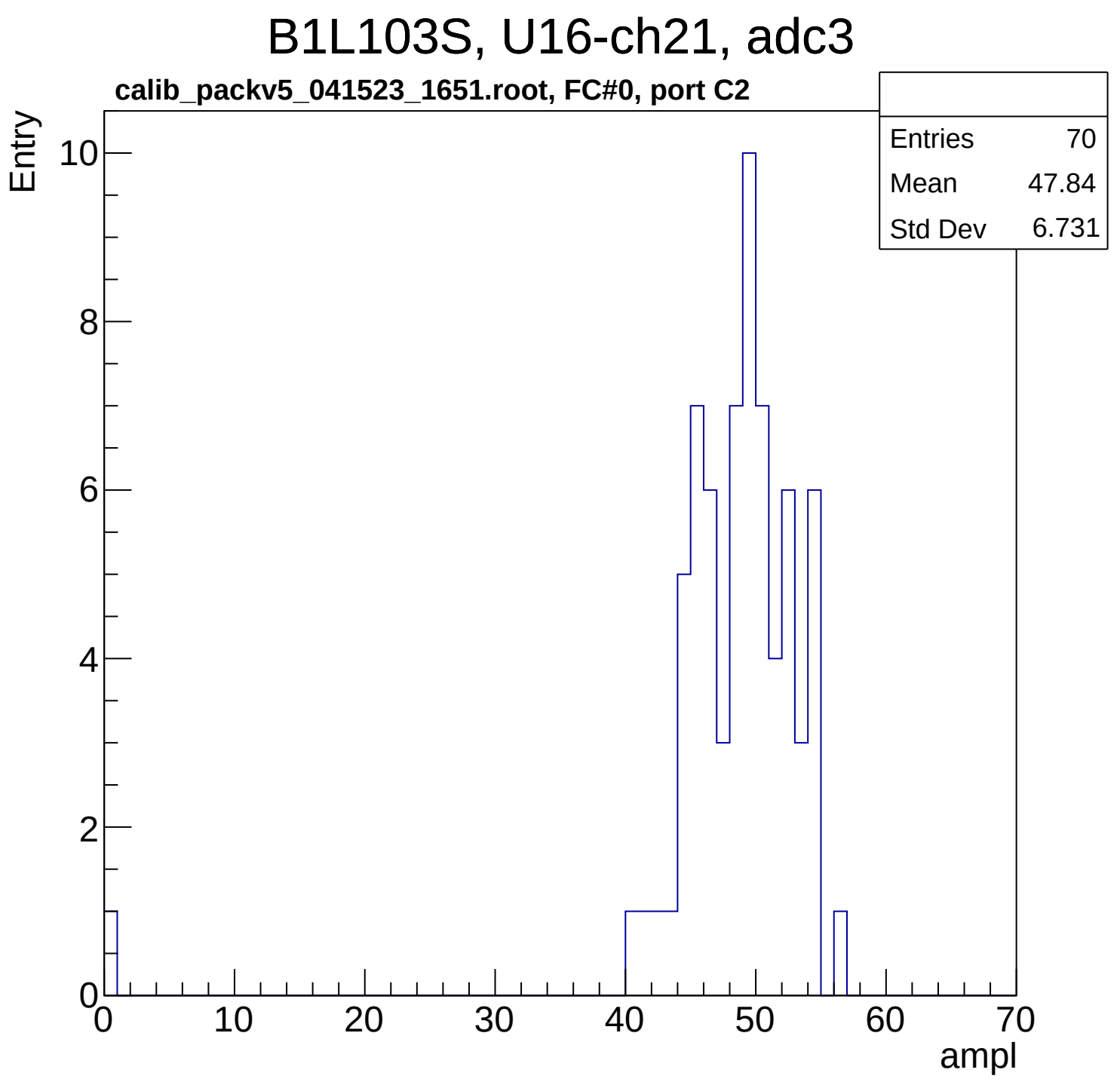

B1L103S, U16-ch20, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 57.32
Std Dev 13.65
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

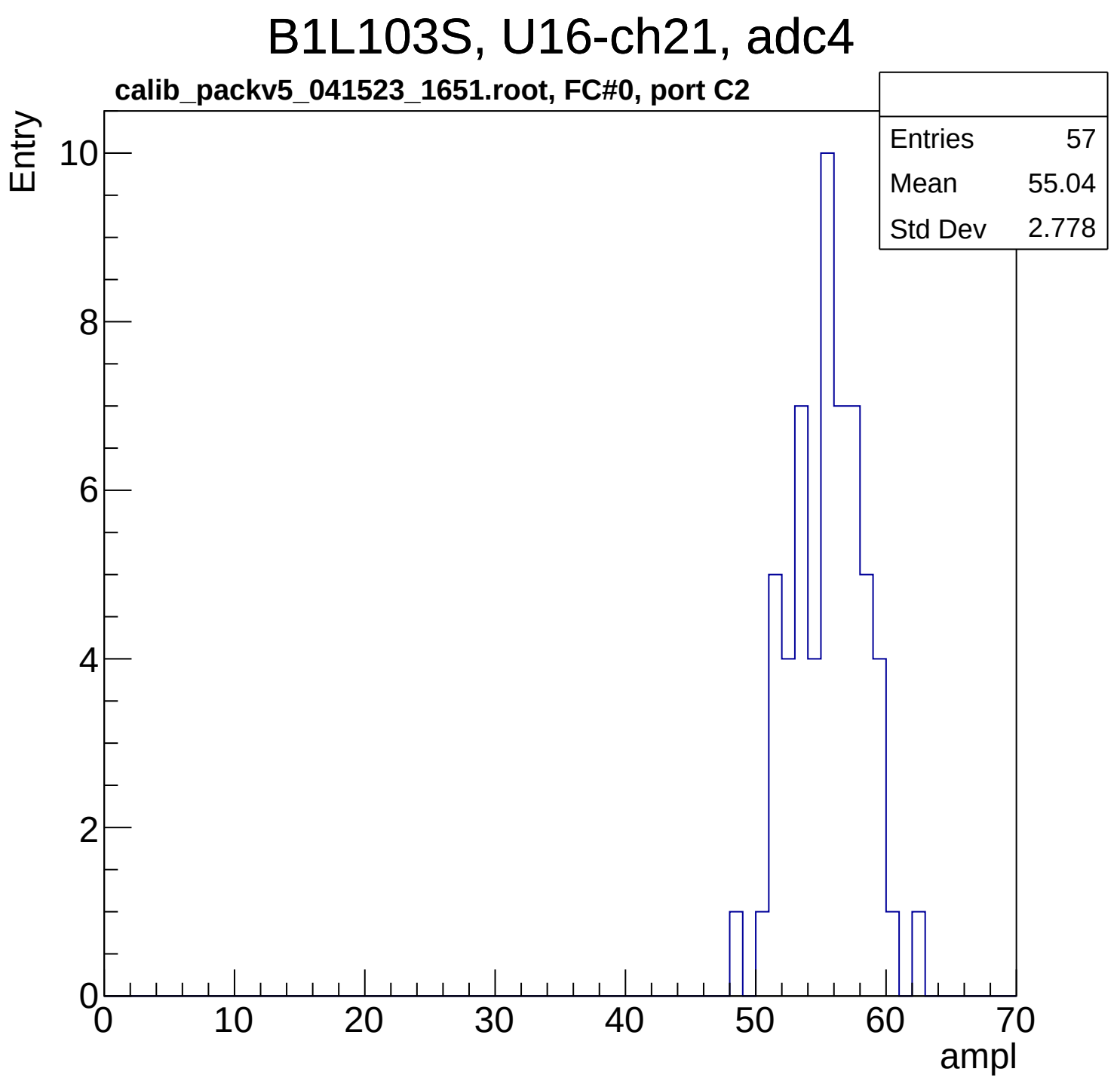

B1L103S, U16-ch20, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 7.25
Std Dev 19.04
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

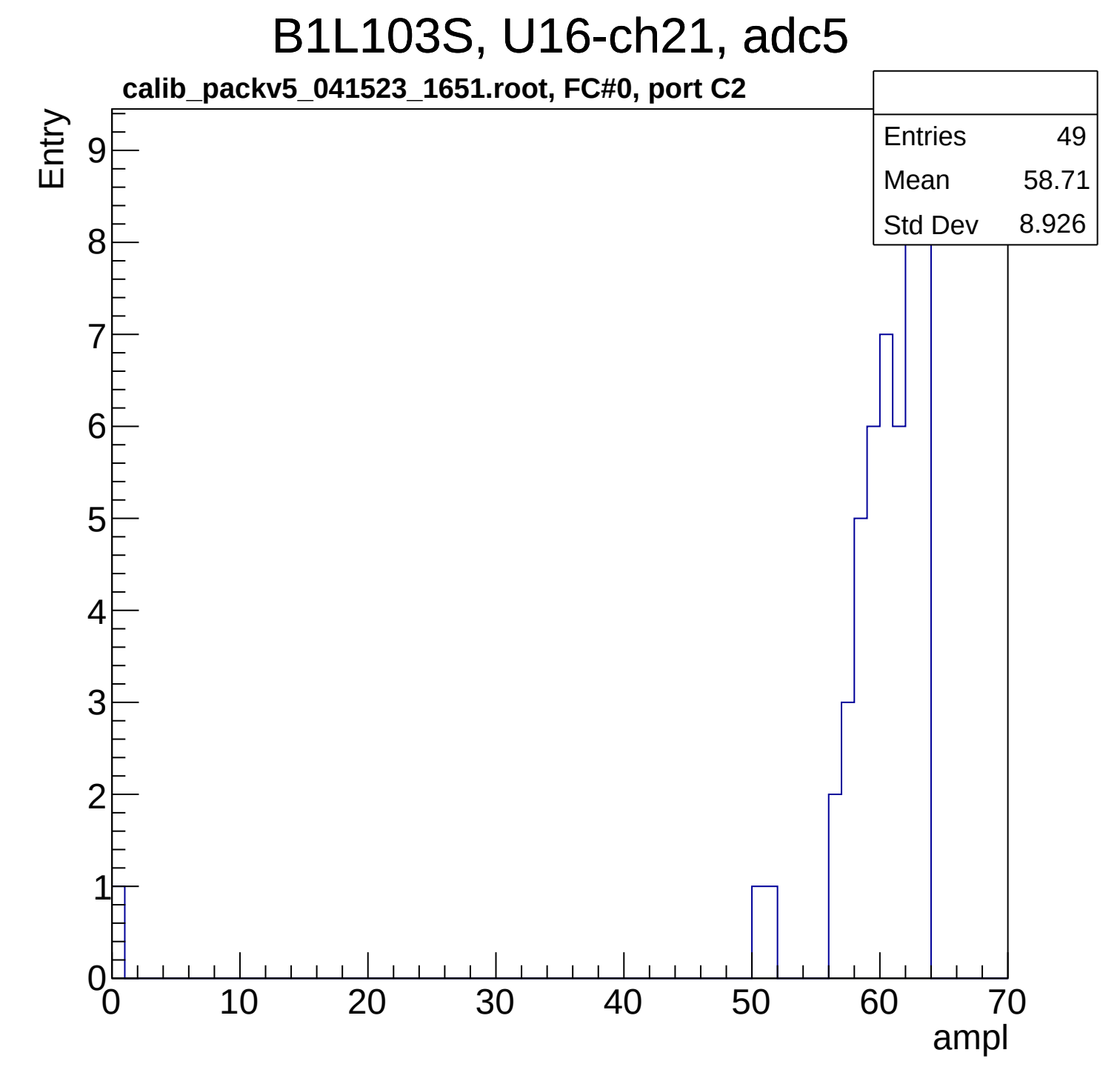

B1L103S, U16-ch21, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 24.04
Std Dev 12.38
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

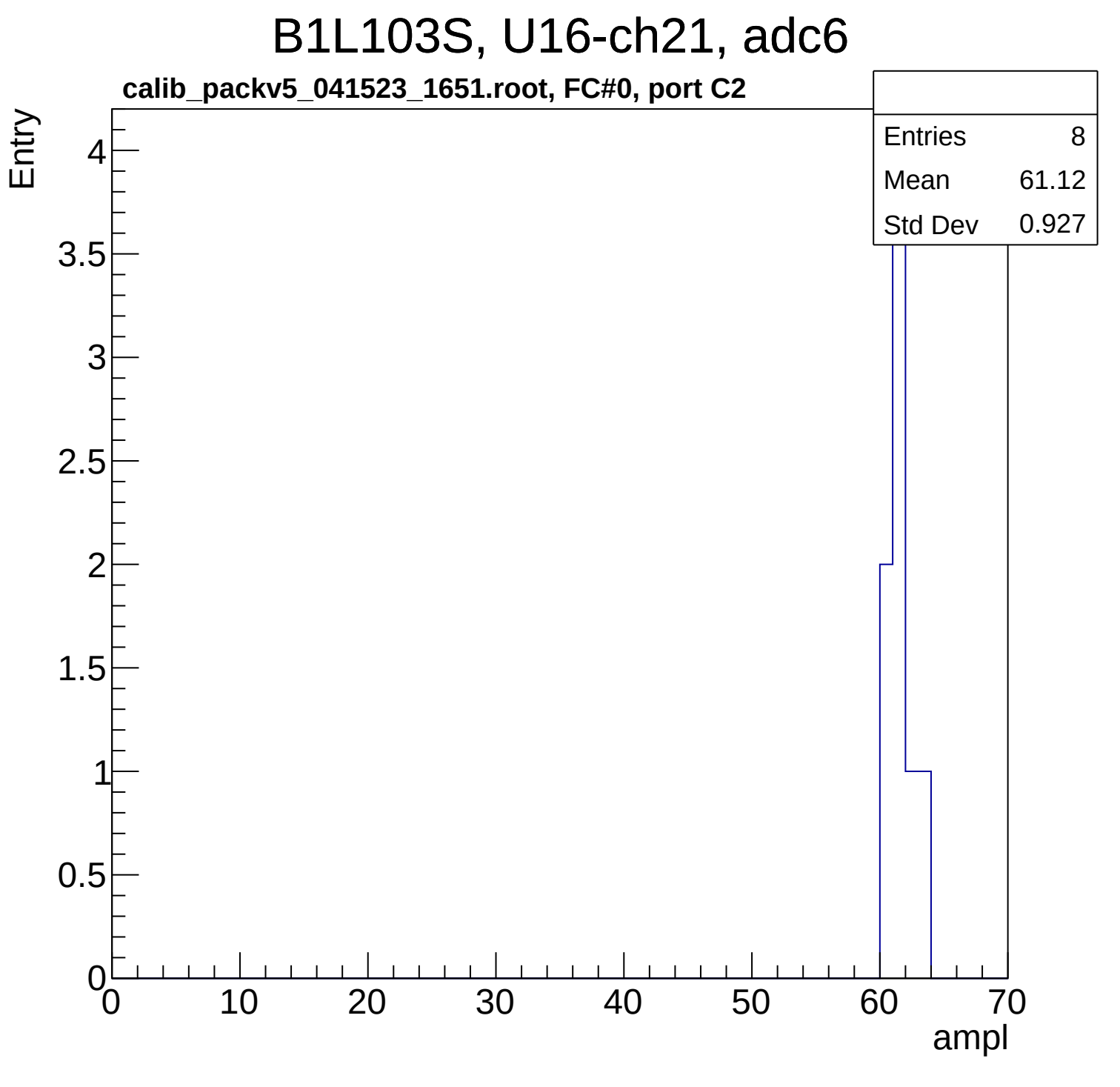

B1L103S, U16-ch21, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 35.05
Std Dev 5.509
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch21, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 35.6
Std Dev 16.07
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch21, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 47.84
Std Dev 6.731
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch21, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 55.04
Std Dev 2.778
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch21, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.71
Std Dev 8.926
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch21, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.12
Std Dev 0.927
Entry
ampl
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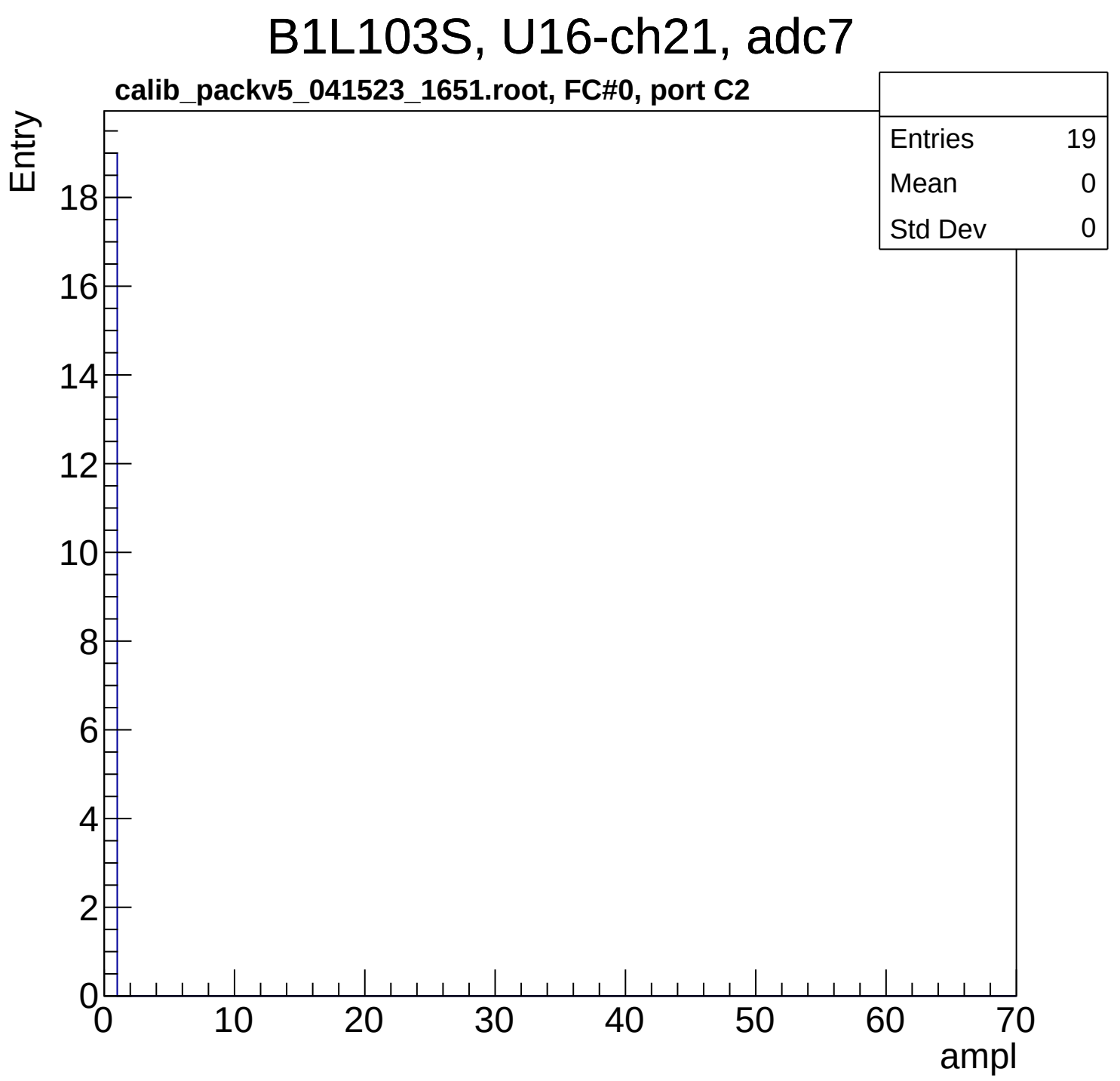
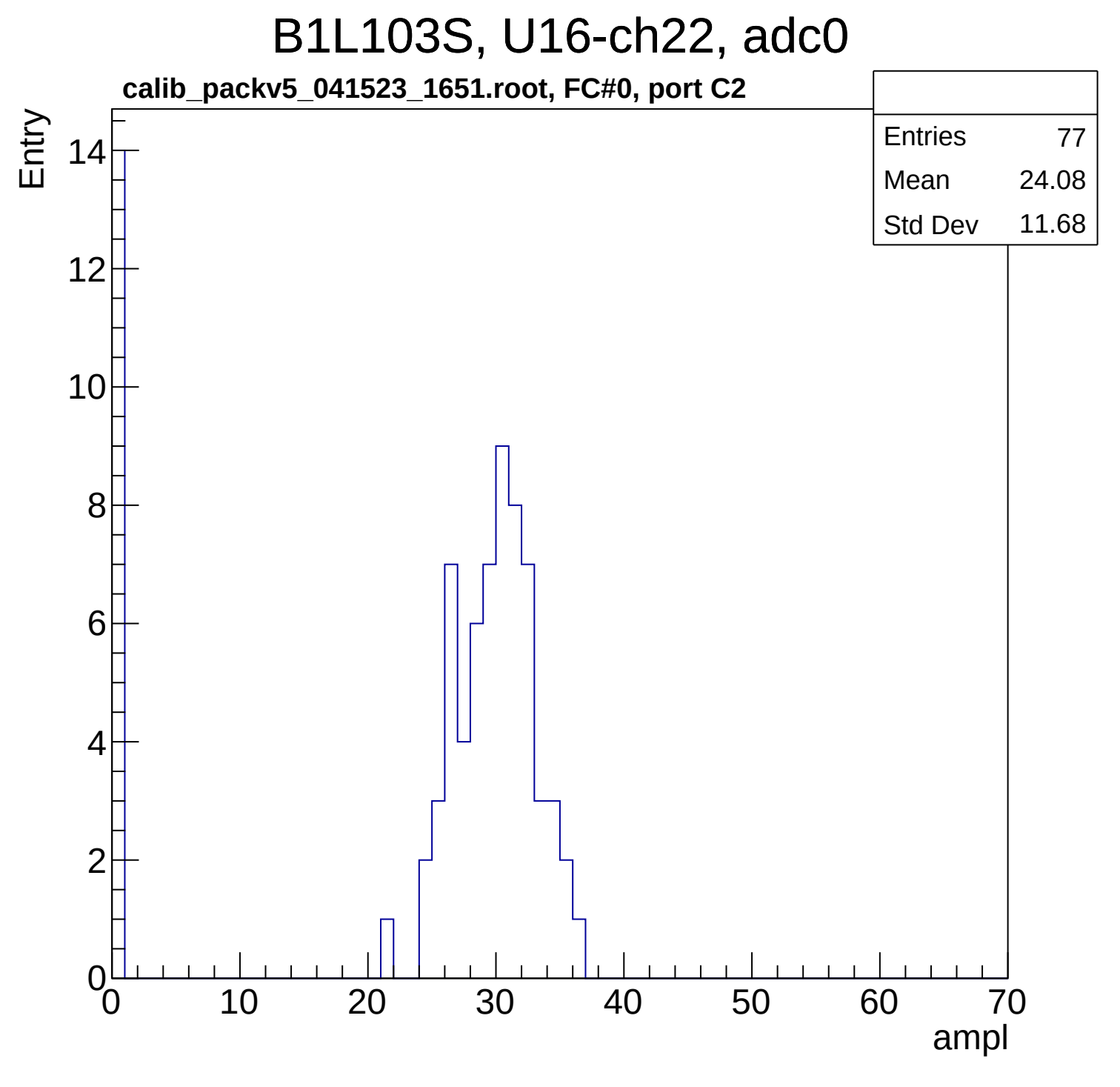
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U16-ch21, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch22, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 24.08
Std Dev 11.68
Entry
ampl
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2
4
6
8
10
12
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0
10
20
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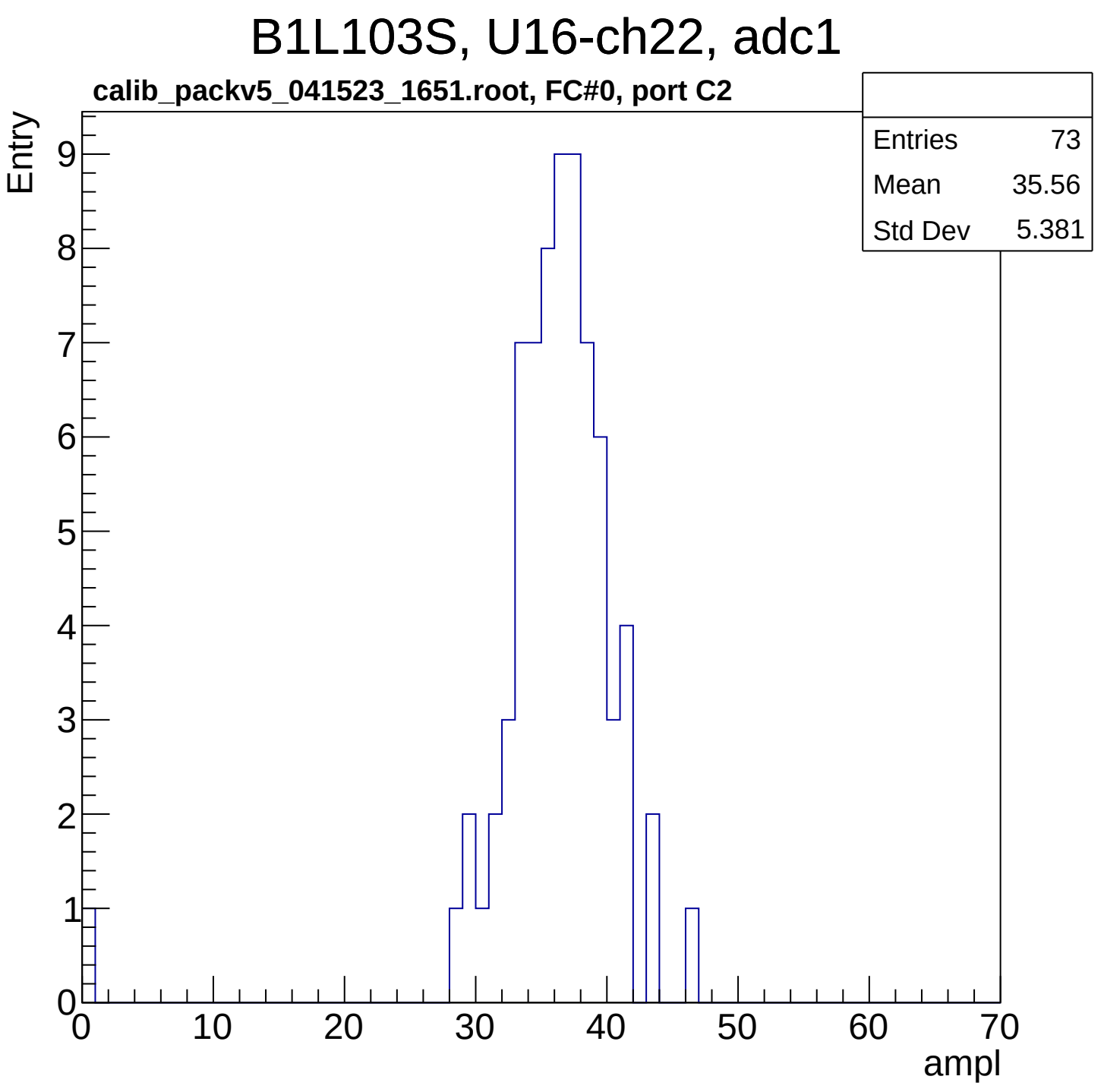
40
50
60
70


B1L103S, U16-ch22, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 35.56
Std Dev 5.381
Entry
ampl
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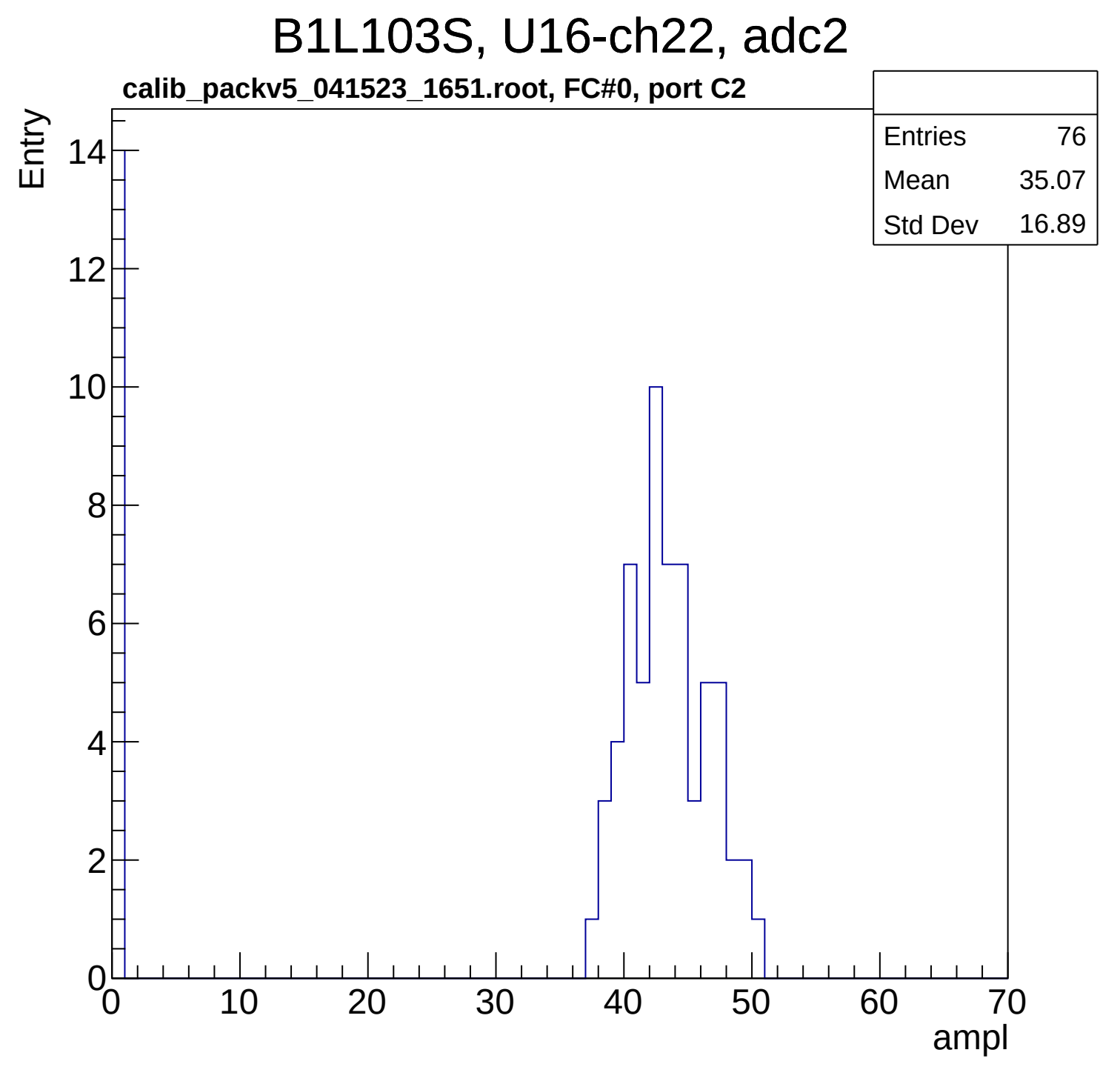
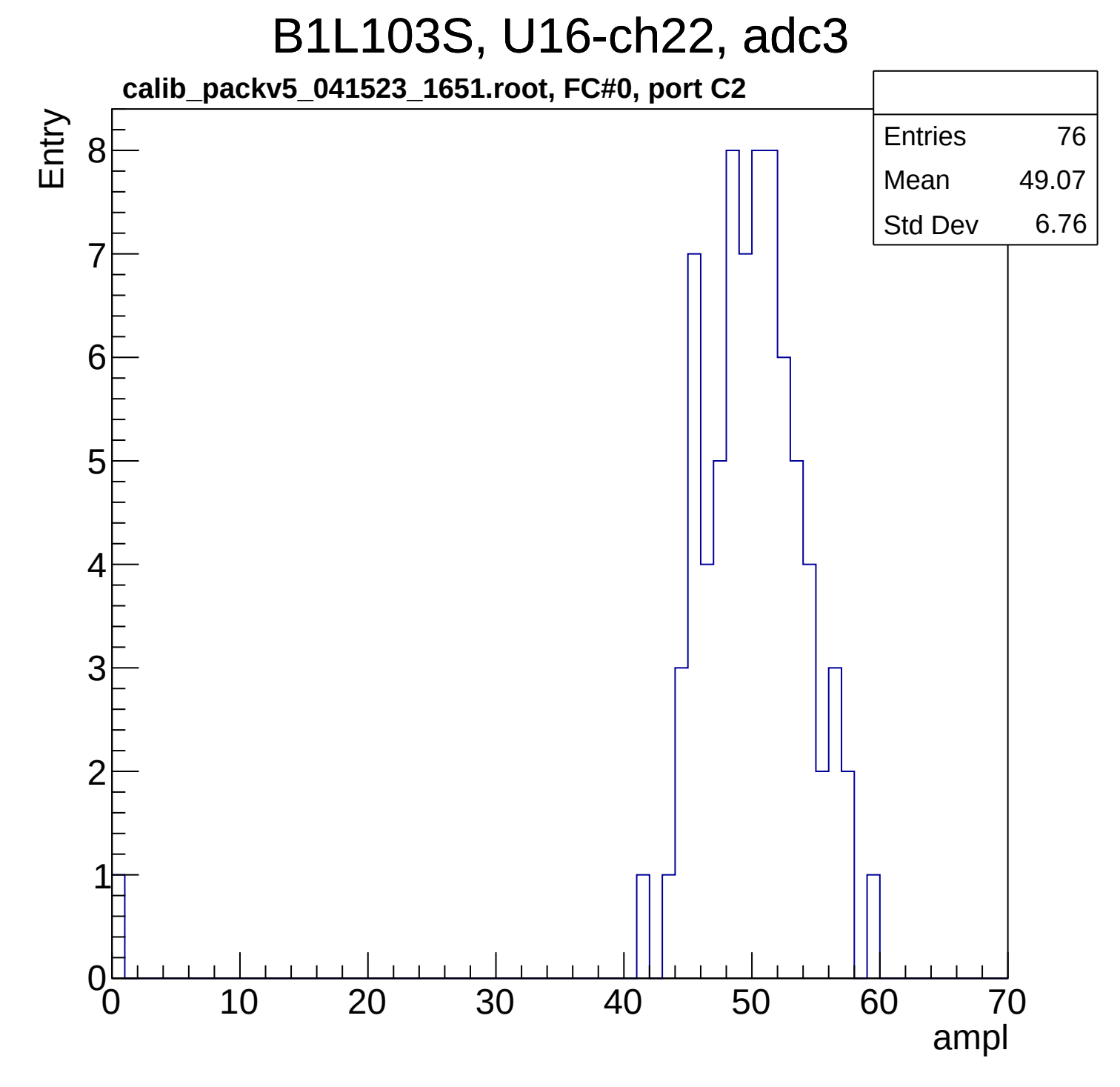
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch22, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 35.07
Std Dev 16.89
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch22, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 49.07
Std Dev 6.76
Entry
ampl
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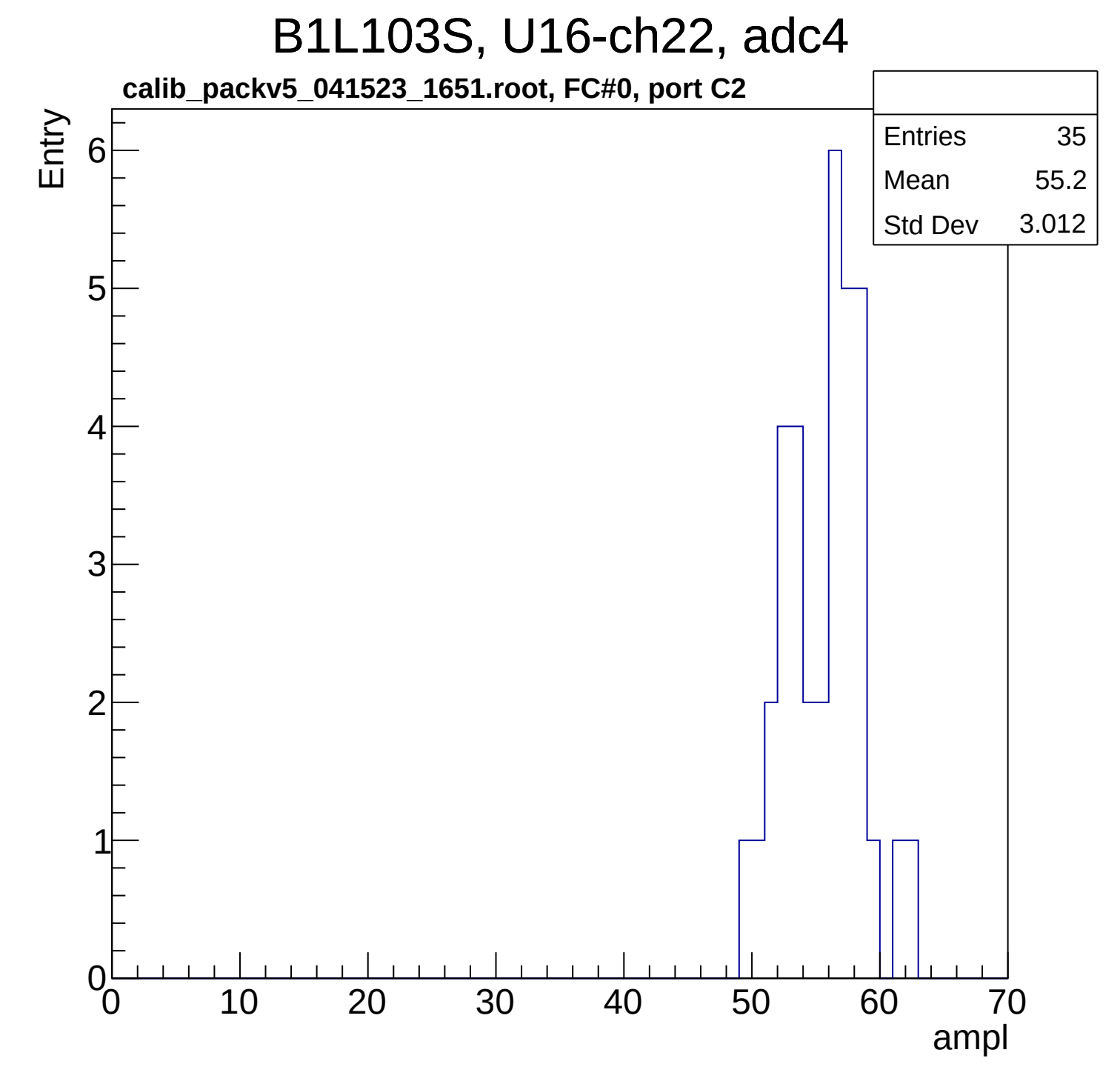
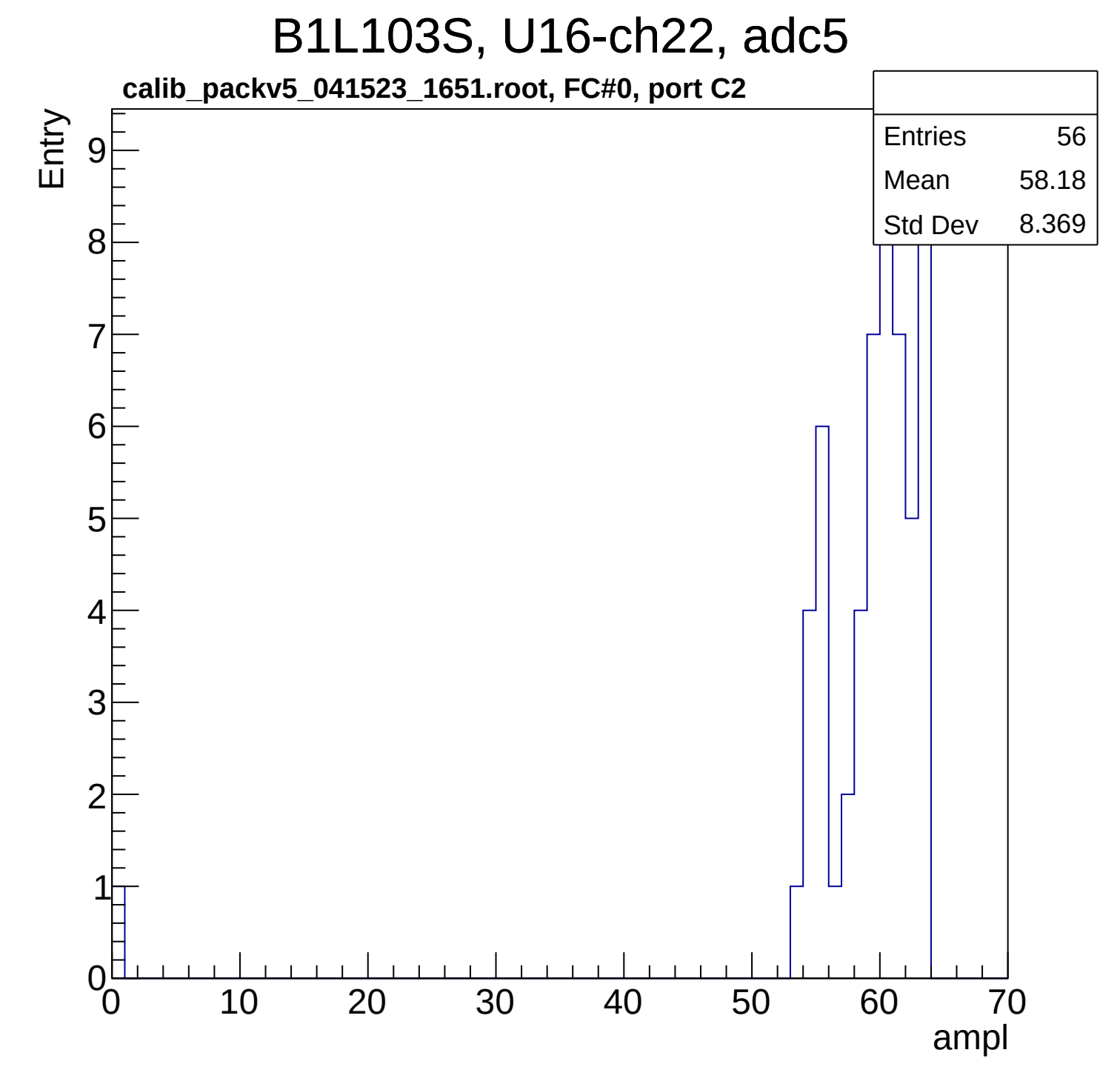
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch22, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 55.2
Std Dev 3.012
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch22, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.18
Std Dev 8.369
Entry
ampl
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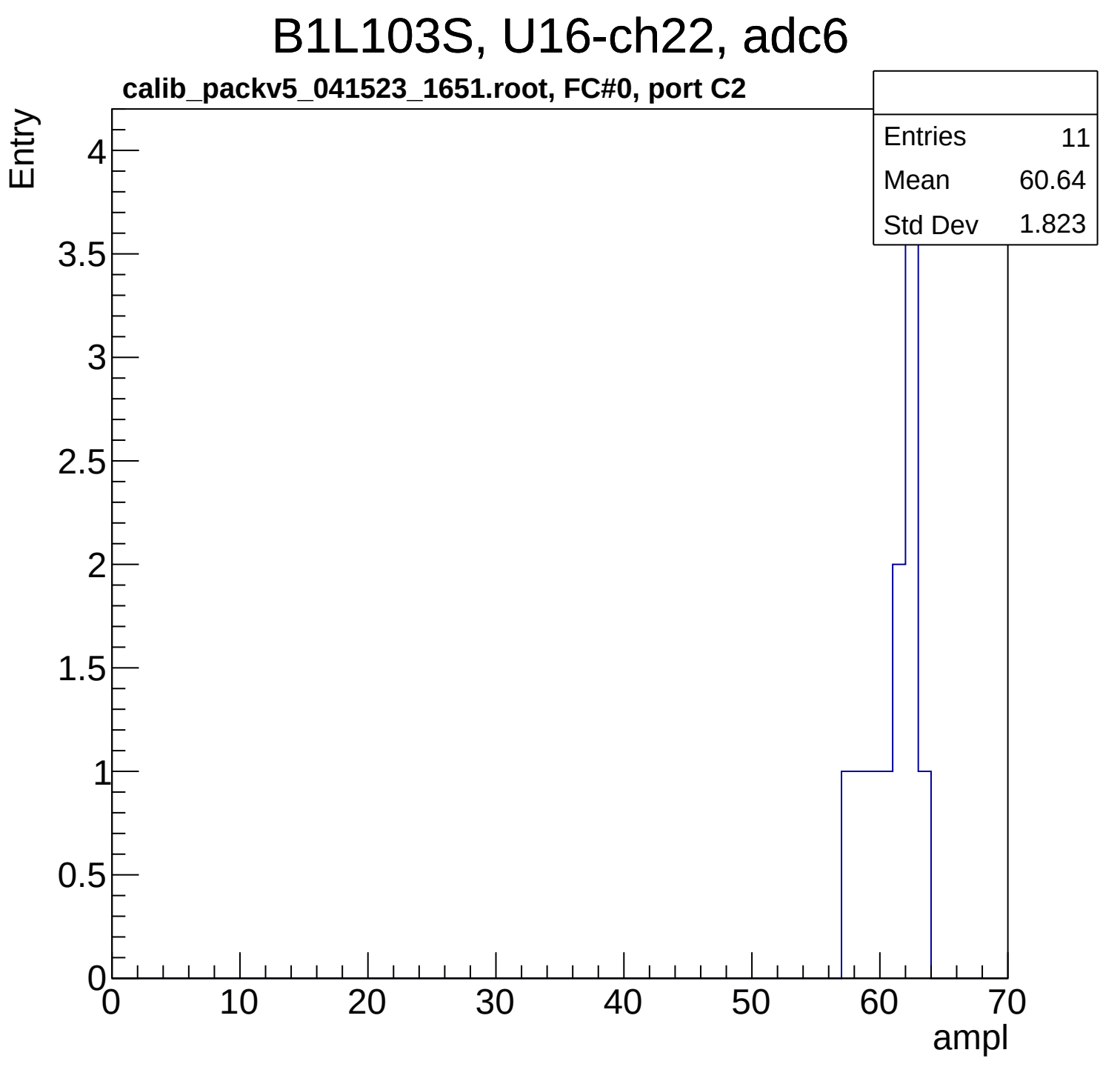
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch22, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 60.64
Std Dev 1.823
Entry
ampl
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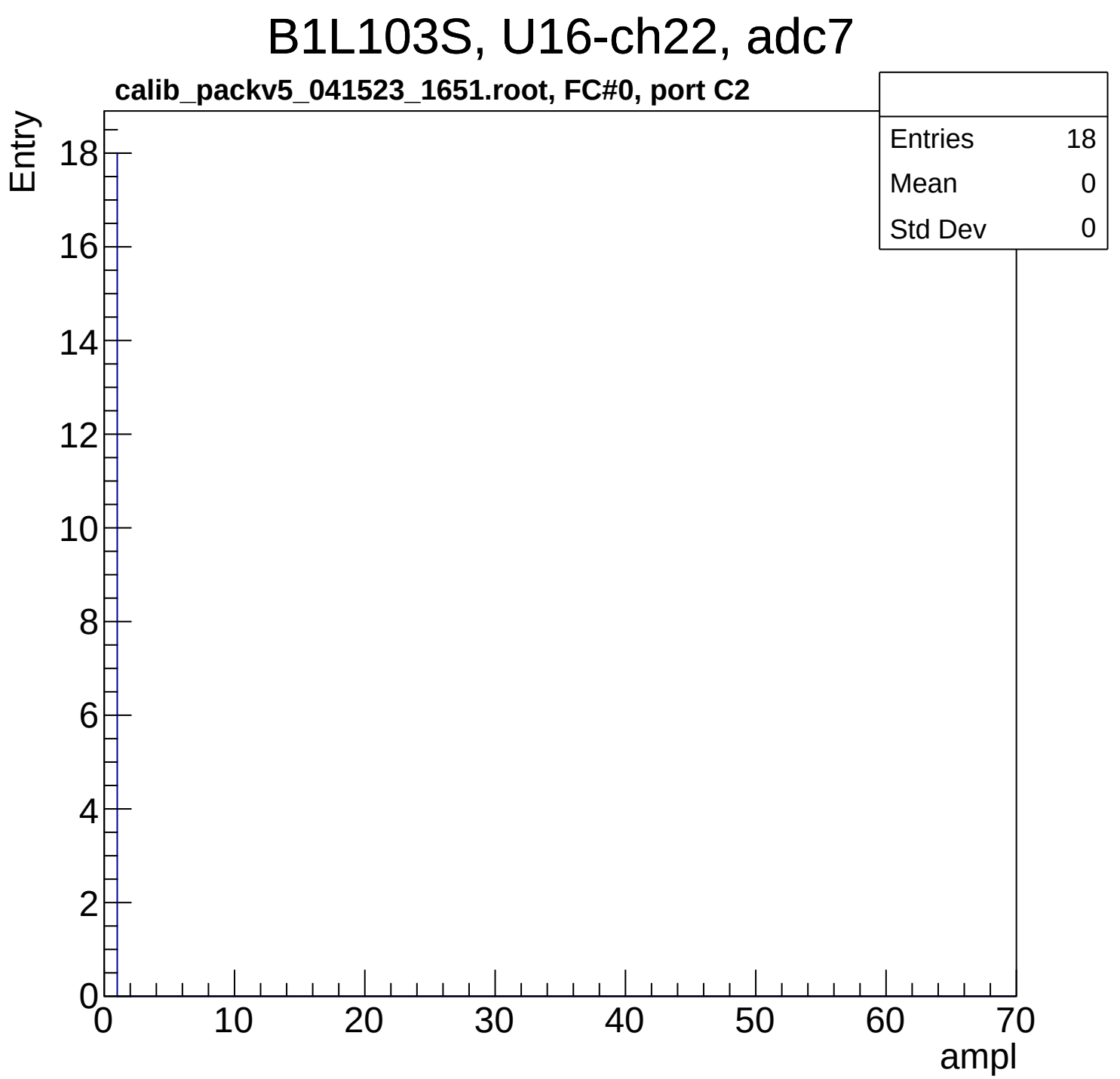
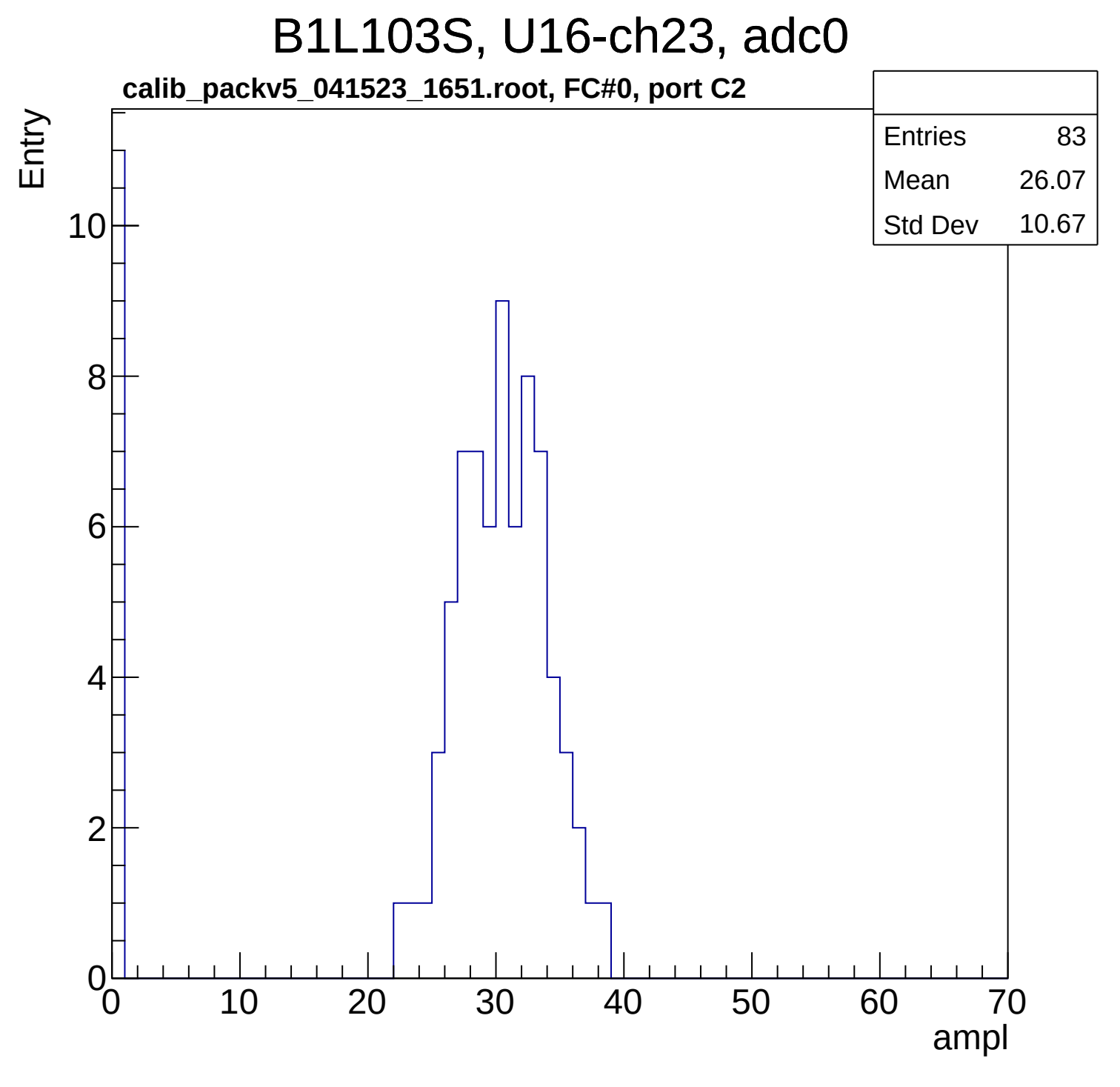
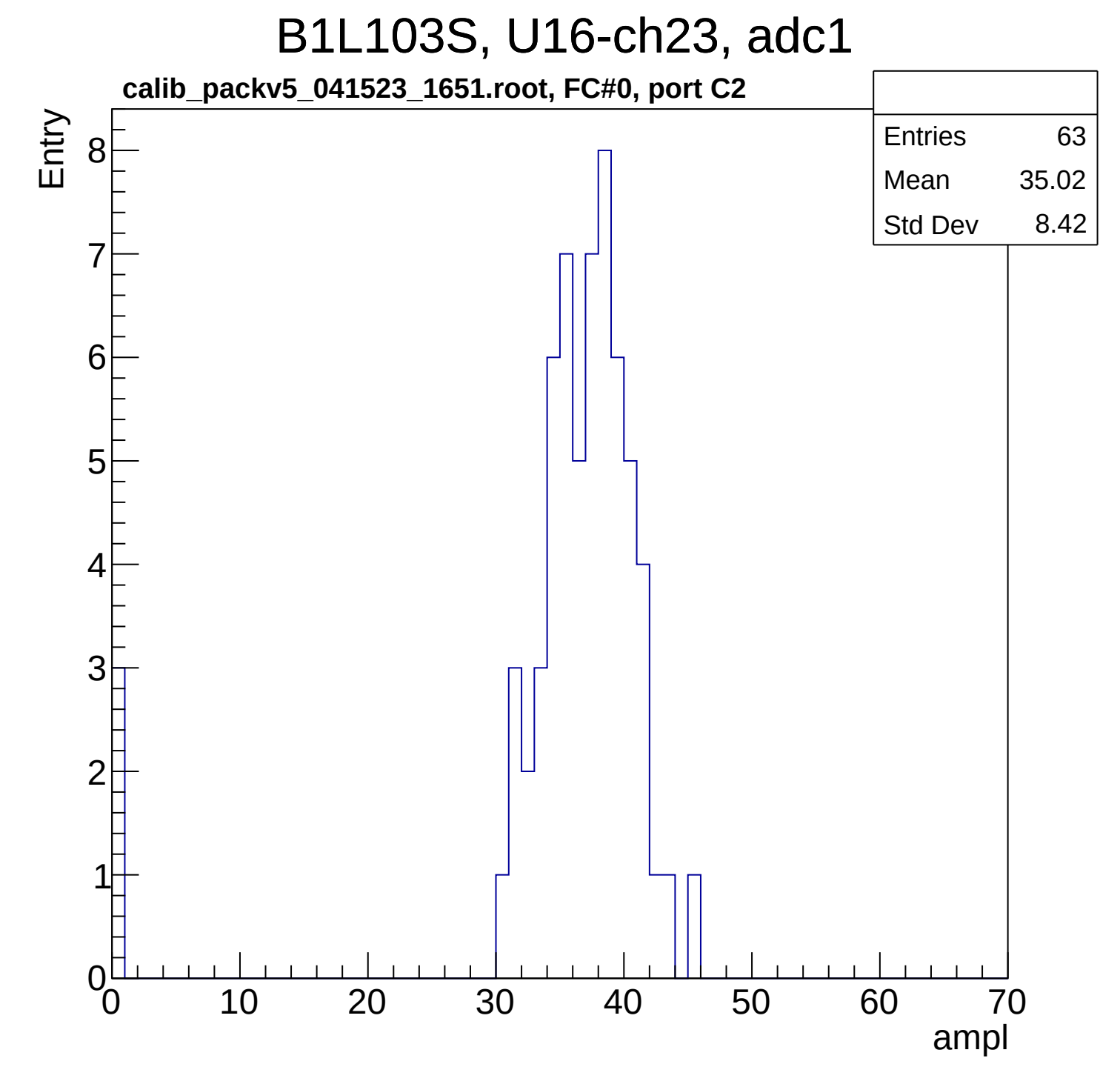
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U16-ch22, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch23, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 26.07
Std Dev 10.67
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch23, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 35.02
Std Dev 8.42
Entry
ampl
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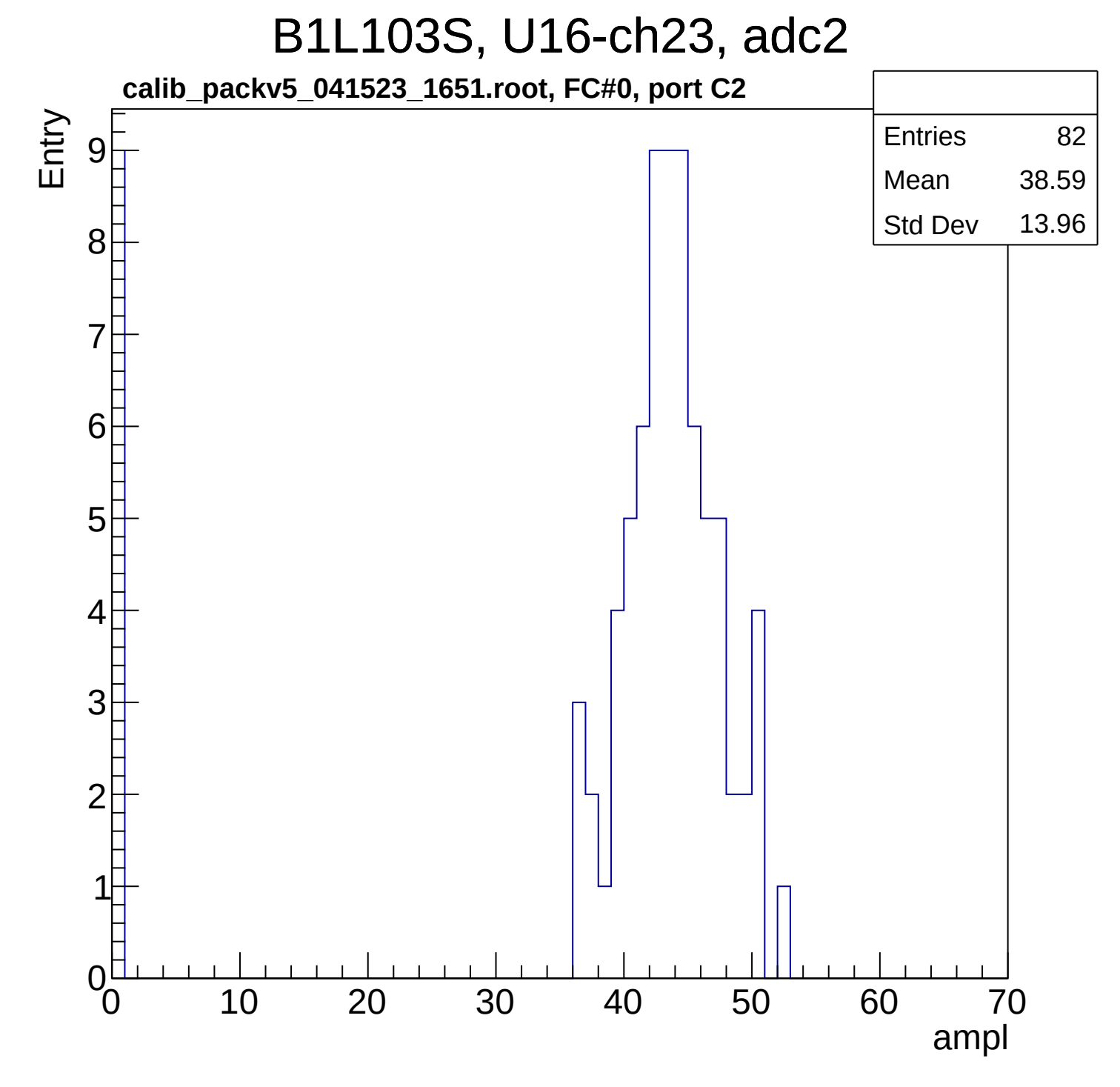
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch23, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 38.59
Std Dev 13.96
Entry
ampl
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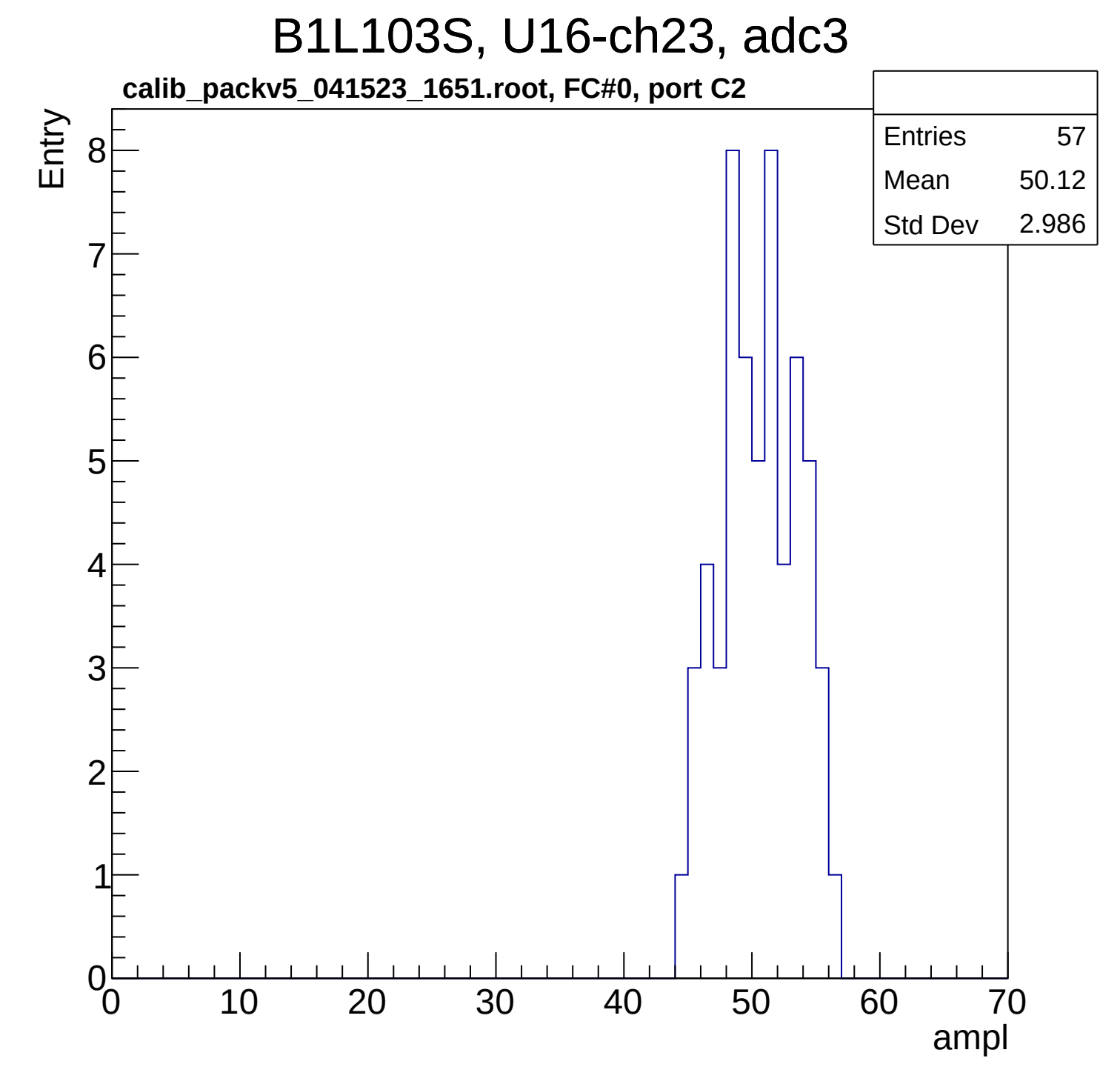
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch23, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 50.12
Std Dev 2.986
Entry
ampl
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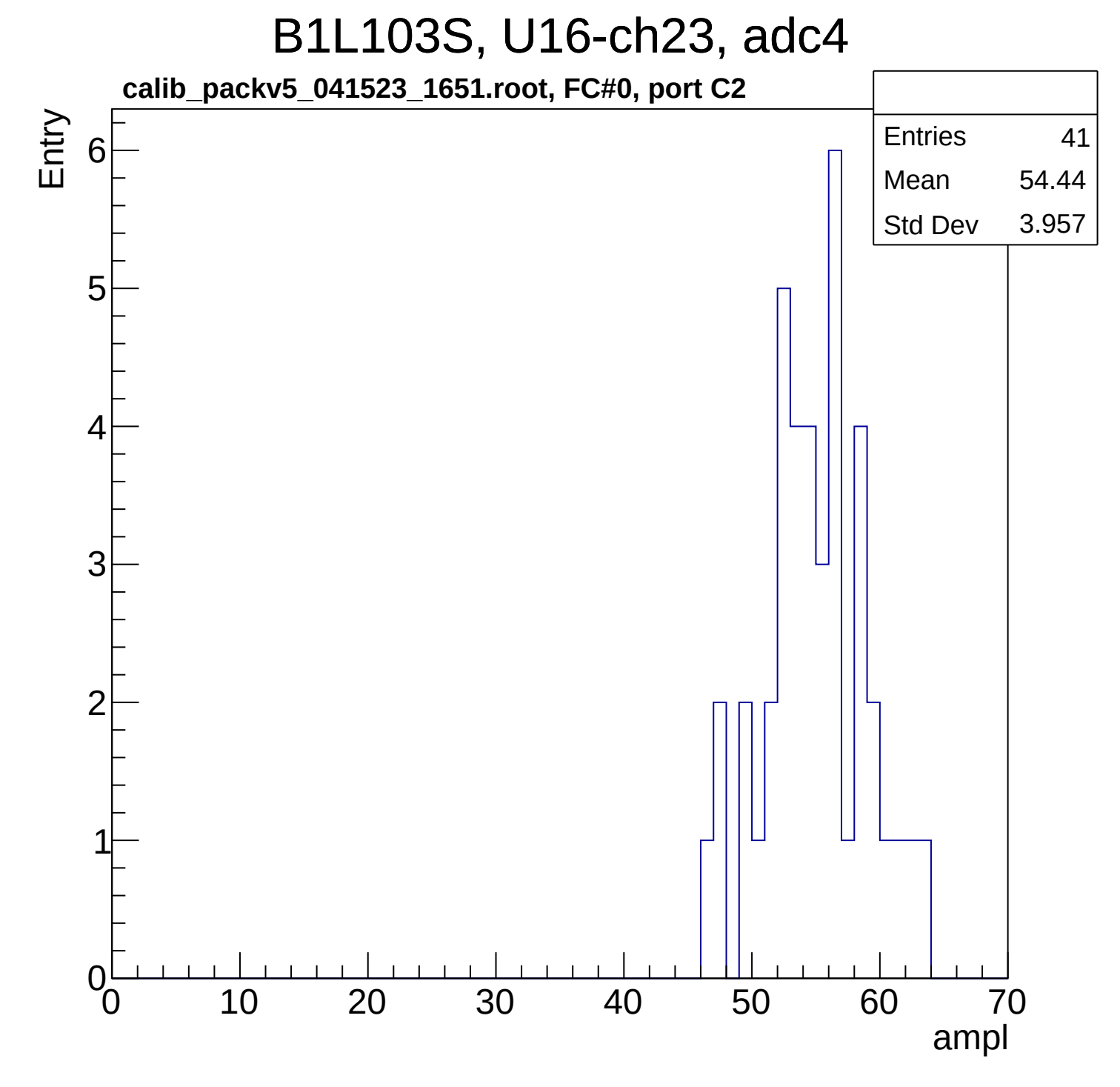
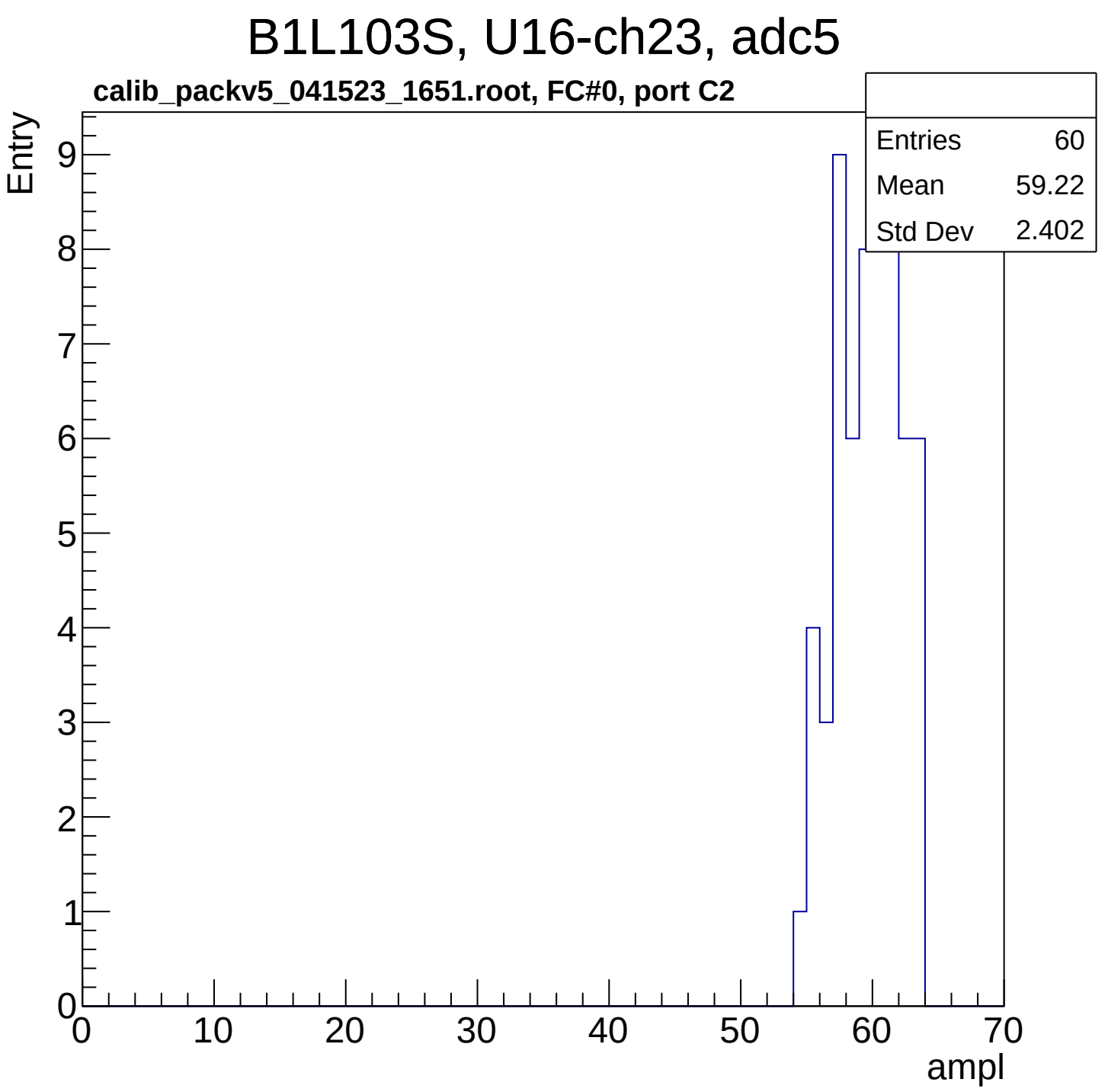
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch23, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 54.44
Std Dev 3.957
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U16-ch23, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 59.22
Std Dev 2.402
Entry
ampl
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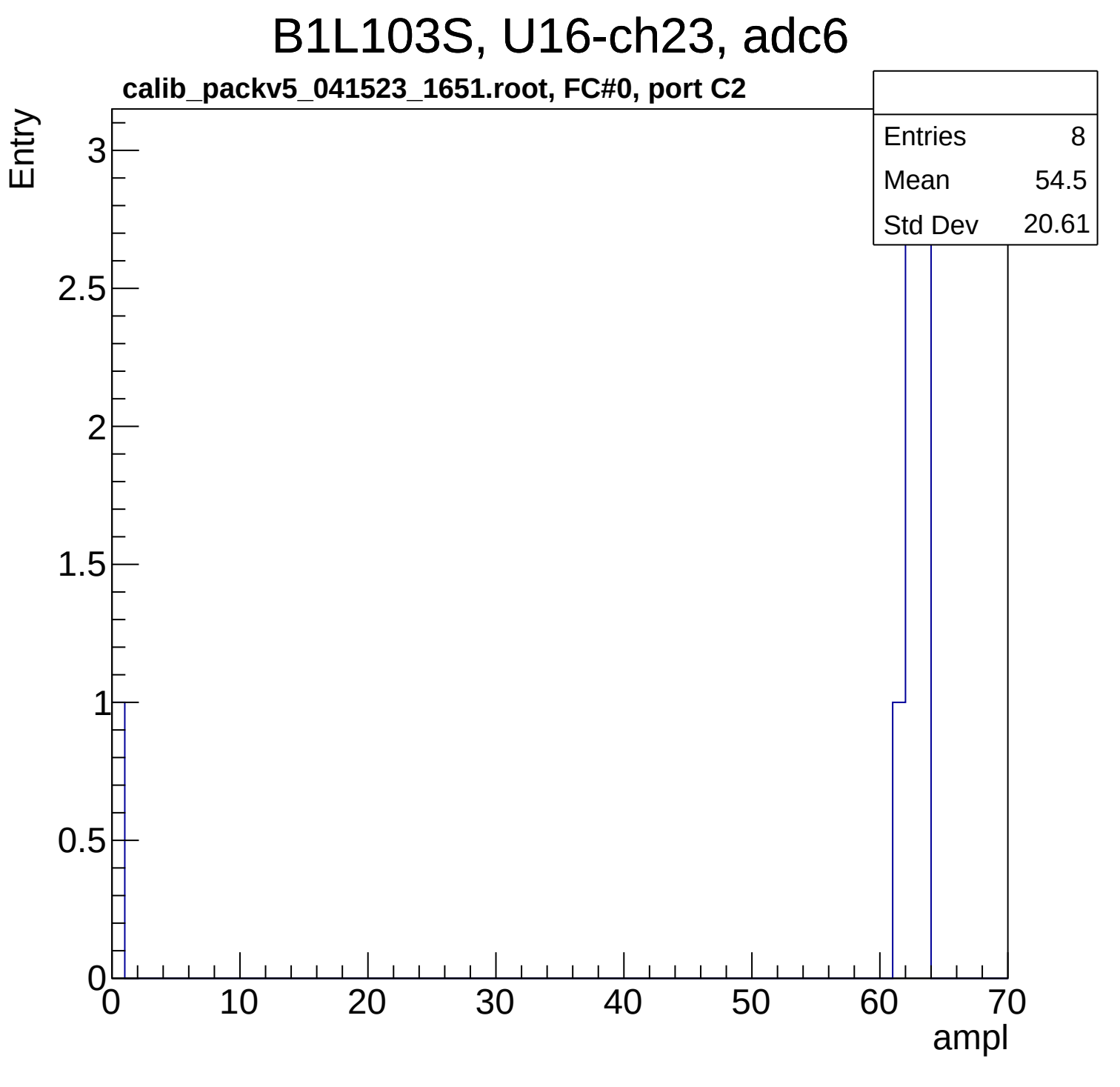
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch23, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 54.5
Std Dev 20.61
Entry
ampl
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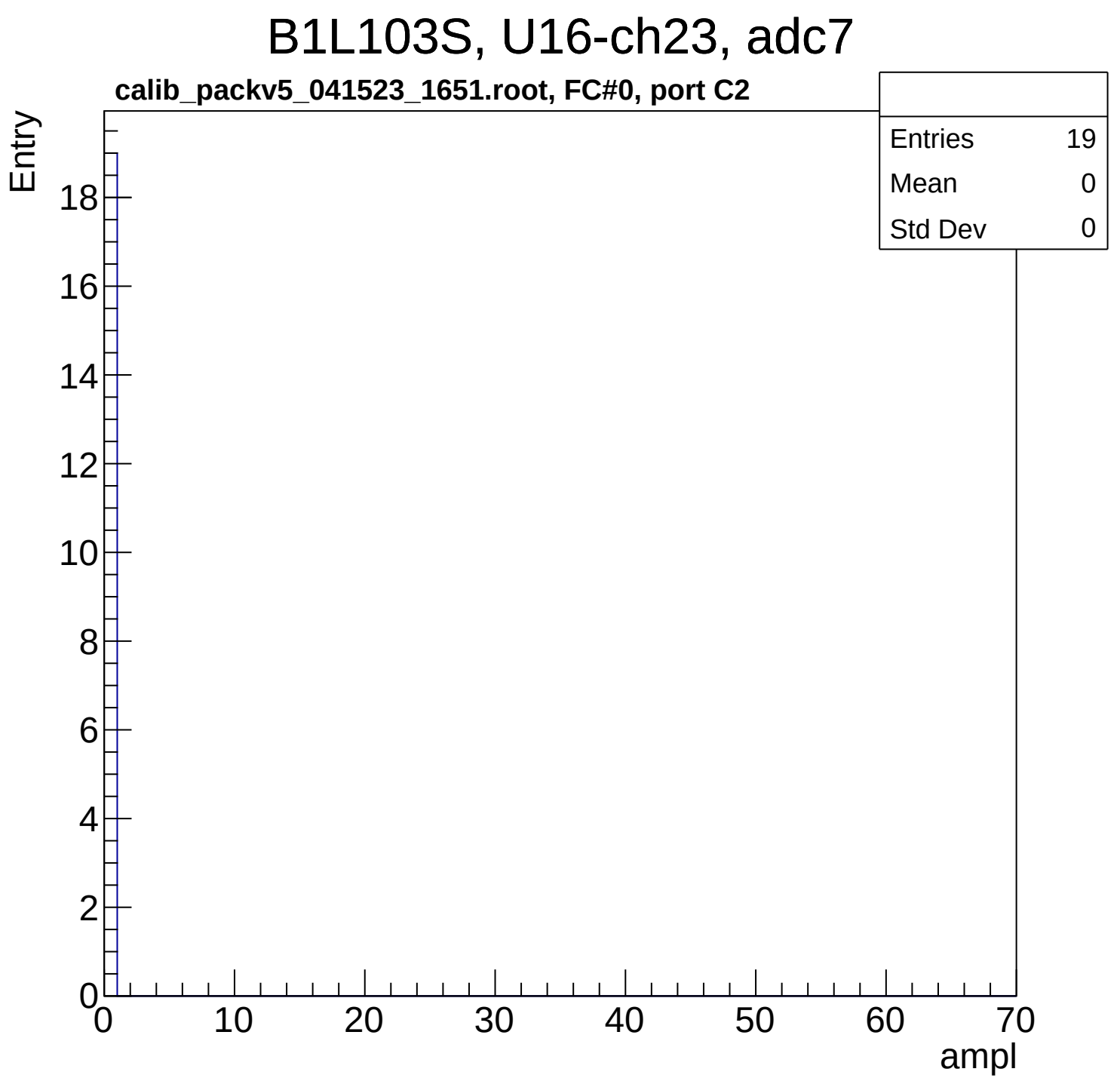
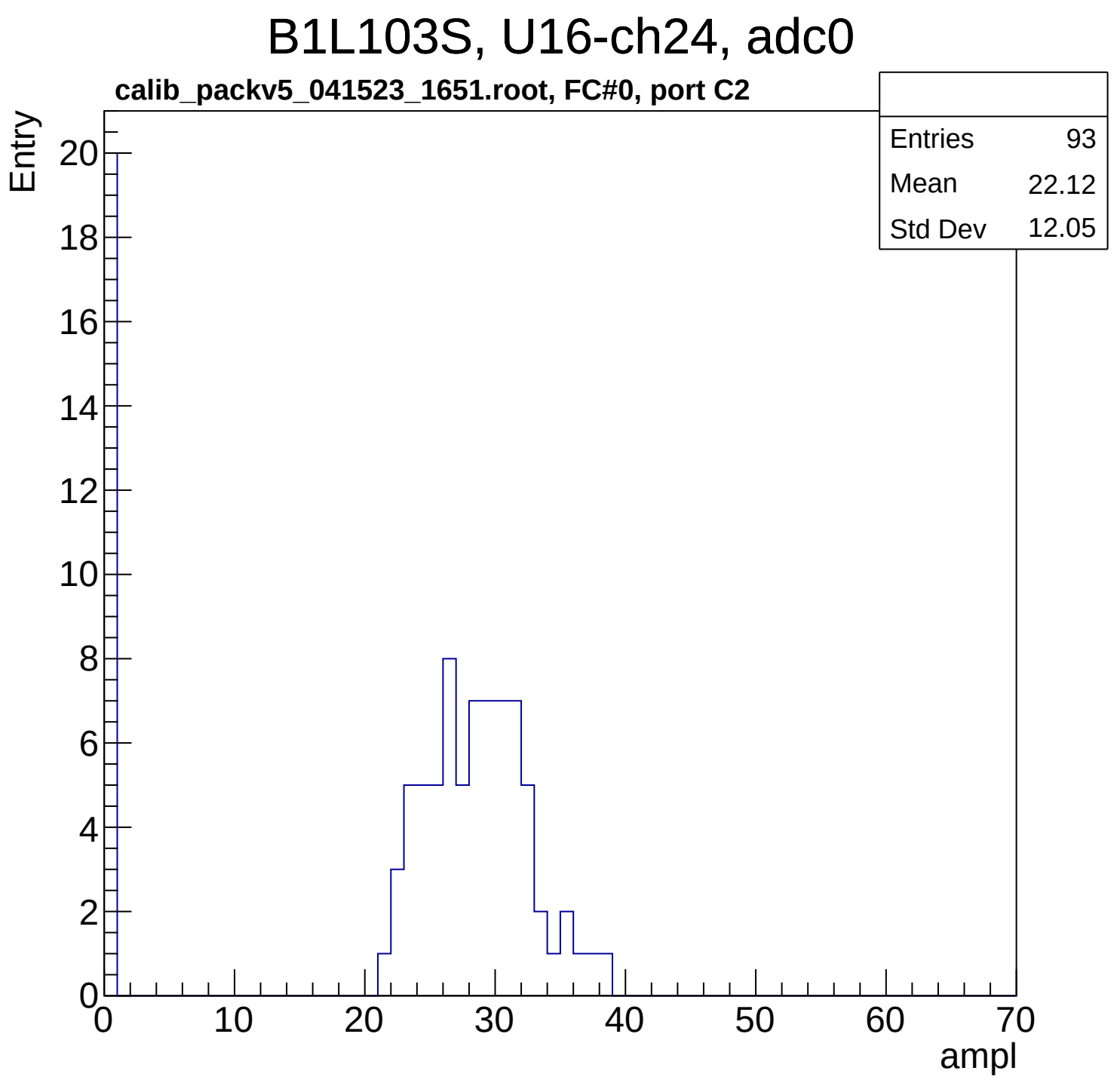
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U16-ch23, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch24, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 22.12
Std Dev 12.05
Entry
0
2
4
6
8
10
12
14
16
18
20
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10
20
30
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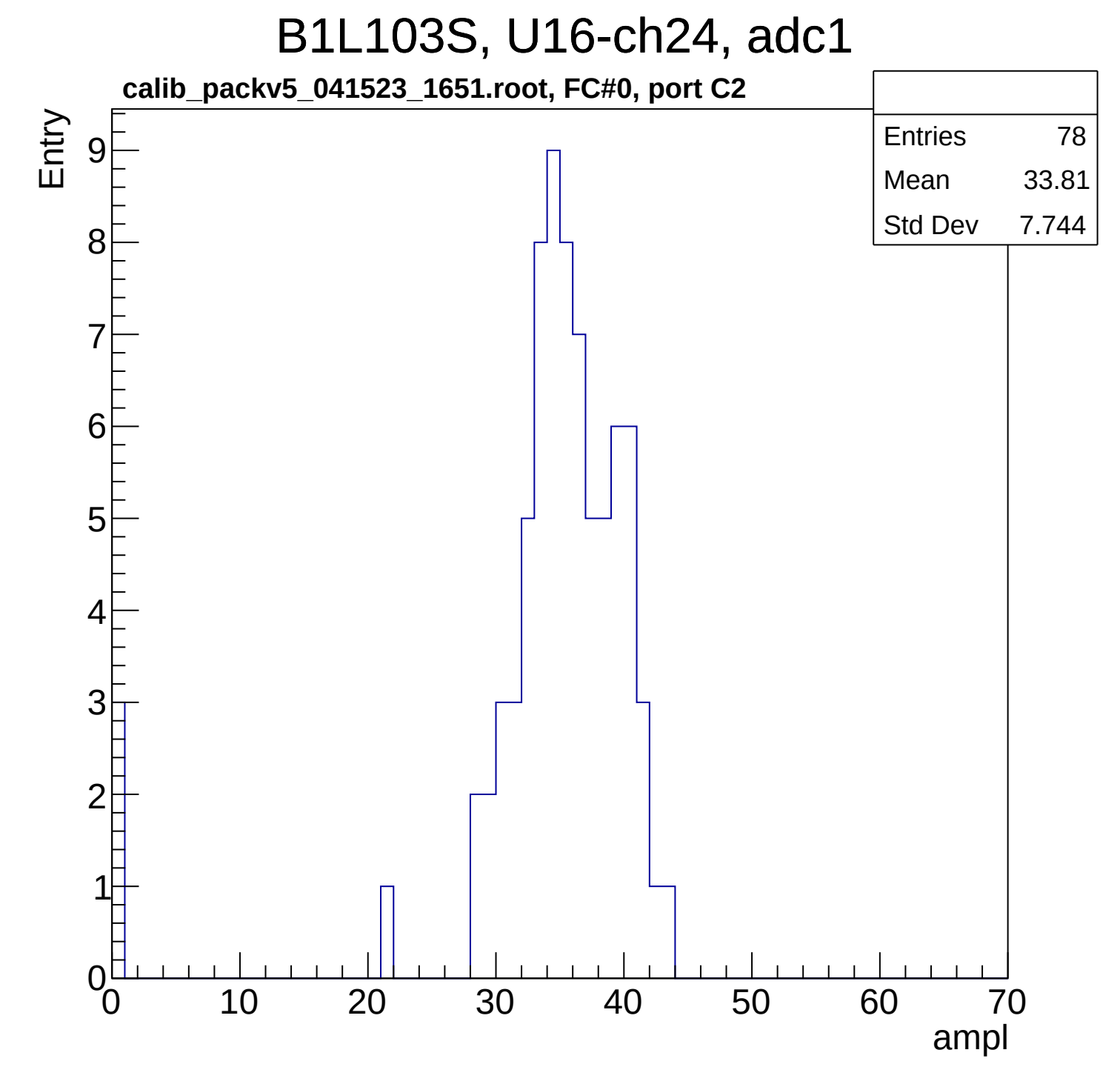
50
60
70
ampl


B1L103S, U16-ch24, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 33.81
Std Dev 7.744
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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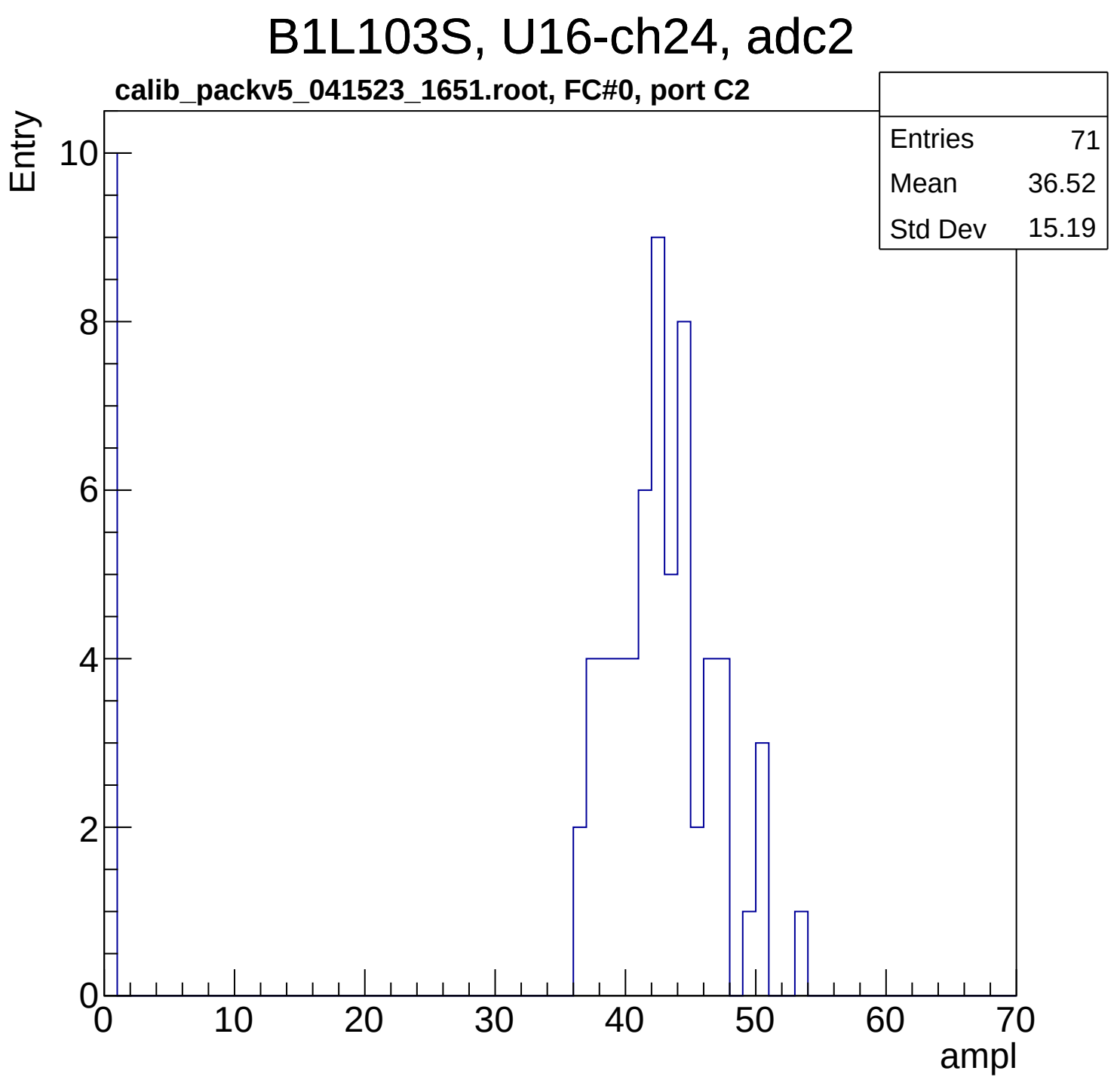
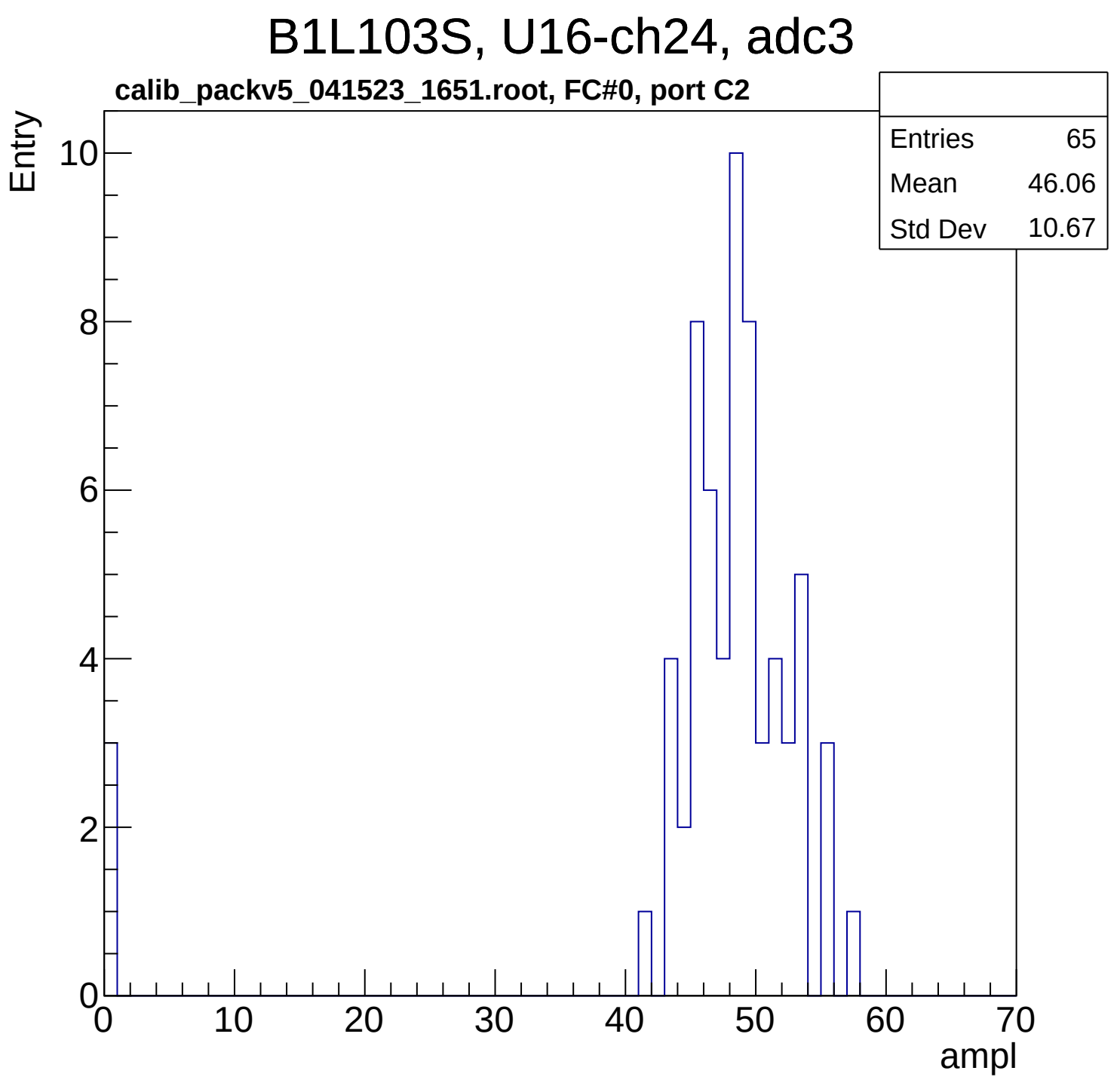
40
50
60
70


B1L103S, U16-ch24, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 36.52
Std Dev 15.19
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch24, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 46.06
Std Dev 10.67
Entry
ampl
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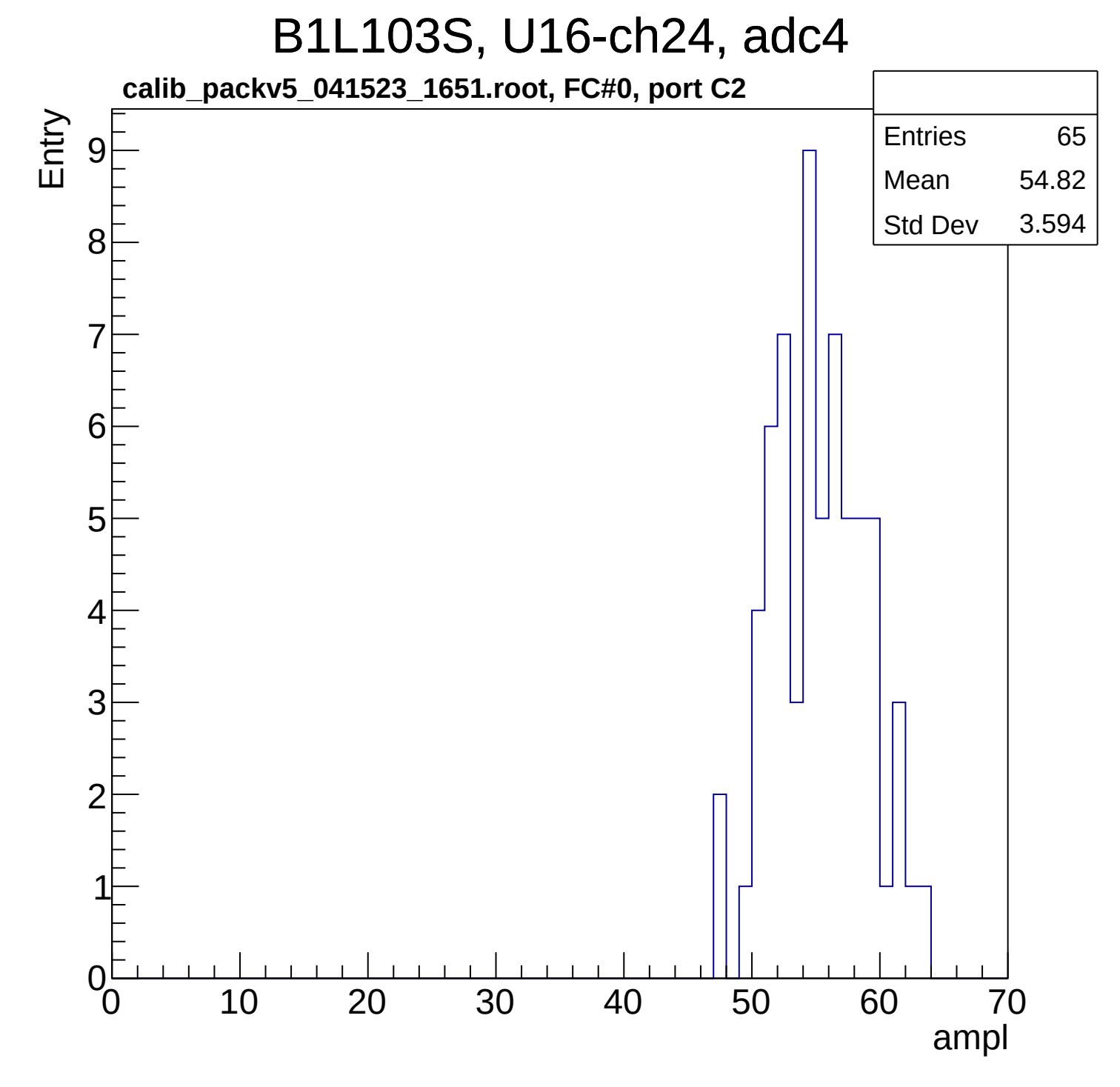
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch24, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 54.82
Std Dev 3.594
Entry
ampl
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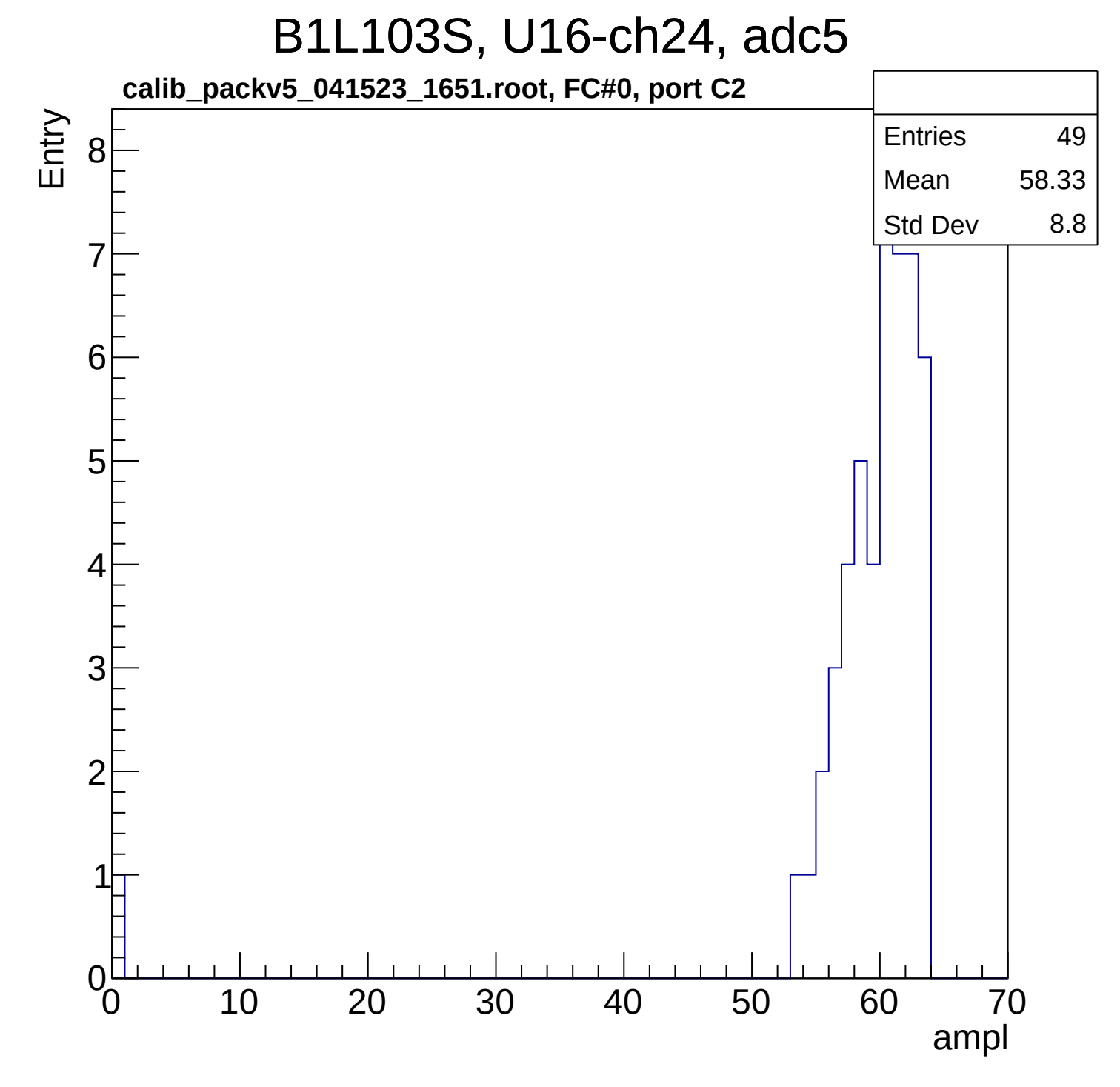
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch24, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.33
Std Dev 8.8
Entry
ampl
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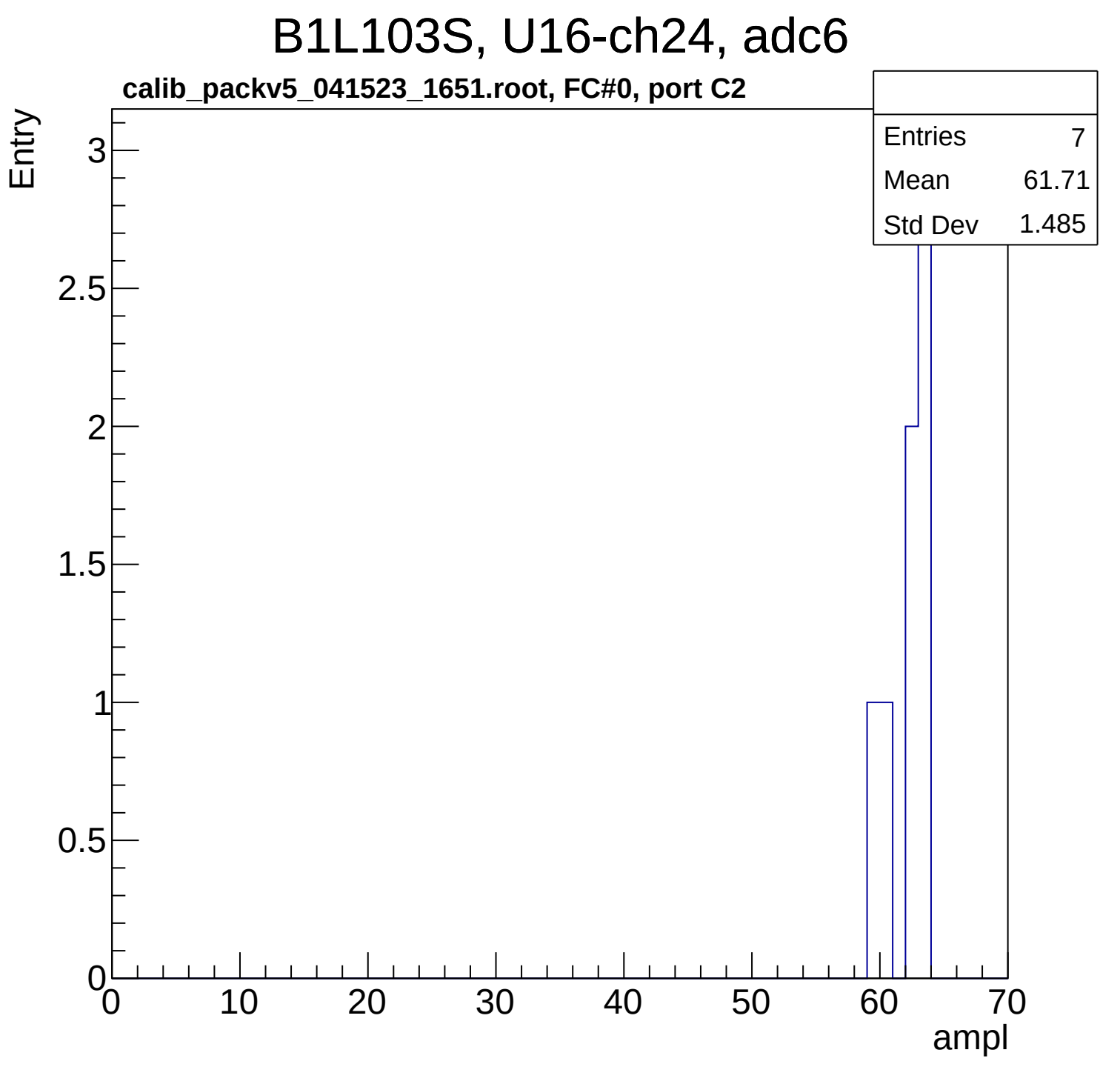
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch24, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.71
Std Dev 1.485
Entry
ampl
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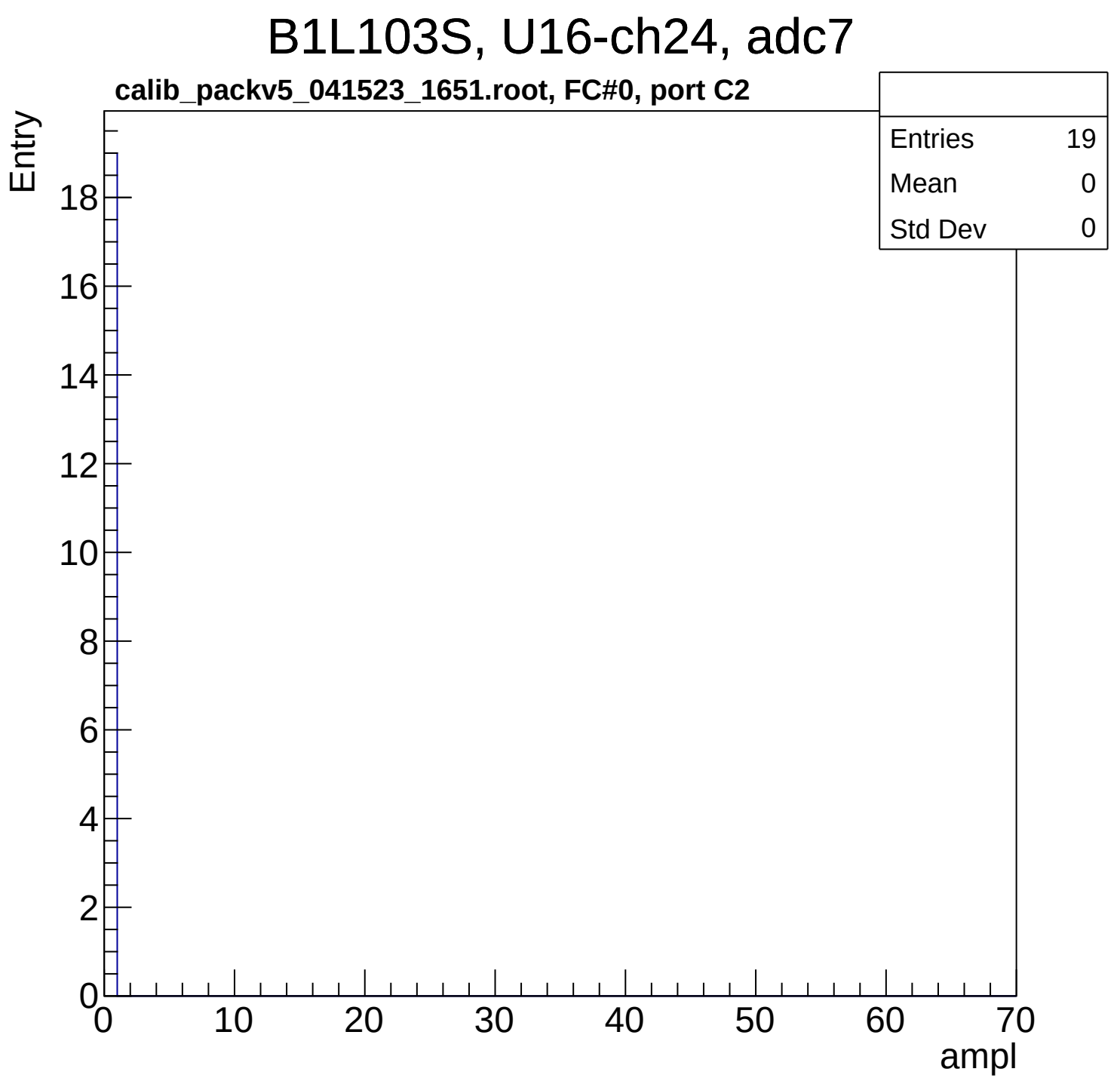
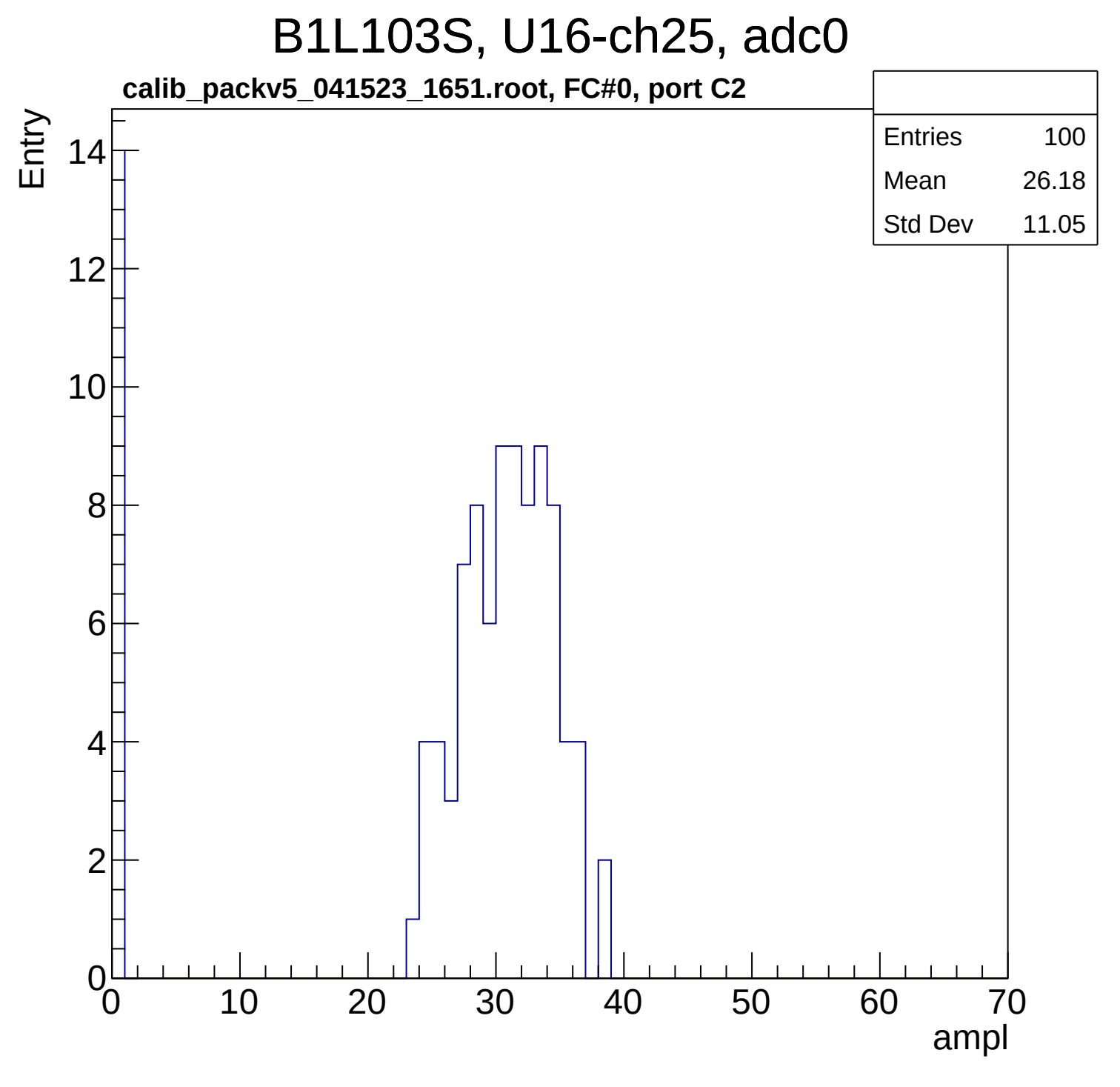
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U16-ch24, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch25, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 26.18
Std Dev 11.05
Entry
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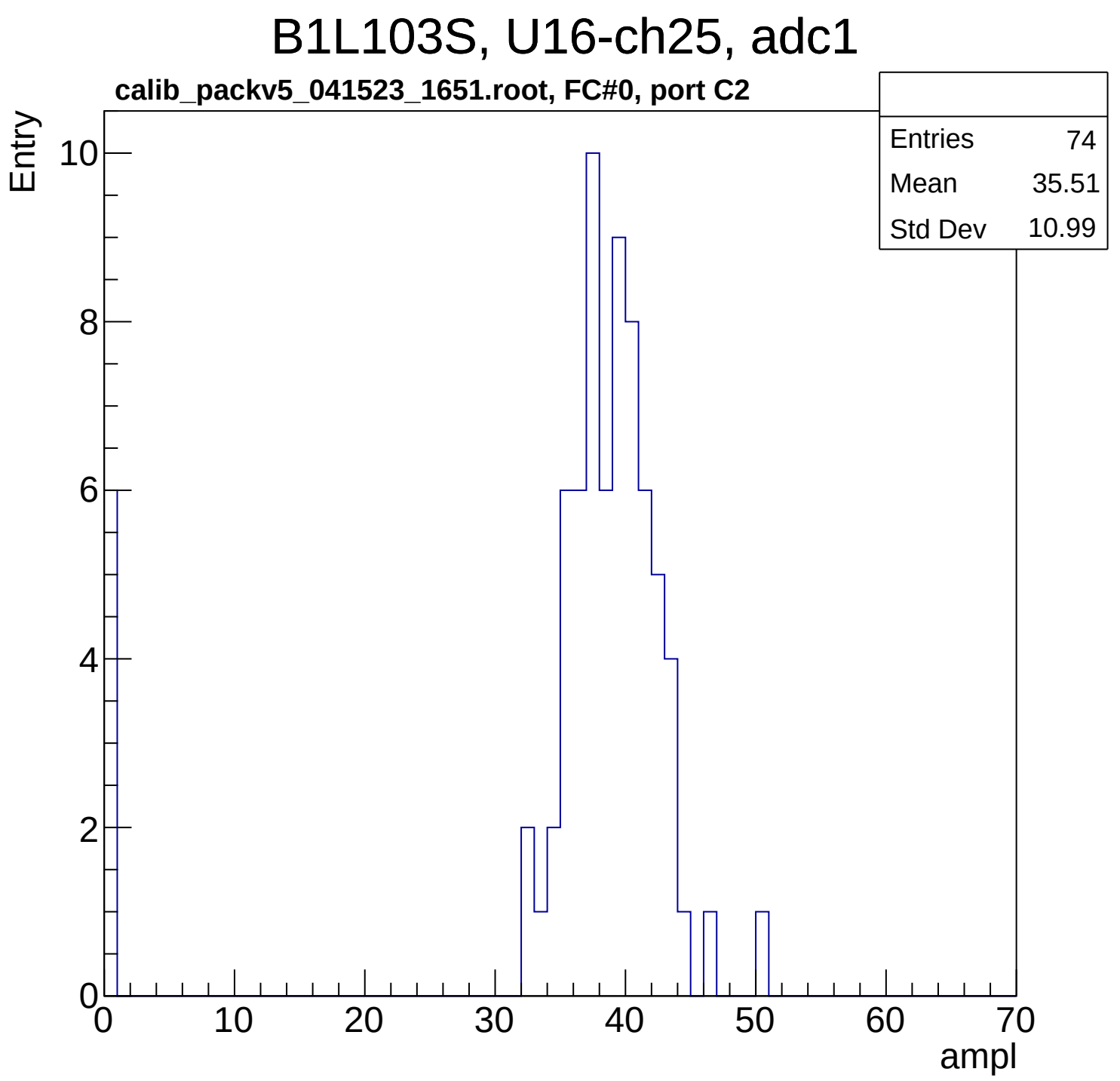
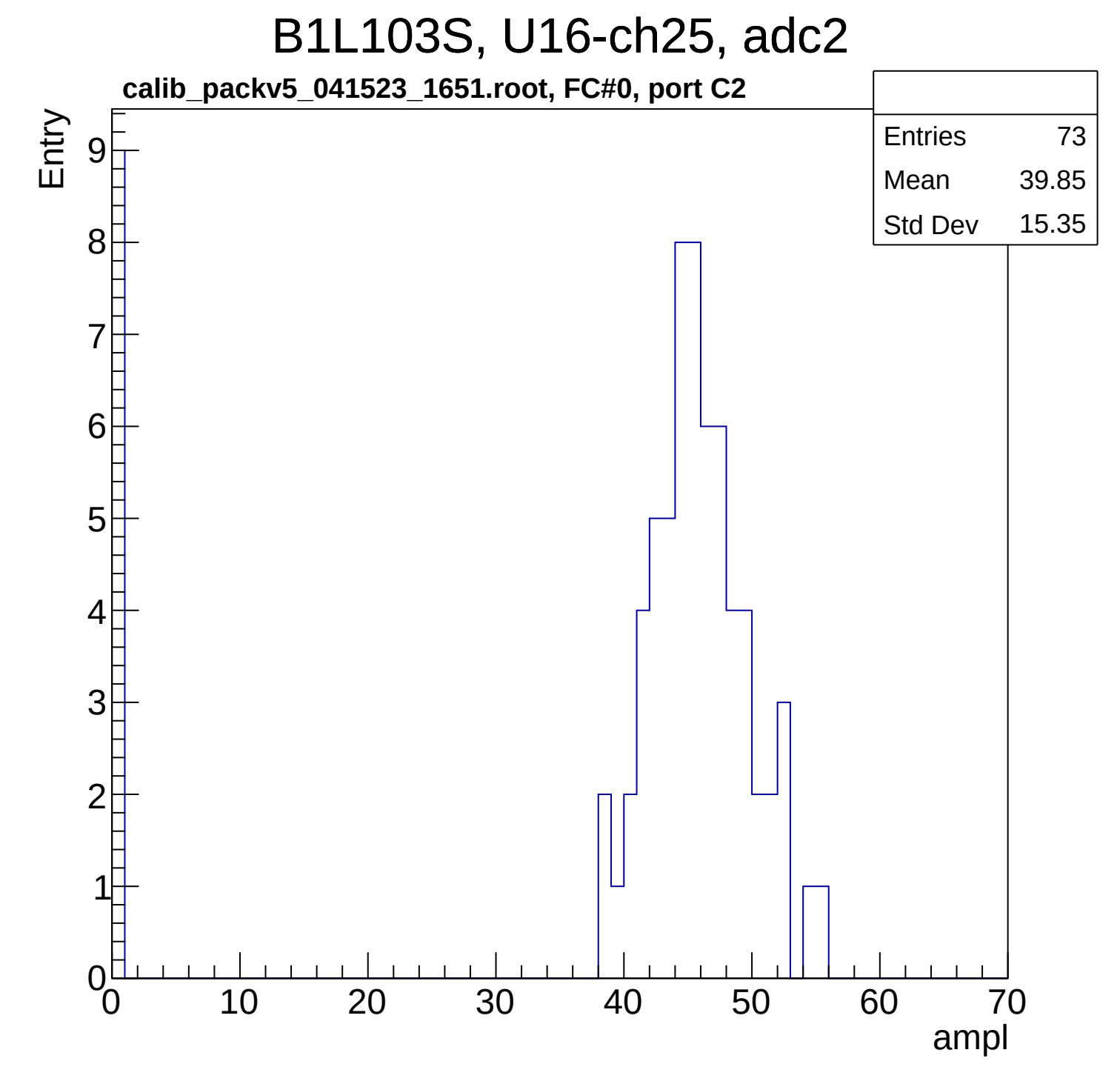
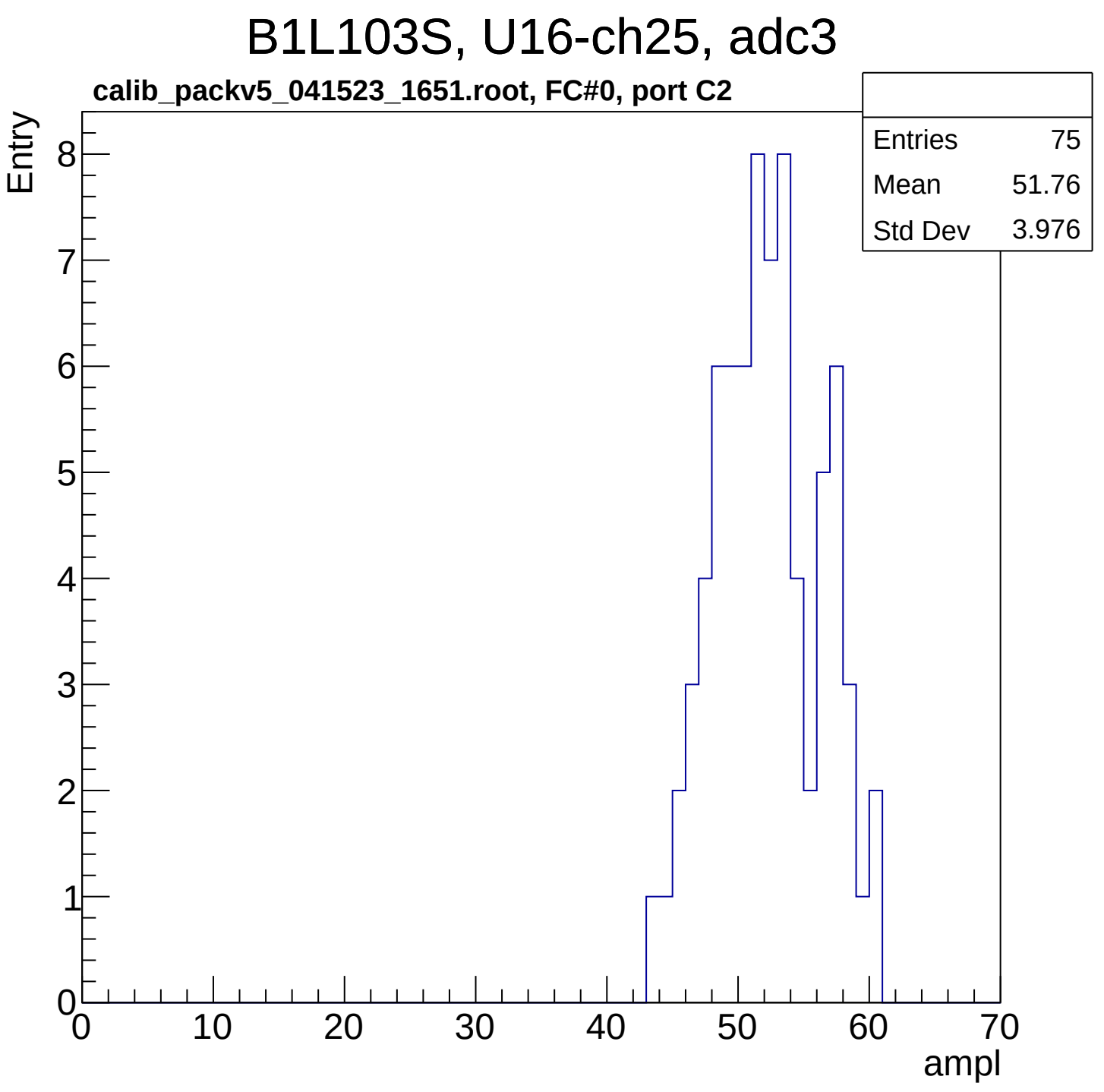
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch25, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 35.51
Std Dev 10.99
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch25, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 39.85
Std Dev 15.35
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch25, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 51.76
Std Dev 3.976
Entry
ampl
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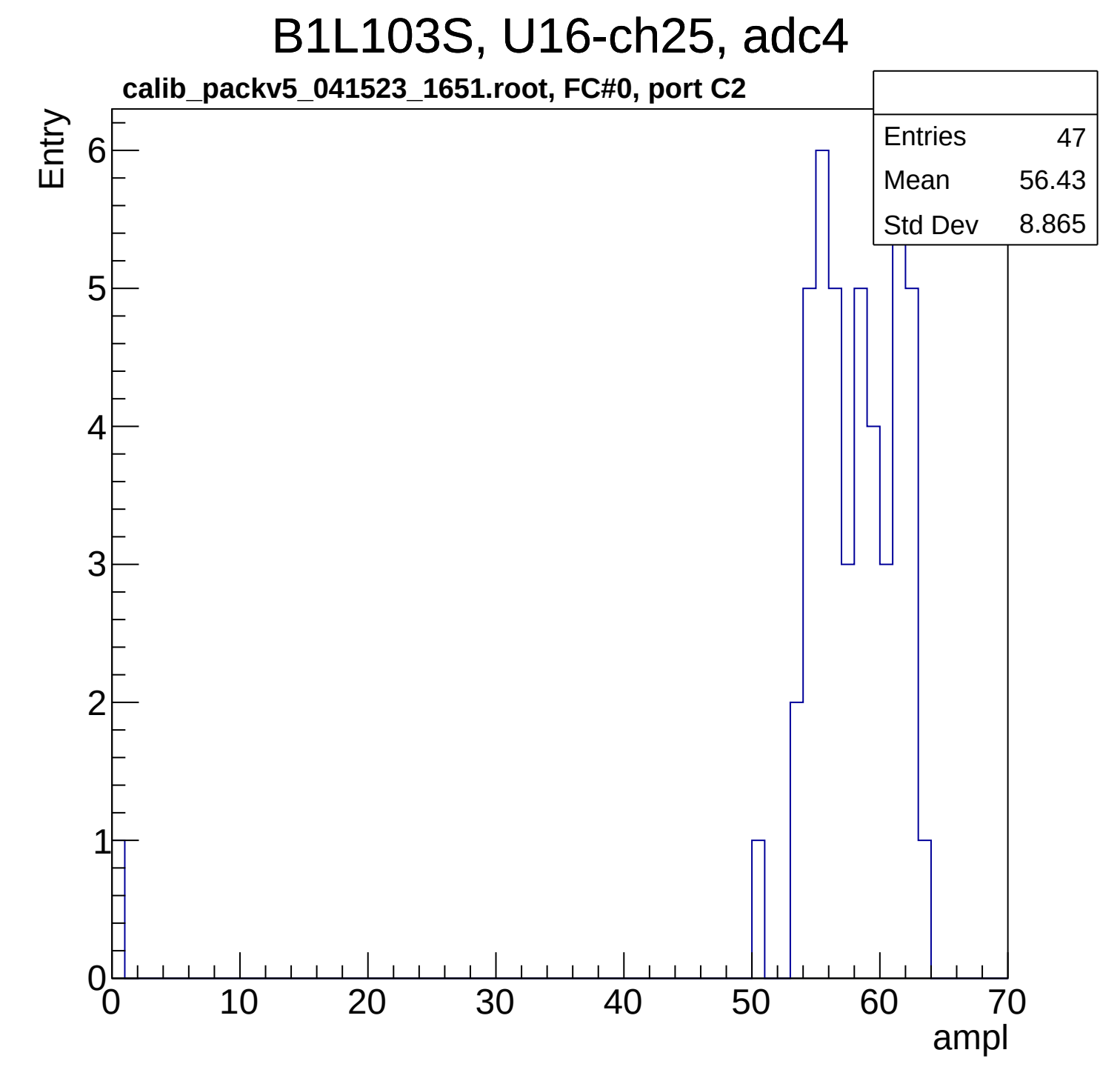
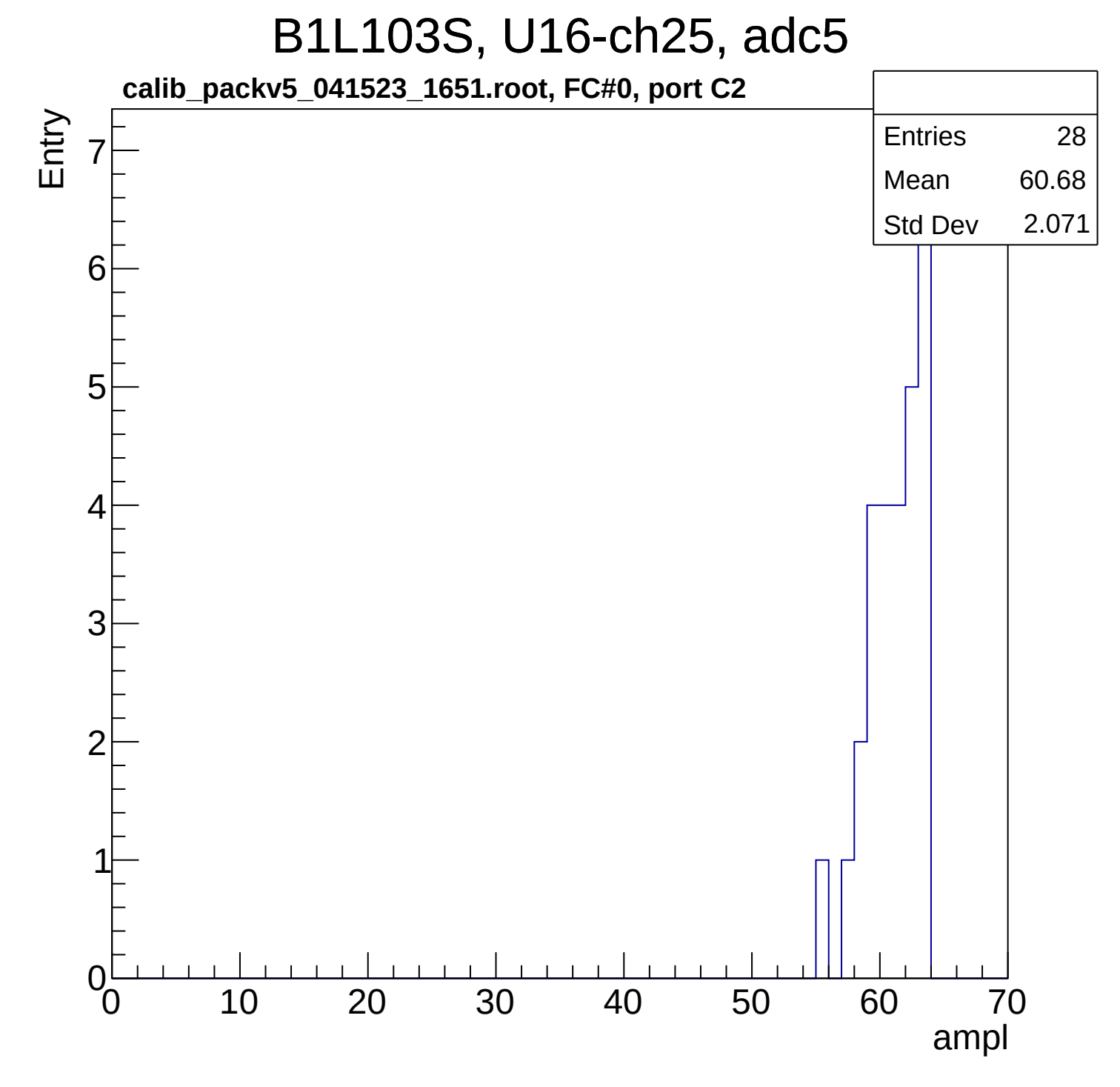
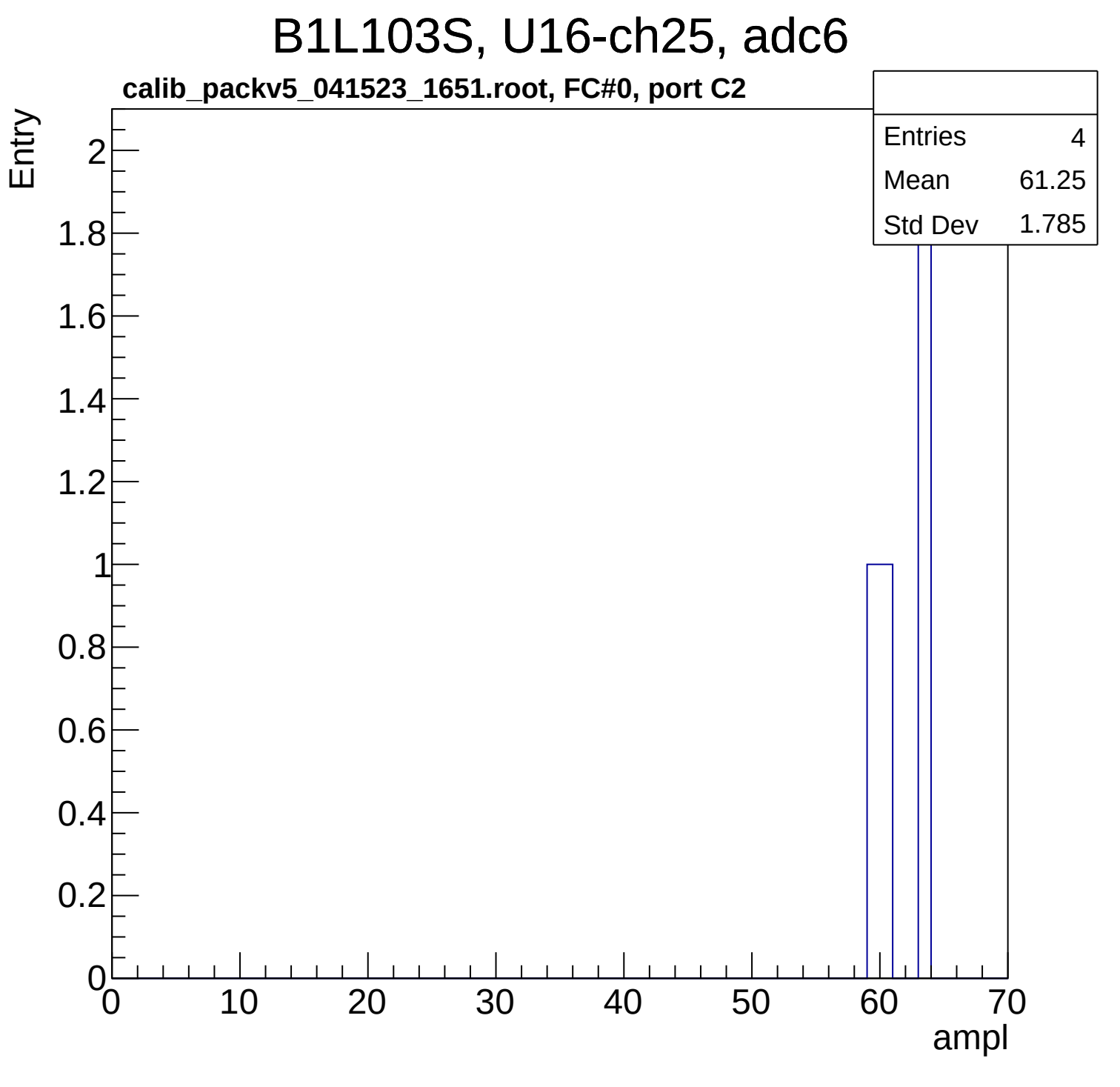
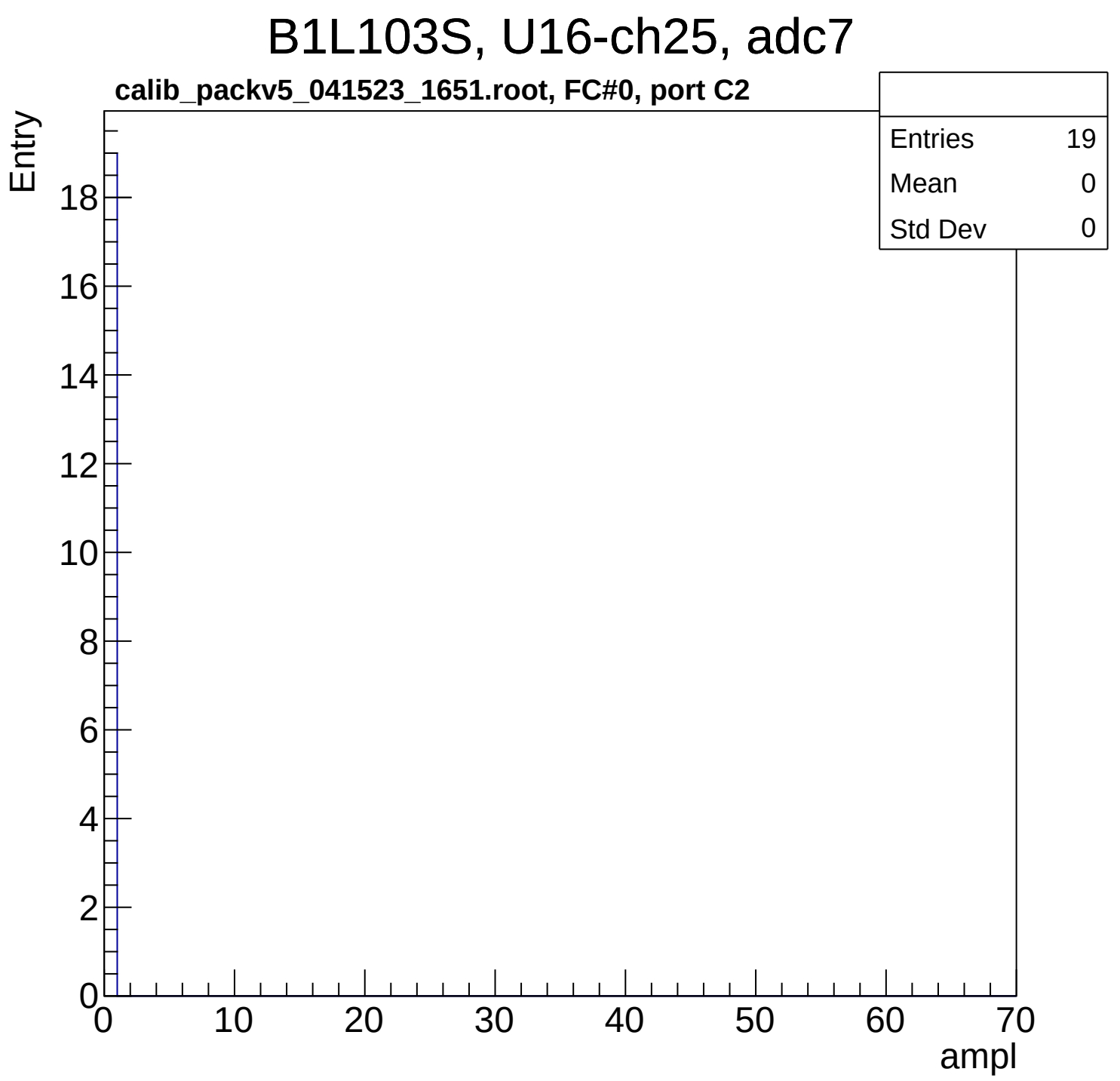
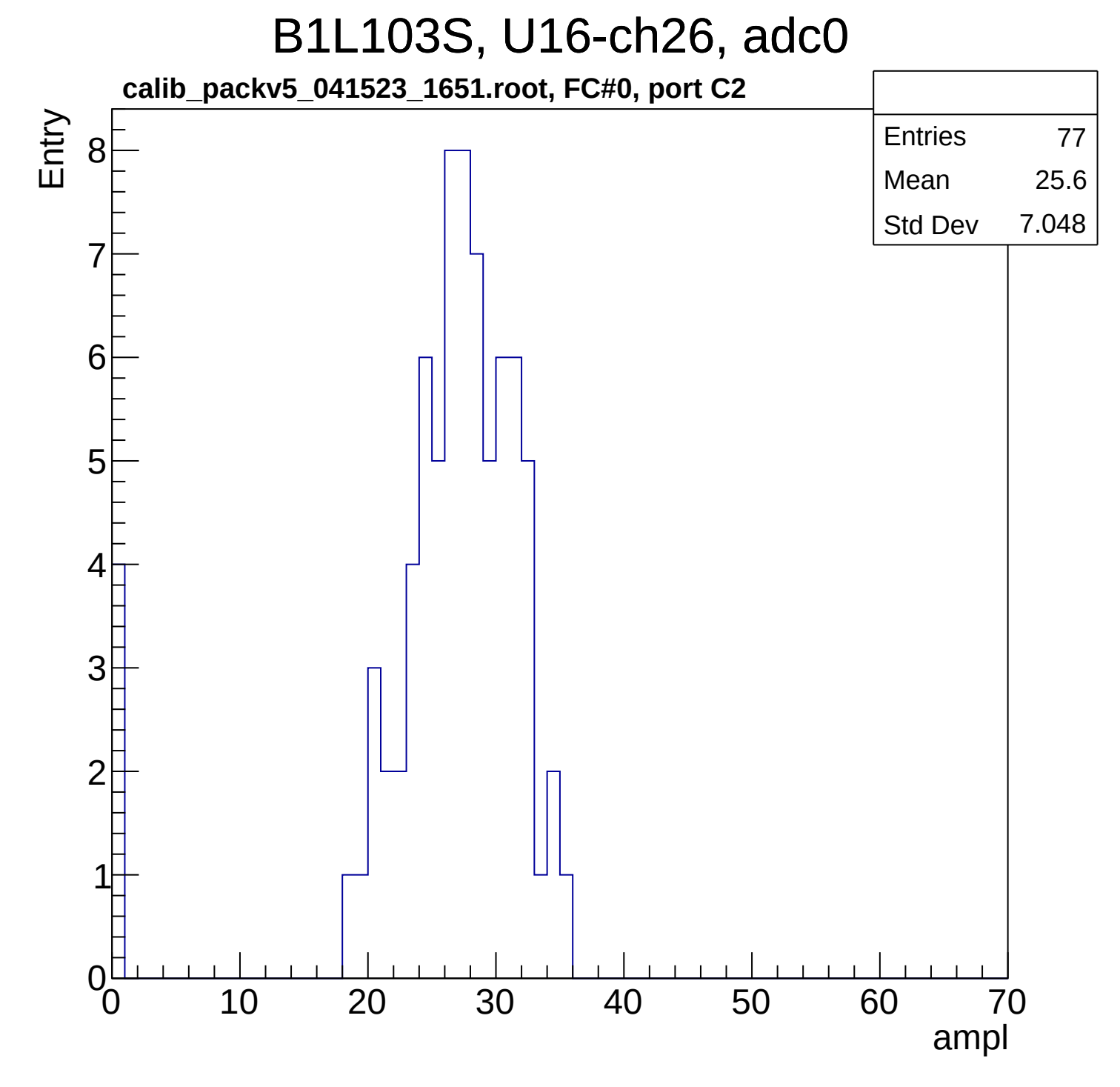
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch25, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 56.43
Std Dev 8.865
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U16-ch25, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 60.68
Std Dev 2.071
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch25, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61.25
Std Dev 1.785
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U16-ch25, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch26, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 25.6
Std Dev 7.048
Entry
ampl
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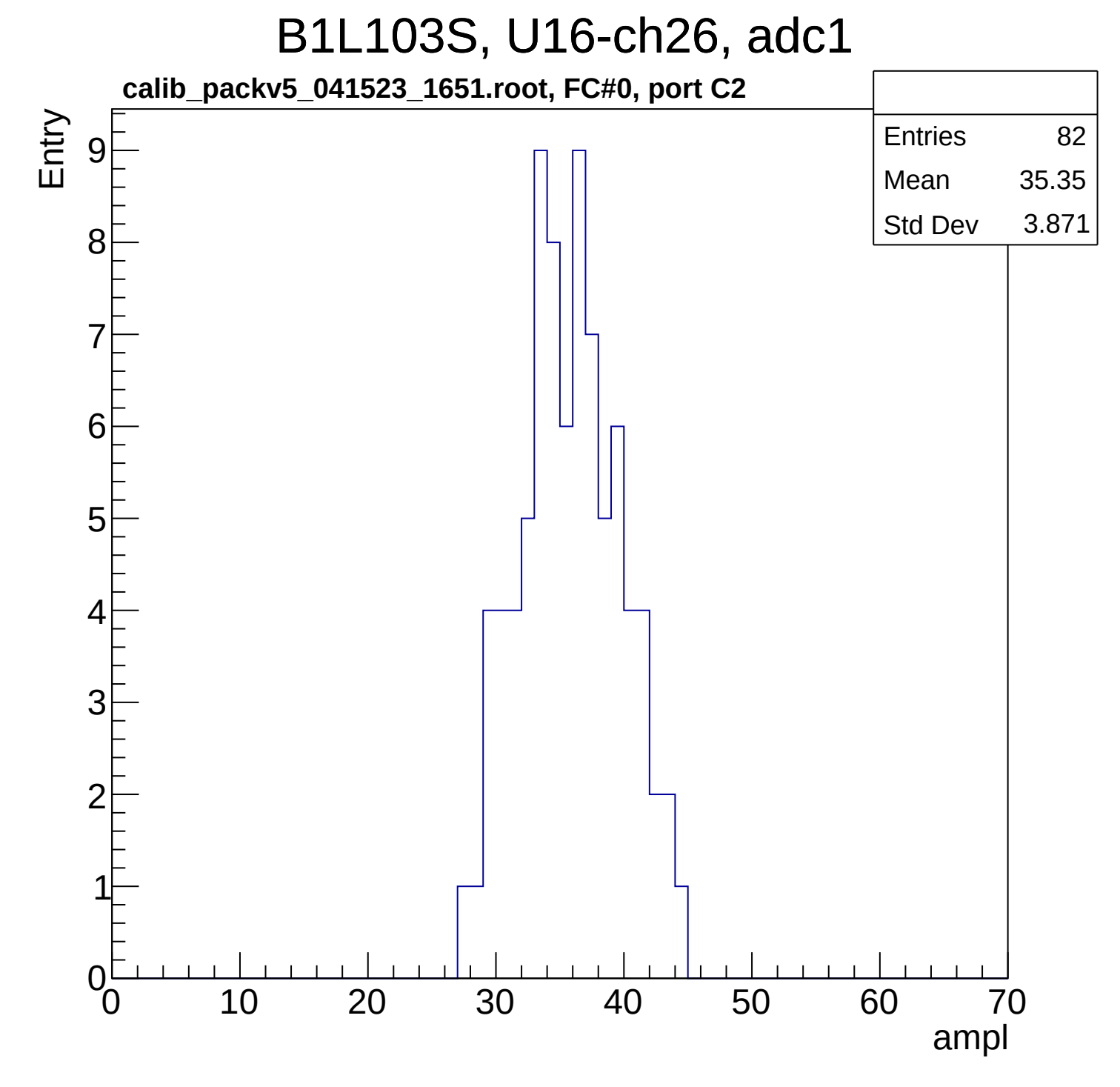
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch26, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 35.35
Std Dev 3.871
Entry
ampl
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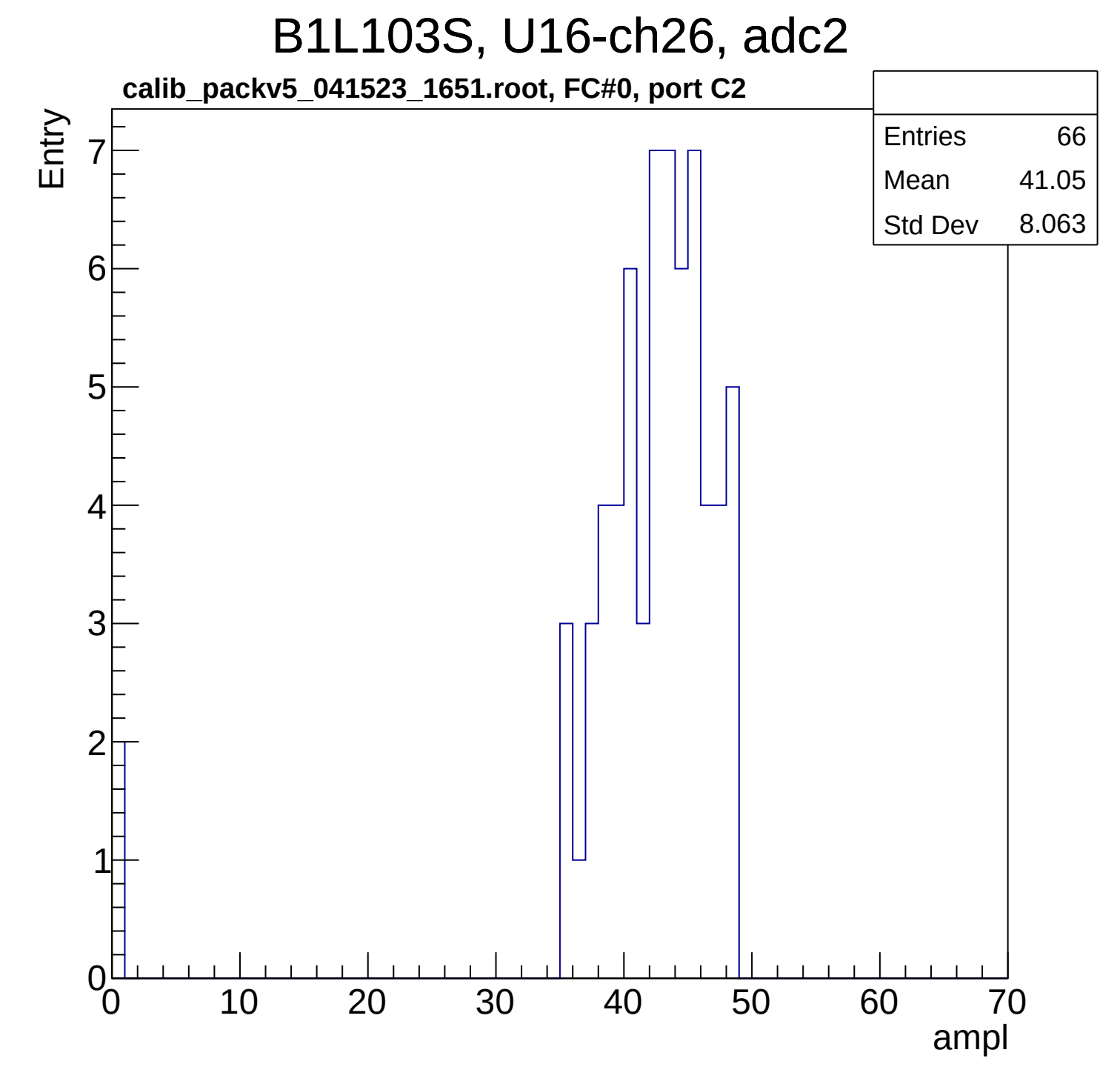
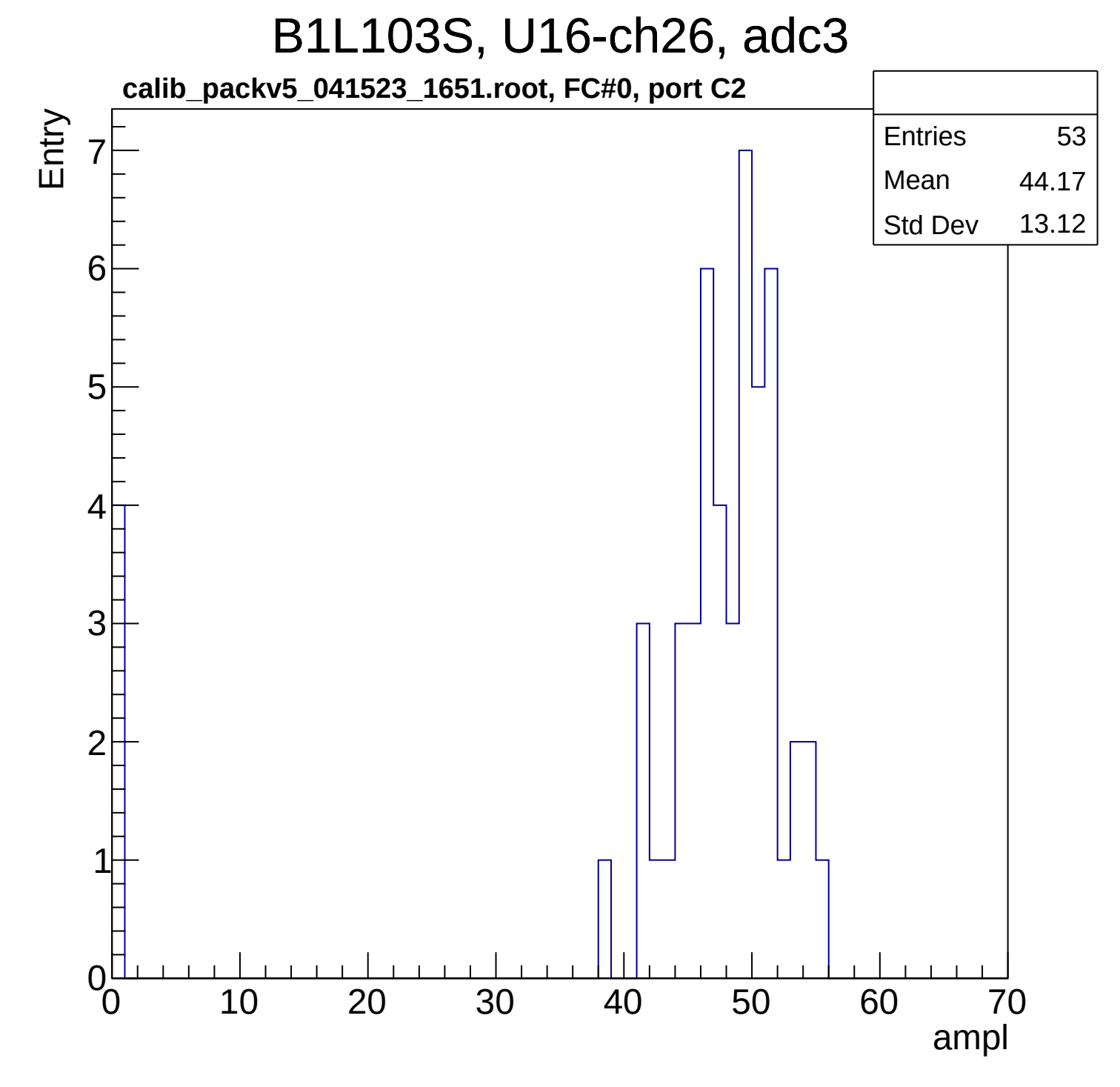
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch26, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 41.05
Std Dev 8.063
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch26, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 44.17
Std Dev 13.12
Entry
ampl
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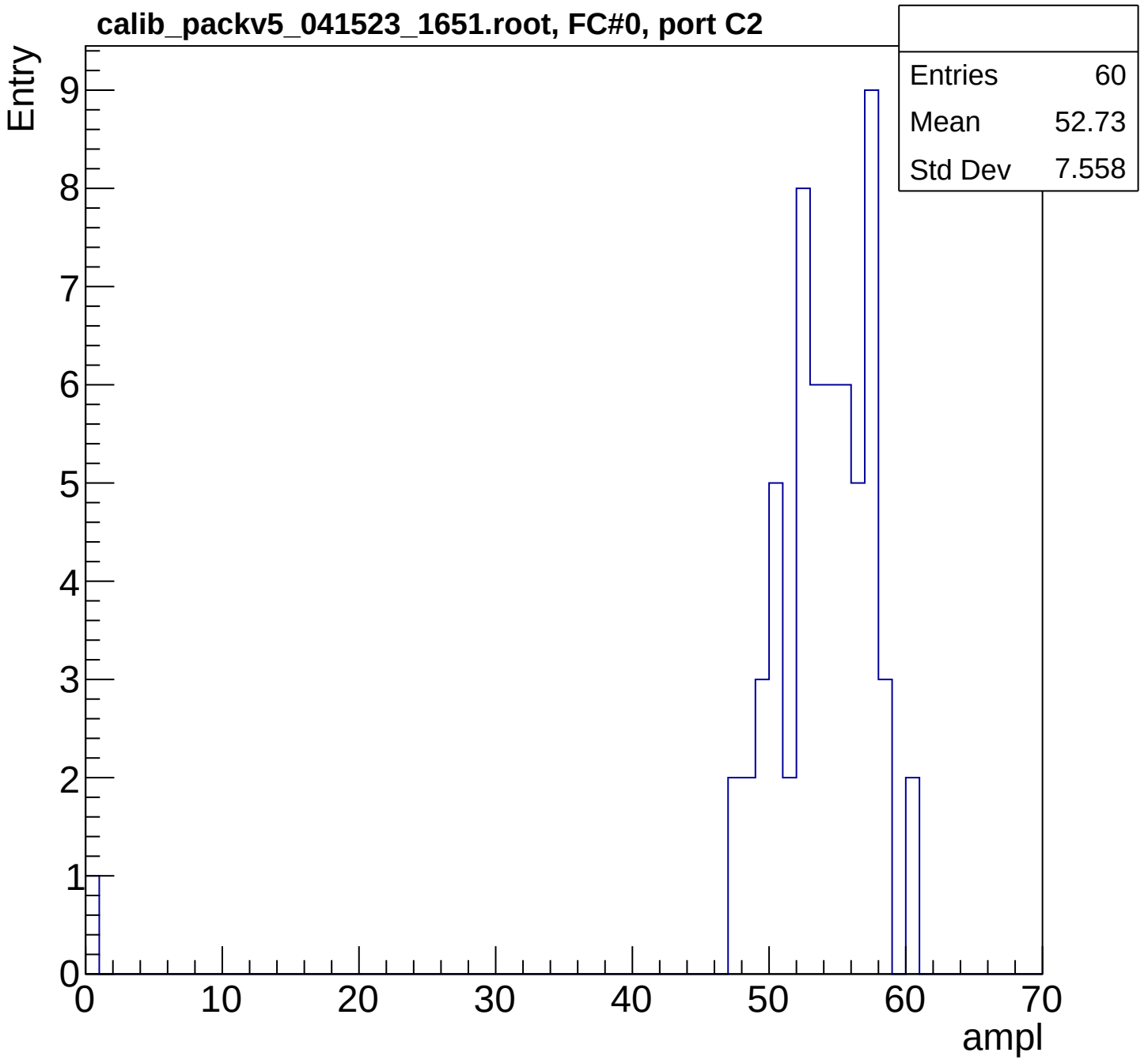
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch26, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 52.73
Std Dev 7.558
Entry
ampl
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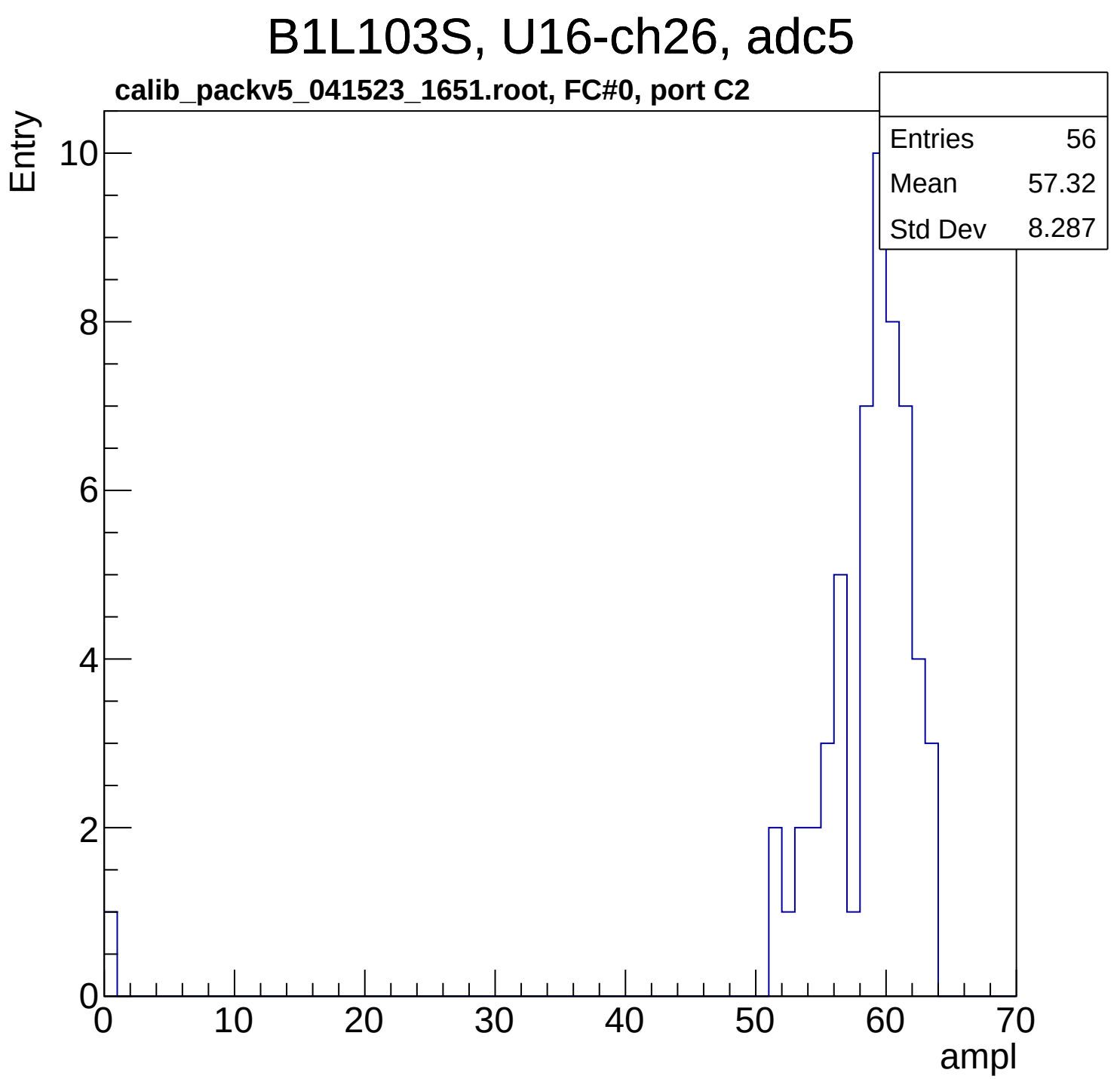
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch26, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 57.32
Std Dev 8.287
Entry
ampl
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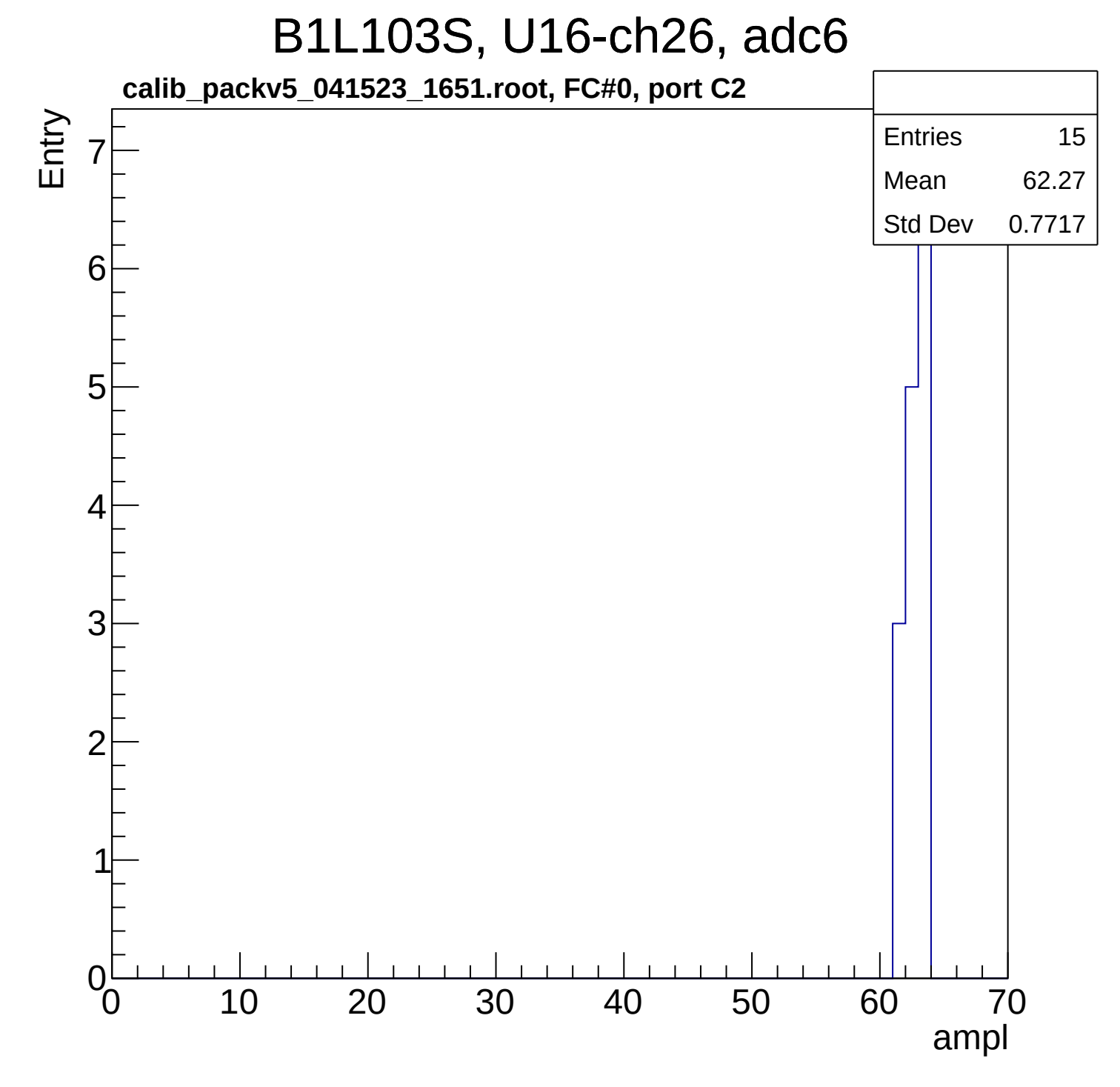
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch26, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 62.27
Std Dev 0.7717
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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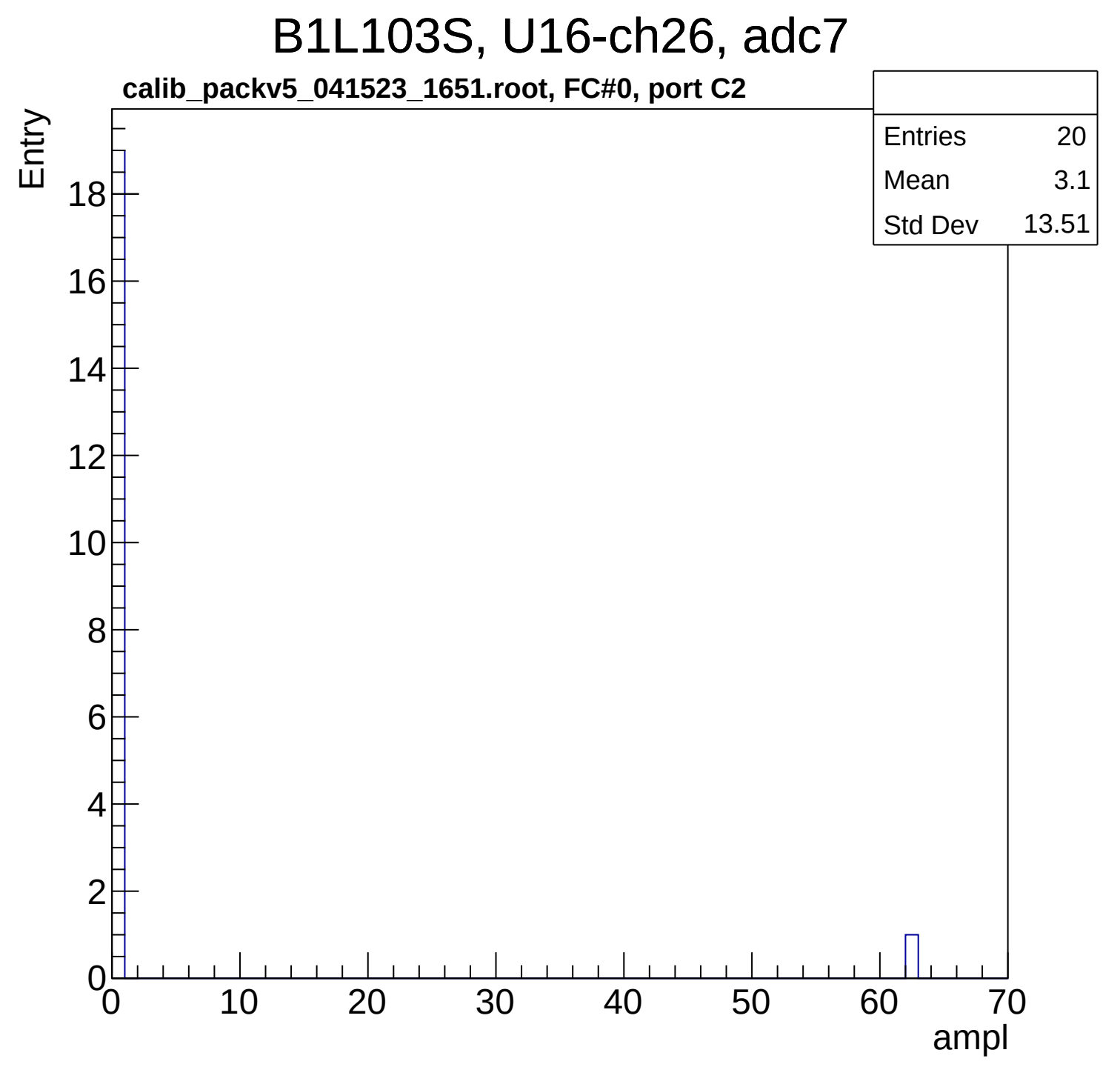
40
50
60
70


B1L103S, U16-ch26, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
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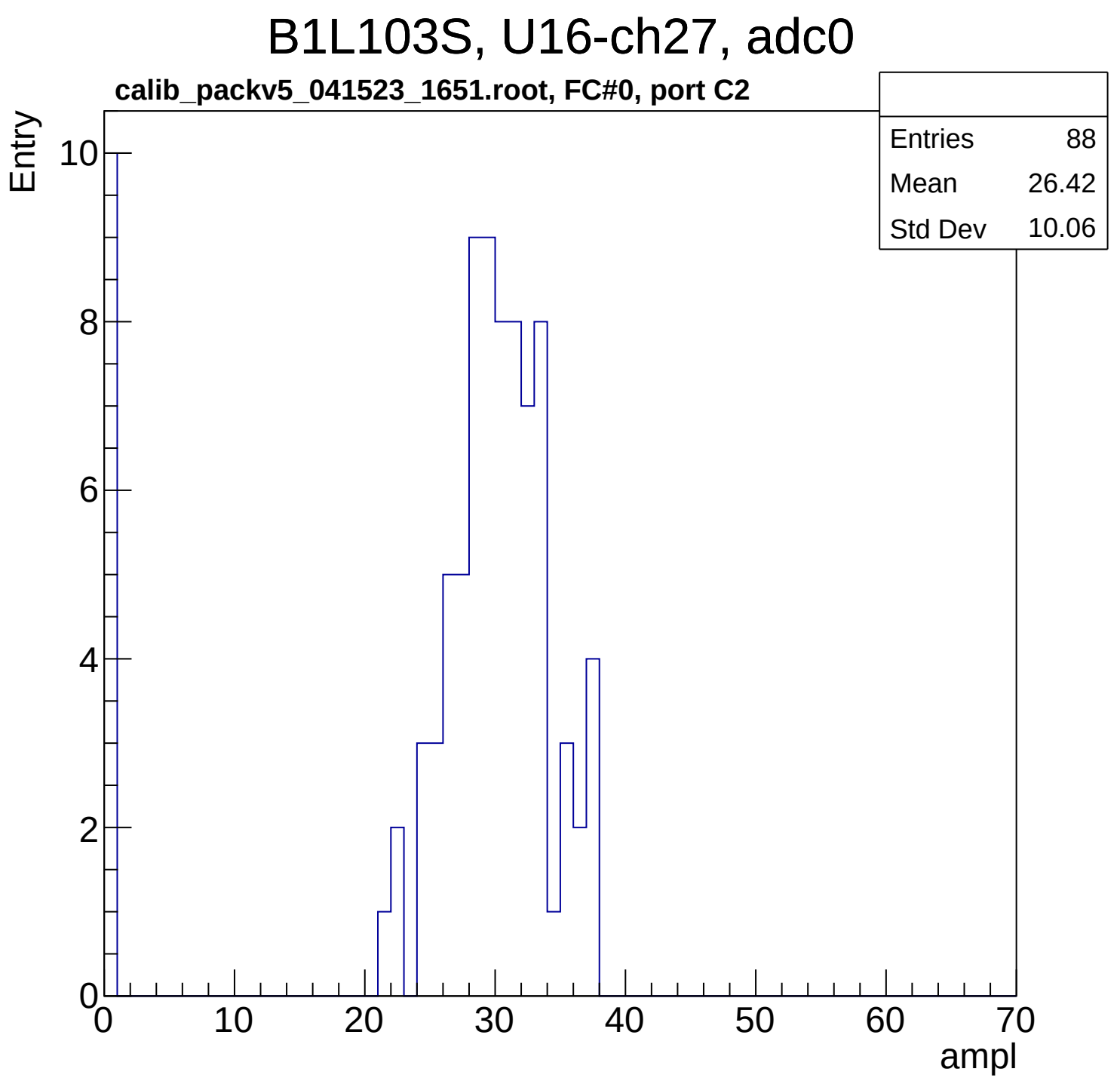
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch27, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 26.42
Std Dev 10.06
Entry
ampl
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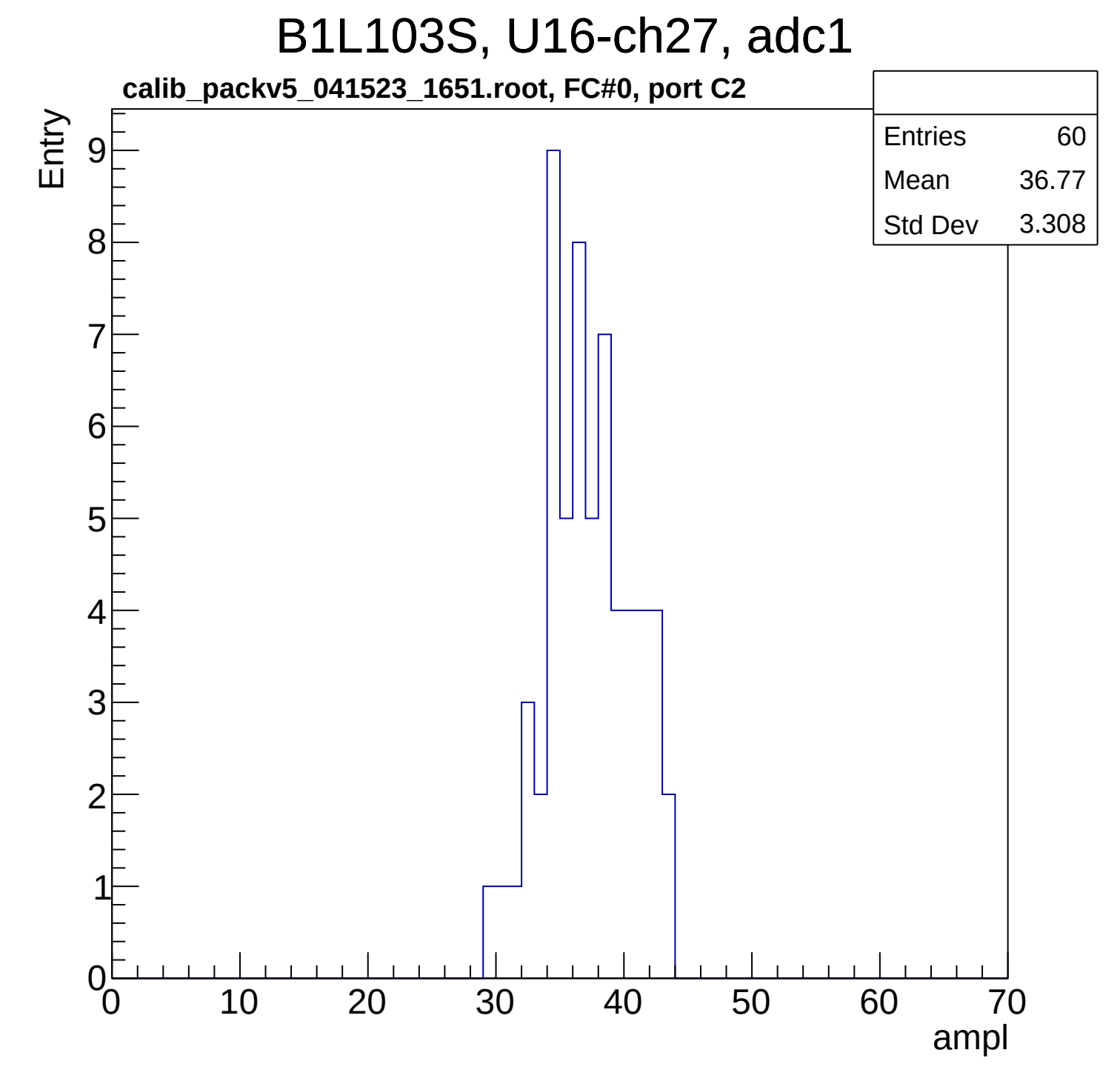
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch27, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 36.77
Std Dev 3.308
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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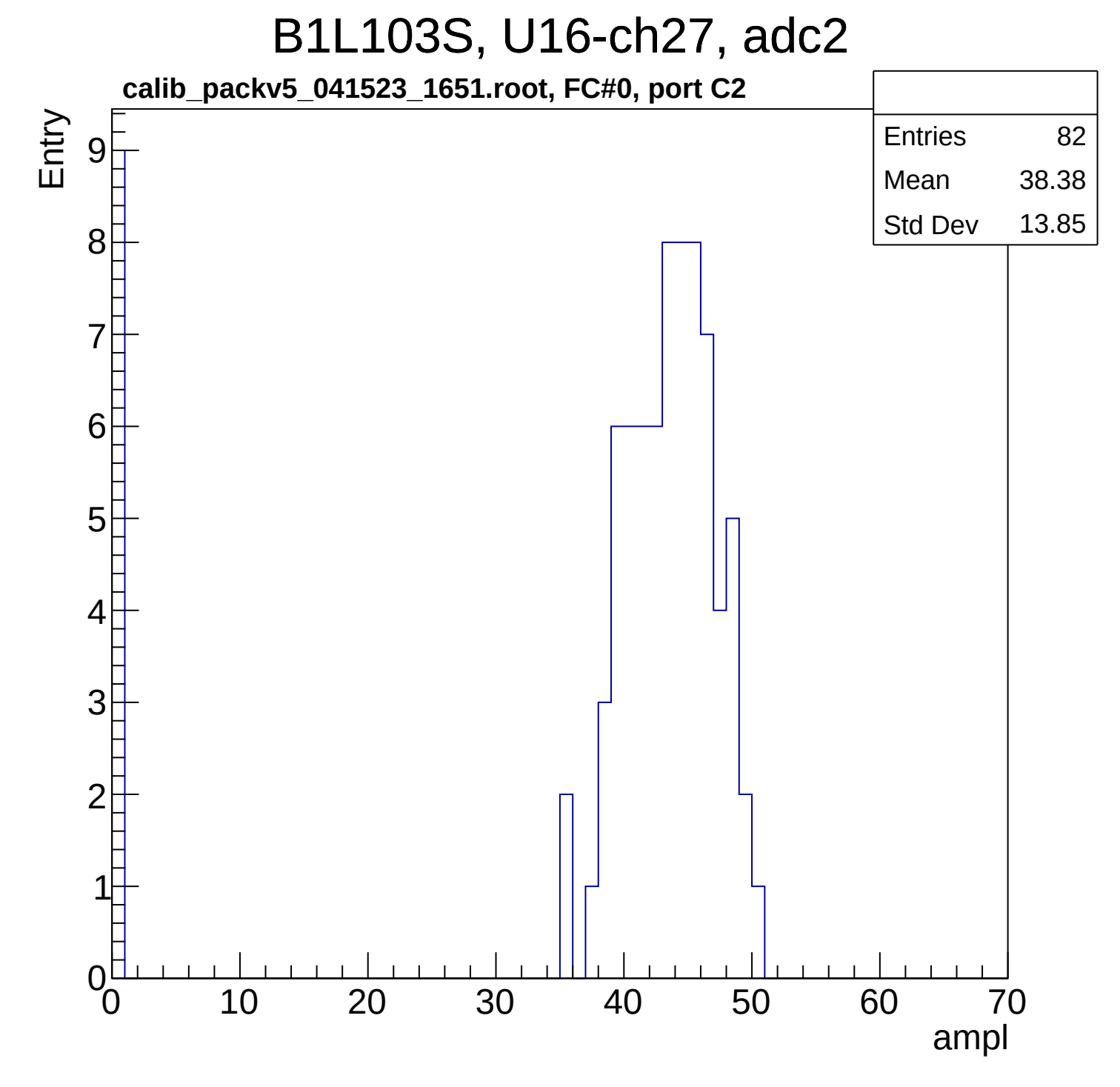
60
70


B1L103S, U16-ch27, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 38.38
Std Dev 13.85
Entry
ampl
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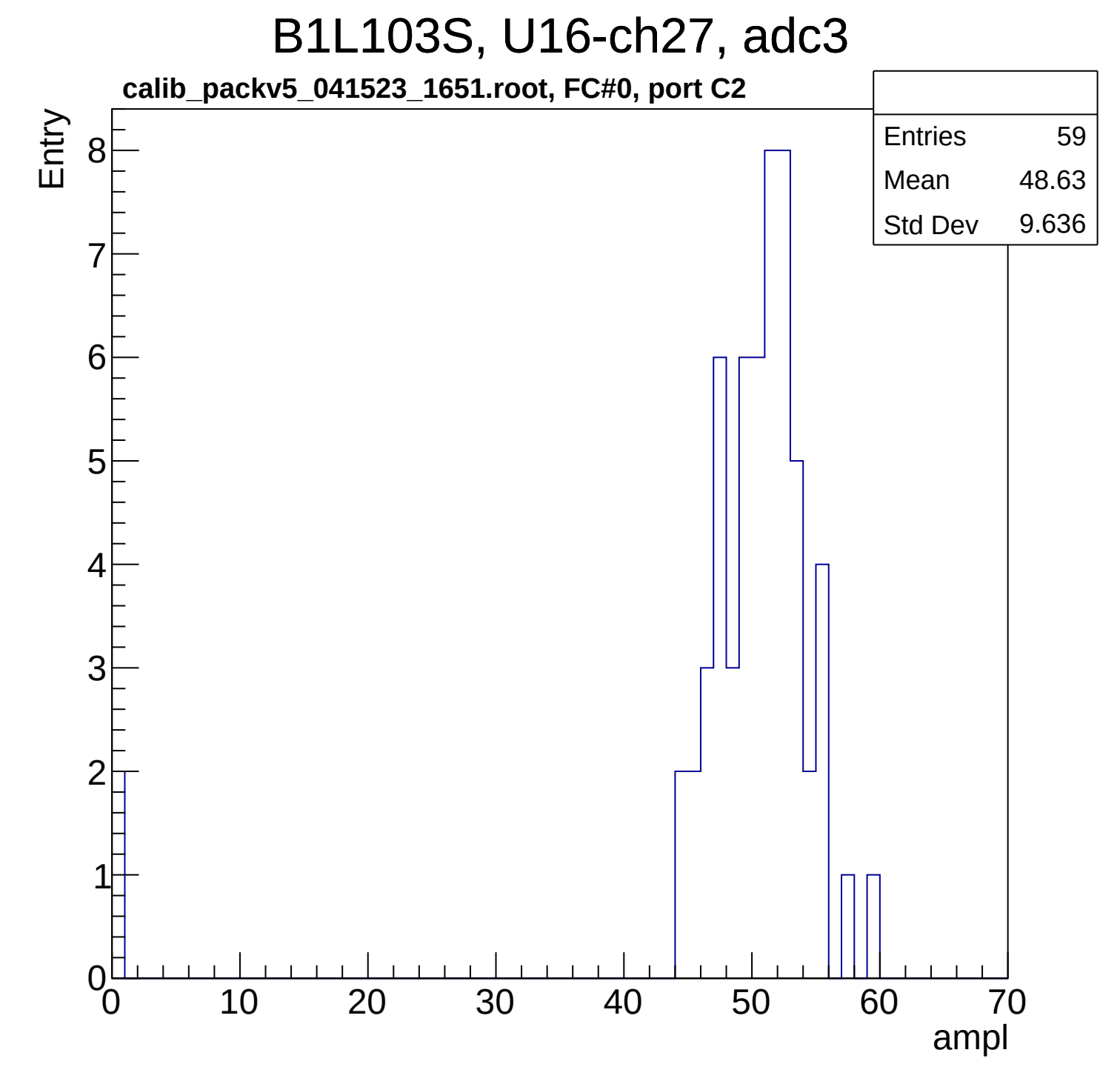
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch27, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 48.63
Std Dev 9.636
Entry
ampl
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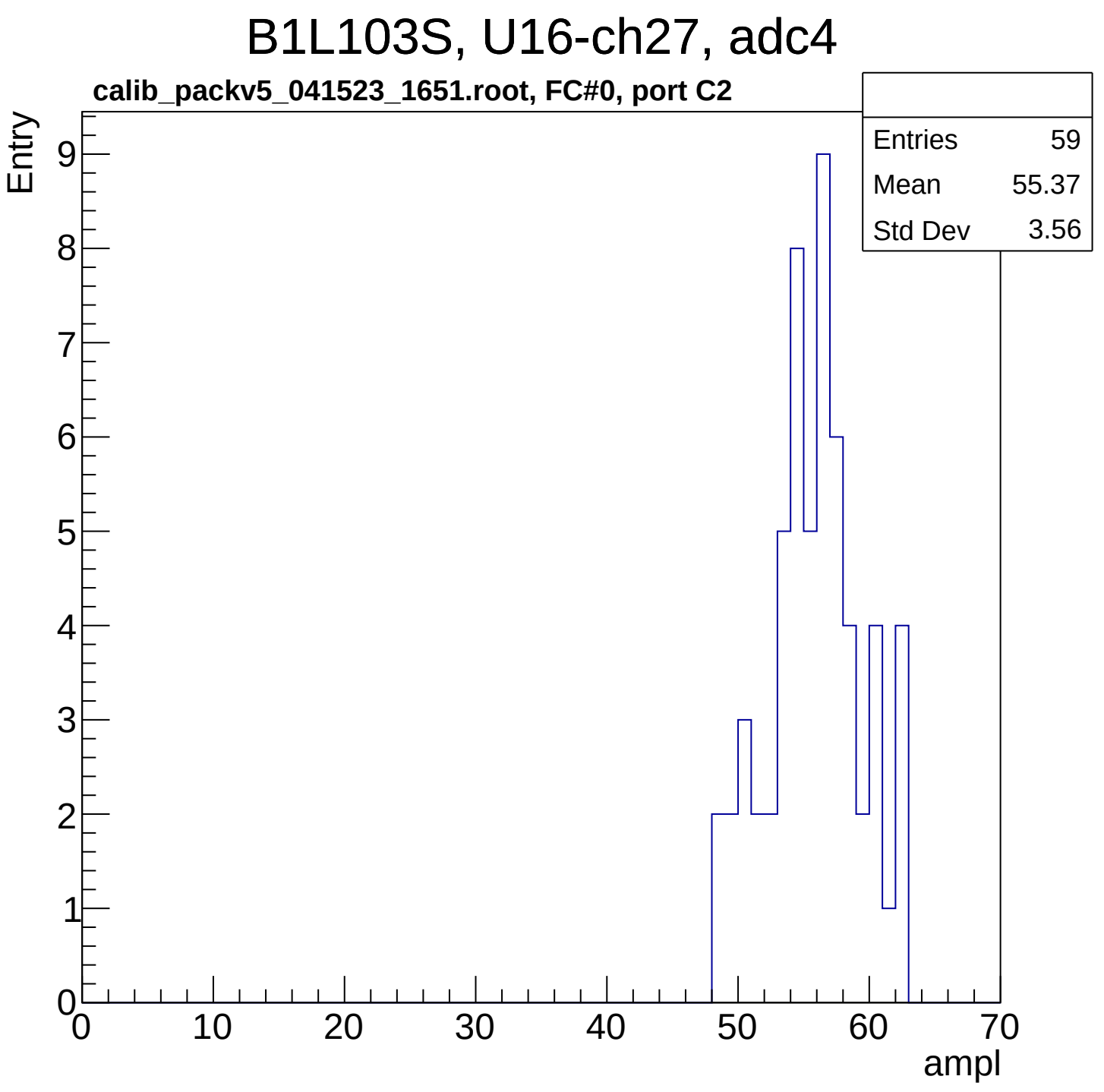
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch27, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 55.37
Std Dev 3.56
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
50
60
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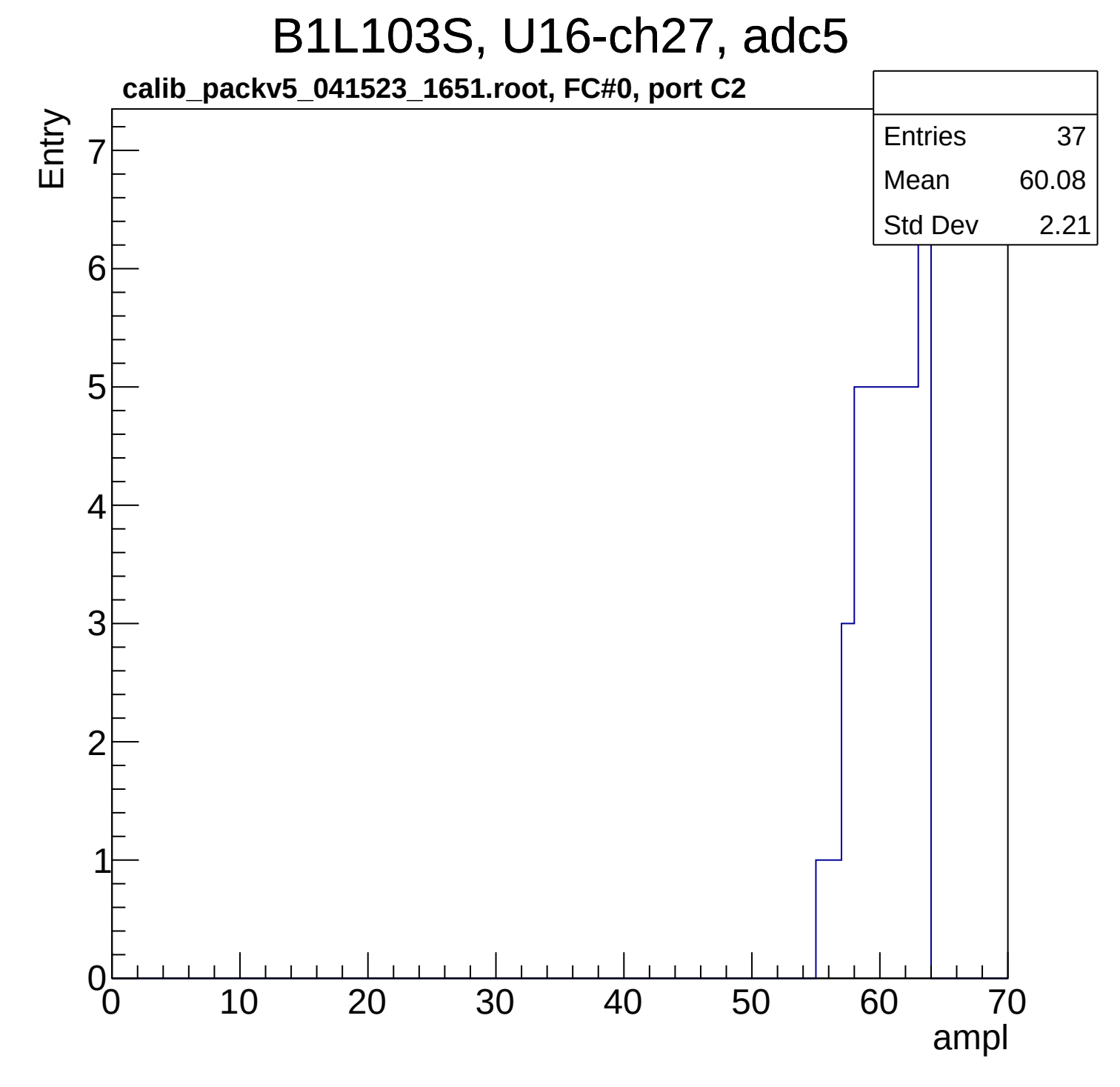
B1L103S, U16-ch27, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 60.08
Std Dev 2.21
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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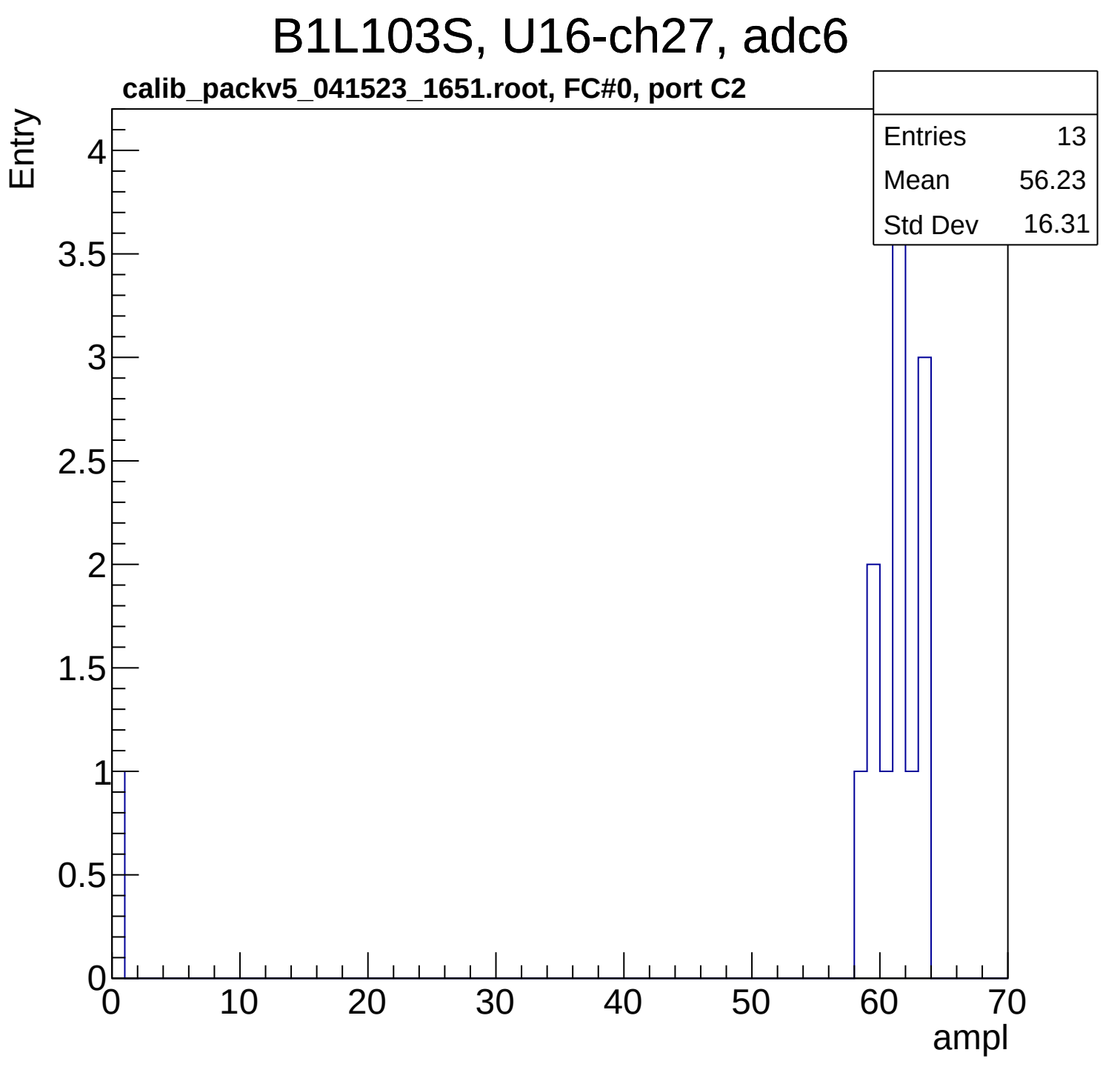
40
50
60
70


B1L103S, U16-ch27, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 56.23
Std Dev 16.31
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
10
20
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40
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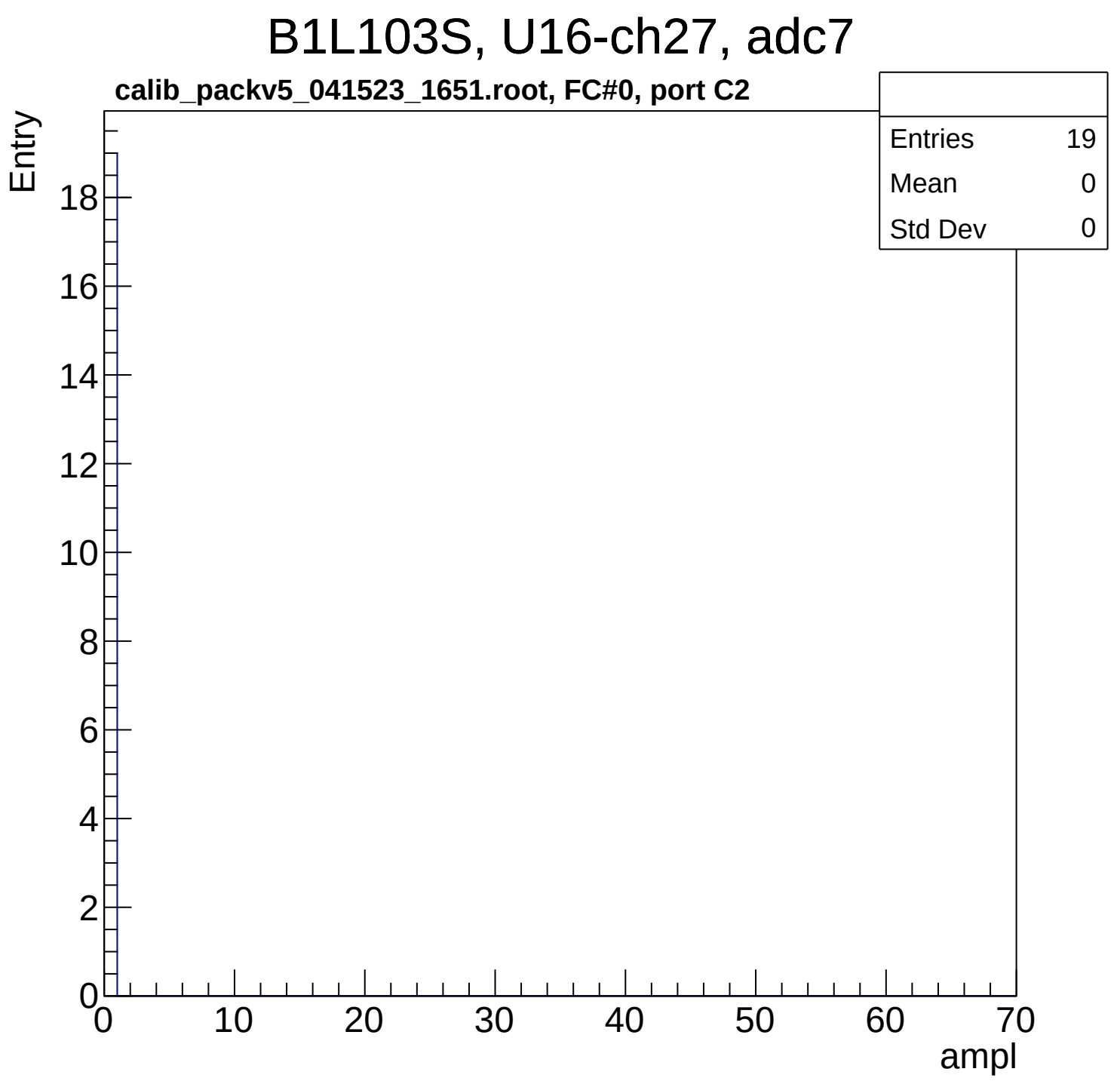
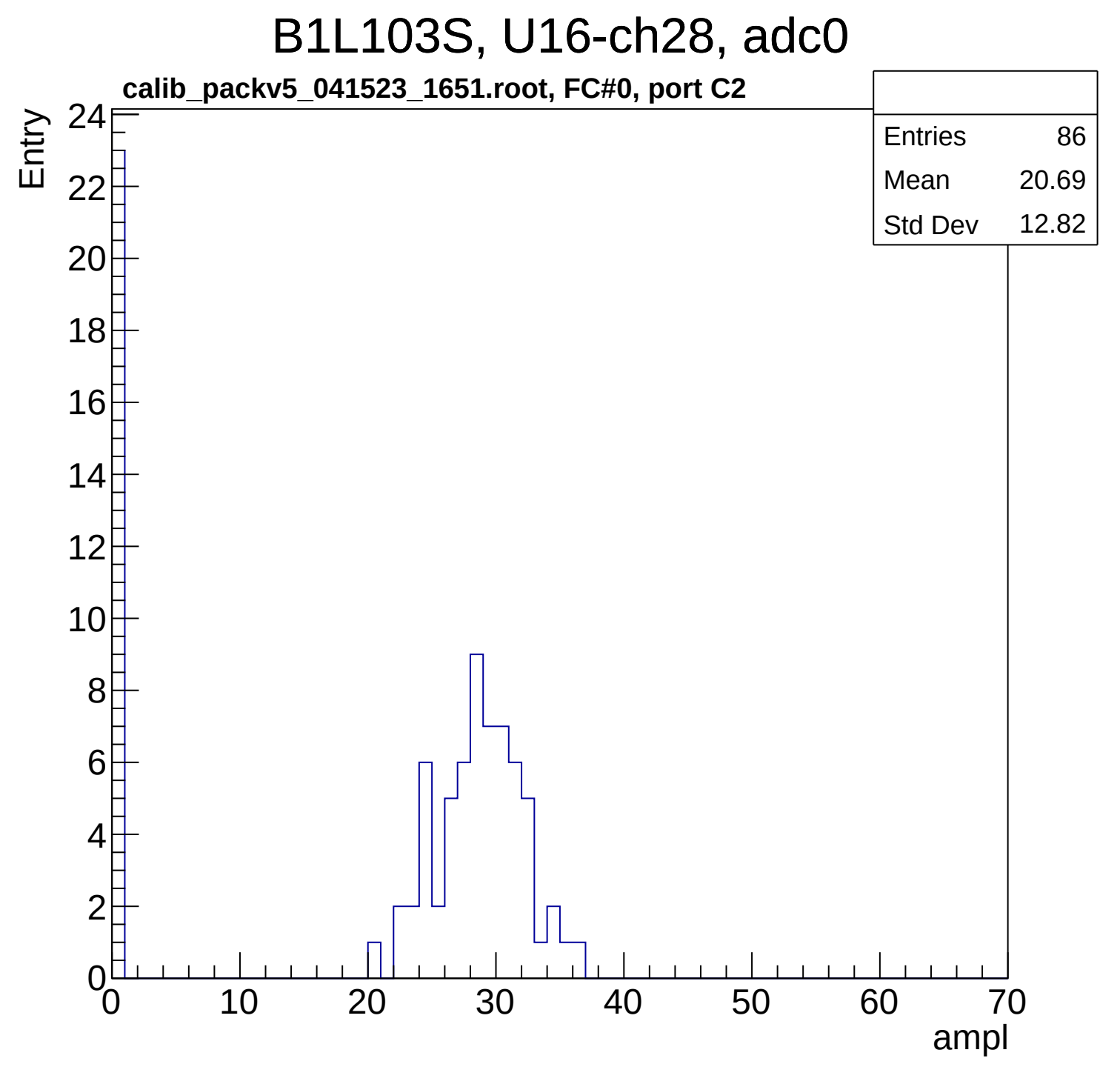
60
70


B1L103S, U16-ch27, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch28, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 20.69
Std Dev 12.82
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
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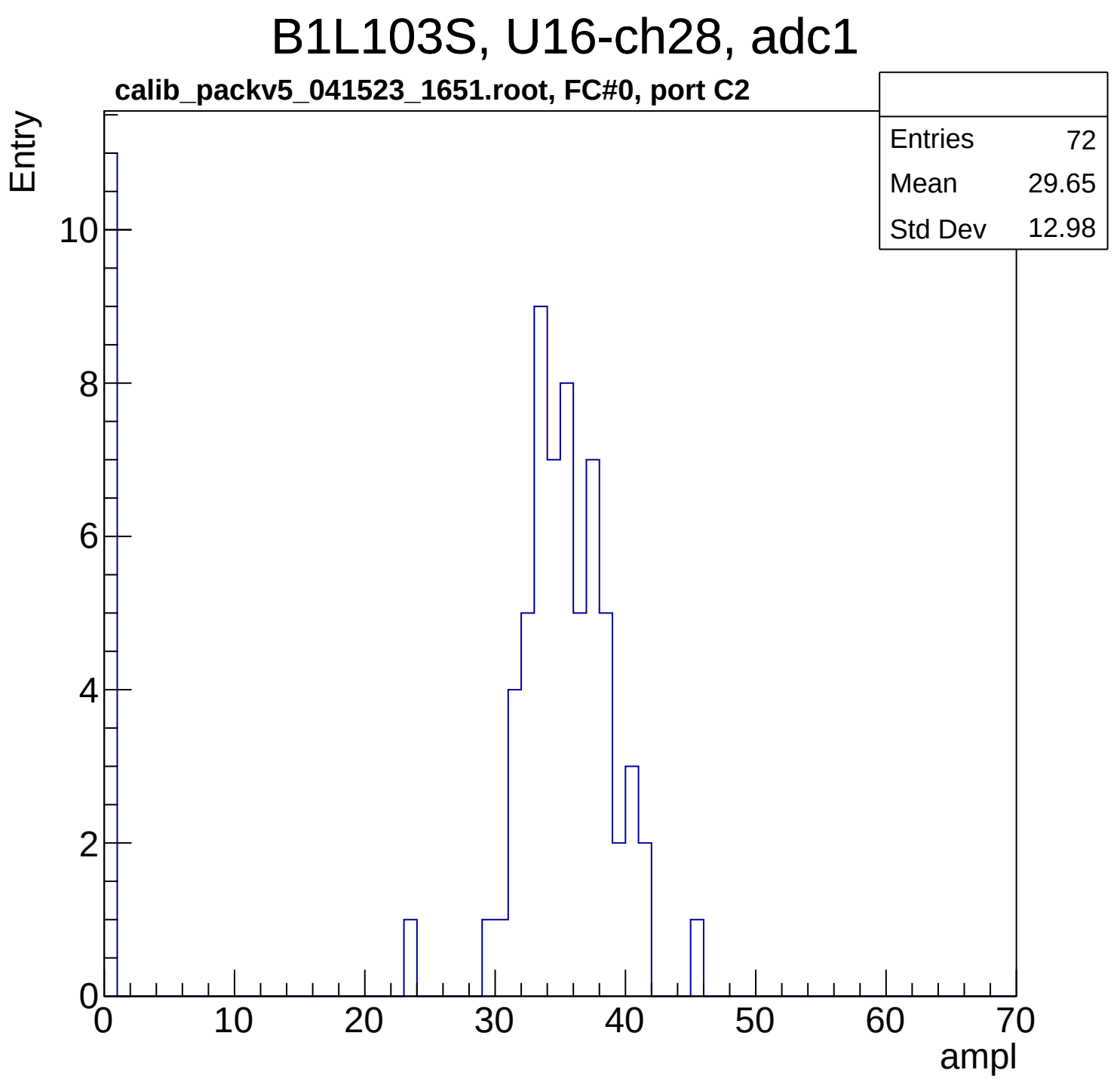
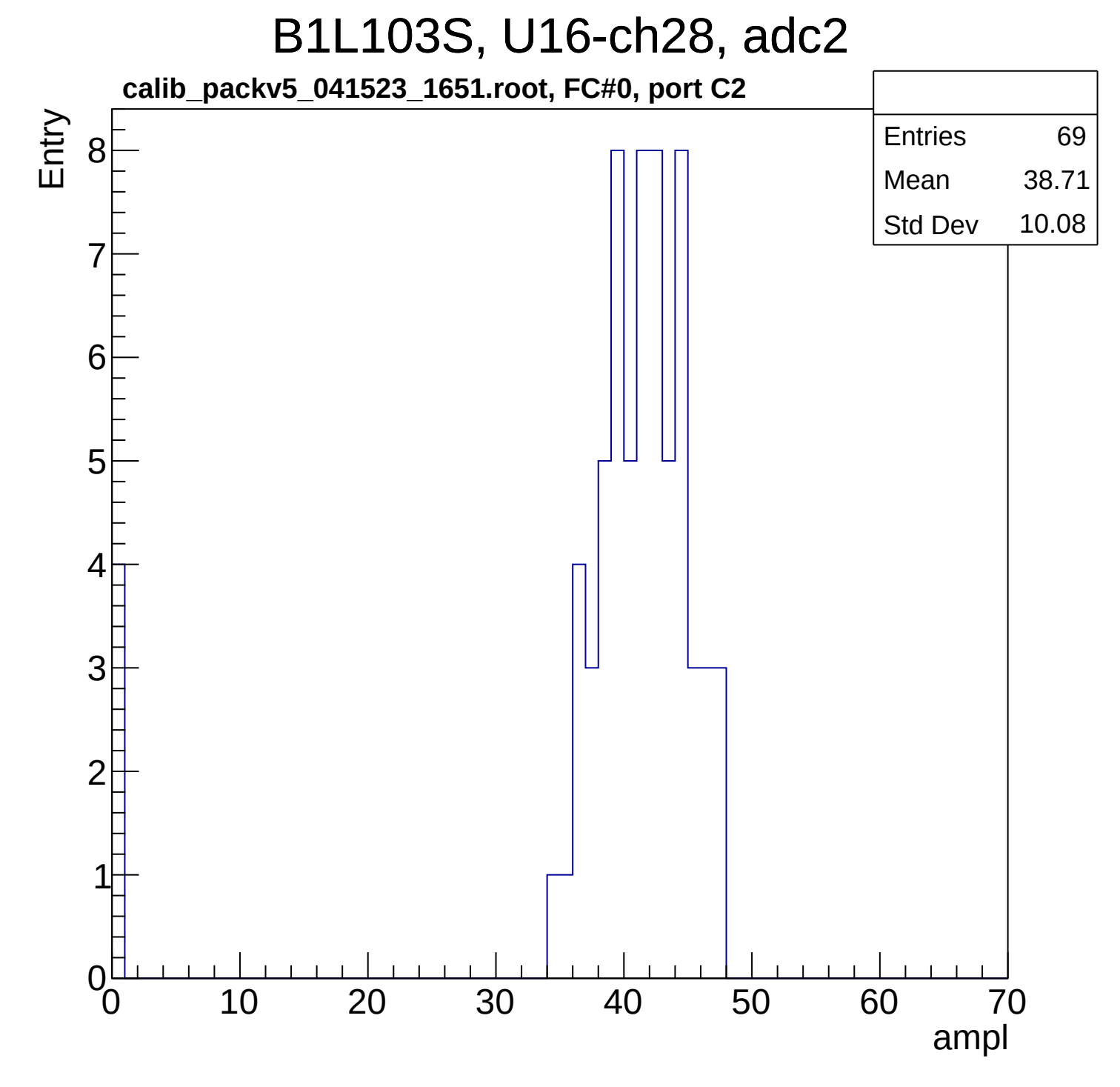
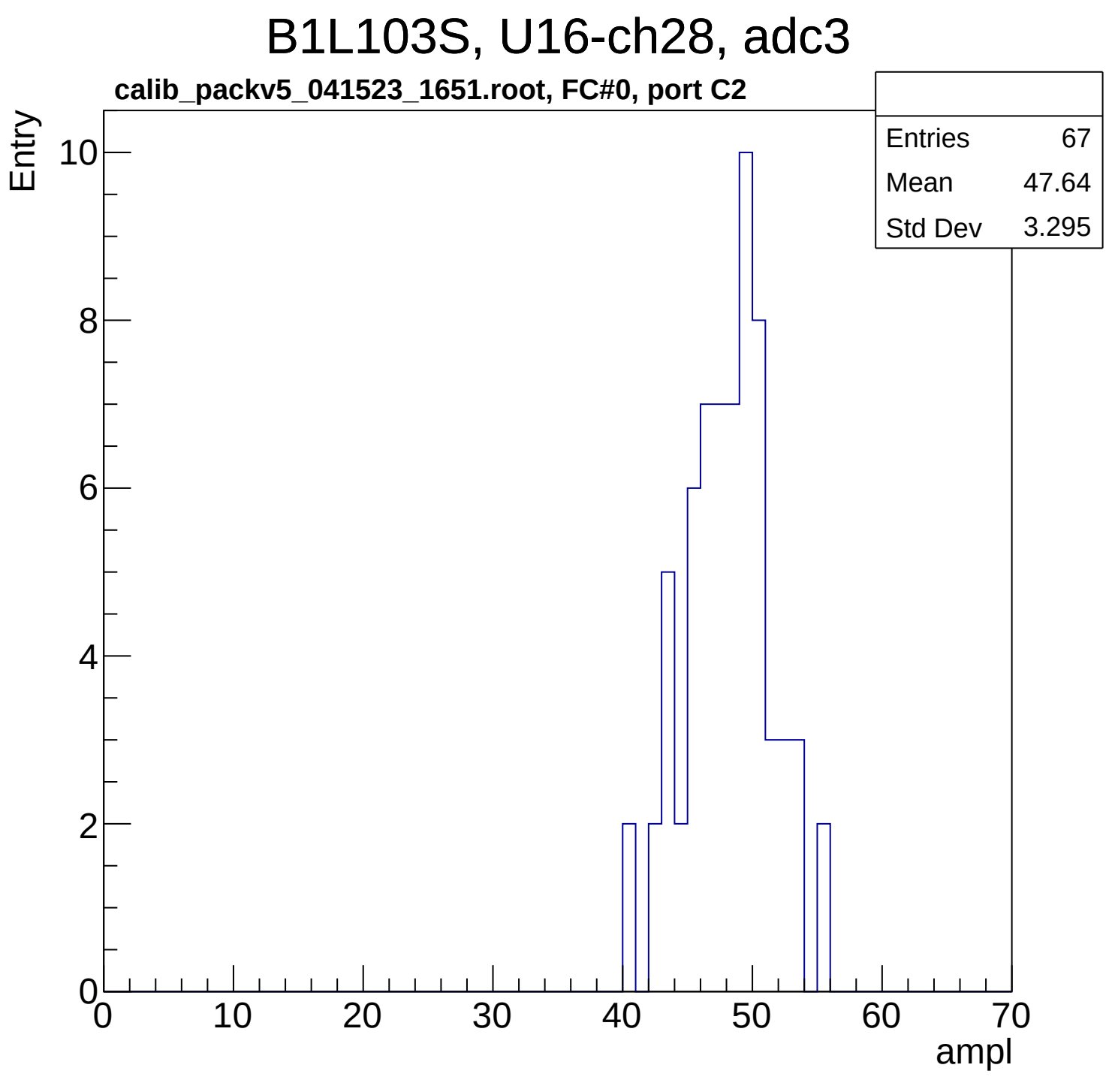
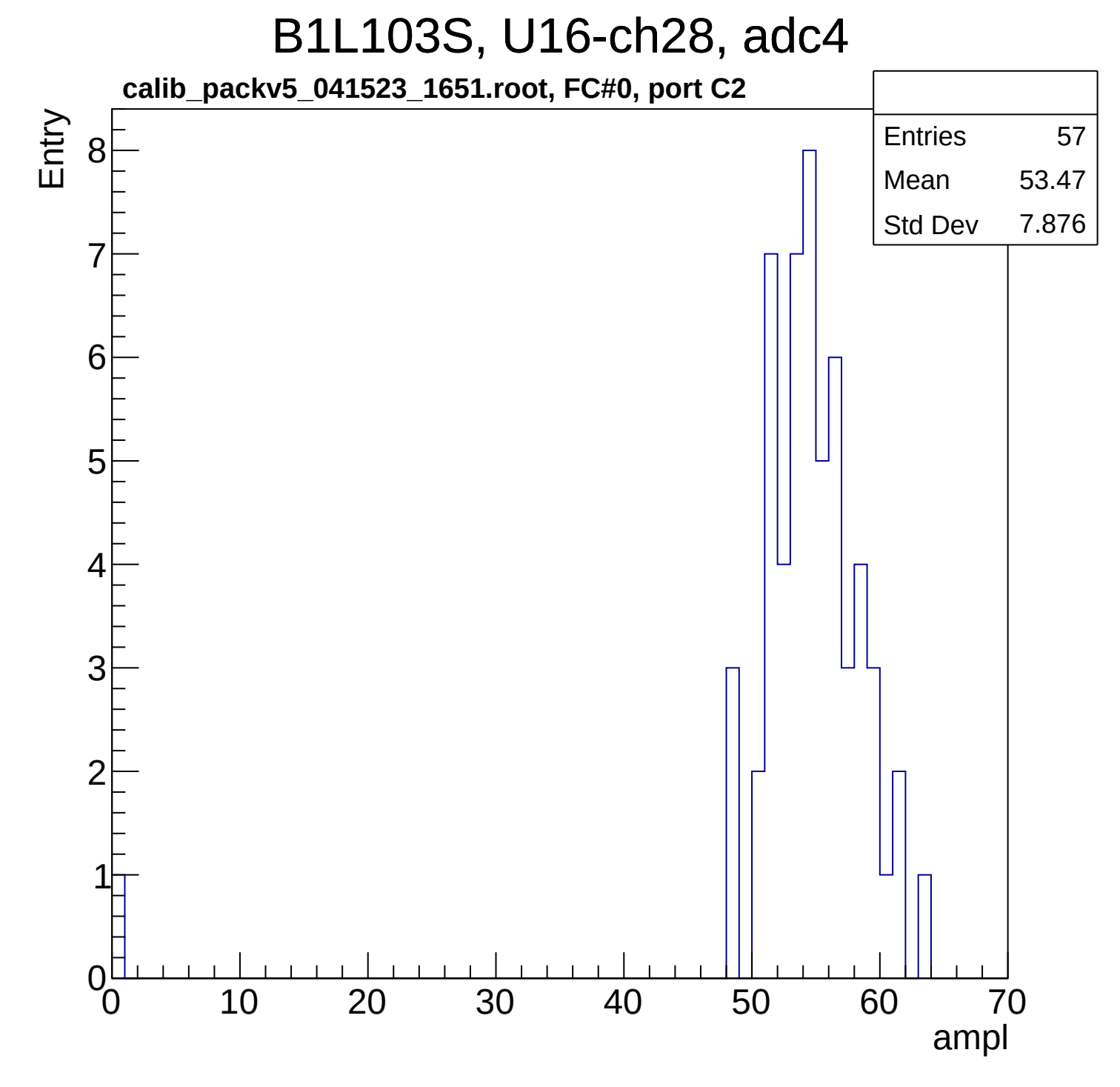
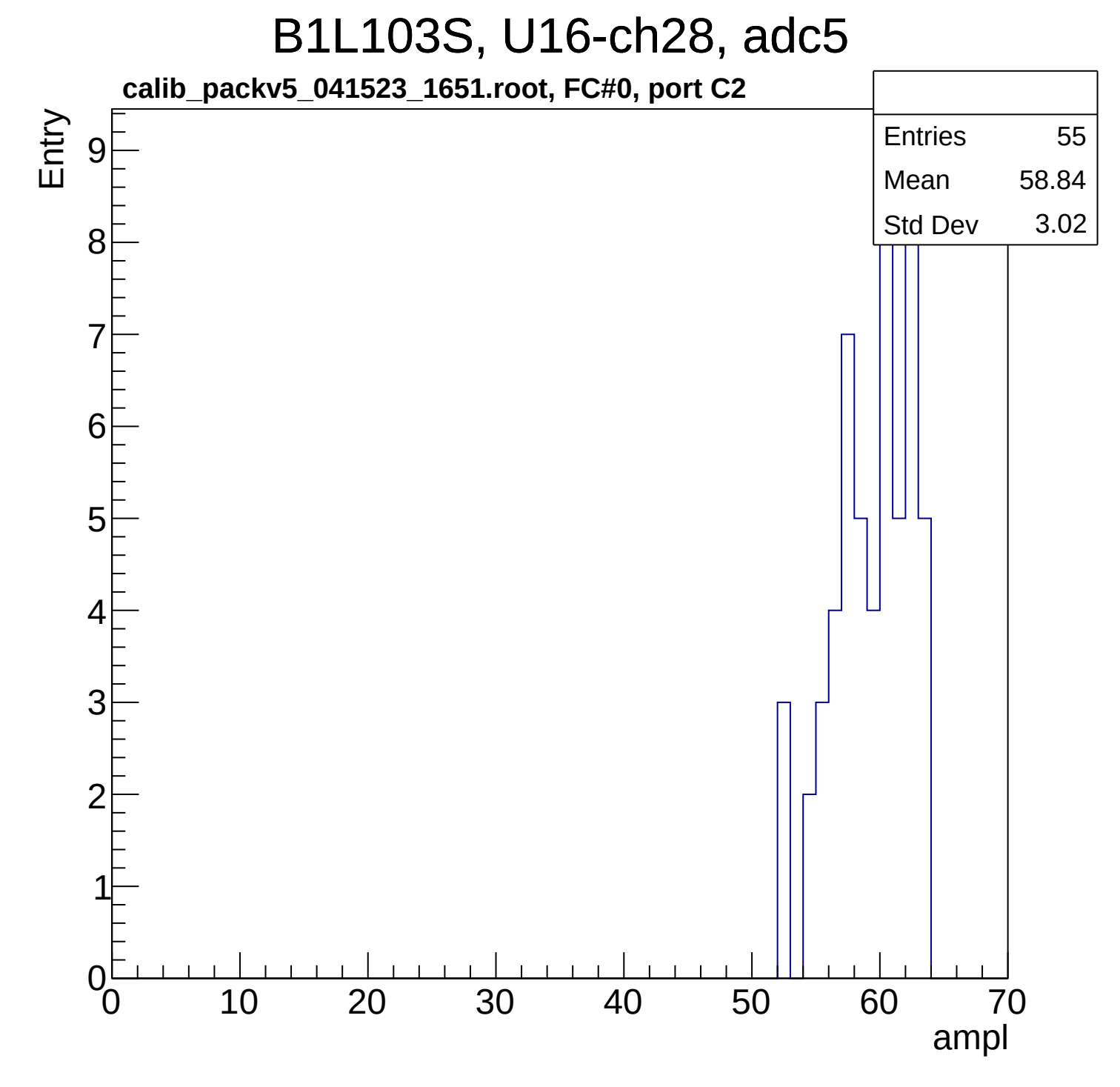
30
40
50
60
70


B1L103S, U16-ch28, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 29.65
Std Dev 12.98
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch28, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 38.71
Std Dev 10.08
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch28, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 47.64
Std Dev 3.295
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch28, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 53.47
Std Dev 7.876
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch28, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.84
Std Dev 3.02
Entry
ampl
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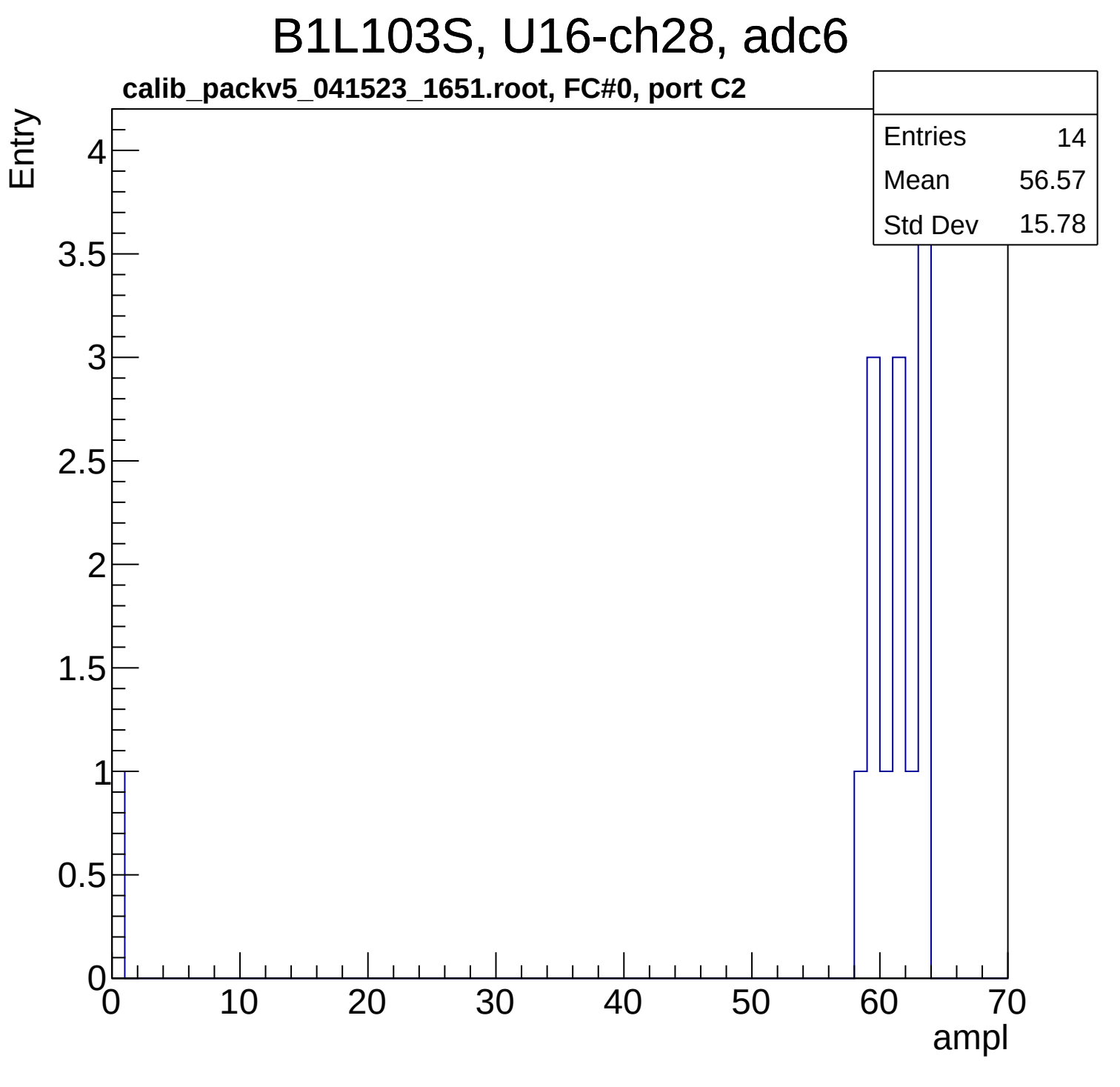
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch28, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 56.57
Std Dev 15.78
Entry
ampl
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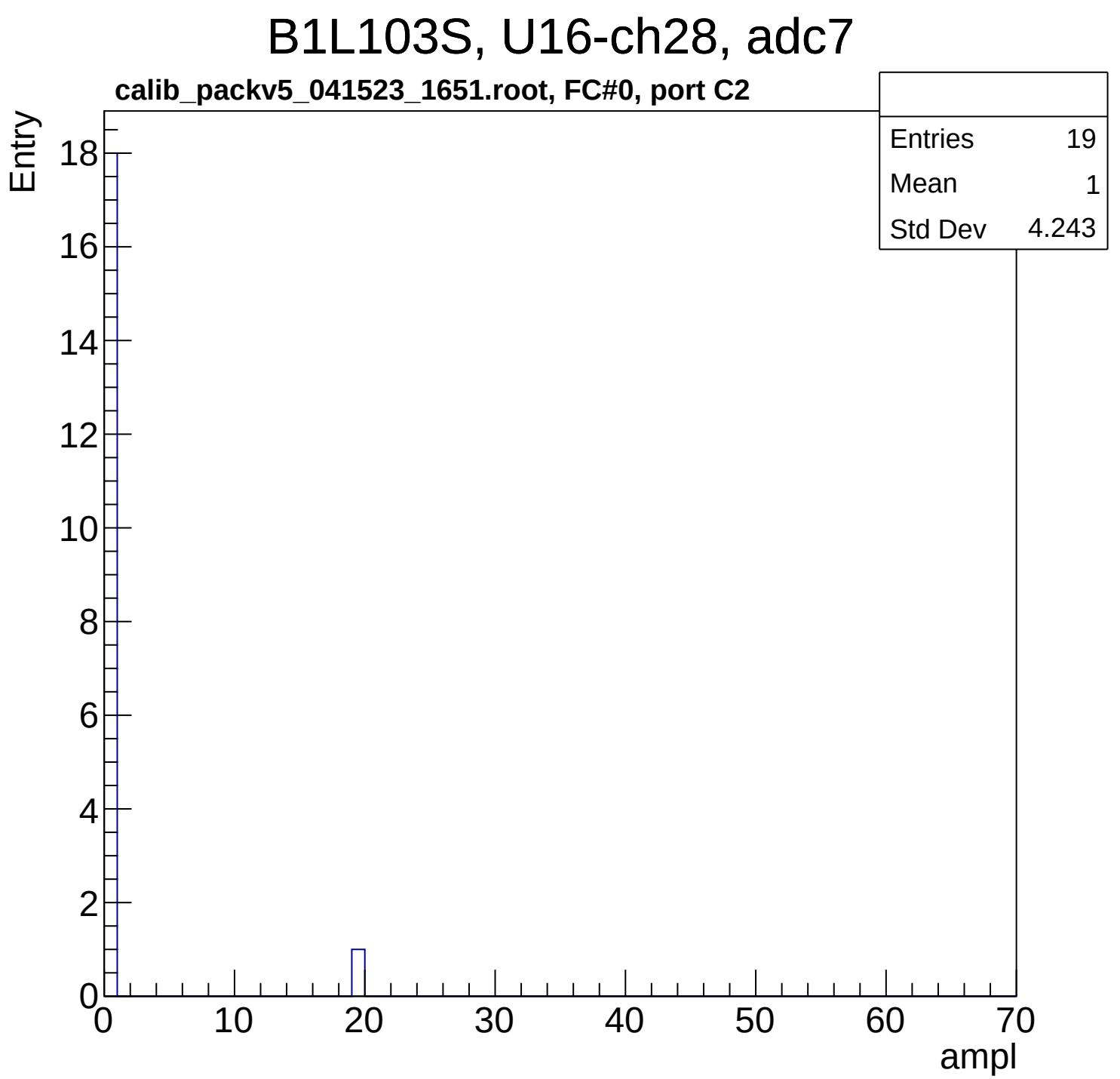
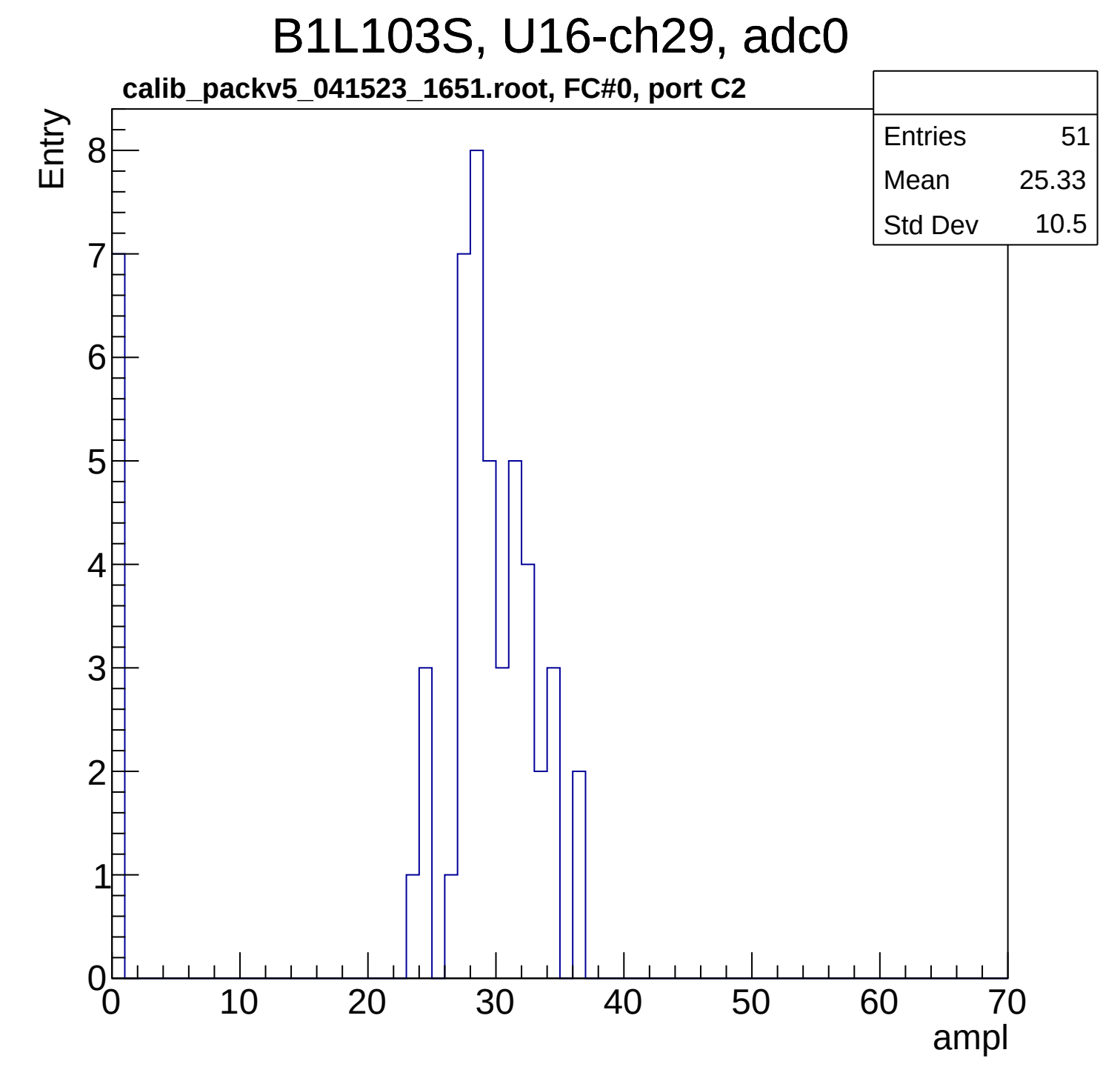
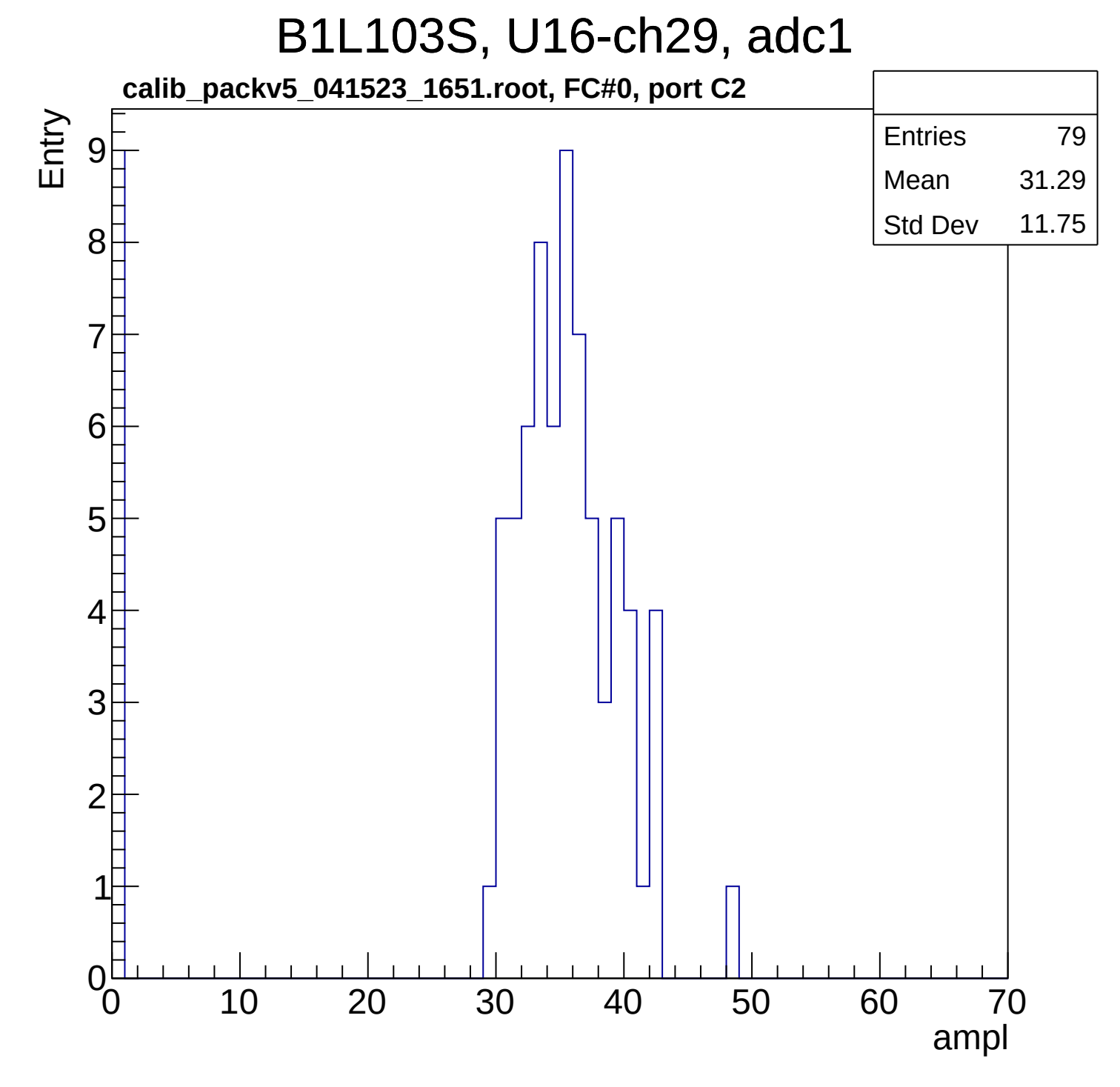
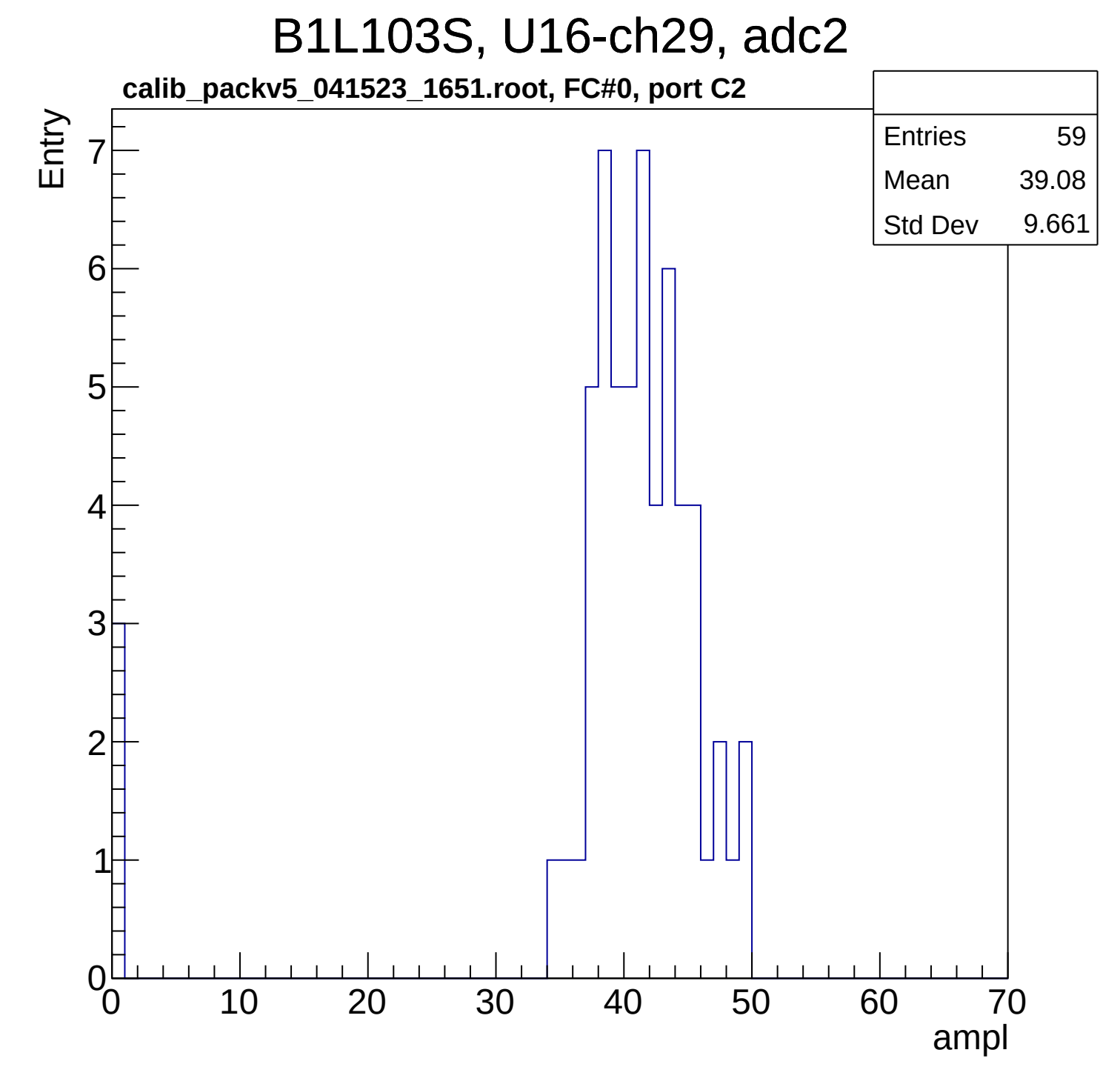
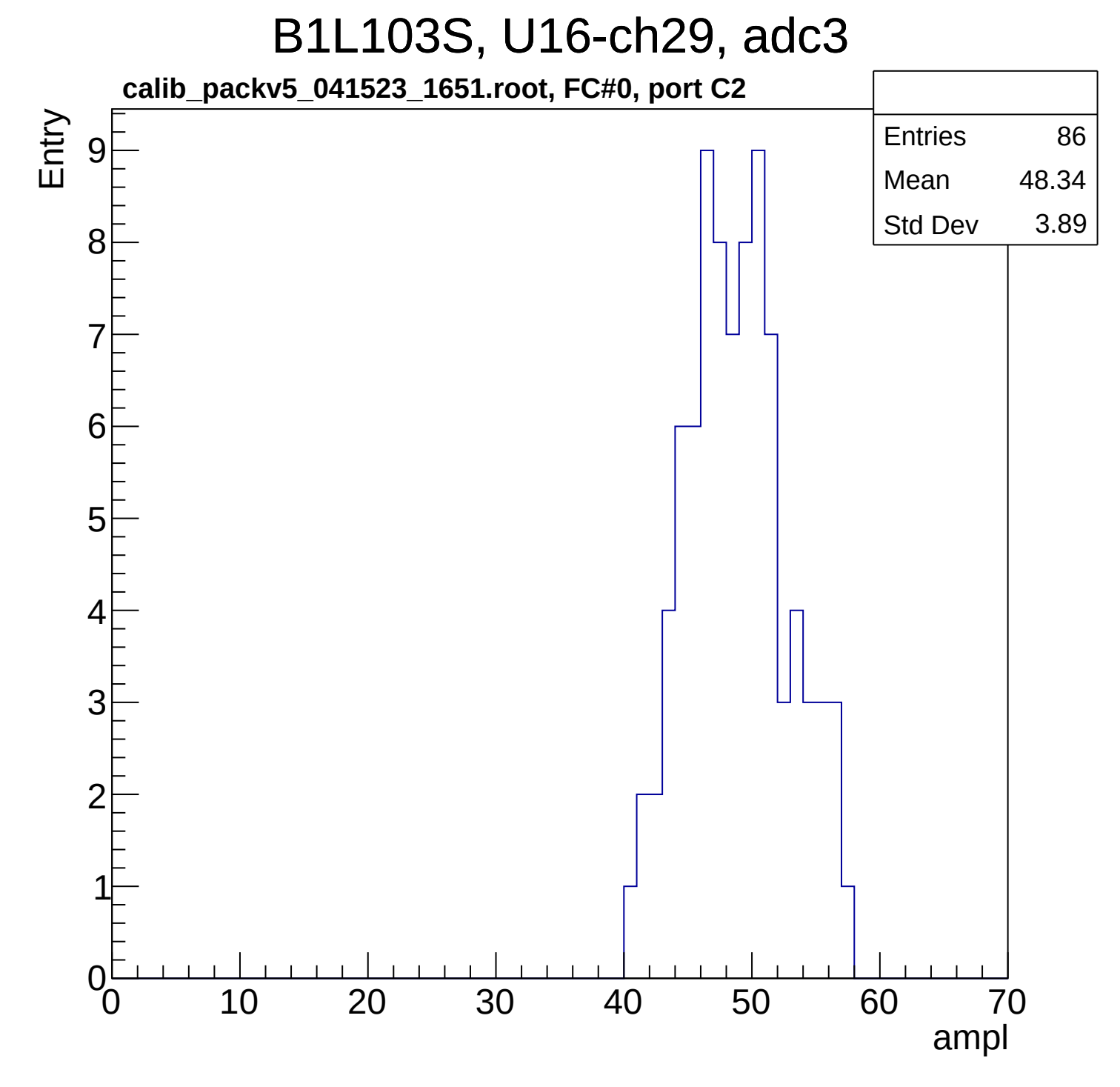
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U16-ch28, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1
Std Dev 4.243
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch29, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 25.33
Std Dev 10.5
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch29, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 31.29
Std Dev 11.75
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch29, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 39.08
Std Dev 9.661
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch29, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 48.34
Std Dev 3.89
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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40
50
60
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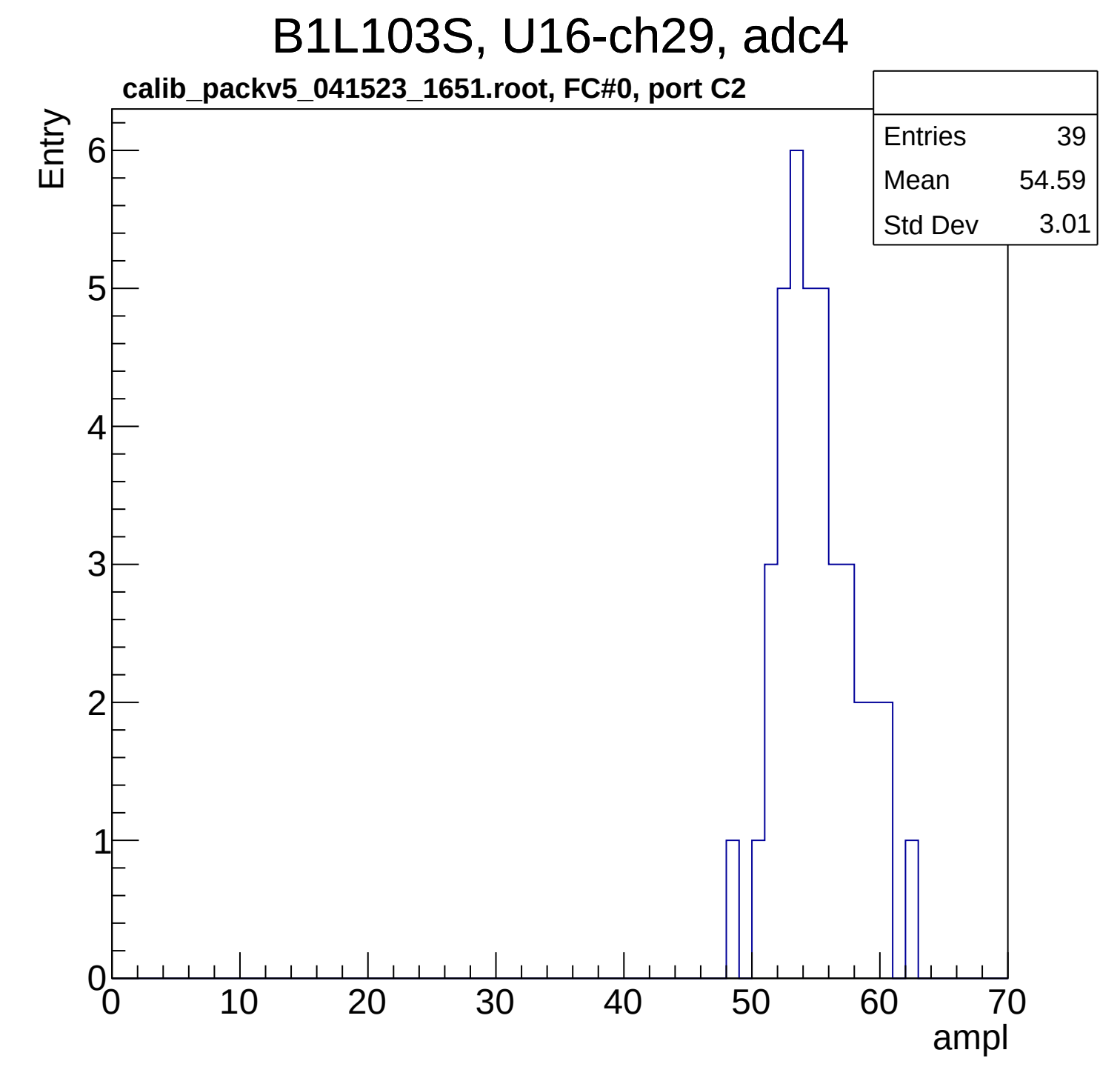
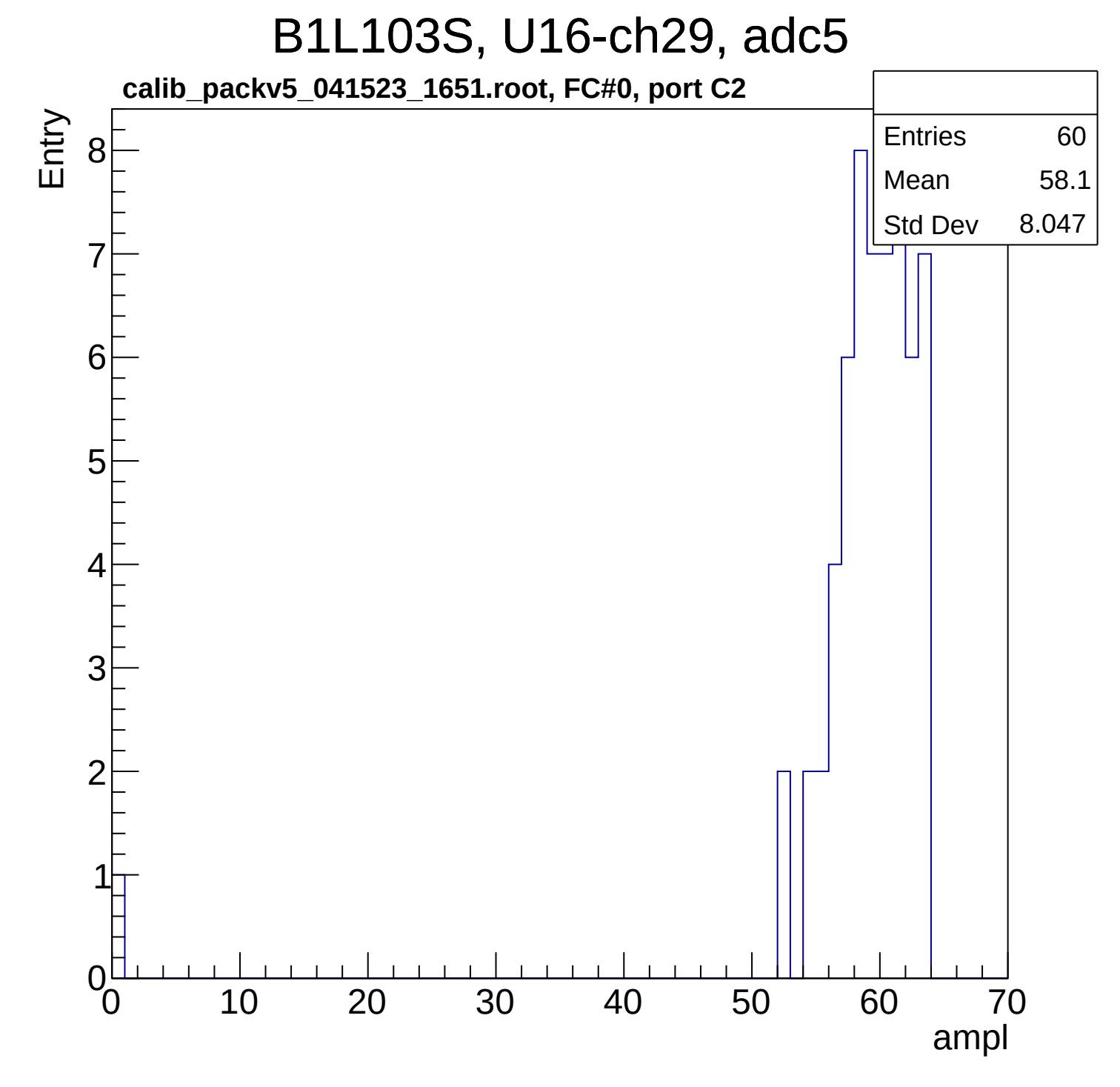

B1L103S, U16-ch29, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 54.59
Std Dev 3.01
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U16-ch29, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 58.1
Std Dev 8.047
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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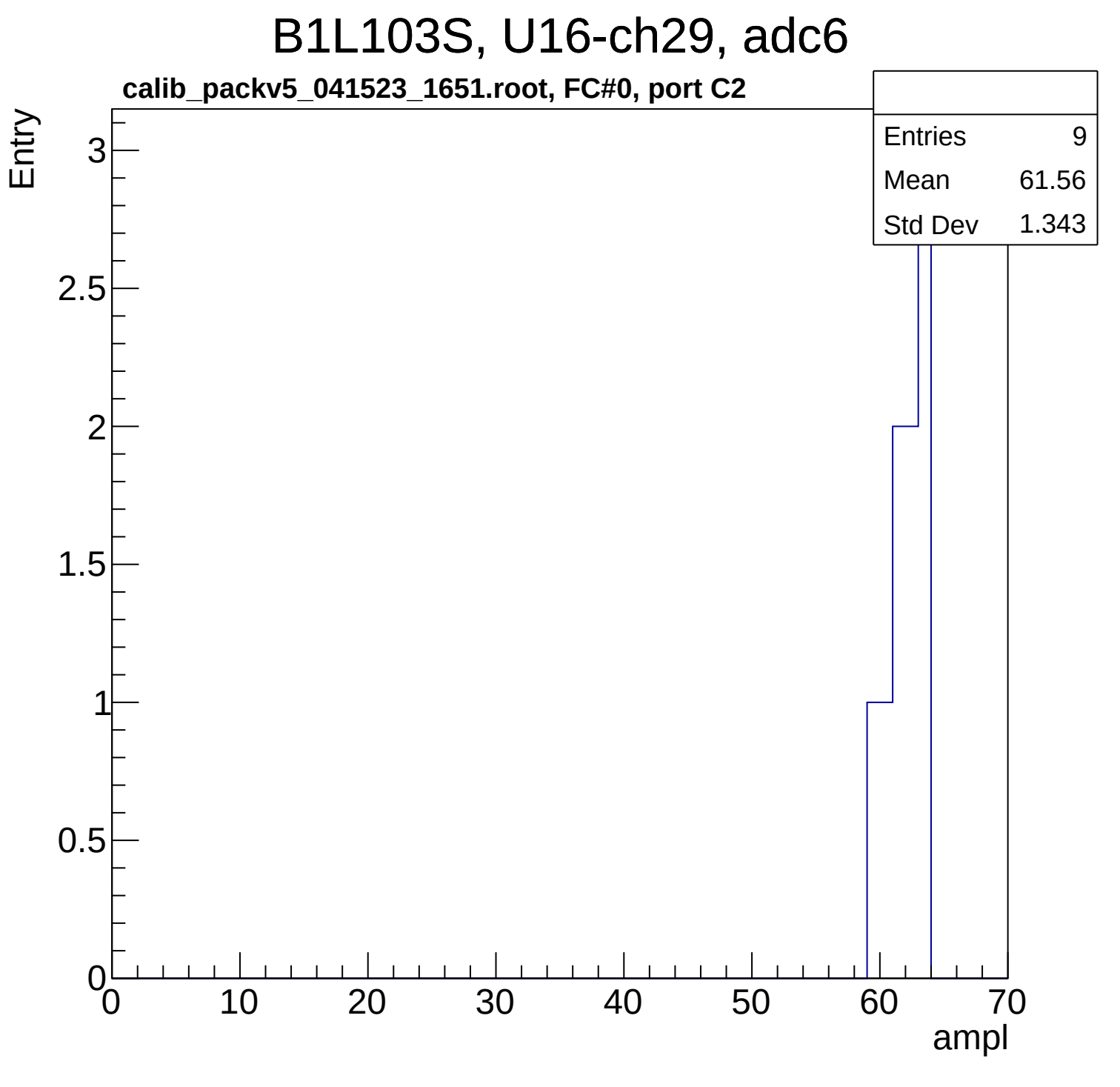
B1L103S, U16-ch29, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.56
Std Dev 1.343
Entry
ampl
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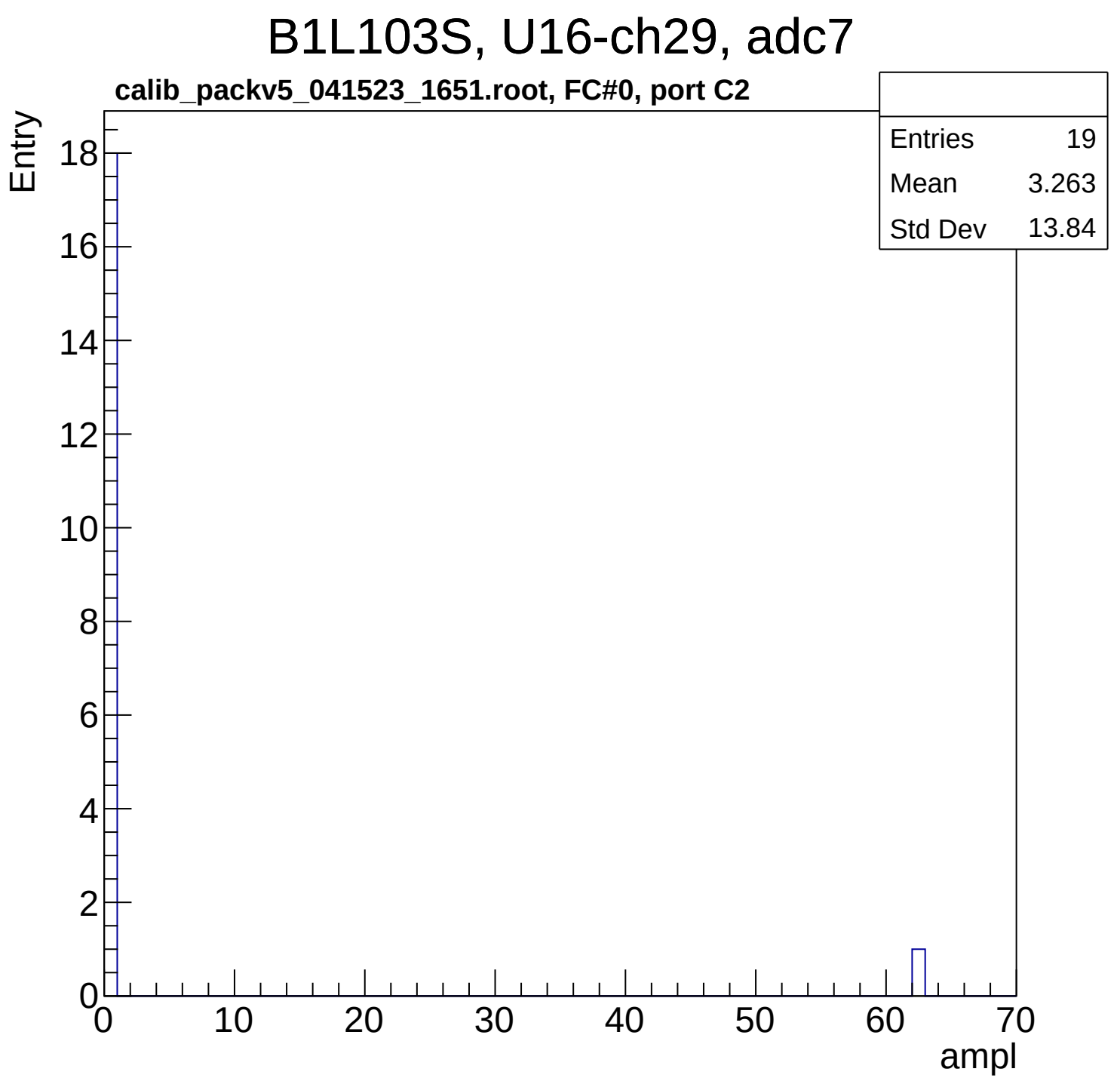
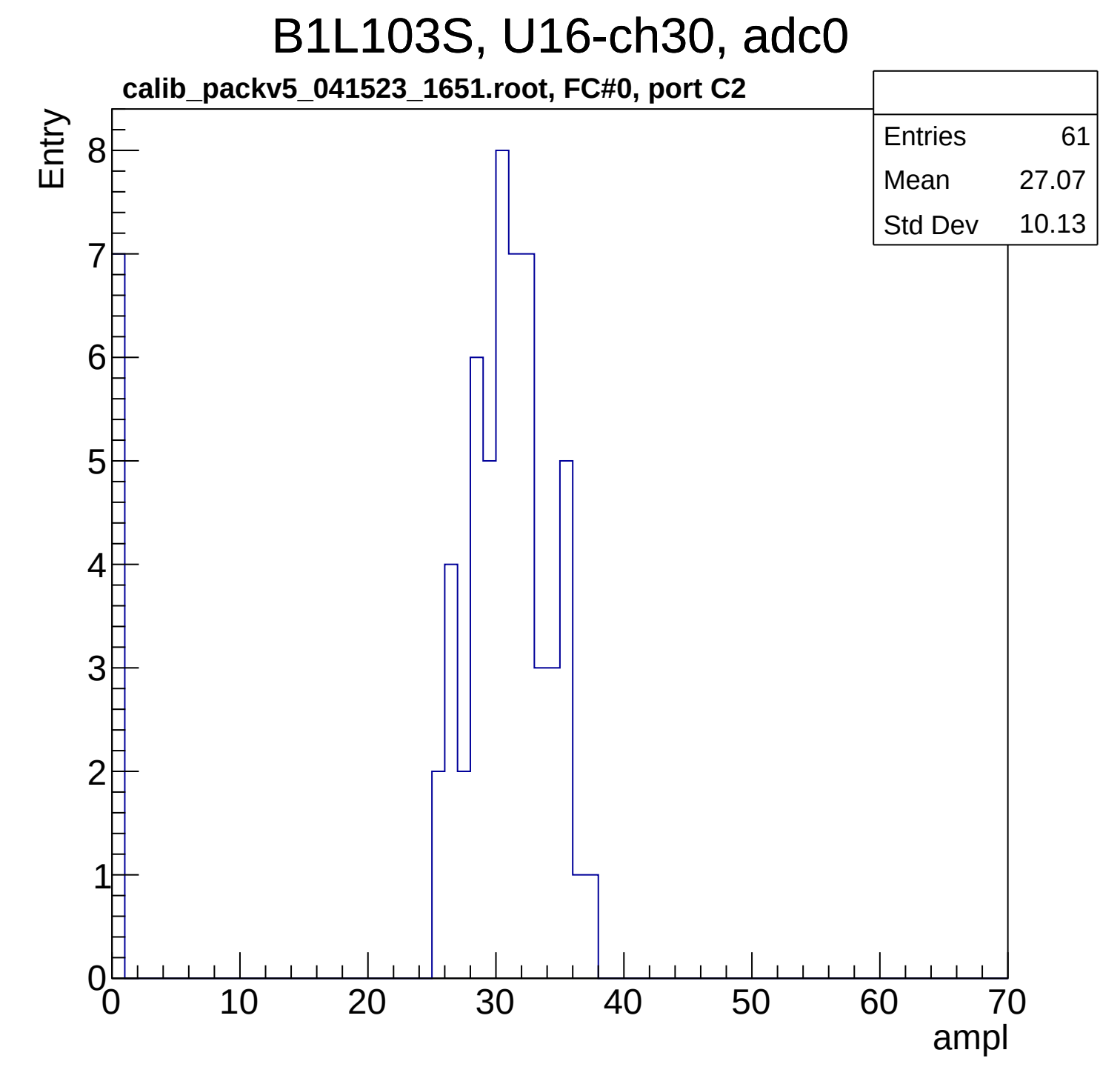
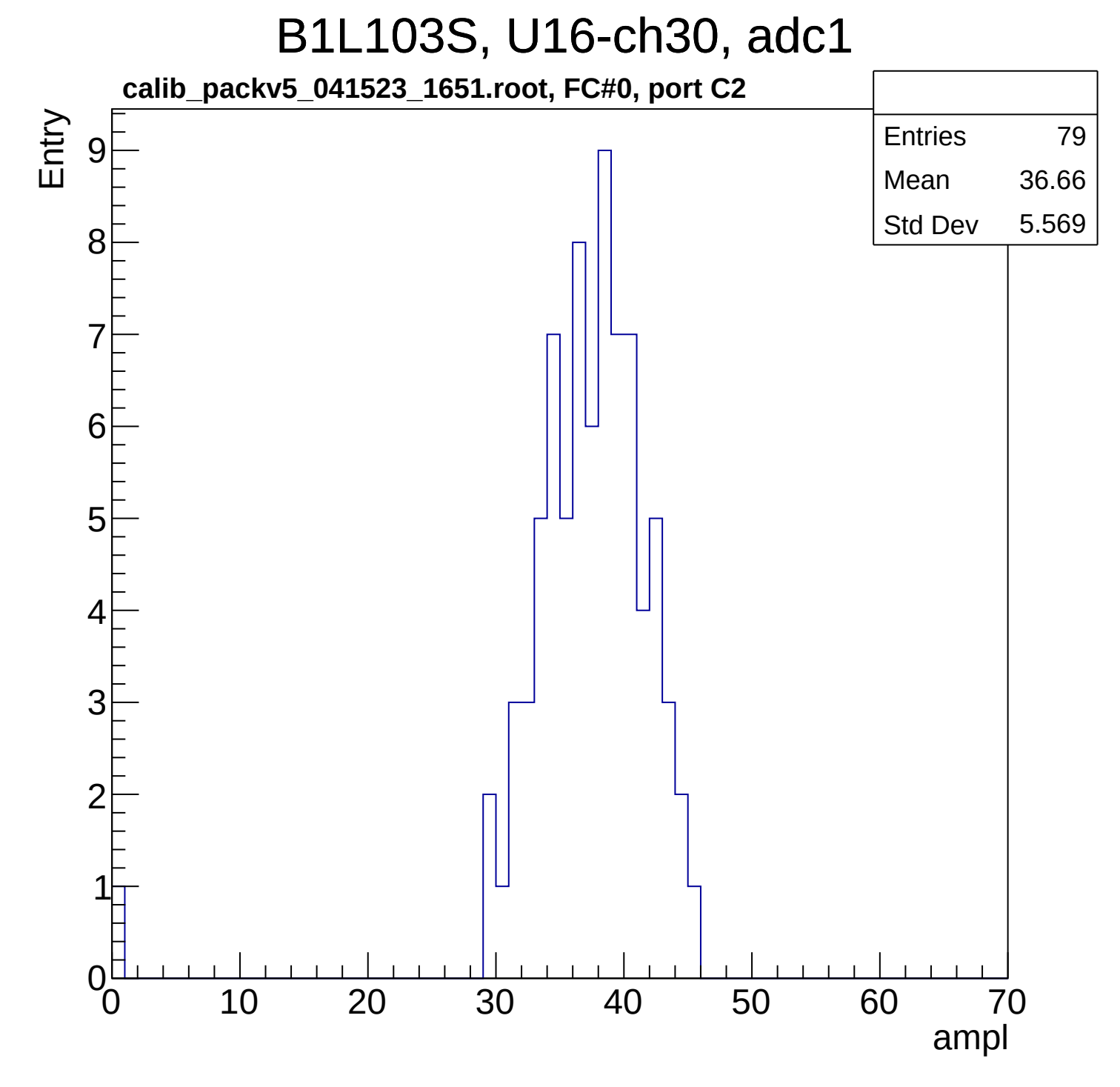
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U16-ch29, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.263
Std Dev 13.84
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch30, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 27.07
Std Dev 10.13
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch30, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 36.66
Std Dev 5.569
Entry
ampl
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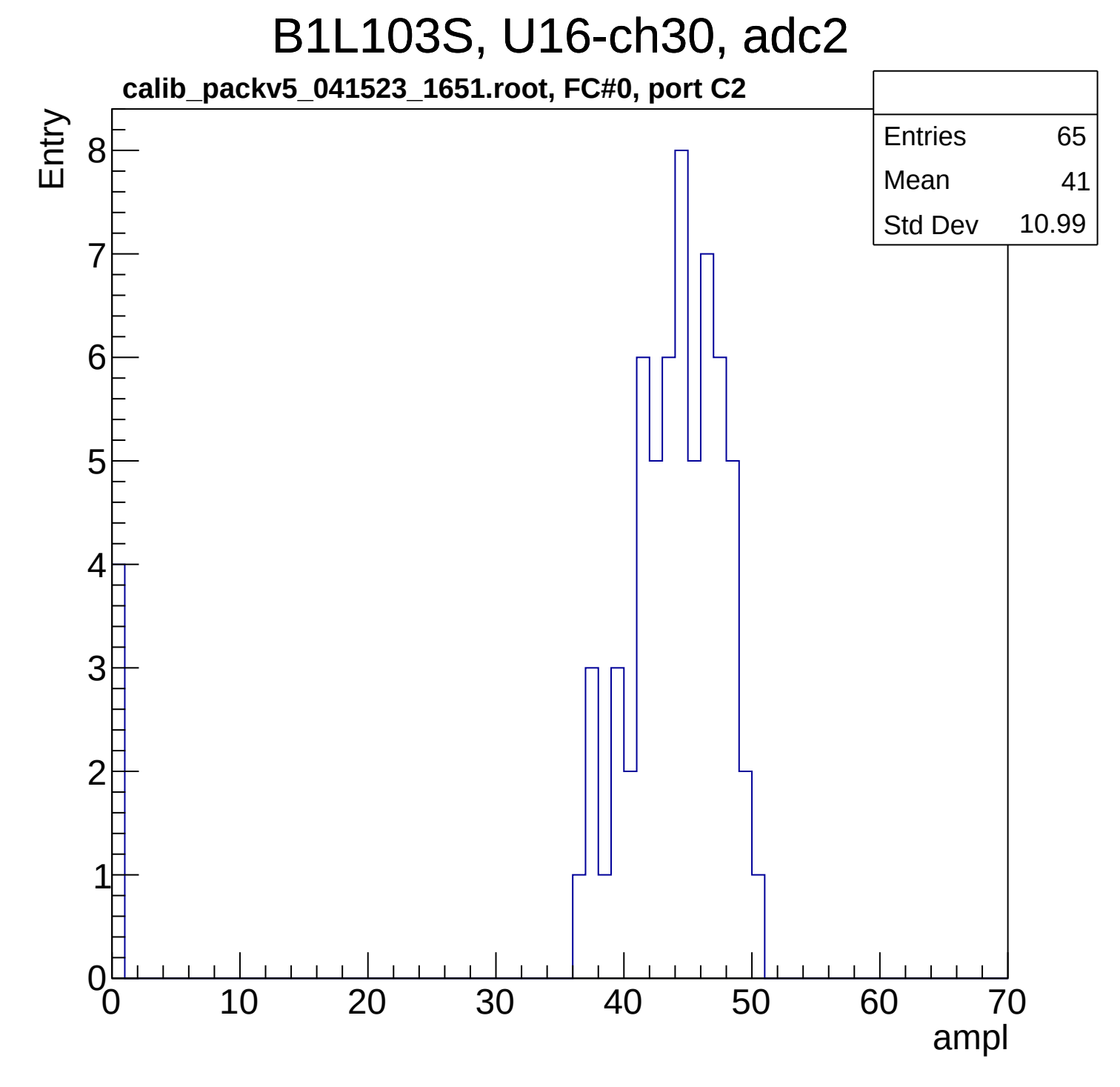
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch30, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 41
Std Dev 10.99
Entry
ampl
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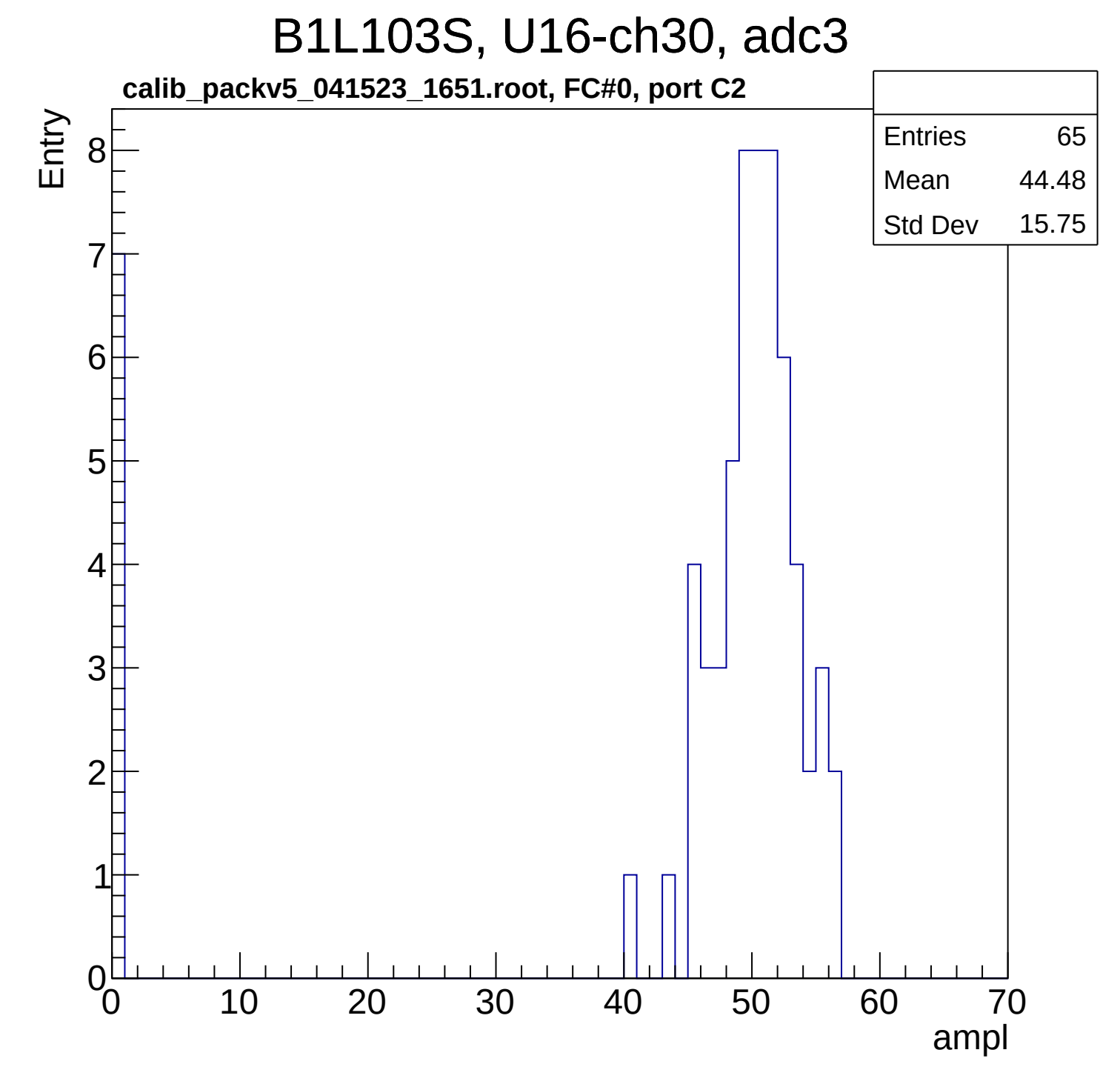
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch30, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 44.48
Std Dev 15.75
Entry
ampl
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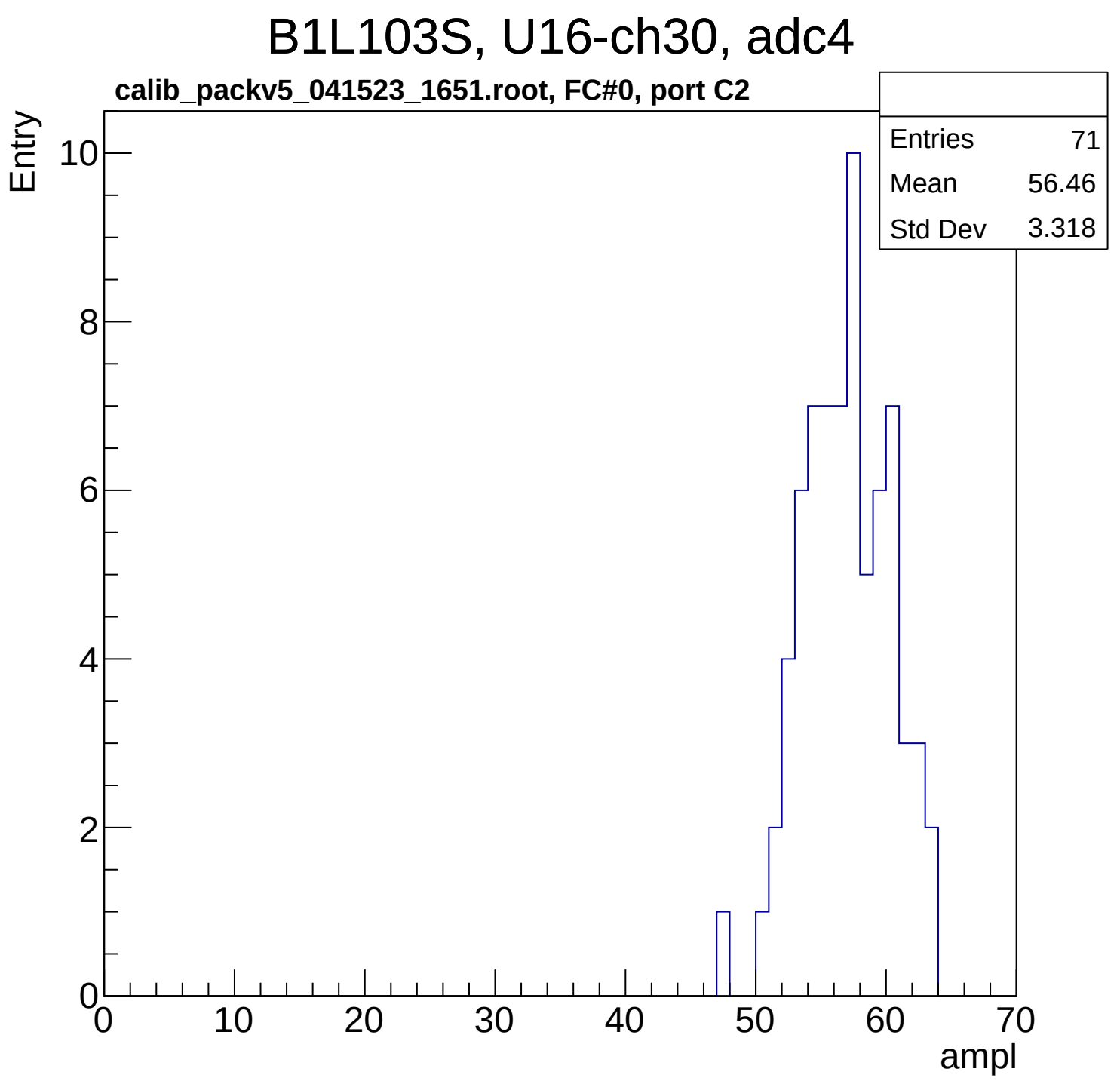
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch30, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 56.46
Std Dev 3.318
Entry
ampl
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2
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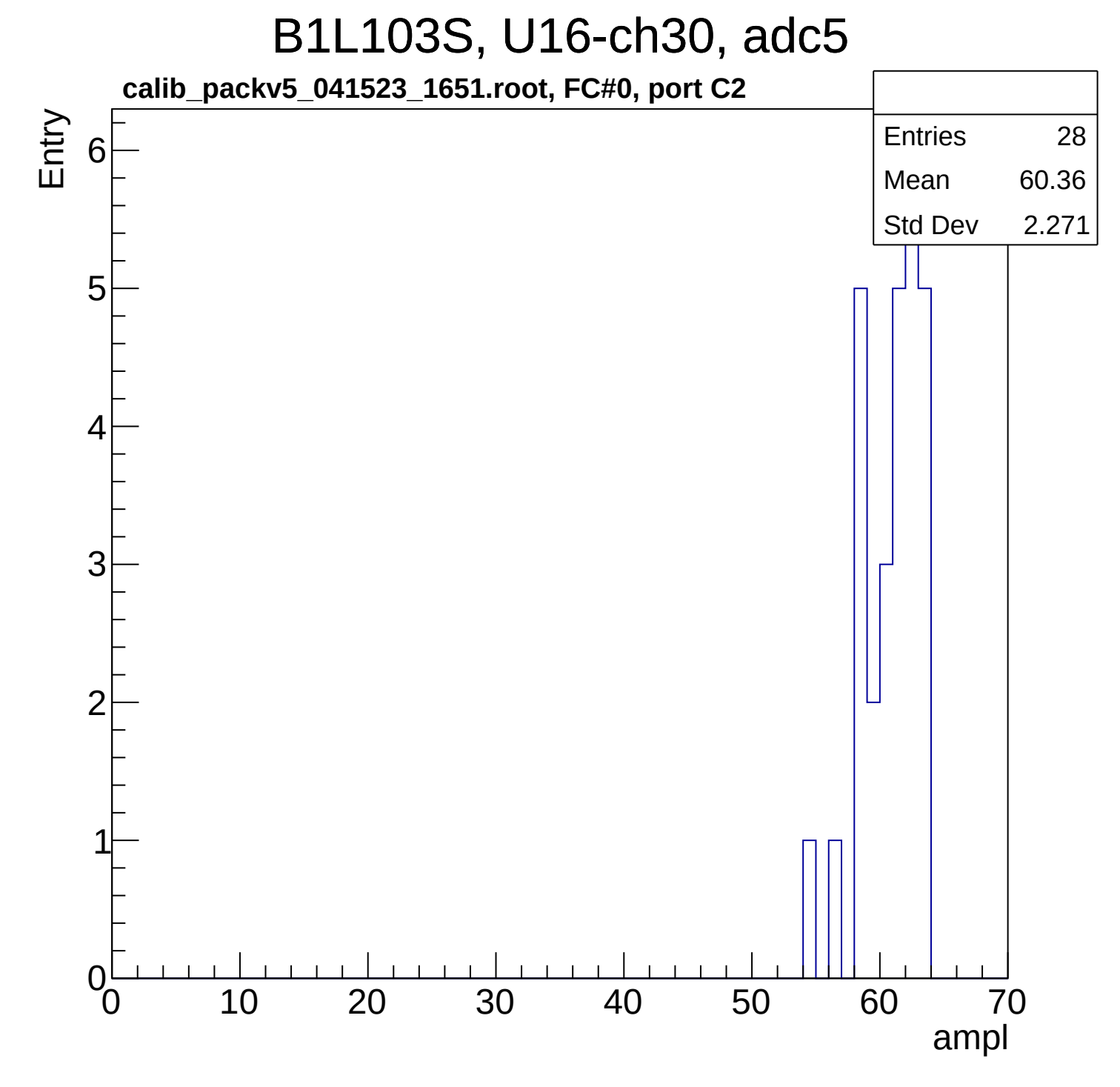
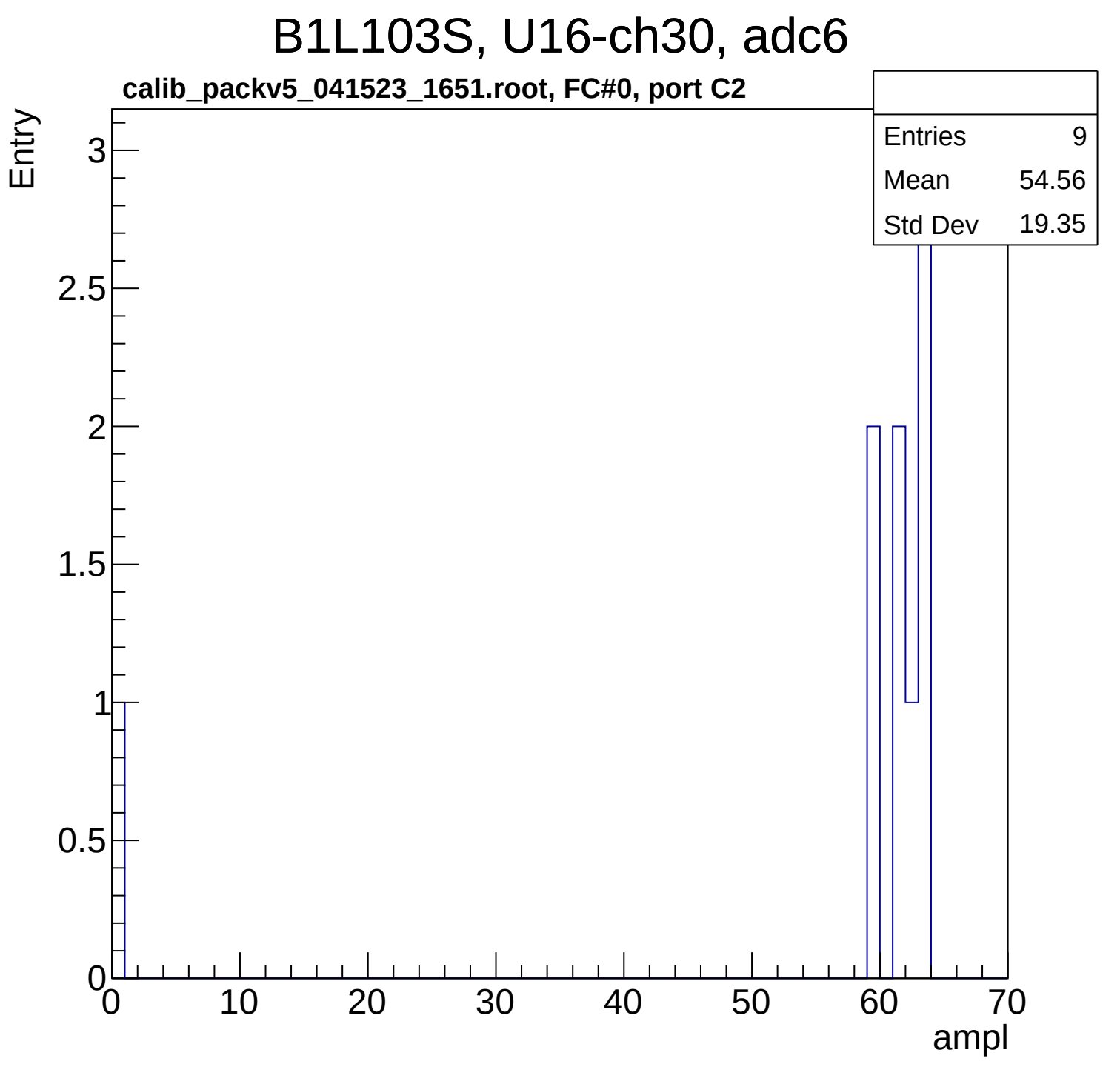
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch30, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 60.36
Std Dev 2.271
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U16-ch30, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 54.56
Std Dev 19.35
Entry
ampl
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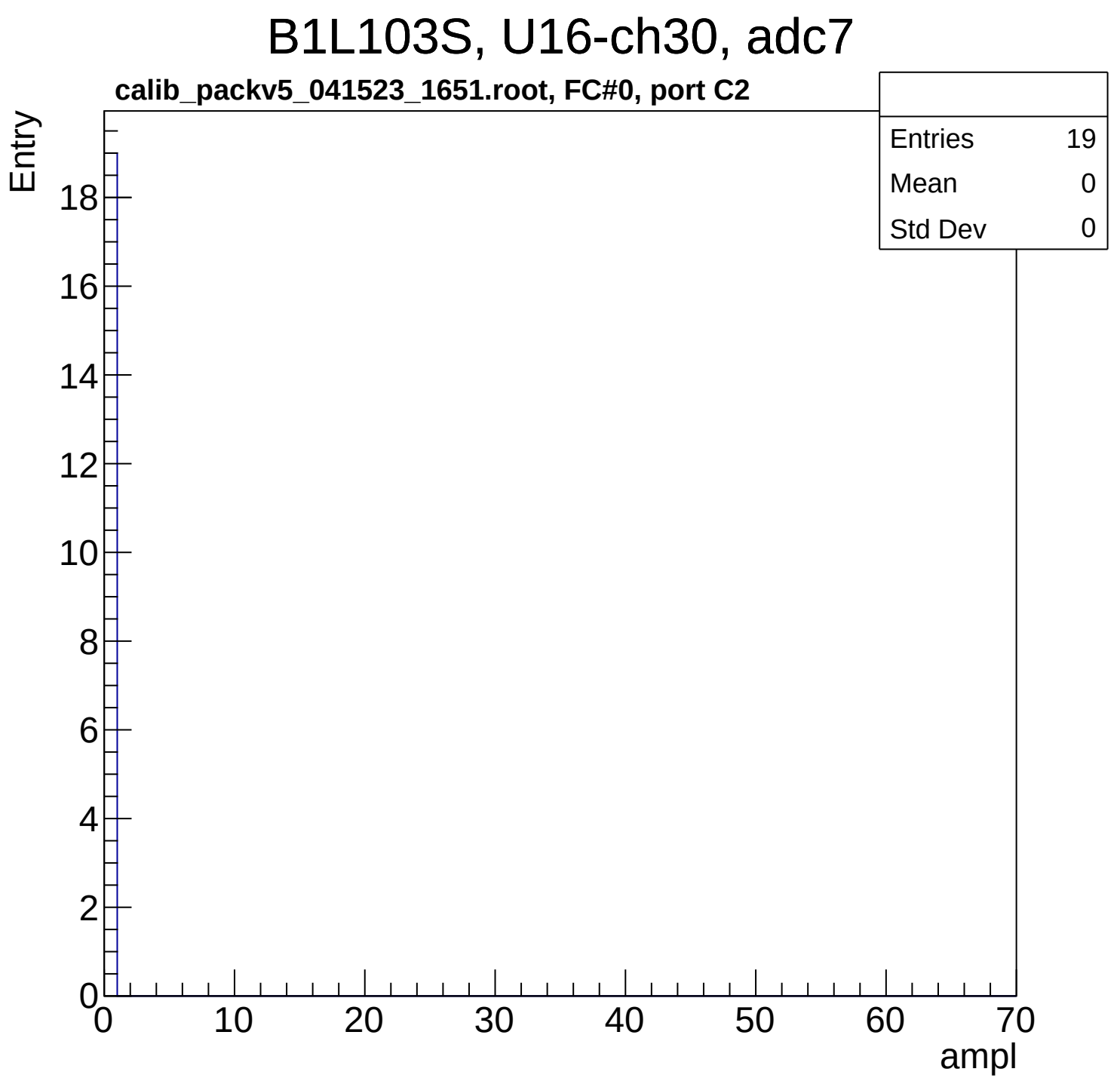
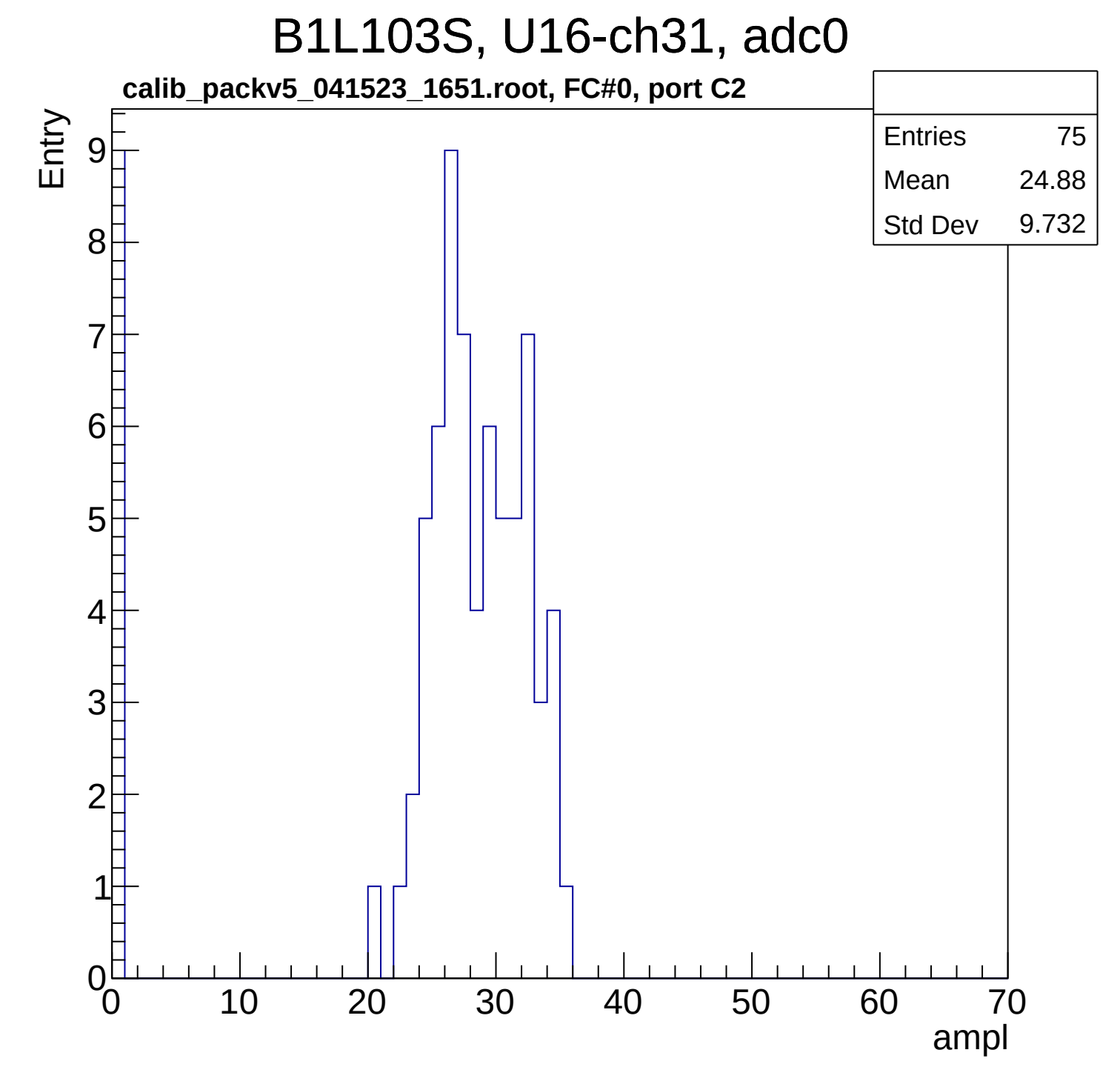
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U16-ch30, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch31, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 24.88
Std Dev 9.732
Entry
ampl
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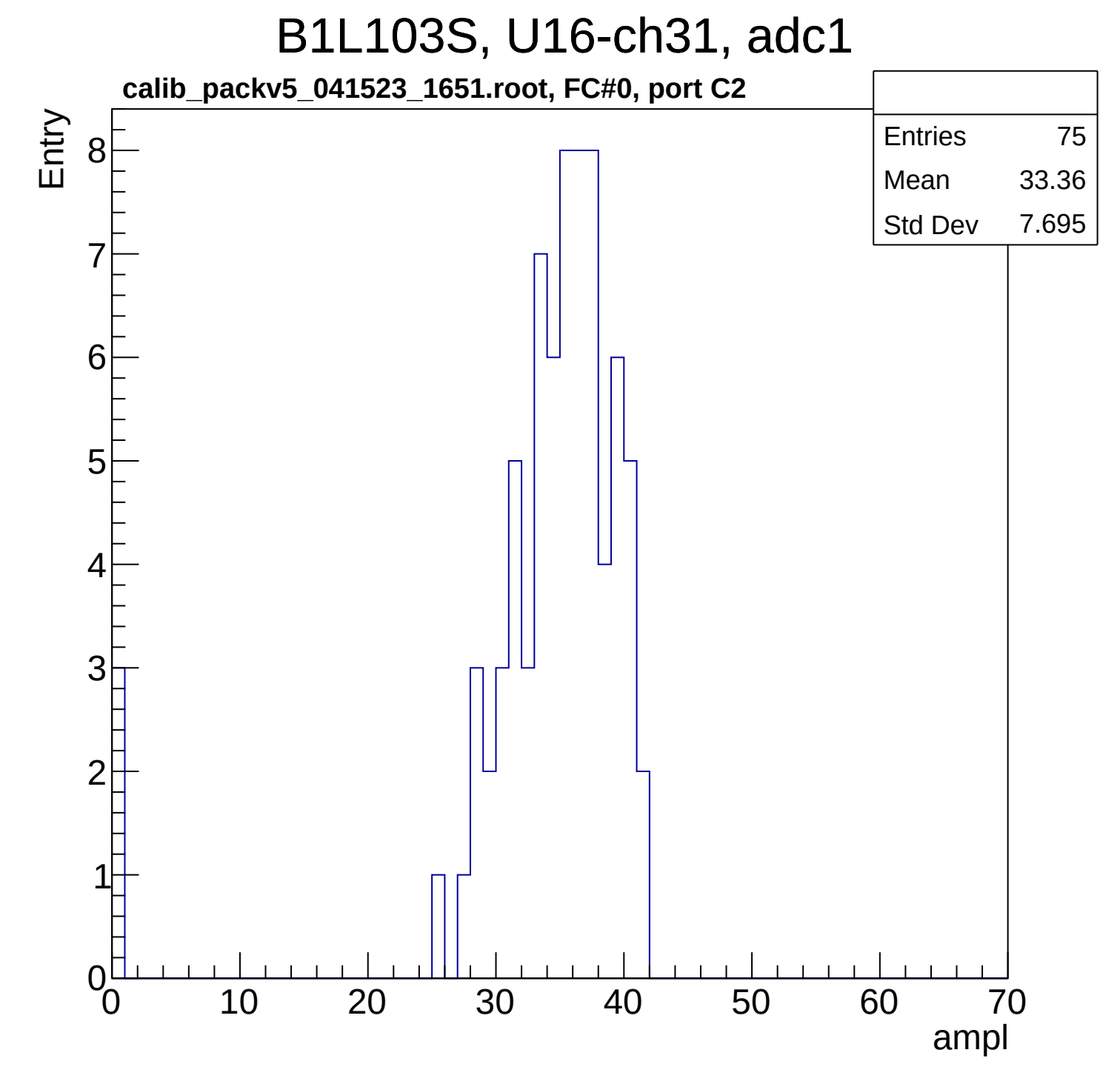
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch31, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 33.36
Std Dev 7.695
Entry
ampl
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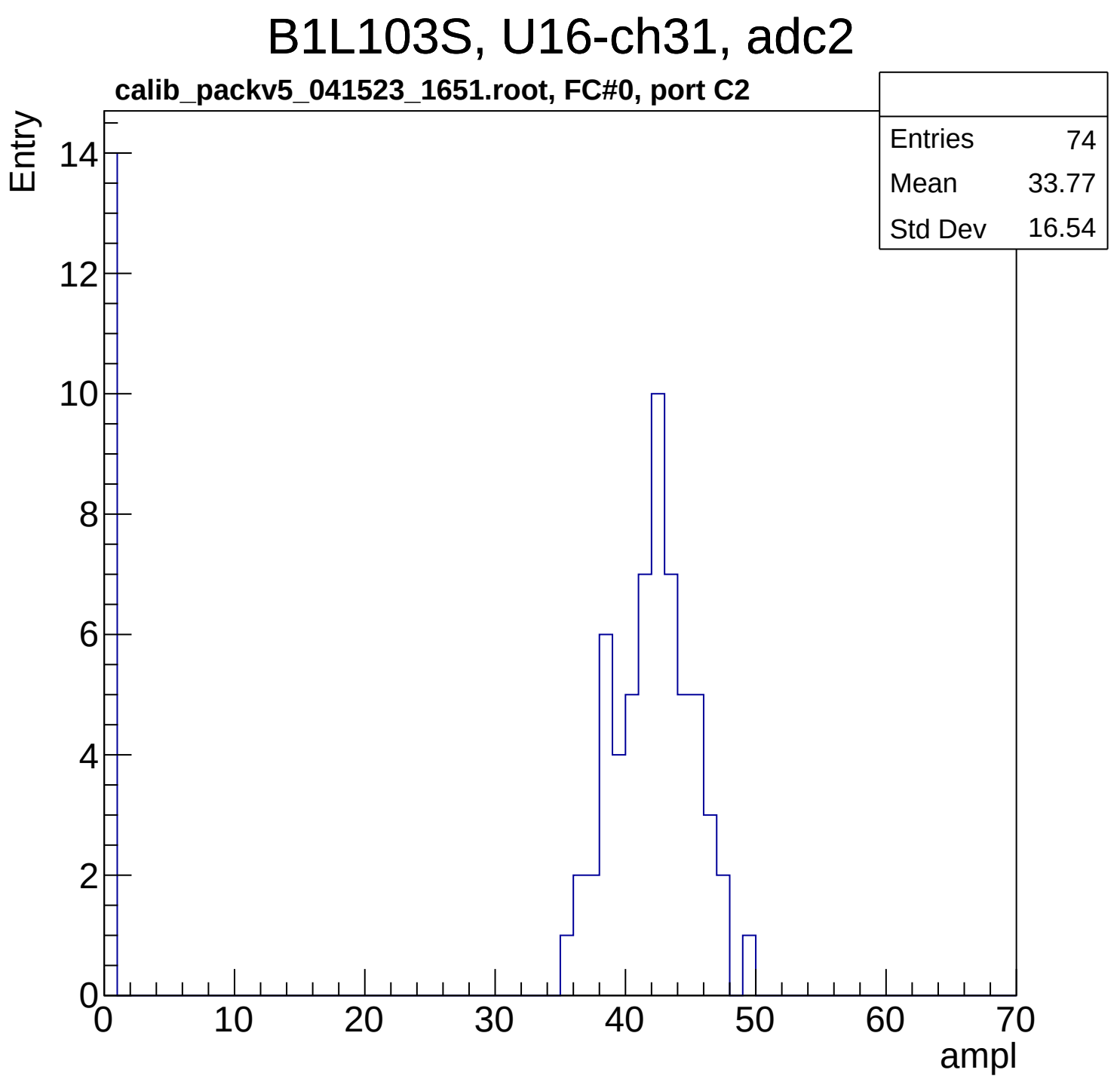
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch31, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 33.77
Std Dev 16.54
Entry
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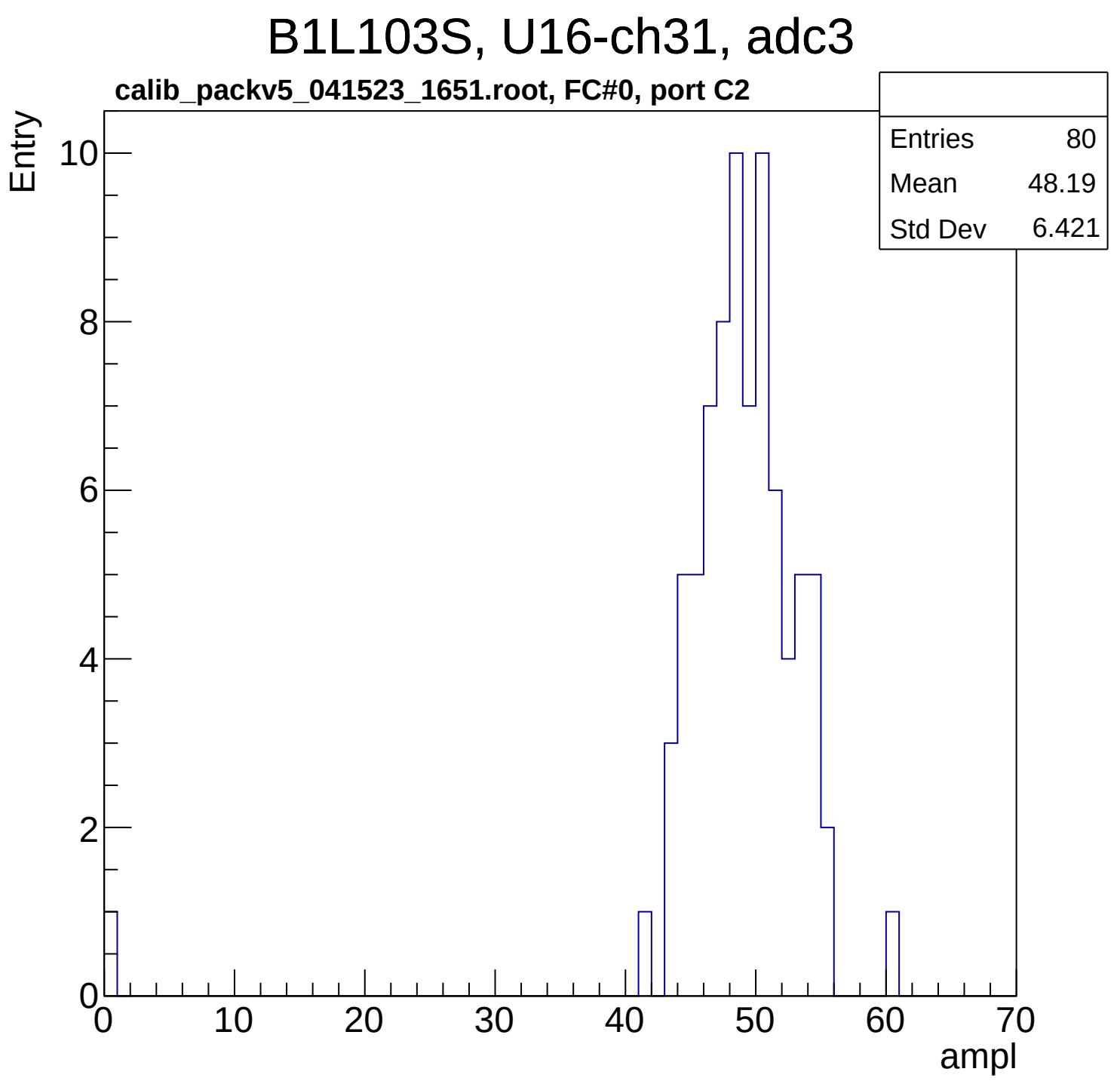
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch31, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 48.19
Std Dev 6.421
Entry
ampl
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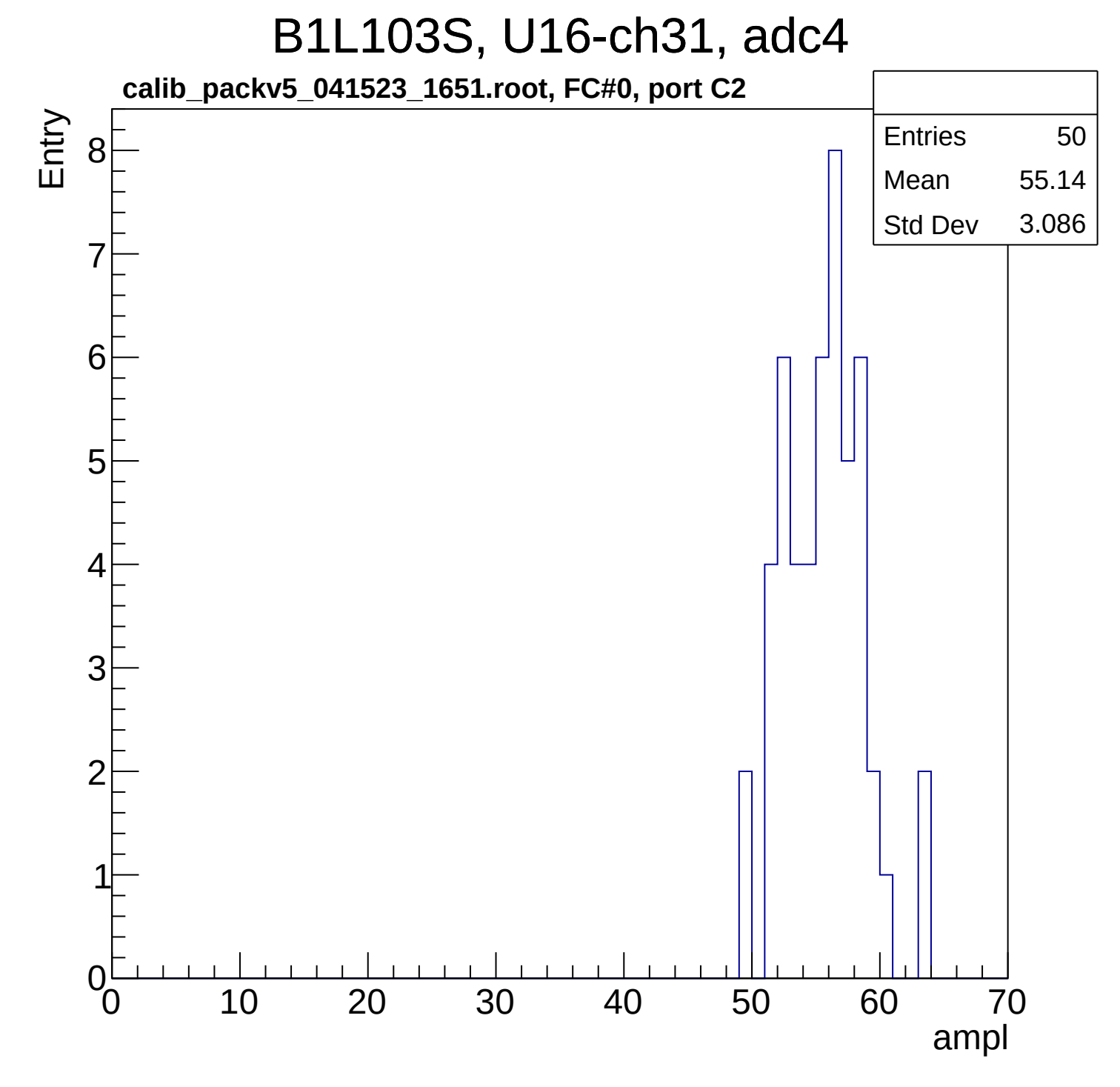
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch31, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 55.14
Std Dev 3.086
Entry
ampl
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1
2
3
4
5
6
7
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0
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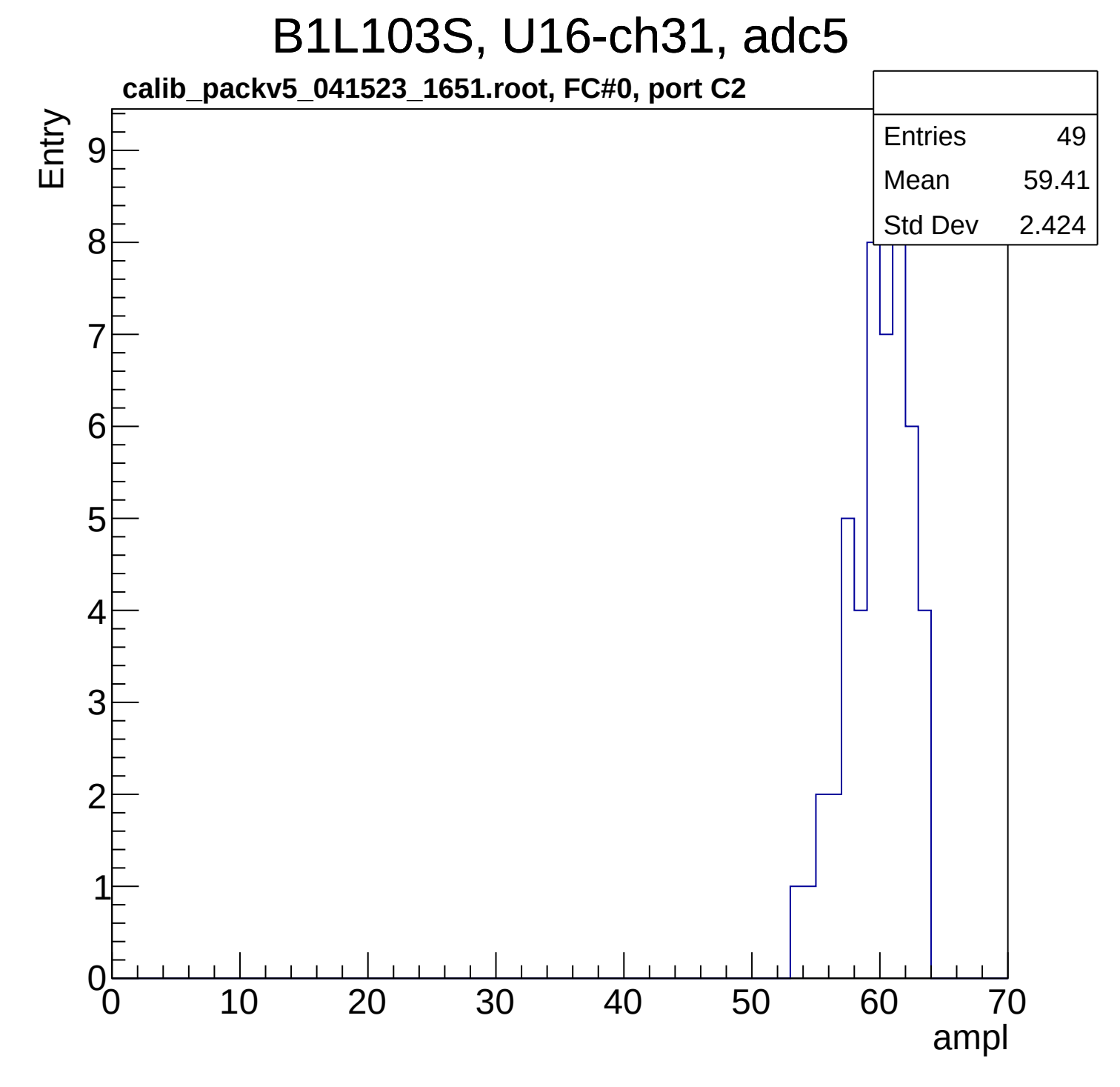
B1L103S, U16-ch31, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 59.41
Std Dev 2.424
Entry
ampl
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3
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6
7
8
9
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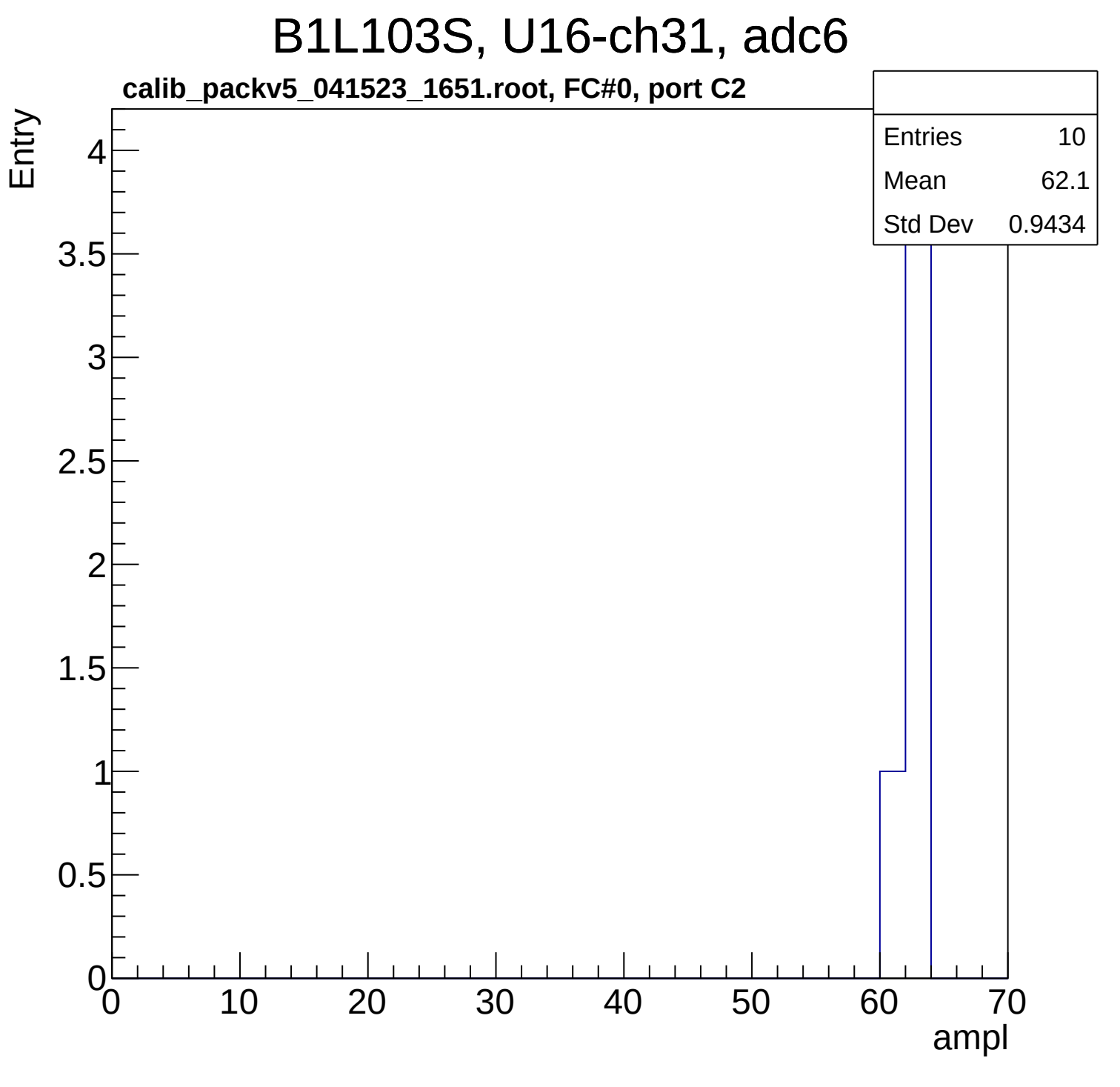
B1L103S, U16-ch31, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 62.1
Std Dev 0.9434
Entry
ampl
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1.5
2
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3
3.5
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0
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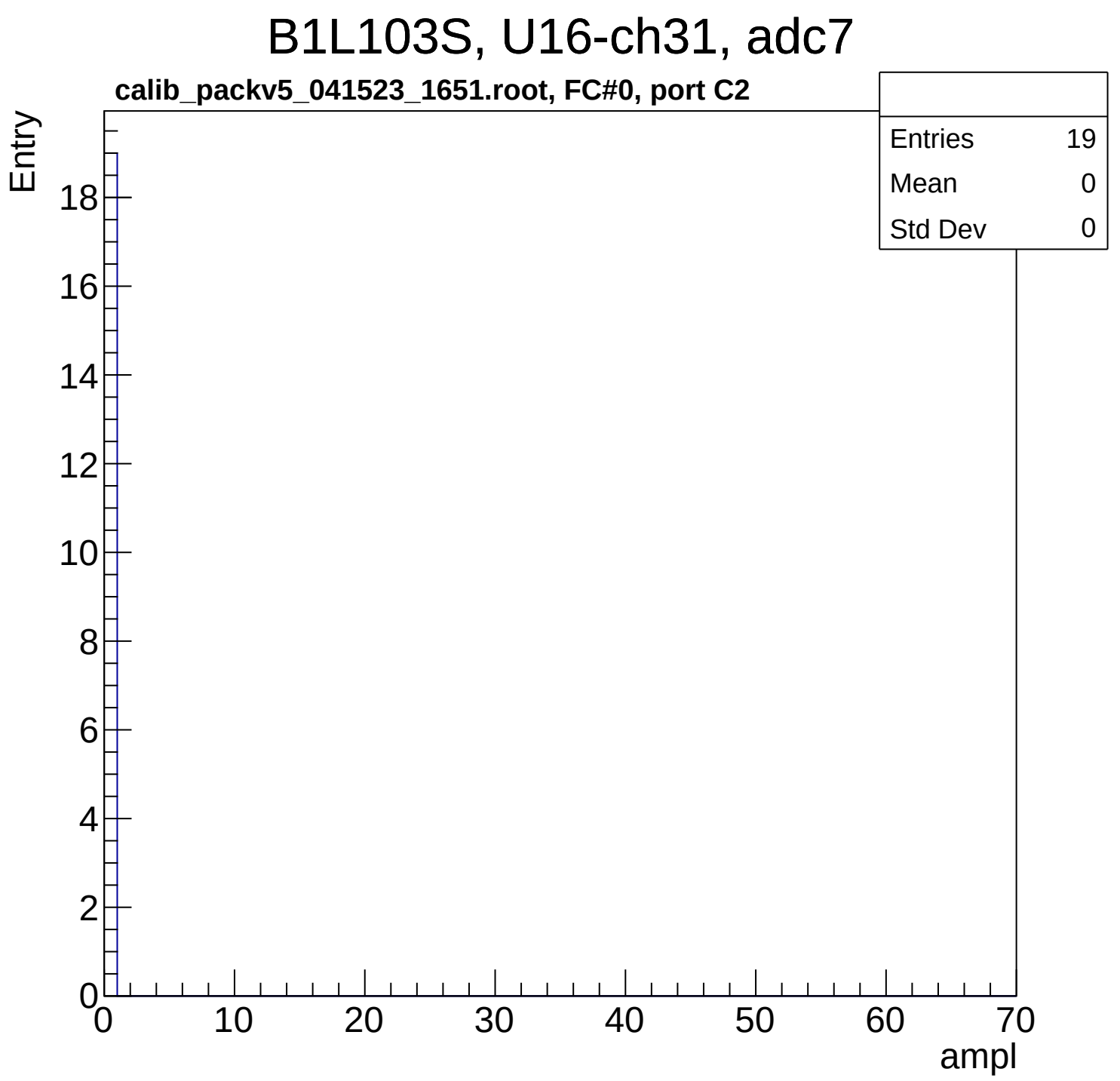
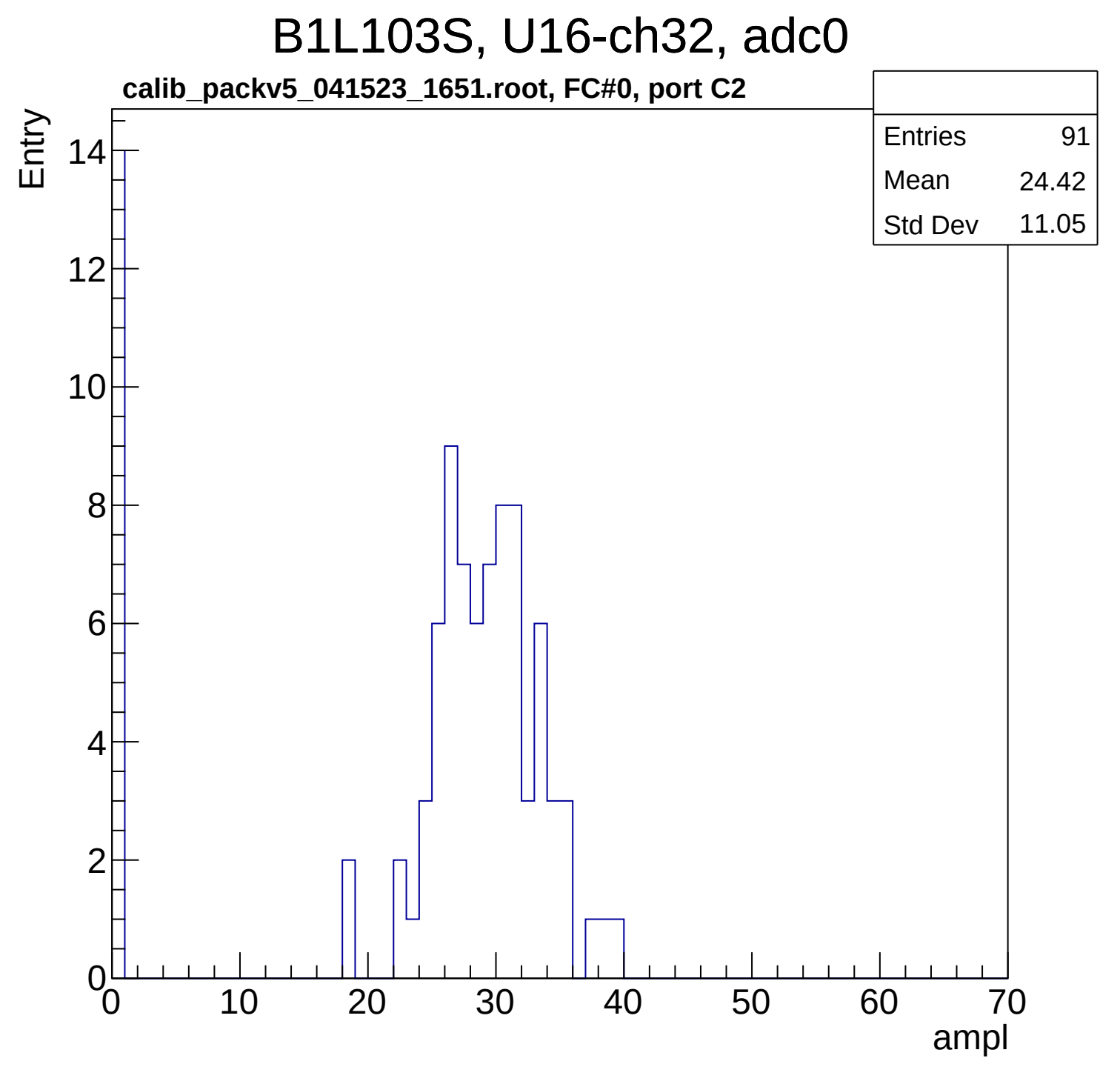
60
70


B1L103S, U16-ch31, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch32, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 24.42
Std Dev 11.05
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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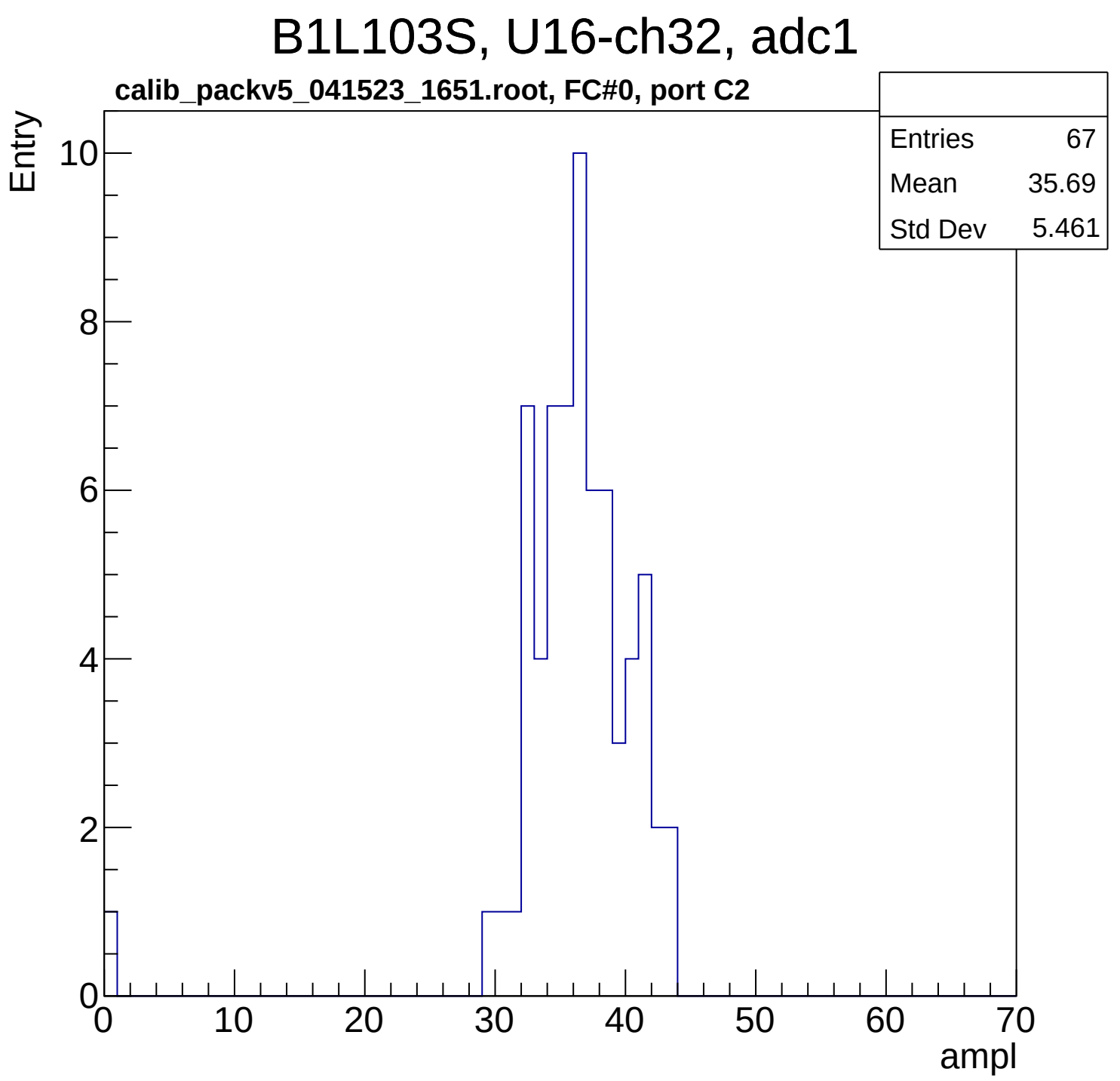
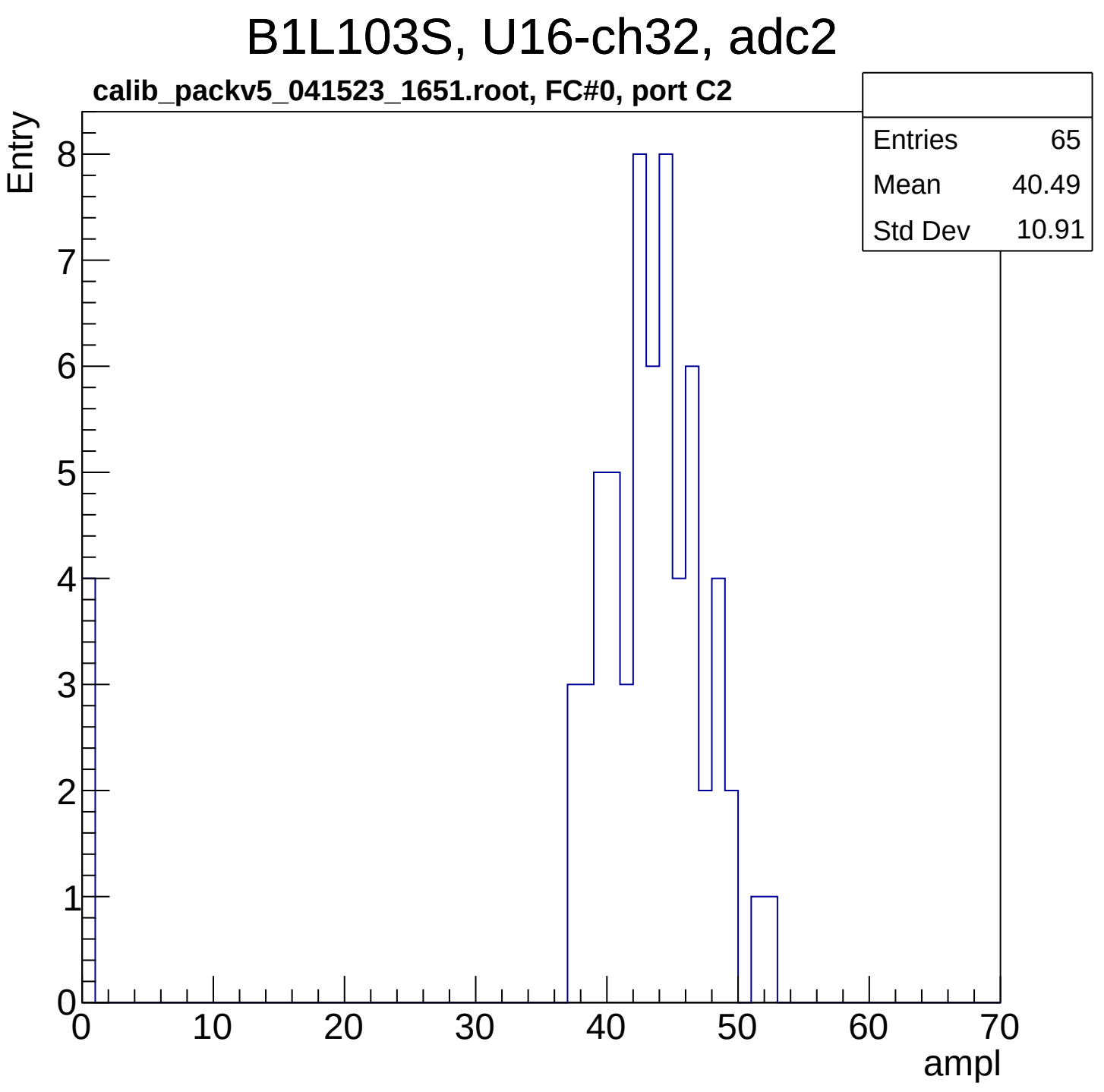

B1L103S, U16-ch32, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 35.69
Std Dev 5.461
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch32, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 40.49
Std Dev 10.91
Entry
ampl
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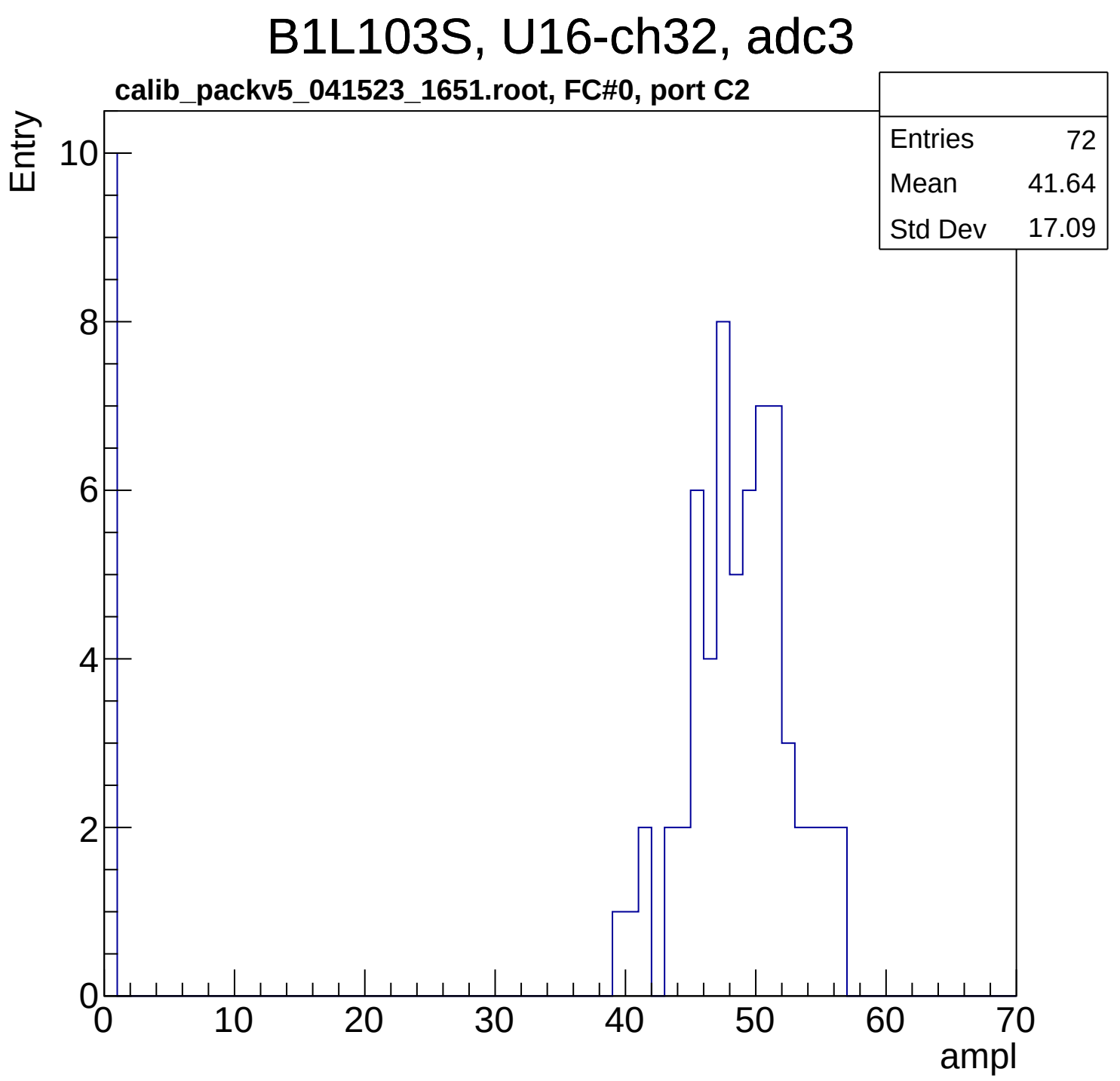
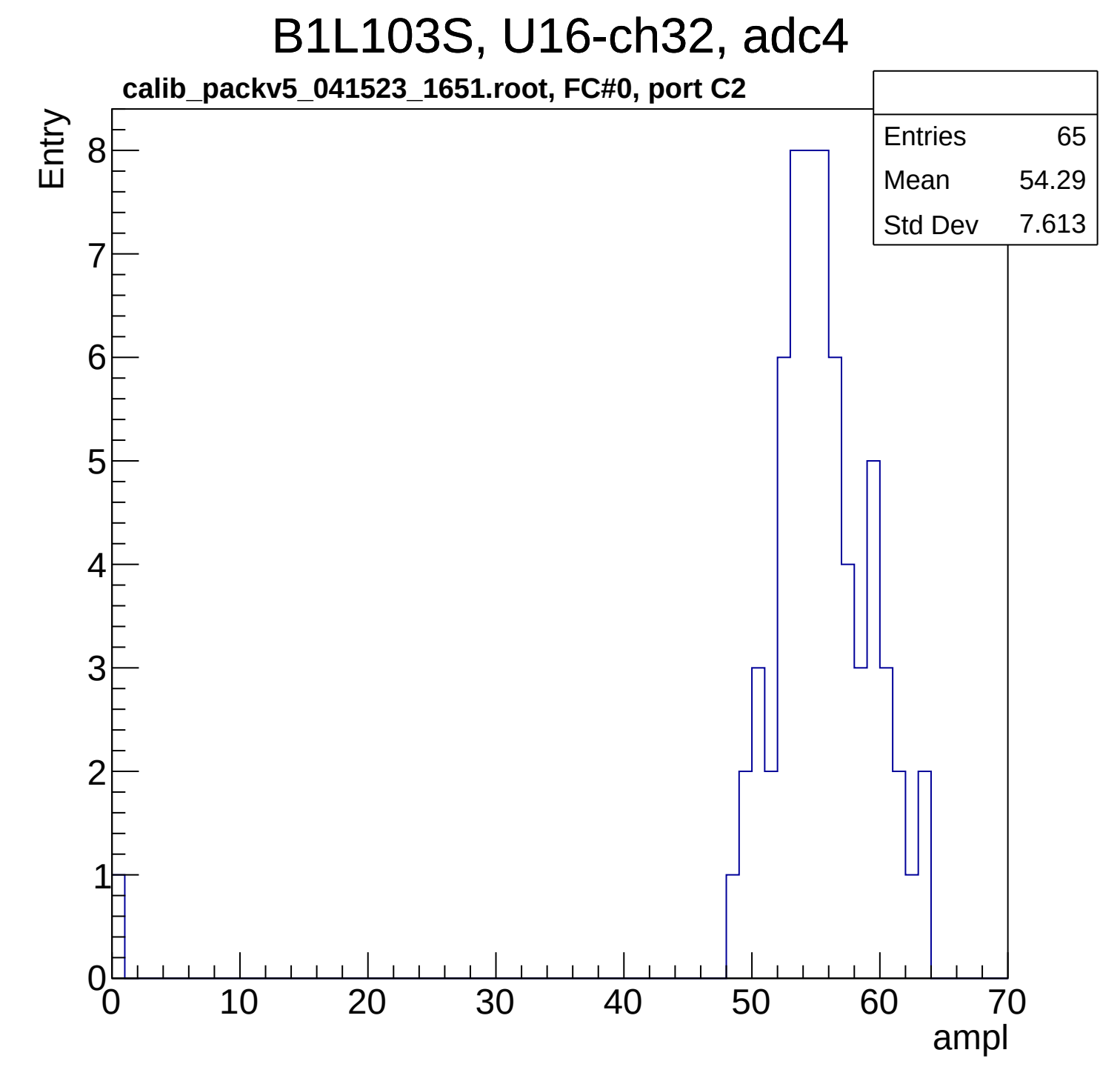
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch32, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 41.64
Std Dev 17.09
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch32, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 54.29
Std Dev 7.613
Entry
ampl
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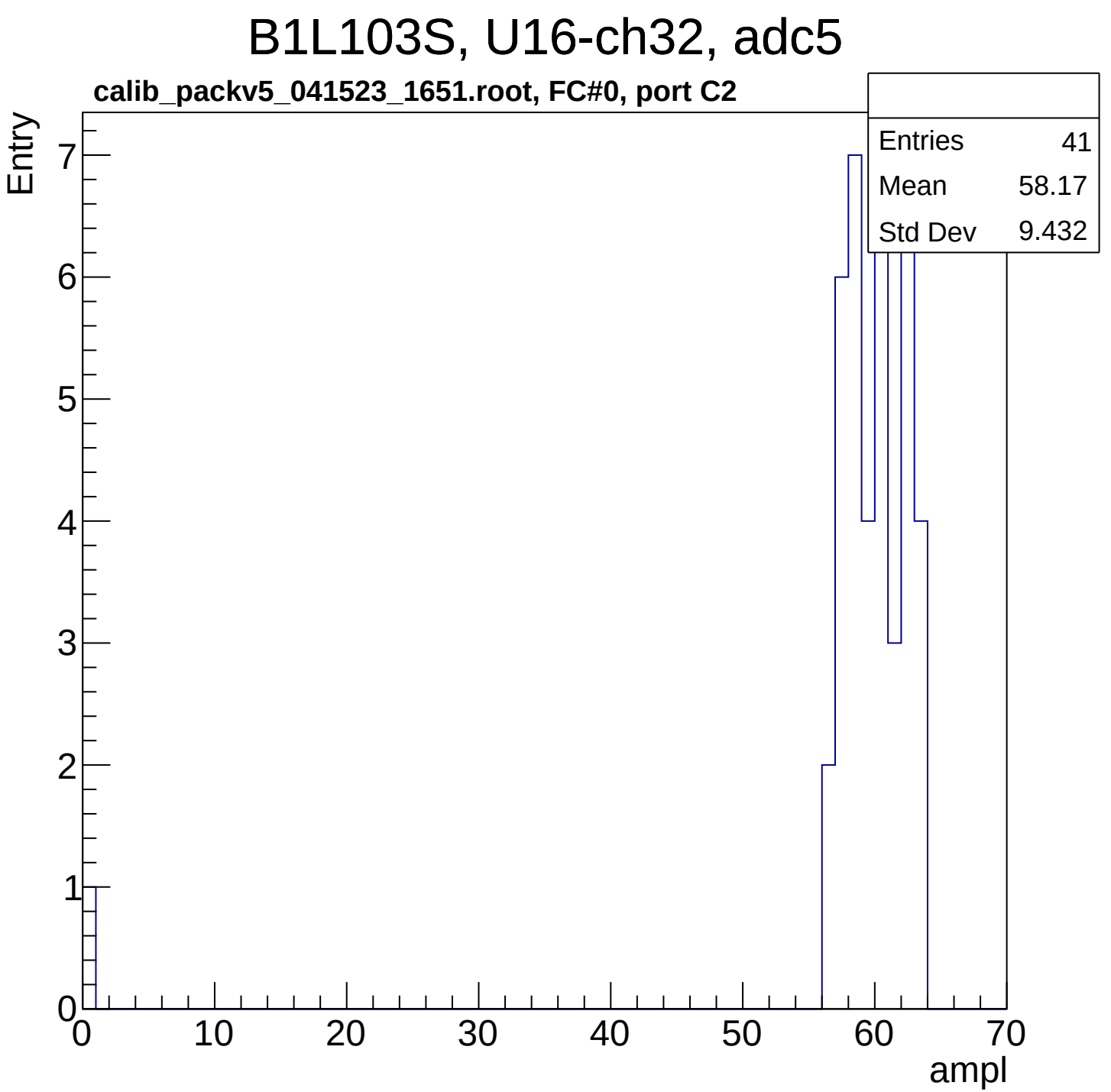
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch32, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 58.17
Std Dev 9.432
Entry
ampl
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2
3
4
5
6
7
0
10
20
30
40
50
60
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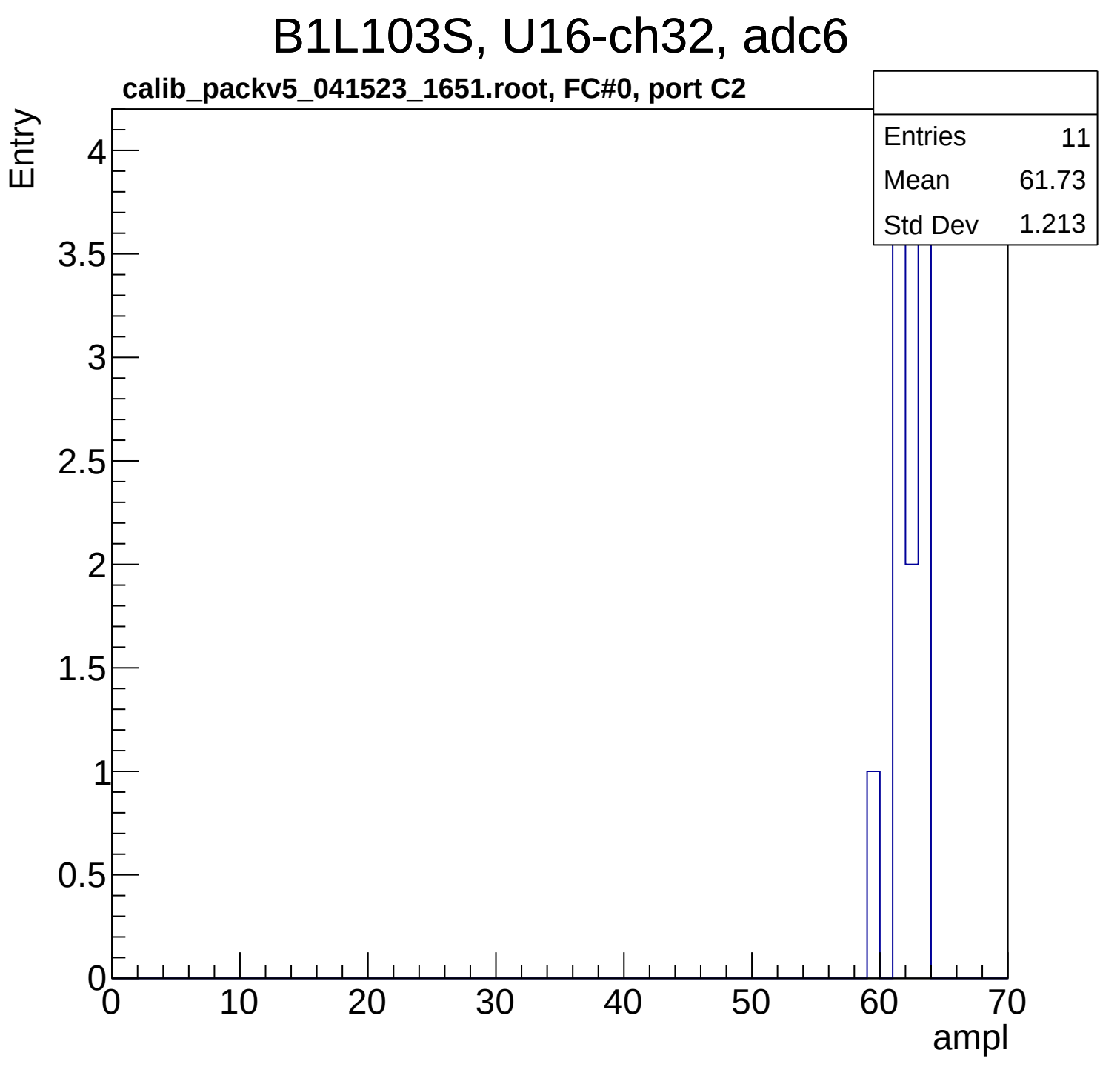
B1L103S, U16-ch32, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.73
Std Dev 1.213
Entry
ampl
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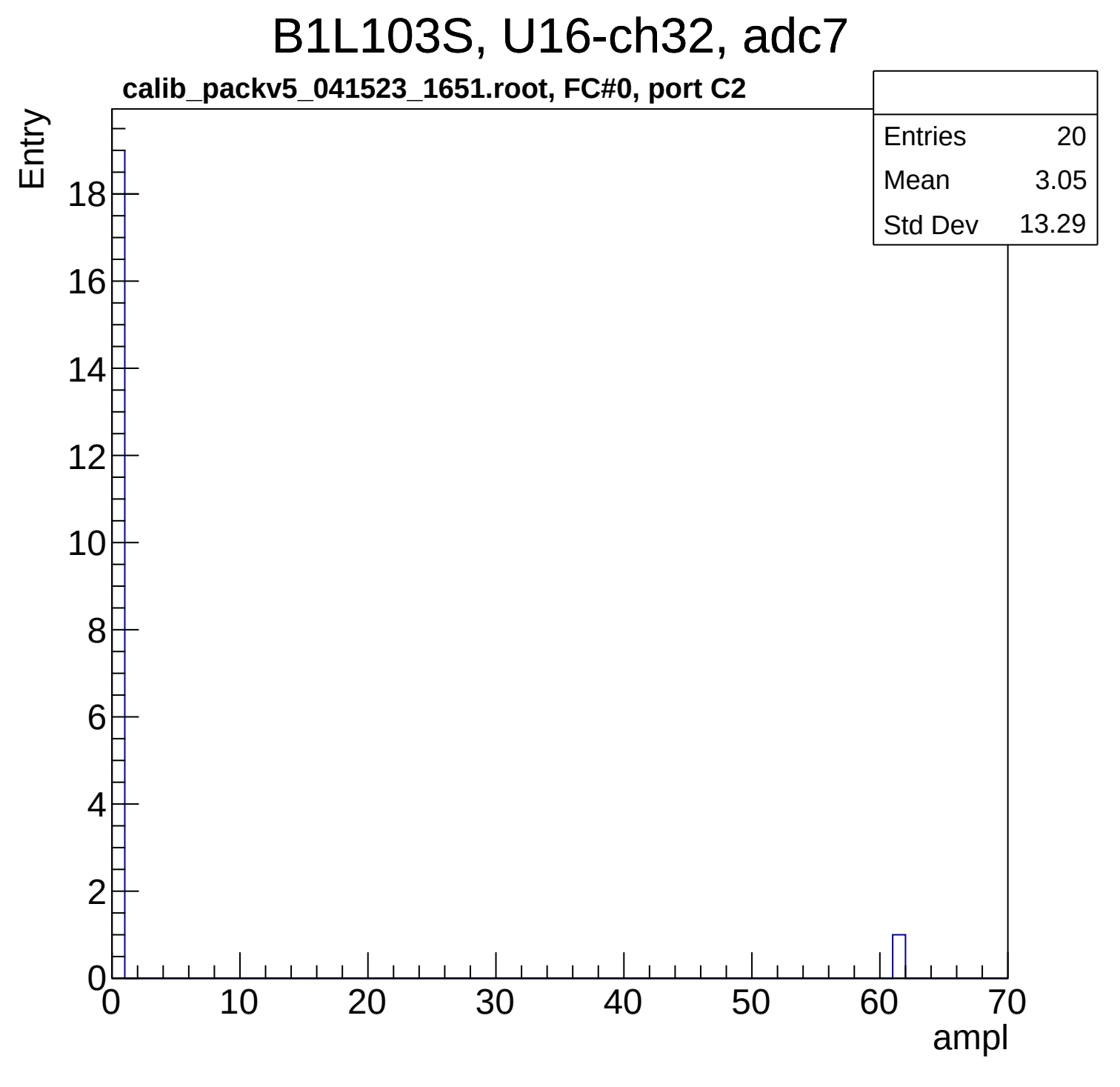
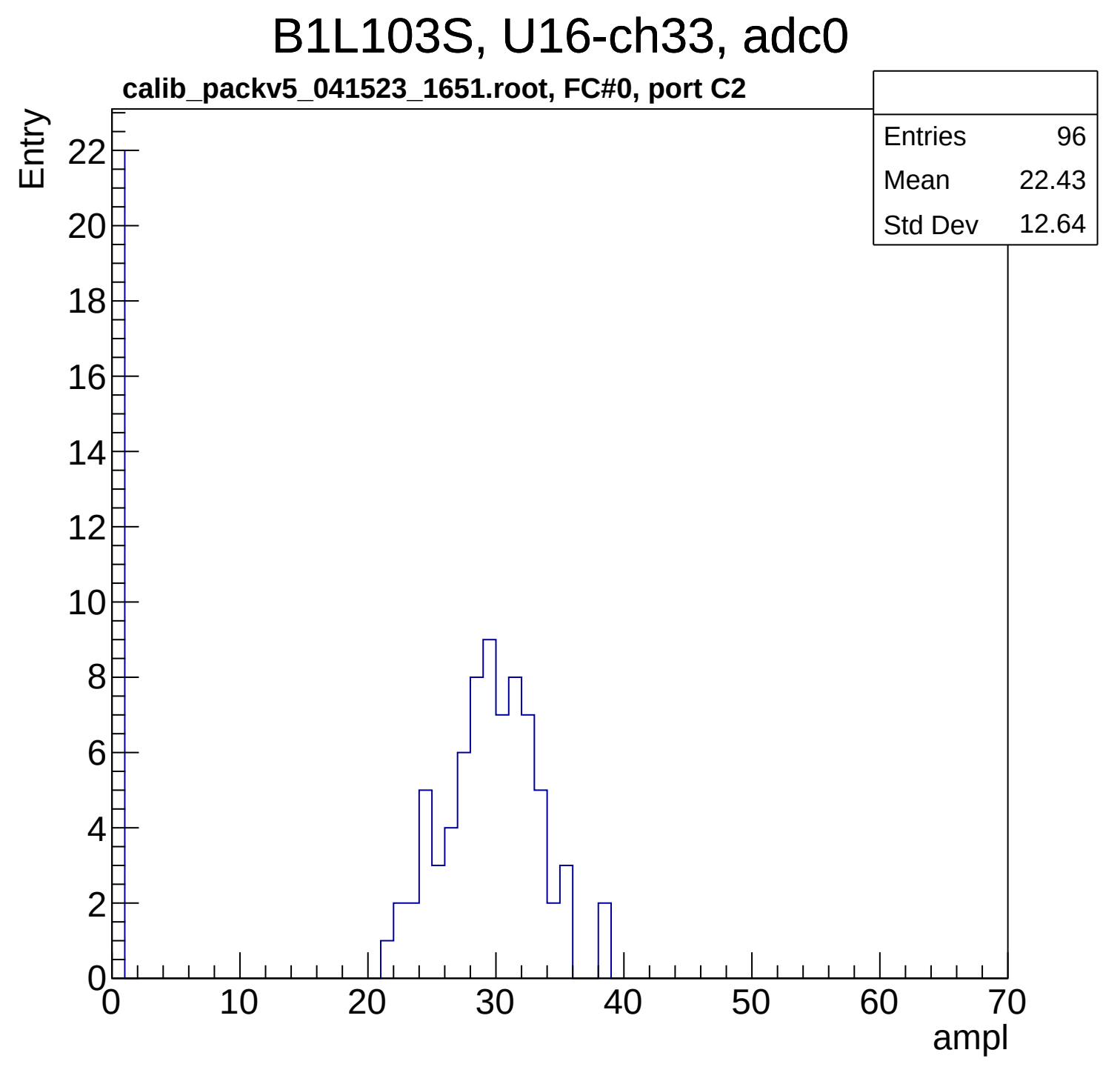
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U16-ch32, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch33, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 22.43
Std Dev 12.64
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
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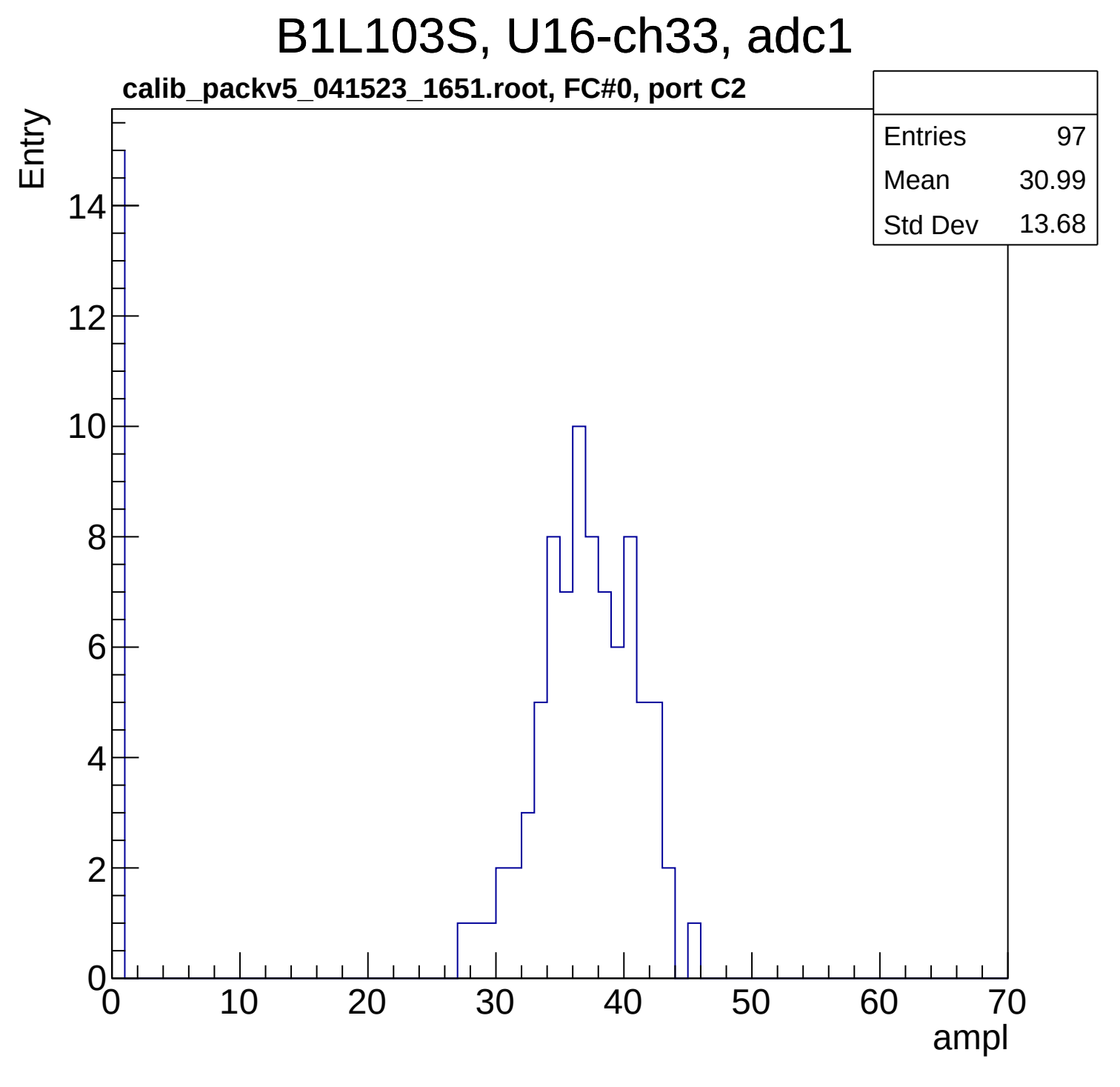
B1L103S, U16-ch33, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 30.99
Std Dev 13.68
Entry
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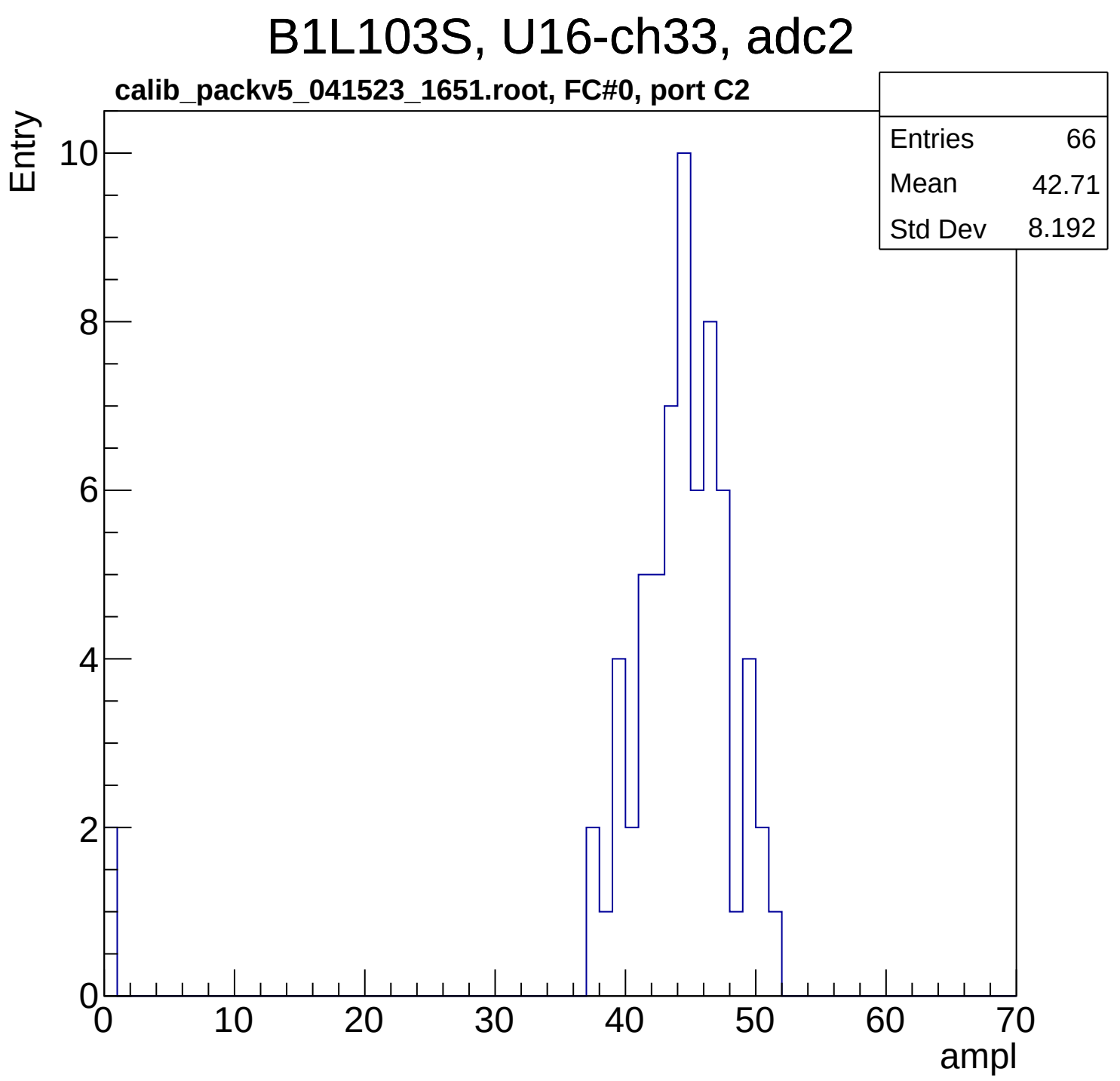
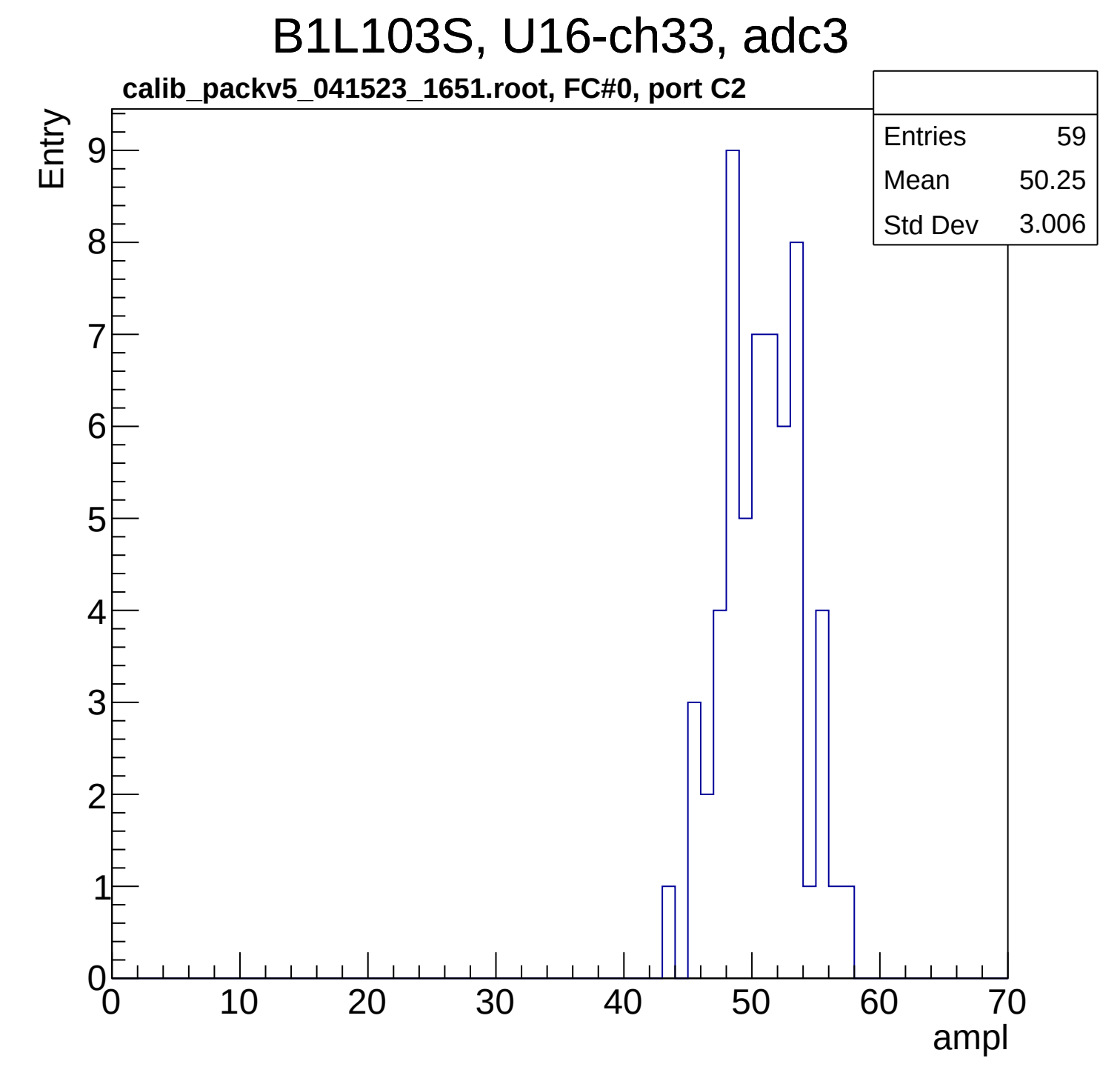
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch33, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 42.71
Std Dev 8.192
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch33, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 50.25
Std Dev 3.006
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
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60
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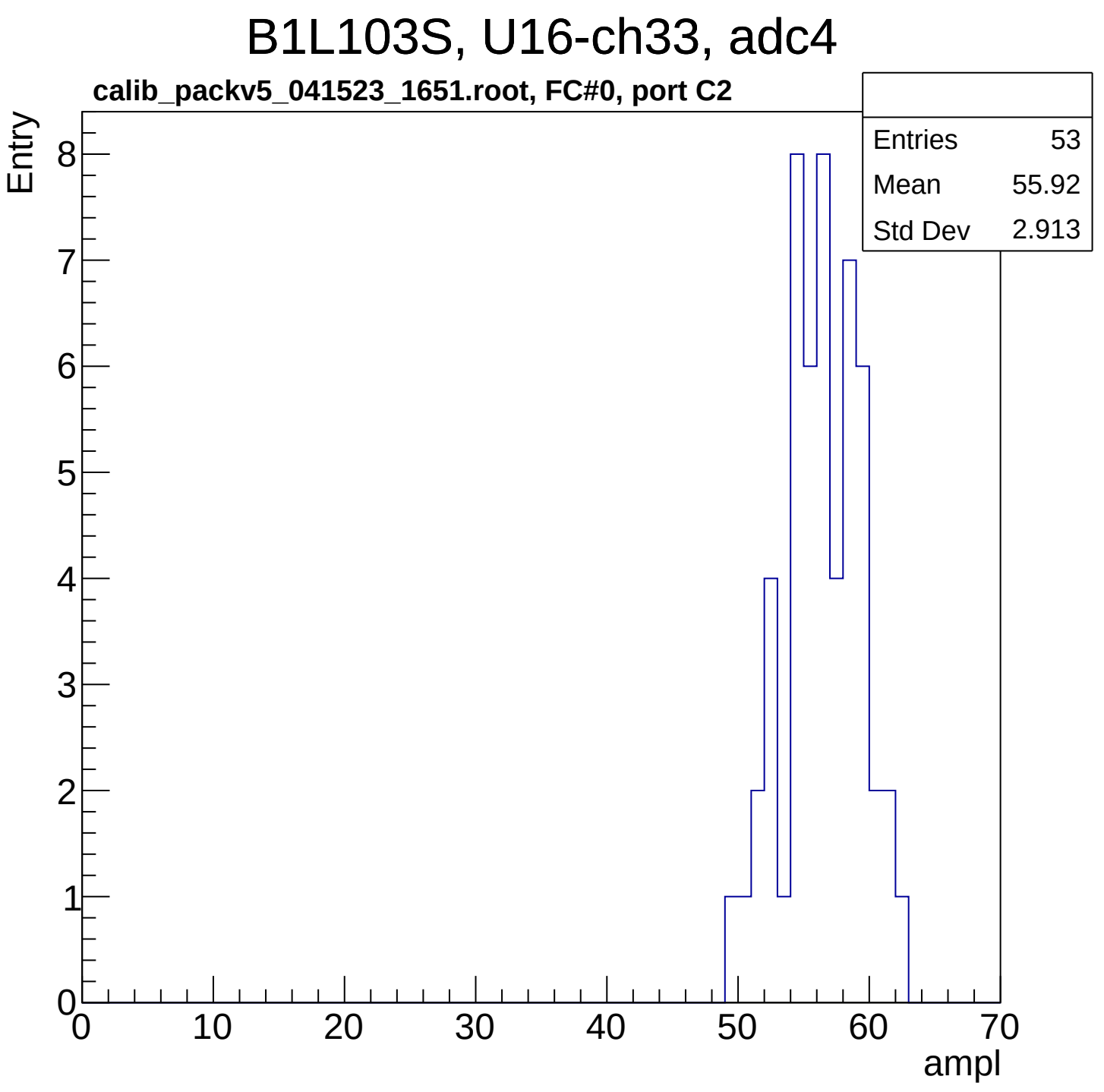
B1L103S, U16-ch33, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 55.92
Std Dev 2.913
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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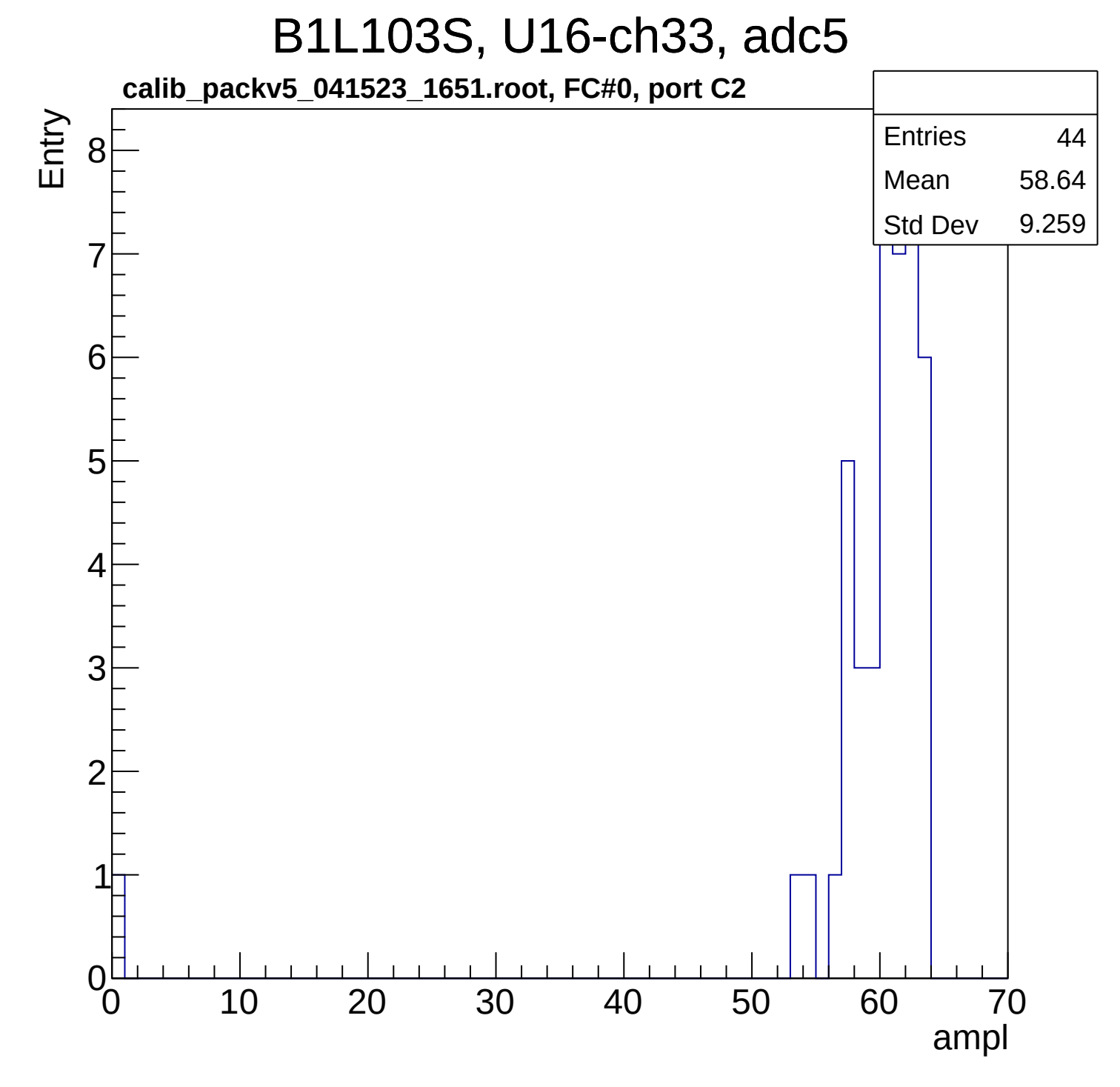
B1L103S, U16-ch33, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 58.64
Std Dev 9.259
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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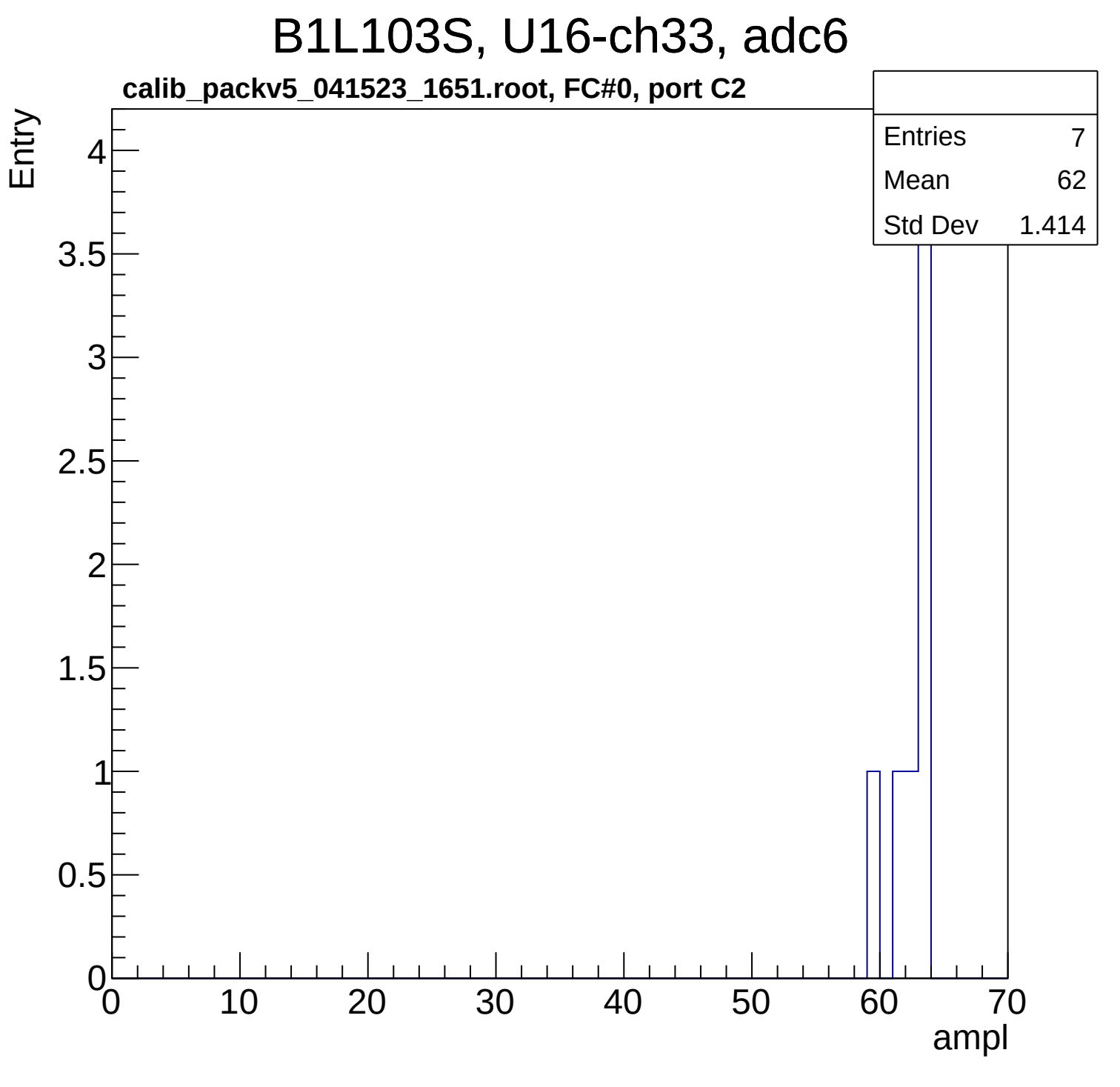
B1L103S, U16-ch33, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62
Std Dev 1.414
Entry
ampl
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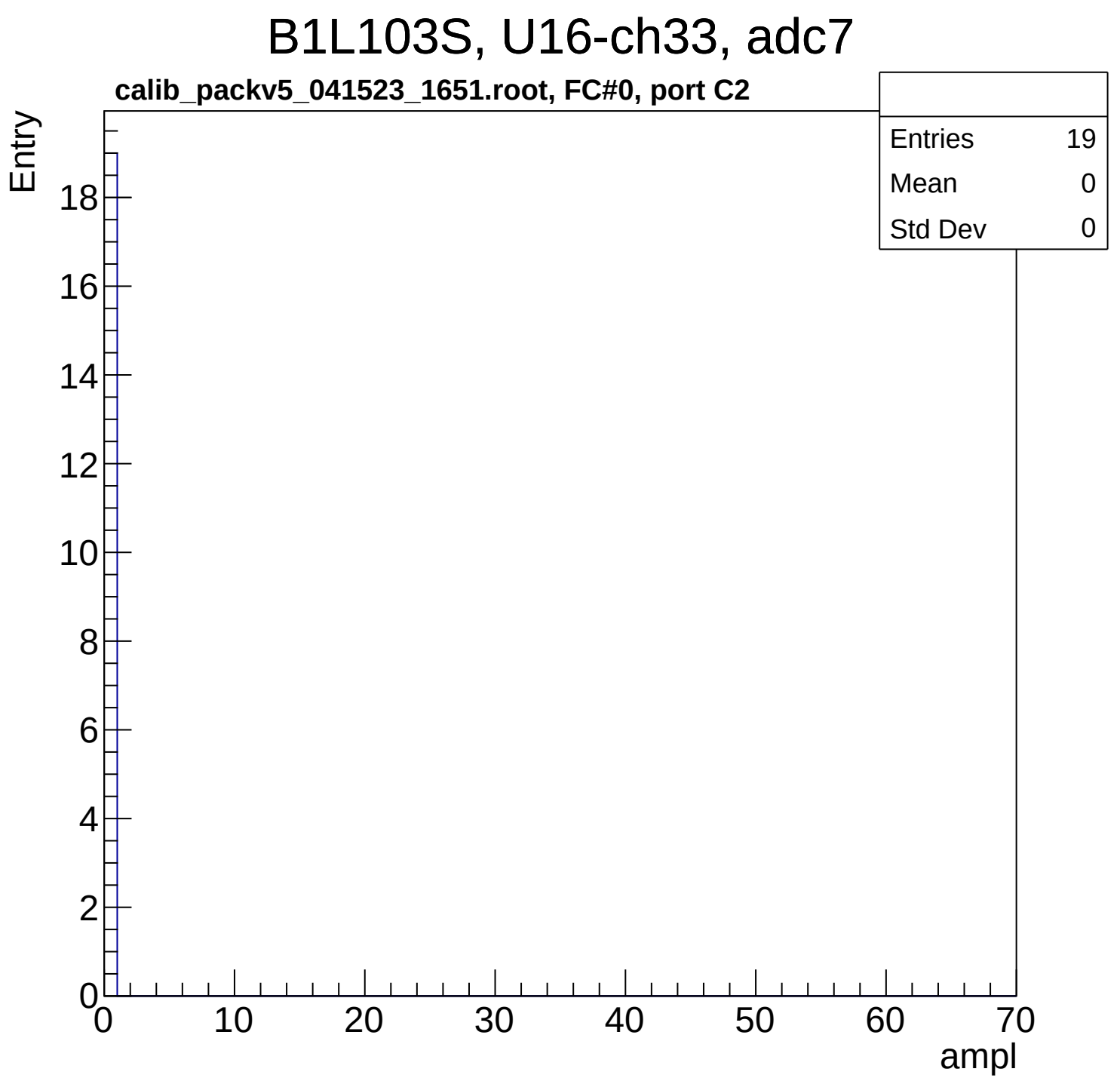
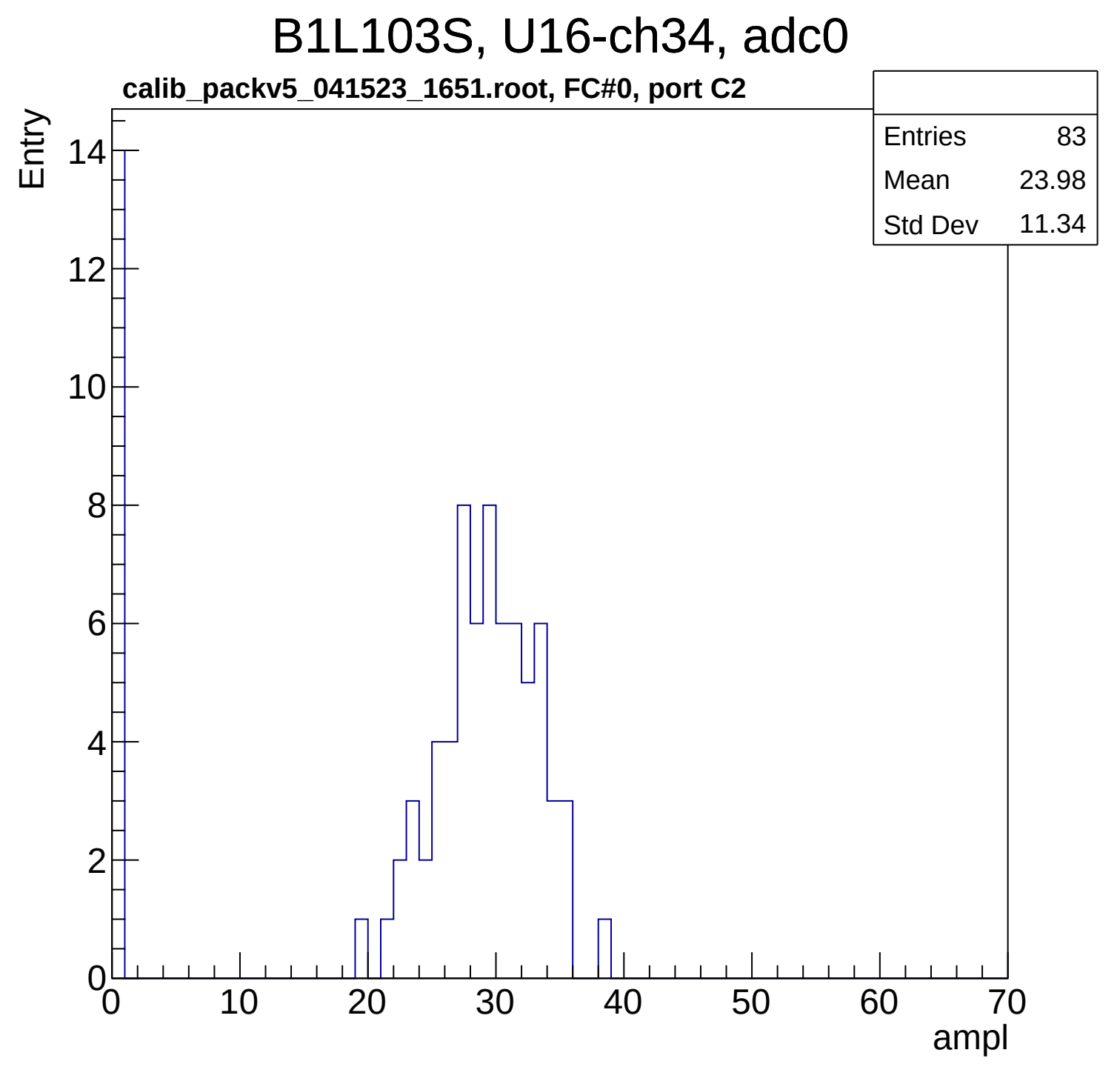
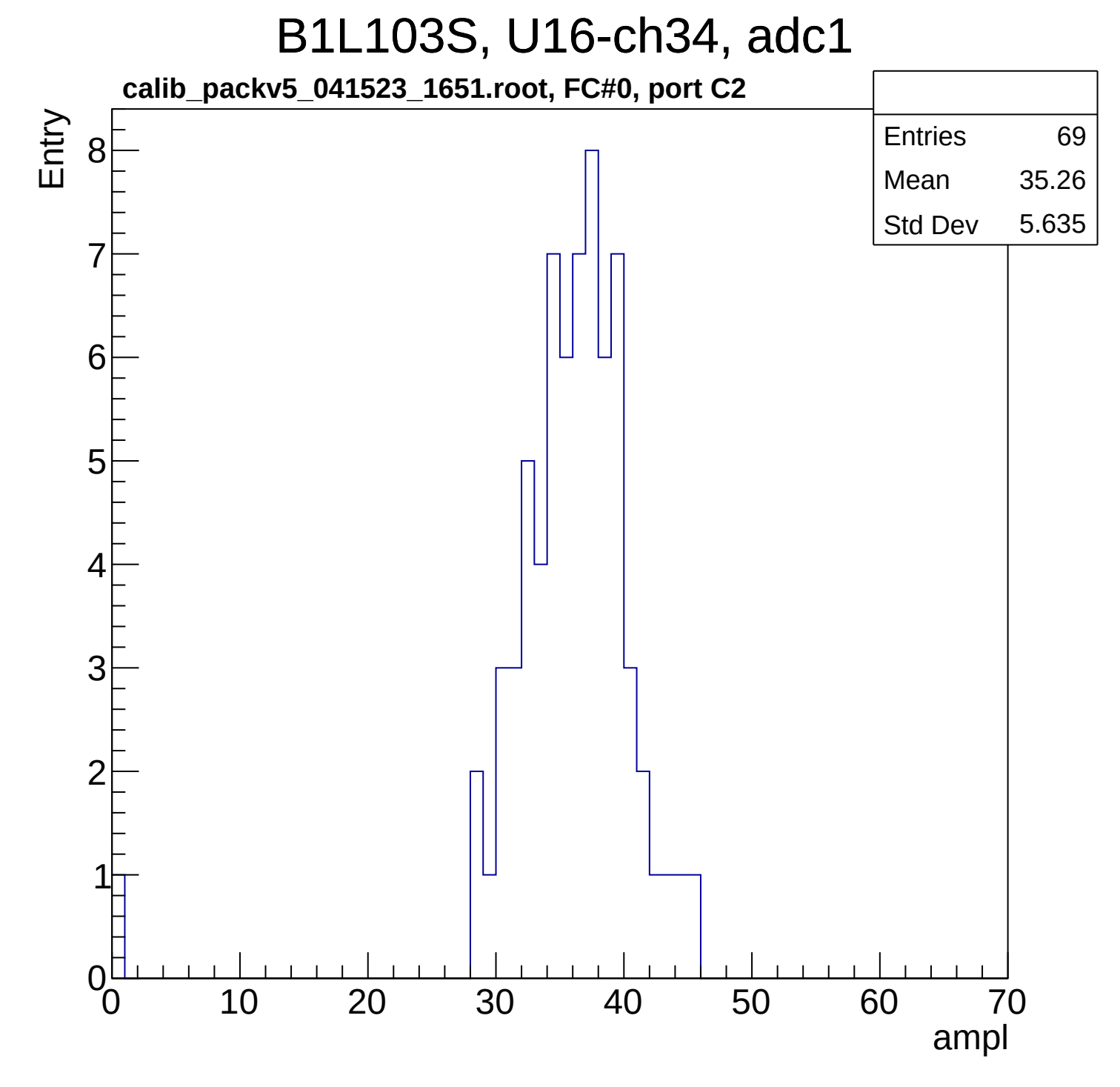
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U16-ch33, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch34, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 23.98
Std Dev 11.34
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U16-ch34, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 35.26
Std Dev 5.635
Entry
ampl
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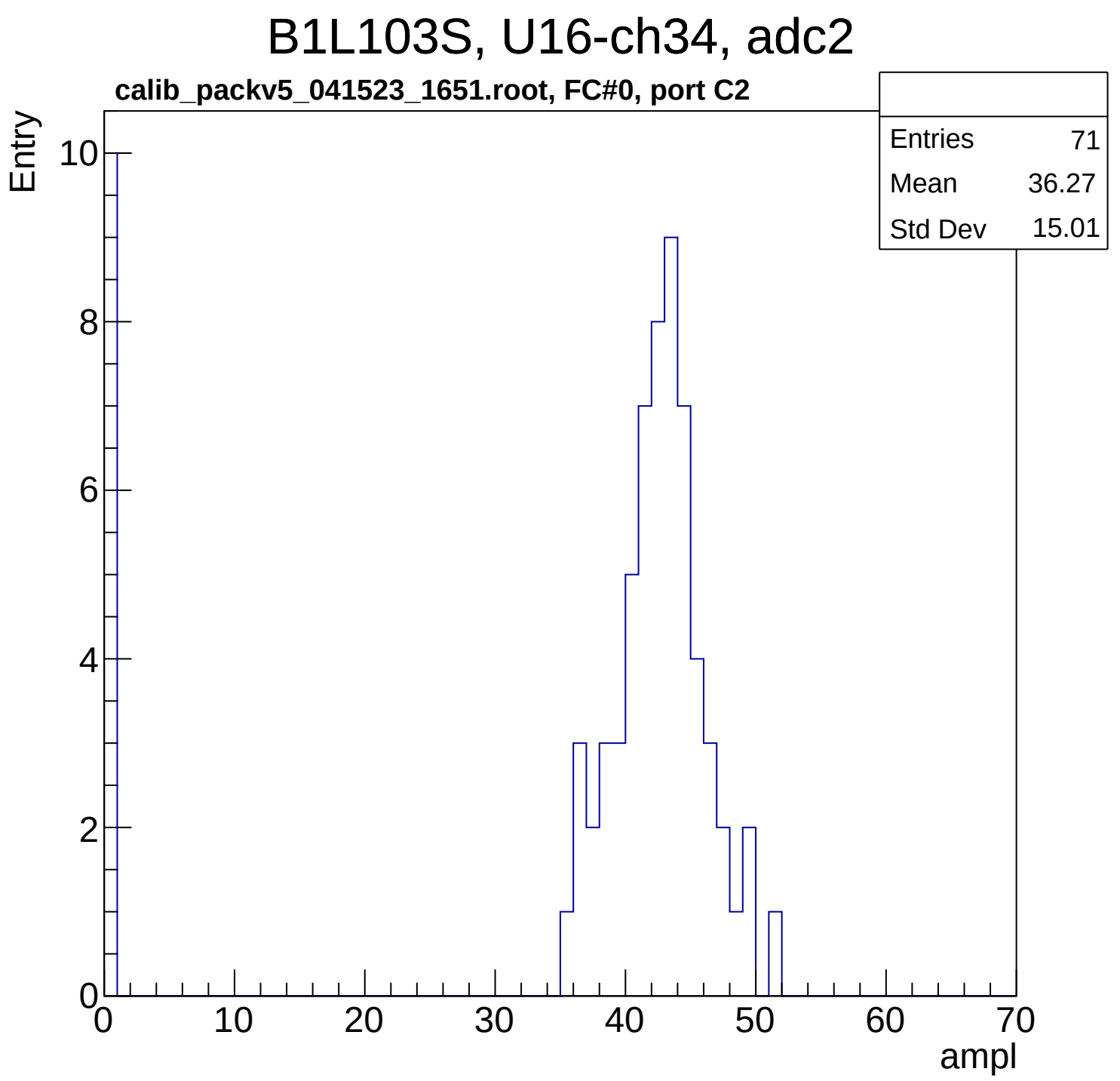
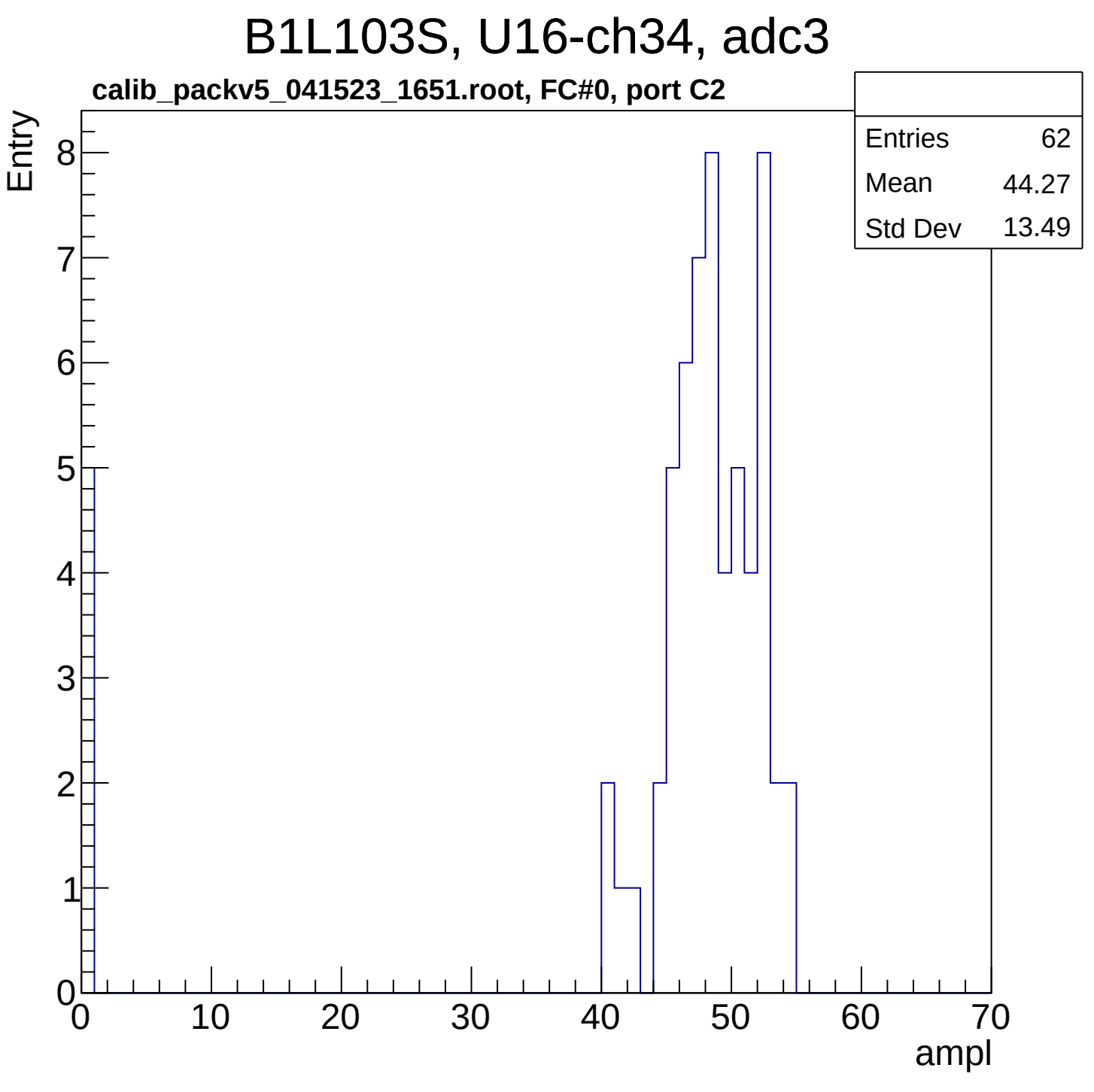
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch34, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 36.27
Std Dev 15.01
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch34, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 44.27
Std Dev 13.49
Entry
ampl
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2
3
4
5
6
7
8
0
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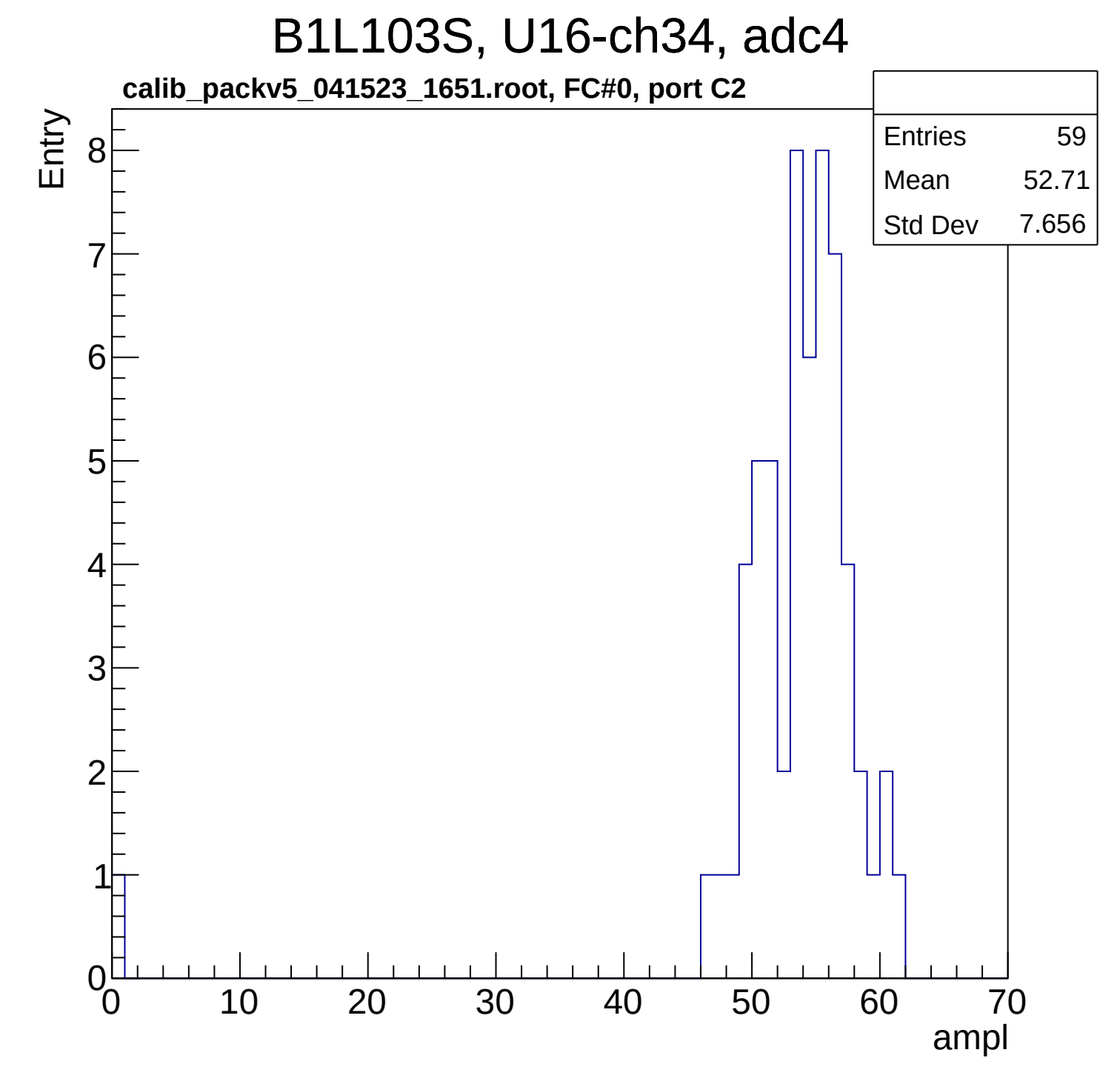
20
30
40
50
60
70


B1L103S, U16-ch34, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 52.71
Std Dev 7.656
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
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60
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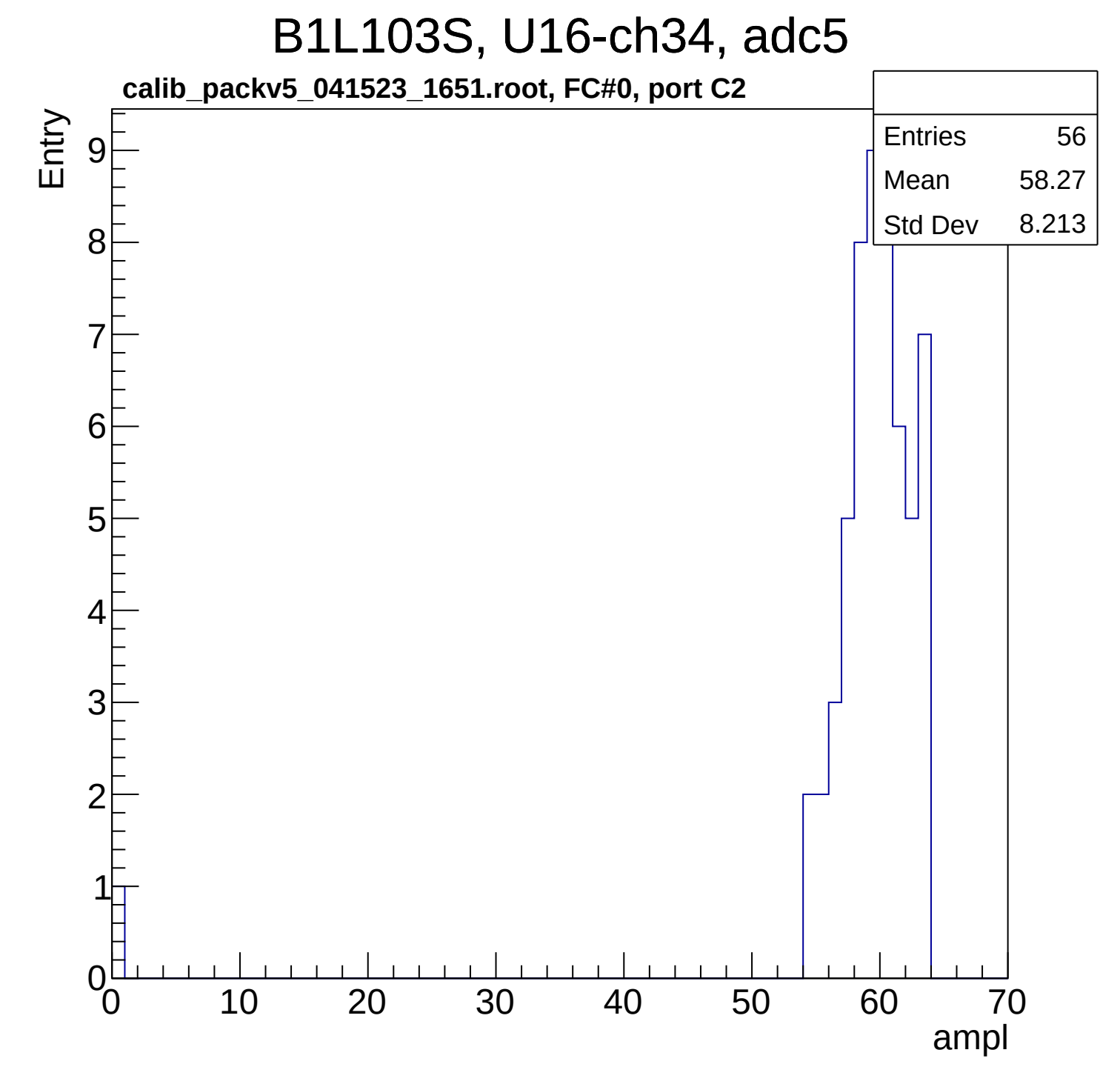
B1L103S, U16-ch34, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.27
Std Dev 8.213
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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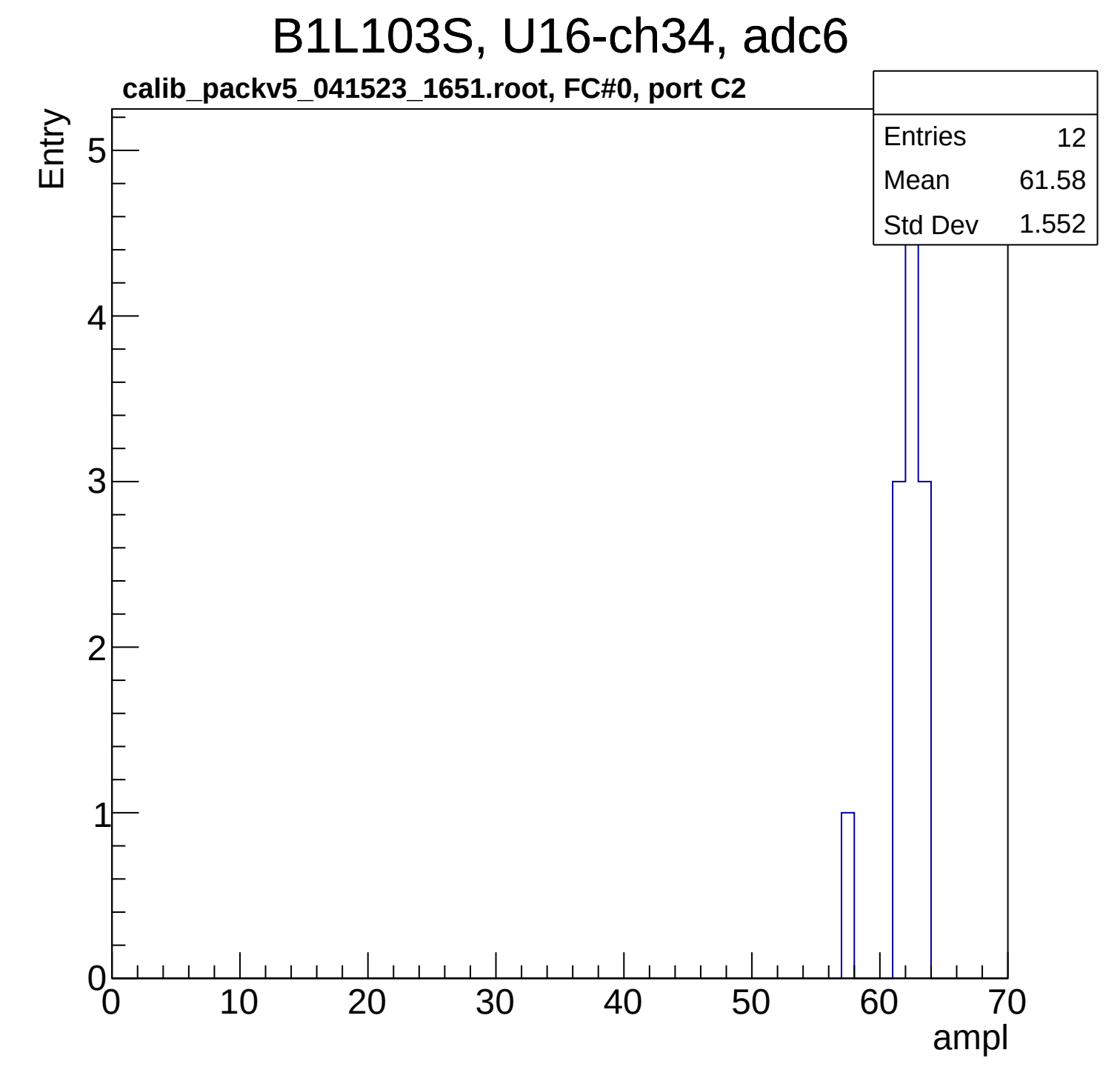
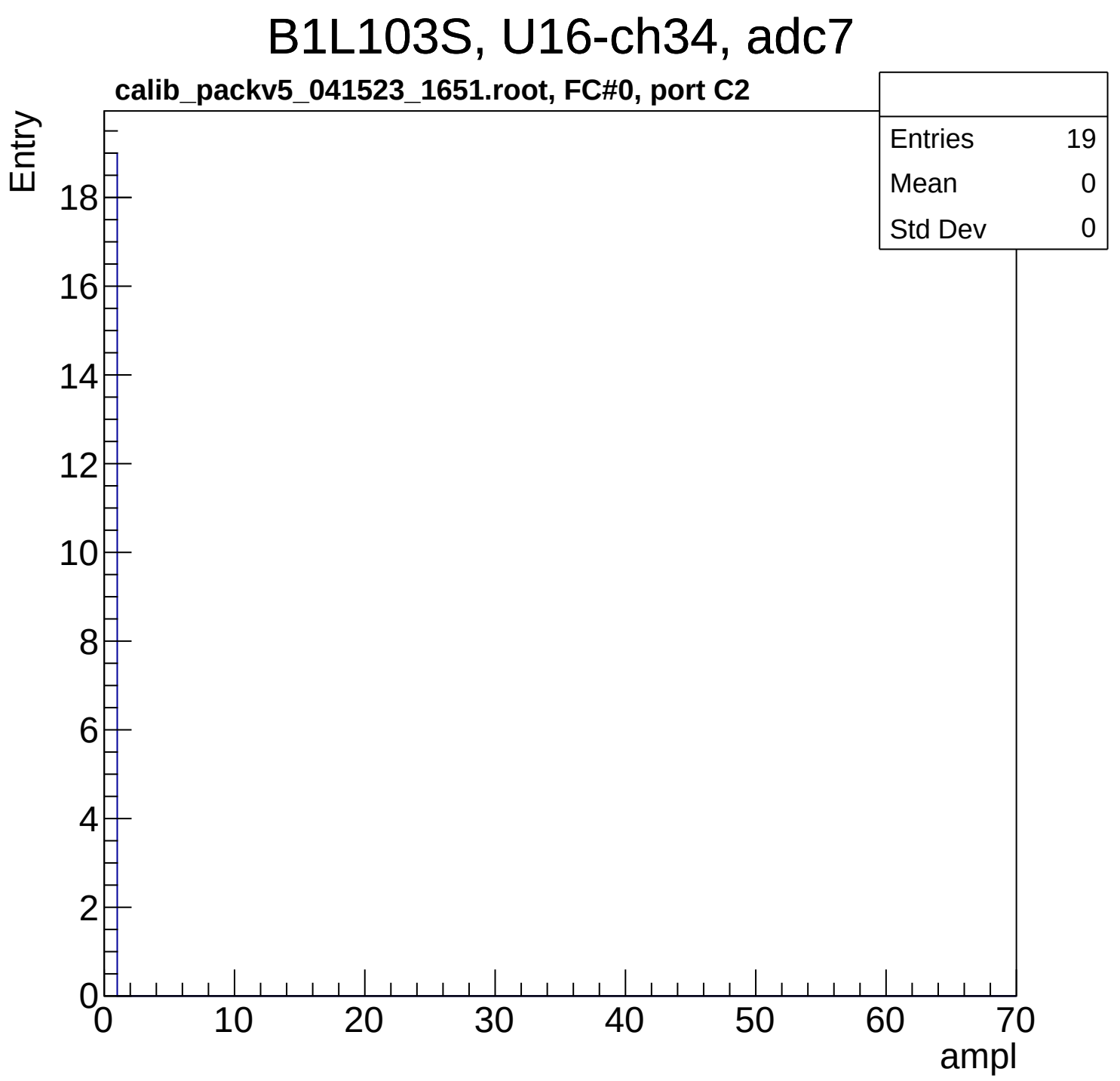
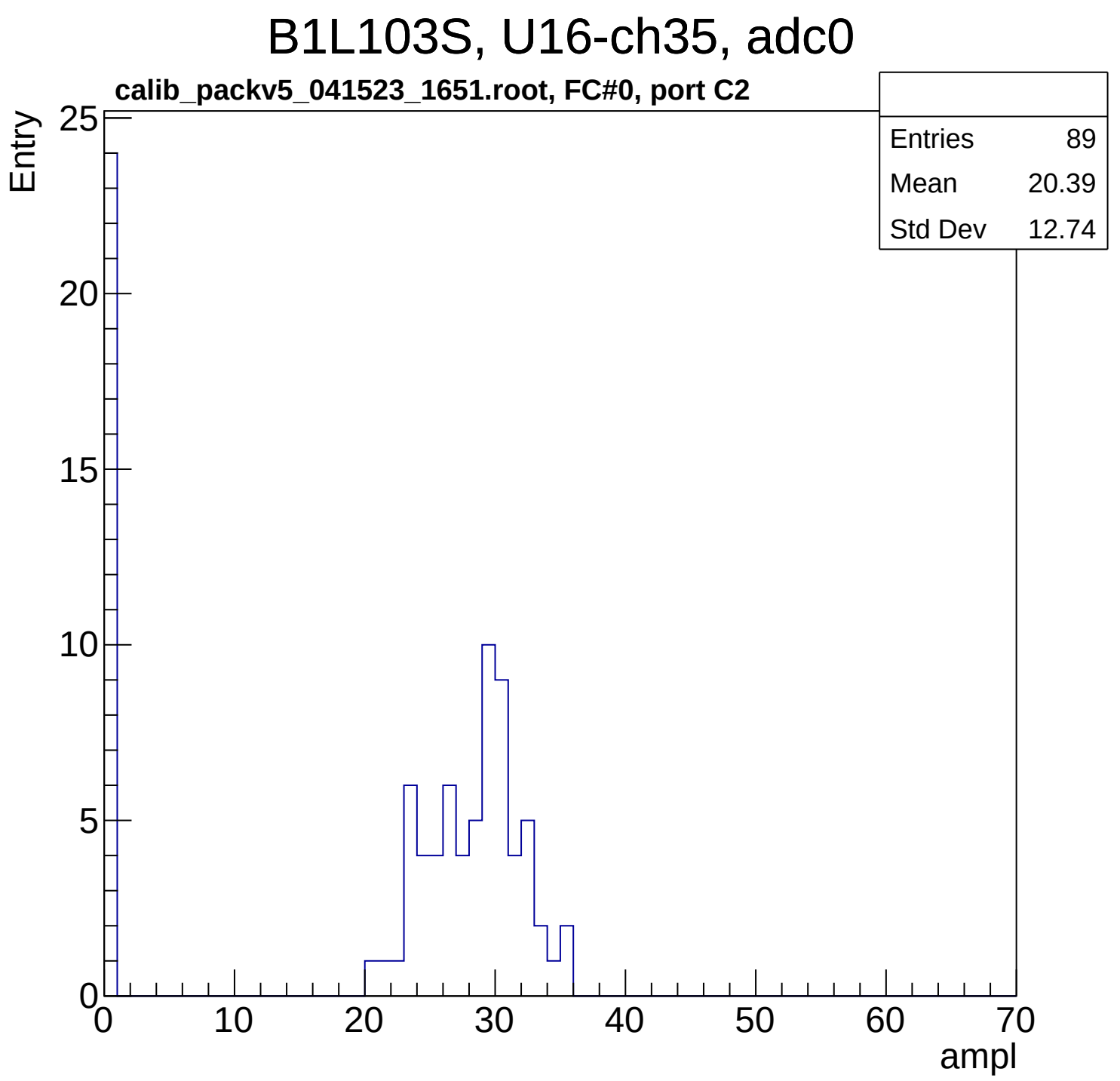

B1L103S, U16-ch34, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.58
Std Dev 1.552
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U16-ch34, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch35, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 20.39
Std Dev 12.74
Entry
ampl
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10
15
20
25
0
10
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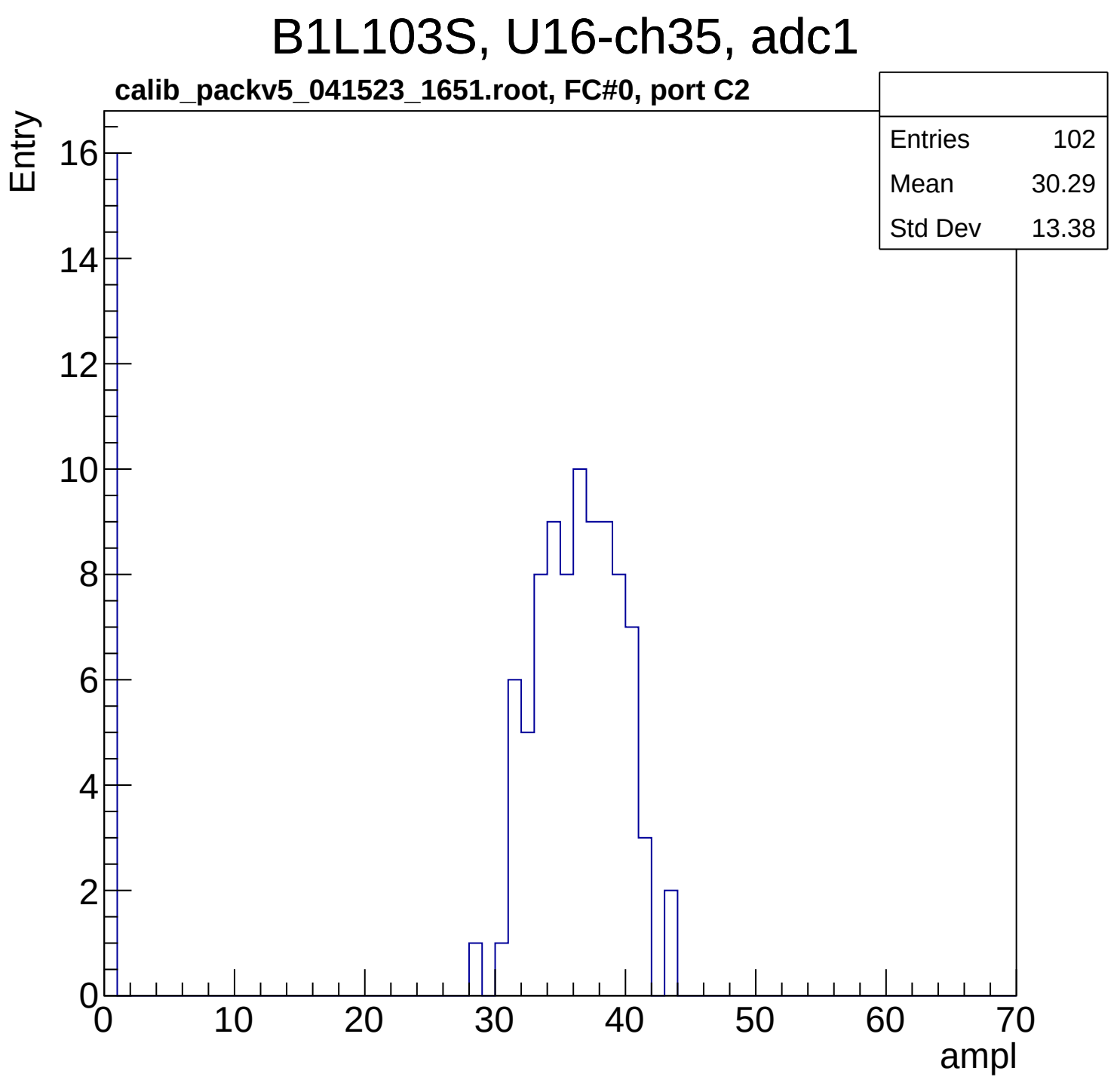
40
50
60
70


B1L103S, U16-ch35, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 30.29
Std Dev 13.38
Entry
0
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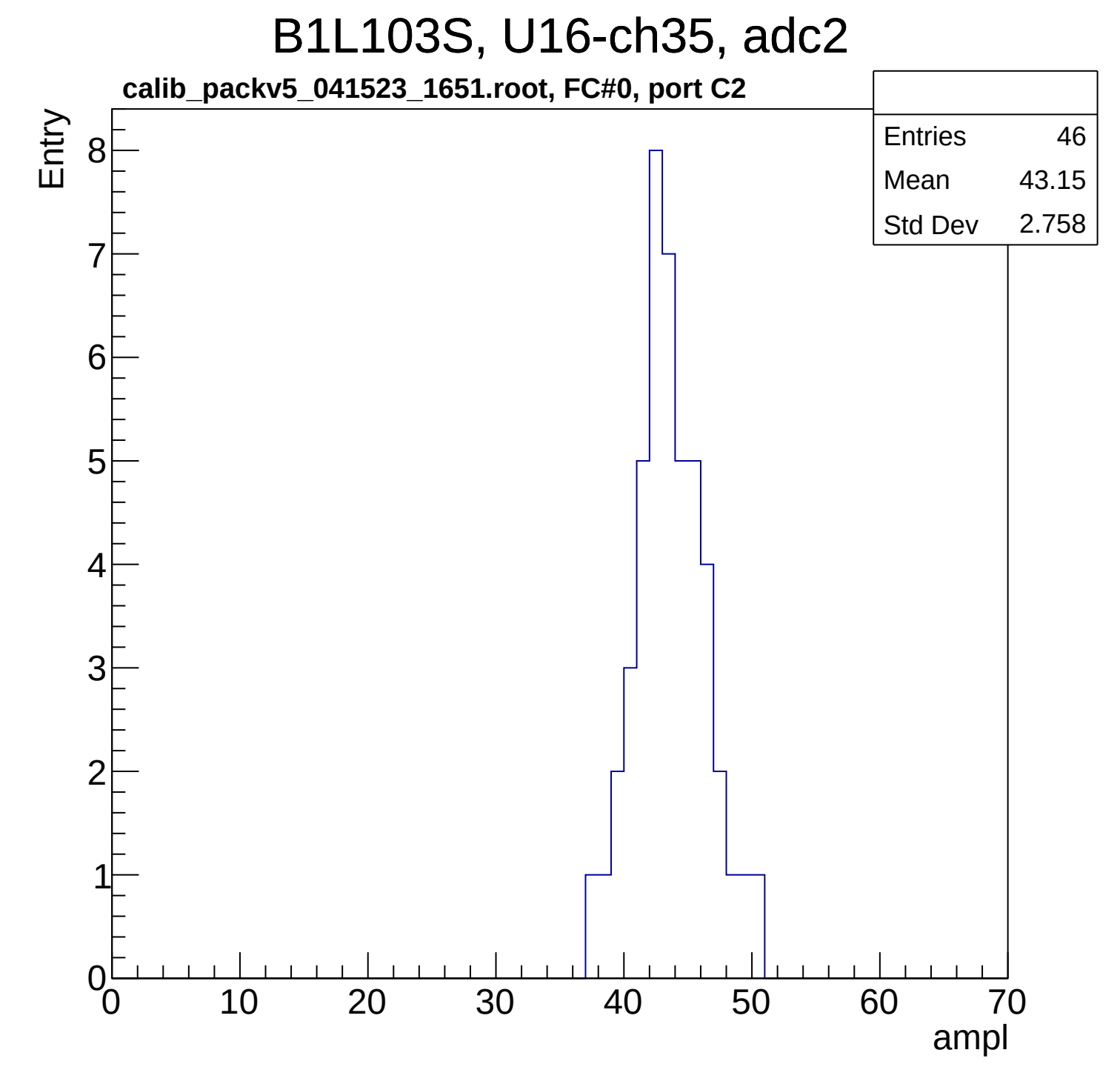
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch35, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 43.15
Std Dev 2.758
Entry
ampl
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2
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4
5
6
7
8
0
10
20
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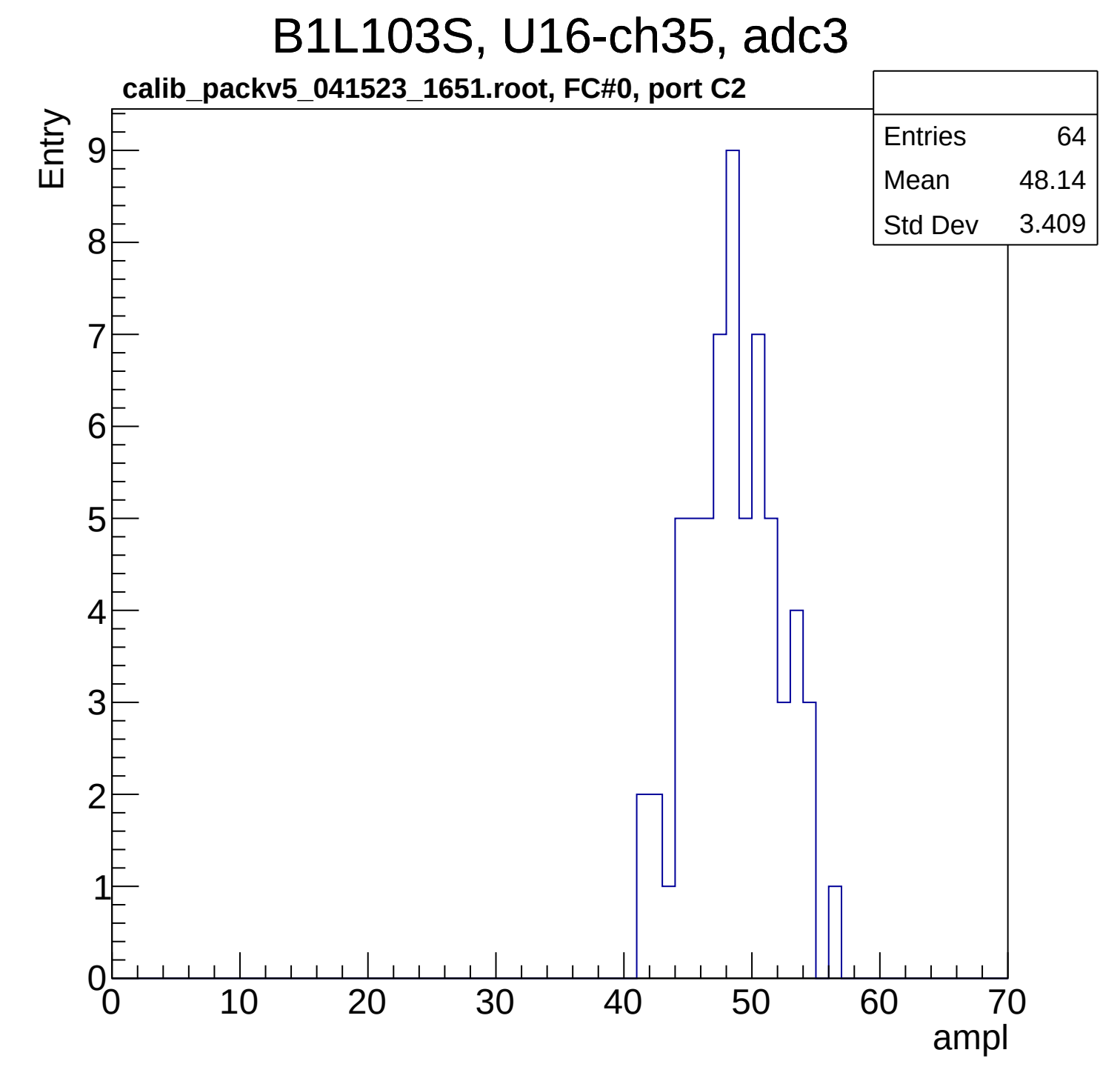
40
50
60
70


B1L103S, U16-ch35, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 48.14
Std Dev 3.409
Entry
ampl
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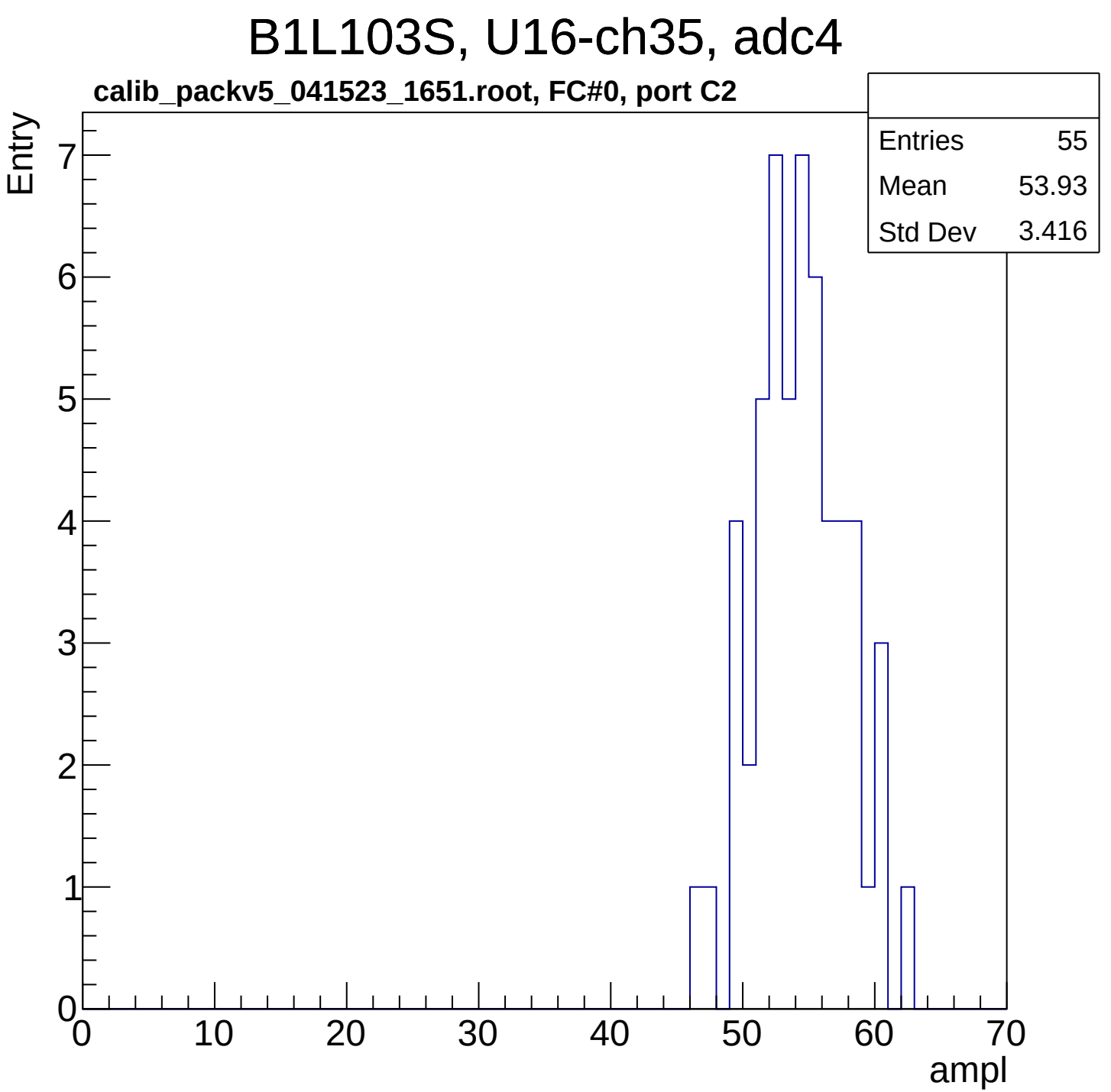
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch35, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 53.93
Std Dev 3.416
Entry
ampl
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1
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3
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7
0
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50
60
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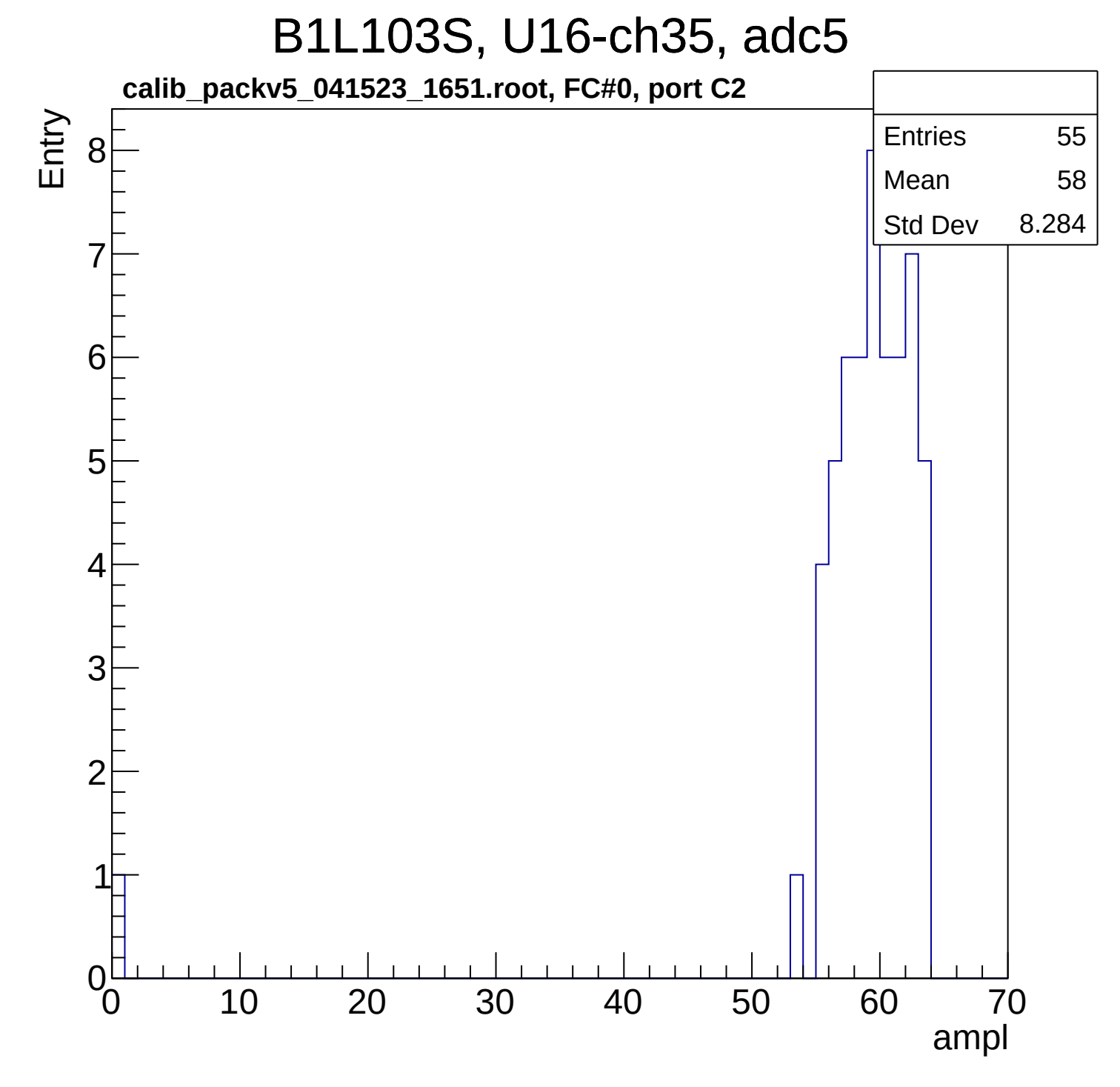
B1L103S, U16-ch35, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58
Std Dev 8.284
Entry
ampl
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2
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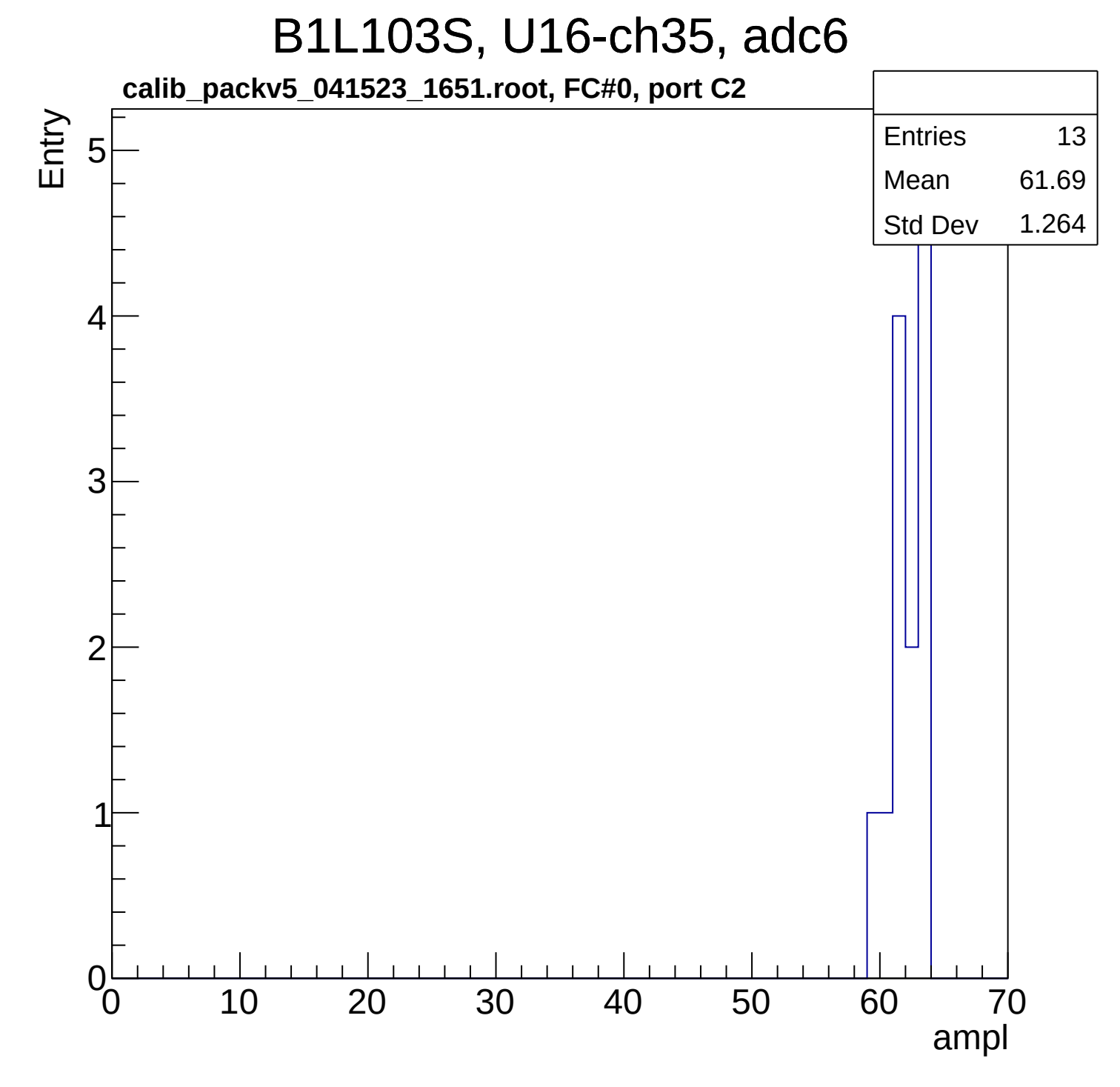
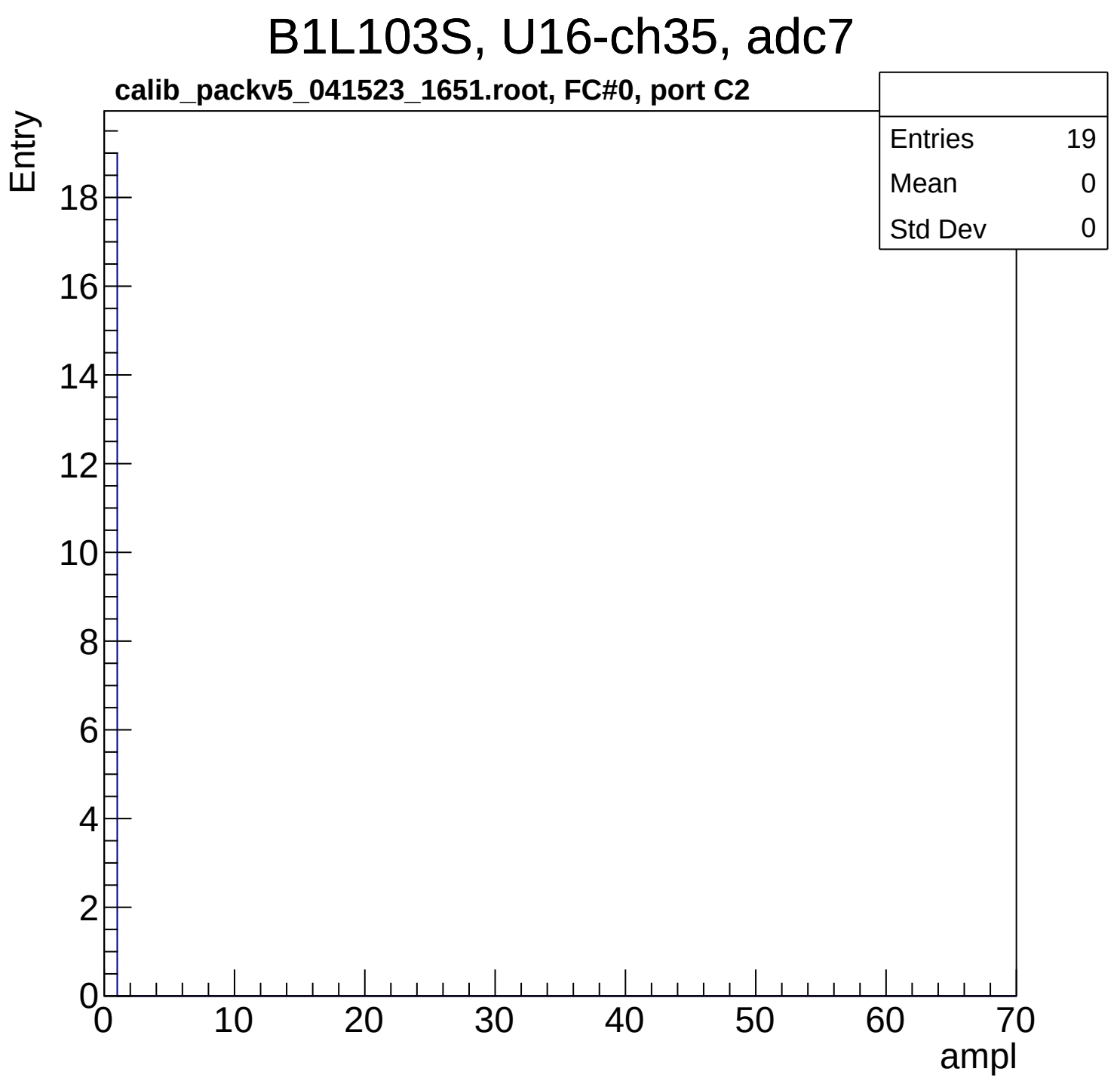
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch35, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.69
Std Dev 1.264
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U16-ch35, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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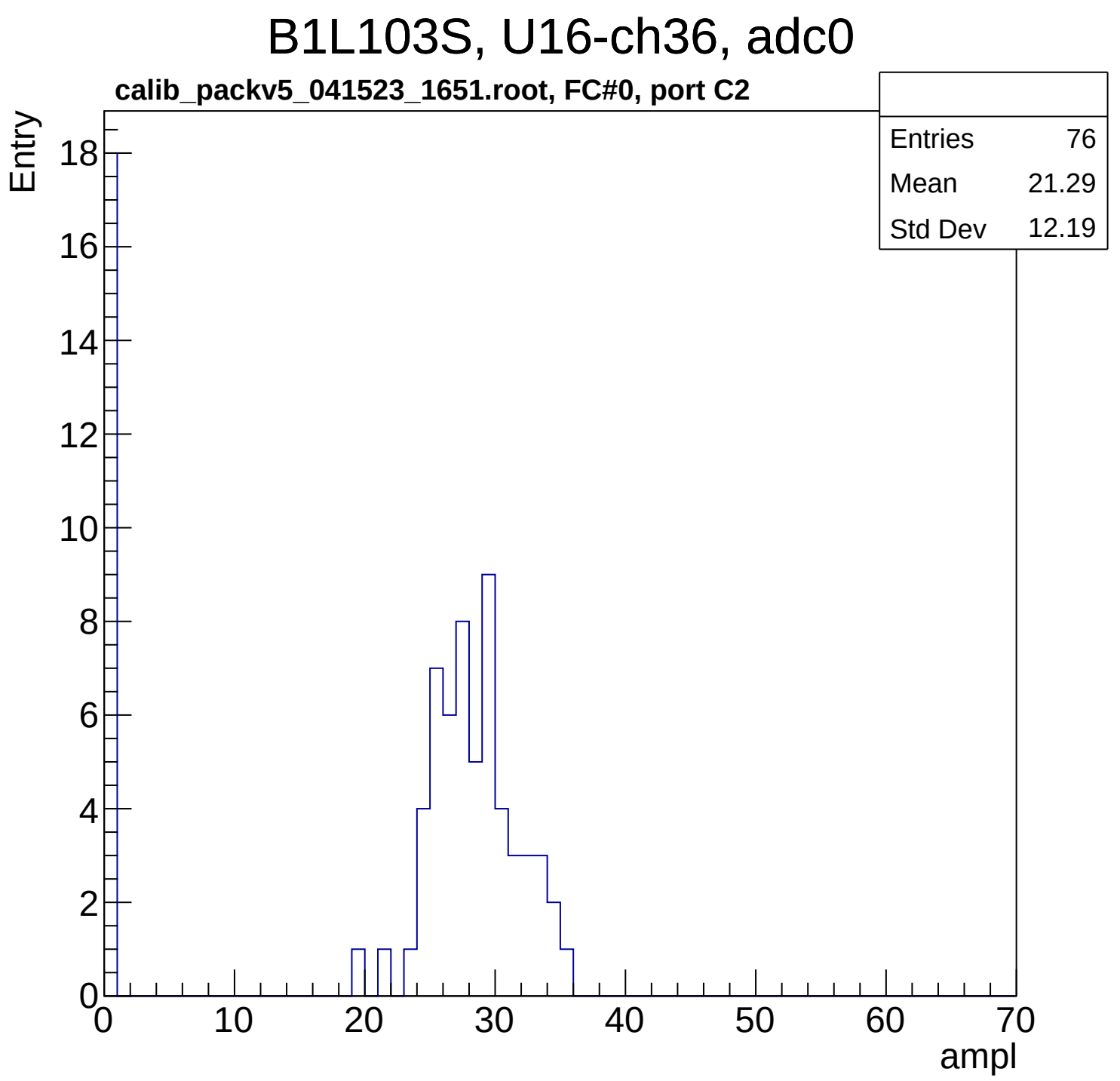
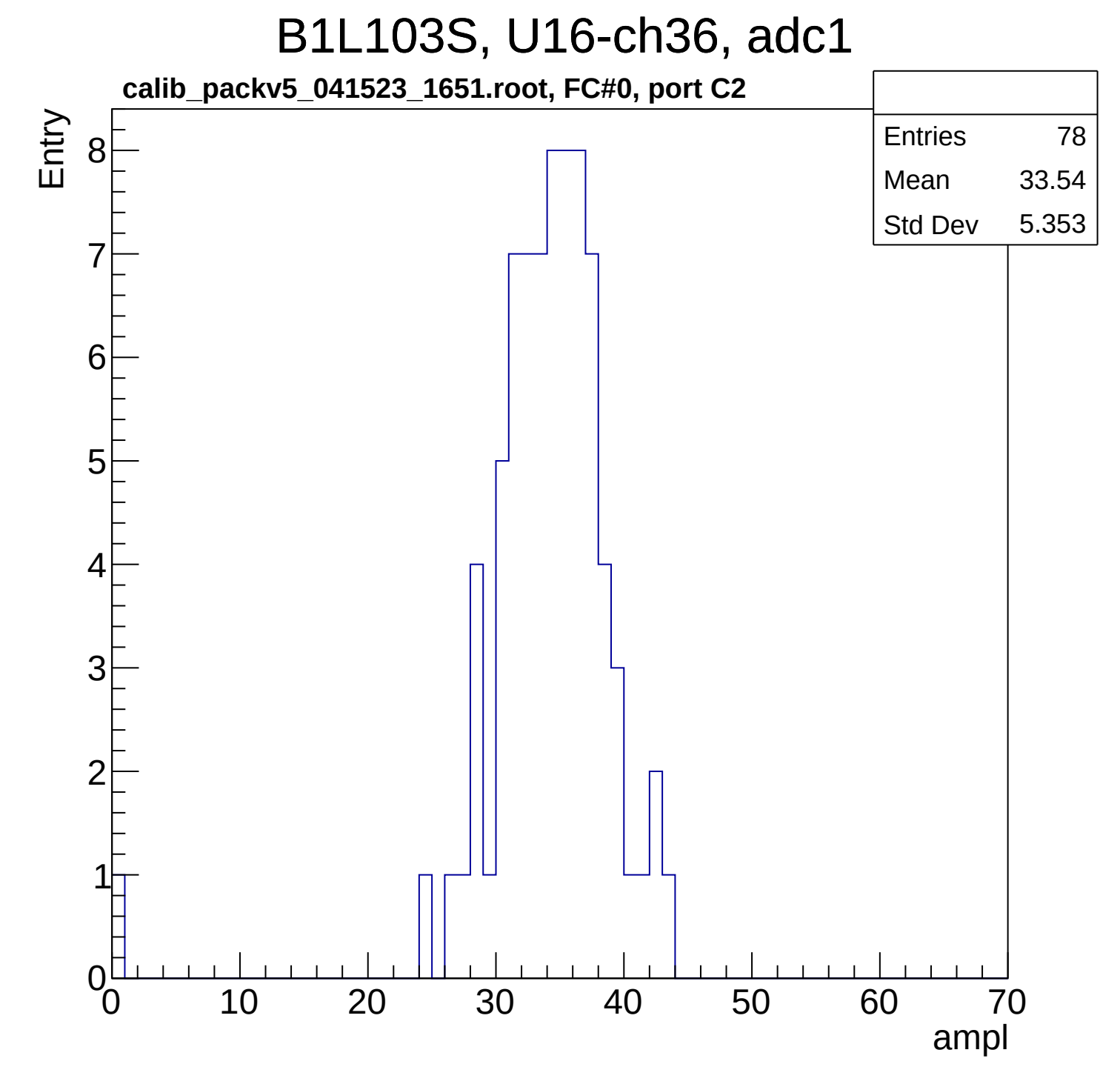
50
60
70
ampl


B1L103S, U16-ch36, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 21.29
Std Dev 12.19
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch36, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 33.54
Std Dev 5.353
Entry
ampl
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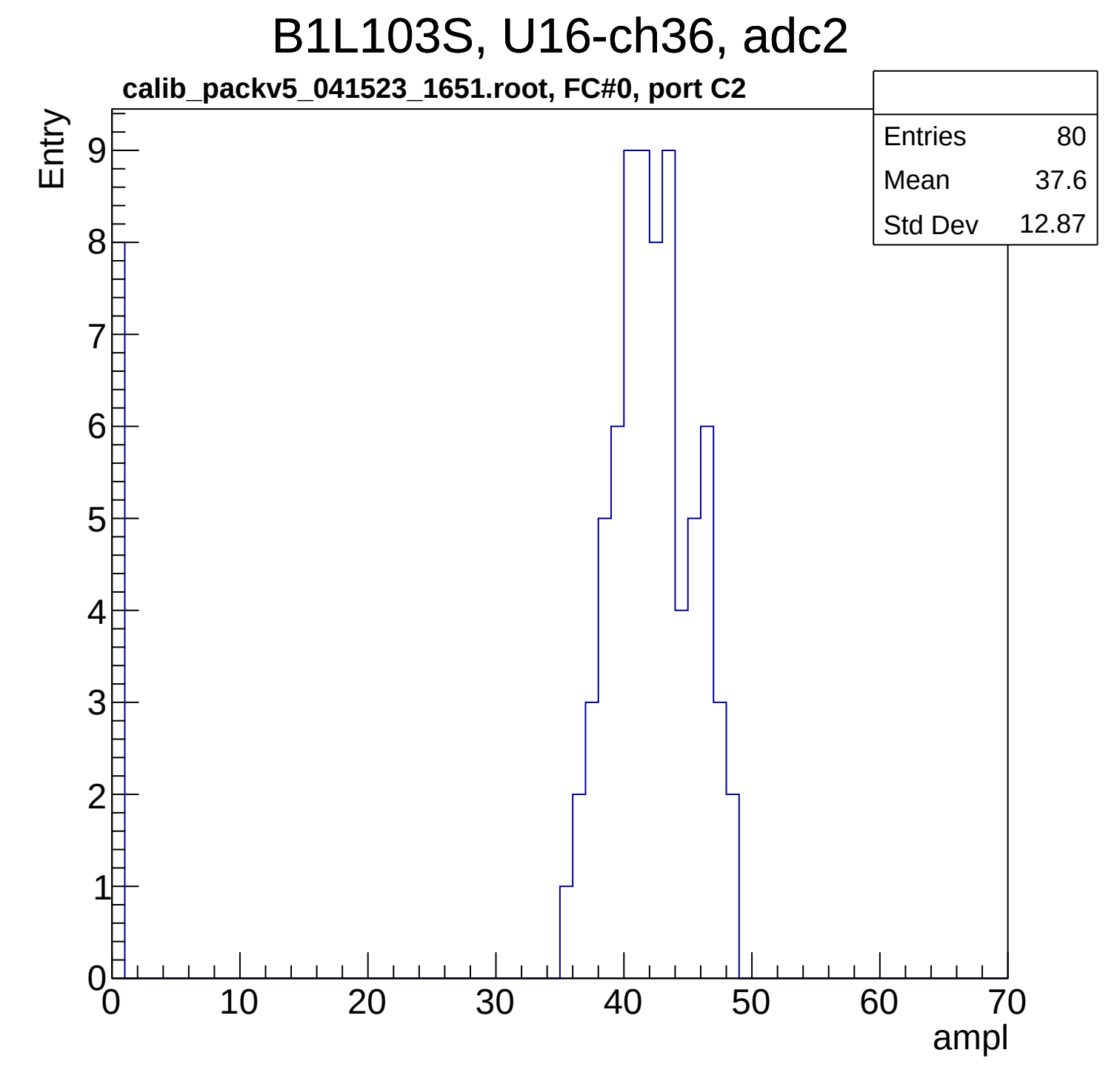
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch36, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 37.6
Std Dev 12.87
Entry
ampl
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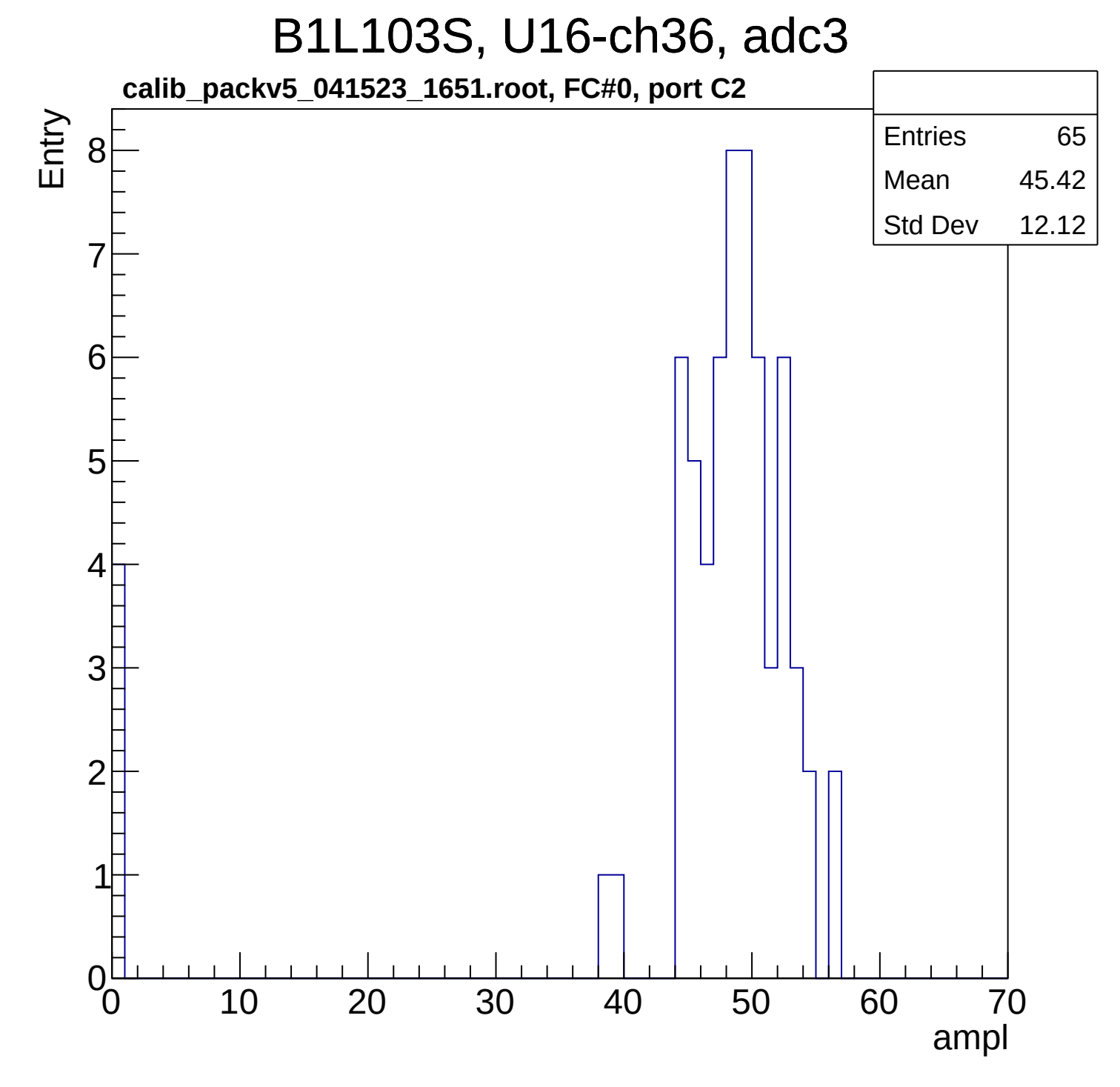
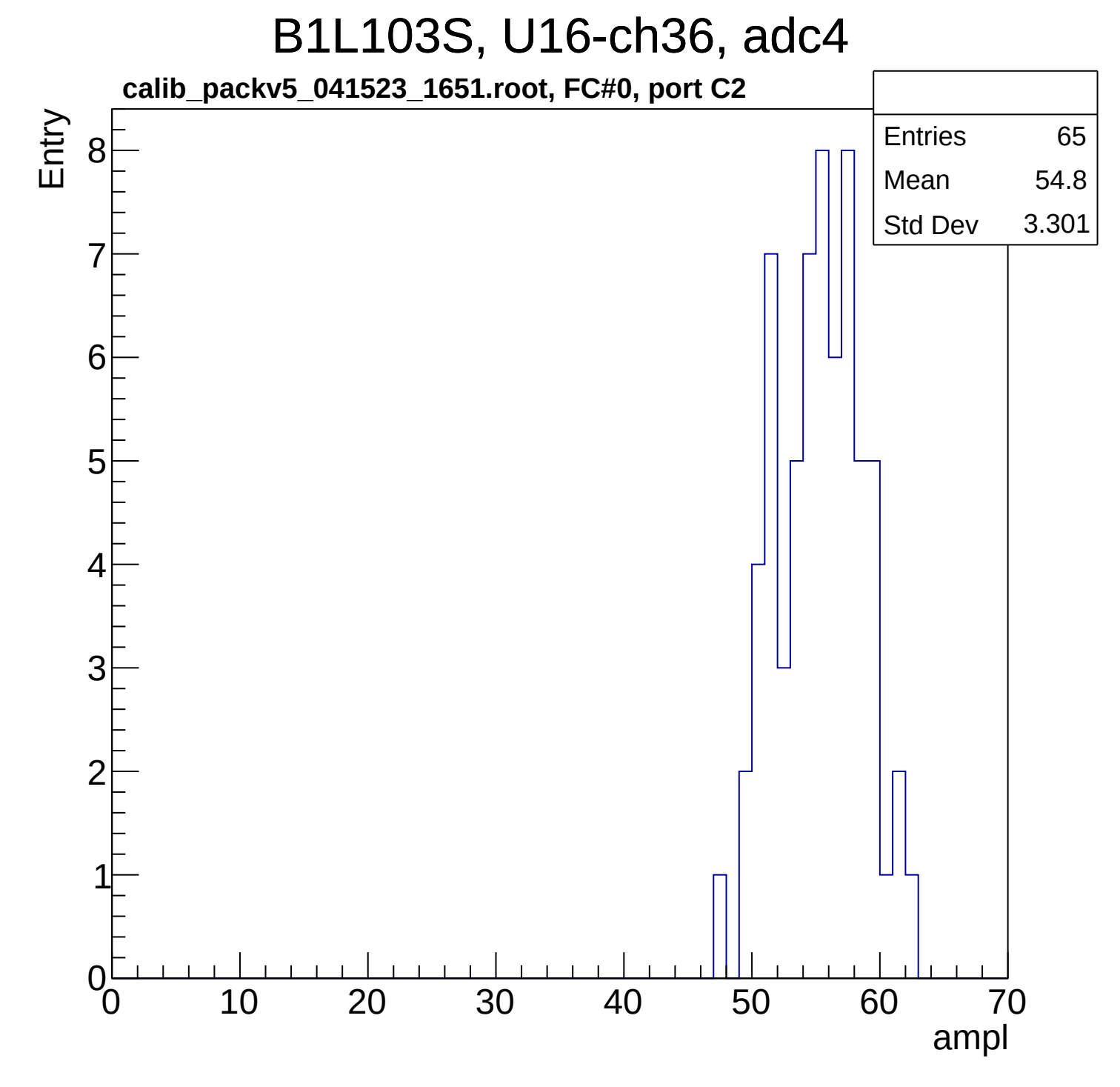
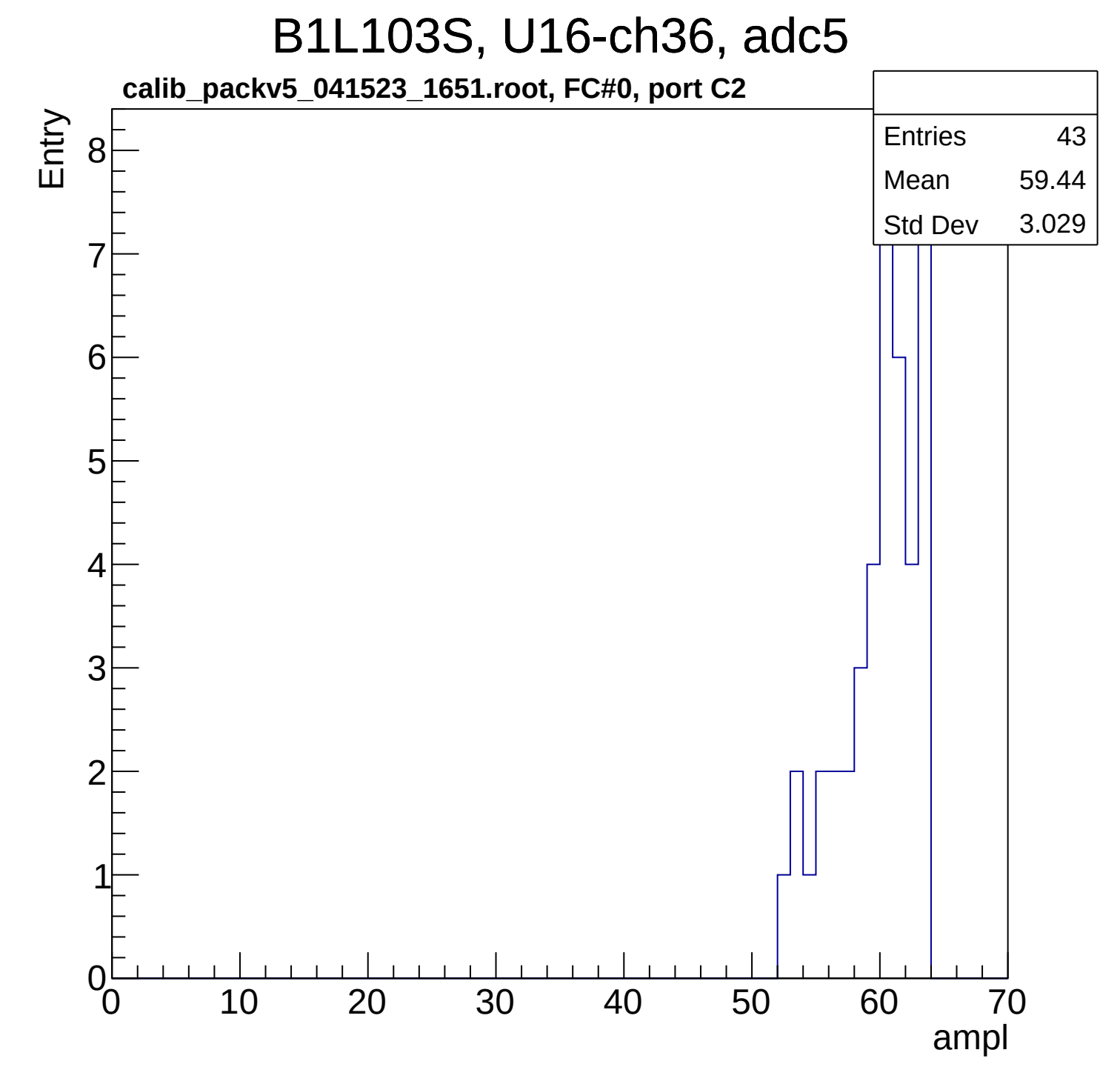
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch36, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 45.42
Std Dev 12.12
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch36, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 54.8
Std Dev 3.301
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch36, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 59.44
Std Dev 3.029
Entry
ampl
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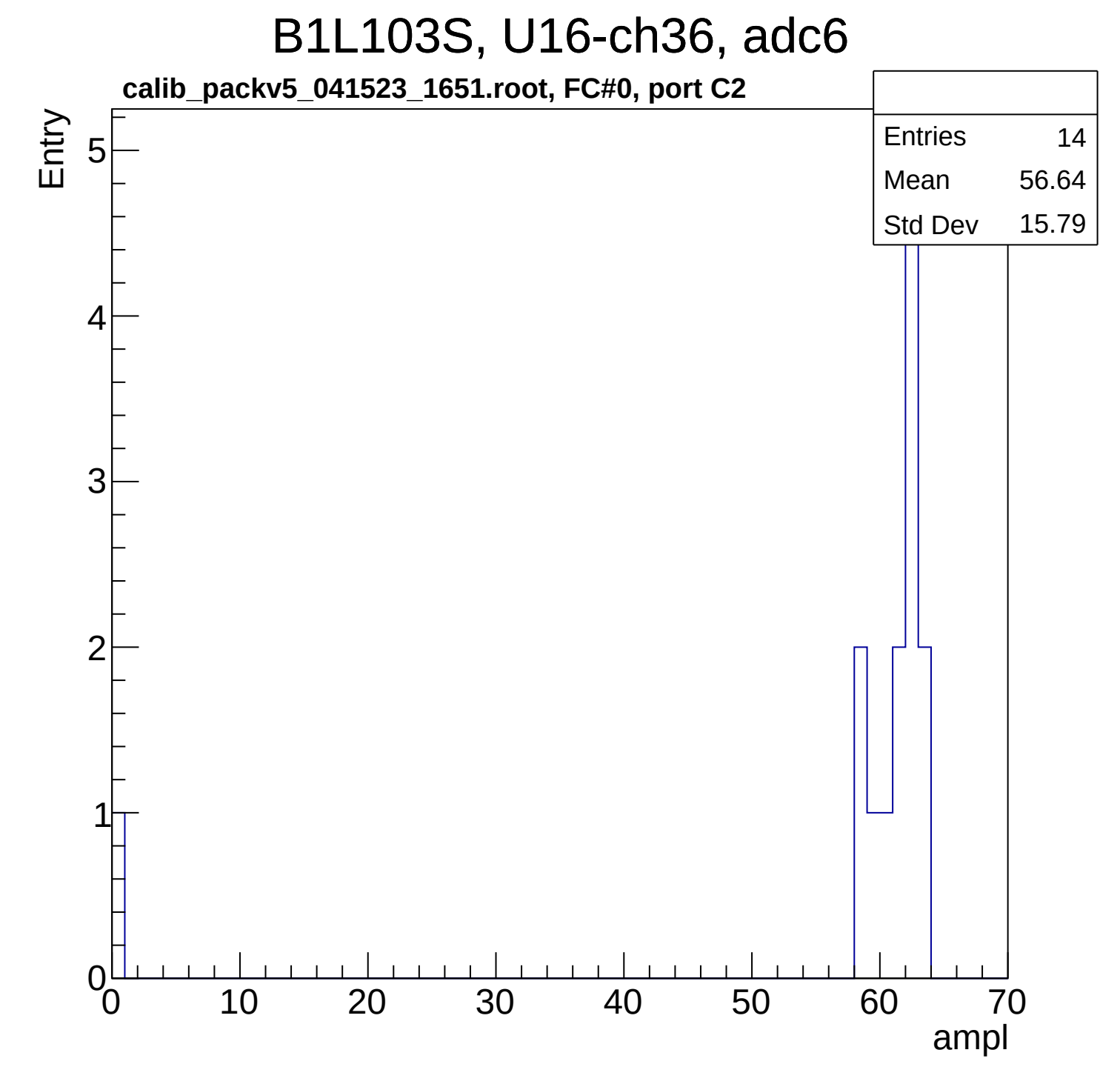
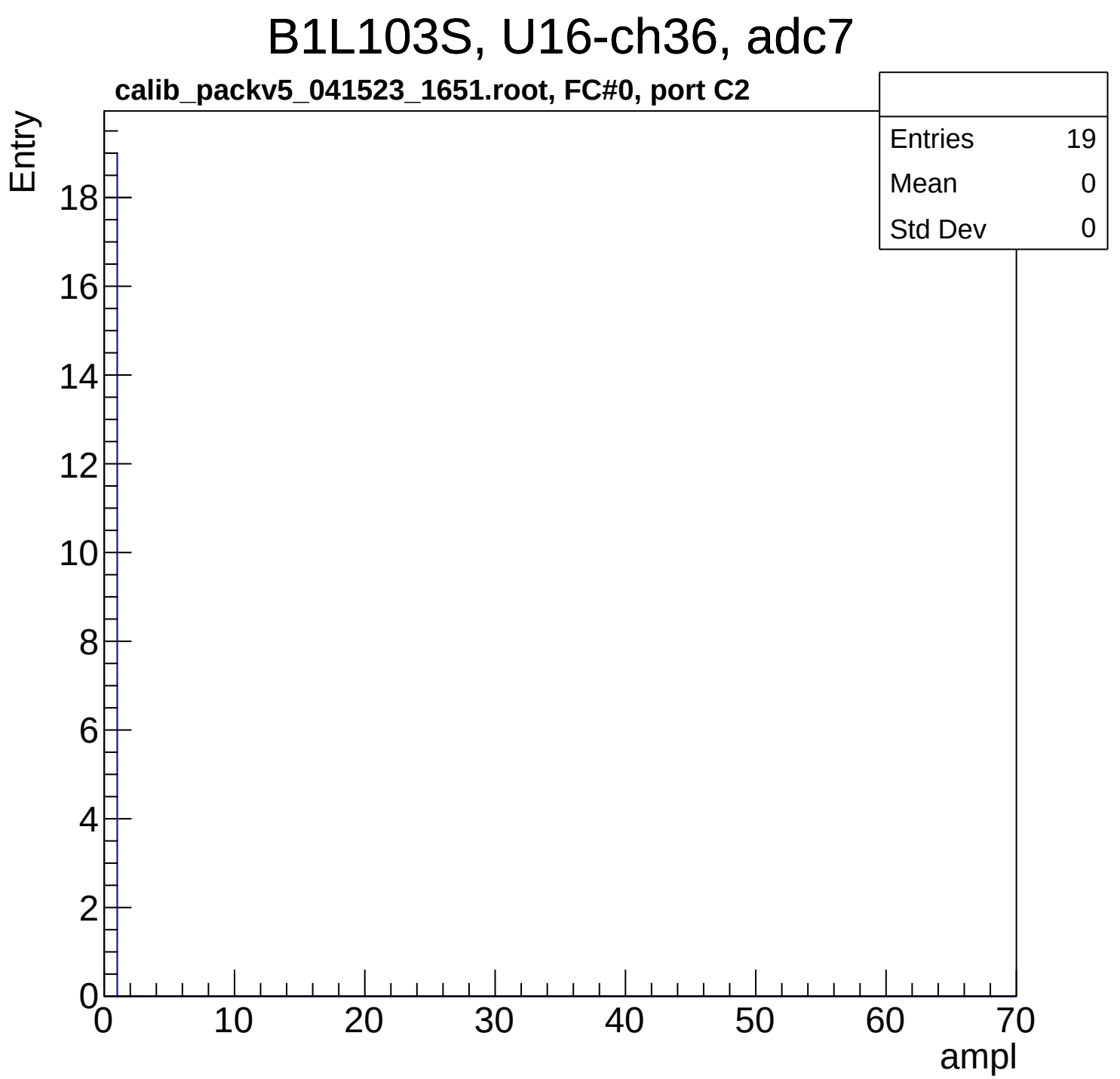
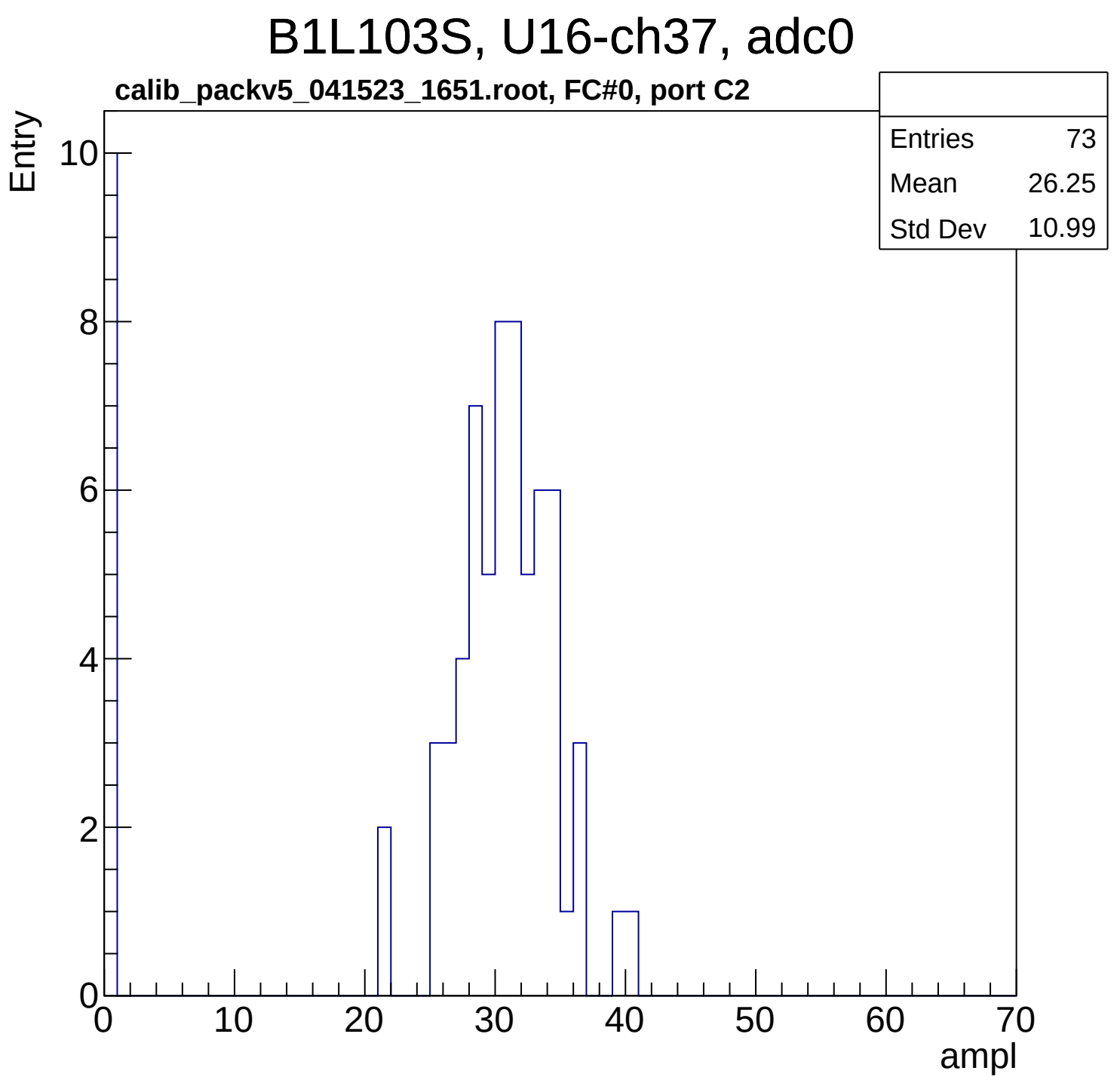
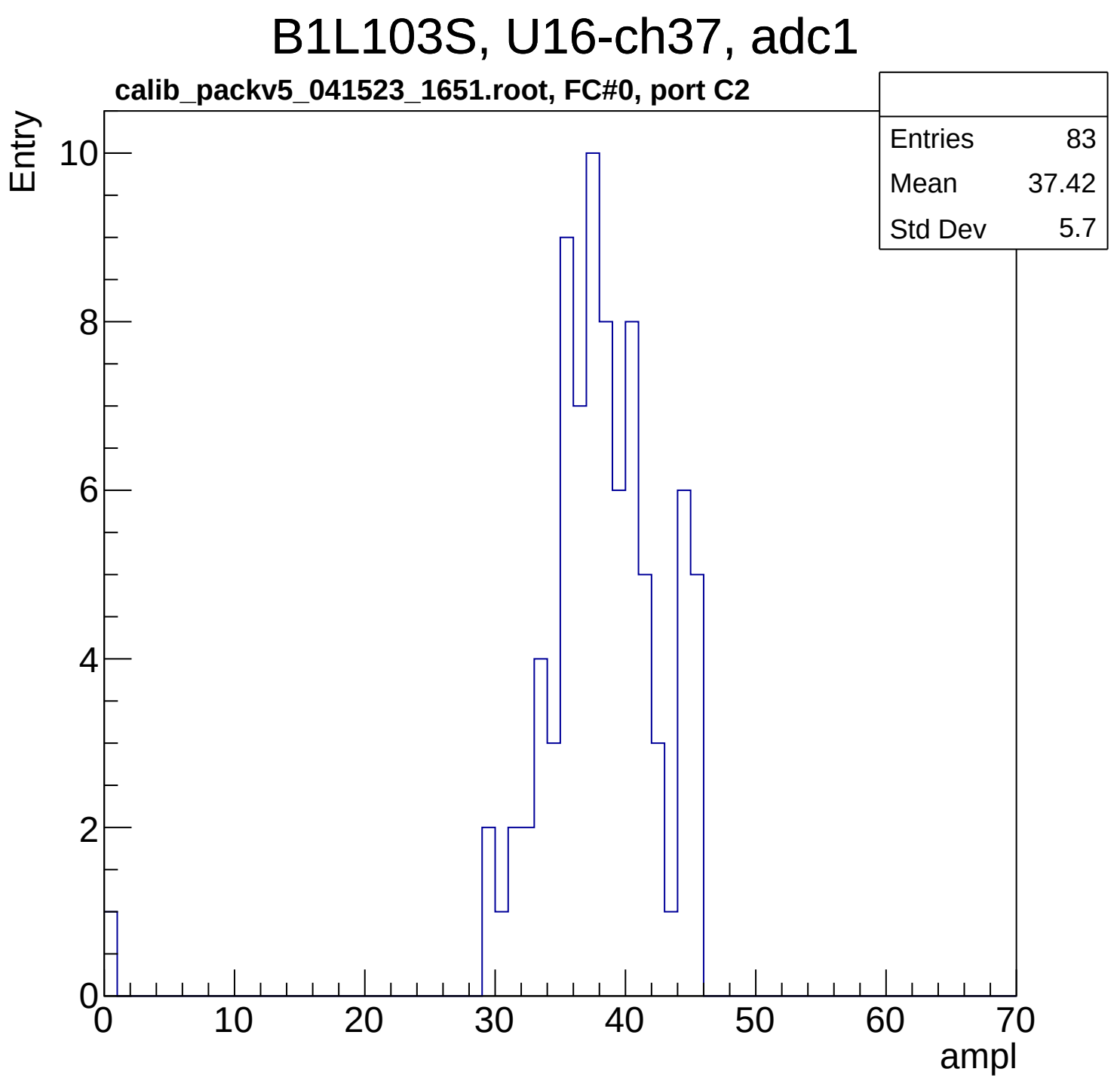
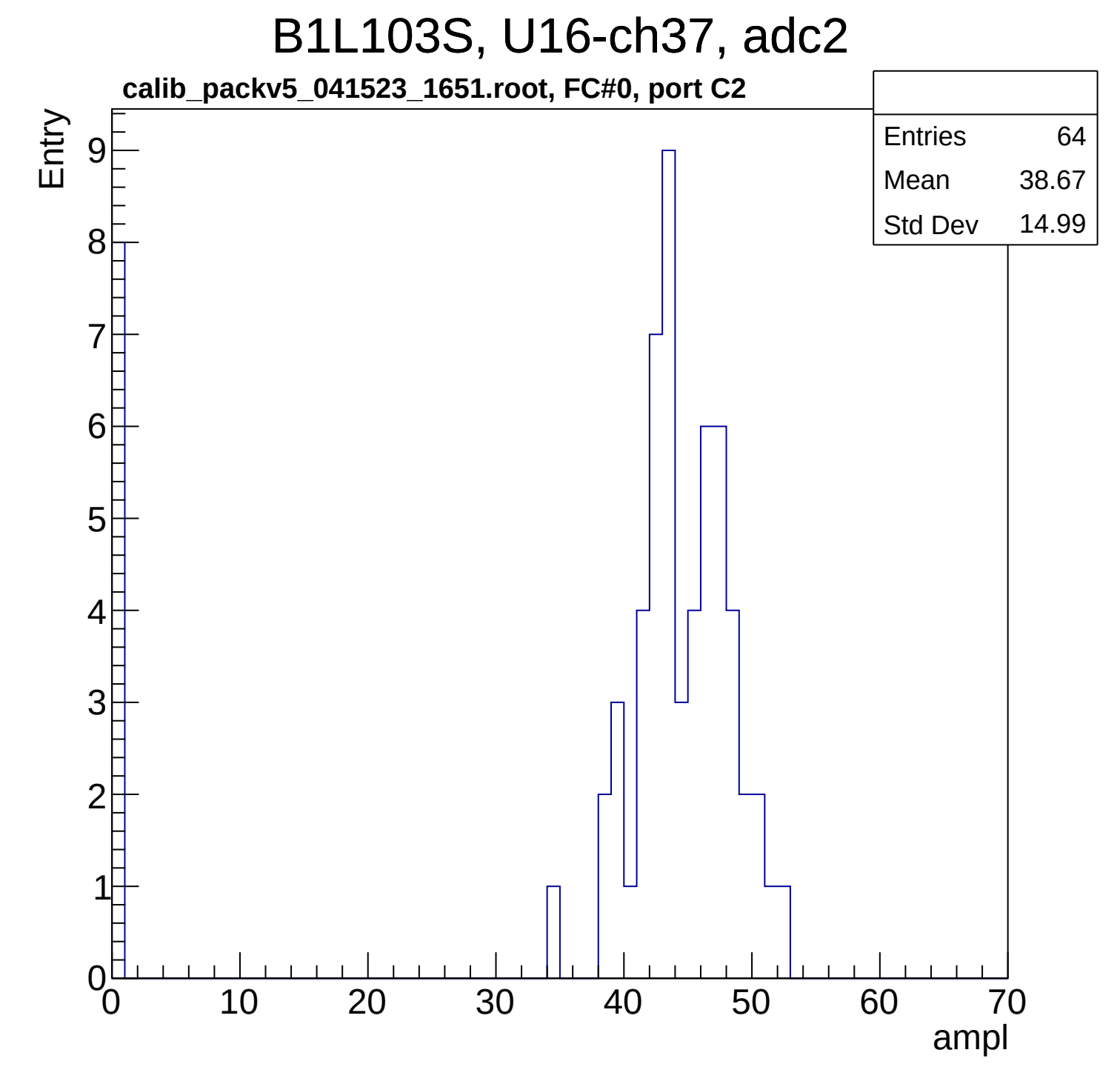
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch36, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 56.64
Std Dev 15.79
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U16-ch36, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch37, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 26.25
Std Dev 10.99
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch37, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 37.42
Std Dev 5.7
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch37, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 38.67
Std Dev 14.99
Entry
ampl
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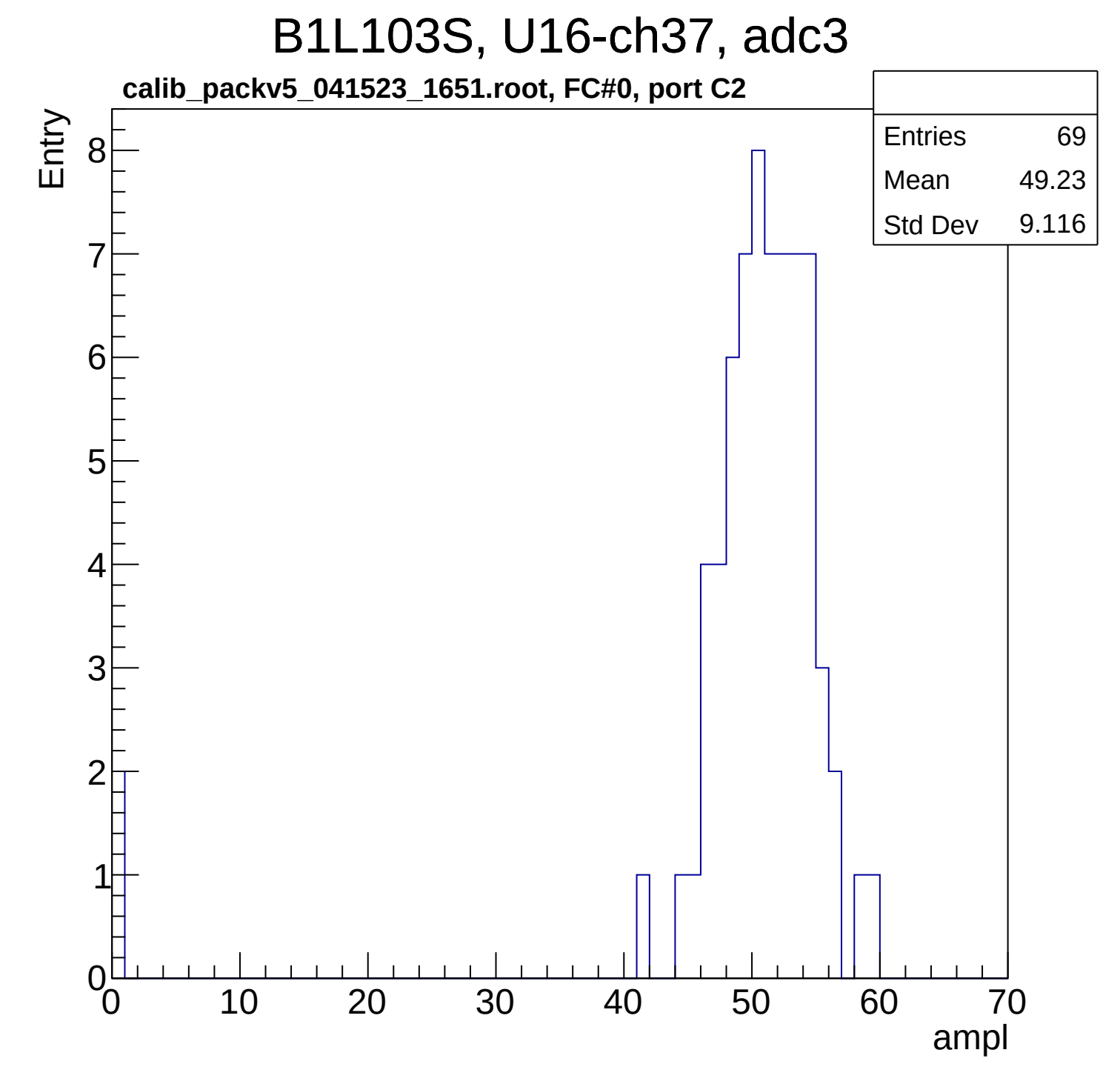
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch37, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 49.23
Std Dev 9.116
Entry
ampl
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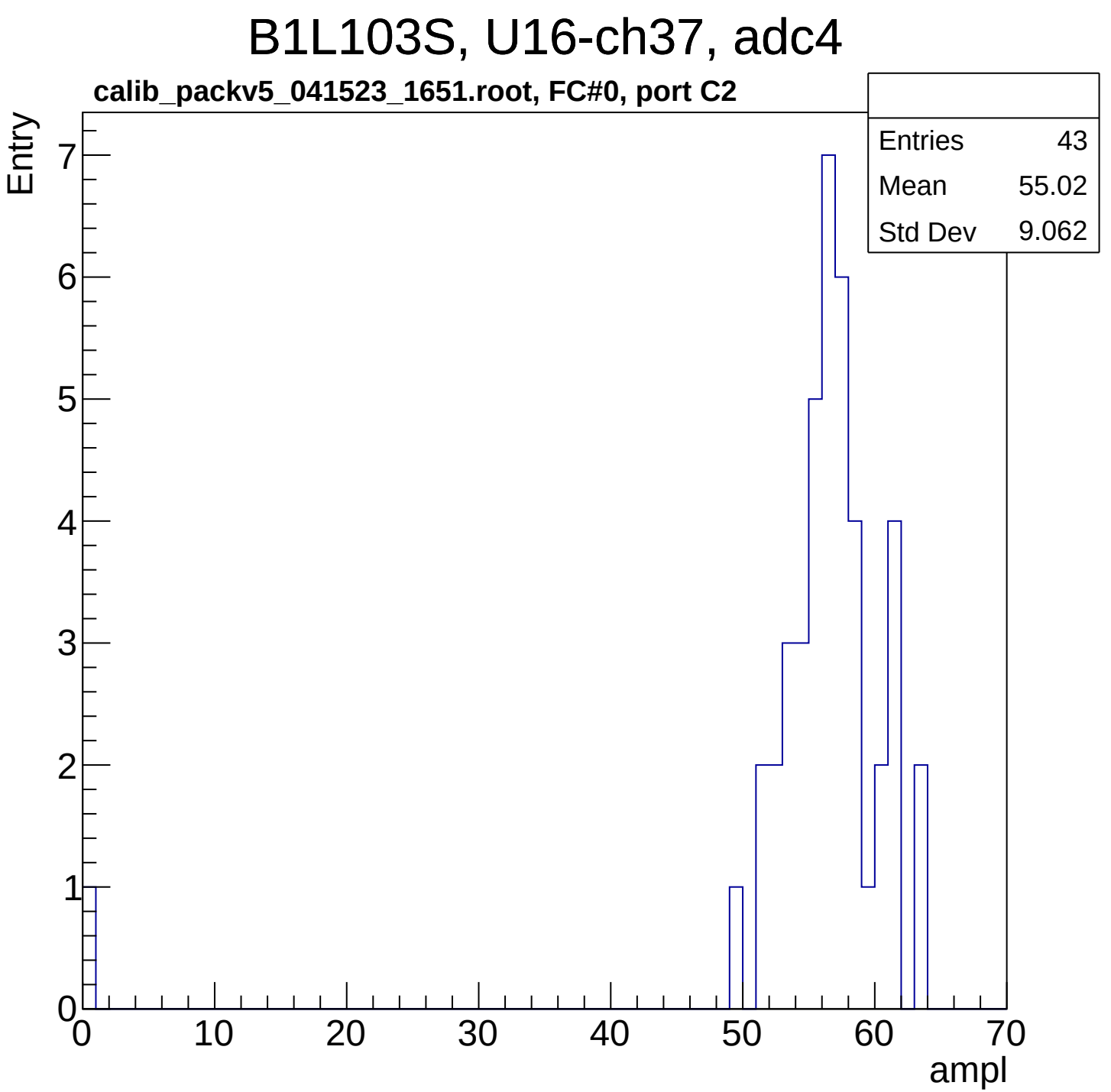
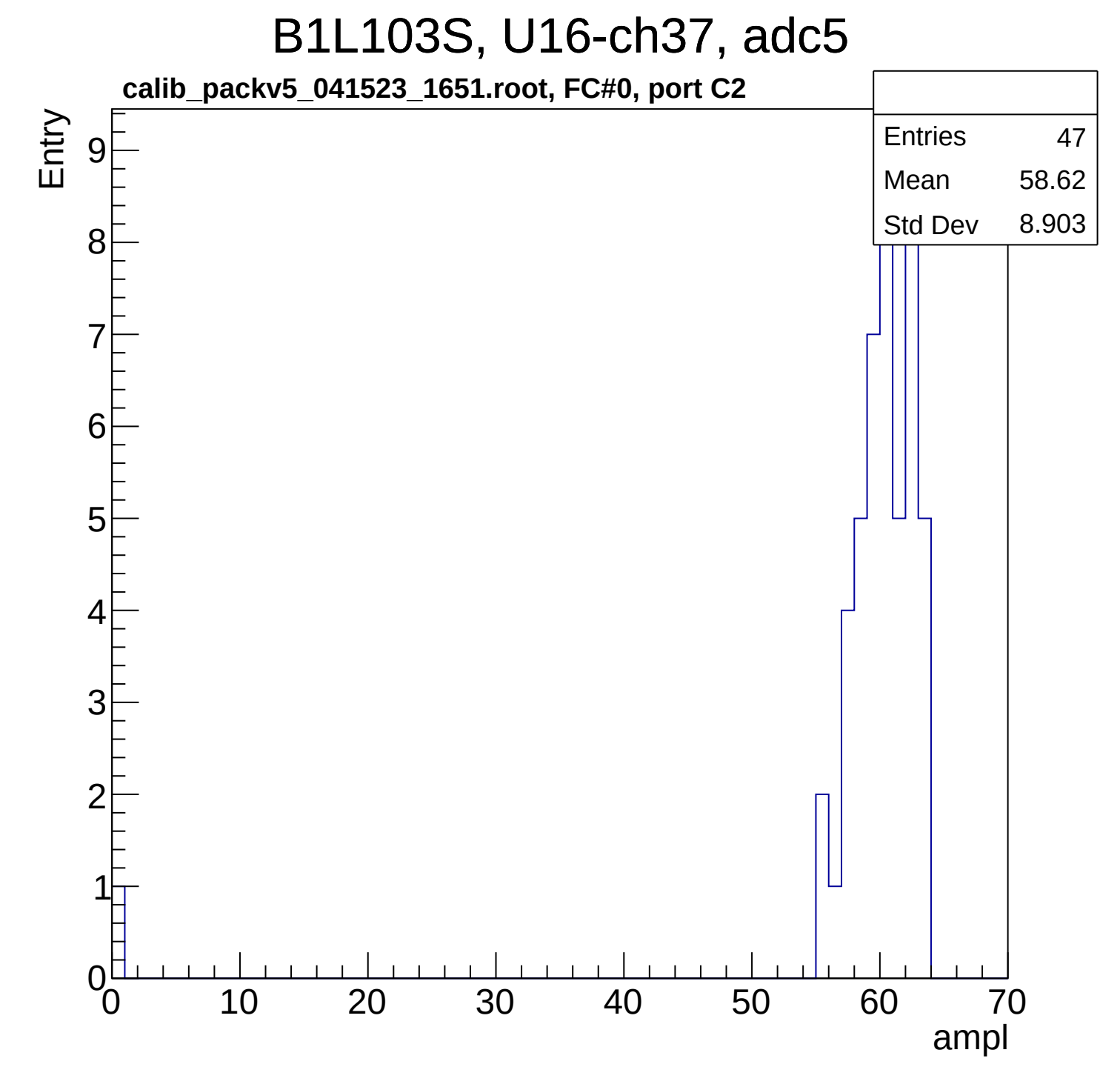
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch37, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 55.02
Std Dev 9.062
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch37, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.62
Std Dev 8.903
Entry
ampl
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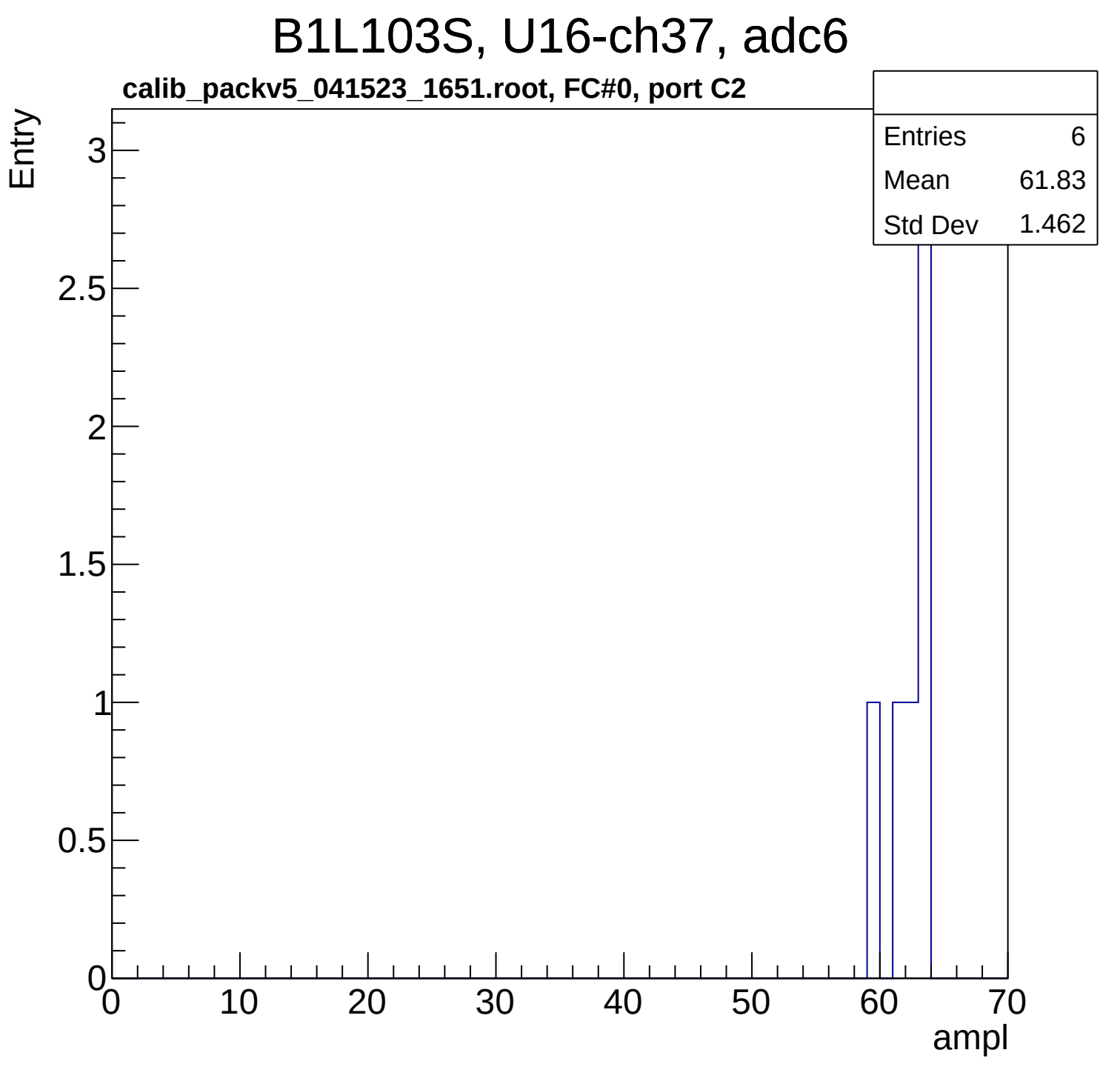
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch37, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.83
Std Dev 1.462
Entry
ampl
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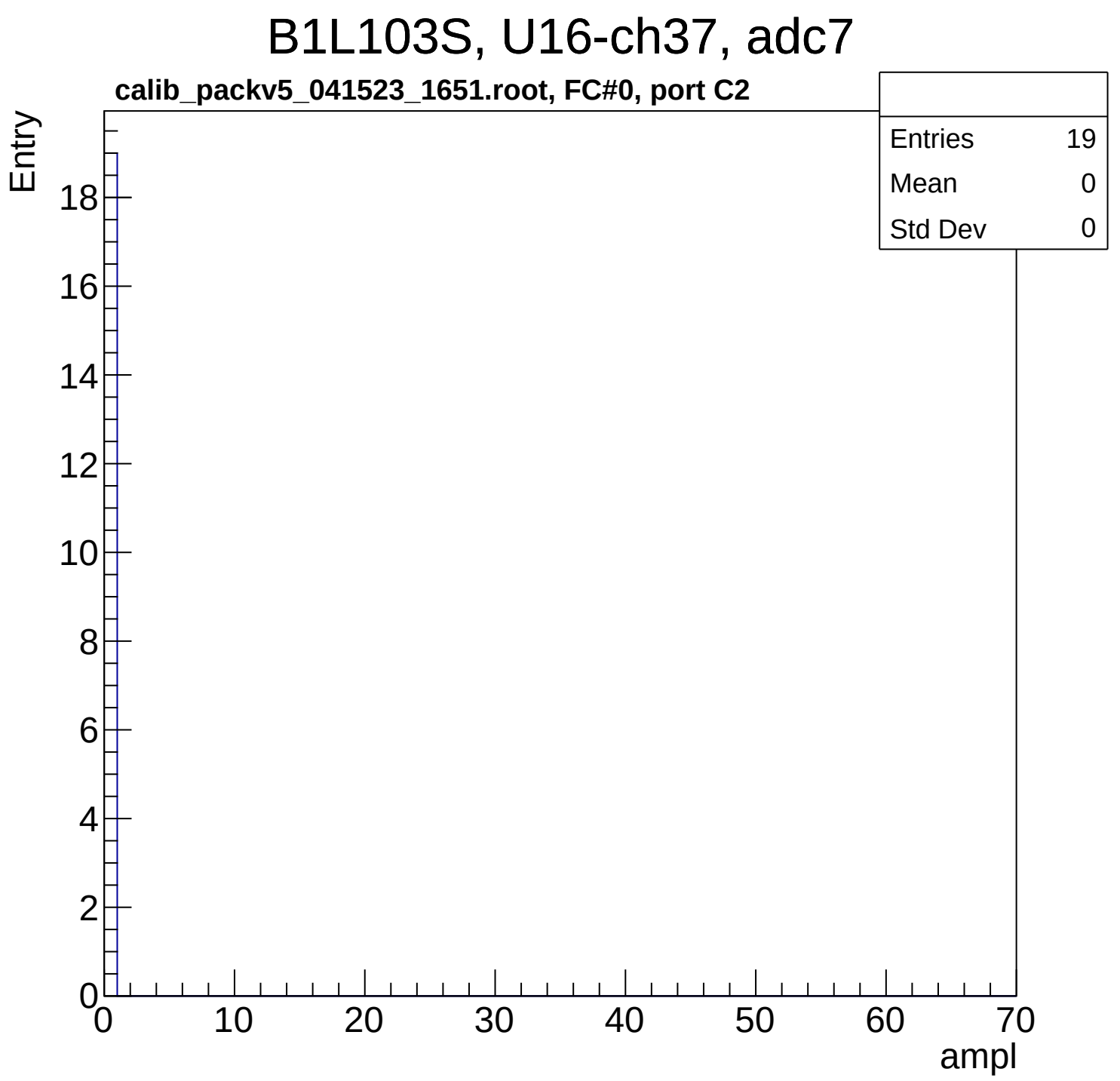
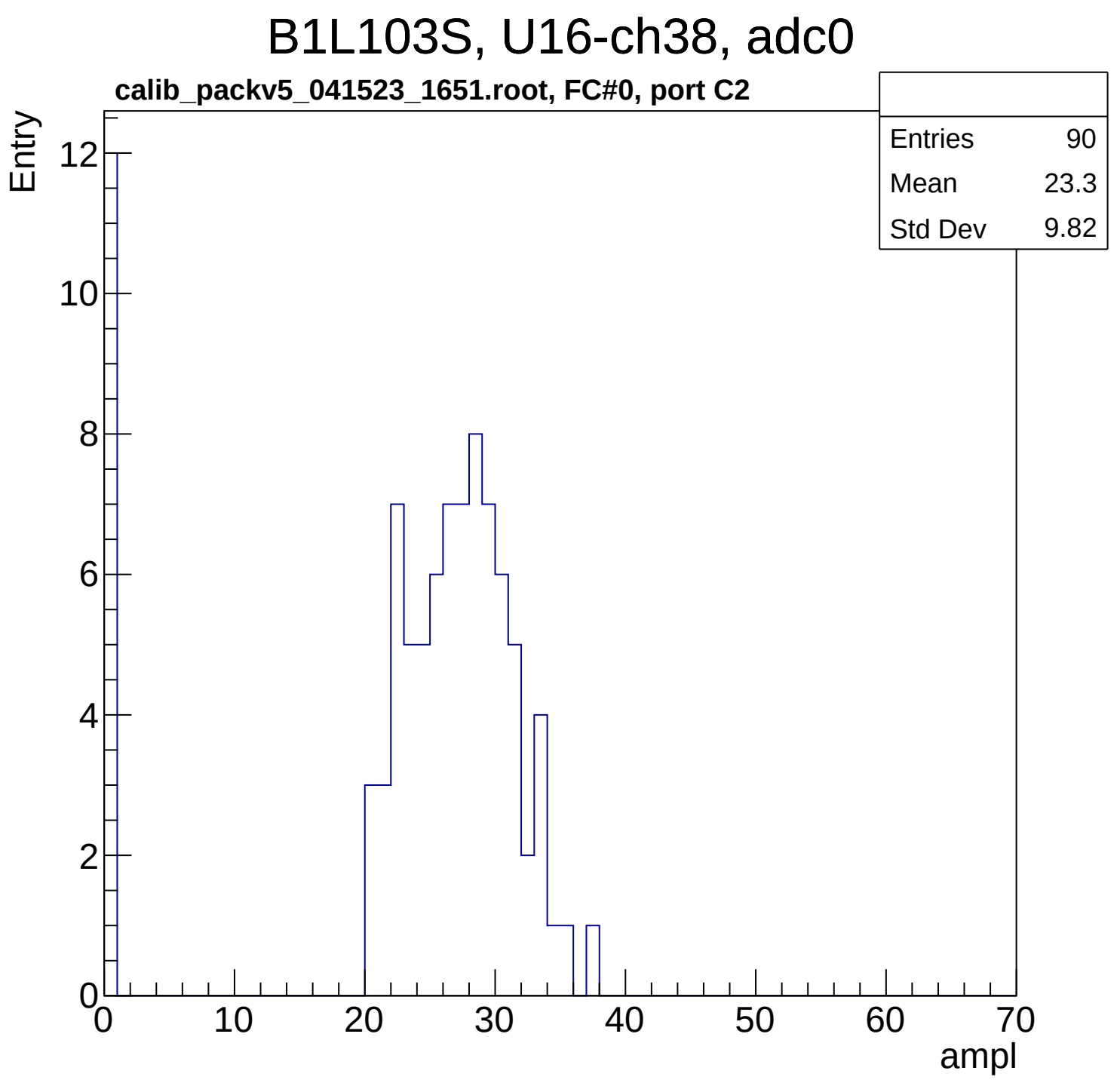
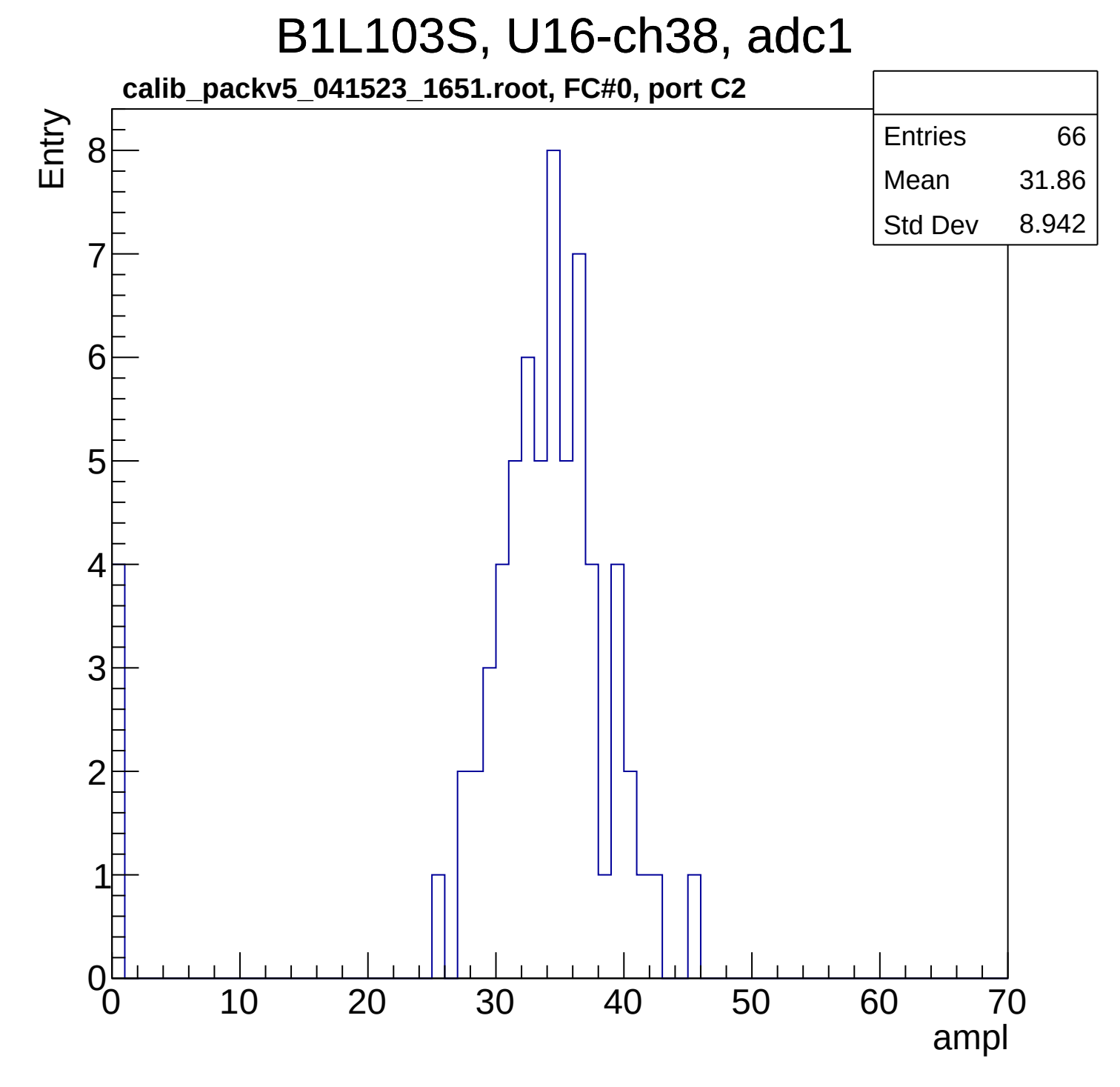
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U16-ch37, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch38, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 23.3
Std Dev 9.82
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch38, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 31.86
Std Dev 8.942
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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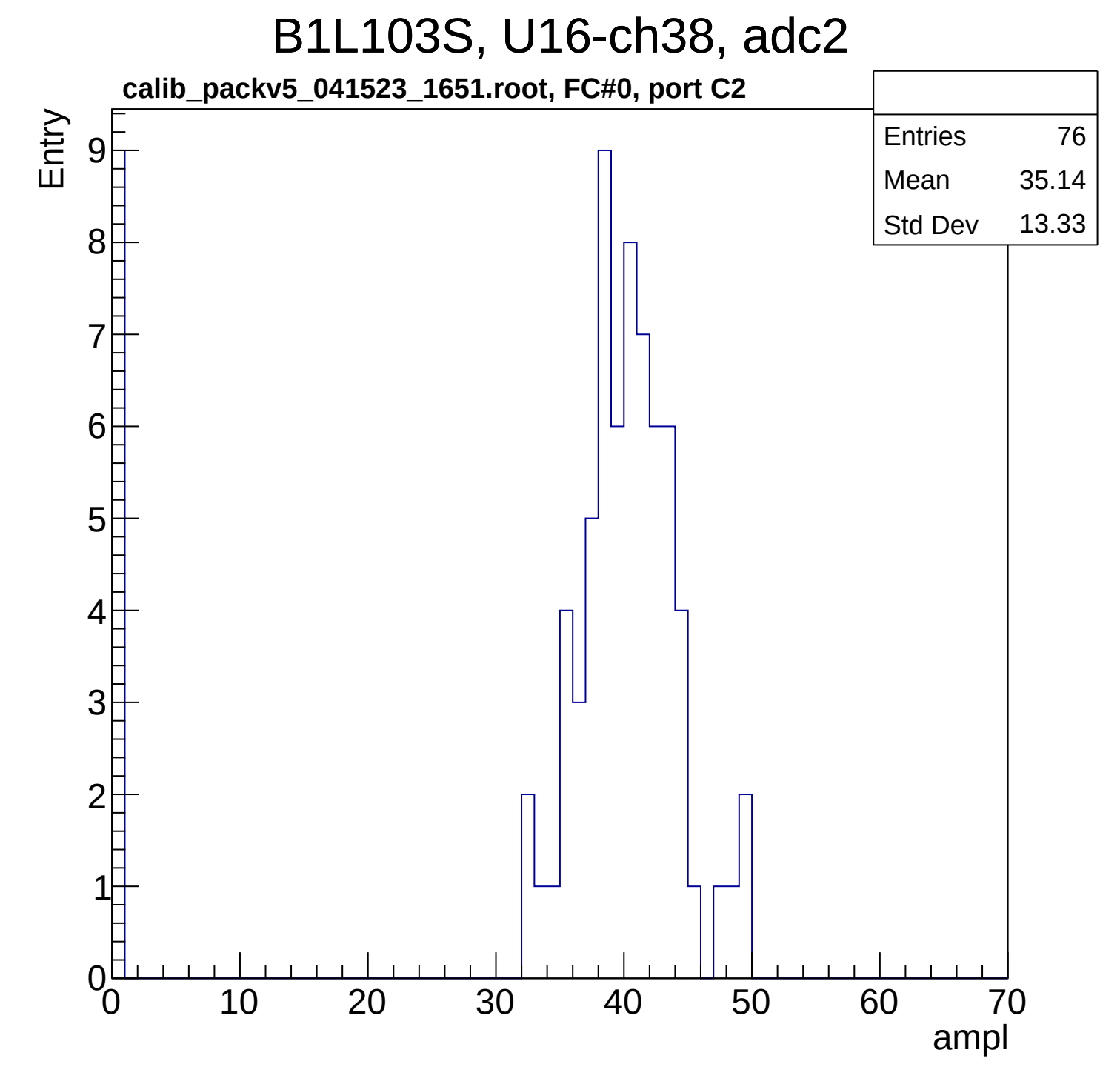
60
70


B1L103S, U16-ch38, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 35.14
Std Dev 13.33
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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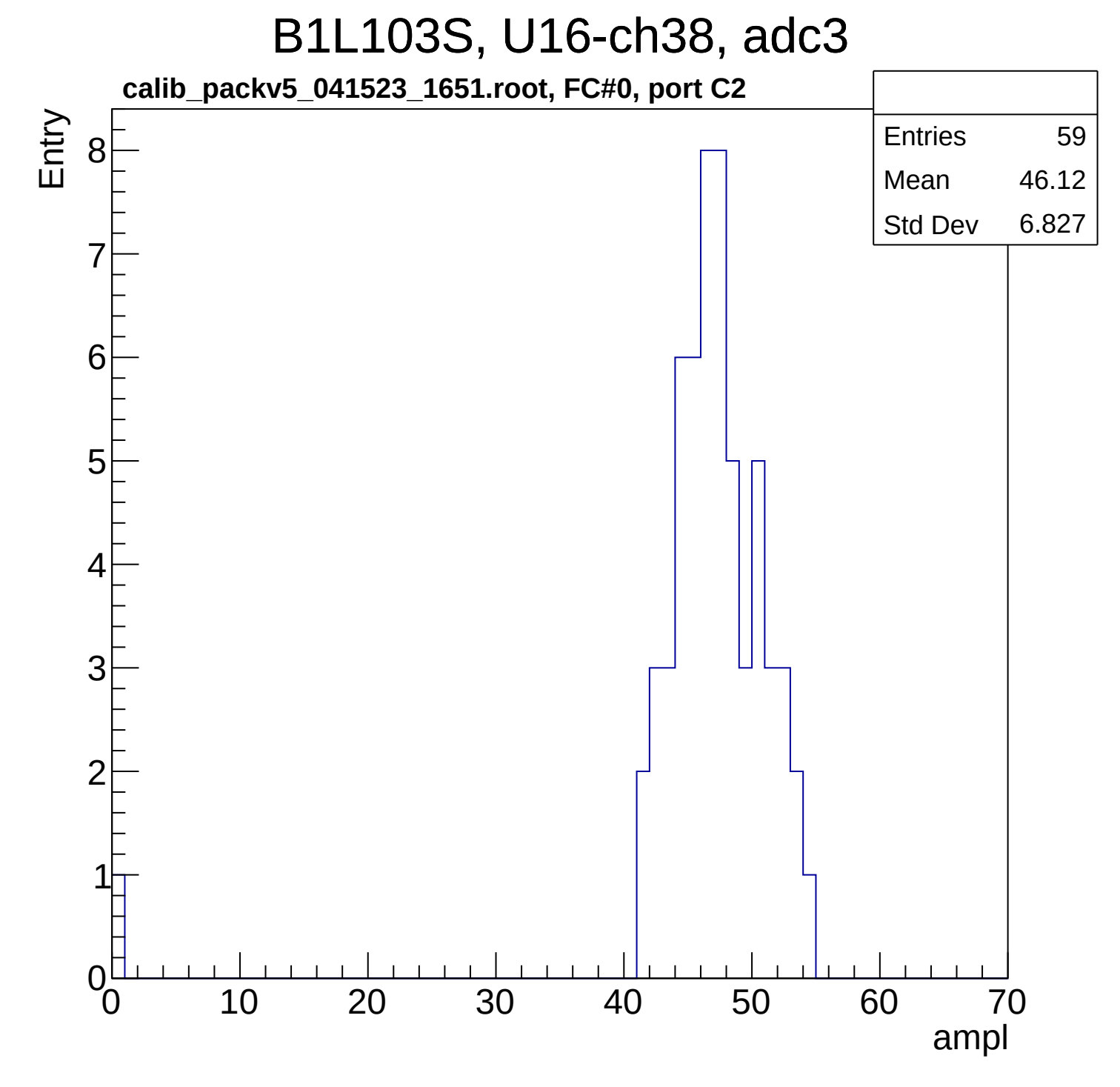
20
30
40
50
60
70


B1L103S, U16-ch38, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 46.12
Std Dev 6.827
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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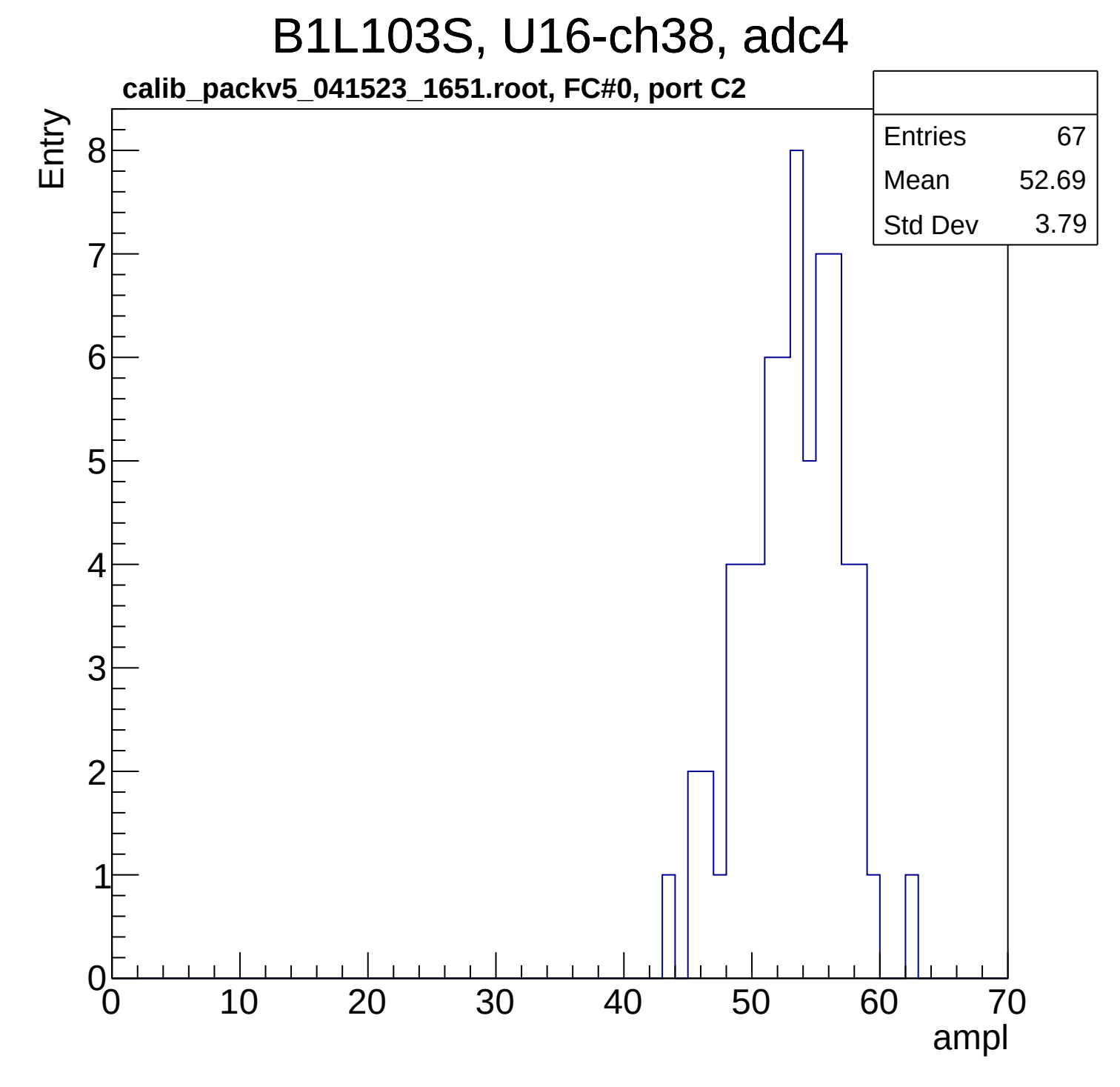
40
50
60
70


B1L103S, U16-ch38, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 52.69
Std Dev 3.79
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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40
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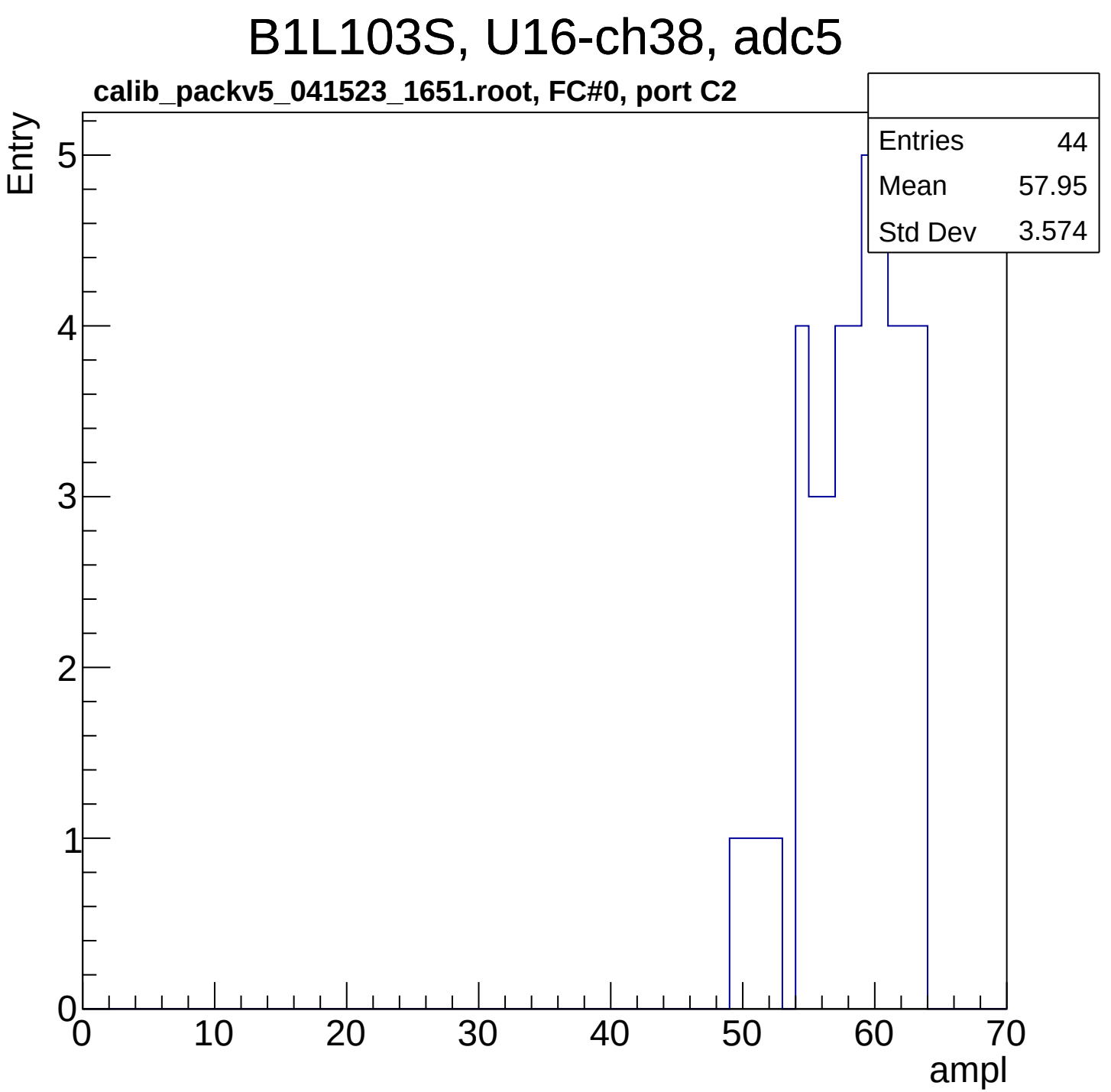
60
70


B1L103S, U16-ch38, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 57.95
Std Dev 3.574
Entry
ampl
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2
3
4
5
0
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20
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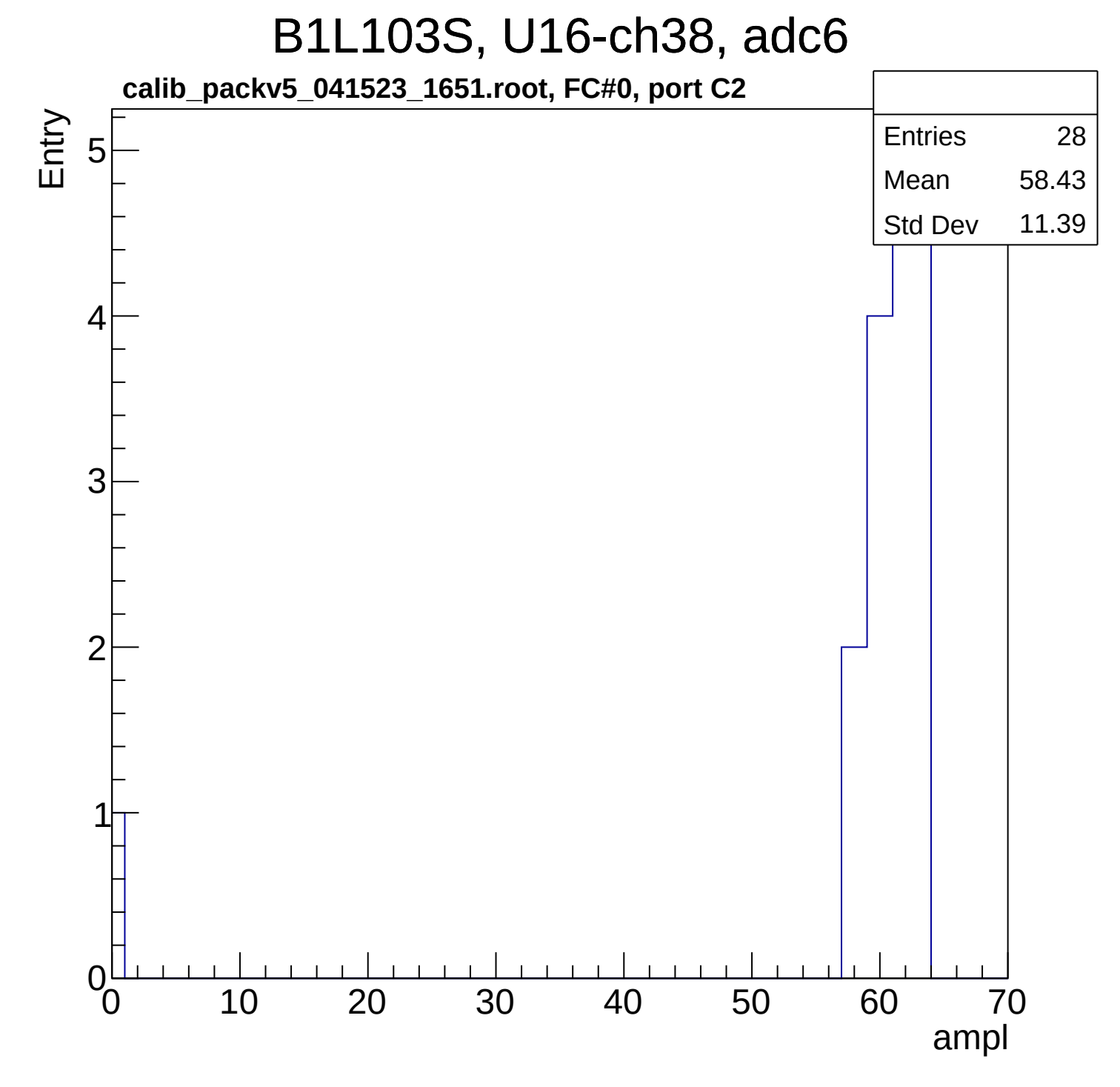
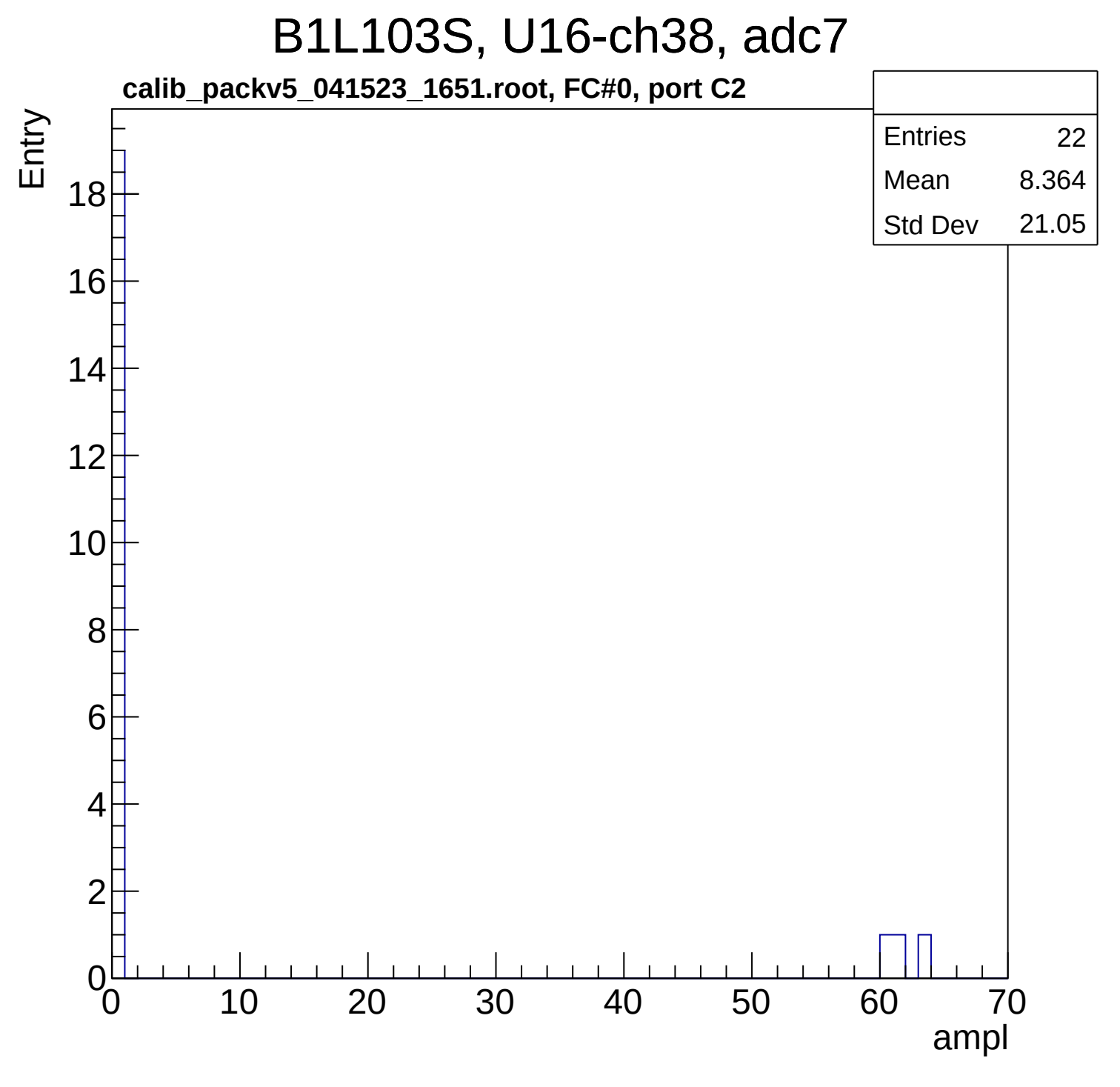
40
50
60
70


B1L103S, U16-ch38, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 58.43
Std Dev 11.39
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch38, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.364
Std Dev 21.05
Entry
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6
8
10
12
14
16
18
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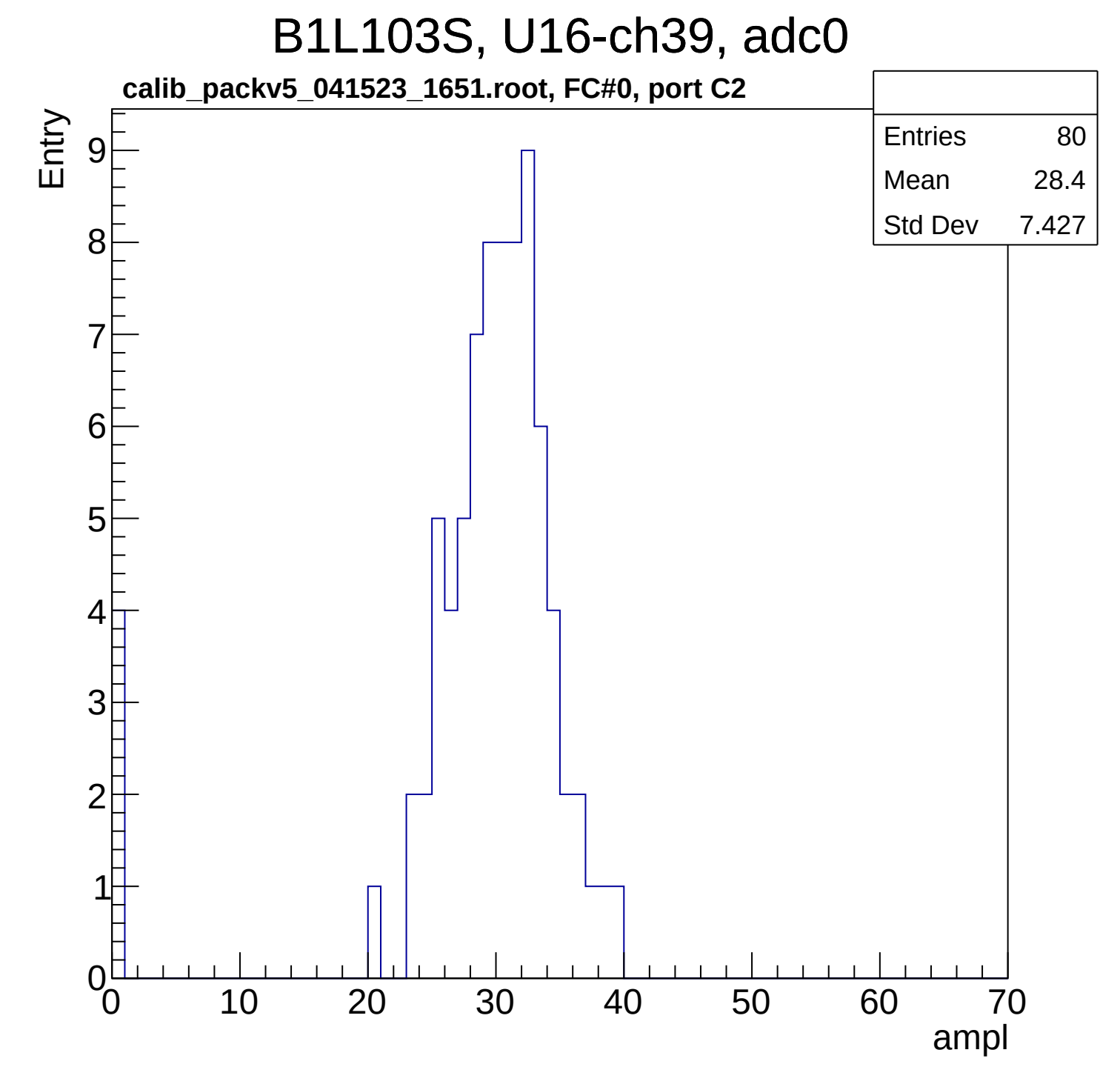
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch39, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 28.4
Std Dev 7.427
Entry
ampl
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3
4
5
6
7
8
9
0
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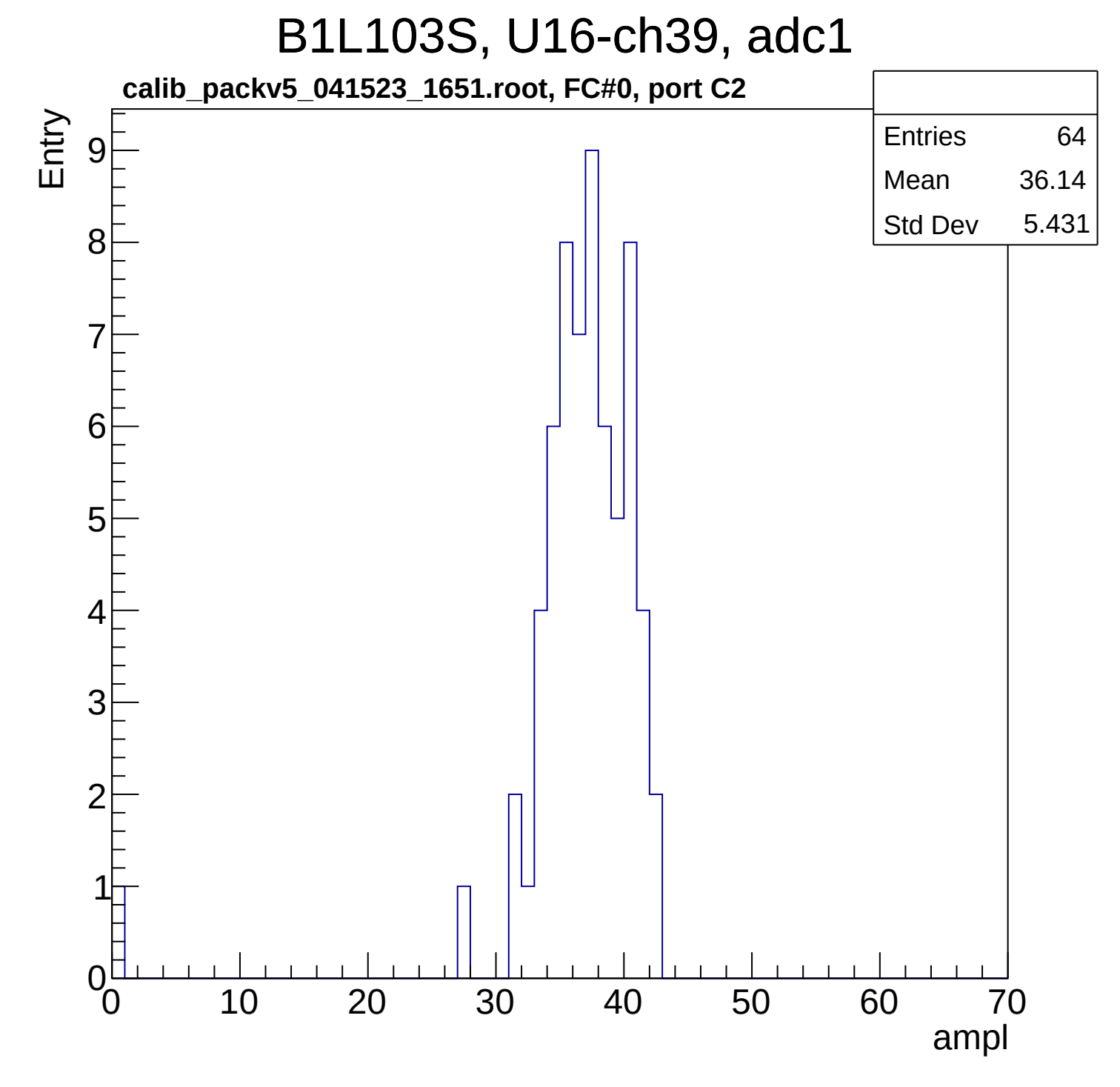
B1L103S, U16-ch39, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 36.14
Std Dev 5.431
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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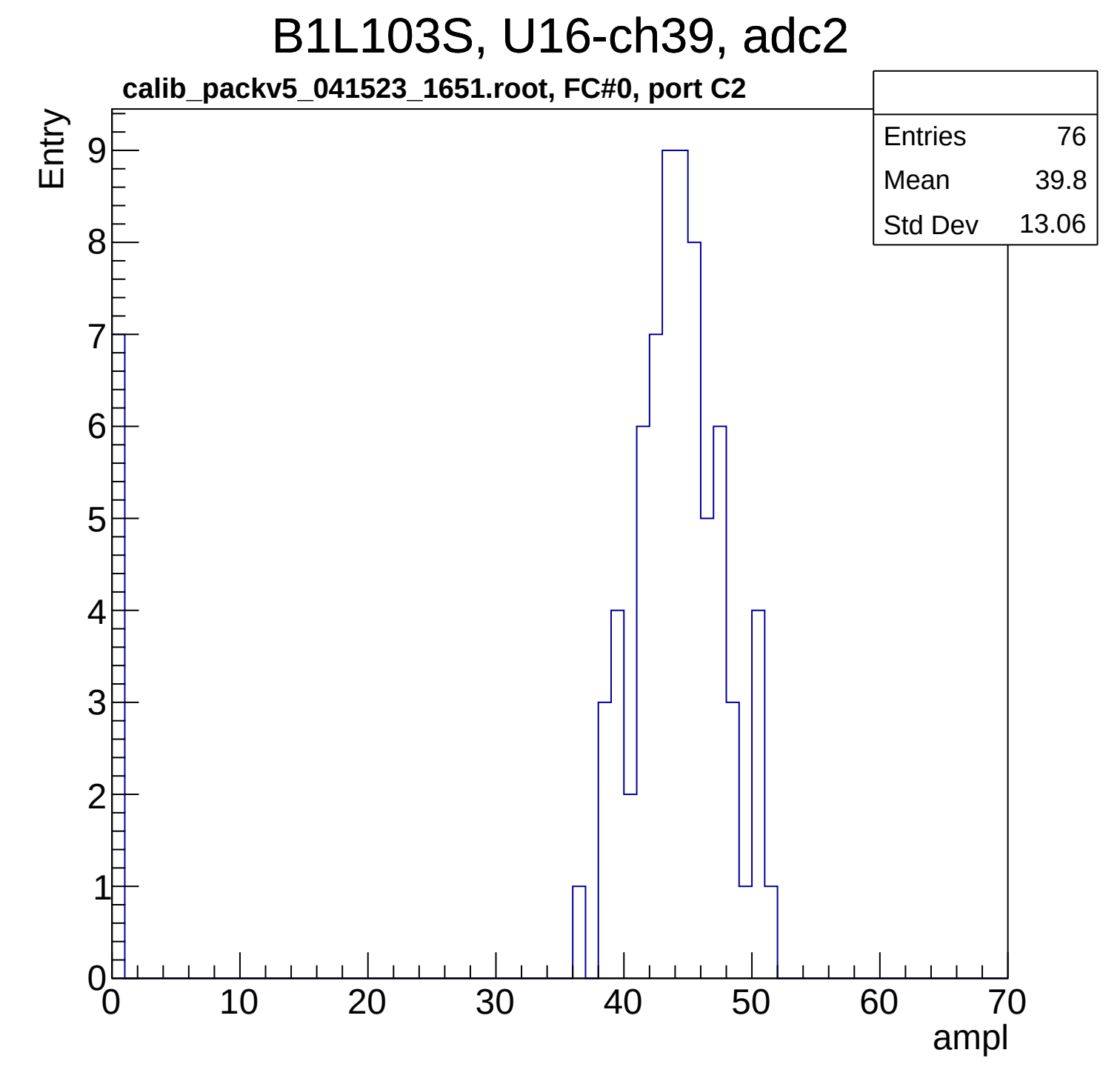
B1L103S, U16-ch39, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 39.8
Std Dev 13.06
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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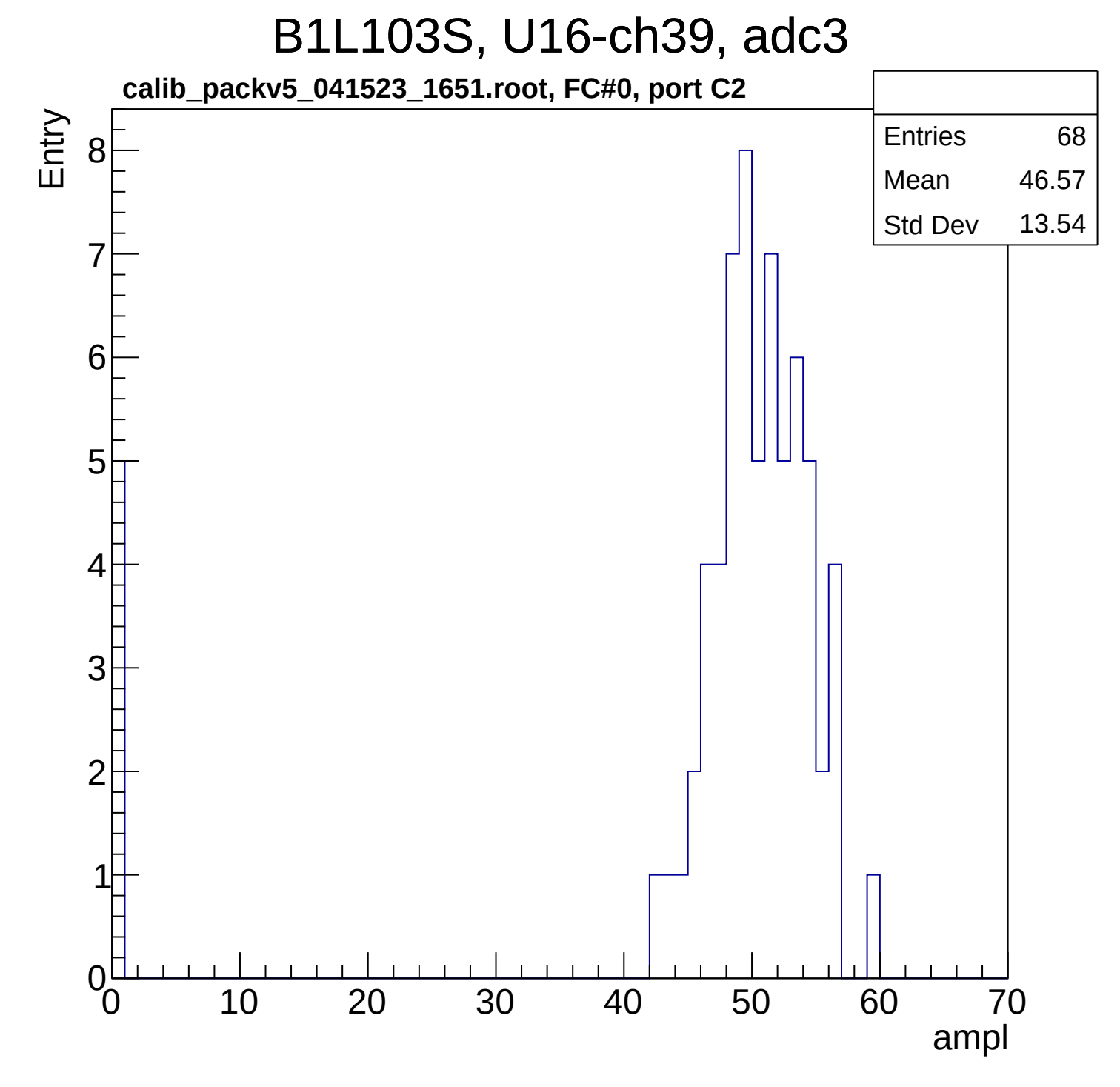
B1L103S, U16-ch39, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 46.57
Std Dev 13.54
Entry
ampl
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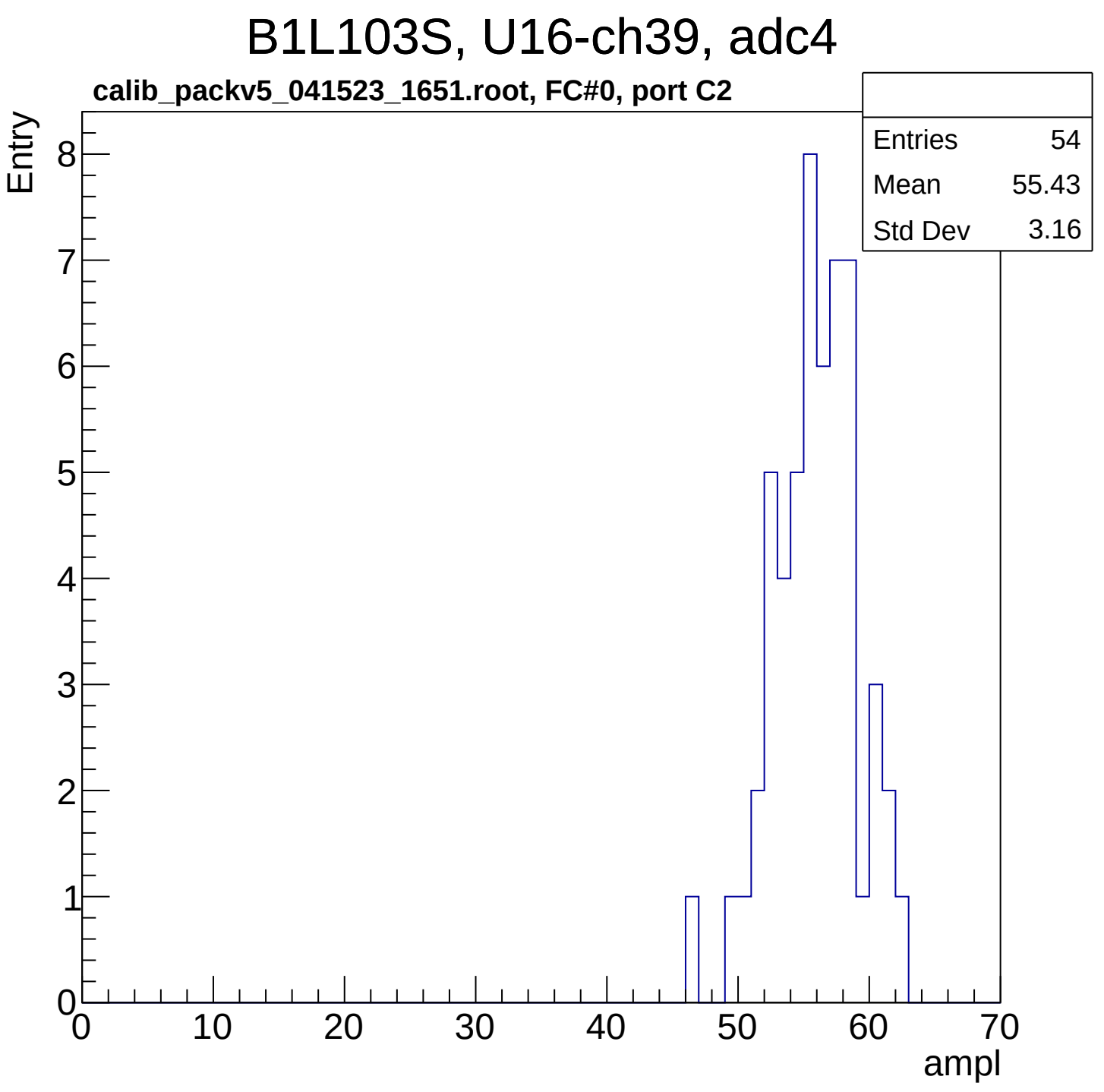
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch39, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 55.43
Std Dev 3.16
Entry
ampl
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2
3
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5
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7
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0
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40
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60
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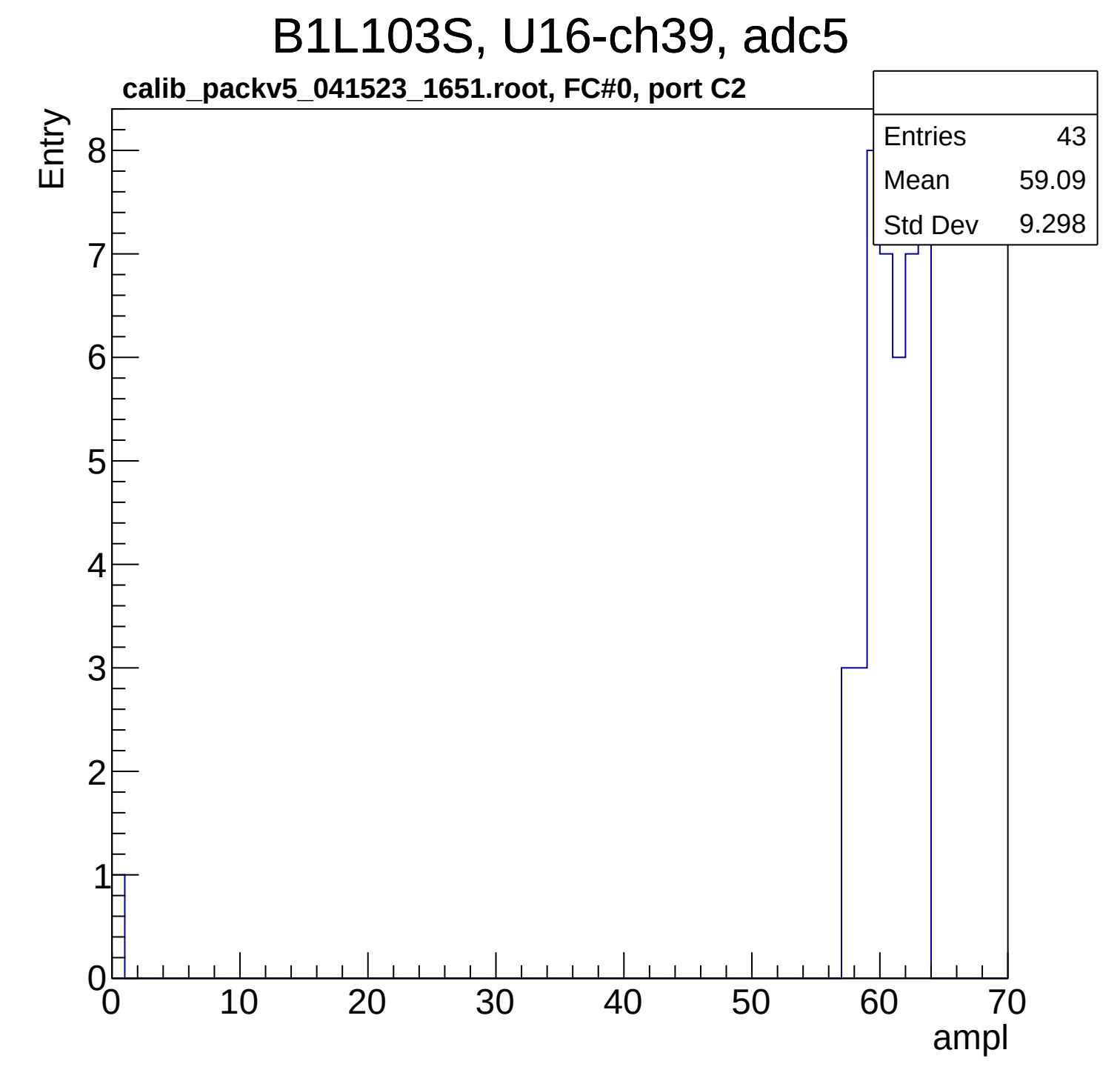
B1L103S, U16-ch39, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 59.09
Std Dev 9.298
Entry
ampl
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2
3
4
5
6
7
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20
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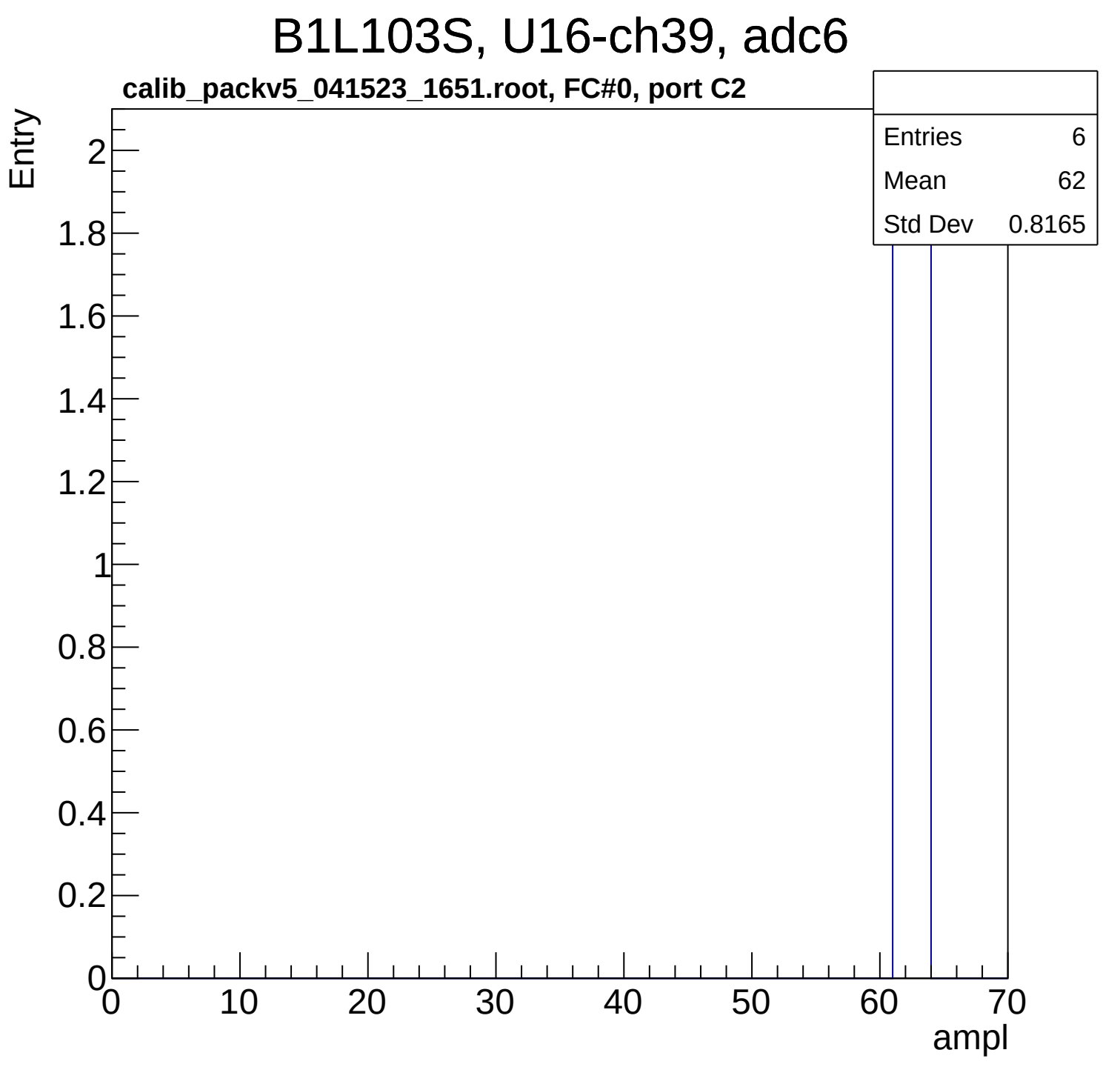
40
50
60
70


B1L103S, U16-ch39, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62
Std Dev 0.8165
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
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40
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60
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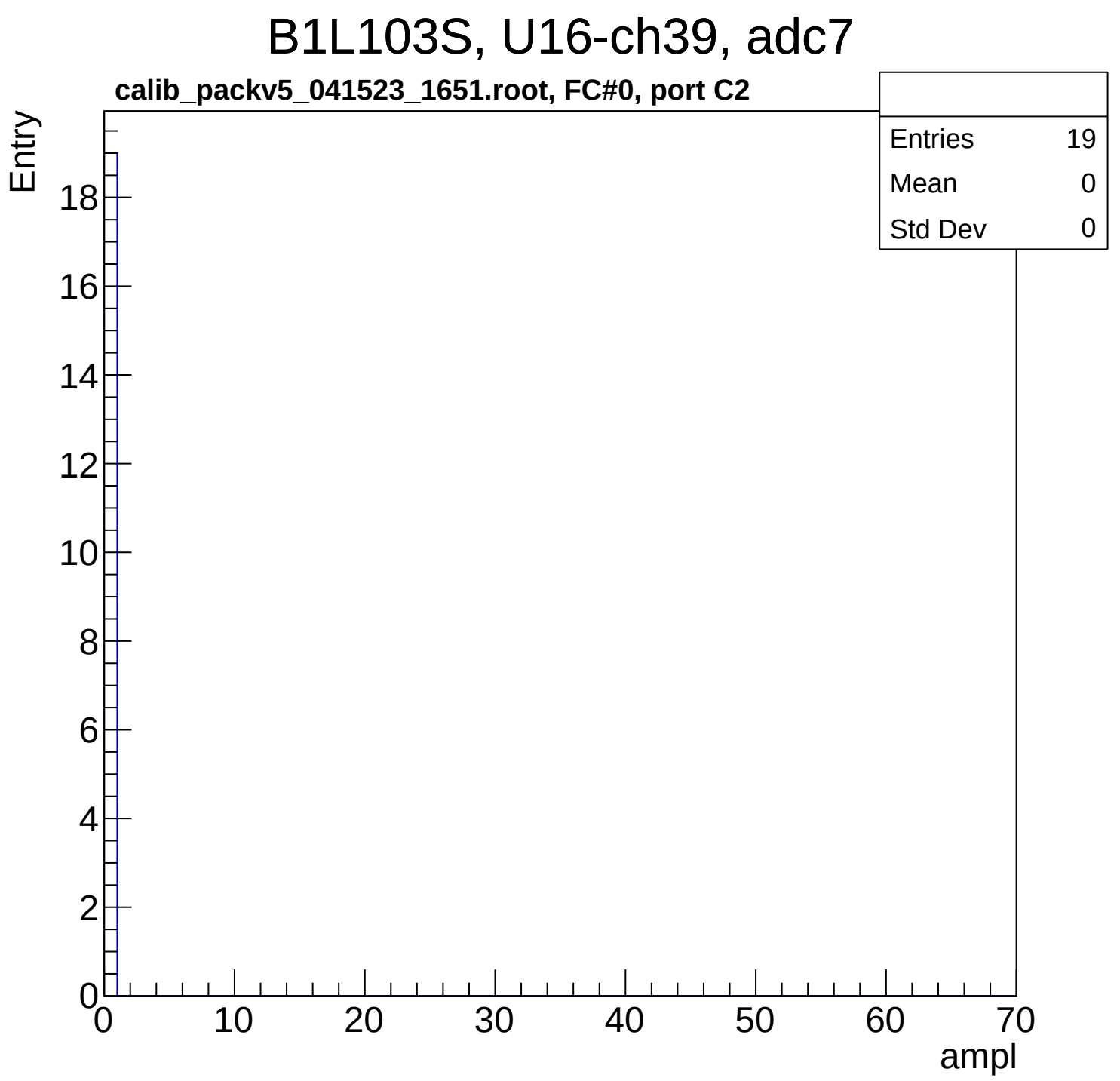
B1L103S, U16-ch39, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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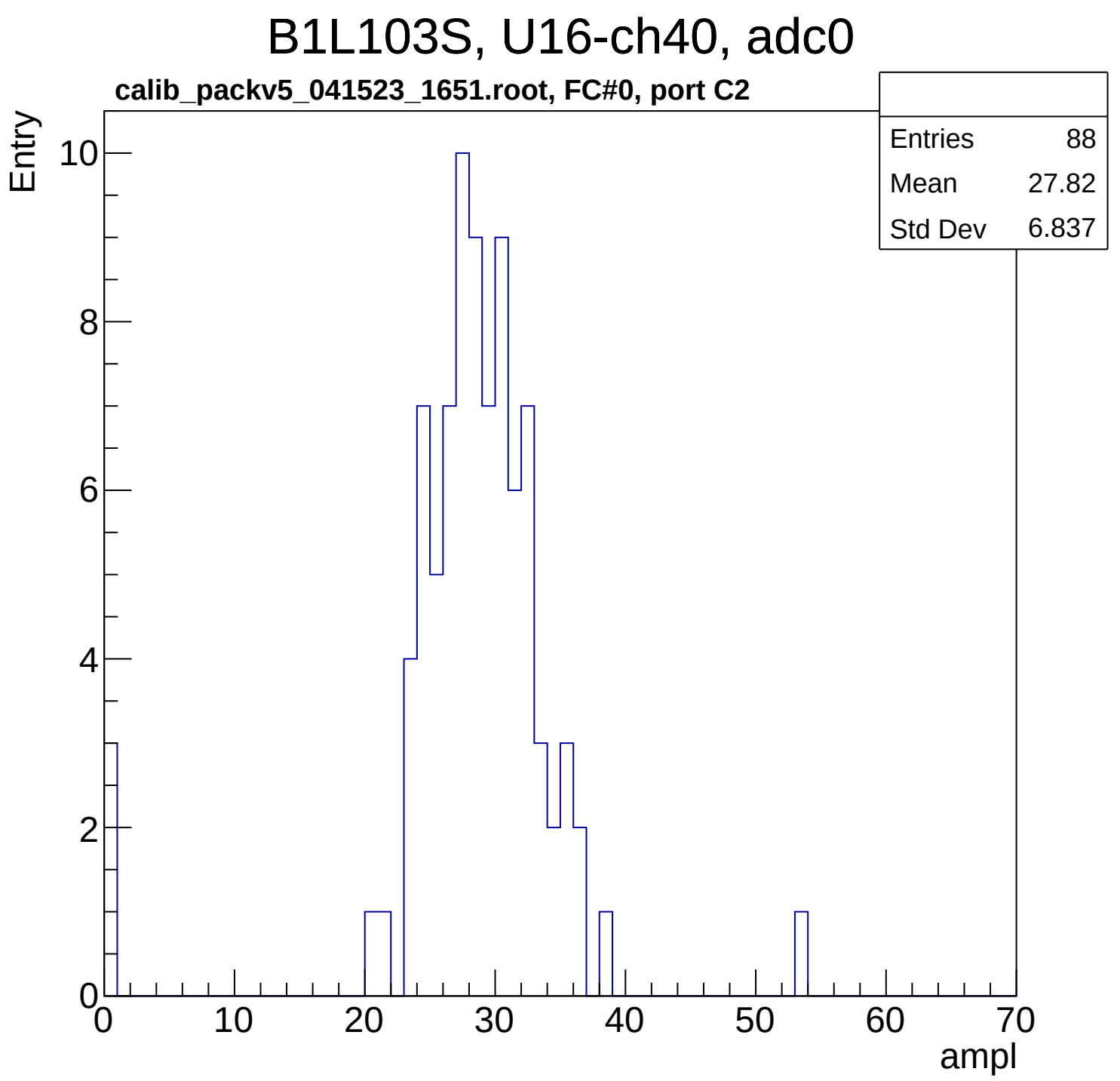
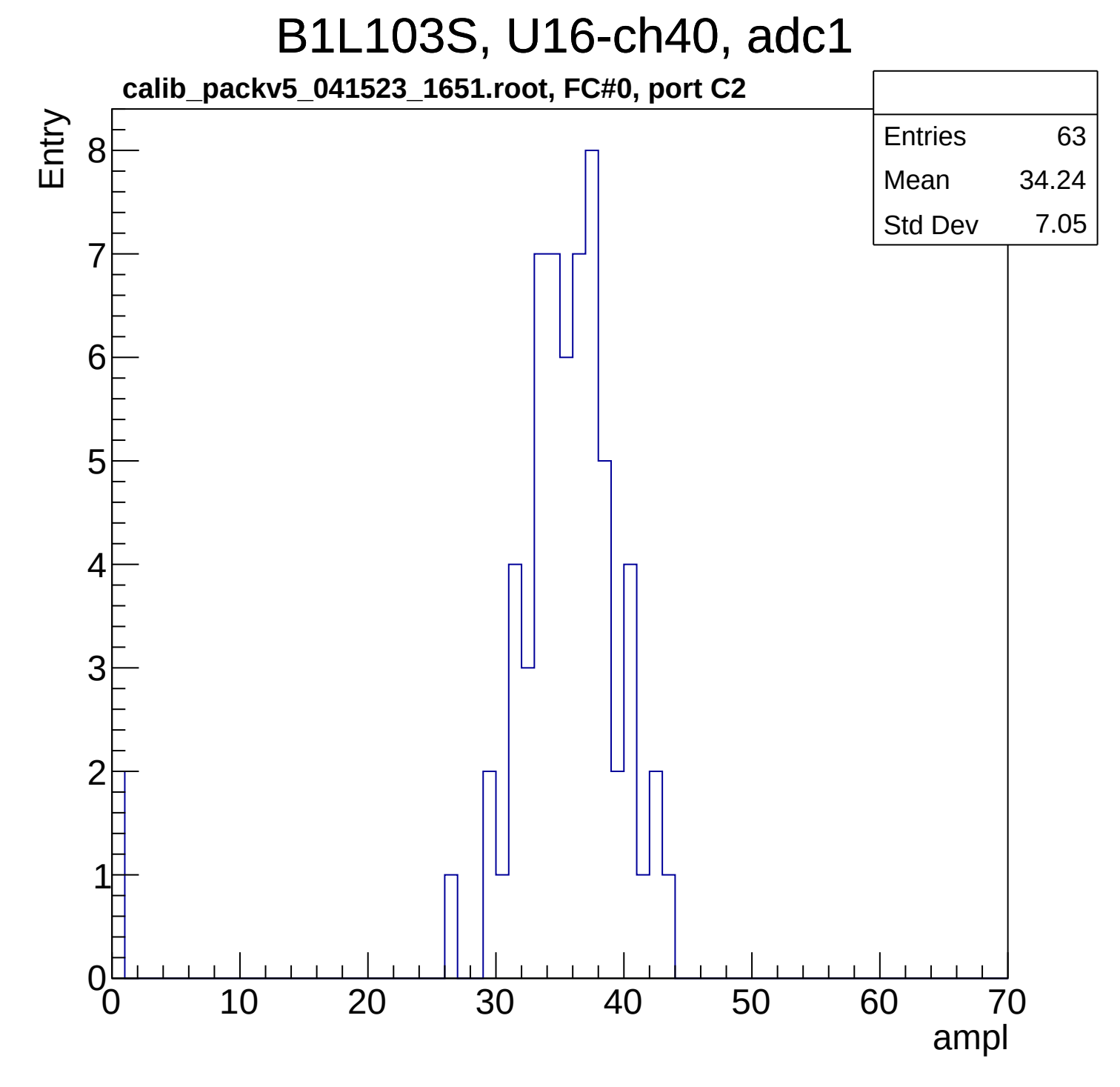
50
60
70
ampl


B1L103S, U16-ch40, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 27.82
Std Dev 6.837
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch40, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 34.24
Std Dev 7.05
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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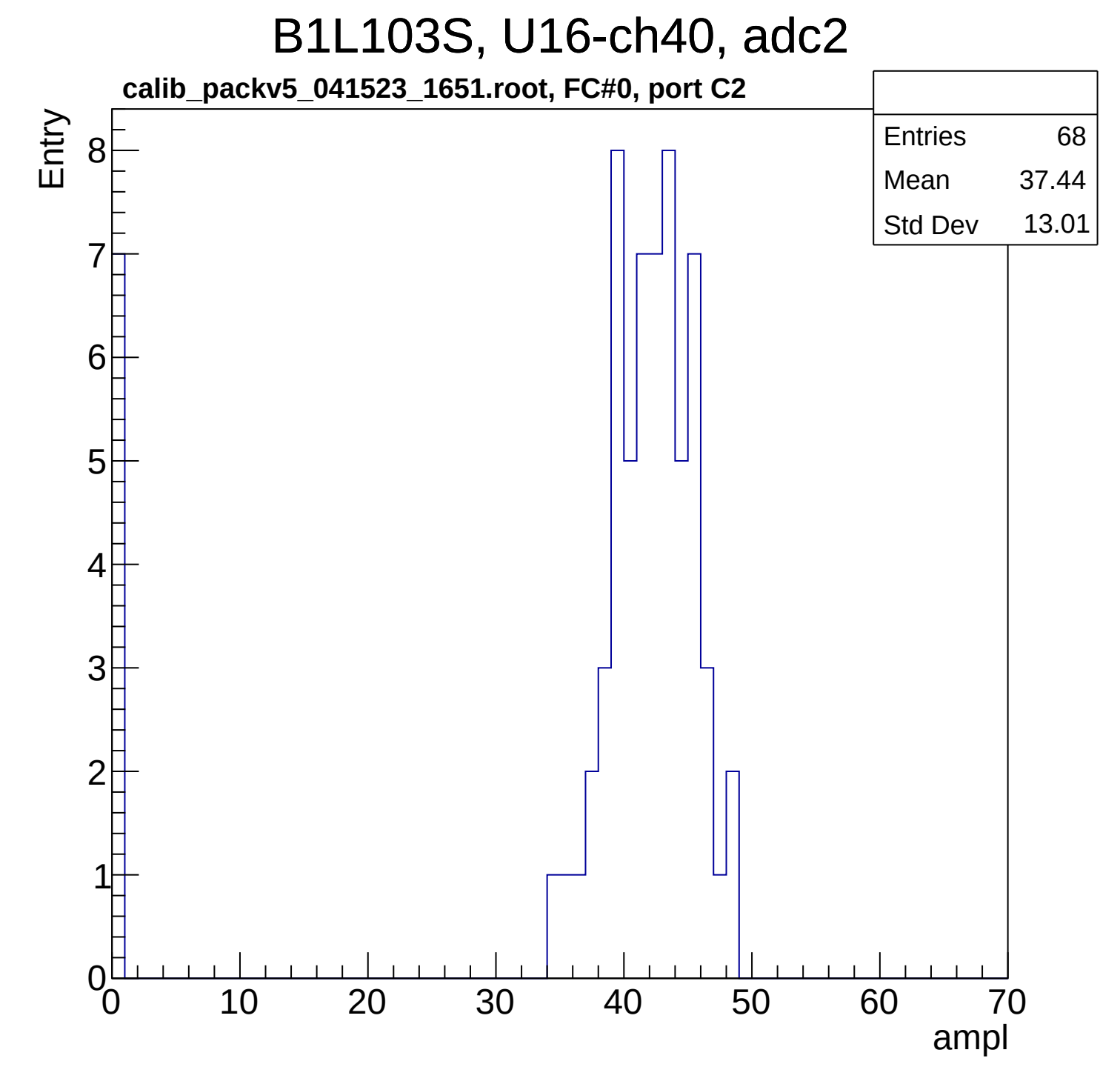
B1L103S, U16-ch40, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 37.44
Std Dev 13.01
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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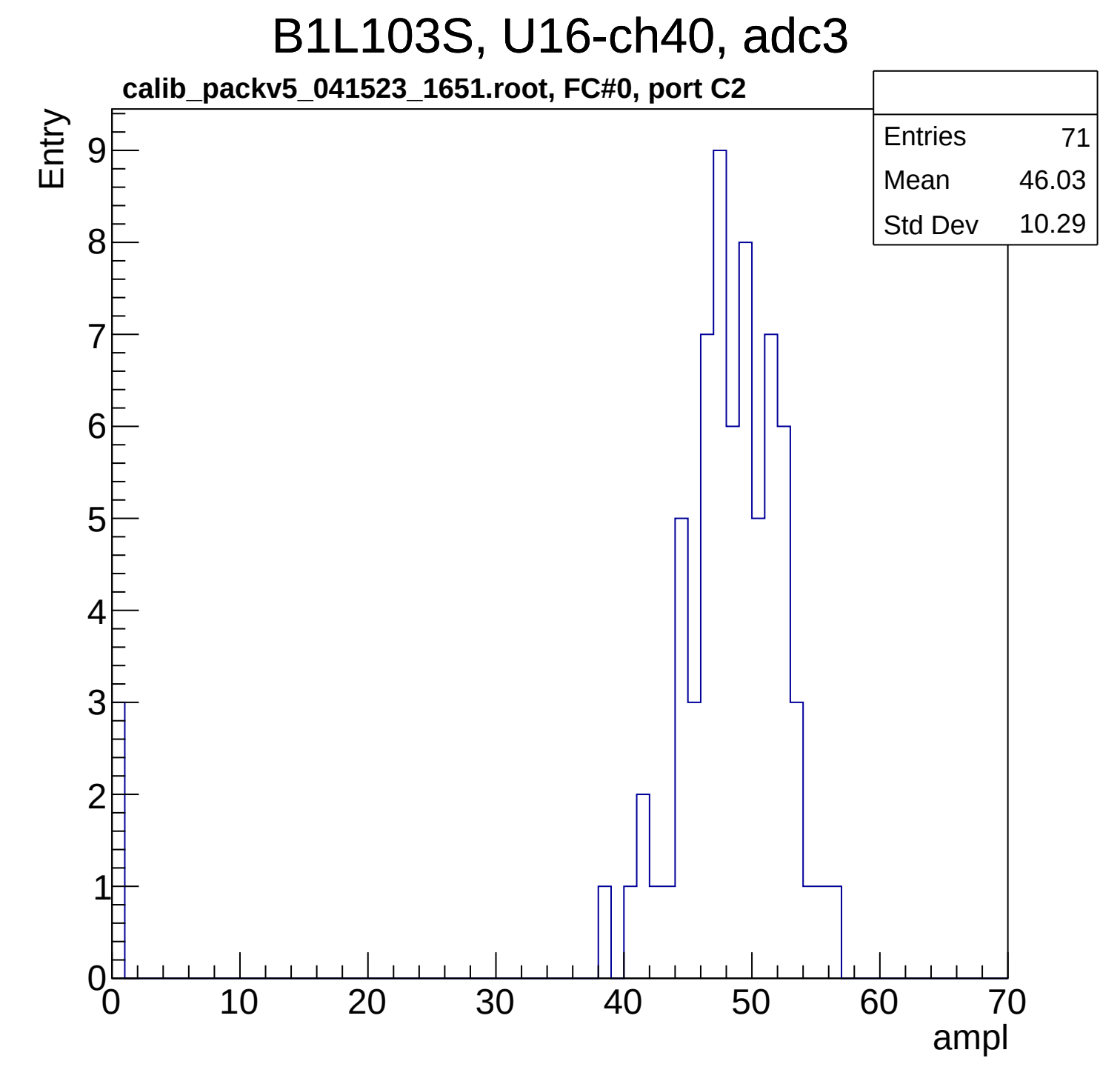
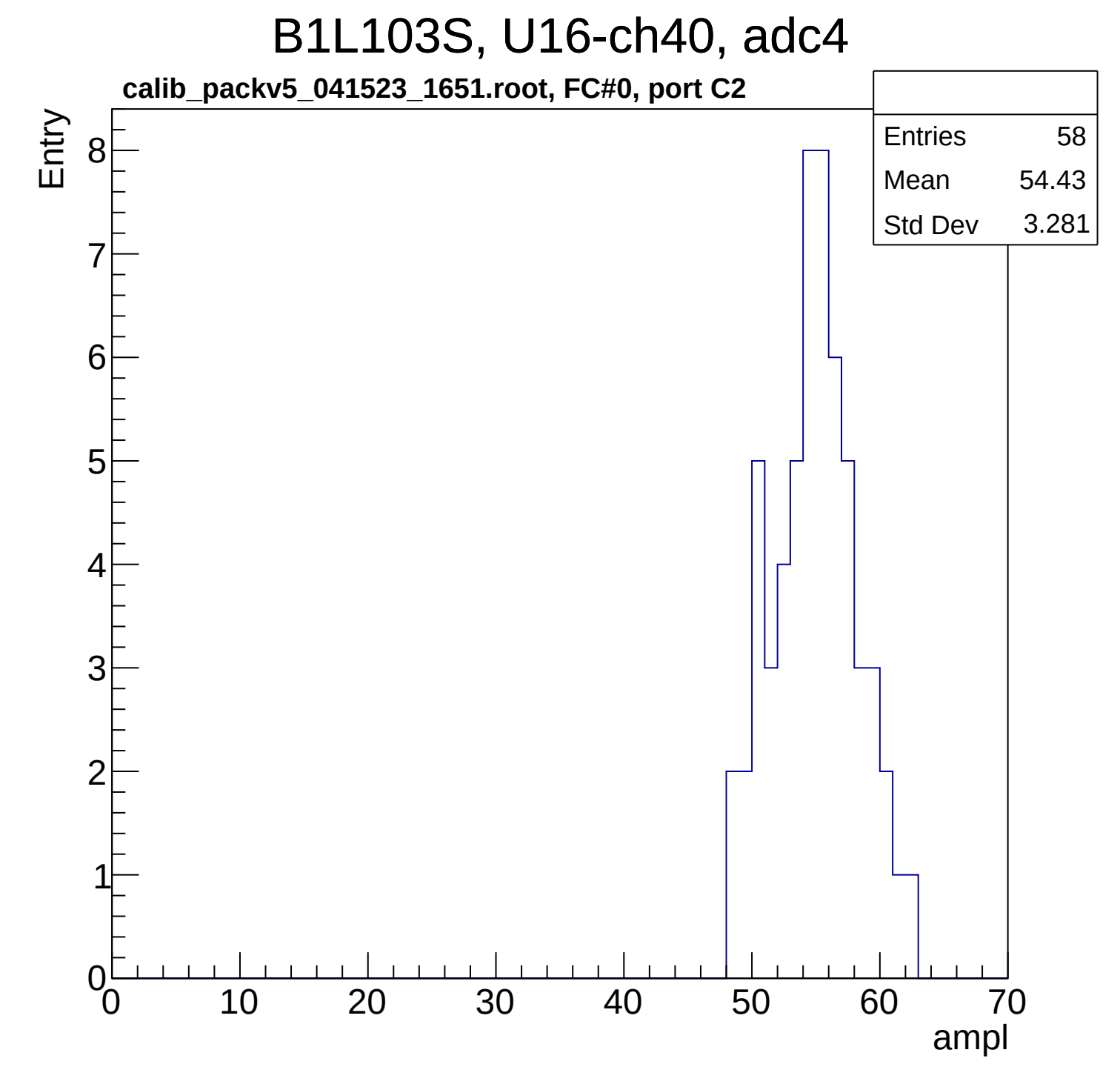

B1L103S, U16-ch40, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 46.03
Std Dev 10.29
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch40, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 54.43
Std Dev 3.281
Entry
ampl
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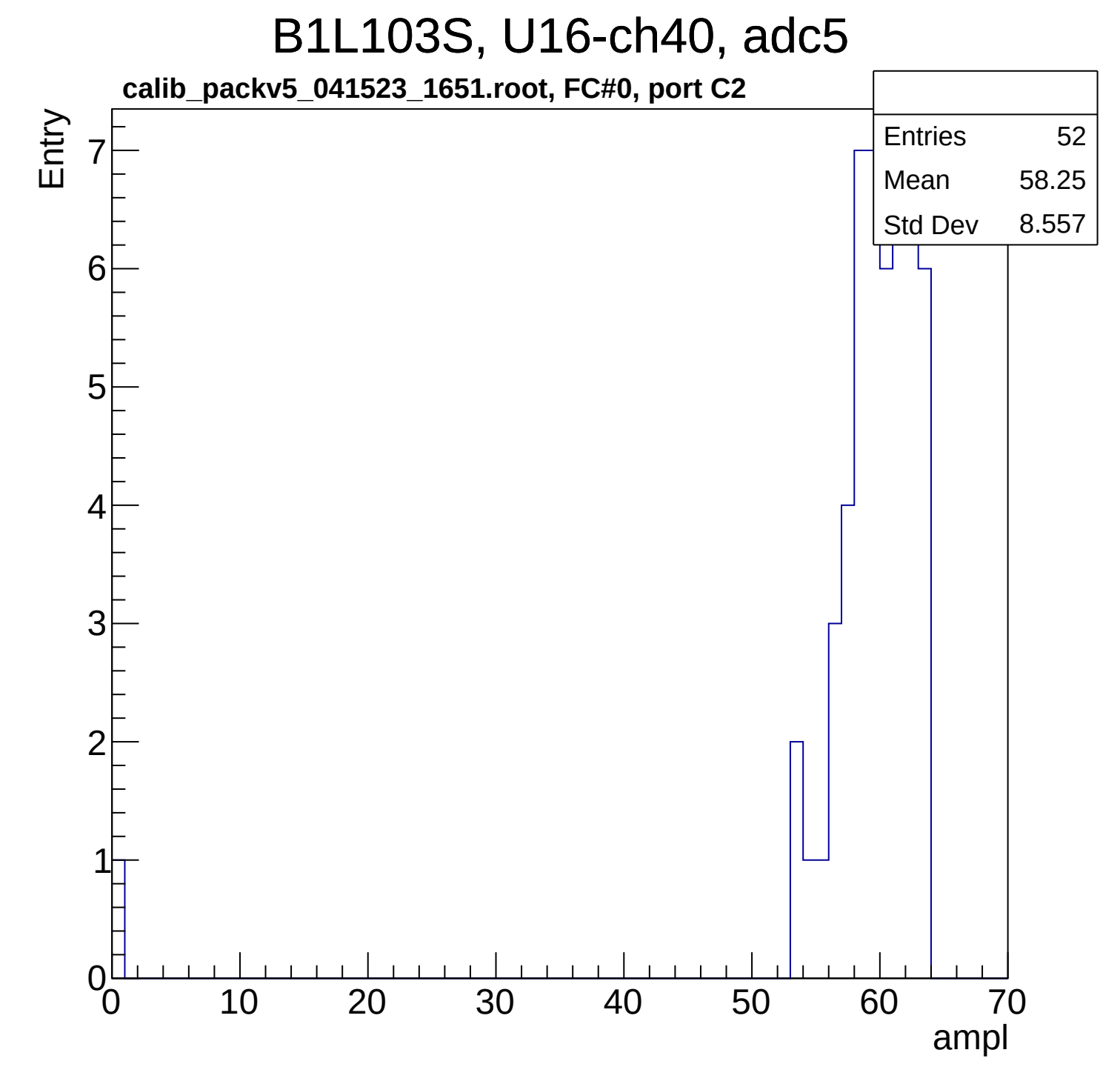
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch40, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.25
Std Dev 8.557
Entry
ampl
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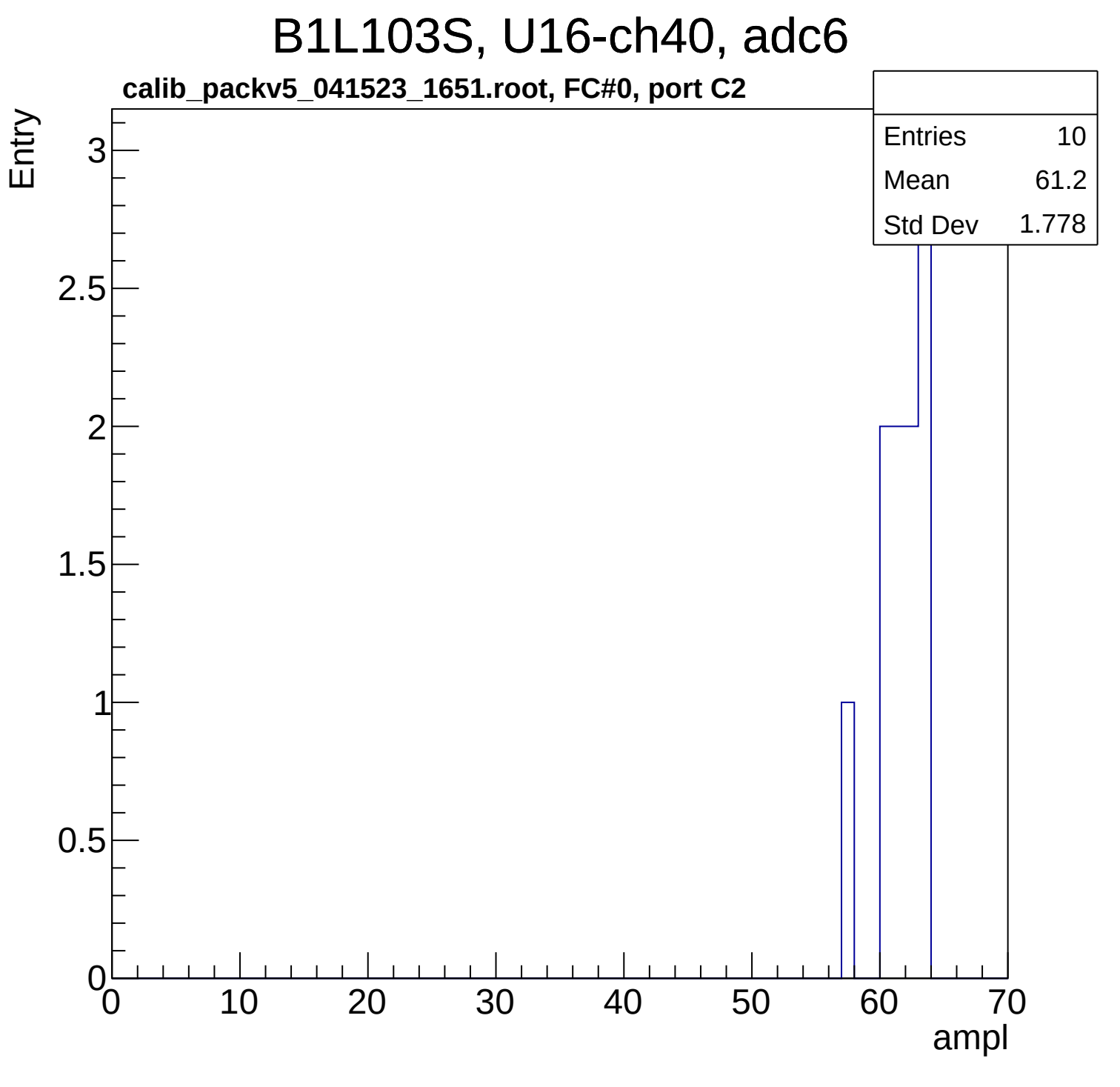
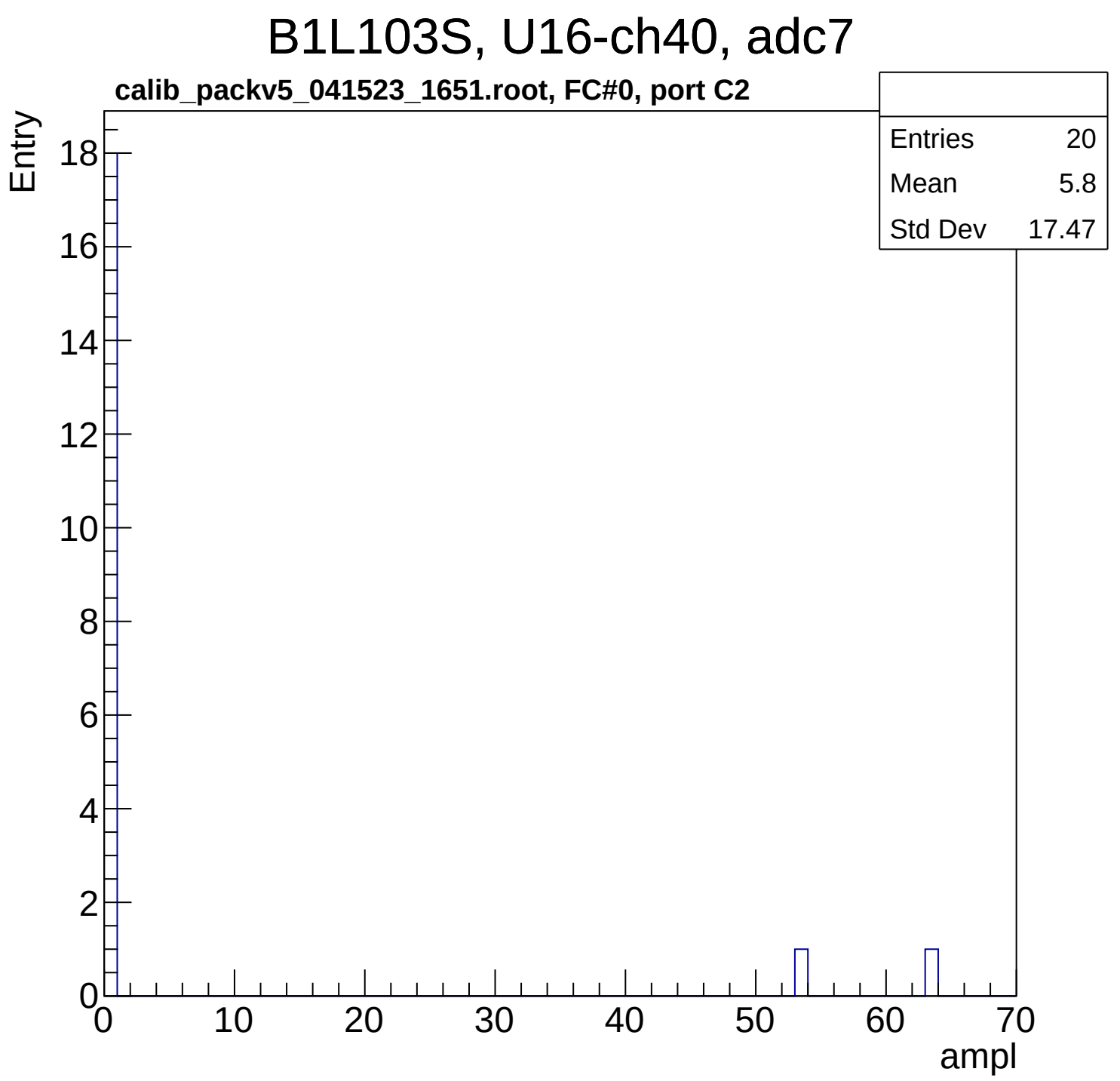
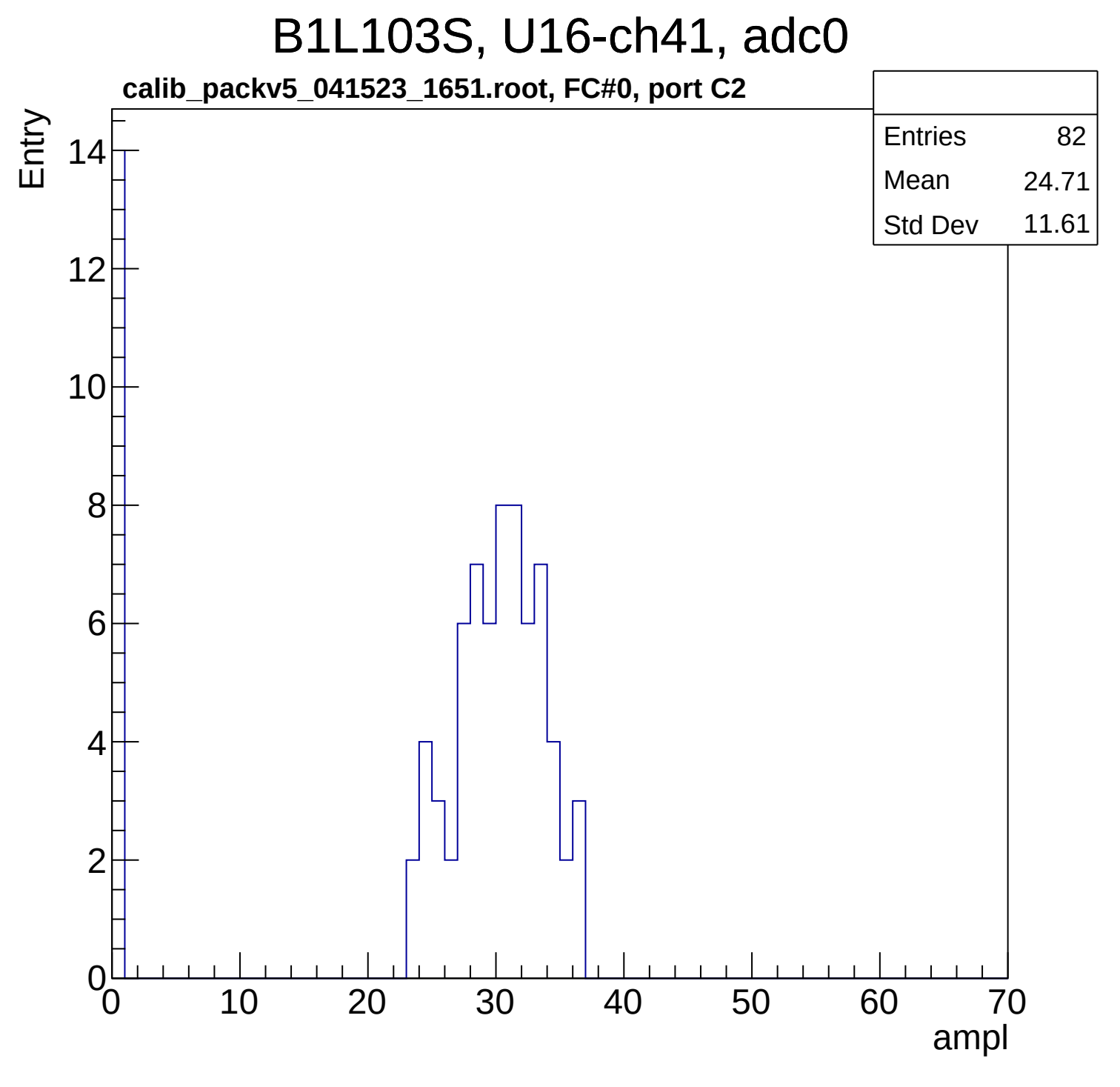
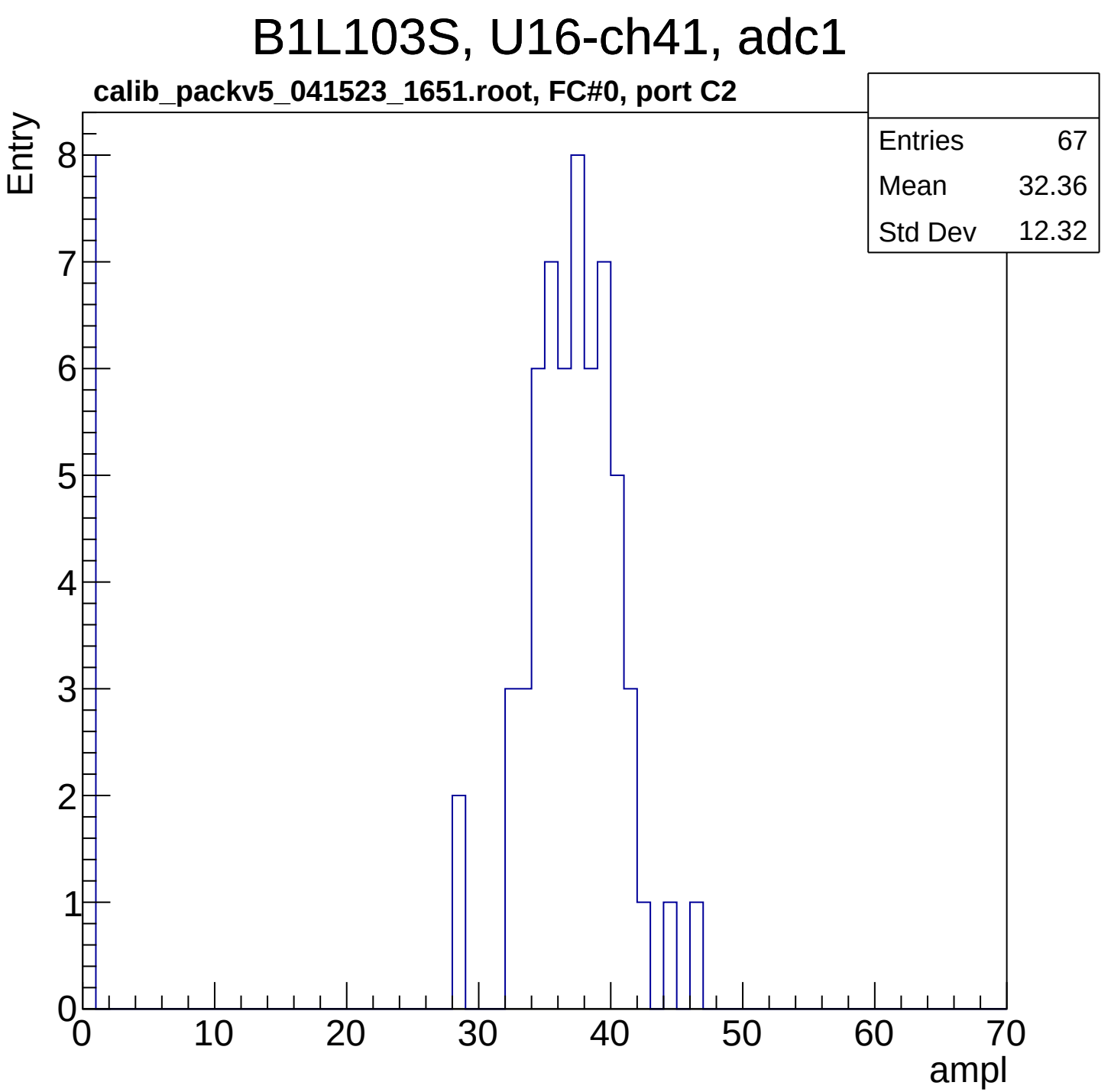
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch40, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.2
Std Dev 1.778
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U16-ch40, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 5.8
Std Dev 17.47
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch41, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 24.71
Std Dev 11.61
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U16-ch41, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 32.36
Std Dev 12.32
Entry
ampl
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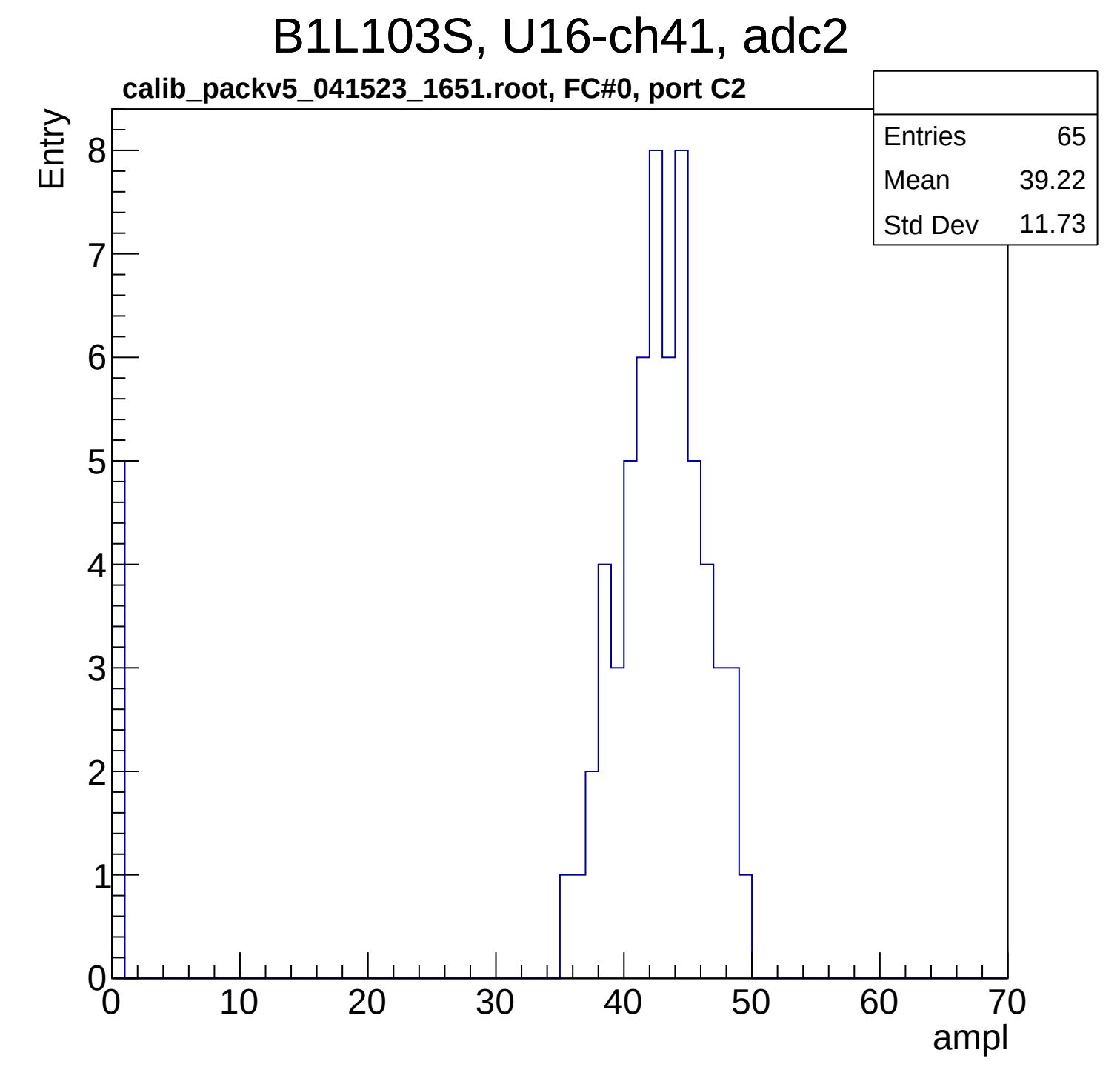
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch41, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 39.22
Std Dev 11.73
Entry
ampl
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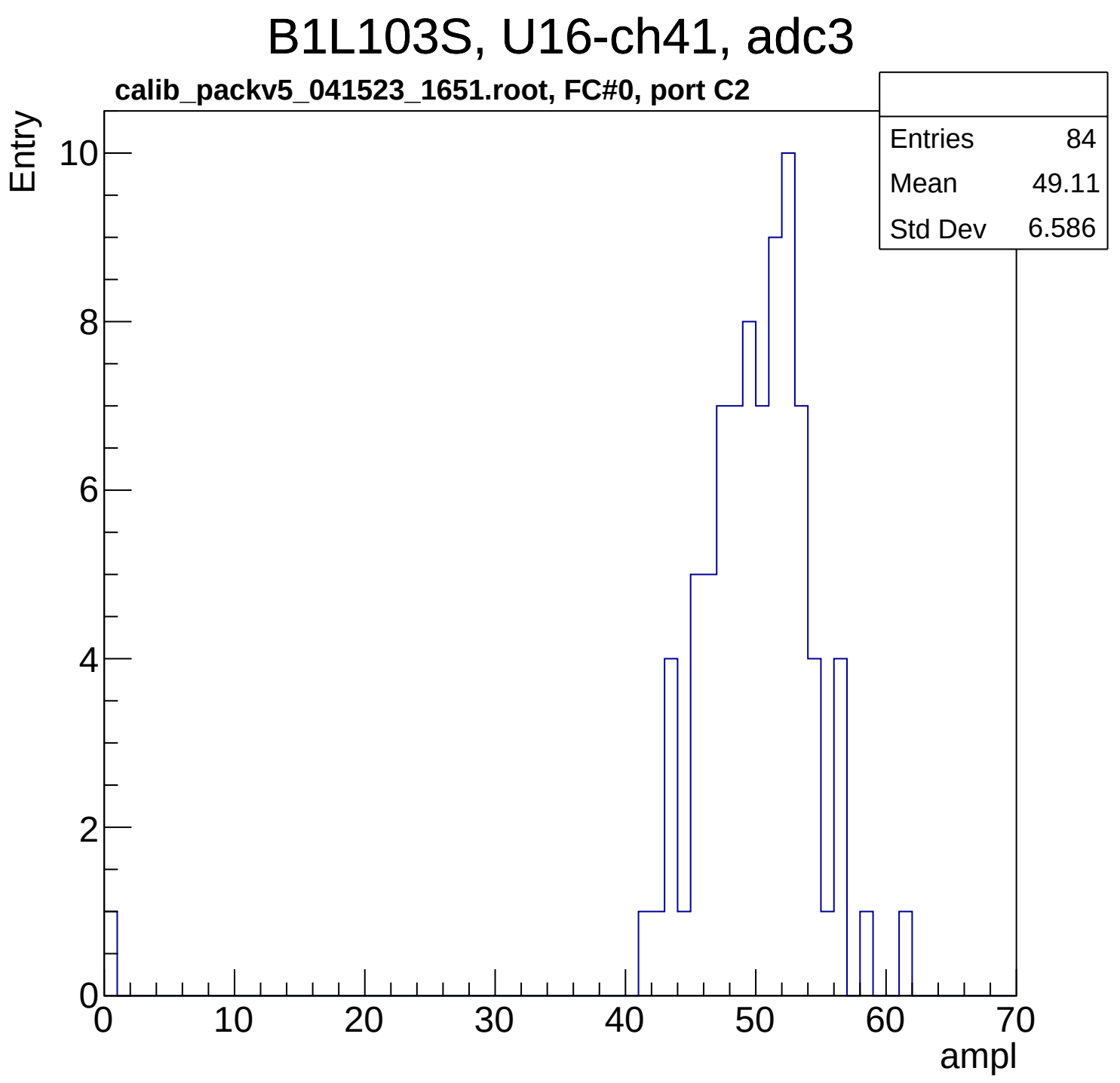
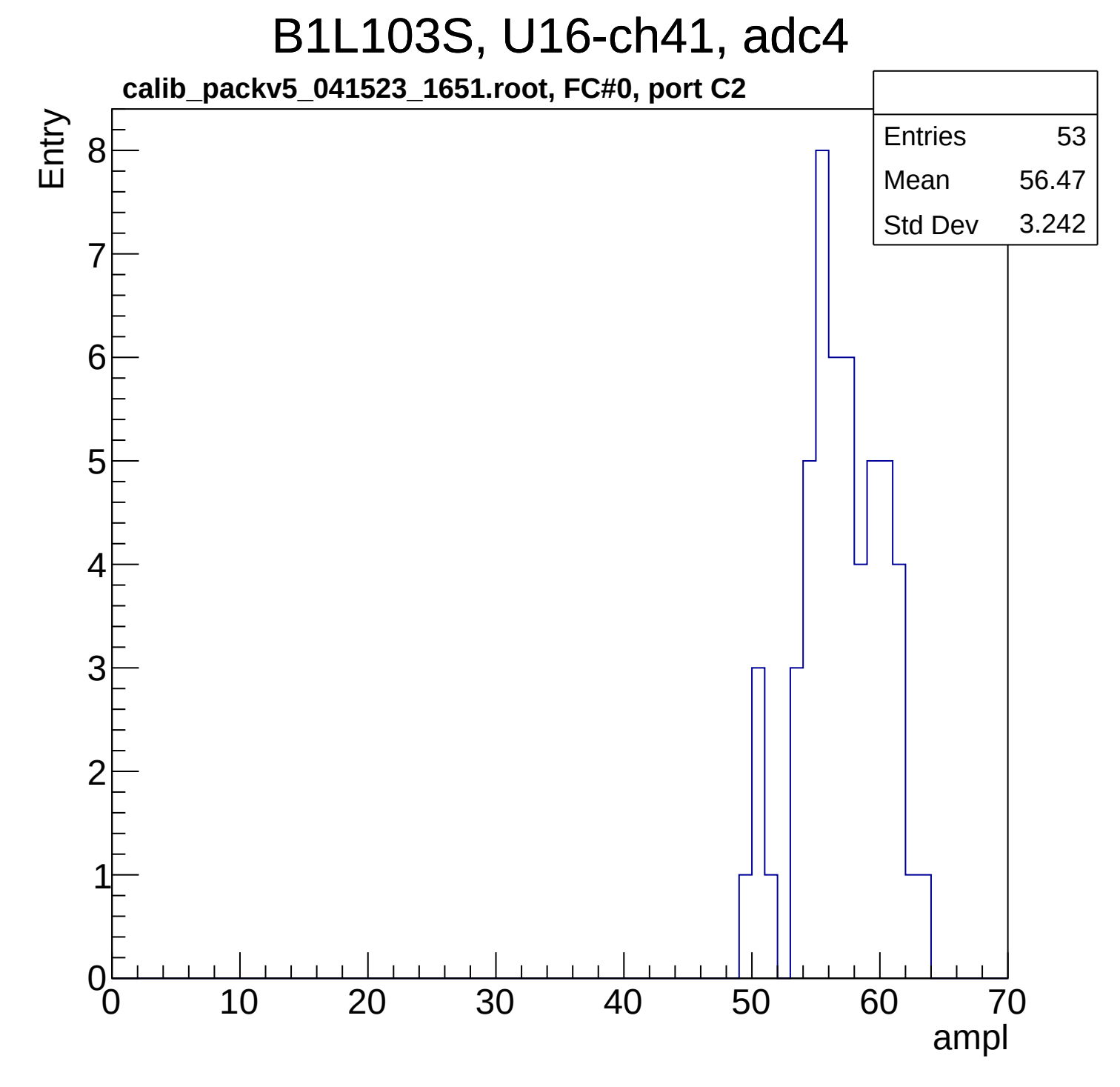
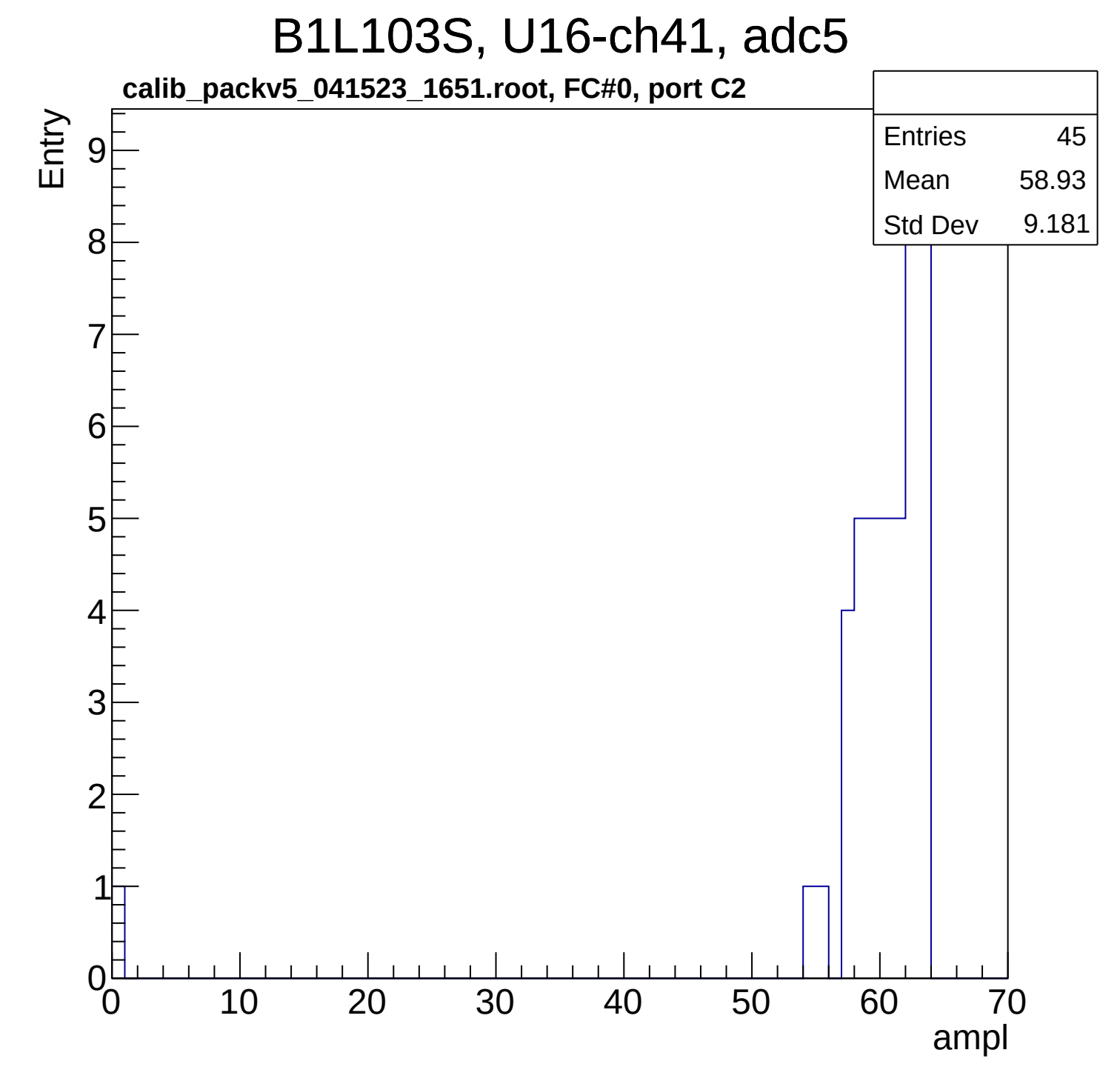
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch41, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 49.11
Std Dev 6.586
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch41, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 56.47
Std Dev 3.242
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch41, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.93
Std Dev 9.181
Entry
ampl
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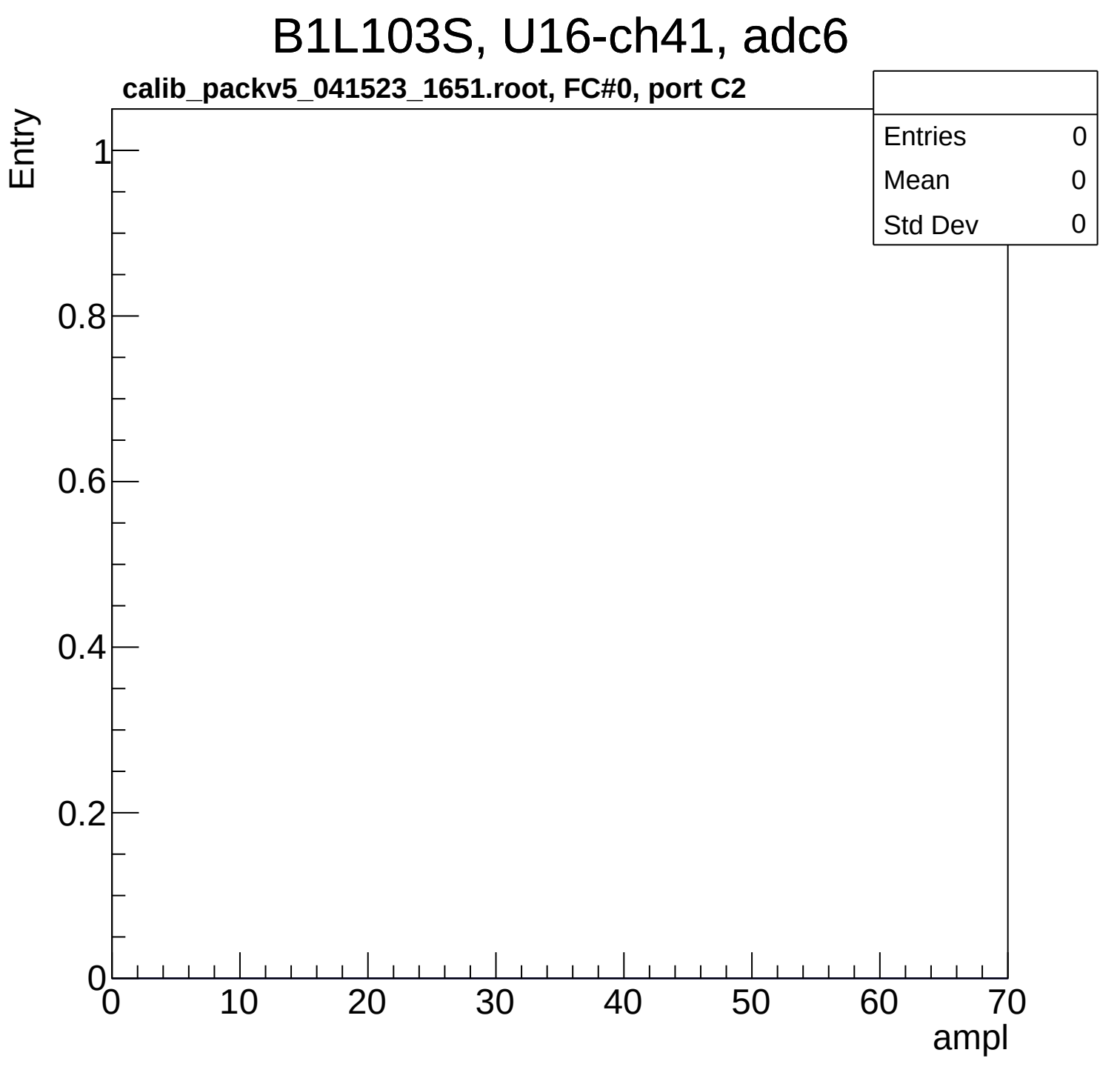
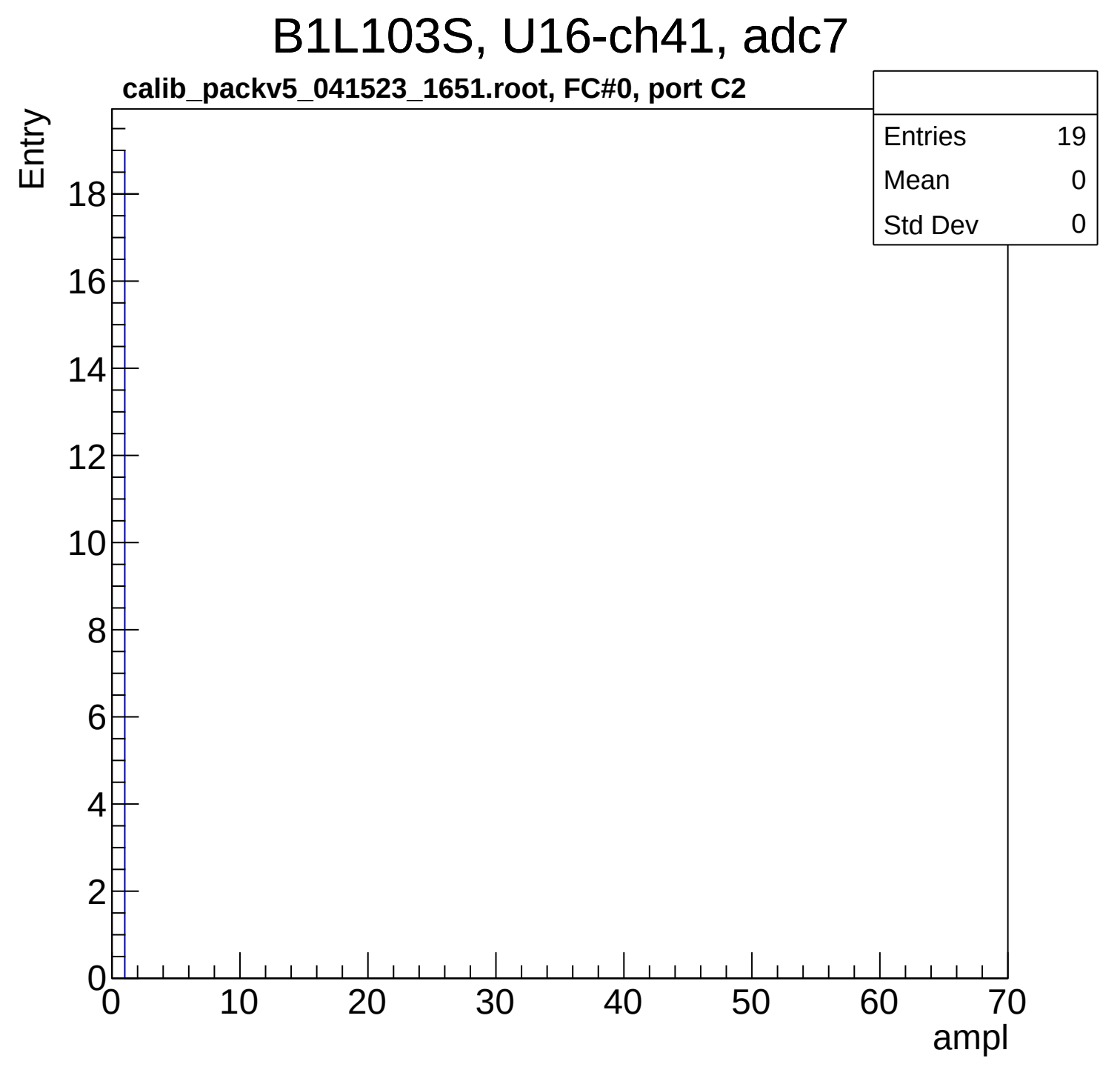
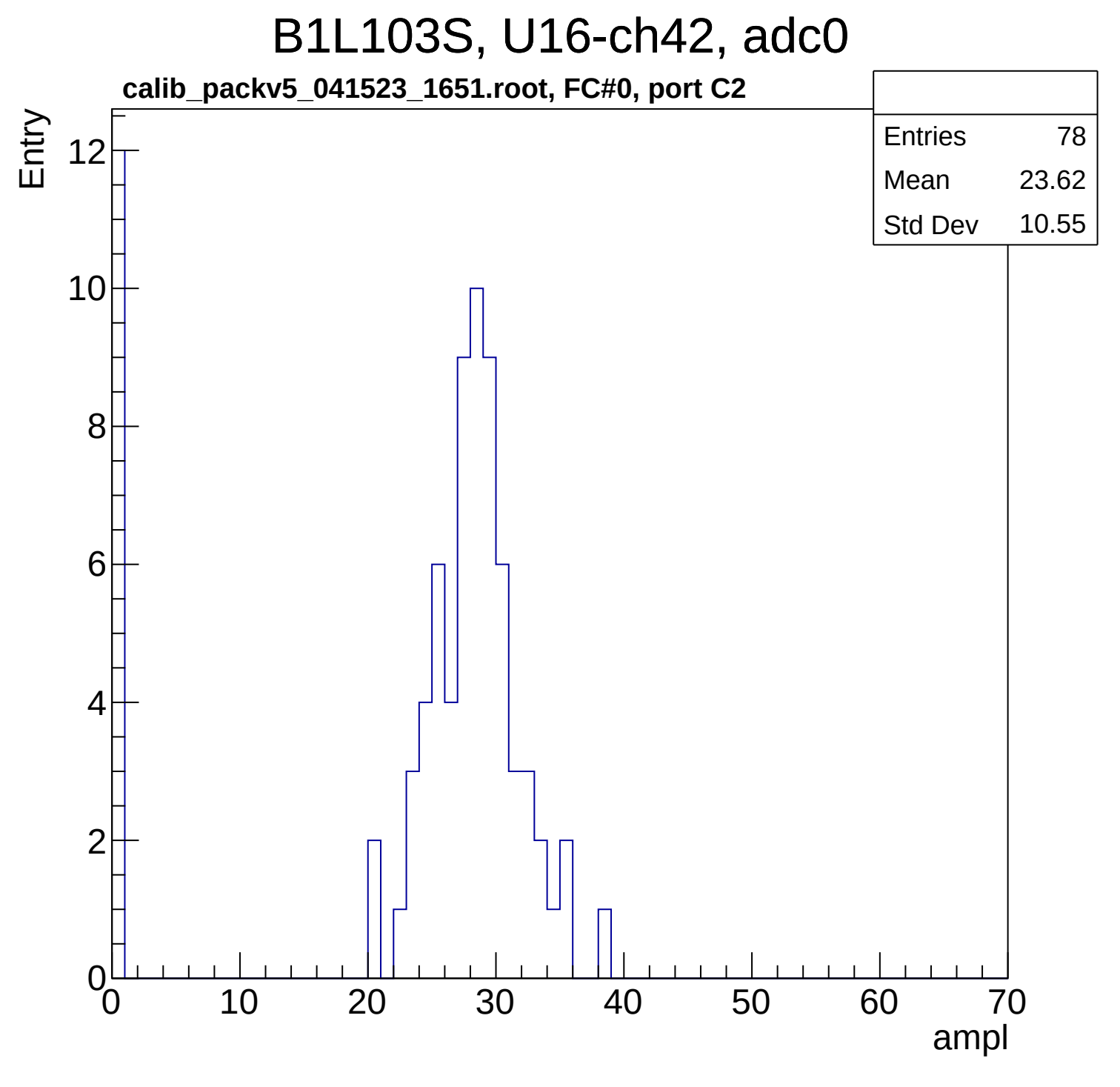
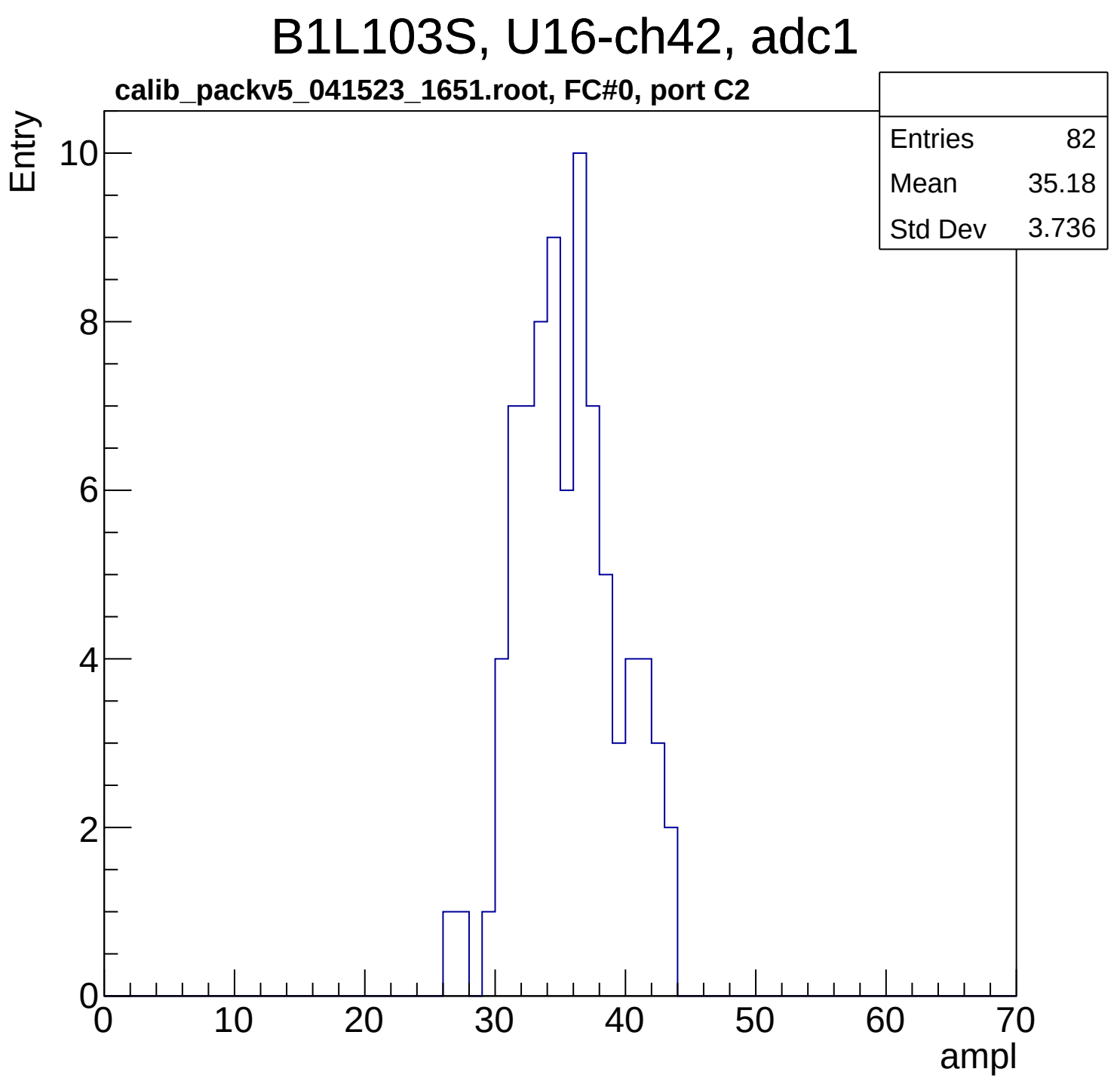
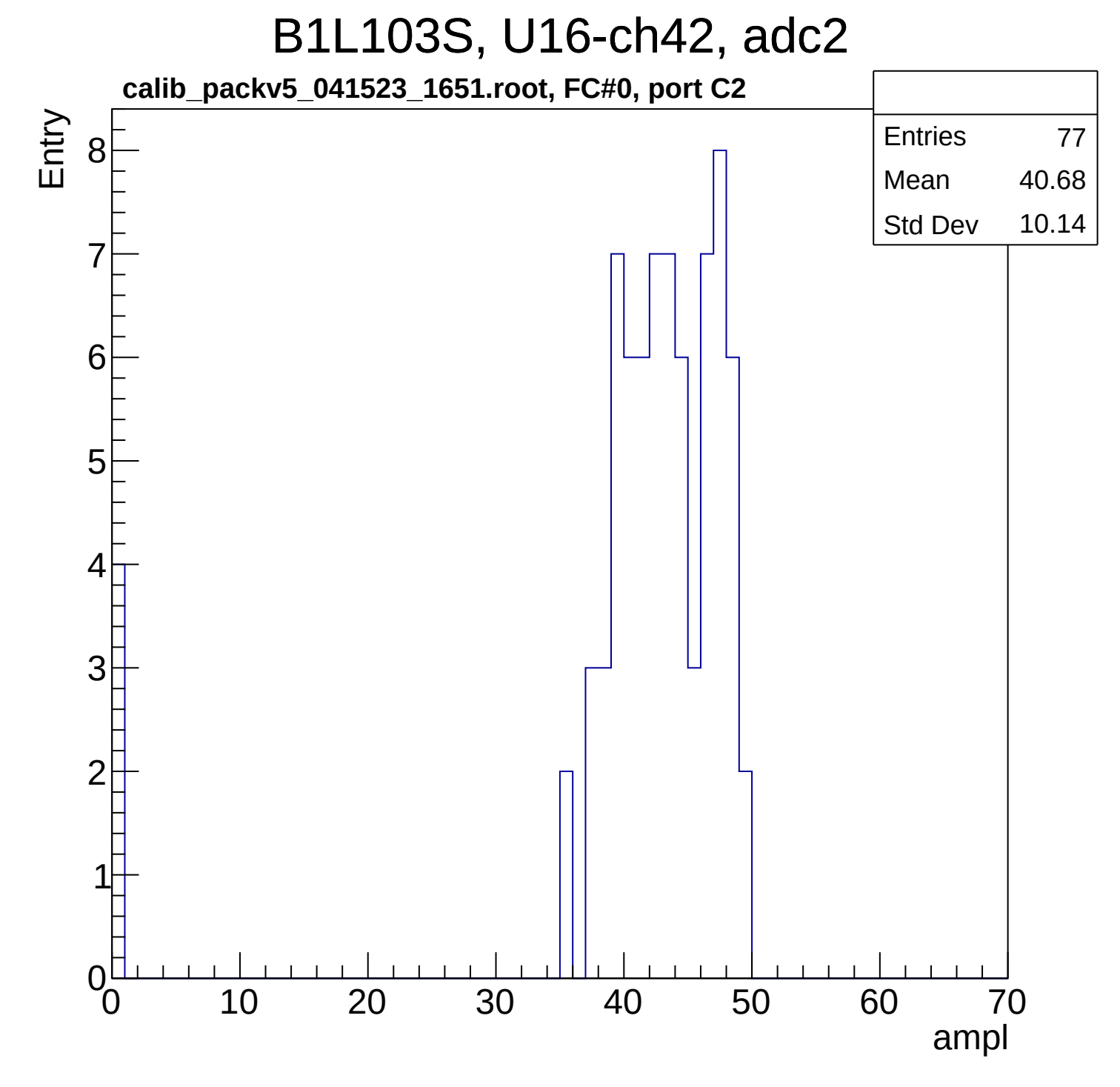
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch41, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch41, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch42, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 23.62
Std Dev 10.55
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U16-ch42, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 35.18
Std Dev 3.736
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch42, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 40.68
Std Dev 10.14
Entry
ampl
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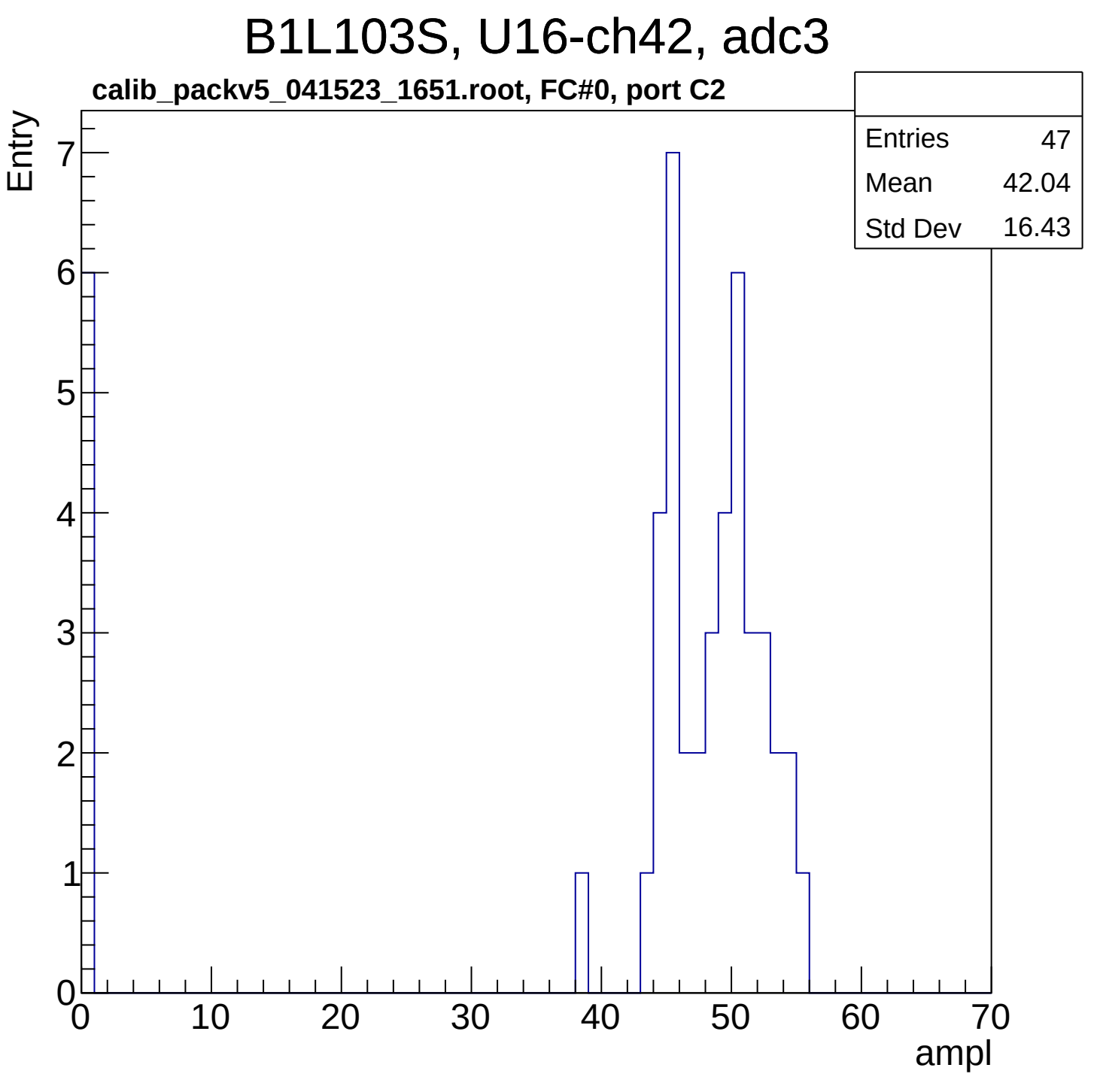
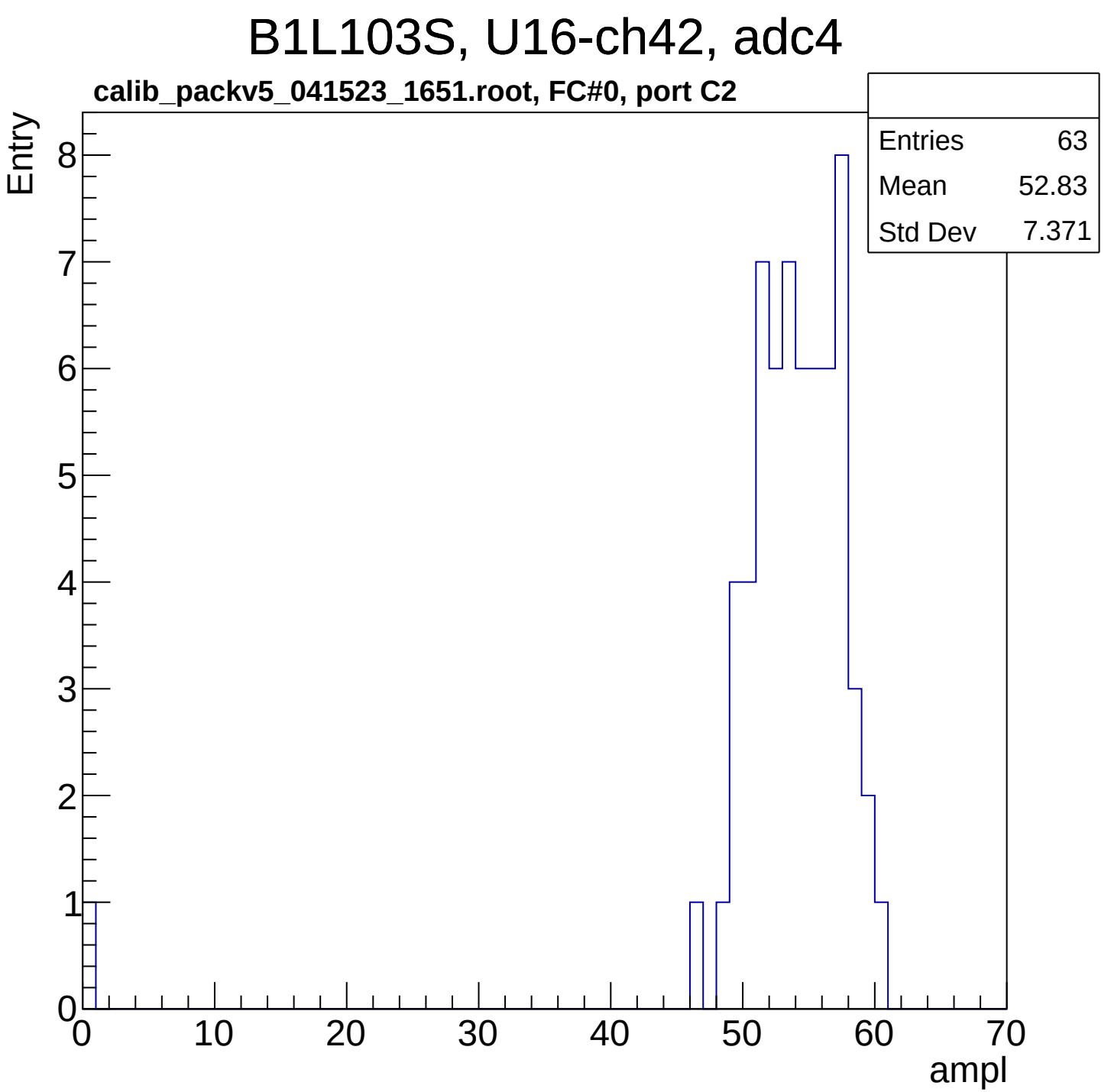
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch42, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 42.04
Std Dev 16.43
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch42, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 52.83
Std Dev 7.371
Entry
ampl
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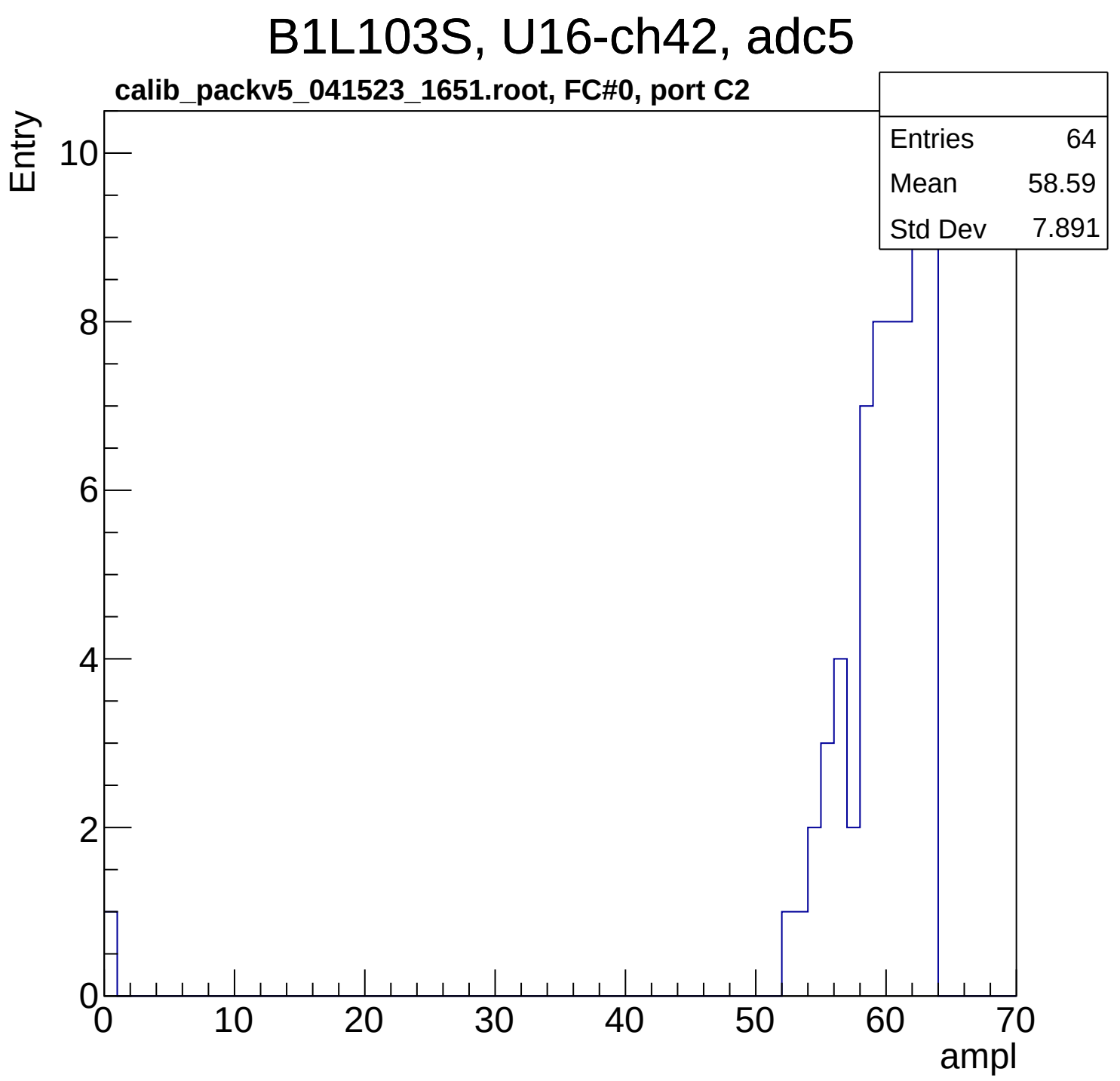
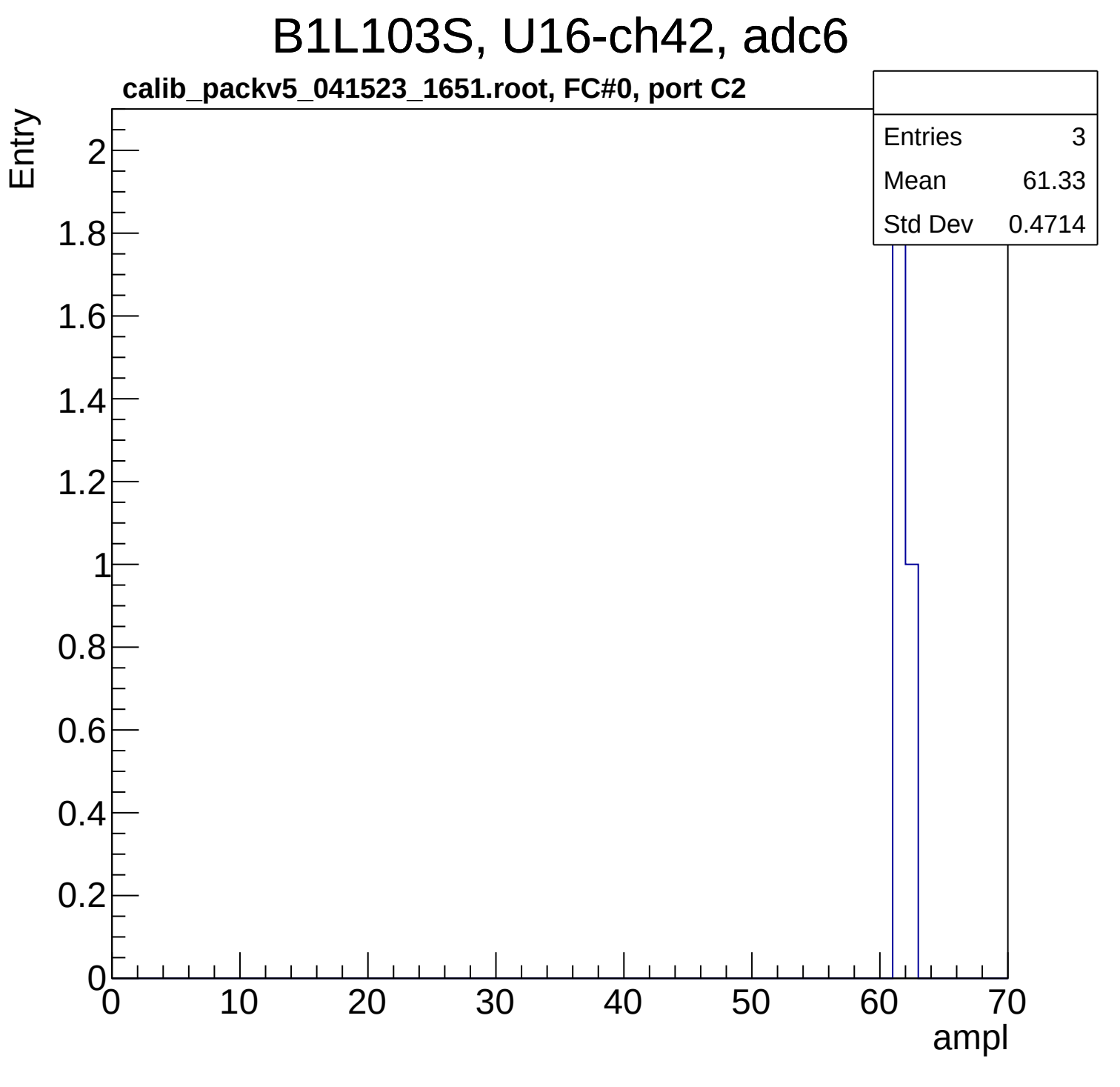
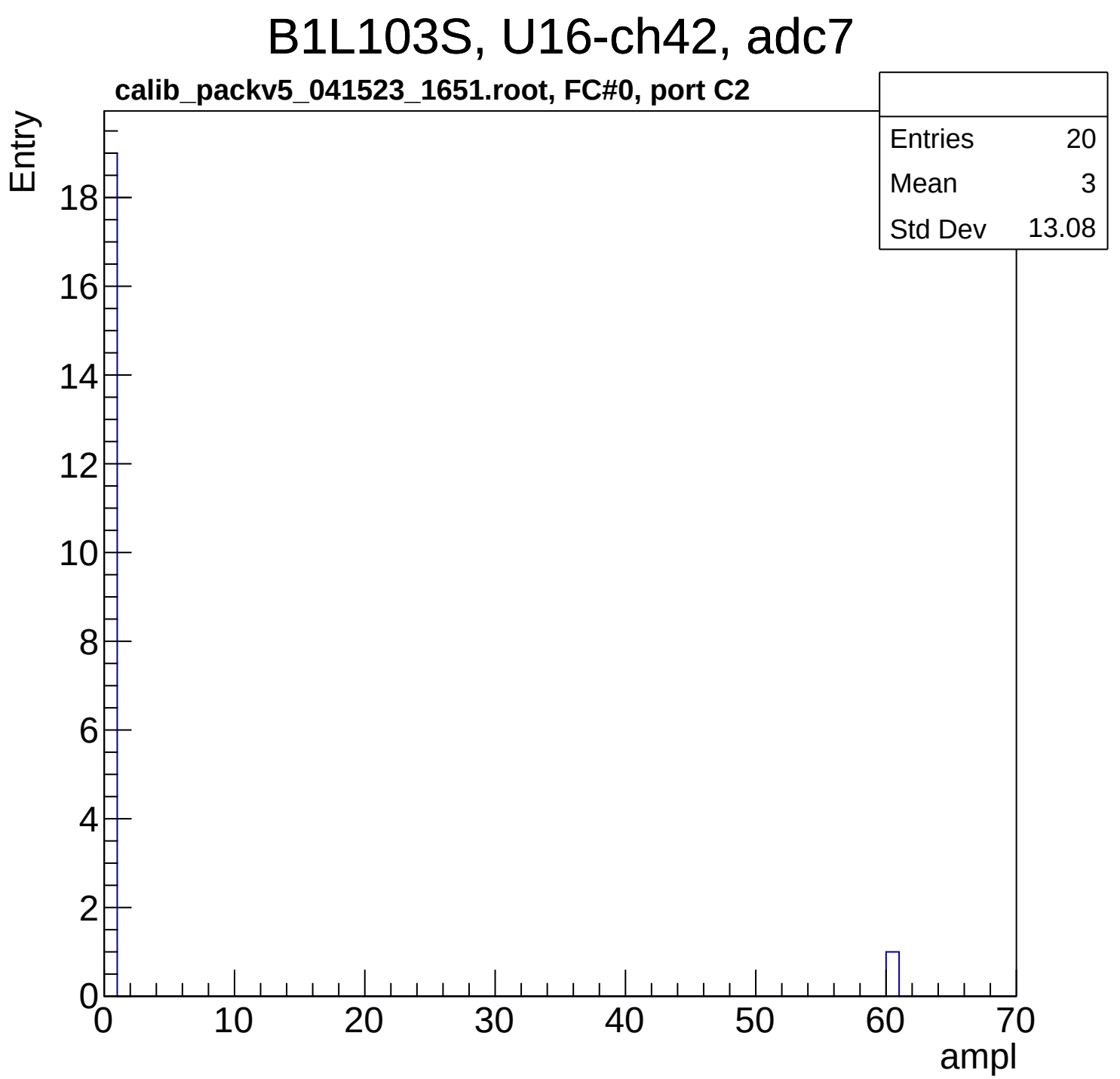
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch42, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 58.59
Std Dev 7.891
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch42, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 61.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U16-ch42, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3
Std Dev 13.08
Entry
0
2
4
6
8
10
12
14
16
18
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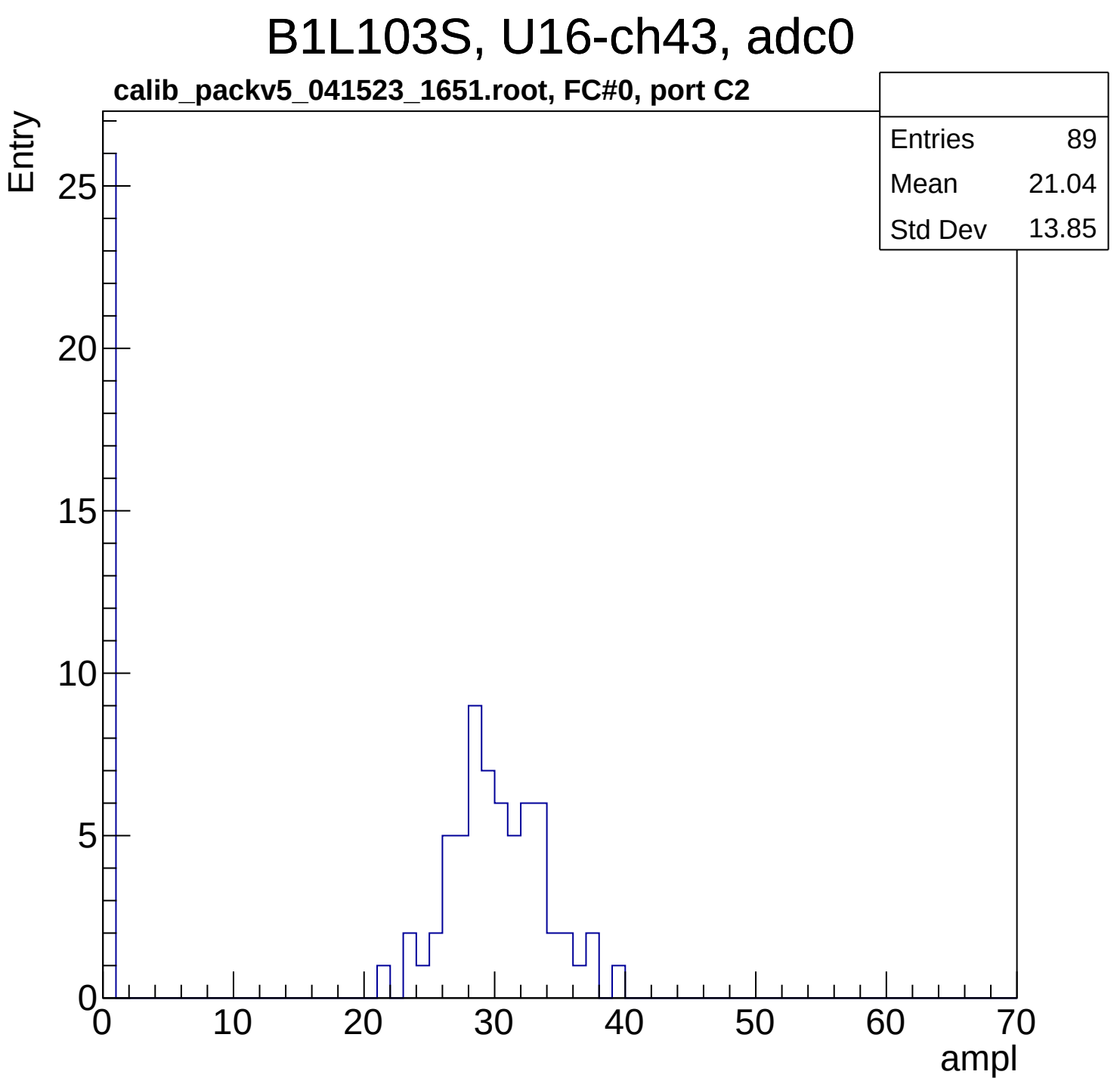
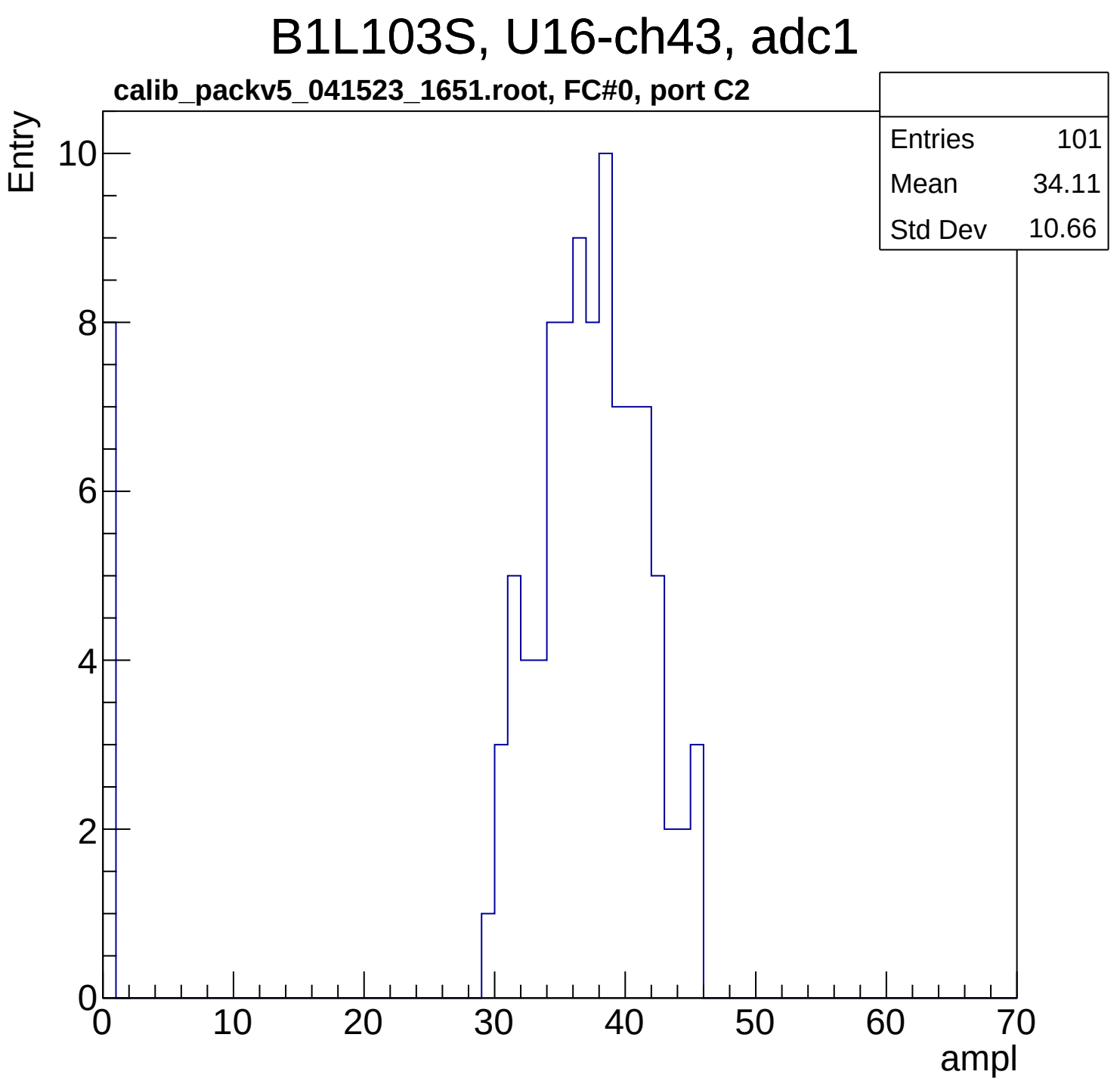
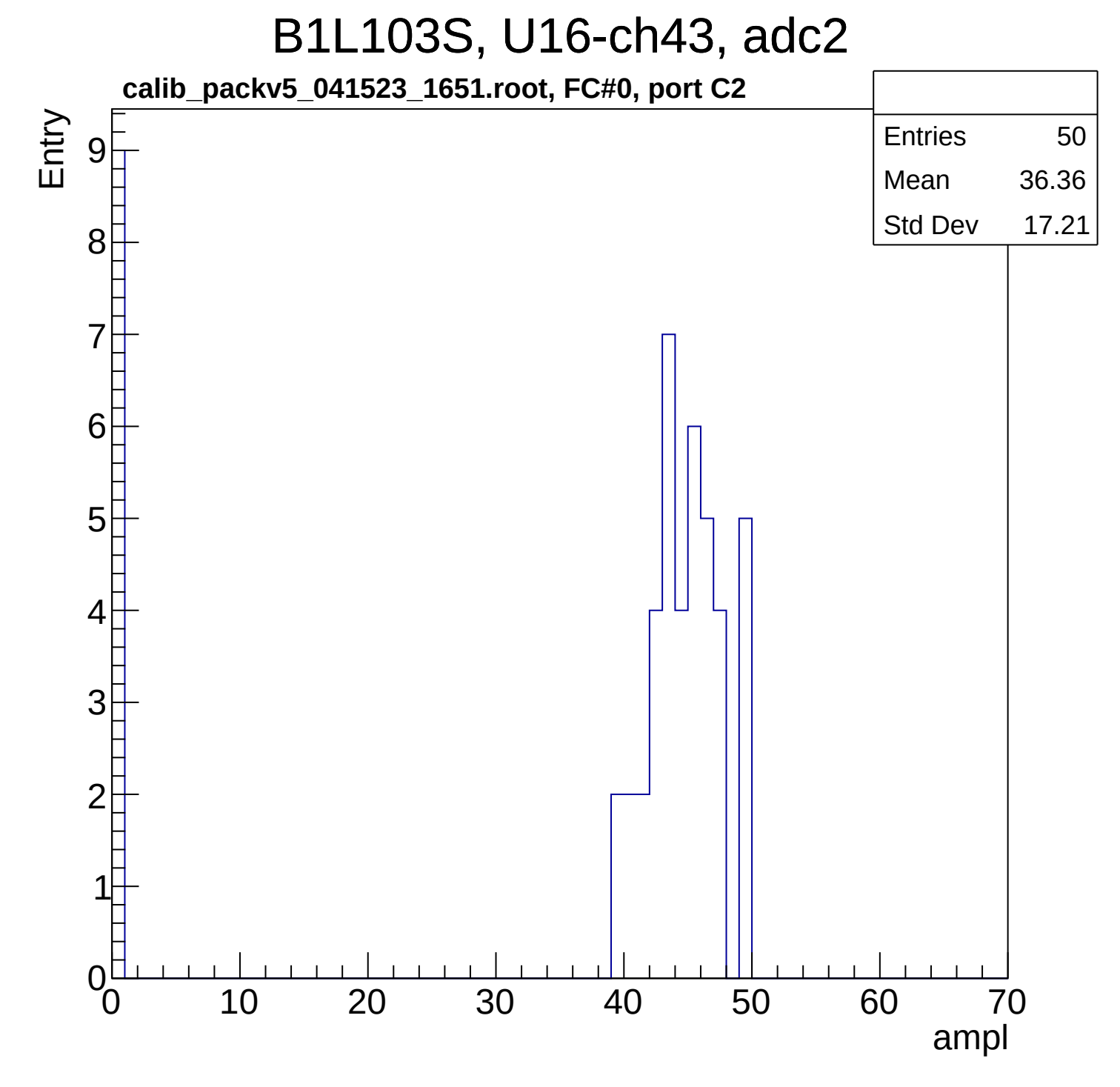
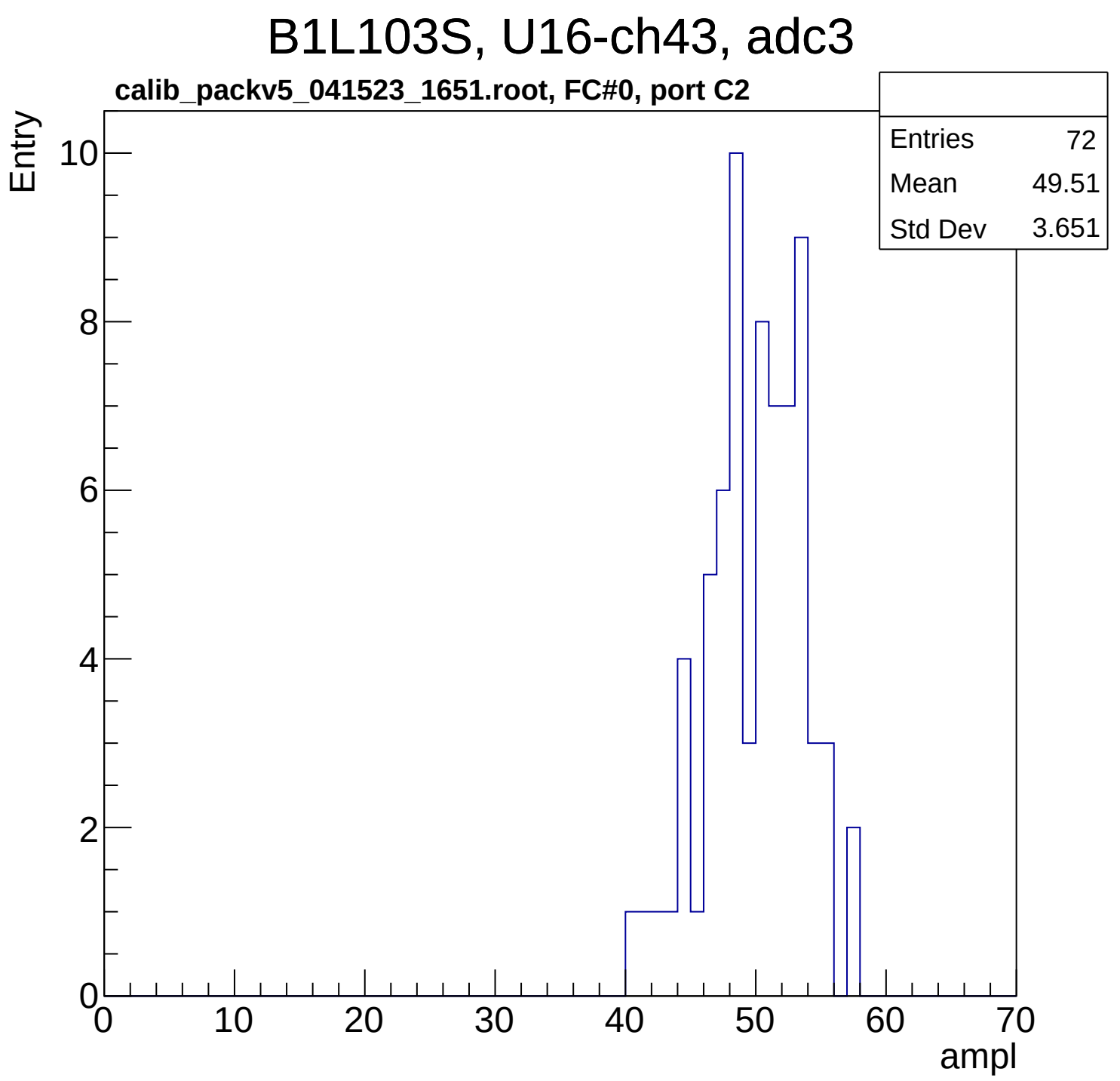
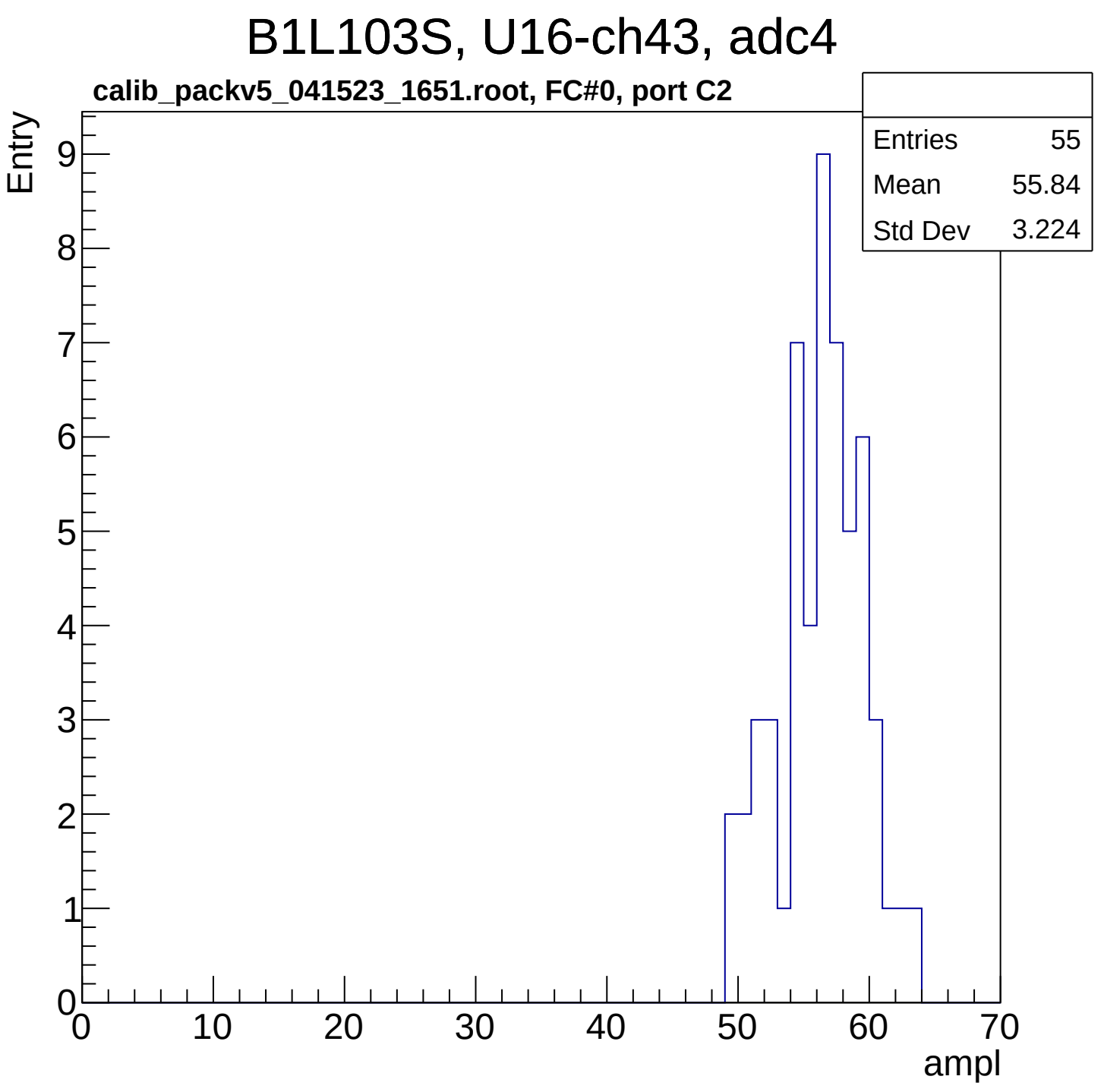
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch43, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 21.04
Std Dev 13.85
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch43, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 34.11
Std Dev 10.66
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch43, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 36.36
Std Dev 17.21
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch43, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 49.51
Std Dev 3.651
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch43, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 55.84
Std Dev 3.224
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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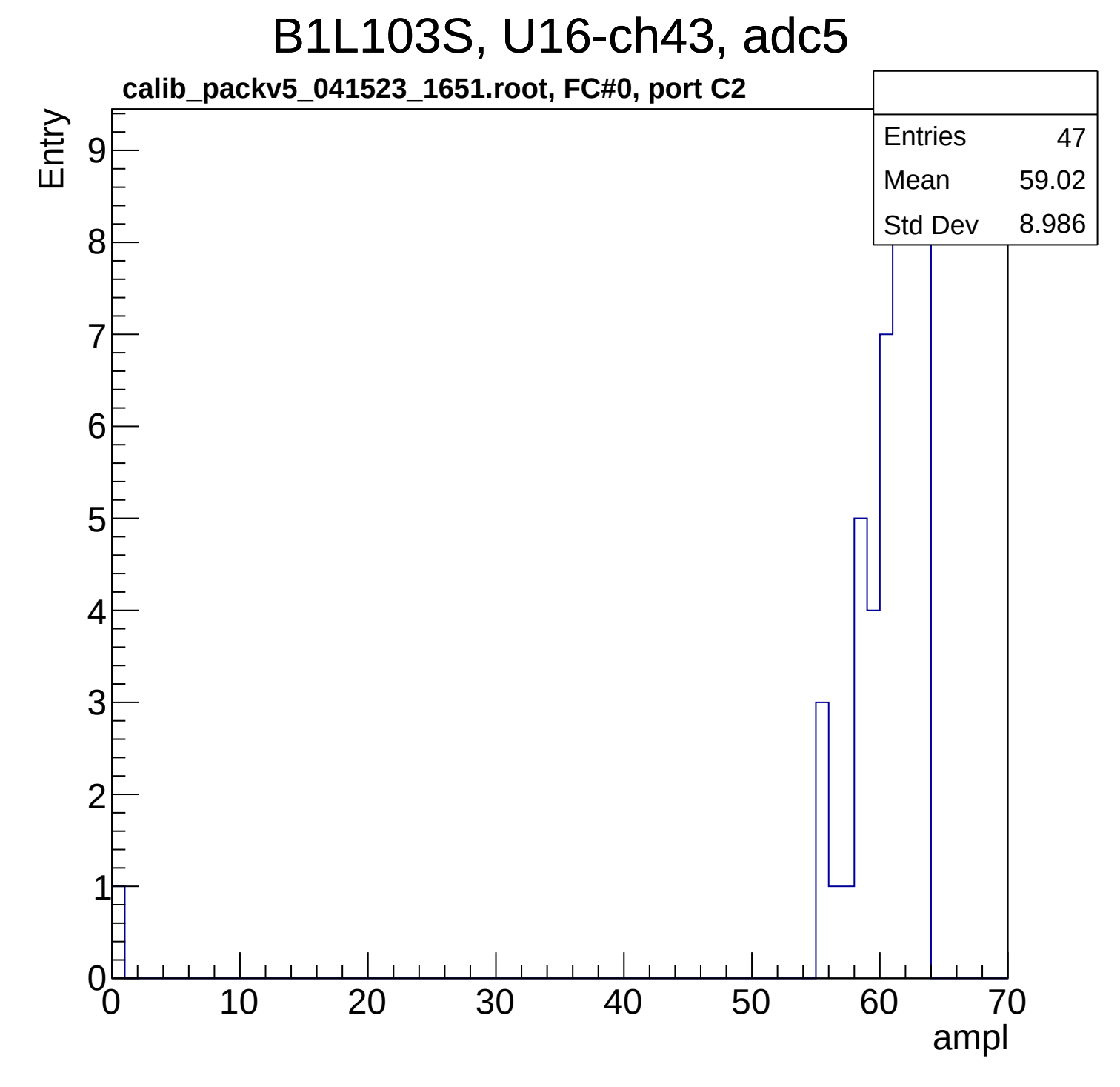
B1L103S, U16-ch43, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 59.02
Std Dev 8.986
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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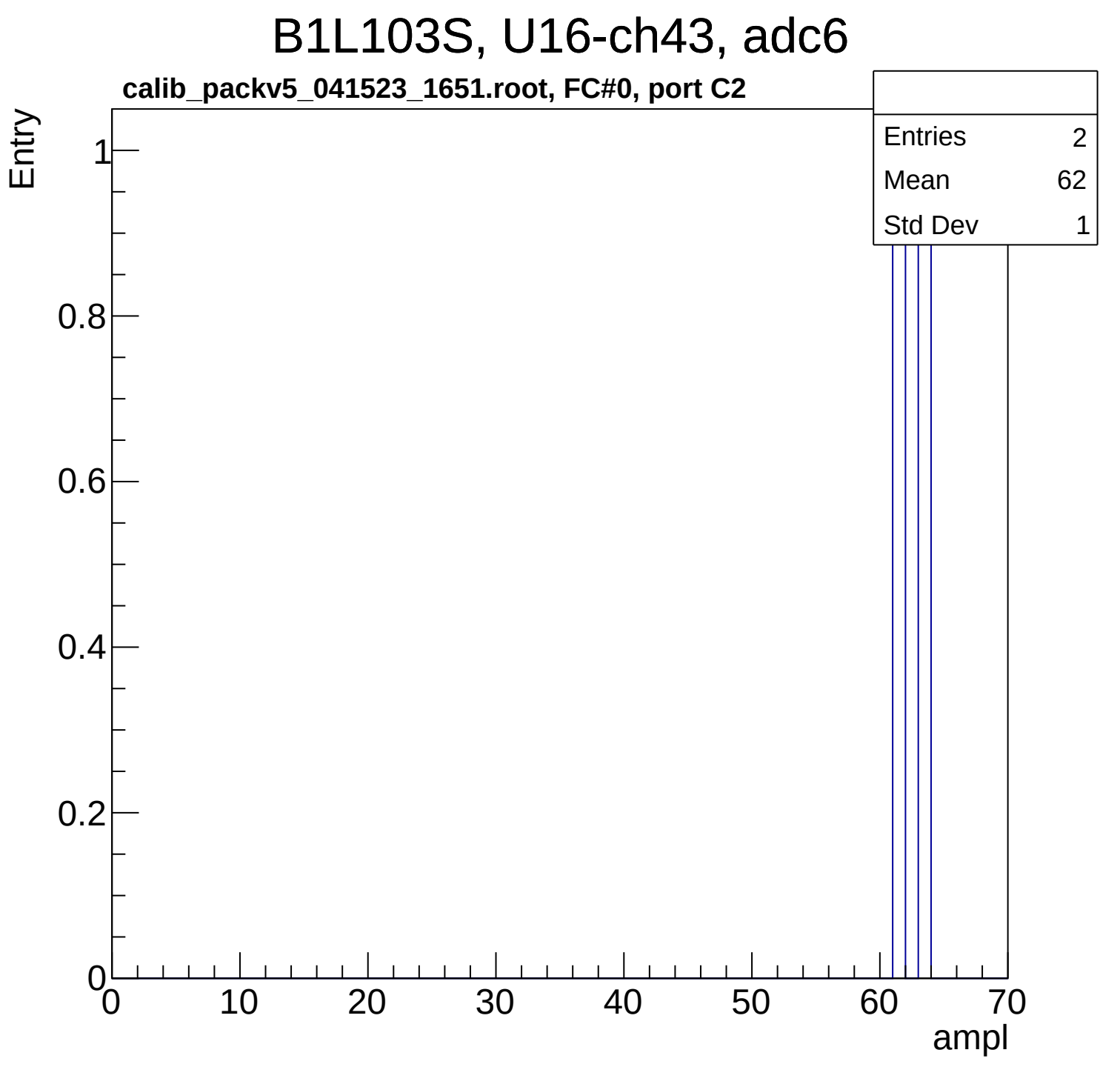
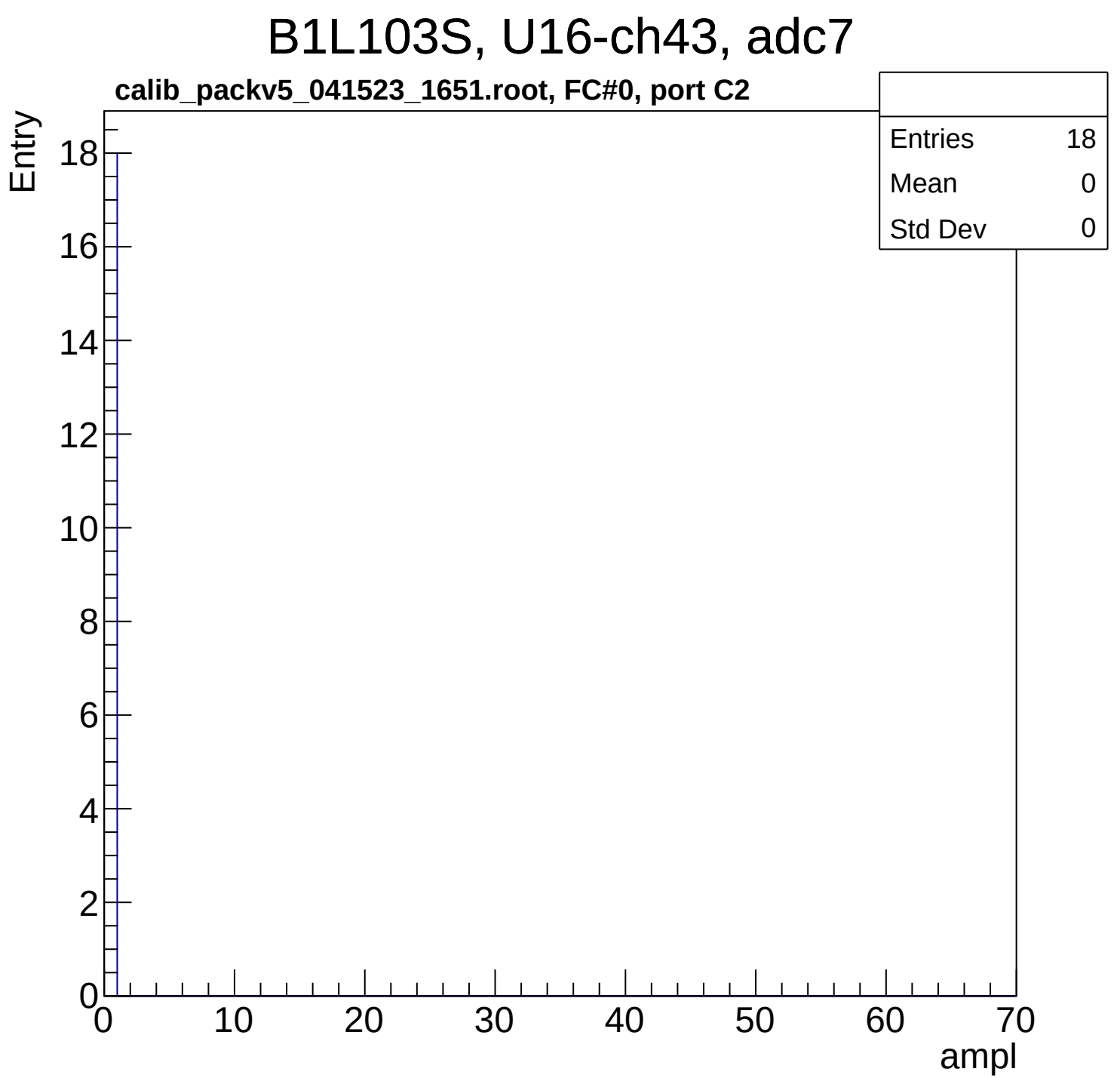
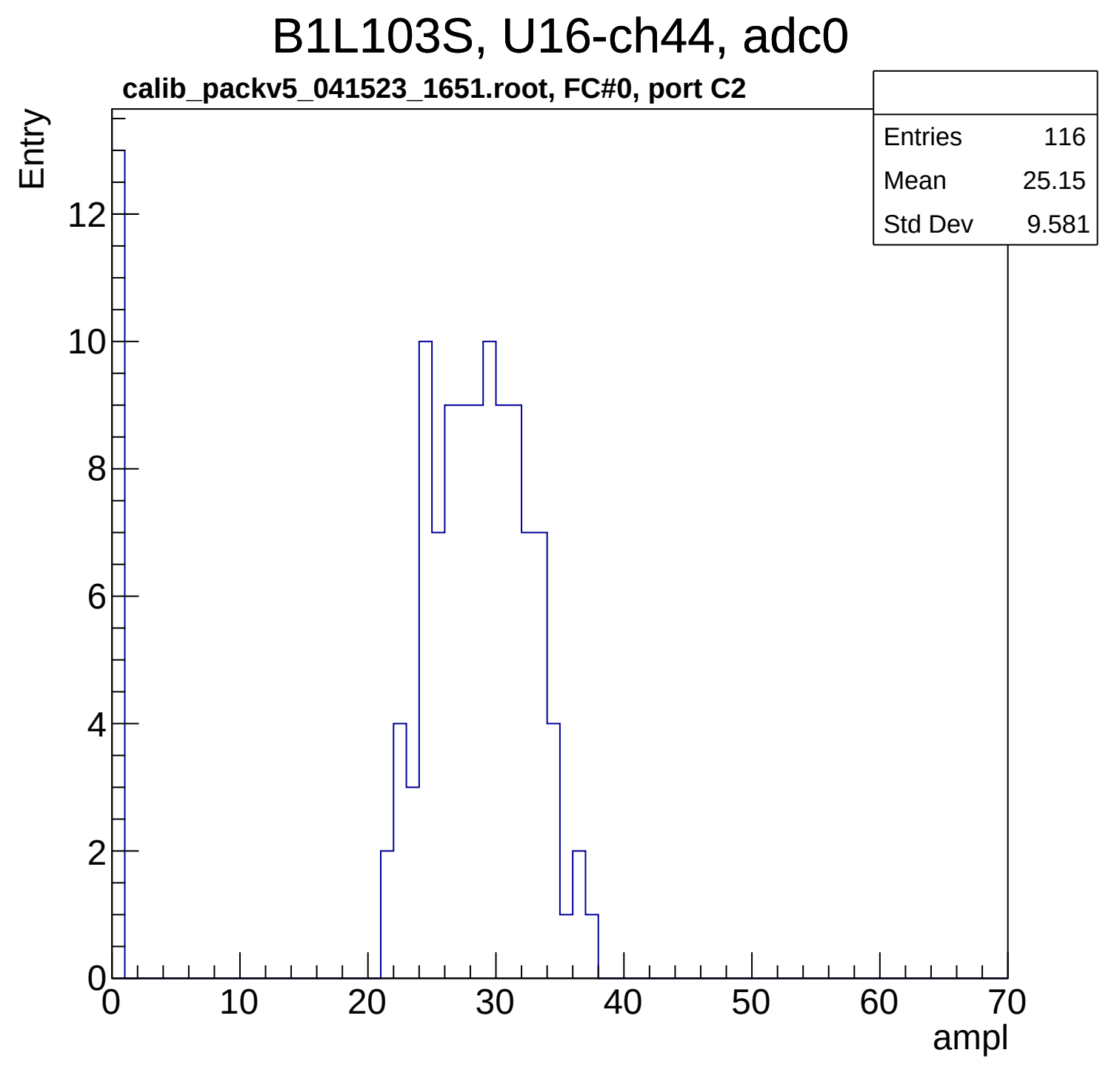
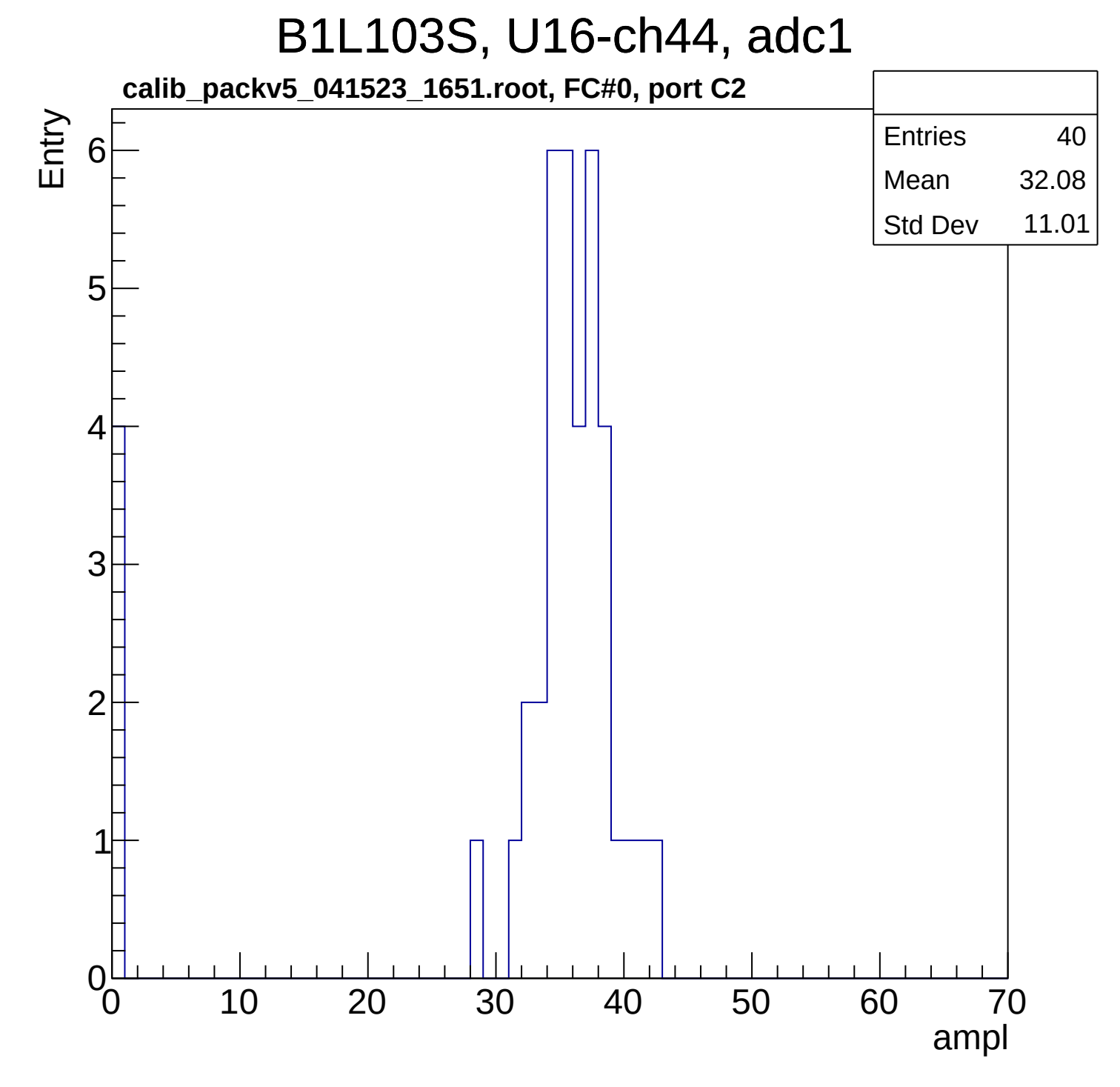
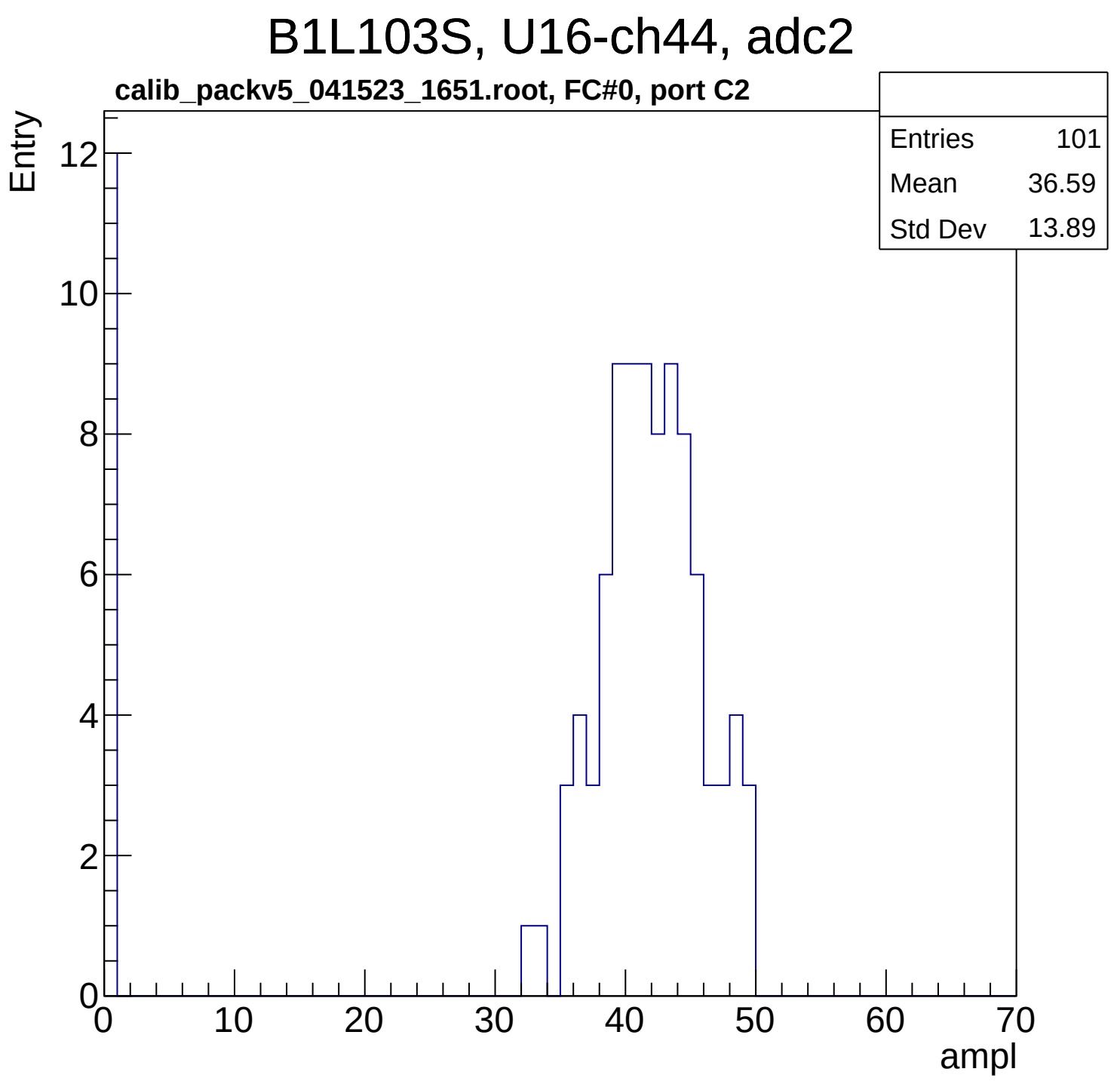
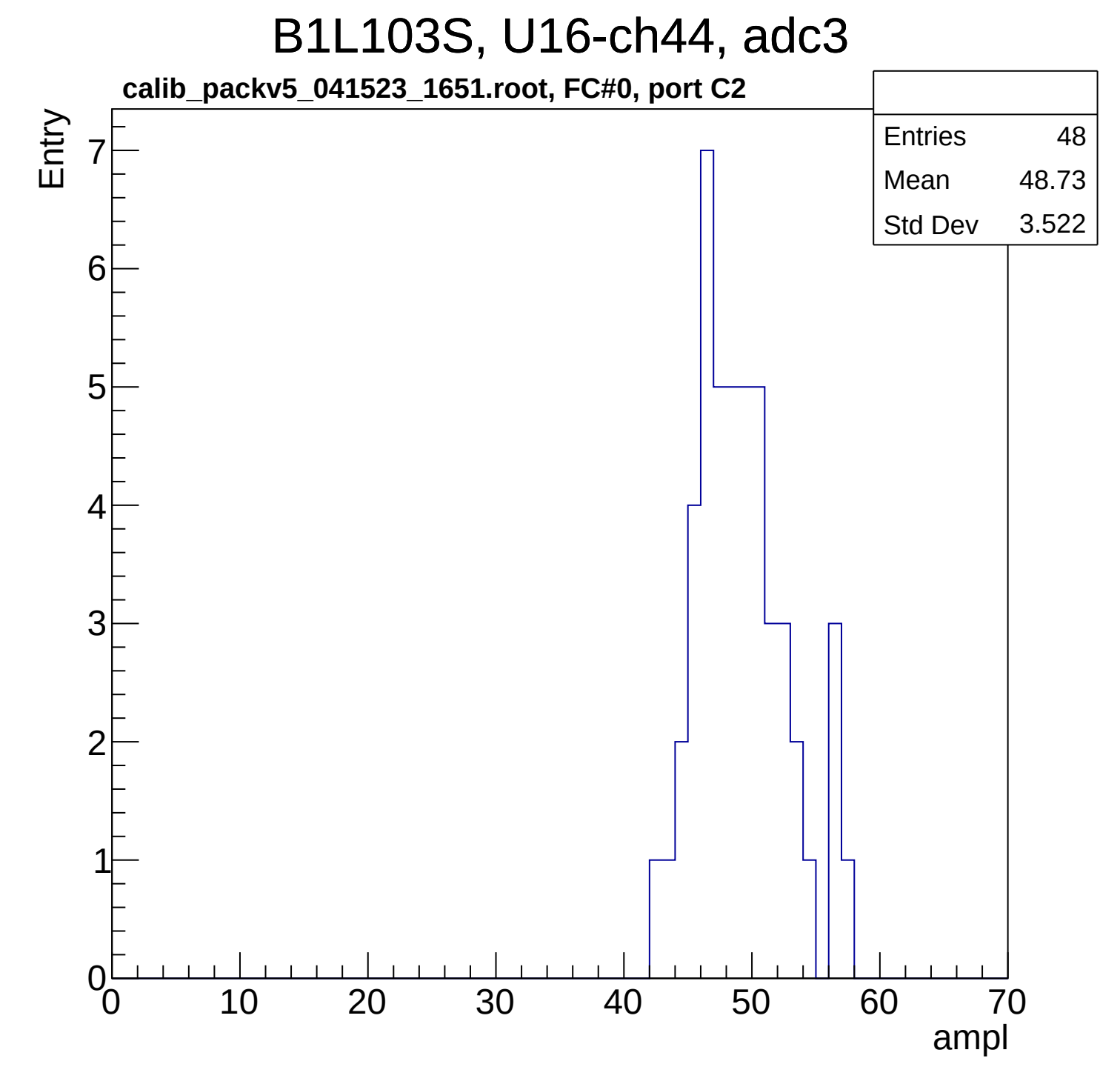

B1L103S, U16-ch43, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62
Std Dev 1
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch43, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch44, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 116
Mean 25.15
Std Dev 9.581
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U16-ch44, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 32.08
Std Dev 11.01
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch44, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 36.59
Std Dev 13.89
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U16-ch44, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 48.73
Std Dev 3.522
Entry
ampl
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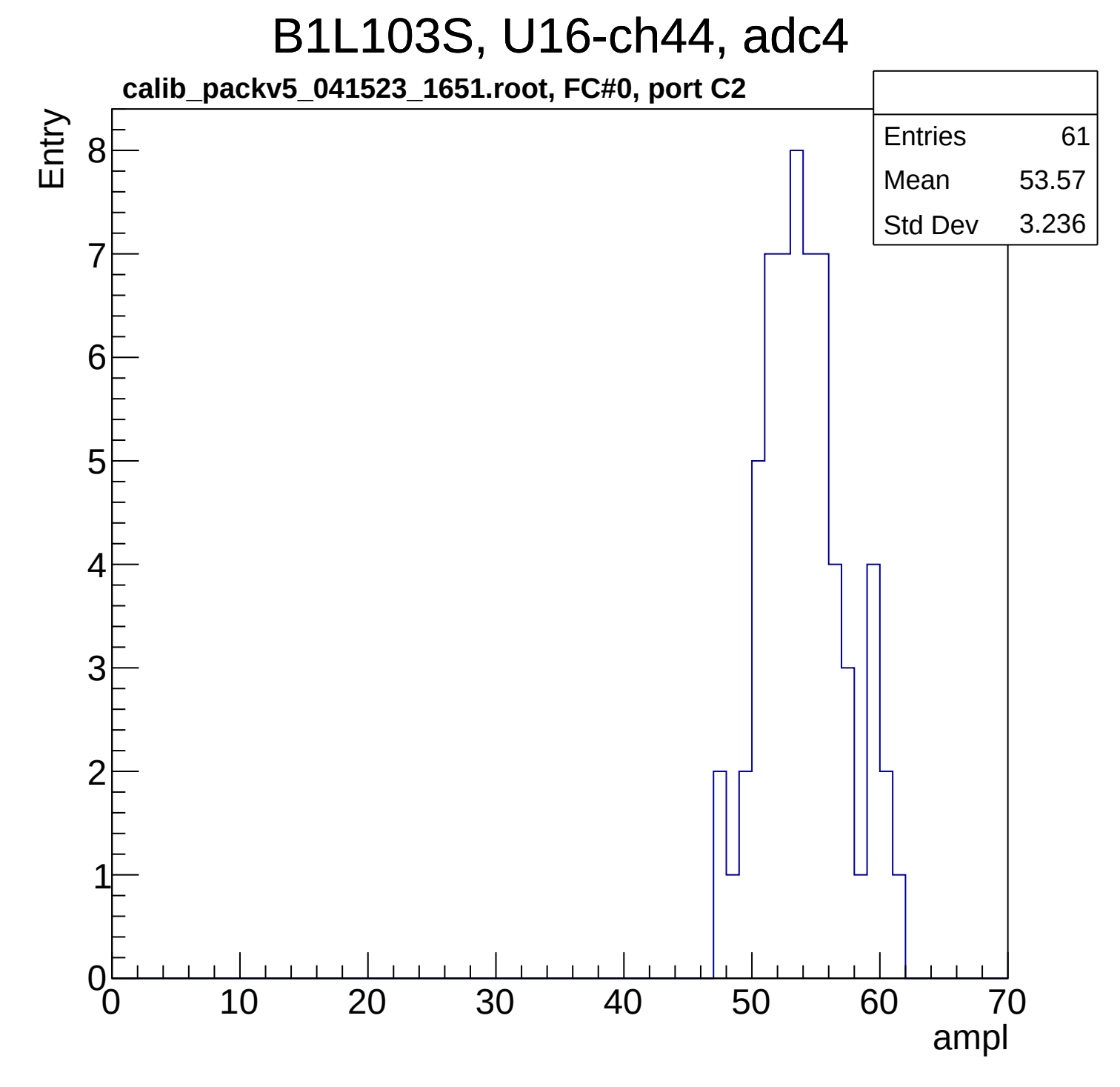
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch44, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 53.57
Std Dev 3.236
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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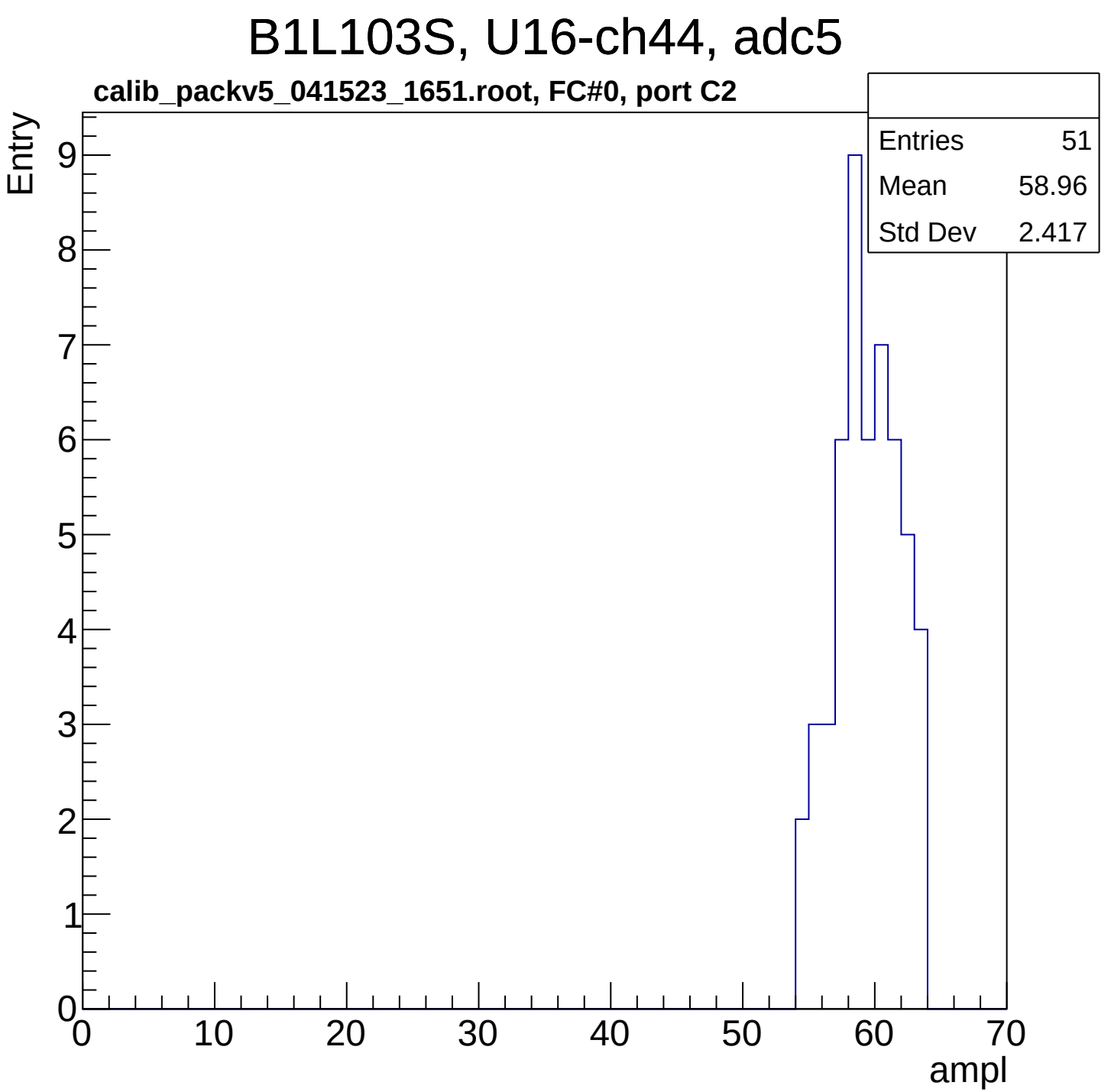
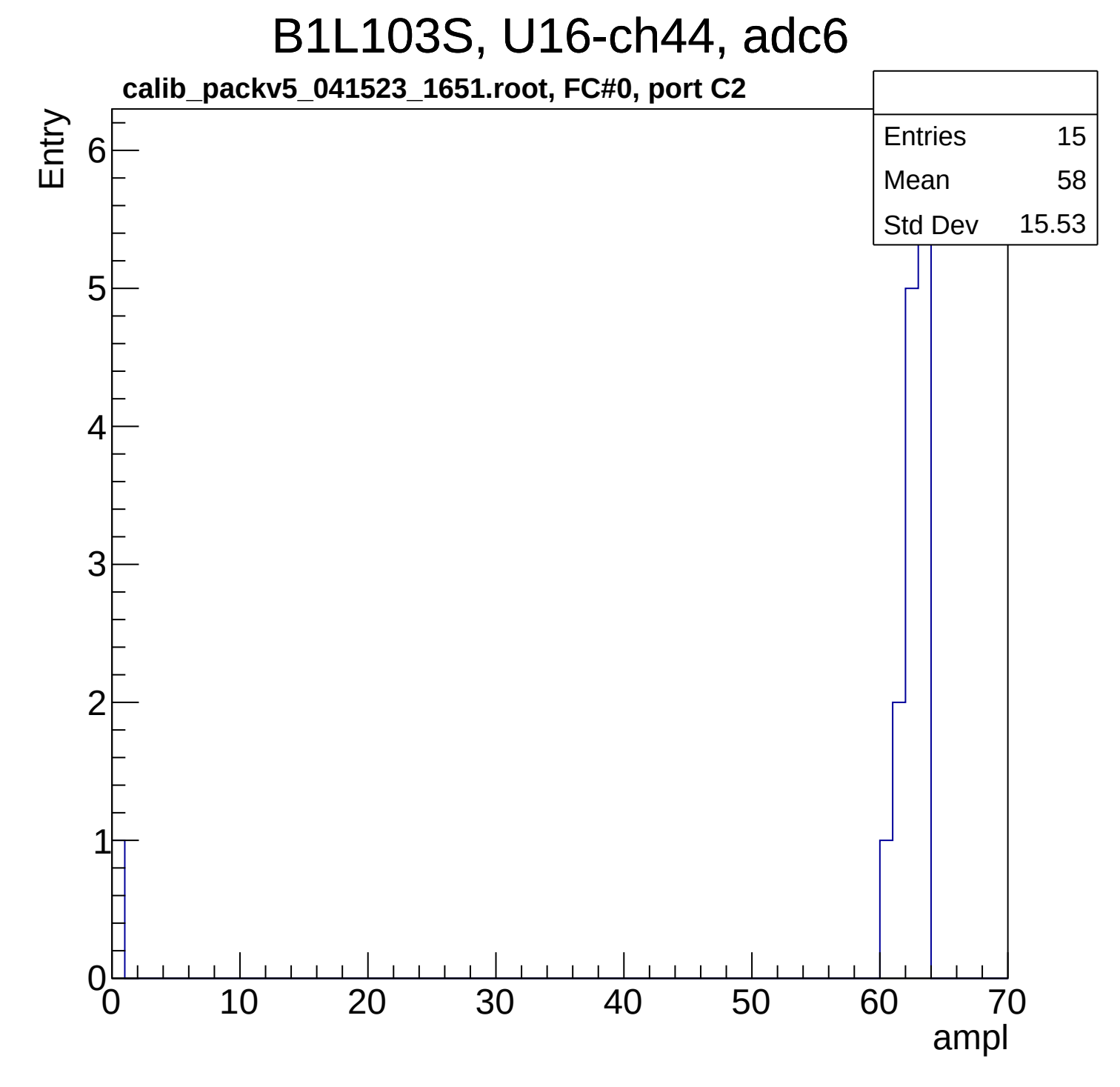
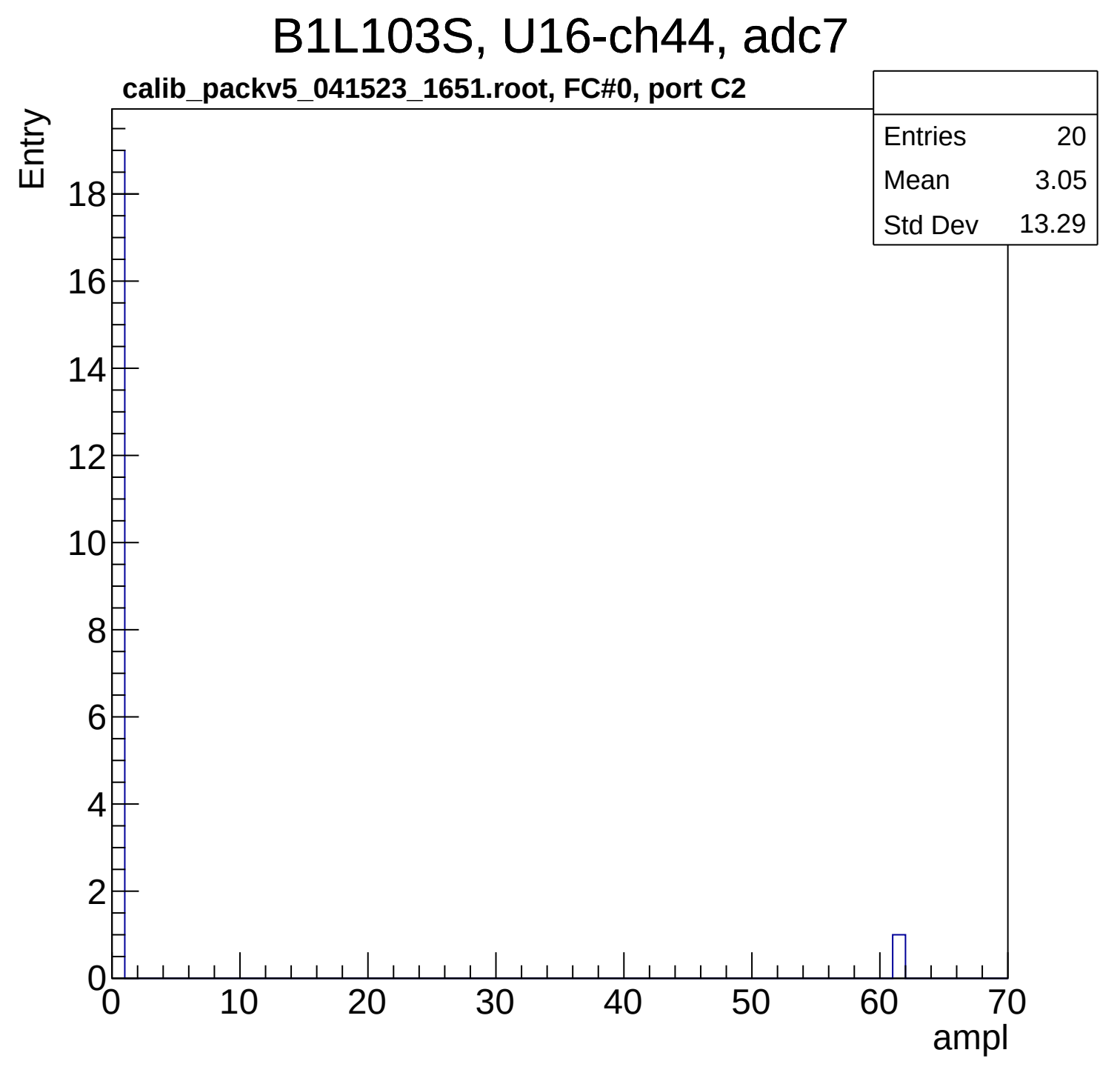
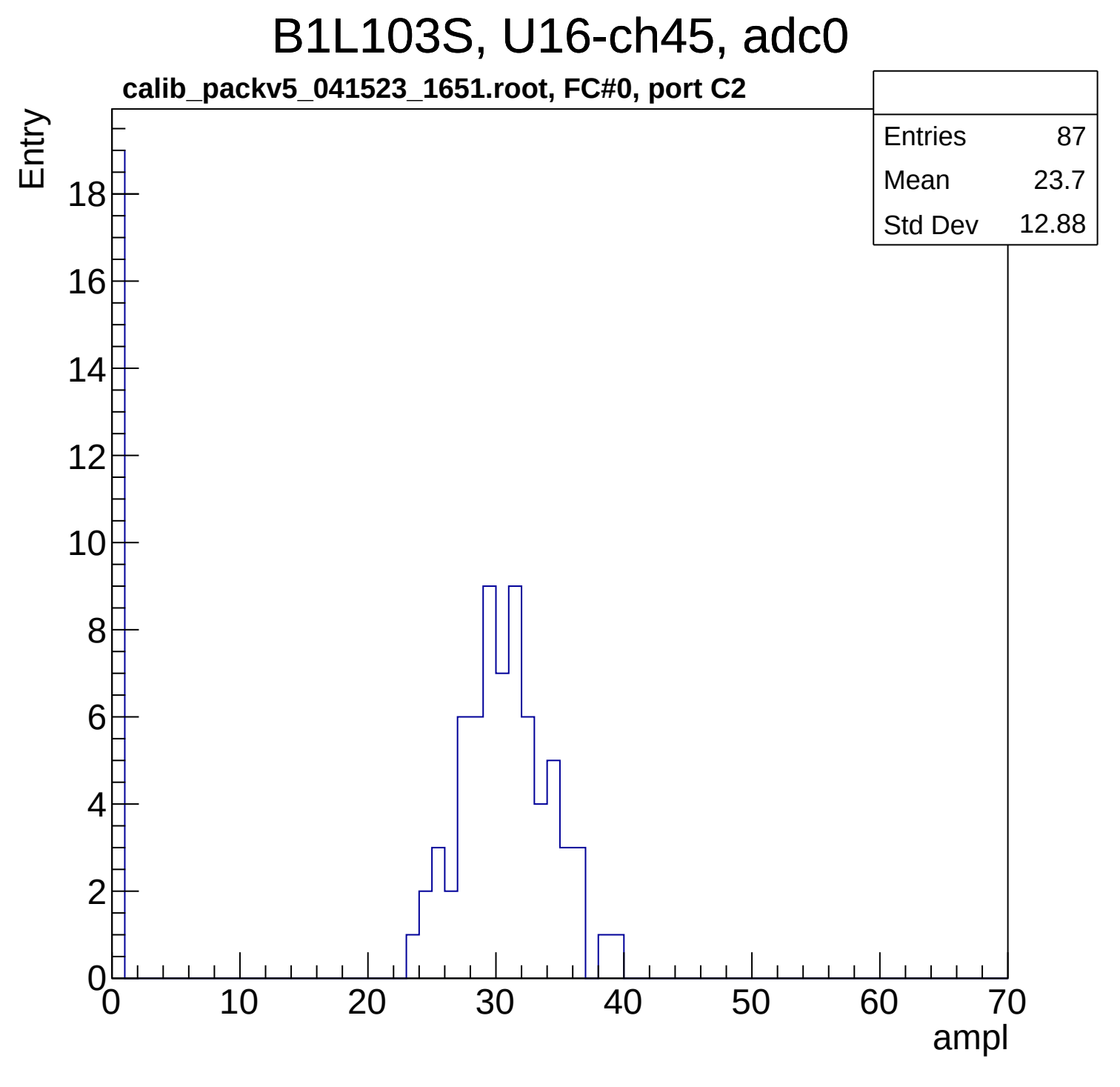
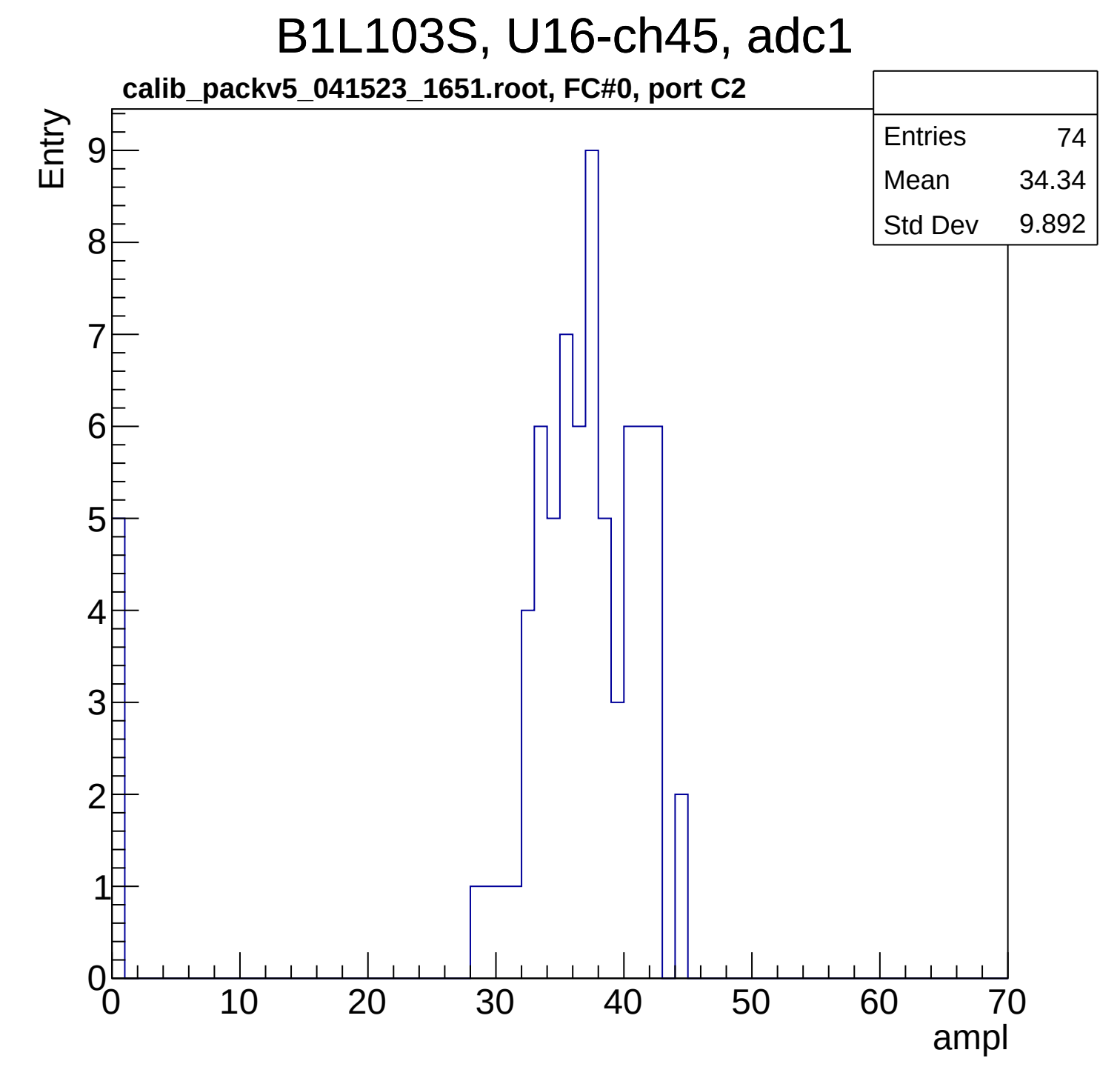
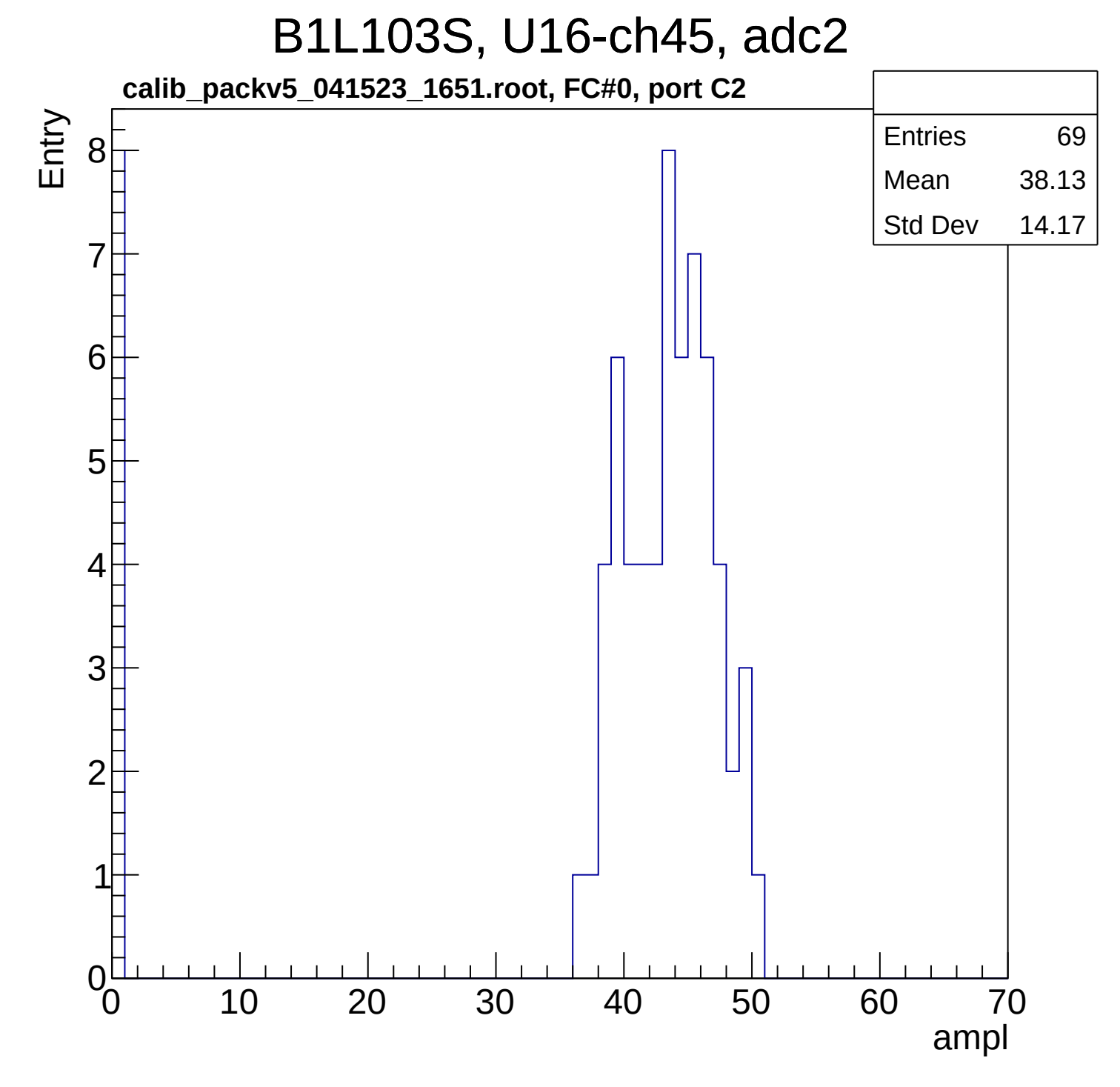

B1L103S, U16-ch44, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.96
Std Dev 2.417
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch44, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 58
Std Dev 15.53
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U16-ch44, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch45, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 23.7
Std Dev 12.88
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch45, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 34.34
Std Dev 9.892
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch45, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 38.13
Std Dev 14.17
Entry
ampl
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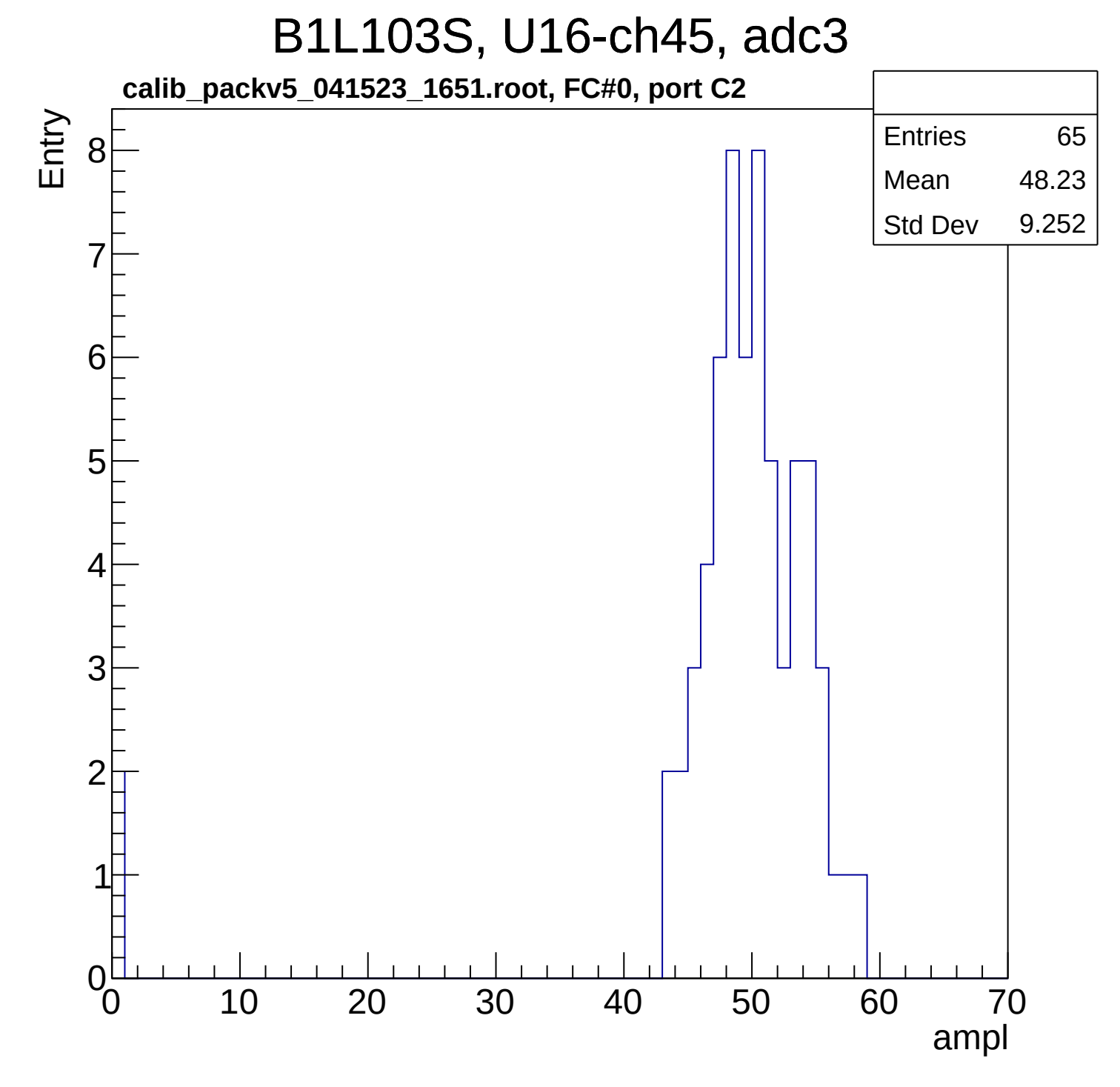
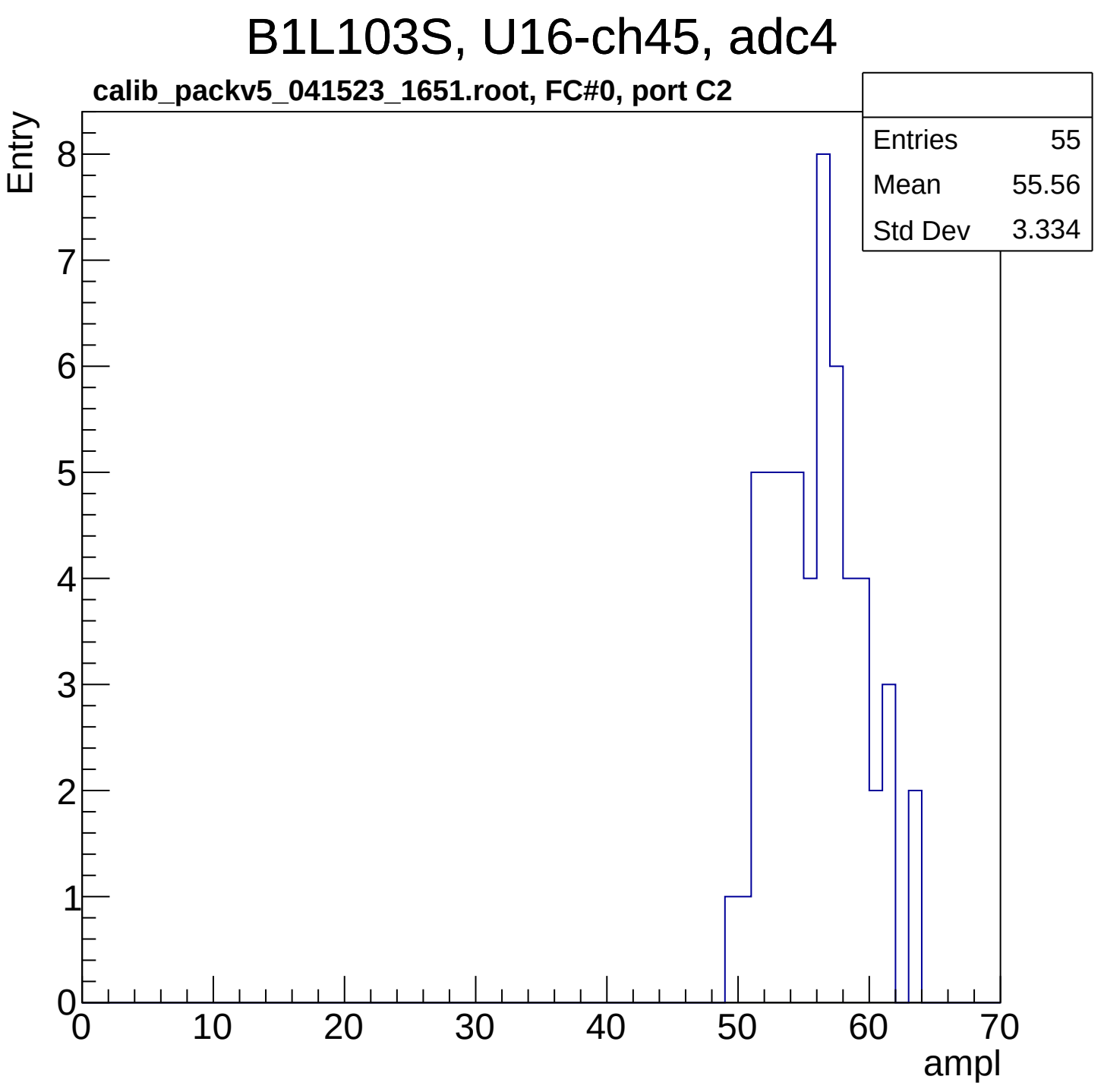
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch45, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 48.23
Std Dev 9.252
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch45, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 55.56
Std Dev 3.334
Entry
ampl
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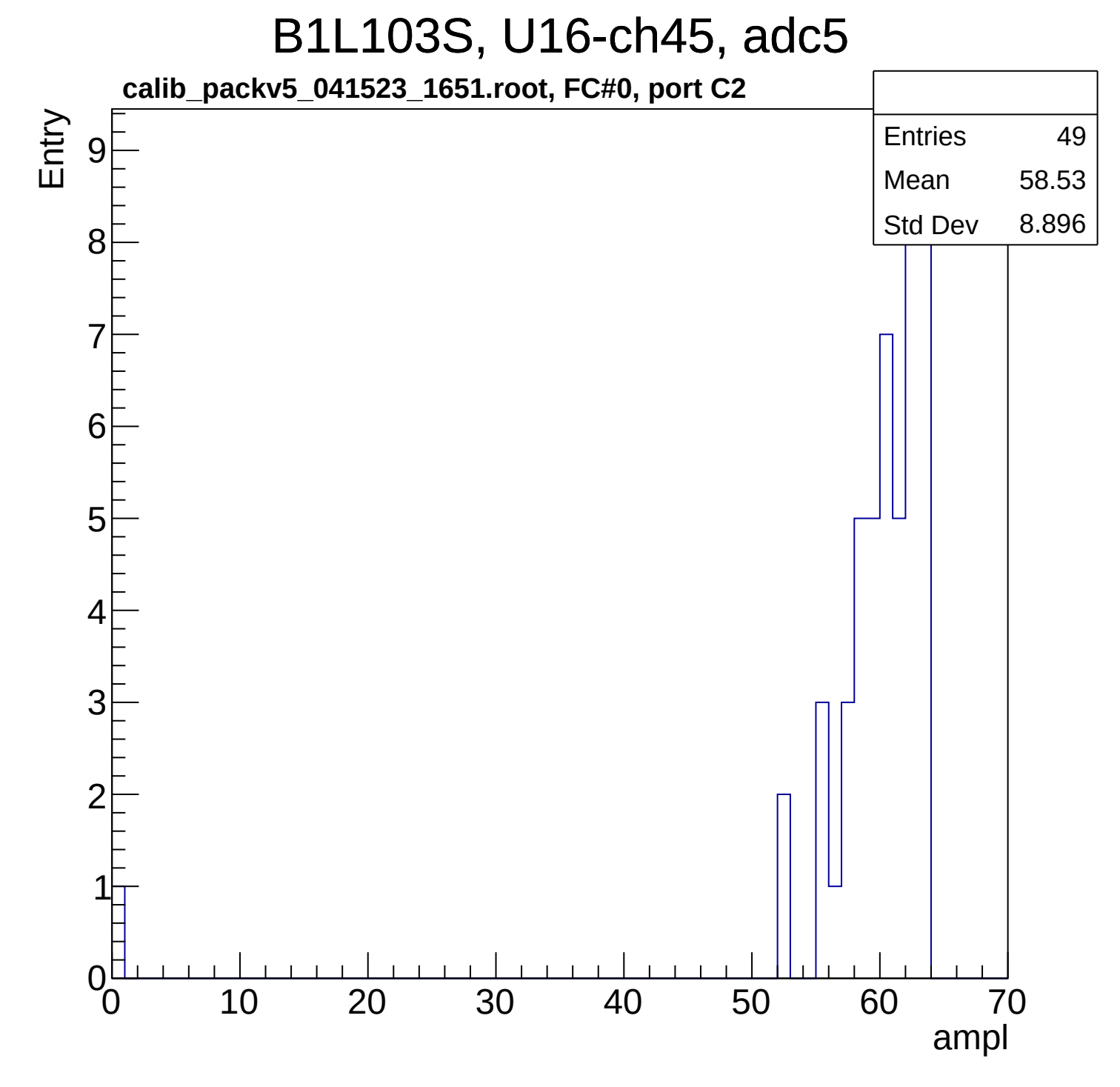
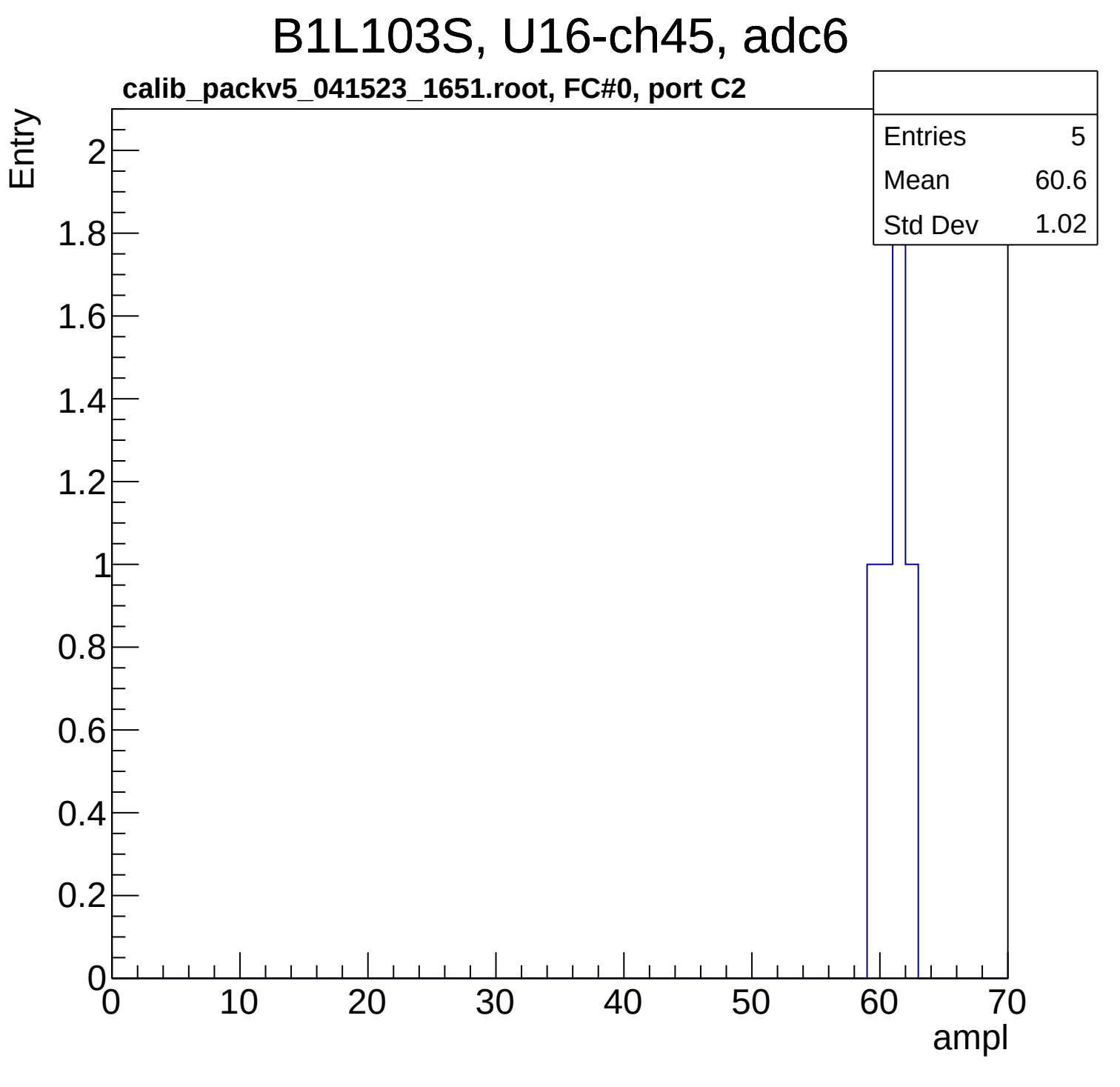
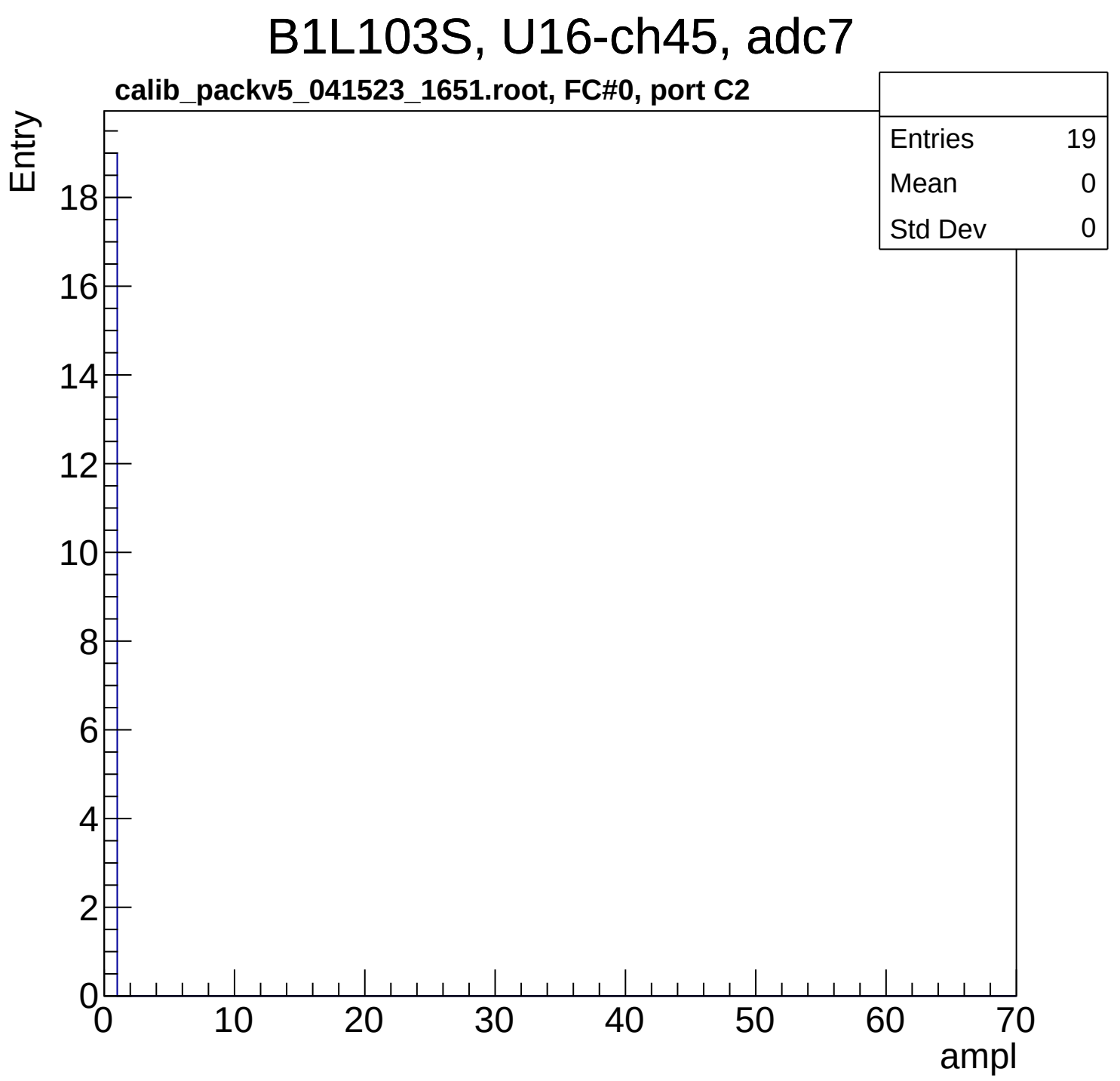
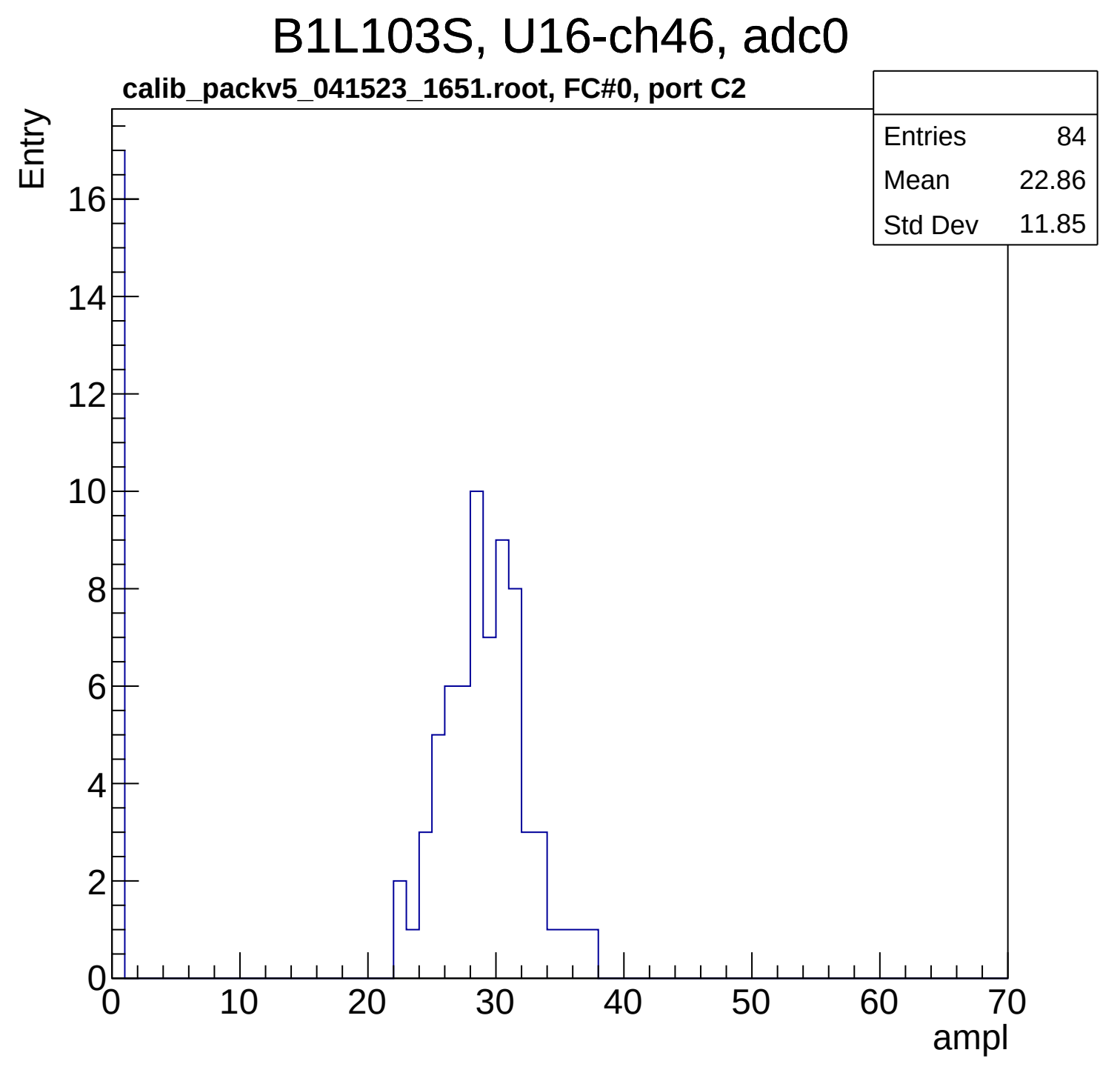
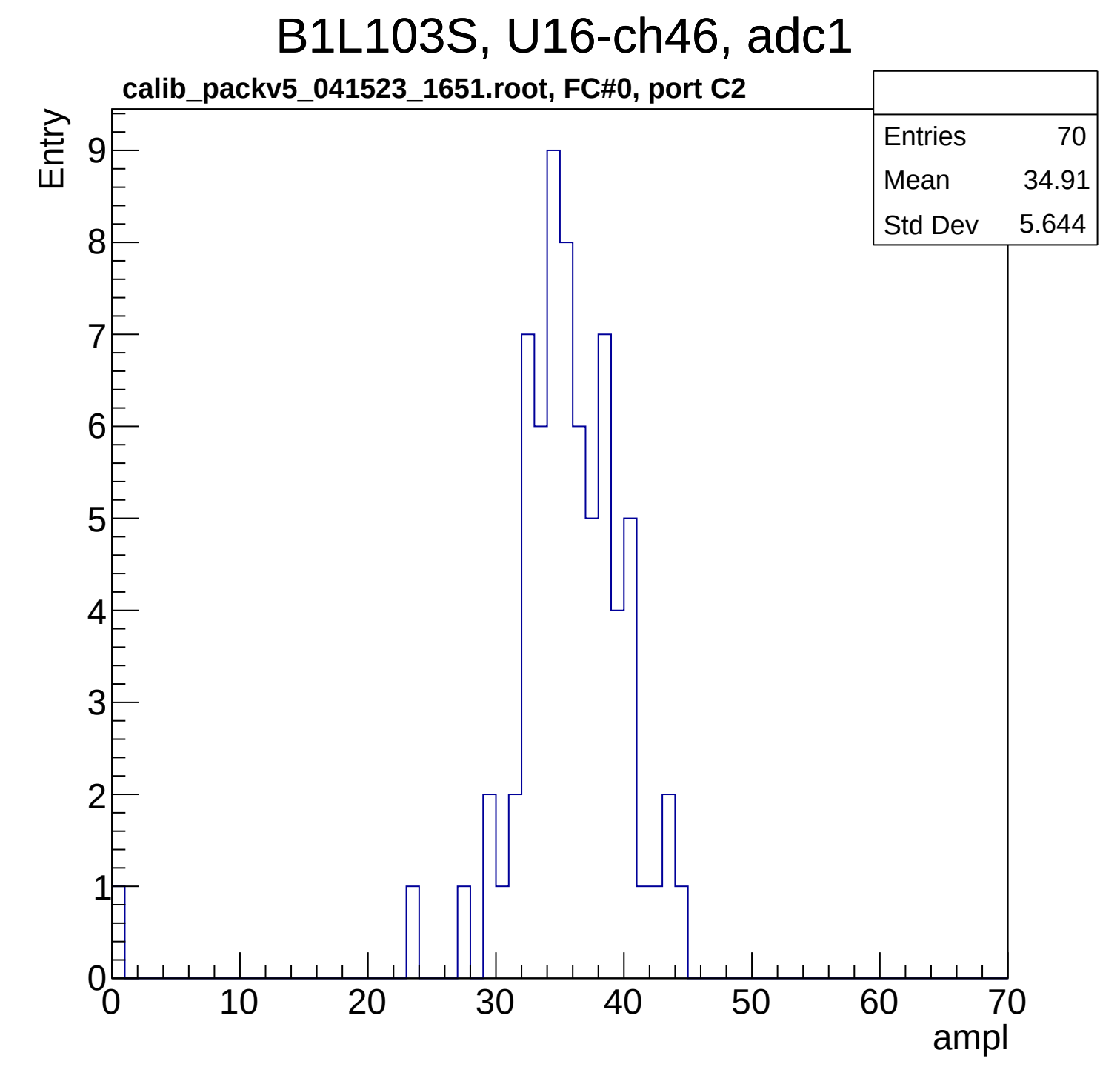
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch45, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.53
Std Dev 8.896
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U16-ch45, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 60.6
Std Dev 1.02
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U16-ch45, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch46, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 22.86
Std Dev 11.85
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch46, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 34.91
Std Dev 5.644
Entry
ampl
0
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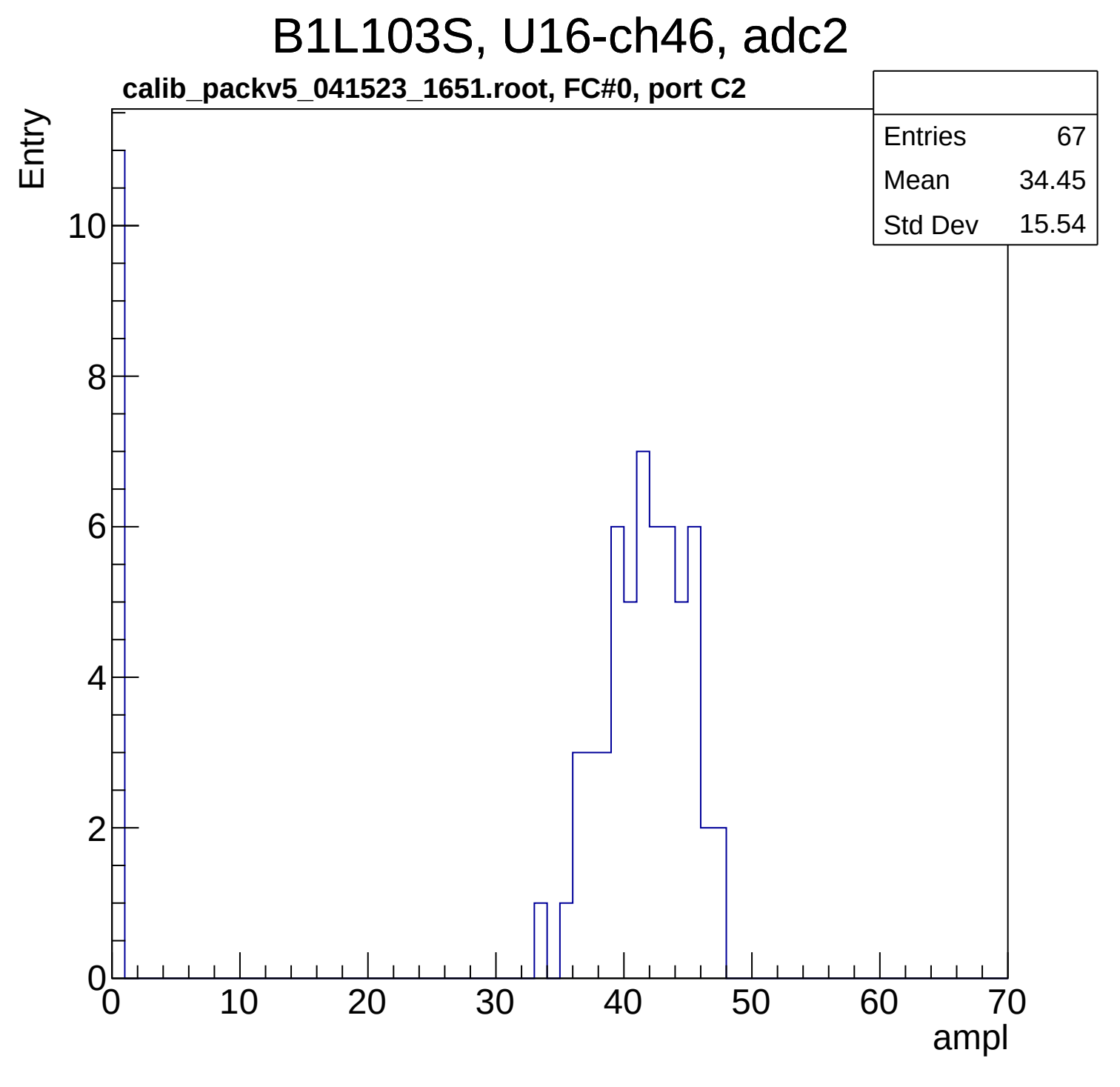
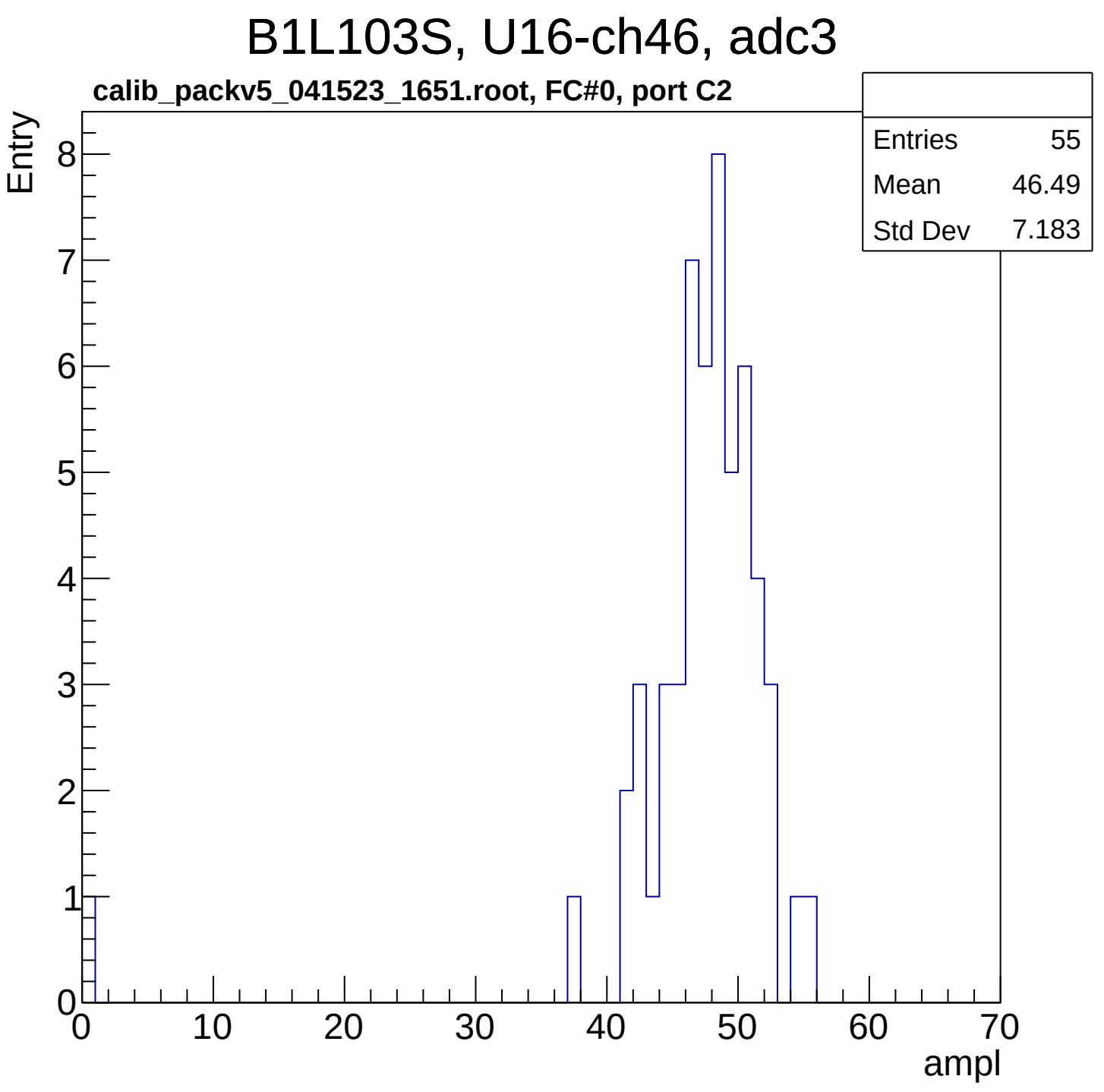
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch46, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 34.45
Std Dev 15.54
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch46, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 46.49
Std Dev 7.183
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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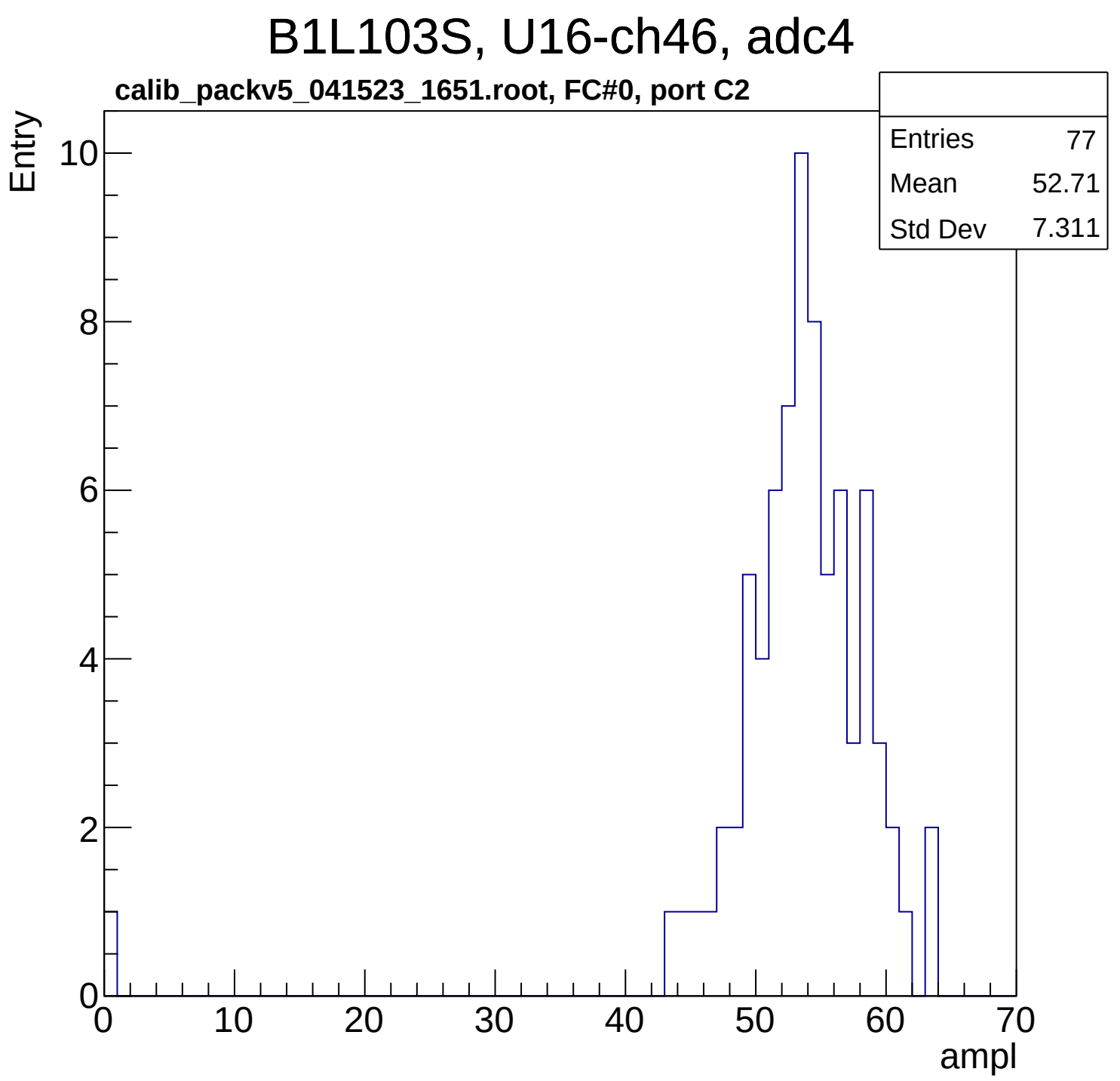
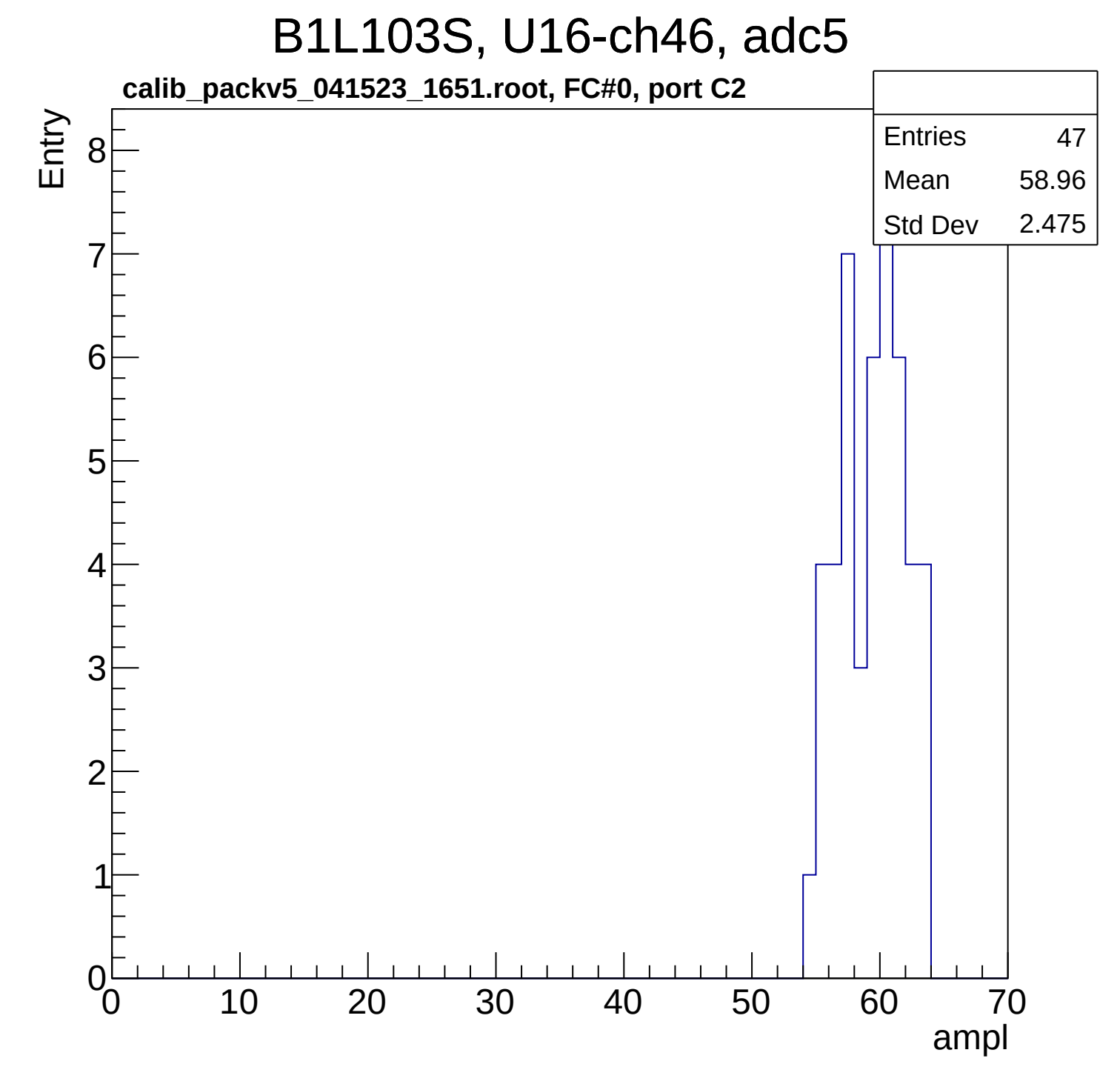
40
50
60
70


B1L103S, U16-ch46, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 52.71
Std Dev 7.311
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch46, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.96
Std Dev 2.475
Entry
ampl
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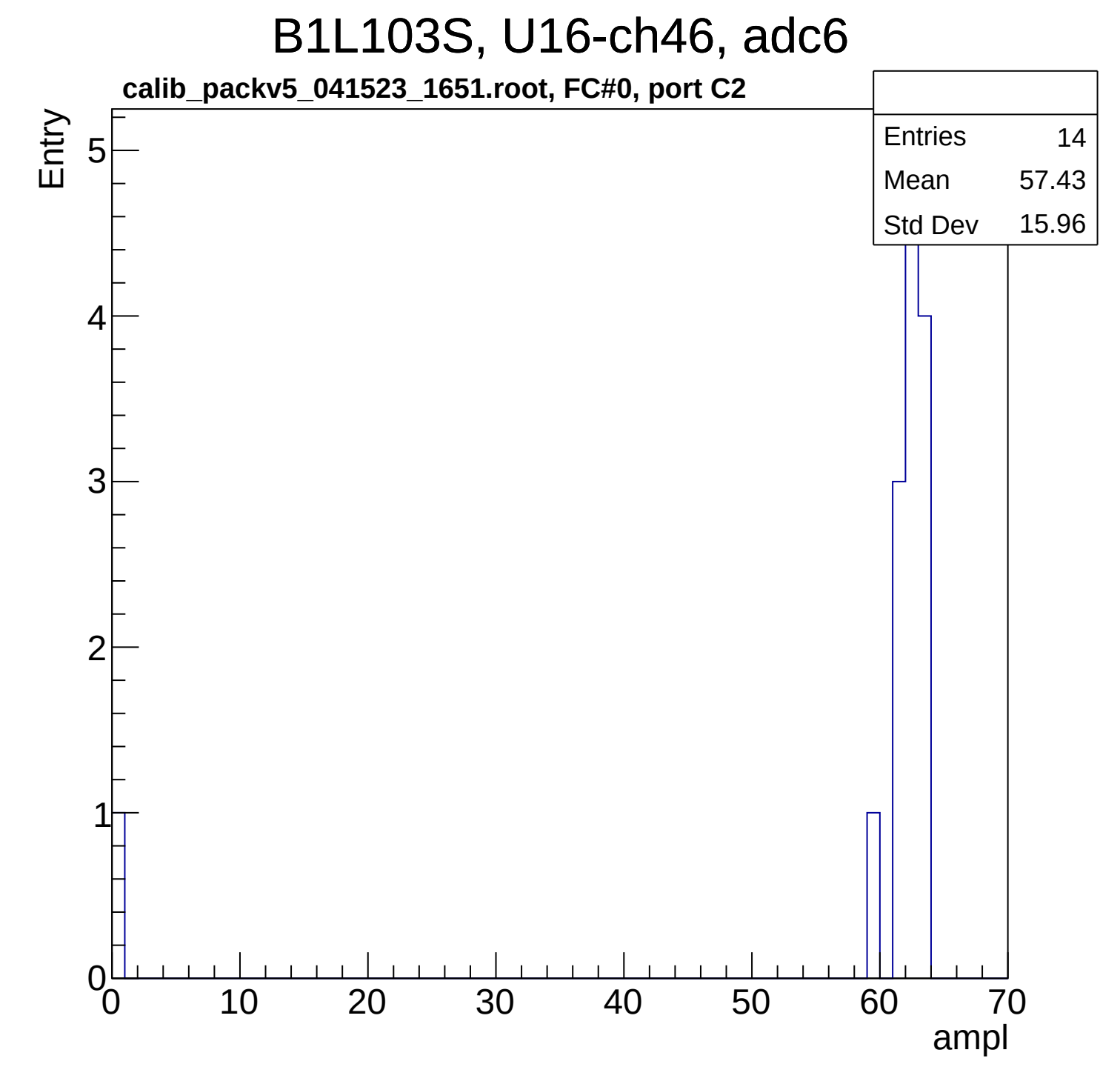
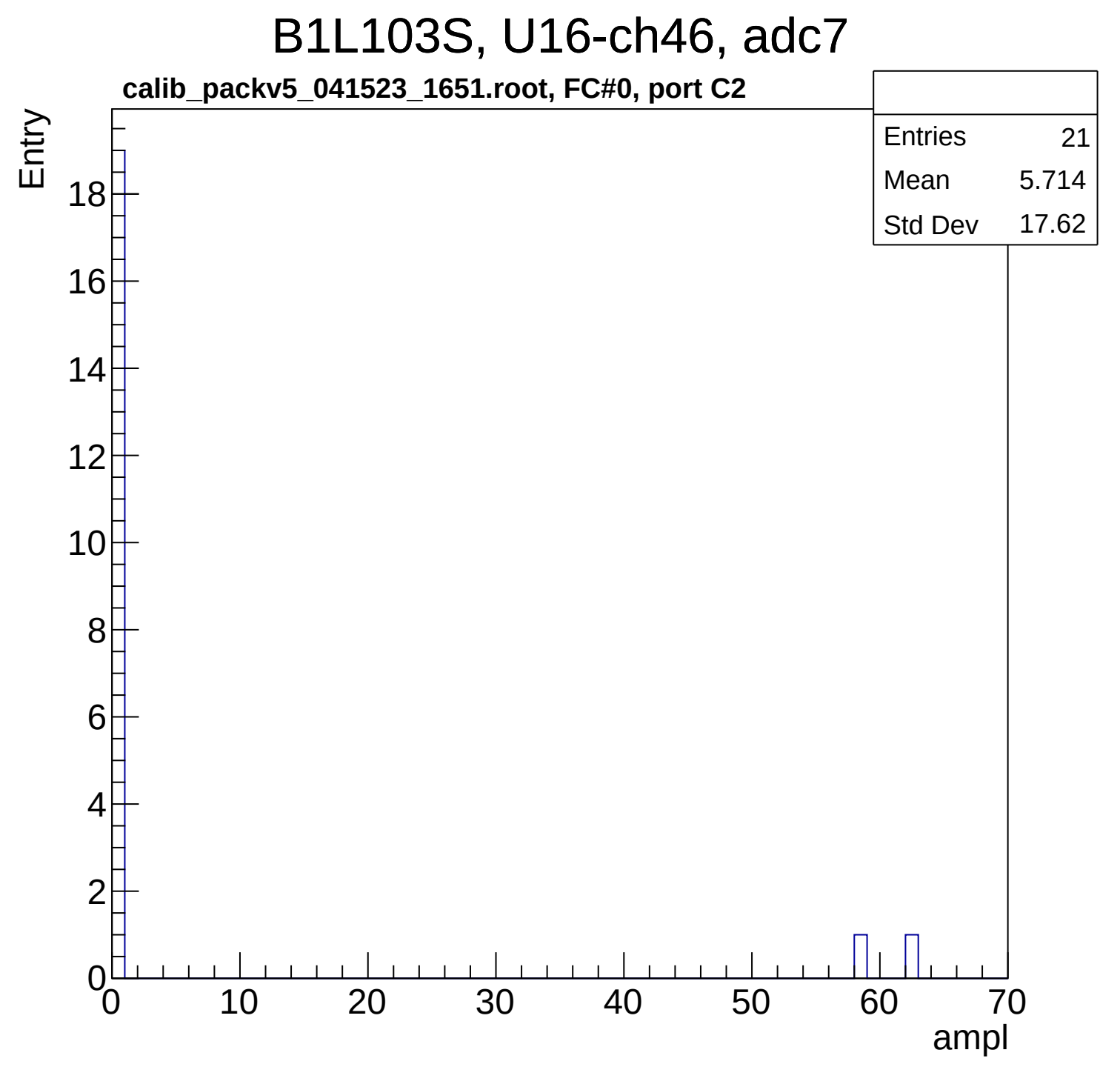
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch46, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 57.43
Std Dev 15.96
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U16-ch46, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.714
Std Dev 17.62
Entry
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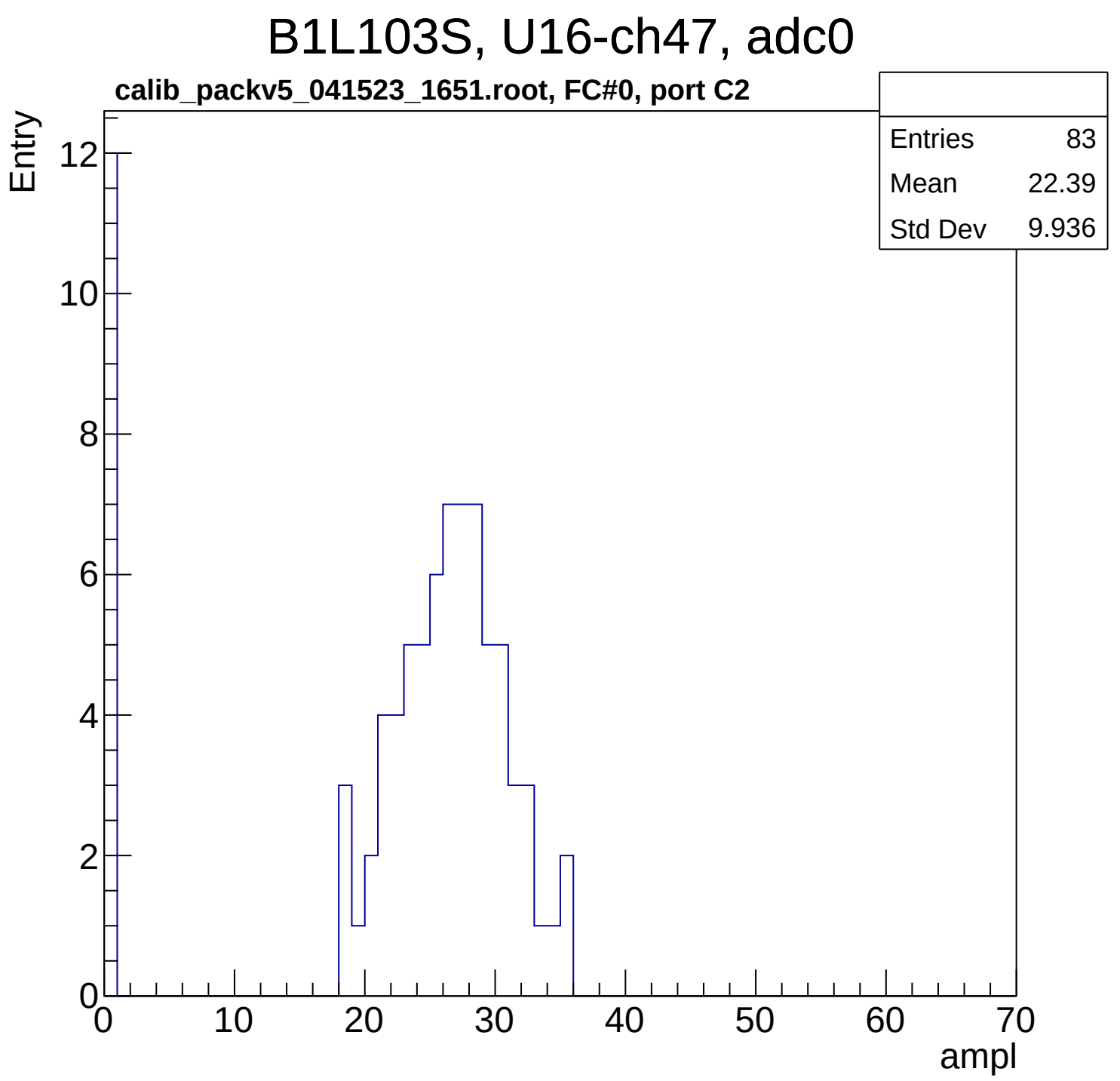
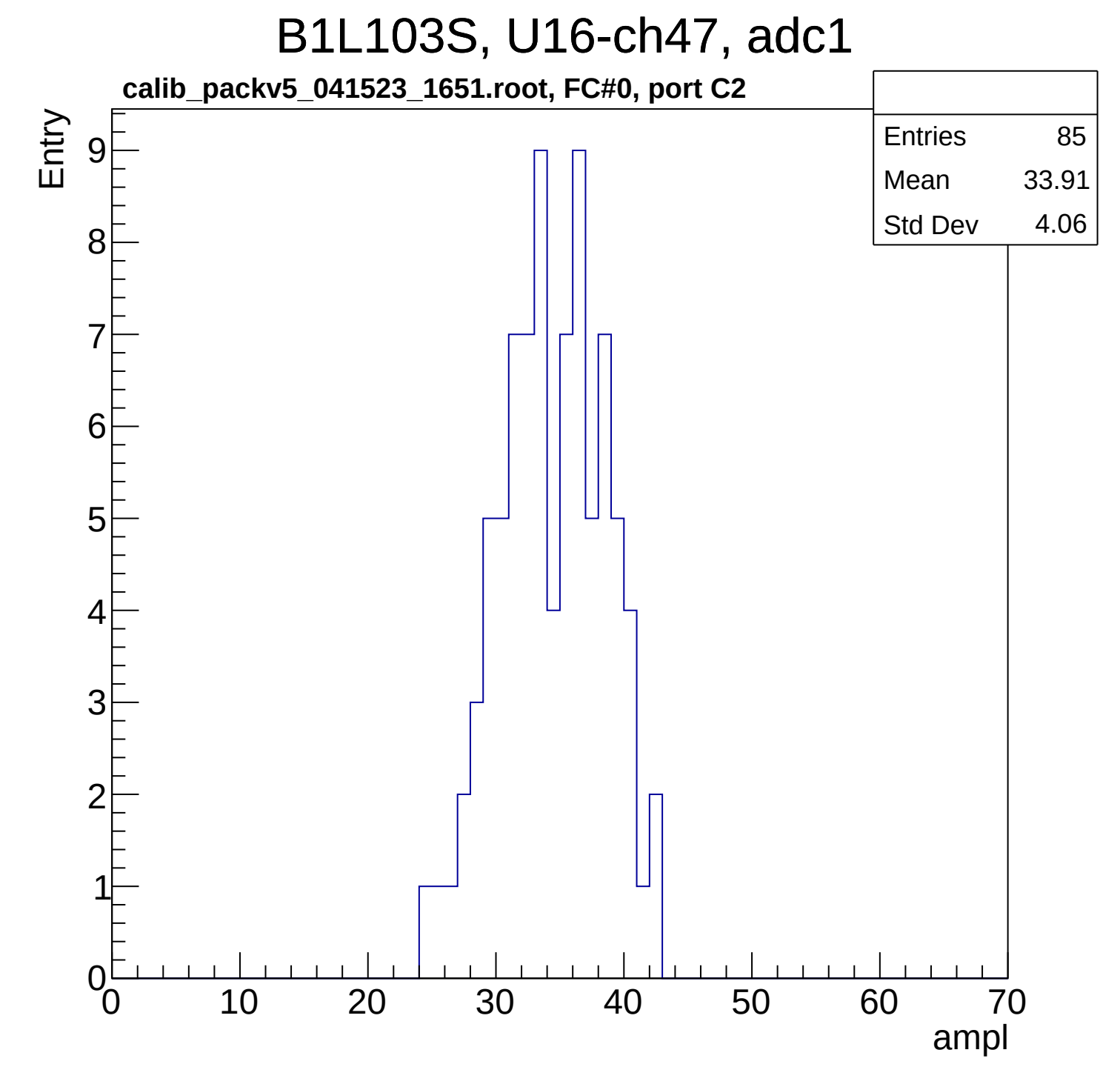
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch47, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 22.39
Std Dev 9.936
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U16-ch47, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 33.91
Std Dev 4.06
Entry
ampl
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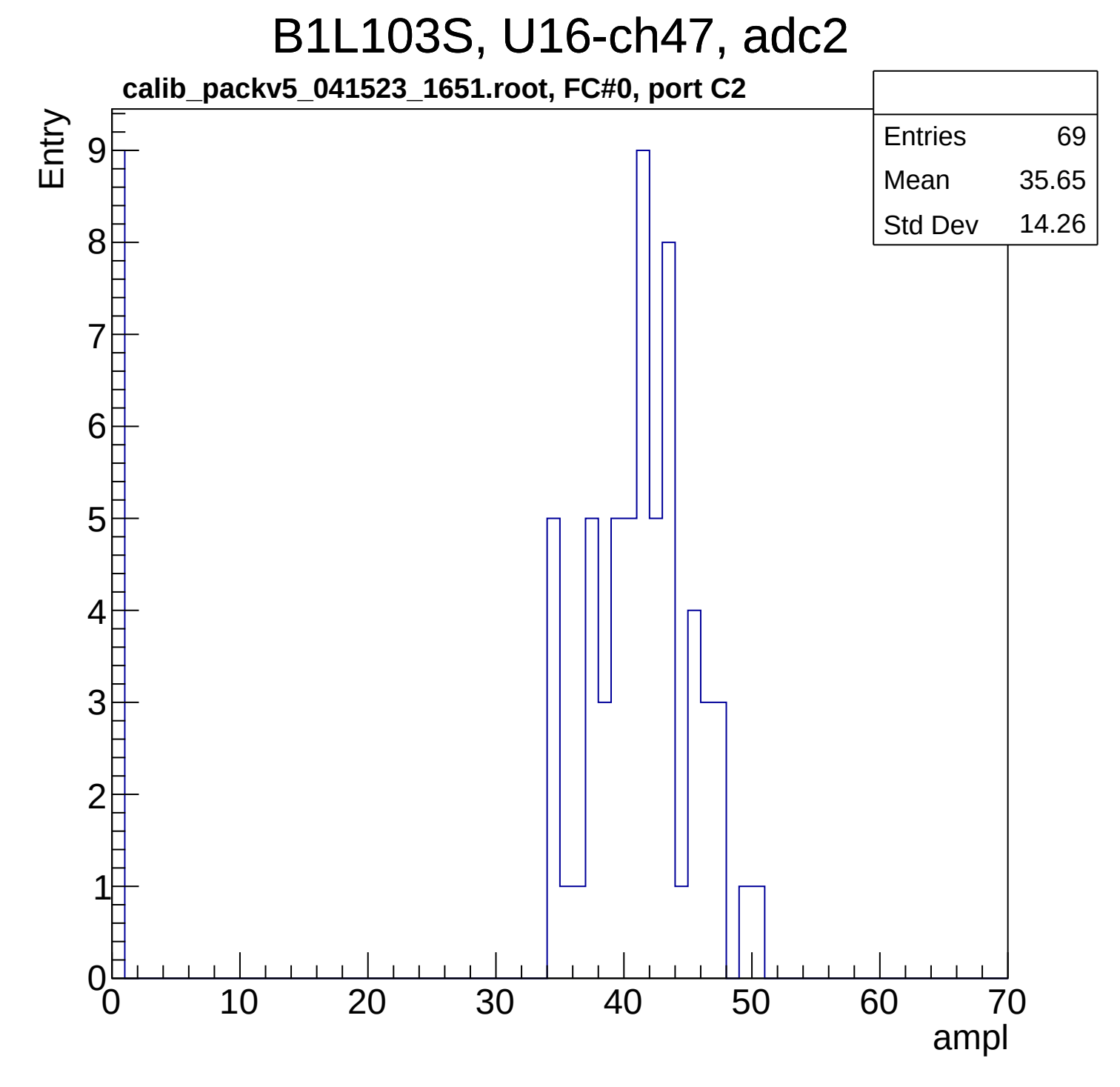
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch47, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 35.65
Std Dev 14.26
Entry
ampl
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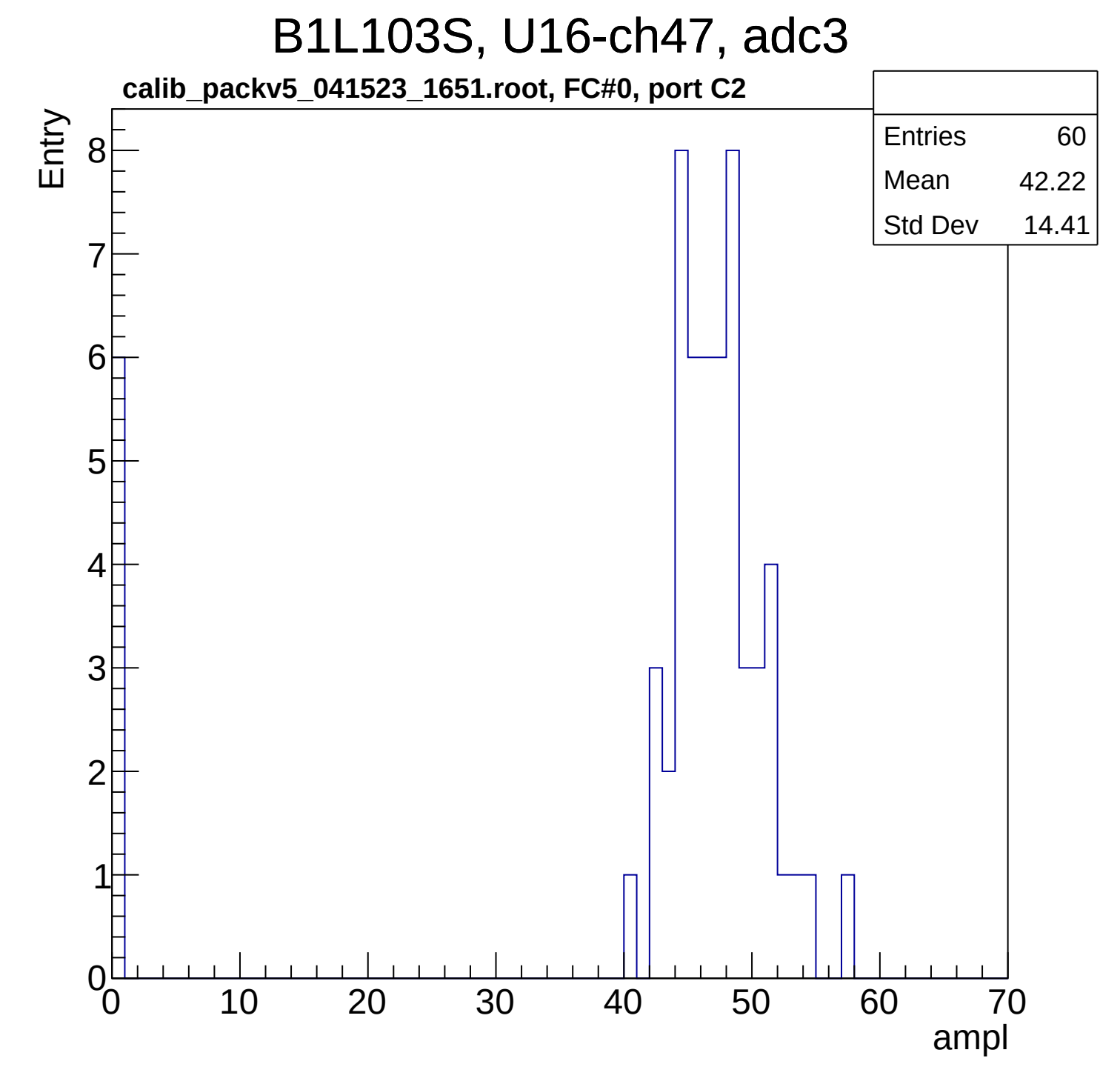
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch47, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 42.22
Std Dev 14.41
Entry
ampl
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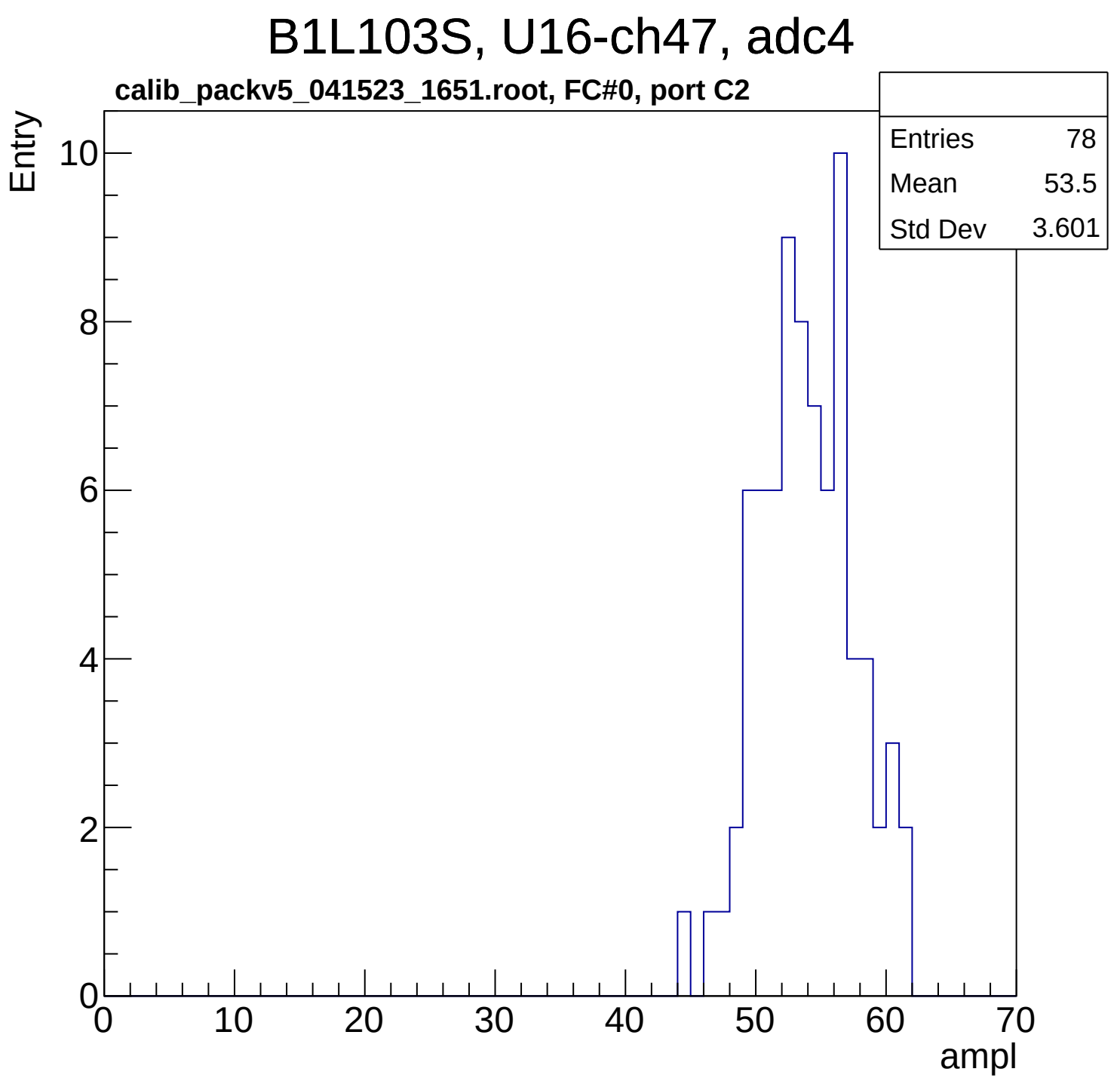
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch47, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 53.5
Std Dev 3.601
Entry
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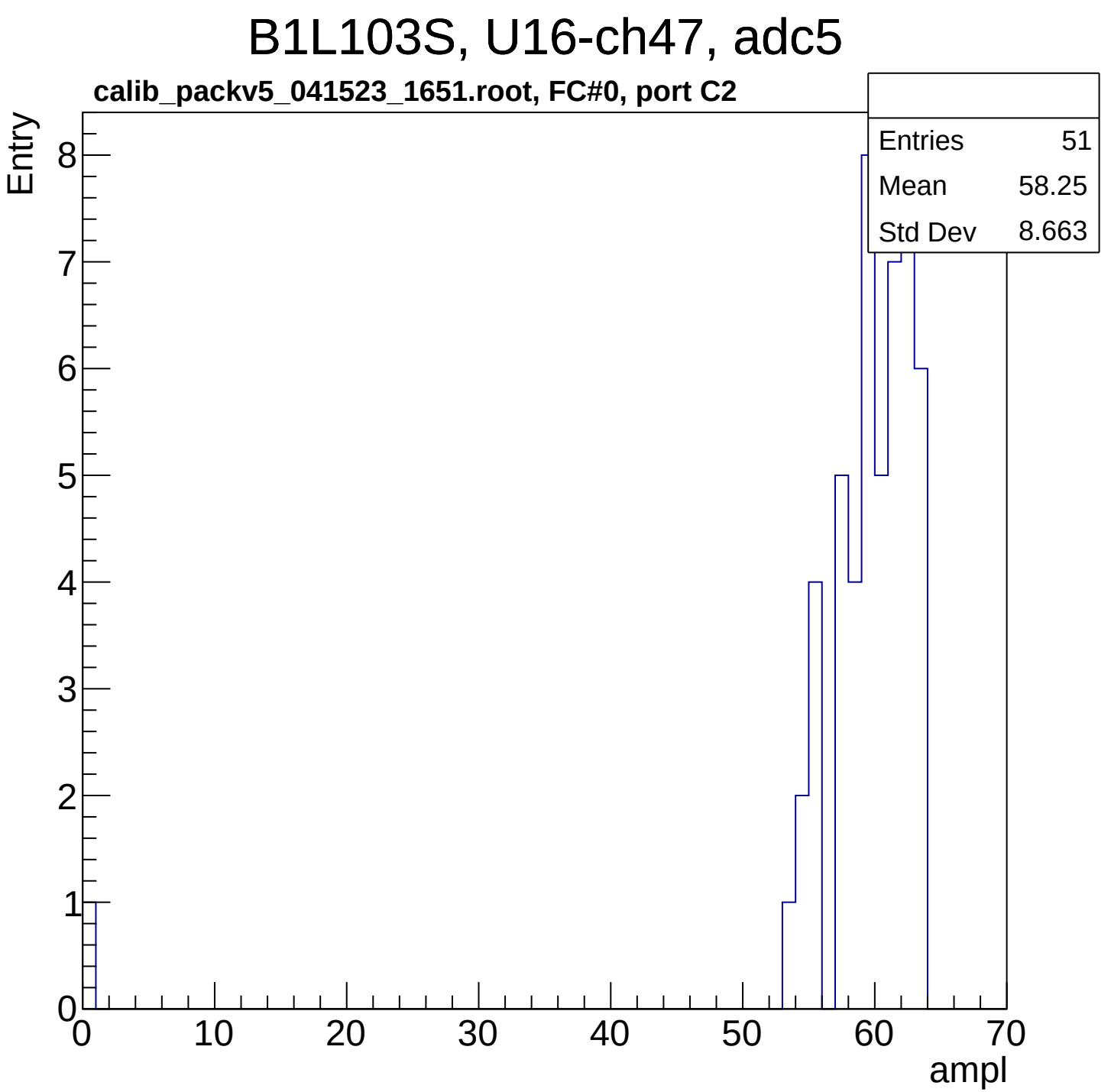
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch47, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.25
Std Dev 8.663
Entry
ampl
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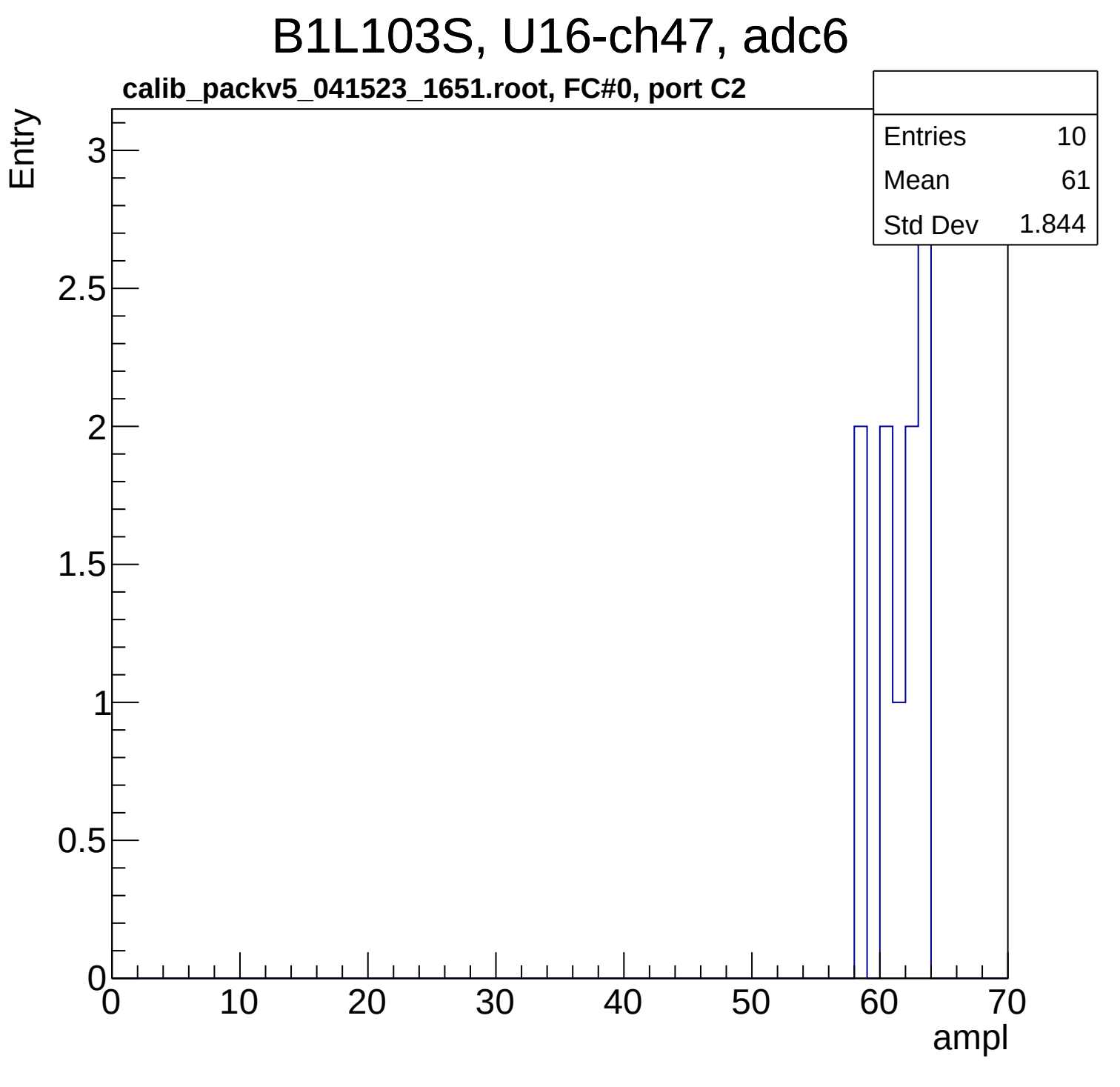
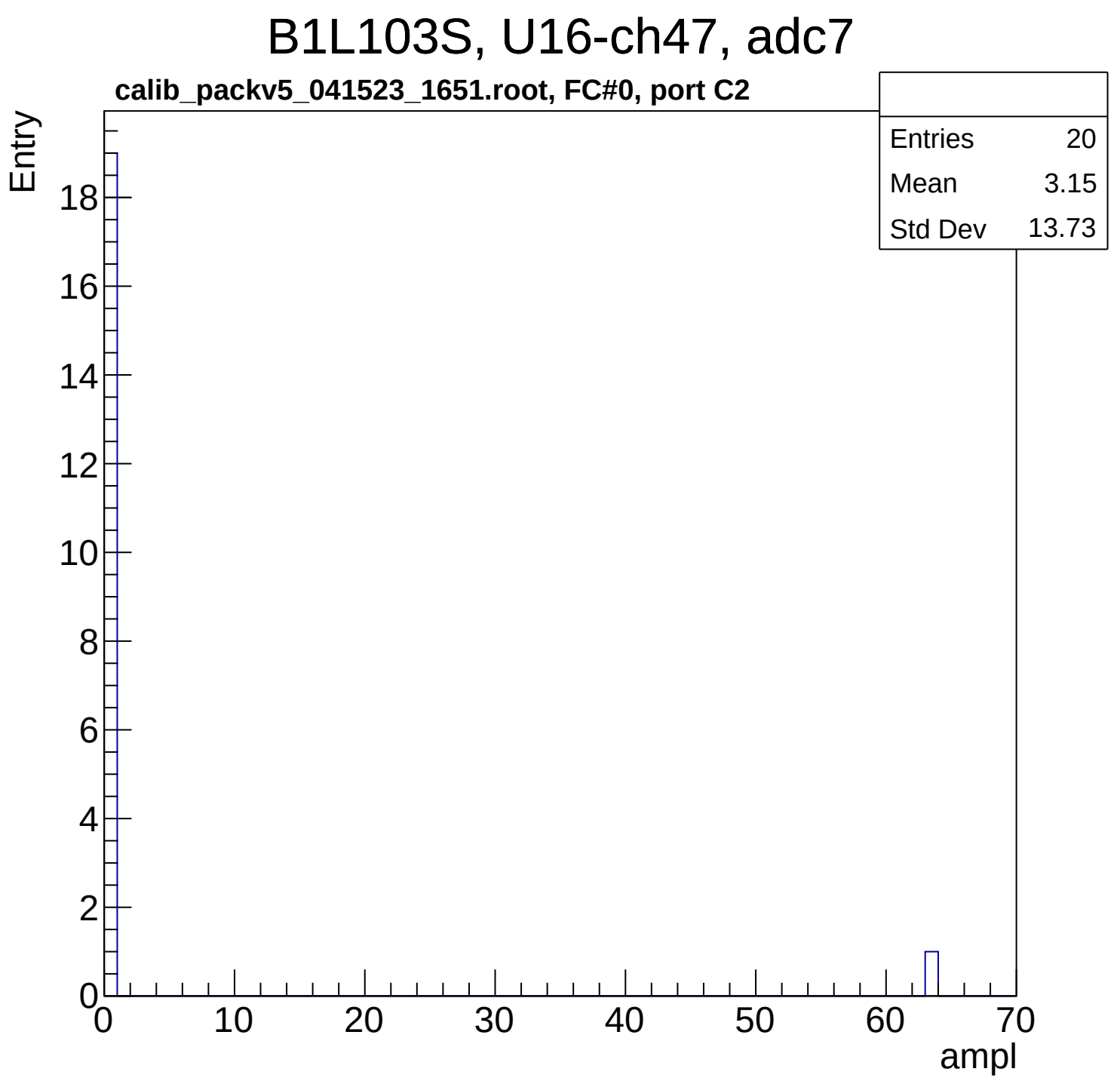
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch47, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61
Std Dev 1.844
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U16-ch47, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
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6
8
10
12
14
16
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10
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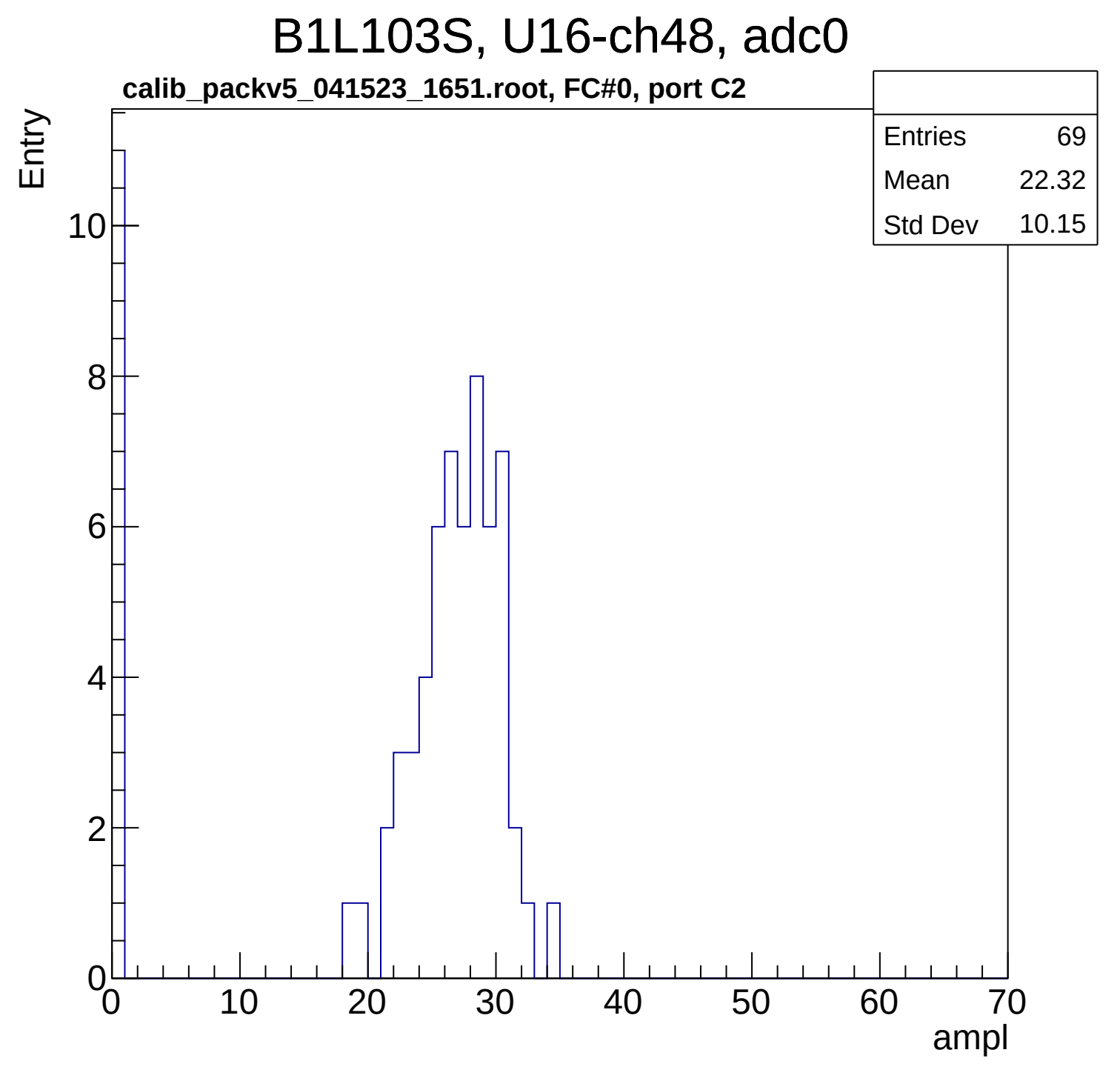
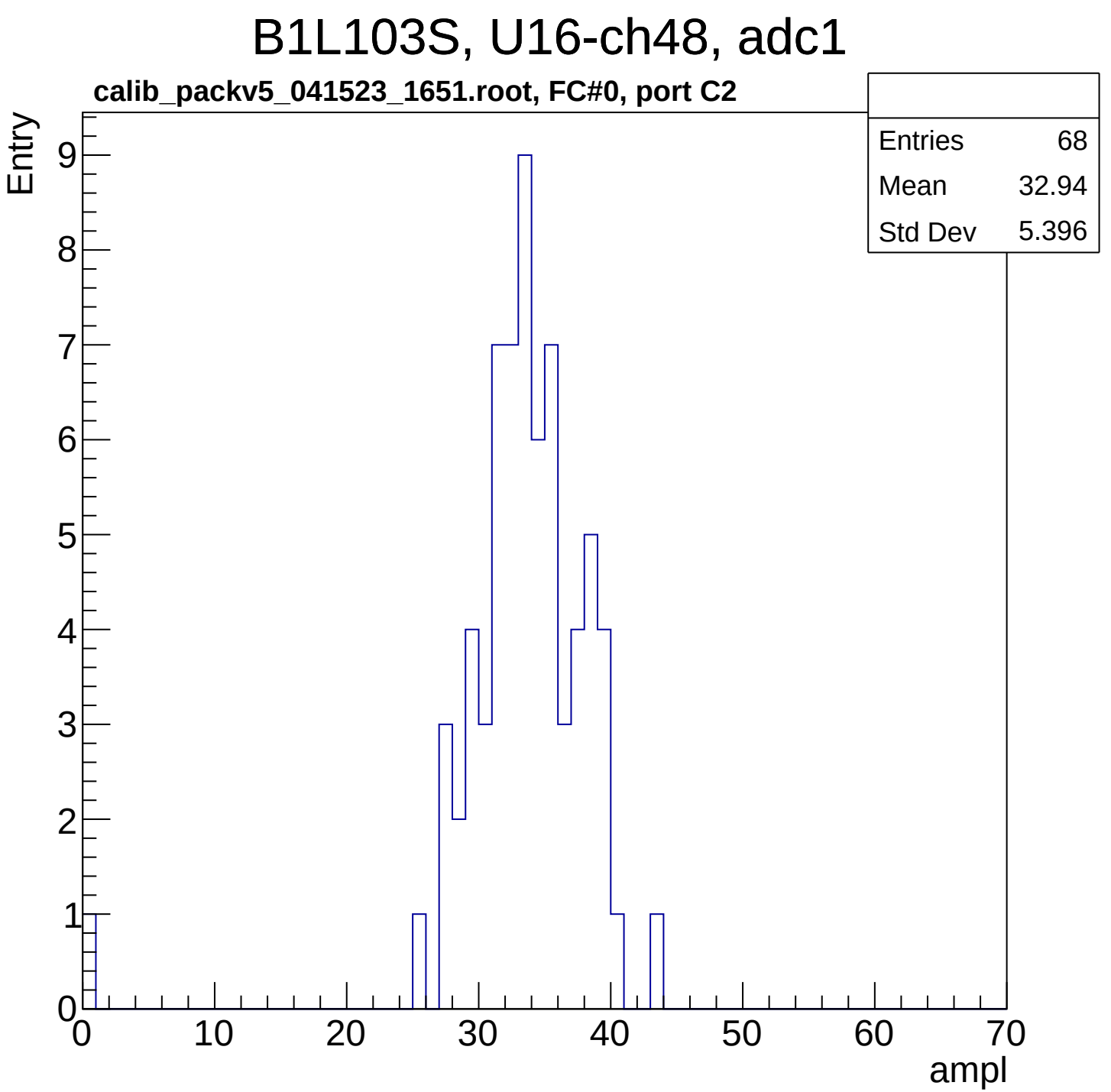
50
60
70
ampl


B1L103S, U16-ch48, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 22.32
Std Dev 10.15
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch48, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 32.94
Std Dev 5.396
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
30
40
50
60
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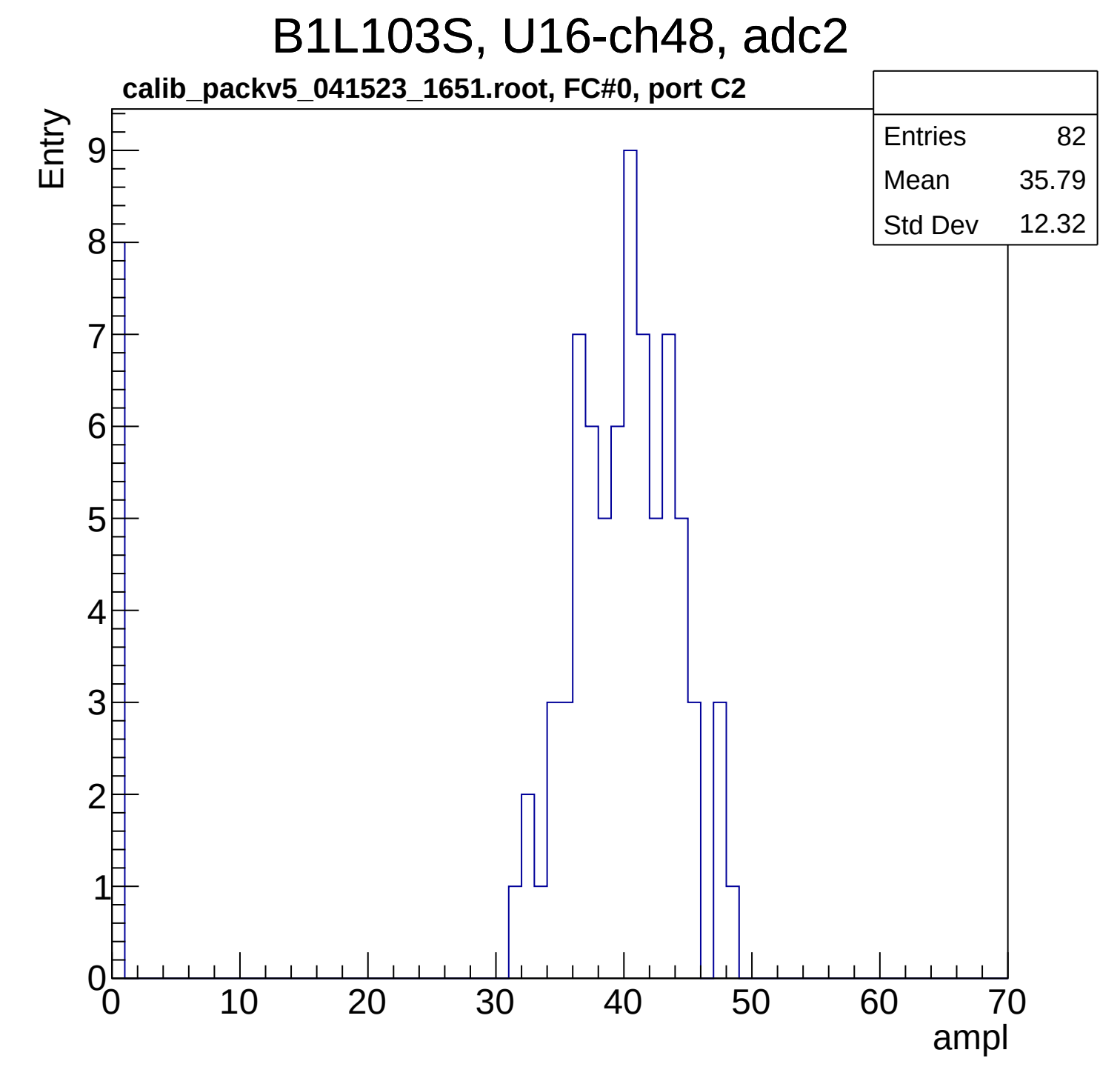
B1L103S, U16-ch48, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 35.79
Std Dev 12.32
Entry
ampl
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3
4
5
6
7
8
9
0
10
20
30
40
50
60
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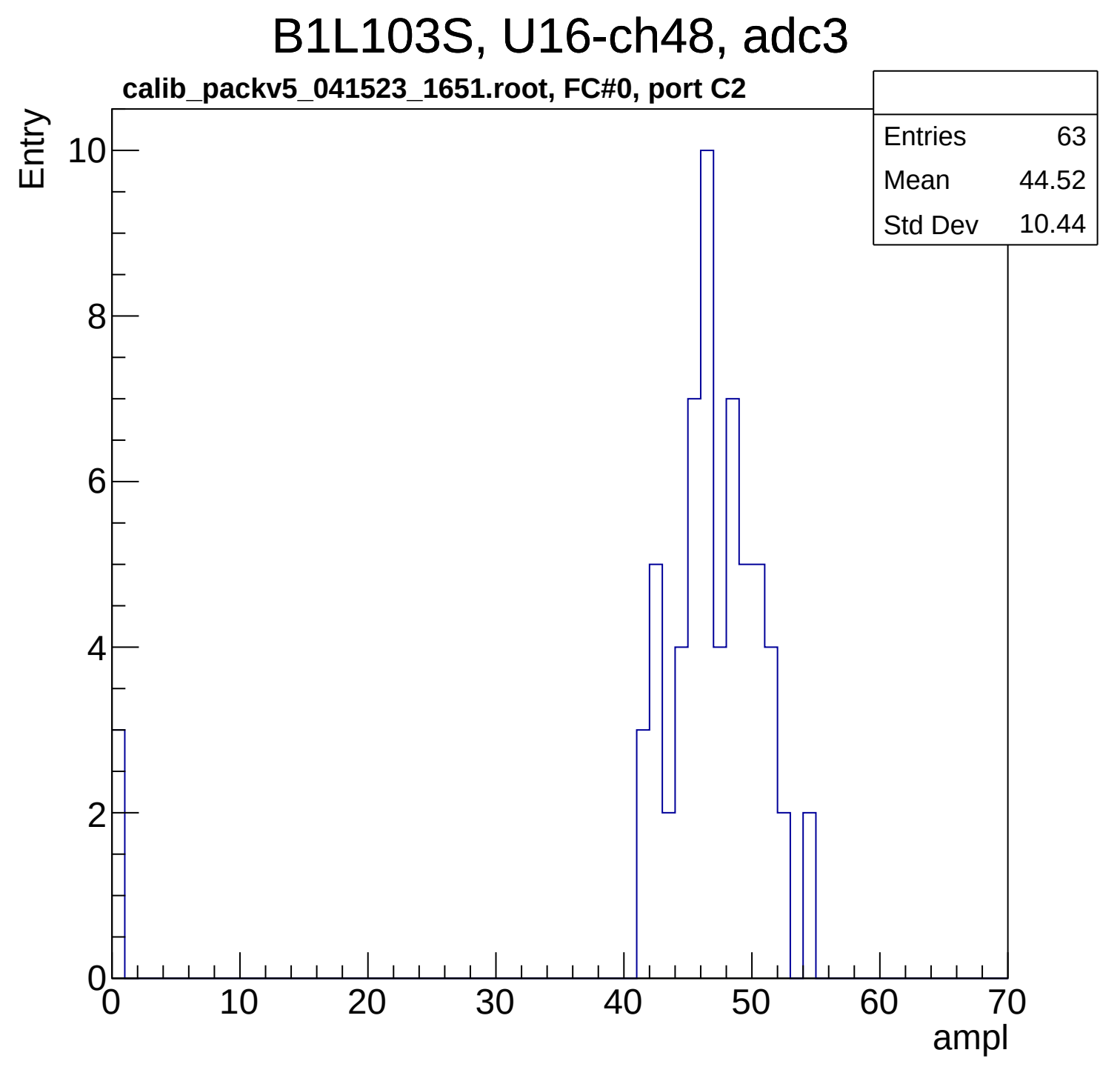
B1L103S, U16-ch48, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 44.52
Std Dev 10.44
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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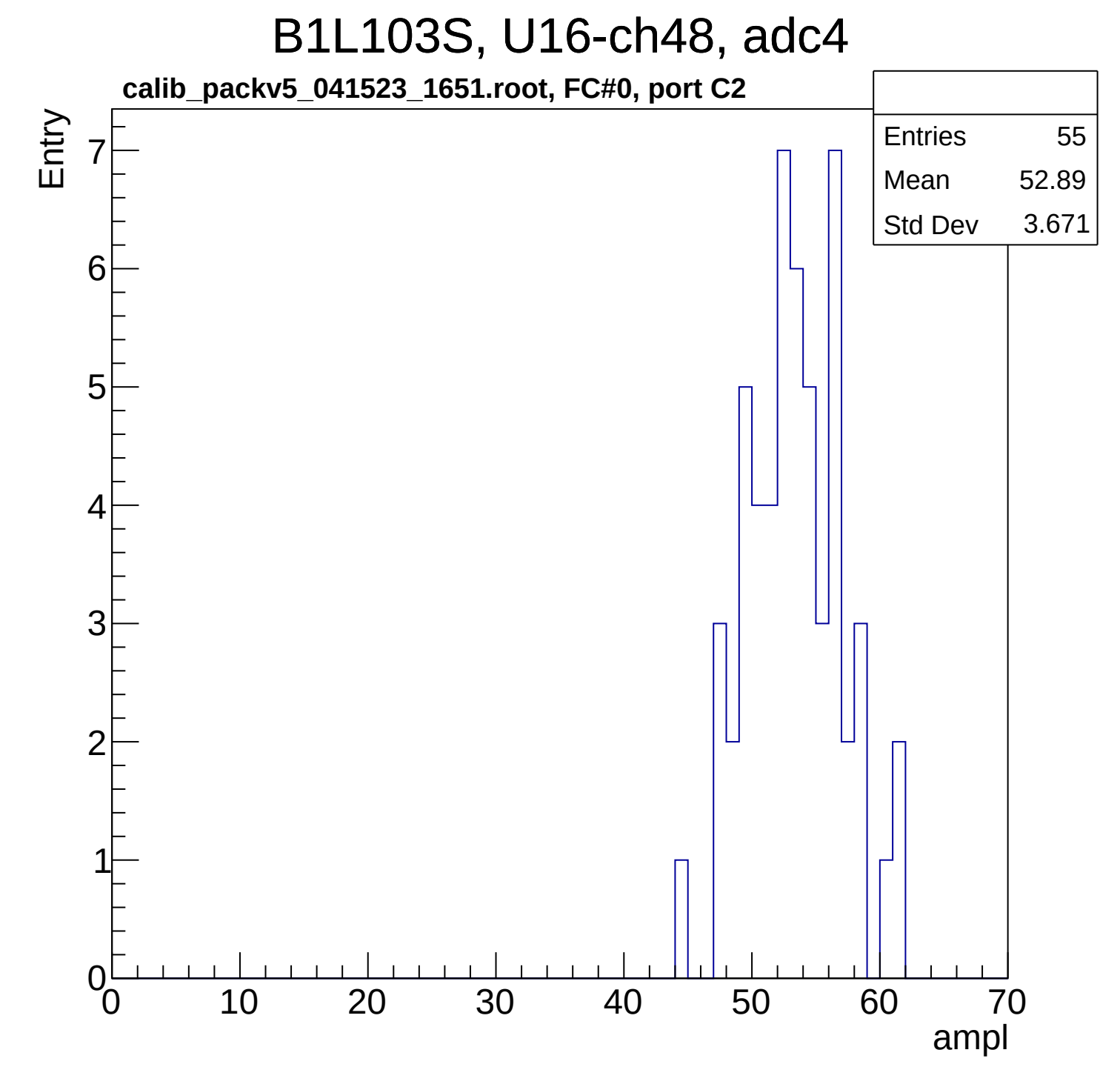
B1L103S, U16-ch48, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 52.89
Std Dev 3.671
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
50
60
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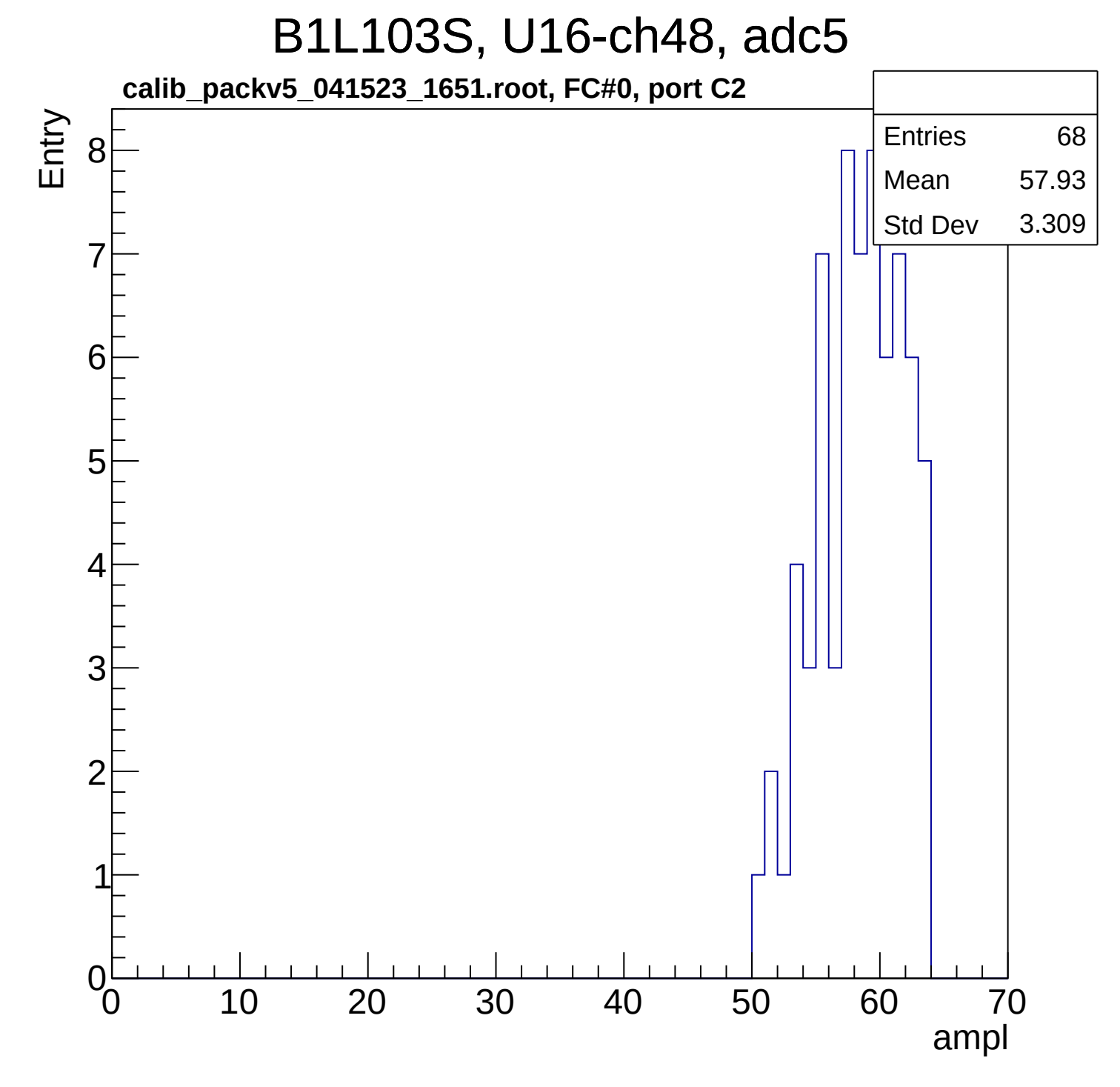
B1L103S, U16-ch48, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 57.93
Std Dev 3.309
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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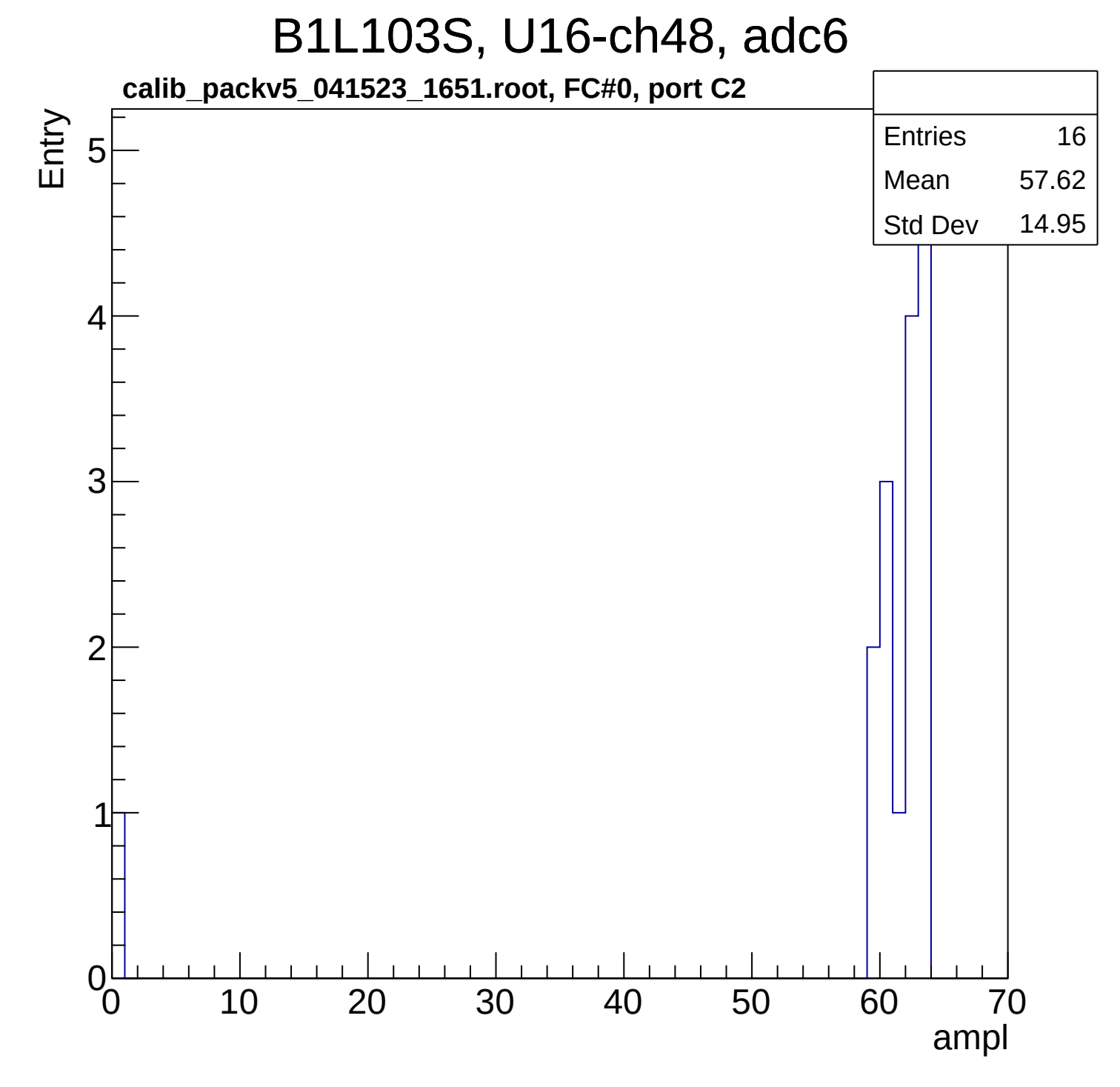
B1L103S, U16-ch48, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.62
Std Dev 14.95
Entry
ampl
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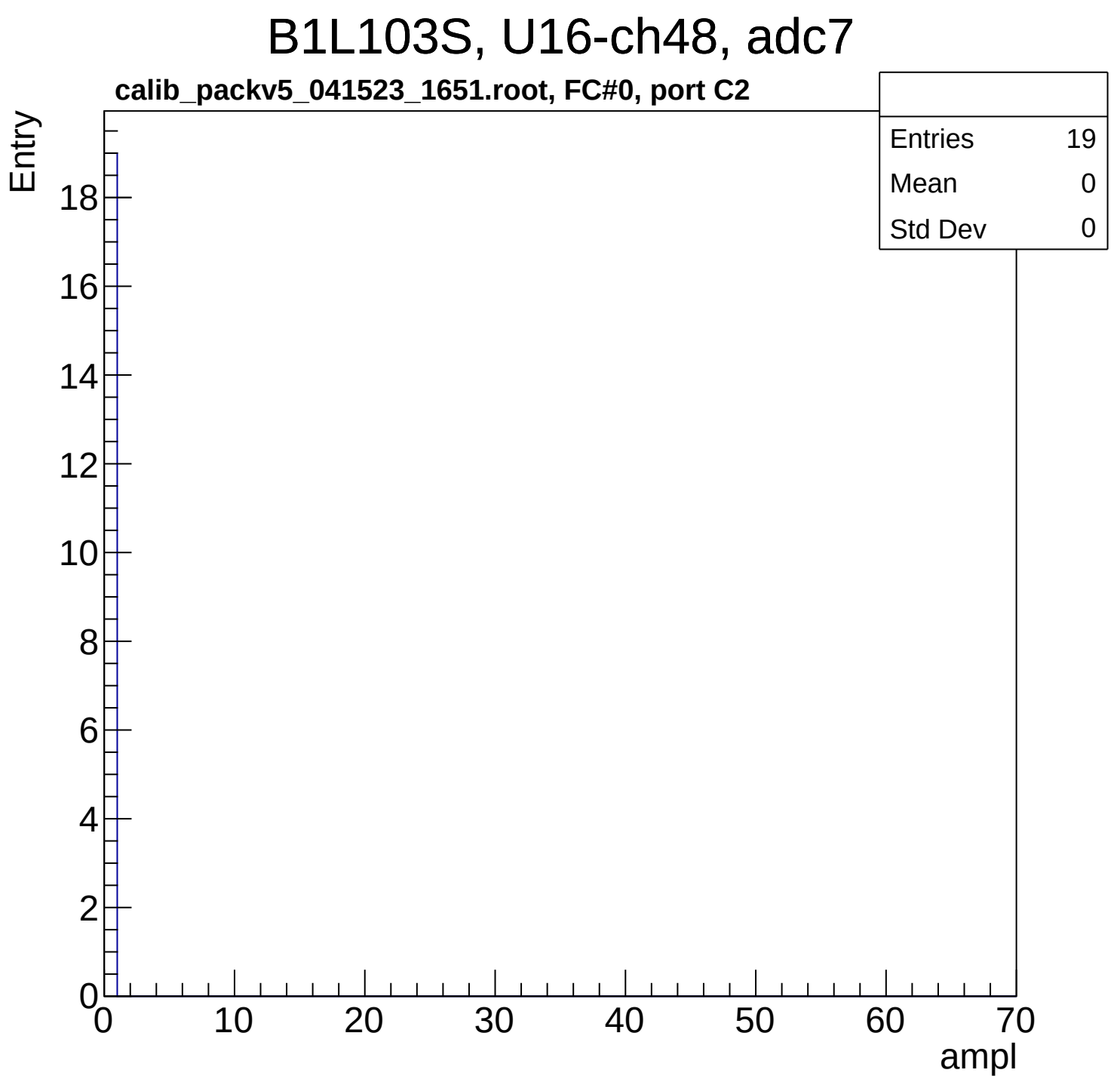
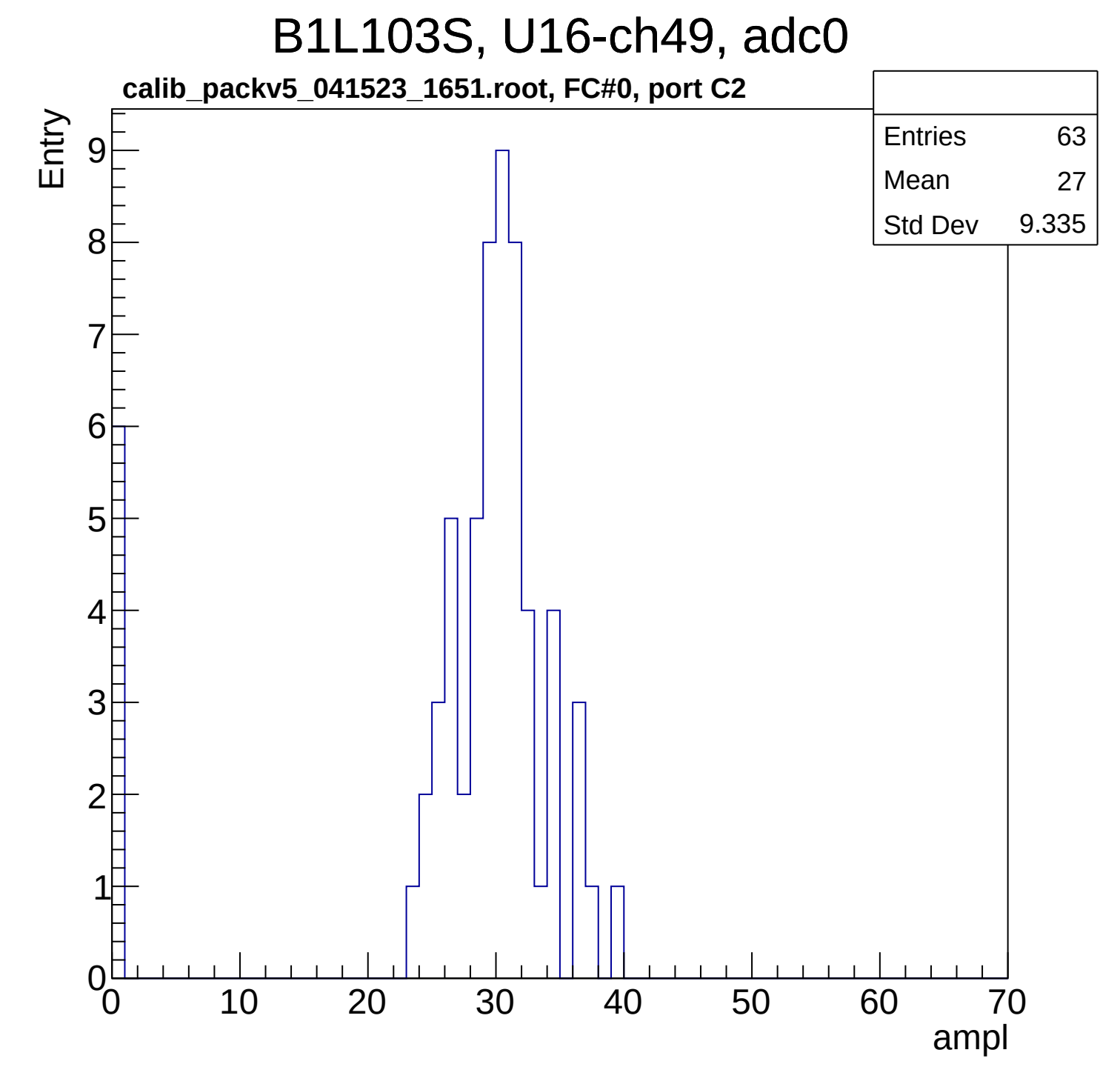
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U16-ch48, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch49, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 27
Std Dev 9.335
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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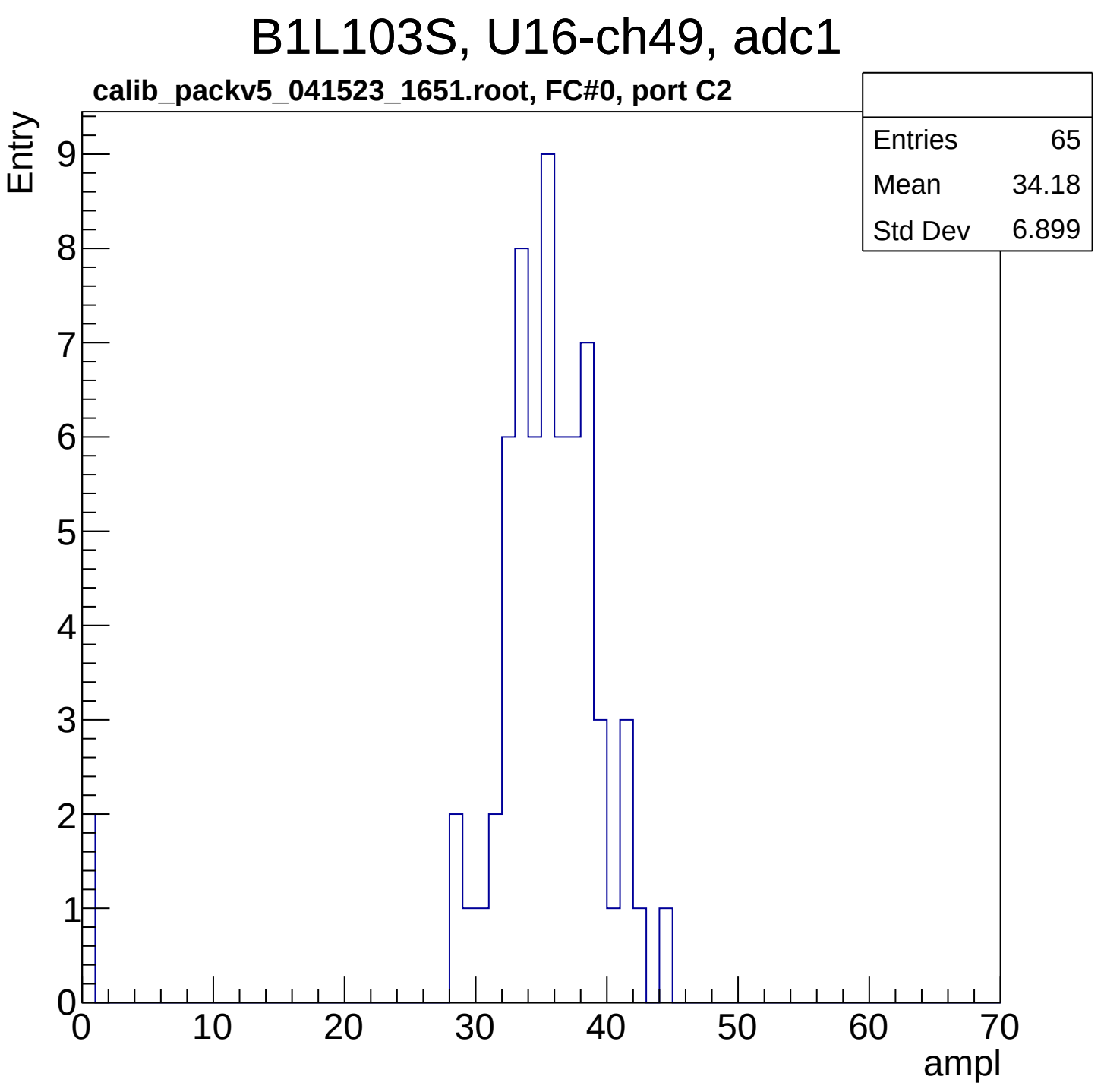
B1L103S, U16-ch49, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 34.18
Std Dev 6.899
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
50
60
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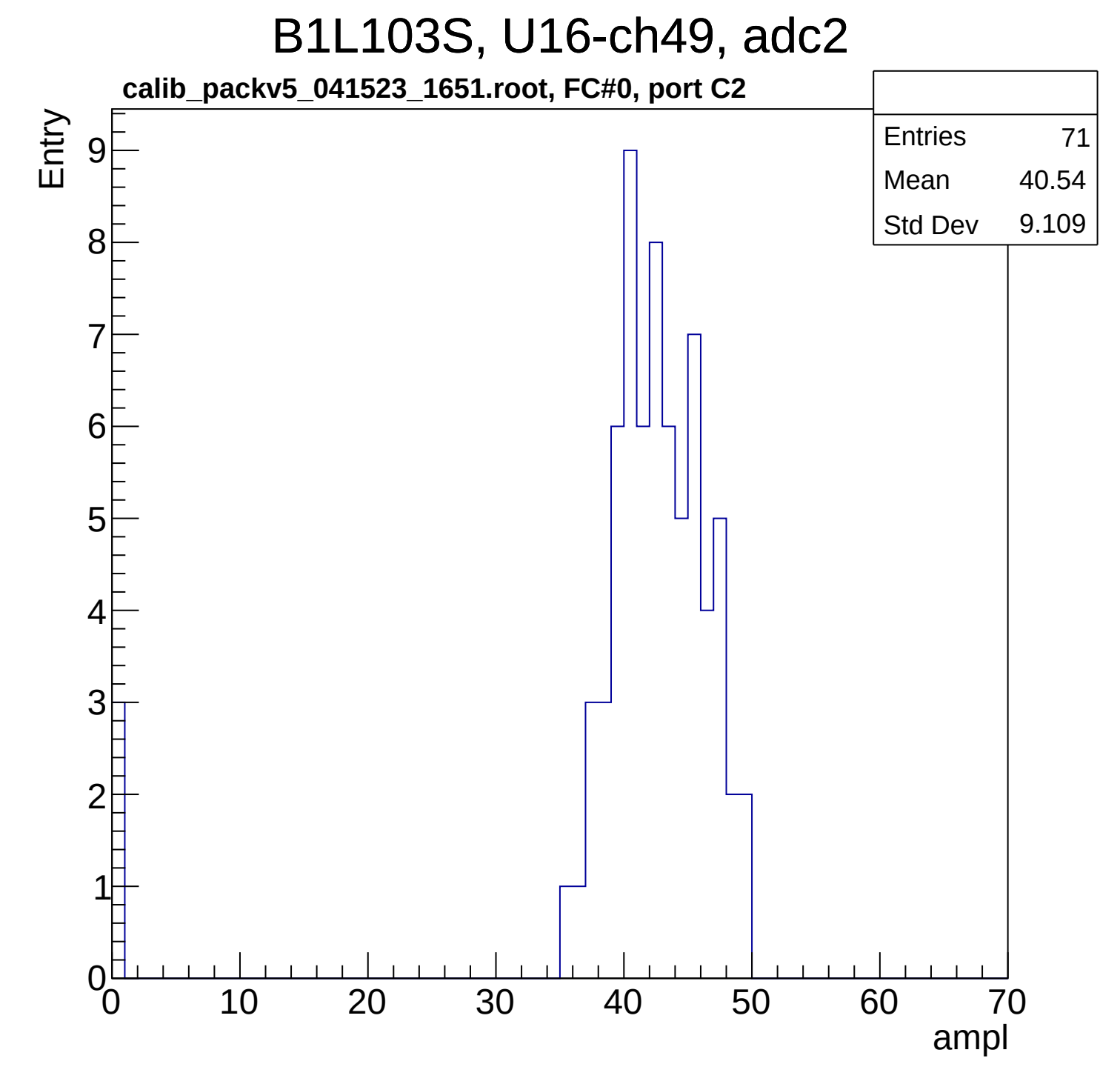
B1L103S, U16-ch49, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 40.54
Std Dev 9.109
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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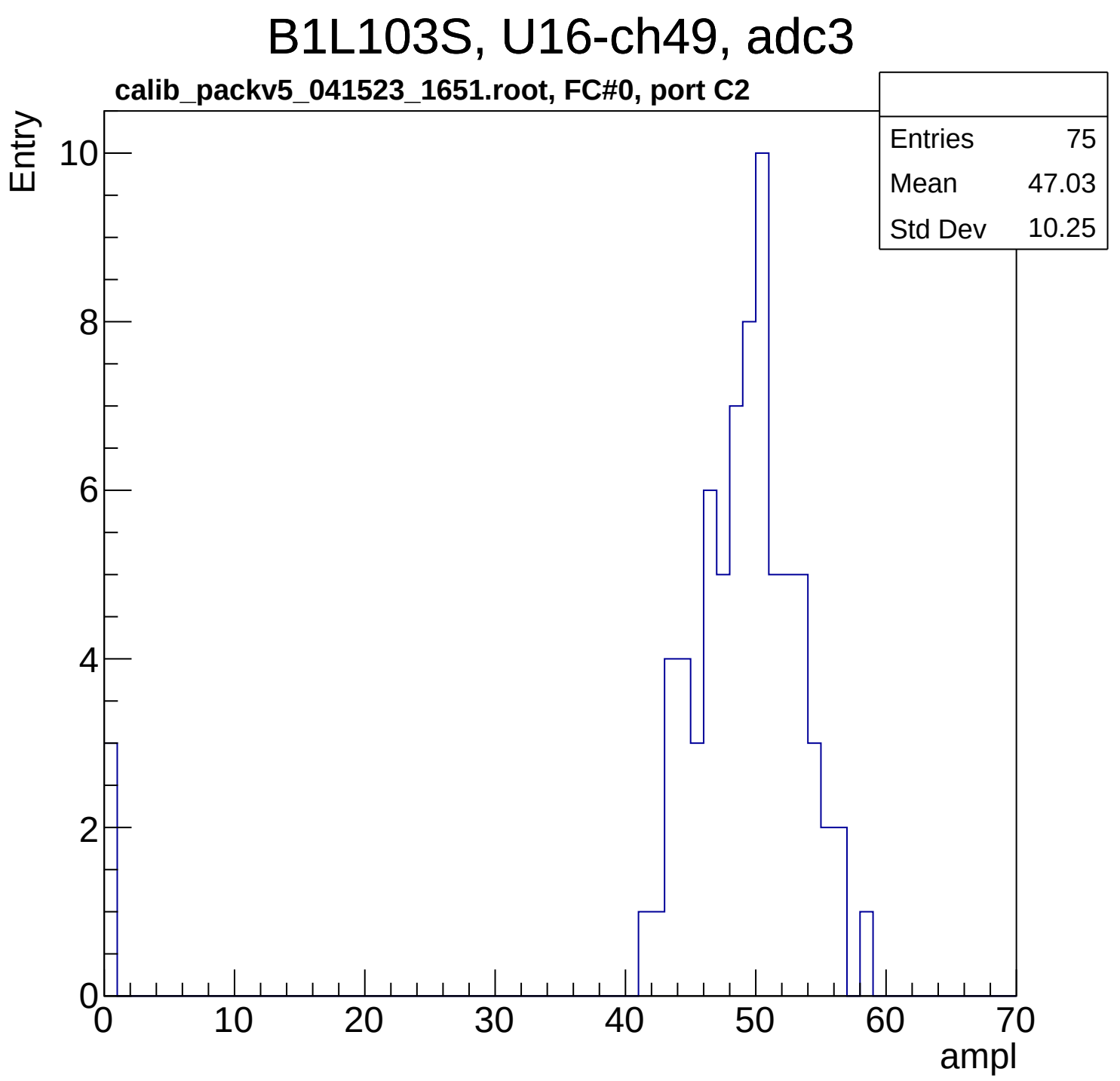
B1L103S, U16-ch49, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 47.03
Std Dev 10.25
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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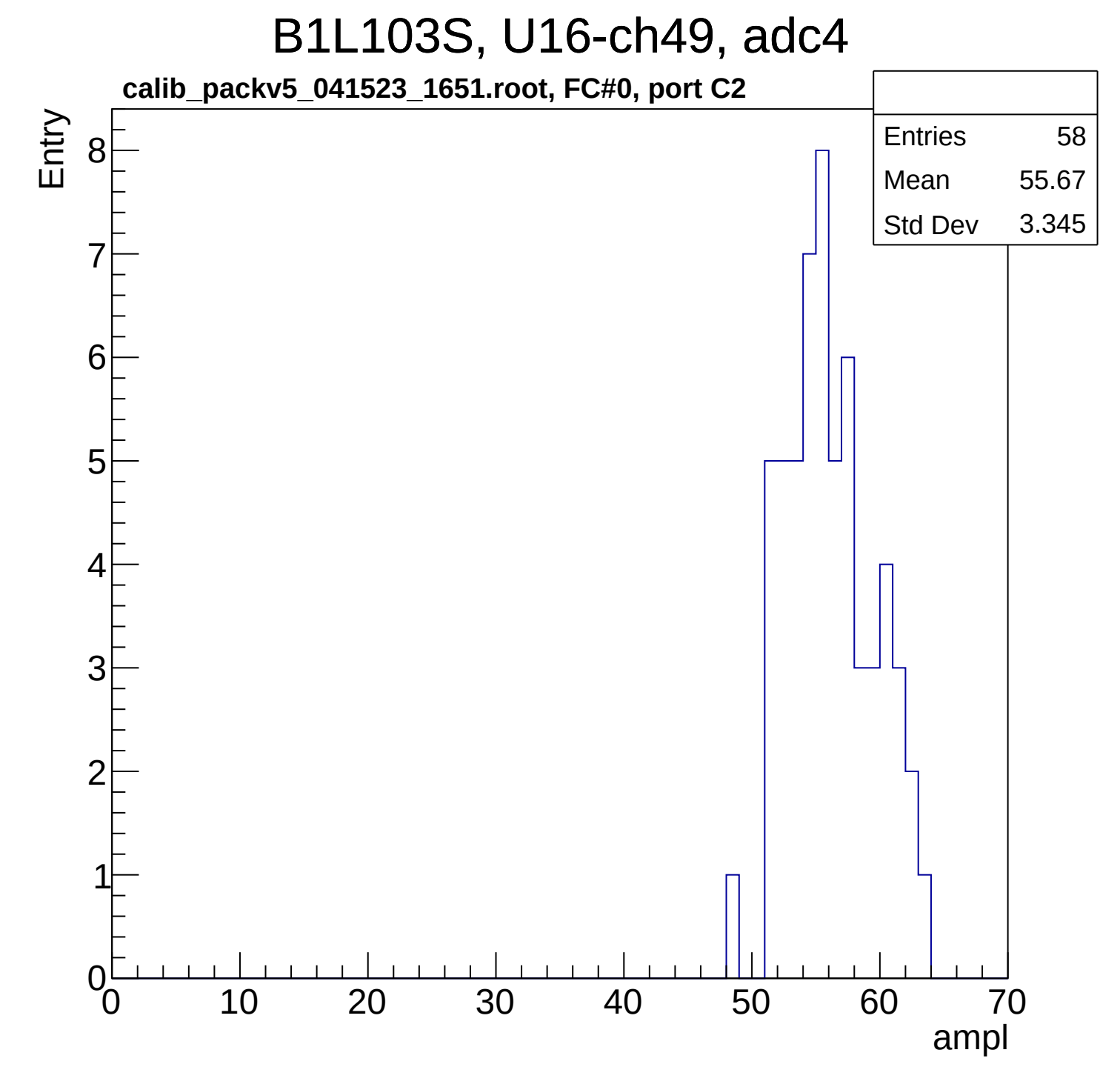
B1L103S, U16-ch49, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 55.67
Std Dev 3.345
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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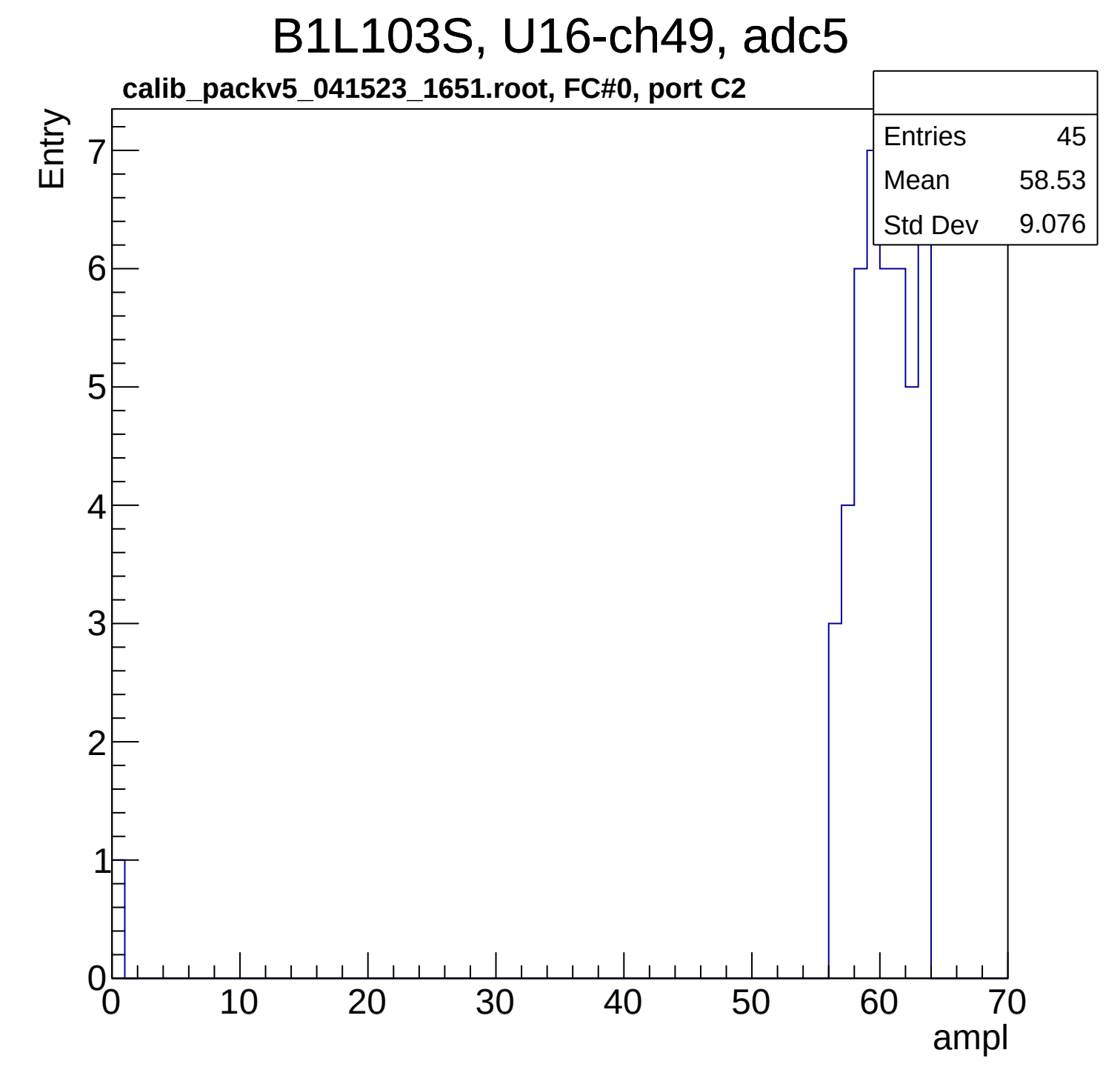
B1L103S, U16-ch49, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.53
Std Dev 9.076
Entry
ampl
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1
2
3
4
5
6
7
0
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40
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60
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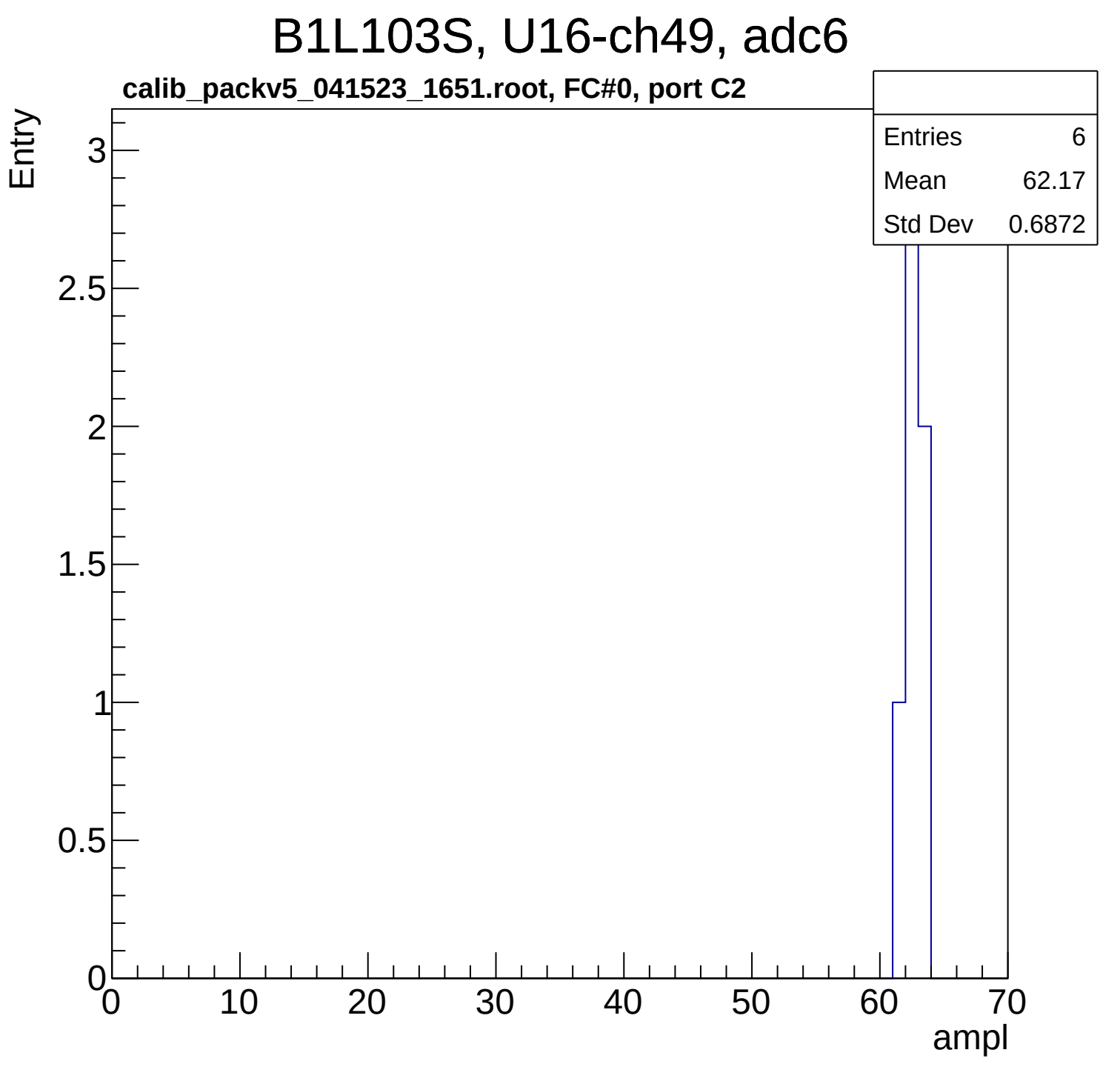
B1L103S, U16-ch49, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.17
Std Dev 0.6872
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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40
50
60
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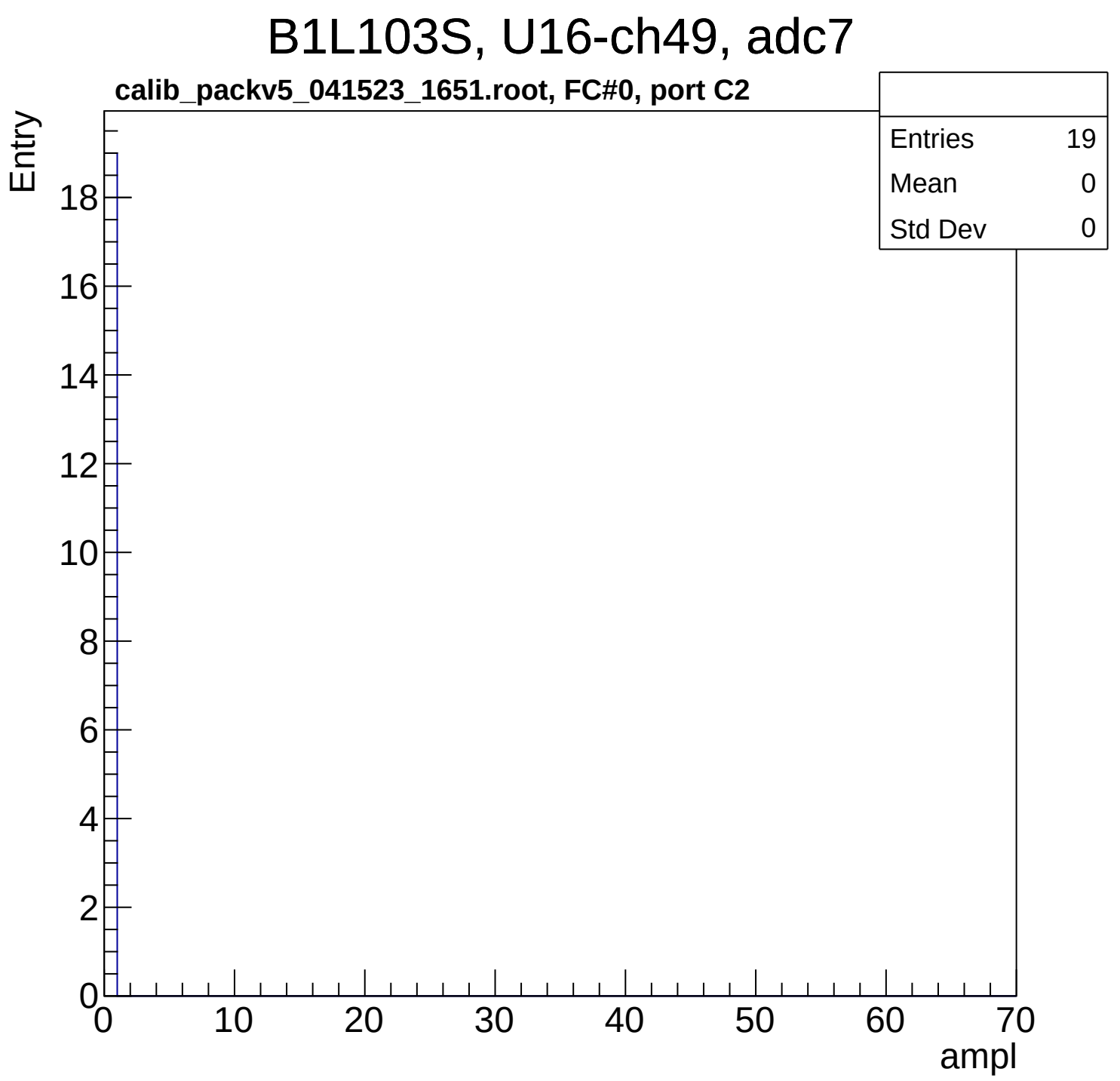
B1L103S, U16-ch49, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
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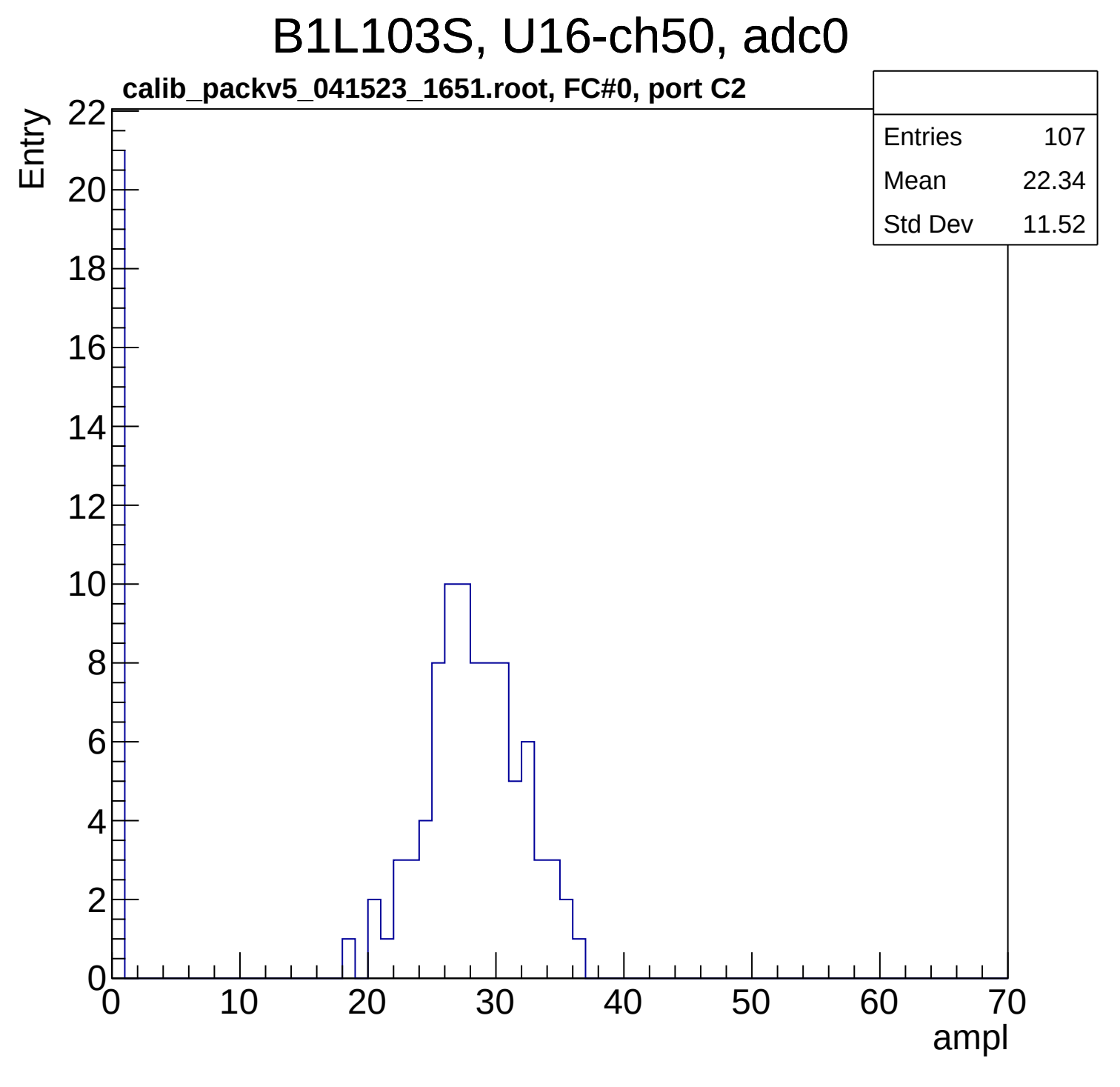
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch50, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 107
Mean 22.34
Std Dev 11.52
Entry
ampl
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8
10
12
14
16
18
20
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0
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20
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40
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60
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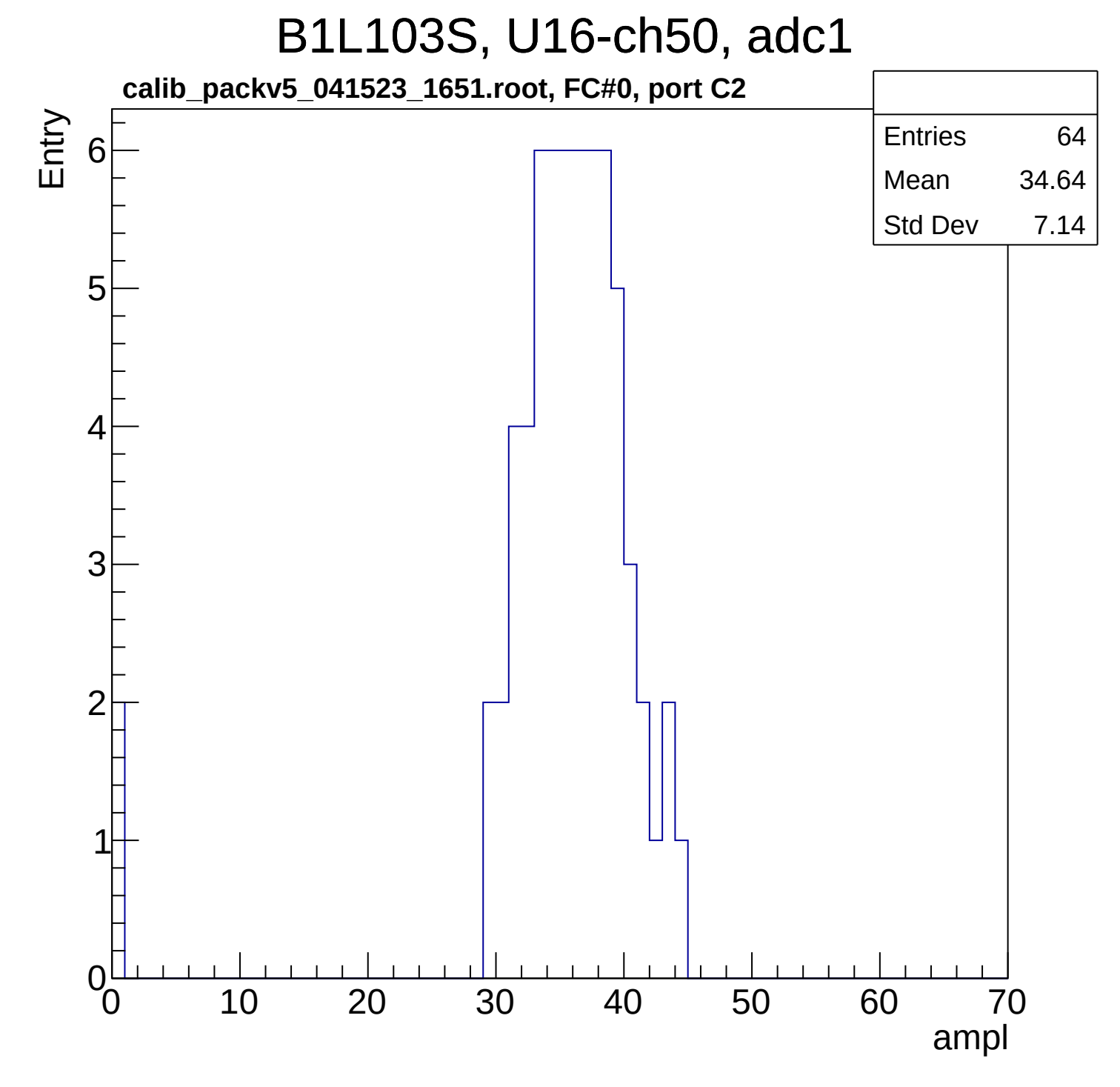
B1L103S, U16-ch50, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 34.64
Std Dev 7.14
Entry
ampl
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40
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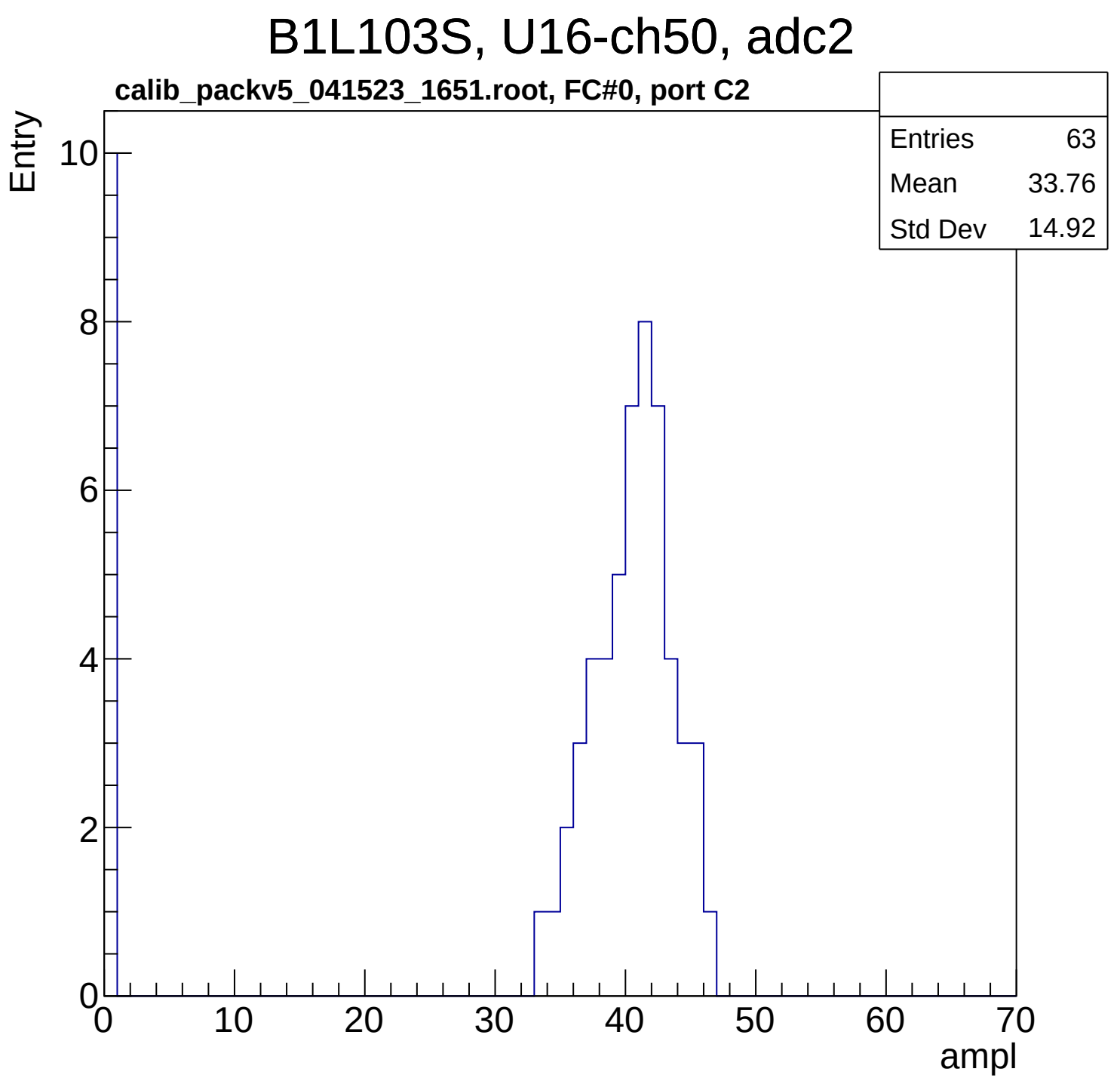
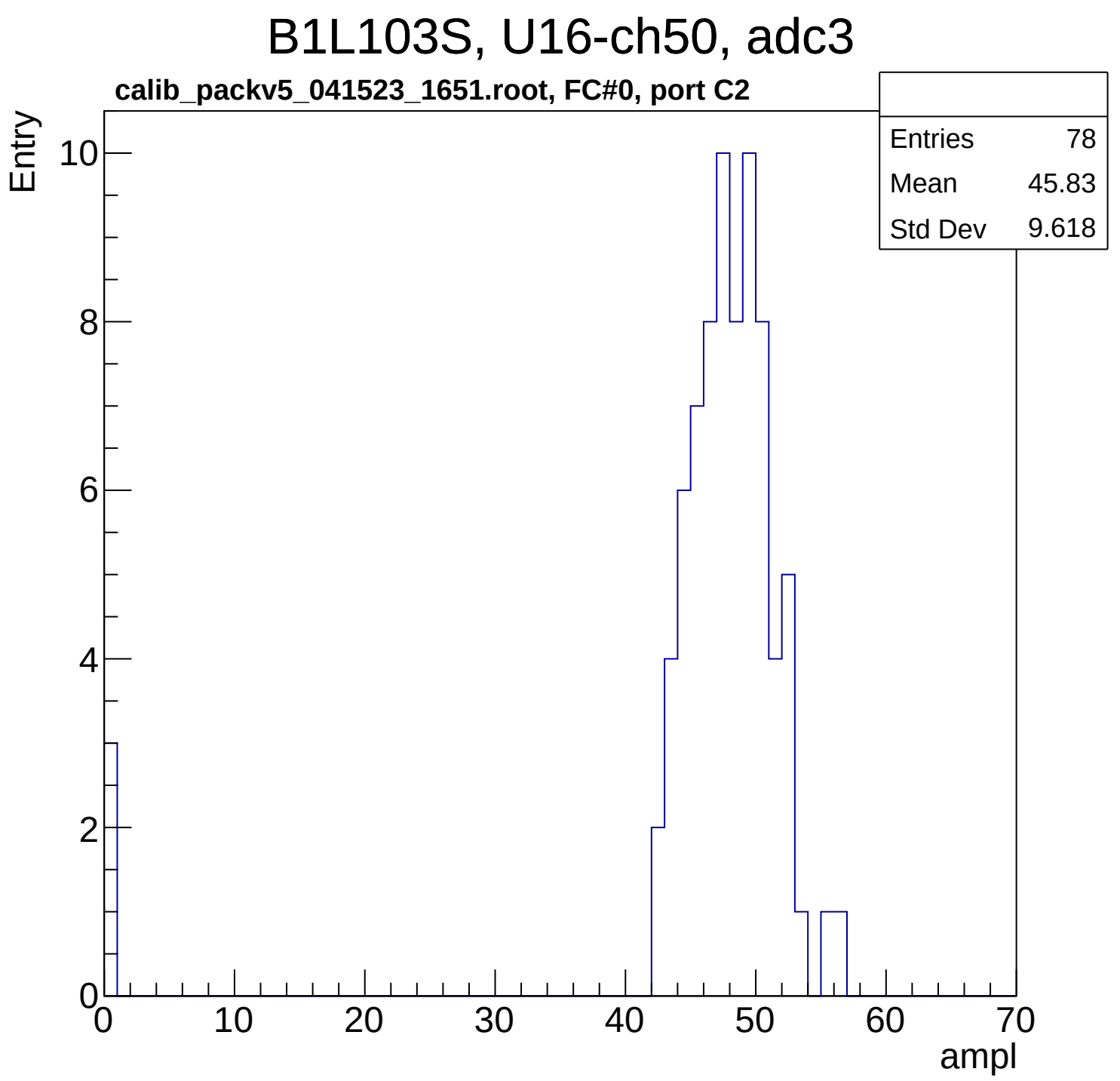
60
70


B1L103S, U16-ch50, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 33.76
Std Dev 14.92
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch50, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 45.83
Std Dev 9.618
Entry
ampl
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60
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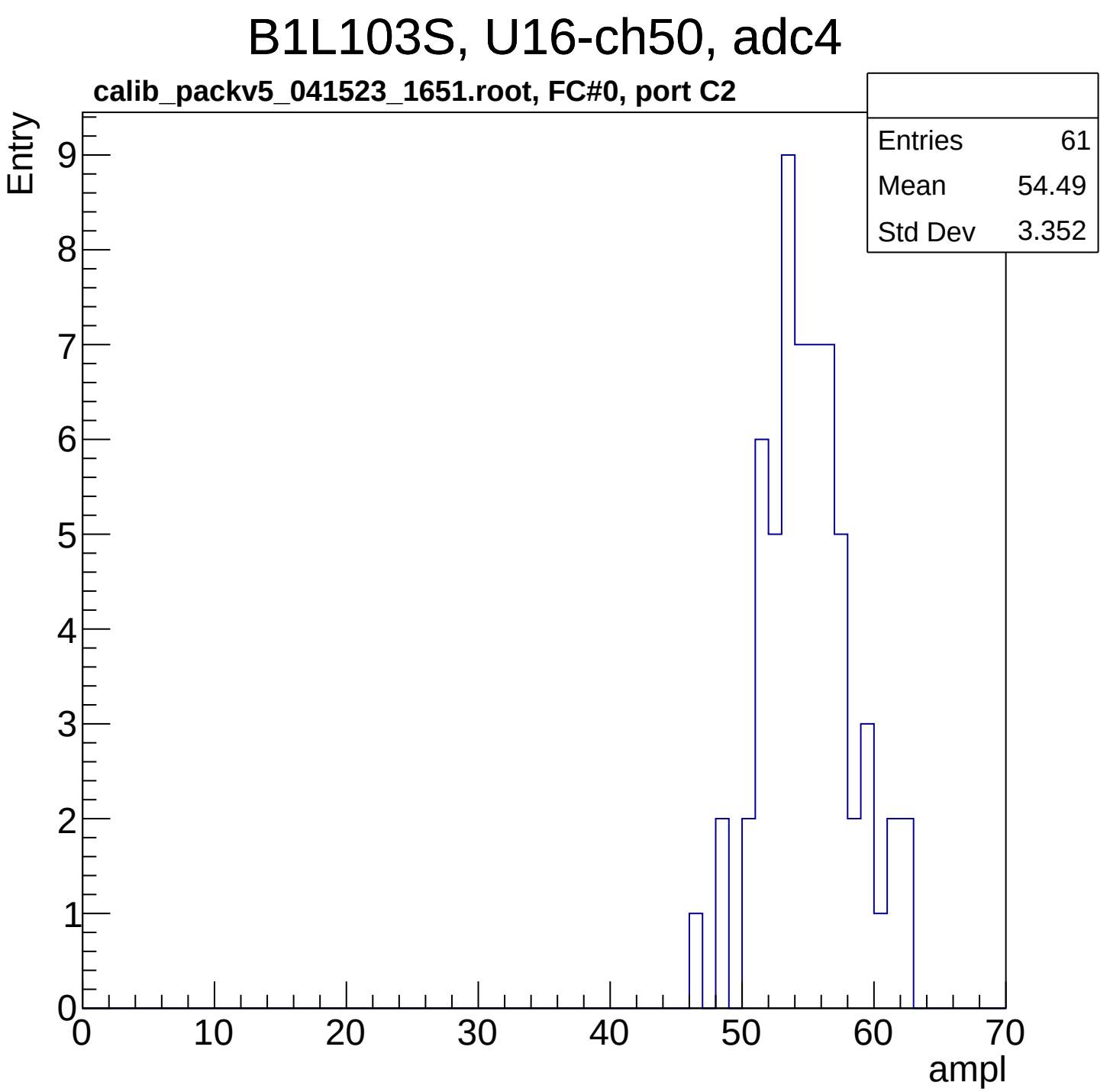
B1L103S, U16-ch50, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 54.49
Std Dev 3.352
Entry
ampl
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4
5
6
7
8
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0
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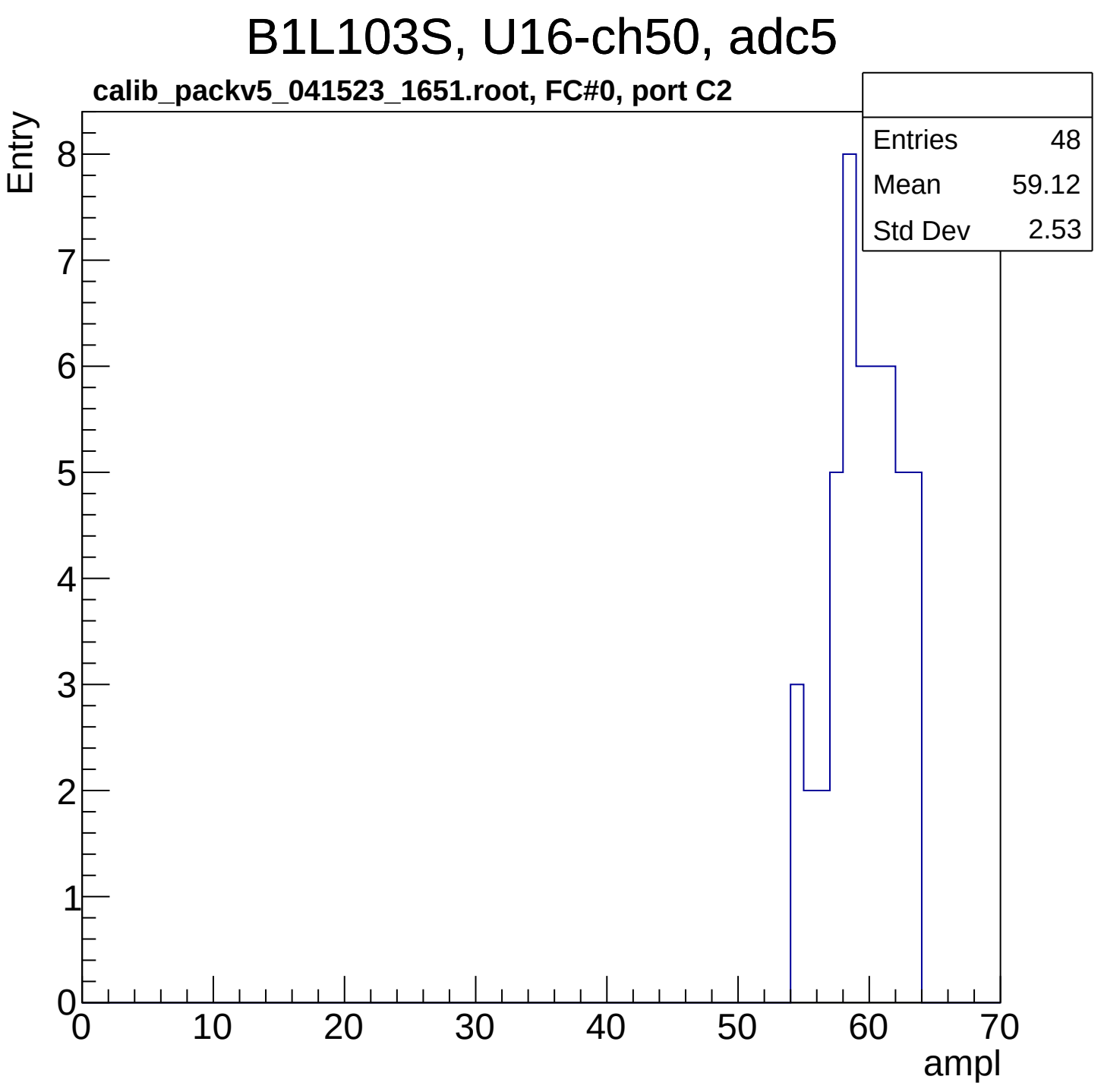
60
70


B1L103S, U16-ch50, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 59.12
Std Dev 2.53
Entry
ampl
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5
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7
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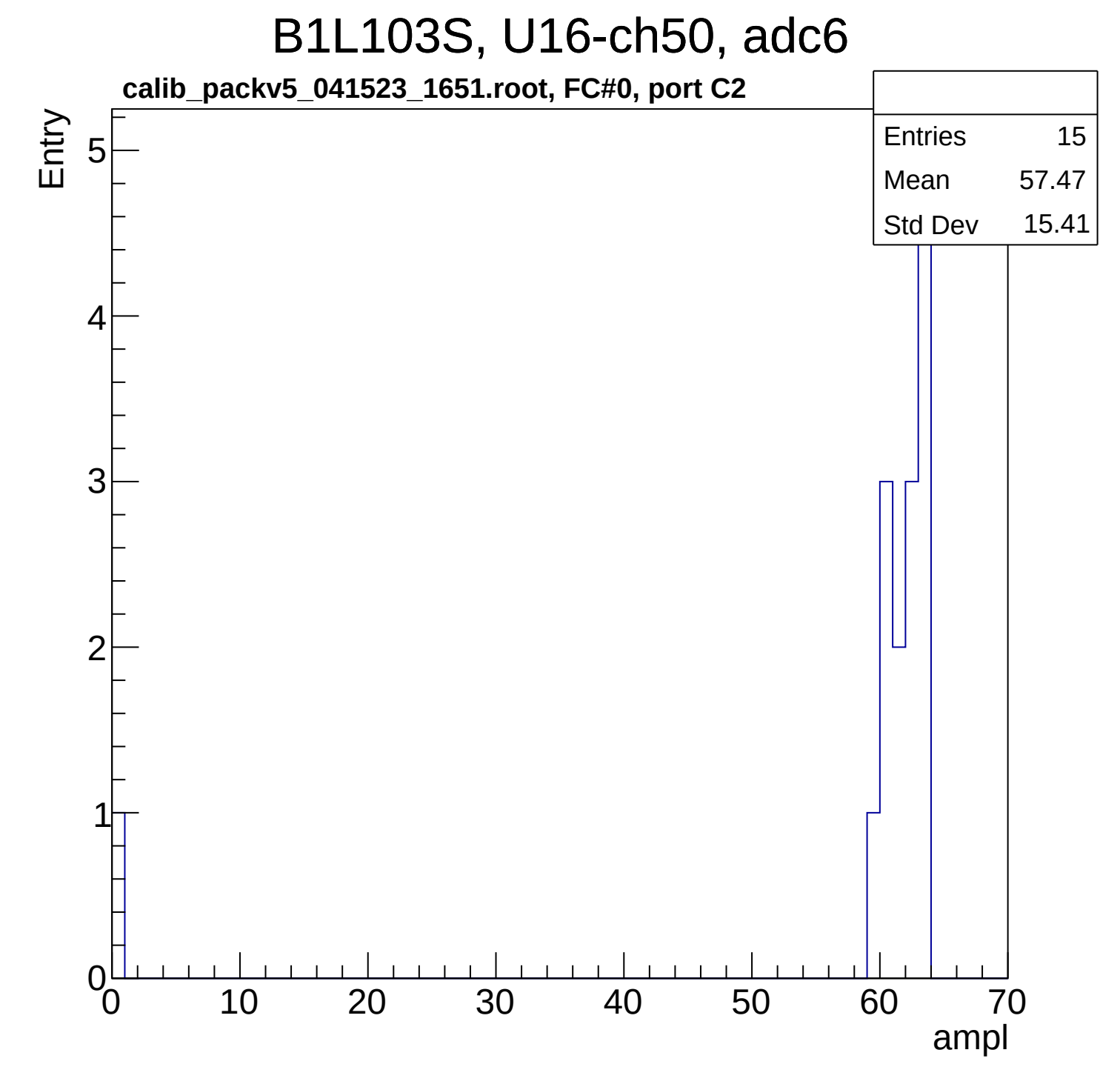
B1L103S, U16-ch50, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.47
Std Dev 15.41
Entry
ampl
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2
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4
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0
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20
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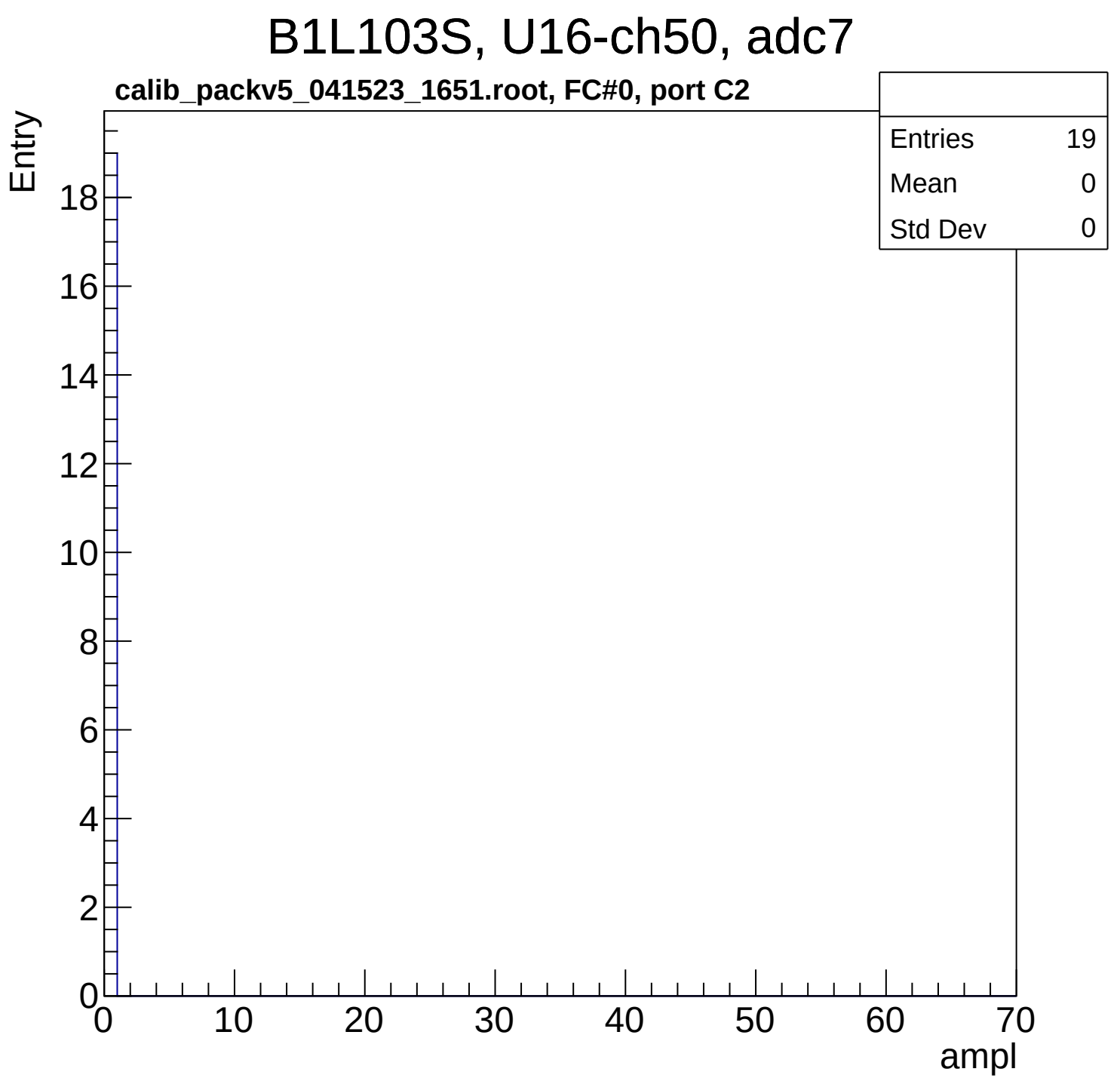
40
50
60
70


B1L103S, U16-ch50, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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10
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30
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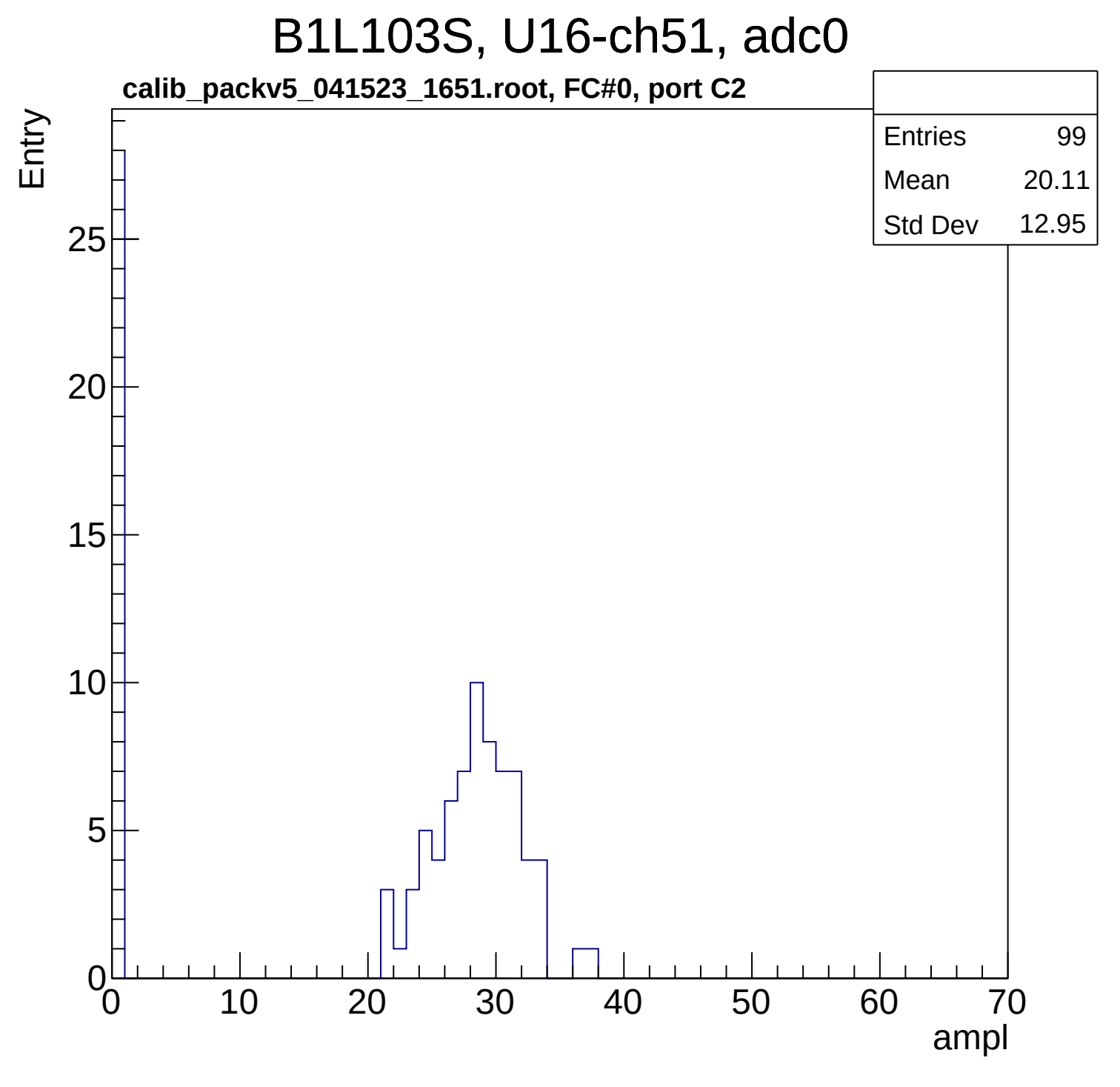
50
60
70
ampl


B1L103S, U16-ch51, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 20.11
Std Dev 12.95
Entry
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15
20
25
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10
20
30
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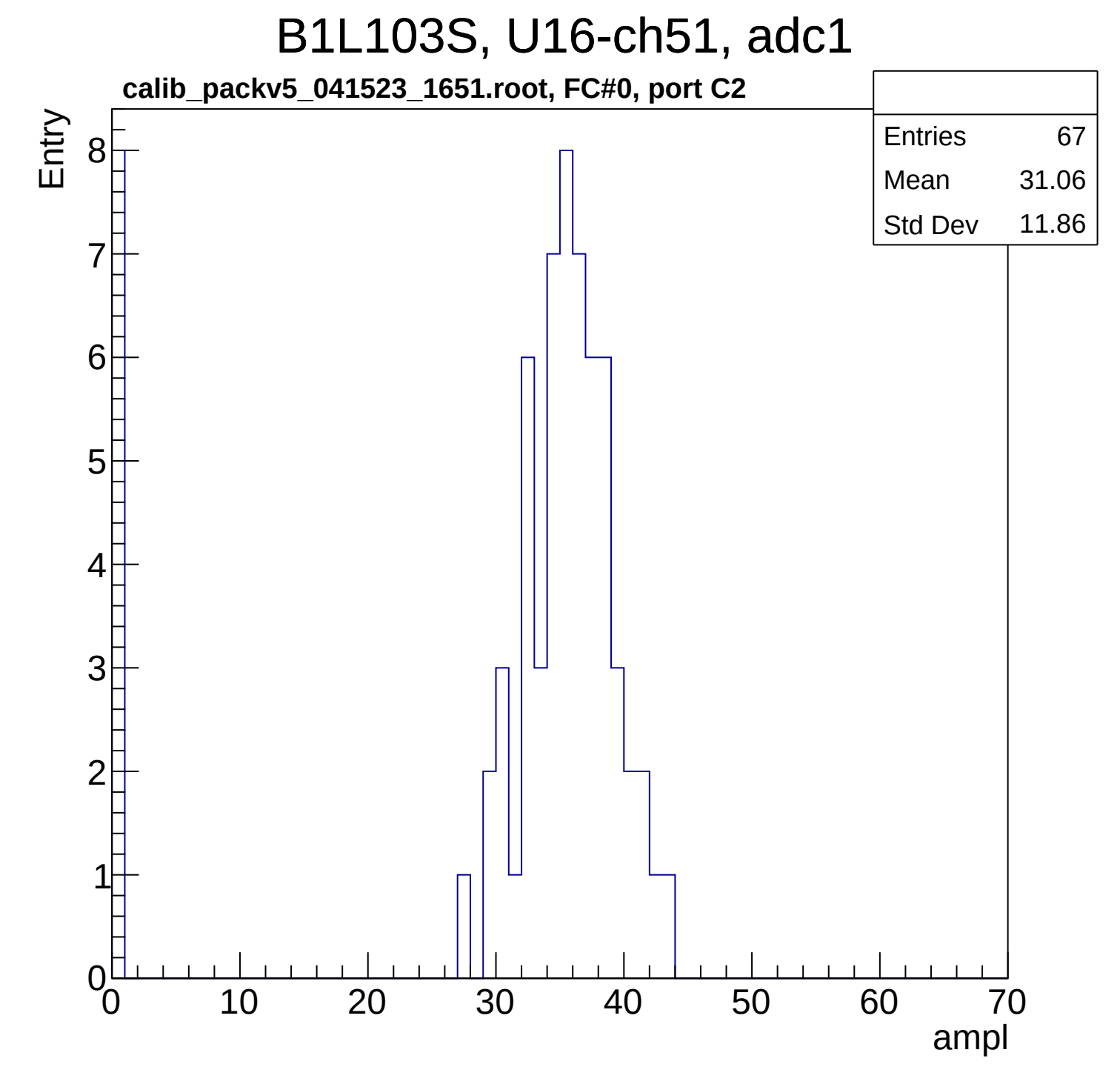
50
60
70
ampl


B1L103S, U16-ch51, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 31.06
Std Dev 11.86
Entry
ampl
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4
5
6
7
8
0
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60
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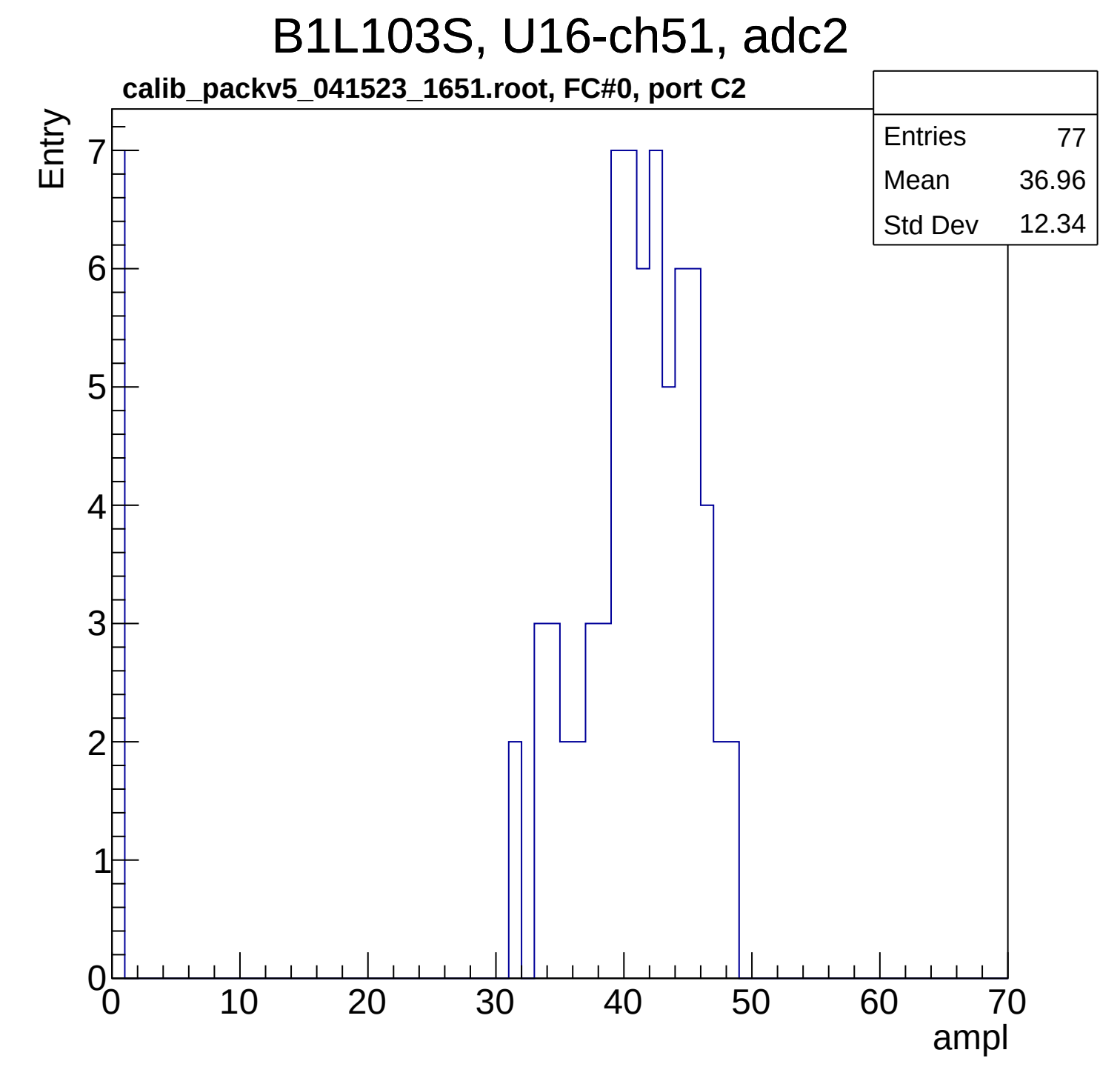
B1L103S, U16-ch51, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 36.96
Std Dev 12.34
Entry
ampl
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4
5
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0
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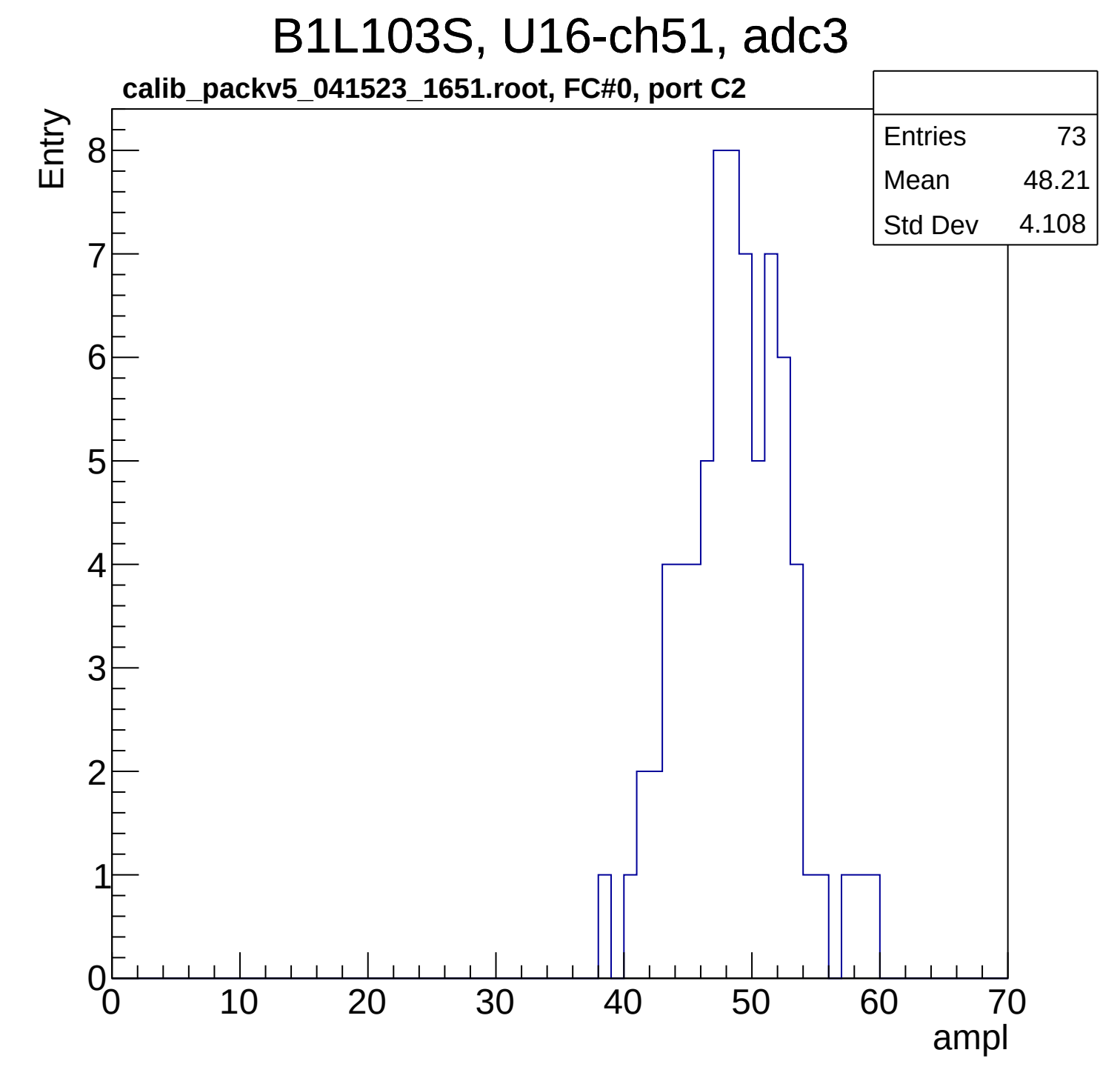
B1L103S, U16-ch51, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 48.21
Std Dev 4.108
Entry
ampl
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3
4
5
6
7
8
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60
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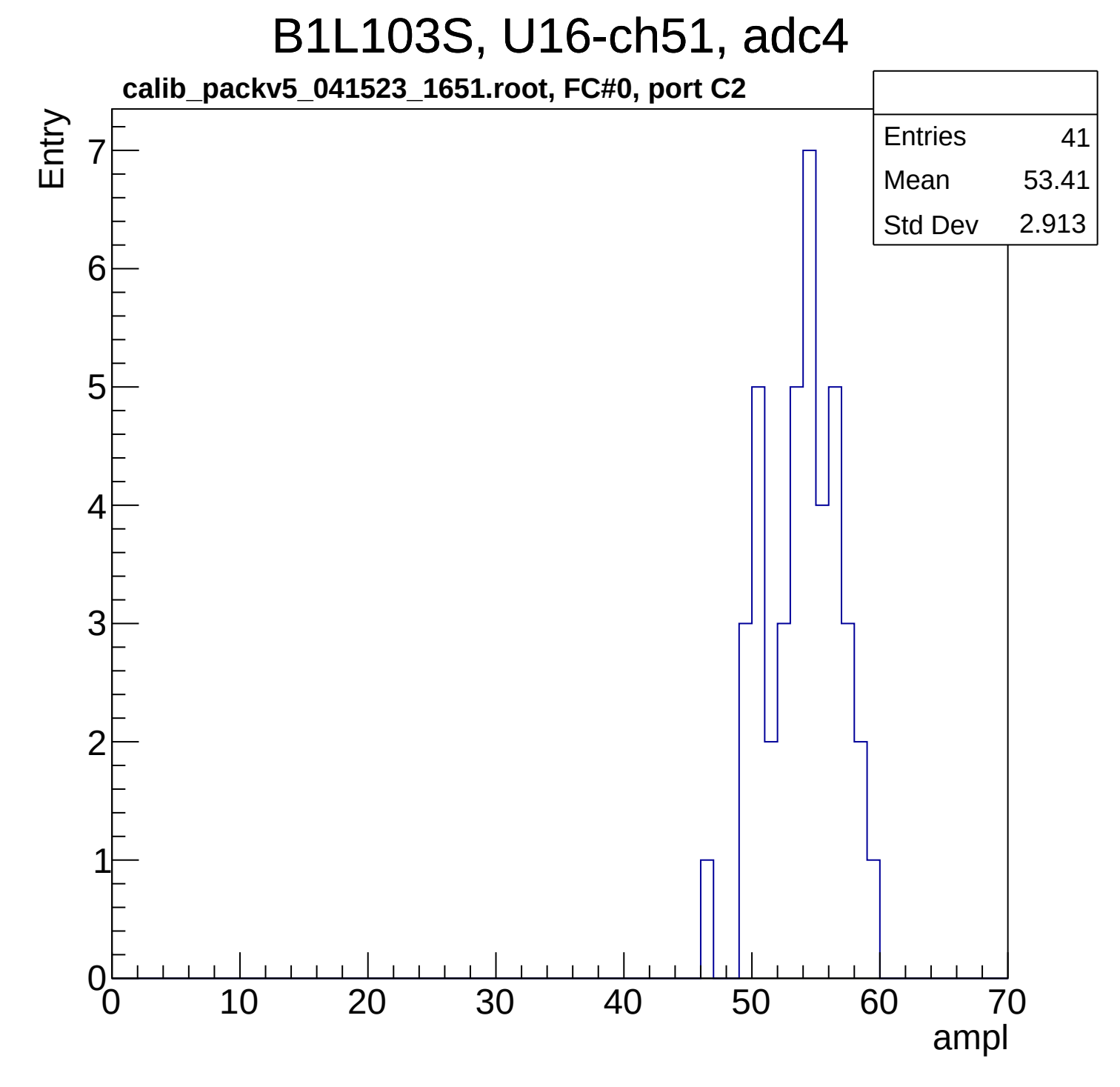
B1L103S, U16-ch51, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 53.41
Std Dev 2.913
Entry
ampl
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4
5
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7
0
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20
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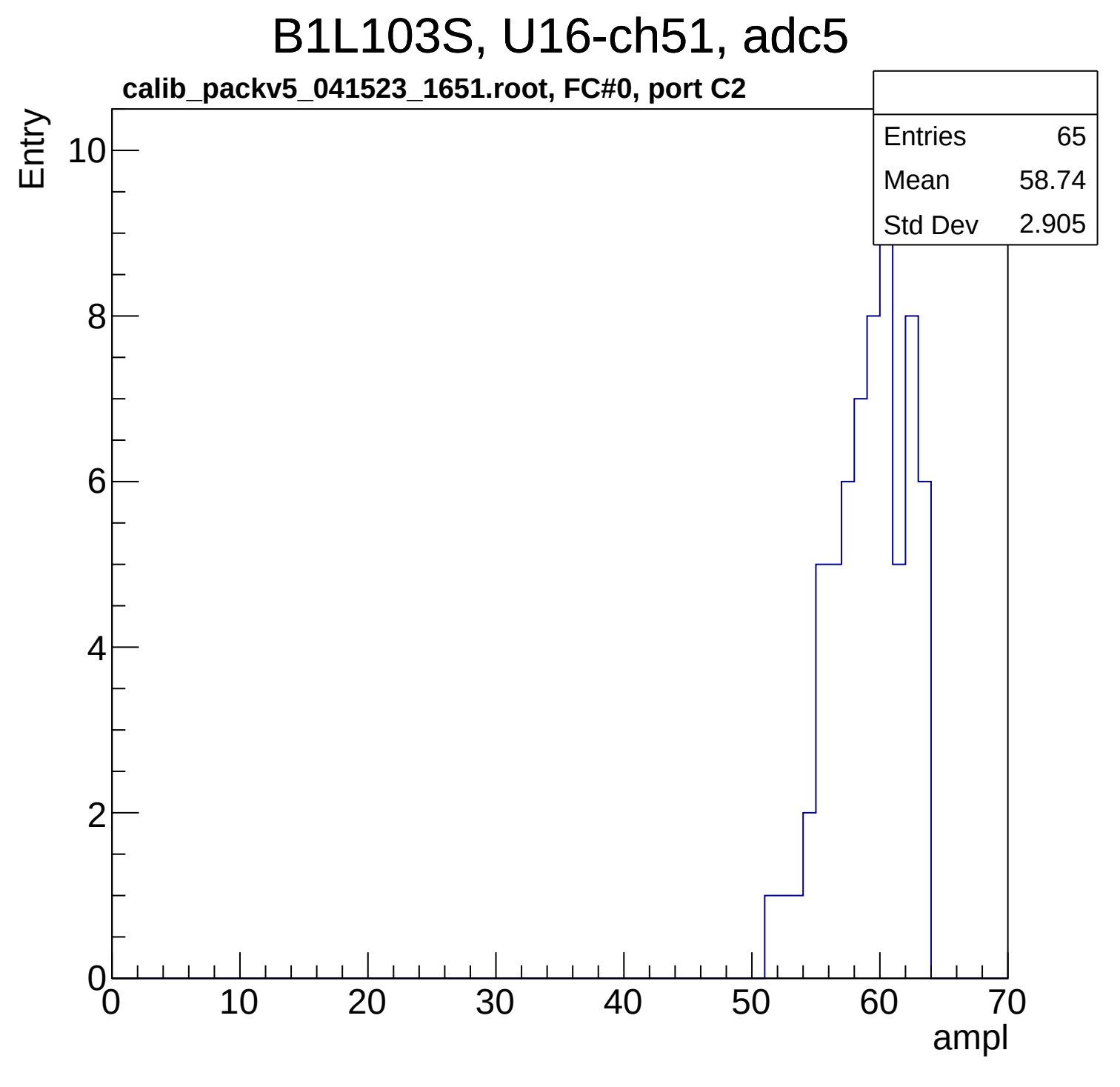
B1L103S, U16-ch51, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 58.74
Std Dev 2.905
Entry
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8
10
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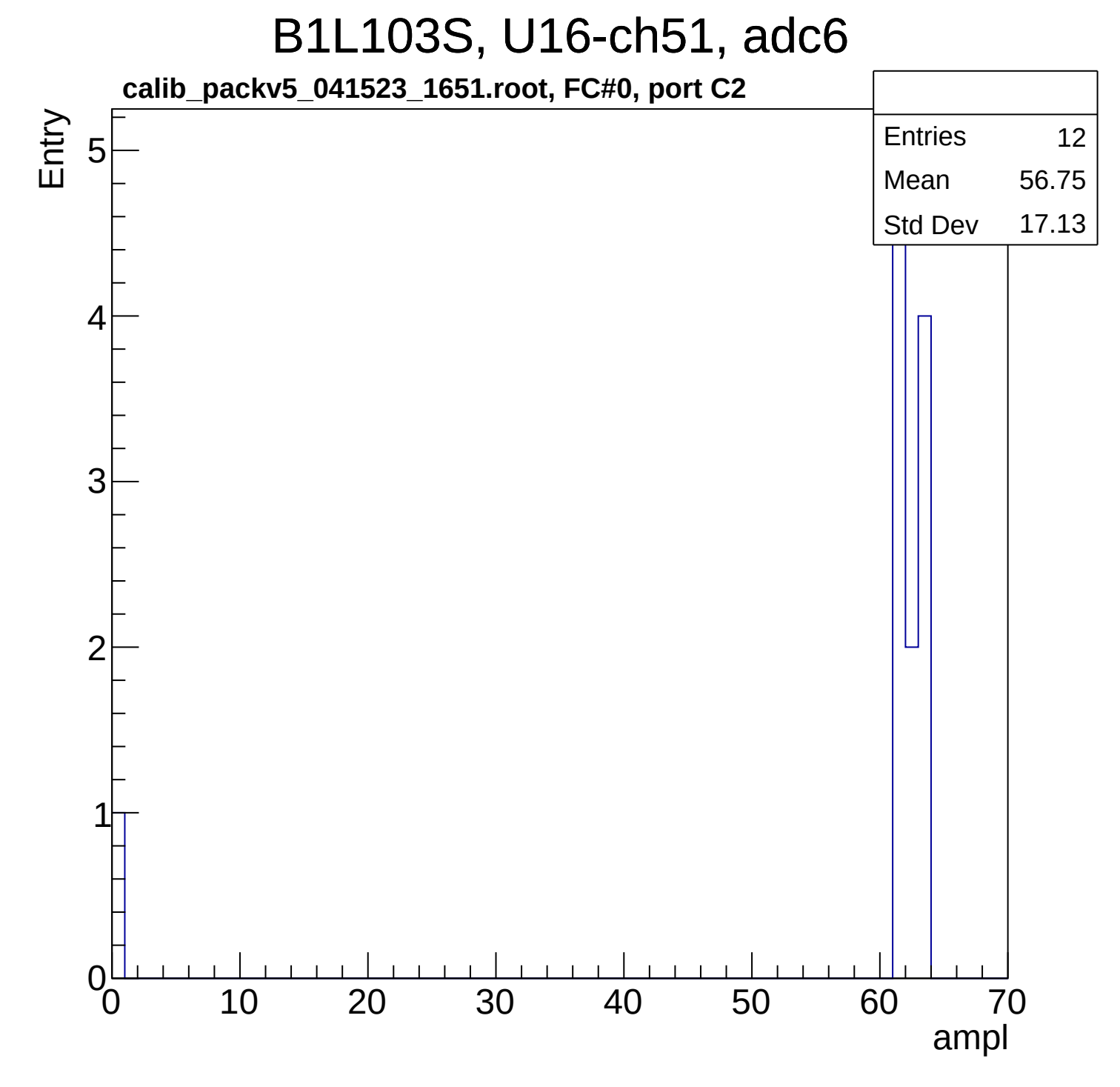
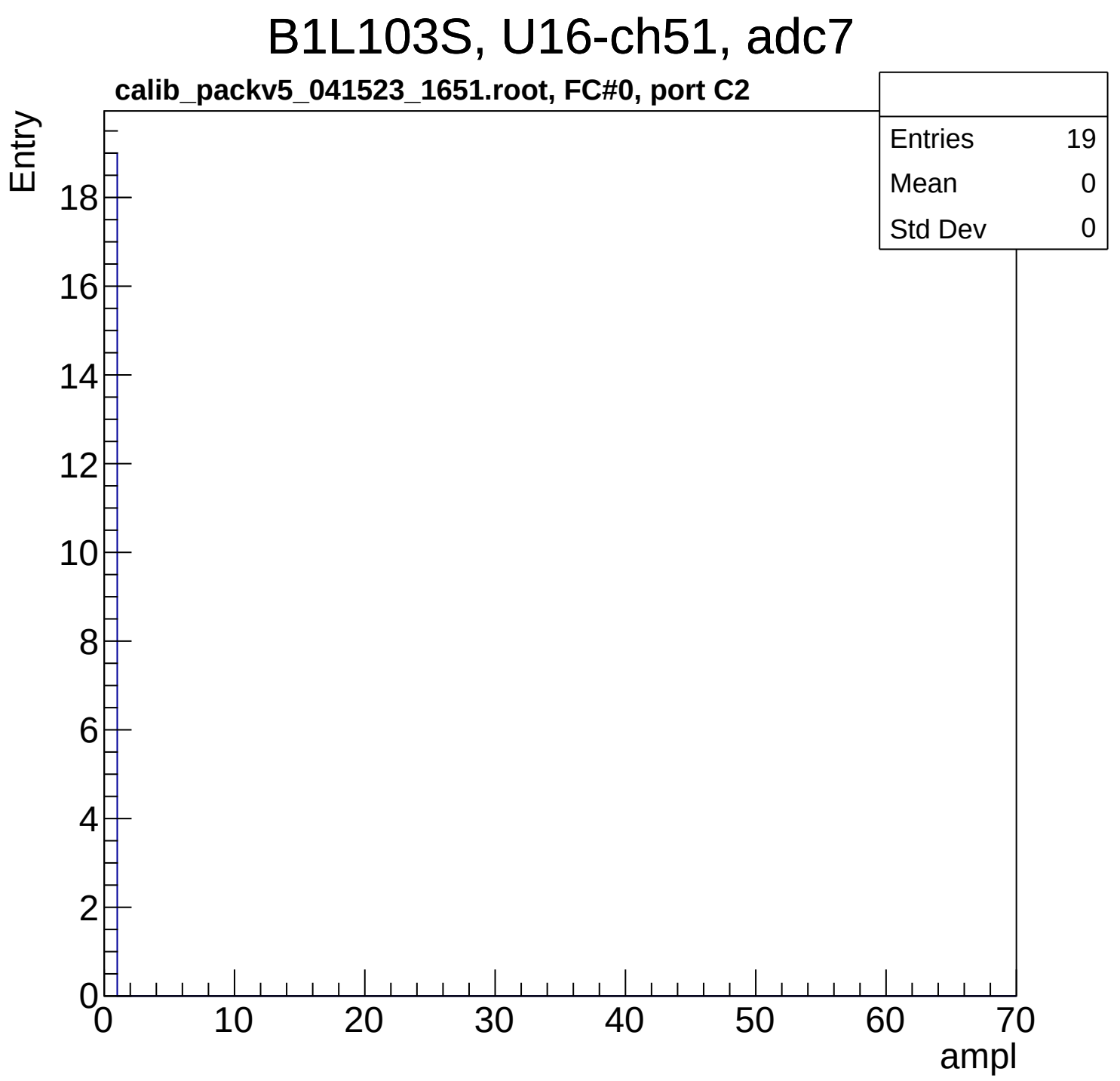
20
30
40
50
60
70
ampl


B1L103S, U16-ch51, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.75
Std Dev 17.13
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch51, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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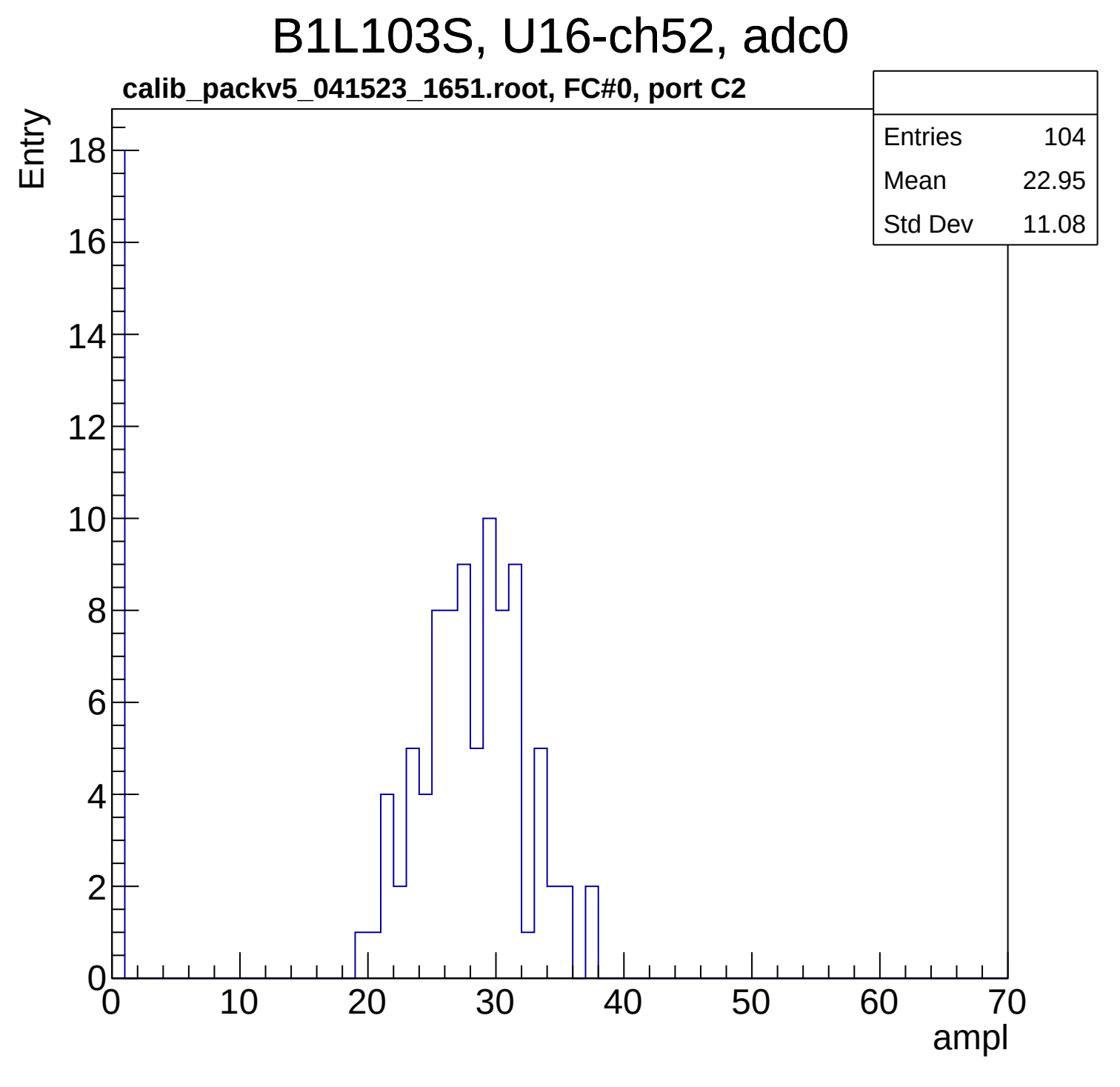
50
60
70
ampl


B1L103S, U16-ch52, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 22.95
Std Dev 11.08
Entry
ampl
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2
4
6
8
10
12
14
16
18
0
10
20
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40
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60
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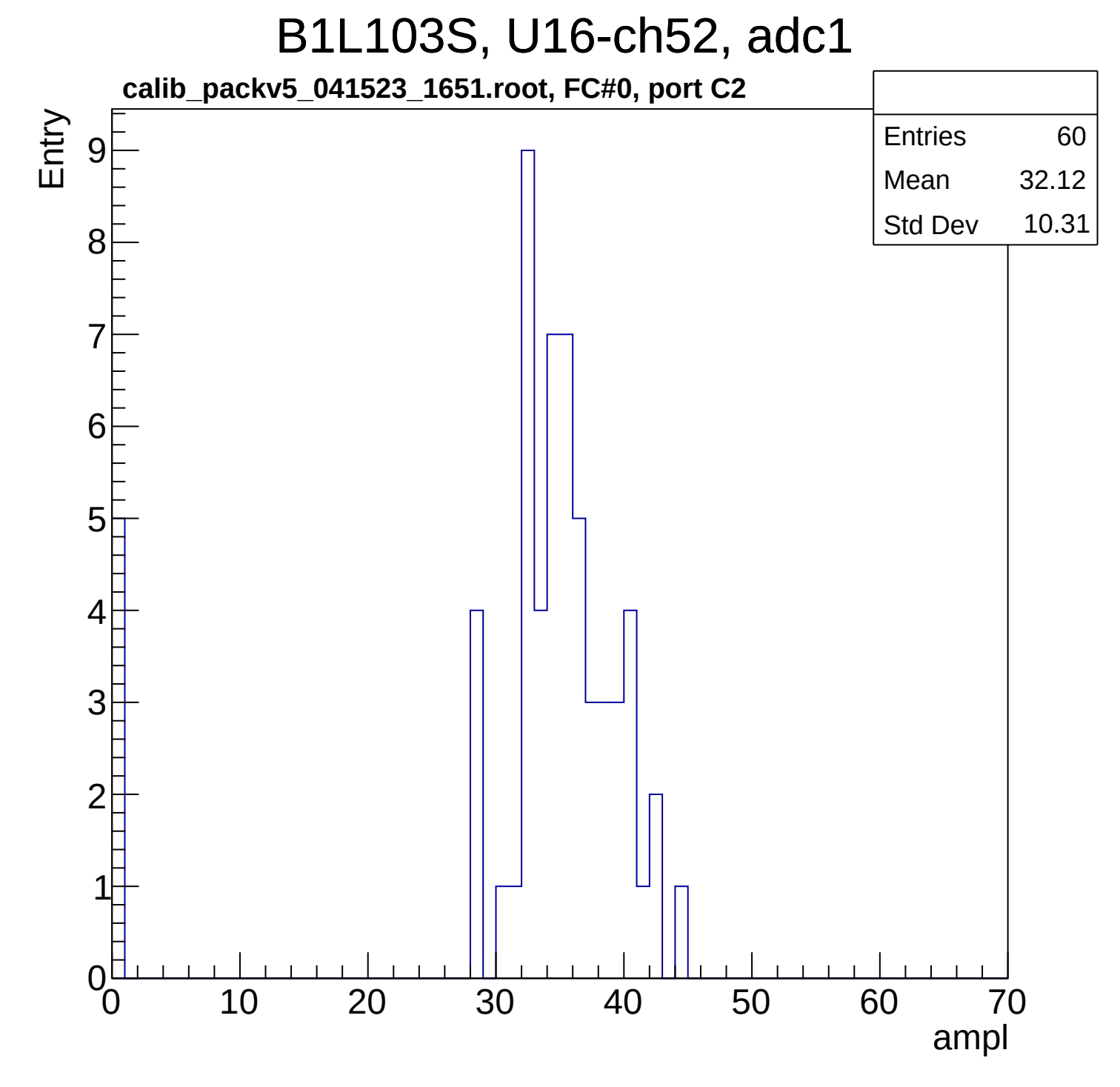
B1L103S, U16-ch52, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 32.12
Std Dev 10.31
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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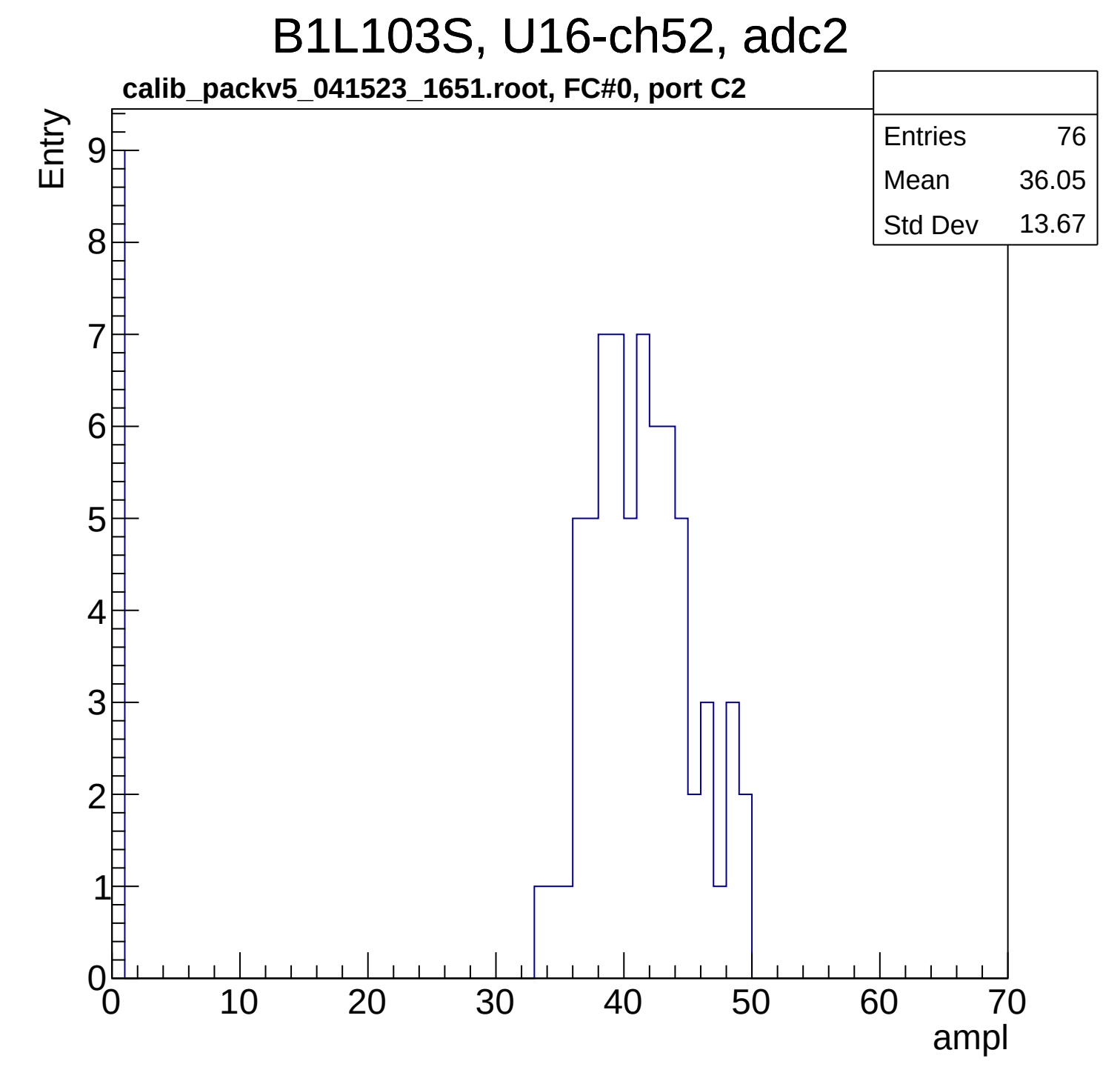
B1L103S, U16-ch52, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 36.05
Std Dev 13.67
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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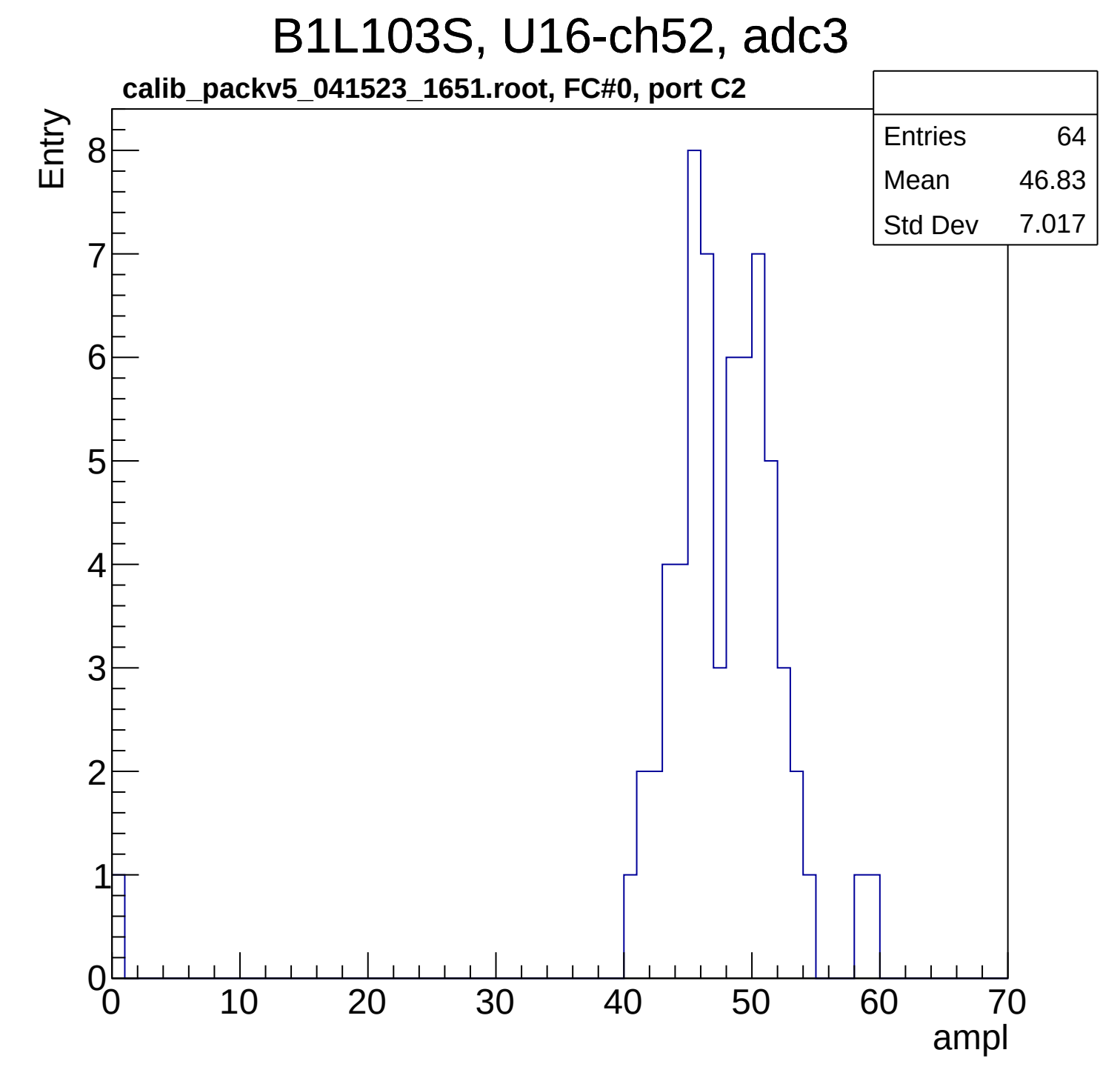
B1L103S, U16-ch52, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 46.83
Std Dev 7.017
Entry
ampl
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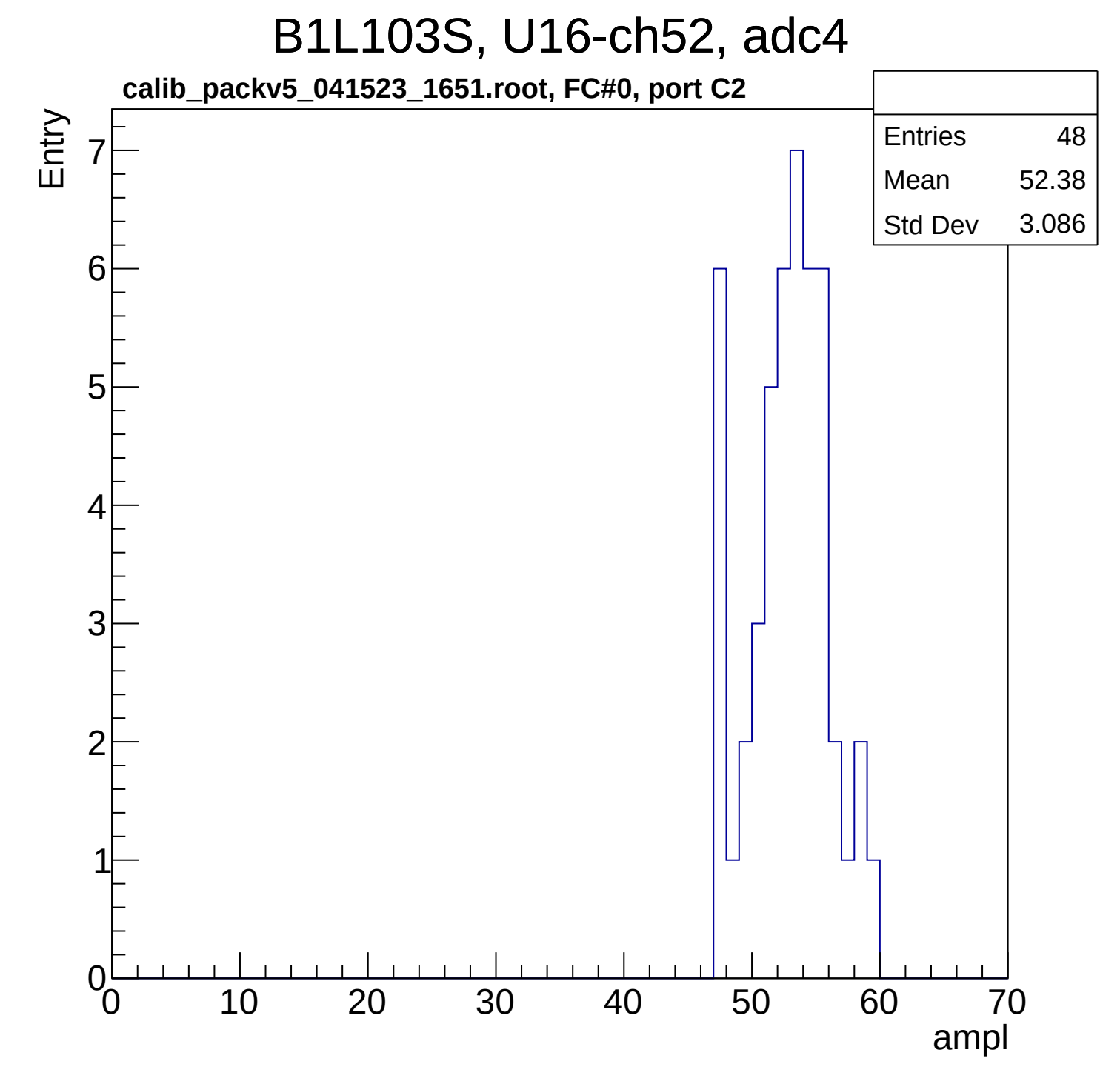
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch52, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 52.38
Std Dev 3.086
Entry
ampl
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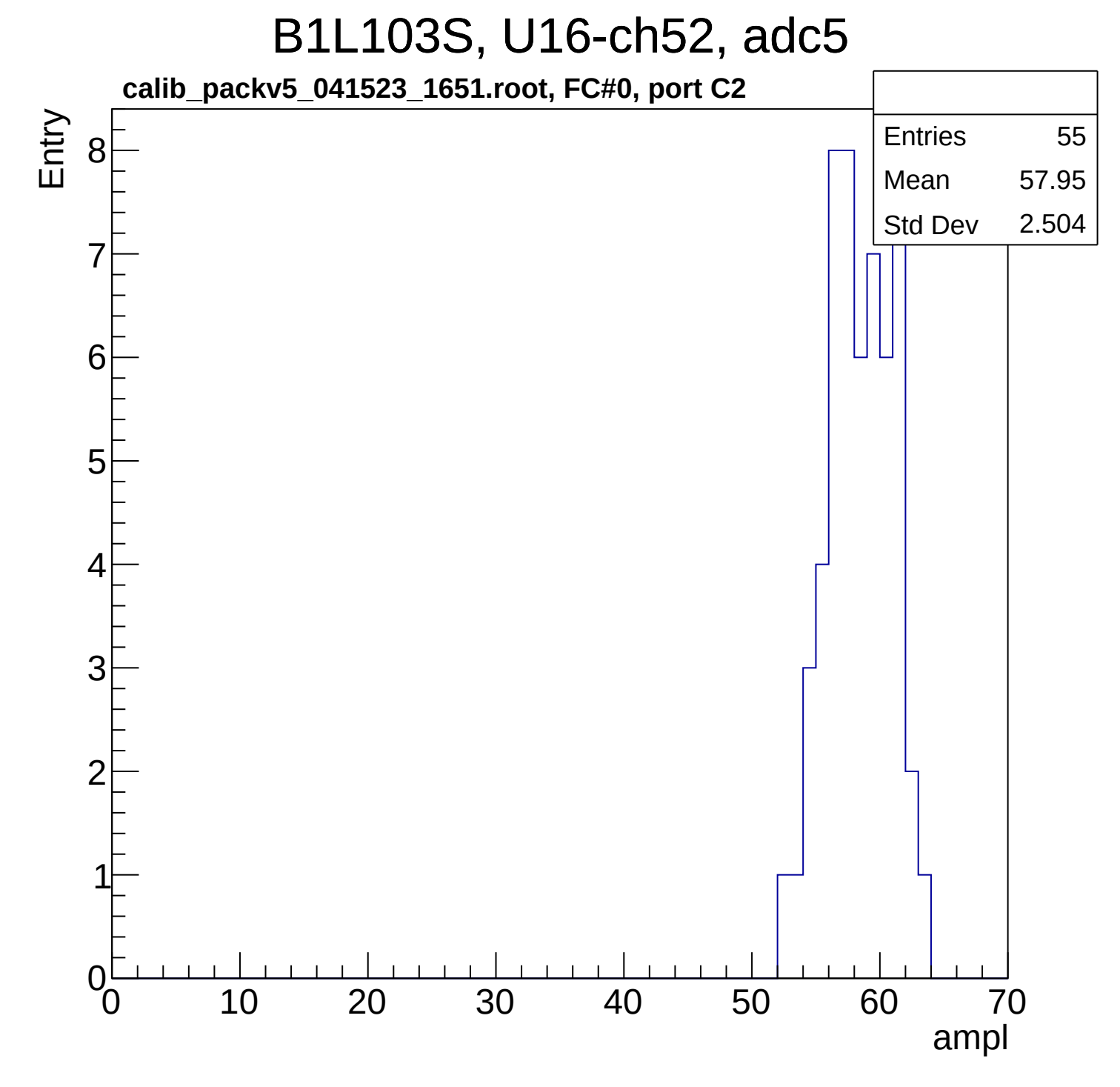
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch52, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.95
Std Dev 2.504
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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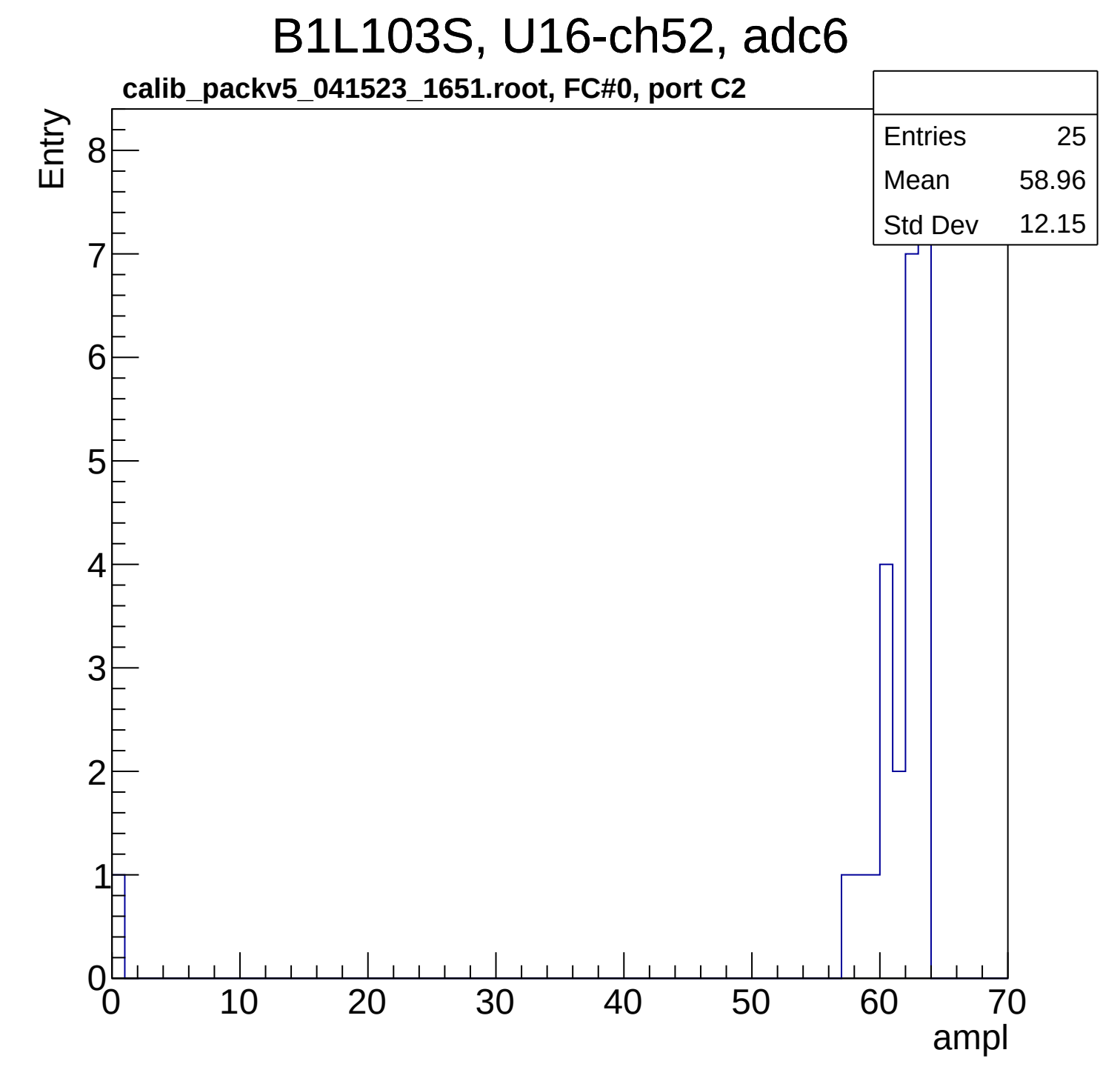
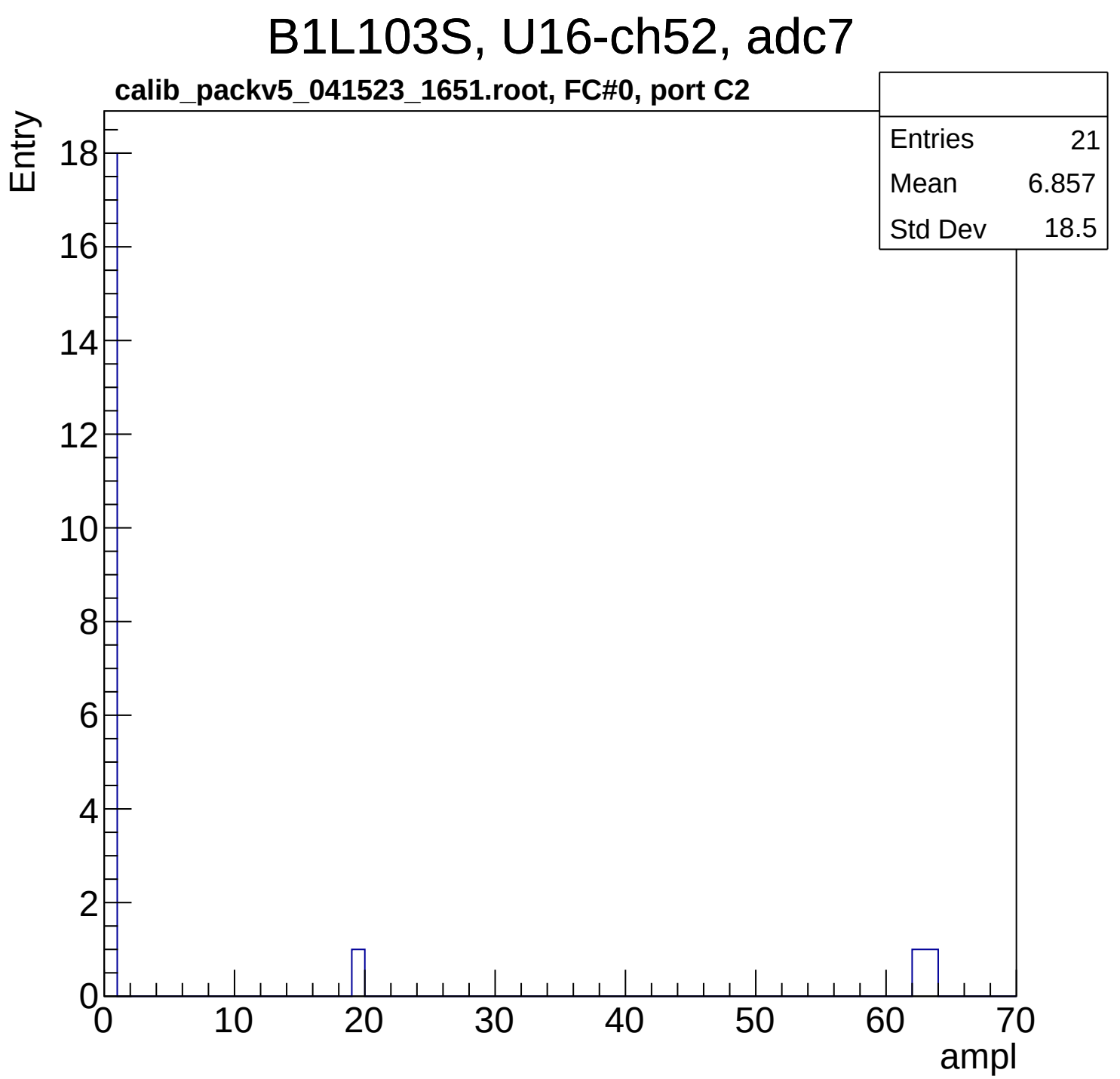
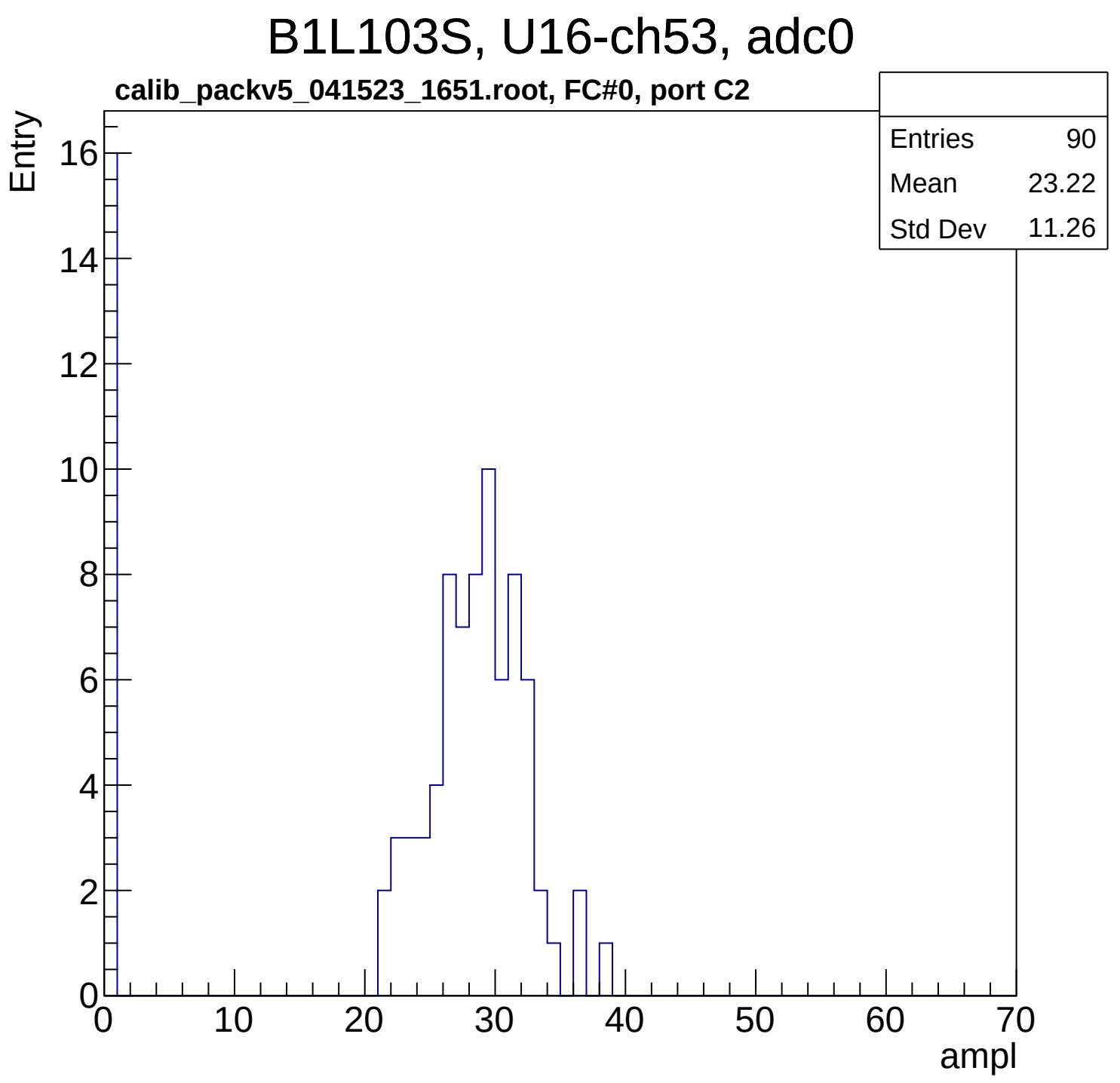
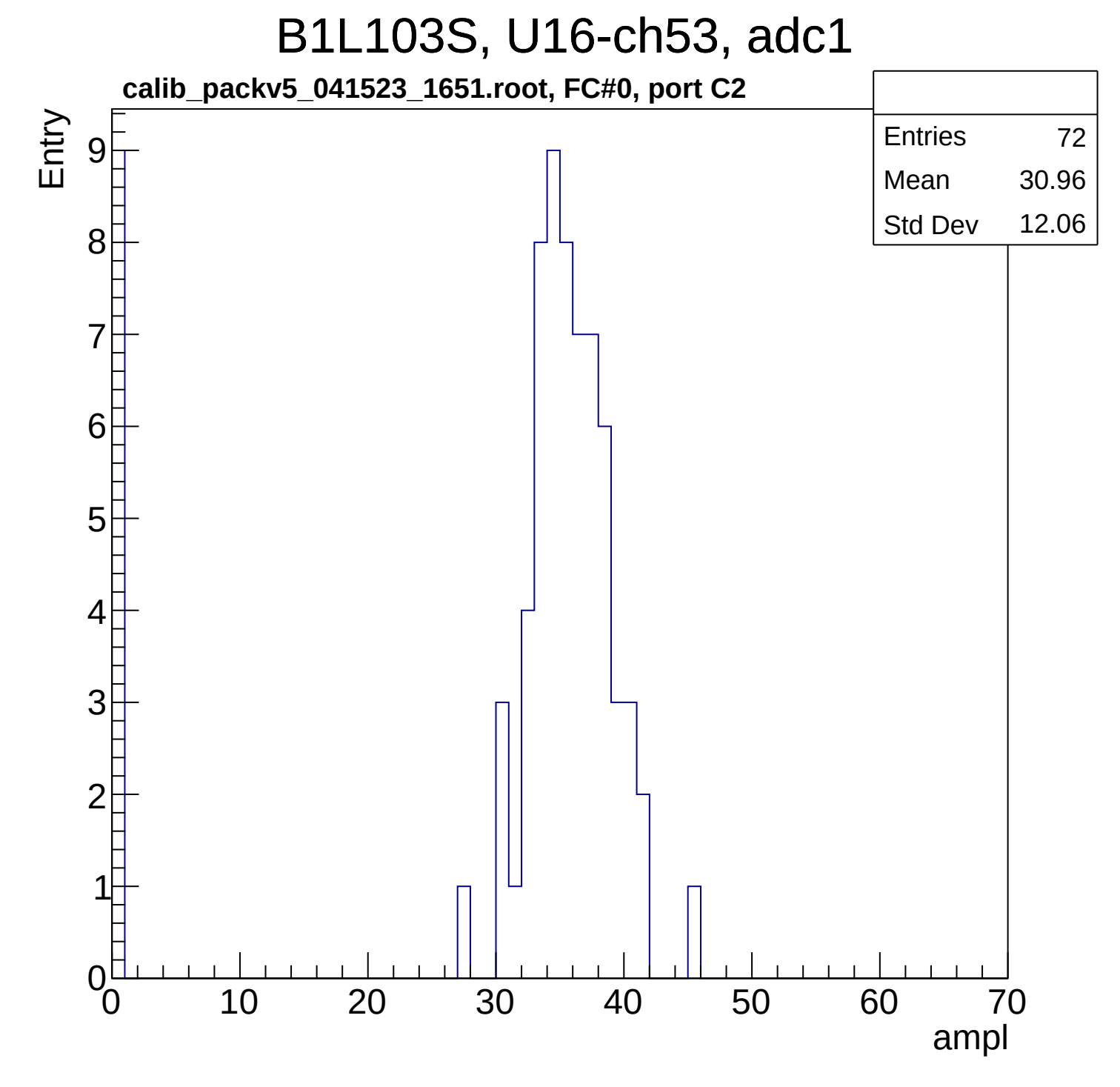
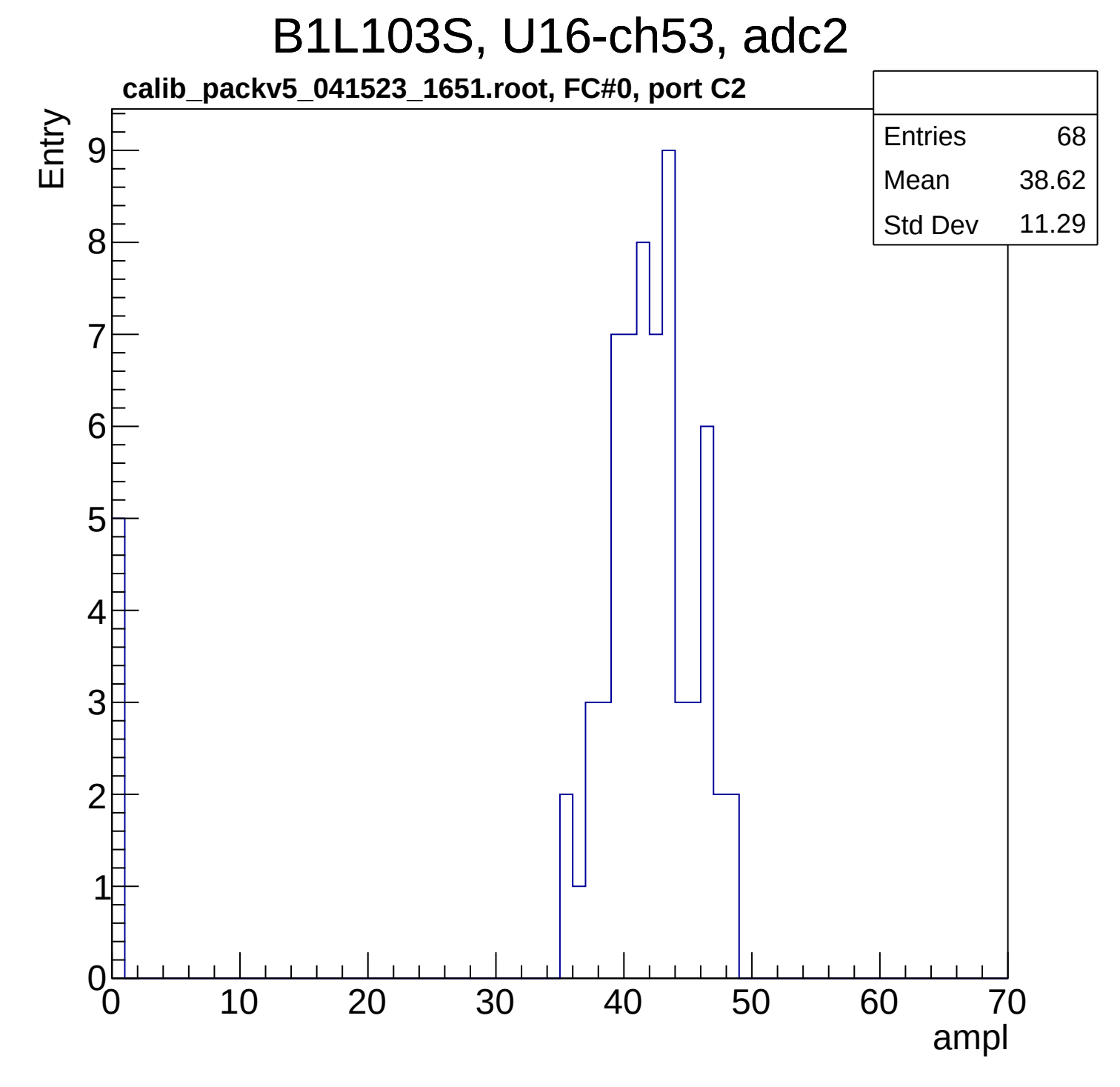

B1L103S, U16-ch52, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 58.96
Std Dev 12.15
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch52, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6.857
Std Dev 18.5
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch53, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 23.22
Std Dev 11.26
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U16-ch53, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 30.96
Std Dev 12.06
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch53, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 38.62
Std Dev 11.29
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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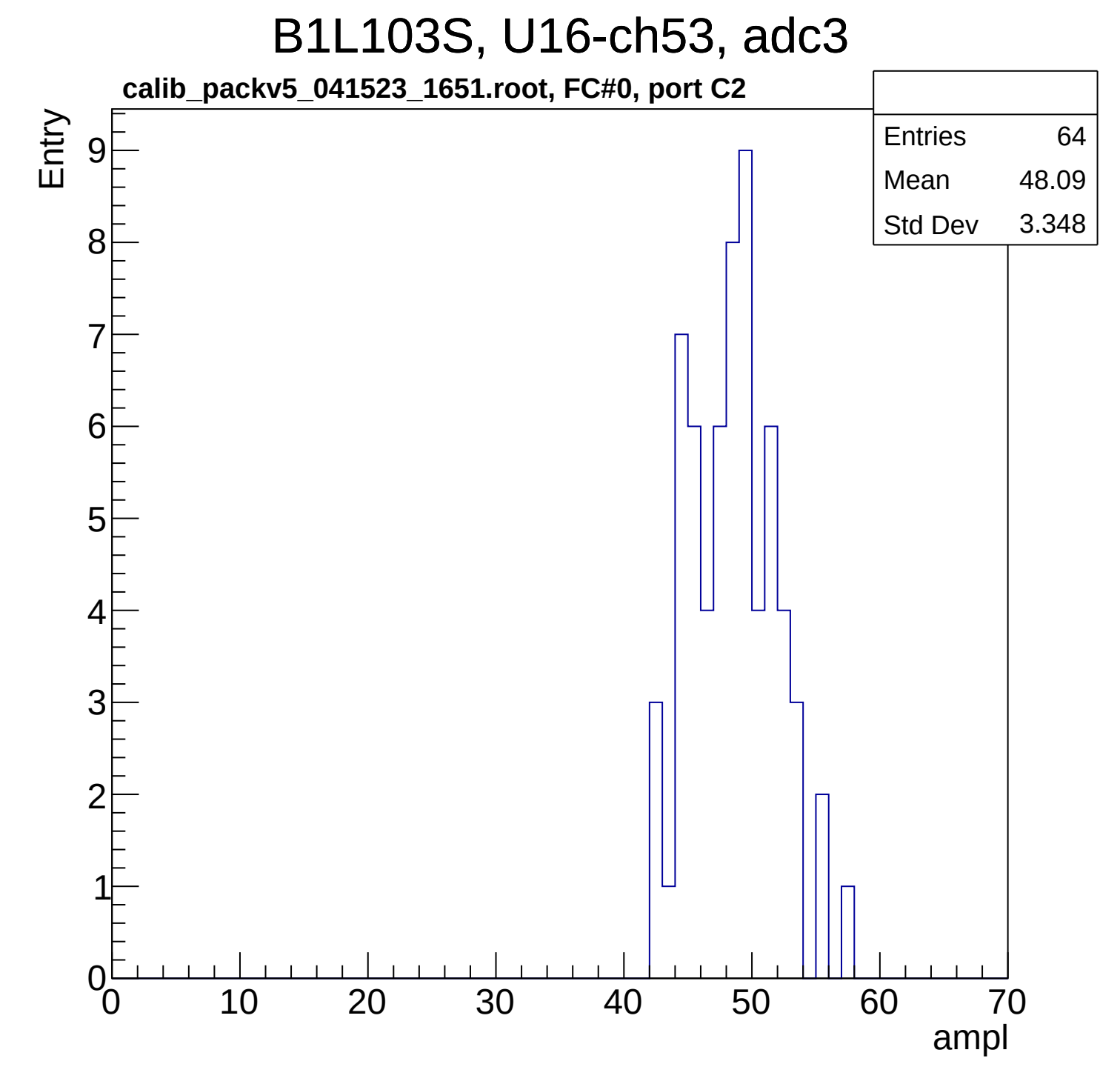
B1L103S, U16-ch53, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 48.09
Std Dev 3.348
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
50
60
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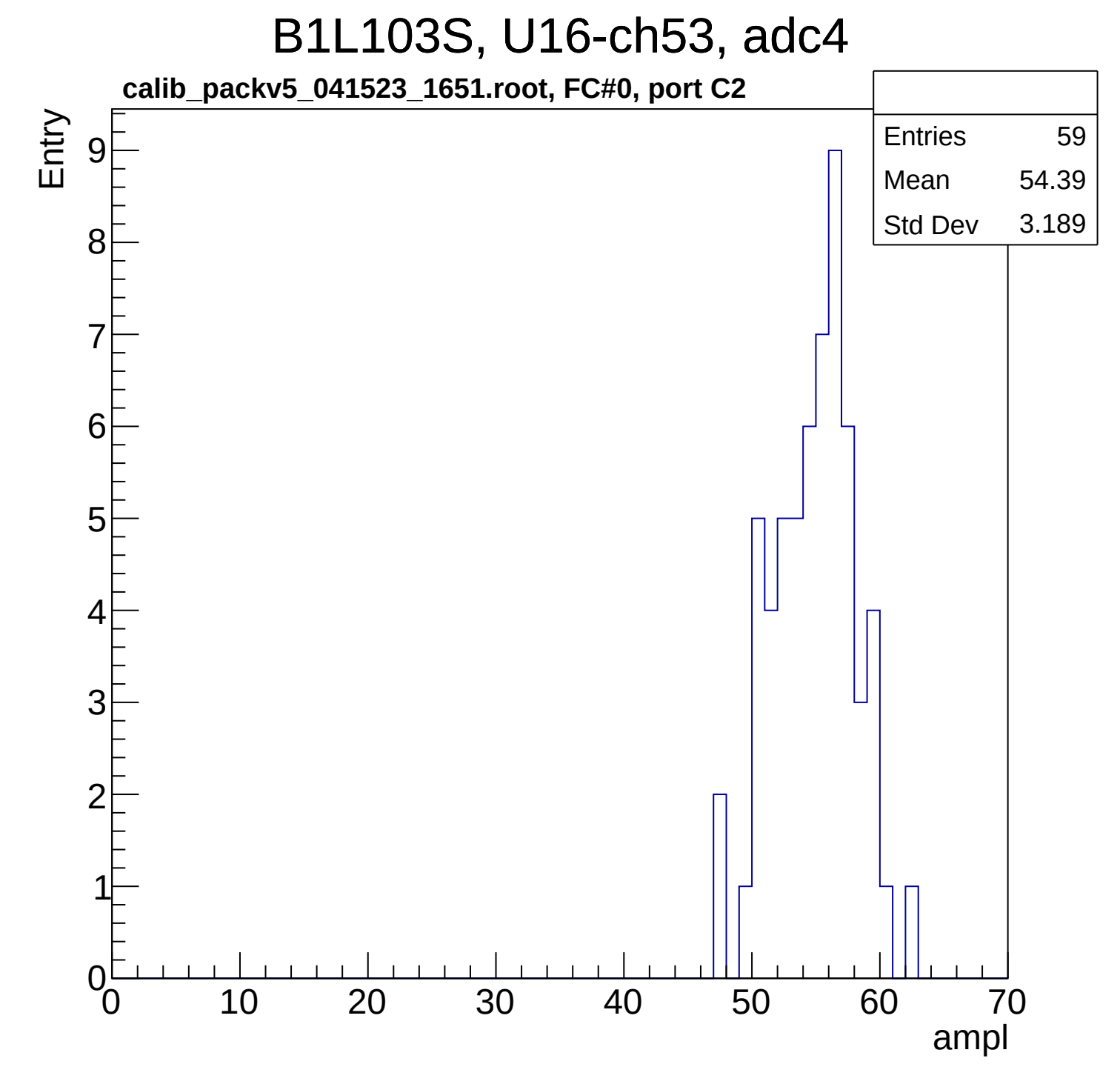
B1L103S, U16-ch53, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.39
Std Dev 3.189
Entry
ampl
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2
3
4
5
6
7
8
9
0
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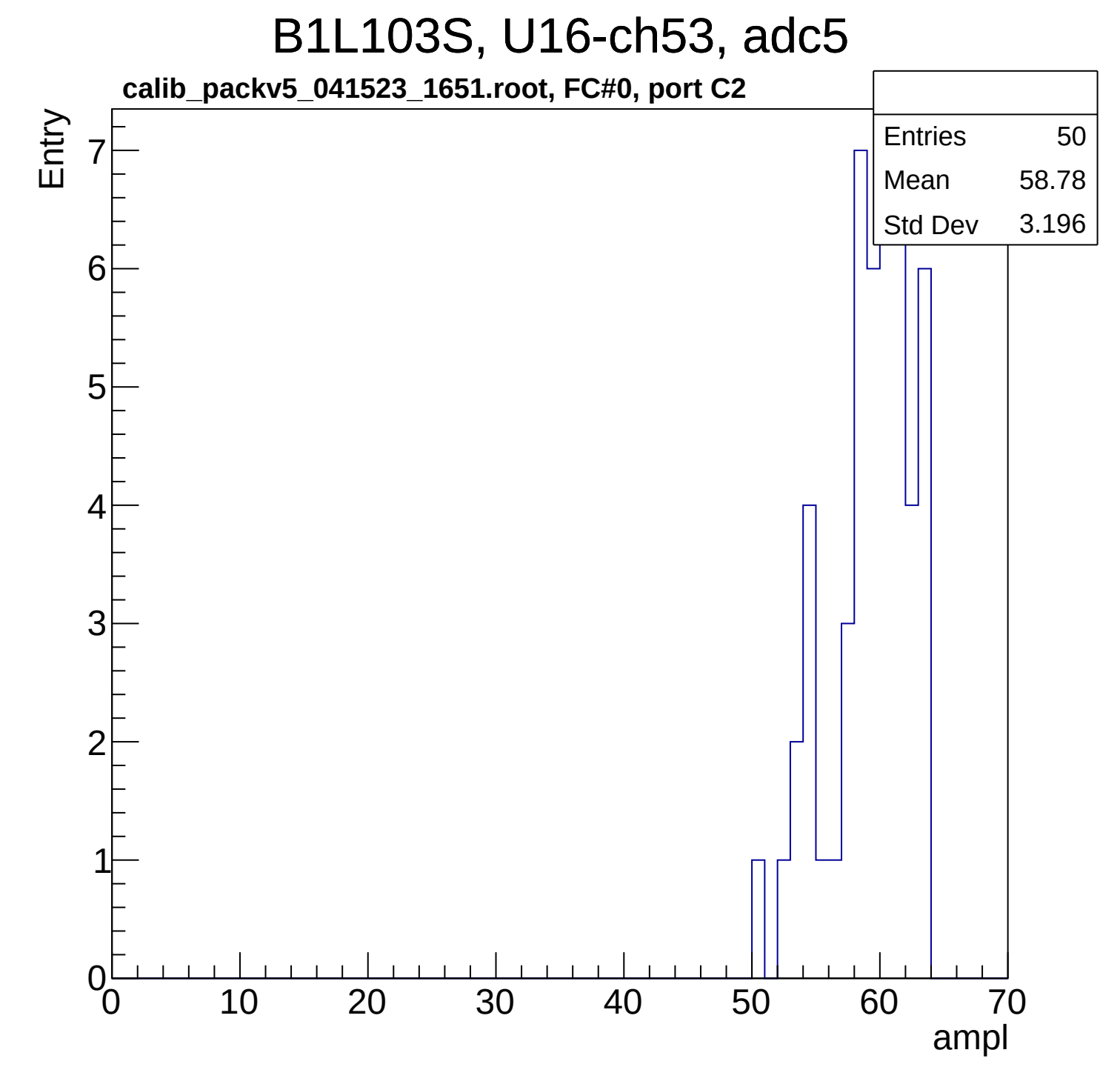
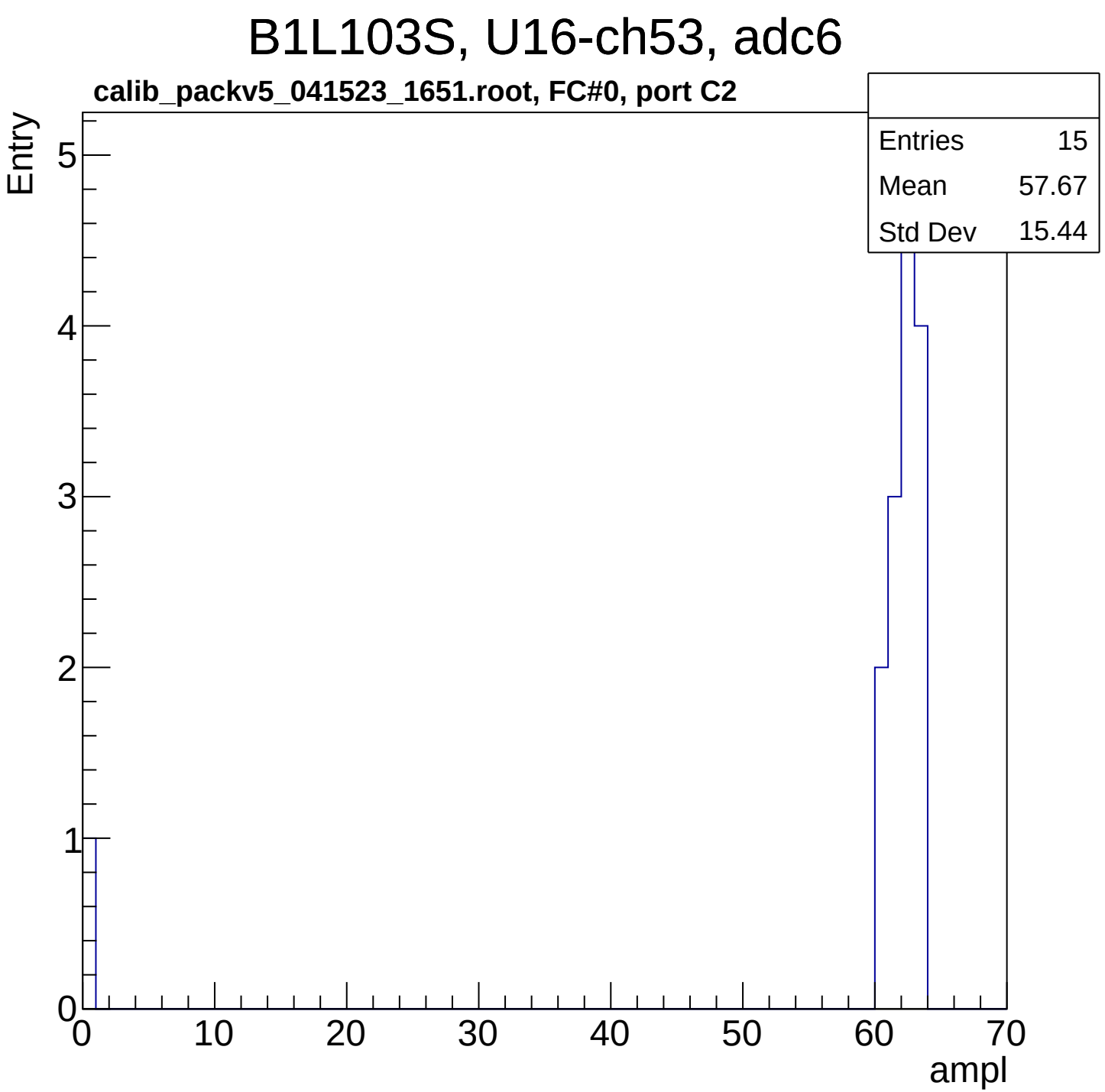
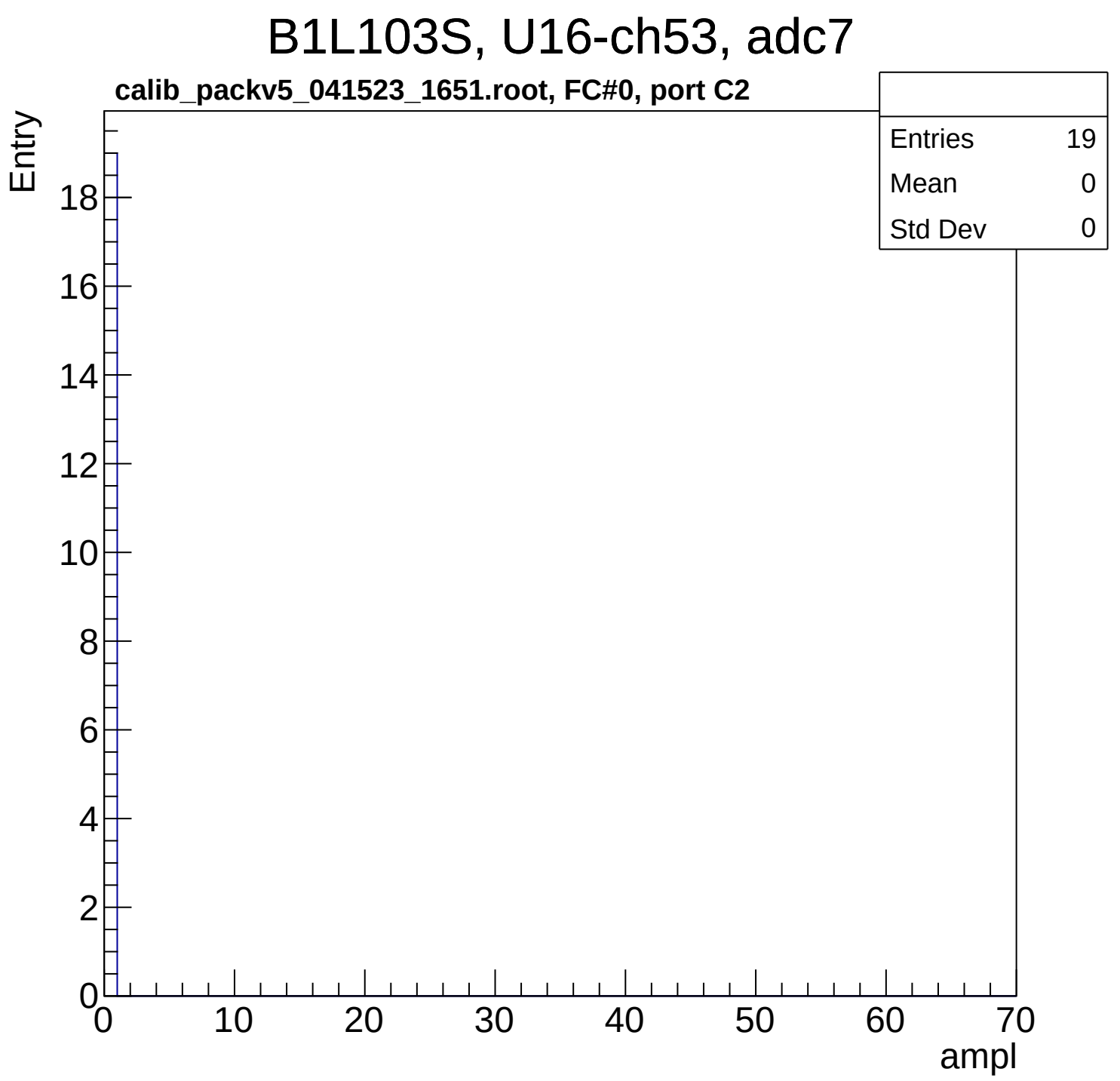
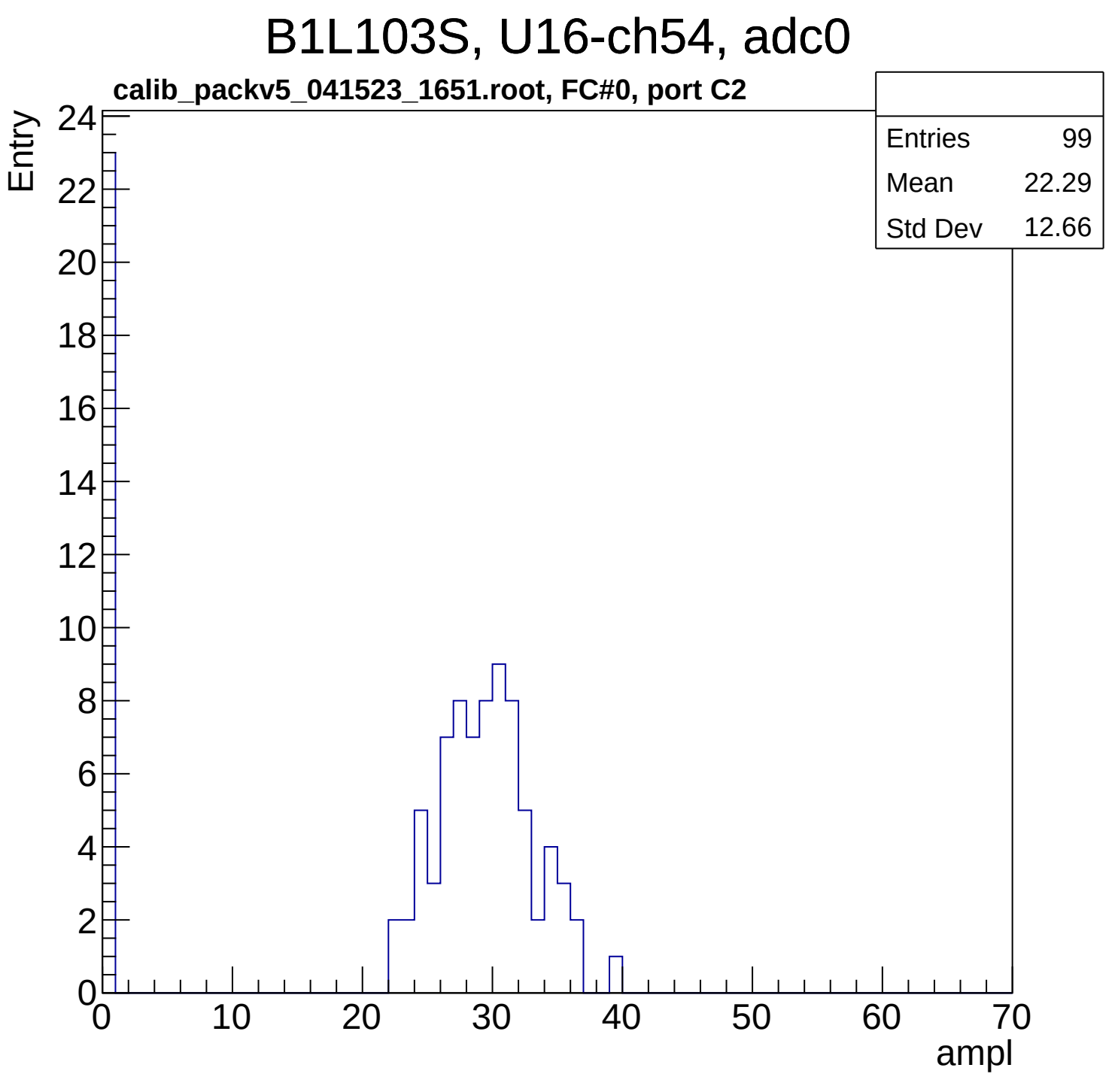
20
30
40
50
60
70


B1L103S, U16-ch53, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.78
Std Dev 3.196
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch53, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.67
Std Dev 15.44
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch53, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch54, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 22.29
Std Dev 12.66
Entry
ampl
0
2
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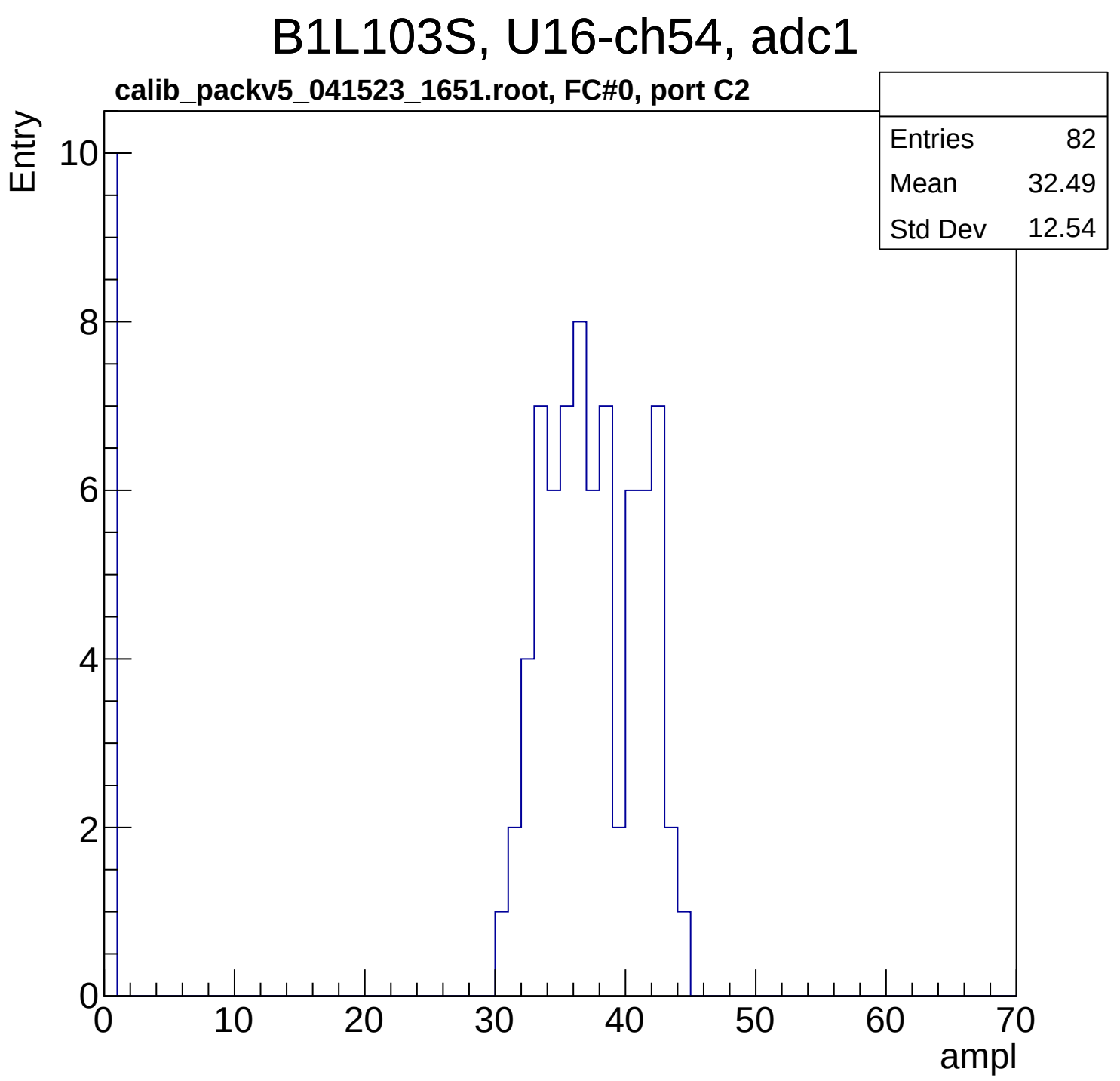
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70


B1L103S, U16-ch54, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 32.49
Std Dev 12.54
Entry
ampl
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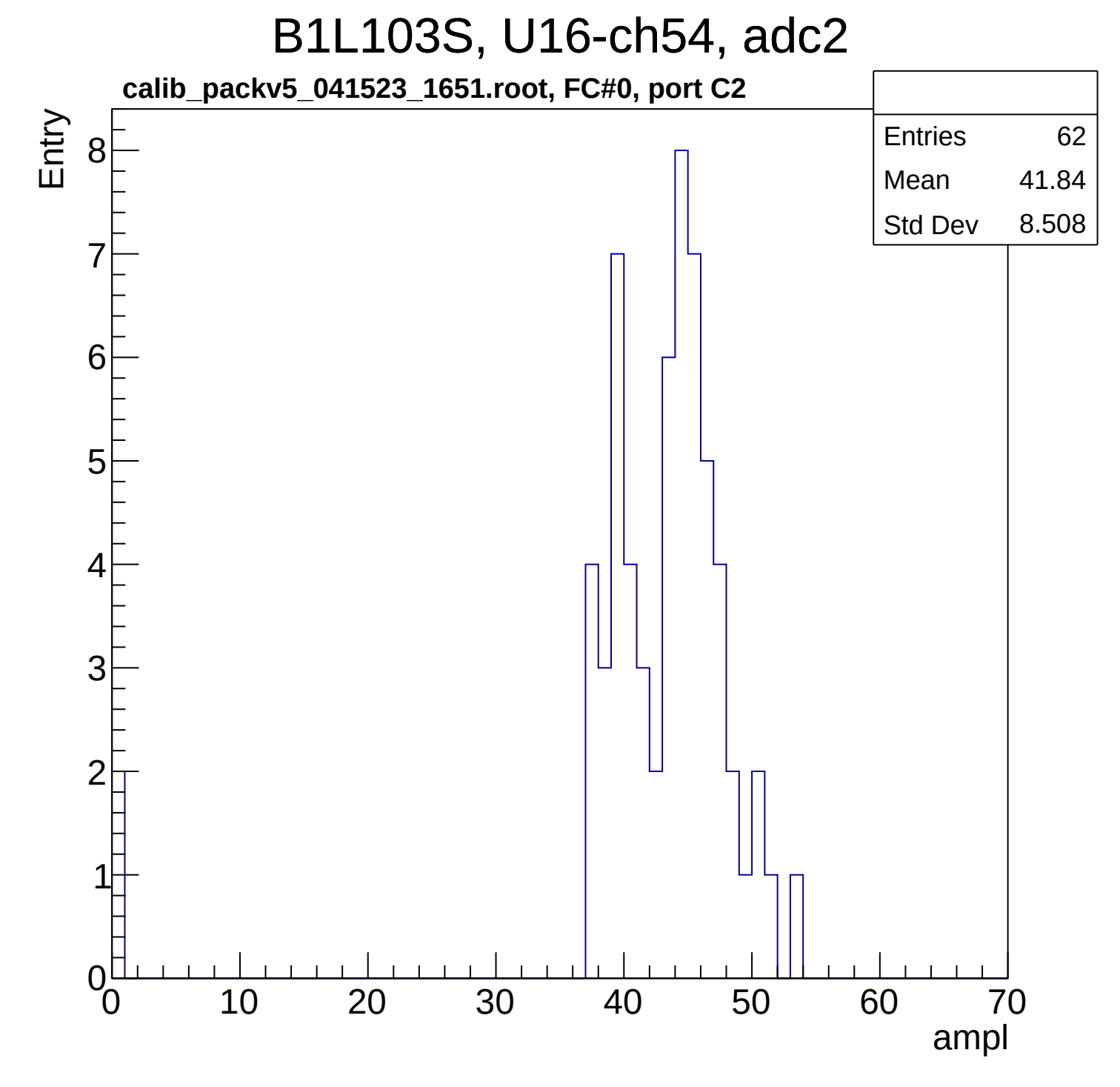
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch54, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 41.84
Std Dev 8.508
Entry
ampl
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1
2
3
4
5
6
7
8
0
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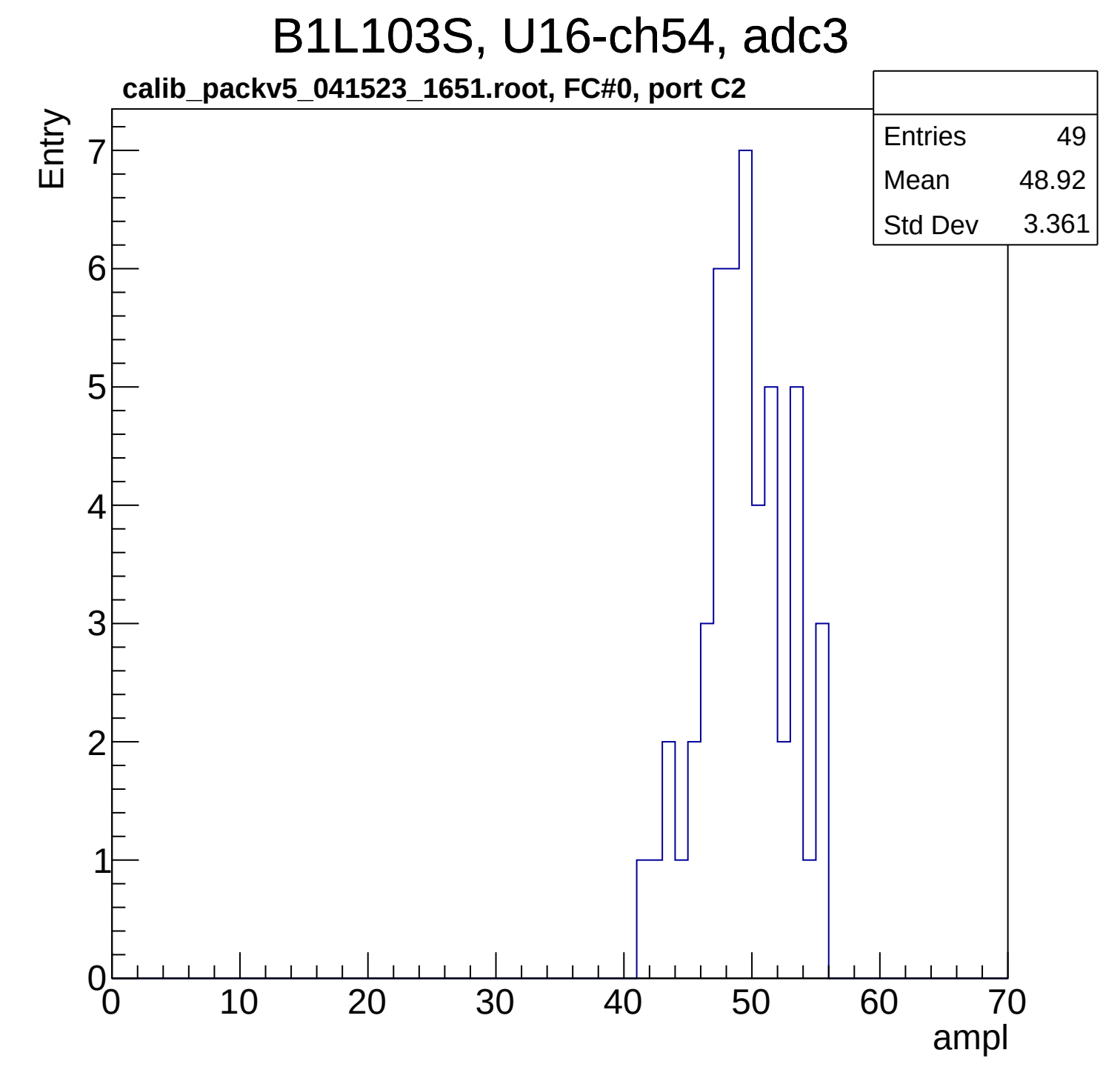
20
30
40
50
60
70


B1L103S, U16-ch54, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 48.92
Std Dev 3.361
Entry
ampl
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1
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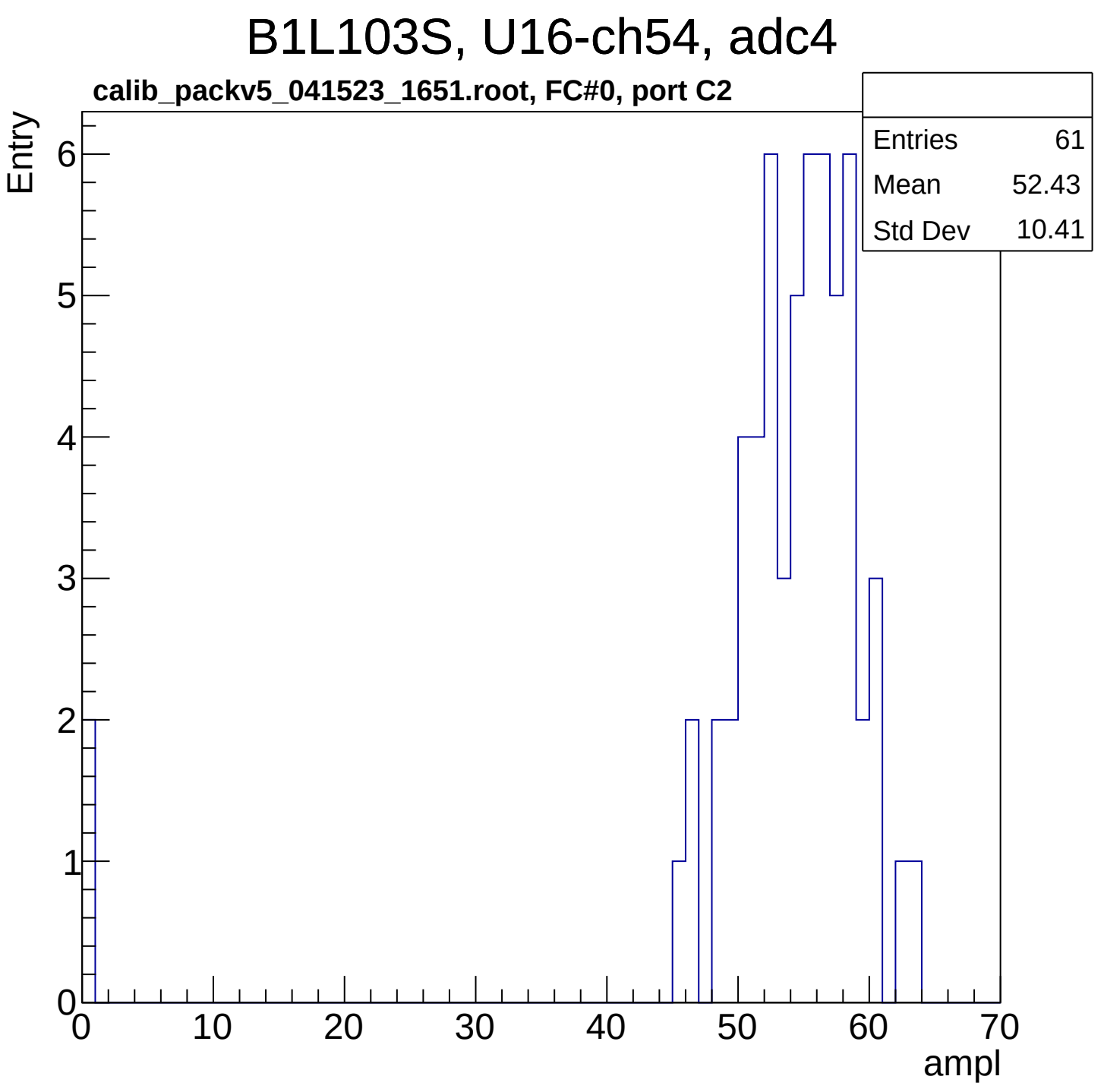
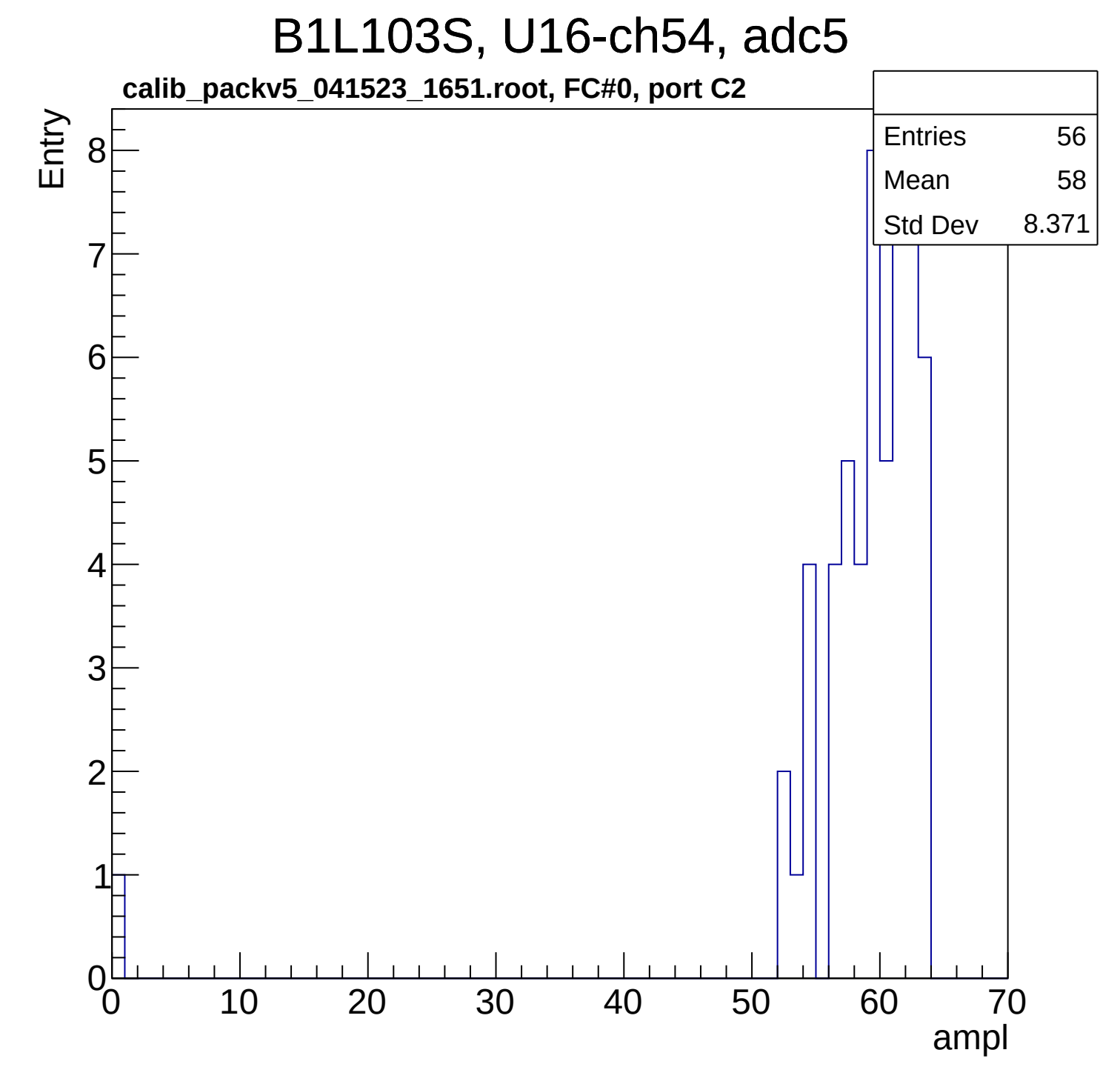
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch54, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 52.43
Std Dev 10.41
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U16-ch54, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58
Std Dev 8.371
Entry
ampl
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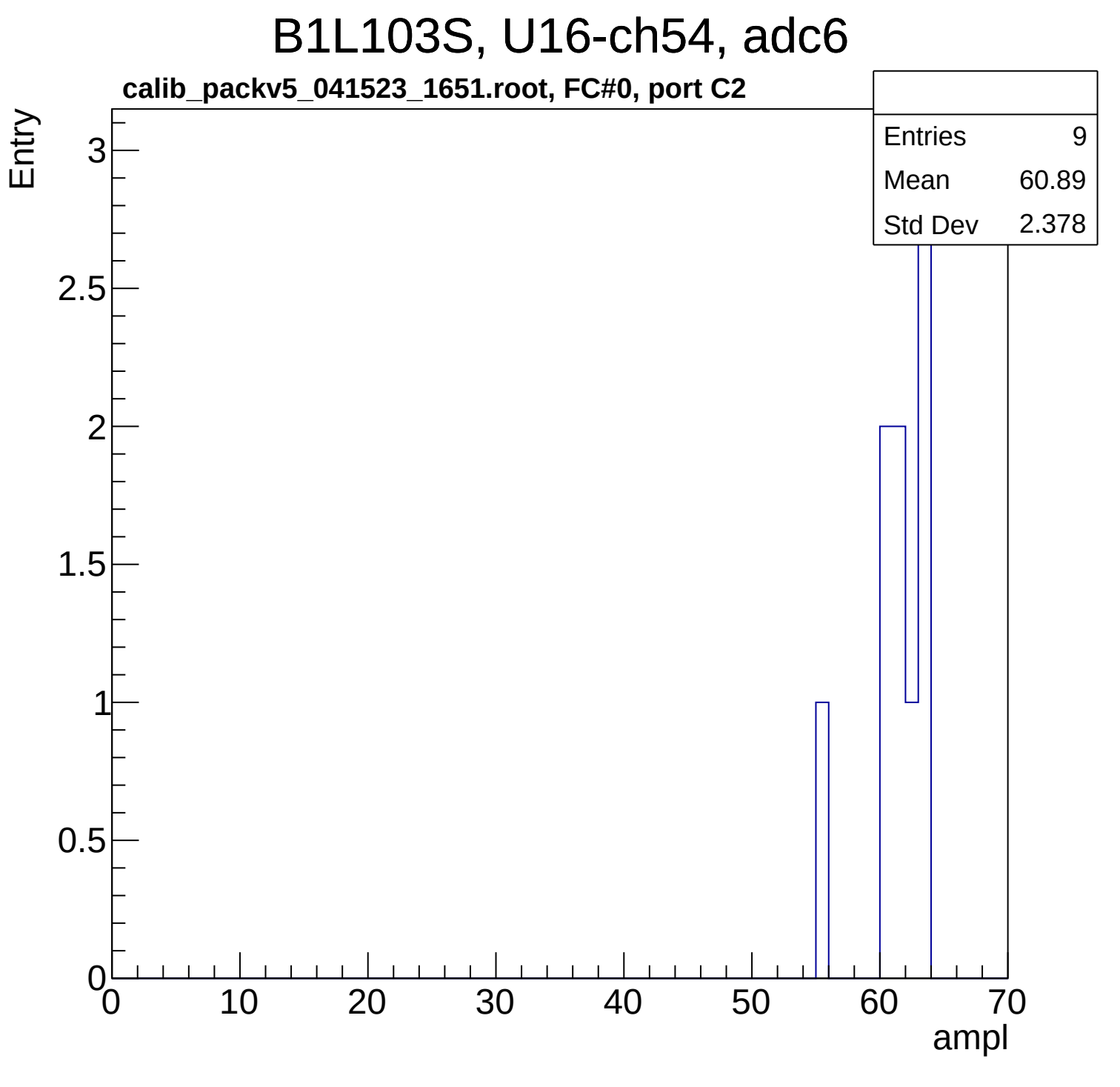
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch54, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 60.89
Std Dev 2.378
Entry
ampl
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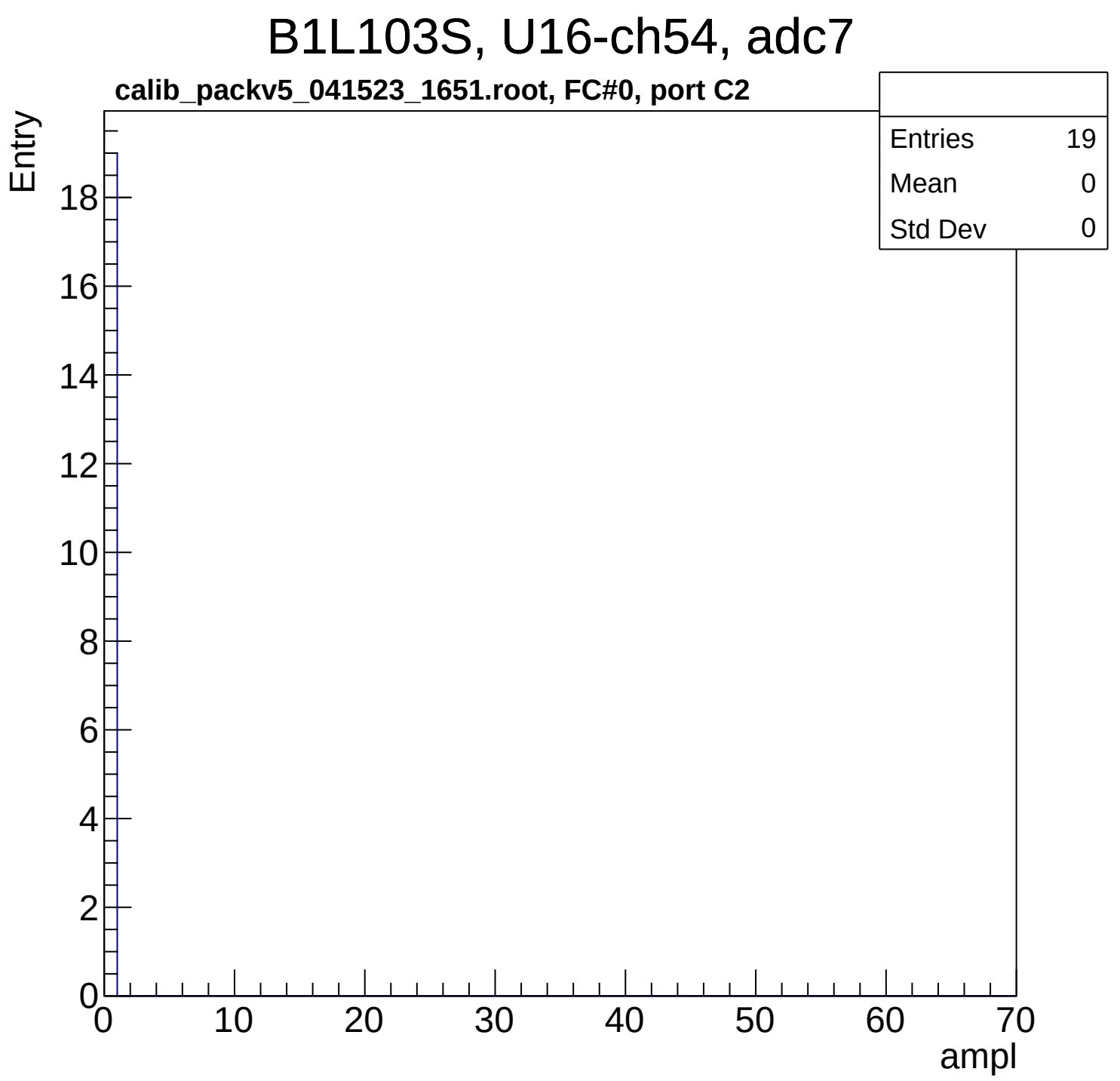
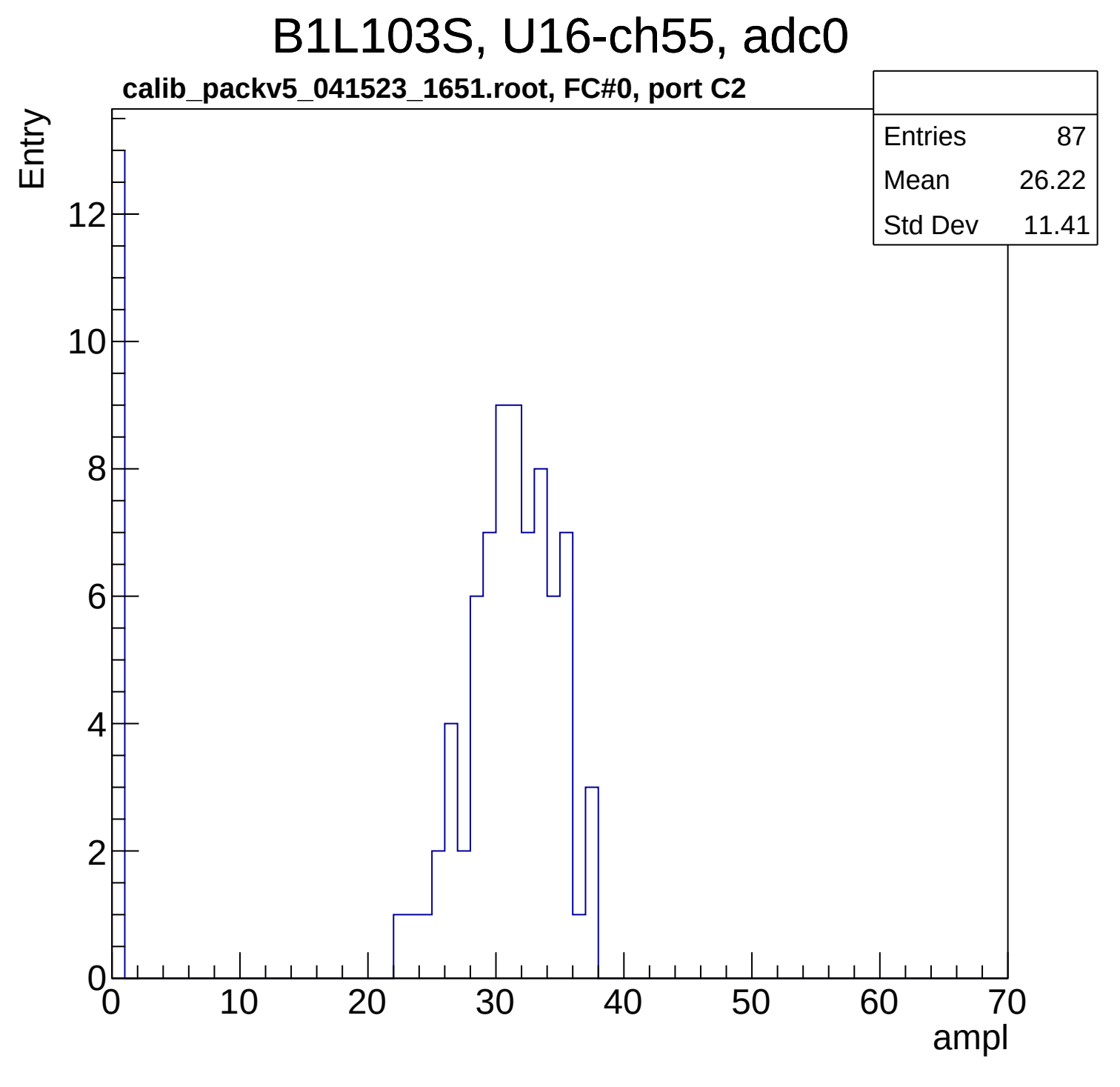
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U16-ch54, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch55, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 26.22
Std Dev 11.41
Entry
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4
6
8
10
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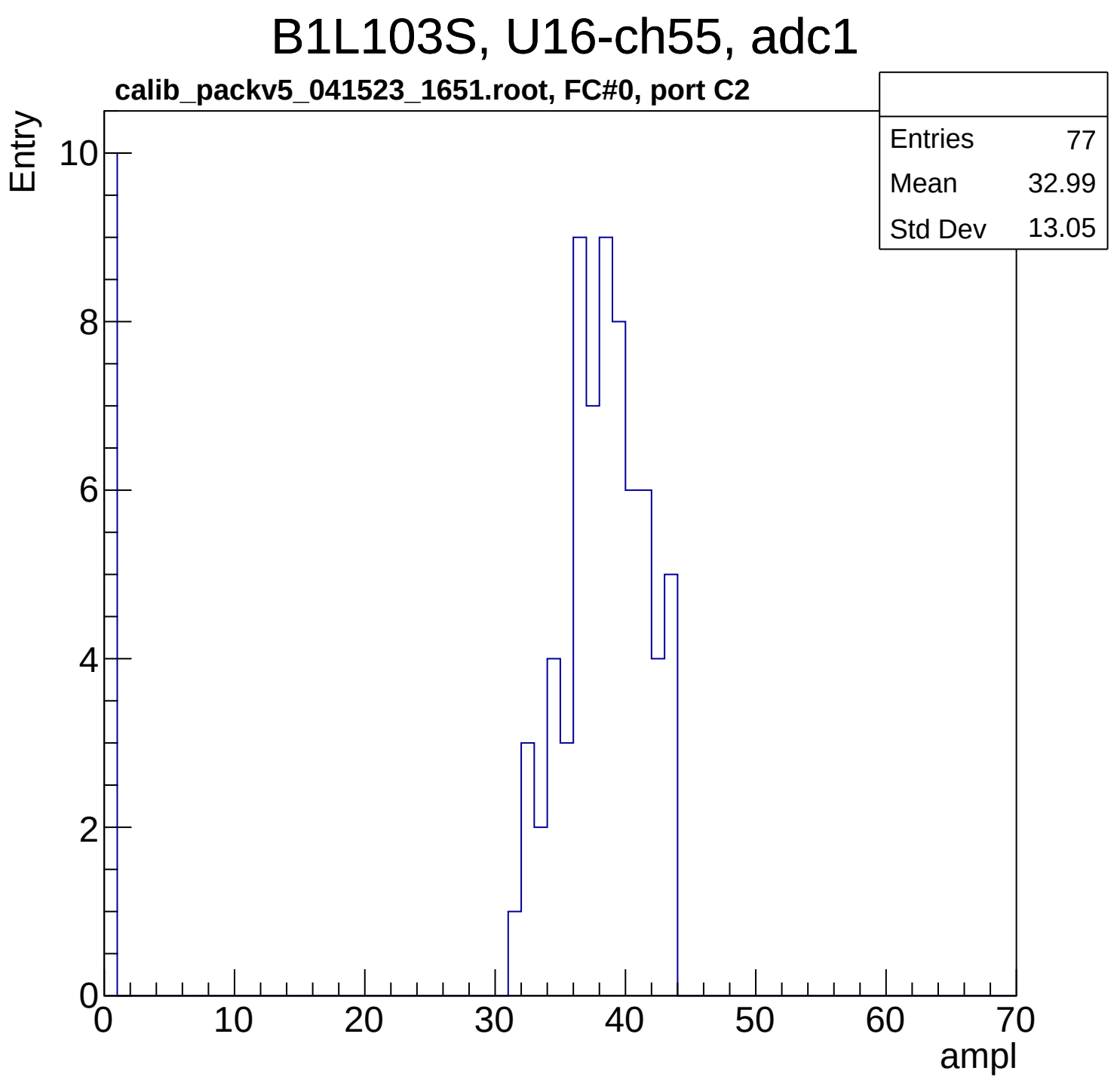
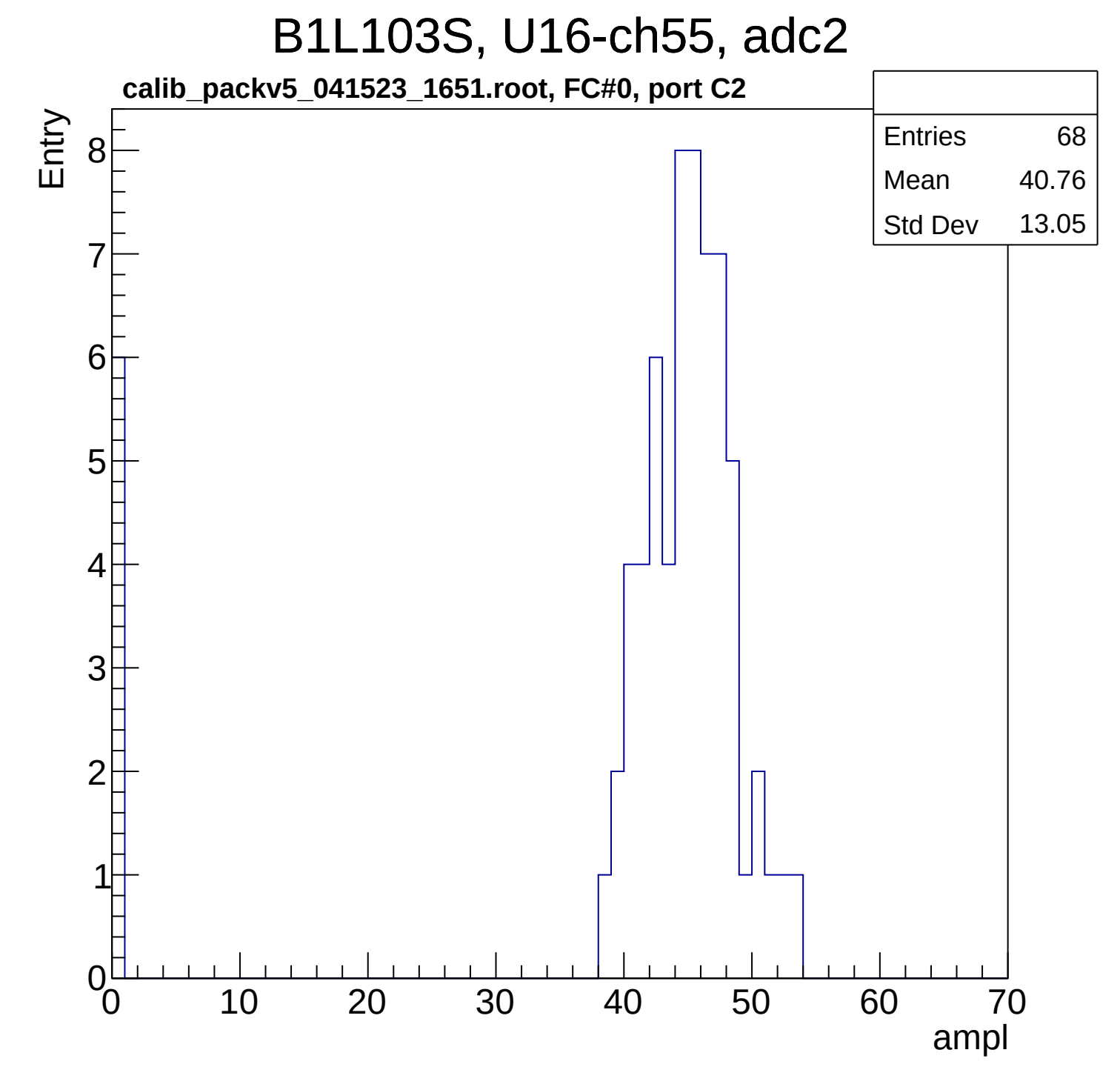
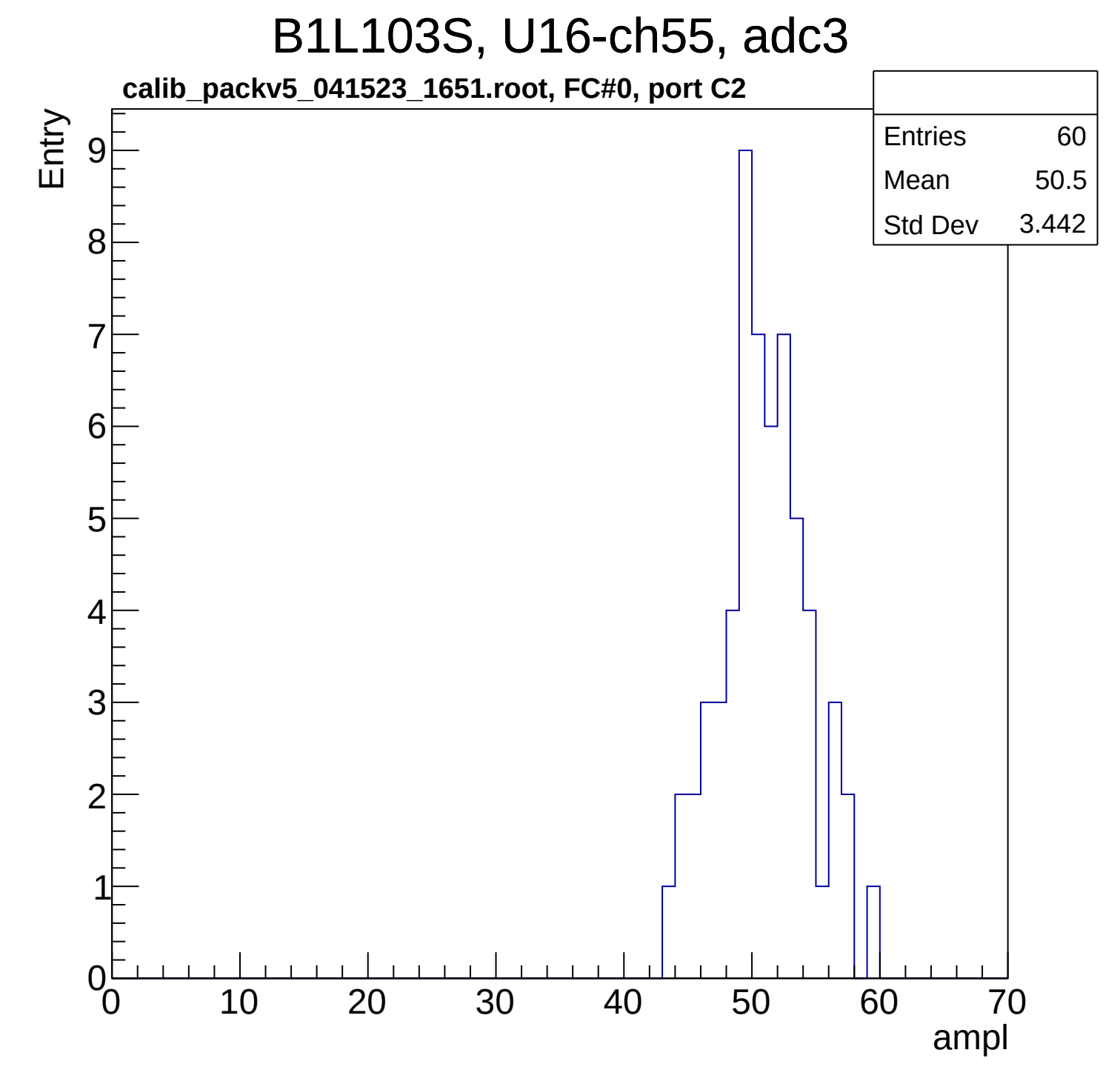
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch55, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 32.99
Std Dev 13.05
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch55, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 40.76
Std Dev 13.05
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch55, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 50.5
Std Dev 3.442
Entry
ampl
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2
3
4
5
6
7
8
9
0
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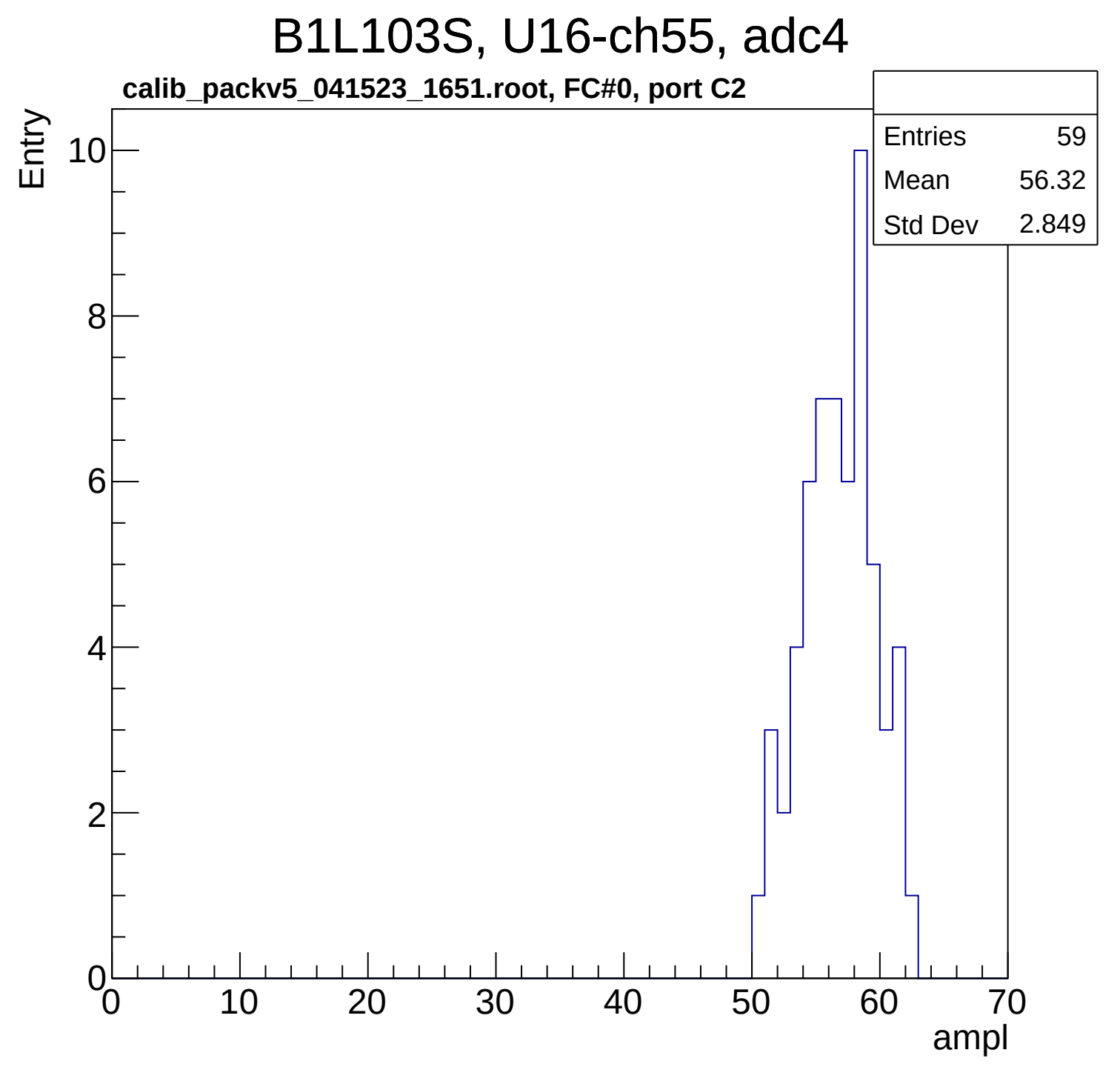
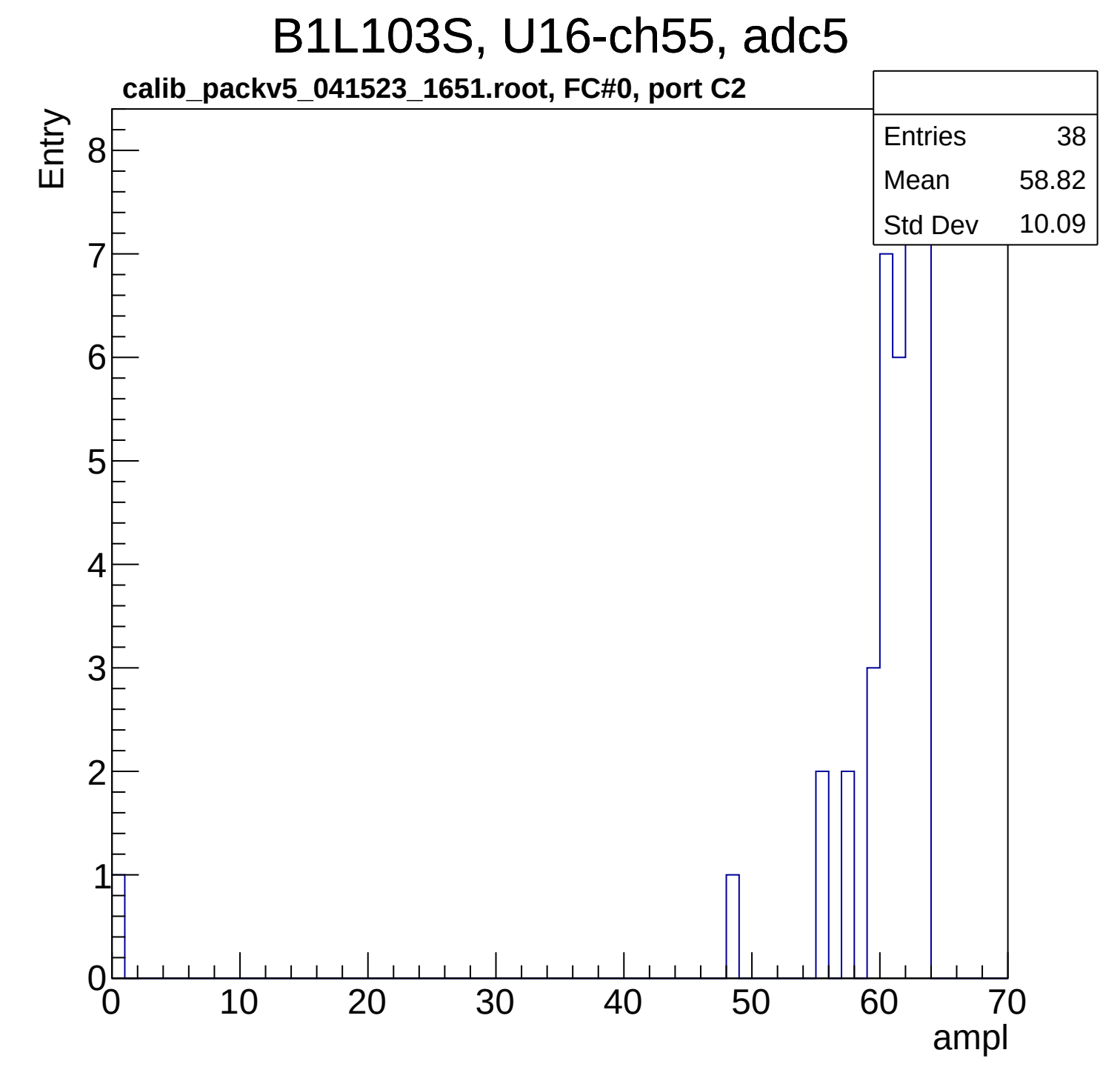
20
30
40
50
60
70


B1L103S, U16-ch55, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 56.32
Std Dev 2.849
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch55, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 58.82
Std Dev 10.09
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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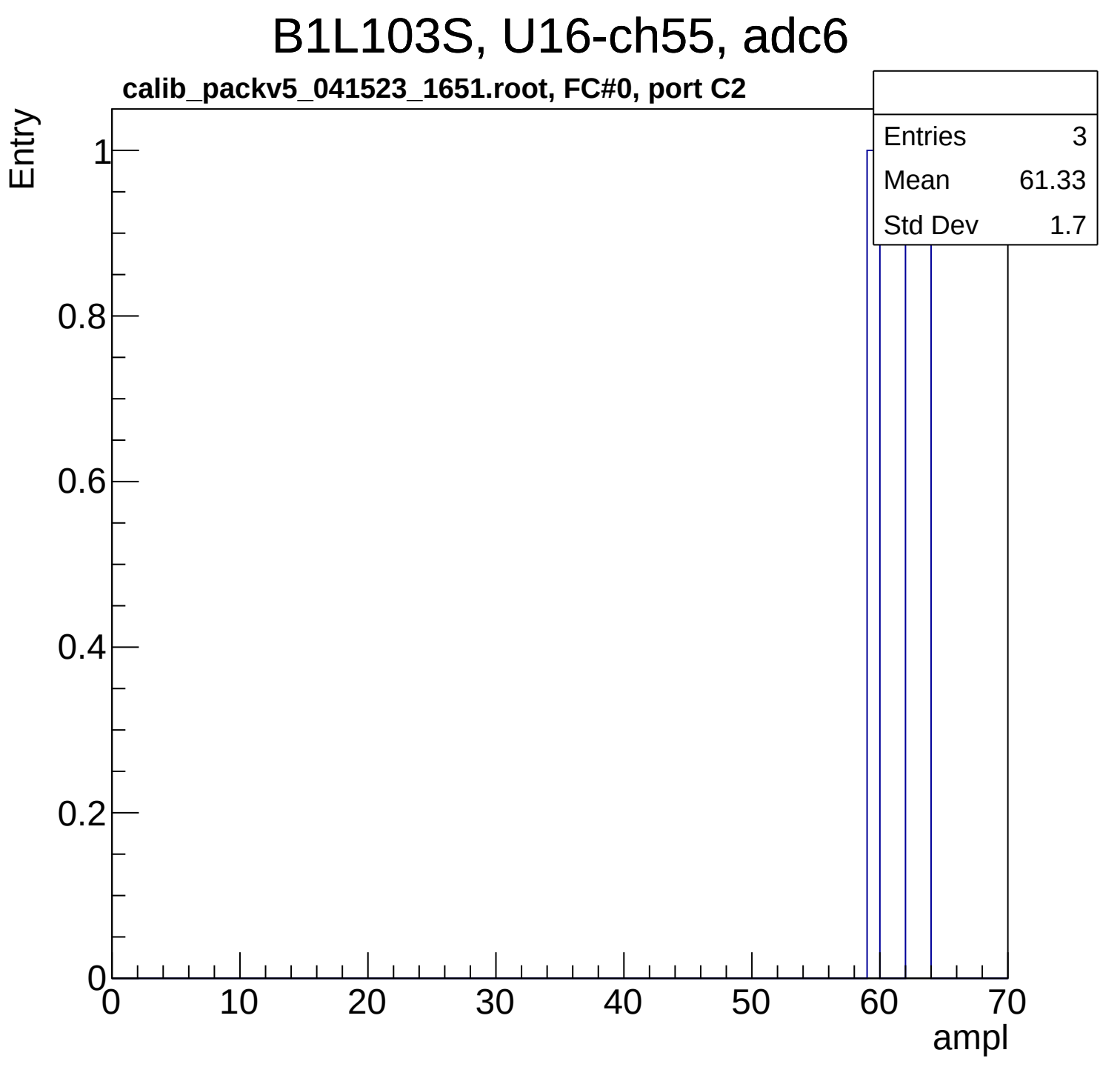
40
50
60
70


B1L103S, U16-ch55, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 61.33
Std Dev 1.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
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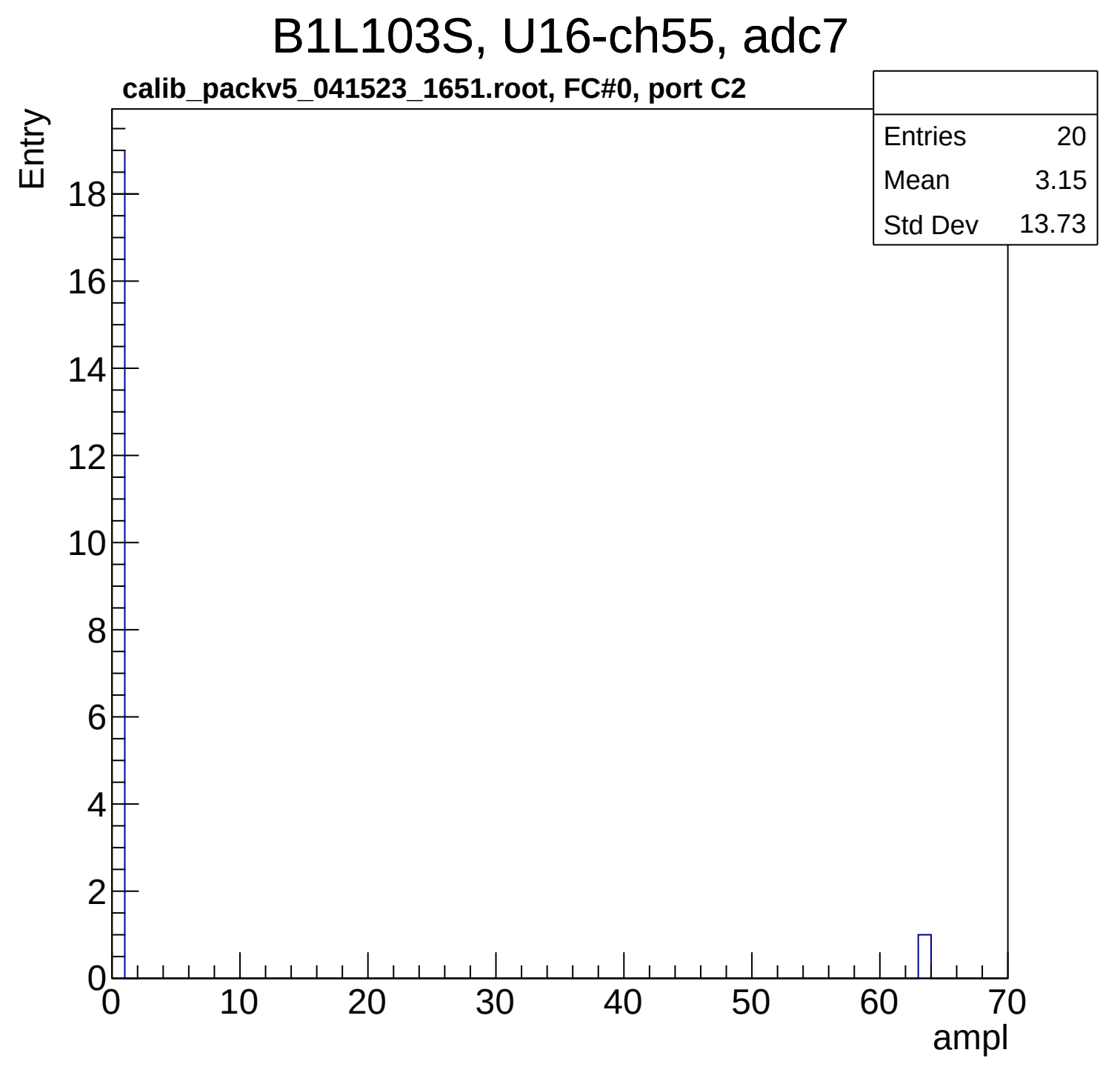
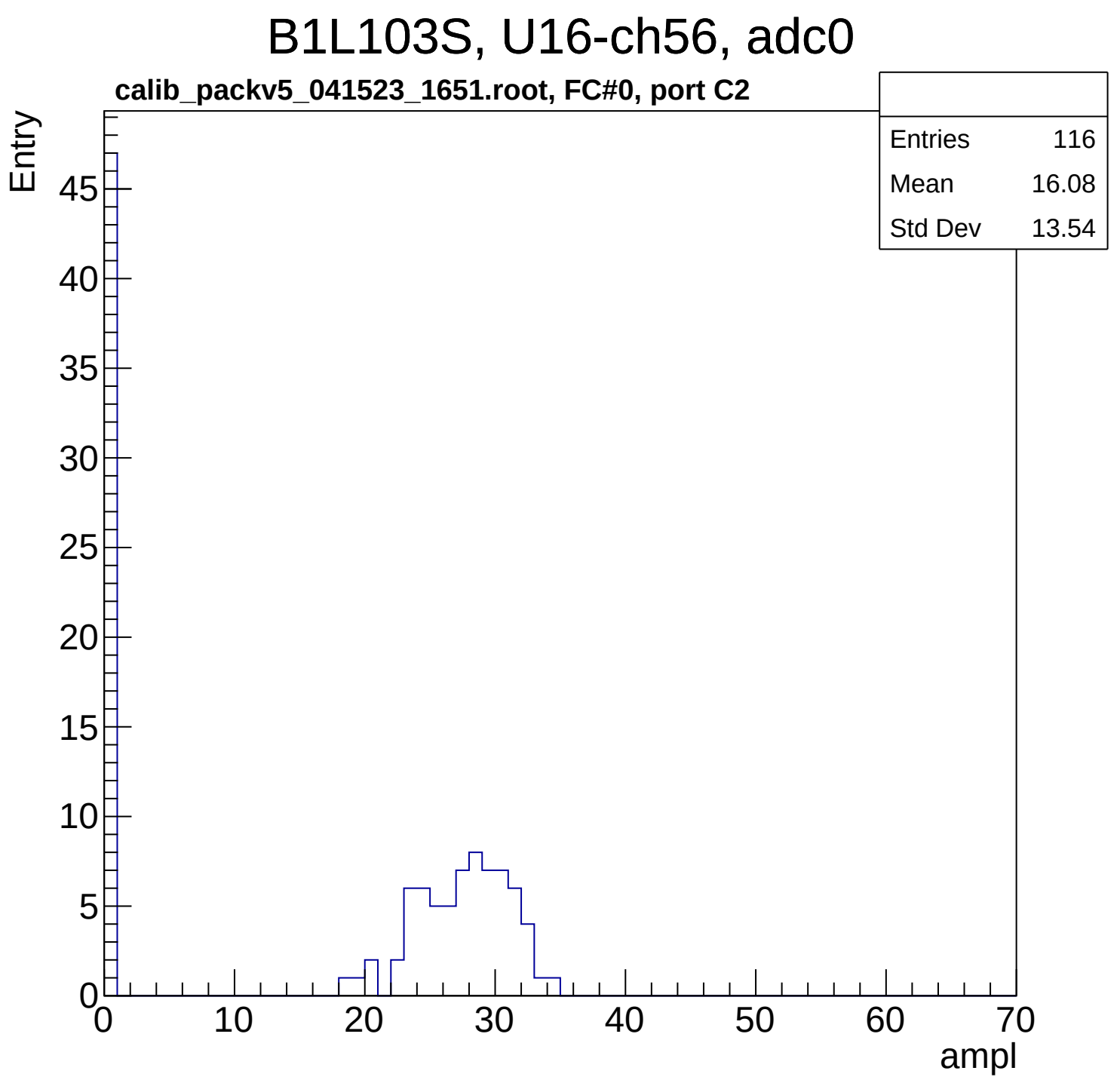
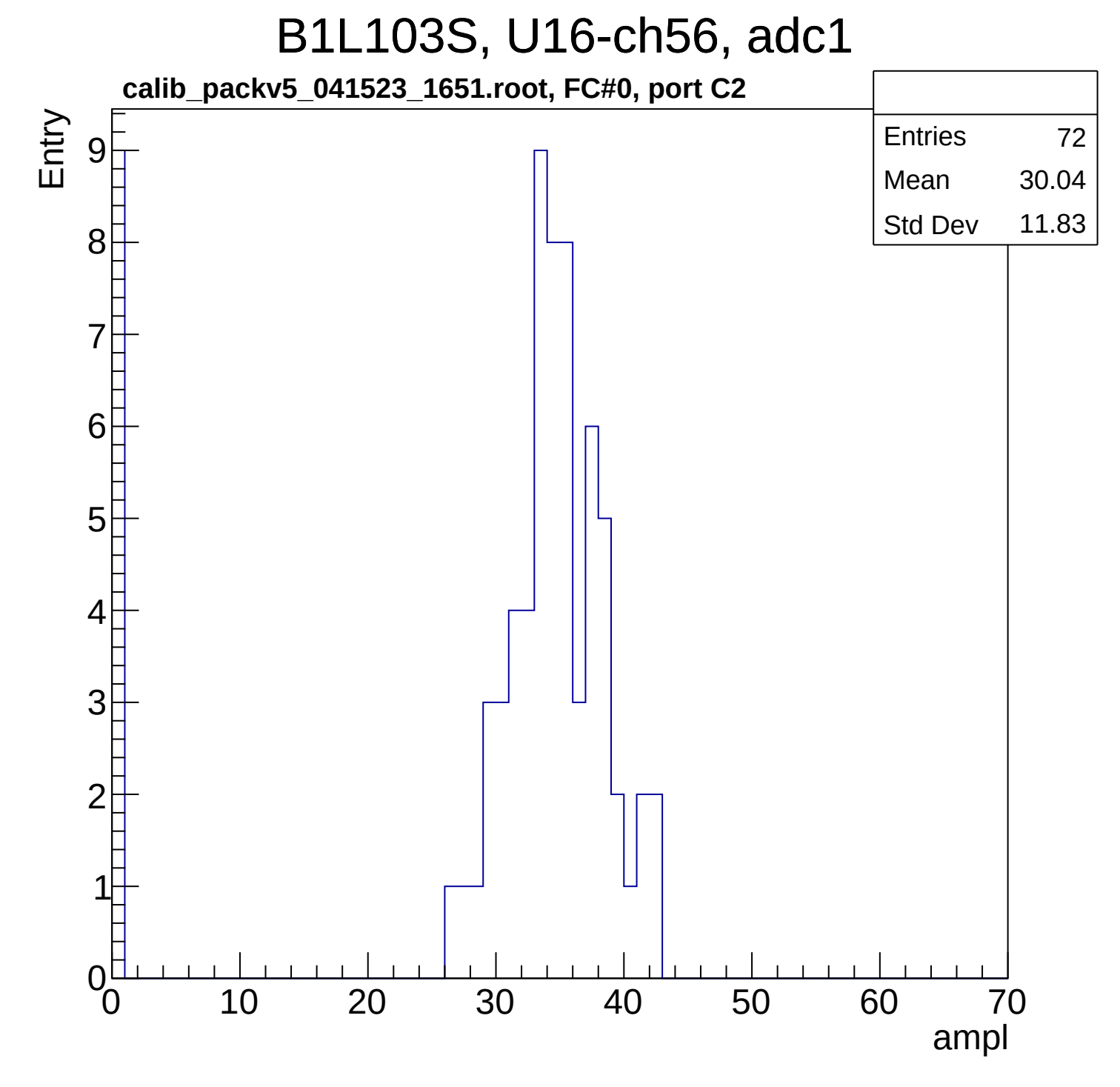

B1L103S, U16-ch55, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch56, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 116
Mean 16.08
Std Dev 13.54
Entry
0
5
10
15
20
25
30
35
40
45
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch56, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 30.04
Std Dev 11.83
Entry
ampl
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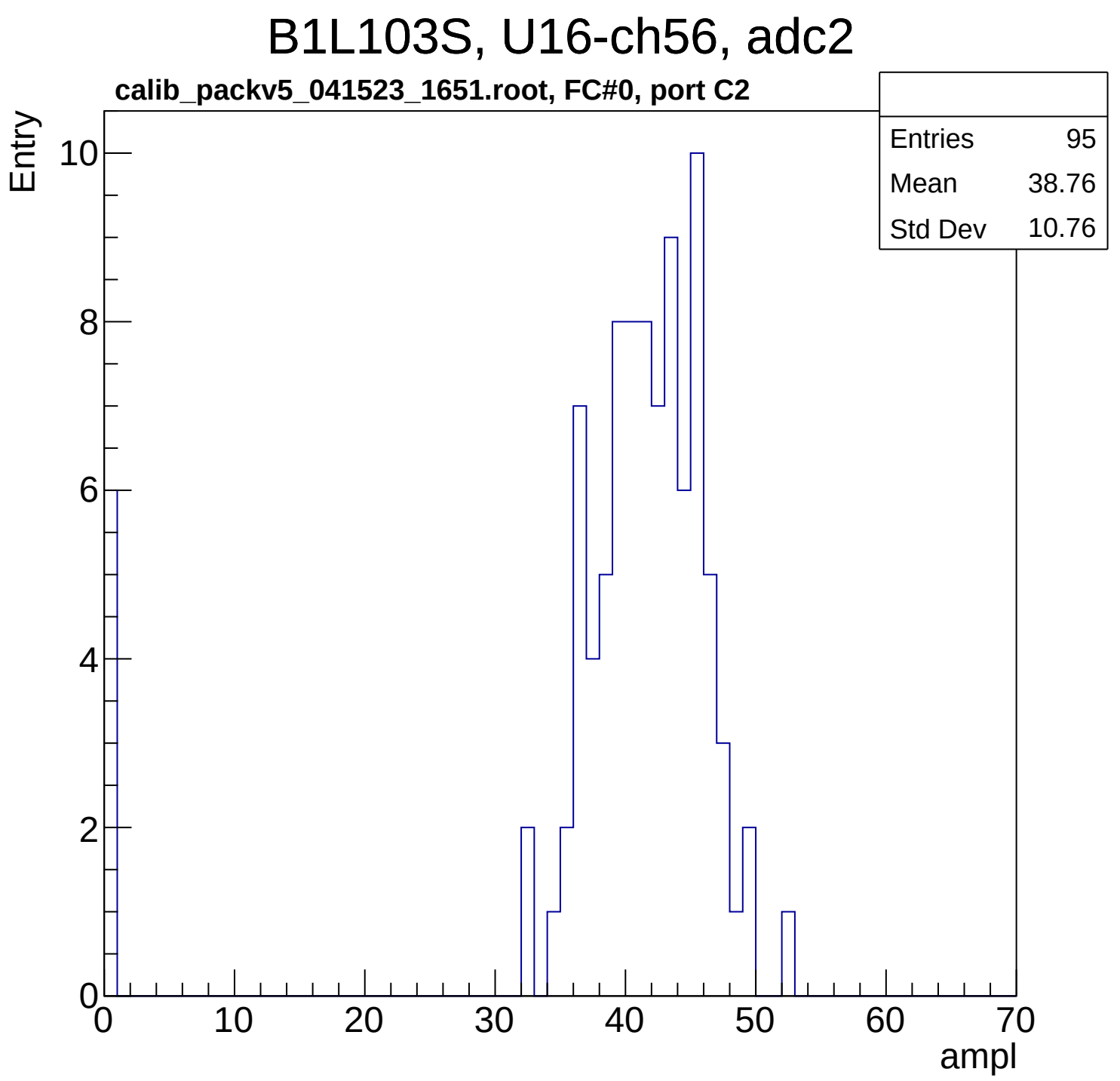
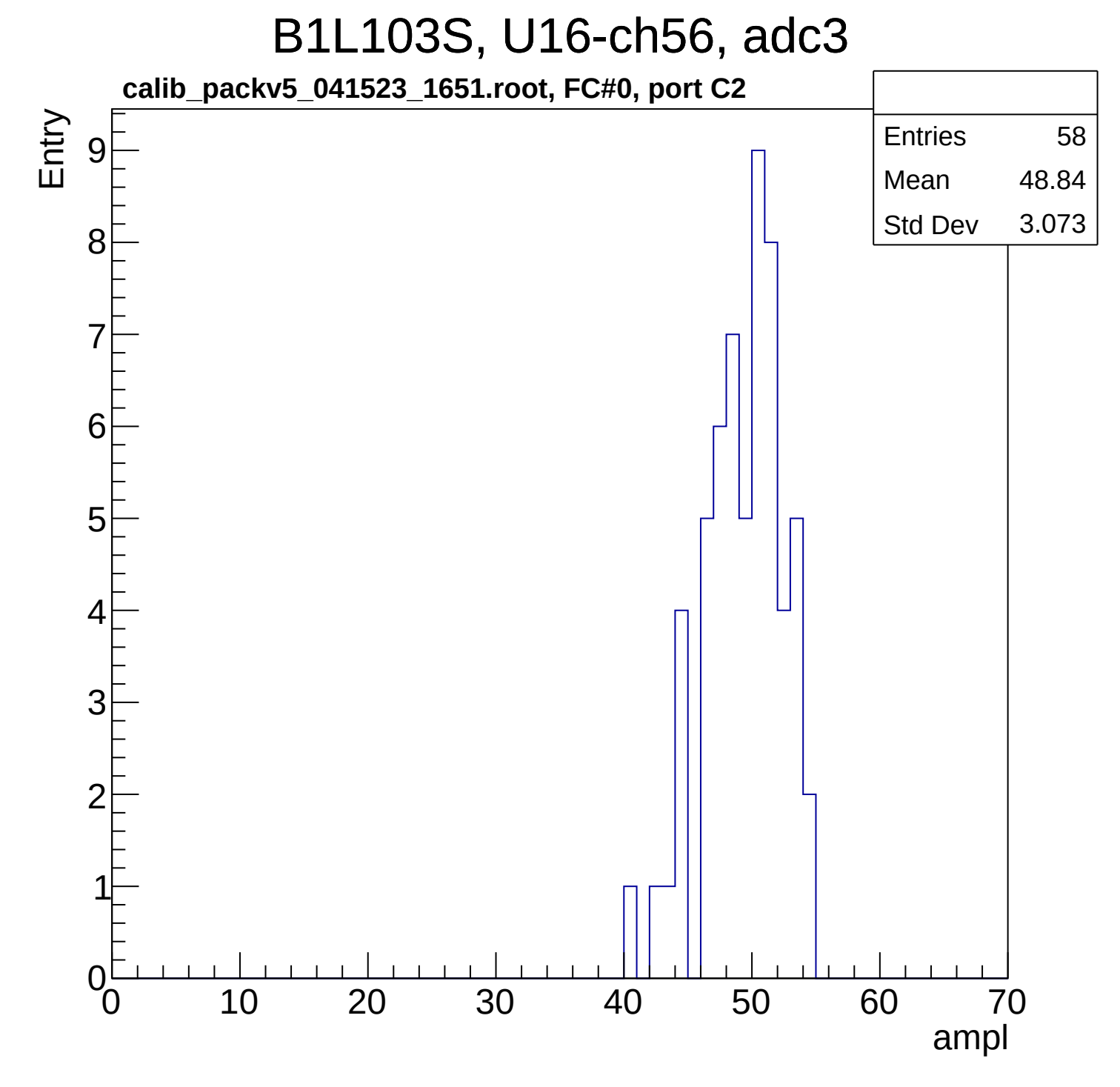
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch56, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 38.76
Std Dev 10.76
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch56, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 48.84
Std Dev 3.073
Entry
ampl
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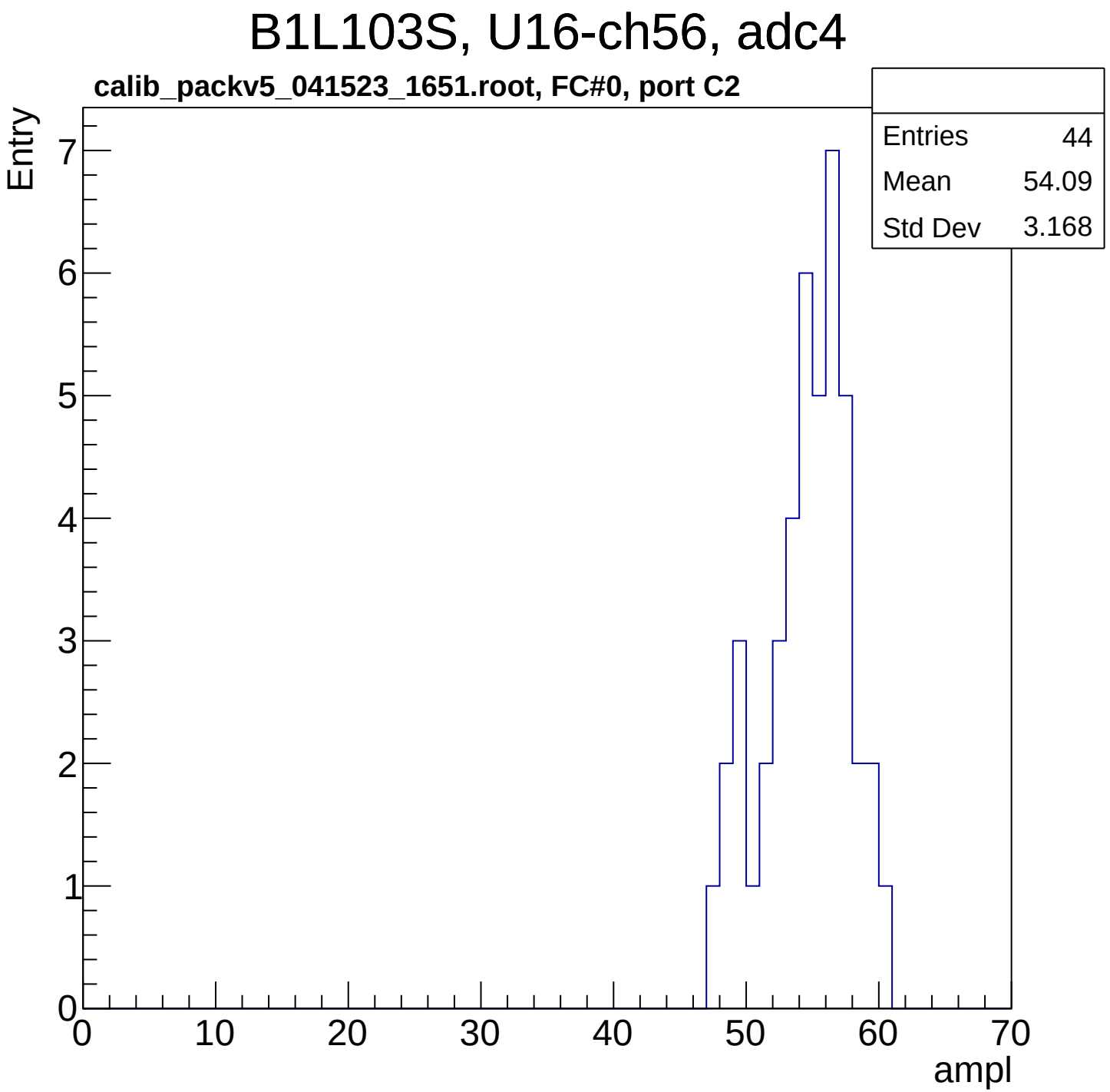
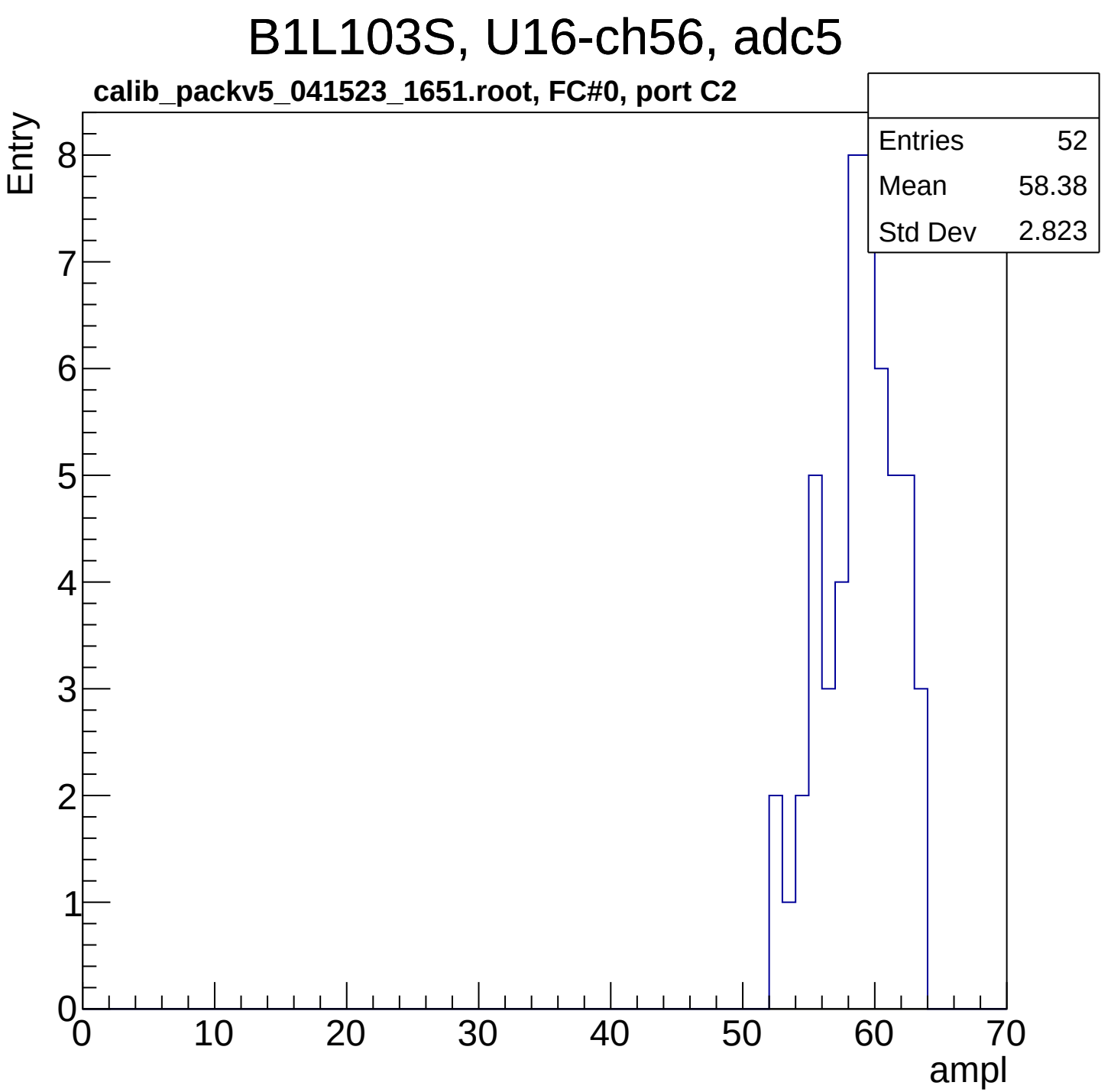
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch56, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 54.09
Std Dev 3.168
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch56, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.38
Std Dev 2.823
Entry
ampl
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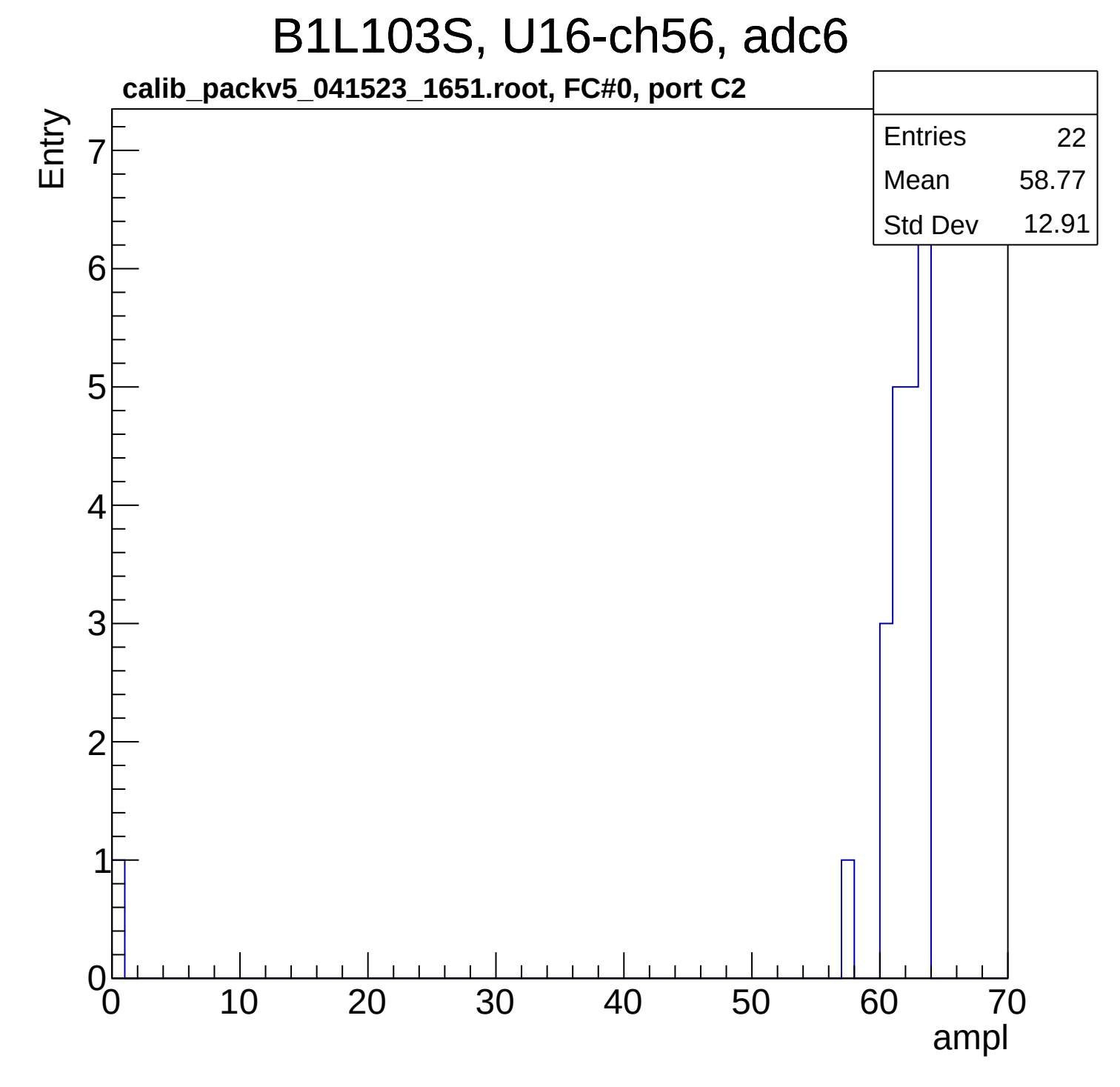
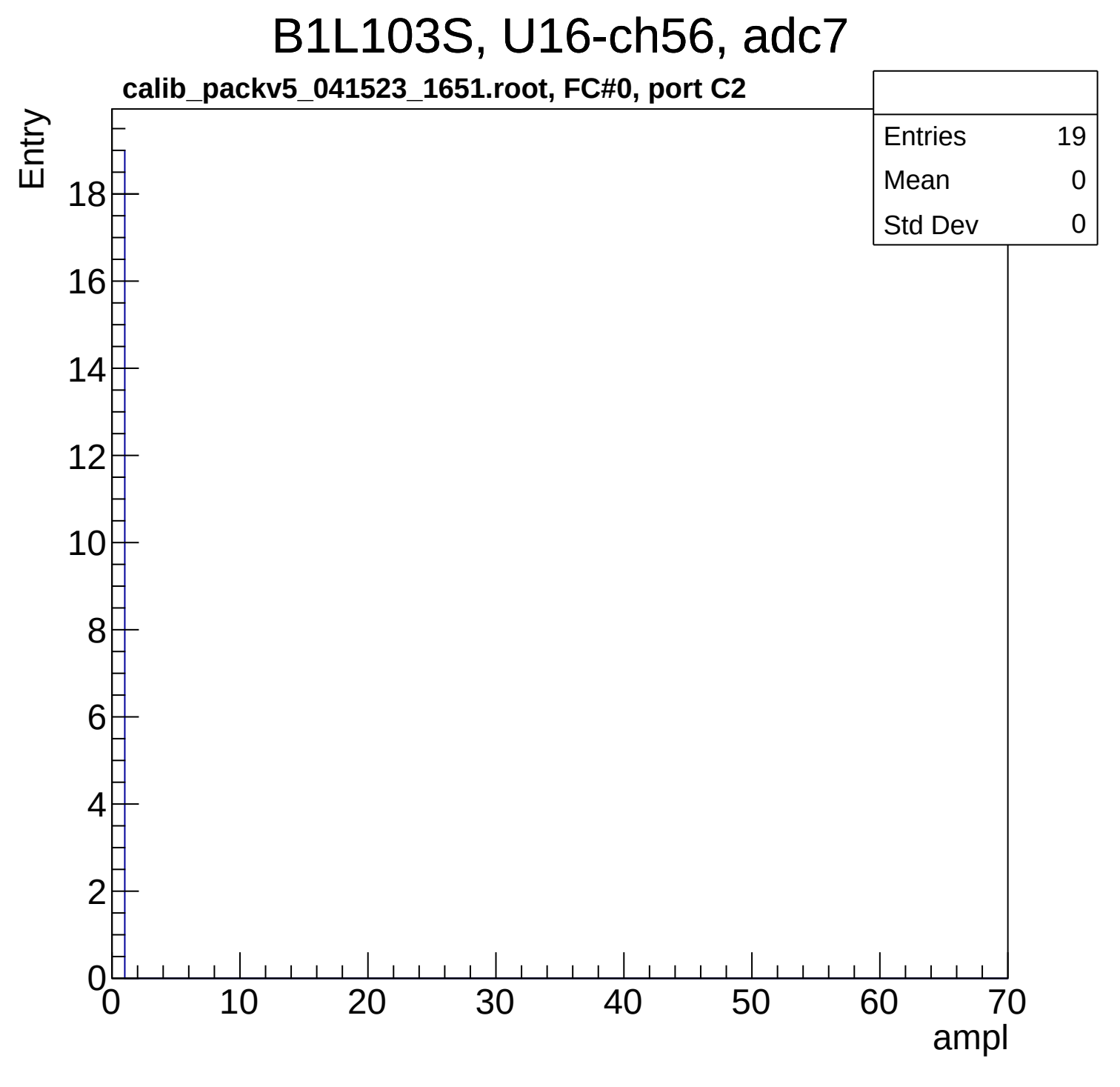
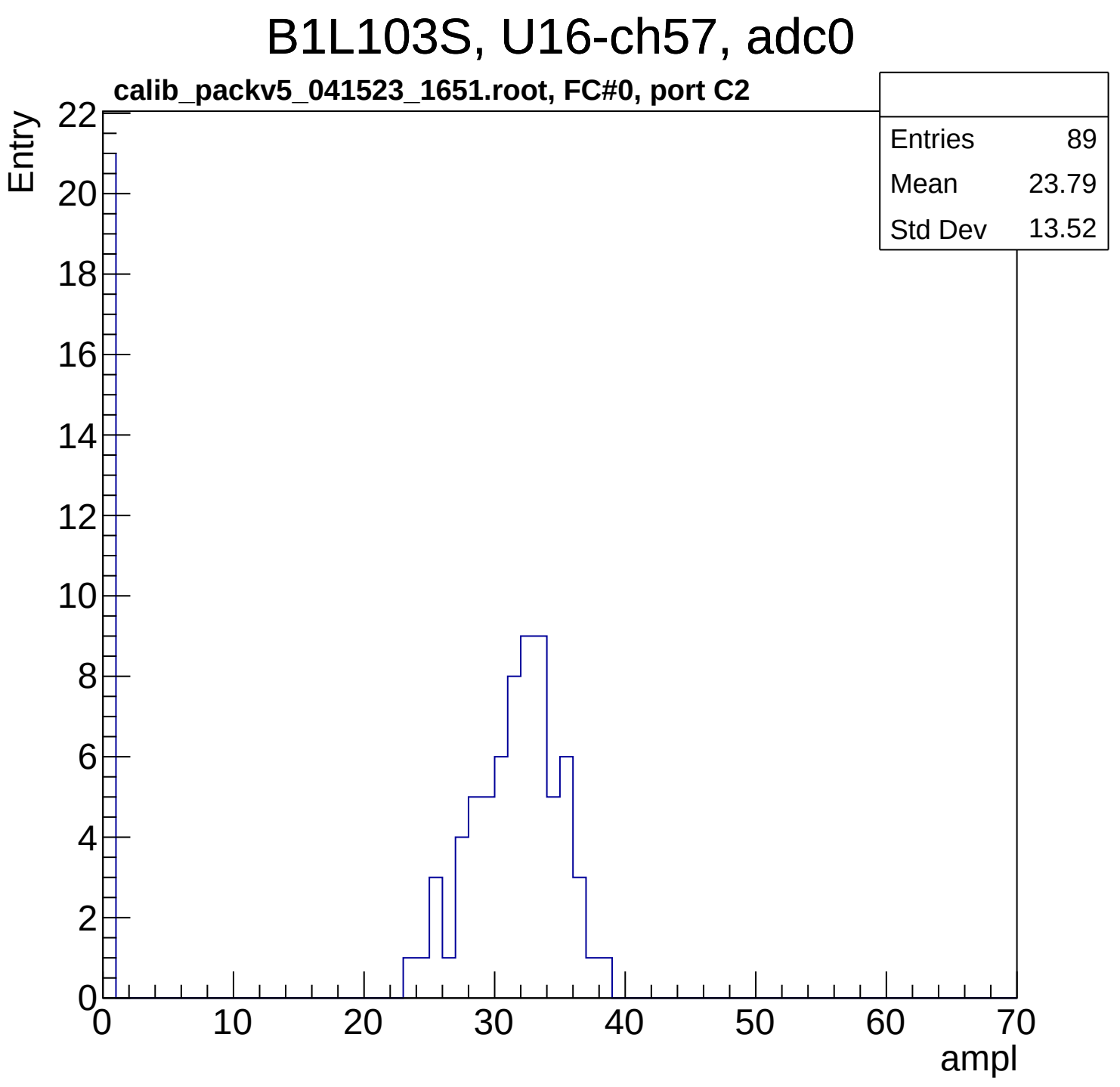
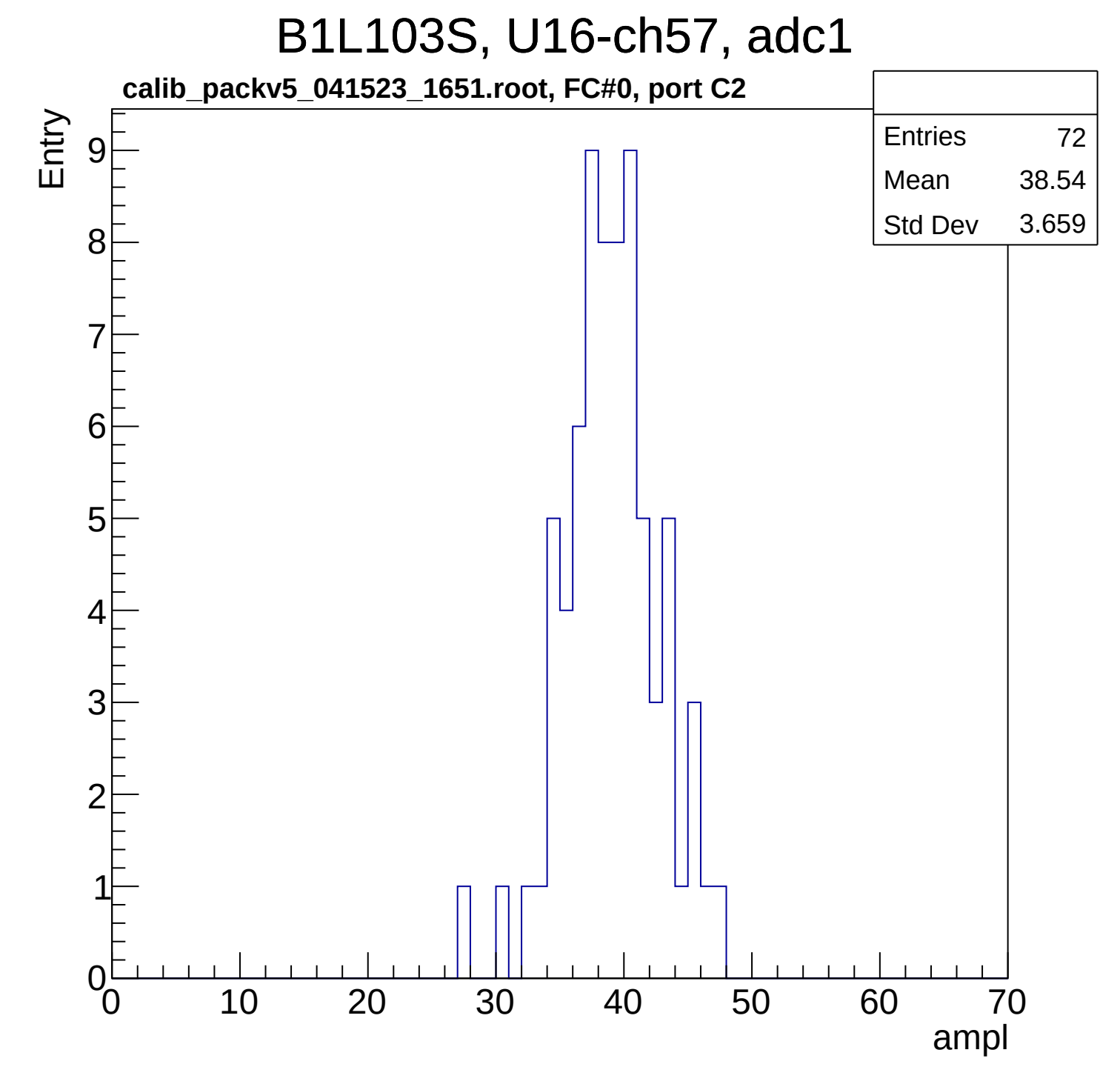
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch56, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.77
Std Dev 12.91
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch56, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch57, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 23.79
Std Dev 13.52
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U16-ch57, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 38.54
Std Dev 3.659
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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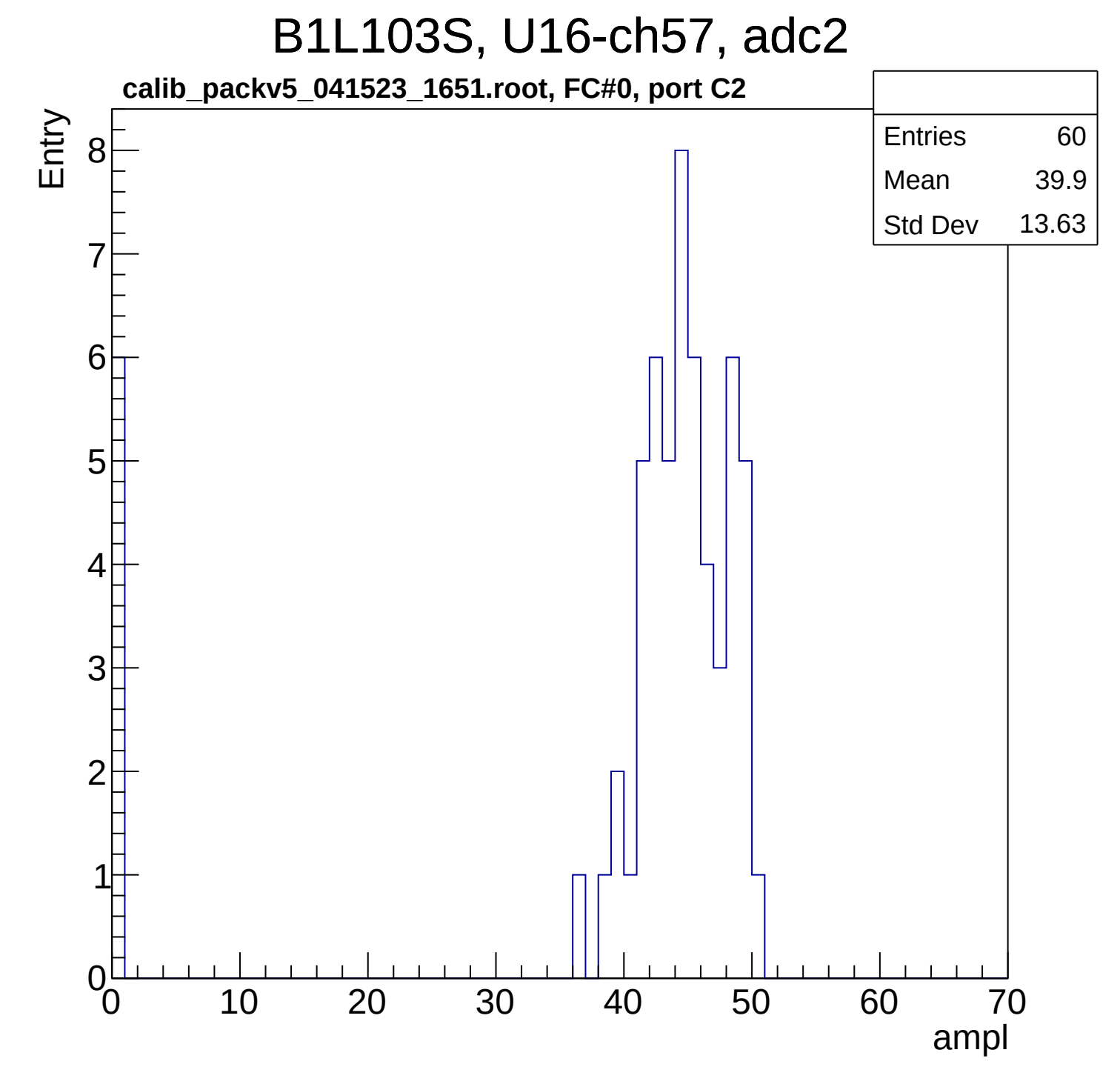
B1L103S, U16-ch57, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 39.9
Std Dev 13.63
Entry
ampl
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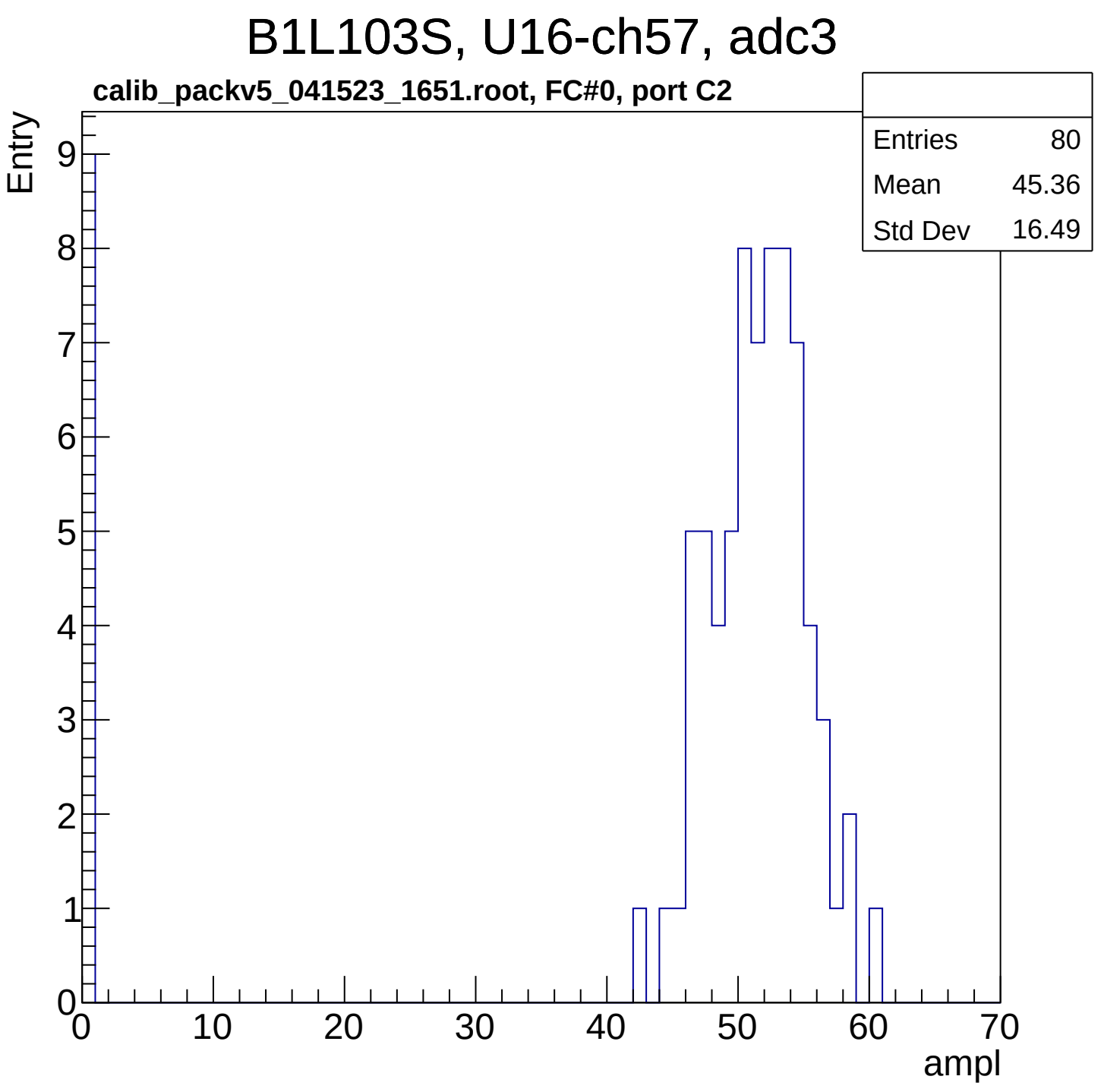
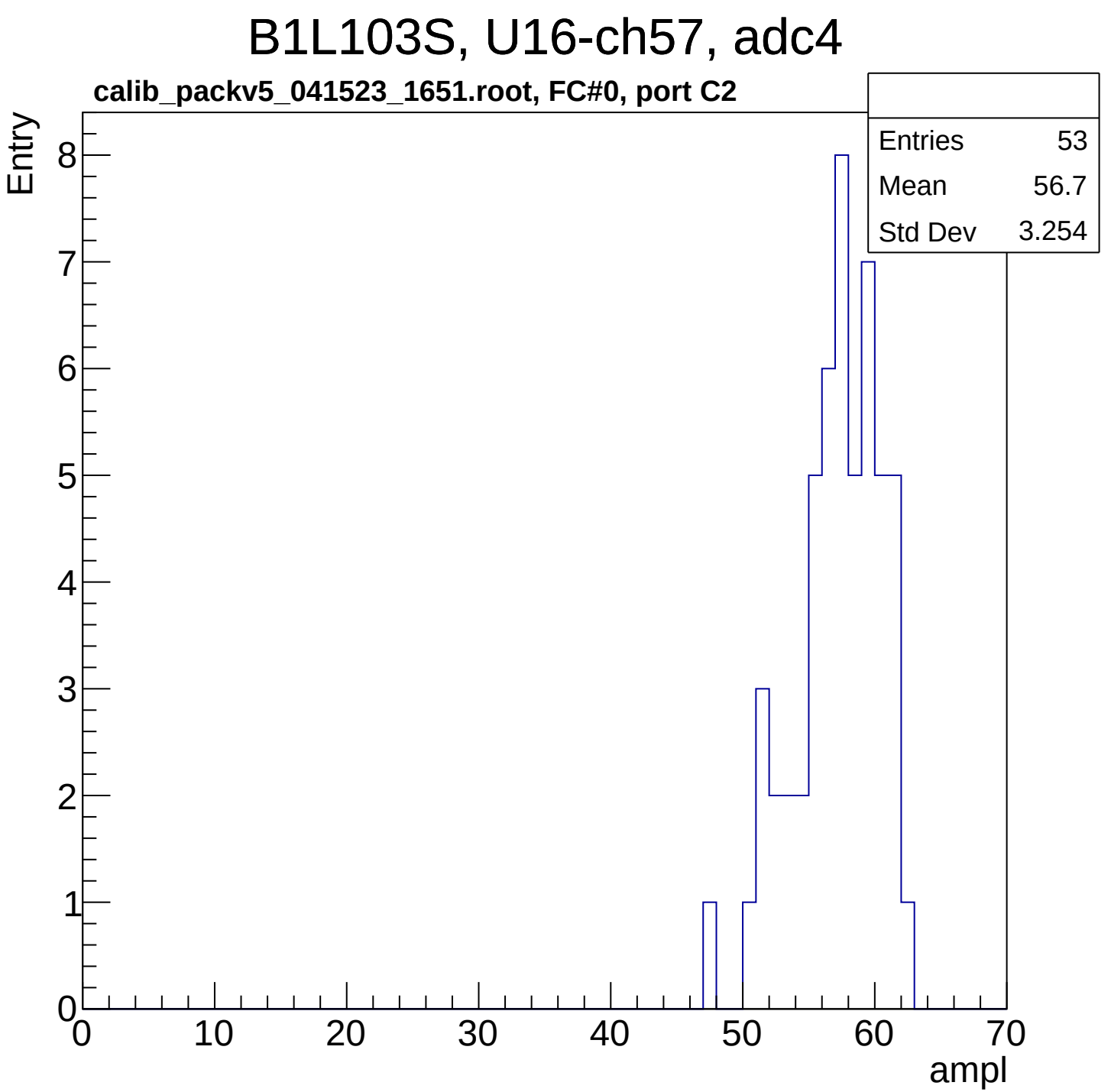
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch57, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 45.36
Std Dev 16.49
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch57, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 56.7
Std Dev 3.254
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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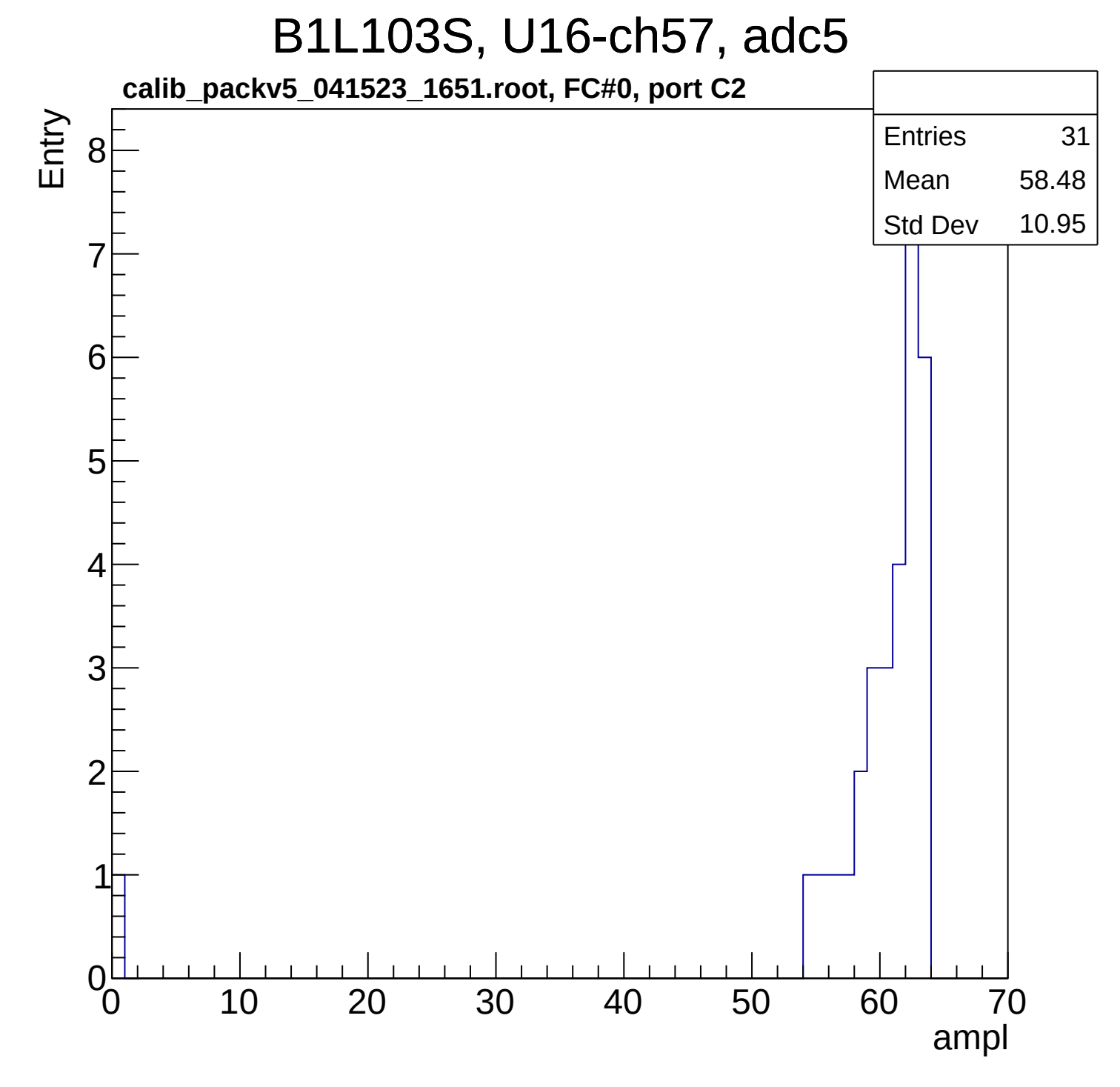
B1L103S, U16-ch57, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 58.48
Std Dev 10.95
Entry
ampl
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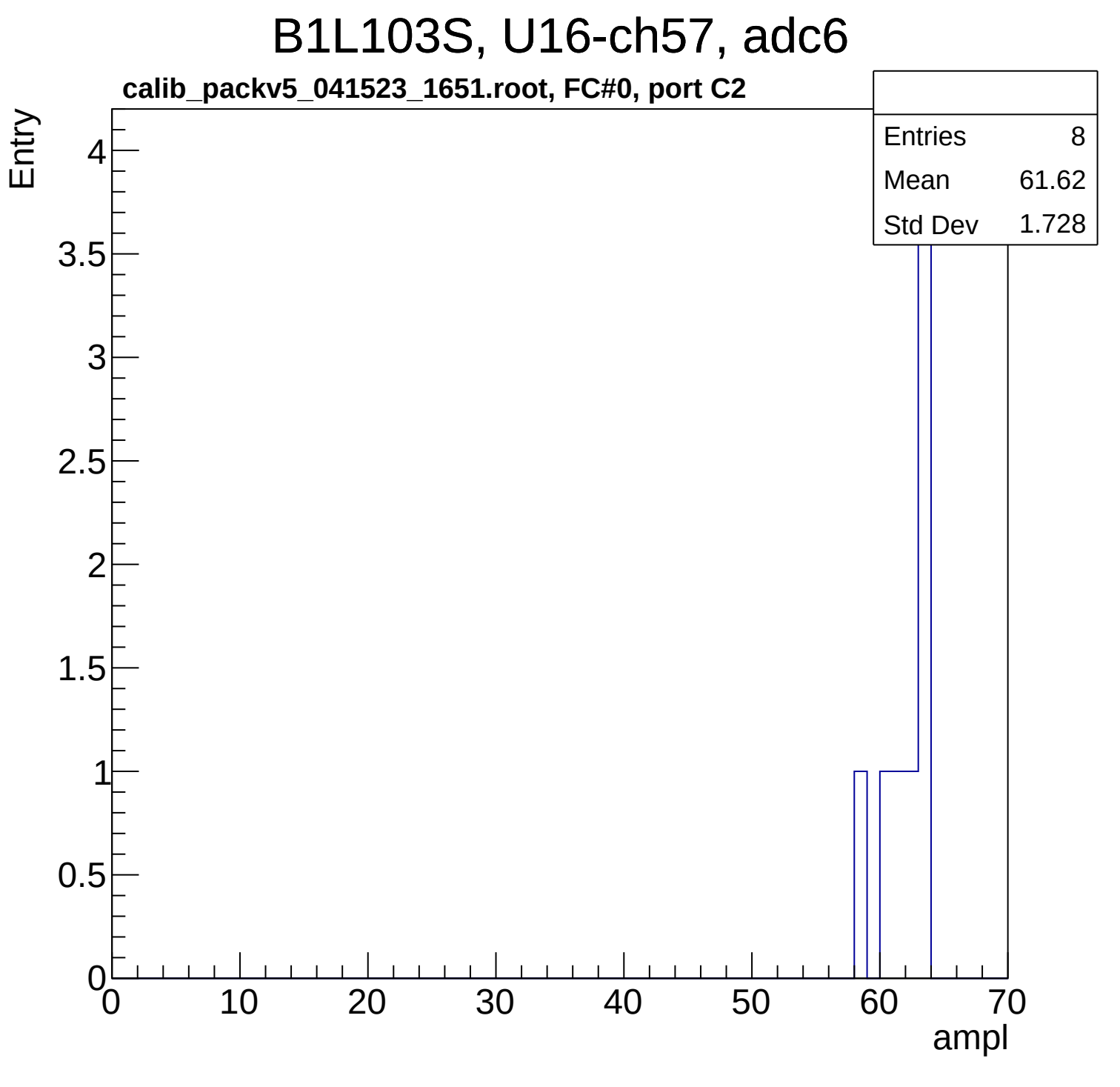
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch57, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.62
Std Dev 1.728
Entry
ampl
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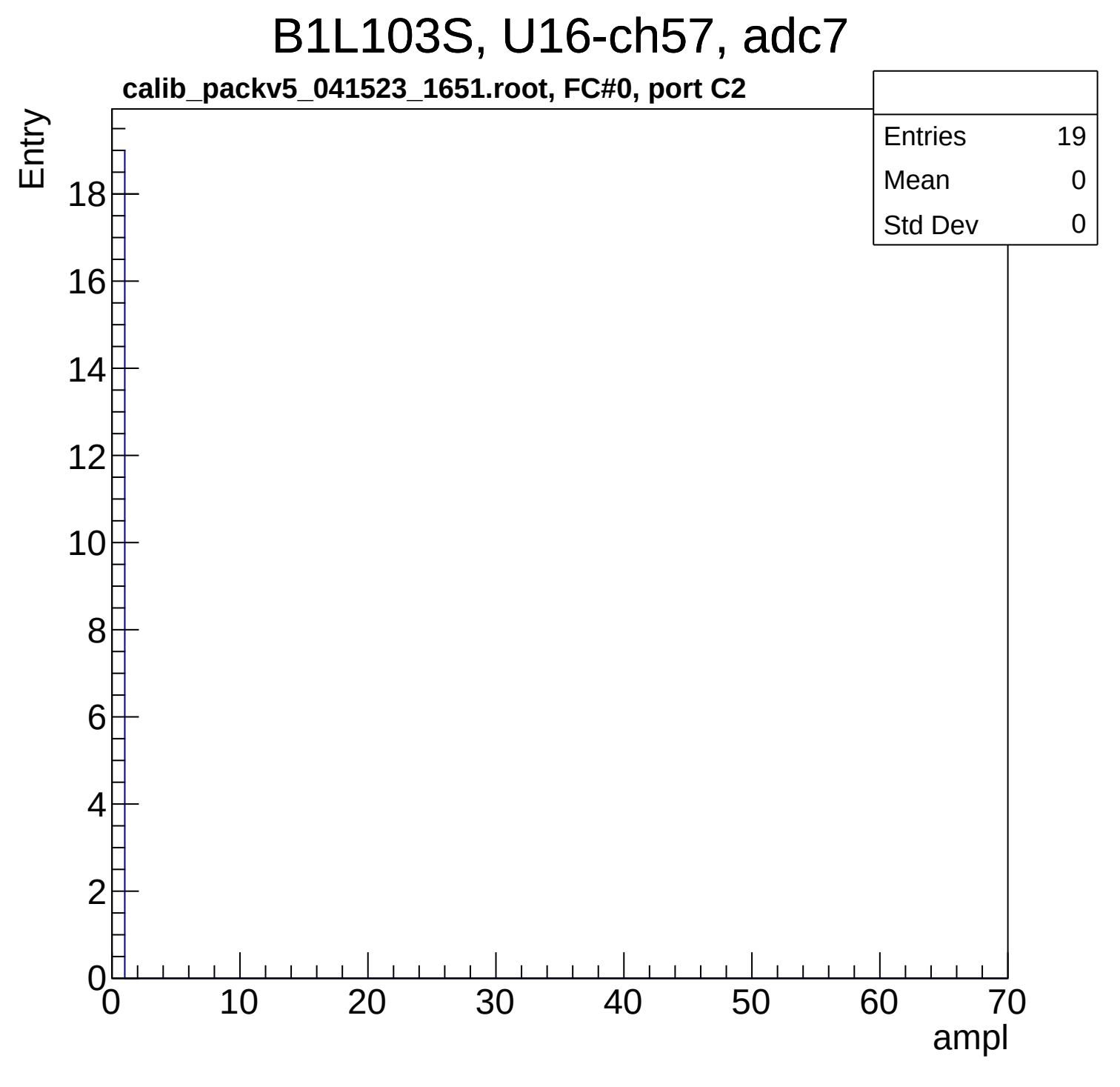
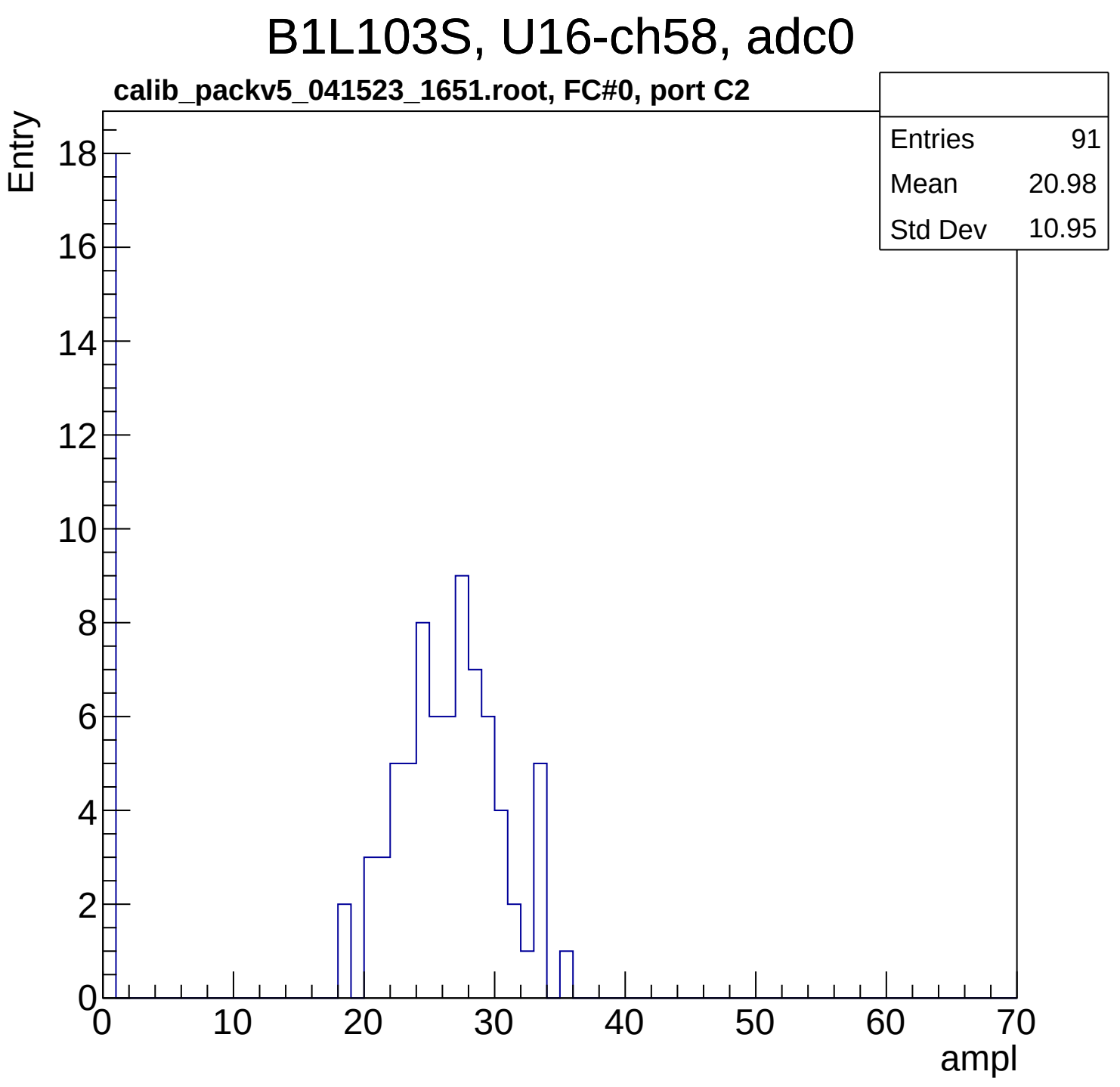
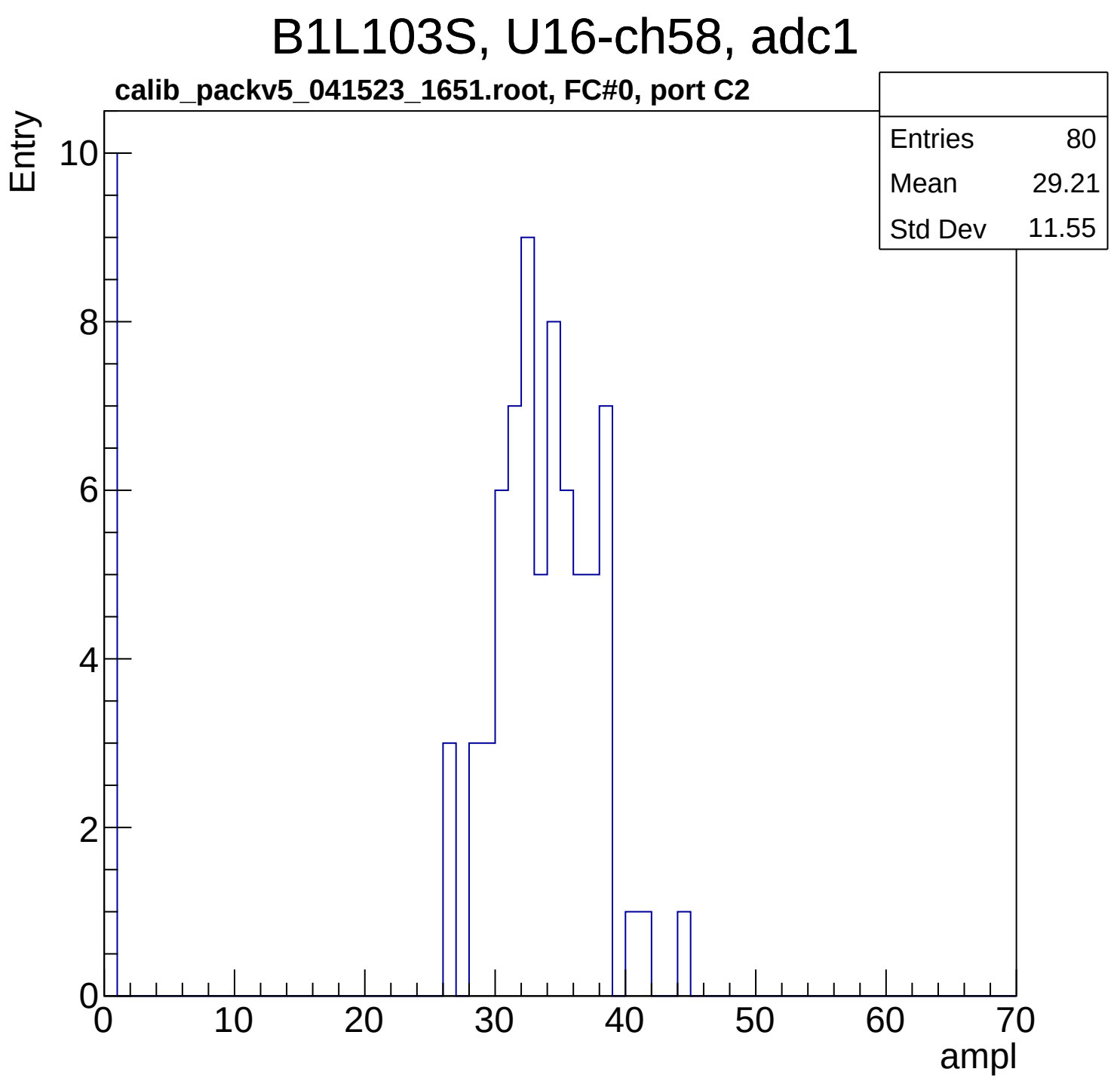
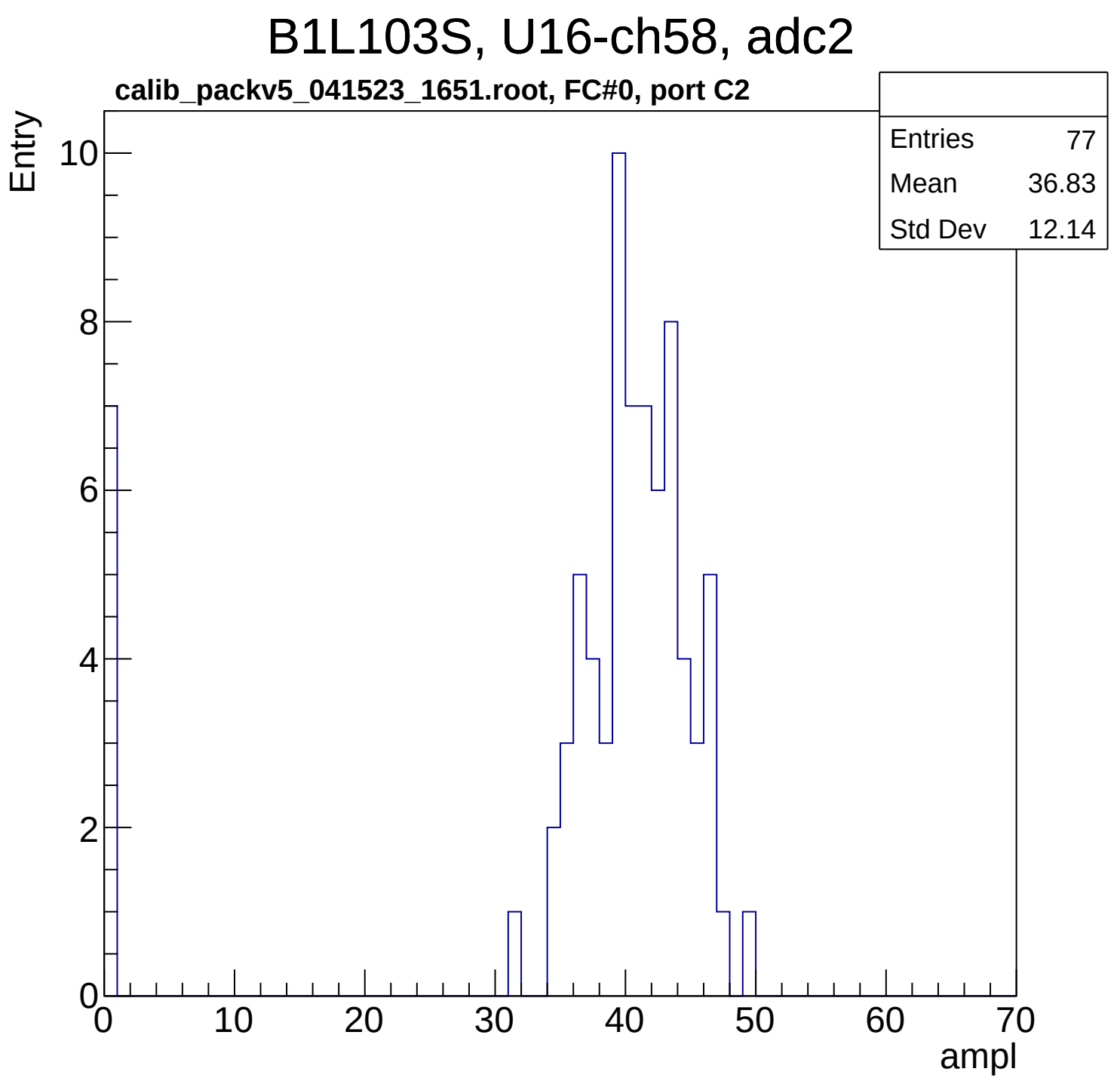
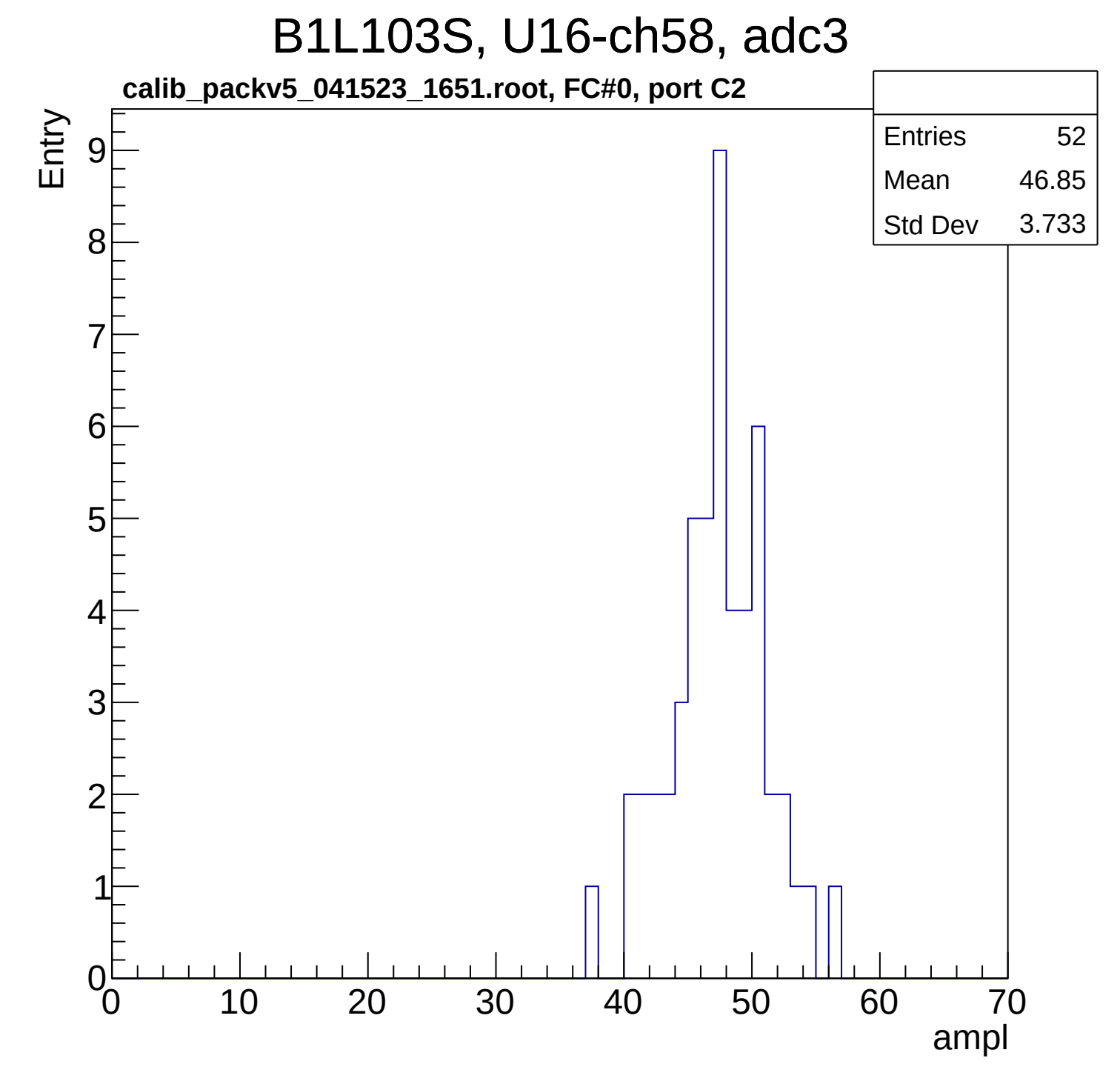
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U16-ch57, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch58, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 20.98
Std Dev 10.95
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch58, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 29.21
Std Dev 11.55
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch58, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 36.83
Std Dev 12.14
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch58, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 46.85
Std Dev 3.733
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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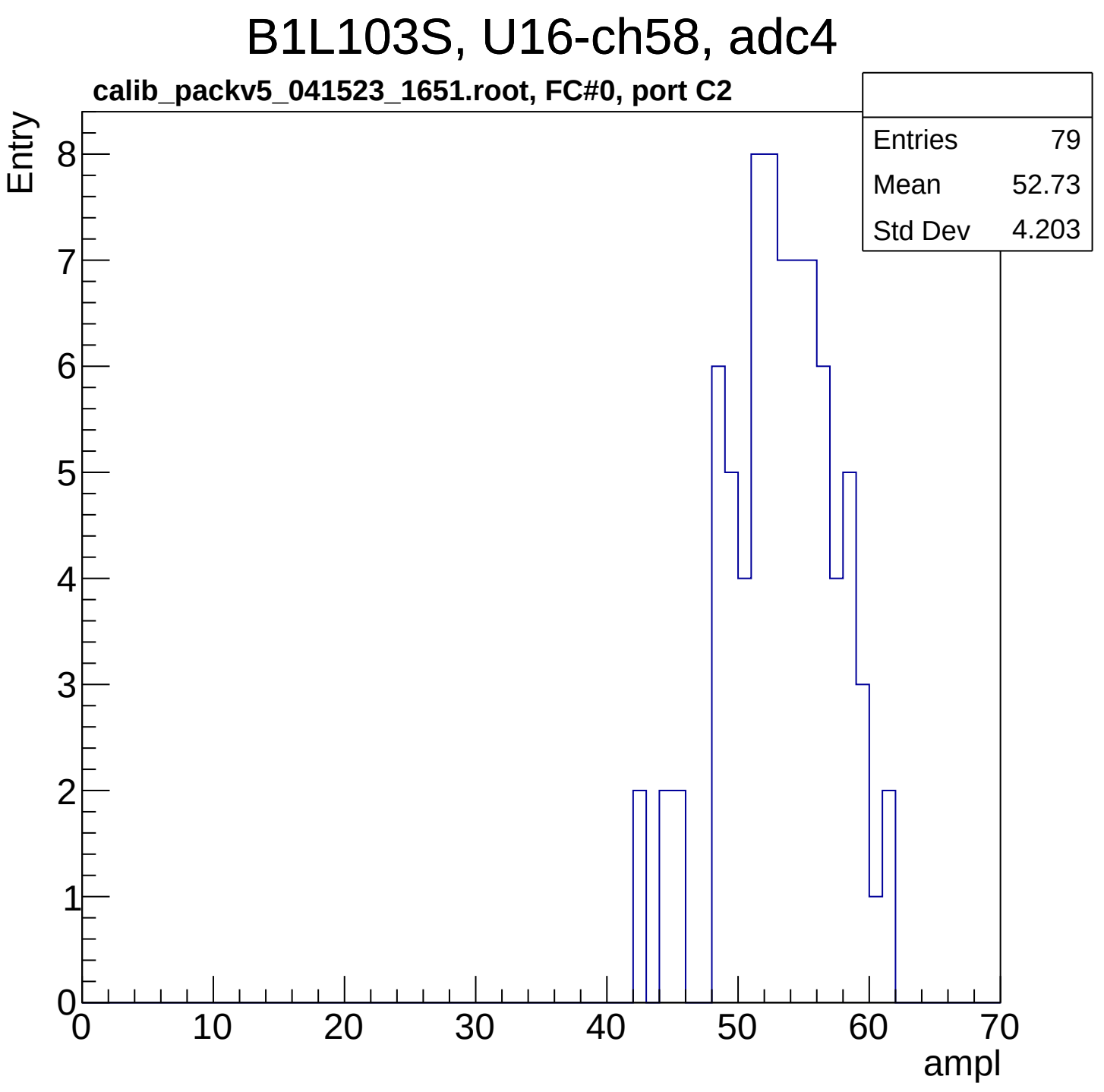
60
70


B1L103S, U16-ch58, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 52.73
Std Dev 4.203
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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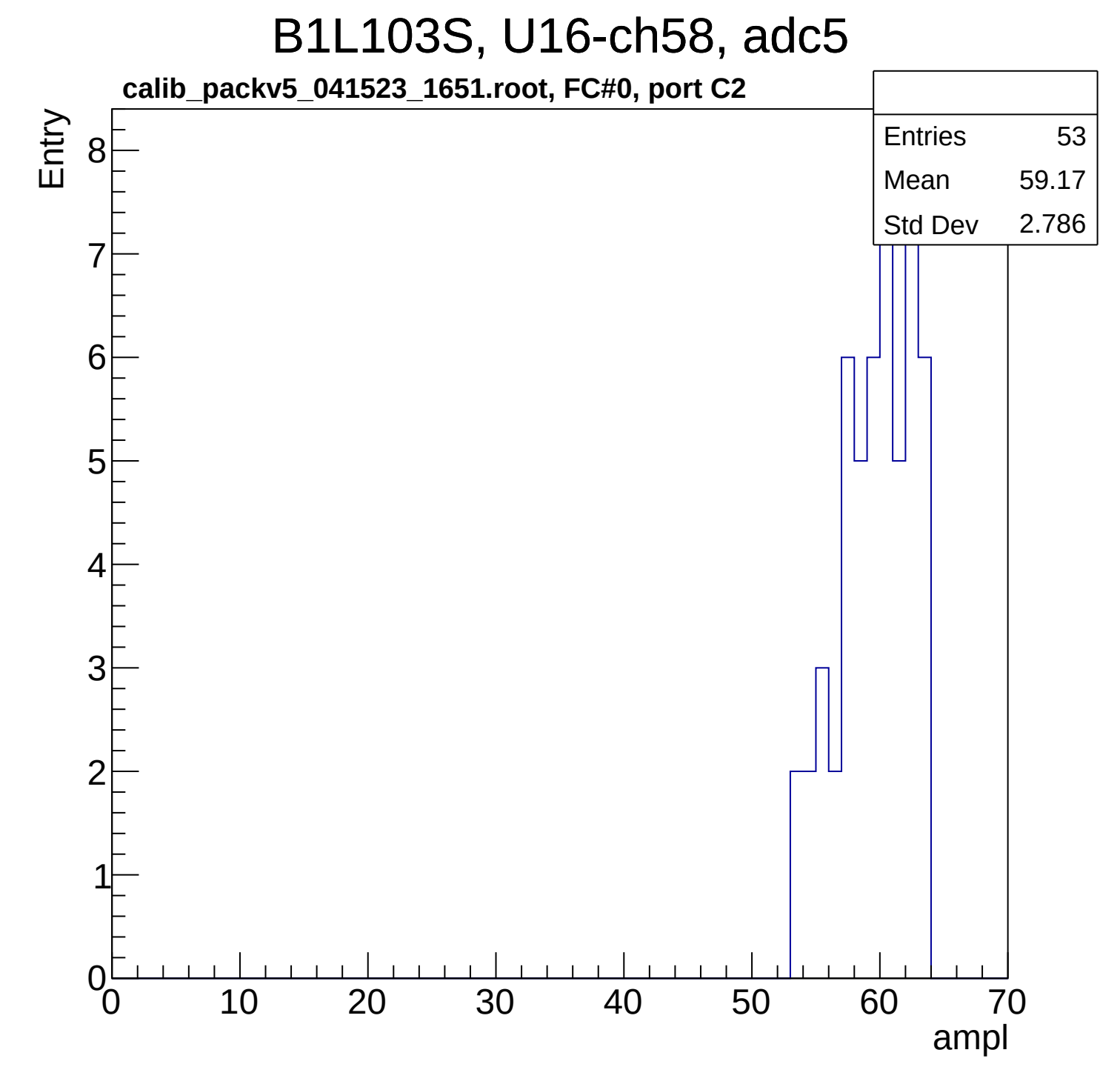
B1L103S, U16-ch58, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 59.17
Std Dev 2.786
Entry
ampl
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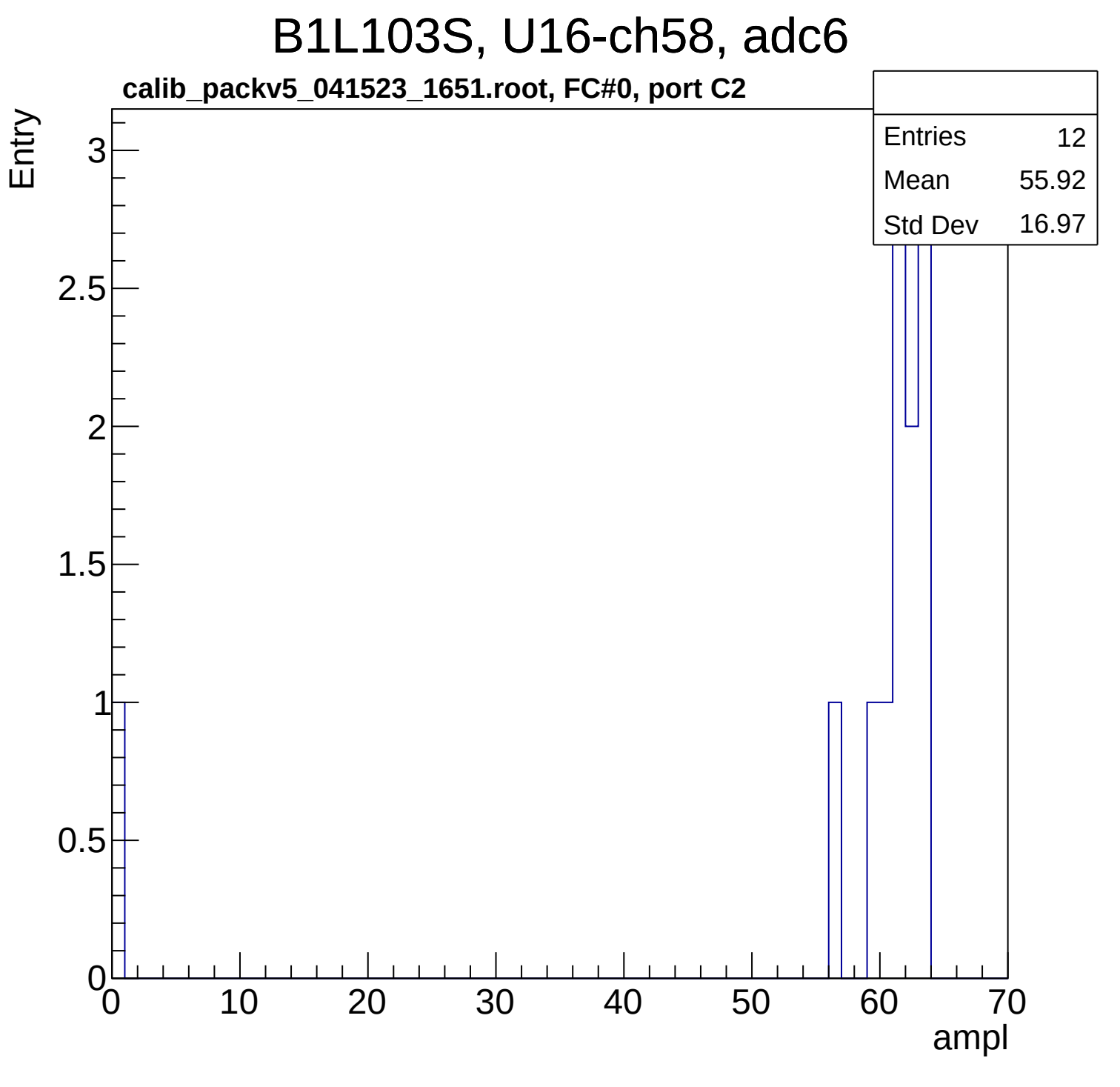
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch58, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 55.92
Std Dev 16.97
Entry
ampl
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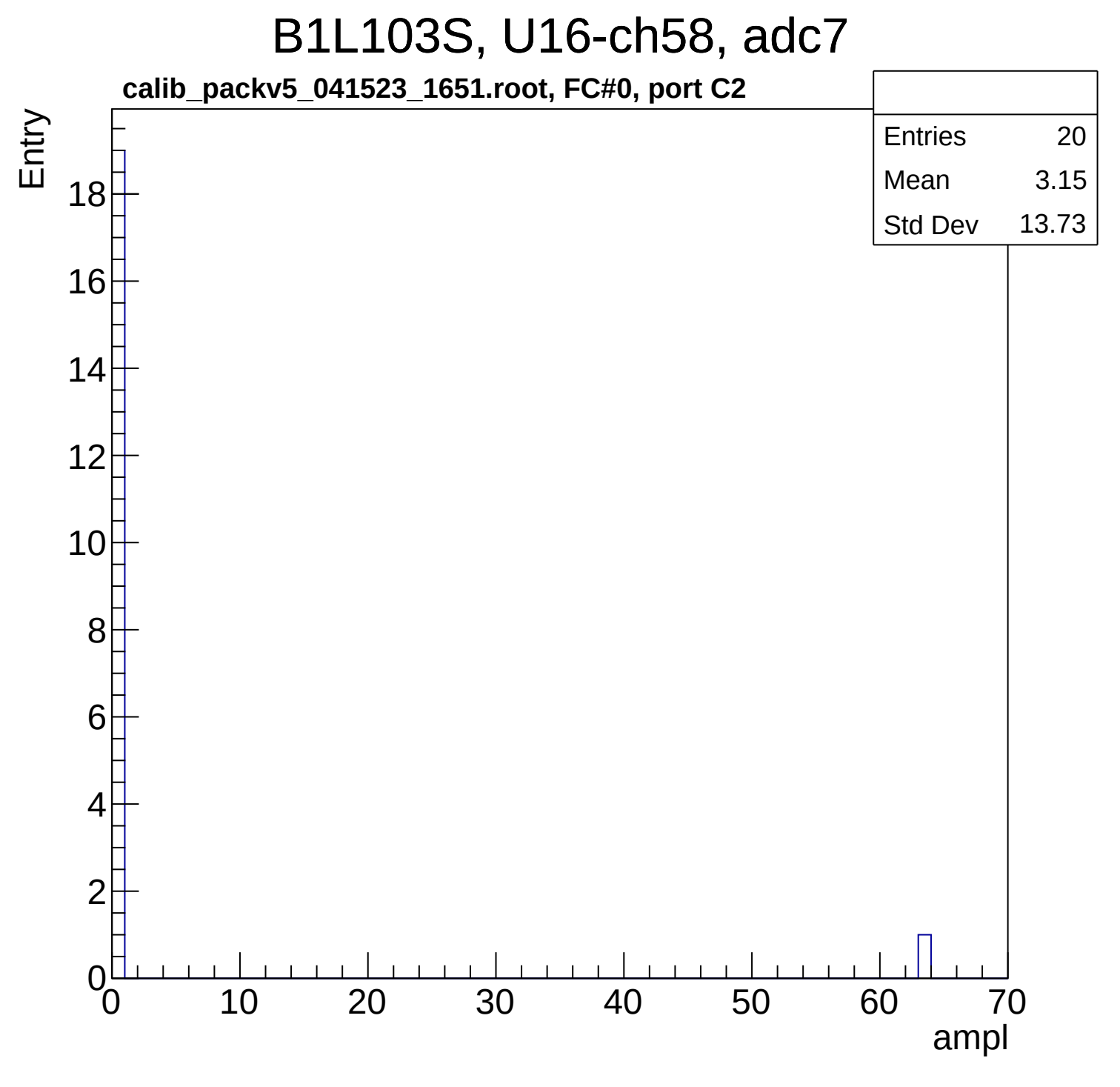
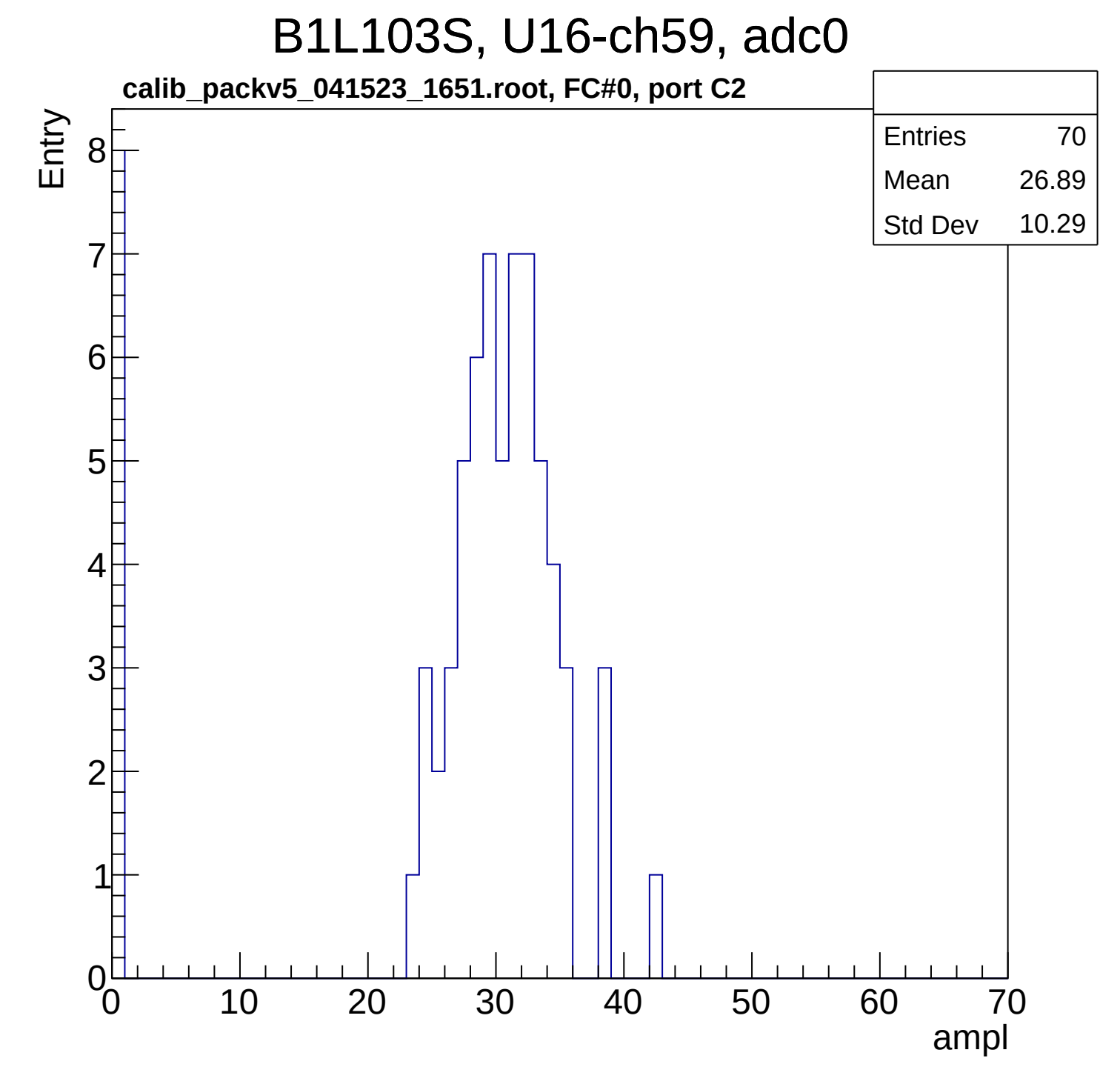
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U16-ch58, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch59, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 26.89
Std Dev 10.29
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
50
60
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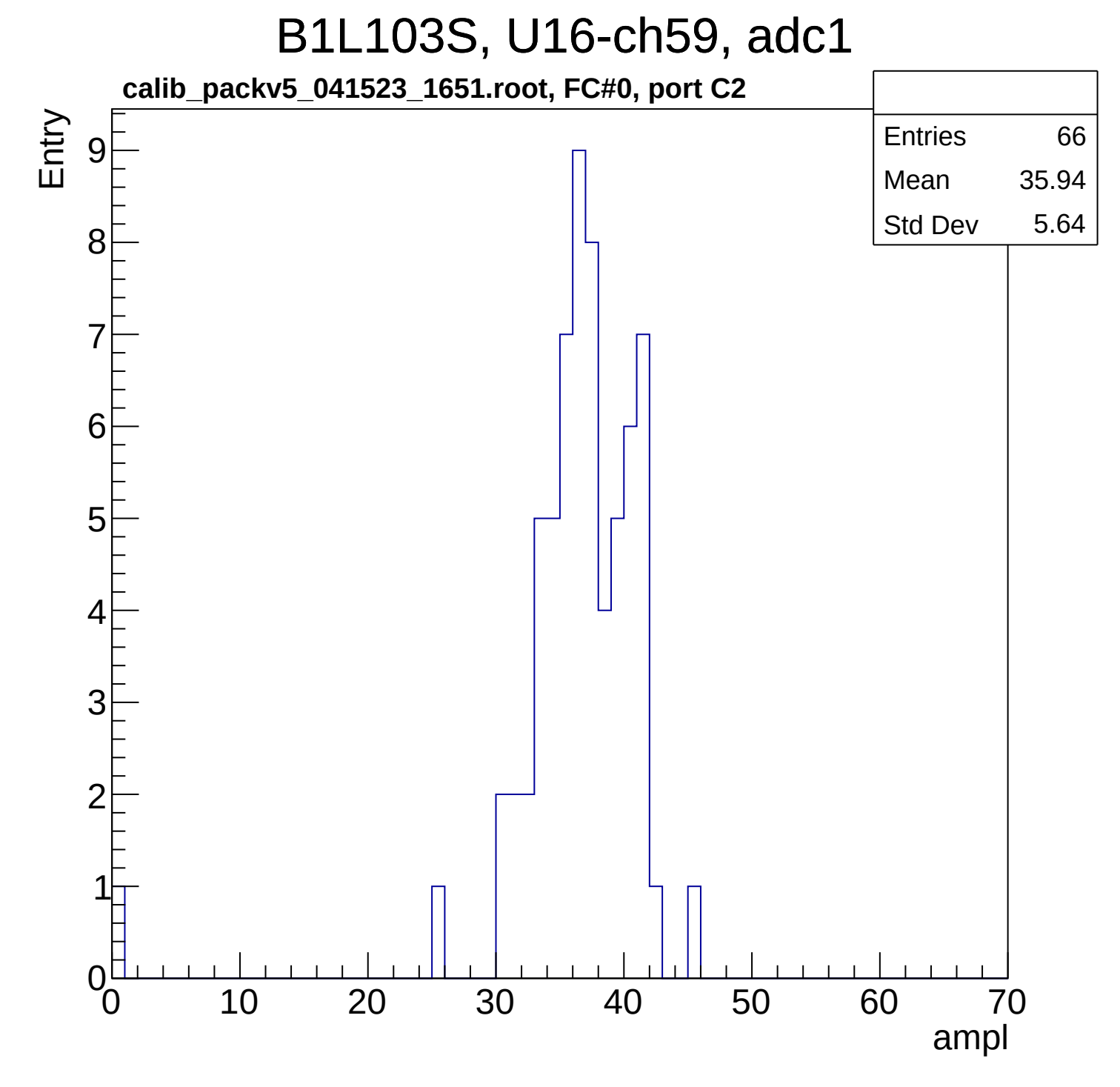
B1L103S, U16-ch59, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 35.94
Std Dev 5.64
Entry
ampl
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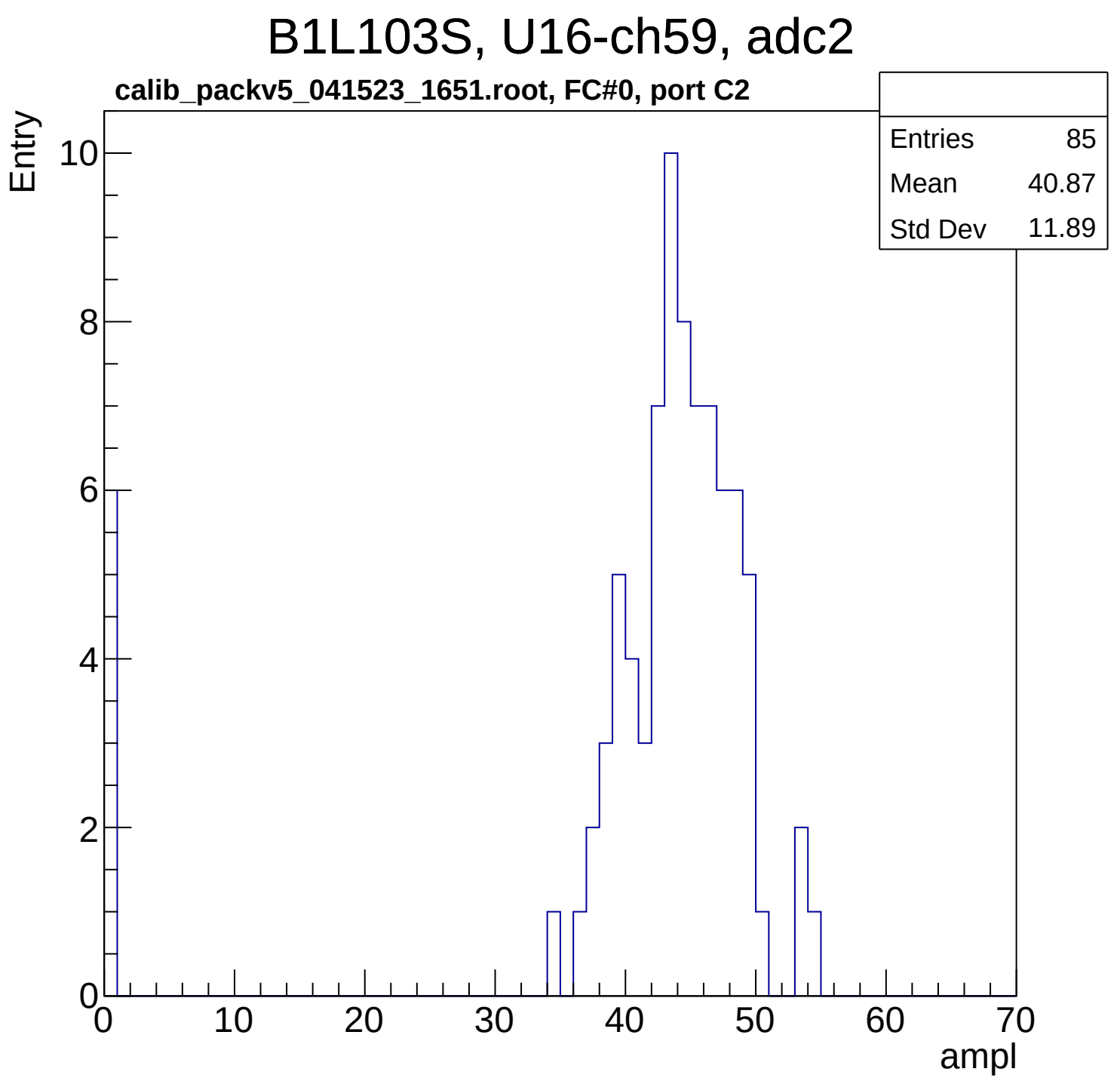
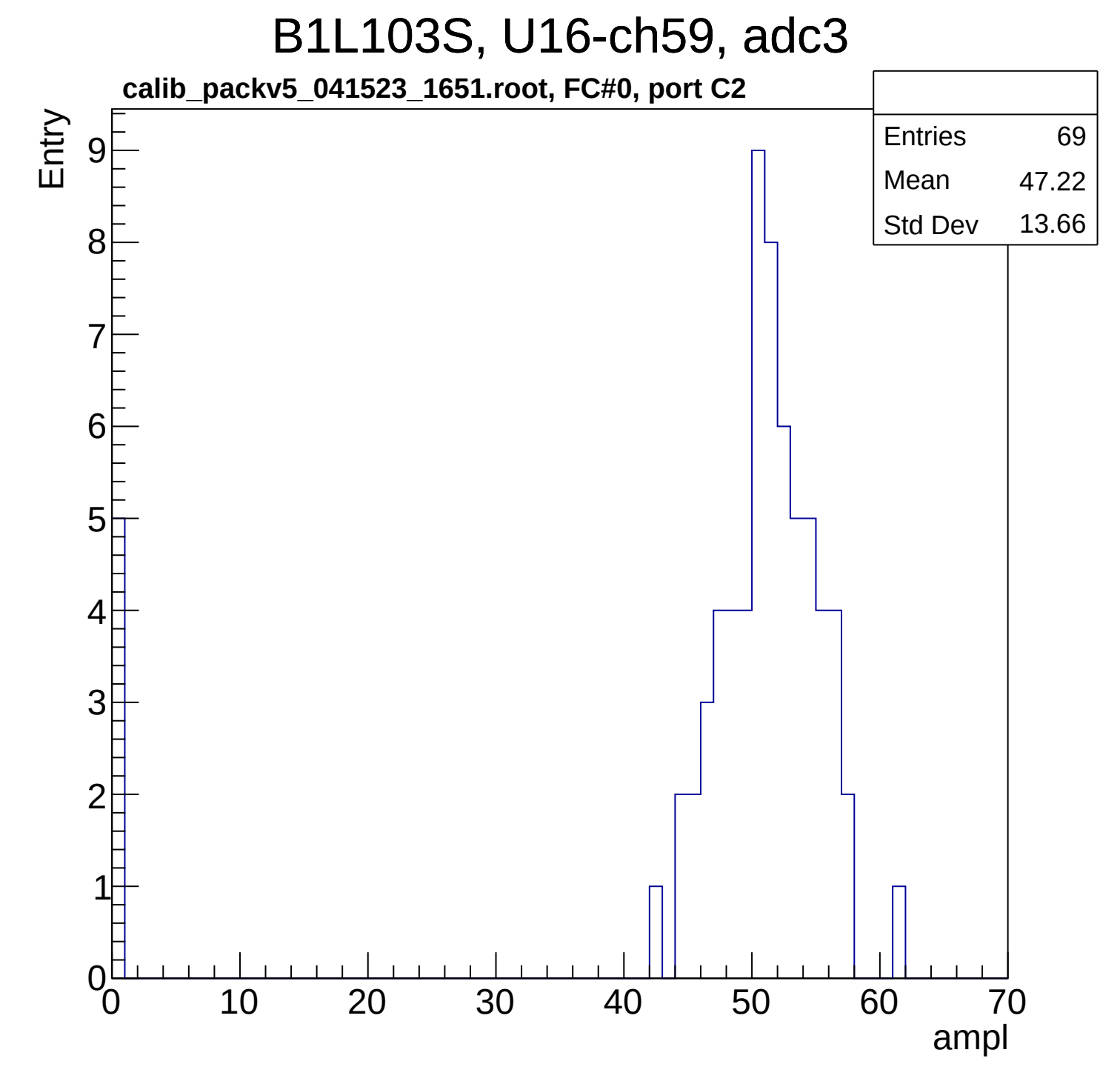
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch59, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 40.87
Std Dev 11.89
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch59, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 47.22
Std Dev 13.66
Entry
ampl
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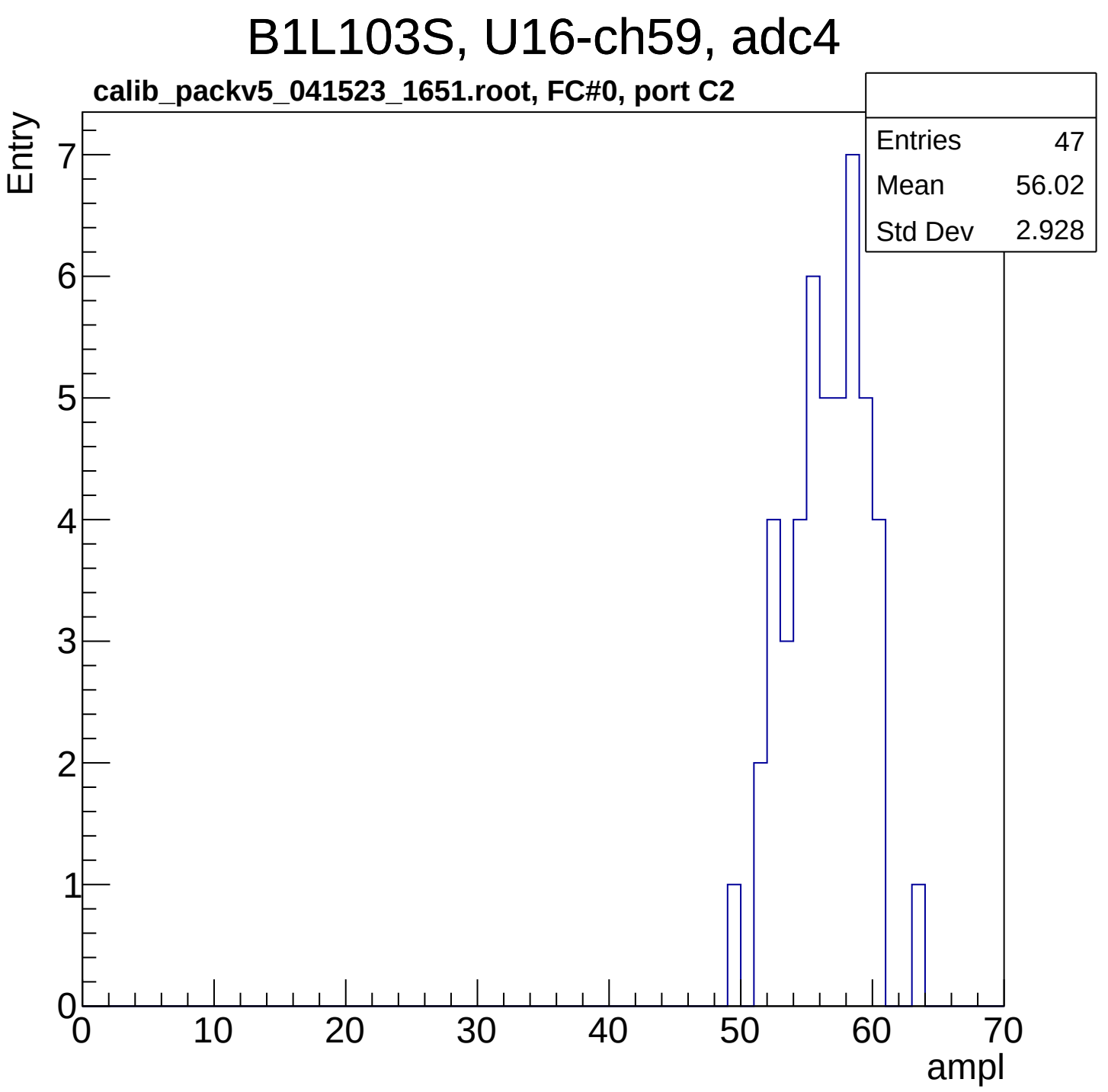
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch59, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 56.02
Std Dev 2.928
Entry
ampl
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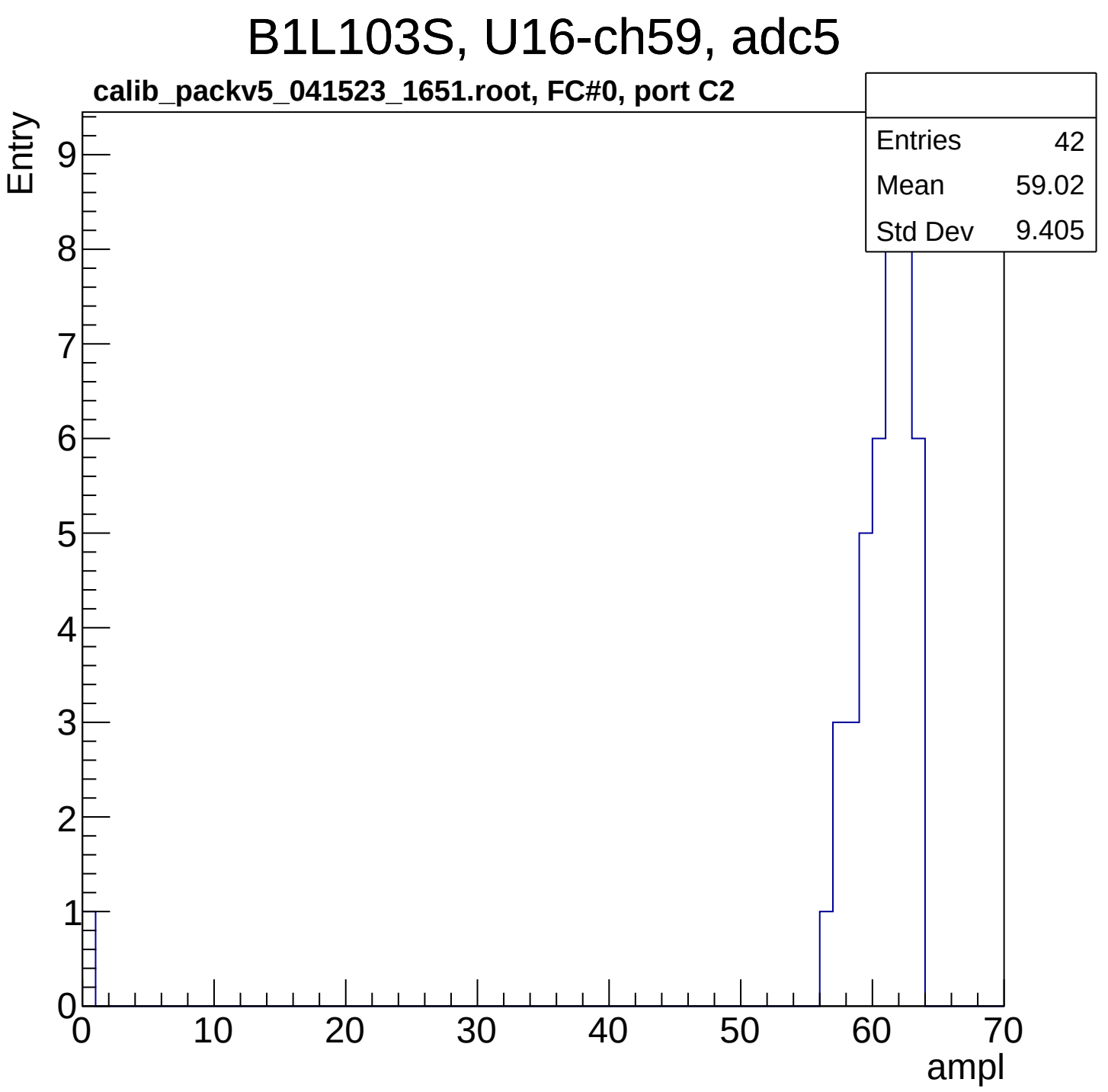
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch59, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 59.02
Std Dev 9.405
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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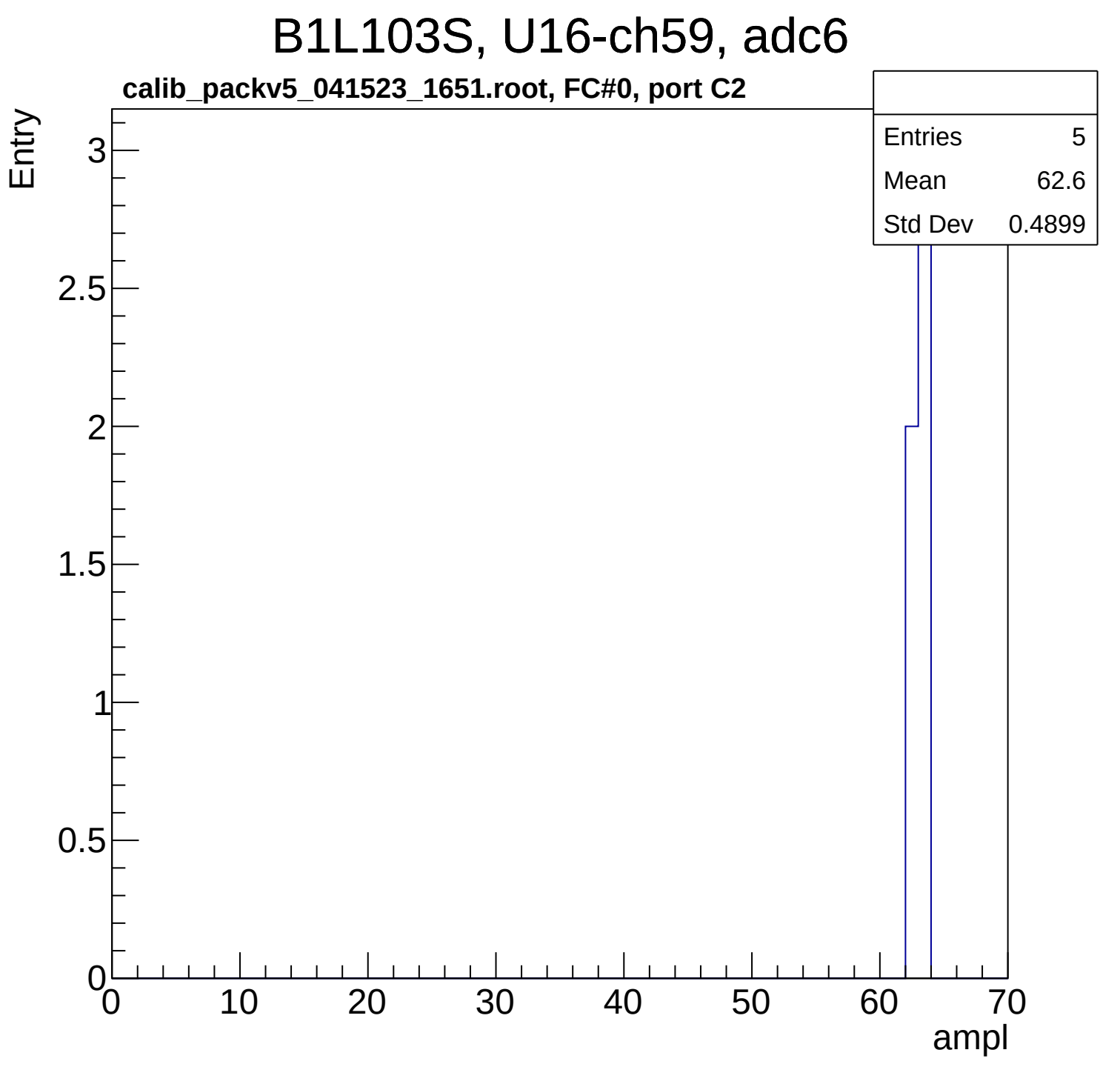
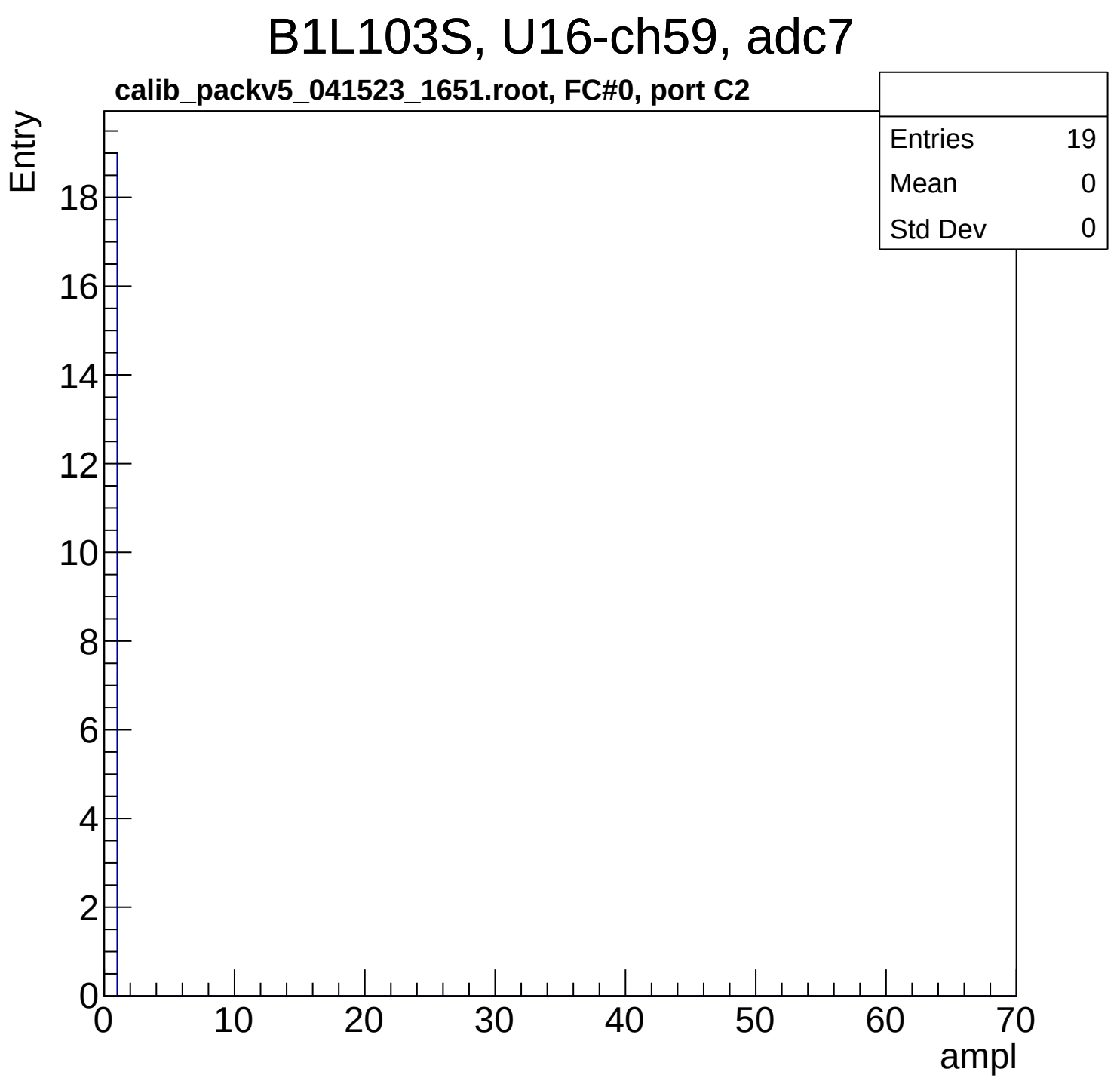
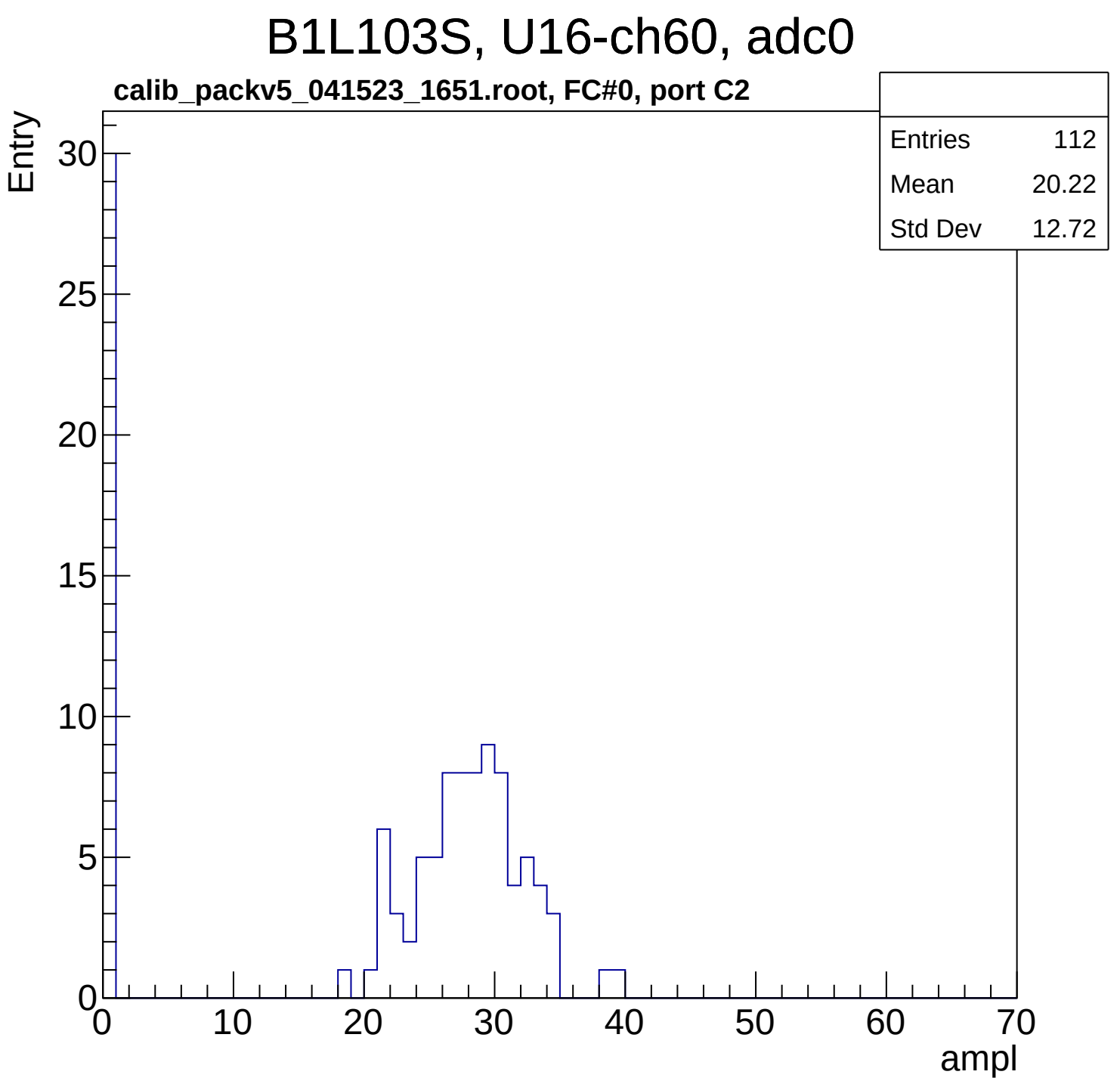
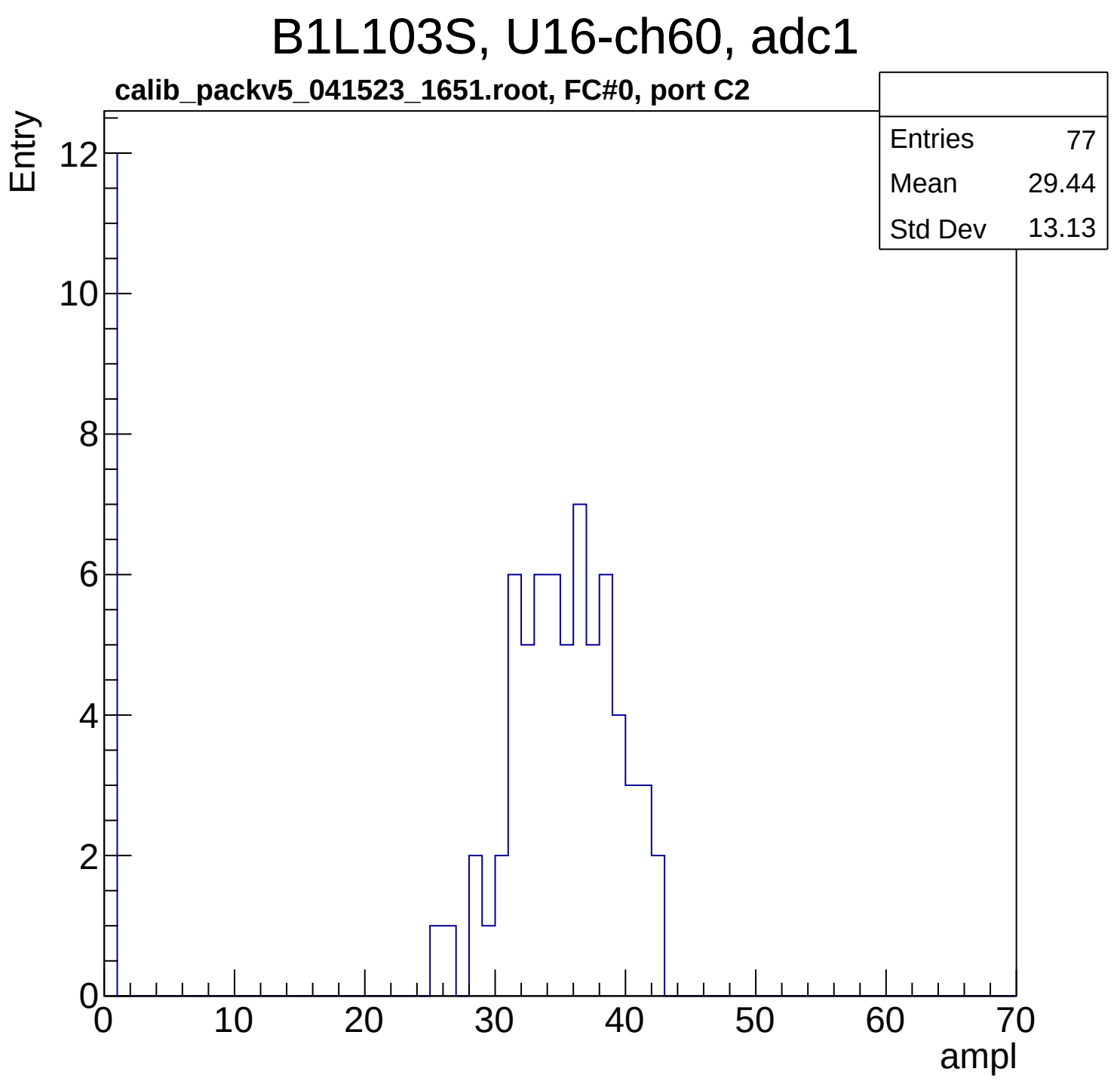
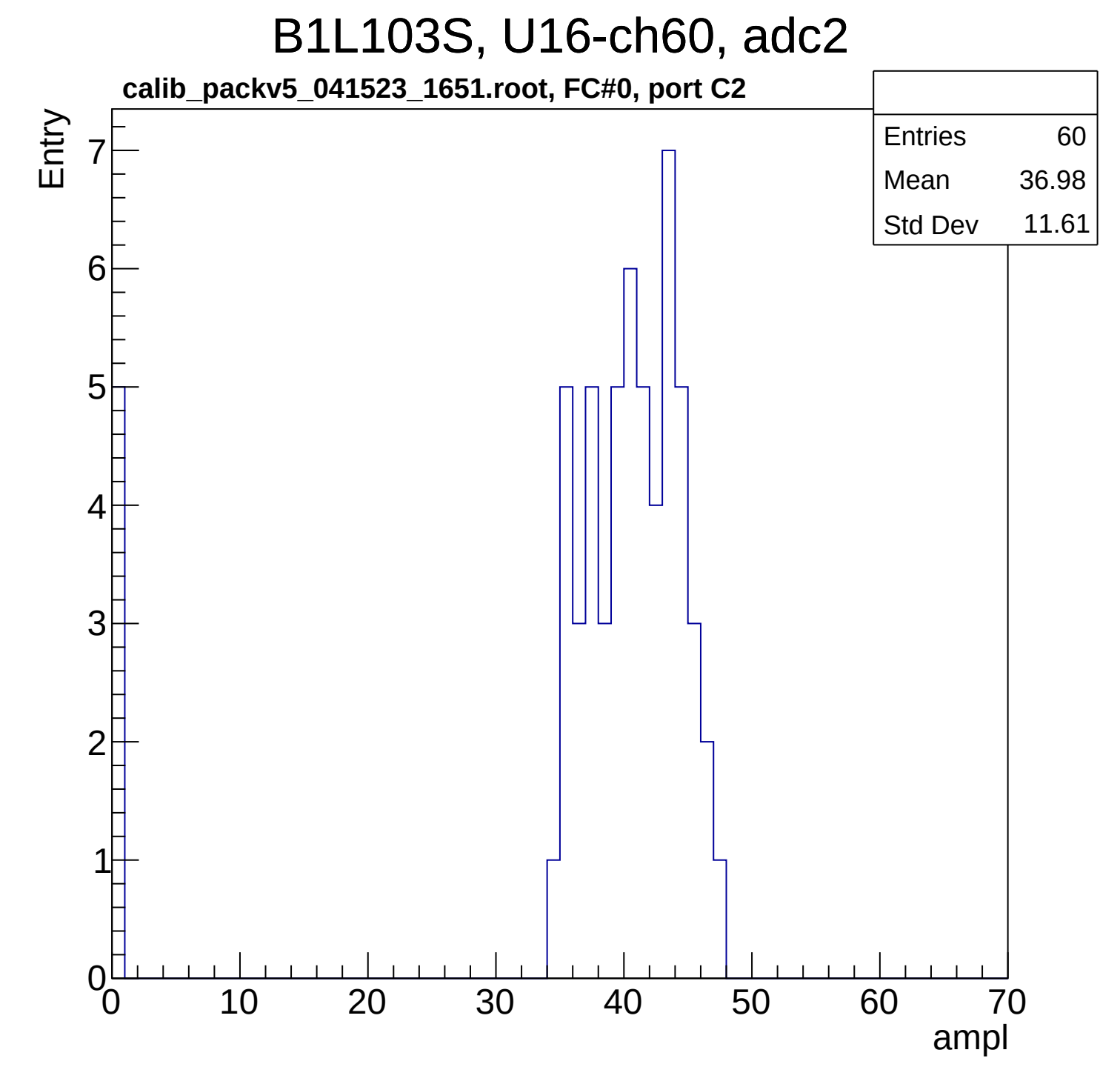
40
50
60
70

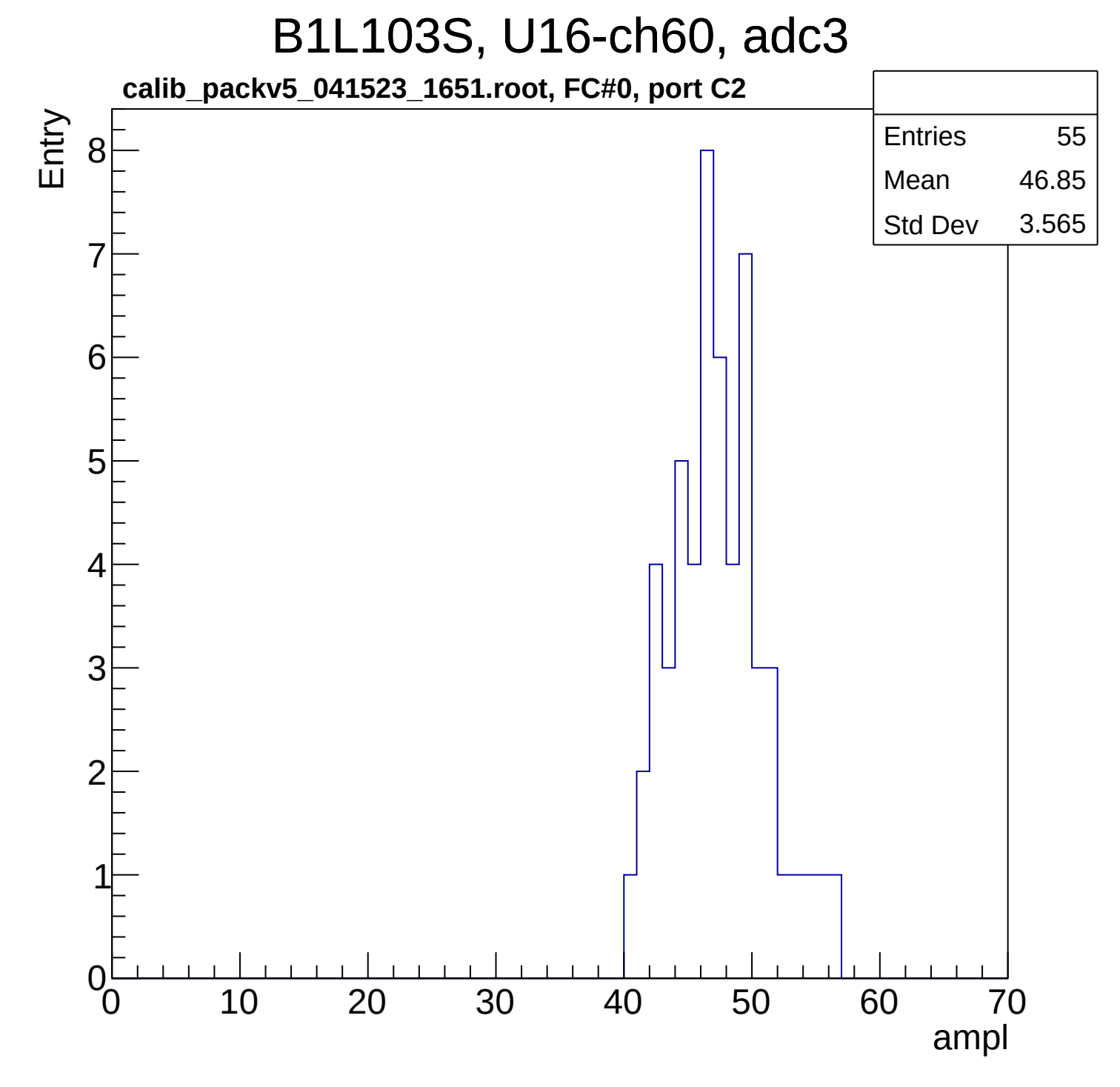

B1L103S, U16-ch59, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.6
Std Dev 0.4899
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U16-ch59, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch60, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 112
Mean 20.22
Std Dev 12.72
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch60, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 29.44
Std Dev 13.13
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch60, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 36.98
Std Dev 11.61
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch60, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 46.85
Std Dev 3.565
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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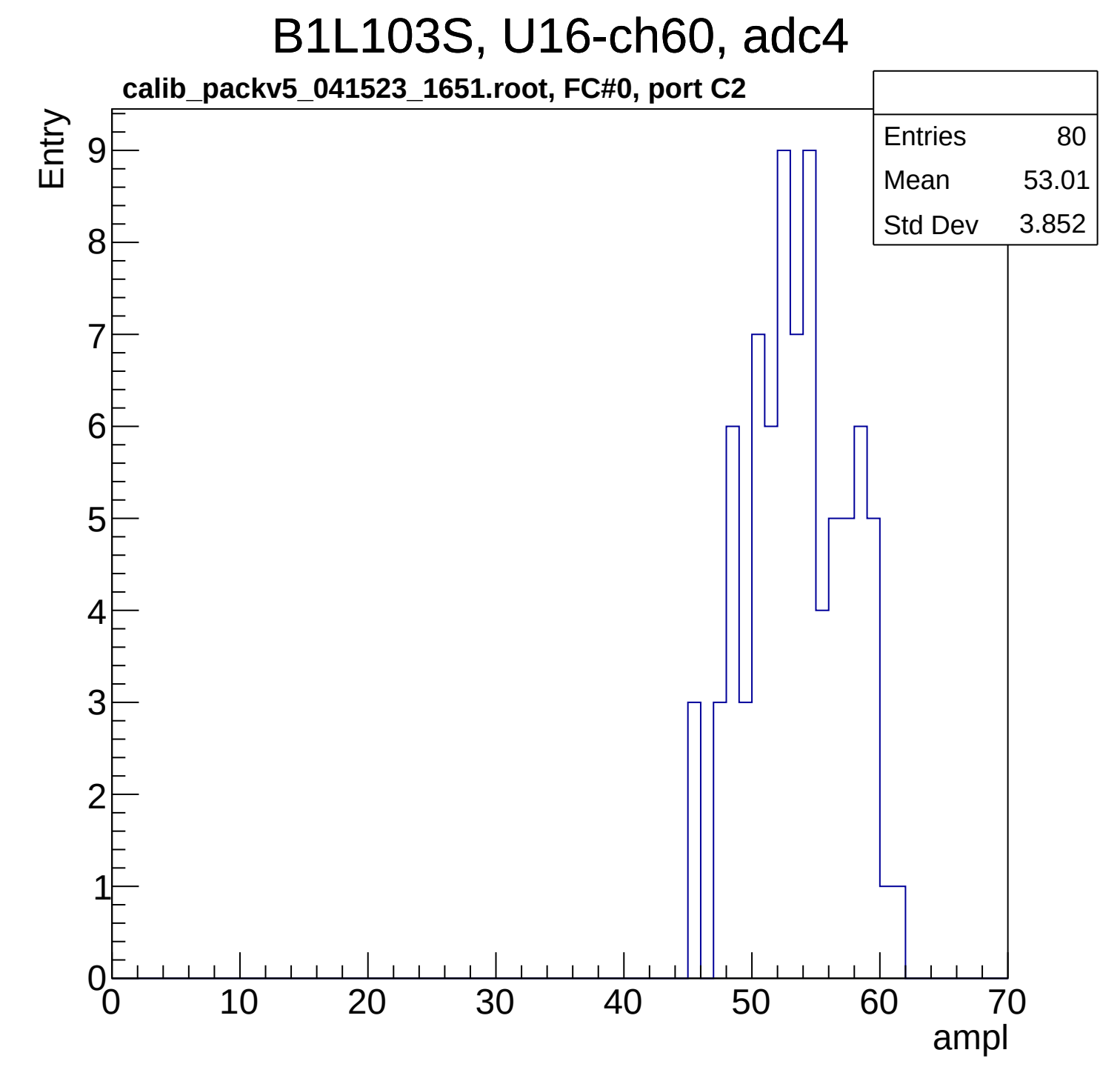
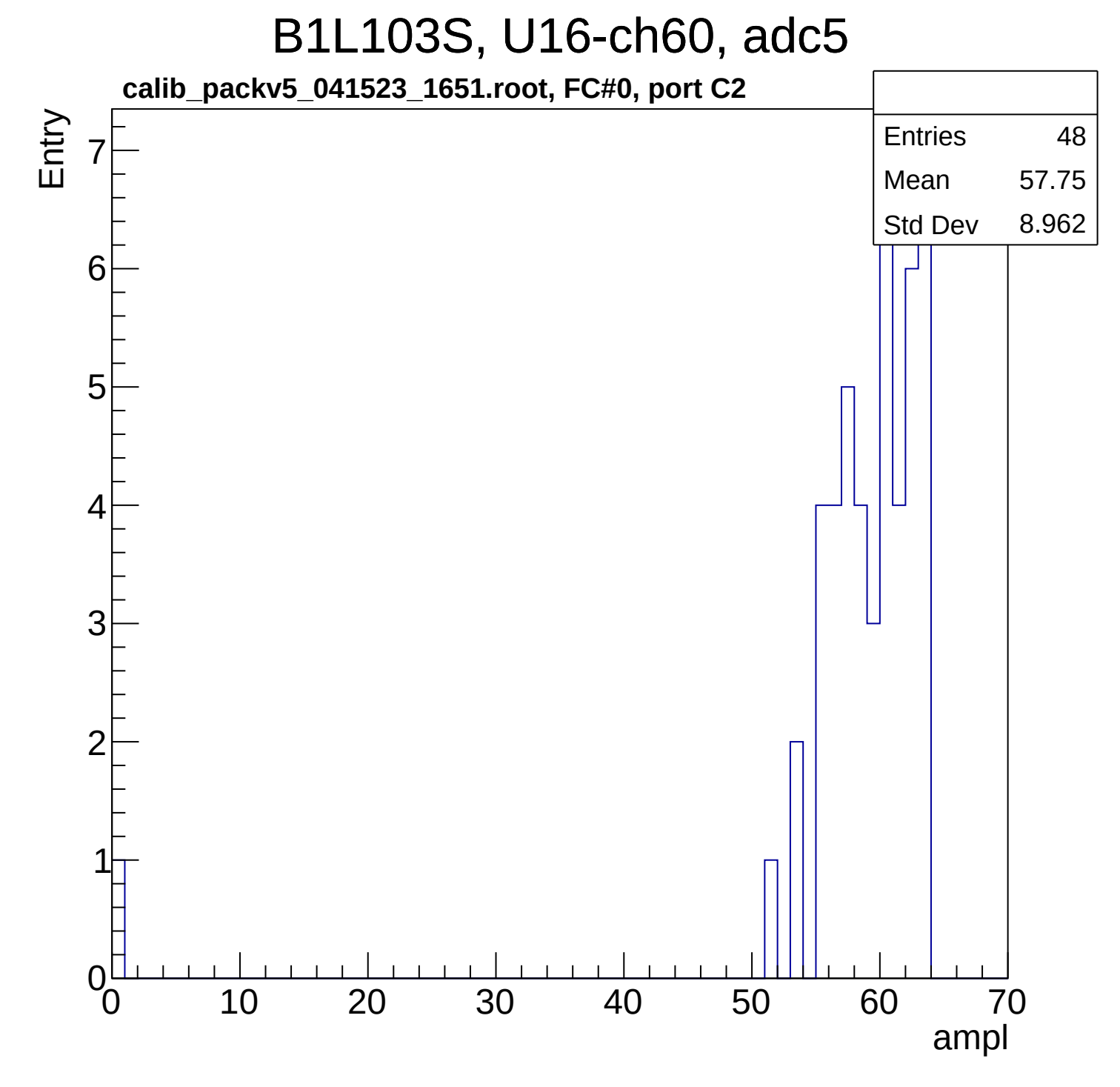
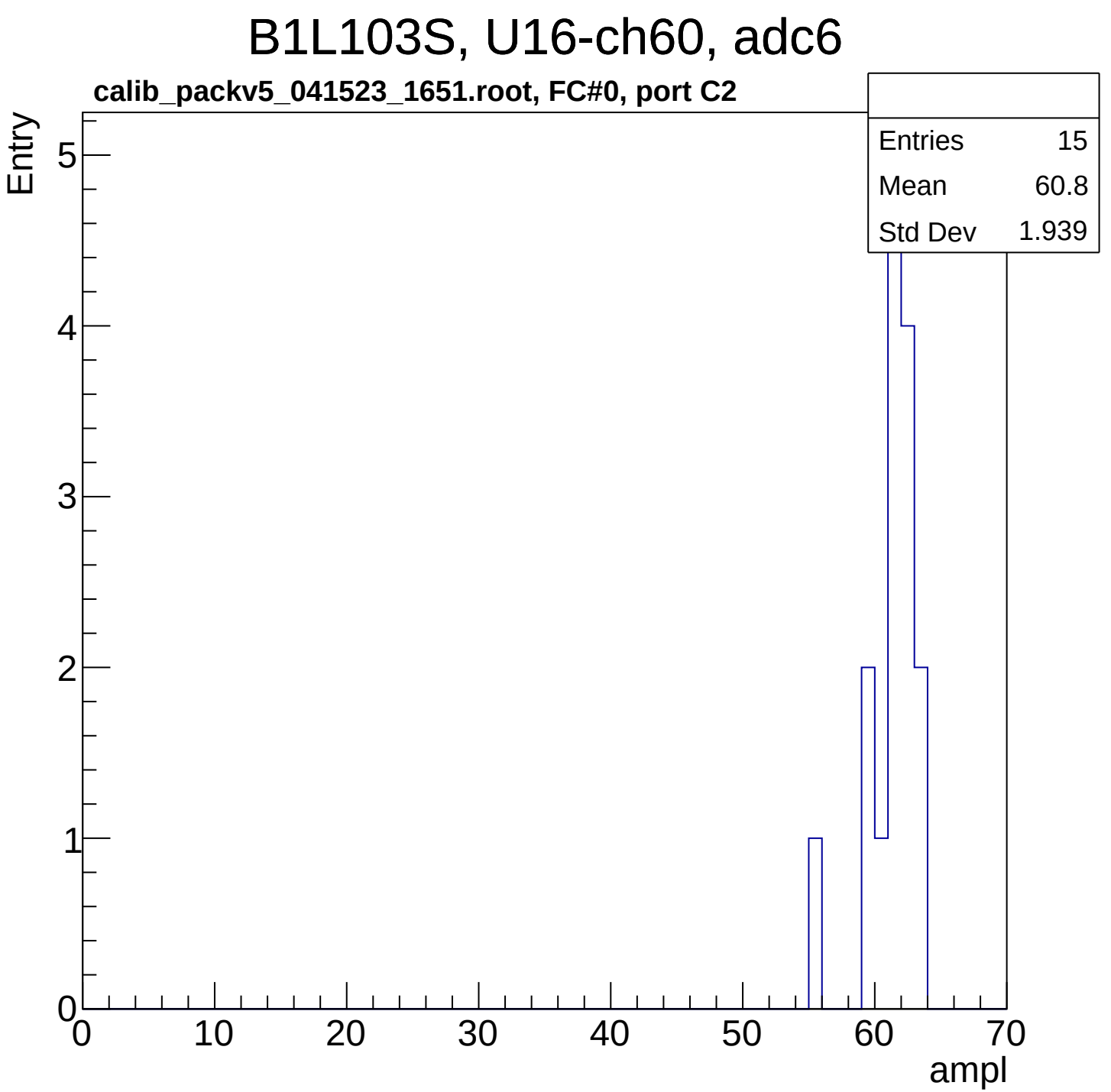
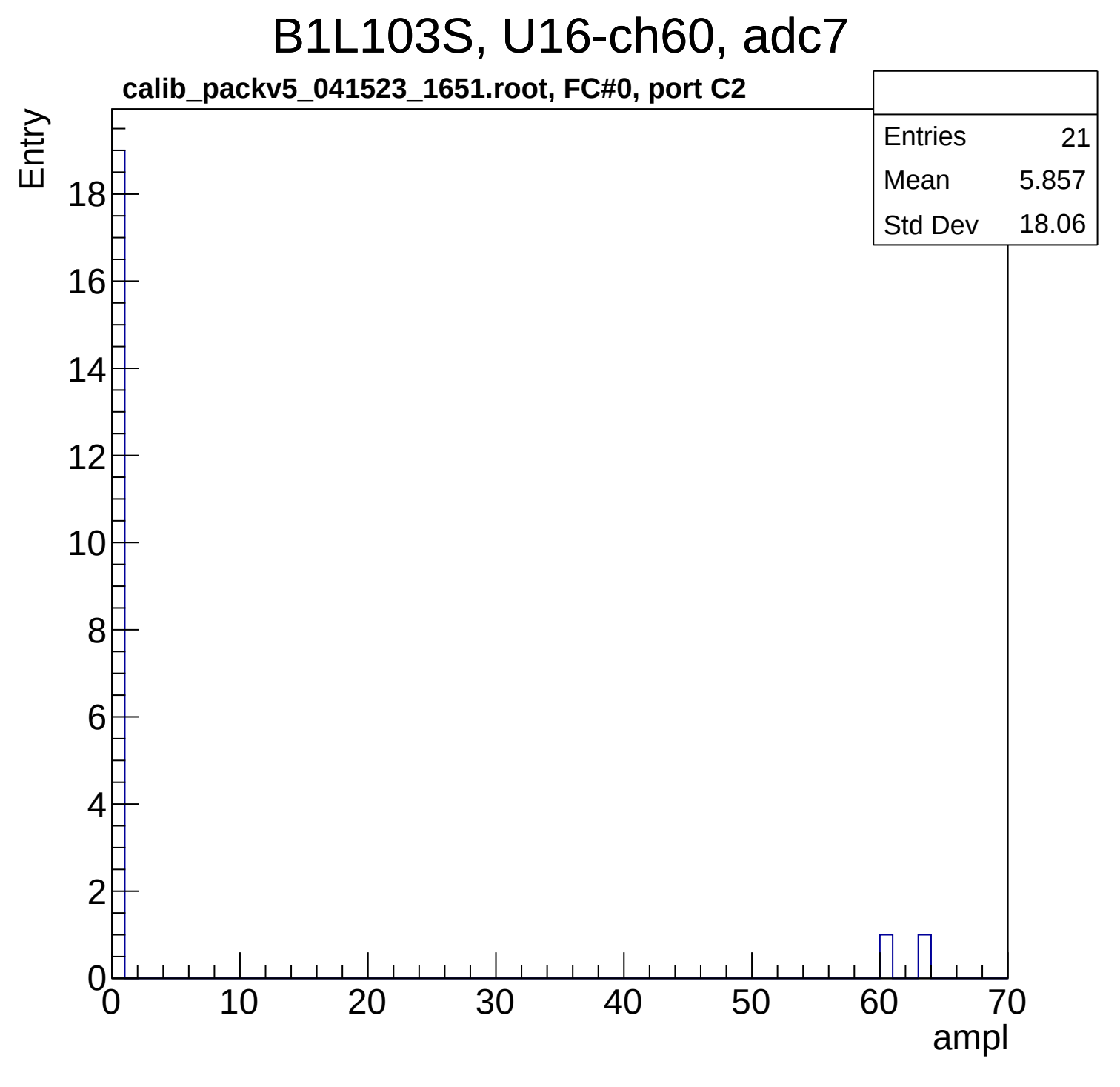

B1L103S, U16-ch60, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 53.01
Std Dev 3.852
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch60, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 57.75
Std Dev 8.962
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch60, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 60.8
Std Dev 1.939
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U16-ch60, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.857
Std Dev 18.06
Entry
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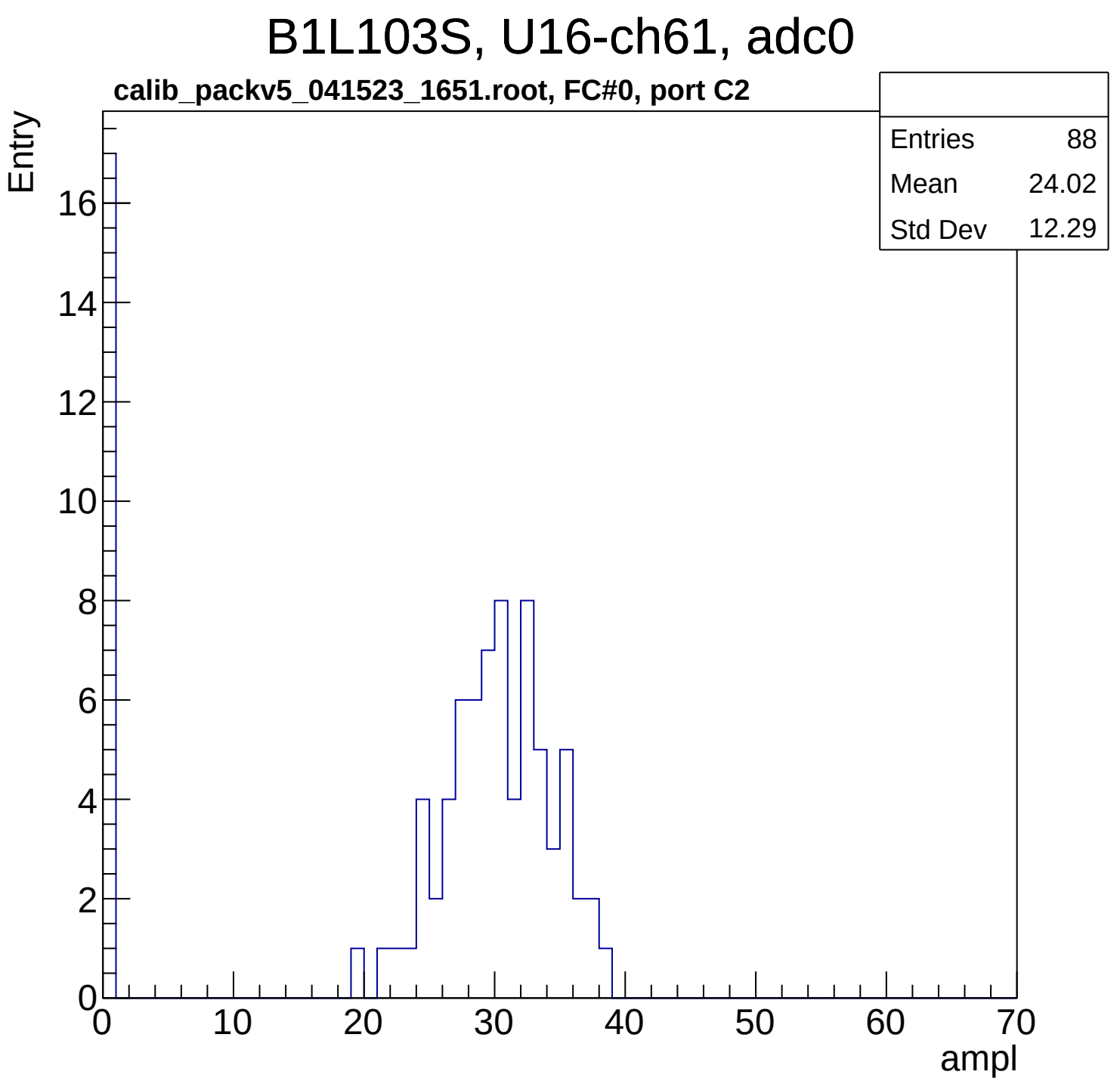
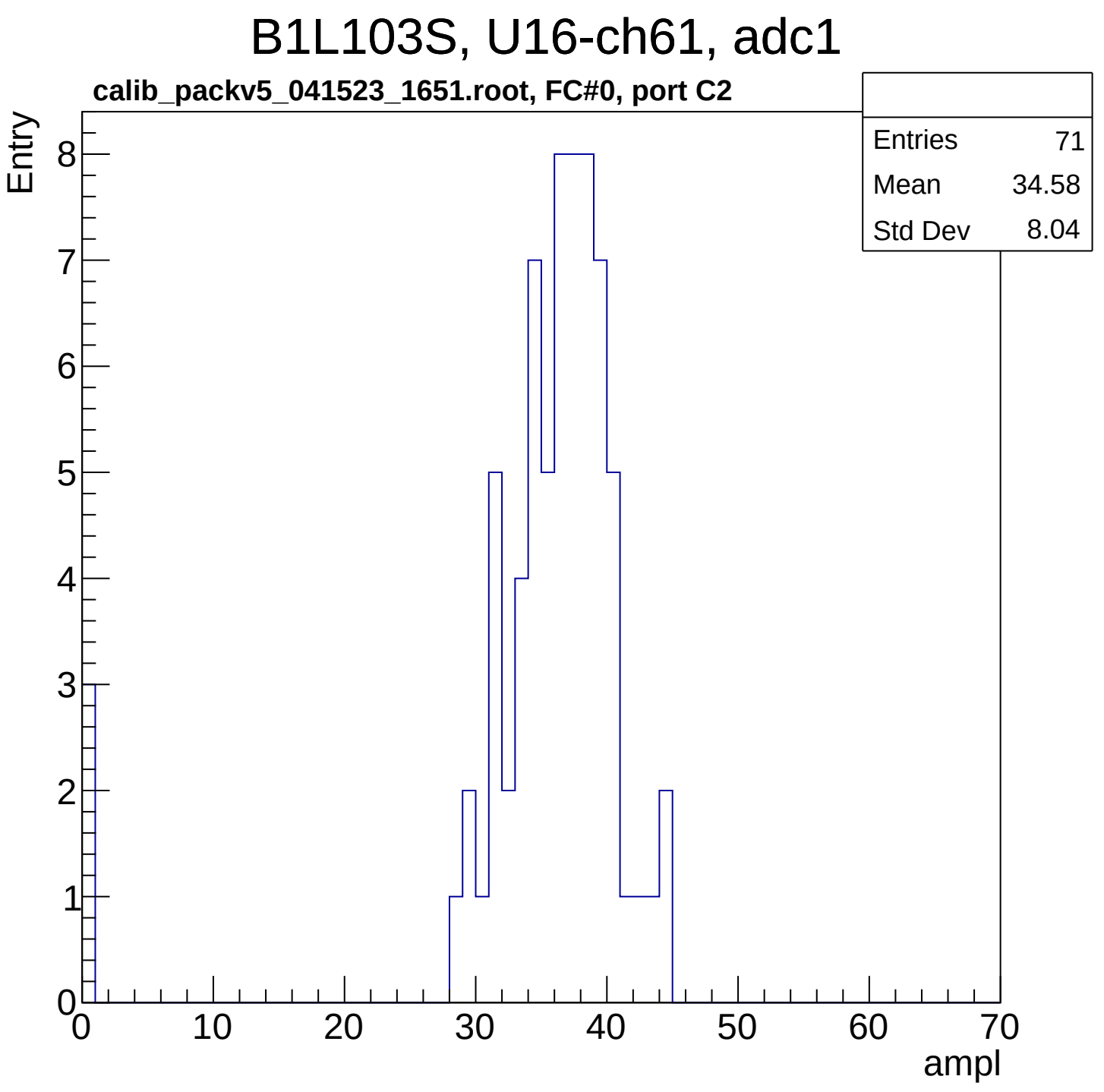
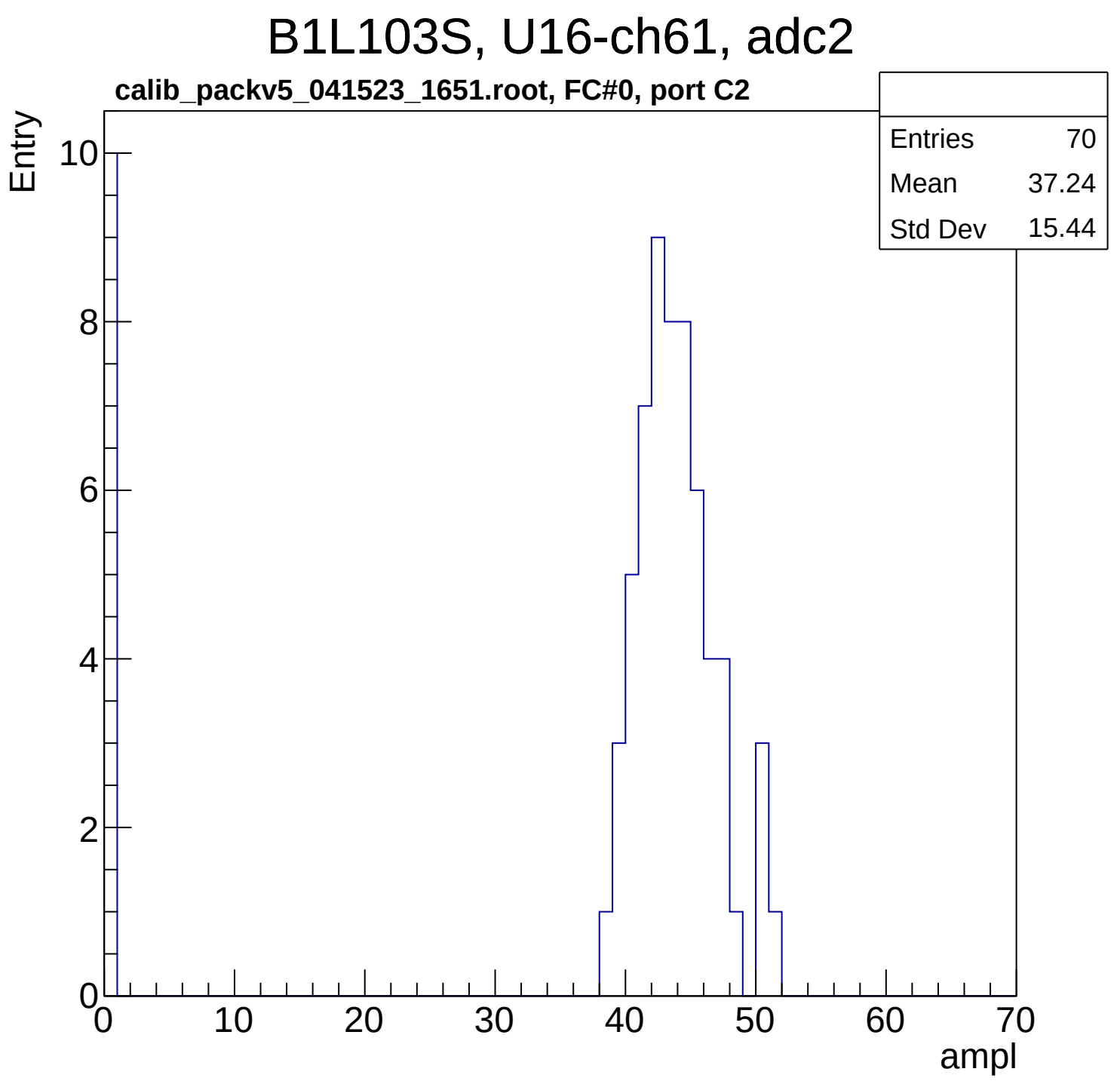
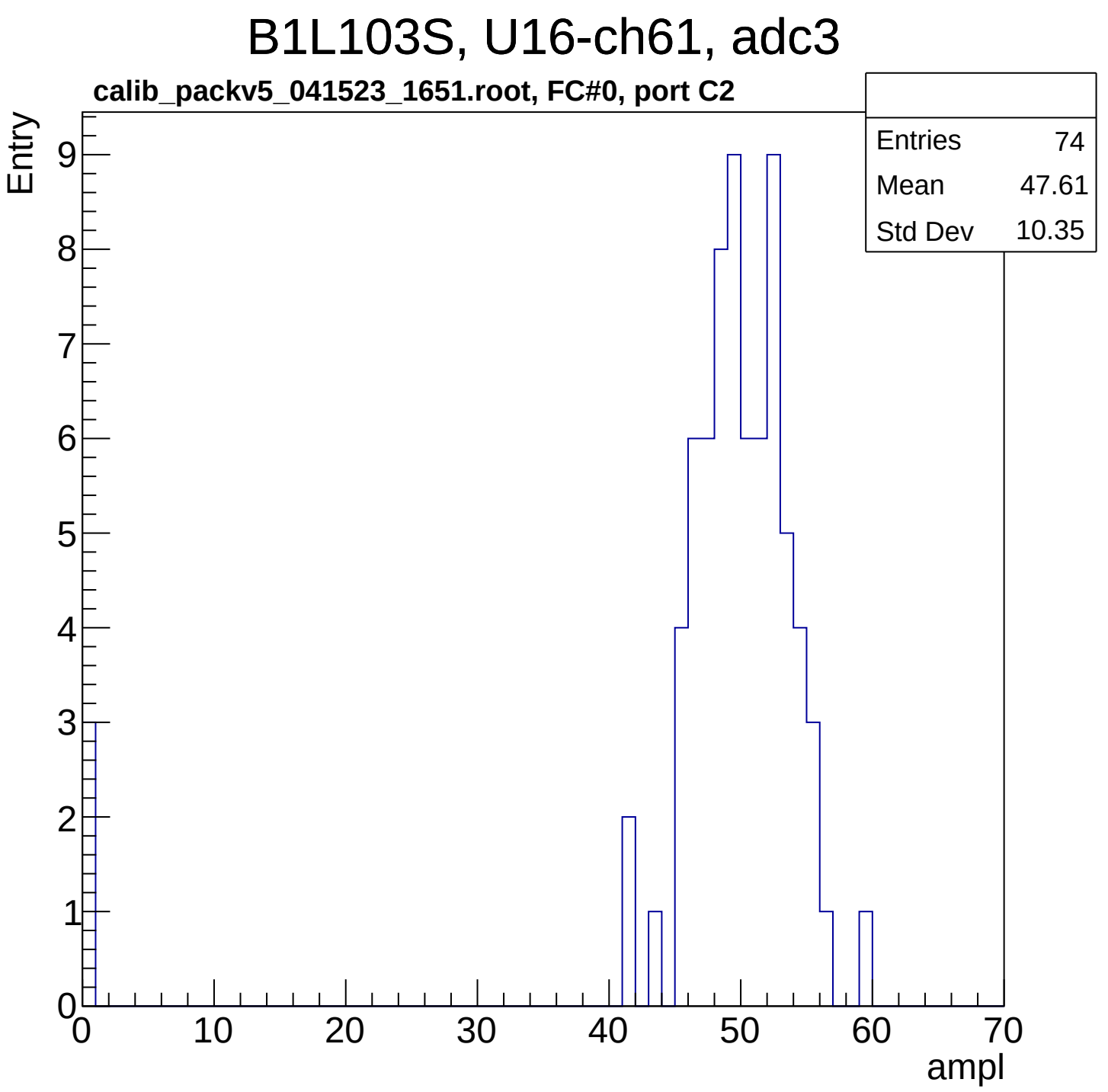
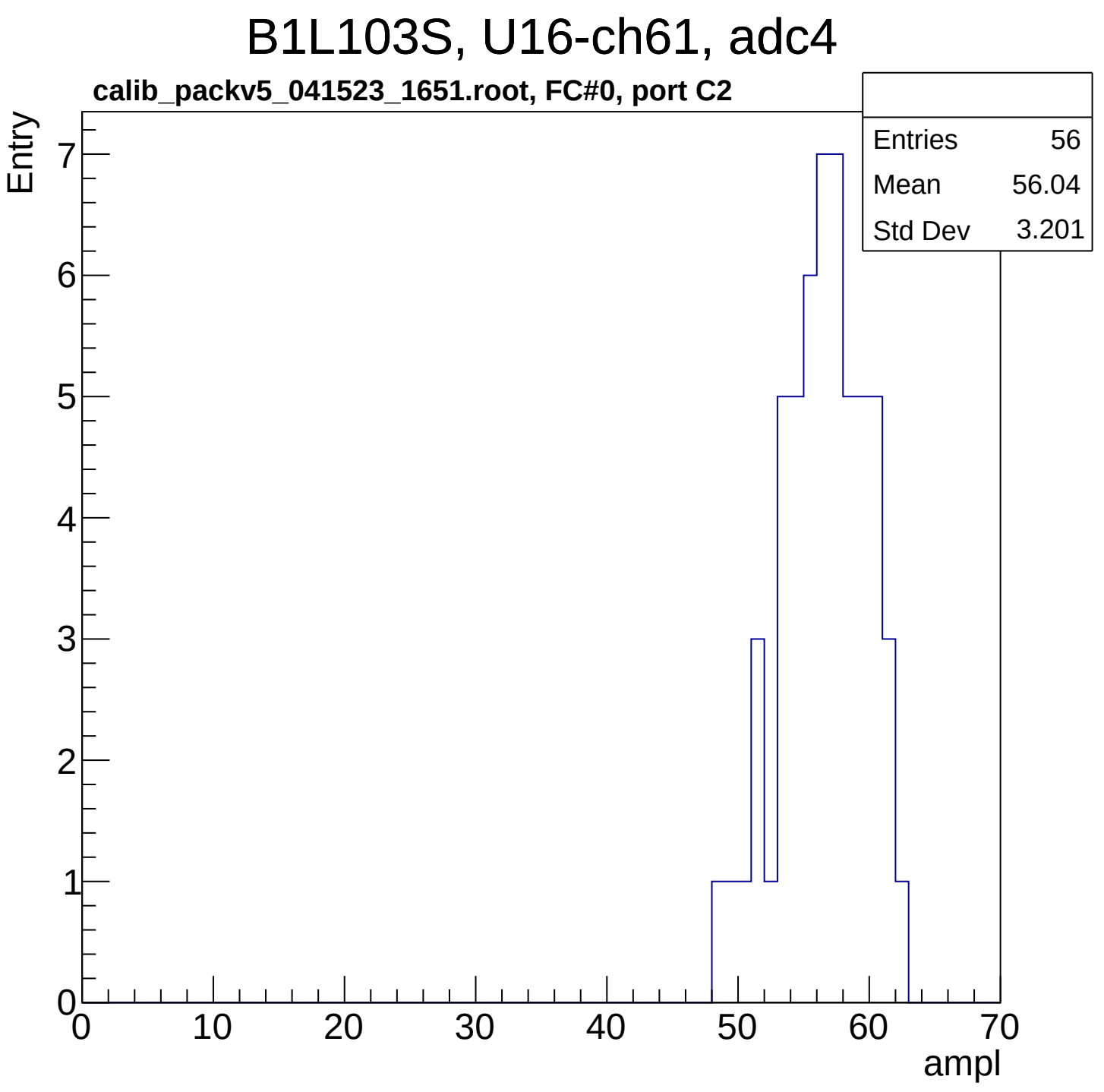
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

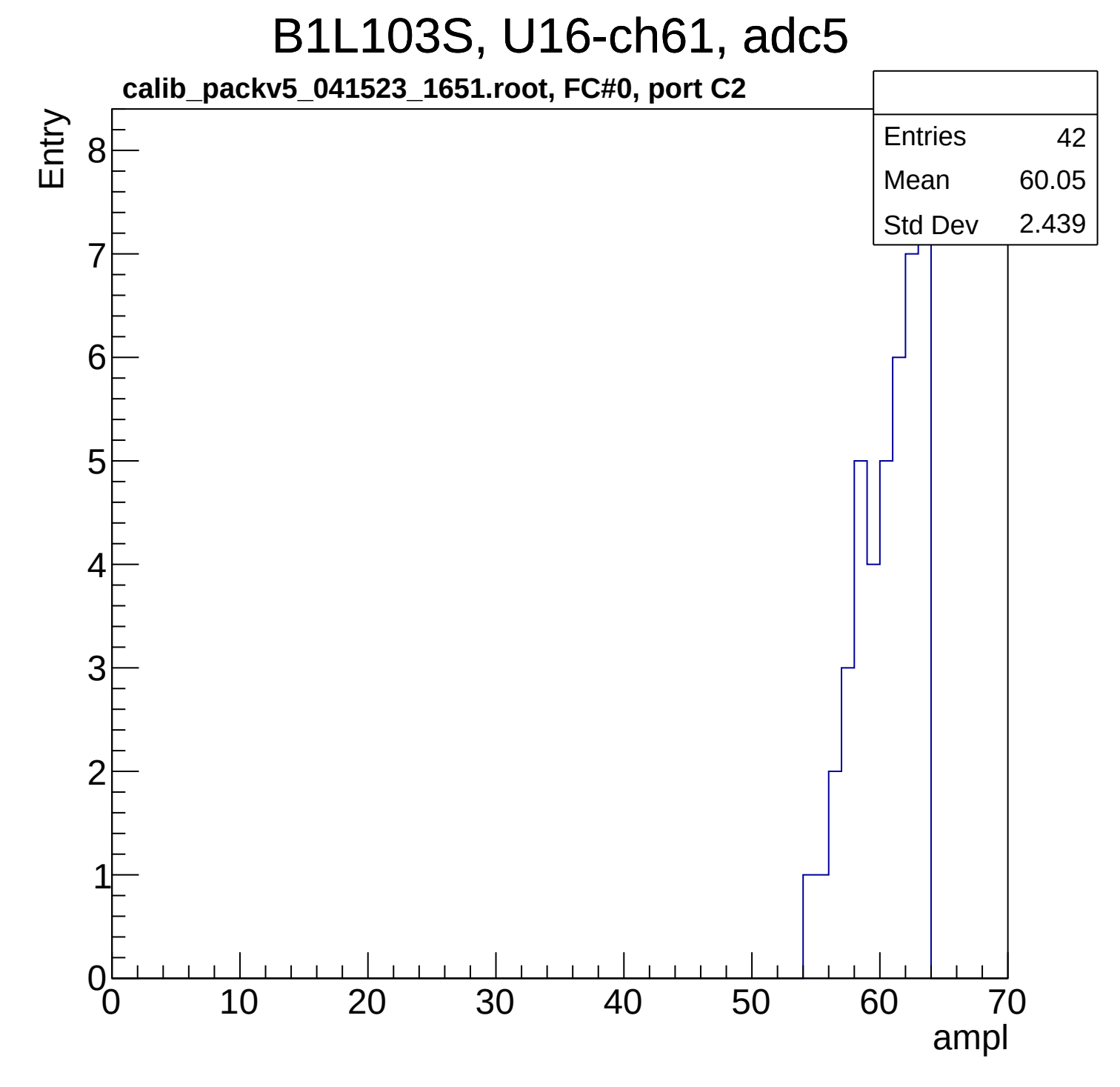

B1L103S, U16-ch61, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 24.02
Std Dev 12.29
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch61, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 34.58
Std Dev 8.04
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch61, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 37.24
Std Dev 15.44
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch61, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 47.61
Std Dev 10.35
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch61, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 56.04
Std Dev 3.201
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch61, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 60.05
Std Dev 2.439
Entry
ampl
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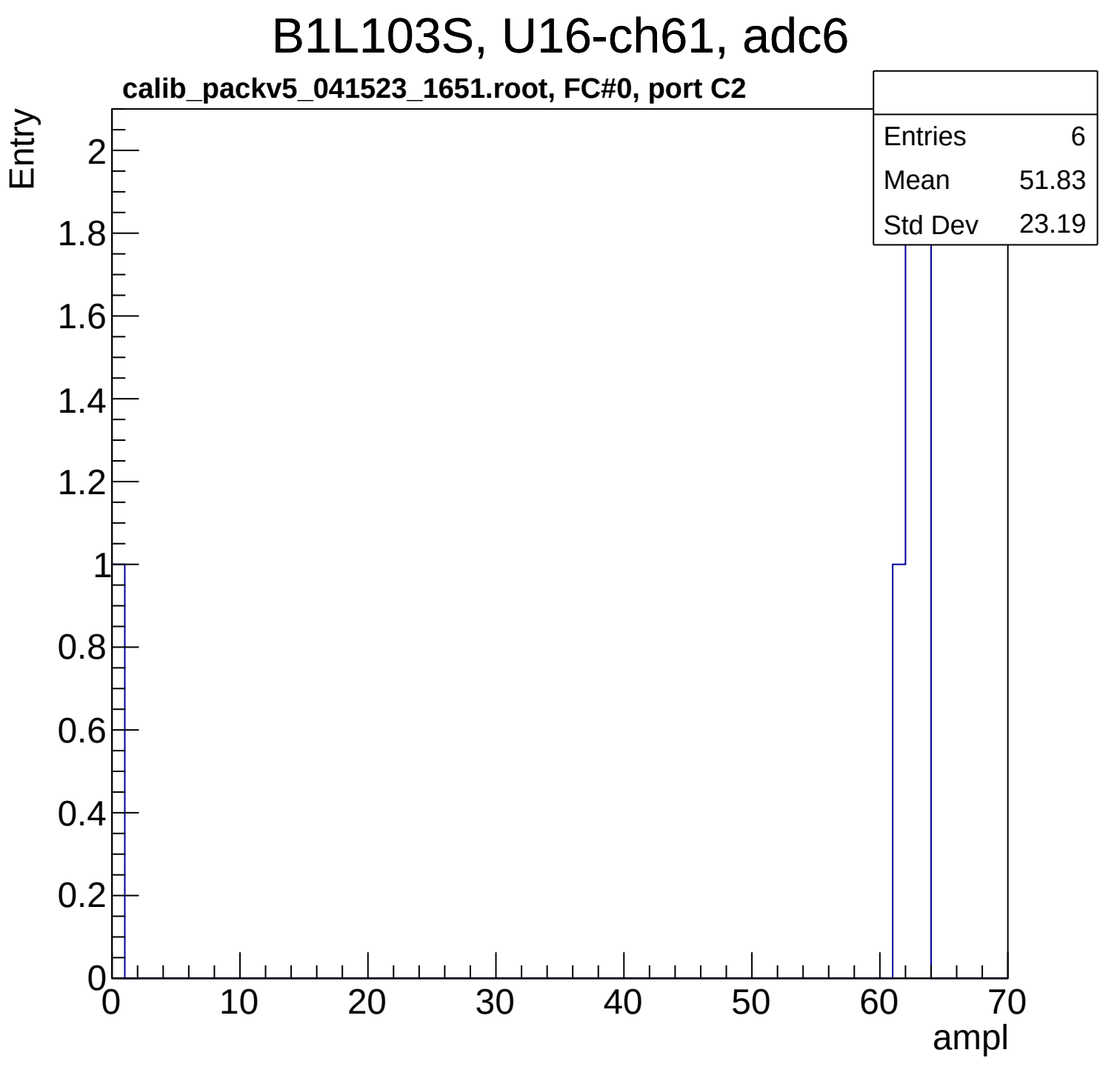
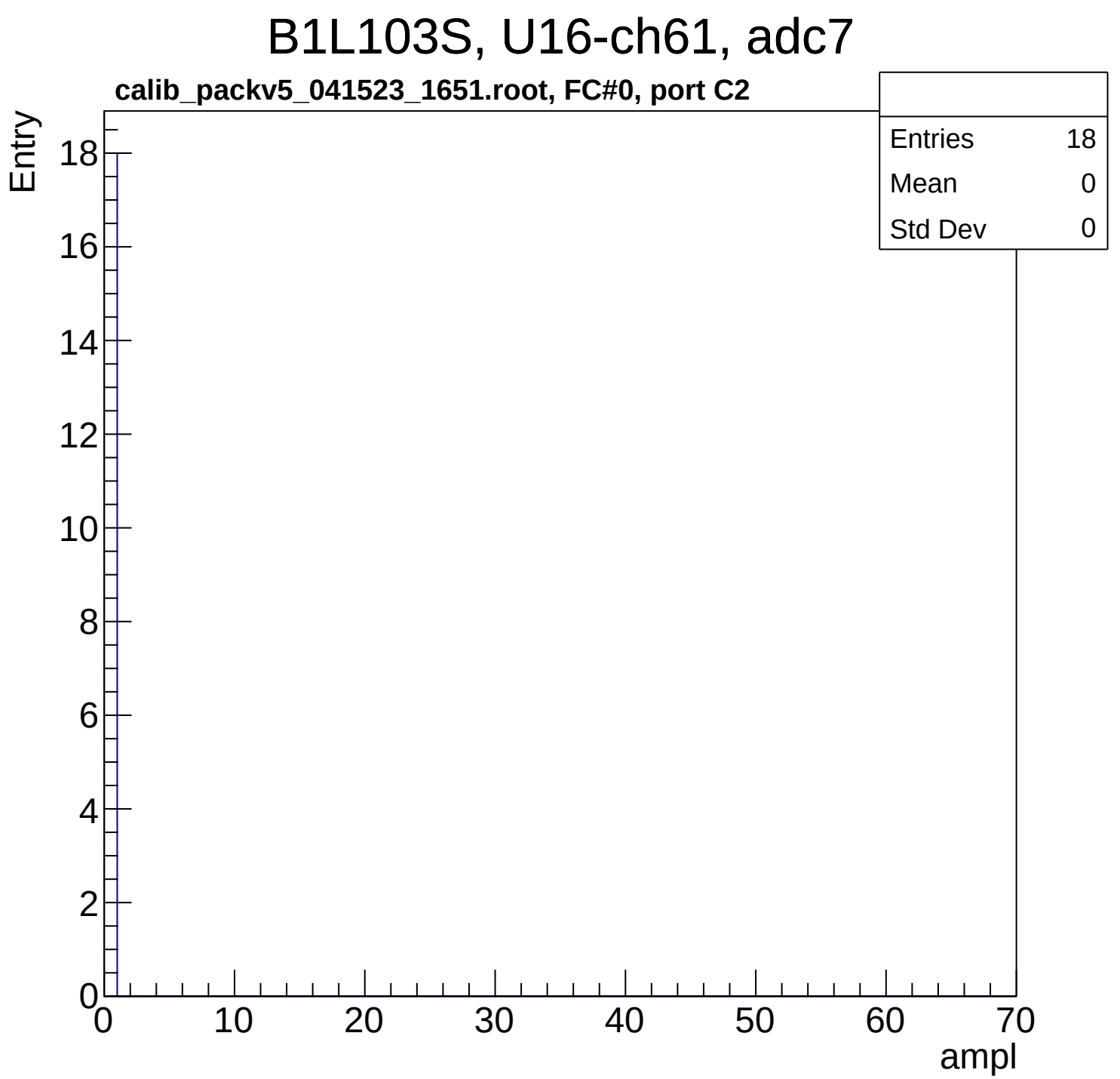
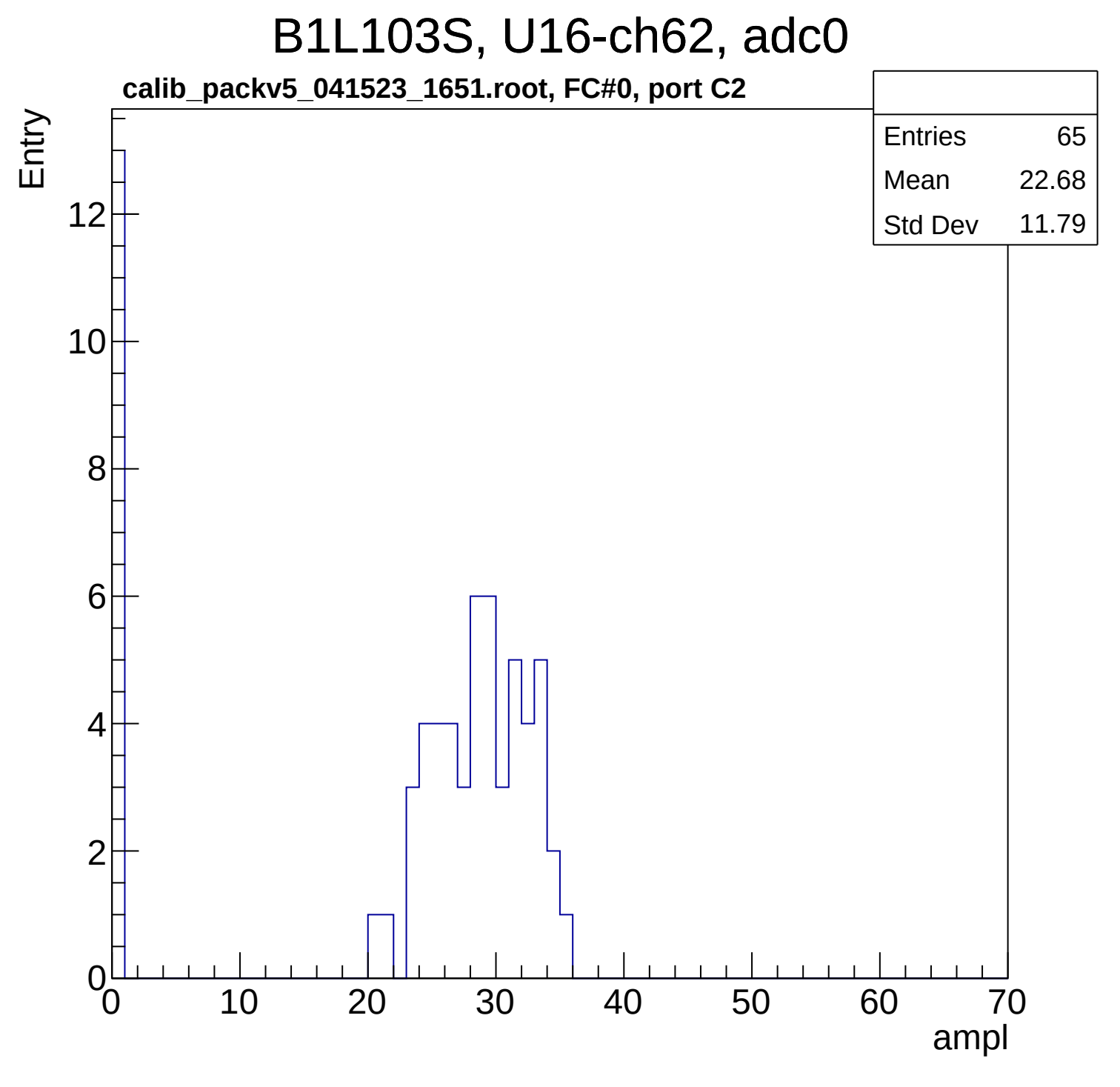
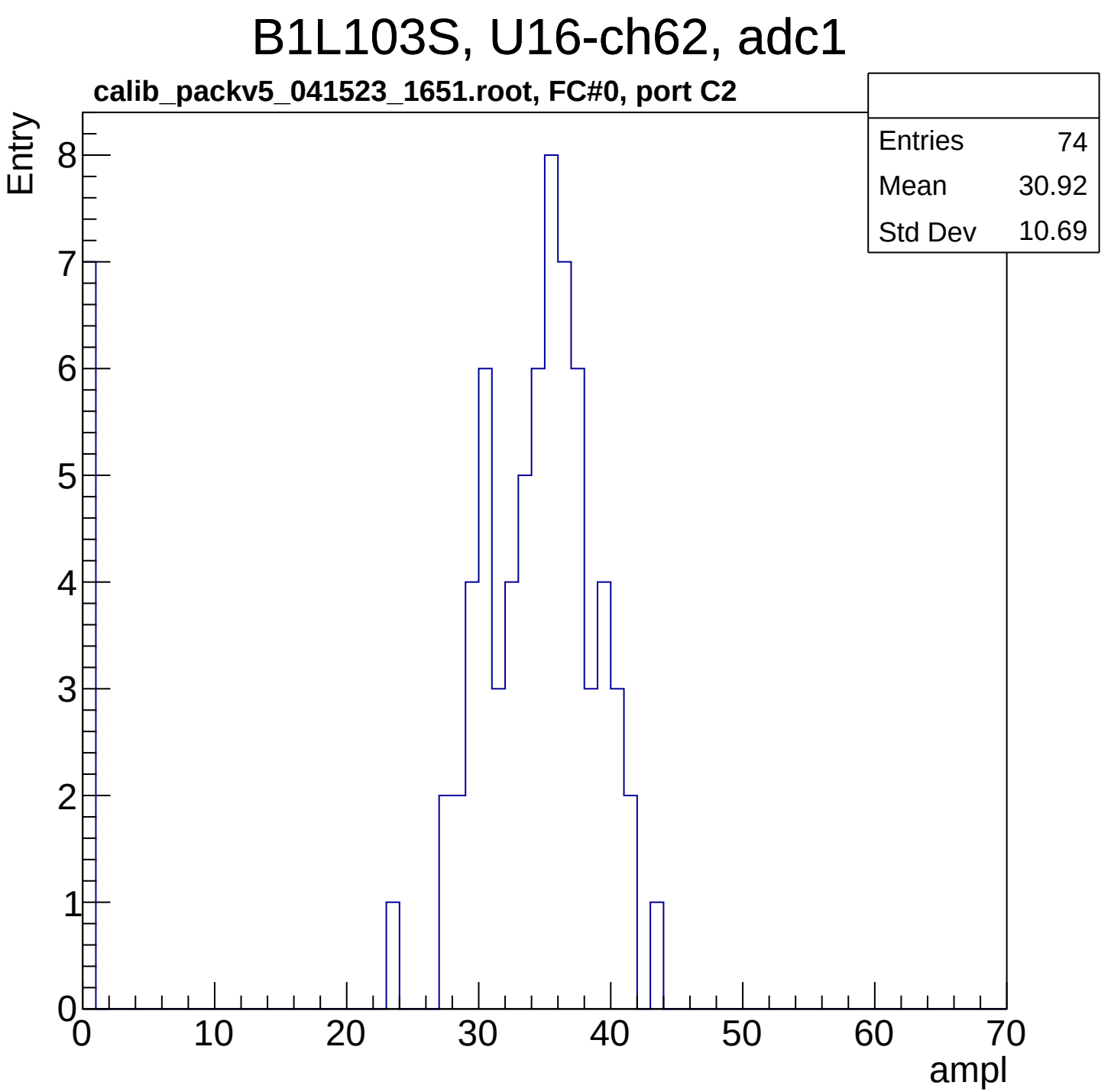
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch61, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 51.83
Std Dev 23.19
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U16-ch61, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch62, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 22.68
Std Dev 11.79
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch62, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 30.92
Std Dev 10.69
Entry
ampl
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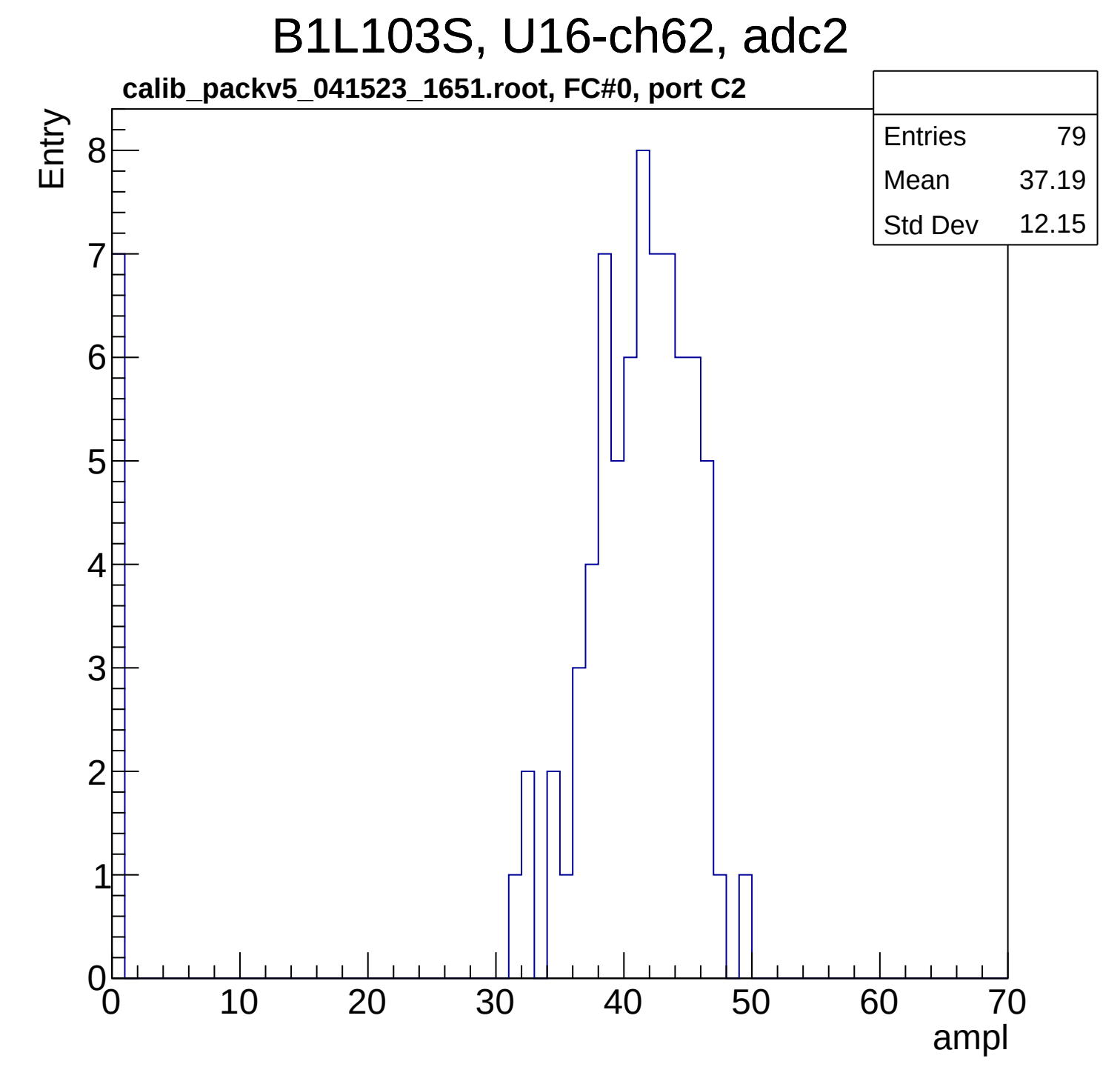
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch62, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 37.19
Std Dev 12.15
Entry
ampl
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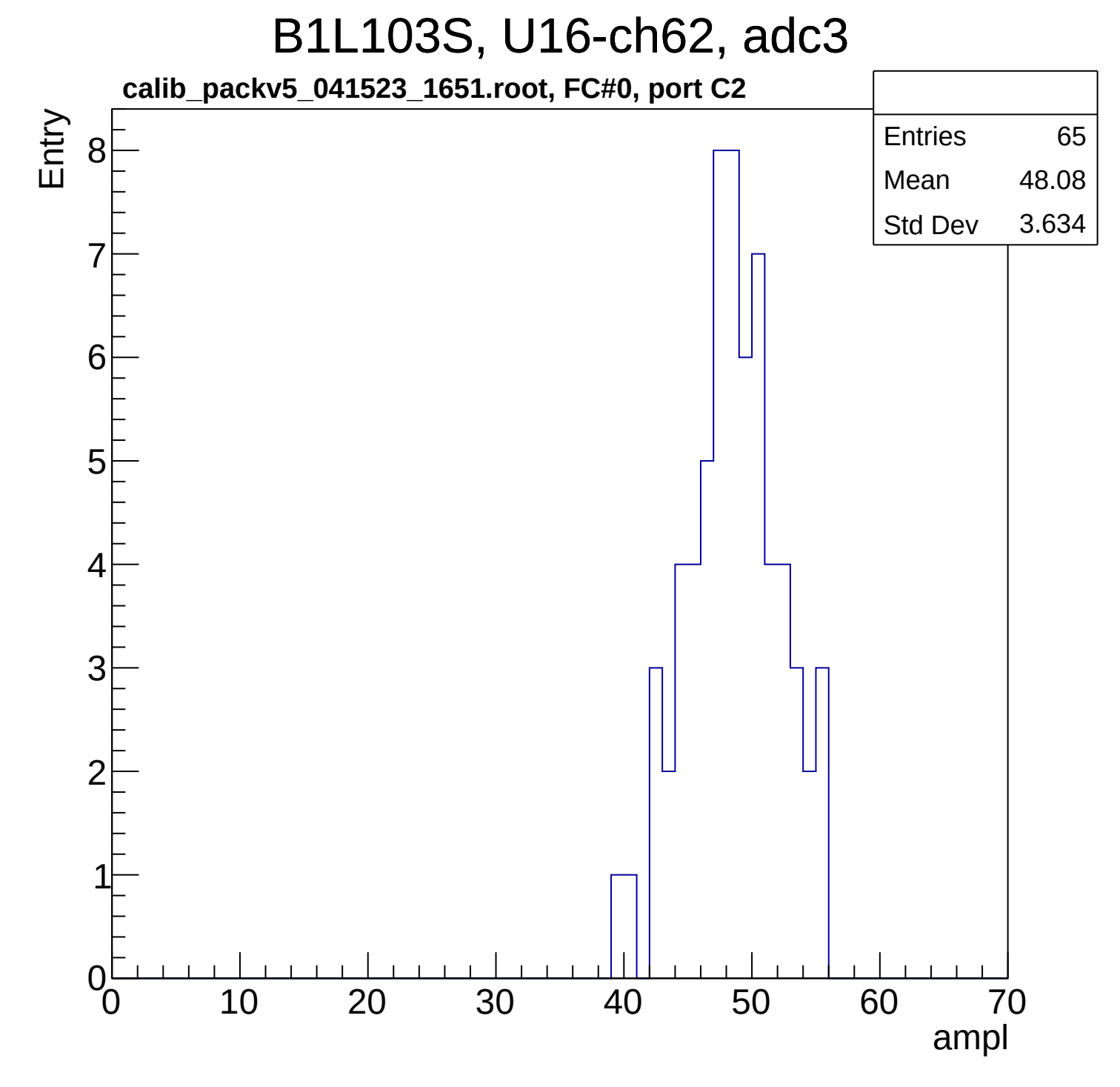
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch62, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 48.08
Std Dev 3.634
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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40
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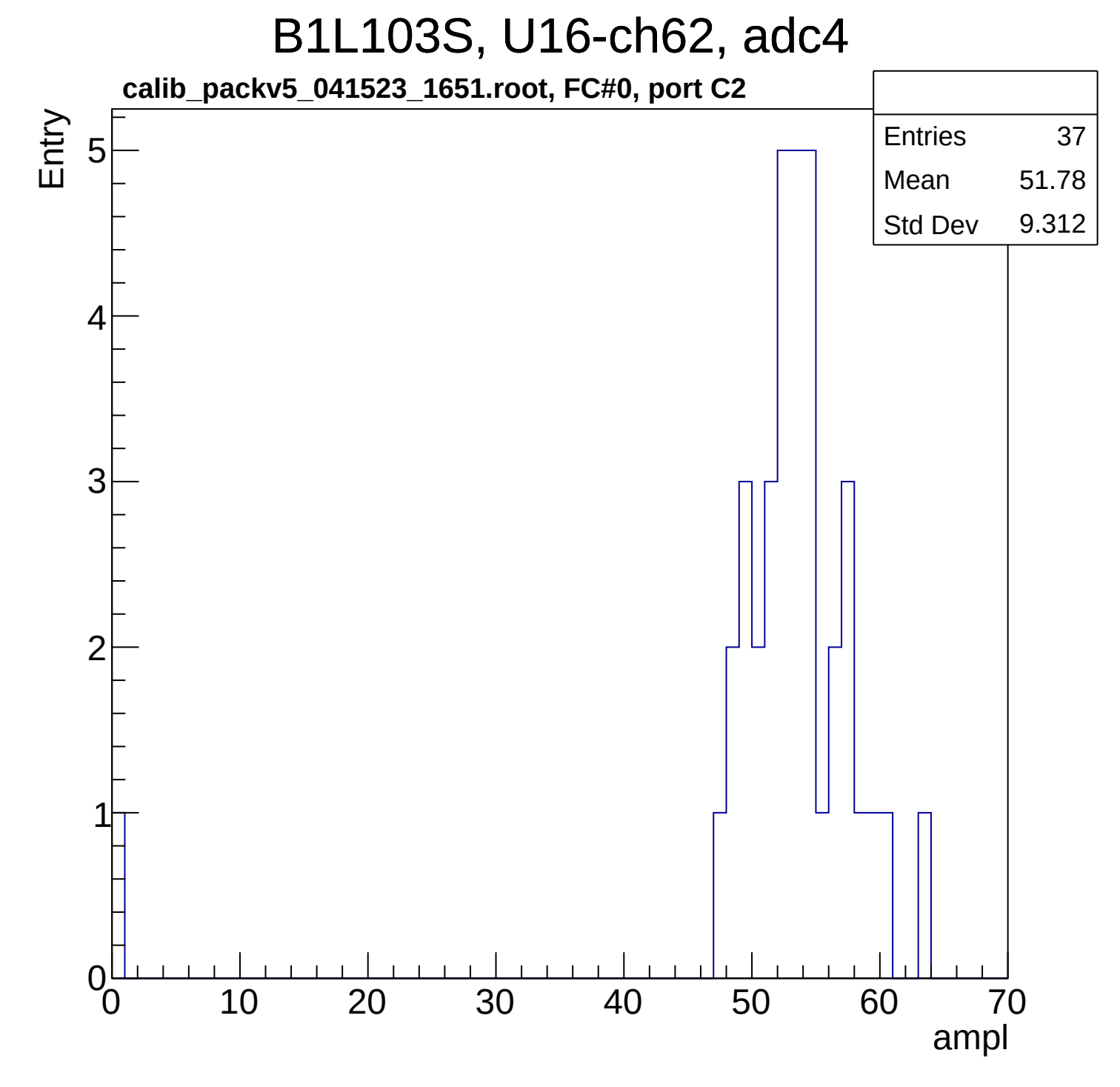
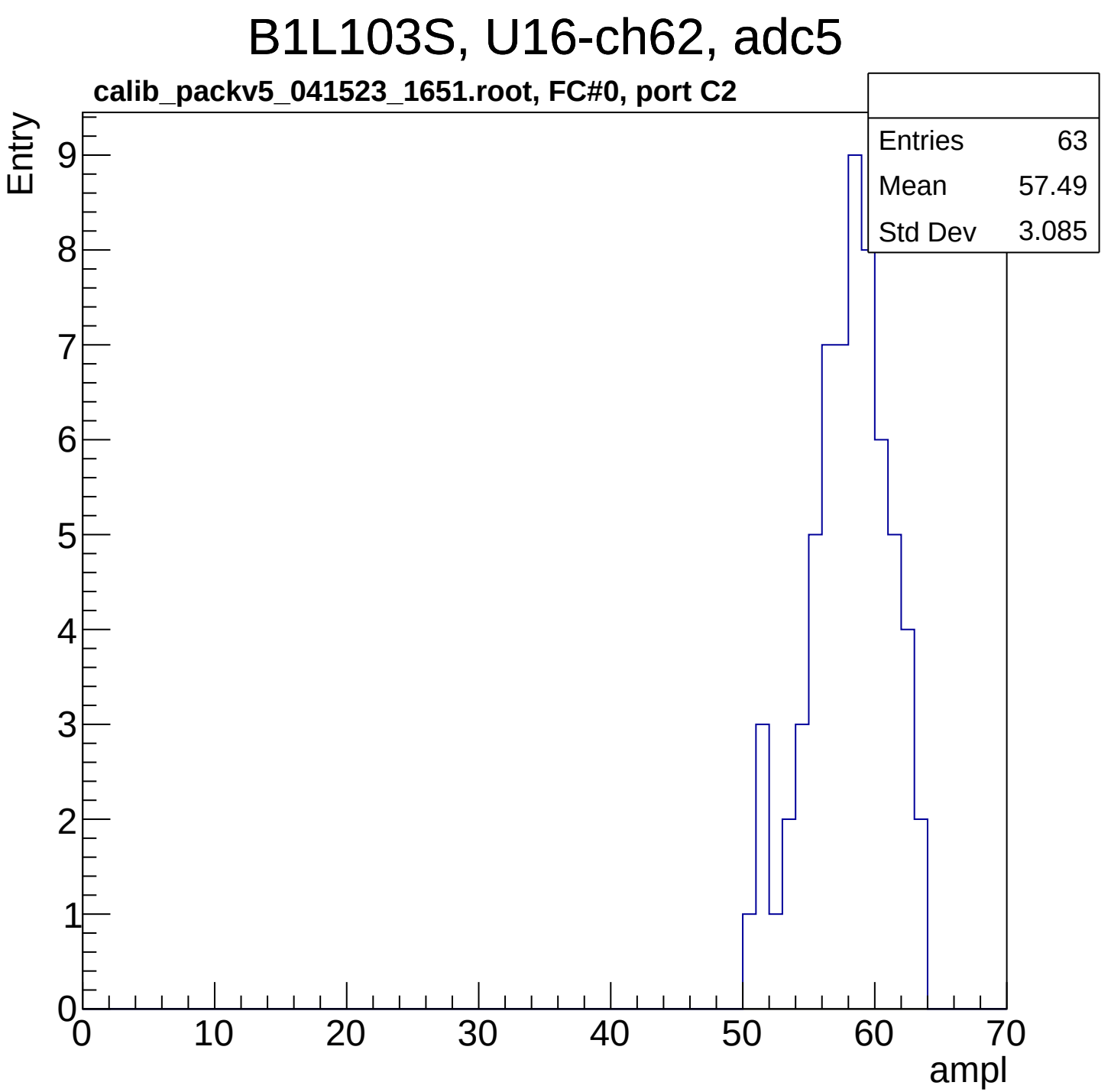
60
70


B1L103S, U16-ch62, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 51.78
Std Dev 9.312
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch62, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 57.49
Std Dev 3.085
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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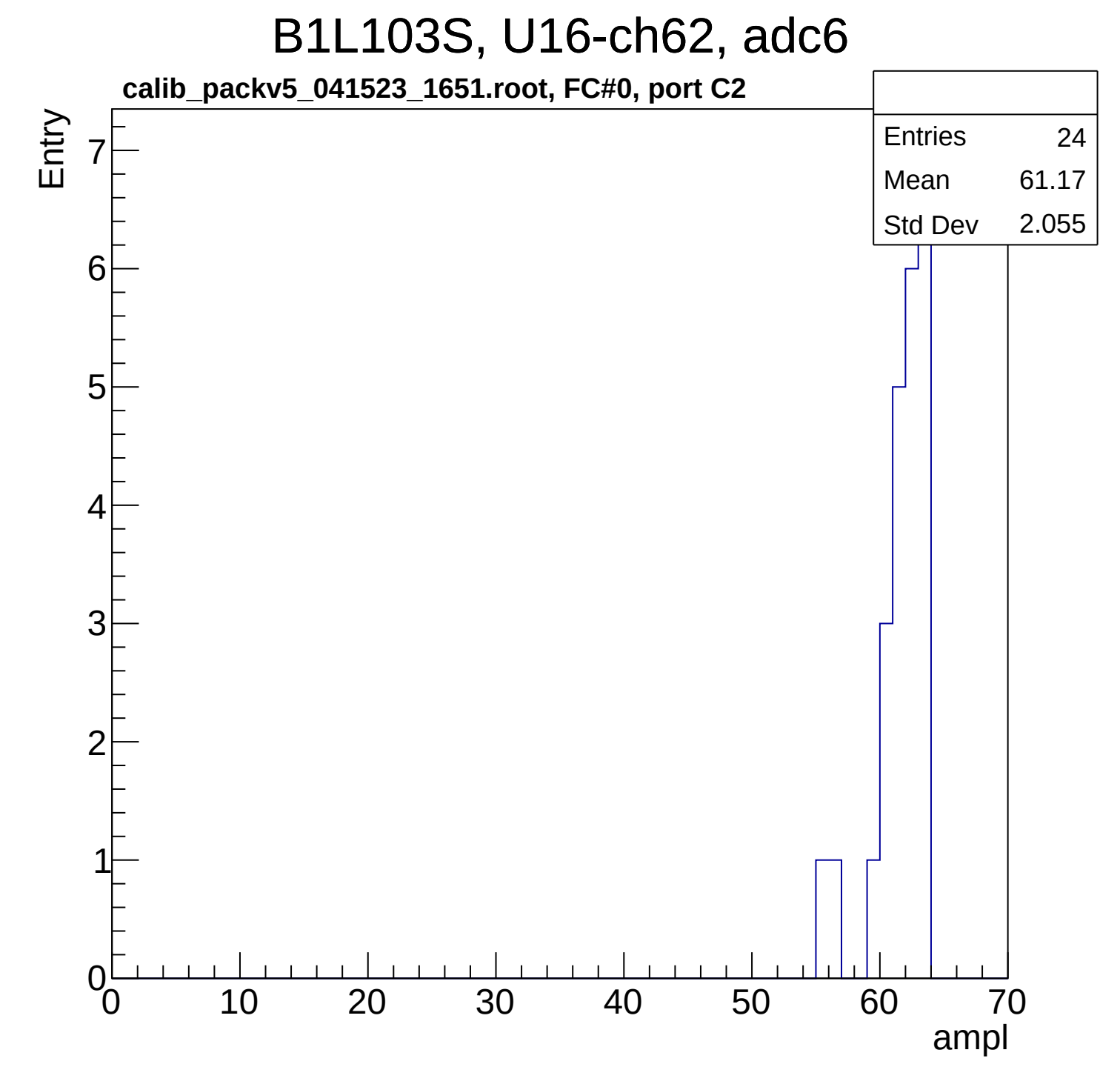
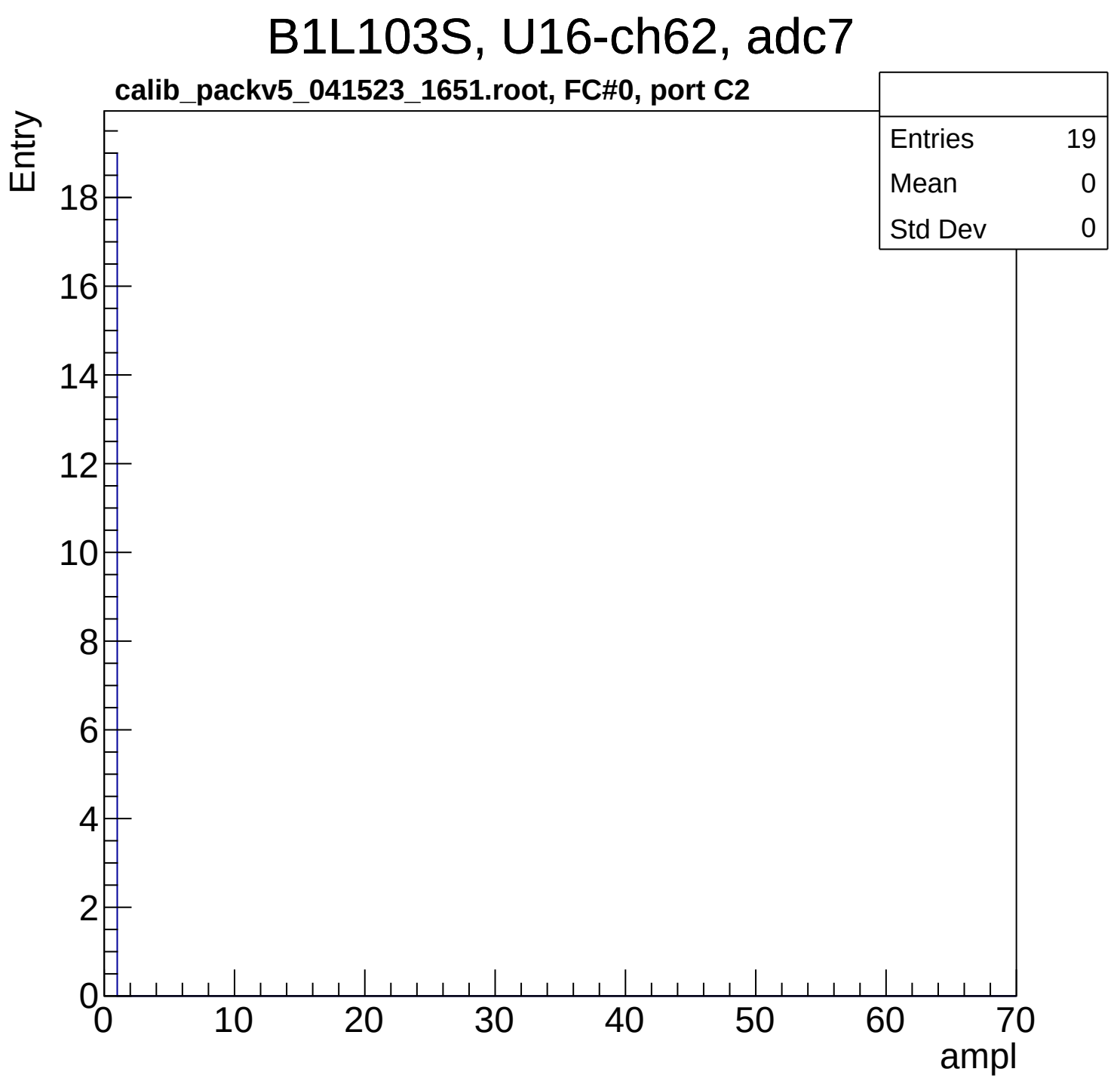
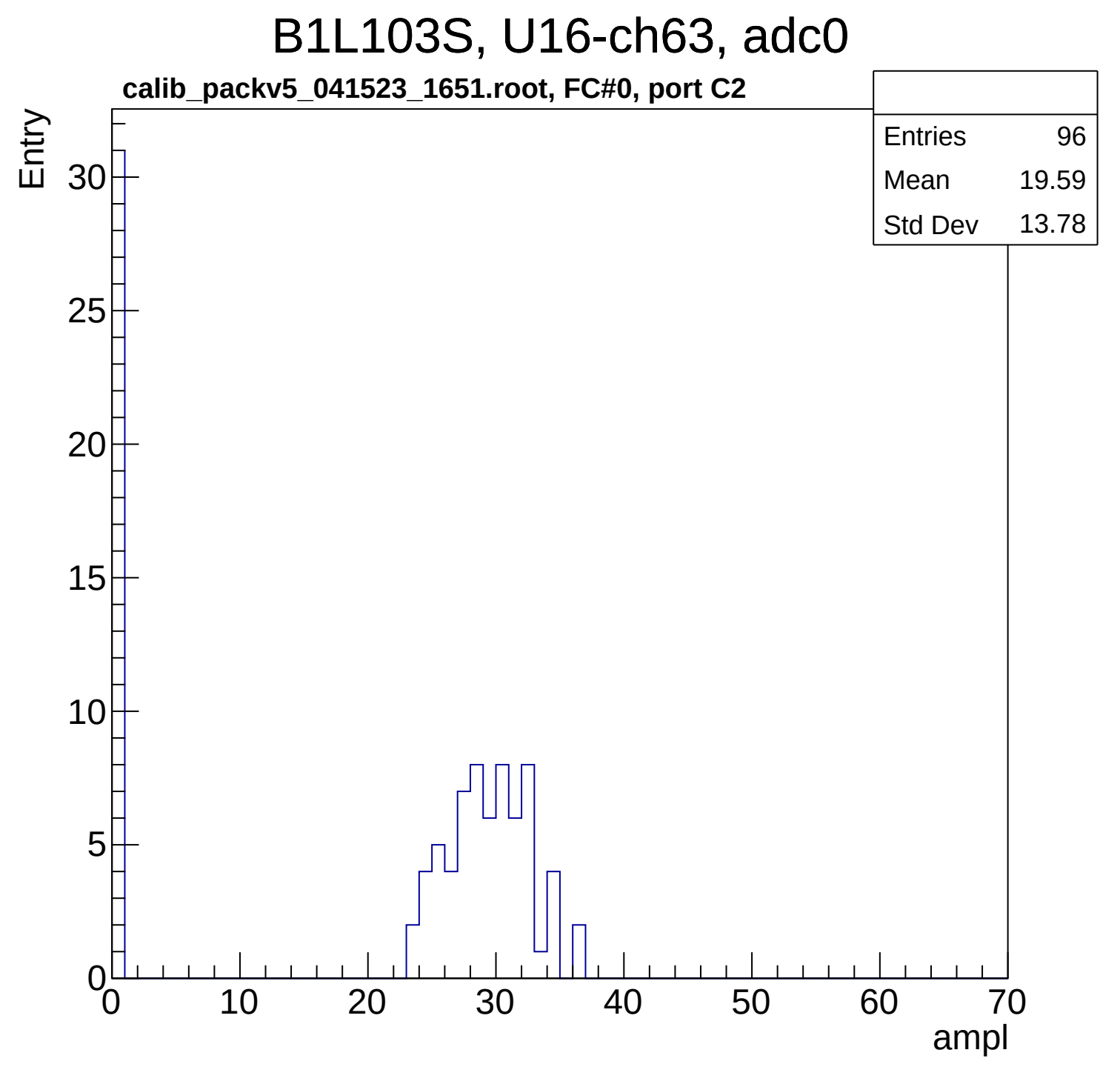
40
50
60
70


B1L103S, U16-ch62, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 61.17
Std Dev 2.055
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch62, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch63, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 19.59
Std Dev 13.78
Entry
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10
15
20
25
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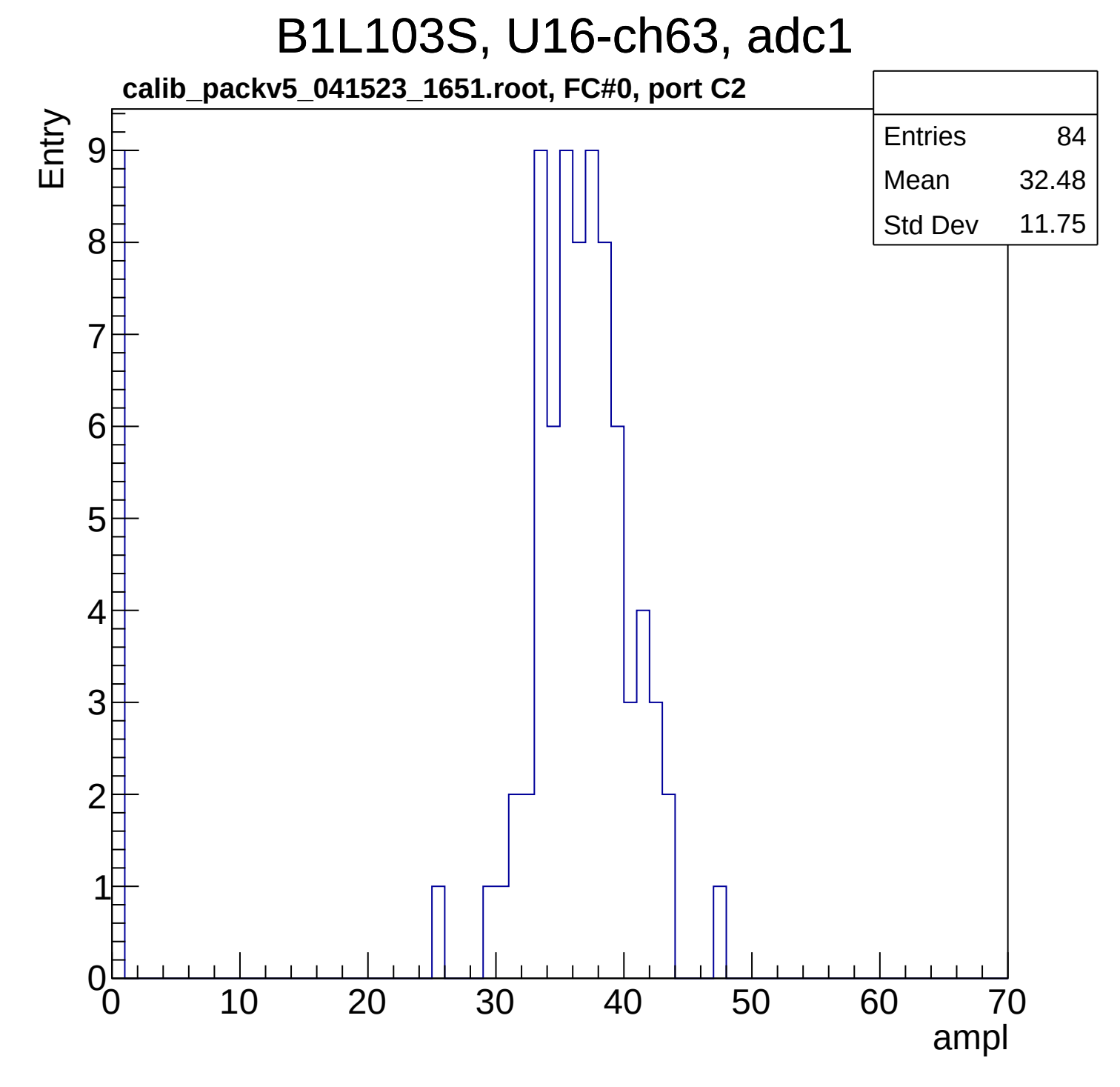
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch63, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 32.48
Std Dev 11.75
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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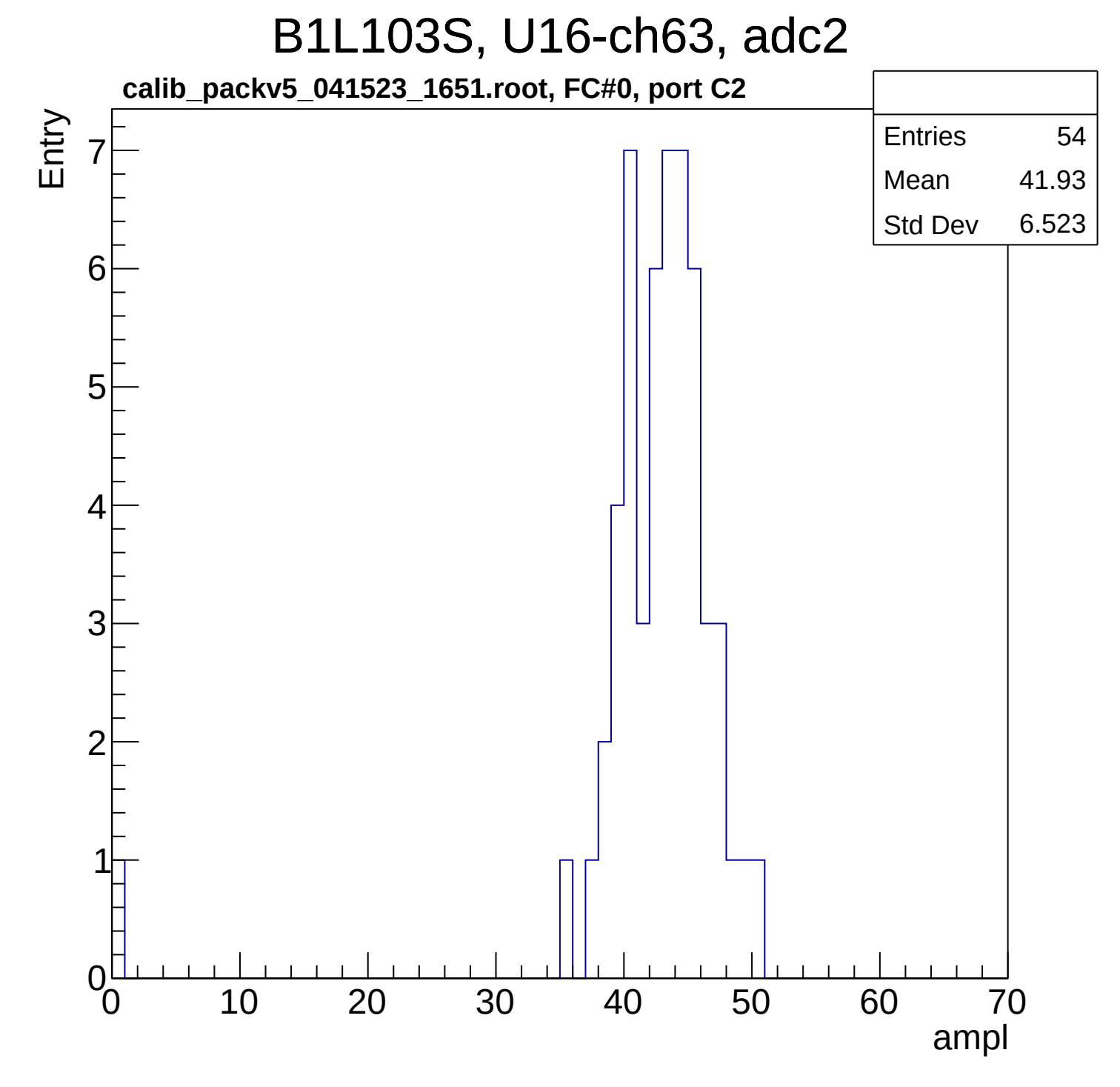
B1L103S, U16-ch63, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 41.93
Std Dev 6.523
Entry
ampl
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1
2
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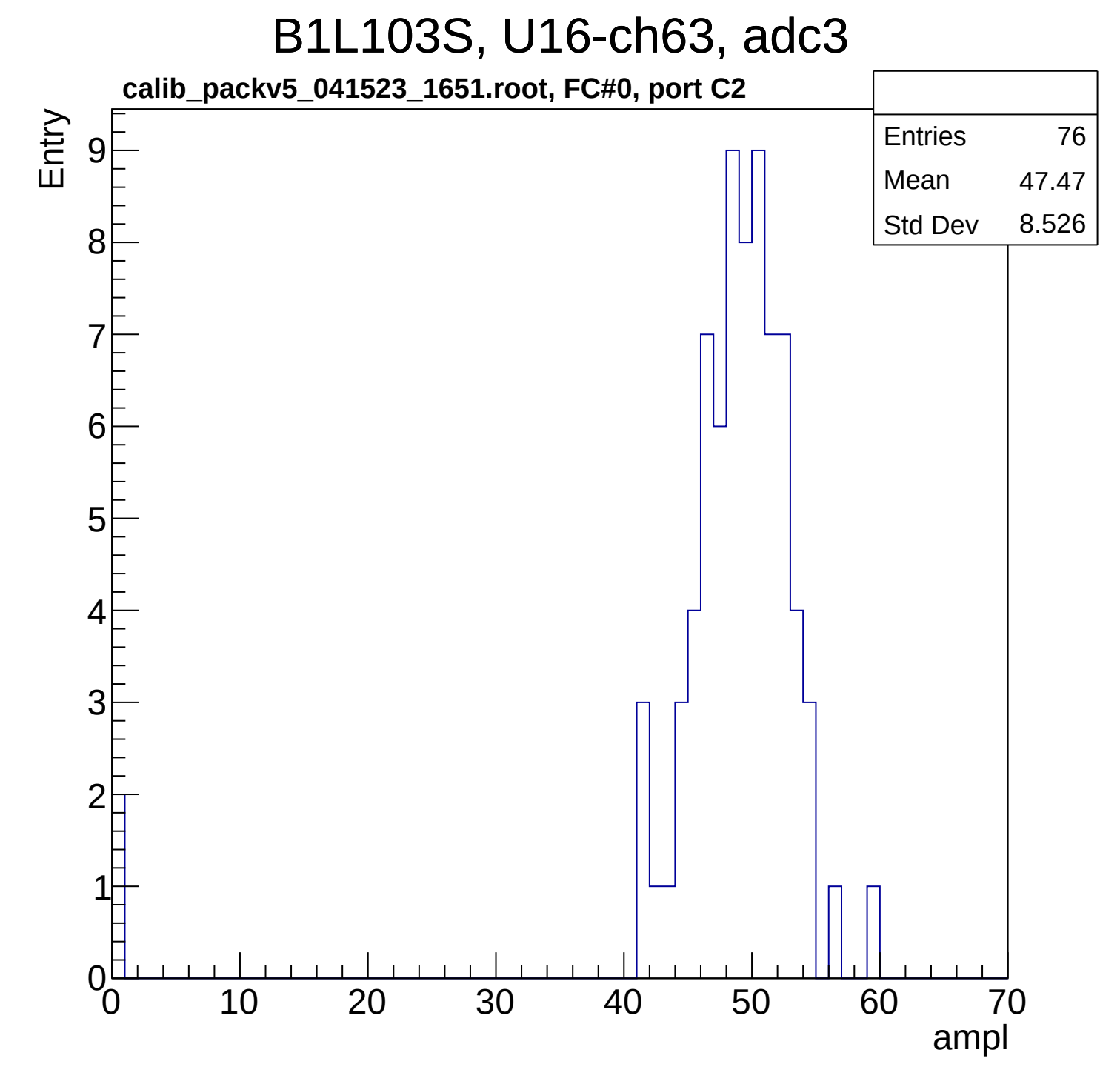
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch63, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 47.47
Std Dev 8.526
Entry
ampl
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2
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6
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8
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0
10
20
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40
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60
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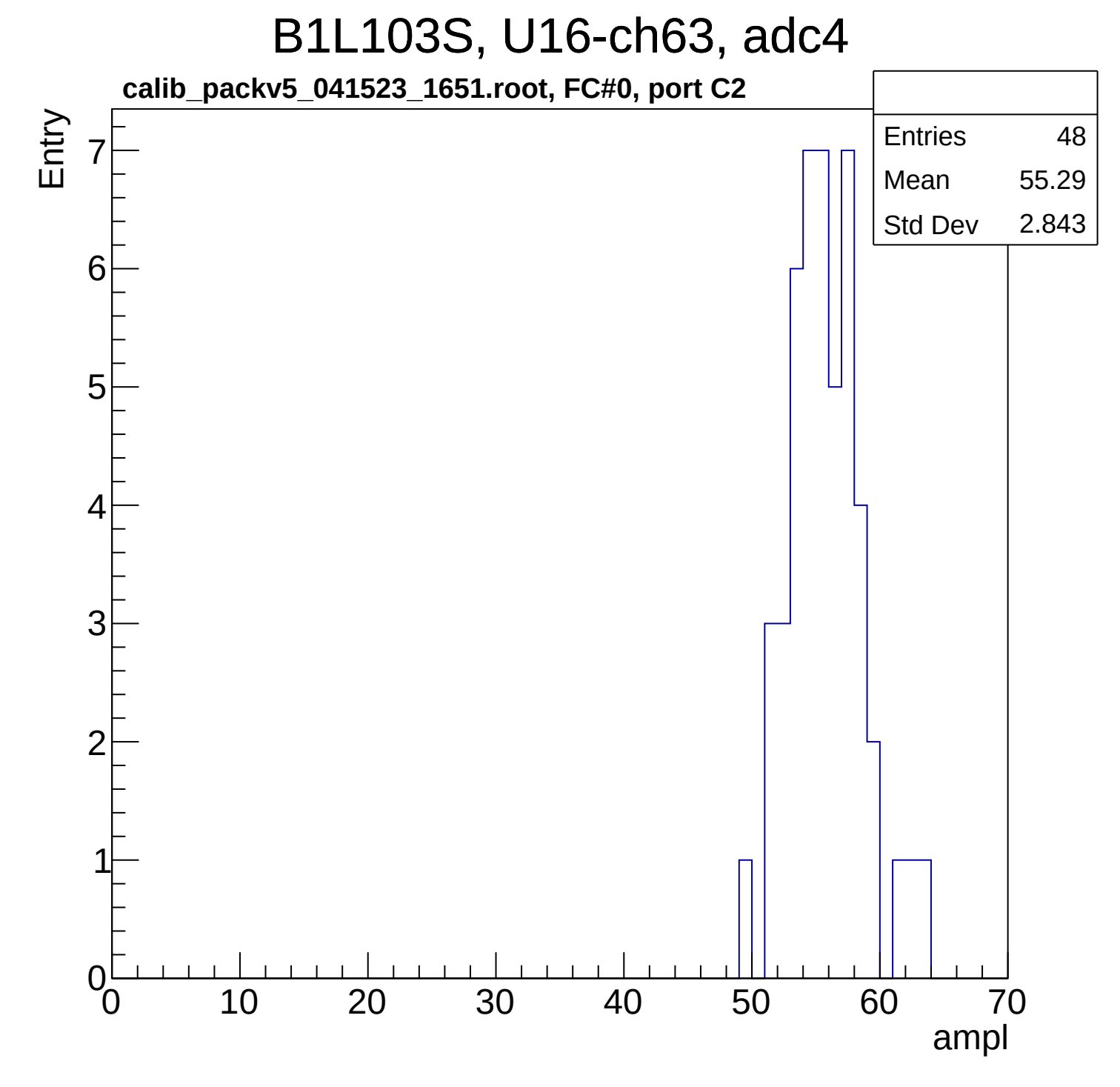
B1L103S, U16-ch63, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 55.29
Std Dev 2.843
Entry
ampl
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3
4
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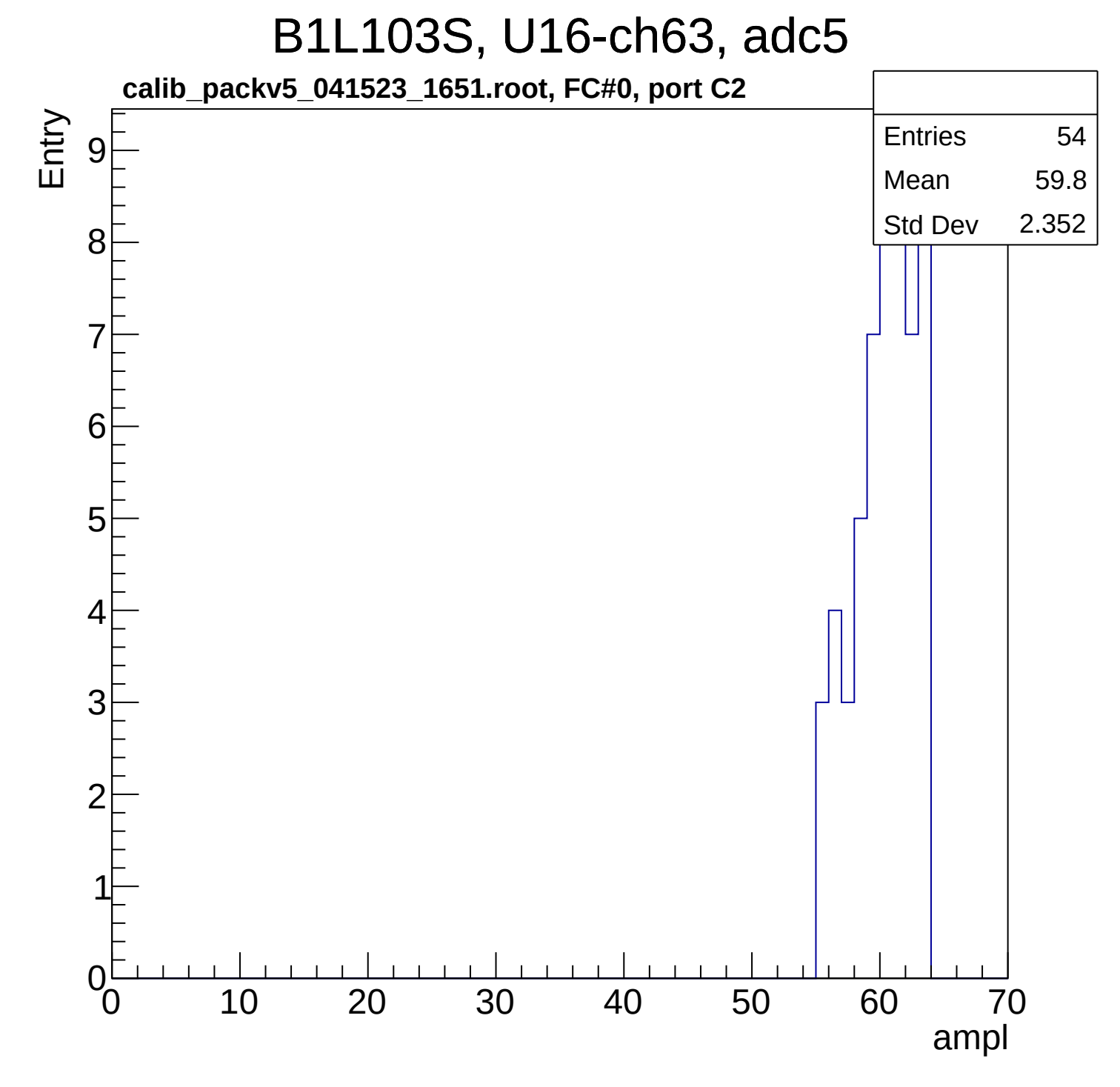
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch63, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 59.8
Std Dev 2.352
Entry
ampl
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2
3
4
5
6
7
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9
0
10
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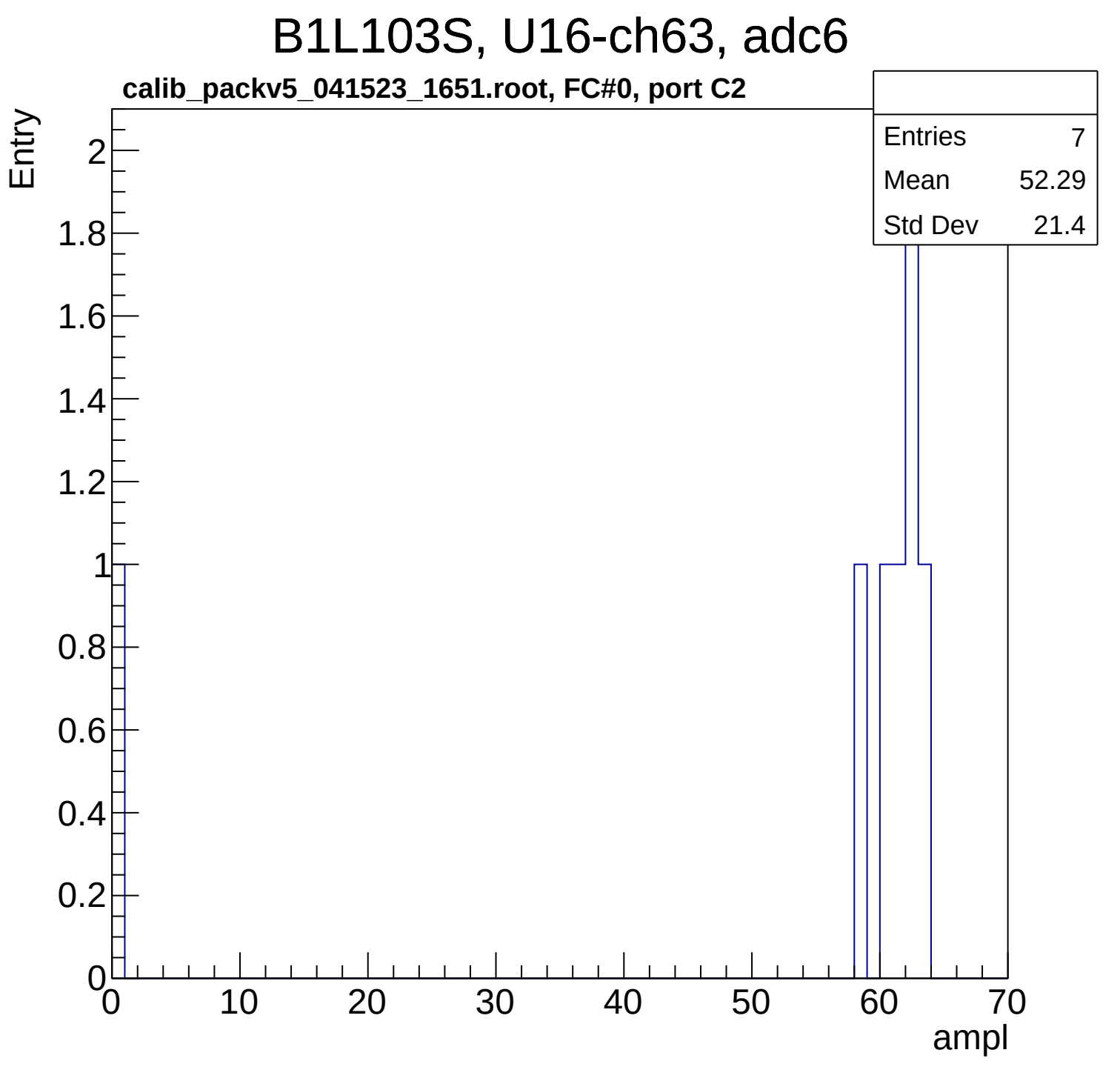
30
40
50
60
70


B1L103S, U16-ch63, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 52.29
Std Dev 21.4
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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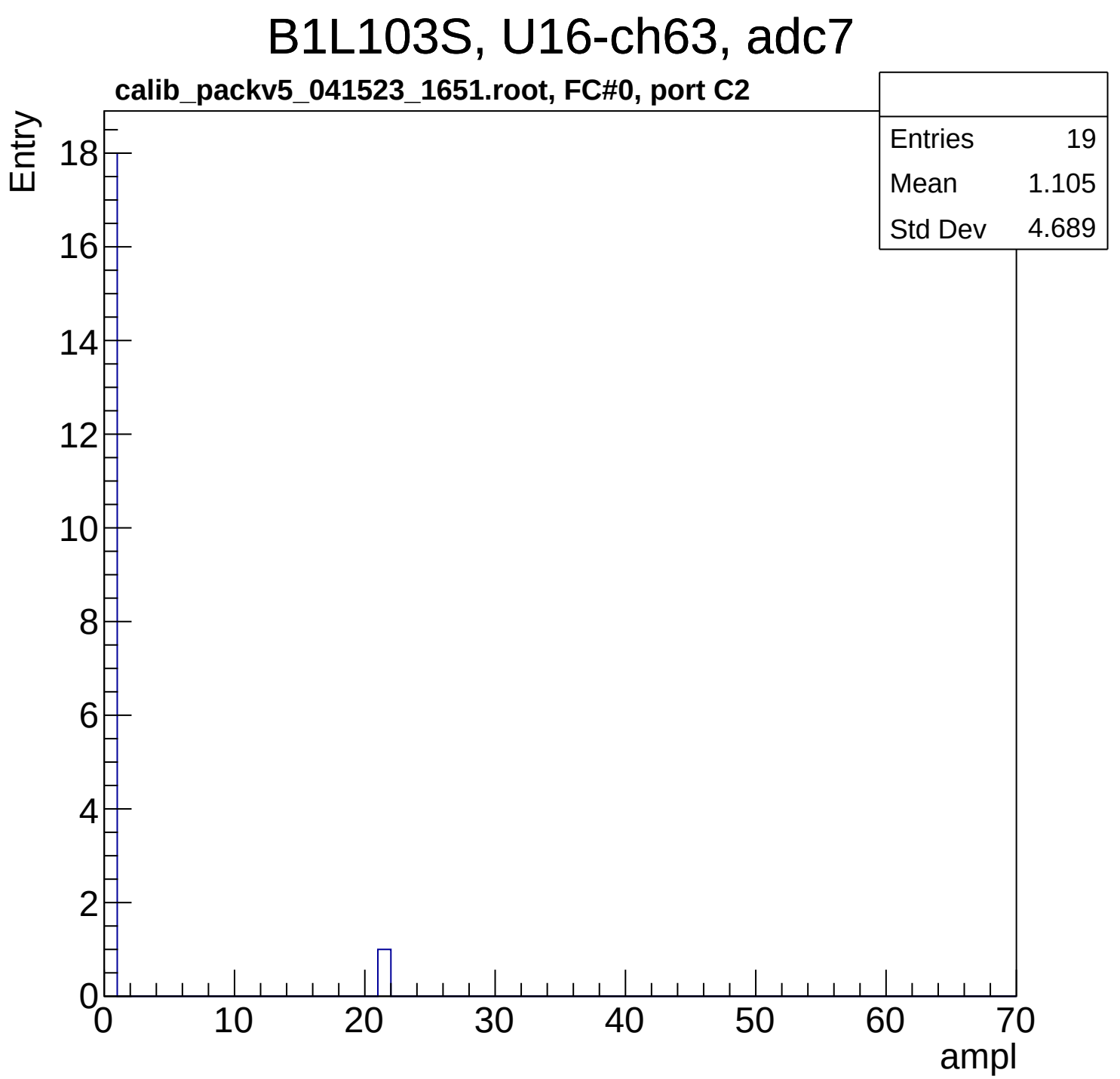
40
50
60
70


B1L103S, U16-ch63, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
0
2
4
6
8
10
12
14
16
18
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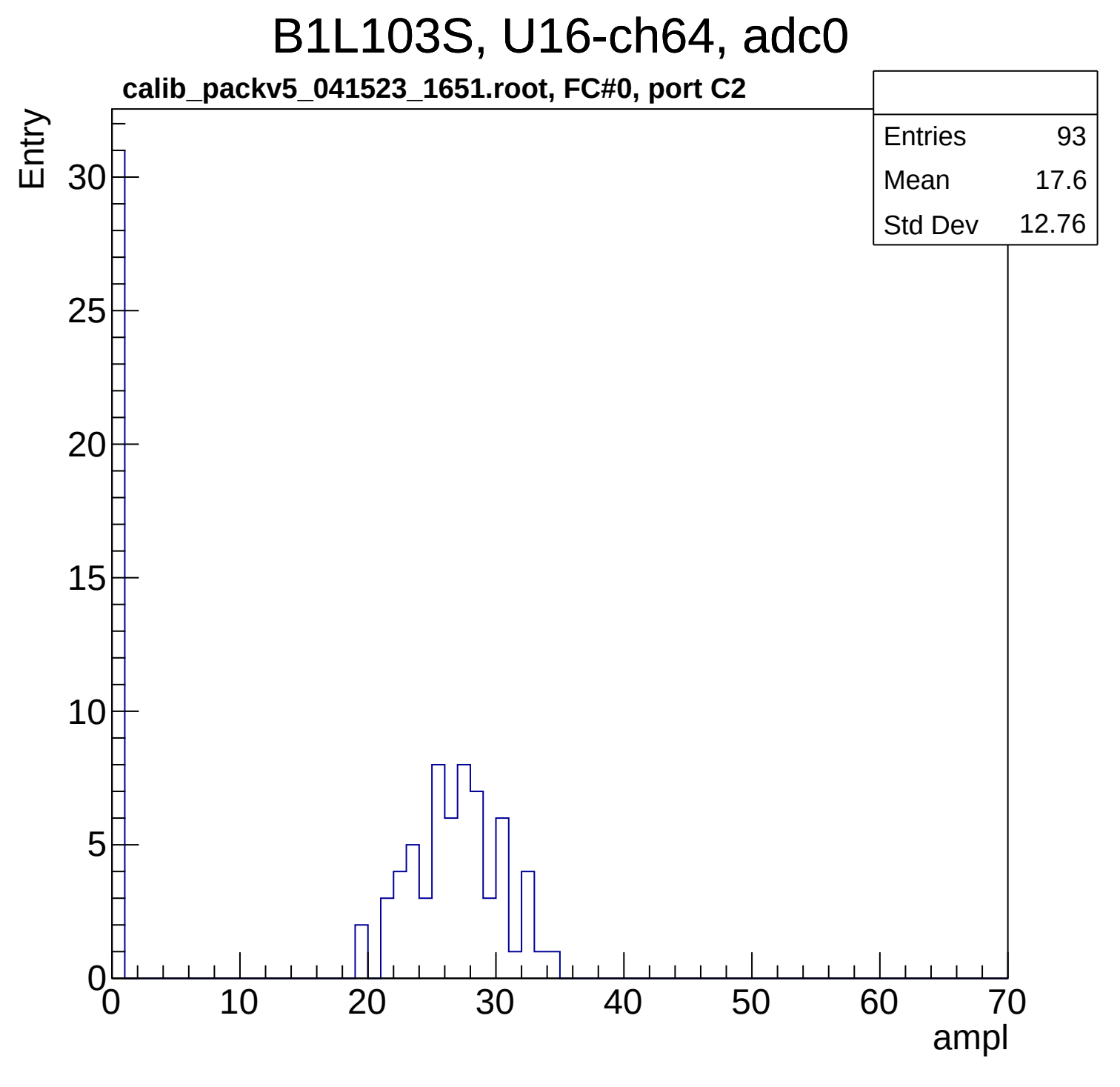
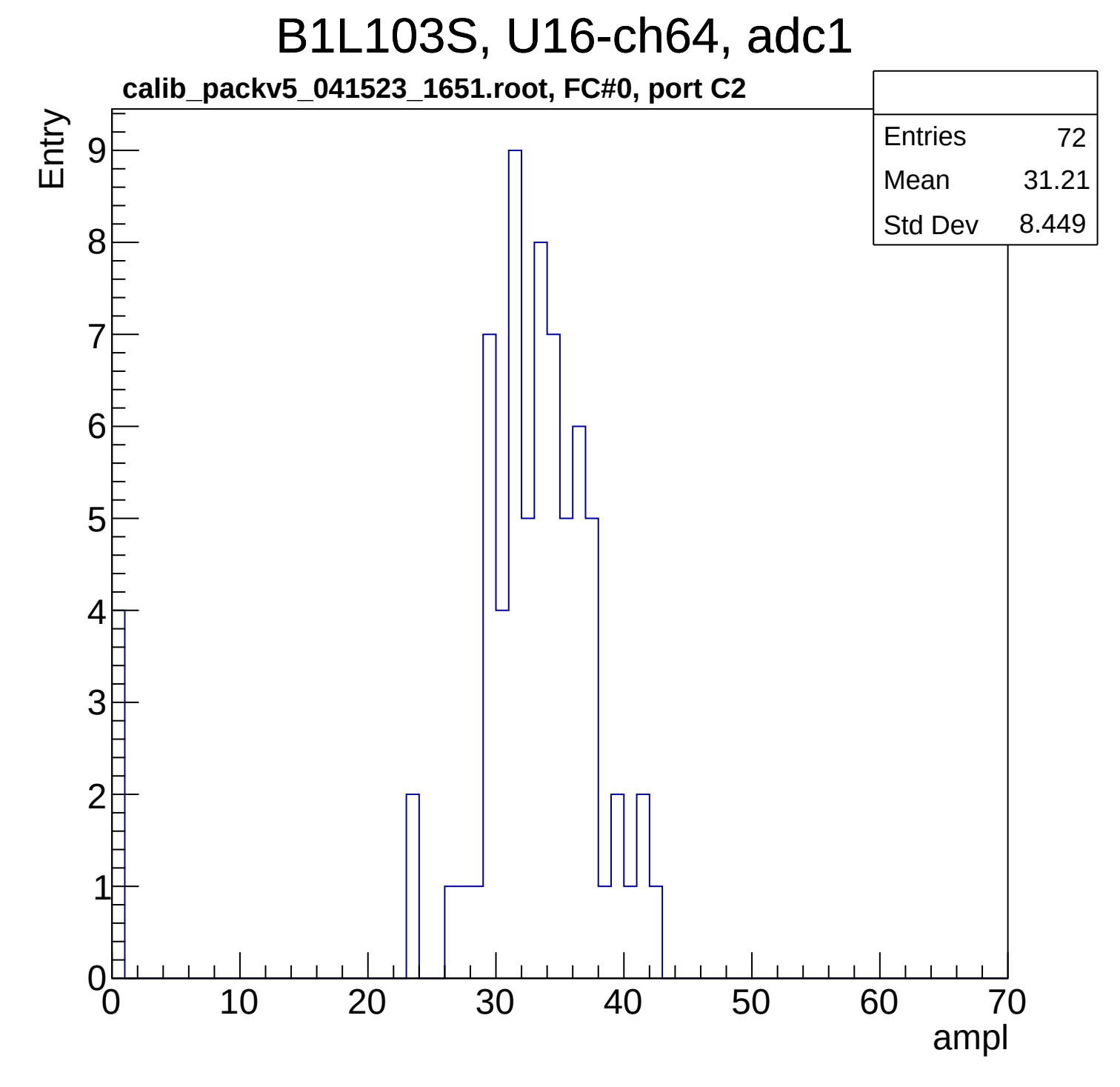
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch64, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 17.6
Std Dev 12.76
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch64, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 31.21
Std Dev 8.449
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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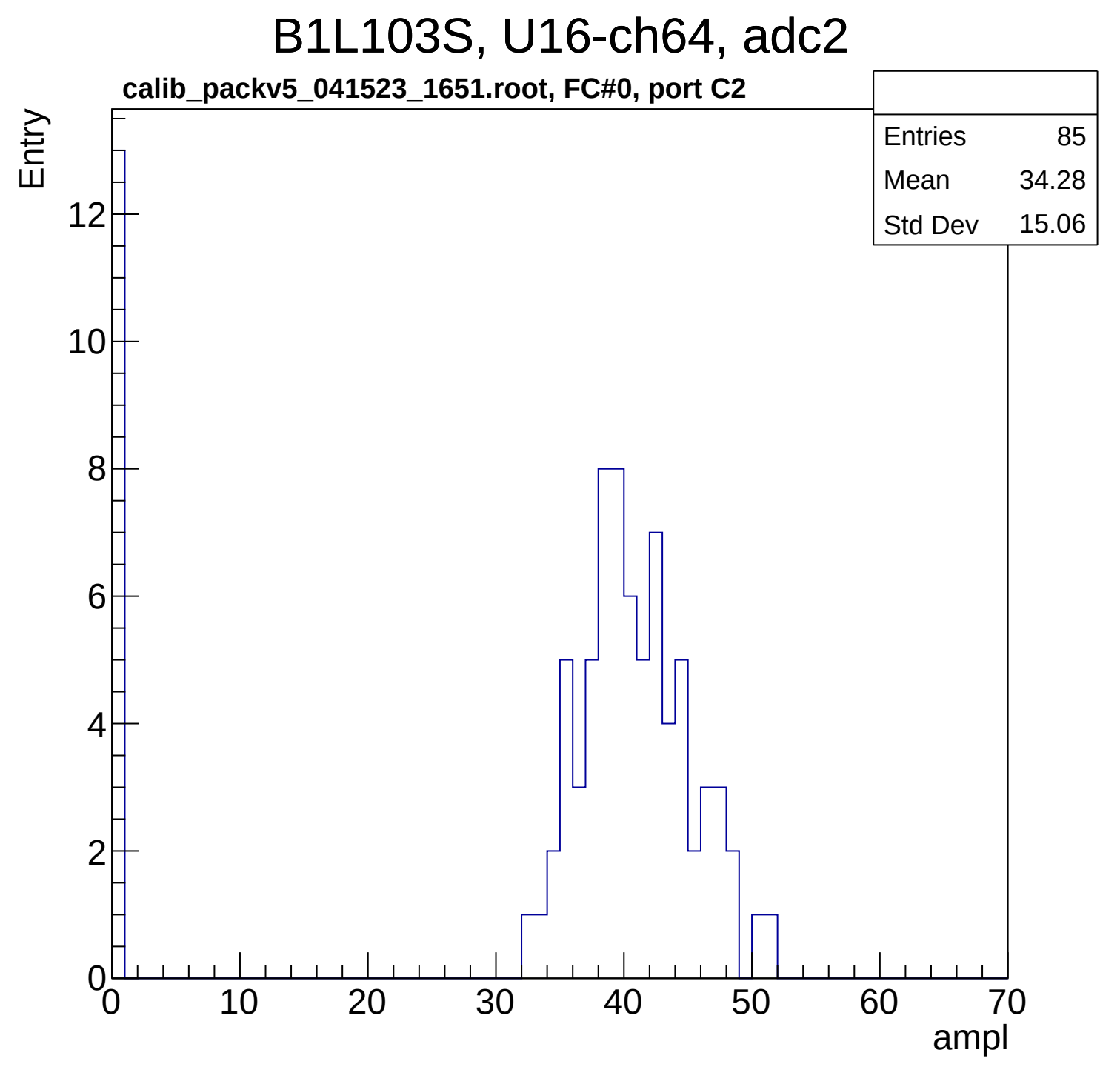
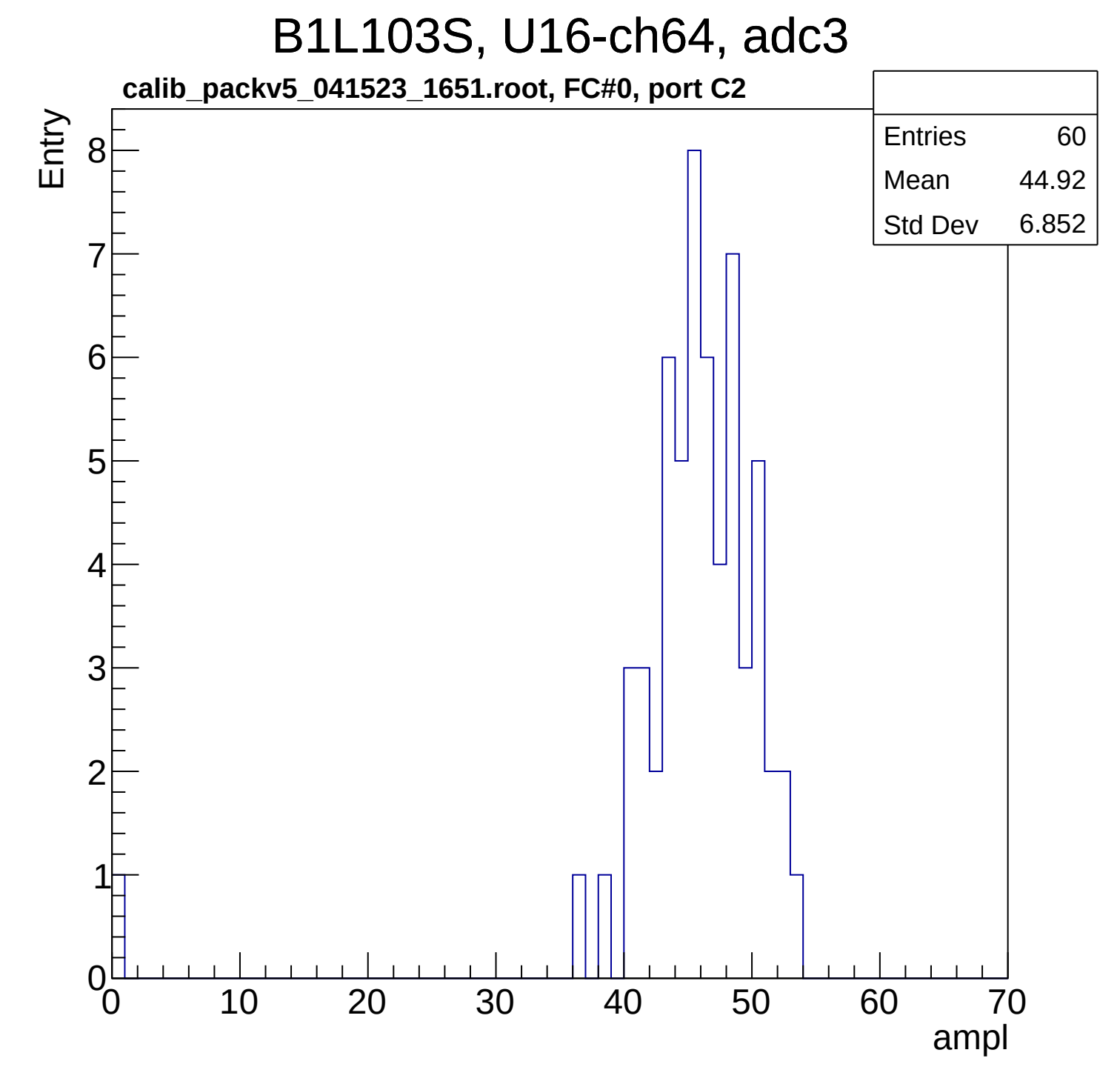

B1L103S, U16-ch64, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 34.28
Std Dev 15.06
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch64, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 44.92
Std Dev 6.852
Entry
ampl
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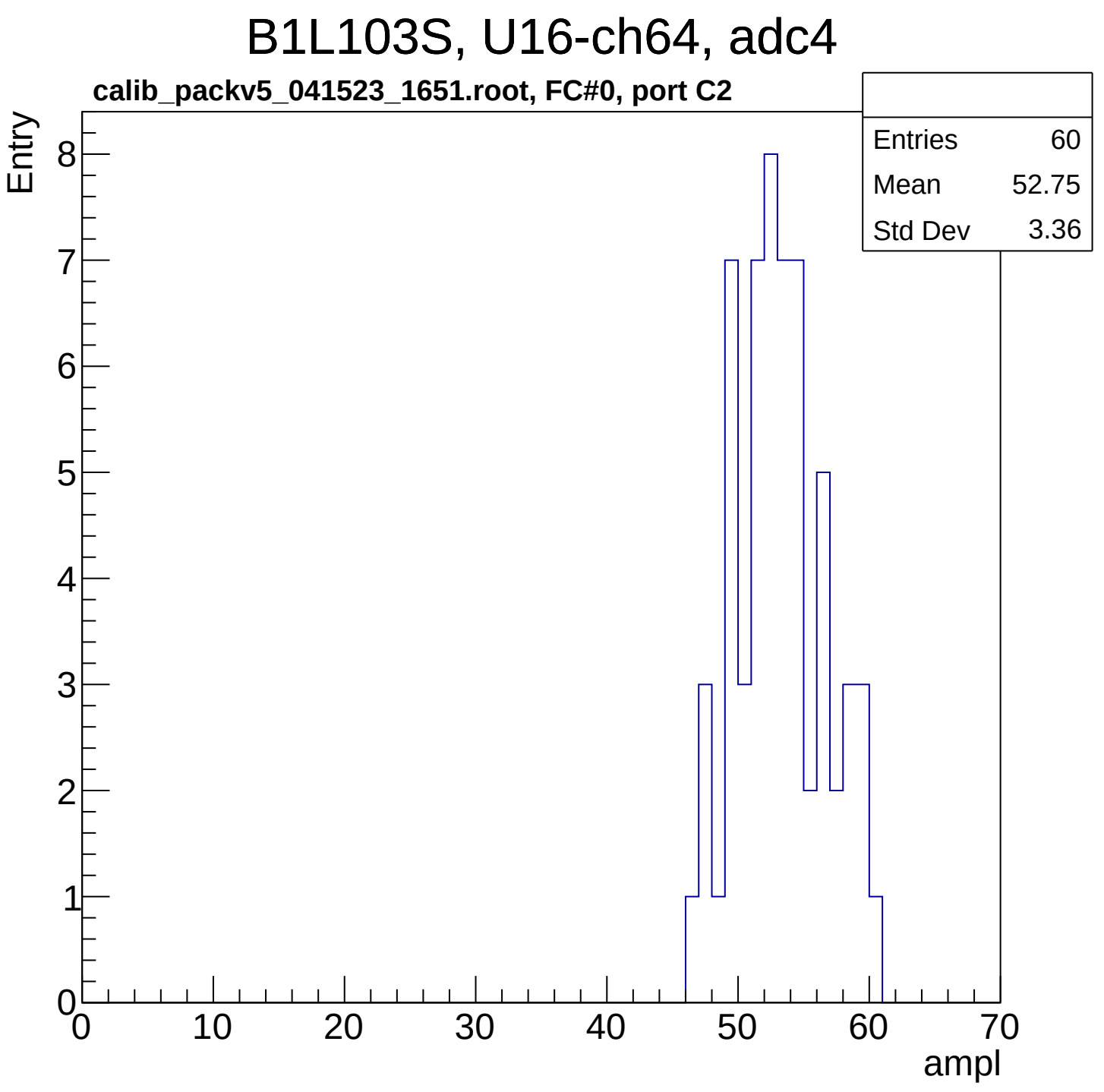
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch64, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 52.75
Std Dev 3.36
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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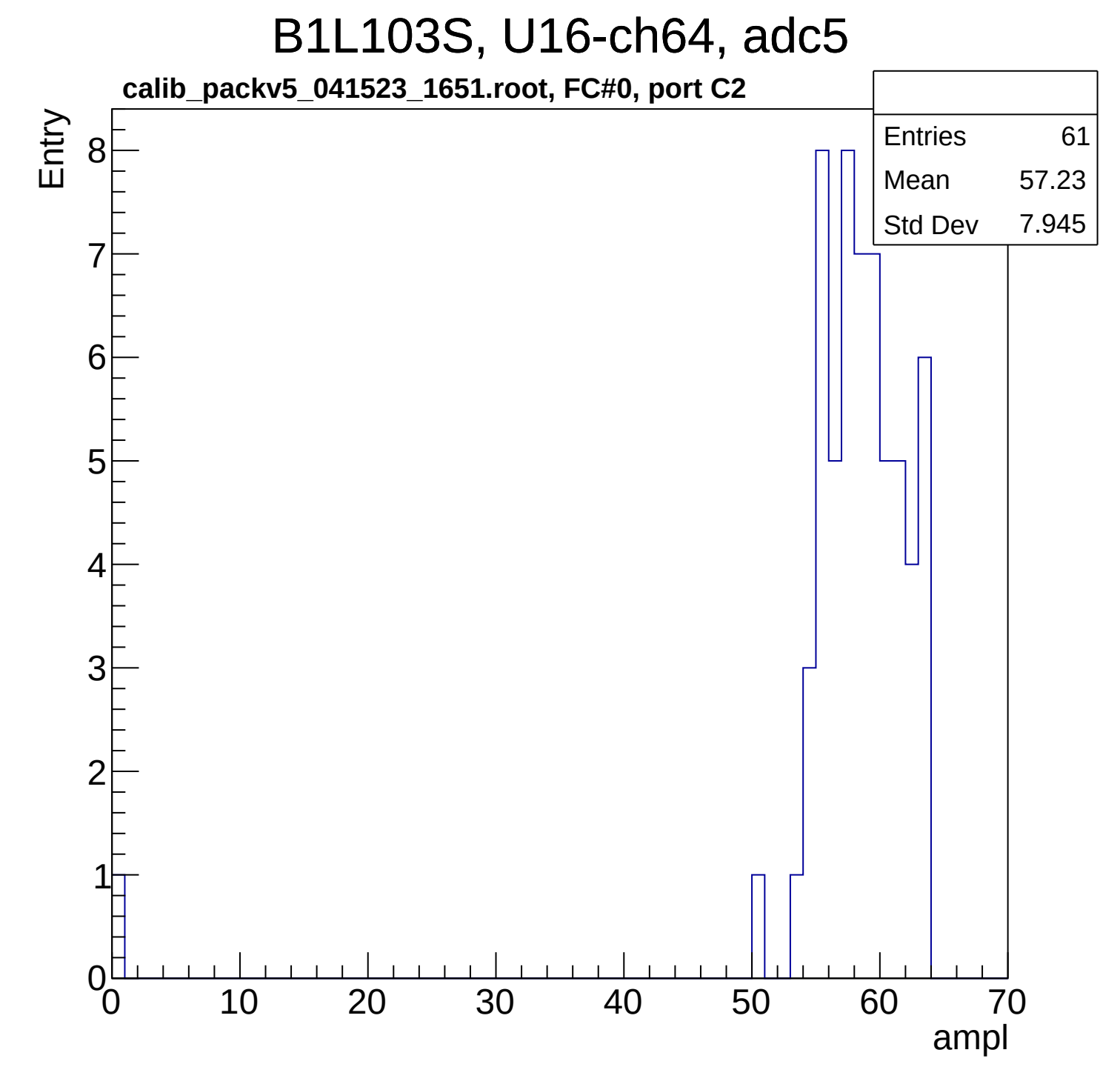
B1L103S, U16-ch64, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 57.23
Std Dev 7.945
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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40
50
60
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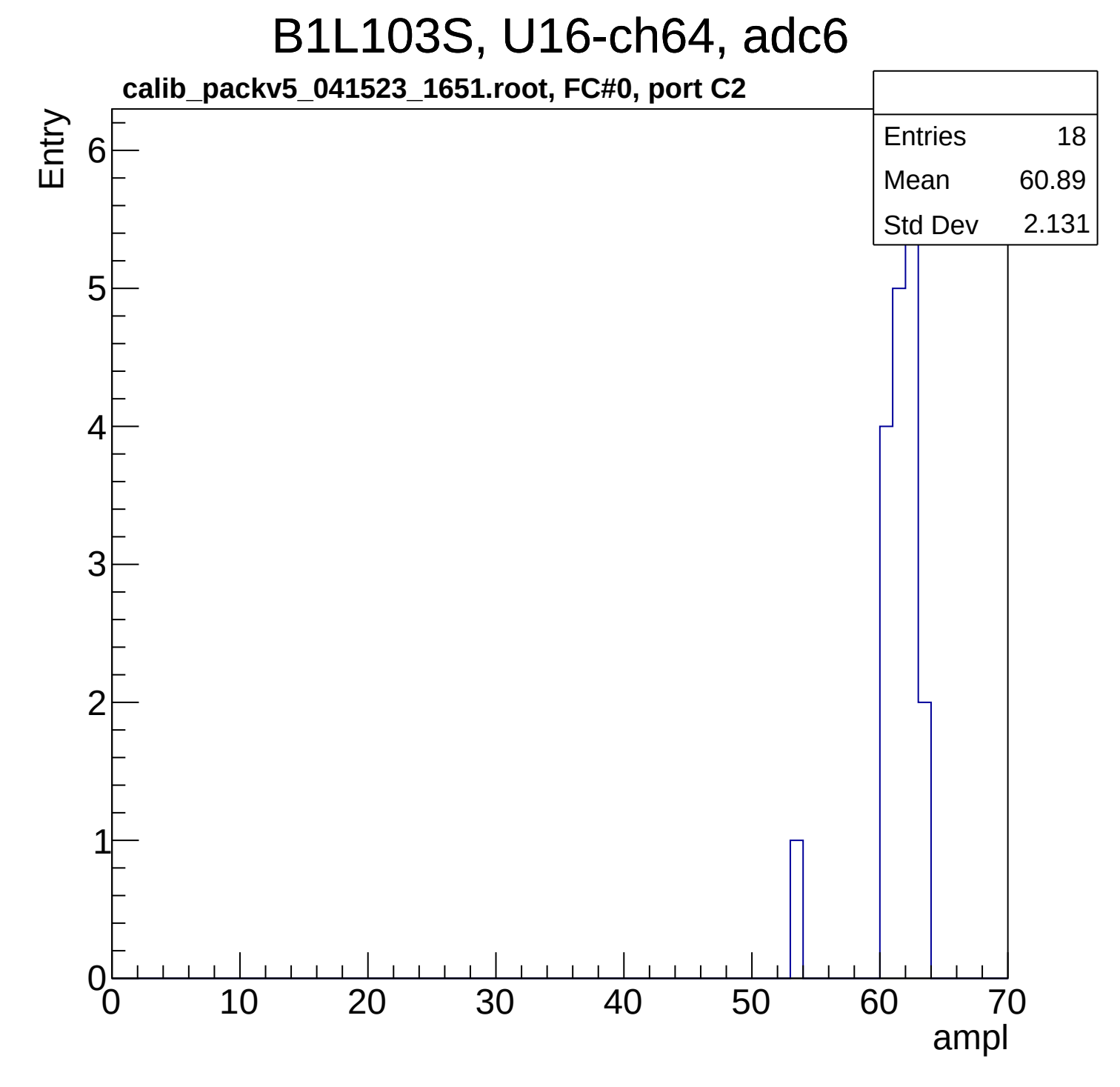
B1L103S, U16-ch64, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 60.89
Std Dev 2.131
Entry
ampl
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2
3
4
5
6
0
10
20
30
40
50
60
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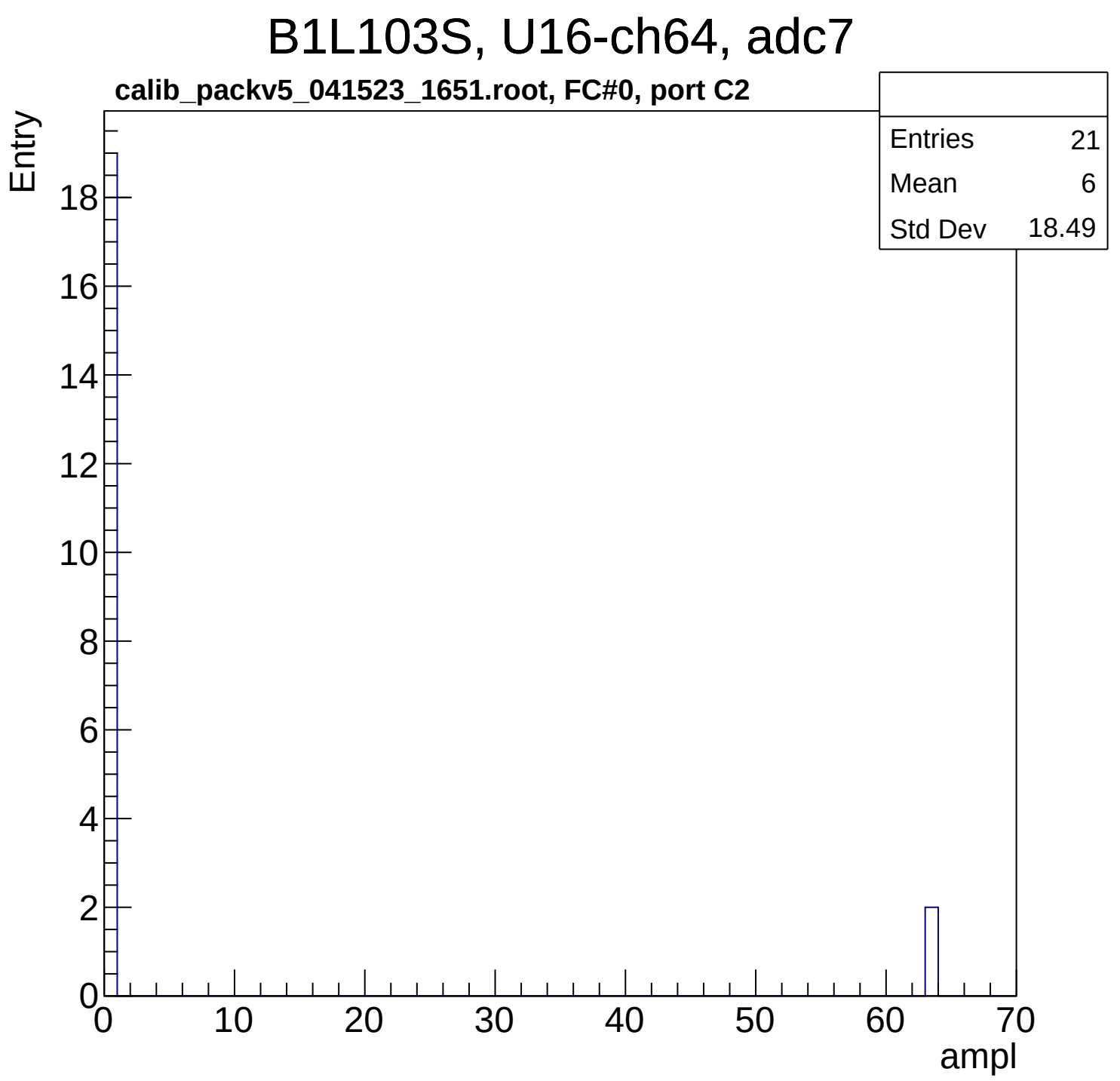
B1L103S, U16-ch64, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
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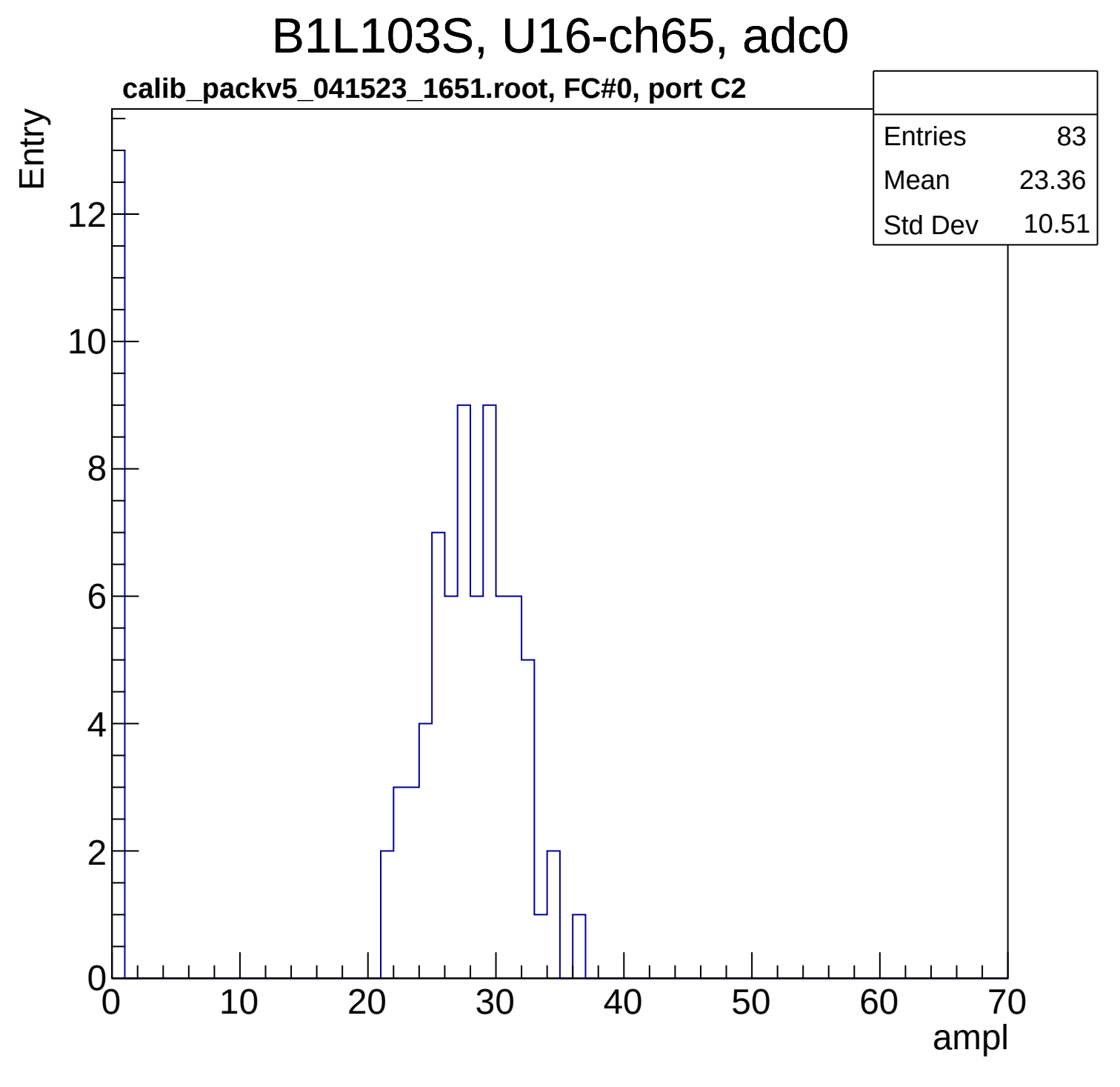
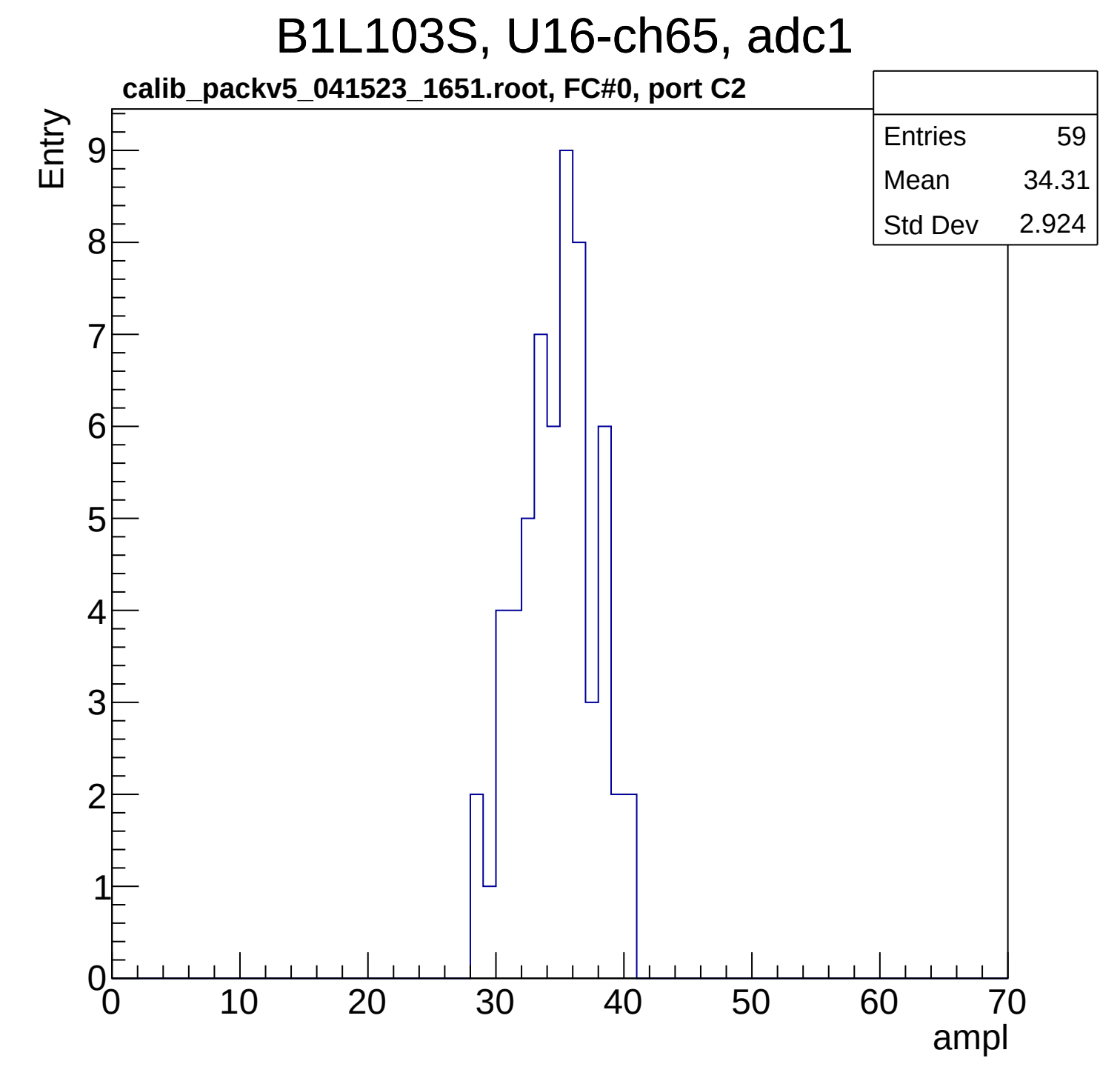
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch65, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 23.36
Std Dev 10.51
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch65, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 34.31
Std Dev 2.924
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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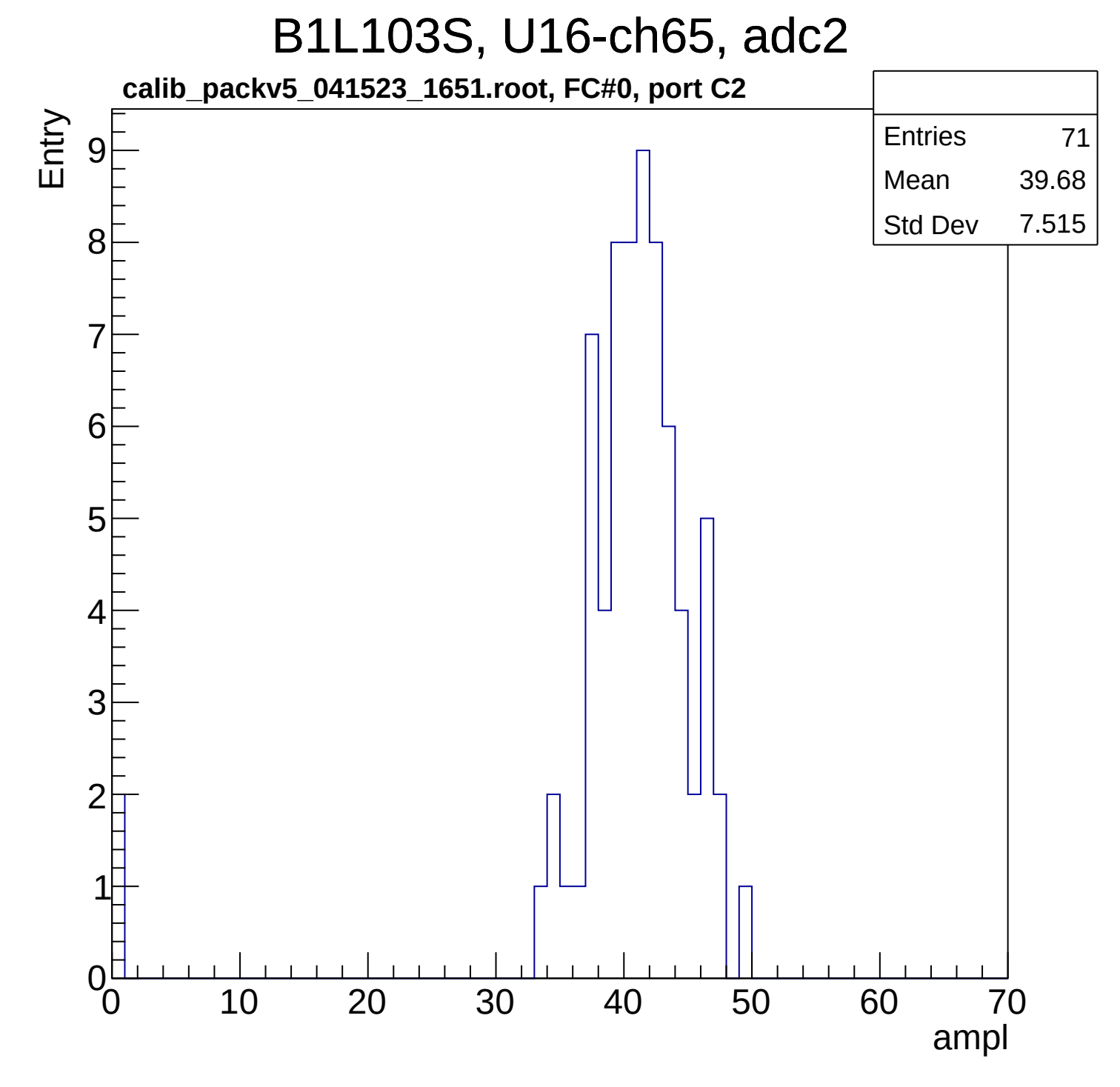
B1L103S, U16-ch65, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 39.68
Std Dev 7.515
Entry
ampl
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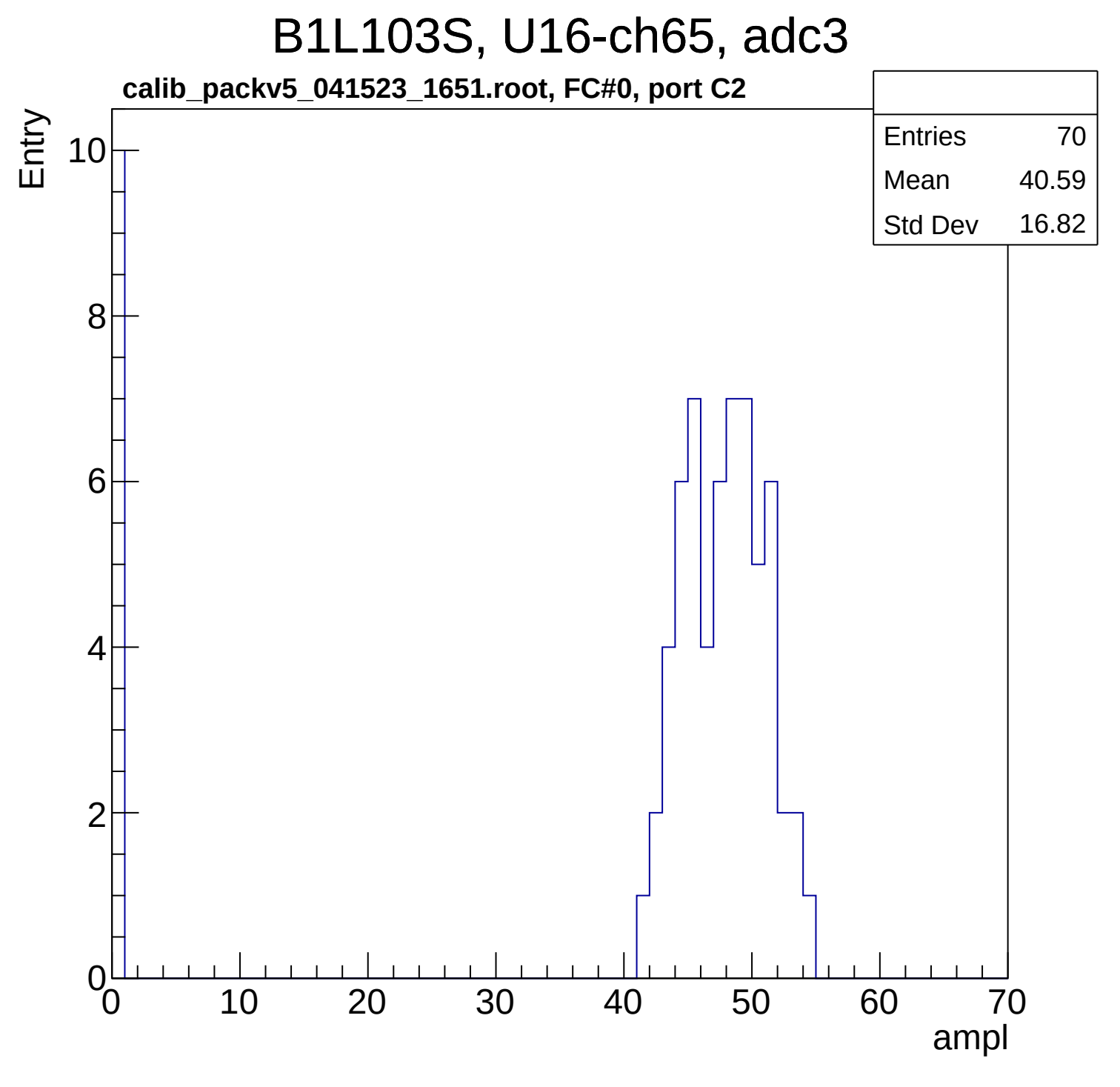
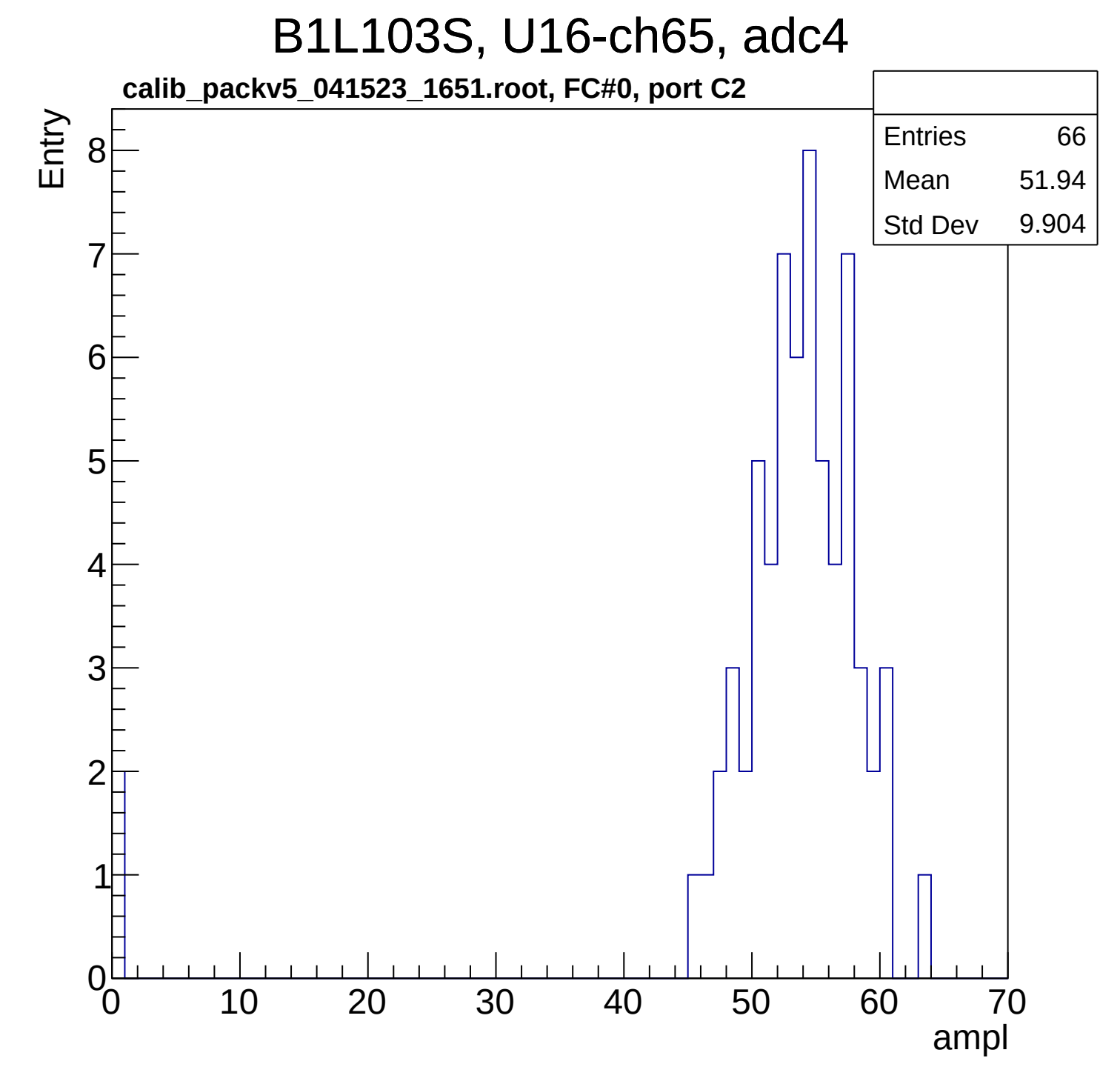
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch65, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 40.59
Std Dev 16.82
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch65, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 51.94
Std Dev 9.904
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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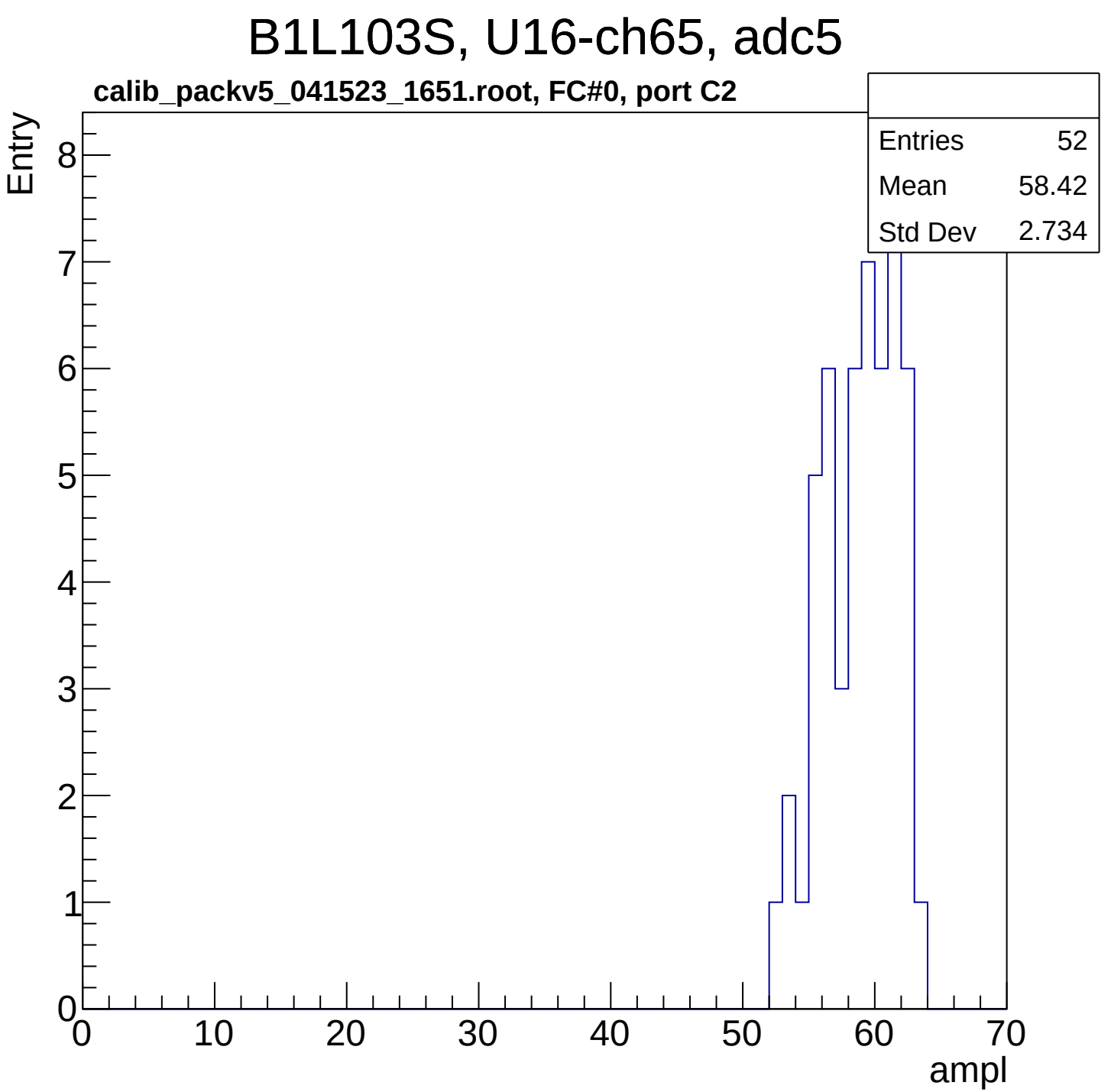
B1L103S, U16-ch65, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.42
Std Dev 2.734
Entry
ampl
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2
3
4
5
6
7
8
0
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20
30
40
50
60
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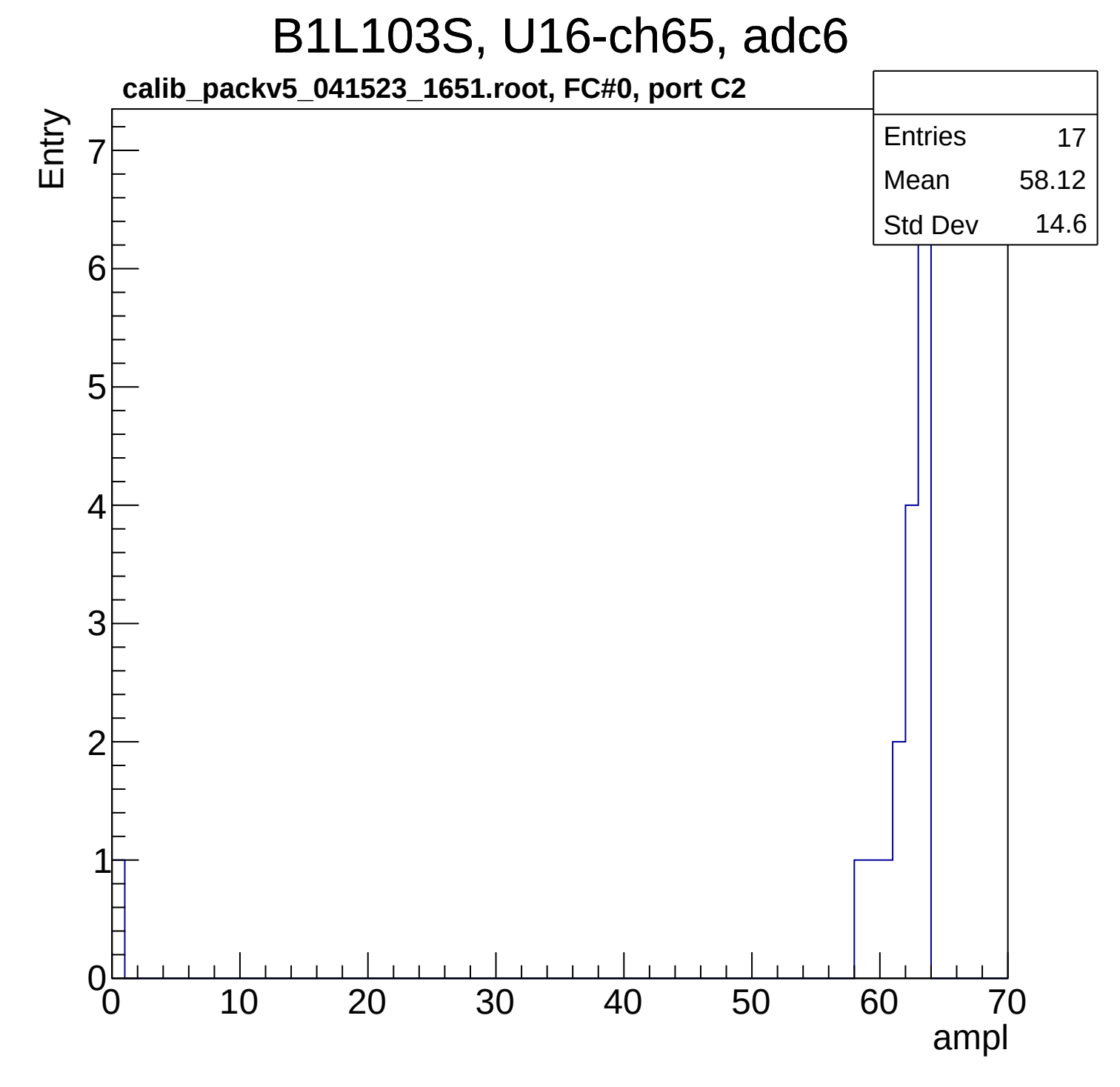
B1L103S, U16-ch65, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 58.12
Std Dev 14.6
Entry
ampl
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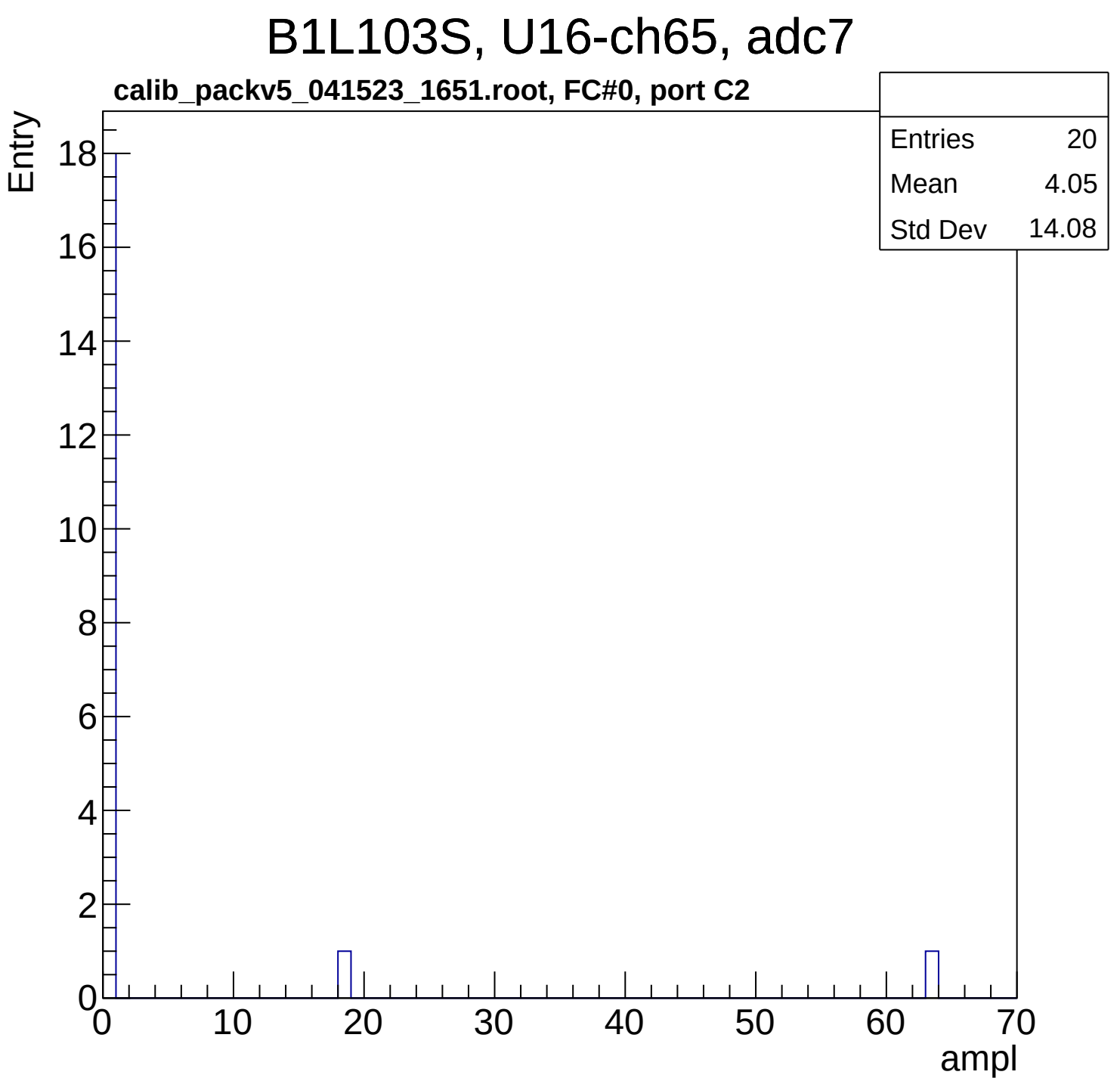
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch65, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.05
Std Dev 14.08
Entry
0
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6
8
10
12
14
16
18
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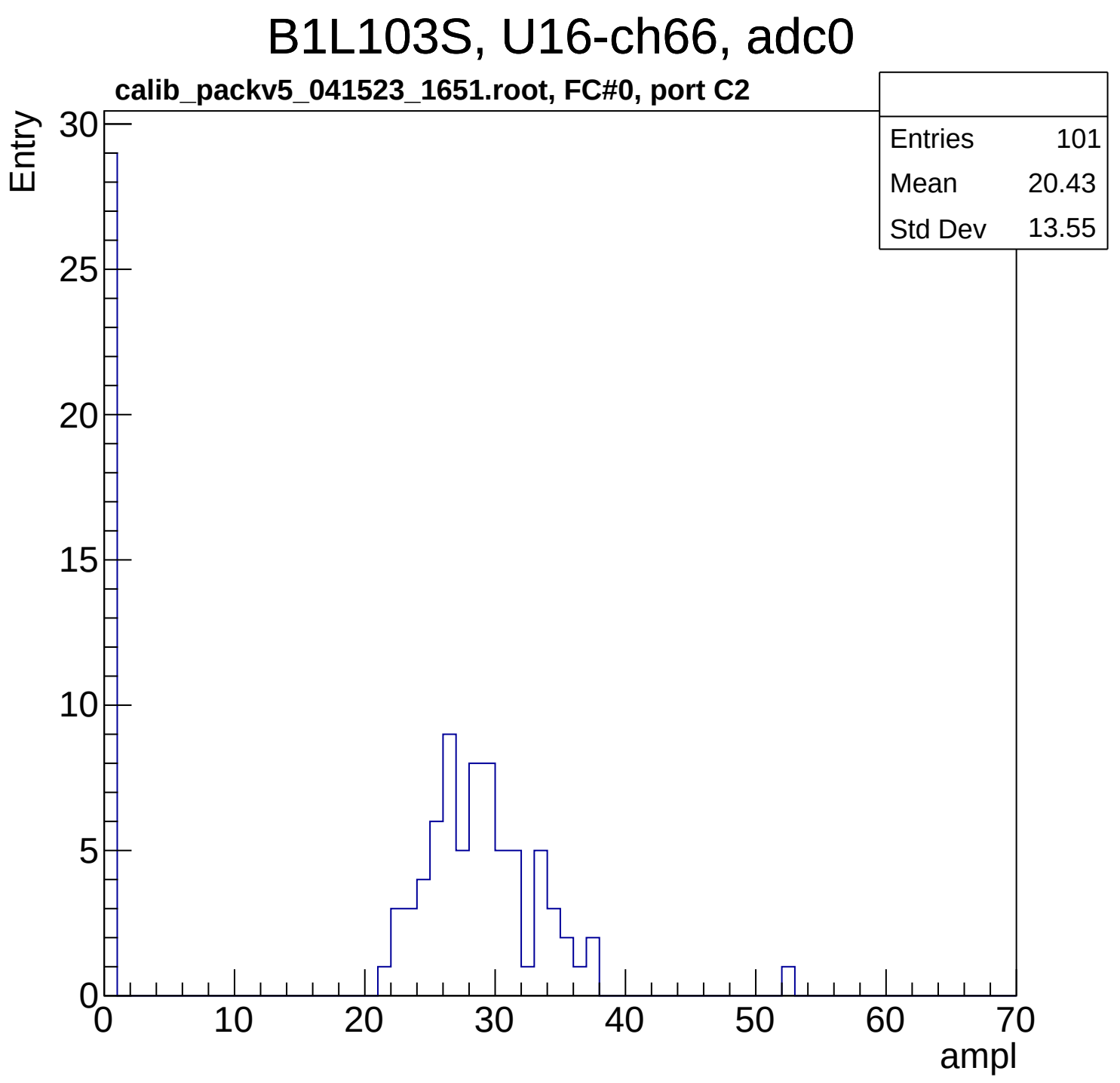
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch66, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 20.43
Std Dev 13.55
Entry
ampl
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5
10
15
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25
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0
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20
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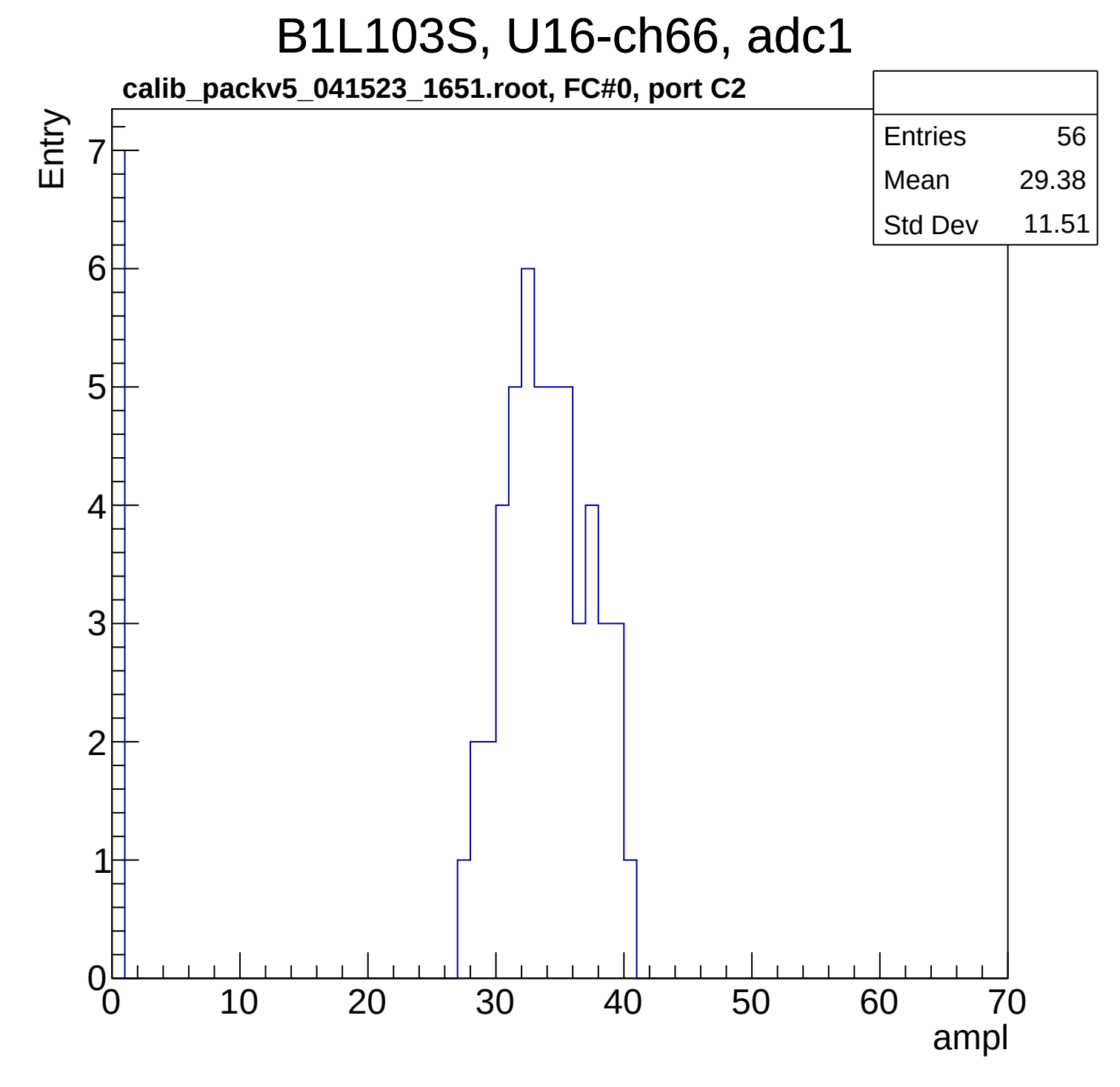
40
50
60
70


B1L103S, U16-ch66, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 29.38
Std Dev 11.51
Entry
ampl
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4
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6
7
0
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20
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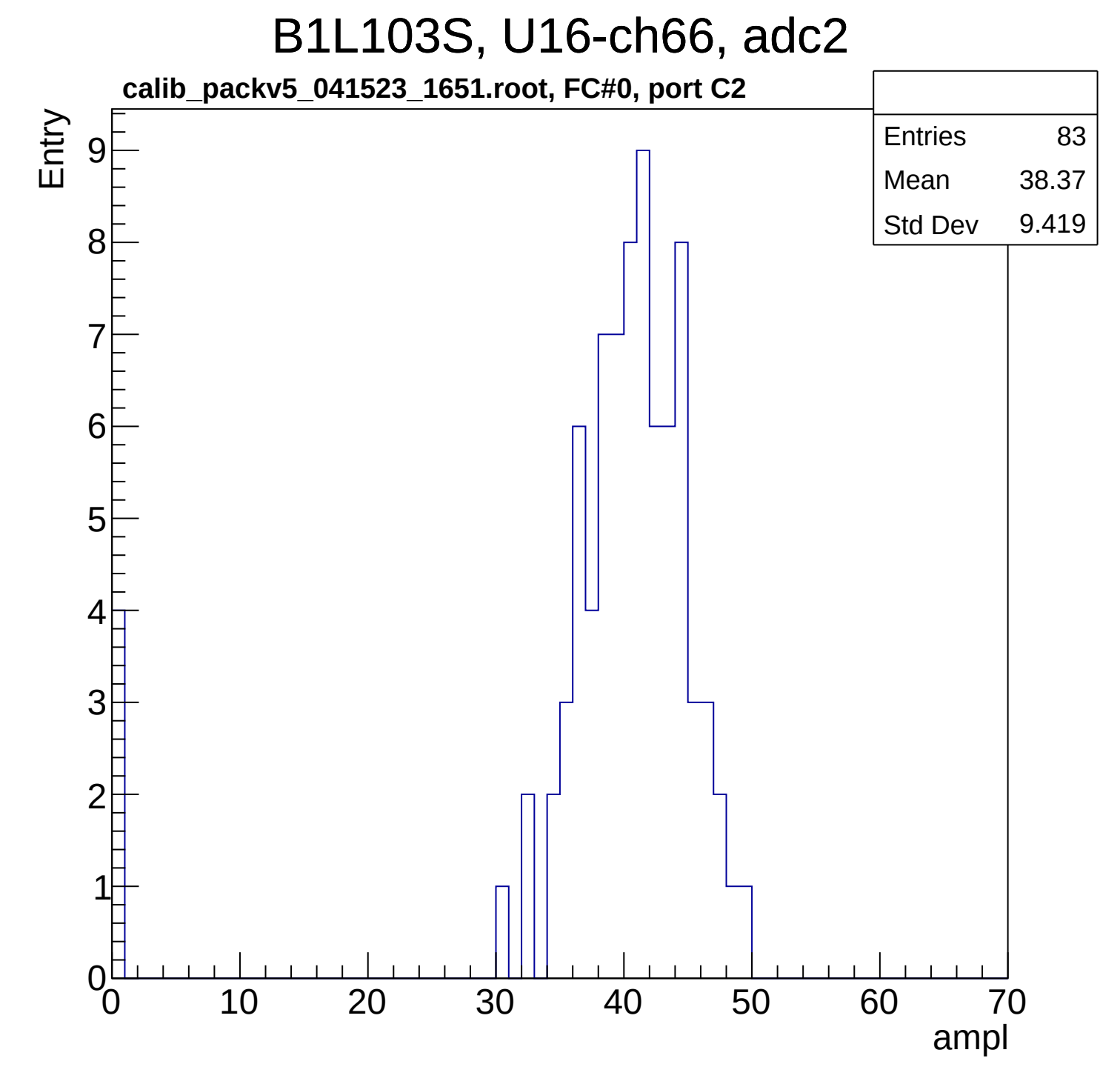
40
50
60
70


B1L103S, U16-ch66, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 38.37
Std Dev 9.419
Entry
ampl
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4
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6
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0
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60
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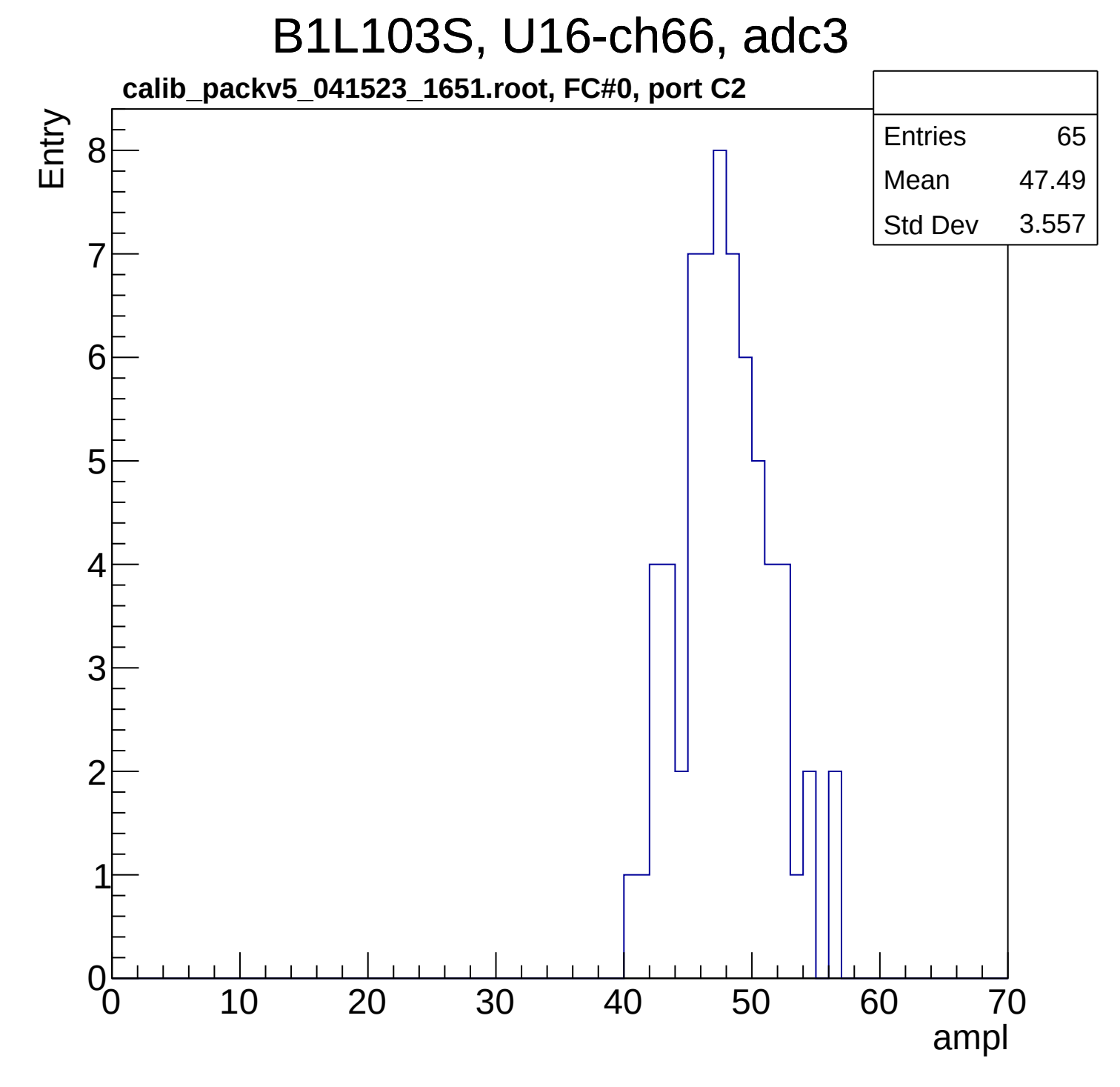
B1L103S, U16-ch66, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 47.49
Std Dev 3.557
Entry
ampl
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0
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20
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40
50
60
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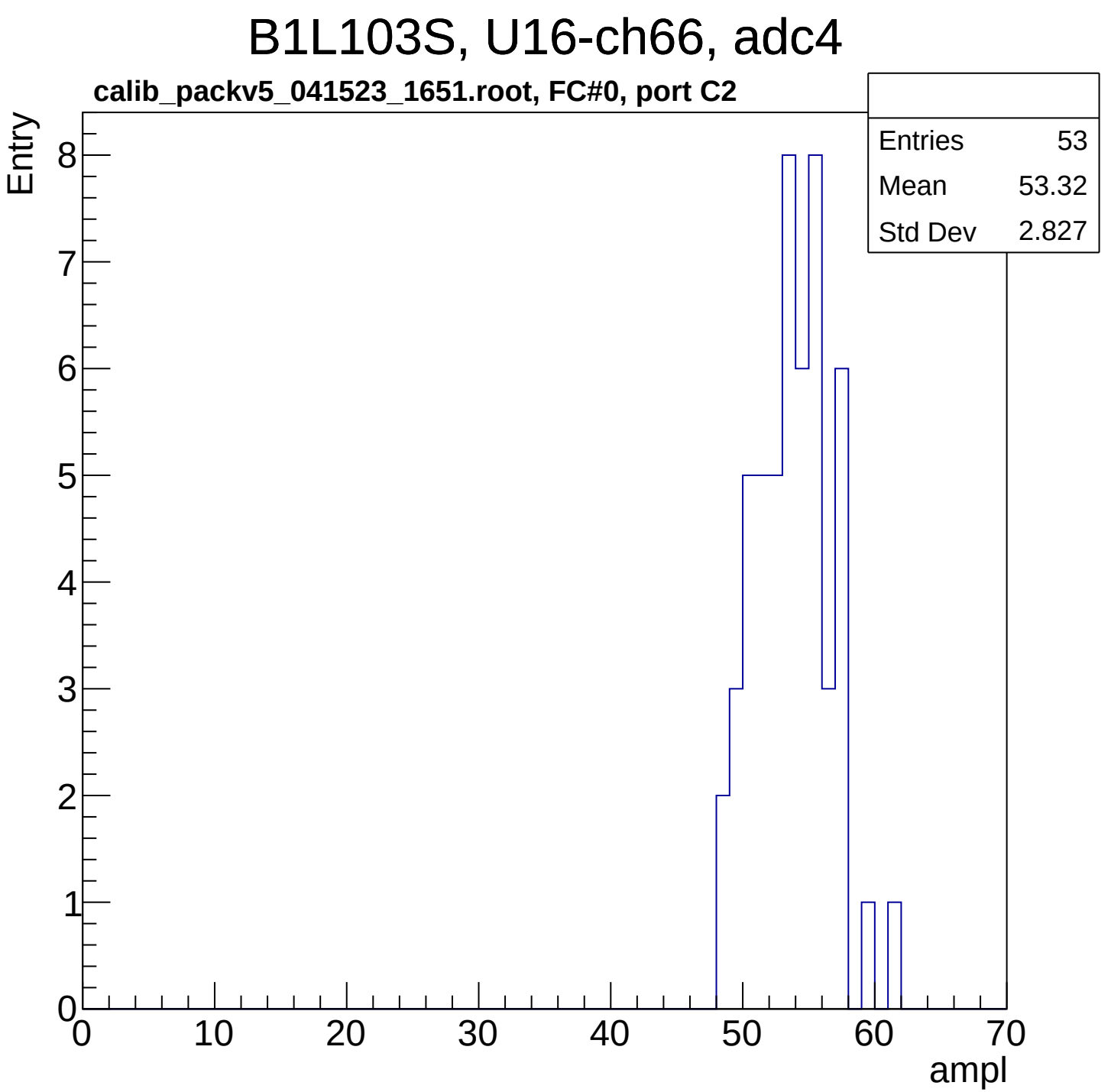
B1L103S, U16-ch66, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 53.32
Std Dev 2.827
Entry
ampl
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4
5
6
7
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0
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20
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40
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60
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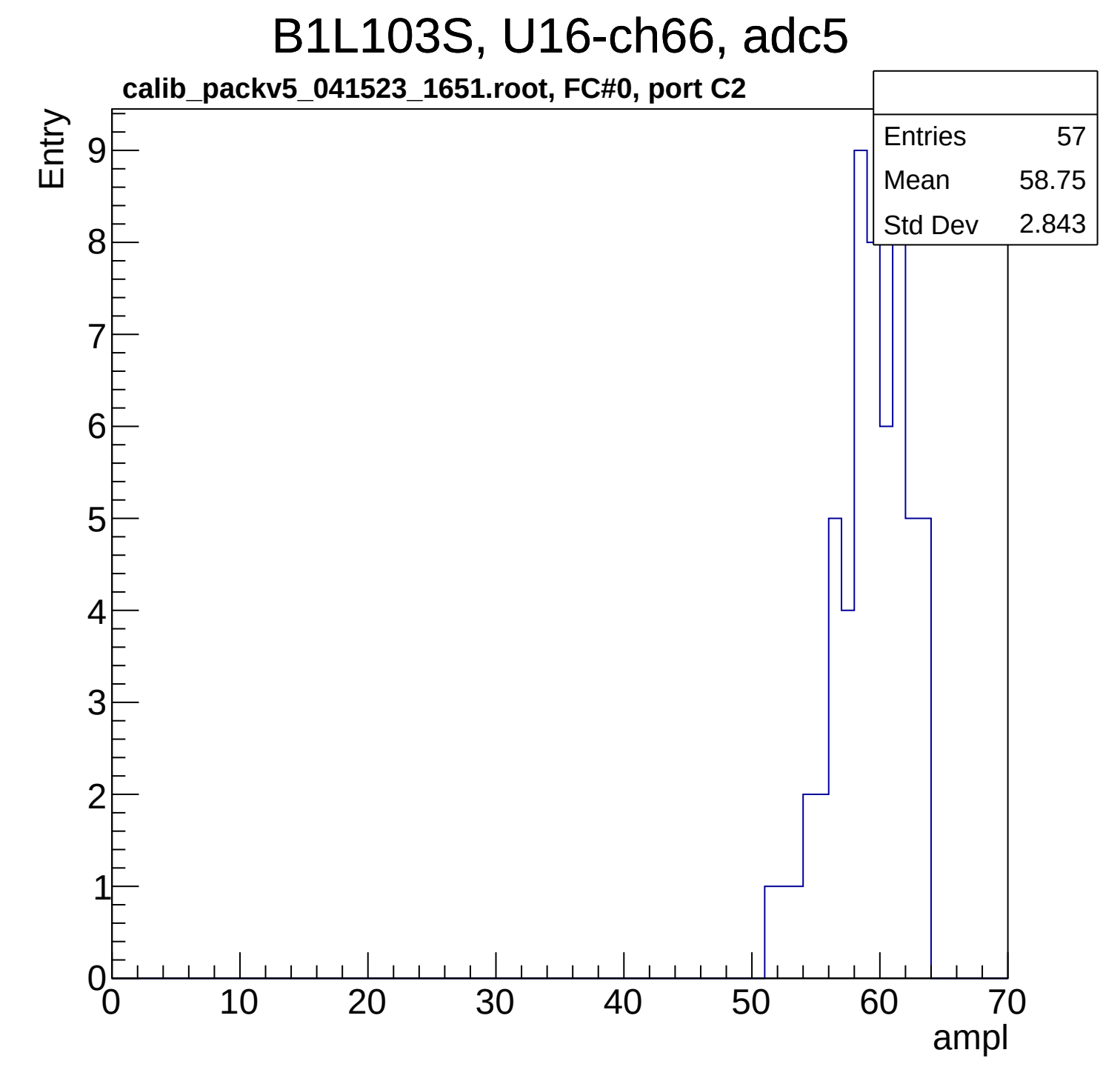
B1L103S, U16-ch66, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.75
Std Dev 2.843
Entry
ampl
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4
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6
7
8
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0
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20
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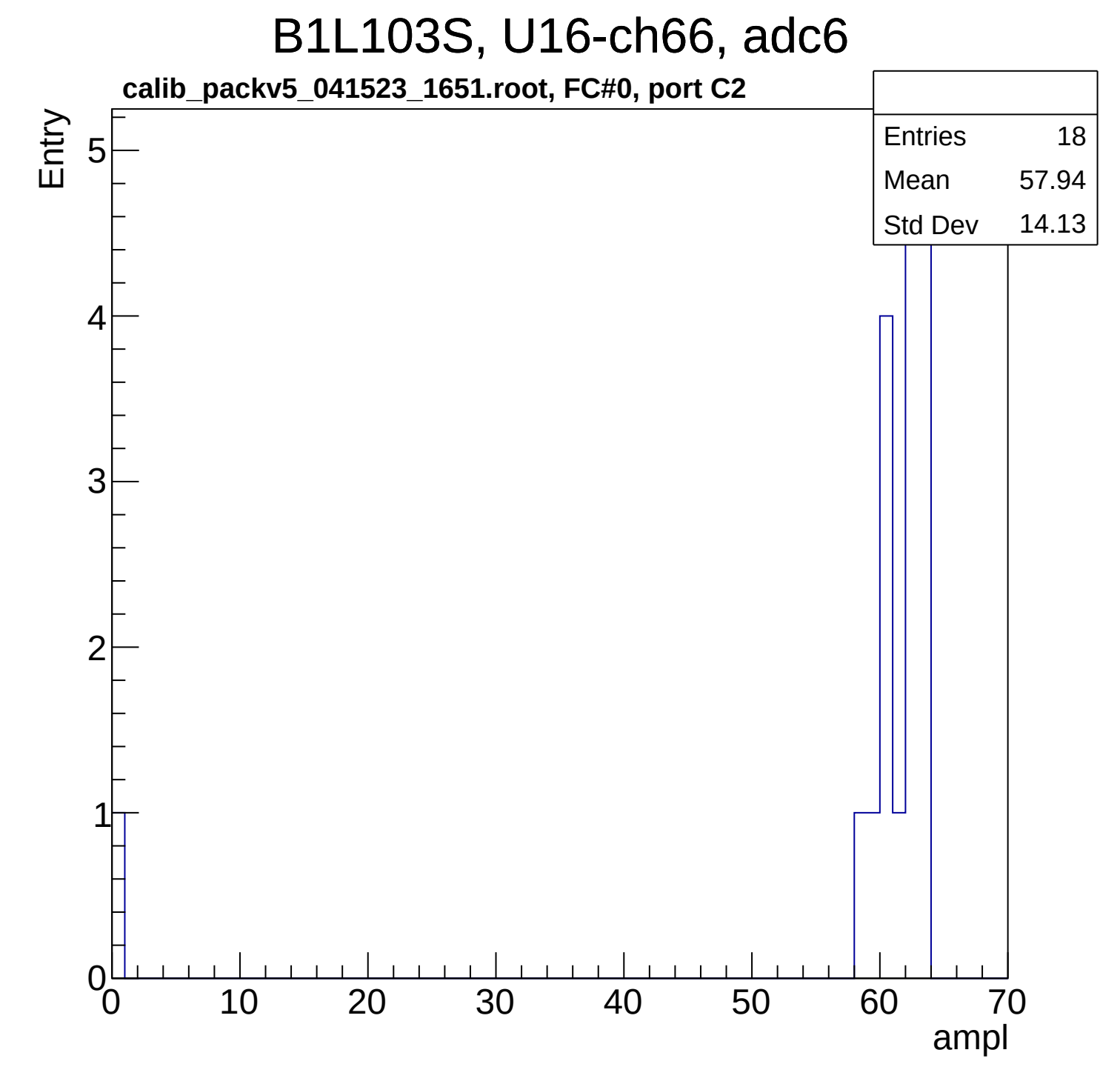
60
70


B1L103S, U16-ch66, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 57.94
Std Dev 14.13
Entry
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3
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5
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10
20
30
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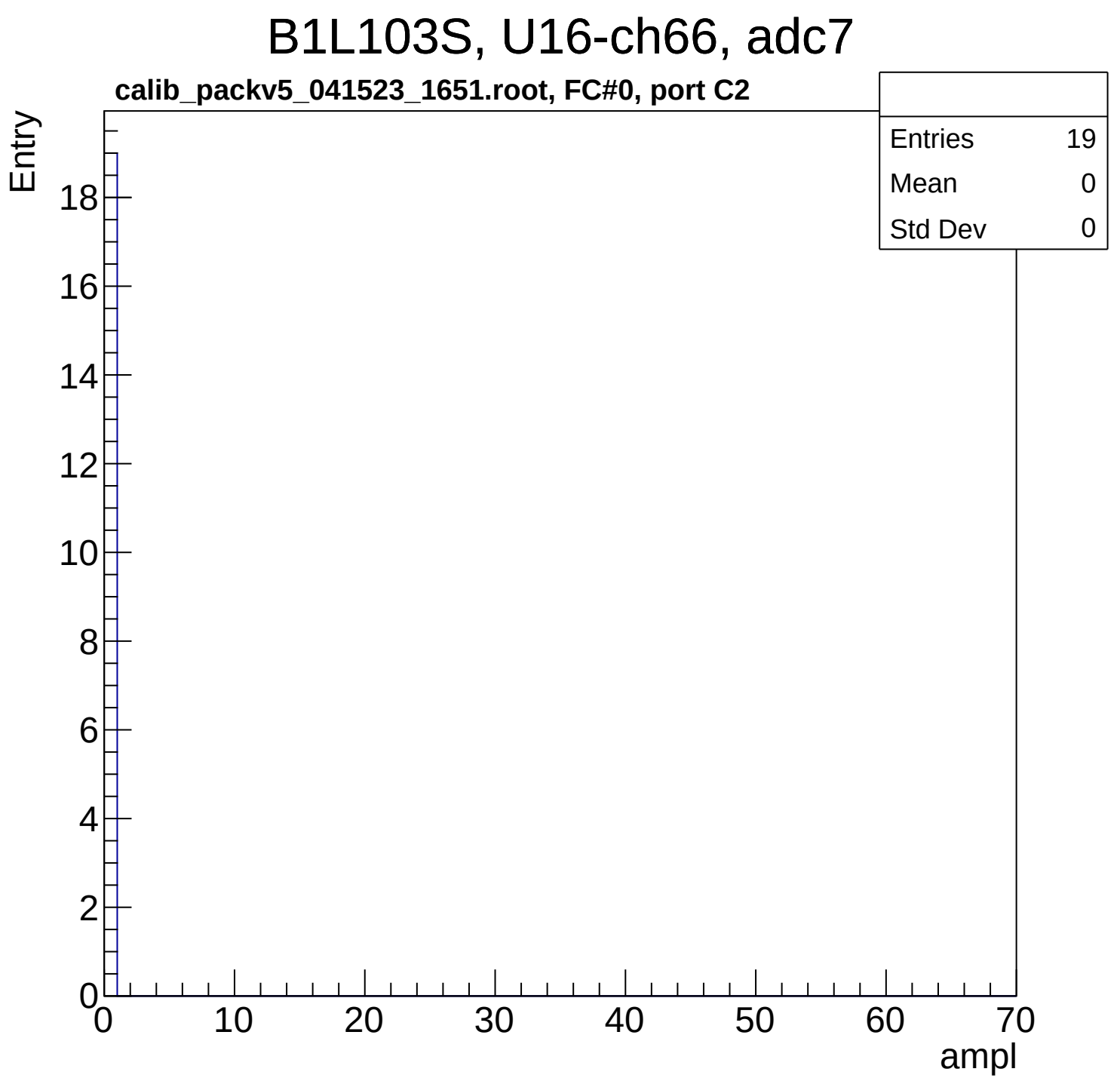
50
60
70
ampl


B1L103S, U16-ch66, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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10
20
30
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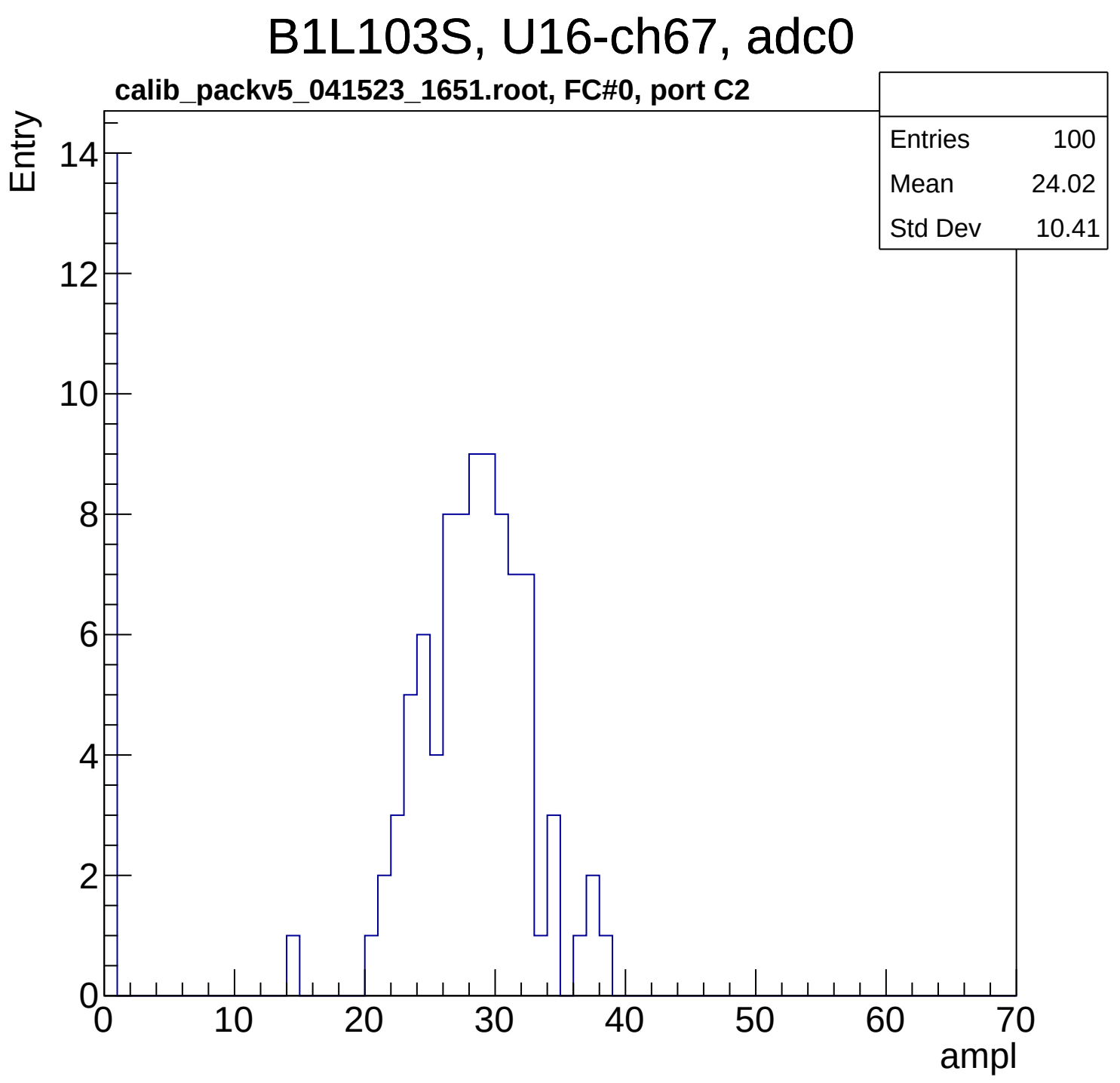
50
60
70
ampl


B1L103S, U16-ch67, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 24.02
Std Dev 10.41
Entry
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4
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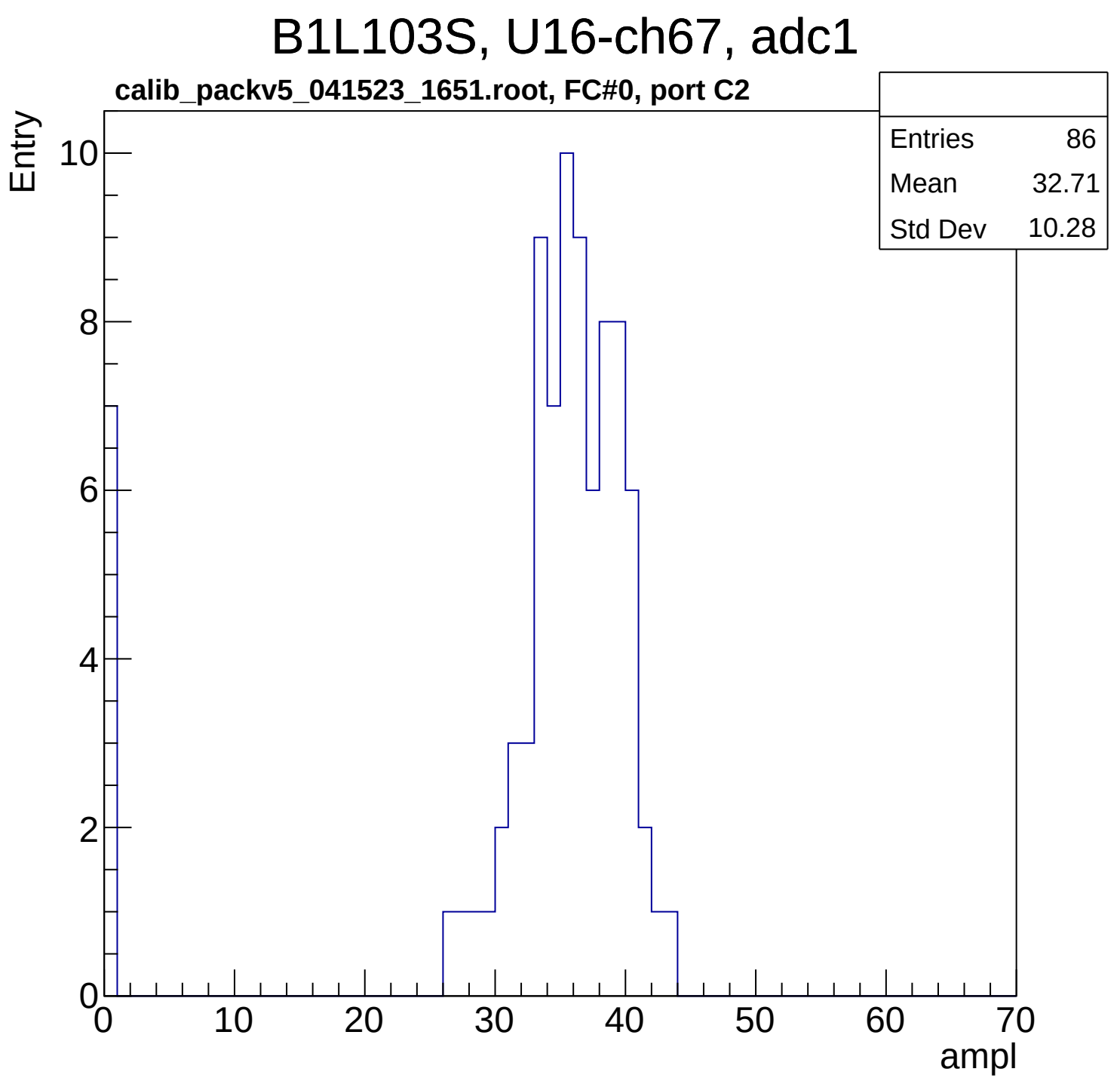
60
70
ampl


B1L103S, U16-ch67, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 32.71
Std Dev 10.28
Entry
ampl
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0
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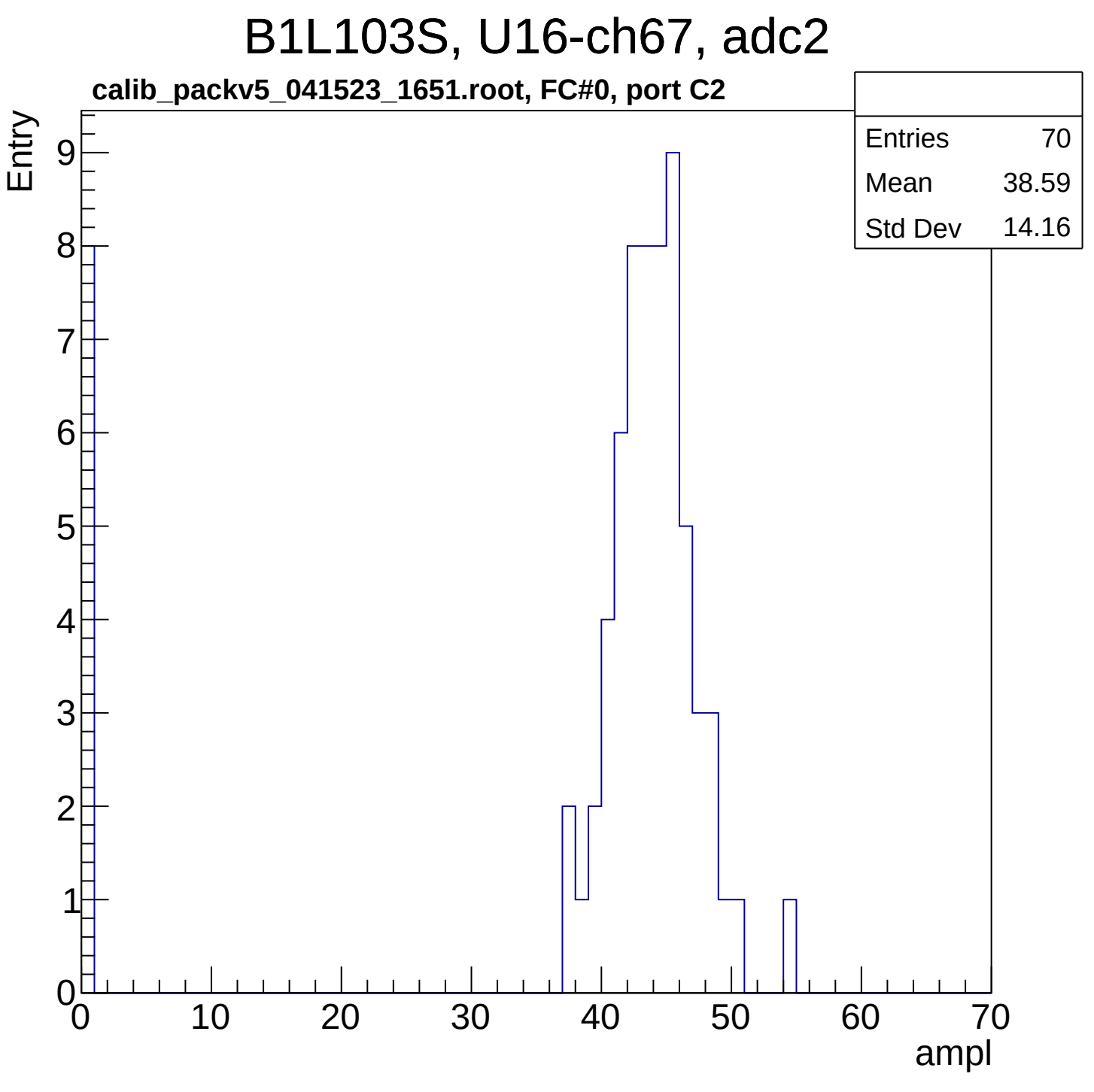
B1L103S, U16-ch67, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 38.59
Std Dev 14.16
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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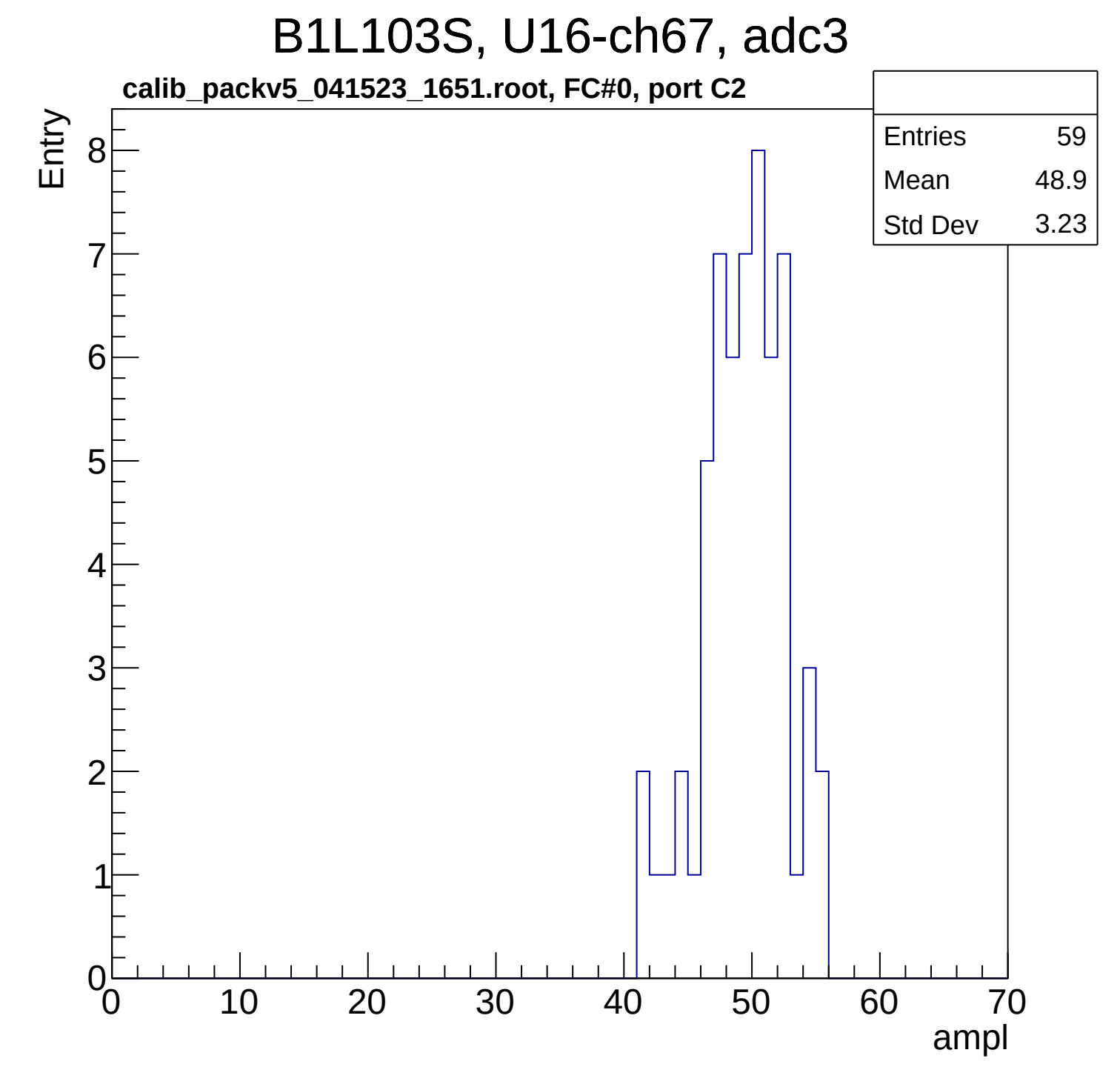
B1L103S, U16-ch67, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 48.9
Std Dev 3.23
Entry
ampl
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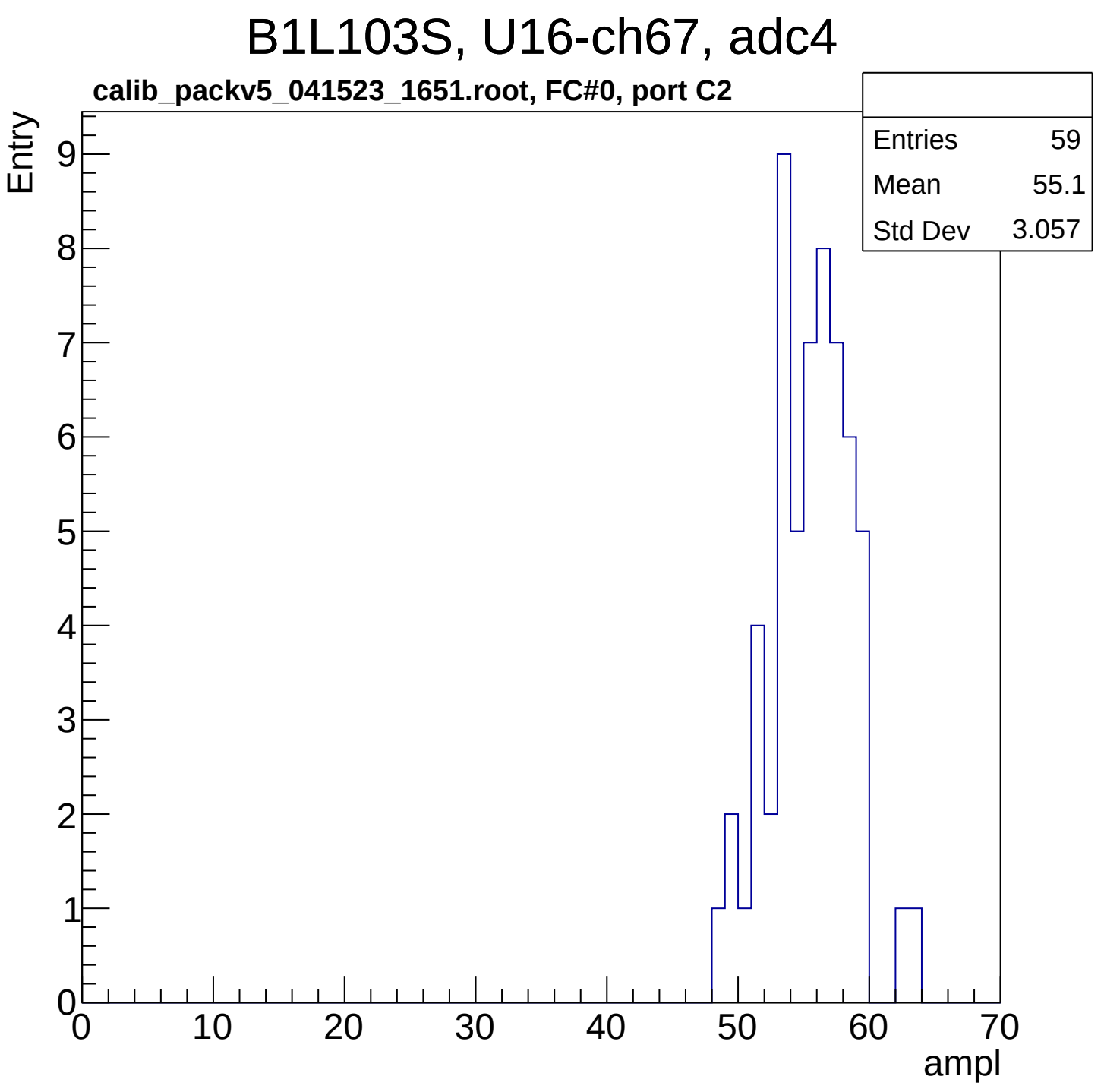
B1L103S, U16-ch67, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 55.1
Std Dev 3.057
Entry
ampl
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5
6
7
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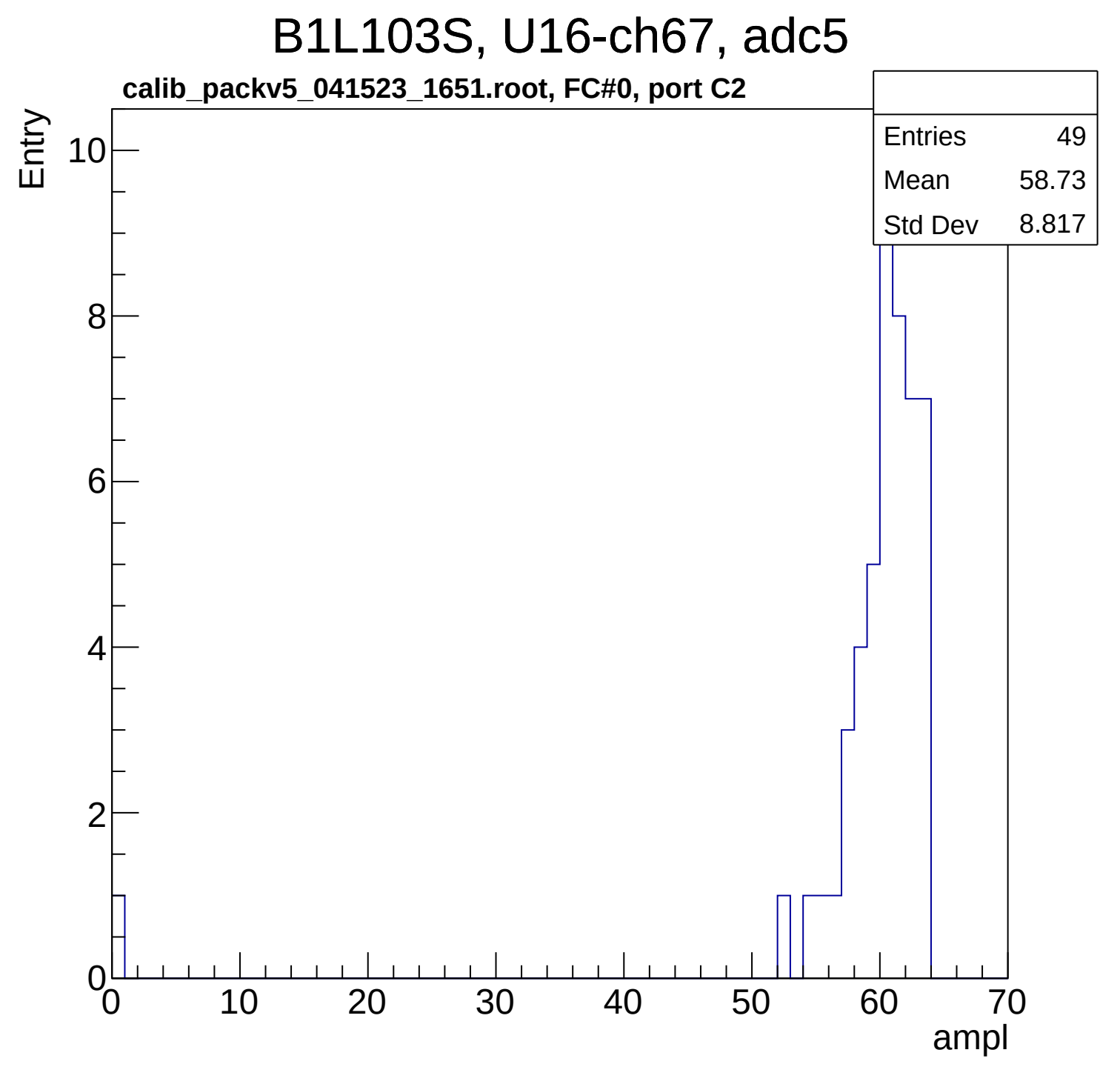
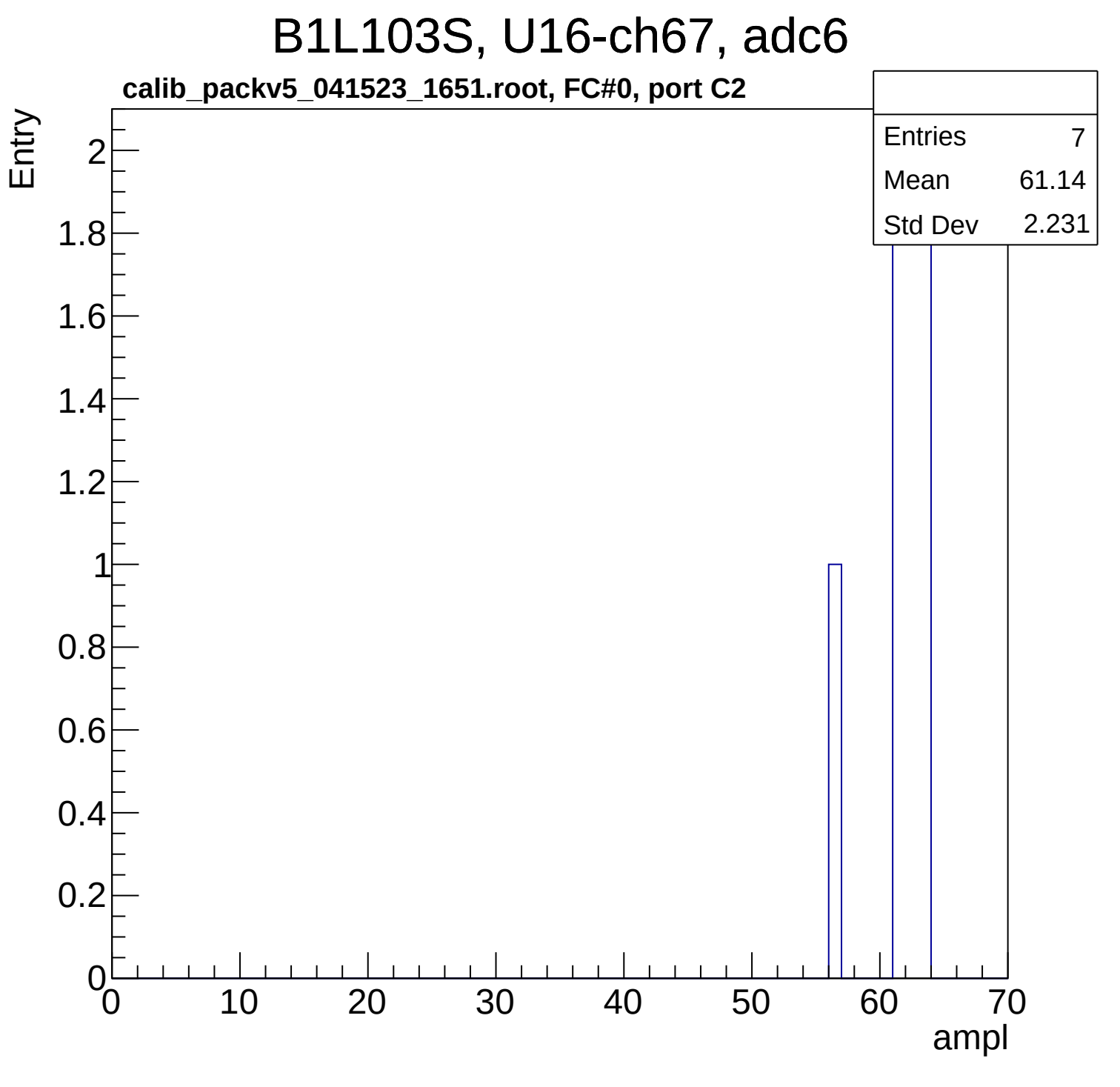
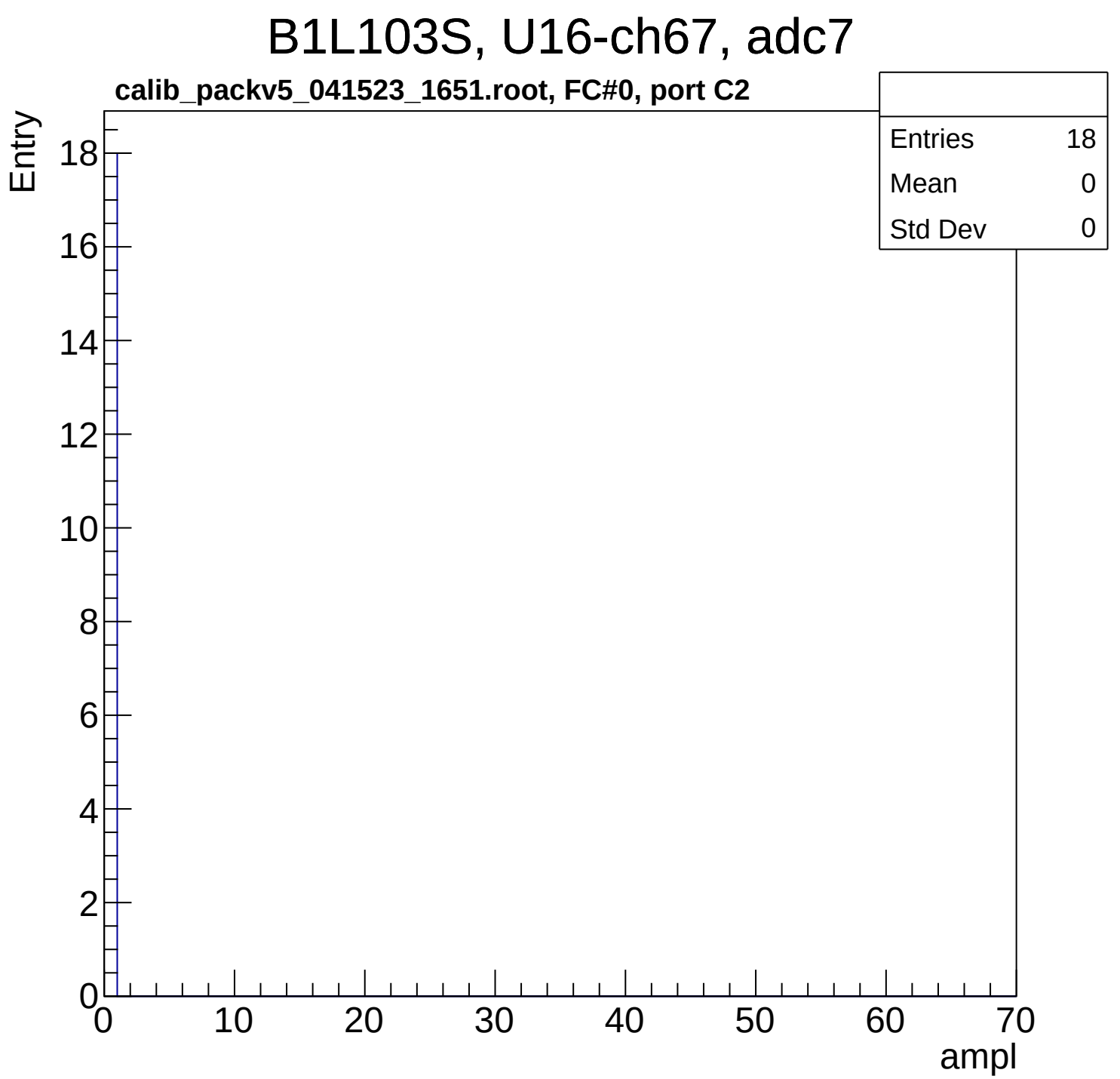
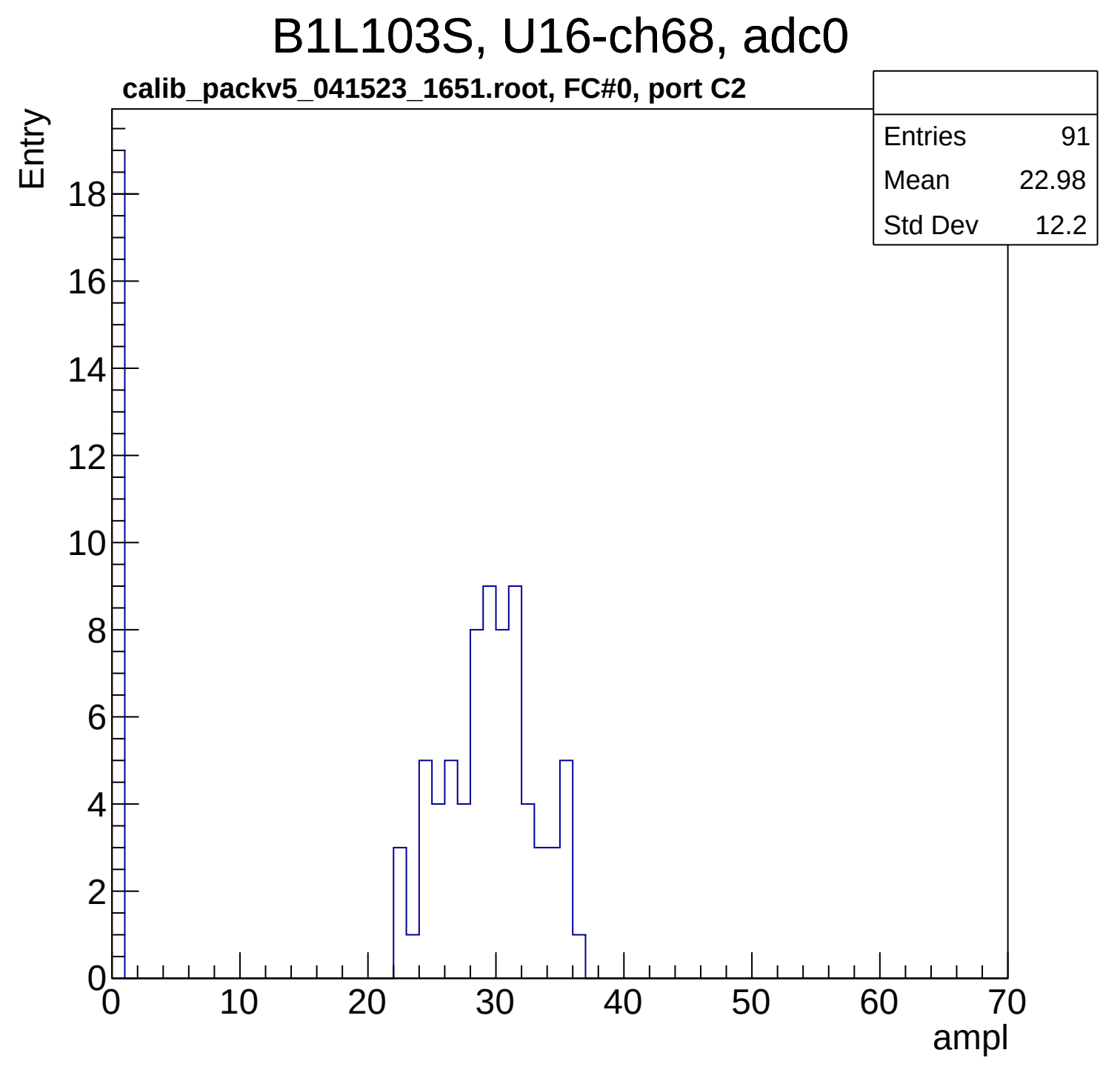
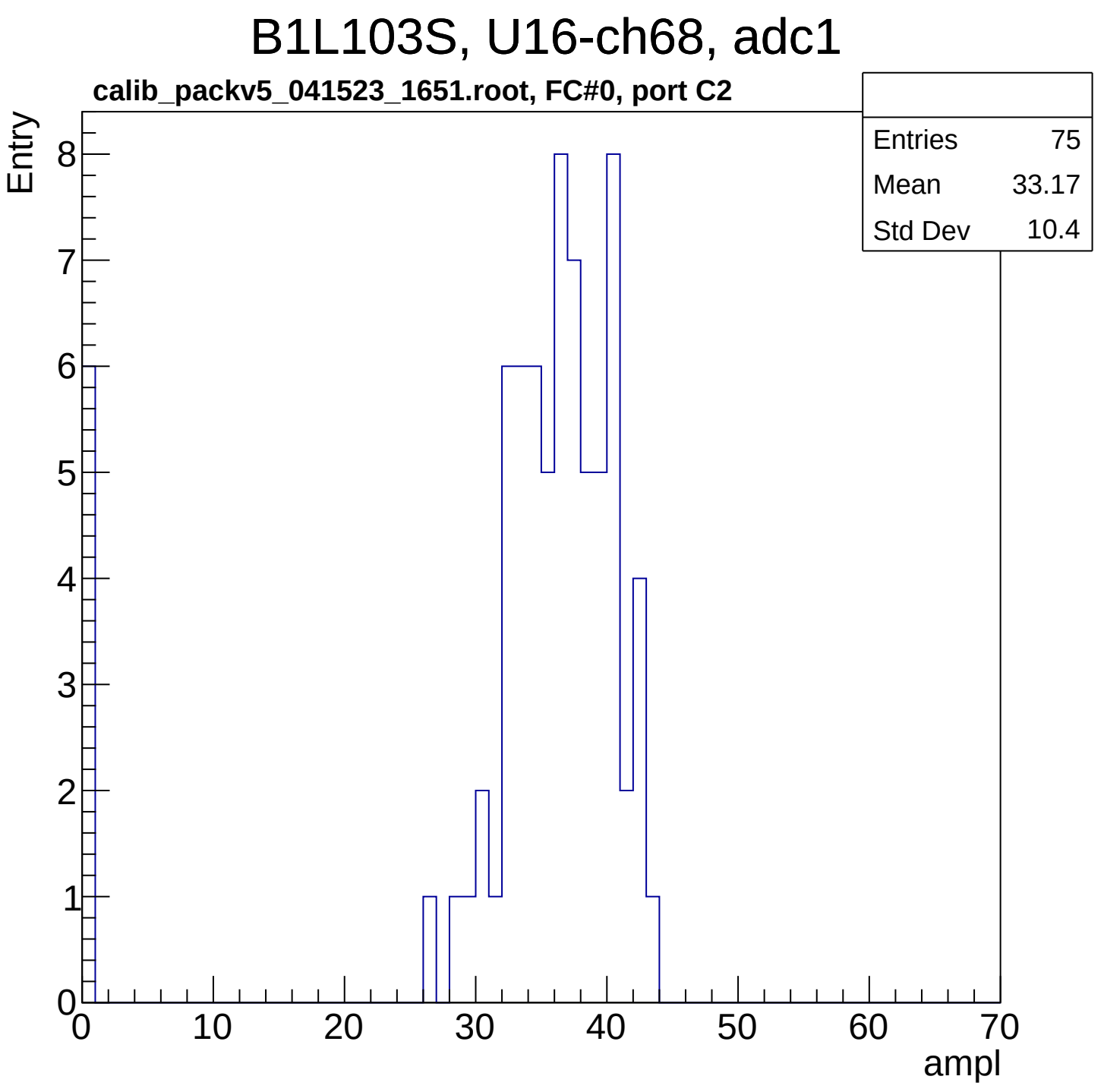
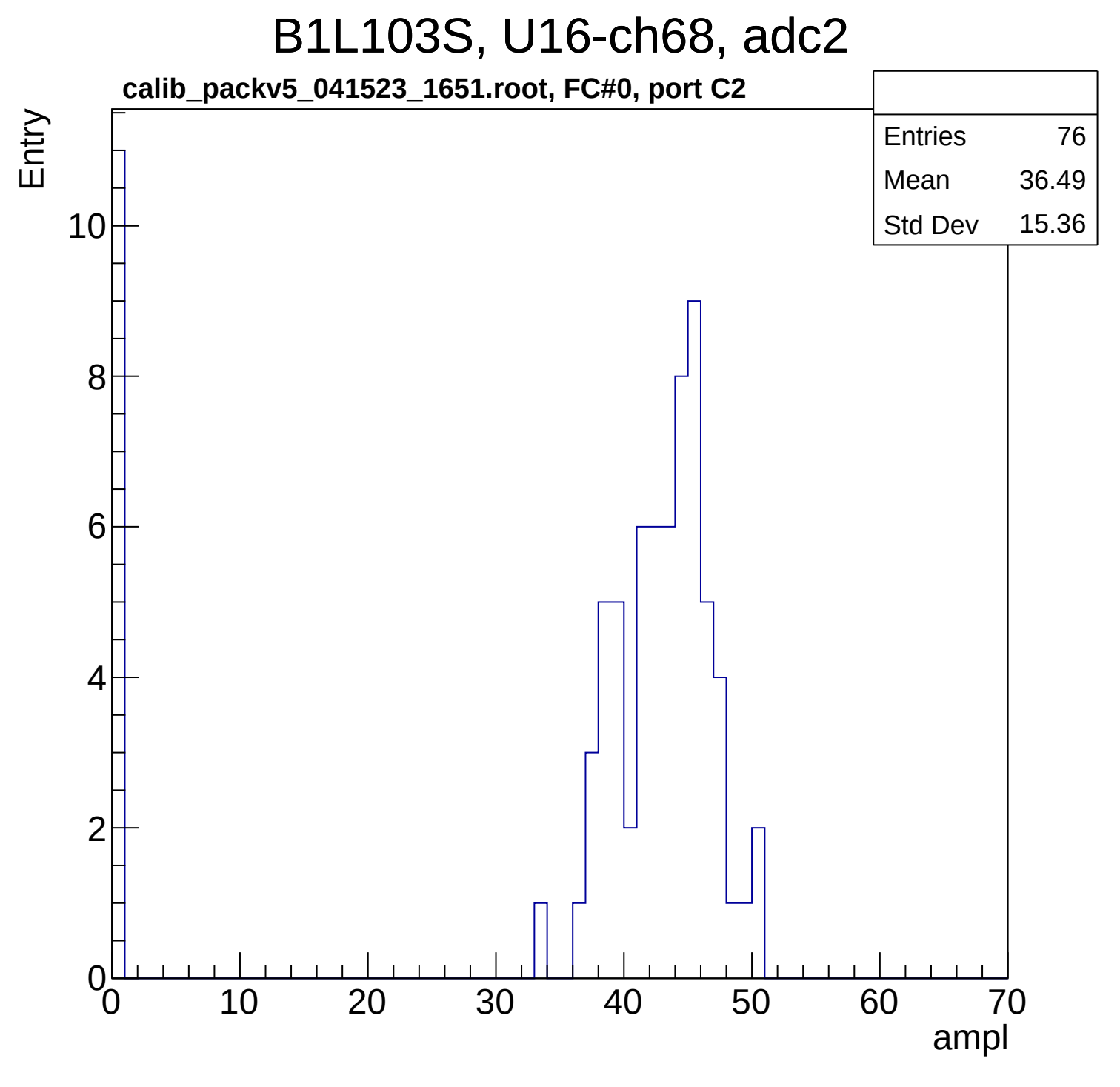

B1L103S, U16-ch67, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.73
Std Dev 8.817
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

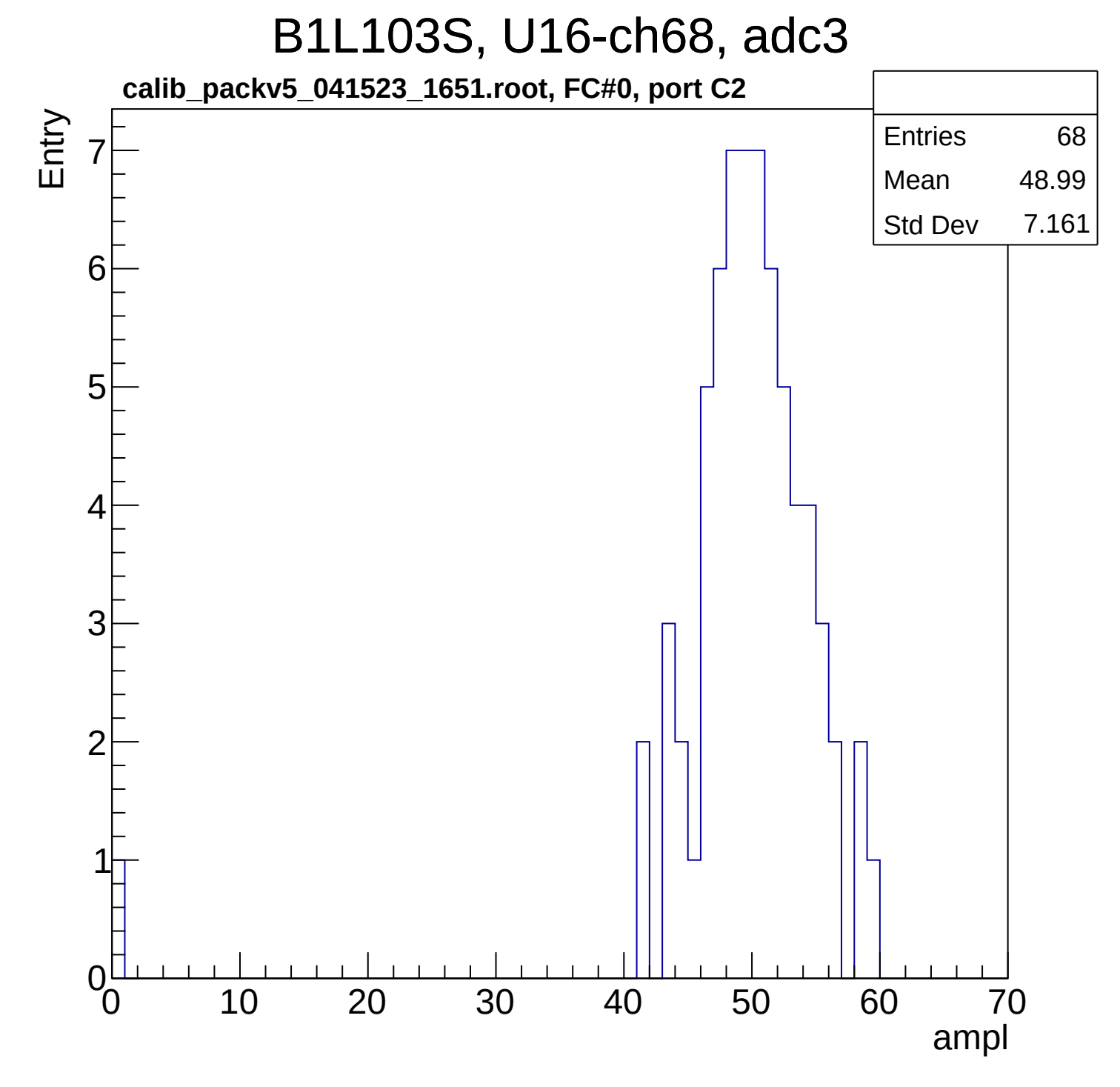

B1L103S, U16-ch67, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.14
Std Dev 2.231
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

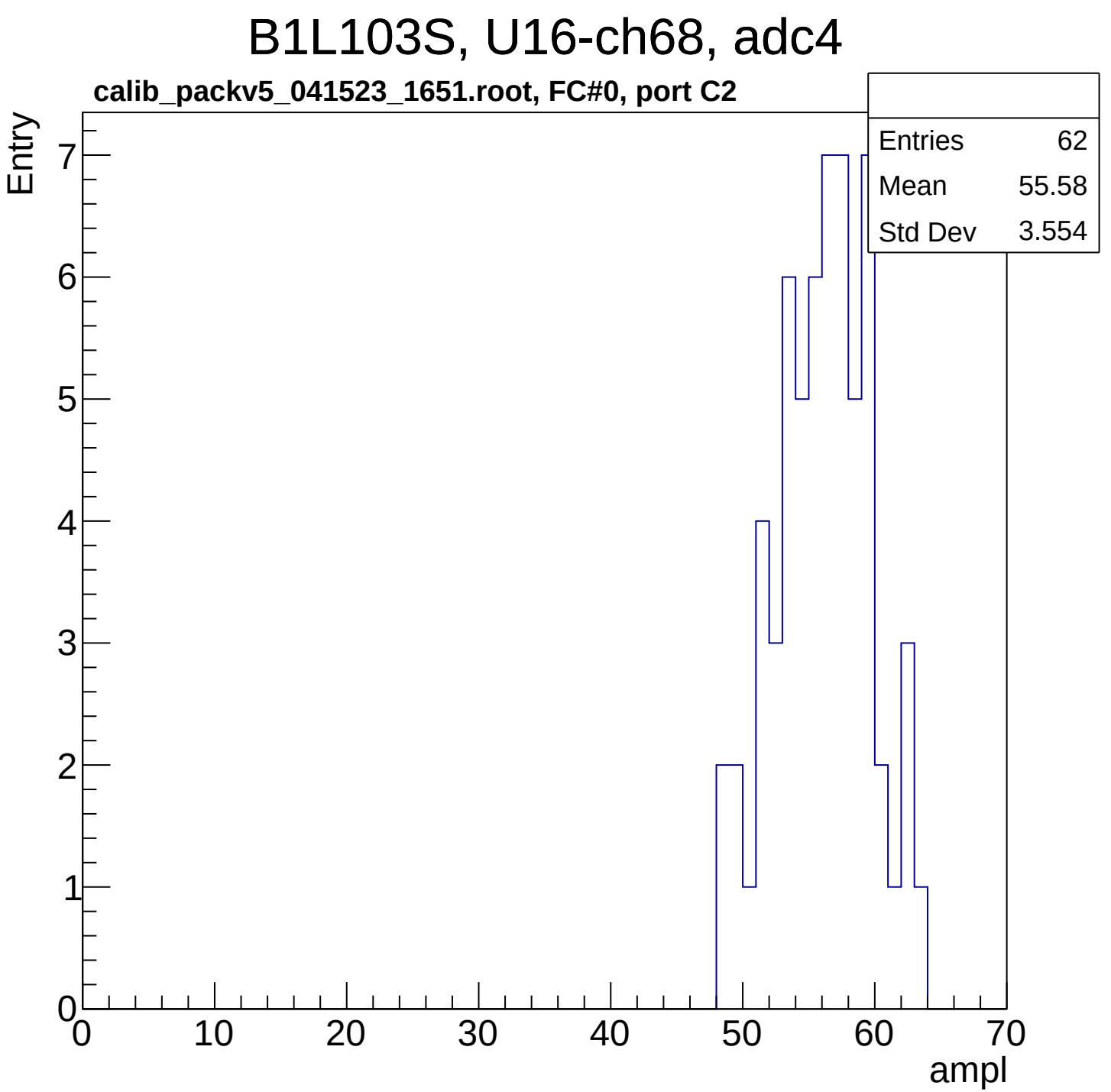

B1L103S, U16-ch67, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

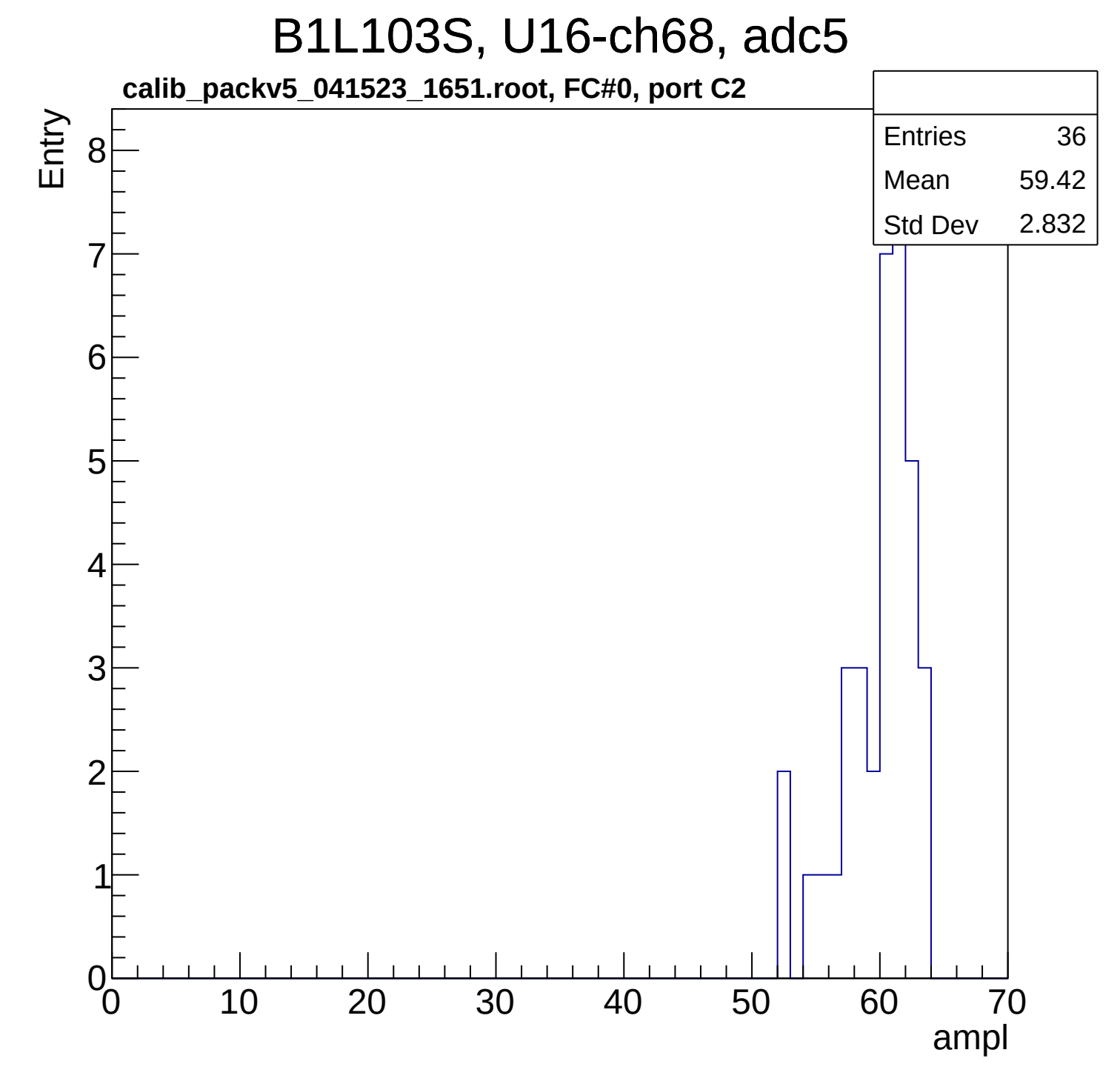

B1L103S, U16-ch68, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 22.98
Std Dev 12.2
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch68, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 33.17
Std Dev 10.4
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch68, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 36.49
Std Dev 15.36
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch68, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 48.99
Std Dev 7.161
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch68, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 55.58
Std Dev 3.554
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch68, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 59.42
Std Dev 2.832
Entry
ampl
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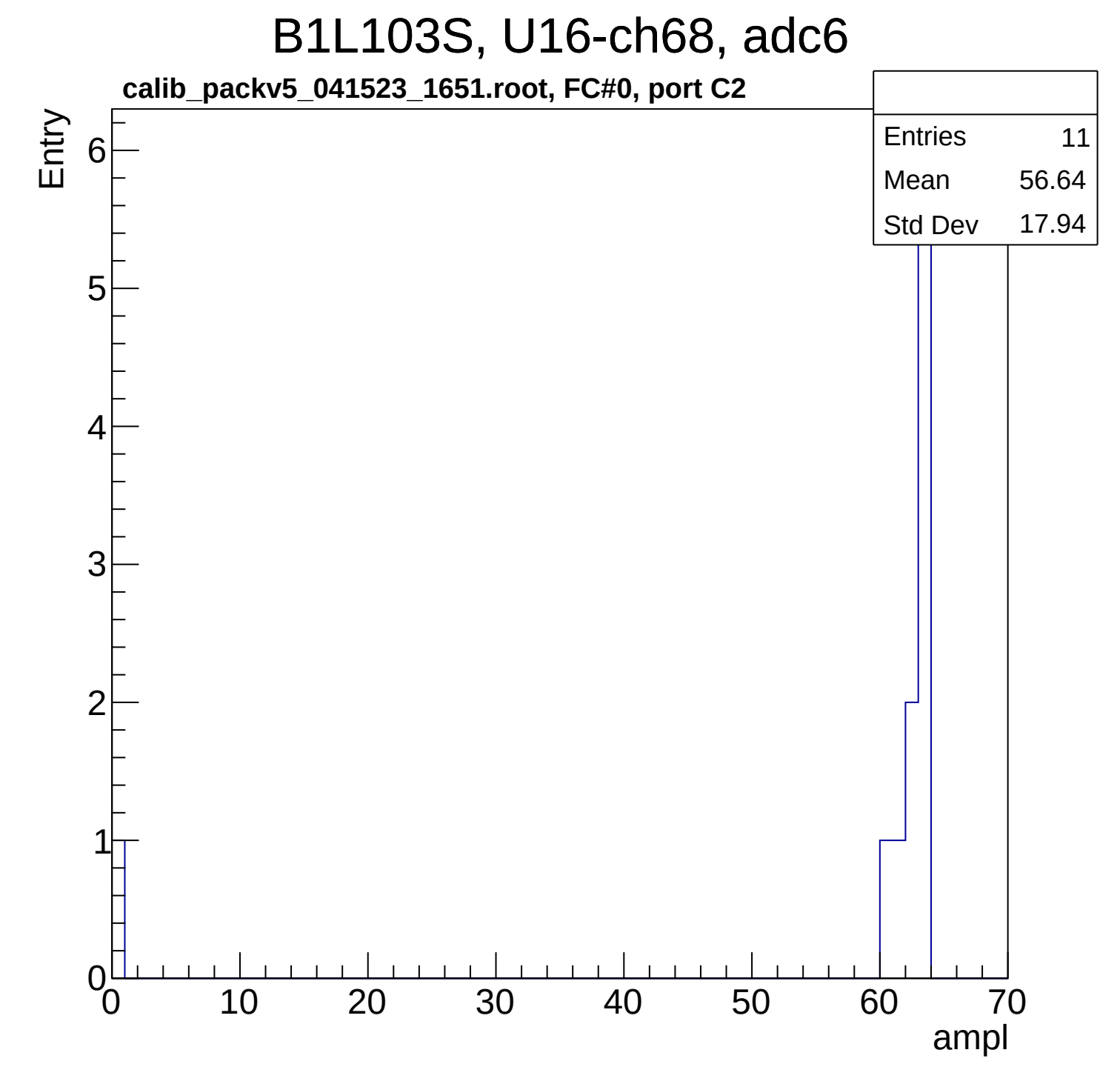
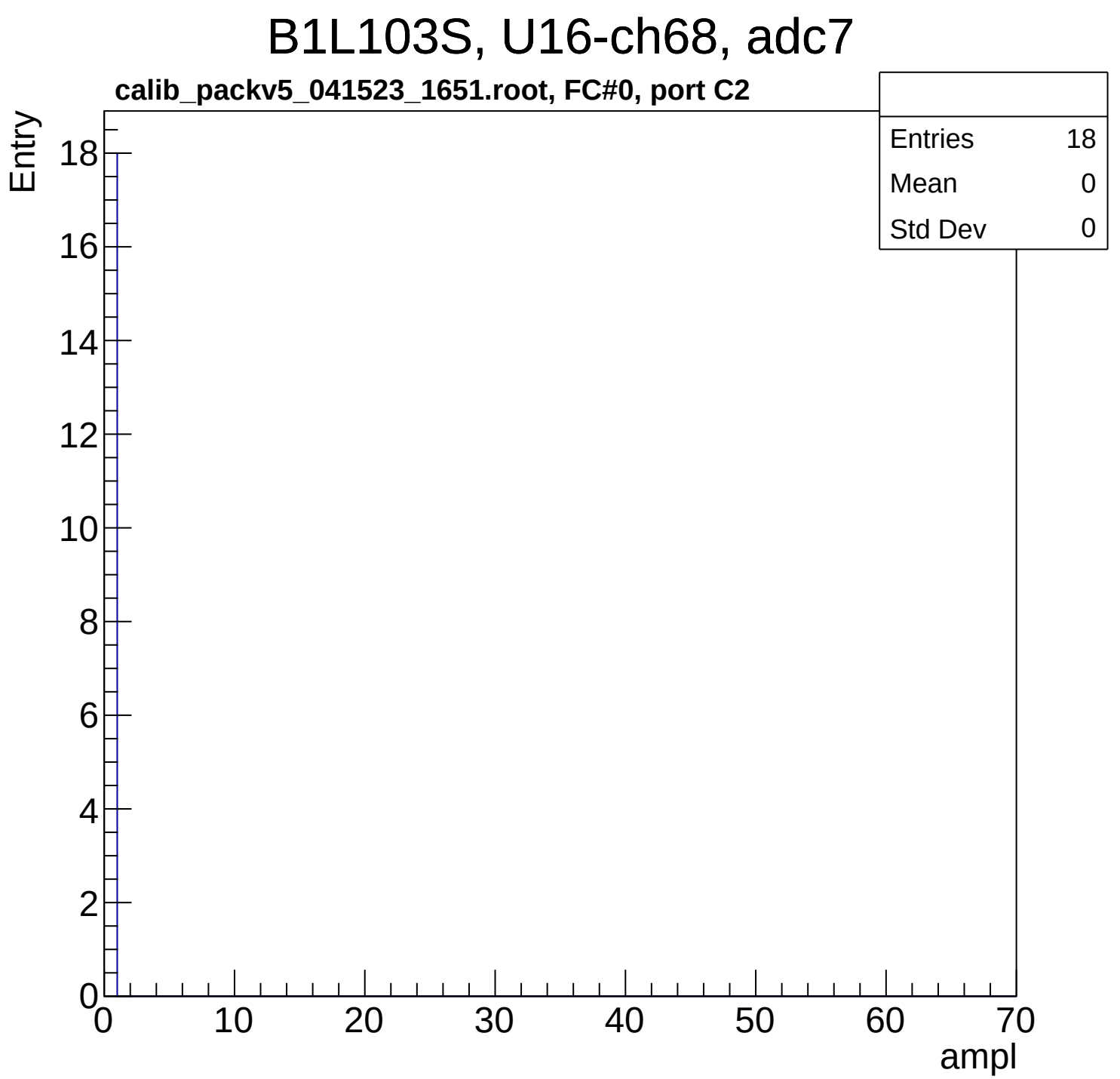
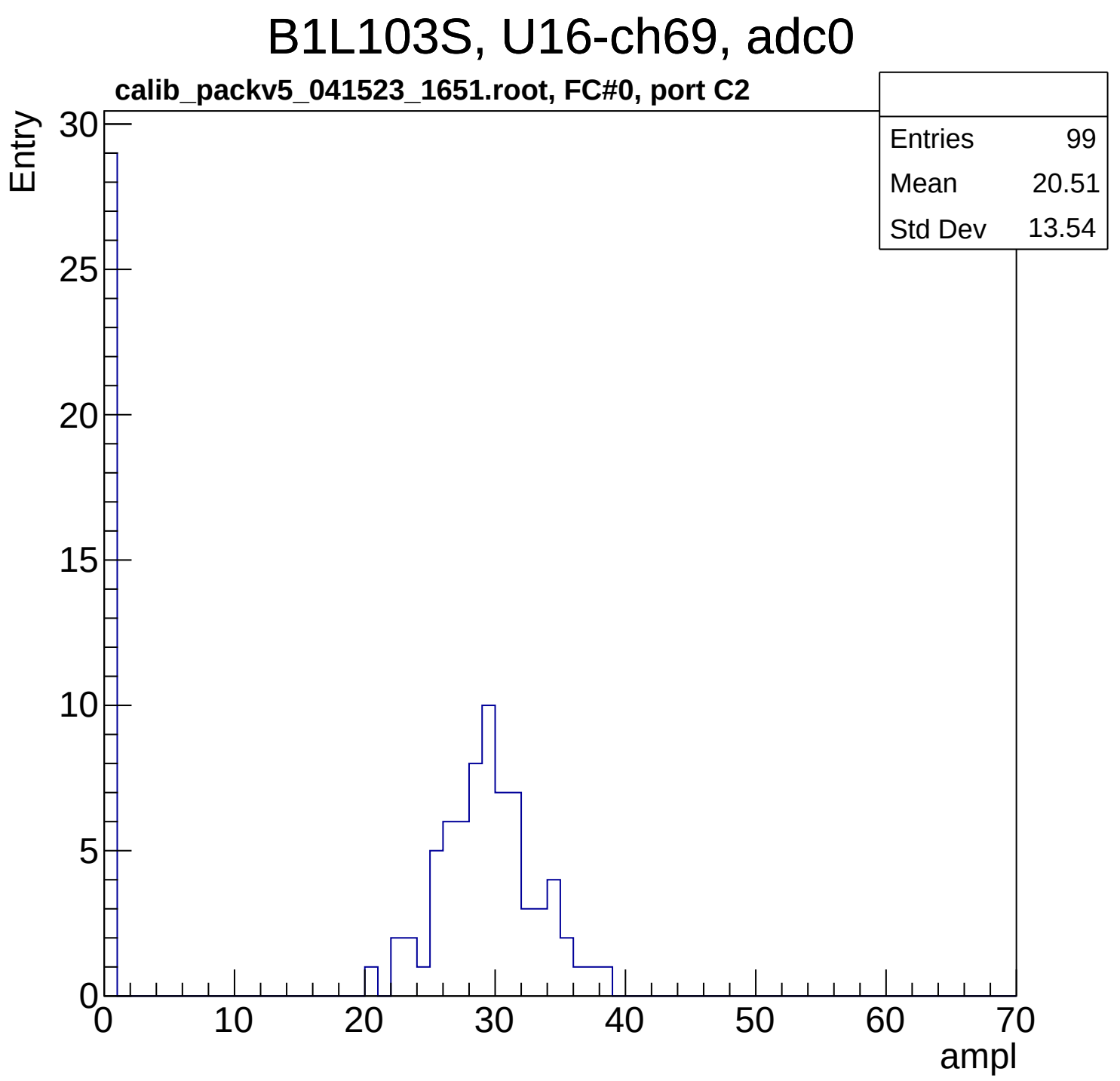
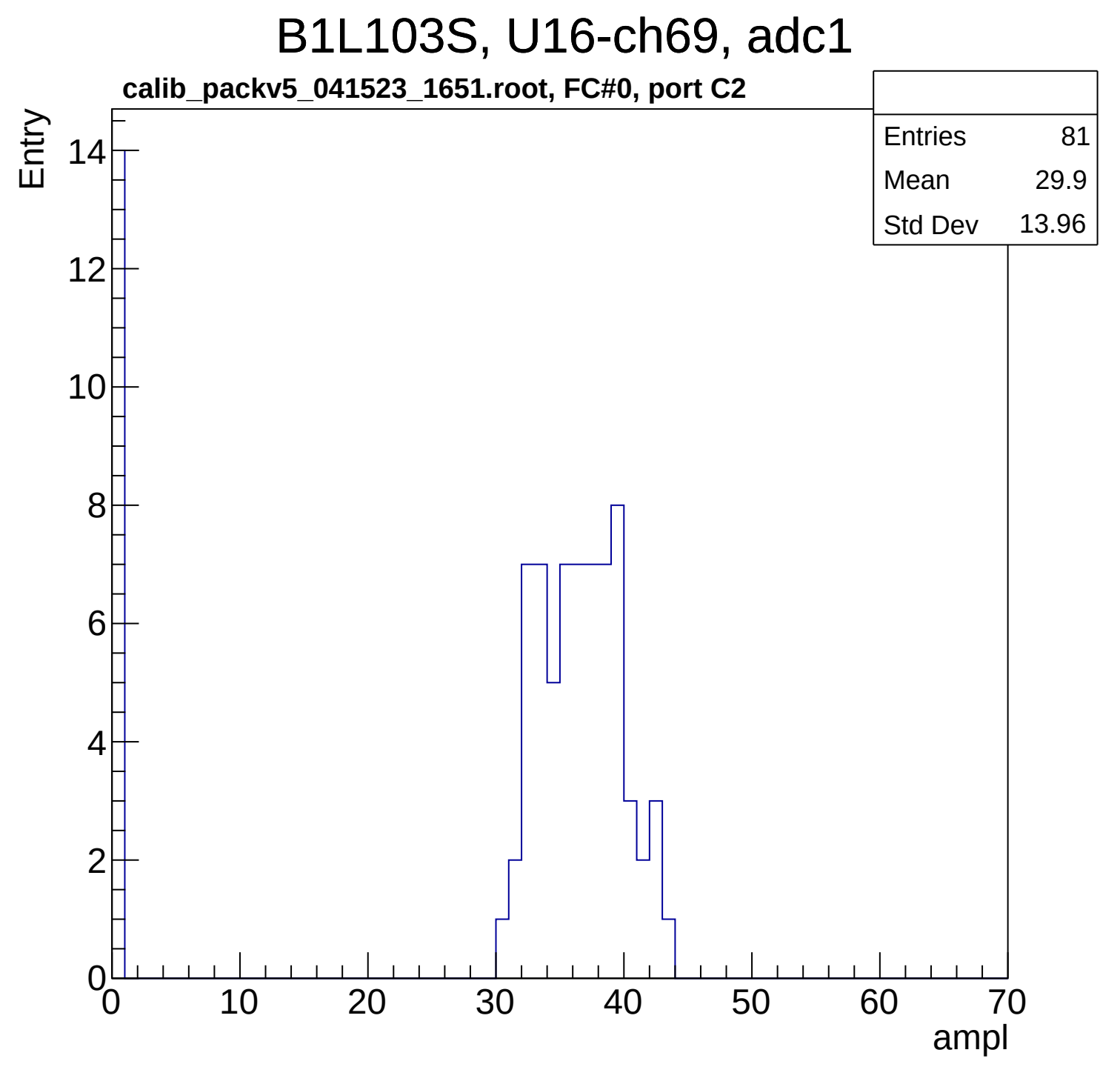
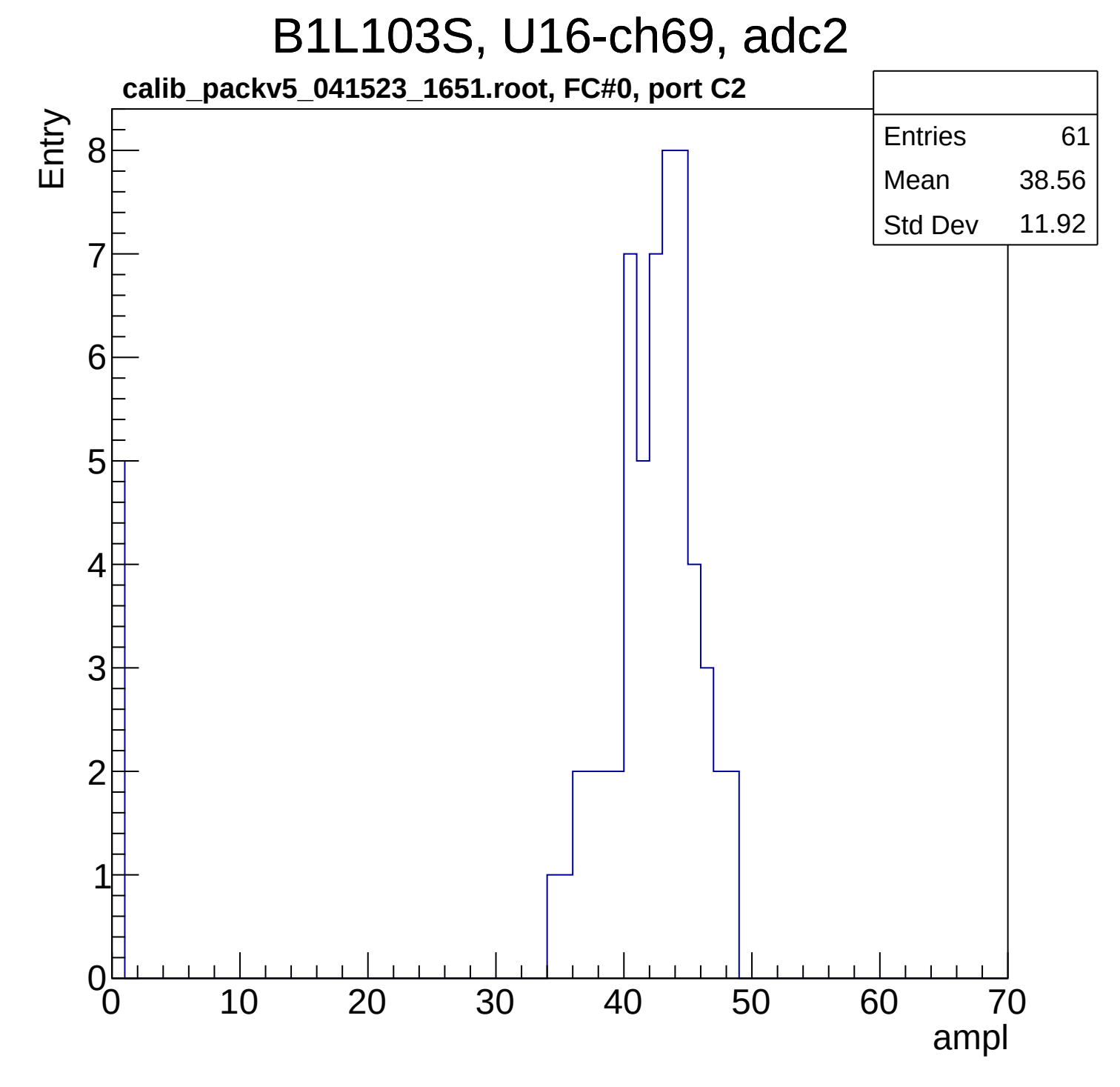
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch68, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 56.64
Std Dev 17.94
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch68, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch69, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 20.51
Std Dev 13.54
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70


B1L103S, U16-ch69, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 29.9
Std Dev 13.96
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U16-ch69, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 38.56
Std Dev 11.92
Entry
ampl
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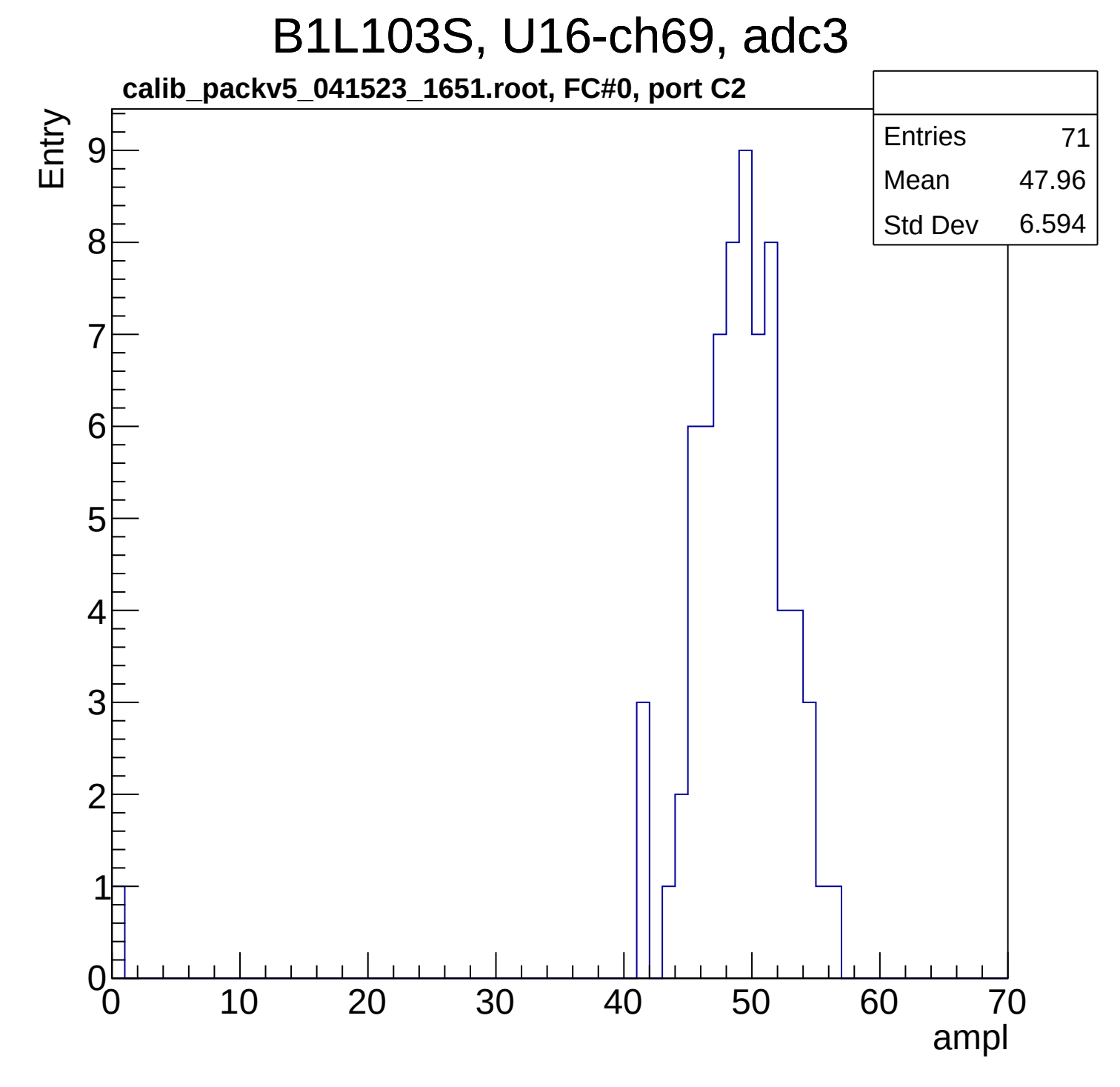
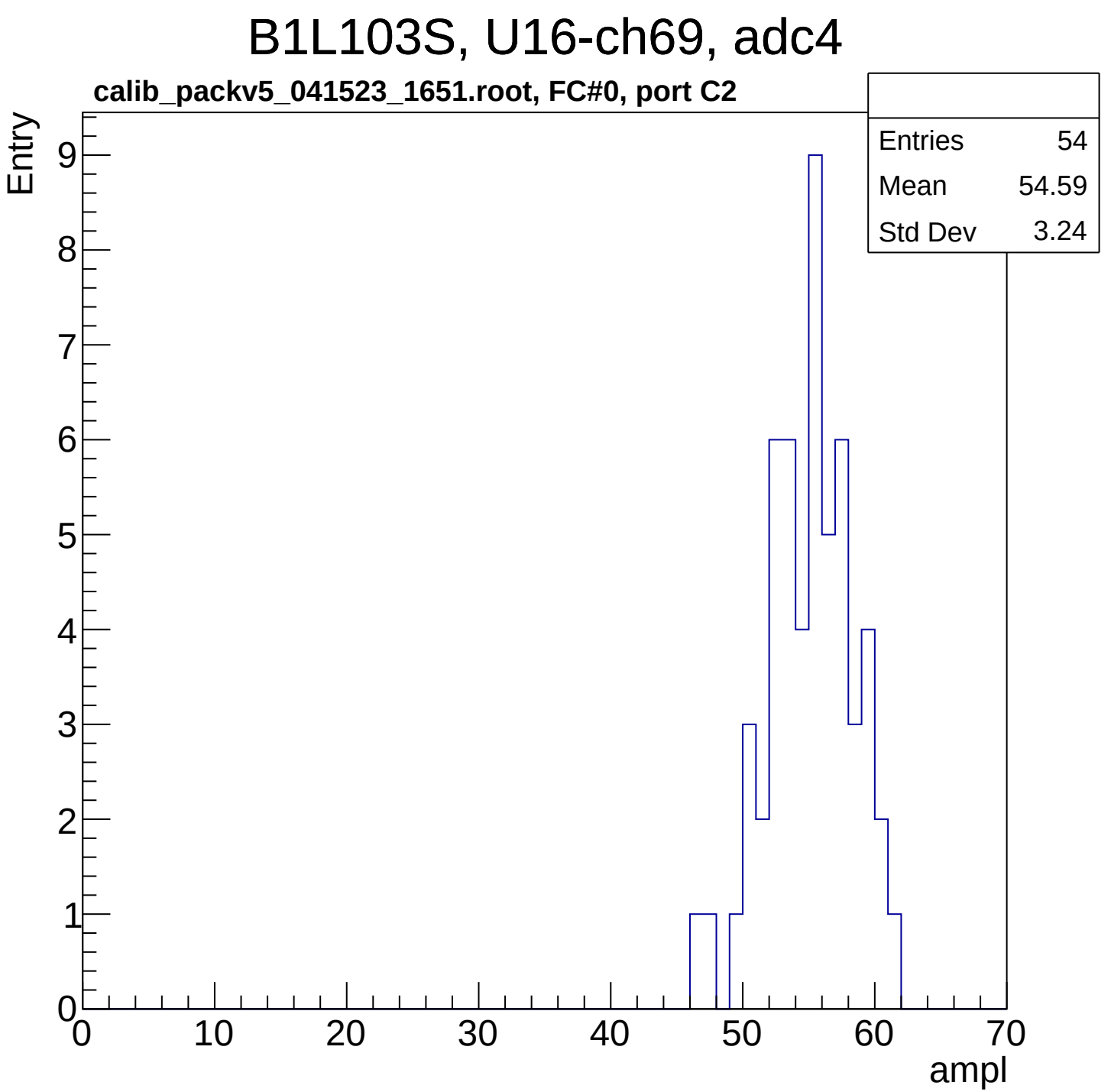
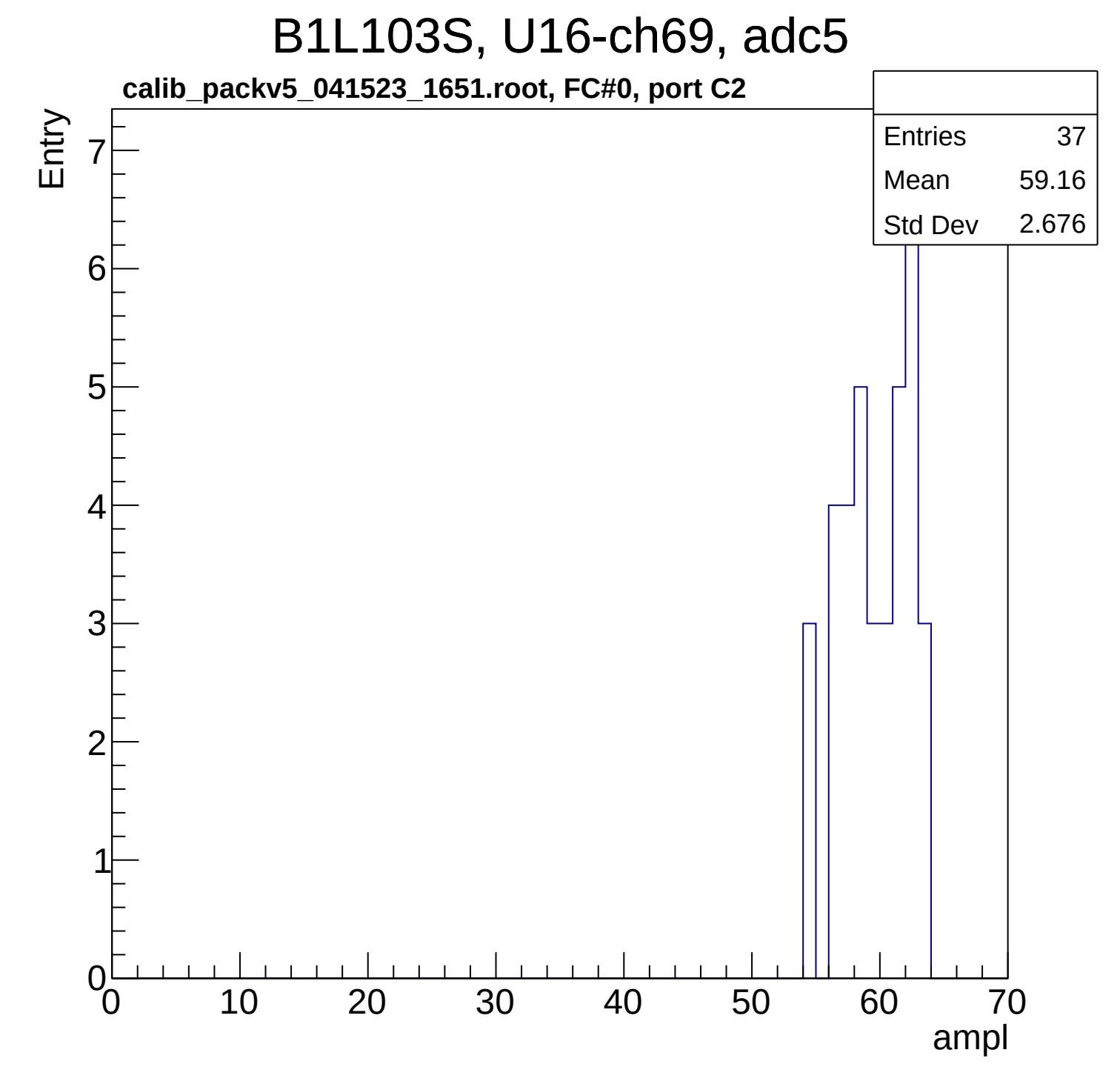
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch69, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 47.96
Std Dev 6.594
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch69, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 54.59
Std Dev 3.24
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch69, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 59.16
Std Dev 2.676
Entry
ampl
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1
2
3
4
5
6
7
0
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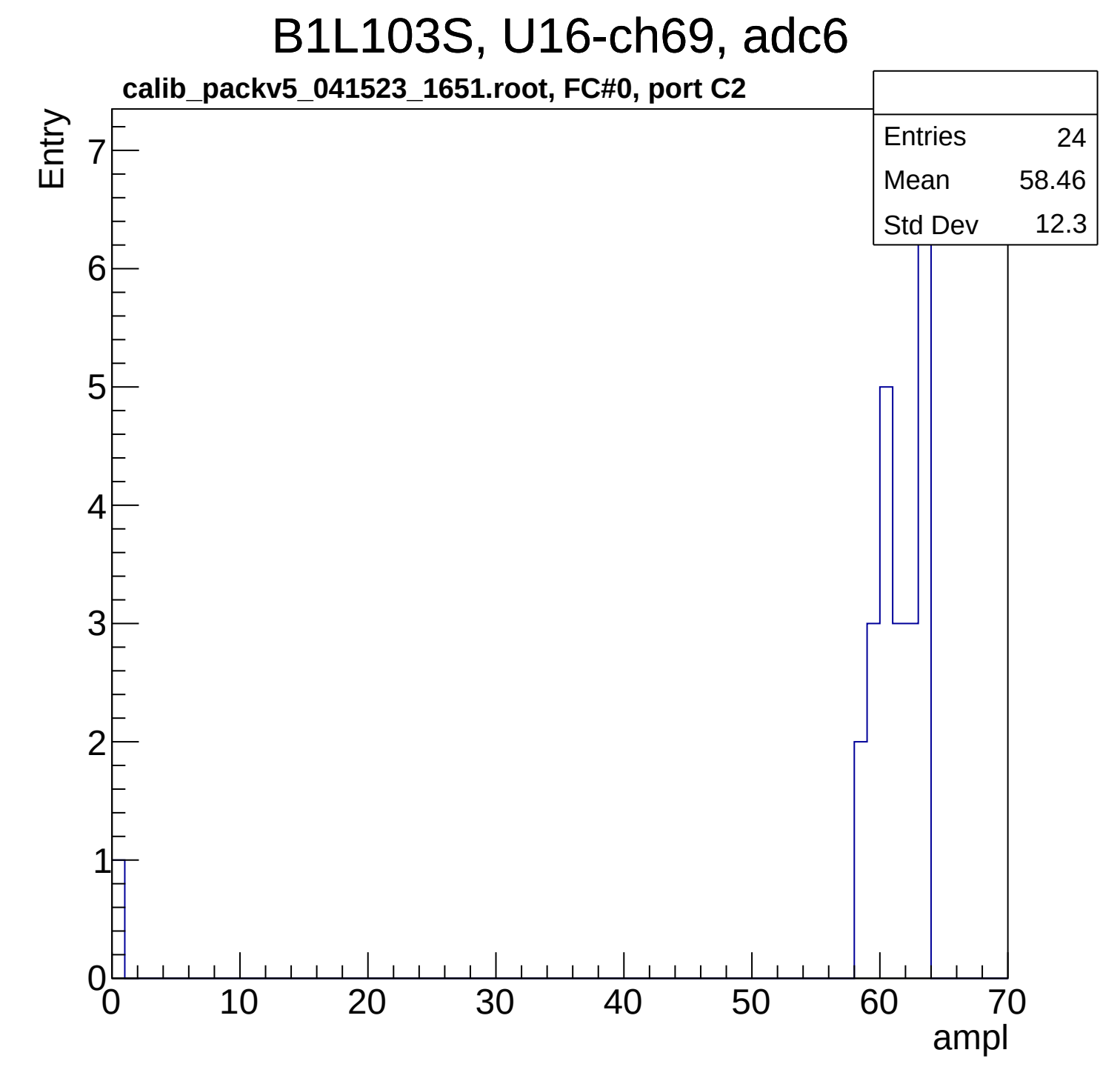
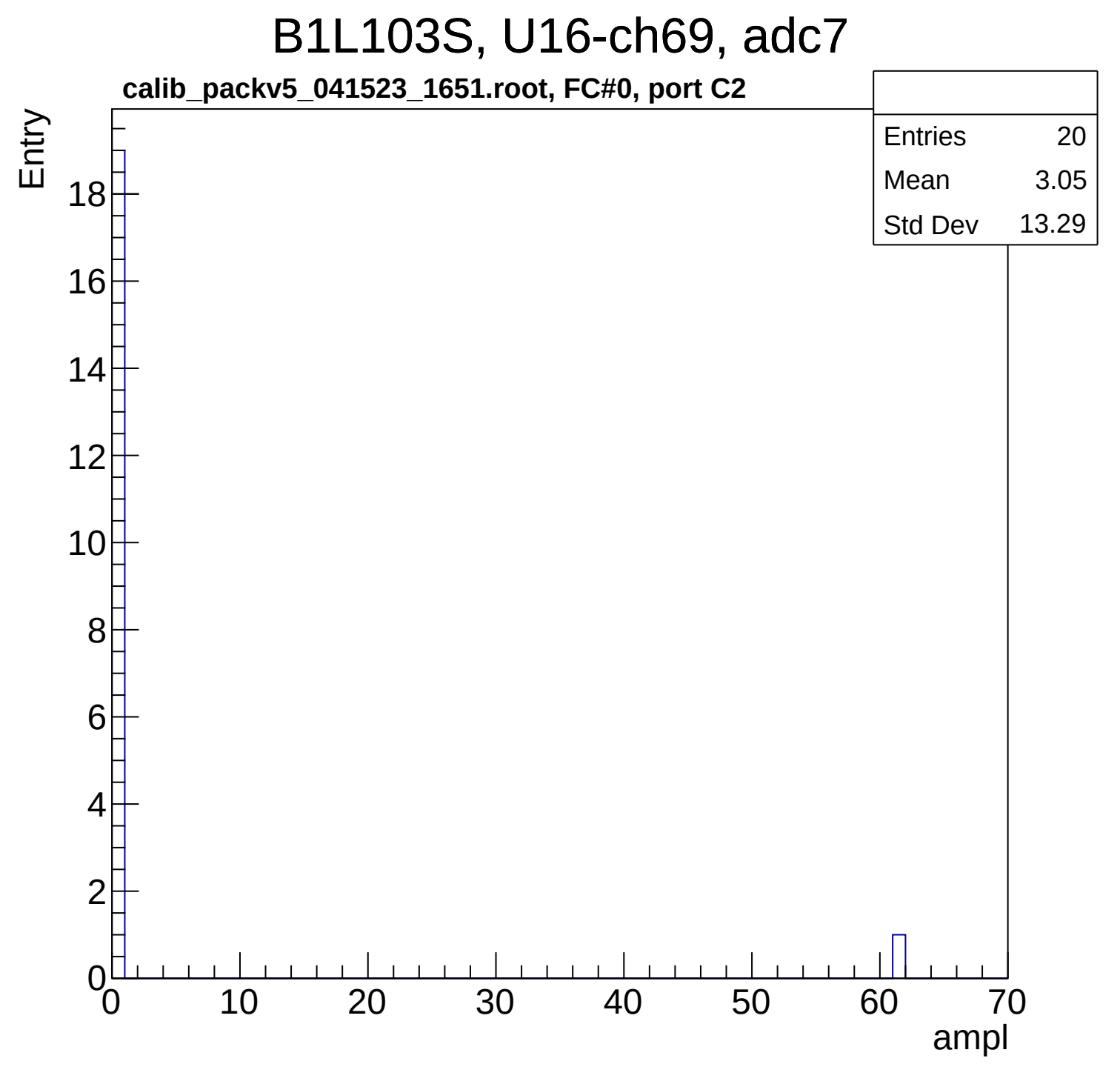
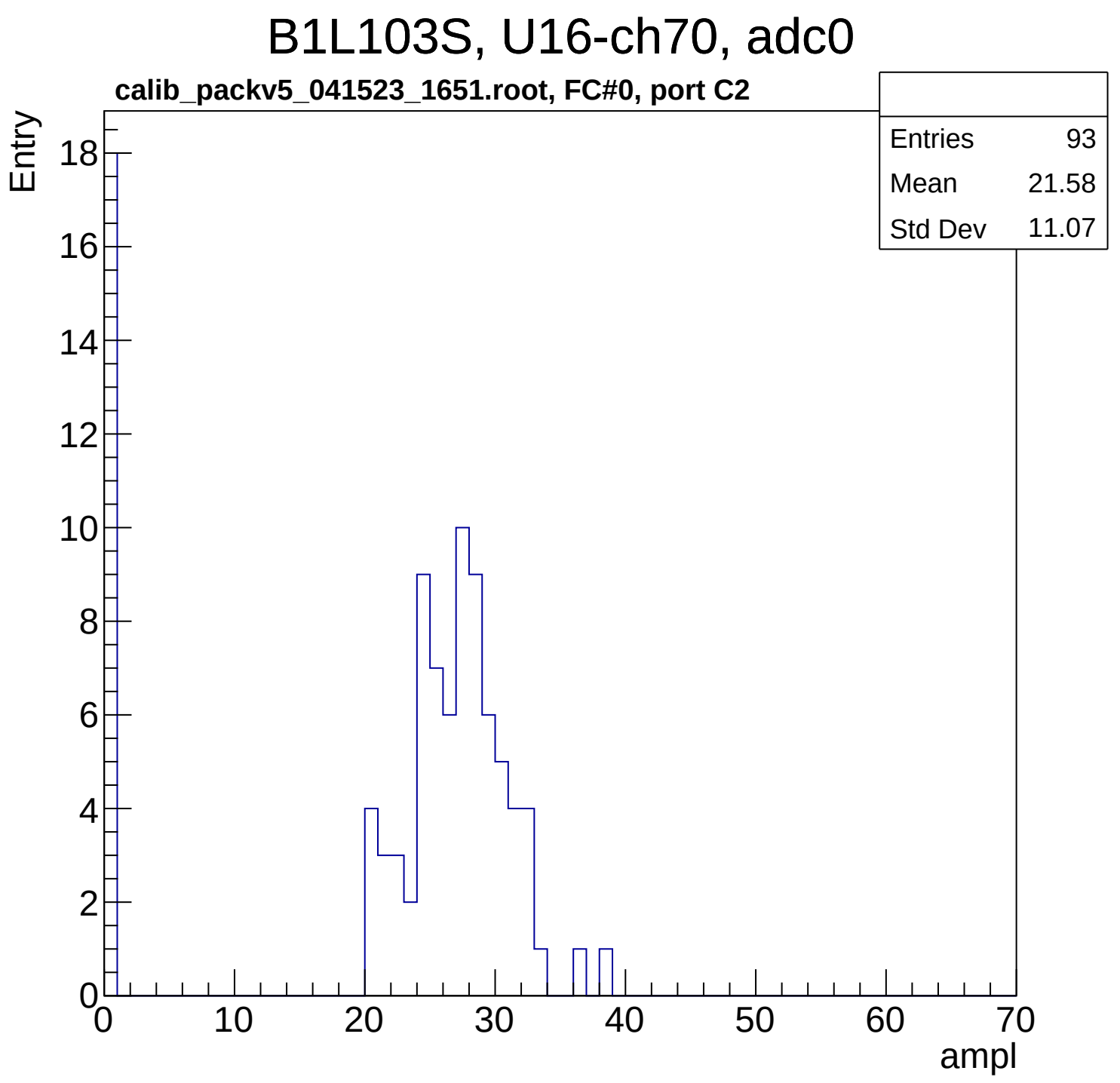
20
30
40
50
60
70


B1L103S, U16-ch69, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 58.46
Std Dev 12.3
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch69, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch70, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 21.58
Std Dev 11.07
Entry
ampl
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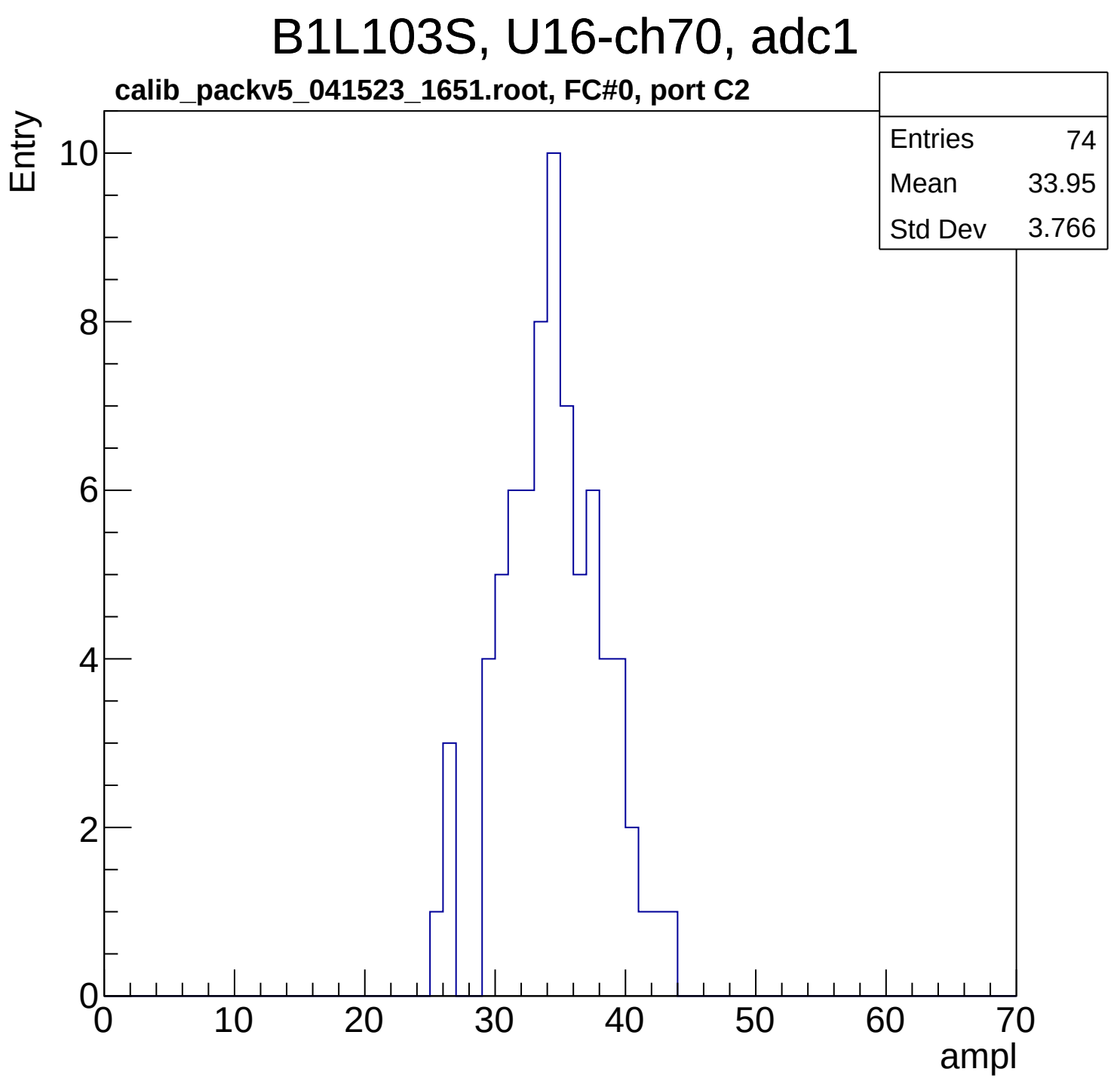
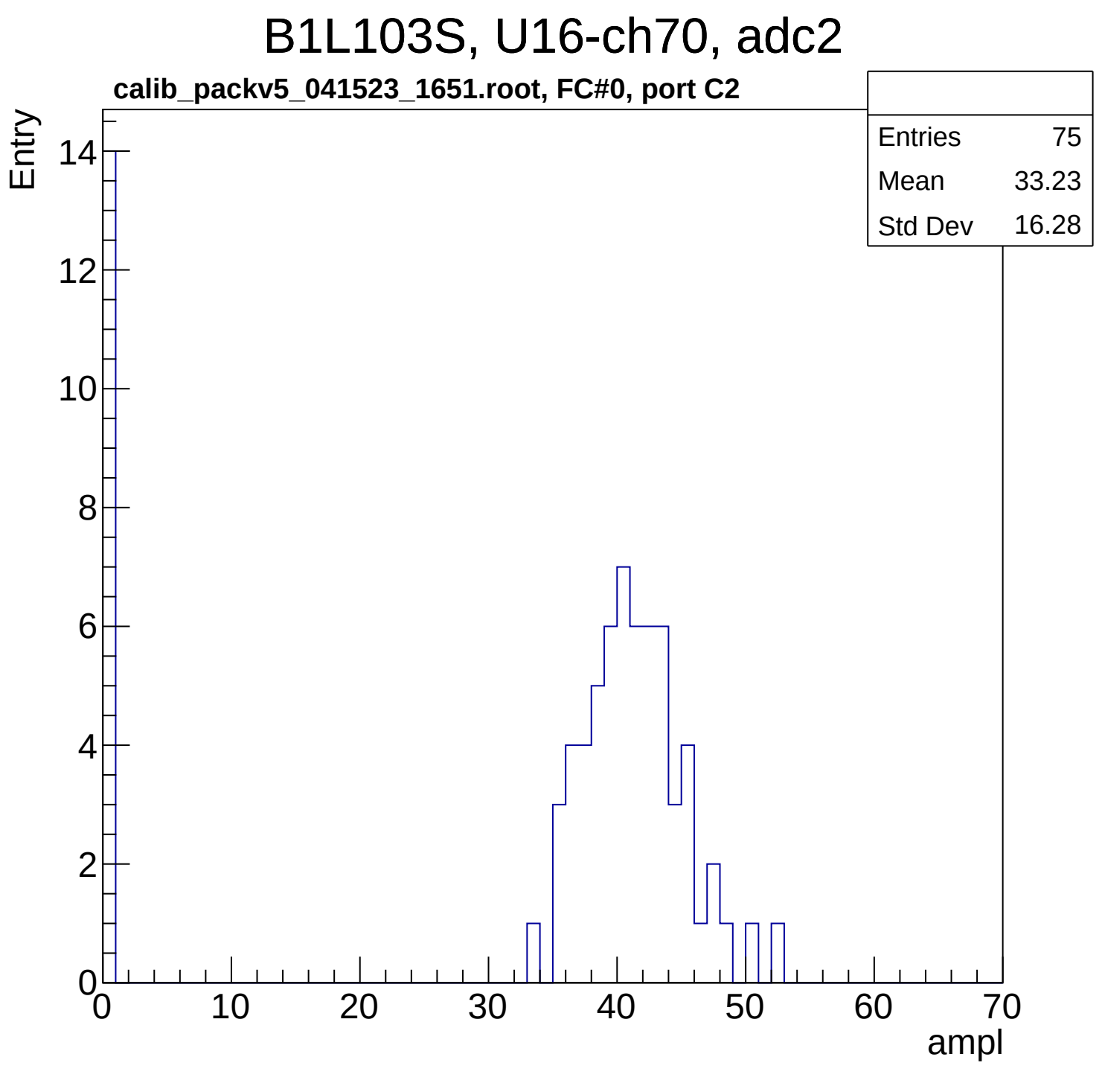
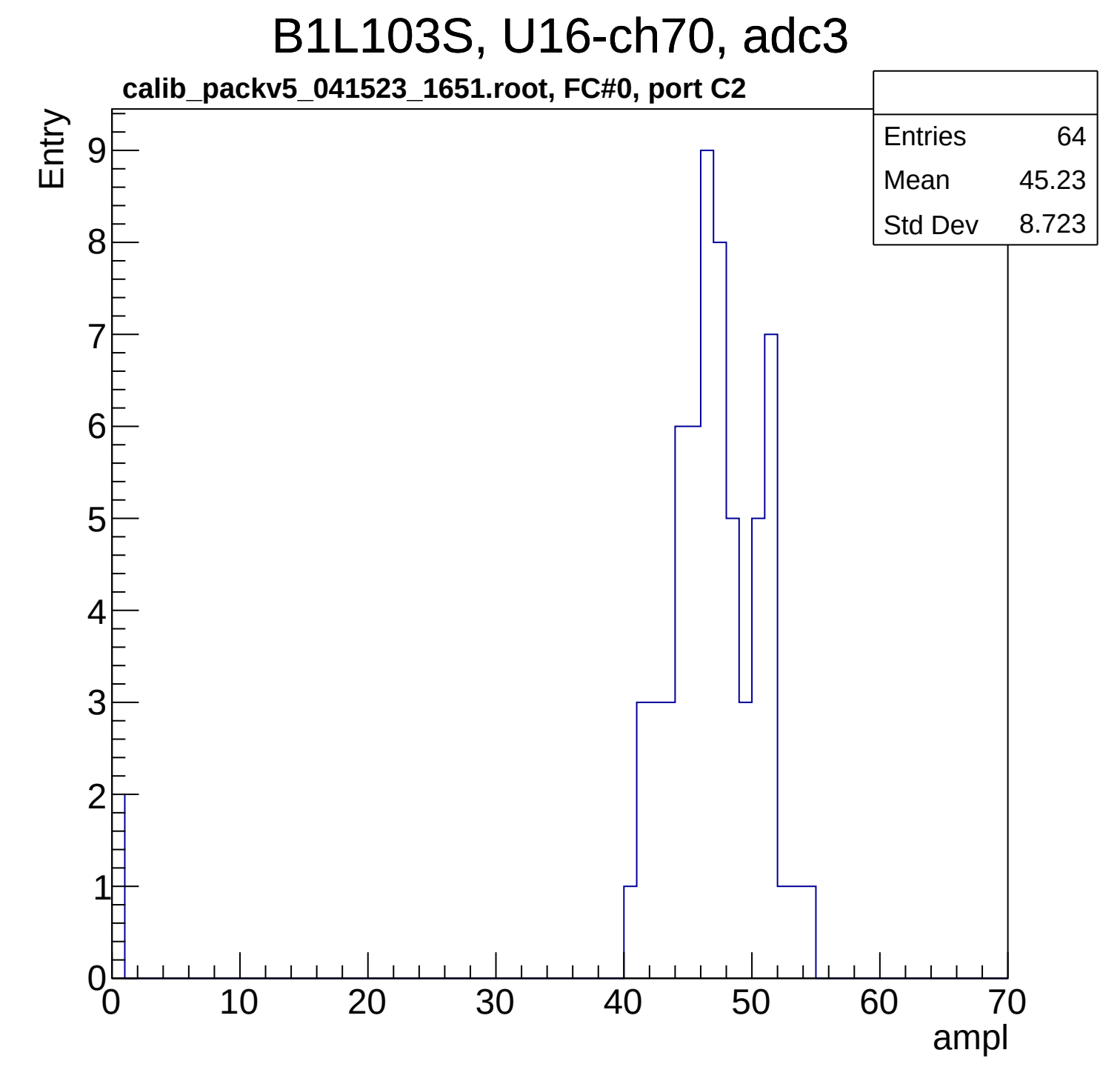
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L103S, U16-ch70, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 33.95
Std Dev 3.766
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch70, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 33.23
Std Dev 16.28
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U16-ch70, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 45.23
Std Dev 8.723
Entry
ampl
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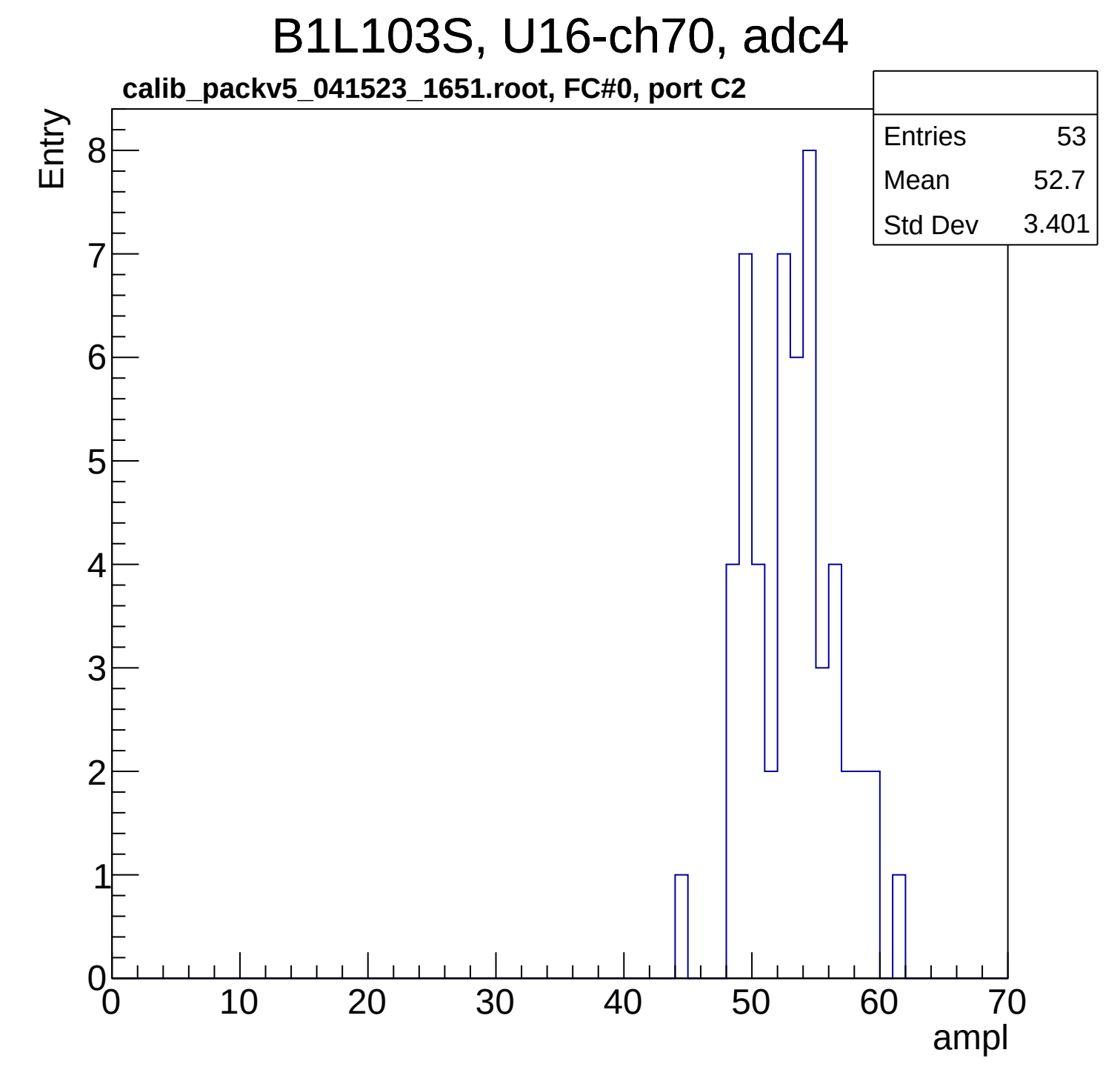
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U16-ch70, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 52.7
Std Dev 3.401
Entry
ampl
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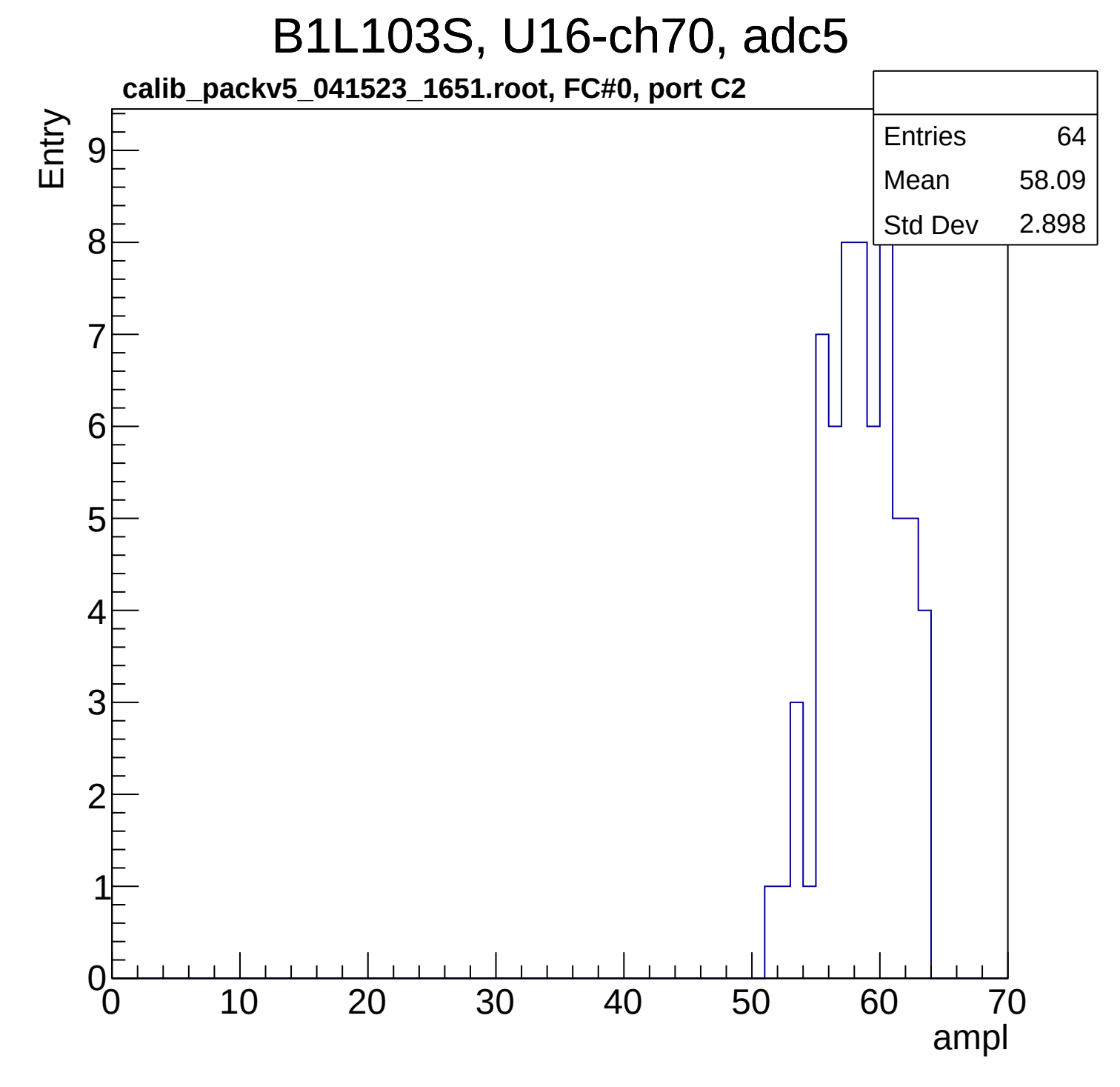
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch70, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 58.09
Std Dev 2.898
Entry
ampl
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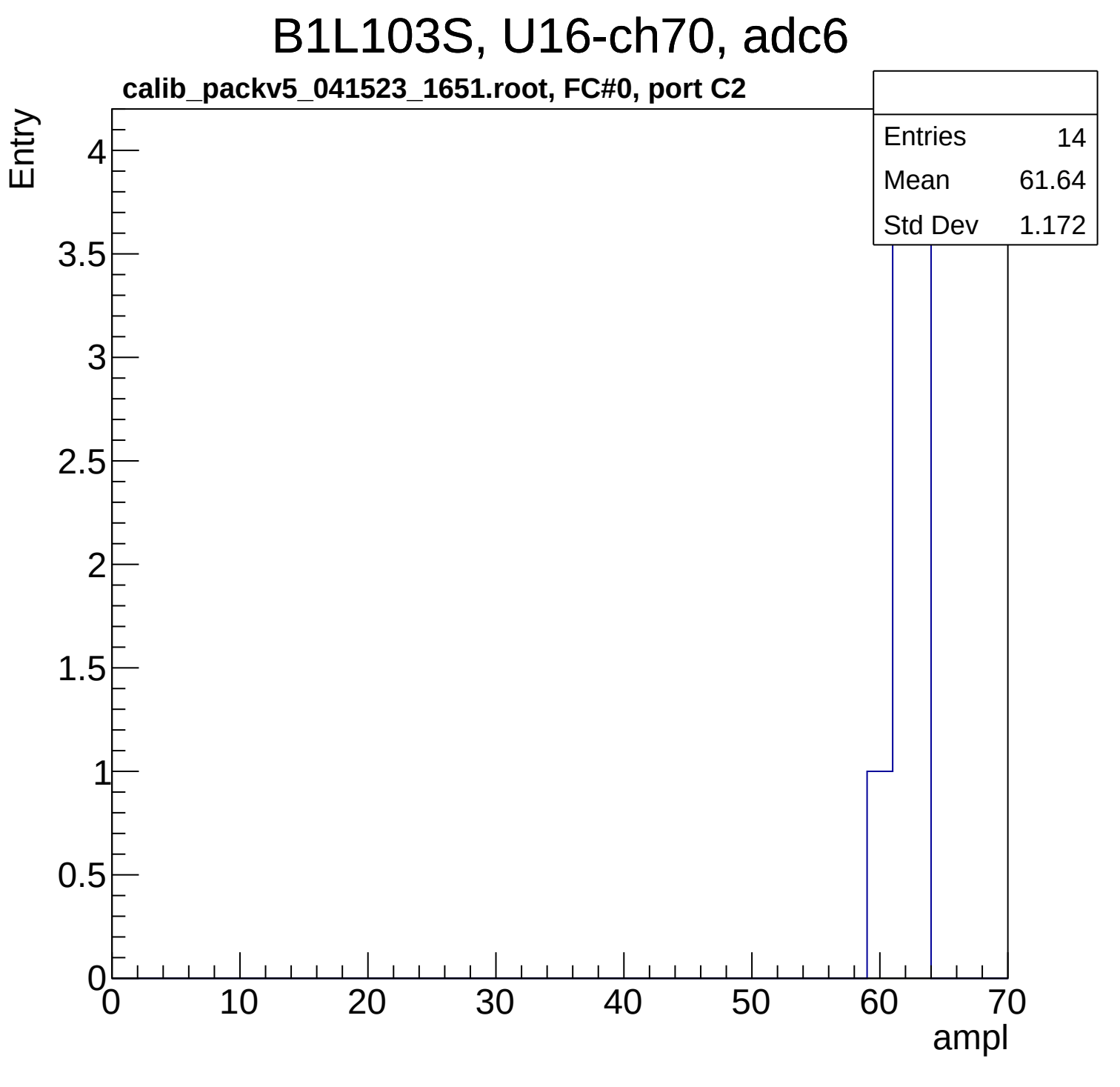
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch70, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.64
Std Dev 1.172
Entry
ampl
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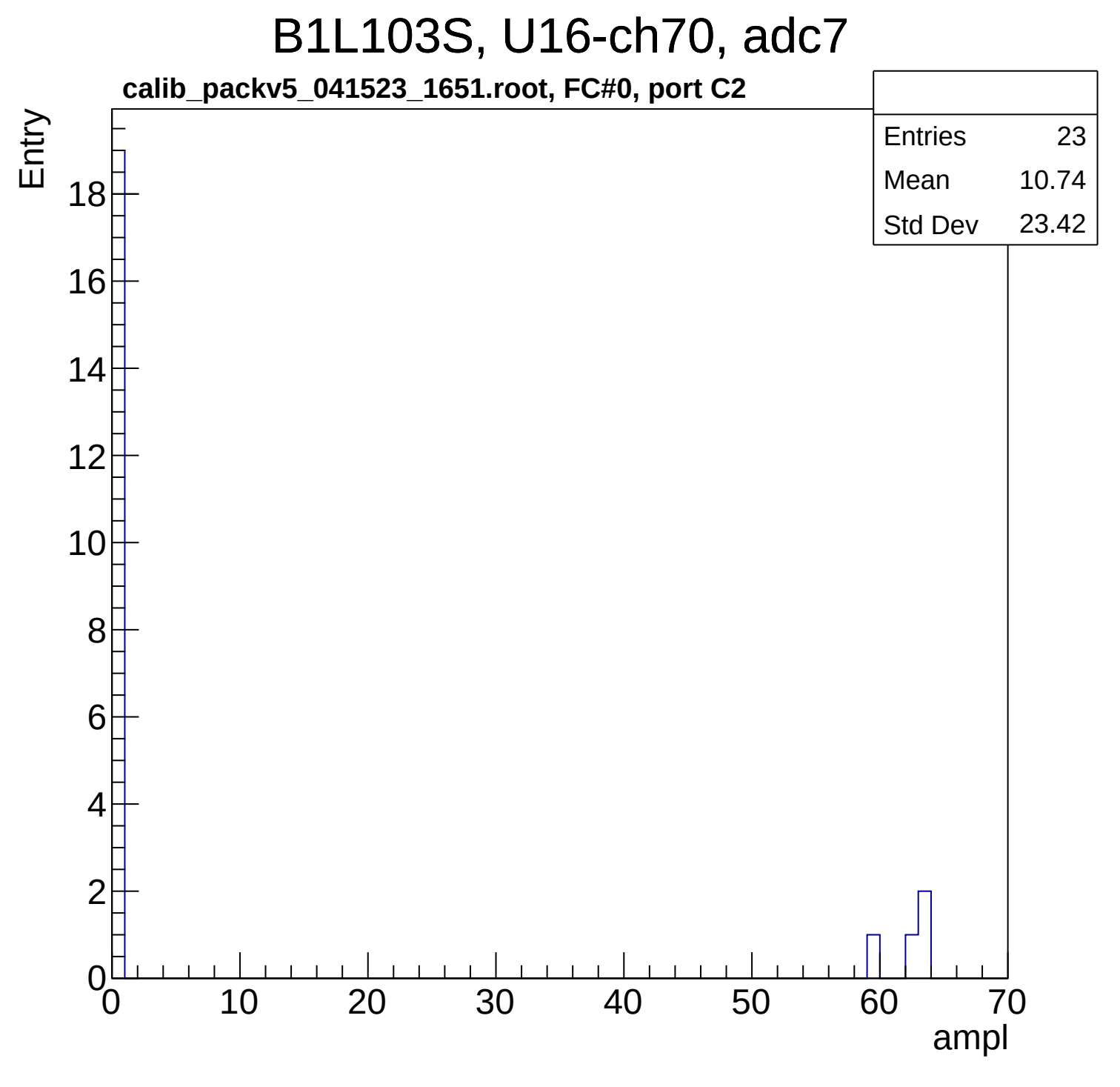
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U16-ch70, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.74
Std Dev 23.42
Entry
0
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4
6
8
10
12
14
16
18
0
10
20
30
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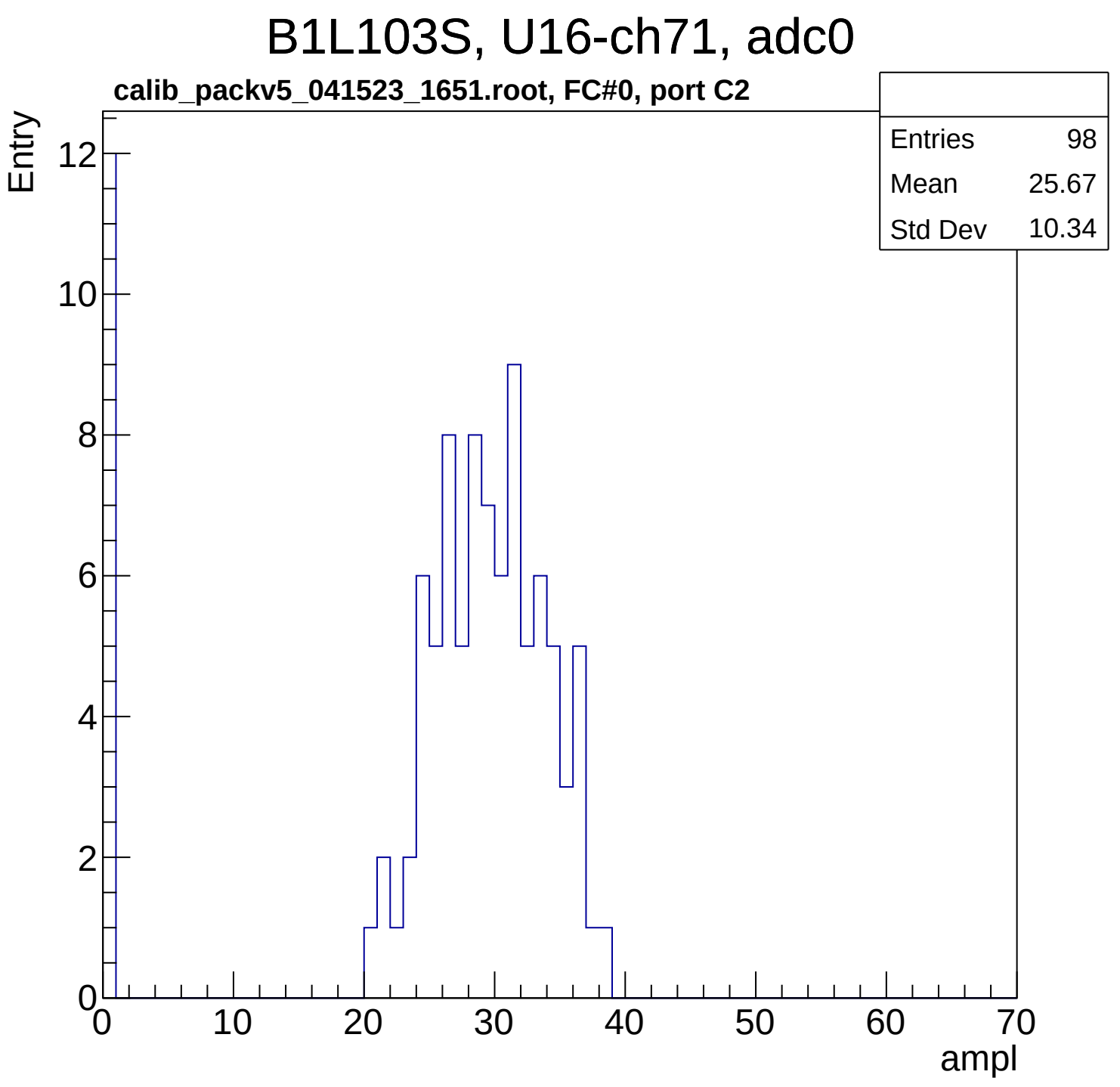
50
60
70
ampl


B1L103S, U16-ch71, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 25.67
Std Dev 10.34
Entry
0
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4
6
8
10
12
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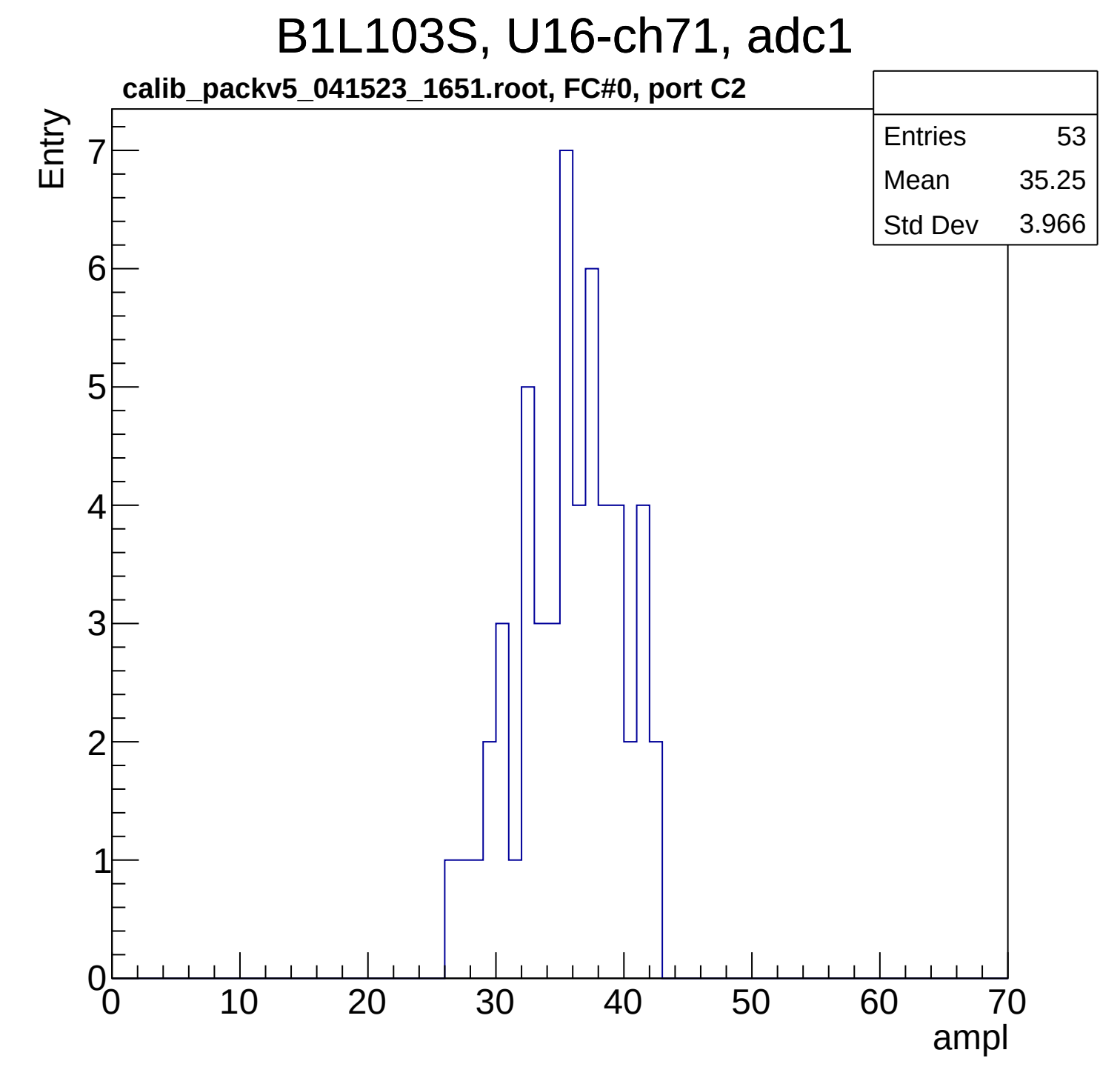
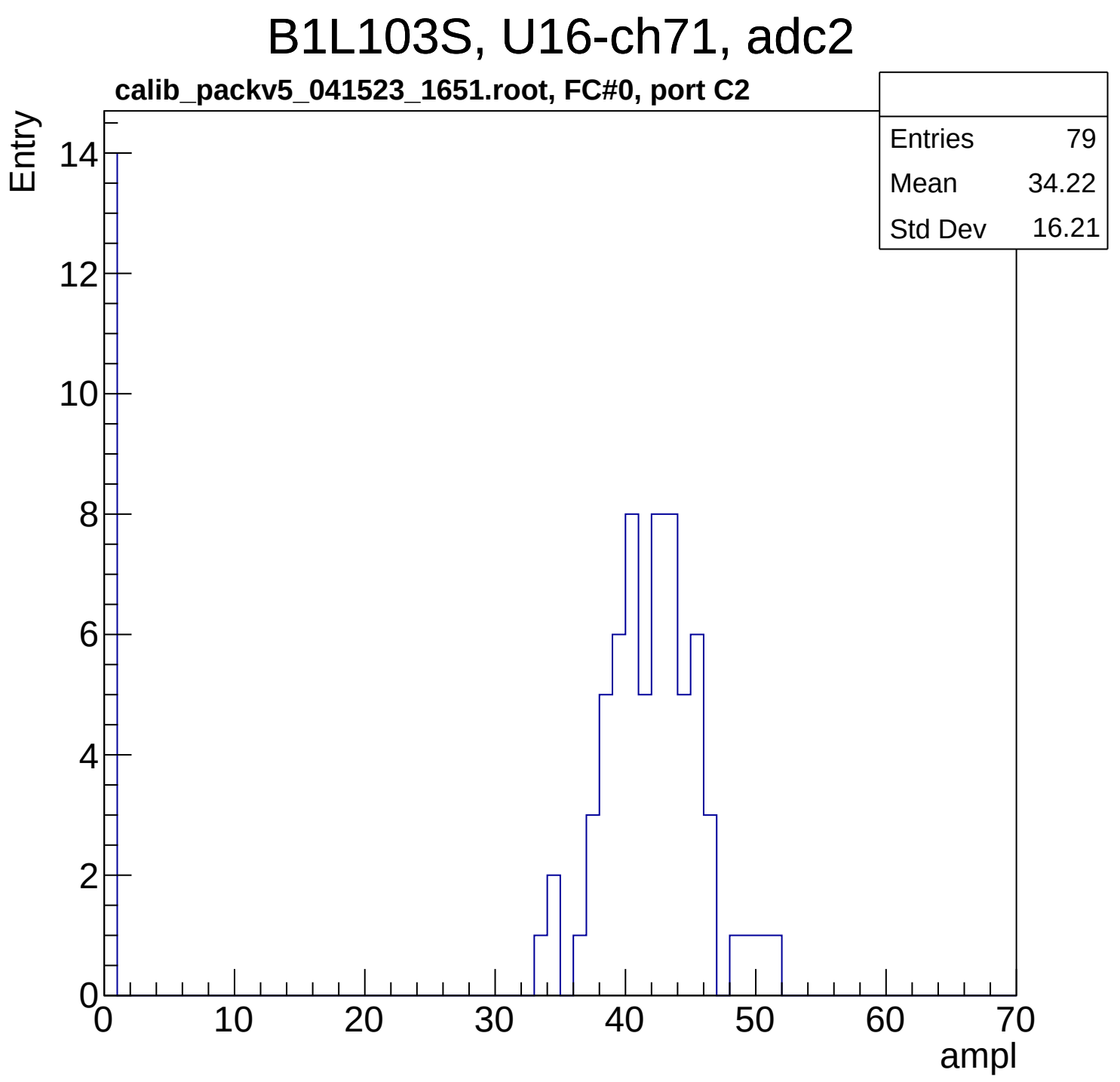
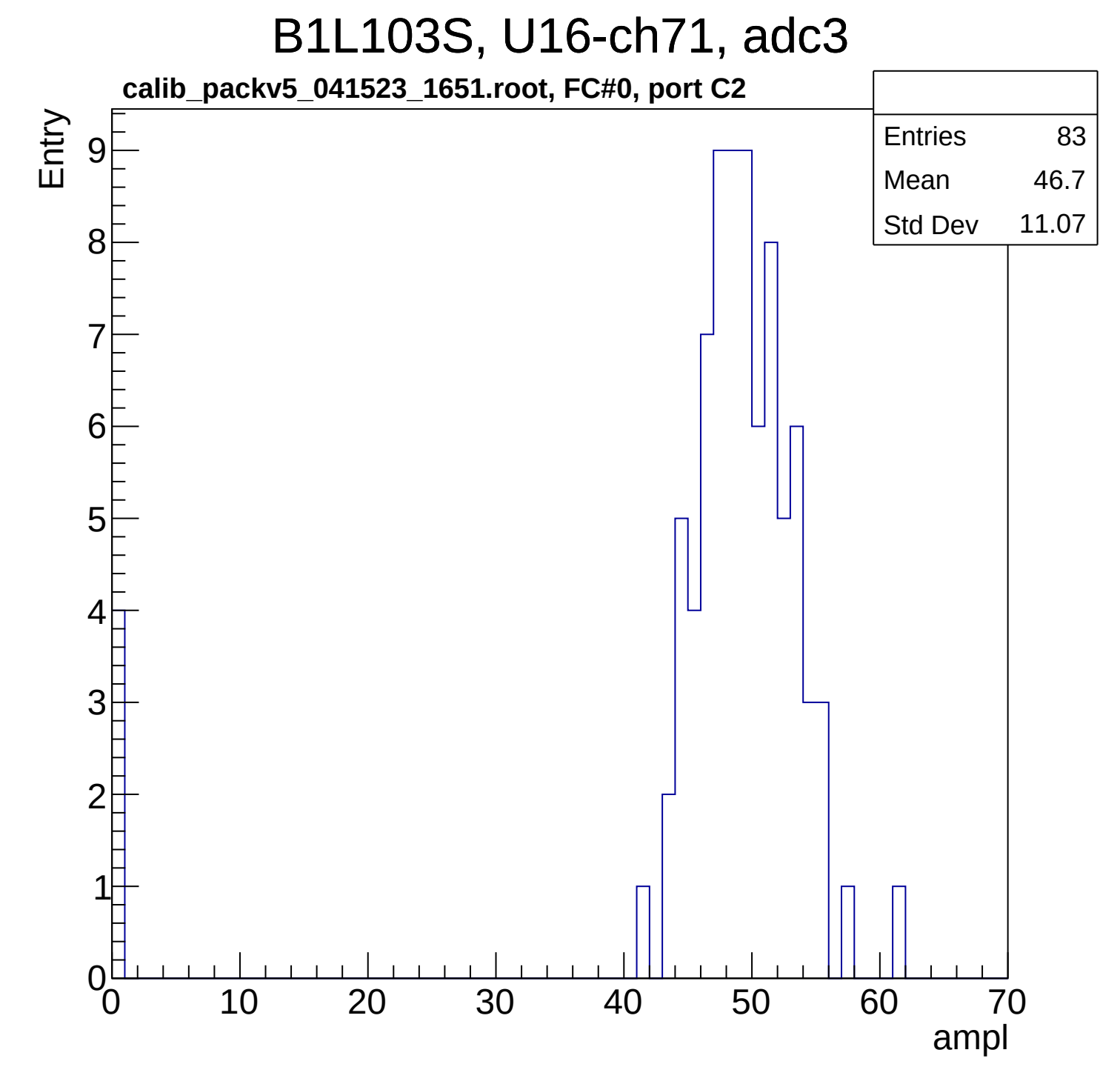
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch71, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 35.25
Std Dev 3.966
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch71, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 34.22
Std Dev 16.21
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch71, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 46.7
Std Dev 11.07
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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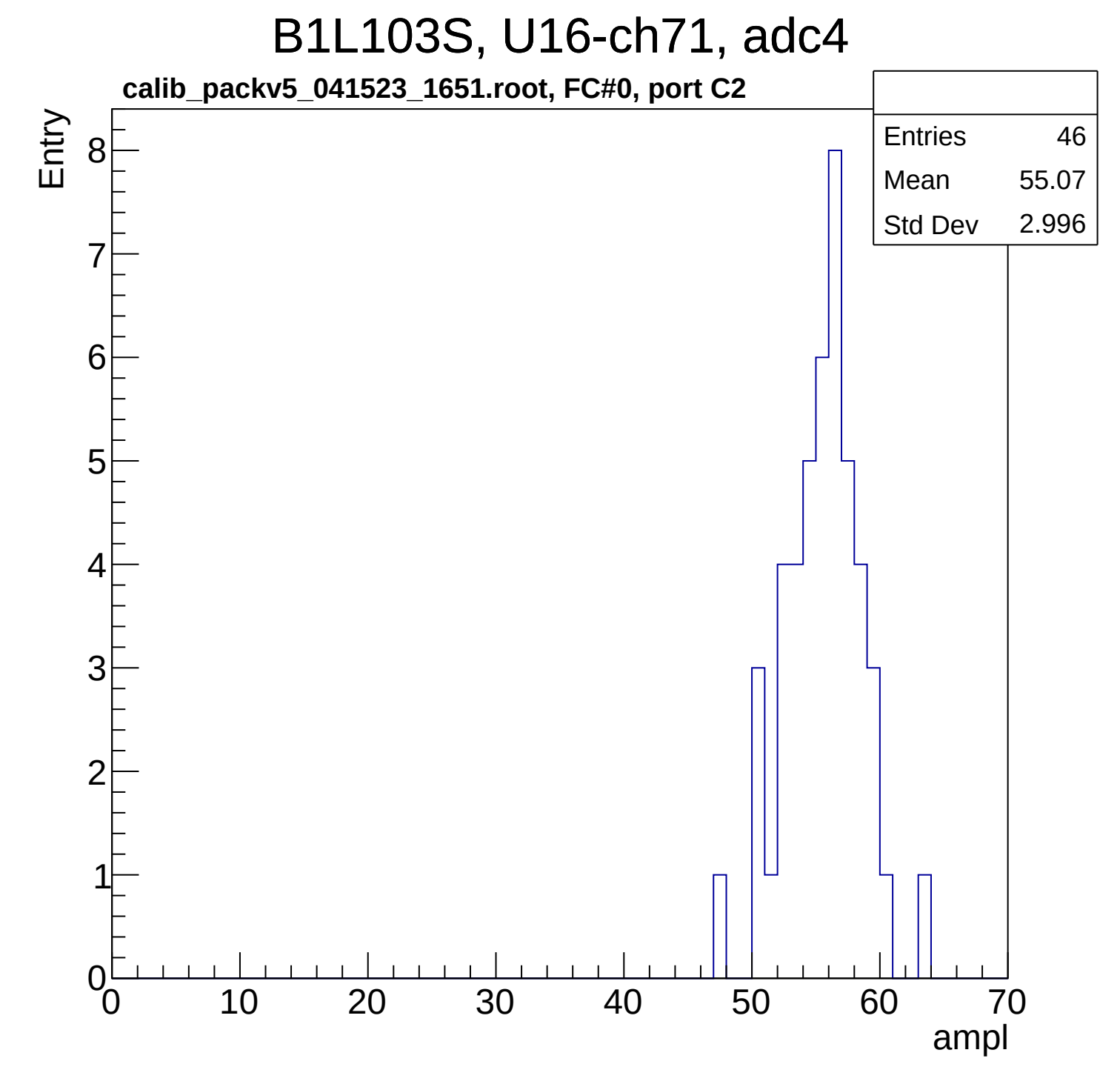
30
40
50
60
70


B1L103S, U16-ch71, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 55.07
Std Dev 2.996
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
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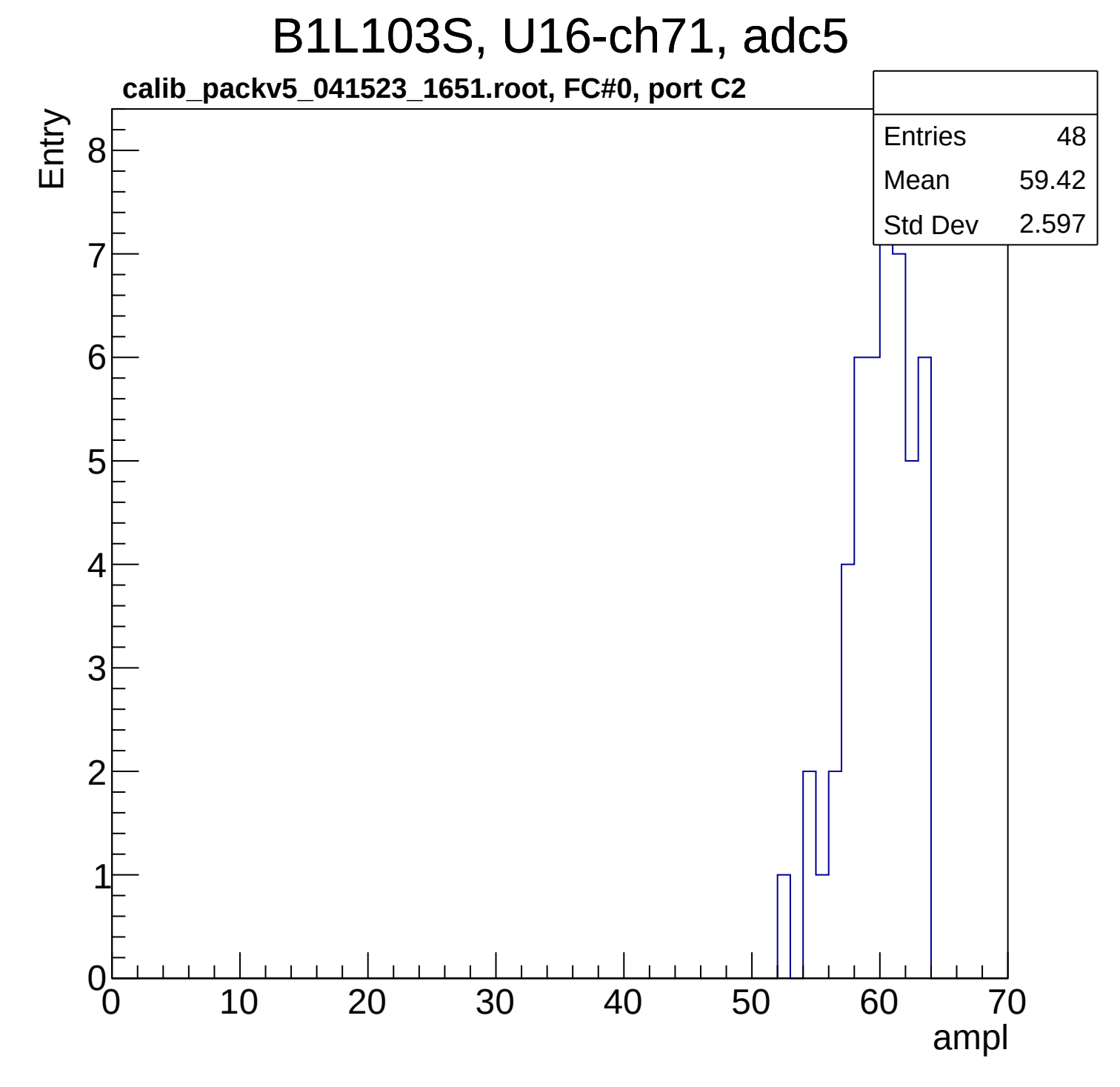
60
70


B1L103S, U16-ch71, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 59.42
Std Dev 2.597
Entry
ampl
0
1
2
3
4
5
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7
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0
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60
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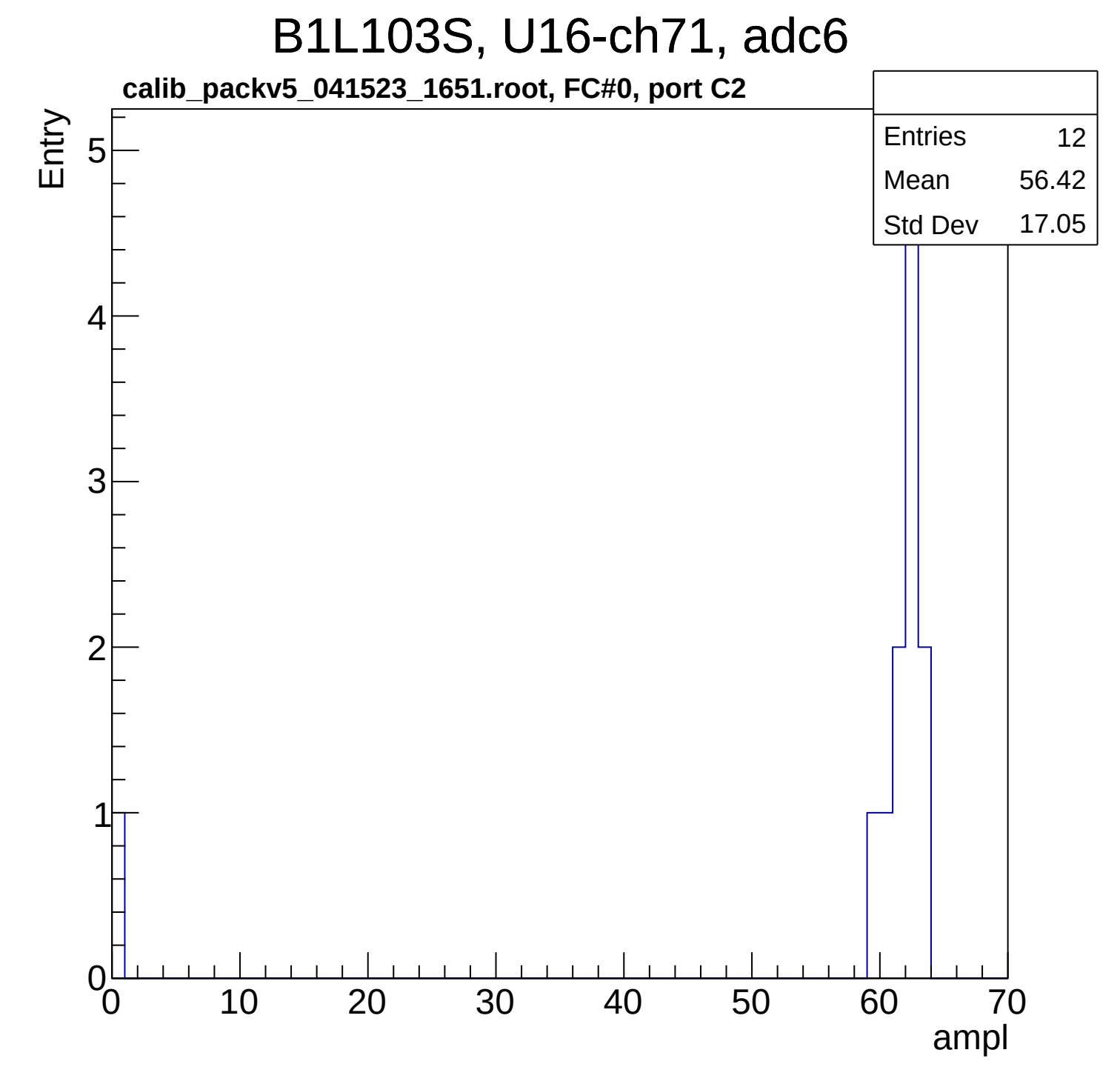
B1L103S, U16-ch71, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.42
Std Dev 17.05
Entry
ampl
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2
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4
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0
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60
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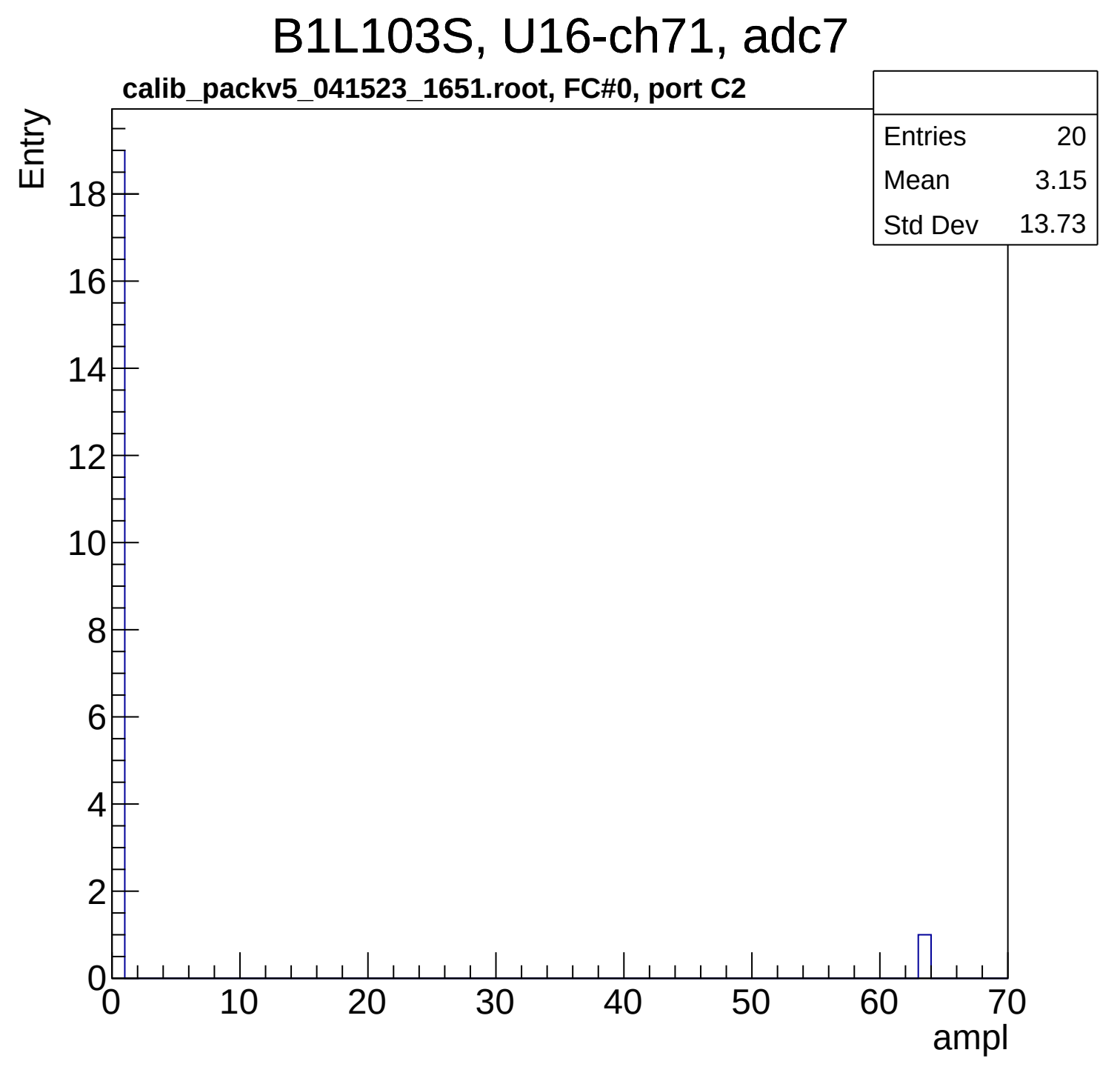
B1L103S, U16-ch71, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
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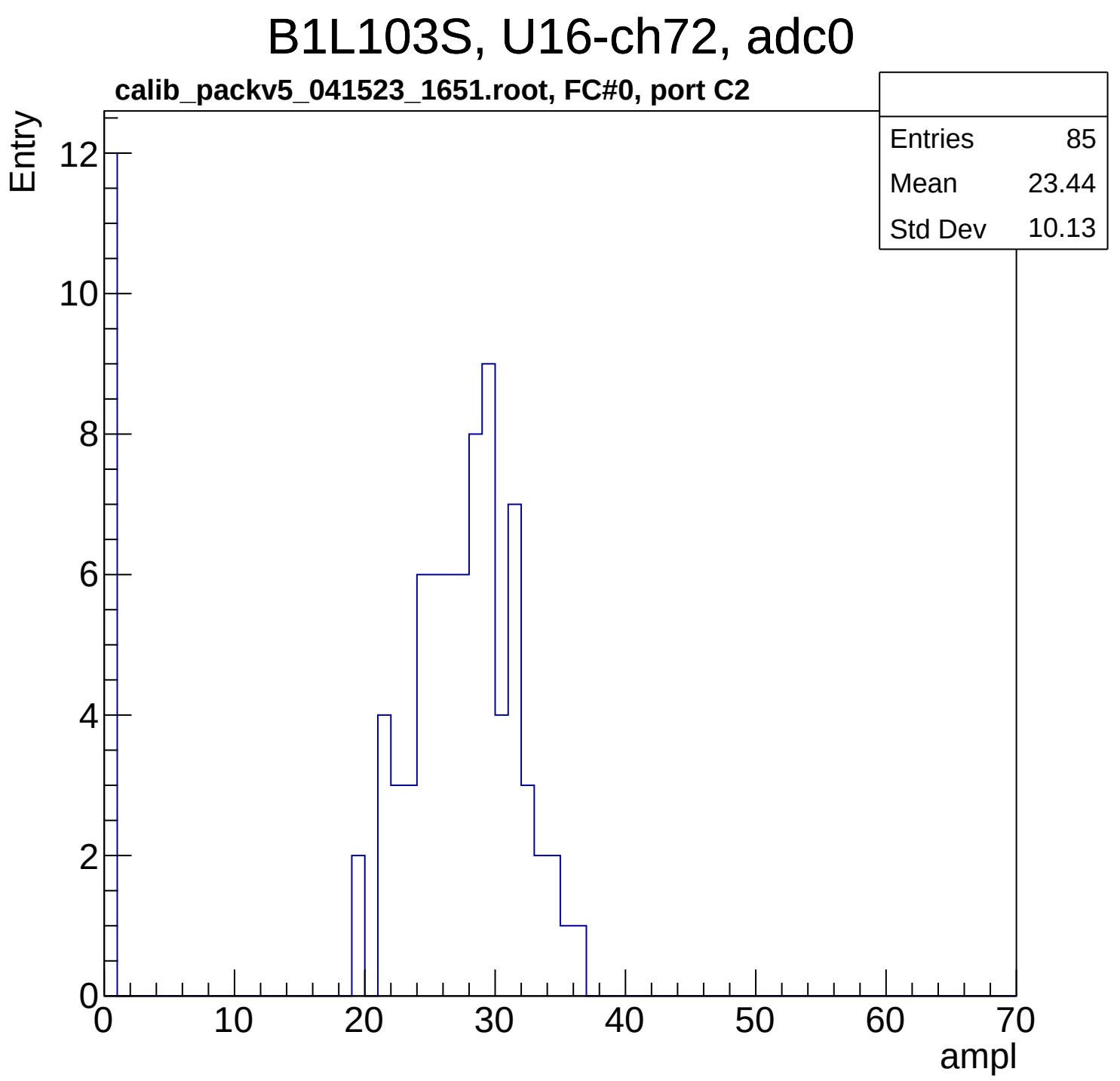
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch72, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 23.44
Std Dev 10.13
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
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60
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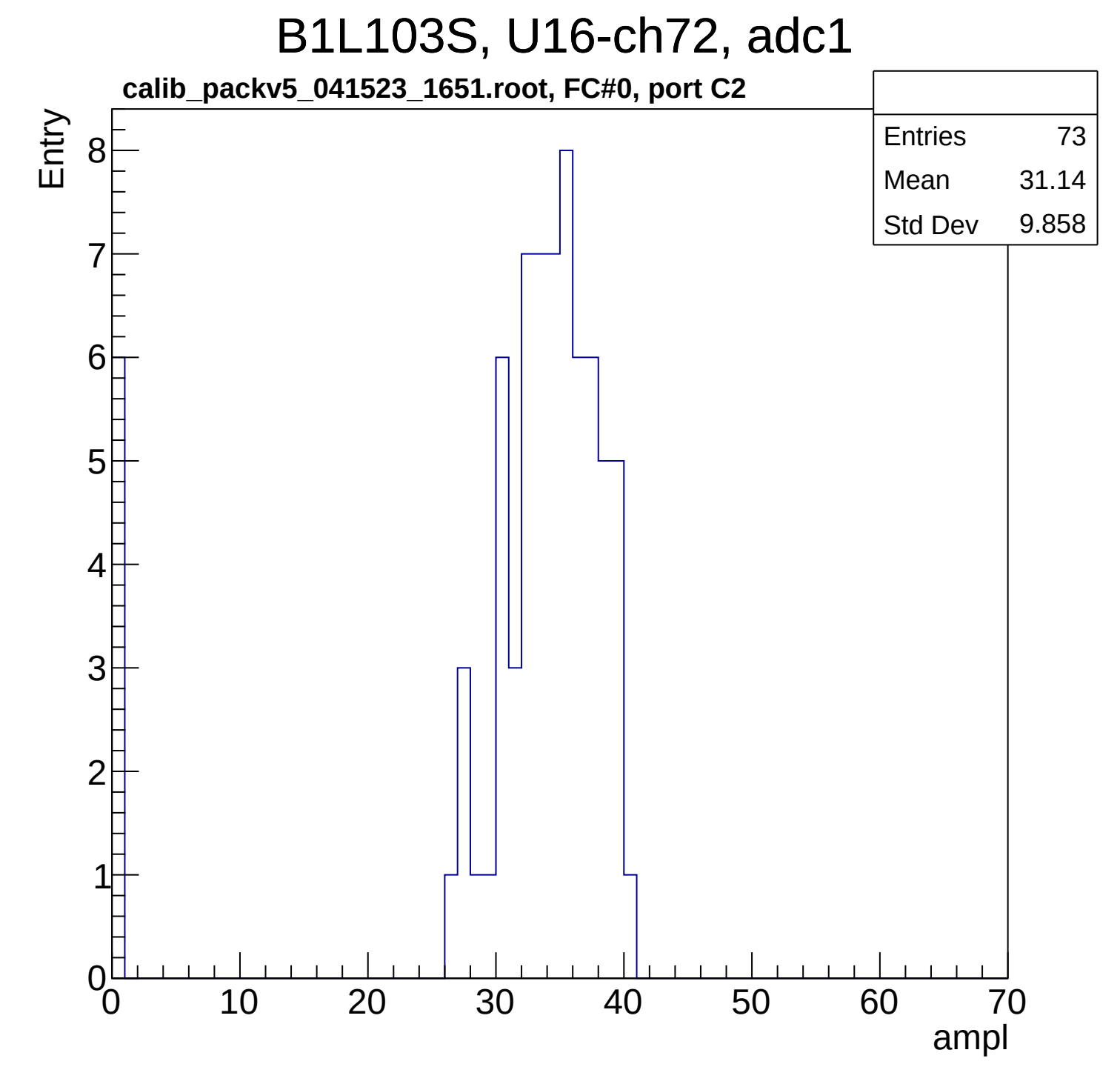
B1L103S, U16-ch72, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 31.14
Std Dev 9.858
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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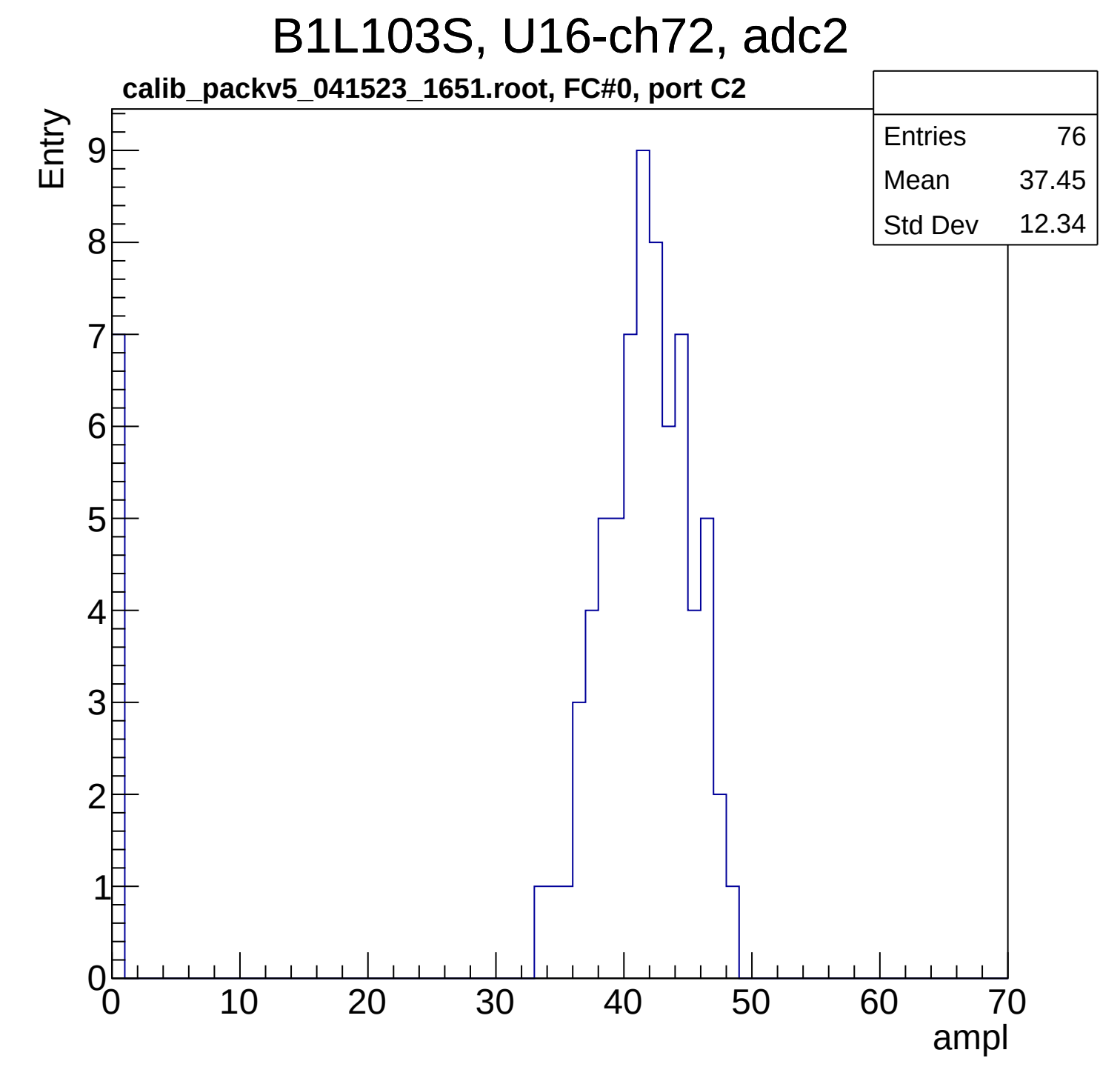
B1L103S, U16-ch72, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 37.45
Std Dev 12.34
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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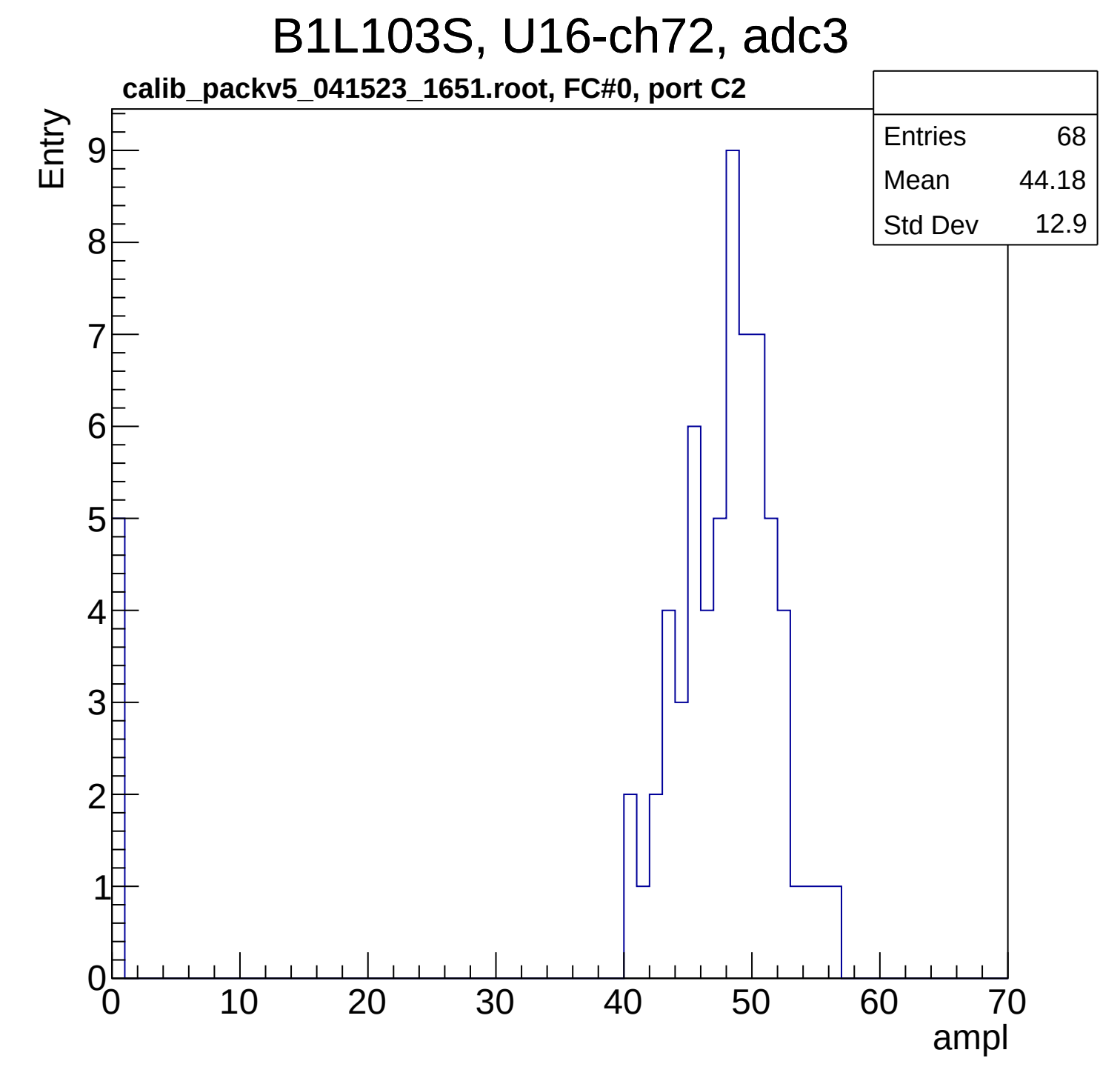
B1L103S, U16-ch72, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 44.18
Std Dev 12.9
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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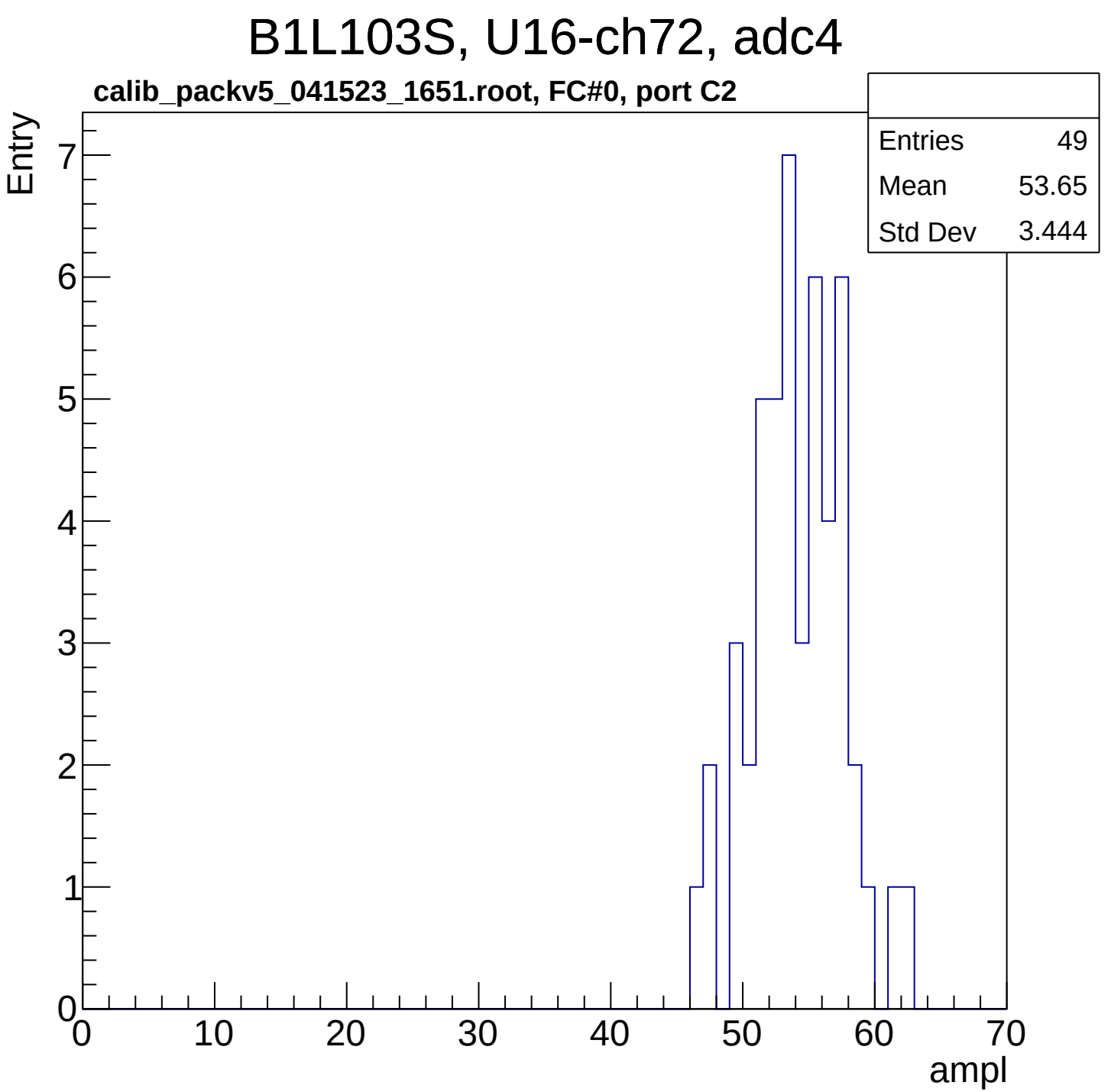
B1L103S, U16-ch72, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 53.65
Std Dev 3.444
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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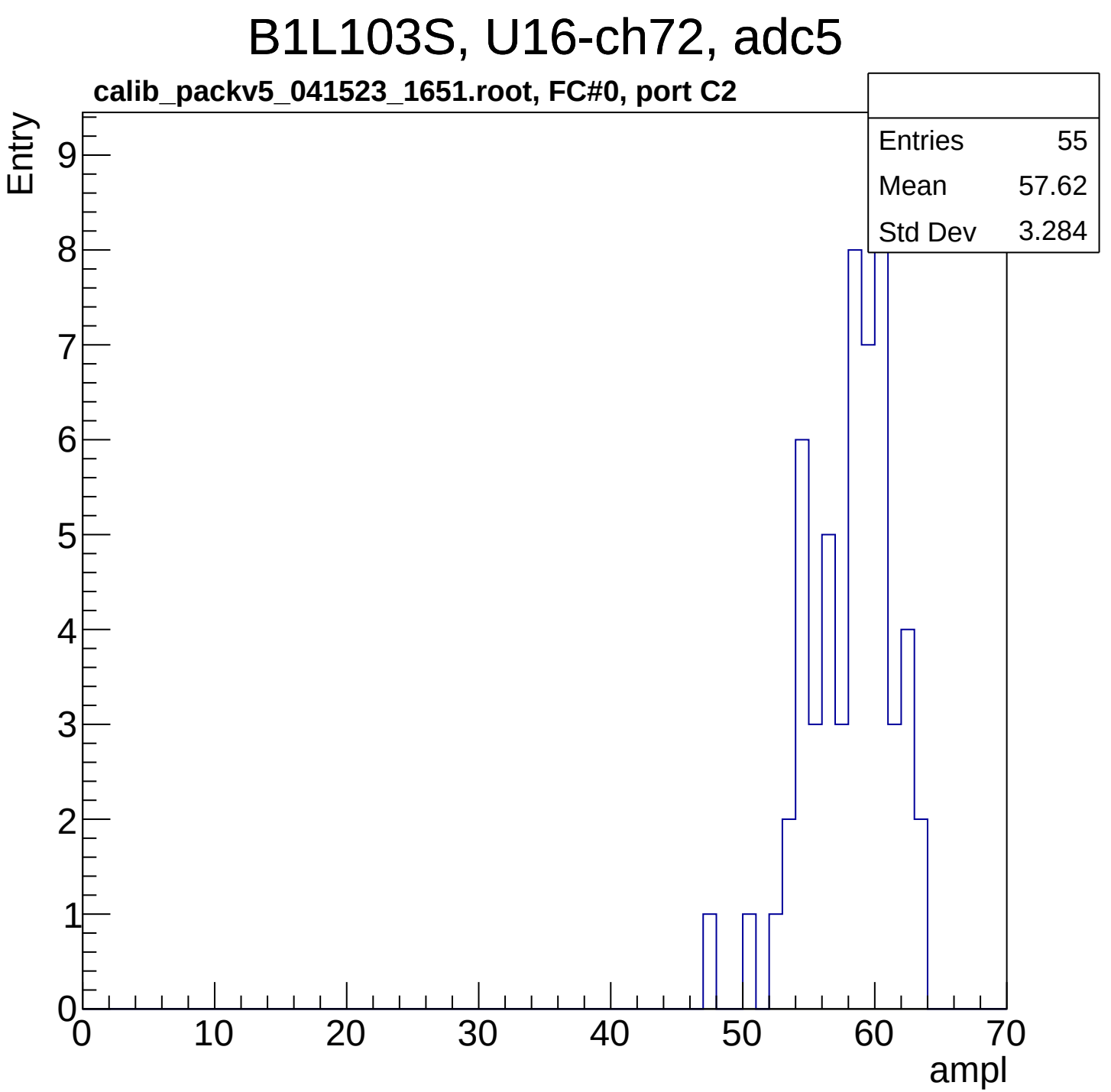
B1L103S, U16-ch72, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.62
Std Dev 3.284
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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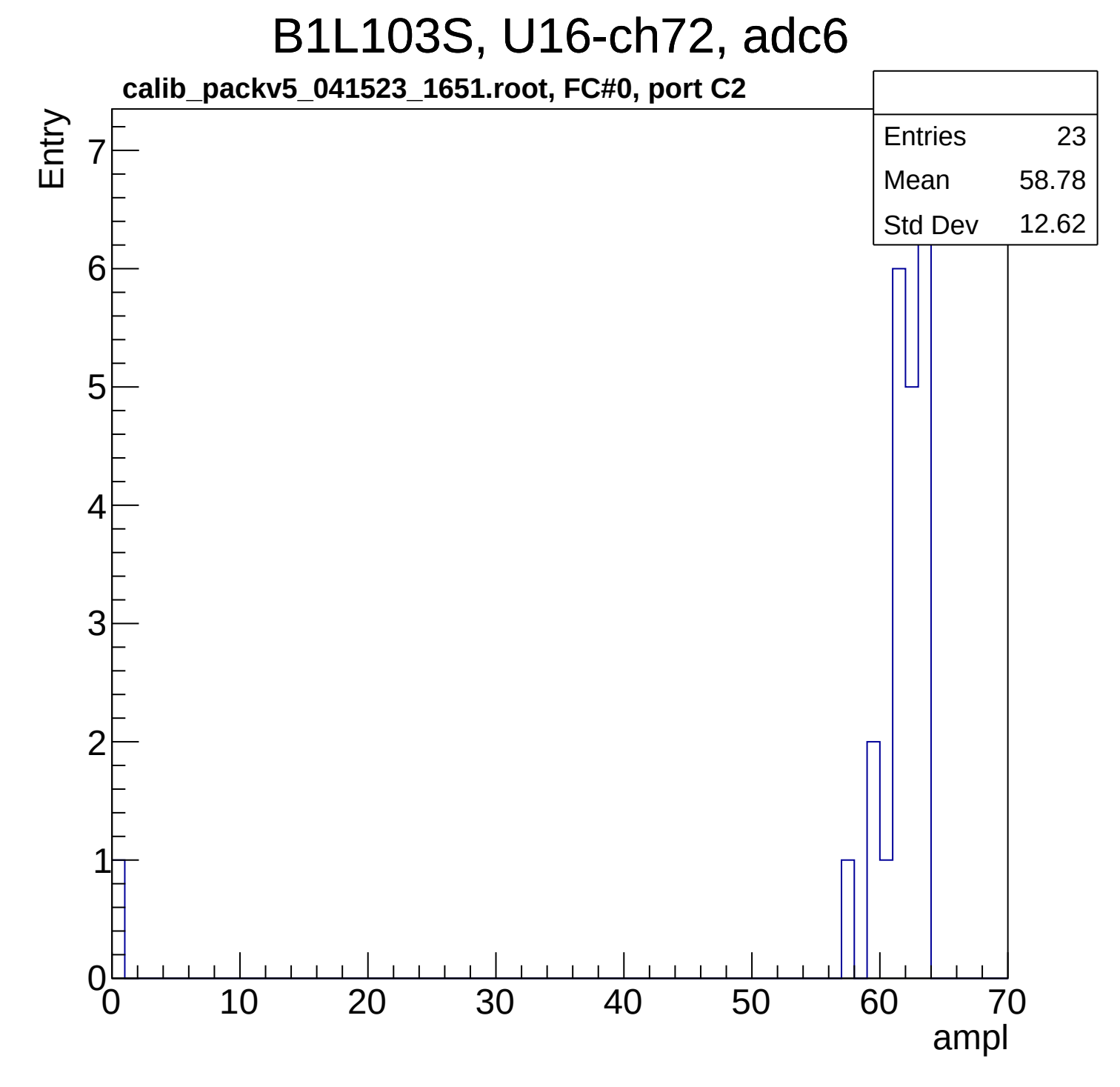
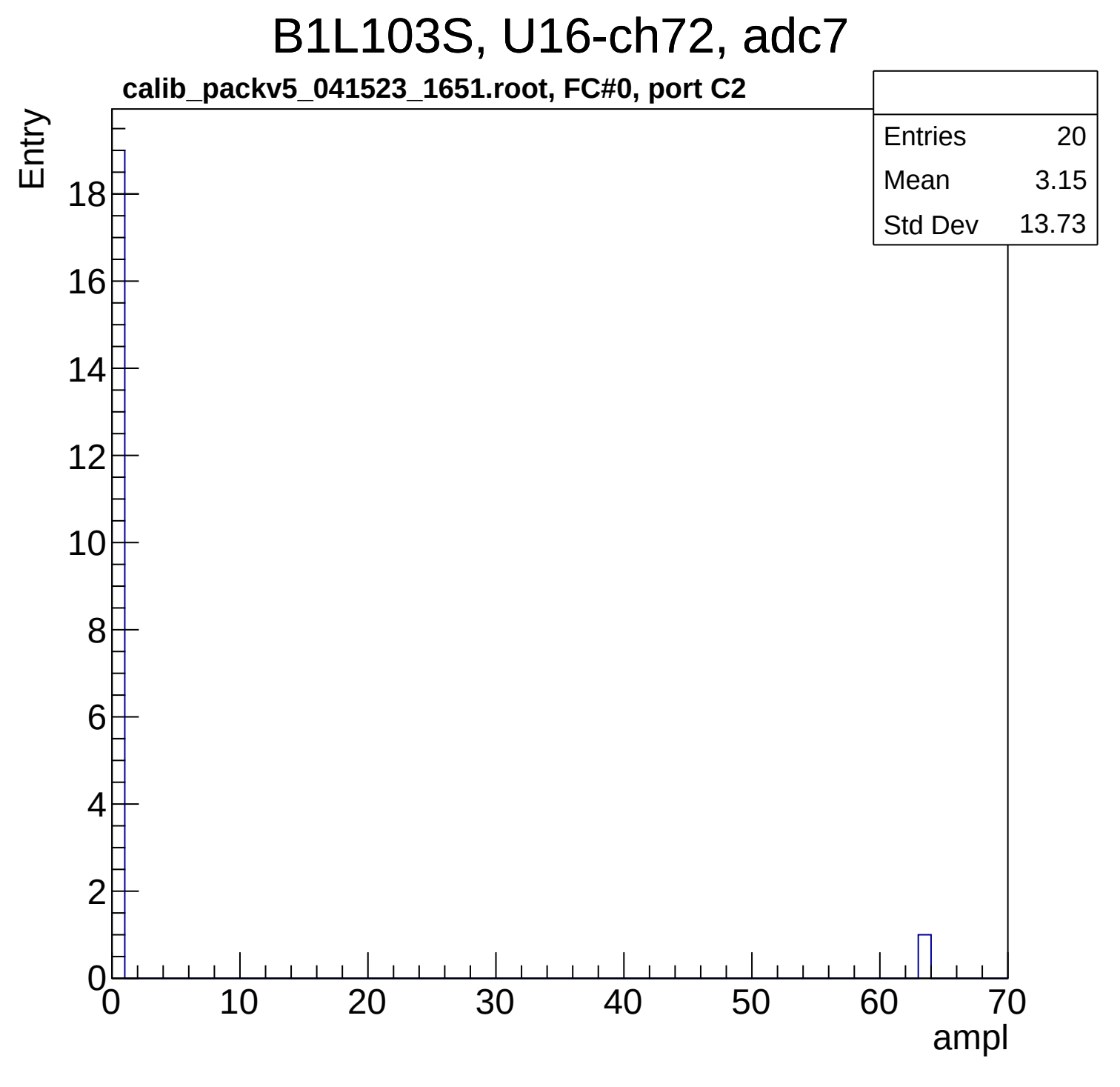
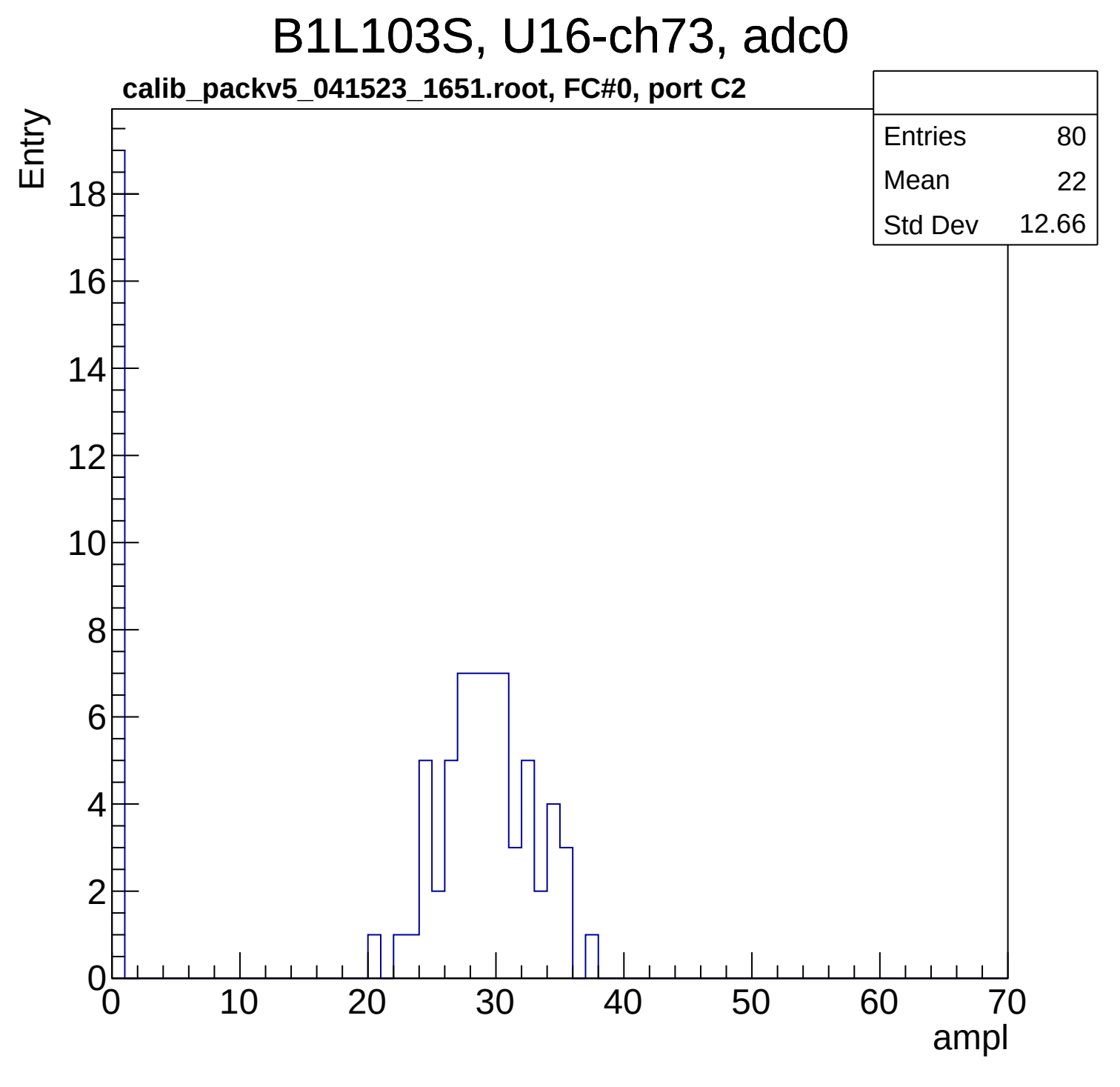
60
70


B1L103S, U16-ch72, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 58.78
Std Dev 12.62
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch72, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch73, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 22
Std Dev 12.66
Entry
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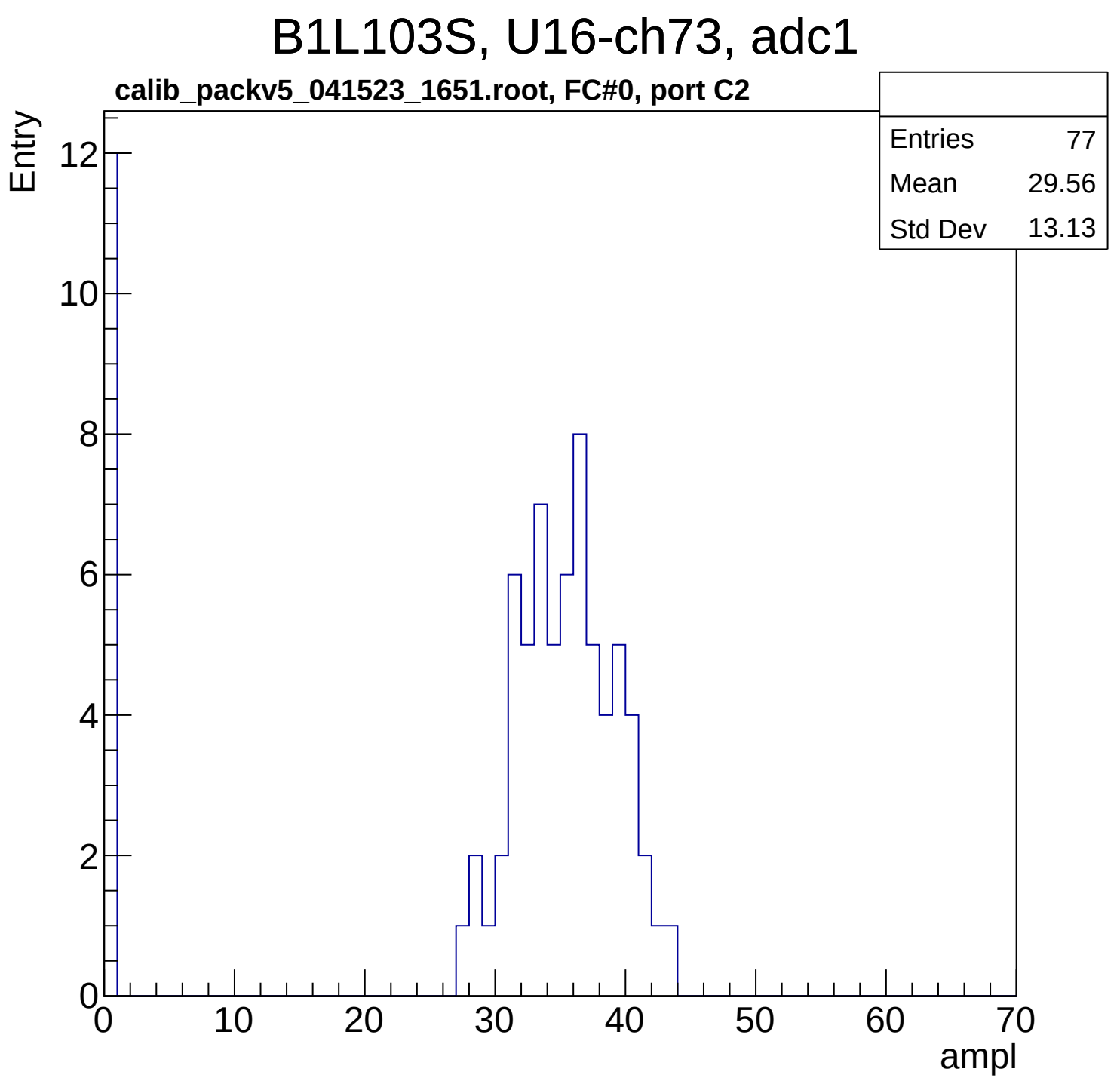
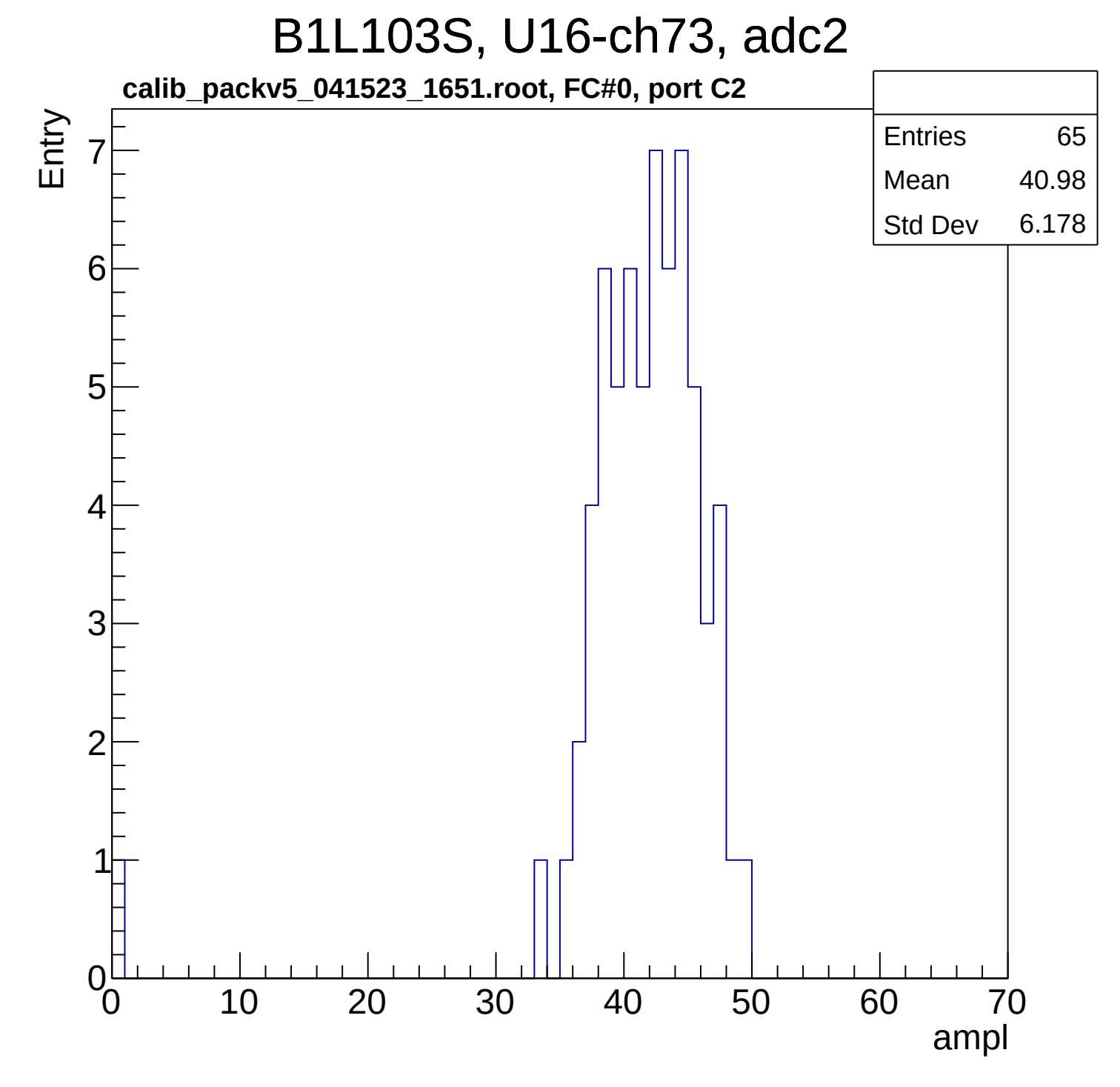
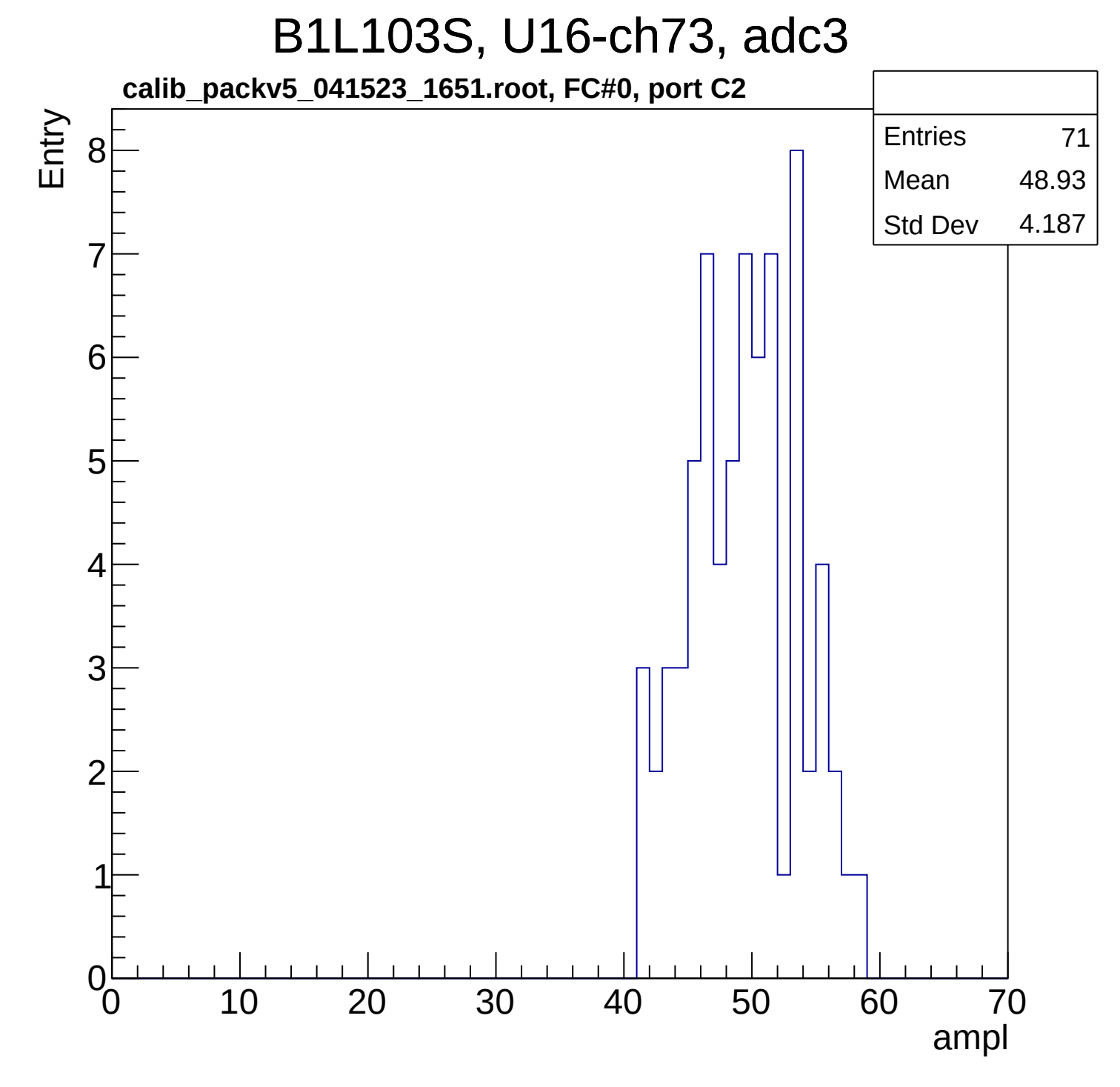
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch73, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 29.56
Std Dev 13.13
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch73, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 40.98
Std Dev 6.178
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch73, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 48.93
Std Dev 4.187
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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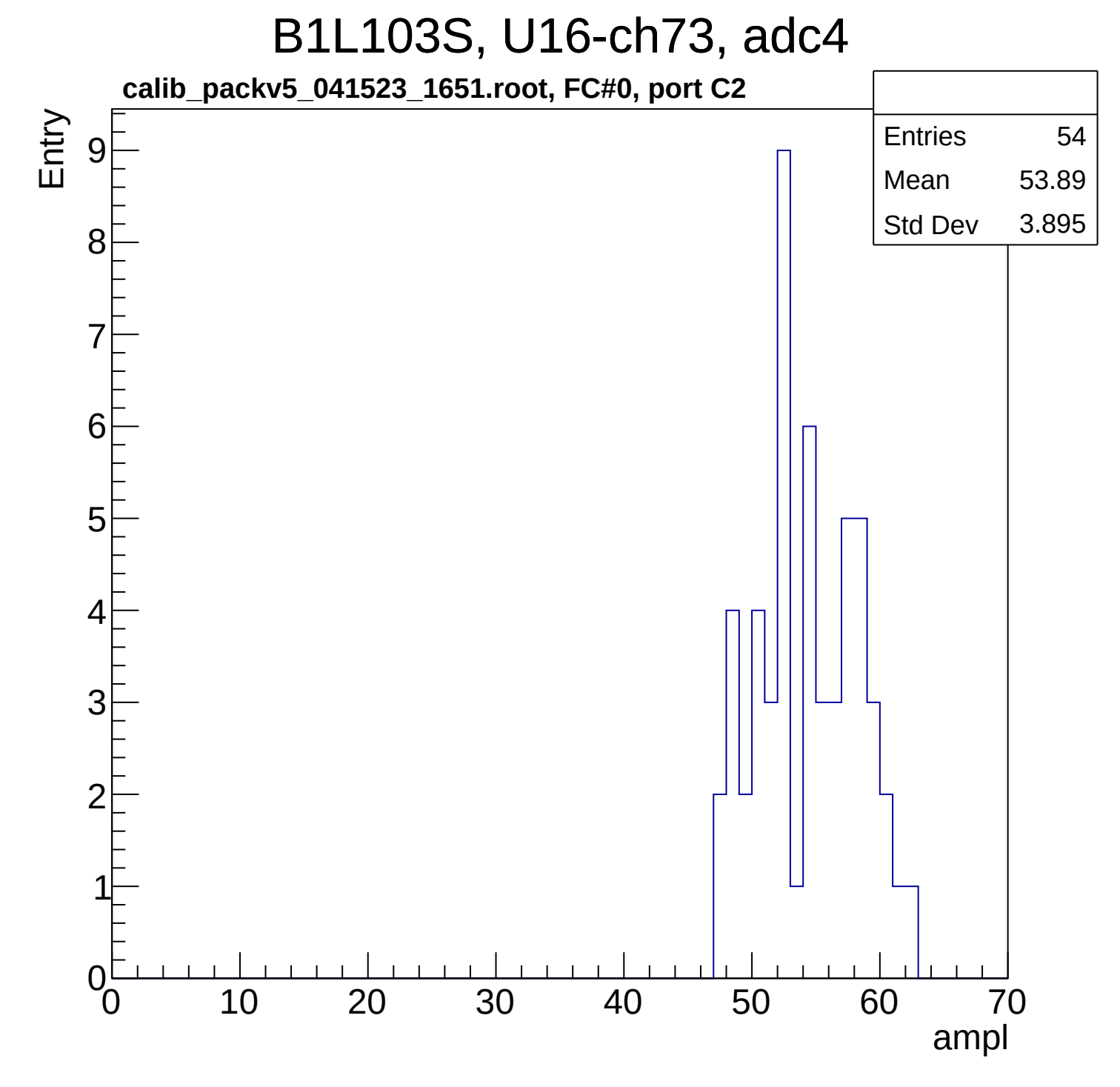
B1L103S, U16-ch73, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 53.89
Std Dev 3.895
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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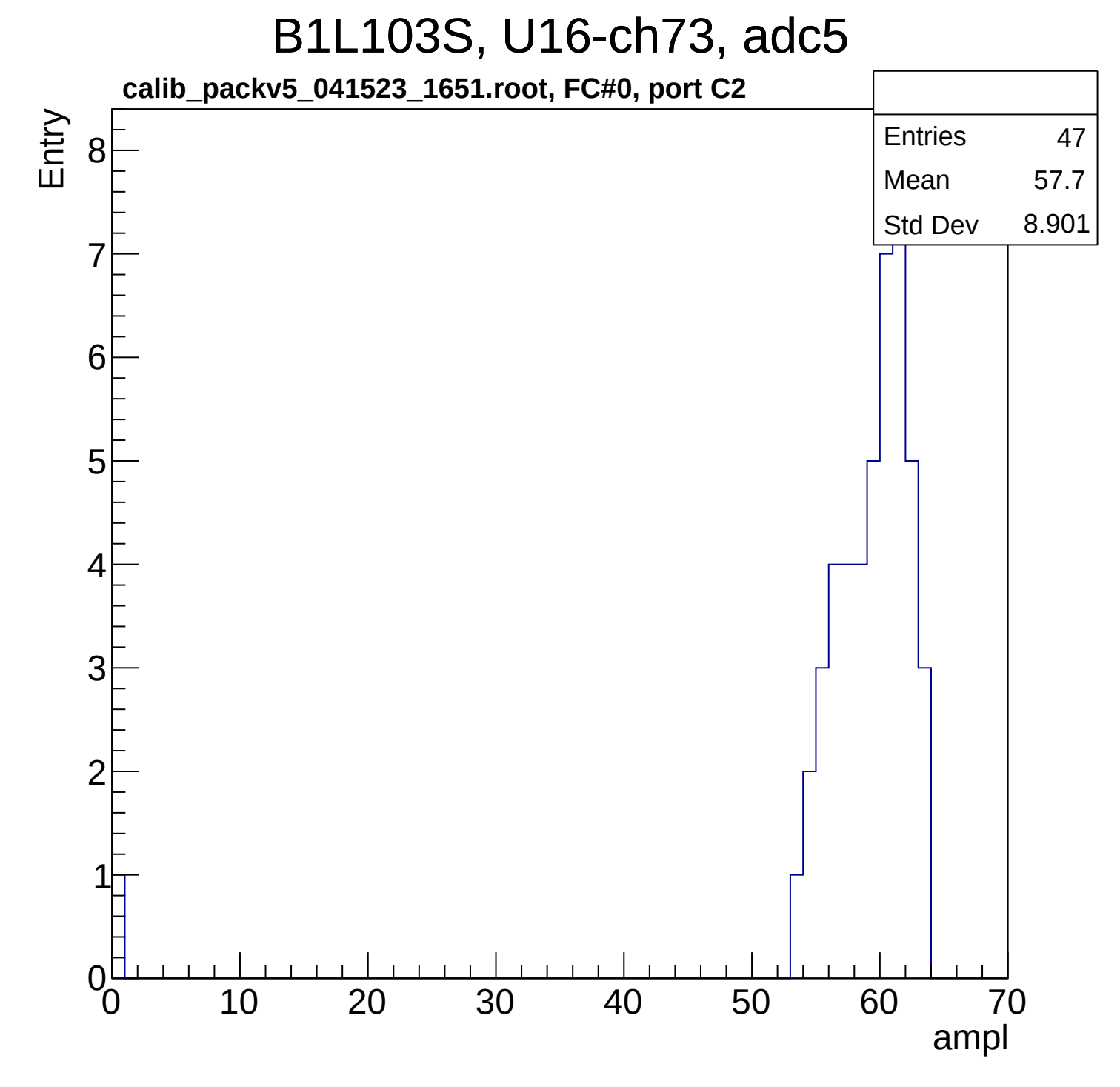
B1L103S, U16-ch73, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 57.7
Std Dev 8.901
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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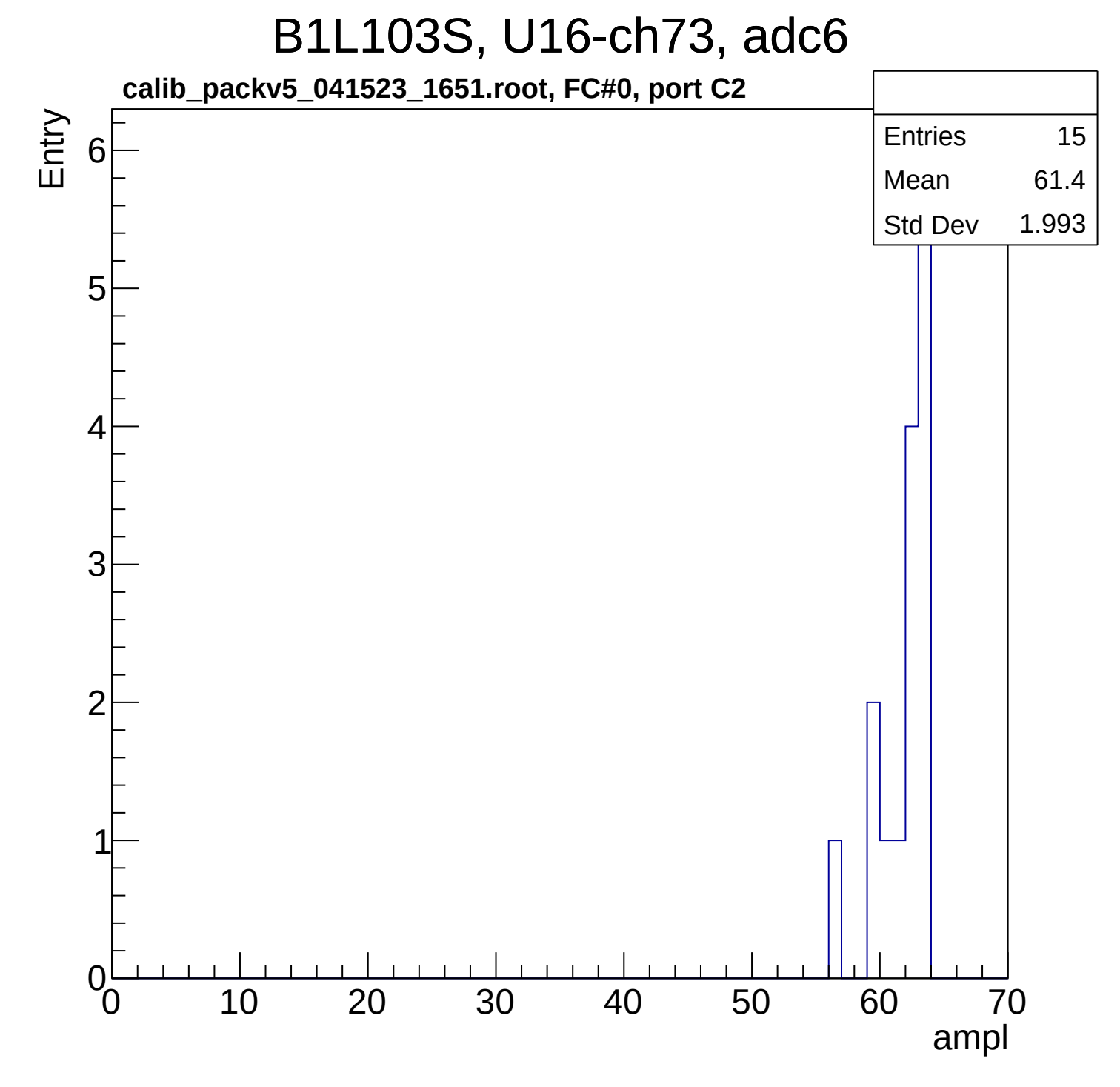
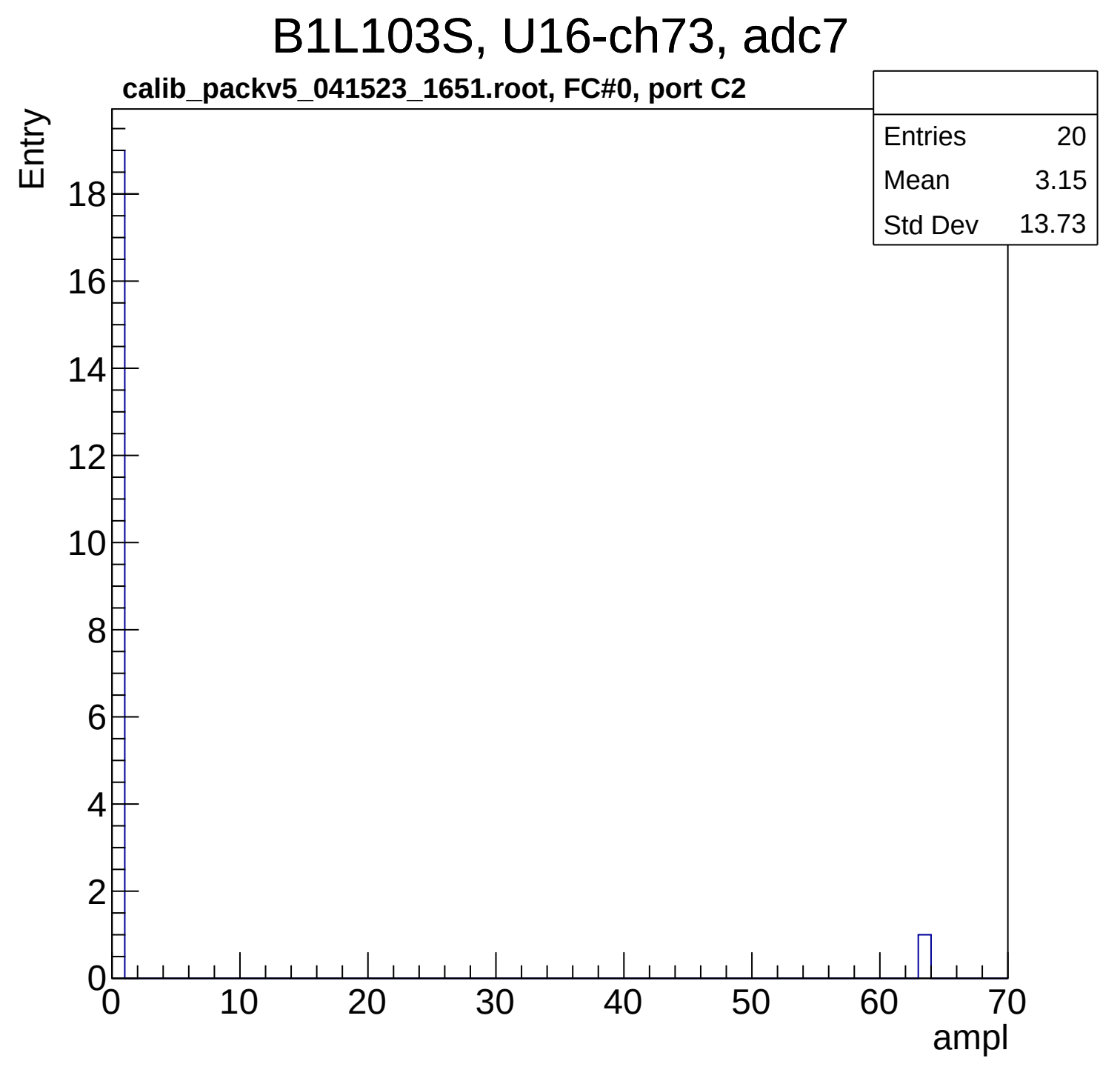
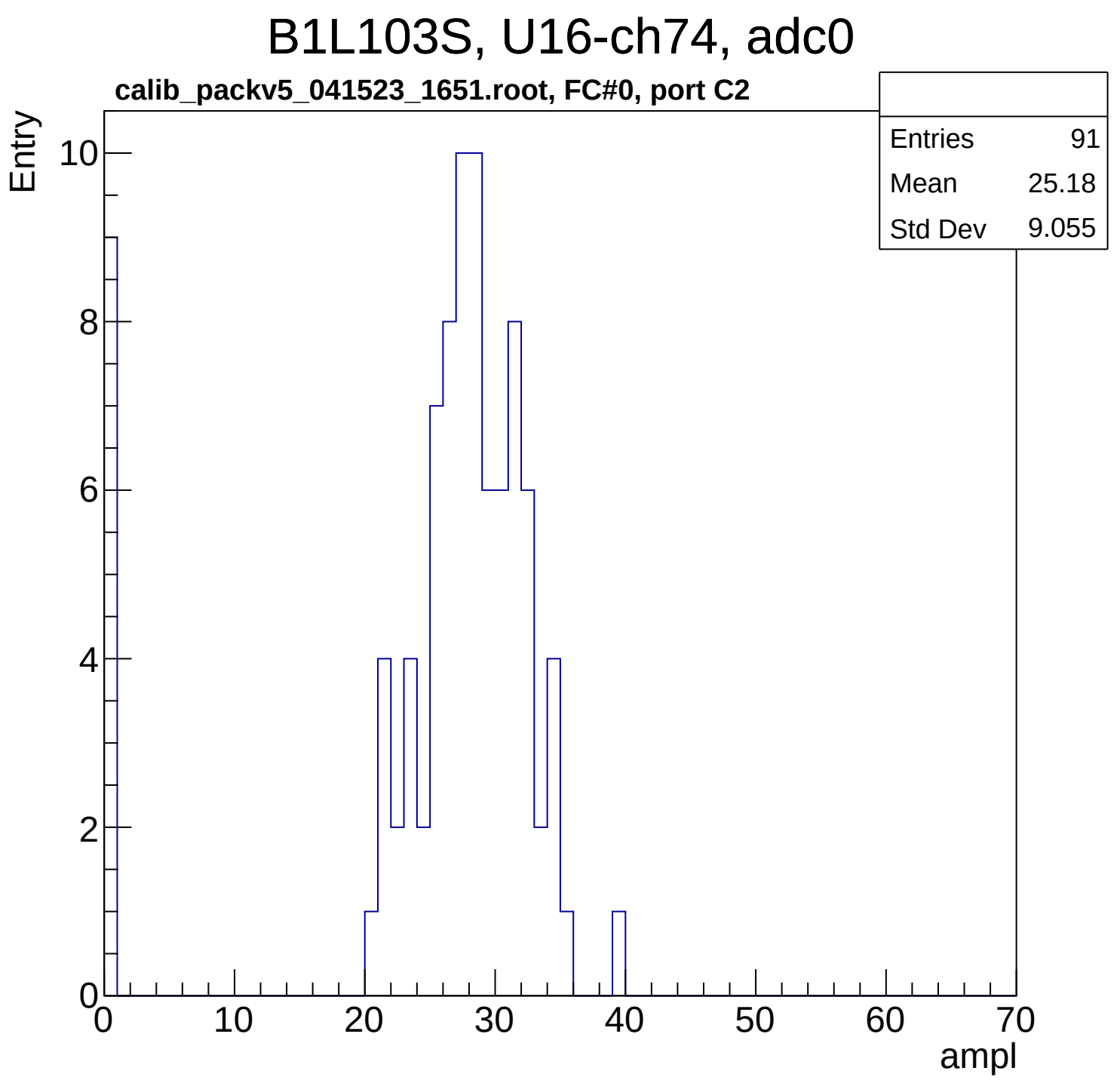

B1L103S, U16-ch73, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.4
Std Dev 1.993
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U16-ch73, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch74, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 25.18
Std Dev 9.055
Entry
ampl
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2
4
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8
10
0
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20
30
40
50
60
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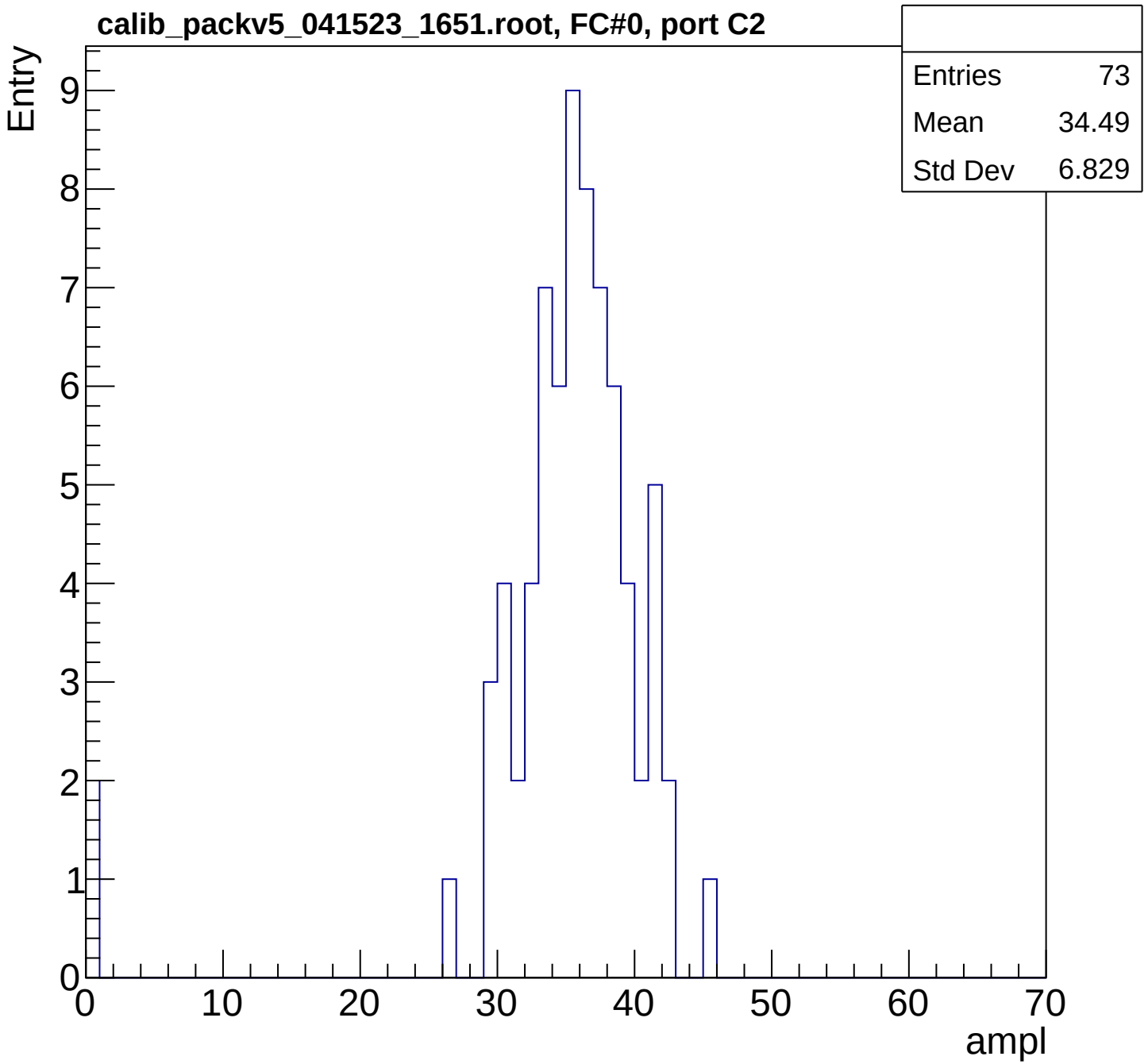
B1L103S, U16-ch74, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 34.49
Std Dev 6.829
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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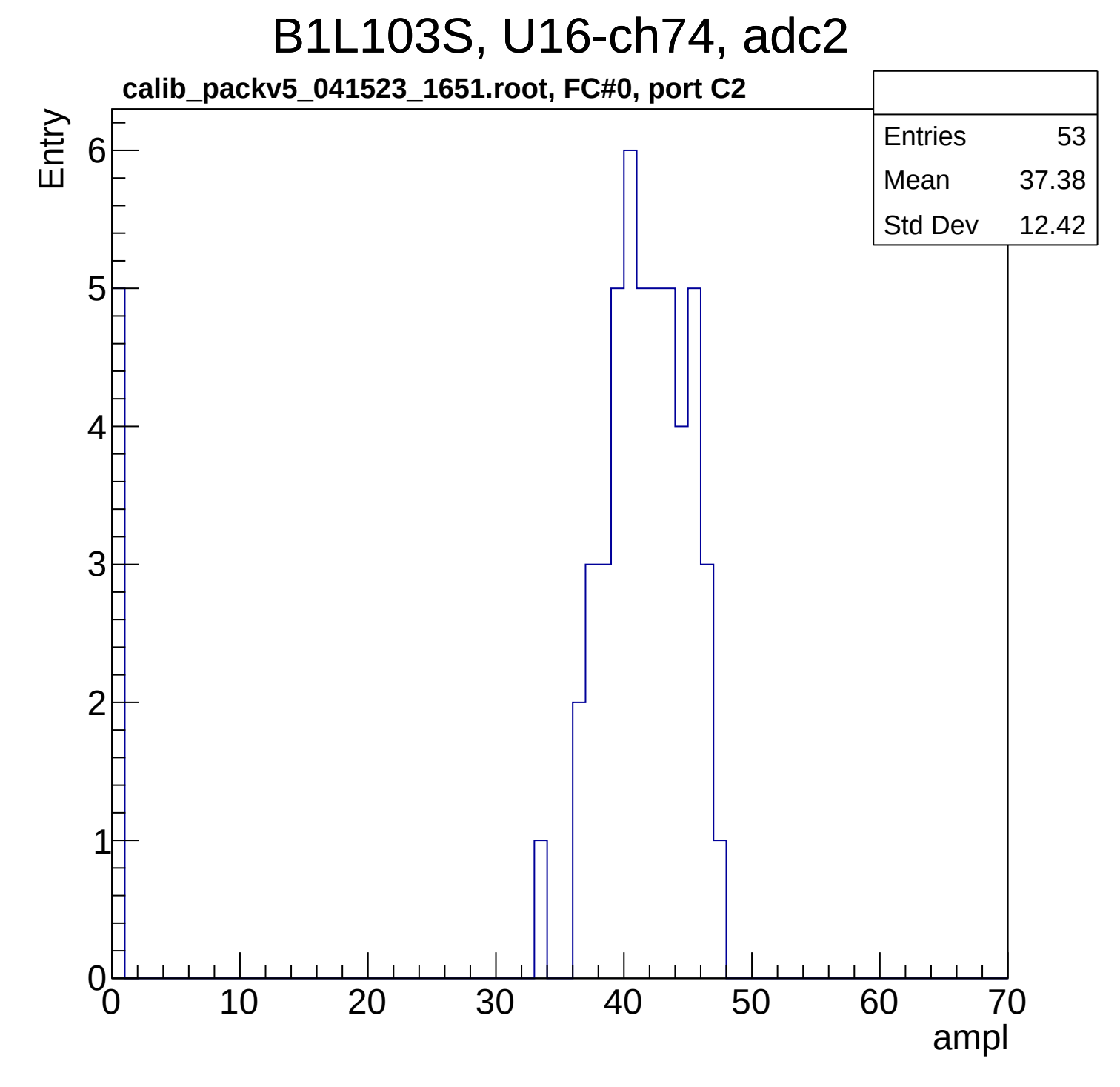
40
50
60
70


B1L103S, U16-ch74, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 37.38
Std Dev 12.42
Entry
0
1
2
3
4
5
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30
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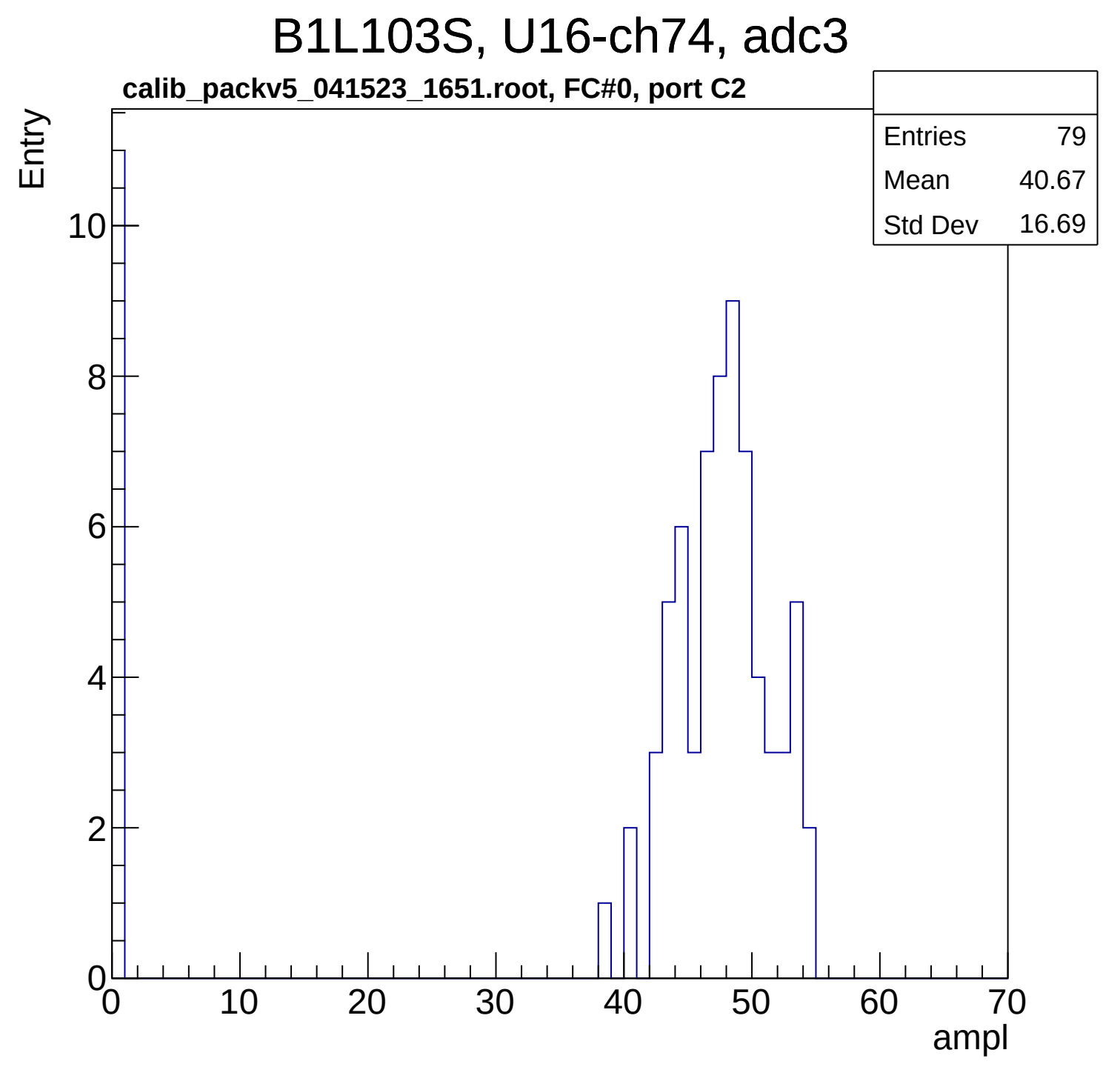
50
60
70
ampl


B1L103S, U16-ch74, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 40.67
Std Dev 16.69
Entry
0
2
4
6
8
10
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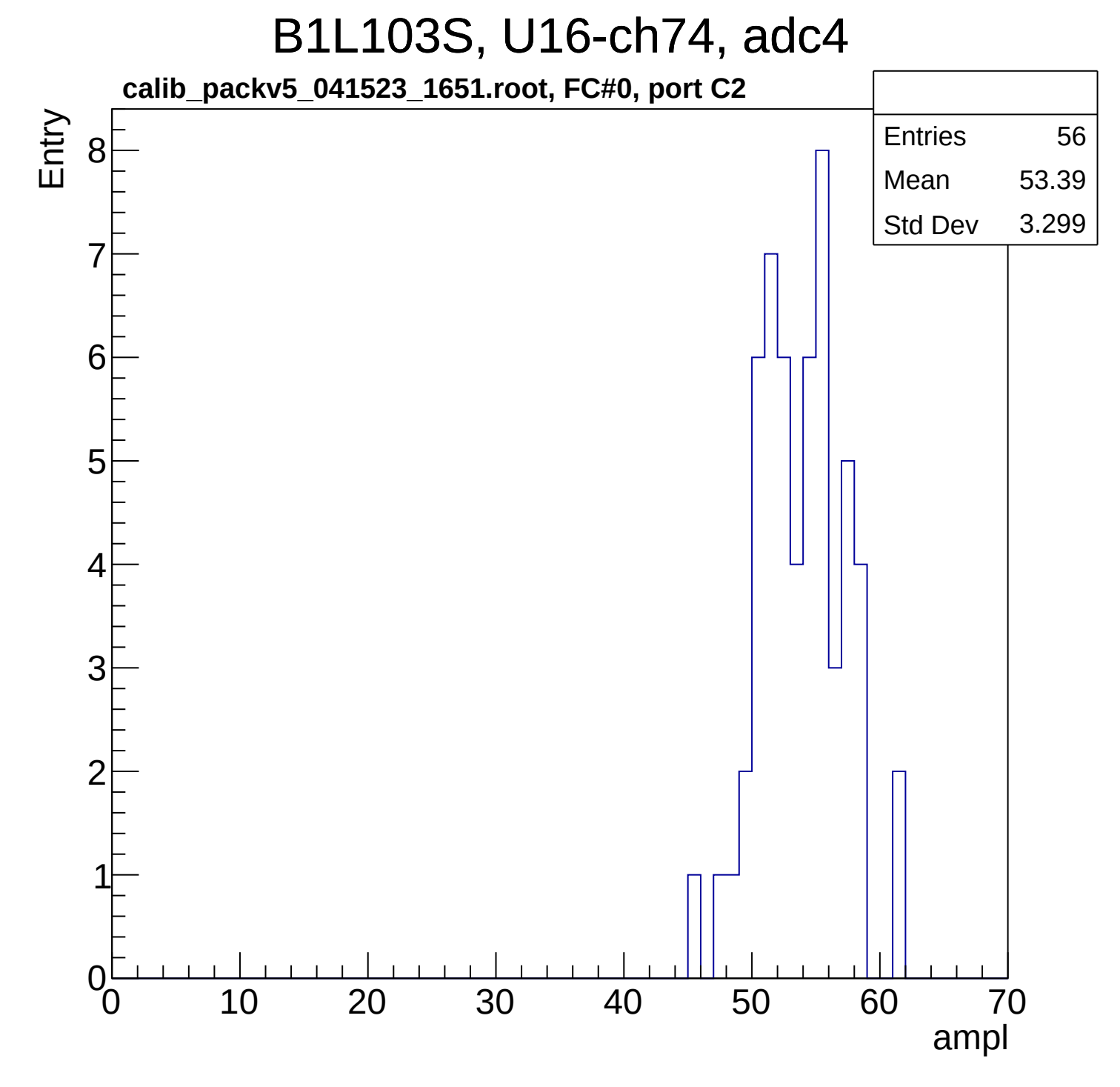
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch74, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 53.39
Std Dev 3.299
Entry
ampl
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1
2
3
4
5
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7
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0
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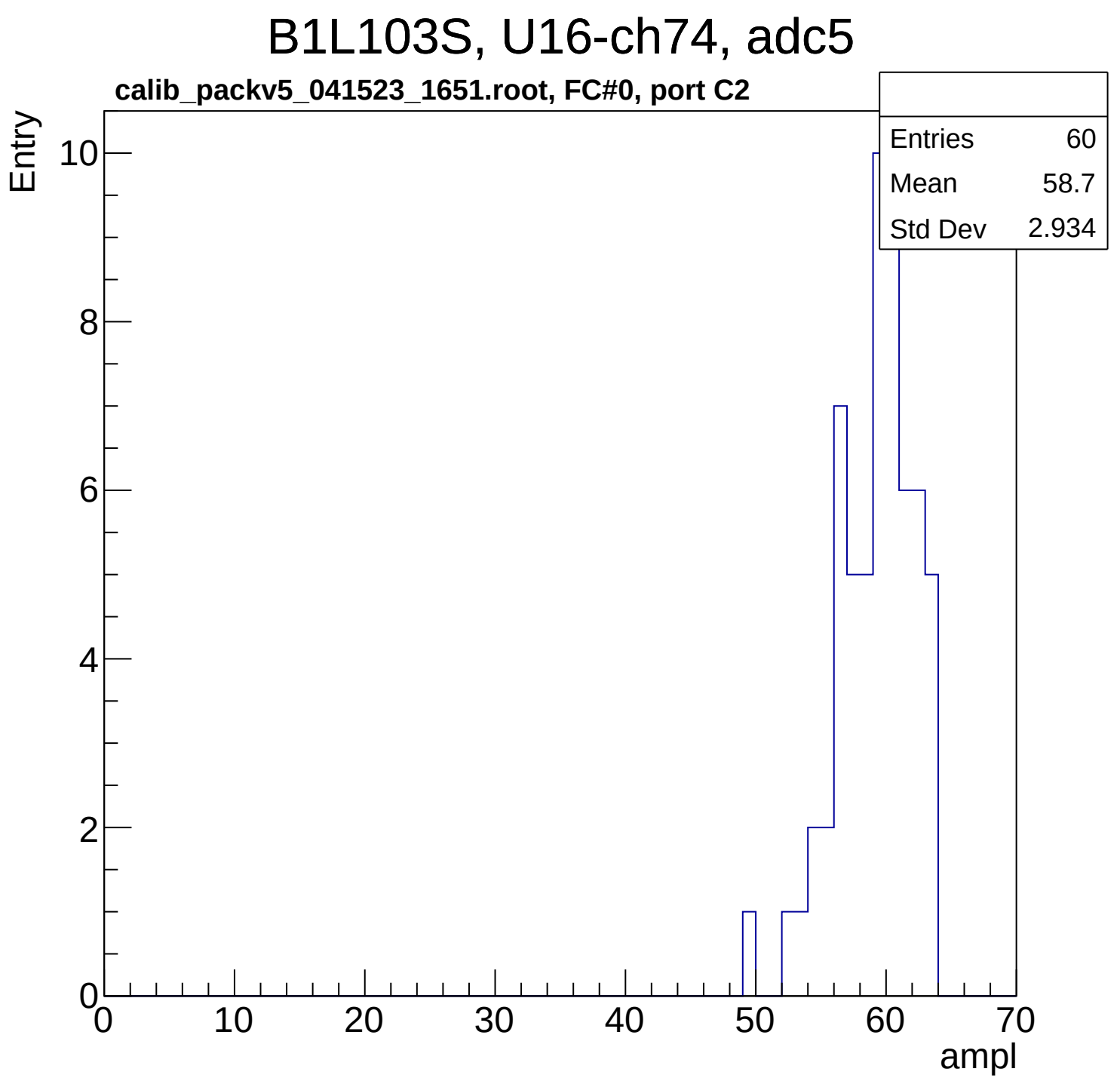
40
50
60
70


B1L103S, U16-ch74, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 58.7
Std Dev 2.934
Entry
ampl
0
2
4
6
8
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0
10
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40
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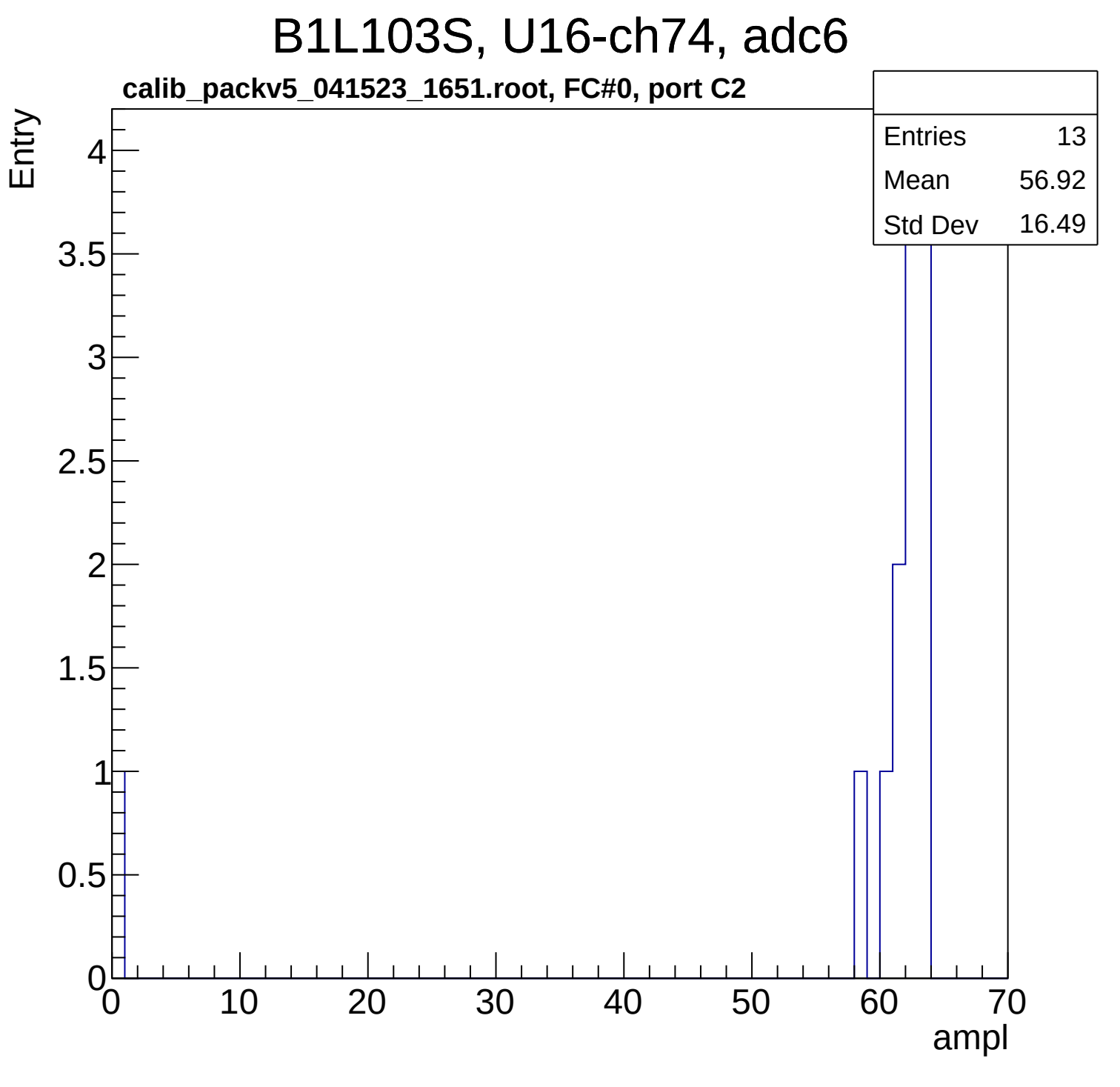
60
70


B1L103S, U16-ch74, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 56.92
Std Dev 16.49
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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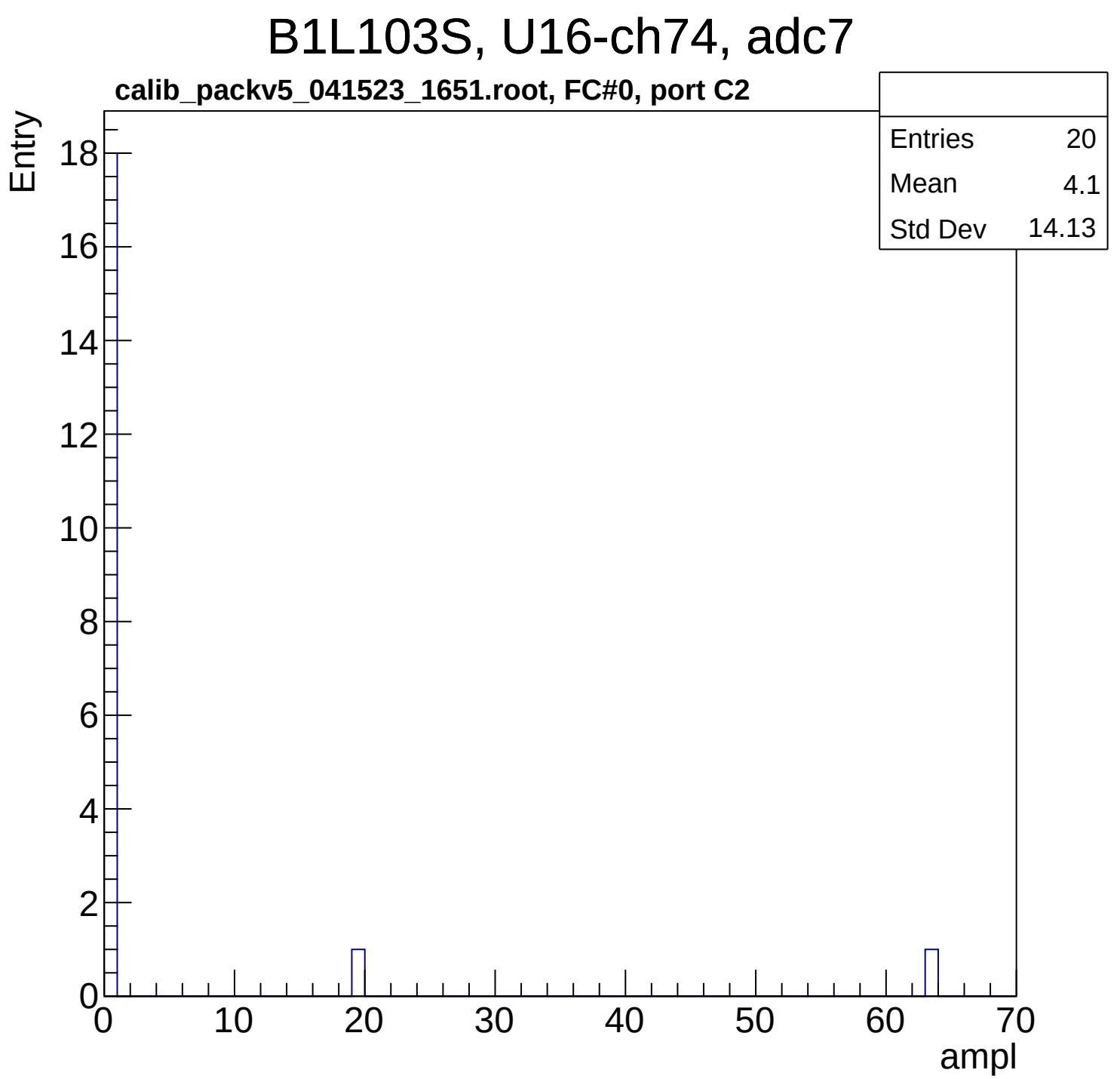
60
70


B1L103S, U16-ch74, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.1
Std Dev 14.13
Entry
0
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6
8
10
12
14
16
18
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10
20
30
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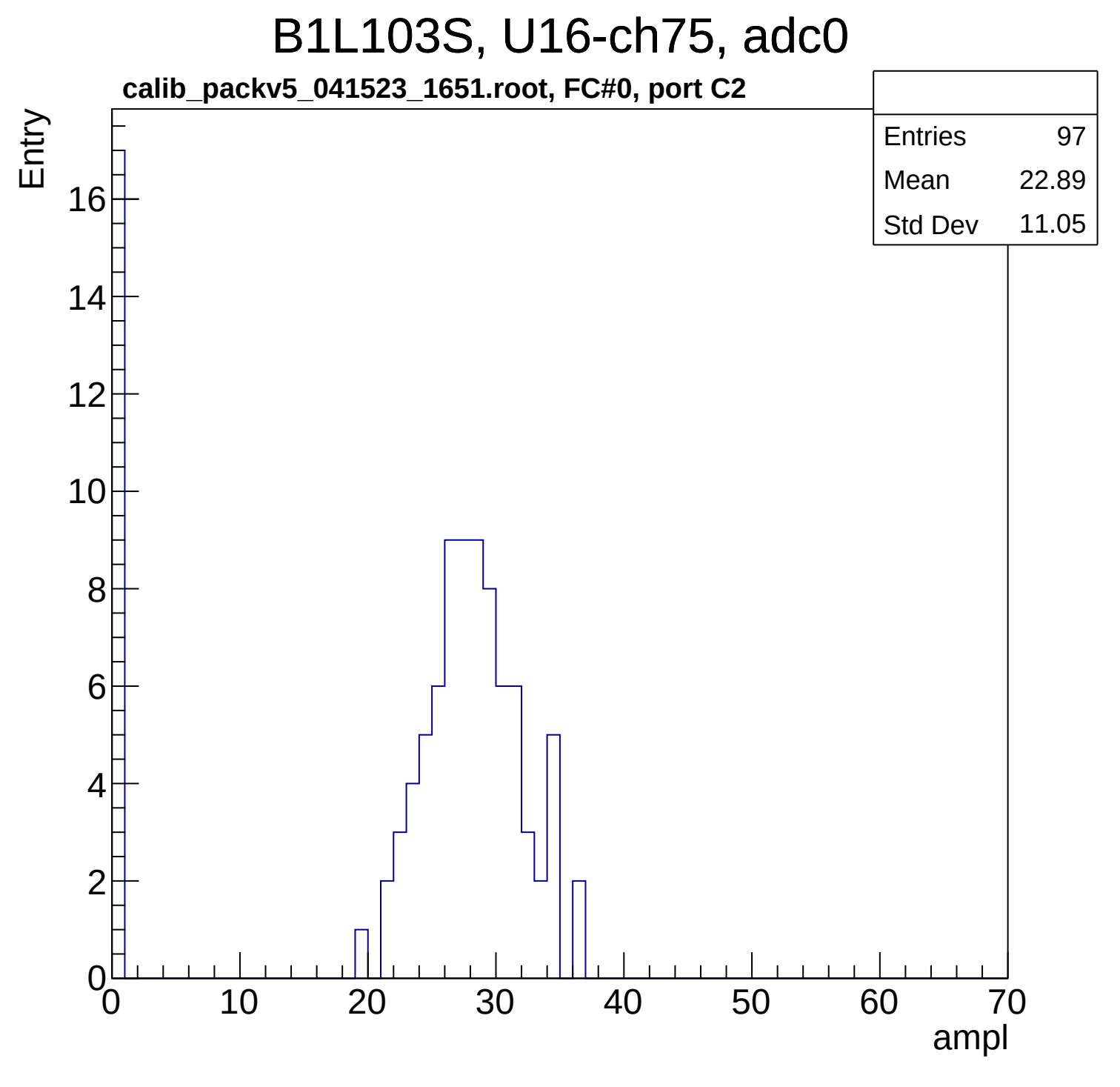
50
60
70
ampl


B1L103S, U16-ch75, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 22.89
Std Dev 11.05
Entry
ampl
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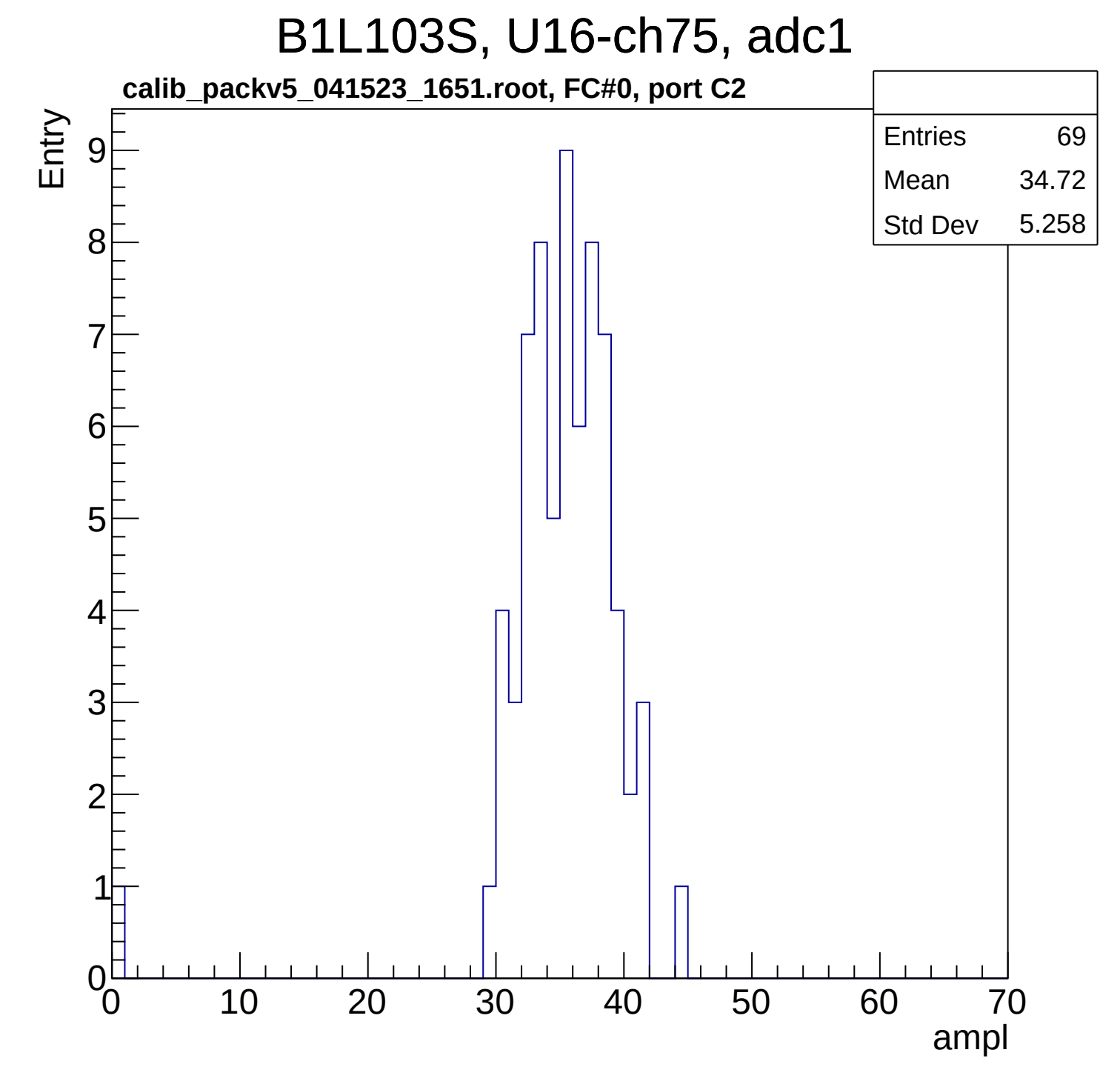
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U16-ch75, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 34.72
Std Dev 5.258
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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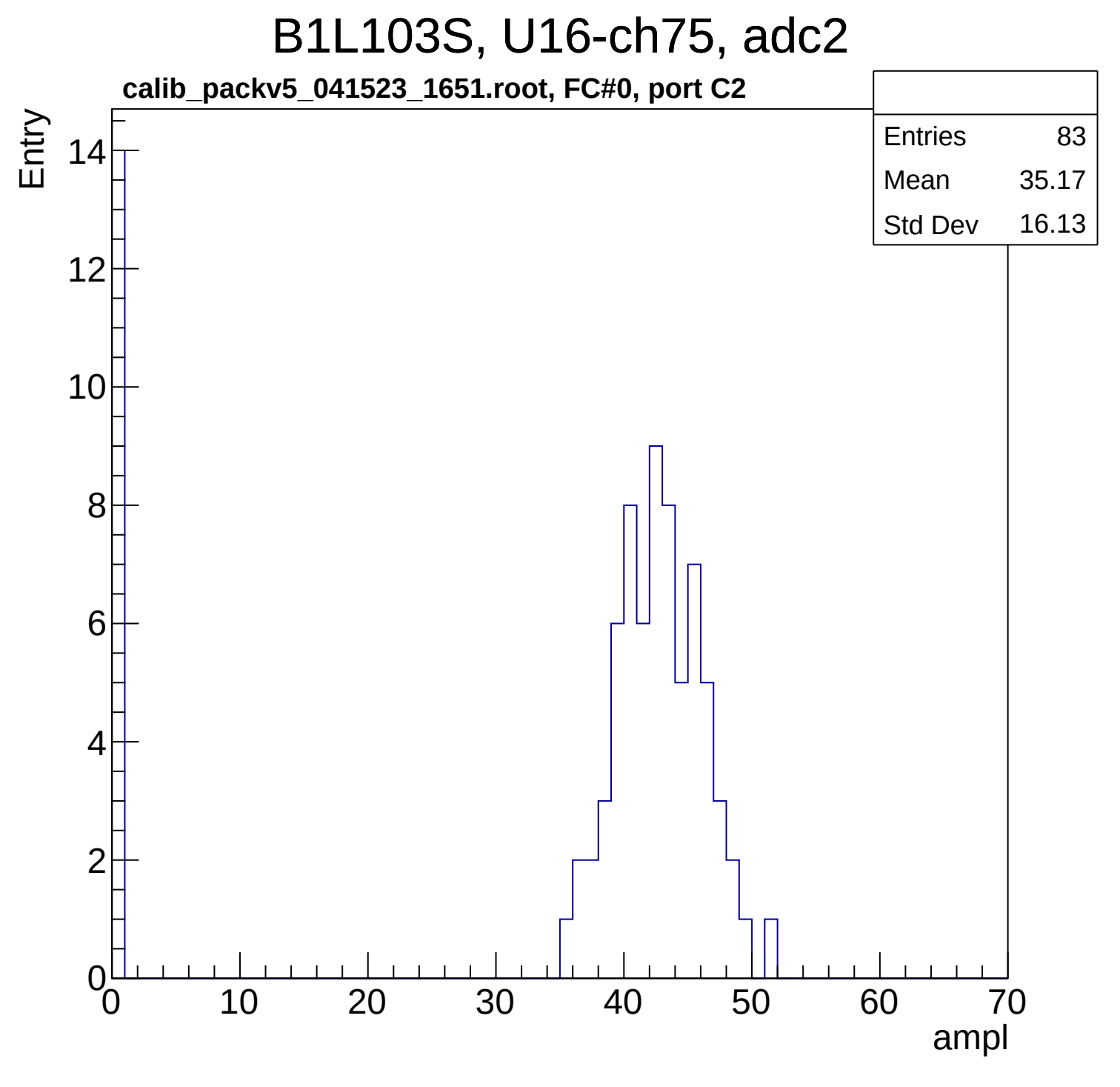
40
50
60
70


B1L103S, U16-ch75, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 35.17
Std Dev 16.13
Entry
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6
8
10
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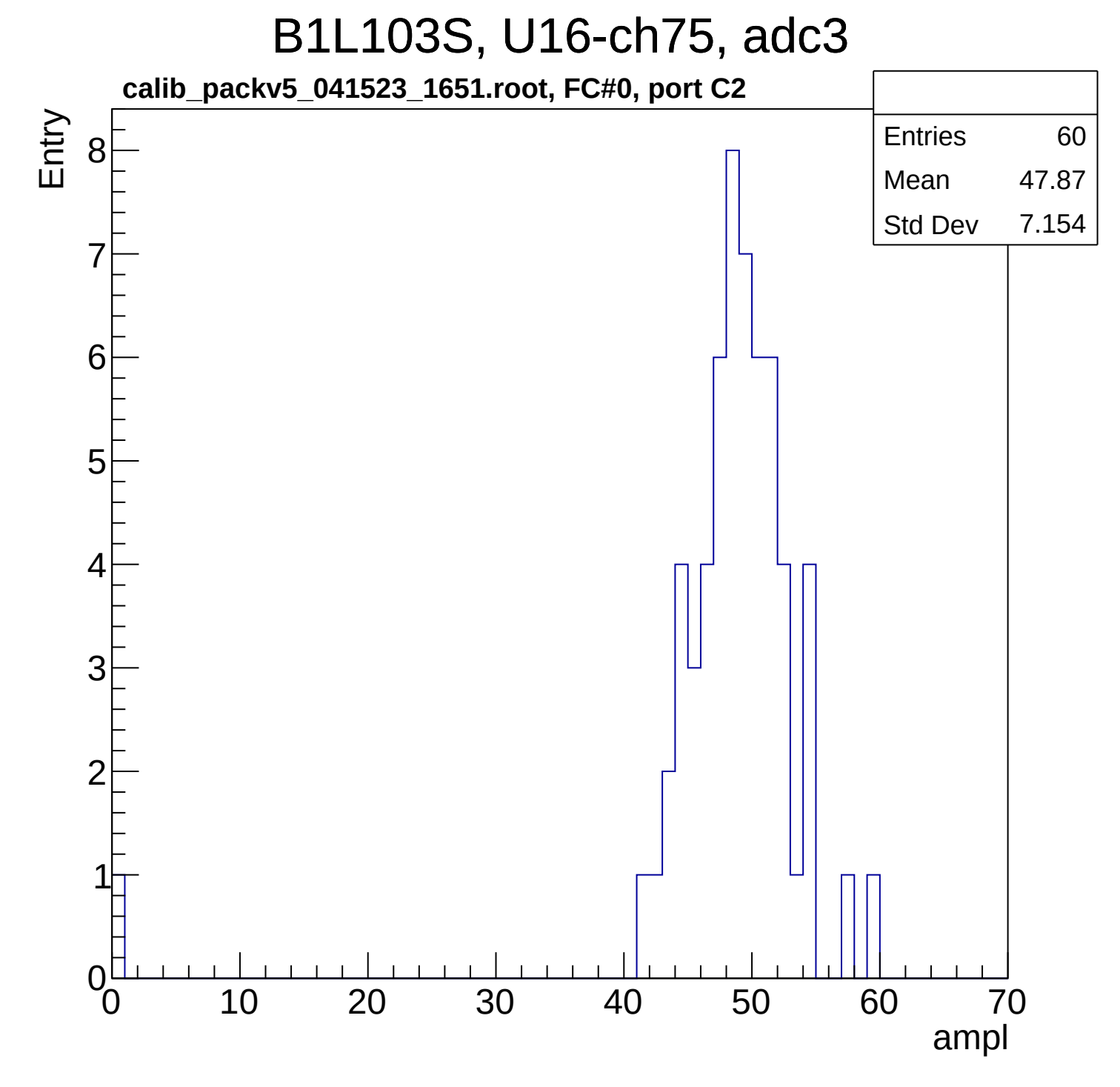
70
ampl


B1L103S, U16-ch75, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 47.87
Std Dev 7.154
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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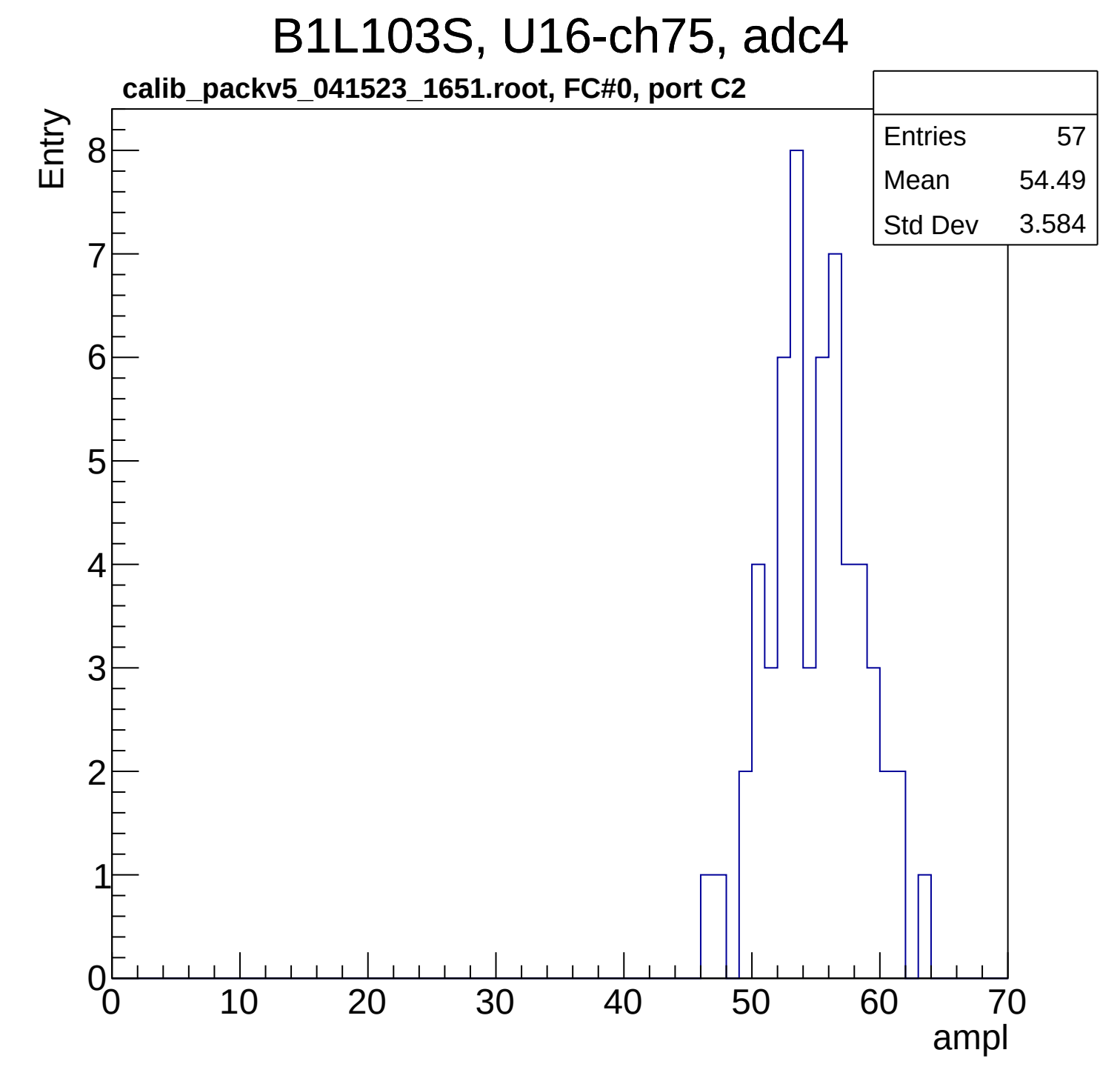
40
50
60
70


B1L103S, U16-ch75, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 54.49
Std Dev 3.584
Entry
ampl
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1
2
3
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7
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0
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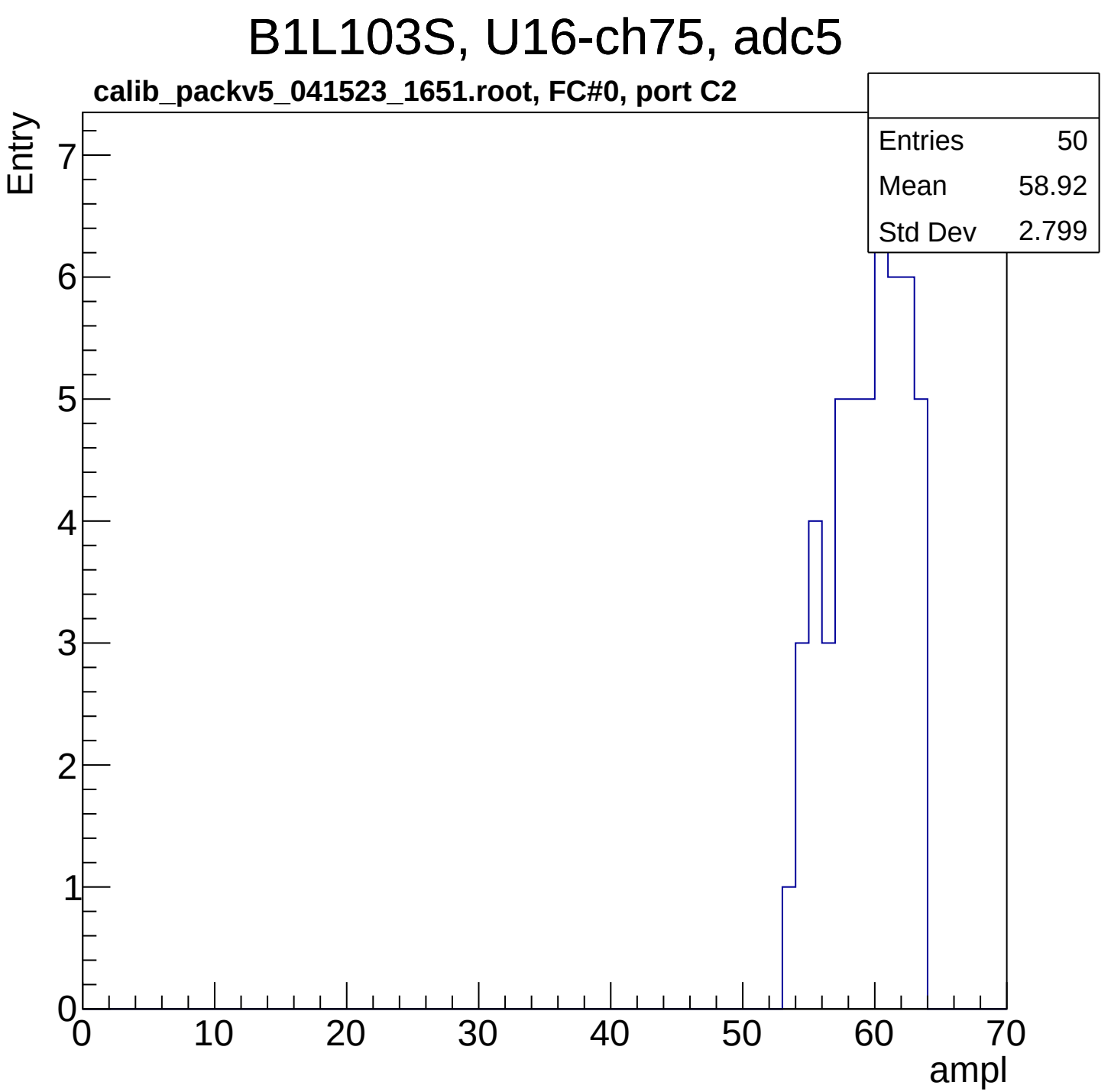
40
50
60
70


B1L103S, U16-ch75, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.92
Std Dev 2.799
Entry
ampl
0
1
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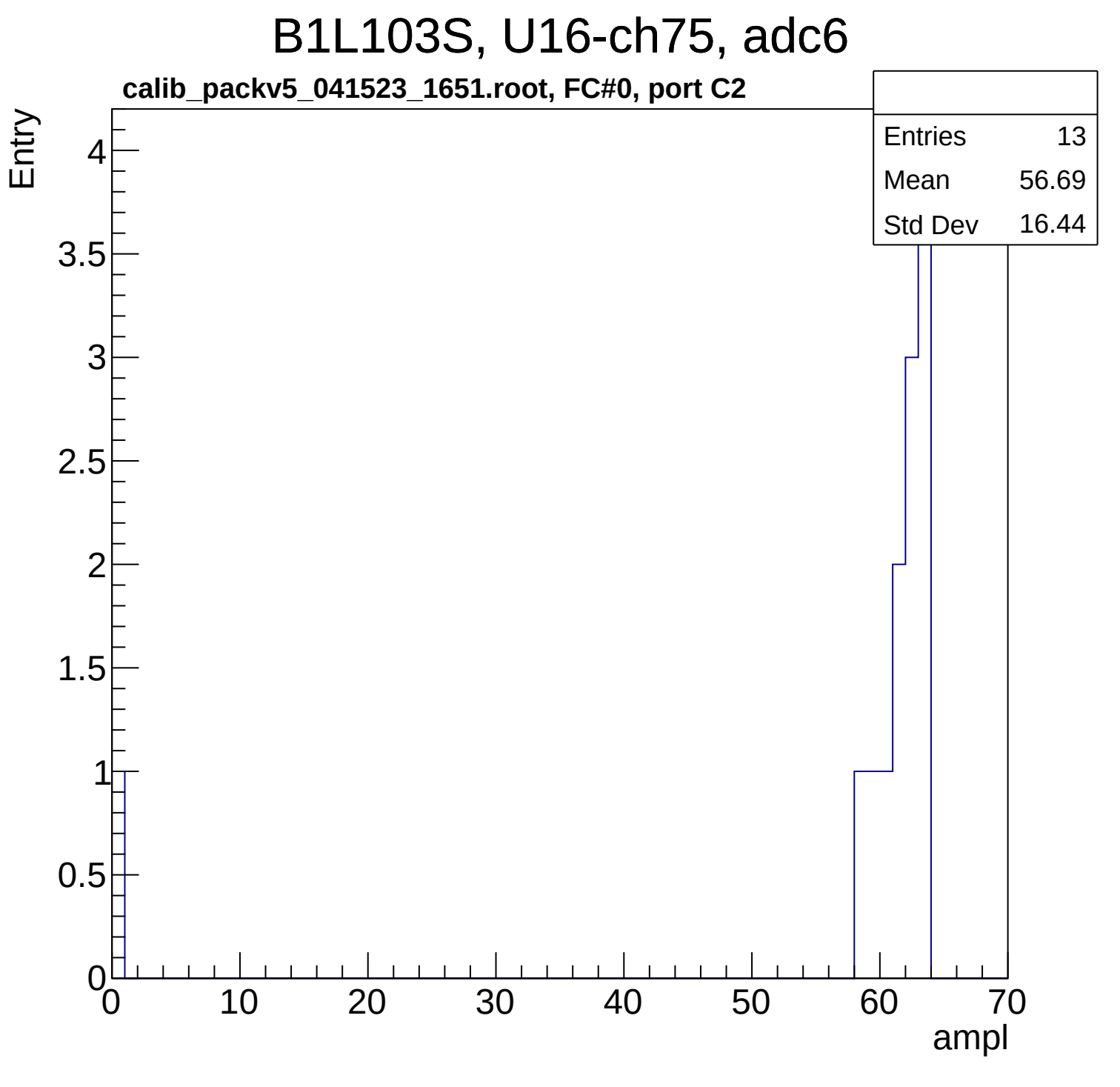
B1L103S, U16-ch75, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 56.69
Std Dev 16.44
Entry
ampl
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1.5
2
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0
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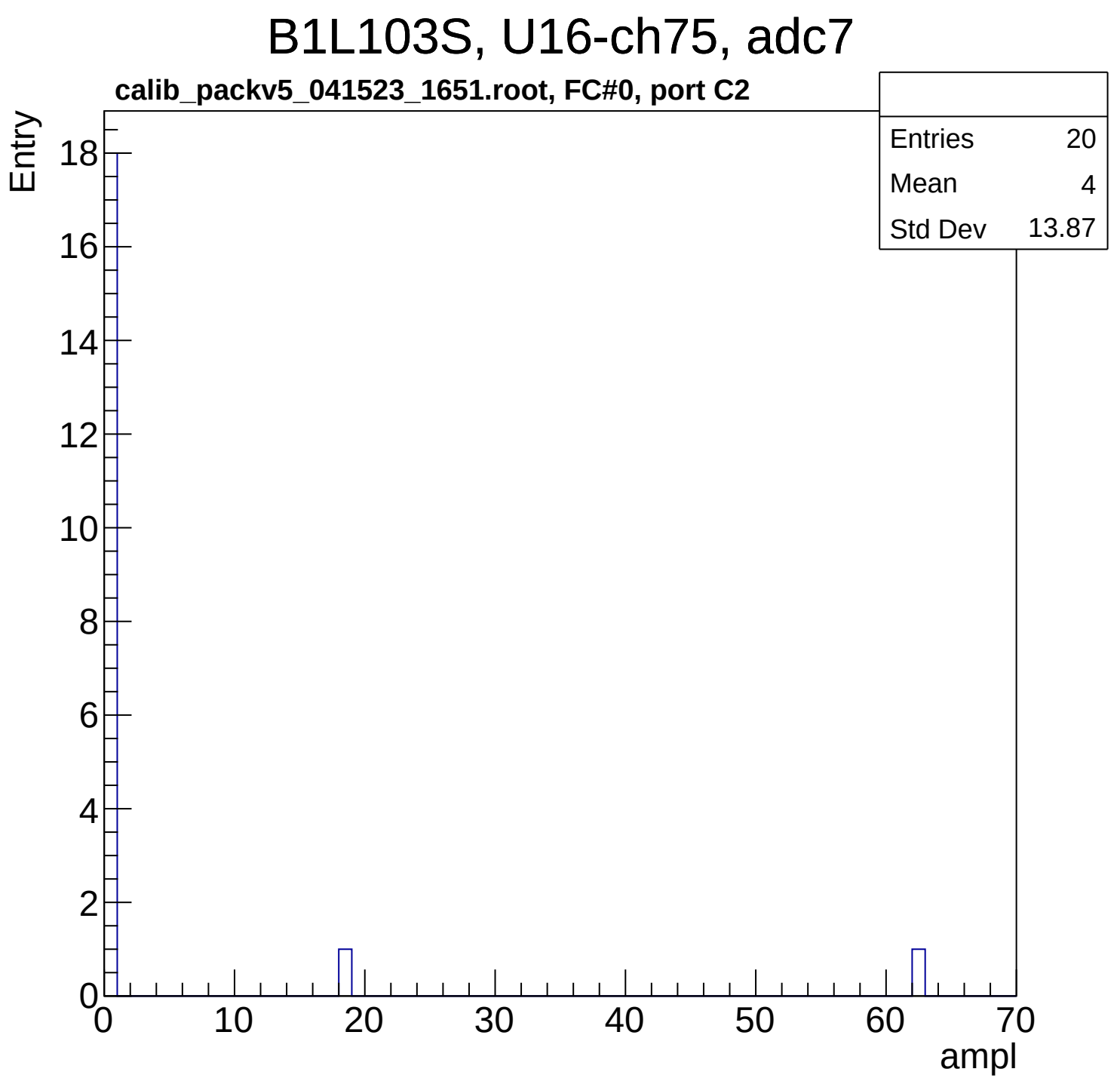
B1L103S, U16-ch75, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4
Std Dev 13.87
Entry
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6
8
10
12
14
16
18
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10
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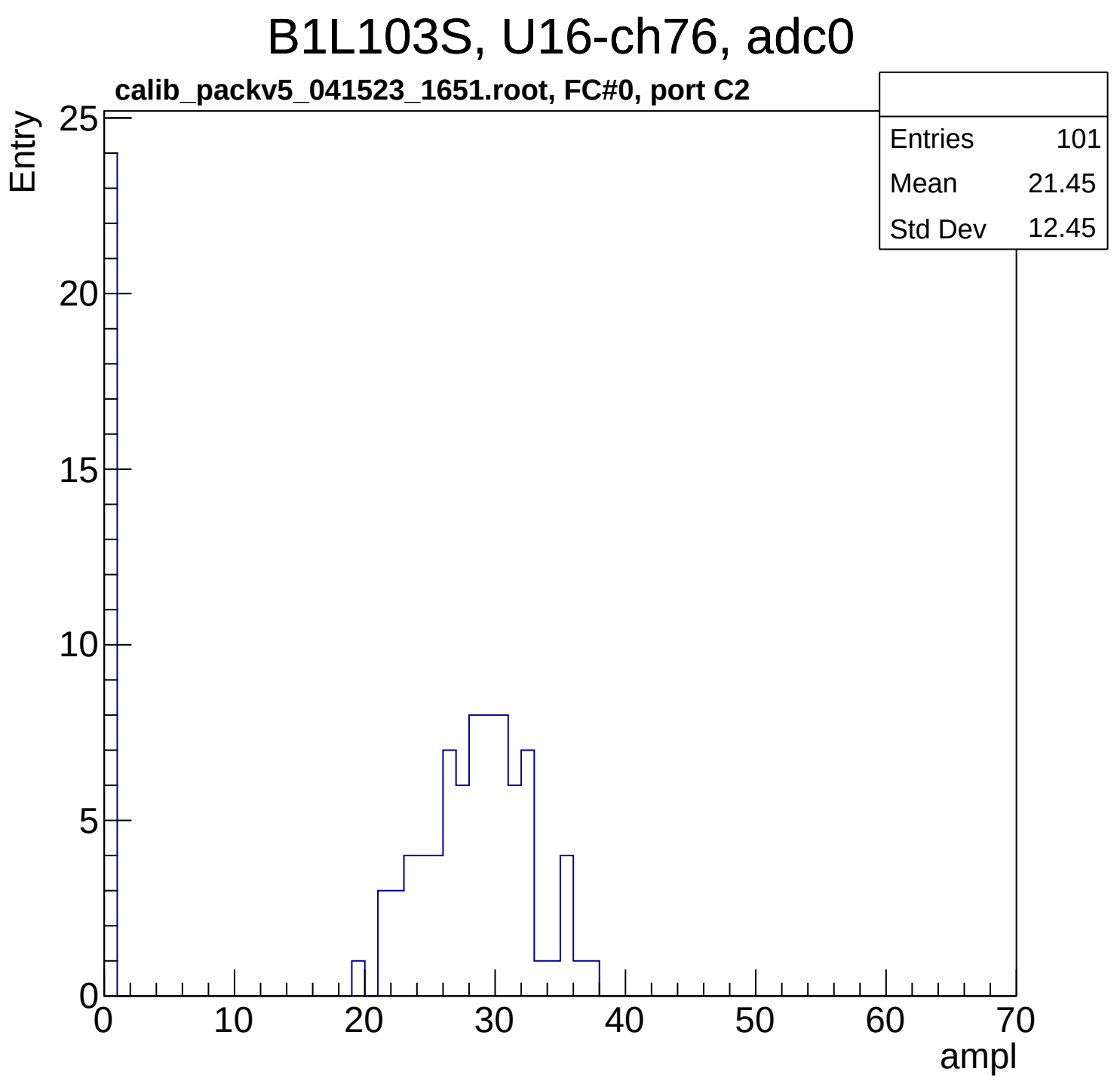
60
70
ampl


B1L103S, U16-ch76, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 21.45
Std Dev 12.45
Entry
ampl
0
5
10
15
20
25
0
10
20
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40
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60
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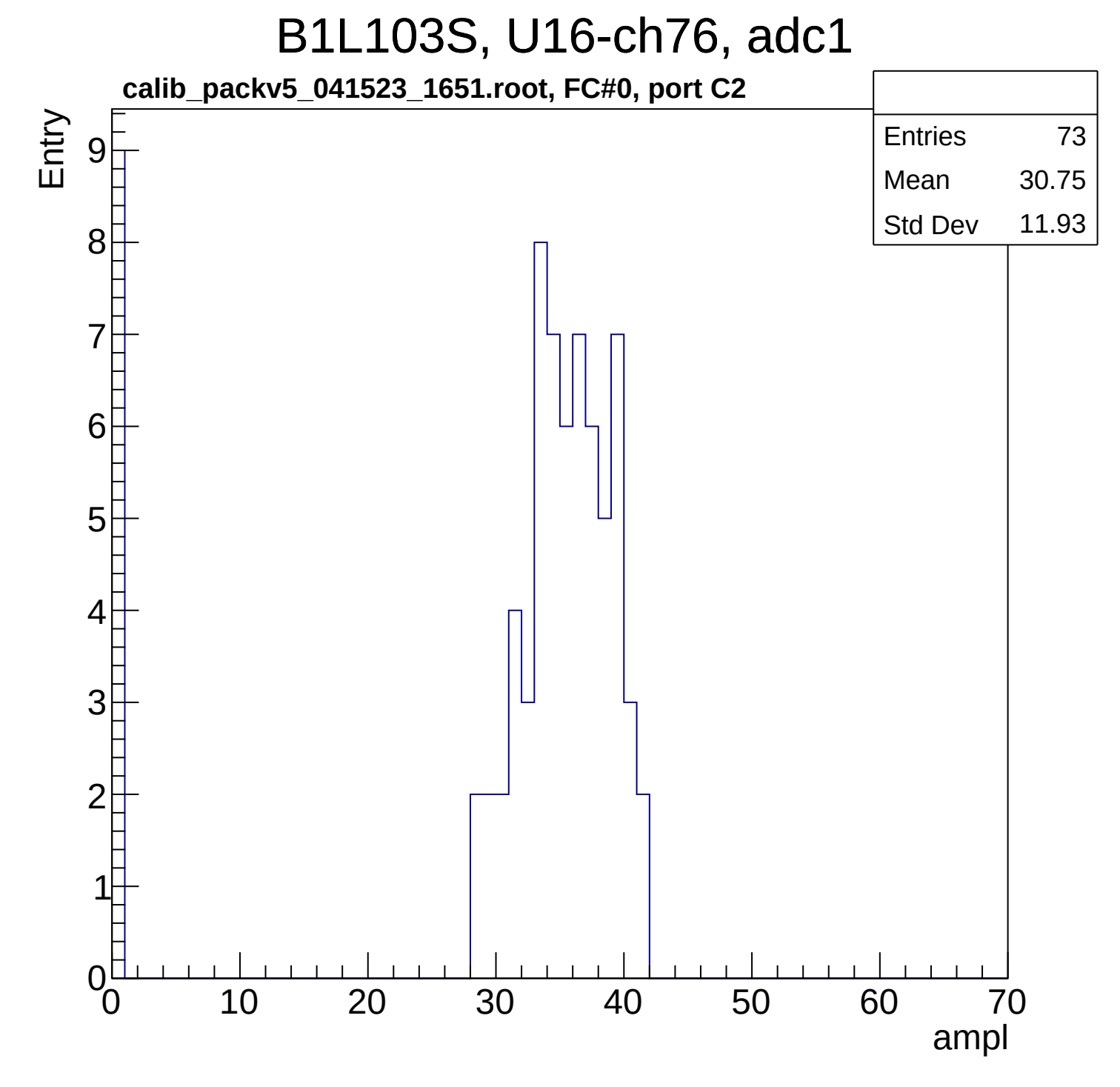
B1L103S, U16-ch76, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 30.75
Std Dev 11.93
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
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60
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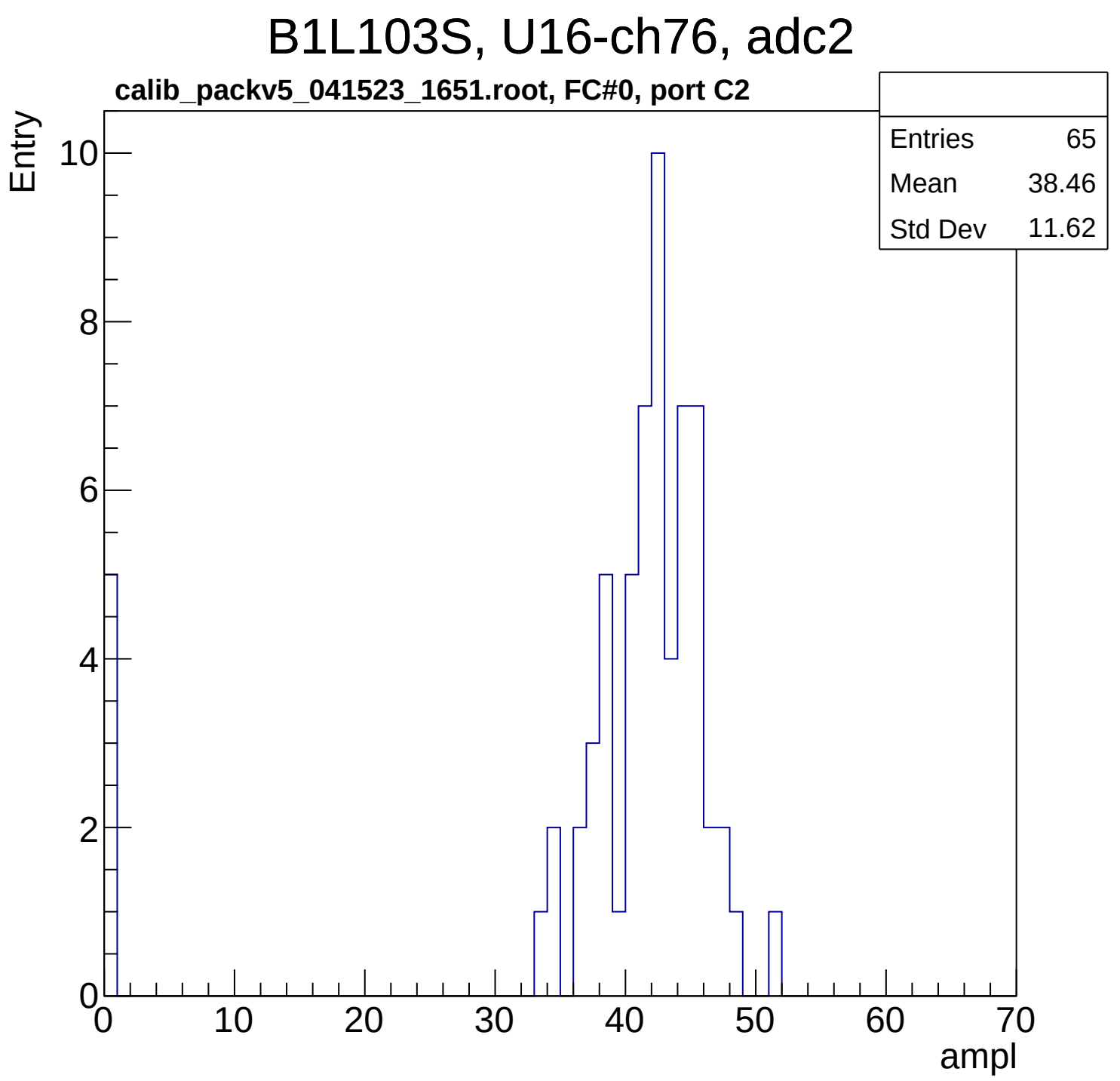
B1L103S, U16-ch76, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 38.46
Std Dev 11.62
Entry
ampl
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4
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0
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40
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60
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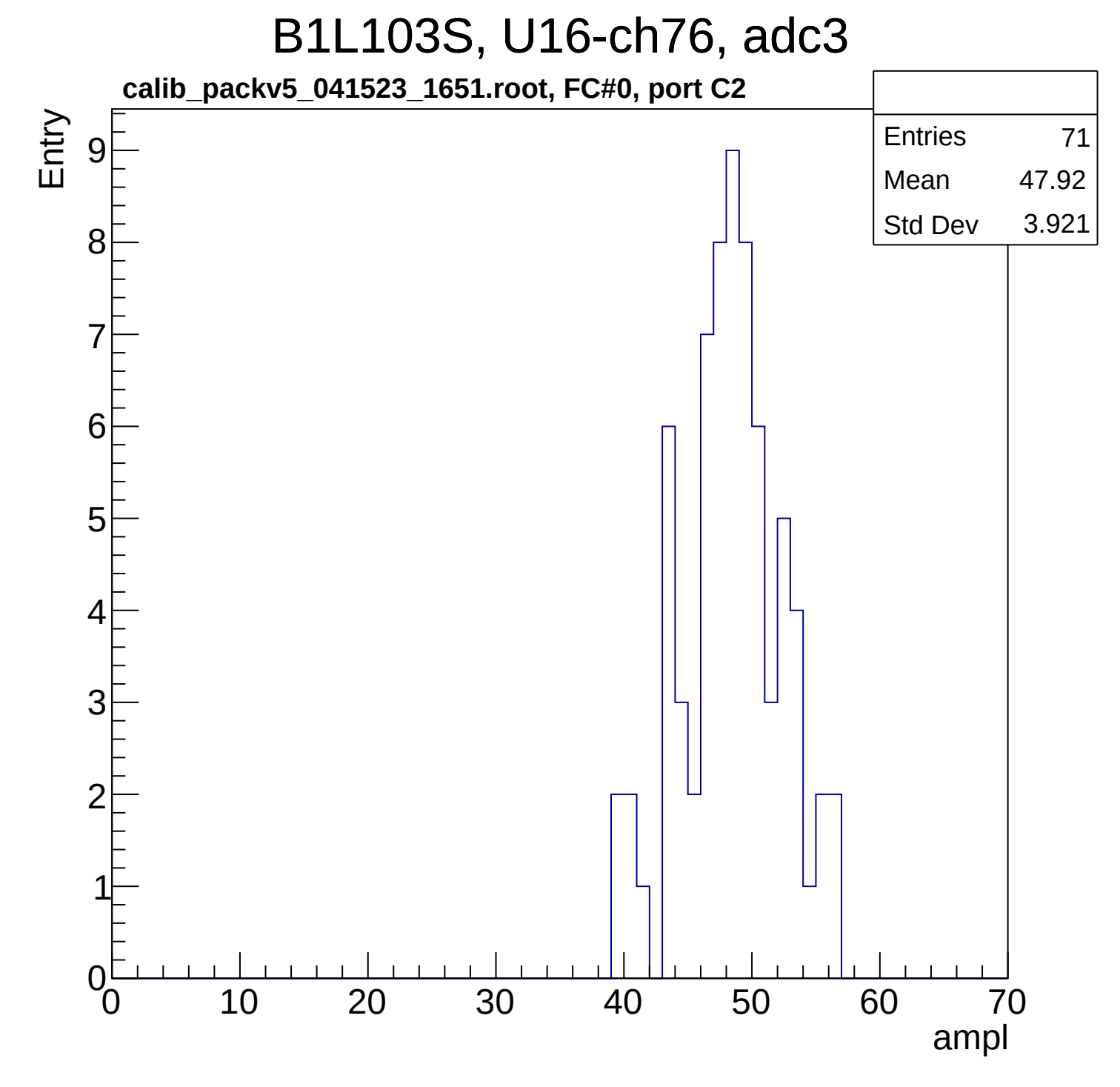
B1L103S, U16-ch76, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 47.92
Std Dev 3.921
Entry
ampl
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3
4
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6
7
8
9
0
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60
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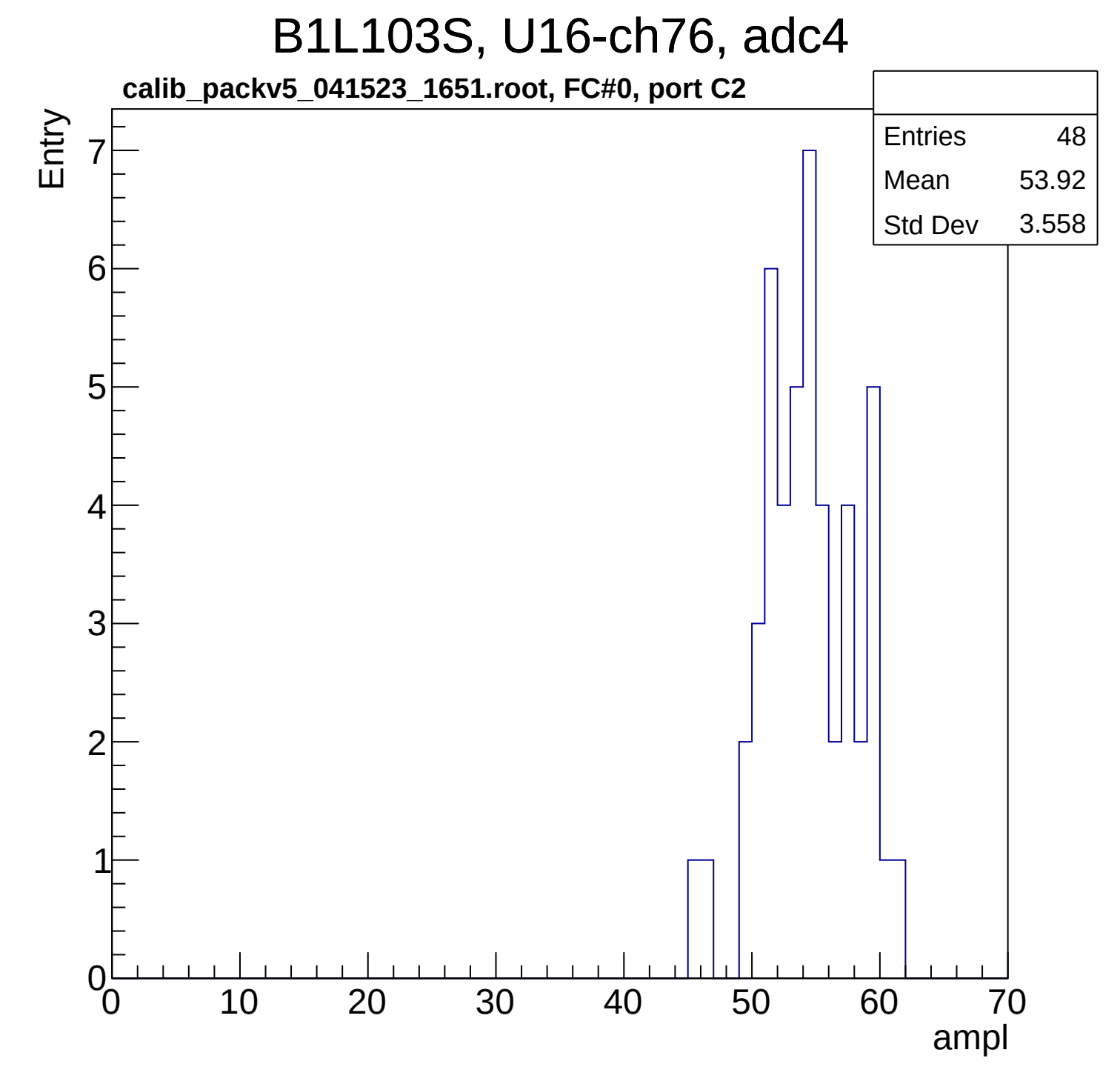
B1L103S, U16-ch76, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 53.92
Std Dev 3.558
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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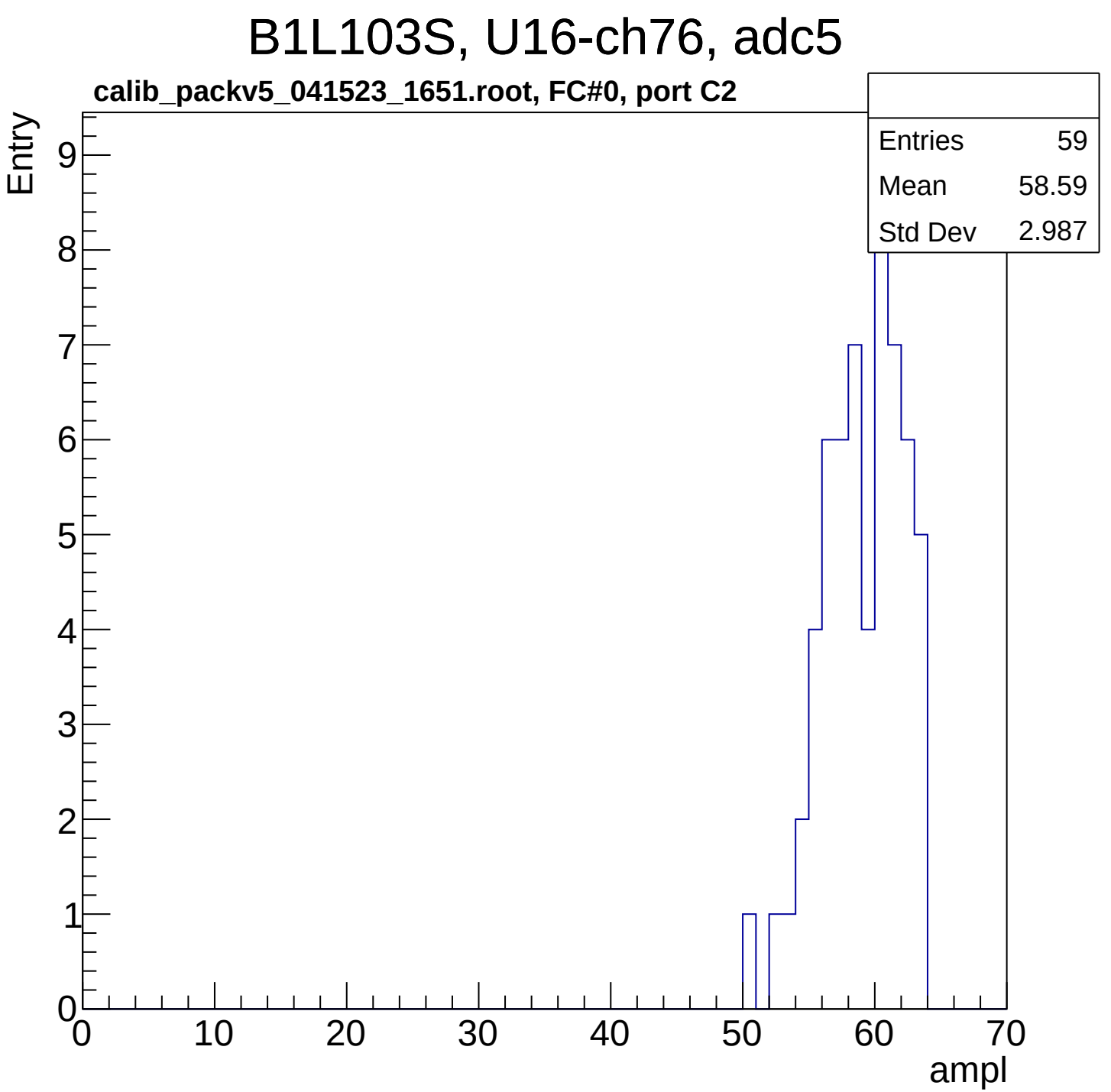
B1L103S, U16-ch76, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 58.59
Std Dev 2.987
Entry
ampl
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4
5
6
7
8
9
0
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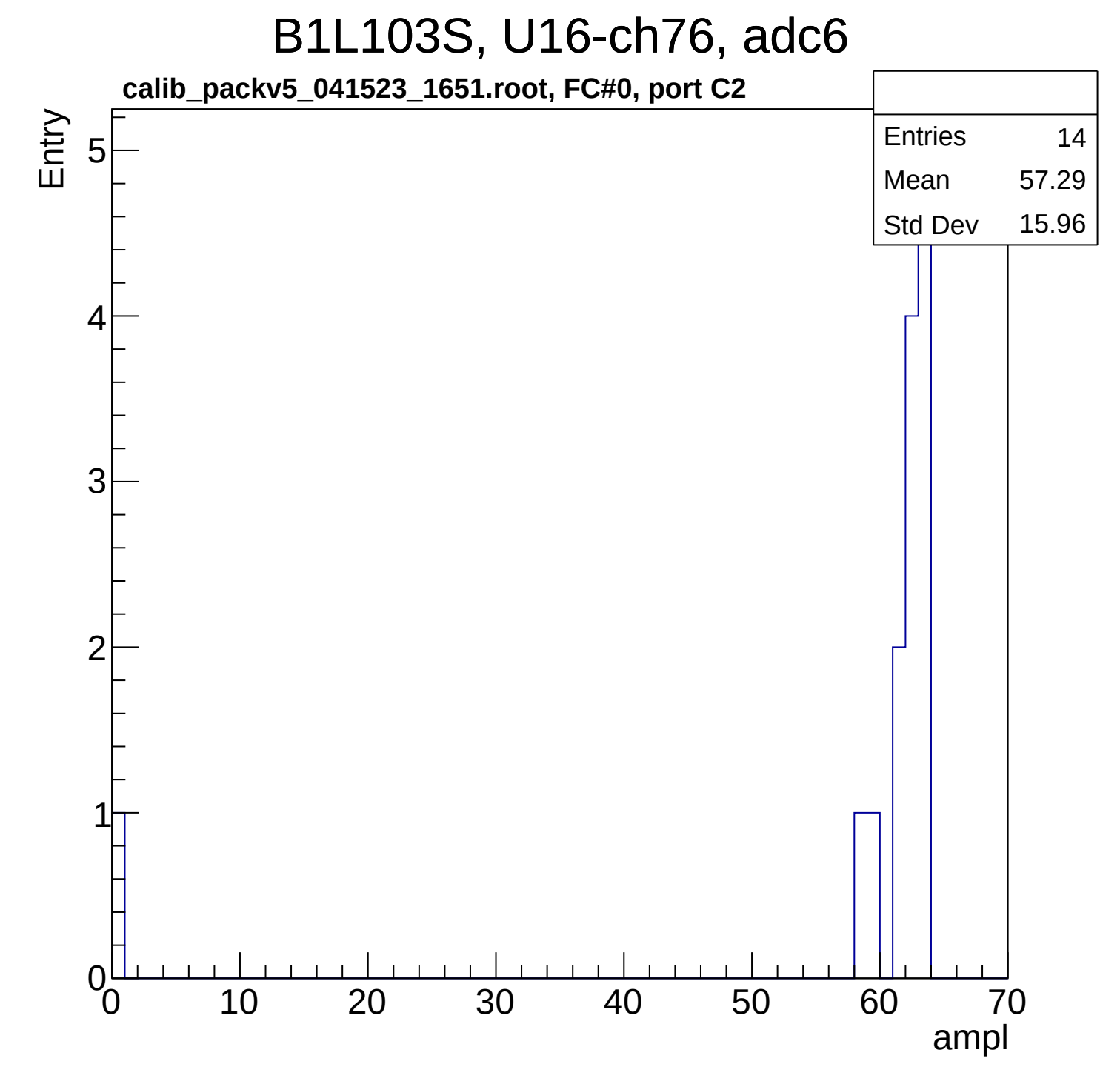
B1L103S, U16-ch76, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 57.29
Std Dev 15.96
Entry
ampl
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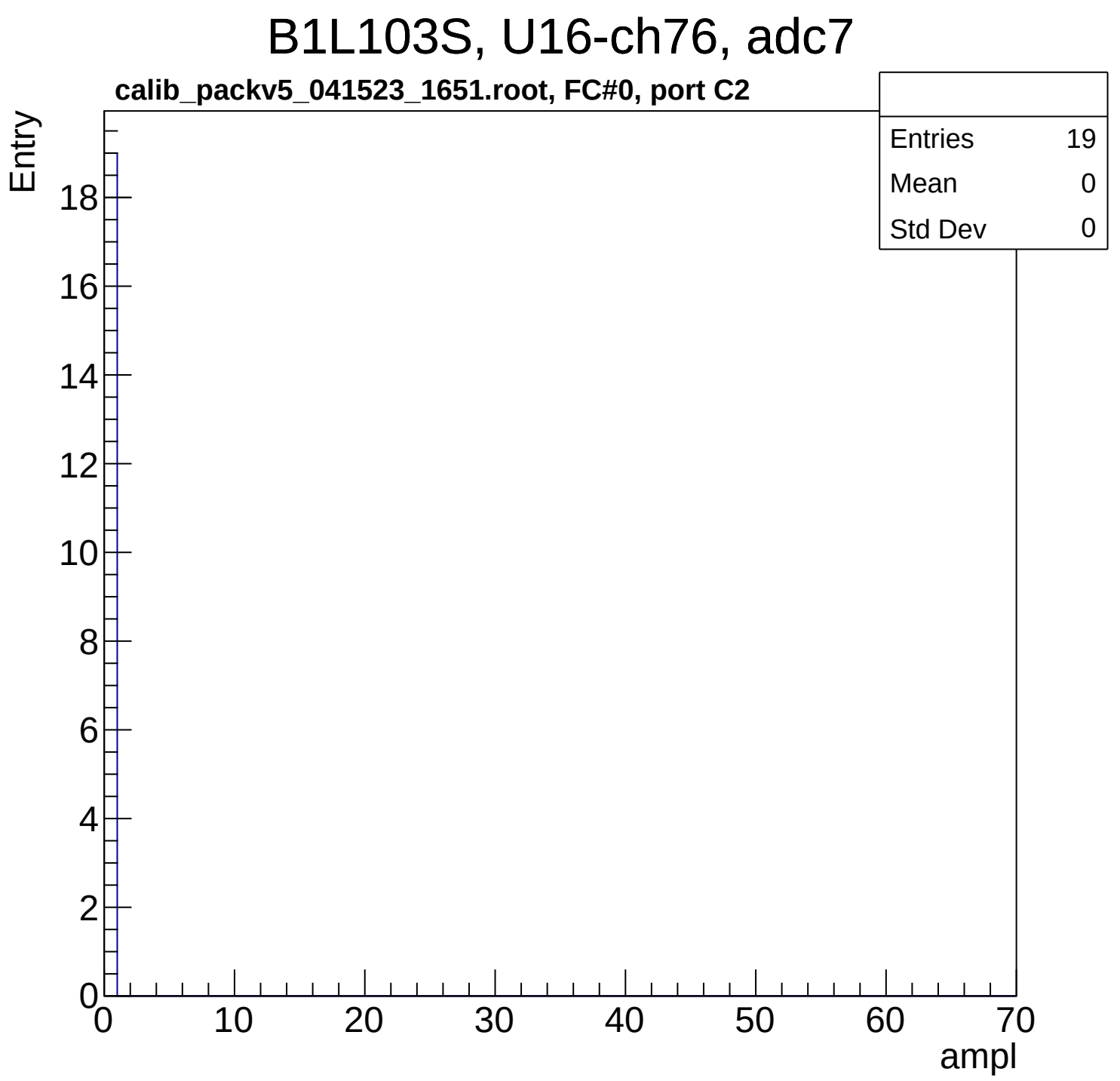
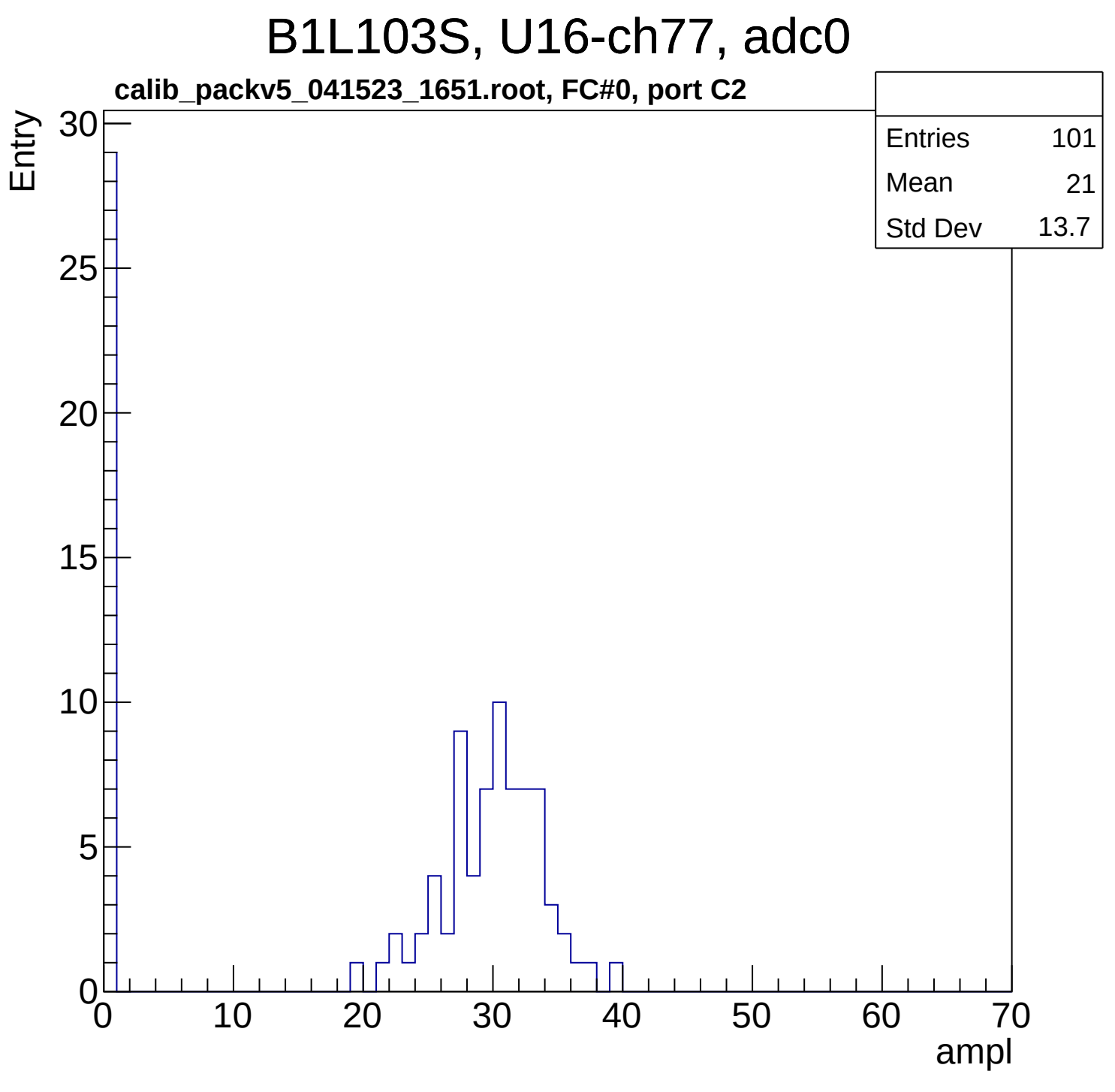
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U16-ch76, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch77, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 21
Std Dev 13.7
Entry
ampl
0
5
10
15
20
25
30
0
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20
30
40
50
60
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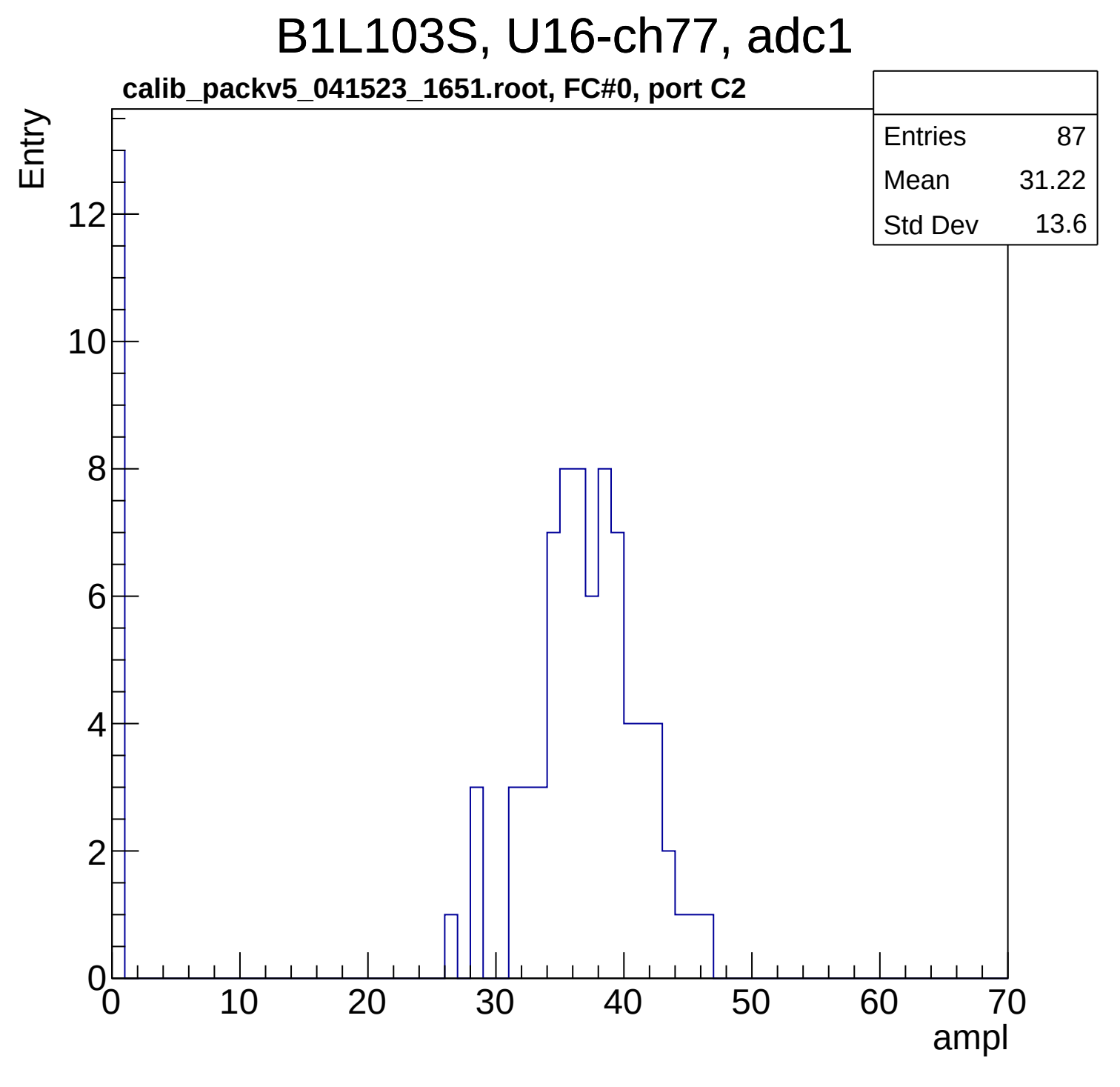
B1L103S, U16-ch77, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 31.22
Std Dev 13.6
Entry
0
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4
6
8
10
12
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10
20
30
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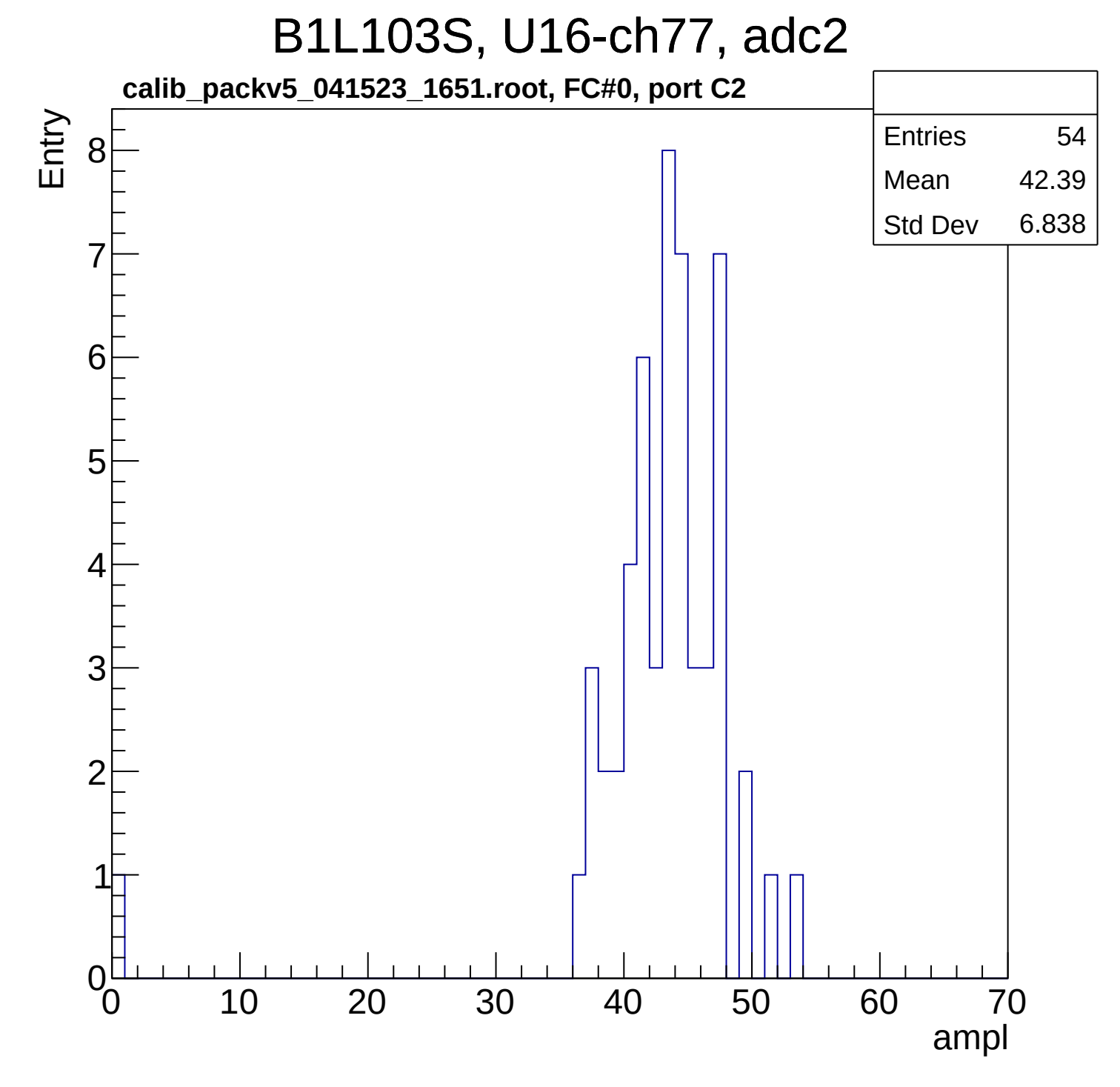
50
60
70
ampl


B1L103S, U16-ch77, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 42.39
Std Dev 6.838
Entry
ampl
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2
3
4
5
6
7
8
0
10
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40
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60
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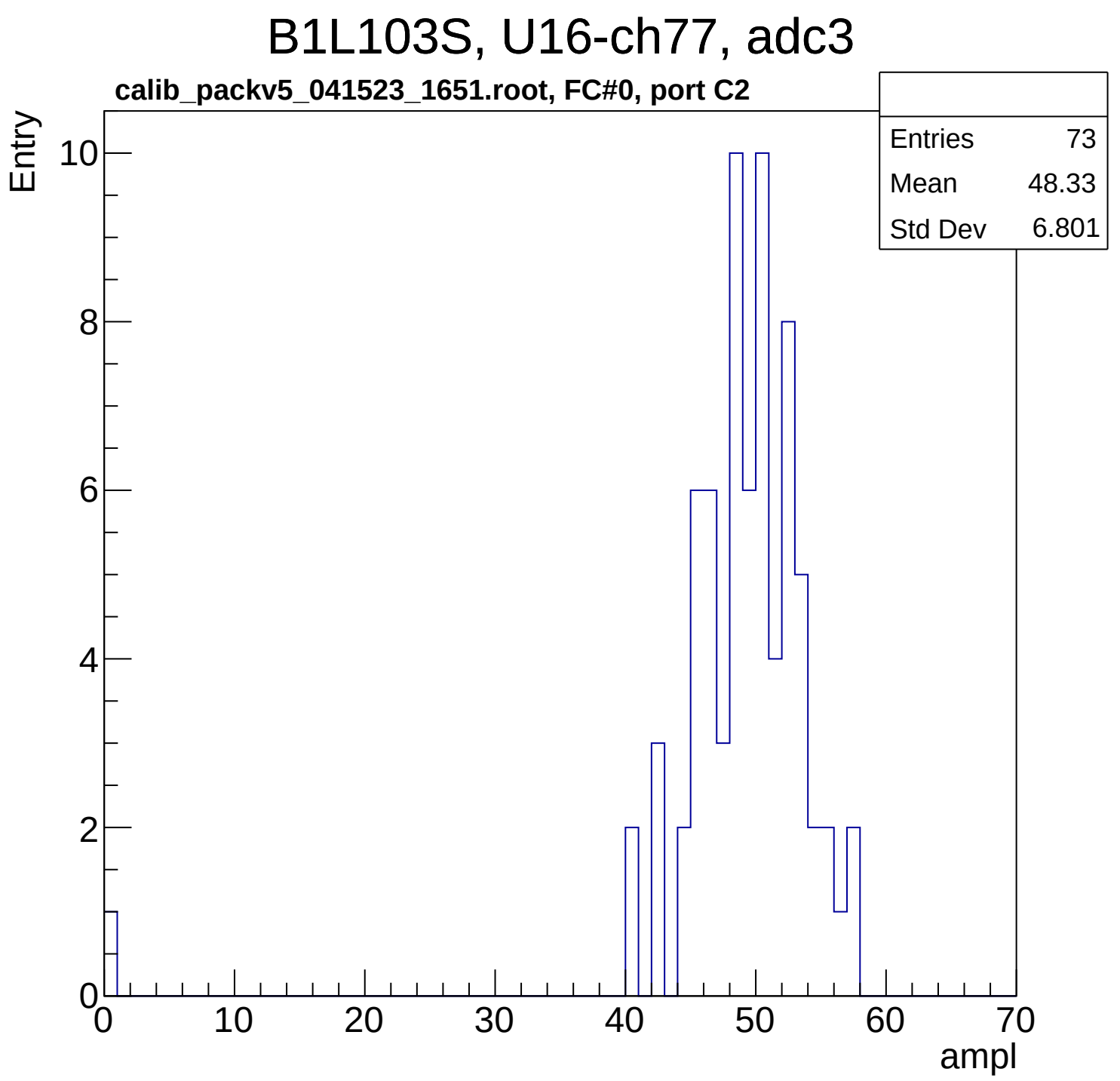
B1L103S, U16-ch77, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 48.33
Std Dev 6.801
Entry
ampl
0
2
4
6
8
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0
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50
60
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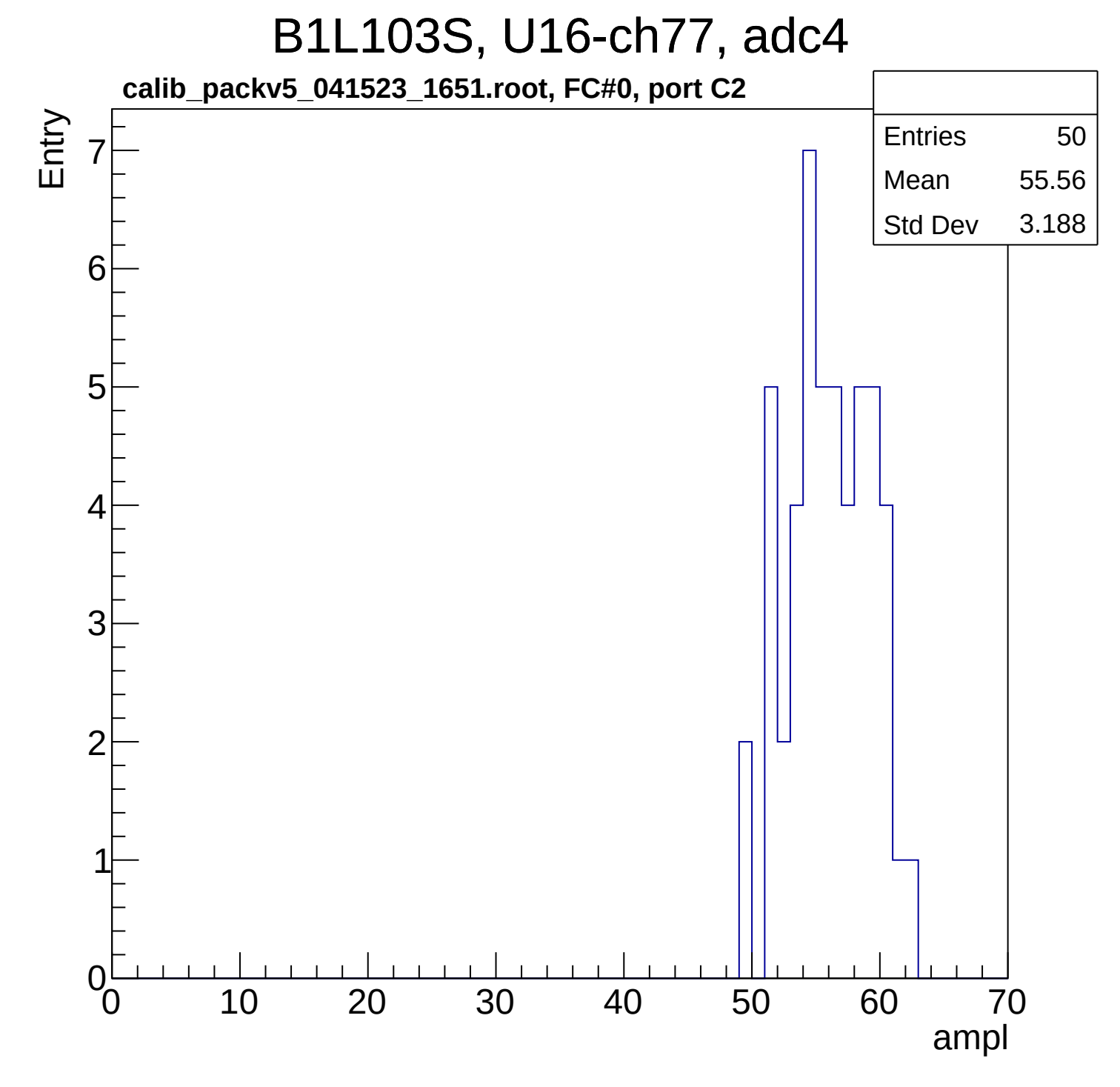
B1L103S, U16-ch77, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 55.56
Std Dev 3.188
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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40
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60
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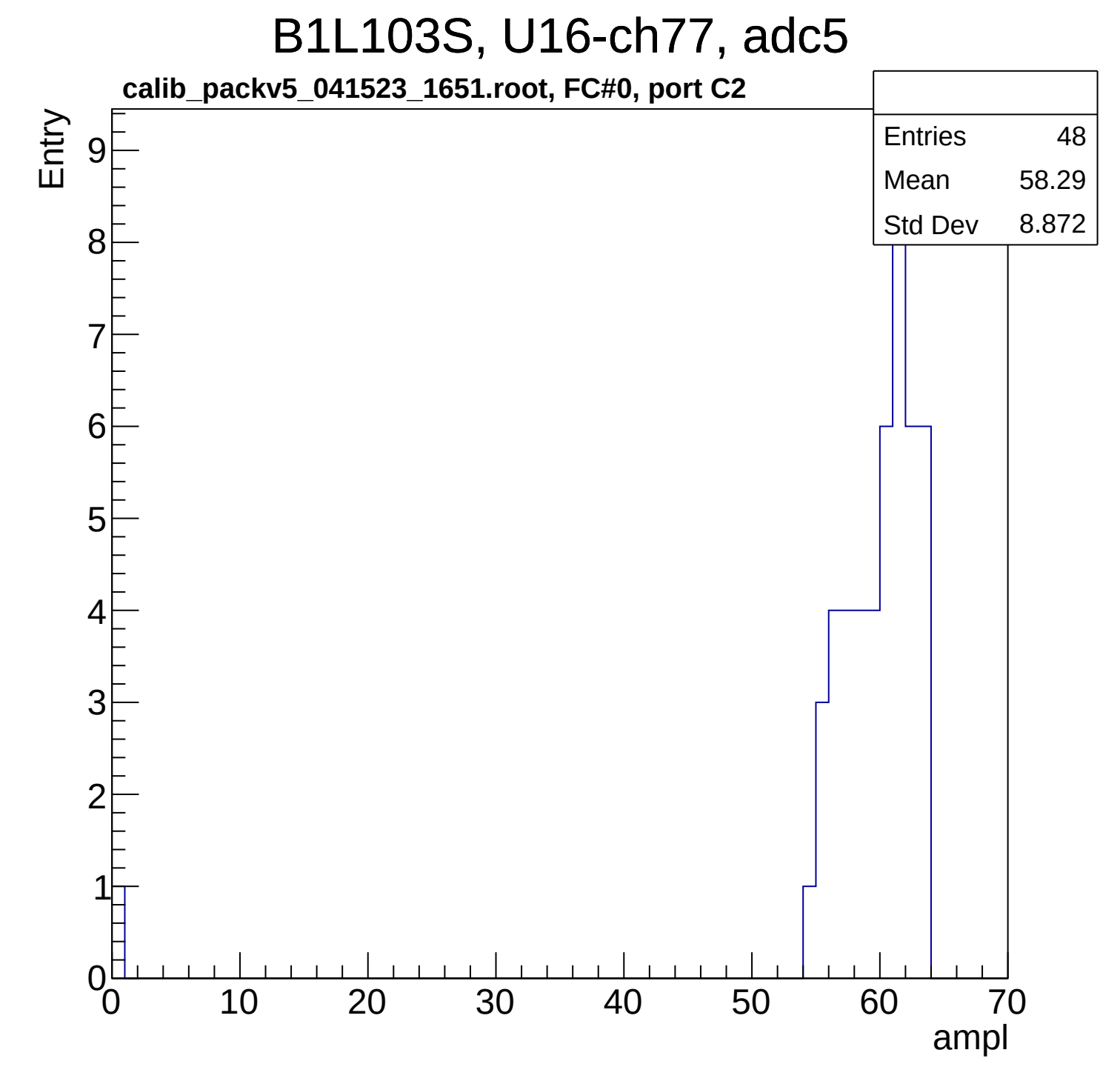
B1L103S, U16-ch77, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.29
Std Dev 8.872
Entry
ampl
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2
3
4
5
6
7
8
9
0
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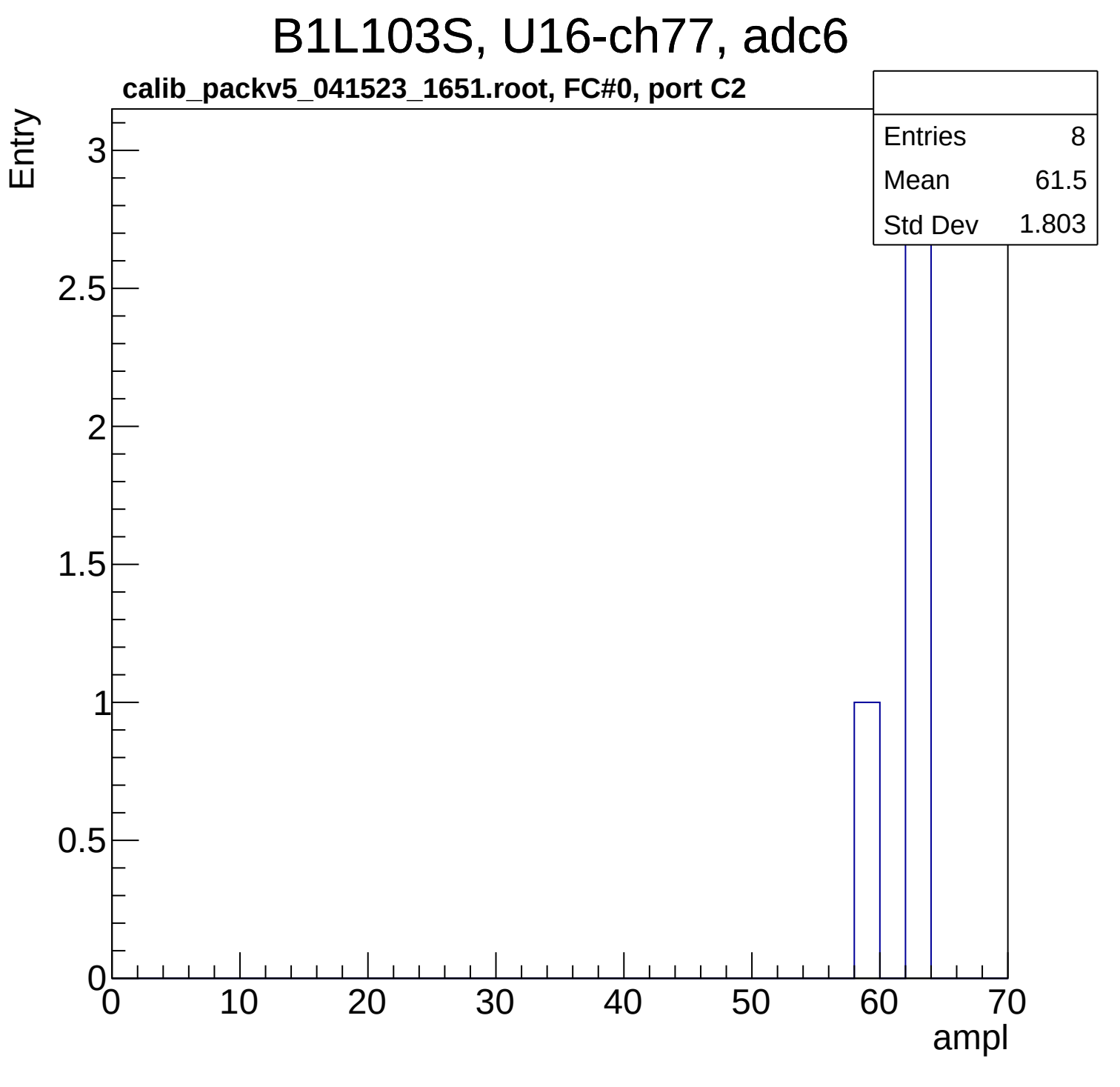
B1L103S, U16-ch77, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.5
Std Dev 1.803
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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40
50
60
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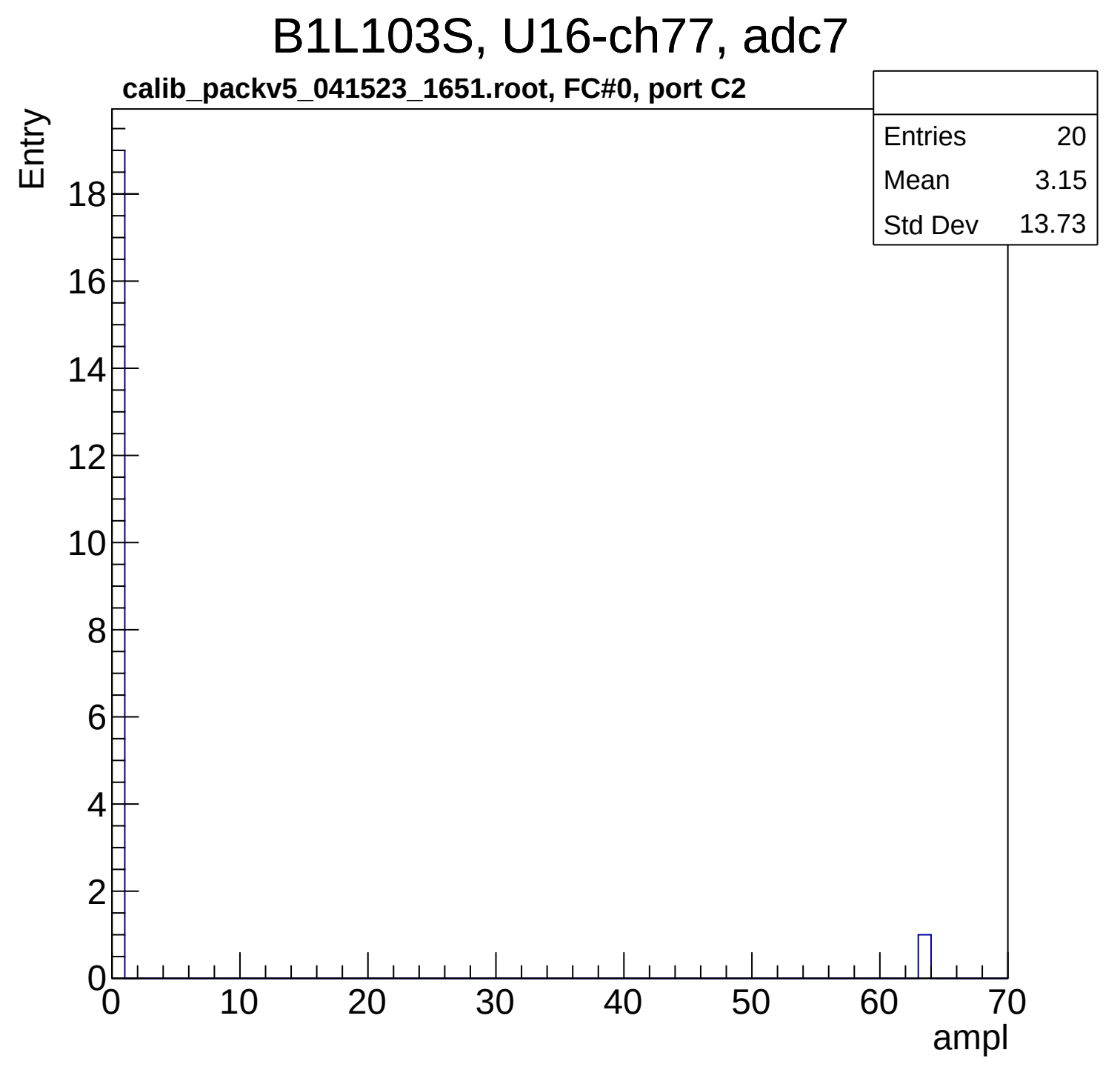
B1L103S, U16-ch77, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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6
8
10
12
14
16
18
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10
20
30
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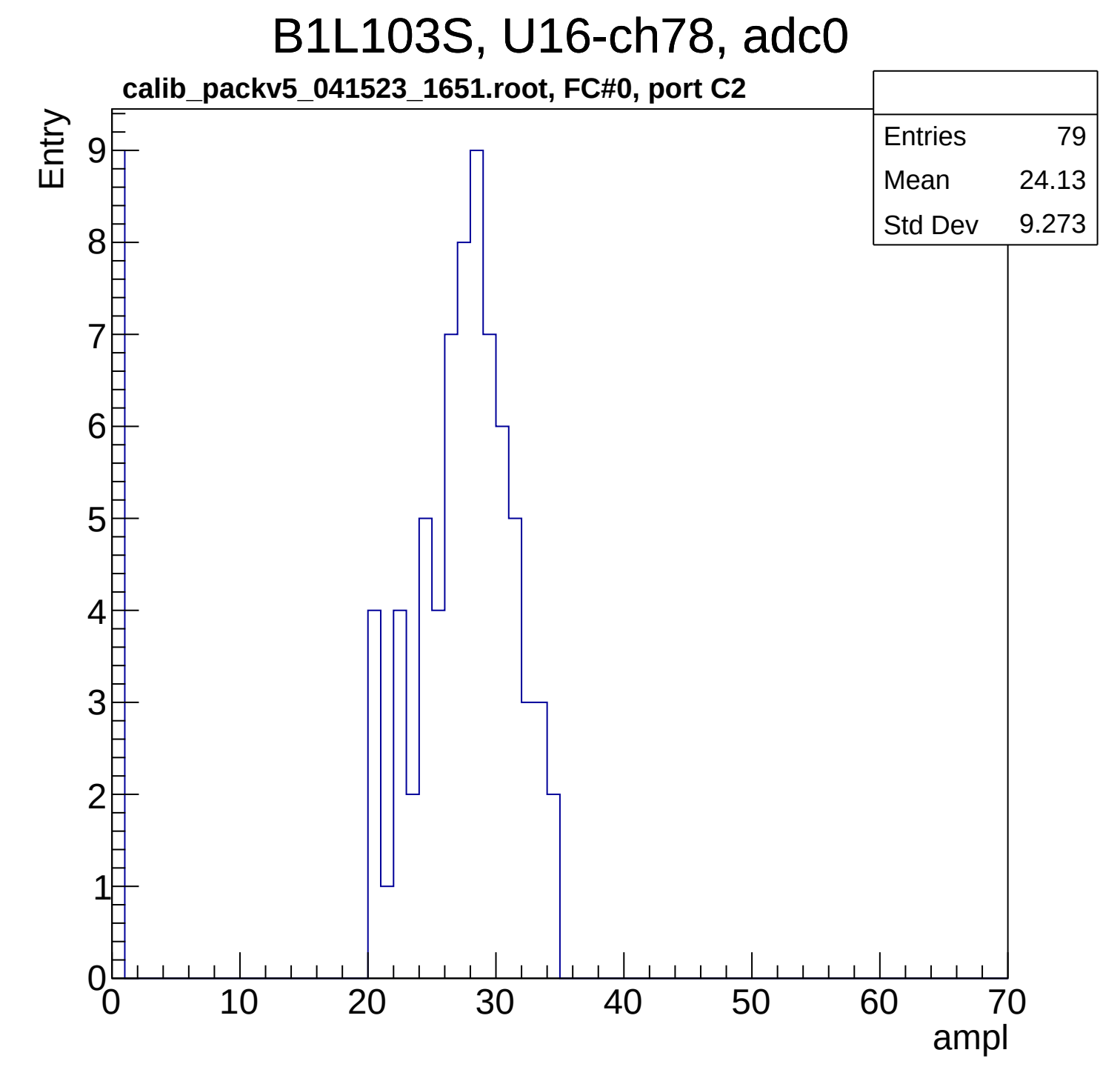
50
60
70
ampl


B1L103S, U16-ch78, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 24.13
Std Dev 9.273
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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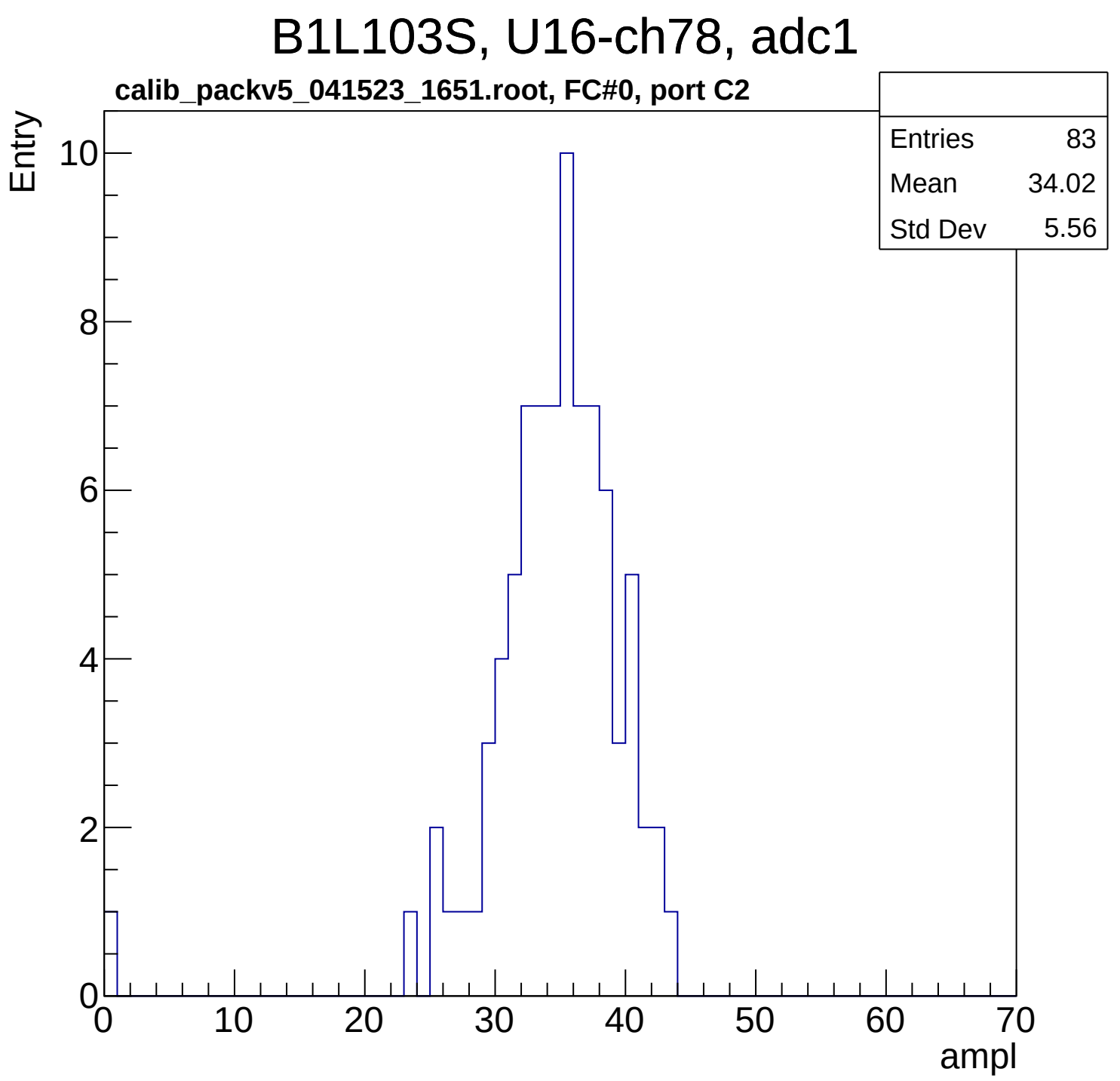
B1L103S, U16-ch78, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 34.02
Std Dev 5.56
Entry
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4
6
8
10
0
10
20
30
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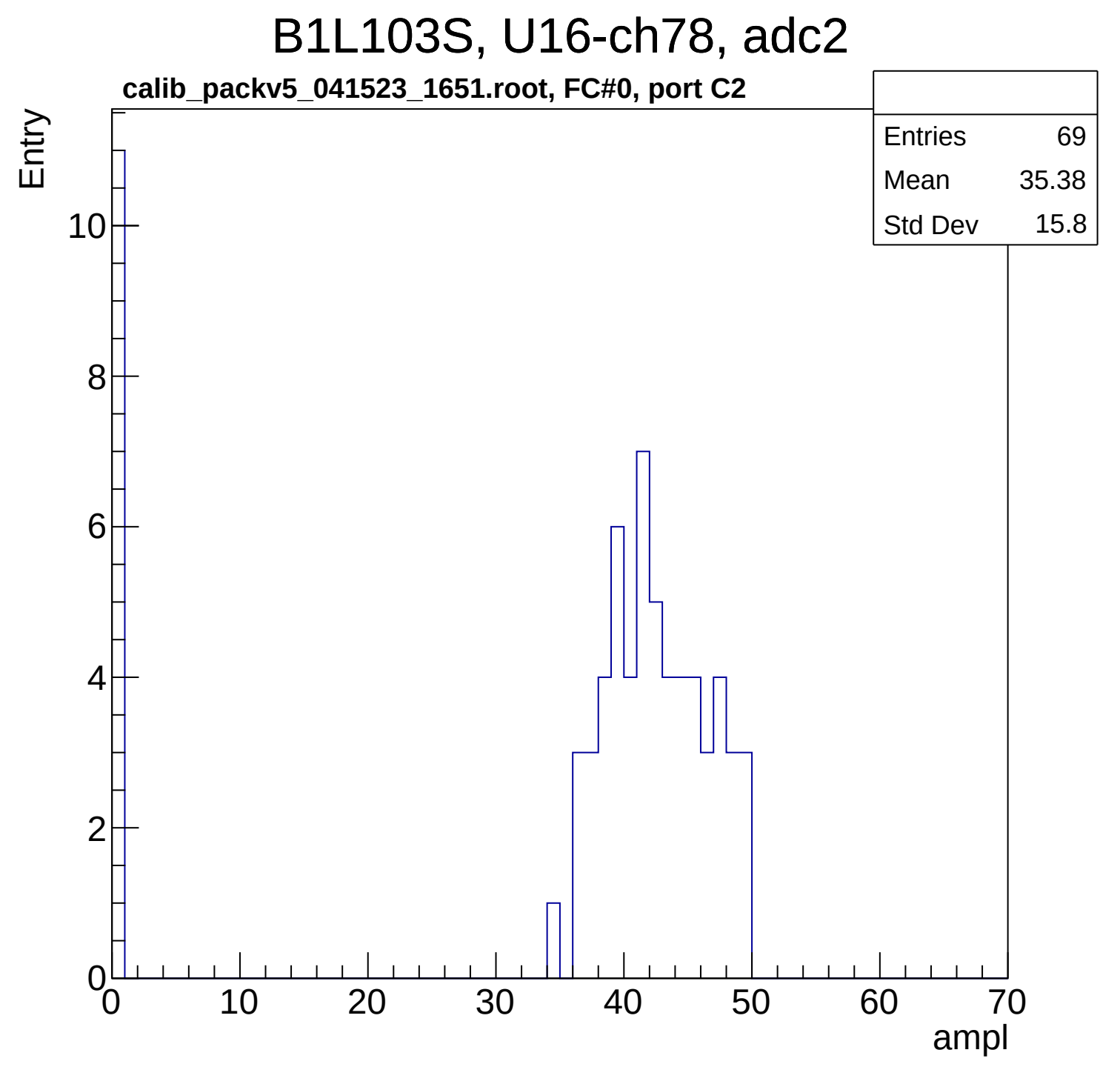
50
60
70
ampl


B1L103S, U16-ch78, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 35.38
Std Dev 15.8
Entry
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6
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10
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30
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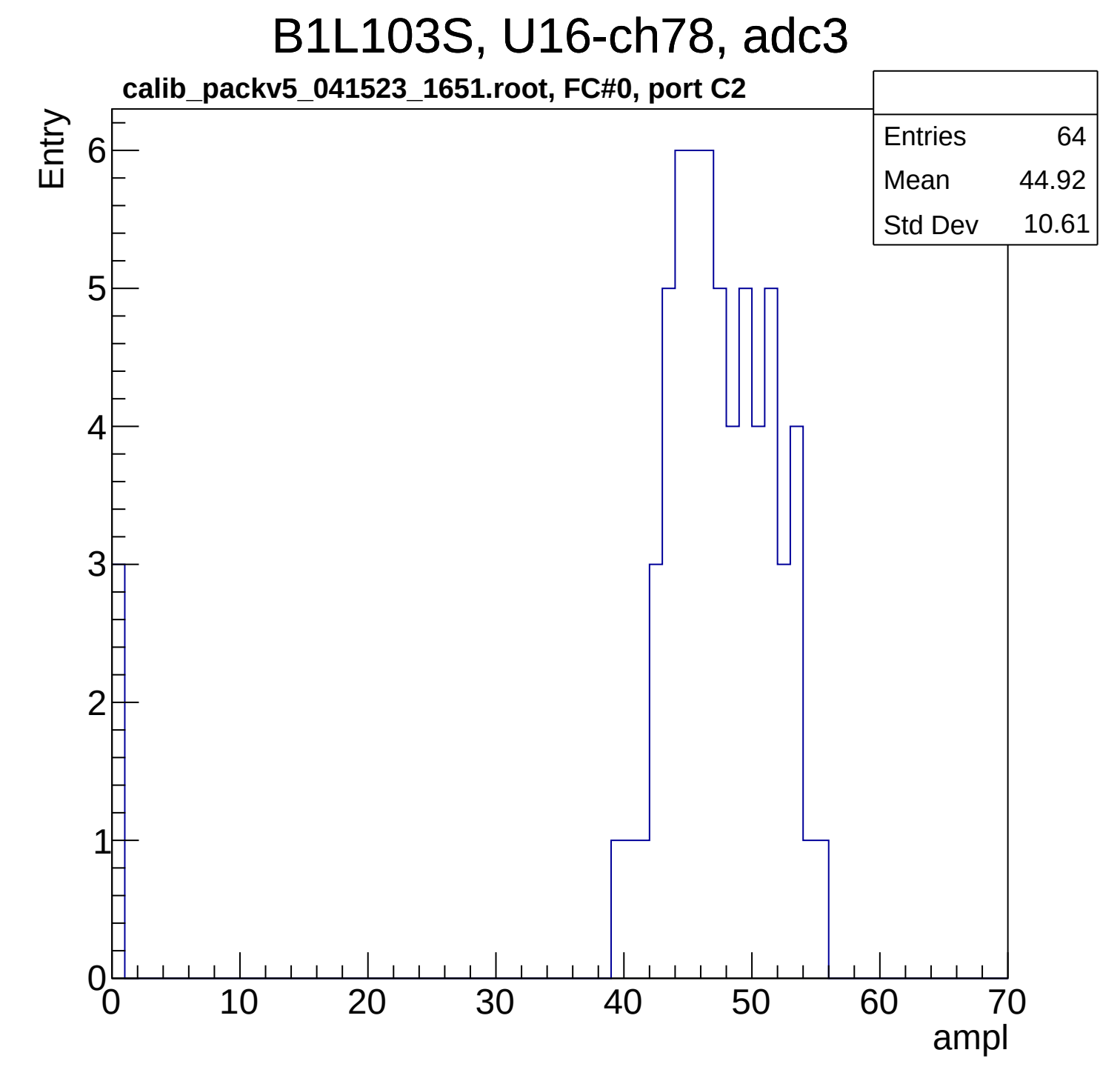
60
70
ampl


B1L103S, U16-ch78, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 44.92
Std Dev 10.61
Entry
ampl
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1
2
3
4
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0
10
20
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40
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60
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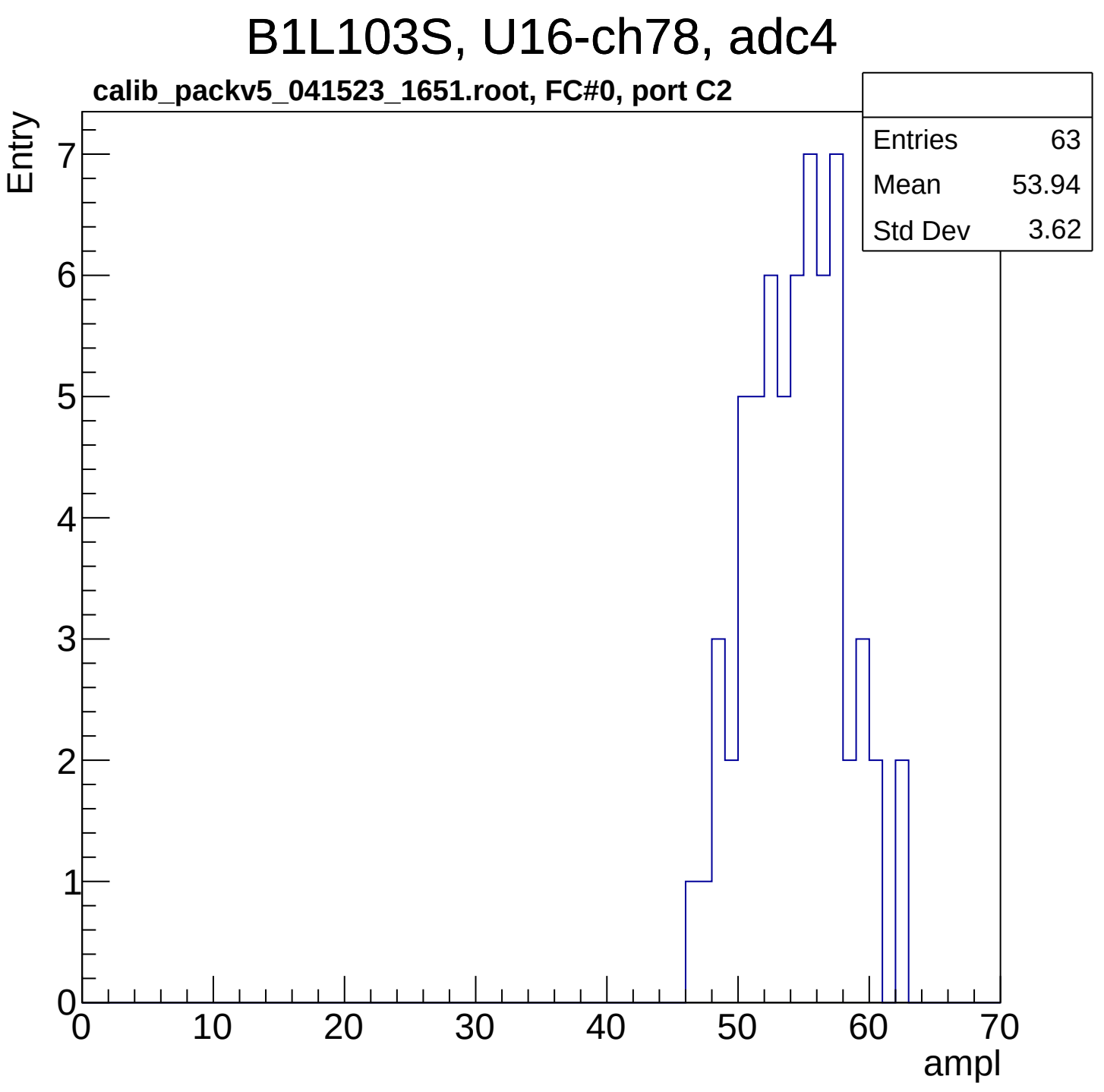
B1L103S, U16-ch78, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 53.94
Std Dev 3.62
Entry
ampl
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1
2
3
4
5
6
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0
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40
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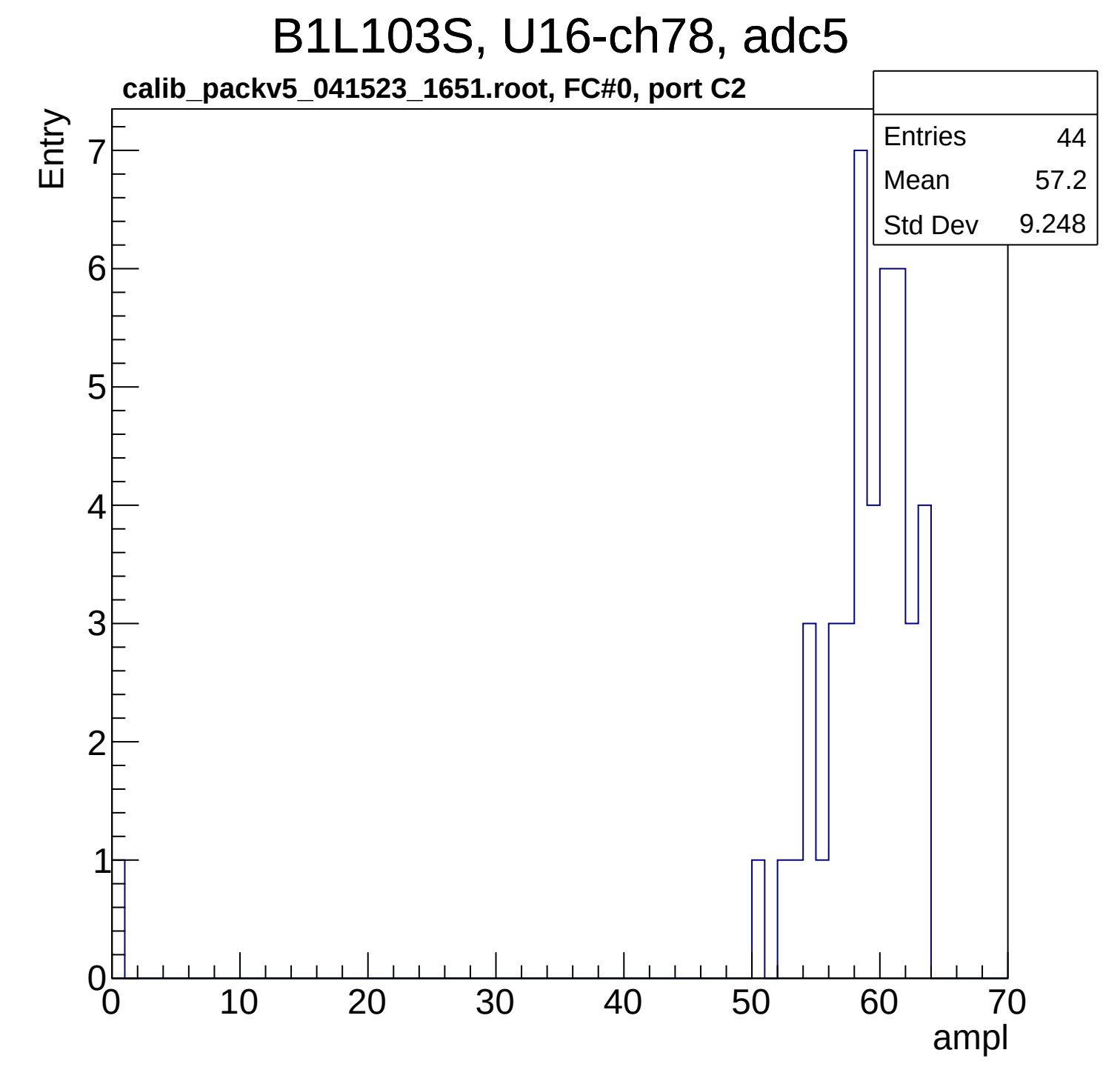
B1L103S, U16-ch78, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 57.2
Std Dev 9.248
Entry
ampl
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2
3
4
5
6
7
0
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20
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40
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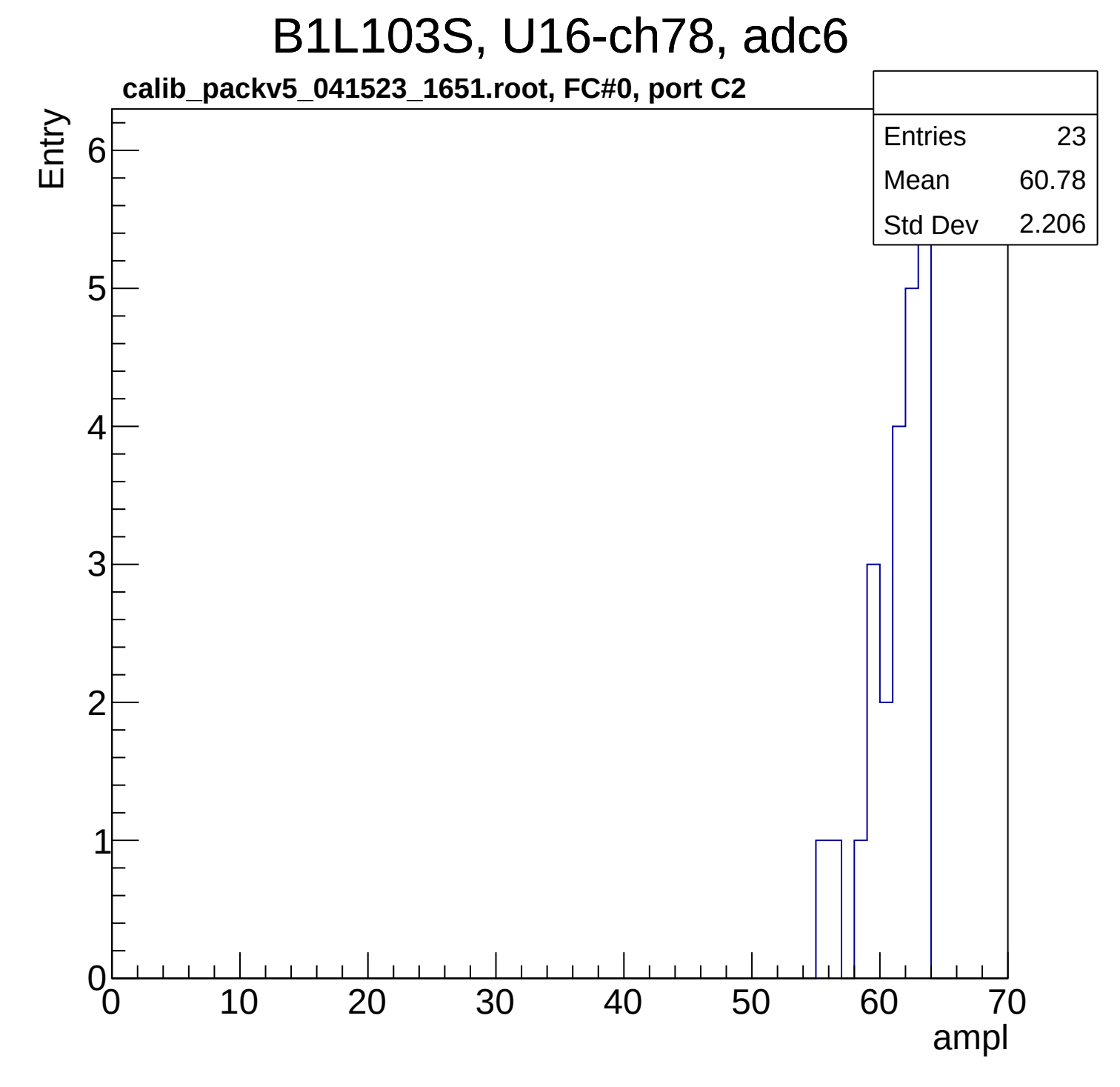
60
70


B1L103S, U16-ch78, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 60.78
Std Dev 2.206
Entry
ampl
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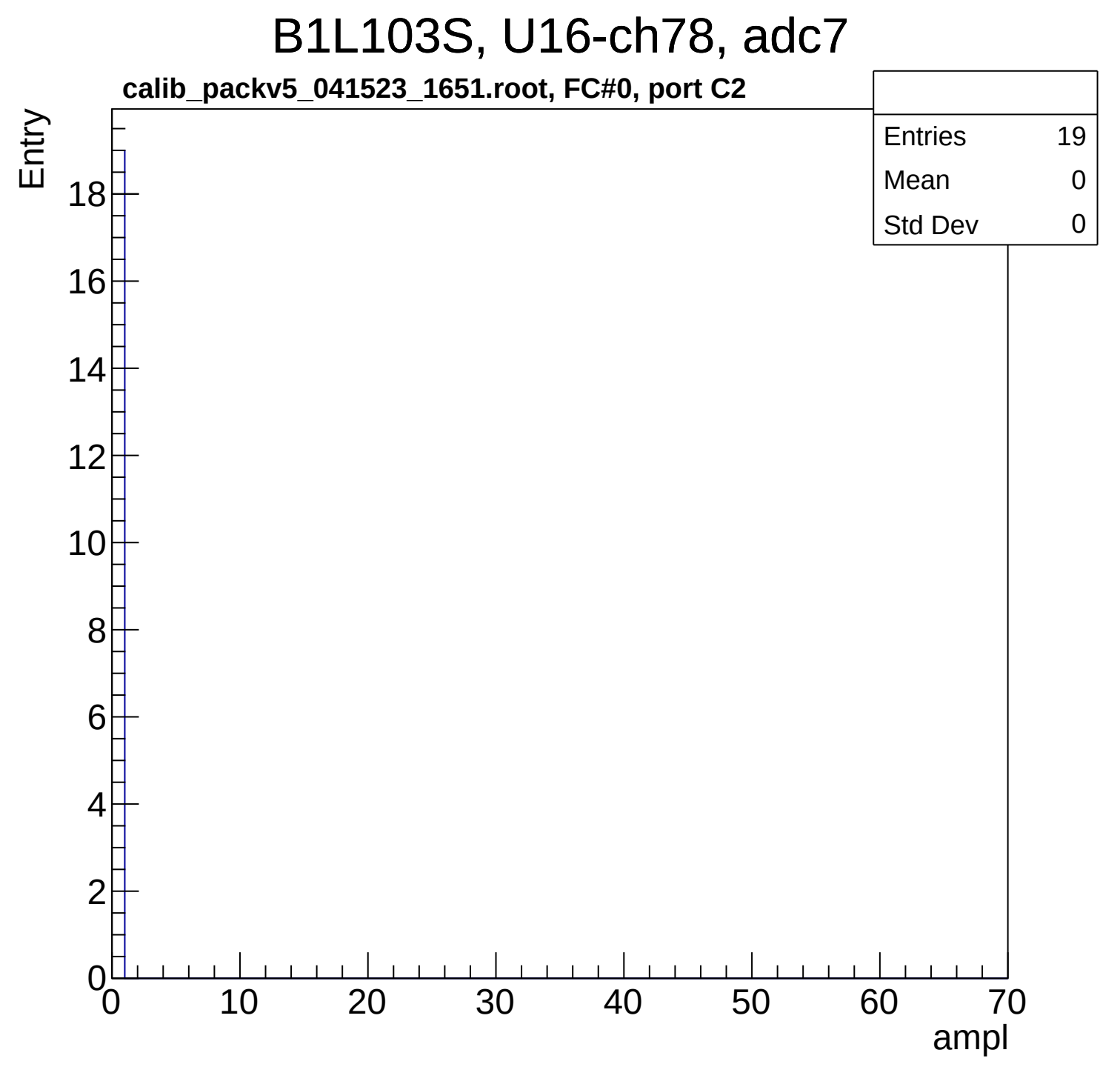
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U16-ch78, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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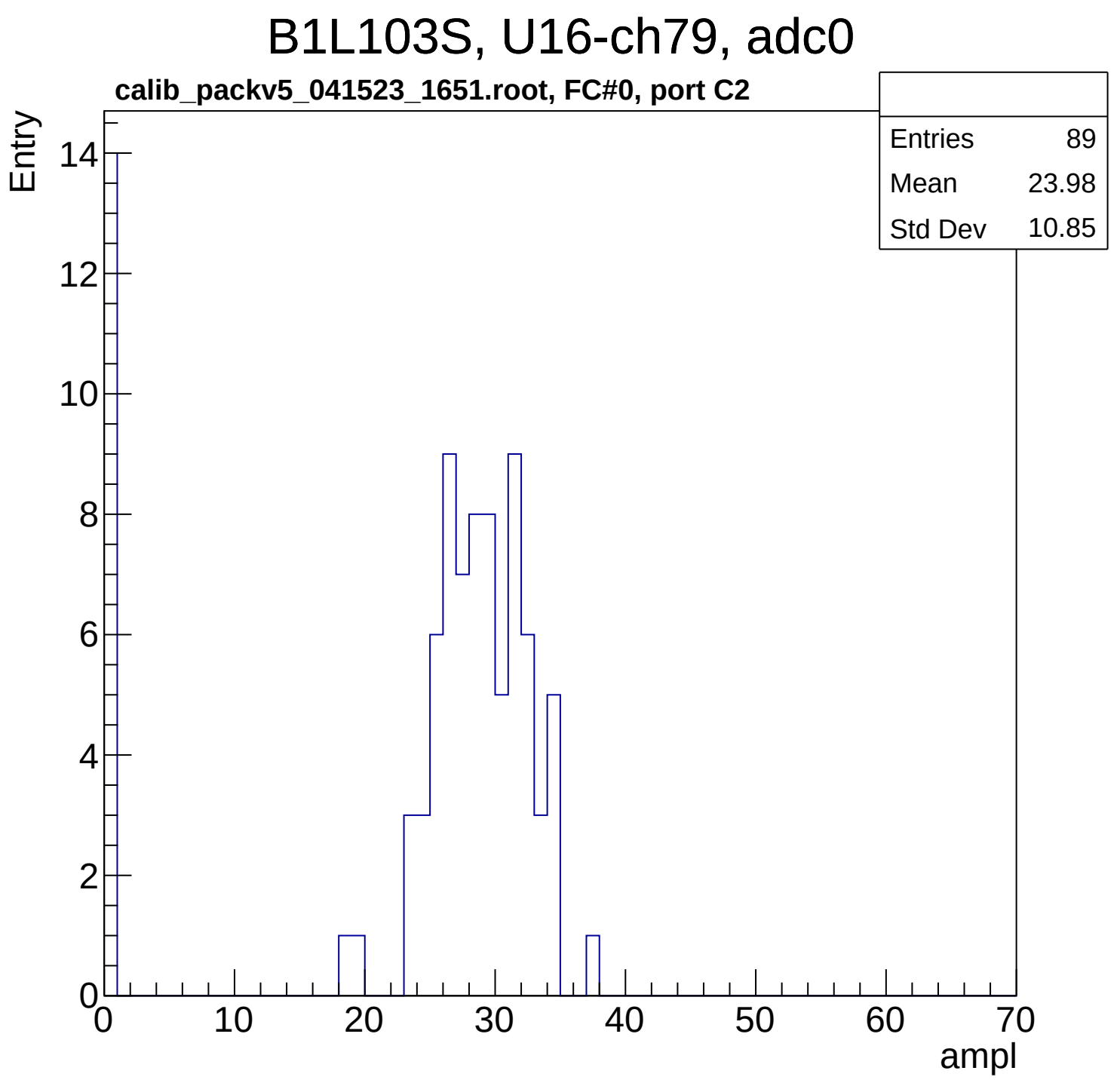
50
60
70
ampl


B1L103S, U16-ch79, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 23.98
Std Dev 10.85
Entry
ampl
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4
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8
10
12
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0
10
20
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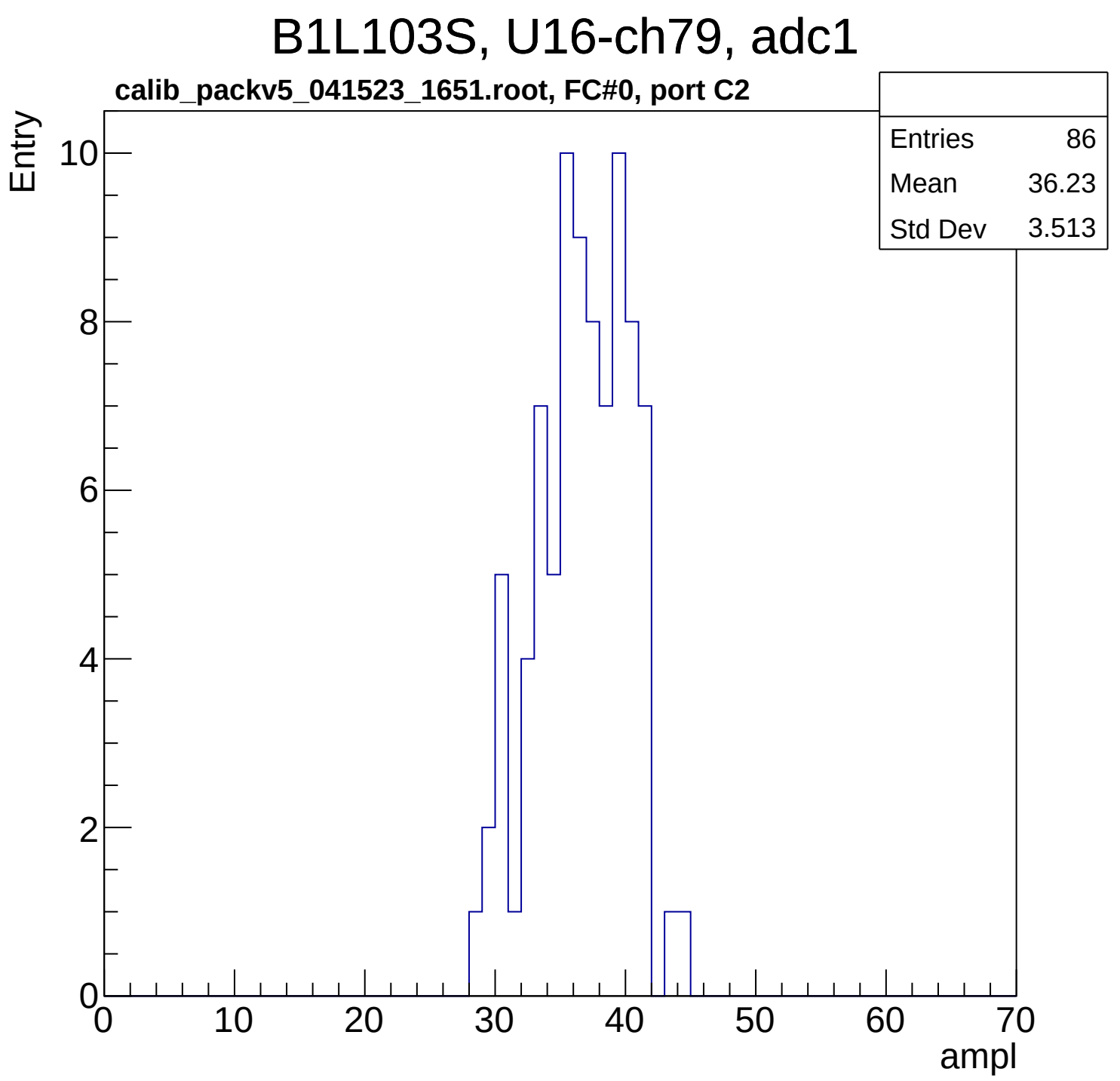
B1L103S, U16-ch79, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 36.23
Std Dev 3.513
Entry
ampl
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0
10
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60
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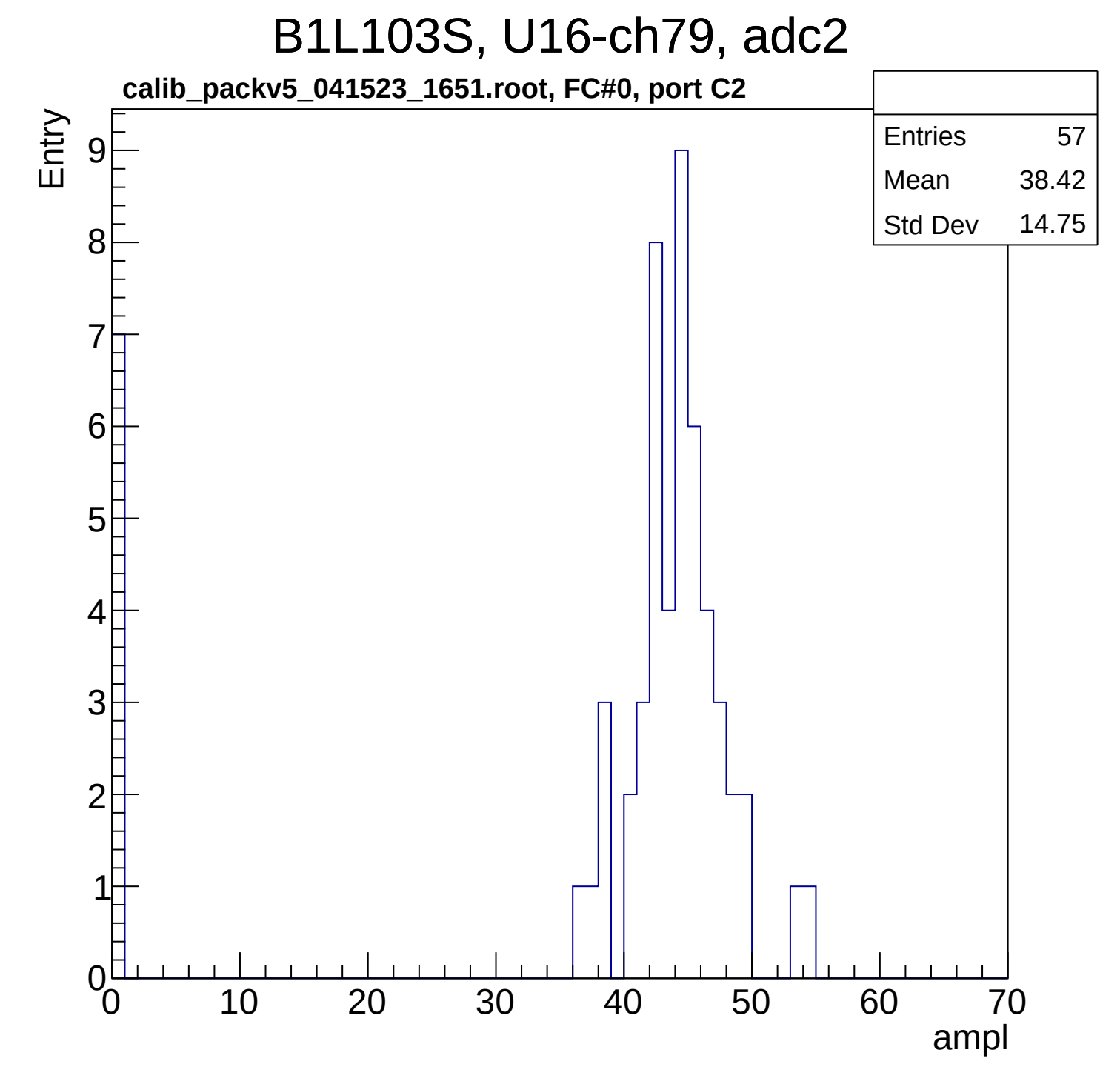
B1L103S, U16-ch79, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 38.42
Std Dev 14.75
Entry
ampl
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3
4
5
6
7
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0
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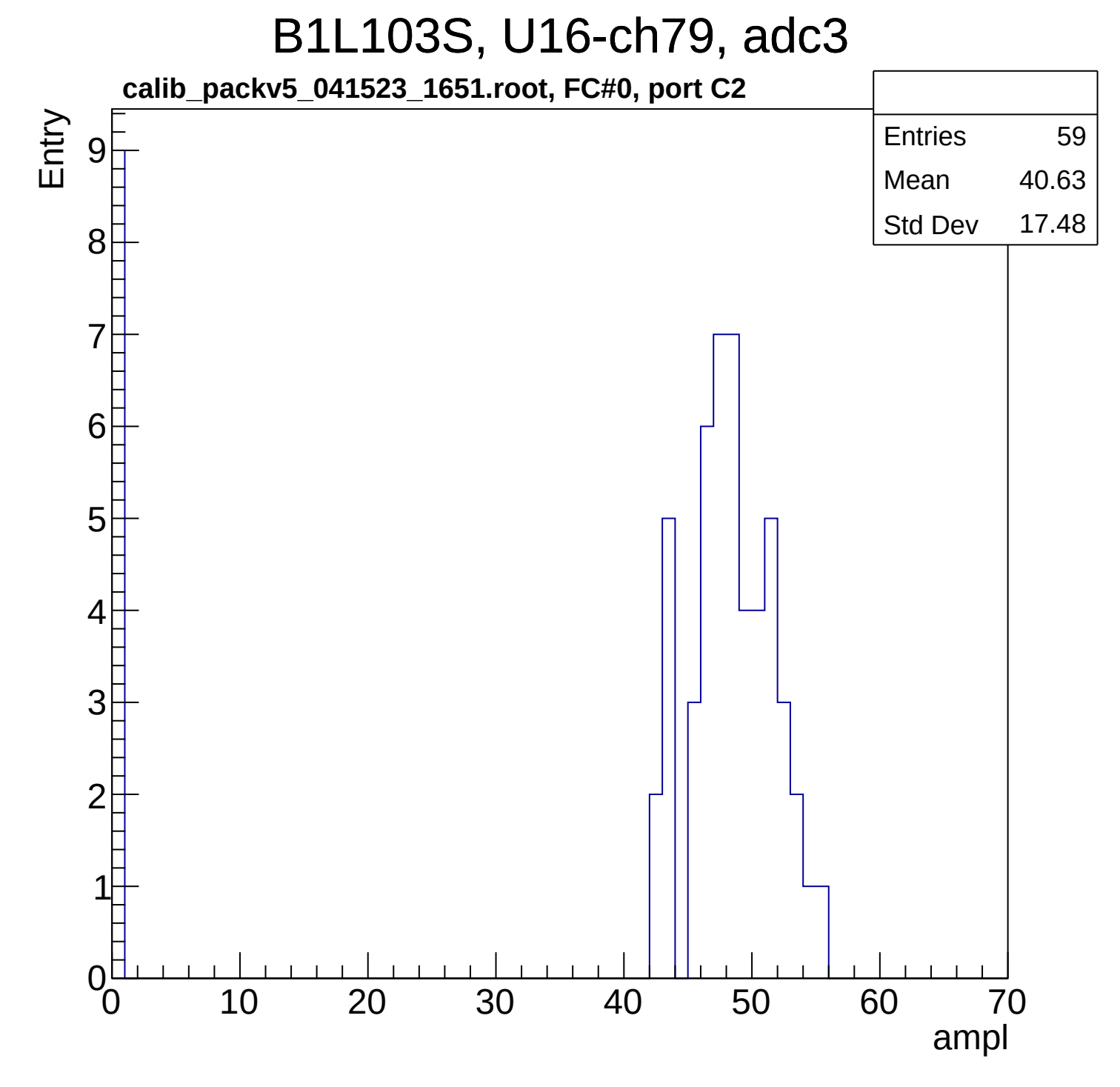
B1L103S, U16-ch79, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 40.63
Std Dev 17.48
Entry
ampl
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4
5
6
7
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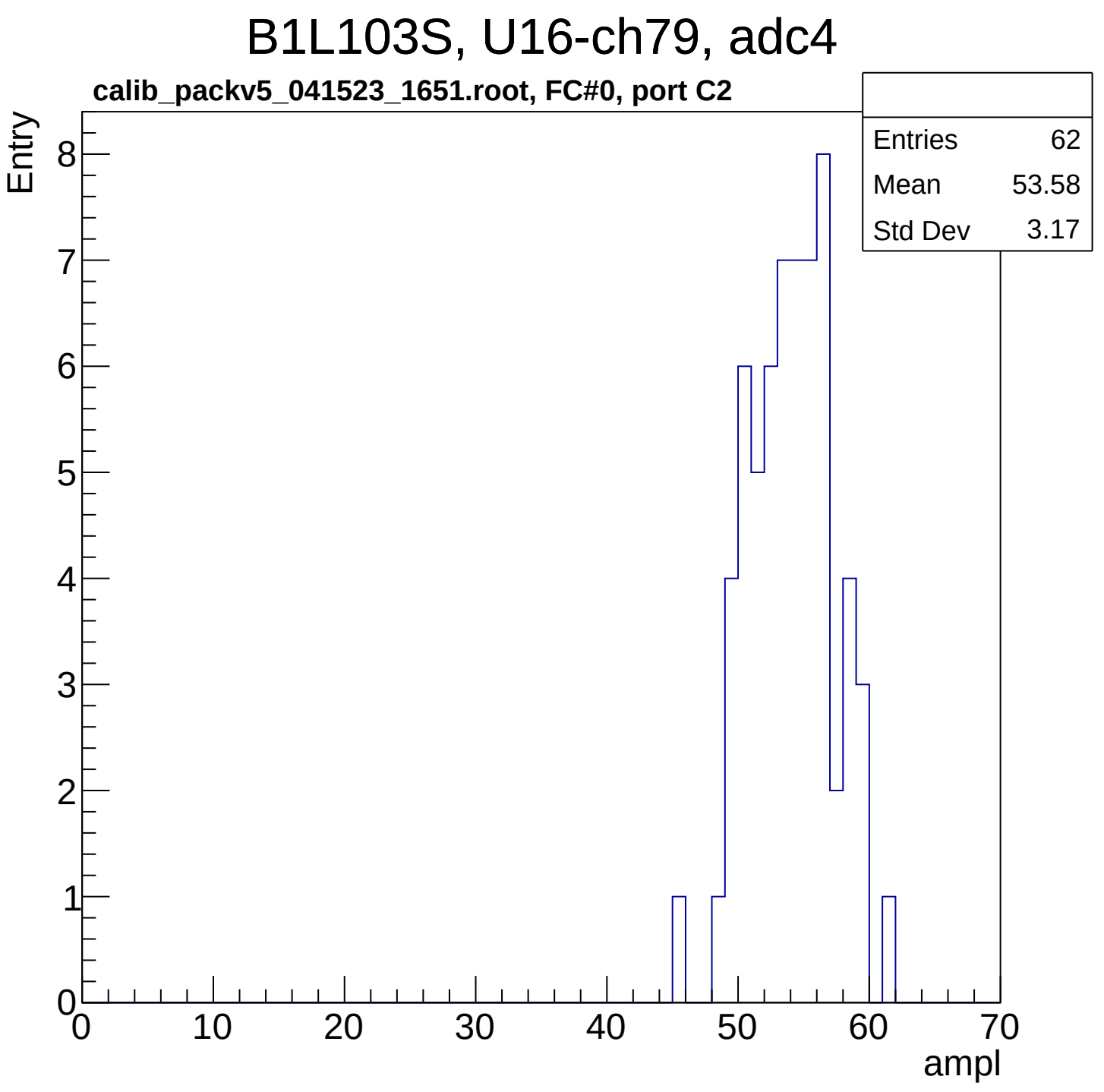
B1L103S, U16-ch79, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 53.58
Std Dev 3.17
Entry
ampl
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4
5
6
7
8
0
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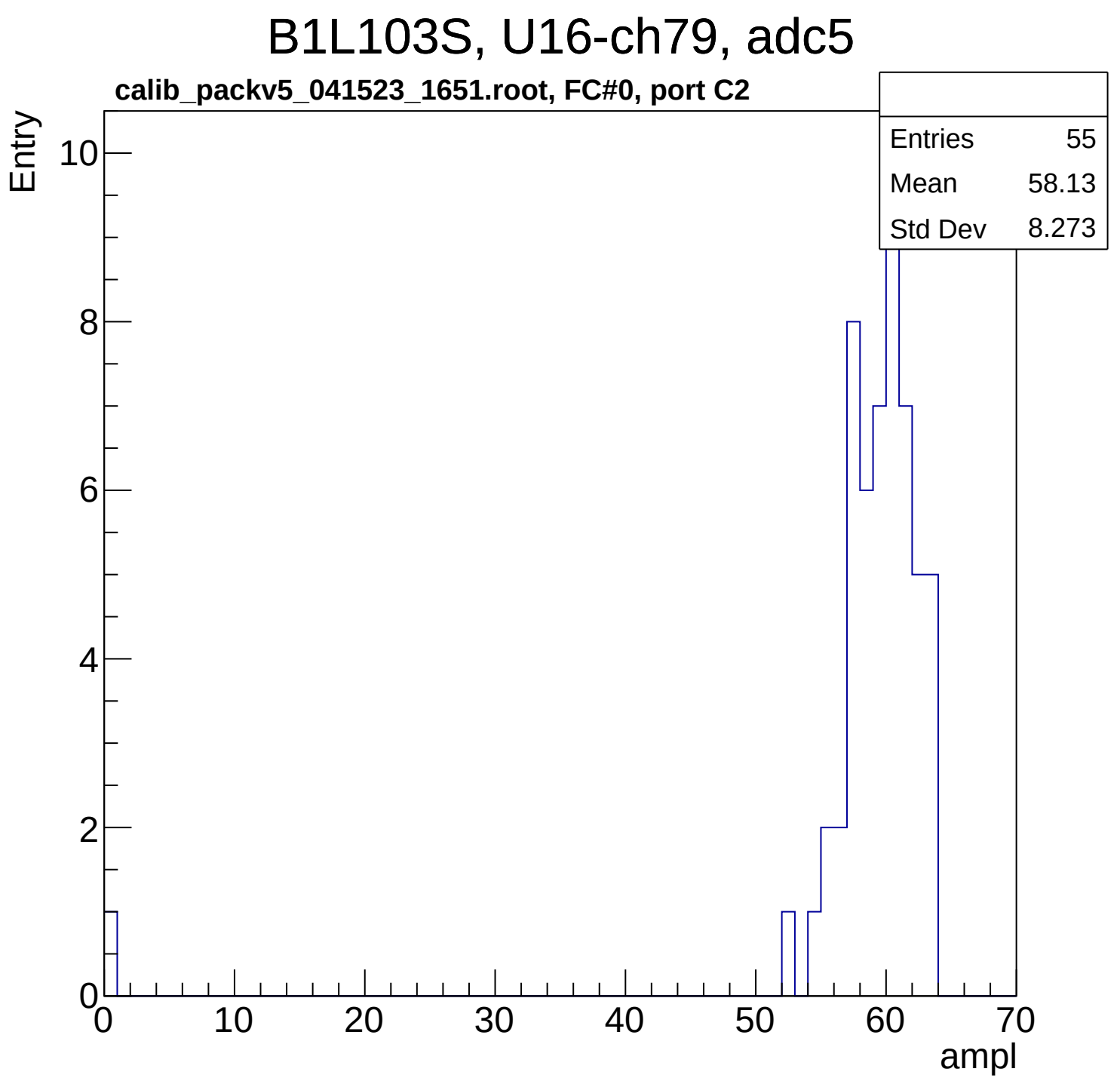
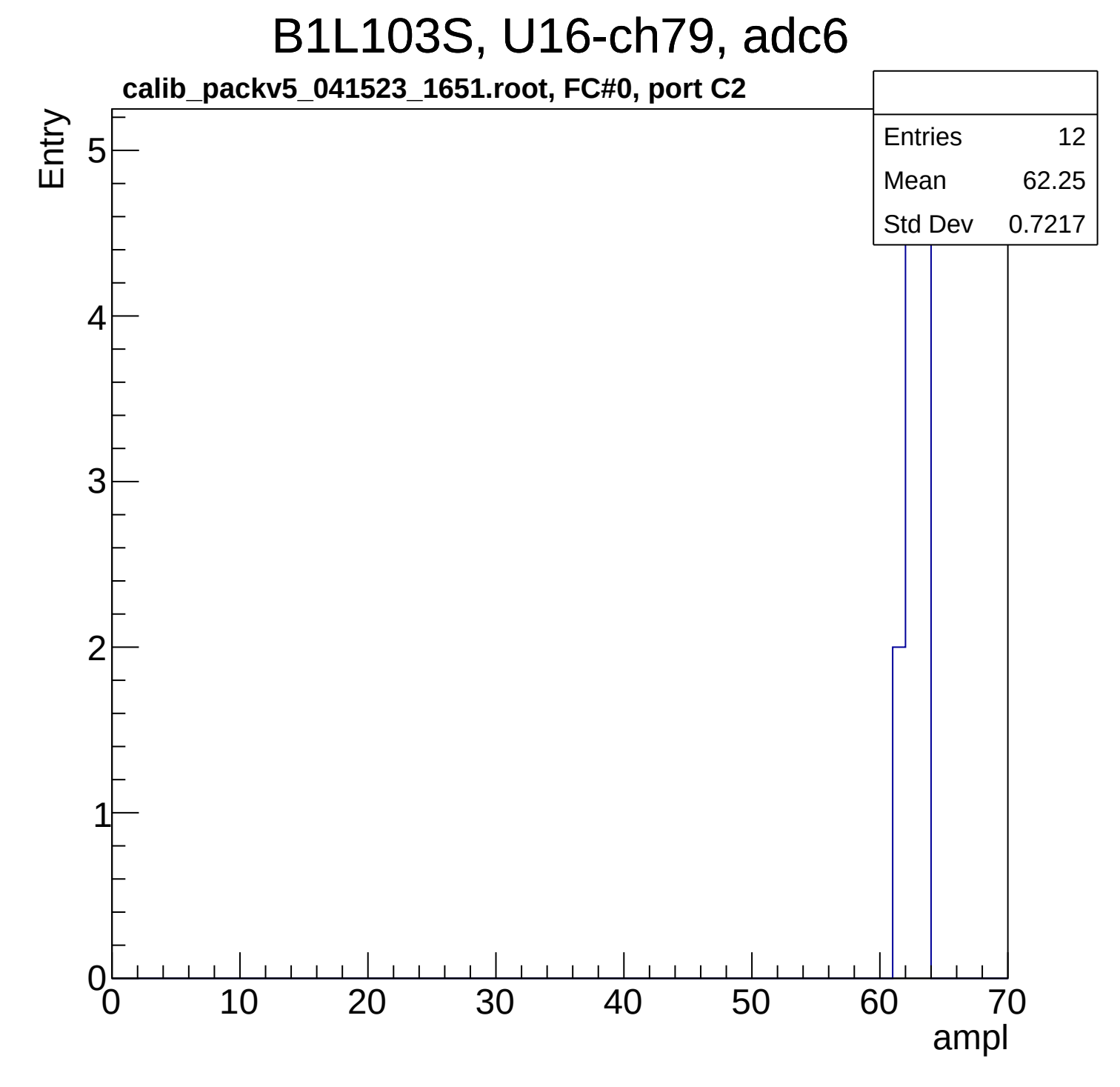

B1L103S, U16-ch79, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.13
Std Dev 8.273
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch79, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 62.25
Std Dev 0.7217
Entry
ampl
0
1
2
3
4
5
0
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60
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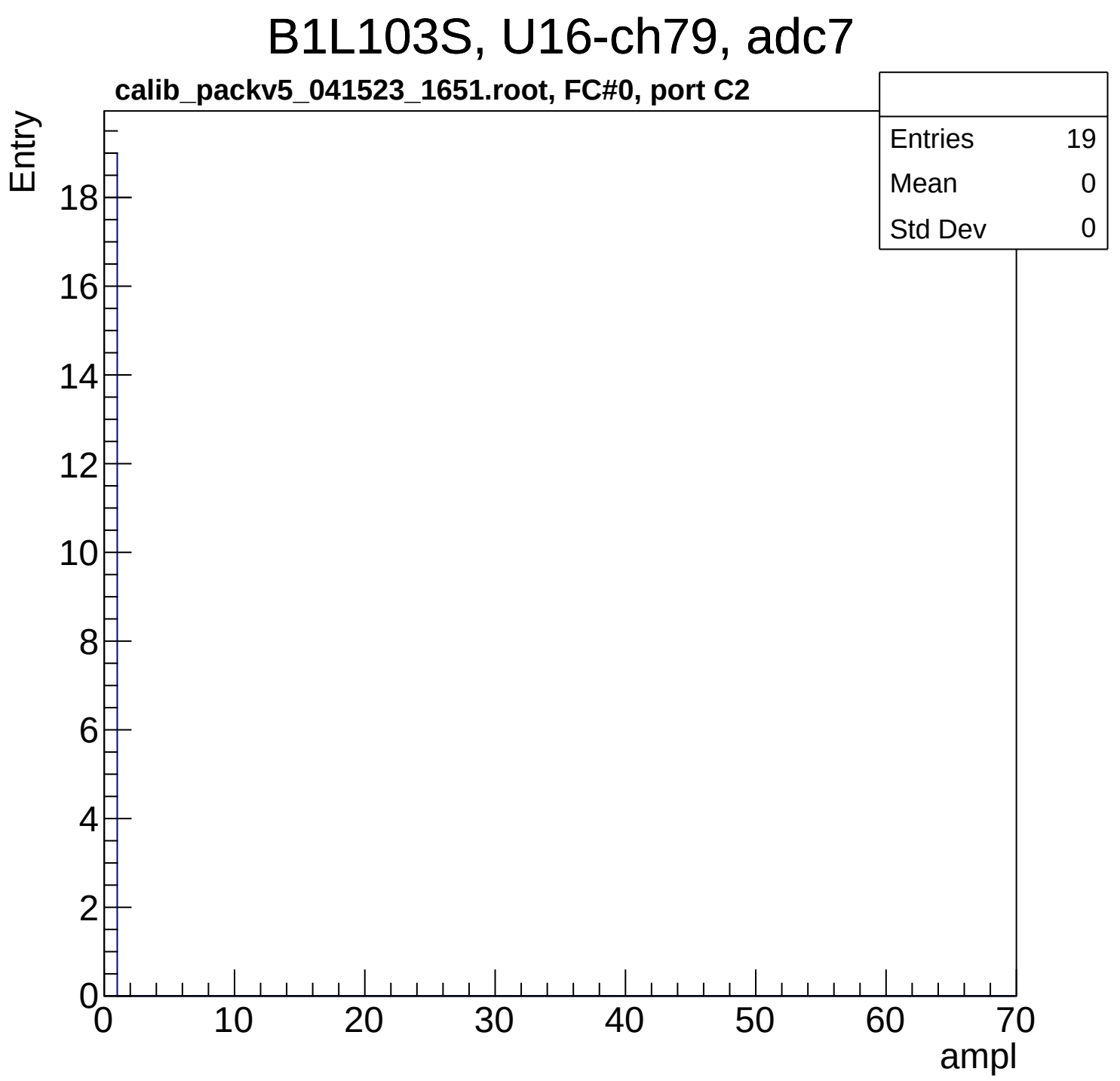
B1L103S, U16-ch79, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
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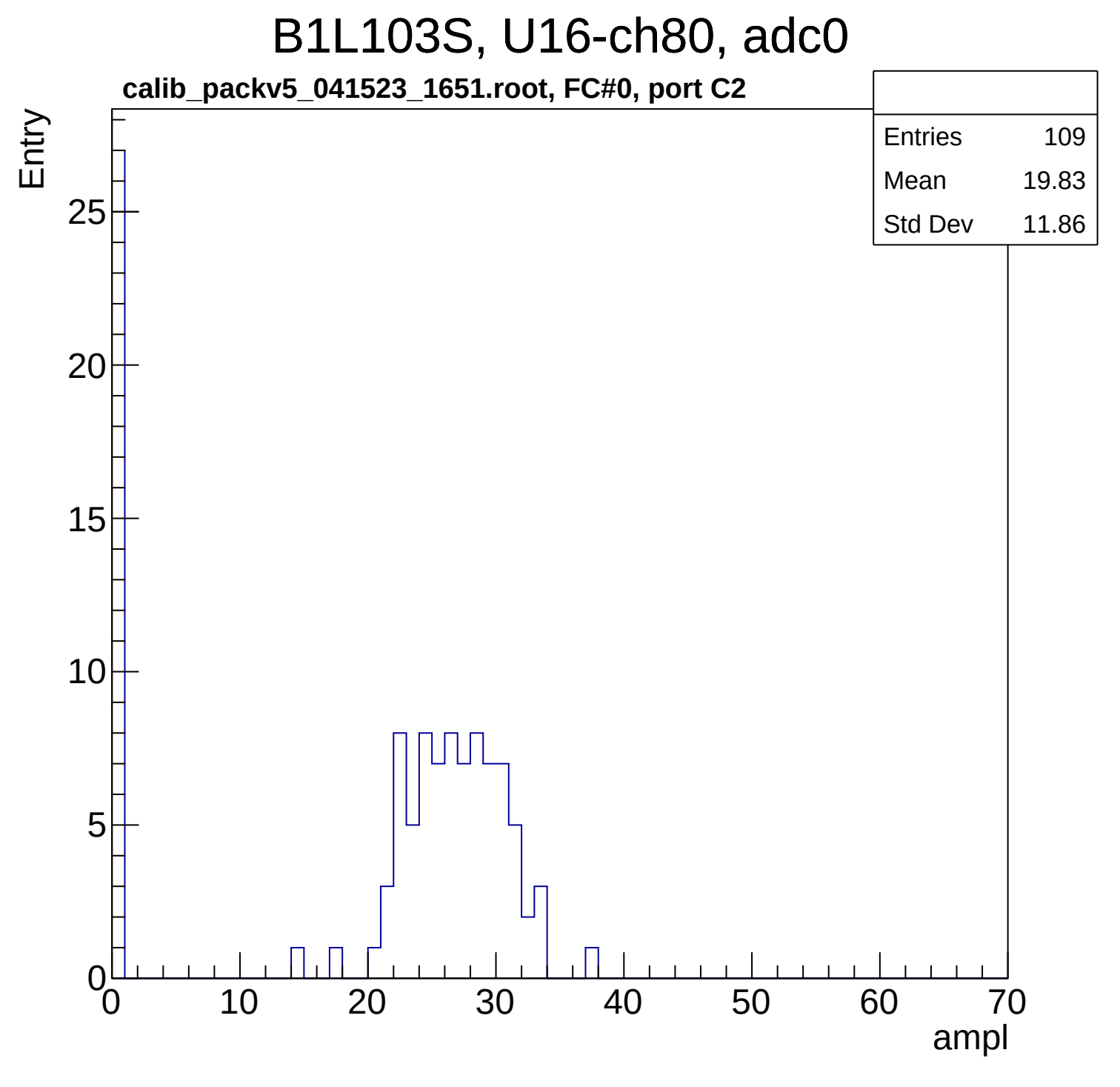
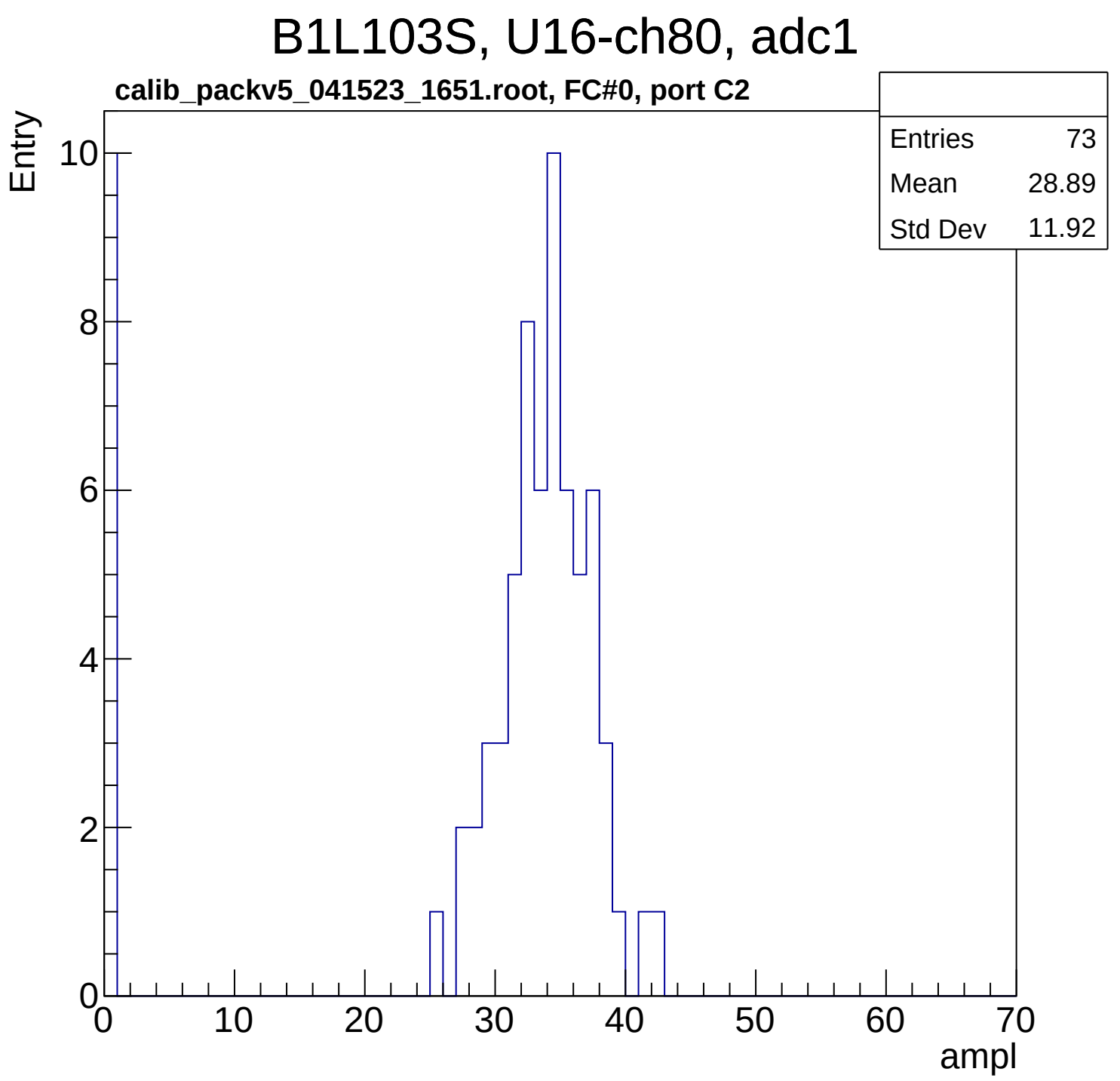
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch80, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 109
Mean 19.83
Std Dev 11.86
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch80, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 28.89
Std Dev 11.92
Entry
ampl
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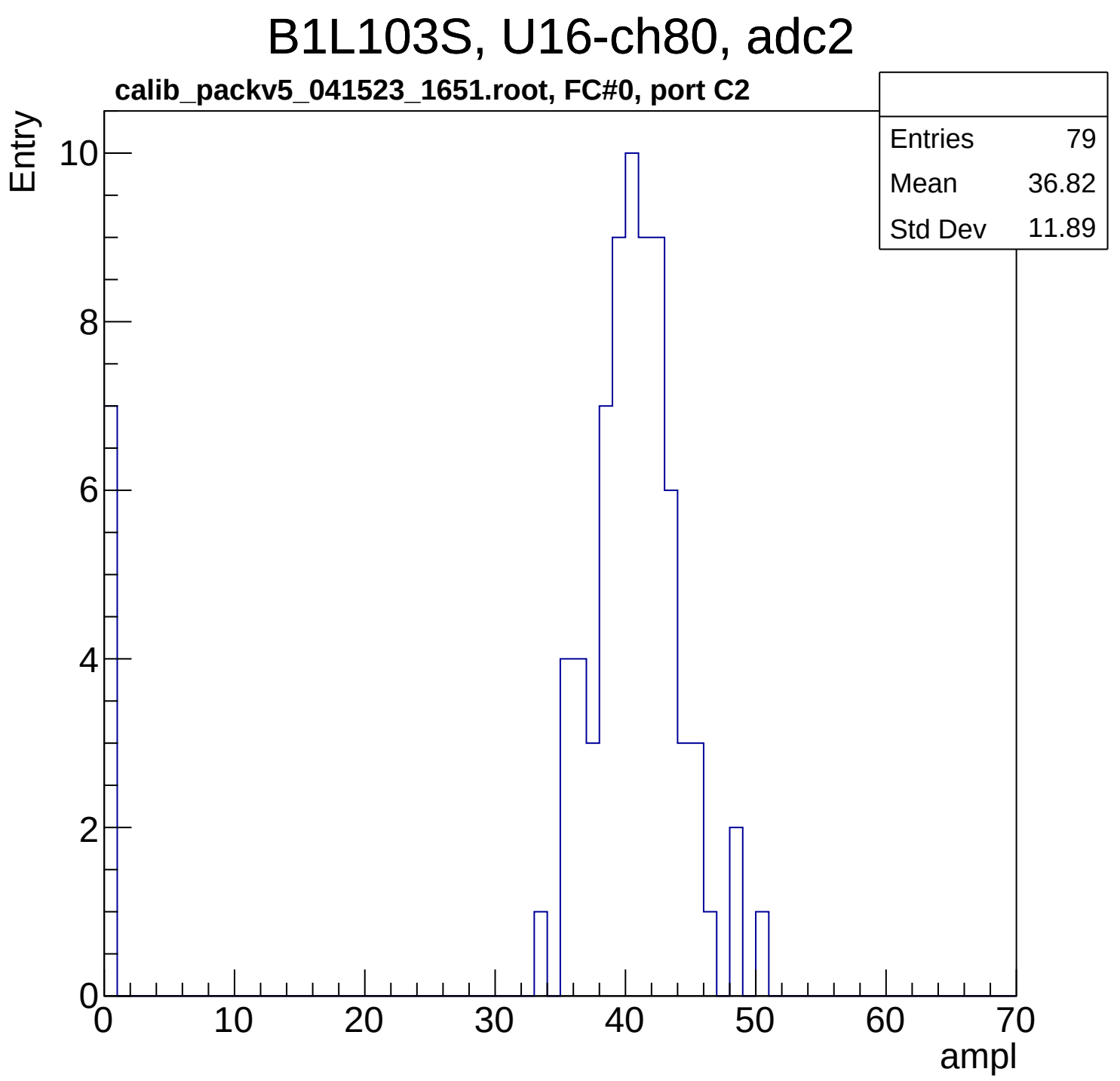
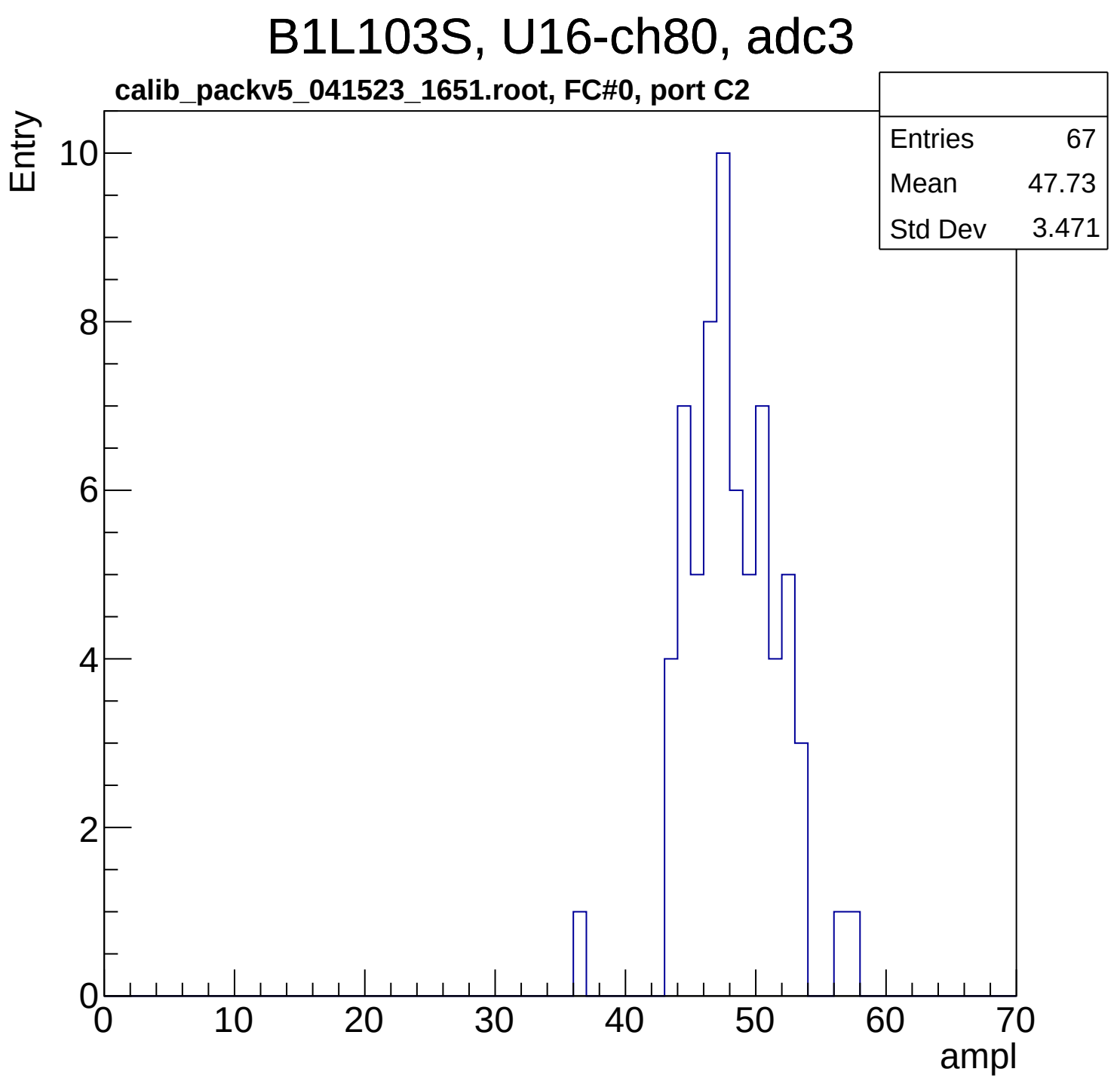
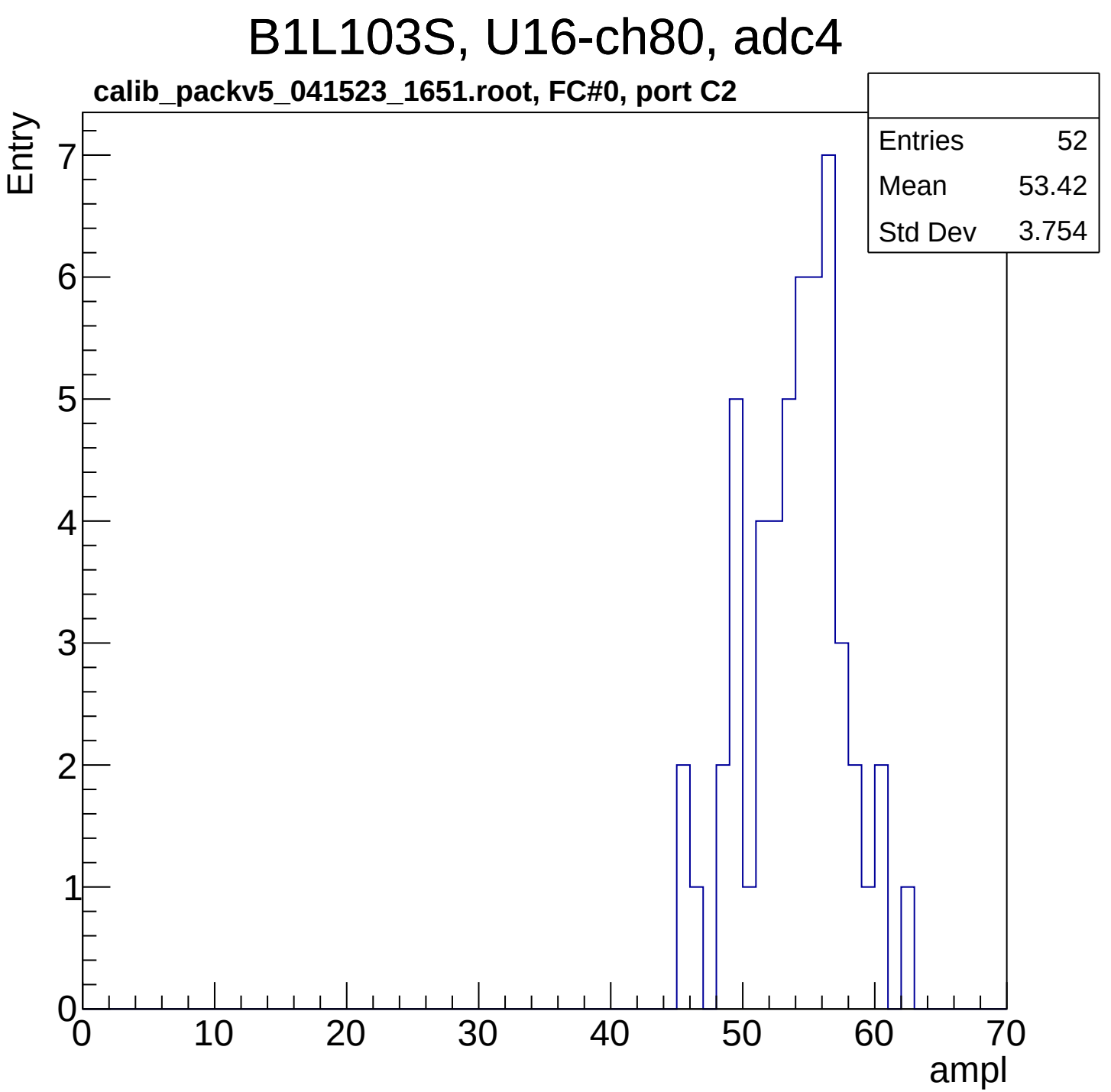
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch80, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 36.82
Std Dev 11.89
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch80, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 47.73
Std Dev 3.471
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch80, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 53.42
Std Dev 3.754
Entry
ampl
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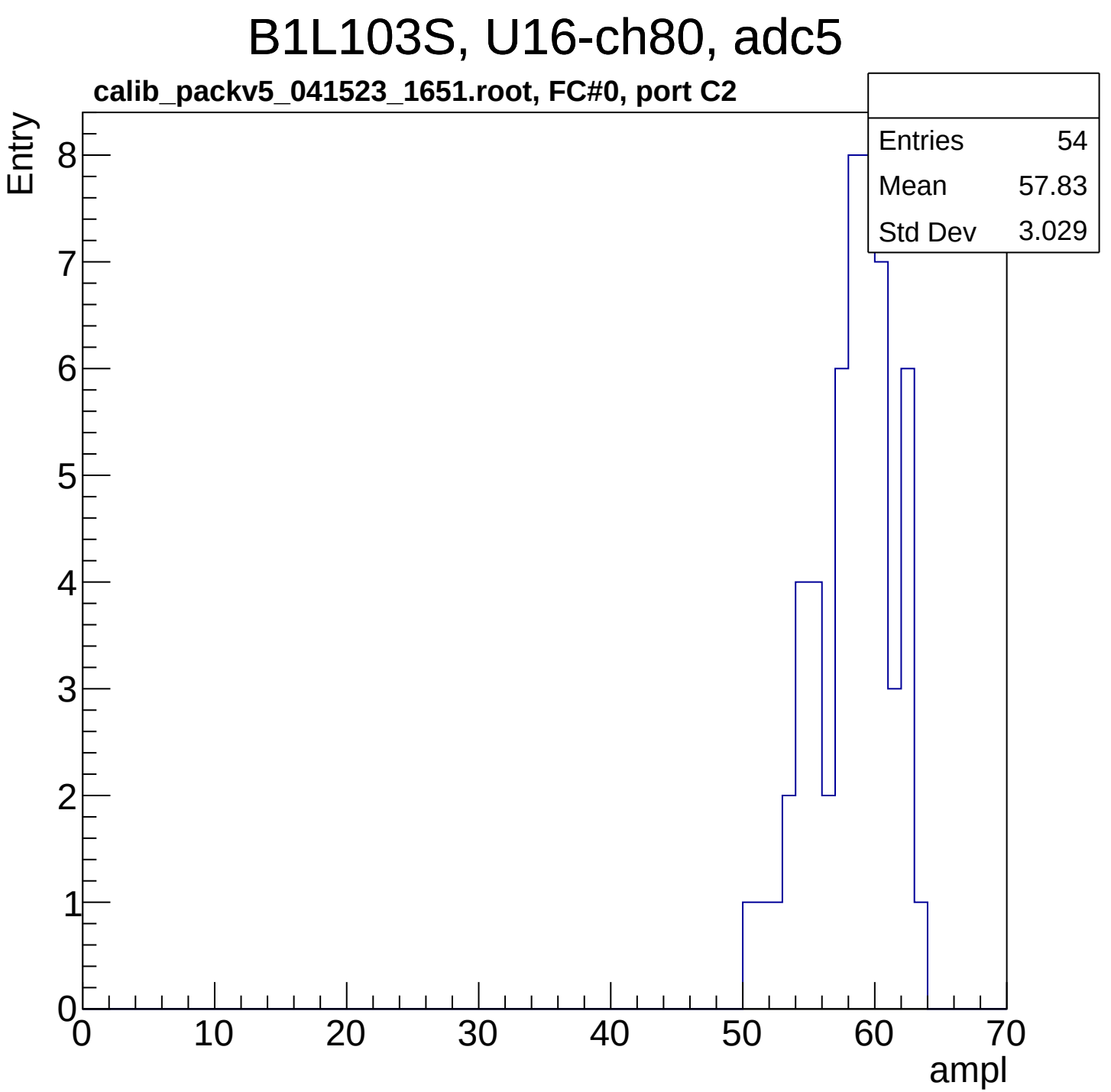
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch80, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.83
Std Dev 3.029
Entry
ampl
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2
3
4
5
6
7
8
0
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40
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60
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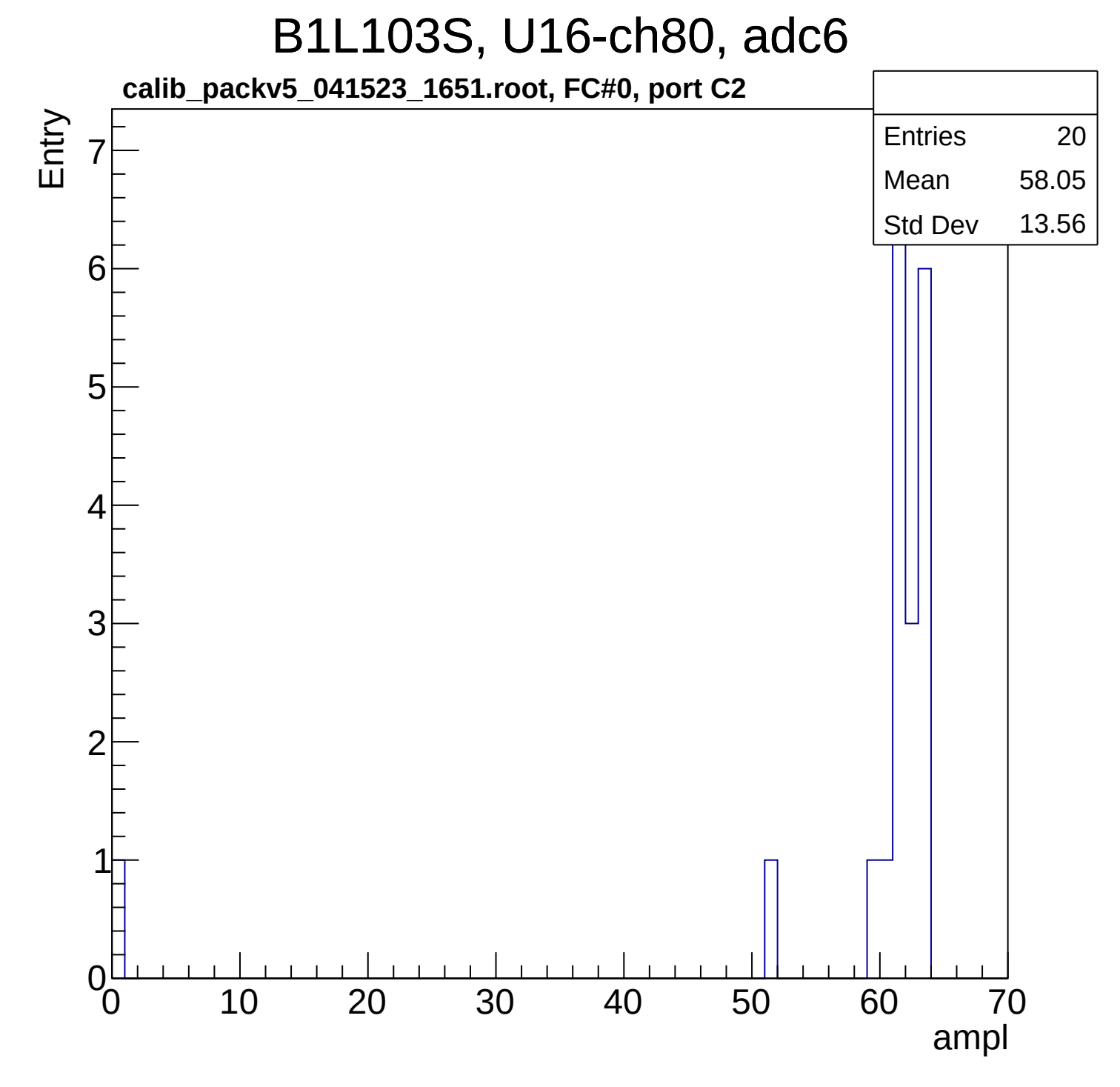
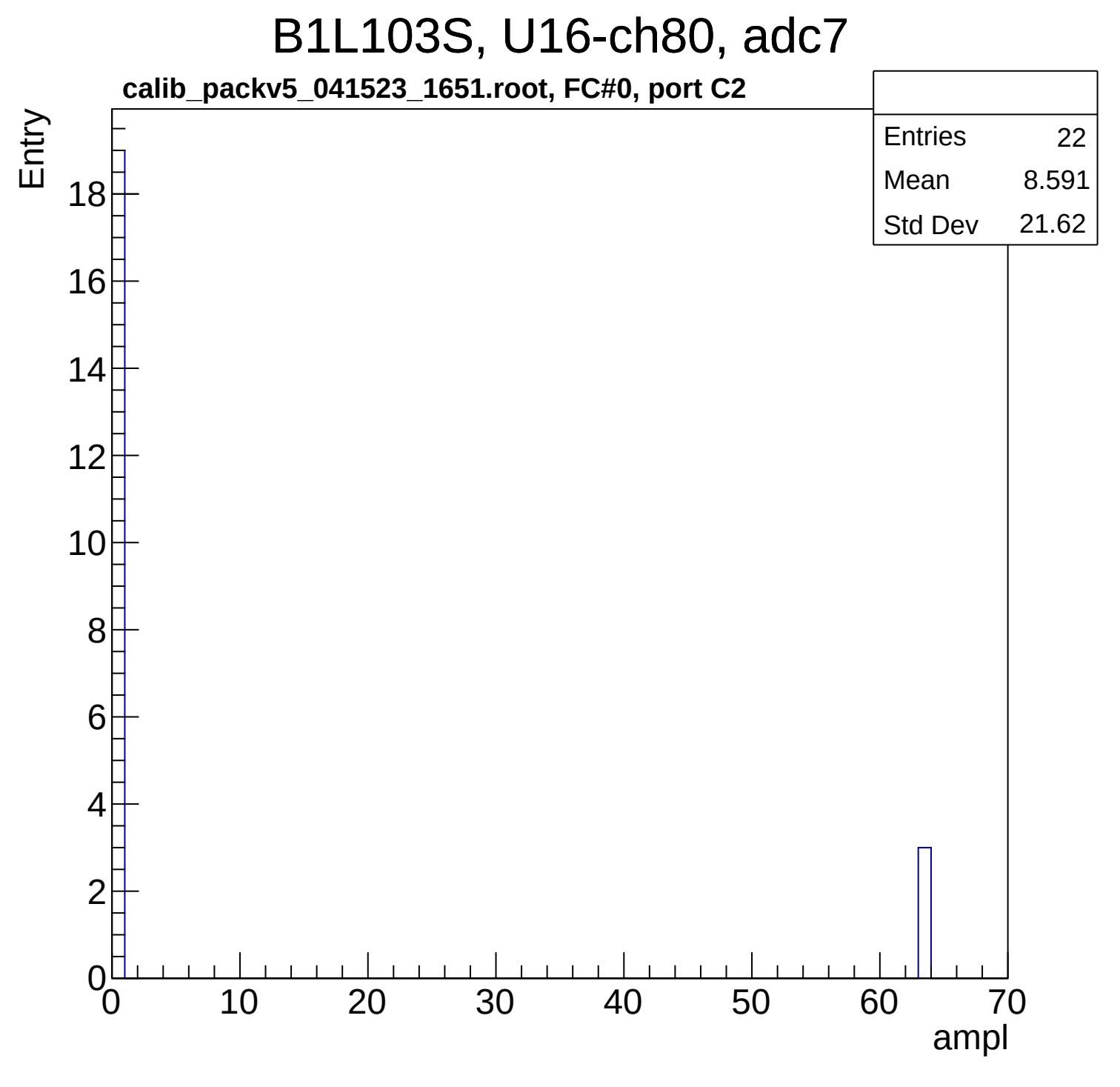
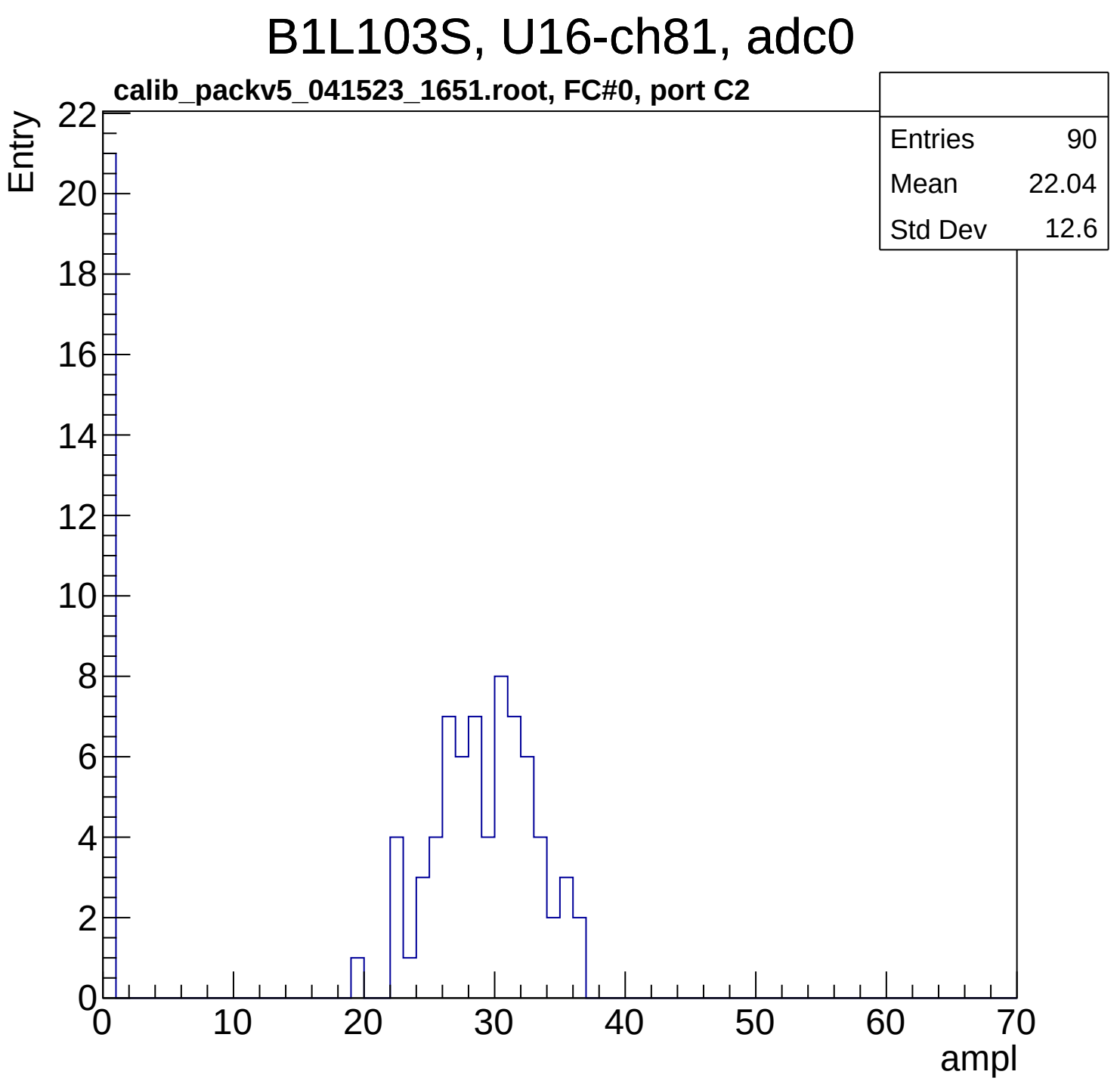

B1L103S, U16-ch80, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 58.05
Std Dev 13.56
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch80, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.591
Std Dev 21.62
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch81, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 22.04
Std Dev 12.6
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
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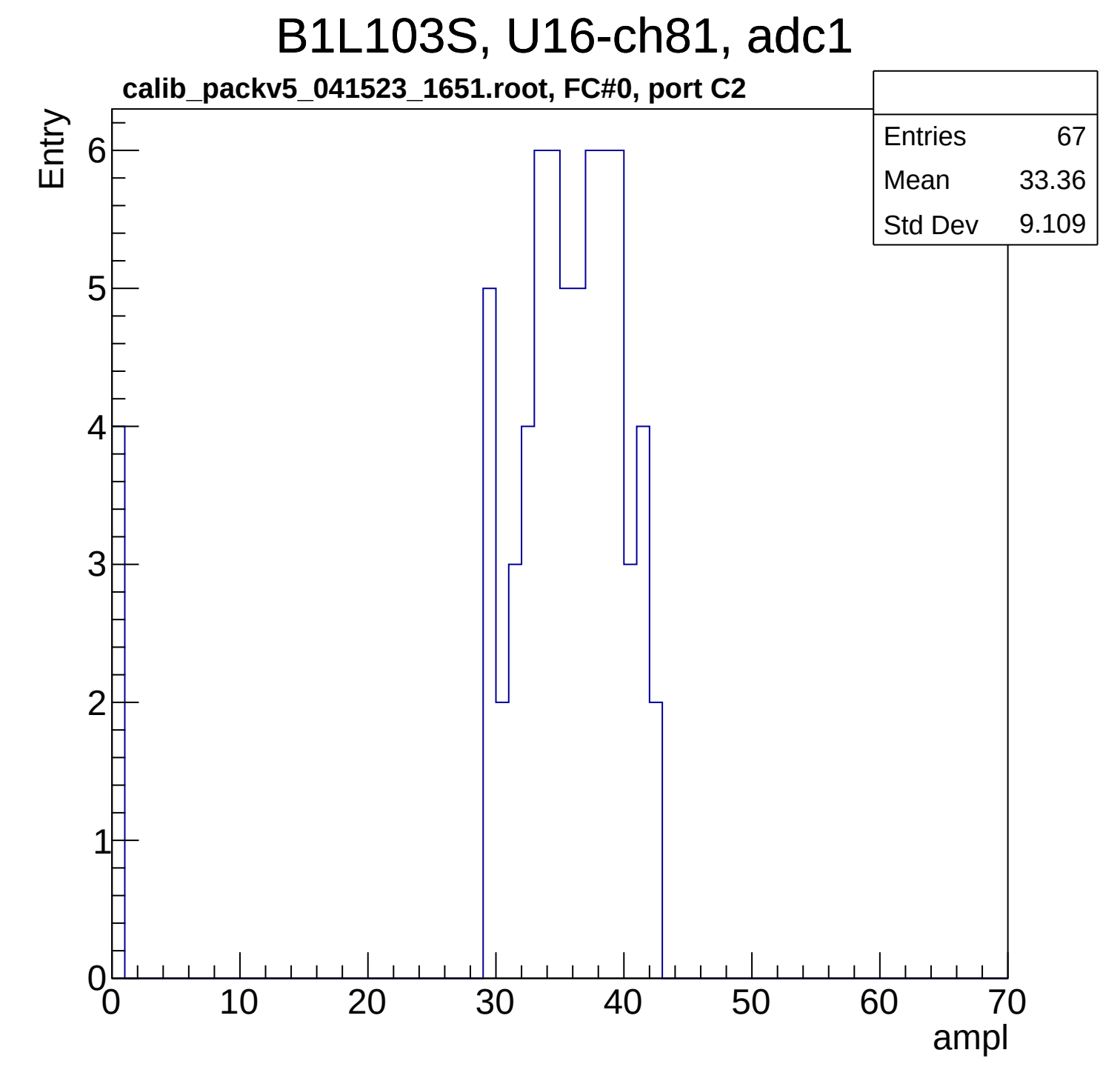
B1L103S, U16-ch81, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 33.36
Std Dev 9.109
Entry
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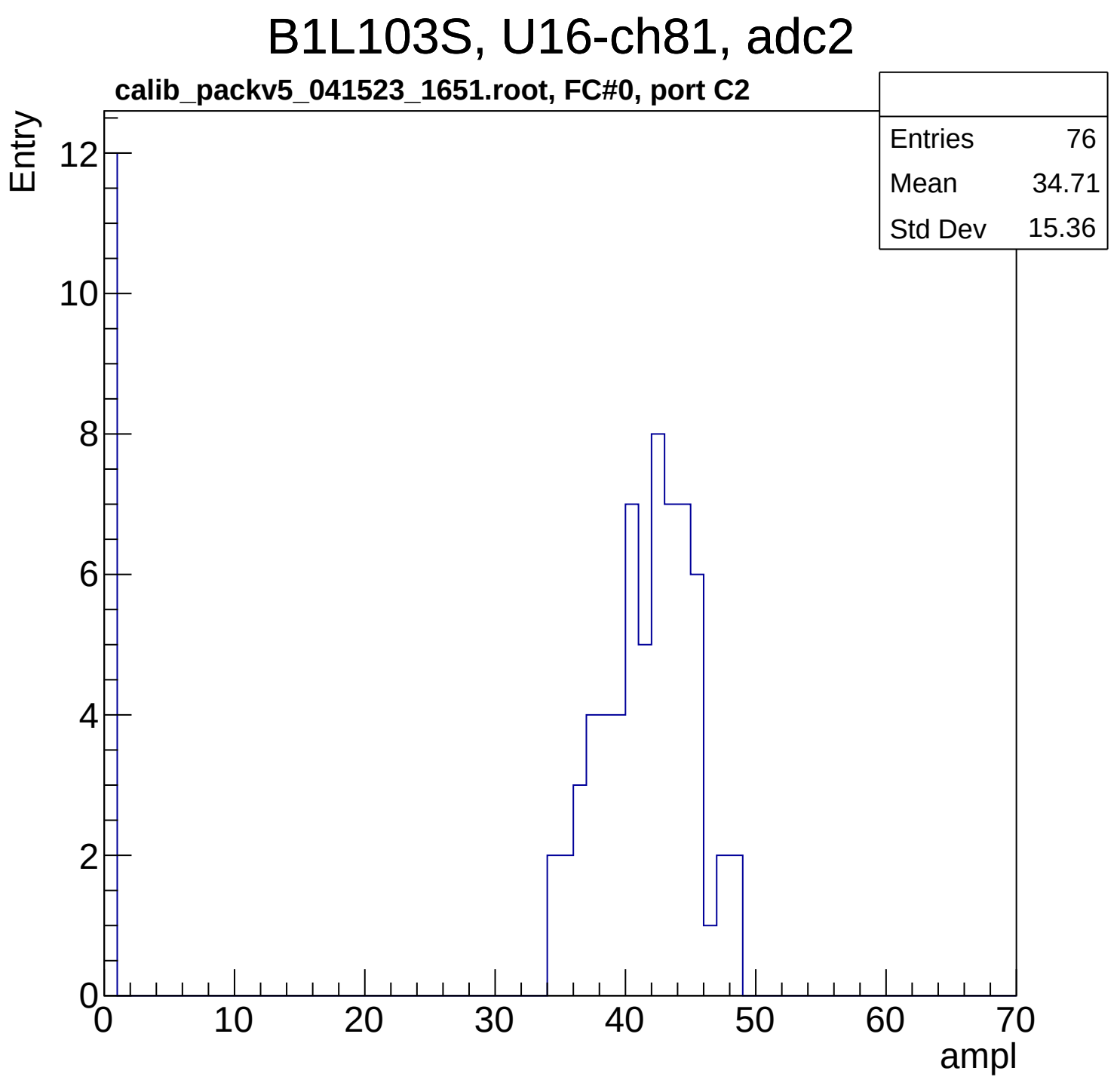
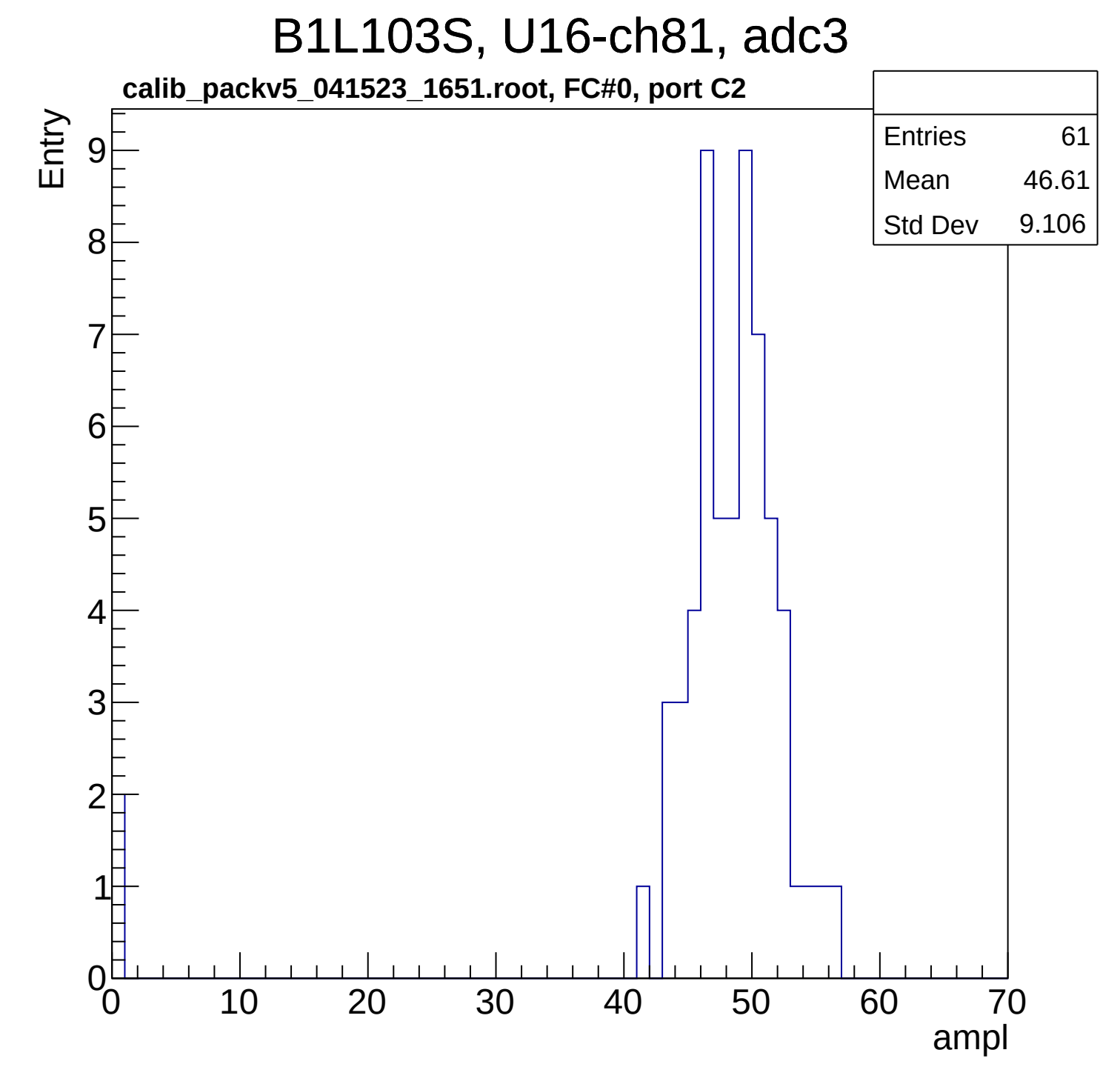
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch81, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 34.71
Std Dev 15.36
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch81, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 46.61
Std Dev 9.106
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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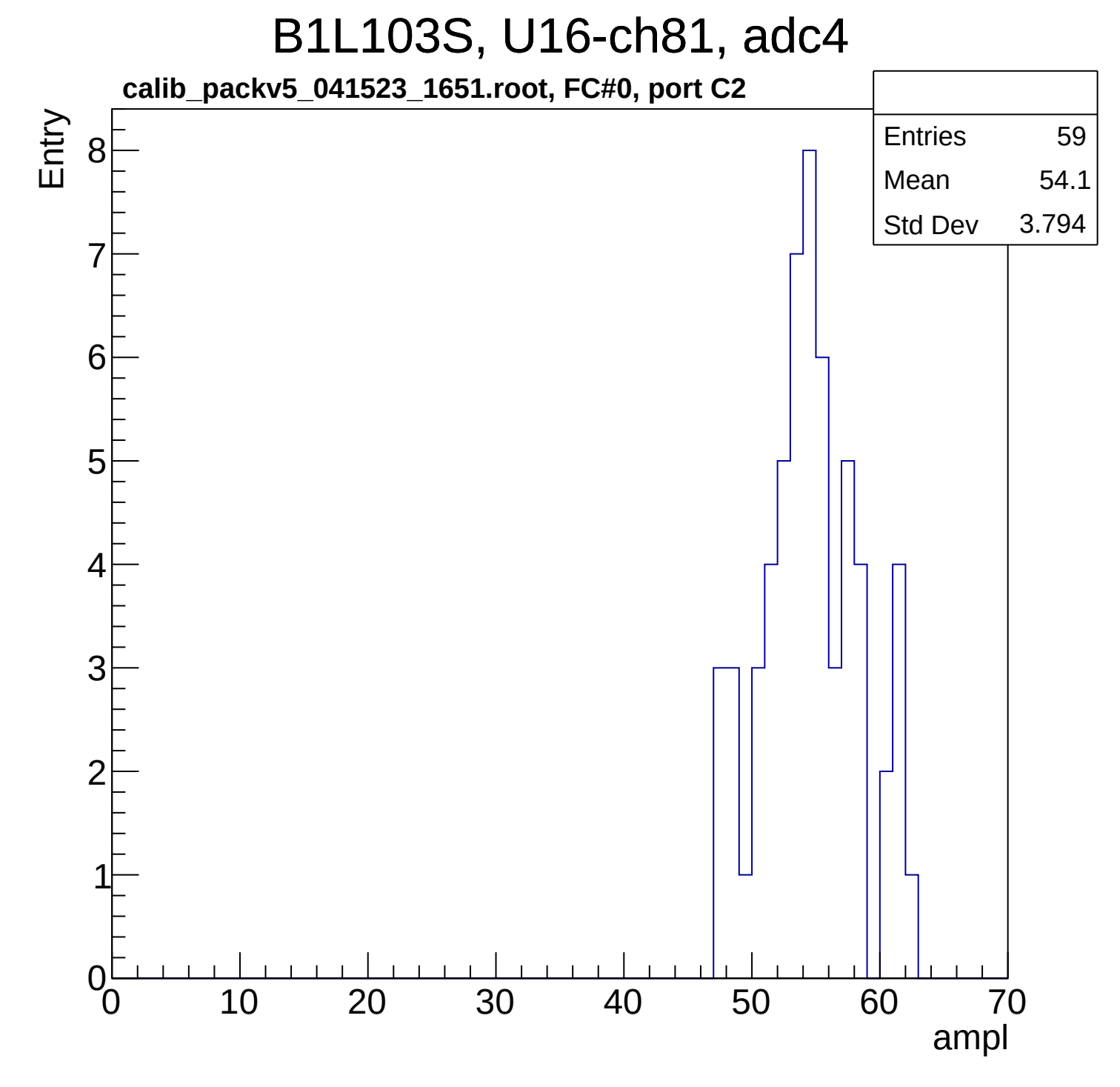
B1L103S, U16-ch81, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.1
Std Dev 3.794
Entry
ampl
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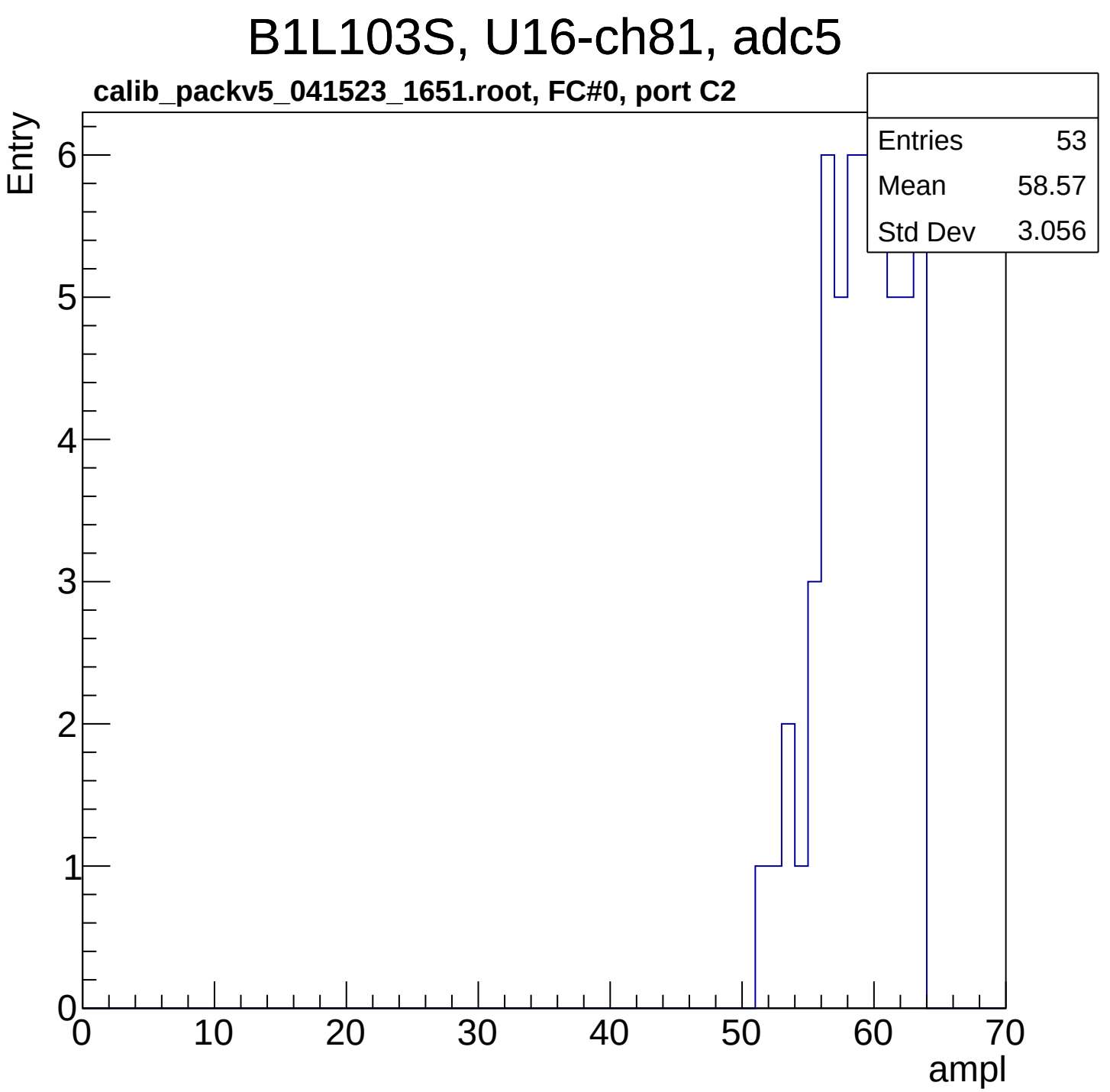
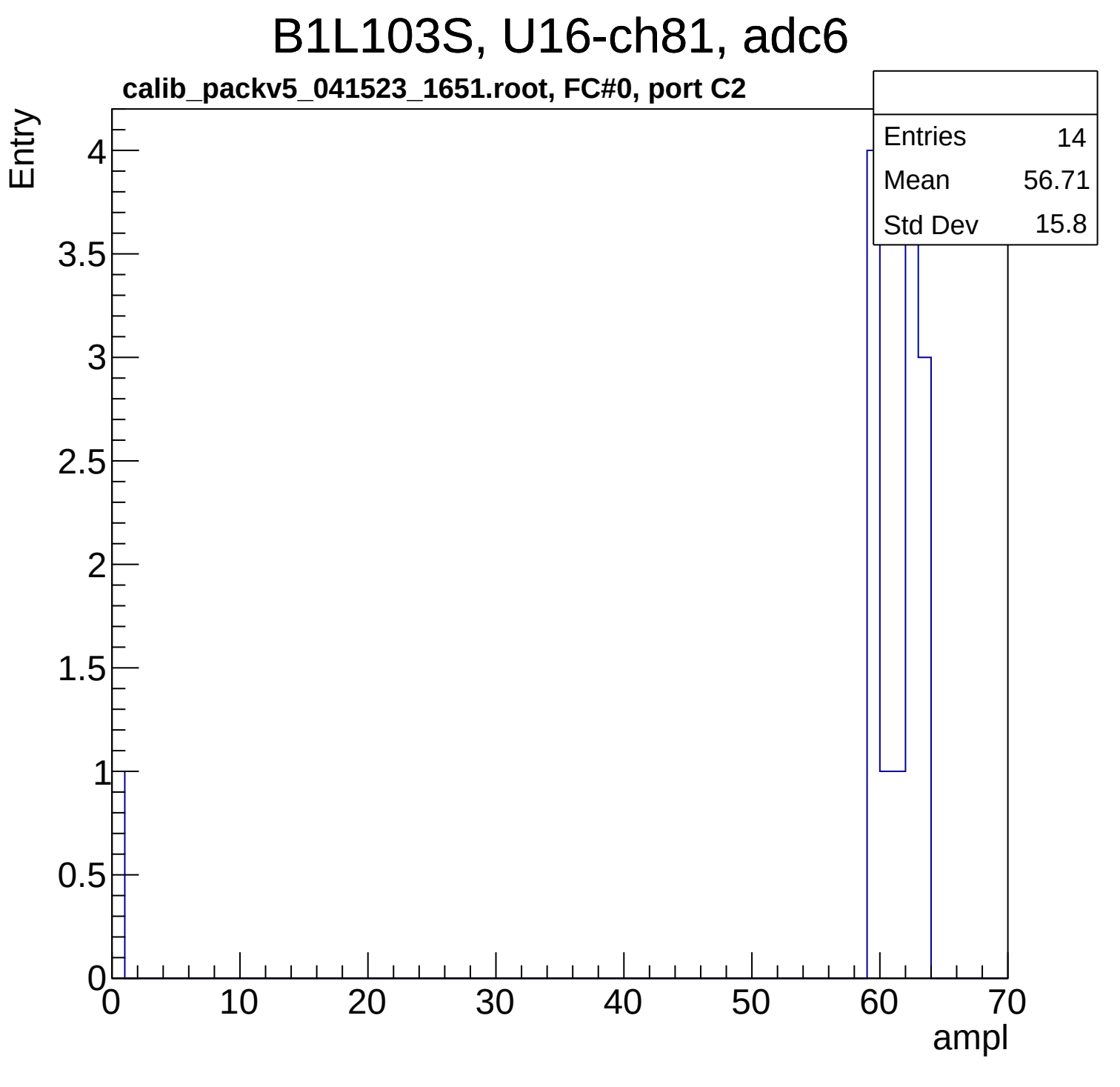
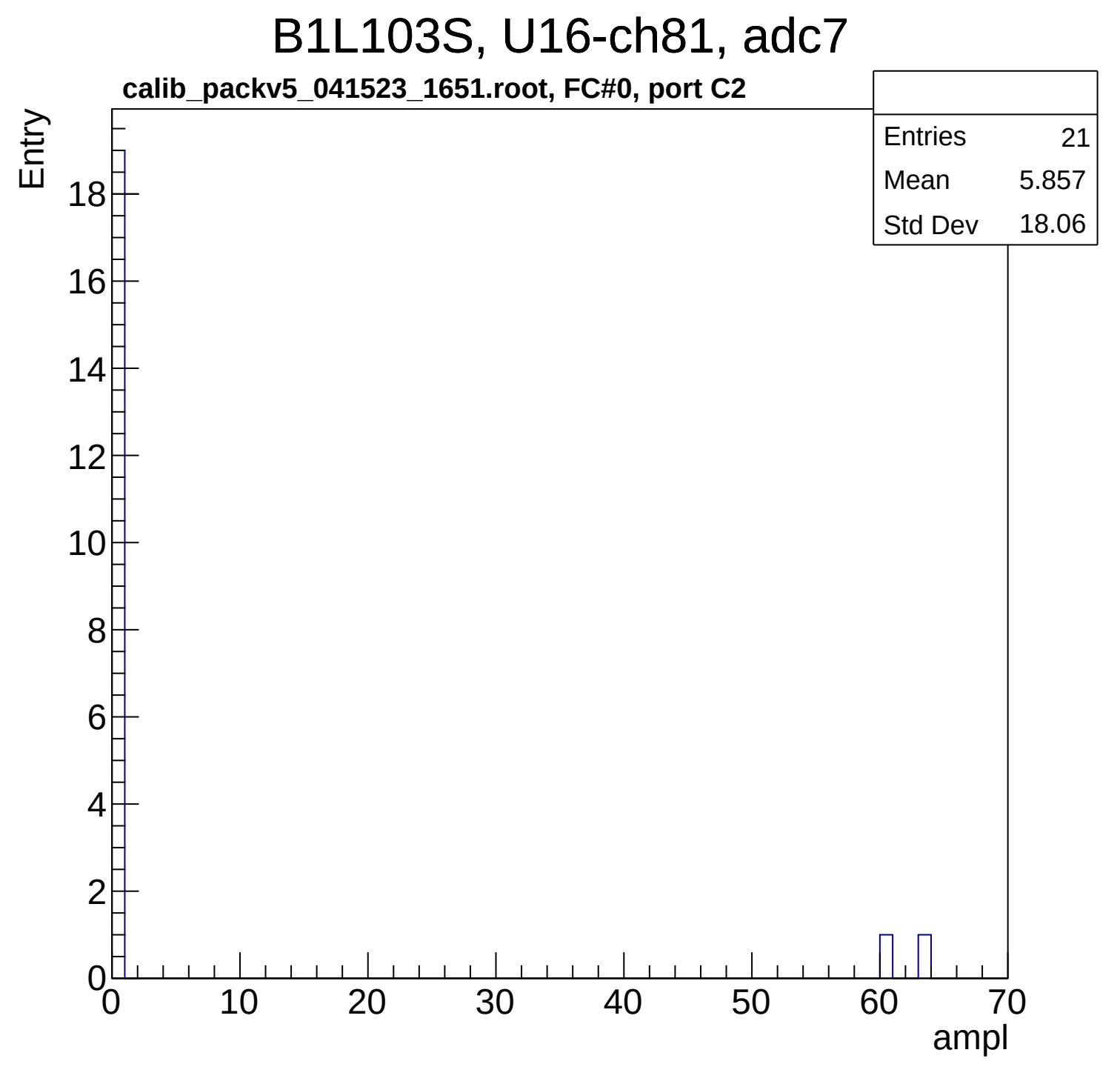
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch81, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.57
Std Dev 3.056
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch81, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 56.71
Std Dev 15.8
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U16-ch81, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.857
Std Dev 18.06
Entry
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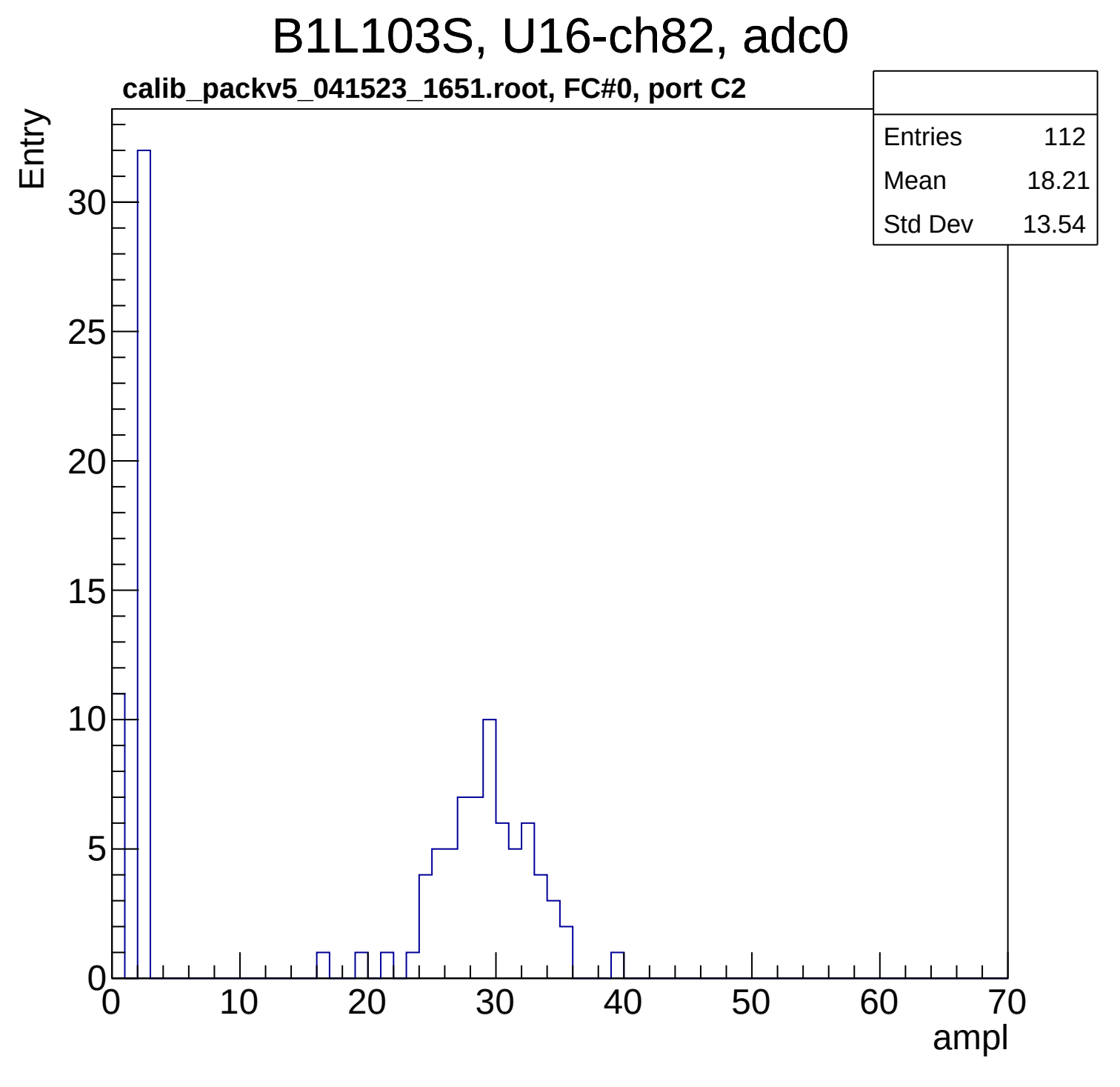
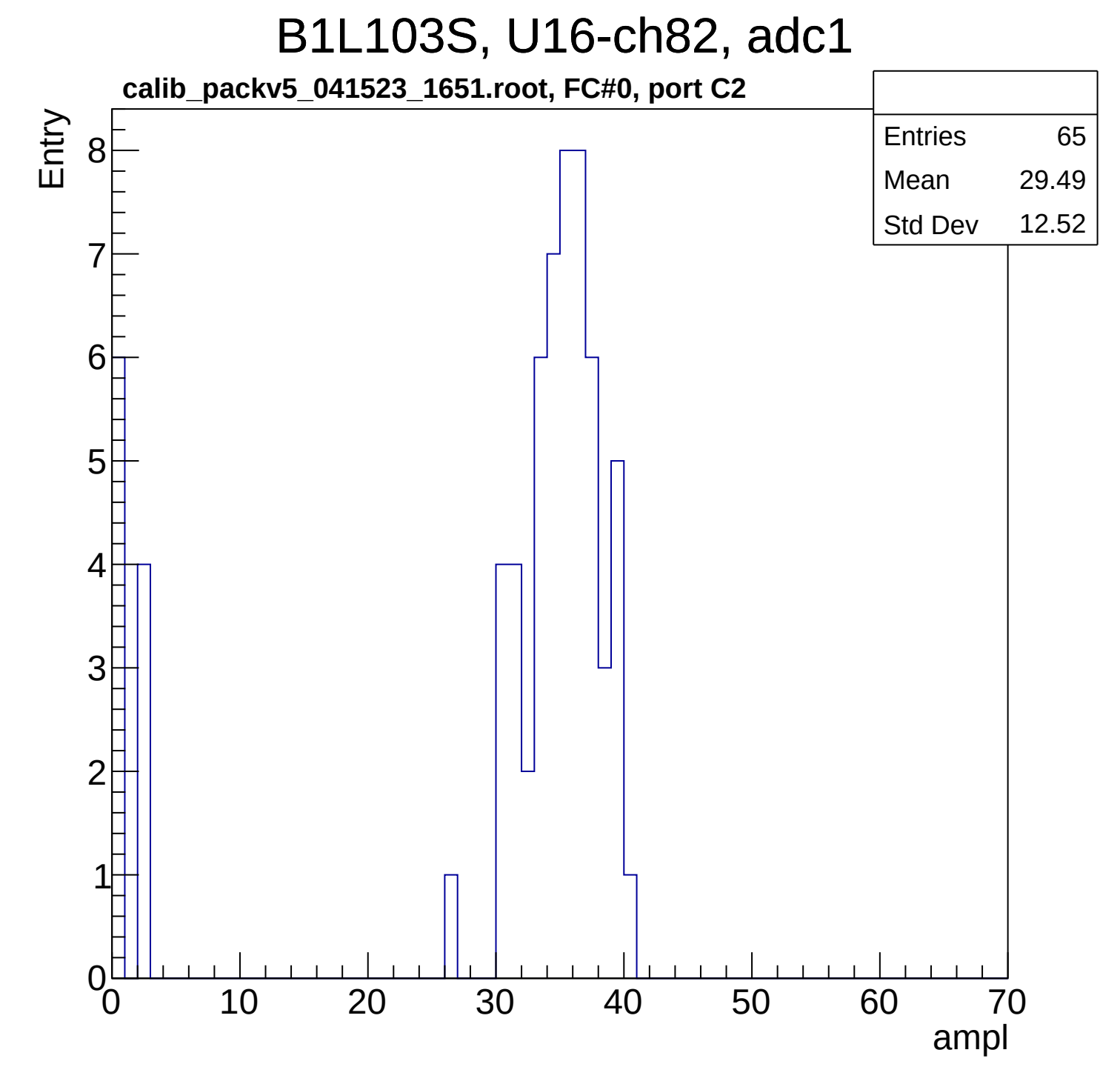
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch82, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 112
Mean 18.21
Std Dev 13.54
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch82, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 29.49
Std Dev 12.52
Entry
ampl
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2
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4
5
6
7
8
0
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20
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40
50
60
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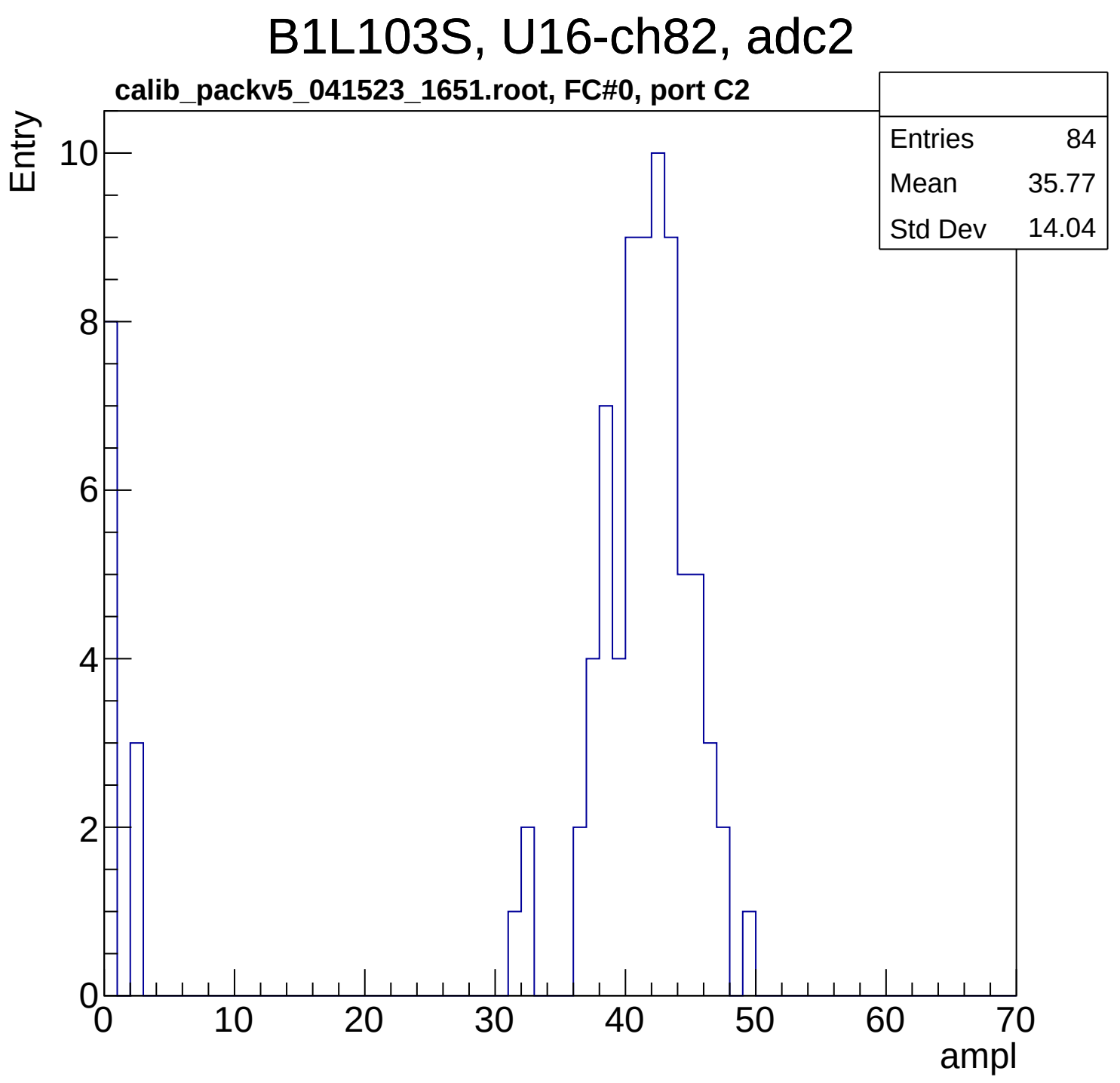
B1L103S, U16-ch82, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 35.77
Std Dev 14.04
Entry
ampl
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4
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8
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0
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20
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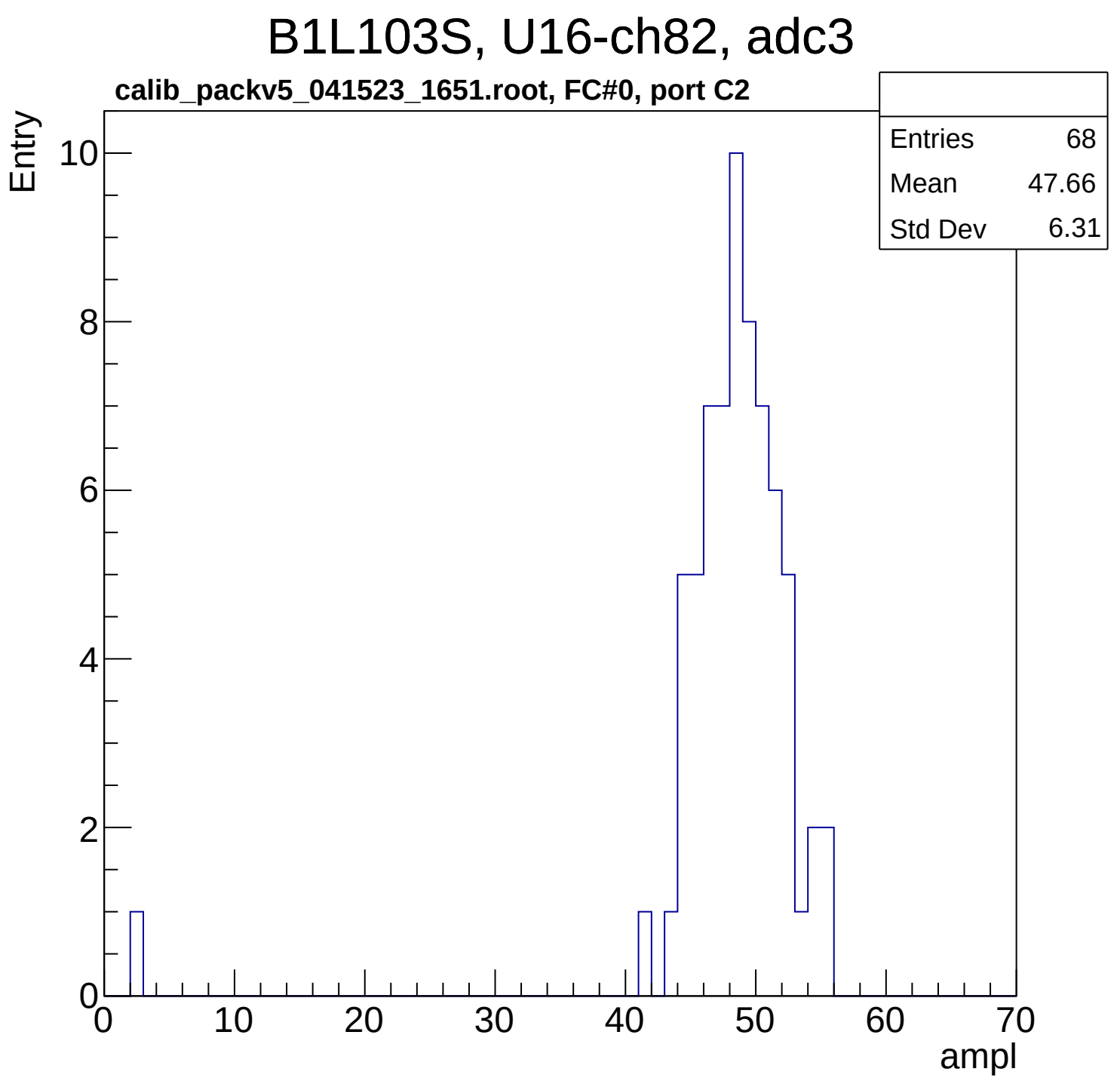
40
50
60
70


B1L103S, U16-ch82, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 47.66
Std Dev 6.31
Entry
ampl
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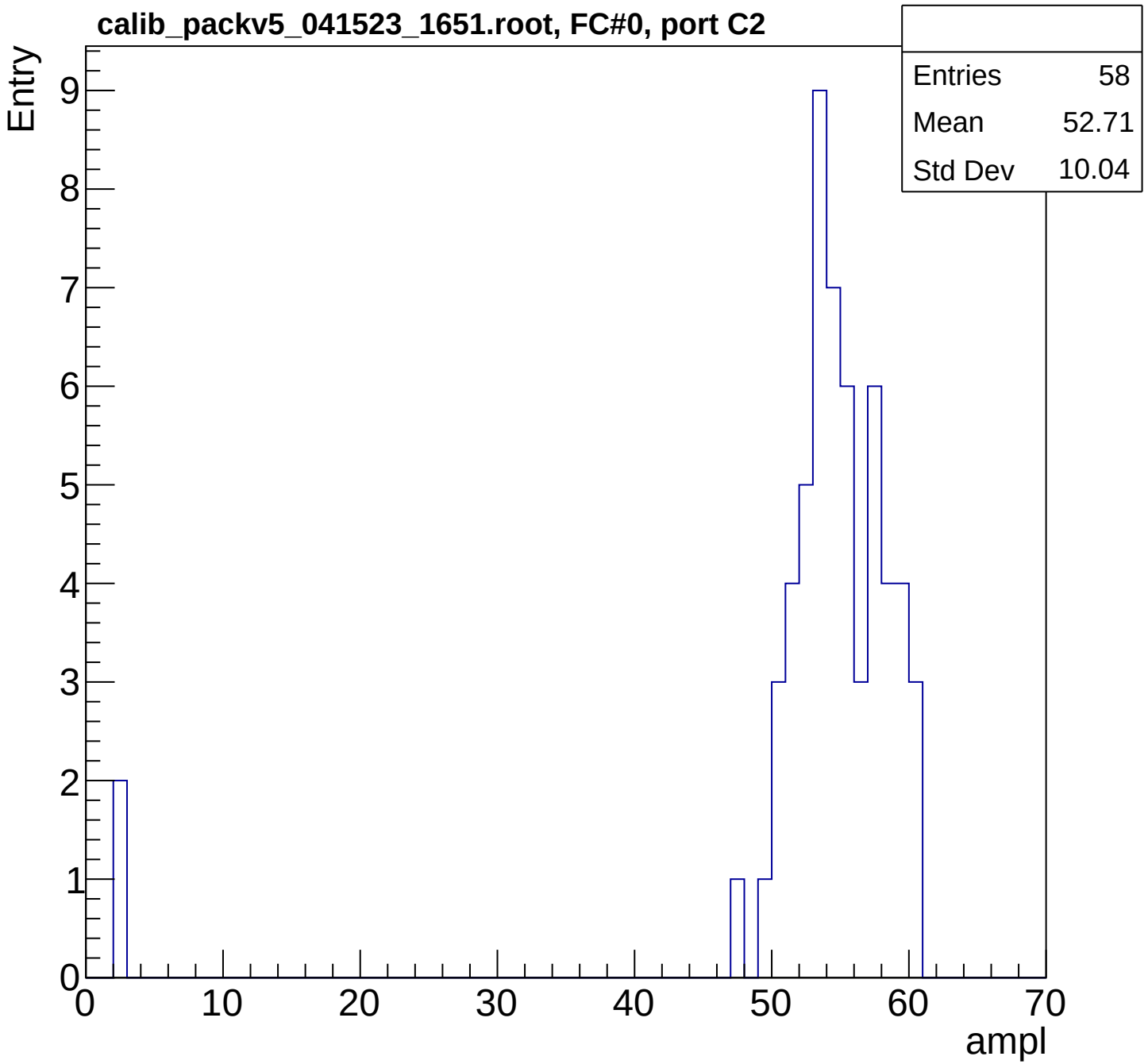
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch82, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 52.71
Std Dev 10.04
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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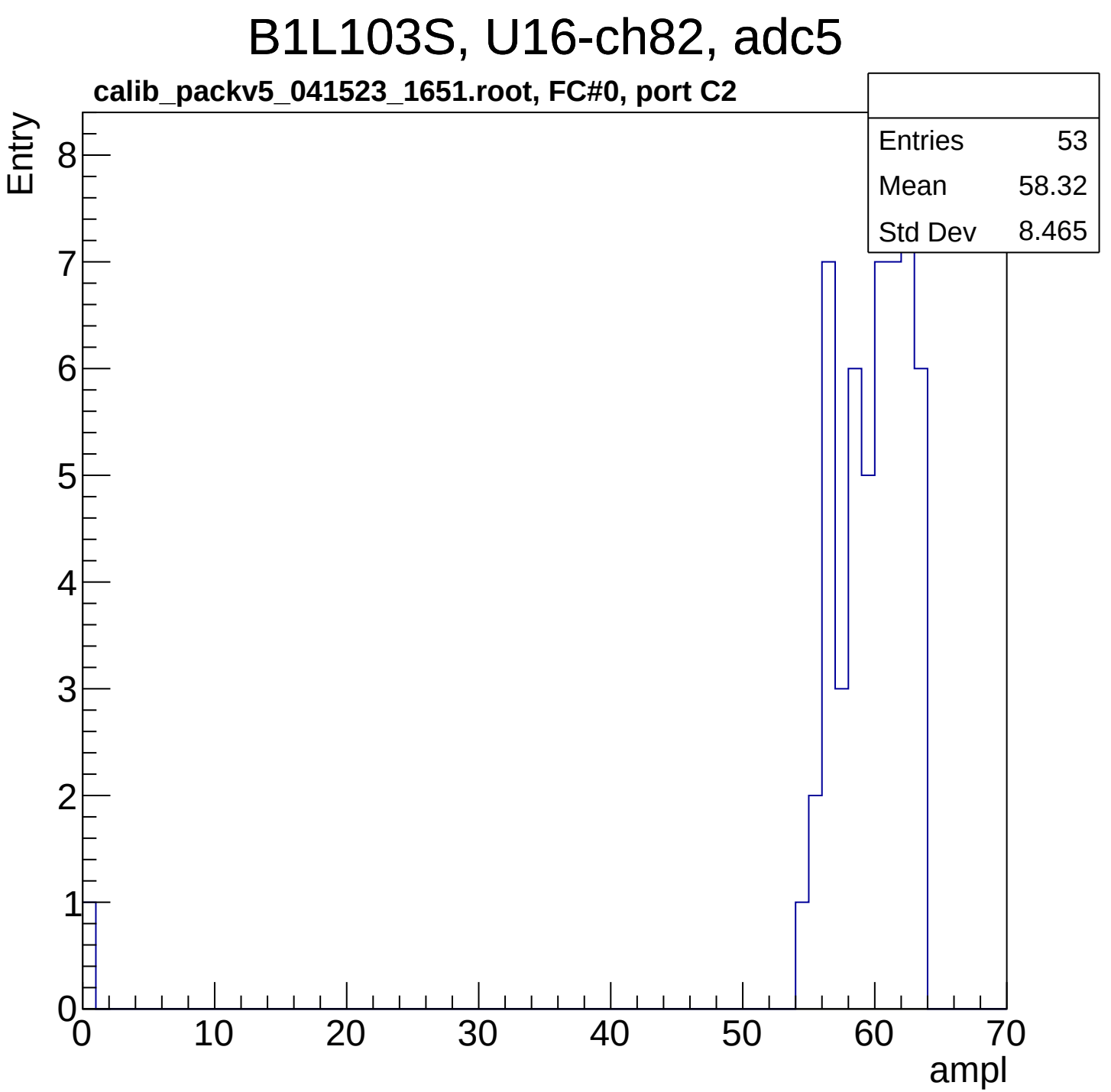
40
50
60
70


B1L103S, U16-ch82, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.32
Std Dev 8.465
Entry
ampl
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2
3
4
5
6
7
8
0
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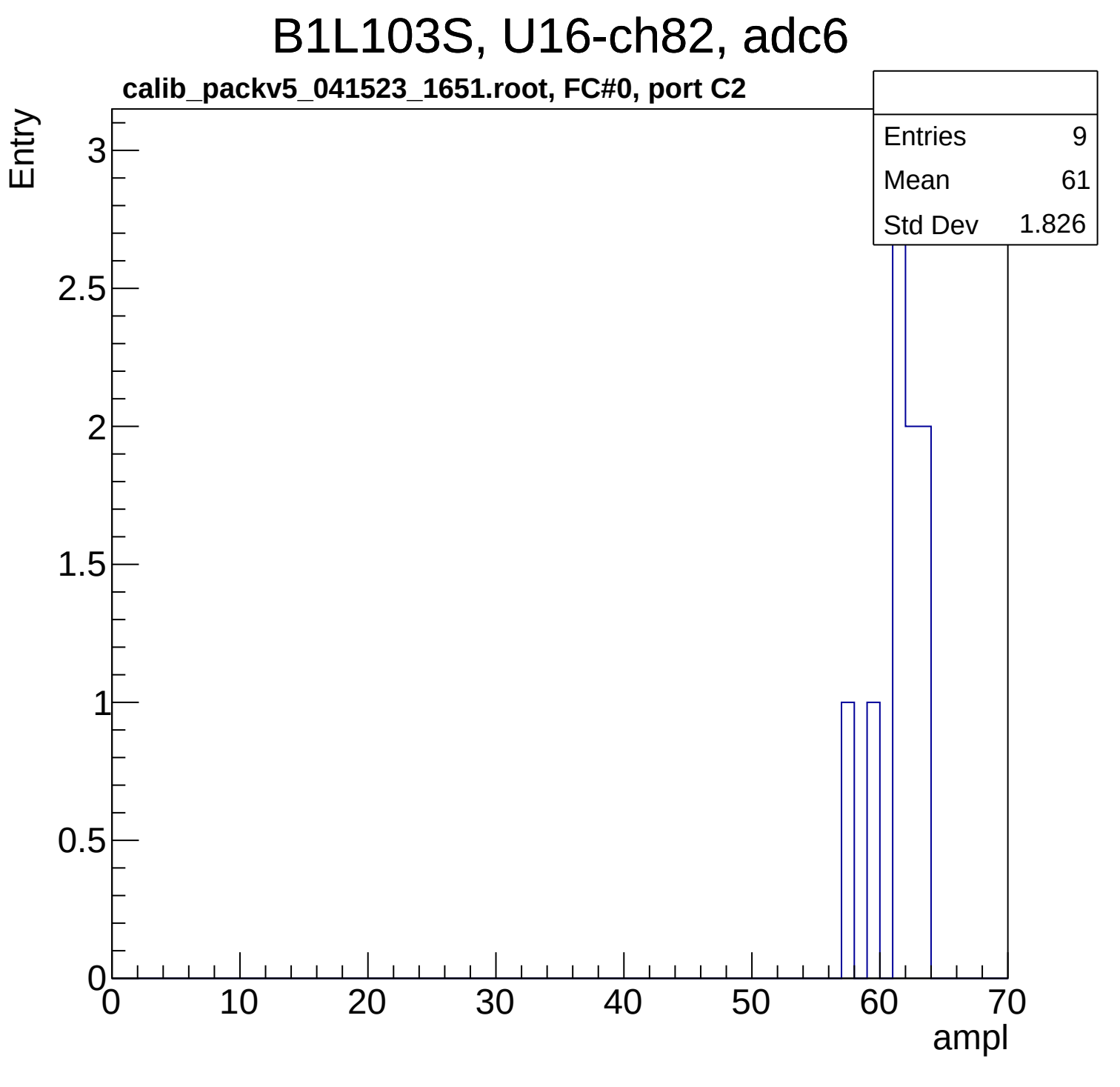
60
70


B1L103S, U16-ch82, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61
Std Dev 1.826
Entry
ampl
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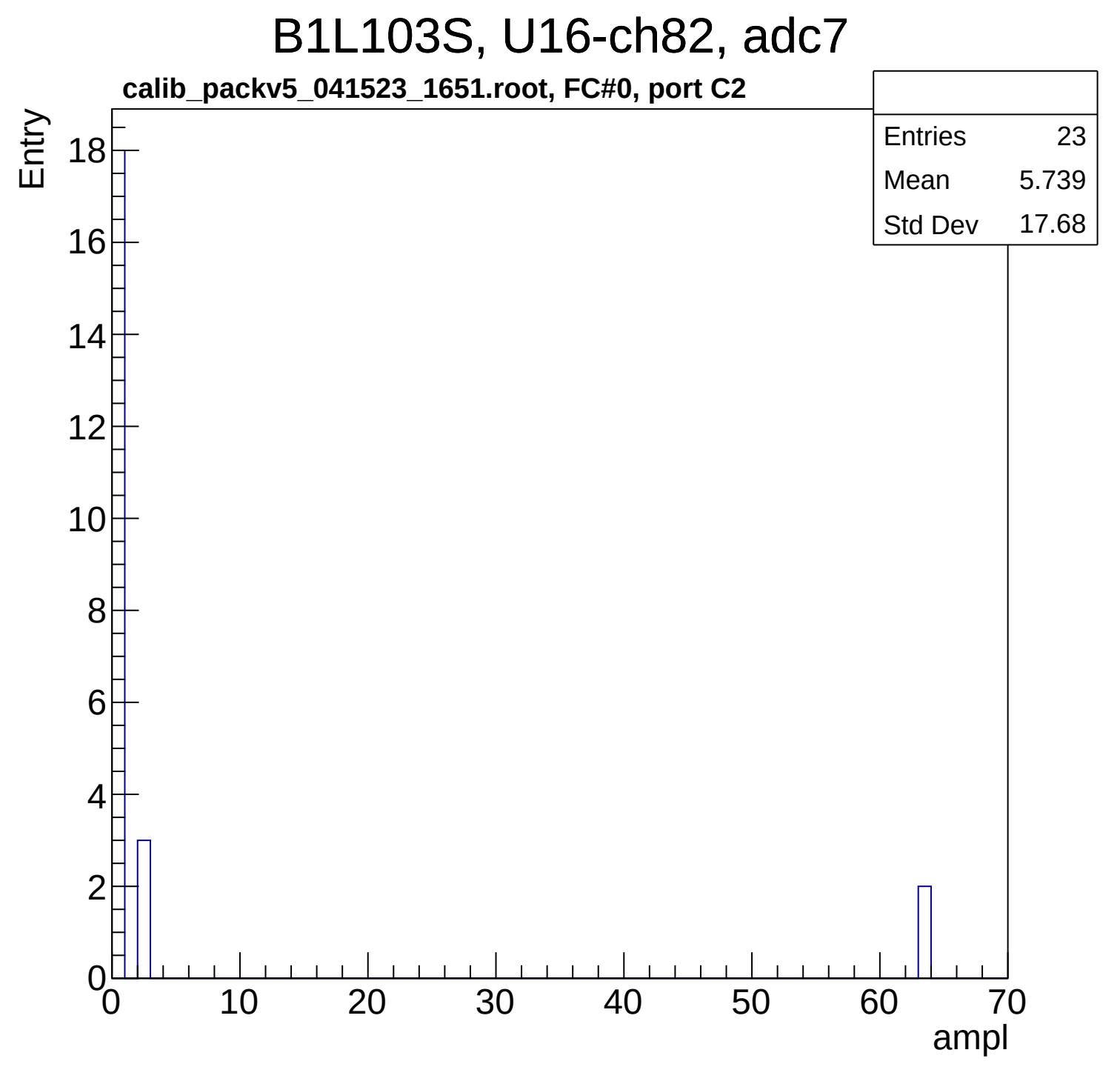
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U16-ch82, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 5.739
Std Dev 17.68
Entry
ampl
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4
6
8
10
12
14
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18
0
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60
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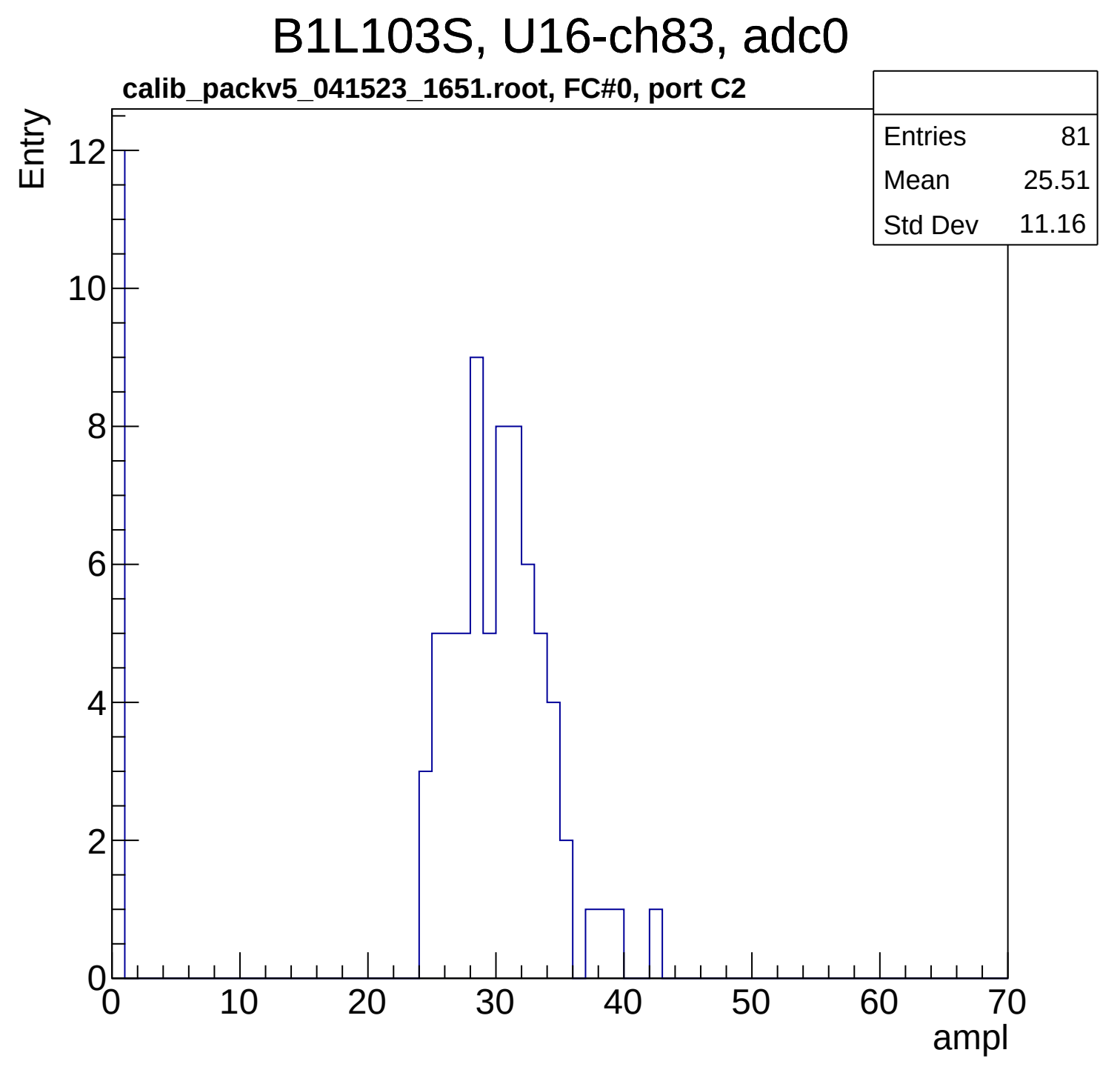
B1L103S, U16-ch83, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 25.51
Std Dev 11.16
Entry
ampl
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0
10
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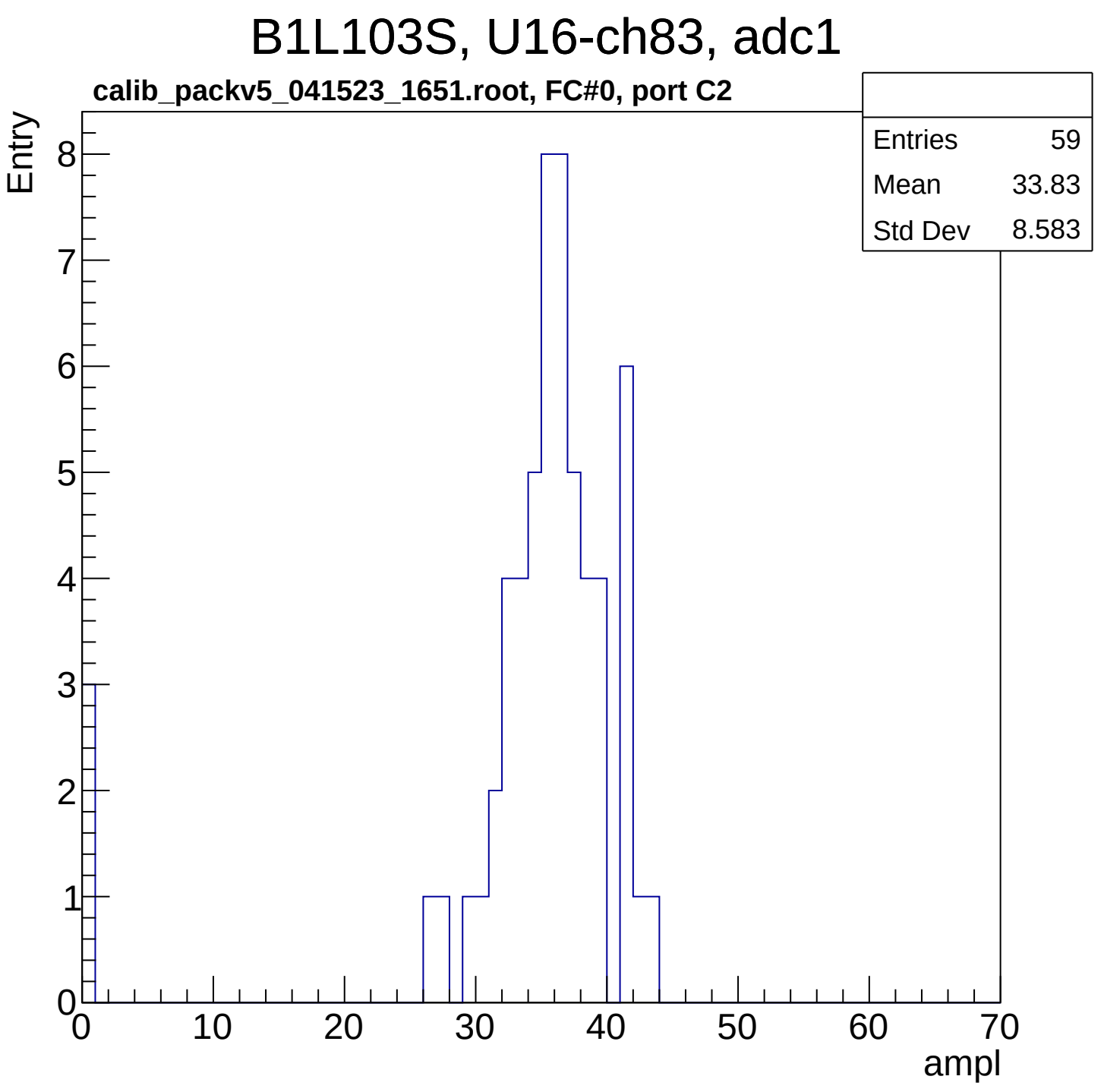
40
50
60
70


B1L103S, U16-ch83, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 33.83
Std Dev 8.583
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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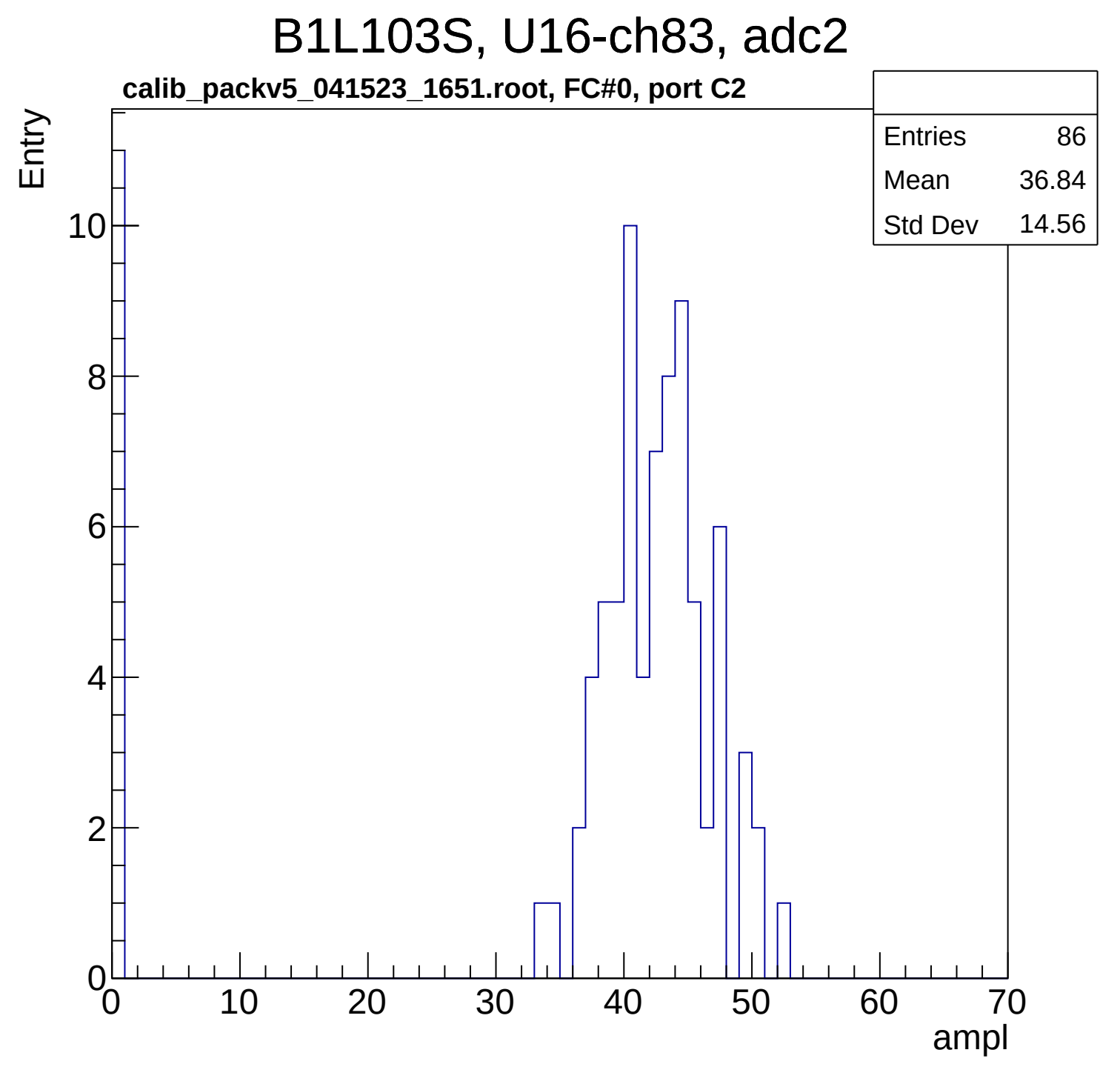
40
50
60
70


B1L103S, U16-ch83, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 36.84
Std Dev 14.56
Entry
0
2
4
6
8
10
0
10
20
30
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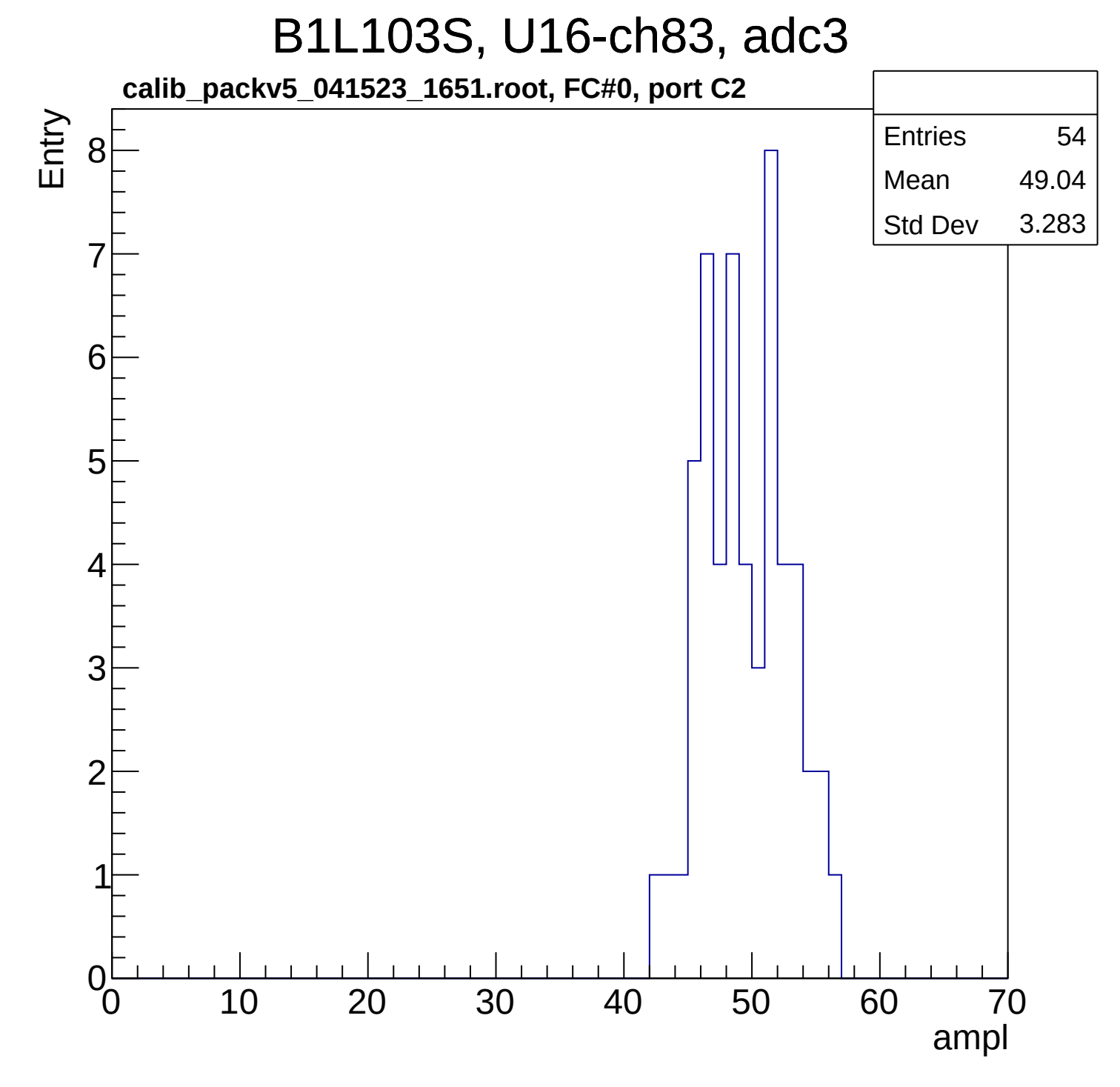
50
60
70
ampl


B1L103S, U16-ch83, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 49.04
Std Dev 3.283
Entry
ampl
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3
4
5
6
7
8
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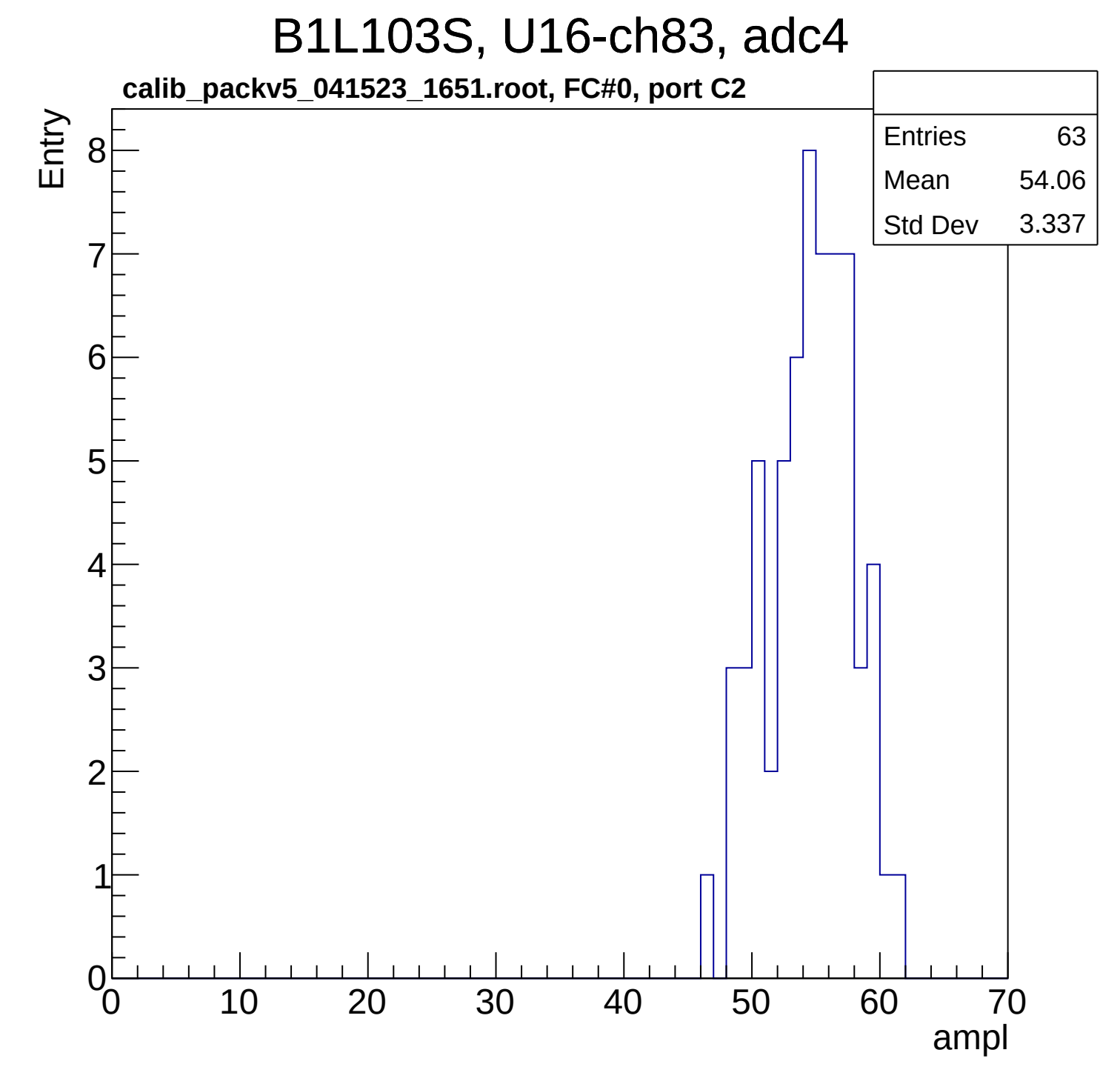
60
70


B1L103S, U16-ch83, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 54.06
Std Dev 3.337
Entry
ampl
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3
4
5
6
7
8
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10
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60
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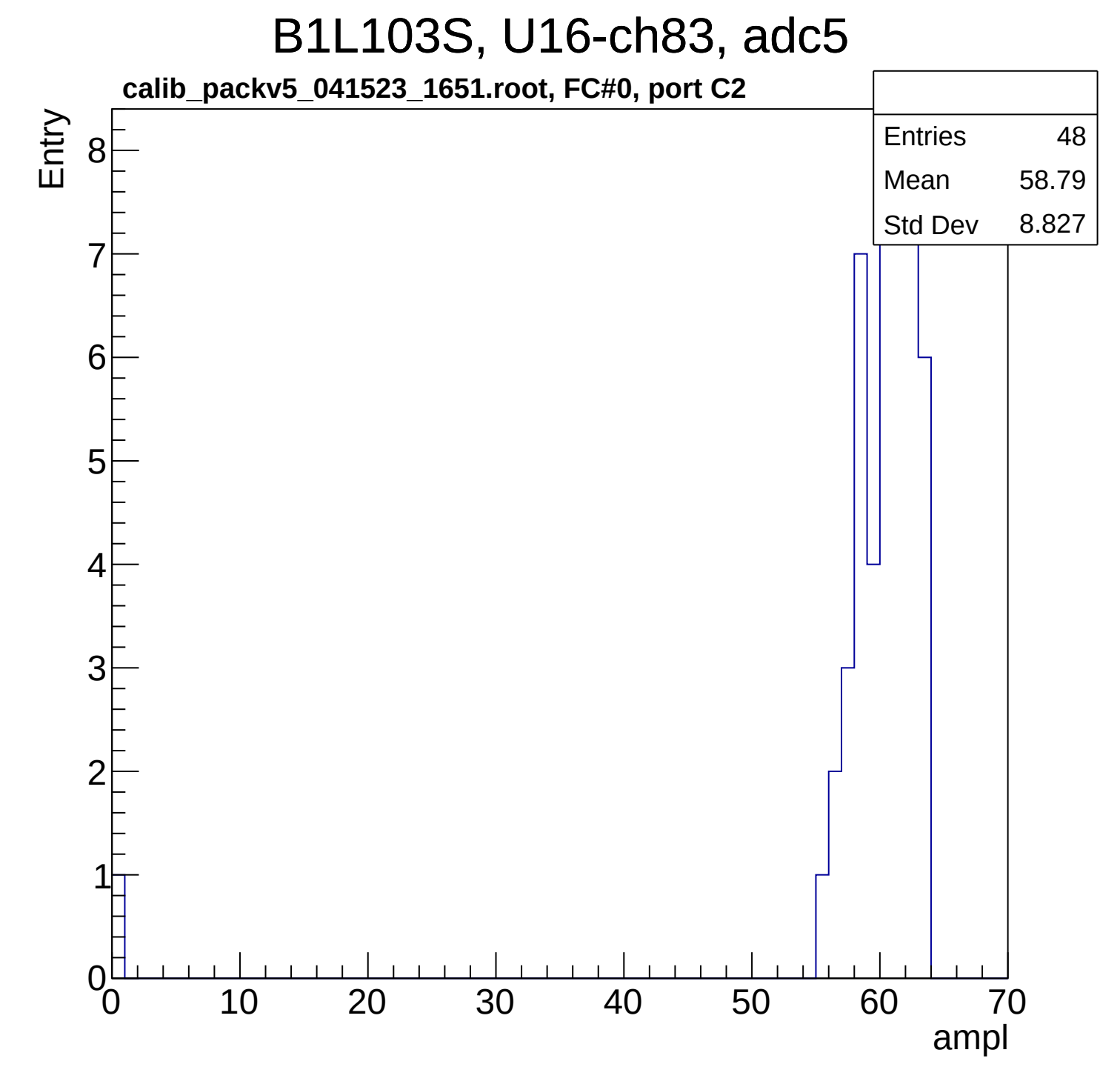
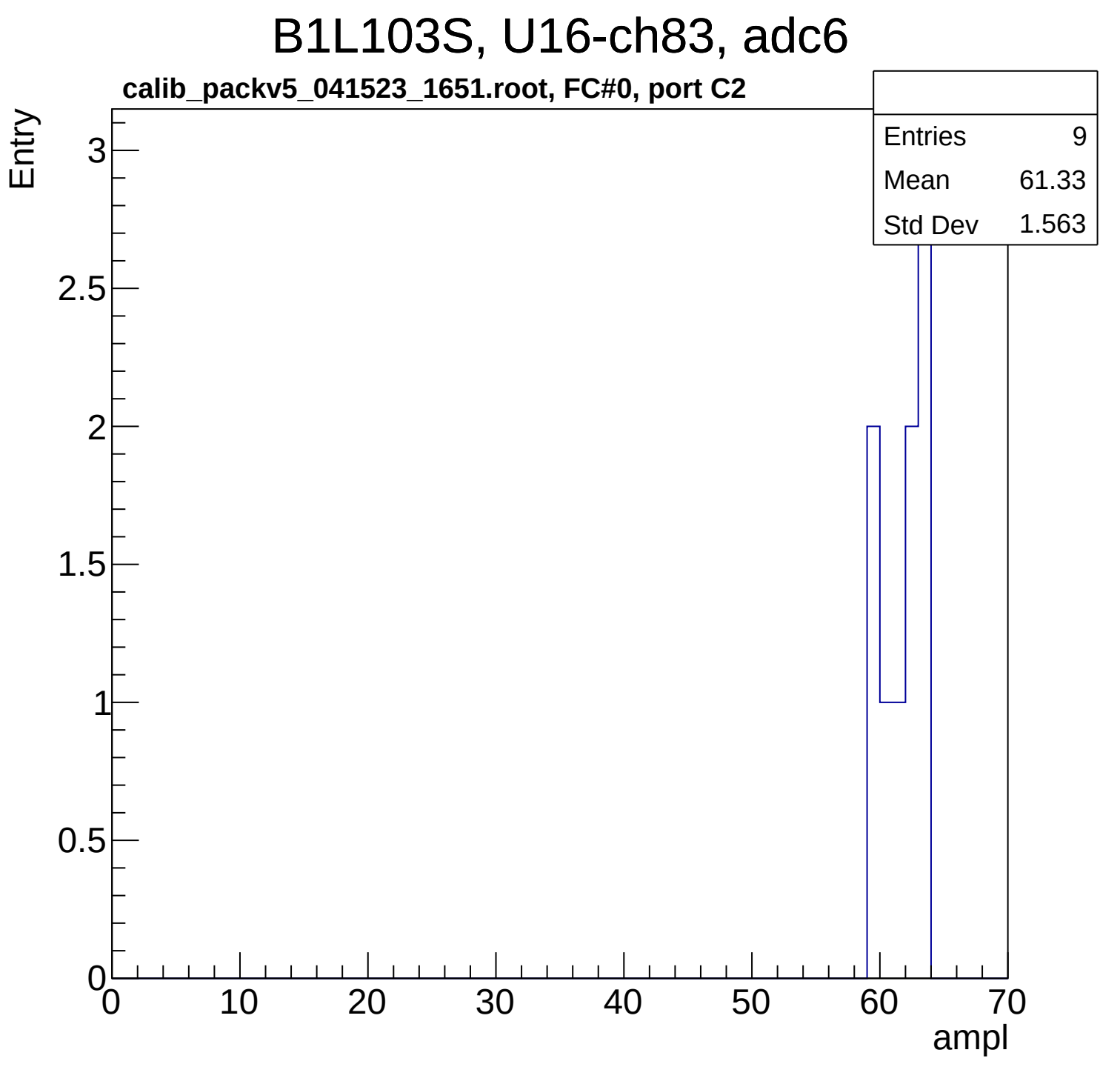

B1L103S, U16-ch83, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.79
Std Dev 8.827
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch83, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.33
Std Dev 1.563
Entry
ampl
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0.5
1
1.5
2
2.5
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0
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40
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60
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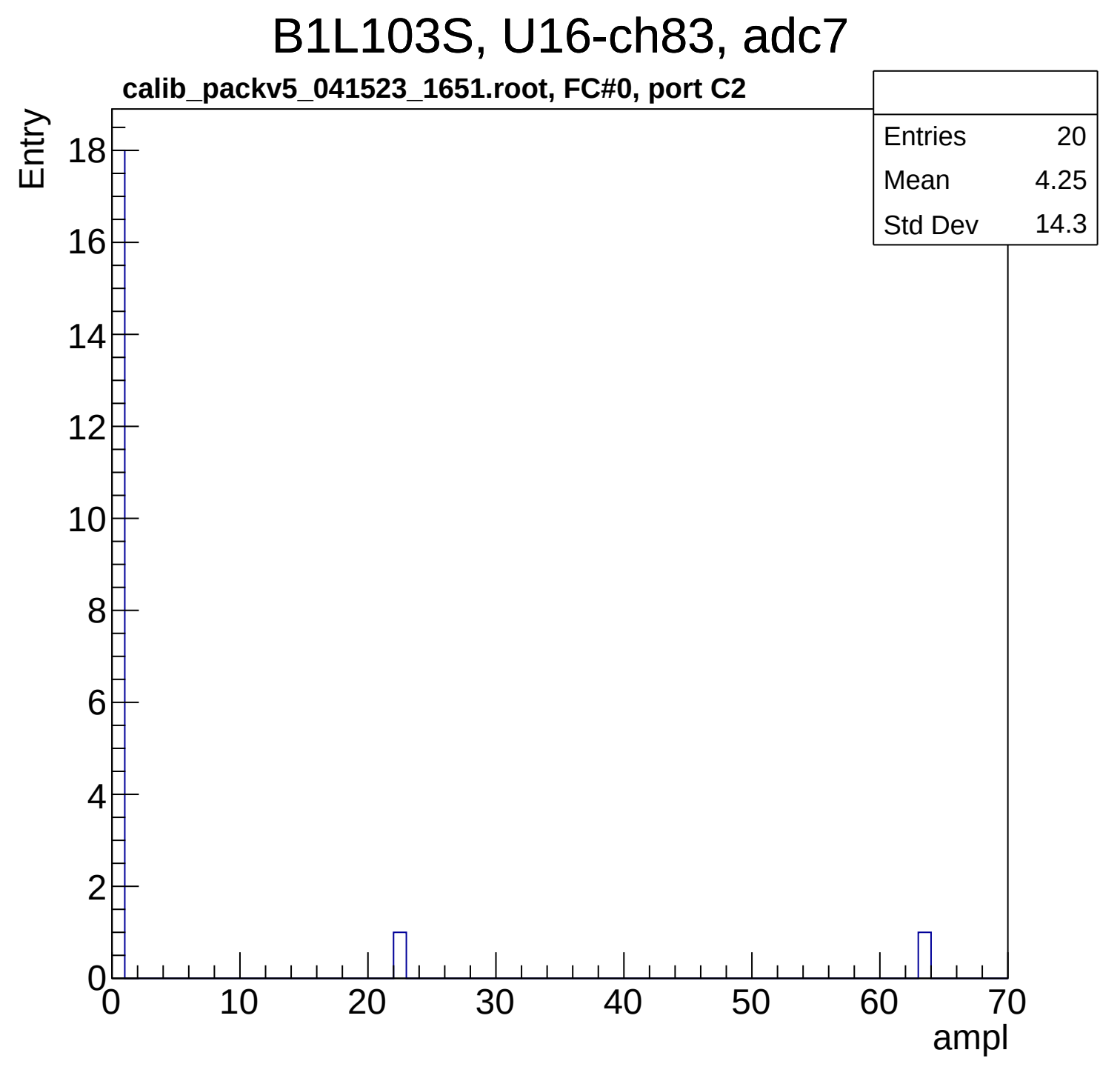
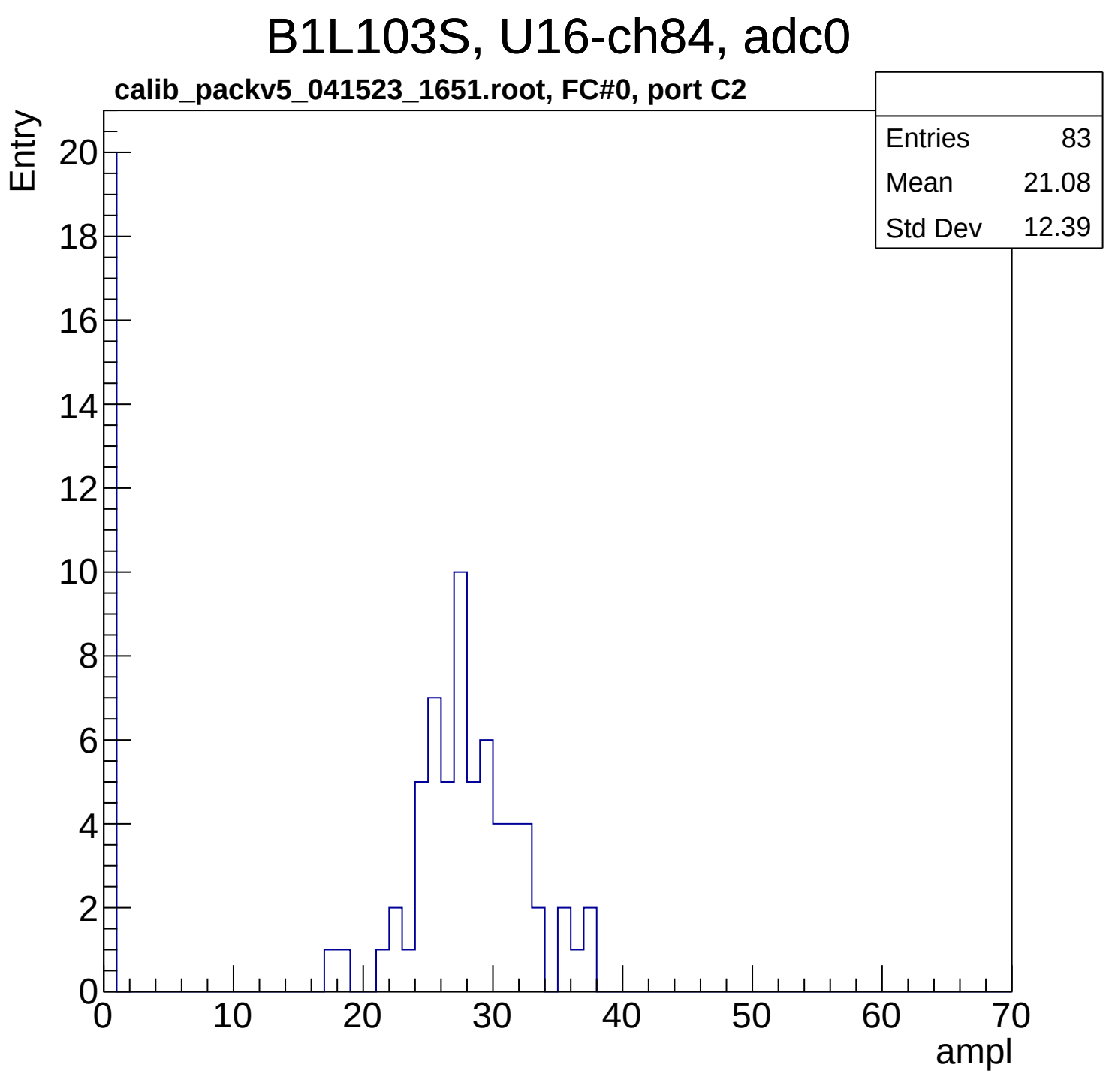
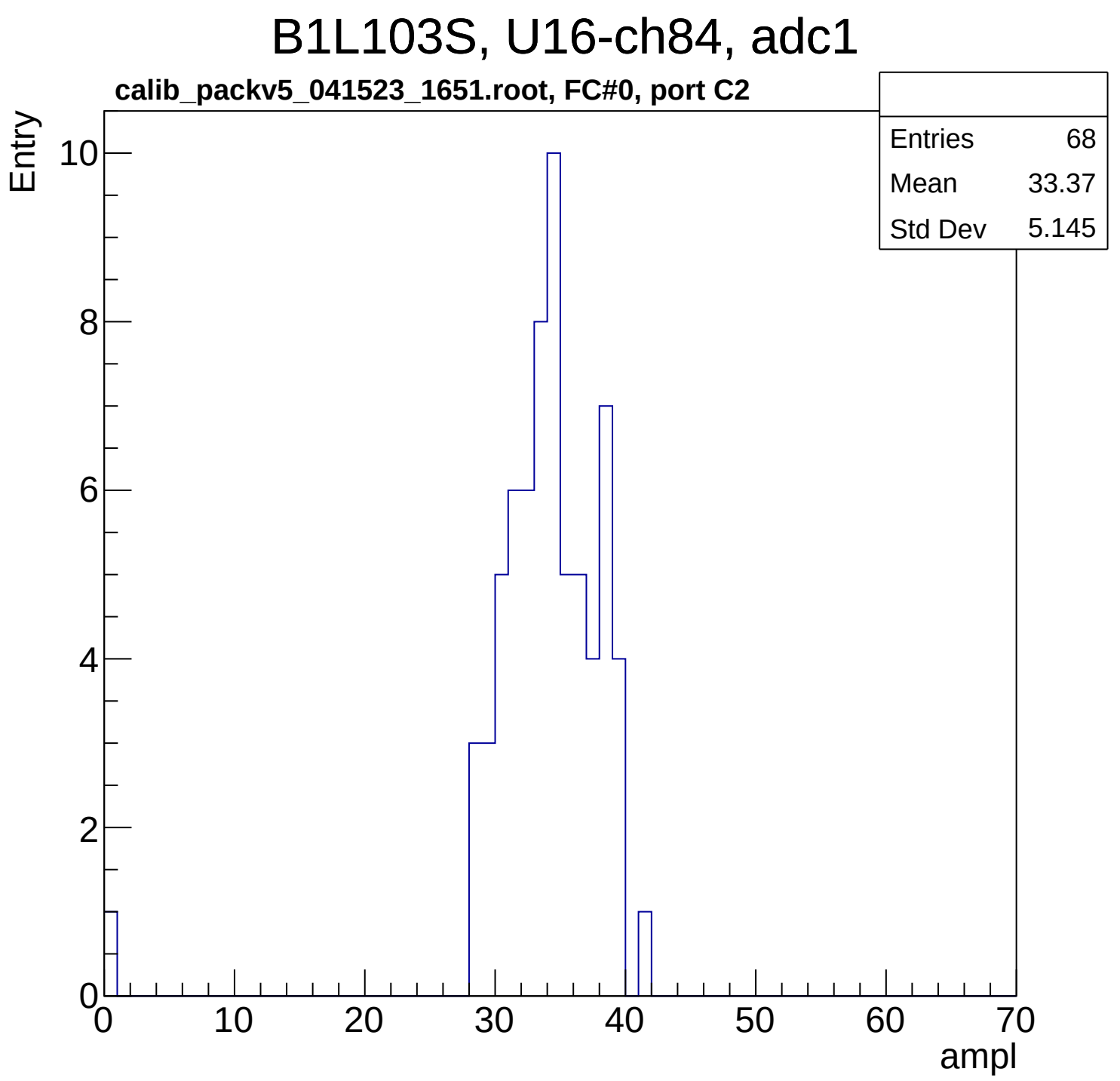
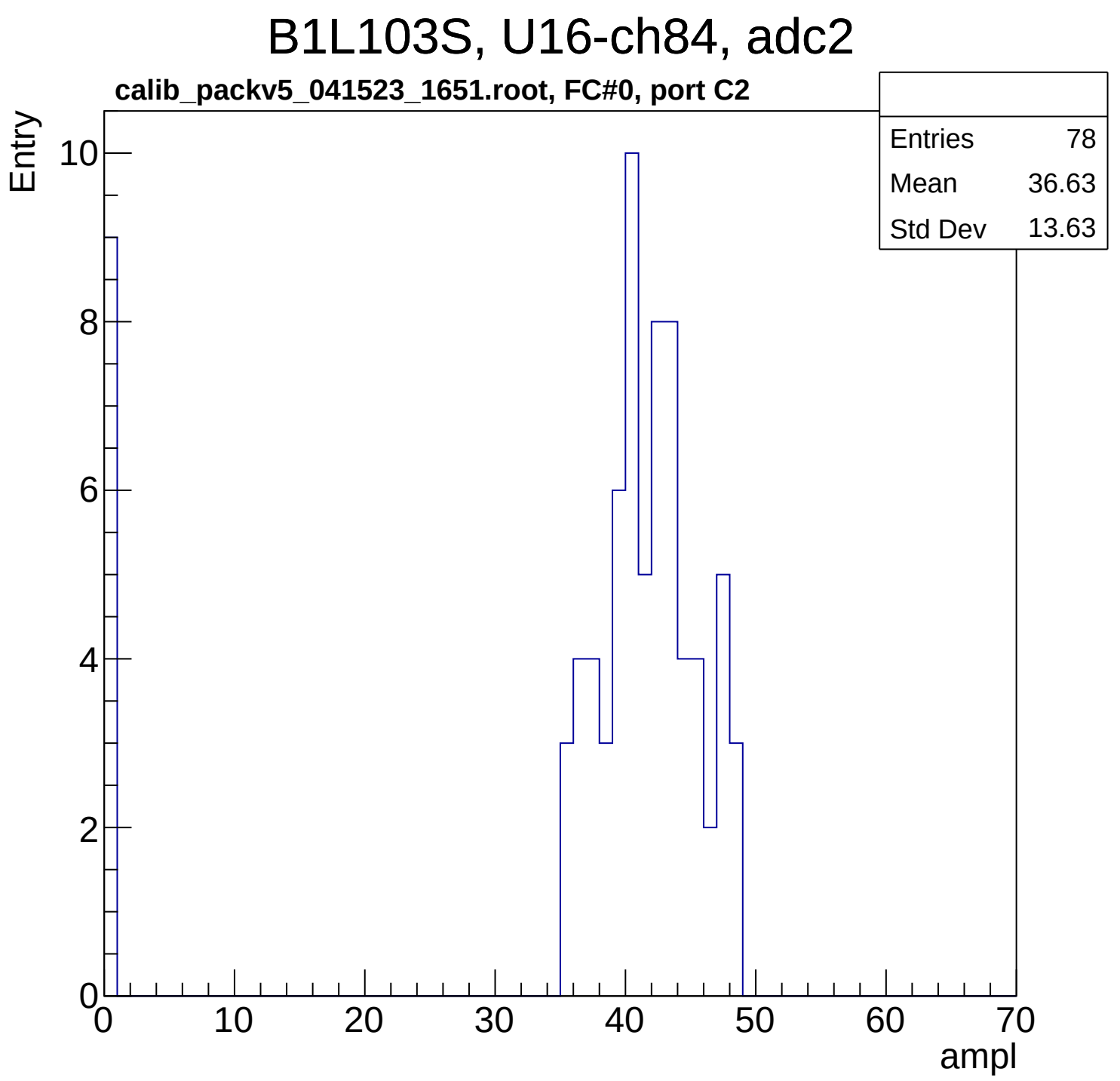
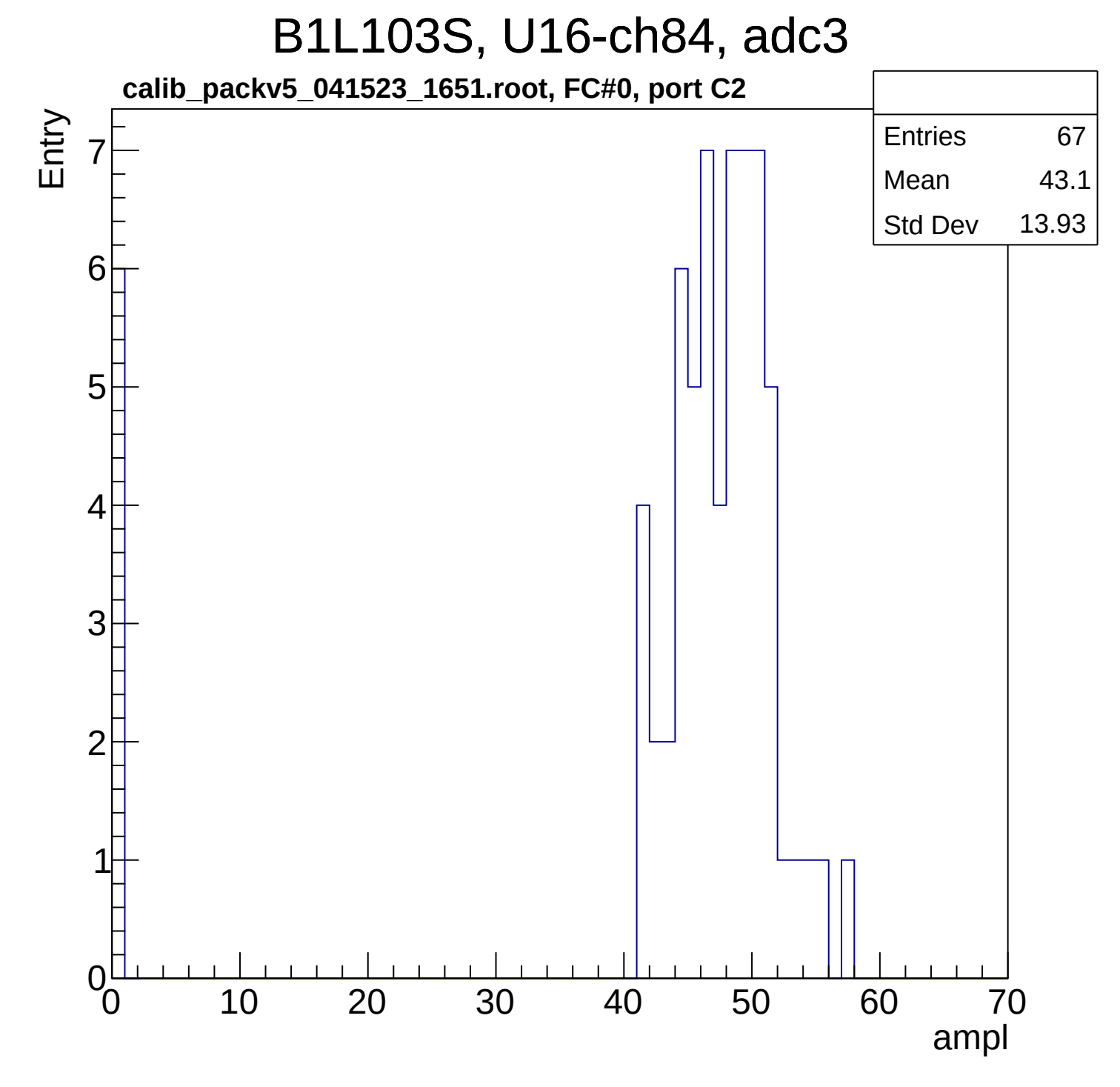
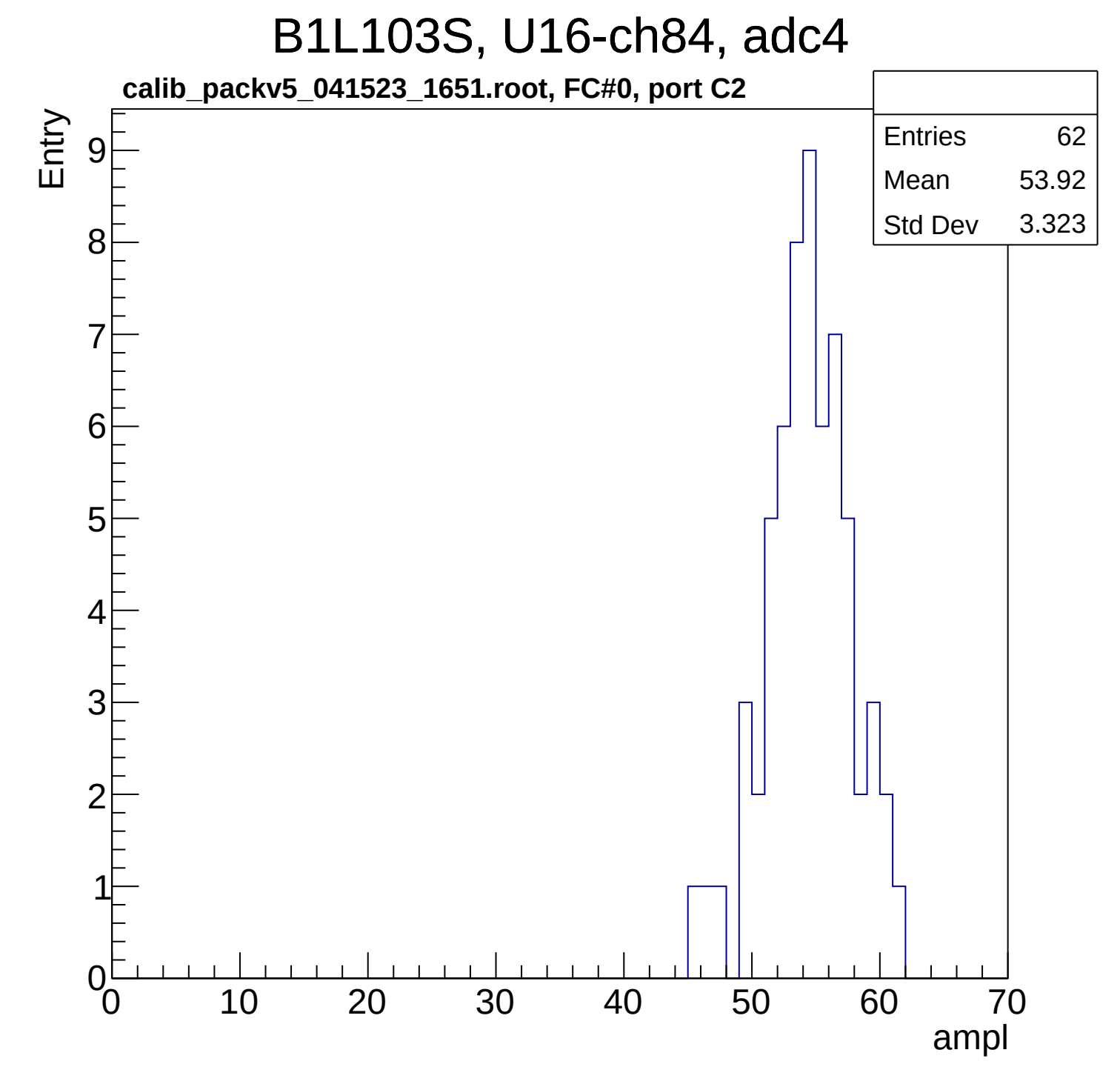

B1L103S, U16-ch83, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.25
Std Dev 14.3
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch84, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 21.08
Std Dev 12.39
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch84, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 33.37
Std Dev 5.145
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch84, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 36.63
Std Dev 13.63
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch84, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 43.1
Std Dev 13.93
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch84, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 53.92
Std Dev 3.323
Entry
ampl
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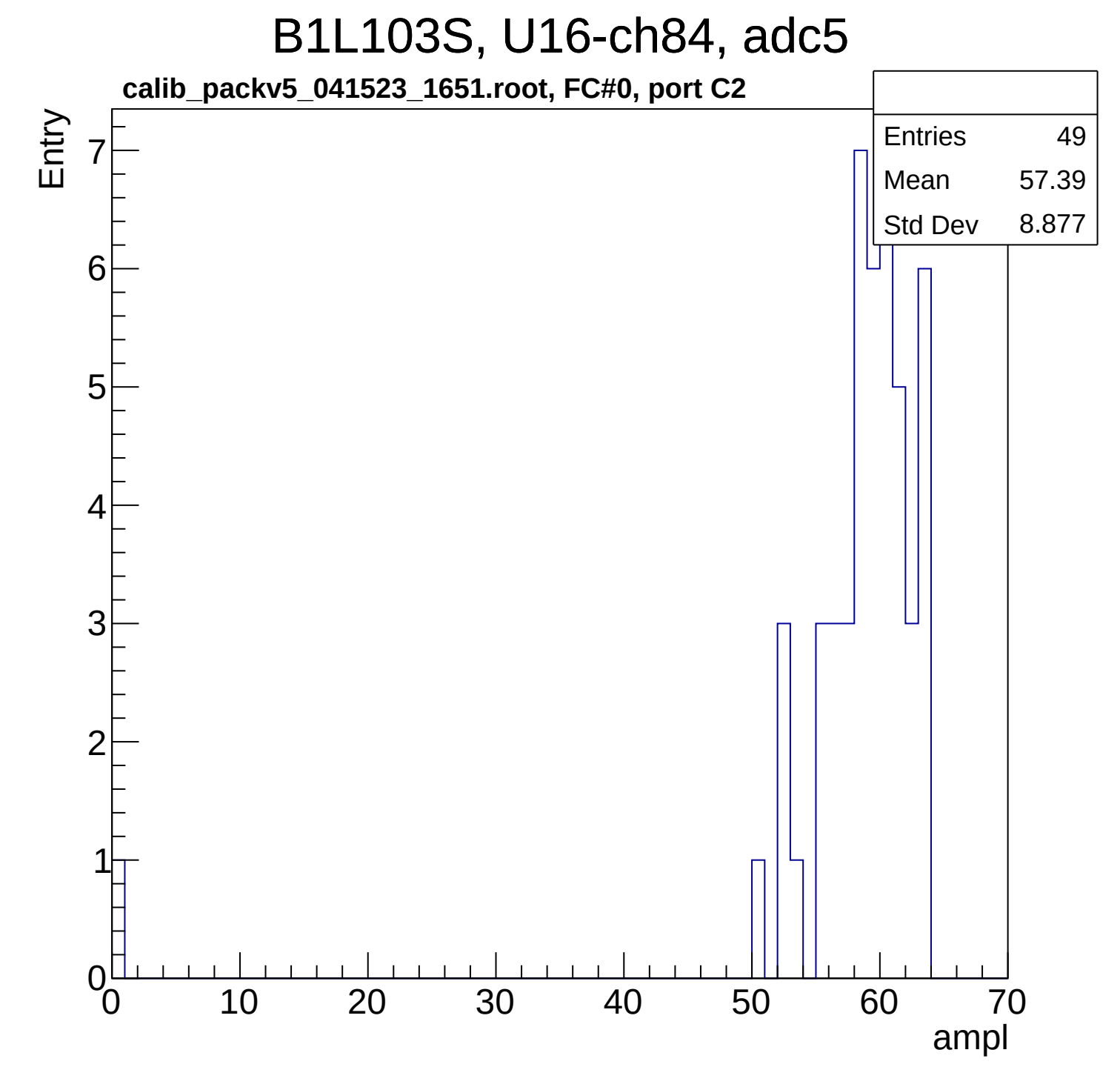
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch84, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 57.39
Std Dev 8.877
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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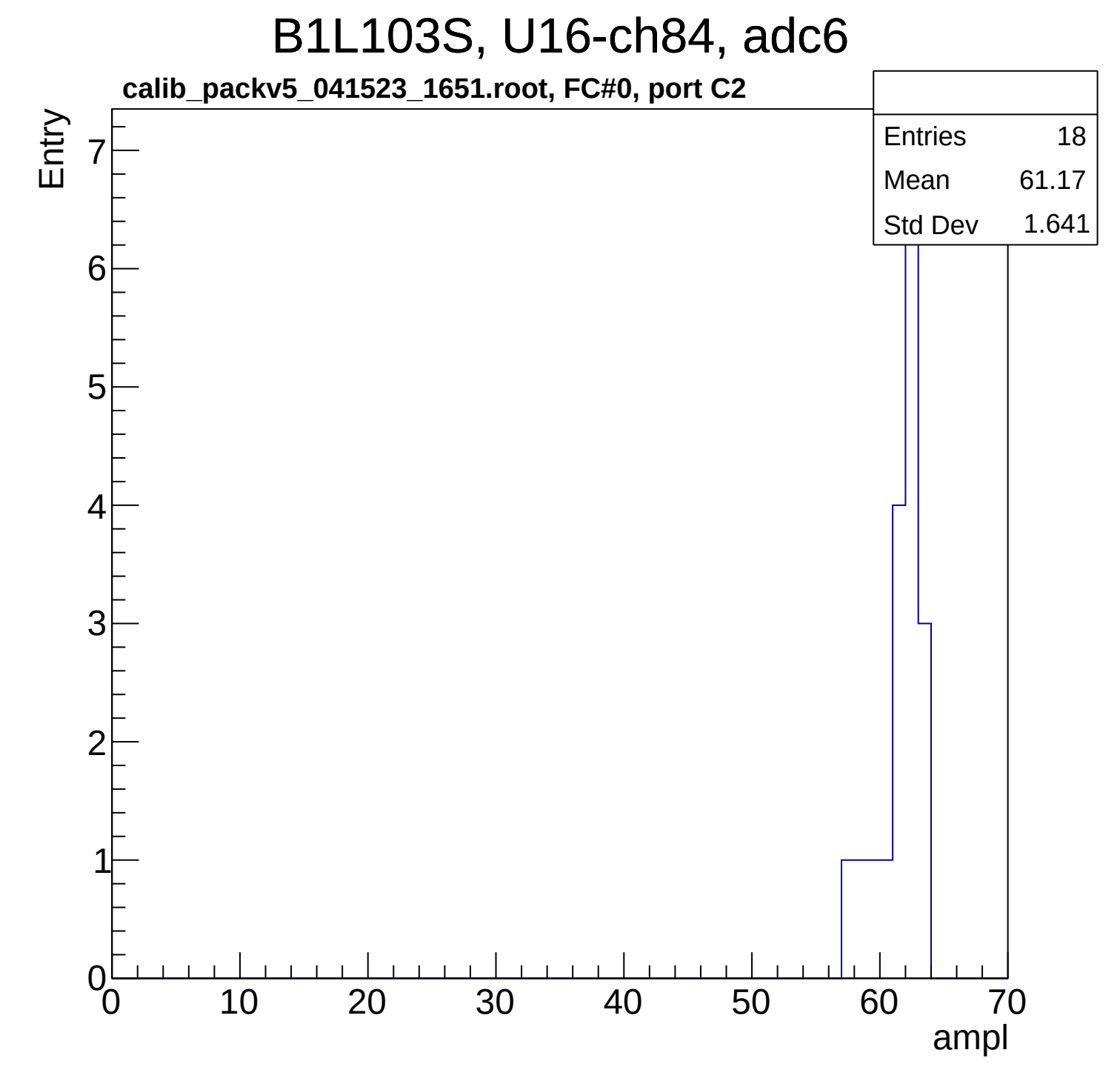
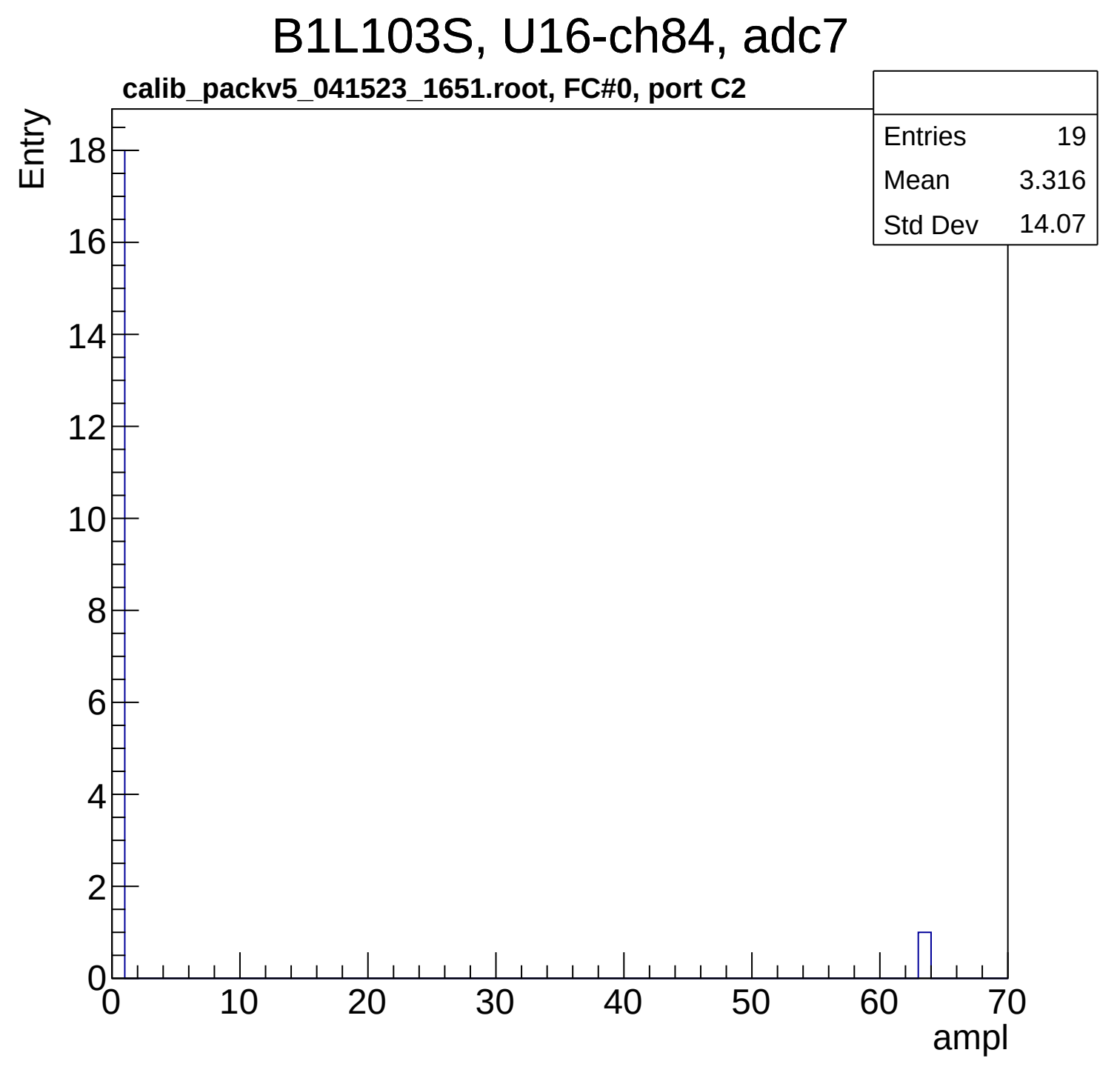

B1L103S, U16-ch84, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 61.17
Std Dev 1.641
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch84, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
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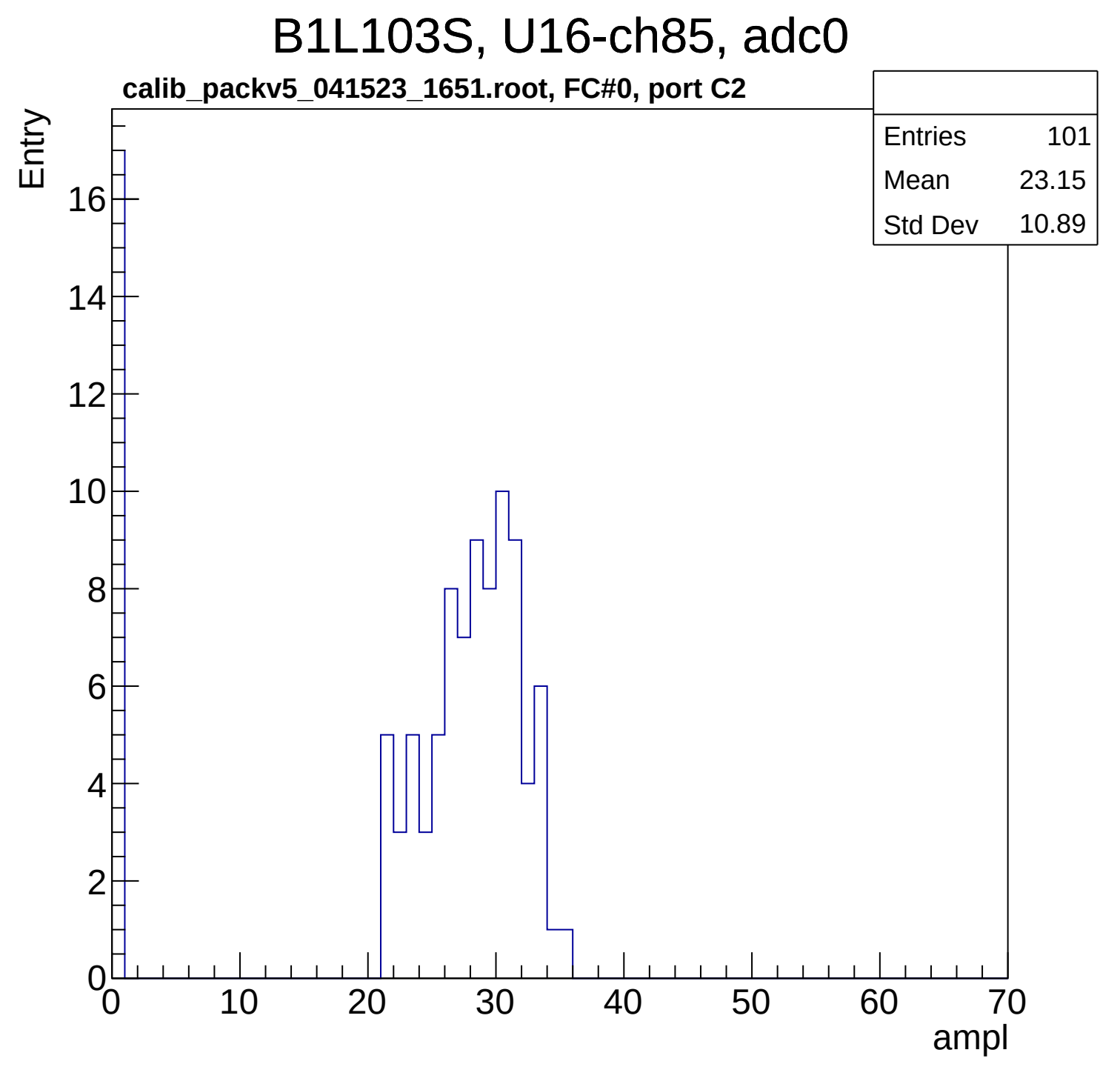
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch85, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 23.15
Std Dev 10.89
Entry
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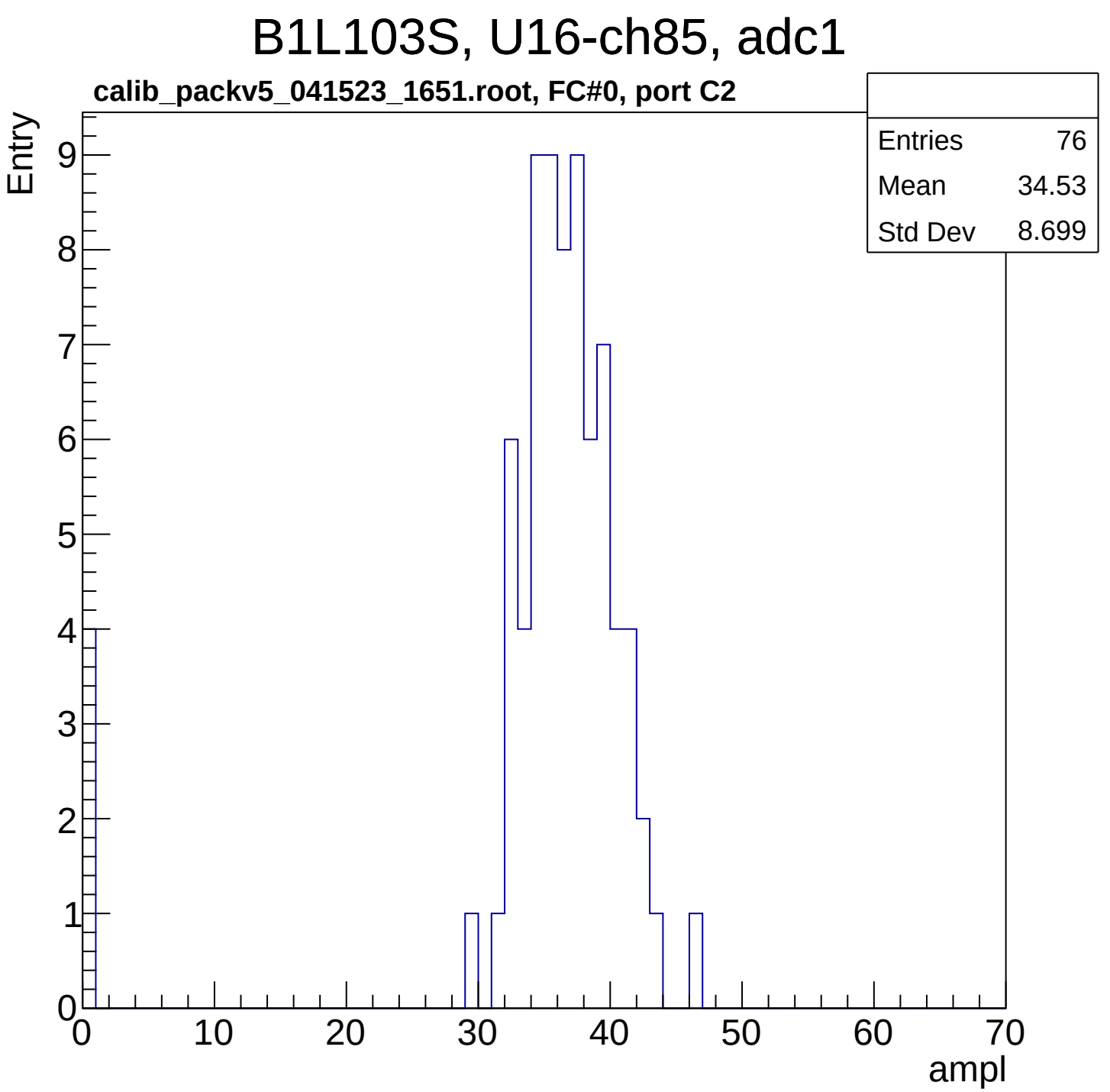
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch85, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 34.53
Std Dev 8.699
Entry
ampl
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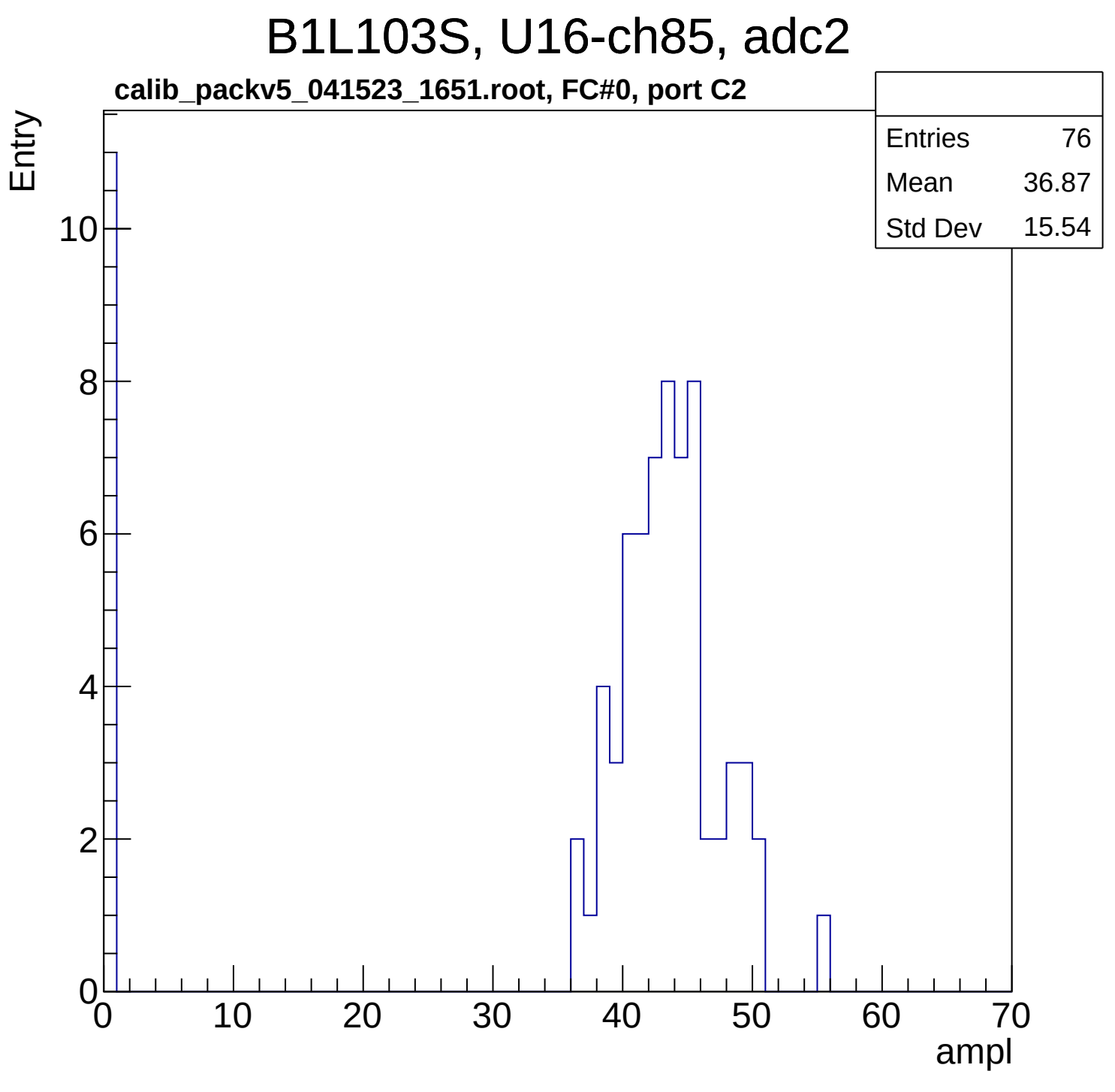
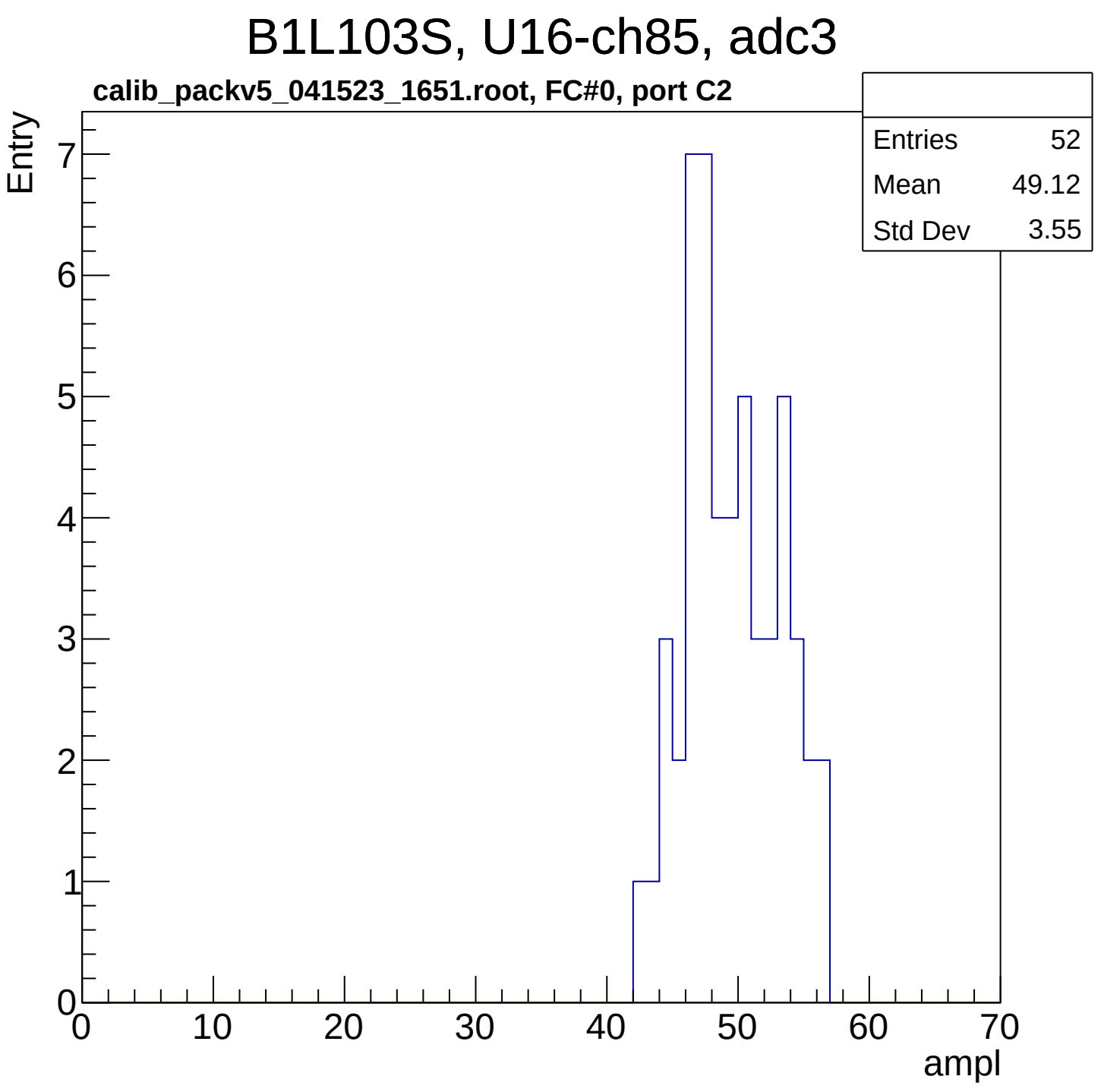
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch85, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 36.87
Std Dev 15.54
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch85, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 49.12
Std Dev 3.55
Entry
ampl
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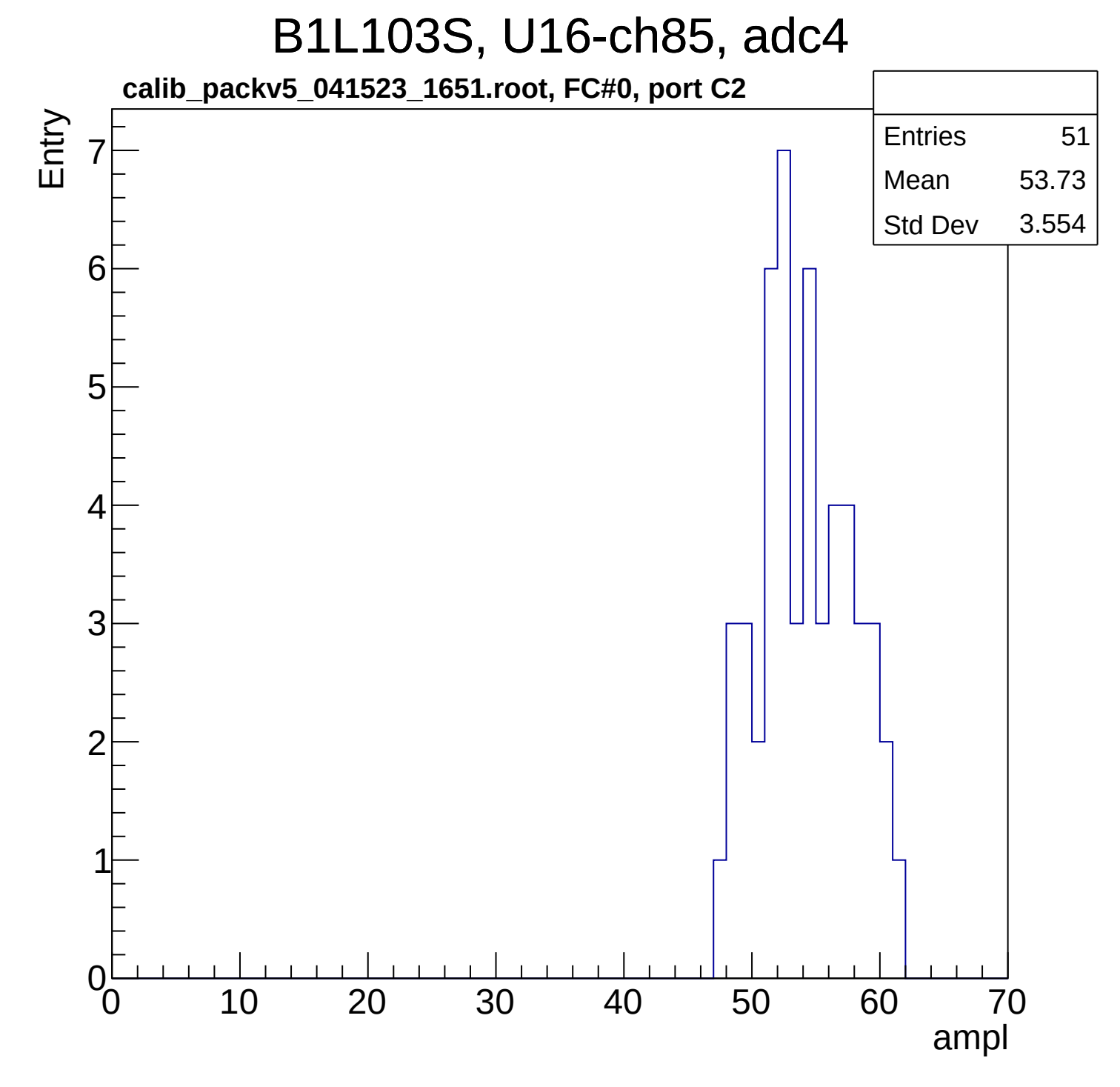
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch85, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 53.73
Std Dev 3.554
Entry
ampl
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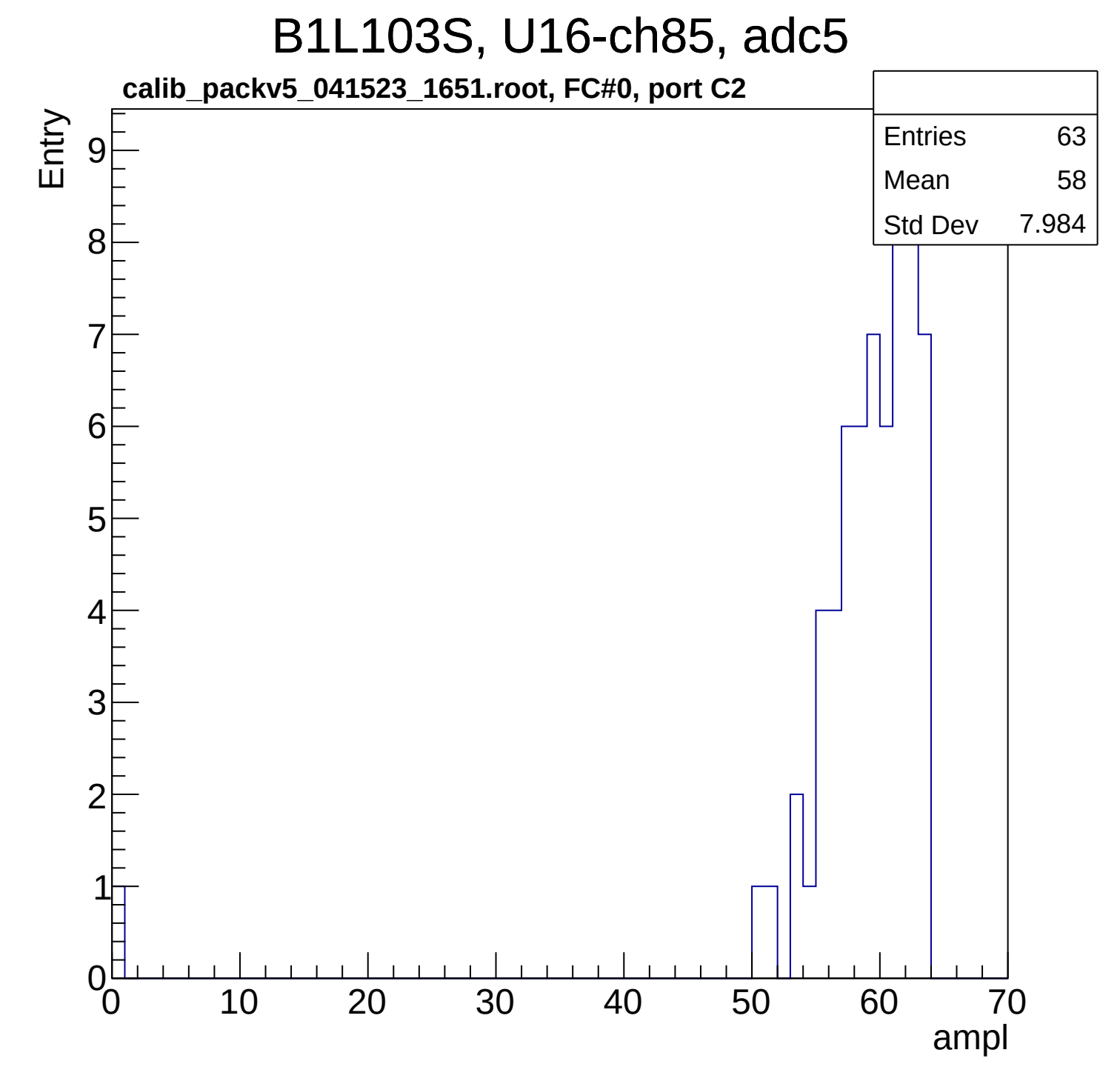
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch85, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 58
Std Dev 7.984
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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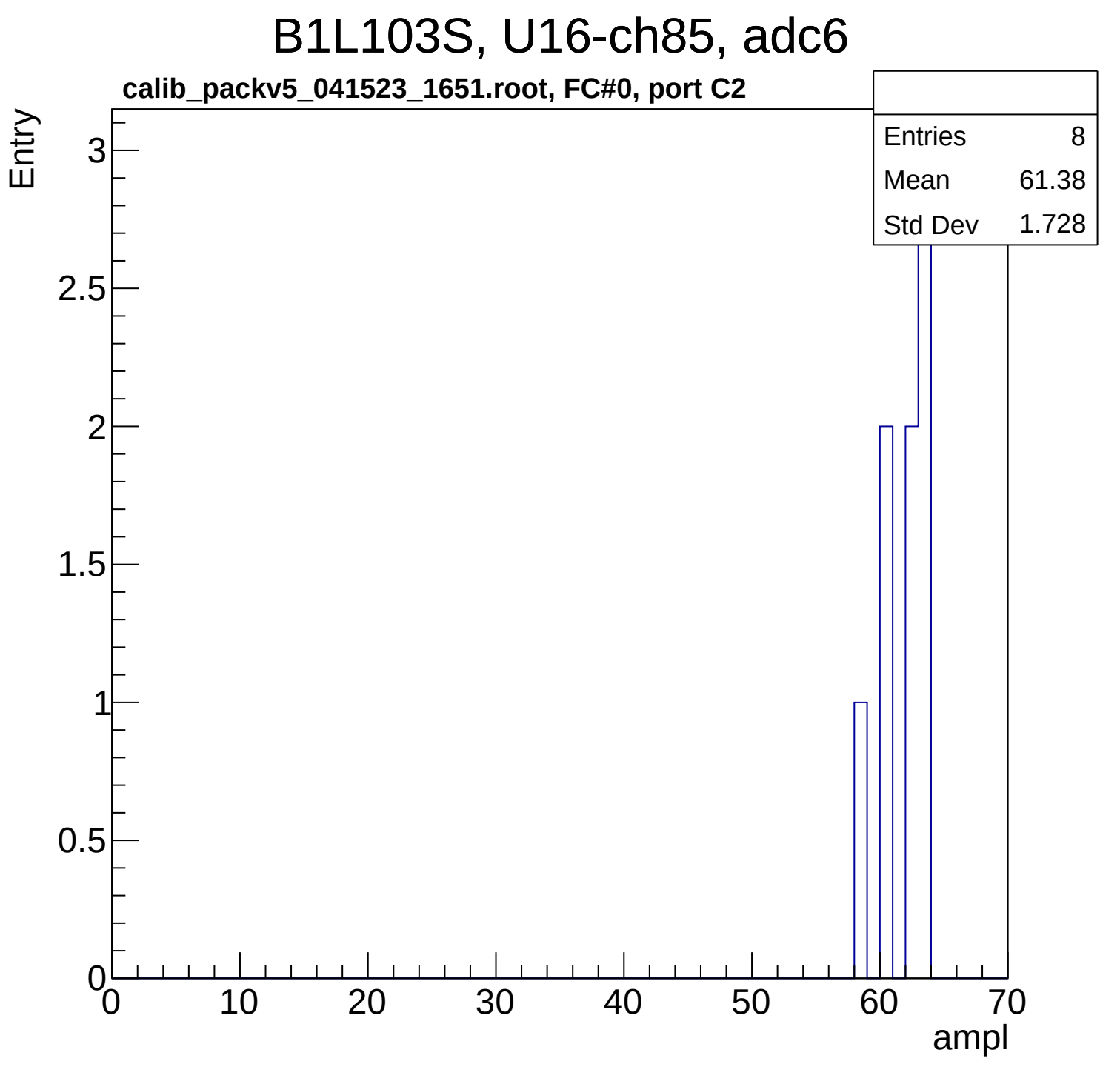
B1L103S, U16-ch85, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.38
Std Dev 1.728
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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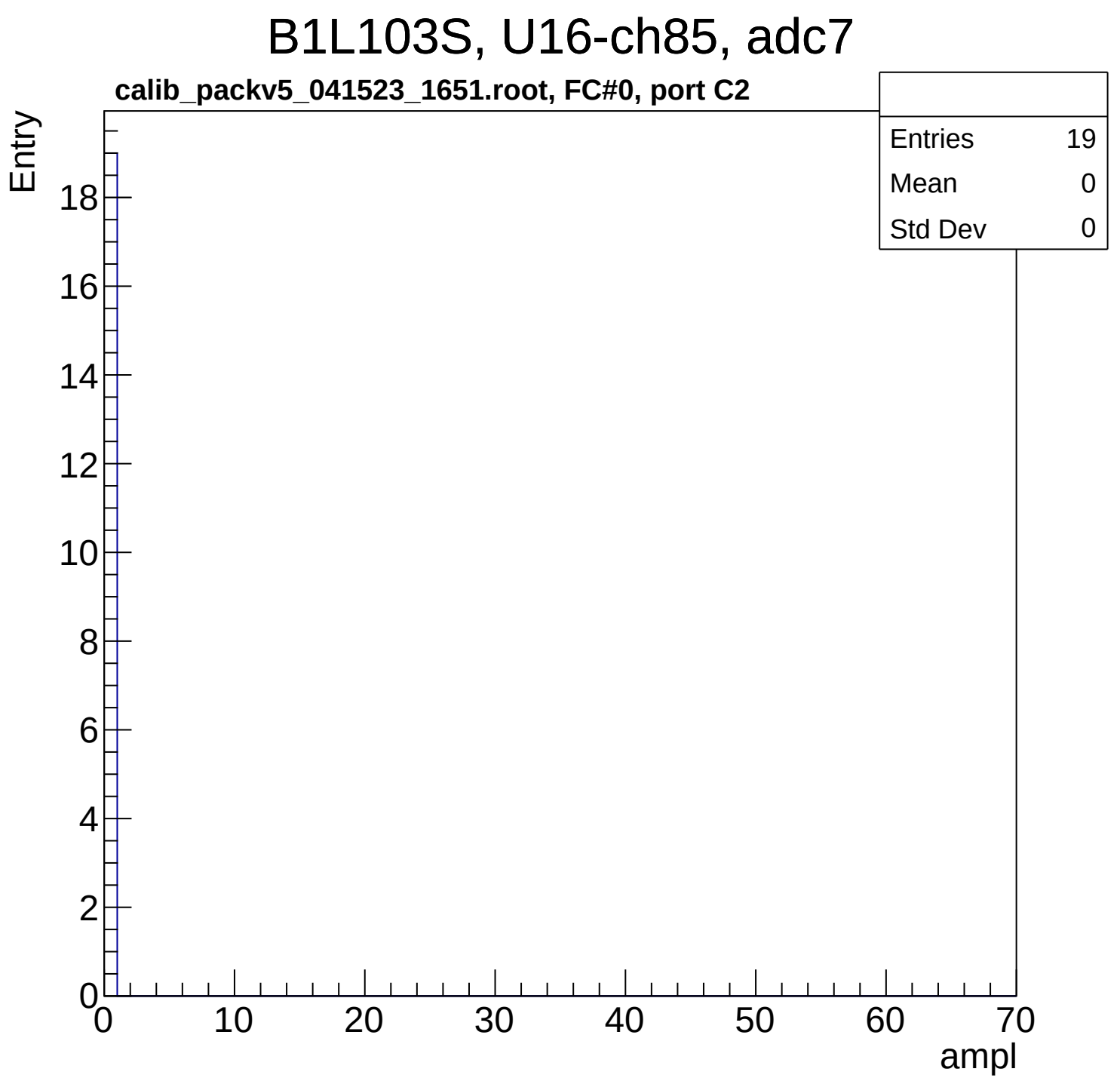
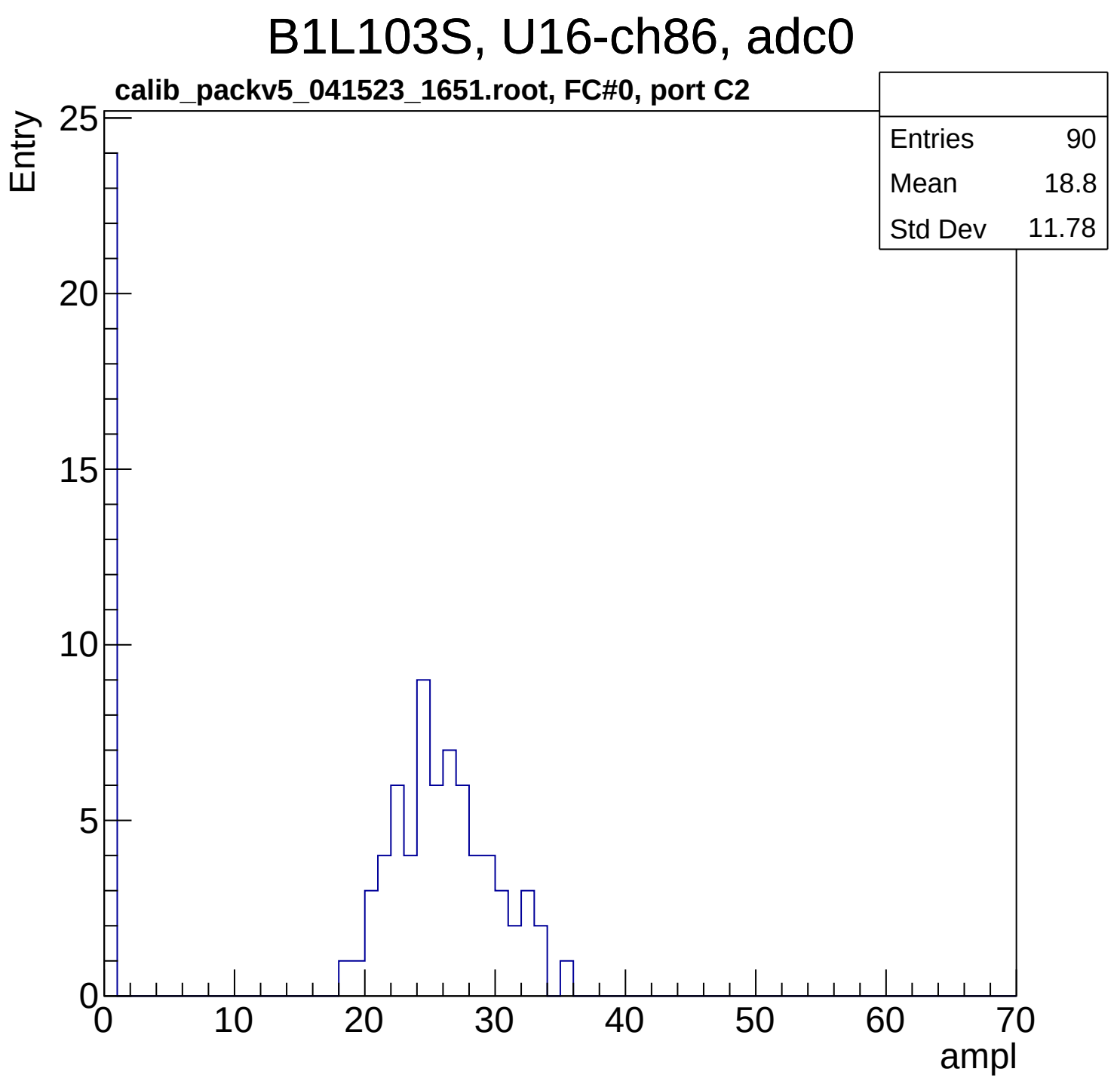
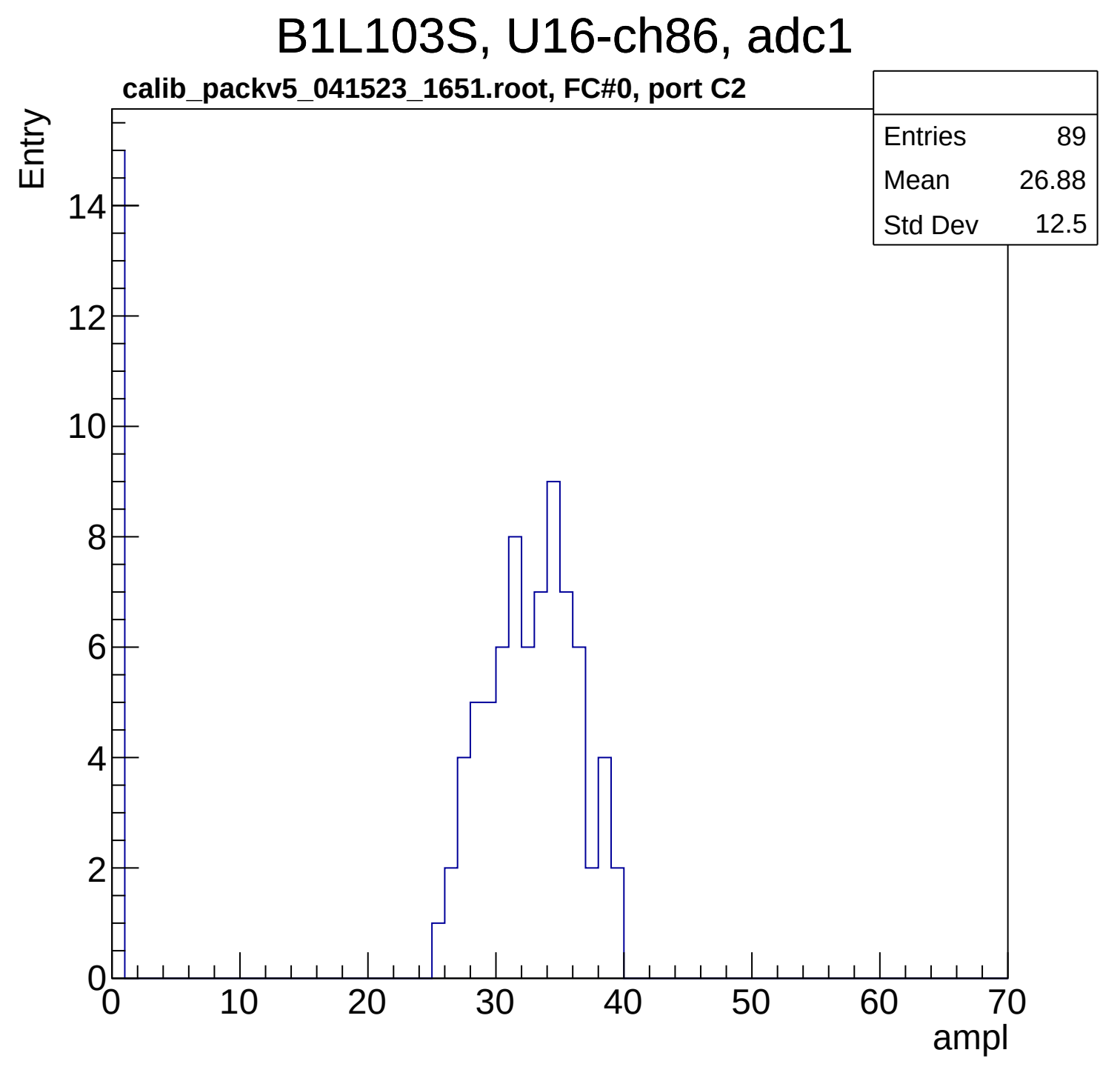

B1L103S, U16-ch85, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch86, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 18.8
Std Dev 11.78
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U16-ch86, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 26.88
Std Dev 12.5
Entry
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2
4
6
8
10
12
14
0
10
20
30
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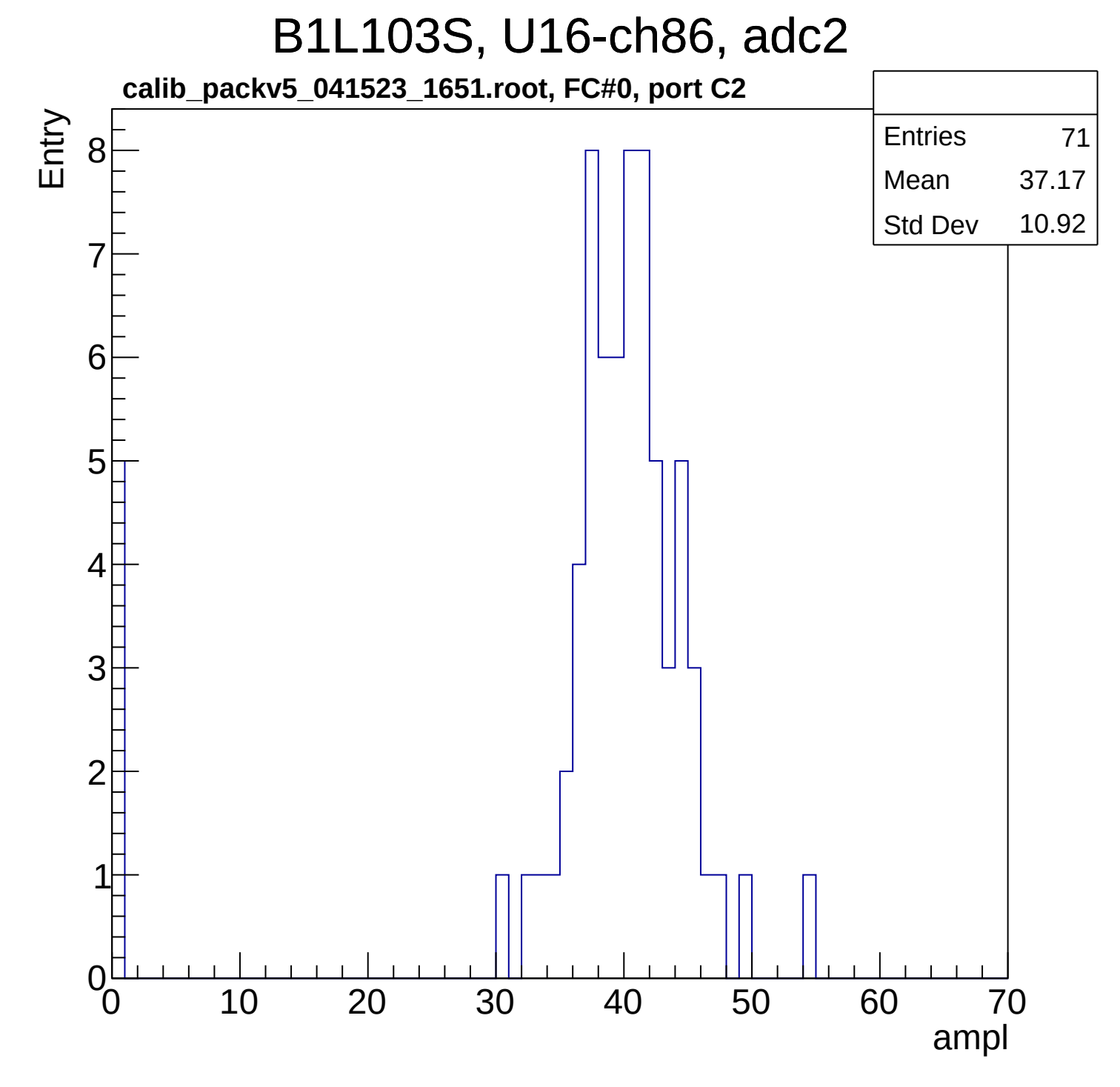
50
60
70
ampl


B1L103S, U16-ch86, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 37.17
Std Dev 10.92
Entry
ampl
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2
3
4
5
6
7
8
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60
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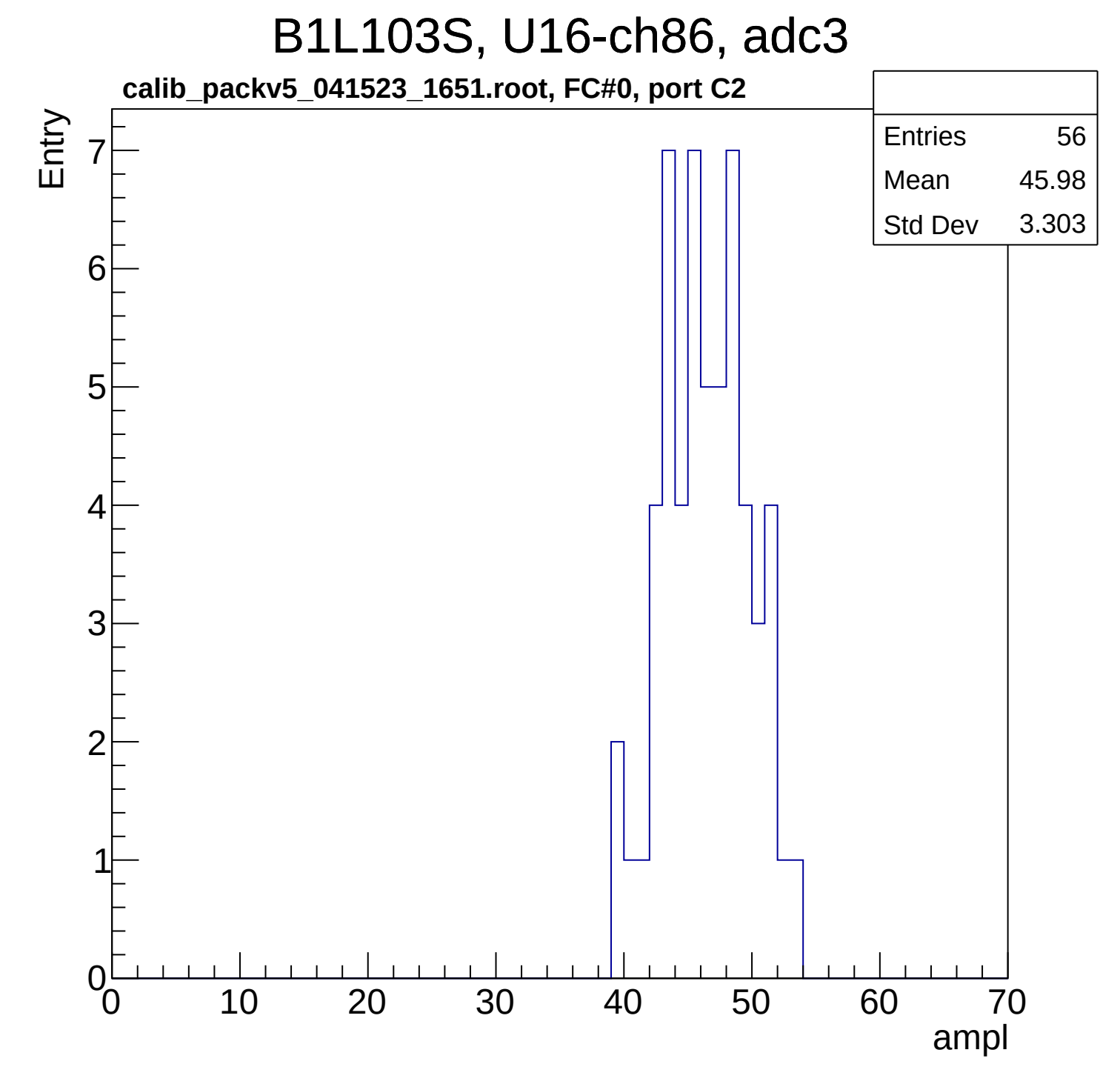
B1L103S, U16-ch86, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 45.98
Std Dev 3.303
Entry
ampl
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1
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3
4
5
6
7
0
10
20
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40
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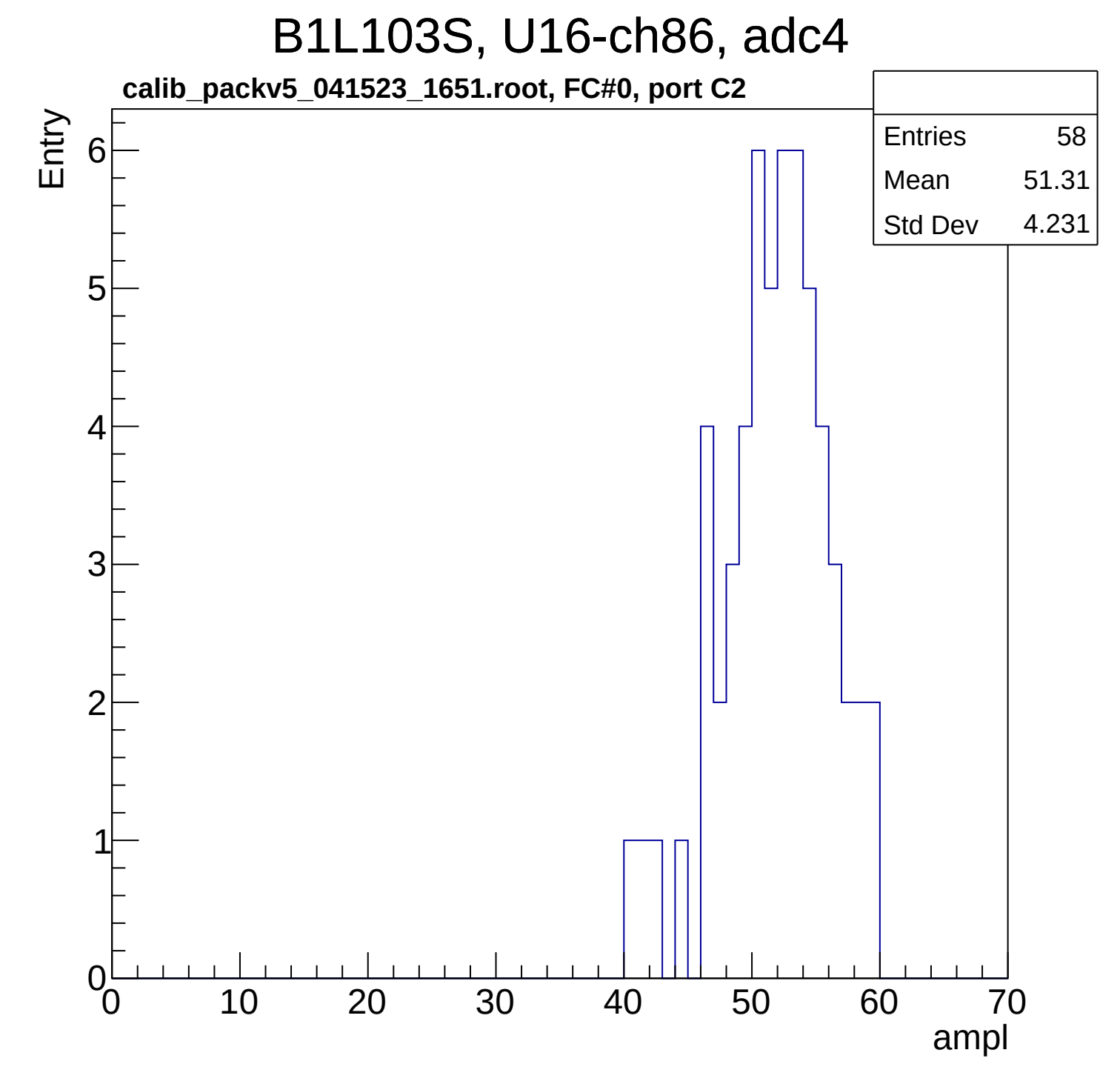
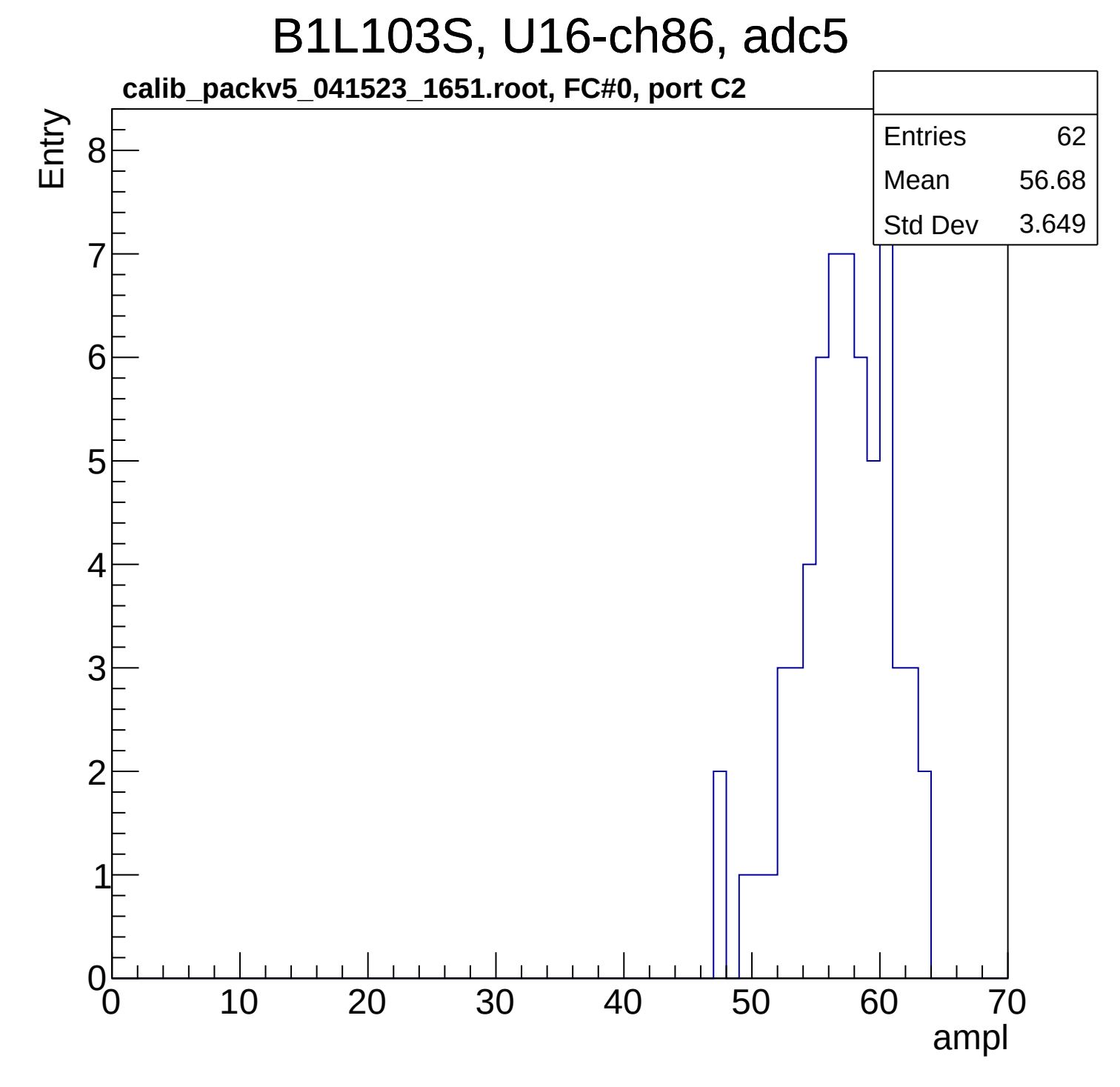
60
70


B1L103S, U16-ch86, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 51.31
Std Dev 4.231
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U16-ch86, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 56.68
Std Dev 3.649
Entry
ampl
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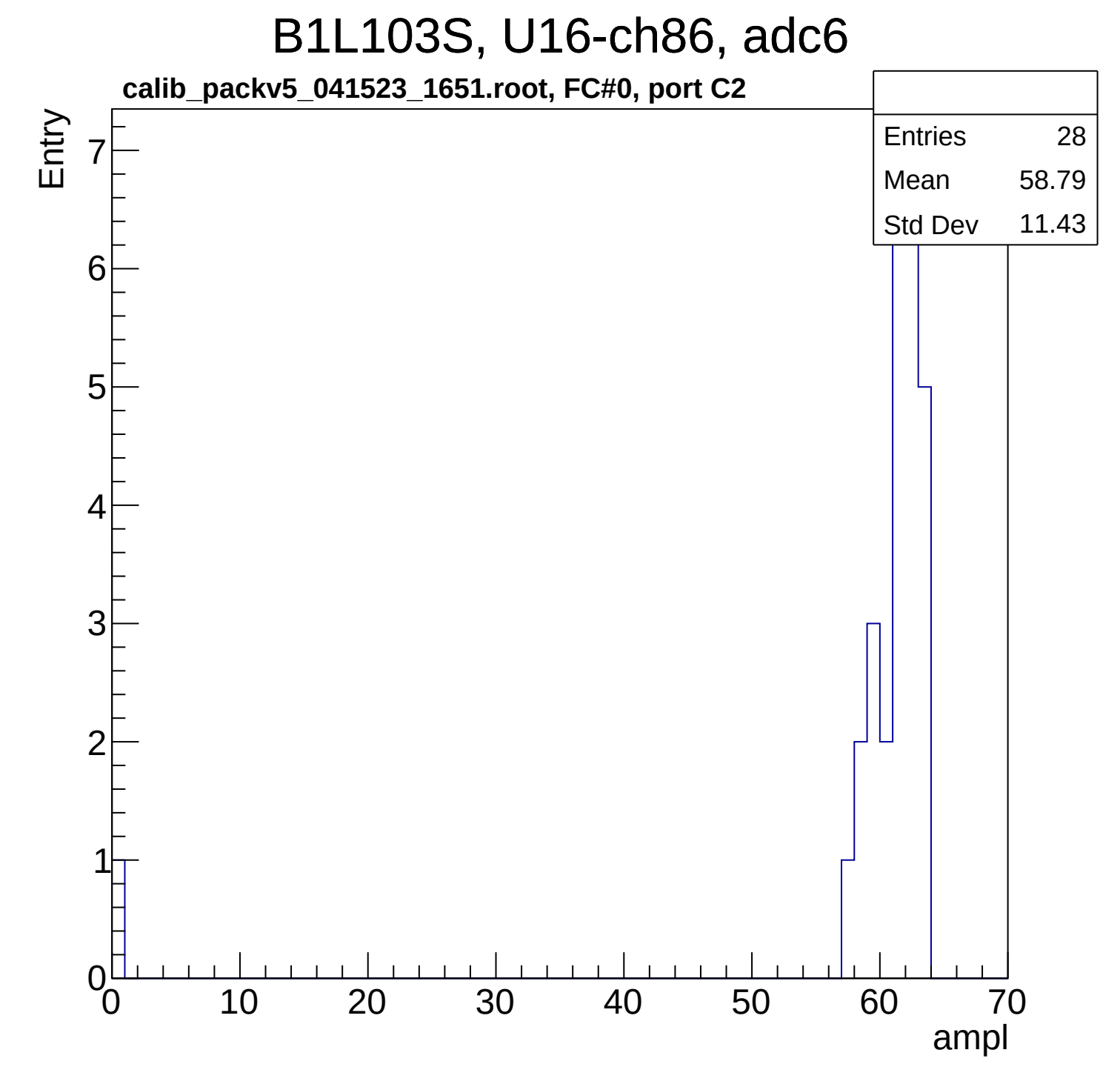
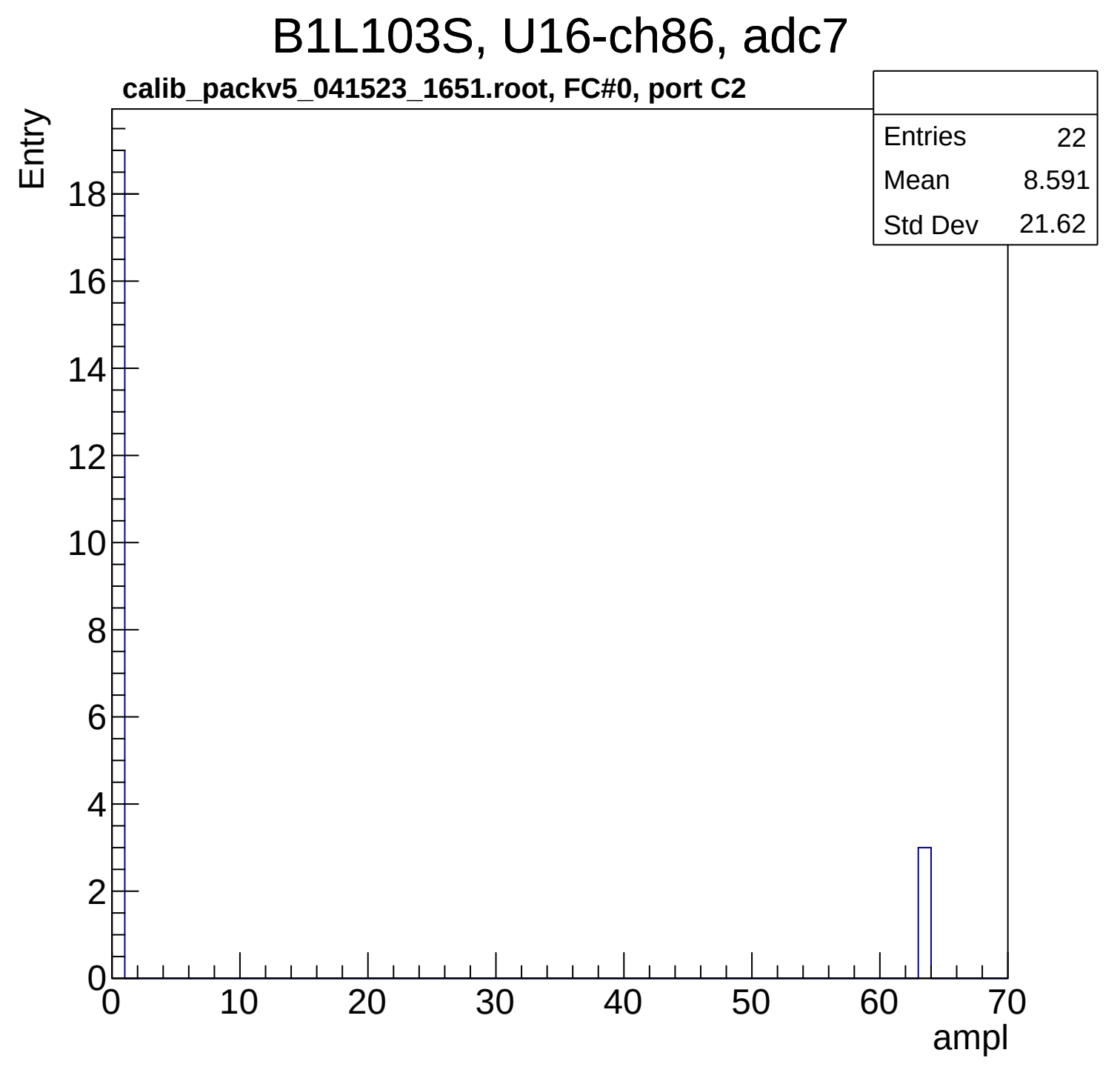
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch86, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 58.79
Std Dev 11.43
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch86, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.591
Std Dev 21.62
Entry
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6
8
10
12
14
16
18
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10
20
30
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50
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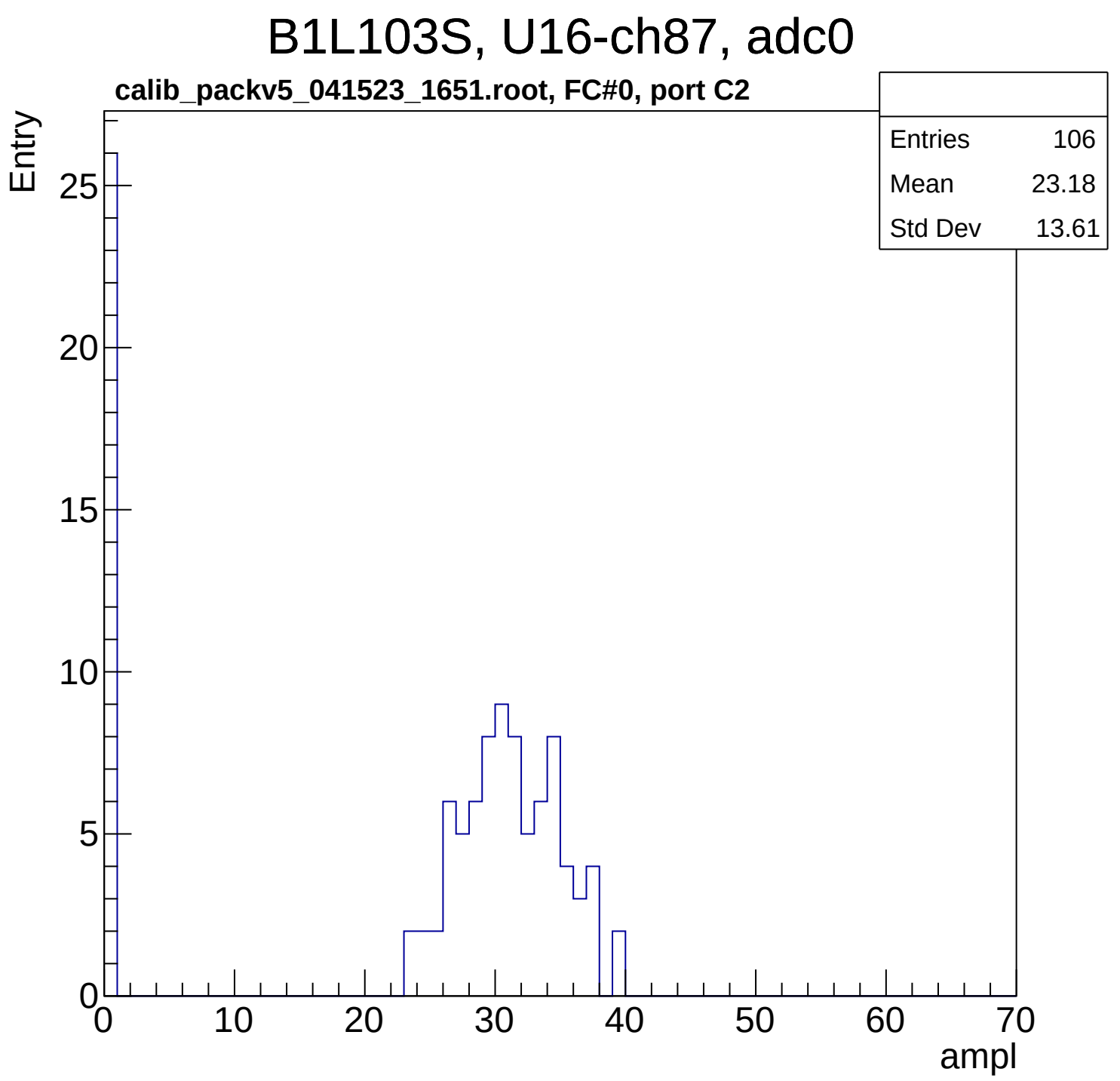
70
ampl


B1L103S, U16-ch87, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 106
Mean 23.18
Std Dev 13.61
Entry
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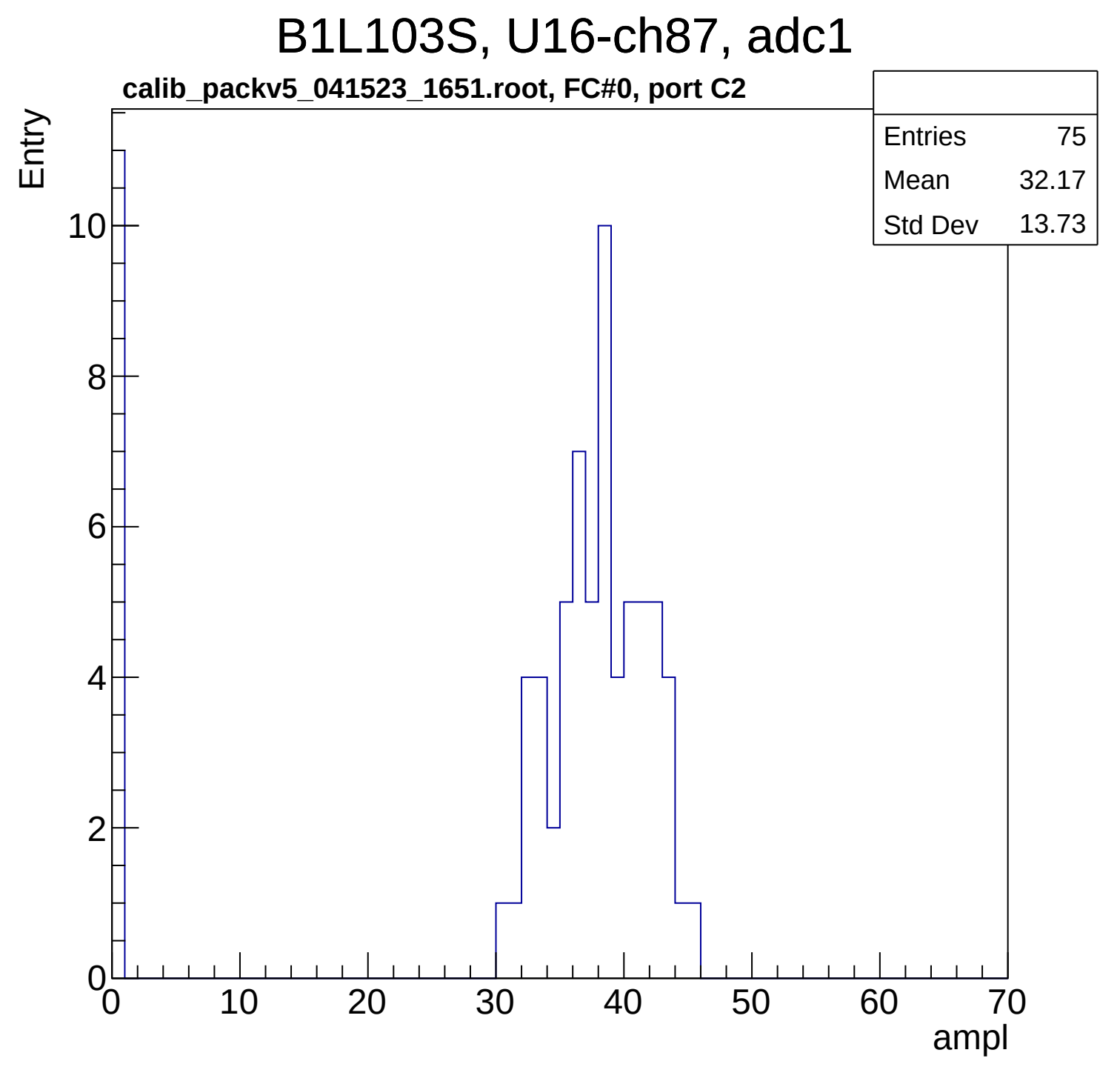
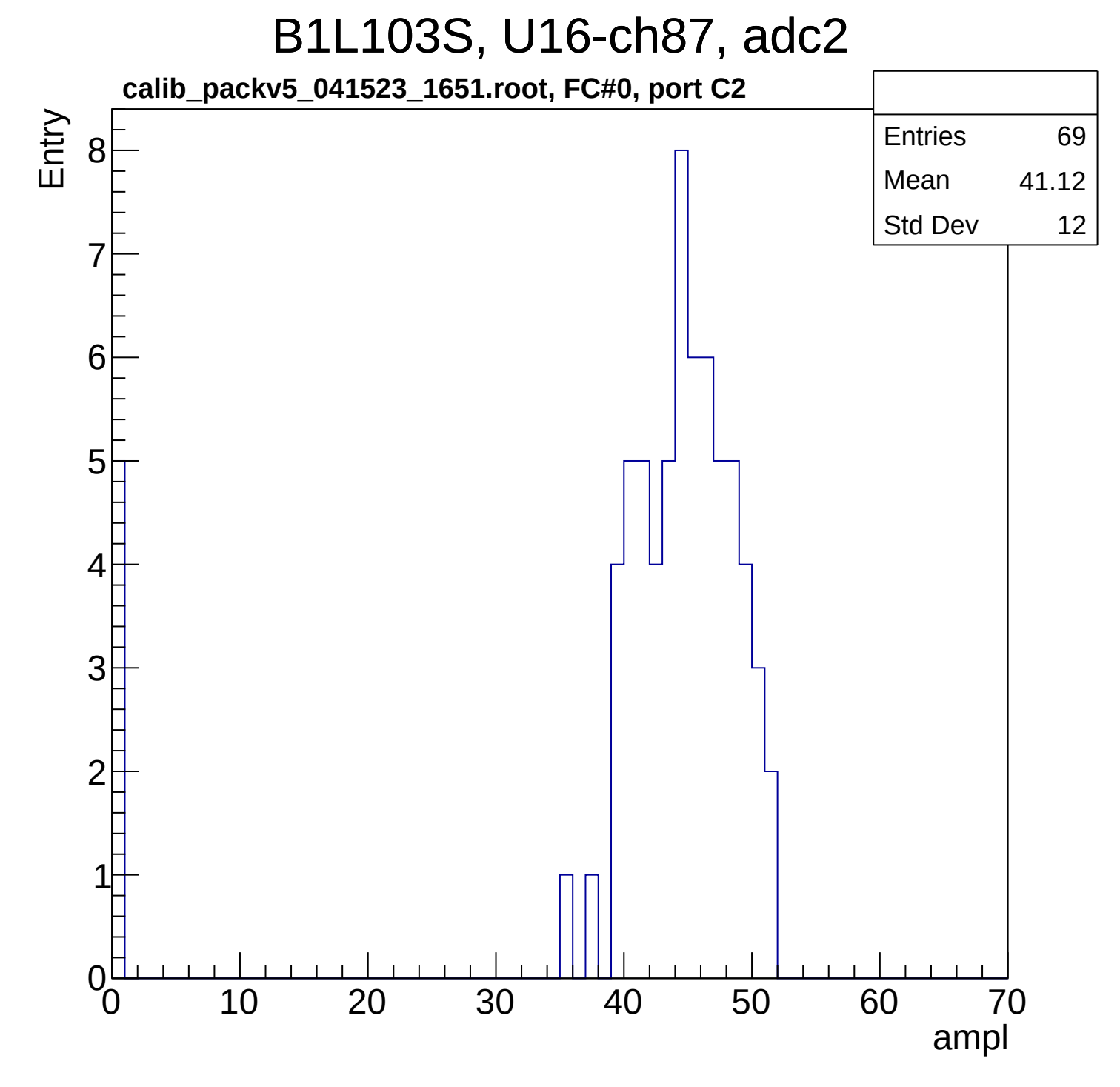
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch87, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 32.17
Std Dev 13.73
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch87, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 41.12
Std Dev 12
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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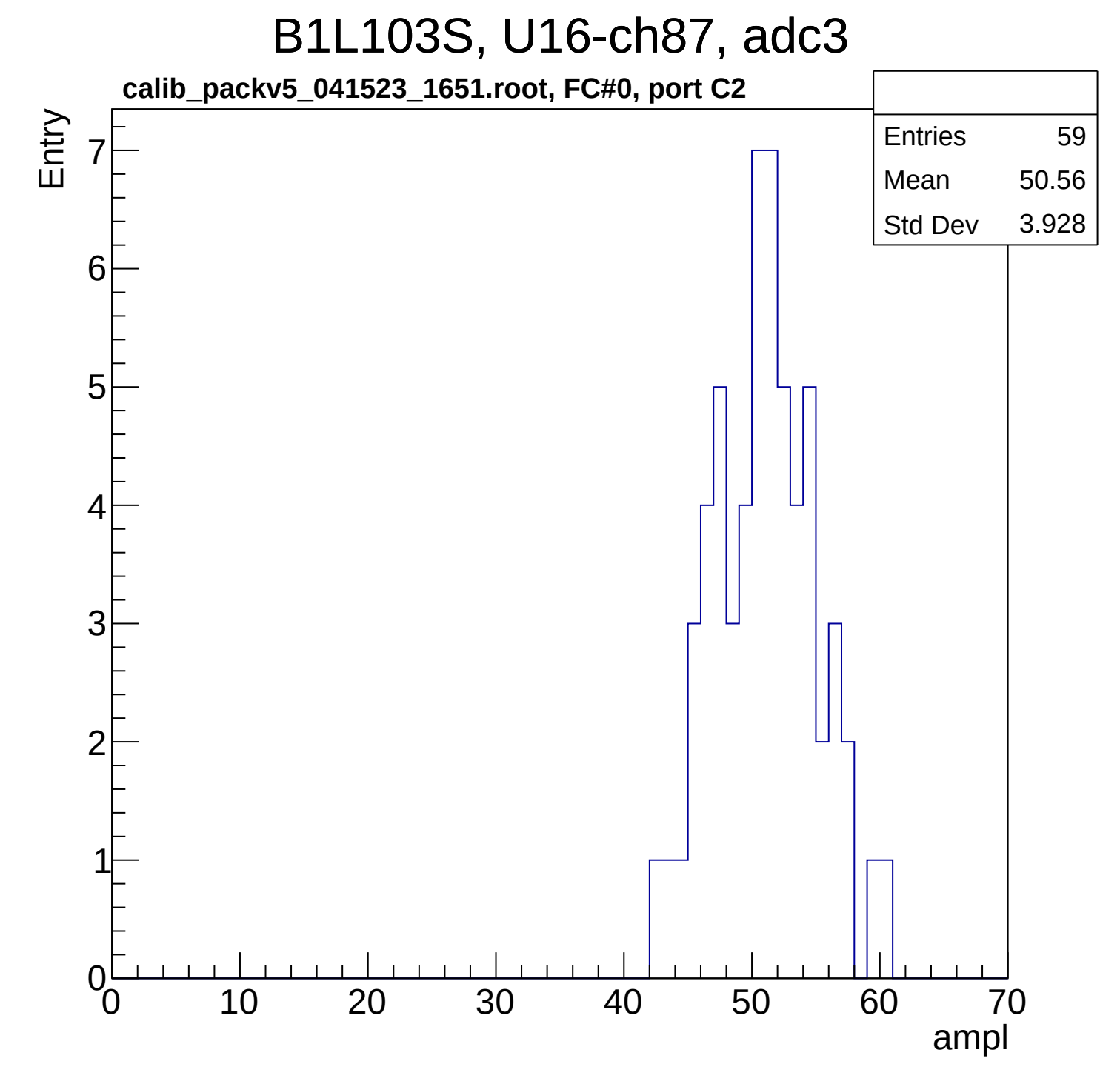
B1L103S, U16-ch87, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 50.56
Std Dev 3.928
Entry
ampl
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4
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6
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40
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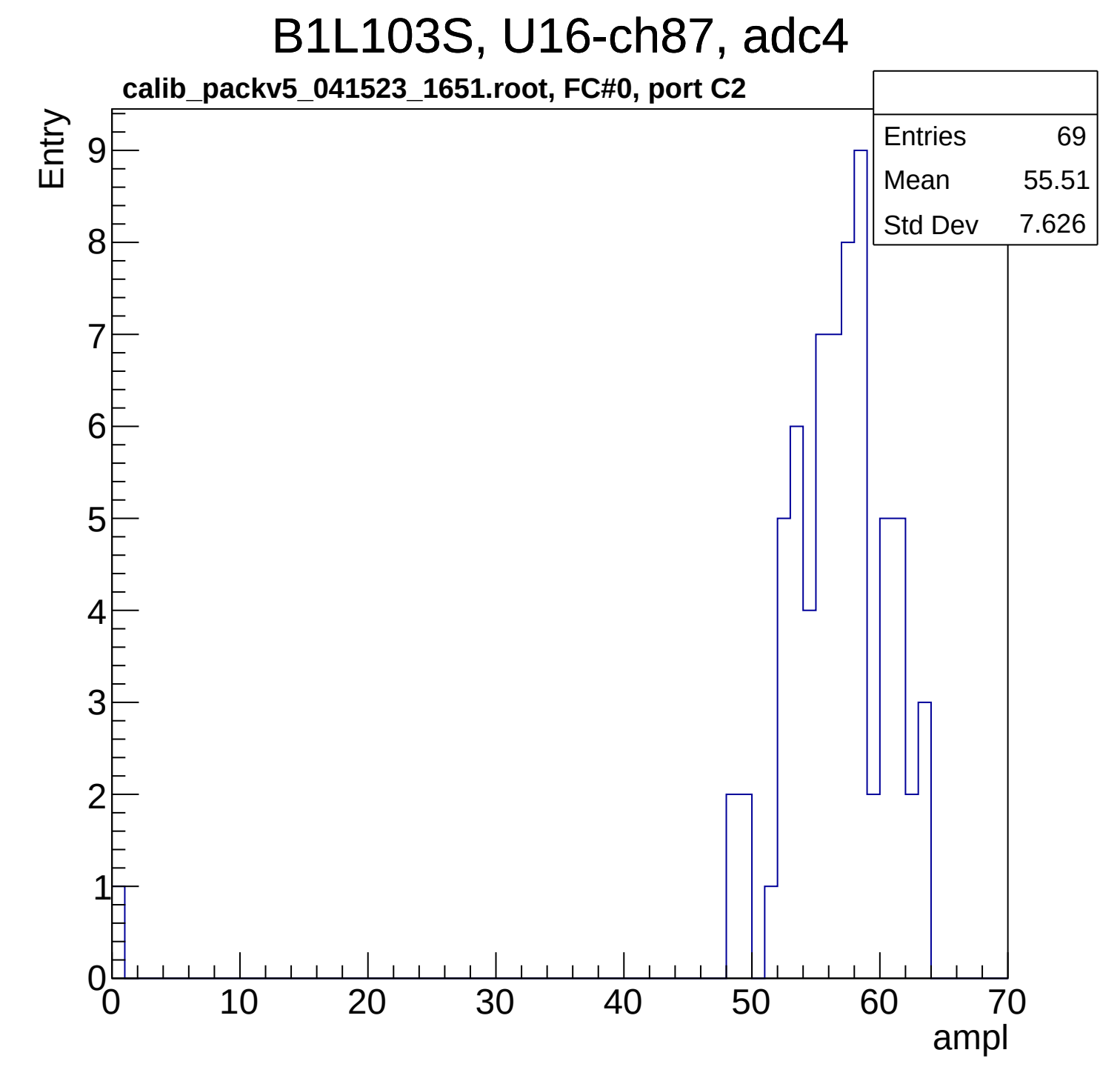
B1L103S, U16-ch87, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 55.51
Std Dev 7.626
Entry
ampl
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2
3
4
5
6
7
8
9
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10
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50
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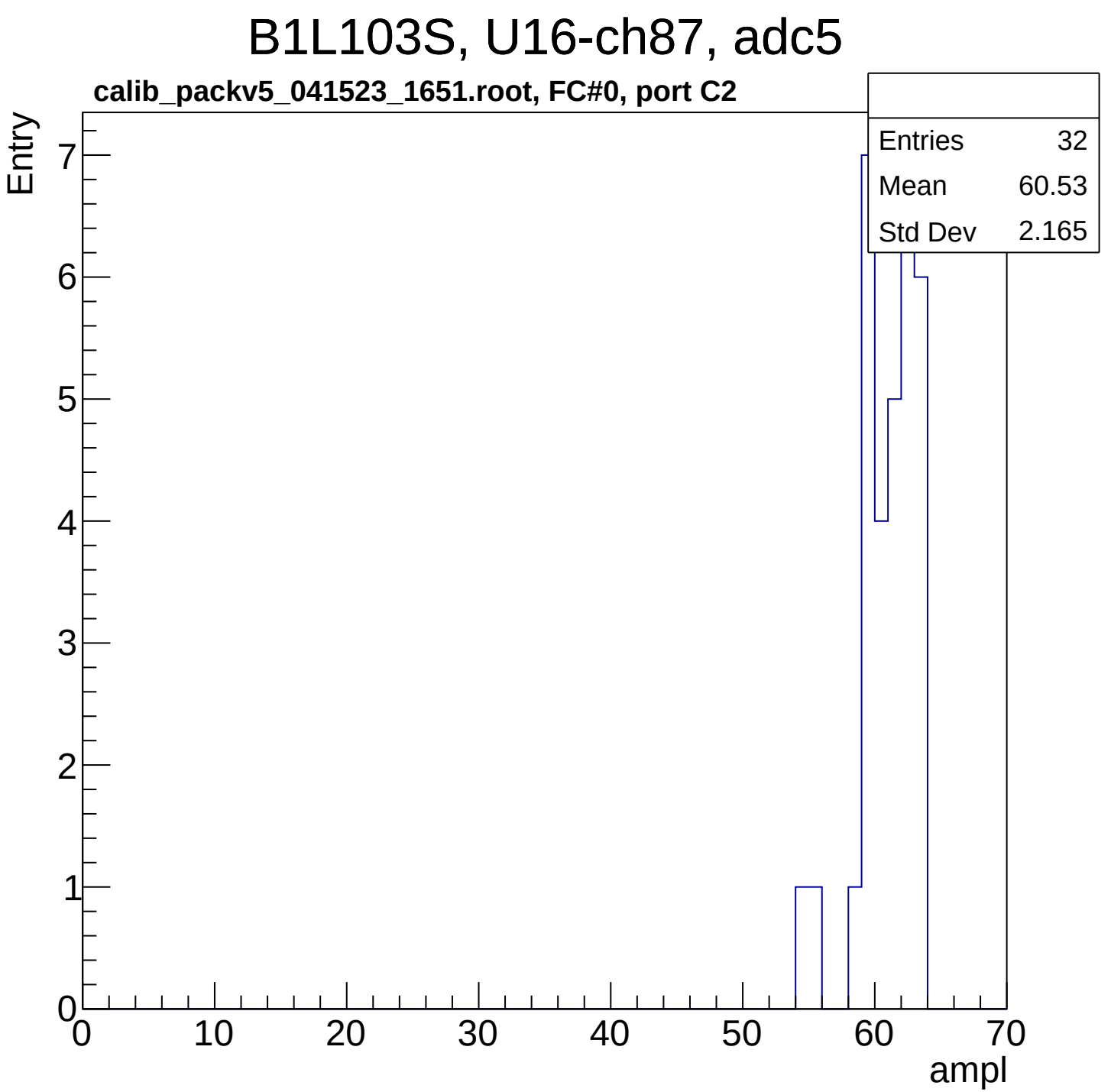
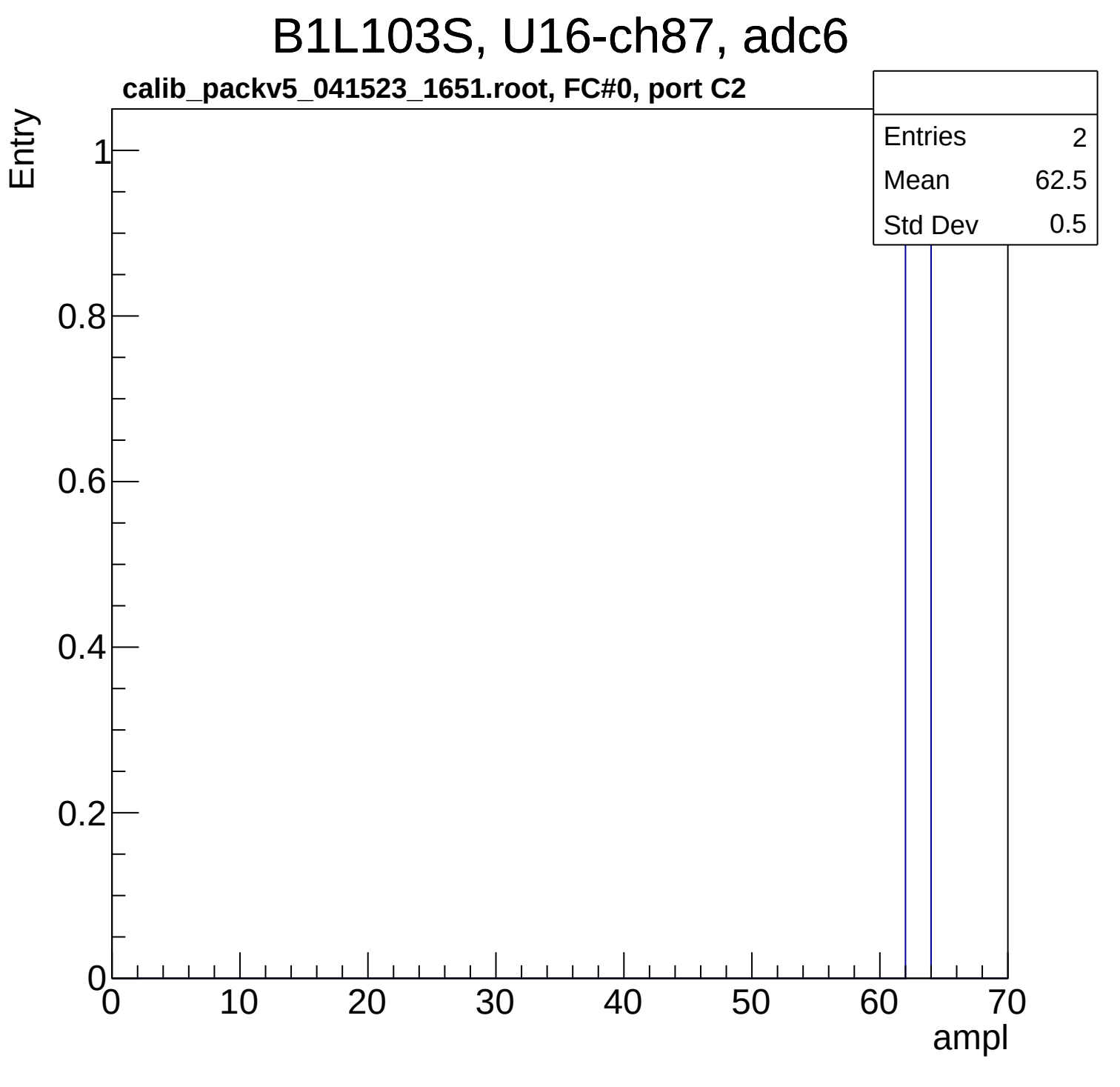

B1L103S, U16-ch87, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 60.53
Std Dev 2.165
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch87, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
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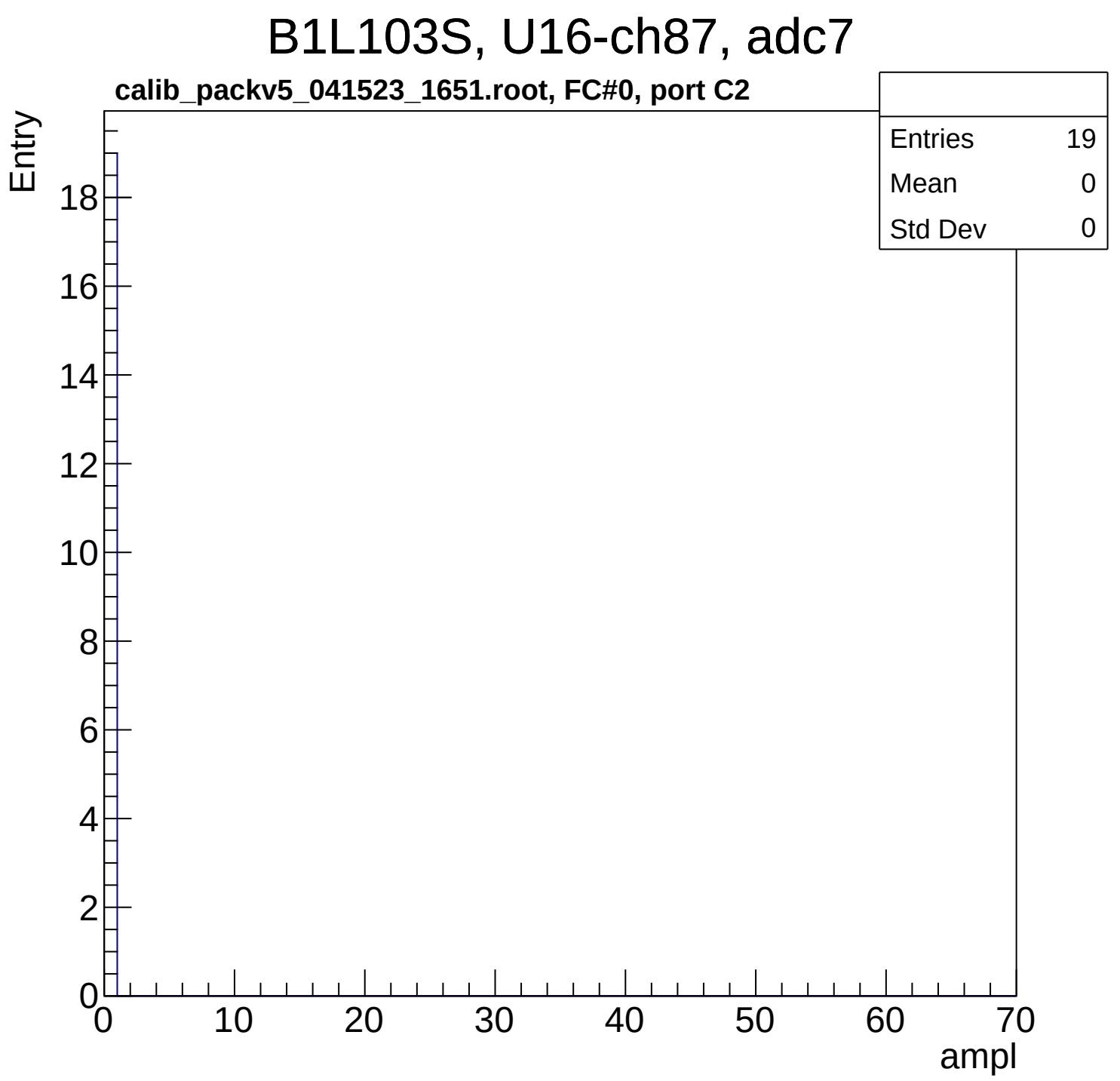
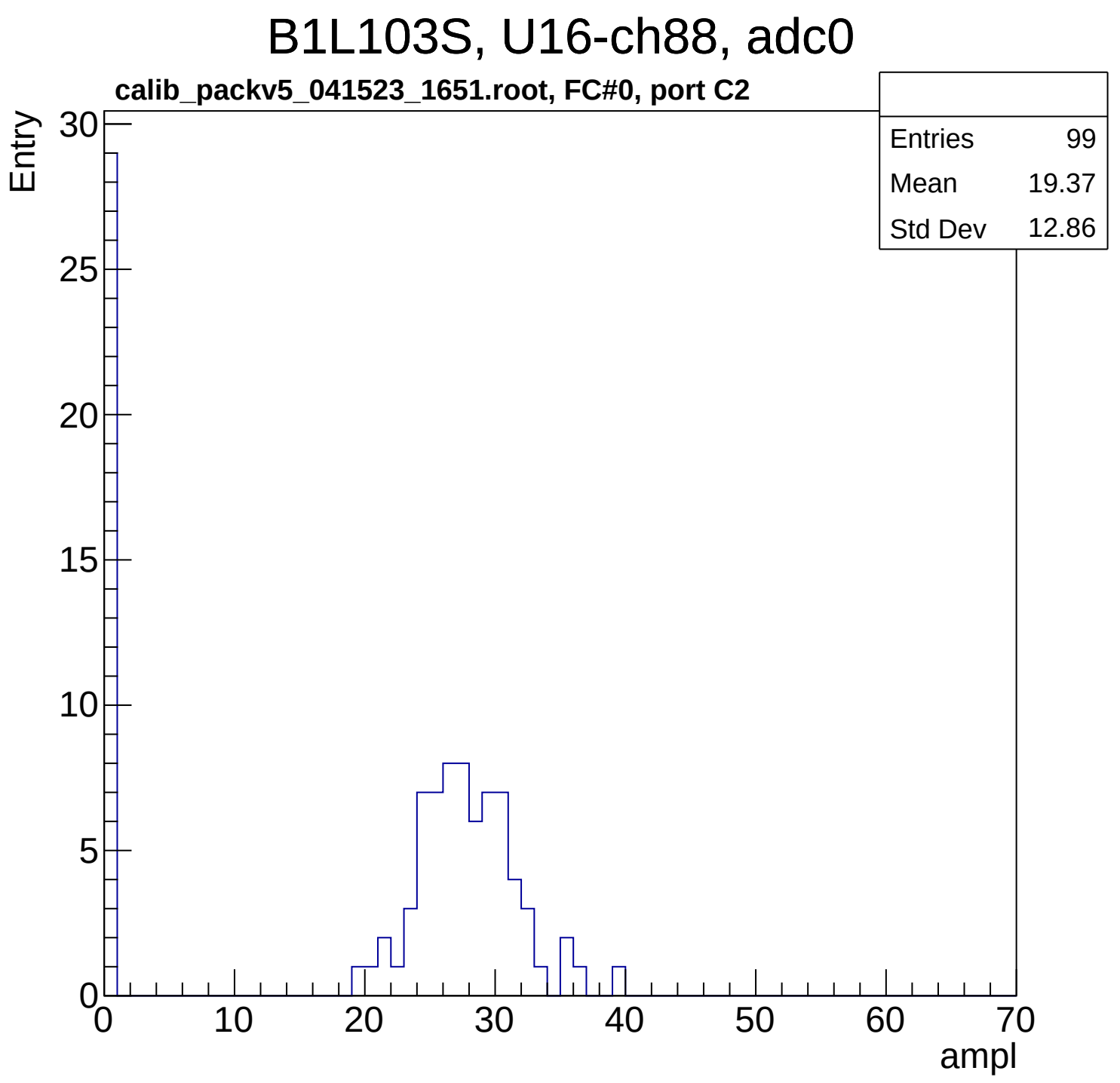
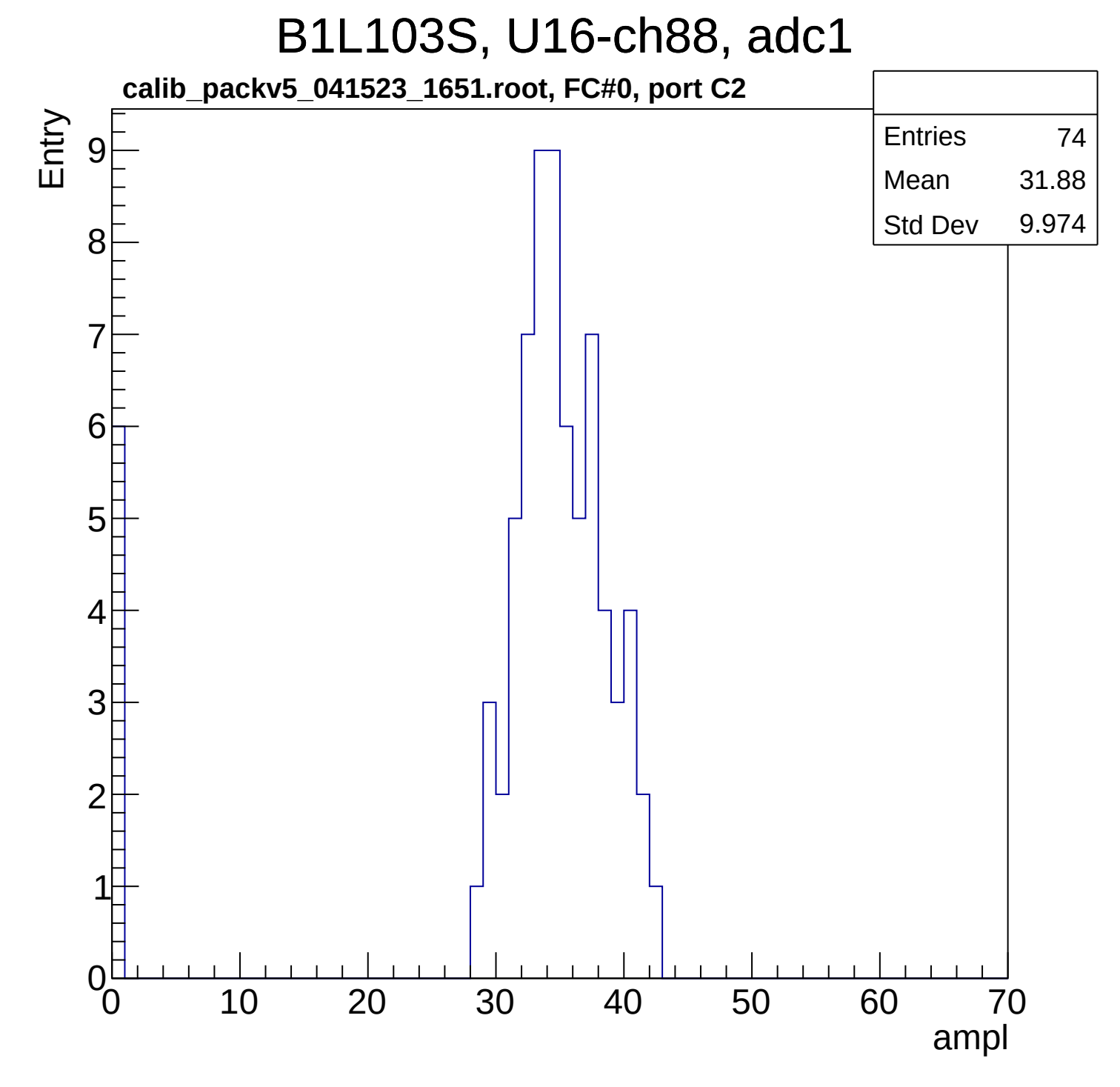
50
60
70
ampl


B1L103S, U16-ch87, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch88, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 19.37
Std Dev 12.86
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70


B1L103S, U16-ch88, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 31.88
Std Dev 9.974
Entry
ampl
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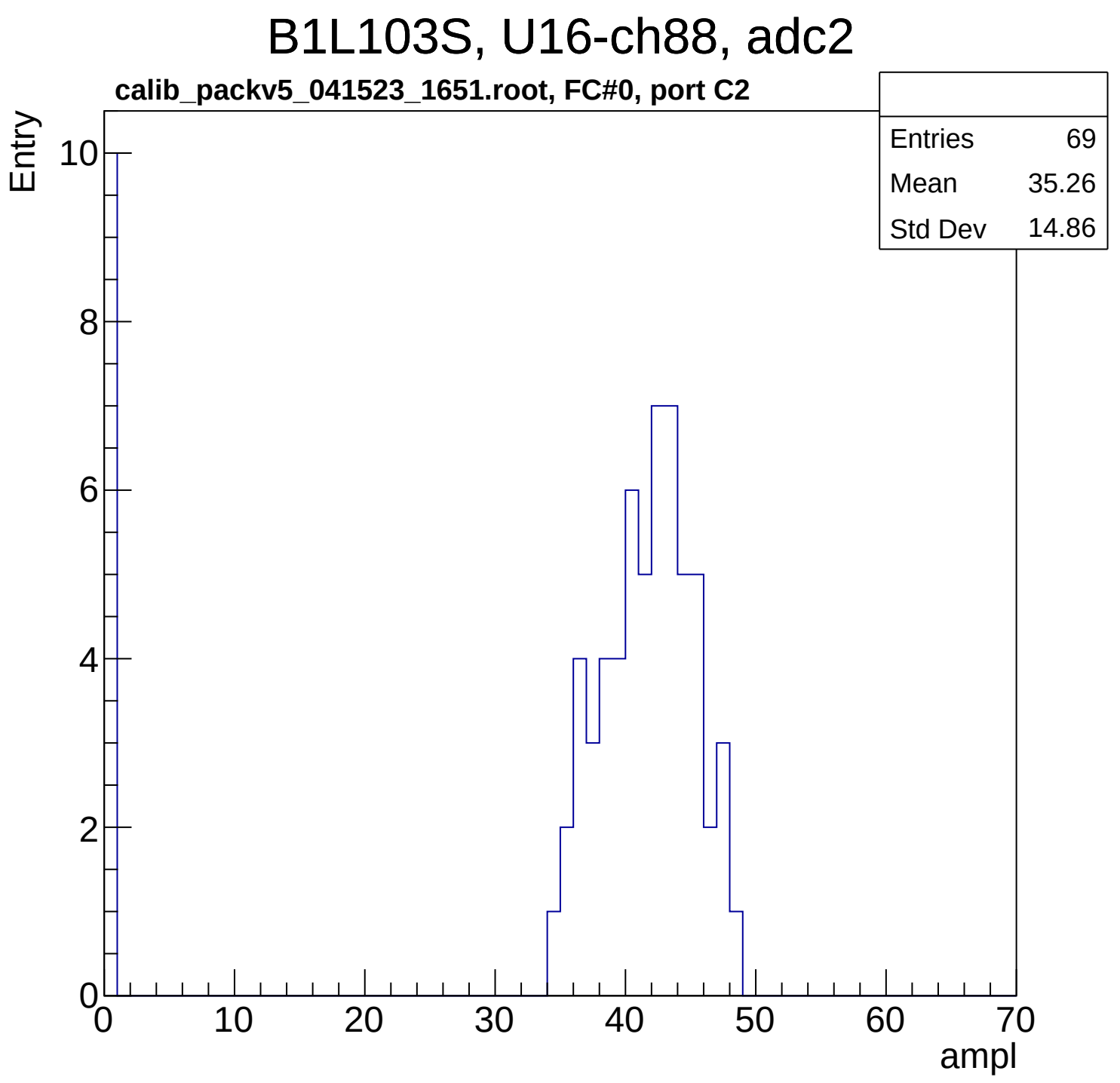
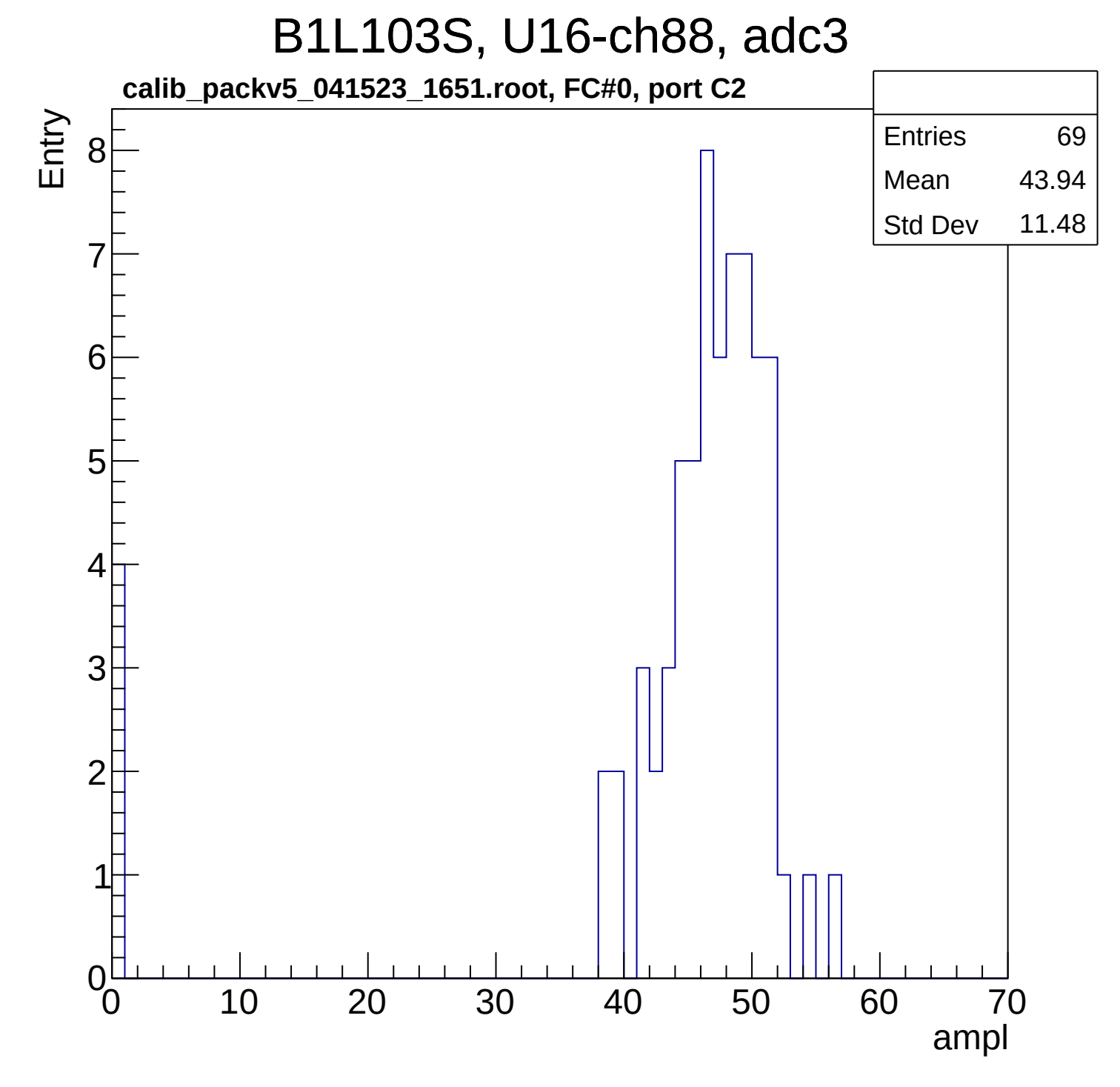
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch88, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 35.26
Std Dev 14.86
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch88, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 43.94
Std Dev 11.48
Entry
ampl
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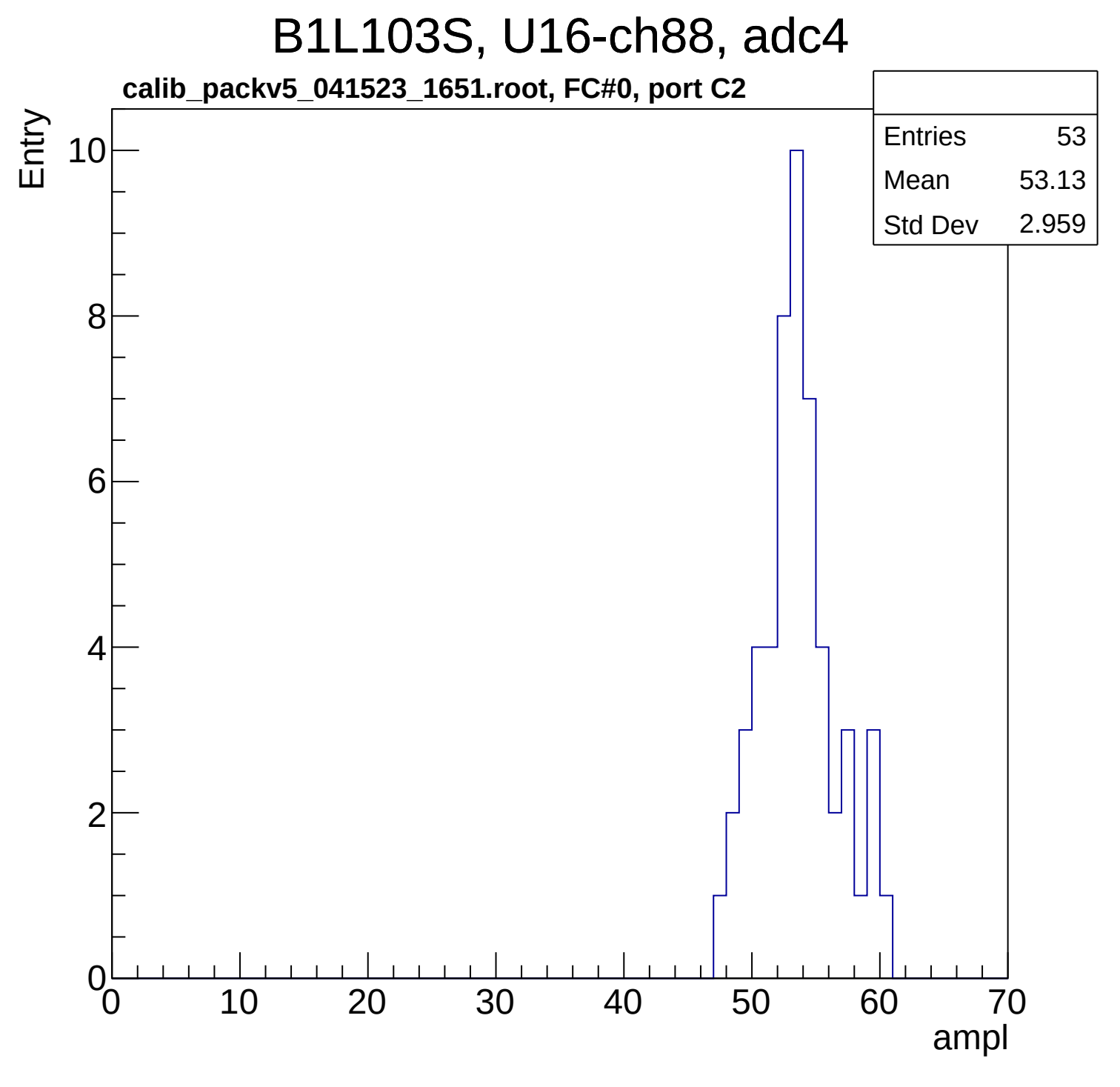
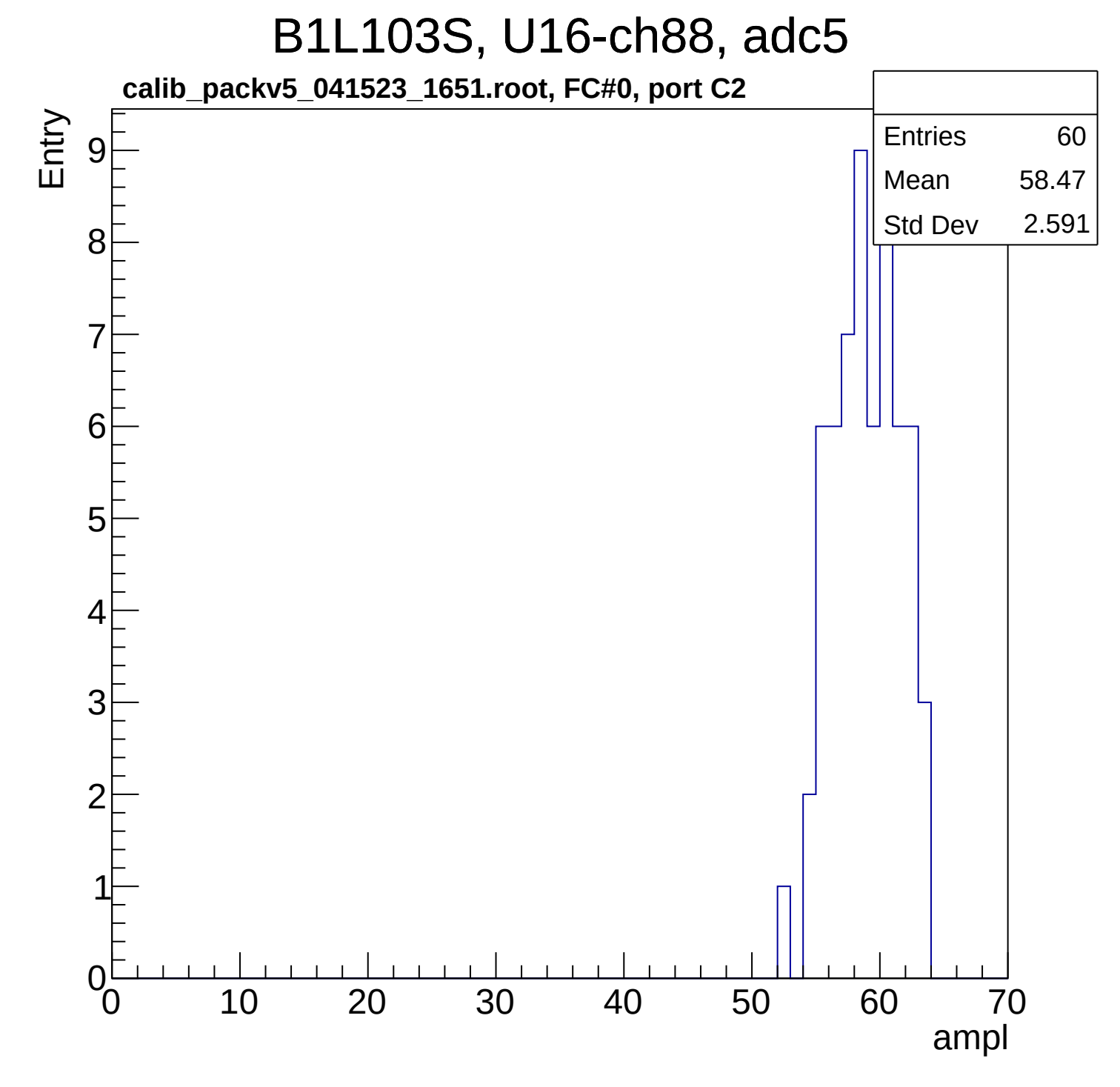
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch88, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 53.13
Std Dev 2.959
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch88, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 58.47
Std Dev 2.591
Entry
ampl
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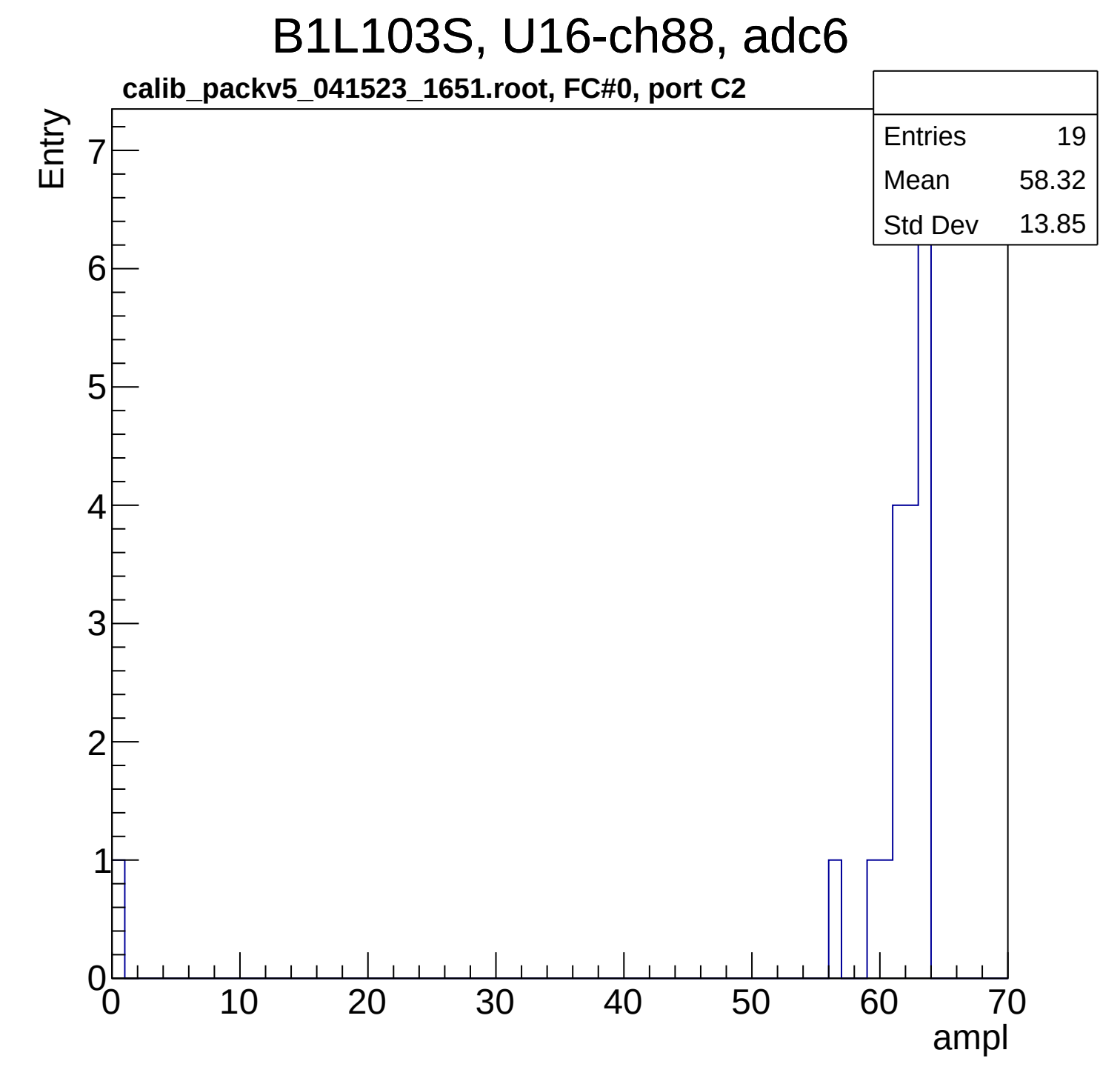
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch88, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 58.32
Std Dev 13.85
Entry
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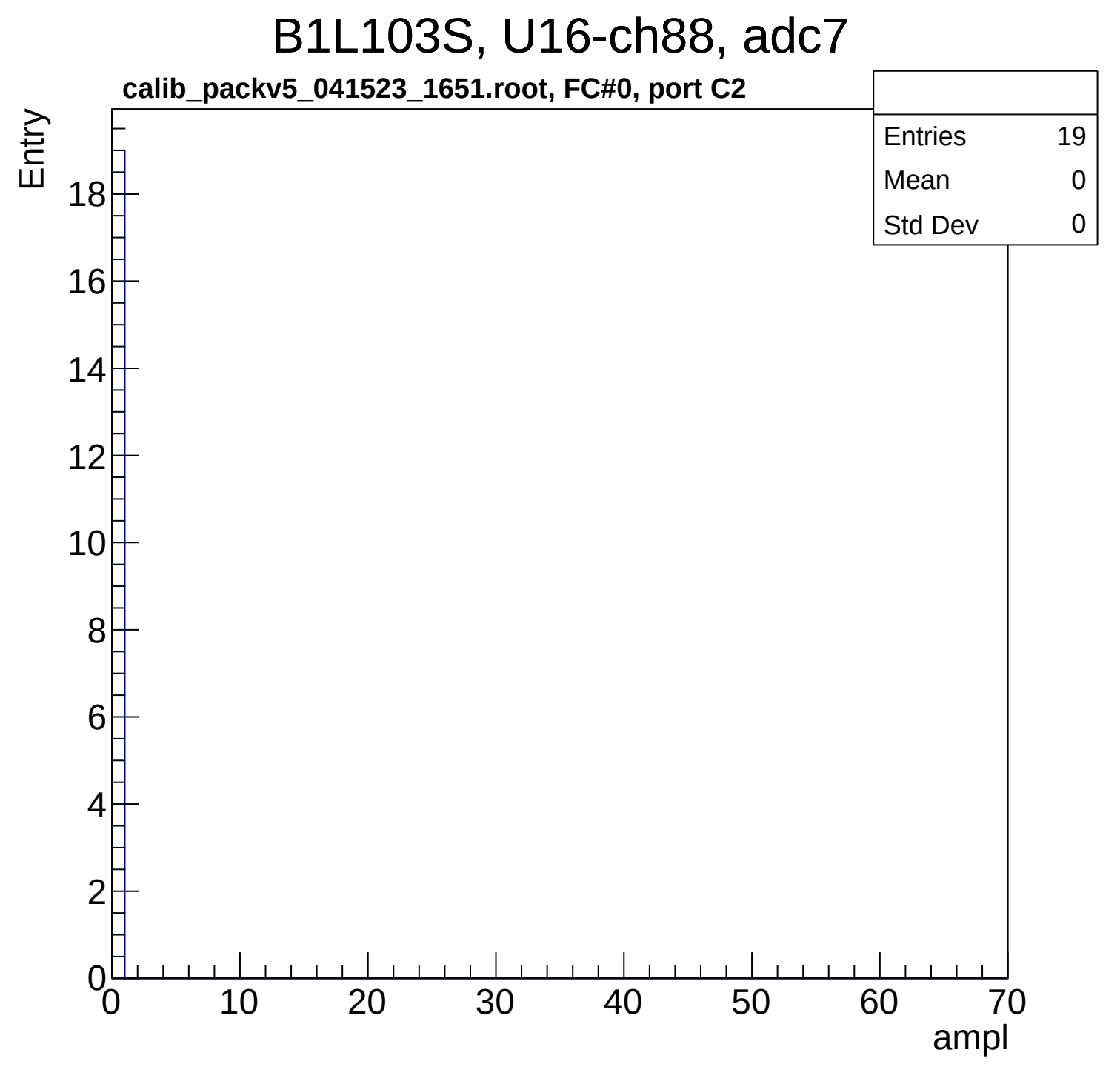
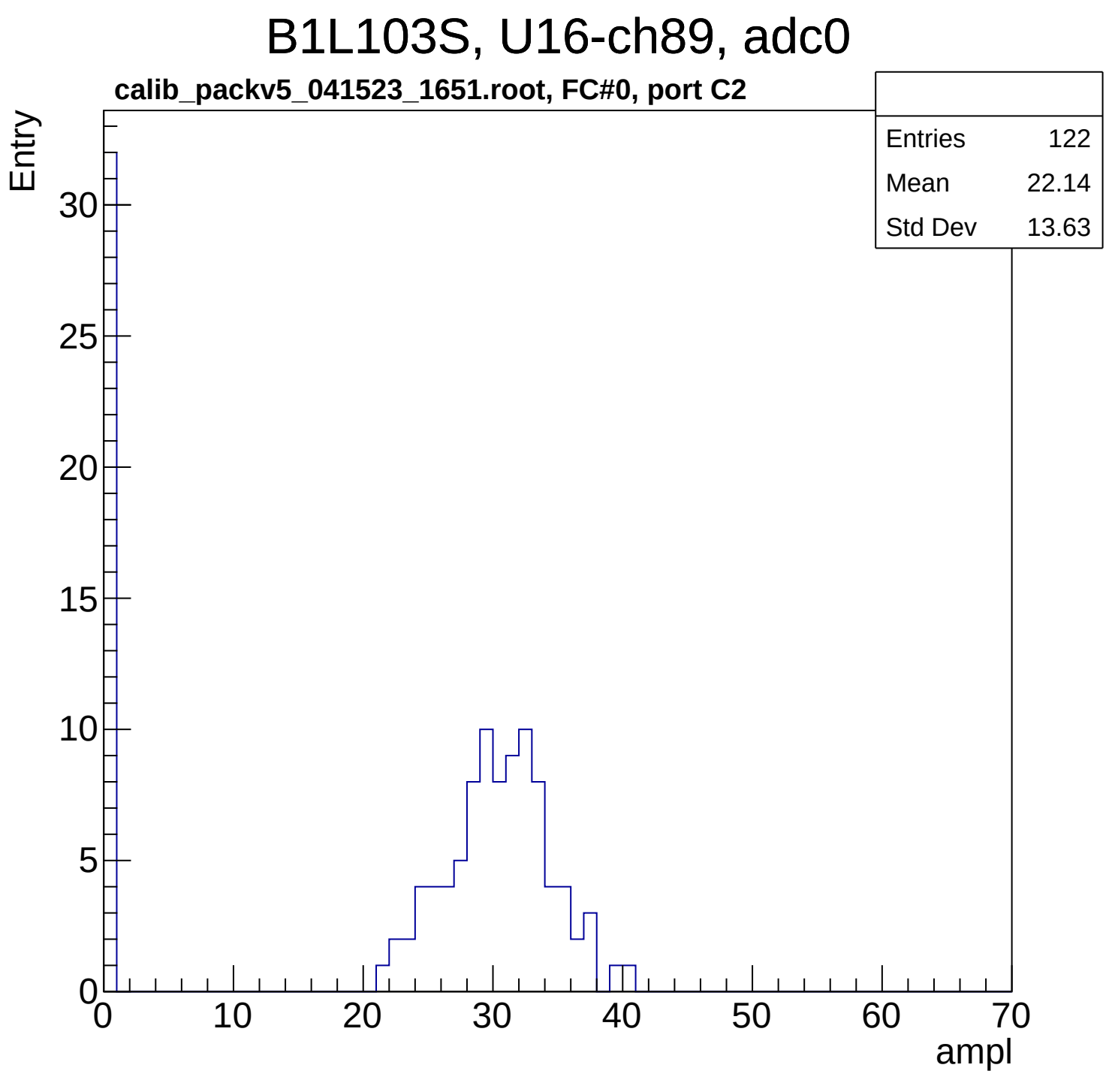
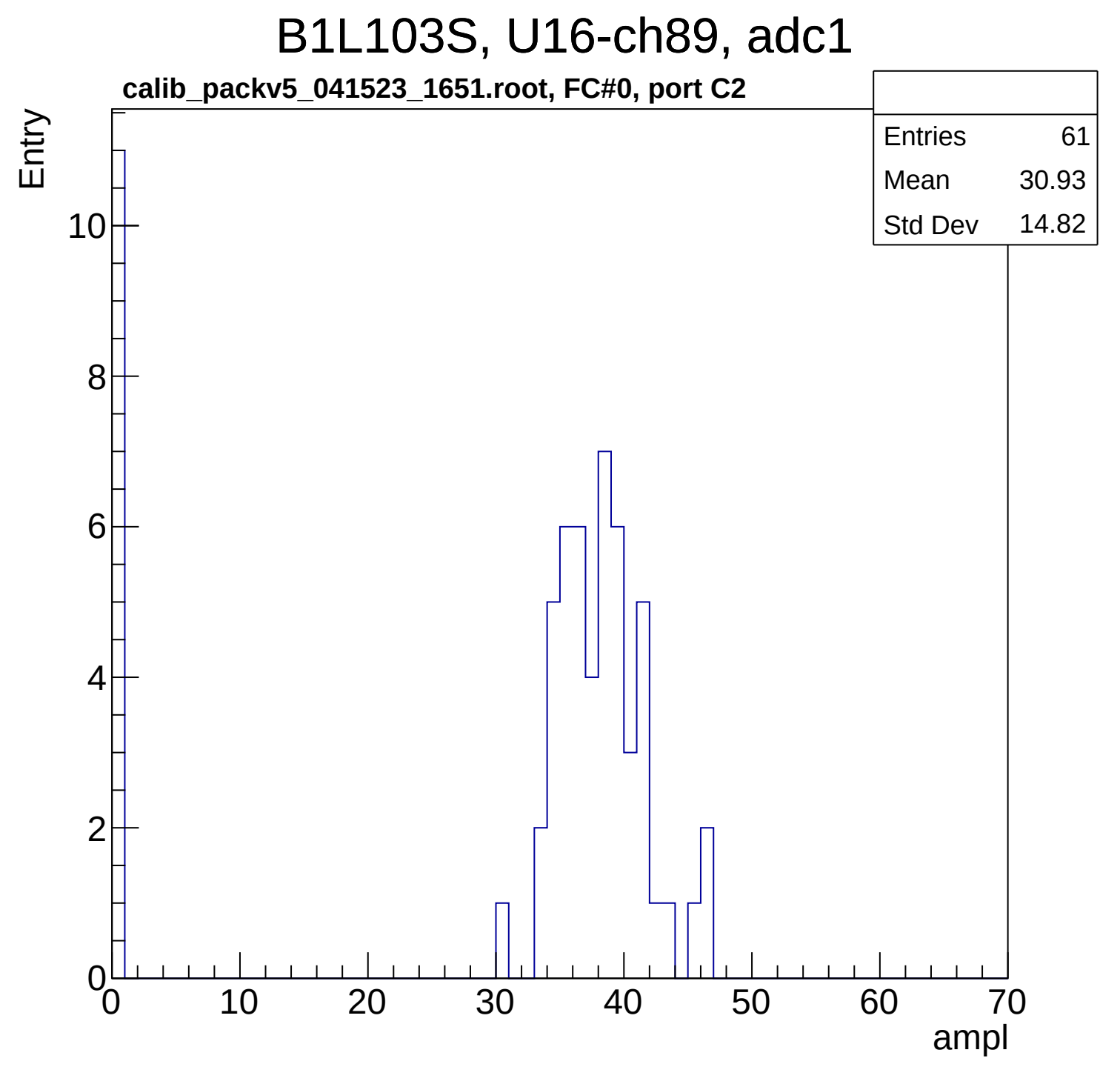
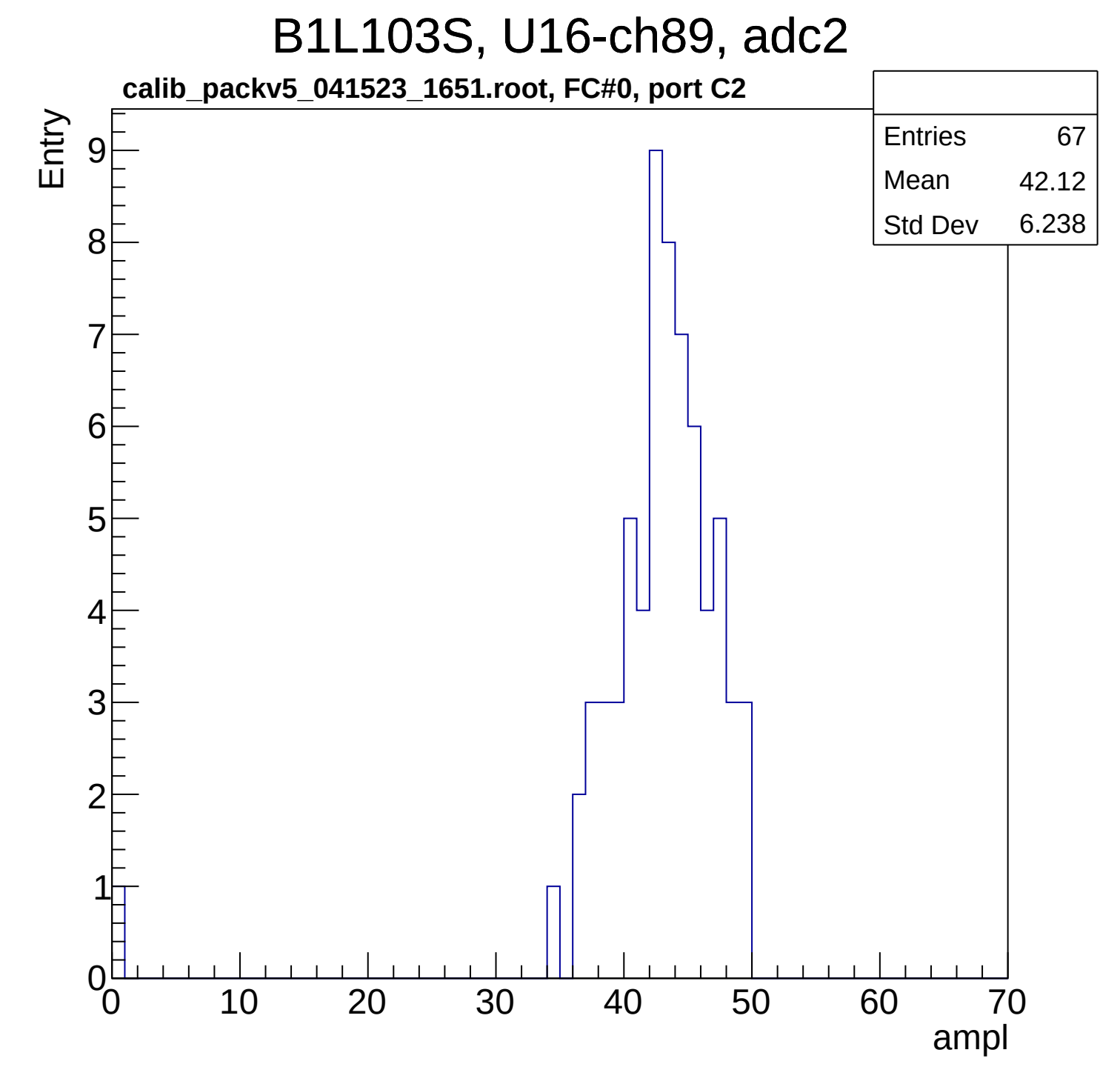
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch88, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch89, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 122
Mean 22.14
Std Dev 13.63
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch89, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 30.93
Std Dev 14.82
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch89, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 42.12
Std Dev 6.238
Entry
ampl
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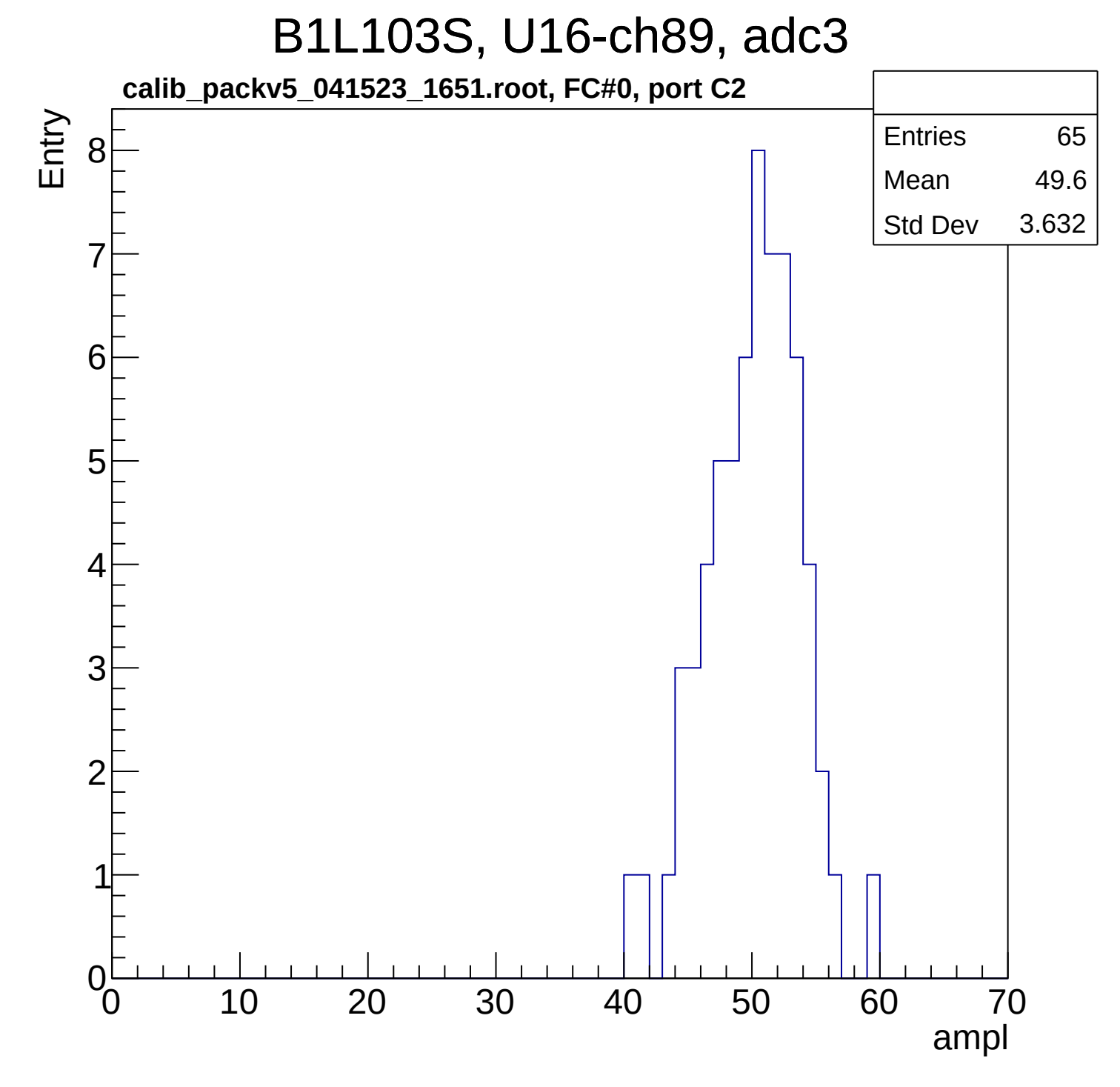
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch89, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 49.6
Std Dev 3.632
Entry
ampl
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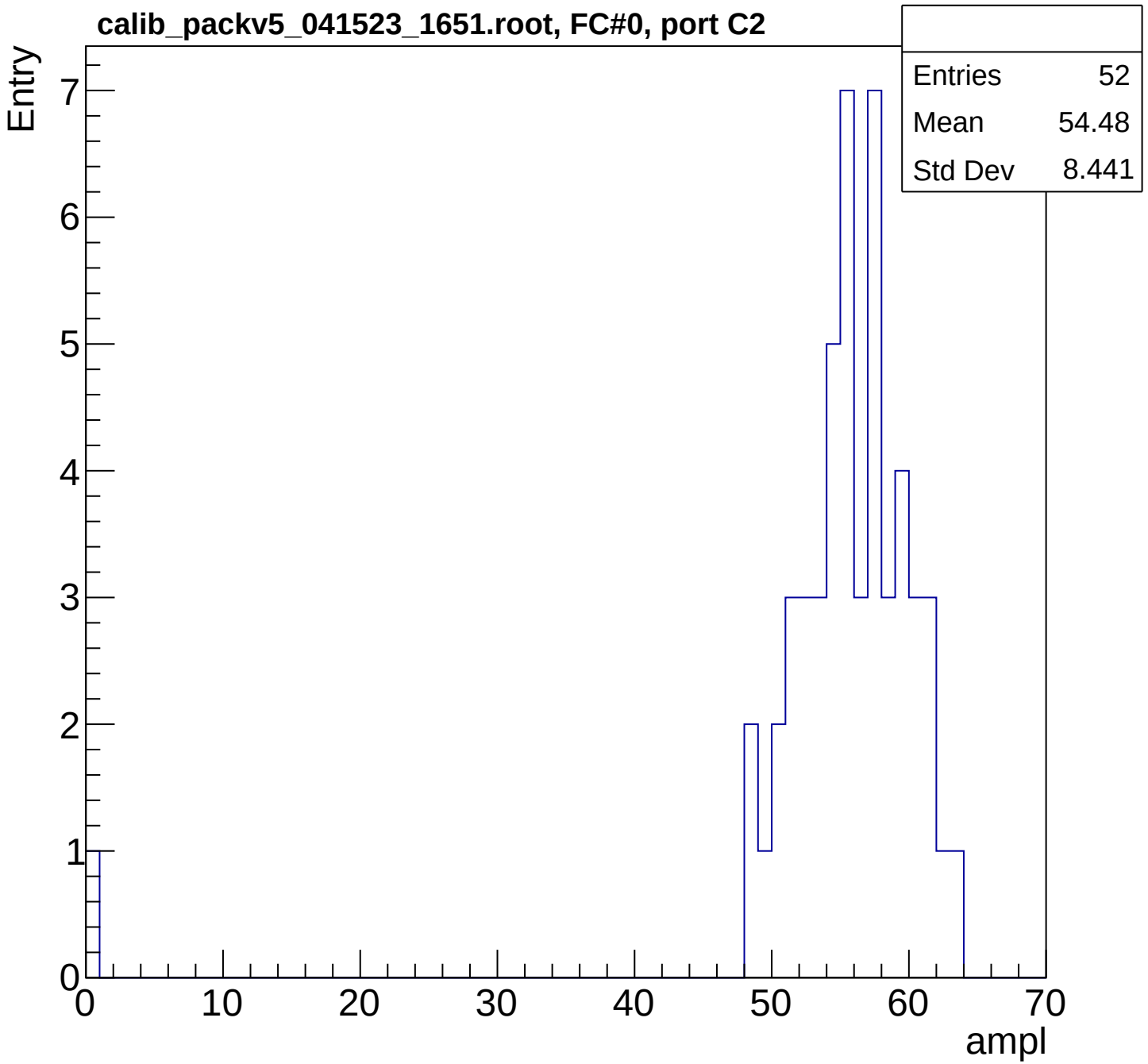
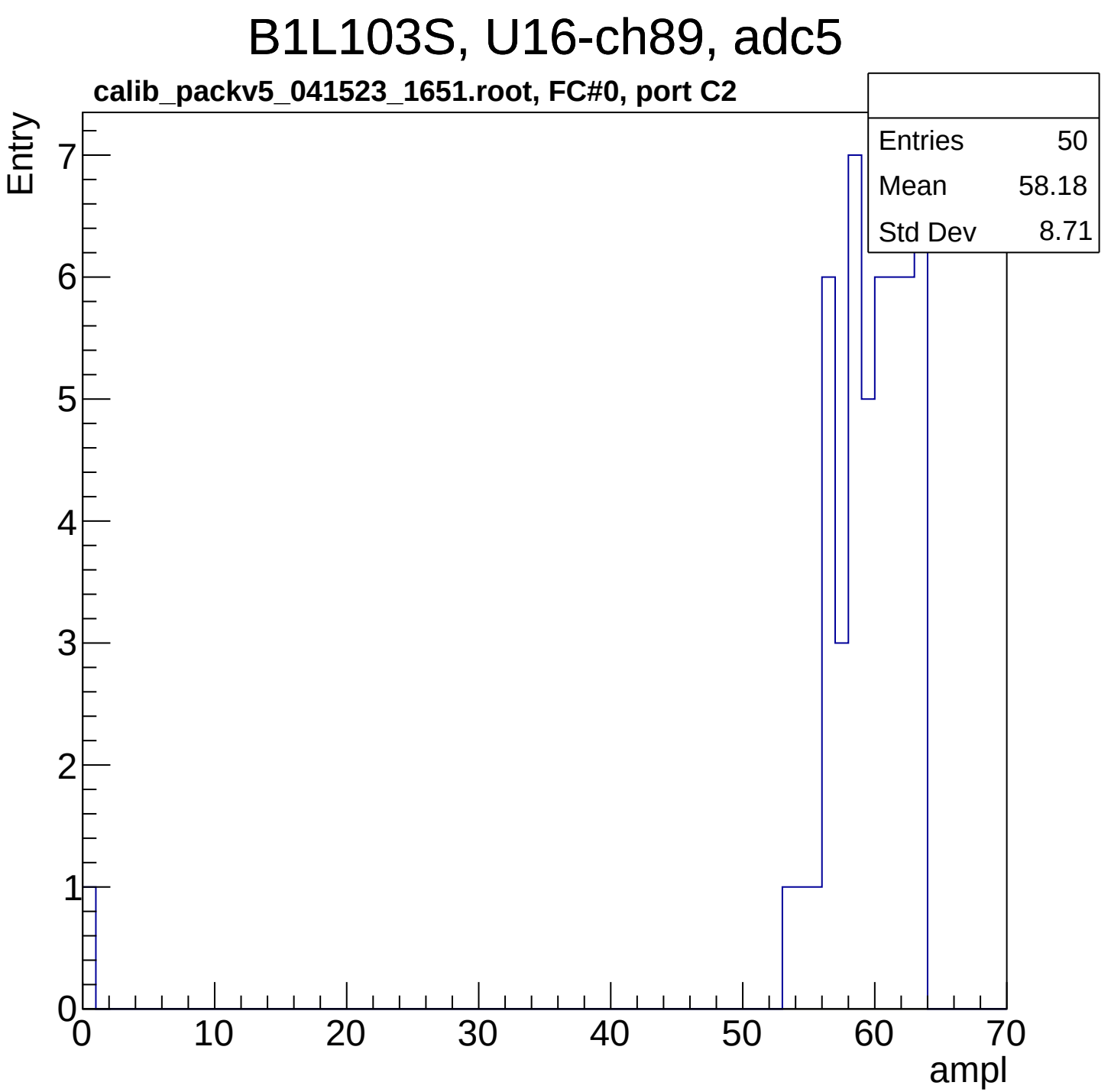
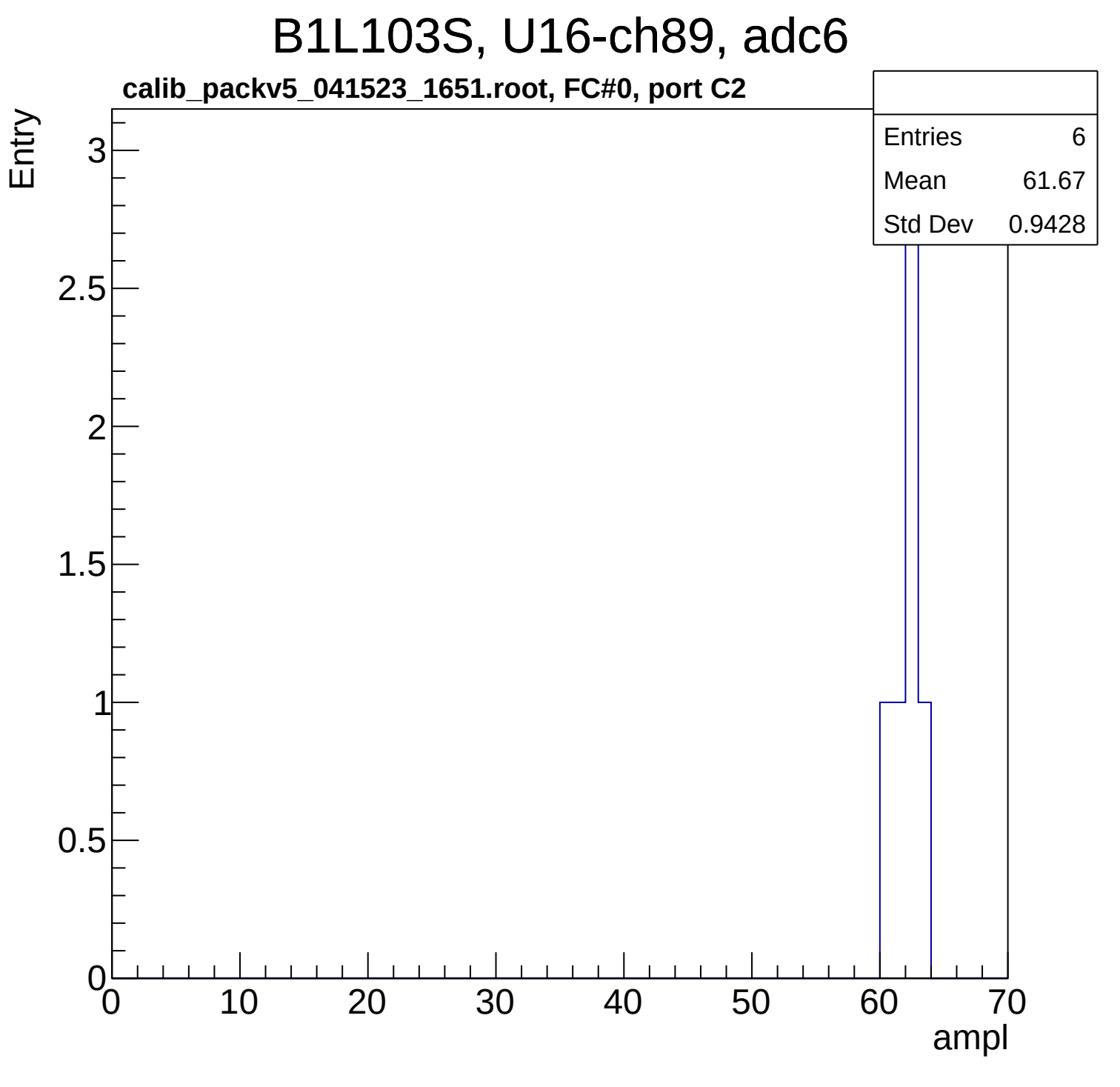
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch89, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 54.48
Std Dev 8.441
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch89, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.18
Std Dev 8.71
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch89, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.67
Std Dev 0.9428
Entry
ampl
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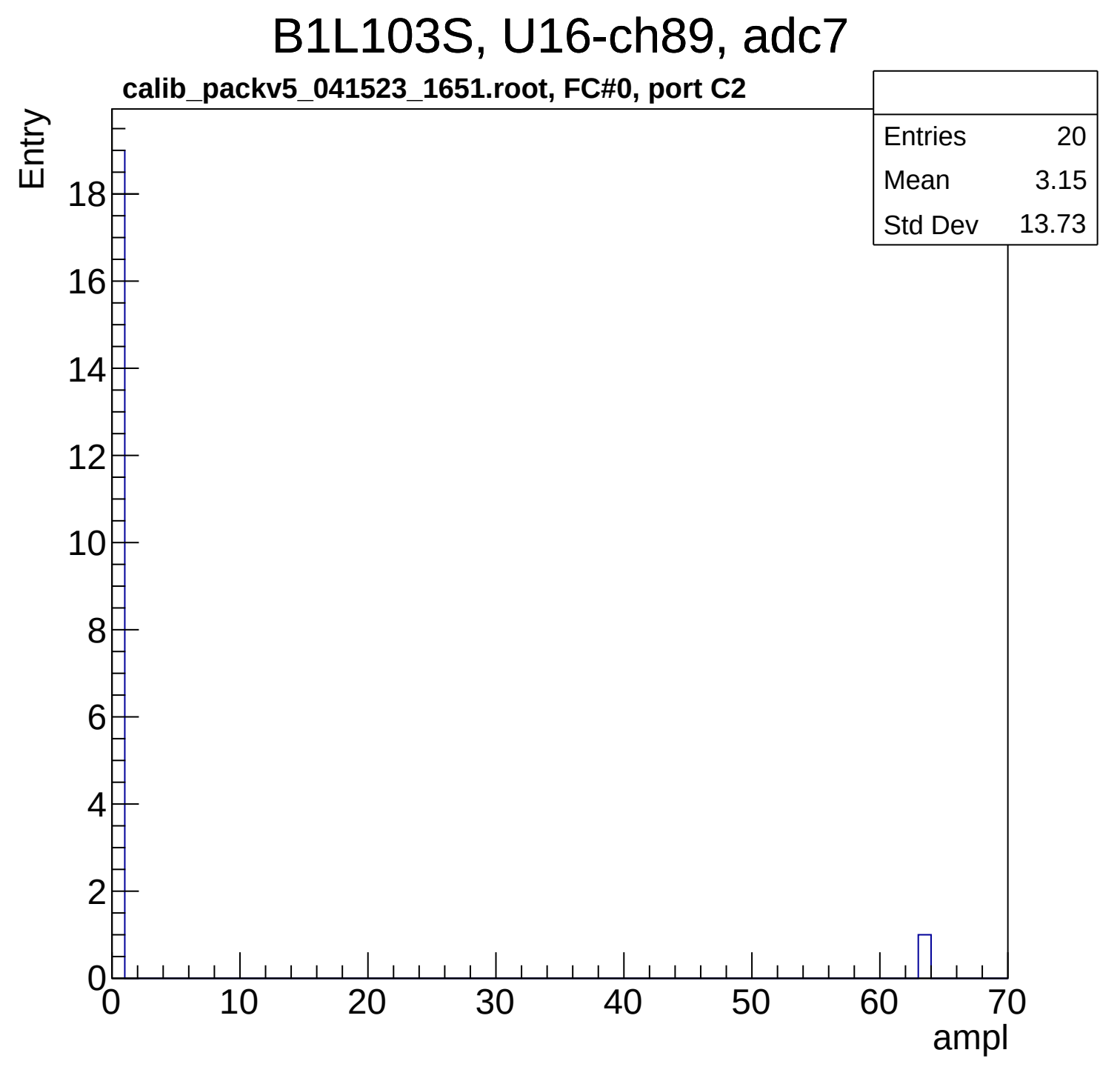
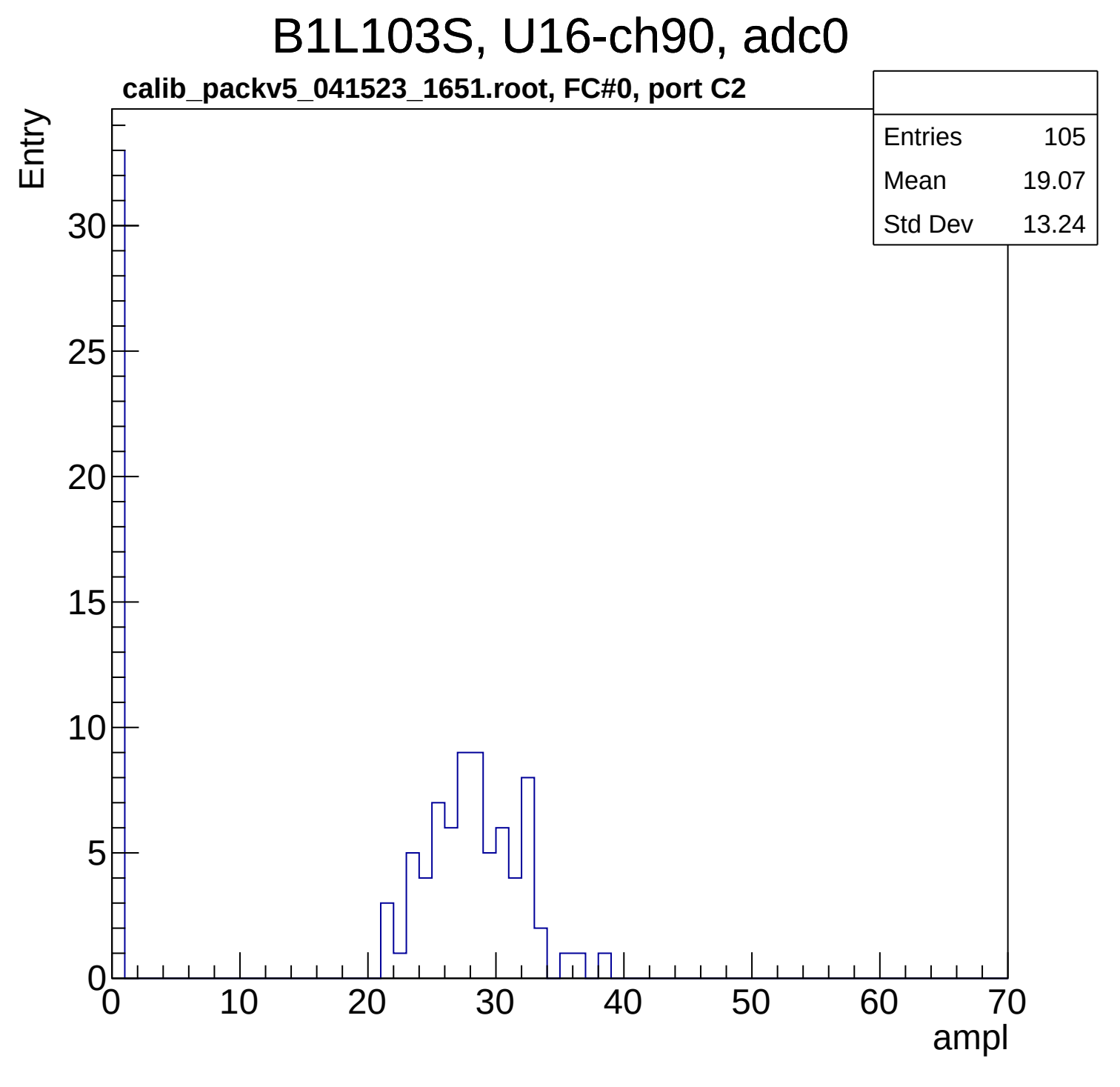
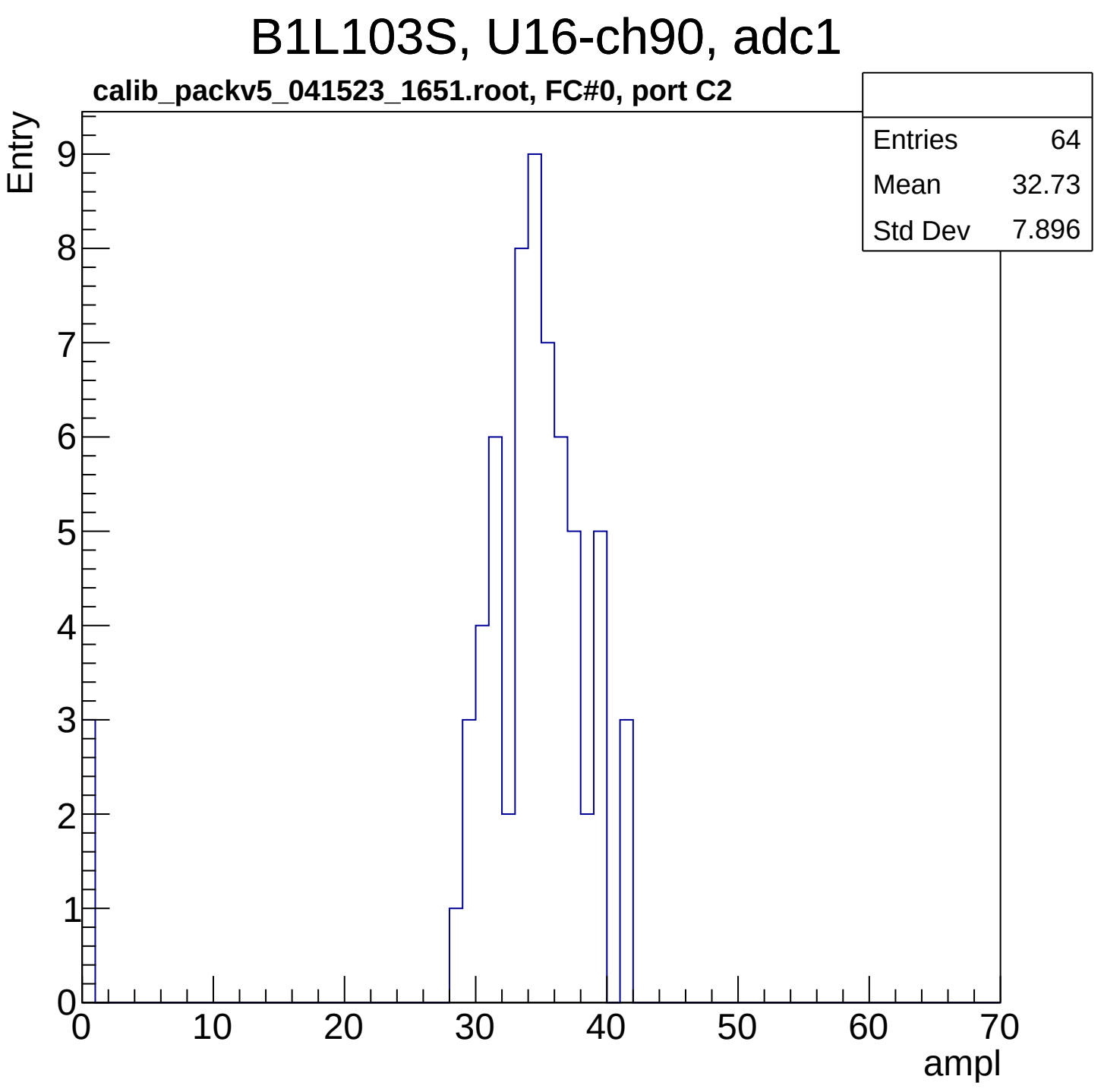
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U16-ch89, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch90, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 105
Mean 19.07
Std Dev 13.24
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch90, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 32.73
Std Dev 7.896
Entry
ampl
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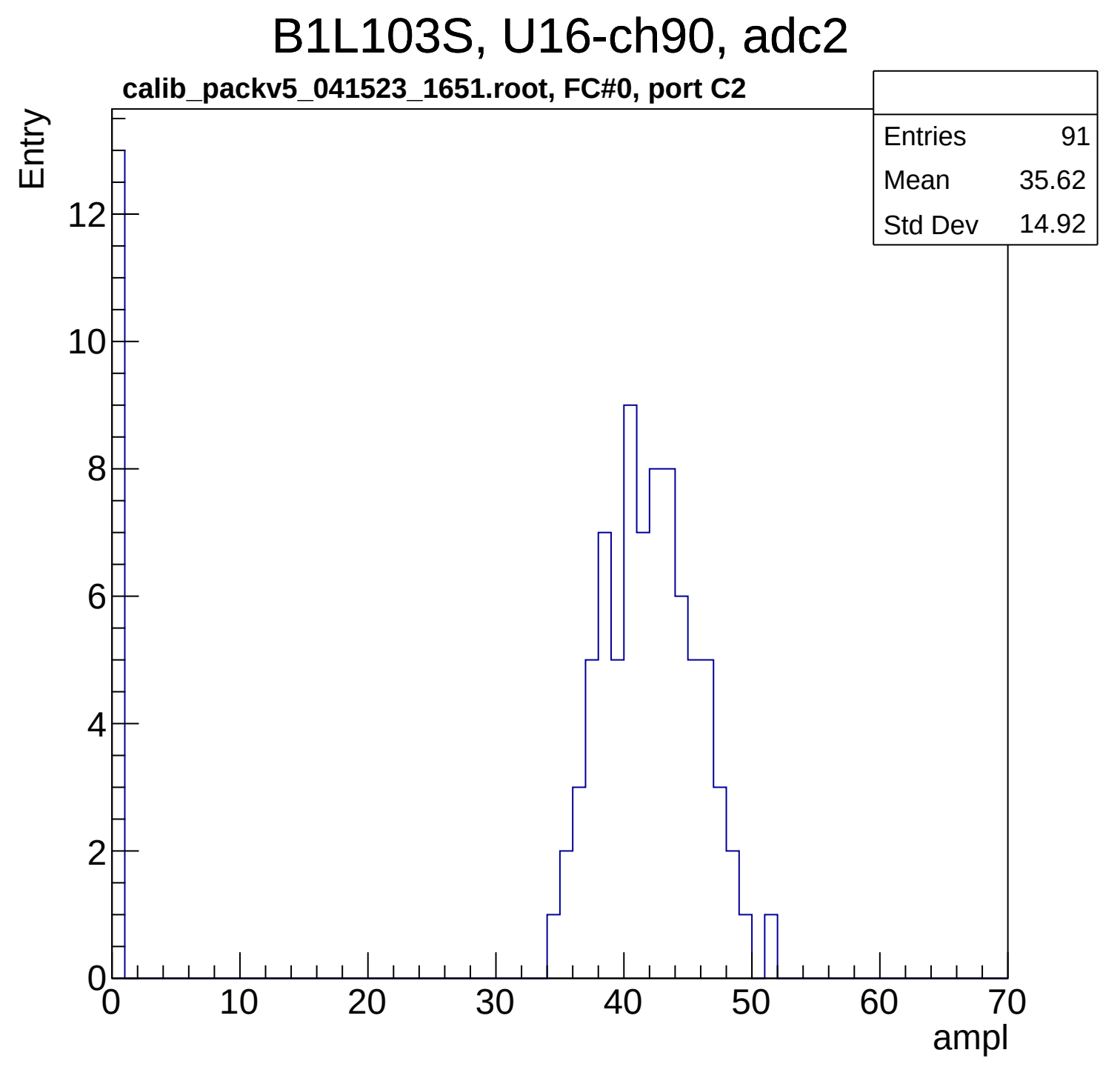
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch90, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 35.62
Std Dev 14.92
Entry
0
2
4
6
8
10
12
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10
20
30
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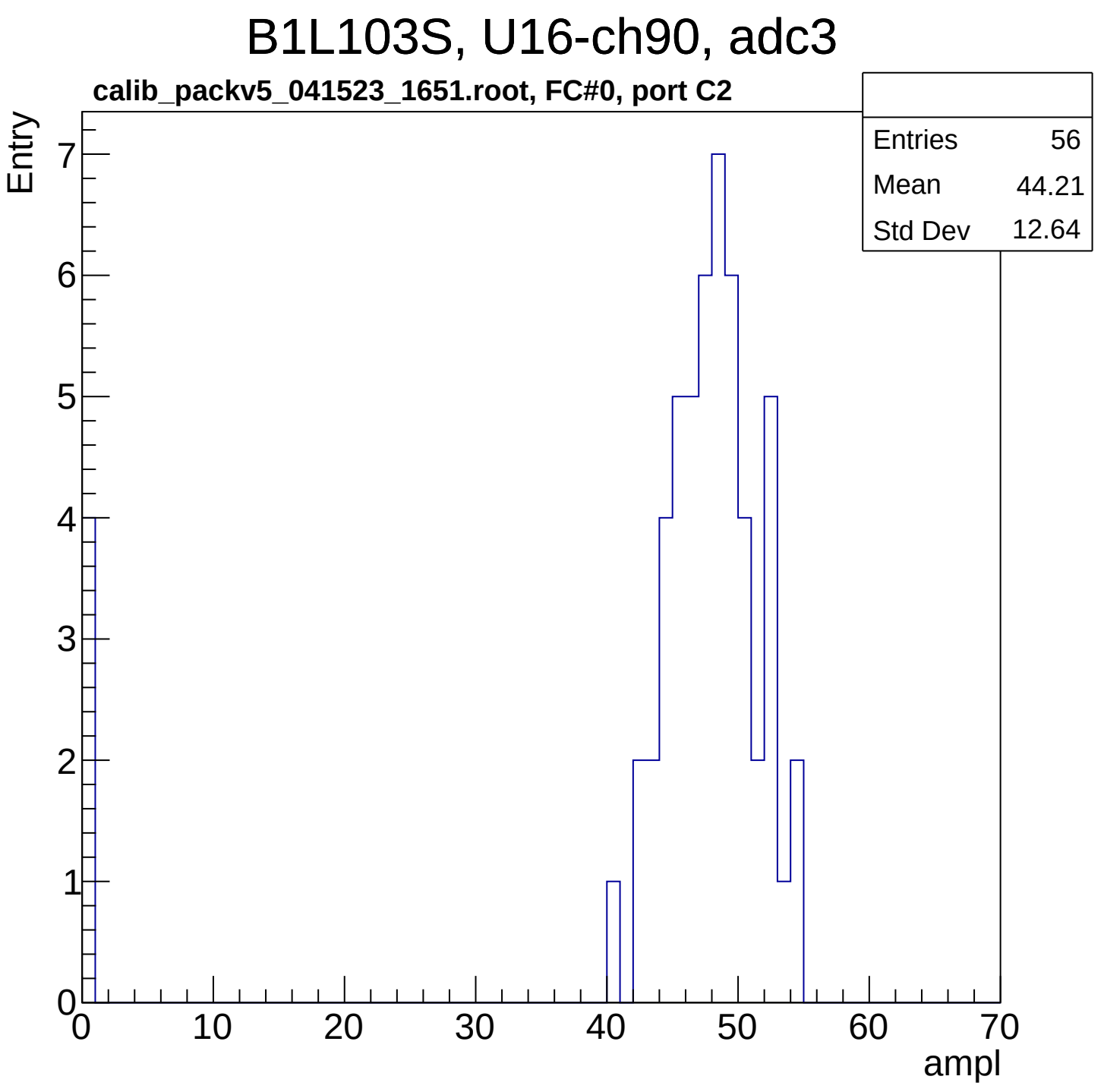
50
60
70
ampl


B1L103S, U16-ch90, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 44.21
Std Dev 12.64
Entry
ampl
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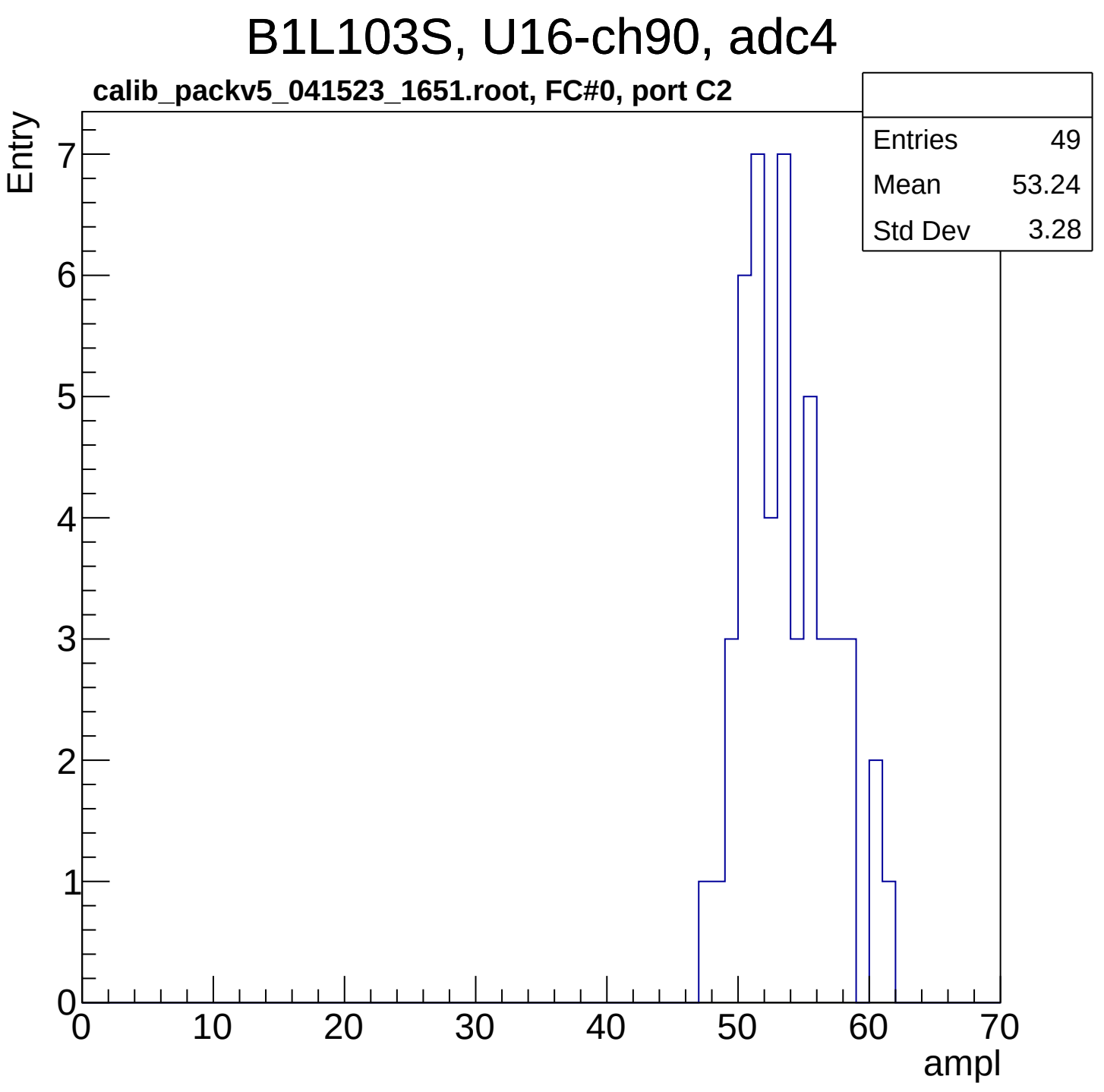
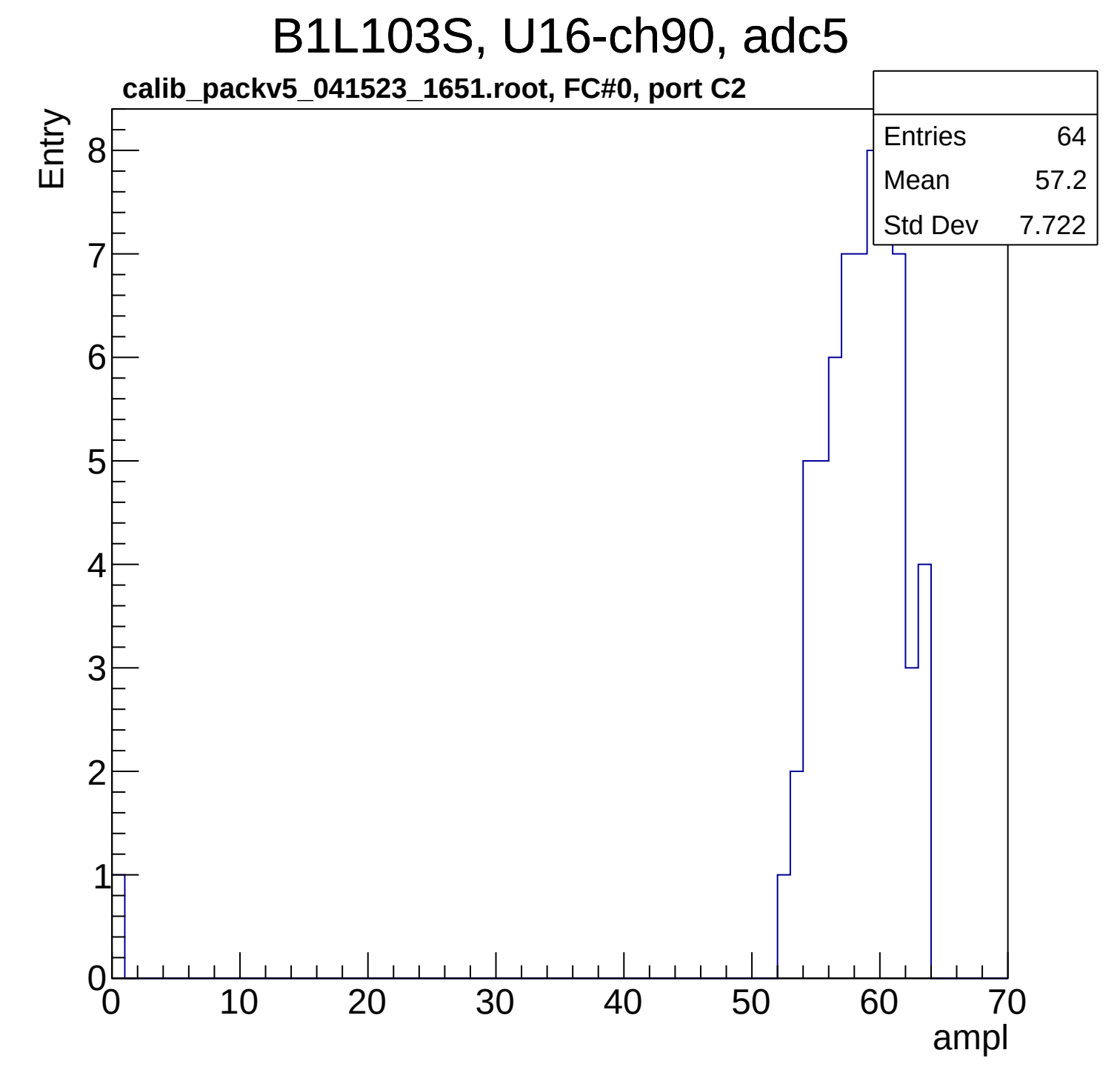
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch90, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 53.24
Std Dev 3.28
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch90, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 57.2
Std Dev 7.722
Entry
ampl
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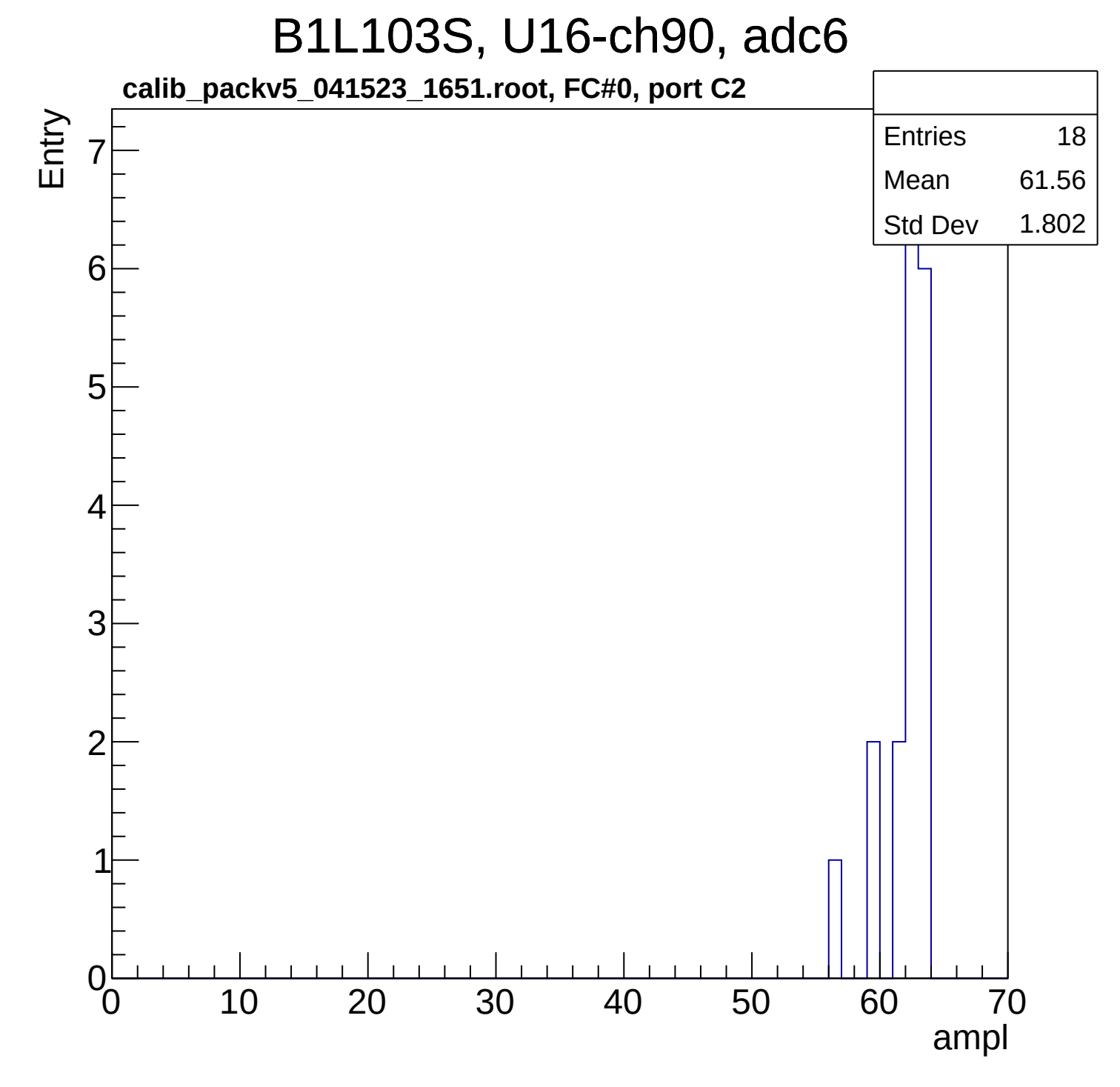
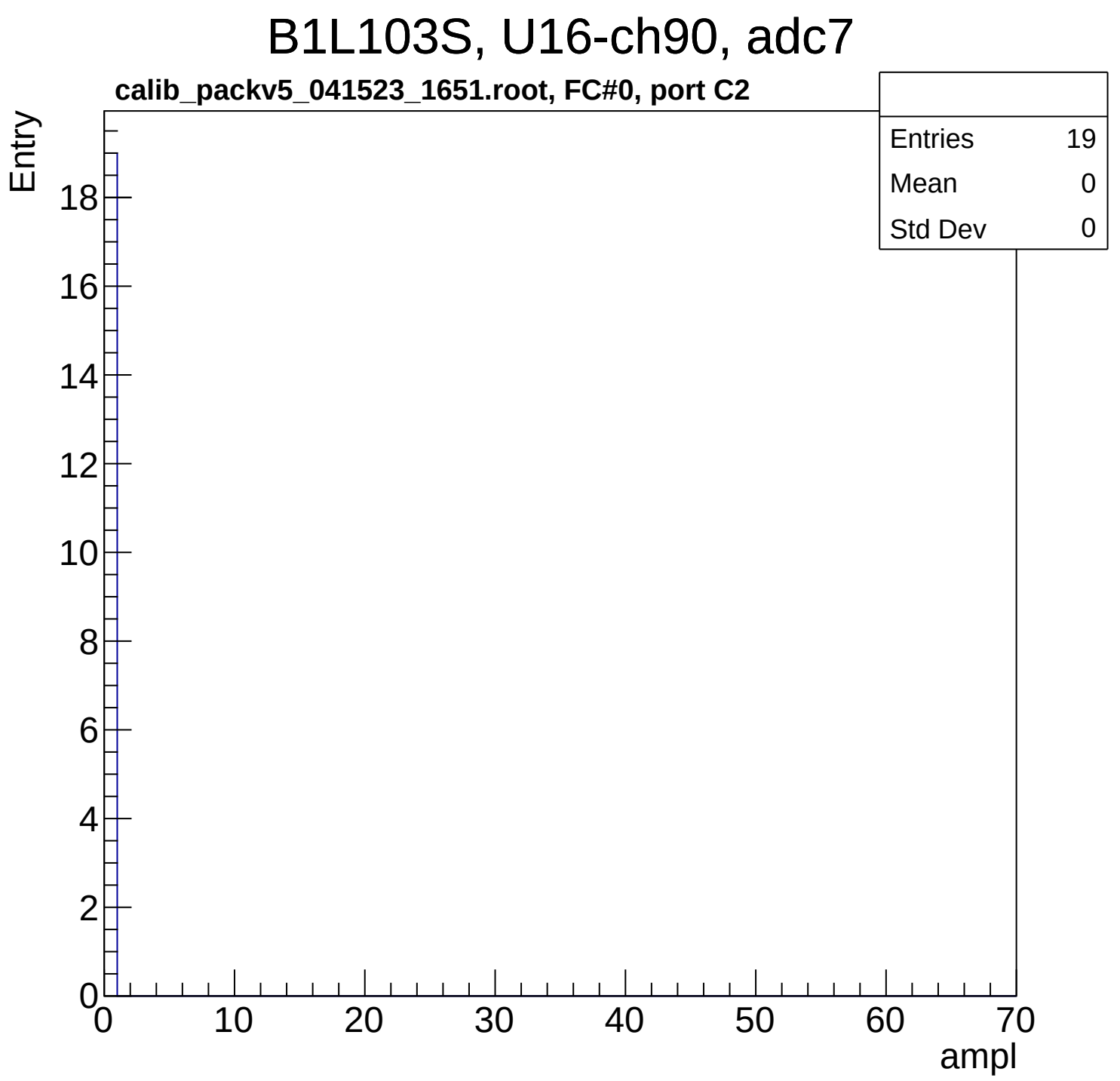
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch90, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 61.56
Std Dev 1.802
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch90, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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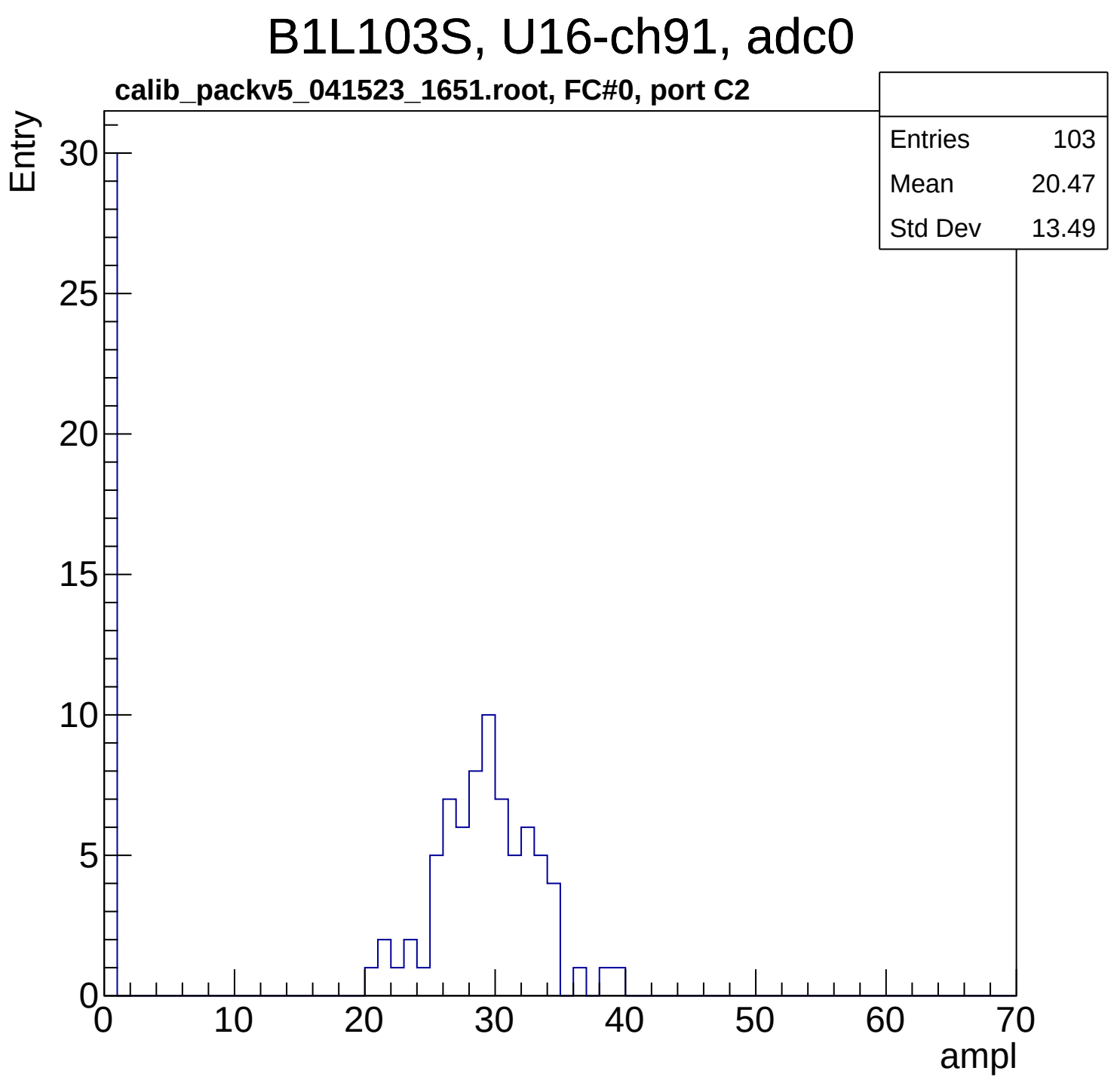
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch91, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 20.47
Std Dev 13.49
Entry
ampl
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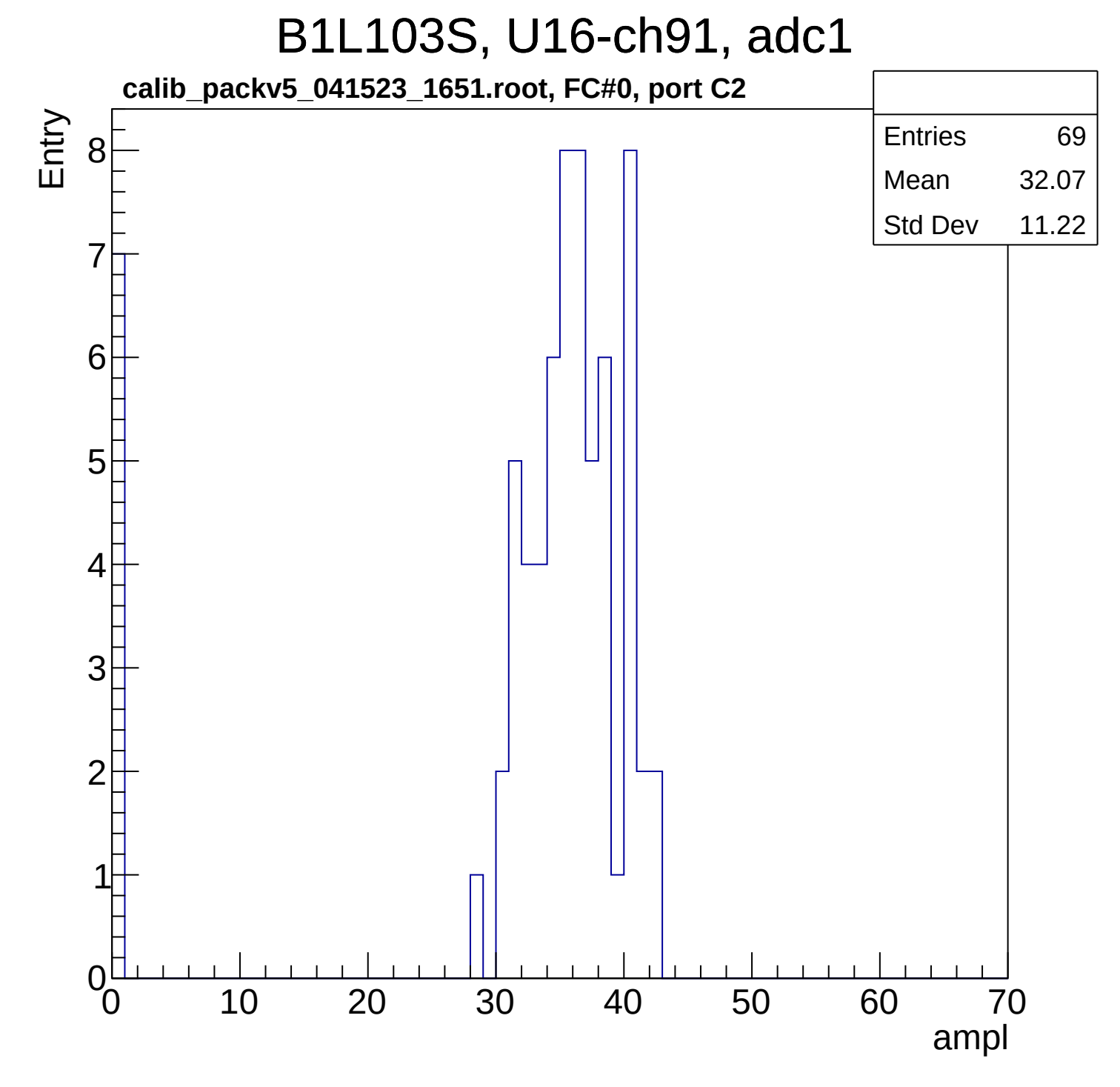
5
10
15
20
25
30
0
10
20
30
40
50
60
70


B1L103S, U16-ch91, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 32.07
Std Dev 11.22
Entry
ampl
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1
2
3
4
5
6
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8
0
10
20
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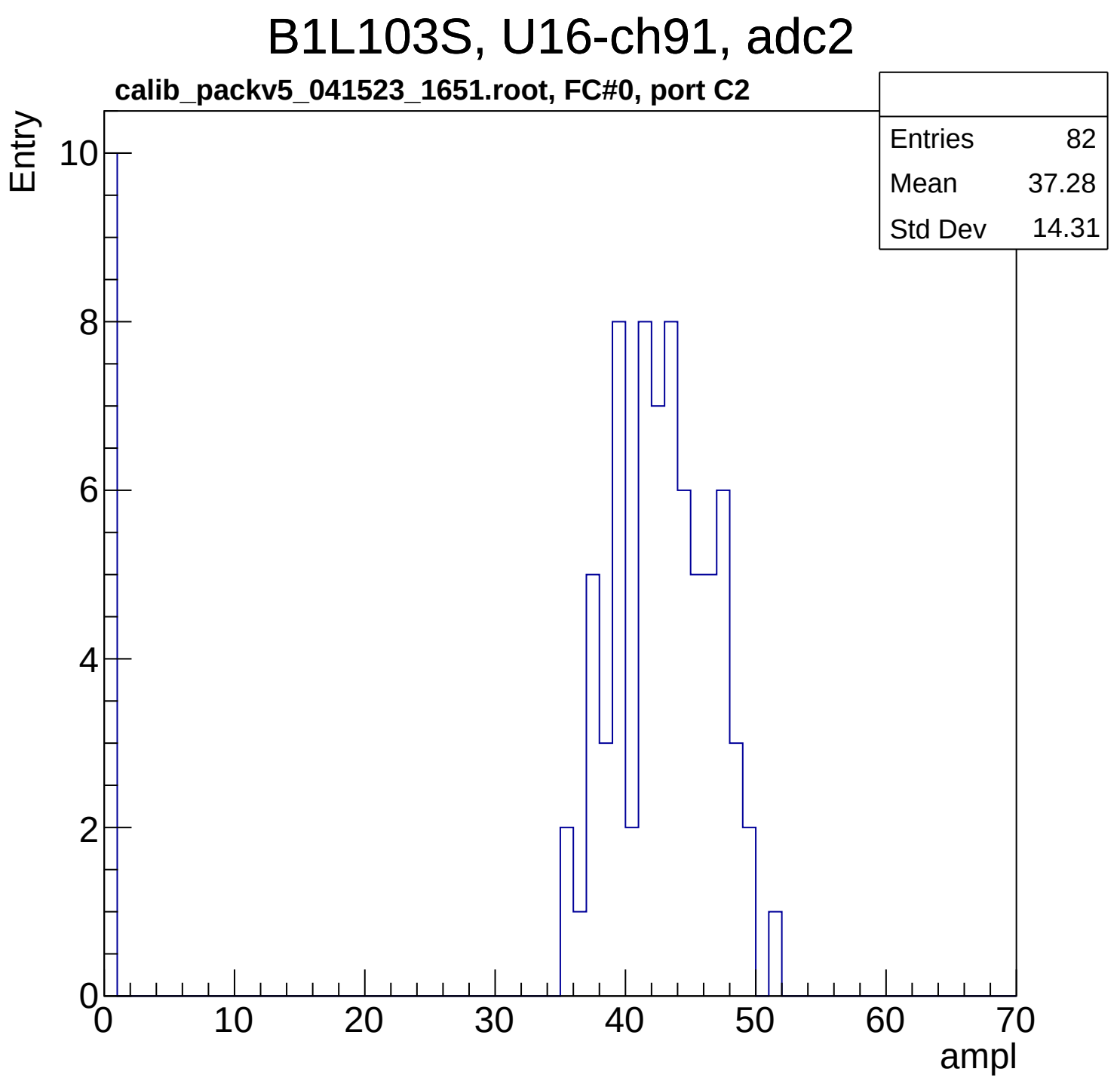
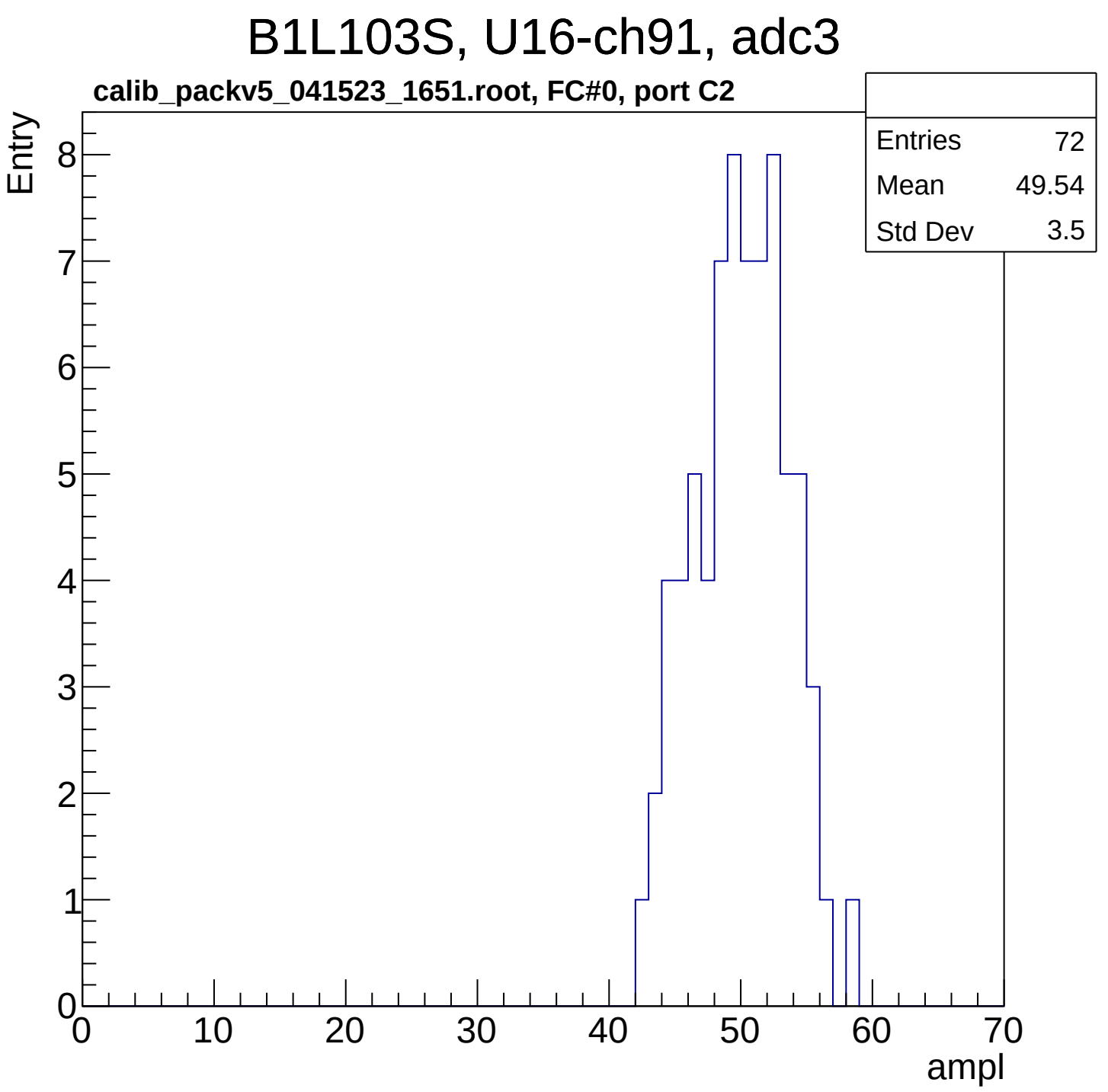
40
50
60
70


B1L103S, U16-ch91, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 37.28
Std Dev 14.31
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch91, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 49.54
Std Dev 3.5
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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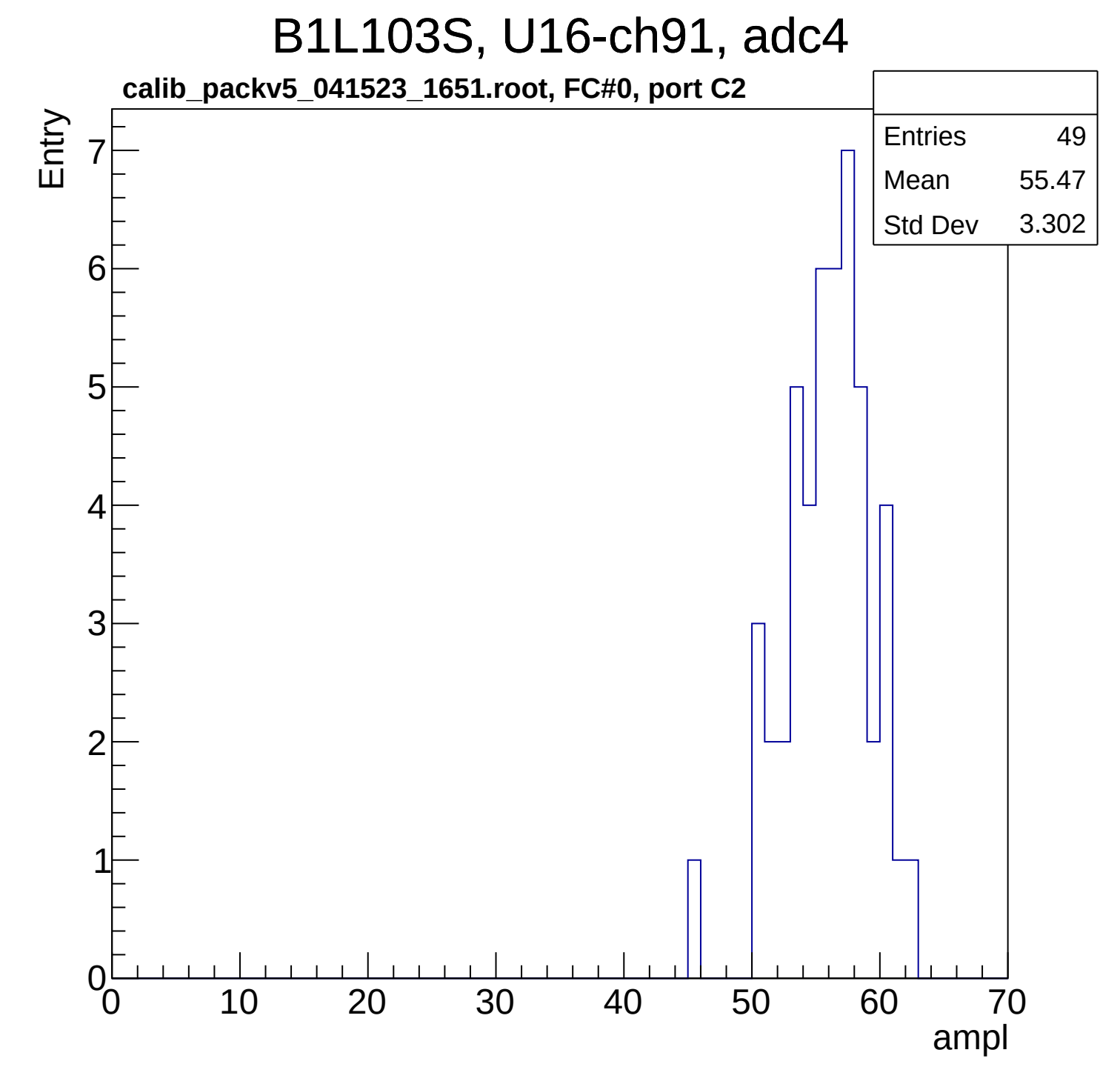
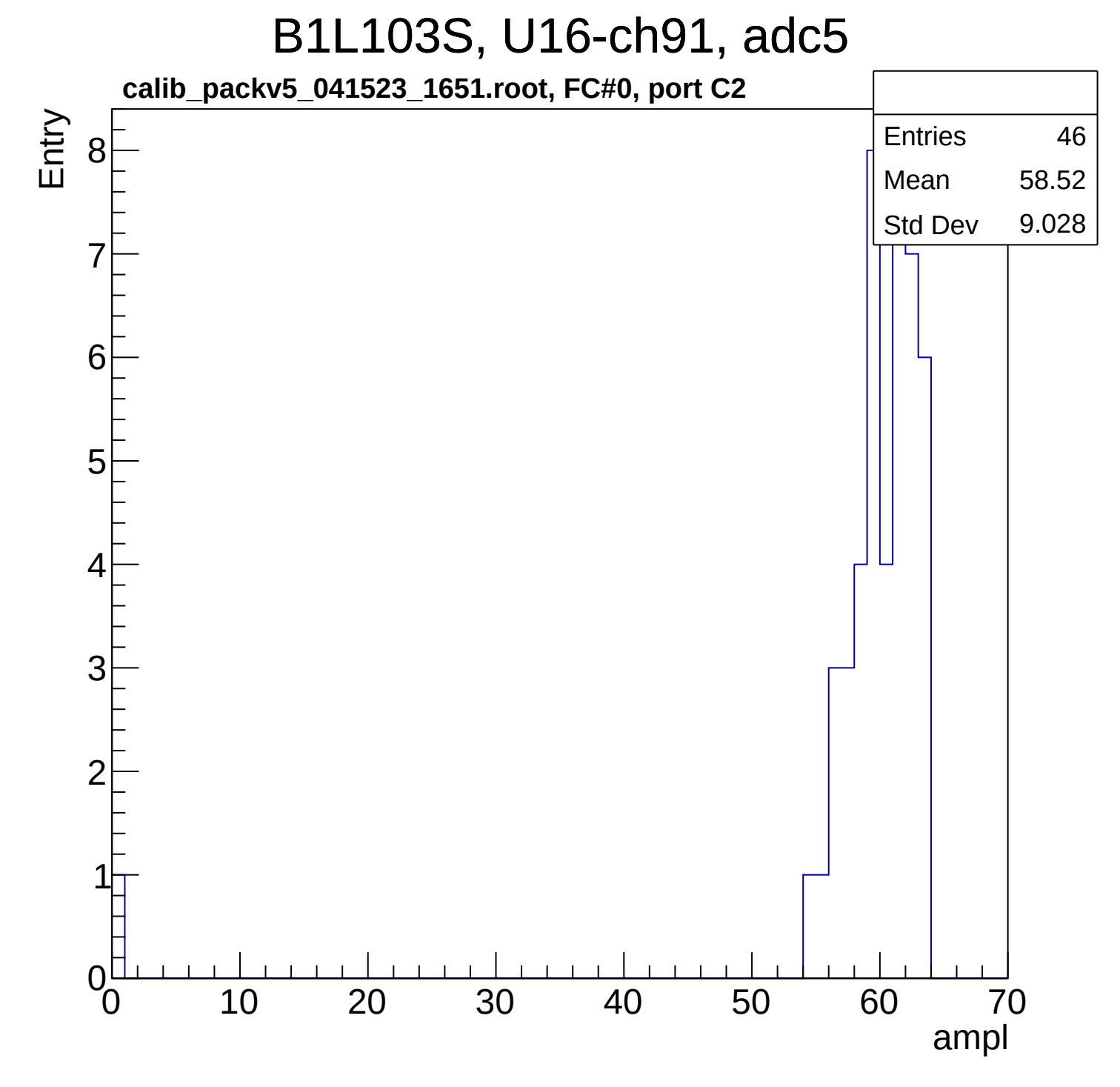
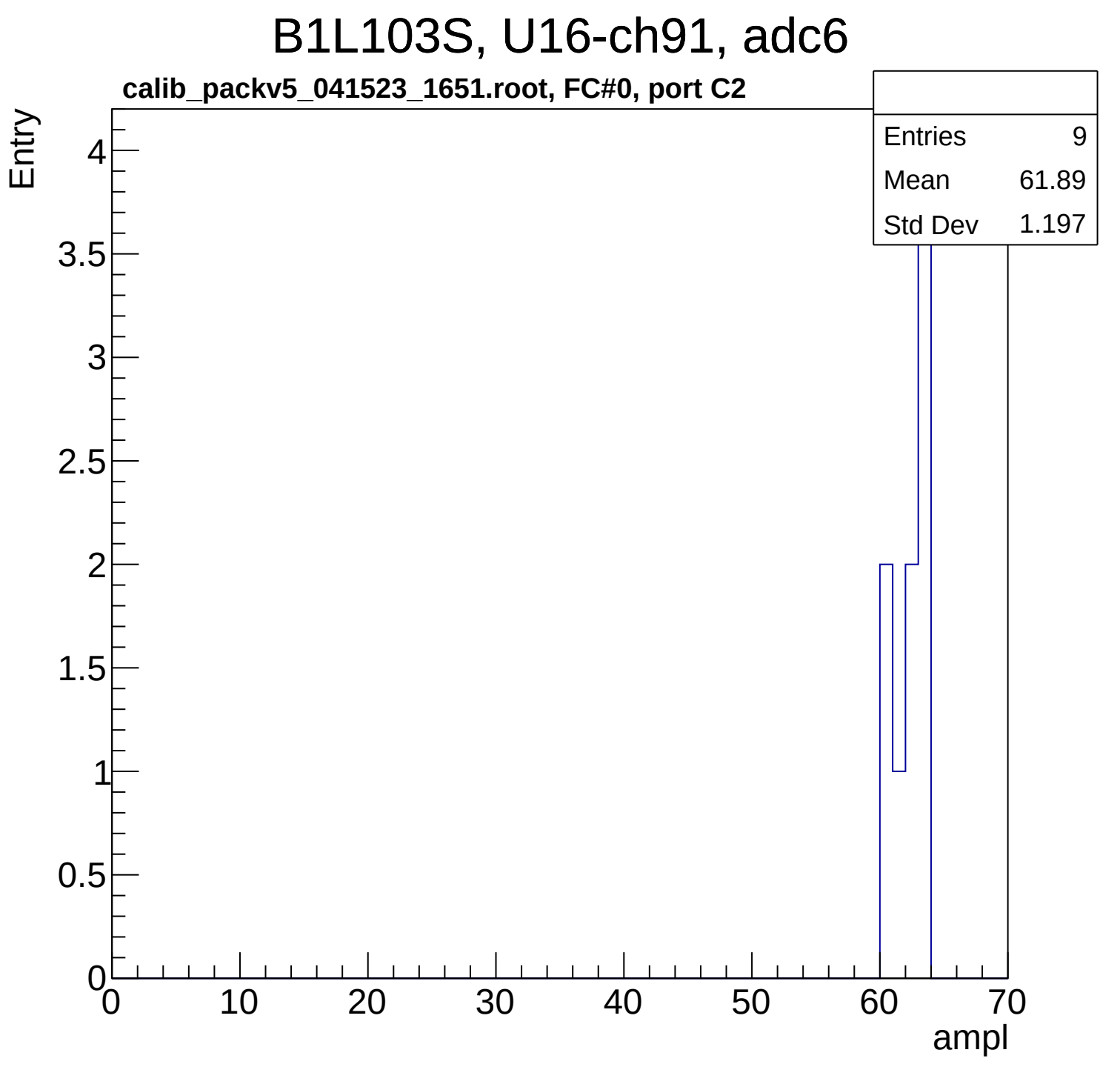

B1L103S, U16-ch91, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 55.47
Std Dev 3.302
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch91, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.52
Std Dev 9.028
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch91, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.89
Std Dev 1.197
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
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20
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40
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60
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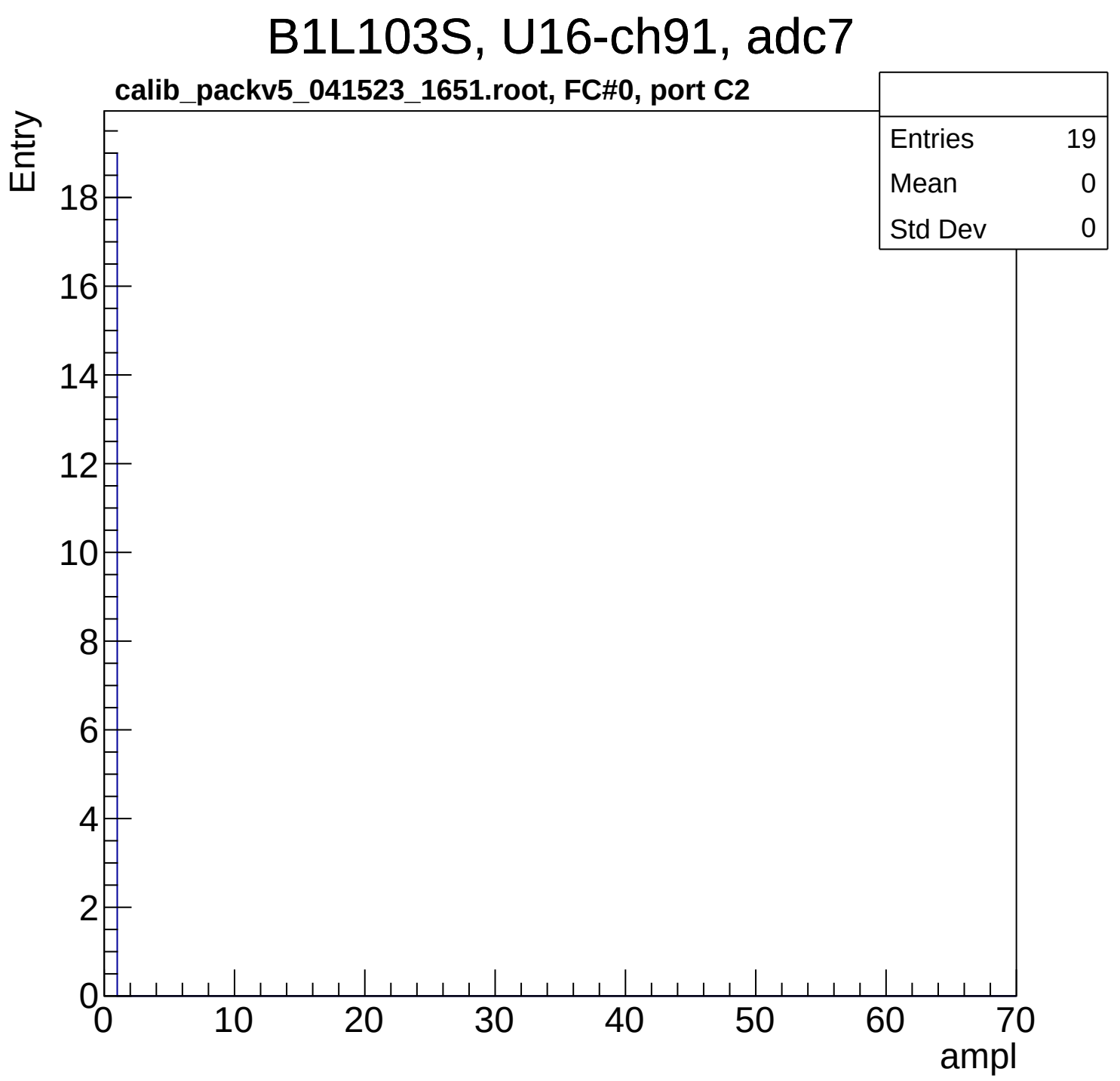
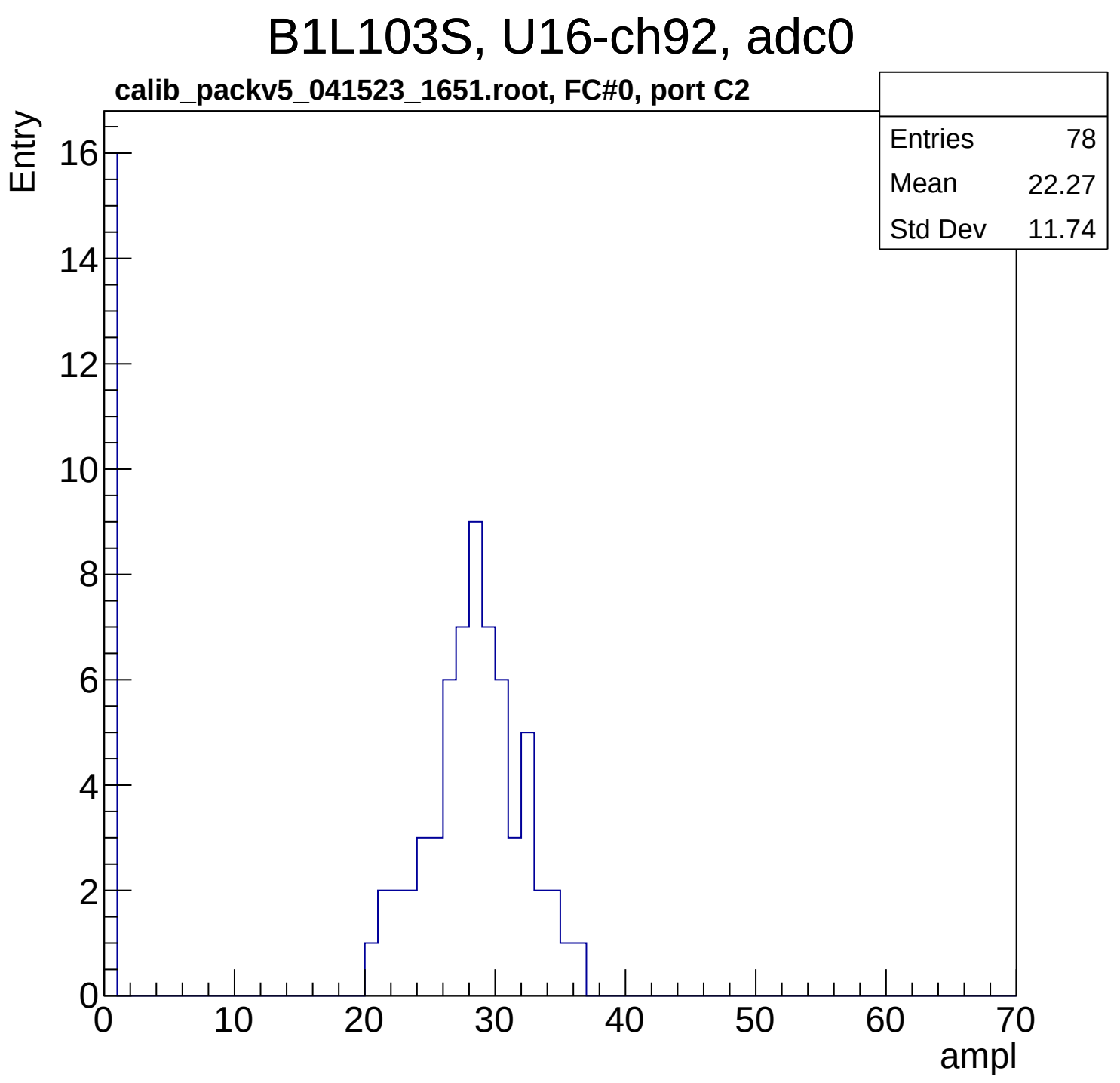

B1L103S, U16-ch91, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch92, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 22.27
Std Dev 11.74
Entry
0
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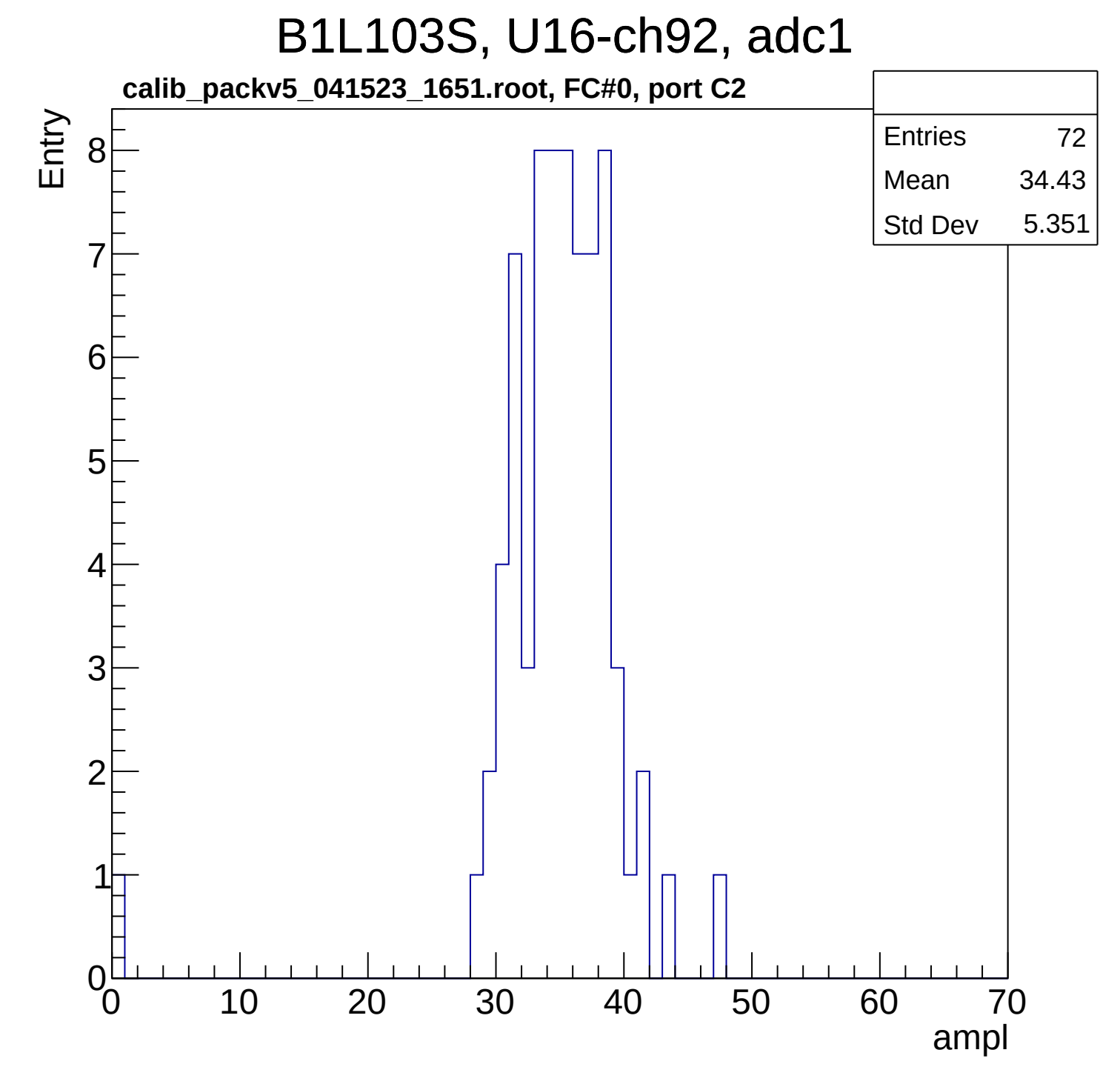
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch92, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 34.43
Std Dev 5.351
Entry
ampl
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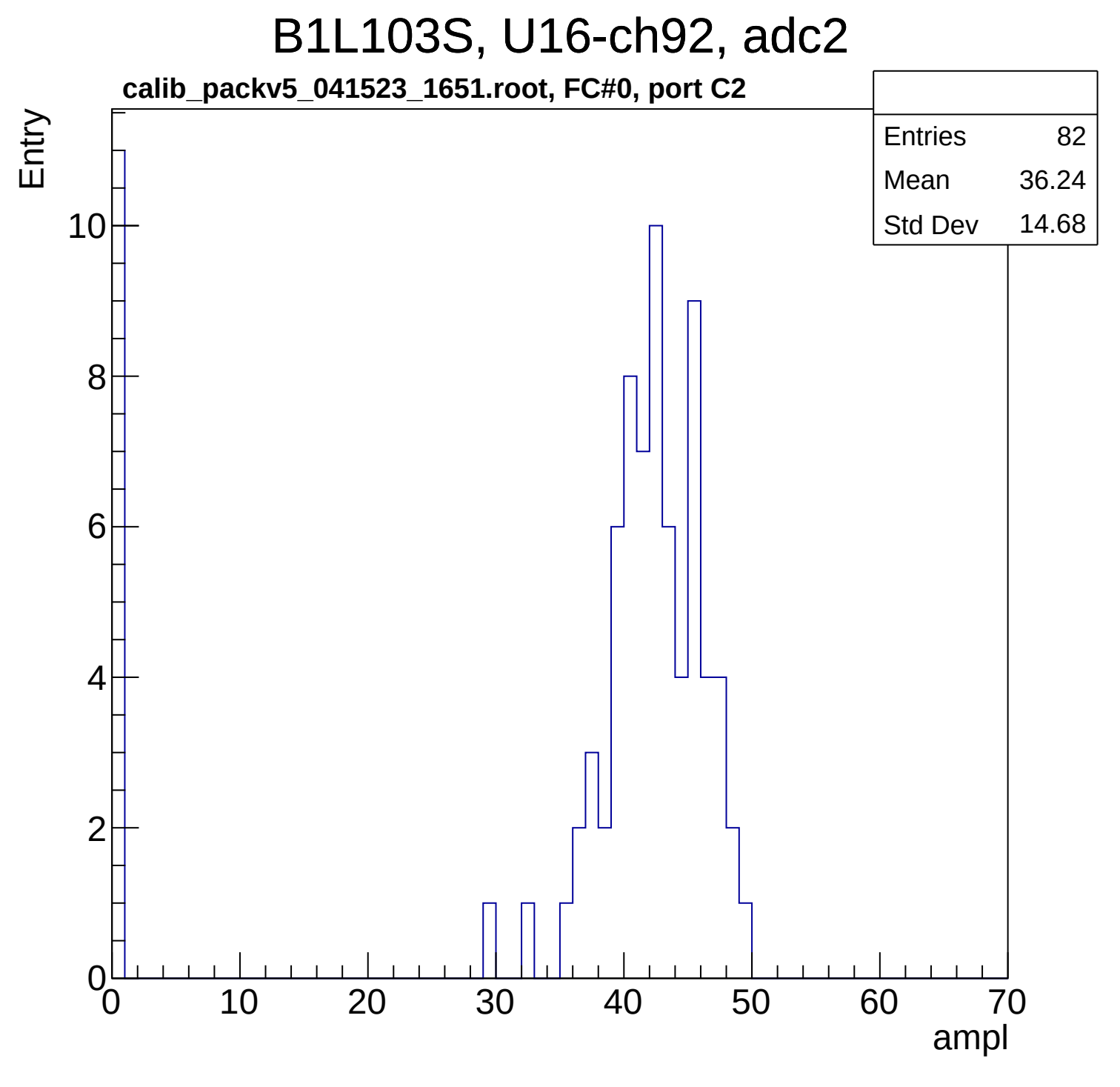
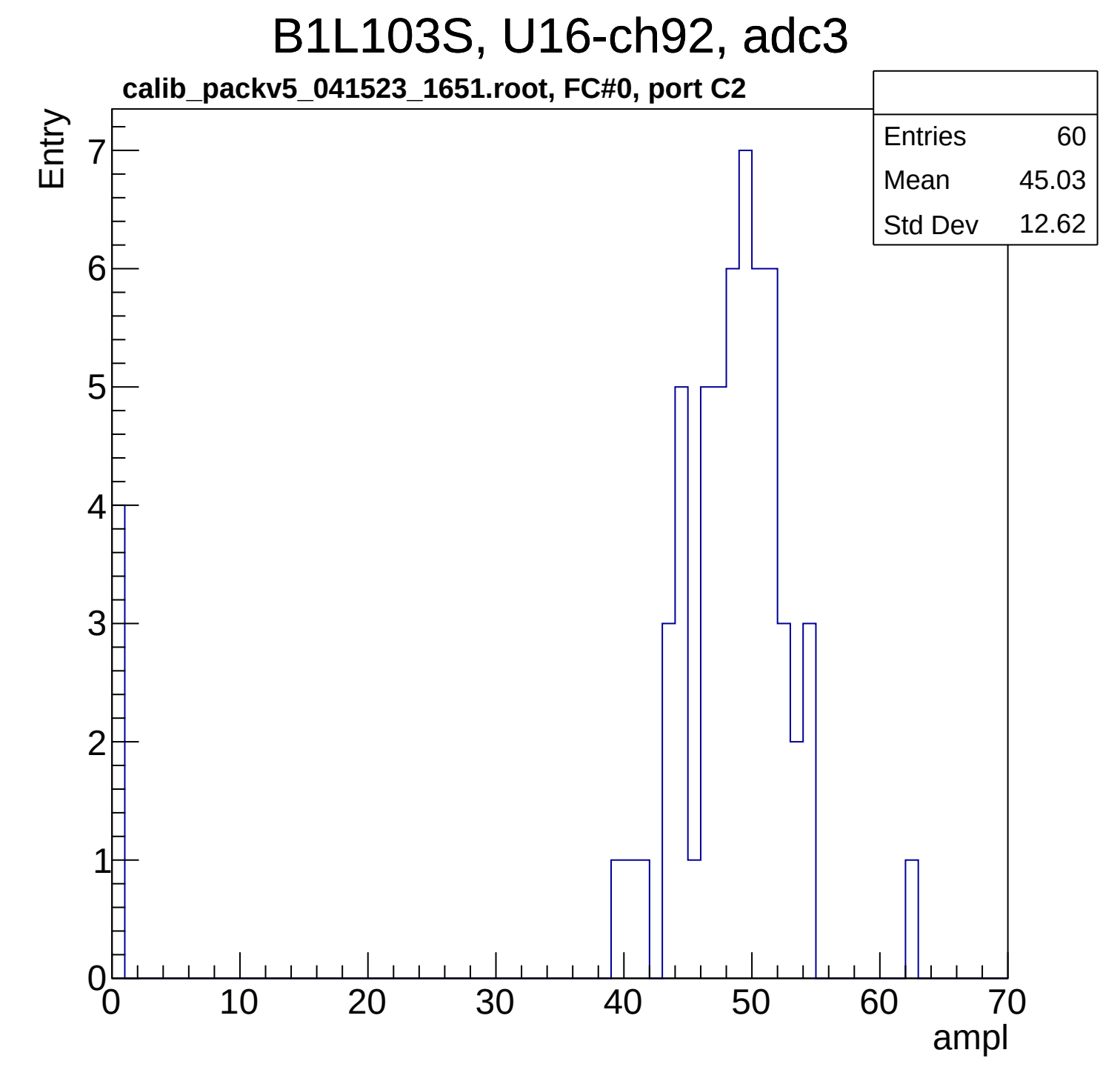
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch92, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 36.24
Std Dev 14.68
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch92, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 45.03
Std Dev 12.62
Entry
ampl
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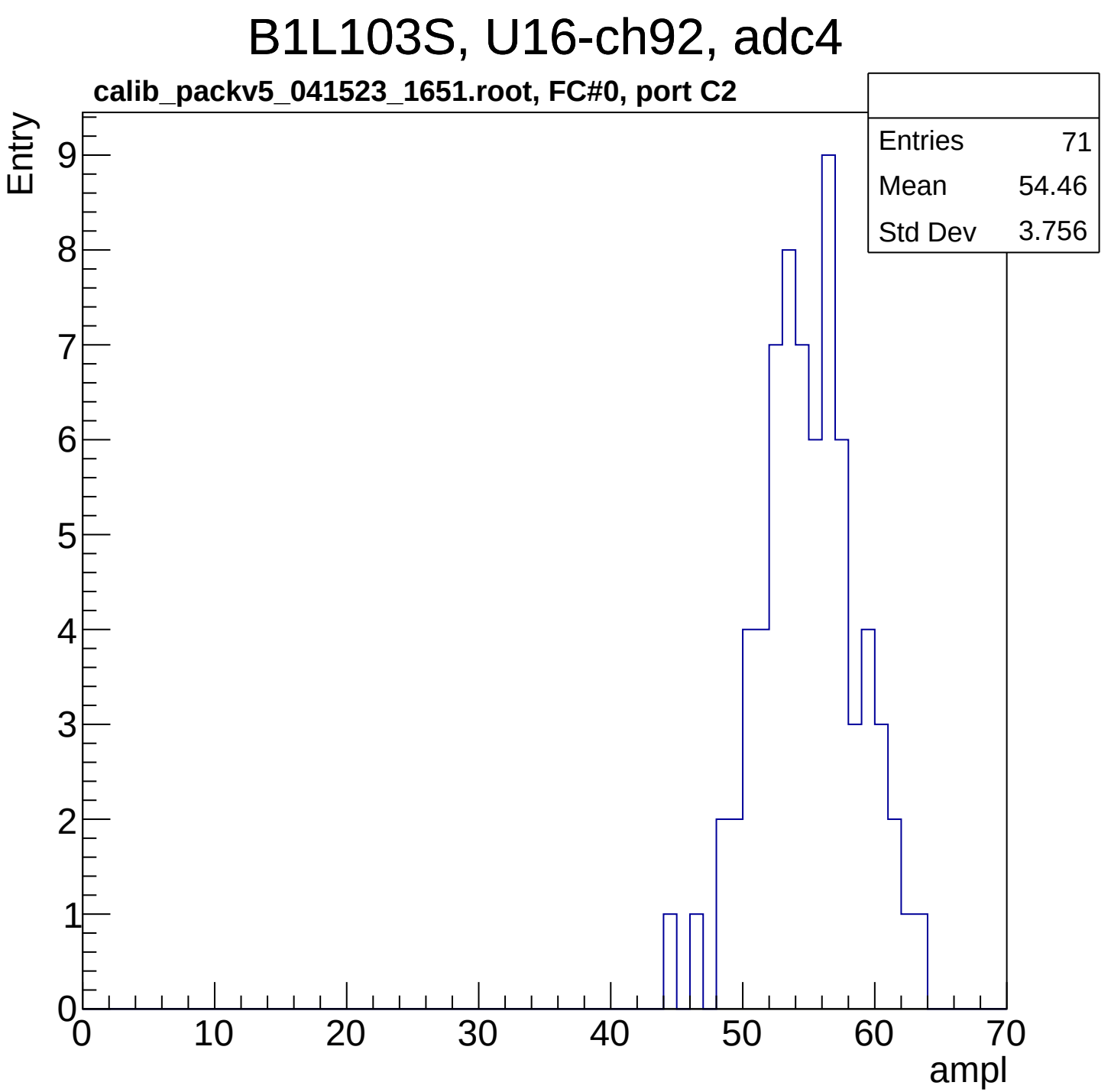
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch92, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 54.46
Std Dev 3.756
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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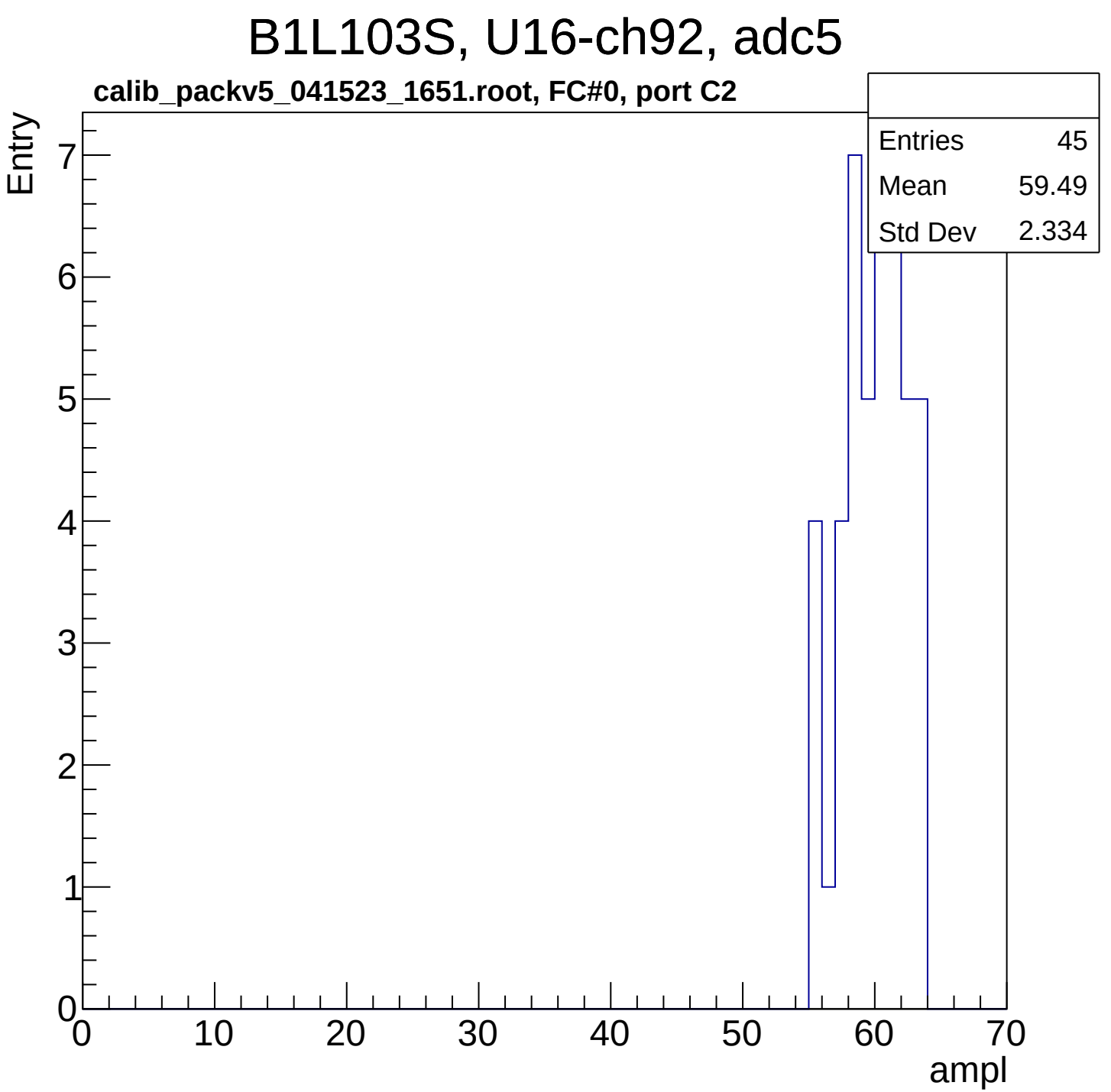
B1L103S, U16-ch92, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 59.49
Std Dev 2.334
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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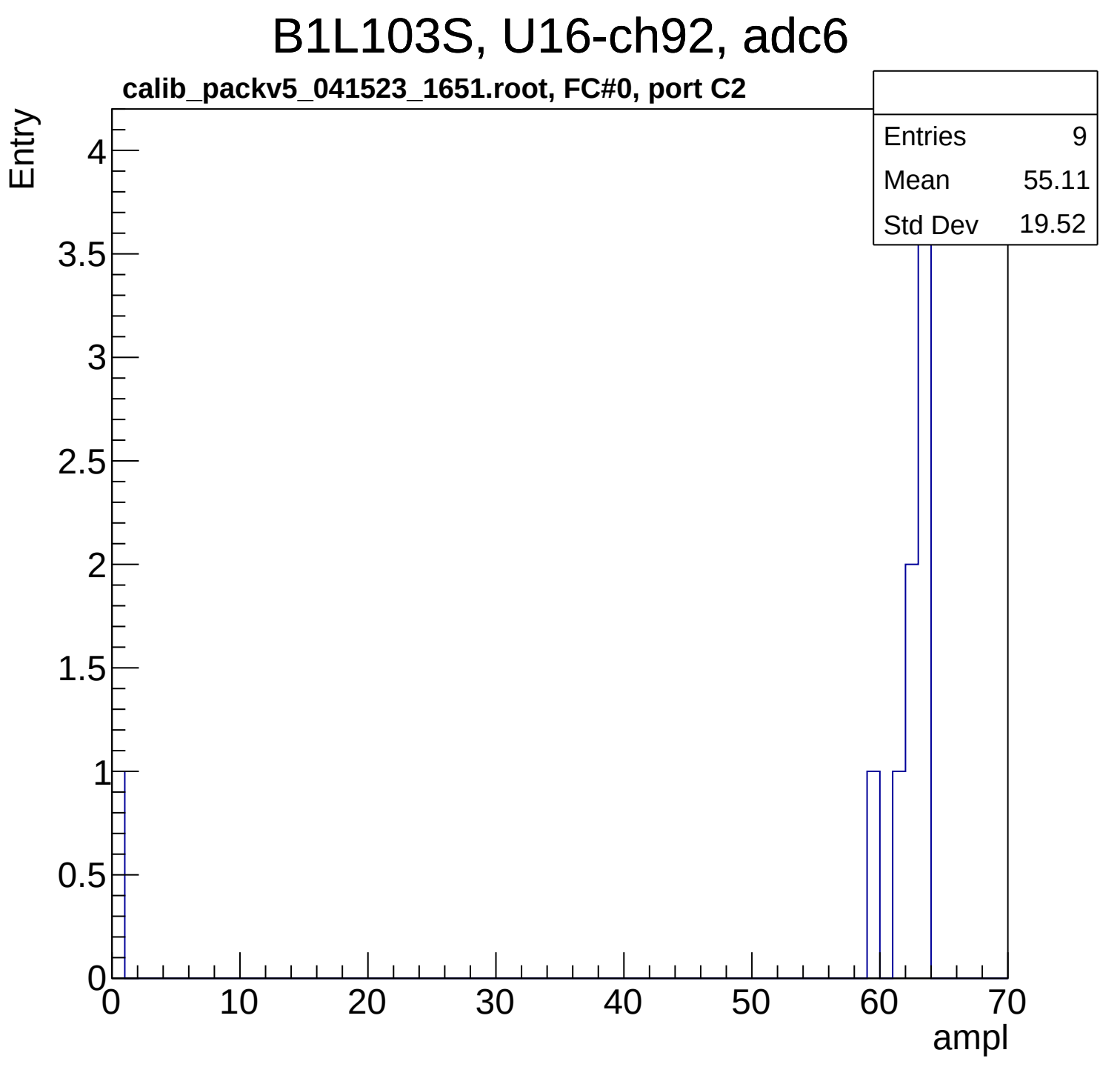
B1L103S, U16-ch92, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 55.11
Std Dev 19.52
Entry
ampl
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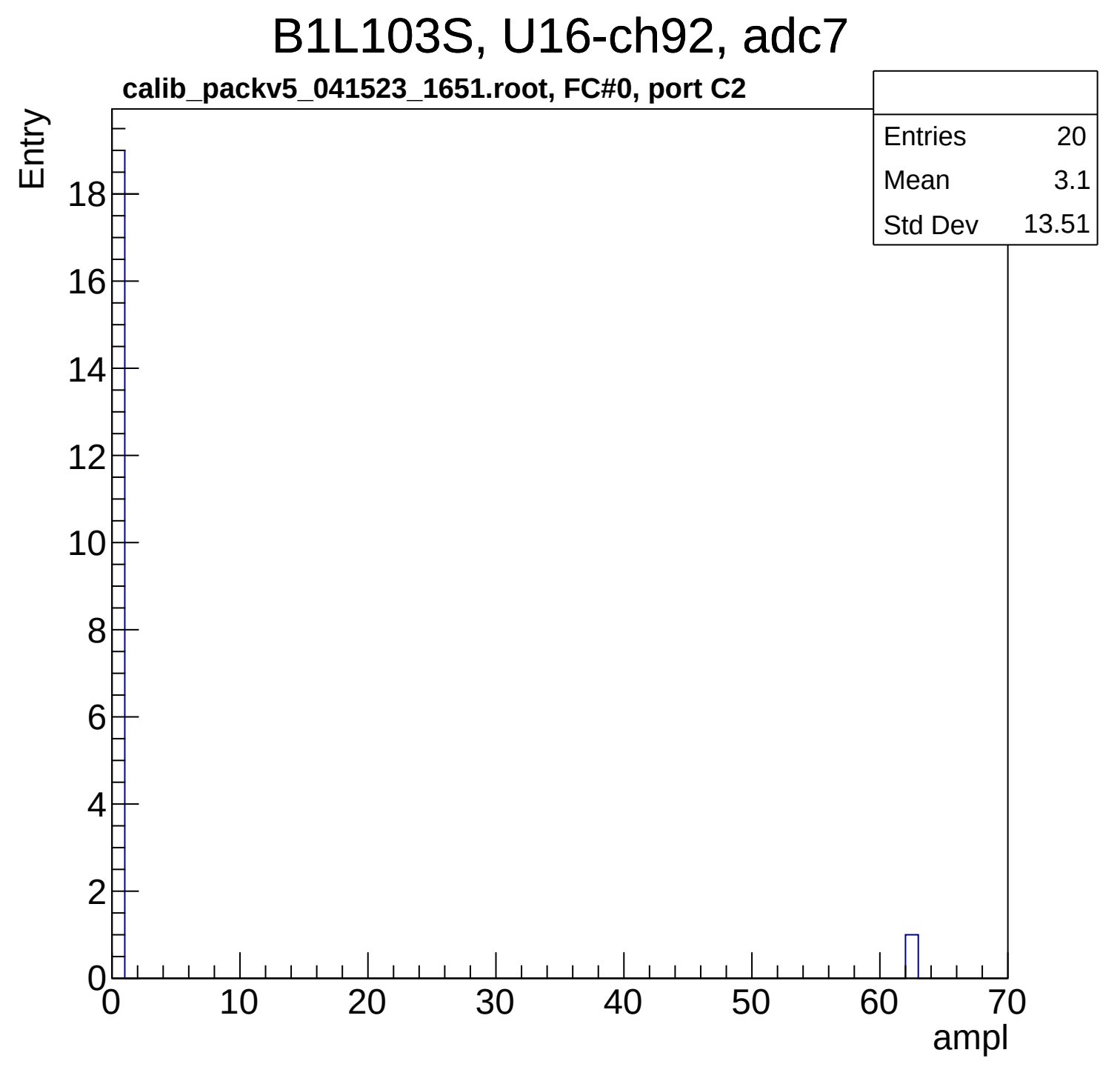
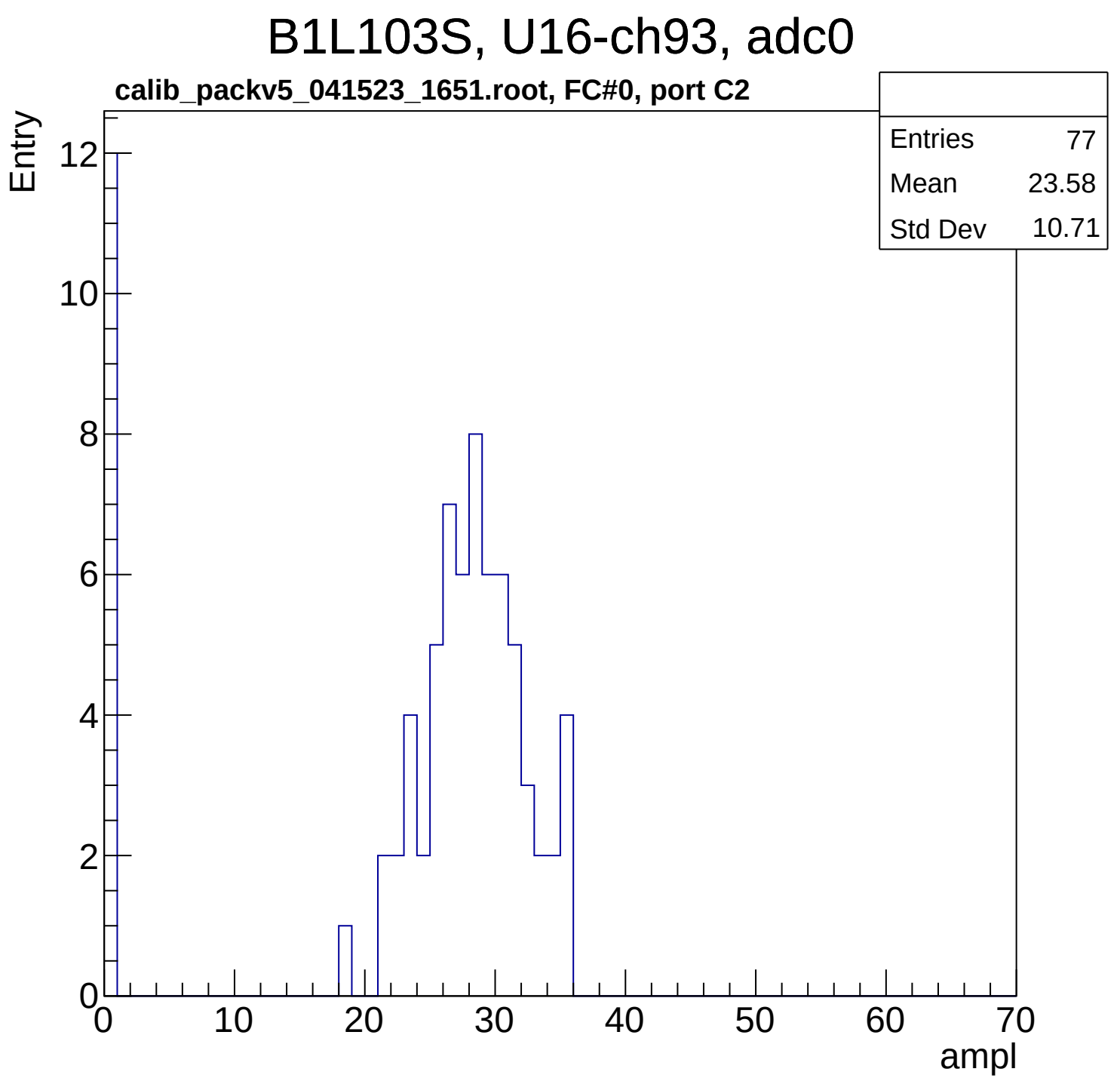
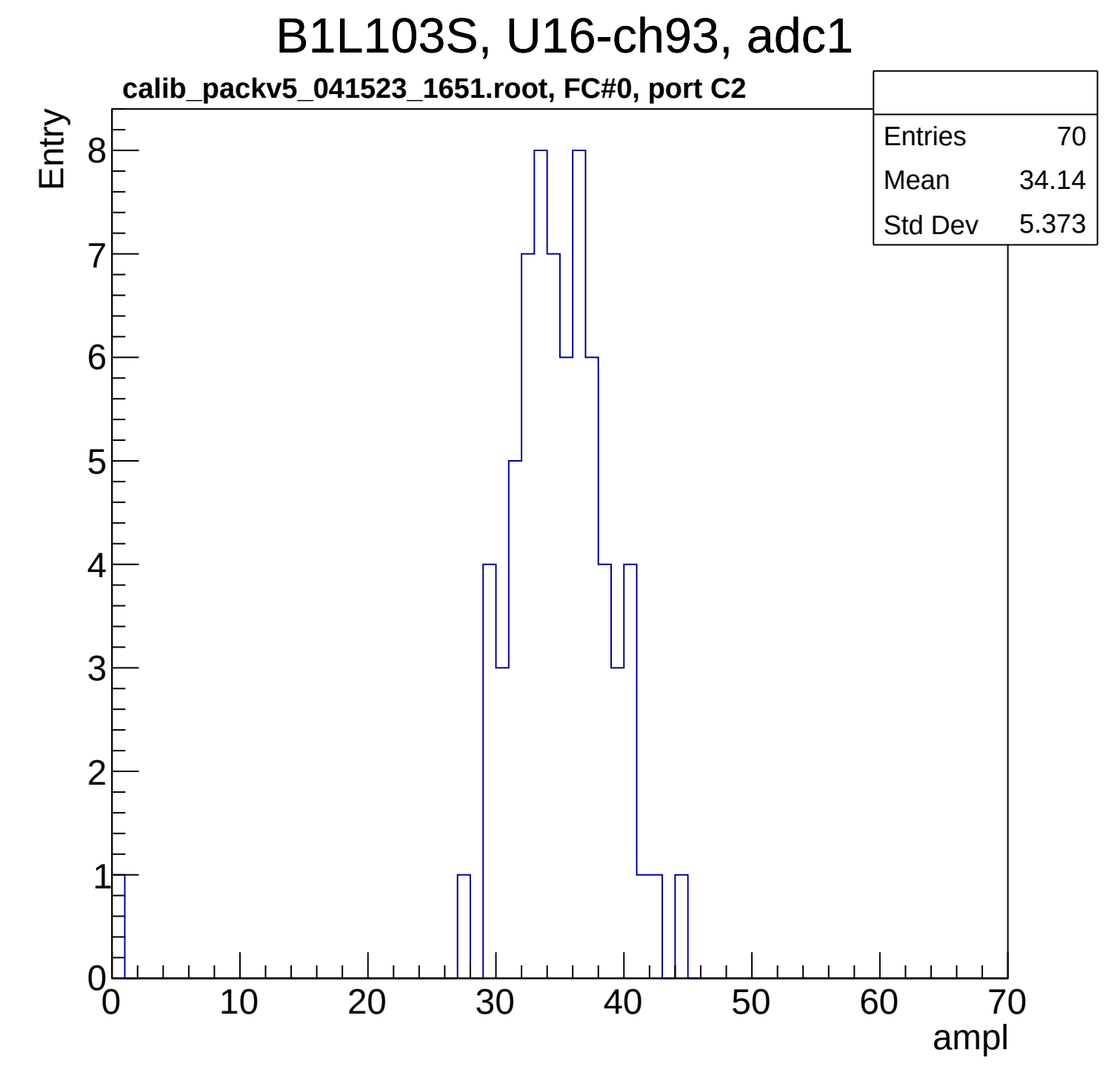
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U16-ch92, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch93, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 23.58
Std Dev 10.71
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch93, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 34.14
Std Dev 5.373
Entry
ampl
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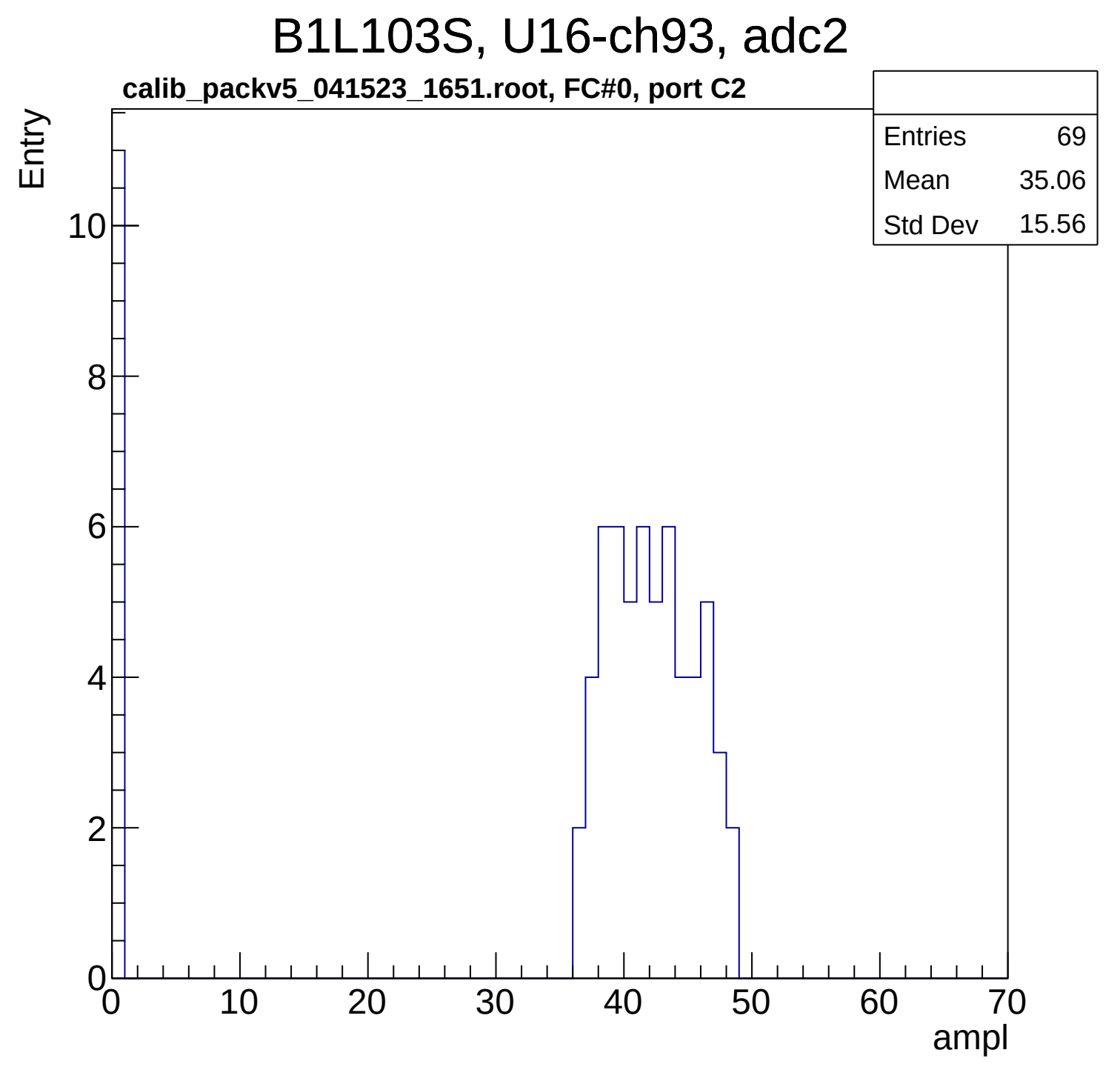
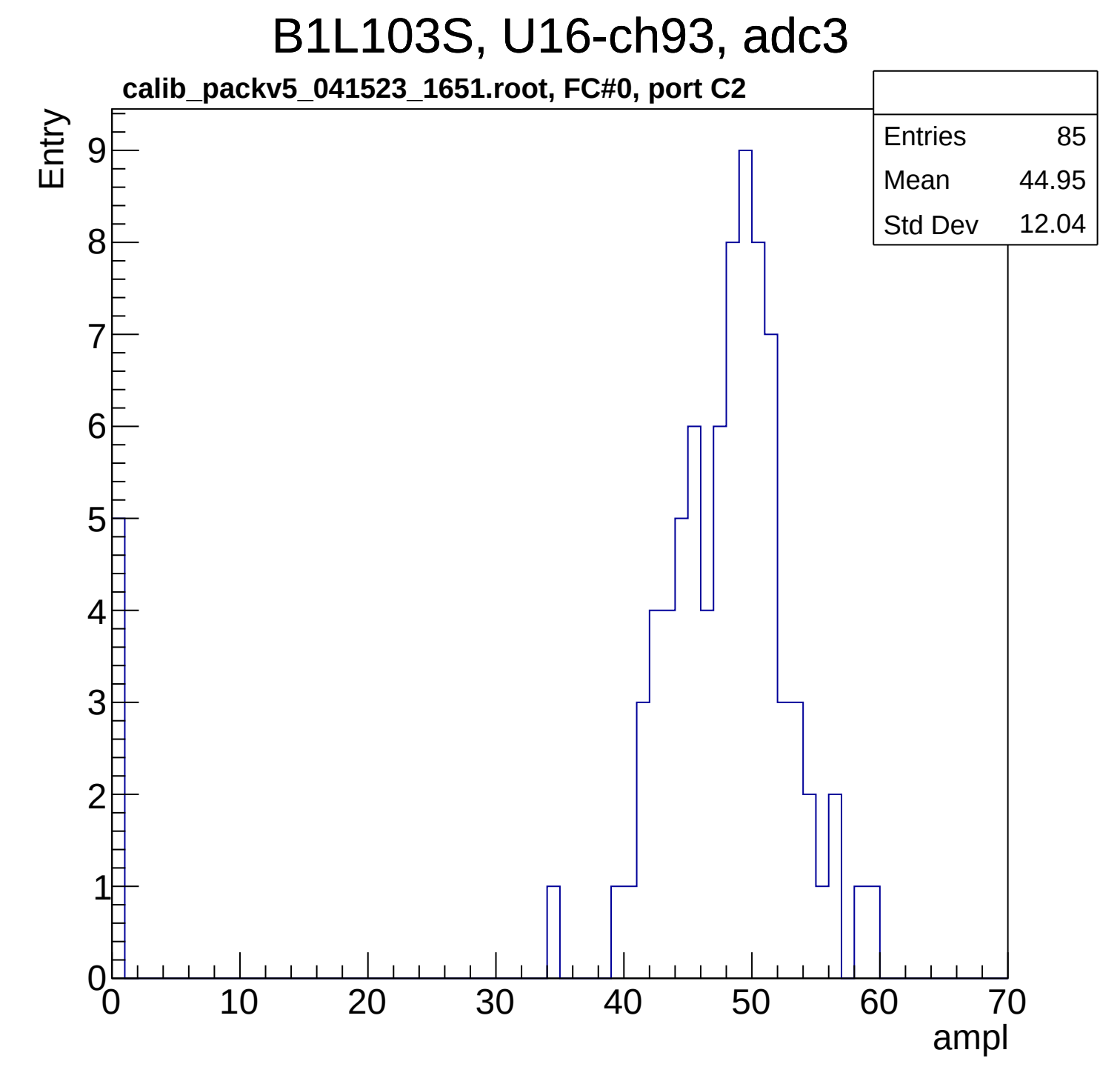
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch93, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 35.06
Std Dev 15.56
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch93, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 44.95
Std Dev 12.04
Entry
ampl
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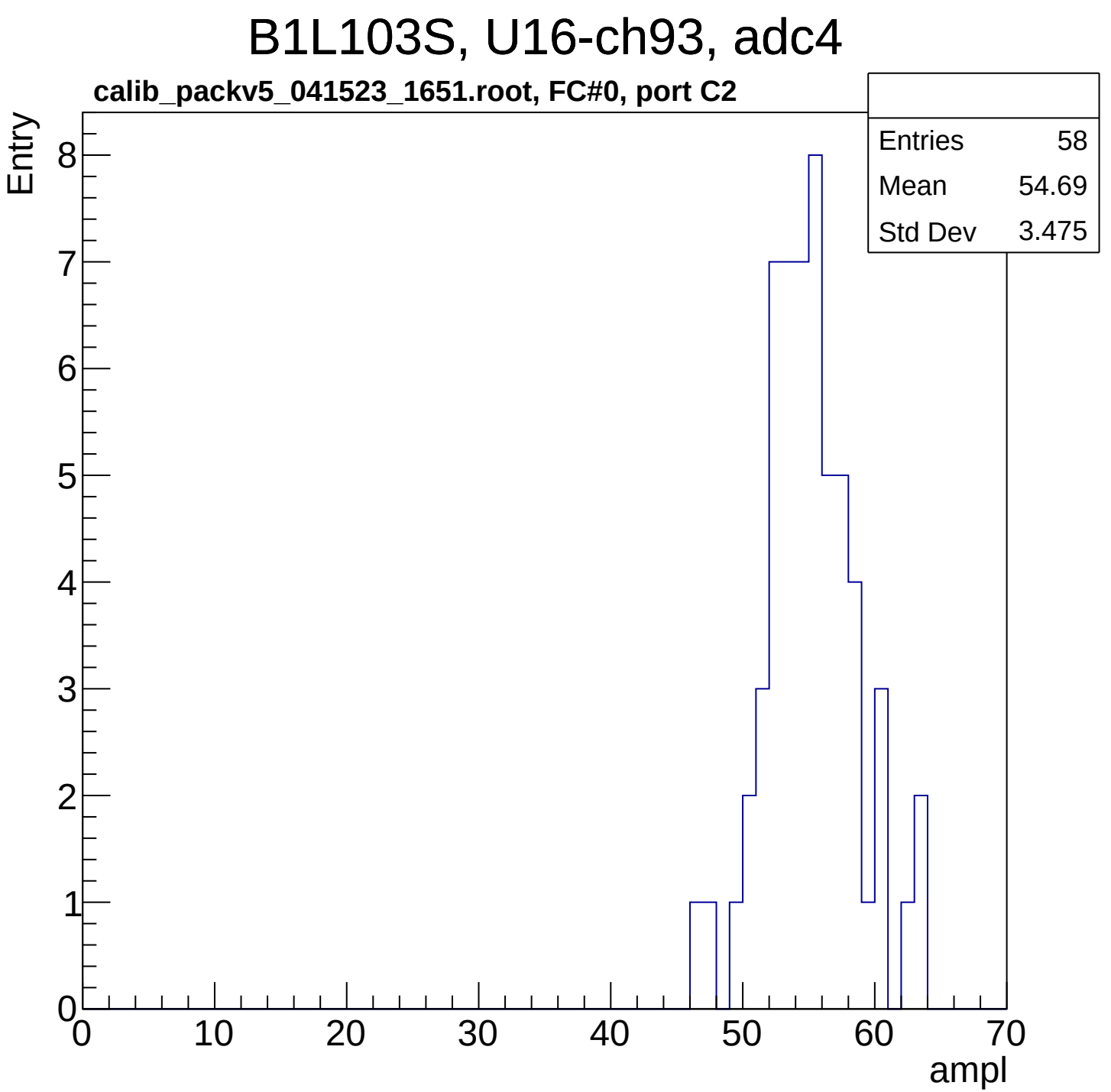
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch93, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 54.69
Std Dev 3.475
Entry
ampl
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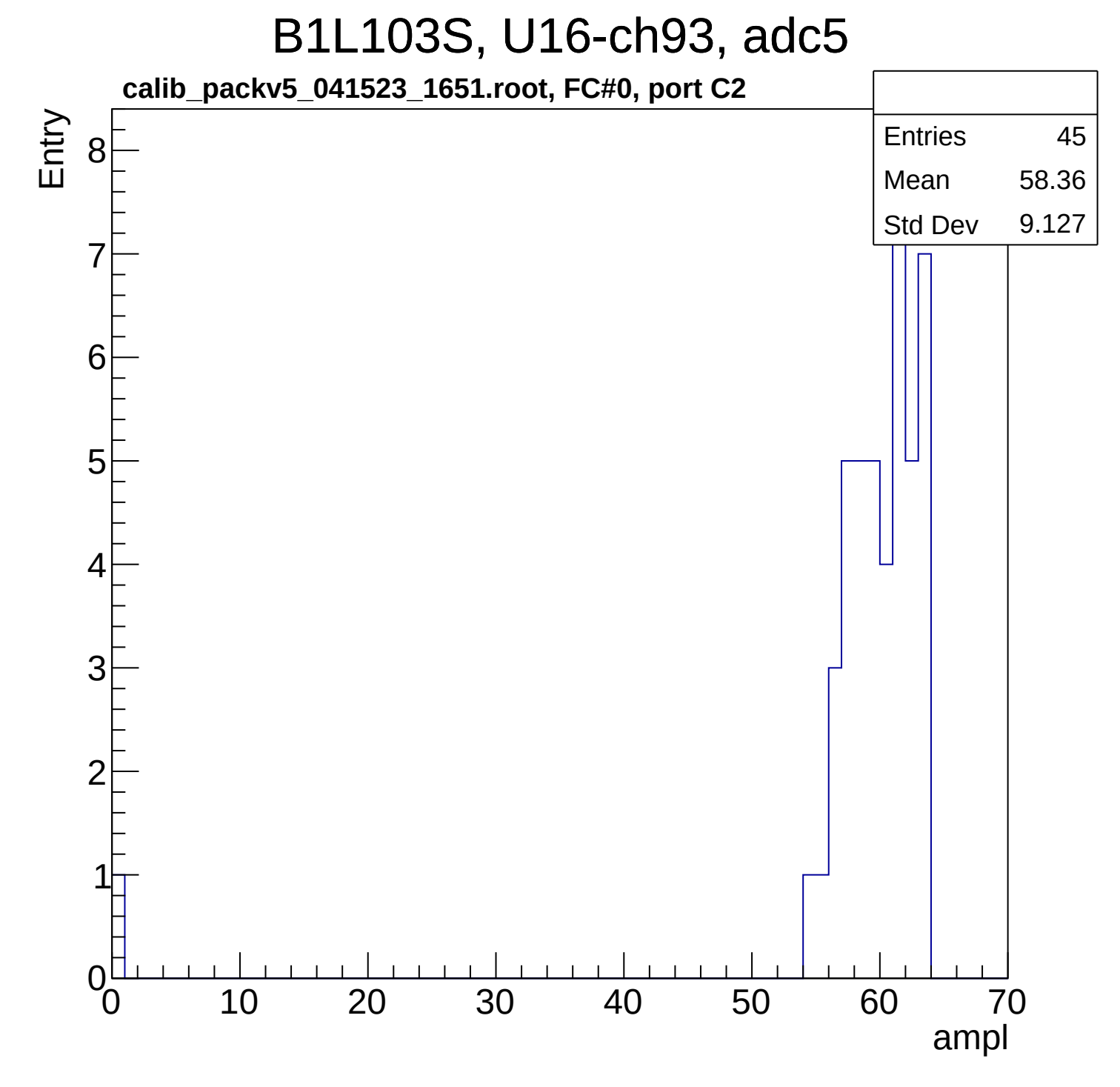
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch93, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.36
Std Dev 9.127
Entry
ampl
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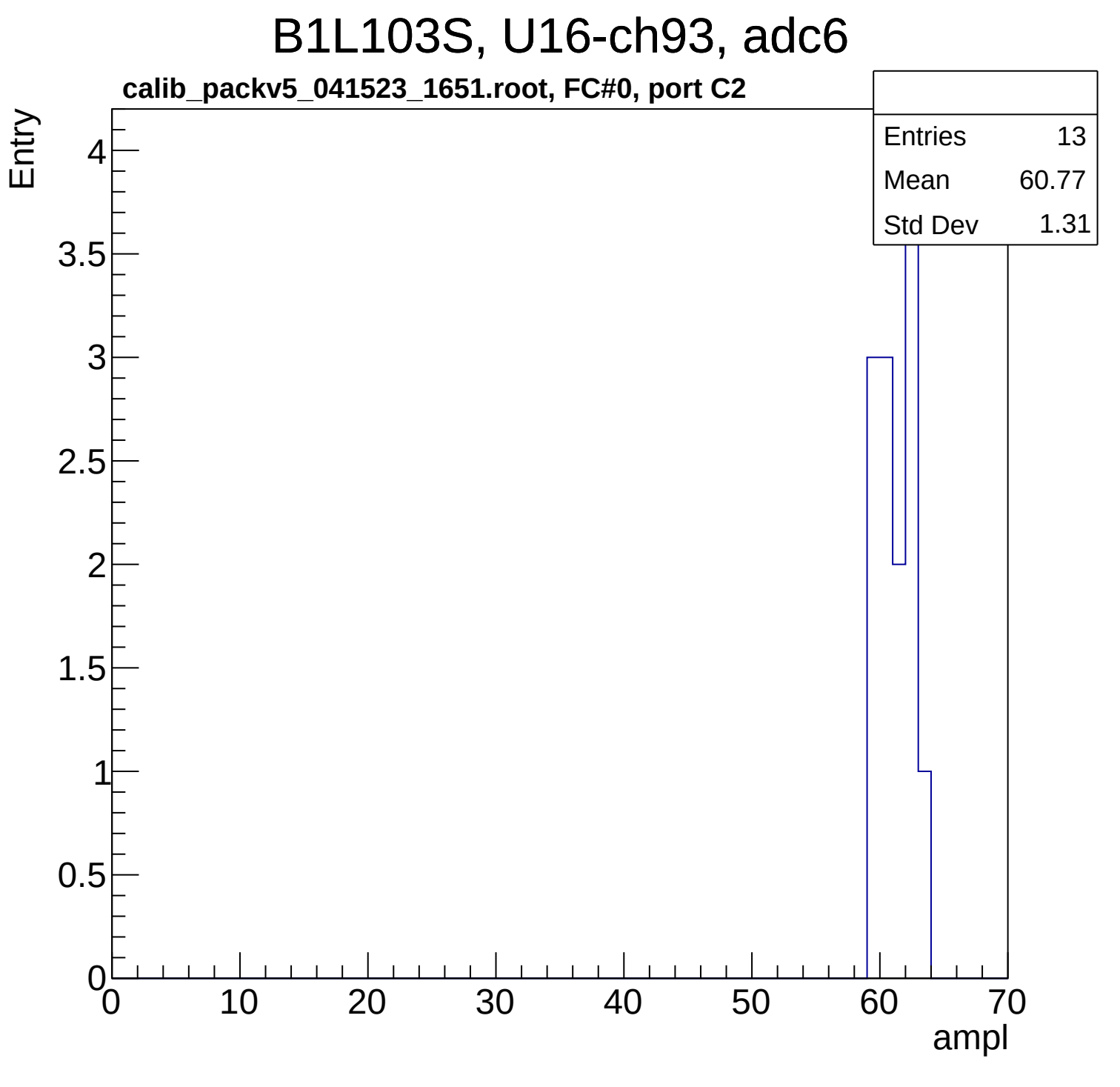
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch93, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 60.77
Std Dev 1.31
Entry
ampl
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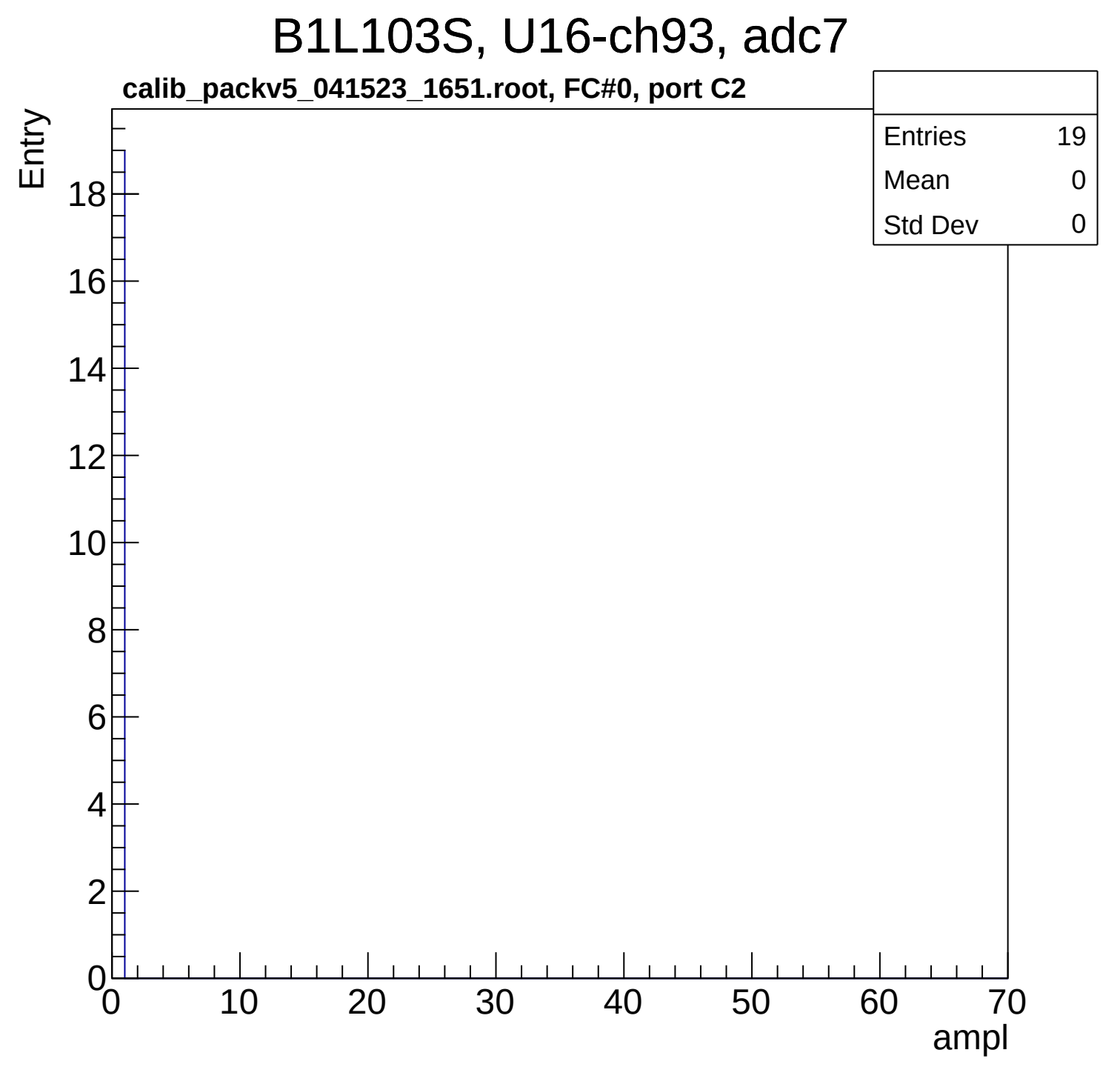
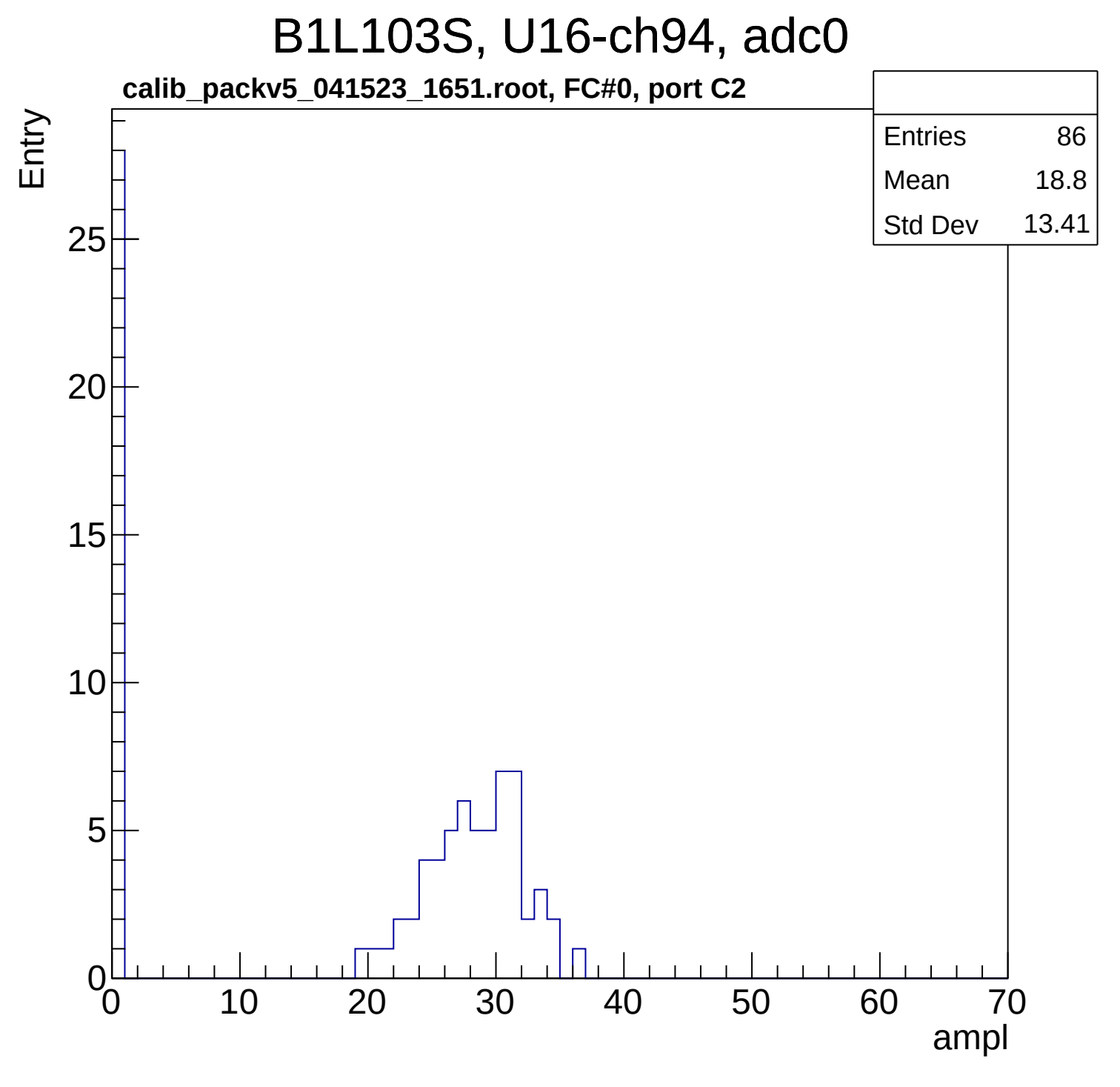
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U16-ch93, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch94, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 18.8
Std Dev 13.41
Entry
0
5
10
15
20
25
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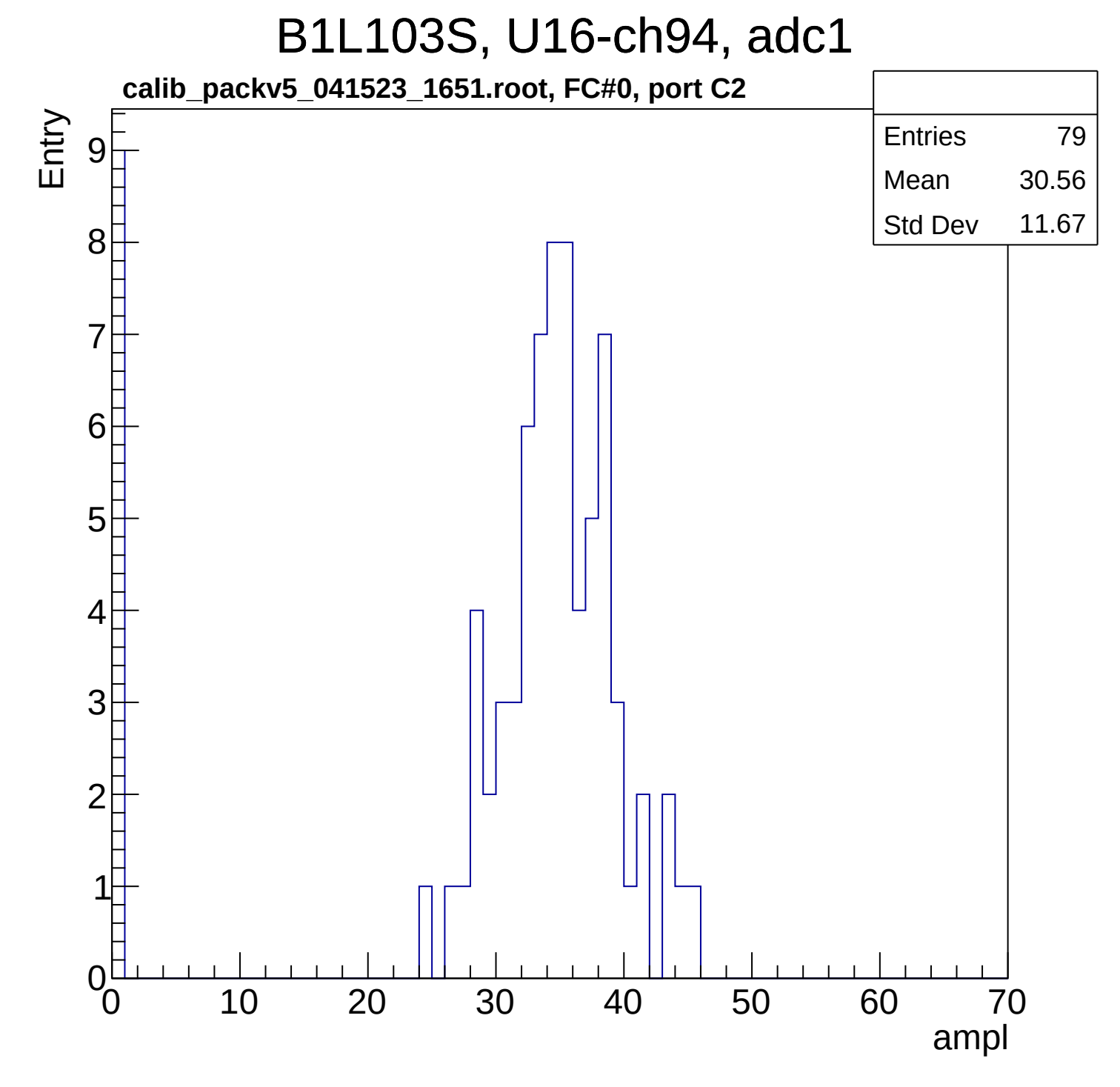
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch94, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 30.56
Std Dev 11.67
Entry
ampl
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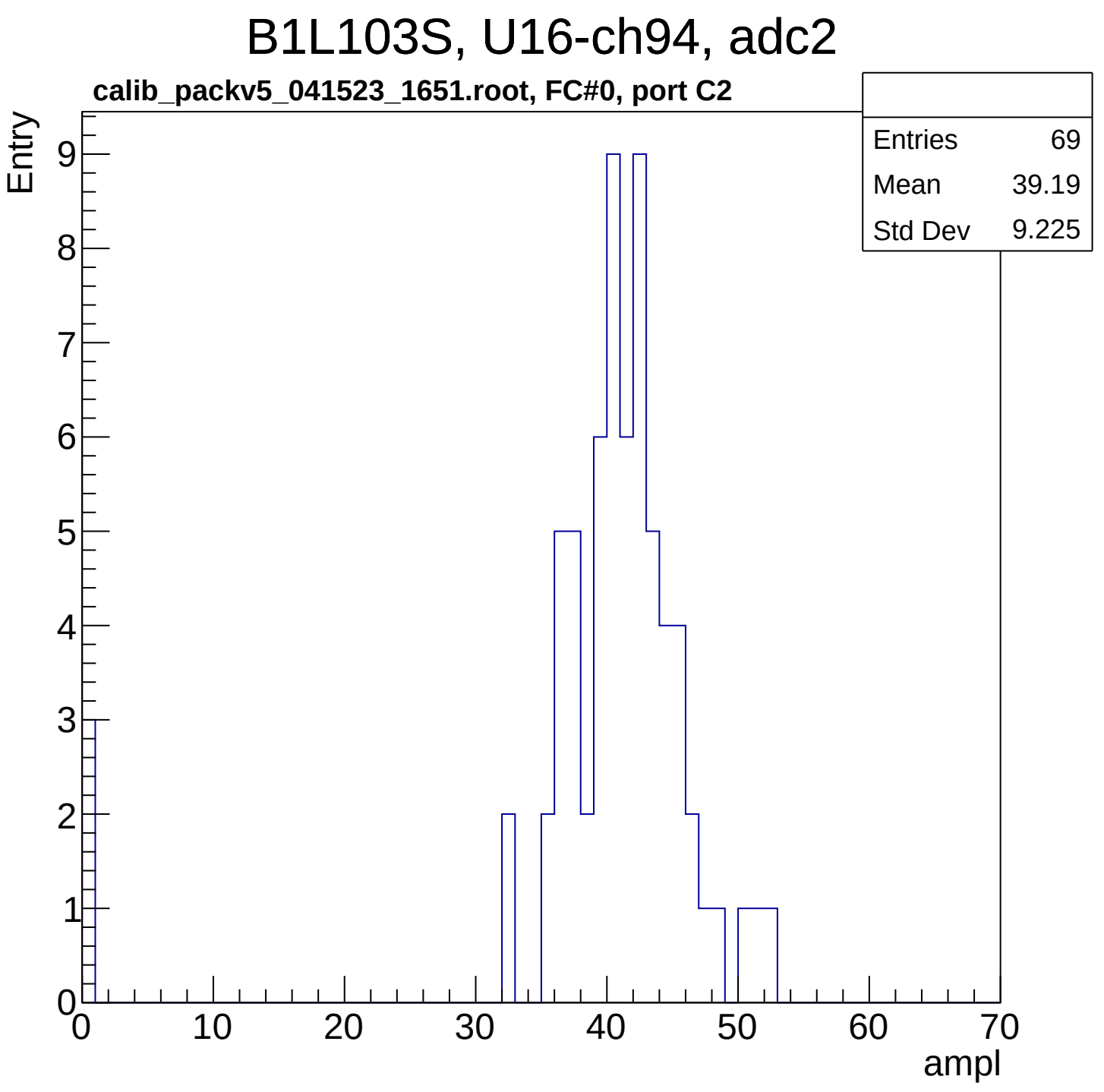
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch94, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 39.19
Std Dev 9.225
Entry
ampl
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2
3
4
5
6
7
8
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0
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30
40
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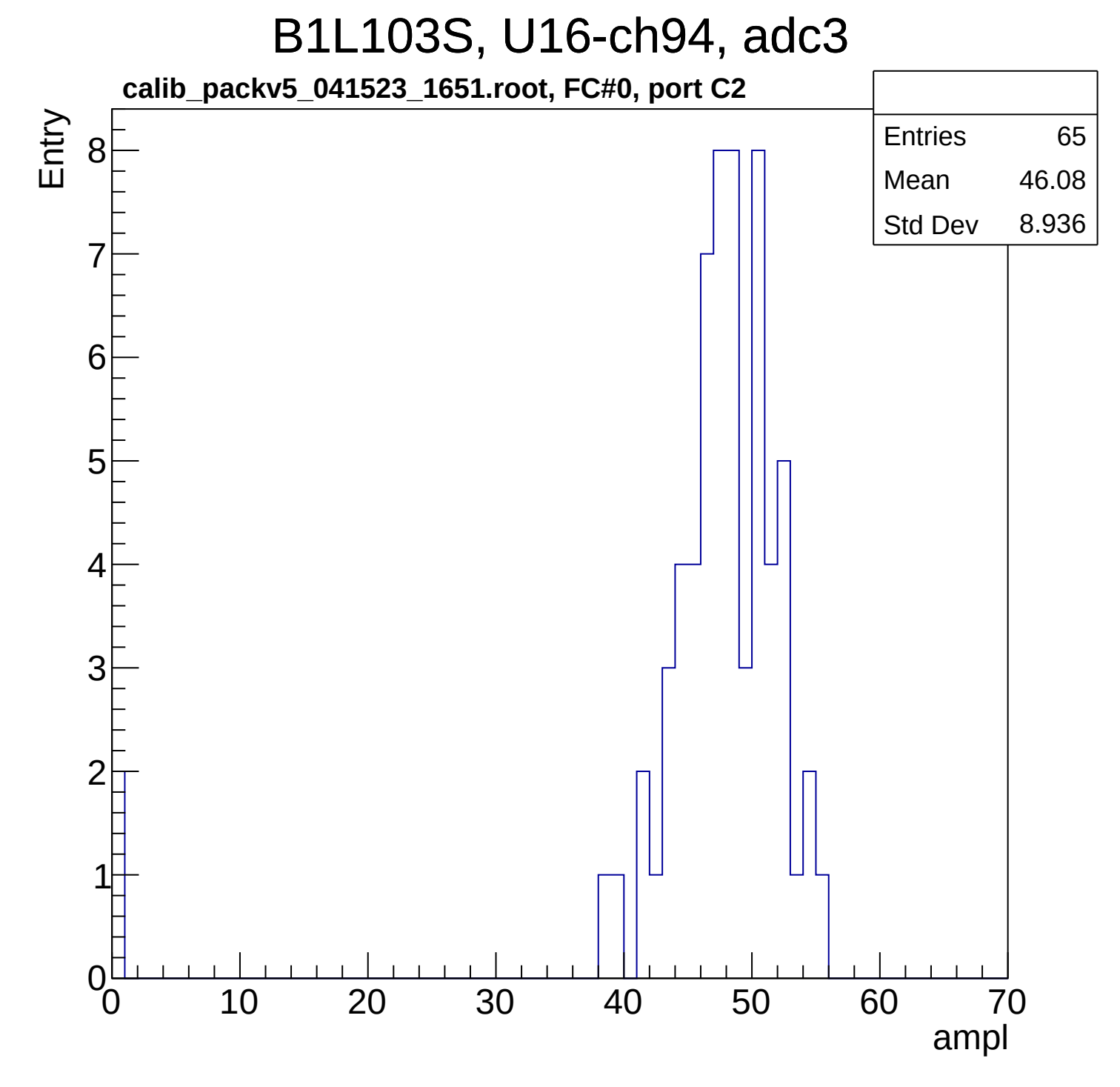
60
70


B1L103S, U16-ch94, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 46.08
Std Dev 8.936
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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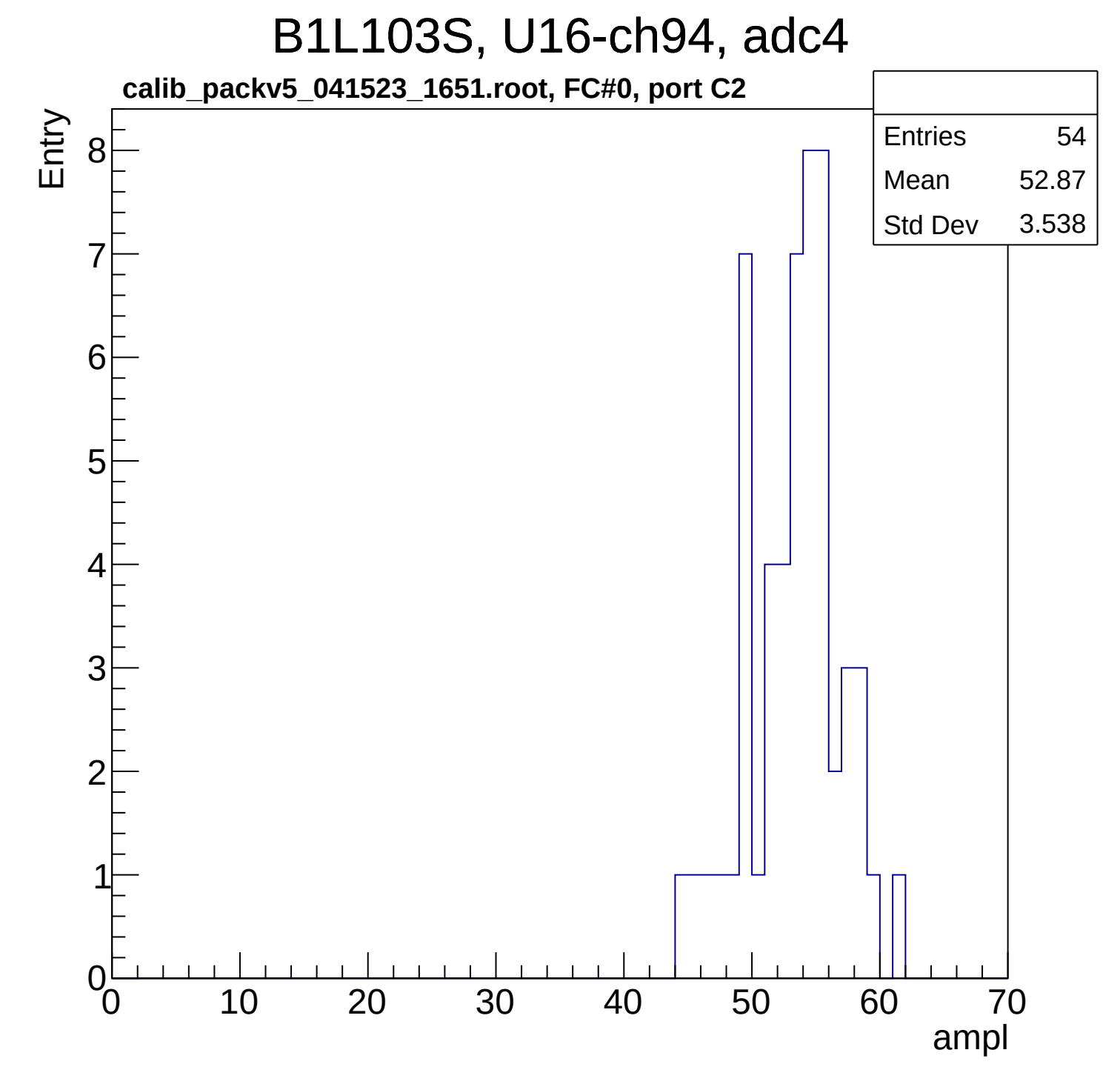
40
50
60
70


B1L103S, U16-ch94, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 52.87
Std Dev 3.538
Entry
ampl
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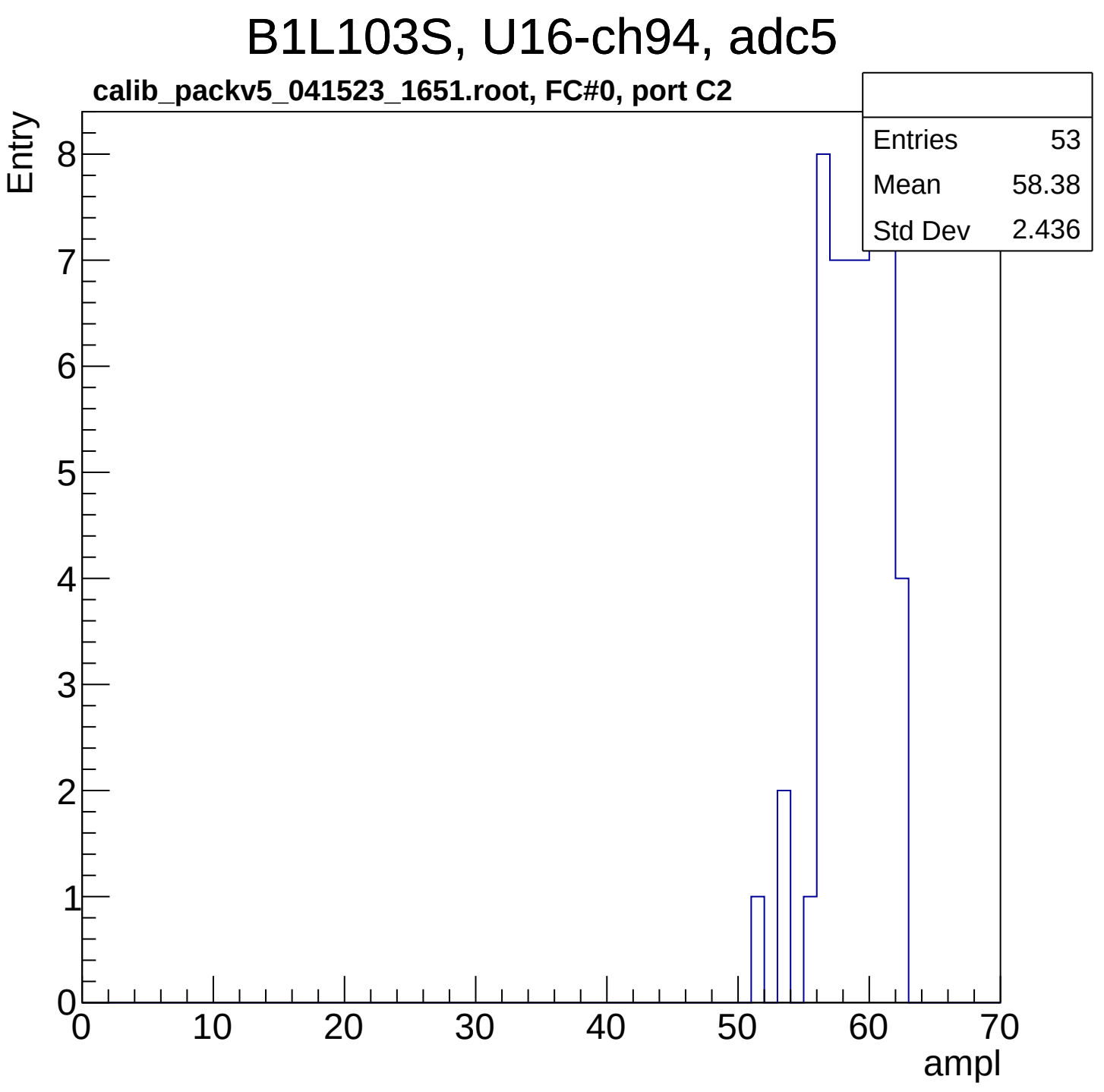
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch94, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.38
Std Dev 2.436
Entry
ampl
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2
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4
5
6
7
8
0
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20
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40
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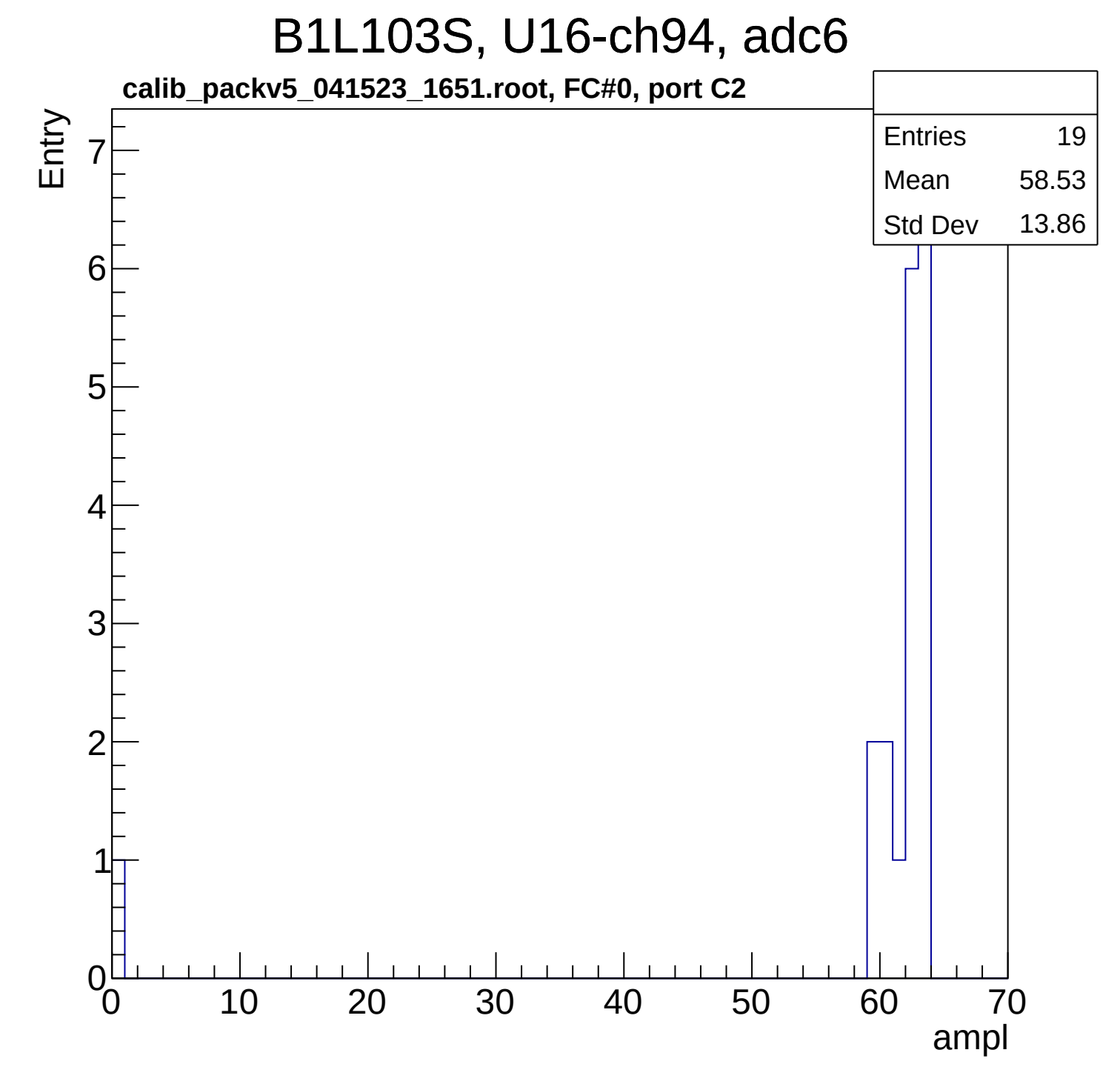
60
70


B1L103S, U16-ch94, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 58.53
Std Dev 13.86
Entry
ampl
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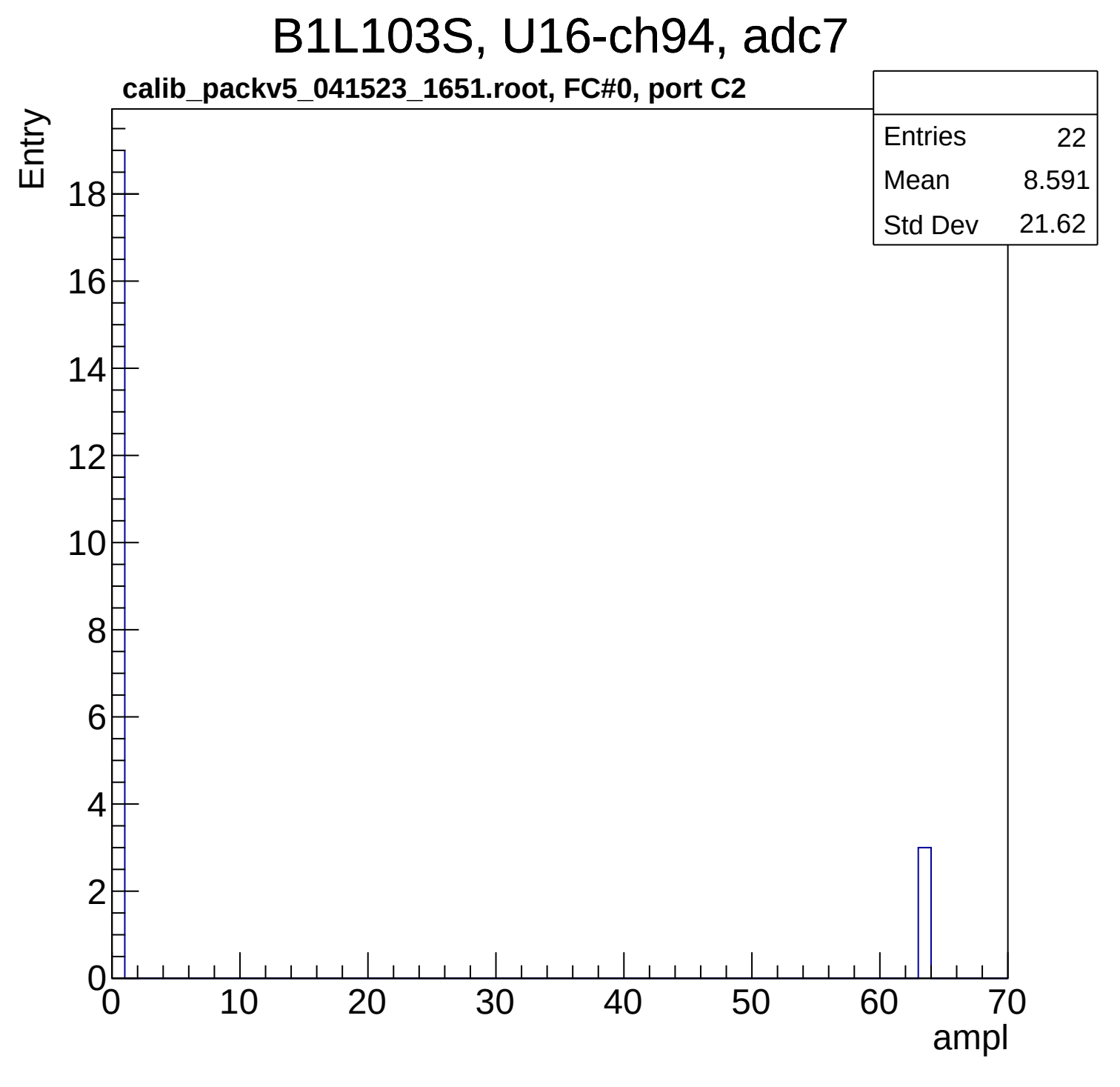
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch94, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.591
Std Dev 21.62
Entry
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6
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10
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14
16
18
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10
20
30
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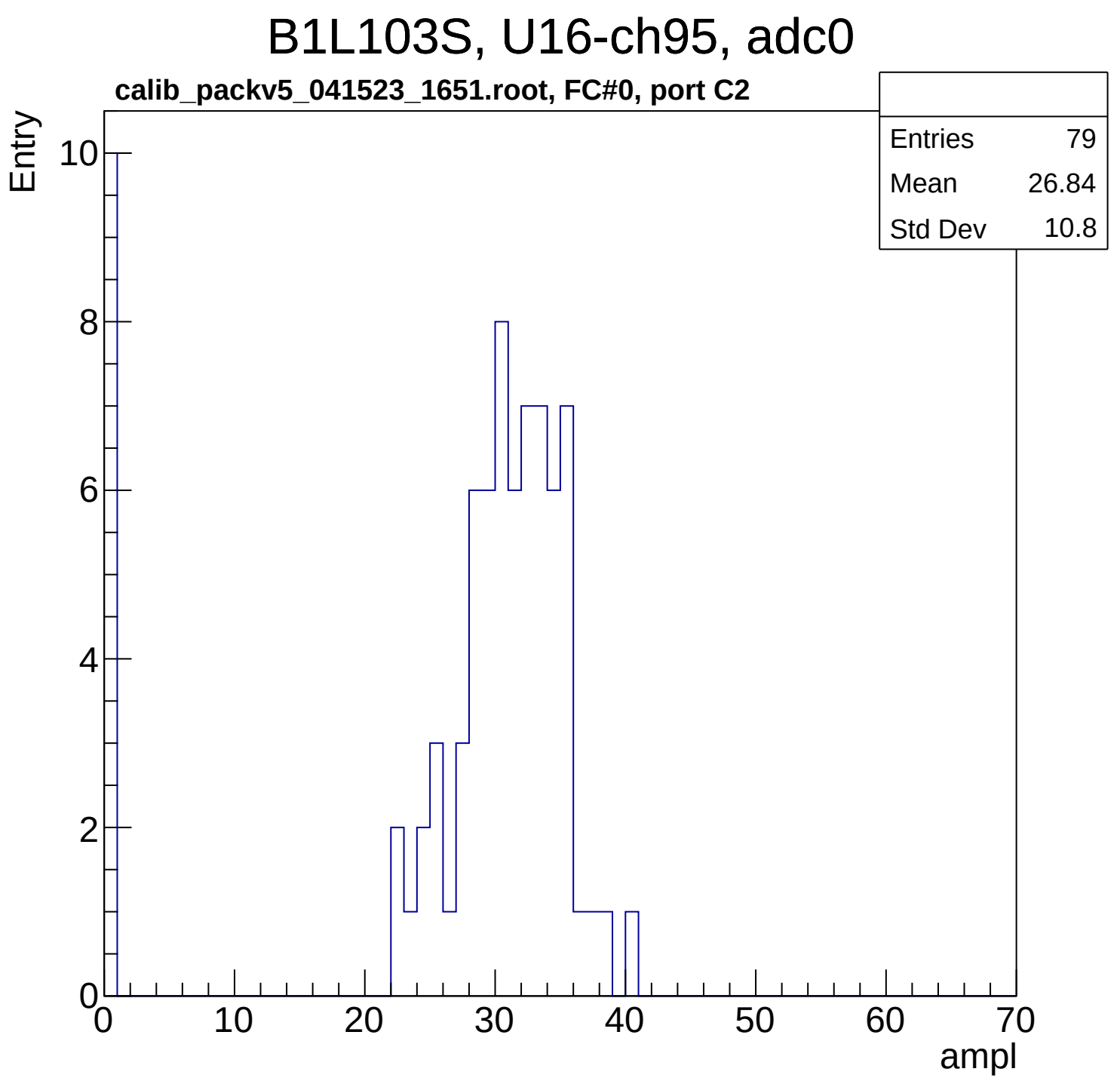
50
60
70
ampl


B1L103S, U16-ch95, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 26.84
Std Dev 10.8
Entry
ampl
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0
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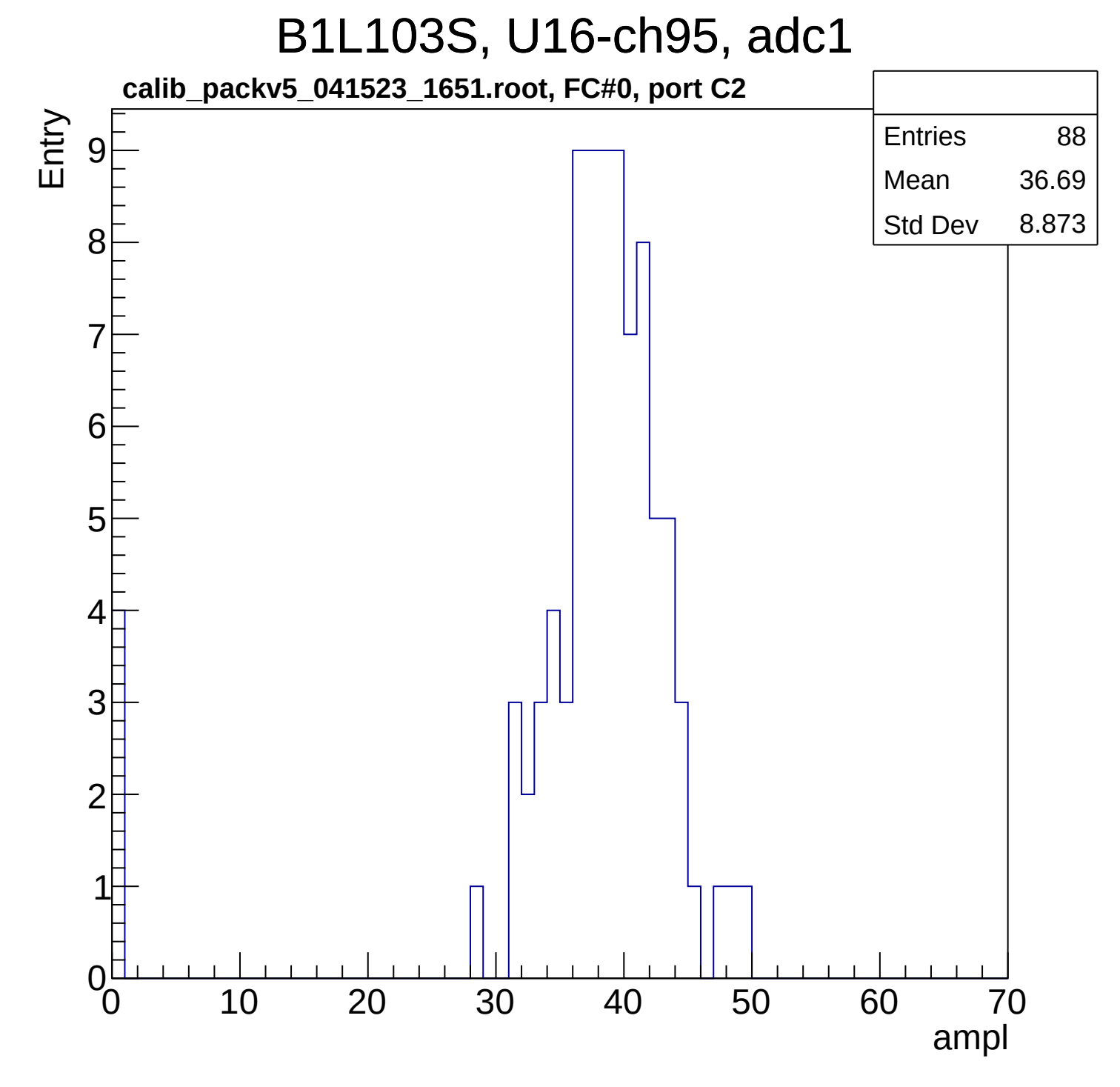
40
50
60
70


B1L103S, U16-ch95, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 36.69
Std Dev 8.873
Entry
ampl
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4
5
6
7
8
9
0
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20
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40
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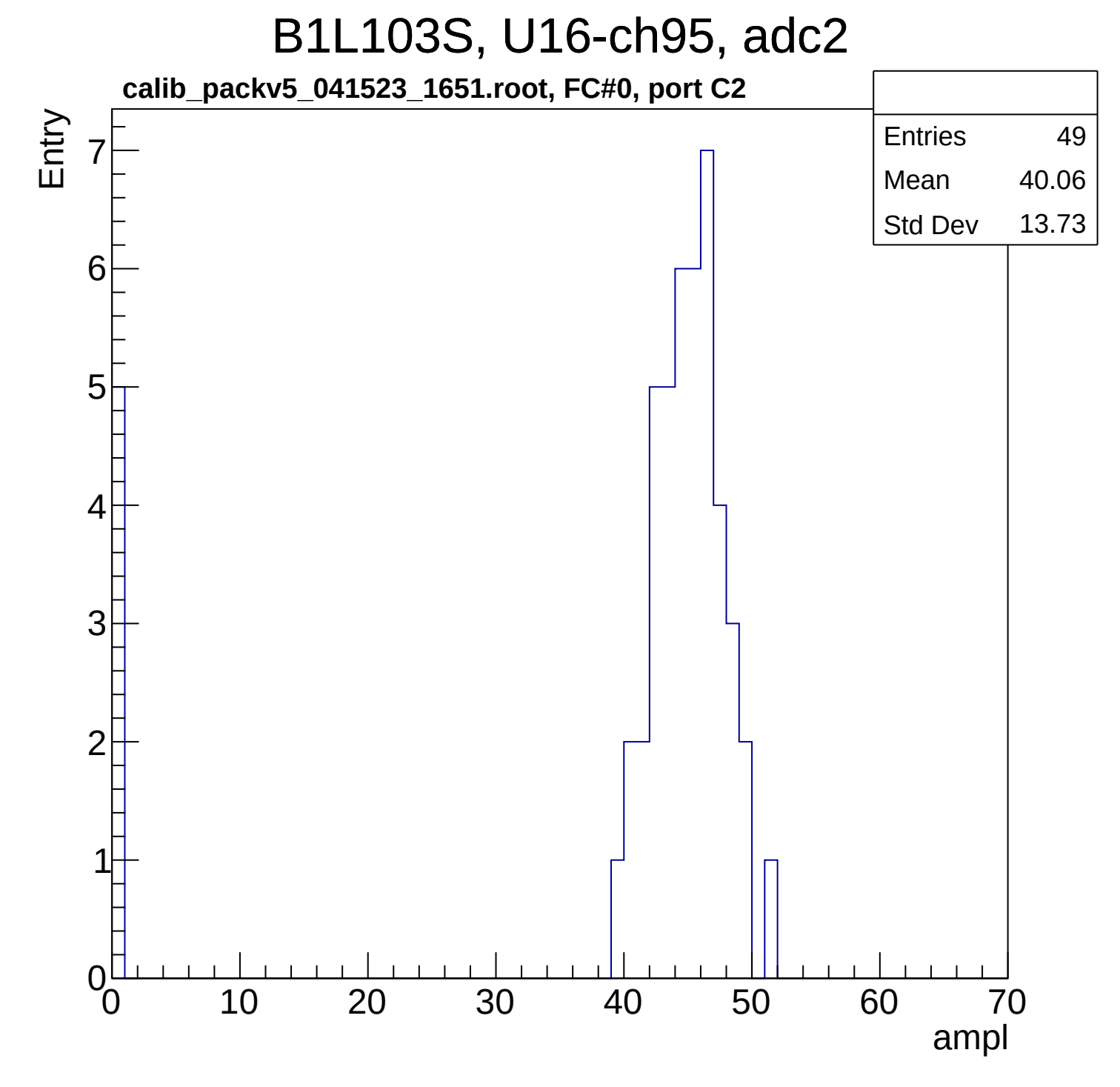
60
70


B1L103S, U16-ch95, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 40.06
Std Dev 13.73
Entry
ampl
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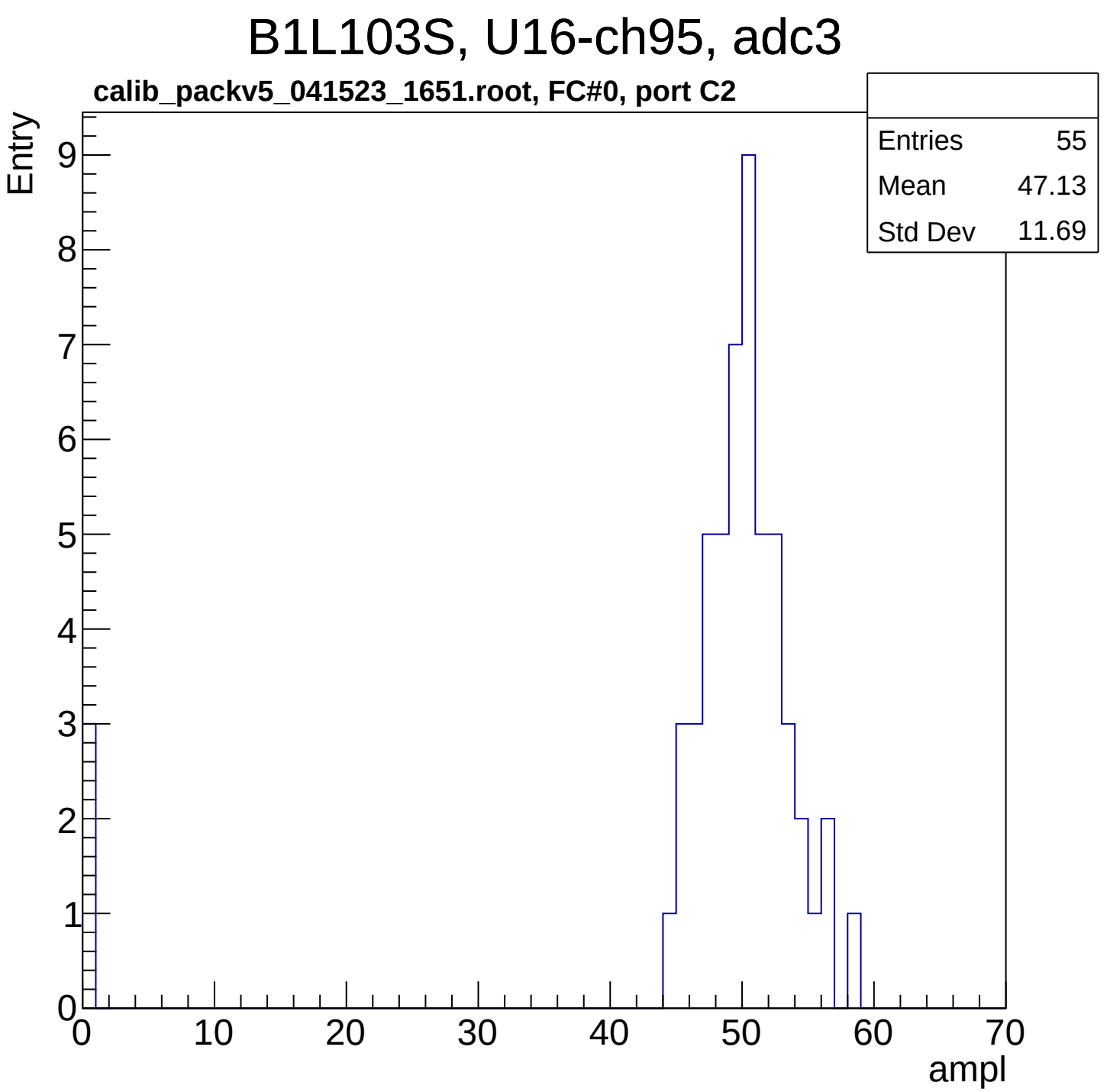
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch95, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 47.13
Std Dev 11.69
Entry
ampl
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2
3
4
5
6
7
8
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0
10
20
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40
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60
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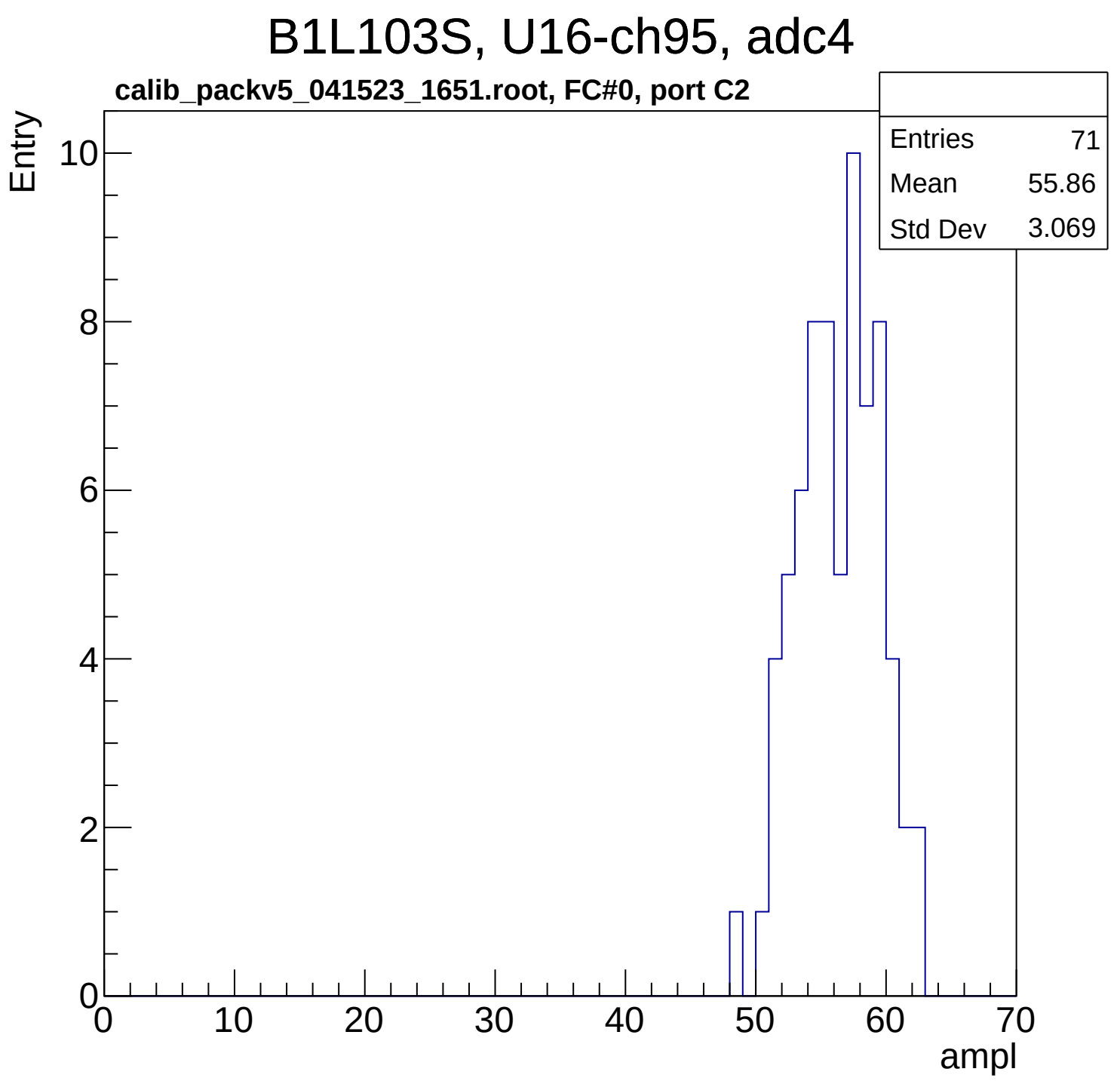
B1L103S, U16-ch95, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 55.86
Std Dev 3.069
Entry
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20
30
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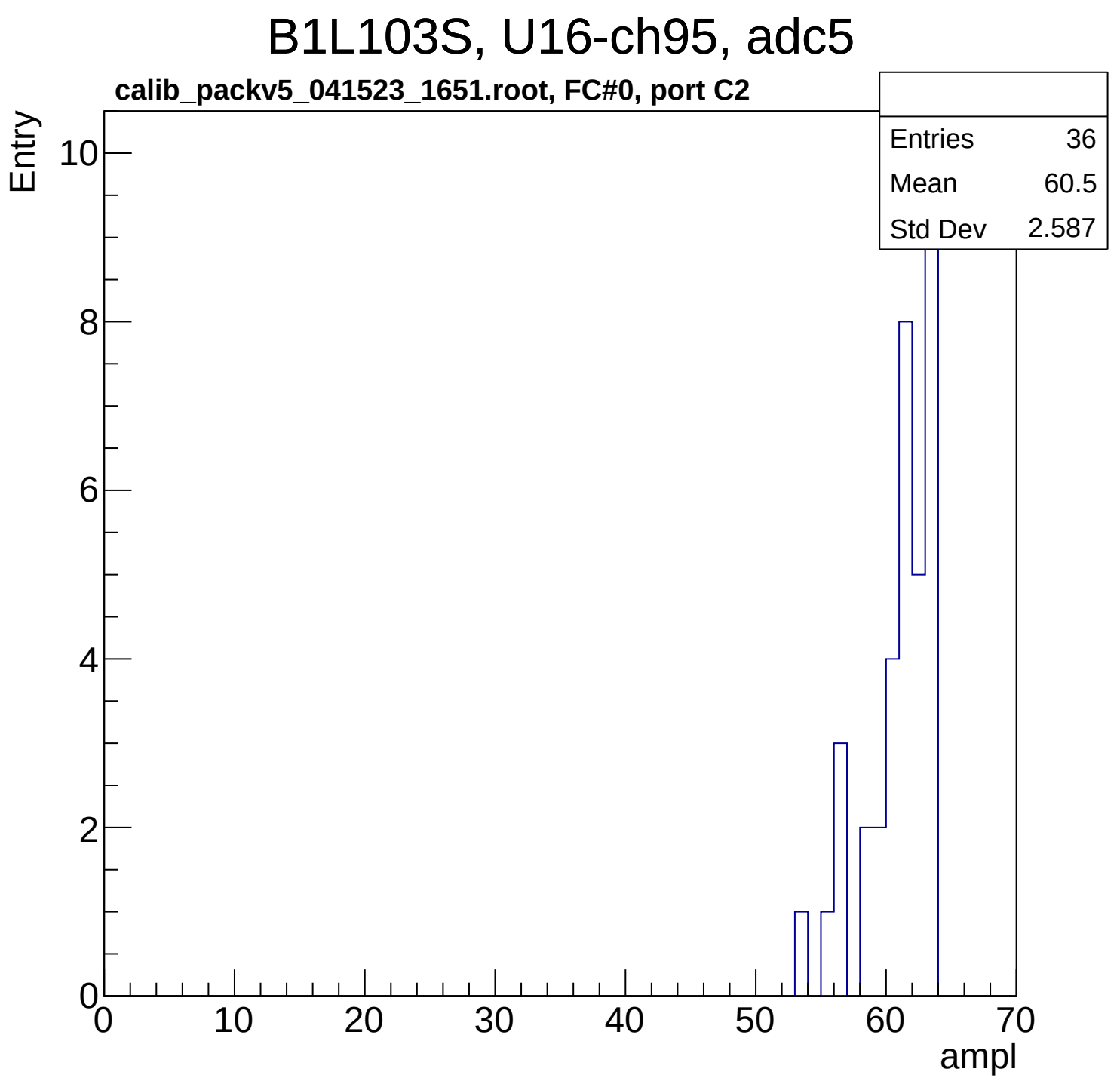
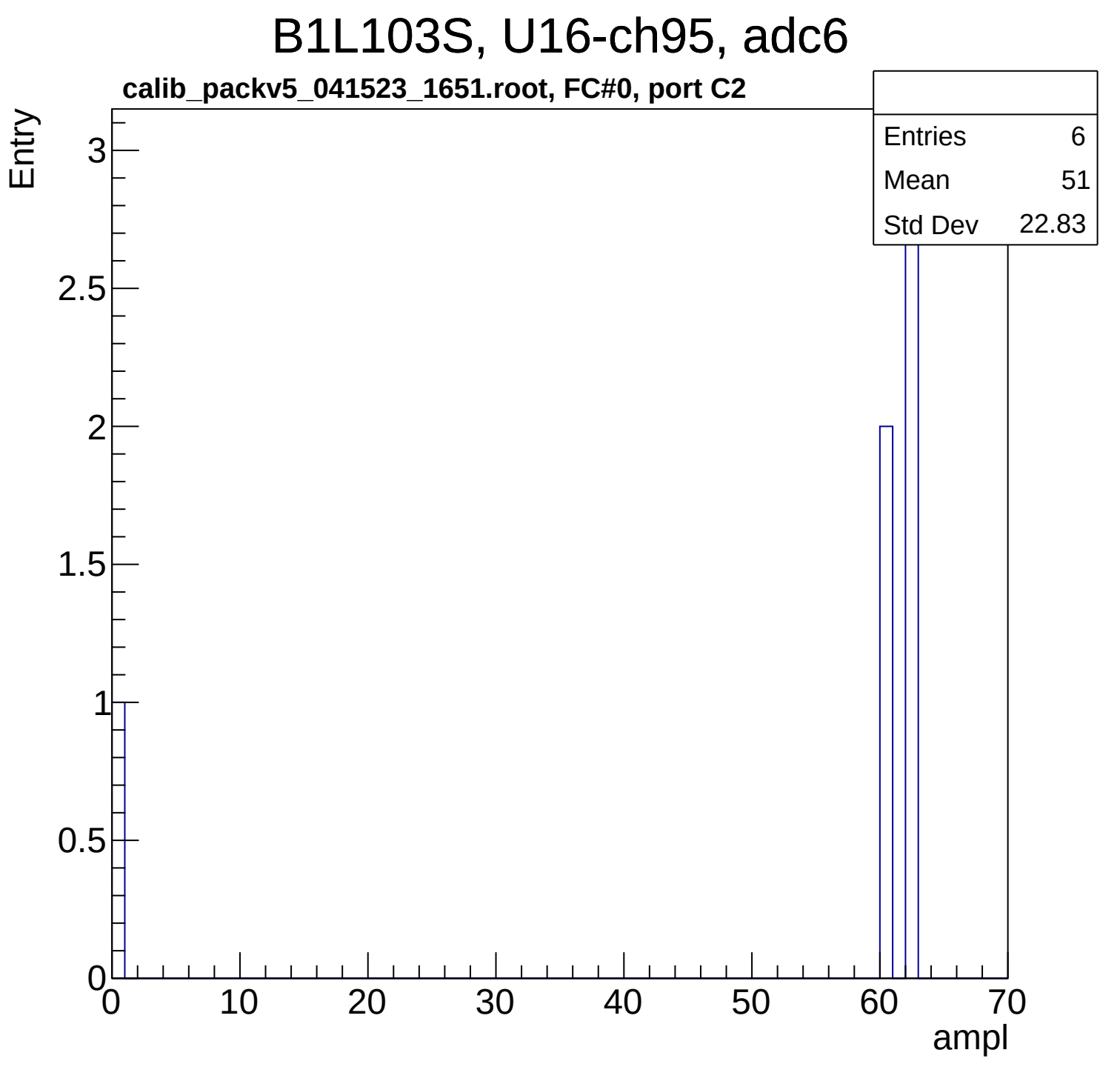
50
60
70
ampl


B1L103S, U16-ch95, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 60.5
Std Dev 2.587
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch95, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 51
Std Dev 22.83
Entry
ampl
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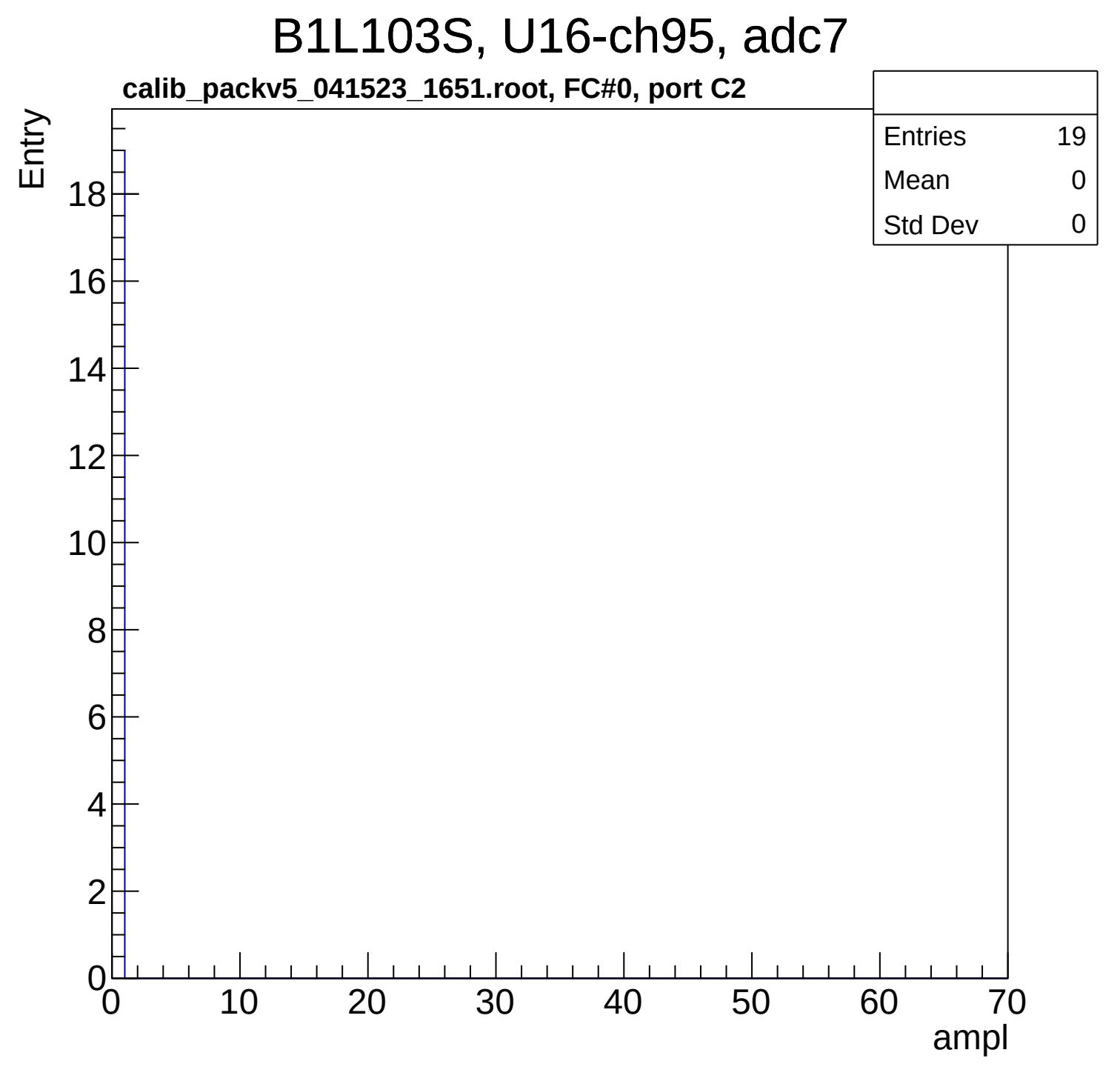
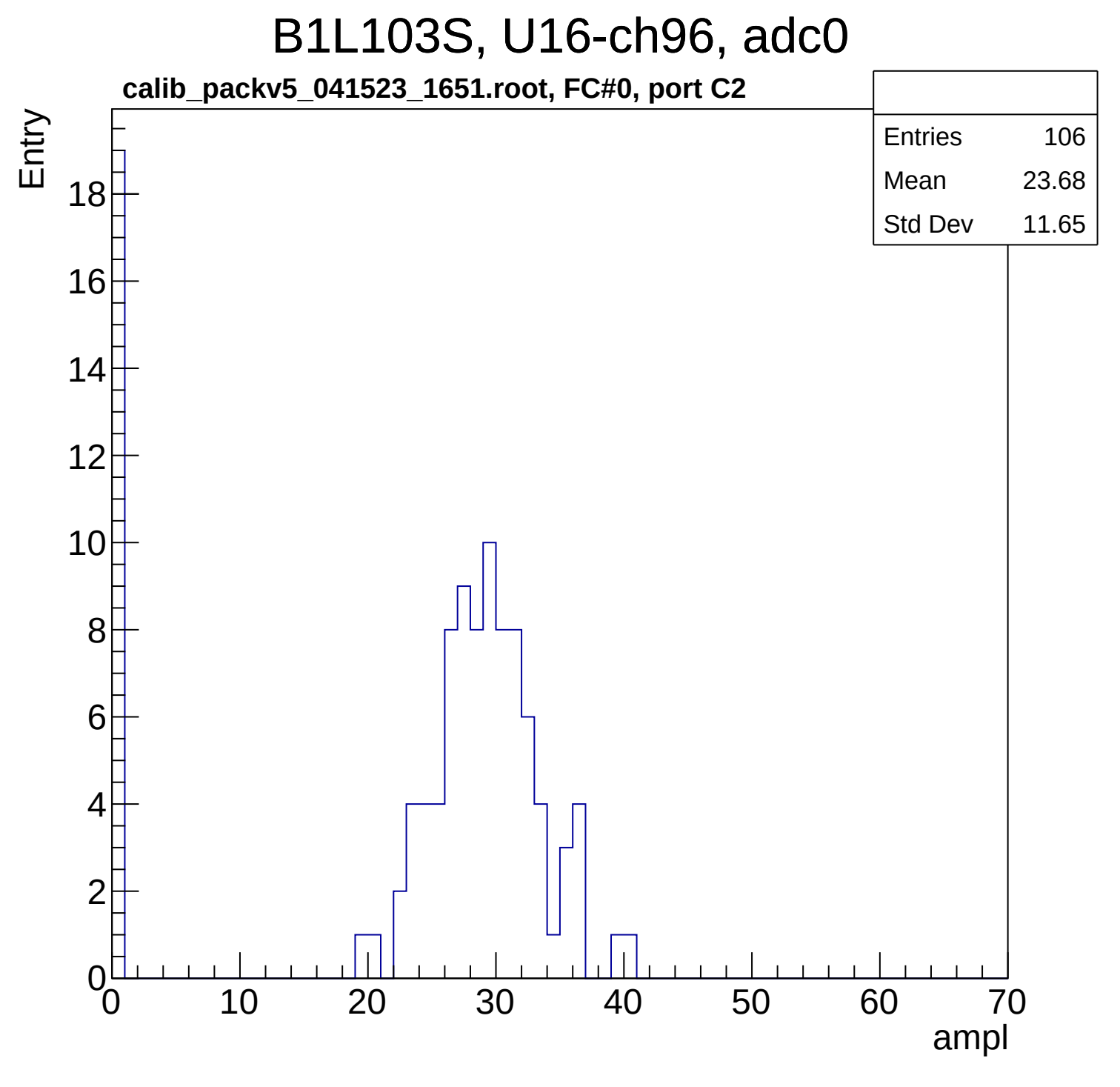
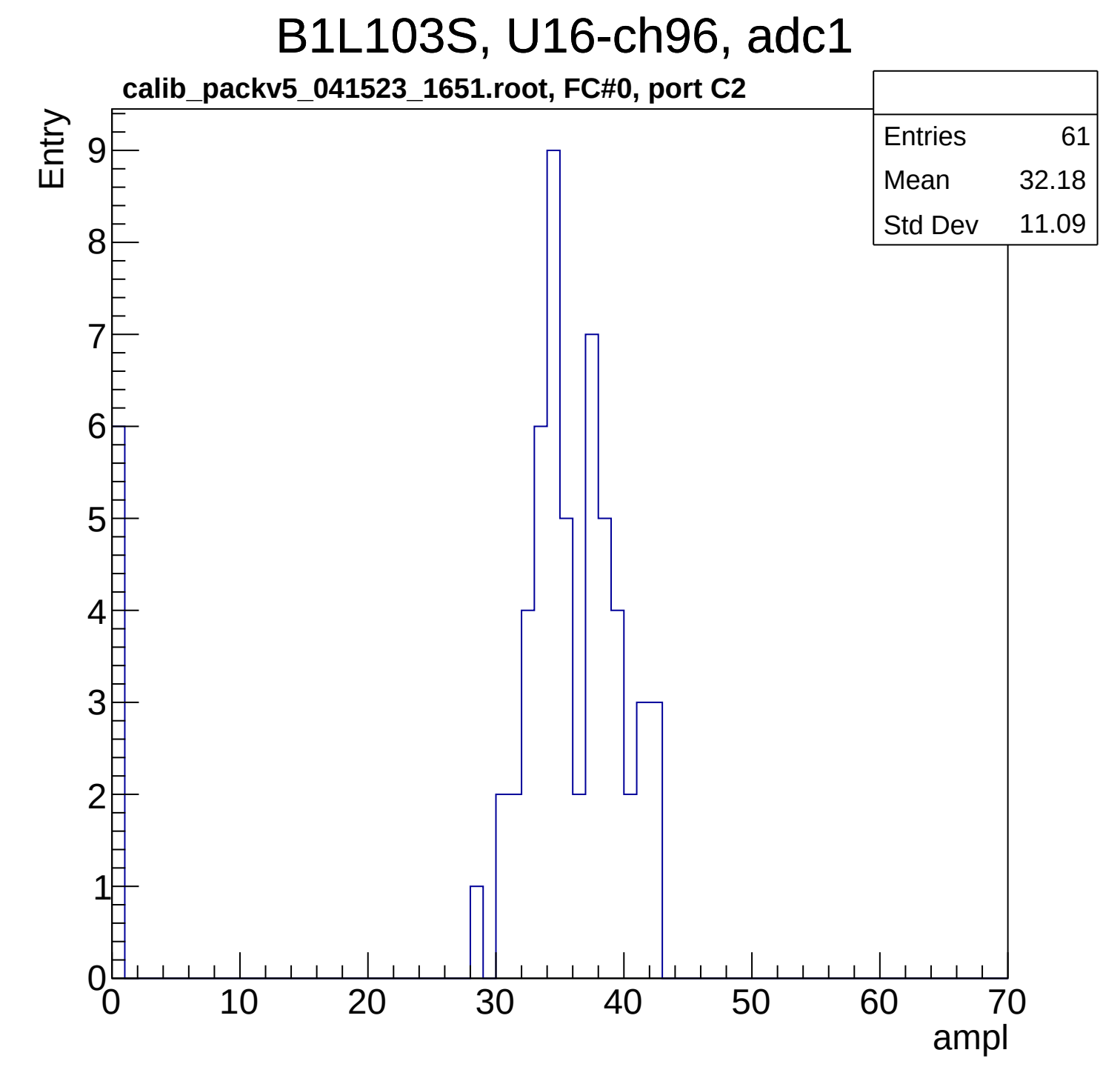
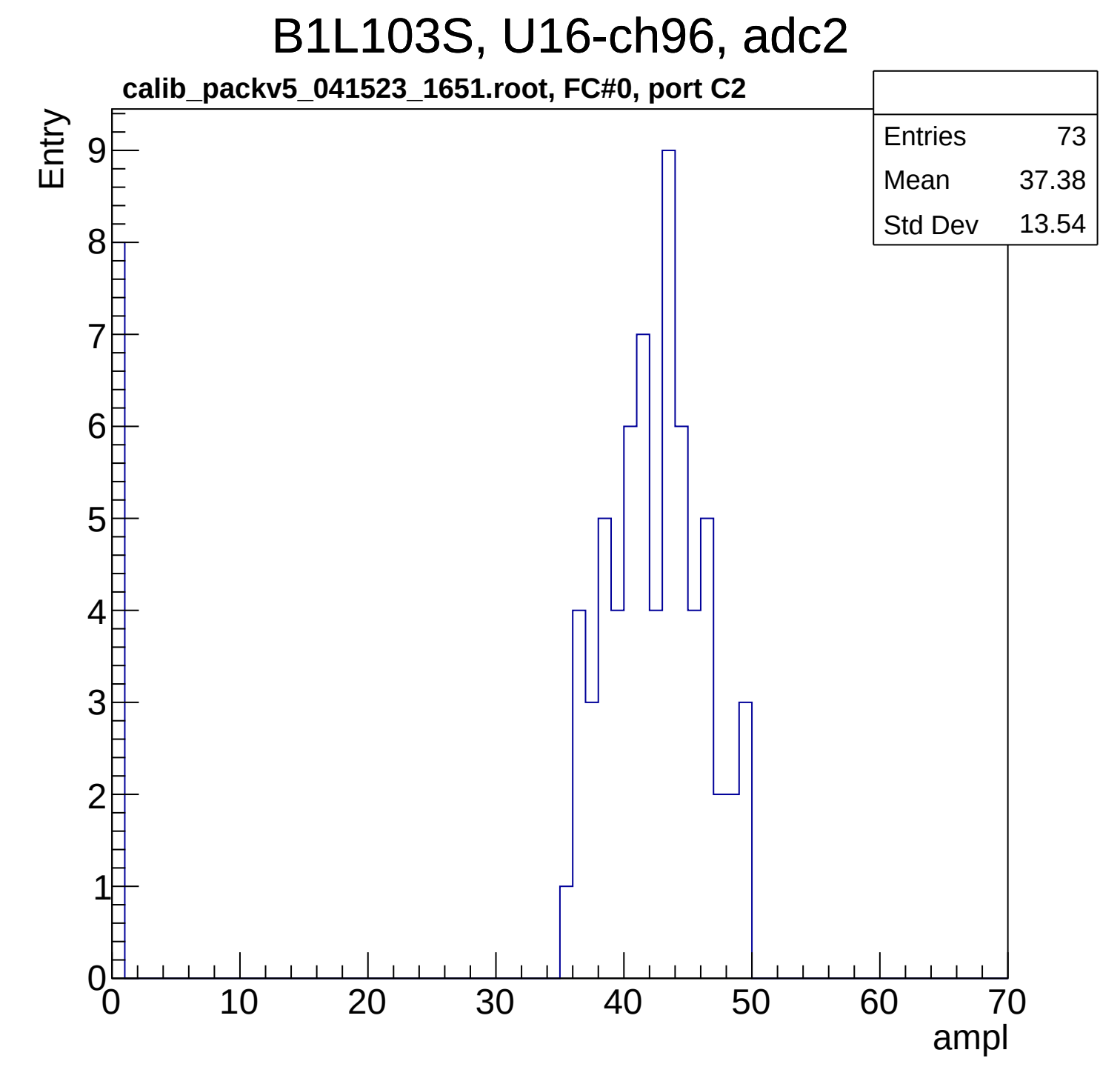
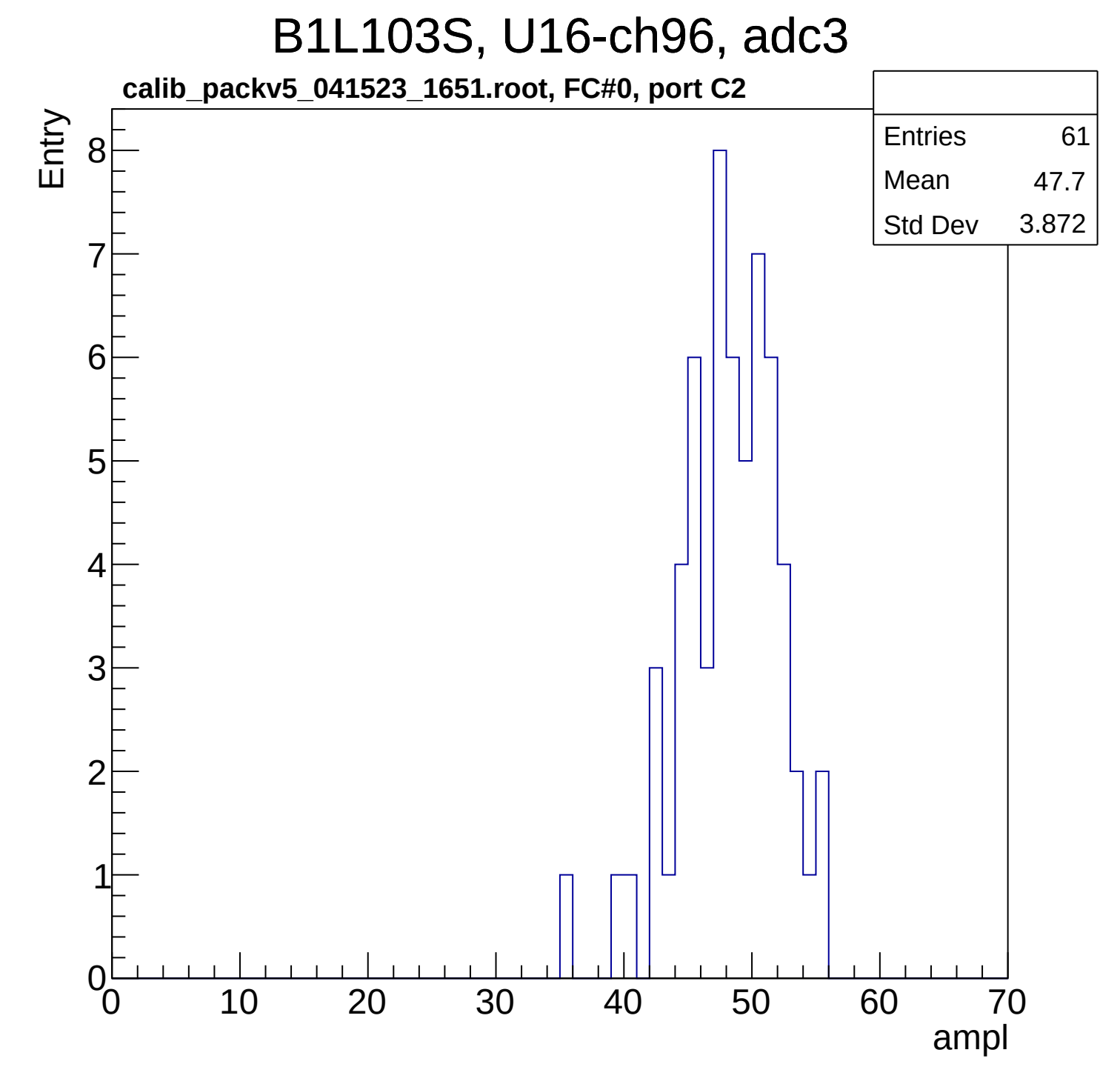
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U16-ch95, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch96, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 106
Mean 23.68
Std Dev 11.65
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch96, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 32.18
Std Dev 11.09
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch96, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 37.38
Std Dev 13.54
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch96, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 47.7
Std Dev 3.872
Entry
ampl
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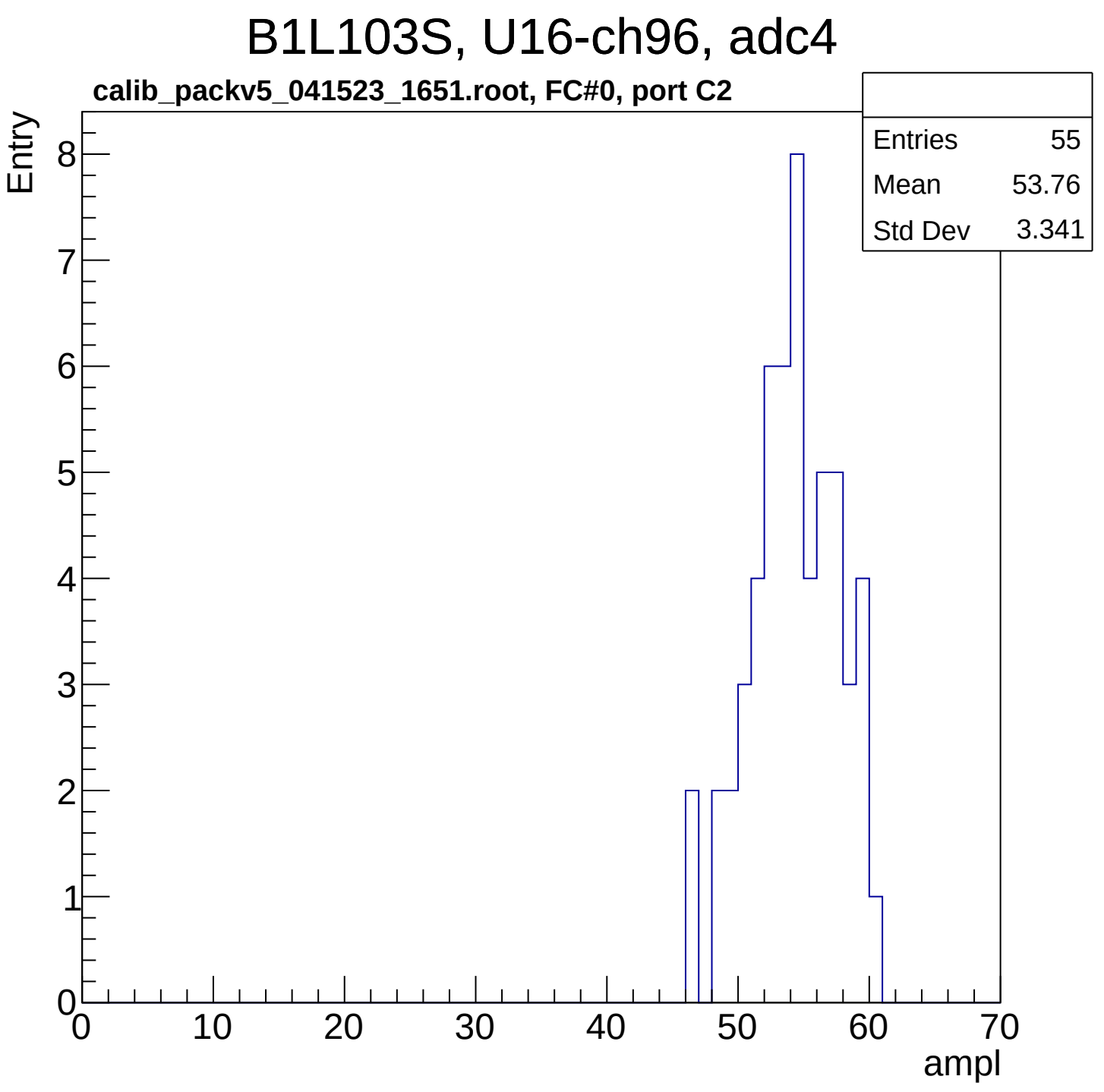
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch96, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 53.76
Std Dev 3.341
Entry
ampl
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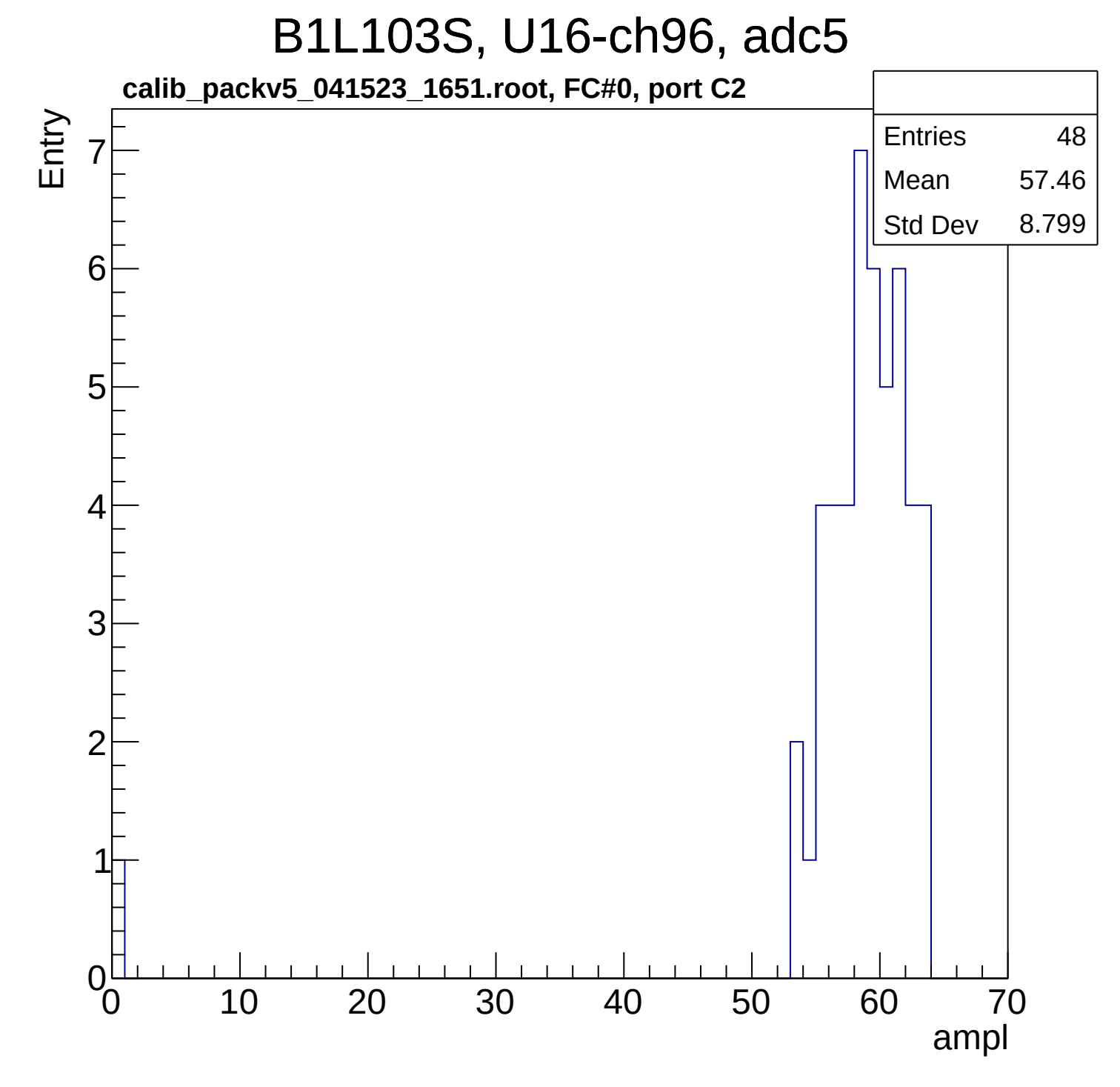
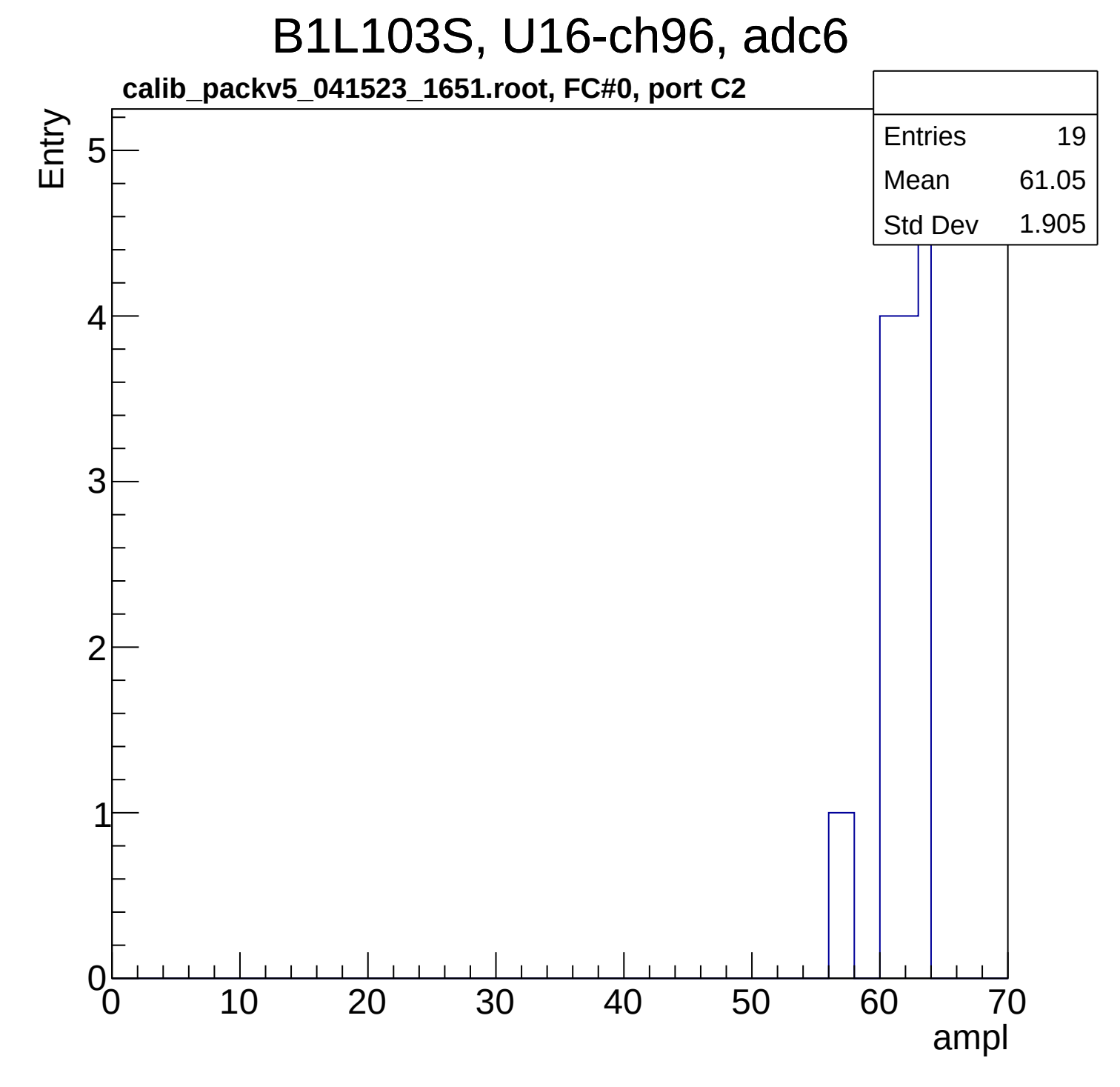
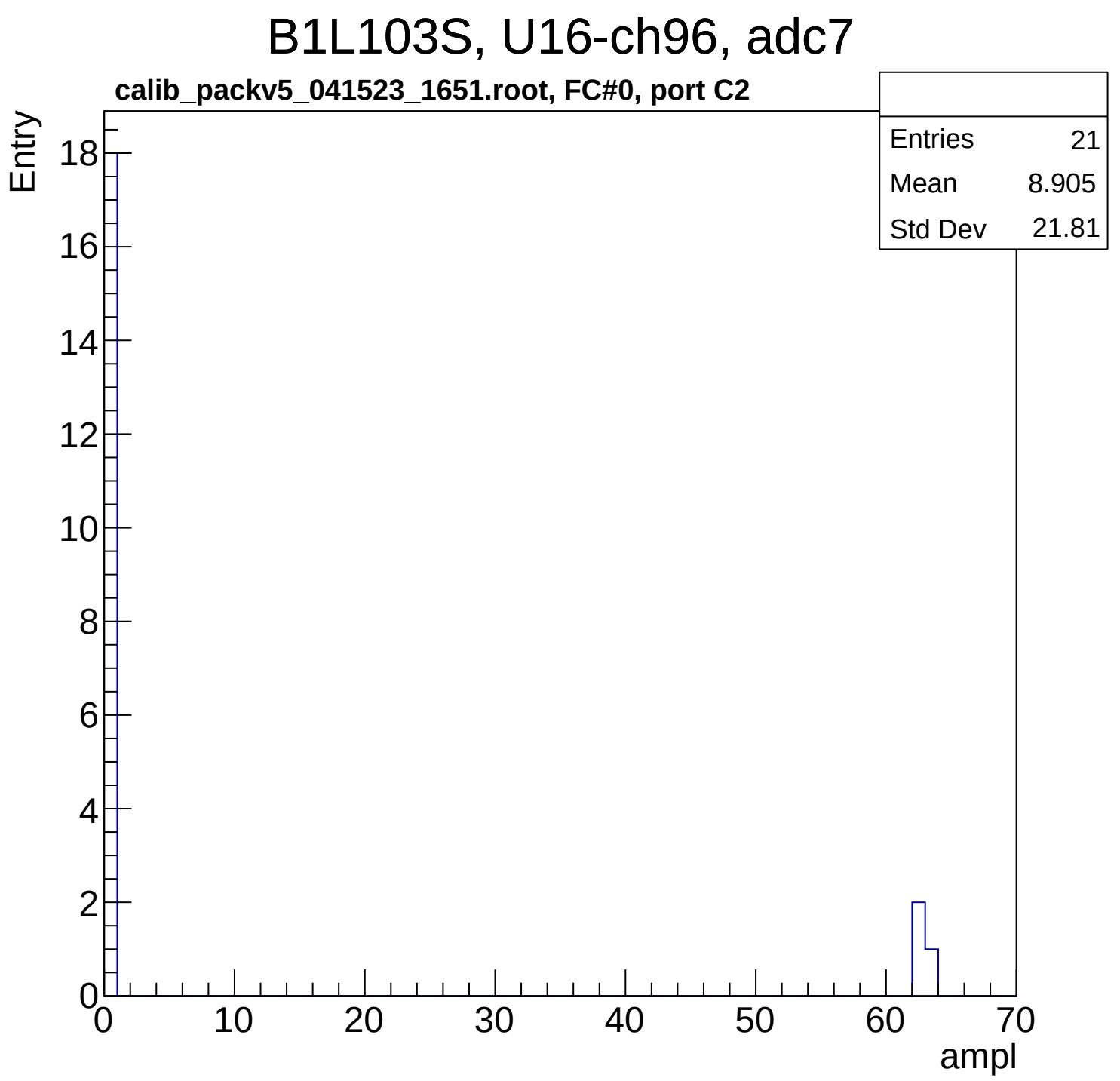
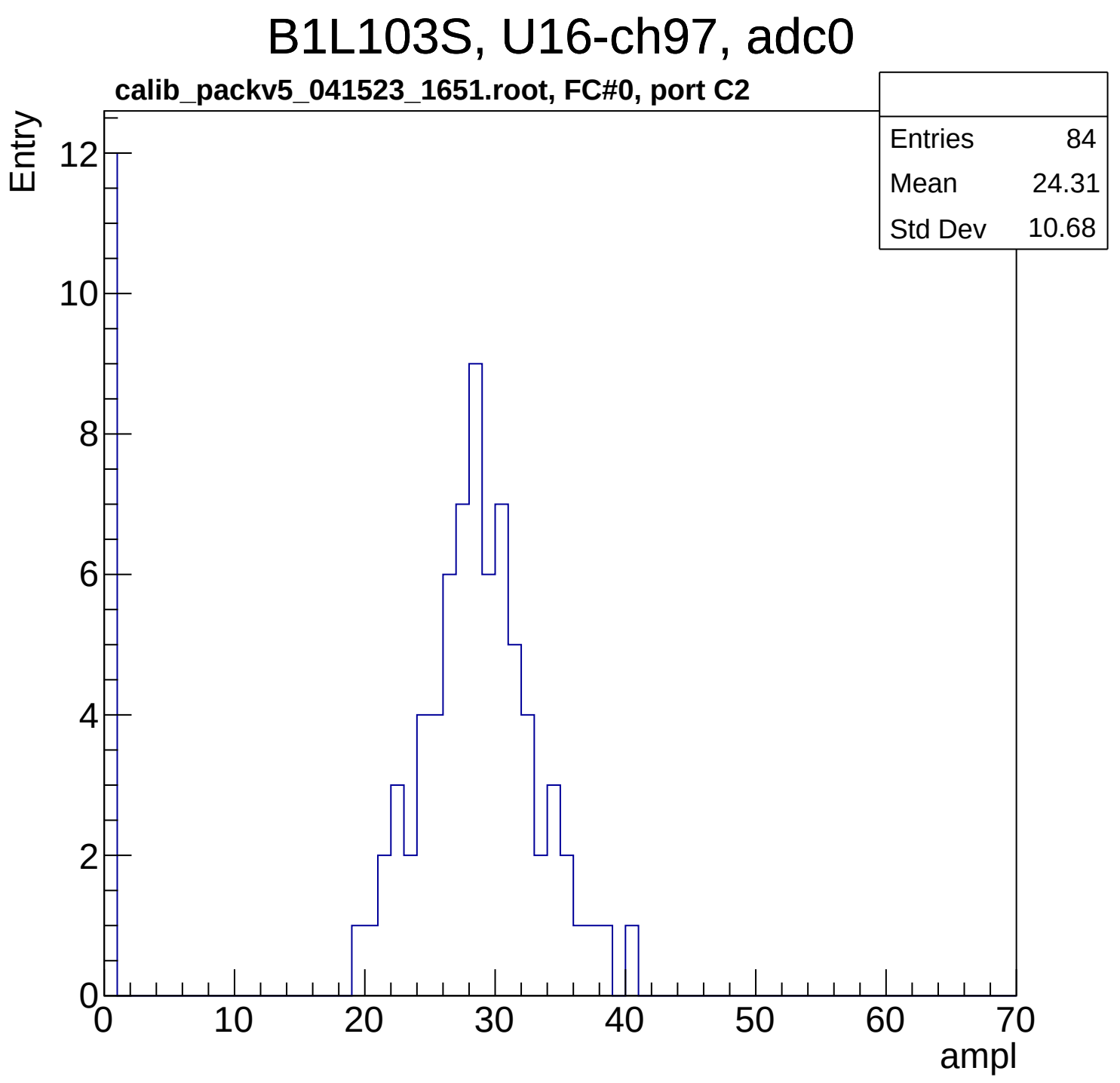
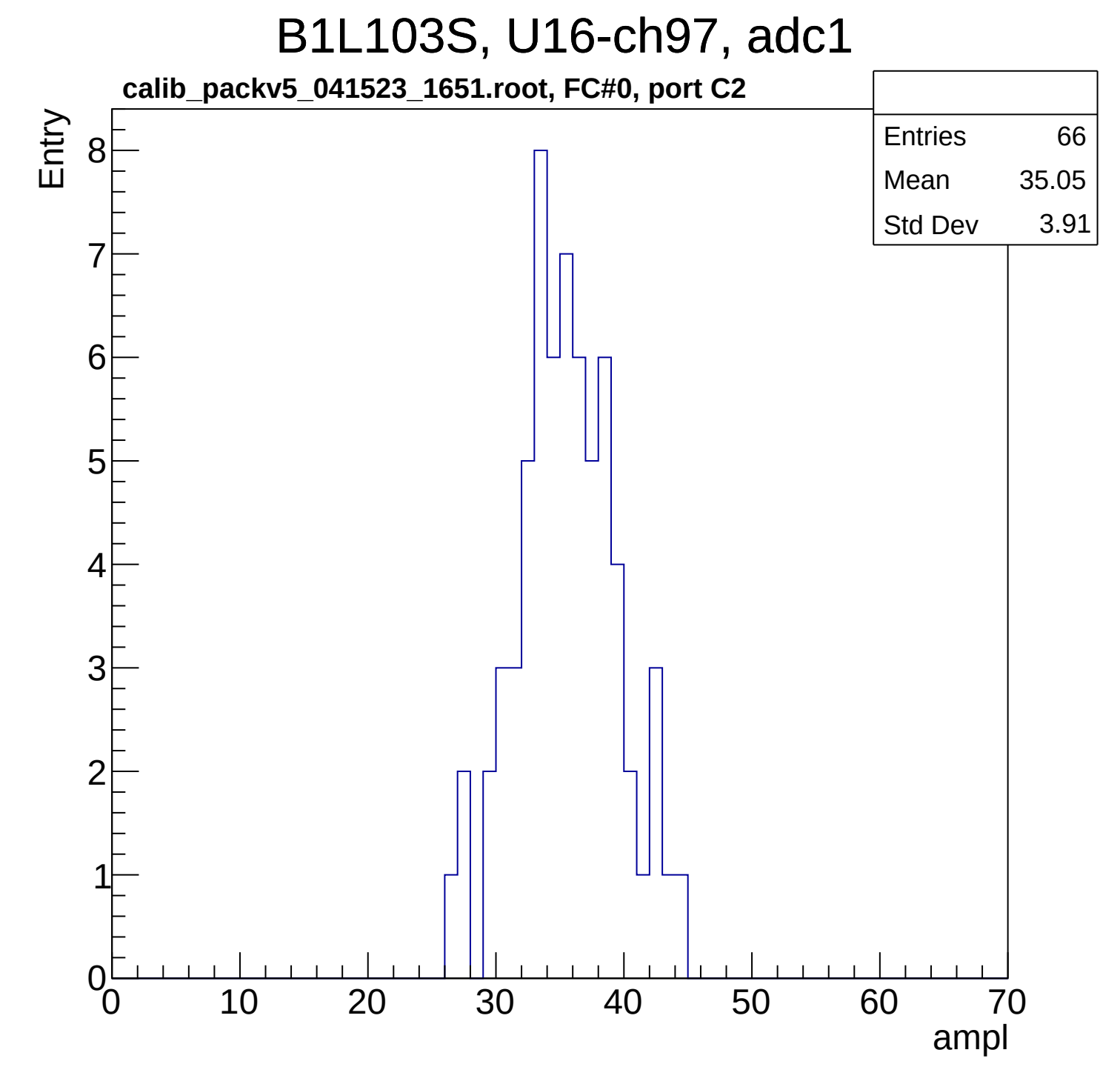
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch96, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 57.46
Std Dev 8.799
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch96, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 61.05
Std Dev 1.905
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U16-ch96, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 8.905
Std Dev 21.81
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch97, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 24.31
Std Dev 10.68
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U16-ch97, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 35.05
Std Dev 3.91
Entry
ampl
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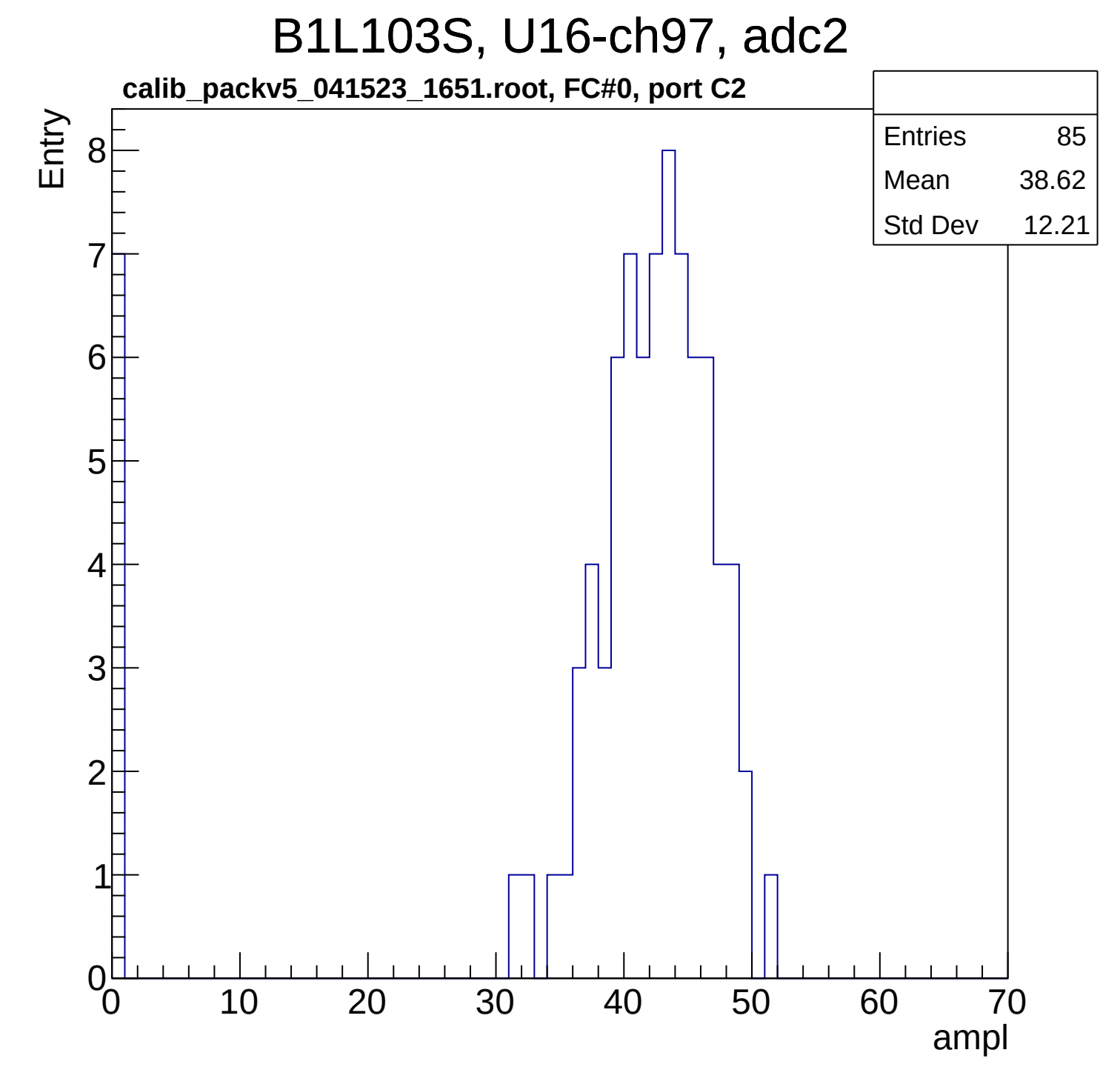
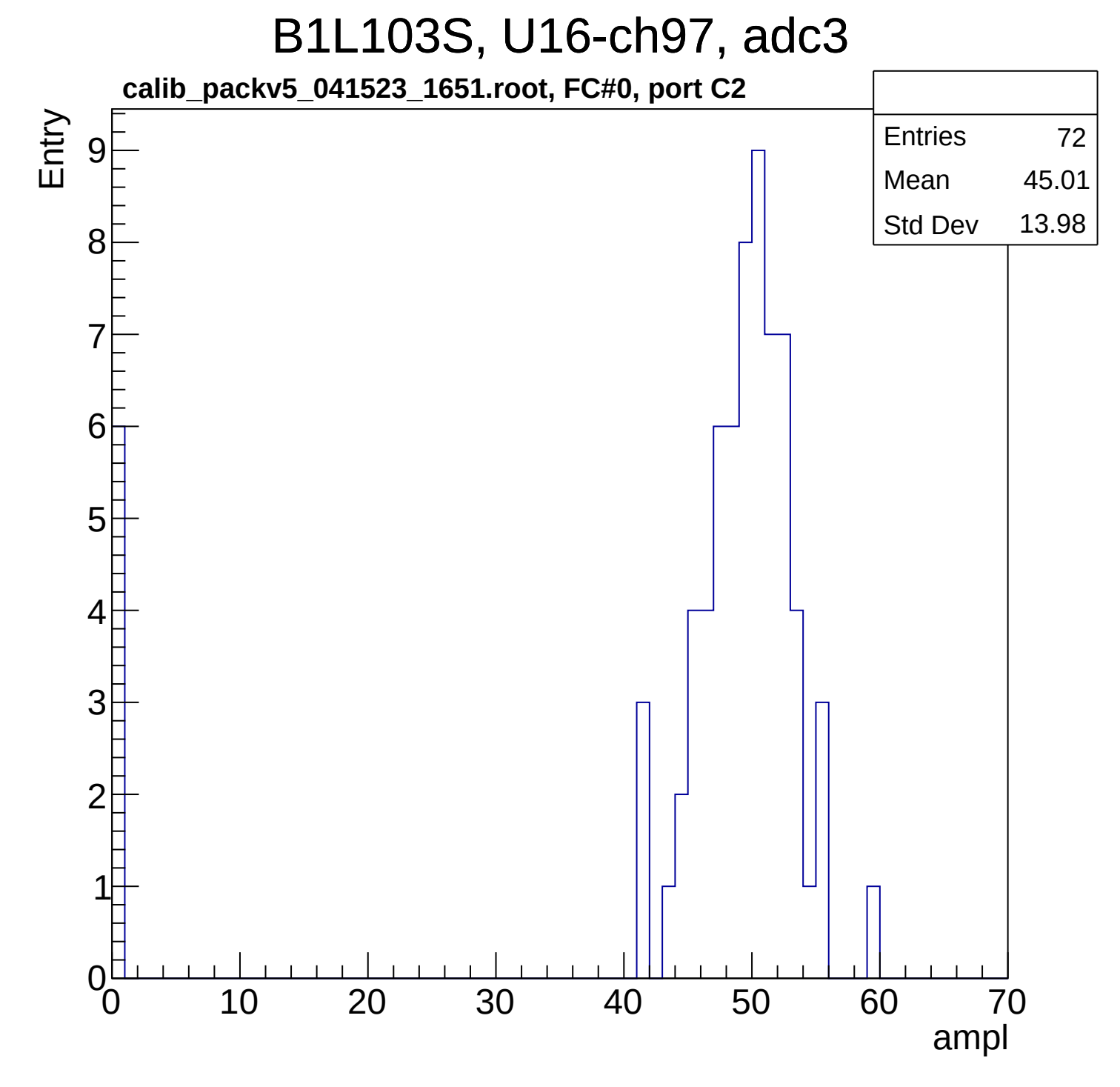
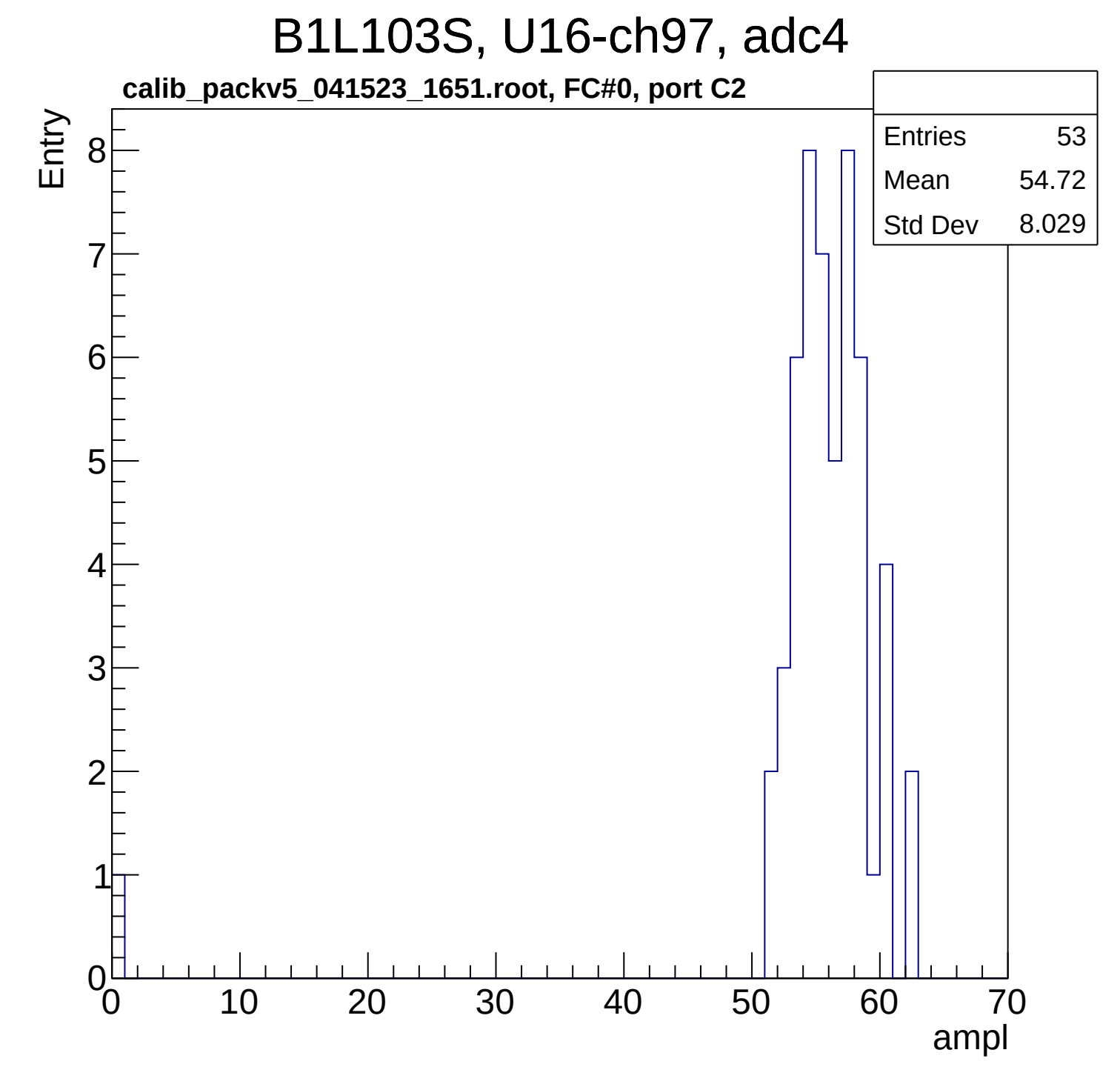
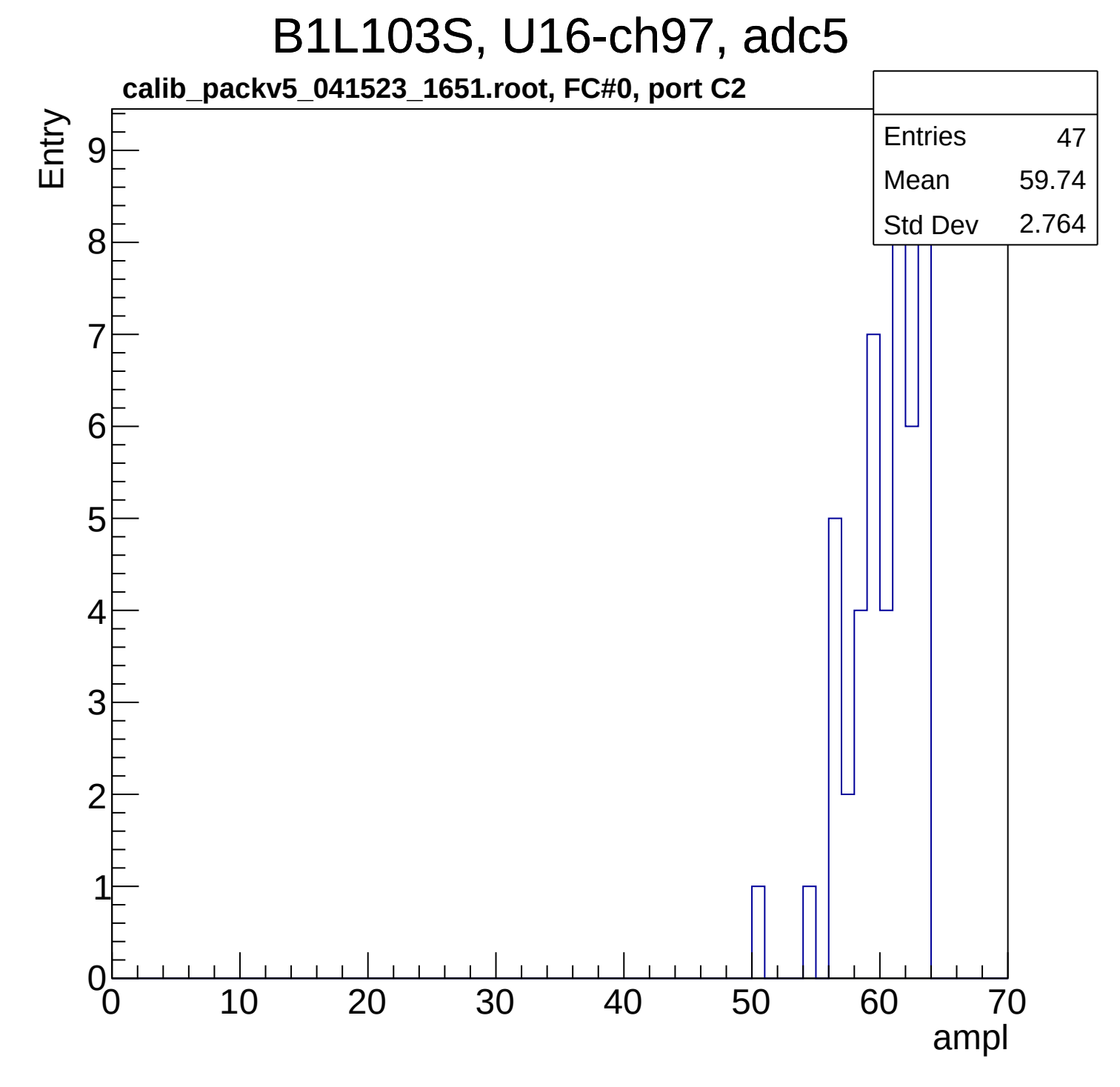
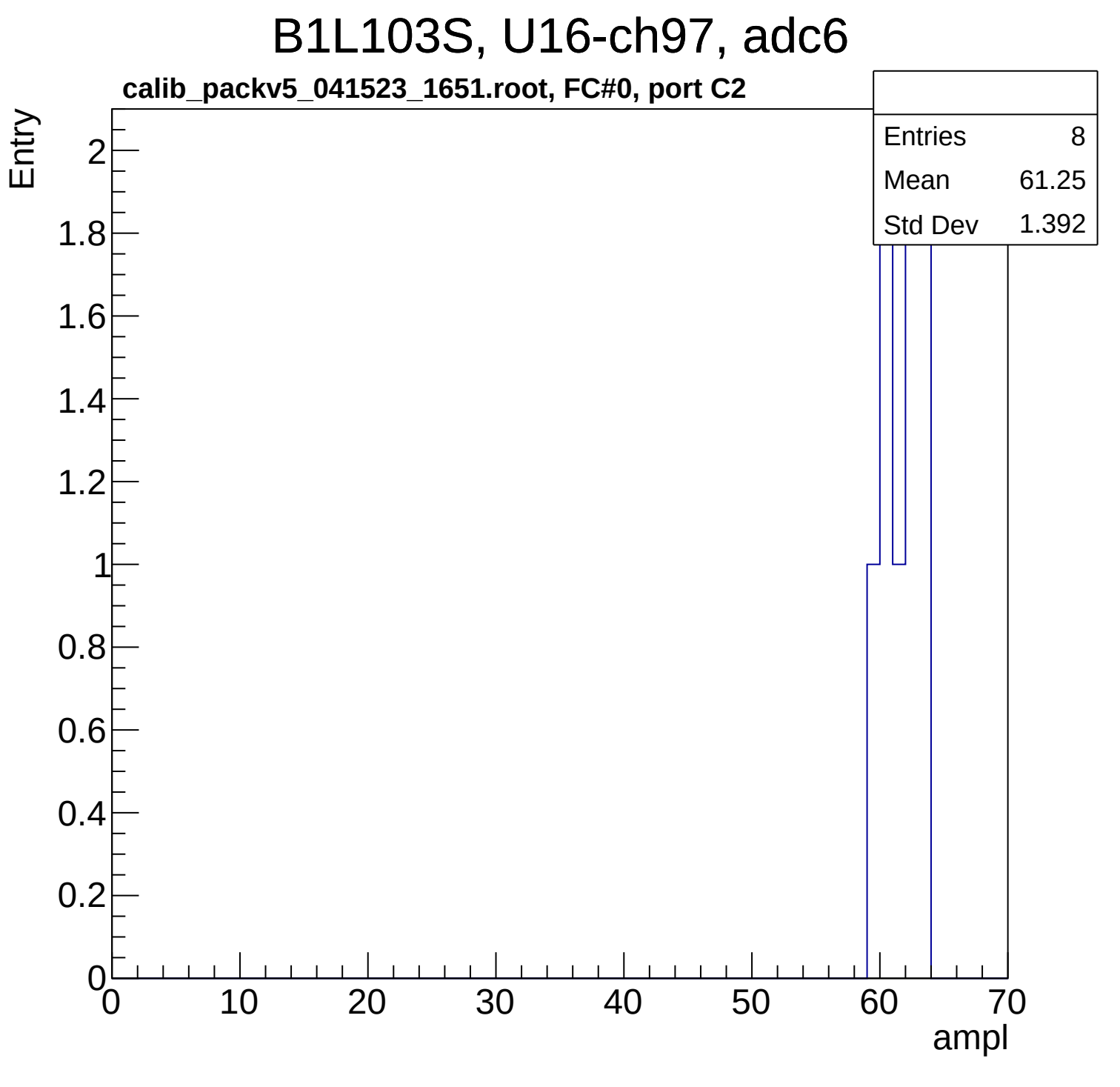
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

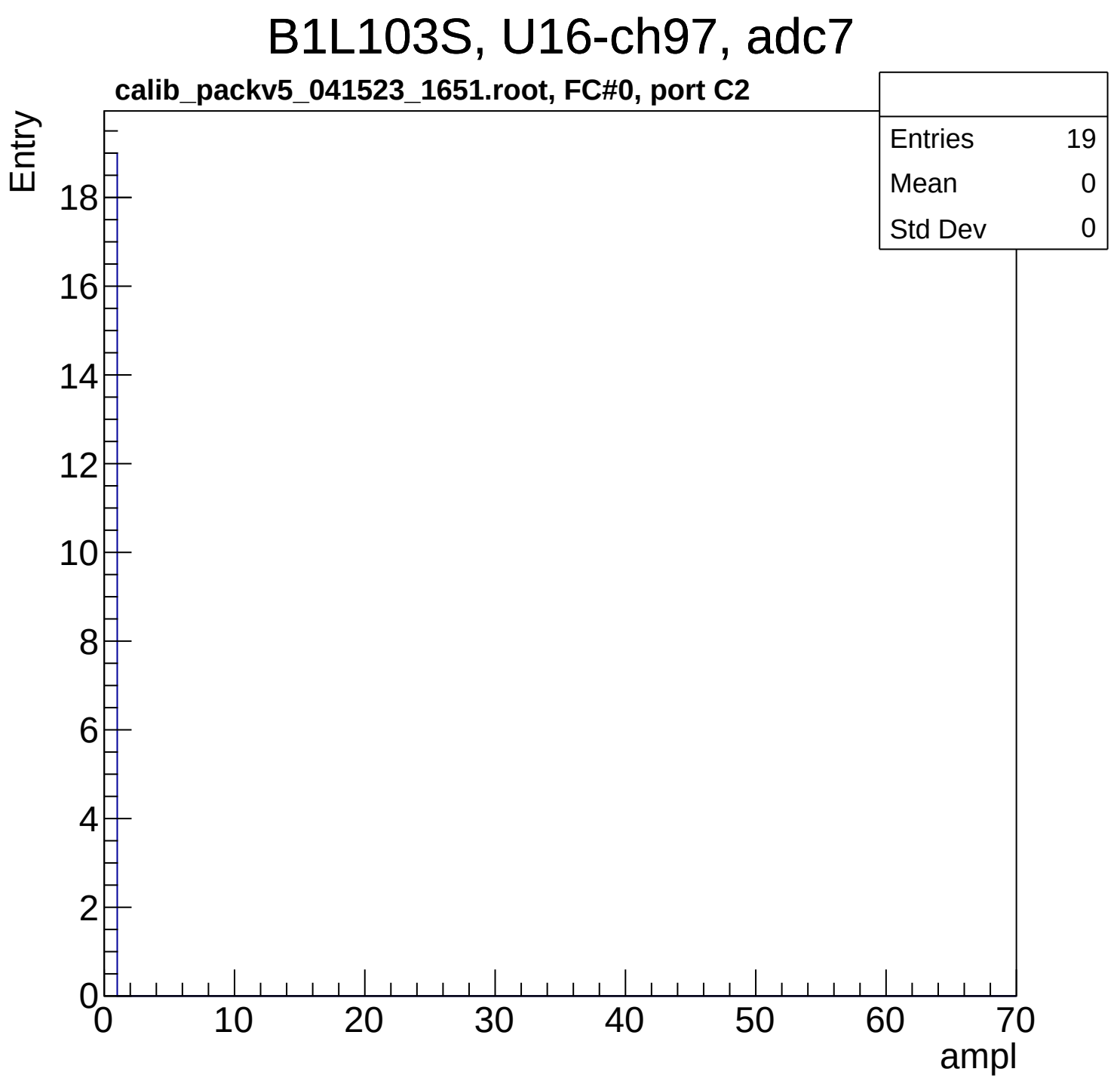

B1L103S, U16-ch97, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 38.62
Std Dev 12.21
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

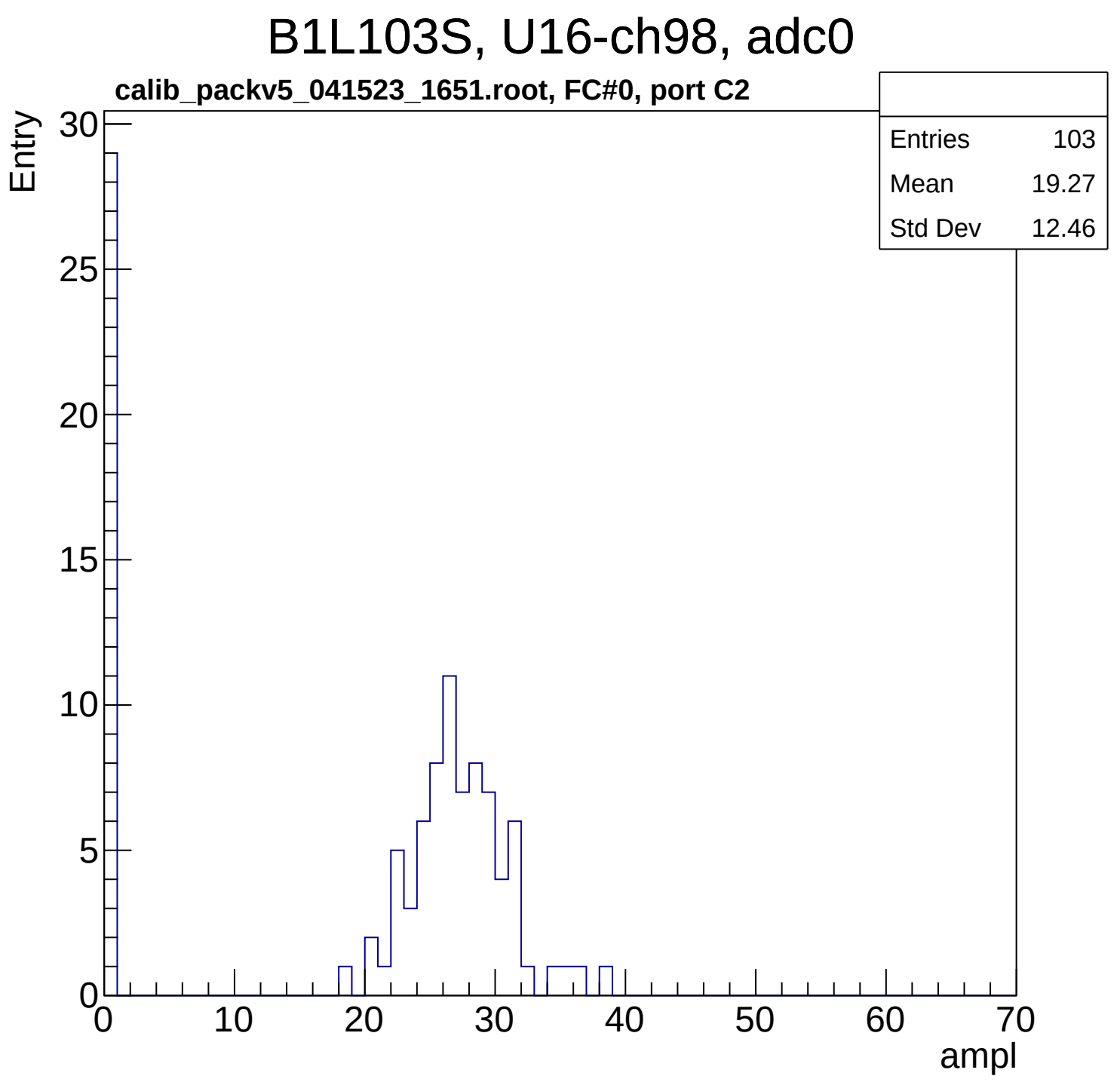

B1L103S, U16-ch97, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 45.01
Std Dev 13.98
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch97, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 54.72
Std Dev 8.029
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch97, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 59.74
Std Dev 2.764
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch97, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.25
Std Dev 1.392
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U16-ch97, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch98, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 19.27
Std Dev 12.46
Entry
ampl
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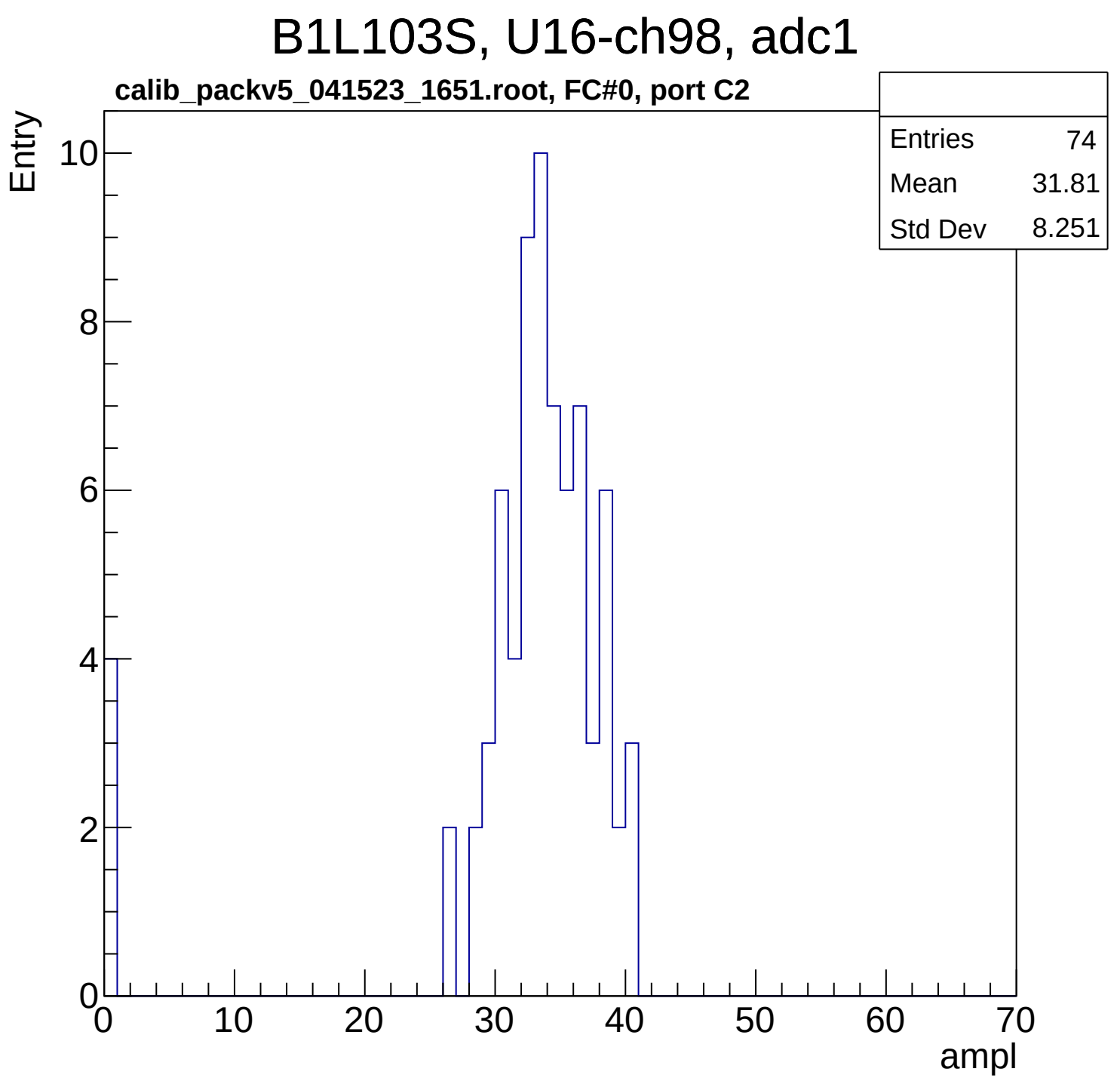
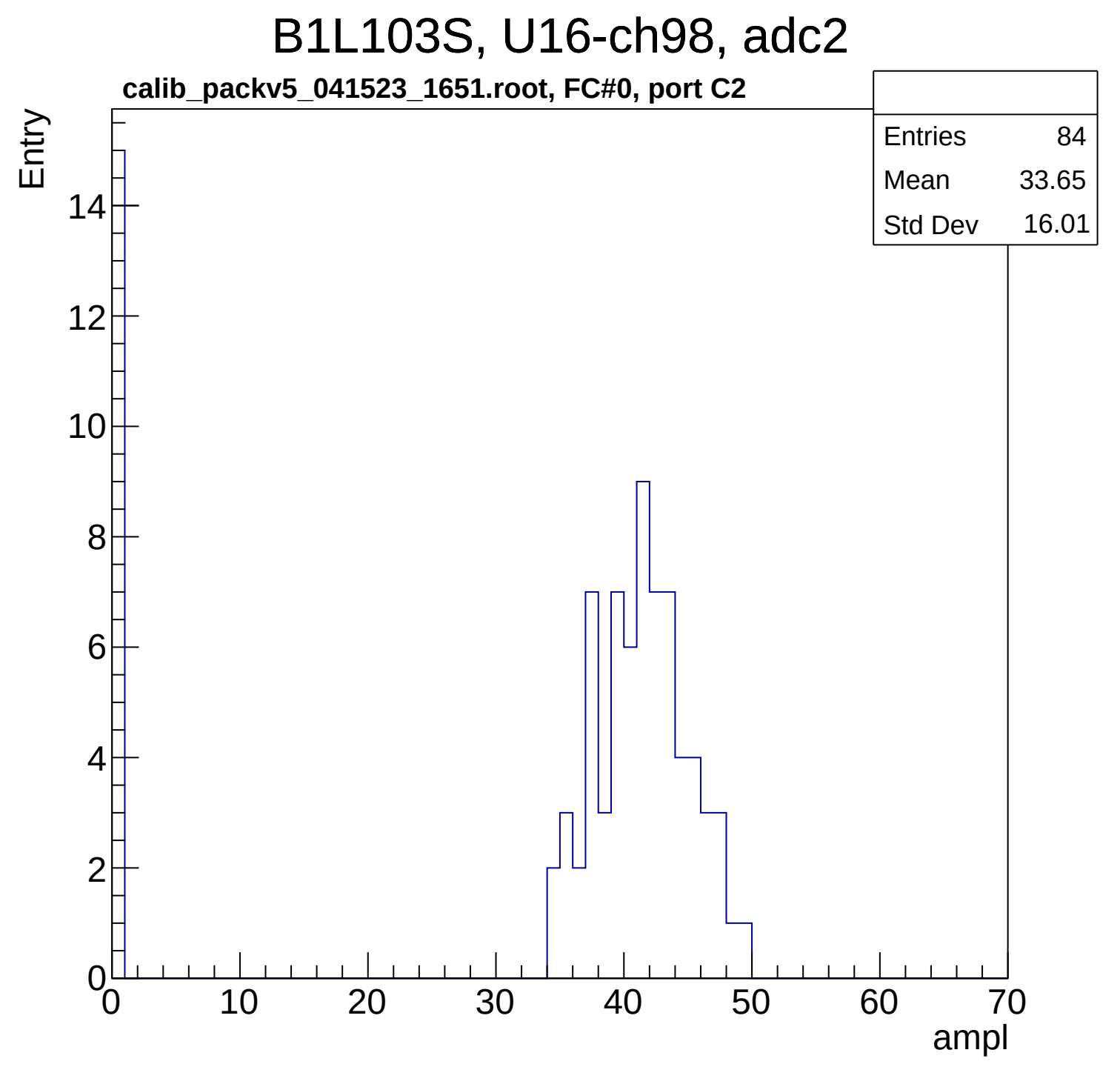
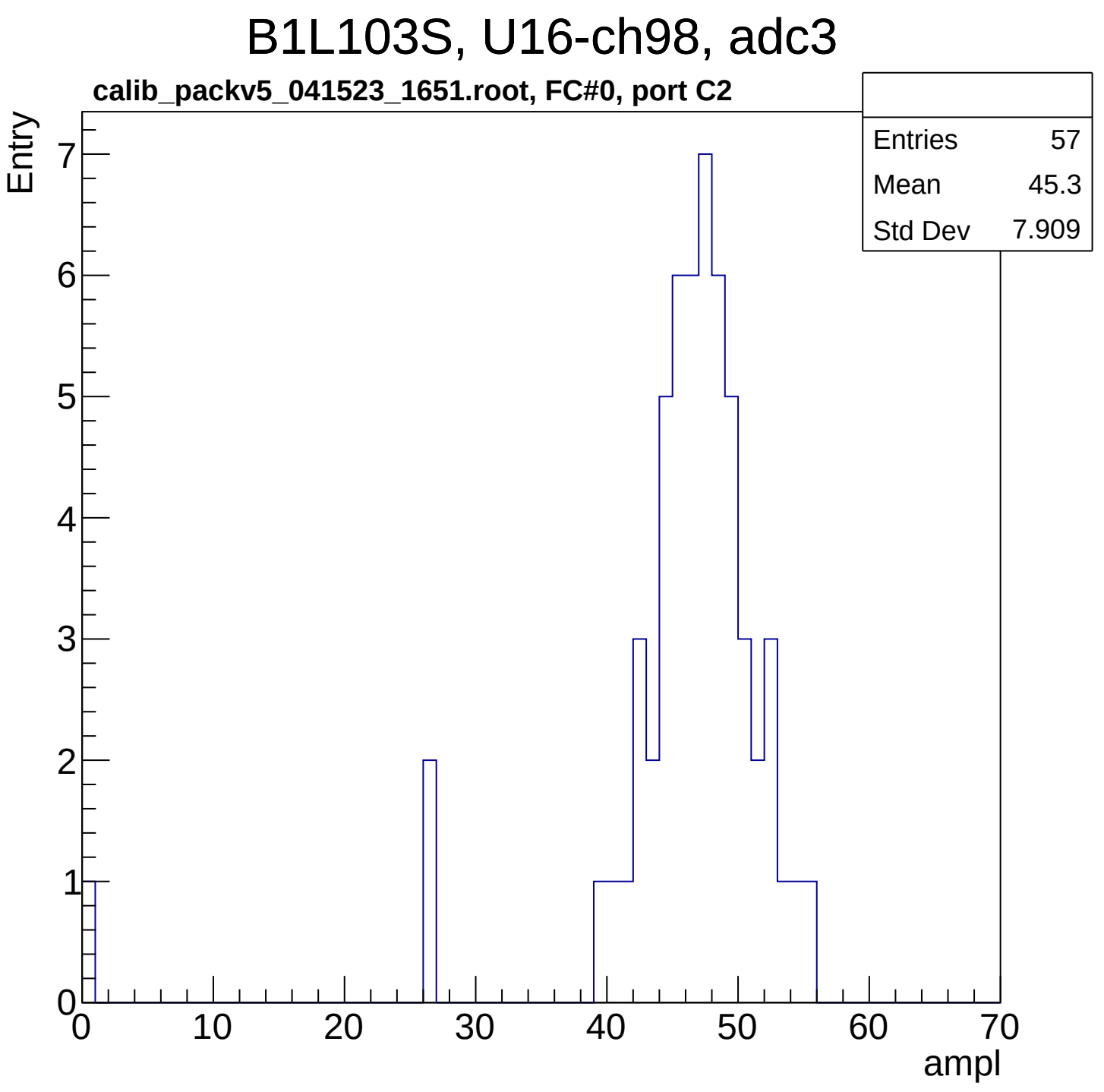
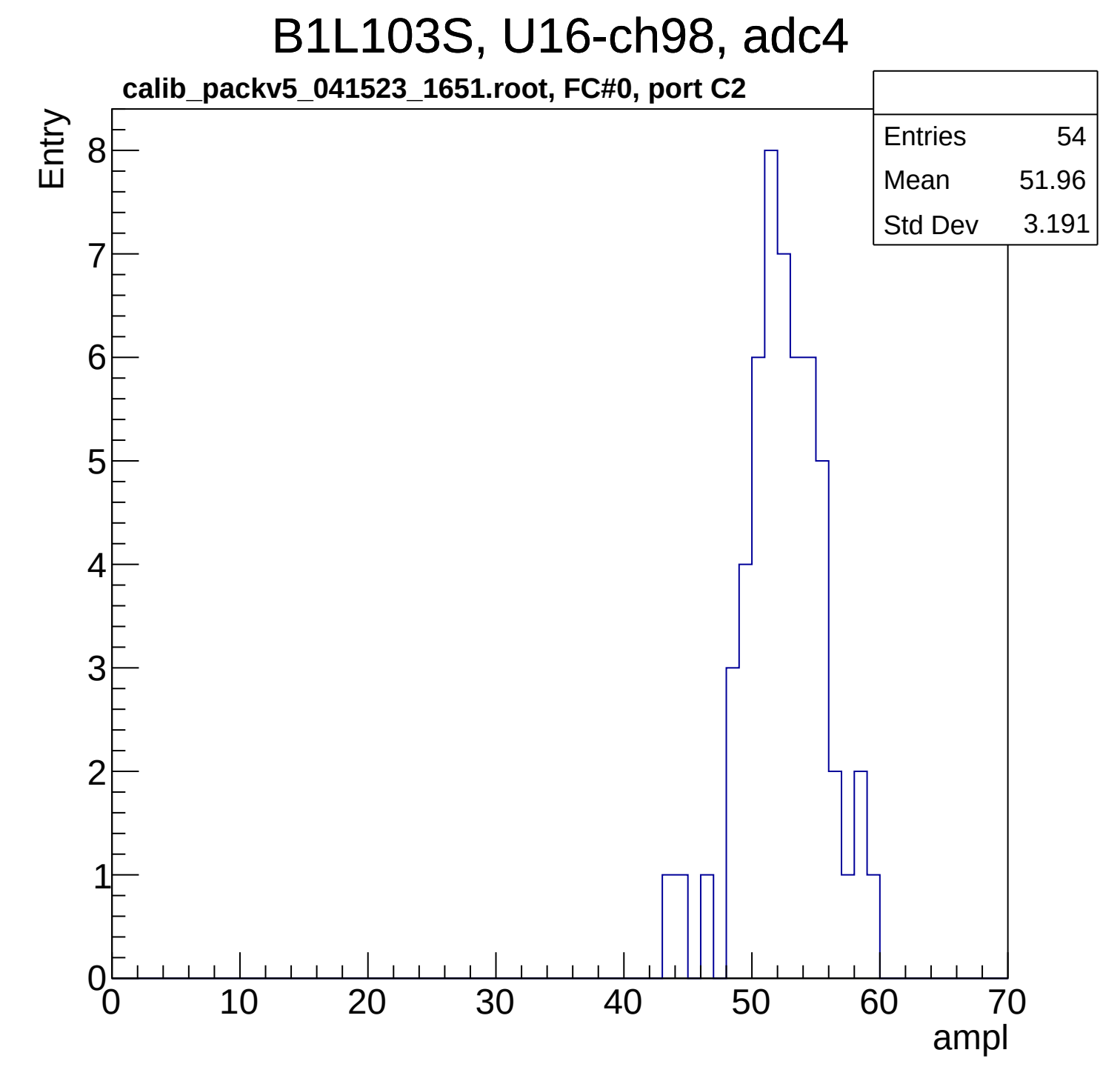
5
10
15
20
25
30
0
10
20
30
40
50
60
70


B1L103S, U16-ch98, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 31.81
Std Dev 8.251
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch98, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 33.65
Std Dev 16.01
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch98, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 45.3
Std Dev 7.909
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch98, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 51.96
Std Dev 3.191
Entry
ampl
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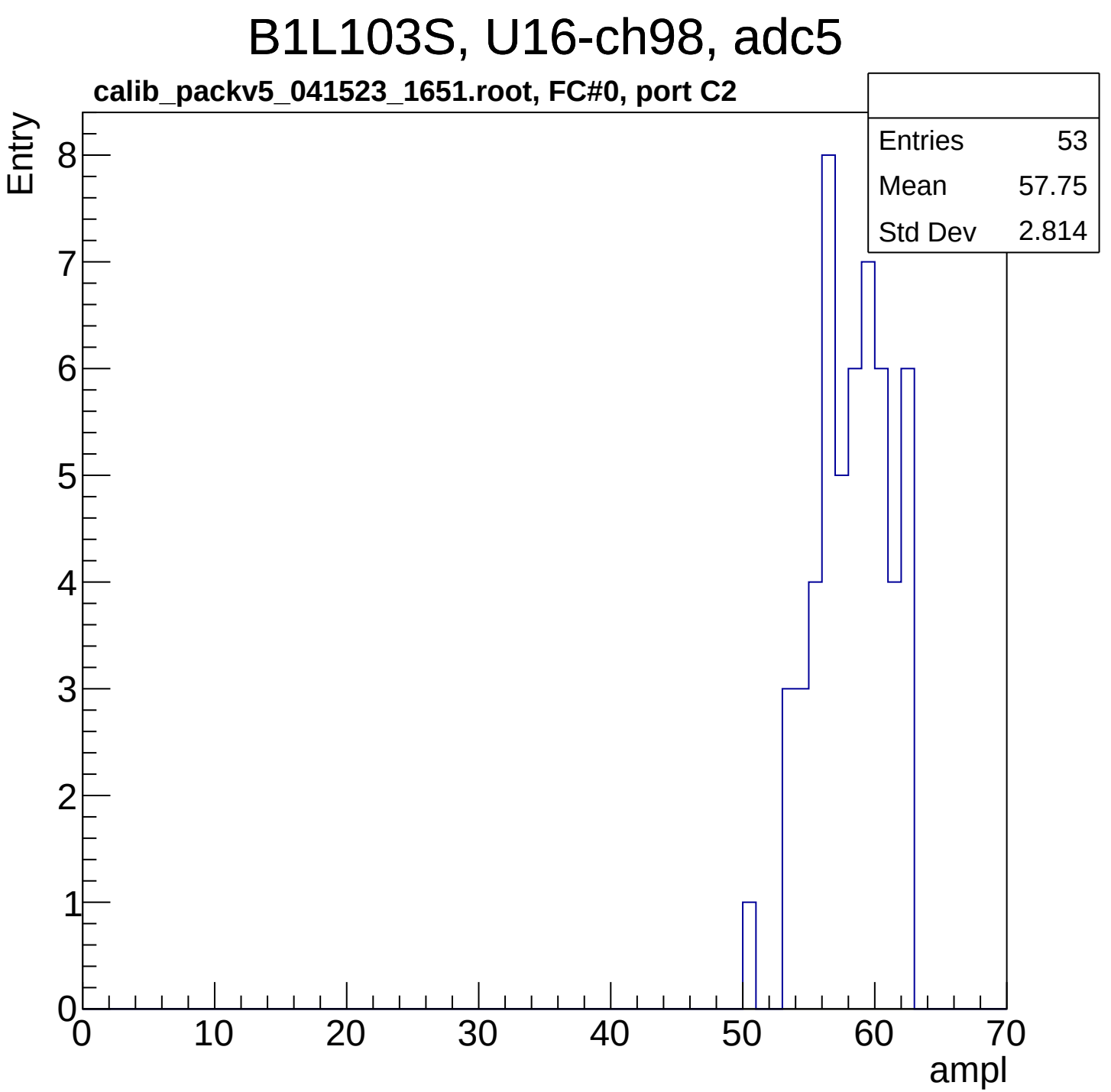
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch98, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 57.75
Std Dev 2.814
Entry
ampl
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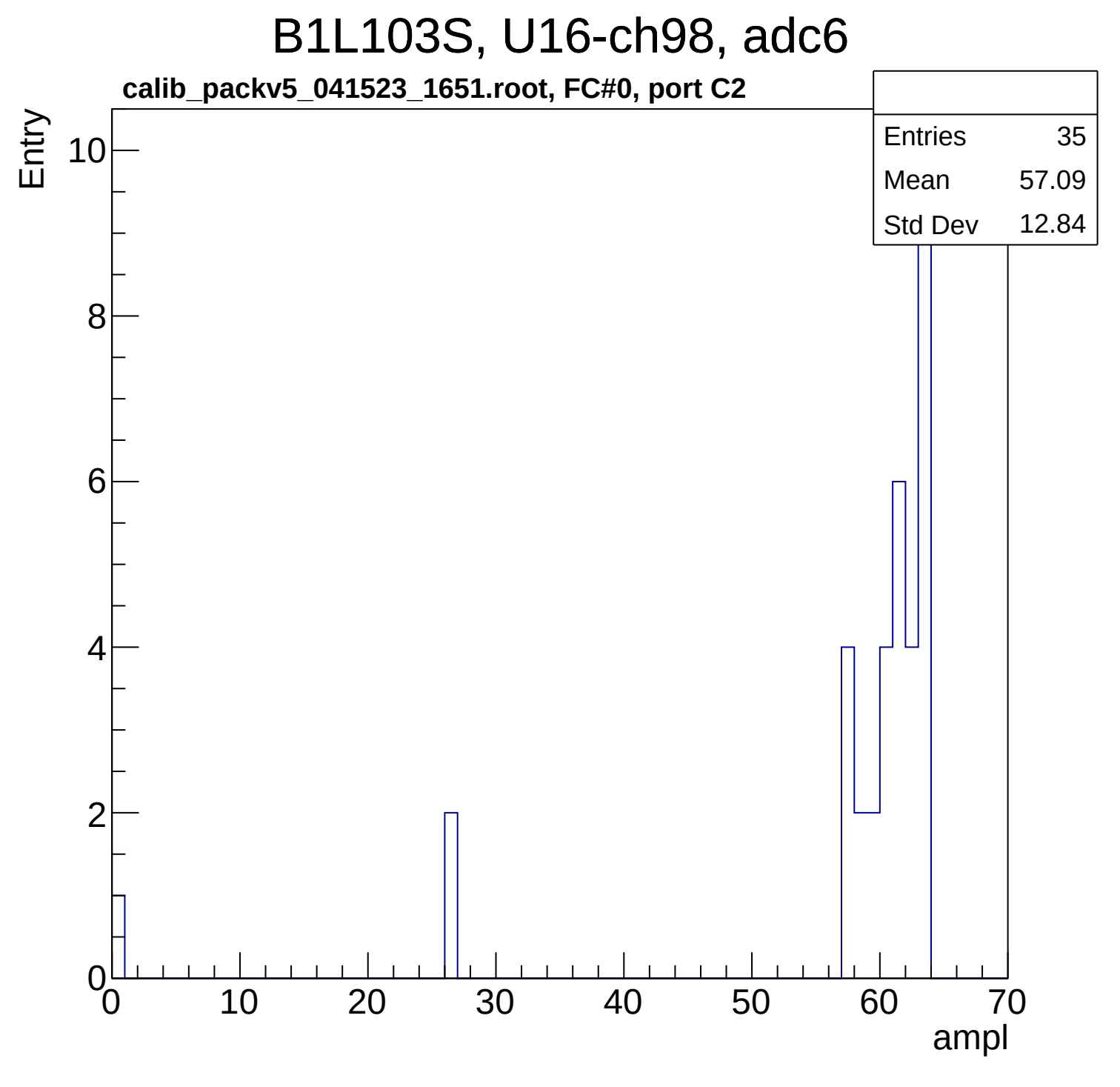
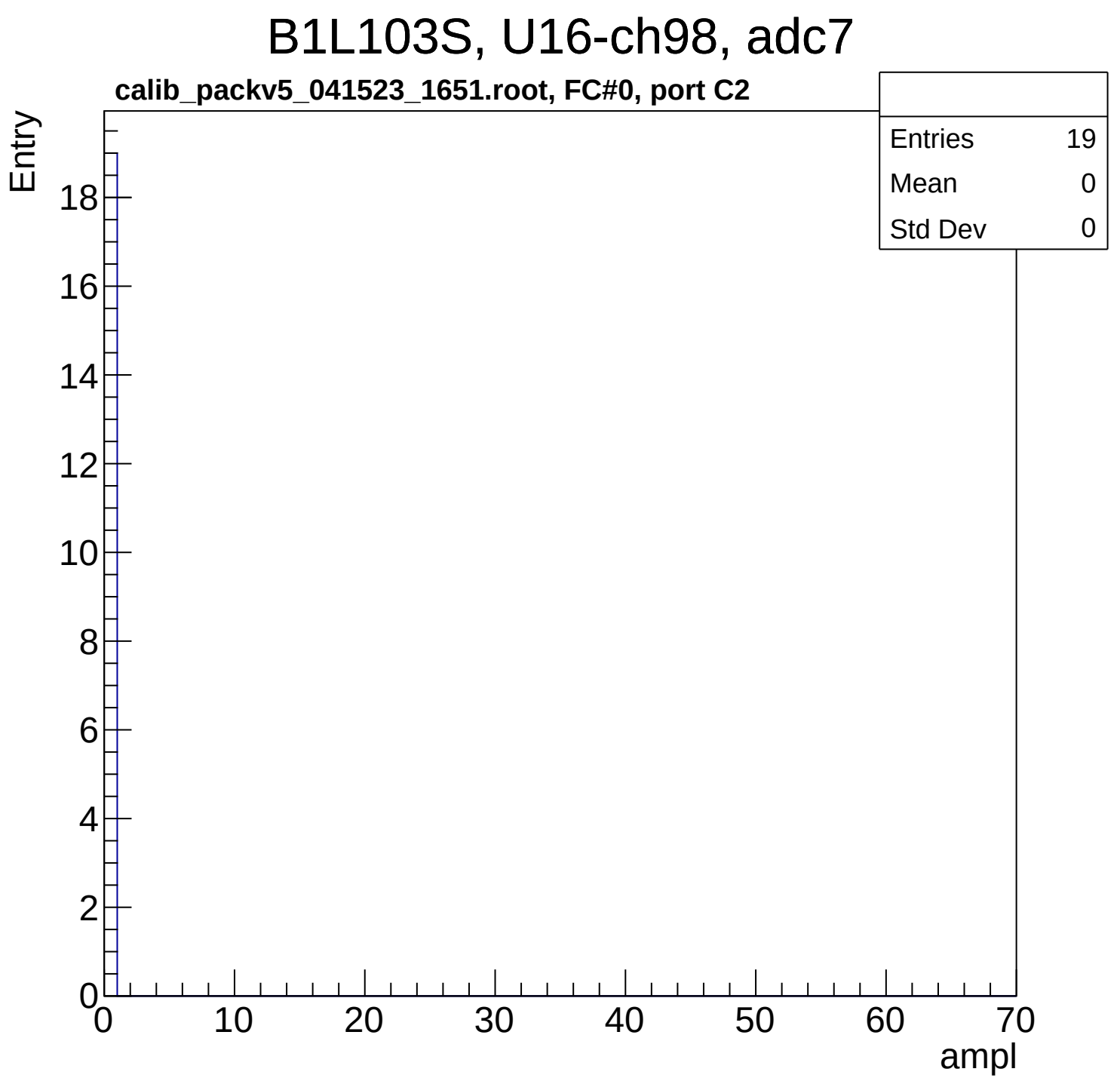
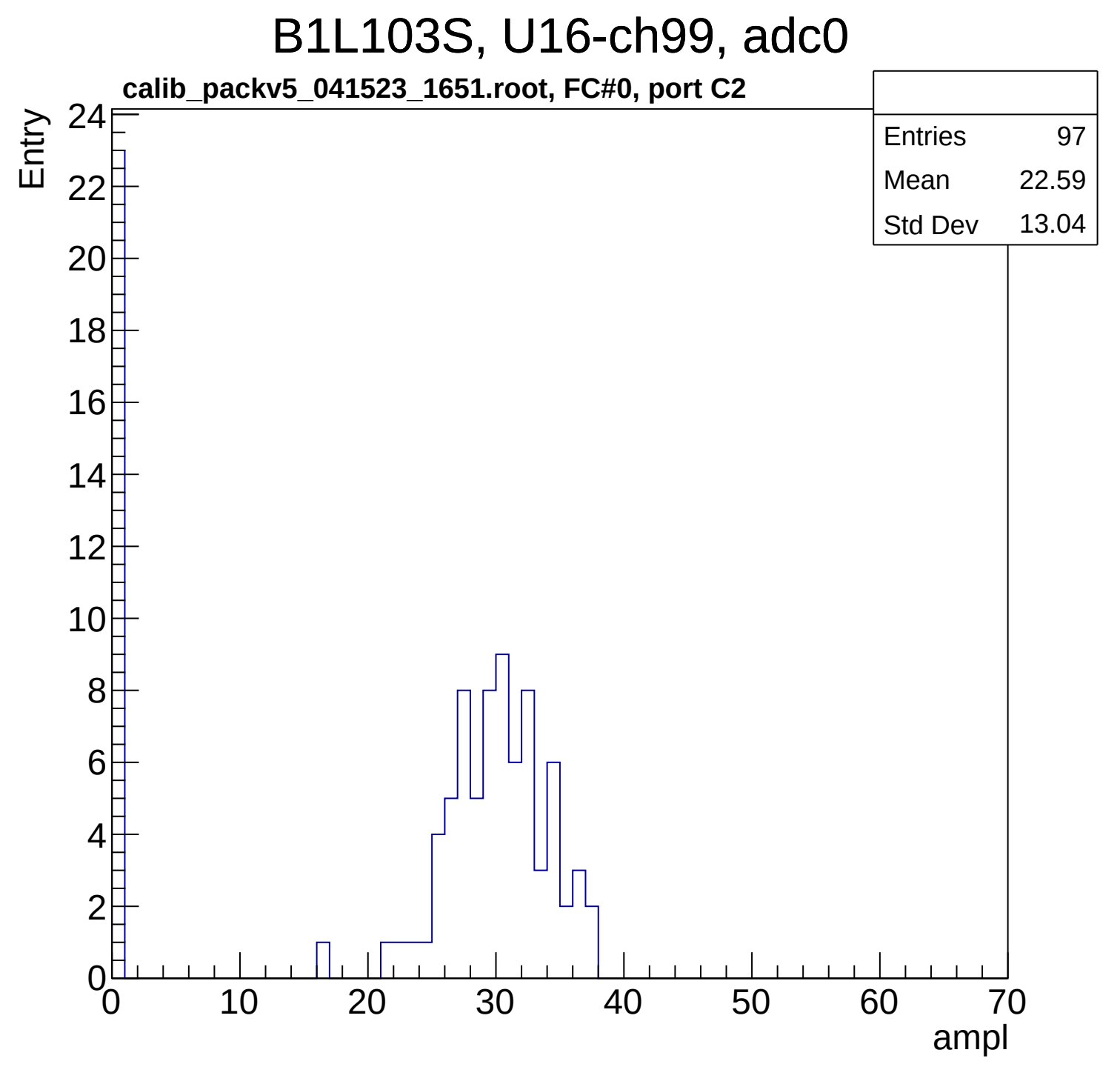
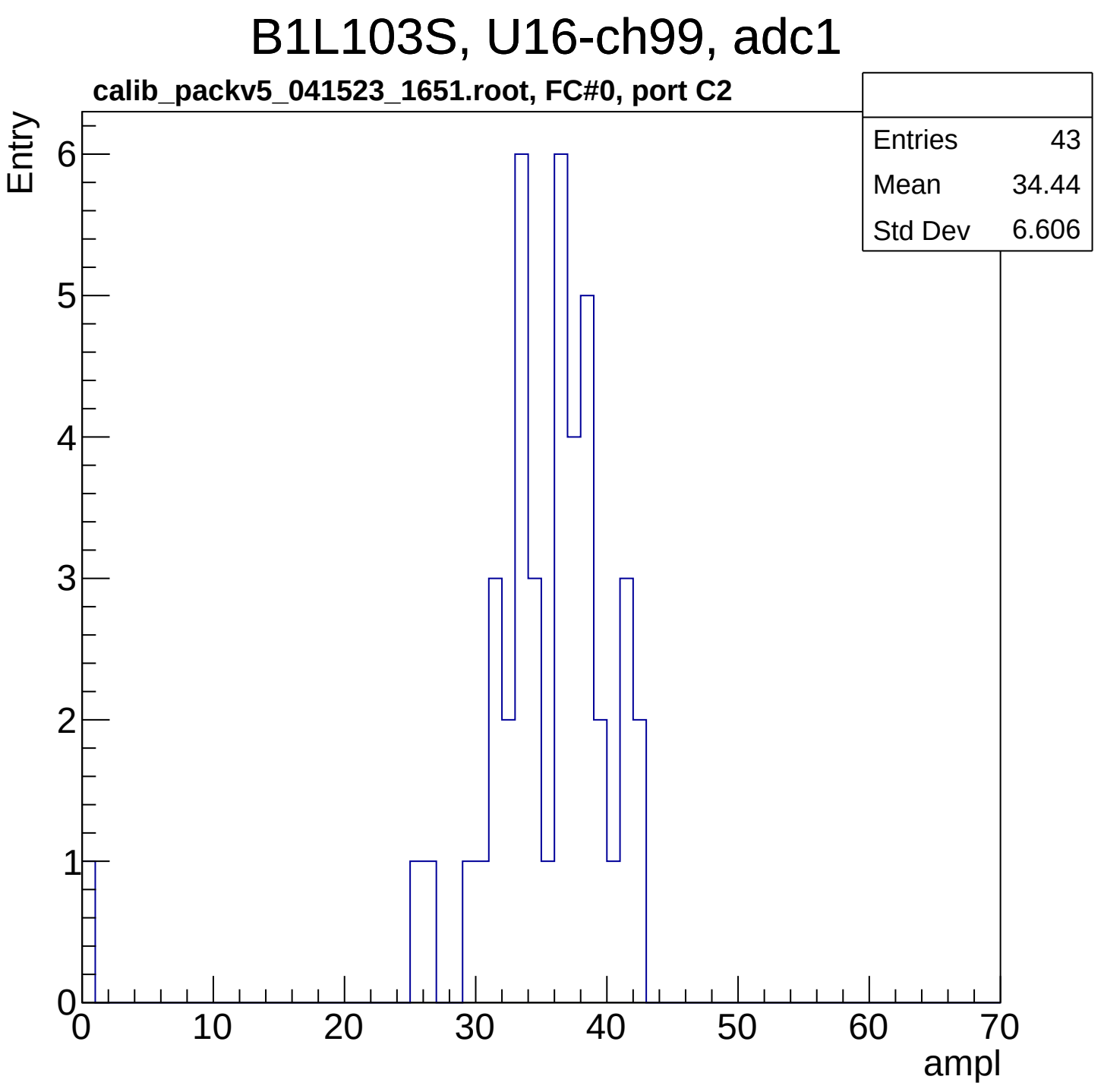
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch98, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 57.09
Std Dev 12.84
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch98, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch99, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 22.59
Std Dev 13.04
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70


B1L103S, U16-ch99, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 34.44
Std Dev 6.606
Entry
ampl
0
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2
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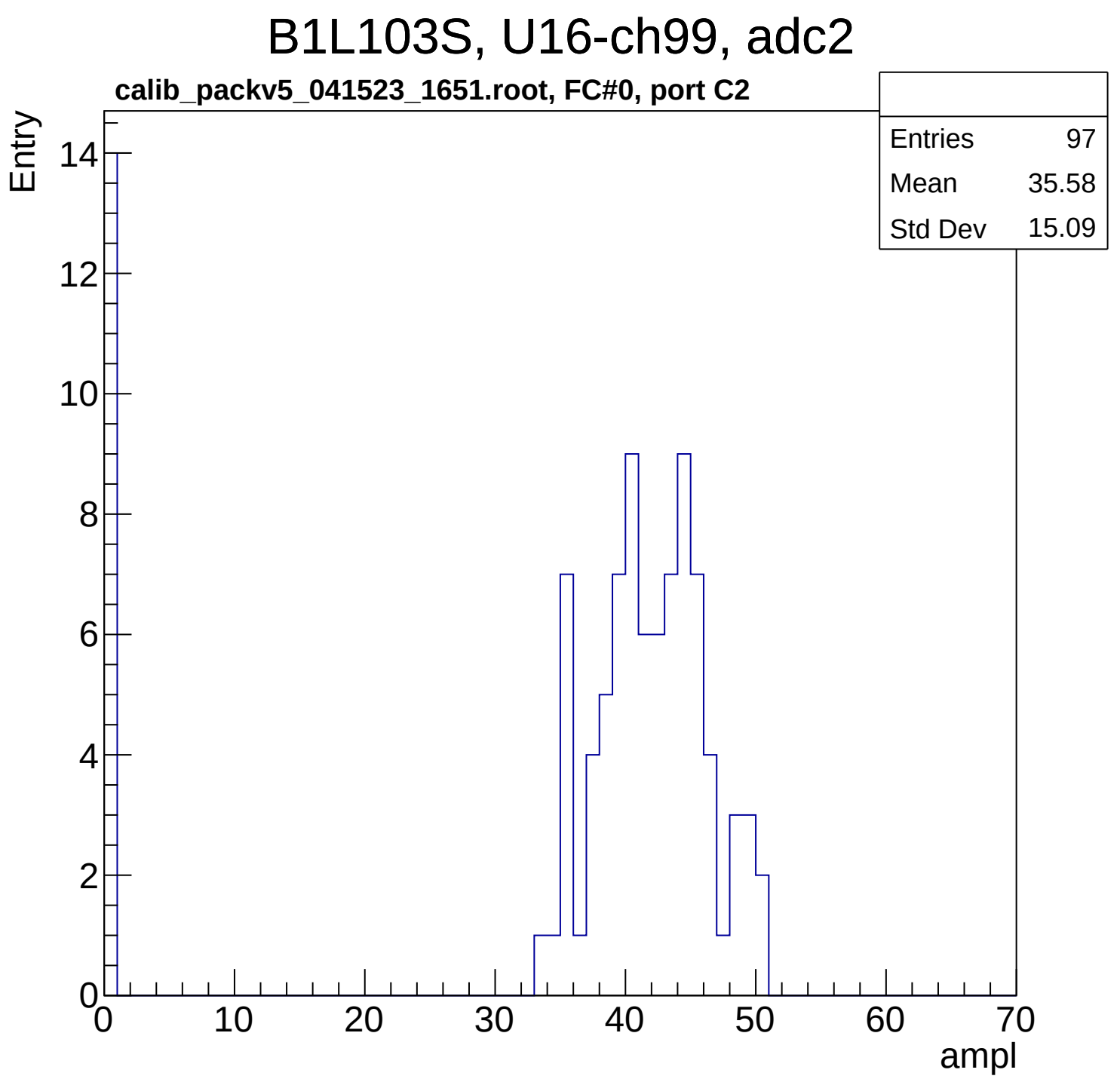
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U16-ch99, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 35.58
Std Dev 15.09
Entry
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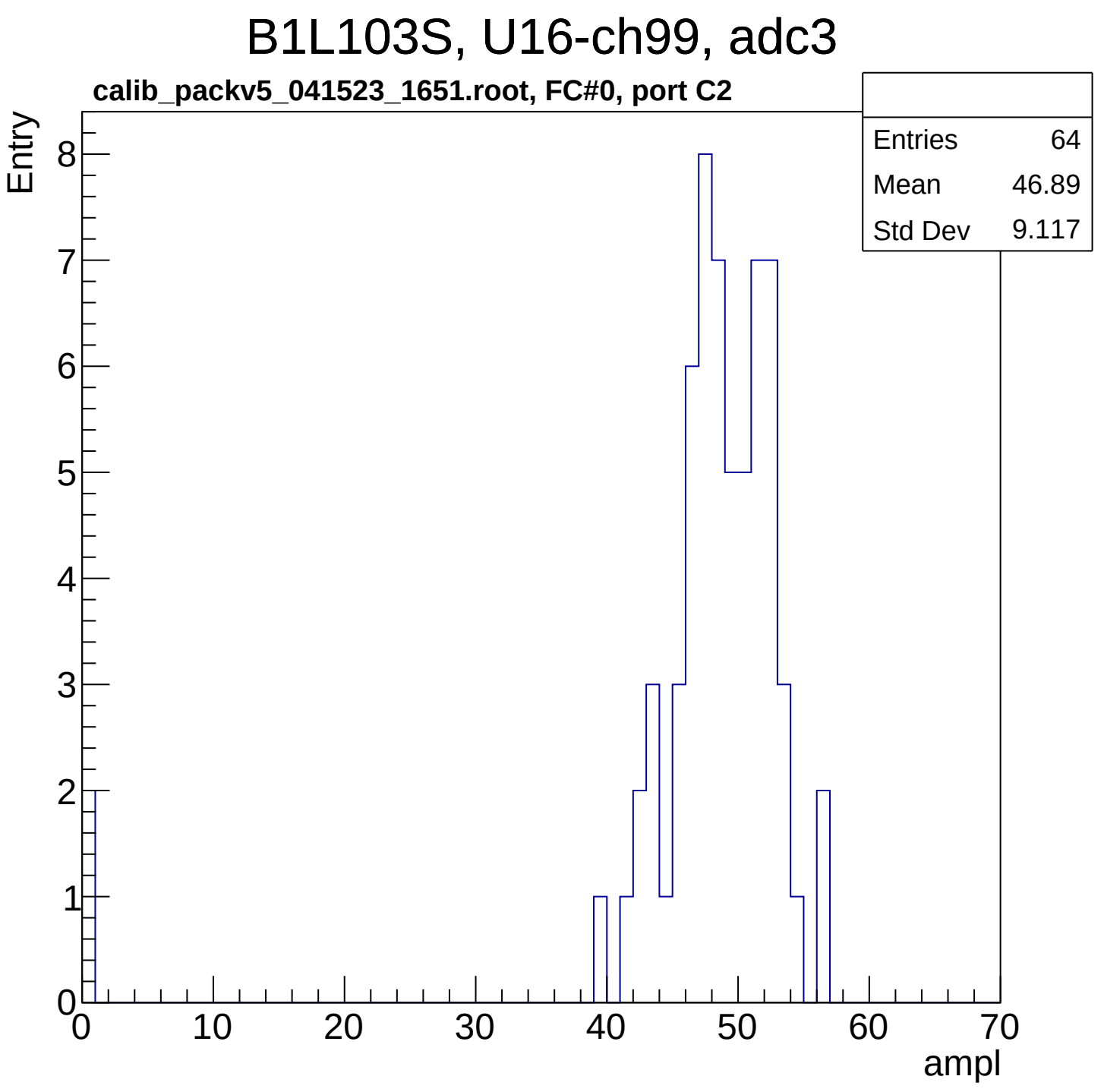
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch99, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 46.89
Std Dev 9.117
Entry
ampl
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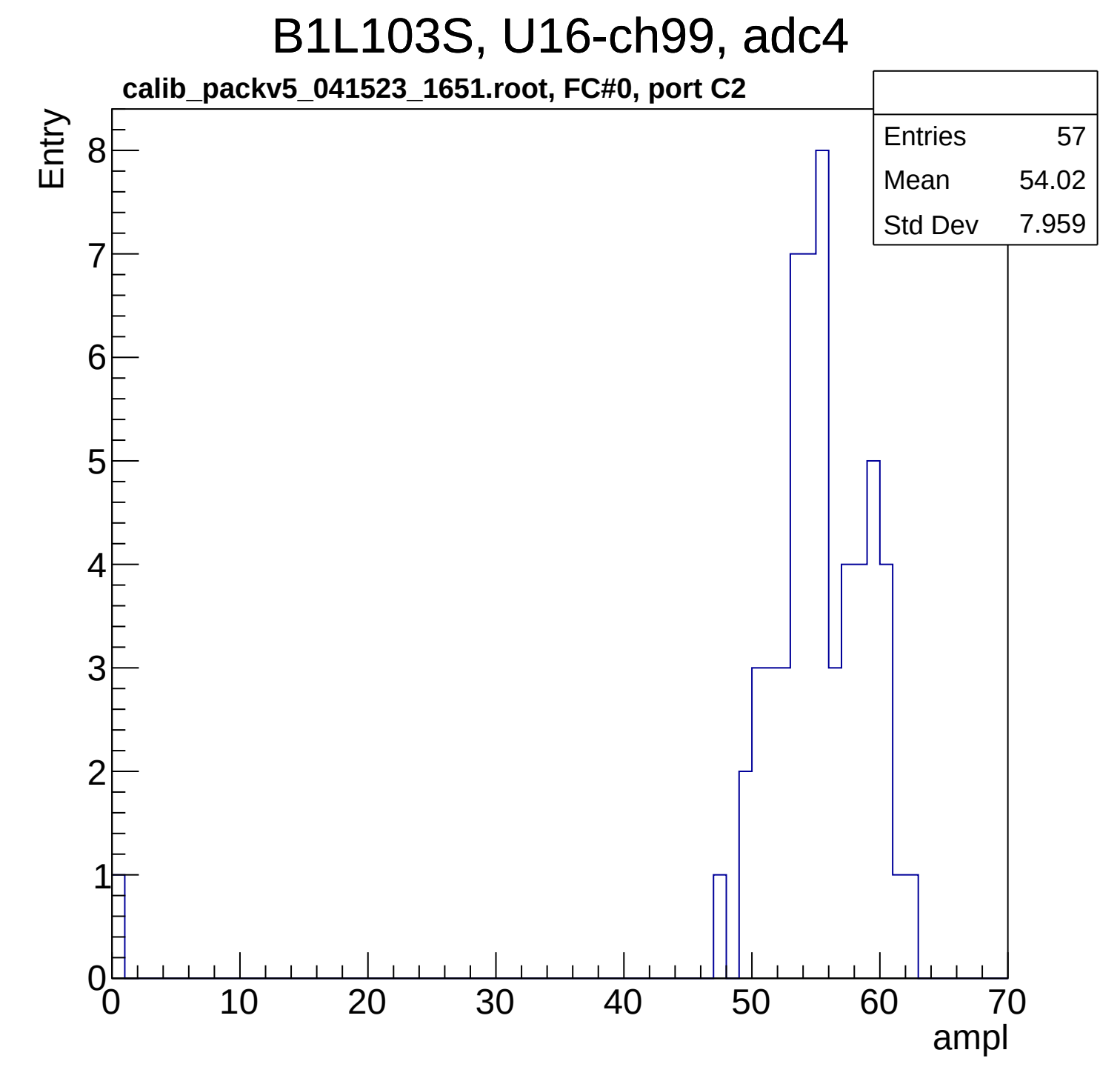
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch99, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 54.02
Std Dev 7.959
Entry
ampl
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1
2
3
4
5
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7
8
0
10
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30
40
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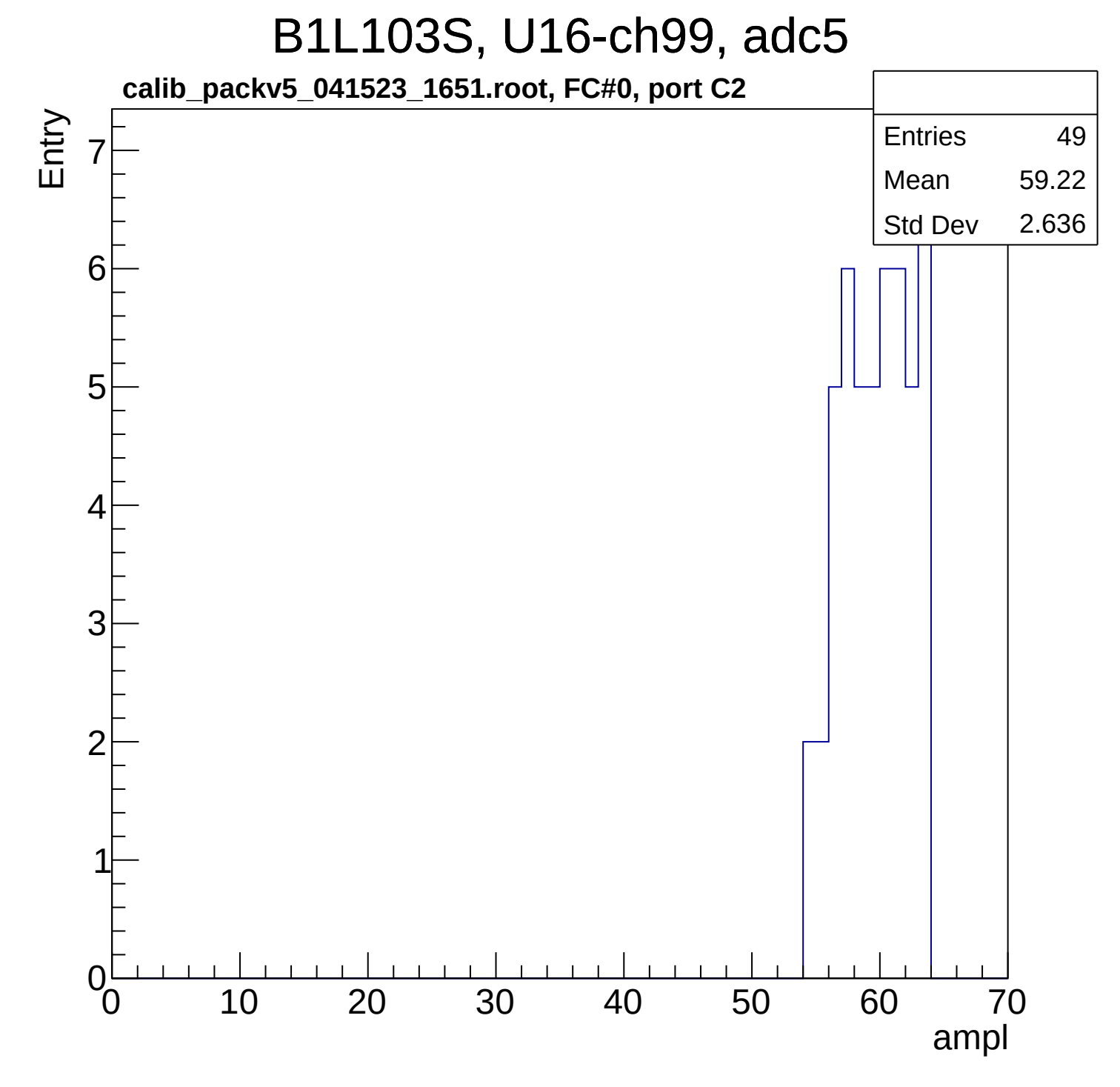
60
70


B1L103S, U16-ch99, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 59.22
Std Dev 2.636
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
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60
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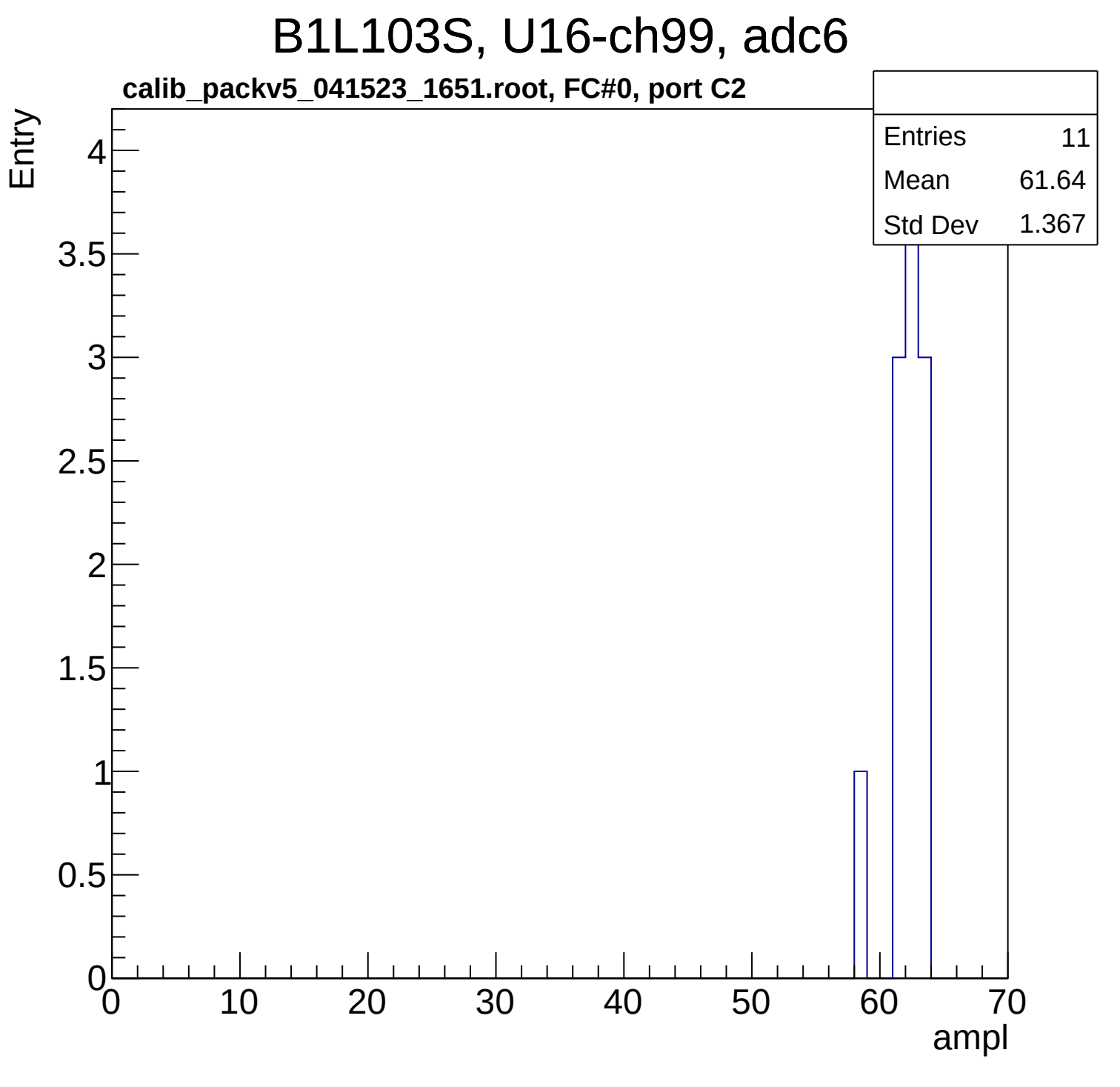
B1L103S, U16-ch99, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.64
Std Dev 1.367
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
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20
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40
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60
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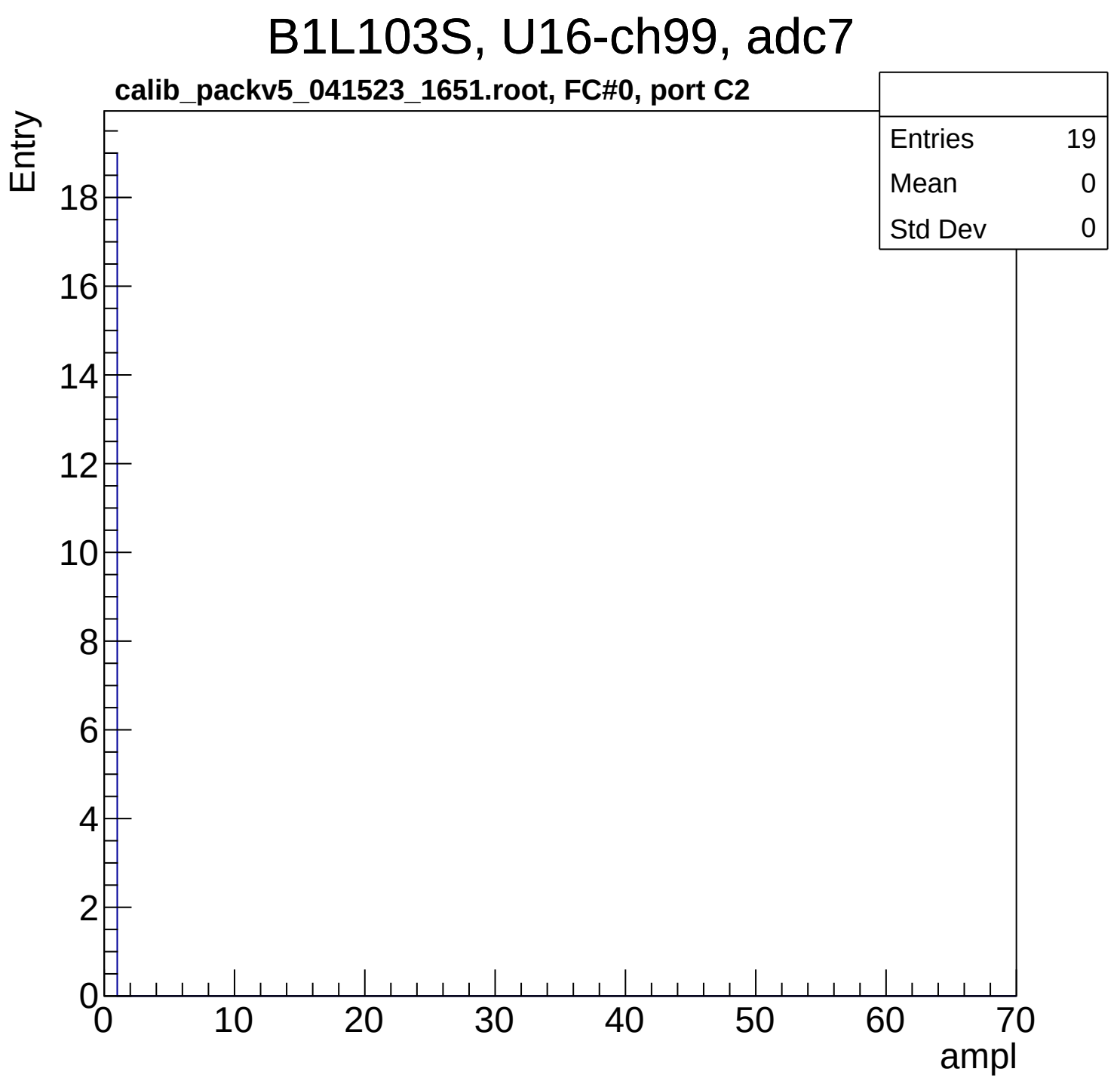
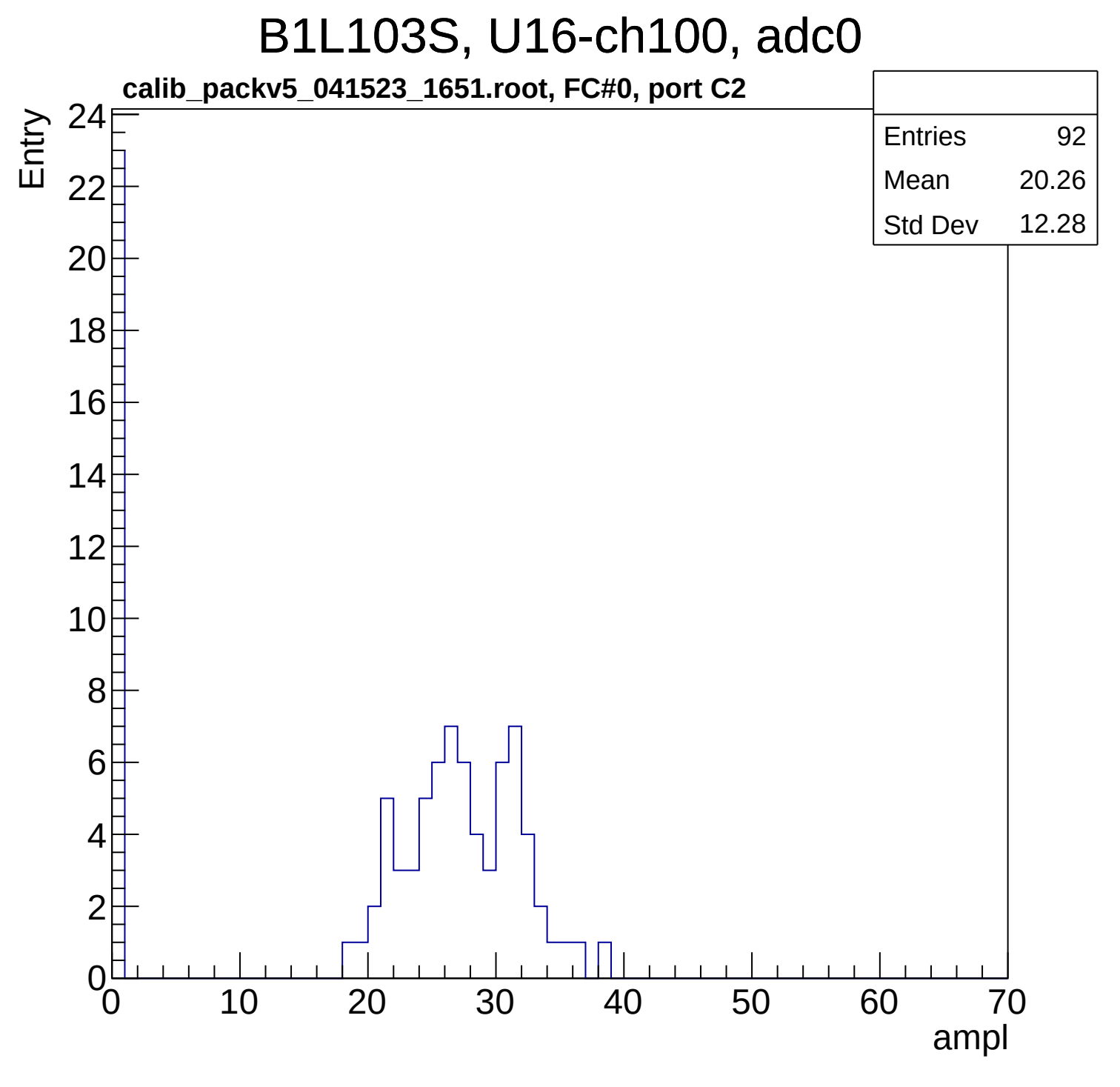
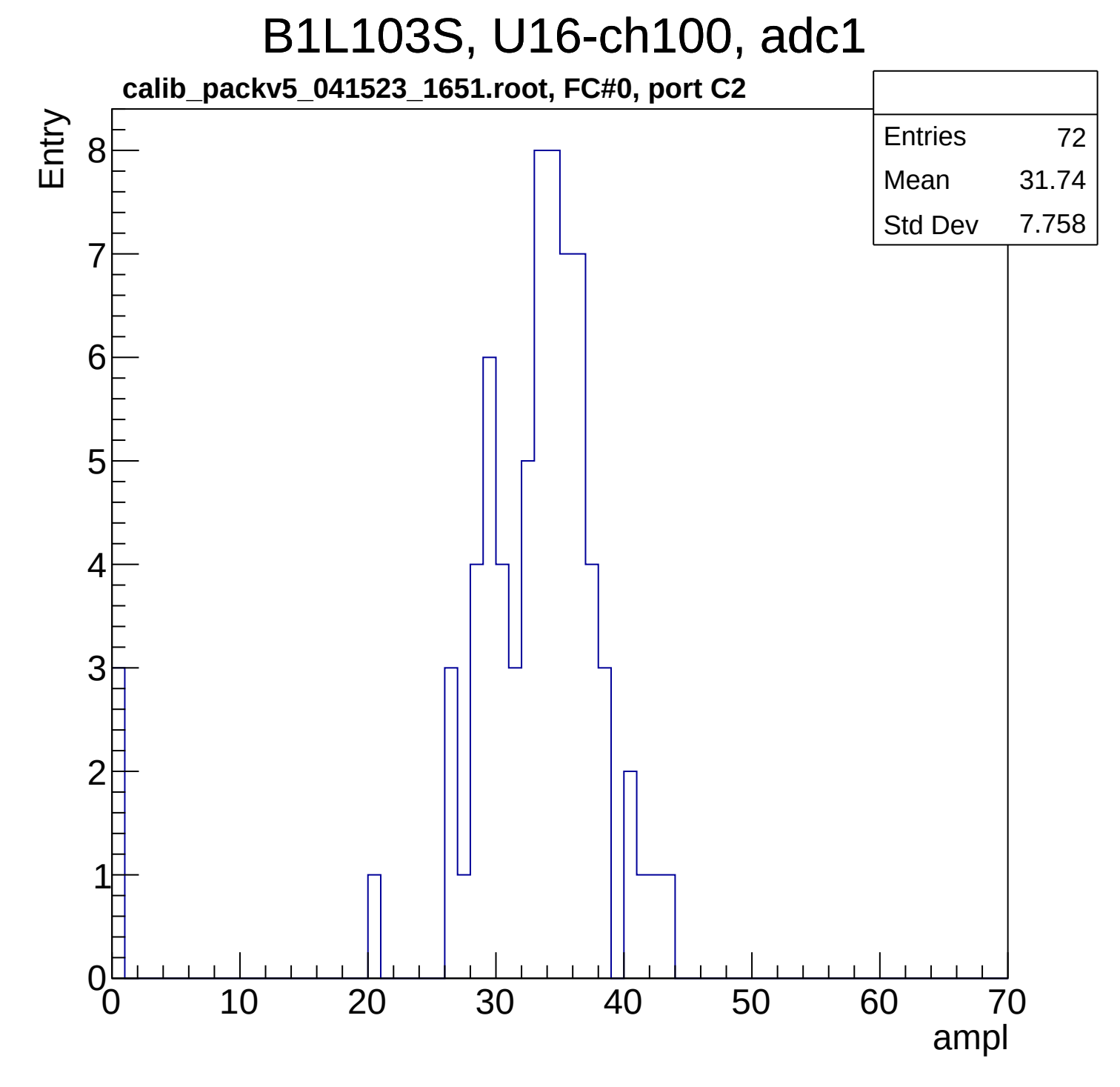

B1L103S, U16-ch99, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch100, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 20.26
Std Dev 12.28
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70


B1L103S, U16-ch100, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 31.74
Std Dev 7.758
Entry
ampl
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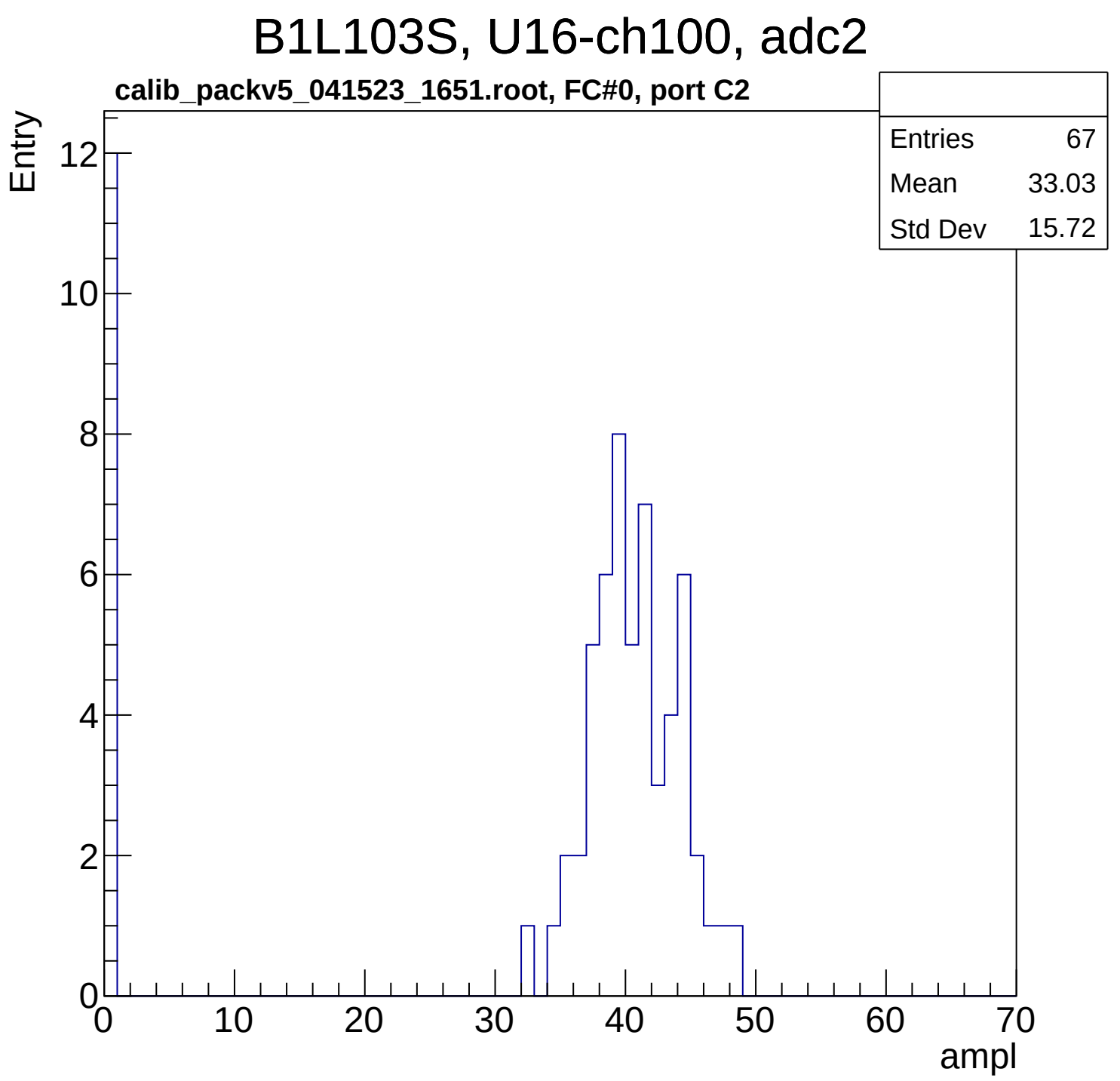
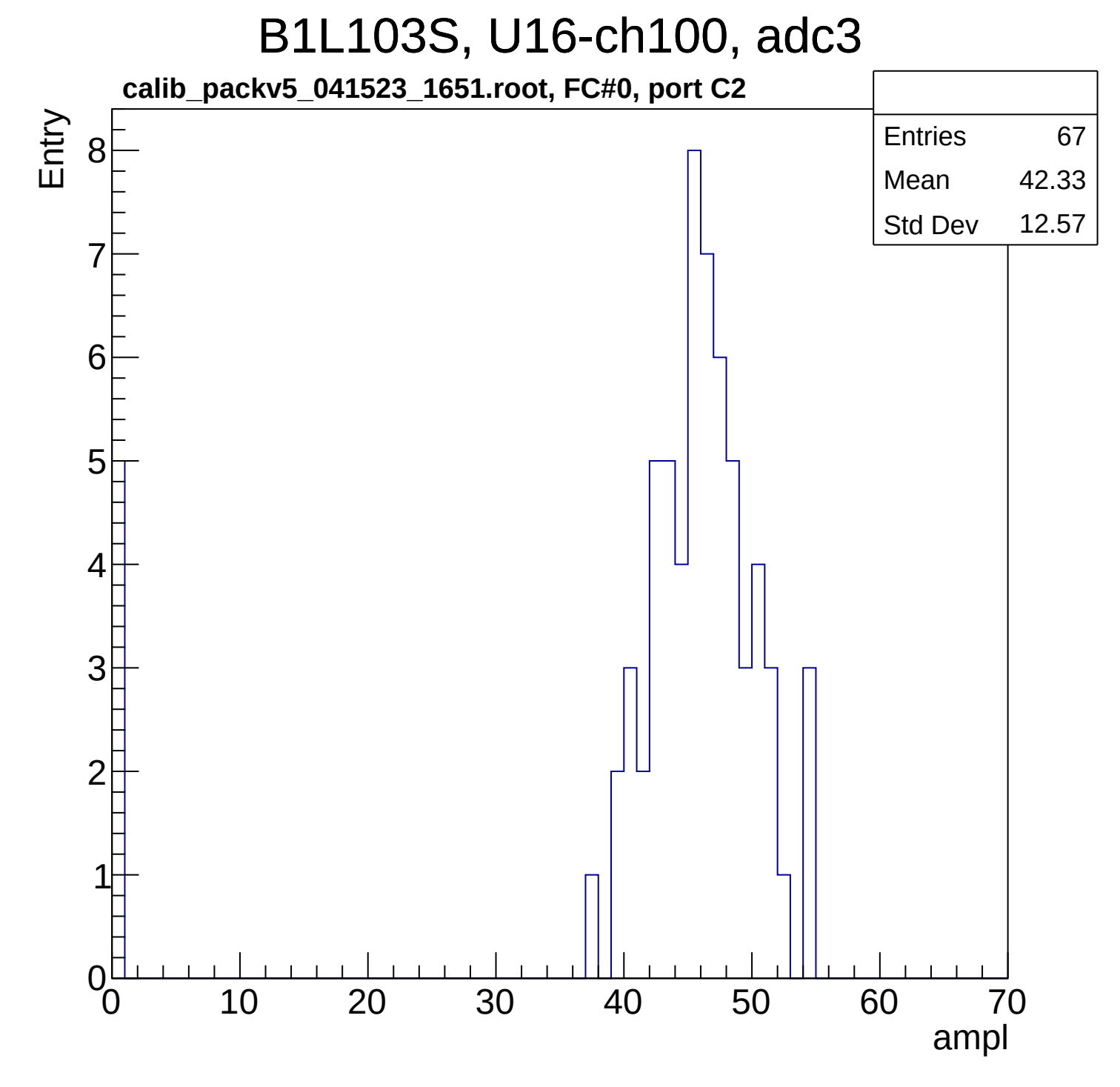
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch100, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 33.03
Std Dev 15.72
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch100, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 42.33
Std Dev 12.57
Entry
ampl
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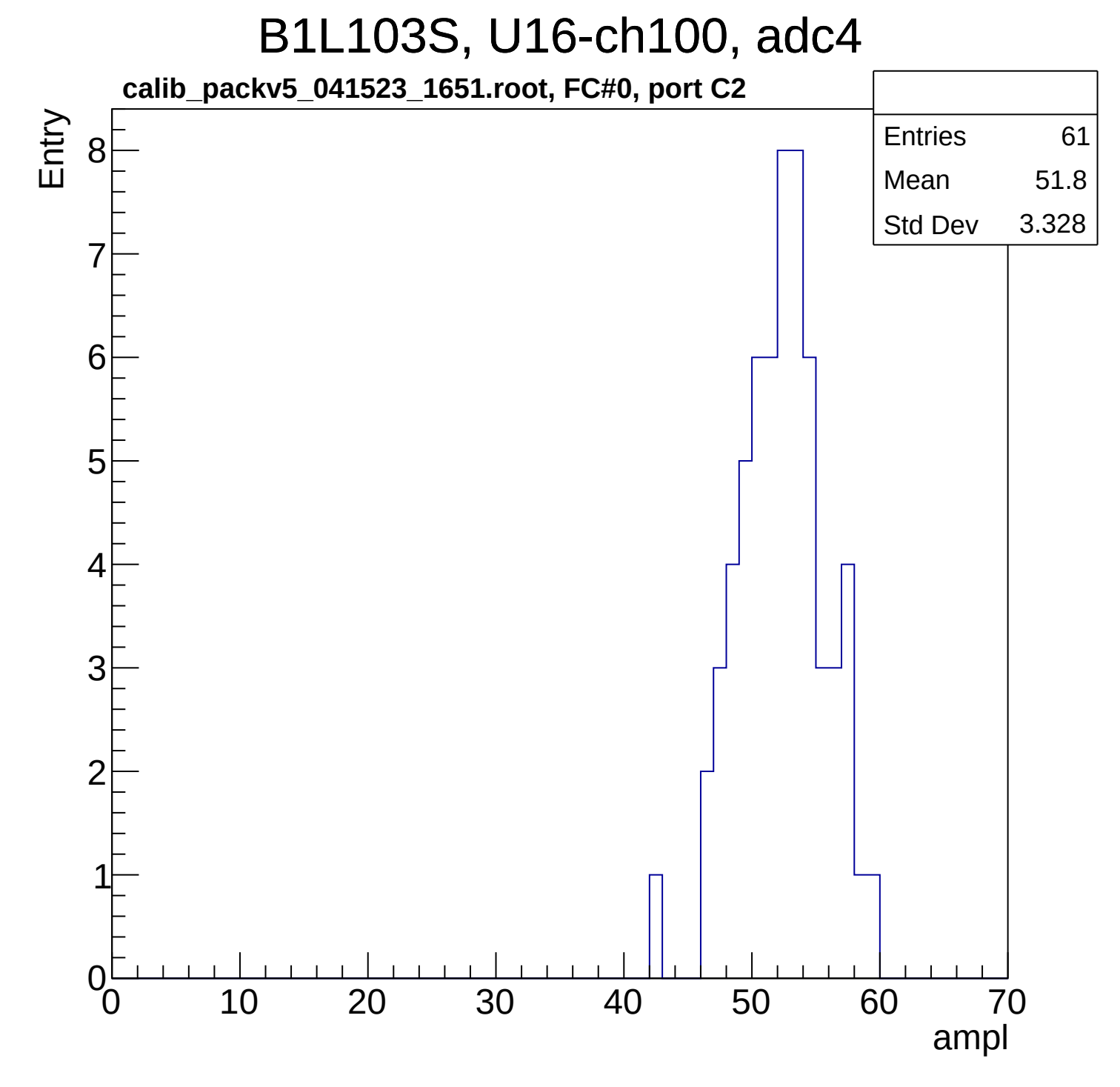
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch100, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 51.8
Std Dev 3.328
Entry
ampl
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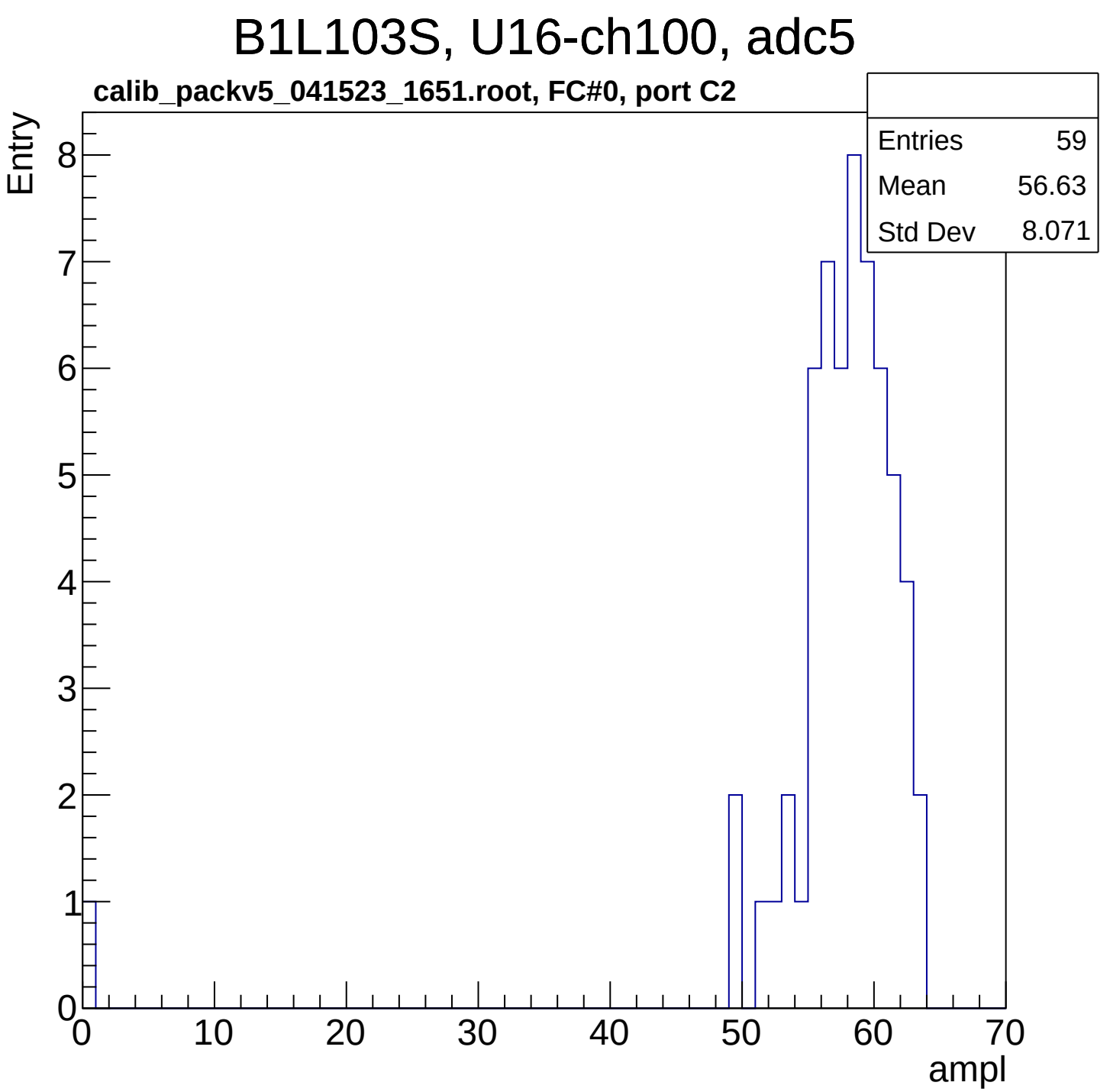
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch100, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 56.63
Std Dev 8.071
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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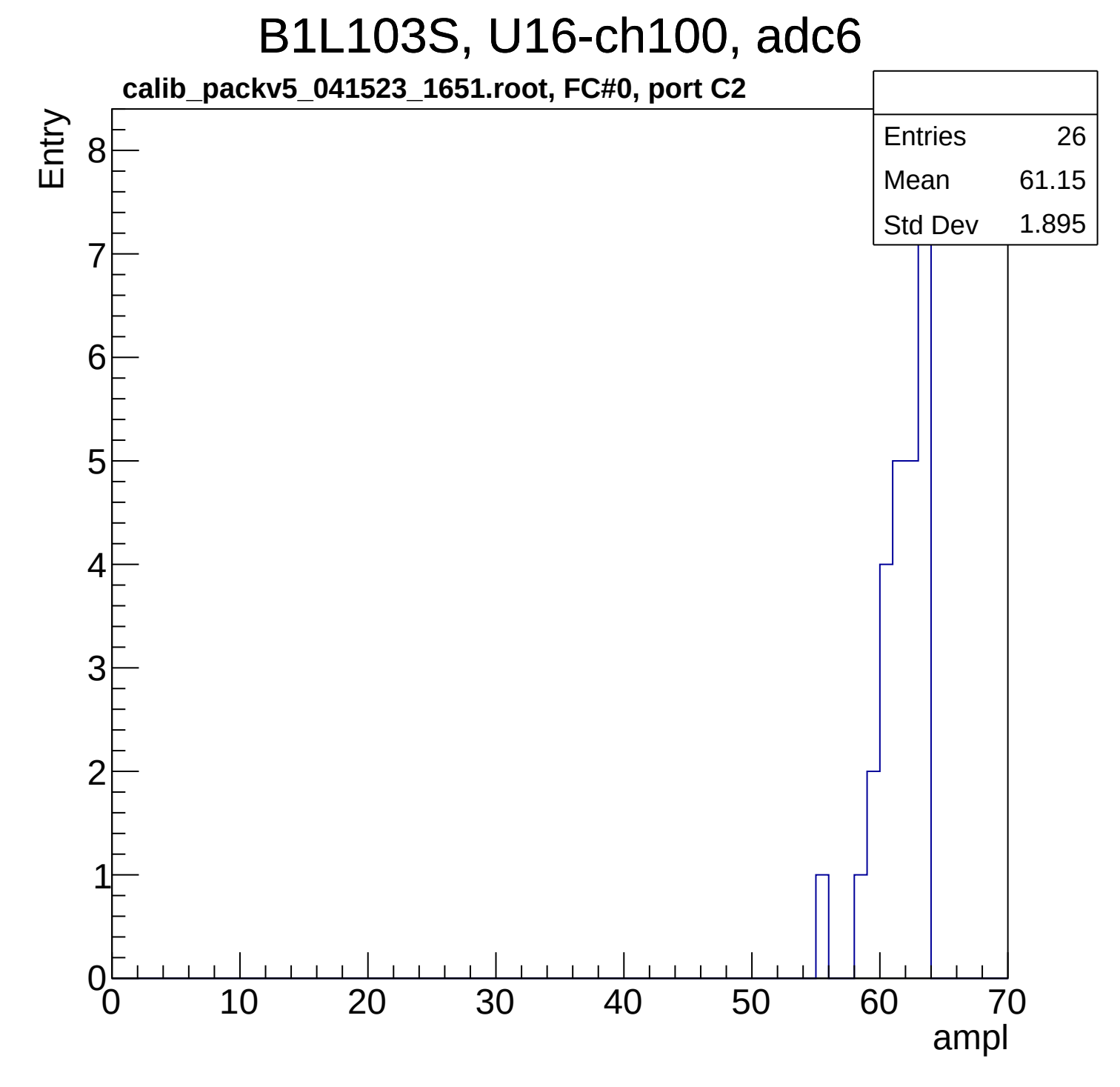
B1L103S, U16-ch100, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 61.15
Std Dev 1.895
Entry
ampl
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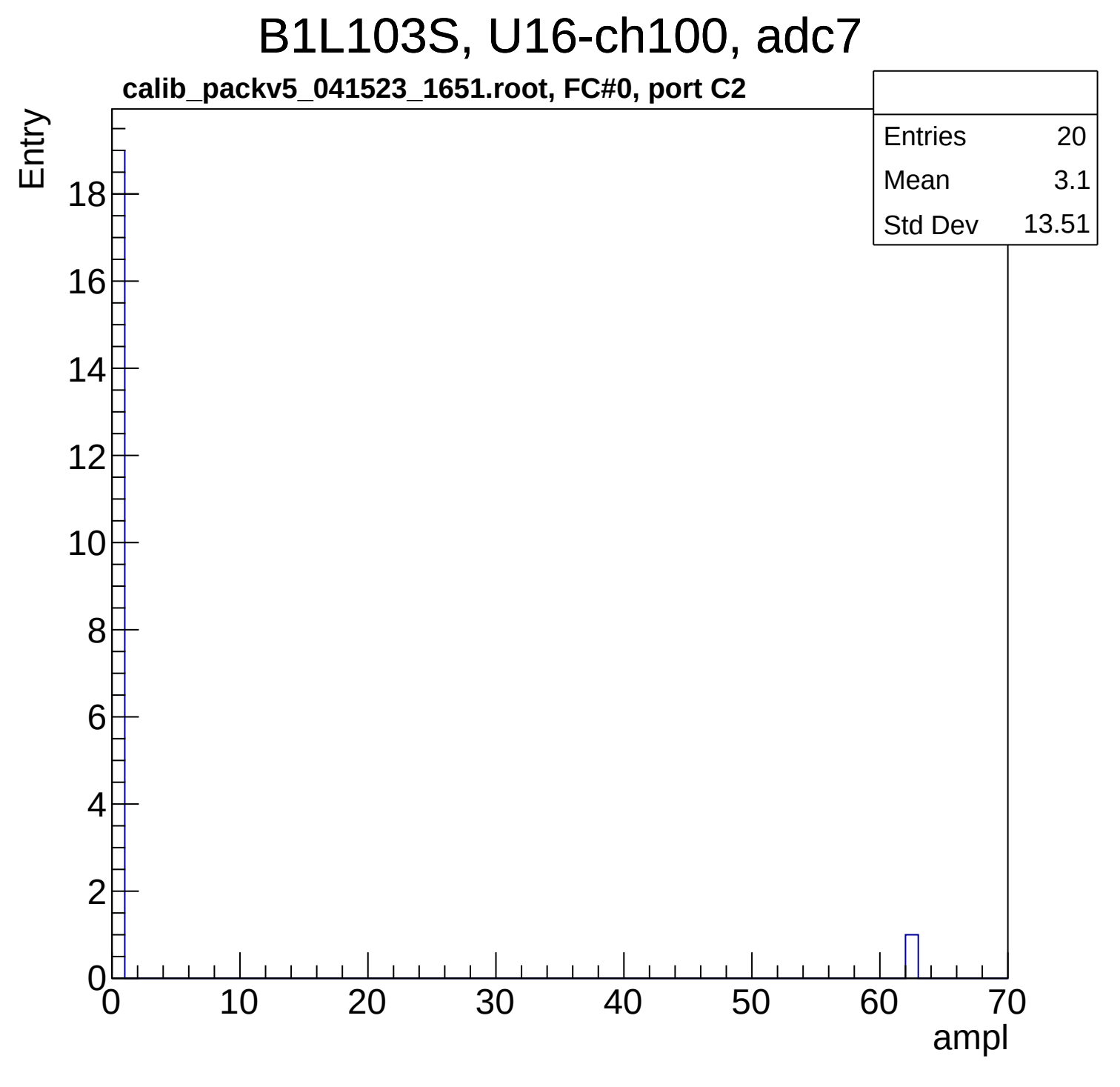
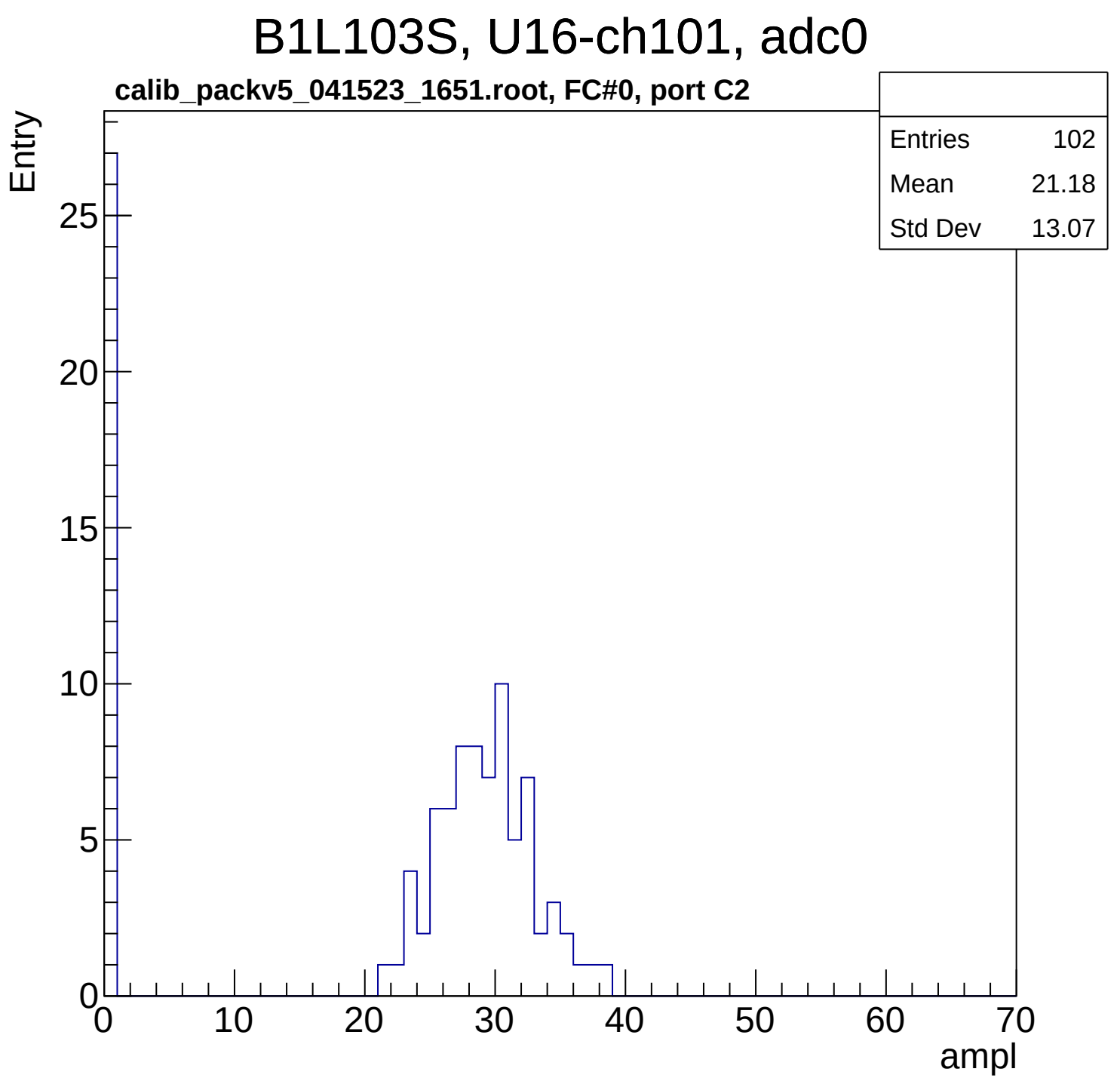
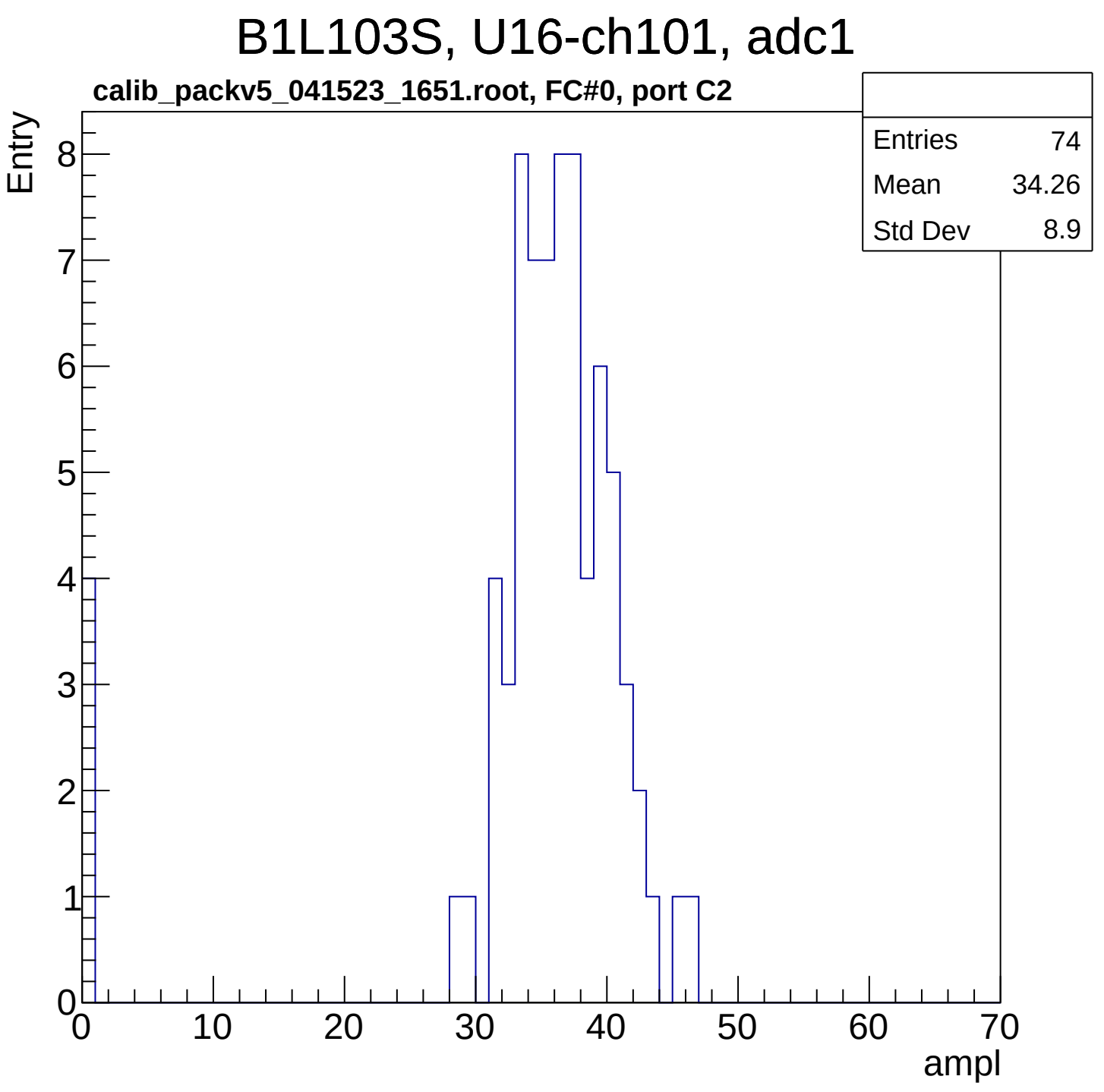
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch100, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch101, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 21.18
Std Dev 13.07
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch101, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 34.26
Std Dev 8.9
Entry
ampl
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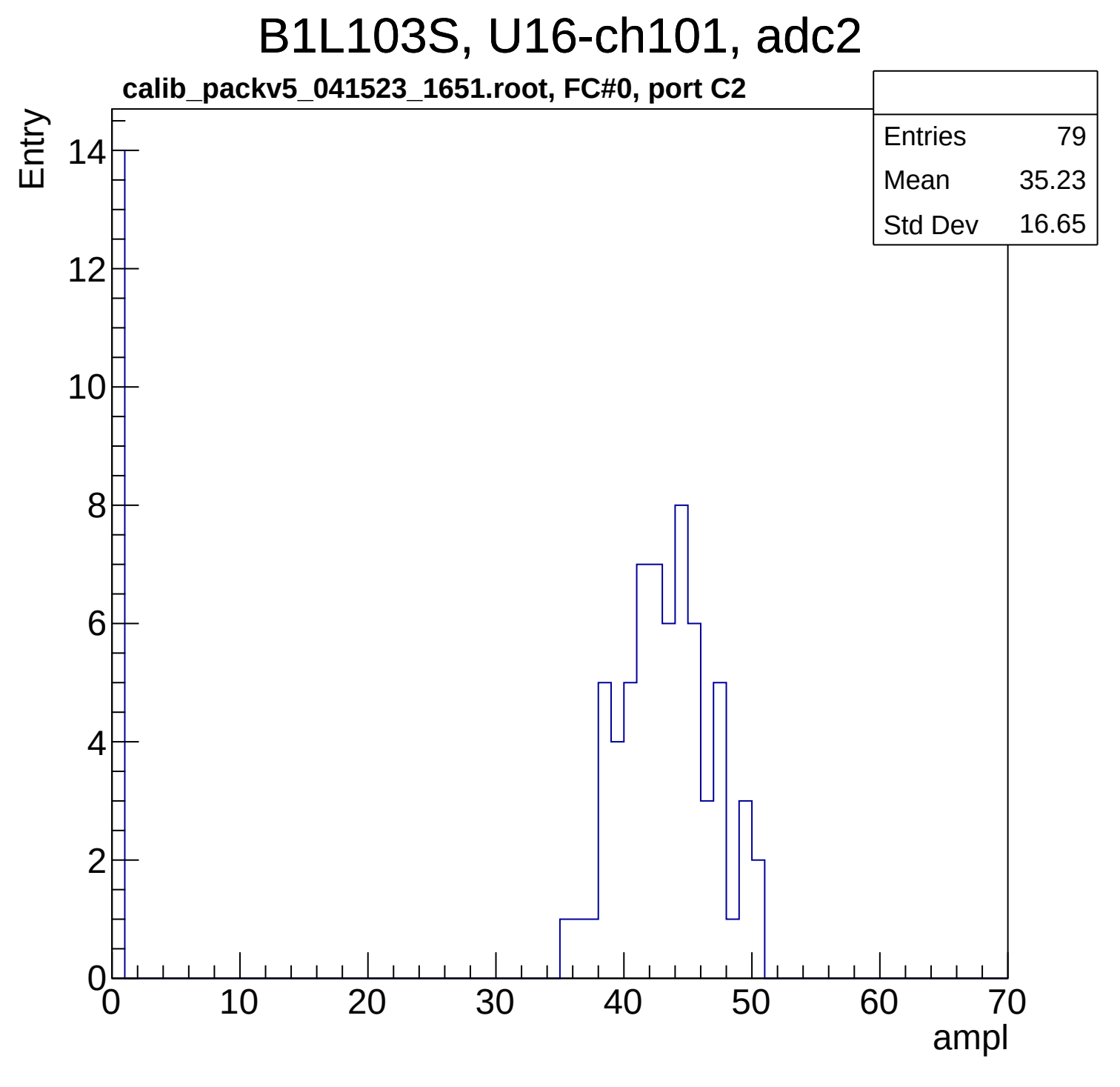
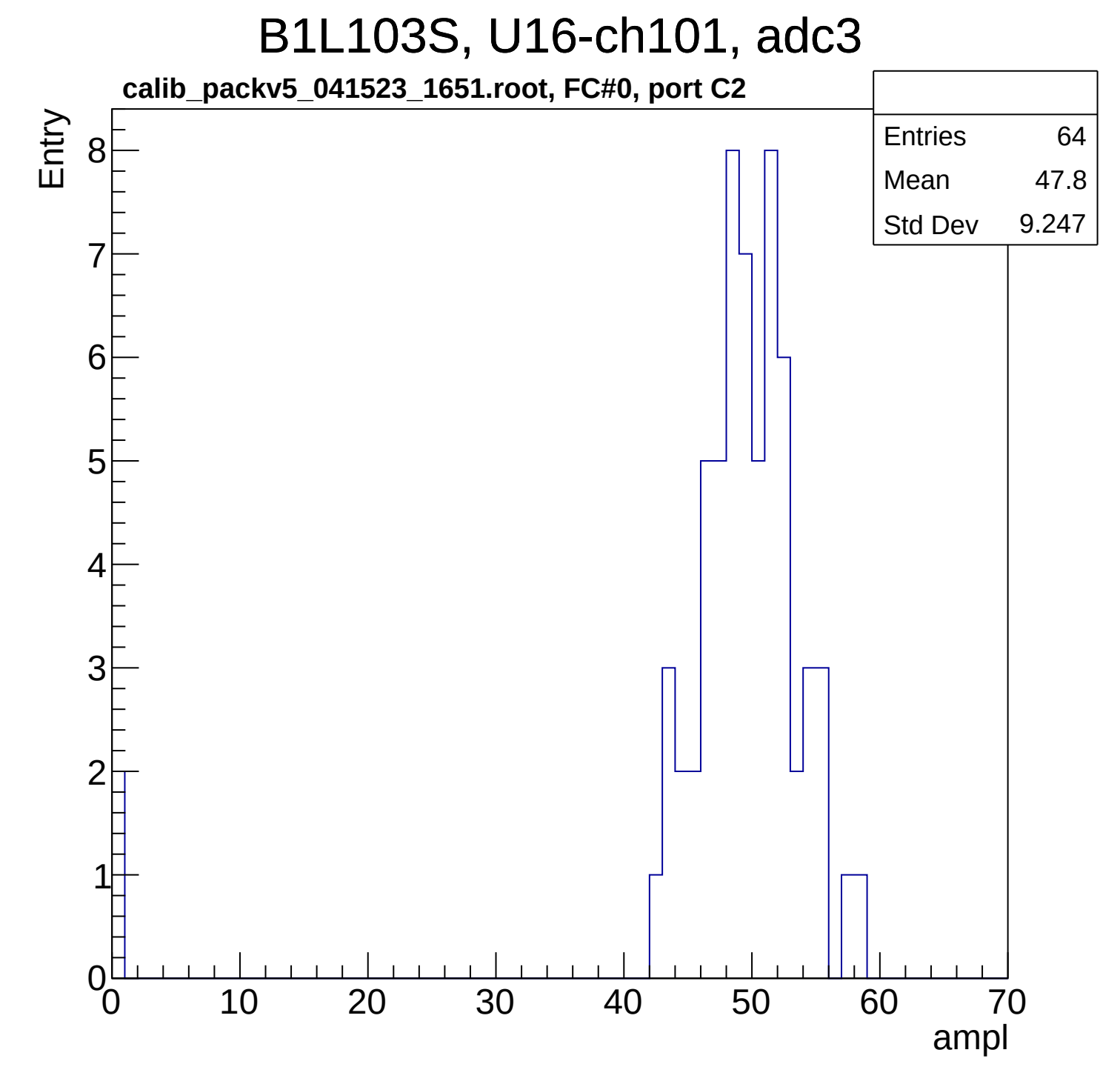
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch101, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 35.23
Std Dev 16.65
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch101, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 47.8
Std Dev 9.247
Entry
ampl
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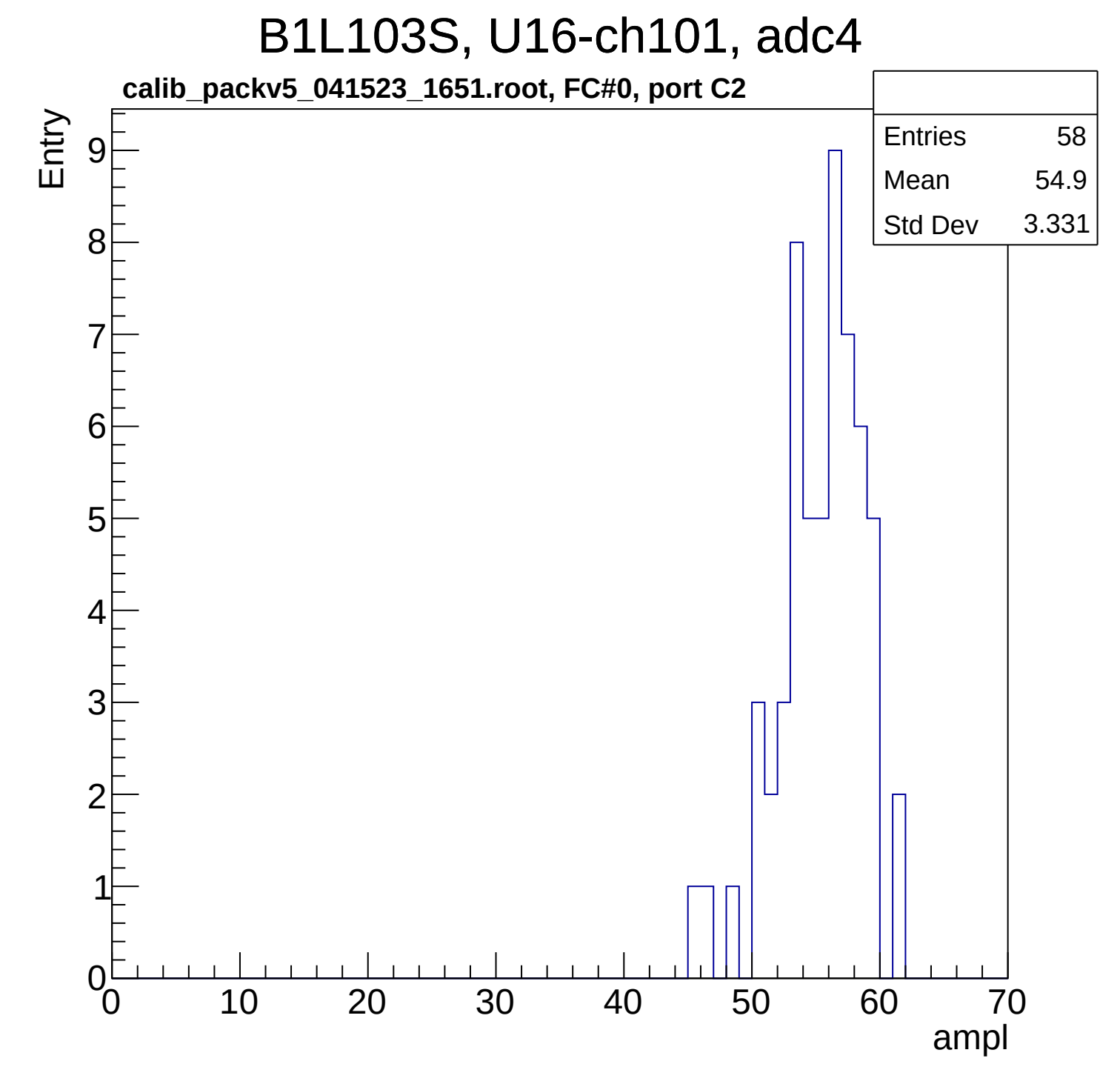
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch101, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 54.9
Std Dev 3.331
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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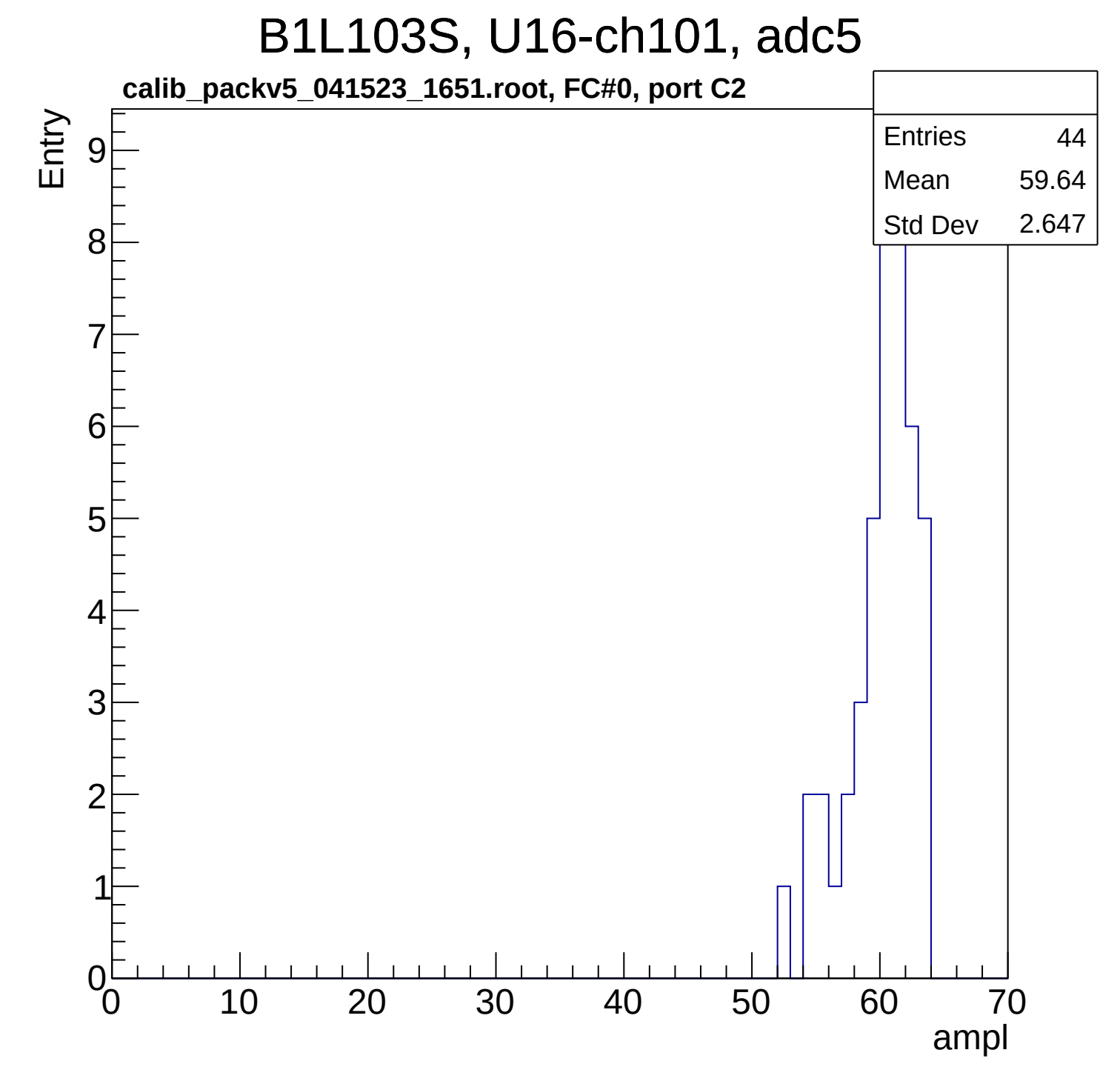
B1L103S, U16-ch101, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 59.64
Std Dev 2.647
Entry
ampl
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2
3
4
5
6
7
8
9
0
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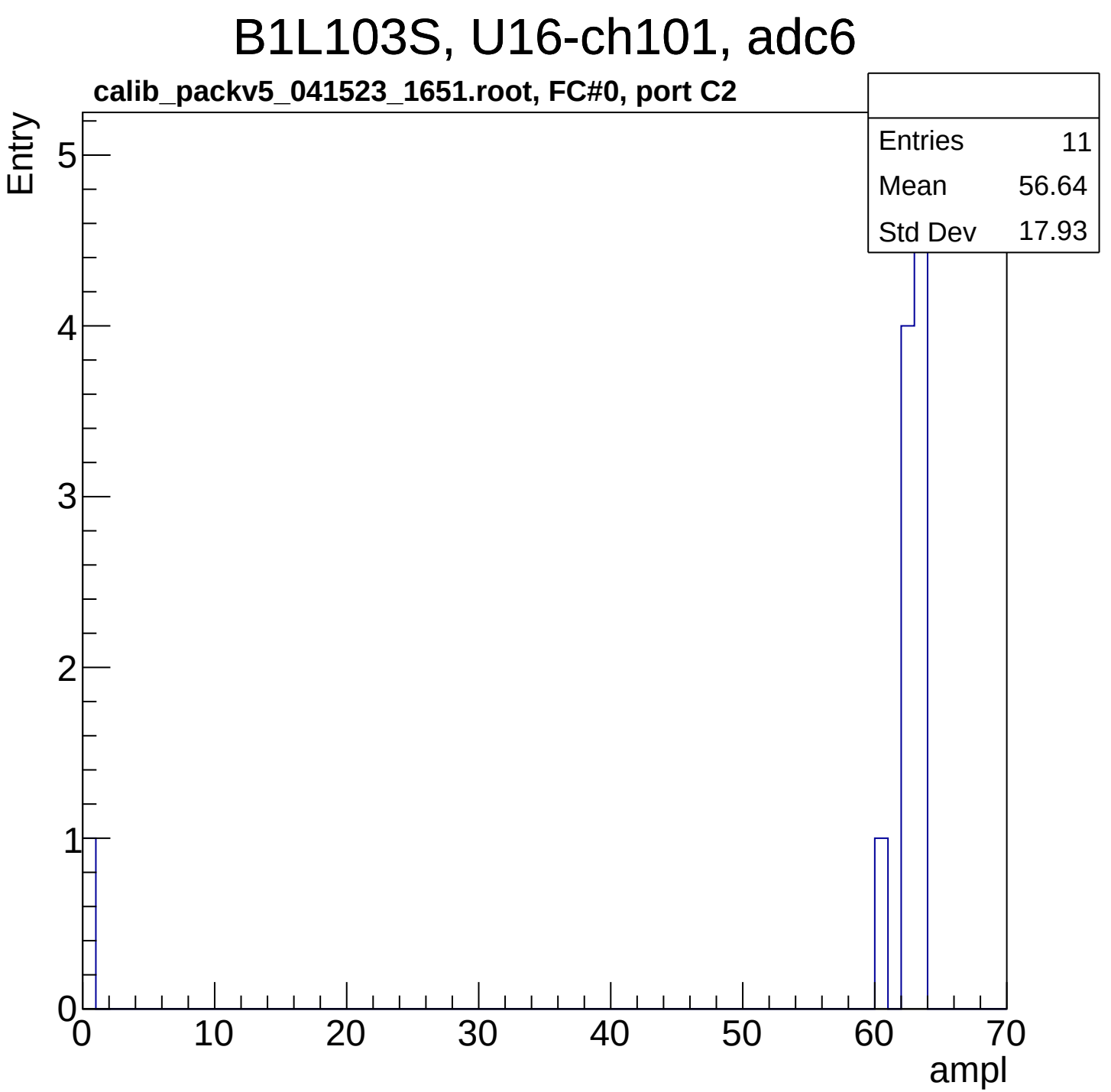
20
30
40
50
60
70


B1L103S, U16-ch101, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 56.64
Std Dev 17.93
Entry
ampl
0
1
2
3
4
5
0
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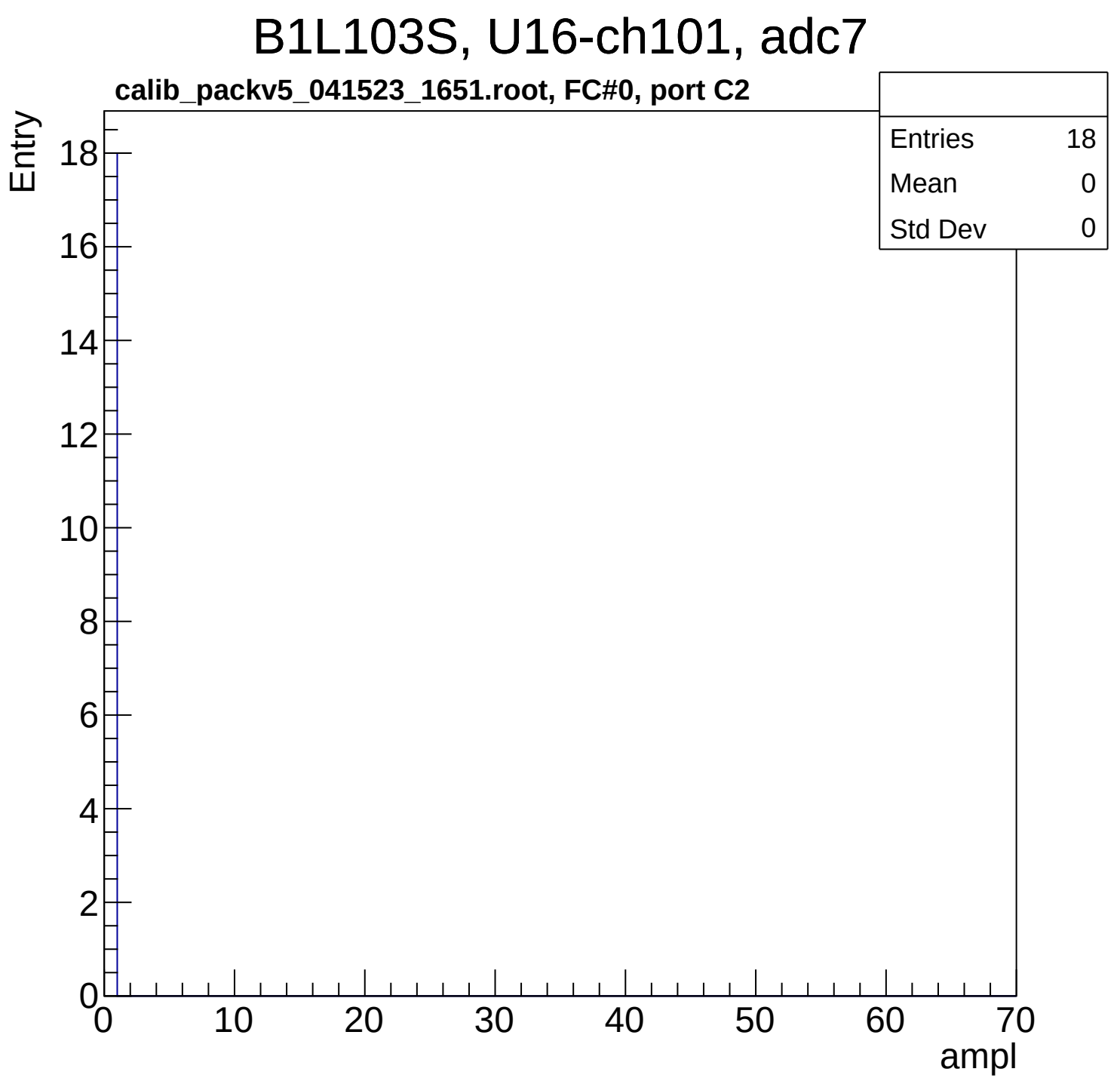
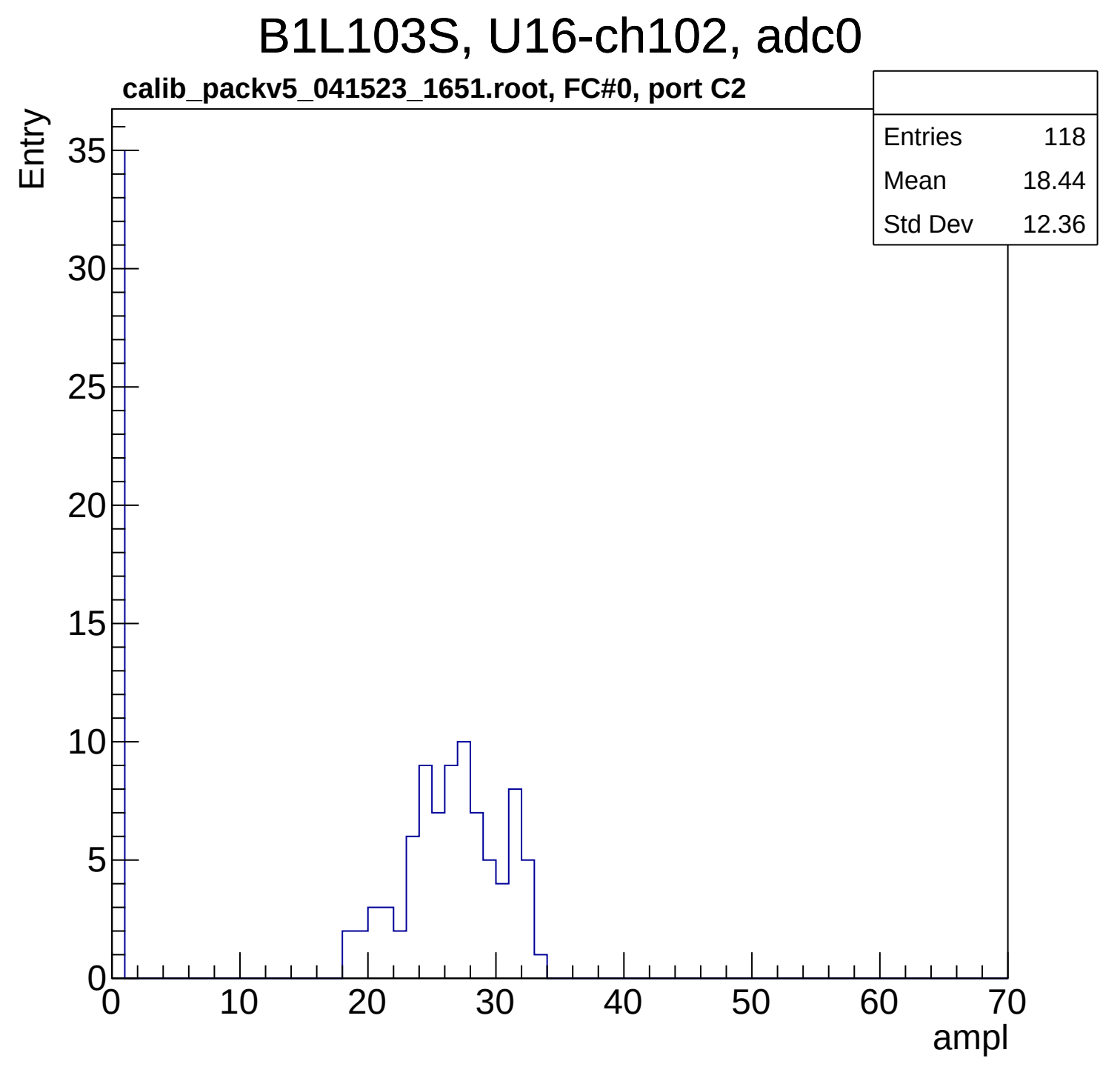
20
30
40
50
60
70


B1L103S, U16-ch101, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch102, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 118
Mean 18.44
Std Dev 12.36
Entry
ampl
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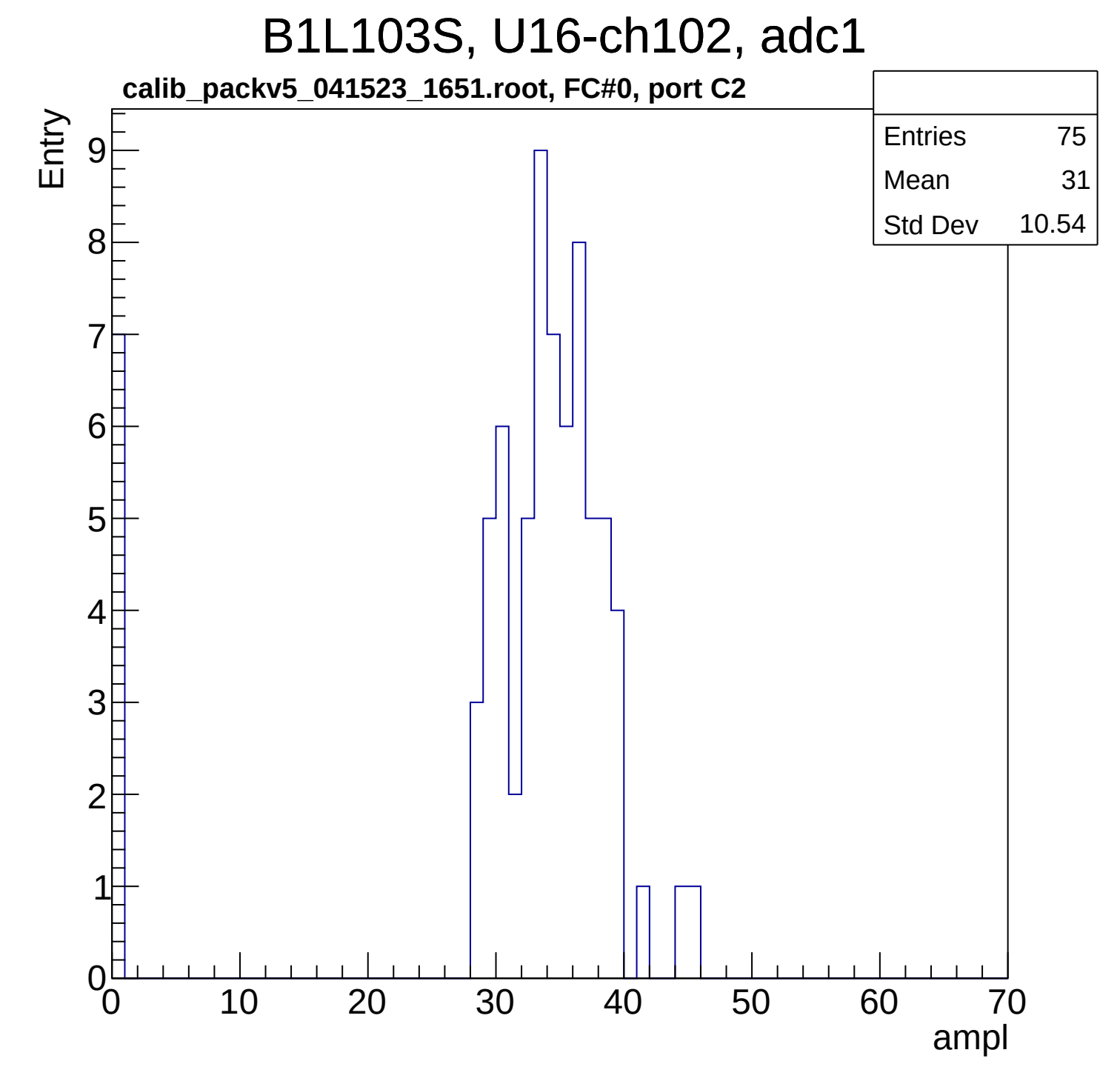
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70


B1L103S, U16-ch102, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 31
Std Dev 10.54
Entry
ampl
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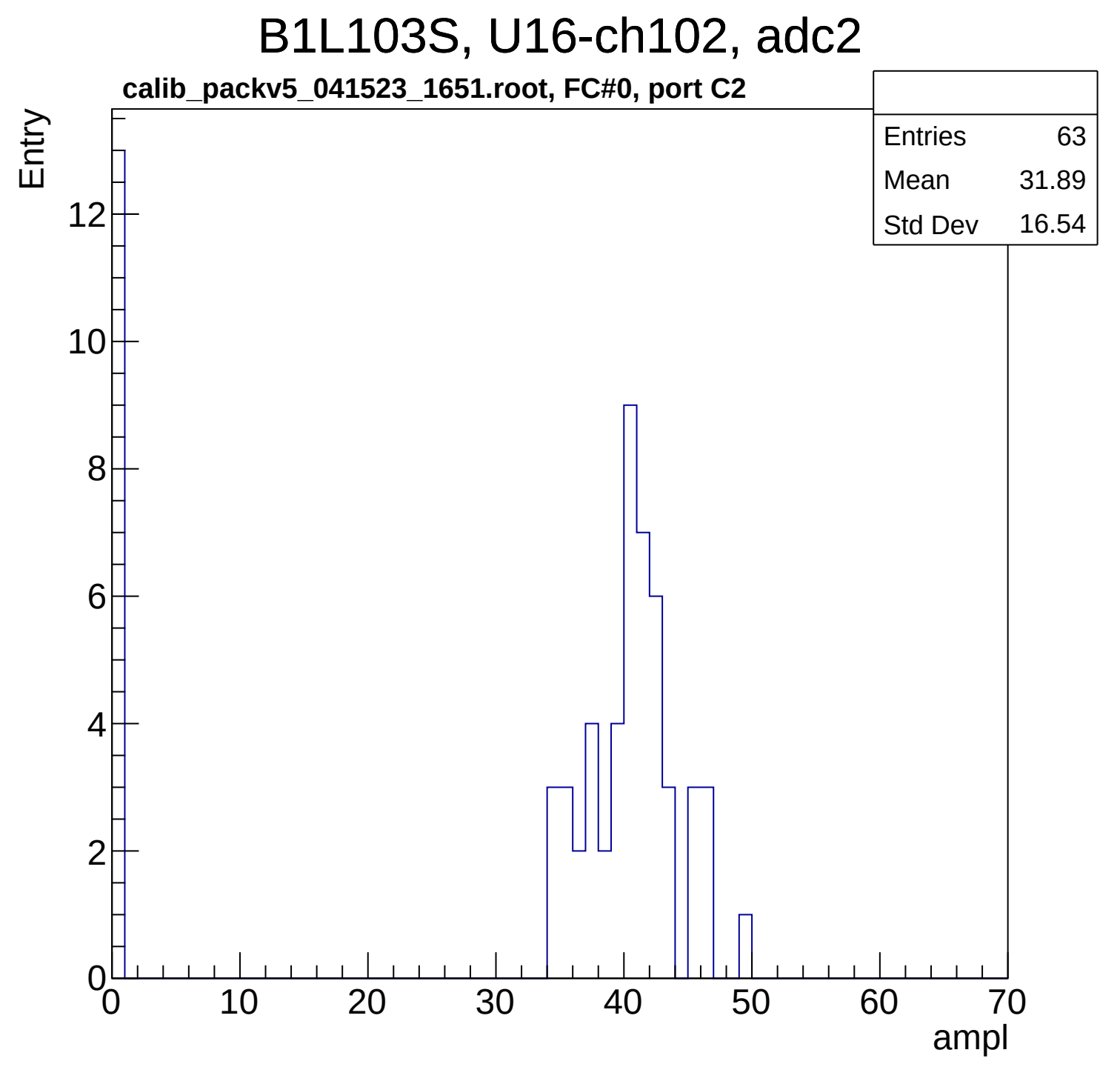
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch102, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 31.89
Std Dev 16.54
Entry
0
2
4
6
8
10
12
0
10
20
30
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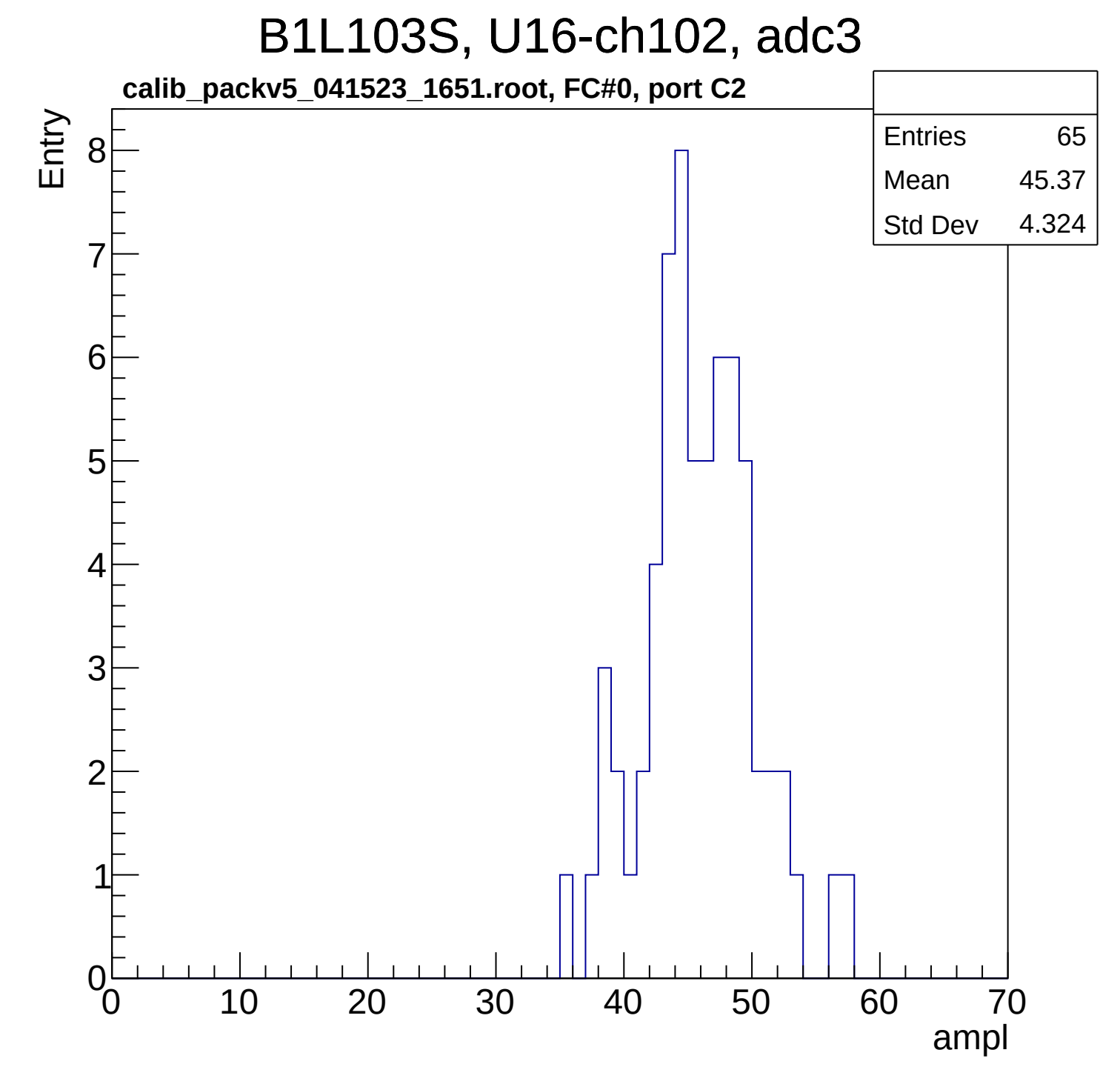
50
60
70
ampl


B1L103S, U16-ch102, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 45.37
Std Dev 4.324
Entry
ampl
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1
2
3
4
5
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7
8
0
10
20
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40
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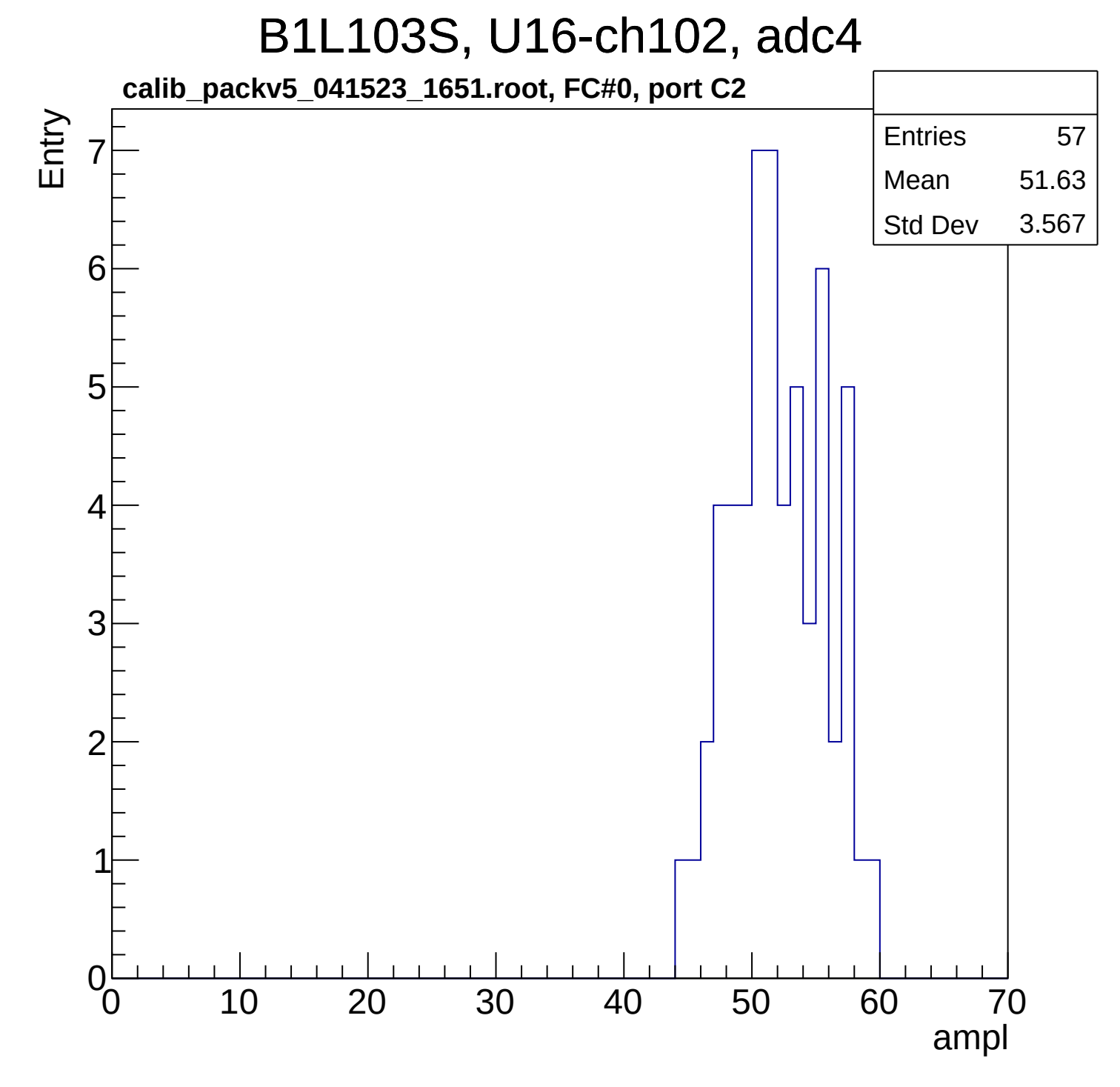
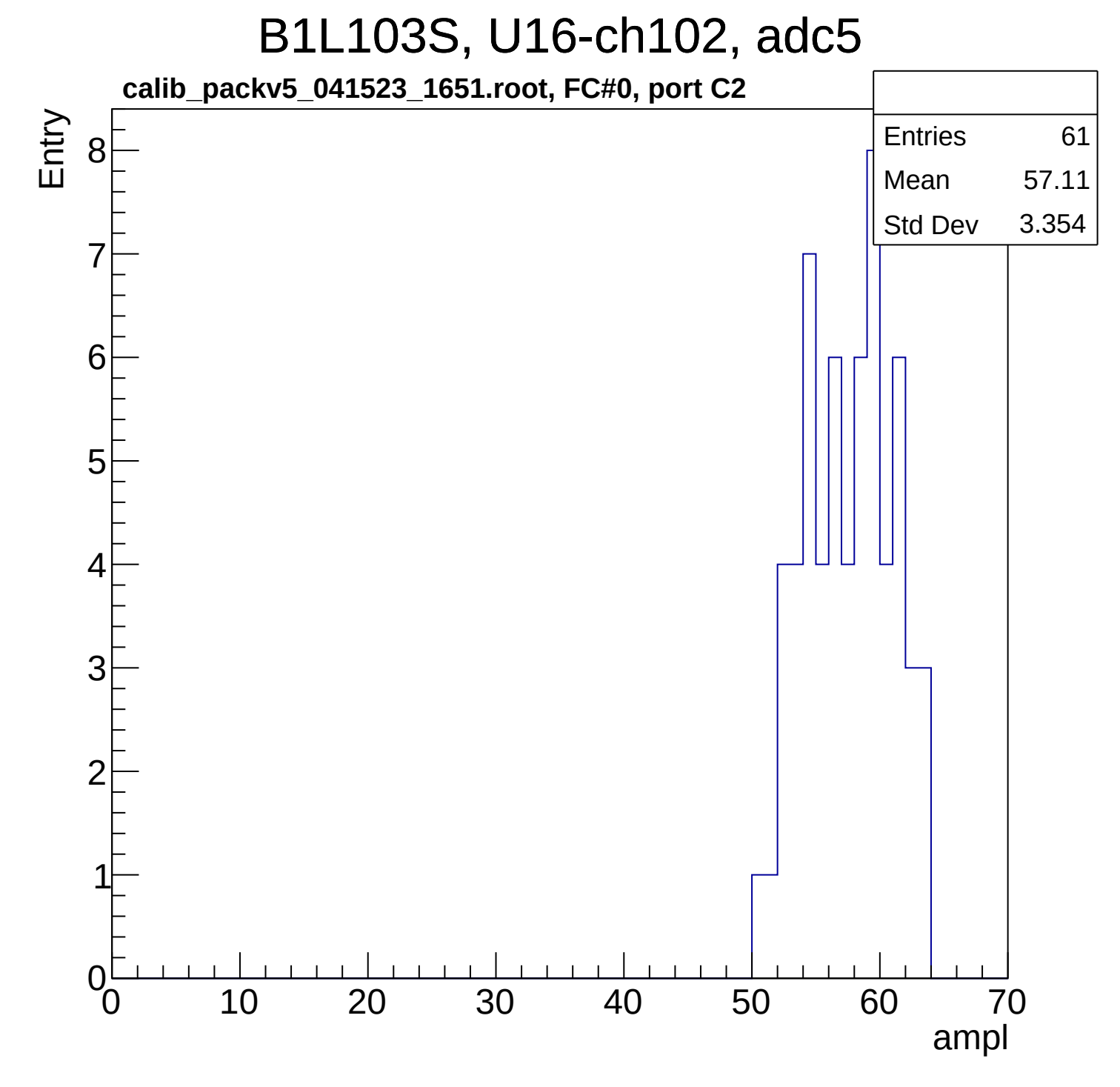
60
70


B1L103S, U16-ch102, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 51.63
Std Dev 3.567
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch102, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 57.11
Std Dev 3.354
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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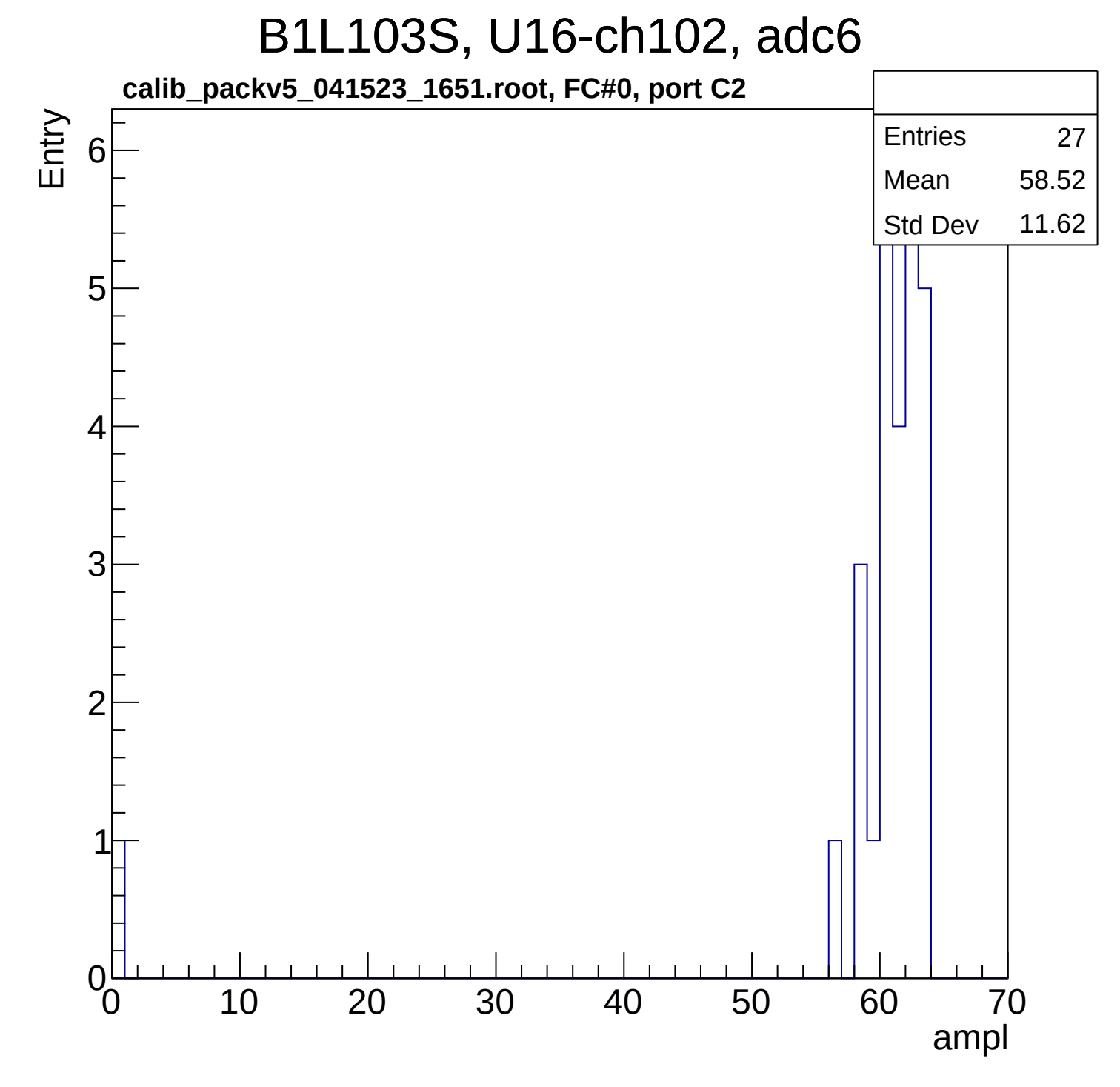
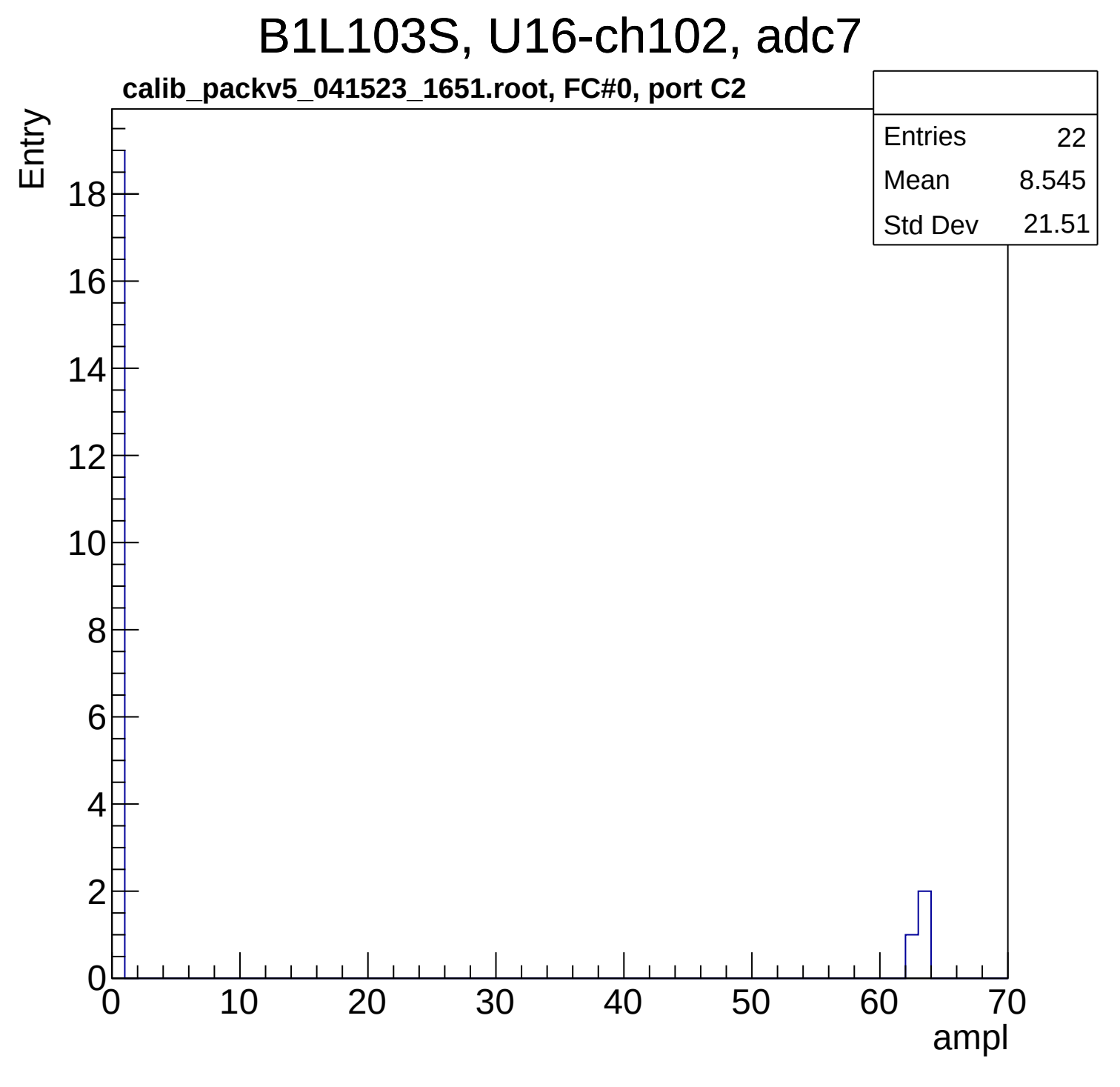
50
60
70


B1L103S, U16-ch102, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 58.52
Std Dev 11.62
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U16-ch102, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.545
Std Dev 21.51
Entry
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6
8
10
12
14
16
18
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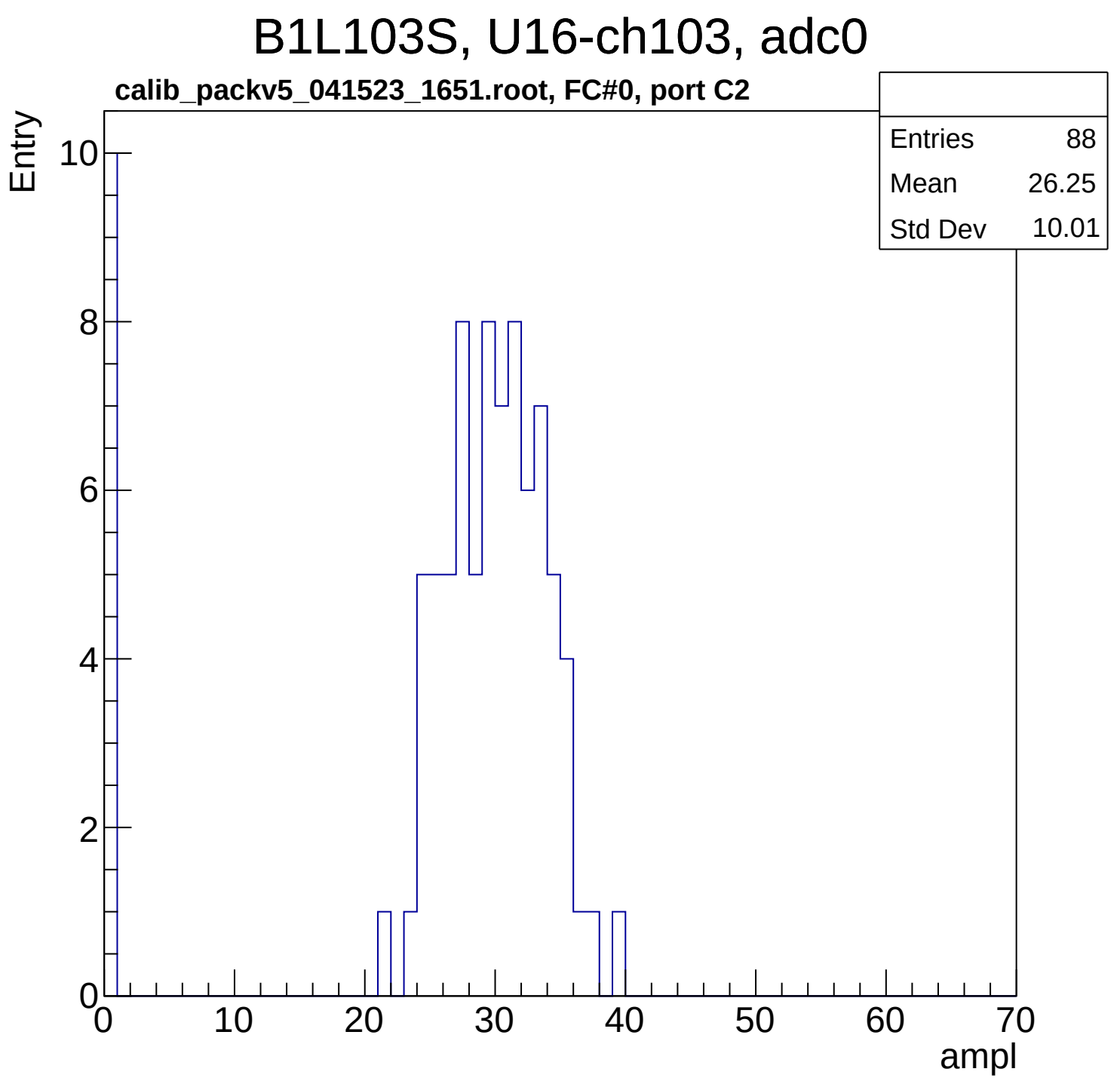
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch103, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 26.25
Std Dev 10.01
Entry
ampl
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0
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40
50
60
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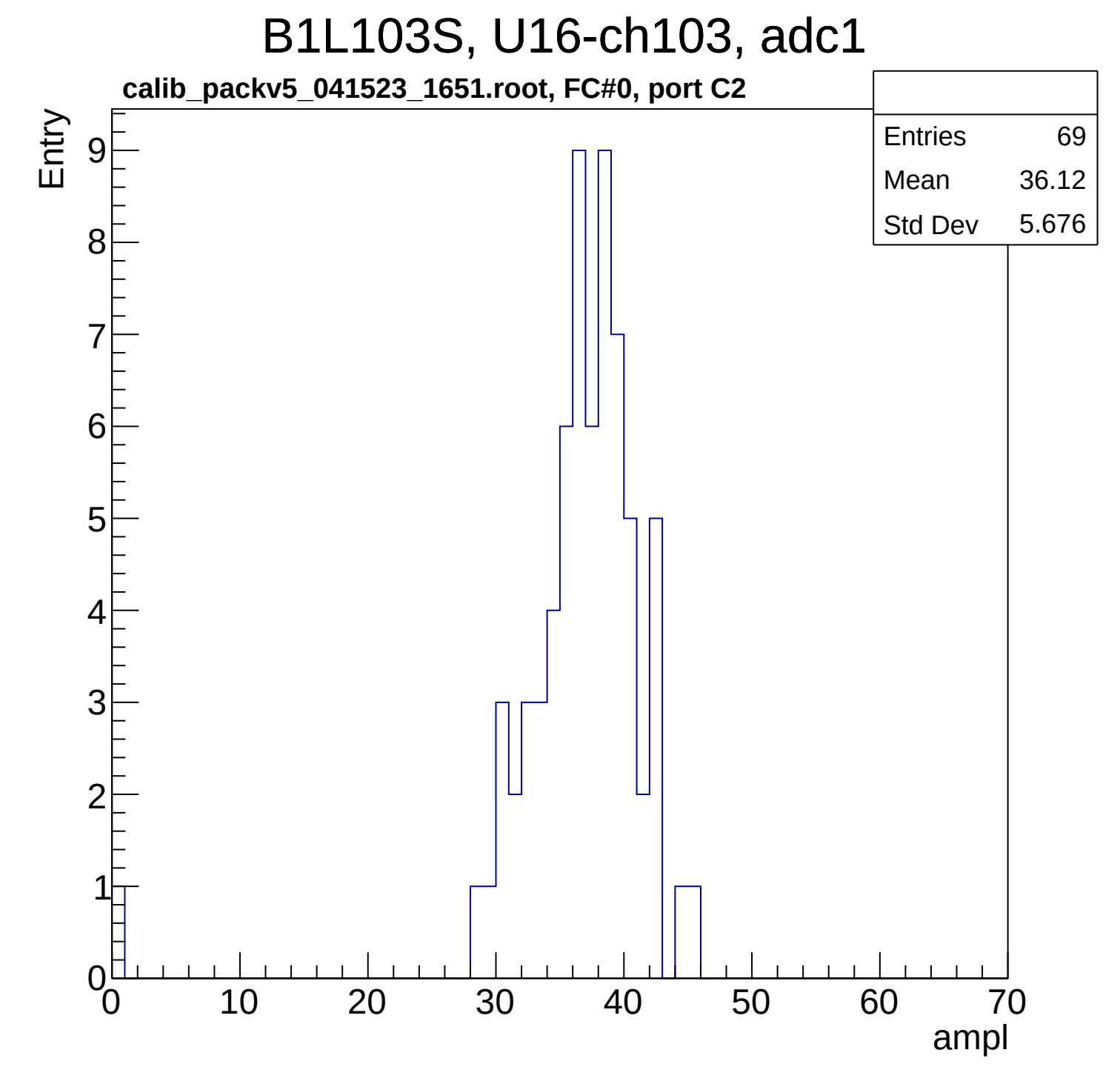
B1L103S, U16-ch103, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 36.12
Std Dev 5.676
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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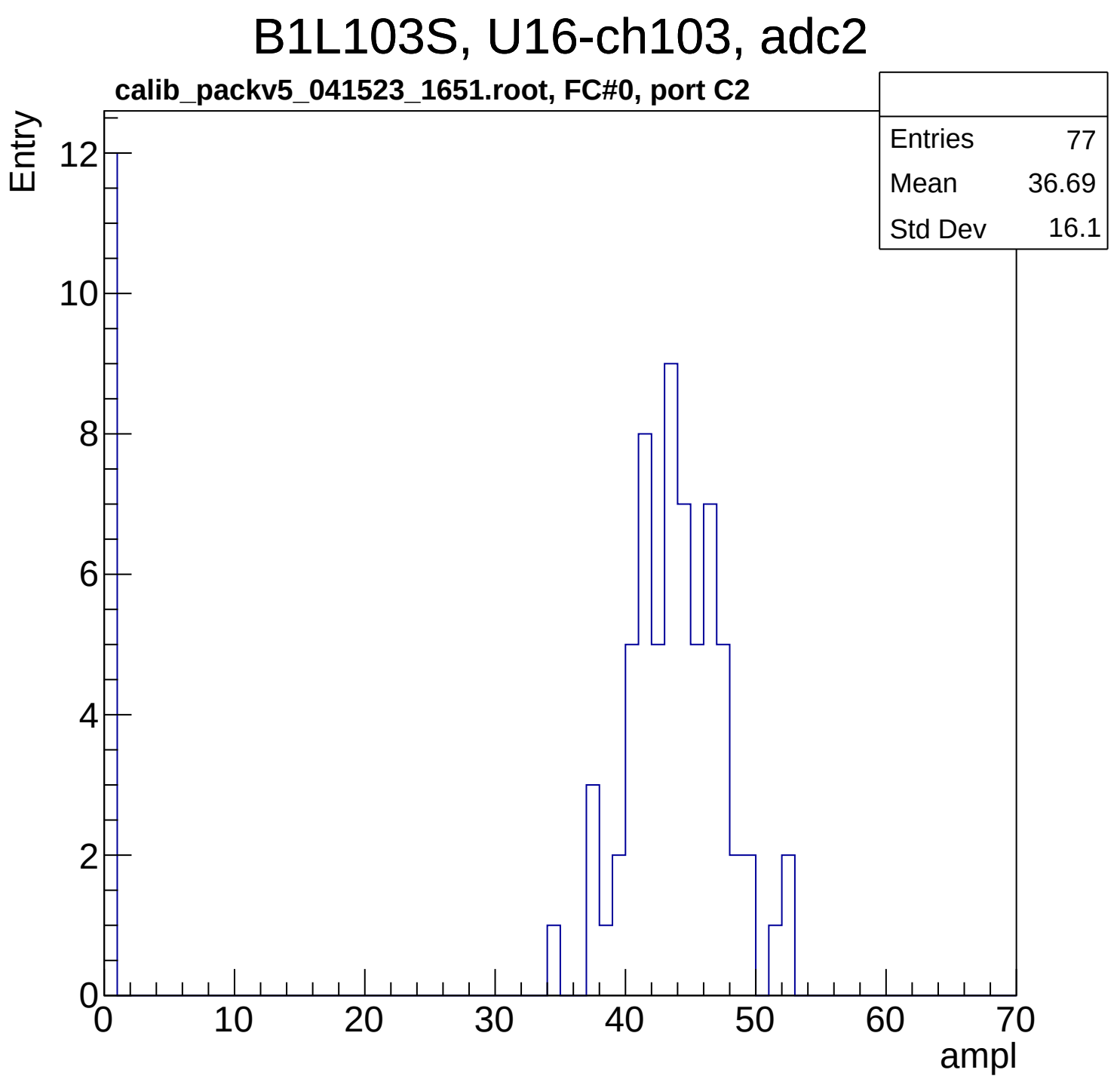
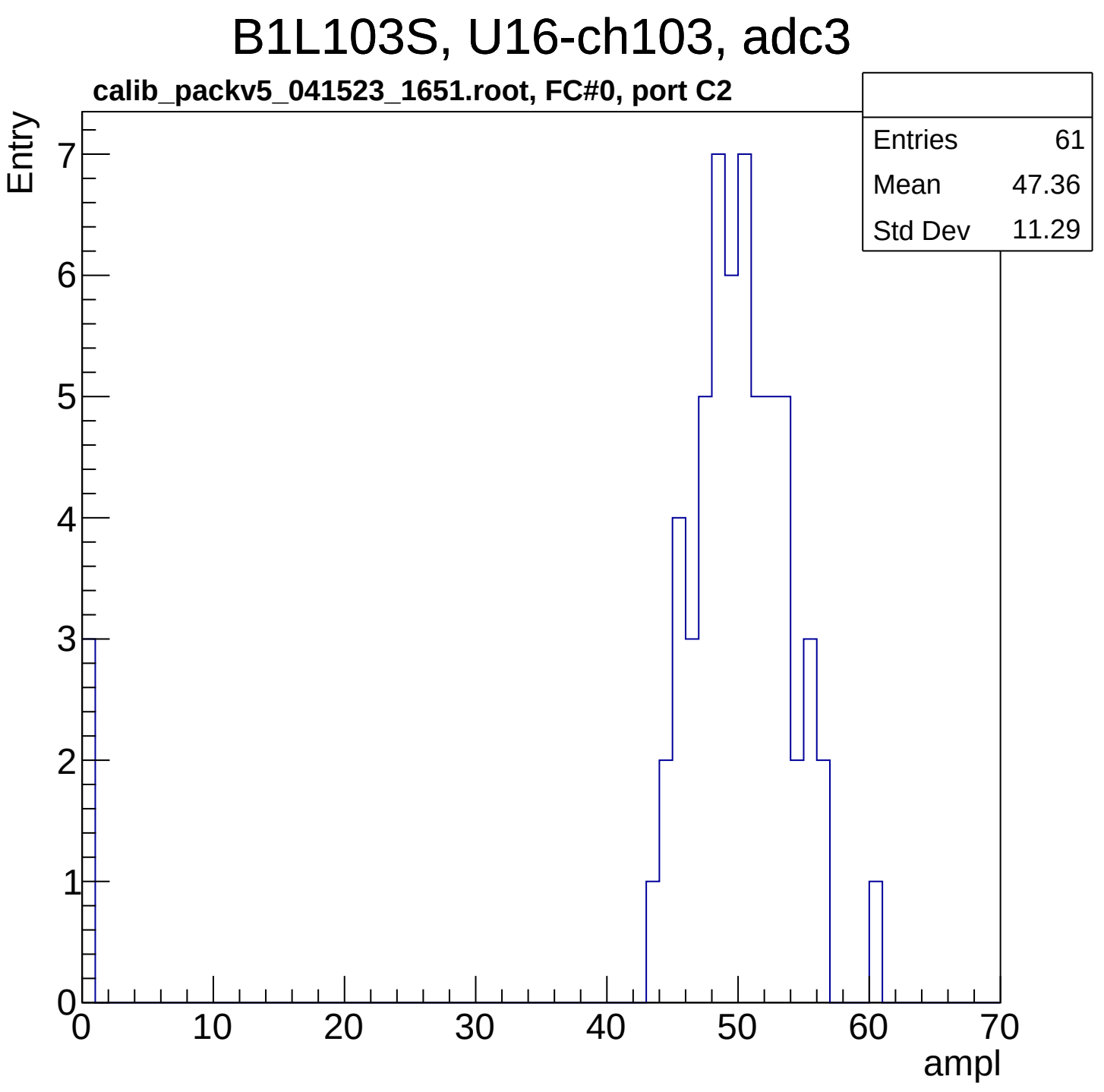
40
50
60
70


B1L103S, U16-ch103, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 36.69
Std Dev 16.1
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch103, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 47.36
Std Dev 11.29
Entry
ampl
0
1
2
3
4
5
6
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60
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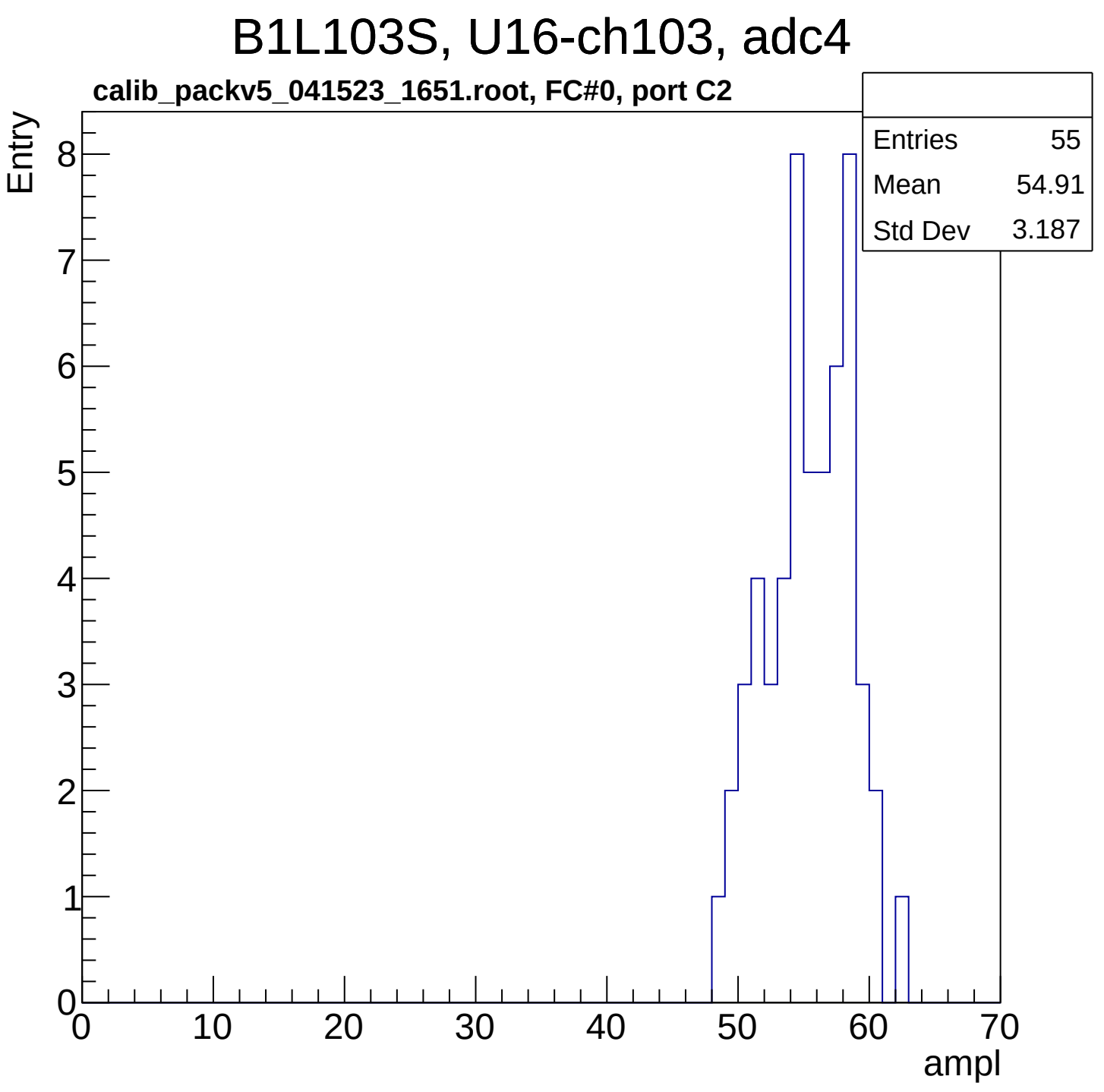
B1L103S, U16-ch103, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 54.91
Std Dev 3.187
Entry
ampl
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3
4
5
6
7
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0
10
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40
50
60
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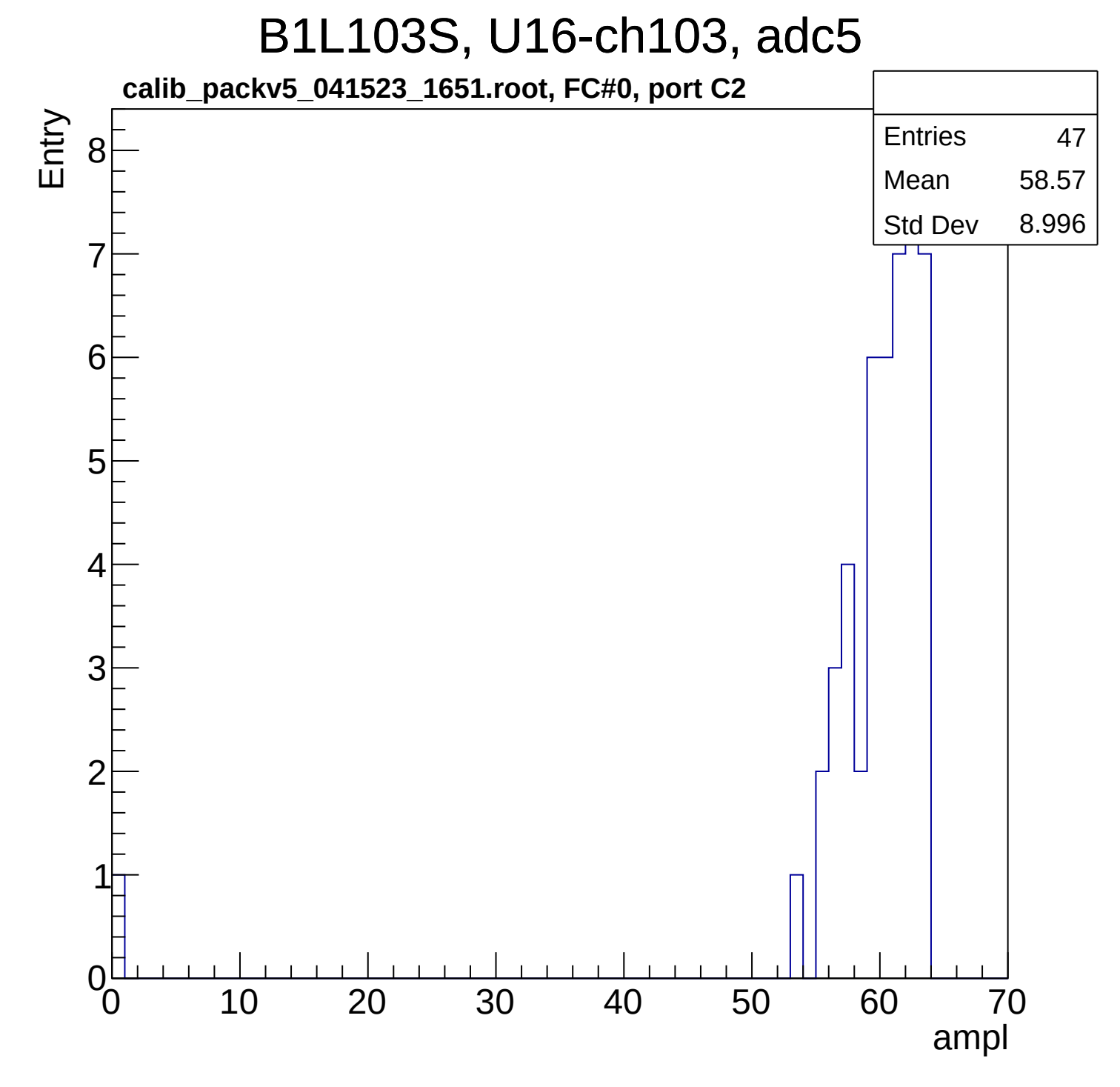
B1L103S, U16-ch103, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.57
Std Dev 8.996
Entry
ampl
0
1
2
3
4
5
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7
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60
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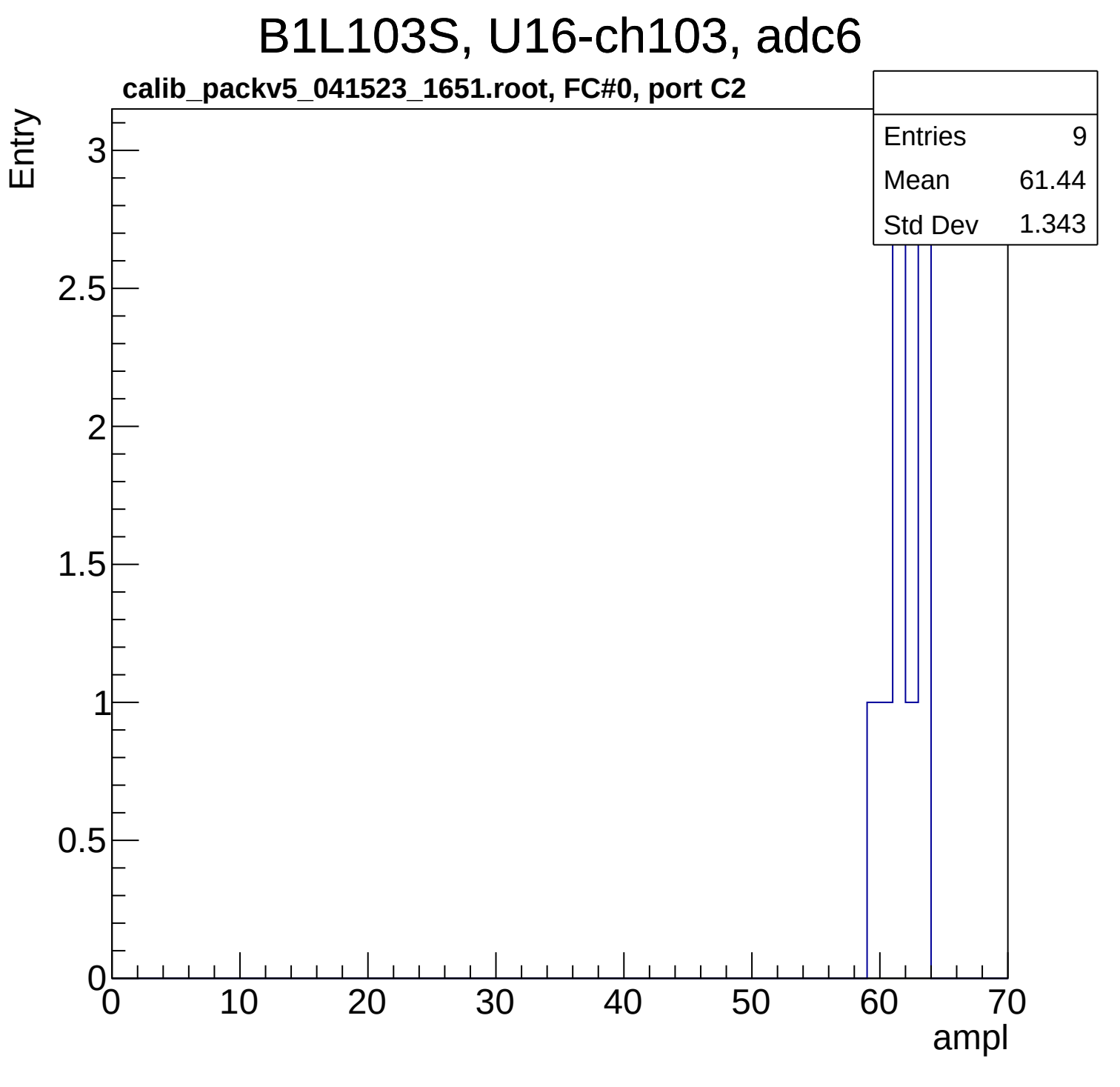
B1L103S, U16-ch103, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.44
Std Dev 1.343
Entry
ampl
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0.5
1
1.5
2
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0
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60
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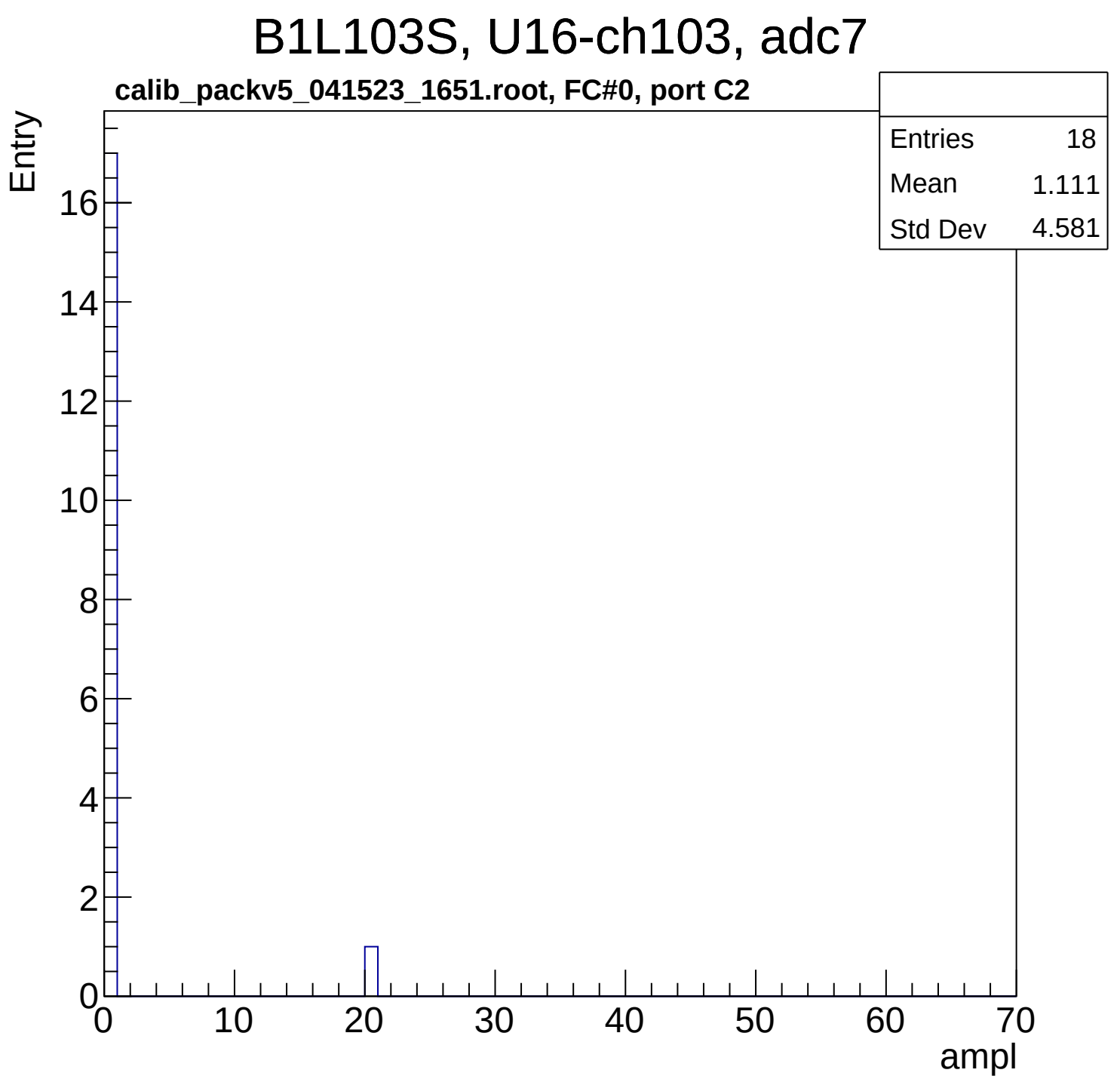
B1L103S, U16-ch103, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.111
Std Dev 4.581
Entry
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4
6
8
10
12
14
16
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10
20
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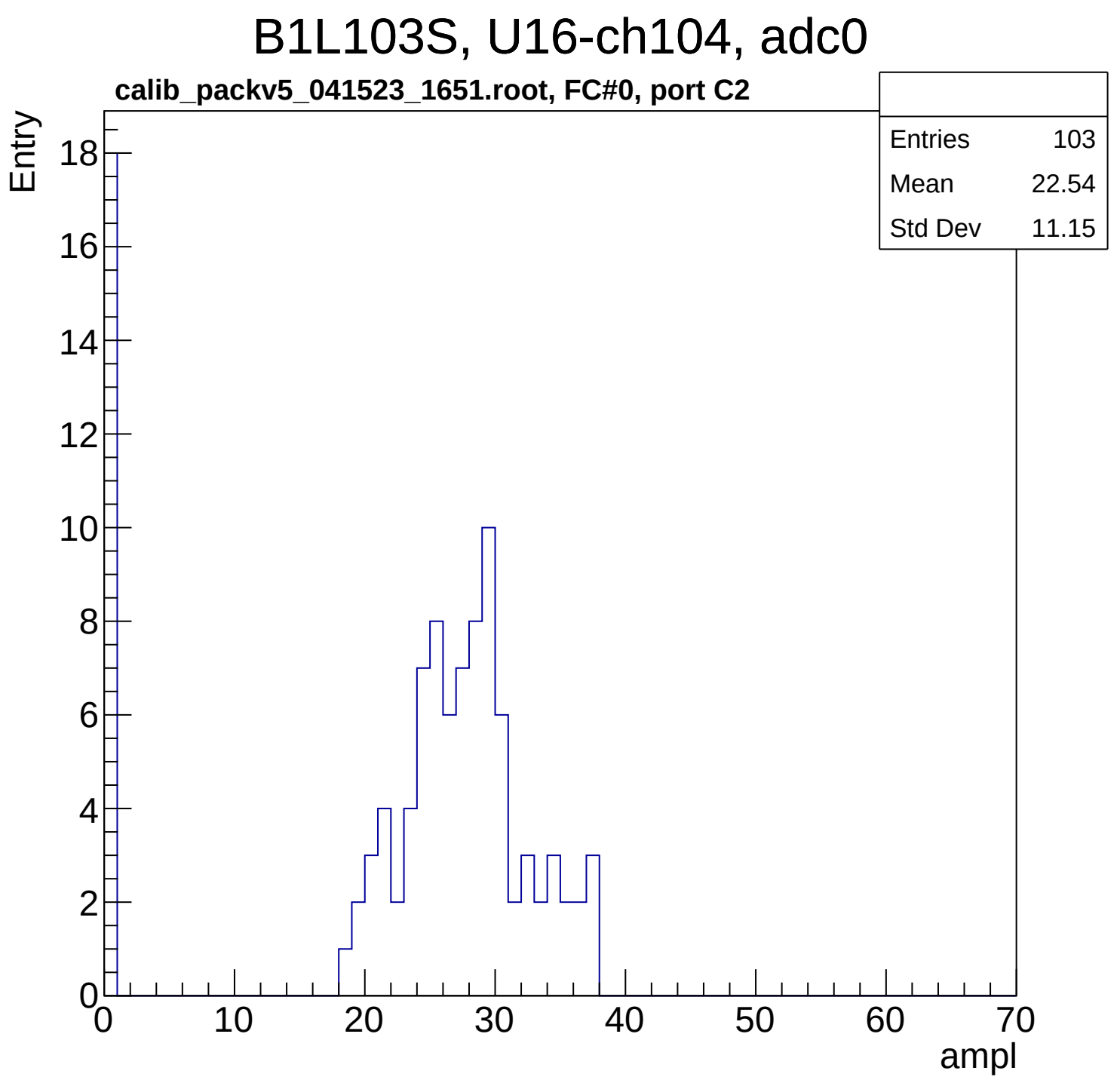
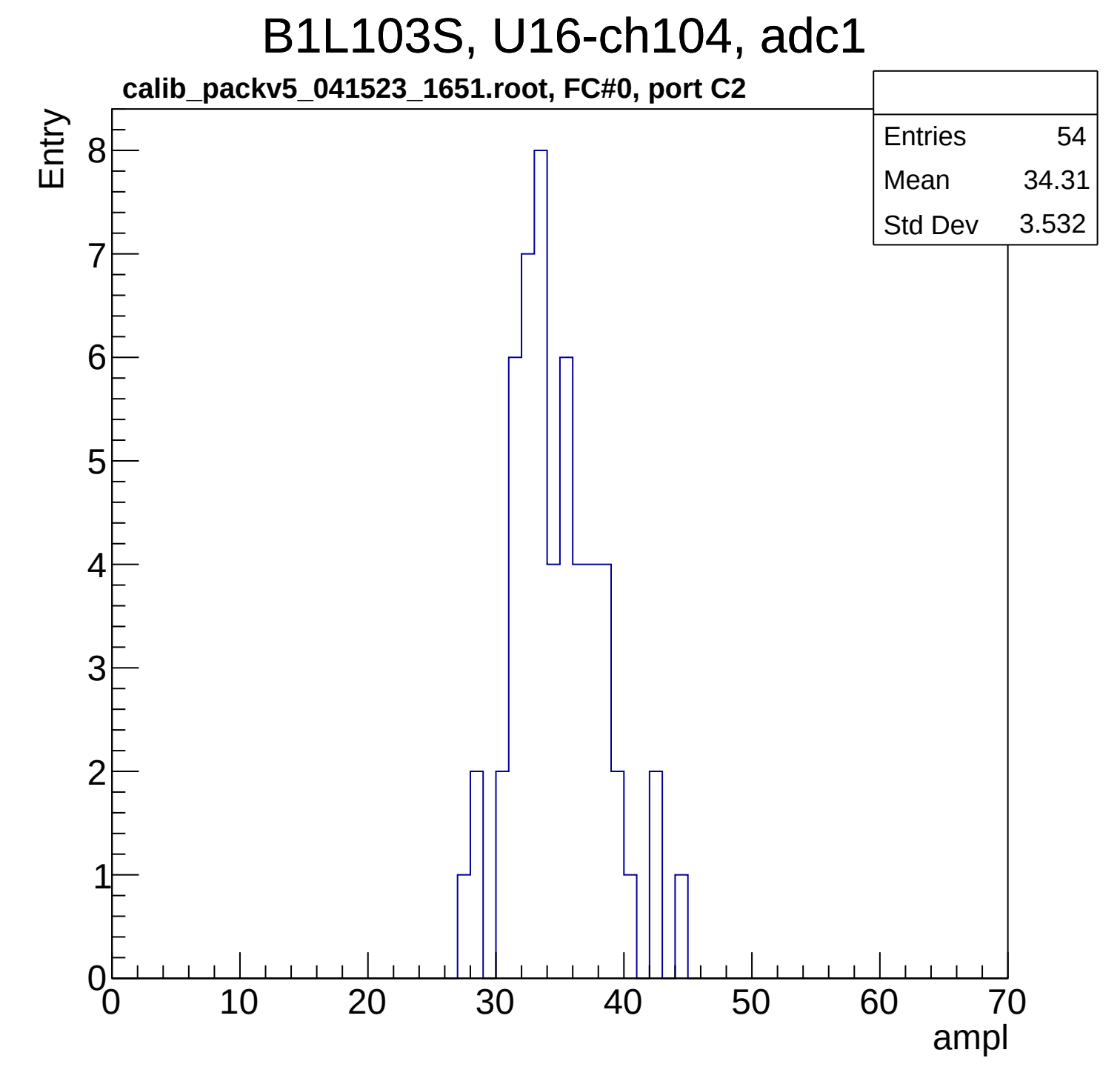
40
50
60
70
ampl


B1L103S, U16-ch104, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 22.54
Std Dev 11.15
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch104, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 34.31
Std Dev 3.532
Entry
ampl
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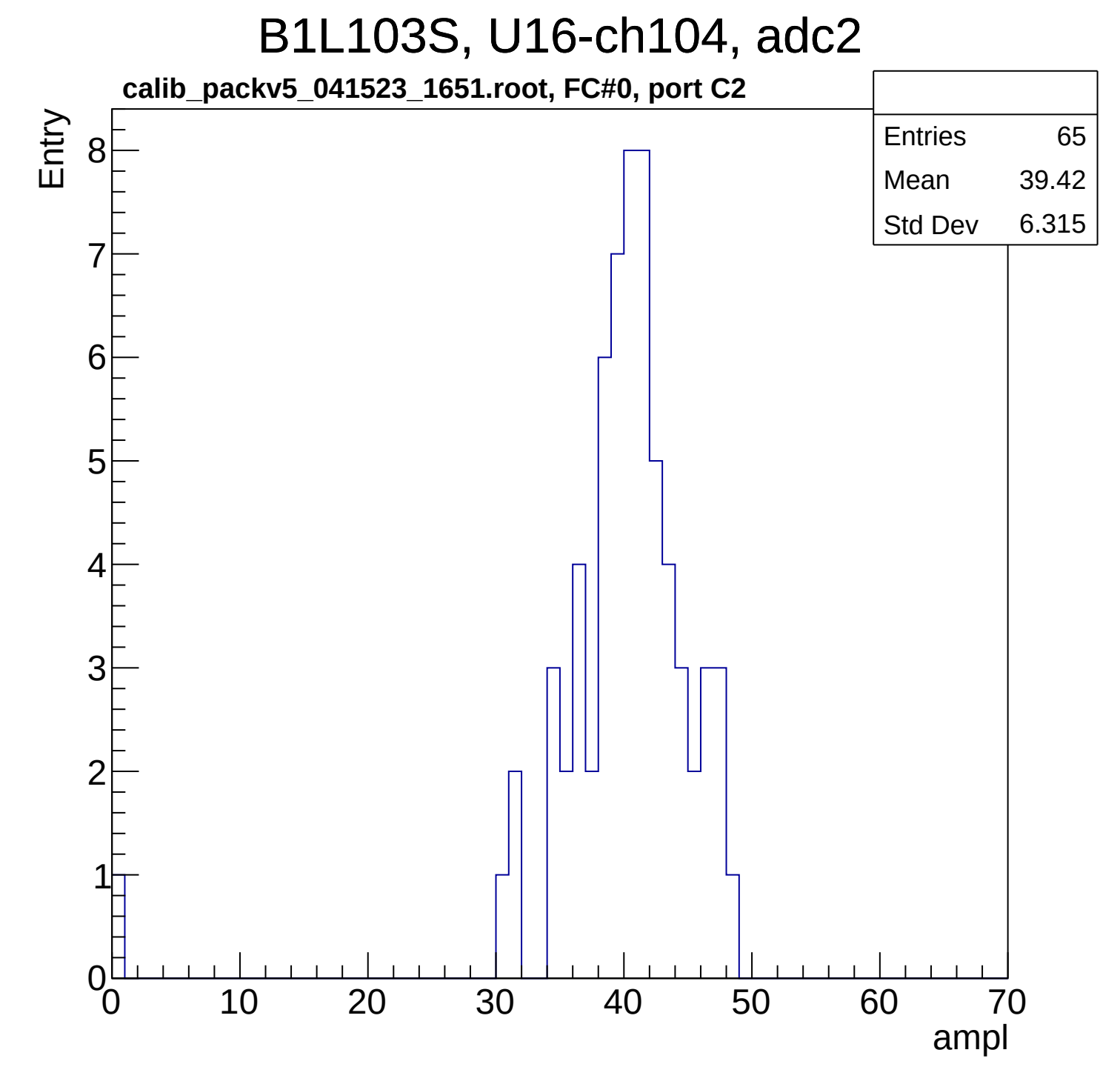
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch104, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 39.42
Std Dev 6.315
Entry
ampl
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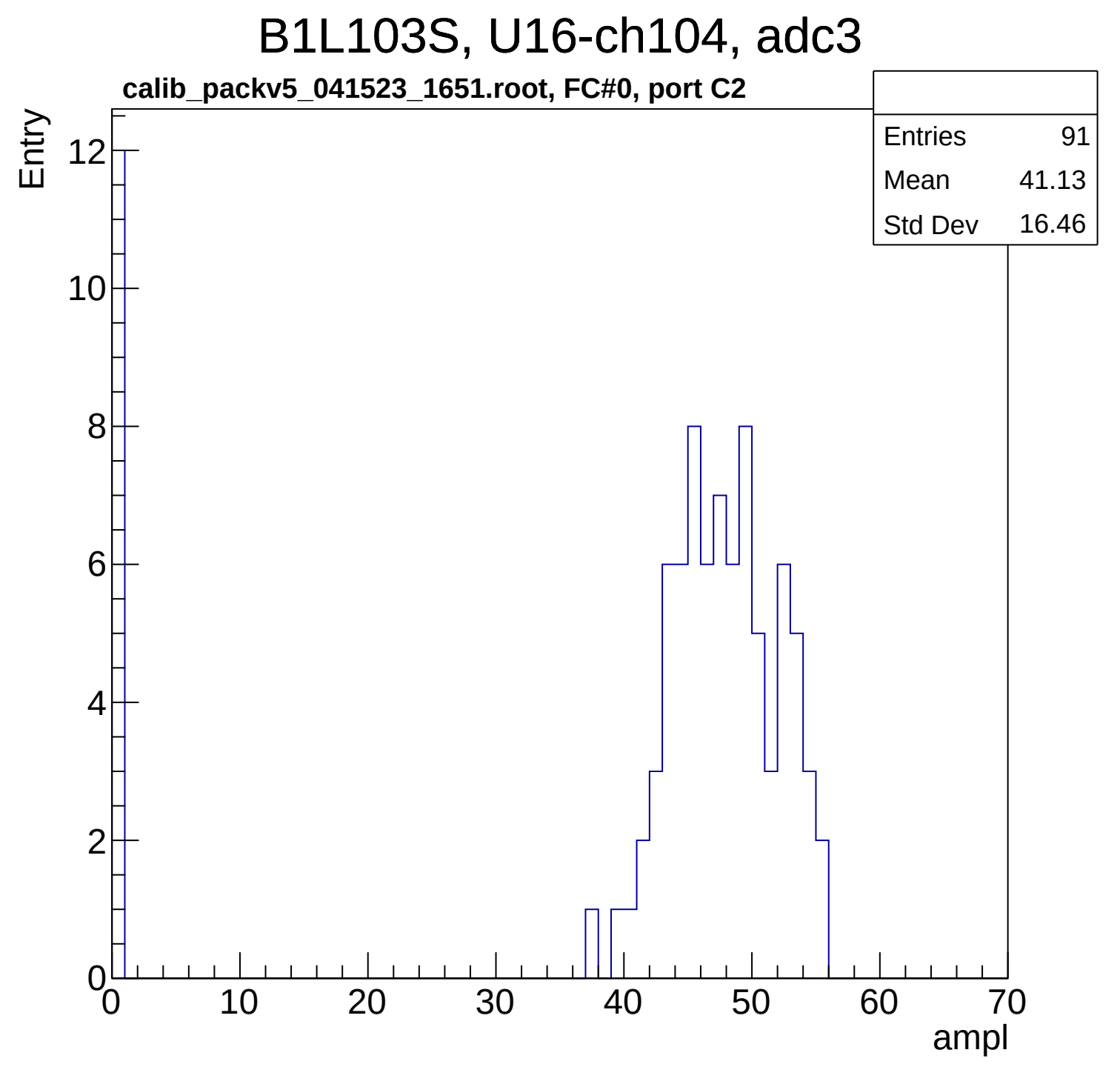
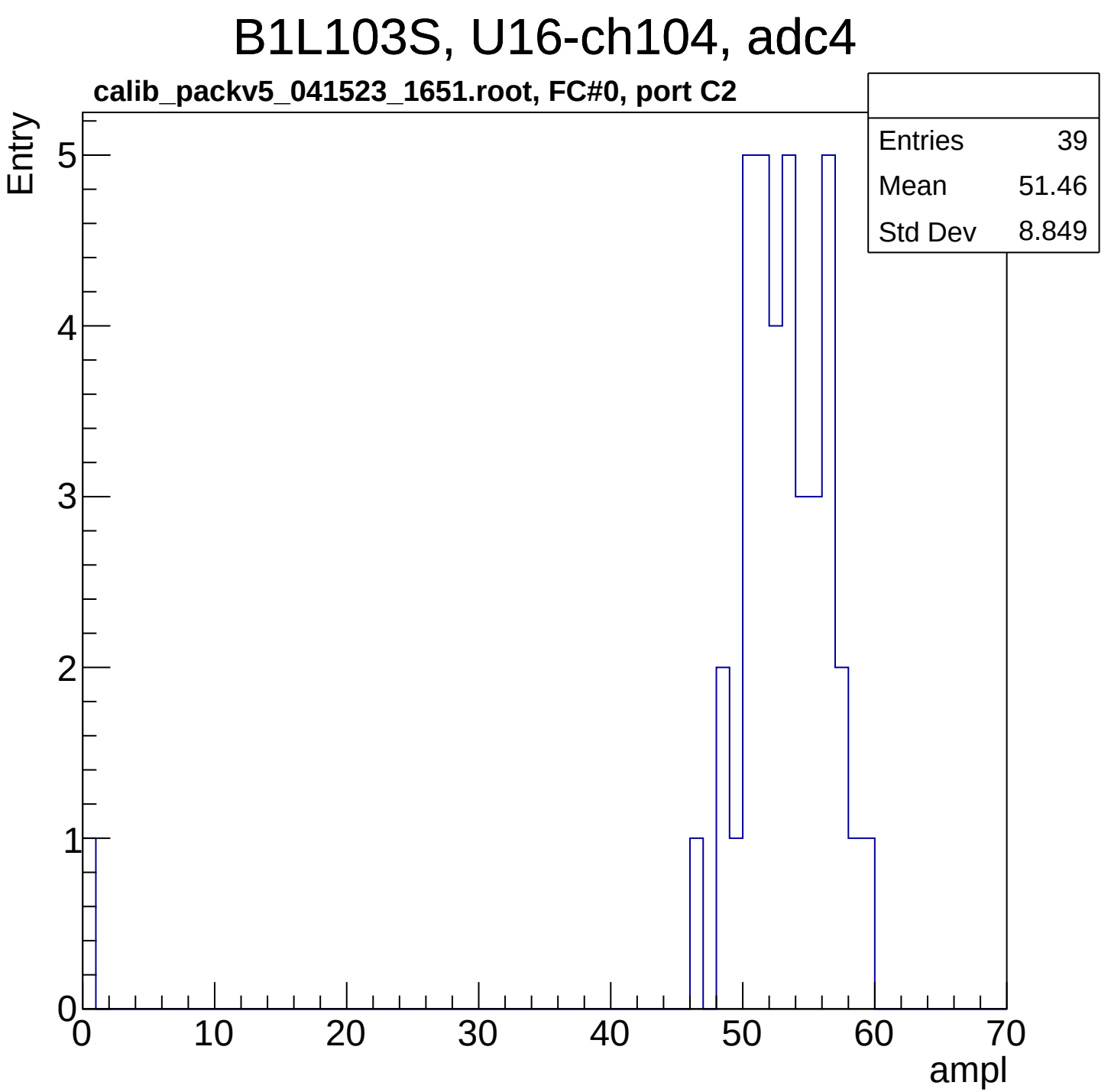
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch104, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 41.13
Std Dev 16.46
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch104, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 51.46
Std Dev 8.849
Entry
ampl
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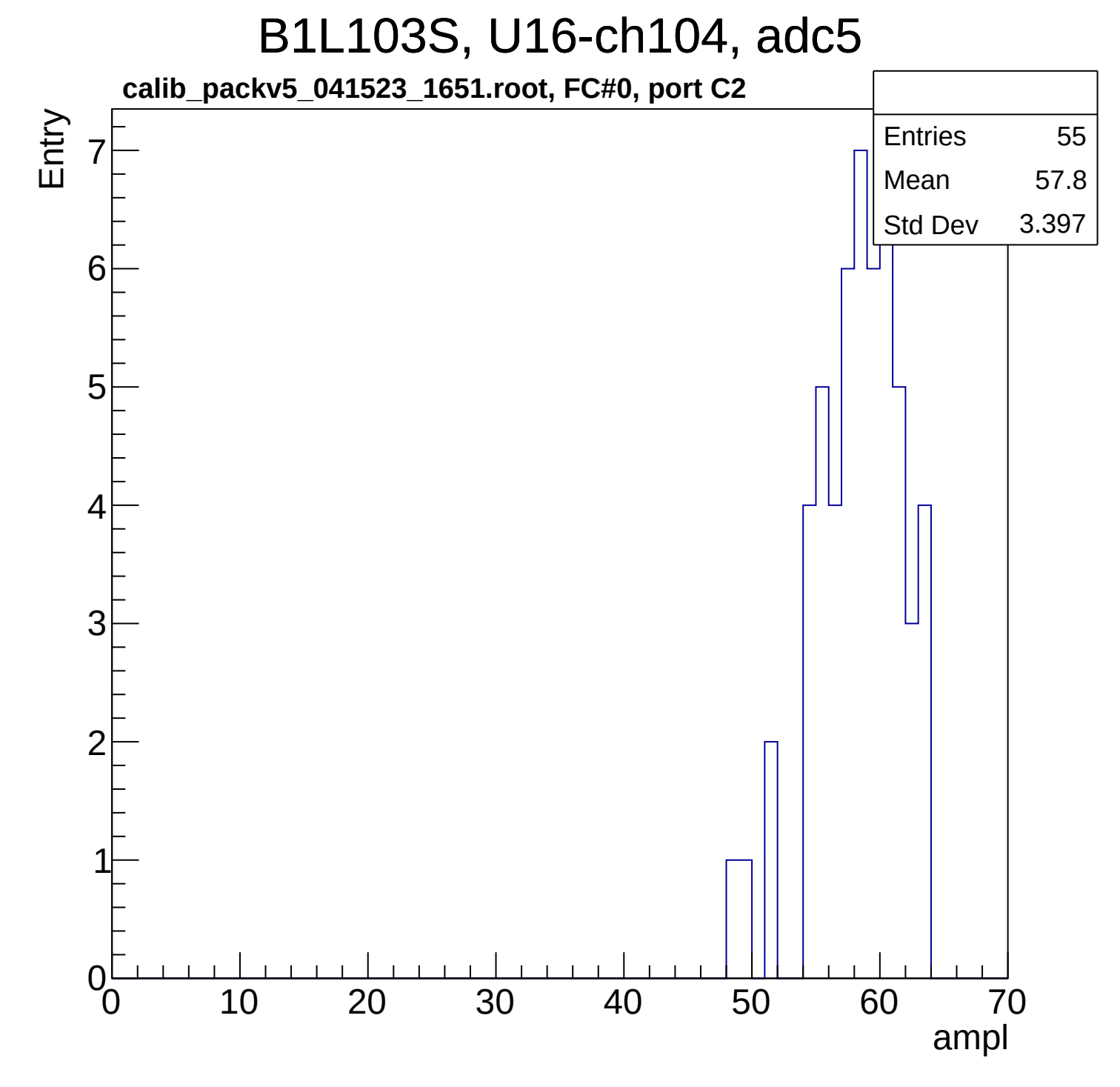
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U16-ch104, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.8
Std Dev 3.397
Entry
ampl
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3
4
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6
7
0
10
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60
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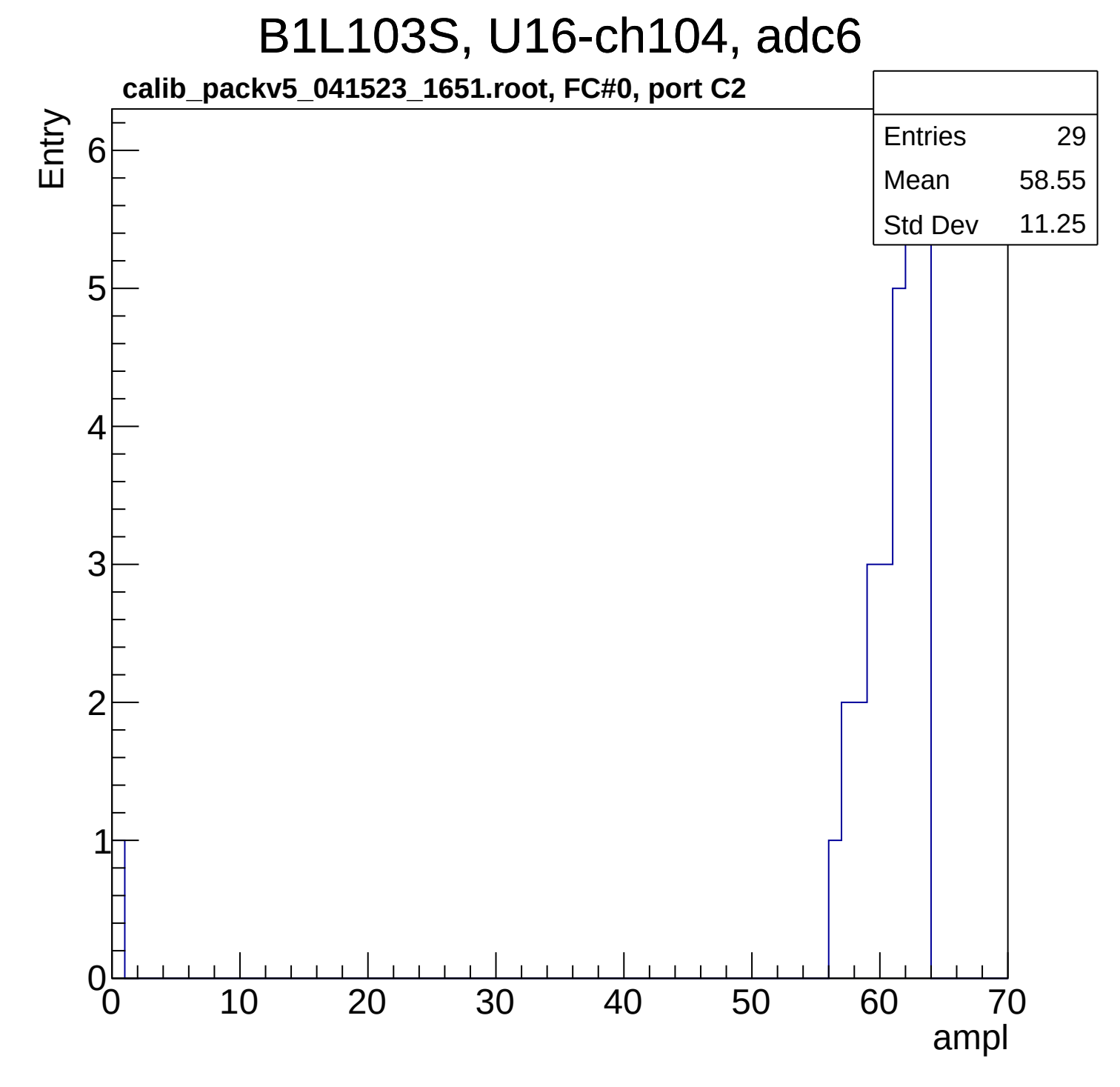
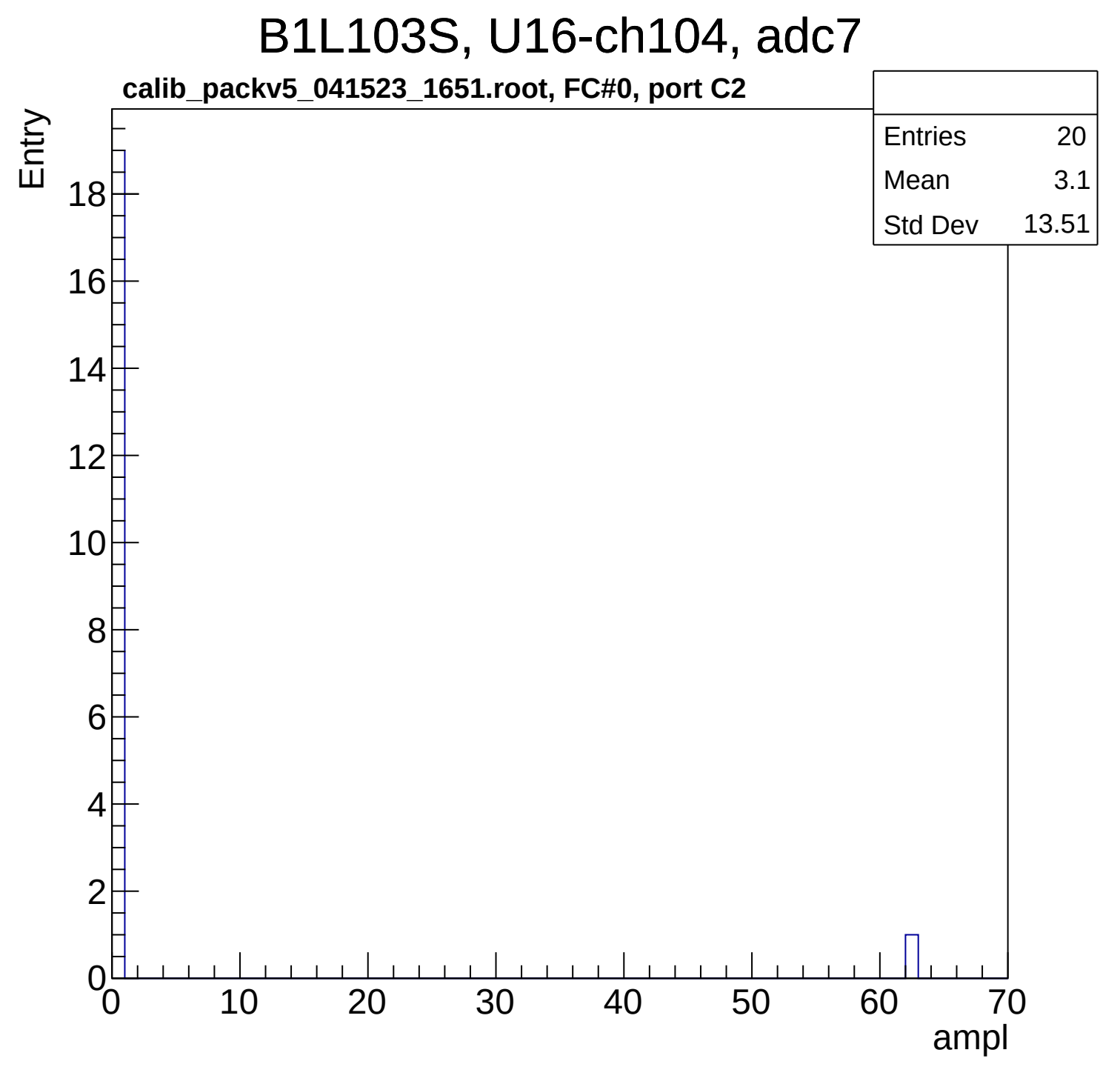
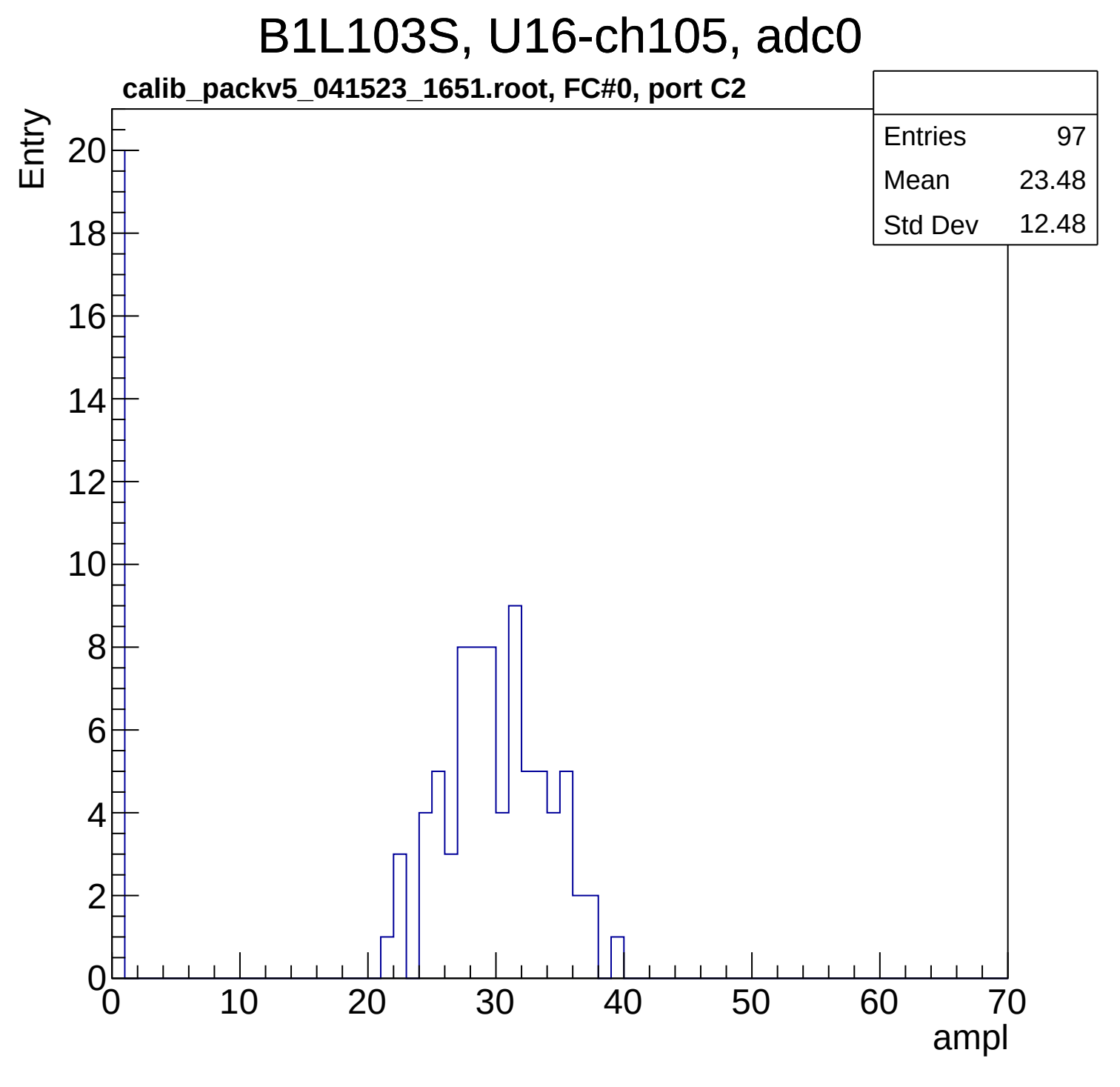

B1L103S, U16-ch104, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 58.55
Std Dev 11.25
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U16-ch104, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch105, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 23.48
Std Dev 12.48
Entry
ampl
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4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
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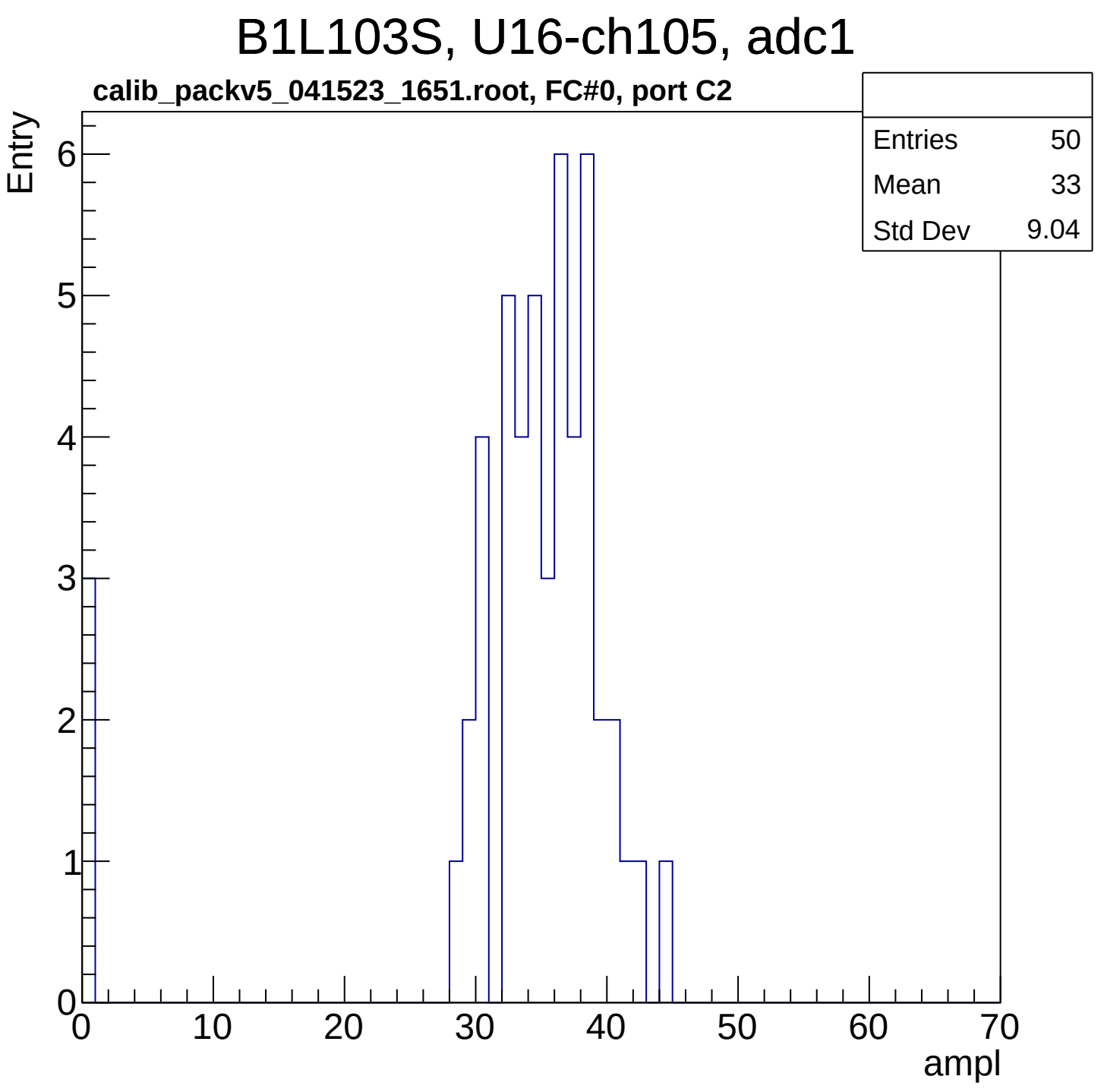
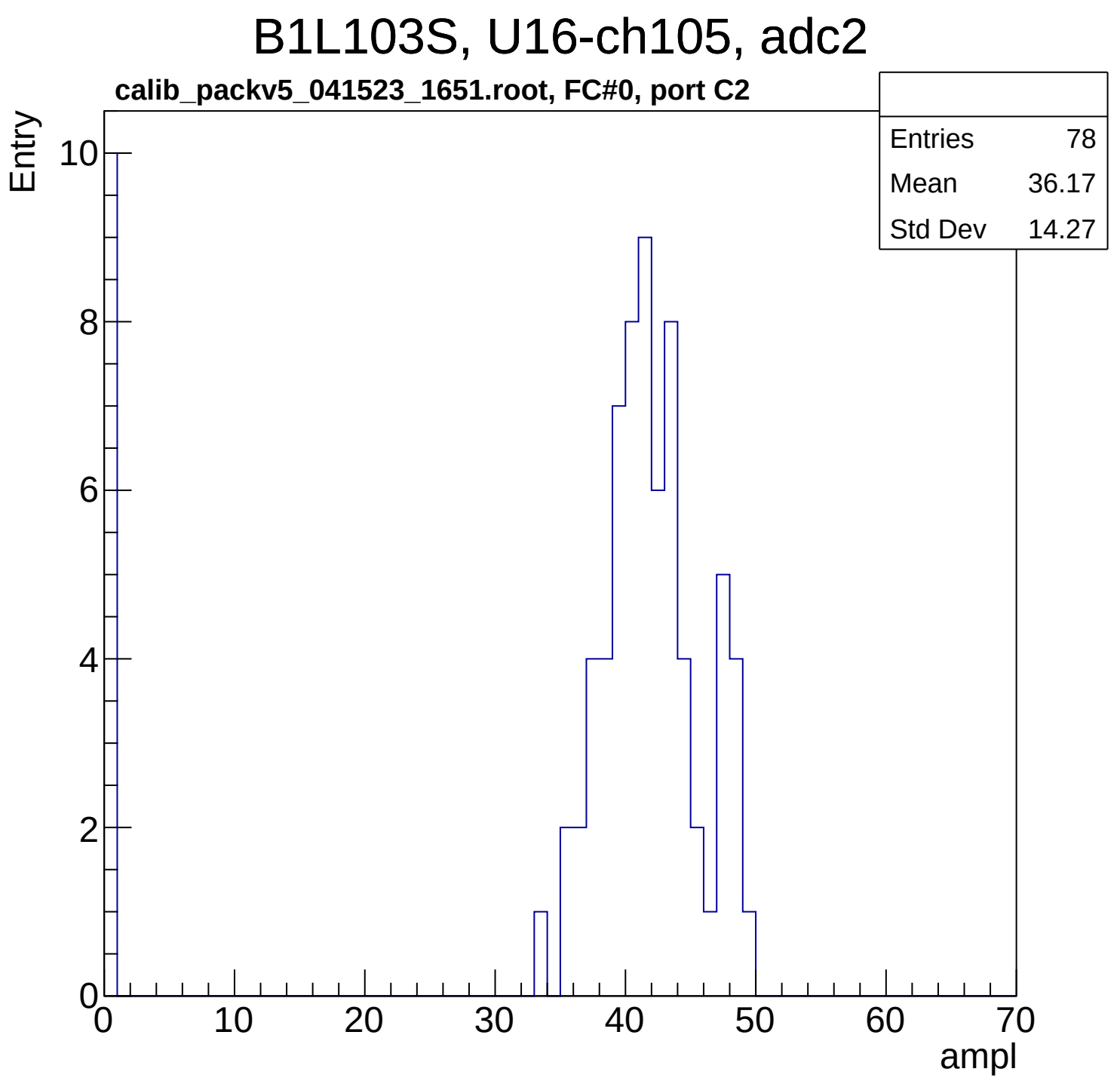
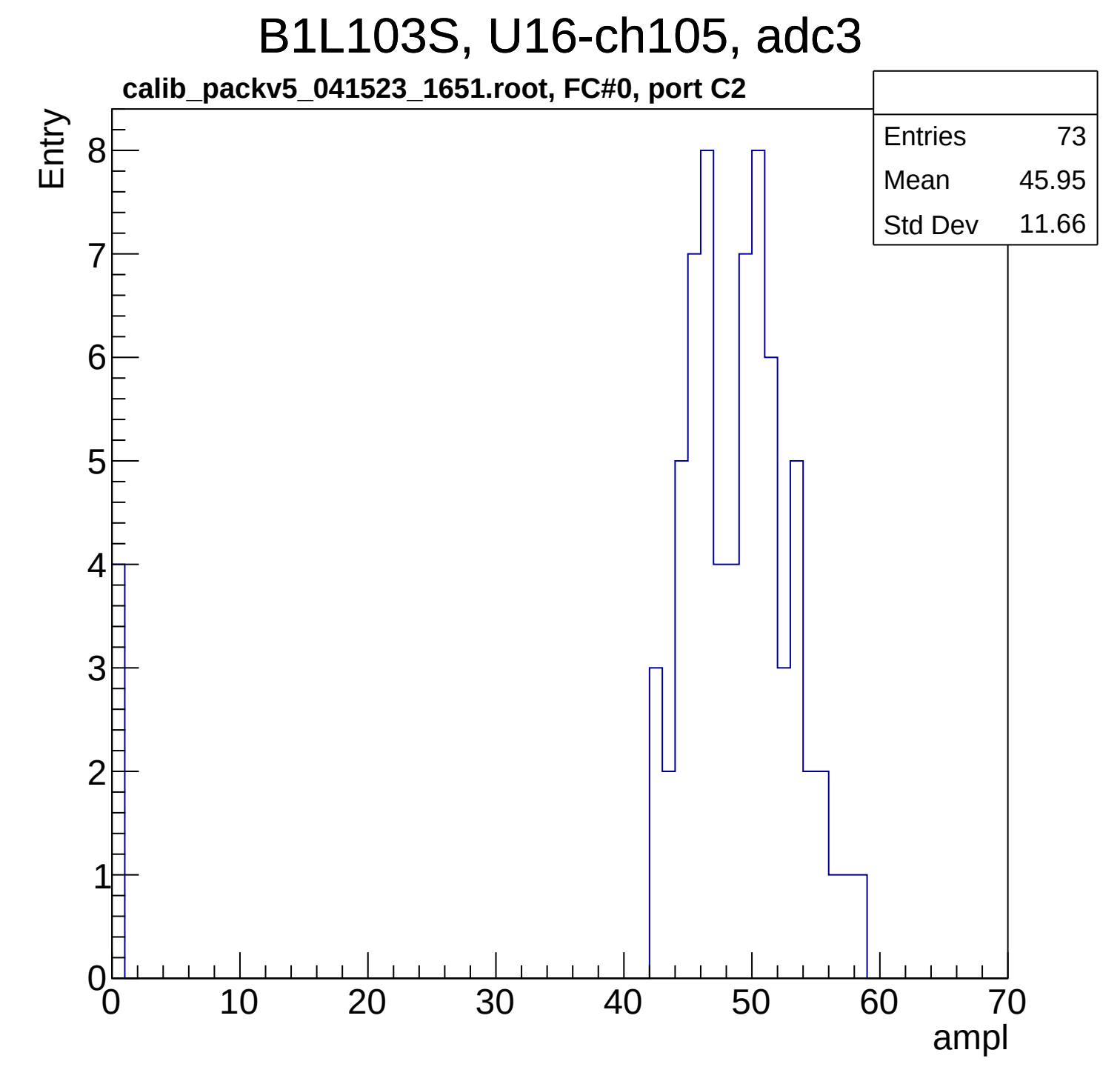

B1L103S, U16-ch105, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 33
Std Dev 9.04
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch105, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 36.17
Std Dev 14.27
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch105, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 45.95
Std Dev 11.66
Entry
ampl
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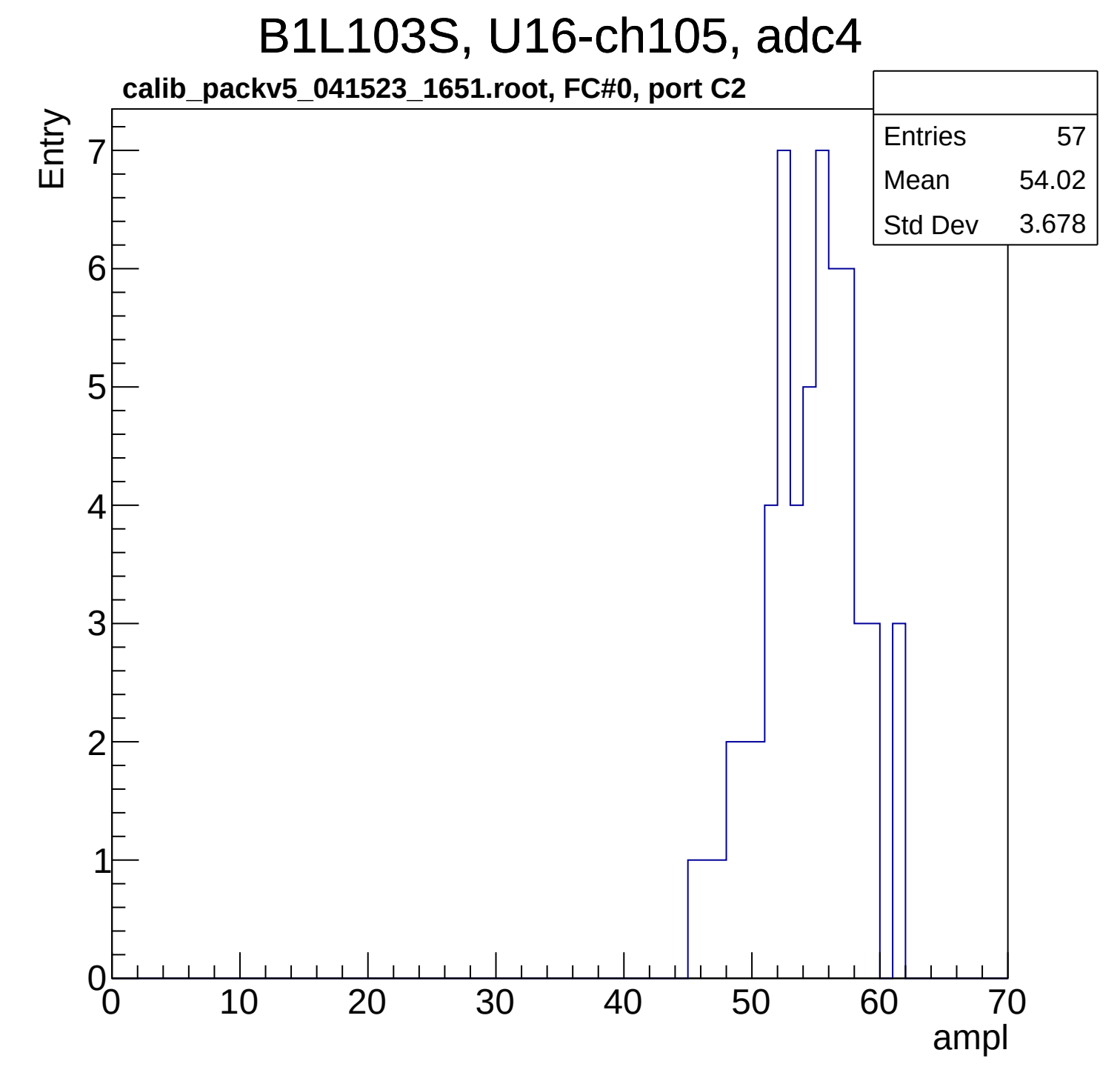
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch105, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 54.02
Std Dev 3.678
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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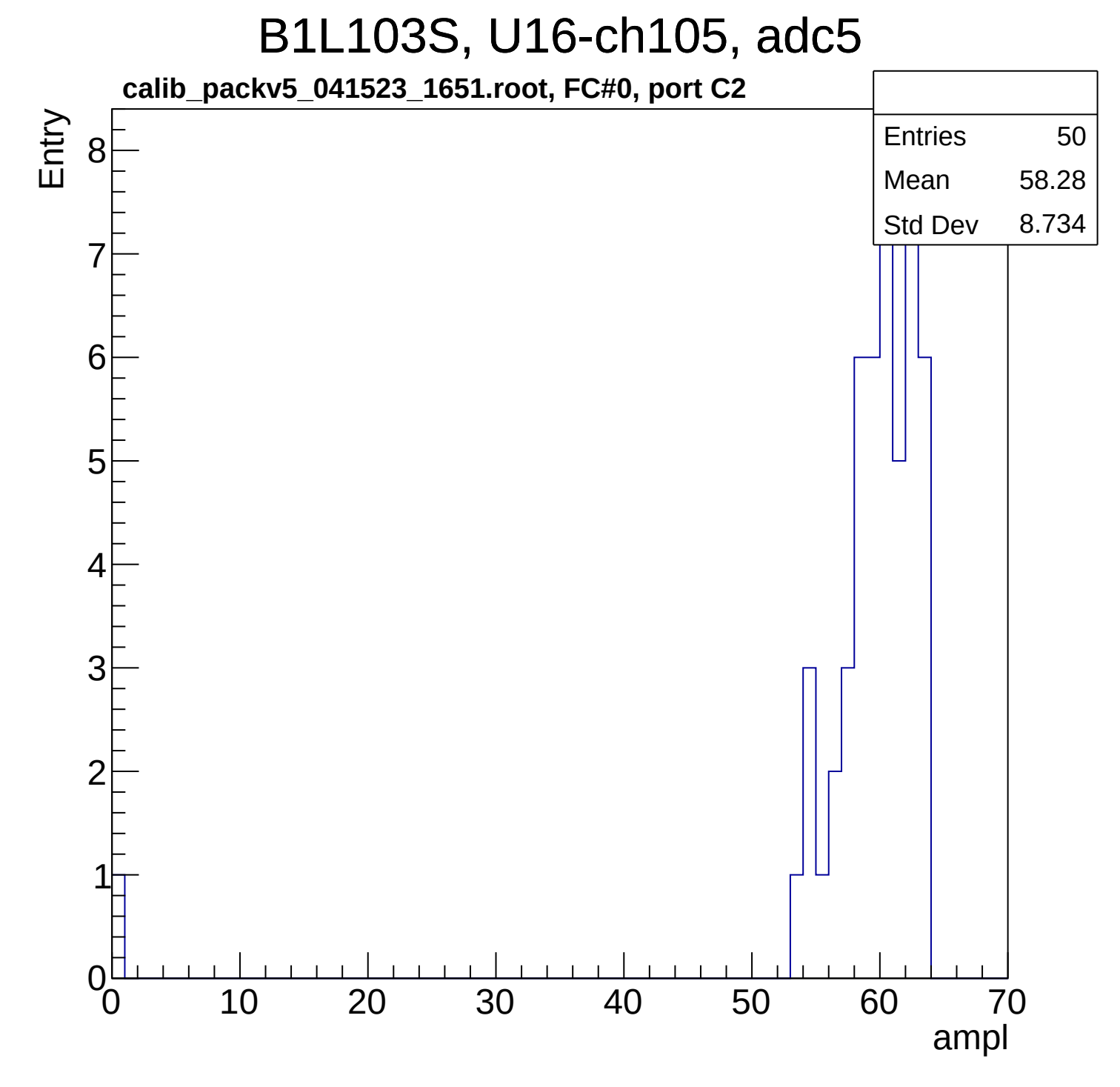
B1L103S, U16-ch105, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.28
Std Dev 8.734
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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40
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60
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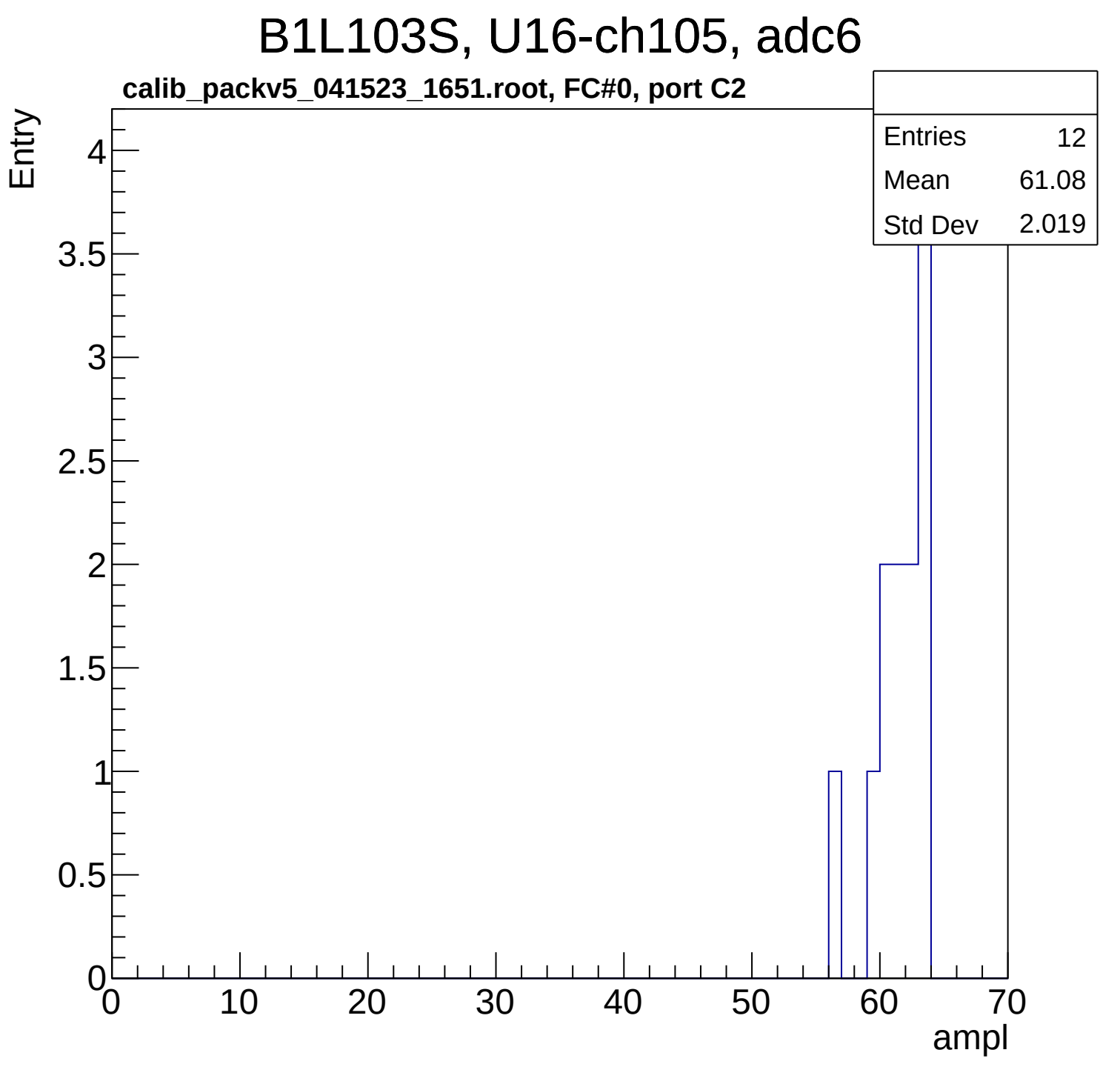
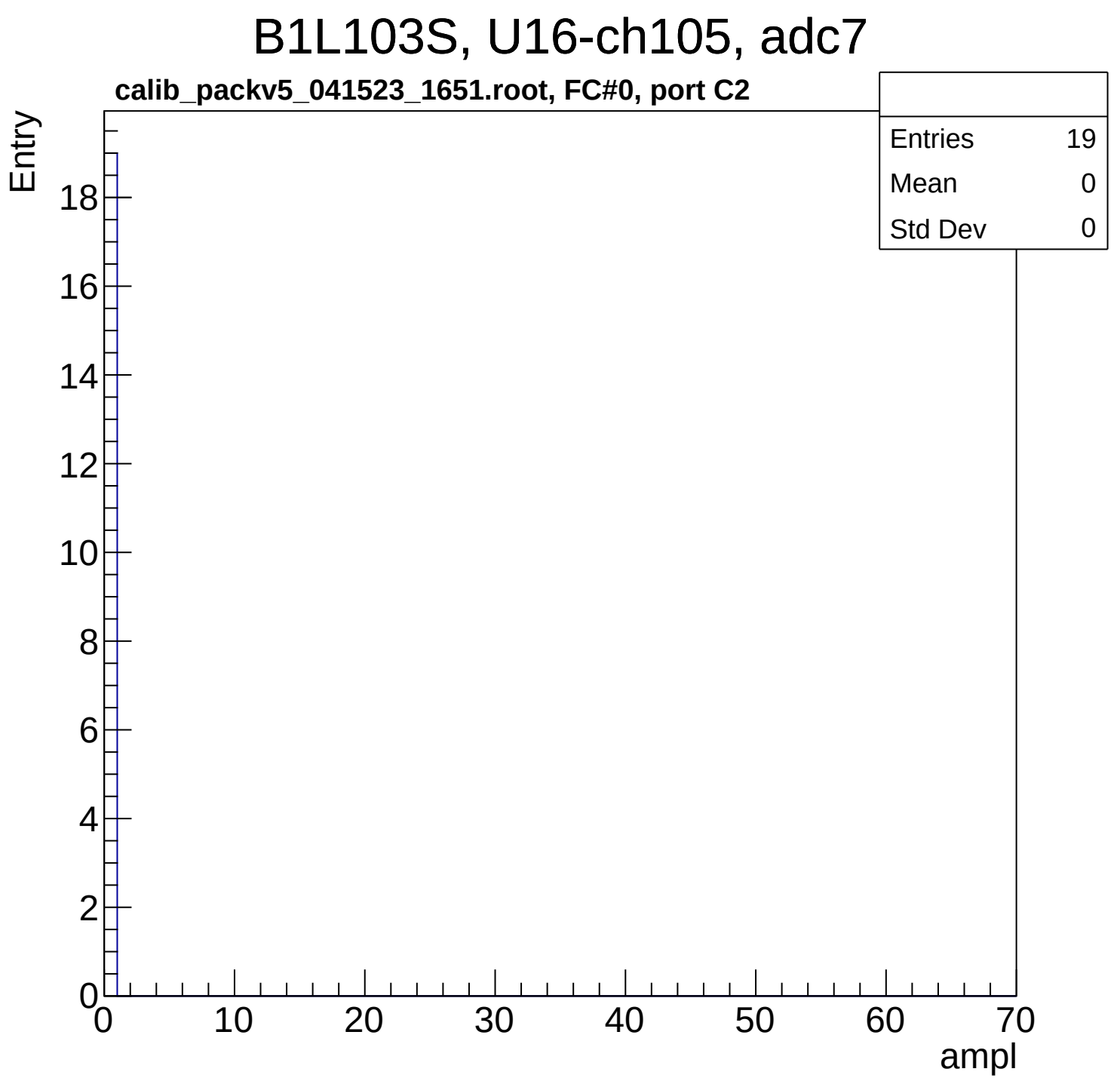

B1L103S, U16-ch105, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.08
Std Dev 2.019
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U16-ch105, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
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6
8
10
12
14
16
18
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20
30
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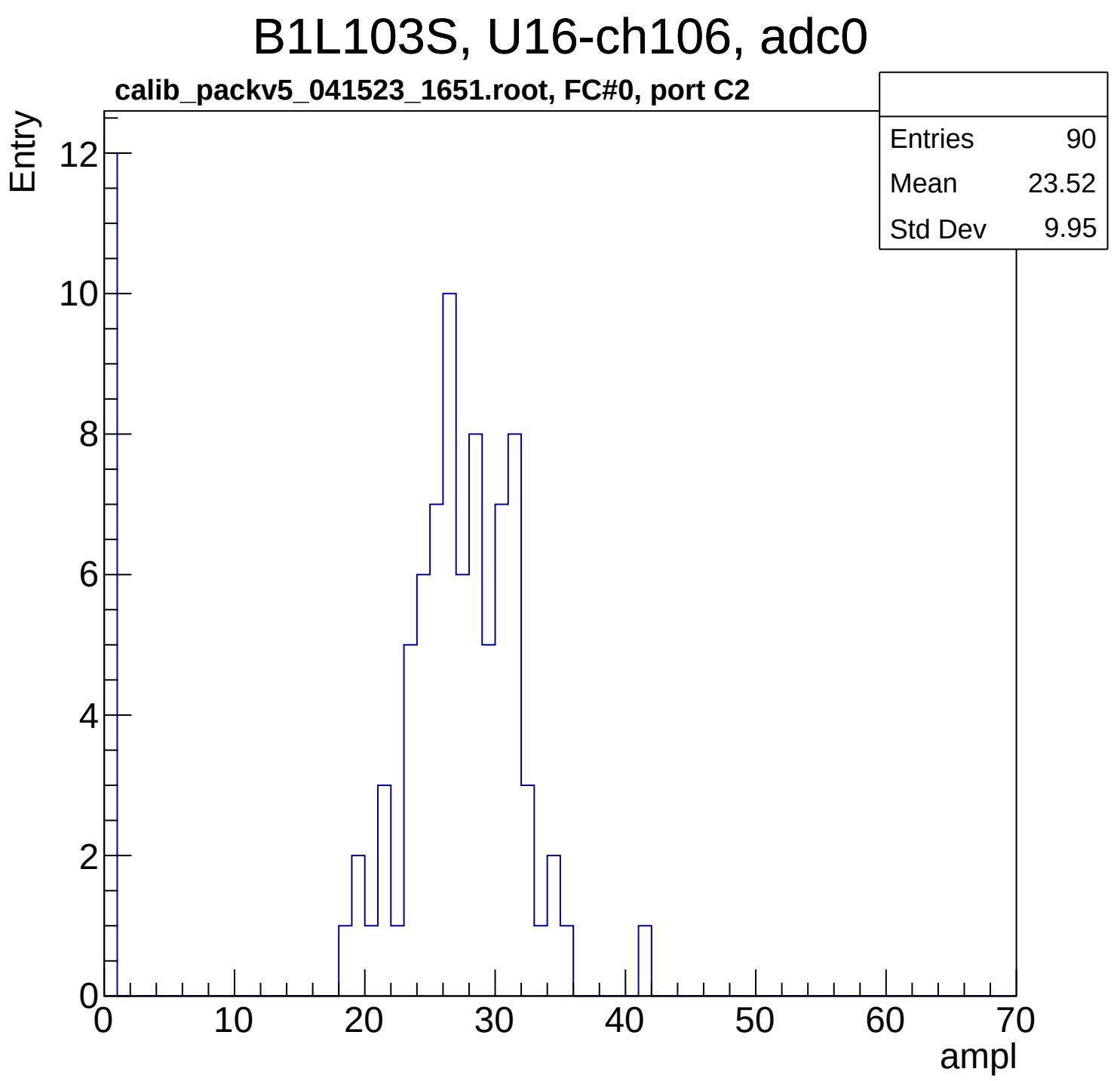
50
60
70
ampl


B1L103S, U16-ch106, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 23.52
Std Dev 9.95
Entry
ampl
0
2
4
6
8
10
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0
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60
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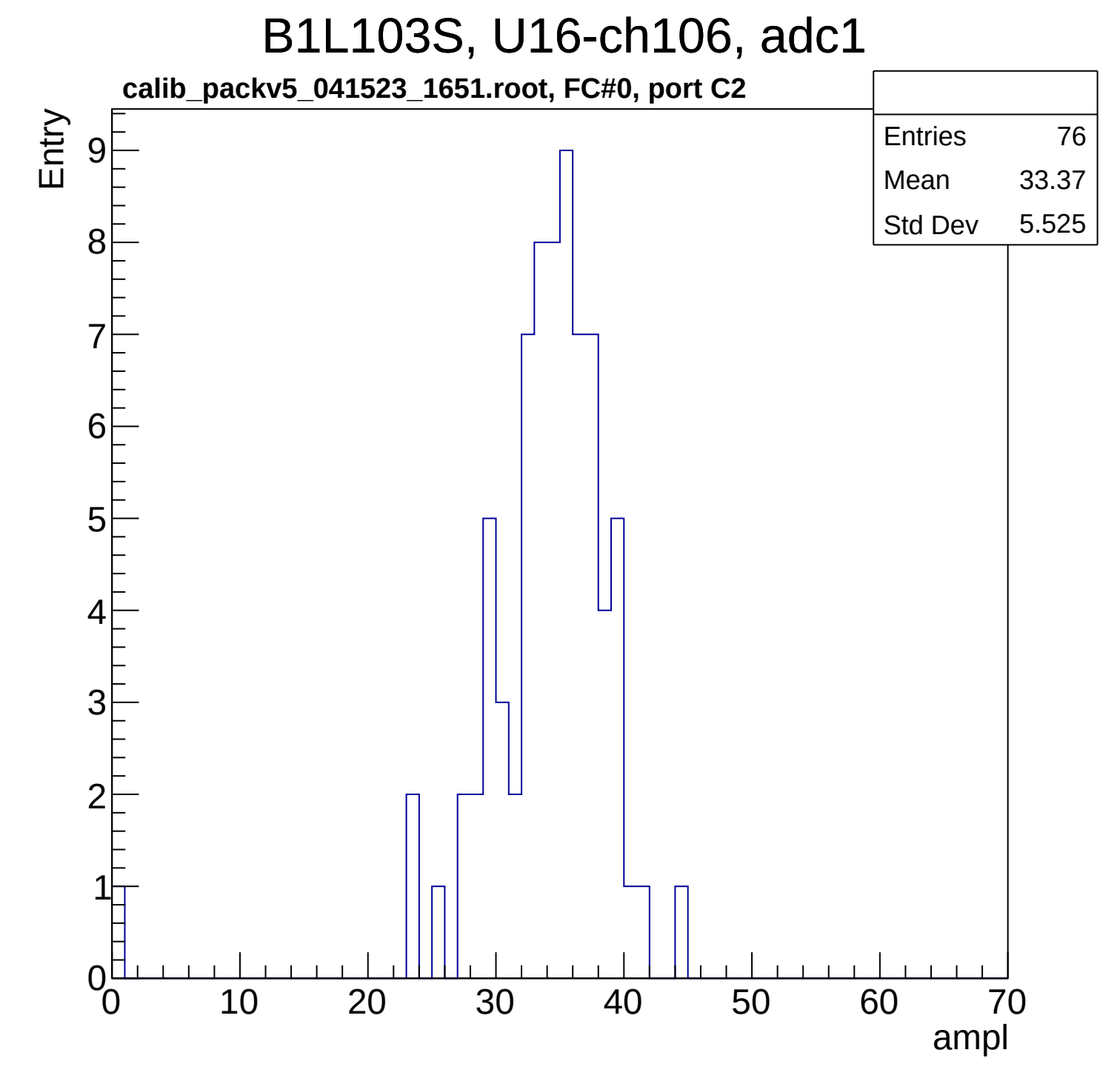
B1L103S, U16-ch106, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 33.37
Std Dev 5.525
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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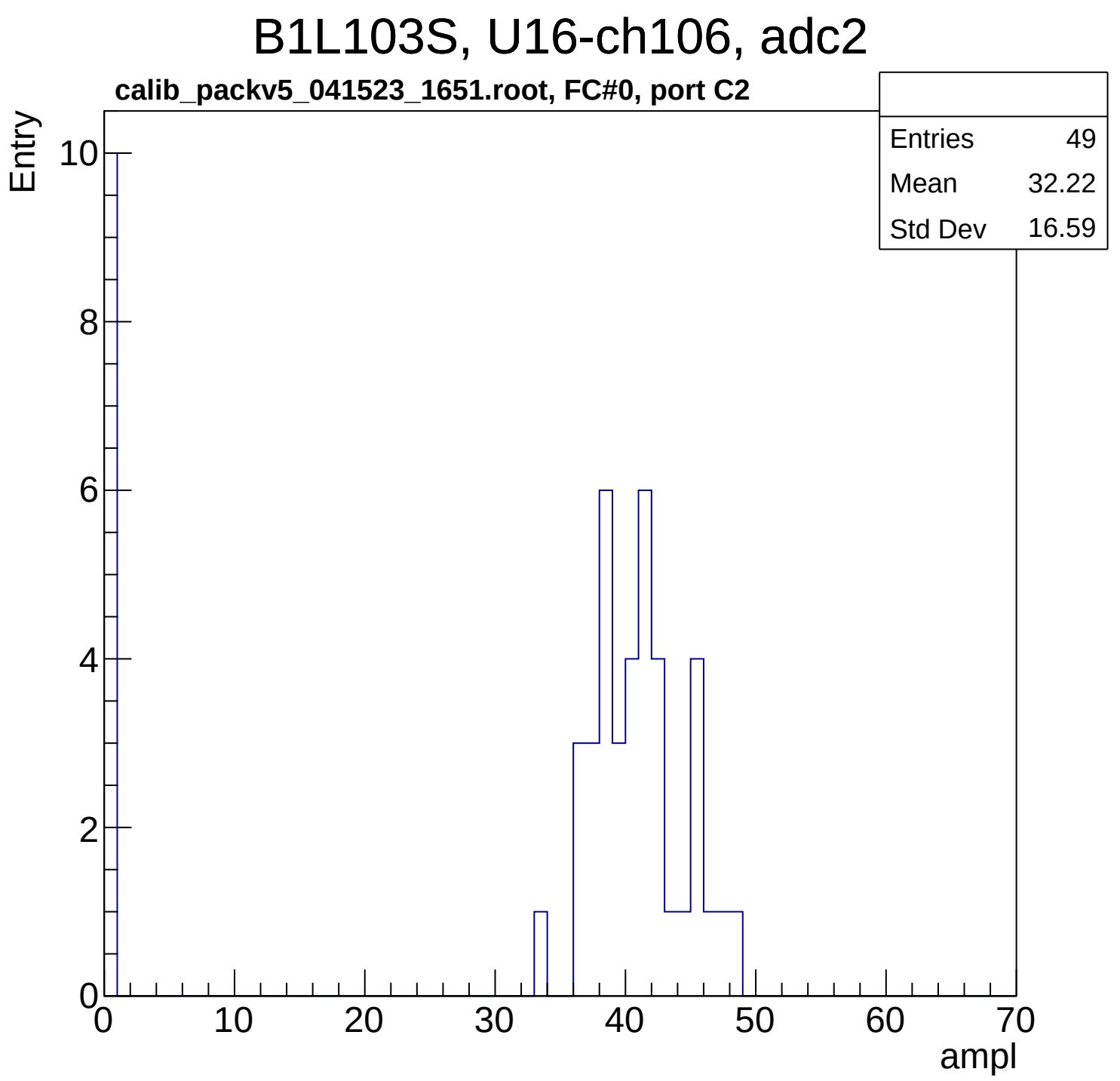
B1L103S, U16-ch106, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 32.22
Std Dev 16.59
Entry
ampl
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4
6
8
10
0
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30
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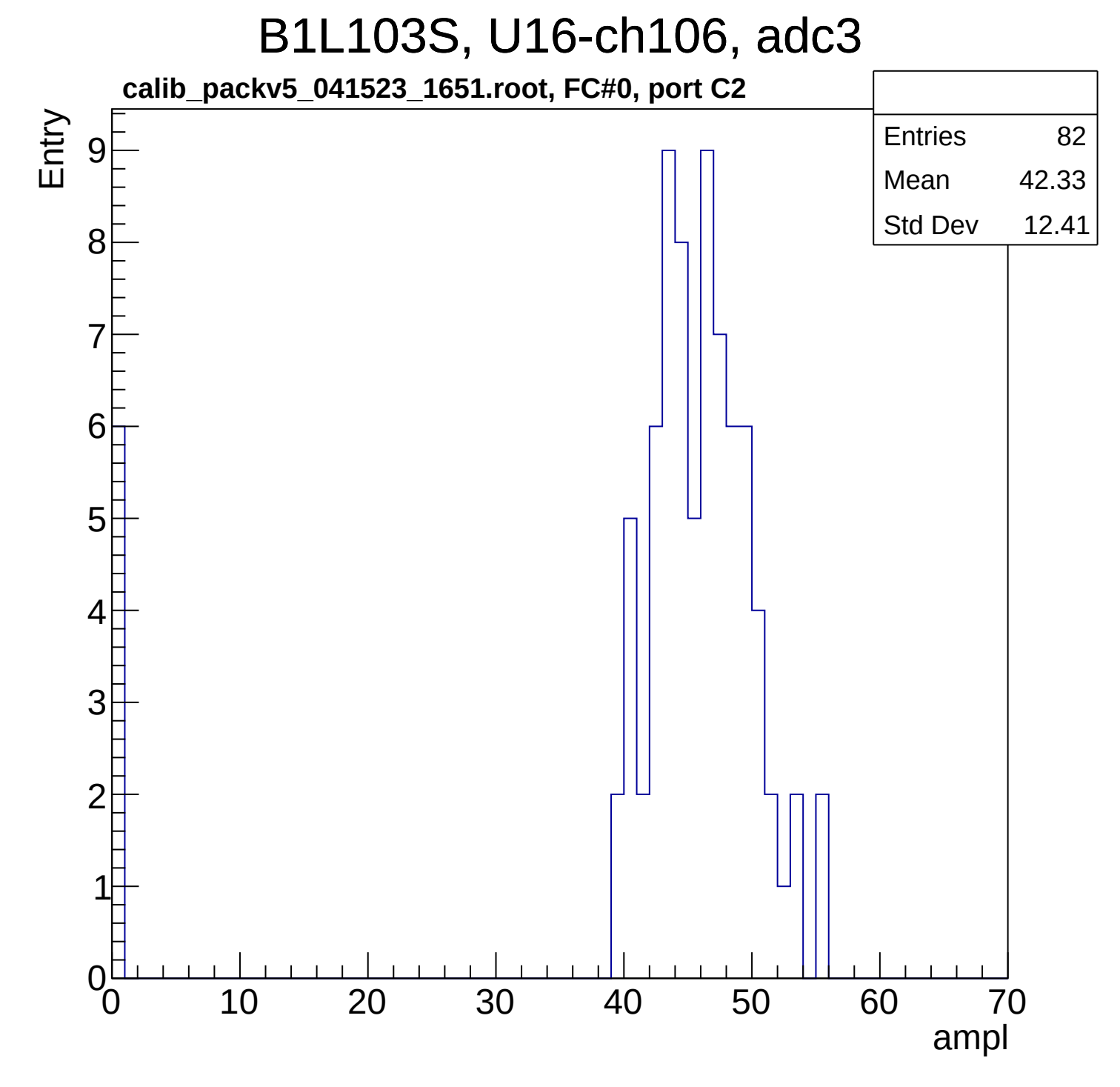
50
60
70


B1L103S, U16-ch106, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 42.33
Std Dev 12.41
Entry
ampl
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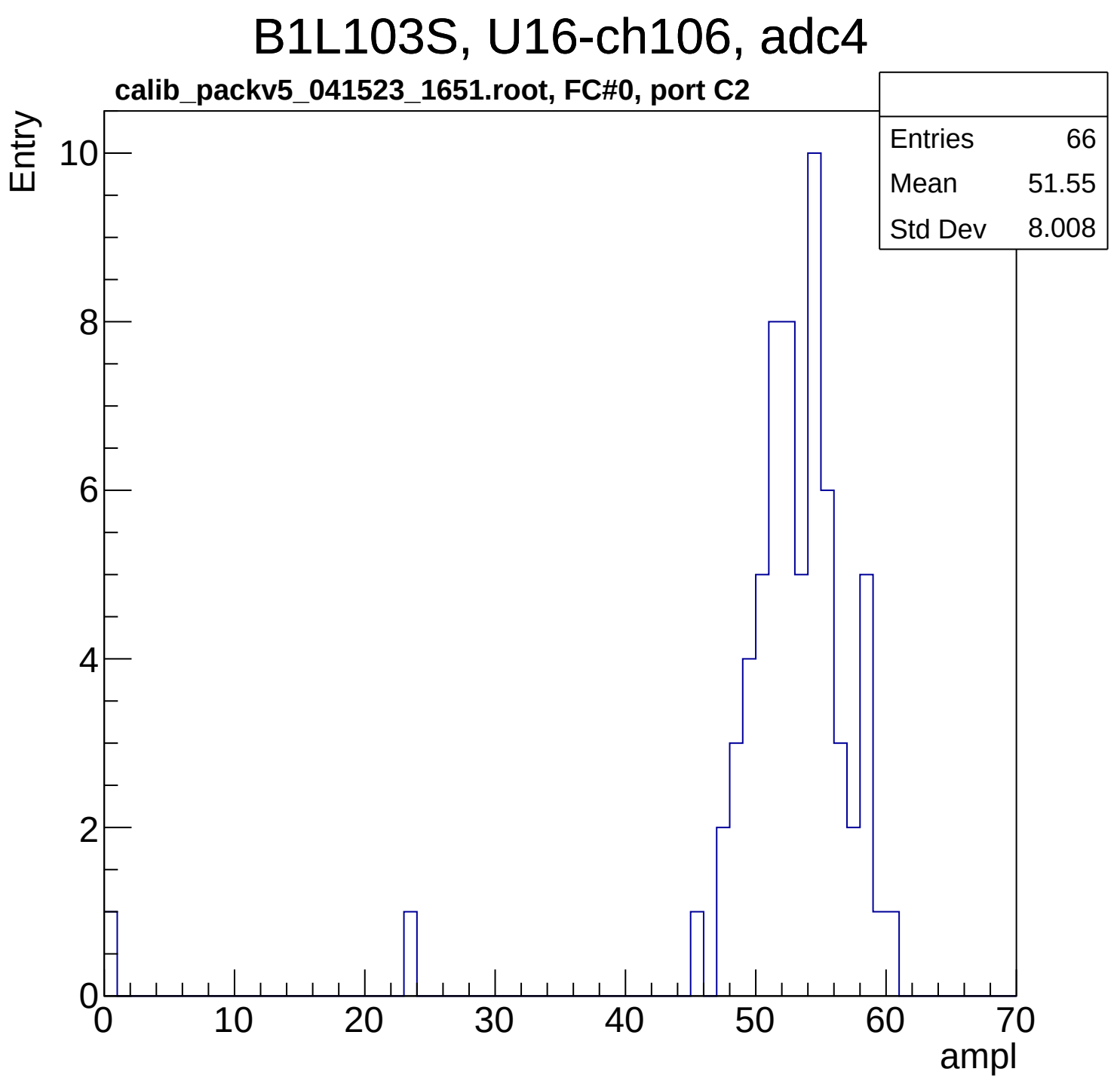
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch106, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 51.55
Std Dev 8.008
Entry
ampl
0
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4
6
8
10
0
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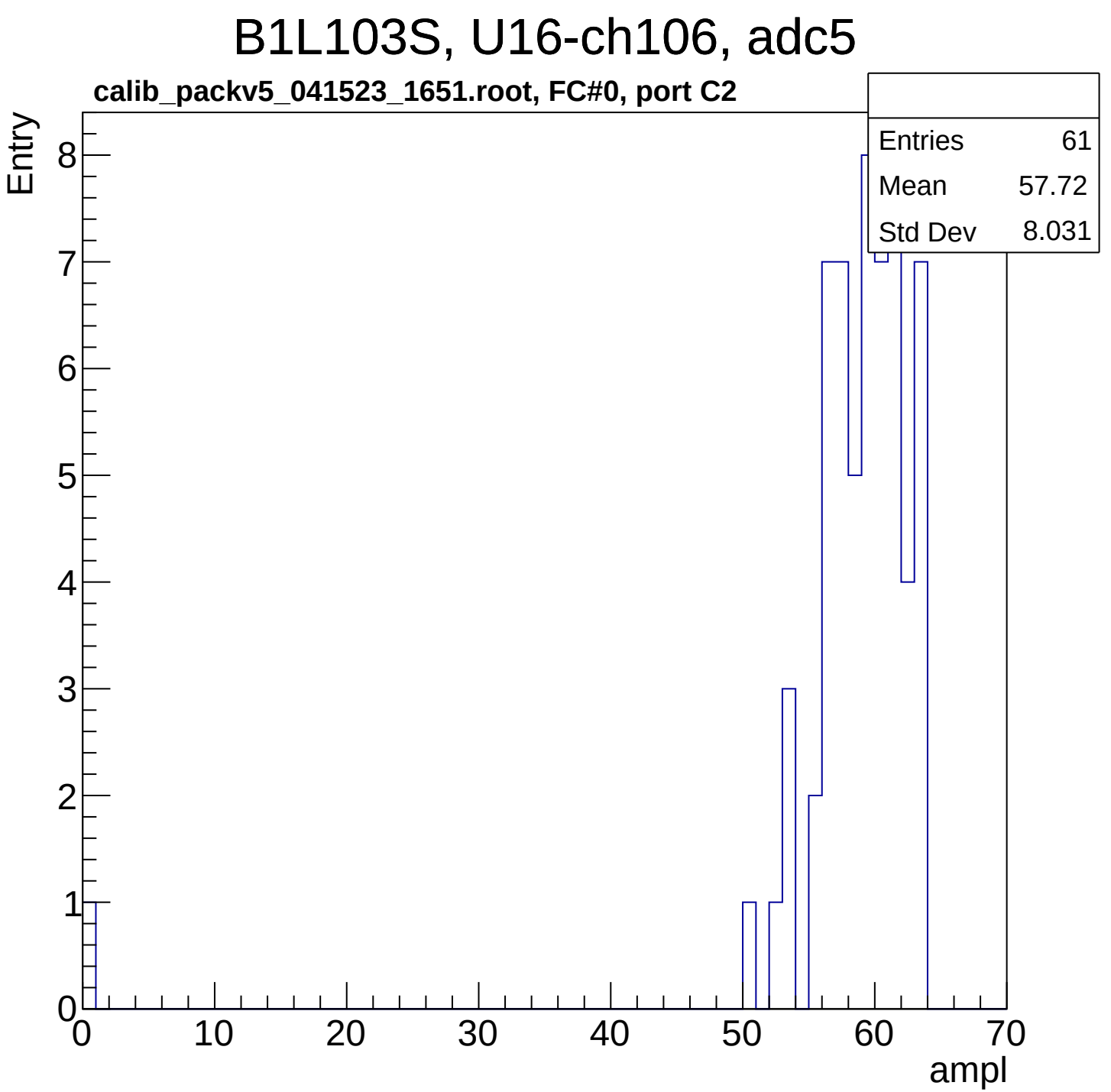
40
50
60
70


B1L103S, U16-ch106, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 57.72
Std Dev 8.031
Entry
ampl
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2
3
4
5
6
7
8
0
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40
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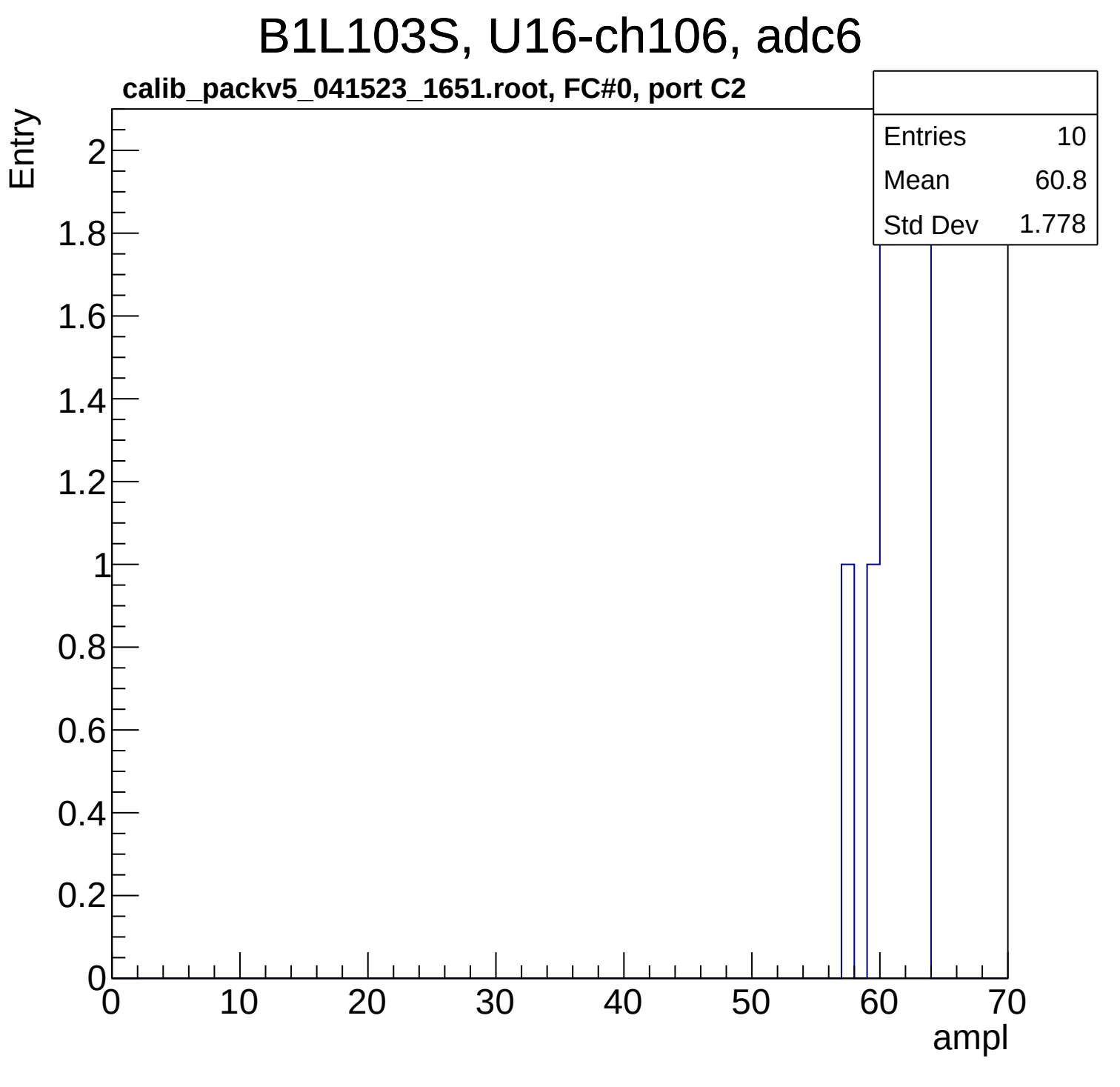
60
70


B1L103S, U16-ch106, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 60.8
Std Dev 1.778
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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20
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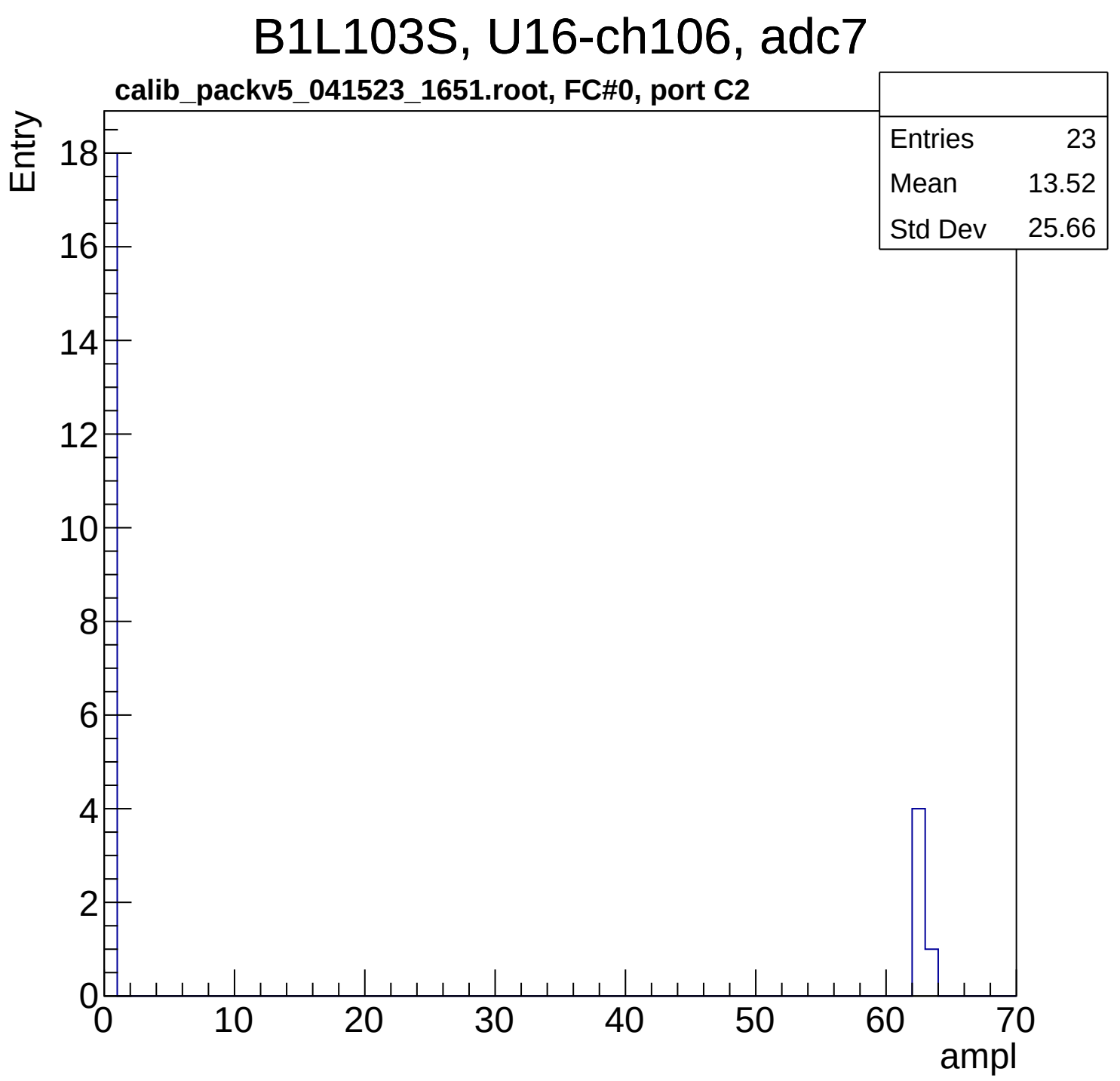
40
50
60
70


B1L103S, U16-ch106, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 13.52
Std Dev 25.66
Entry
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6
8
10
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14
16
18
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10
20
30
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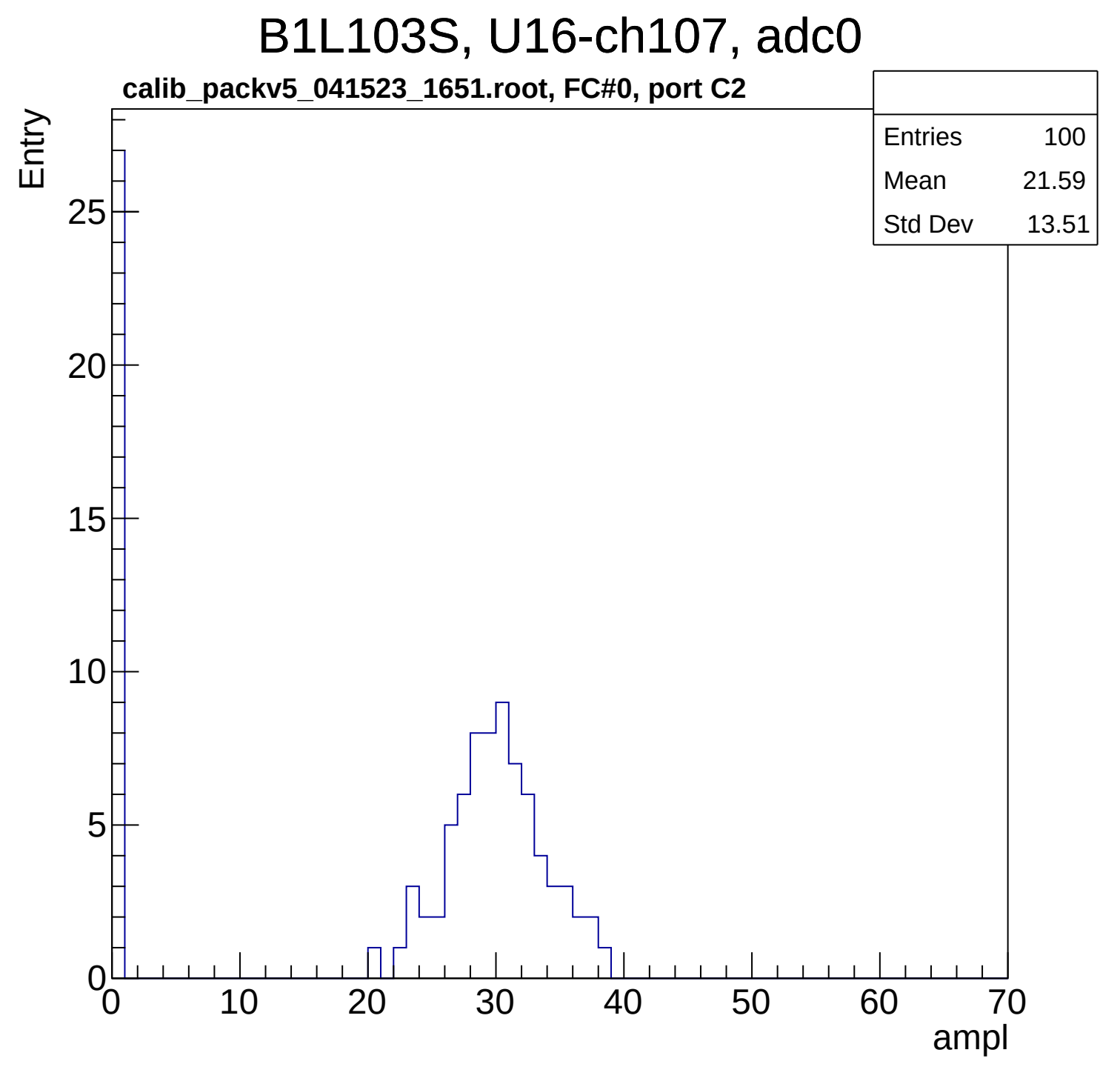
50
60
70
ampl


B1L103S, U16-ch107, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 21.59
Std Dev 13.51
Entry
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5
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15
20
25
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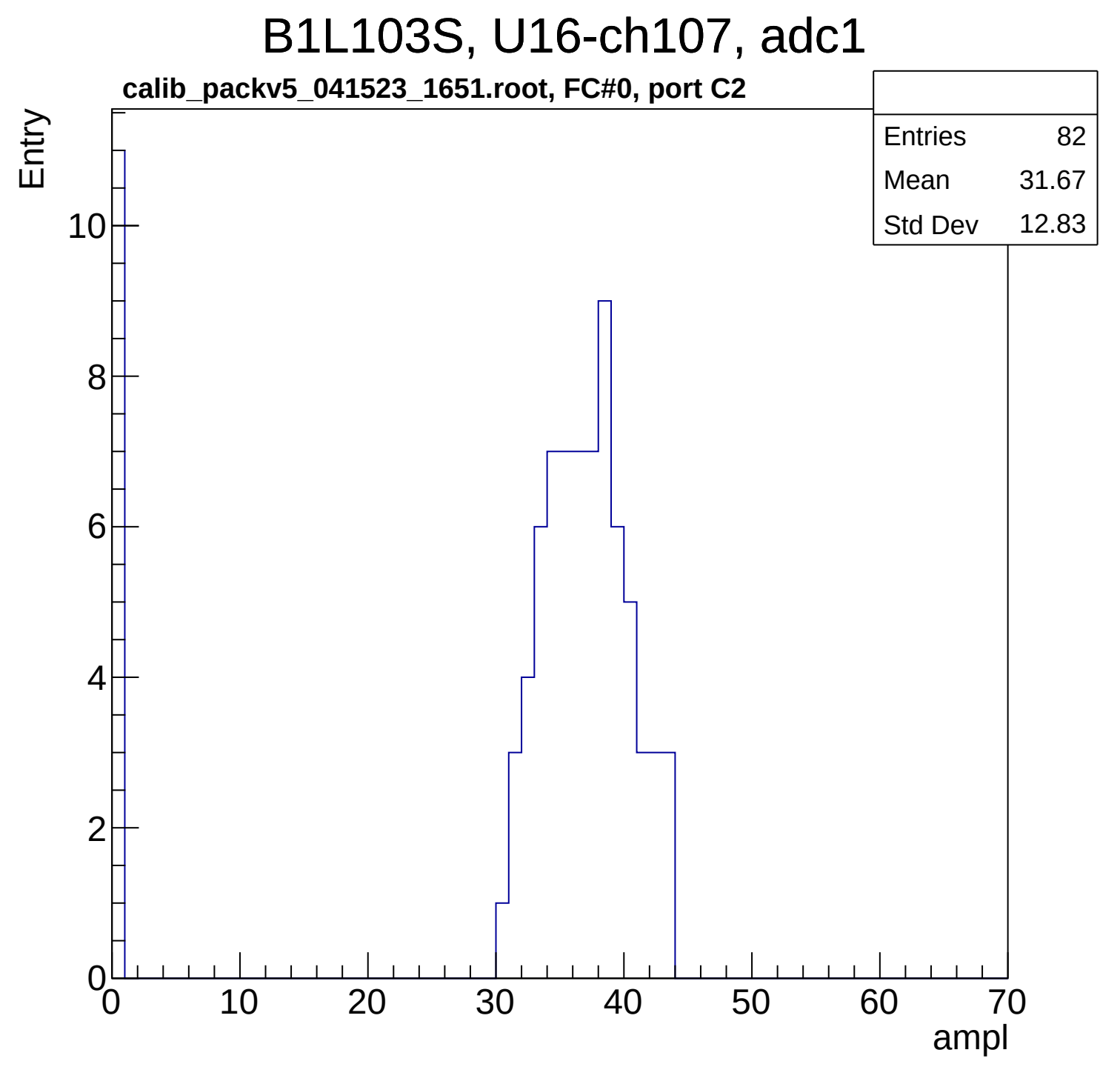
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch107, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 31.67
Std Dev 12.83
Entry
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2
4
6
8
10
0
10
20
30
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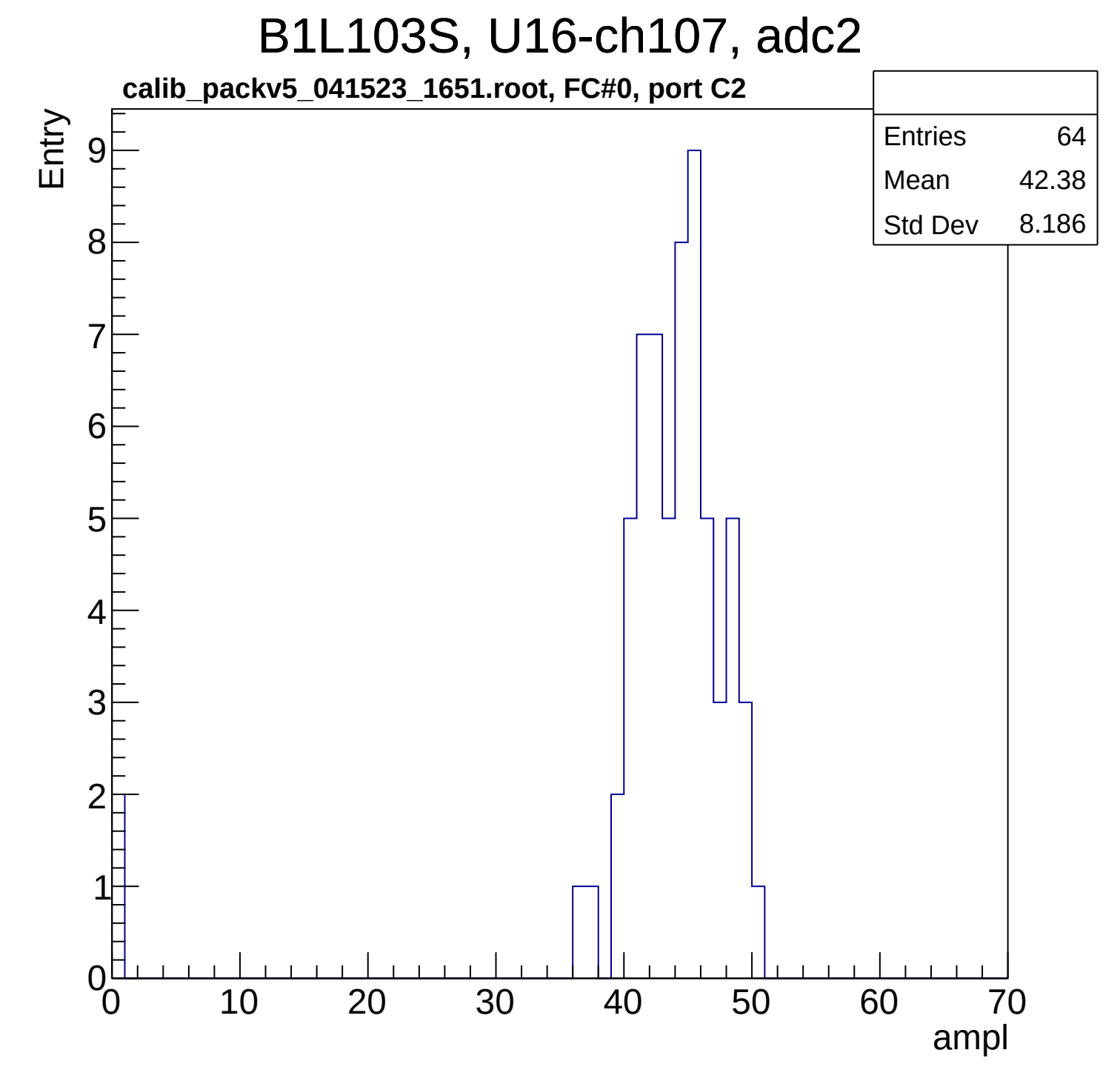
50
60
70
ampl


B1L103S, U16-ch107, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 42.38
Std Dev 8.186
Entry
ampl
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3
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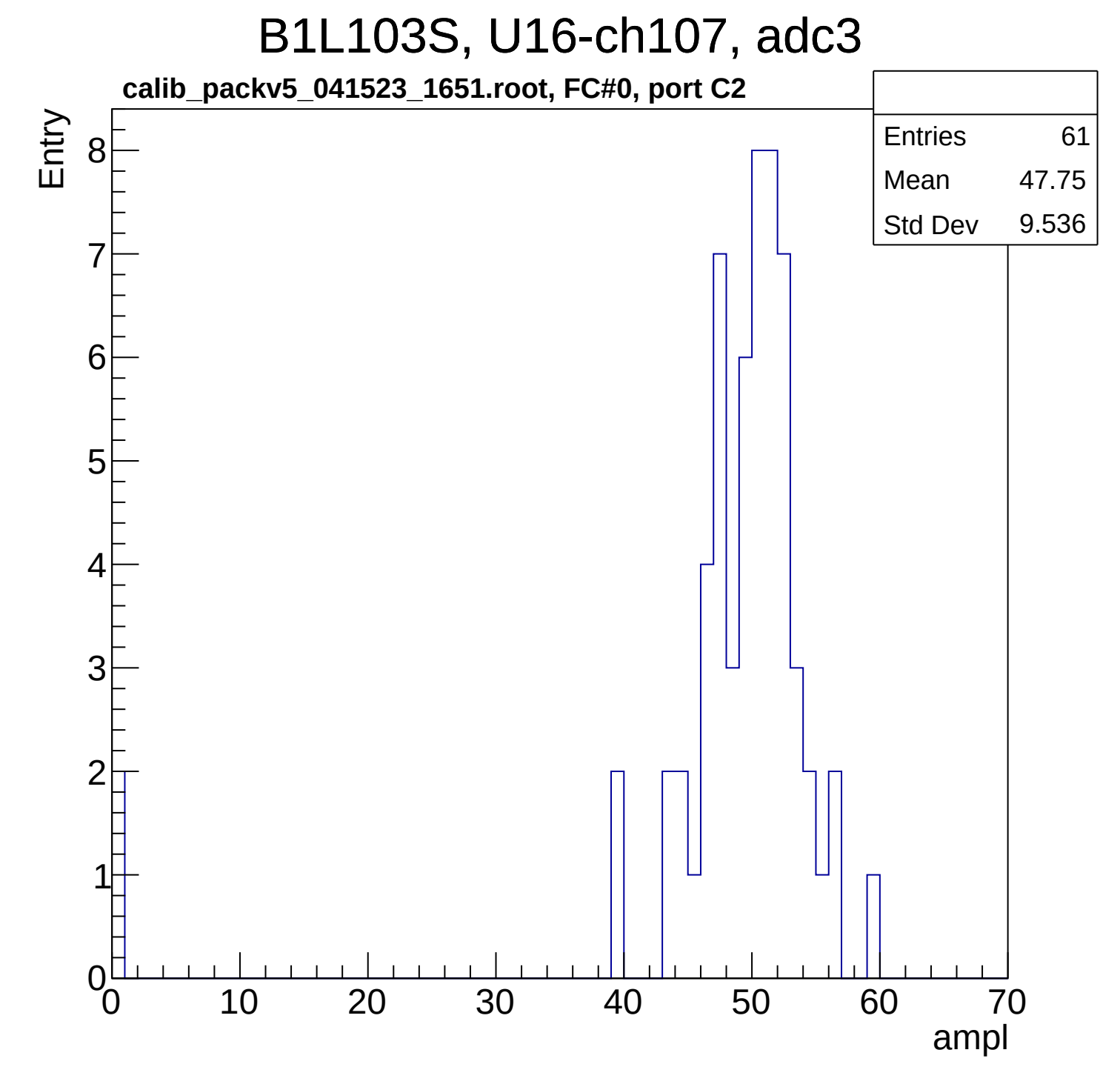
B1L103S, U16-ch107, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 47.75
Std Dev 9.536
Entry
ampl
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7
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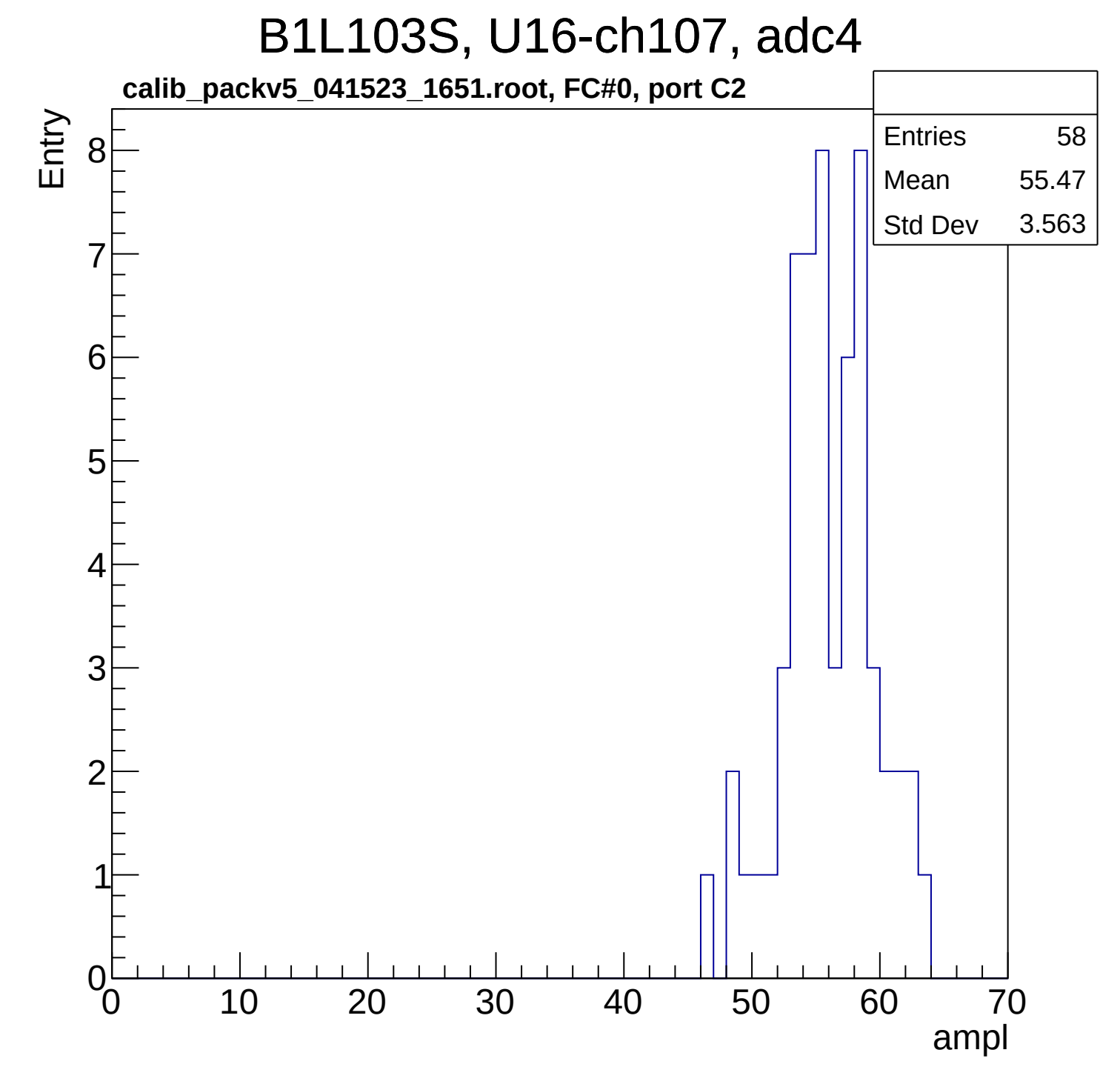
B1L103S, U16-ch107, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 55.47
Std Dev 3.563
Entry
ampl
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40
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60
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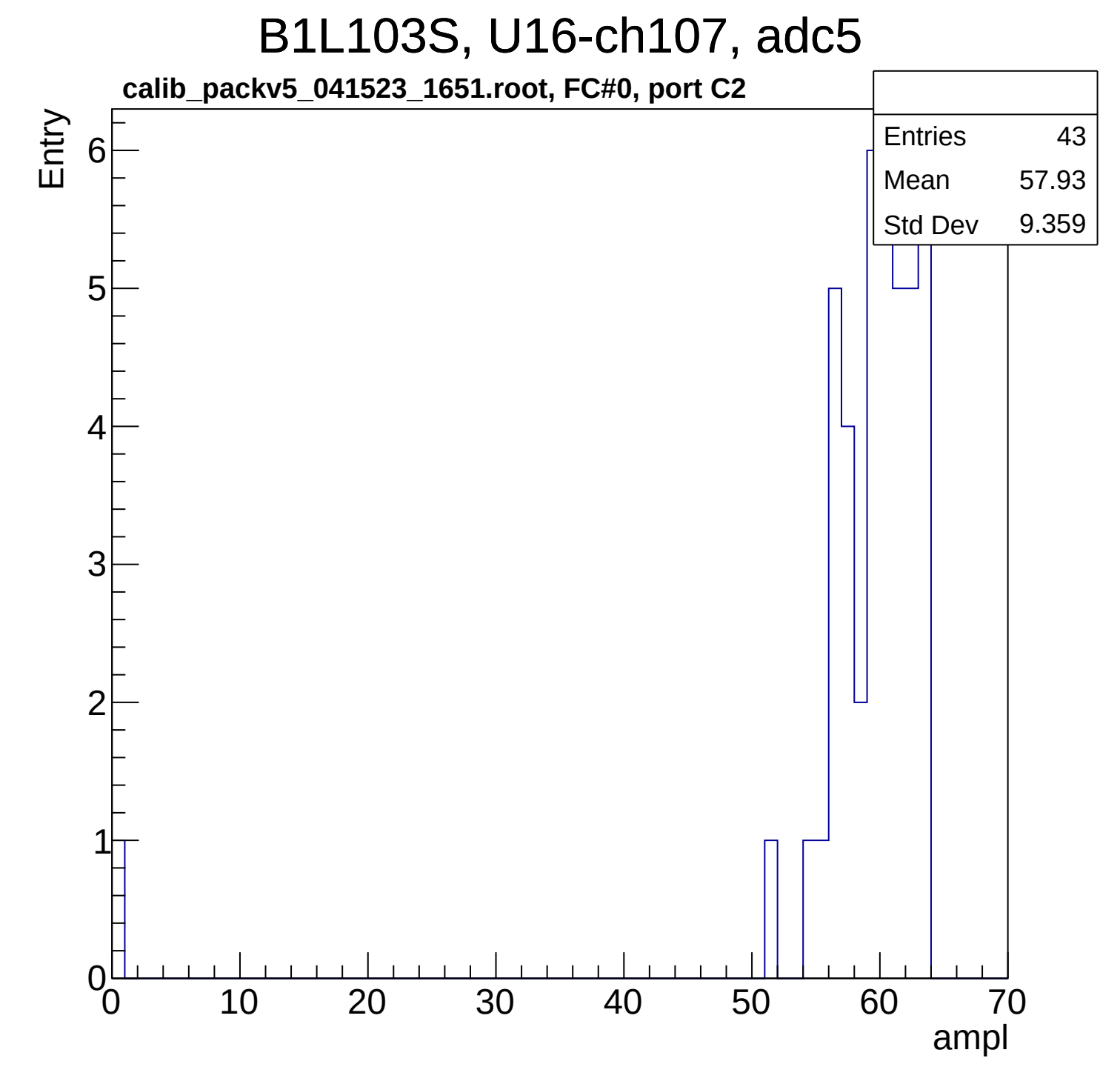
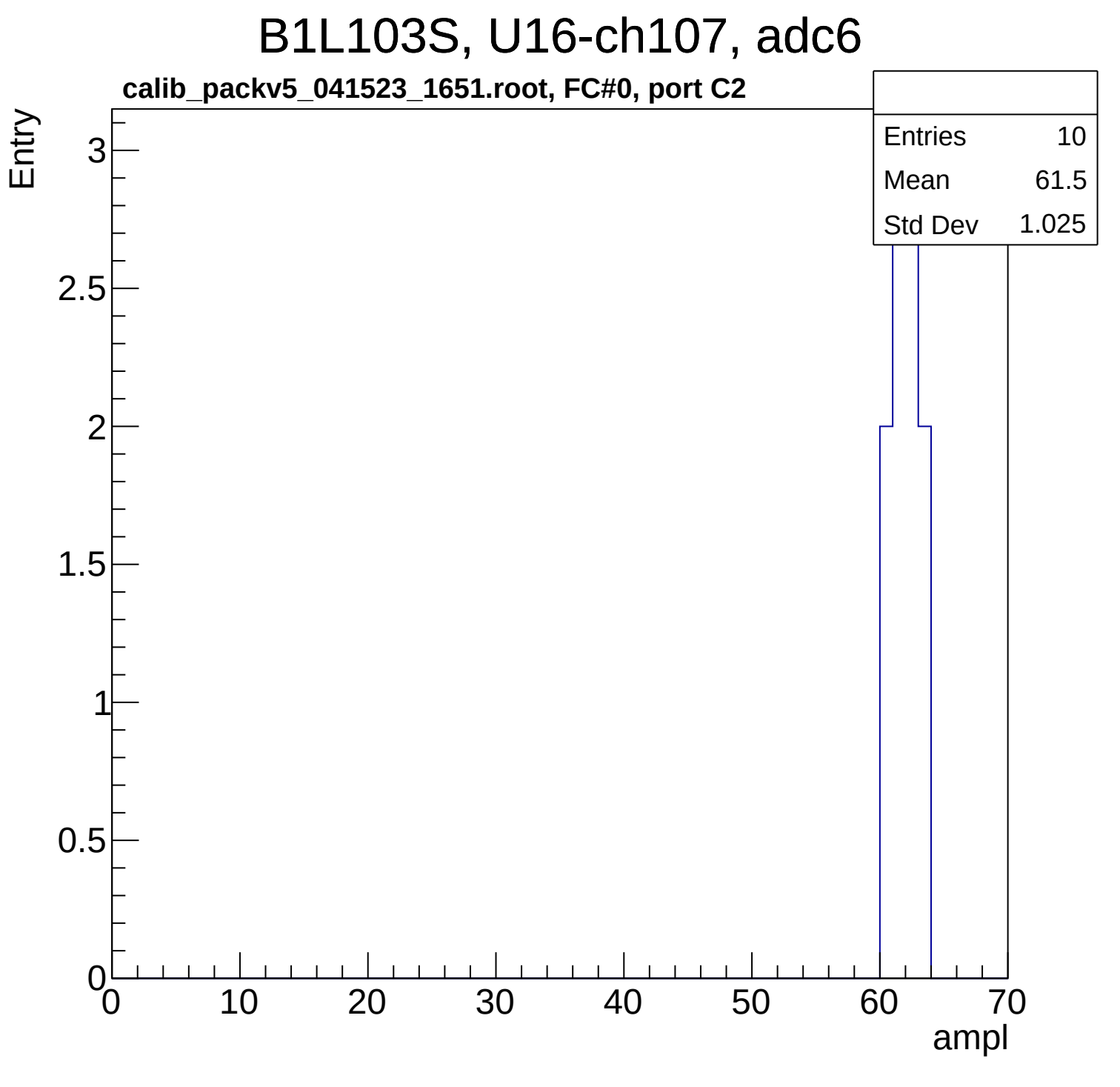
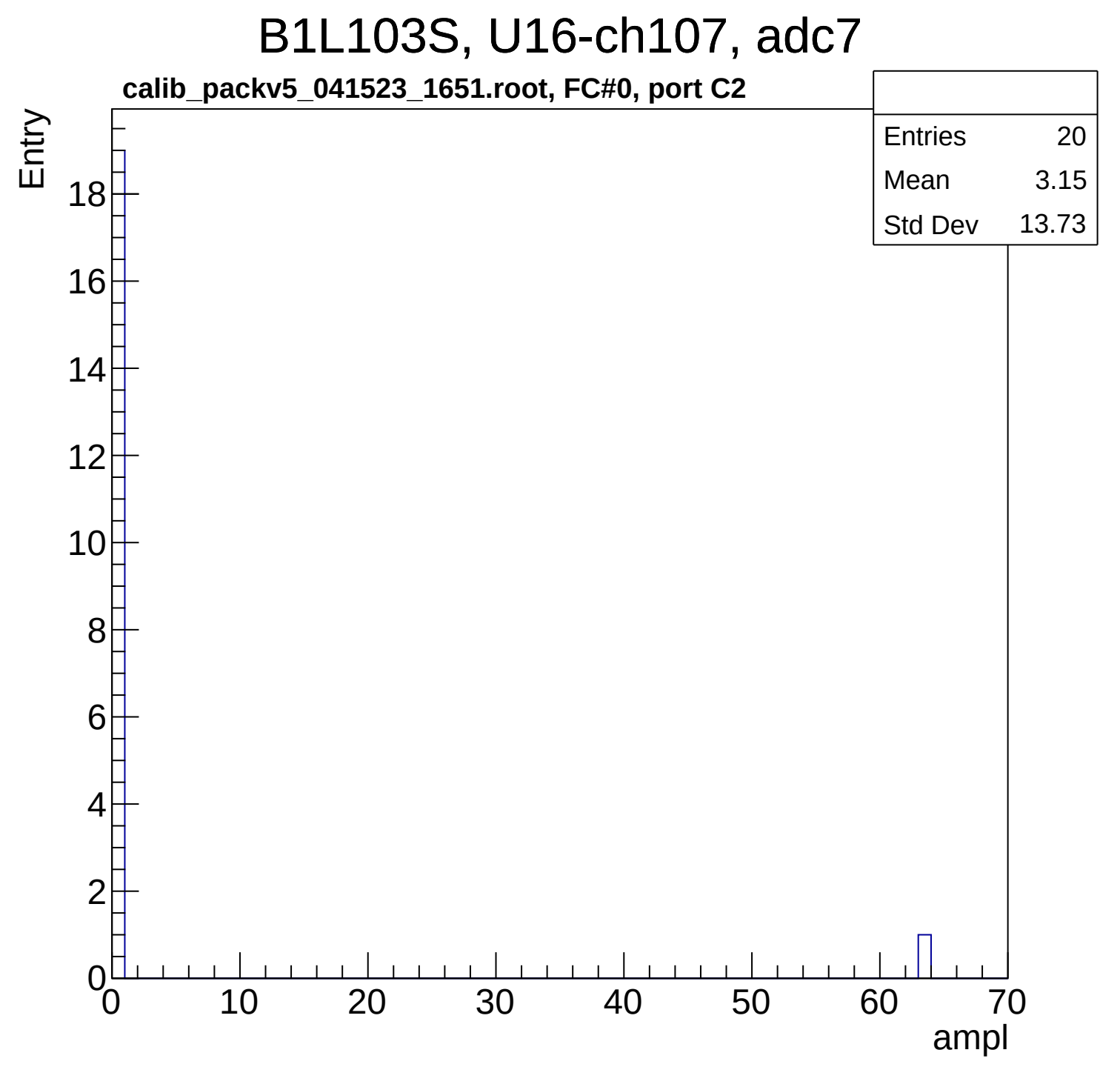
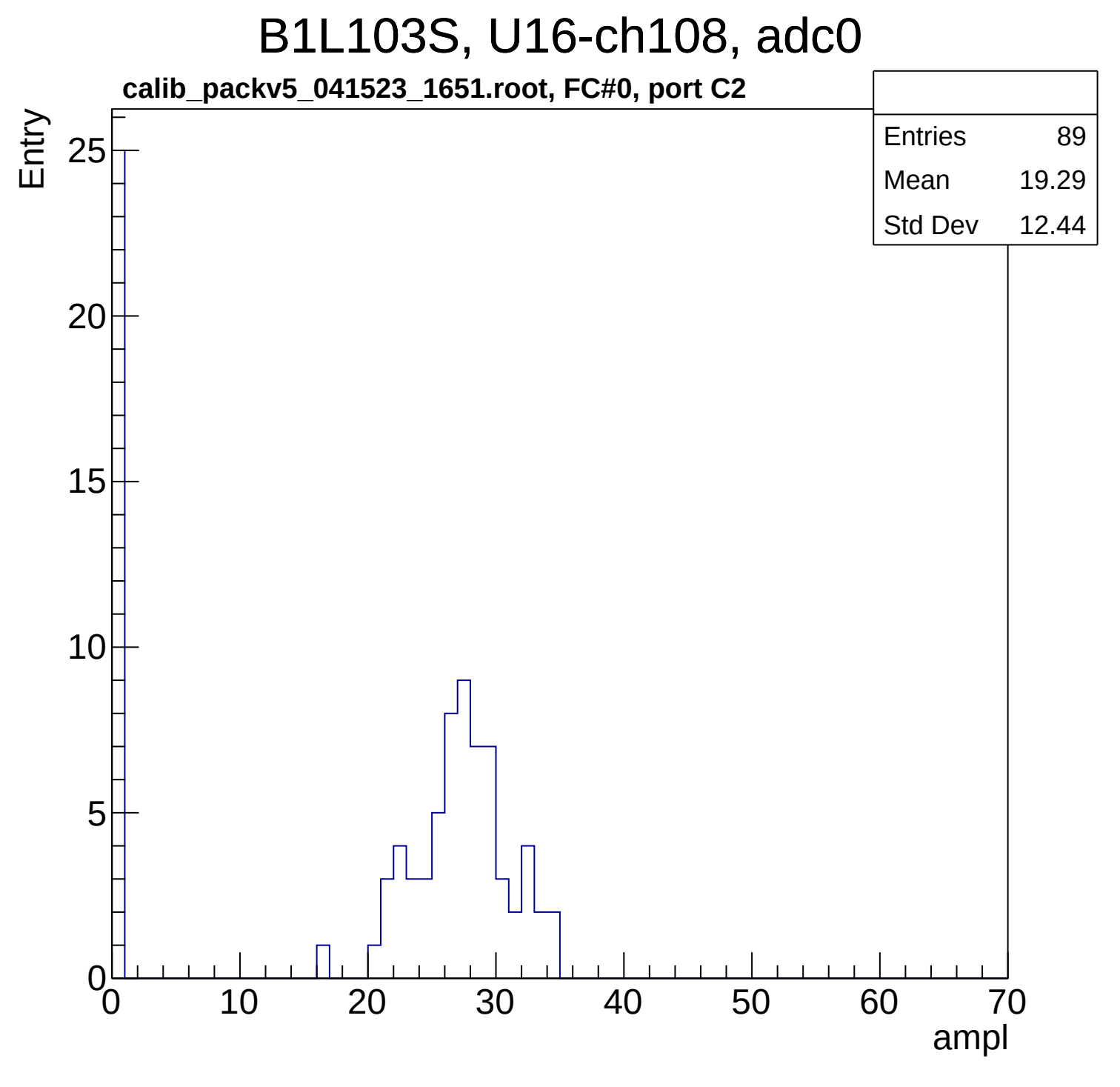
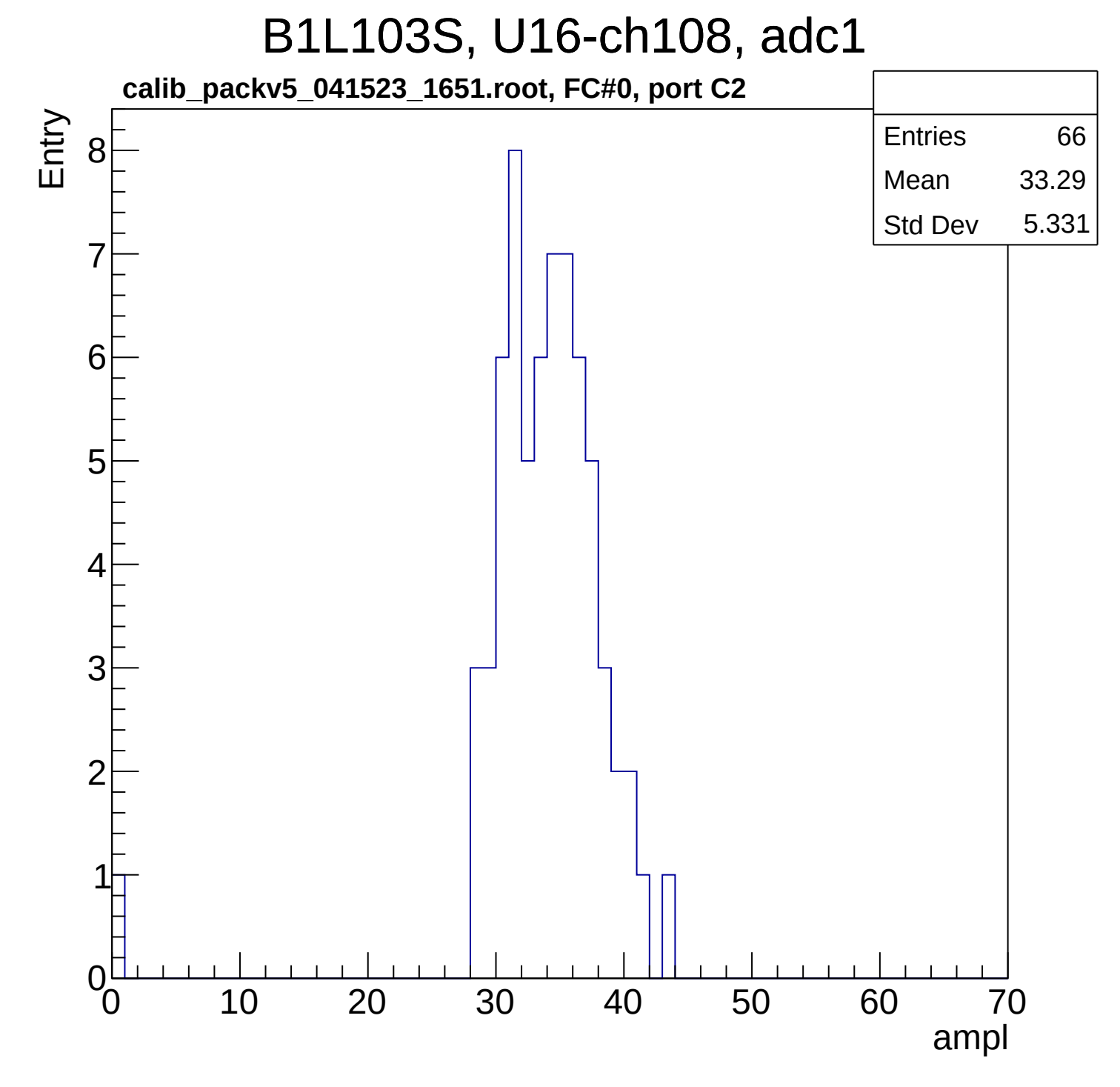

B1L103S, U16-ch107, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 57.93
Std Dev 9.359
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch107, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.5
Std Dev 1.025
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U16-ch107, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch108, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 19.29
Std Dev 12.44
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U16-ch108, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 33.29
Std Dev 5.331
Entry
ampl
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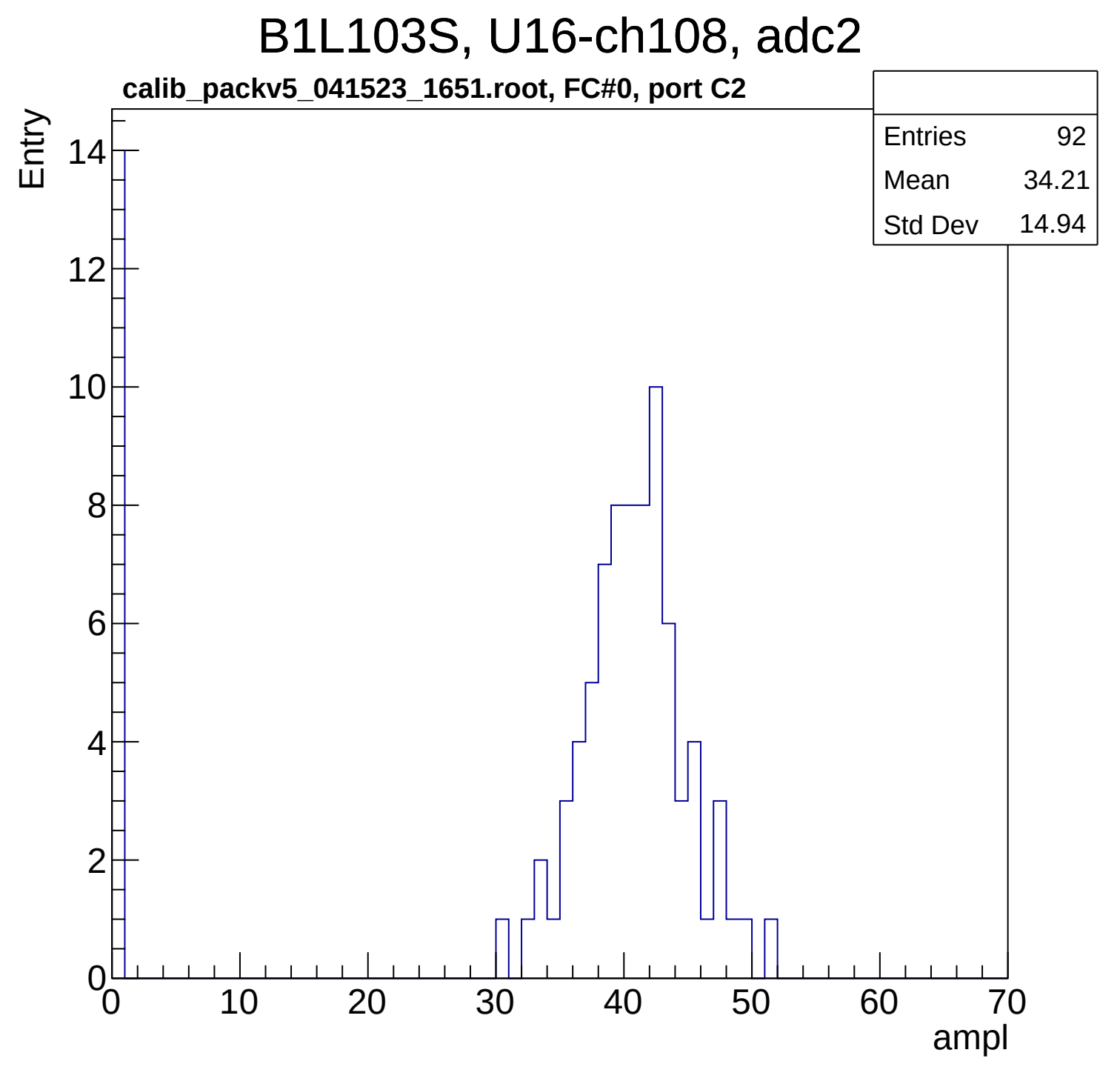
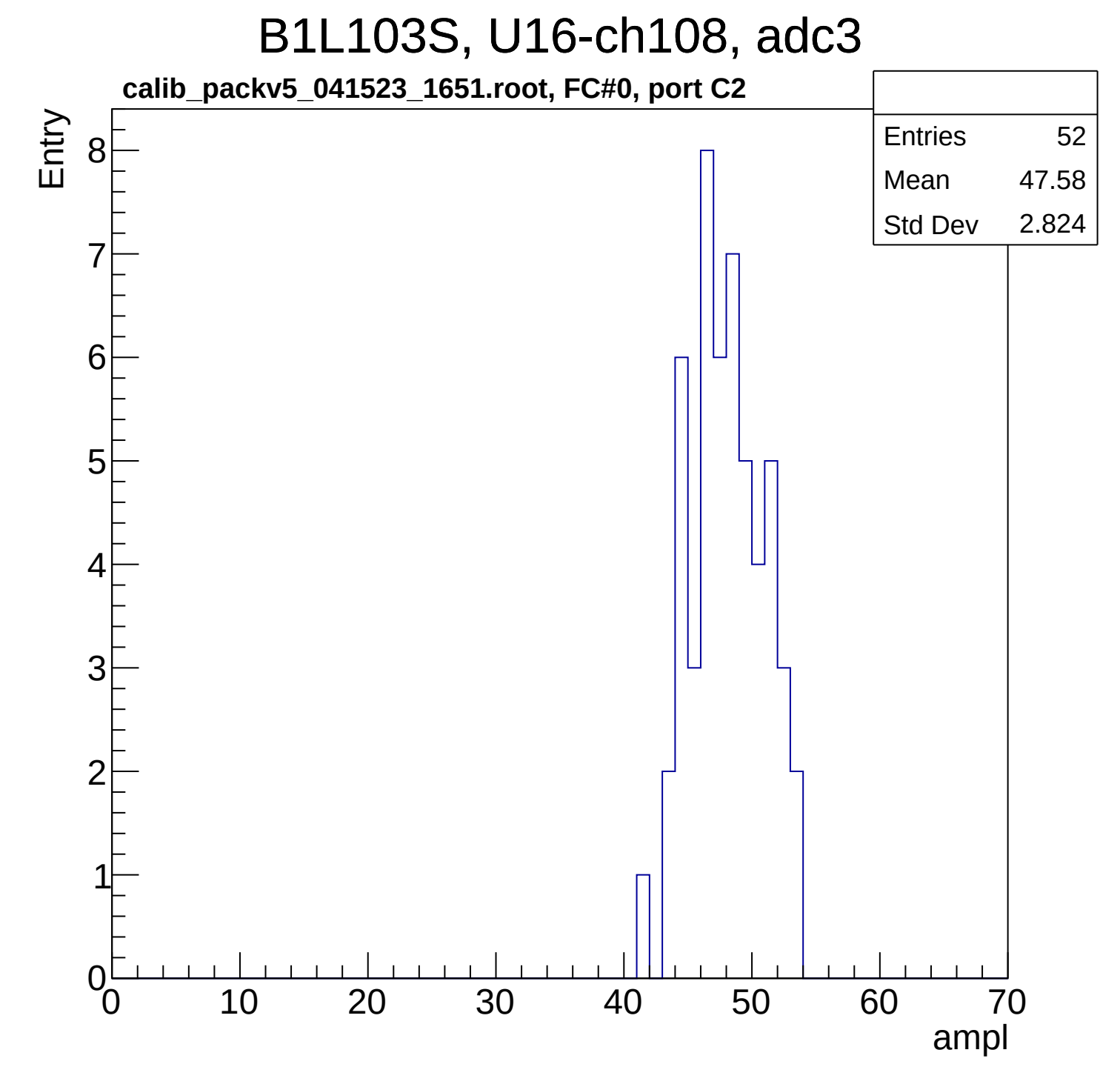
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch108, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 34.21
Std Dev 14.94
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U16-ch108, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 47.58
Std Dev 2.824
Entry
ampl
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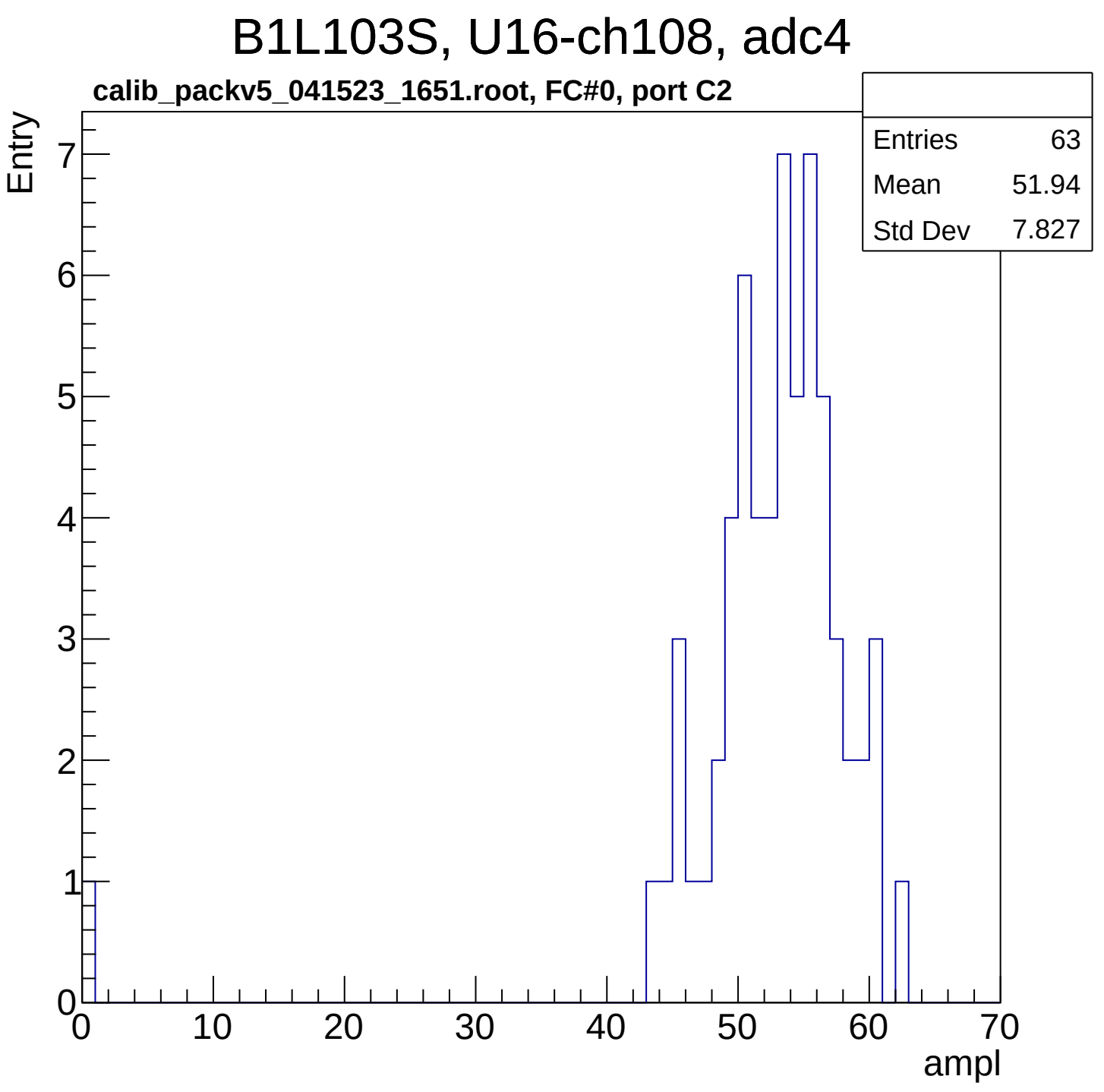
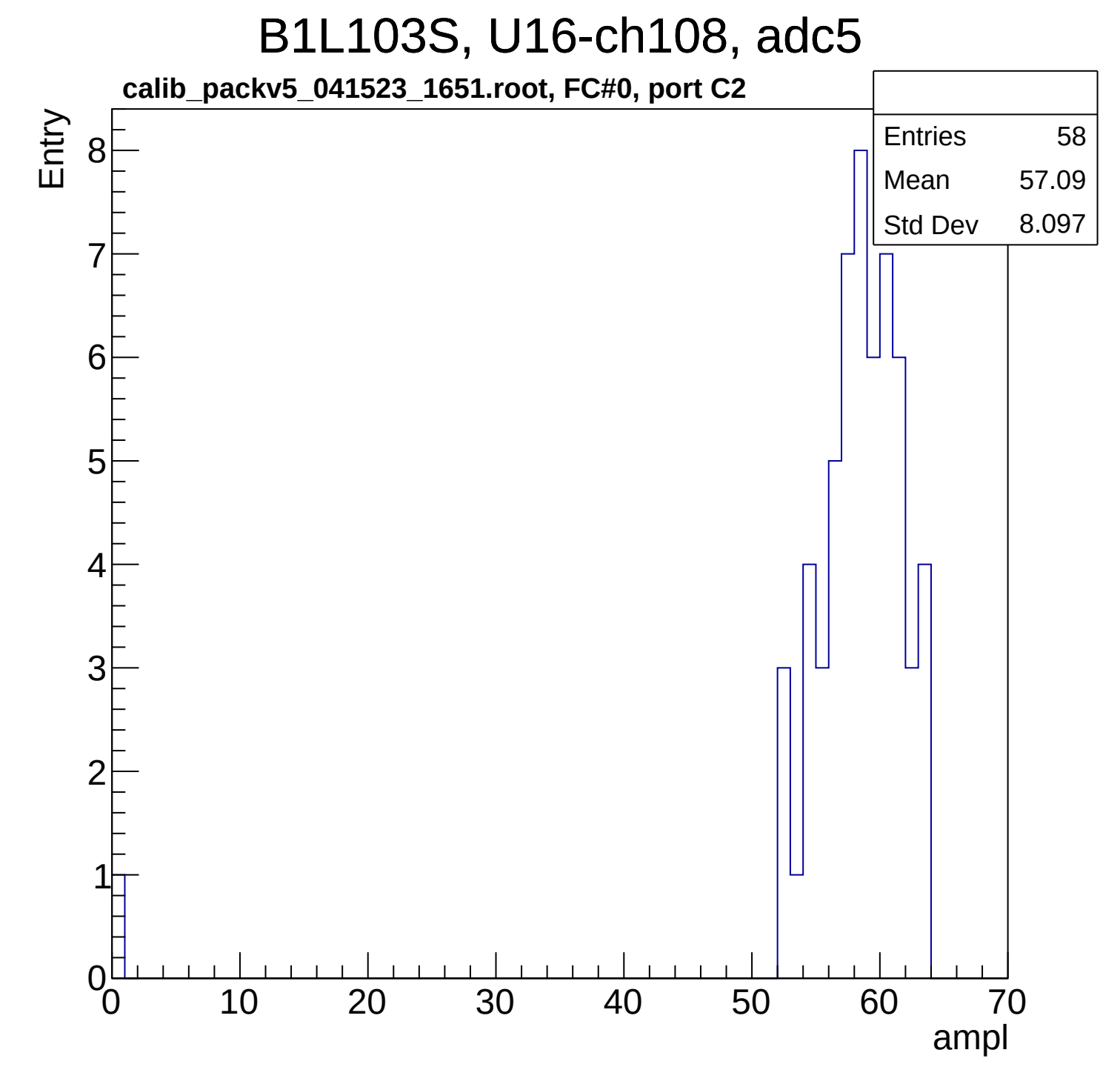
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch108, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 51.94
Std Dev 7.827
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch108, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 57.09
Std Dev 8.097
Entry
ampl
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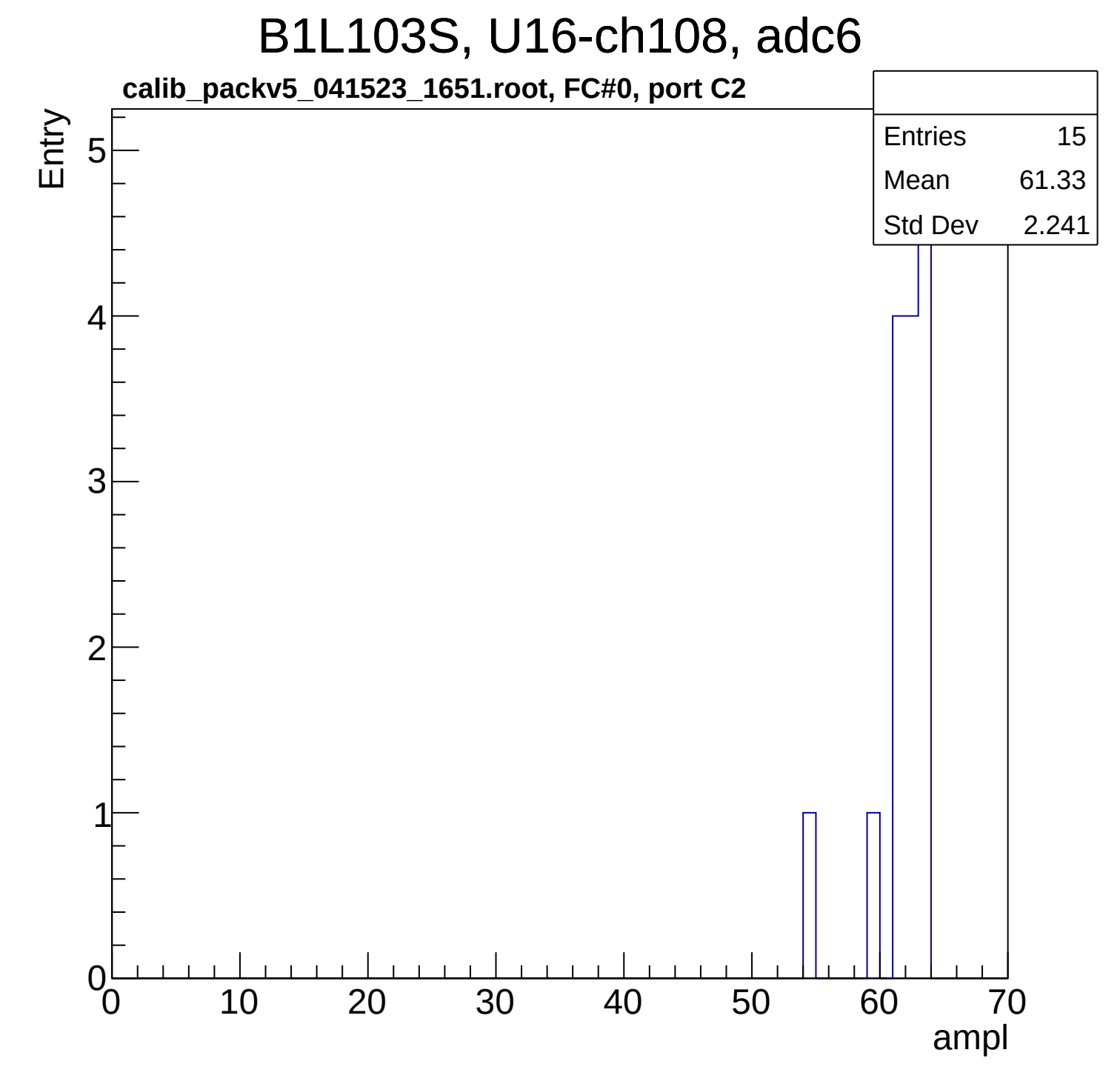
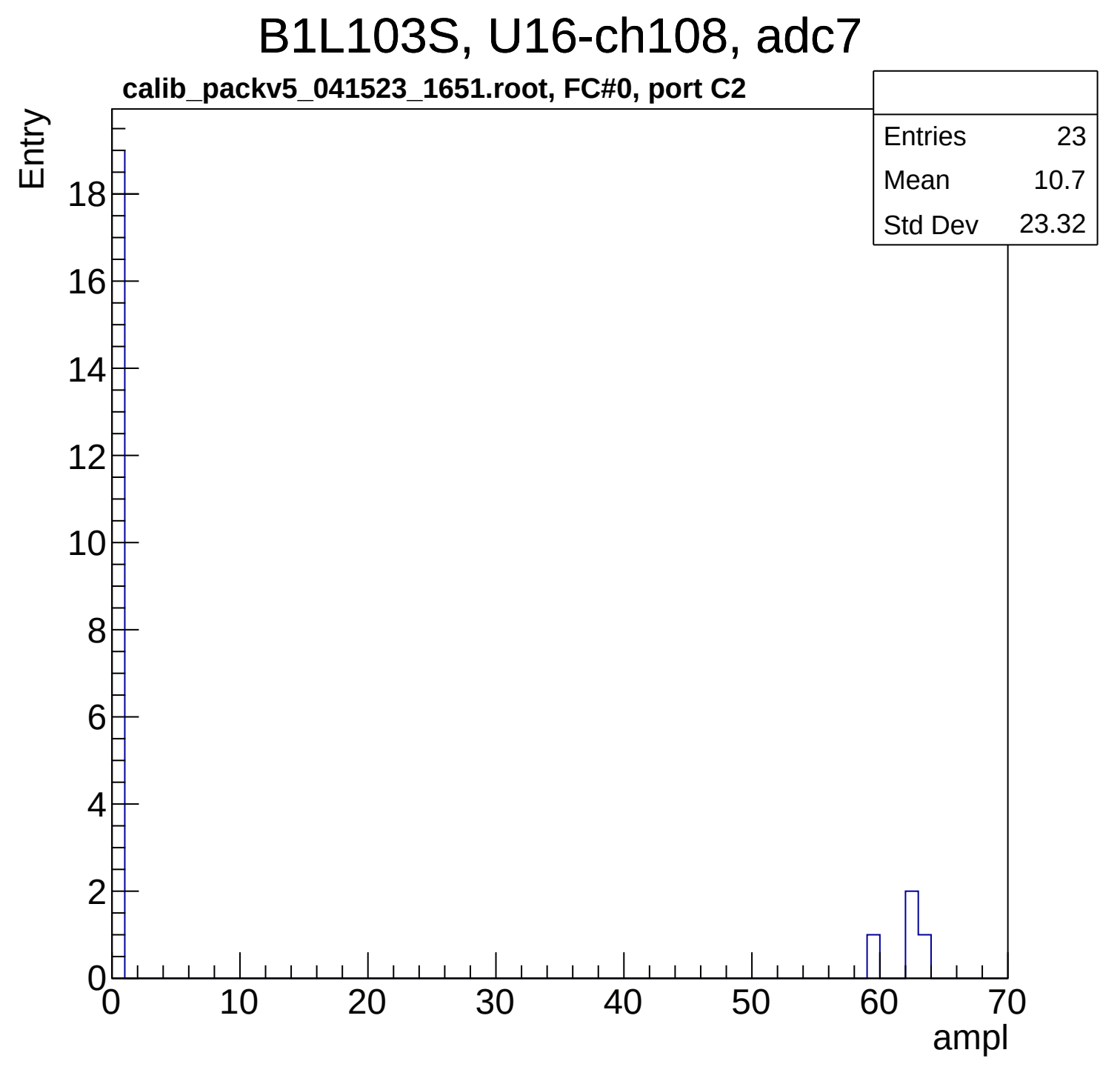
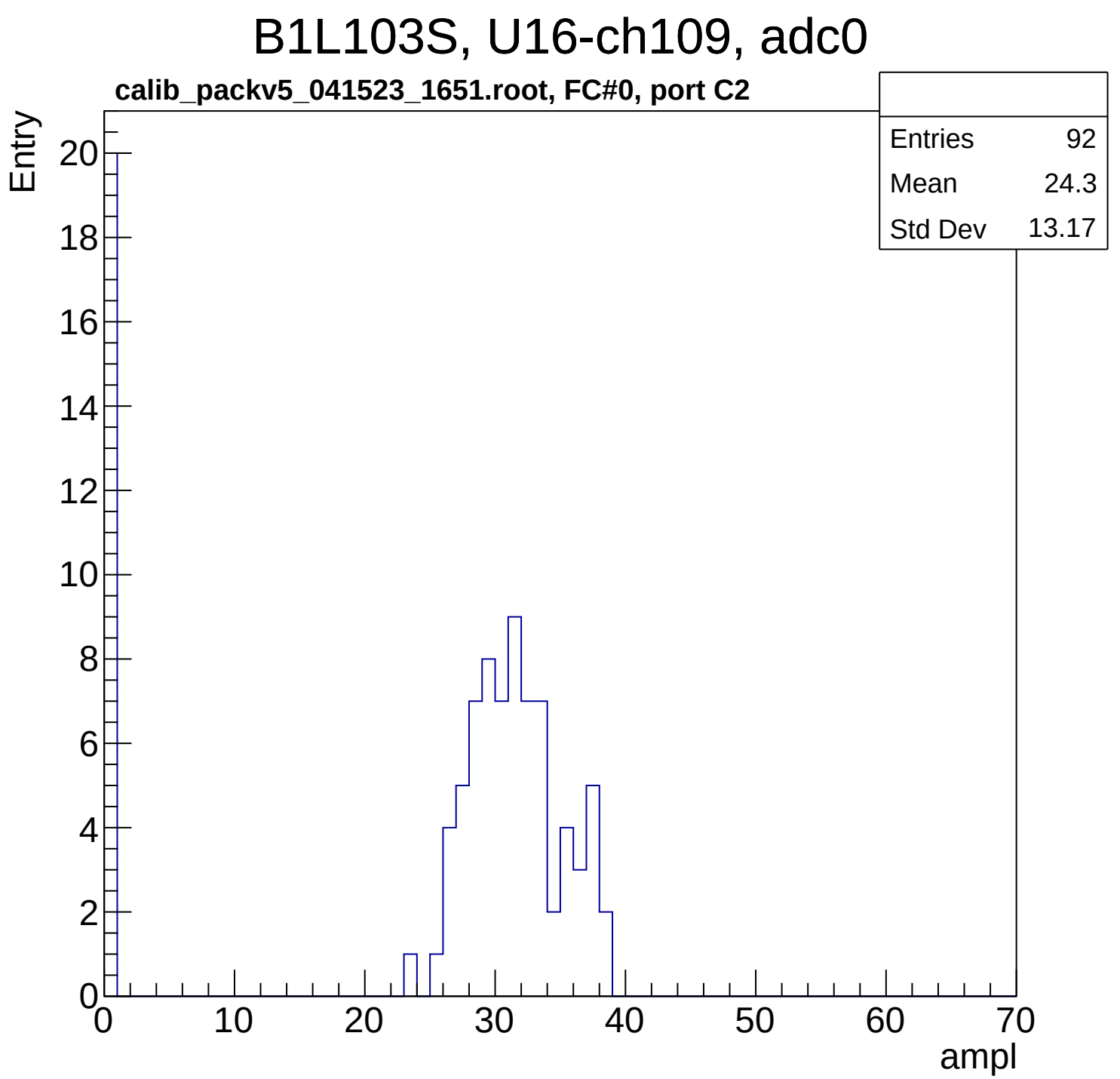
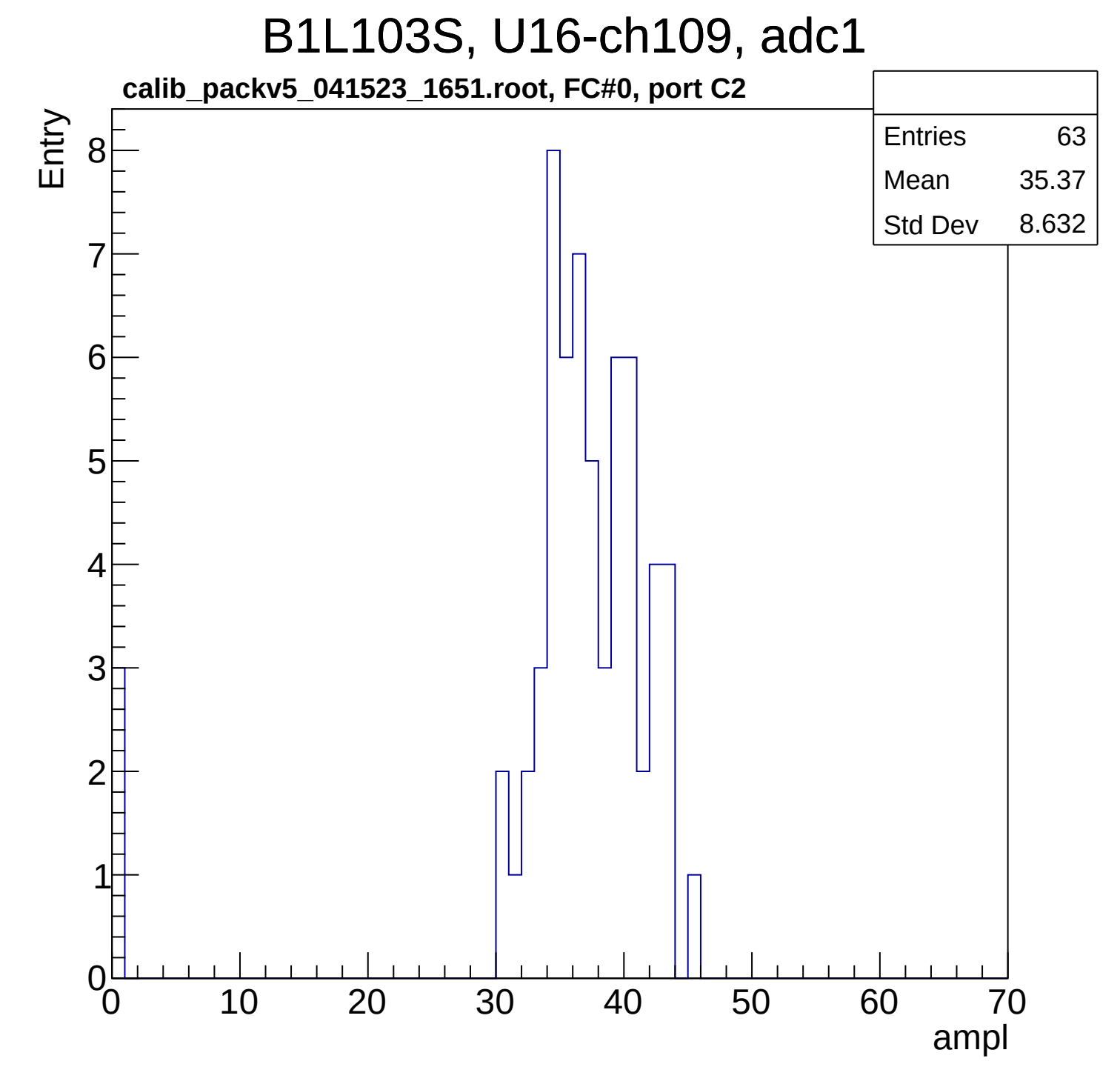
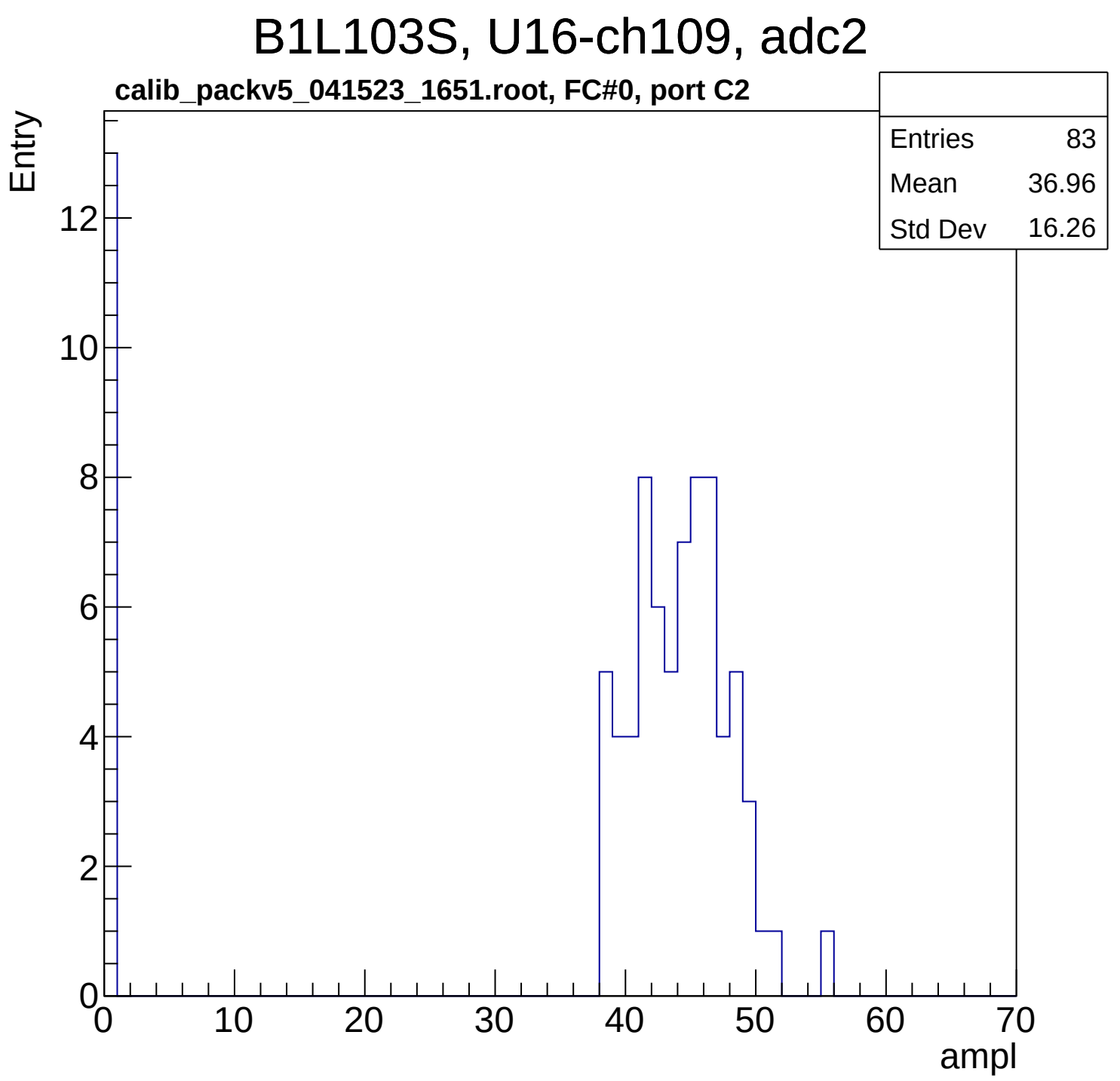
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

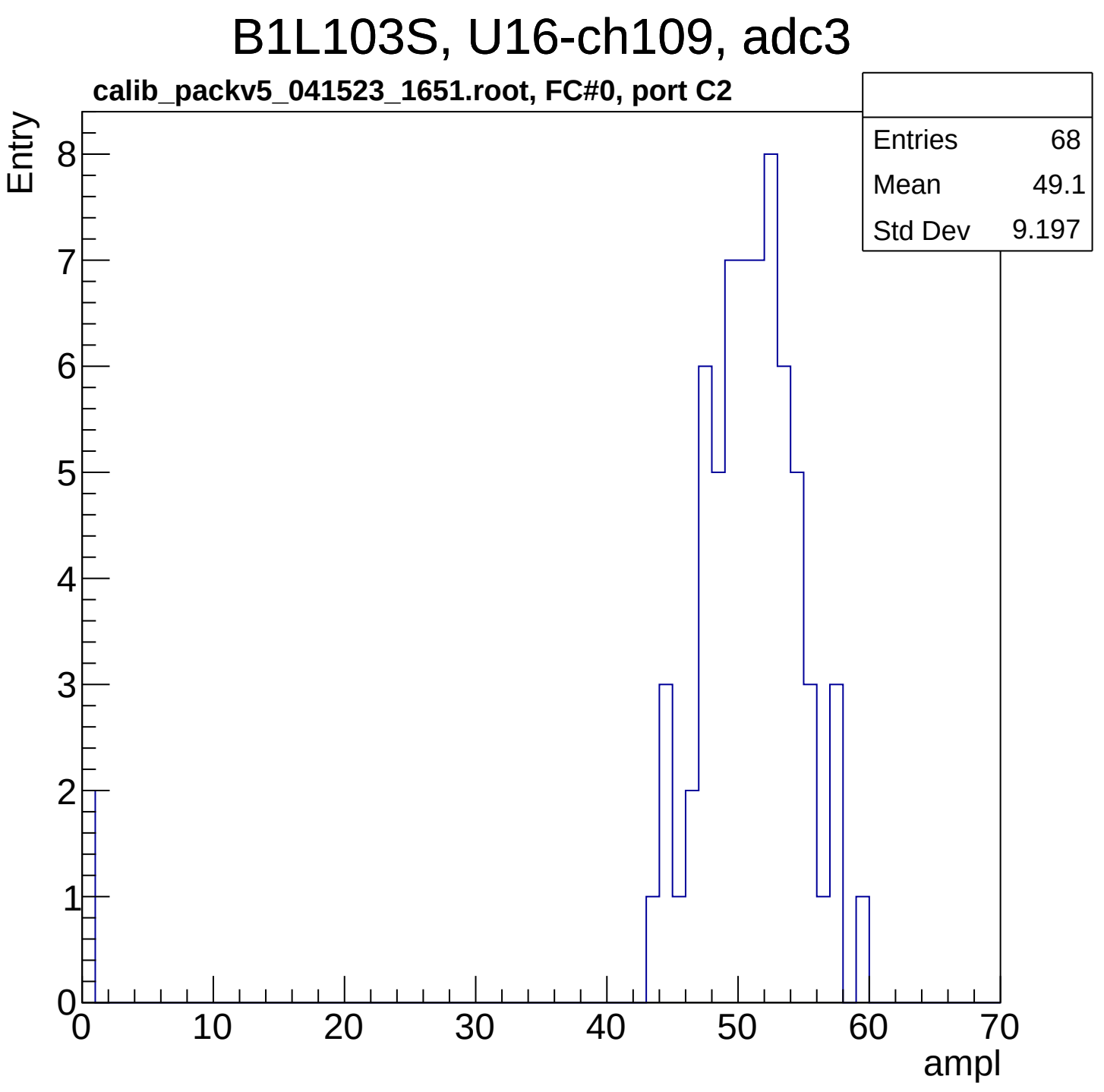

B1L103S, U16-ch108, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.33
Std Dev 2.241
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

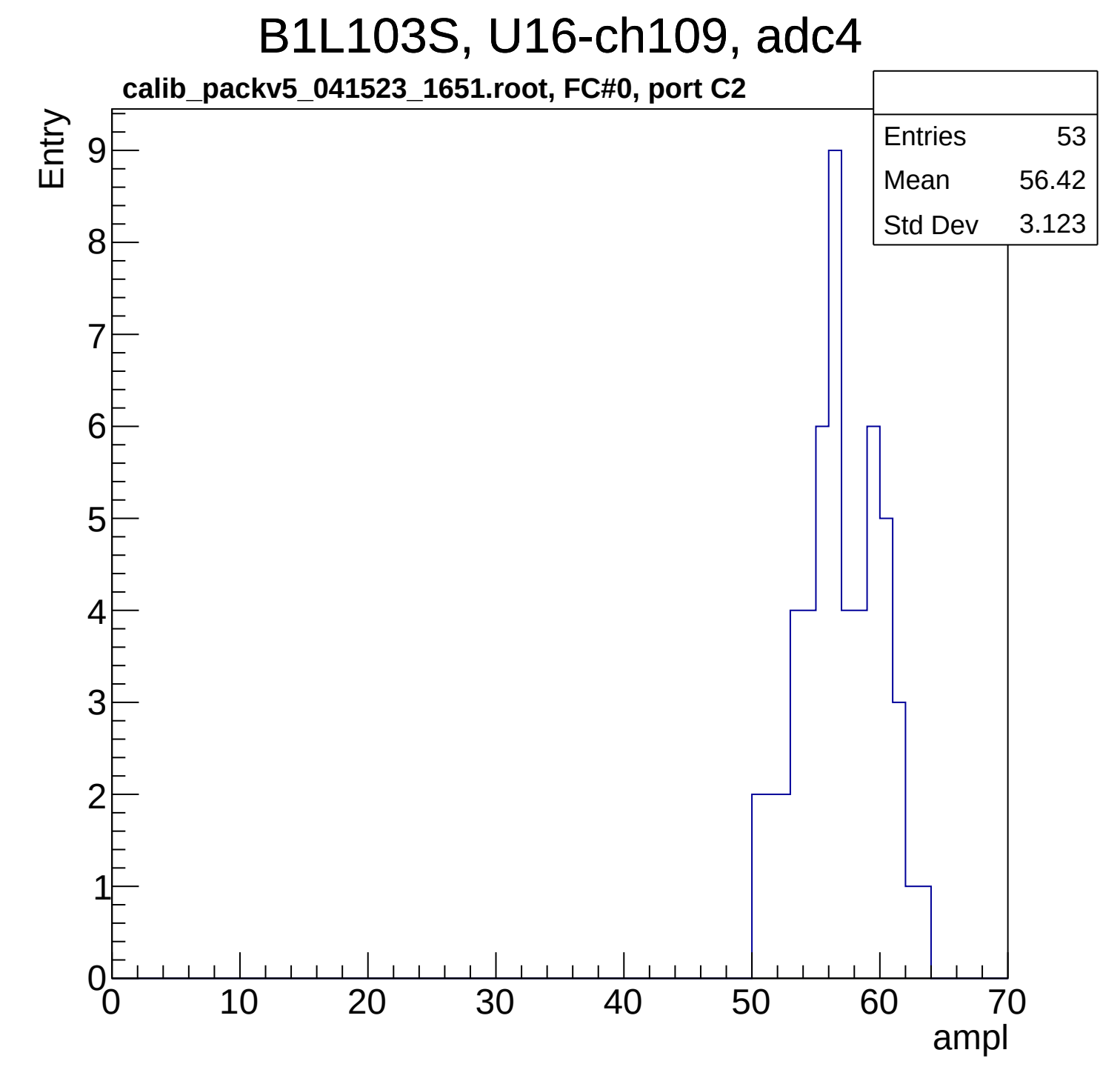

B1L103S, U16-ch108, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.7
Std Dev 23.32
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

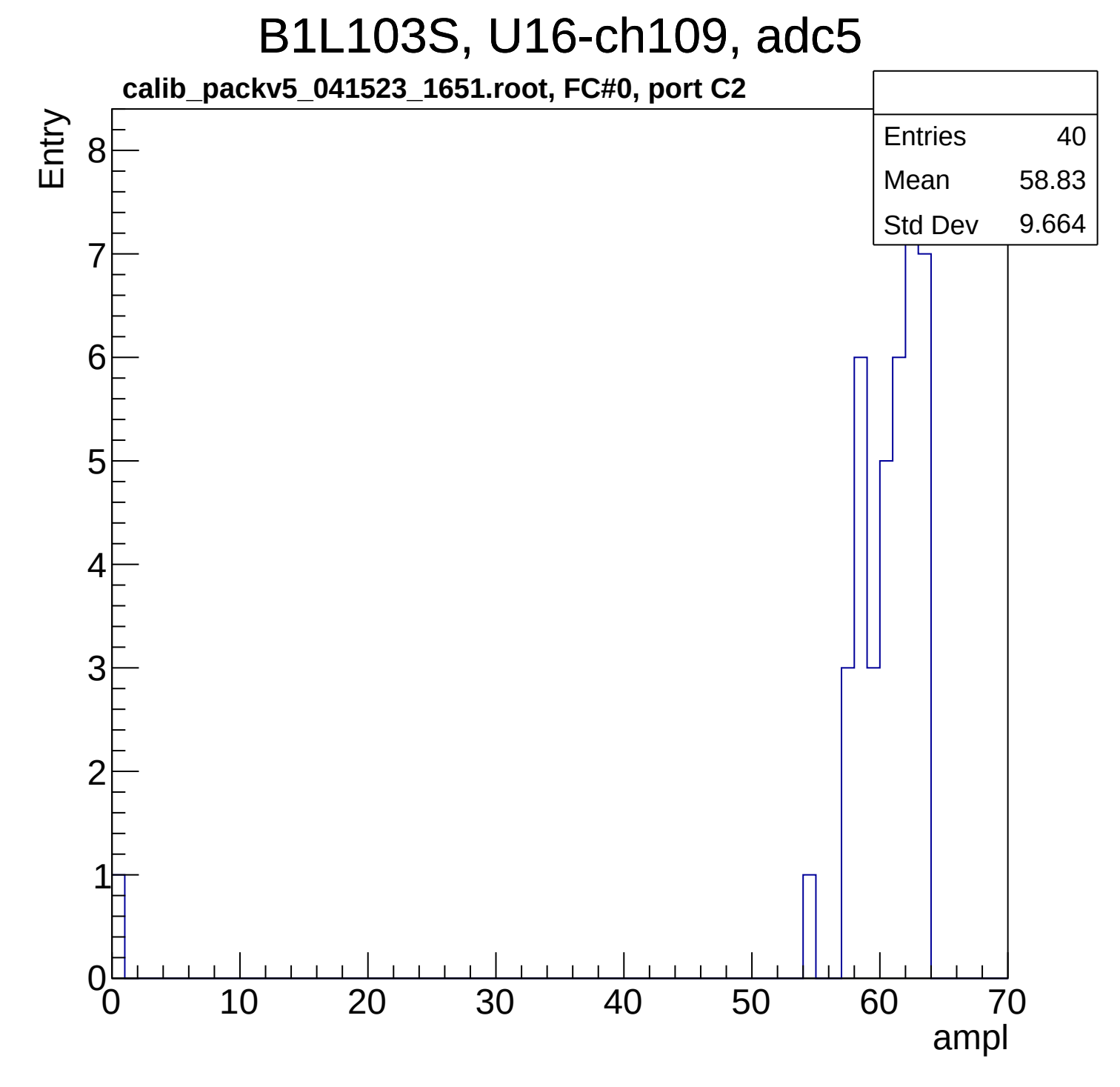

B1L103S, U16-ch109, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 24.3
Std Dev 13.17
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70


B1L103S, U16-ch109, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 35.37
Std Dev 8.632
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch109, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 36.96
Std Dev 16.26
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch109, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 49.1
Std Dev 9.197
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch109, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 56.42
Std Dev 3.123
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch109, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 58.83
Std Dev 9.664
Entry
ampl
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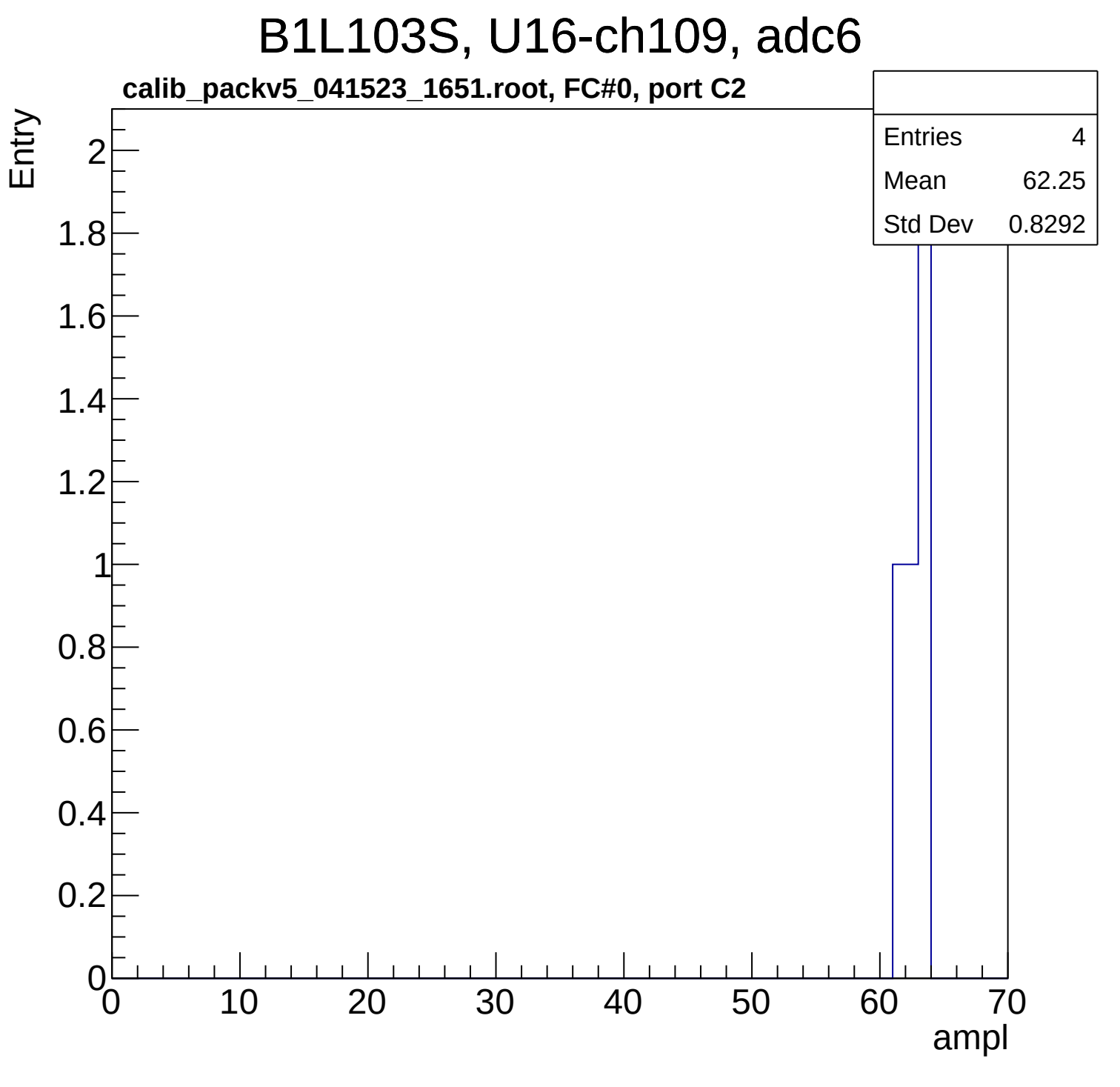
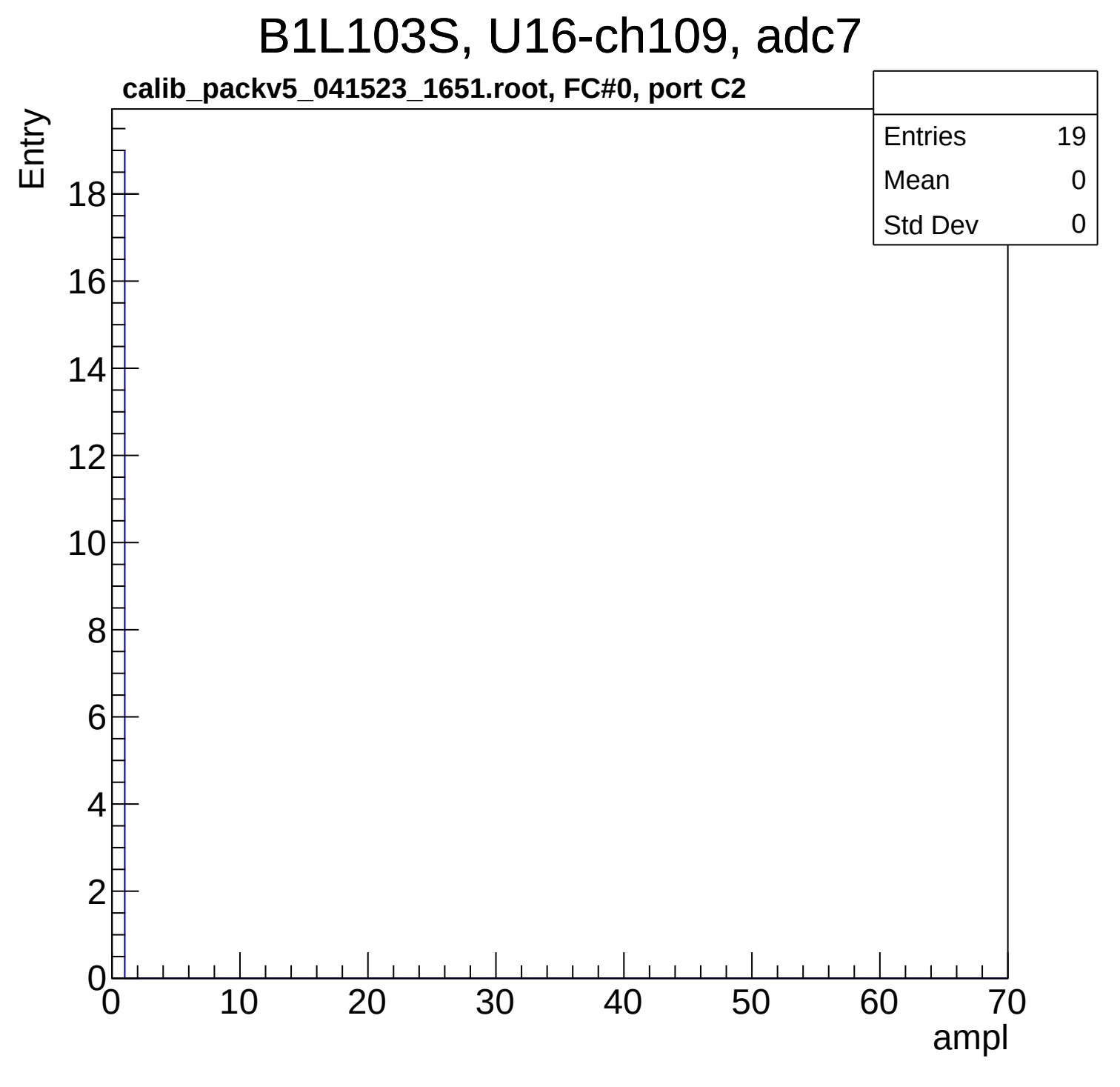
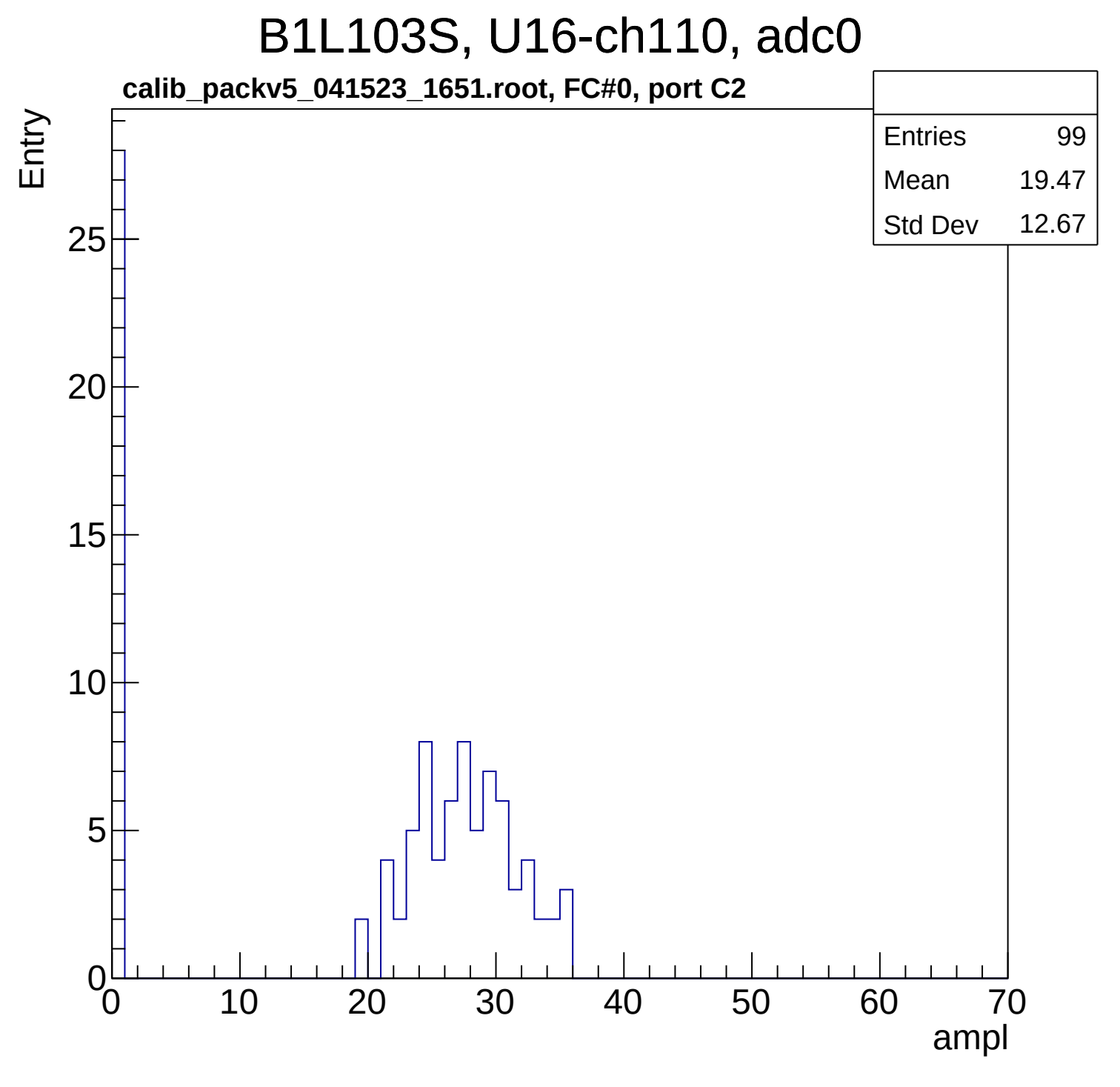
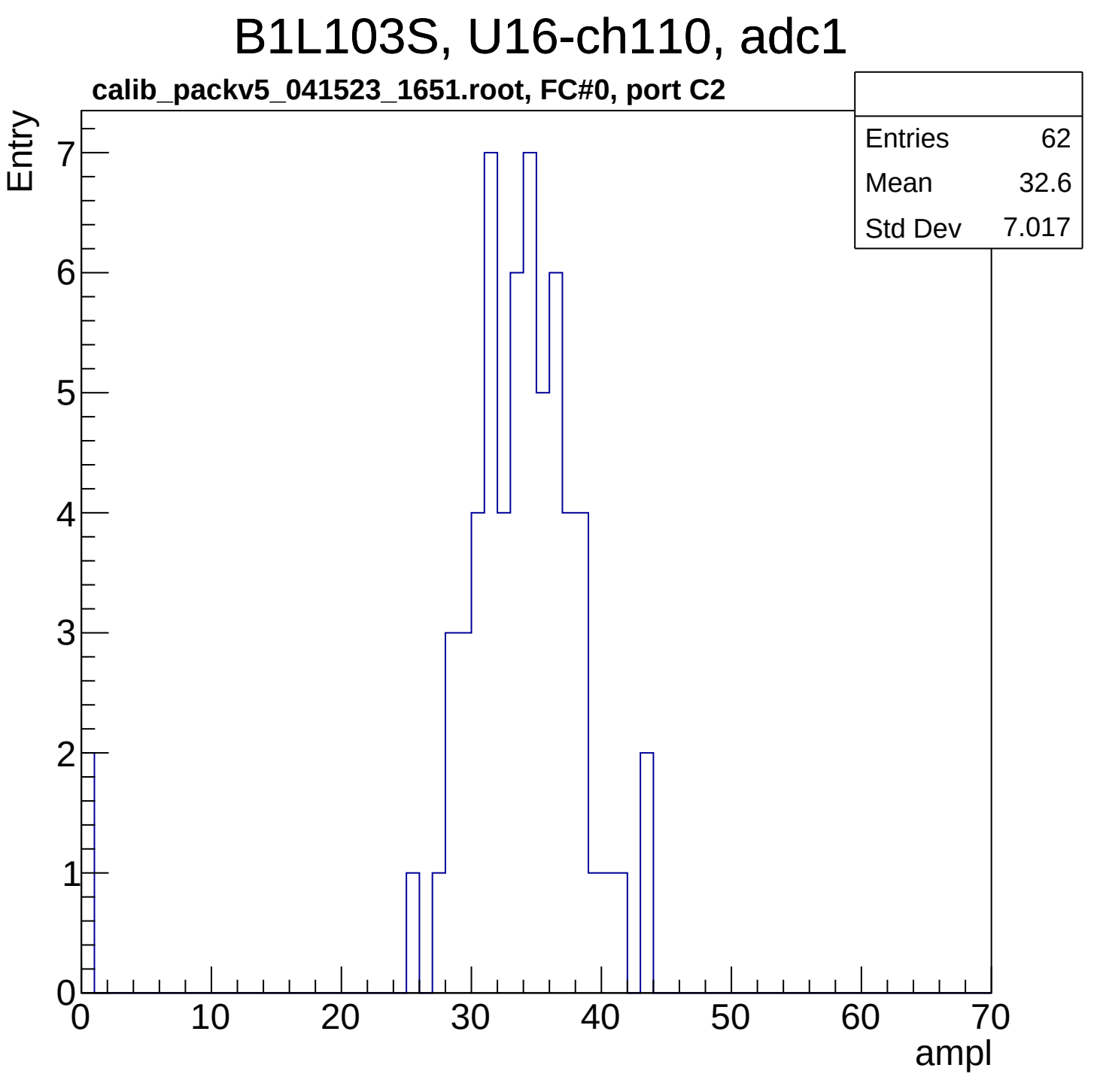
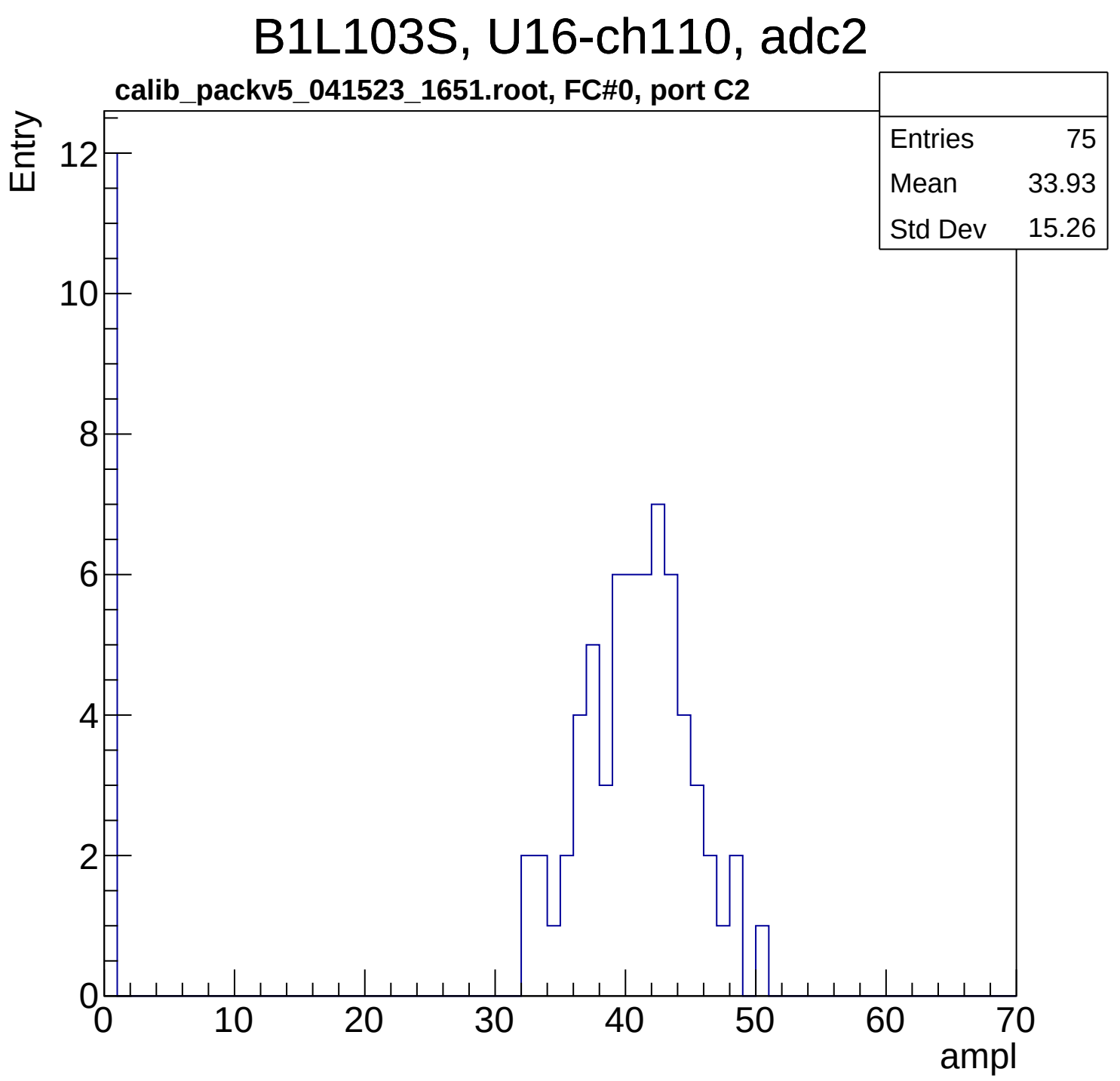
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

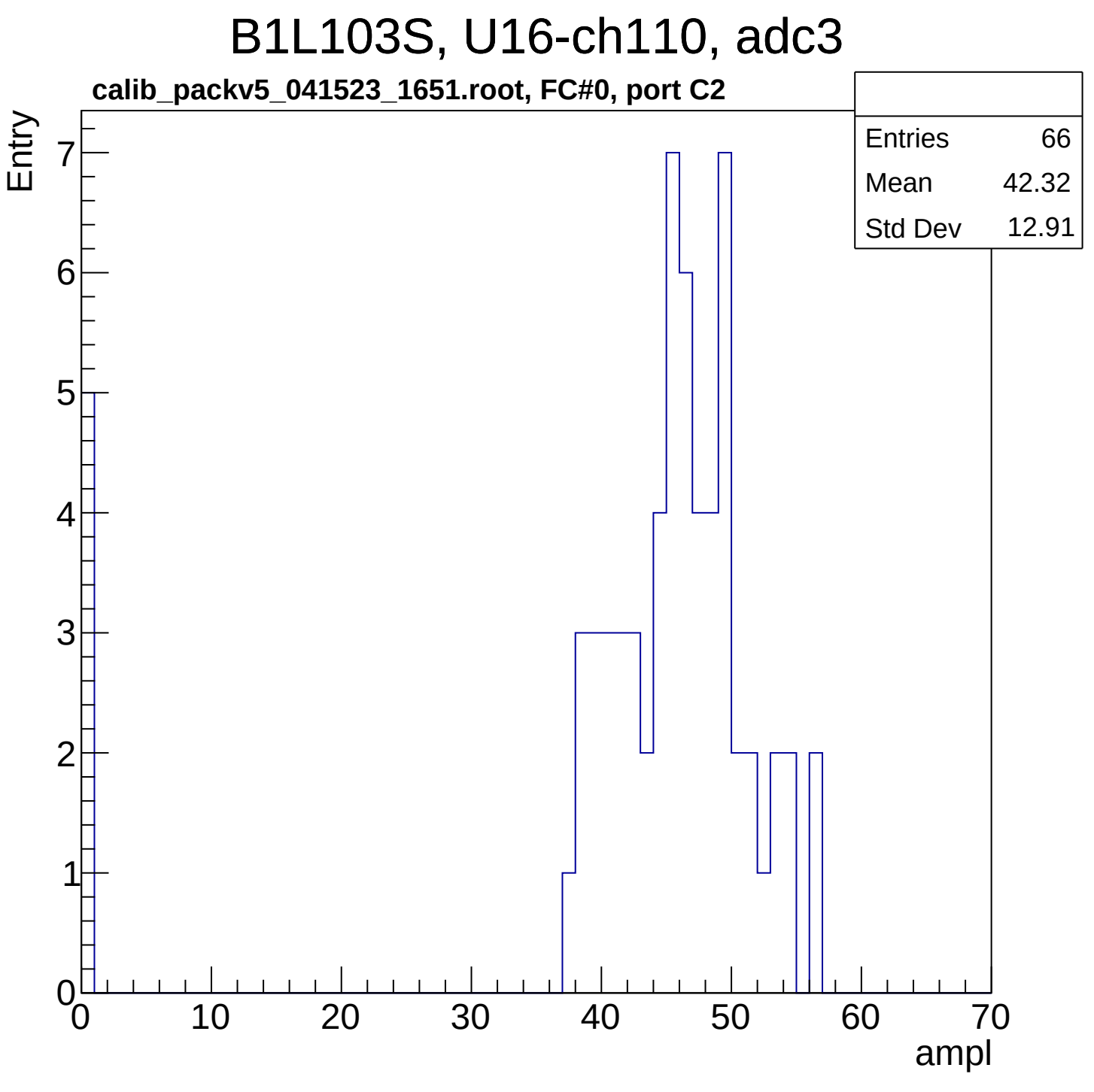

B1L103S, U16-ch109, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

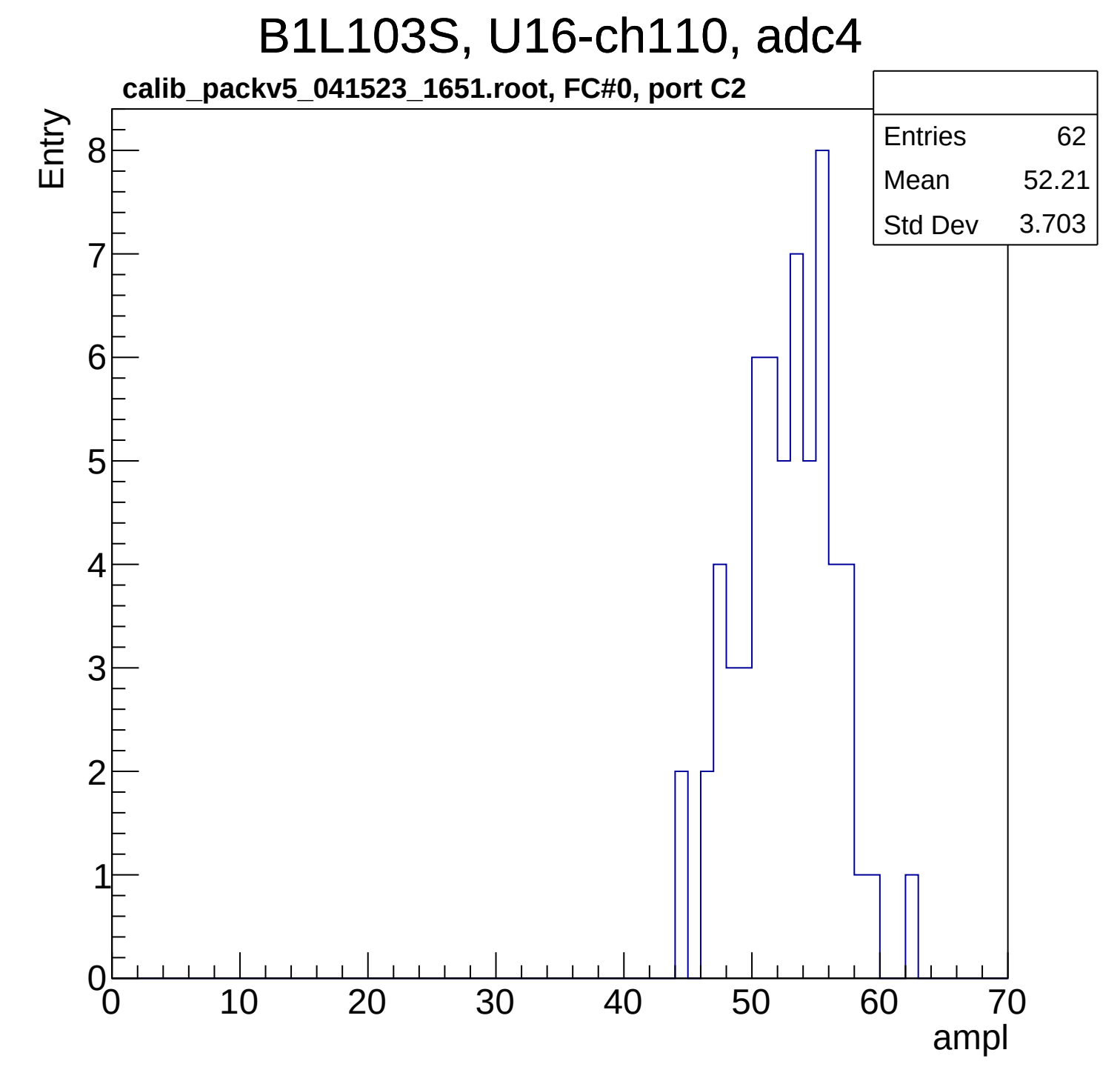

B1L103S, U16-ch109, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

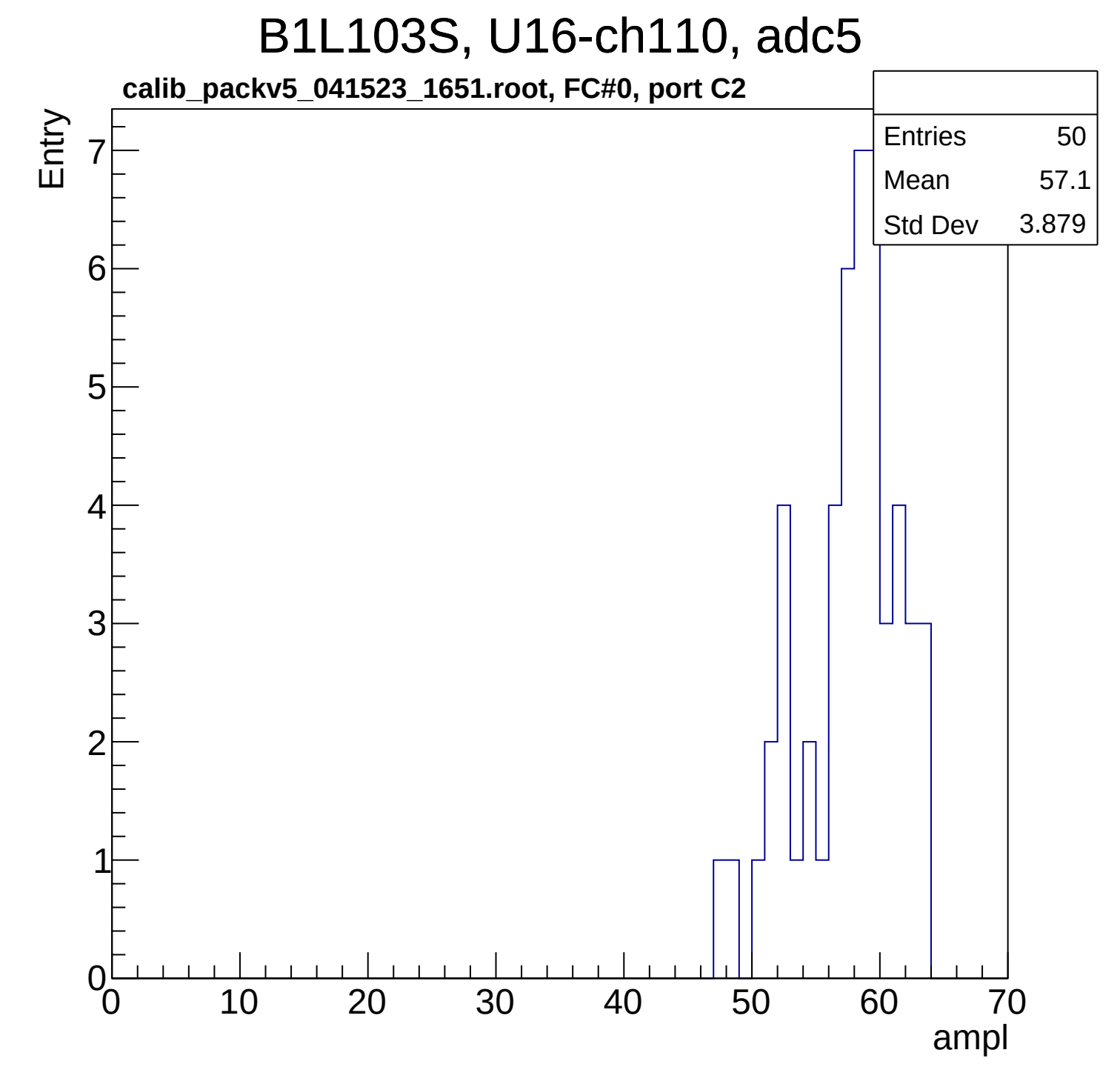

B1L103S, U16-ch110, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 19.47
Std Dev 12.67
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl

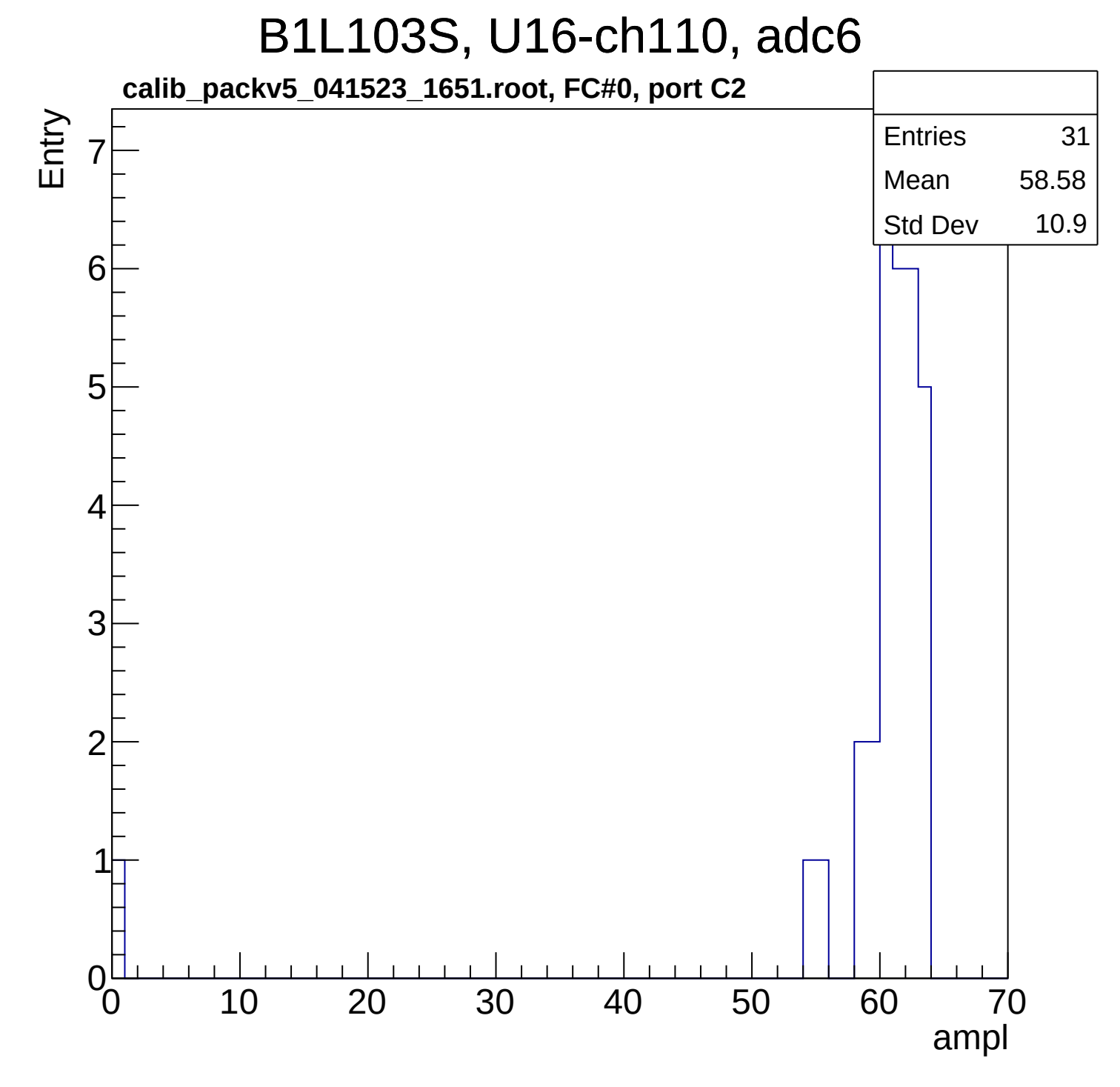

B1L103S, U16-ch110, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 32.6
Std Dev 7.017
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

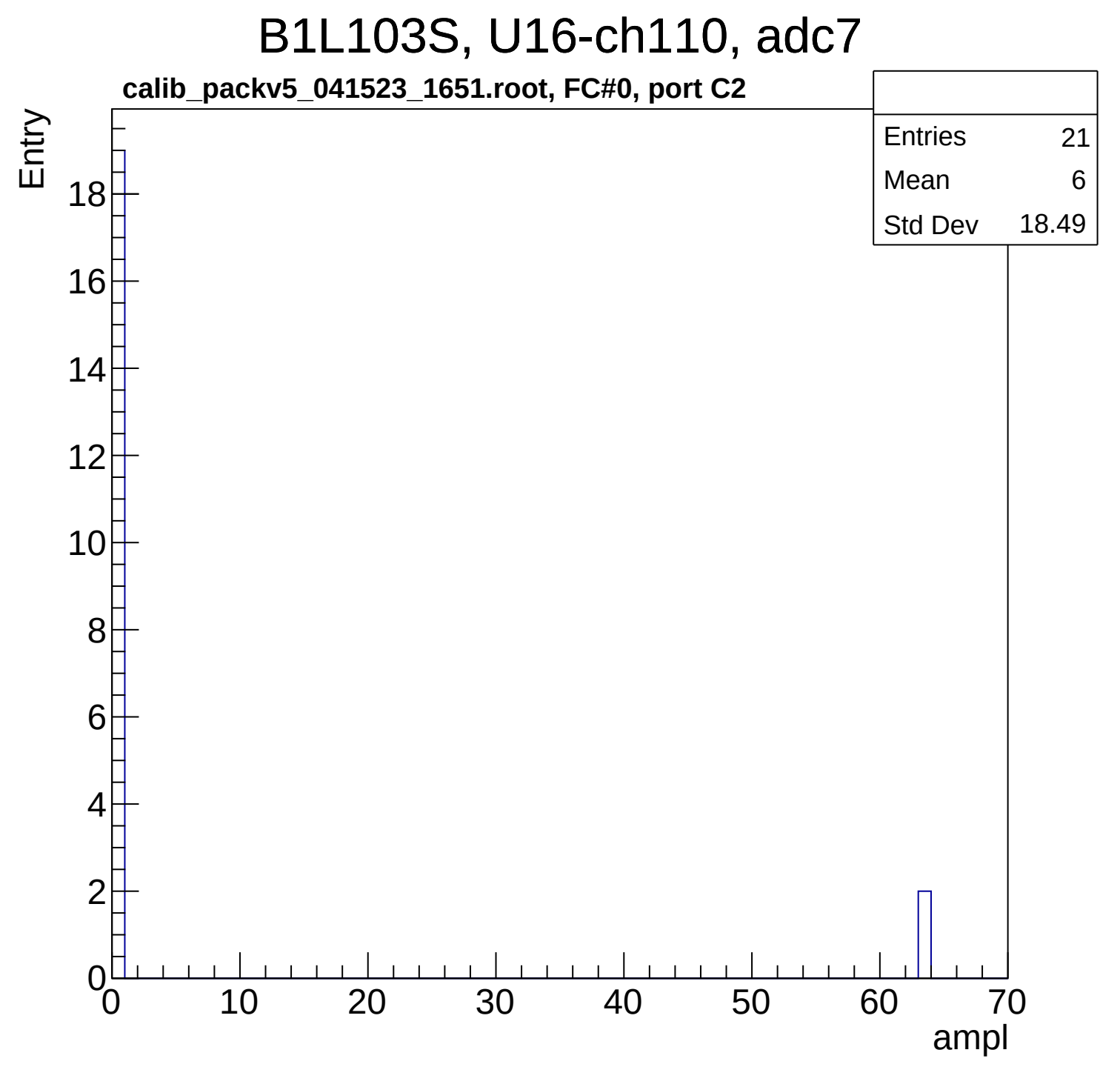

B1L103S, U16-ch110, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 33.93
Std Dev 15.26
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

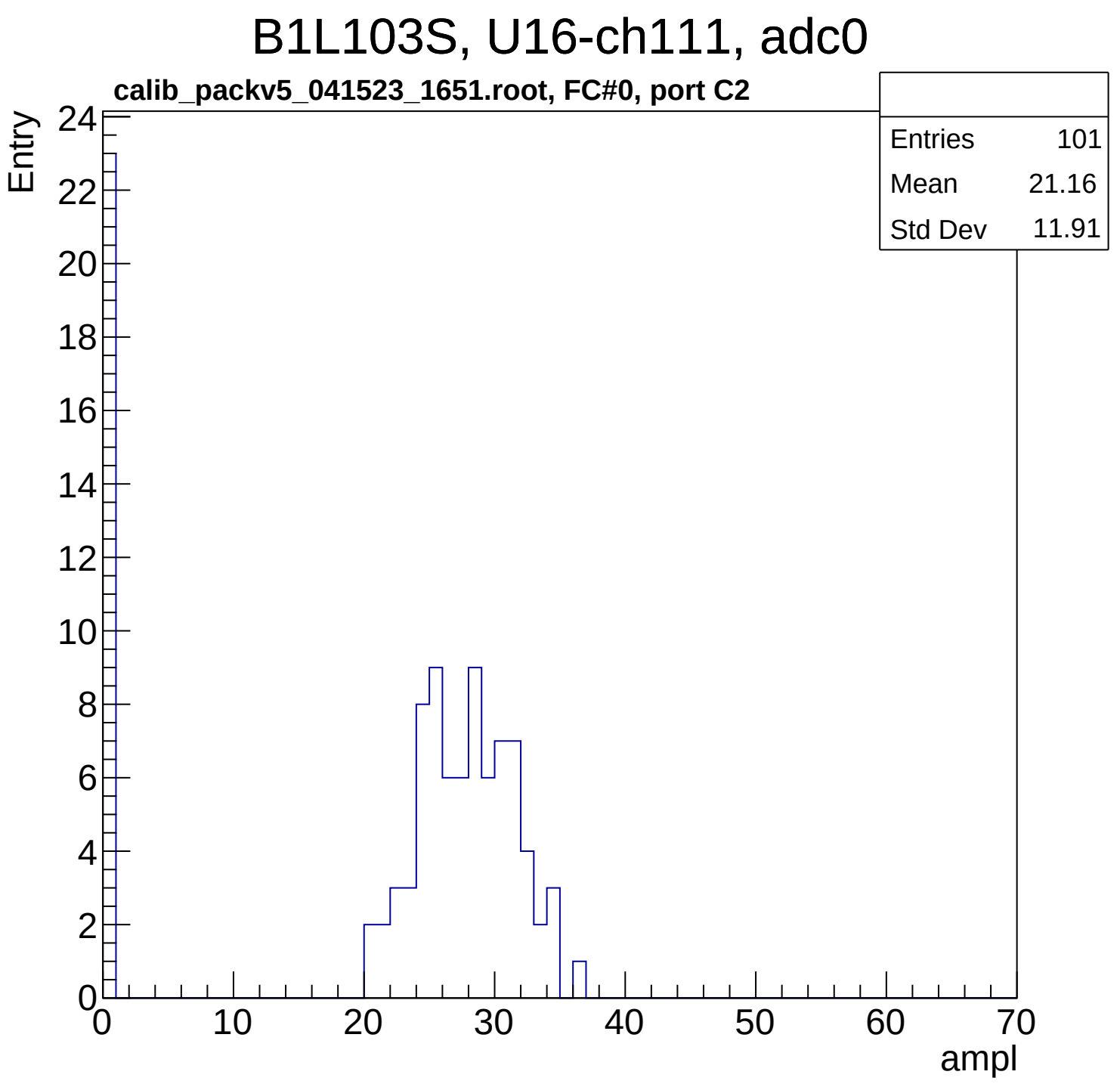

B1L103S, U16-ch110, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 42.32
Std Dev 12.91
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

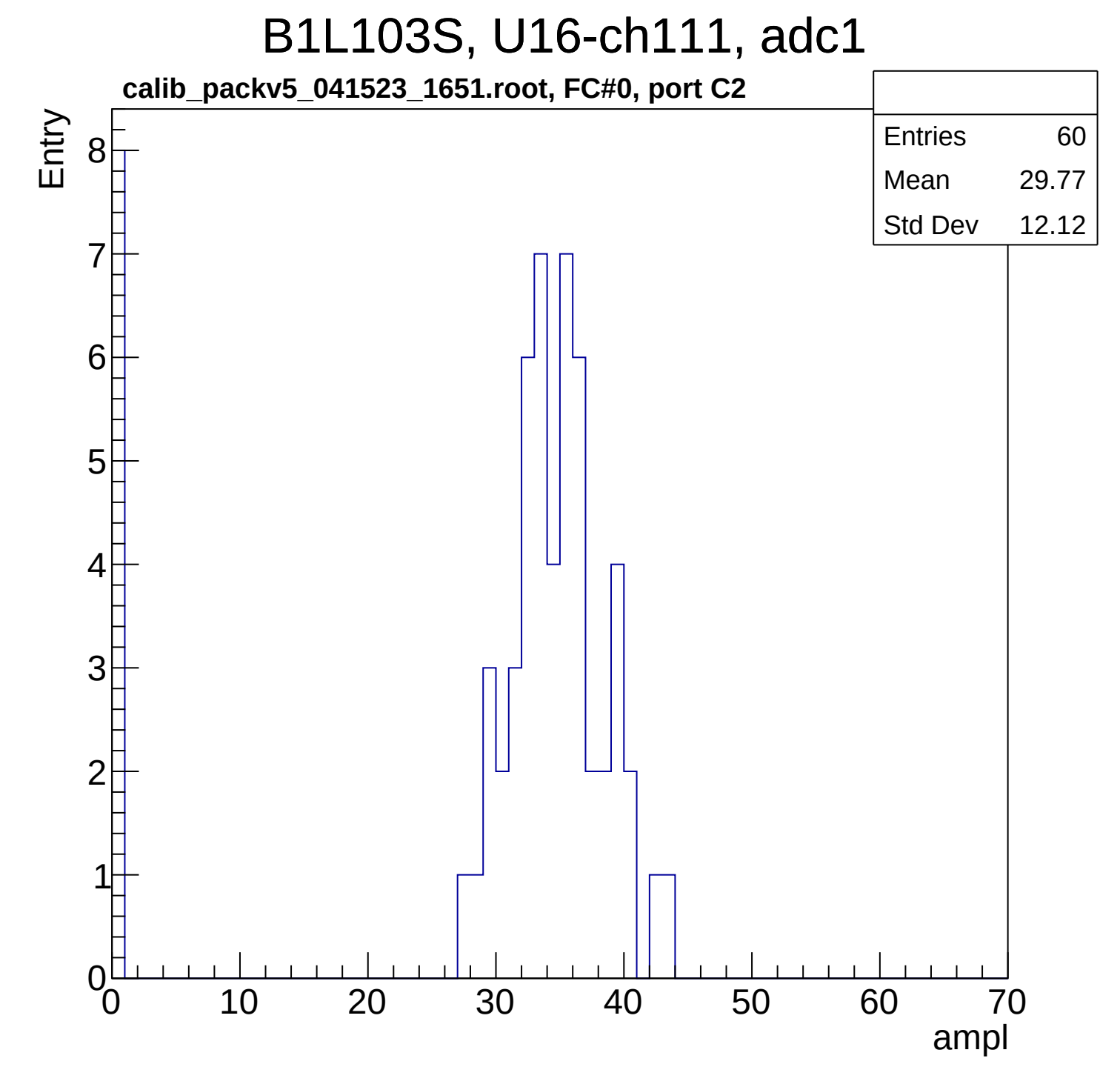

B1L103S, U16-ch110, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 52.21
Std Dev 3.703
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch110, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 57.1
Std Dev 3.879
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch110, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 58.58
Std Dev 10.9
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch110, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch111, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 21.16
Std Dev 11.91
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70


B1L103S, U16-ch111, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 29.77
Std Dev 12.12
Entry
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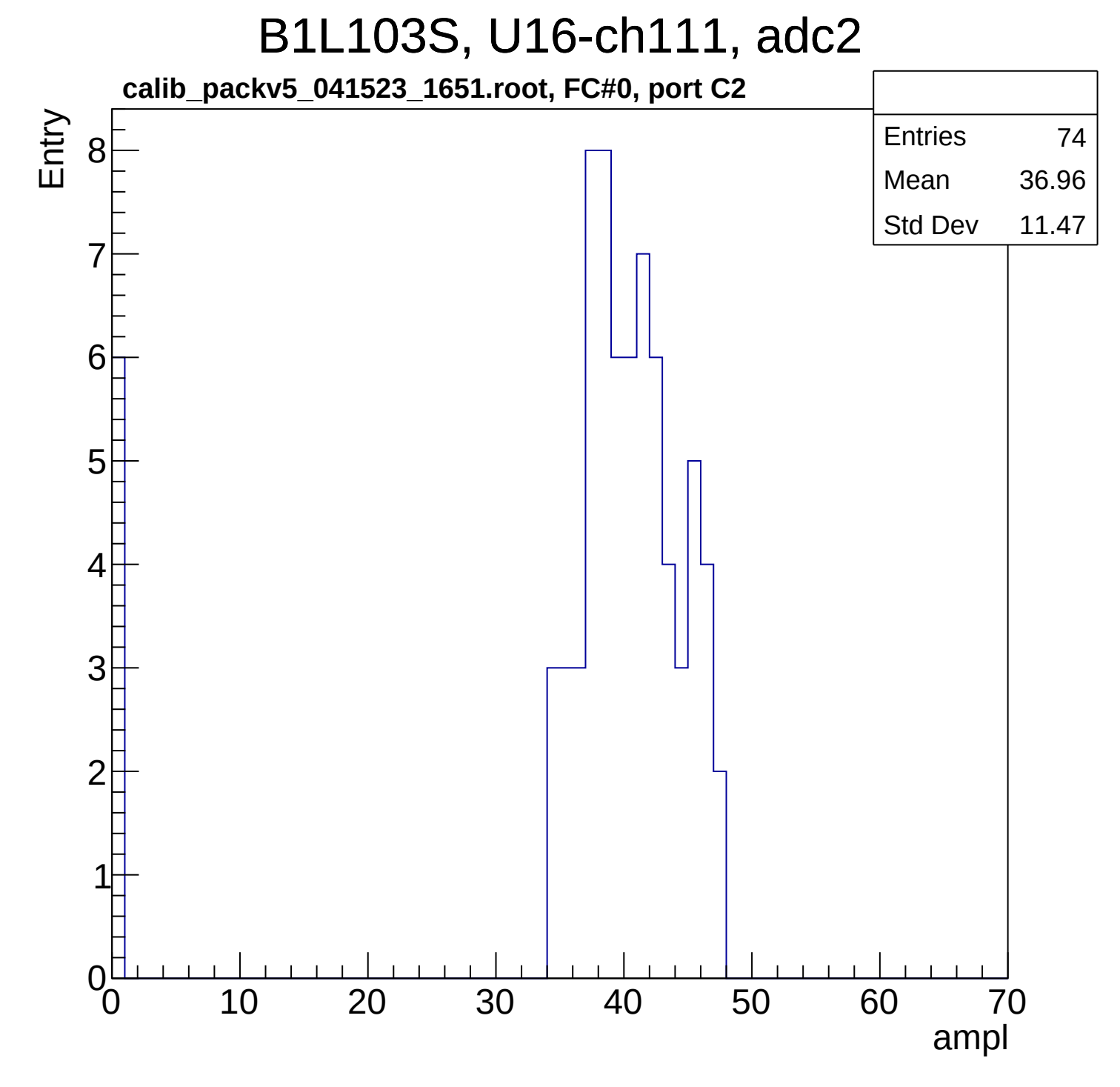
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch111, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 36.96
Std Dev 11.47
Entry
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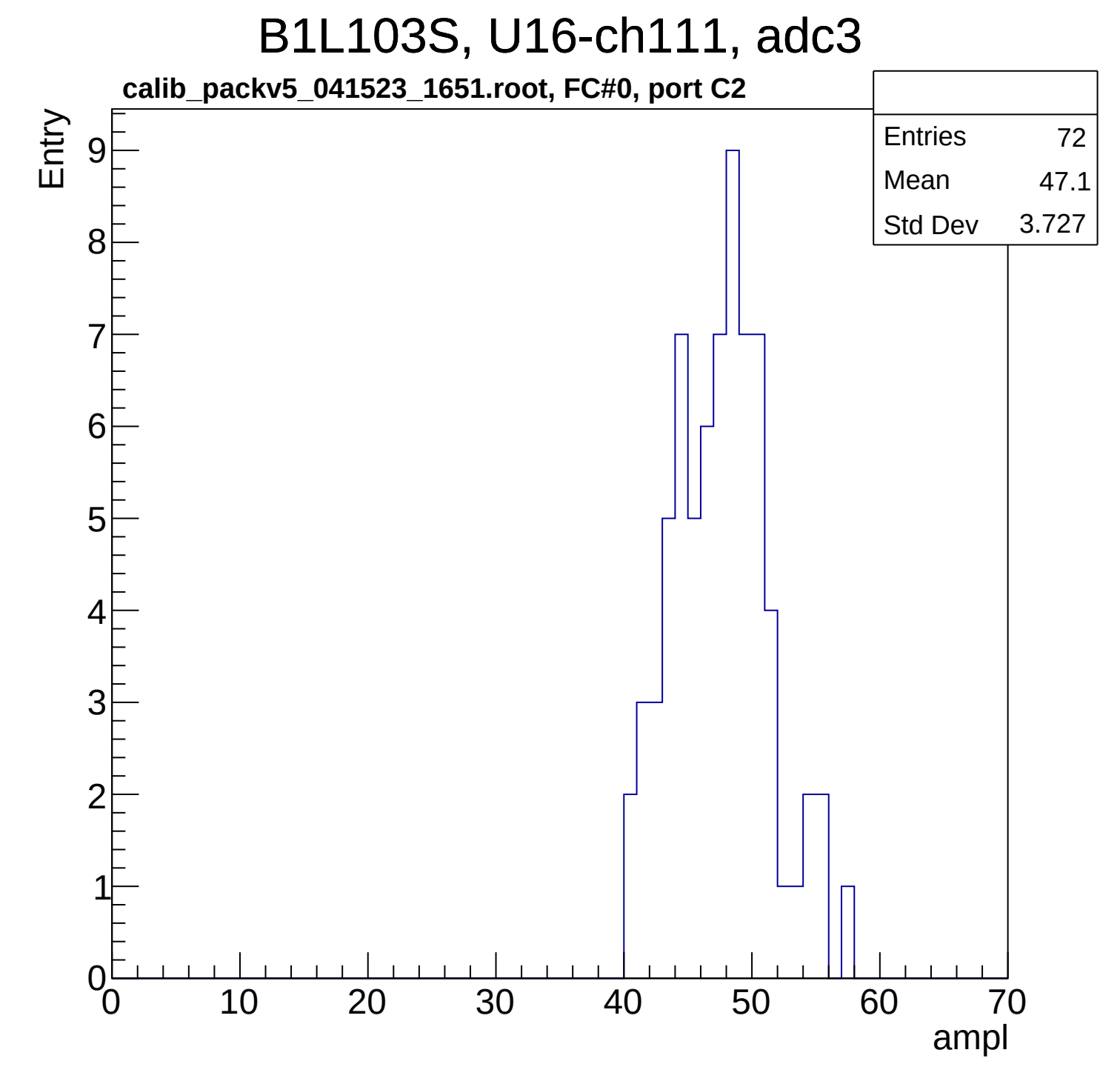
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch111, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 47.1
Std Dev 3.727
Entry
ampl
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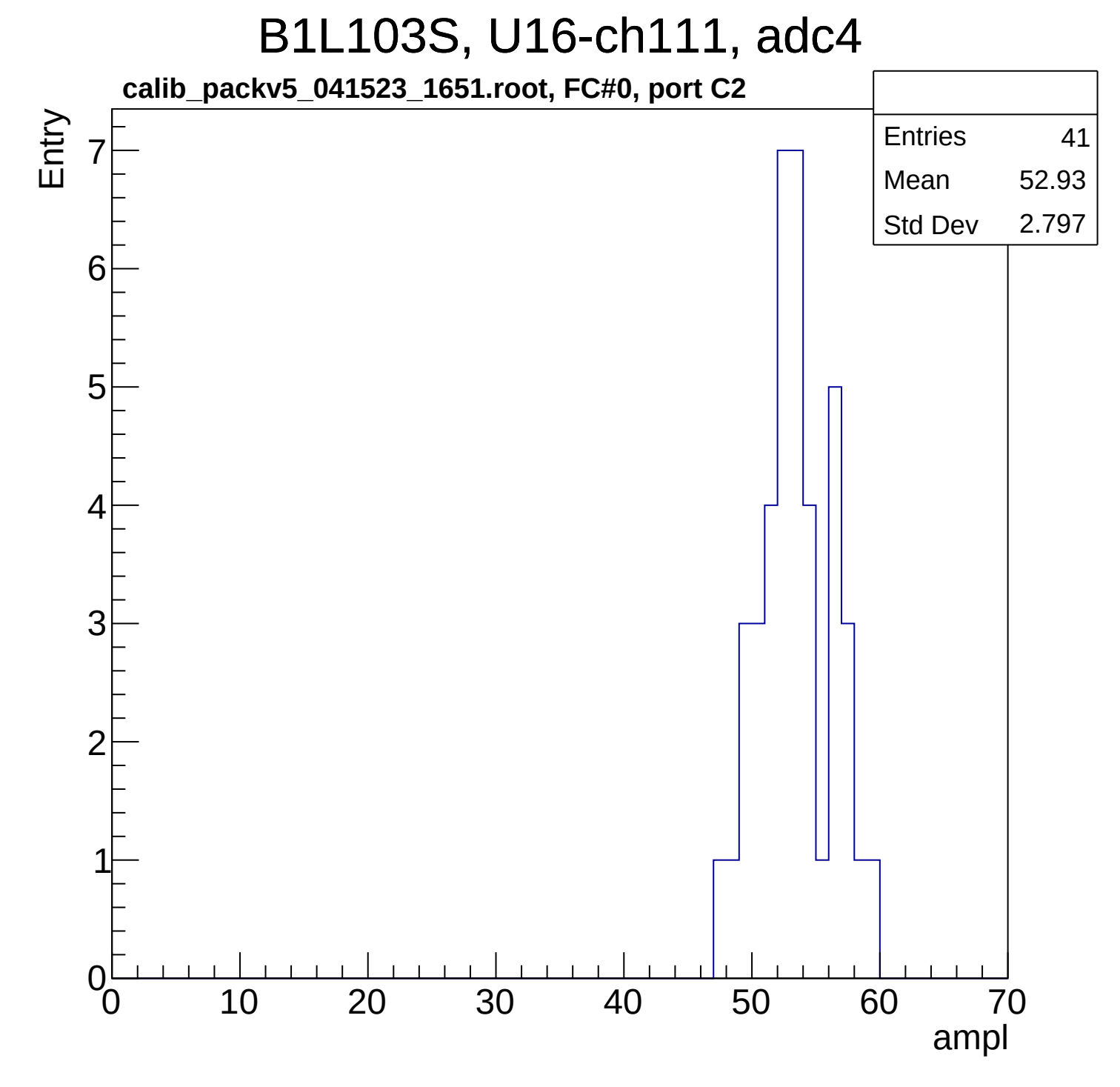
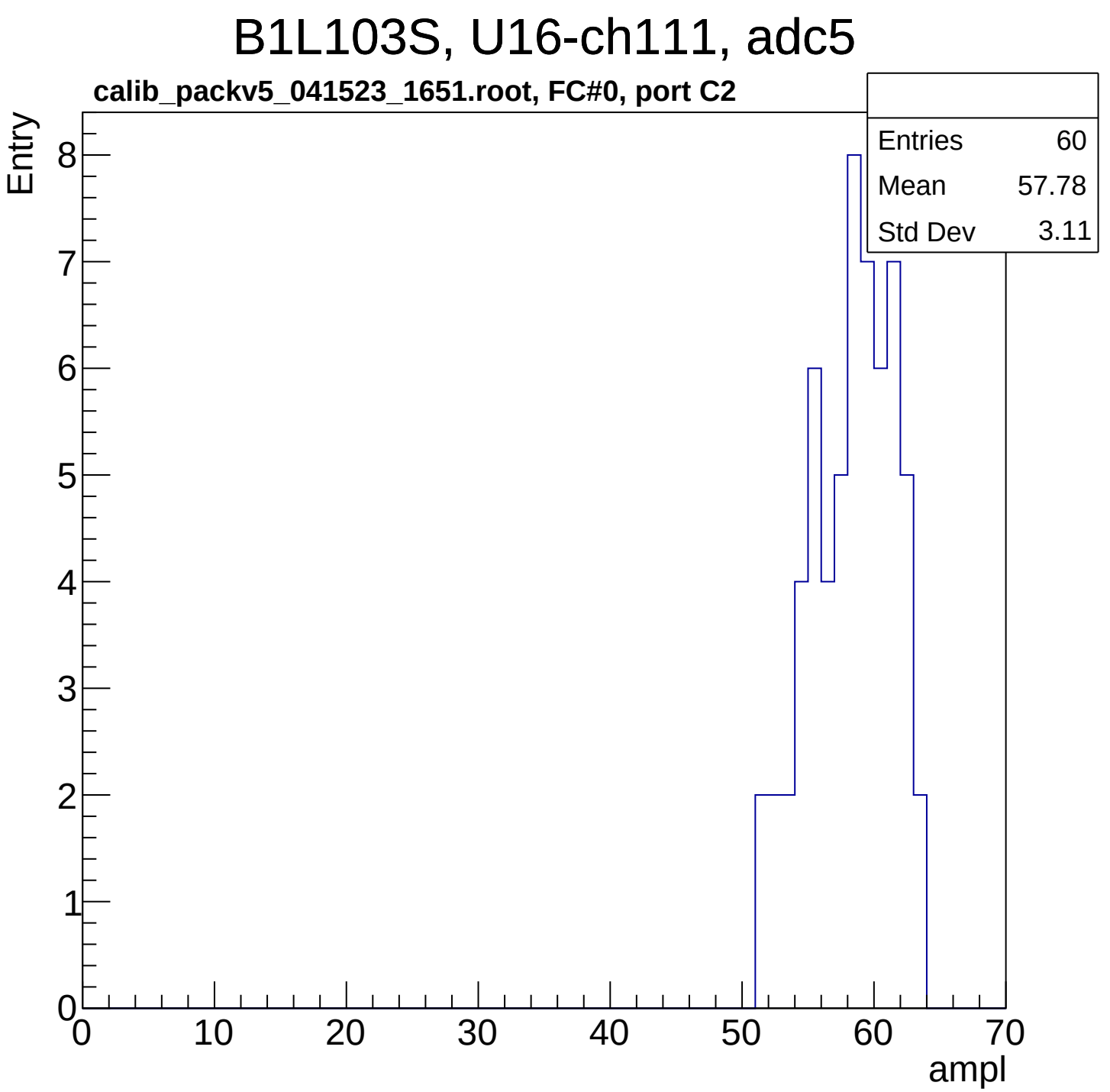
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch111, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 52.93
Std Dev 2.797
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch111, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 57.78
Std Dev 3.11
Entry
ampl
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2
3
4
5
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7
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0
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20
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40
50
60
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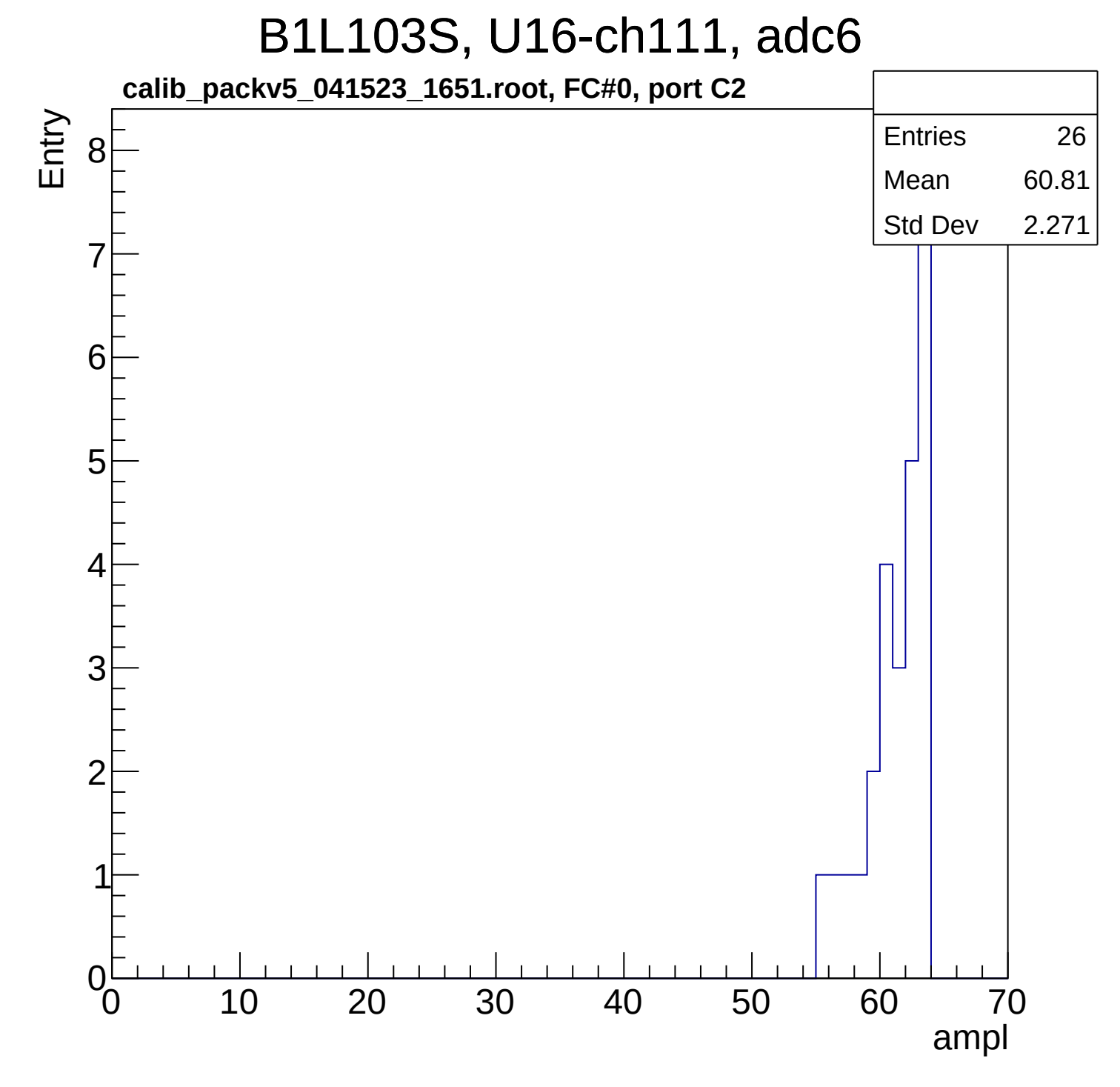
B1L103S, U16-ch111, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 60.81
Std Dev 2.271
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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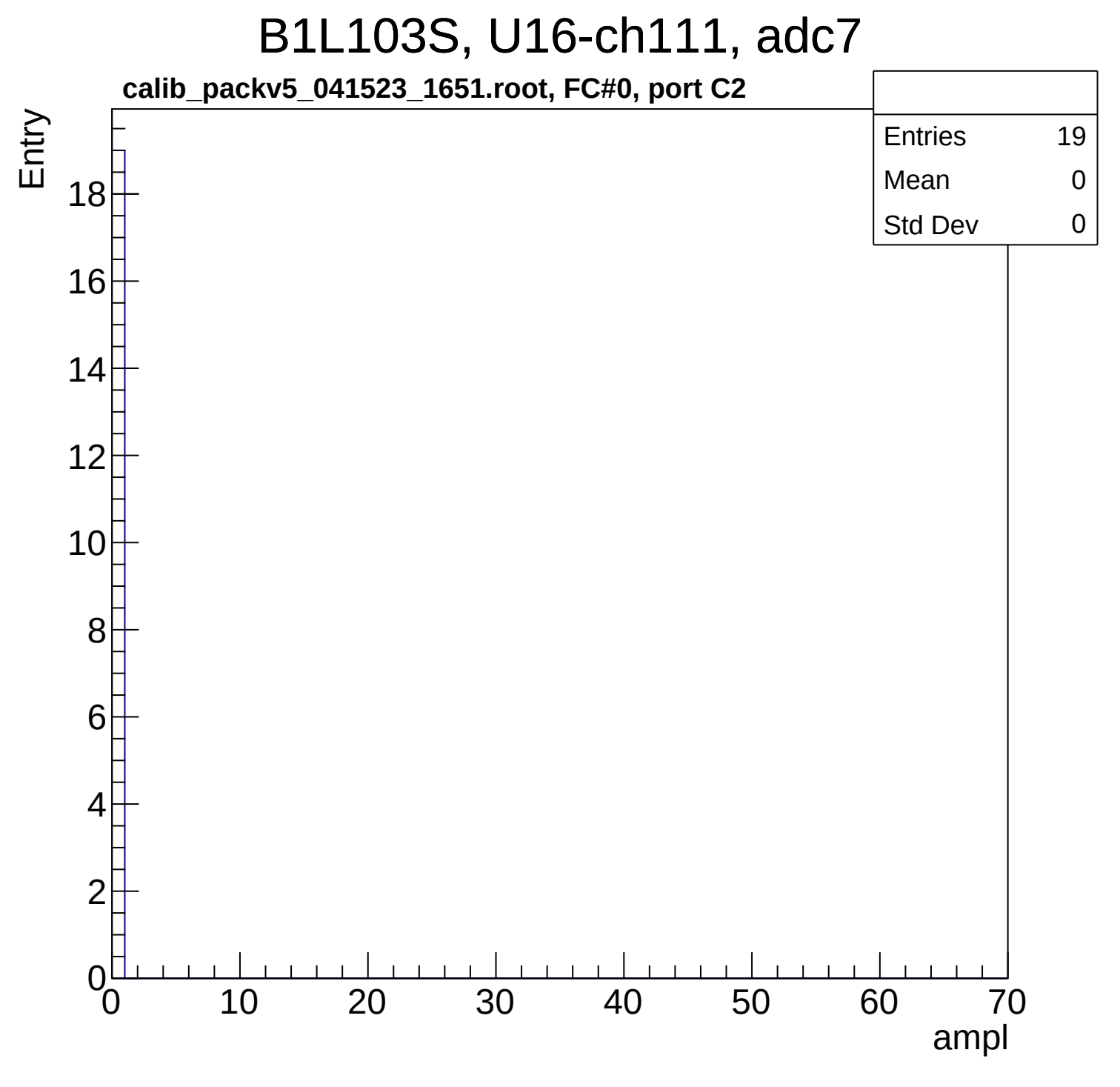
B1L103S, U16-ch111, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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2
4
6
8
10
12
14
16
18
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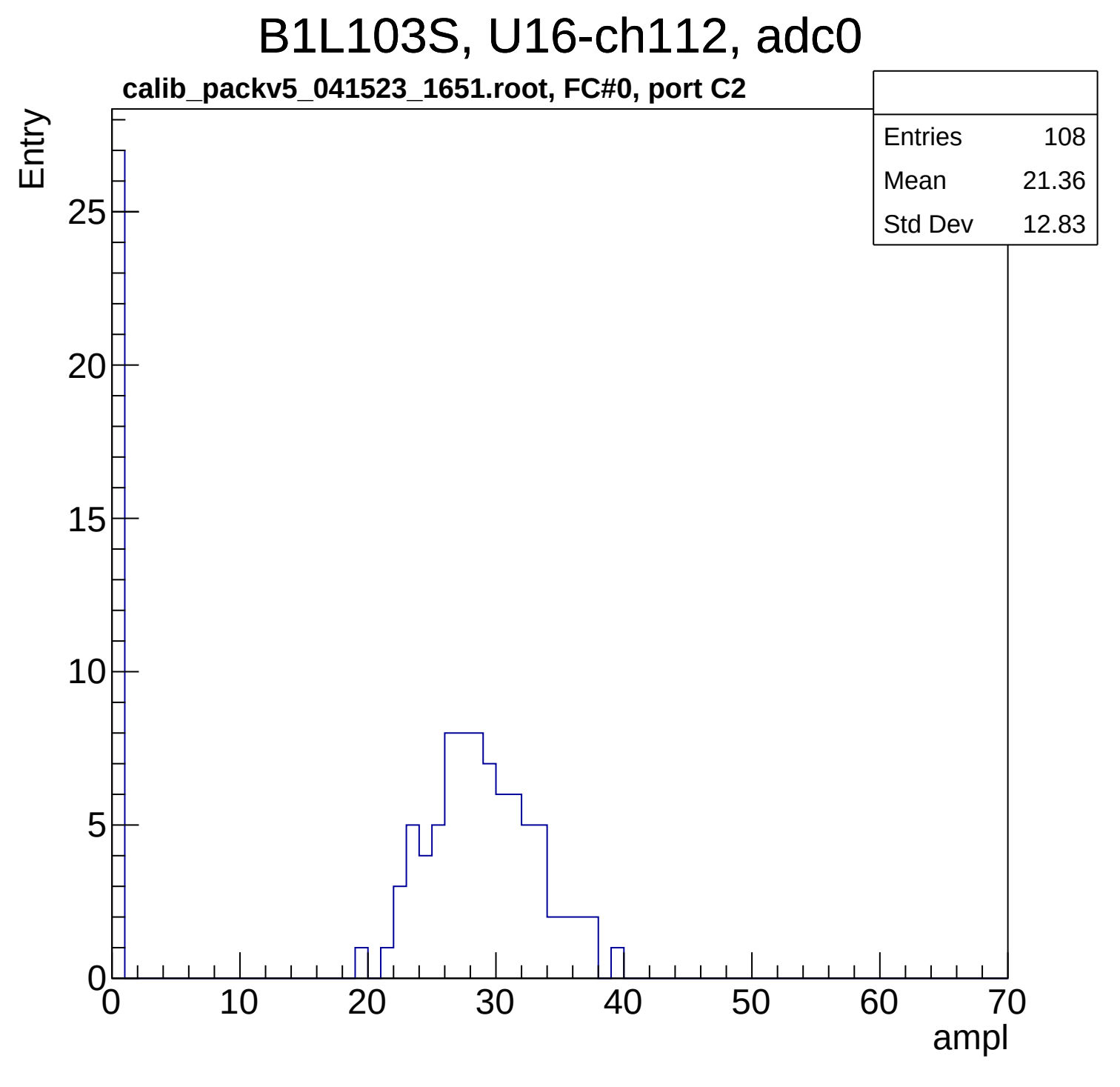
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch112, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 108
Mean 21.36
Std Dev 12.83
Entry
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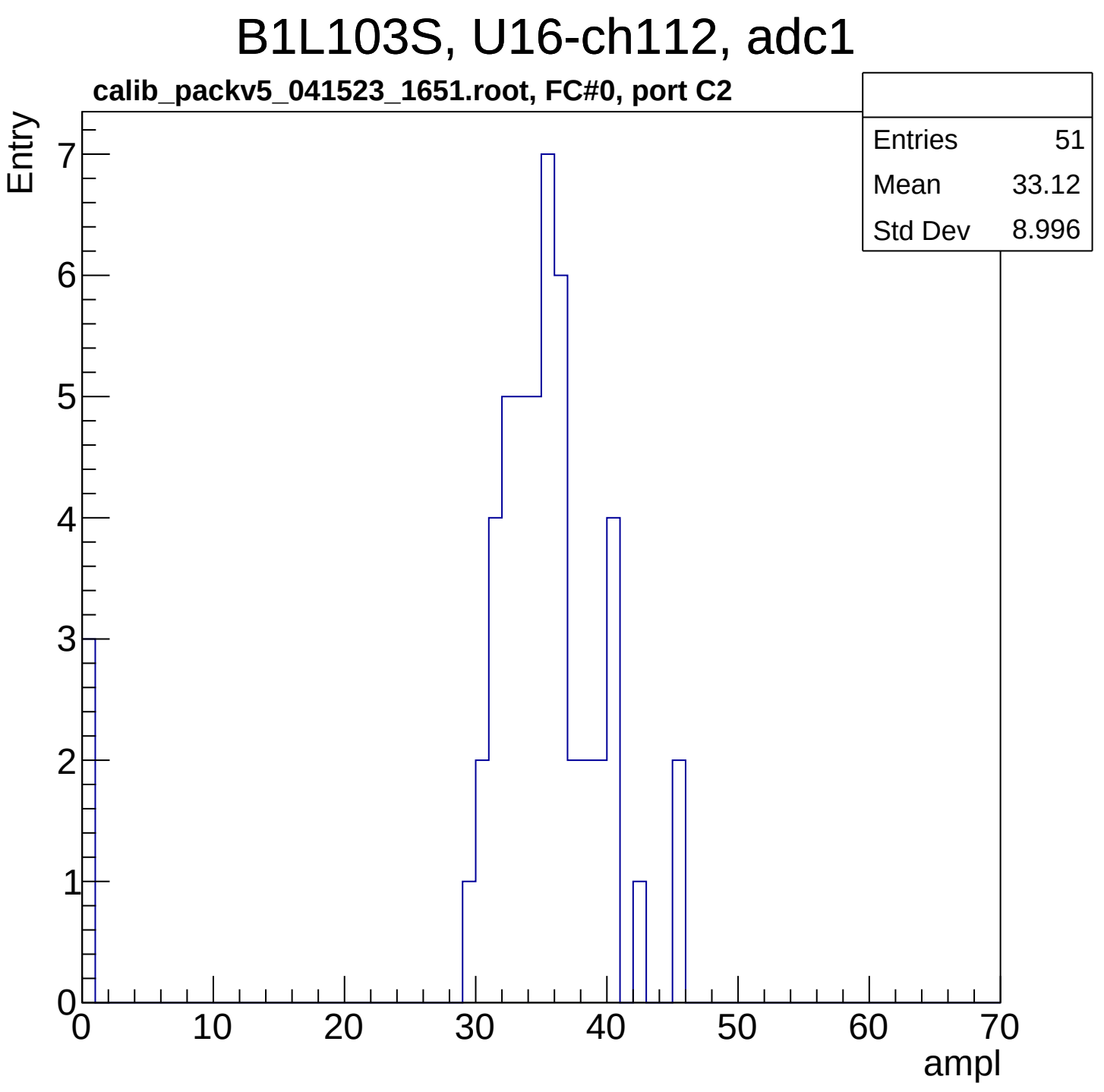
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch112, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 33.12
Std Dev 8.996
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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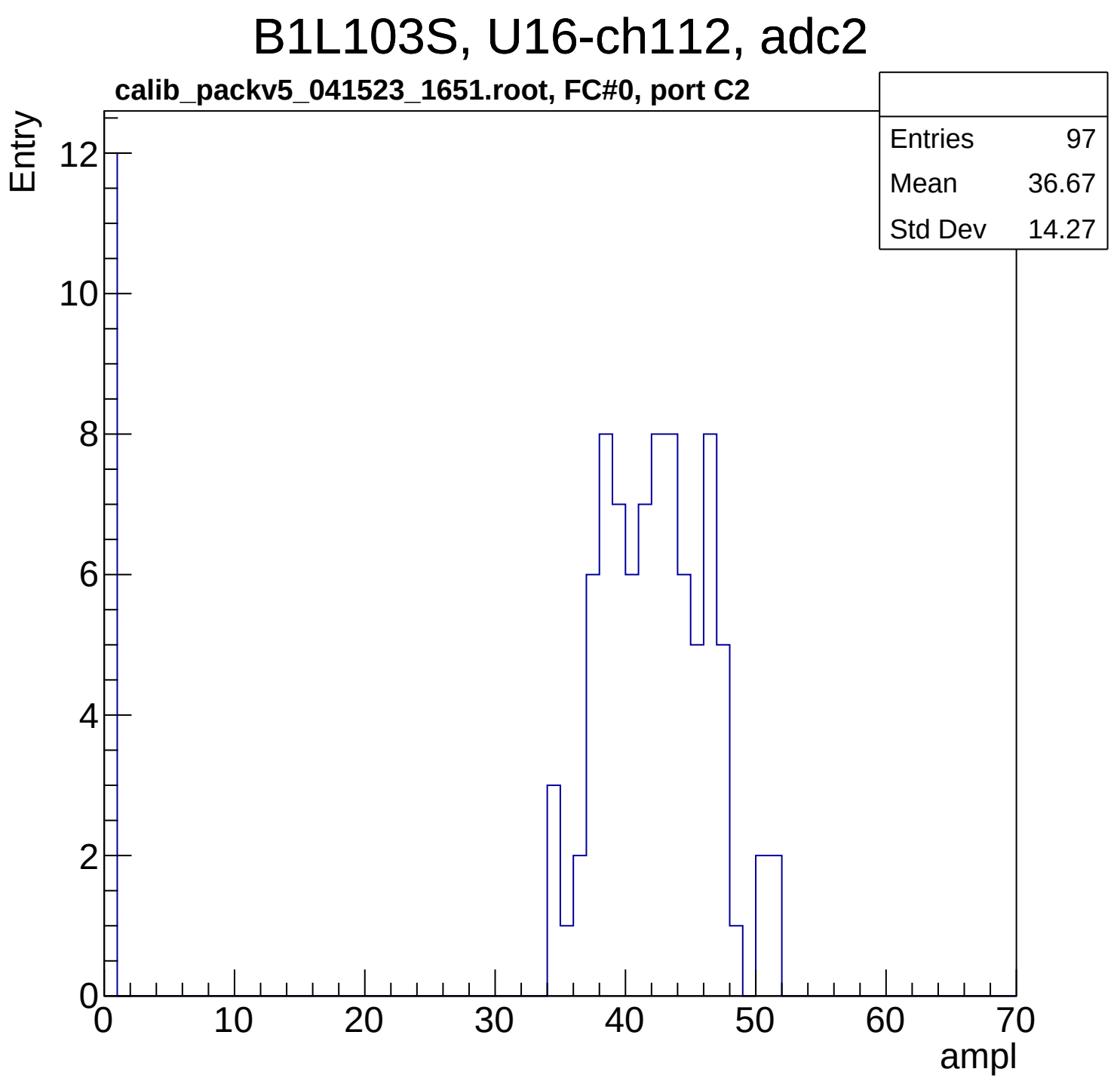
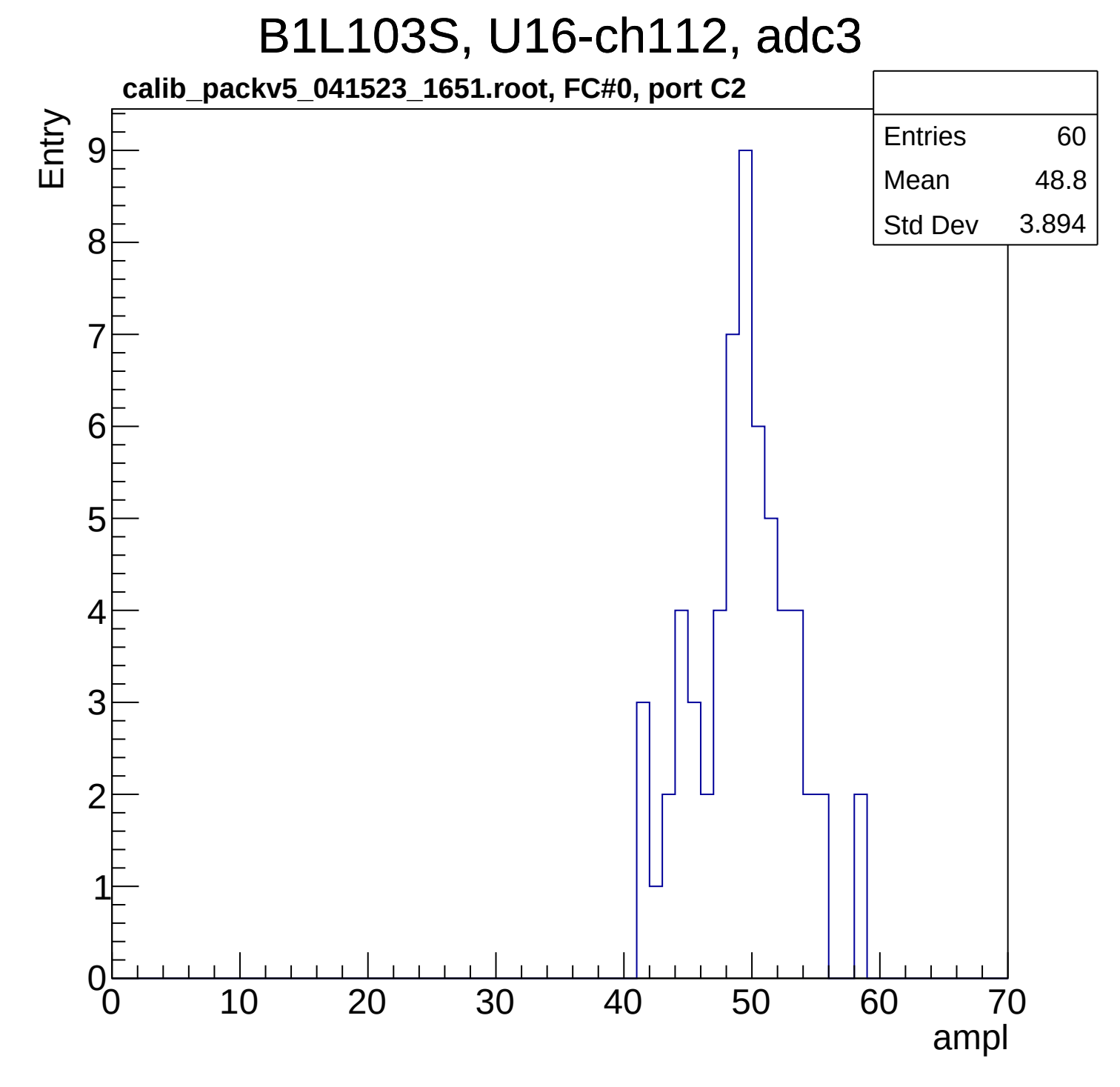

B1L103S, U16-ch112, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 36.67
Std Dev 14.27
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch112, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 48.8
Std Dev 3.894
Entry
ampl
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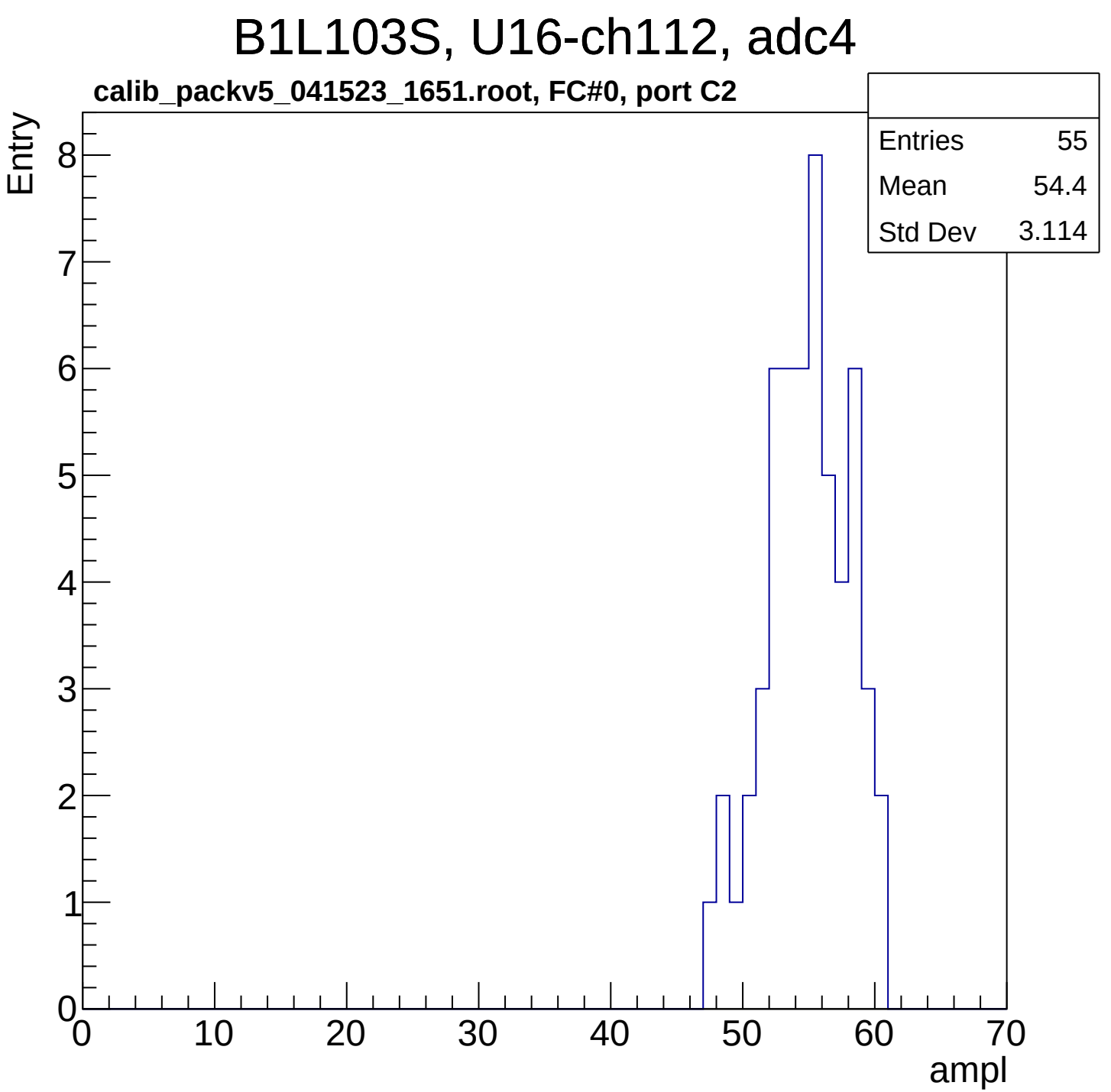
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch112, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 54.4
Std Dev 3.114
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
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60
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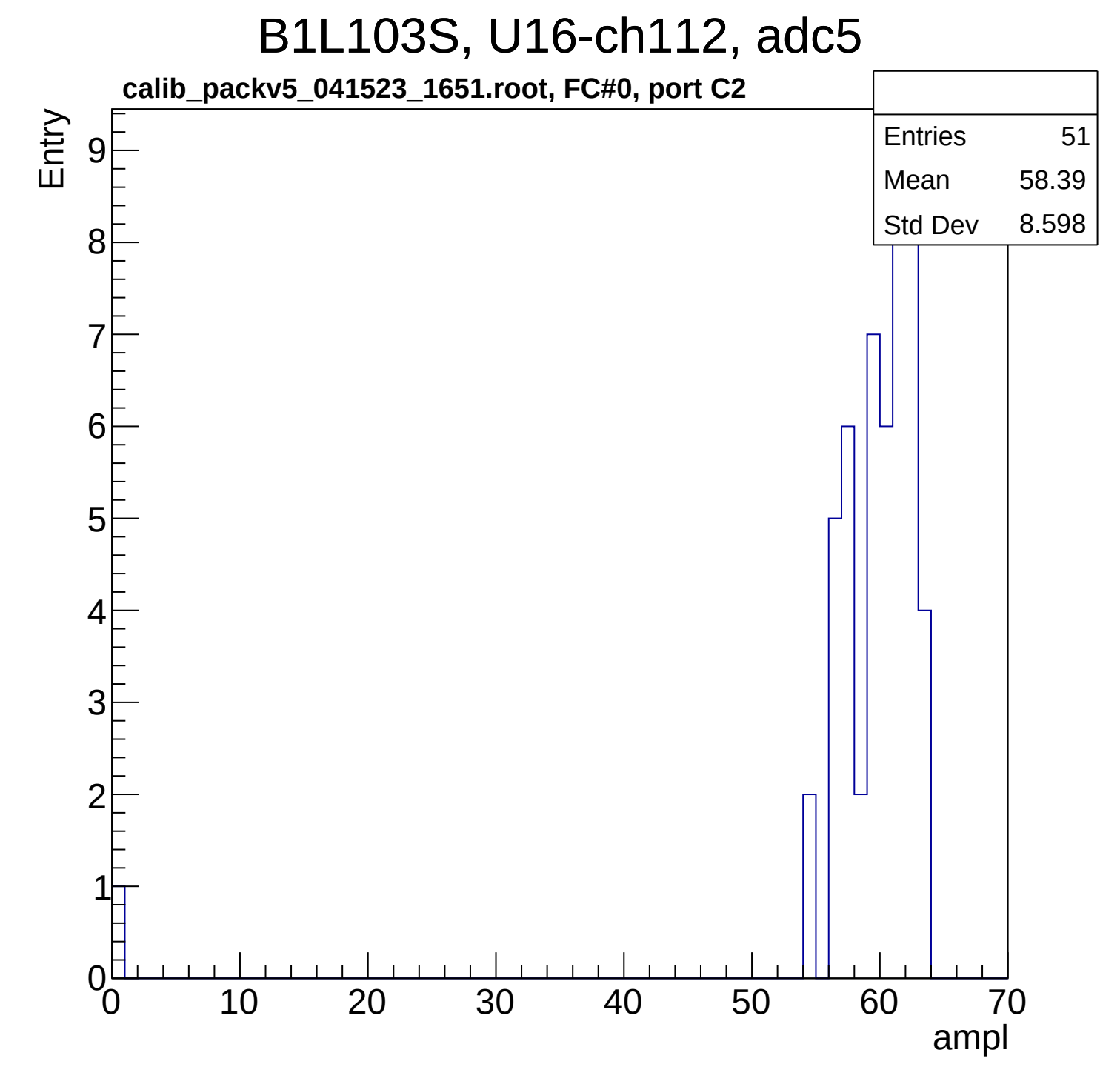
B1L103S, U16-ch112, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.39
Std Dev 8.598
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
50
60
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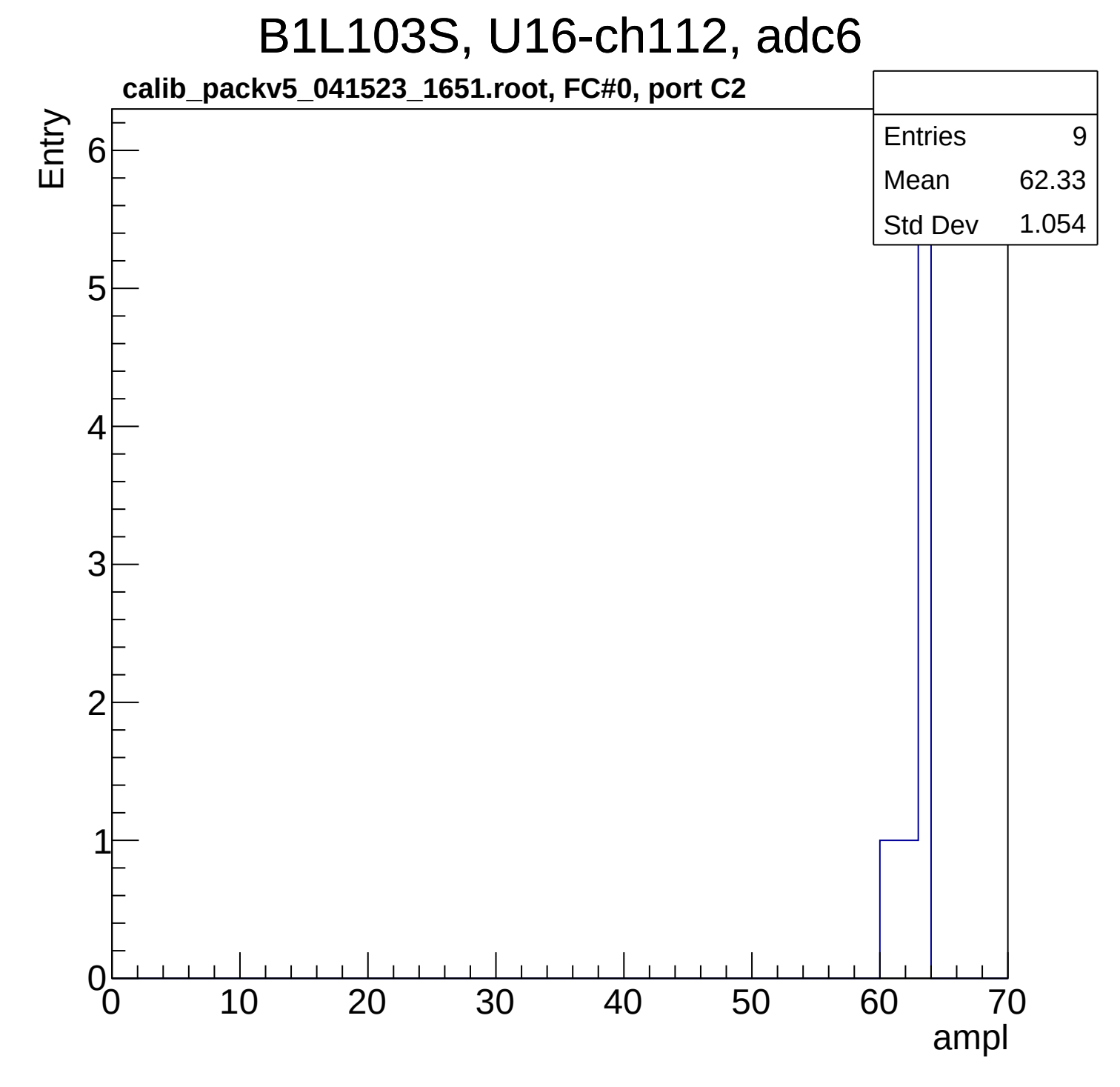
B1L103S, U16-ch112, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 62.33
Std Dev 1.054
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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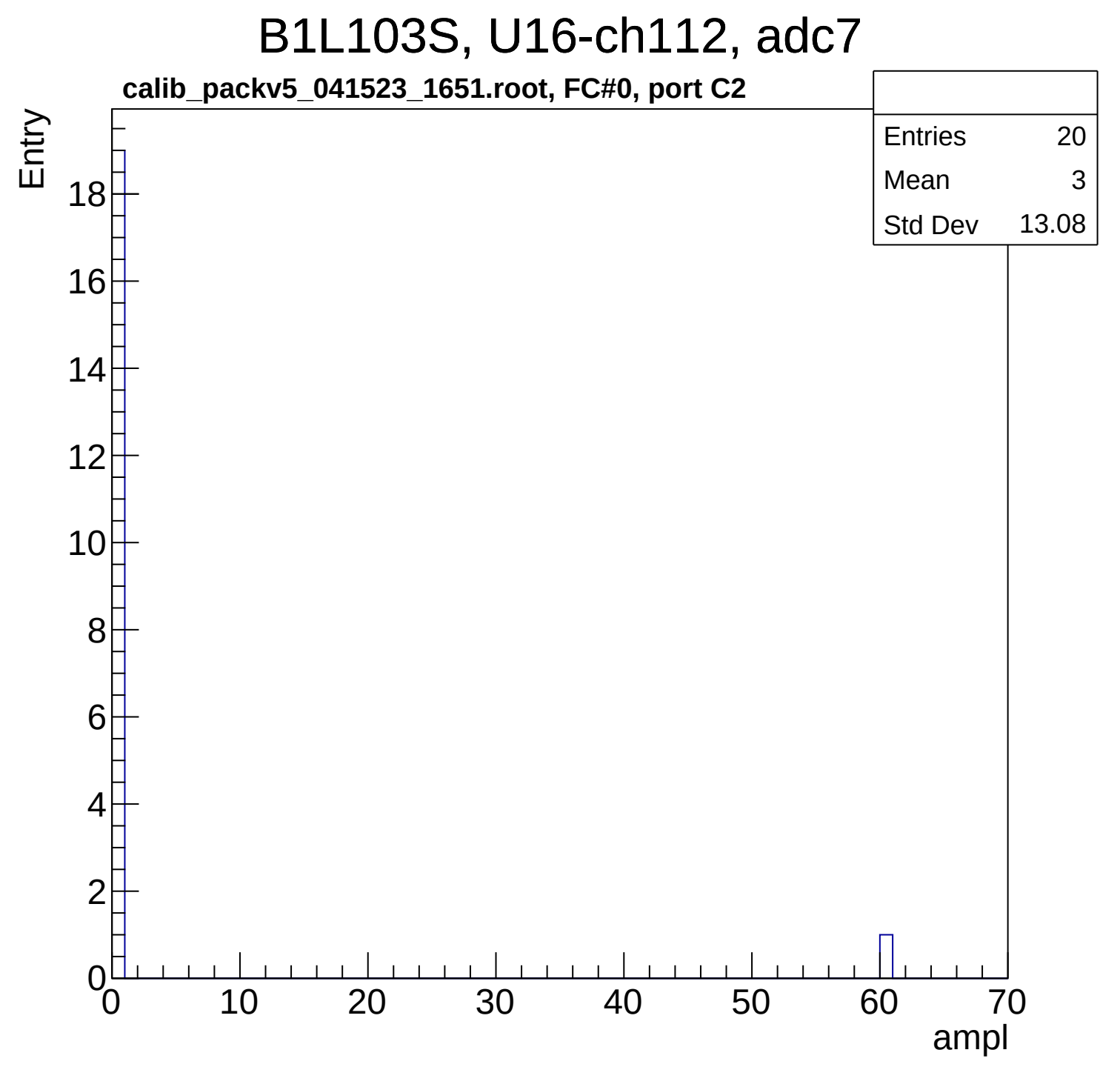
B1L103S, U16-ch112, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3
Std Dev 13.08
Entry
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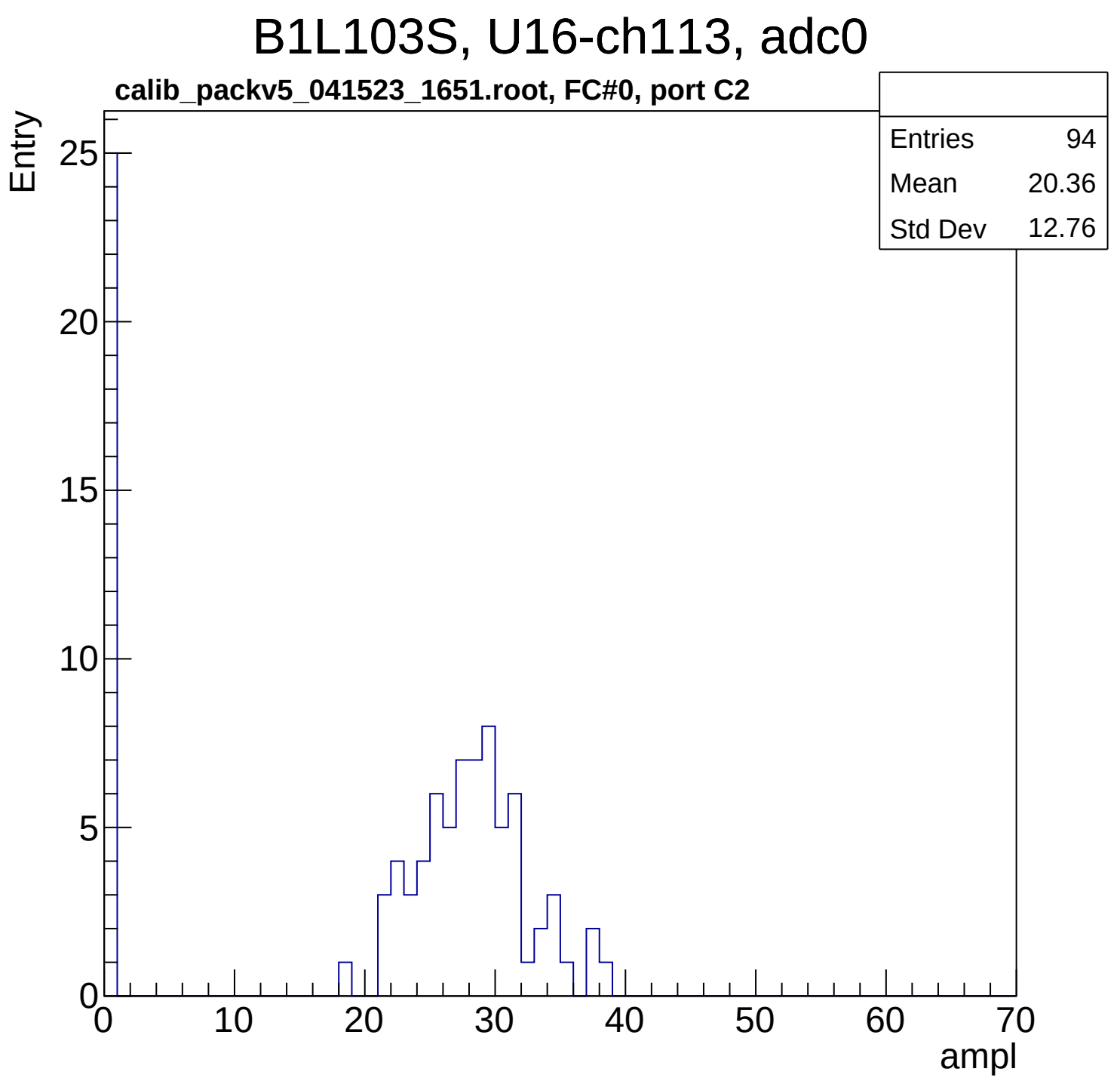
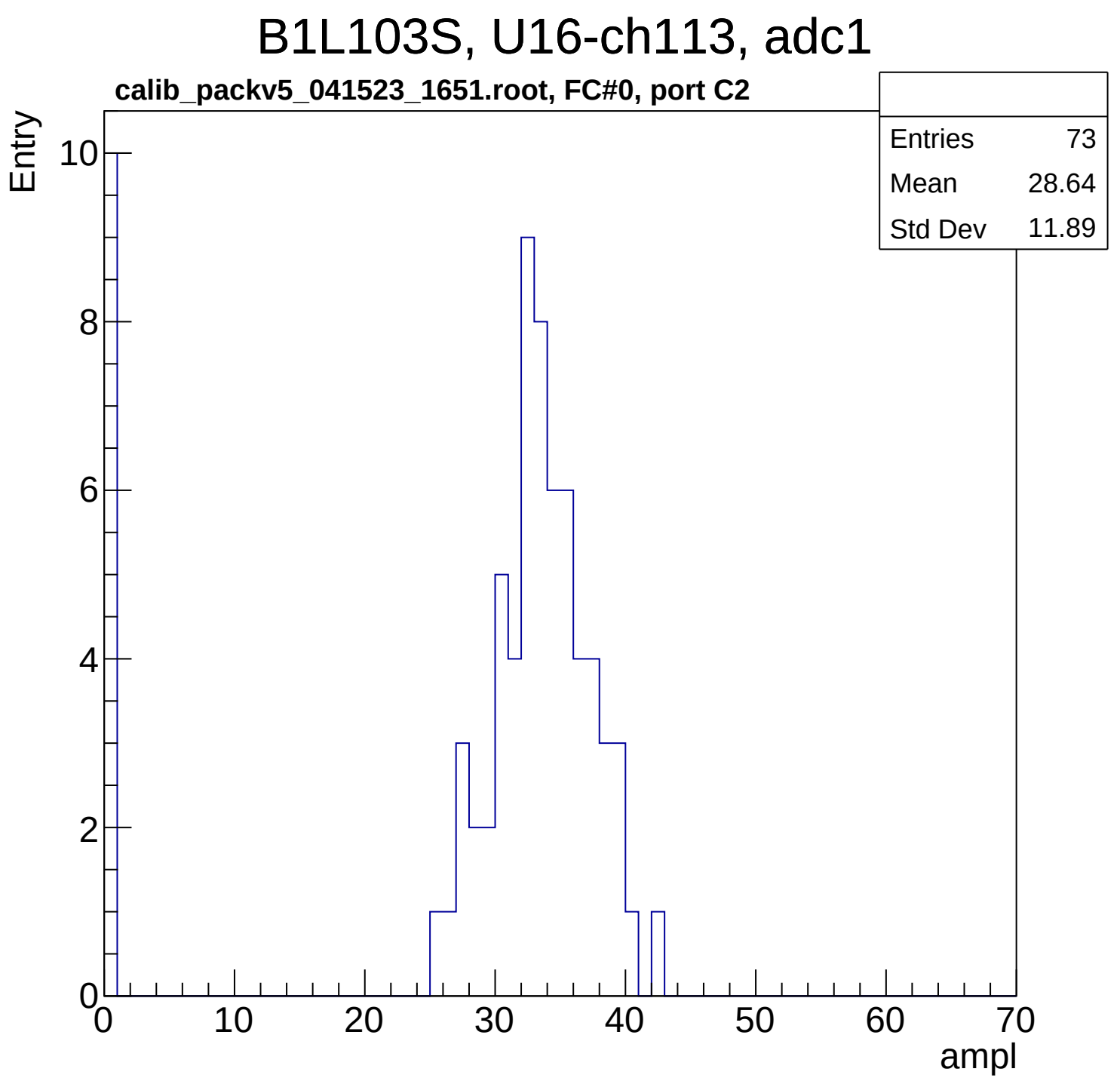
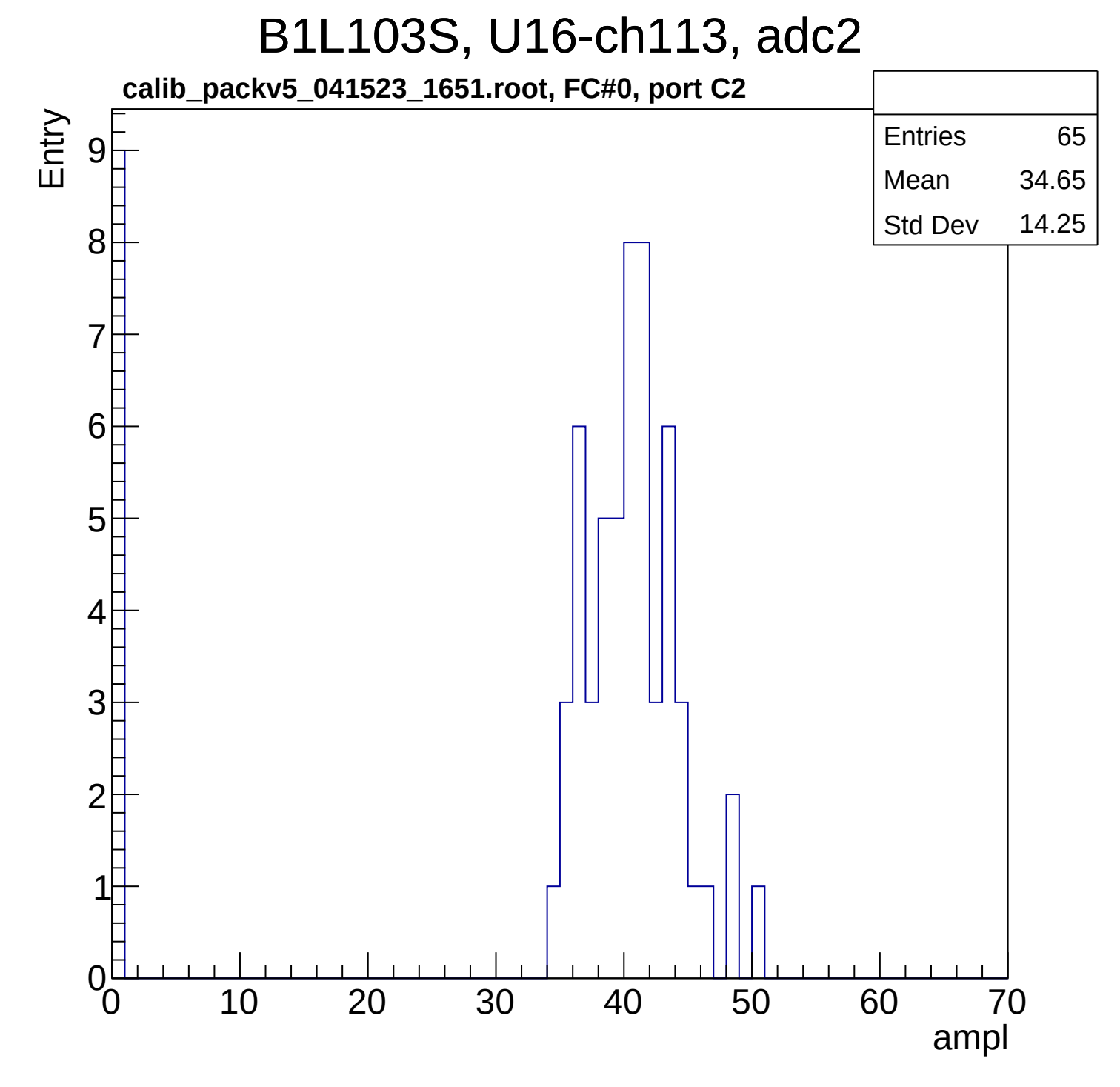
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch113, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 20.36
Std Dev 12.76
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch113, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 28.64
Std Dev 11.89
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch113, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 34.65
Std Dev 14.25
Entry
ampl
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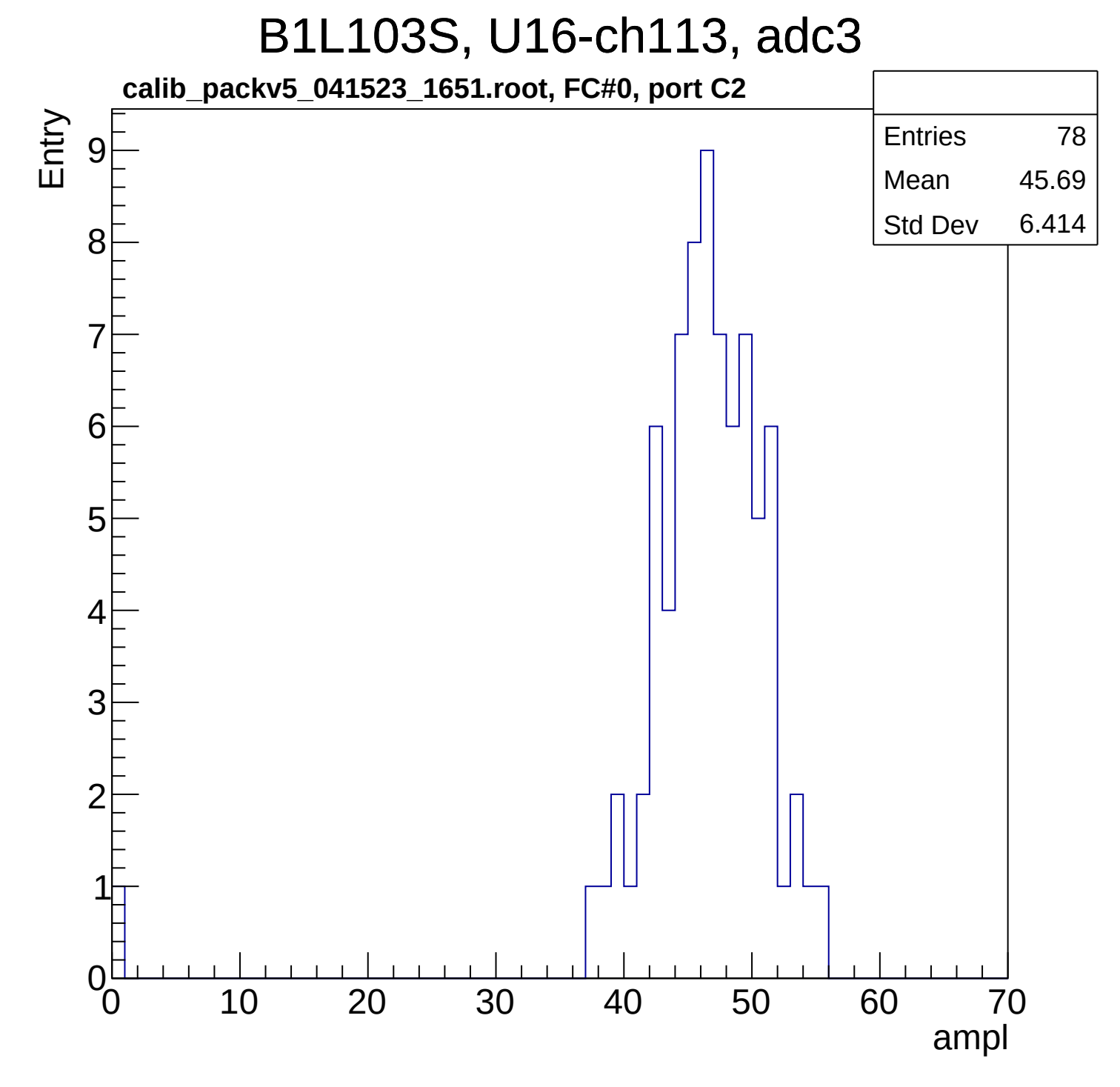
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch113, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 45.69
Std Dev 6.414
Entry
ampl
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2
3
4
5
6
7
8
9
0
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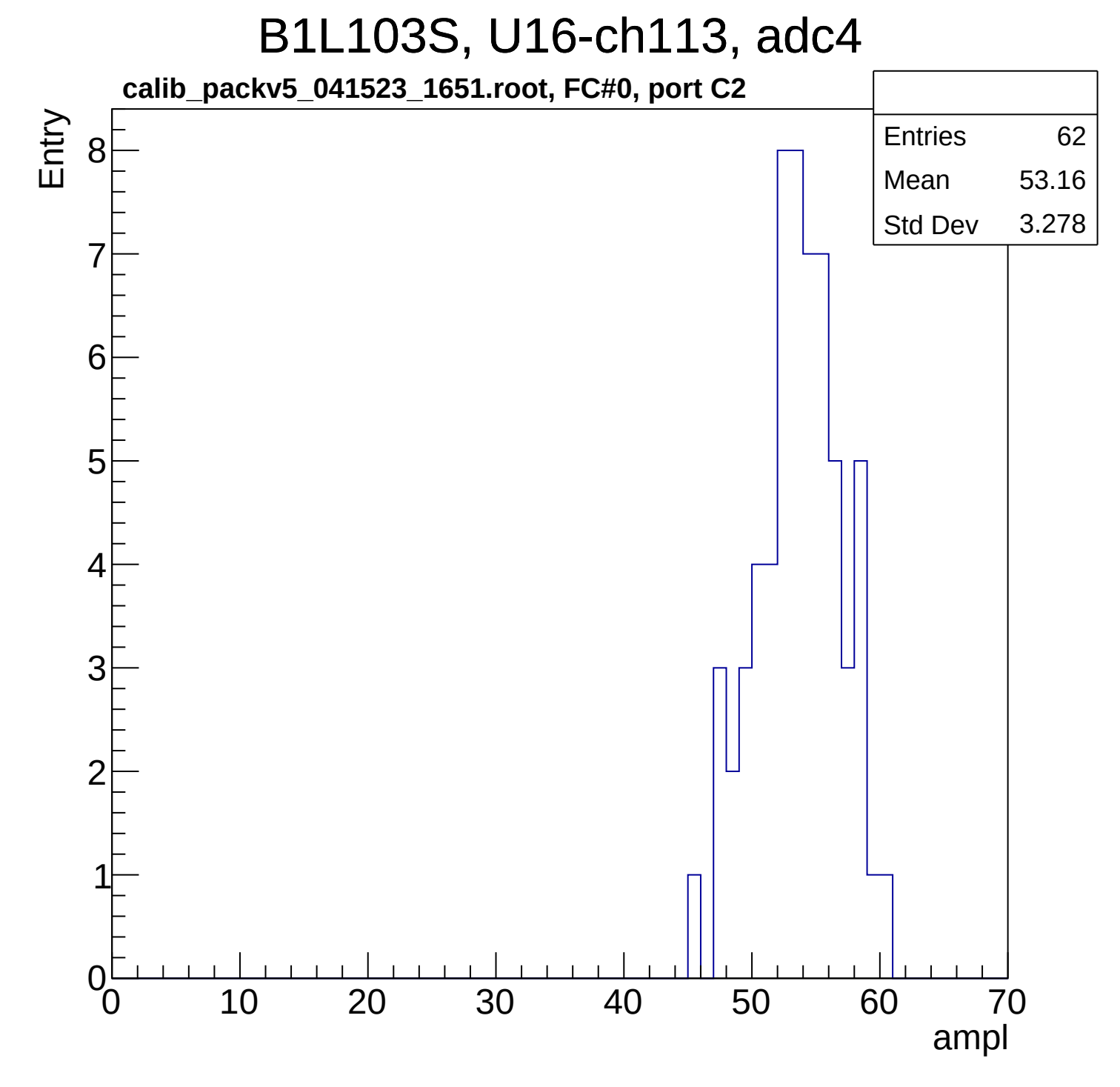
B1L103S, U16-ch113, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 53.16
Std Dev 3.278
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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60
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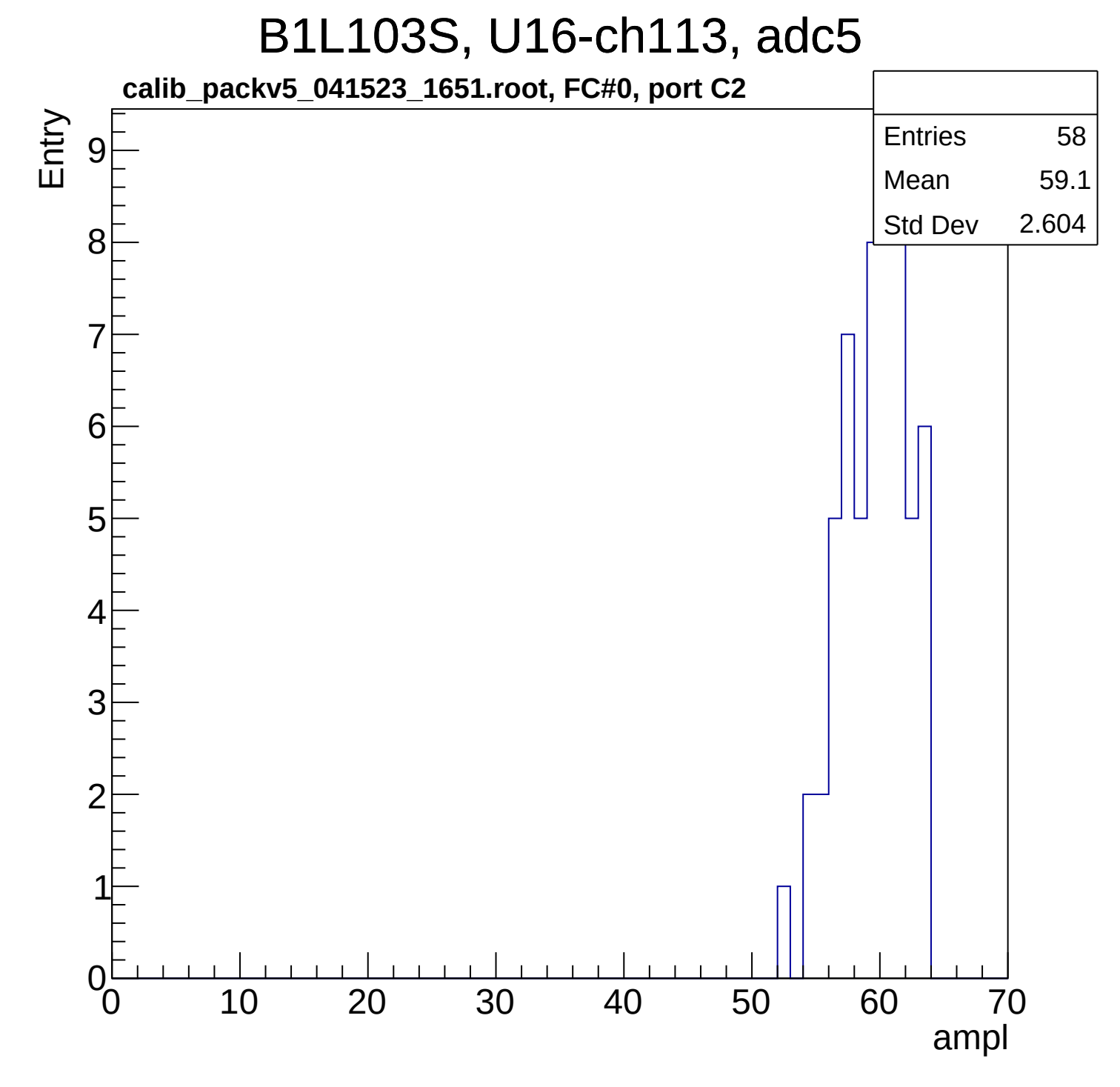
B1L103S, U16-ch113, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 59.1
Std Dev 2.604
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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60
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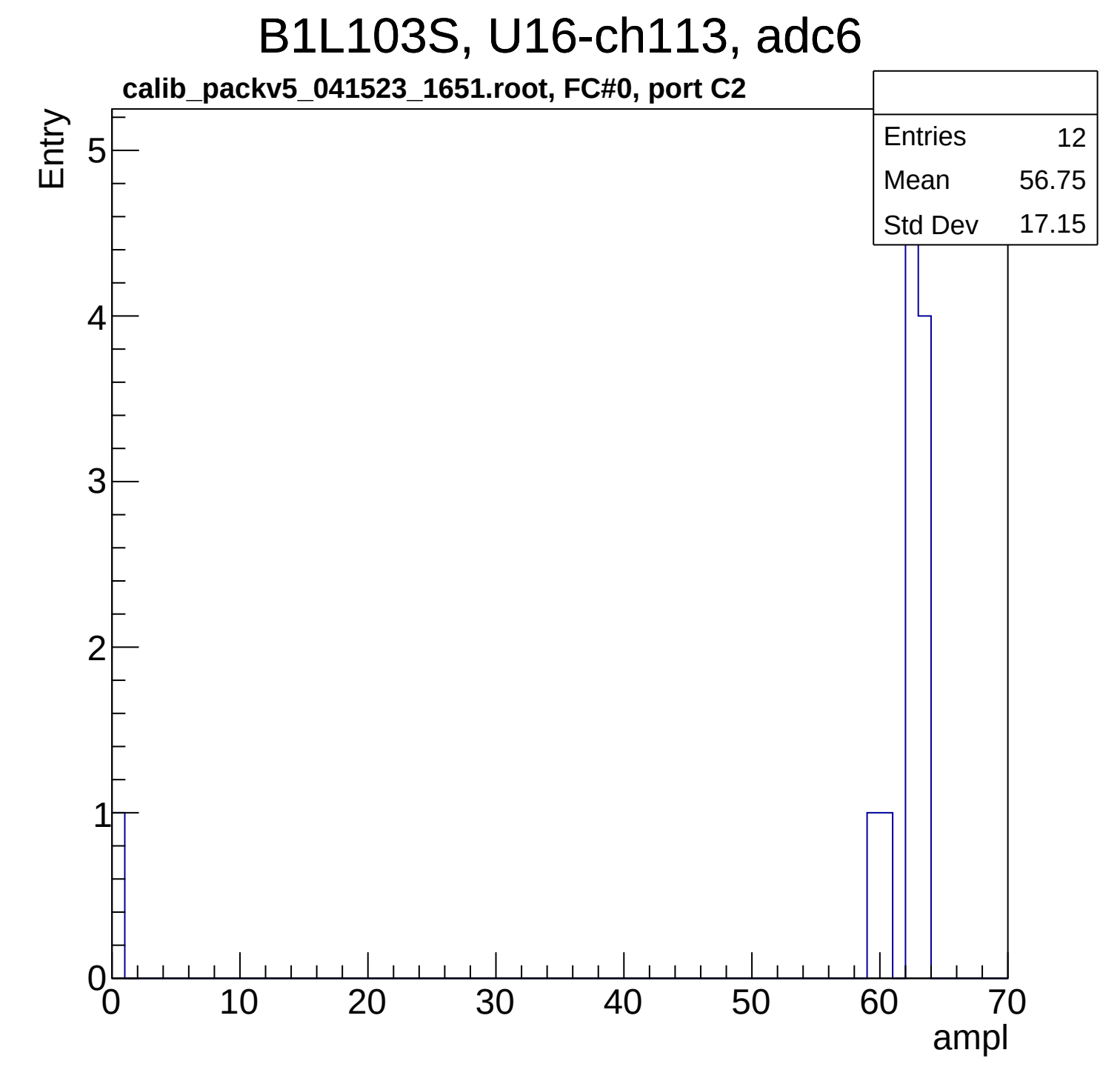
B1L103S, U16-ch113, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.75
Std Dev 17.15
Entry
ampl
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1
2
3
4
5
0
10
20
30
40
50
60
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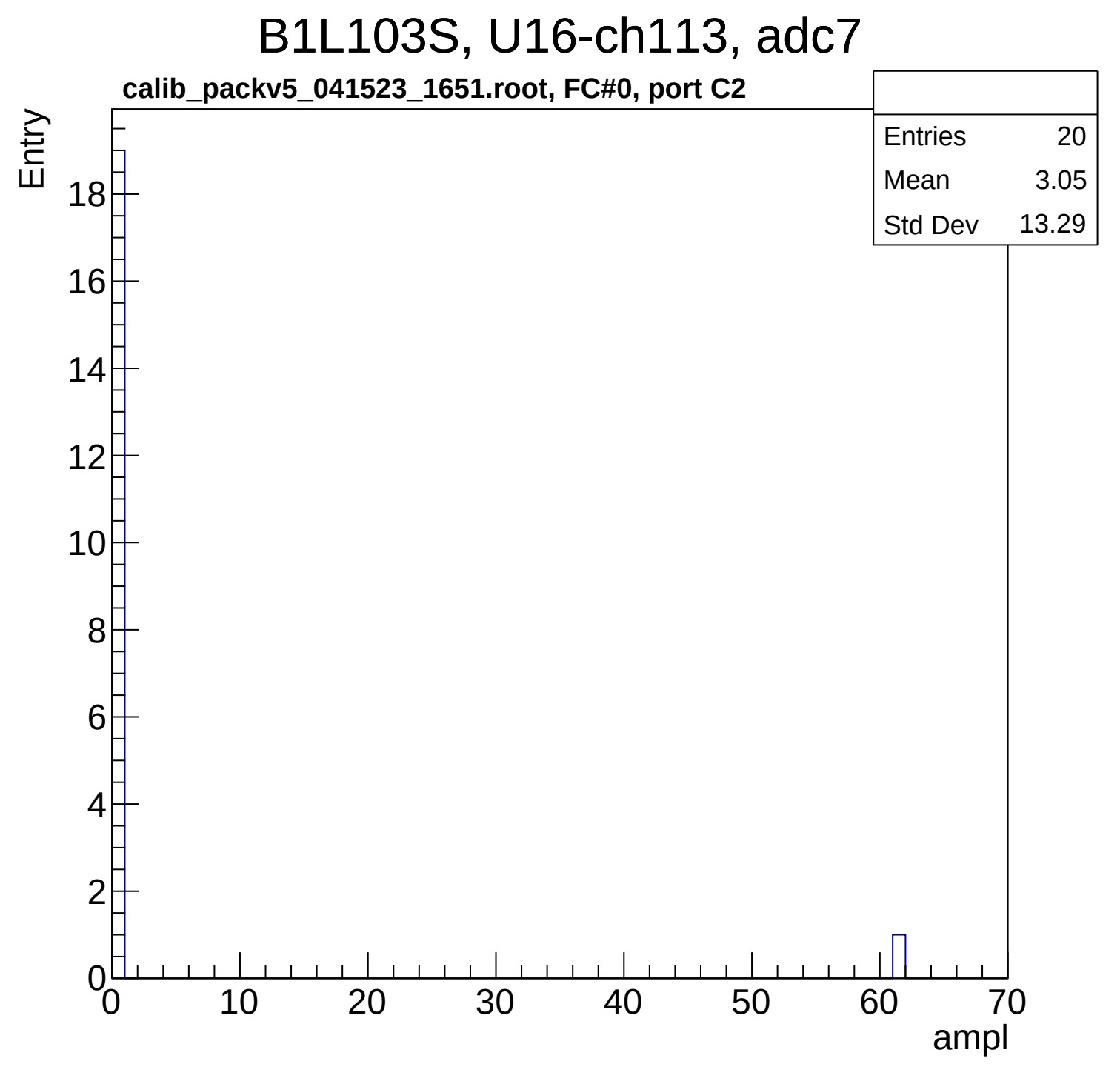
B1L103S, U16-ch113, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
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6
8
10
12
14
16
18
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10
20
30
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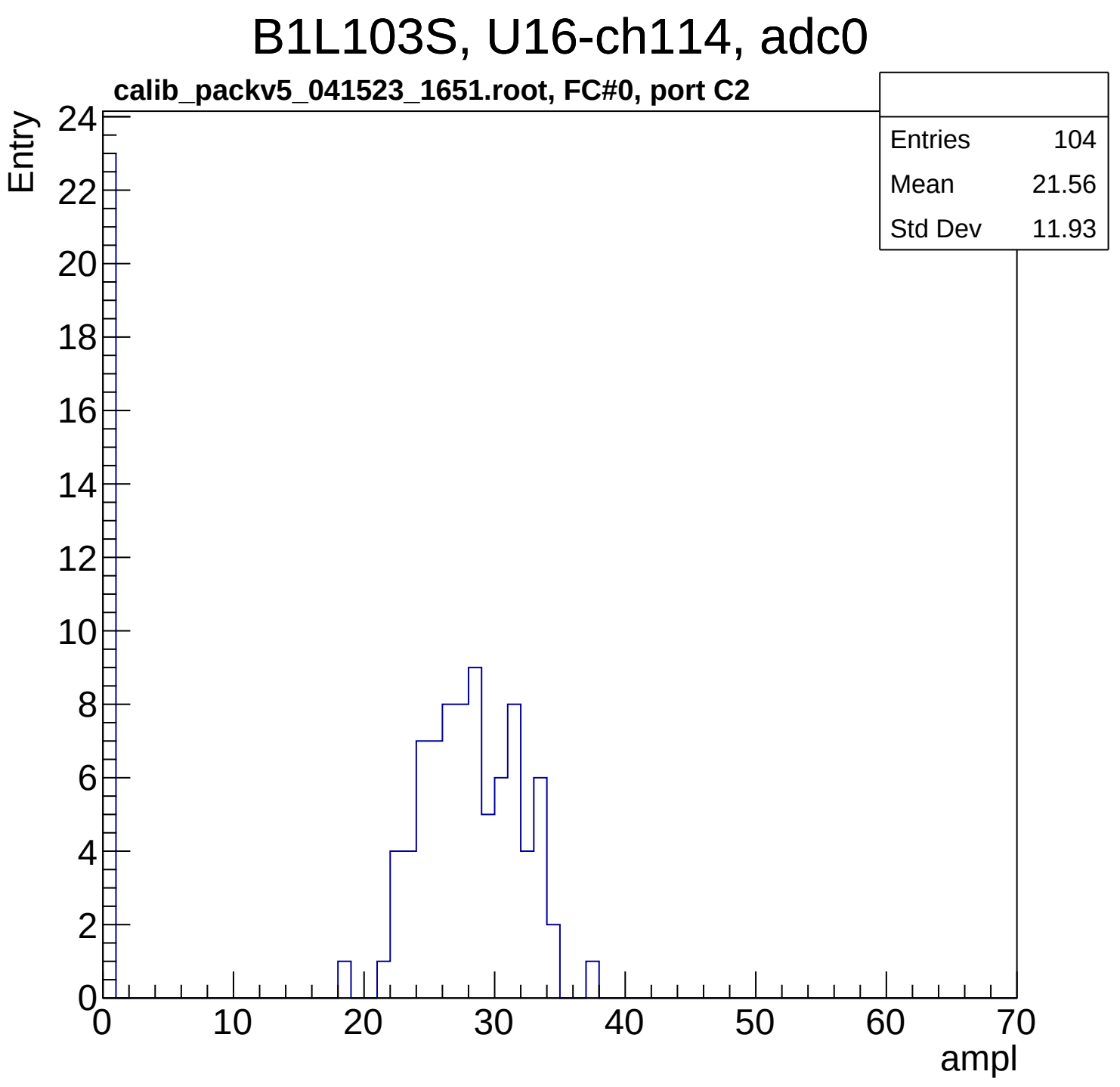
70
ampl


B1L103S, U16-ch114, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 21.56
Std Dev 11.93
Entry
ampl
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4
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10
12
14
16
18
20
22
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60
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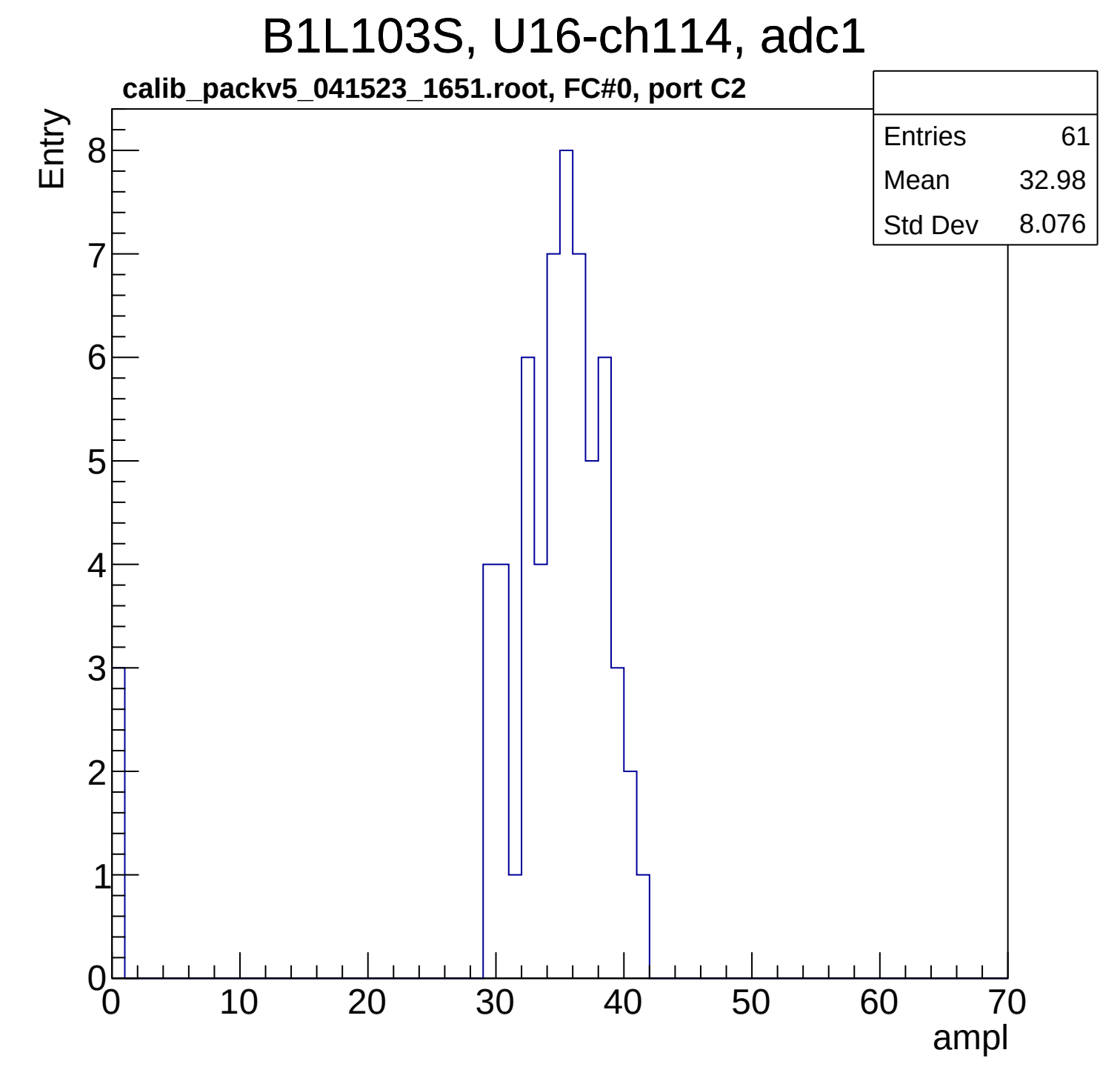
B1L103S, U16-ch114, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 32.98
Std Dev 8.076
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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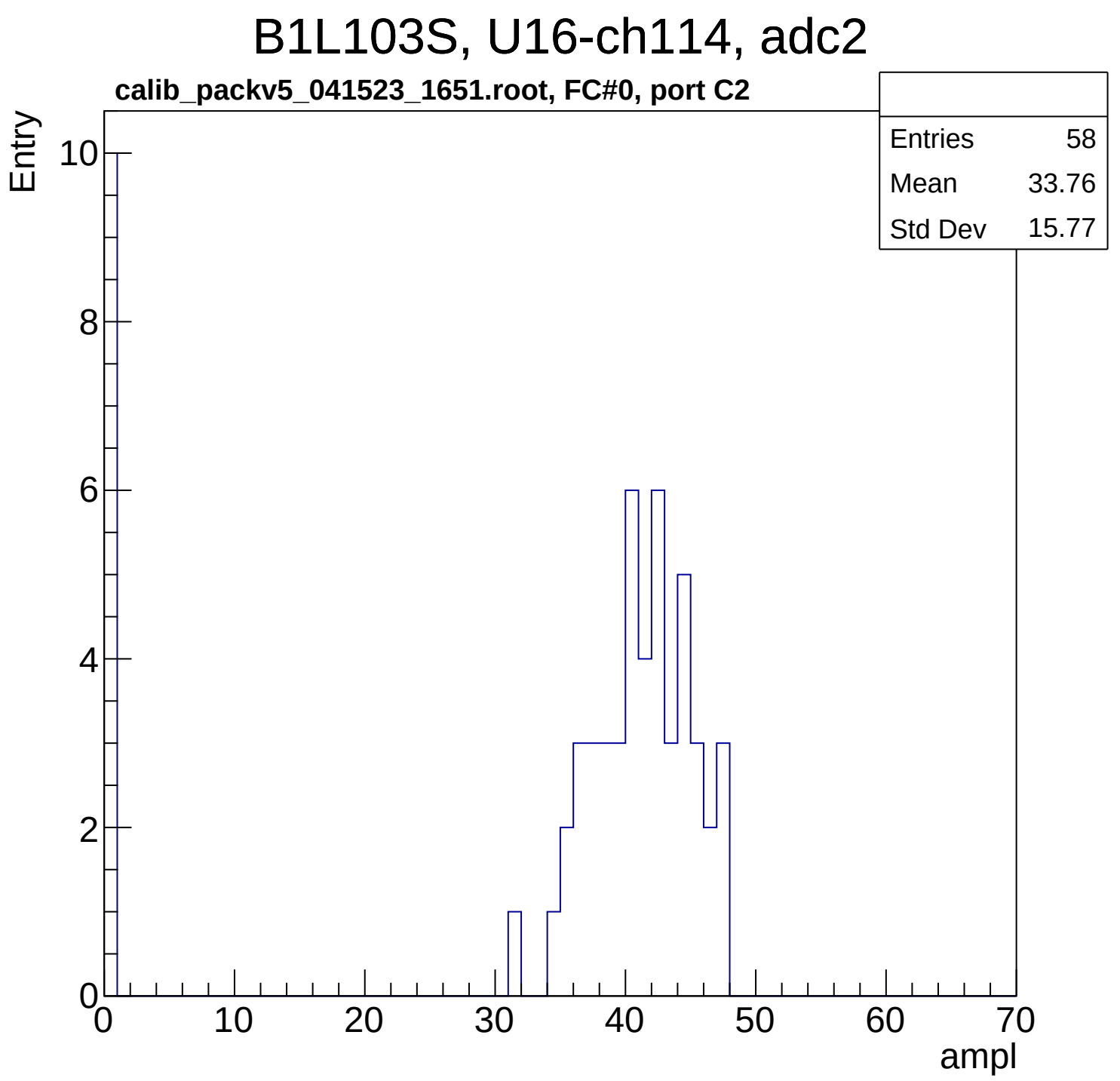
B1L103S, U16-ch114, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 33.76
Std Dev 15.77
Entry
0
2
4
6
8
10
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10
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30
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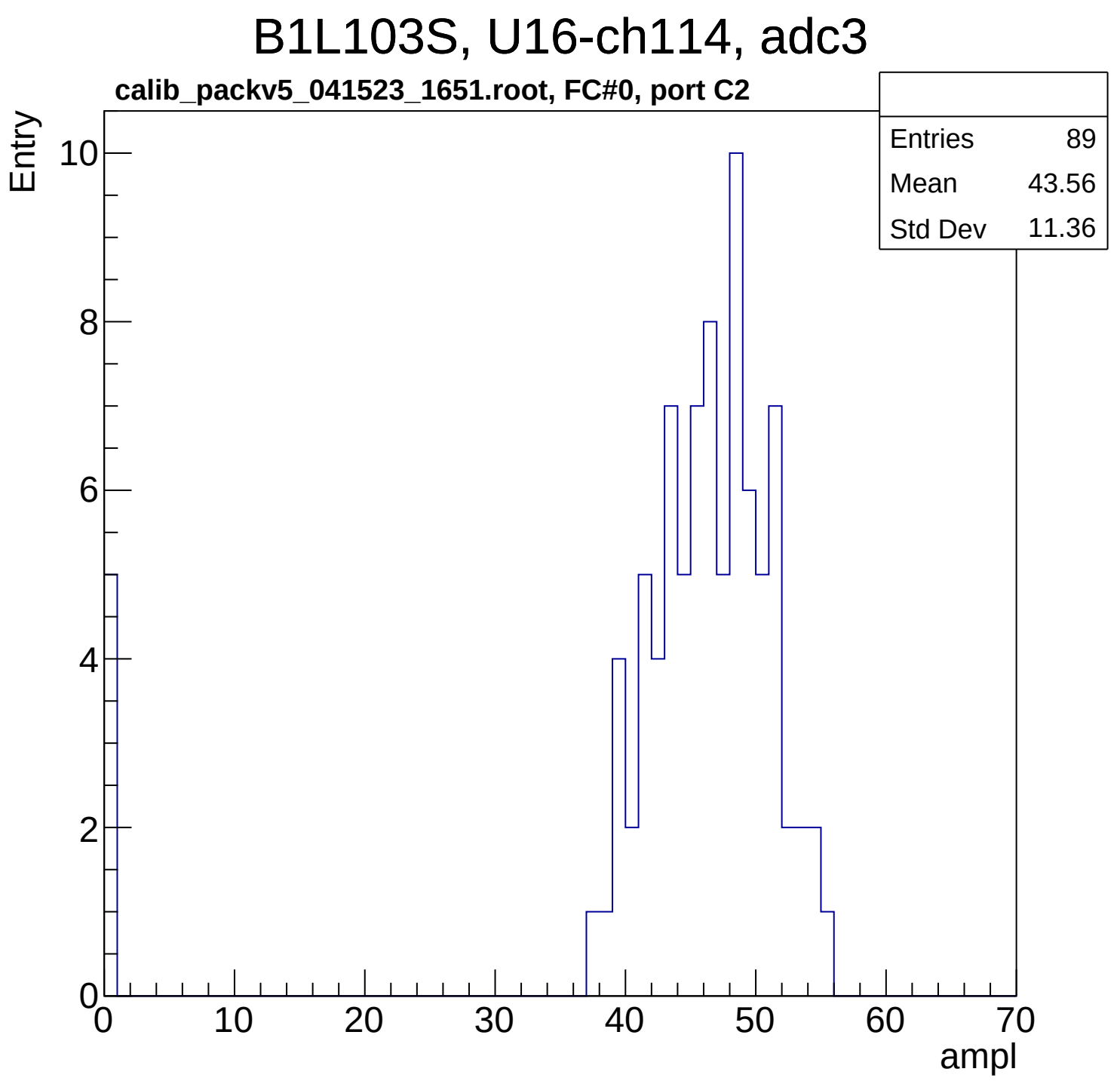
50
60
70
ampl


B1L103S, U16-ch114, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 43.56
Std Dev 11.36
Entry
ampl
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4
6
8
10
0
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20
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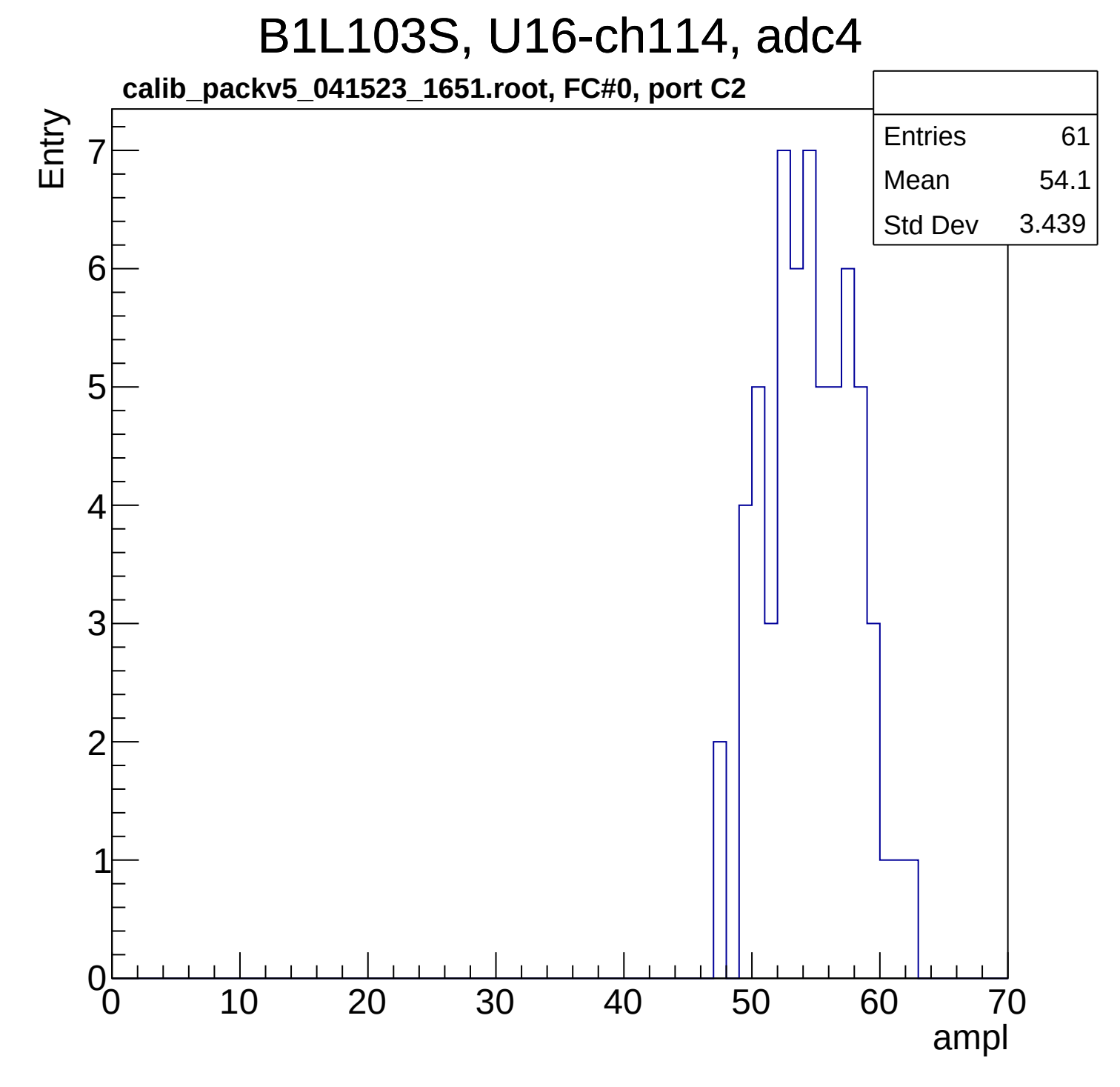
50
60
70


B1L103S, U16-ch114, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 54.1
Std Dev 3.439
Entry
ampl
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1
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4
5
6
7
0
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60
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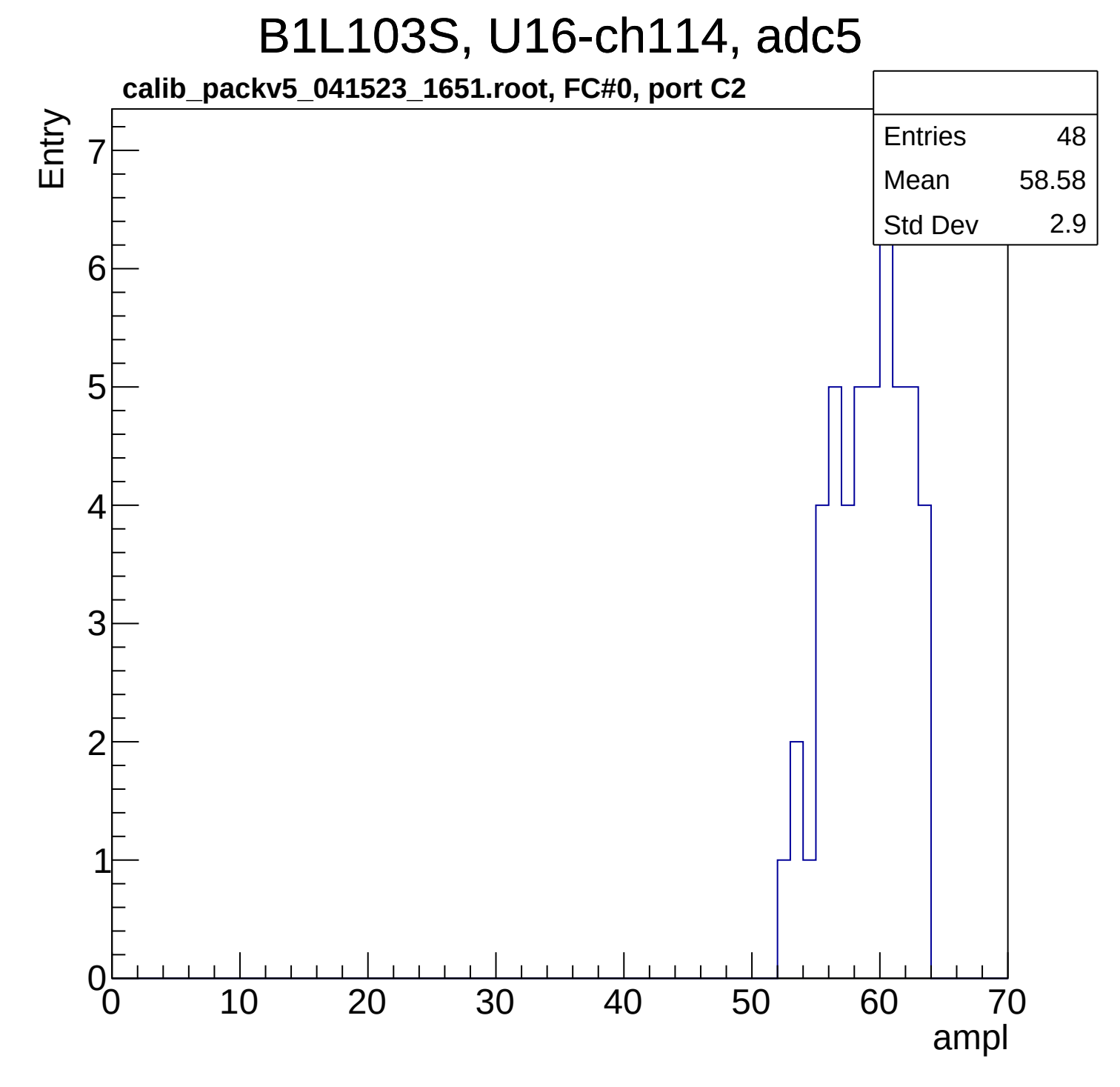
B1L103S, U16-ch114, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.58
Std Dev 2.9
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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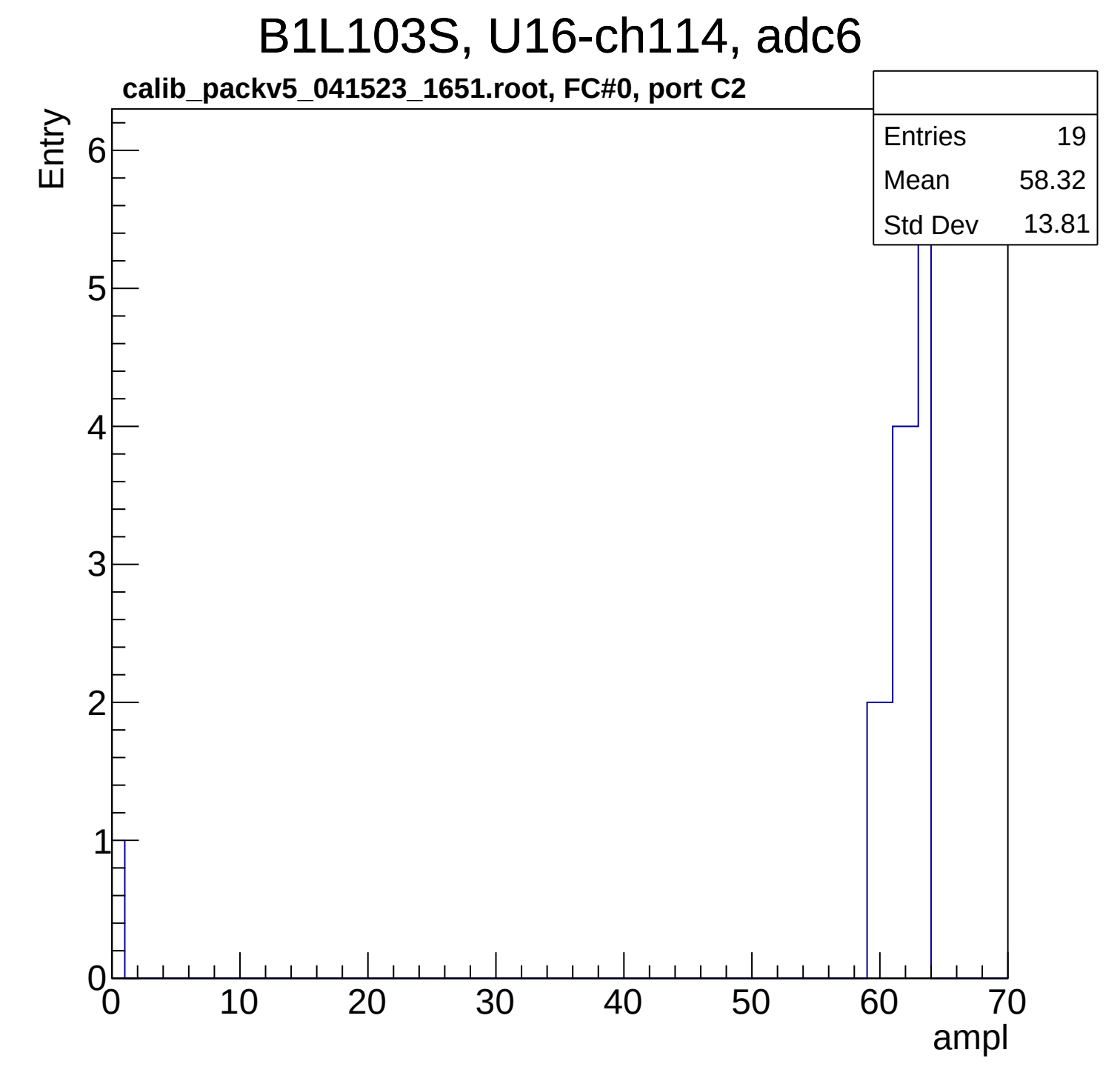
B1L103S, U16-ch114, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 58.32
Std Dev 13.81
Entry
ampl
0
1
2
3
4
5
6
0
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30
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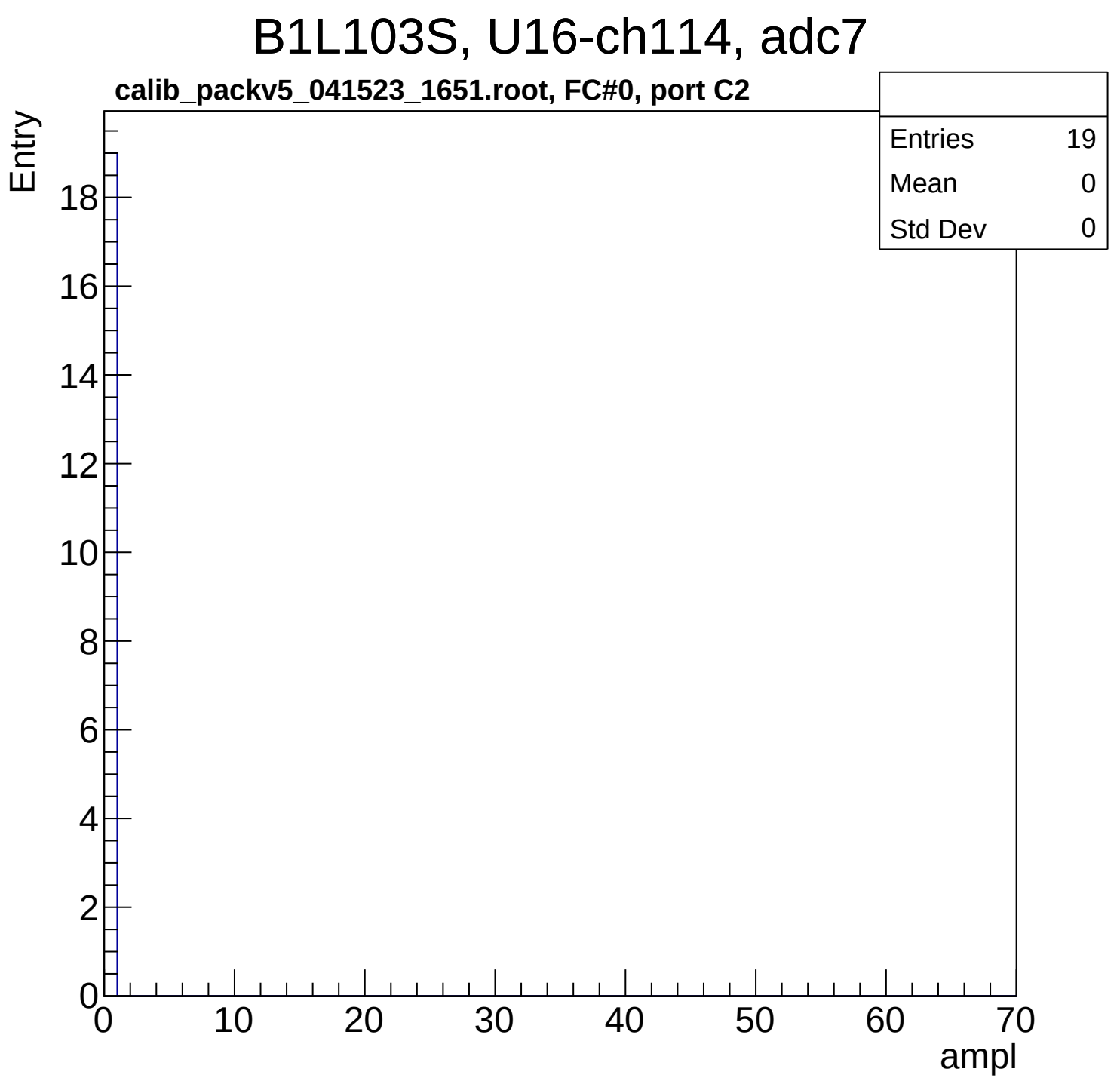
50
60
70


B1L103S, U16-ch114, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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10
20
30
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50
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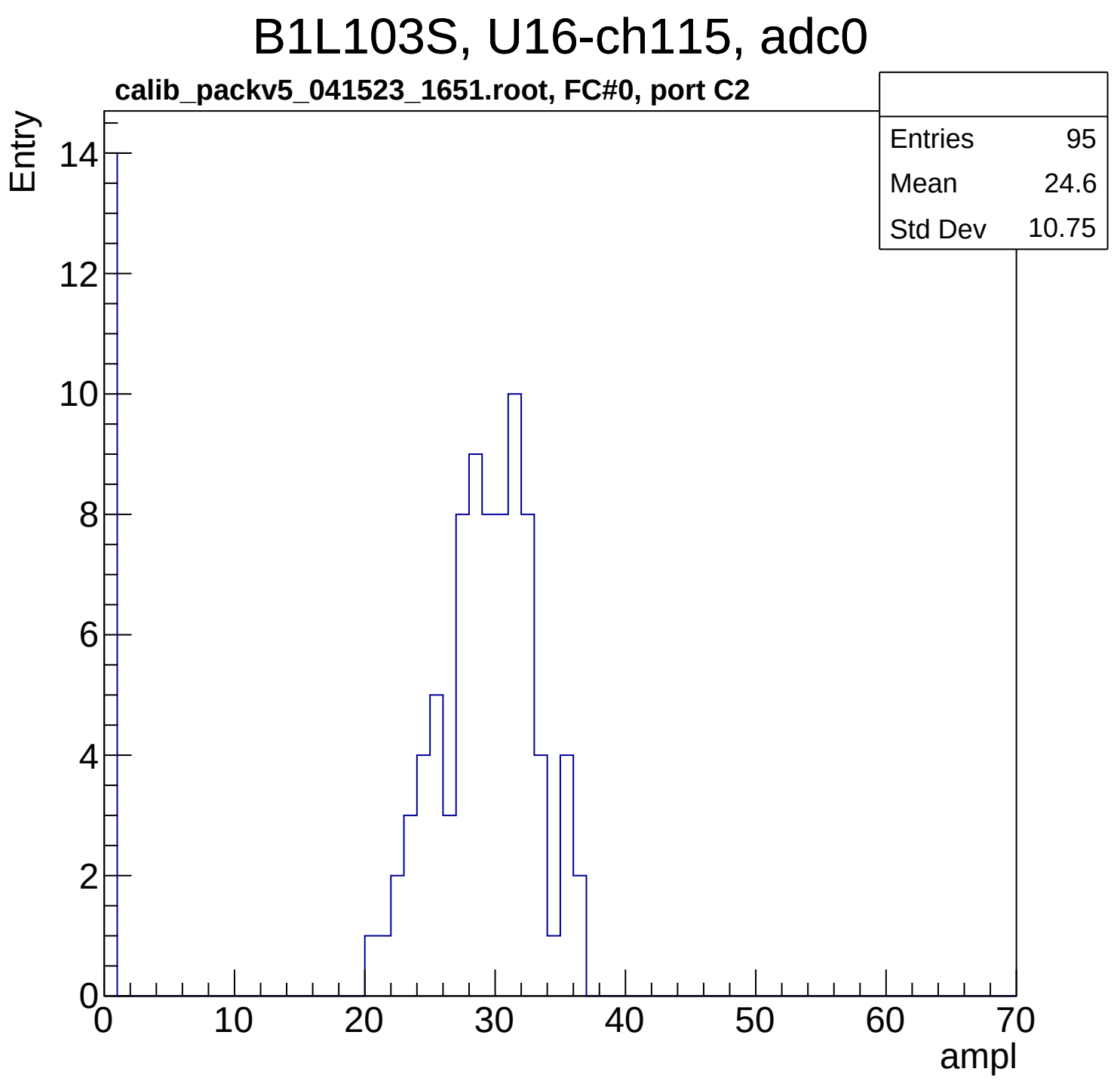
70
ampl


B1L103S, U16-ch115, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 24.6
Std Dev 10.75
Entry
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2
4
6
8
10
12
14
0
10
20
30
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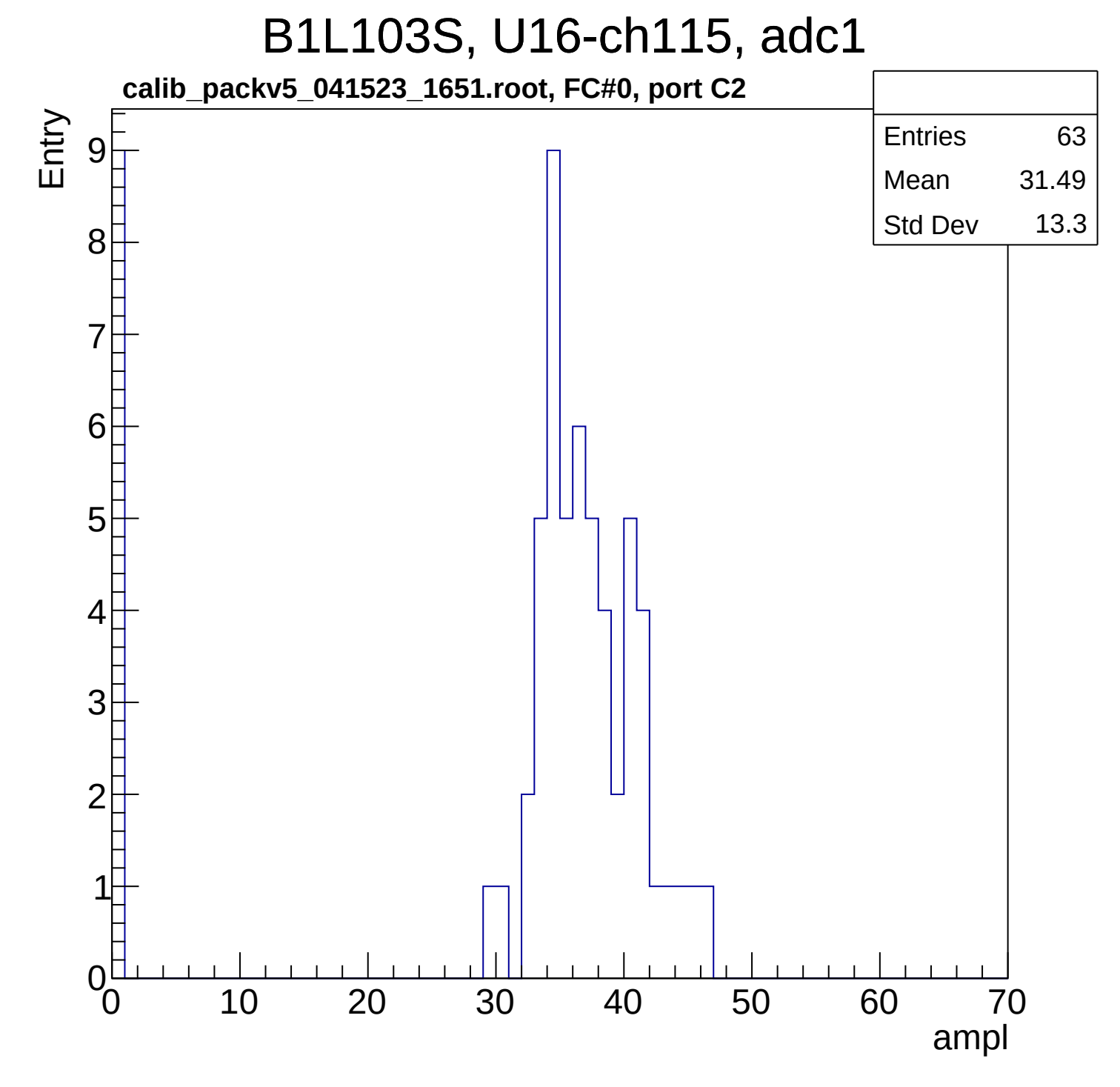
50
60
70
ampl


B1L103S, U16-ch115, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 31.49
Std Dev 13.3
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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40
50
60
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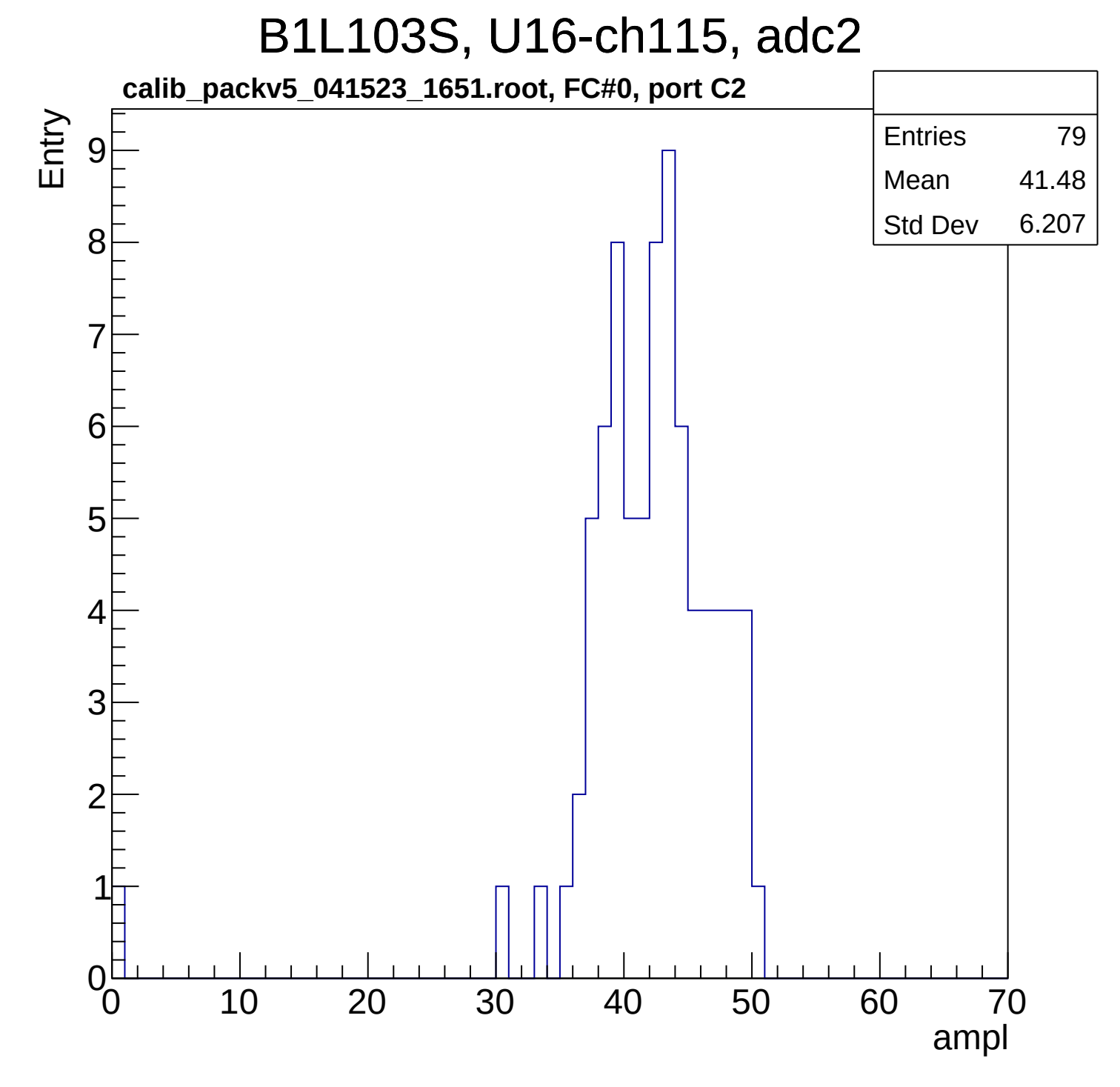
B1L103S, U16-ch115, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 41.48
Std Dev 6.207
Entry
ampl
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4
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6
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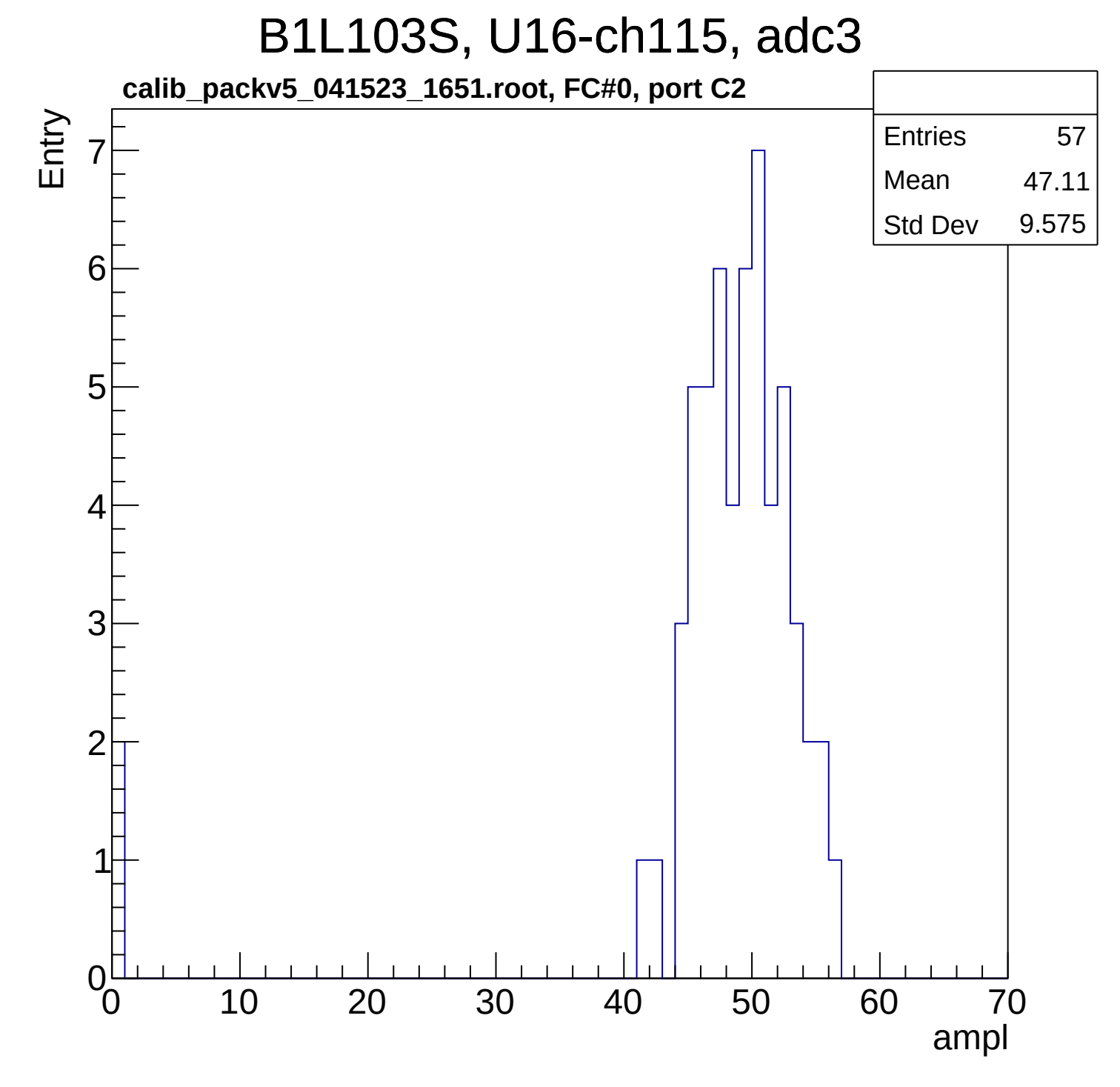
B1L103S, U16-ch115, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 47.11
Std Dev 9.575
Entry
ampl
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4
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6
7
0
10
20
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40
50
60
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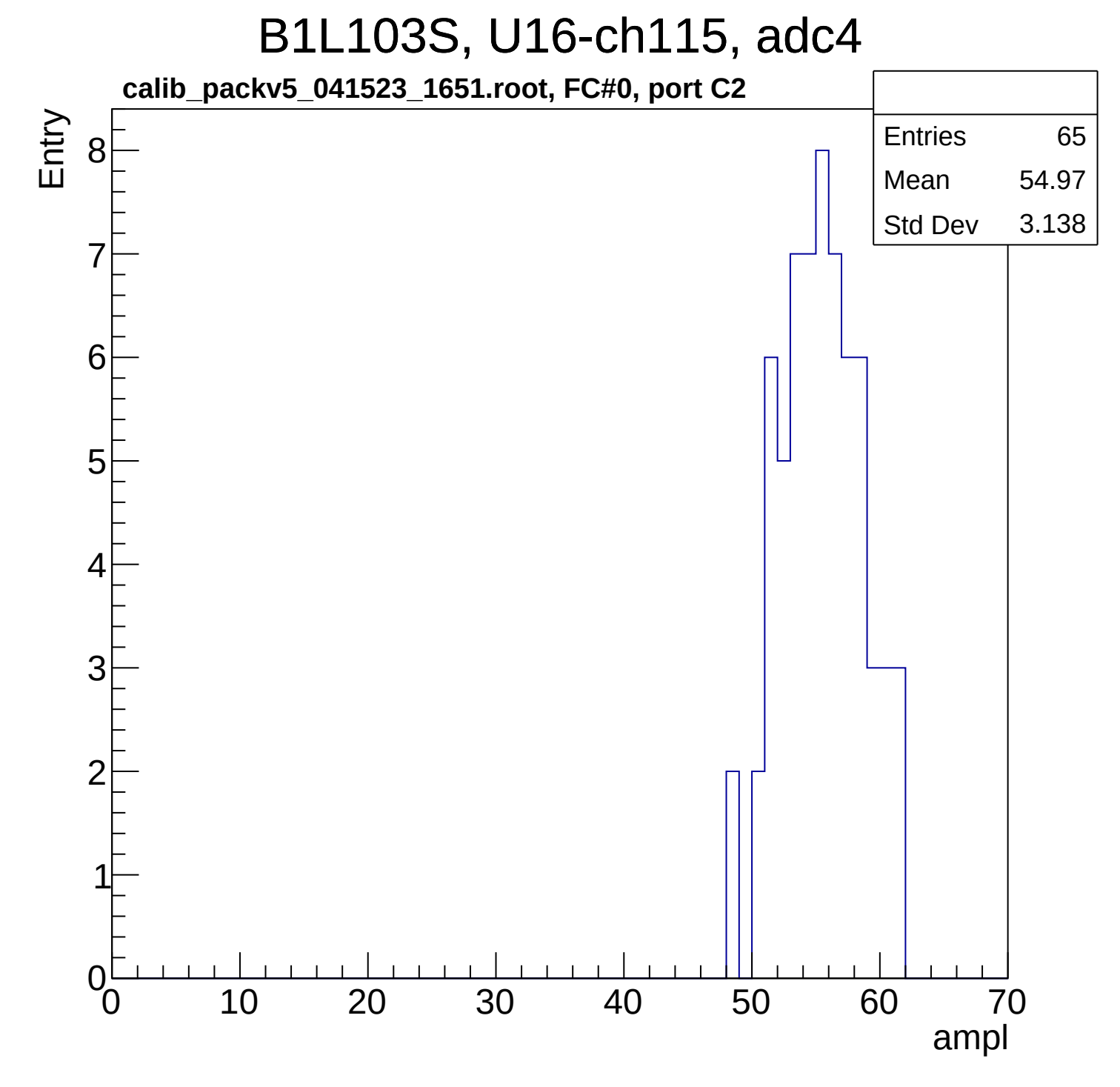
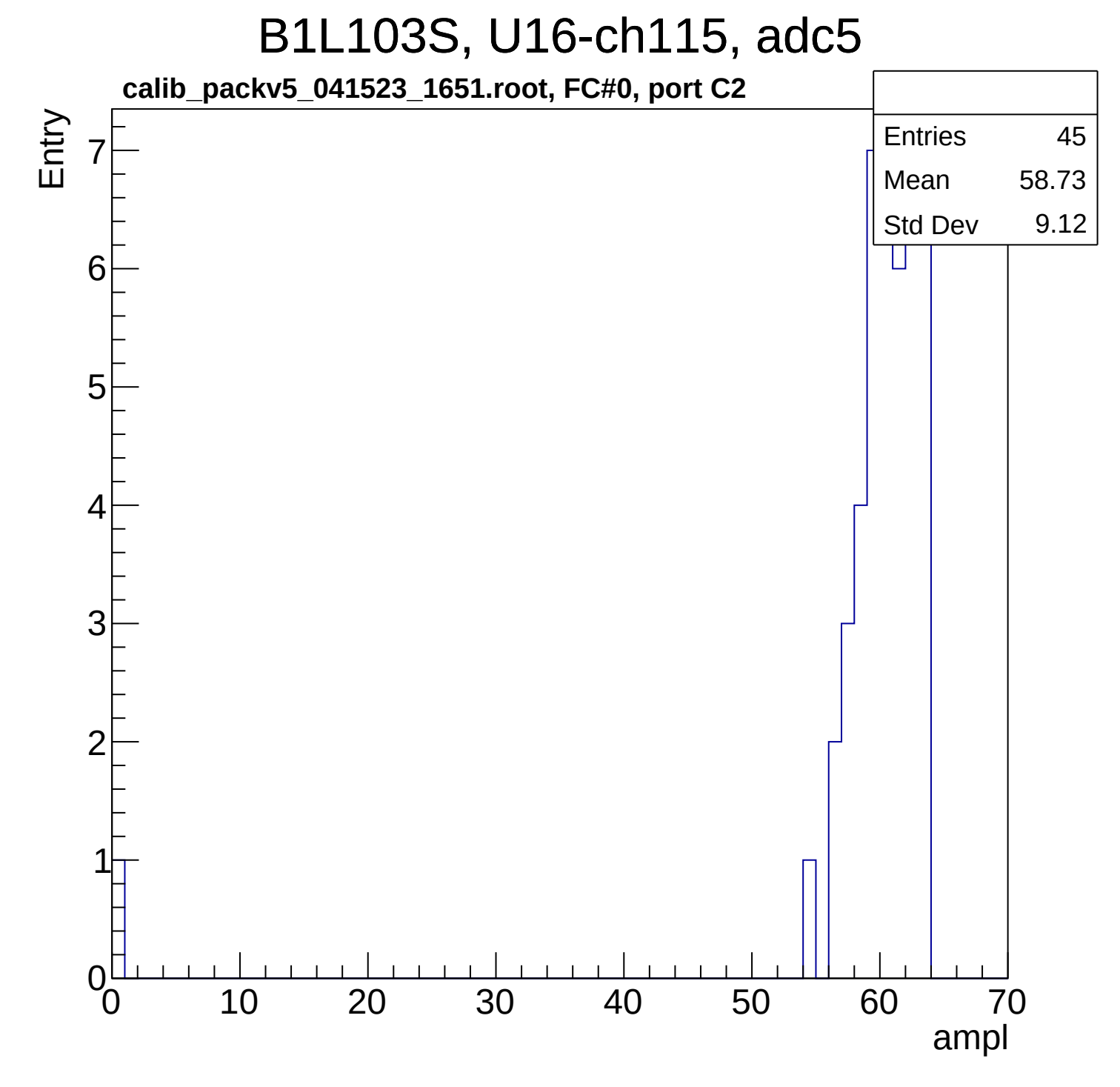

B1L103S, U16-ch115, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 54.97
Std Dev 3.138
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch115, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.73
Std Dev 9.12
Entry
ampl
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0
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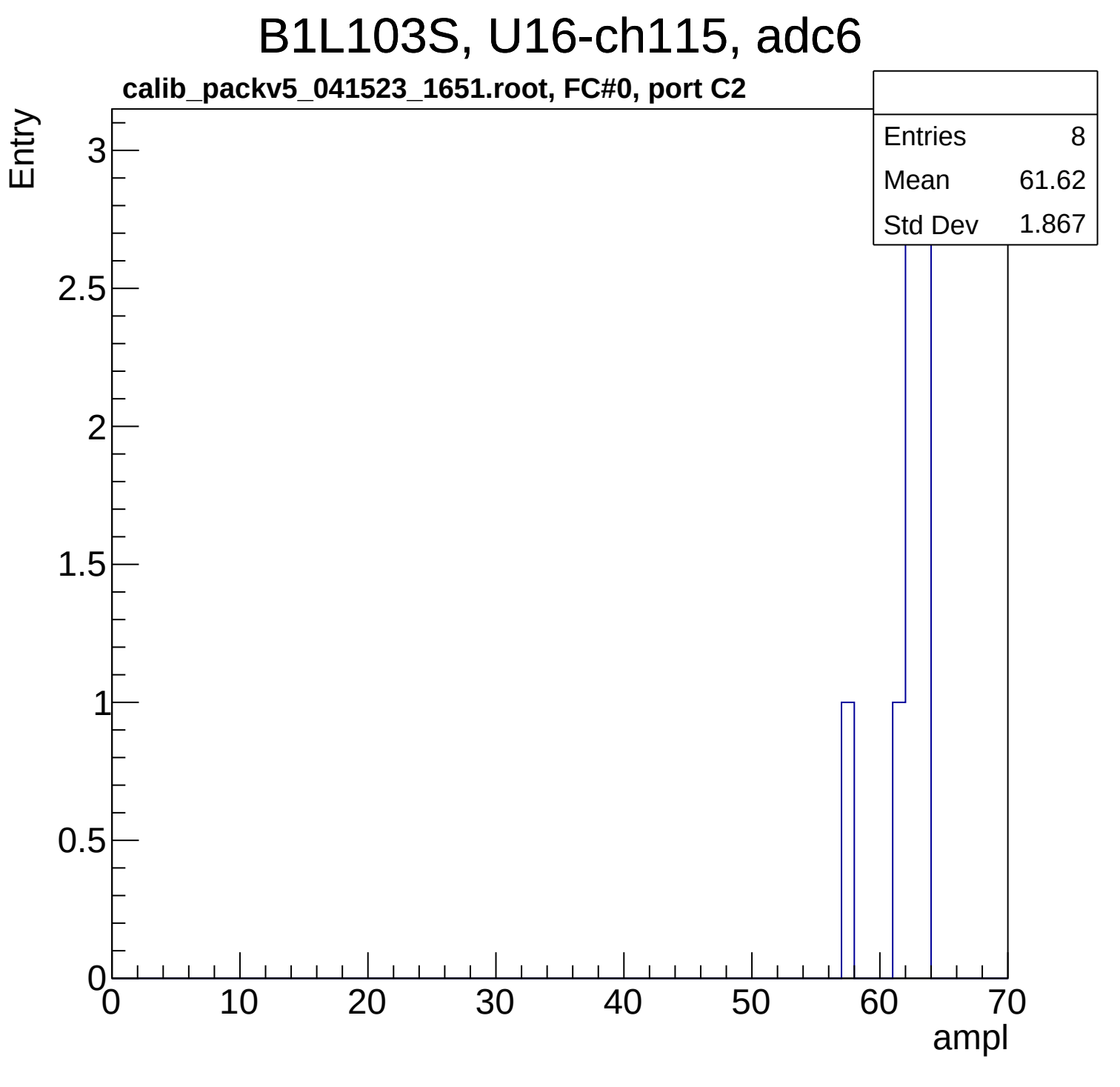
B1L103S, U16-ch115, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.62
Std Dev 1.867
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
50
60
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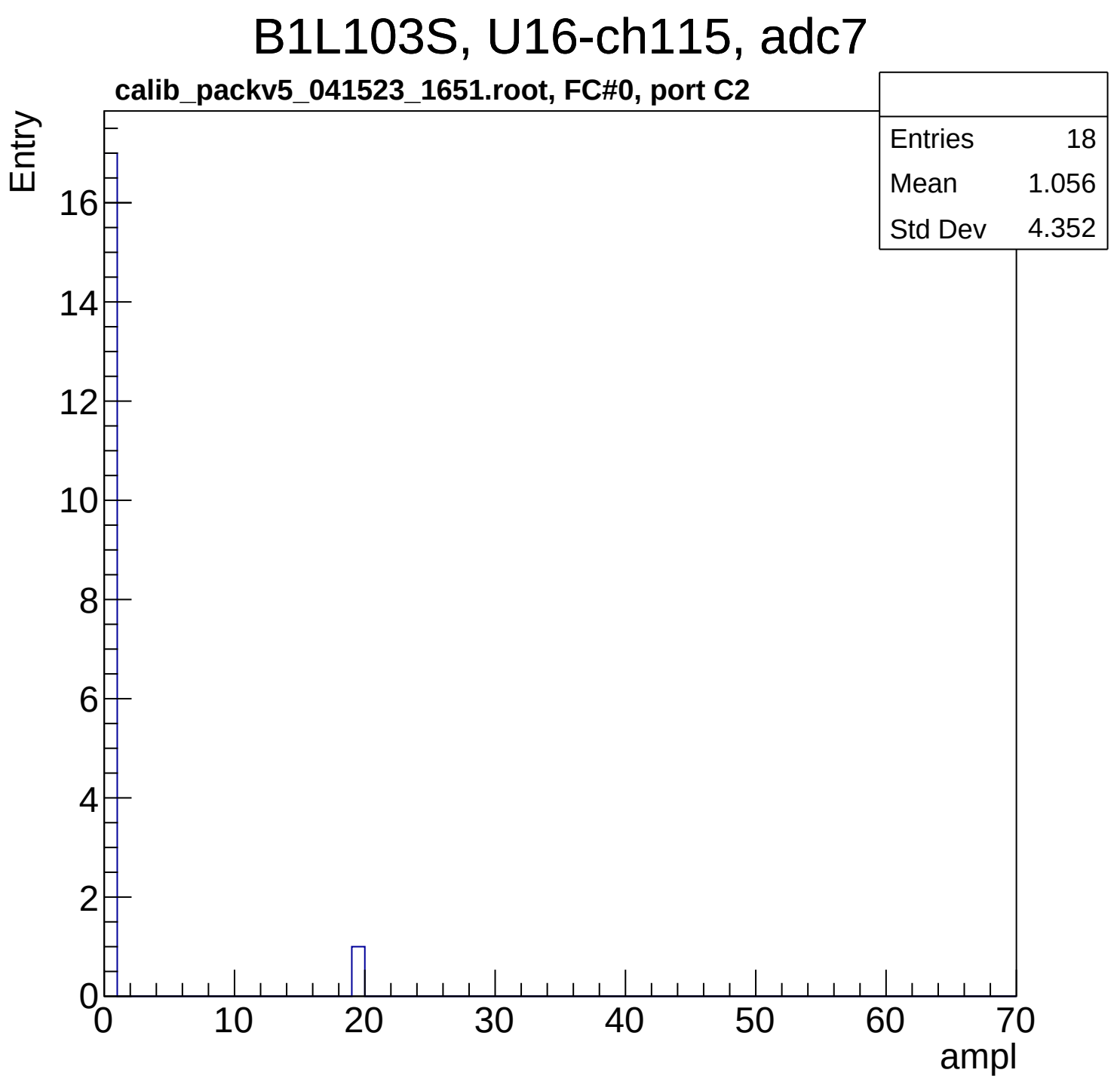
B1L103S, U16-ch115, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.056
Std Dev 4.352
Entry
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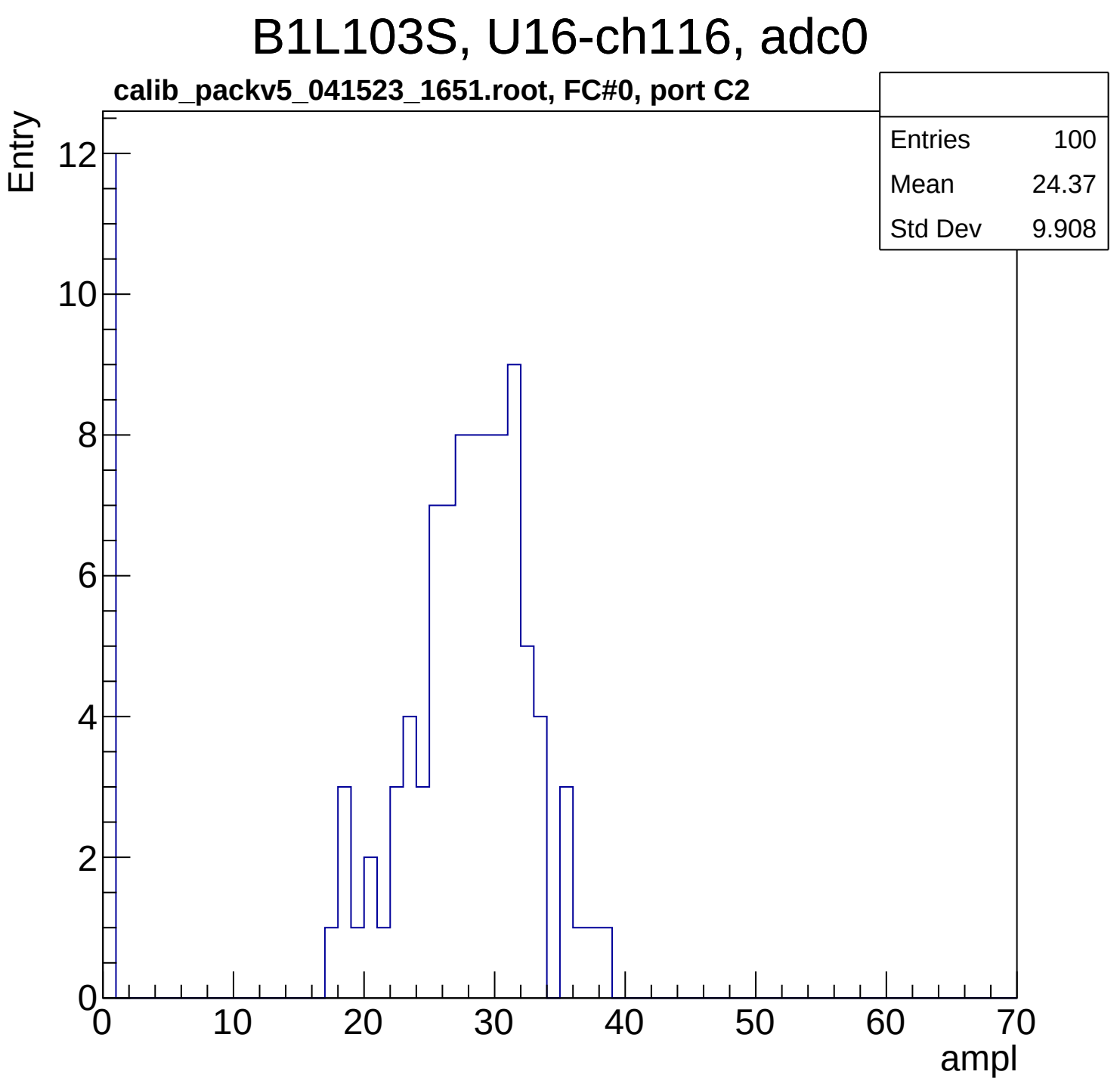
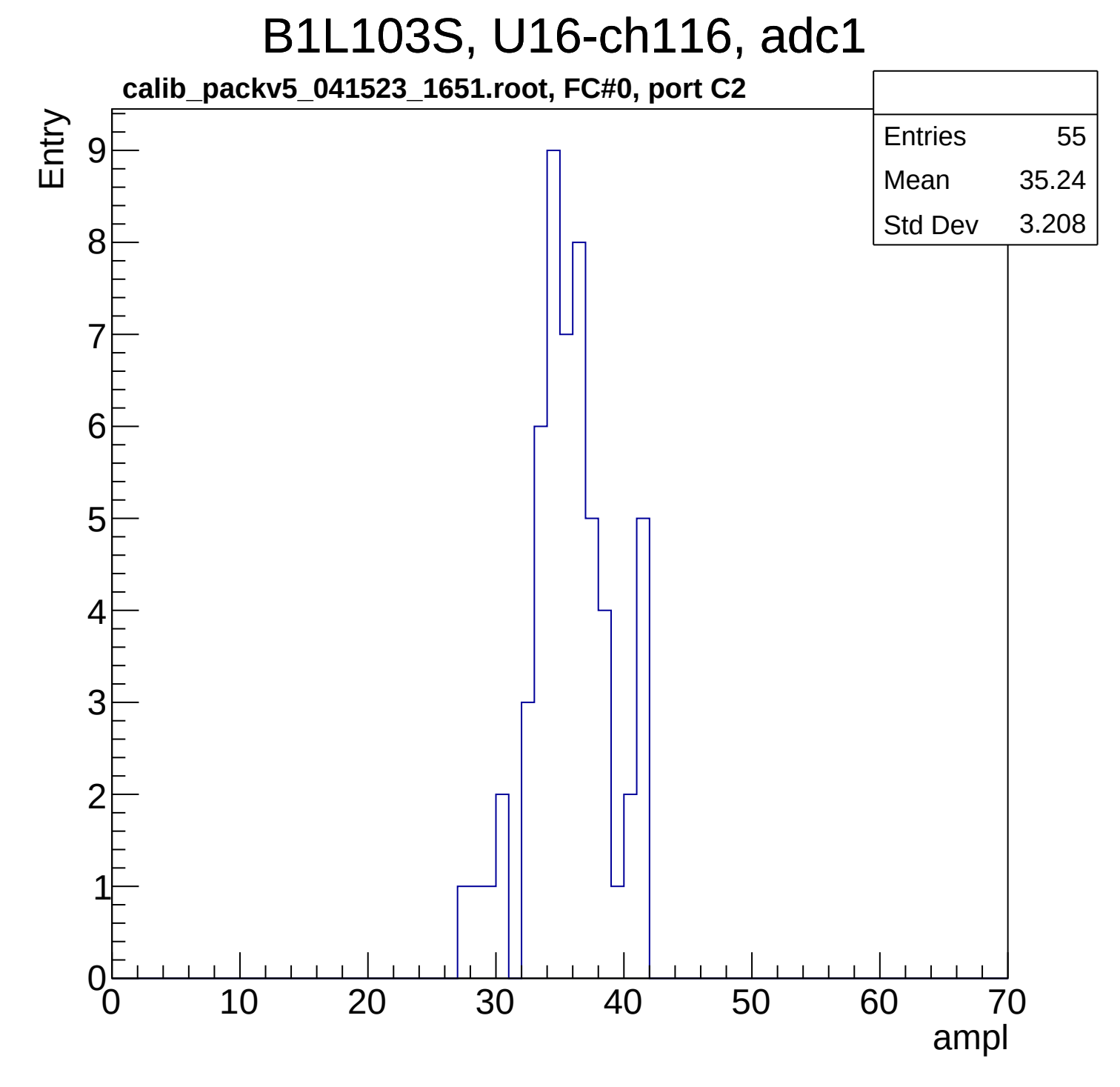
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch116, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 24.37
Std Dev 9.908
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch116, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 35.24
Std Dev 3.208
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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30
40
50
60
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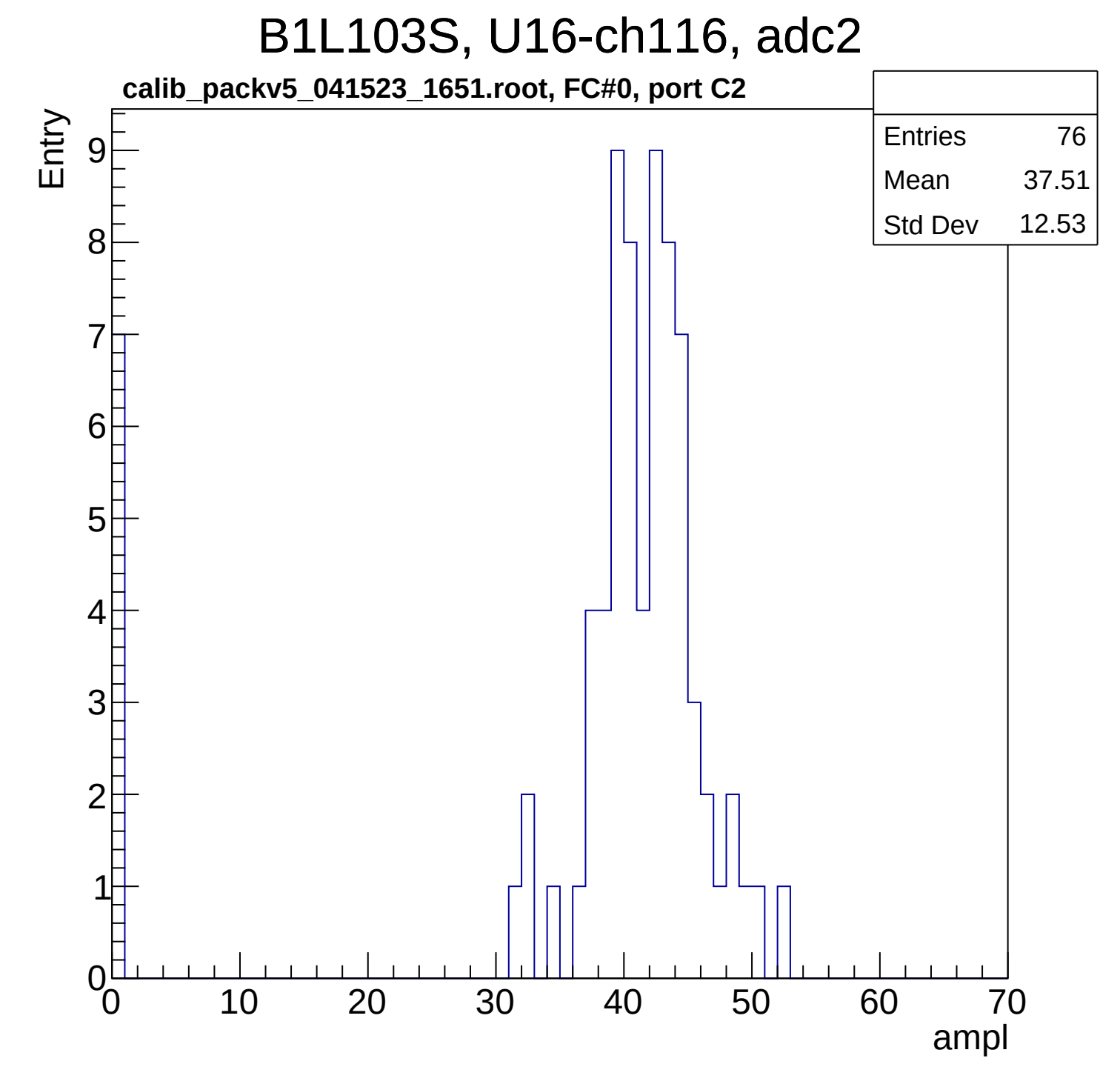
B1L103S, U16-ch116, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 37.51
Std Dev 12.53
Entry
ampl
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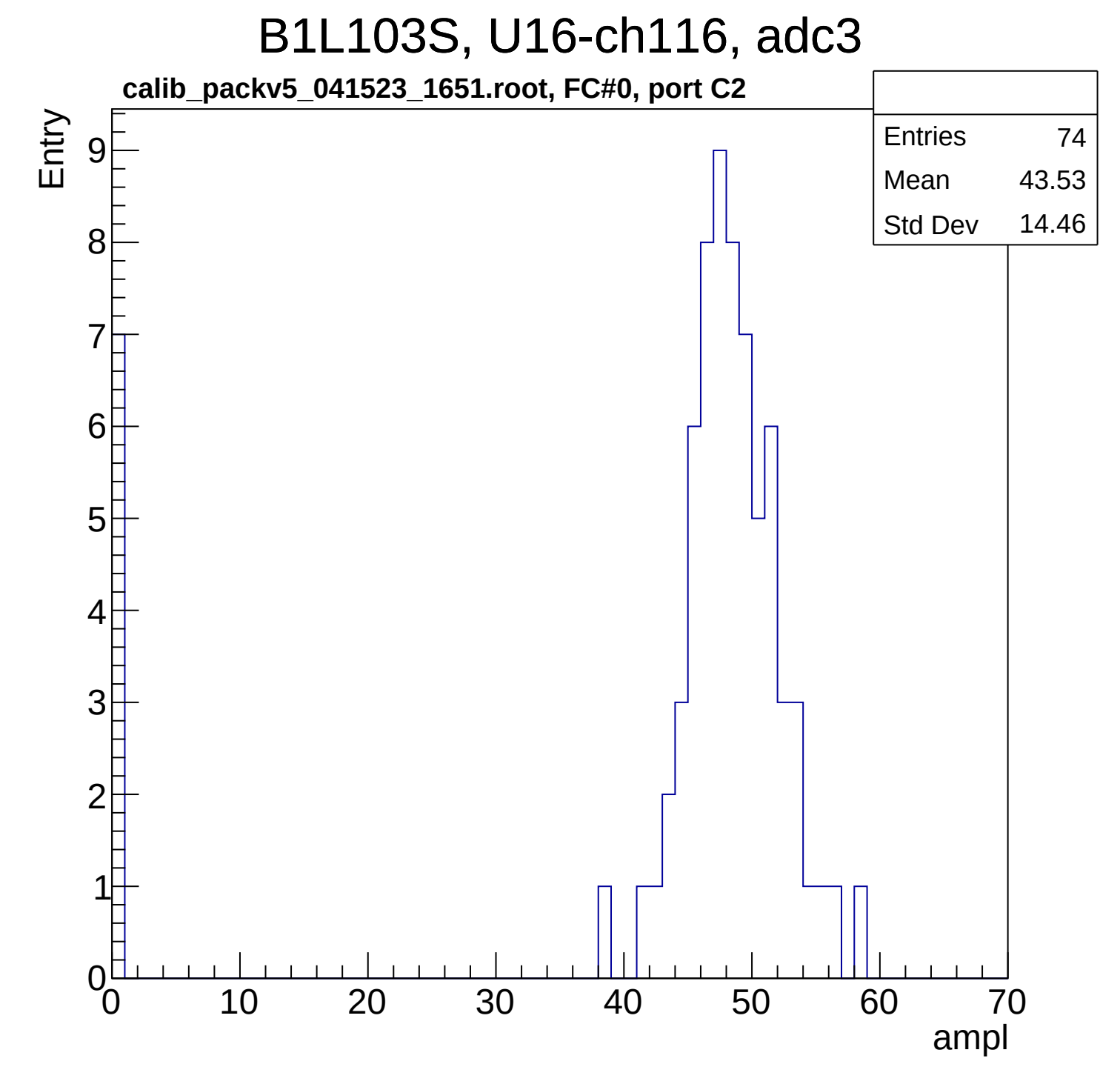
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch116, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 43.53
Std Dev 14.46
Entry
ampl
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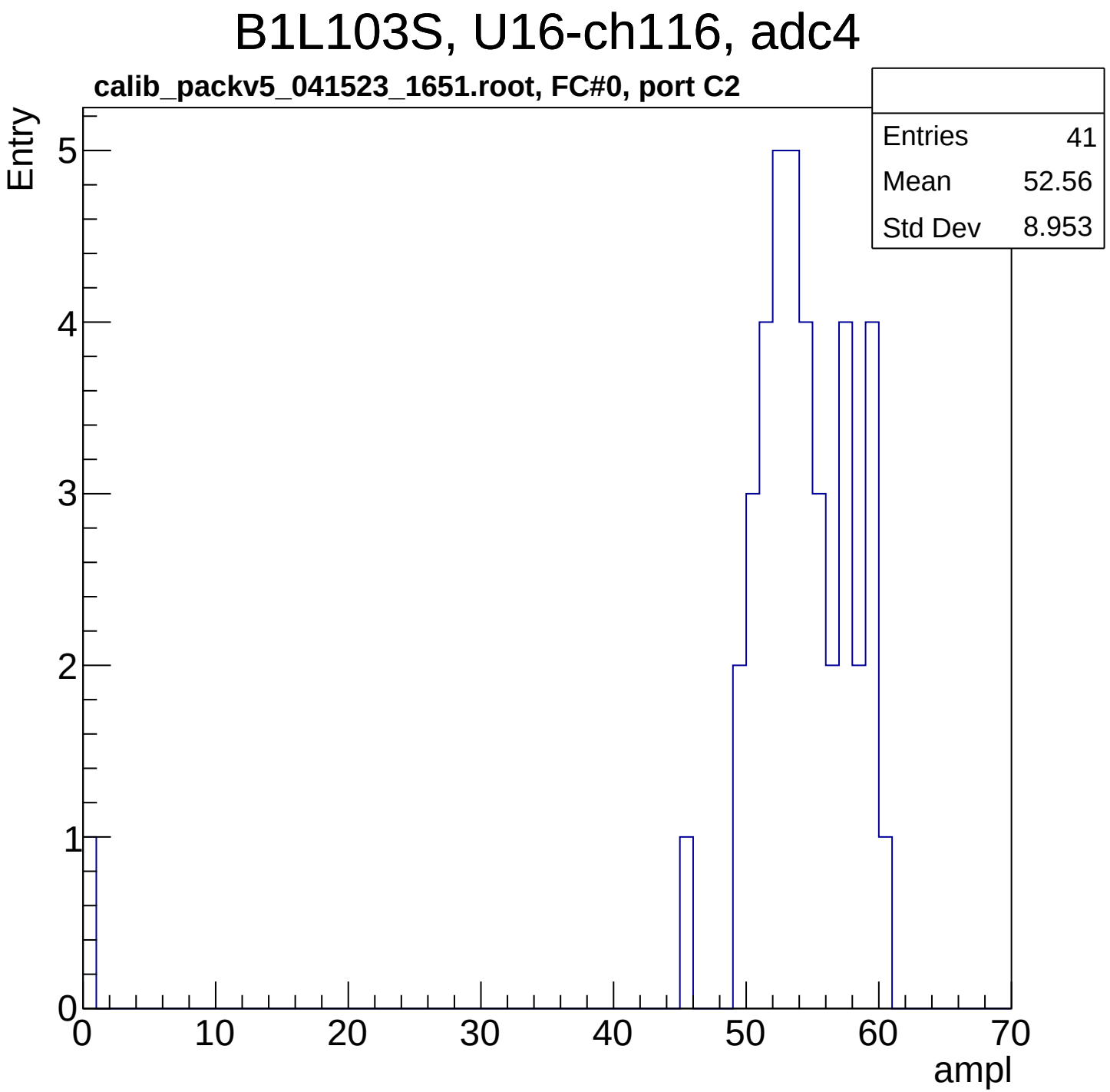
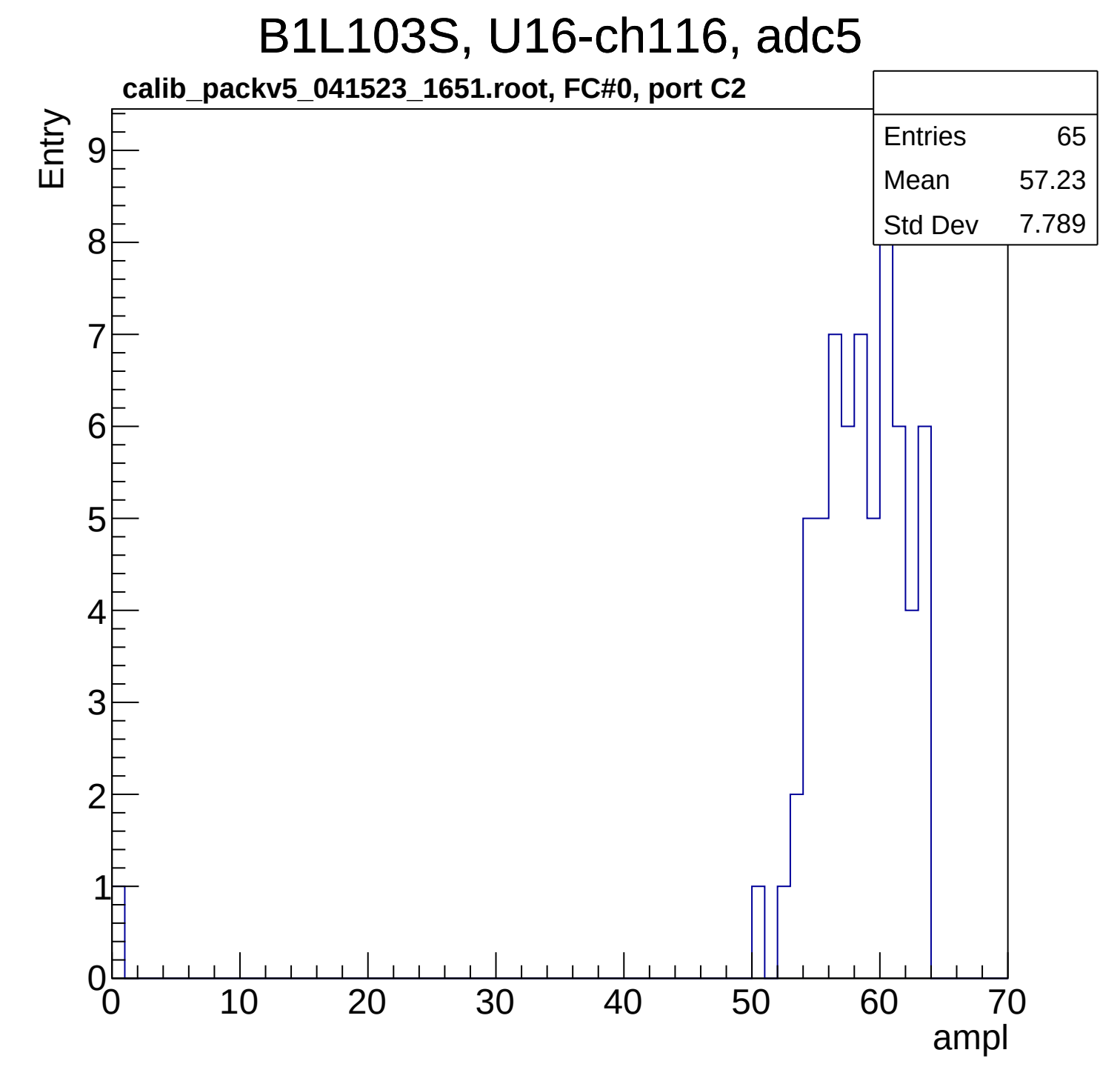
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch116, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 52.56
Std Dev 8.953
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch116, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 57.23
Std Dev 7.789
Entry
ampl
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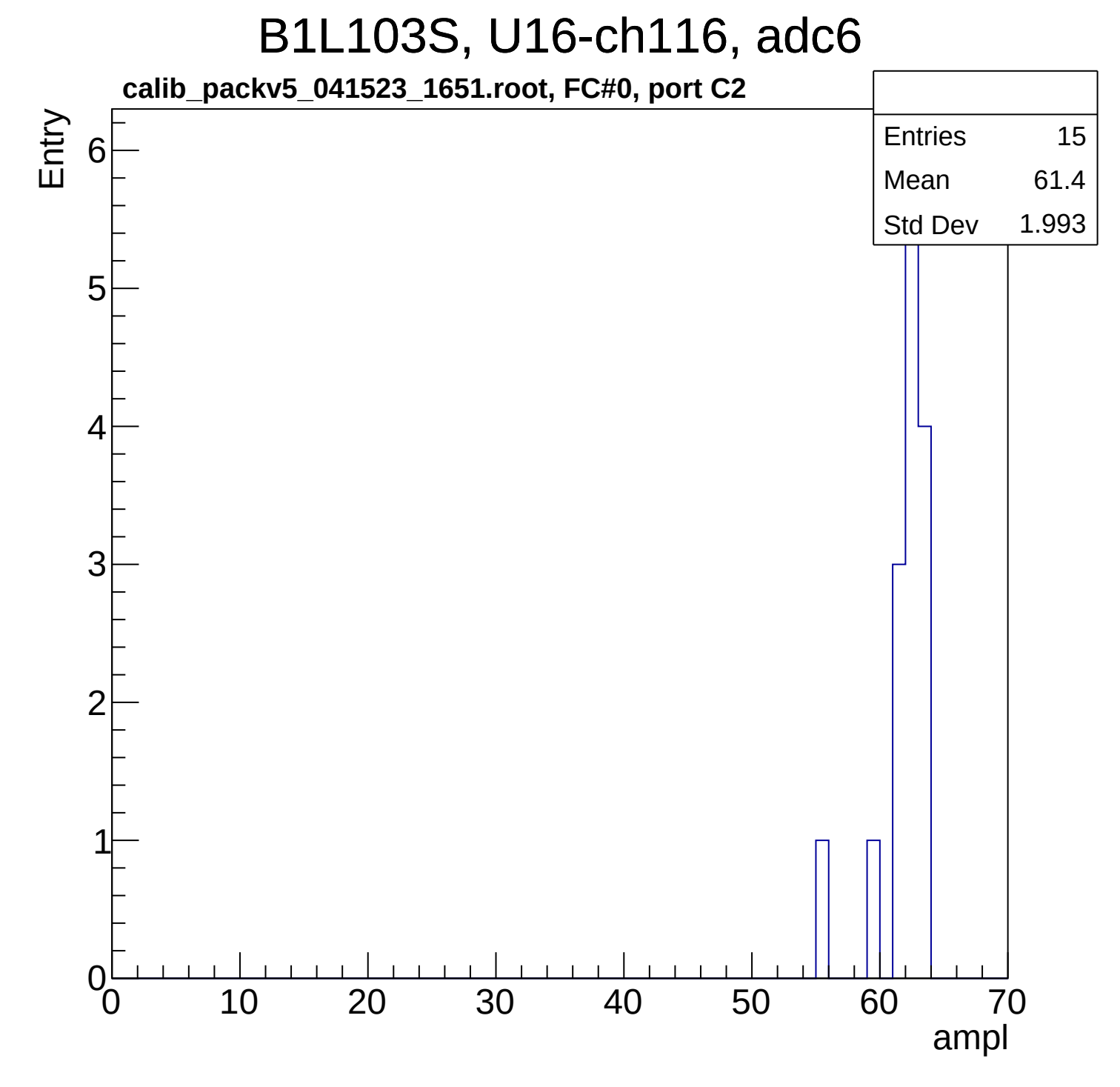
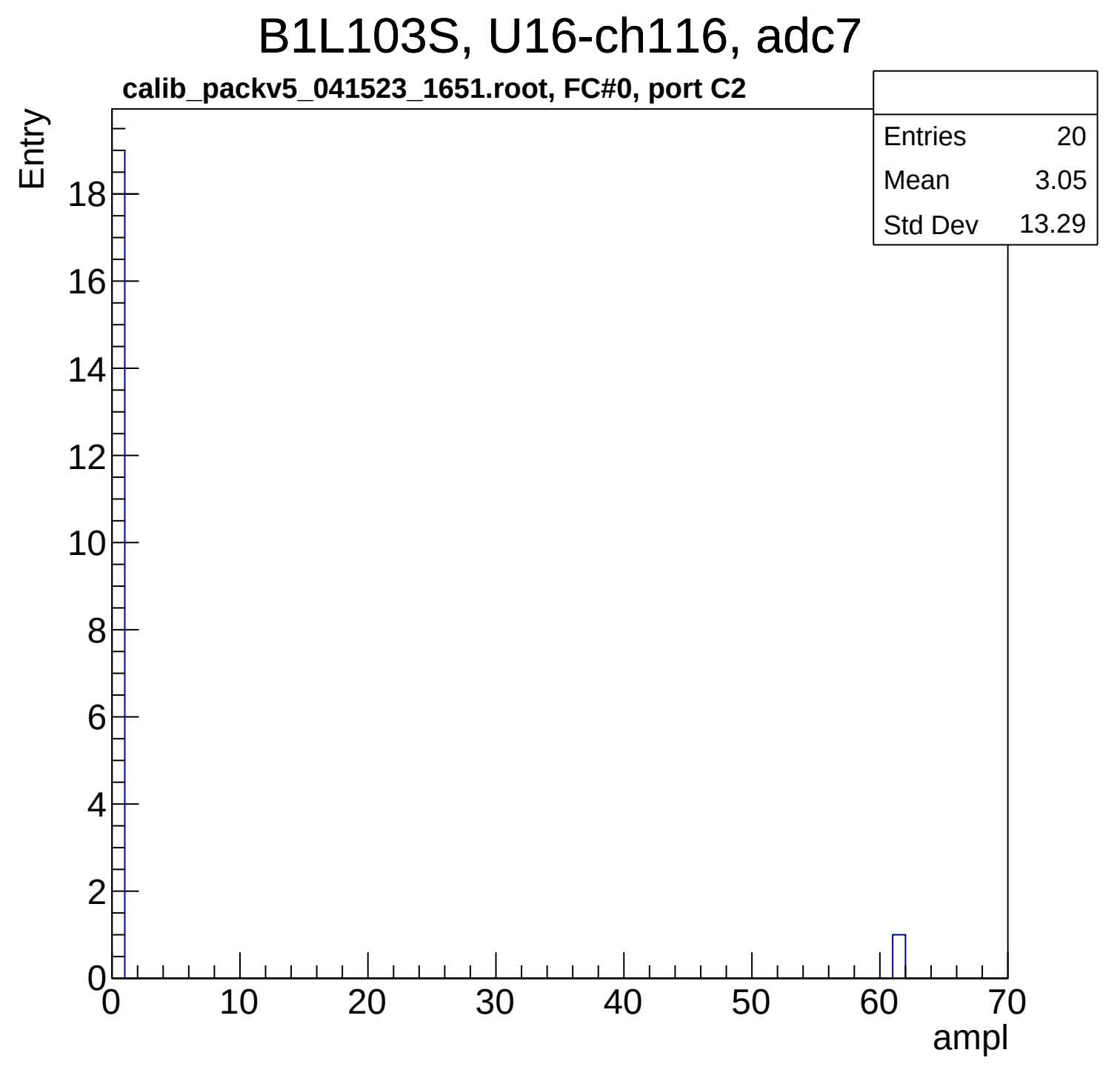
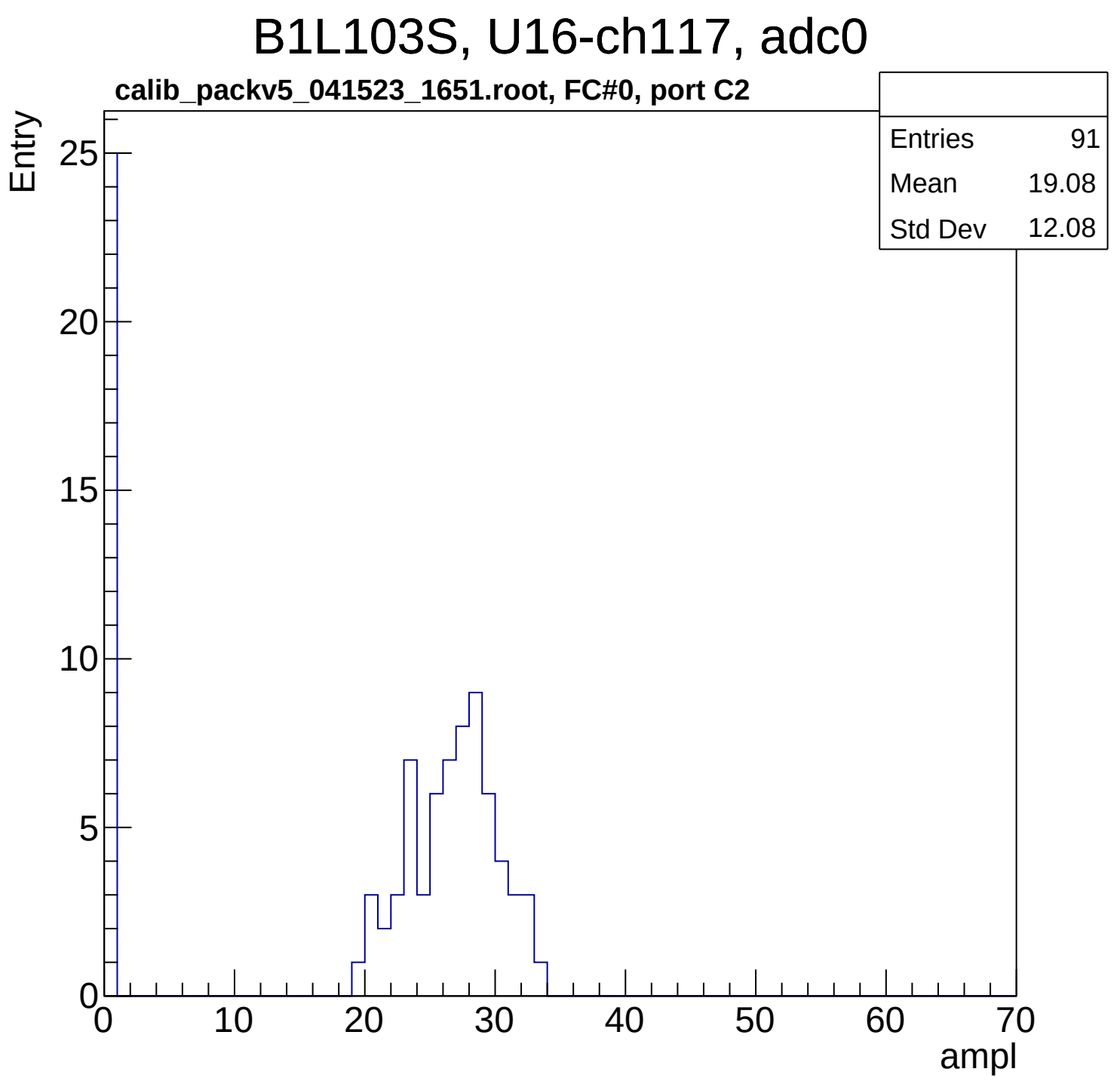
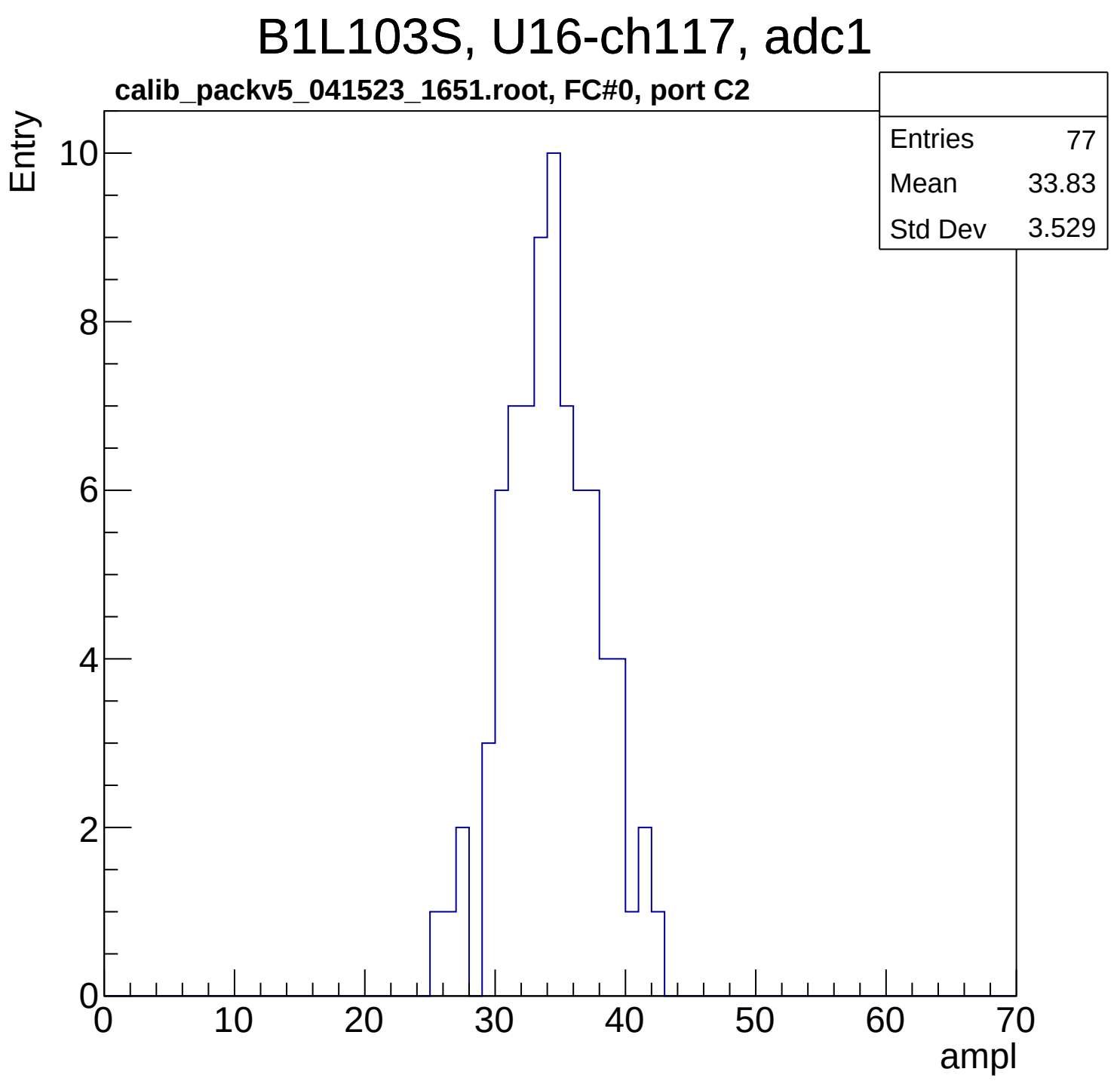
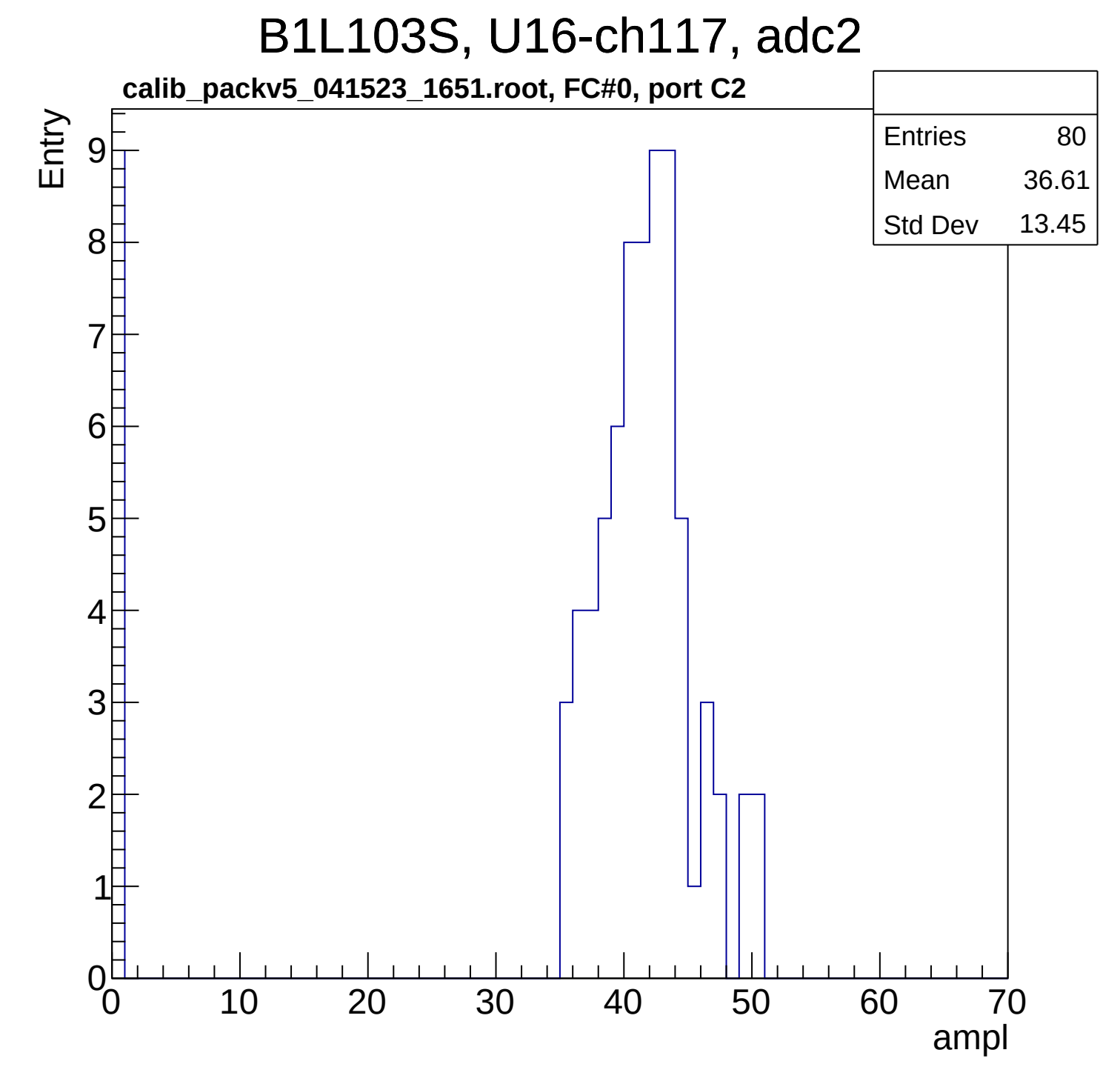
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

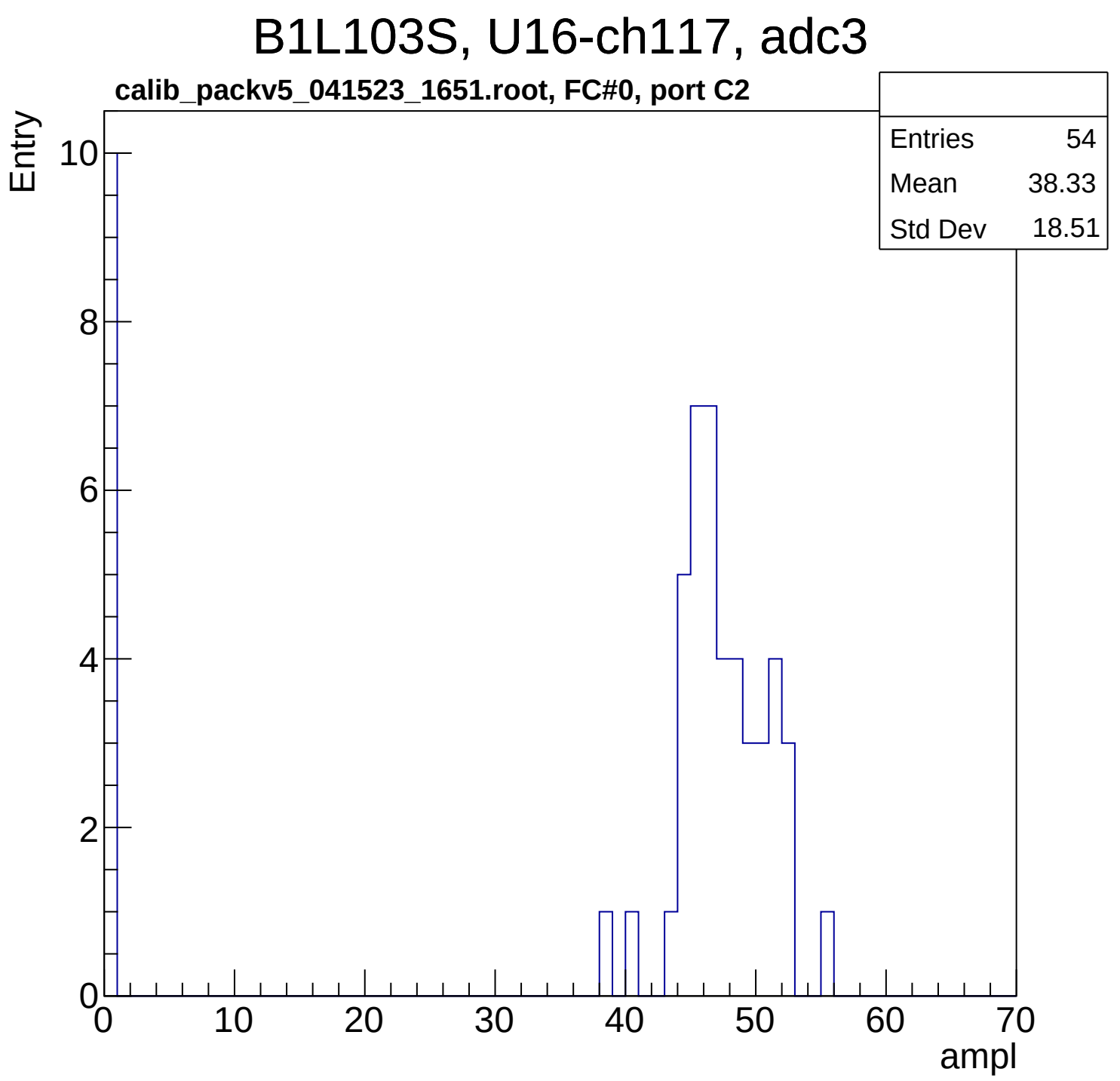

B1L103S, U16-ch116, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.4
Std Dev 1.993
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

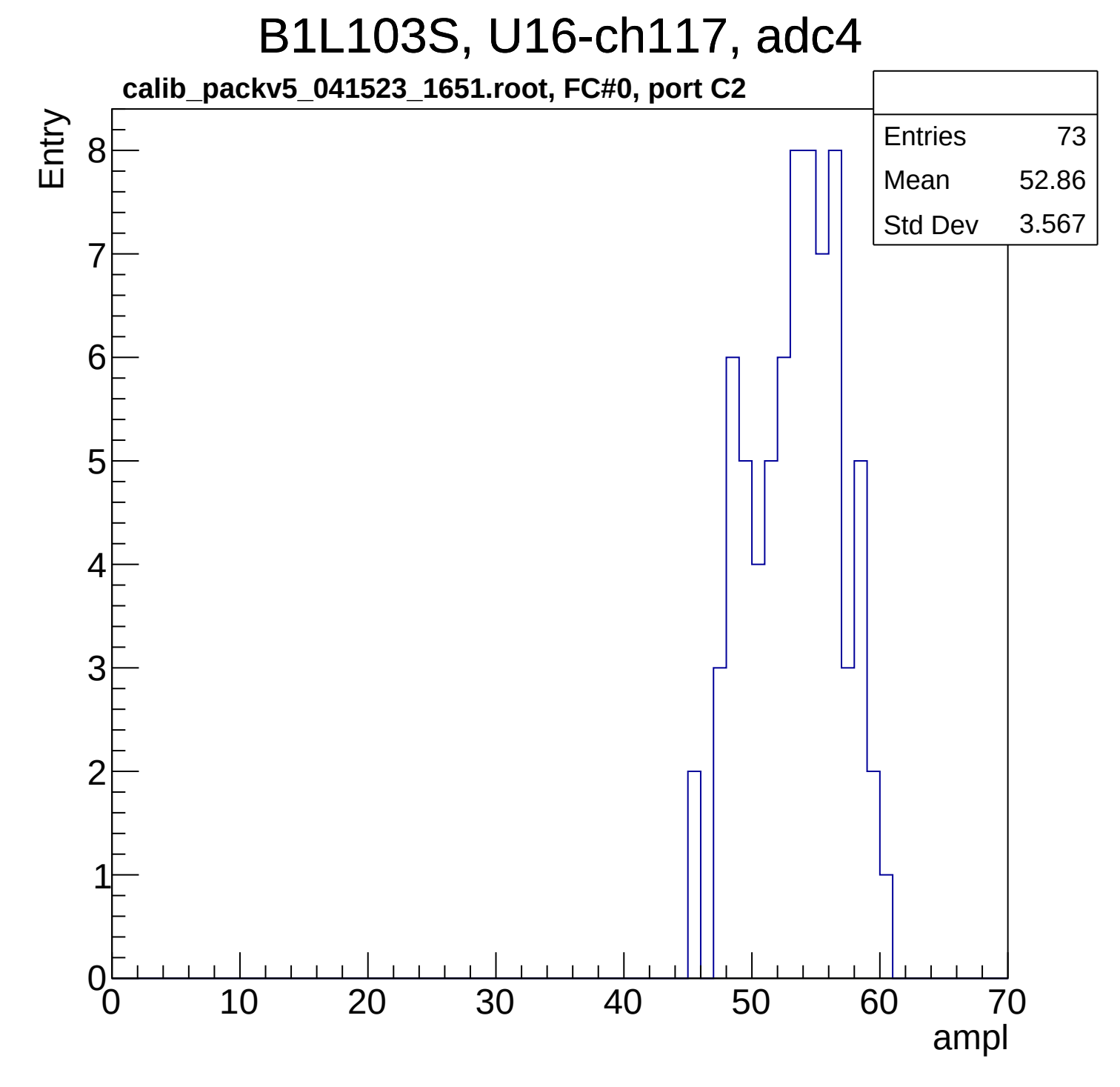

B1L103S, U16-ch116, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch117, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 19.08
Std Dev 12.08
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch117, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 33.83
Std Dev 3.529
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch117, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 36.61
Std Dev 13.45
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch117, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 38.33
Std Dev 18.51
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch117, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 52.86
Std Dev 3.567
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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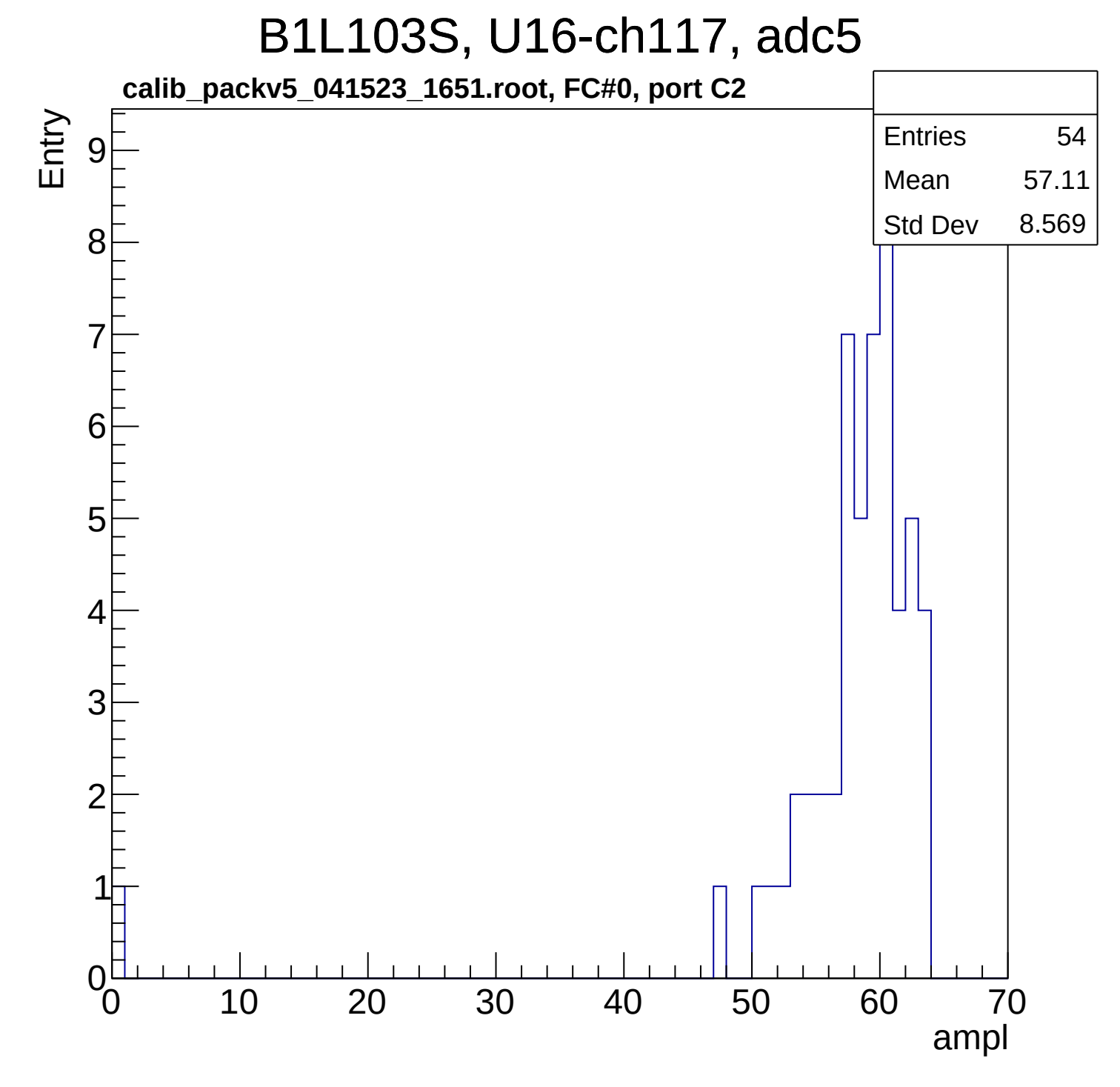
B1L103S, U16-ch117, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.11
Std Dev 8.569
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
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60
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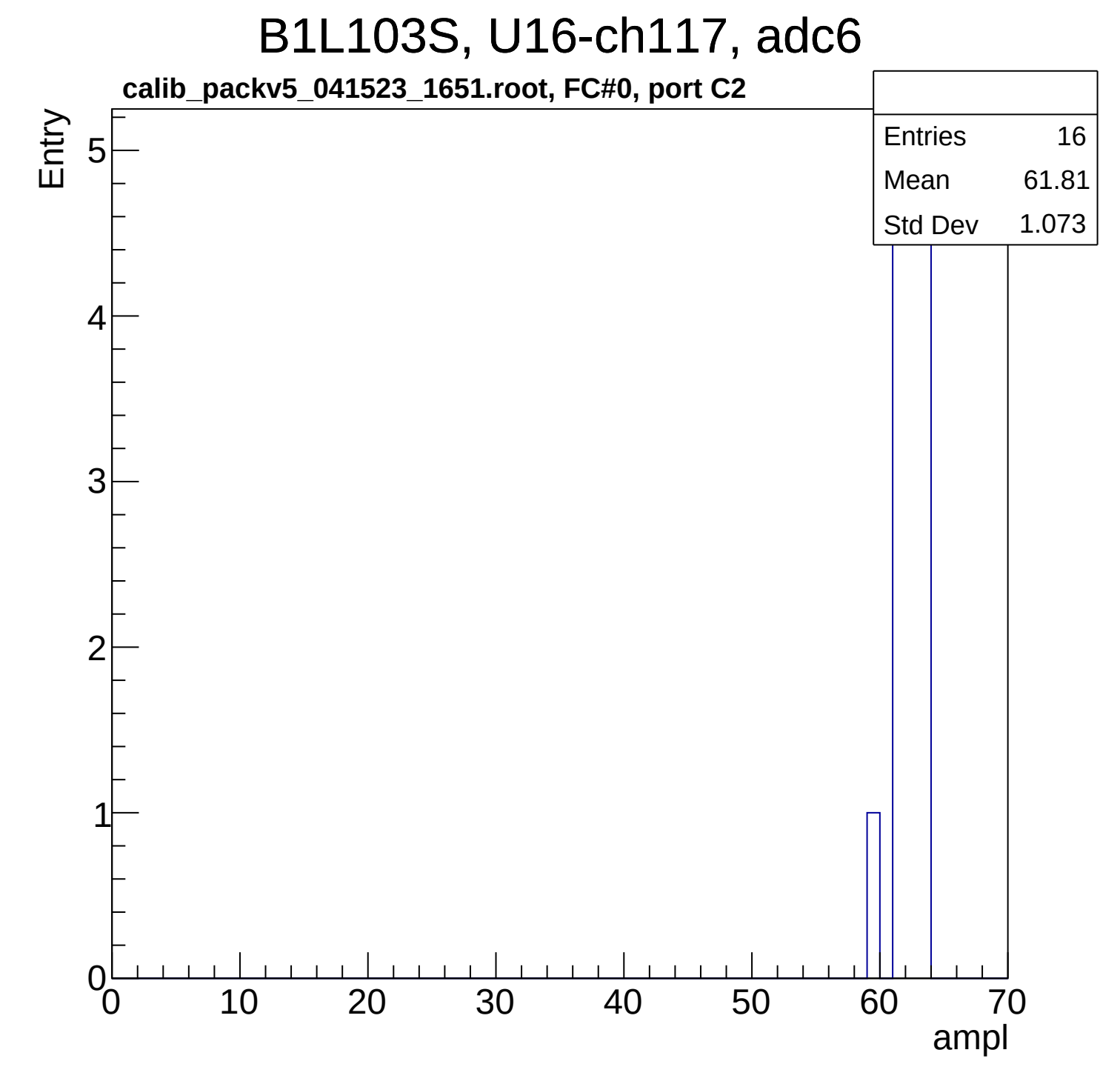
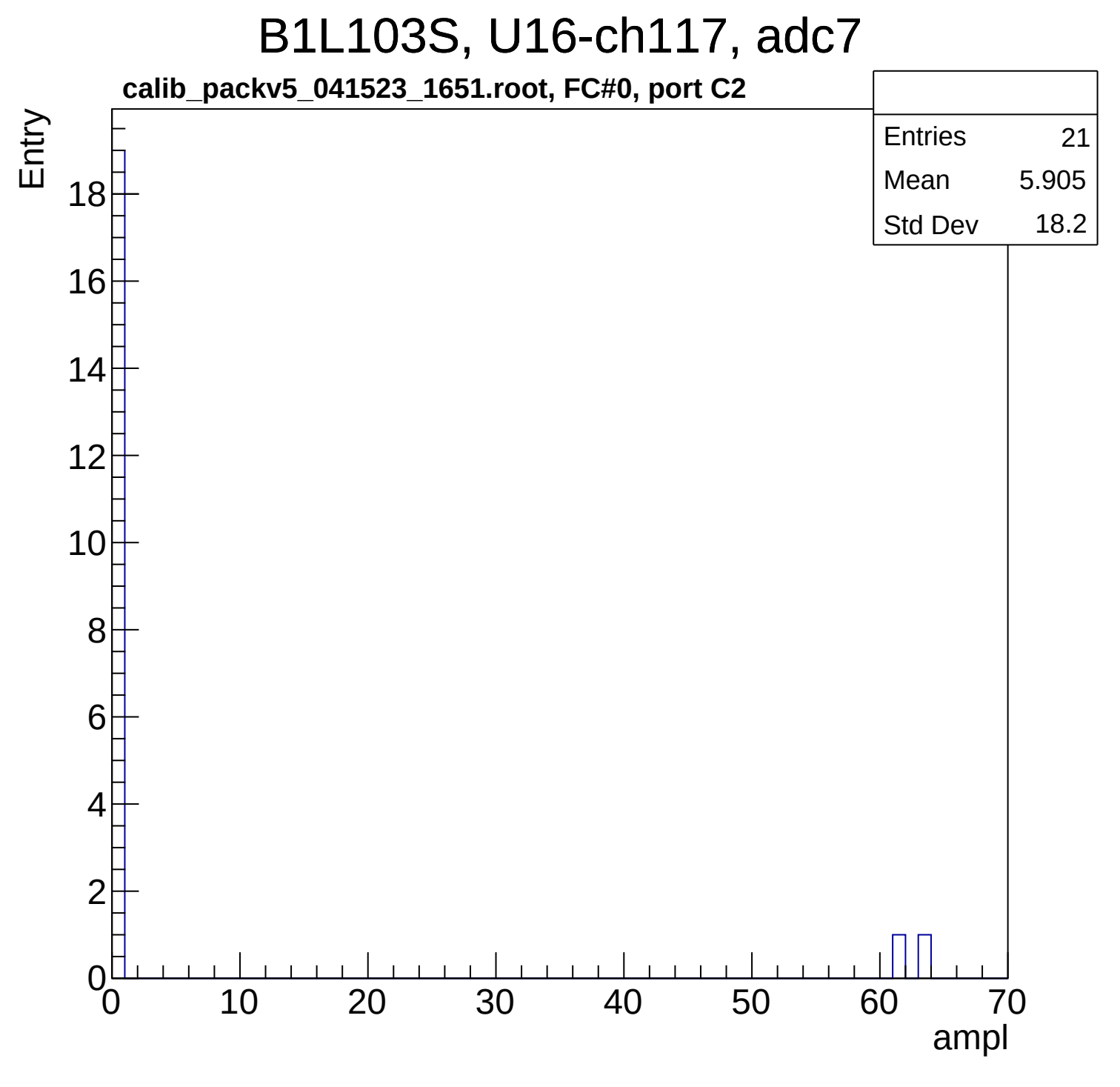
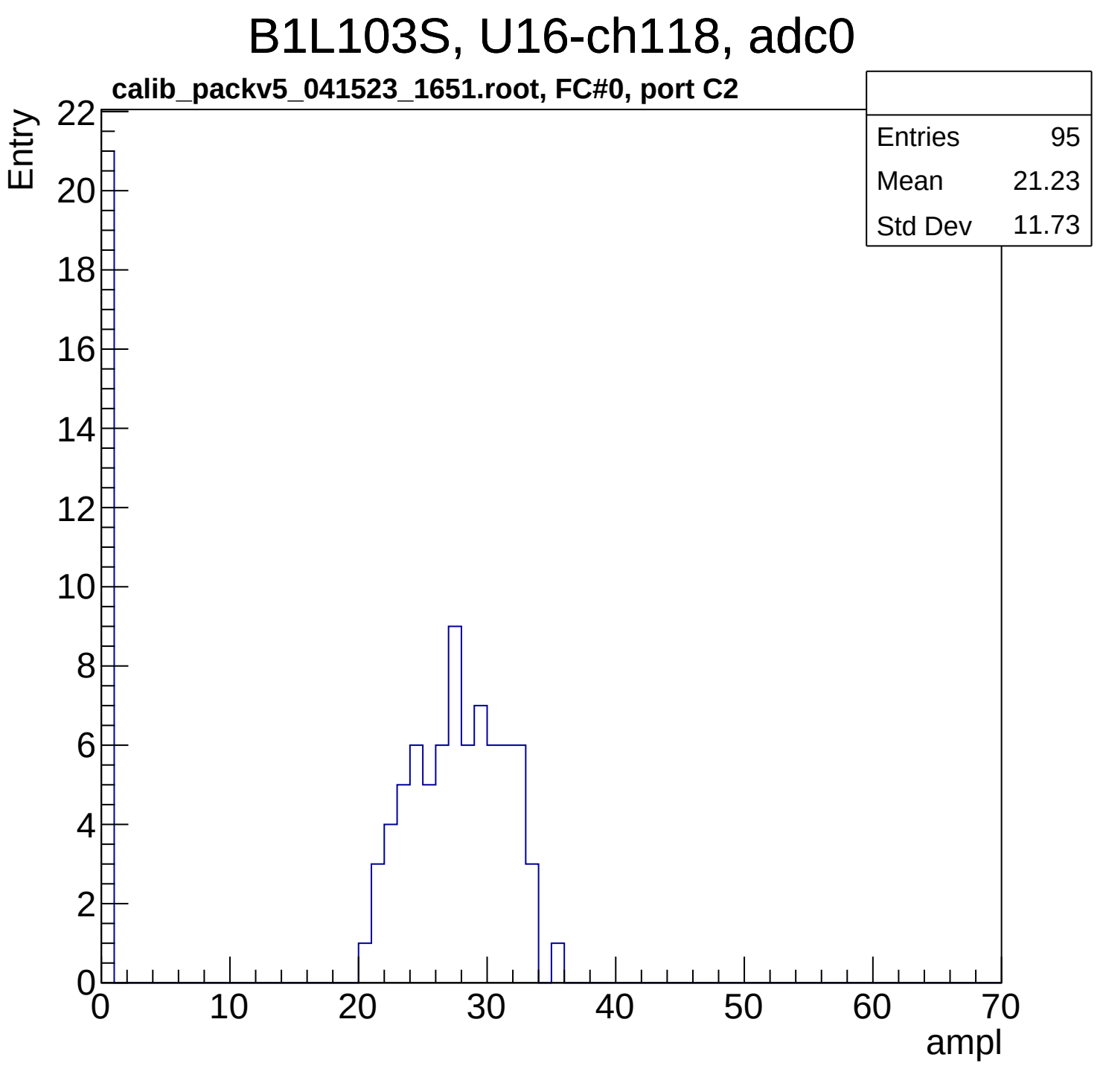

B1L103S, U16-ch117, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 61.81
Std Dev 1.073
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U16-ch117, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch118, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 21.23
Std Dev 11.73
Entry
ampl
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2
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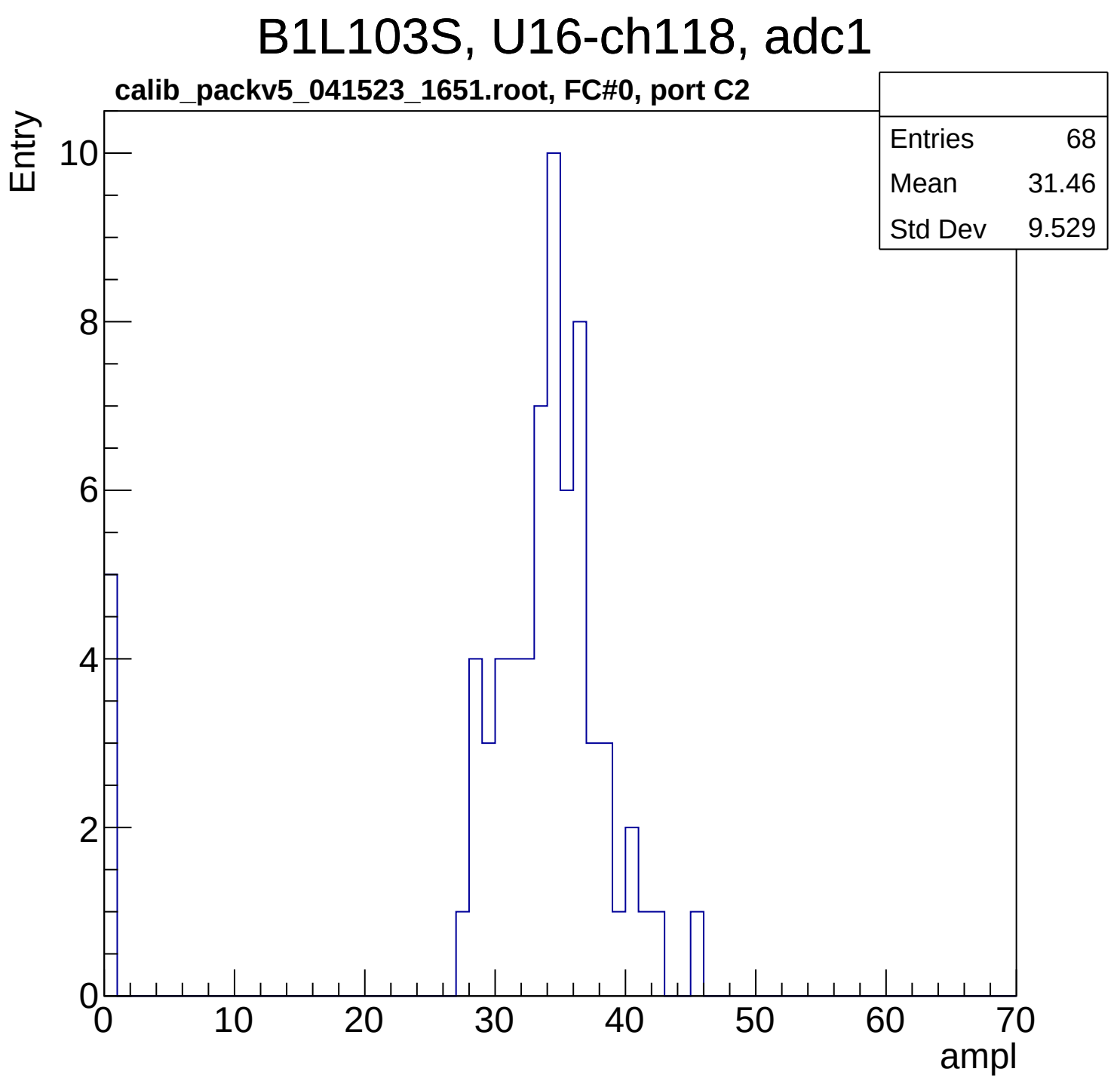
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U16-ch118, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 31.46
Std Dev 9.529
Entry
ampl
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2
4
6
8
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0
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20
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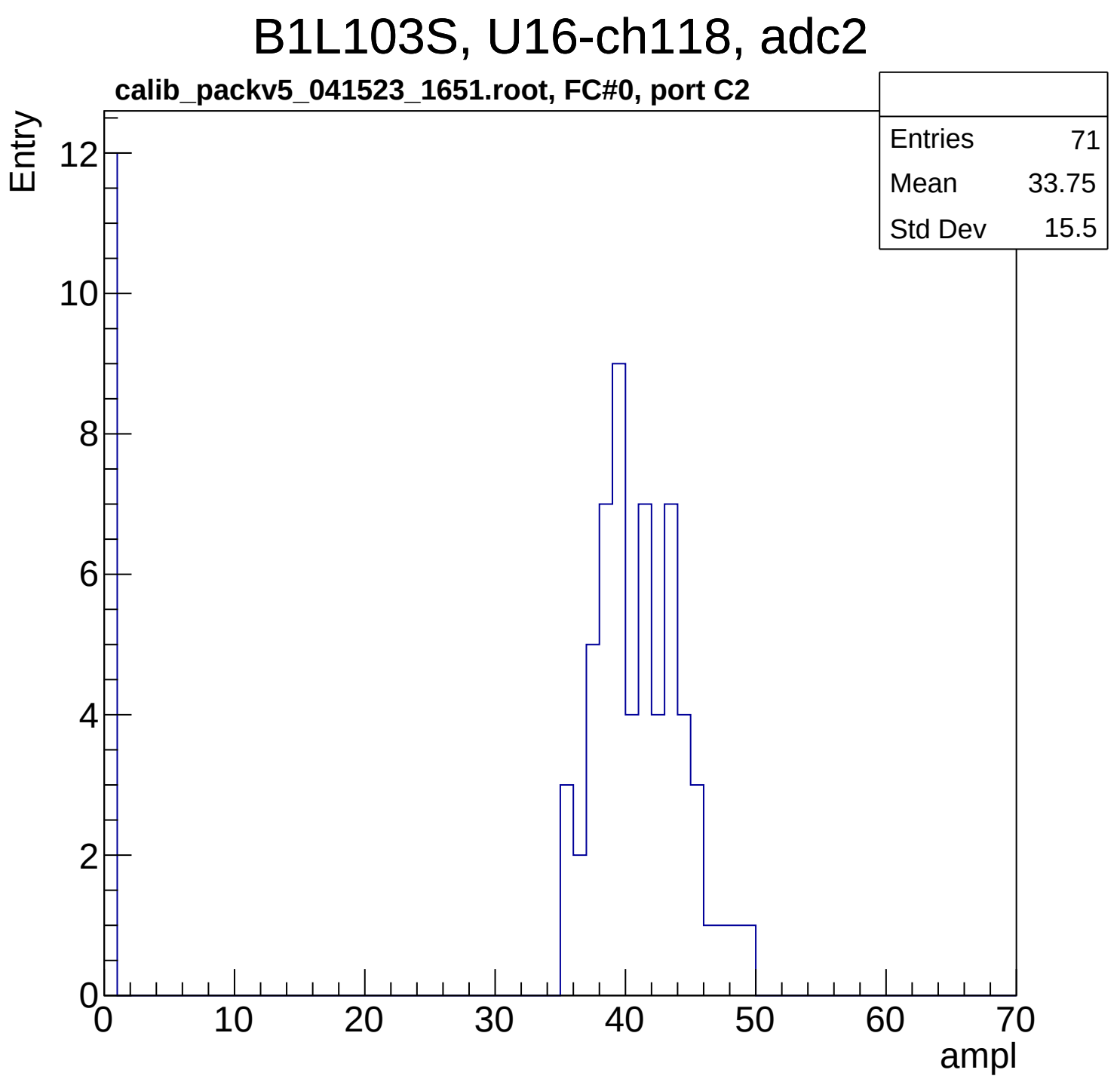
60
70


B1L103S, U16-ch118, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 33.75
Std Dev 15.5
Entry
0
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4
6
8
10
12
0
10
20
30
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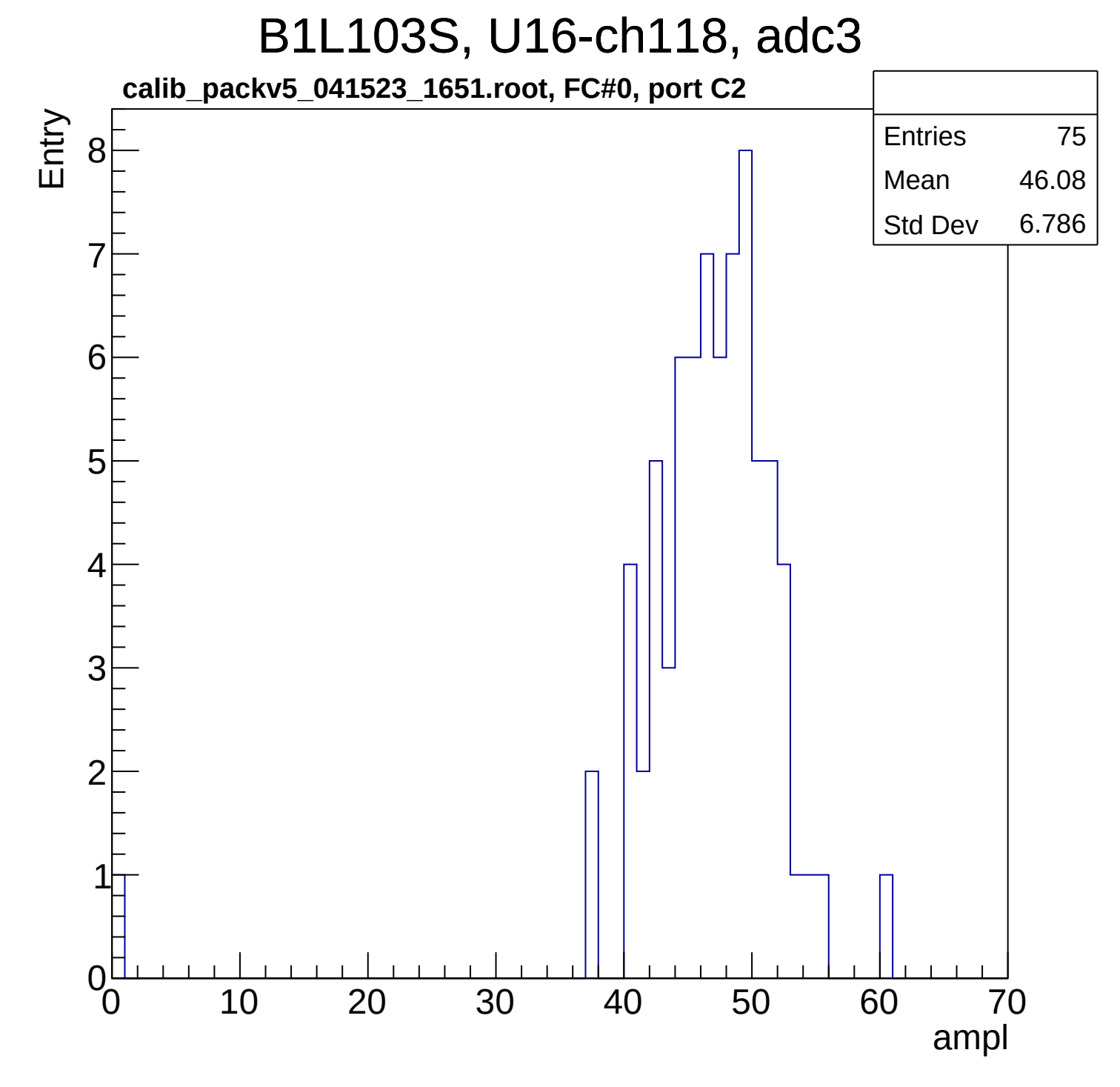
50
60
70
ampl


B1L103S, U16-ch118, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 46.08
Std Dev 6.786
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
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60
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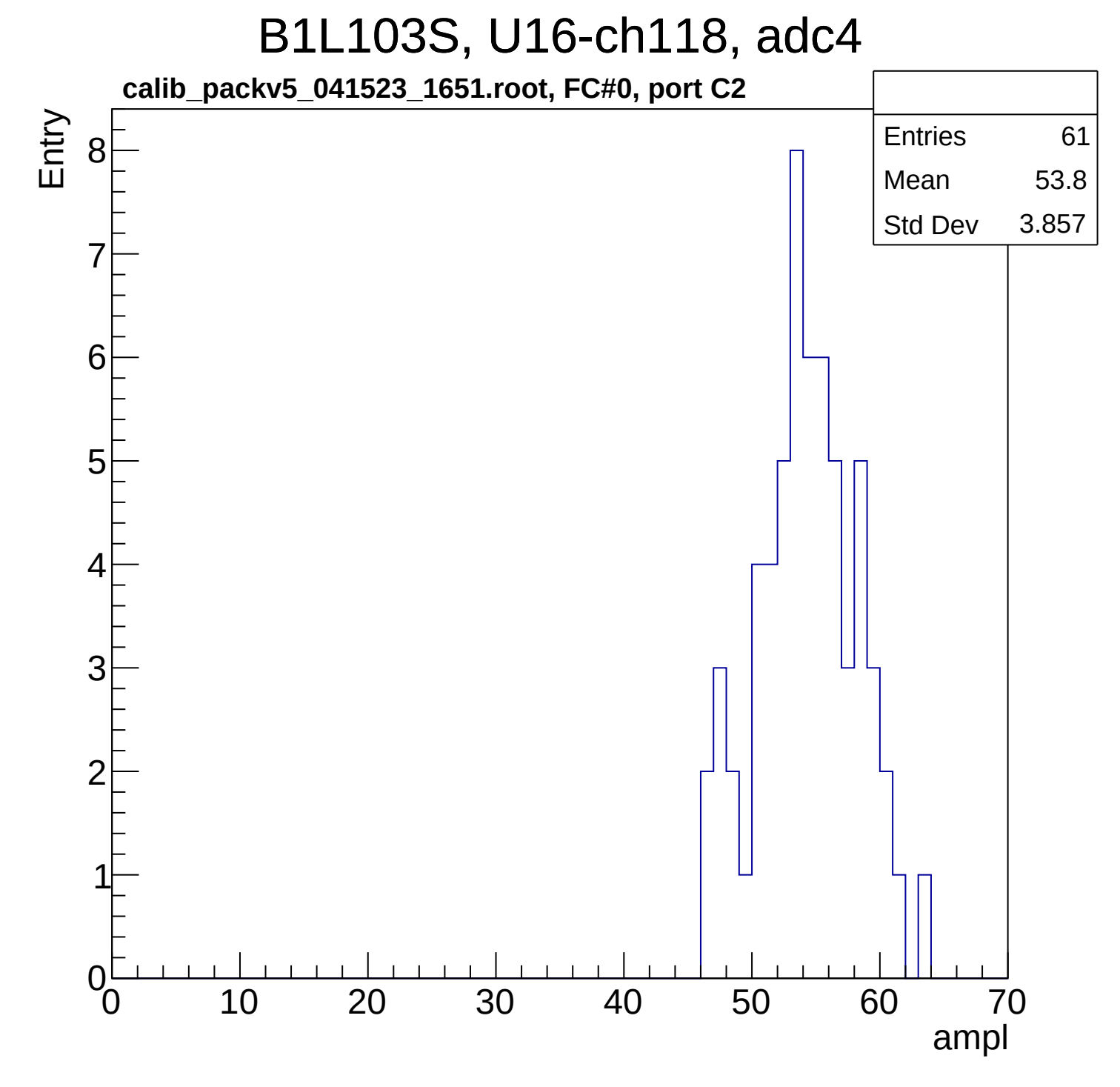
B1L103S, U16-ch118, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 53.8
Std Dev 3.857
Entry
ampl
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3
4
5
6
7
8
0
10
20
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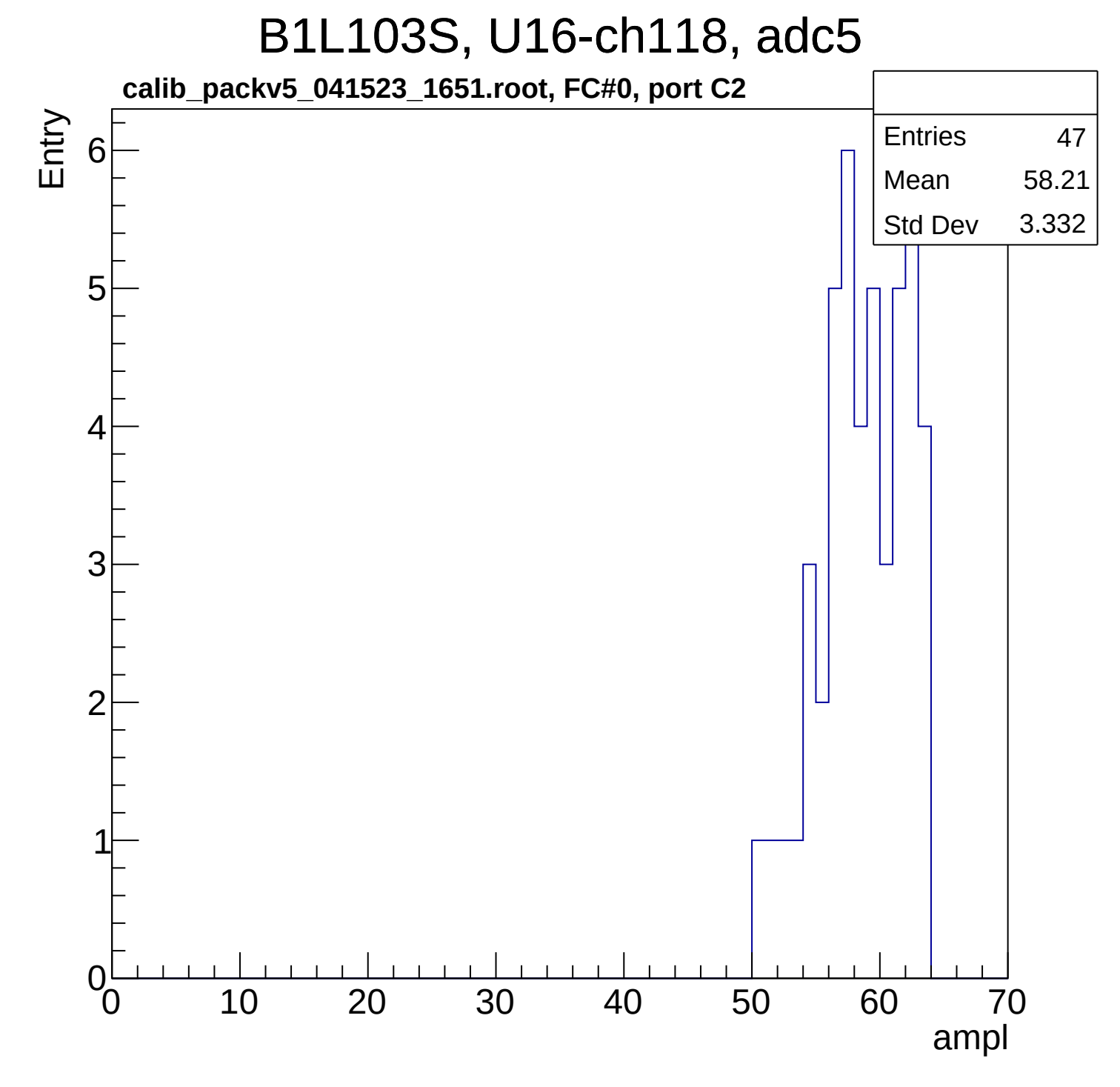
50
60
70


B1L103S, U16-ch118, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.21
Std Dev 3.332
Entry
ampl
0
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3
4
5
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0
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60
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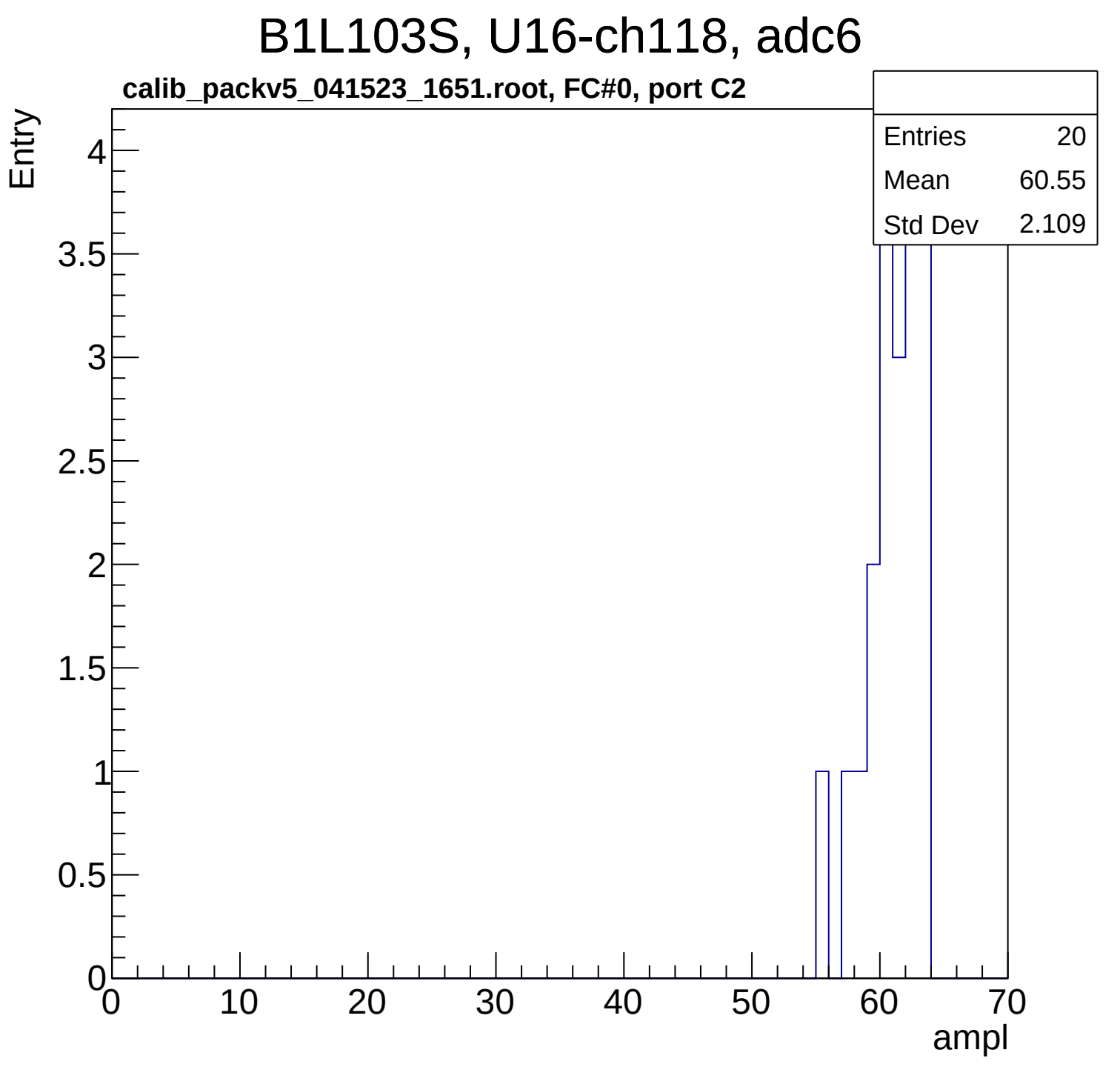
B1L103S, U16-ch118, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 60.55
Std Dev 2.109
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
10
20
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40
50
60
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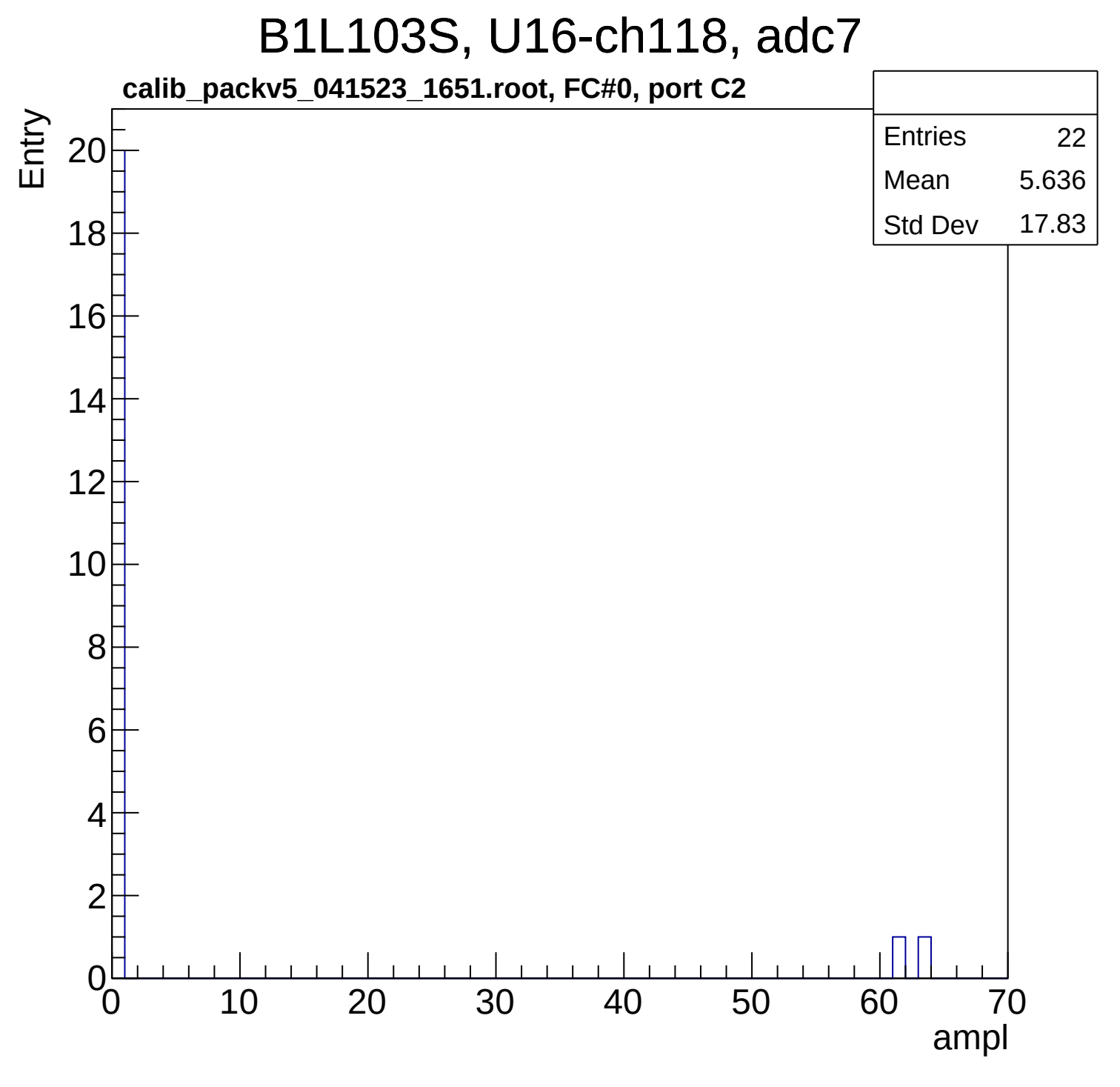
B1L103S, U16-ch118, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 5.636
Std Dev 17.83
Entry
ampl
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6
8
10
12
14
16
18
20
0
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20
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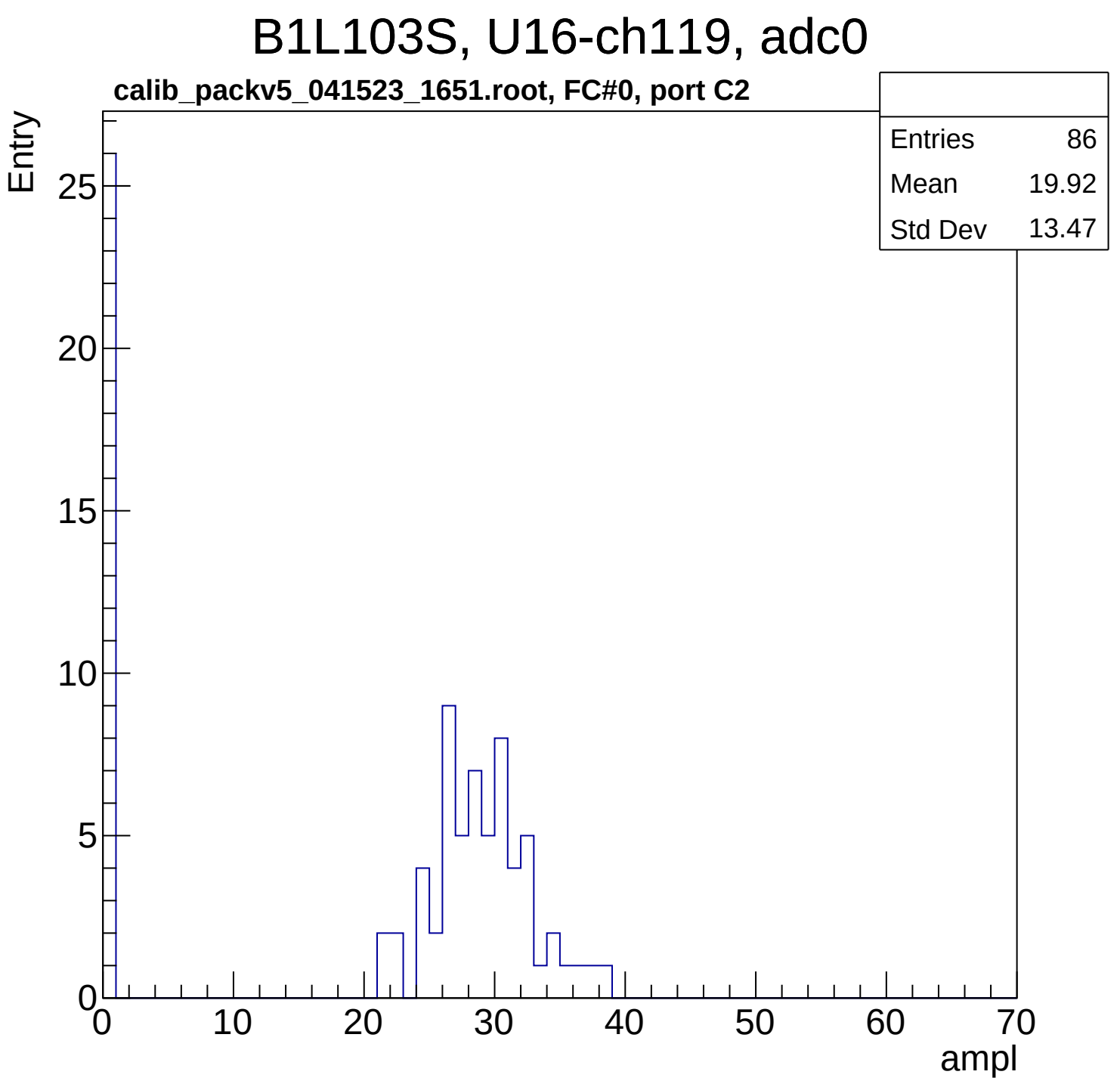
40
50
60
70


B1L103S, U16-ch119, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 19.92
Std Dev 13.47
Entry
0
5
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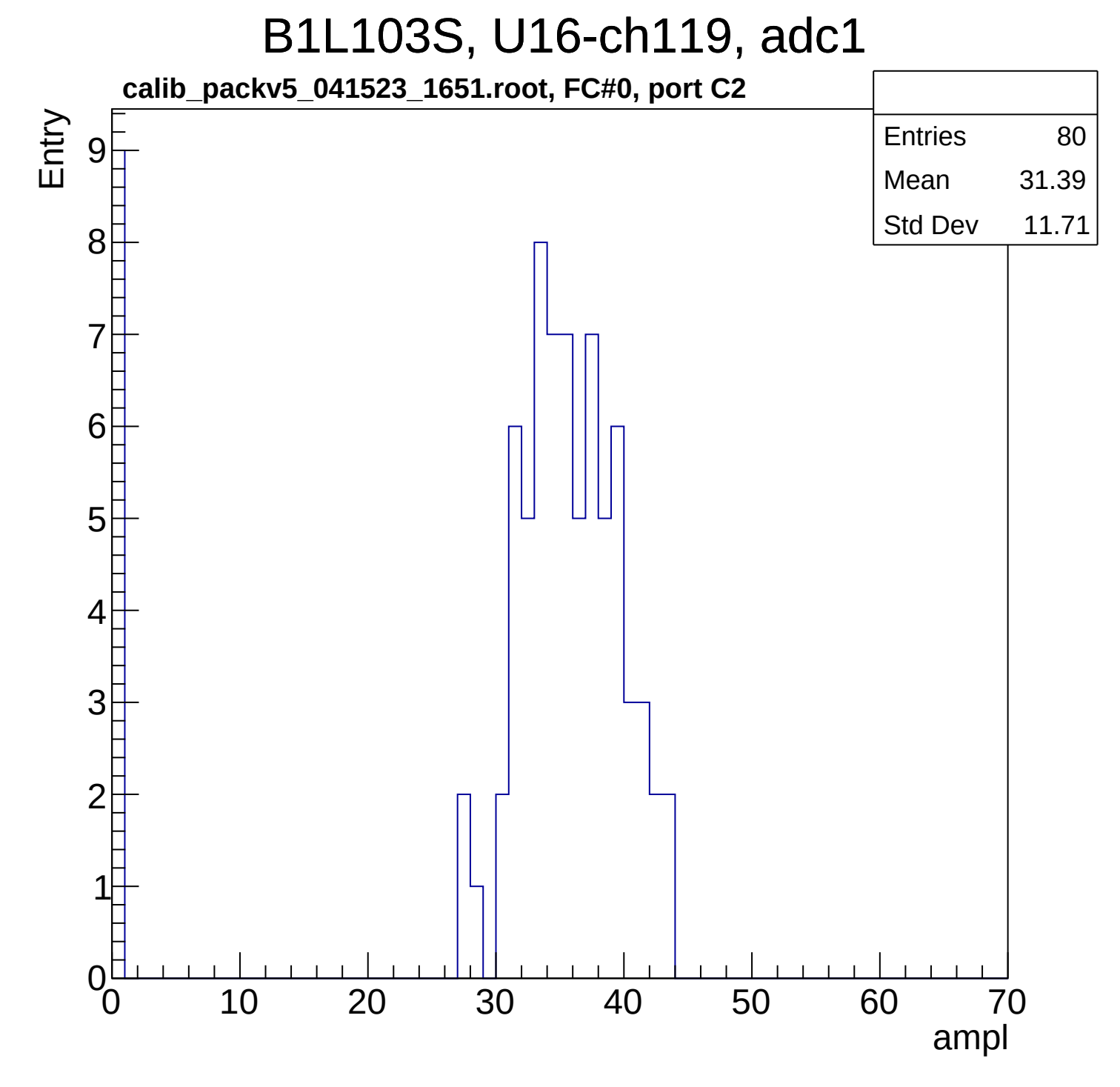
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch119, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 31.39
Std Dev 11.71
Entry
ampl
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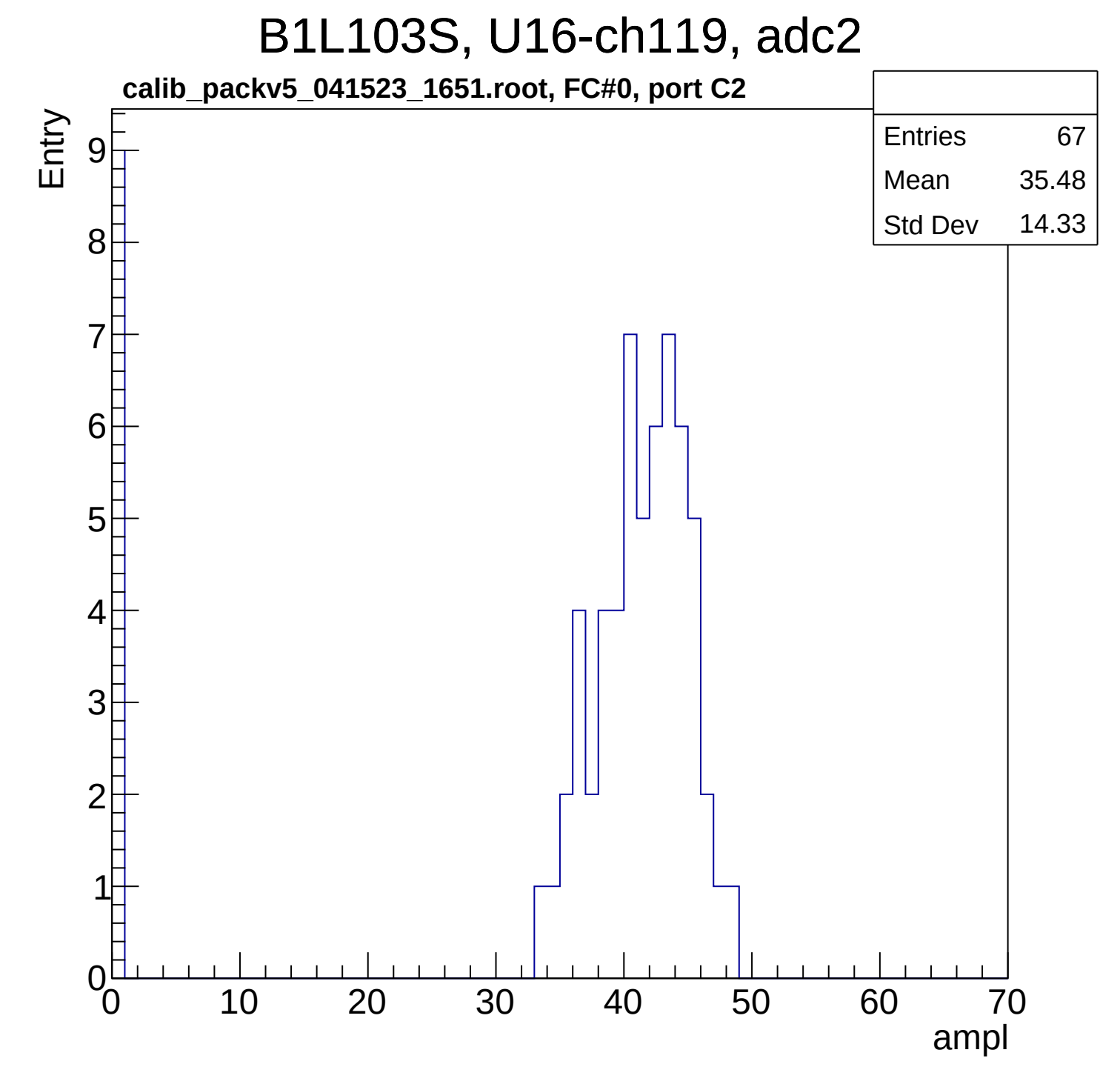
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch119, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 35.48
Std Dev 14.33
Entry
ampl
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2
3
4
5
6
7
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0
10
20
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40
50
60
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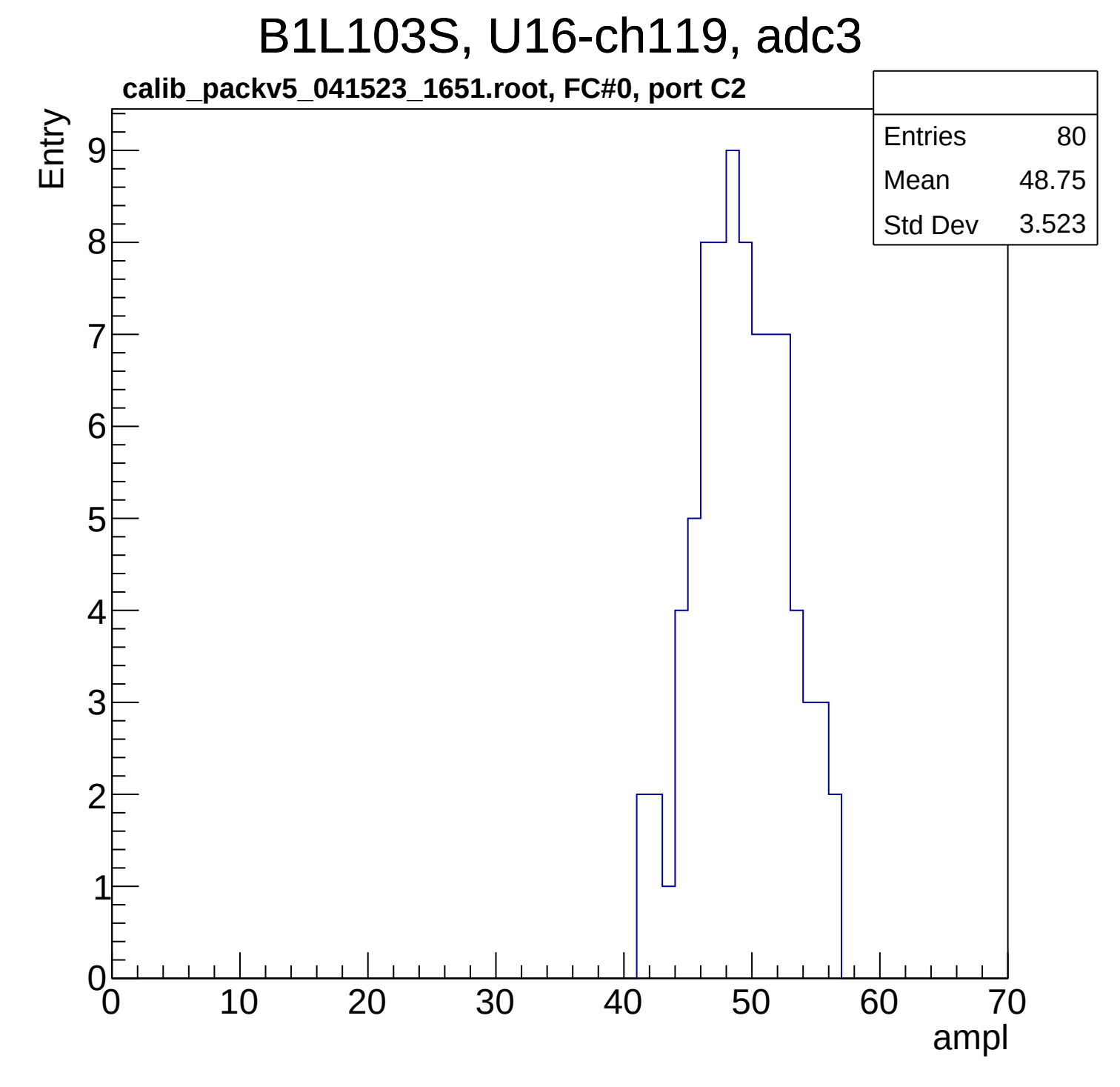
B1L103S, U16-ch119, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 48.75
Std Dev 3.523
Entry
ampl
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3
4
5
6
7
8
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60
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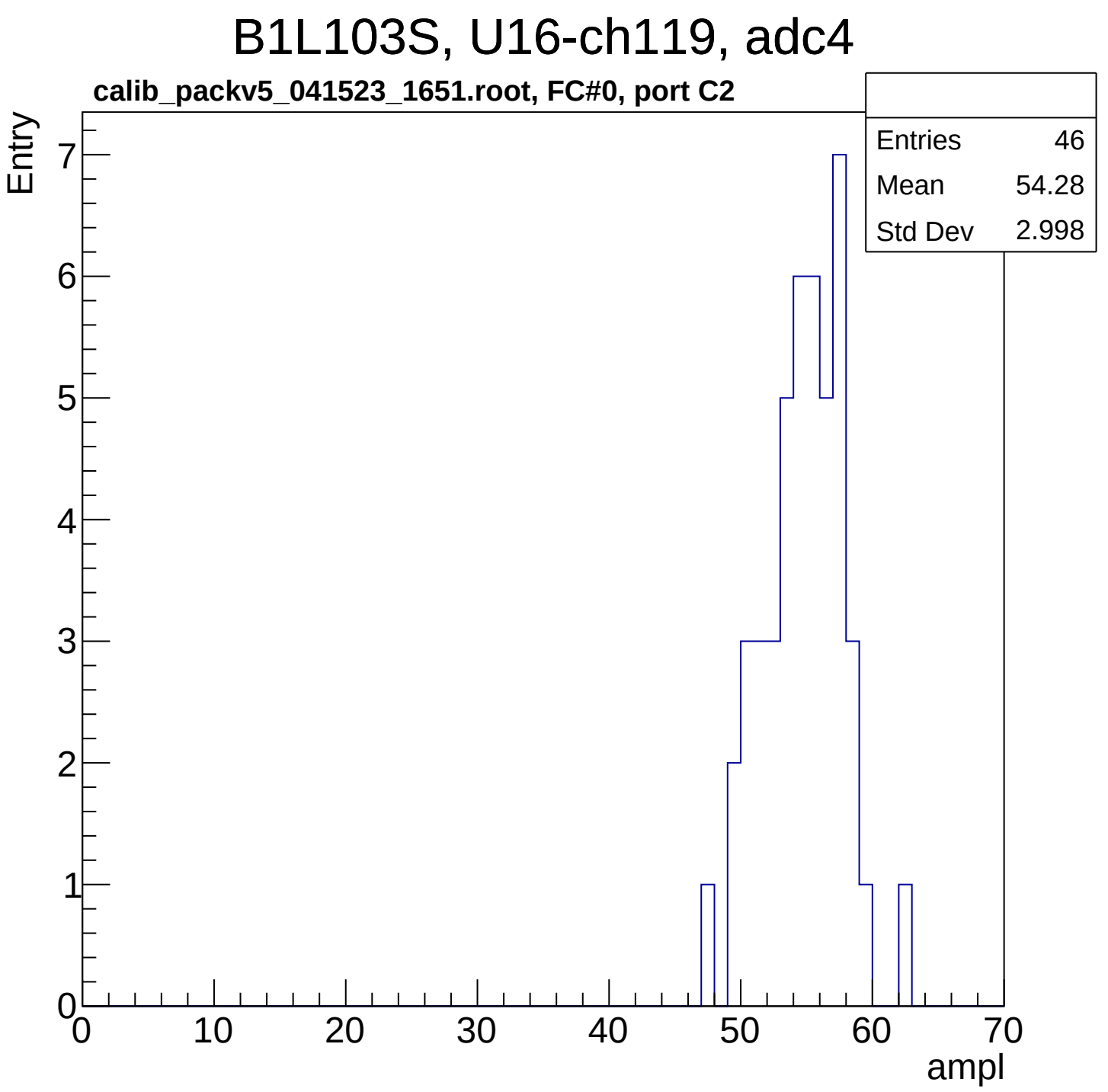
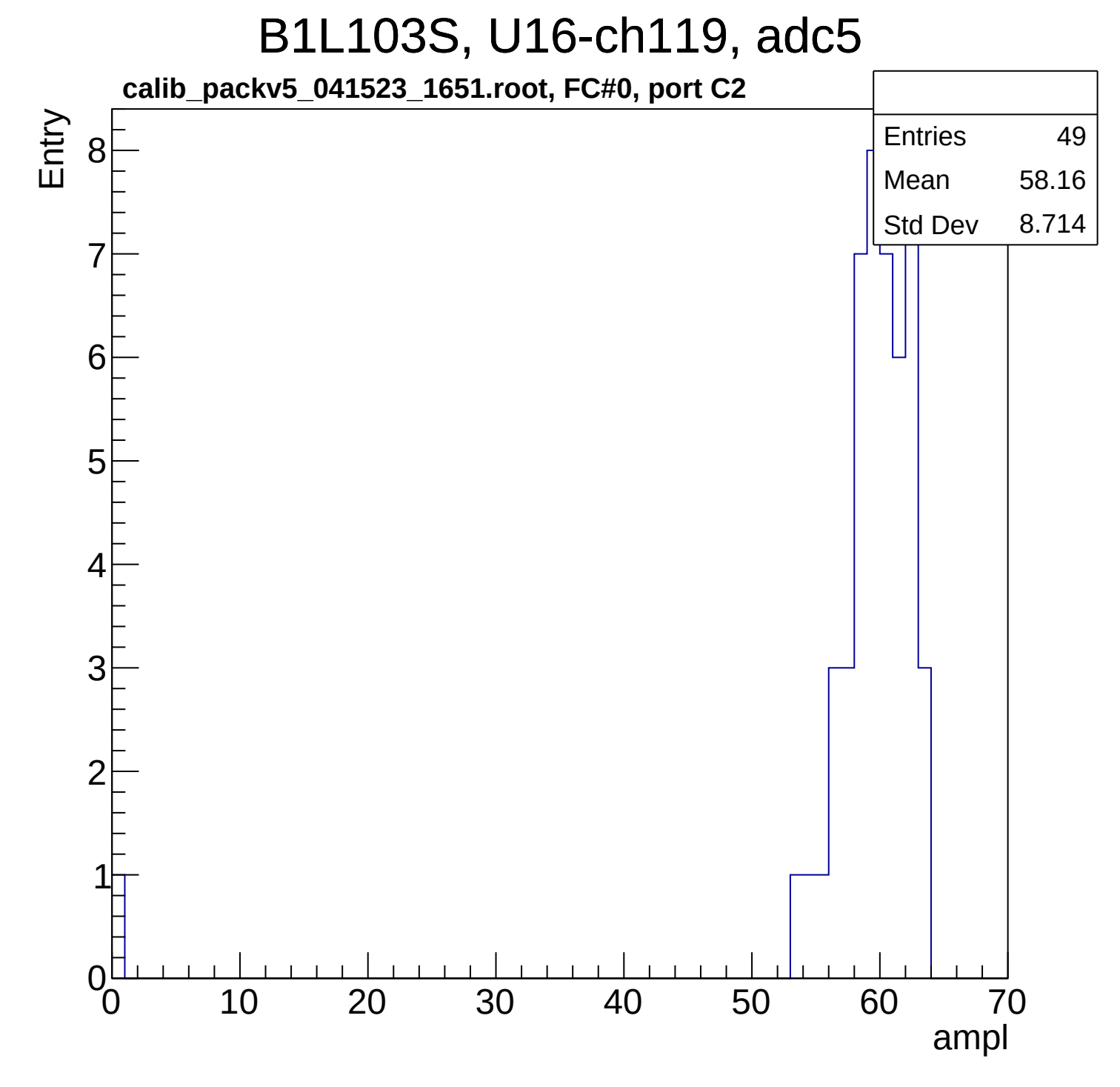

B1L103S, U16-ch119, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 54.28
Std Dev 2.998
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch119, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.16
Std Dev 8.714
Entry
ampl
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1
2
3
4
5
6
7
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0
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40
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60
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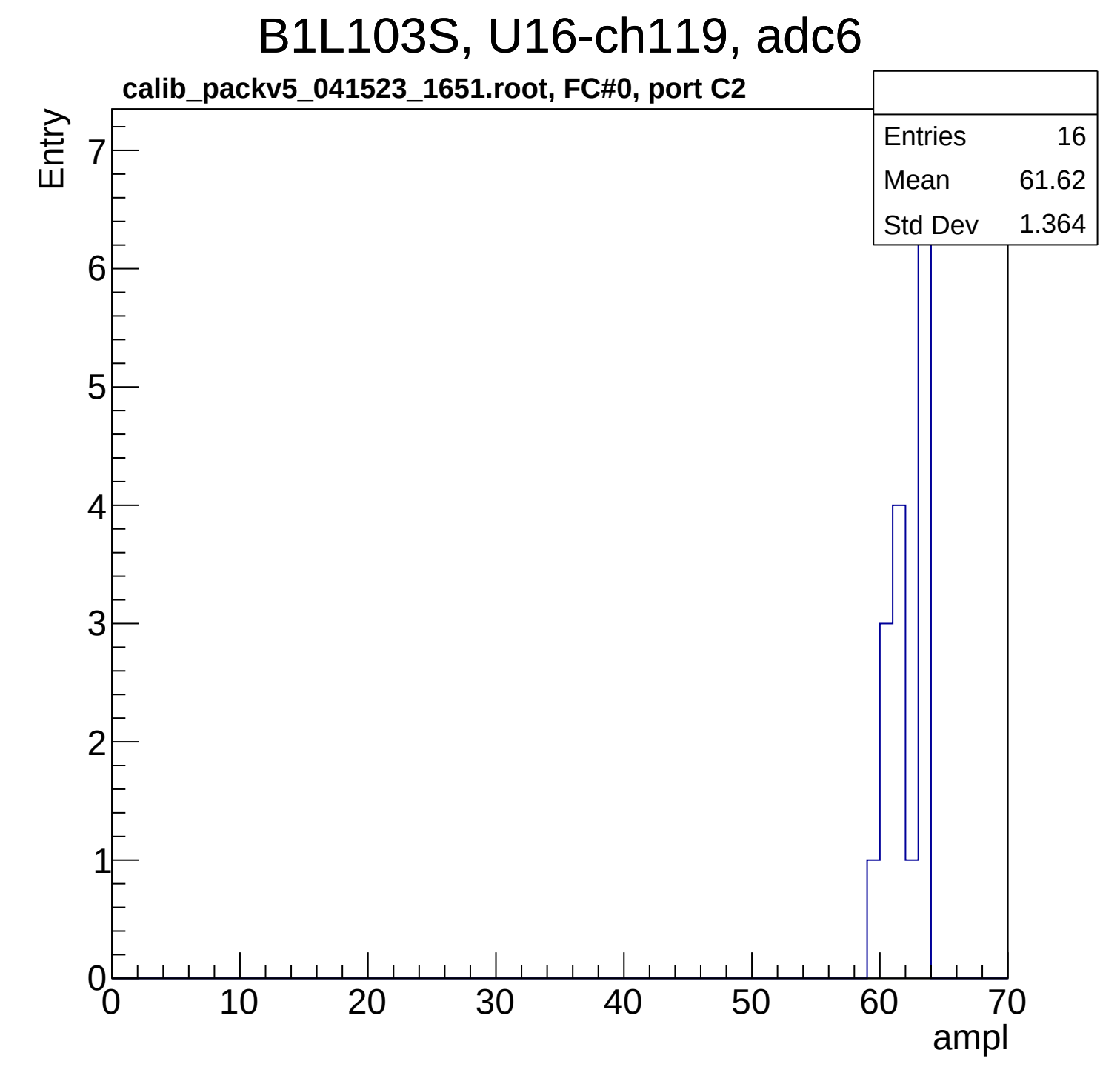
B1L103S, U16-ch119, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 61.62
Std Dev 1.364
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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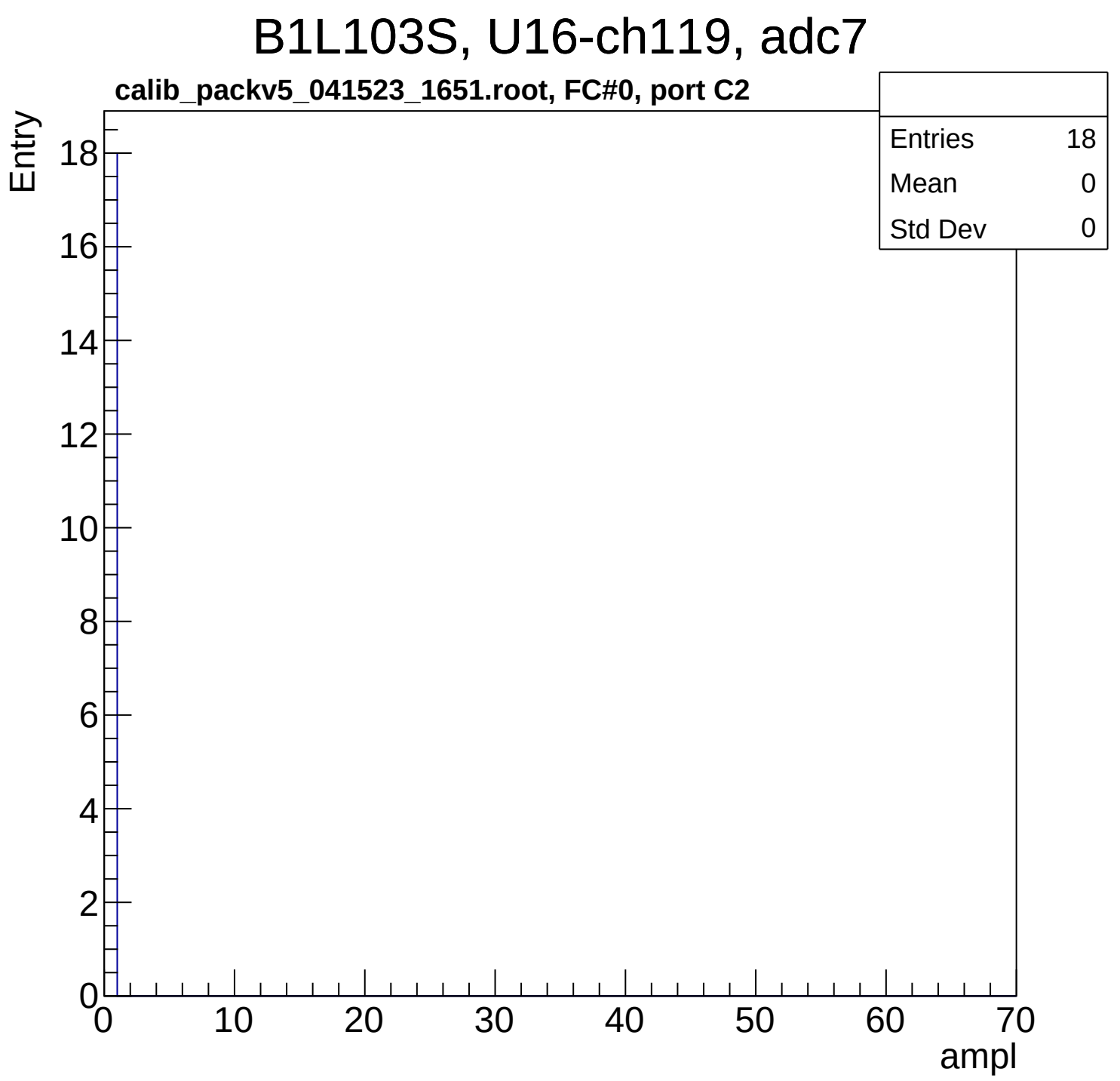
40
50
60
70


B1L103S, U16-ch119, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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2
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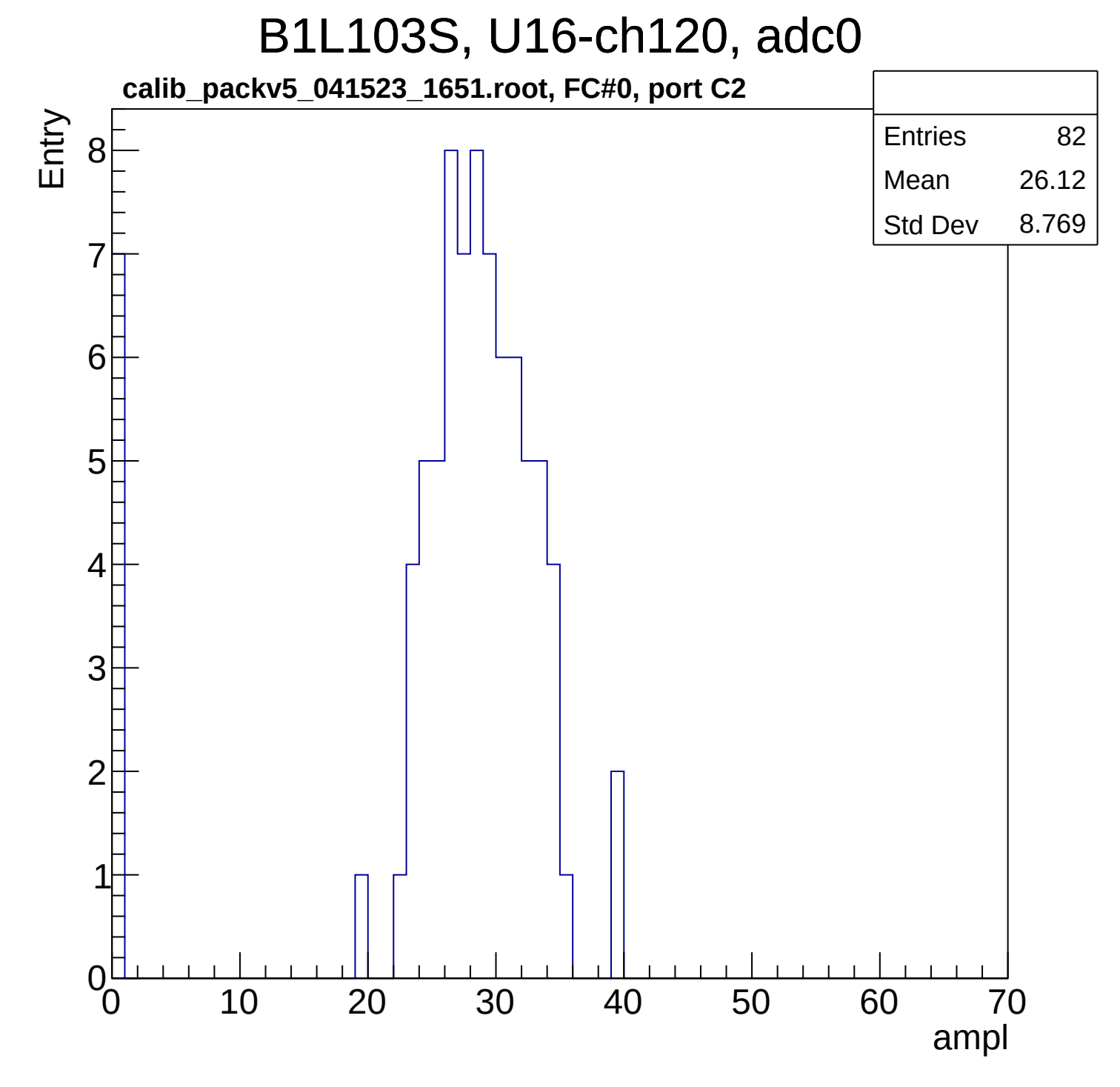
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch120, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 26.12
Std Dev 8.769
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
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60
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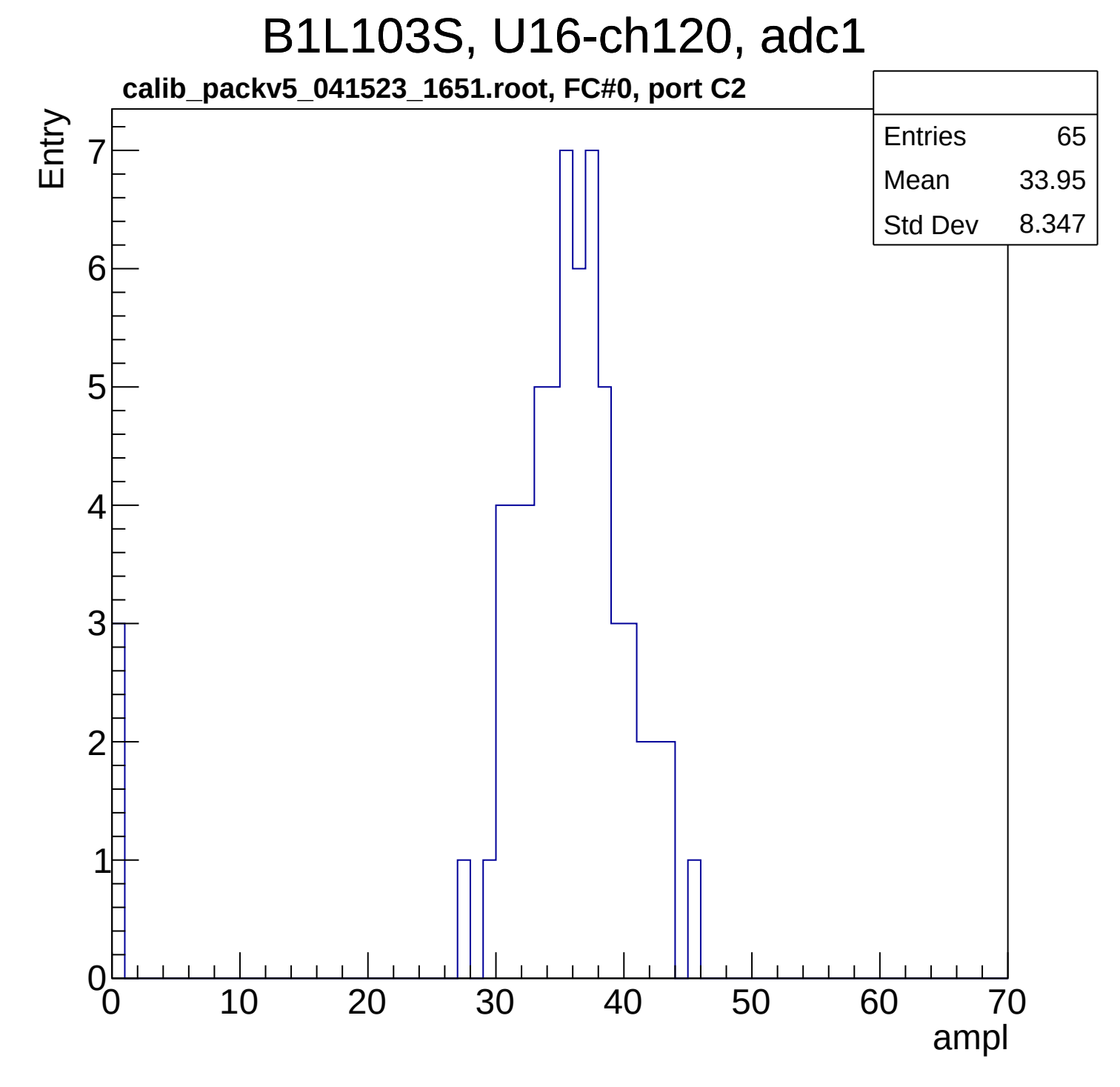
B1L103S, U16-ch120, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 33.95
Std Dev 8.347
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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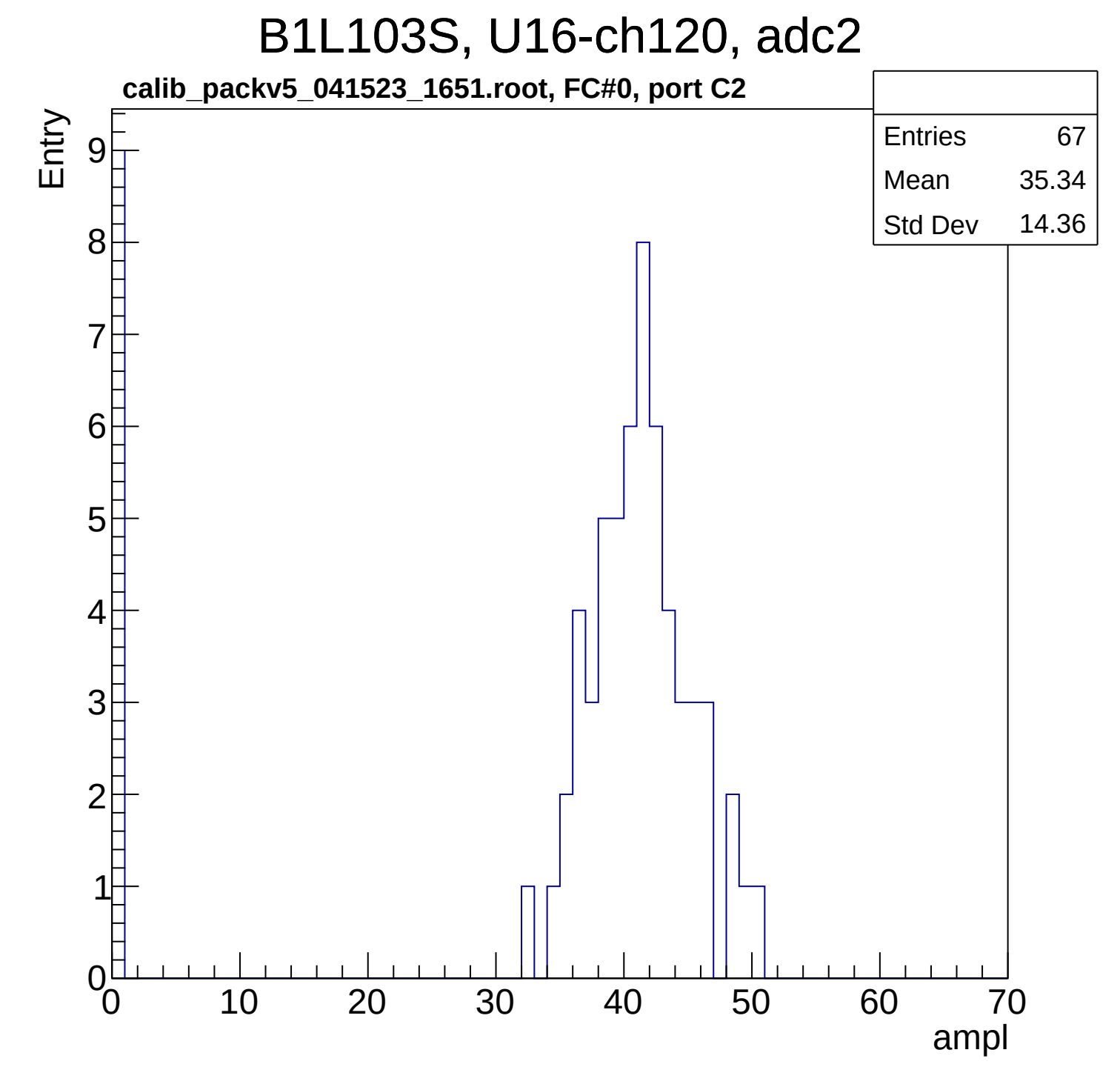
B1L103S, U16-ch120, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 35.34
Std Dev 14.36
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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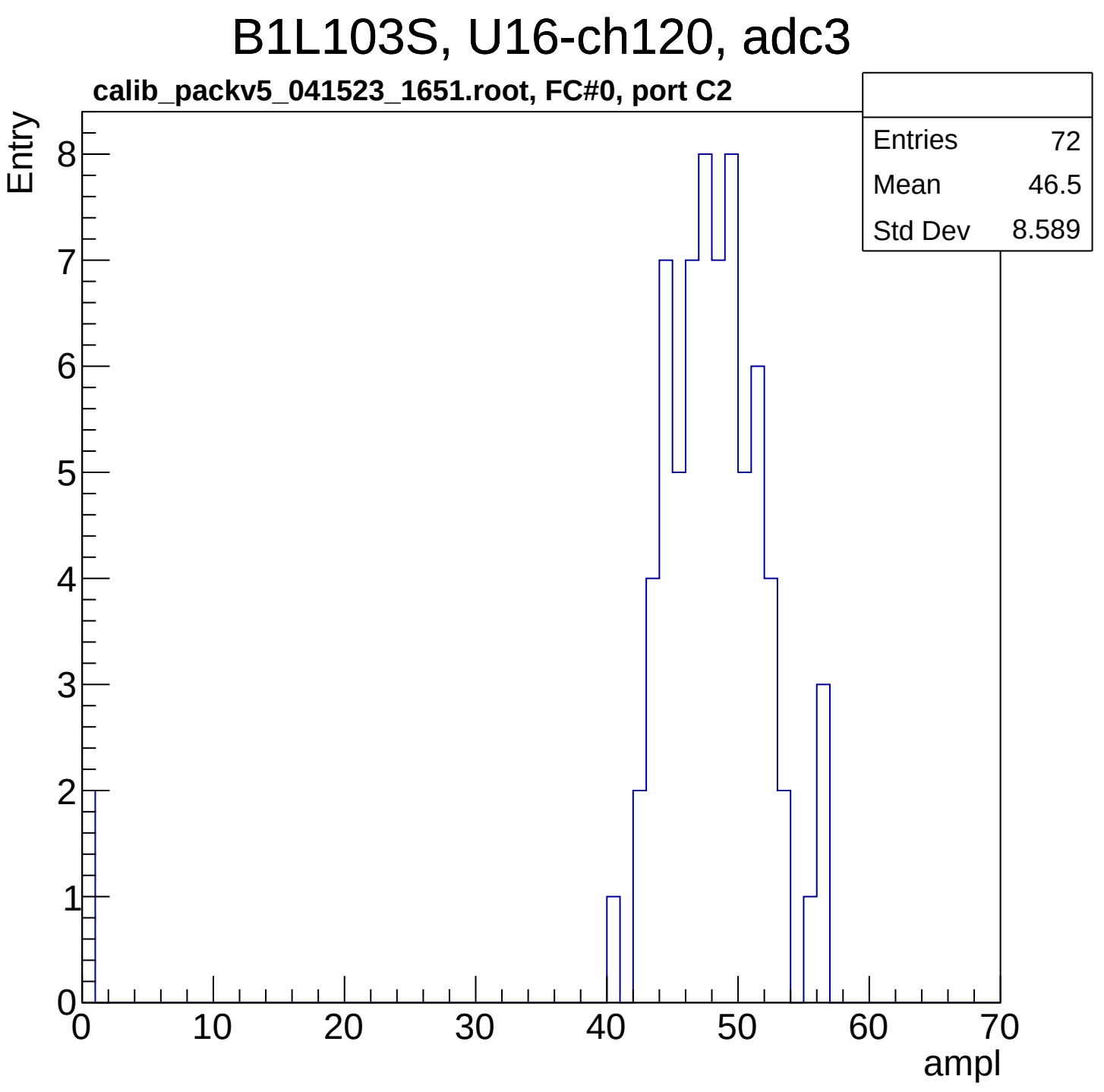
B1L103S, U16-ch120, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 46.5
Std Dev 8.589
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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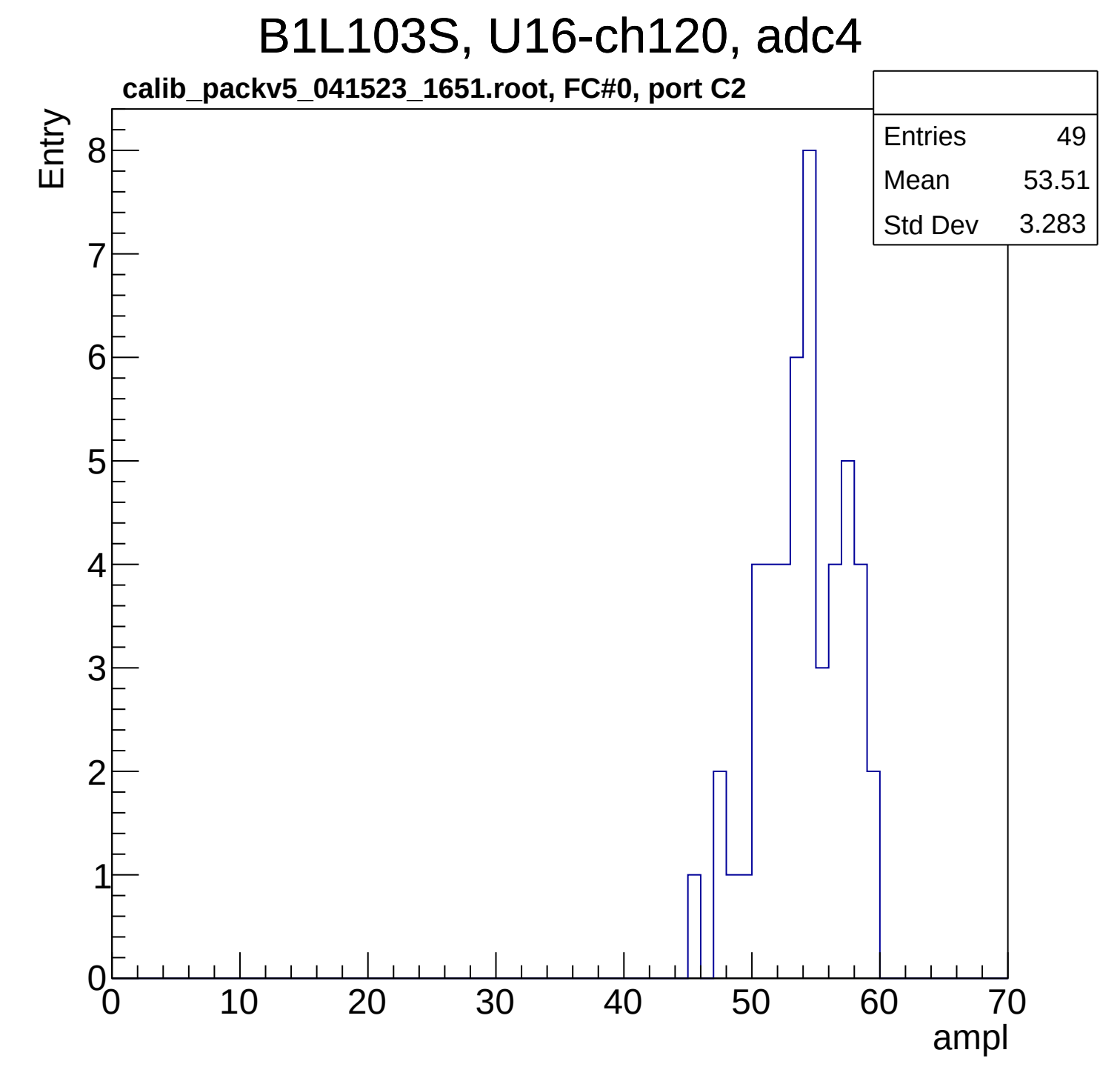
B1L103S, U16-ch120, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 53.51
Std Dev 3.283
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
50
60
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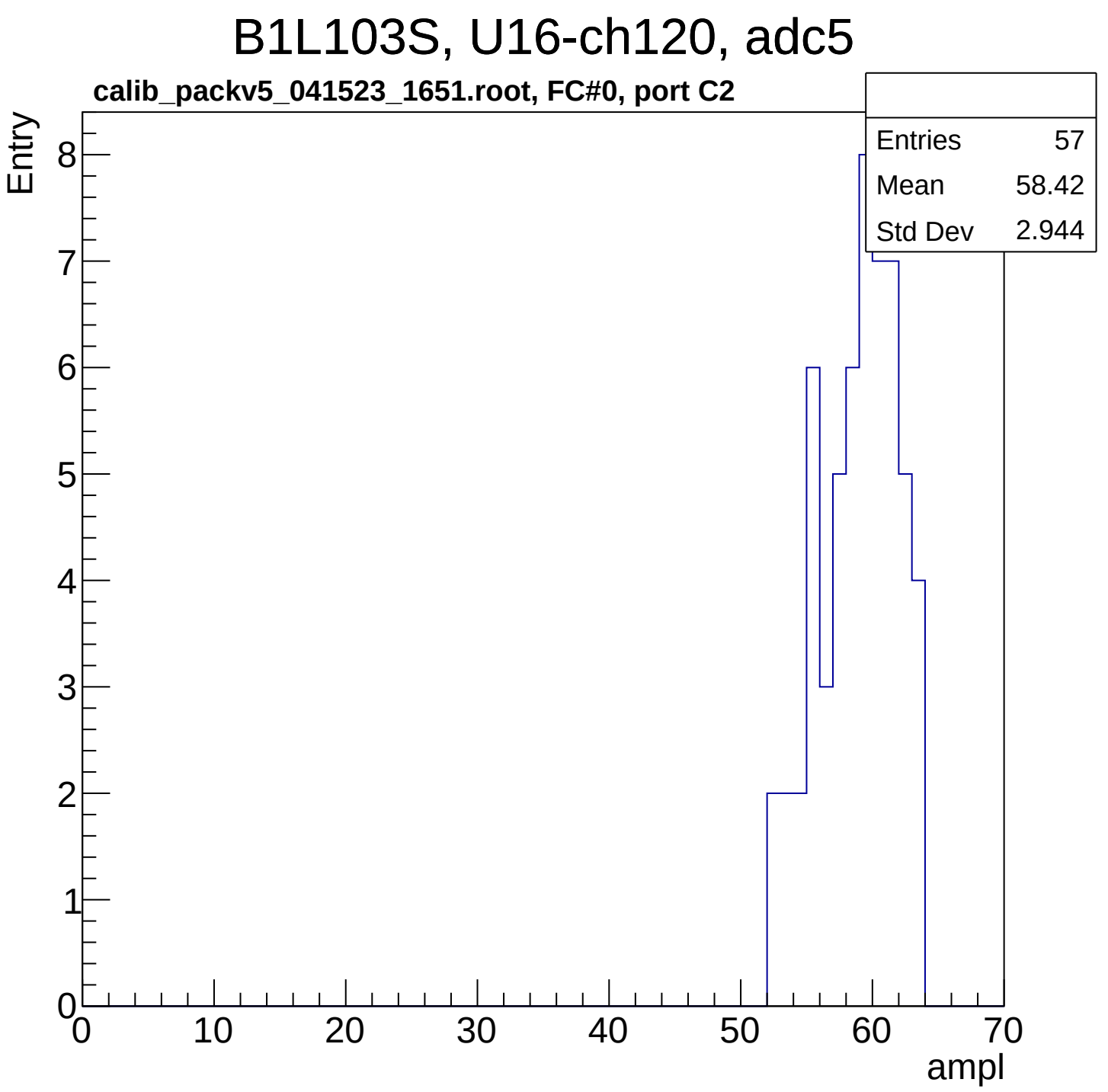
B1L103S, U16-ch120, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.42
Std Dev 2.944
Entry
ampl
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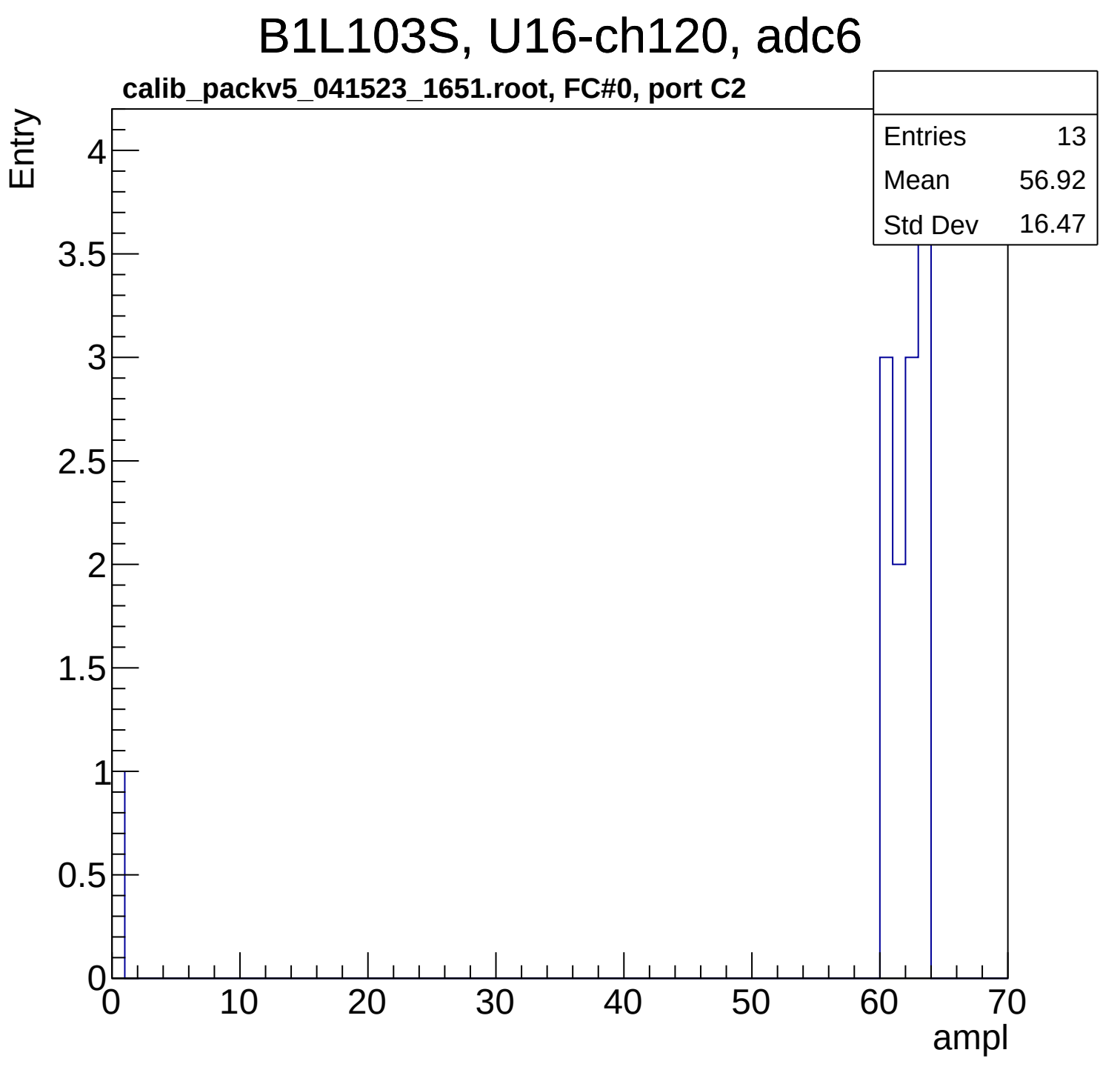
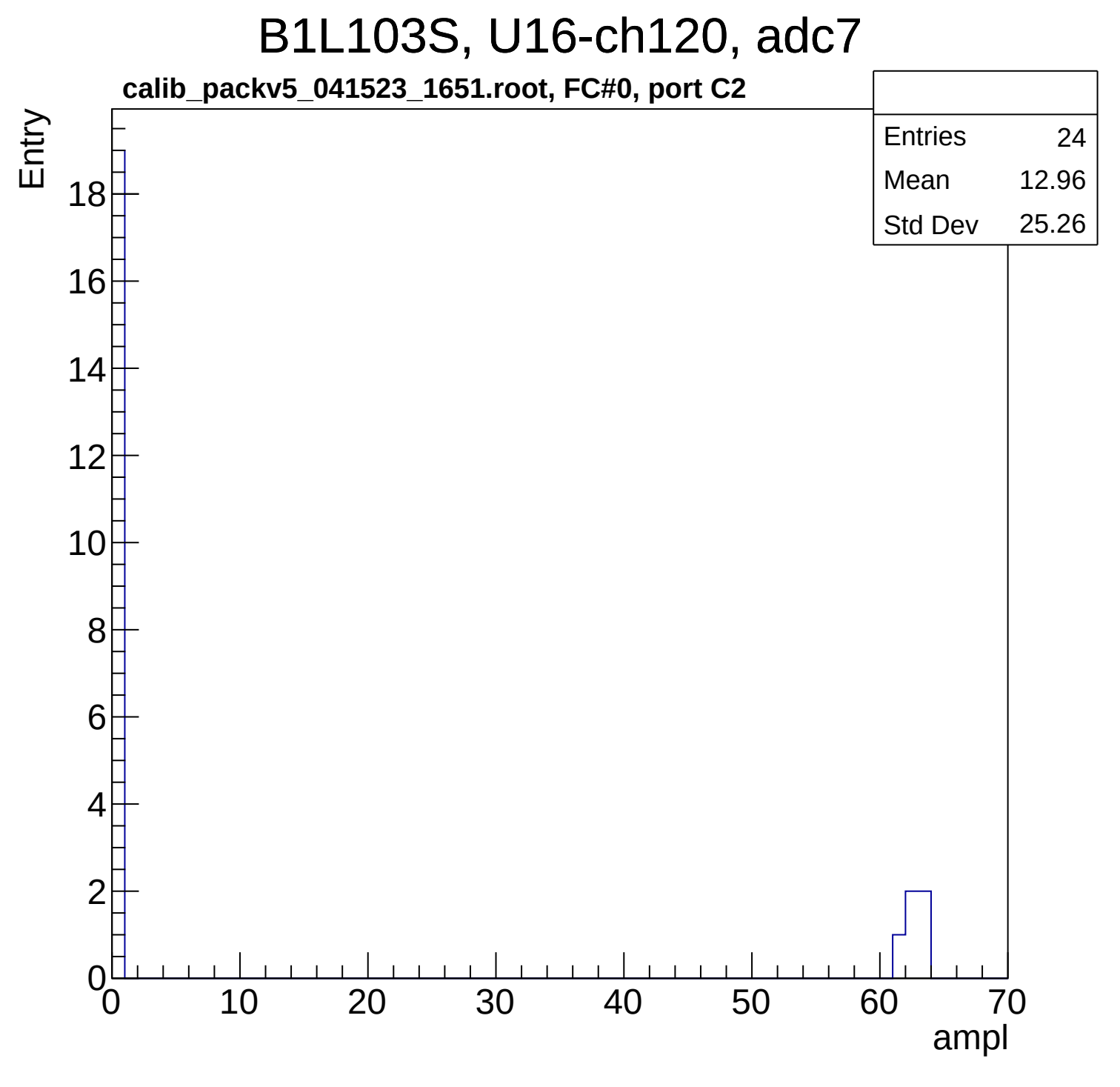
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch120, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 56.92
Std Dev 16.47
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U16-ch120, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 12.96
Std Dev 25.26
Entry
0
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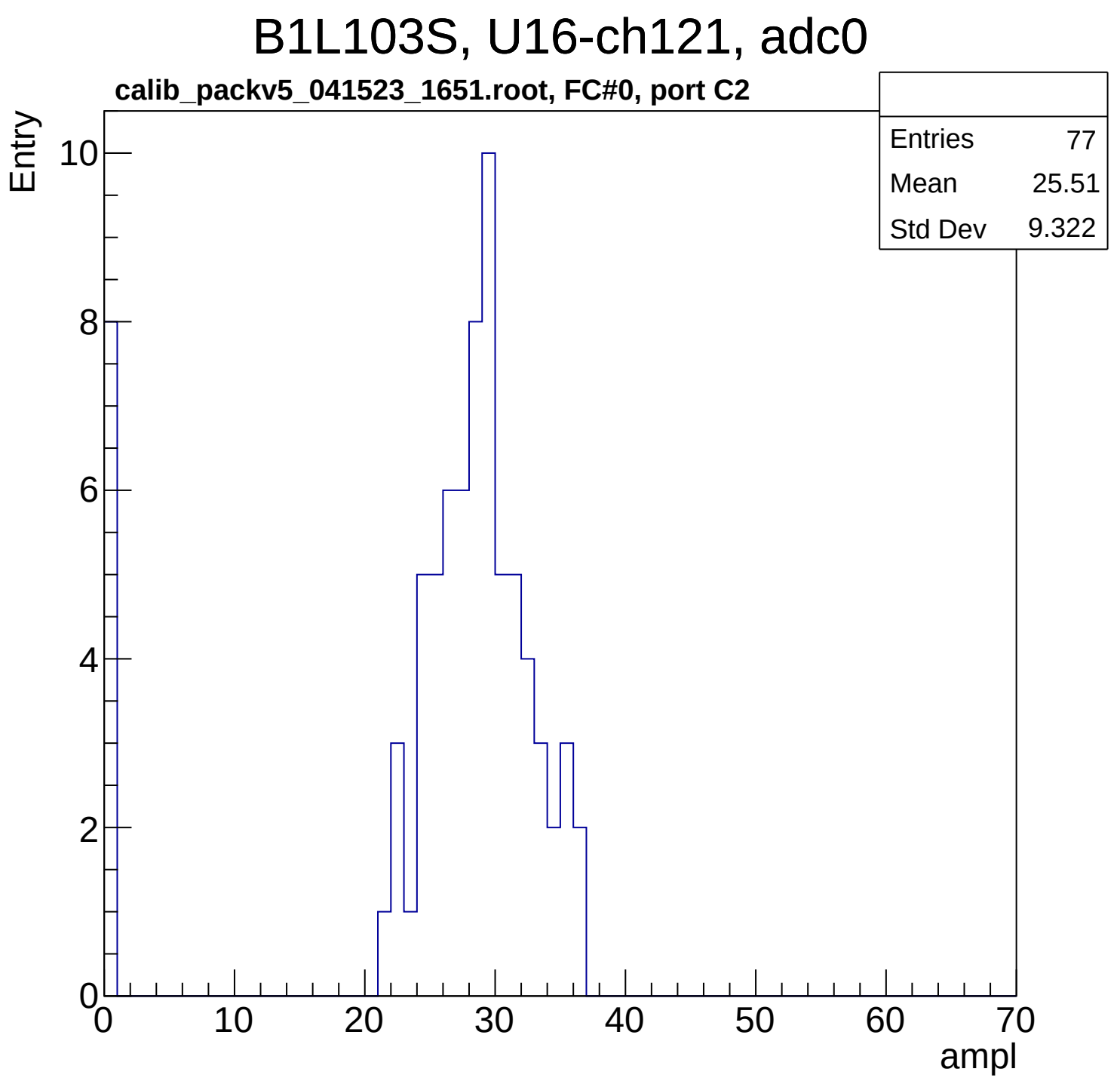
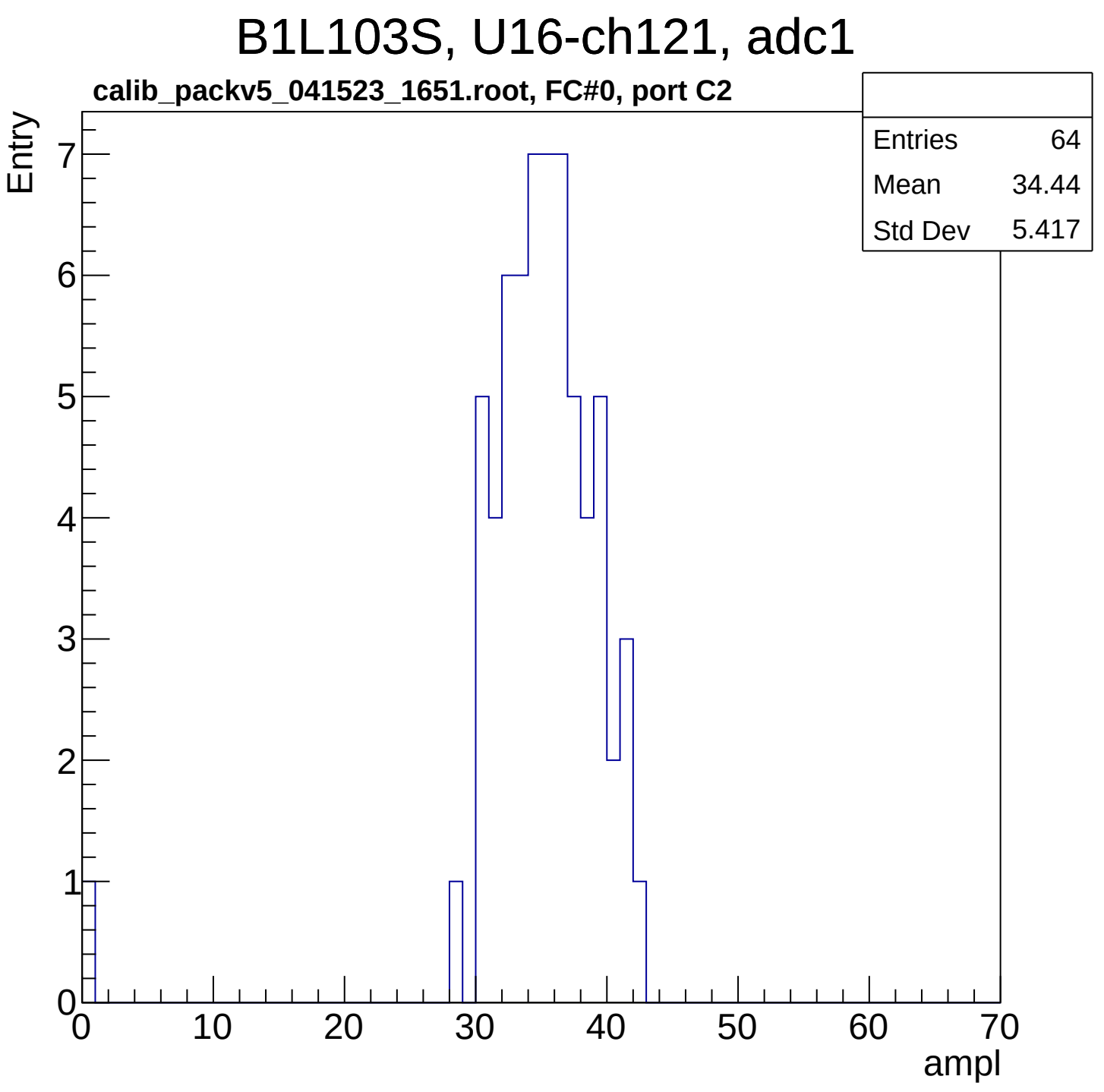
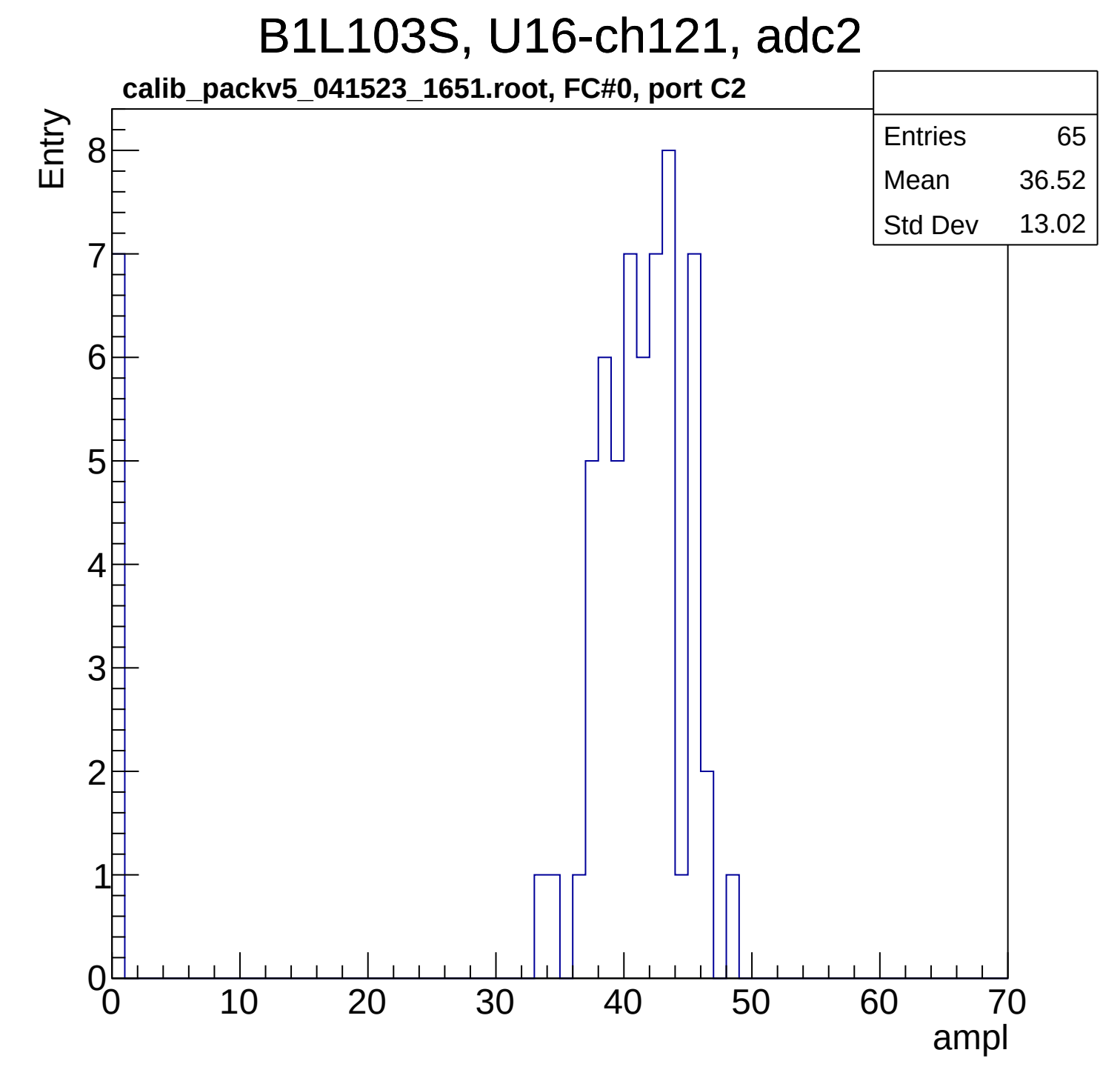
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch121, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 25.51
Std Dev 9.322
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch121, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 34.44
Std Dev 5.417
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch121, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 36.52
Std Dev 13.02
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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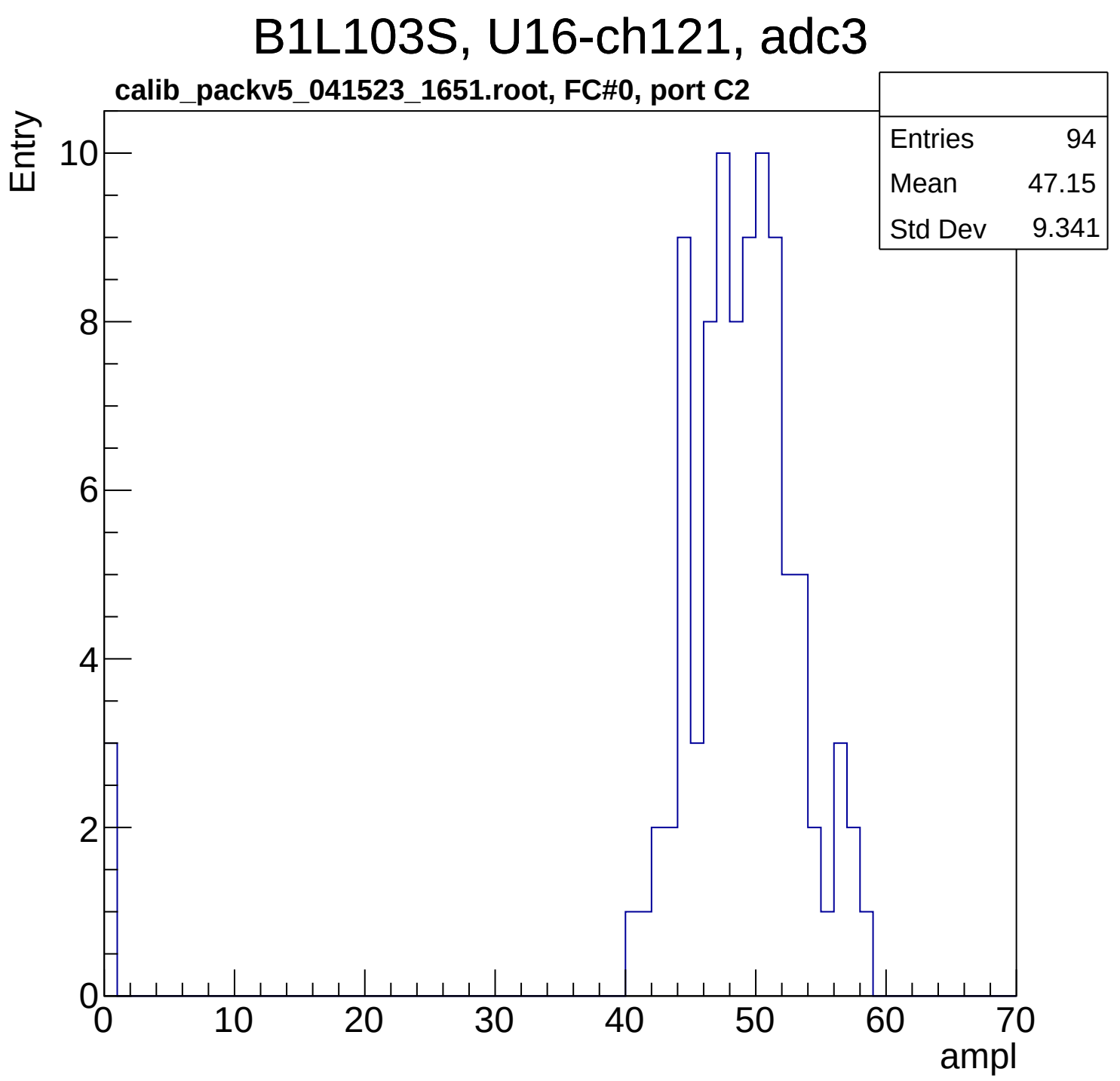
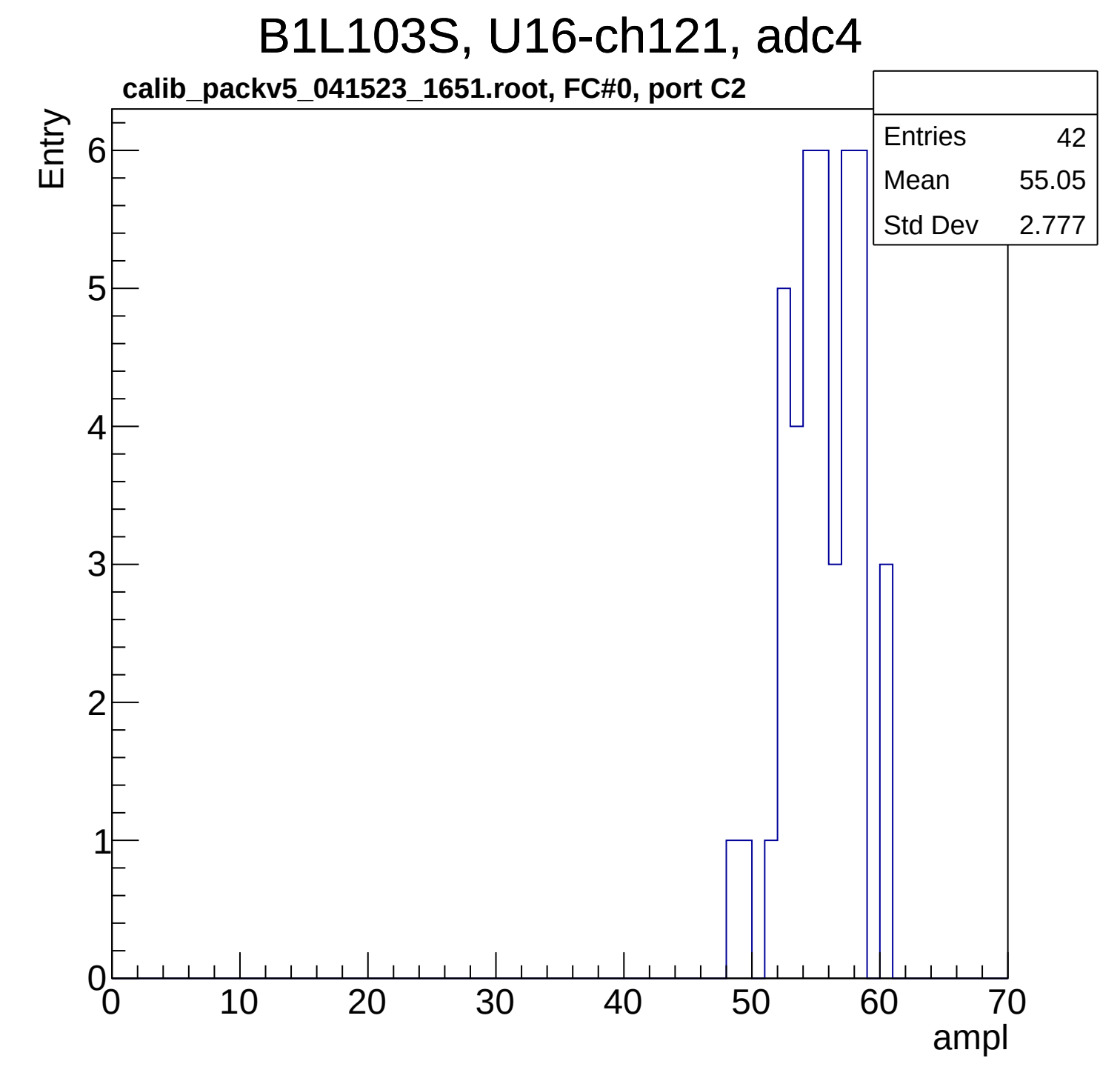
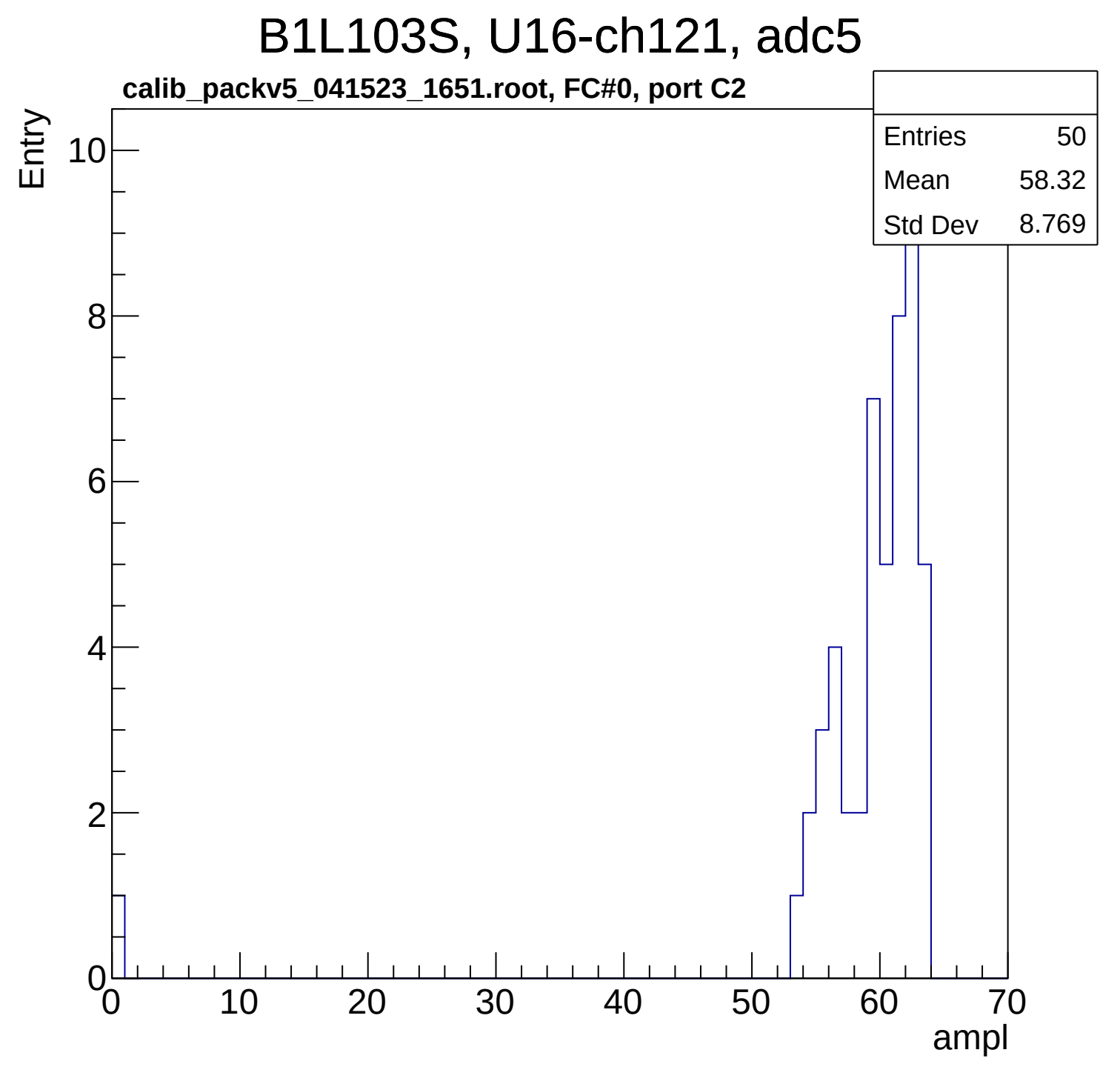
40
50
60
70


B1L103S, U16-ch121, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 47.15
Std Dev 9.341
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch121, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 55.05
Std Dev 2.777
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U16-ch121, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.32
Std Dev 8.769
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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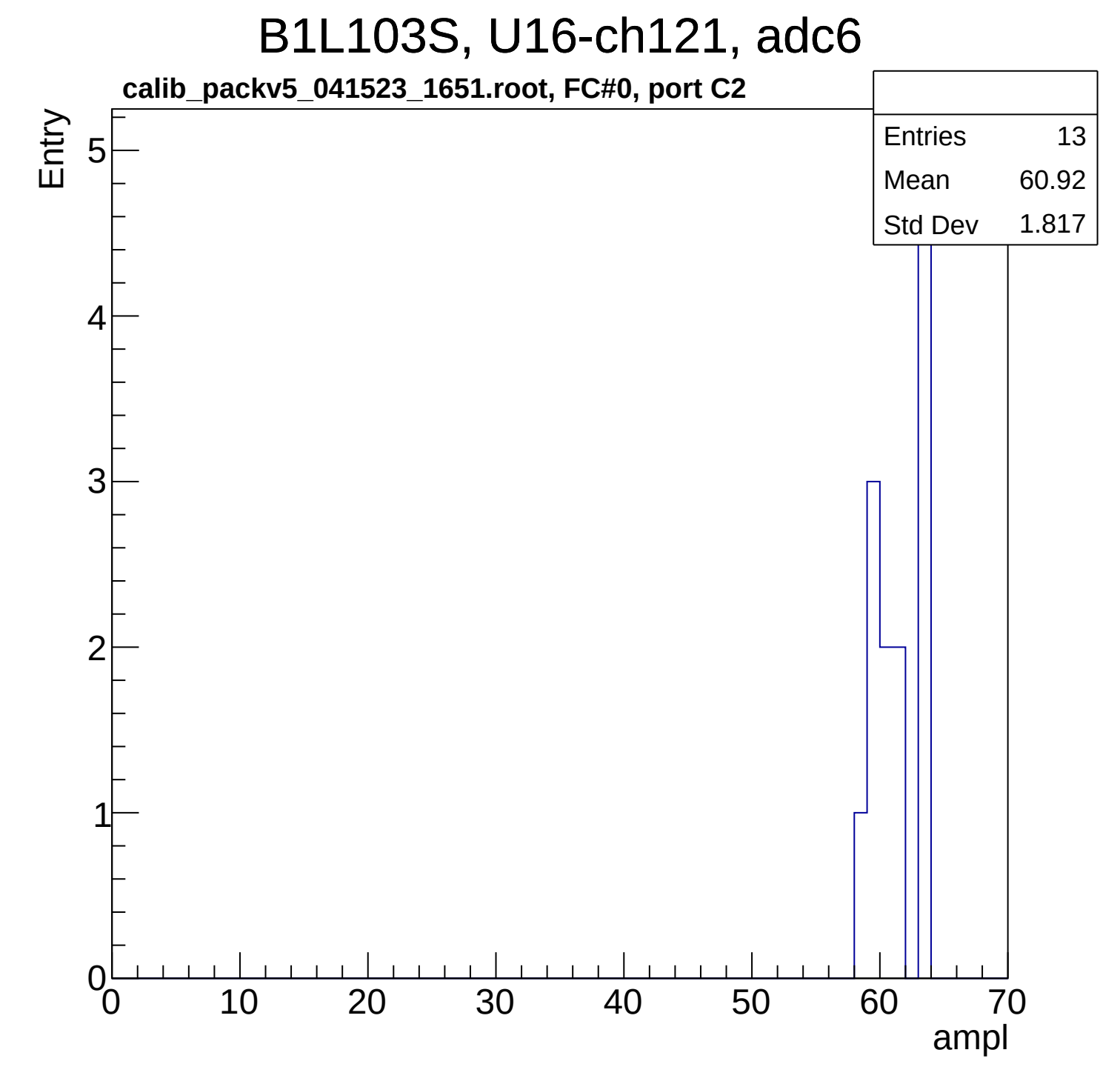
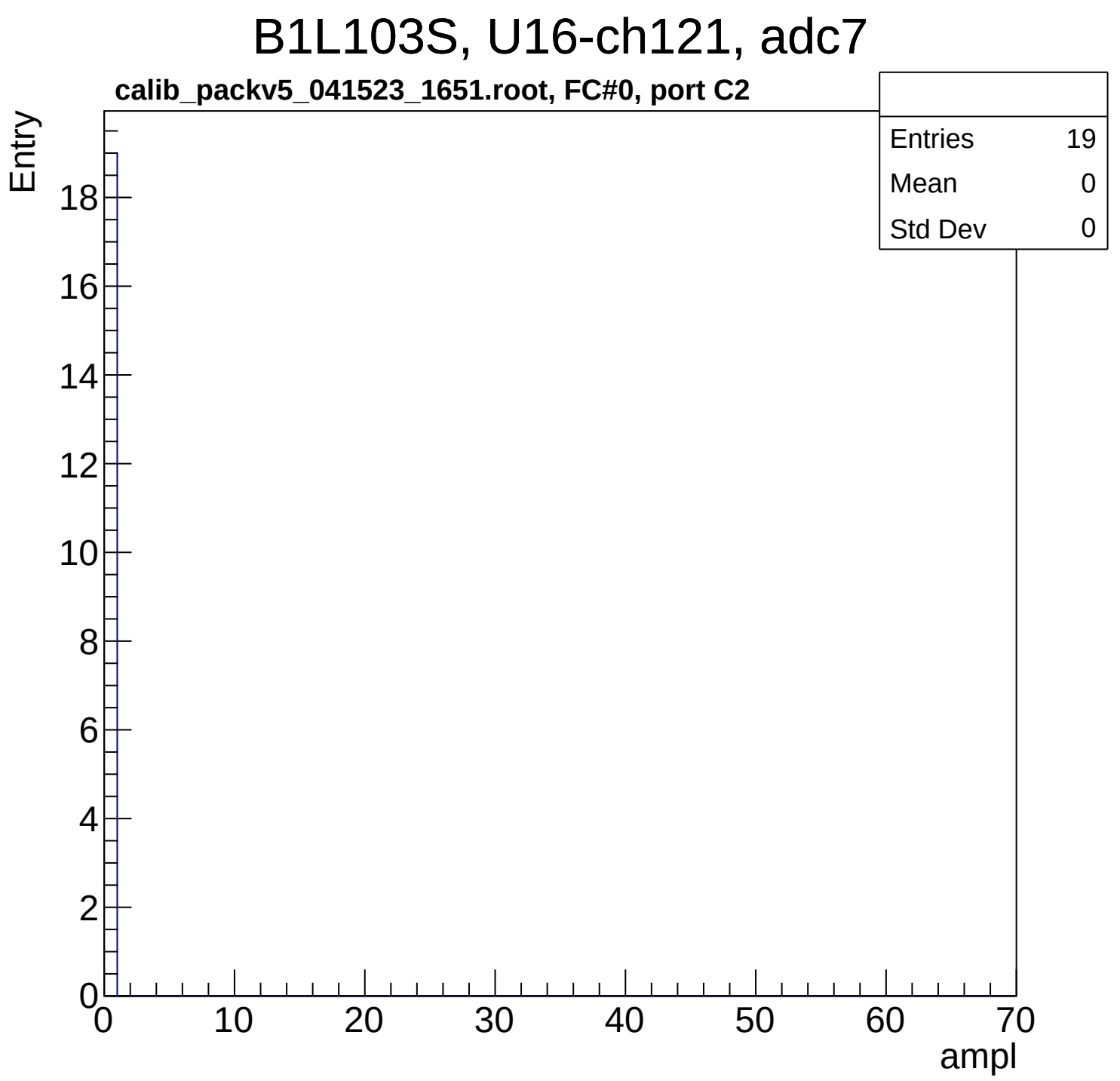
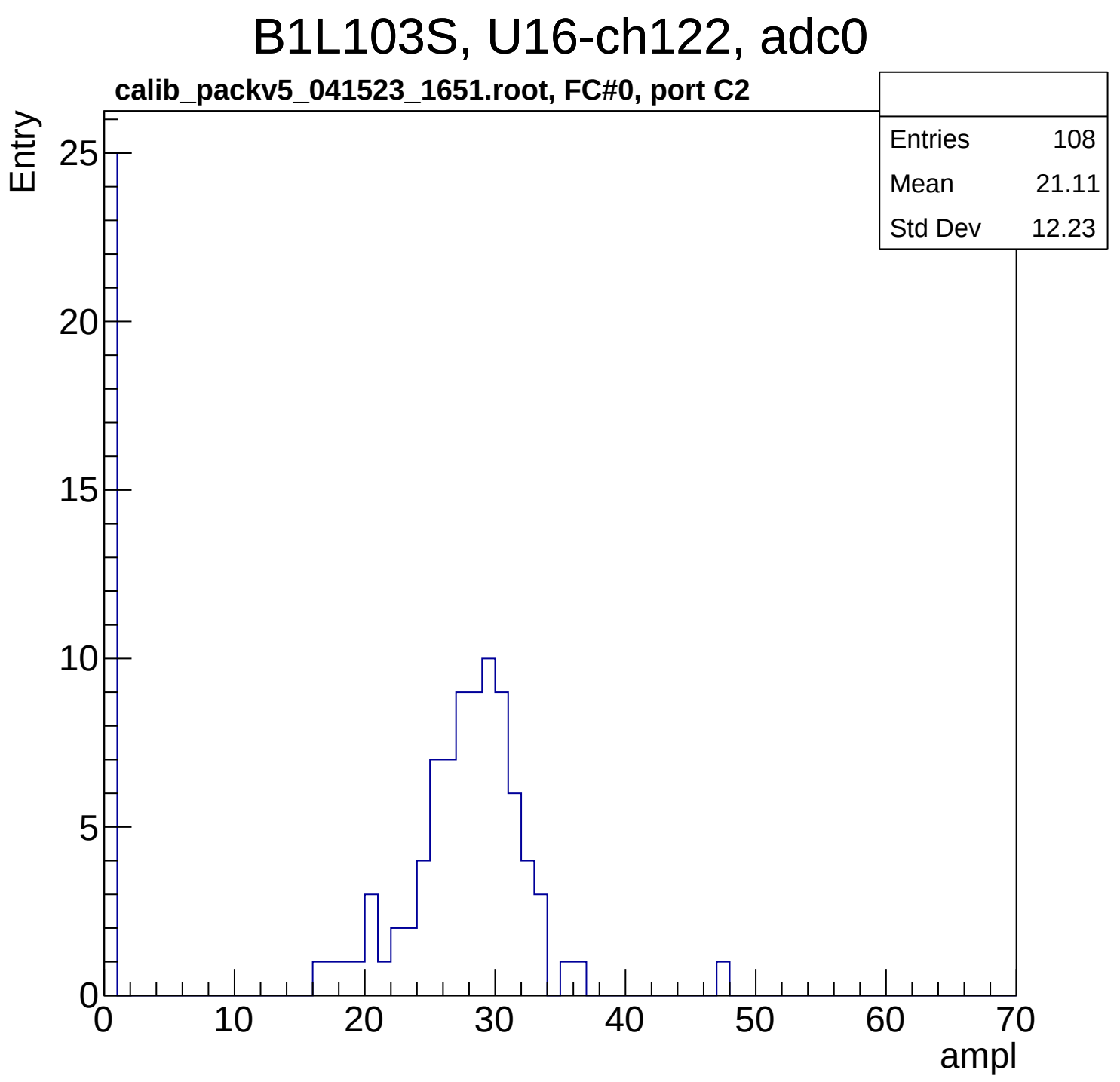
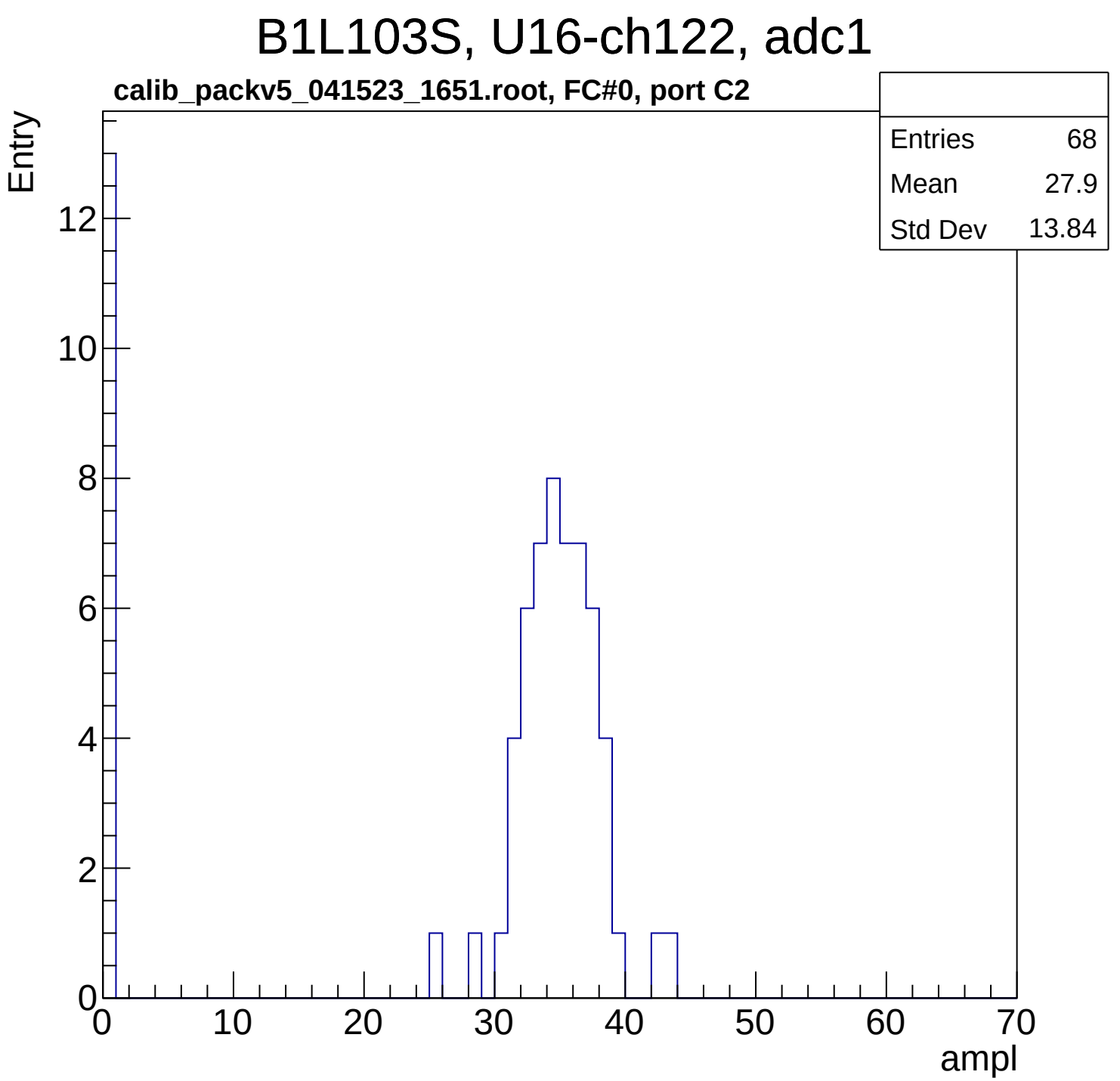

B1L103S, U16-ch121, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 60.92
Std Dev 1.817
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U16-ch121, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch122, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 108
Mean 21.11
Std Dev 12.23
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch122, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 27.9
Std Dev 13.84
Entry
0
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4
6
8
10
12
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10
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30
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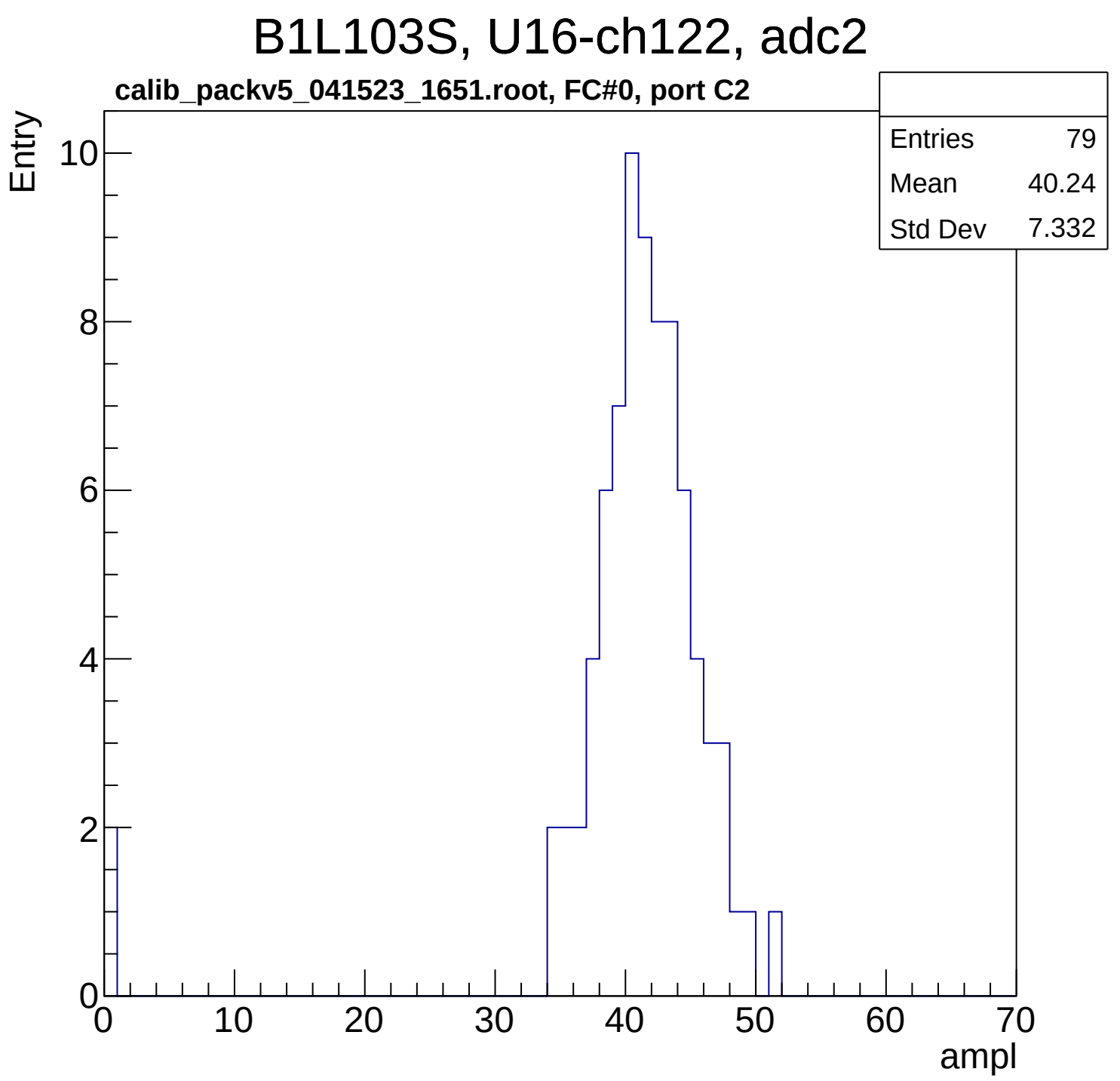
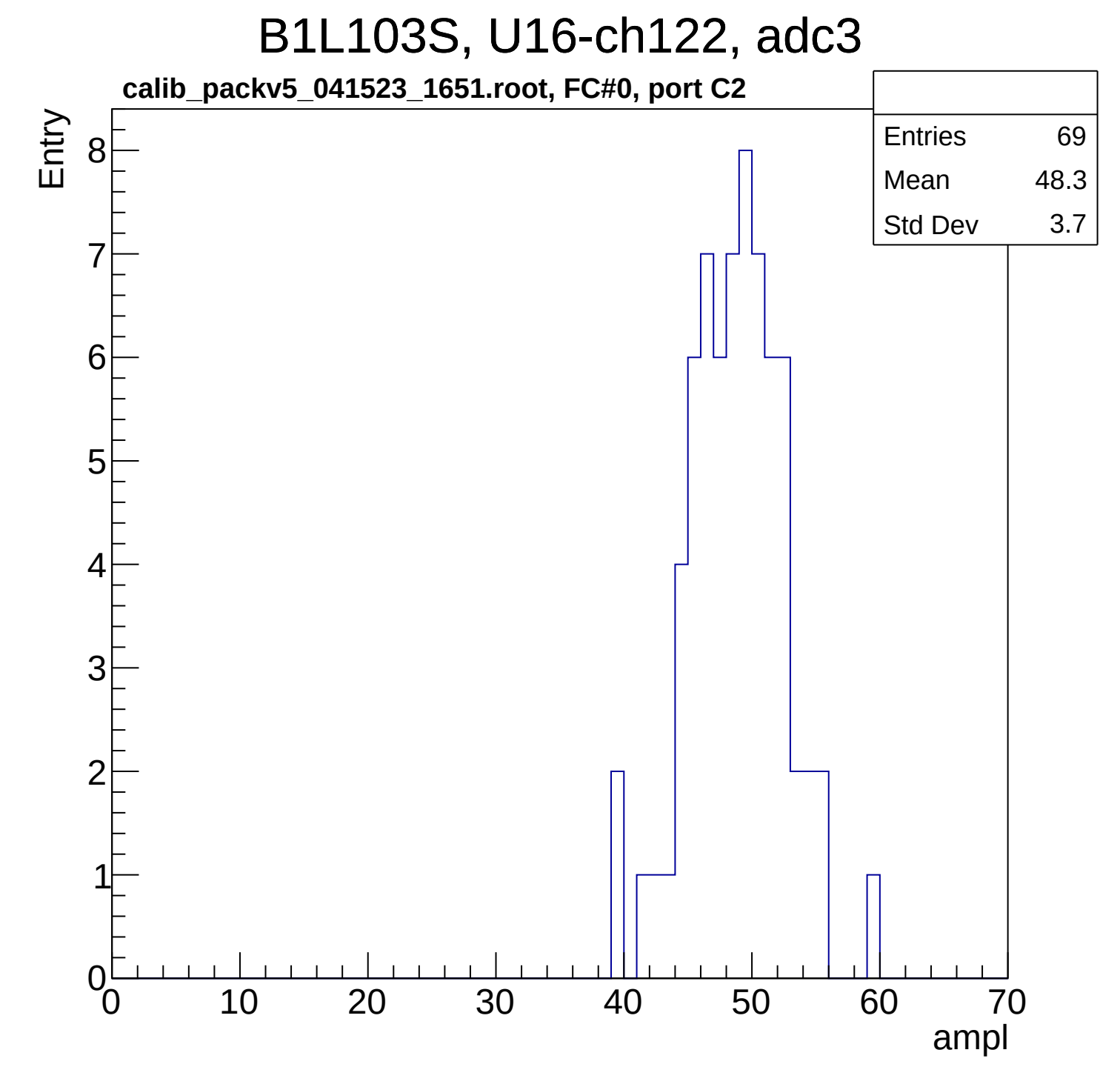
50
60
70
ampl


B1L103S, U16-ch122, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 40.24
Std Dev 7.332
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch122, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 48.3
Std Dev 3.7
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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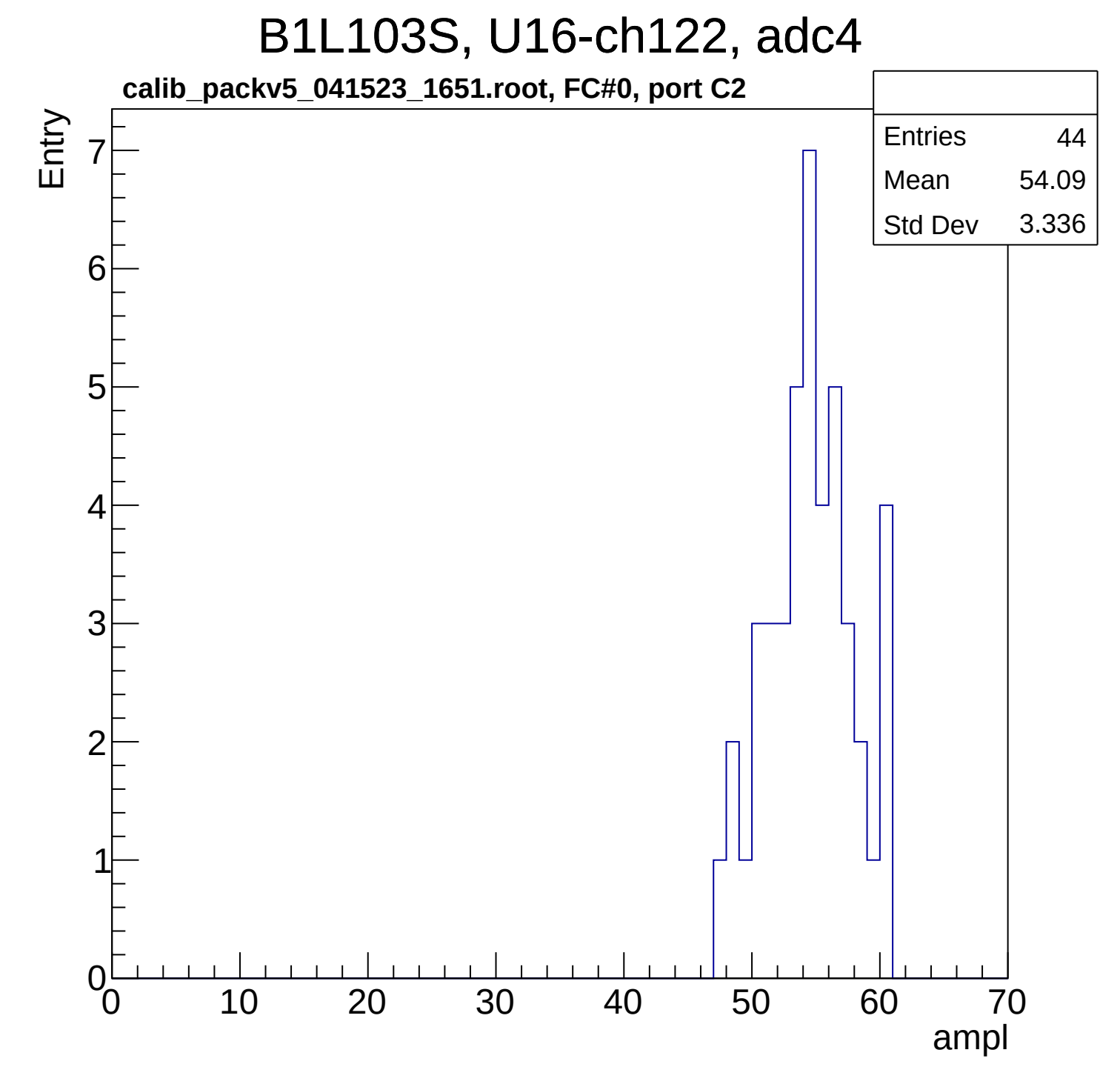
B1L103S, U16-ch122, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 54.09
Std Dev 3.336
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
50
60
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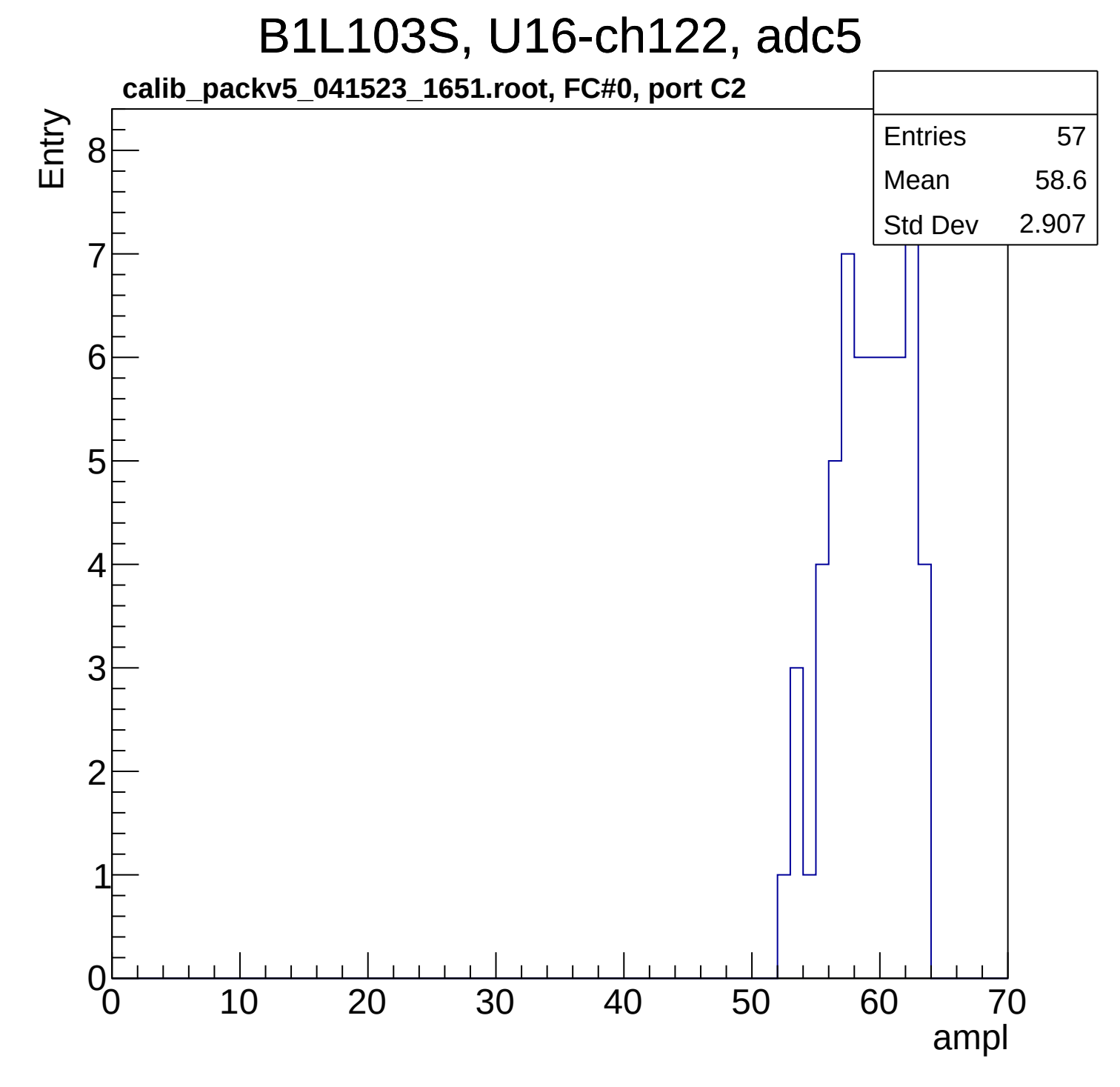
B1L103S, U16-ch122, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.6
Std Dev 2.907
Entry
ampl
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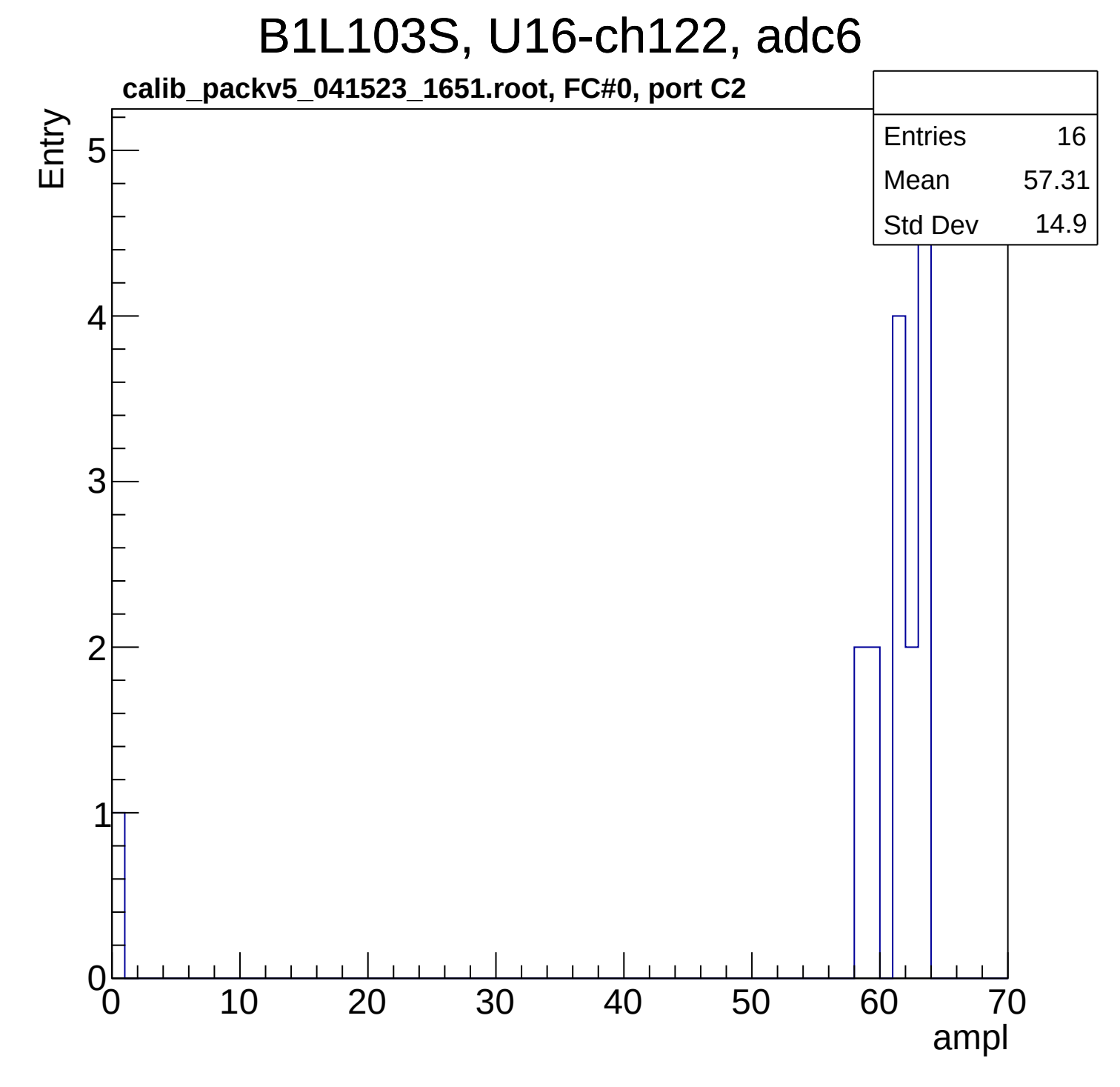
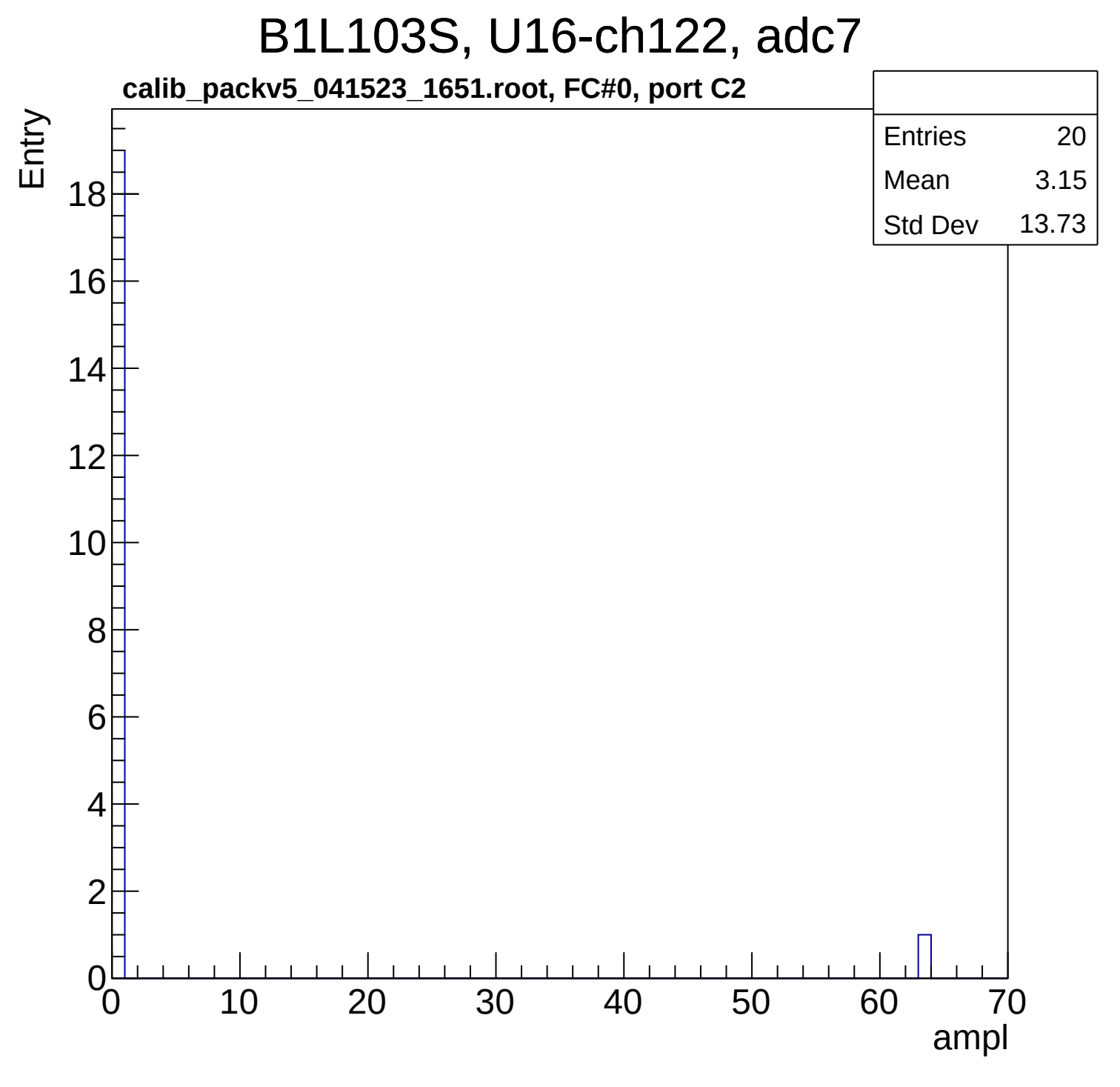
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch122, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.31
Std Dev 14.9
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U16-ch122, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
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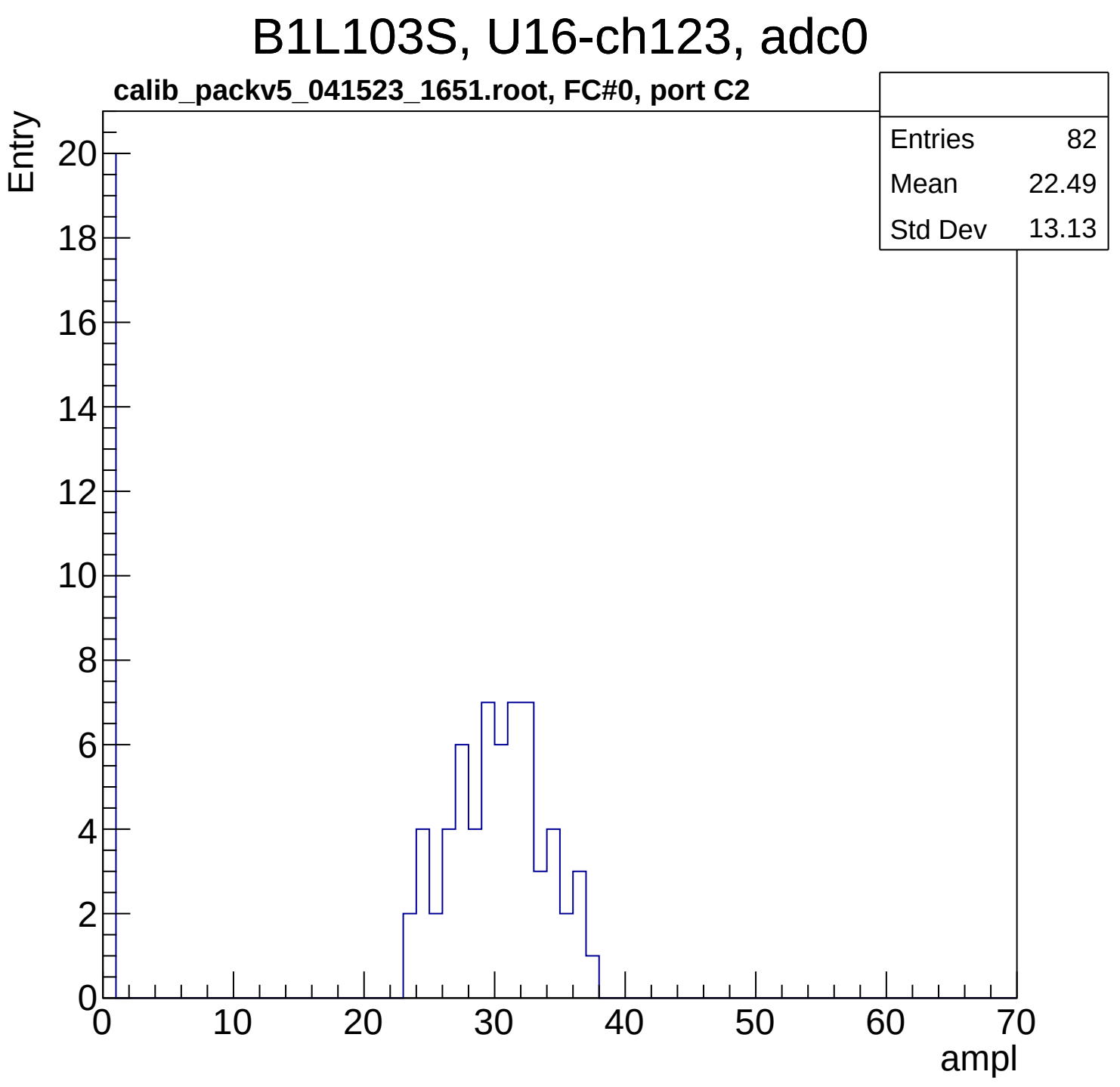
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch123, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 22.49
Std Dev 13.13
Entry
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8
10
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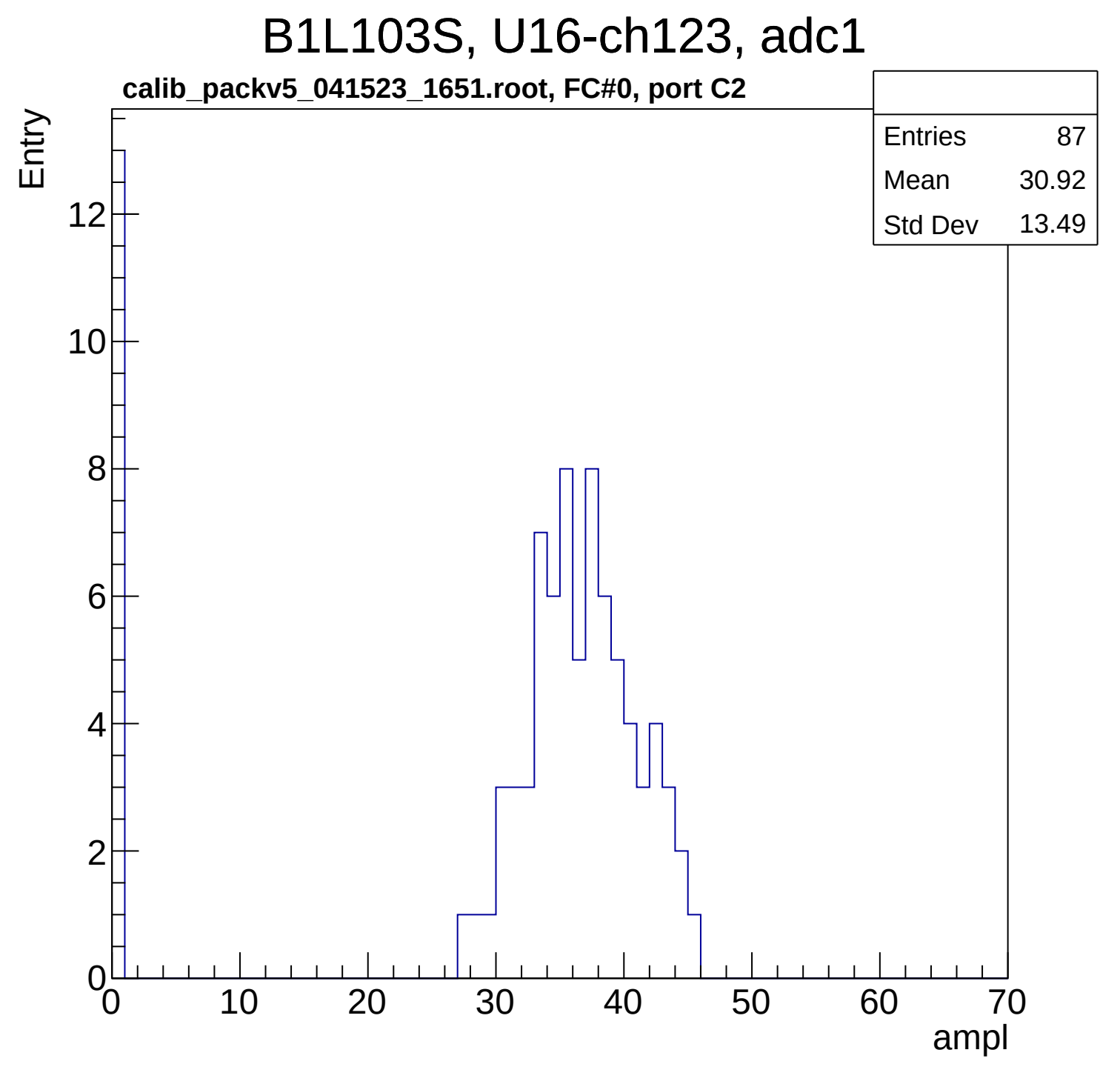
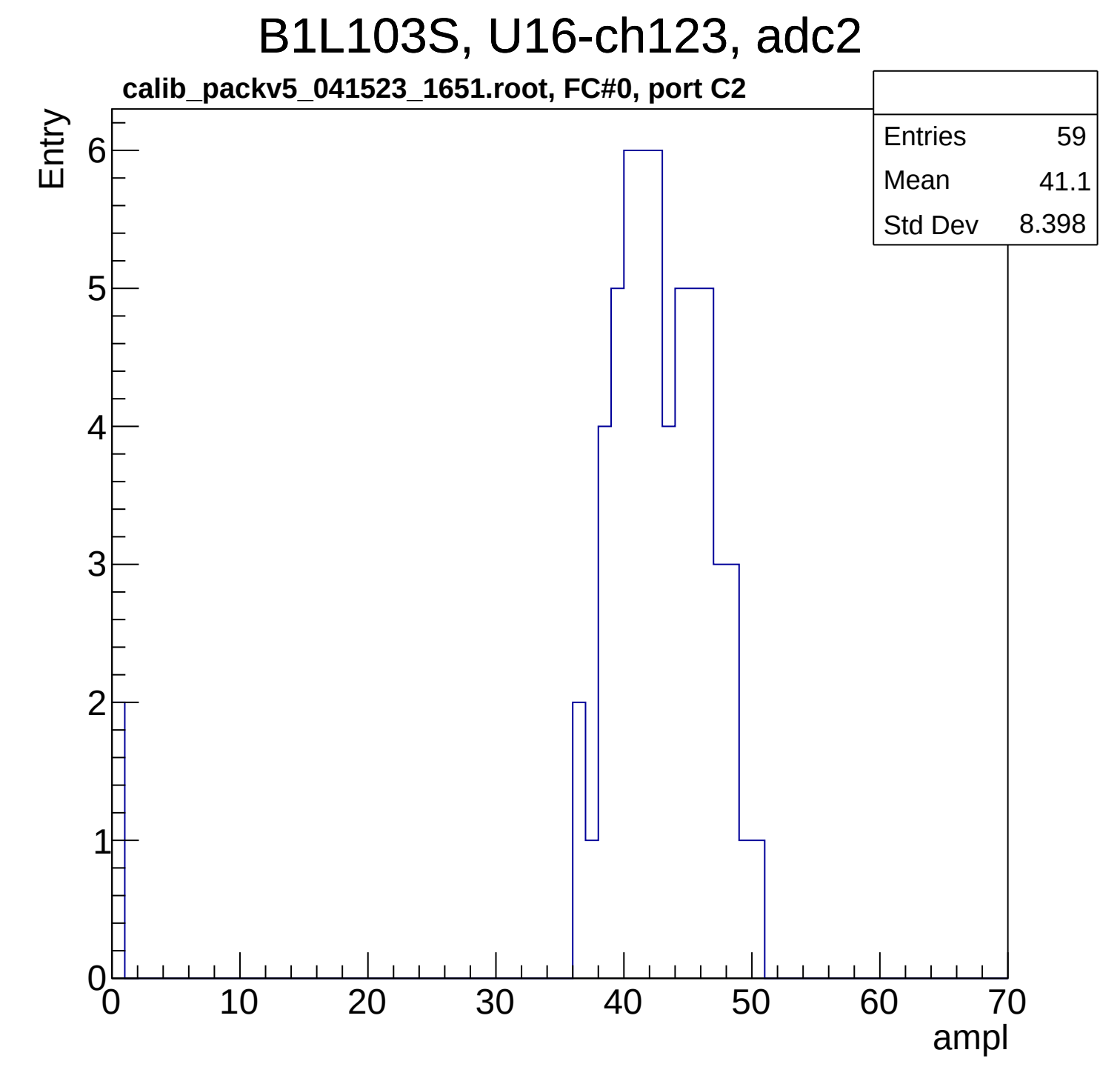
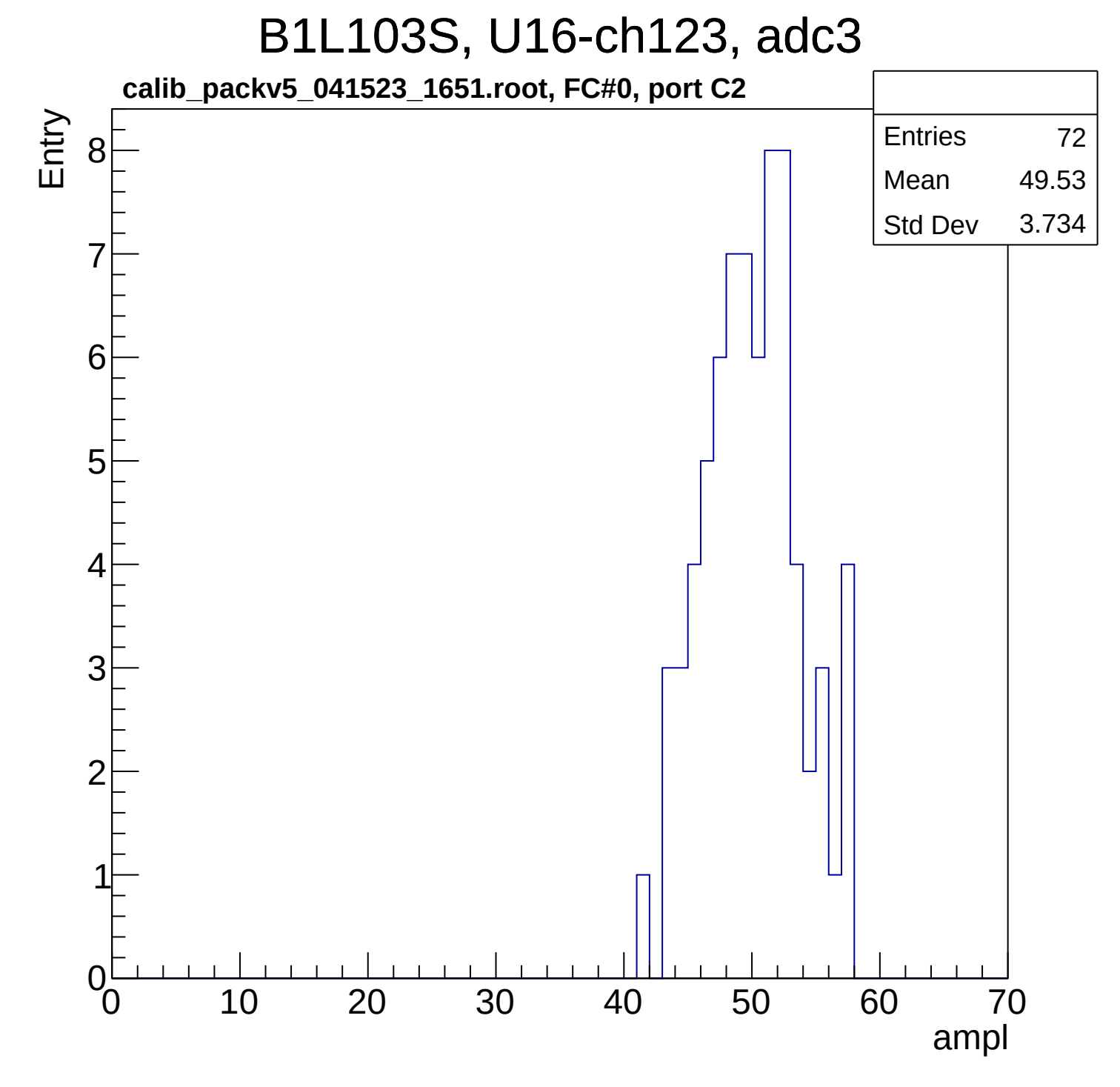
14
16
18
20
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch123, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 30.92
Std Dev 13.49
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch123, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 41.1
Std Dev 8.398
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U16-ch123, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 49.53
Std Dev 3.734
Entry
ampl
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2
3
4
5
6
7
8
0
10
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40
50
60
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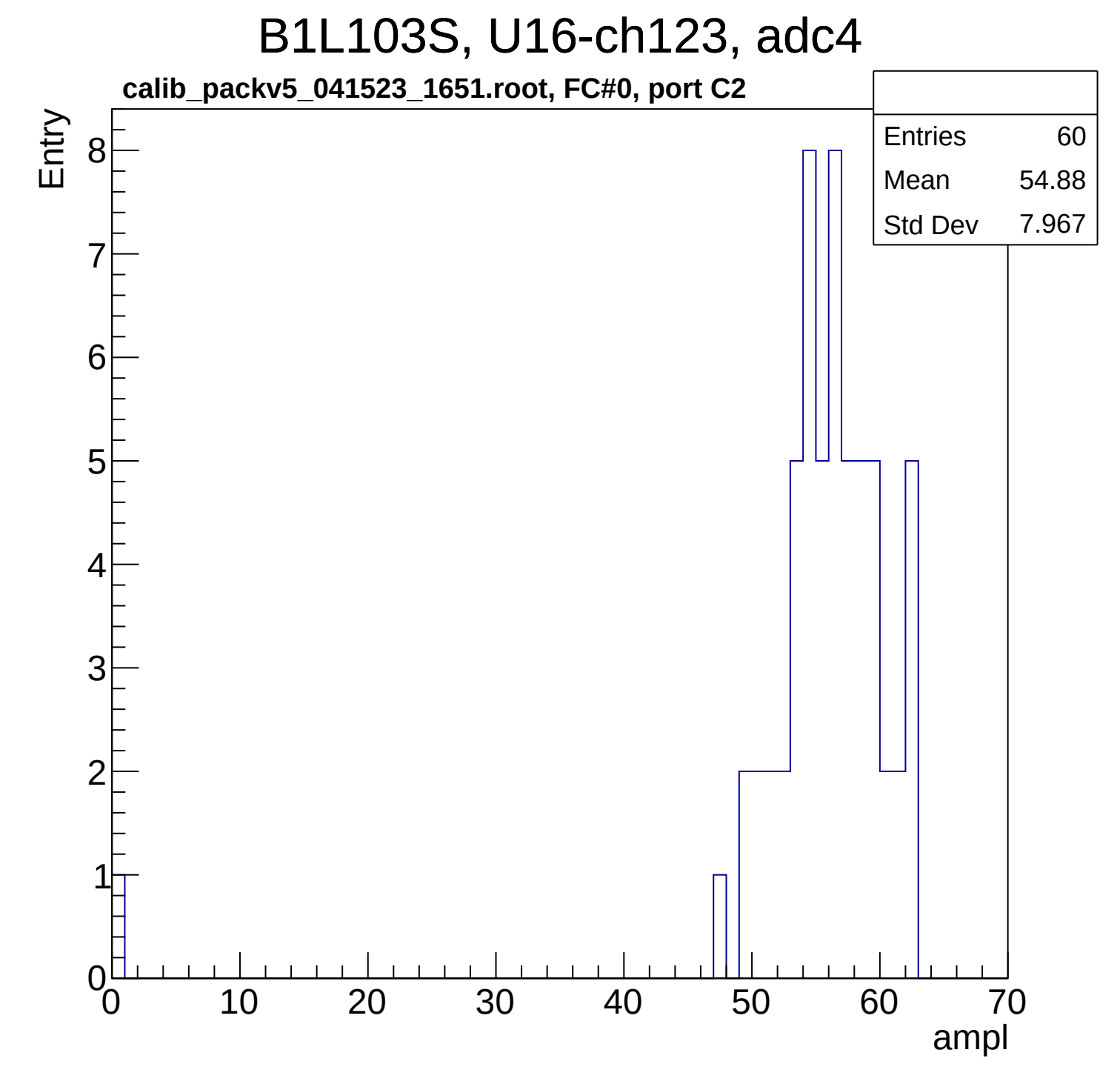
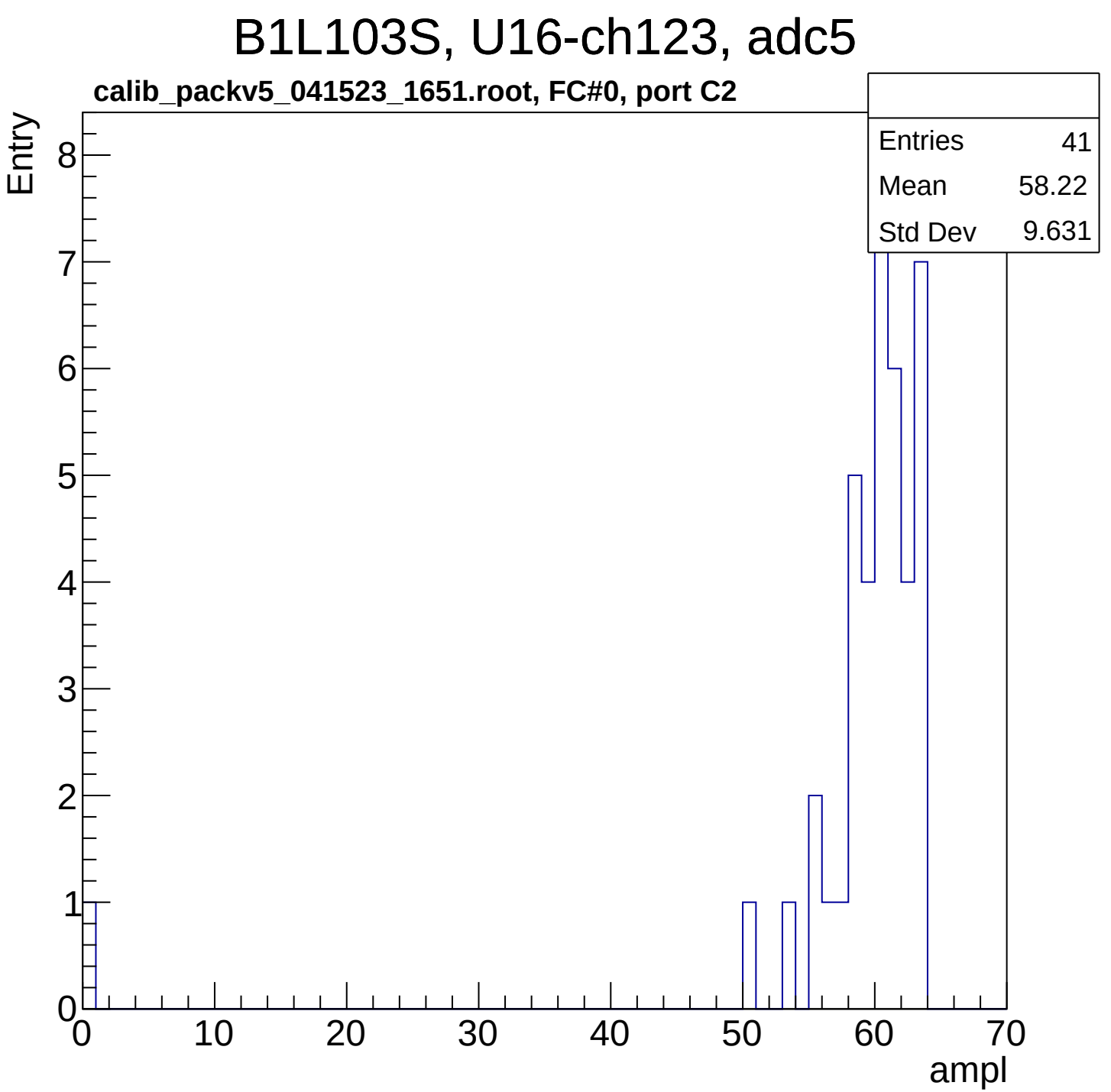

B1L103S, U16-ch123, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 54.88
Std Dev 7.967
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch123, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 58.22
Std Dev 9.631
Entry
ampl
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2
3
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5
6
7
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0
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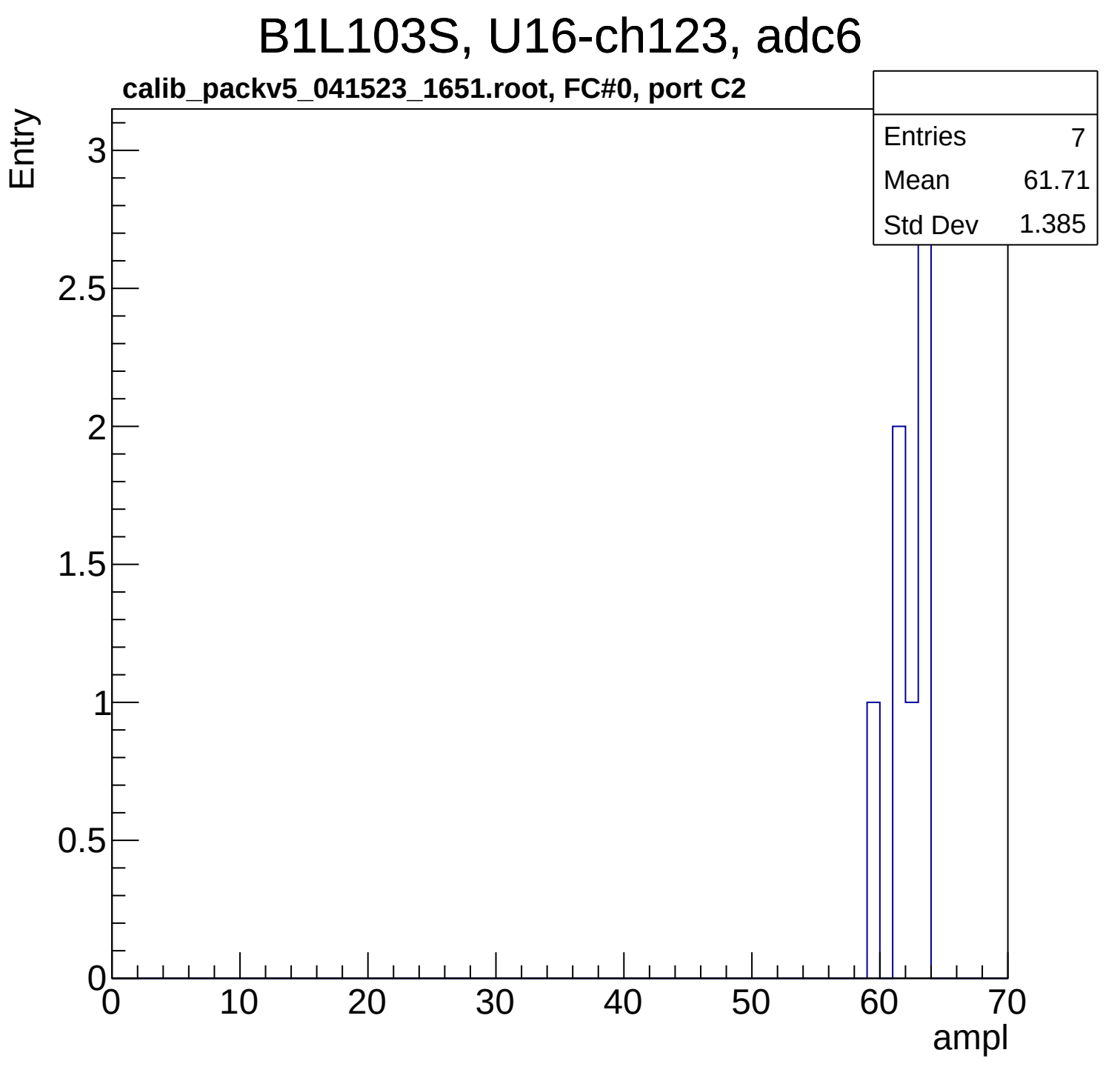
B1L103S, U16-ch123, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.71
Std Dev 1.385
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
50
60
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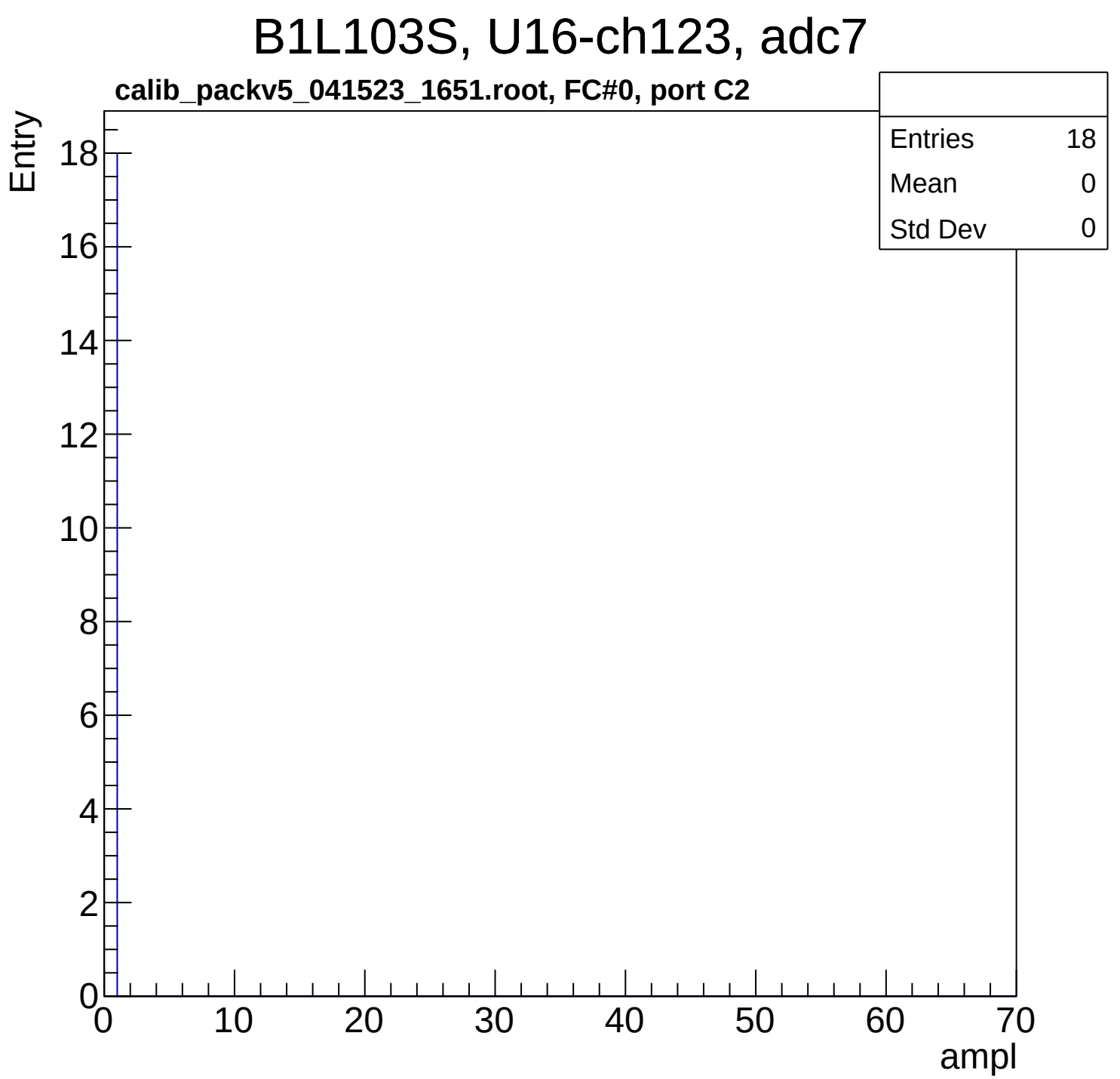
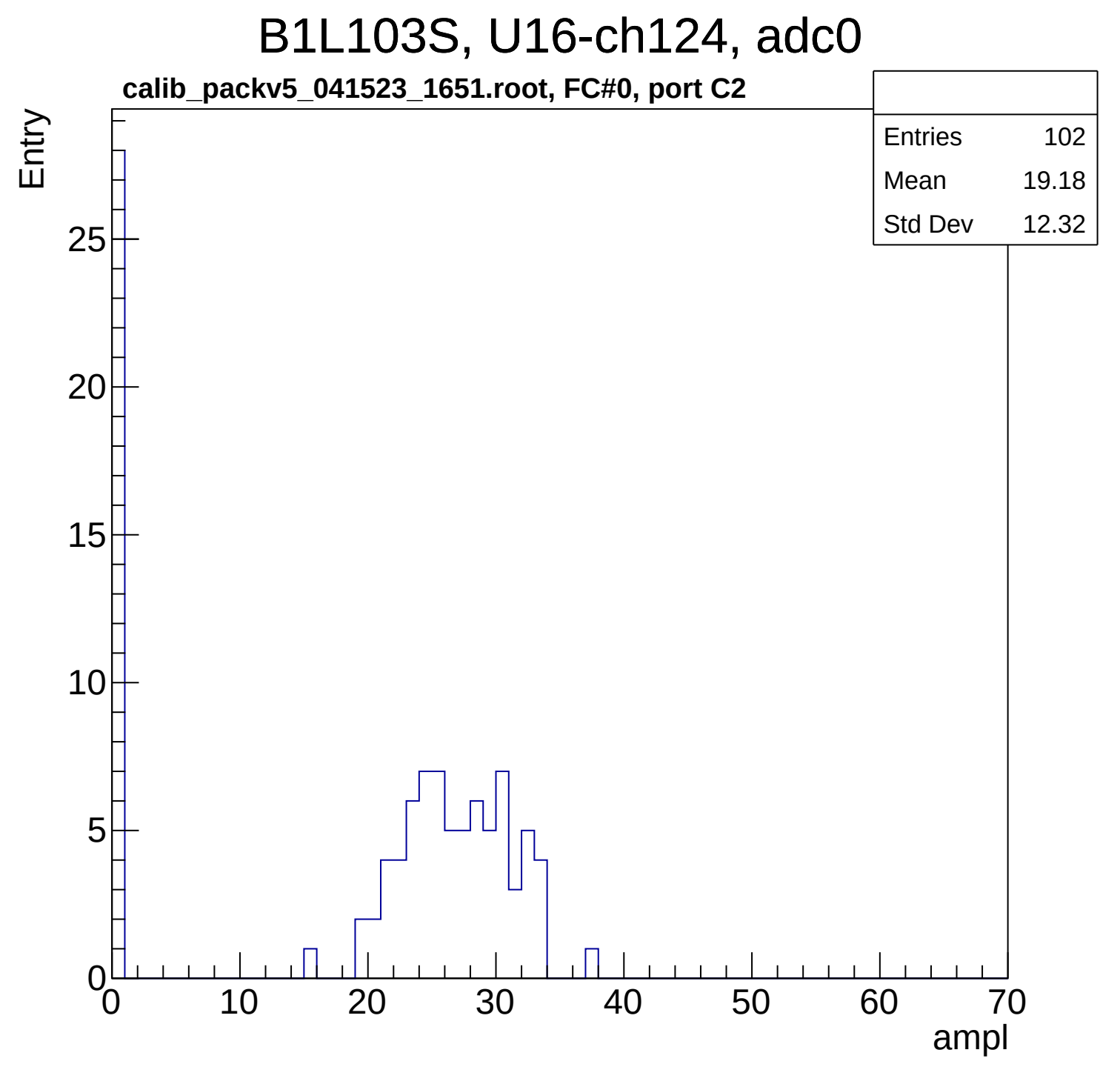
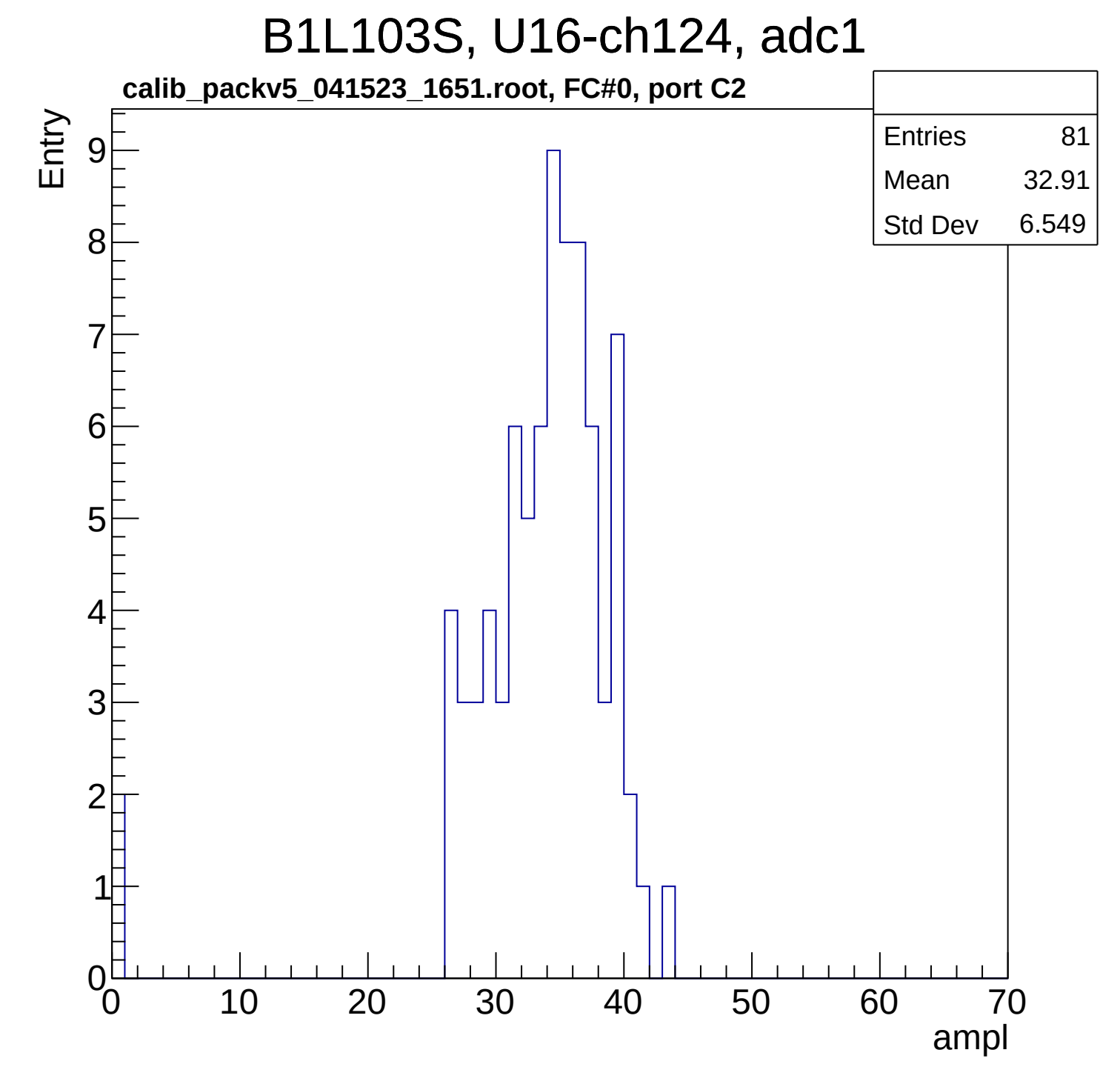

B1L103S, U16-ch123, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch124, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 19.18
Std Dev 12.32
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch124, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 32.91
Std Dev 6.549
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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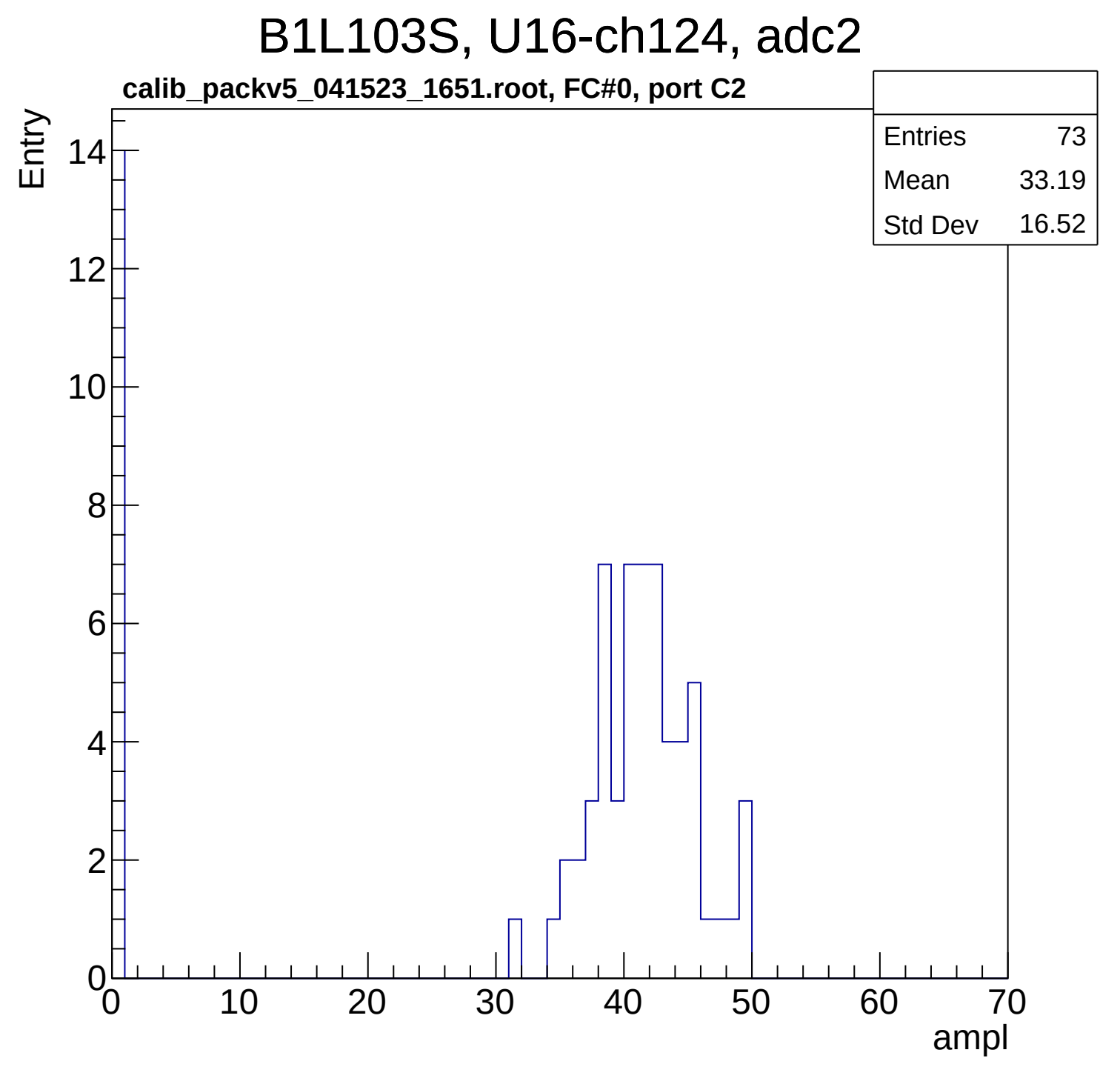
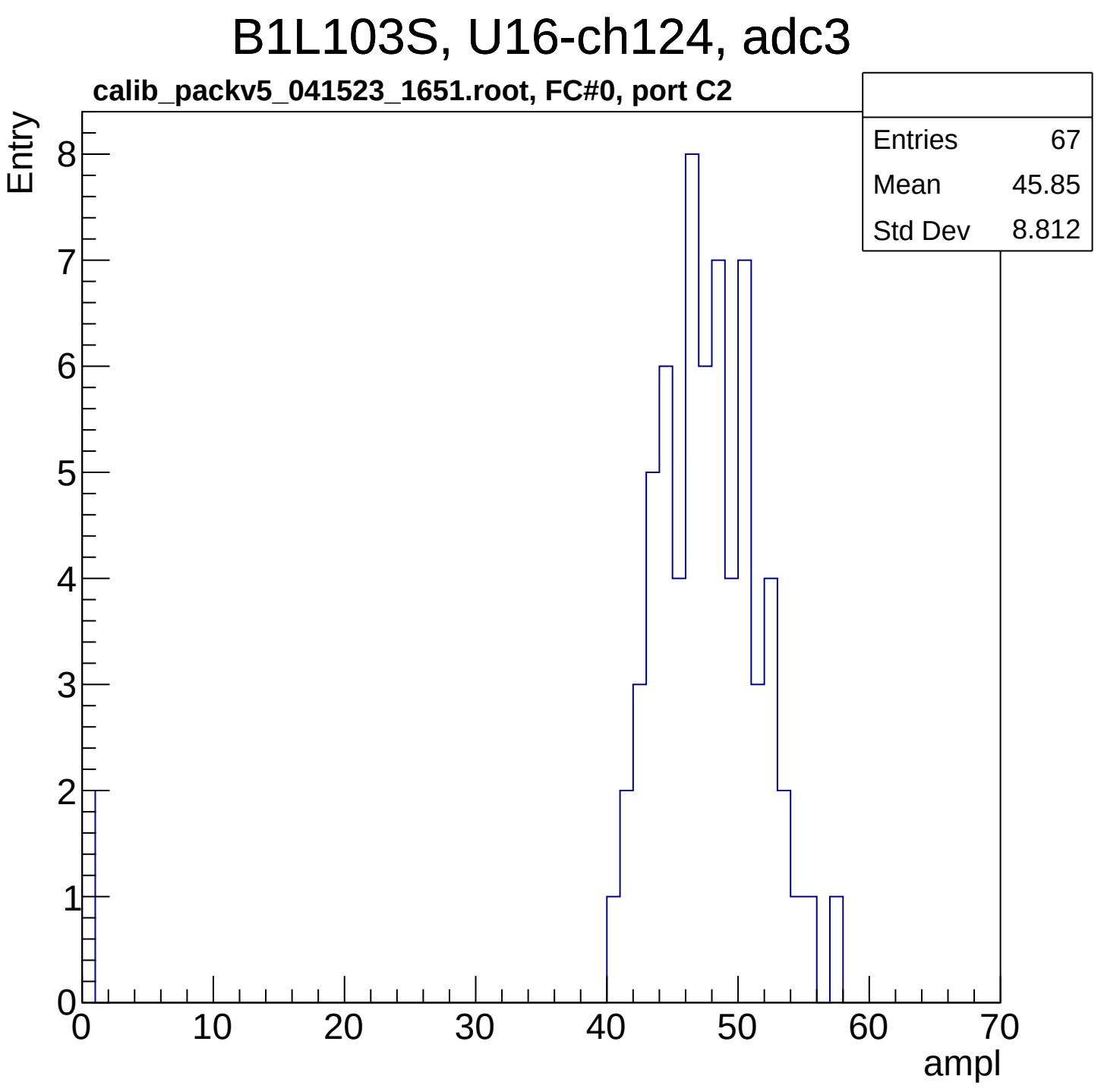

B1L103S, U16-ch124, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 33.19
Std Dev 16.52
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U16-ch124, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 45.85
Std Dev 8.812
Entry
ampl
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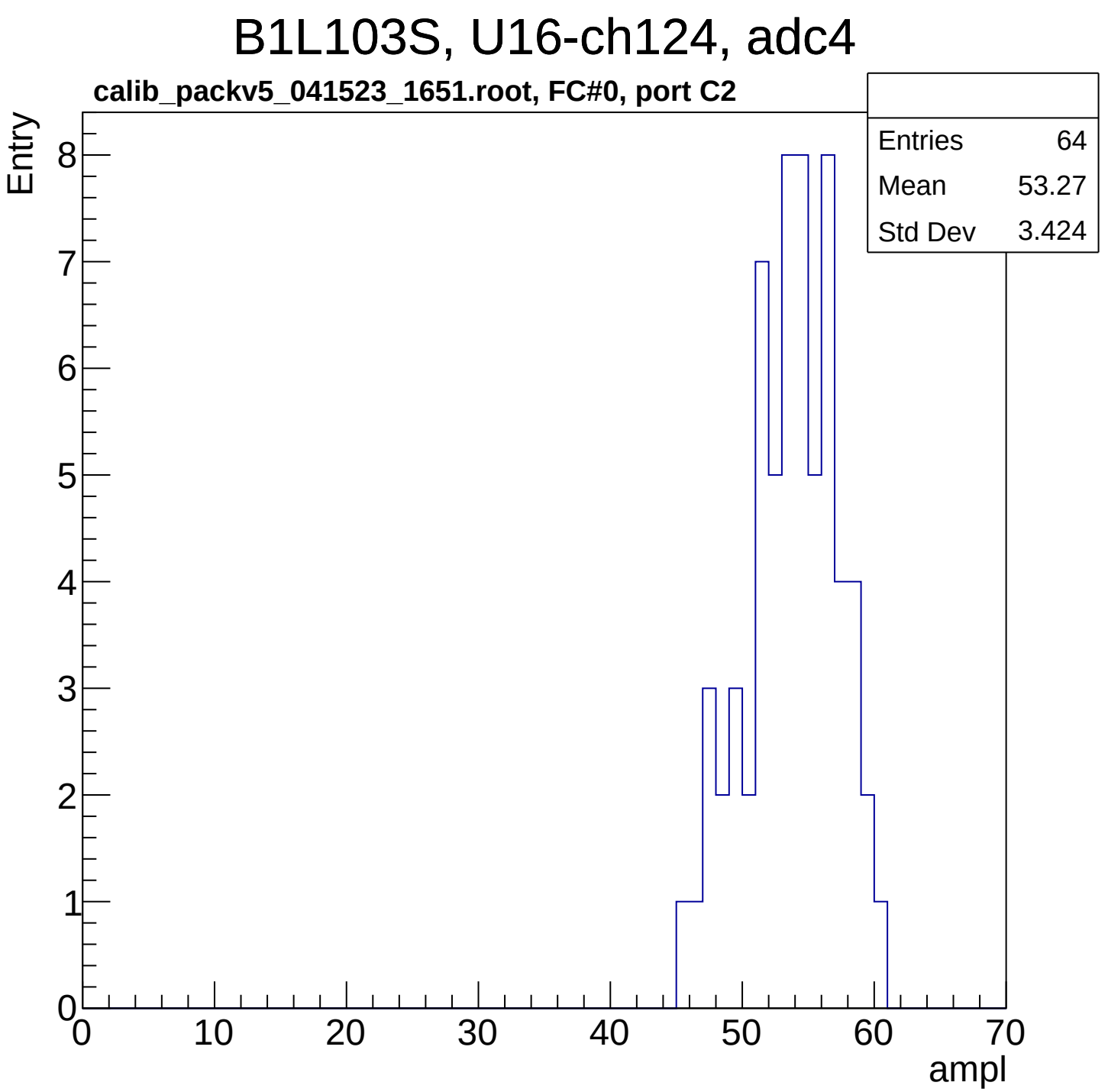
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch124, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 53.27
Std Dev 3.424
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
30
40
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60
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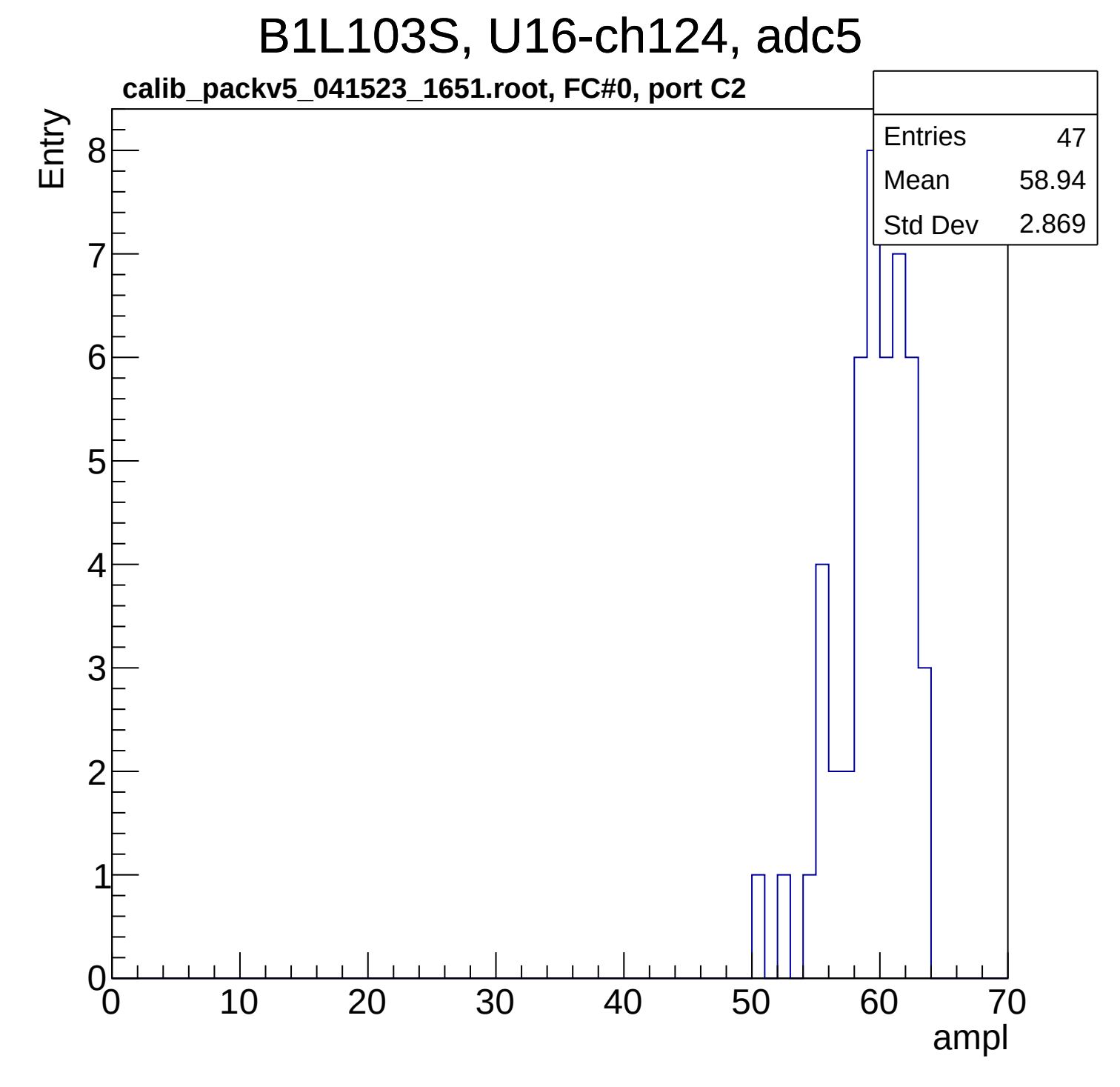
B1L103S, U16-ch124, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.94
Std Dev 2.869
Entry
ampl
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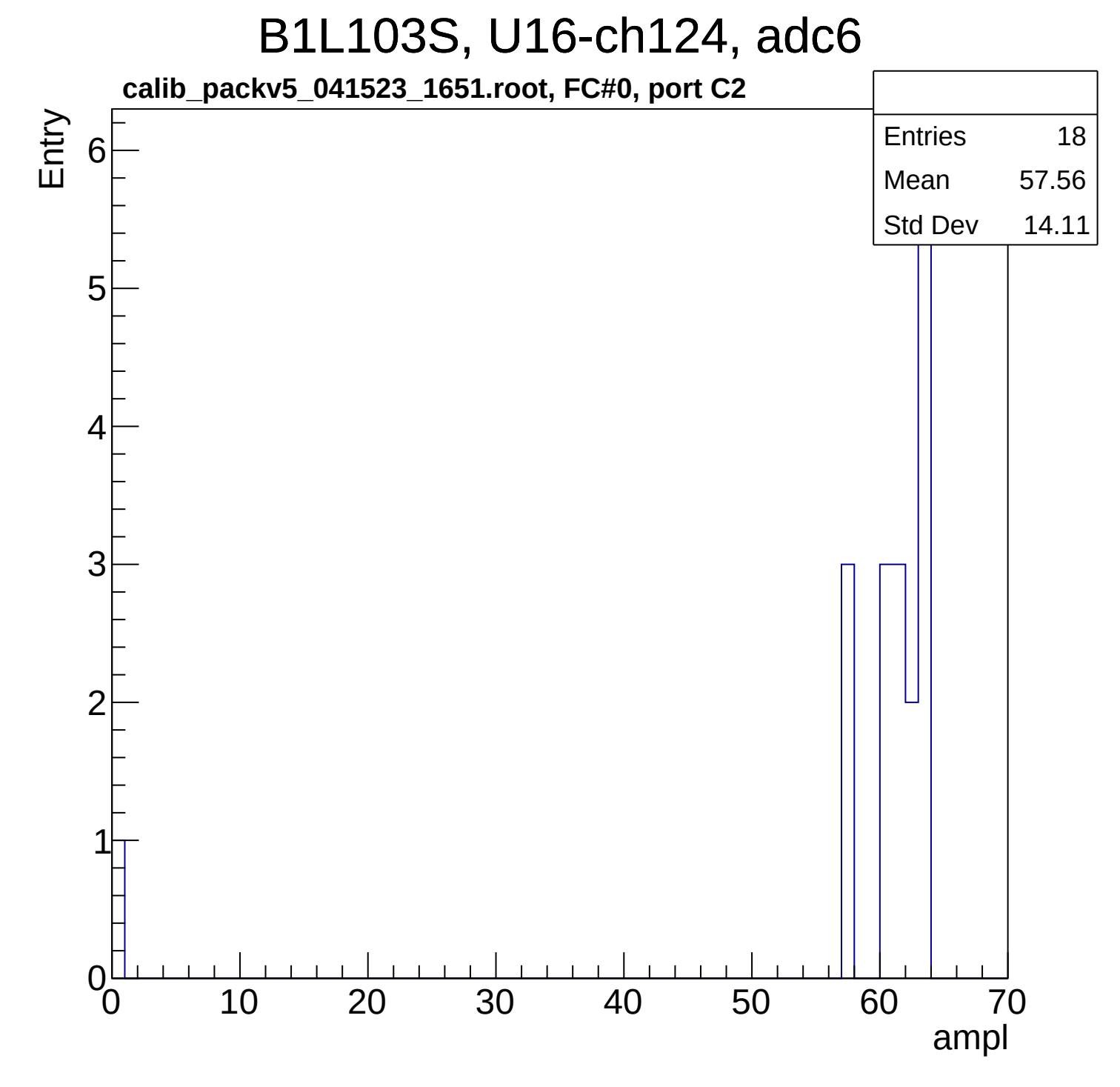
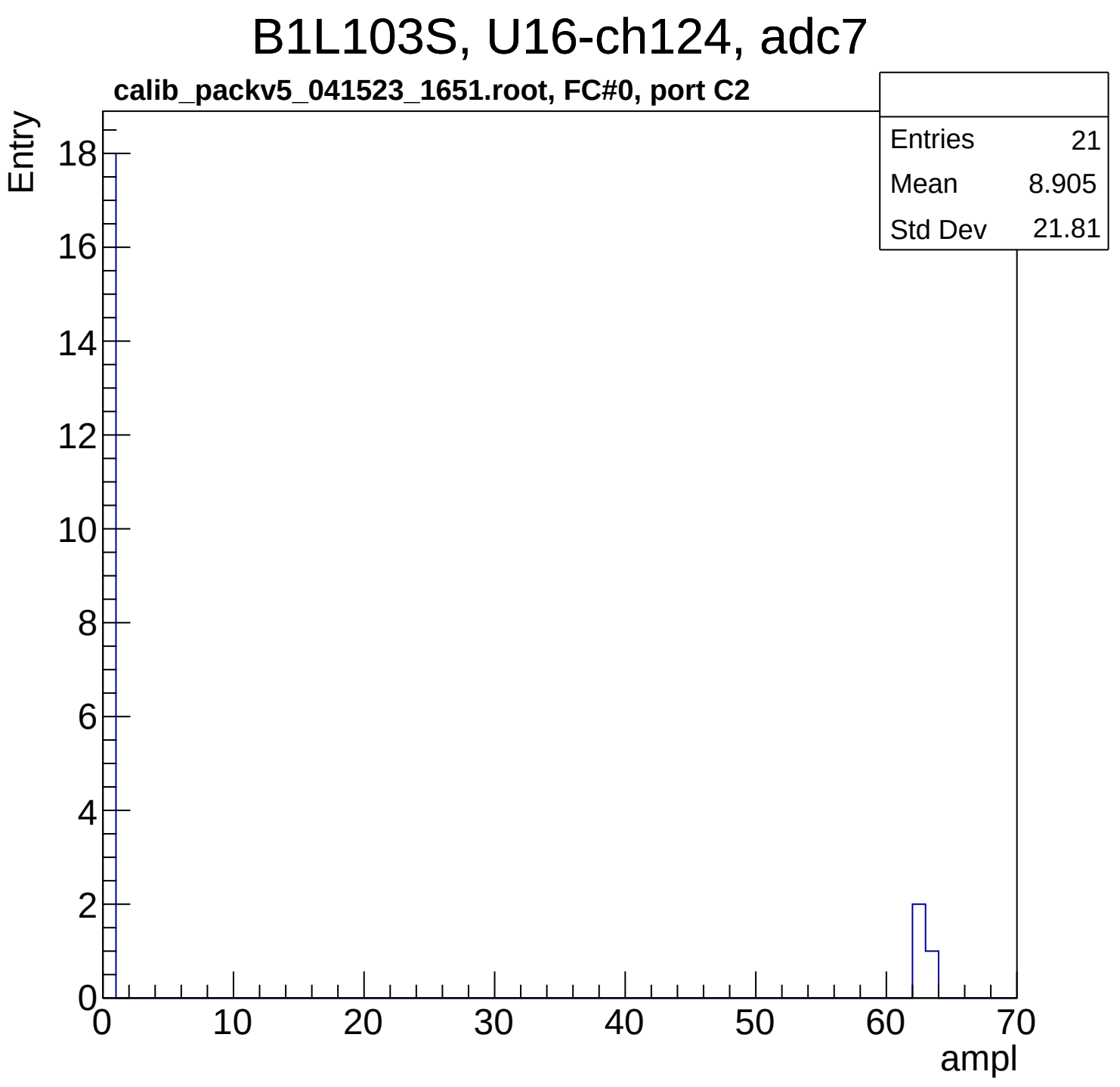
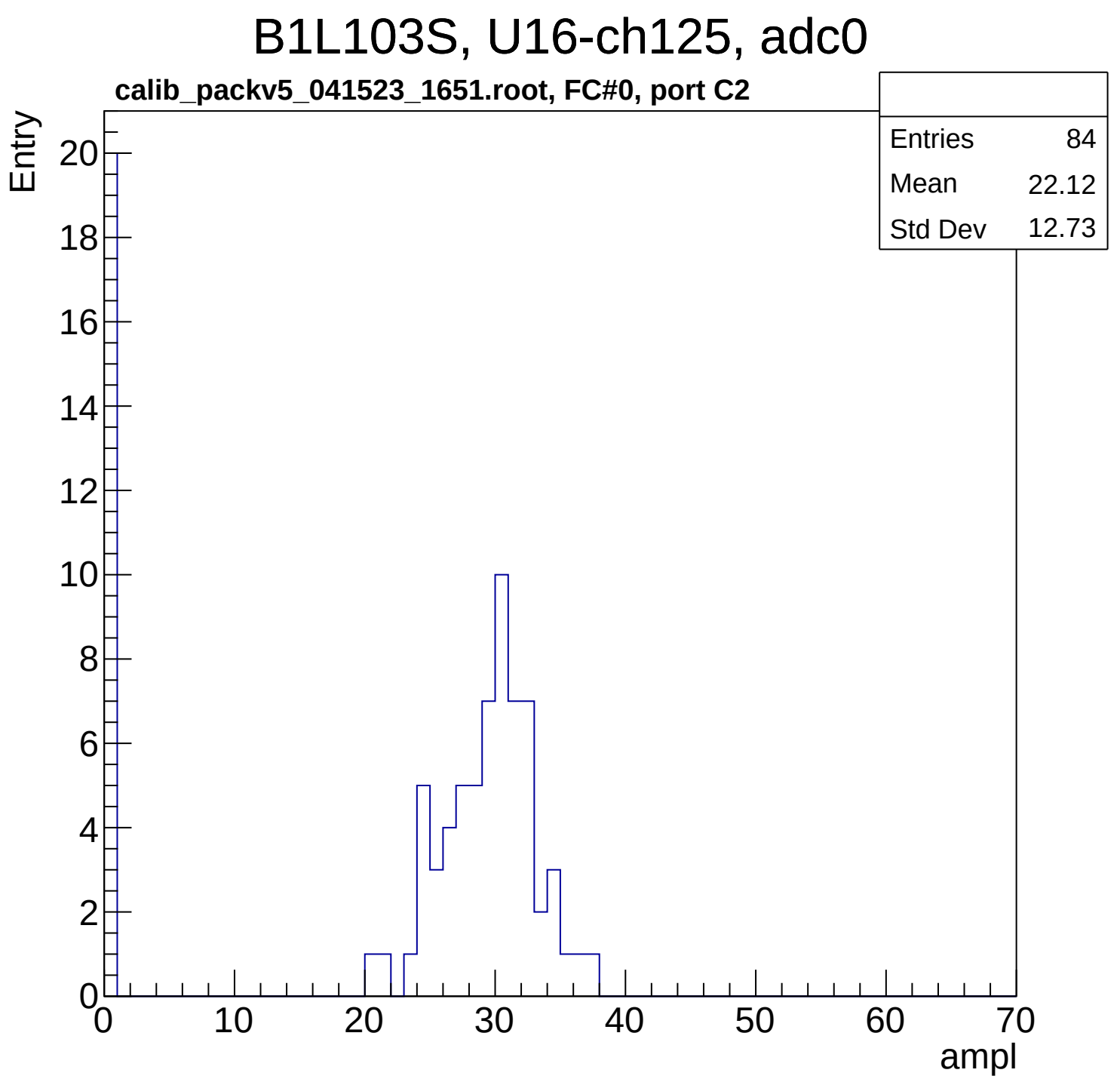
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch124, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 57.56
Std Dev 14.11
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U16-ch124, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 8.905
Std Dev 21.81
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch125, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 22.12
Std Dev 12.73
Entry
ampl
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6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
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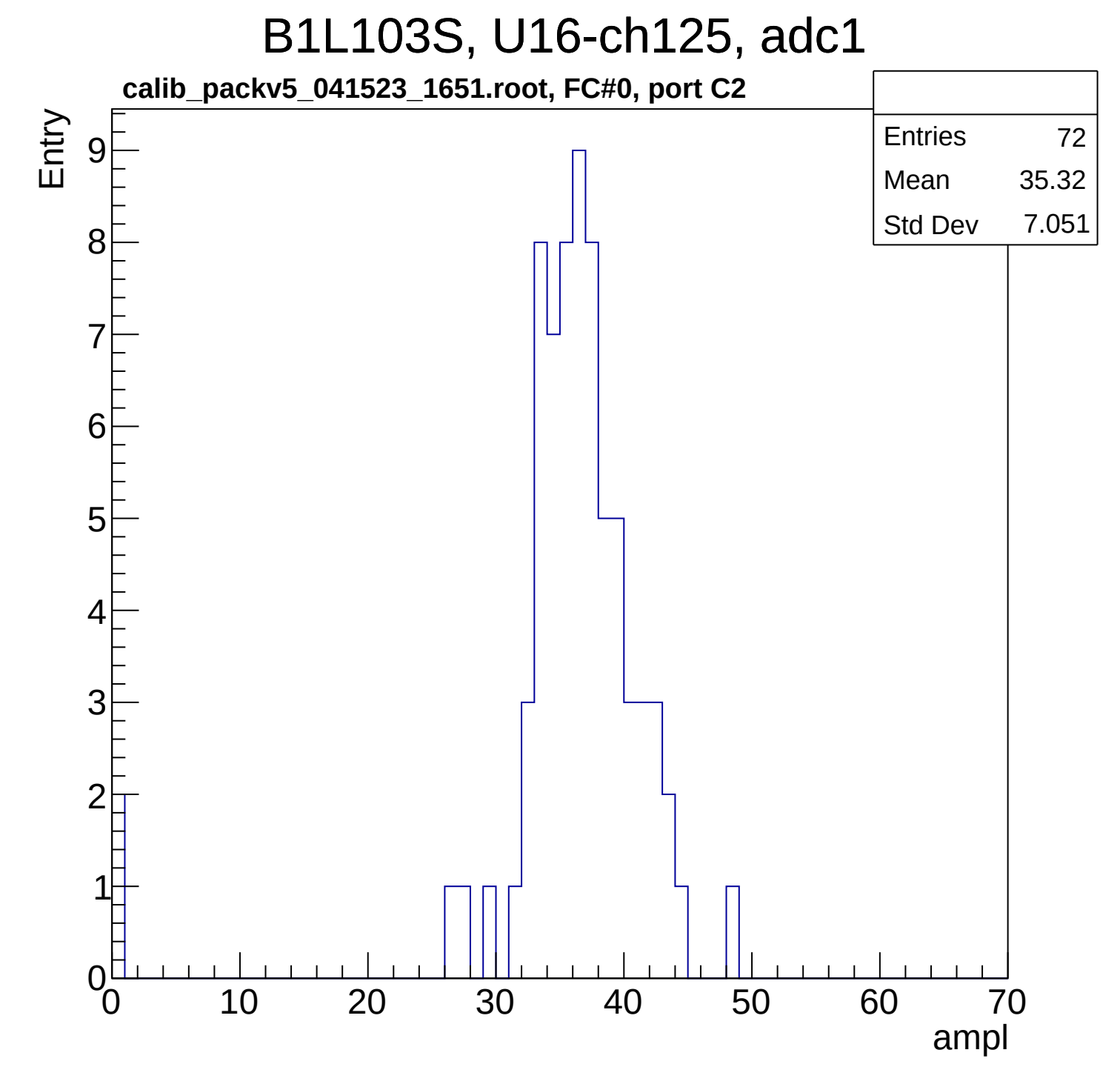
B1L103S, U16-ch125, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 35.32
Std Dev 7.051
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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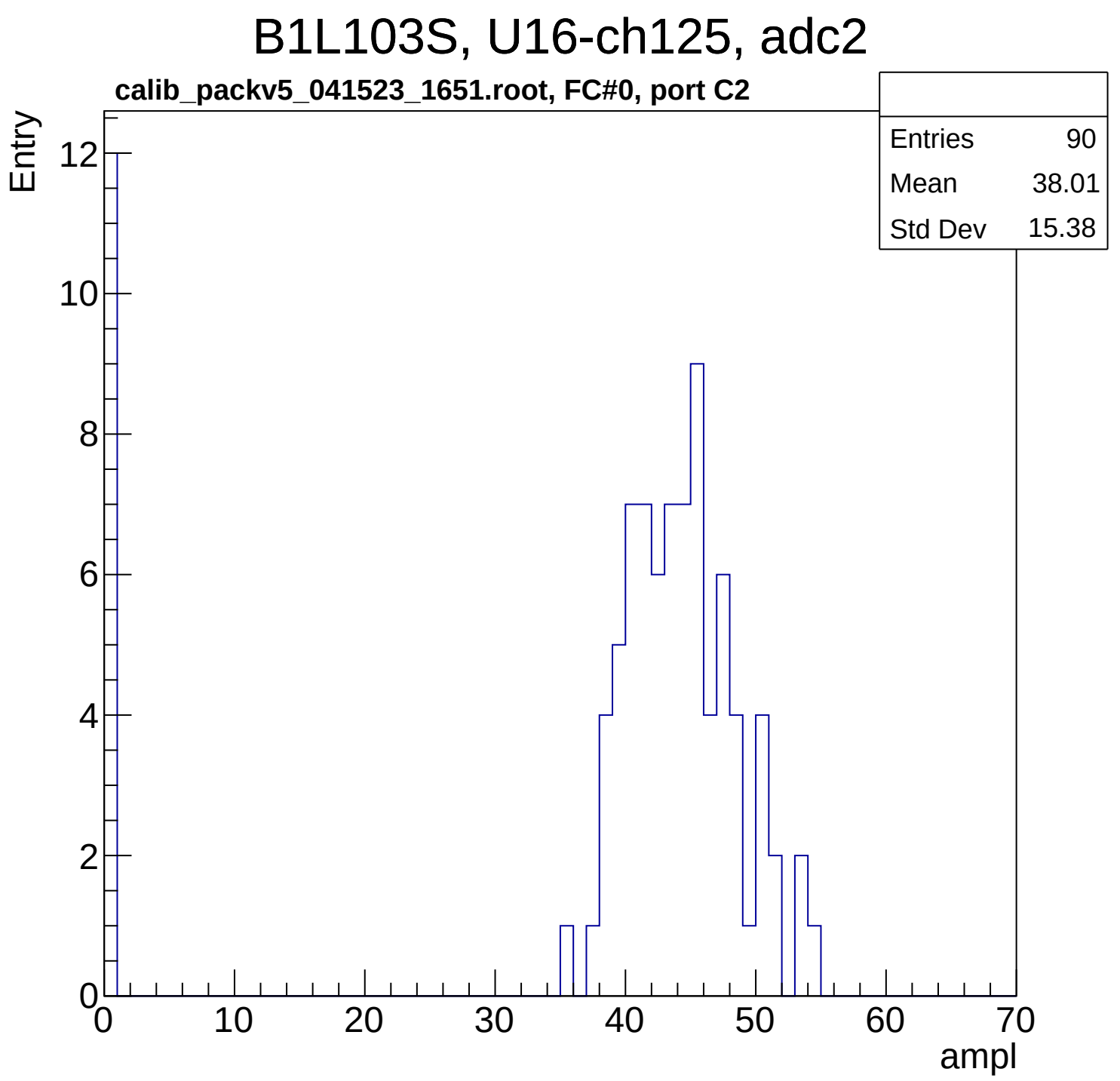
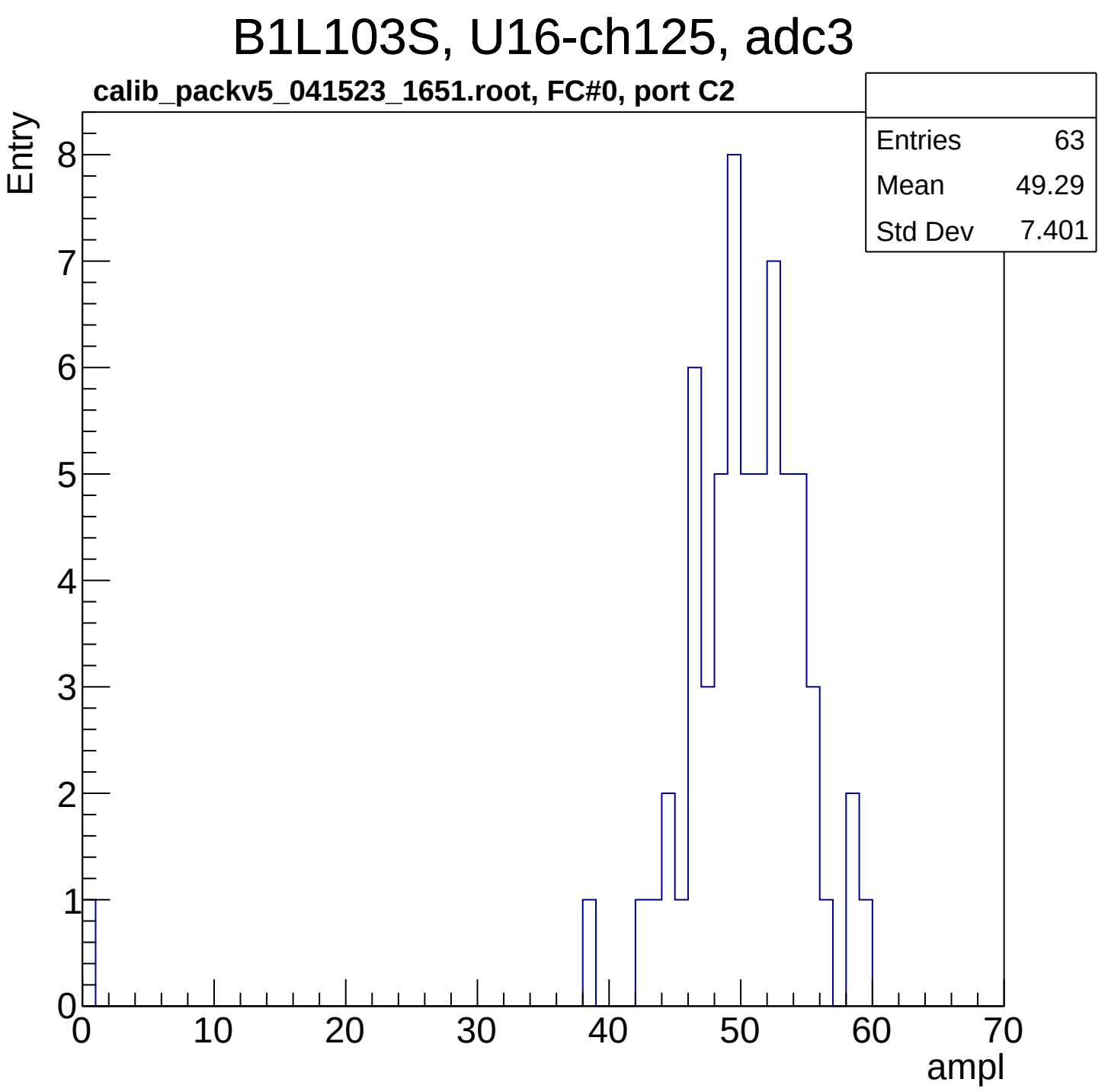

B1L103S, U16-ch125, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 38.01
Std Dev 15.38
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U16-ch125, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 49.29
Std Dev 7.401
Entry
ampl
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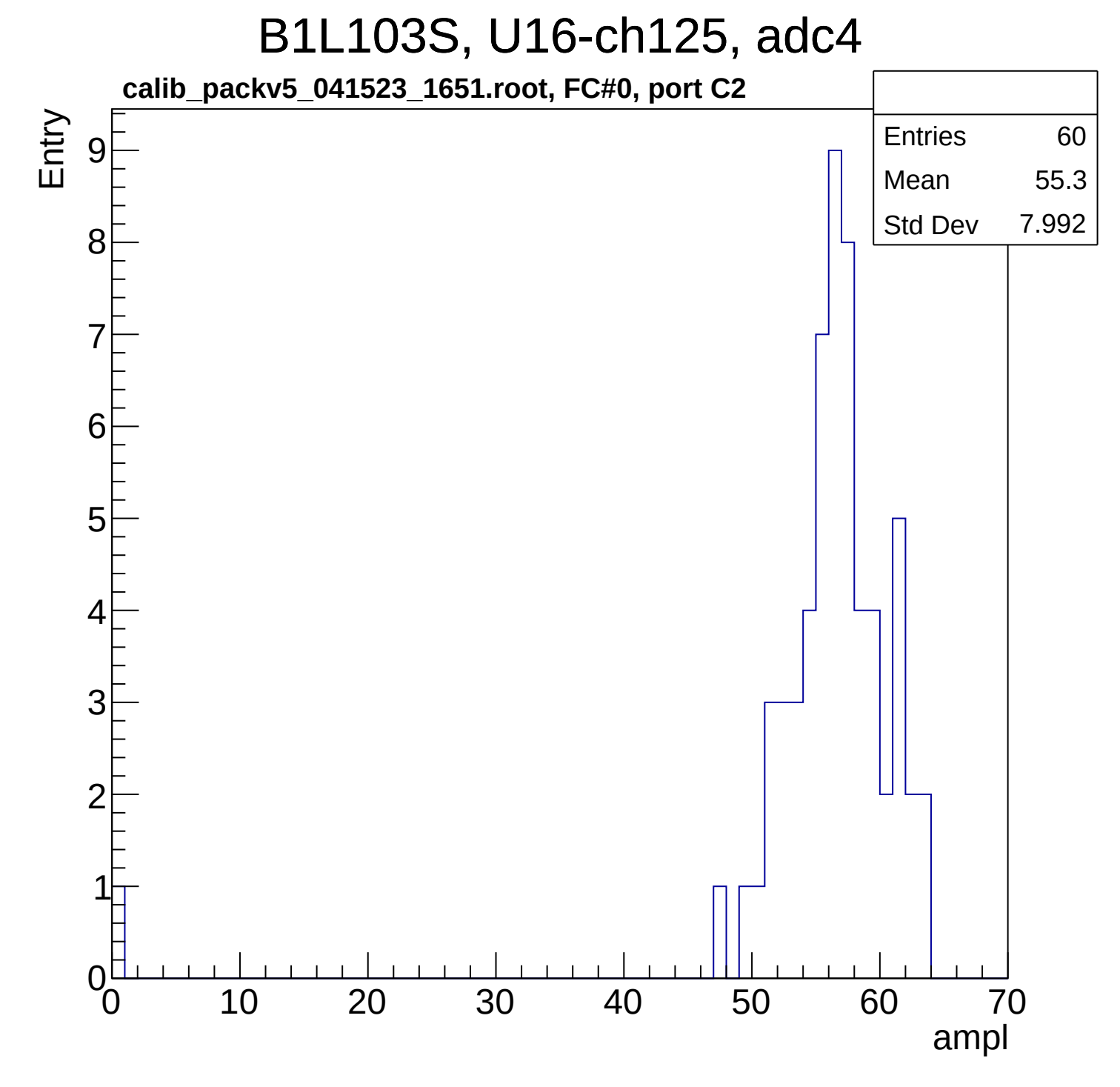
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch125, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 55.3
Std Dev 7.992
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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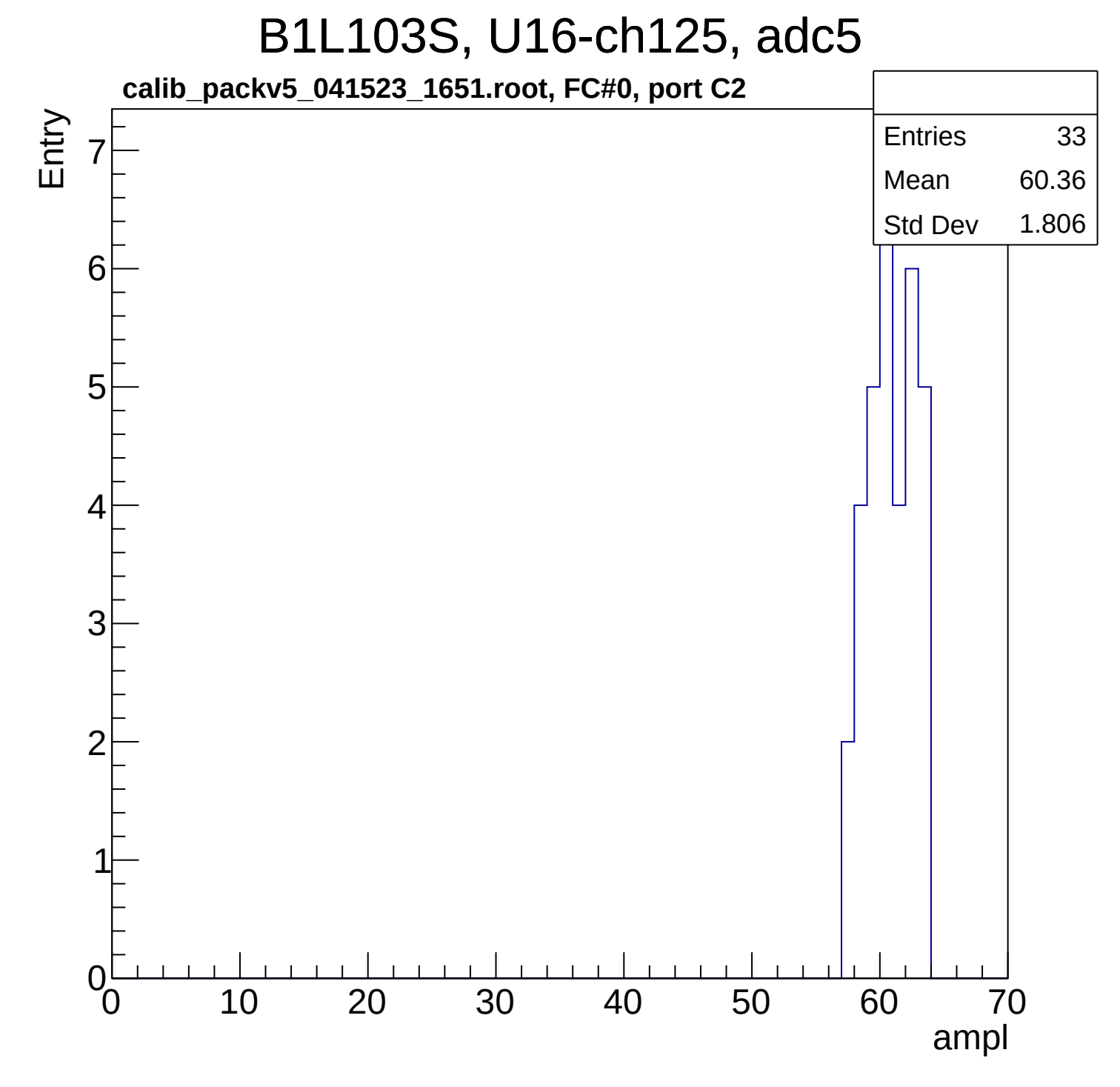
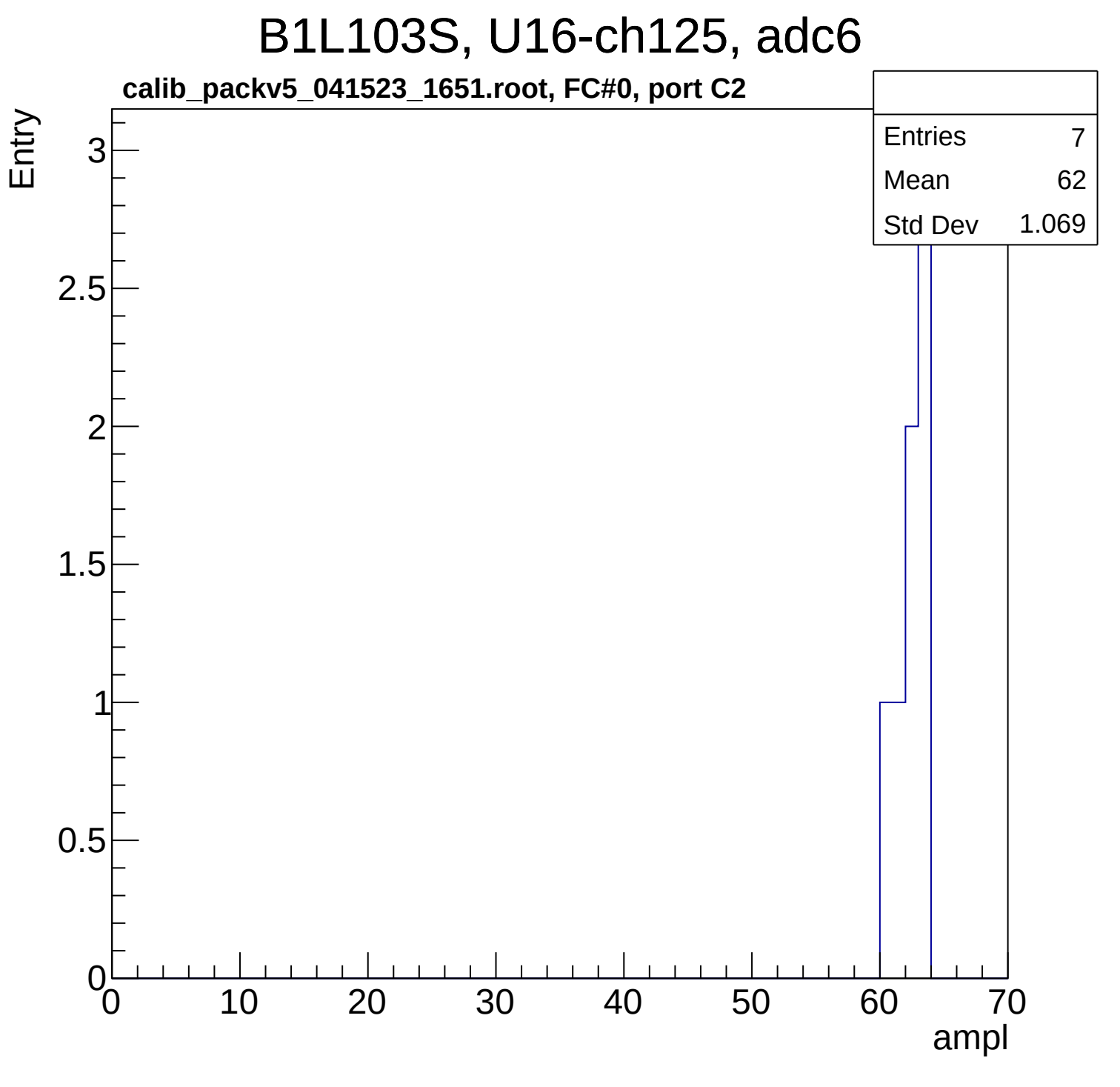
60
70


B1L103S, U16-ch125, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 60.36
Std Dev 1.806
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch125, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62
Std Dev 1.069
Entry
ampl
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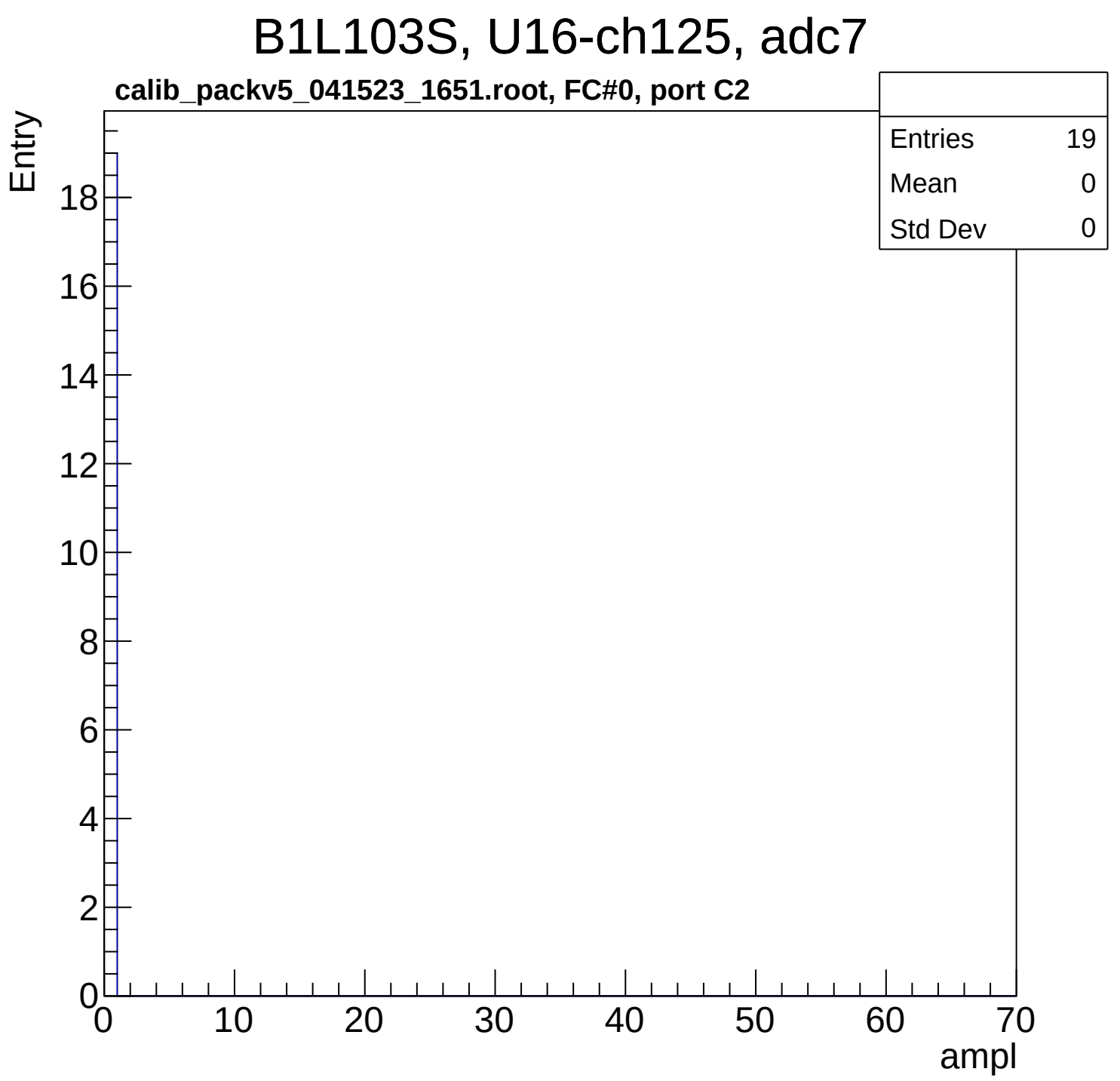
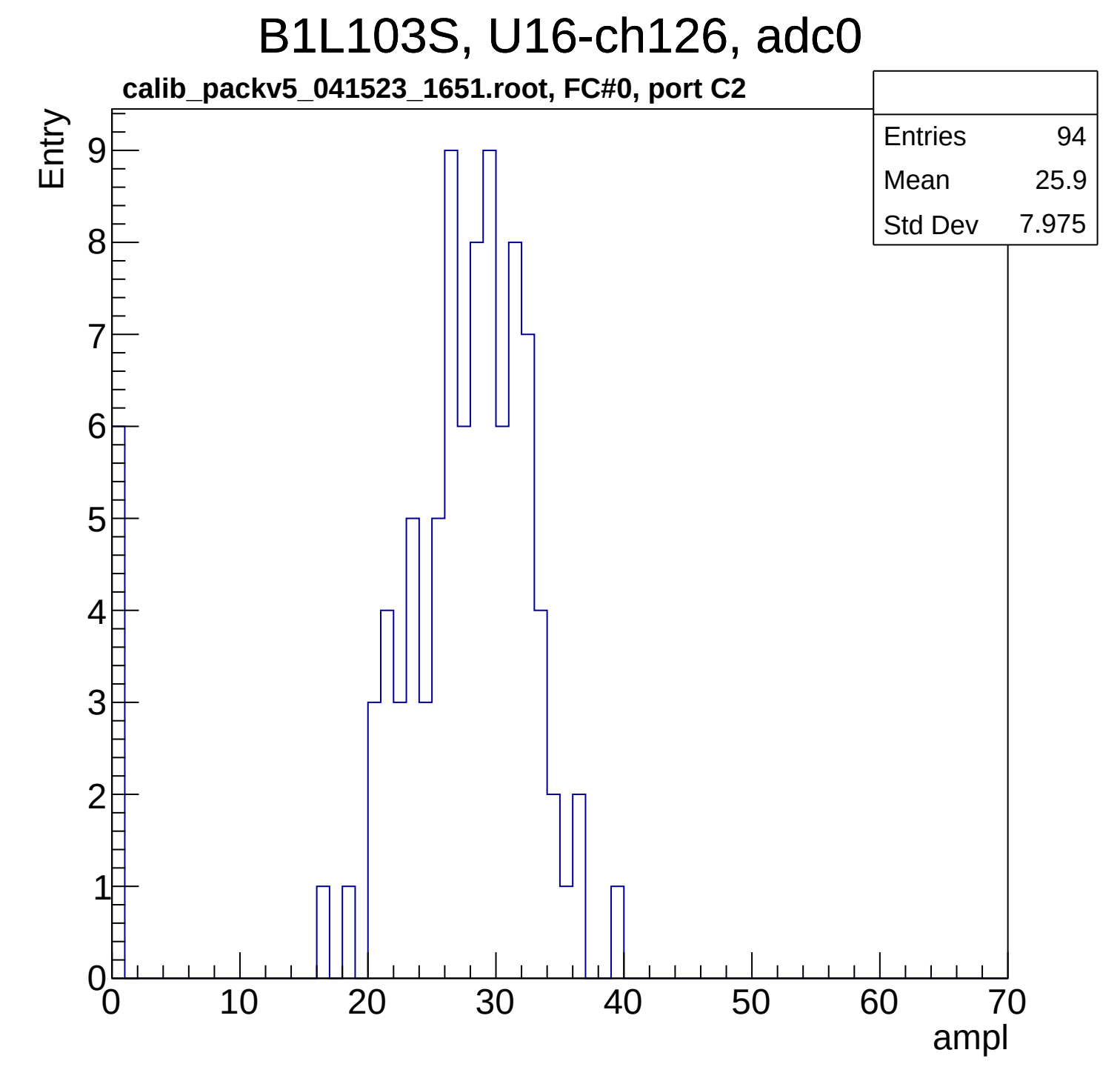
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U16-ch125, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch126, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 25.9
Std Dev 7.975
Entry
ampl
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2
3
4
5
6
7
8
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0
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20
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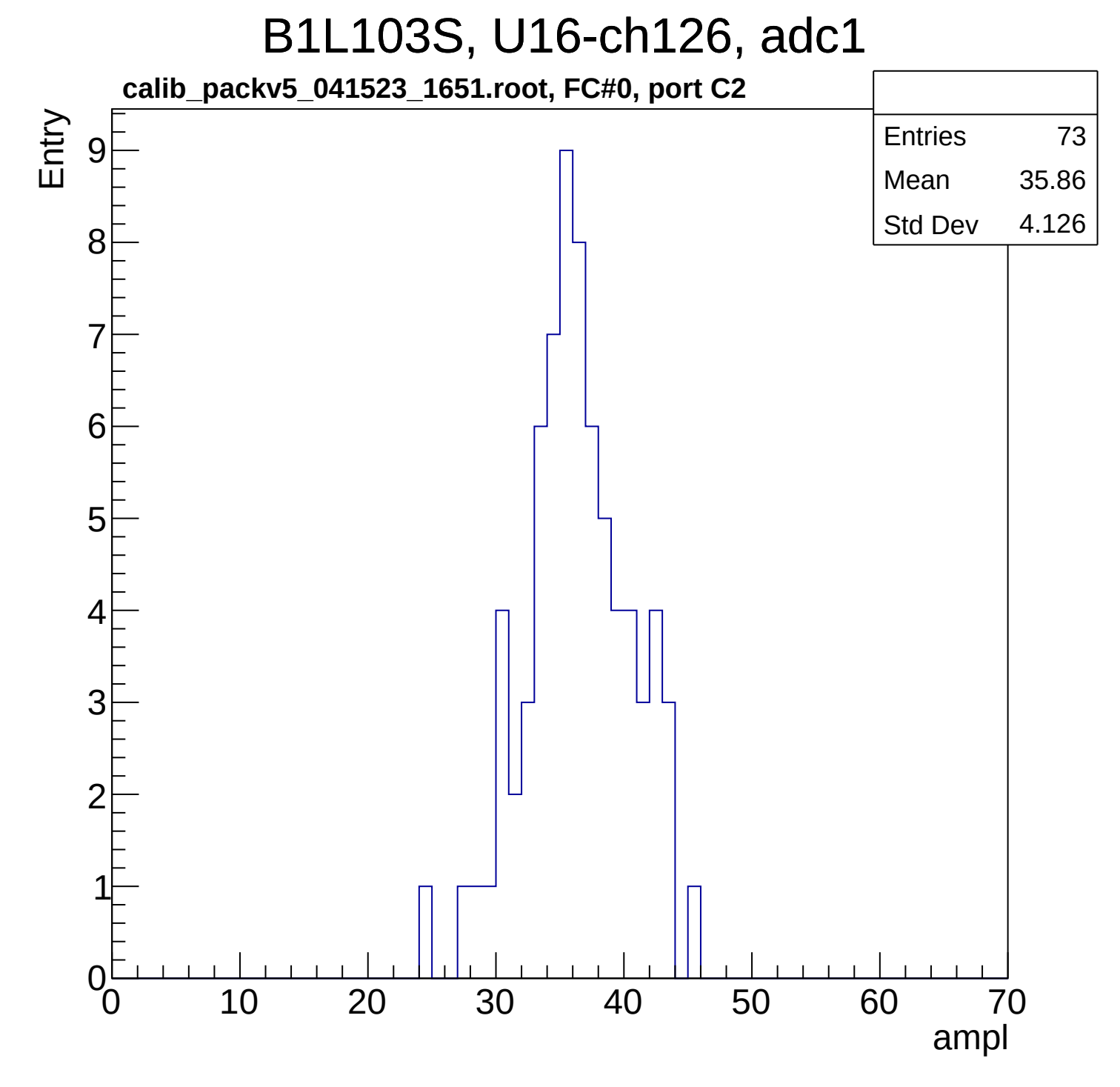
40
50
60
70


B1L103S, U16-ch126, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 35.86
Std Dev 4.126
Entry
ampl
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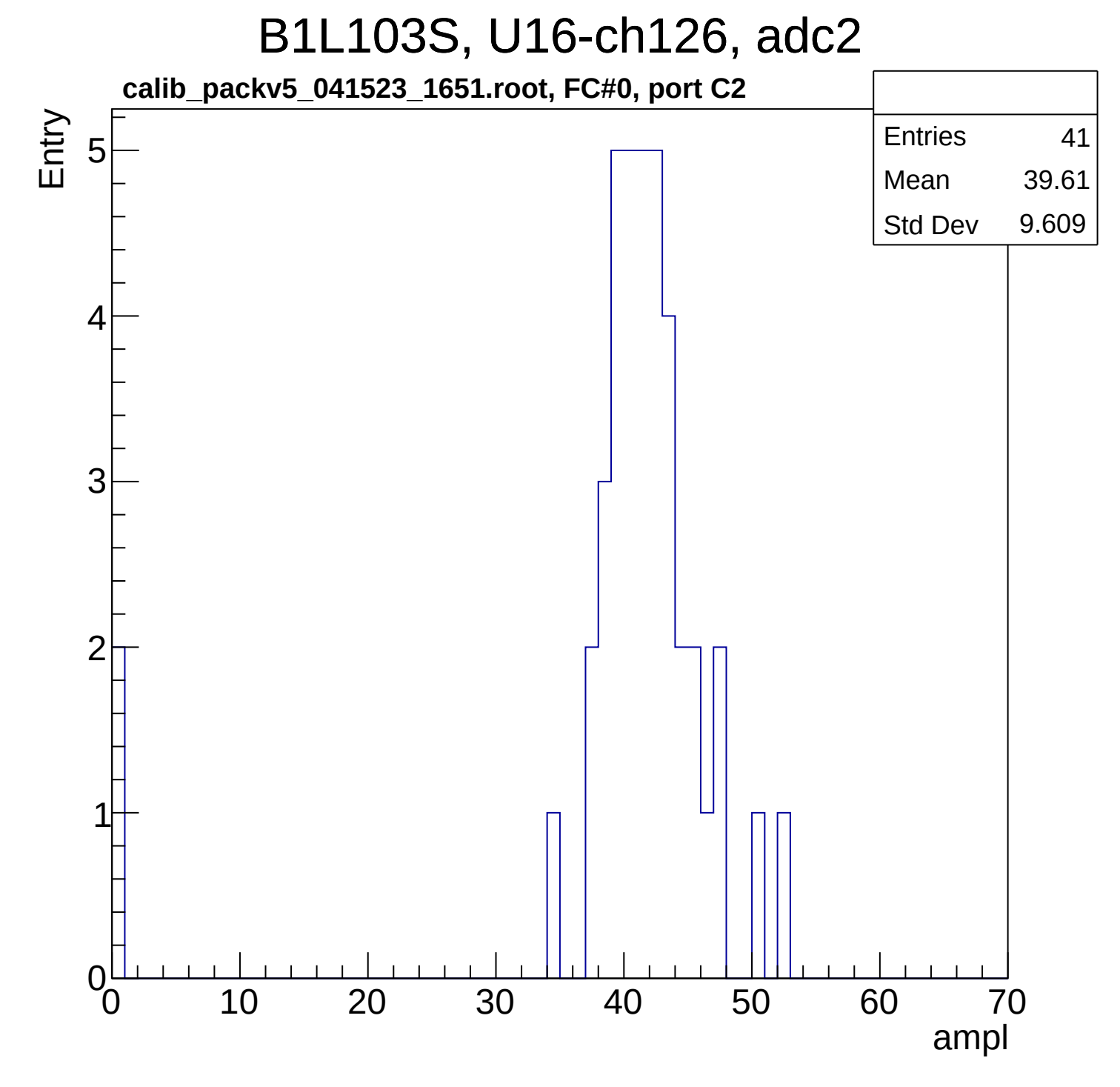
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U16-ch126, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 39.61
Std Dev 9.609
Entry
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1
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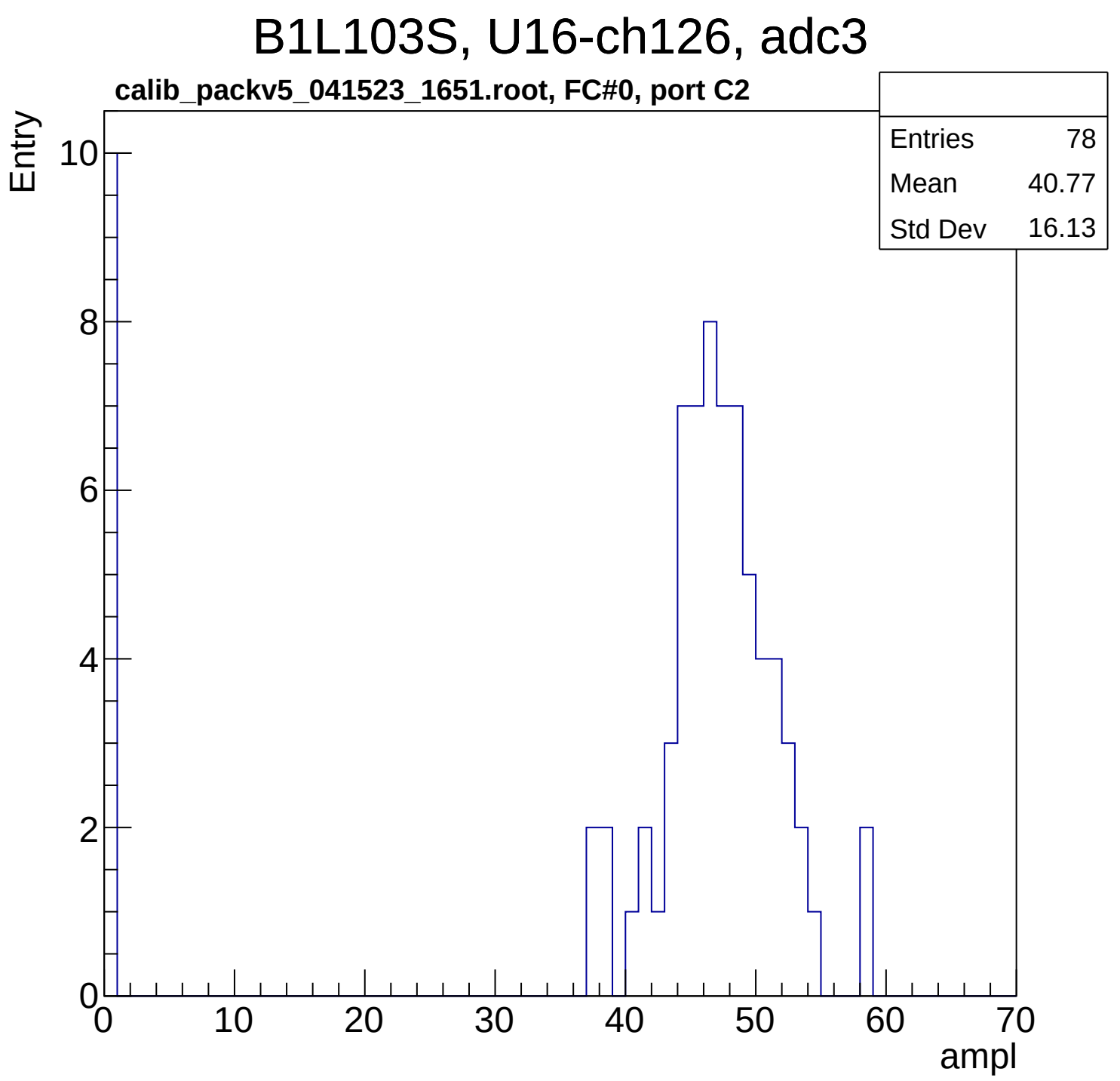
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch126, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 40.77
Std Dev 16.13
Entry
ampl
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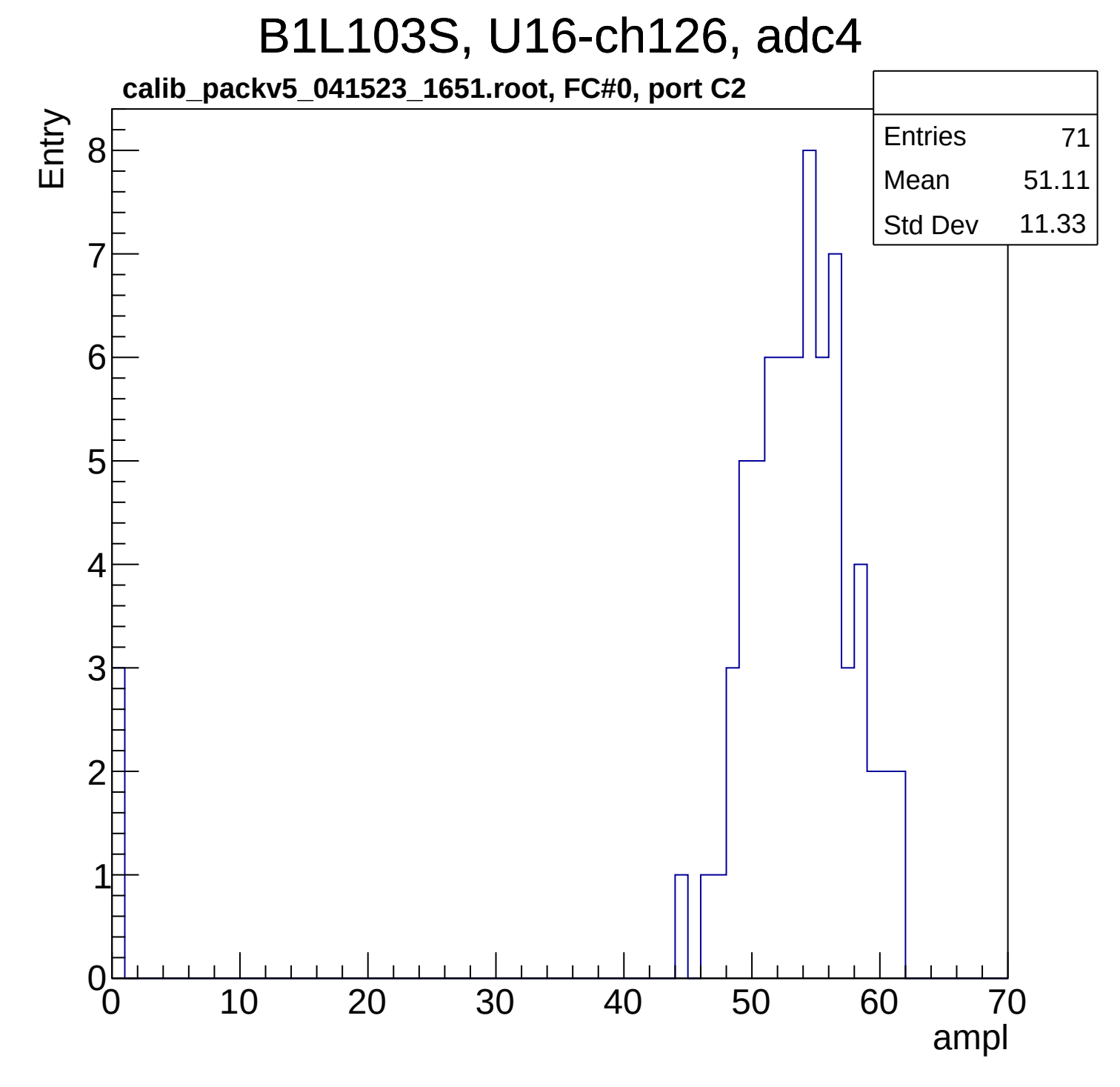
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U16-ch126, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 51.11
Std Dev 11.33
Entry
ampl
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4
5
6
7
8
0
10
20
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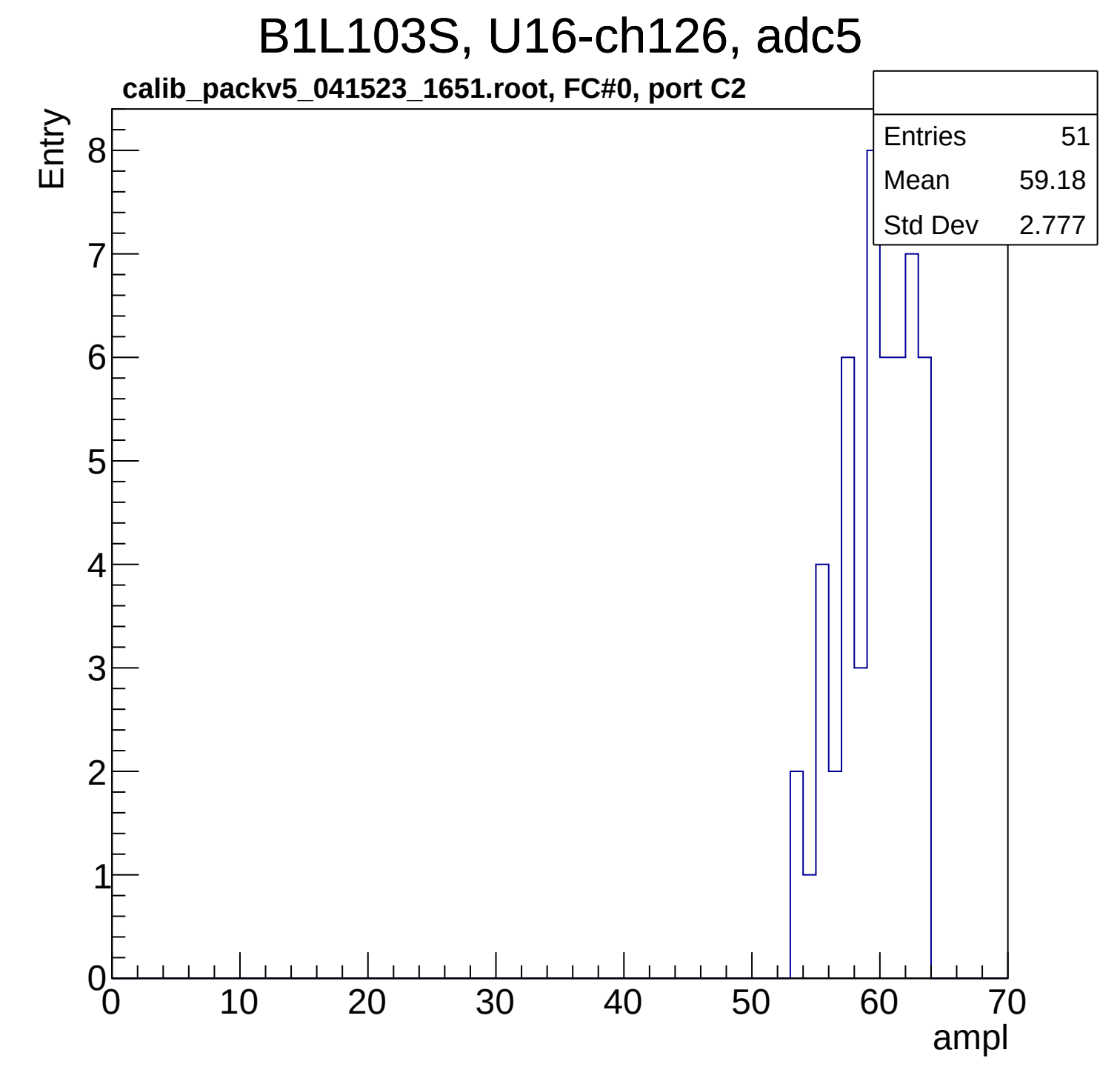
40
50
60
70


B1L103S, U16-ch126, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 59.18
Std Dev 2.777
Entry
ampl
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4
5
6
7
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0
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40
50
60
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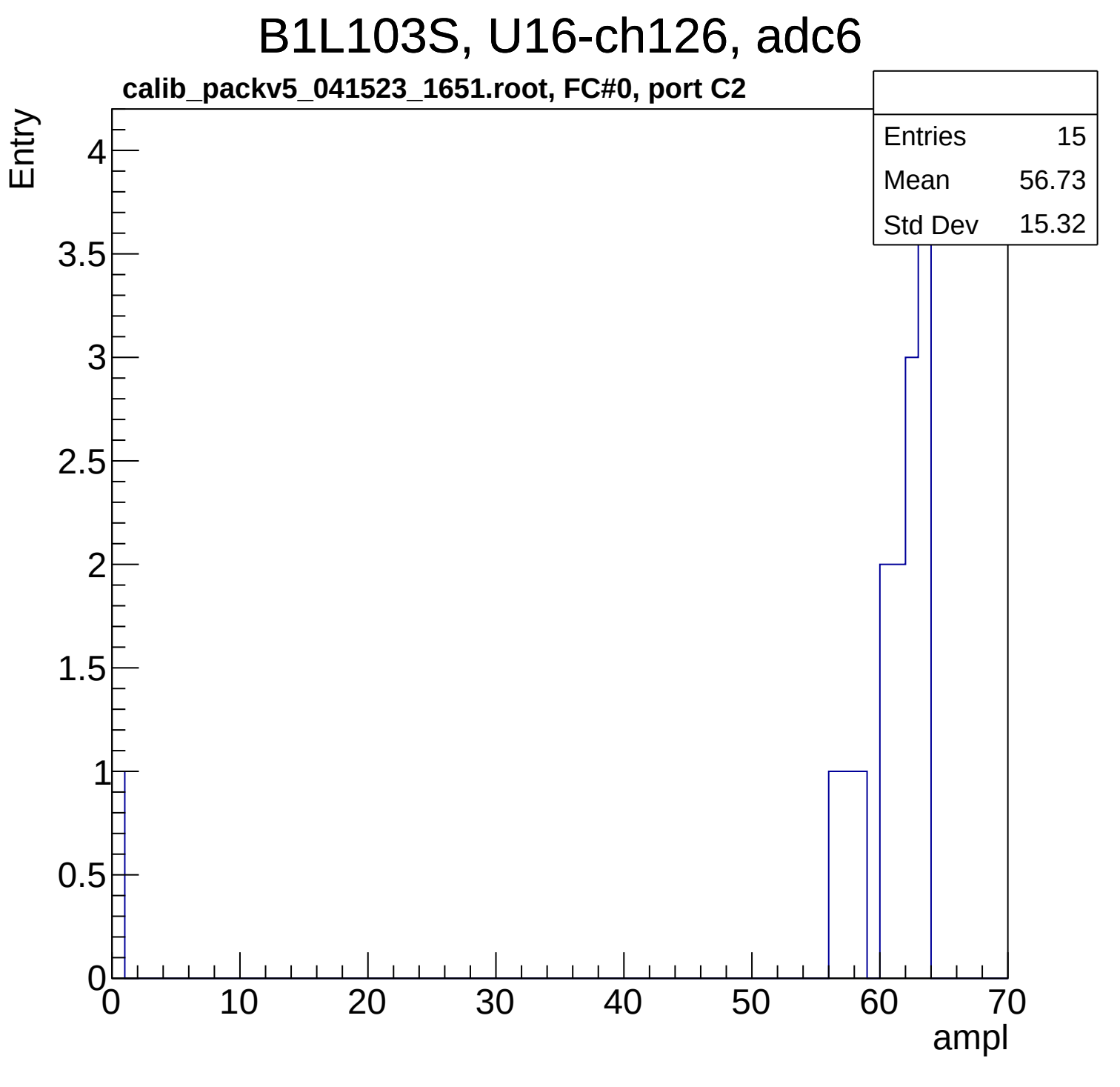
B1L103S, U16-ch126, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 56.73
Std Dev 15.32
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
10
20
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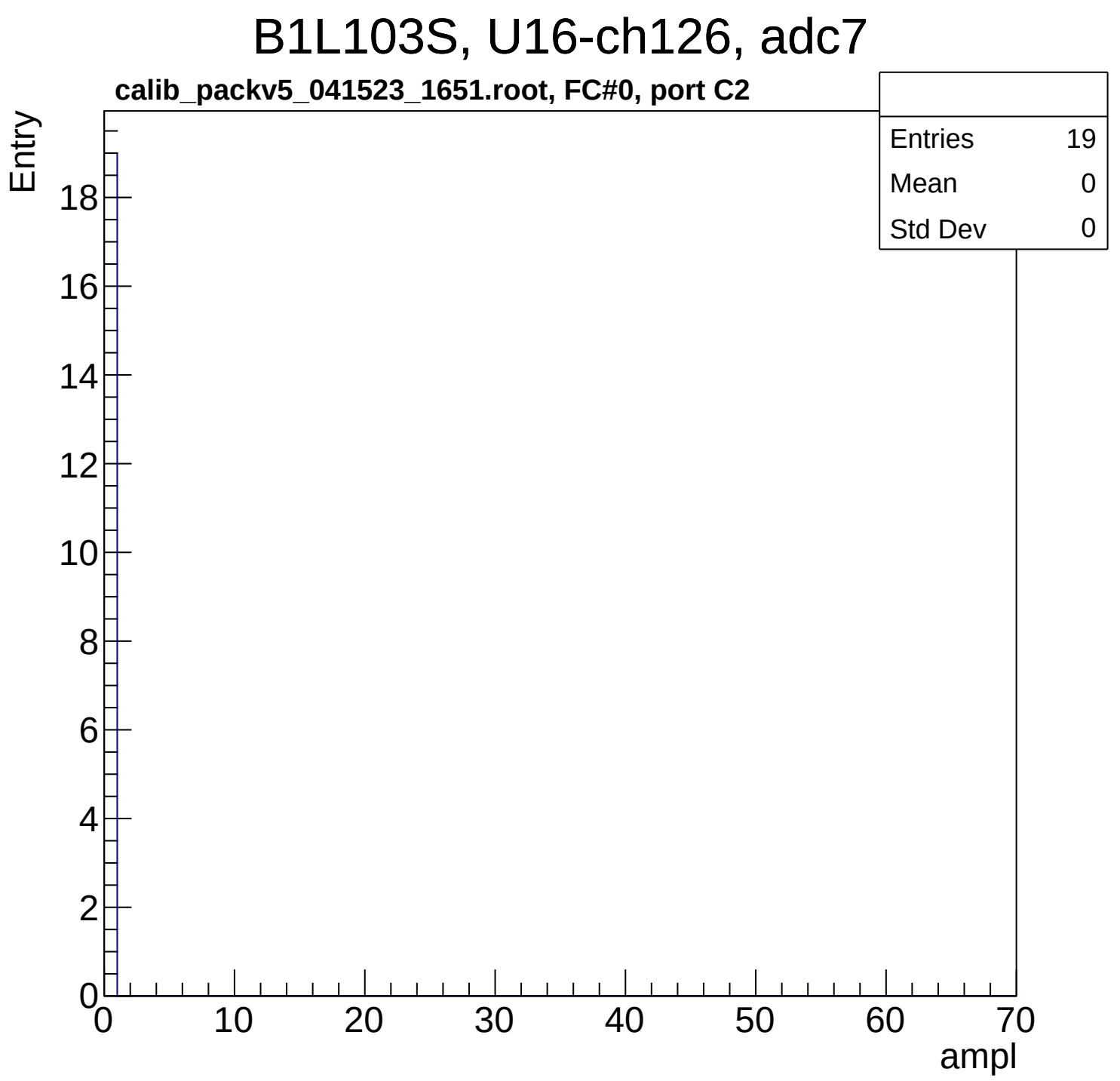
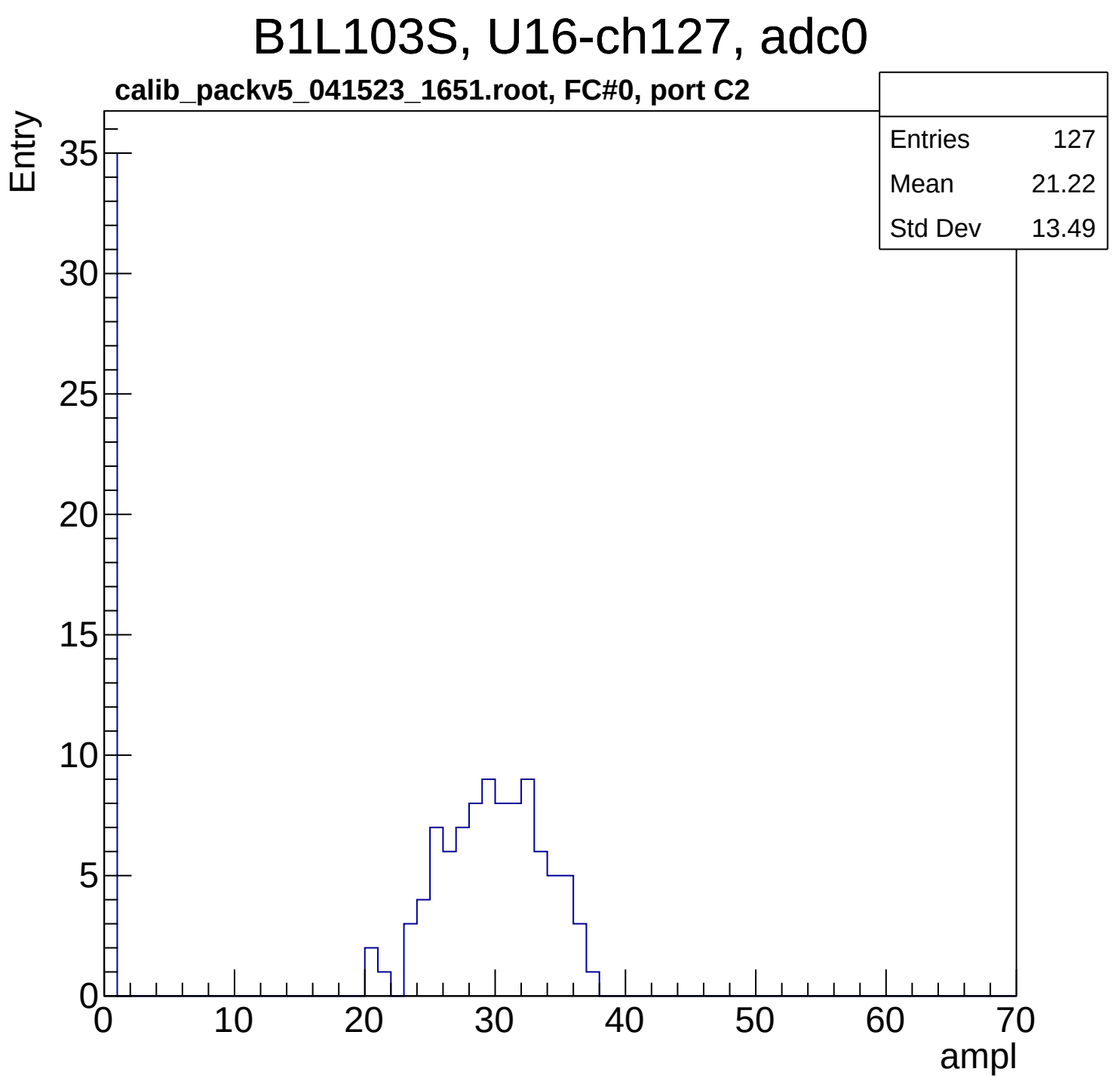
40
50
60
70


B1L103S, U16-ch126, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch127, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 127
Mean 21.22
Std Dev 13.49
Entry
ampl
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5
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15
20
25
30
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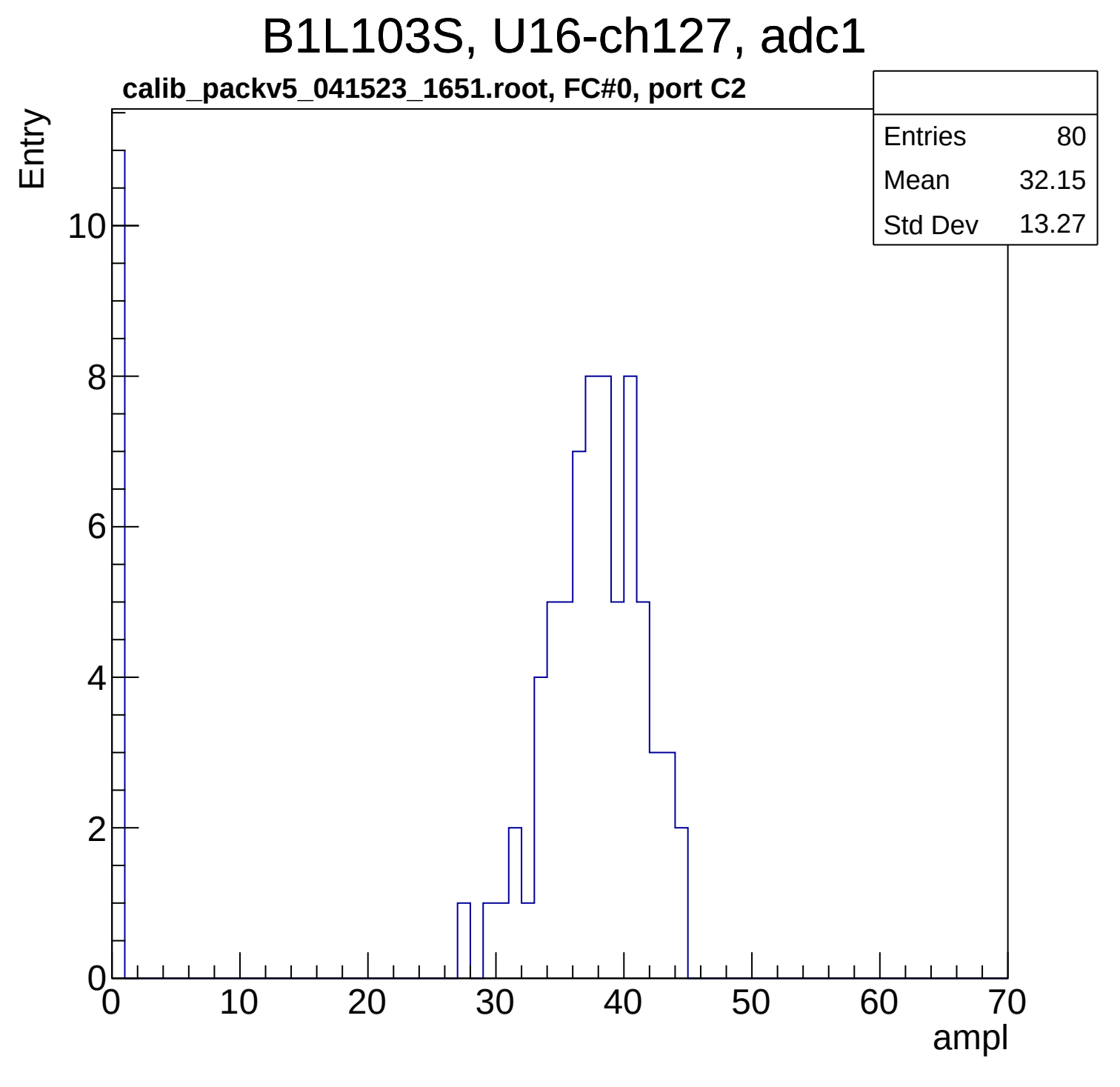
0
10
20
30
40
50
60
70


B1L103S, U16-ch127, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 32.15
Std Dev 13.27
Entry
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6
8
10
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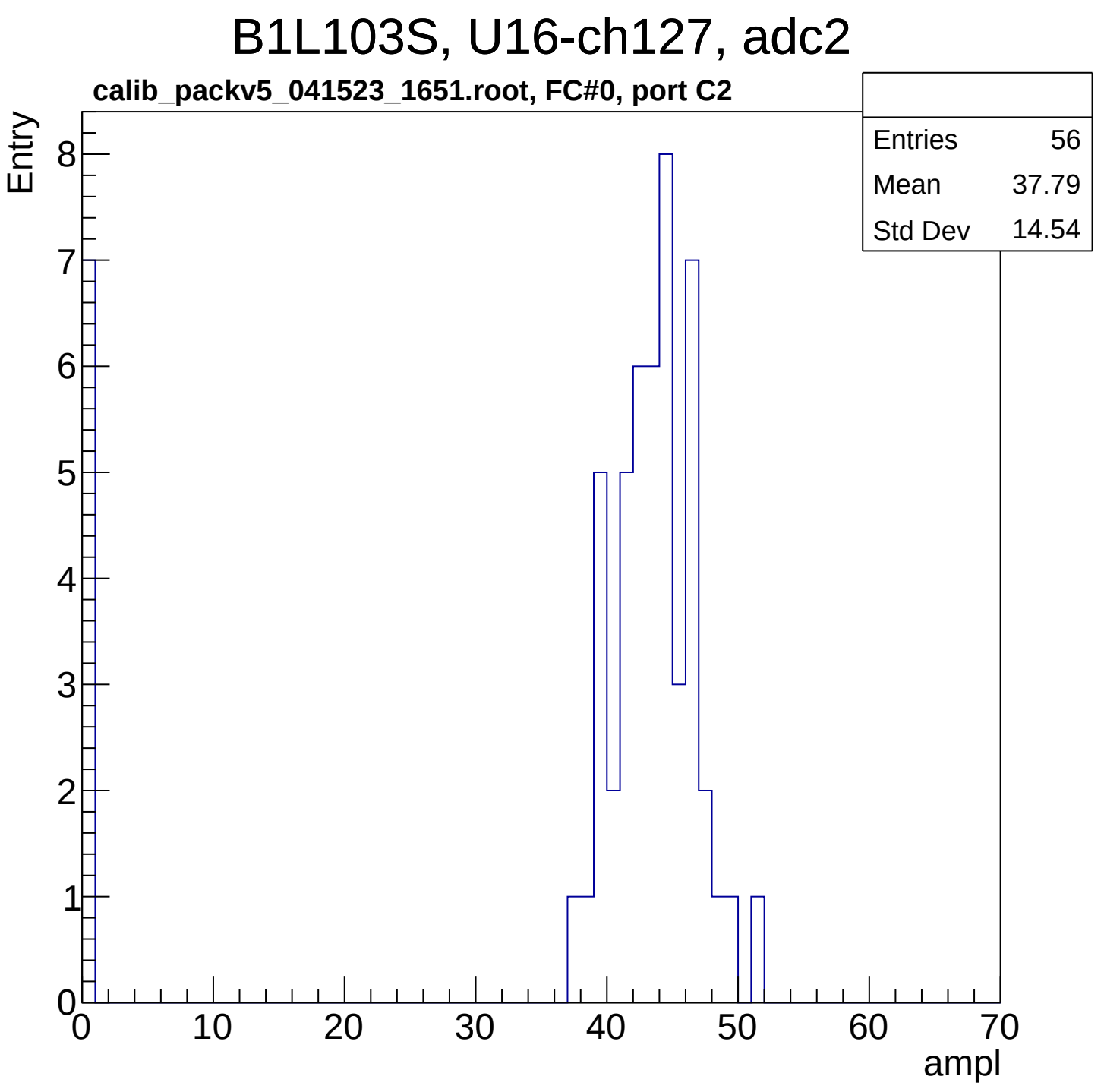
10
20
30
40
50
60
70
ampl


B1L103S, U16-ch127, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 37.79
Std Dev 14.54
Entry
ampl
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1
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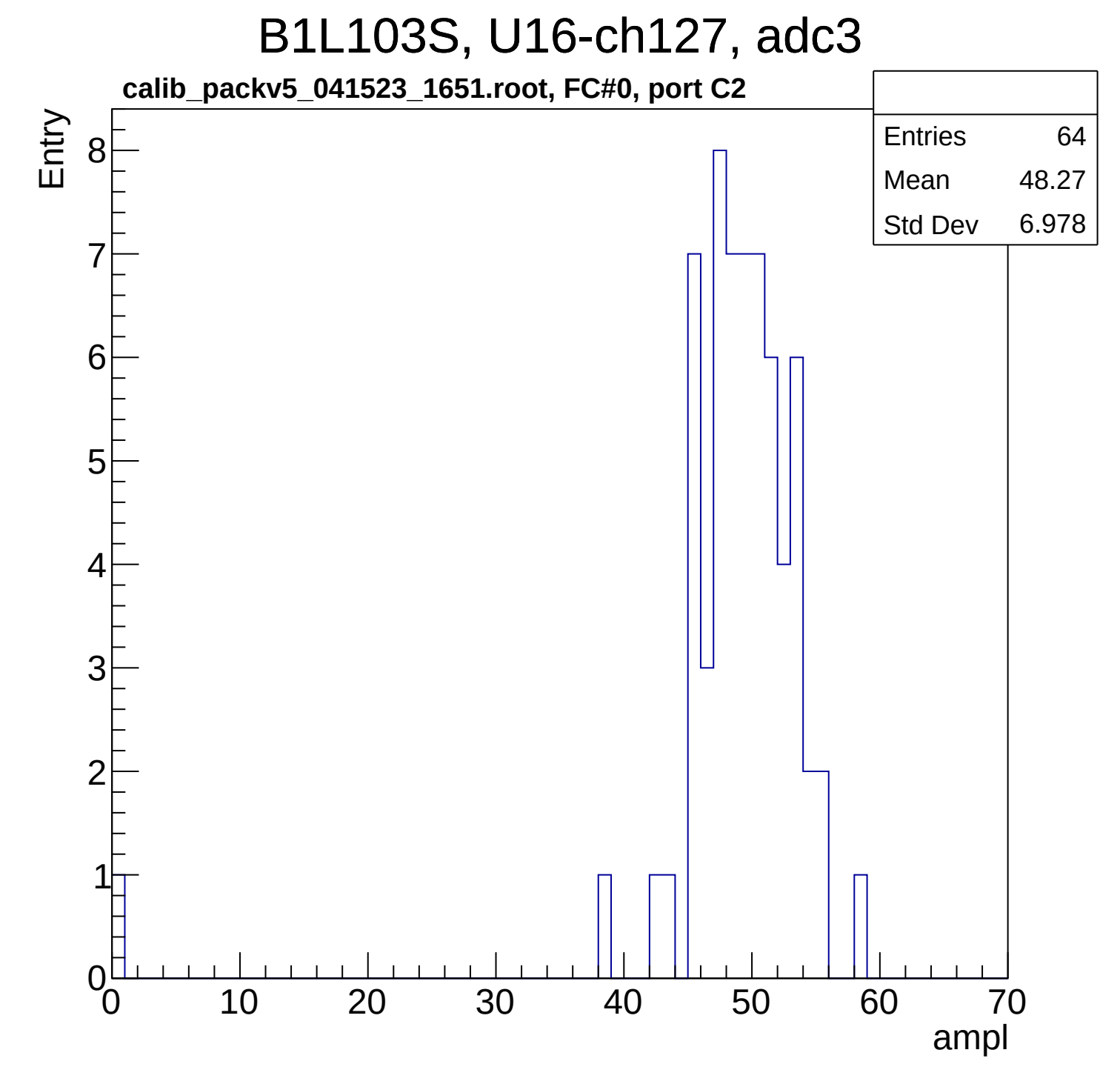
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch127, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 48.27
Std Dev 6.978
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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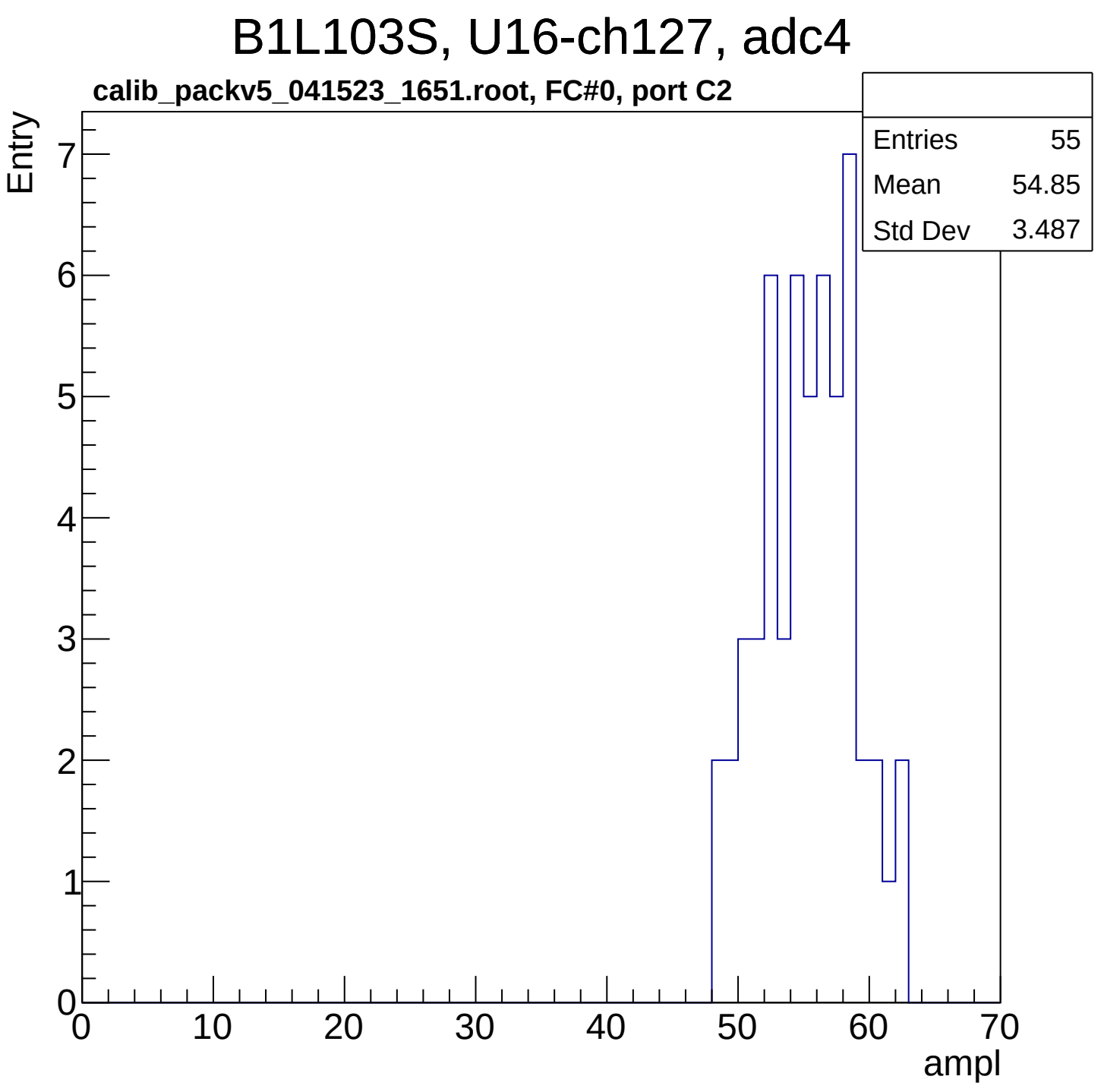
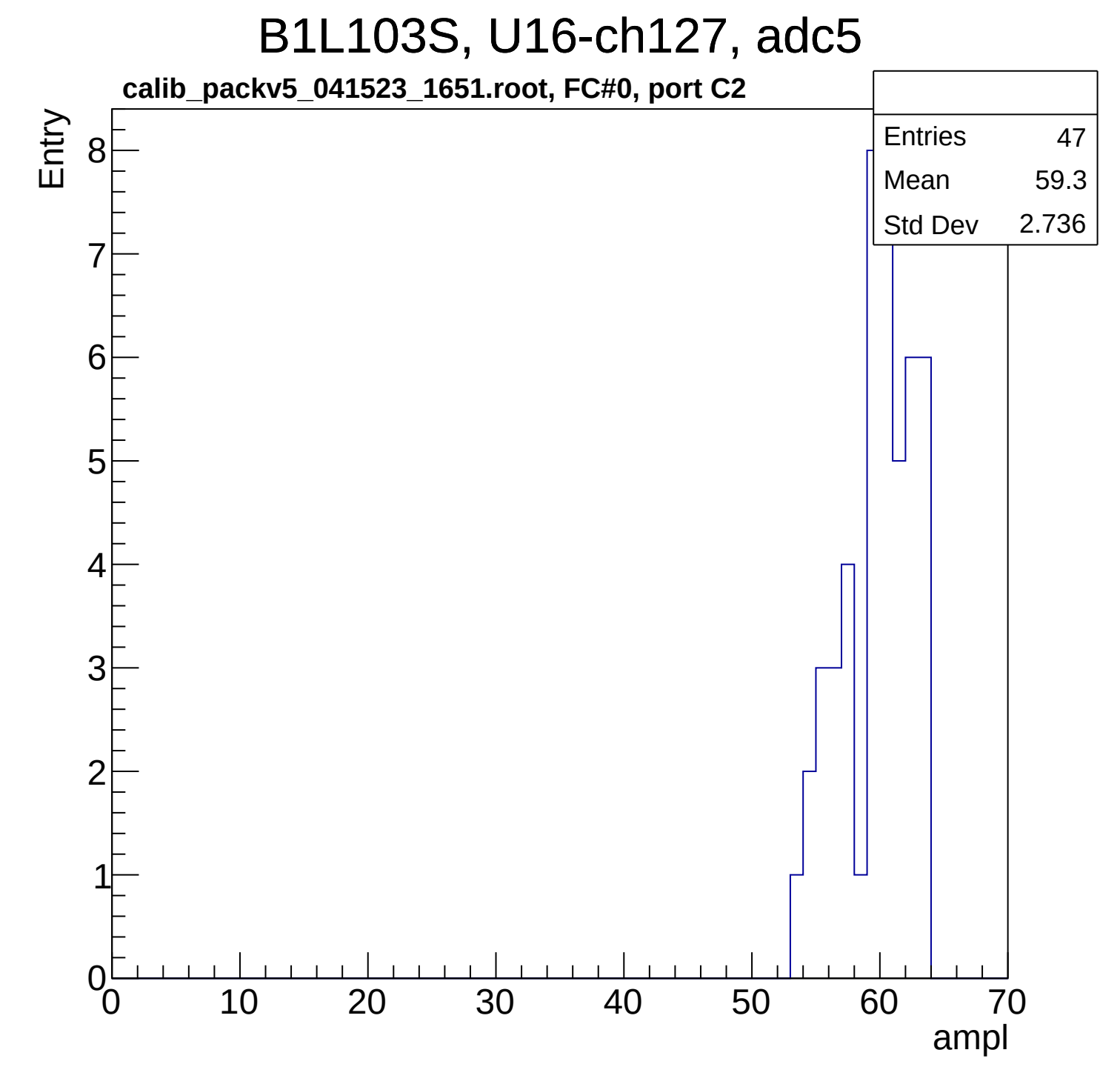
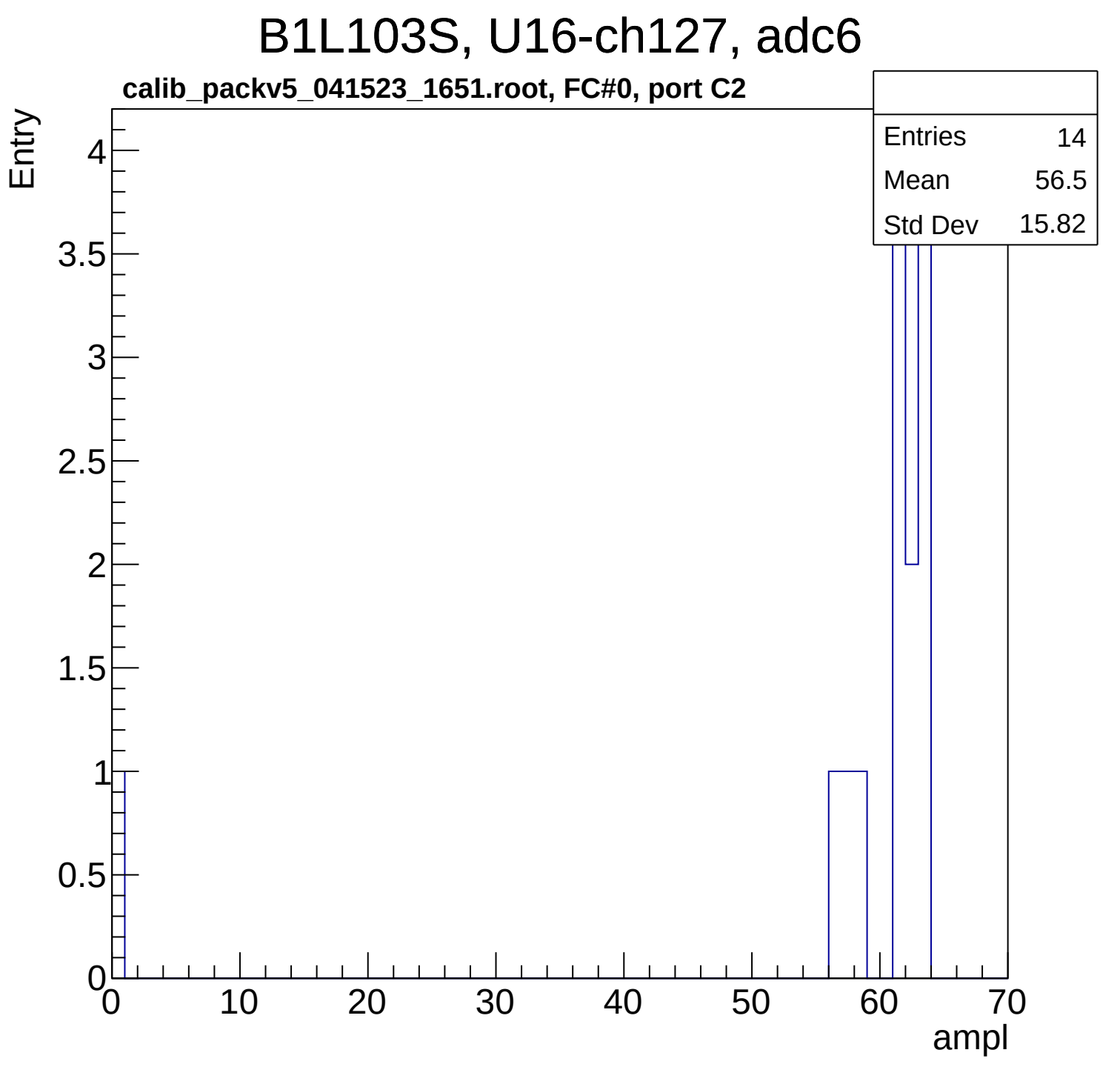
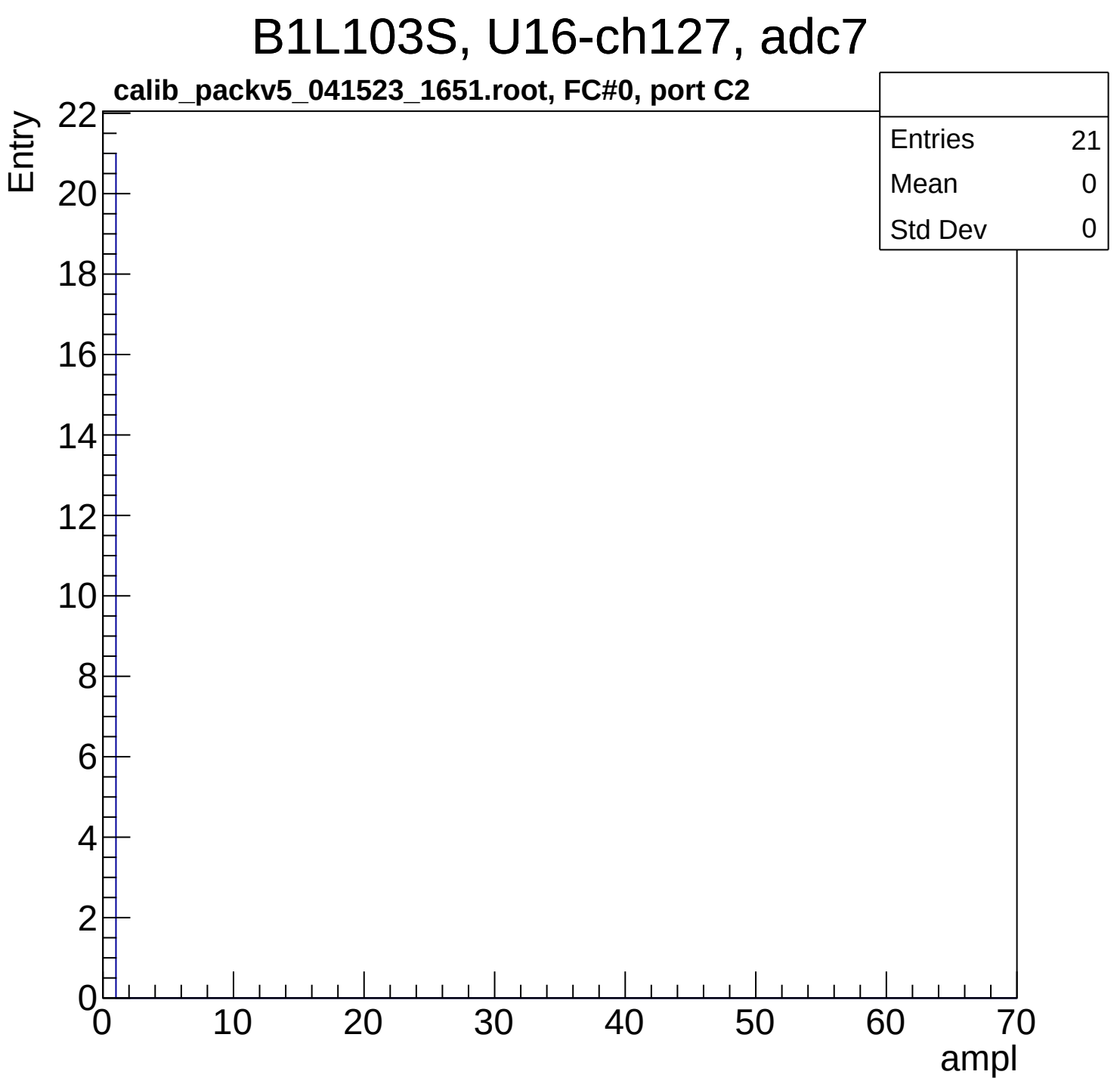
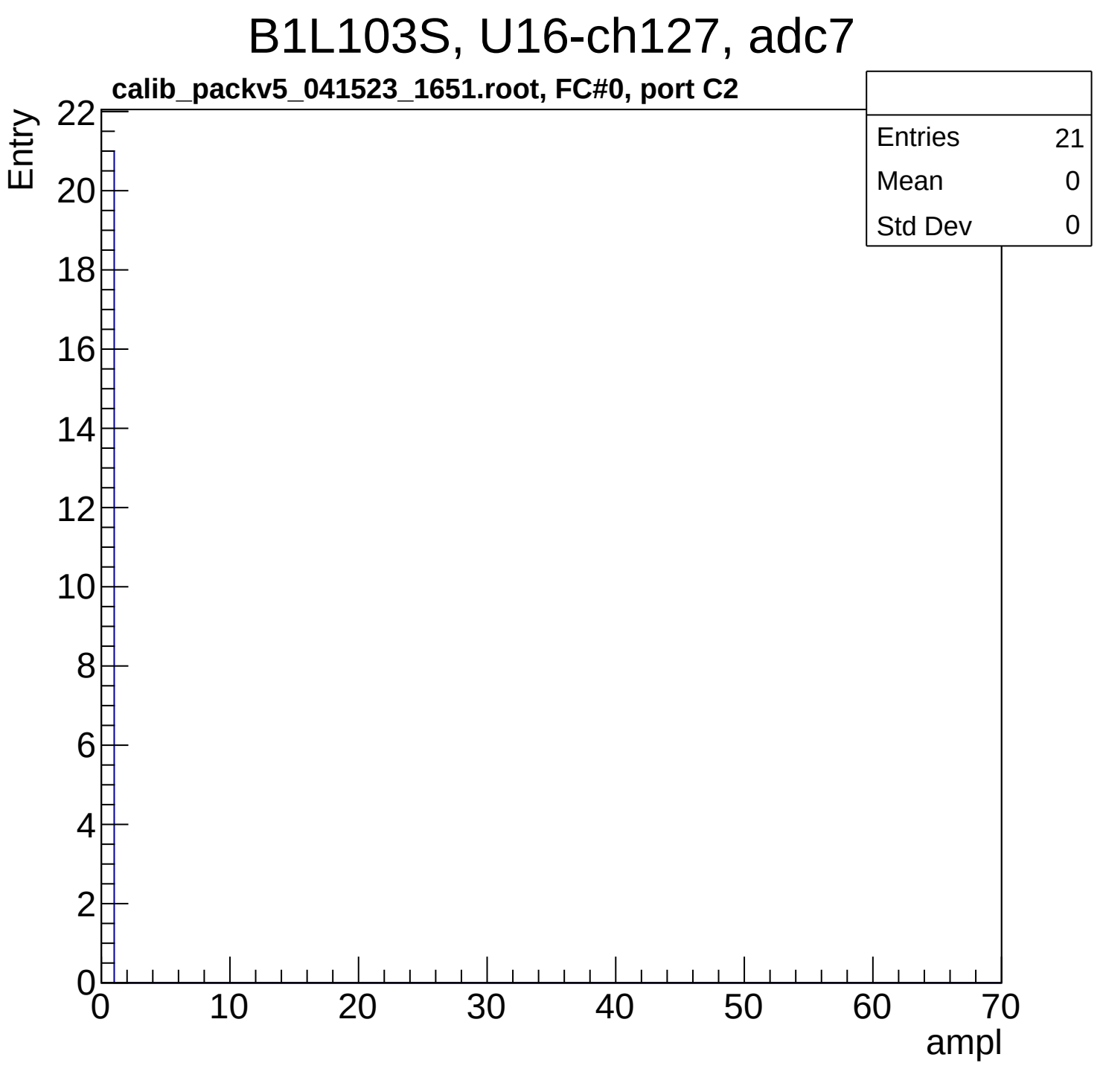
40
50
60
70


B1L103S, U16-ch127, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 54.85
Std Dev 3.487
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U16-ch127, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 59.3
Std Dev 2.736
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U16-ch127, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 56.5
Std Dev 15.82
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U16-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 0
Std Dev 0
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U16-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 0
Std Dev 0
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70