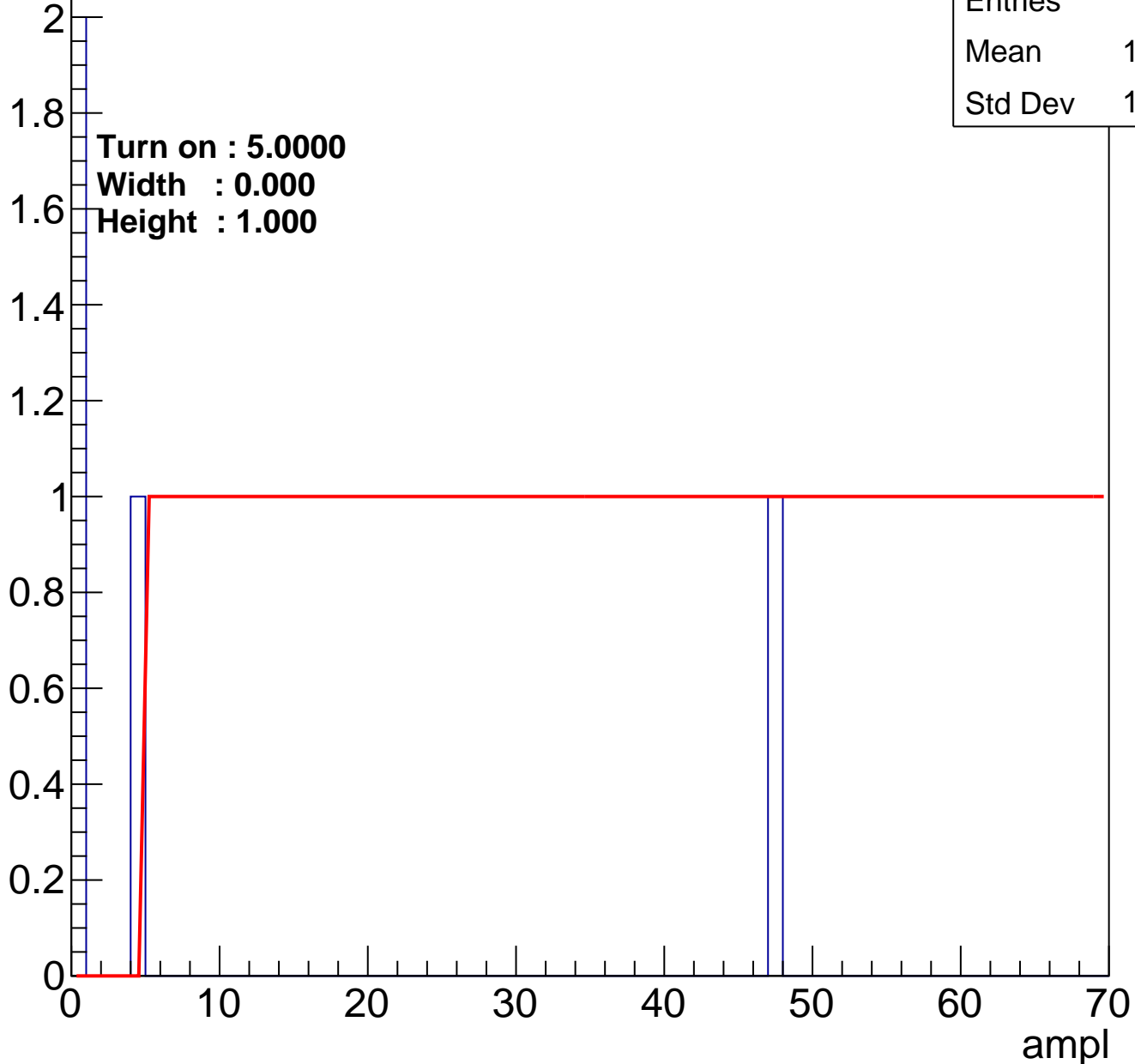


B0L101S, U2-ch0

calib_packv5_042523_0143.root, FC#1, port C1

Entry



B0L101S, U2-ch1

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	2
Mean	0
Std Dev	0

B0L101S, U2-ch2

calib_packv5_042523_0143.root, FC#1, port C1

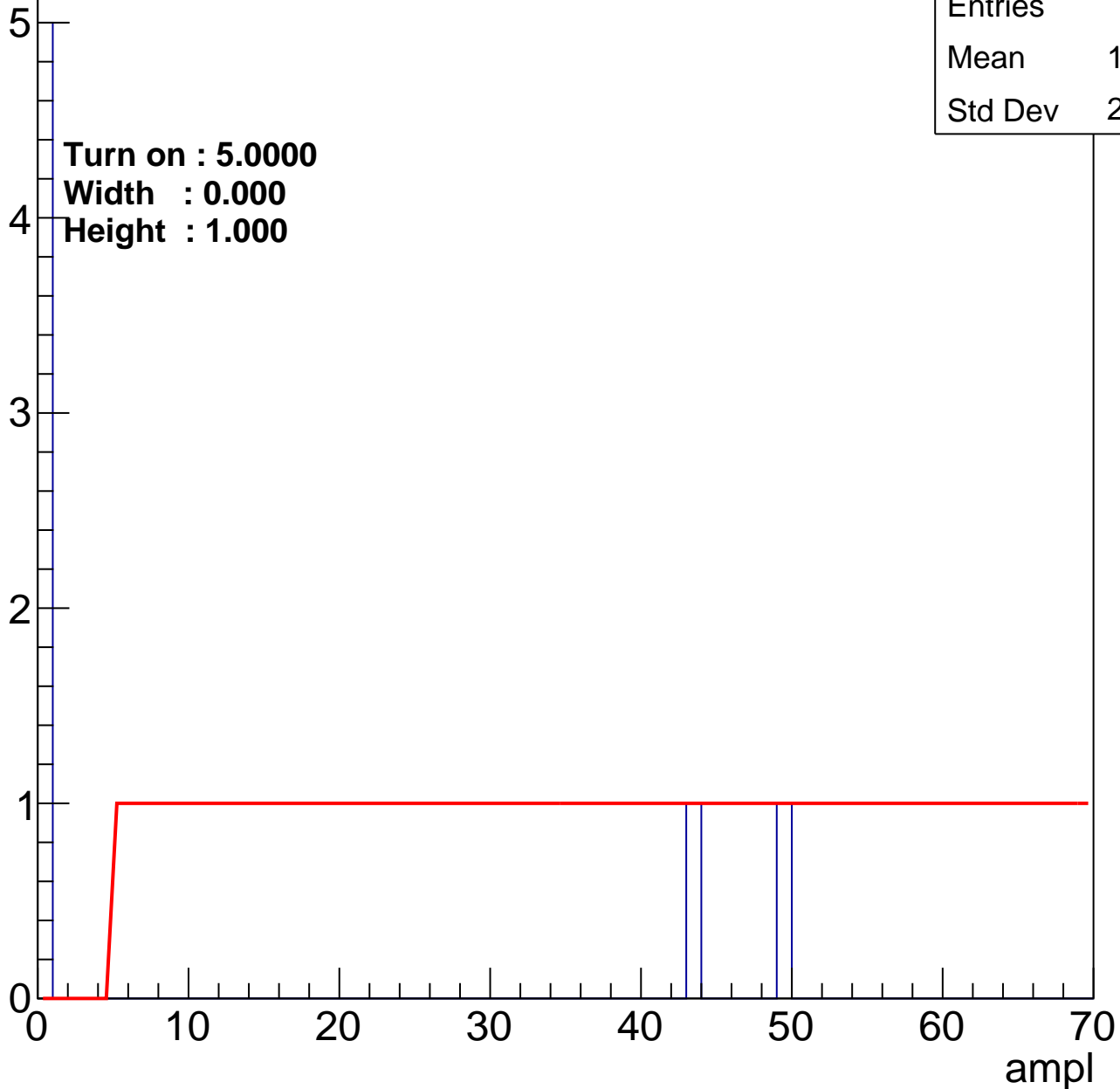
Entry

Entries	7
Mean	13.14
Std Dev	20.84

Turn on : 5.0000

Width : 0.000

Height : 1.000



B0L101S, U2-ch3

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	1
Mean	0
Std Dev	0

B0L101S, U2-ch4

calib_packv5_042523_0143.root, FC#1, port C1

Entry

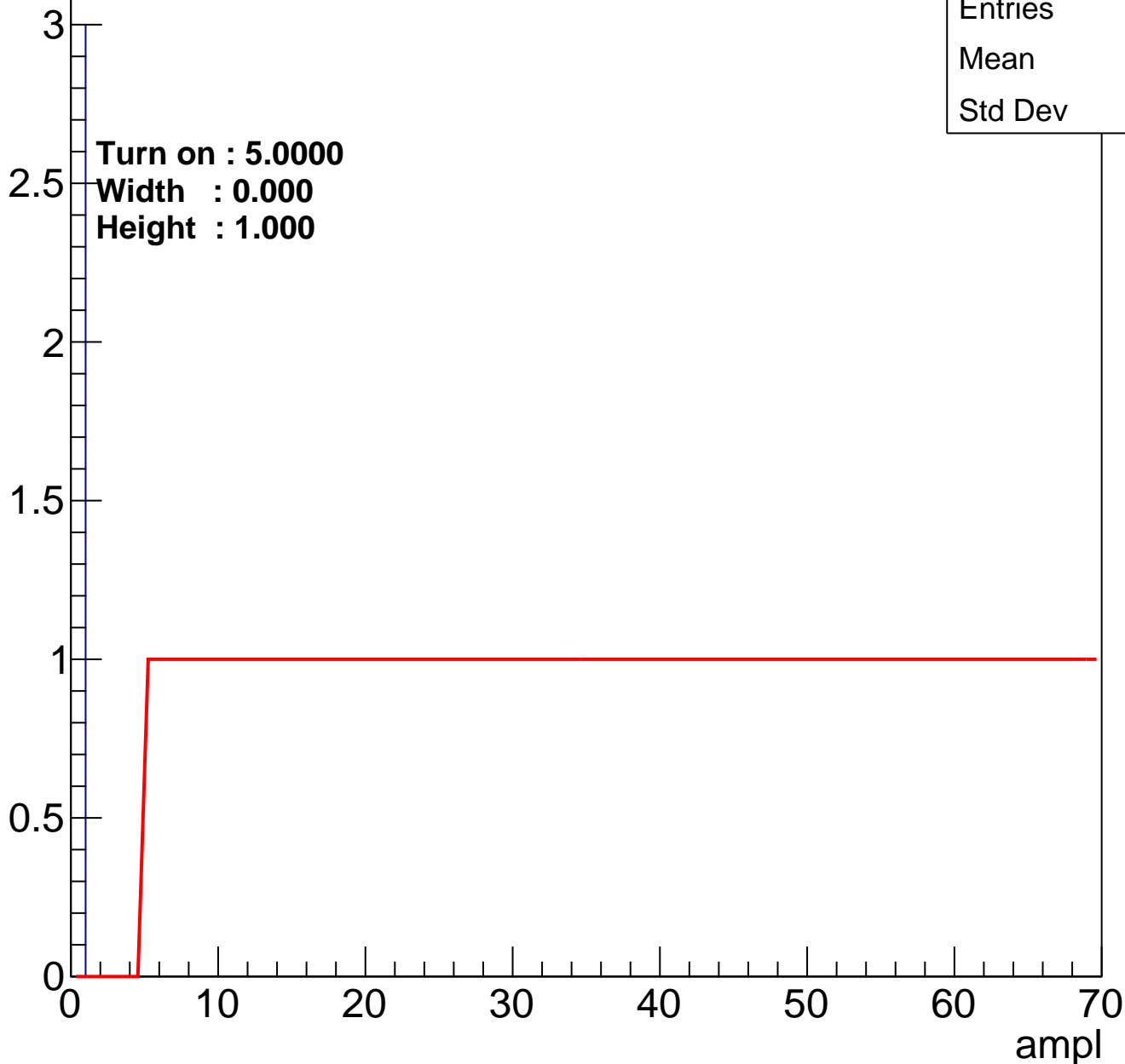


Entries	3
Mean	0
Std Dev	0

B0L101S, U2-ch5

calib_packv5_042523_0143.root, FC#1, port C1

Entry



B0L101S, U2-ch6

calib_packv5_042523_0143.root, FC#1, port C1

Entry



B0L101S, U2-ch7

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	0
Mean	0
Std Dev	0

B0L101S, U2-ch8

calib_packv5_042523_0143.root, FC#1, port C1

Entry

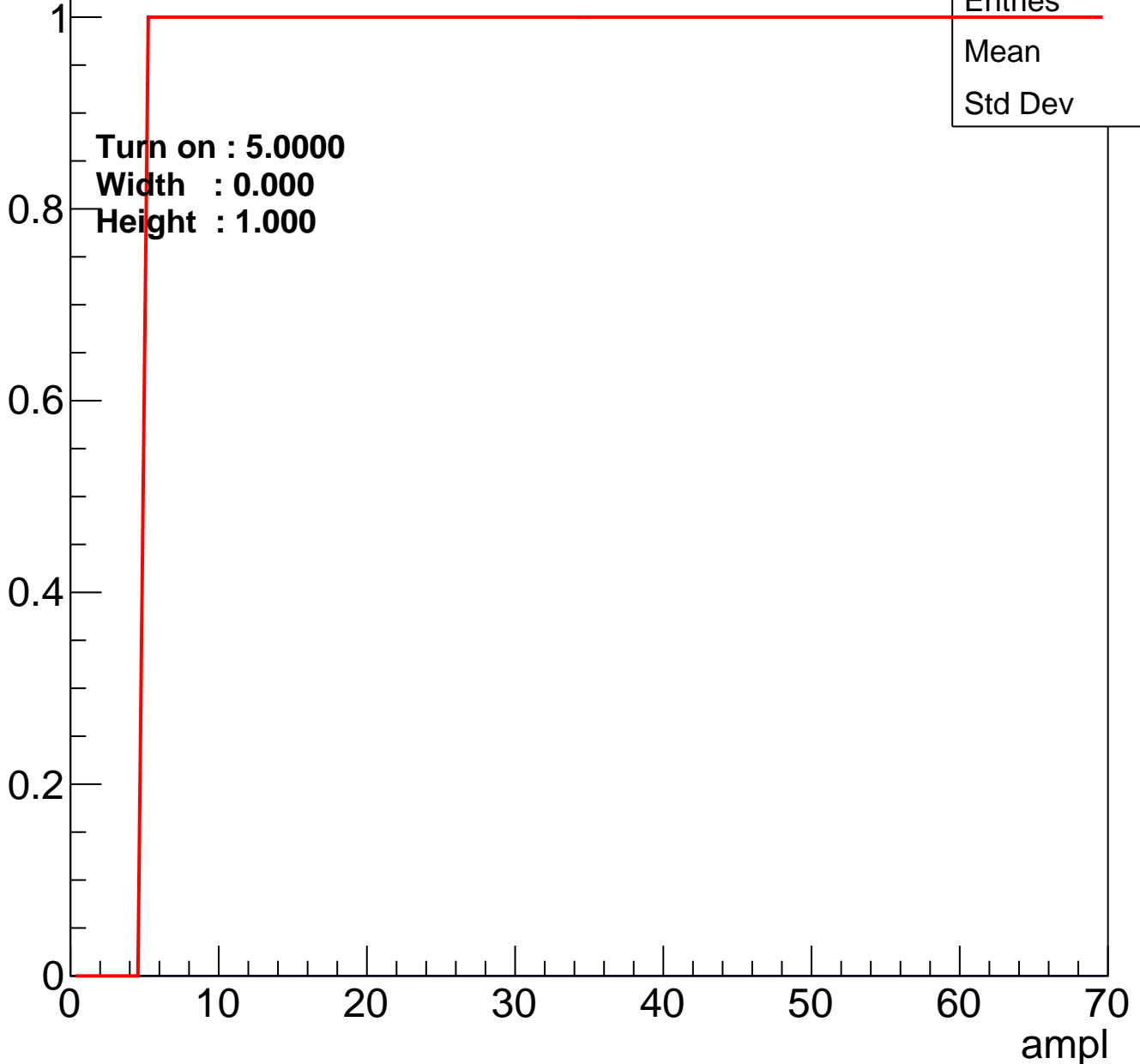


Entries	2
Mean	0
Std Dev	0

B0L101S, U2-ch9

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	0
Mean	0
Std Dev	0

B0L101S, U2-ch10

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	0
Mean	0
Std Dev	0

B0L101S, U2-ch11

calib_packv5_042523_0143.root, FC#1, port C1

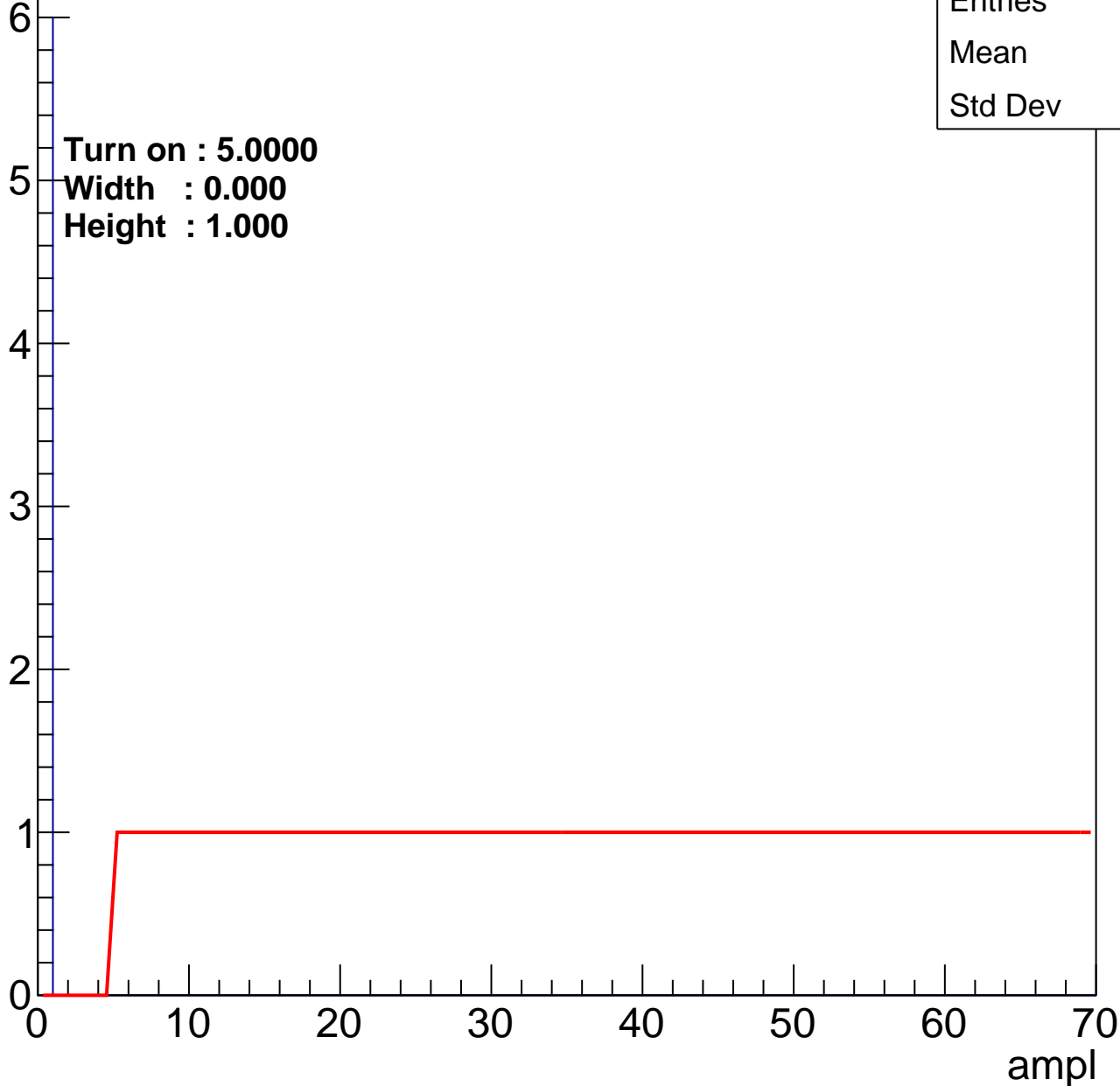
Entry

Entries	6
Mean	0
Std Dev	0

Turn on : 5.0000

Width : 0.000

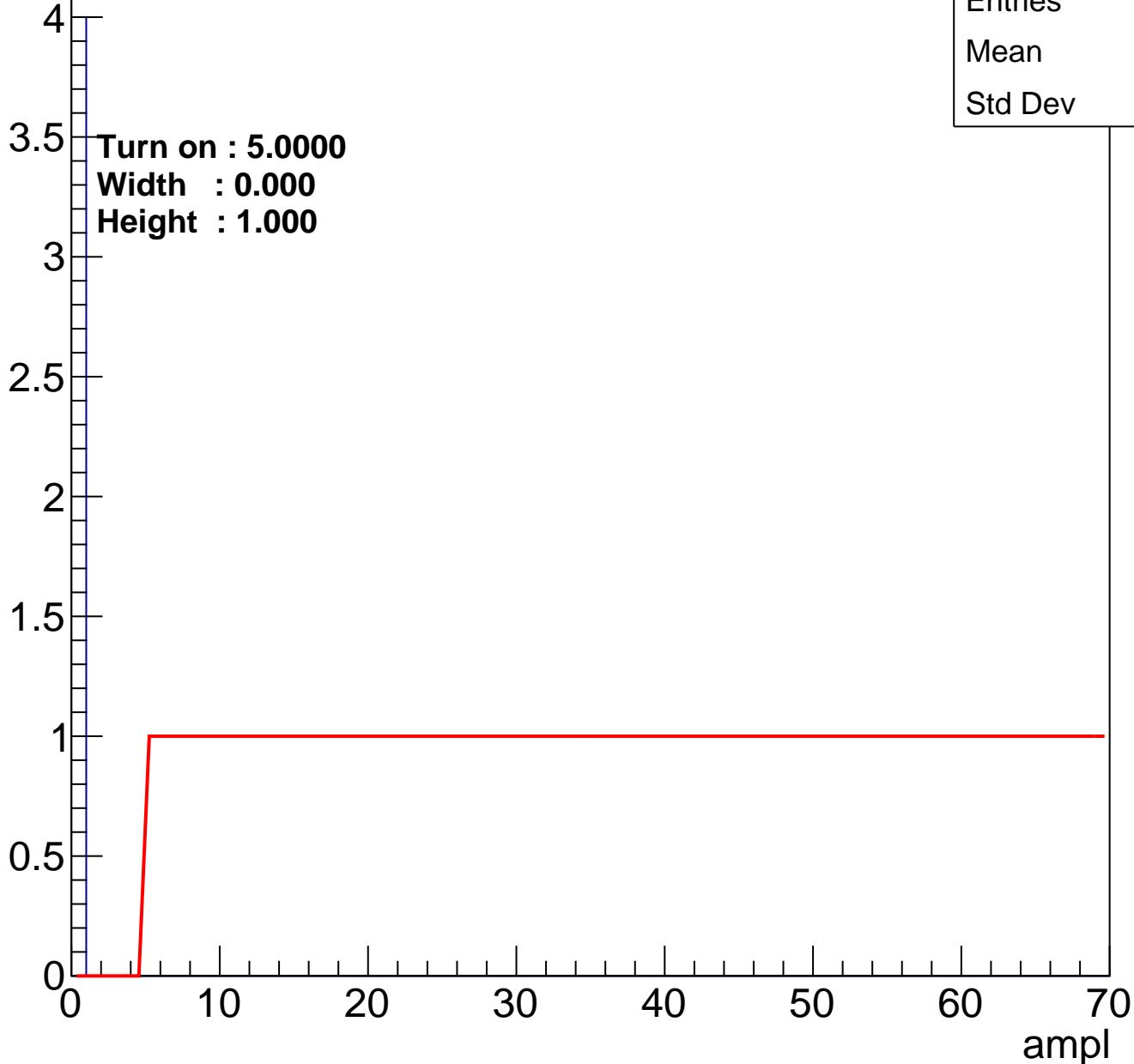
Height : 1.000



B0L101S, U2-ch12

calib_packv5_042523_0143.root, FC#1, port C1

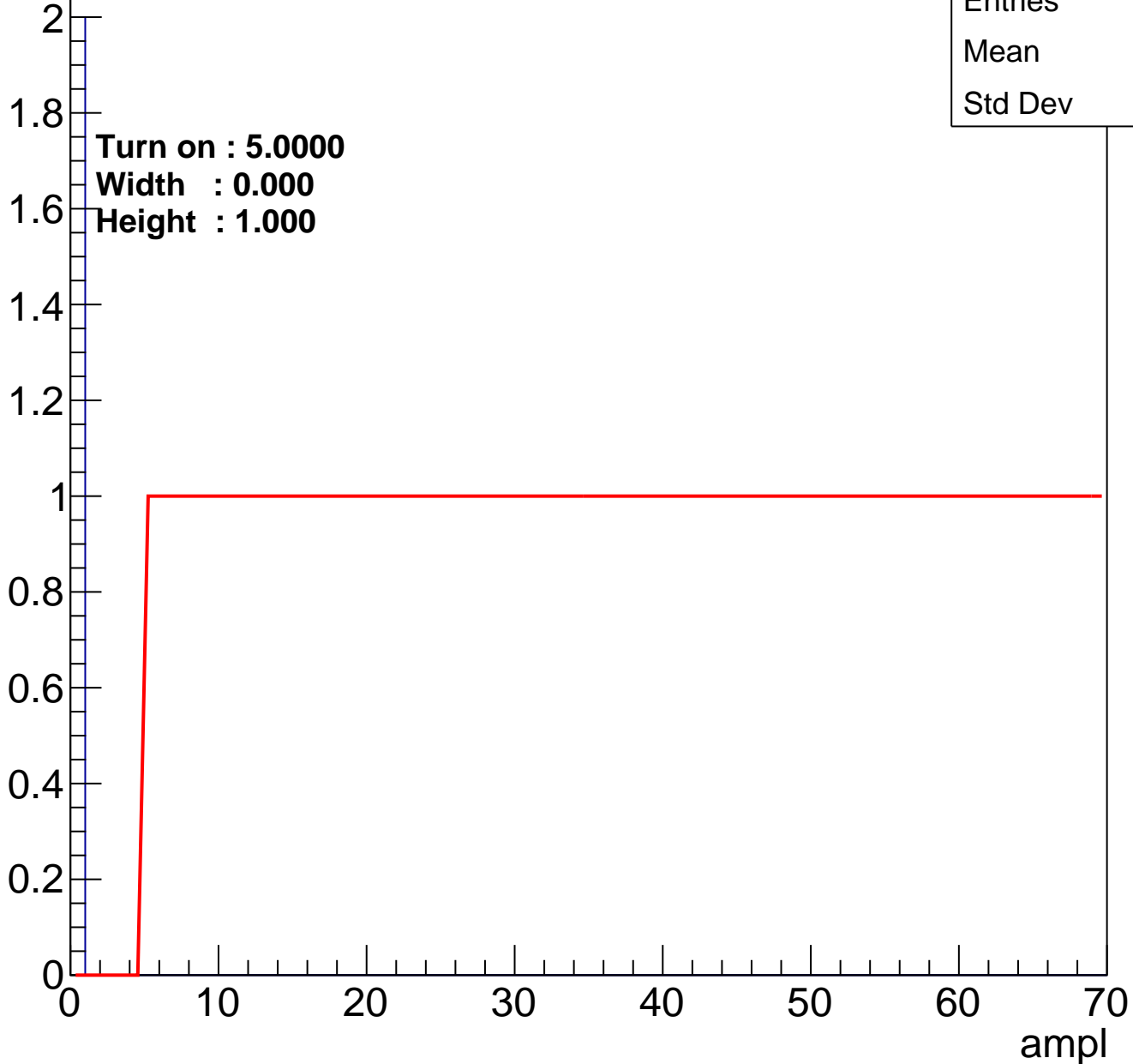
Entry



B0L101S, U2-ch13

calib_packv5_042523_0143.root, FC#1, port C1

Entry



B0L101S, U2-ch14

calib_packv5_042523_0143.root, FC#1, port C1

Entry



B0L101S, U2-ch15

calib_packv5_042523_0143.root, FC#1, port C1

Entry

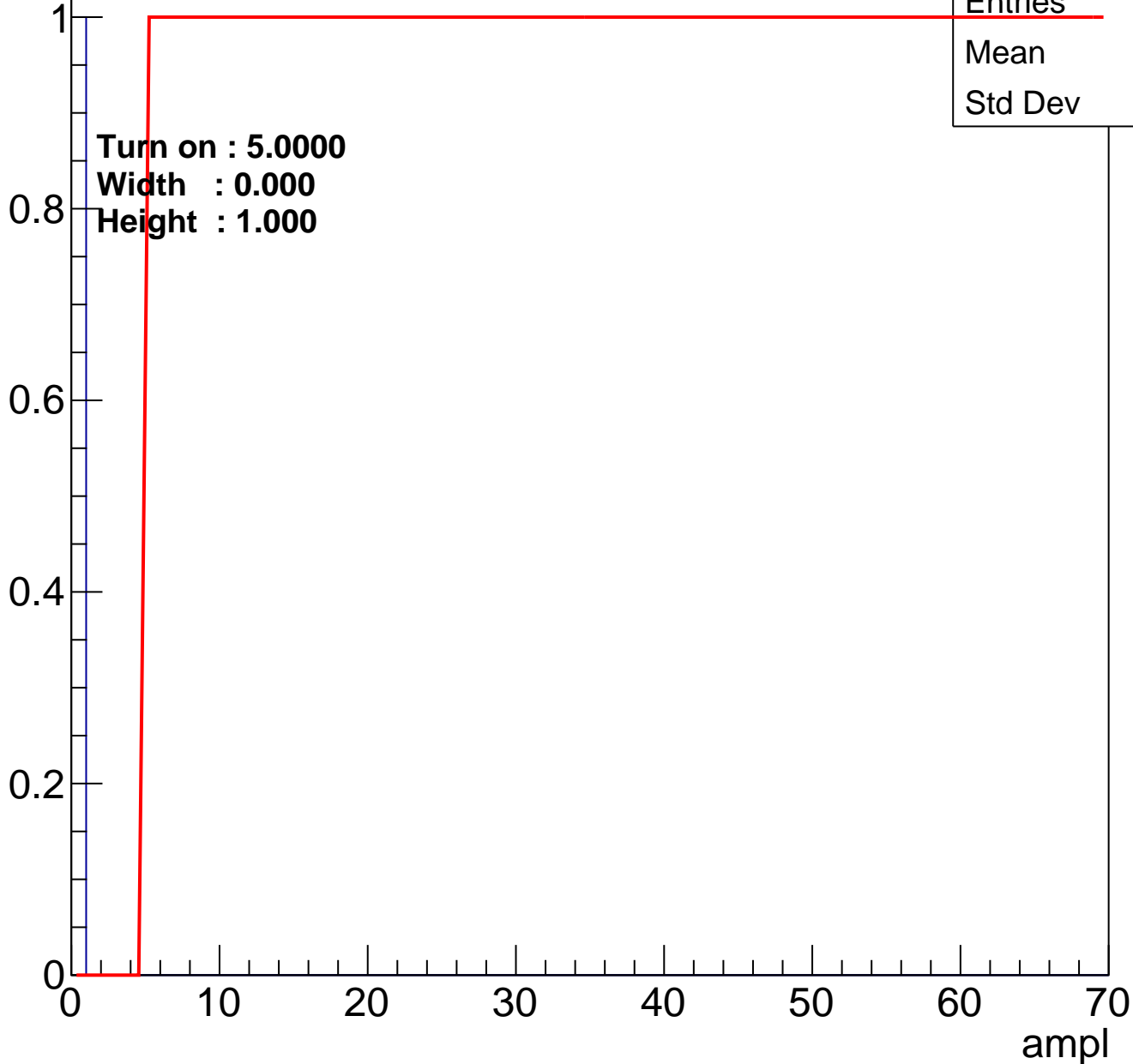


Entries	2
Mean	0
Std Dev	0

B0L101S, U2-ch16

calib_packv5_042523_0143.root, FC#1, port C1

Entry

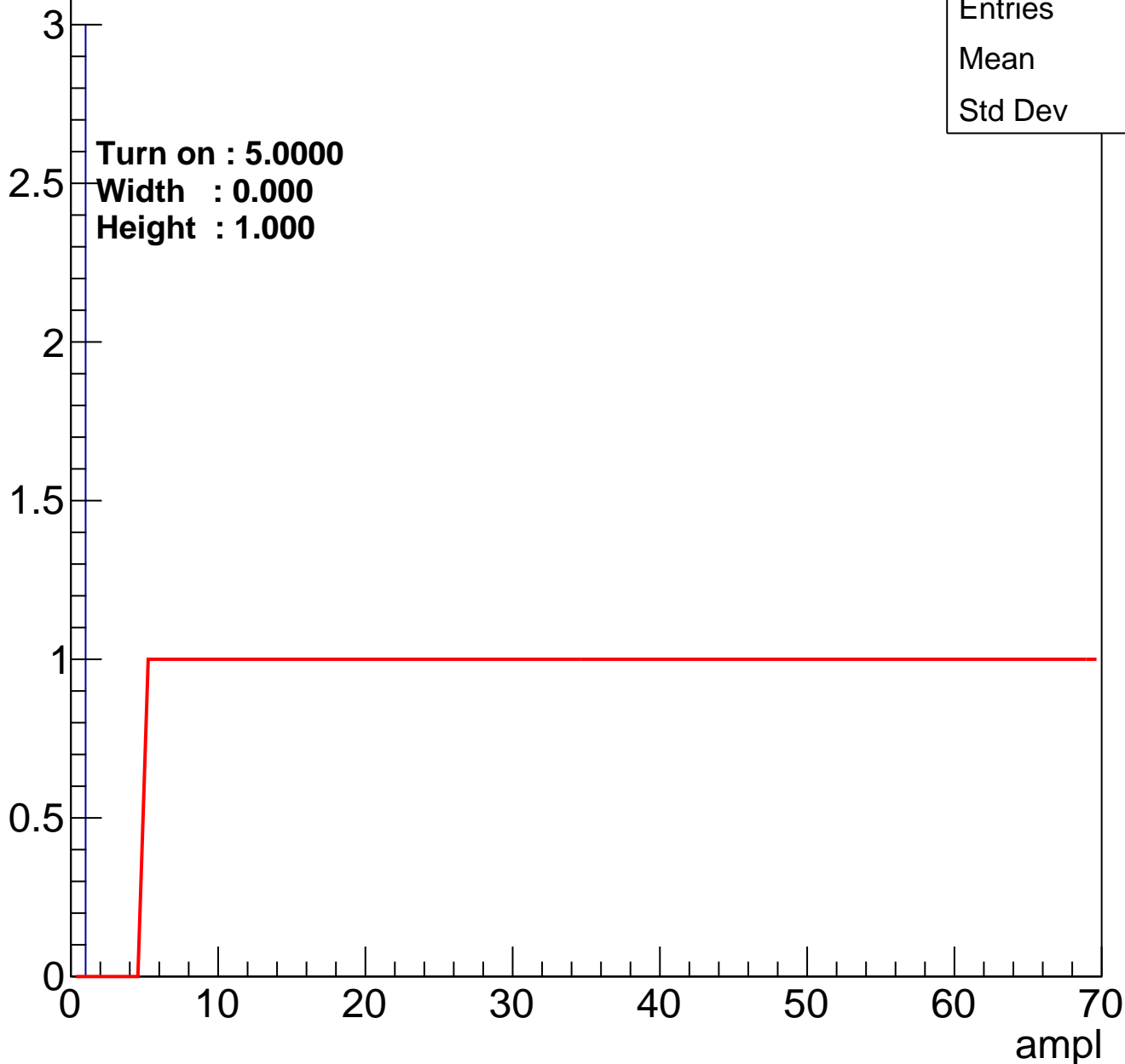


Entries	1
Mean	0
Std Dev	0

B0L101S, U2-ch17

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	3
Mean	0
Std Dev	0

B0L101S, U2-ch18

calib_packv5_042523_0143.root, FC#1, port C1

Entry



B0L101S, U2-ch19

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	2
Mean	0
Std Dev	0

B0L101S, U2-ch20

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	2
Mean	0
Std Dev	0

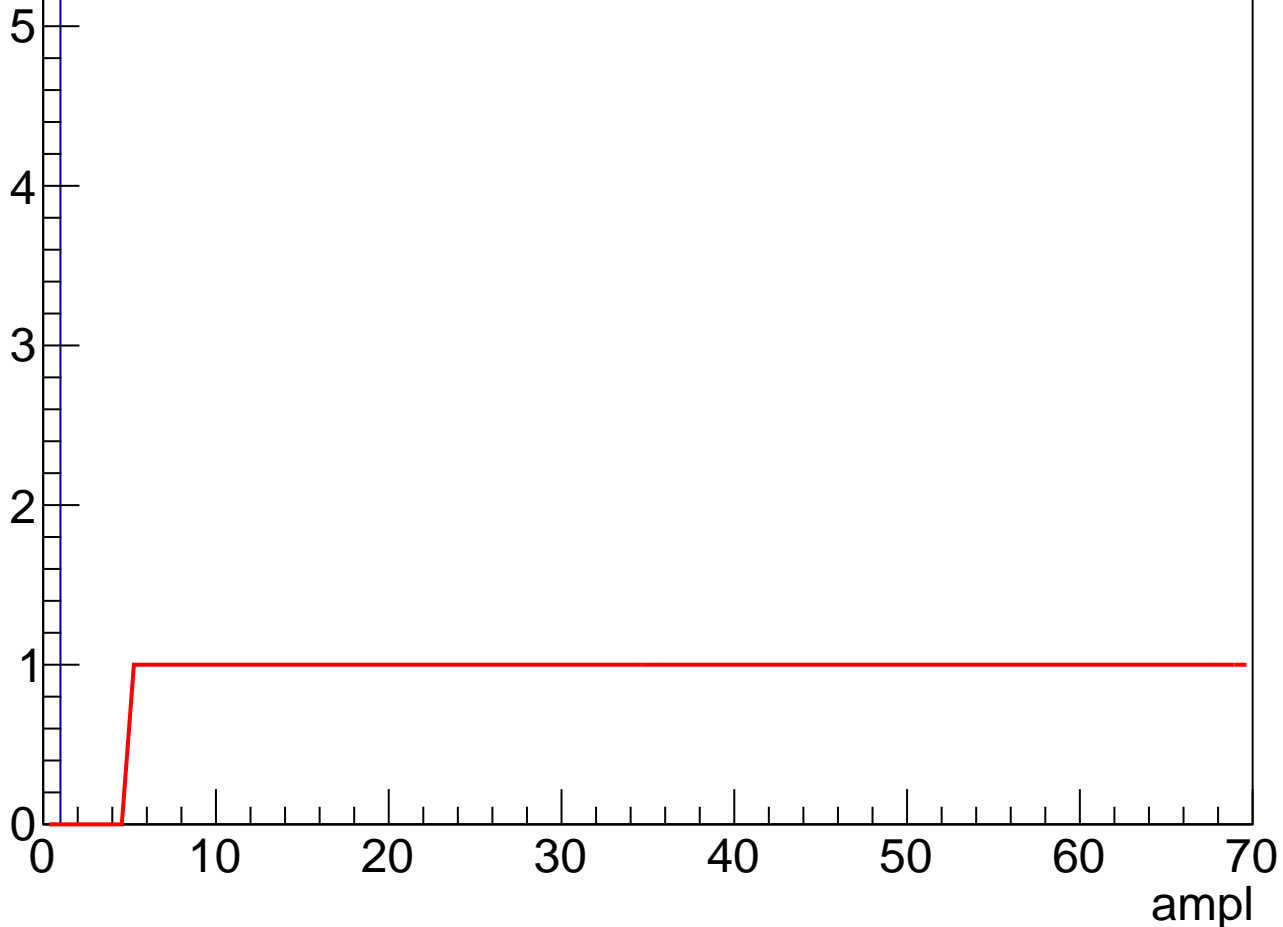
B0L101S, U2-ch21

calib_packv5_042523_0143.root, FC#1, port C1

Entry

Entries	7
Mean	0
Std Dev	0

Turn on : 5.0000
Width : 0.000
Height : 1.000



B0L101S, U2-ch22

calib_packv5_042523_0143.root, FC#1, port C1

Entry



B0L101S, U2-ch23

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	2
Mean	0
Std Dev	0

B0L101S, U2-ch24

calib_packv5_042523_0143.root, FC#1, port C1

Entry

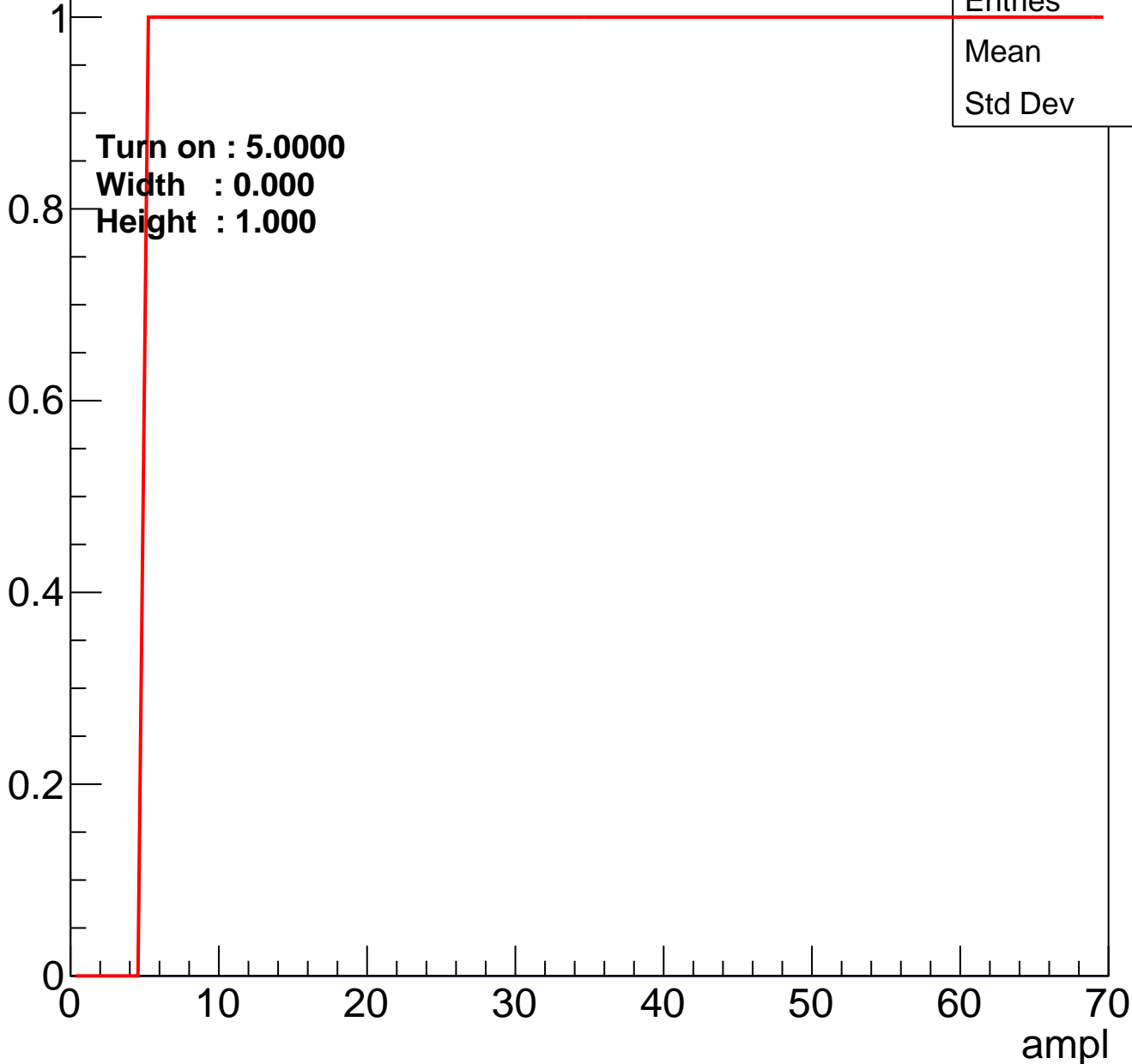


Entries	2
Mean	0
Std Dev	0

B0L101S, U2-ch25

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	0
Mean	0
Std Dev	0

B0L101S, U2-ch26

calib_packv5_042523_0143.root, FC#1, port C1

Entry

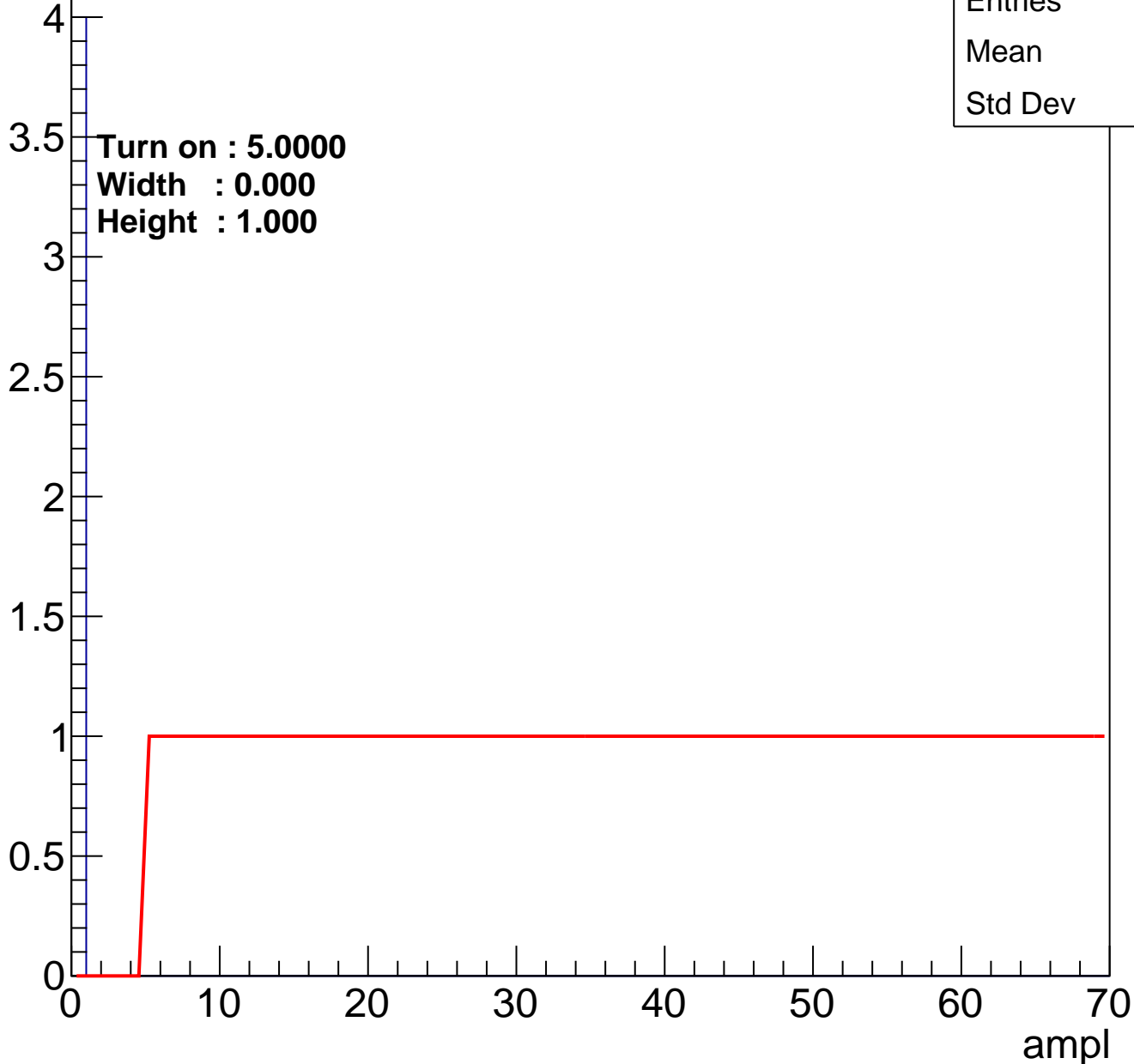


Entries	2
Mean	0
Std Dev	0

B0L101S, U2-ch27

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	4
Mean	0
Std Dev	0

B0L101S, U2-ch28

calib_packv5_042523_0143.root, FC#1, port C1

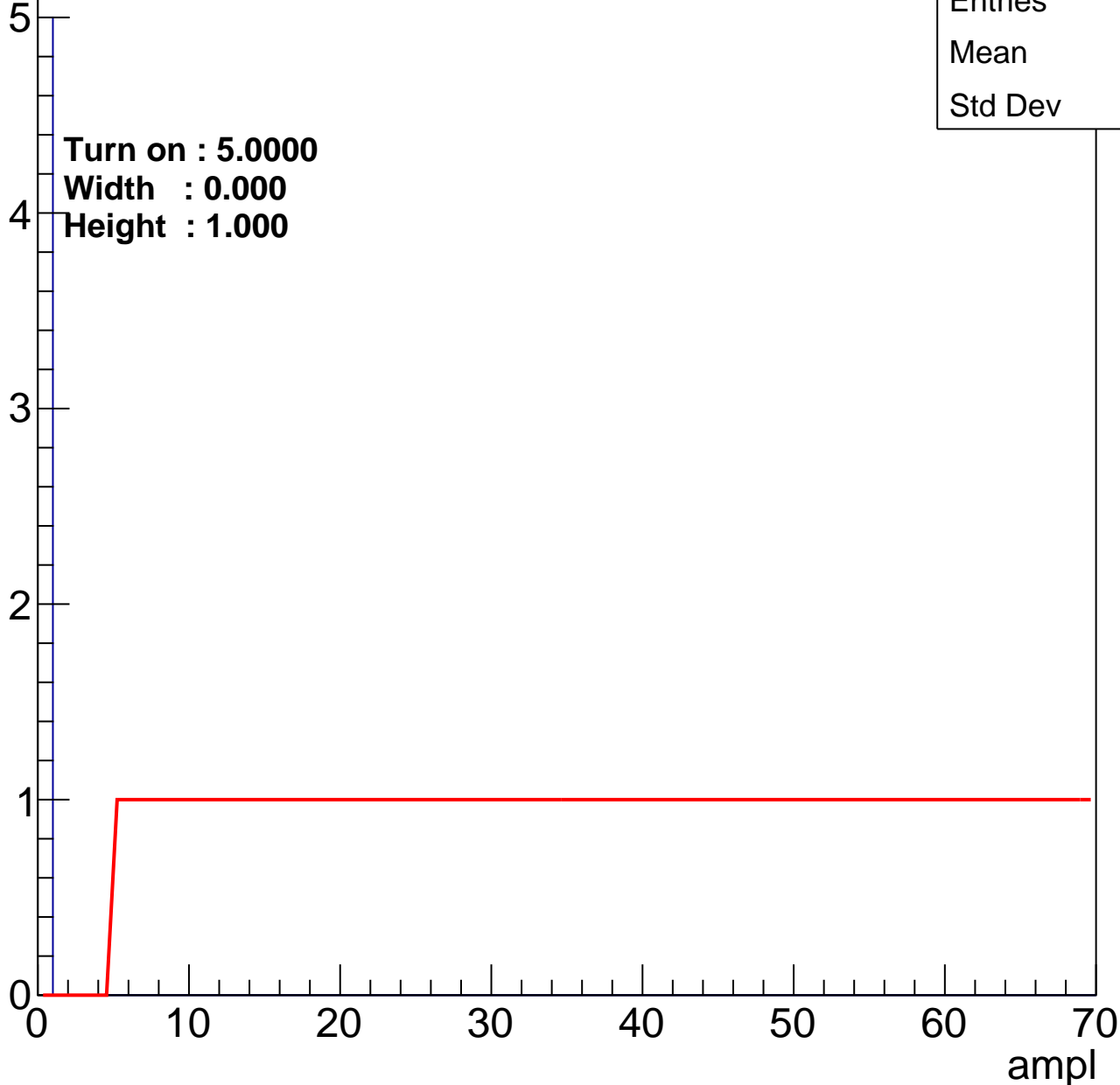
Entry

Entries	5
Mean	0
Std Dev	0

Turn on : 5.0000

Width : 0.000

Height : 1.000



B0L101S, U2-ch29

calib_packv5_042523_0143.root, FC#1, port C1

Entry

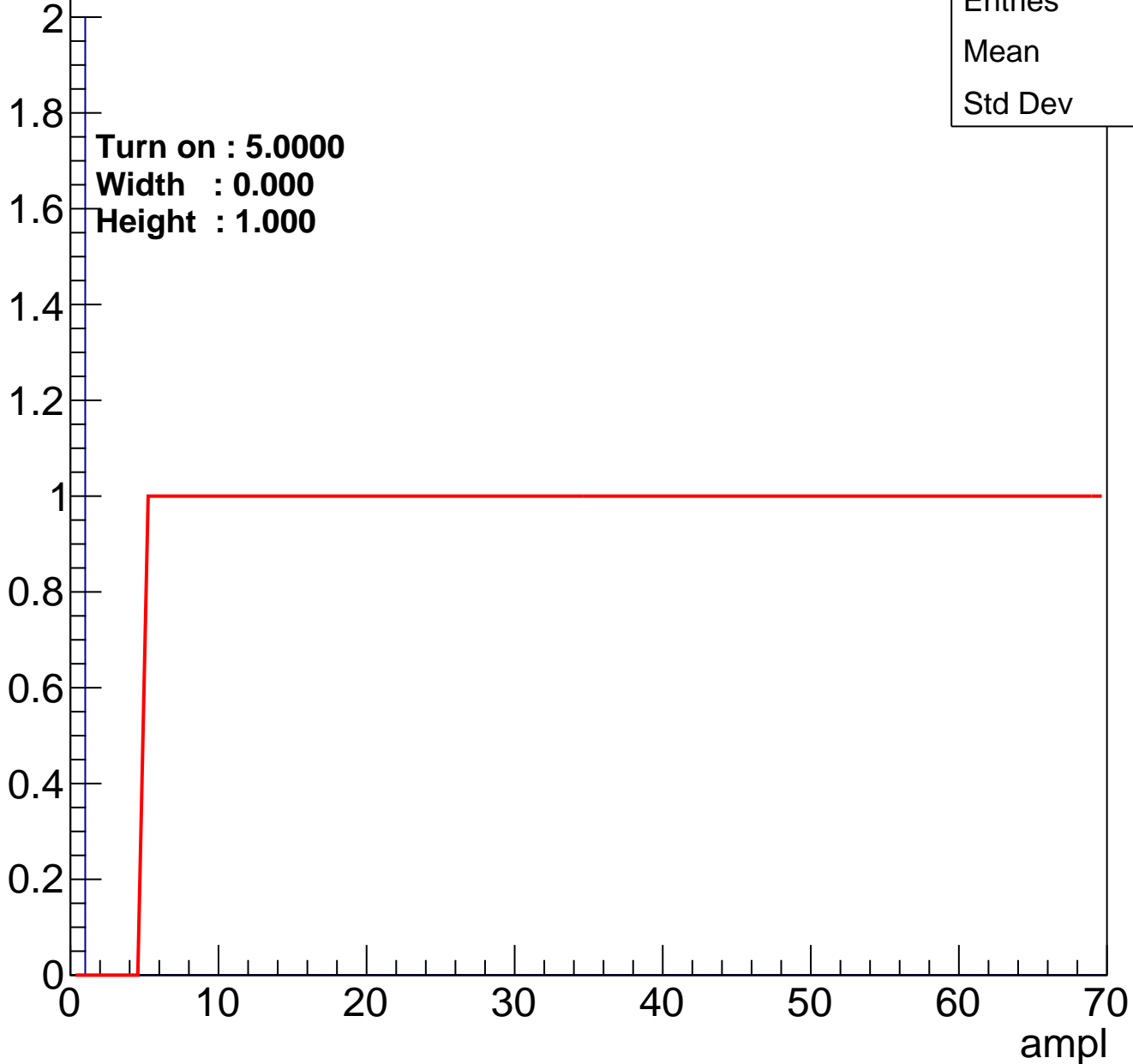


Entries	2
Mean	0
Std Dev	0

B0L101S, U2-ch30

calib_packv5_042523_0143.root, FC#1, port C1

Entry



B0L101S, U2-ch31

calib_packv5_042523_0143.root, FC#1, port C1

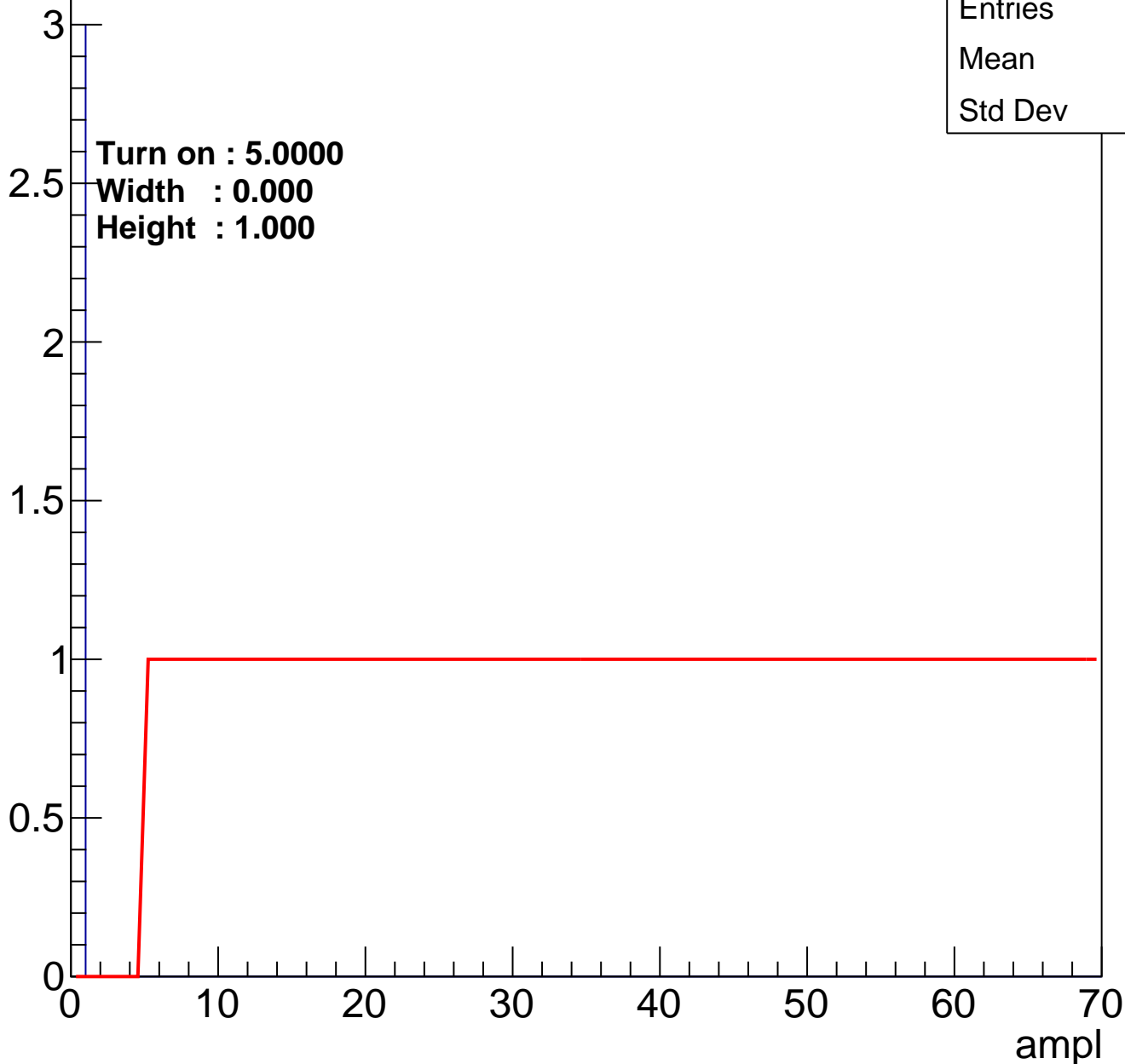
Entry



B0L101S, U2-ch32

calib_packv5_042523_0143.root, FC#1, port C1

Entry

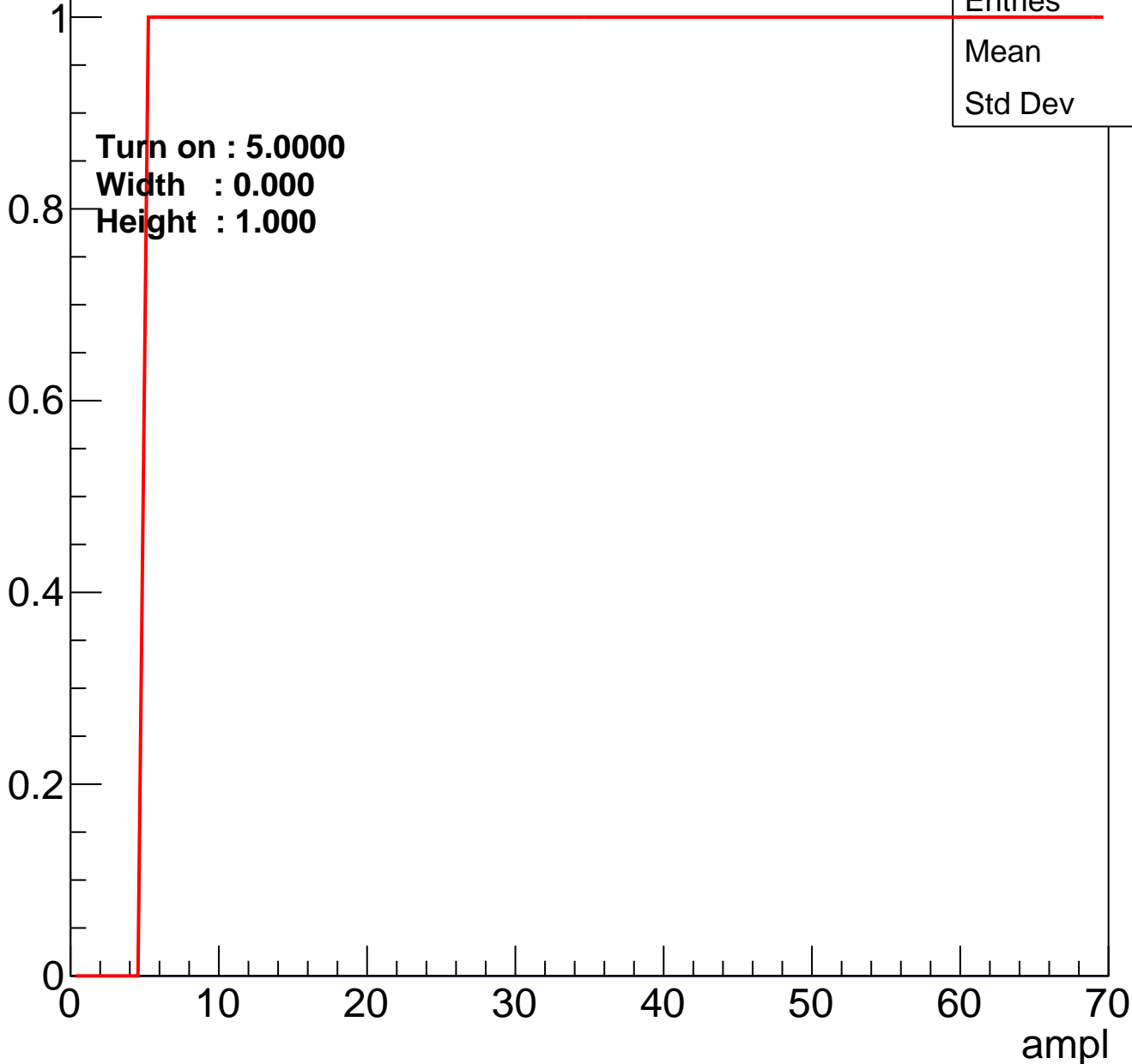


Entries	3
Mean	0
Std Dev	0

B0L101S, U2-ch33

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	0
Mean	0
Std Dev	0

B0L101S, U2-ch34

calib_packv5_042523_0143.root, FC#1, port C1

Entry

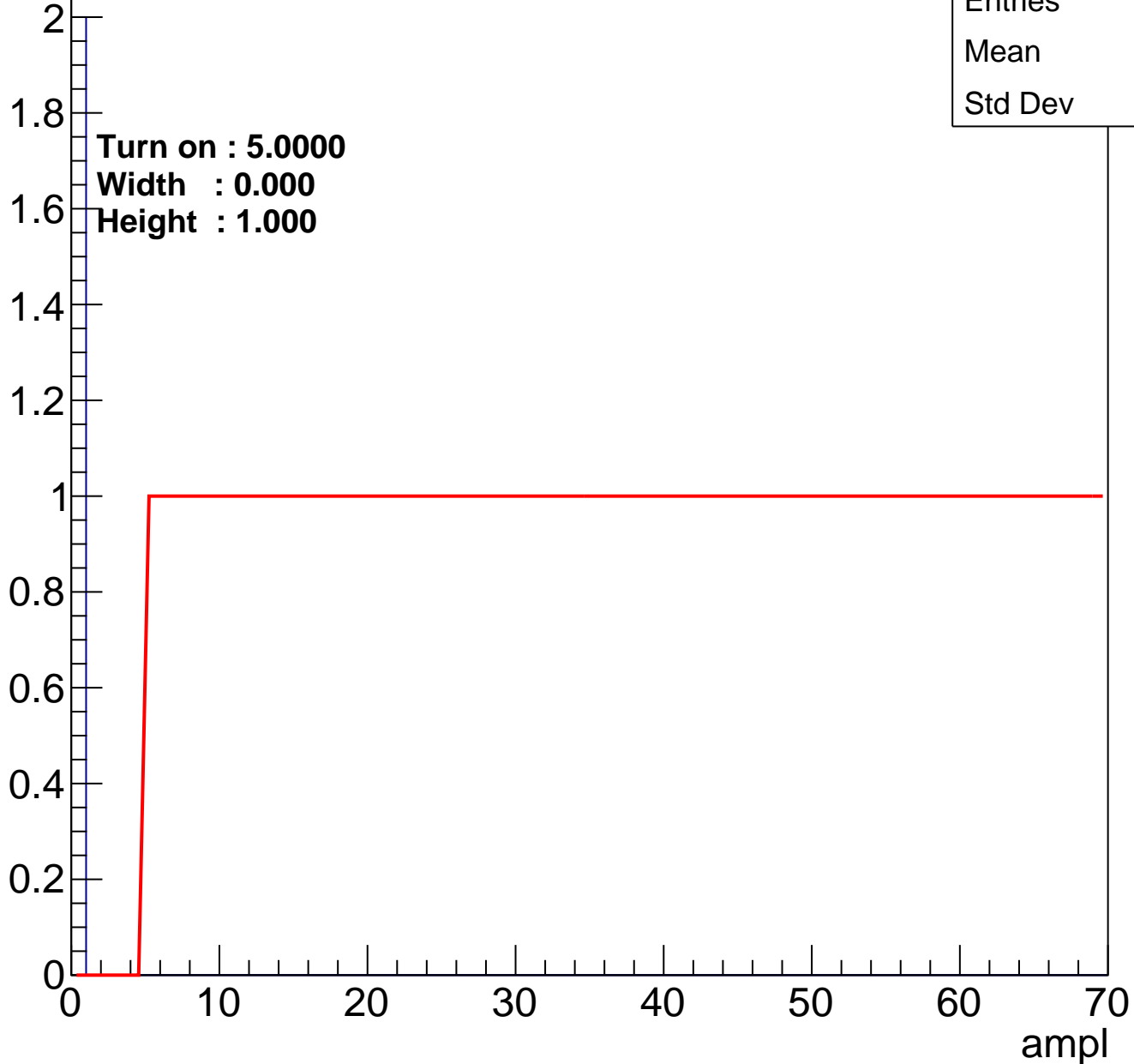


Entries	2
Mean	0
Std Dev	0

B0L101S, U2-ch35

calib_packv5_042523_0143.root, FC#1, port C1

Entry



B0L101S, U2-ch36

calib_packv5_042523_0143.root, FC#1, port C1

Entry

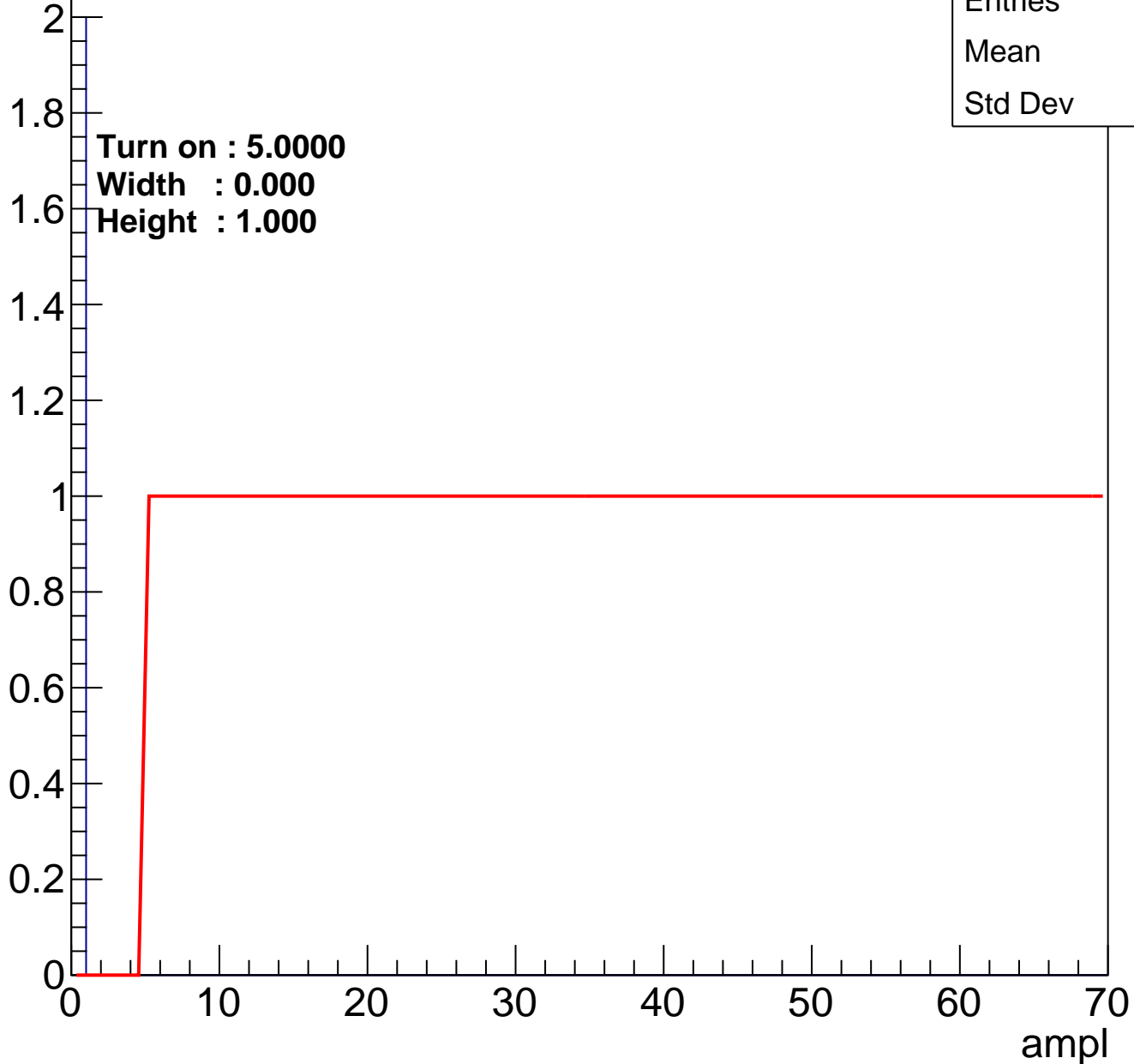


Entries	0
Mean	0
Std Dev	0

B0L101S, U2-ch37

calib_packv5_042523_0143.root, FC#1, port C1

Entry



B0L101S, U2-ch38

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	0
Mean	0
Std Dev	0

B0L101S, U2-ch39

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	2
Mean	0
Std Dev	0

B0L101S, U2-ch40

calib_packv5_042523_0143.root, FC#1, port C1

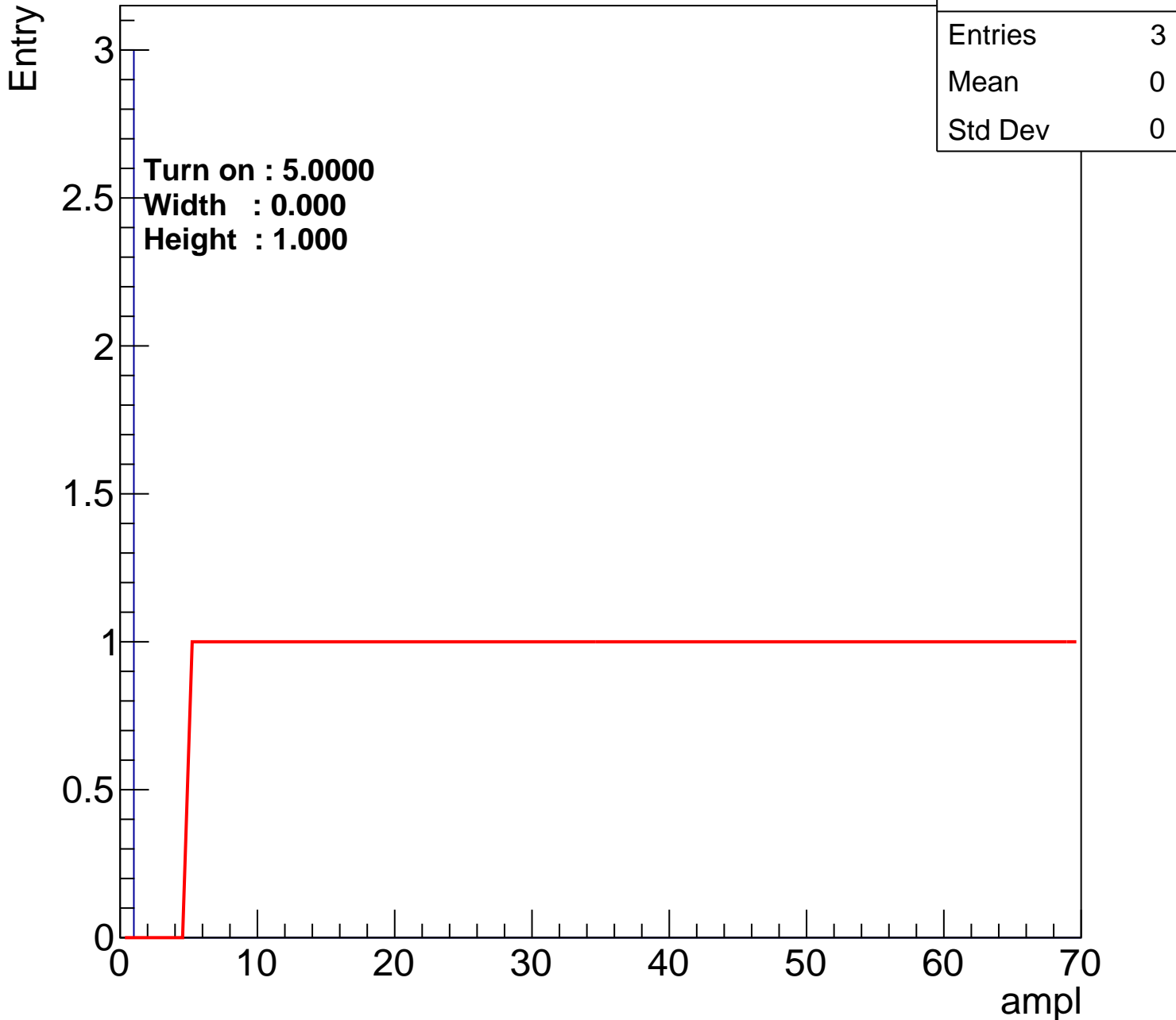
Entry

3
2.5
2
1.5
1
0.5
0

Turn on : 5.0000
Width : 0.000
Height : 1.000

Entries	3
Mean	0
Std Dev	0

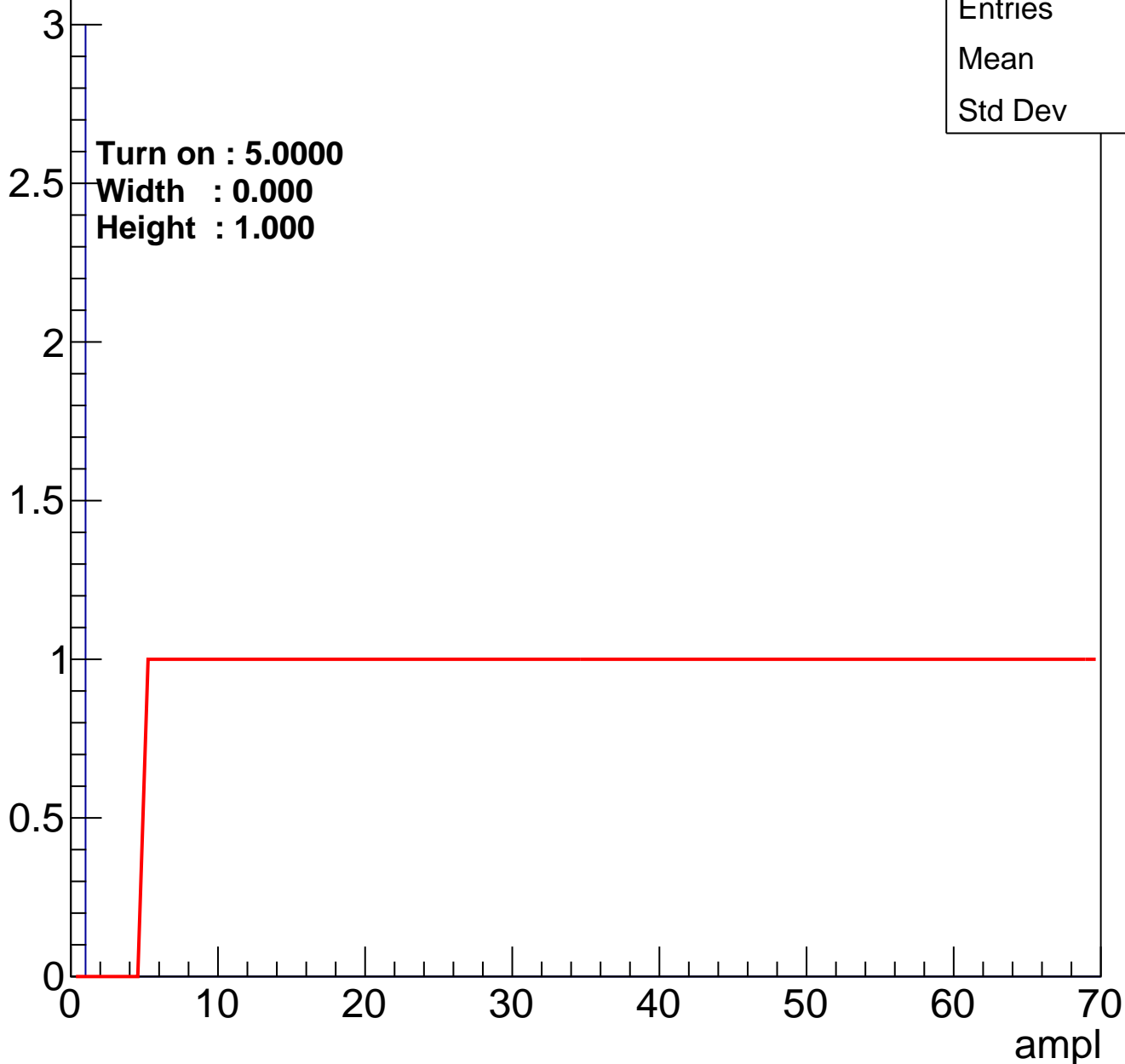
ampl



B0L101S, U2-ch41

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	3
Mean	0
Std Dev	0

B0L101S, U2-ch42

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	0
Mean	0
Std Dev	0

B0L101S, U2-ch43

calib_packv5_042523_0143.root, FC#1, port C1

Entry

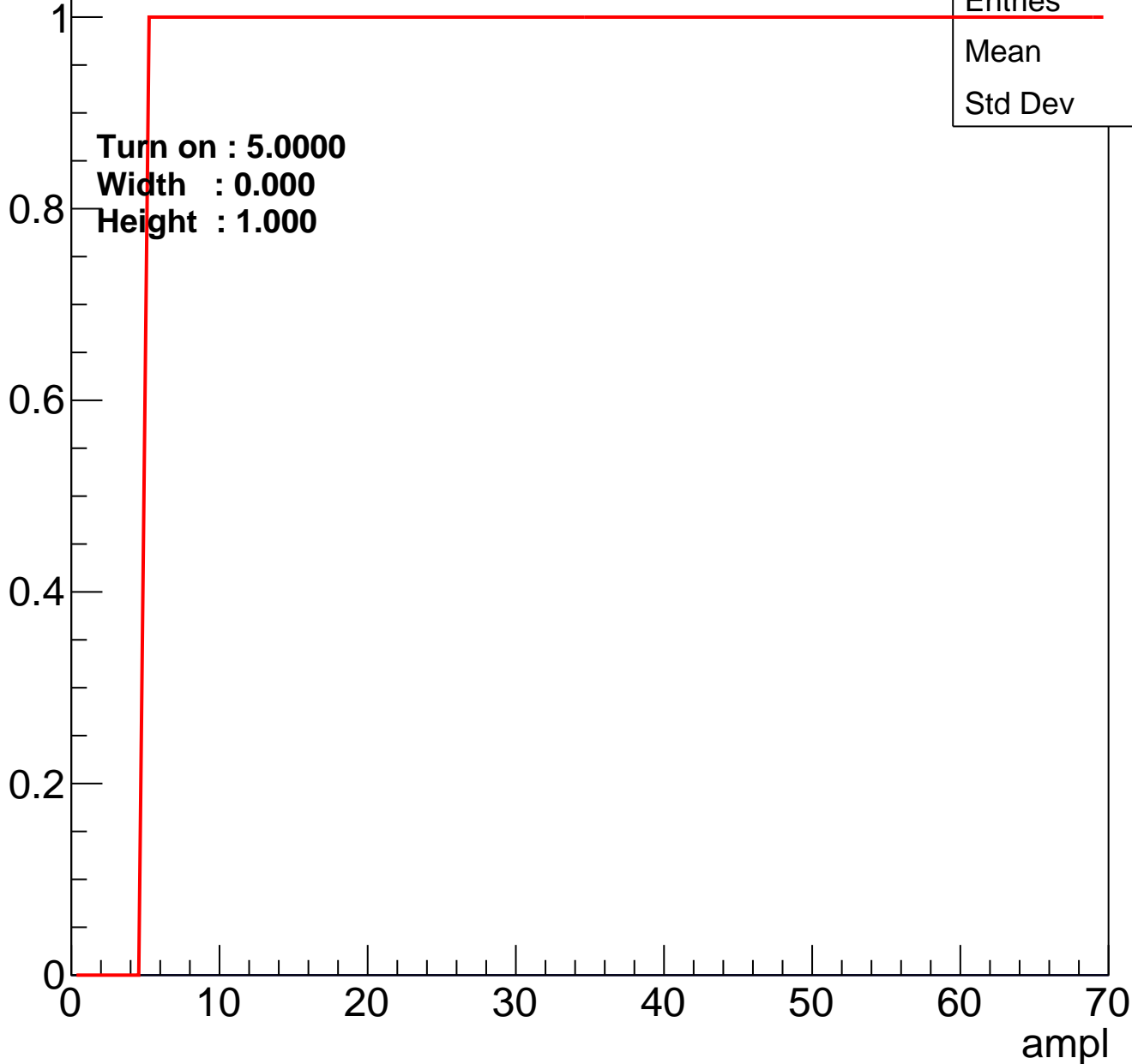


Entries	1
Mean	0
Std Dev	0

B0L101S, U2-ch44

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	0
Mean	0
Std Dev	0

B0L101S, U2-ch45

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	1
Mean	0
Std Dev	0

B0L101S, U2-ch46

calib_packv5_042523_0143.root, FC#1, port C1

Entry



B0L101S, U2-ch47

calib_packv5_042523_0143.root, FC#1, port C1

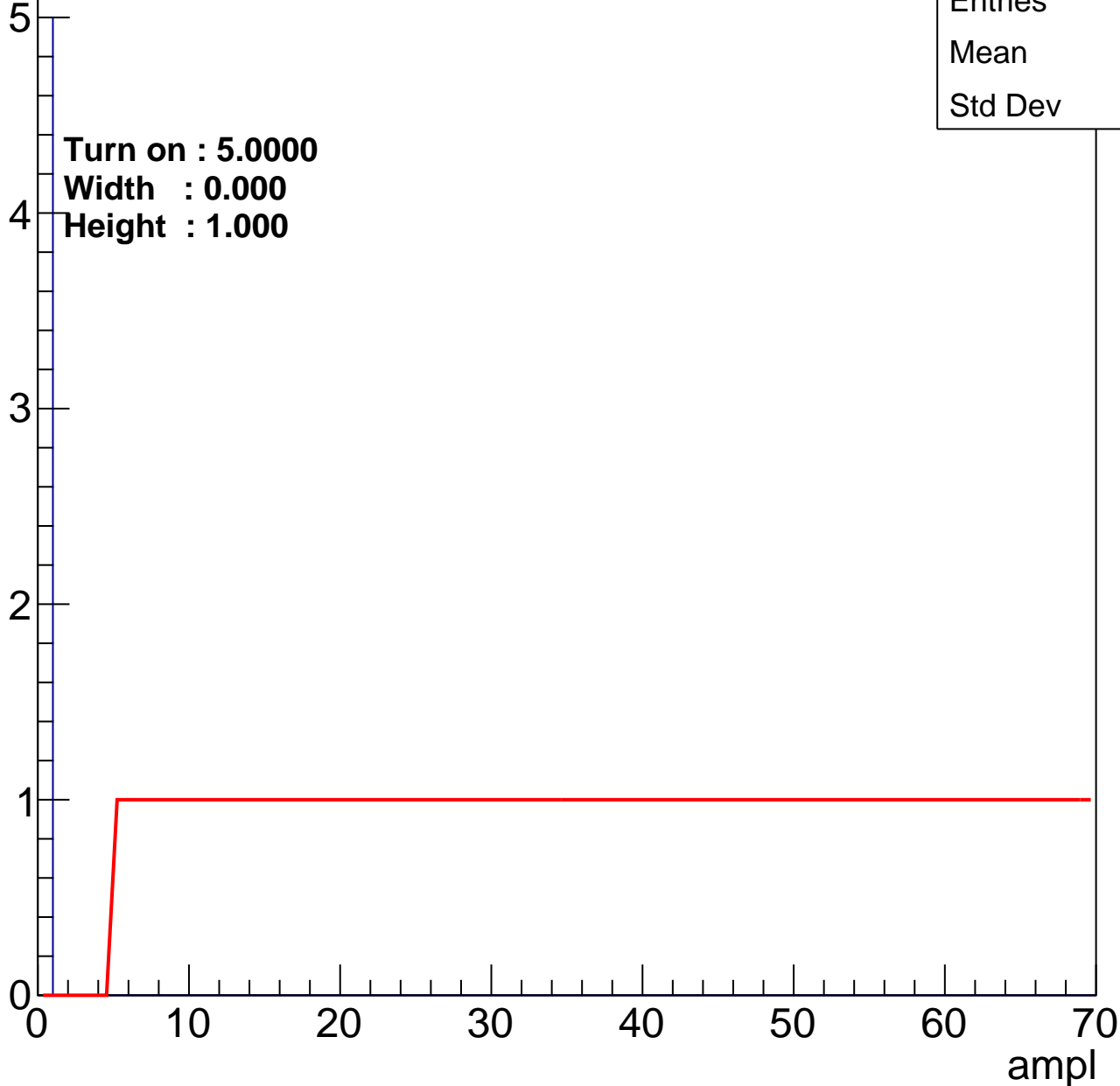
Entry

Entries	5
Mean	0
Std Dev	0

Turn on : 5.0000

Width : 0.000

Height : 1.000



B0L101S, U2-ch48

calib_packv5_042523_0143.root, FC#1, port C1

Entry

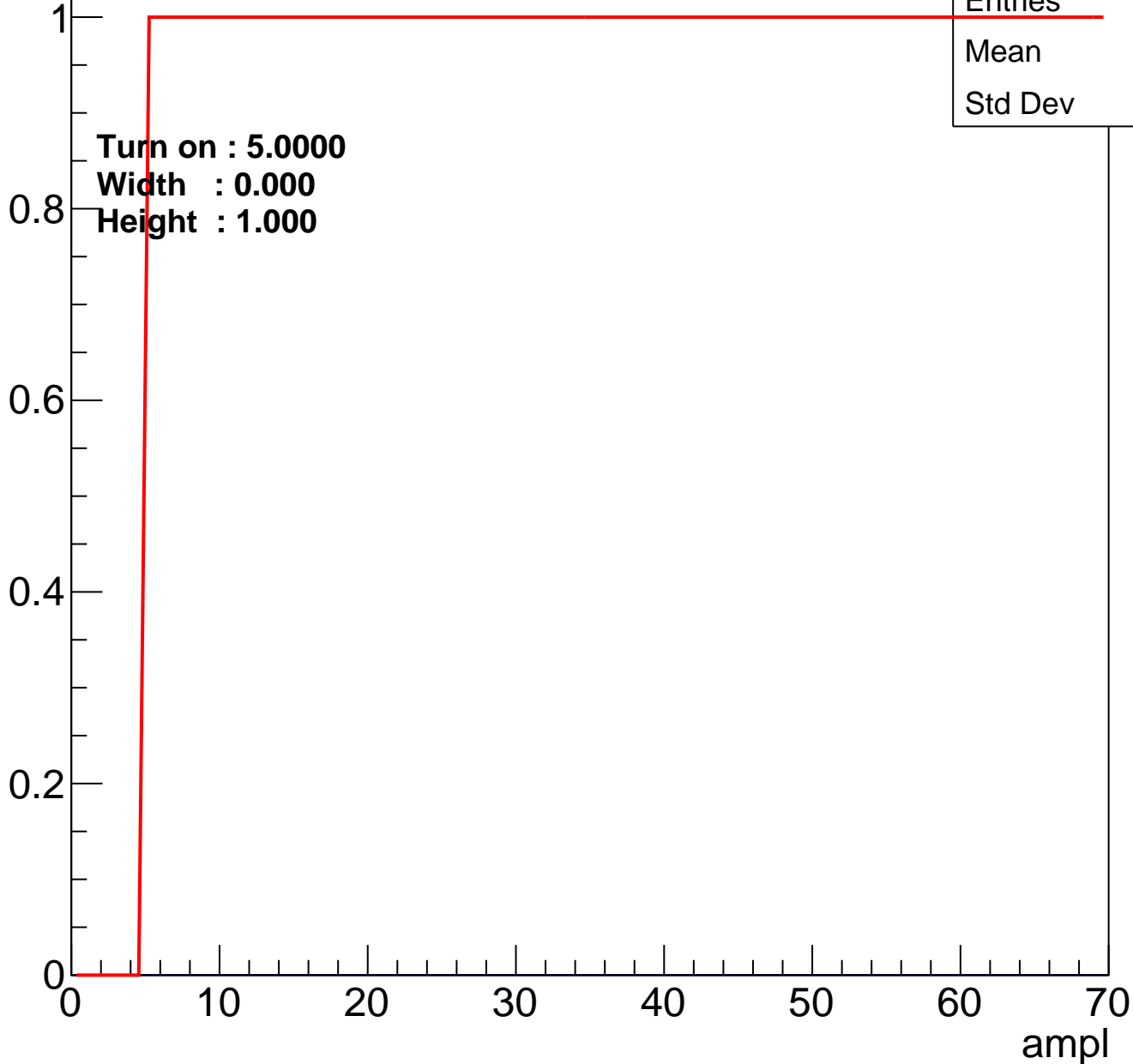


Entries	2
Mean	0
Std Dev	0

B0L101S, U2-ch49

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	0
Mean	0
Std Dev	0

B0L101S, U2-ch50

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	0
Mean	0
Std Dev	0

B0L101S, U2-ch51

calib_packv5_042523_0143.root, FC#1, port C1

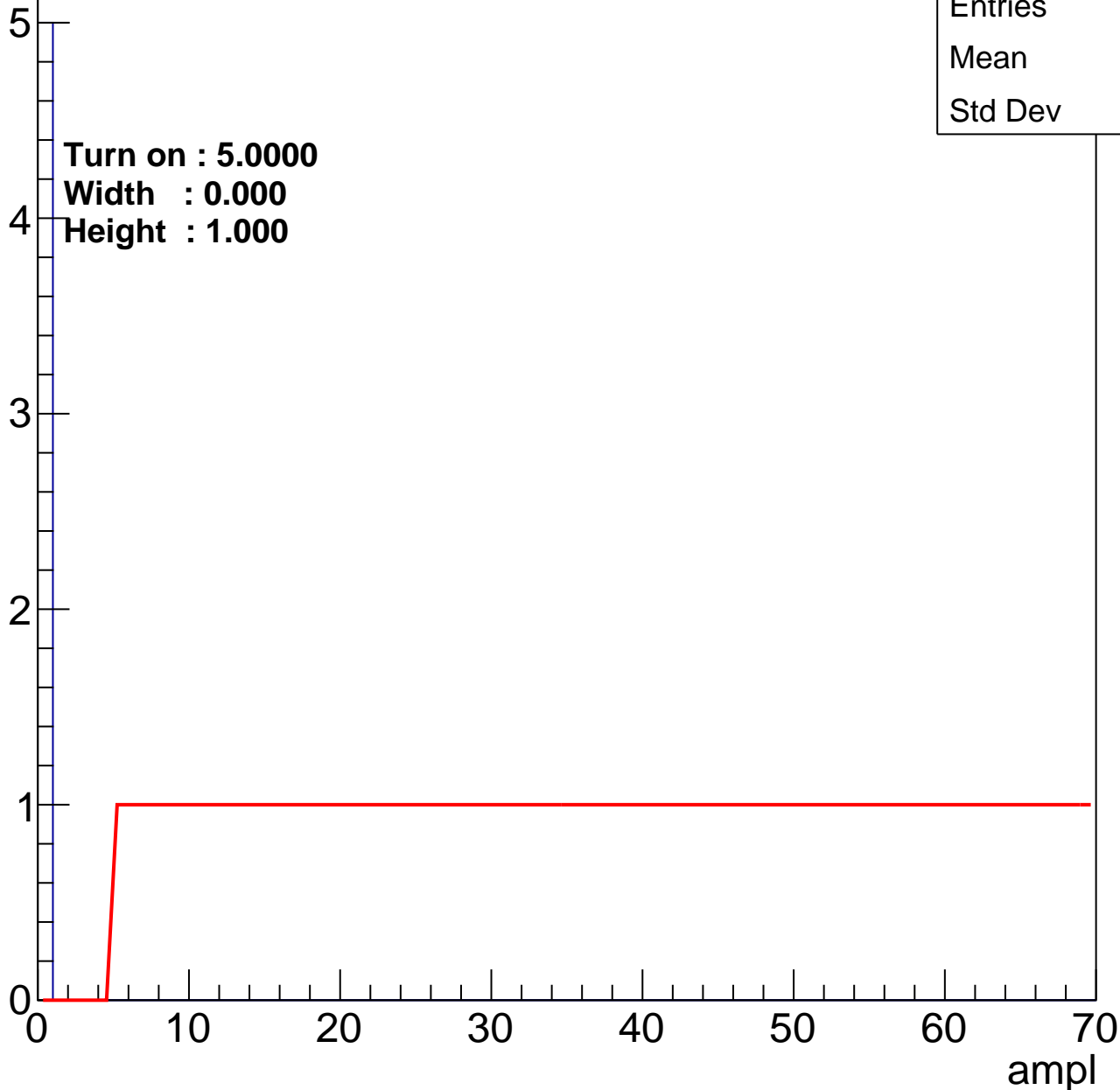
Entry

Entries	5
Mean	0
Std Dev	0

Turn on : 5.0000

Width : 0.000

Height : 1.000



B0L101S, U2-ch52

calib_packv5_042523_0143.root, FC#1, port C1

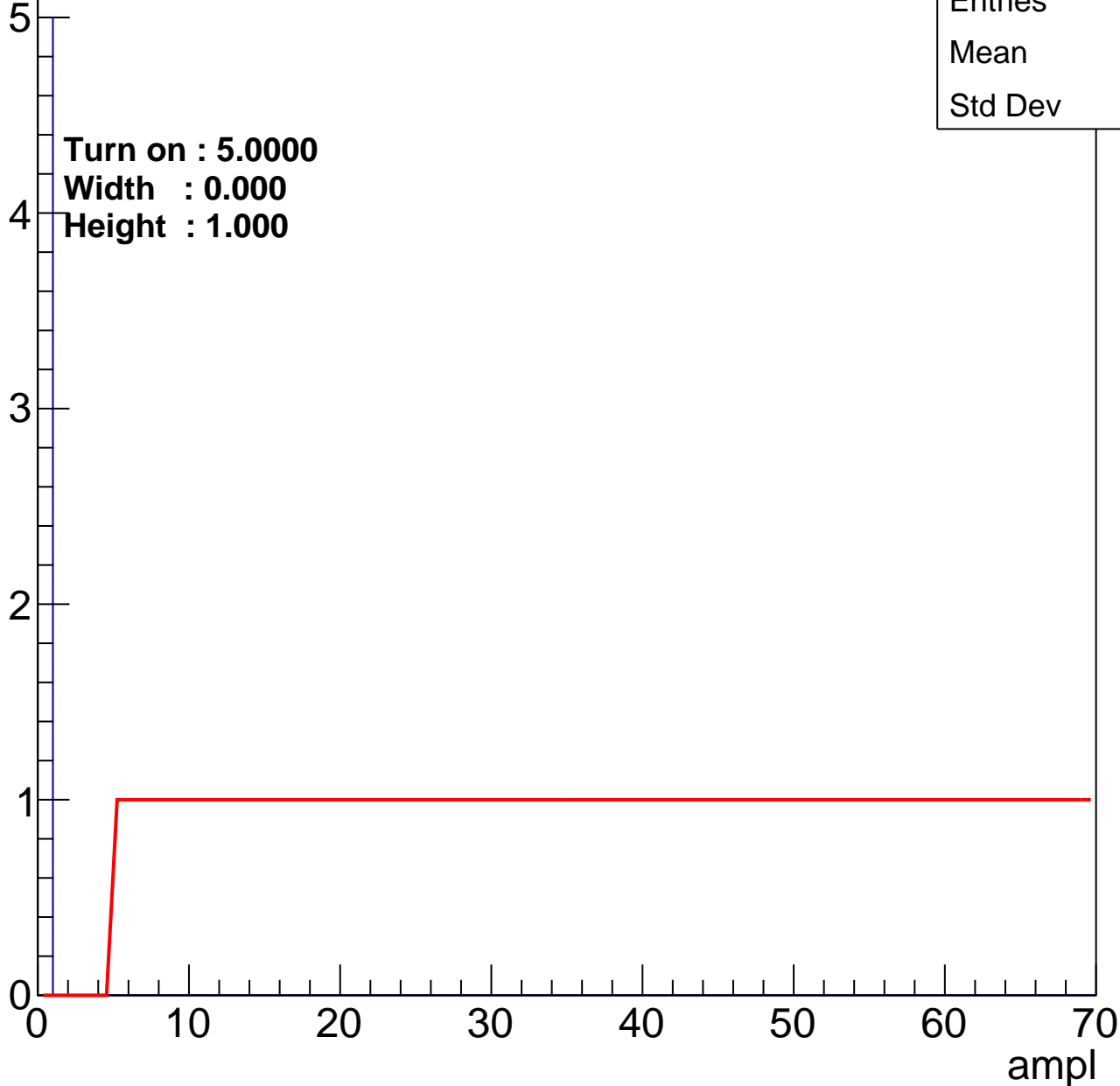
Entry

Entries	5
Mean	0
Std Dev	0

Turn on : 5.0000

Width : 0.000

Height : 1.000



B0L101S, U2-ch53

calib_packv5_042523_0143.root, FC#1, port C1

Entry

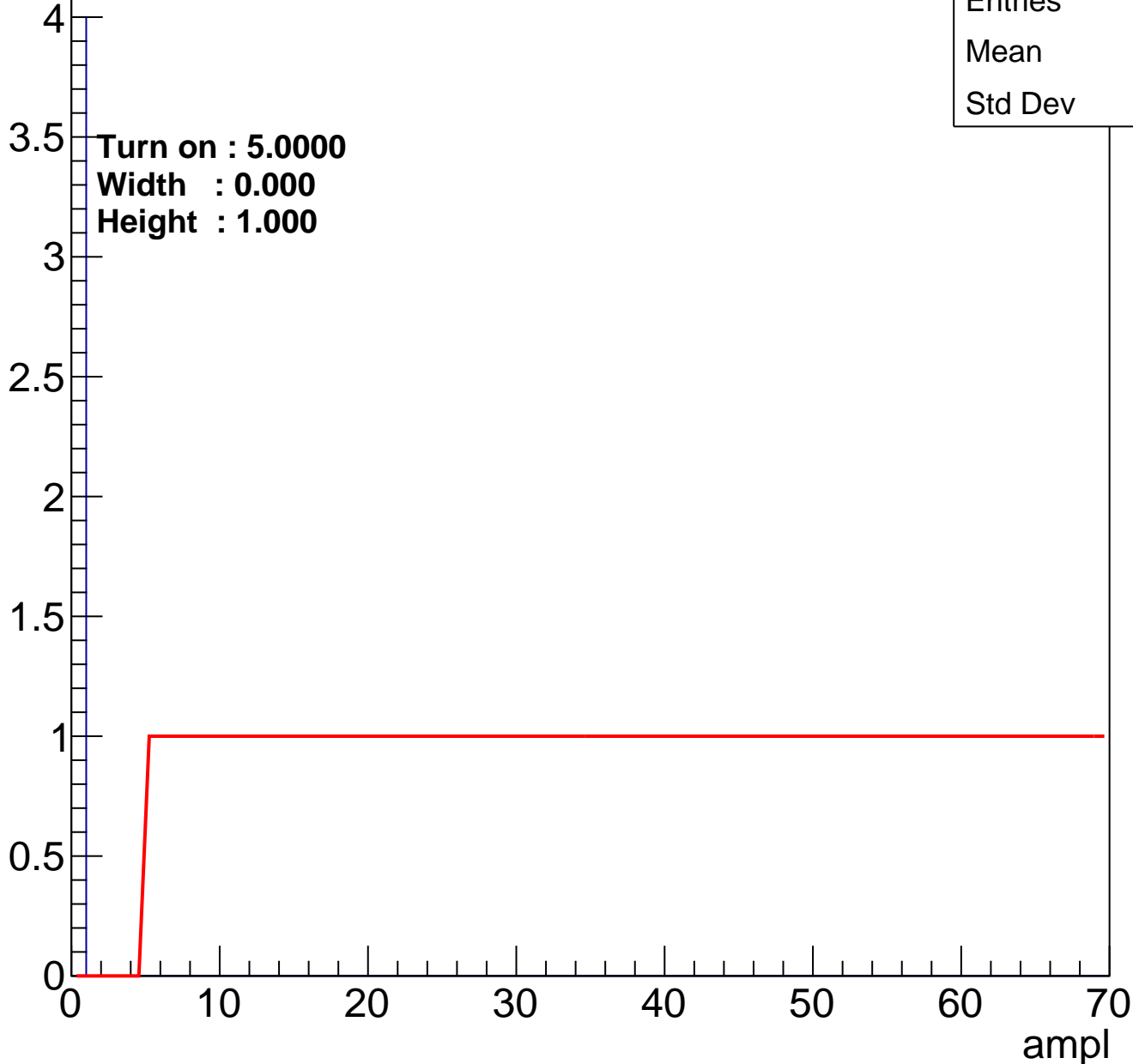


Entries	2
Mean	0
Std Dev	0

B0L101S, U2-ch54

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	4
Mean	0
Std Dev	0

B0L101S, U2-ch55

calib_packv5_042523_0143.root, FC#1, port C1

Entry

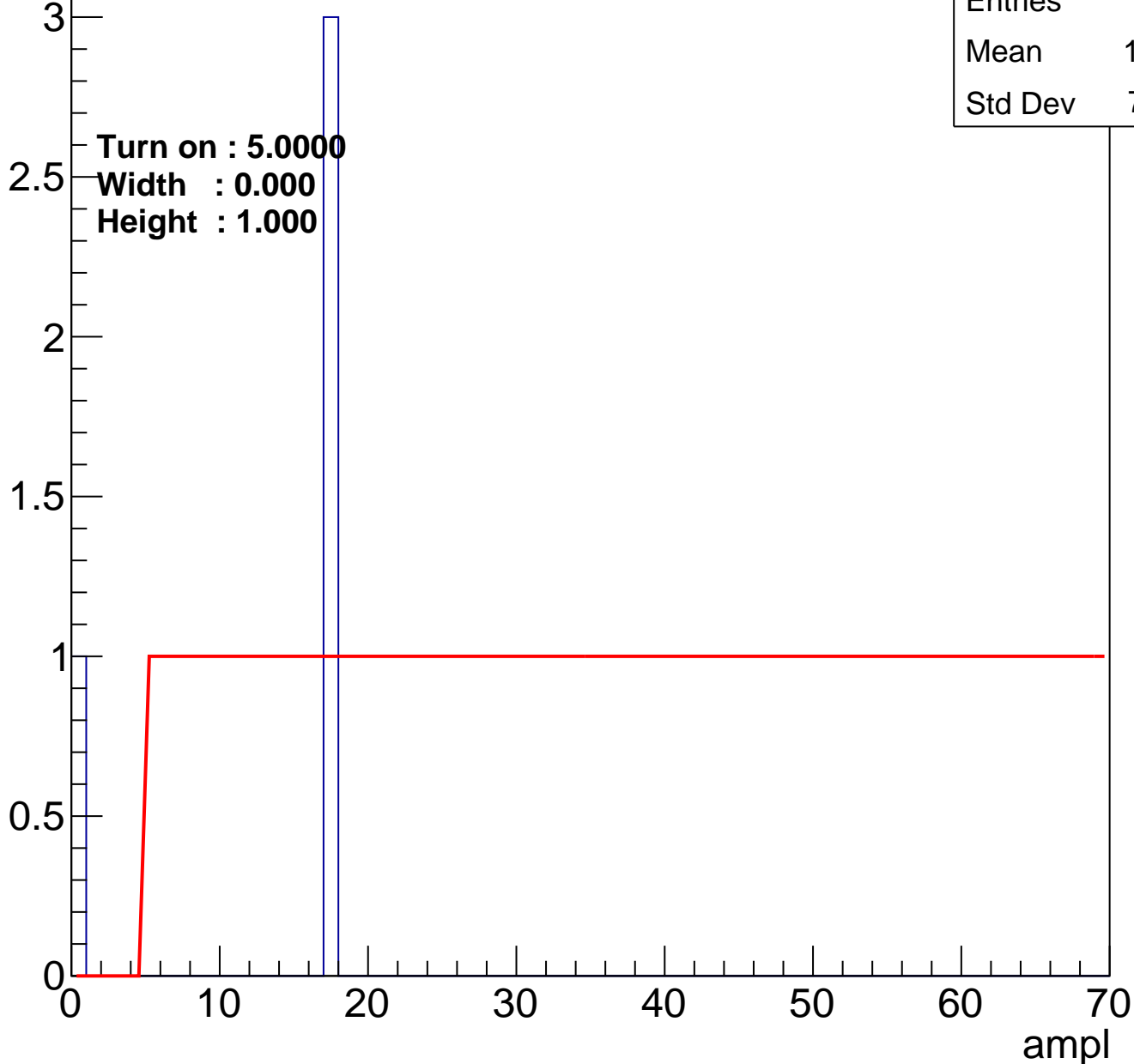


Entries	2
Mean	0
Std Dev	0

B0L101S, U2-ch56

calib_packv5_042523_0143.root, FC#1, port C1

Entry



B0L101S, U2-ch57

calib_packv5_042523_0143.root, FC#1, port C1

Entry

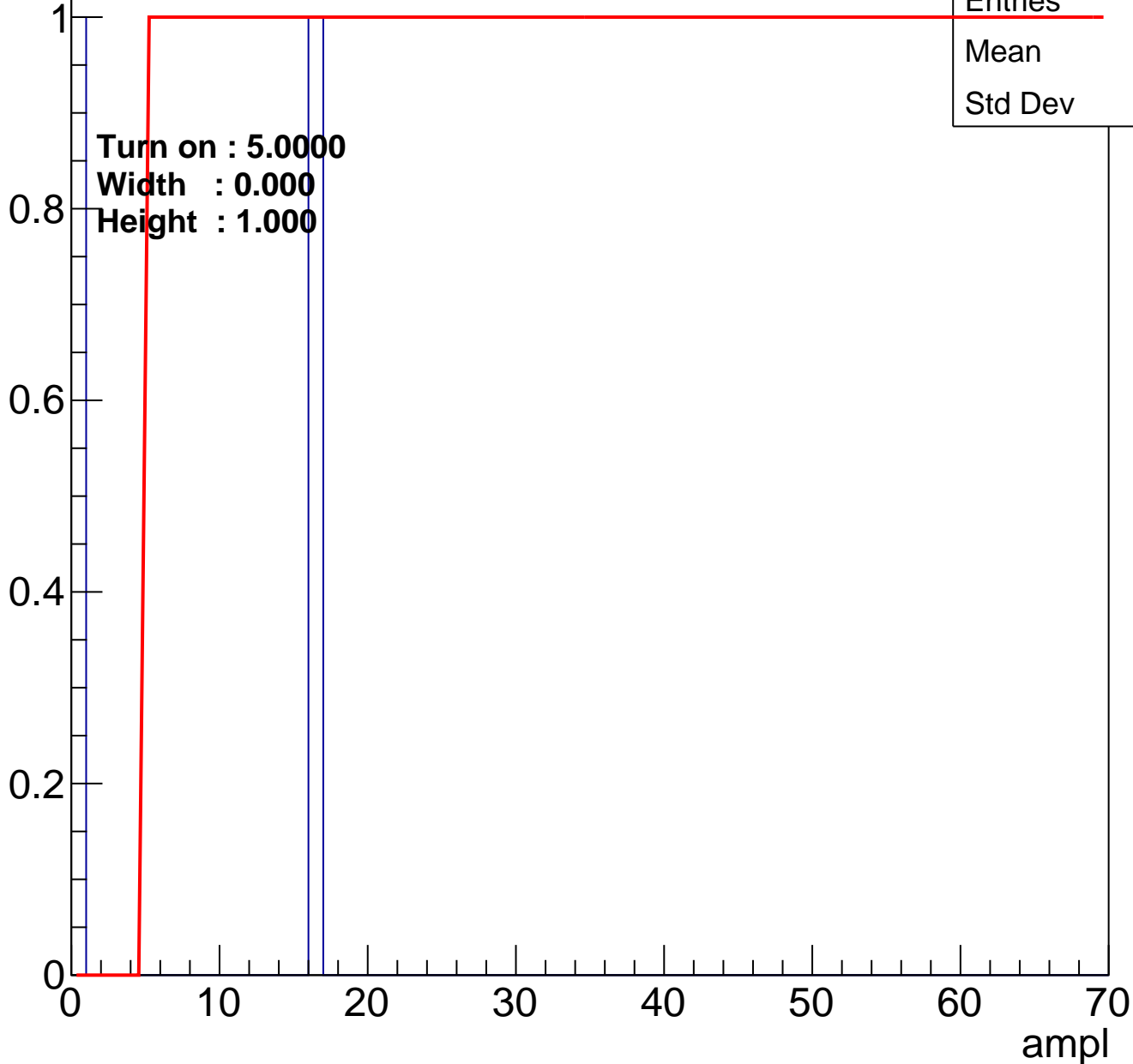


Entries	0
Mean	0
Std Dev	0

B0L101S, U2-ch58

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	2
Mean	8
Std Dev	8

B0L101S, U2-ch59

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	2
Mean	0
Std Dev	0

B0L101S, U2-ch60

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	2
Mean	0
Std Dev	0

B0L101S, U2-ch61

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	2
Mean	0
Std Dev	0

B0L101S, U2-ch62

calib_packv5_042523_0143.root, FC#1, port C1

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Turn on : 5.0000

Width : 0.000

Height : 1.000

Entries

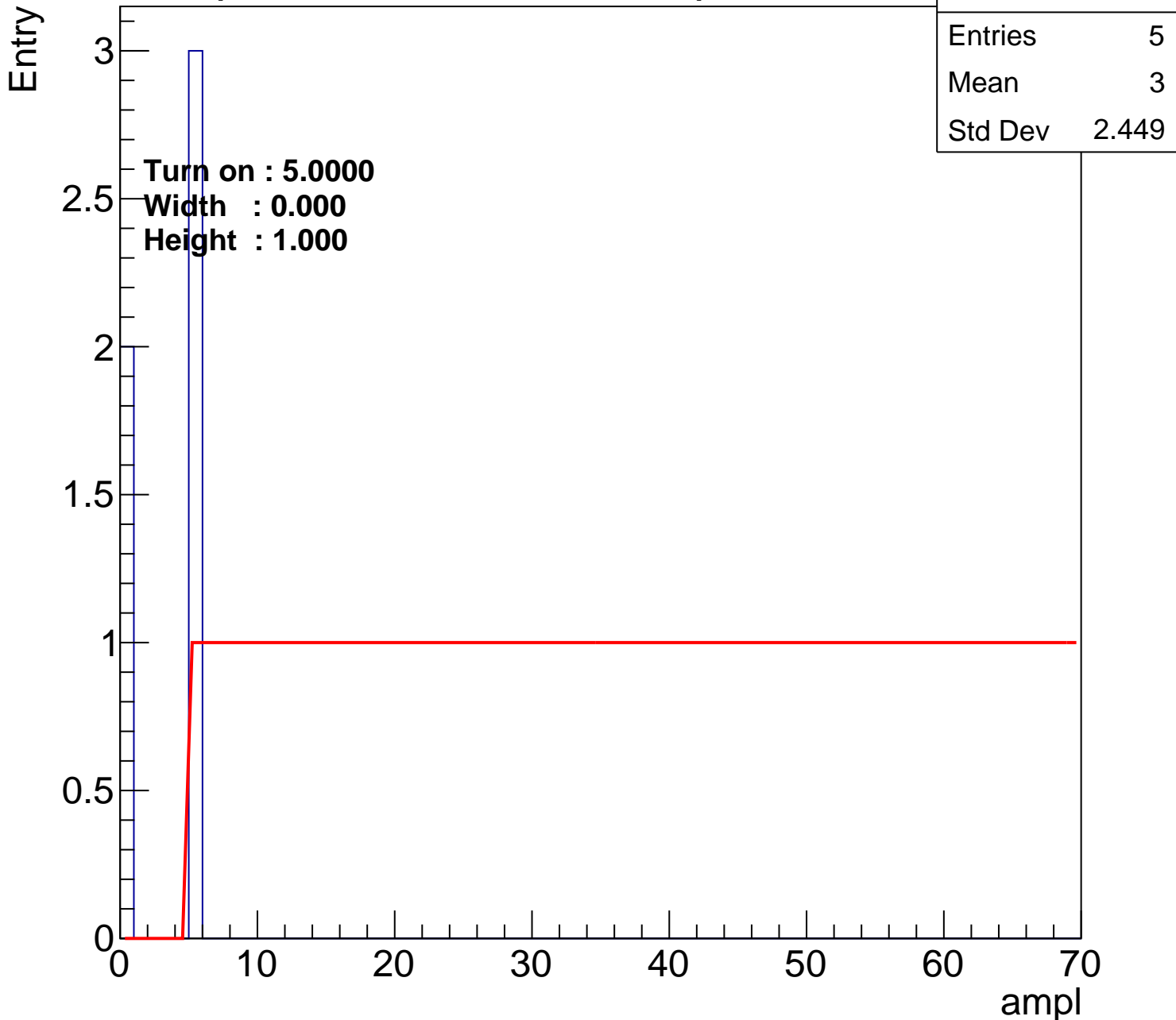
5

Mean

3

Std Dev

2.449



B0L101S, U2-ch63

calib_packv5_042523_0143.root, FC#1, port C1

Entry

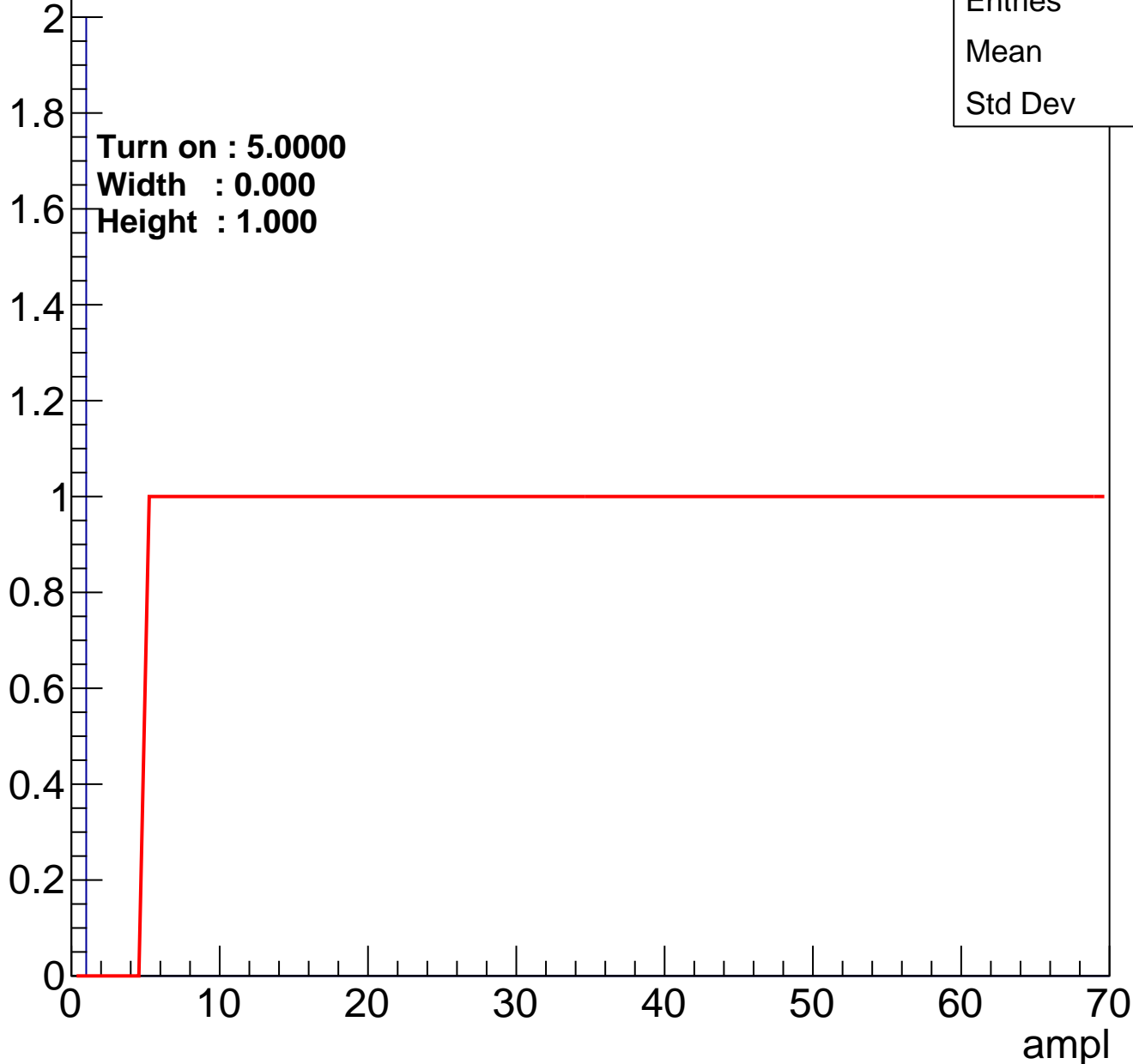


Entries	0
Mean	0
Std Dev	0

B0L101S, U2-ch64

calib_packv5_042523_0143.root, FC#1, port C1

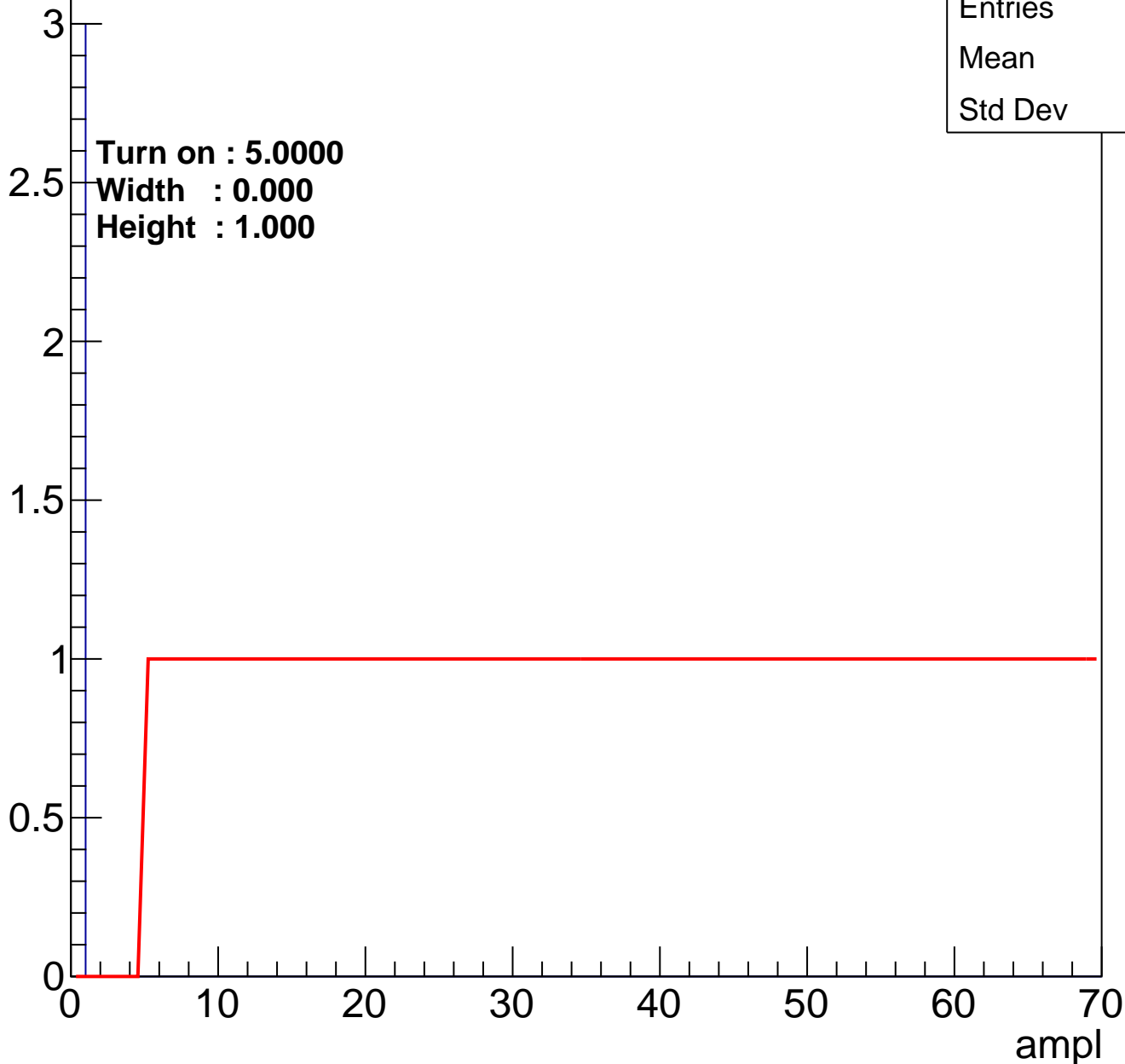
Entry



B0L101S, U2-ch65

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	3
Mean	0
Std Dev	0

B0L101S, U2-ch66

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	2
Mean	0
Std Dev	0

B0L101S, U2-ch67

calib_packv5_042523_0143.root, FC#1, port C1

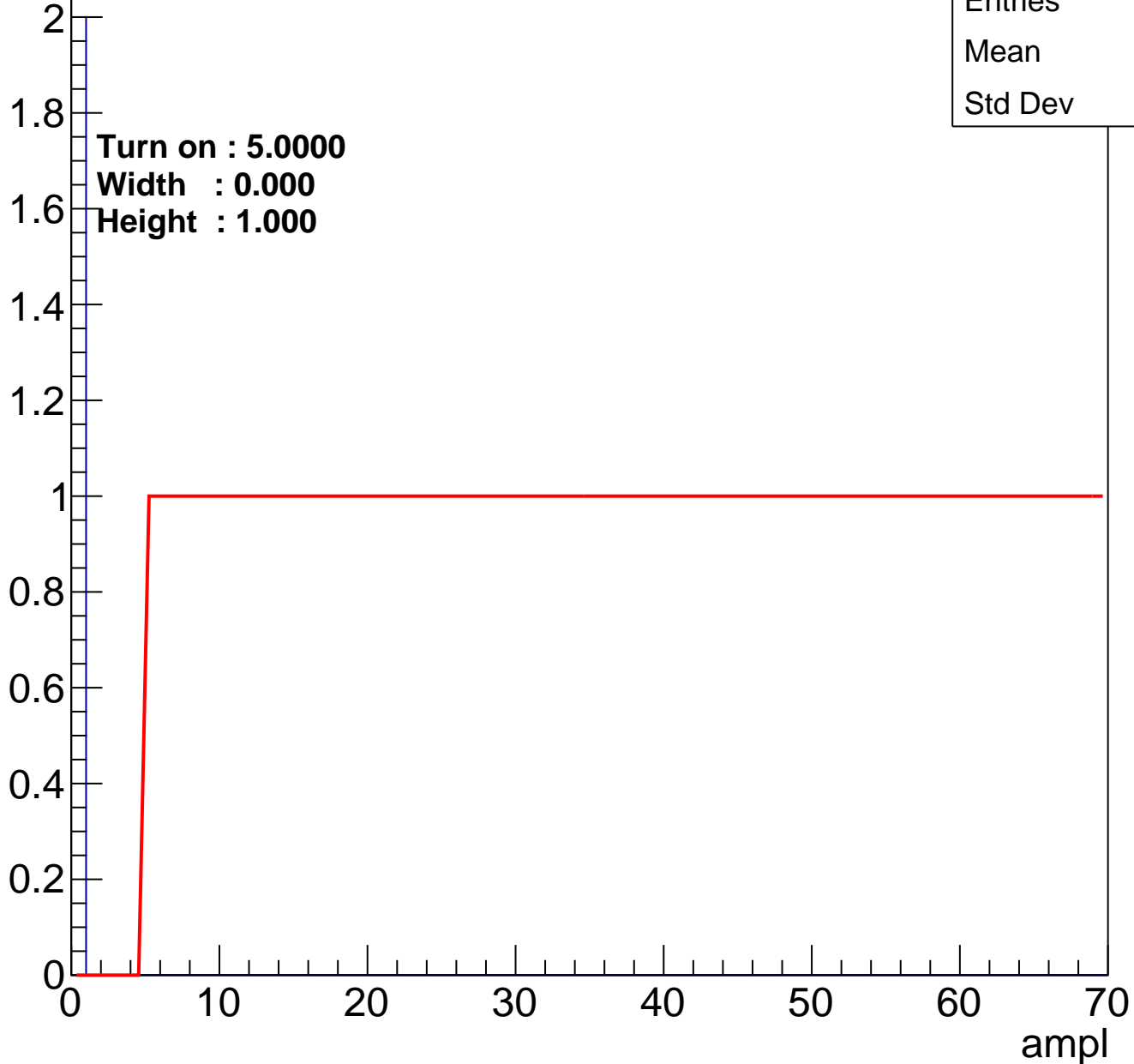
Entry



B0L101S, U2-ch68

calib_packv5_042523_0143.root, FC#1, port C1

Entry



B0L101S, U2-ch69

calib_packv5_042523_0143.root, FC#1, port C1

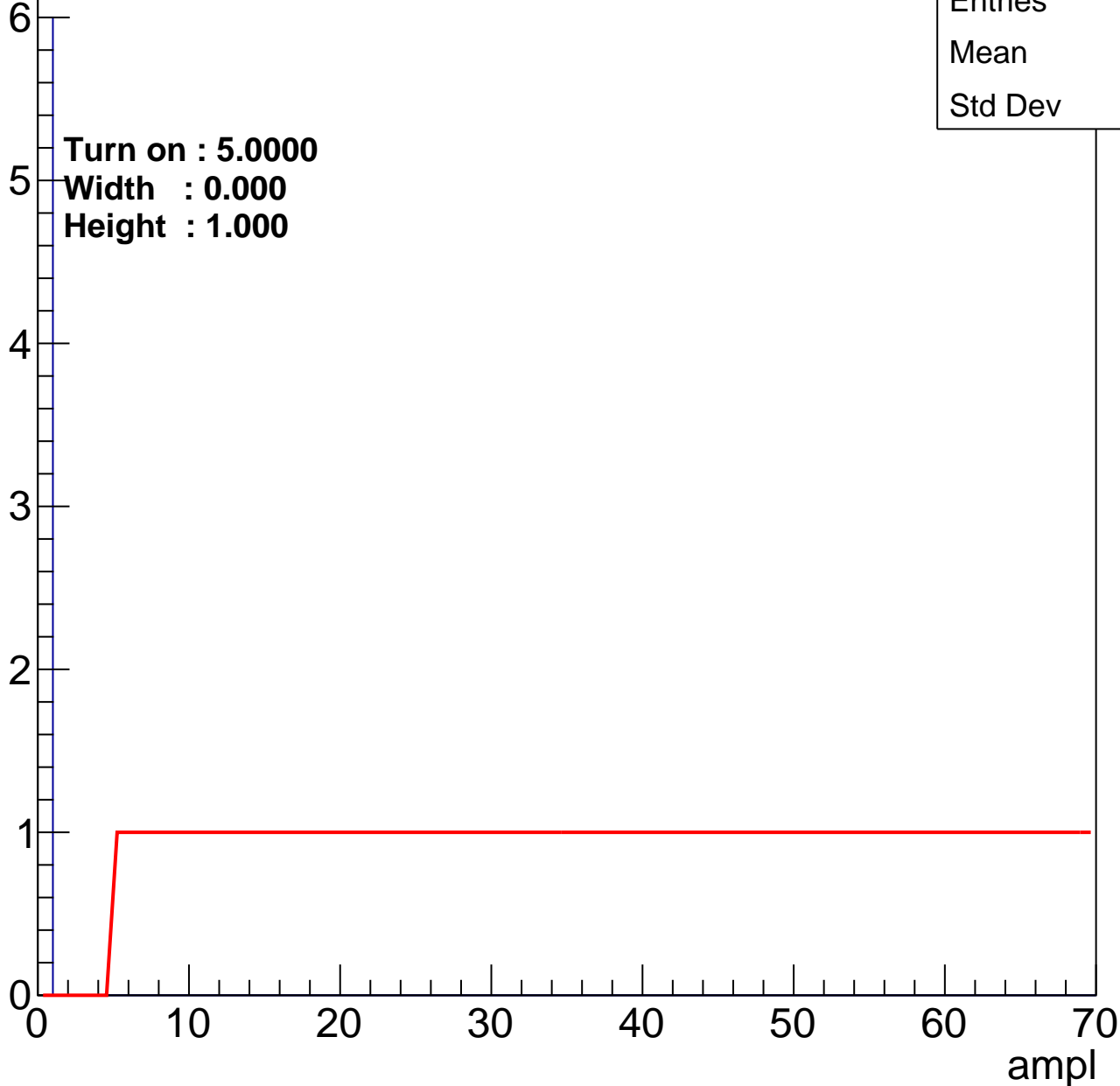
Entry

Entries	6
Mean	0
Std Dev	0

Turn on : 5.0000

Width : 0.000

Height : 1.000



B0L101S, U2-ch70

calib_packv5_042523_0143.root, FC#1, port C1

Entry

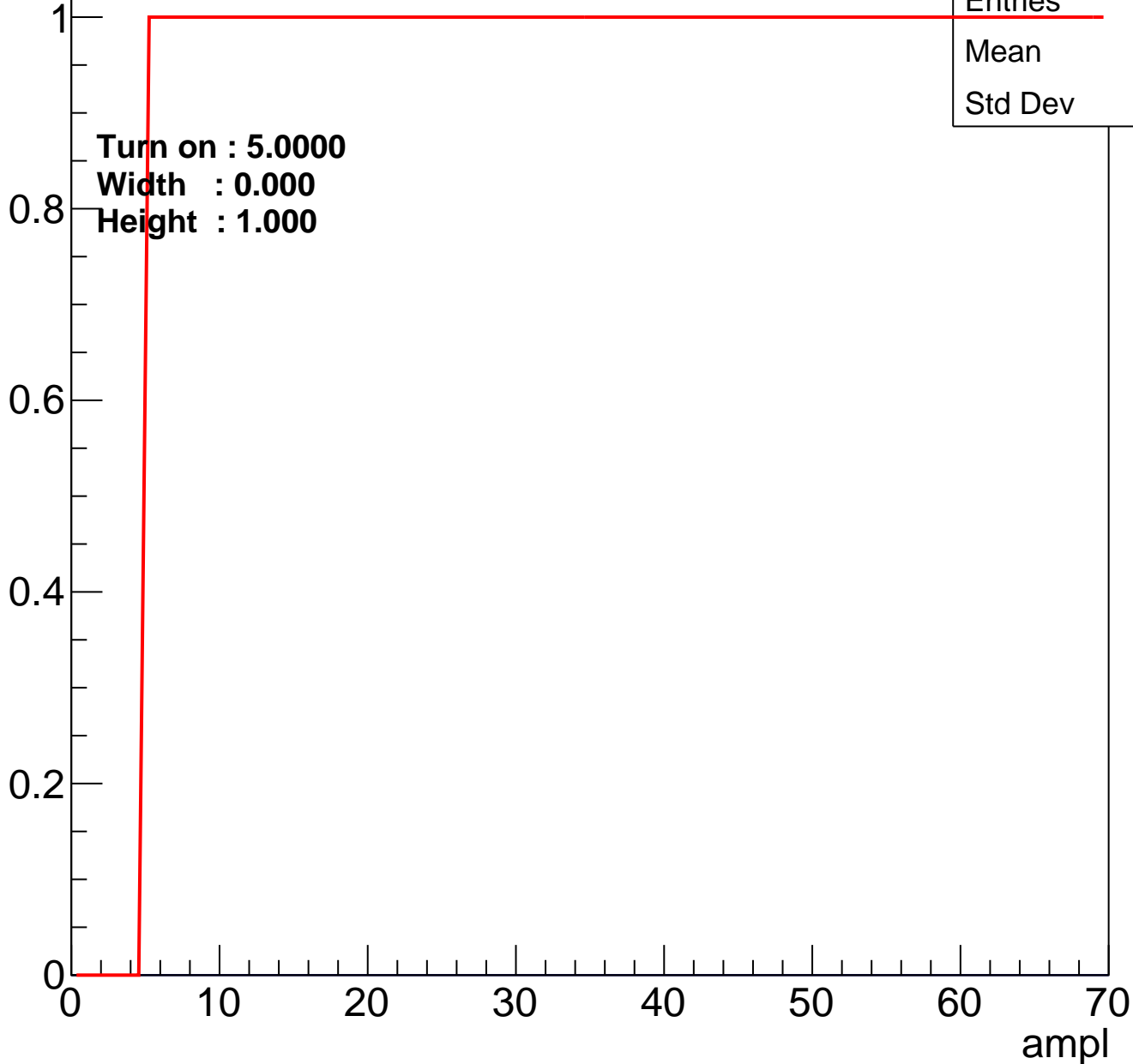


Entries	2
Mean	0
Std Dev	0

B0L101S, U2-ch71

calib_packv5_042523_0143.root, FC#1, port C1

Entry

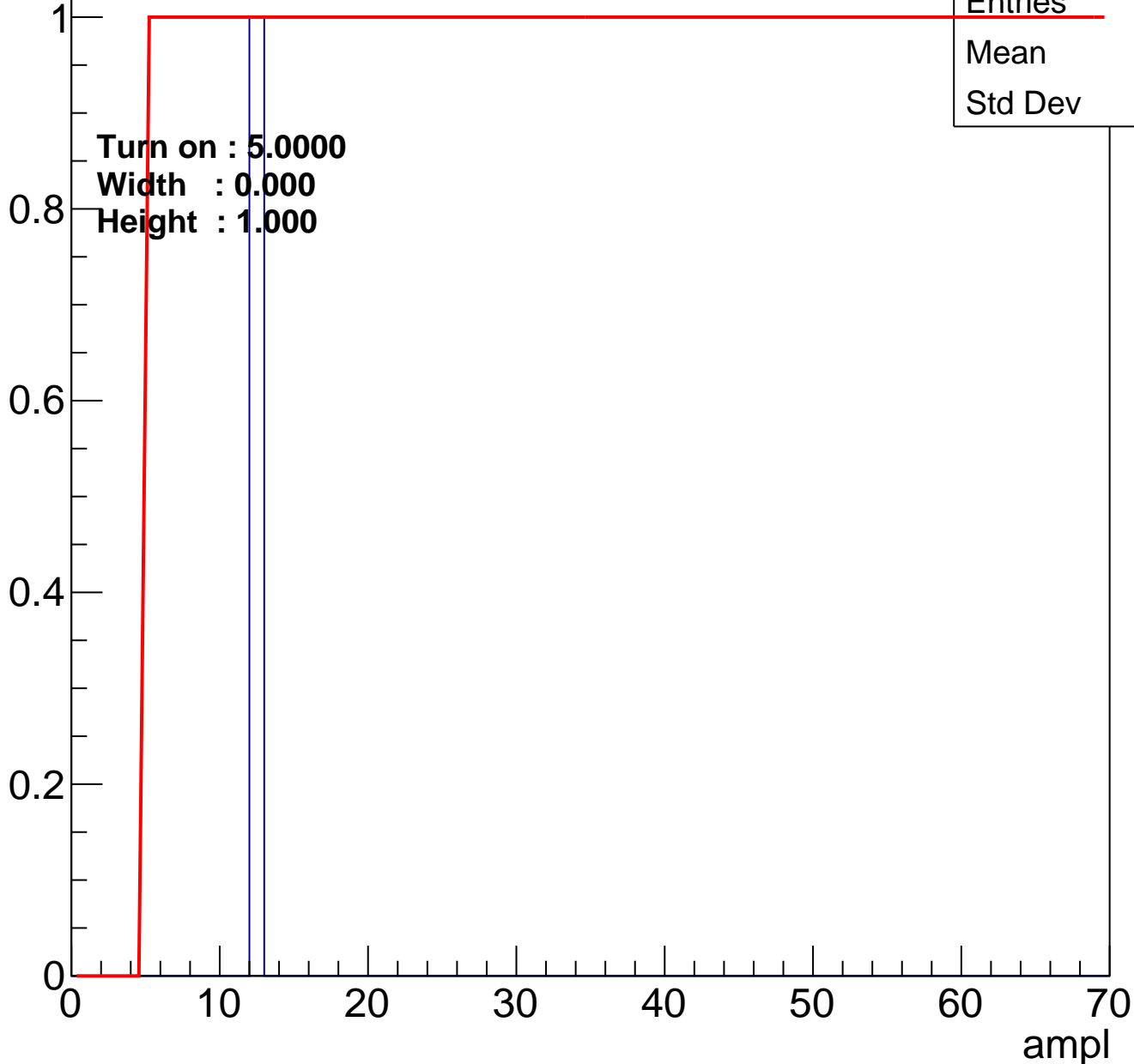


Entries	0
Mean	0
Std Dev	0

B0L101S, U2-ch72

calib_packv5_042523_0143.root, FC#1, port C1

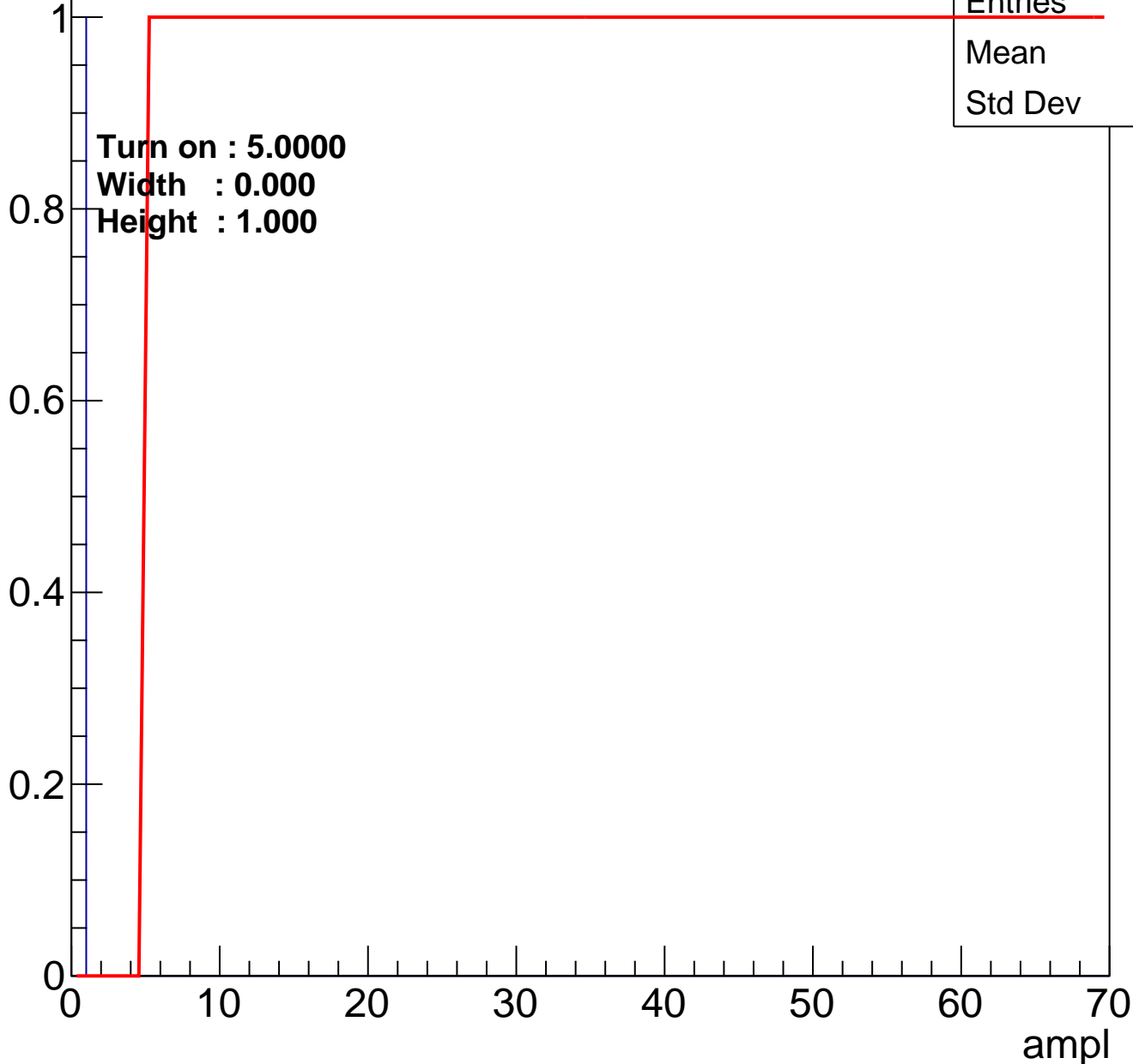
Entry



B0L101S, U2-ch73

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	1
Mean	0
Std Dev	0

B0L101S, U2-ch74

calib_packv5_042523_0143.root, FC#1, port C1

Entry



B0L101S, U2-ch75

calib_packv5_042523_0143.root, FC#1, port C1

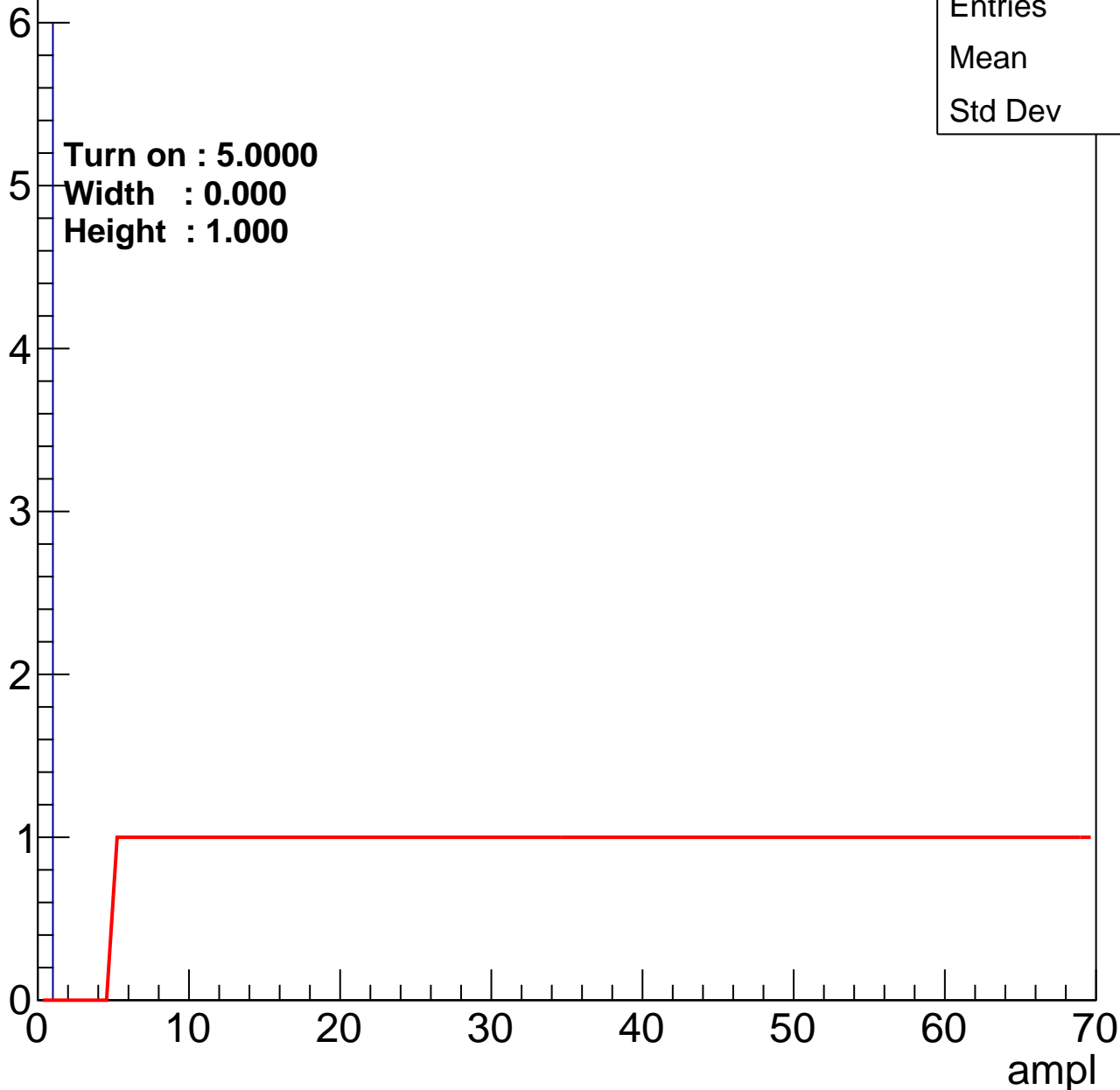
Entry

Entries	6
Mean	0
Std Dev	0

Turn on : 5.0000

Width : 0.000

Height : 1.000



B0L101S, U2-ch76

calib_packv5_042523_0143.root, FC#1, port C1

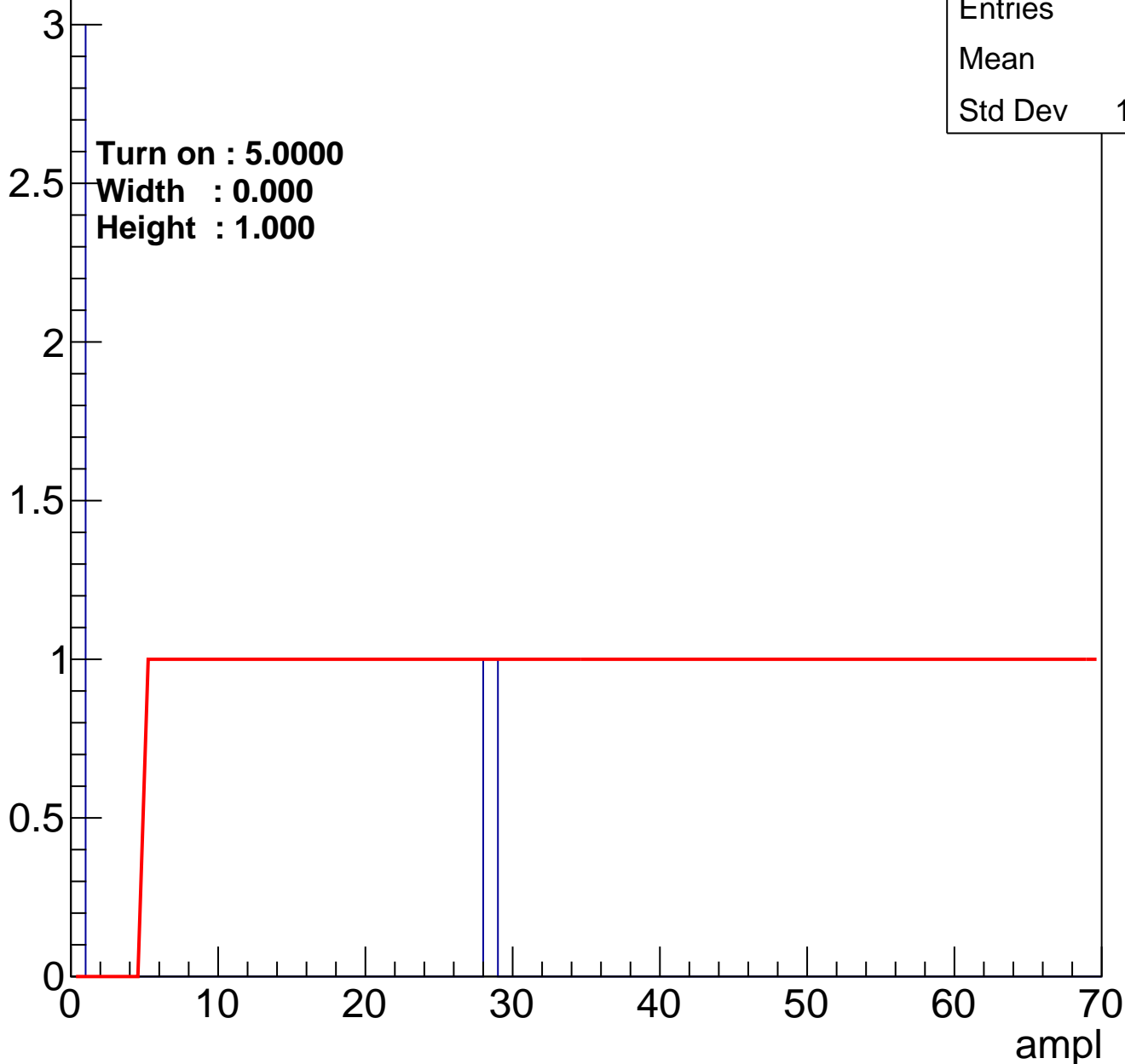
Entry



B0L101S, U2-ch77

calib_packv5_042523_0143.root, FC#1, port C1

Entry



B0L101S, U2-ch78

calib_packv5_042523_0143.root, FC#1, port C1

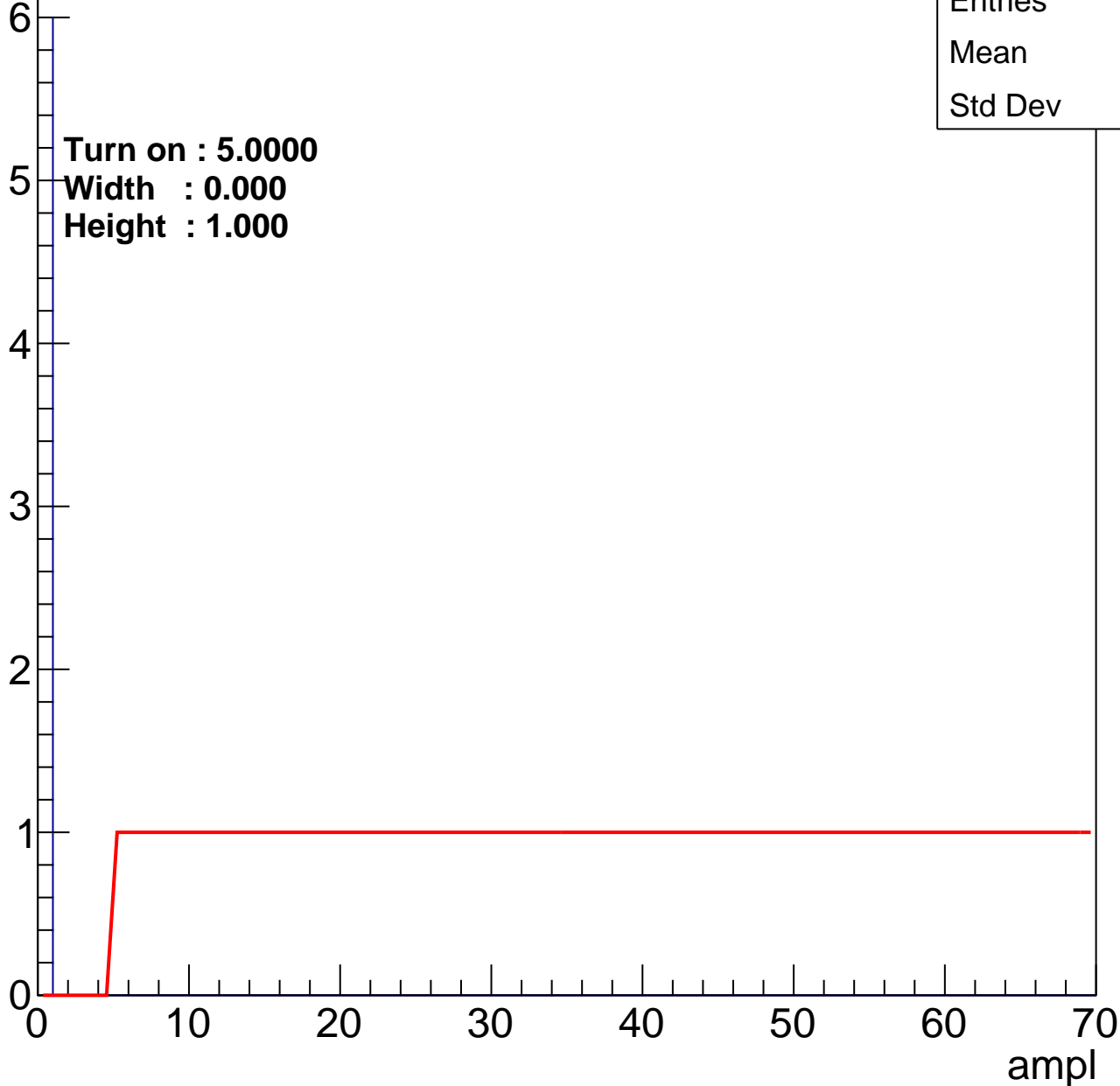
Entry

Entries	6
Mean	0
Std Dev	0

Turn on : 5.0000

Width : 0.000

Height : 1.000



B0L101S, U2-ch79

calib_packv5_042523_0143.root, FC#1, port C1

Entry

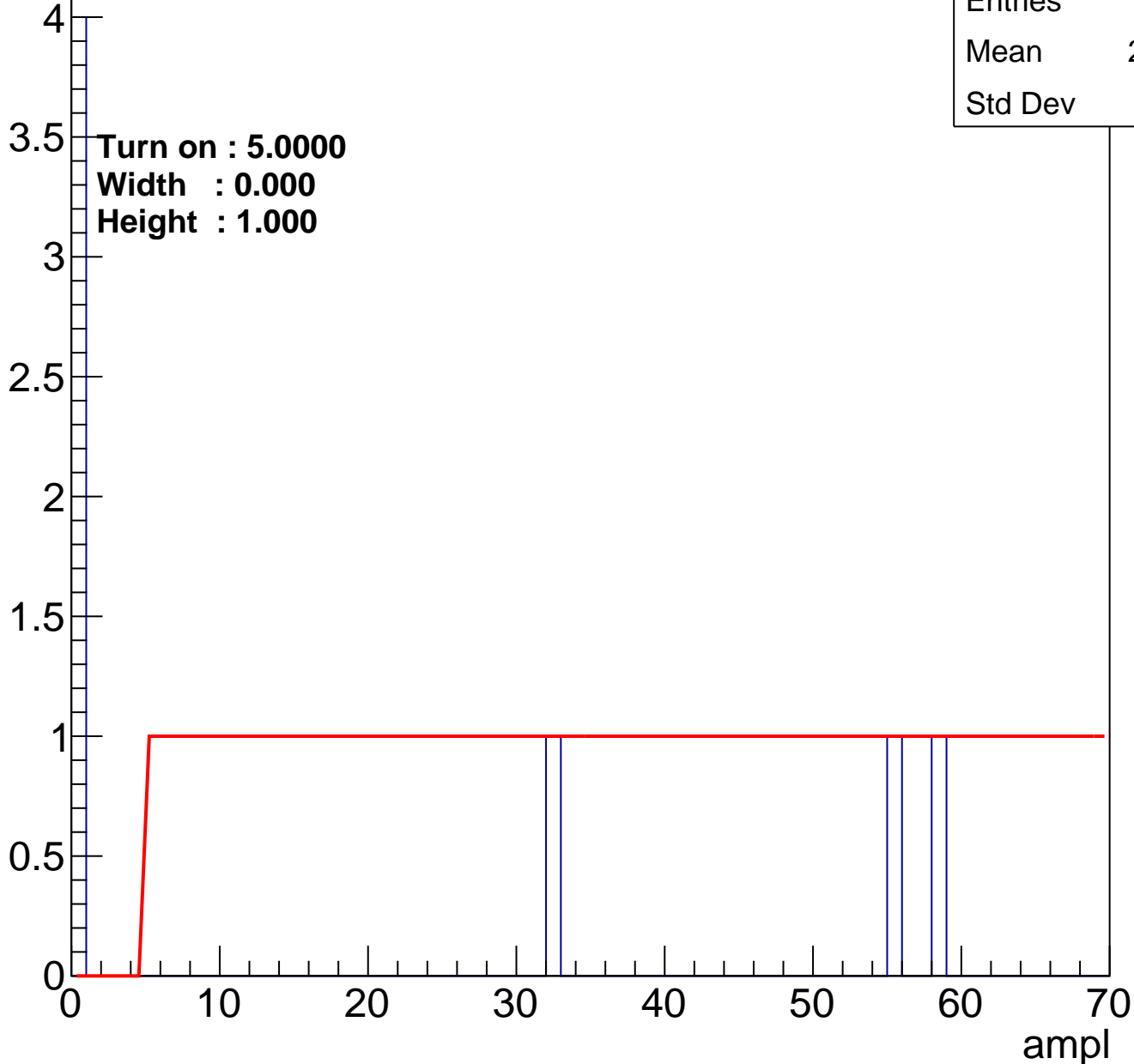


Entries	1
Mean	0
Std Dev	0

B0L101S, U2-ch80

calib_packv5_042523_0143.root, FC#1, port C1

Entry



B0L101S, U2-ch81

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	0
Mean	0
Std Dev	0

B0L101S, U2-ch82

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	2
Mean	0
Std Dev	0

B0L101S, U2-ch83

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	2
Mean	0
Std Dev	0

B0L101S, U2-ch84

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	0
Mean	0
Std Dev	0

B0L101S, U2-ch85

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	1
Mean	0
Std Dev	0

B0L101S, U2-ch86

calib_packv5_042523_0143.root, FC#1, port C1

Entry

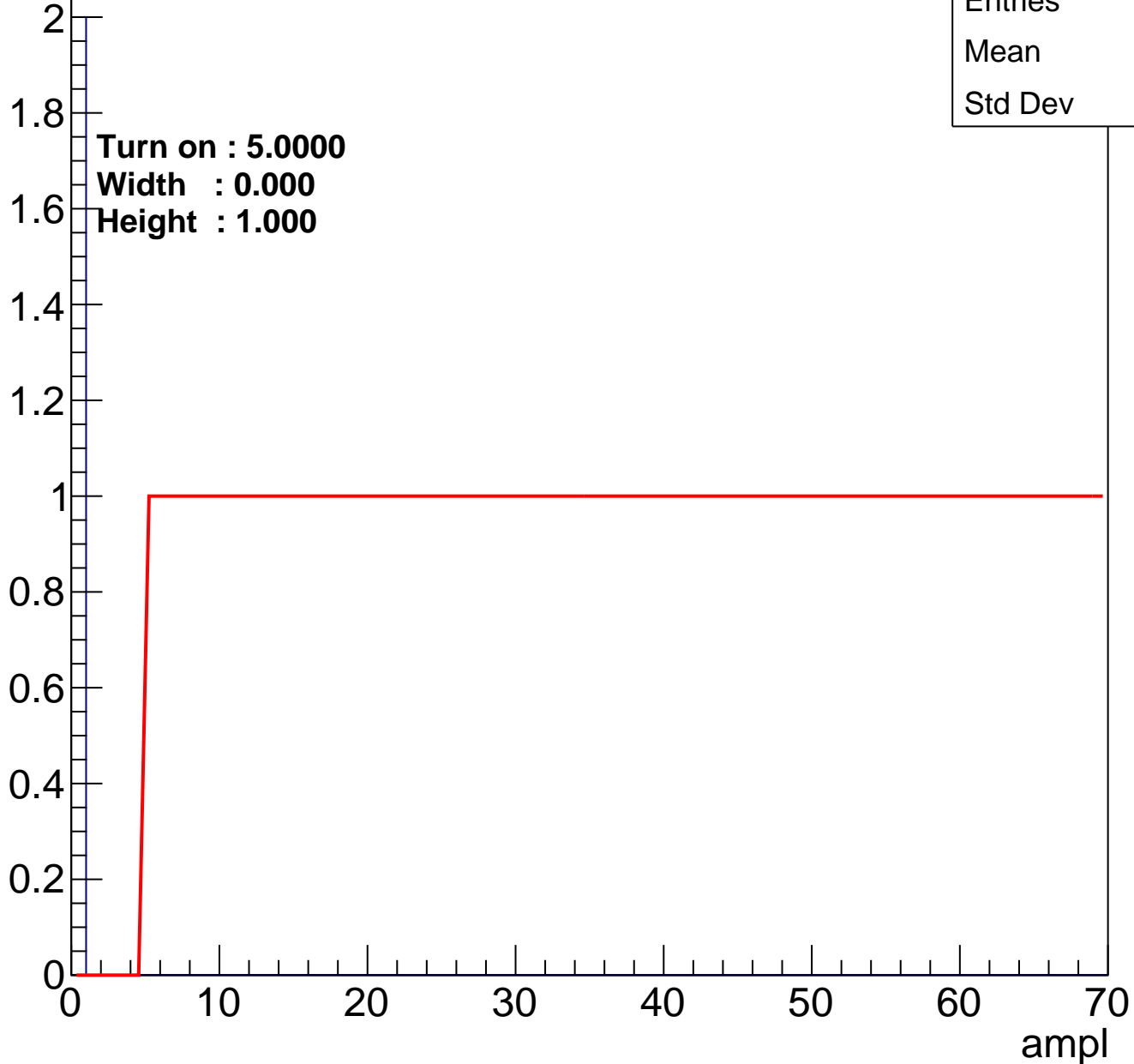


Entries	0
Mean	0
Std Dev	0

B0L101S, U2-ch87

calib_packv5_042523_0143.root, FC#1, port C1

Entry



B0L101S, U2-ch88

calib_packv5_042523_0143.root, FC#1, port C1

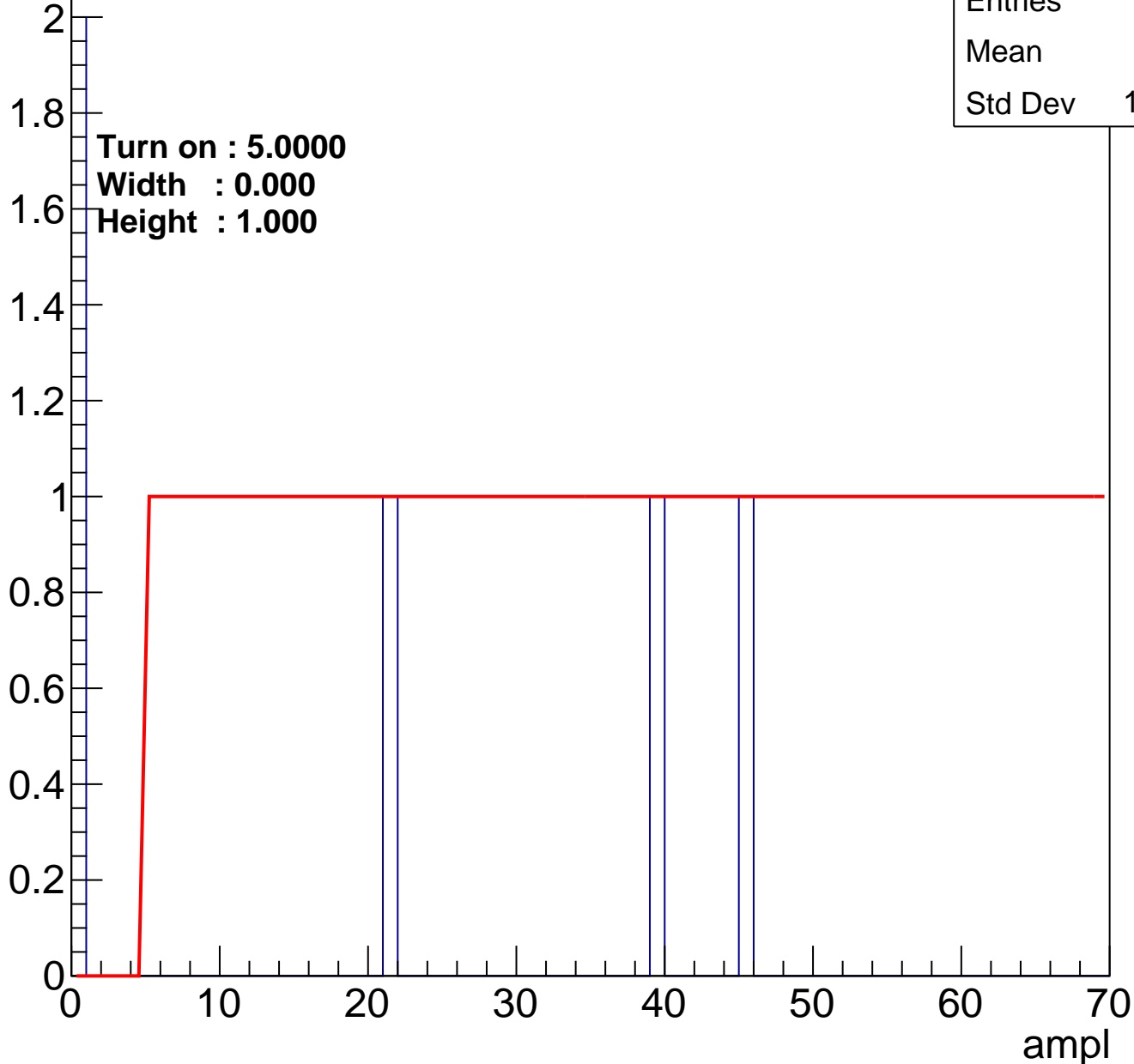
Entry

Entries	5
Mean	21
Std Dev	18.88

Turn on : 5.0000

Width : 0.000

Height : 1.000



B0L101S, U2-ch89

calib_packv5_042523_0143.root, FC#1, port C1

Entry

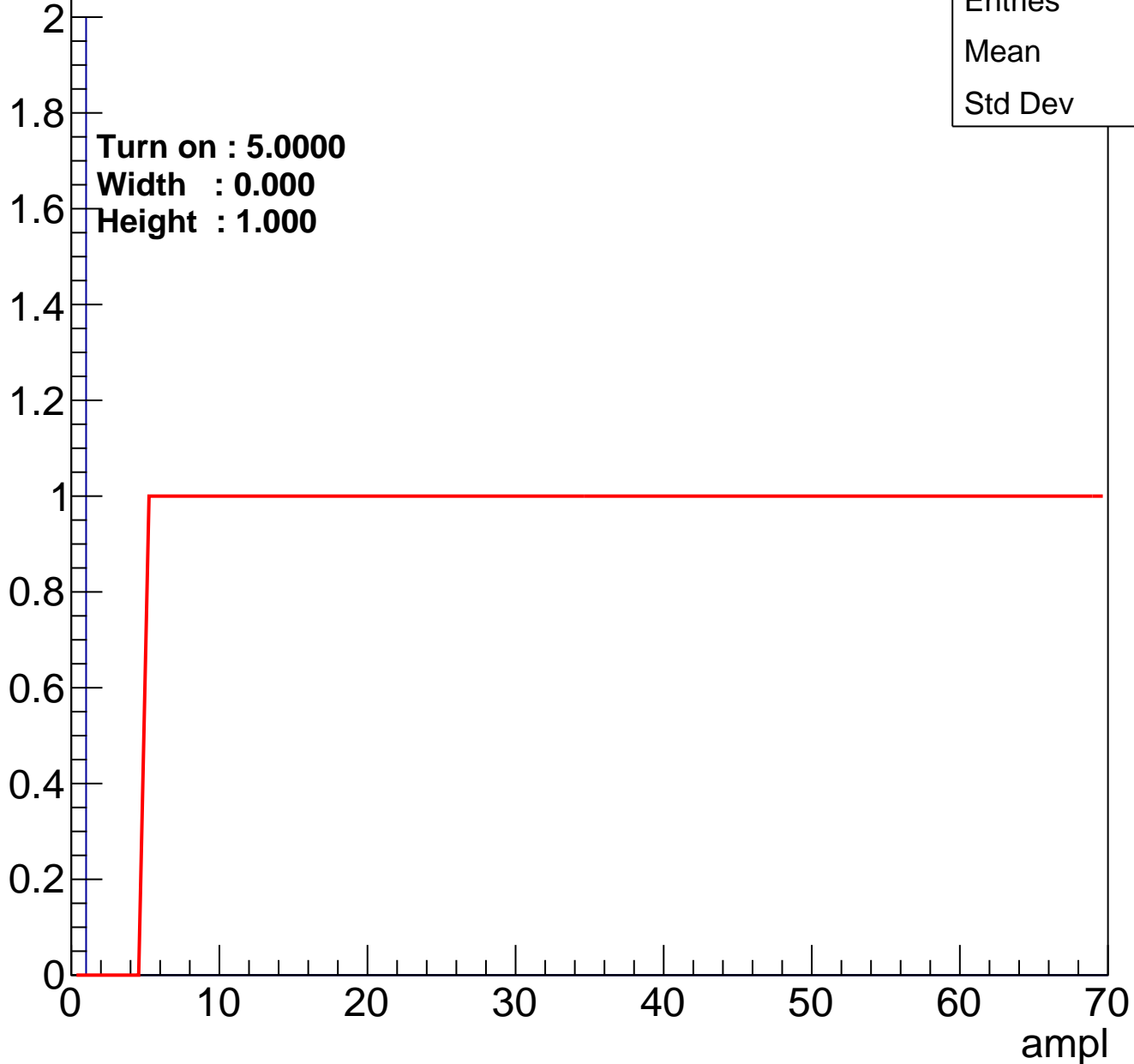


Entries	0
Mean	0
Std Dev	0

B0L101S, U2-ch90

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	2
Mean	0
Std Dev	0

B0L101S, U2-ch91

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	2
Mean	0
Std Dev	0

B0L101S, U2-ch92

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	1
Mean	0
Std Dev	0

B0L101S, U2-ch93

calib_packv5_042523_0143.root, FC#1, port C1

Entry

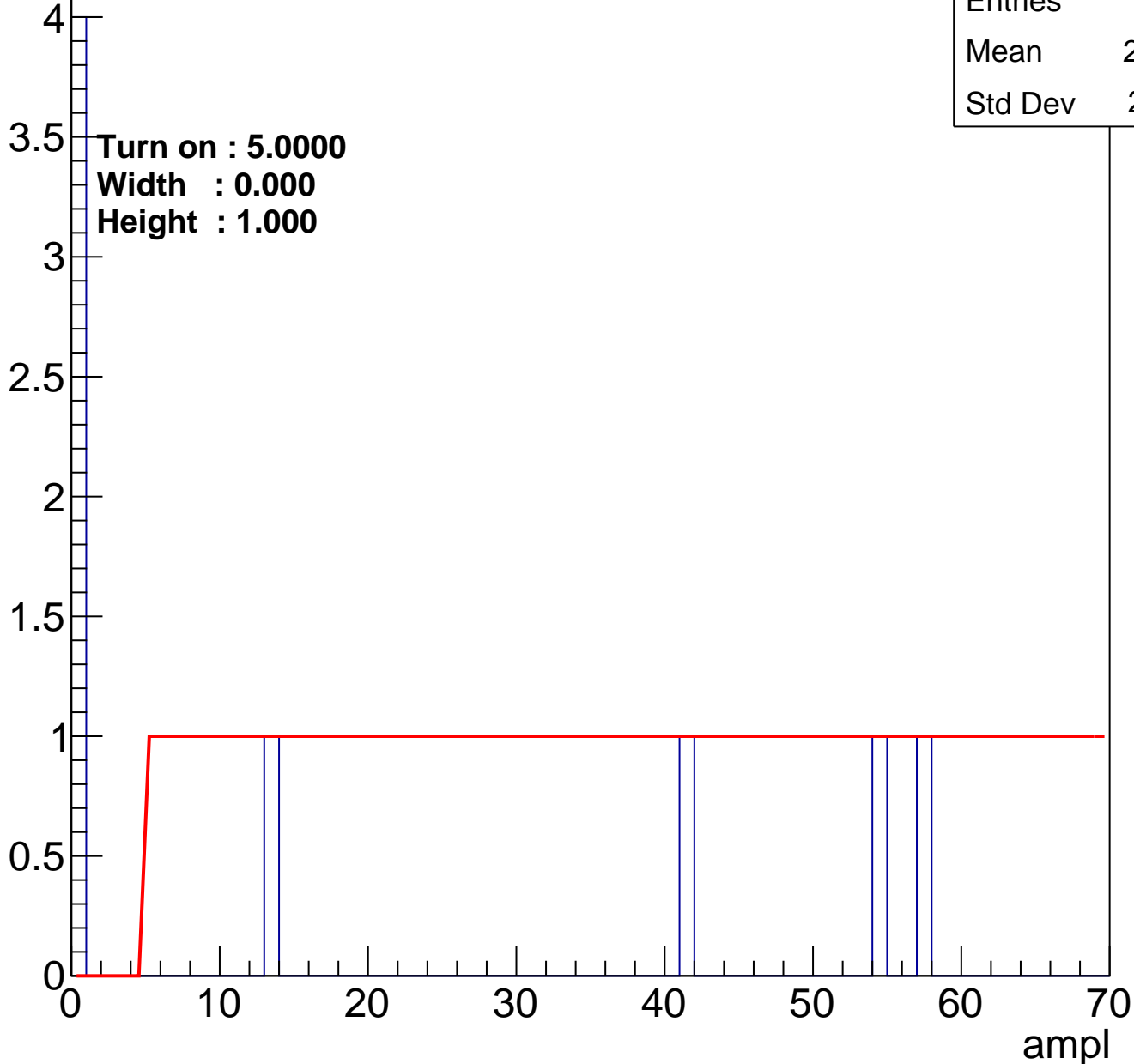


Entries	2
Mean	0
Std Dev	0

B0L101S, U2-ch94

calib_packv5_042523_0143.root, FC#1, port C1

Entry



B0L101S, U2-ch95

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	2
Mean	0
Std Dev	0

B0L101S, U2-ch96

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	2
Mean	0
Std Dev	0

B0L101S, U2-ch97

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	0
Mean	0
Std Dev	0

B0L101S, U2-ch98

calib_packv5_042523_0143.root, FC#1, port C1

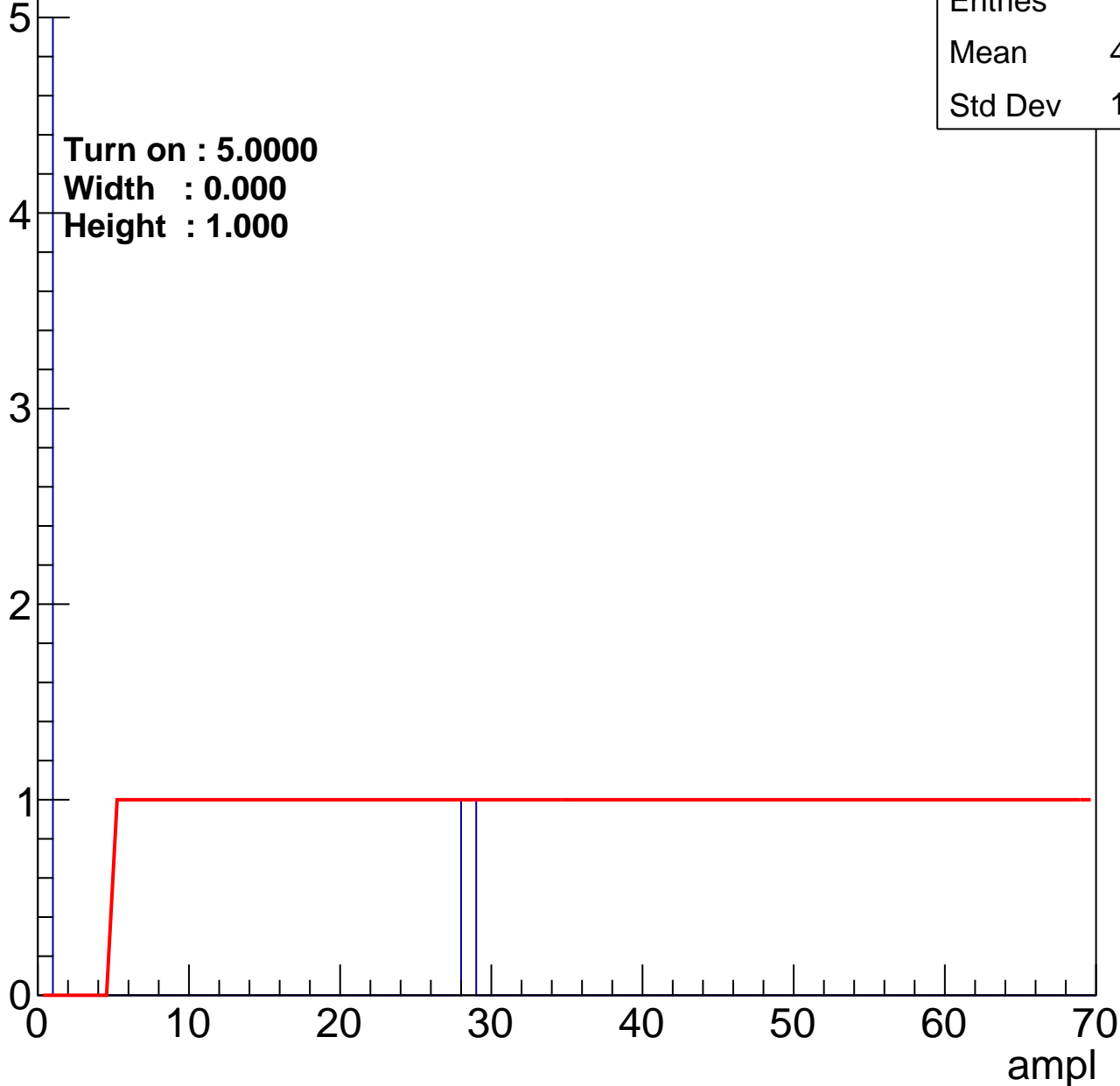
Entry

Entries	6
Mean	4.667
Std Dev	10.43

Turn on : 5.0000

Width : 0.000

Height : 1.000



B0L101S, U2-ch99

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	0
Mean	0
Std Dev	0

B0L101S, U2-ch100

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	2
Mean	0
Std Dev	0

B0L101S, U2-ch101

calib_packv5_042523_0143.root, FC#1, port C1

Entry

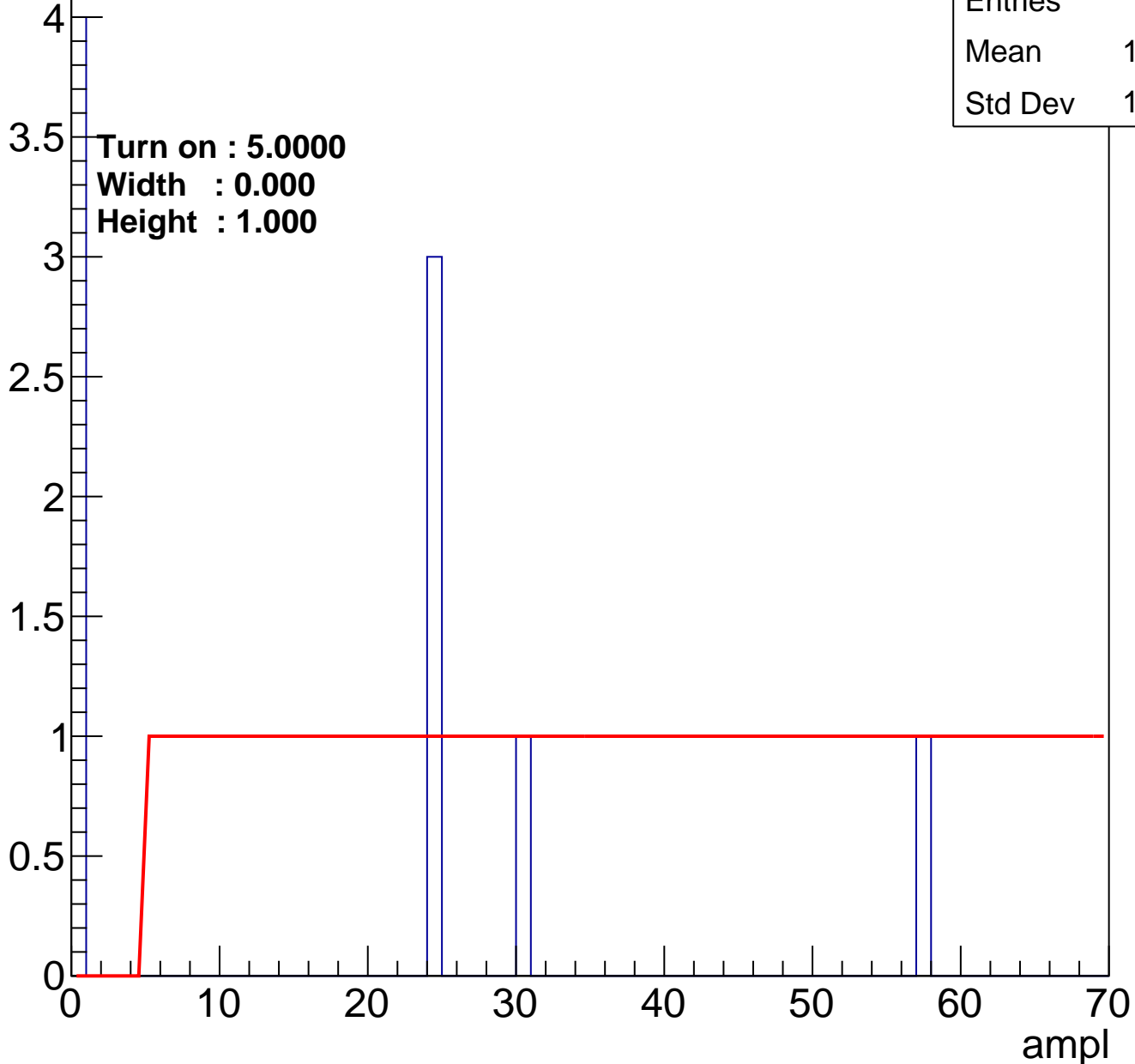


Entries	0
Mean	0
Std Dev	0

B0L101S, U2-ch102

calib_packv5_042523_0143.root, FC#1, port C1

Entry

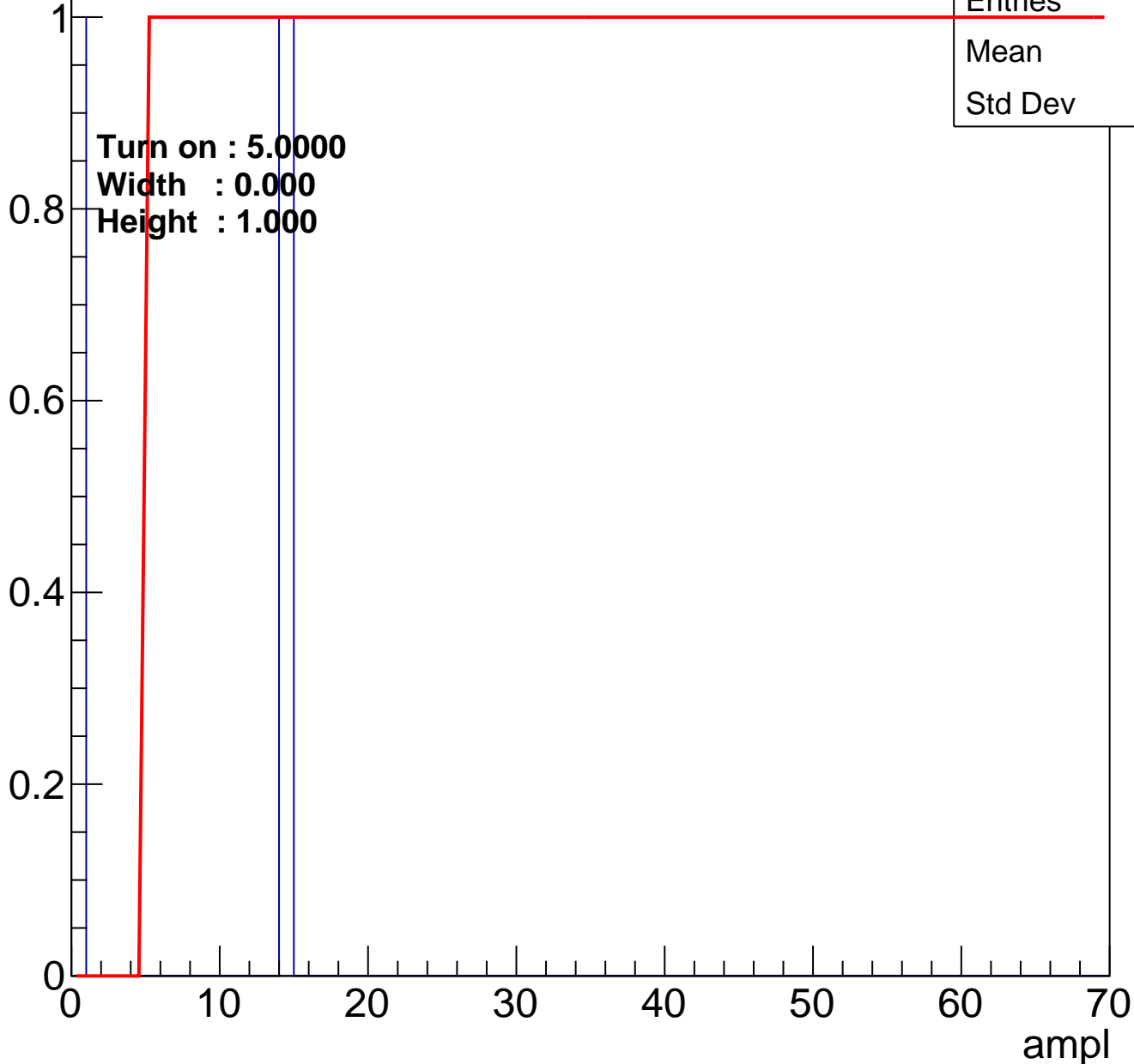


Entries	9
Mean	17.67
Std Dev	18.46

B0L101S, U2-ch103

calib_packv5_042523_0143.root, FC#1, port C1

Entry

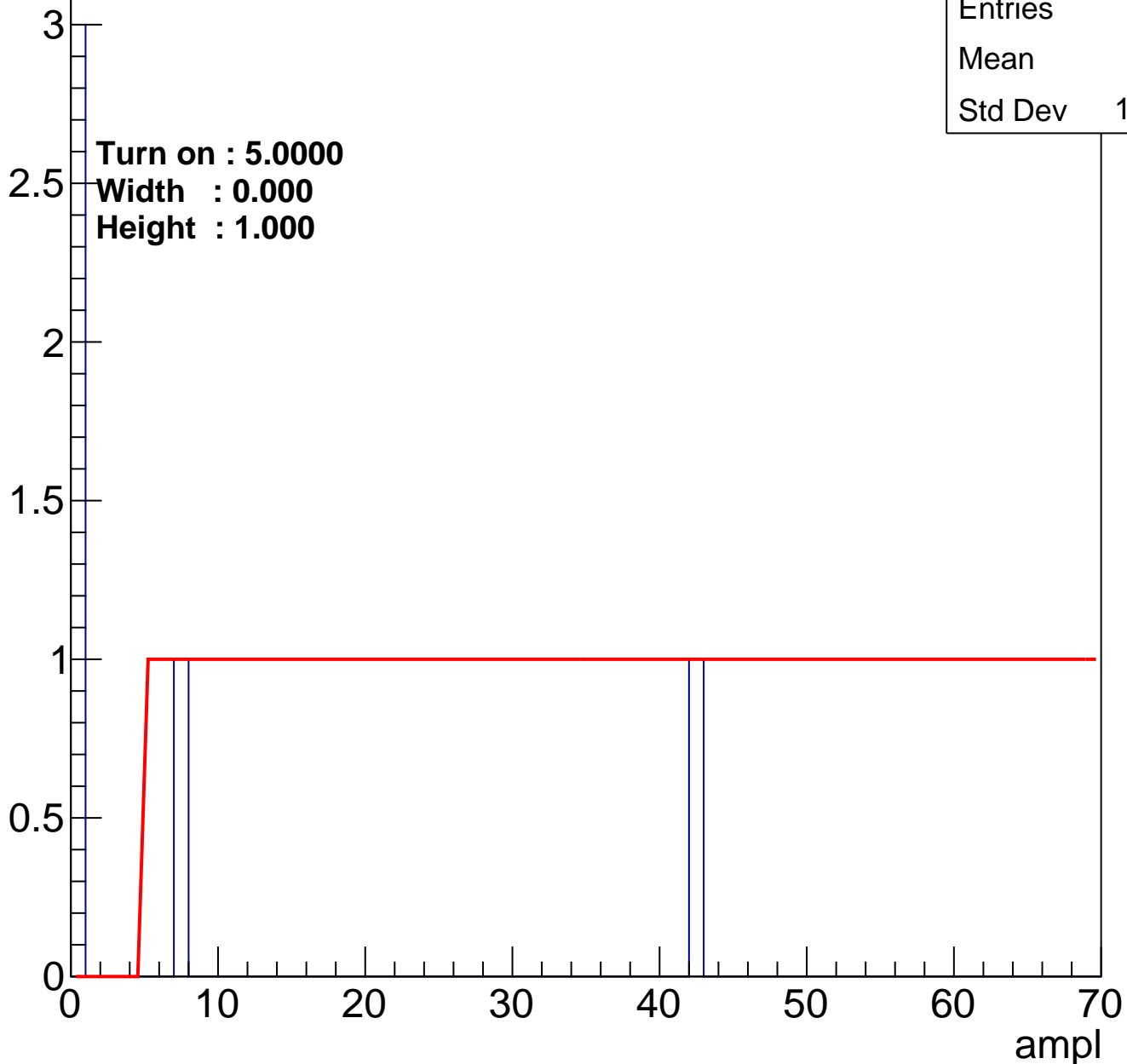


Entries	2
Mean	7
Std Dev	7

B0L101S, U2-ch104

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	5
Mean	9.8
Std Dev	16.33

B0L101S, U2-ch105

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	3
Mean	0
Std Dev	0

B0L101S, U2-ch106

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	2
Mean	0
Std Dev	0

B0L101S, U2-ch107

calib_packv5_042523_0143.root, FC#1, port C1

Entry

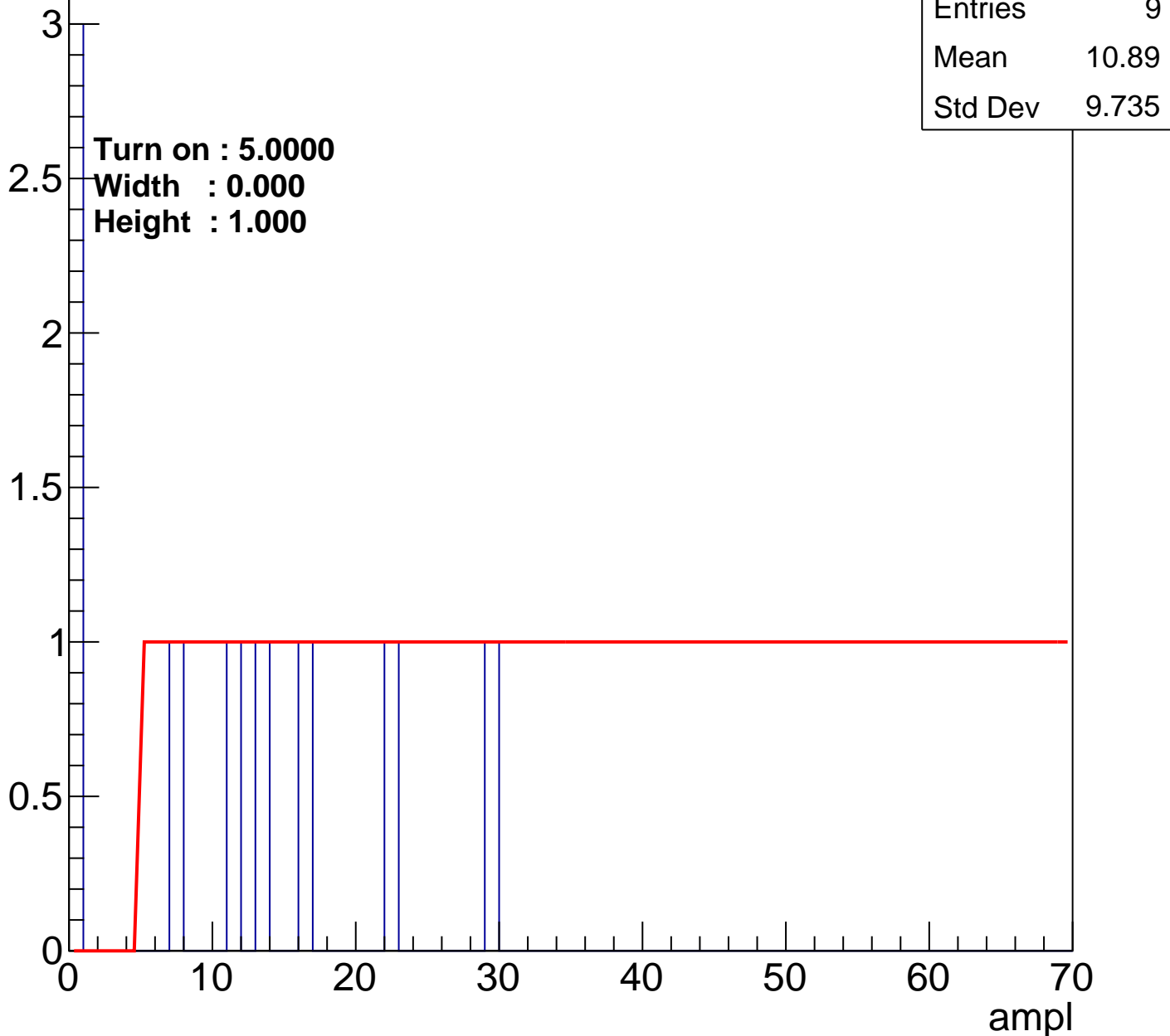


Entries	1
Mean	0
Std Dev	0

B0L101S, U2-ch108

calib_packv5_042523_0143.root, FC#1, port C1

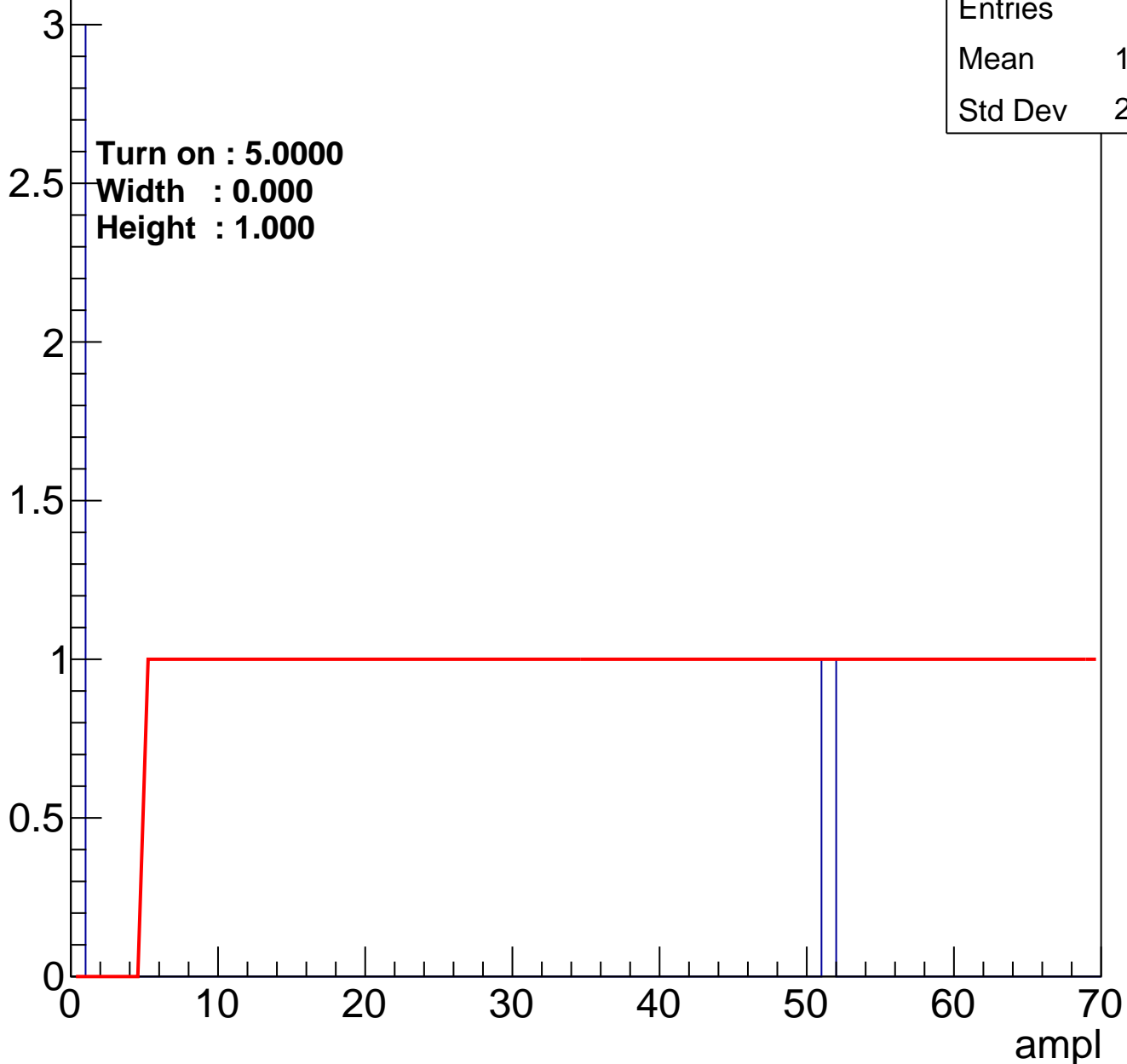
Entry



B0L101S, U2-ch109

calib_packv5_042523_0143.root, FC#1, port C1

Entry

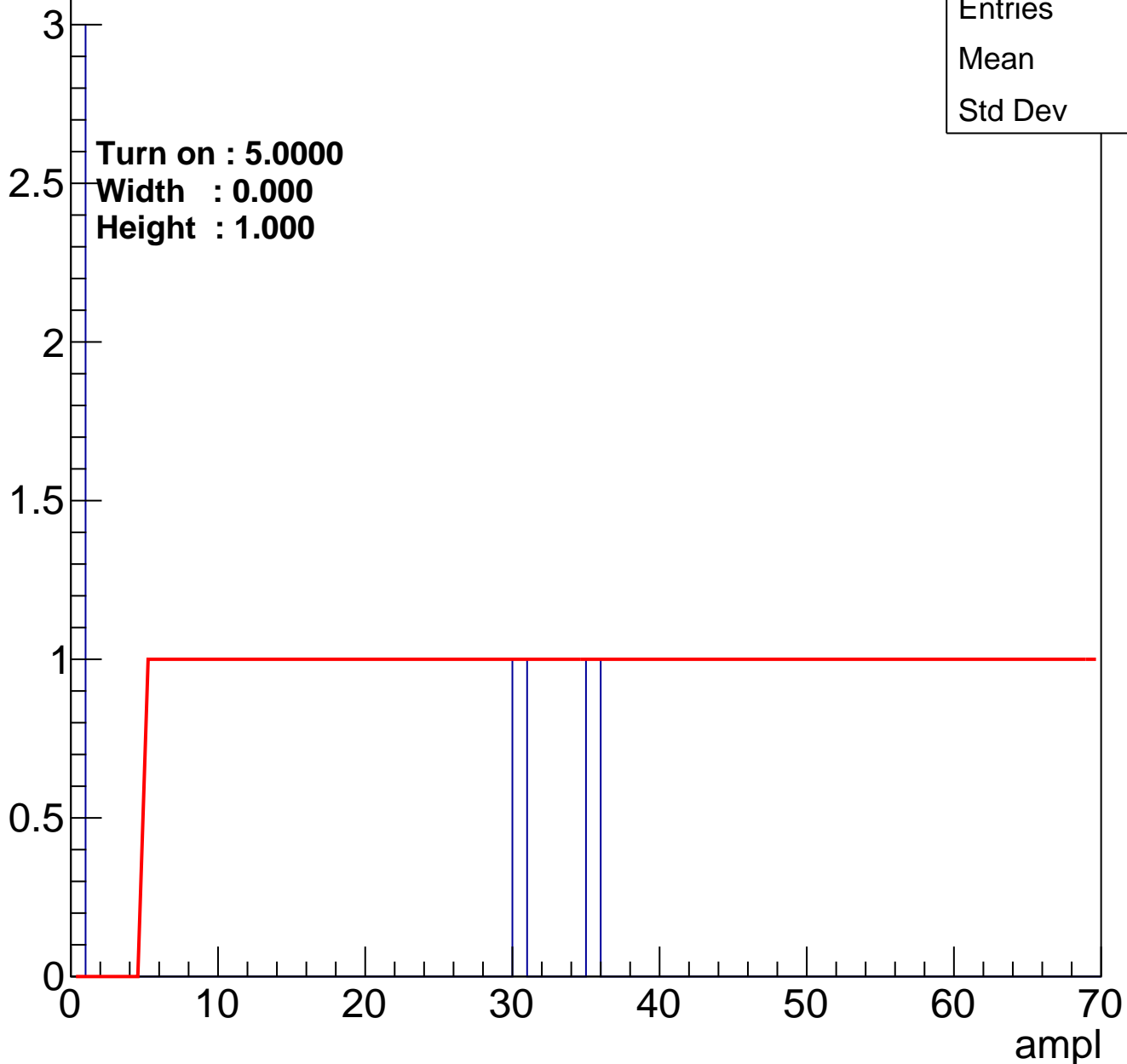


Entries	4
Mean	12.75
Std Dev	22.08

B0L101S, U2-ch110

calib_packv5_042523_0143.root, FC#1, port C1

Entry



B0L101S, U2-ch111

calib_packv5_042523_0143.root, FC#1, port C1

Entry

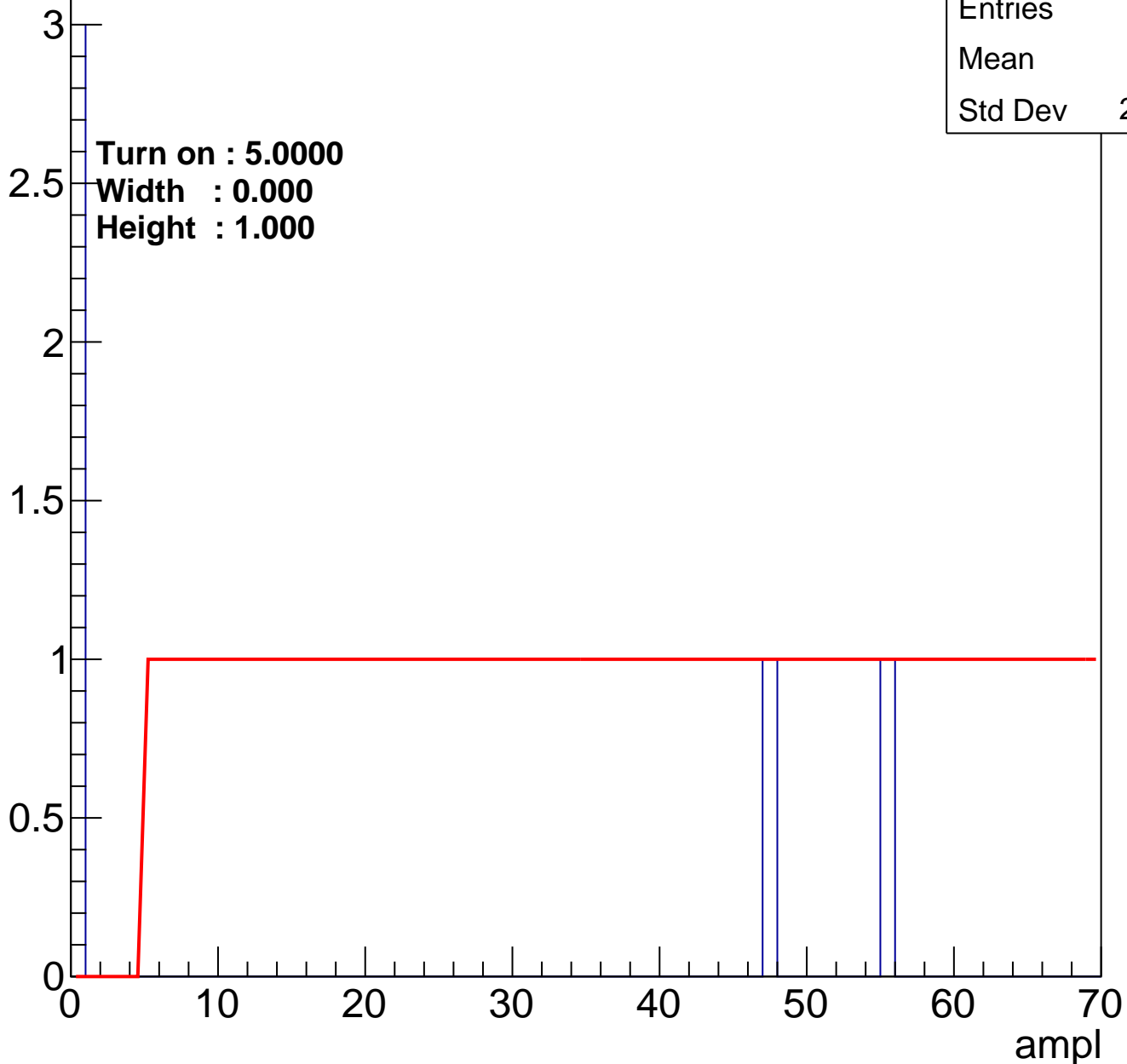


Entries	2
Mean	0
Std Dev	0

B0L101S, U2-ch112

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	5
Mean	20.4
Std Dev	25.11

B0L101S, U2-ch113

calib_packv5_042523_0143.root, FC#1, port C1

Entry

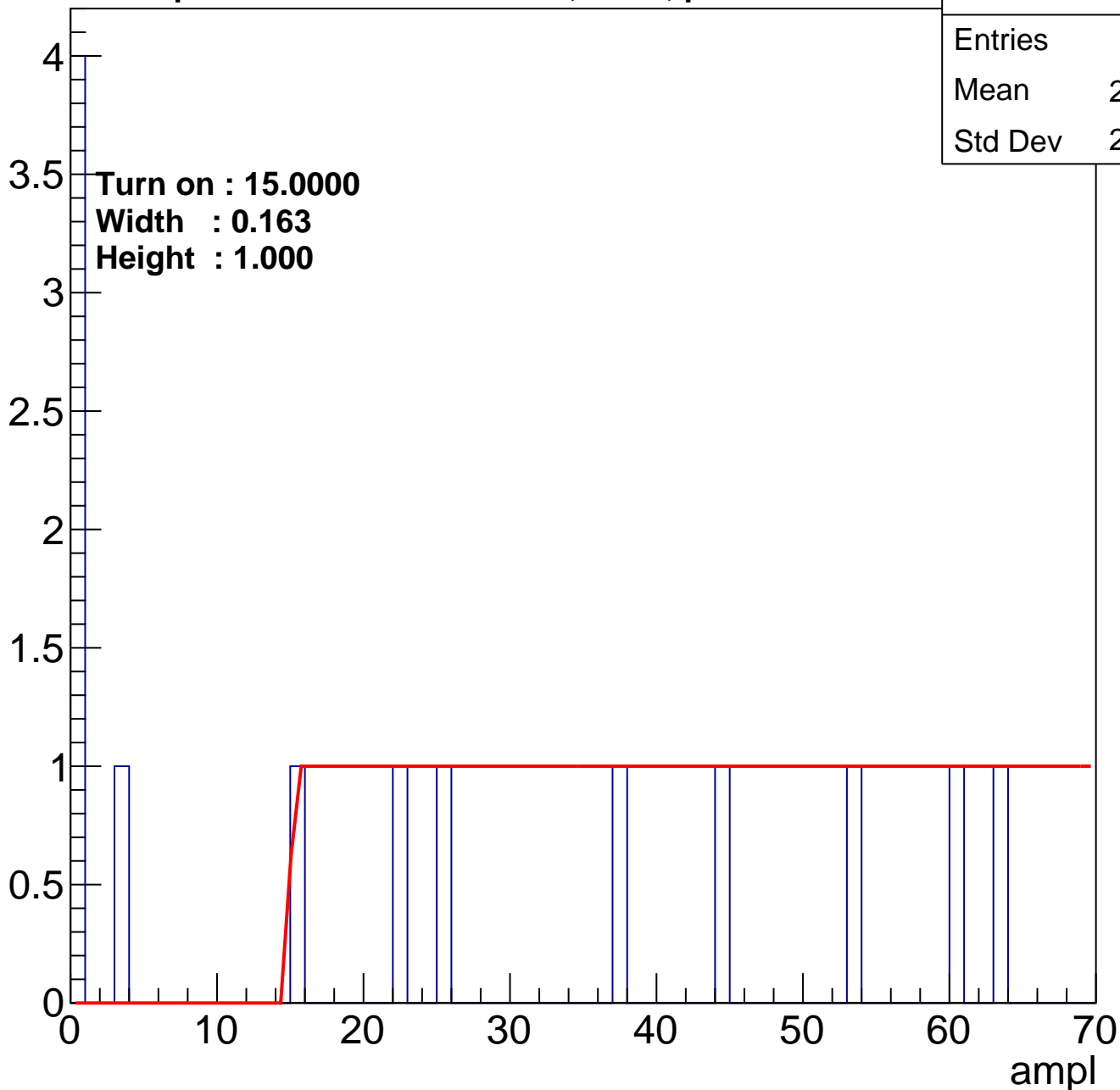


Entries	2
Mean	0
Std Dev	0

B0L101S, U2-ch114

calib_packv5_042523_0143.root, FC#1, port C1

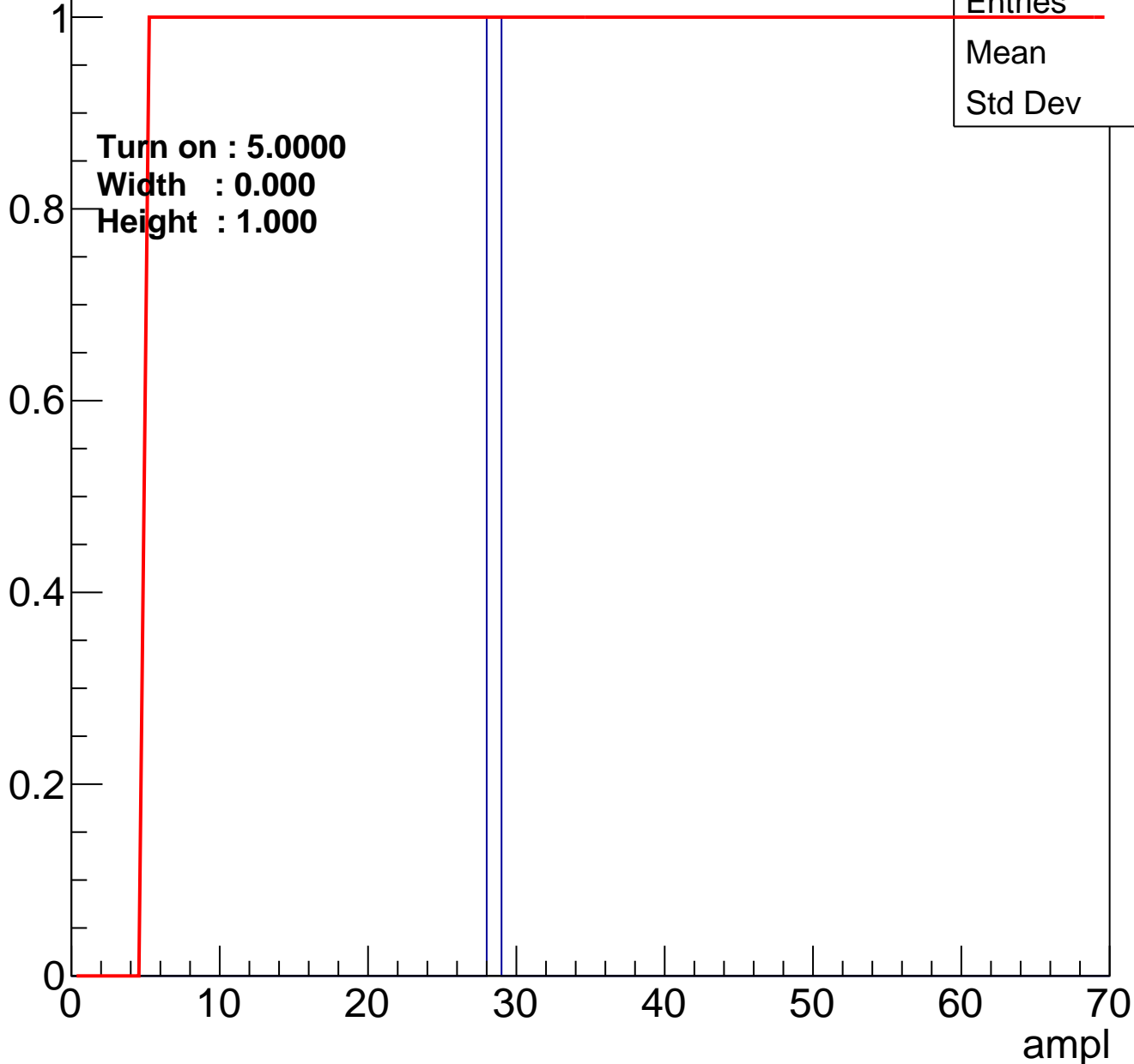
Entry



B0L101S, U2-ch115

calib_packv5_042523_0143.root, FC#1, port C1

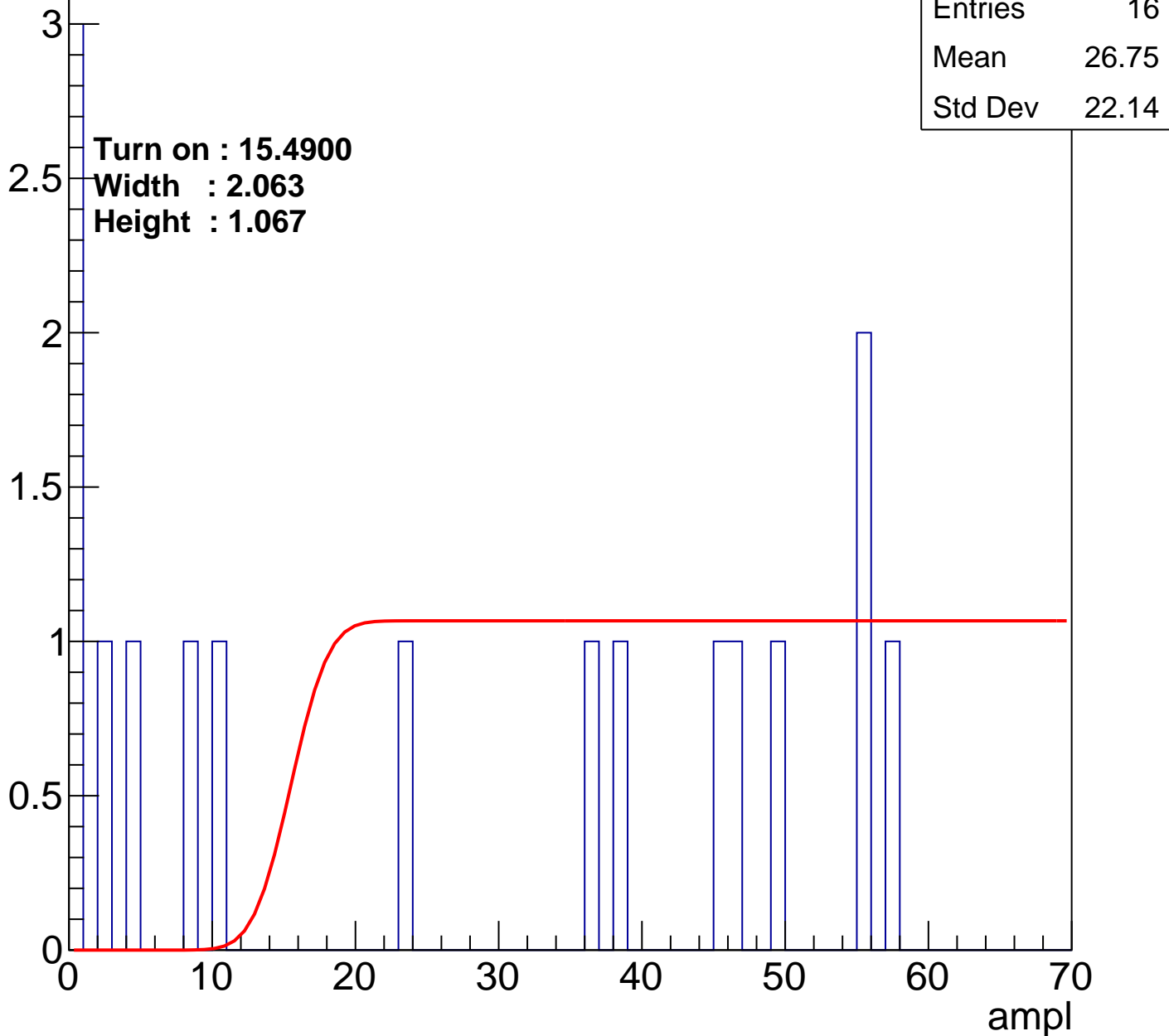
Entry



B0L101S, U2-ch116

calib_packv5_042523_0143.root, FC#1, port C1

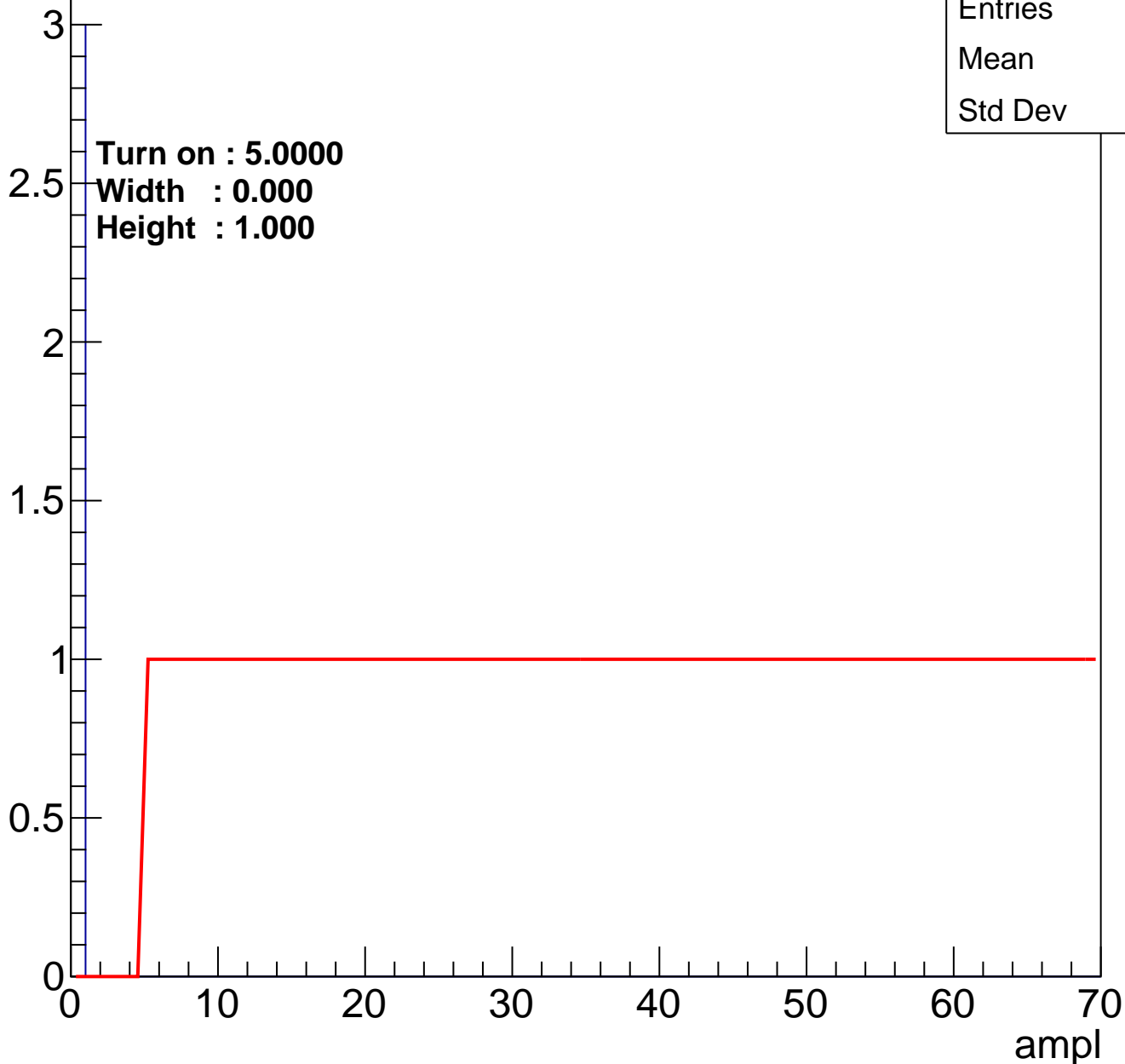
Entry



B0L101S, U2-ch117

calib_packv5_042523_0143.root, FC#1, port C1

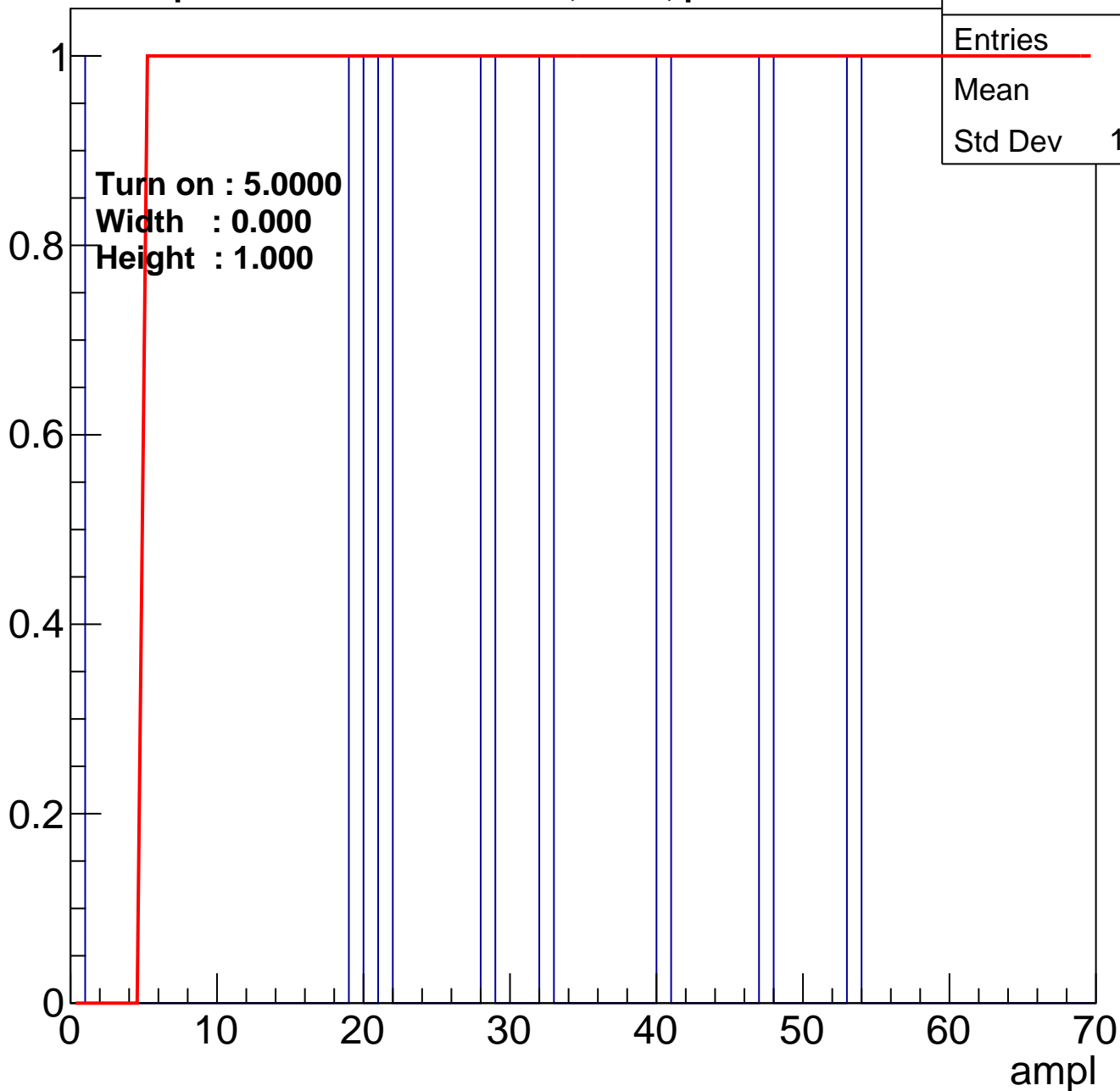
Entry



B0L101S, U2-ch118

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Entries	8
Mean	30
Std Dev	15.92

B0L101S, U2-ch119

calib_packv5_042523_0143.root, FC#1, port C1

Entry

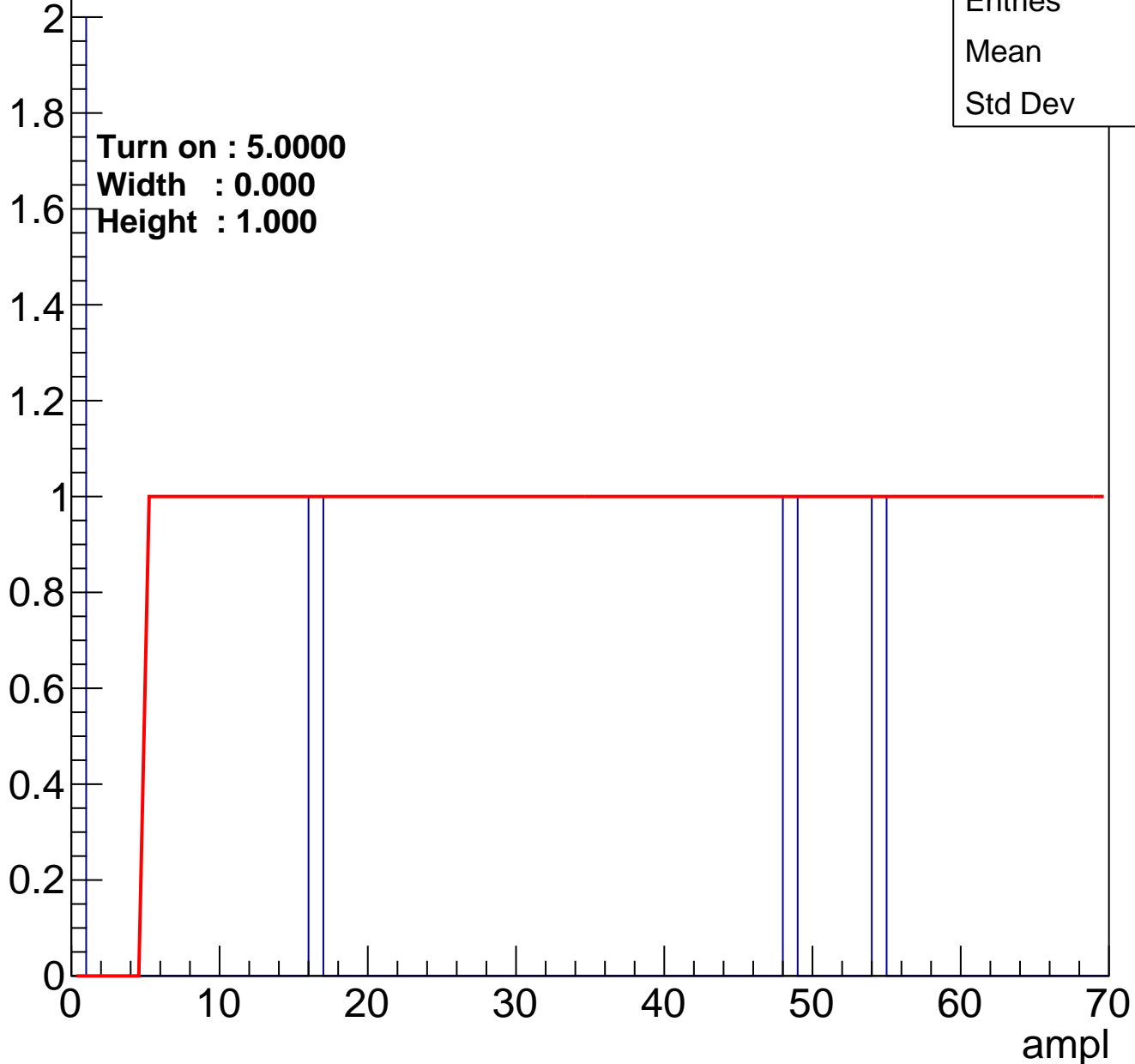


Entries	2
Mean	0
Std Dev	0

B0L101S, U2-ch120

calib_packv5_042523_0143.root, FC#1, port C1

Entry



Turn on : 5.0000

Width : 0.000

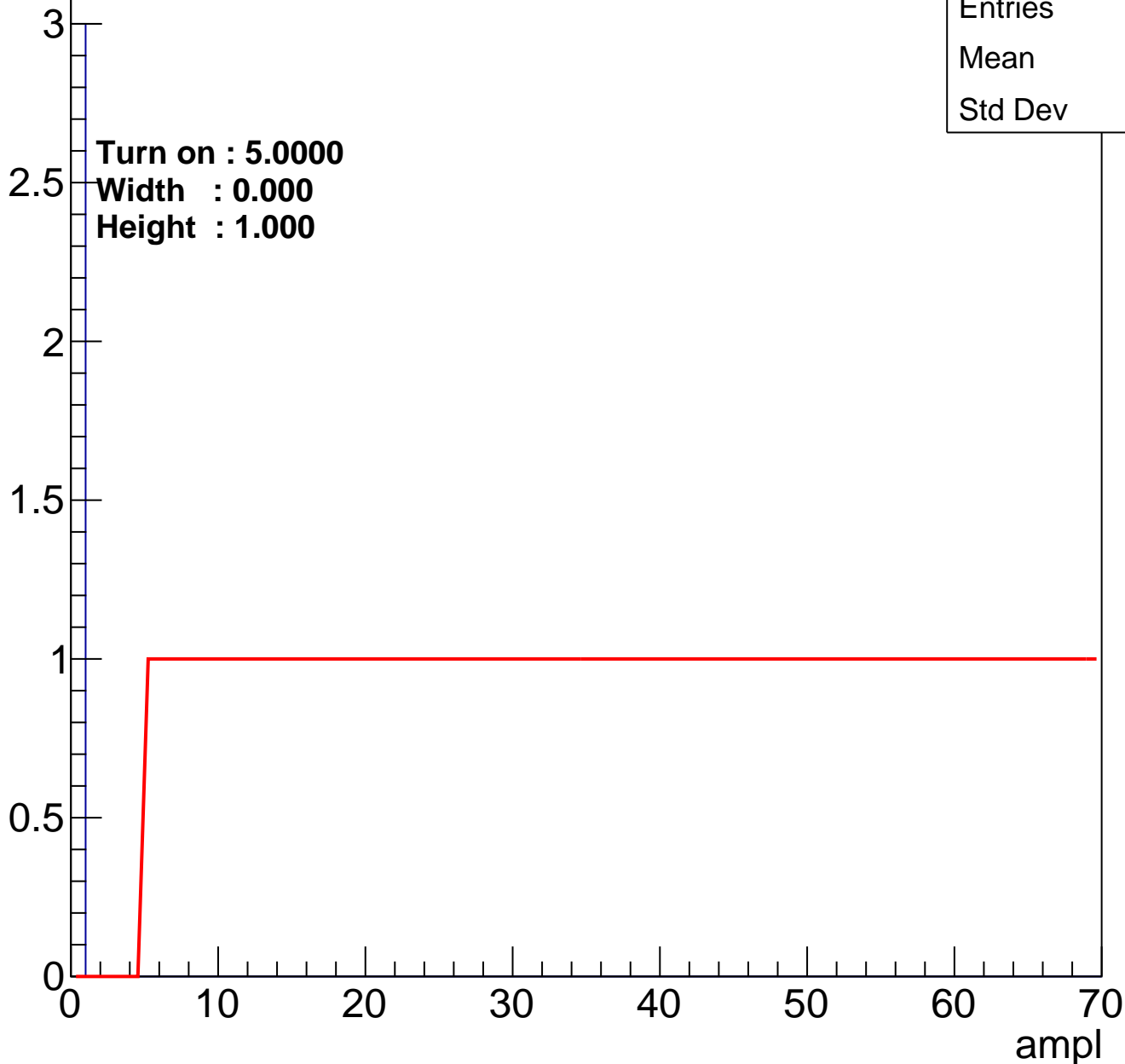
Height : 1.000

Entries	5
Mean	23.6
Std Dev	23.2

B0L101S, U2-ch121

calib_packv5_042523_0143.root, FC#1, port C1

Entry

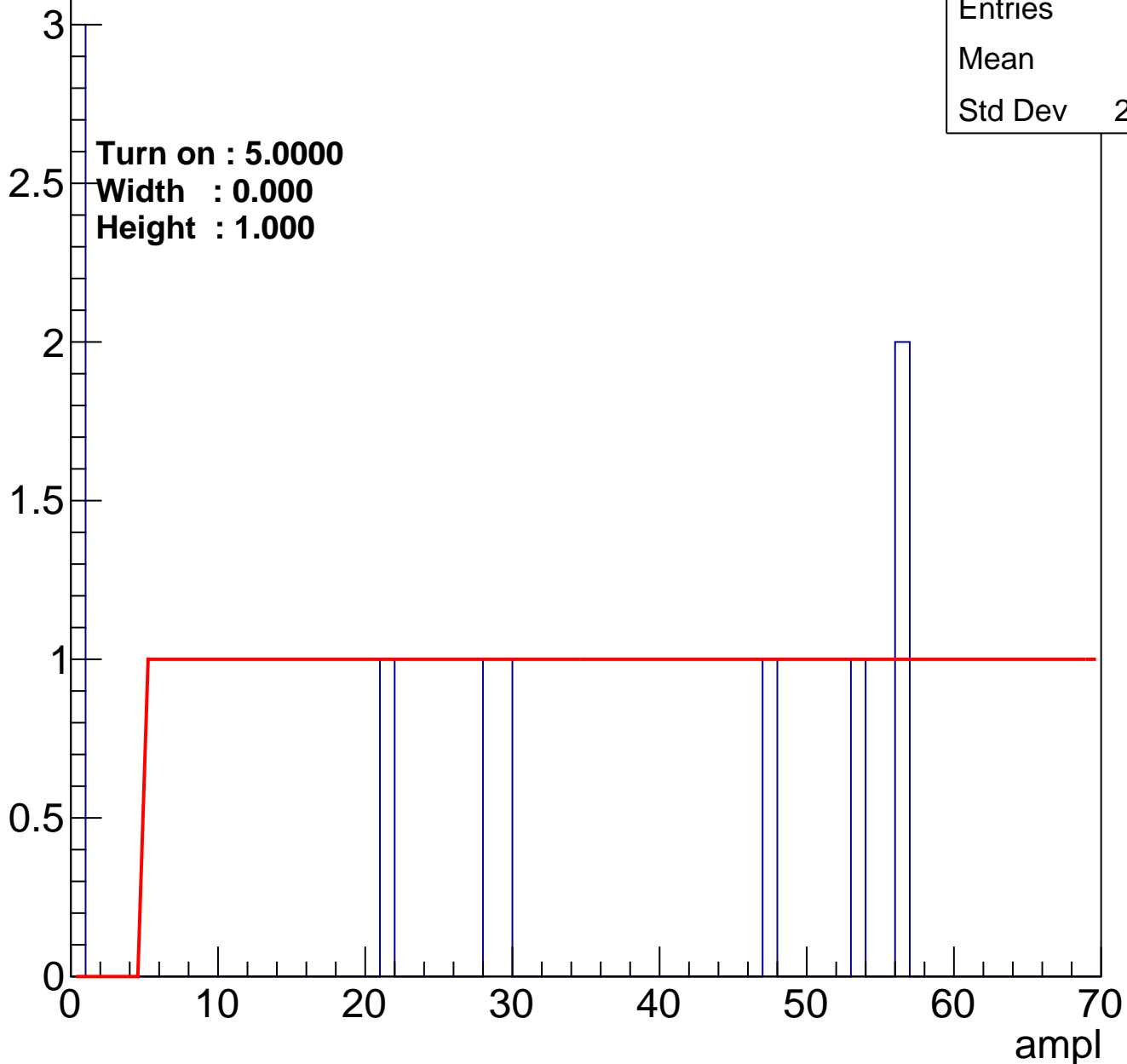


Entries	3
Mean	0
Std Dev	0

B0L101S, U2-ch122

calib_packv5_042523_0143.root, FC#1, port C1

Entry

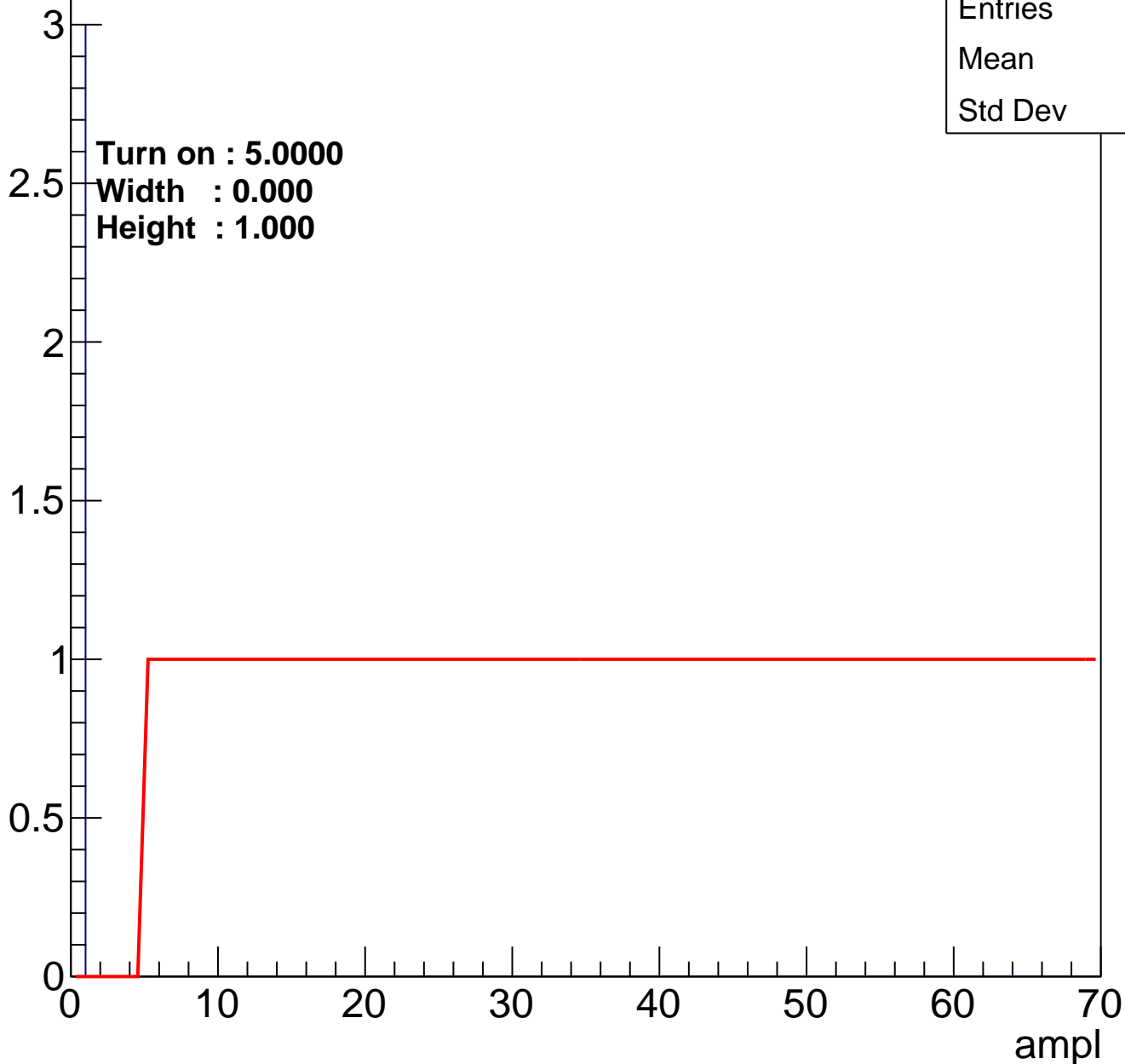


Entries	10
Mean	29
Std Dev	22.24

B0L101S, U2-ch123

calib_packv5_042523_0143.root, FC#1, port C1

Entry

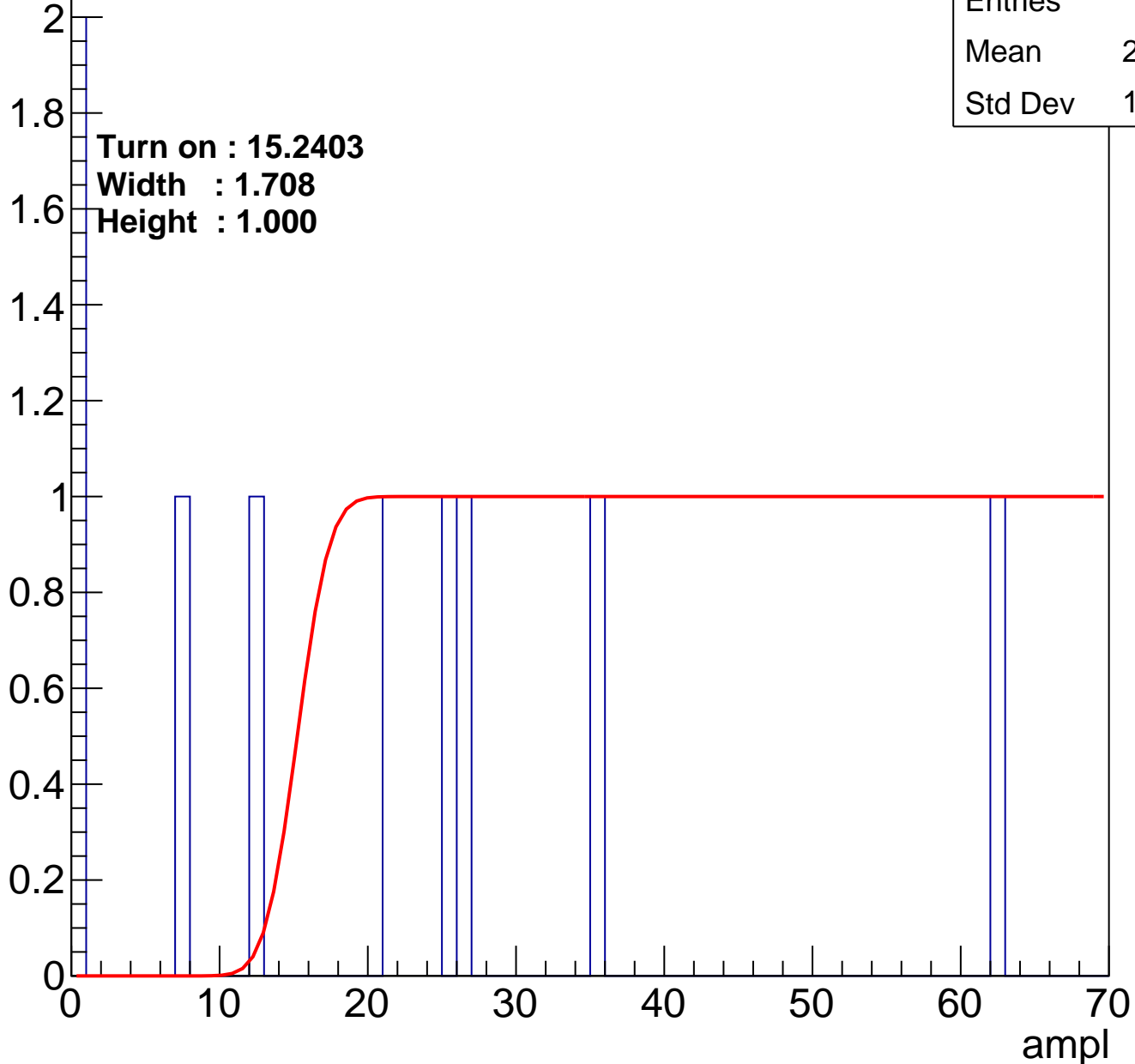


Entries	3
Mean	0
Std Dev	0

B0L101S, U2-ch124

calib_packv5_042523_0143.root, FC#1, port C1

Entry

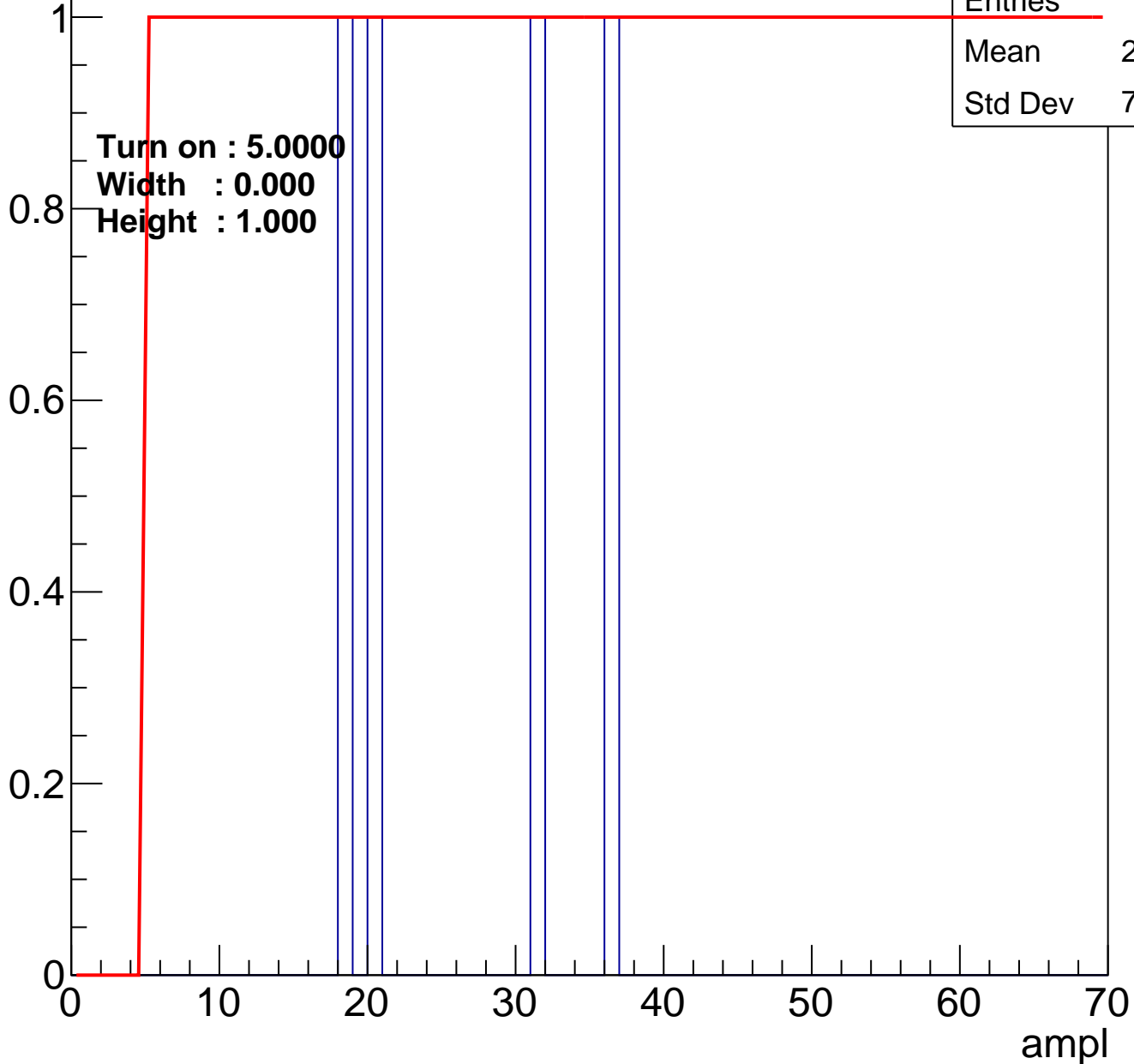


Entries	11
Mean	21.09
Std Dev	16.72

B0L101S, U2-ch125

calib_packv5_042523_0143.root, FC#1, port C1

Entry

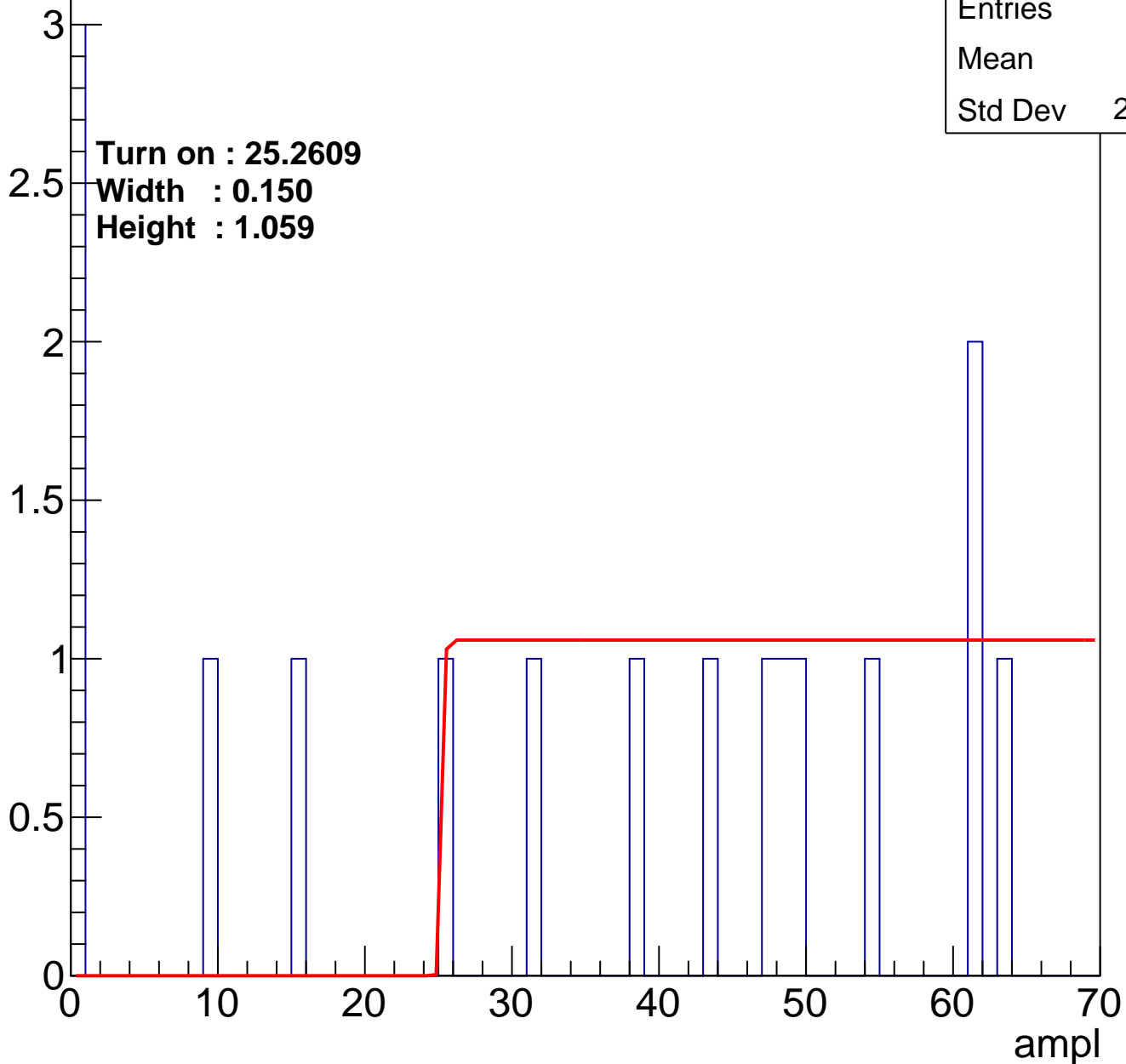


Entries	4
Mean	26.25
Std Dev	7.496

B0L101S, U2-ch126

calib_packv5_042523_0143.root, FC#1, port C1

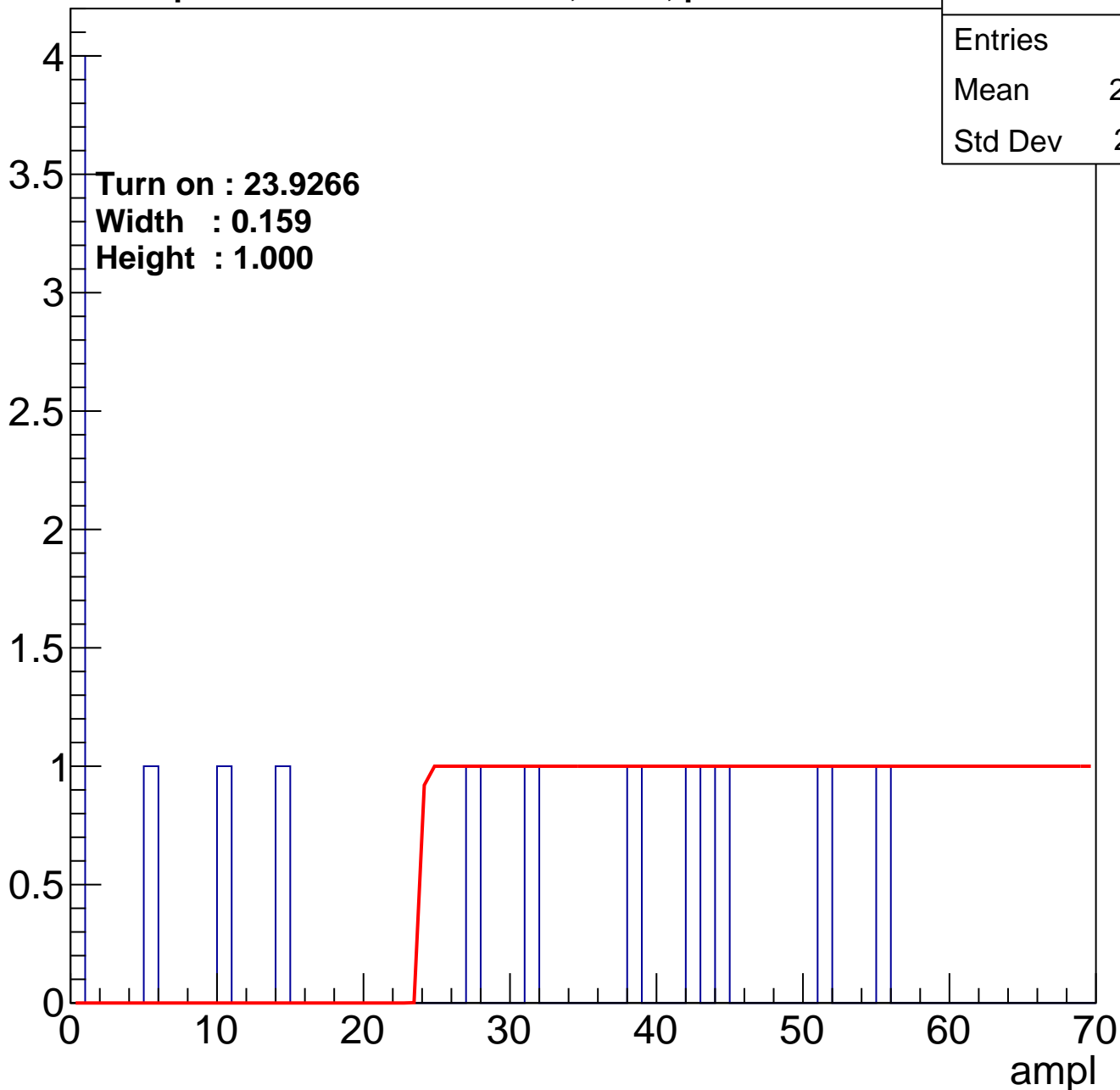
Entry



B0L101S, U2-ch127

calib_packv5_042523_0143.root, FC#1, port C1

Entry



B0L101S, U2-ch127

calib_packv5_042523_0143.root, FC#1, port C1

Entry

