



# B0L001S, U25-ch0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	352
Mean	45.62
Std Dev	10.84

Turn on : 28.9092

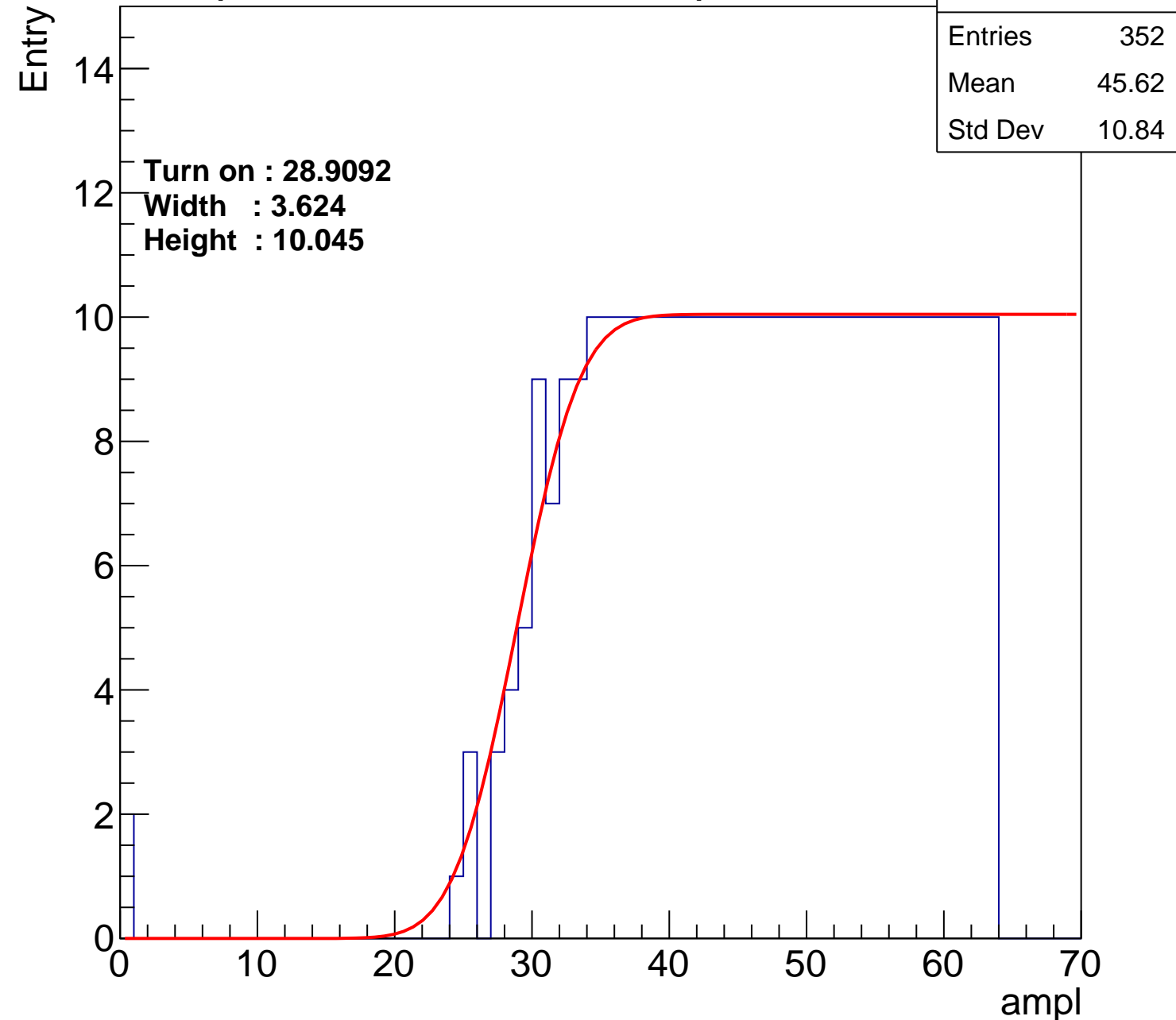
Width : 3.624

Height : 10.045

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	350
Mean	45.73
Std Dev	10.77

**Turn on : 29.6438**

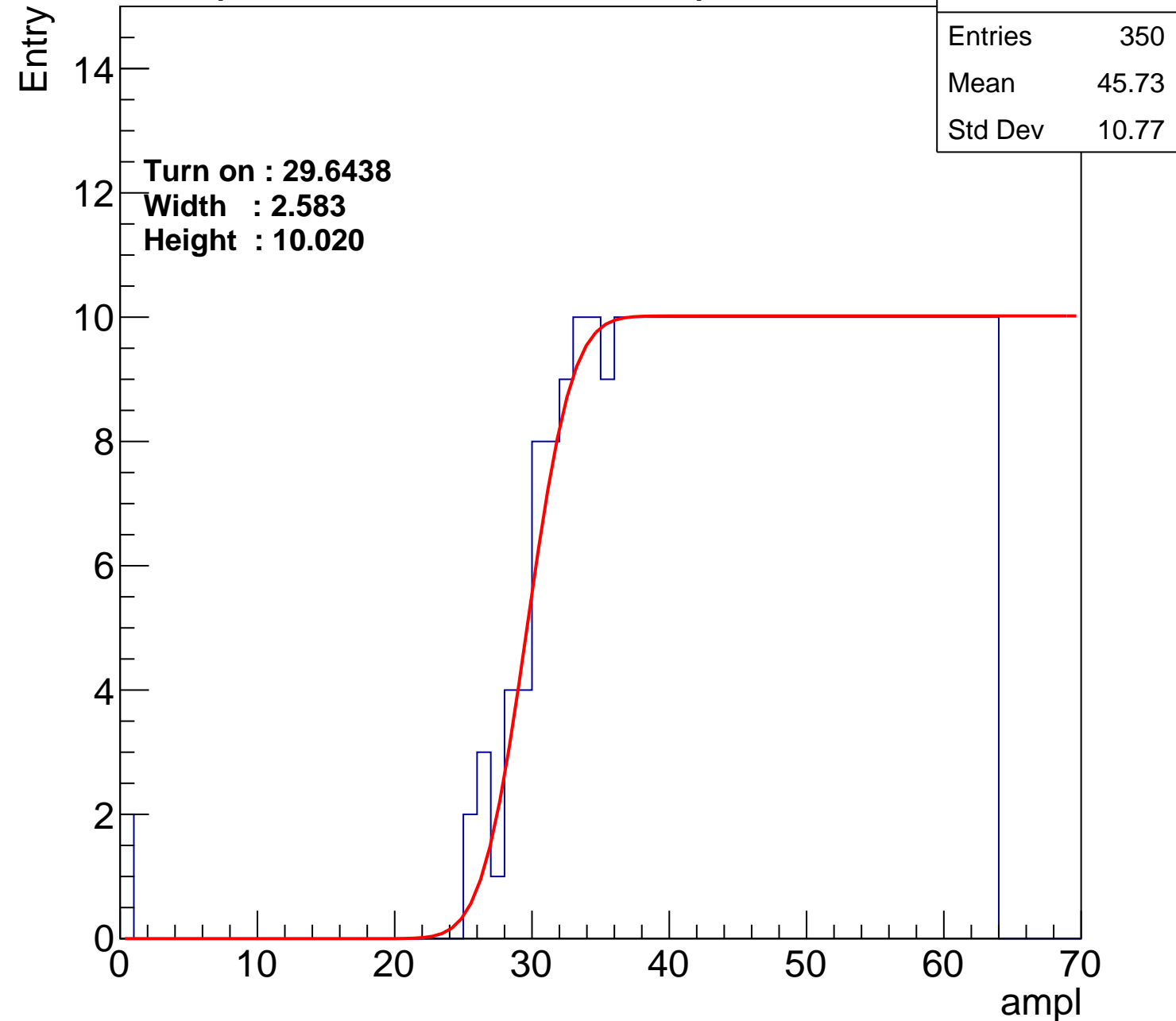
**Width : 2.583**

**Height : 10.020**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	360
Mean	45.29
Std Dev	10.93

**Turn on : 28.6528**

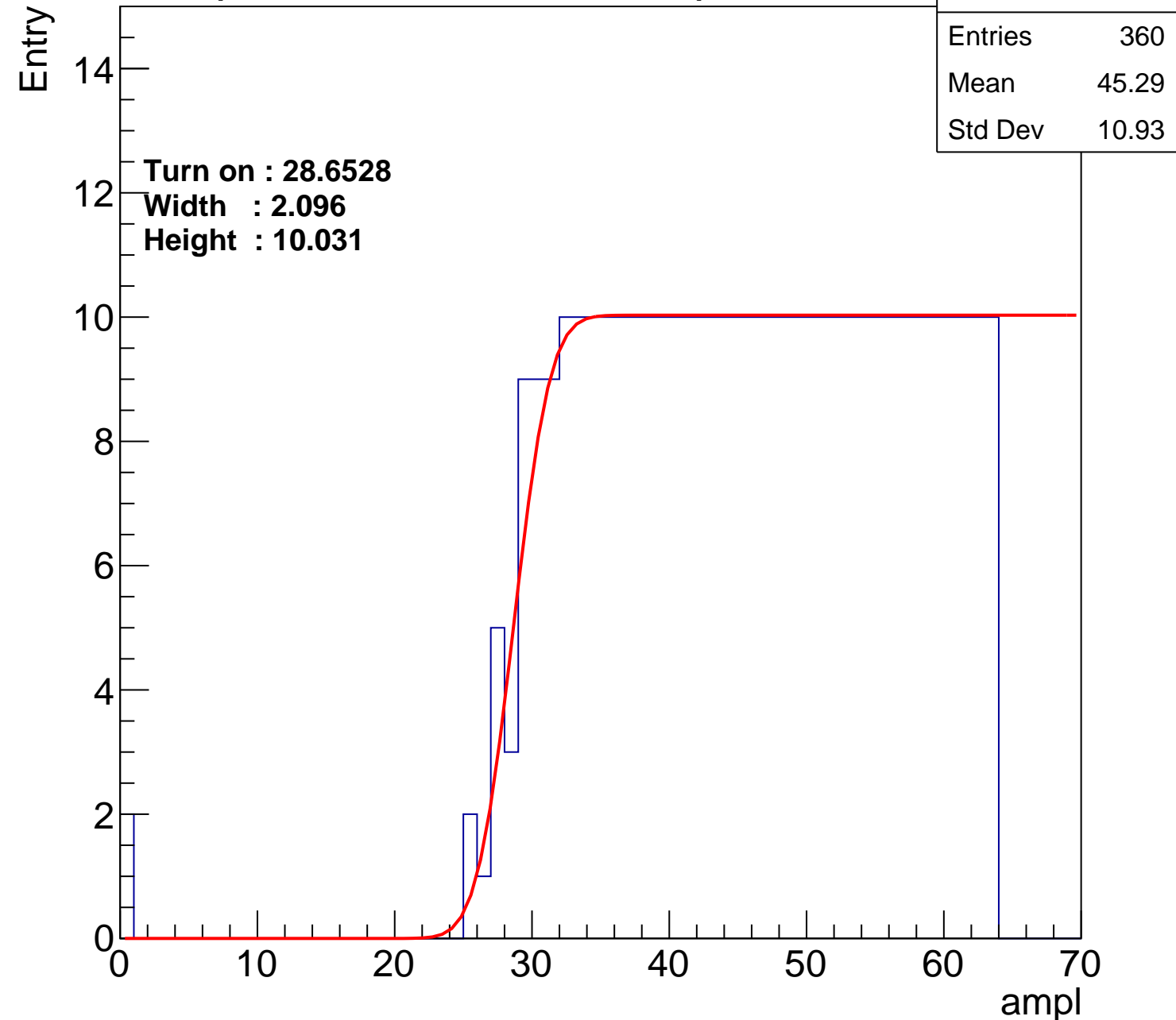
**Width : 2.096**

**Height : 10.031**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	361
Mean	45.13
Std Dev	11.24

**Turn on : 28.5040**

**Width : 2.142**

**Height : 9.997**

Entry

14

12

10

8

6

4

2

0

0

10

20

30

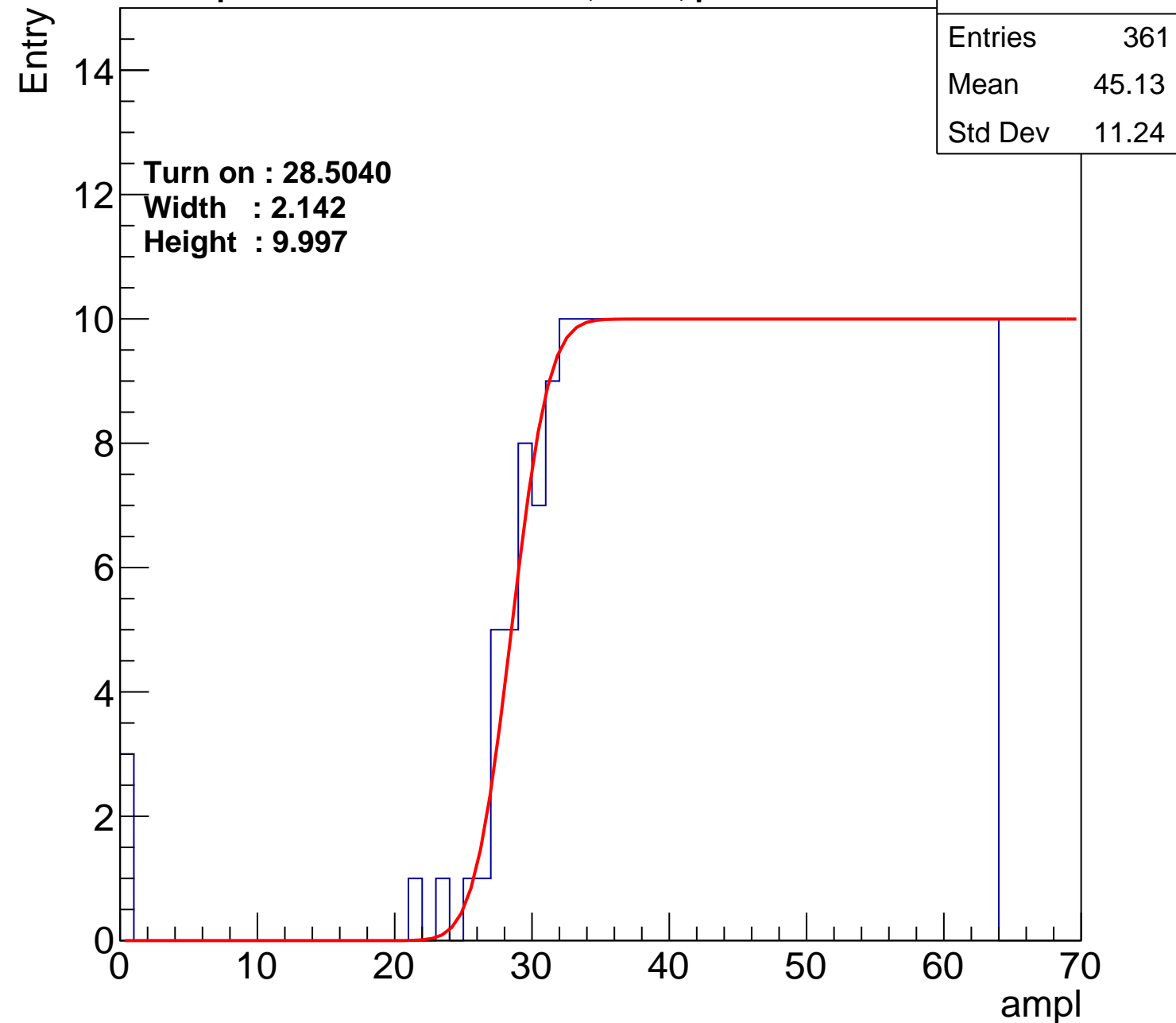
40

50

60

70

ampl



# B0L001S, U25-ch4

calib\_packv5\_042523\_0143.root, FC#9, port A1

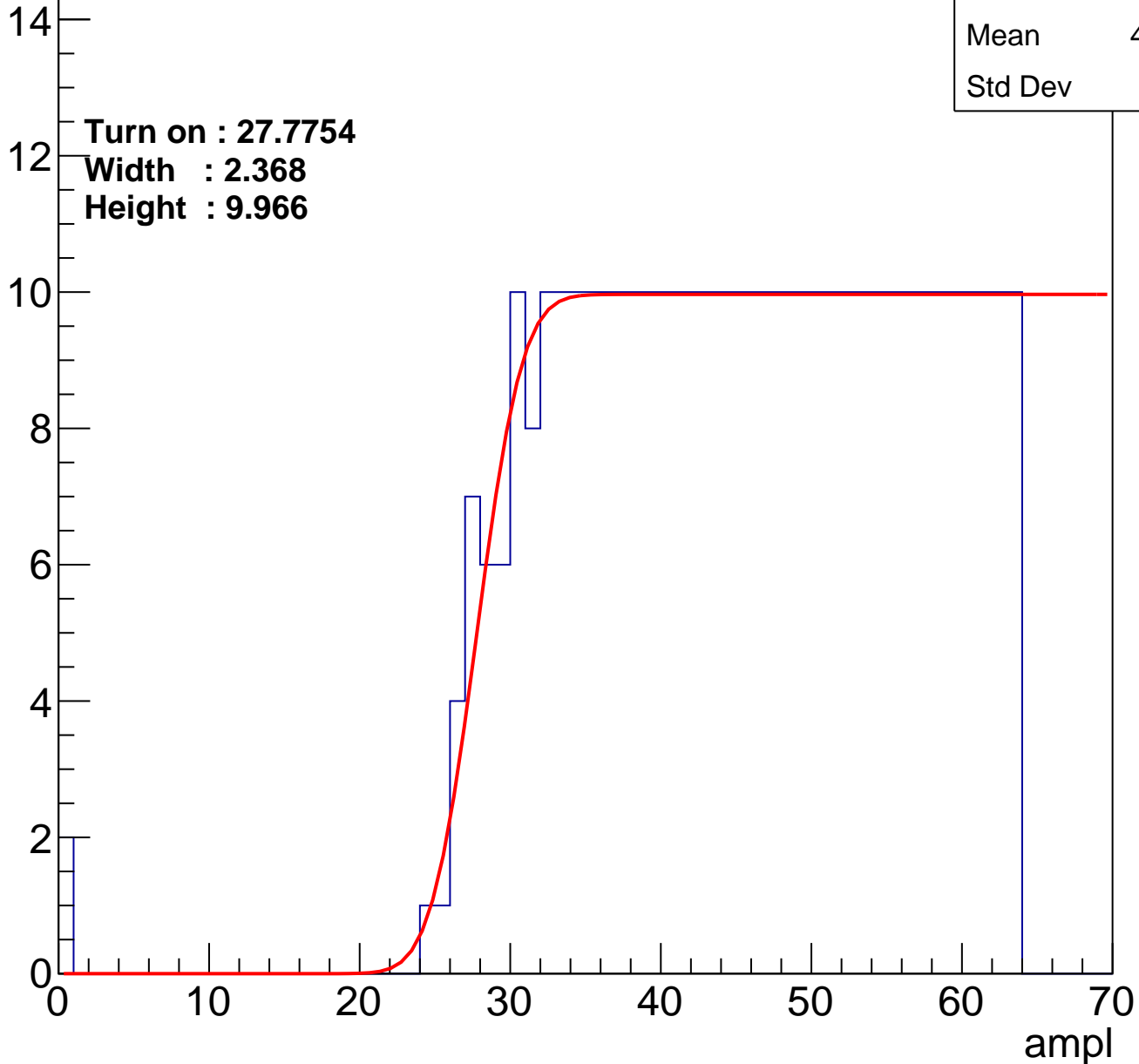
Entries	365
Mean	45.02
Std Dev	11.1

**Turn on : 27.7754**

**Width : 2.368**

**Height : 9.966**

Entry



# B0L001S, U25-ch5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	372
Mean	44.62
Std Dev	11.45

Turn on : 26.8295

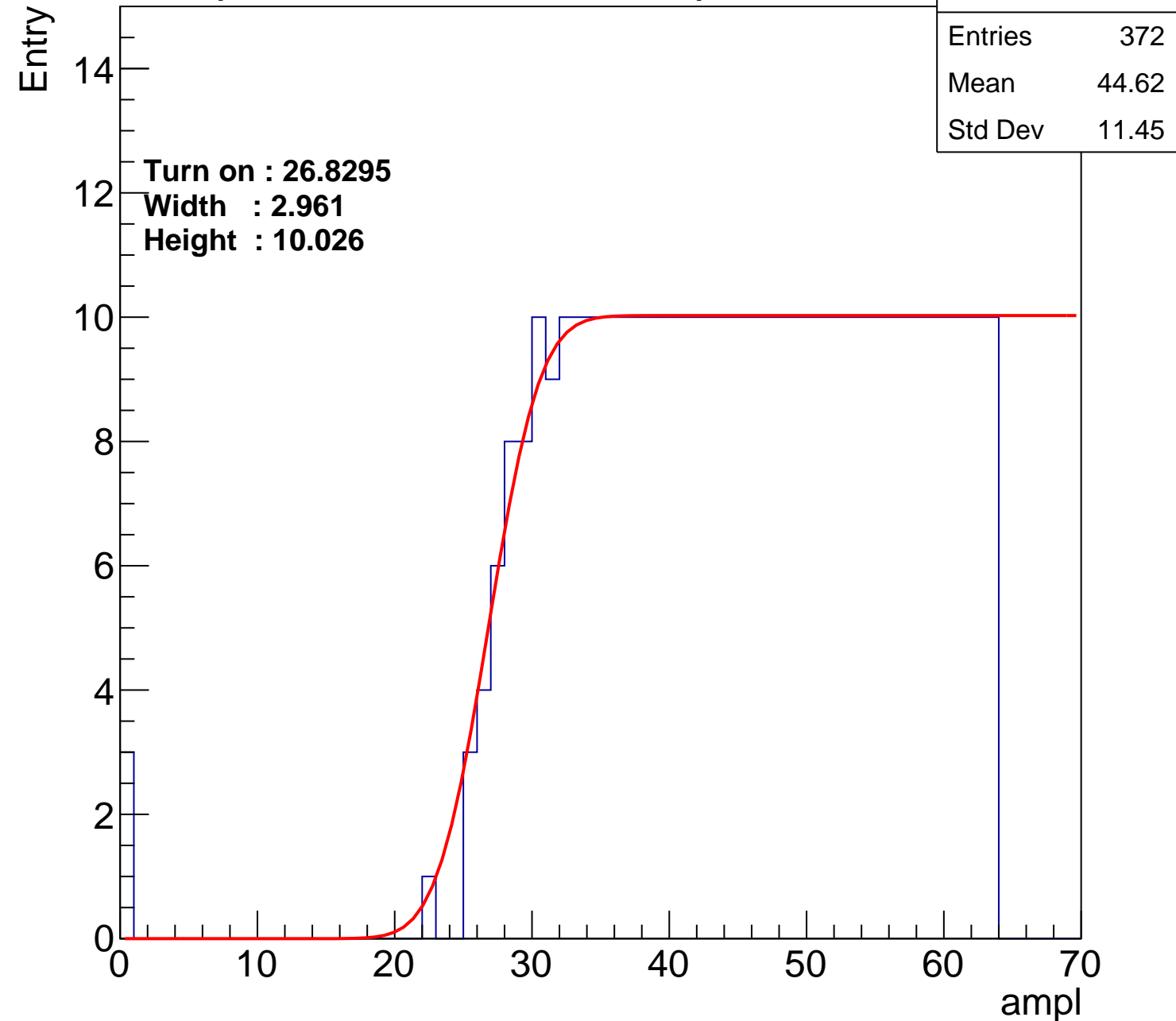
Width : 2.961

Height : 10.026

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	348
Mean	45.97
Std Dev	10.39

Turn on : 29.9381

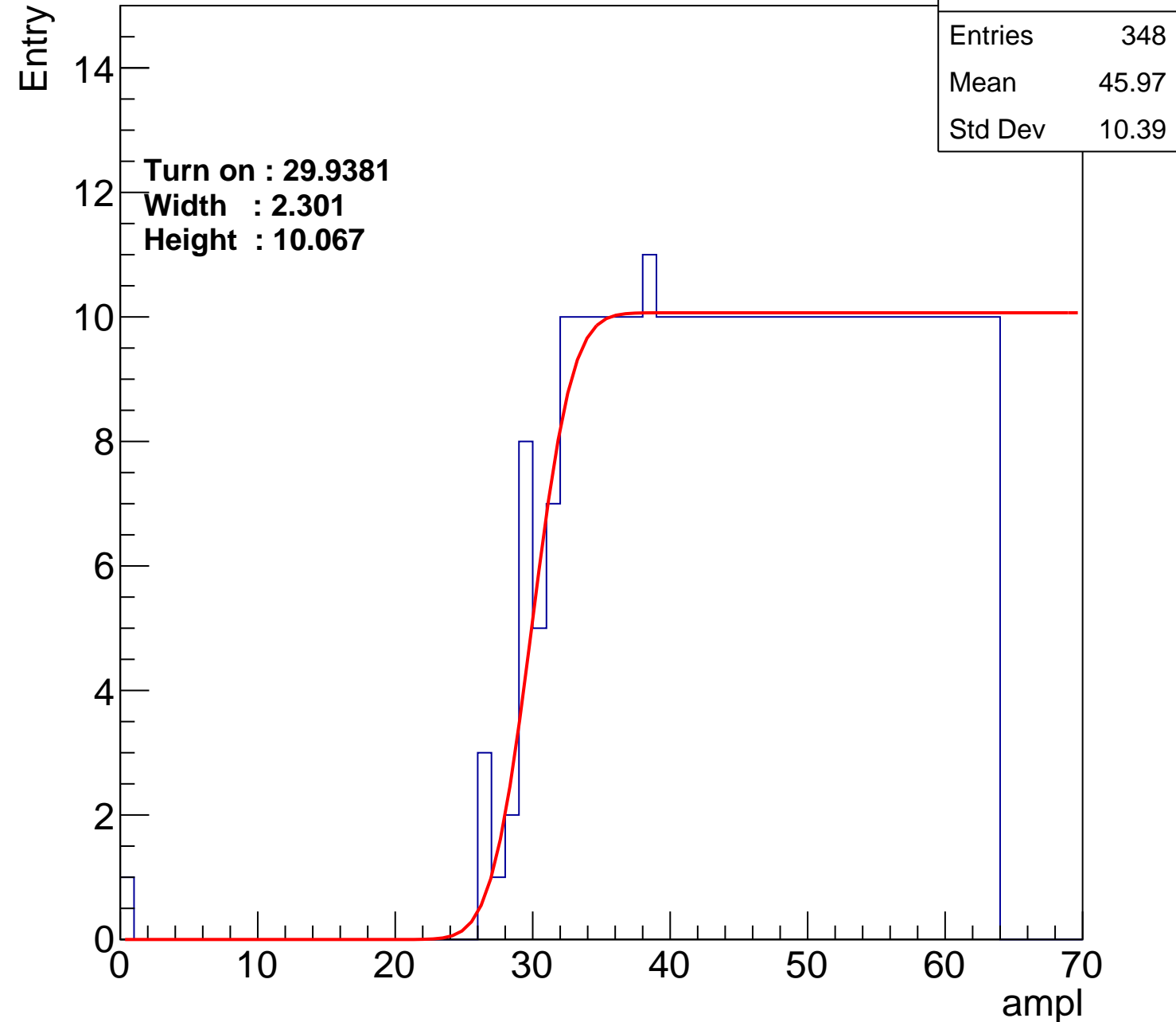
Width : 2.301

Height : 10.067

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U25-ch7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	357
Mean	45.54
Std Dev	10.63

Turn on : 28.5154

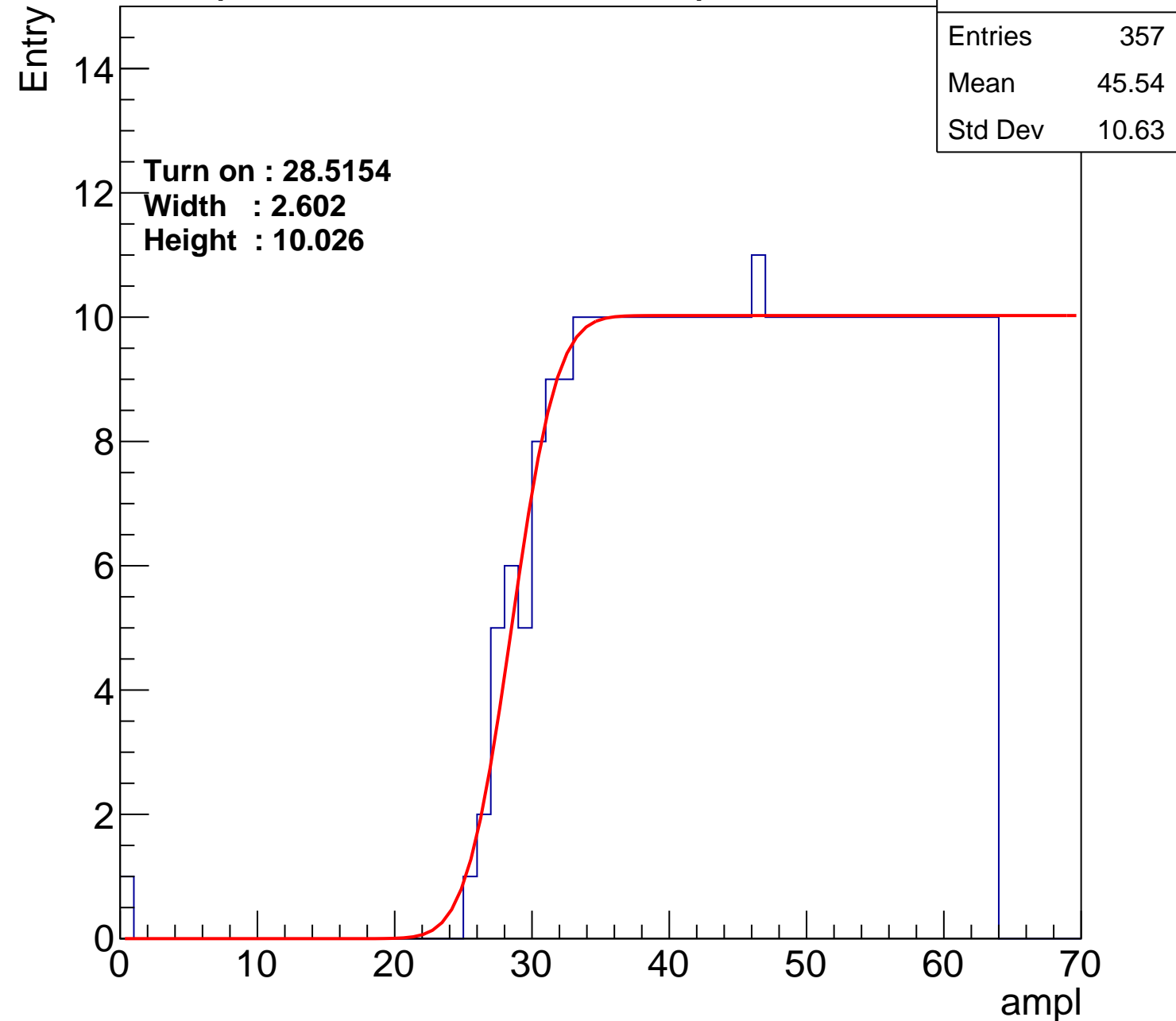
Width : 2.602

Height : 10.026

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch8

calib\_packv5\_042523\_0143.root, FC#9, port A1

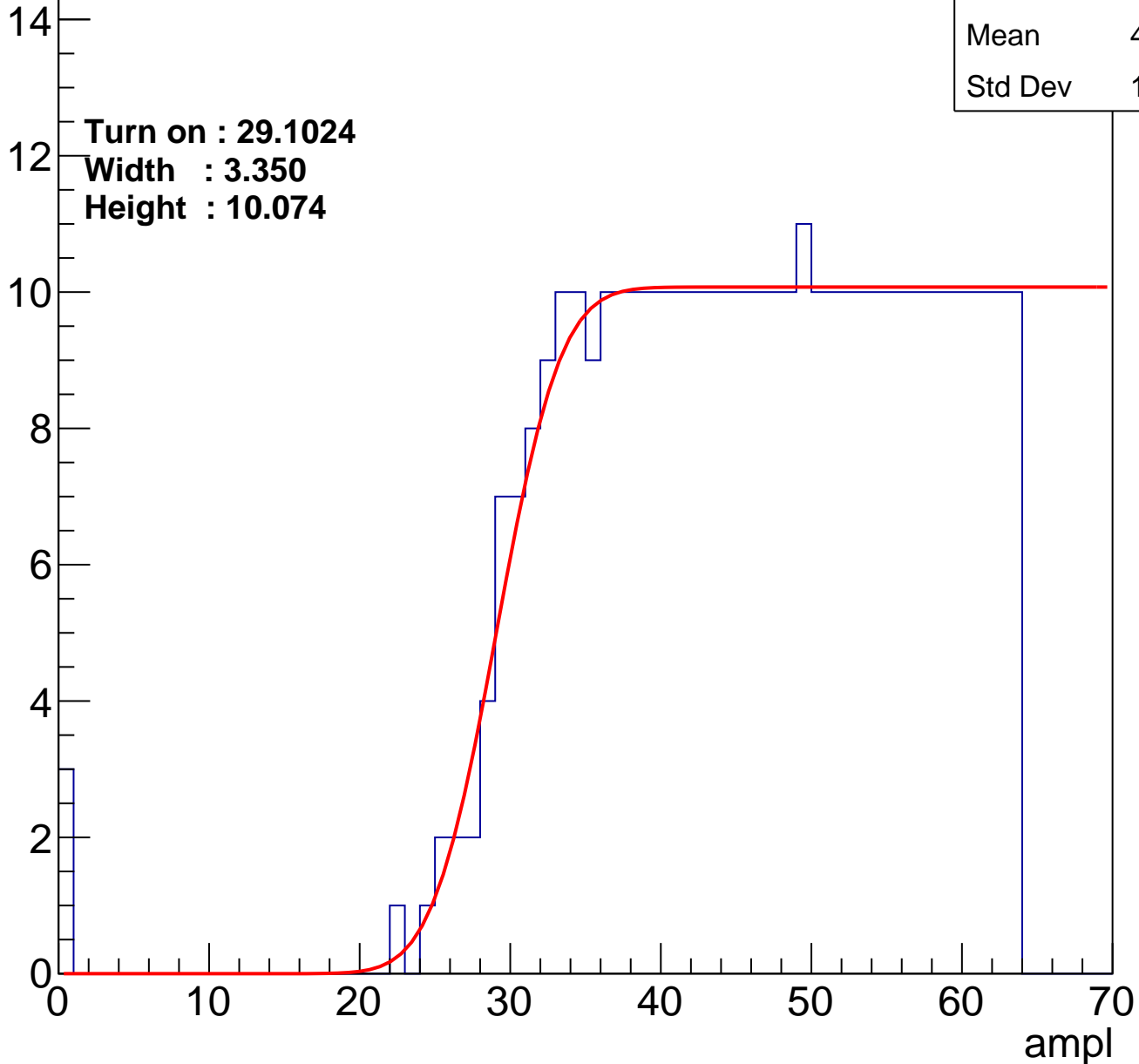
Entries	356
Mean	45.38
Std Dev	11.15

Turn on : 29.1024

Width : 3.350

Height : 10.074

Entry



# B0L001S, U25-ch9

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	381
Mean	44.4
Std Dev	11.4

Turn on : 26.7066

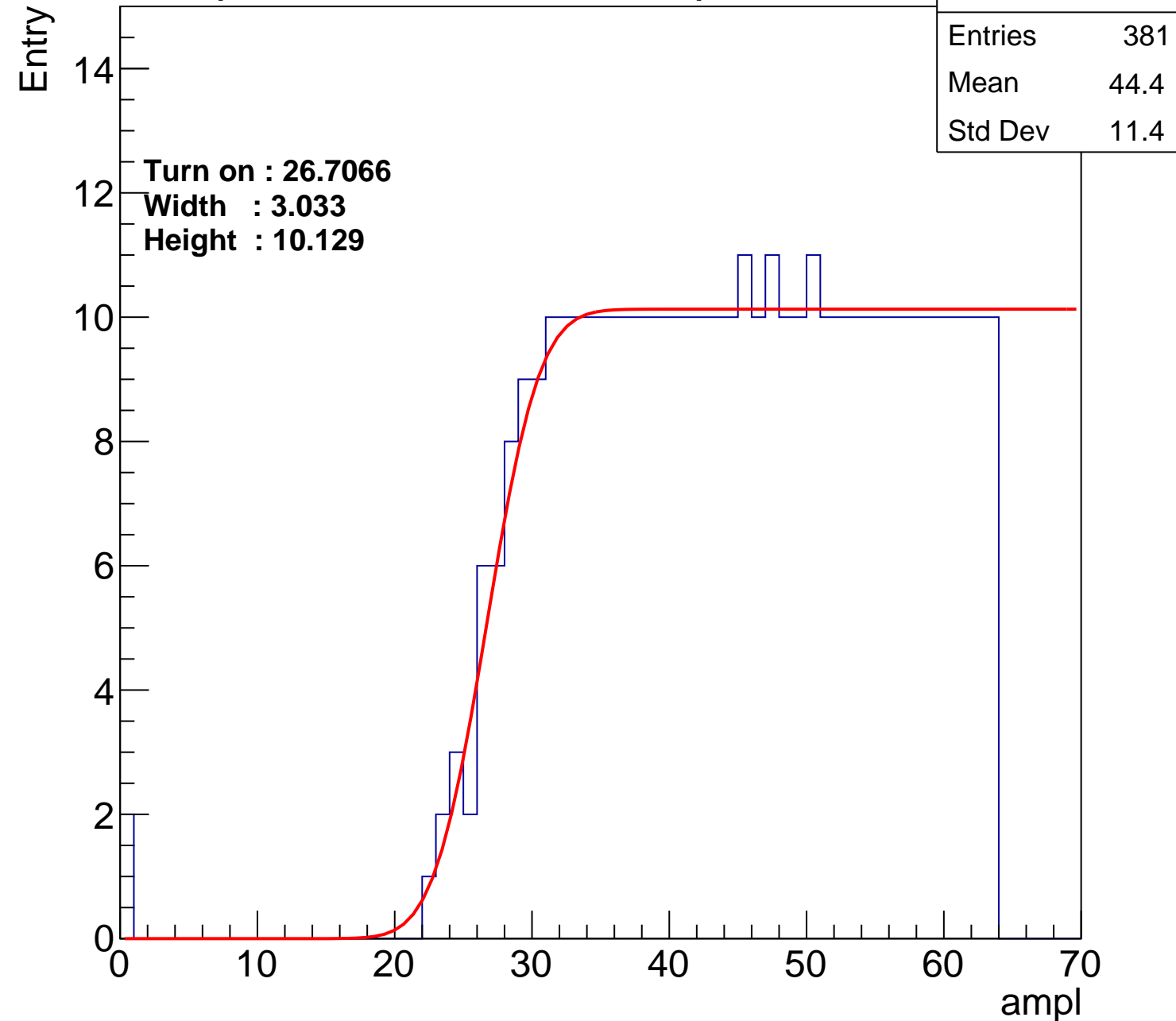
Width : 3.033

Height : 10.129

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch10

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	361
Mean	45.03
Std Dev	11.47

Turn on : 28.7611

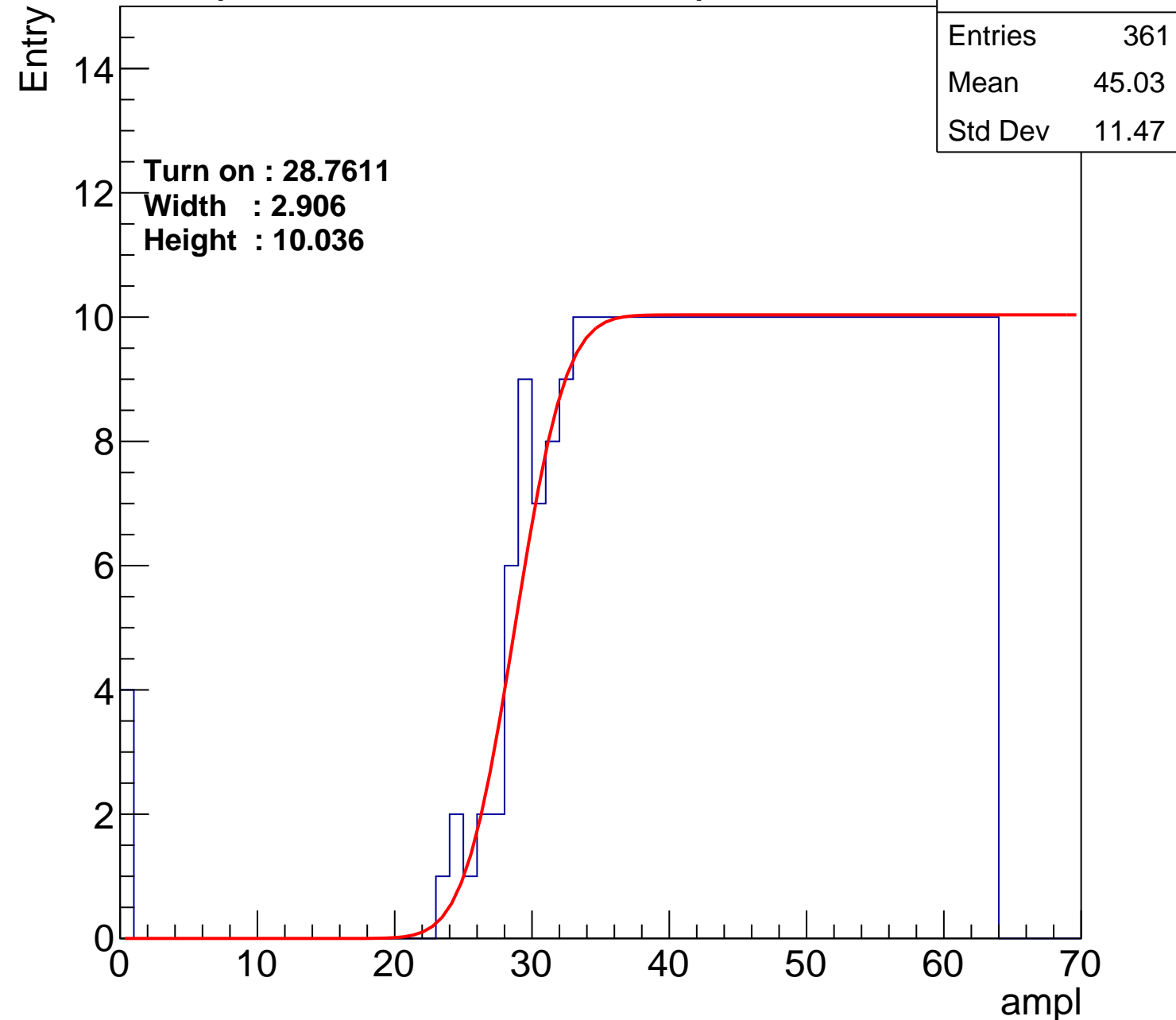
Width : 2.906

Height : 10.036

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch11

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	338
Mean	46.39
Std Dev	10.24

Turn on : 30.3919

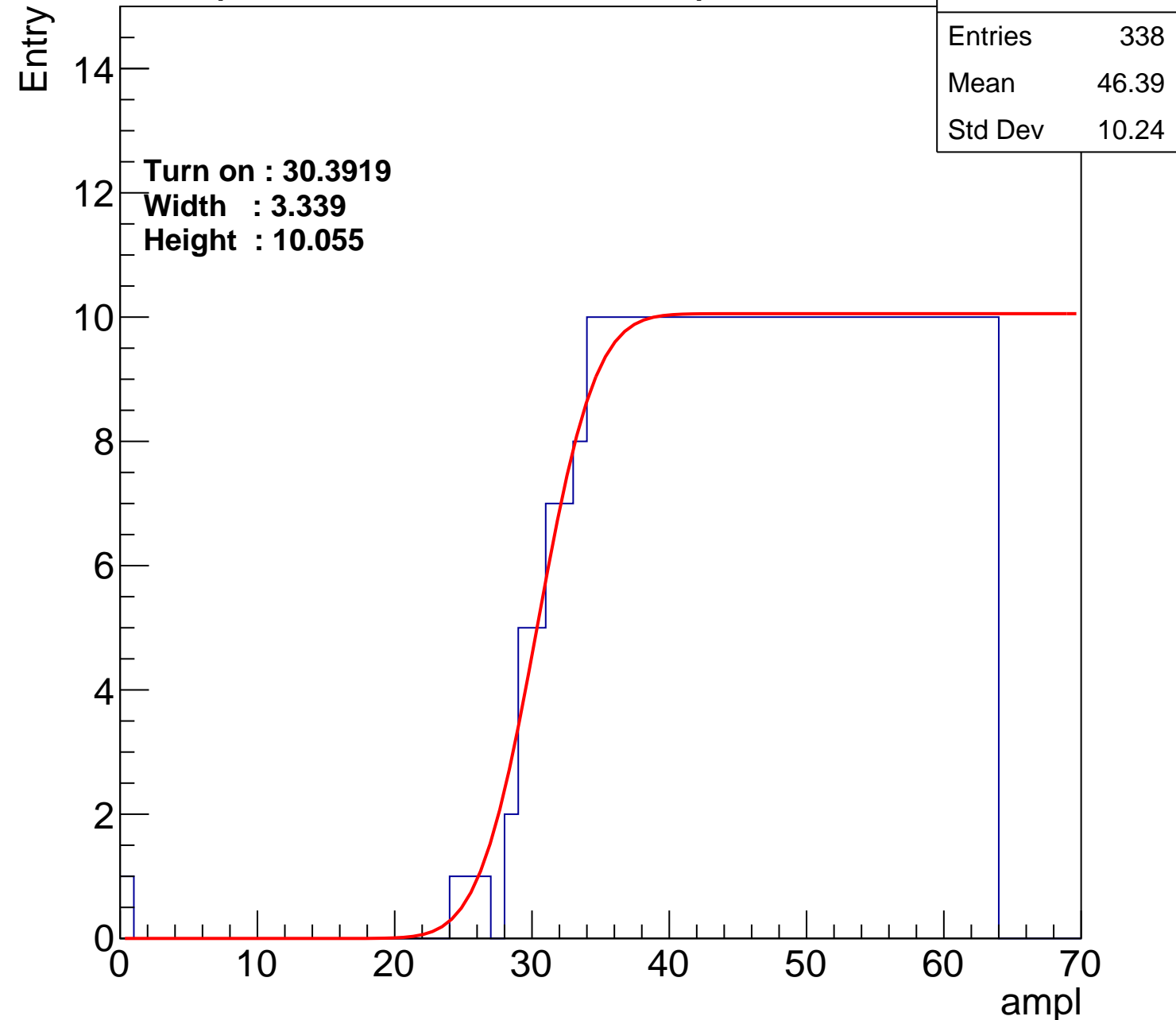
Width : 3.339

Height : 10.055

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch12

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	376
Mean	44.57
Std Dev	11.16

Turn on : 26.2675

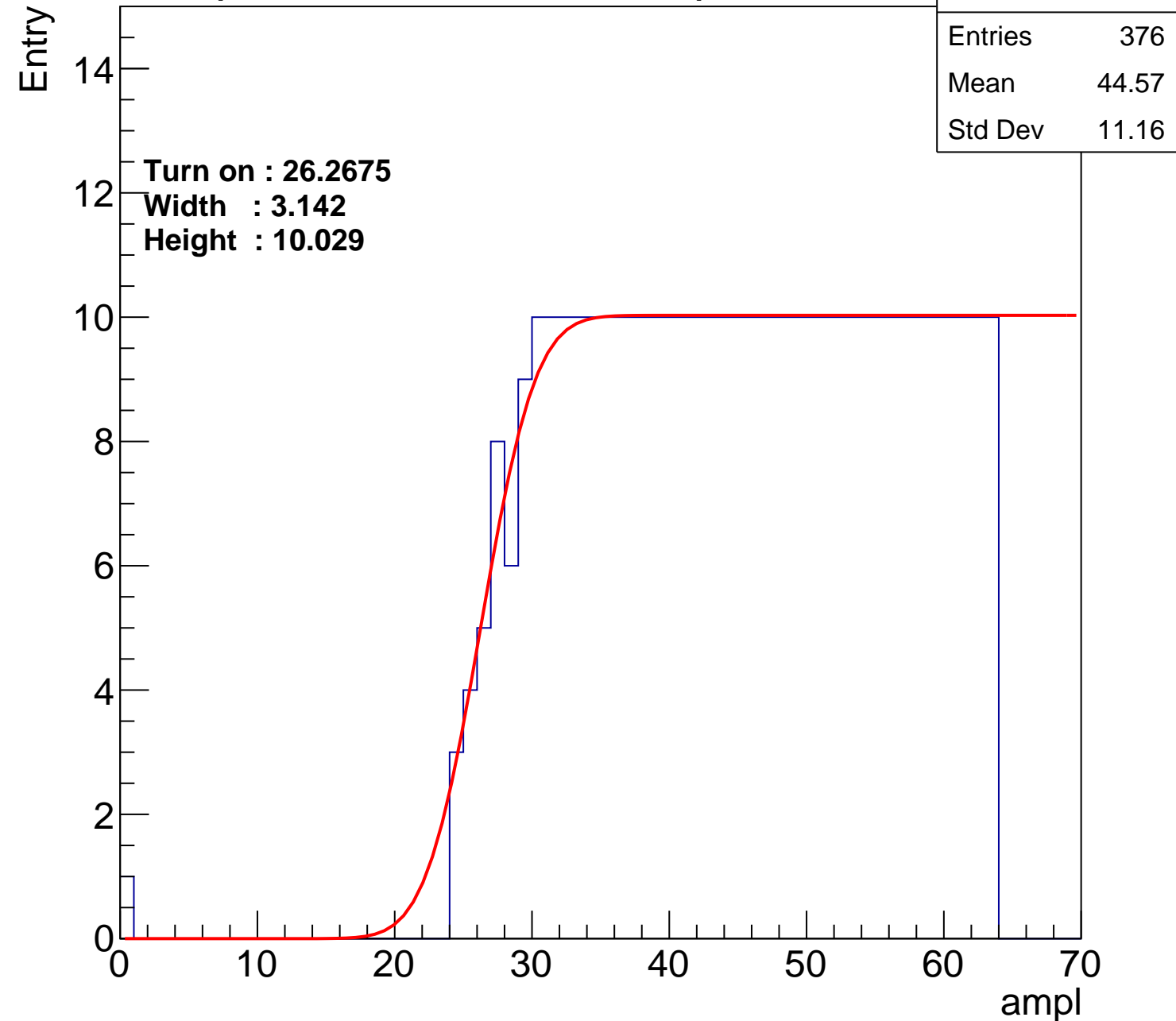
Width : 3.142

Height : 10.029

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch13

calib\_packv5\_042523\_0143.root, FC#9, port A1

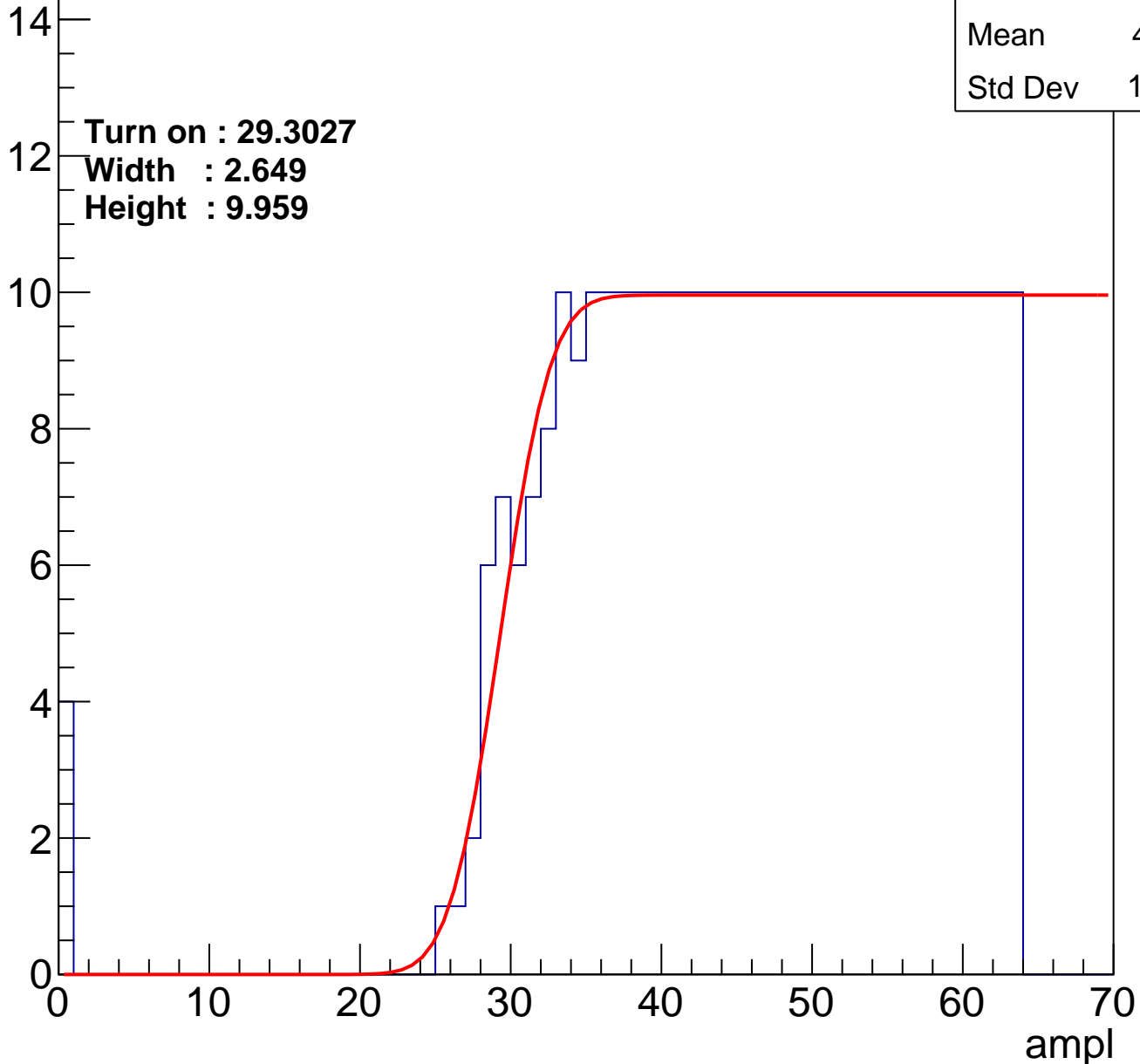
Entries	351
Mean	45.51
Std Dev	11.26

**Turn on : 29.3027**

**Width : 2.649**

**Height : 9.959**

Entry



# B0L001S, U25-ch14

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	364
Mean	44.87
Std Dev	11.56

Turn on : 28.1289

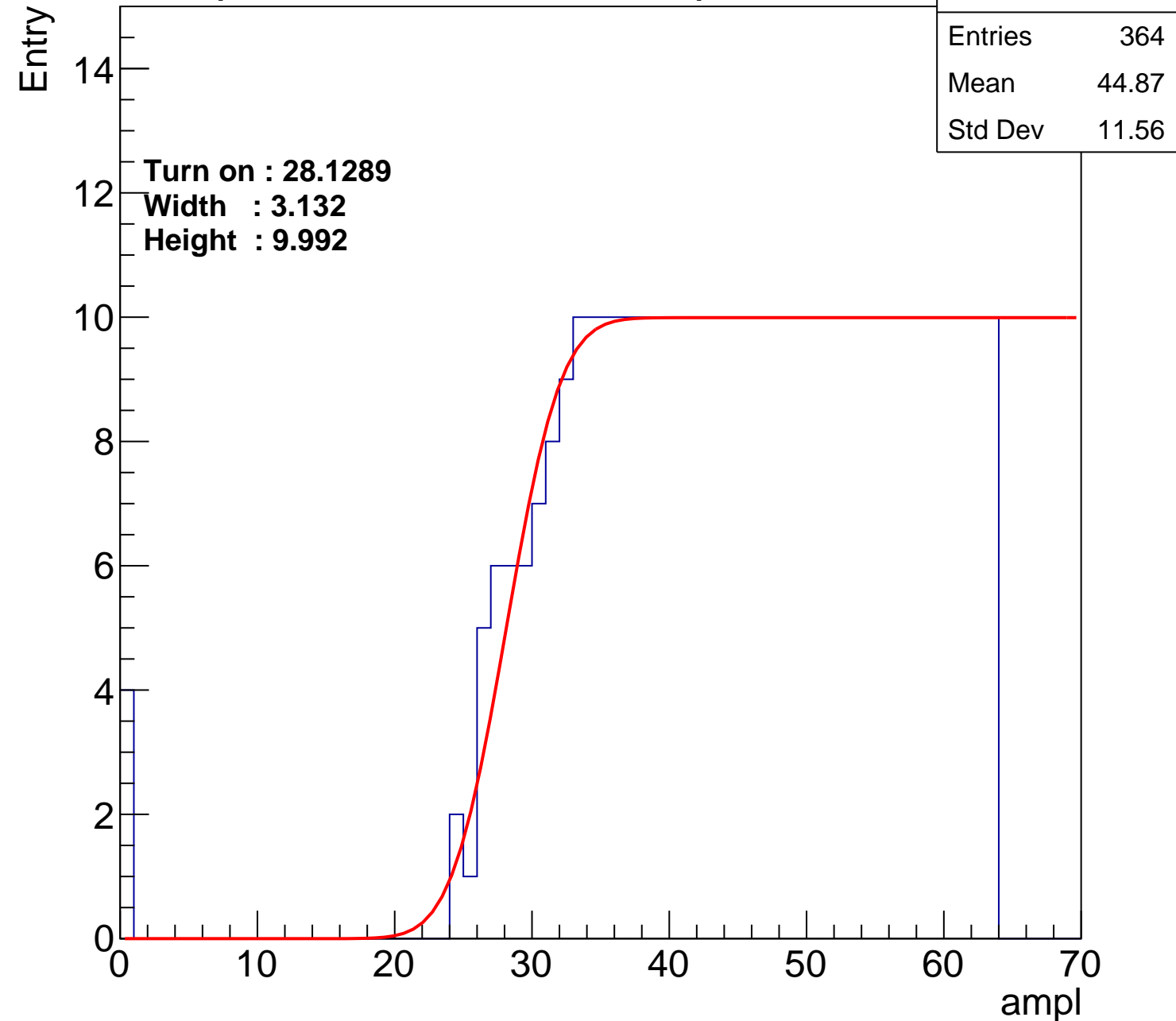
Width : 3.132

Height : 9.992

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U25-ch15

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	356
Mean	45.39
Std Dev	11.1

**Turn on : 29.3225**

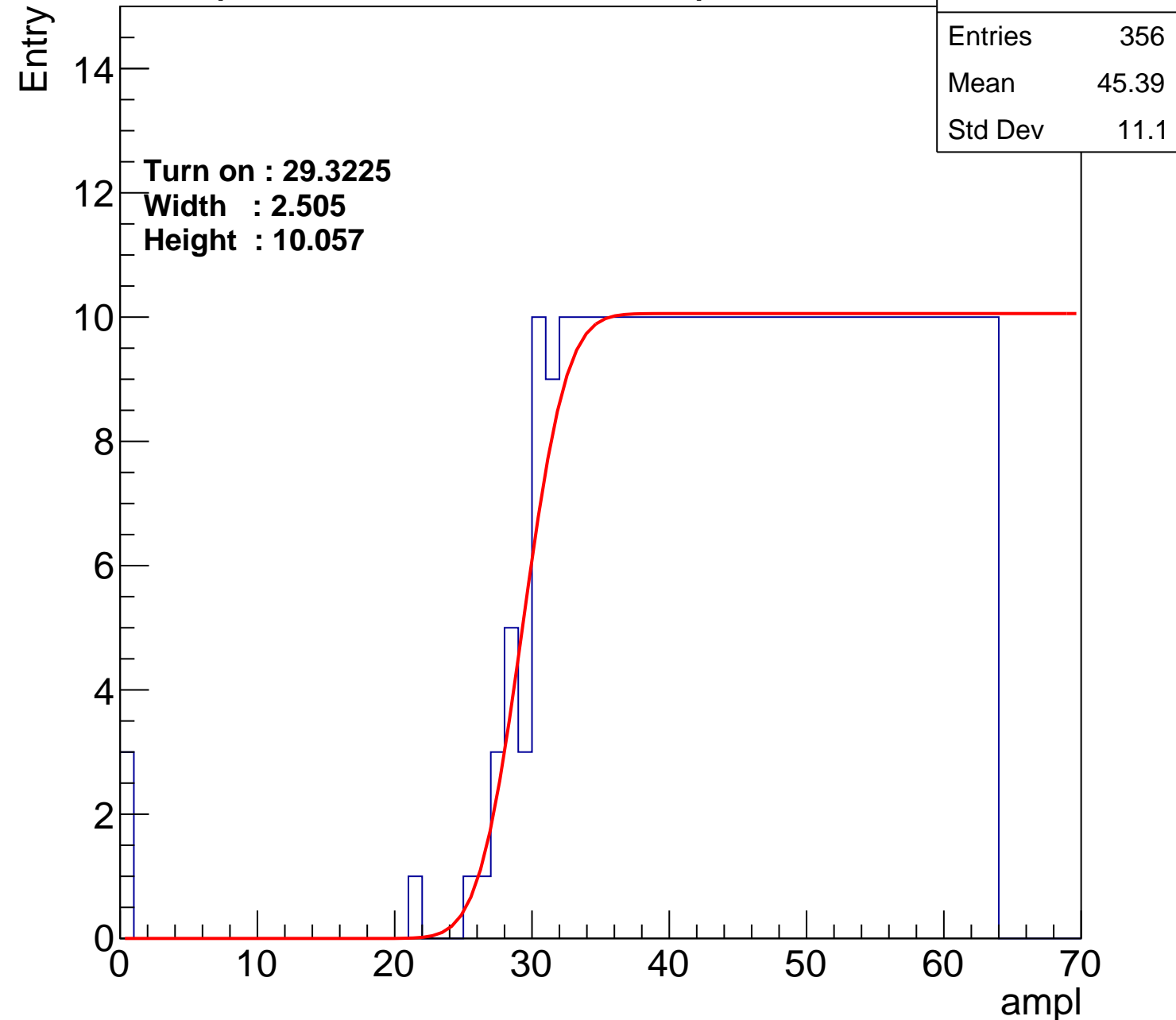
**Width : 2.505**

**Height : 10.057**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch16

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	352
Mean	45.64
Std Dev	10.8

Turn on : 29.1990

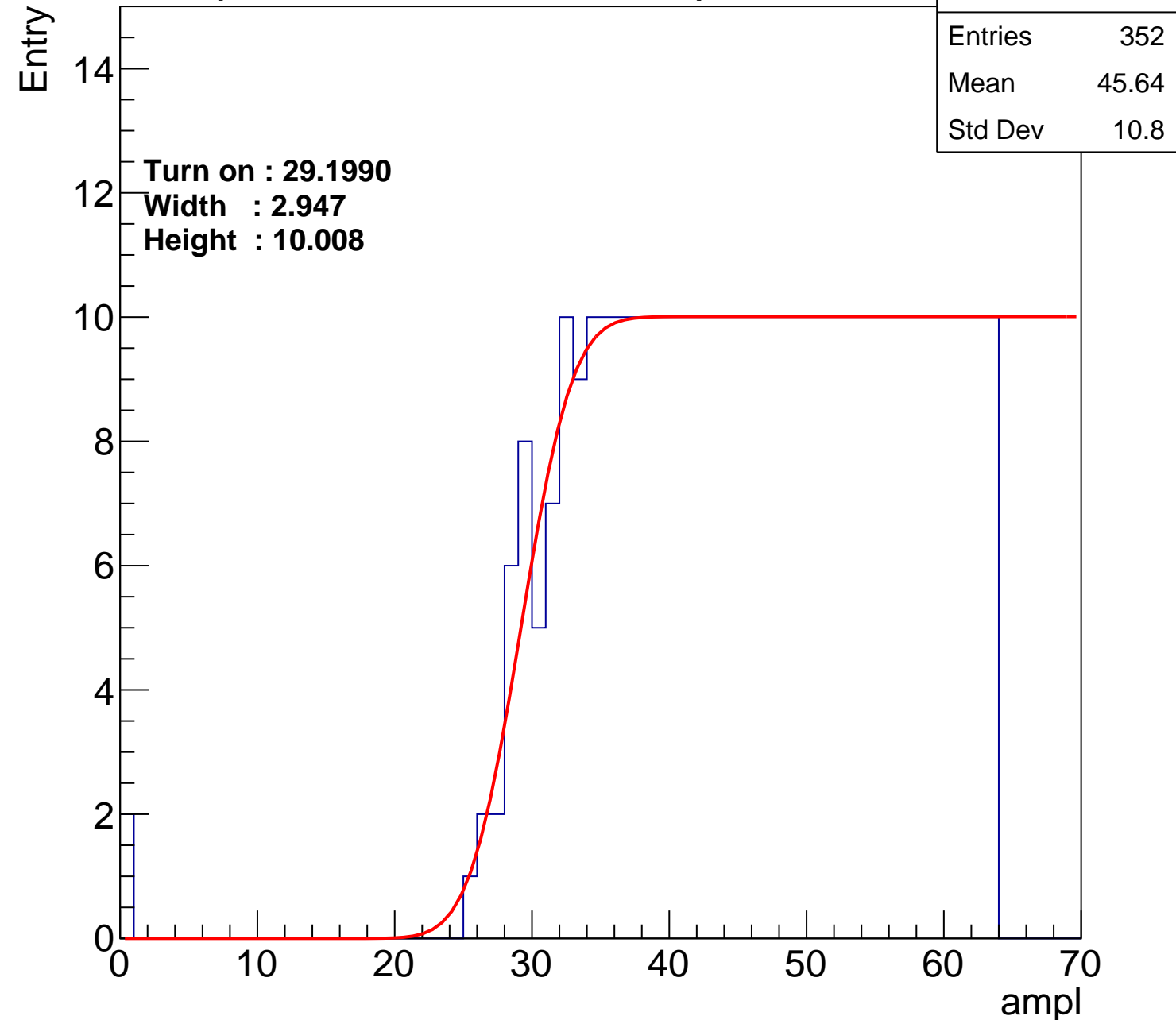
Width : 2.947

Height : 10.008

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch17

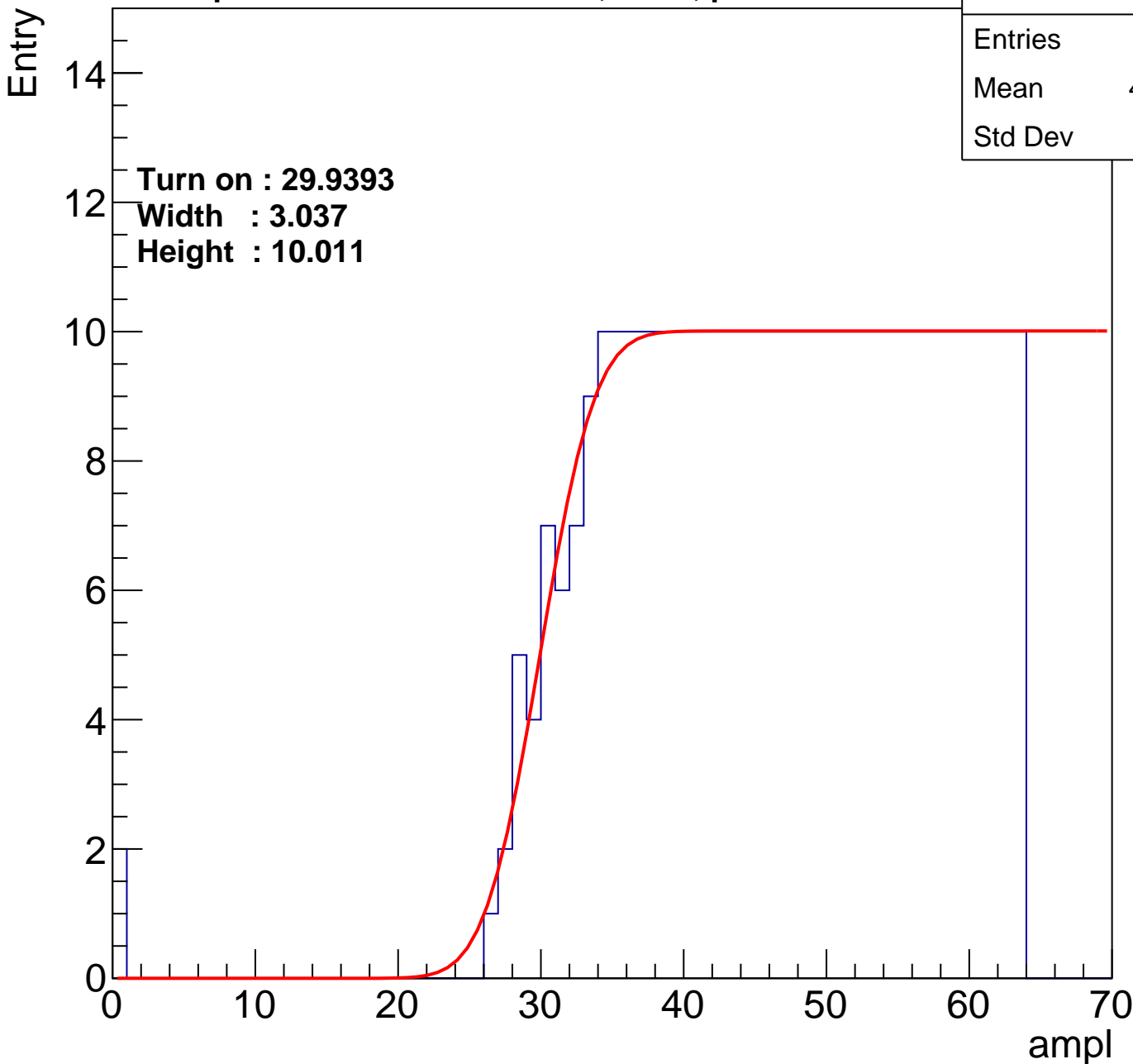
**calib\_packv5\_042523\_0143.root, FC#9, port A1**

Entries	343
Mean	46.07
Std Dev	10.6

**Turn on : 29.9393**

**Width : 3.037**

**Height : 10.011**



# B0L001S, U25-ch18

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	356
Mean	45.49
Std Dev	10.73

**Turn on : 29.2794**

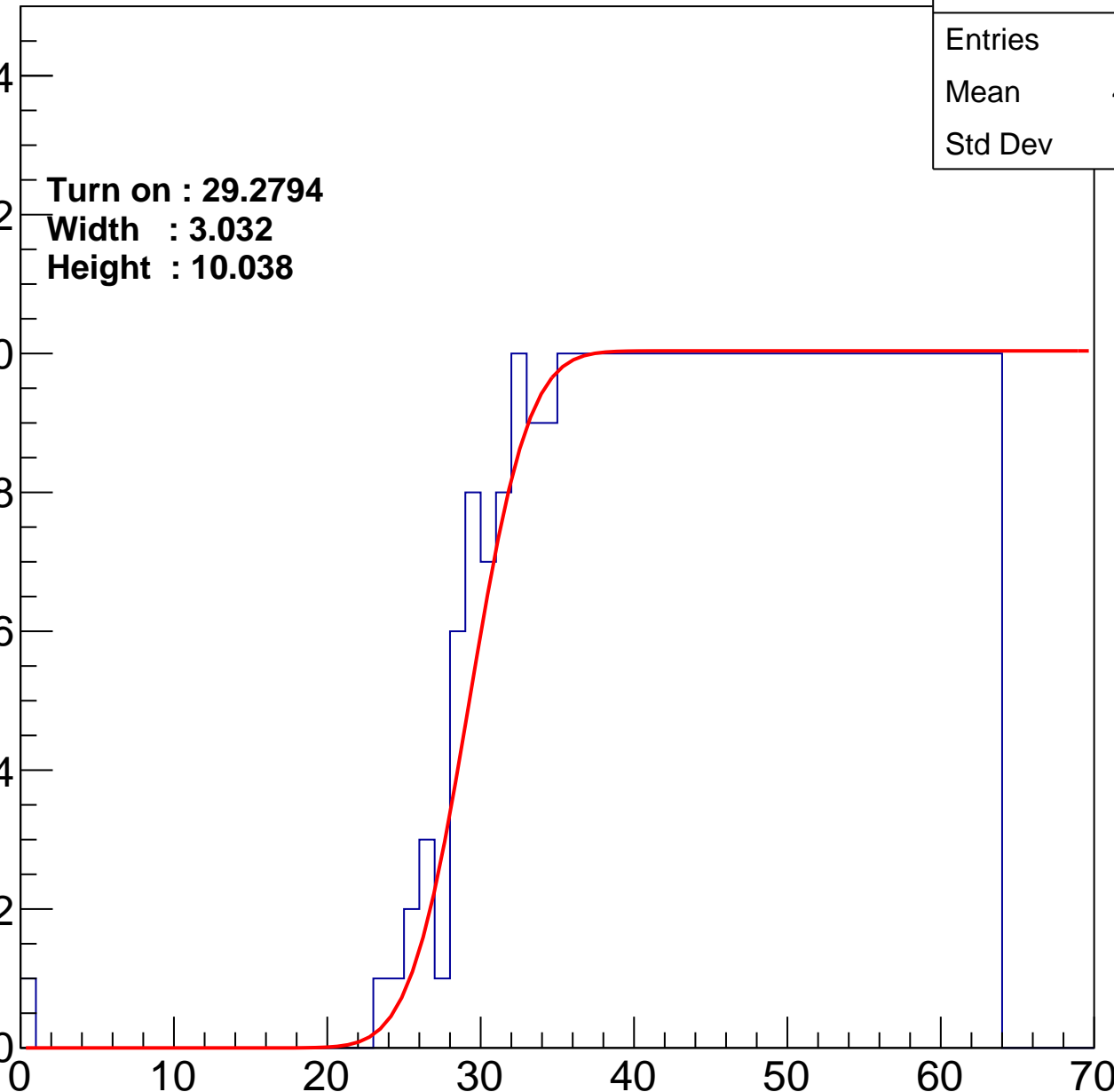
**Width : 3.032**

**Height : 10.038**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch19

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	365
Mean	44.77
Std Dev	11.75

Turn on : 28.4148

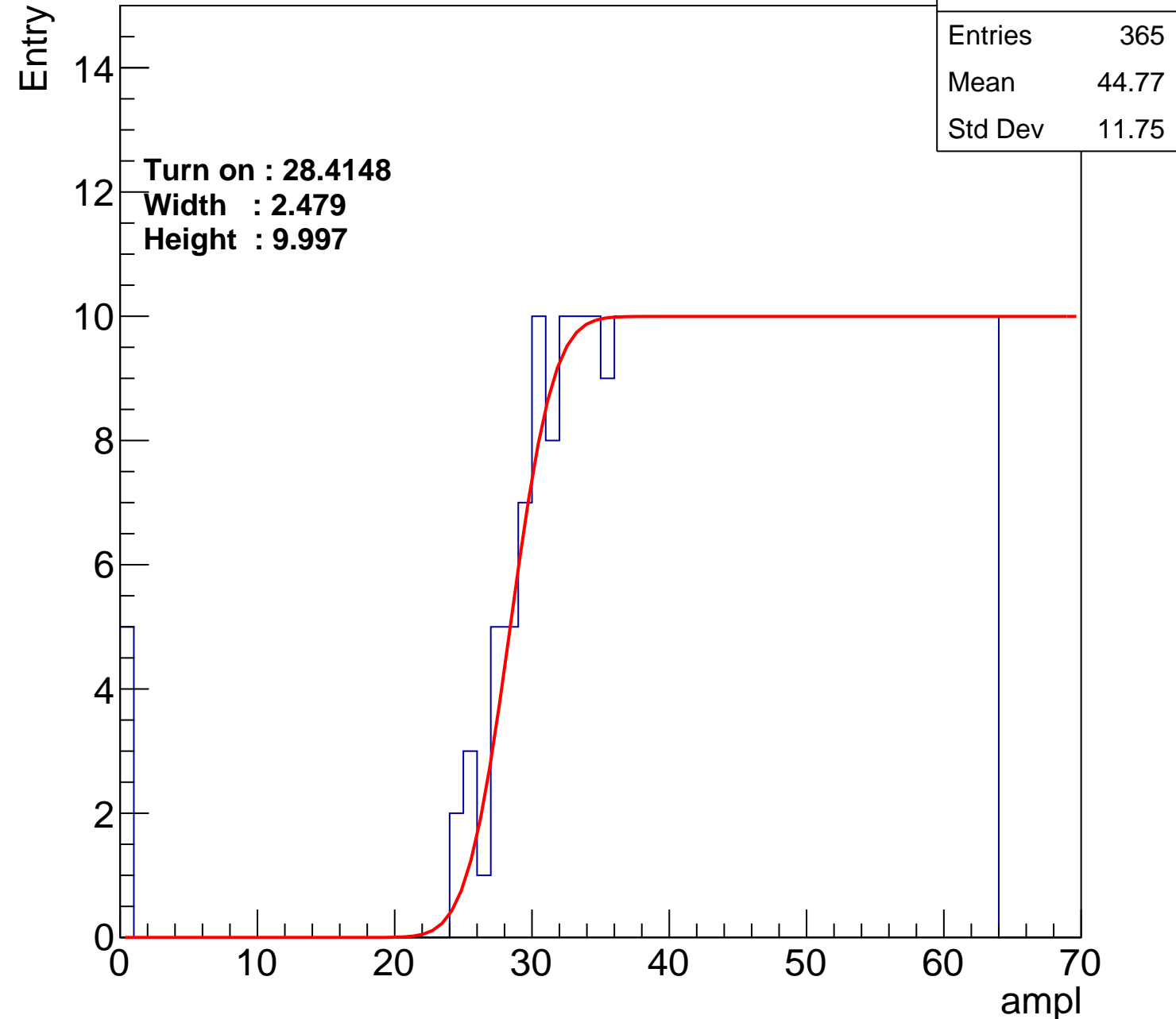
Width : 2.479

Height : 9.997

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch20

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	364
Mean	44.99
Std Dev	11.3

Turn on : 28.3212

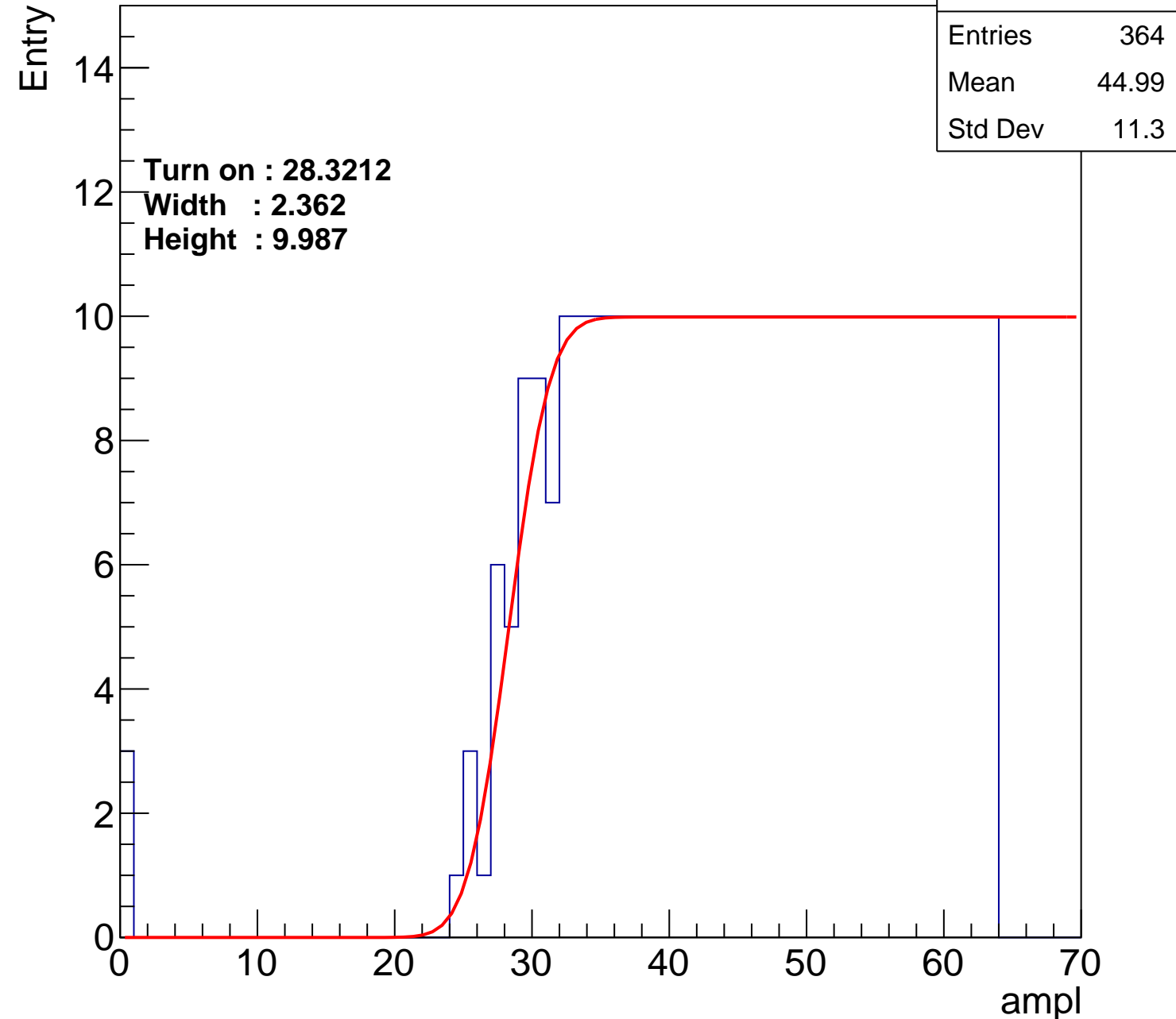
Width : 2.362

Height : 9.987

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch21

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	361
Mean	44.87
Std Dev	11.9

Turn on : 28.7129

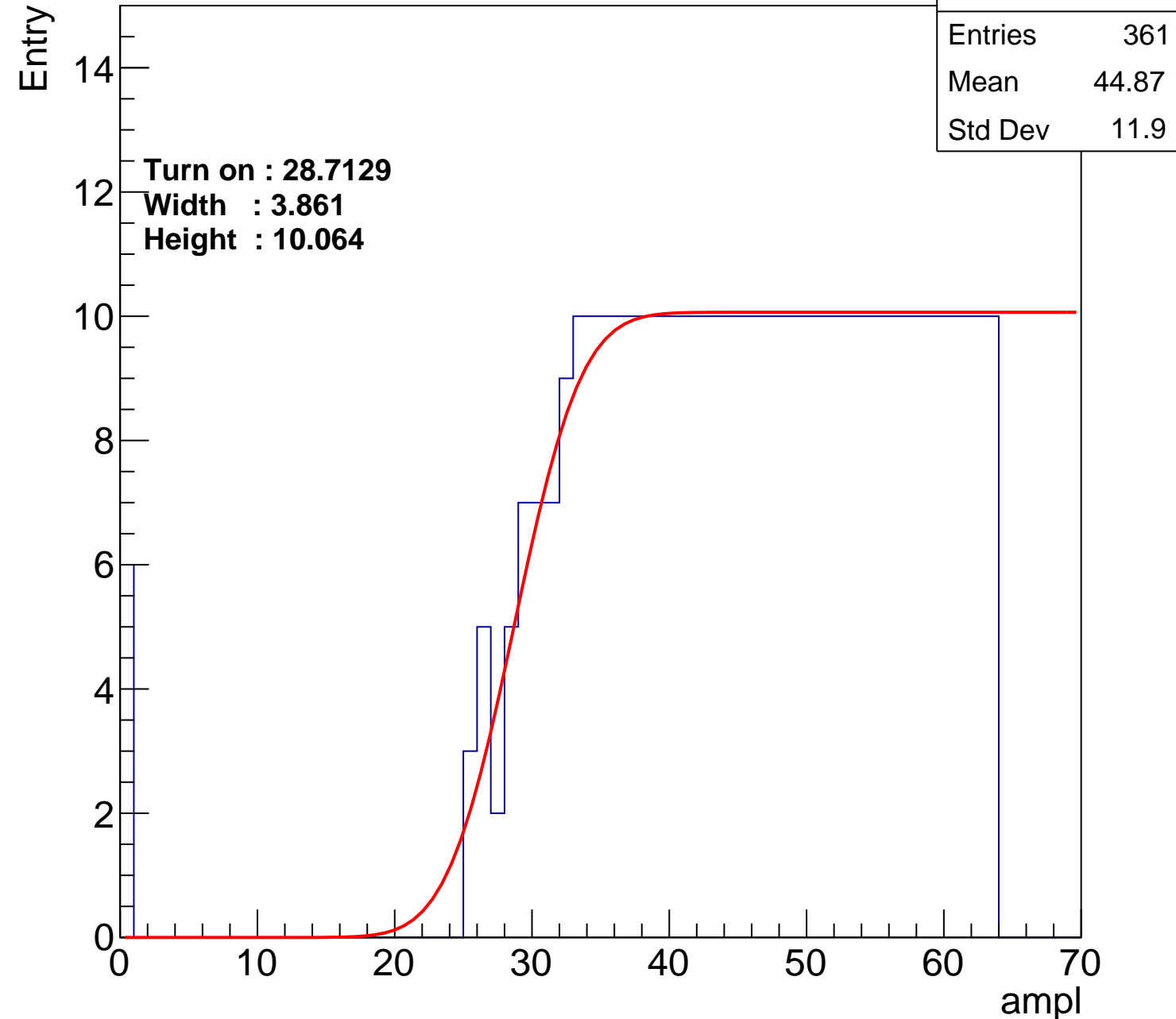
Width : 3.861

Height : 10.064

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch22

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	367
Mean	44.9
Std Dev	11.18

Turn on : 27.2110

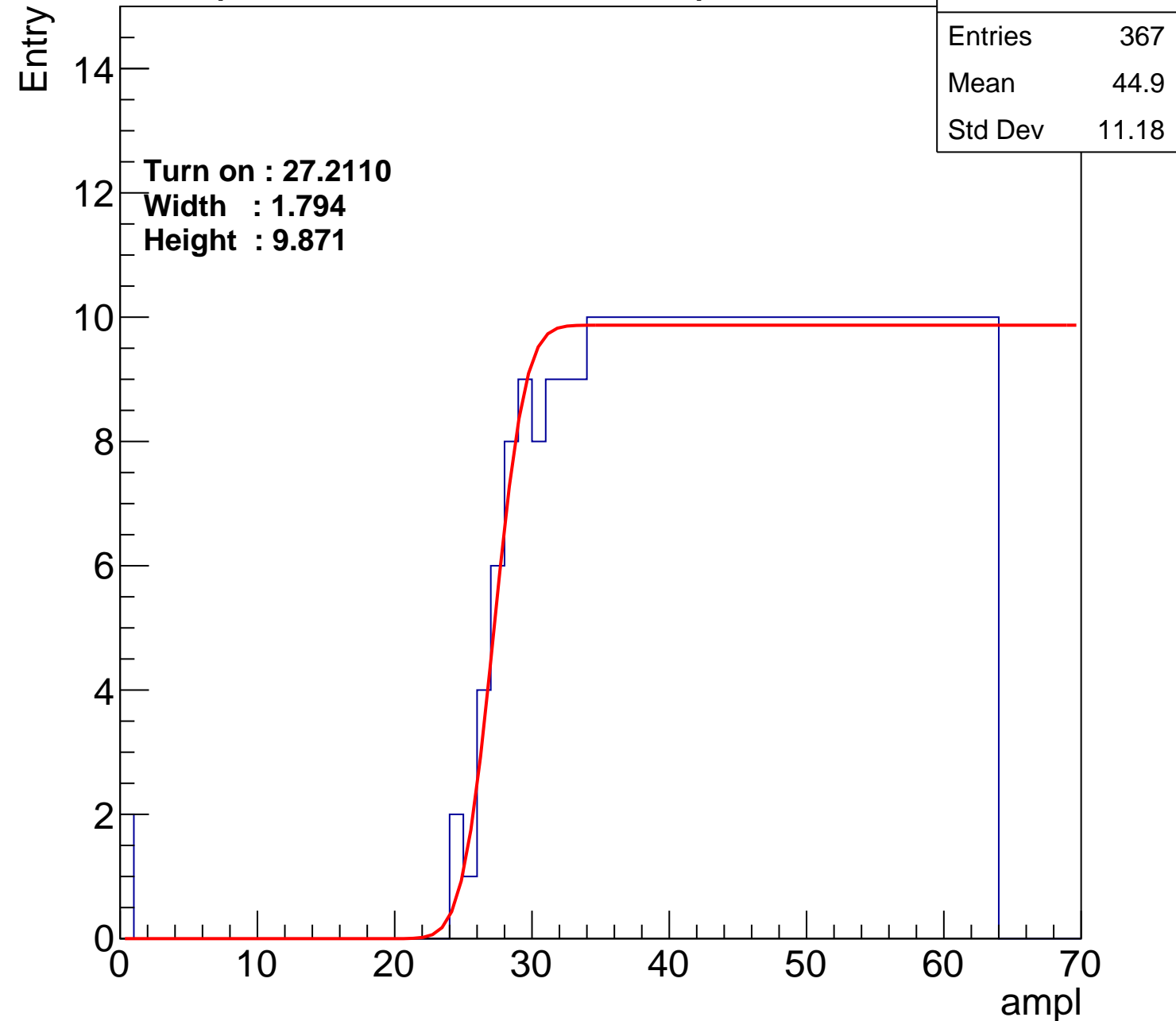
Width : 1.794

Height : 9.871

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U25-ch23

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	365
Mean	44.92
Std Dev	11.26

Turn on : 27.5843

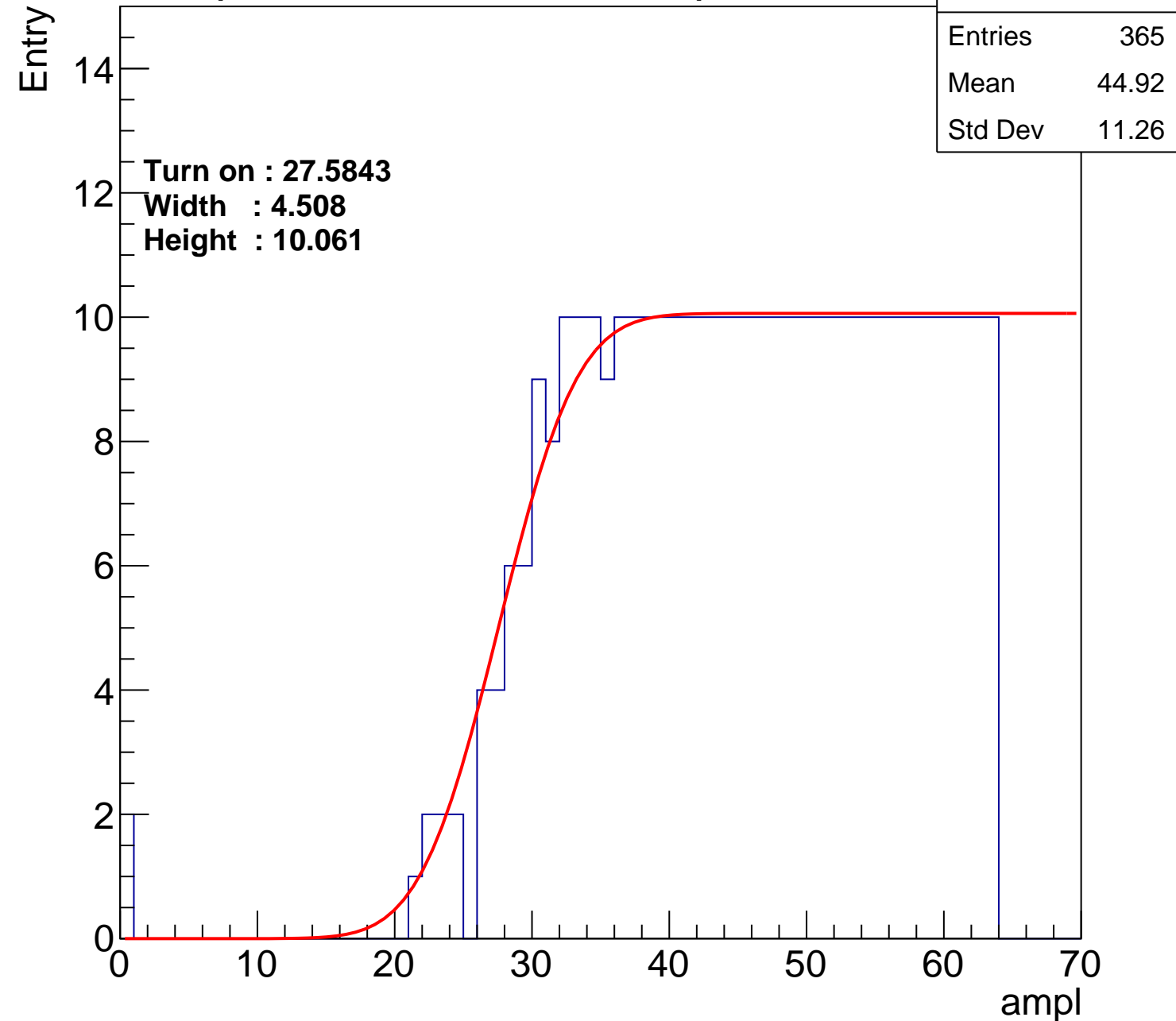
Width : 4.508

Height : 10.061

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch24

calib\_packv5\_042523\_0143.root, FC#9, port A1

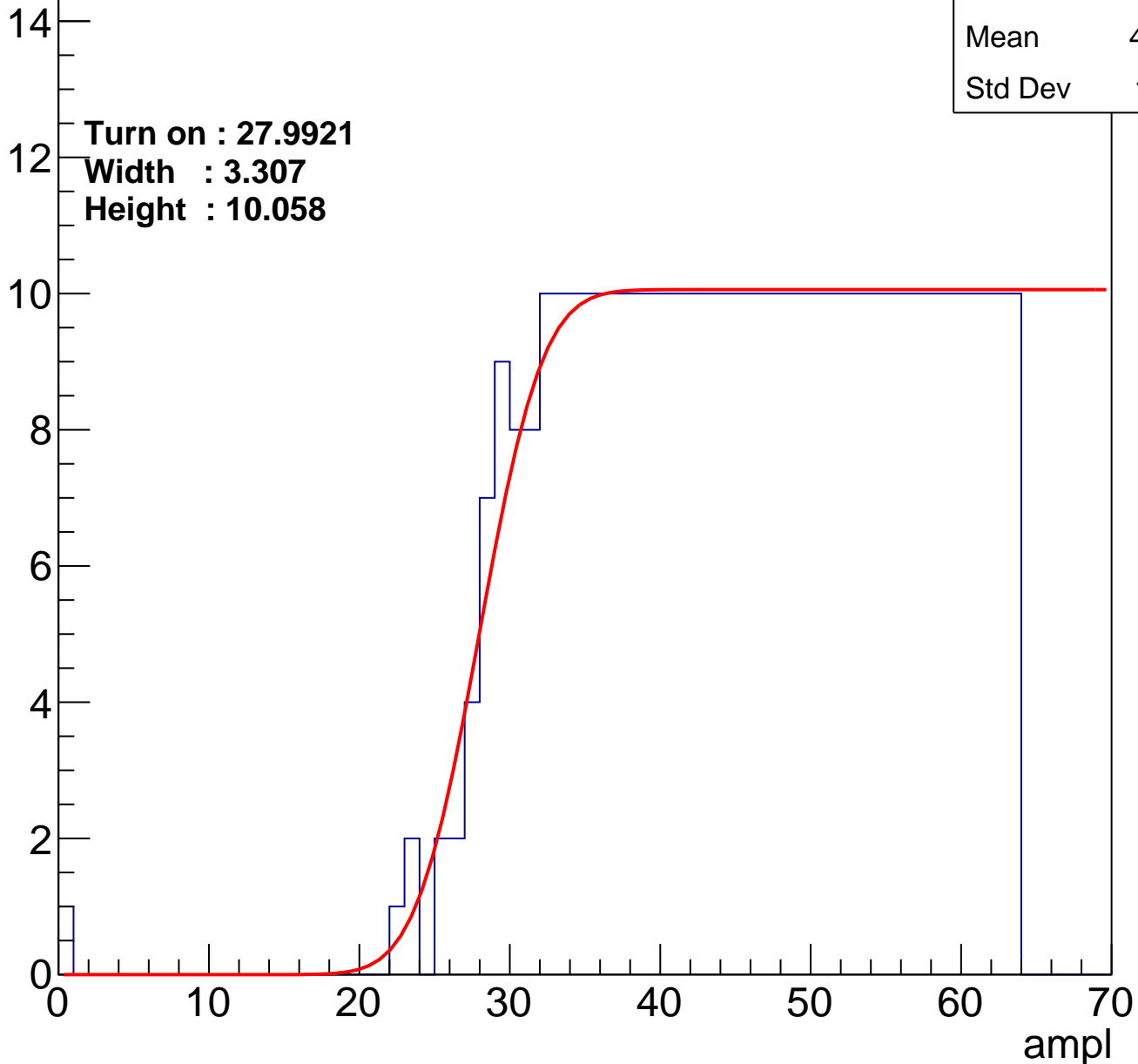
Entries	364
Mean	45.12
Std Dev	10.91

Turn on : 27.9921

Width : 3.307

Height : 10.058

Entry



# B0L001S, U25-ch25

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	364
Mean	45.14
Std Dev	10.86

Turn on : 27.2641

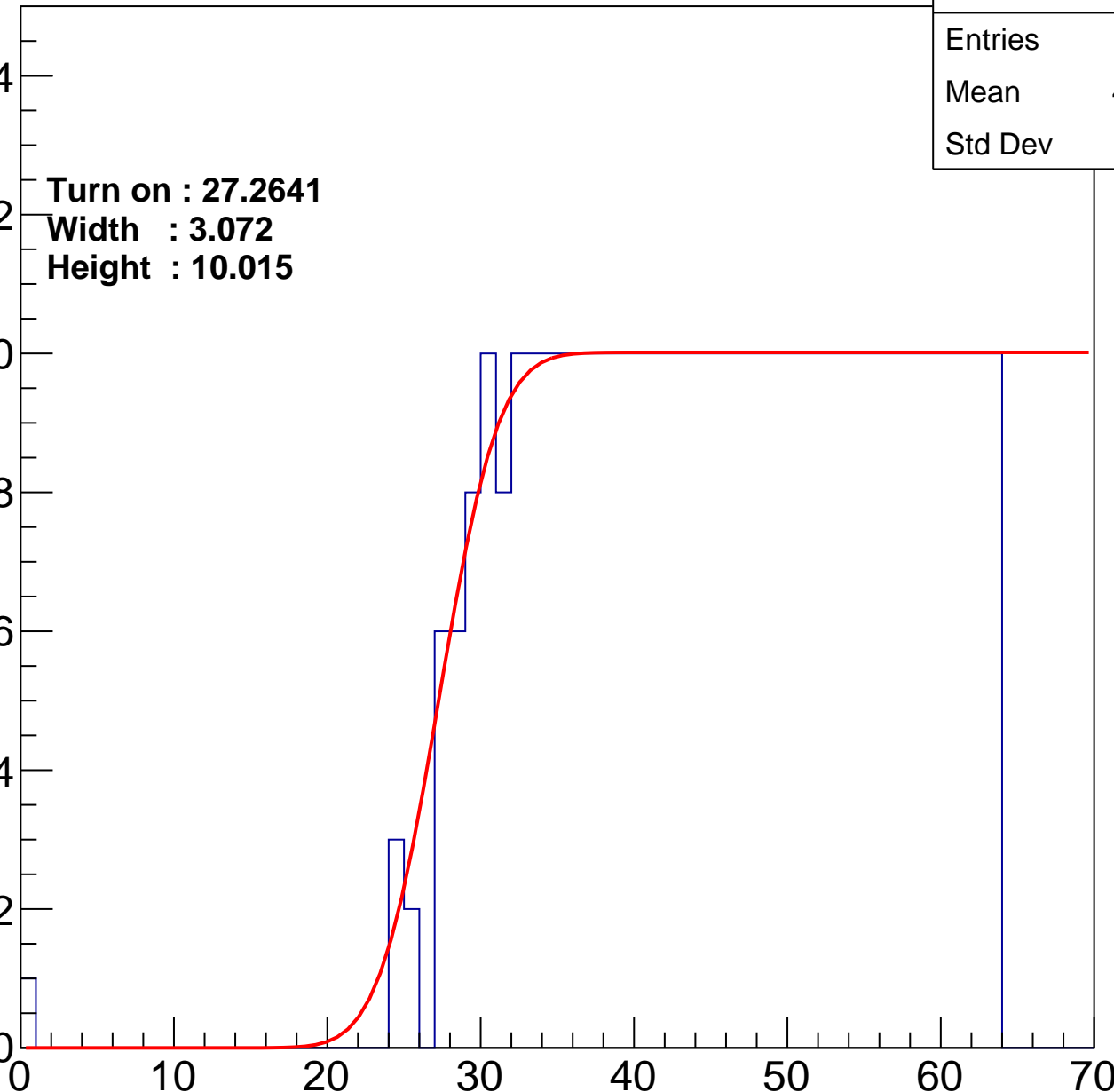
Width : 3.072

Height : 10.015

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

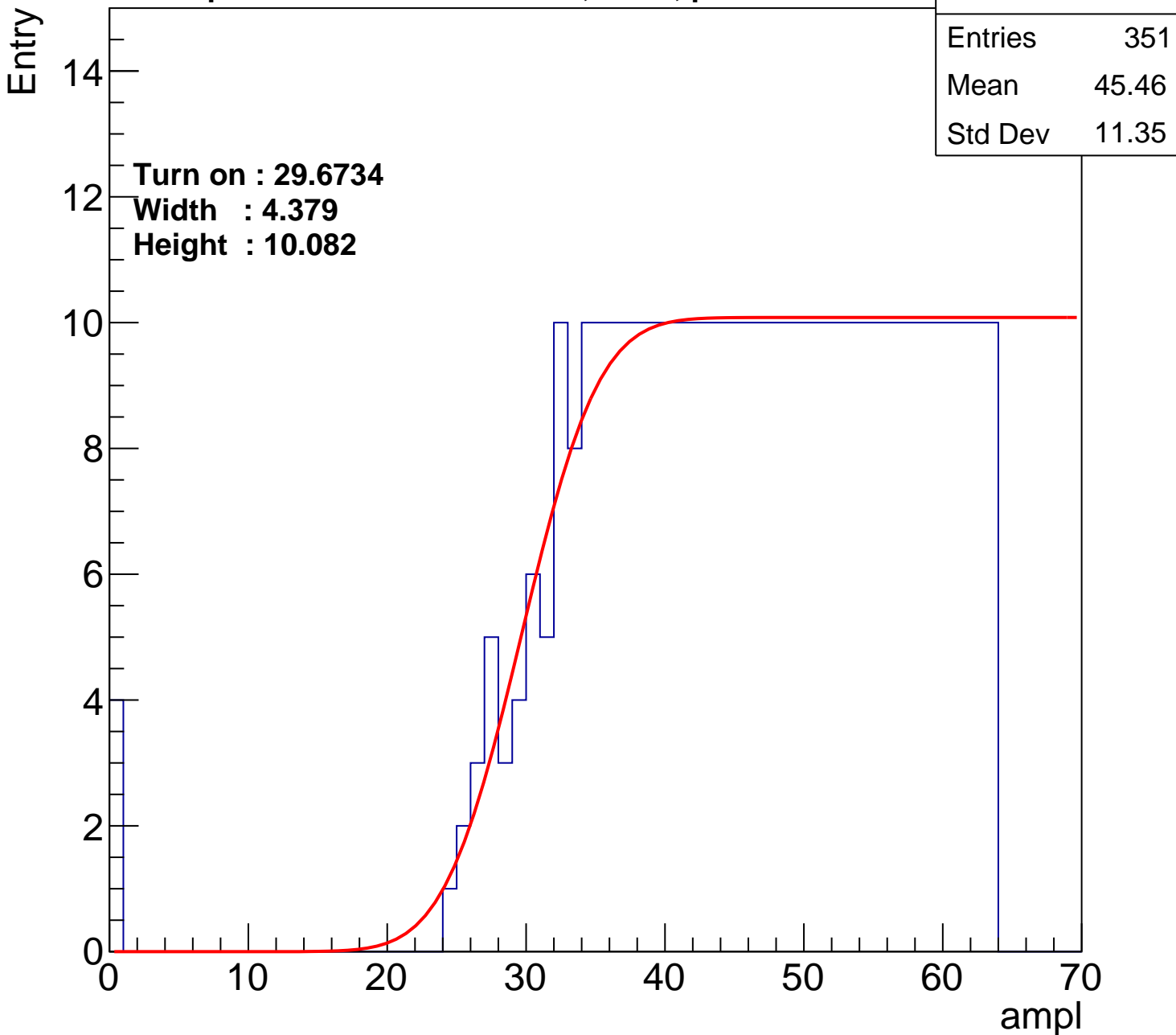


**calib\_packv5\_042523\_0143.root, FC#9, port A1**

**calib\_packv5\_042523\_0143.root, FC#9, port A1**

Entries	351
Mean	45.46
Std Dev	11.35

**Height : 10.082**



# B0L001S, U25-ch27

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	359
Mean	45.28
Std Dev	11.13

Turn on : 28.5979

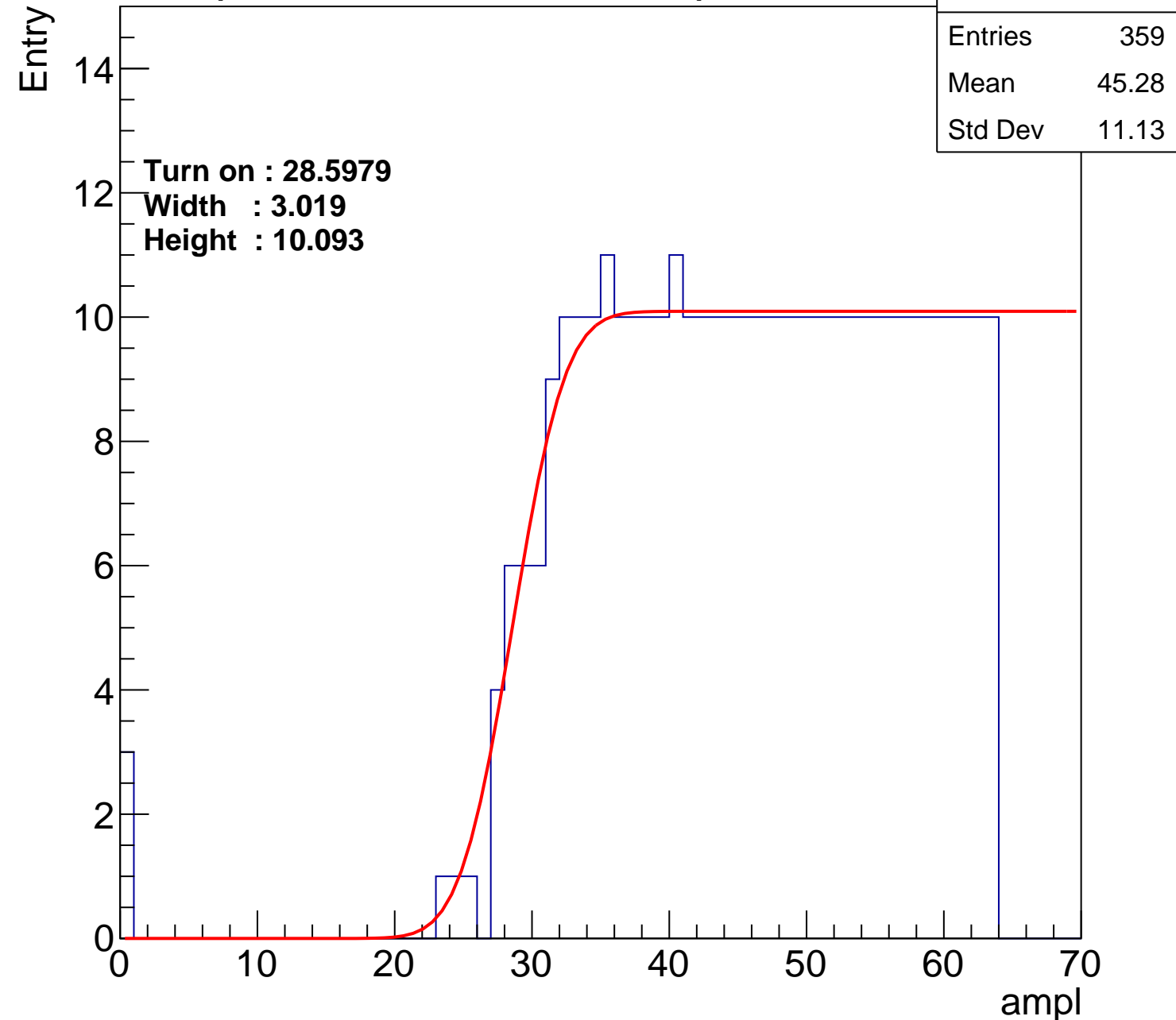
Width : 3.019

Height : 10.093

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch28

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	339
Mean	46.09
Std Dev	11.01

Turn on : 30.8590

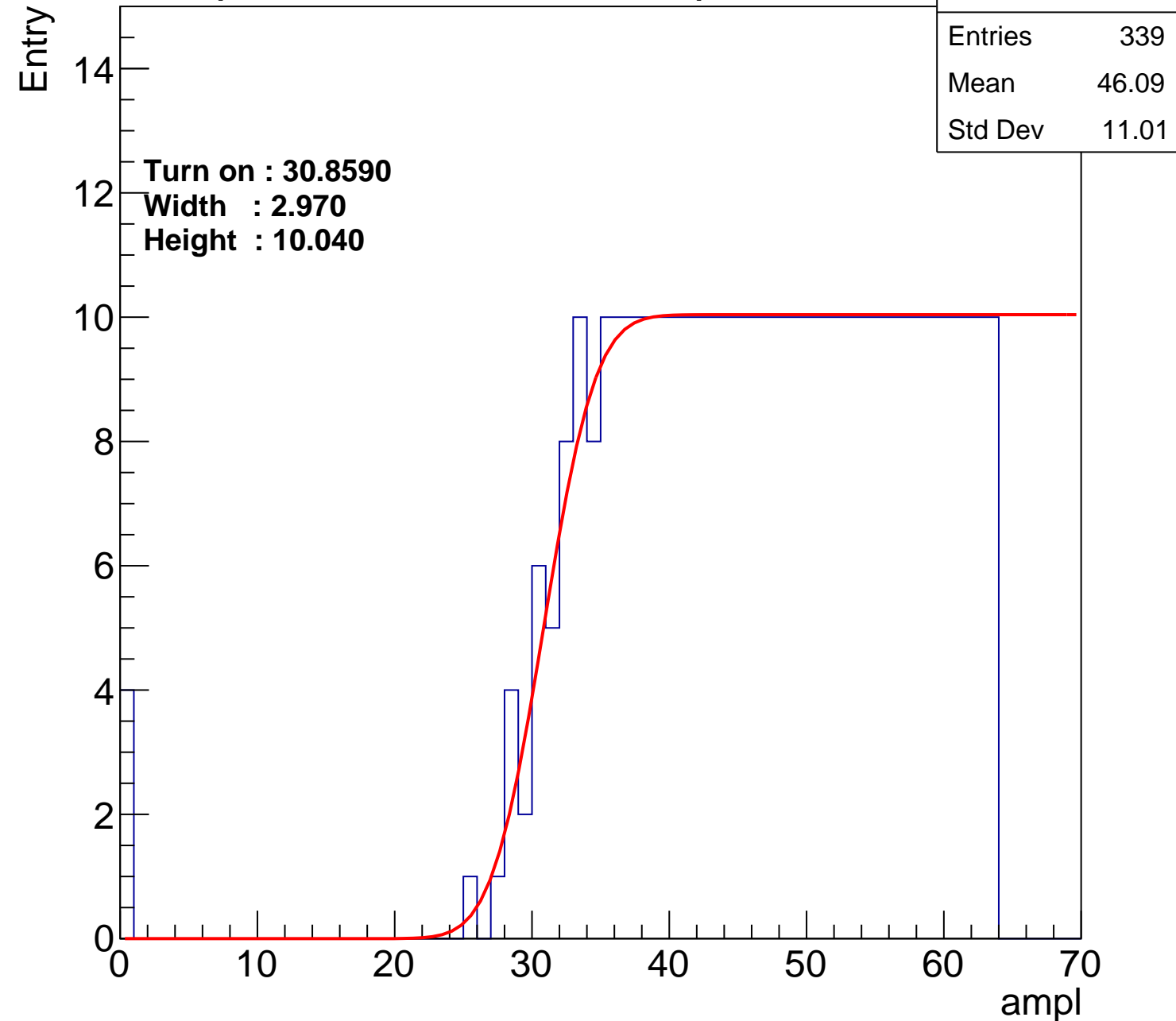
Width : 2.970

Height : 10.040

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch29

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	368
Mean	44.83
Std Dev	11.25

Turn on : 27.8640

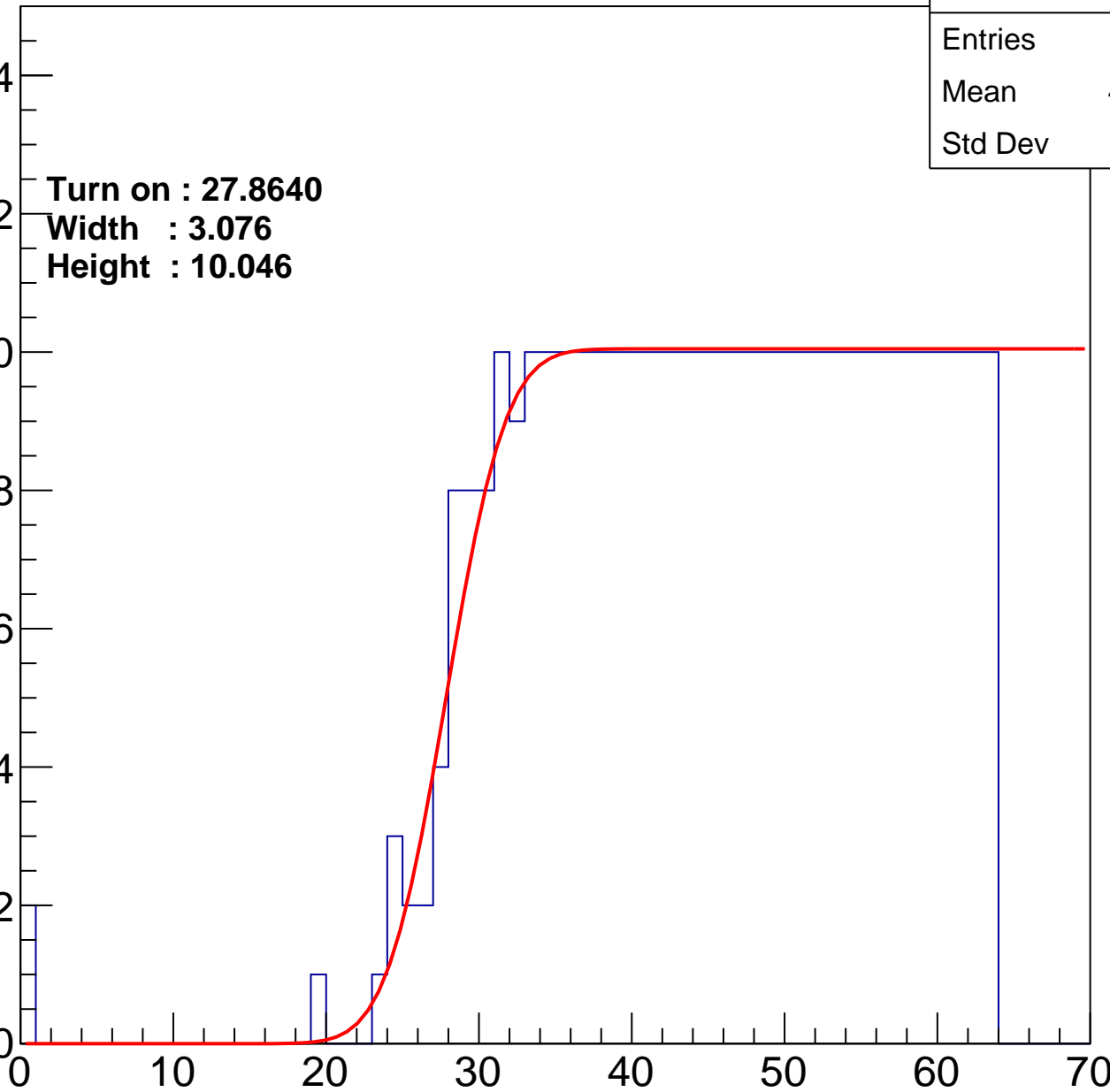
Width : 3.076

Height : 10.046

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch30

calib\_packv5\_042523\_0143.root, FC#9, port A1

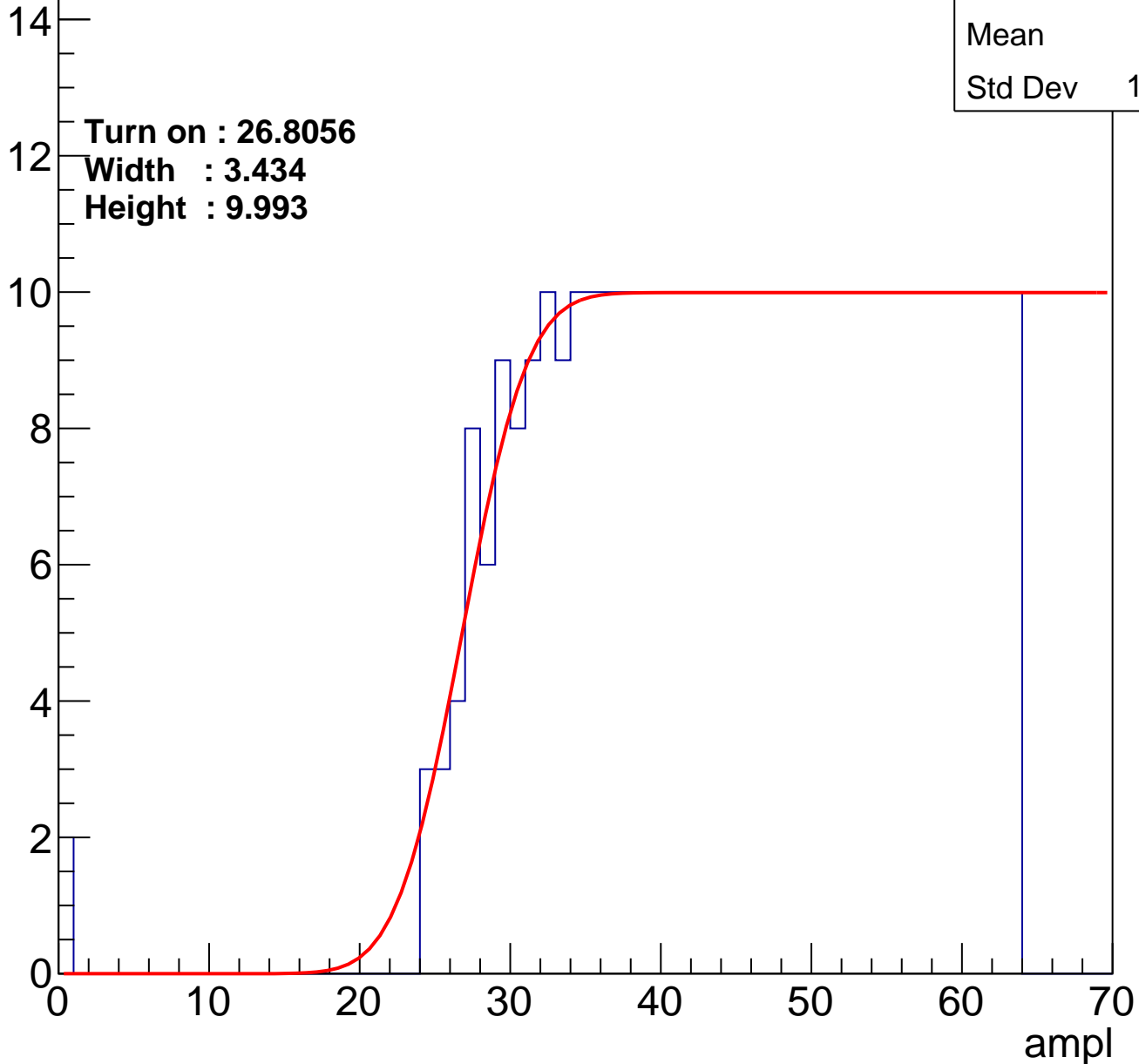
Entries	371
Mean	44.7
Std Dev	11.29

**Turn on : 26.8056**

**Width : 3.434**

**Height : 9.993**

Entry





# B0L001S, U25-ch31

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	354
Mean	45.49
Std Dev	11.05

**Turn on : 29.2985**

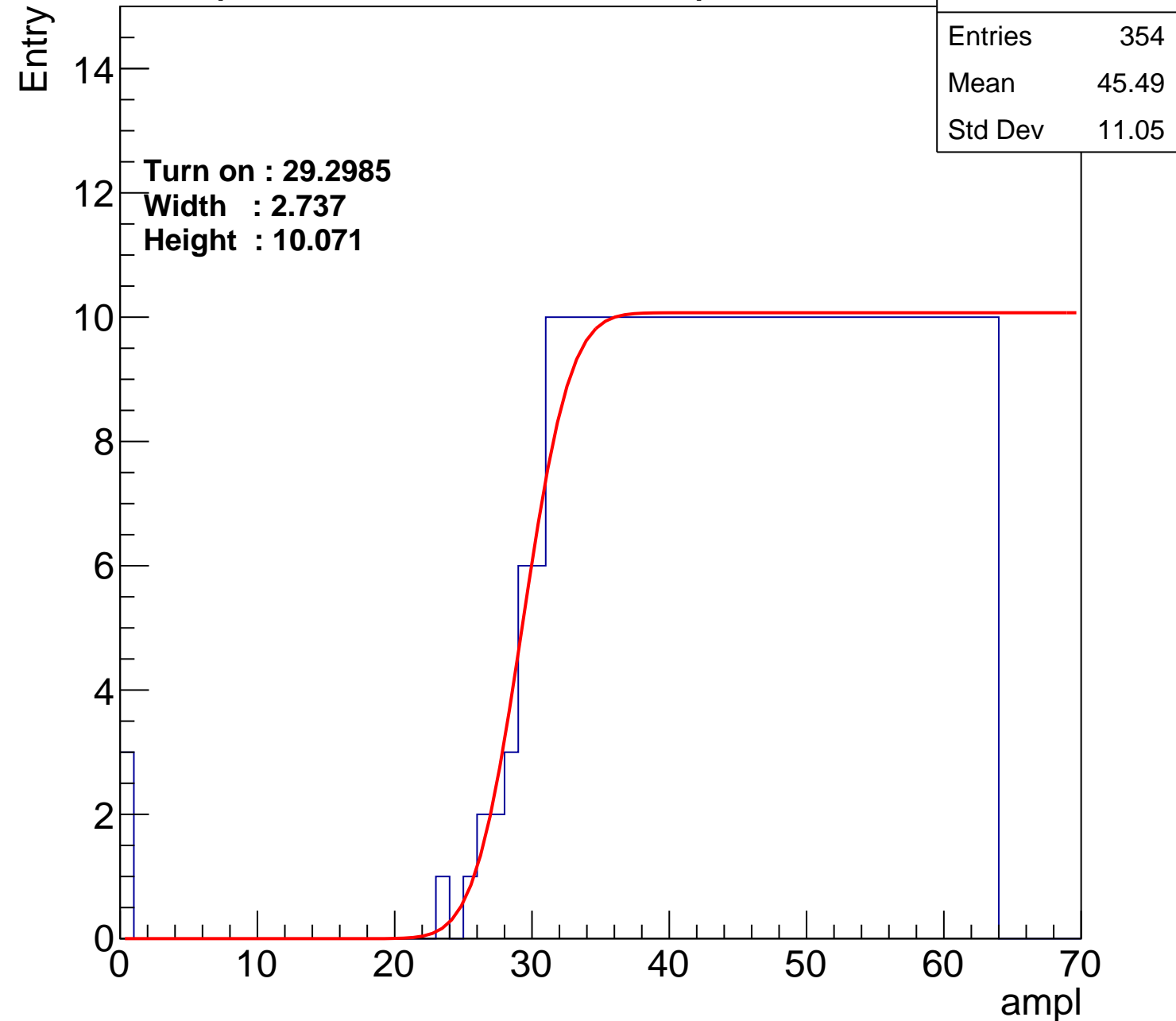
**Width : 2.737**

**Height : 10.071**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch32

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	356
Mean	45.41
Std Dev	10.94

**Turn on : 28.6578**

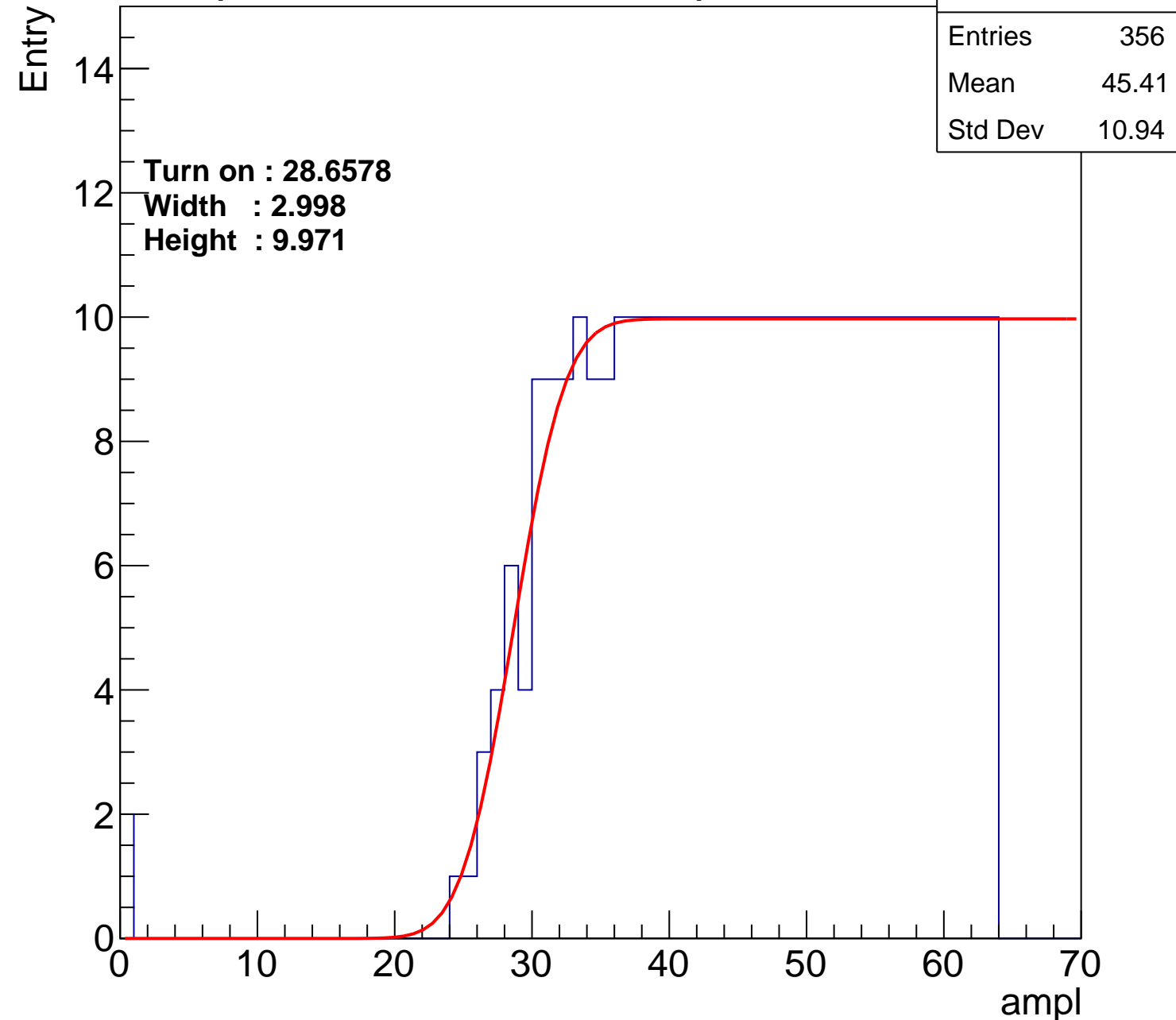
**Width : 2.998**

**Height : 9.971**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch33

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	347
Mean	45.7
Std Dev	11.2

Turn on : 30.4828

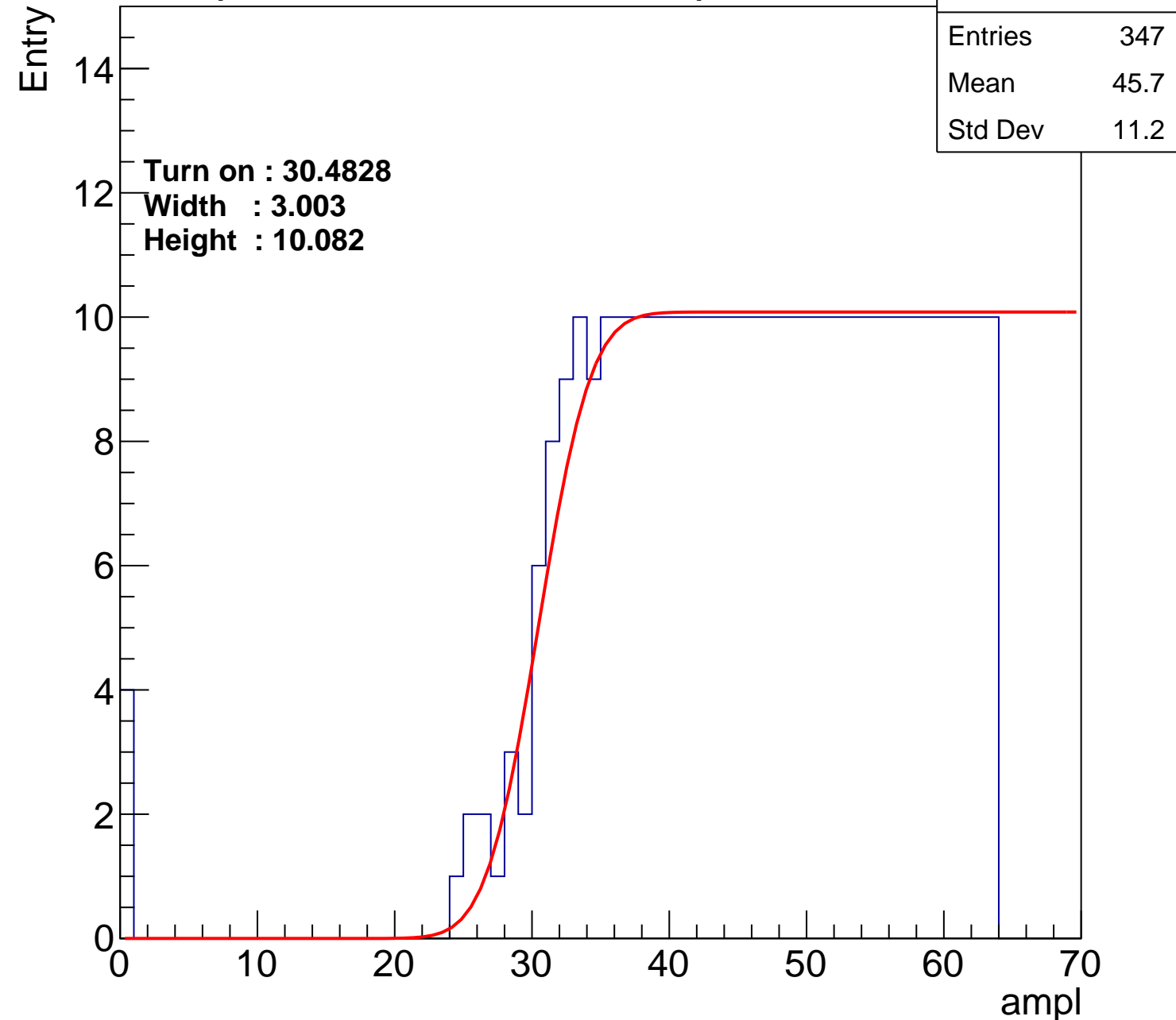
Width : 3.003

Height : 10.082

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch34

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	338
Mean	46.36
Std Dev	10.29

Turn on : 29.9005

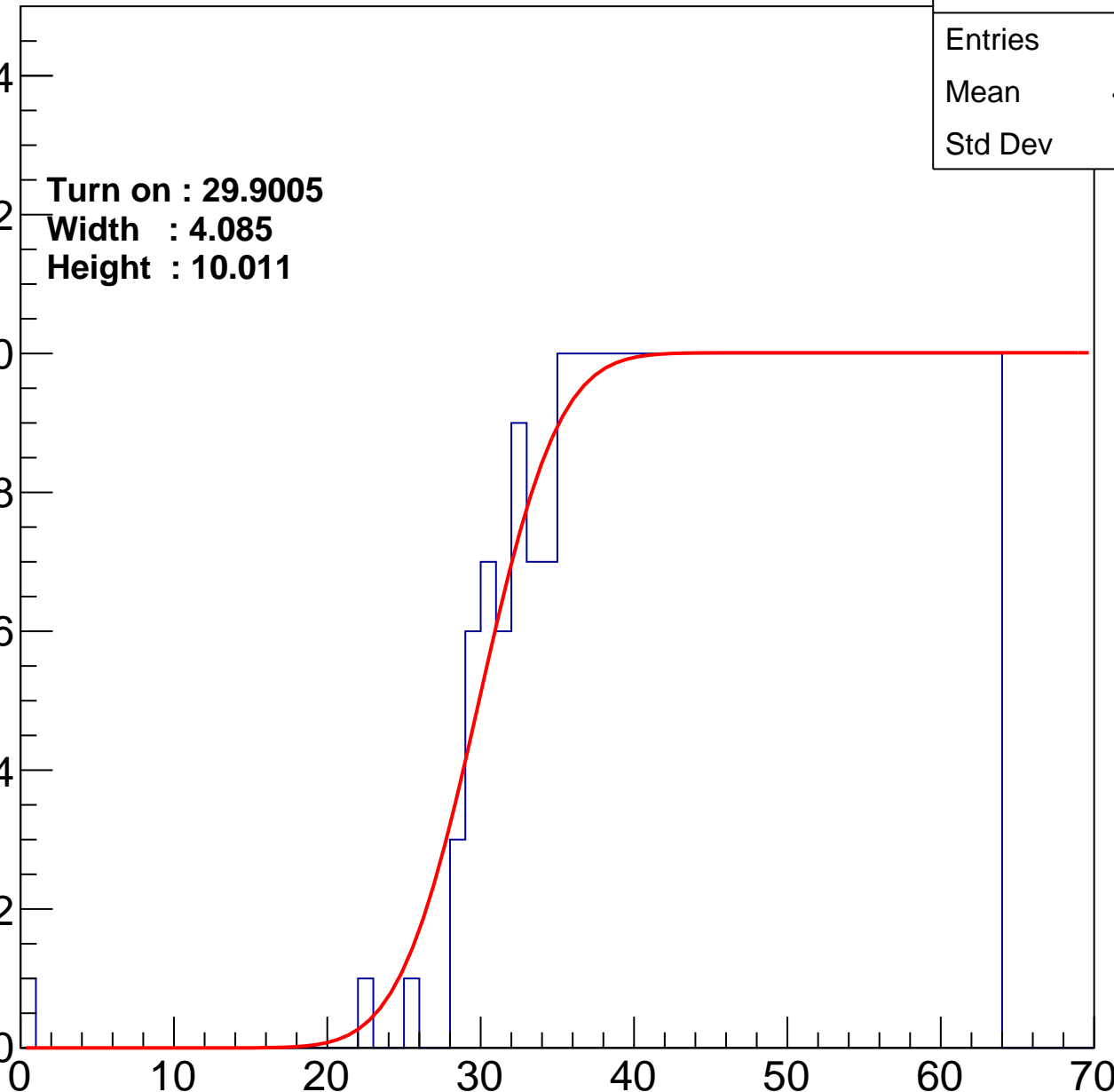
Width : 4.085

Height : 10.011

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch35

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	365
Mean	45.03
Std Dev	11.09

**Turn on : 27.7957**

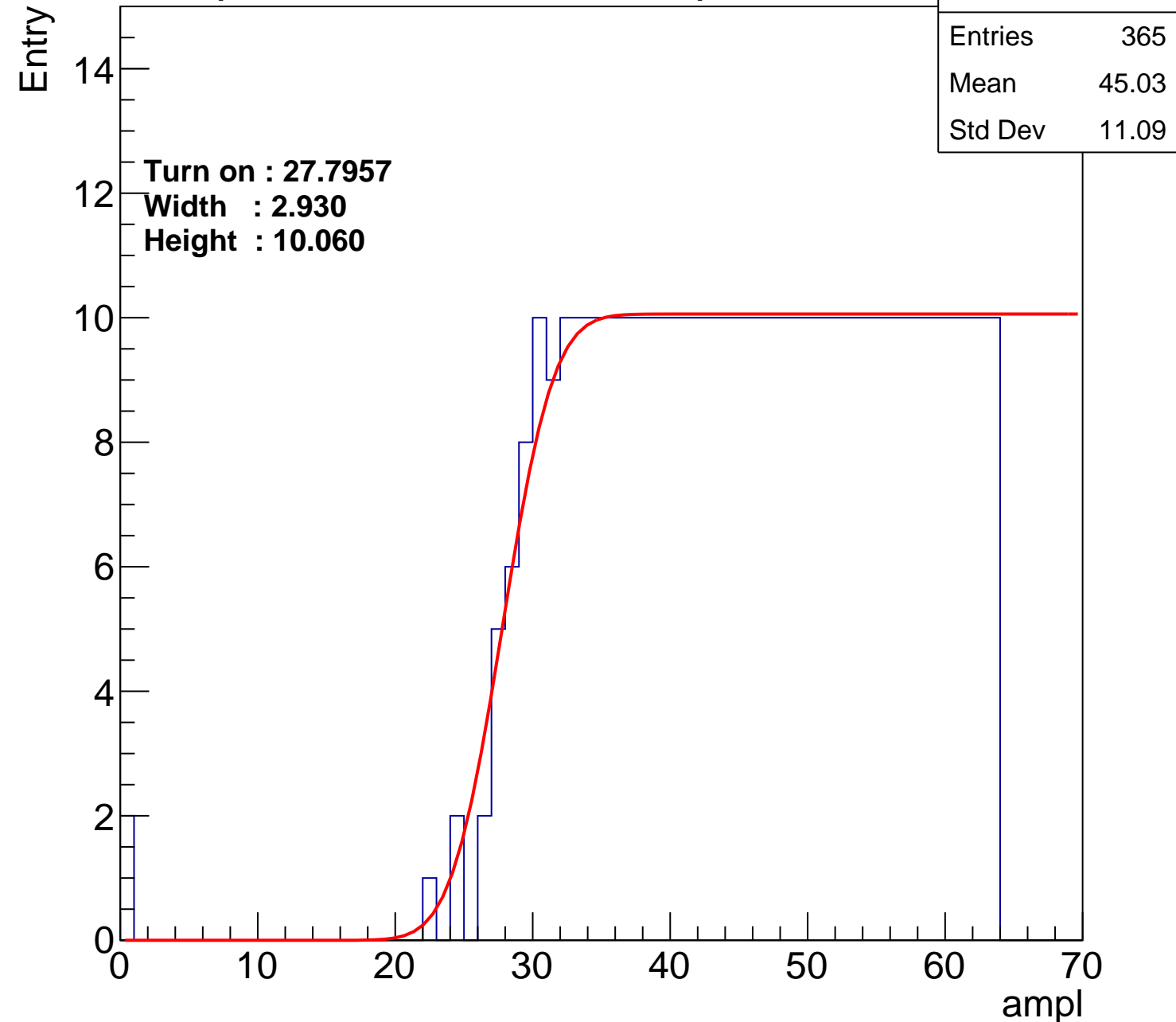
**Width : 2.930**

**Height : 10.060**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch36

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	386
Mean	44.01
Std Dev	11.54

**Turn on : 25.7363**

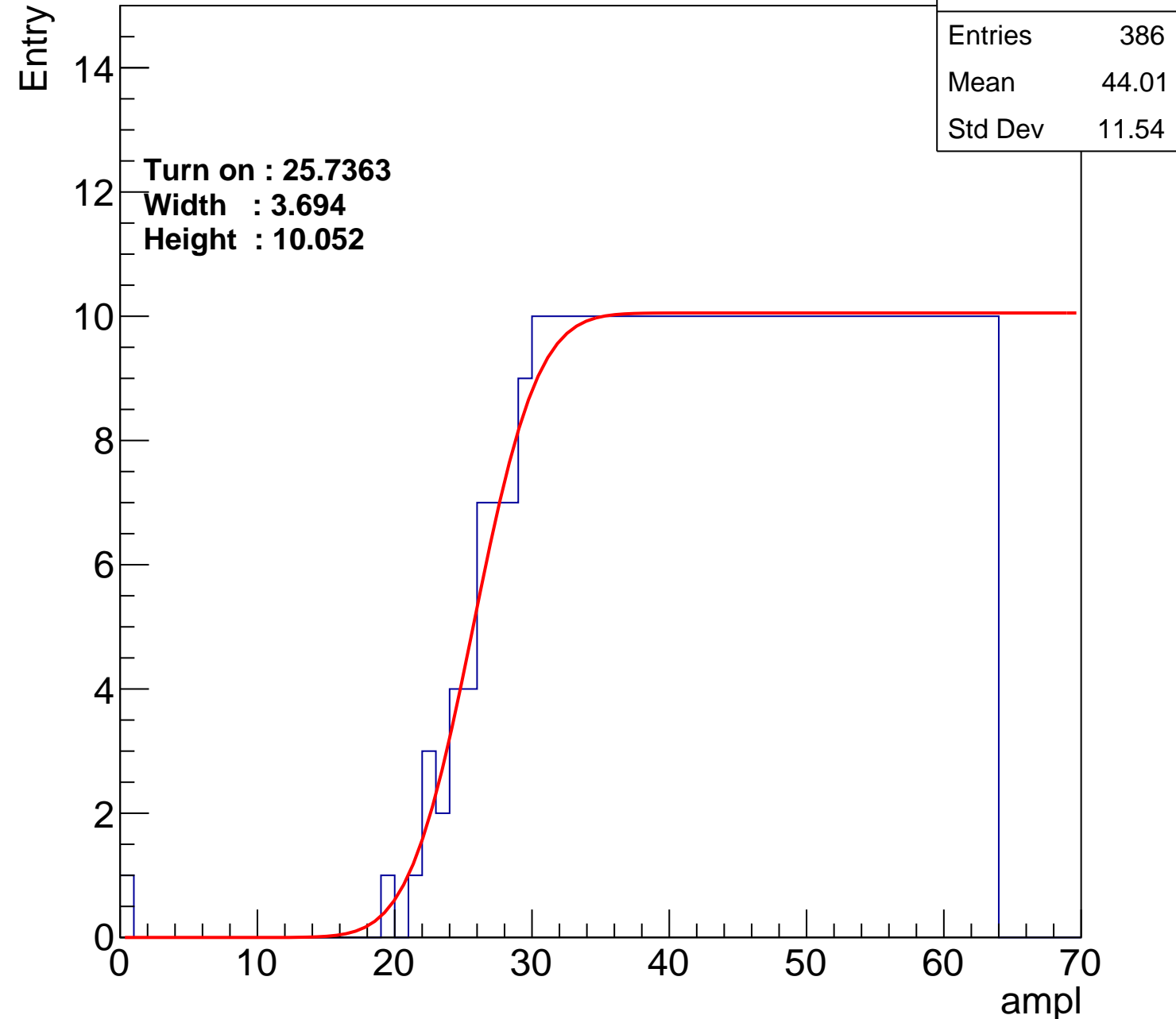
**Width : 3.694**

**Height : 10.052**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch37

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	356
Mean	45.19
Std Dev	11.59

Turn on : 29.4981

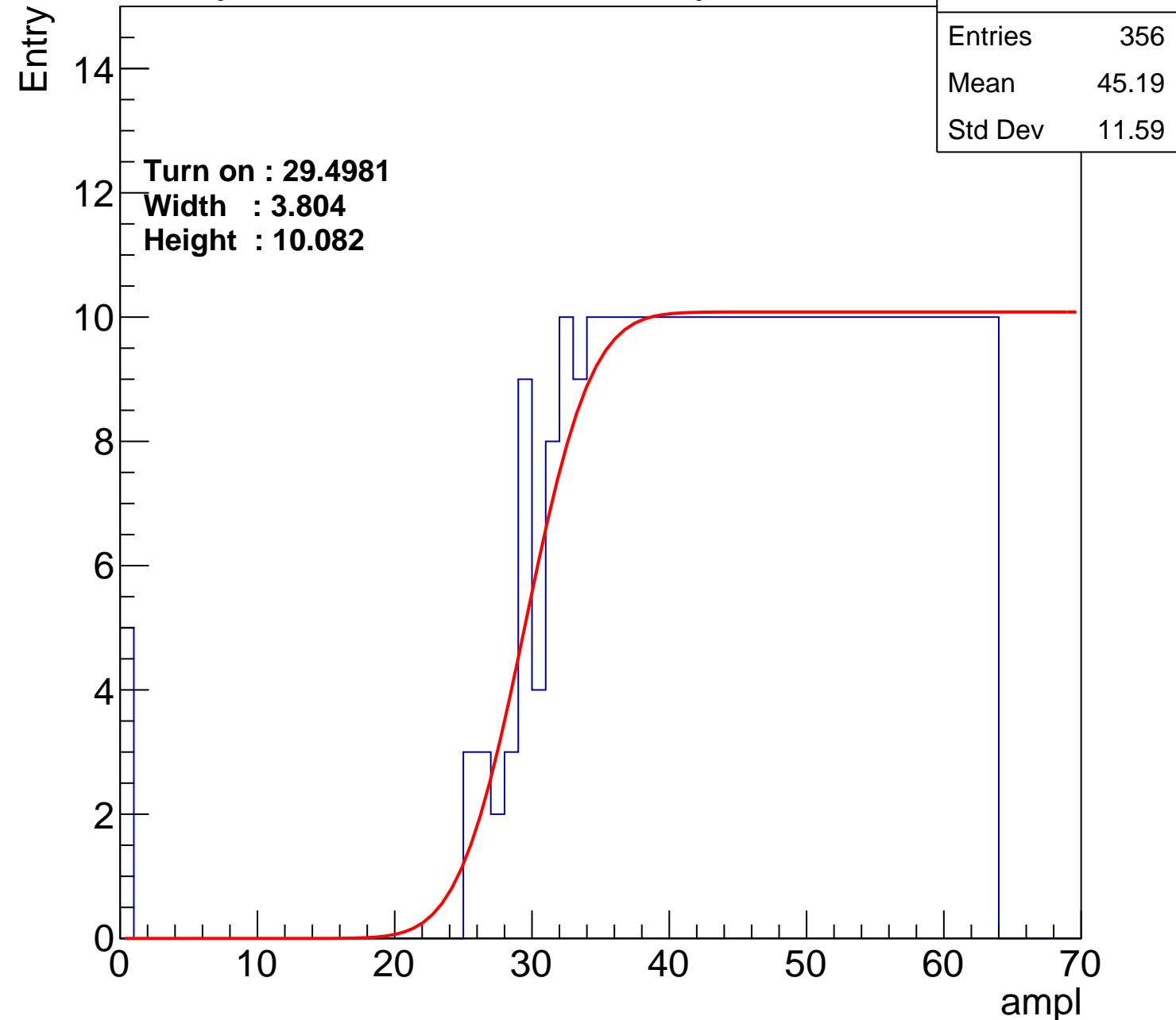
Width : 3.804

Height : 10.082

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch38

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	343
Mean	46.09
Std Dev	10.57

Turn on : 29.8511

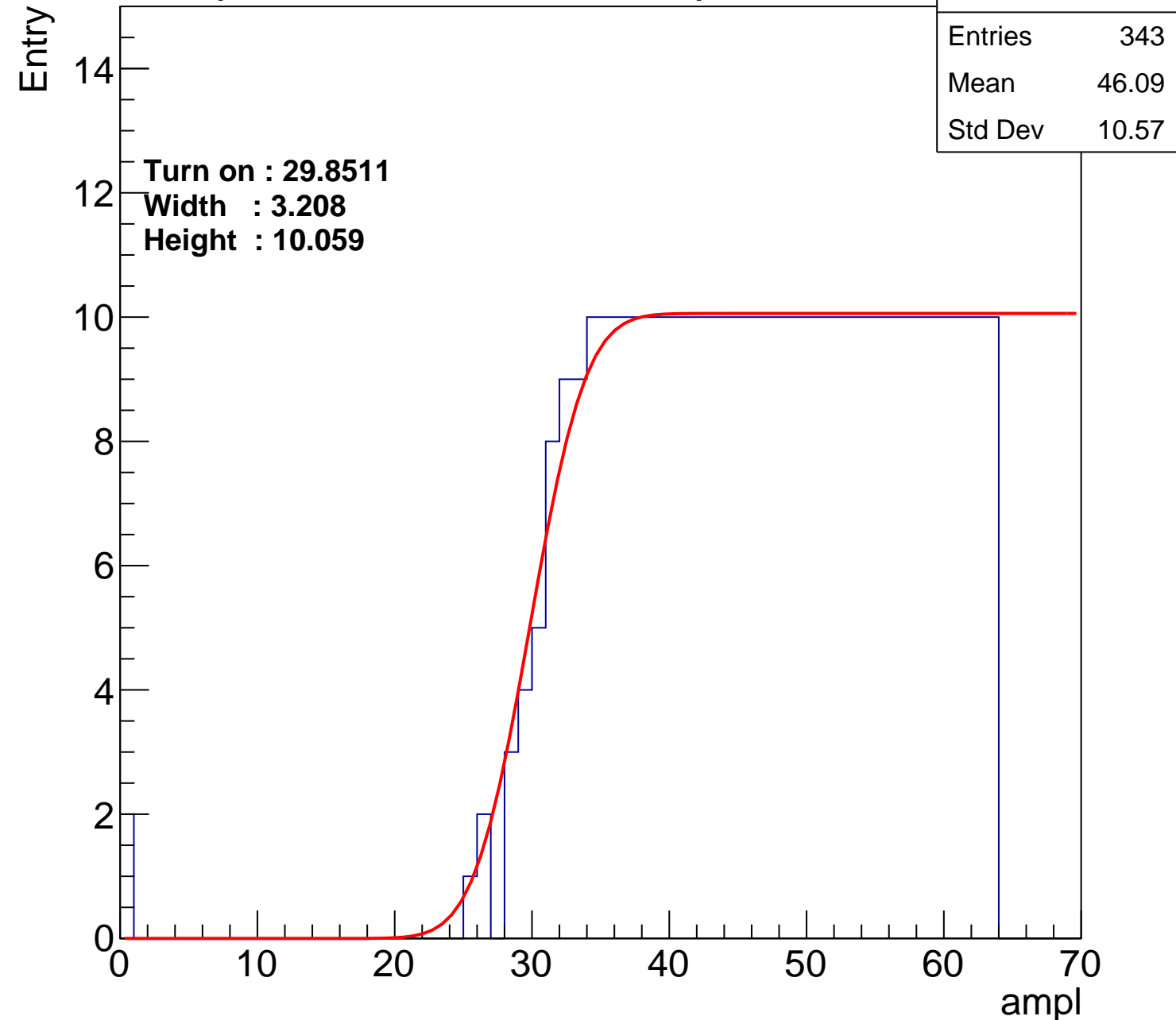
Width : 3.208

Height : 10.059

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U25-ch39

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	343
Mean	45.94
Std Dev	10.92

Turn on : 29.9656

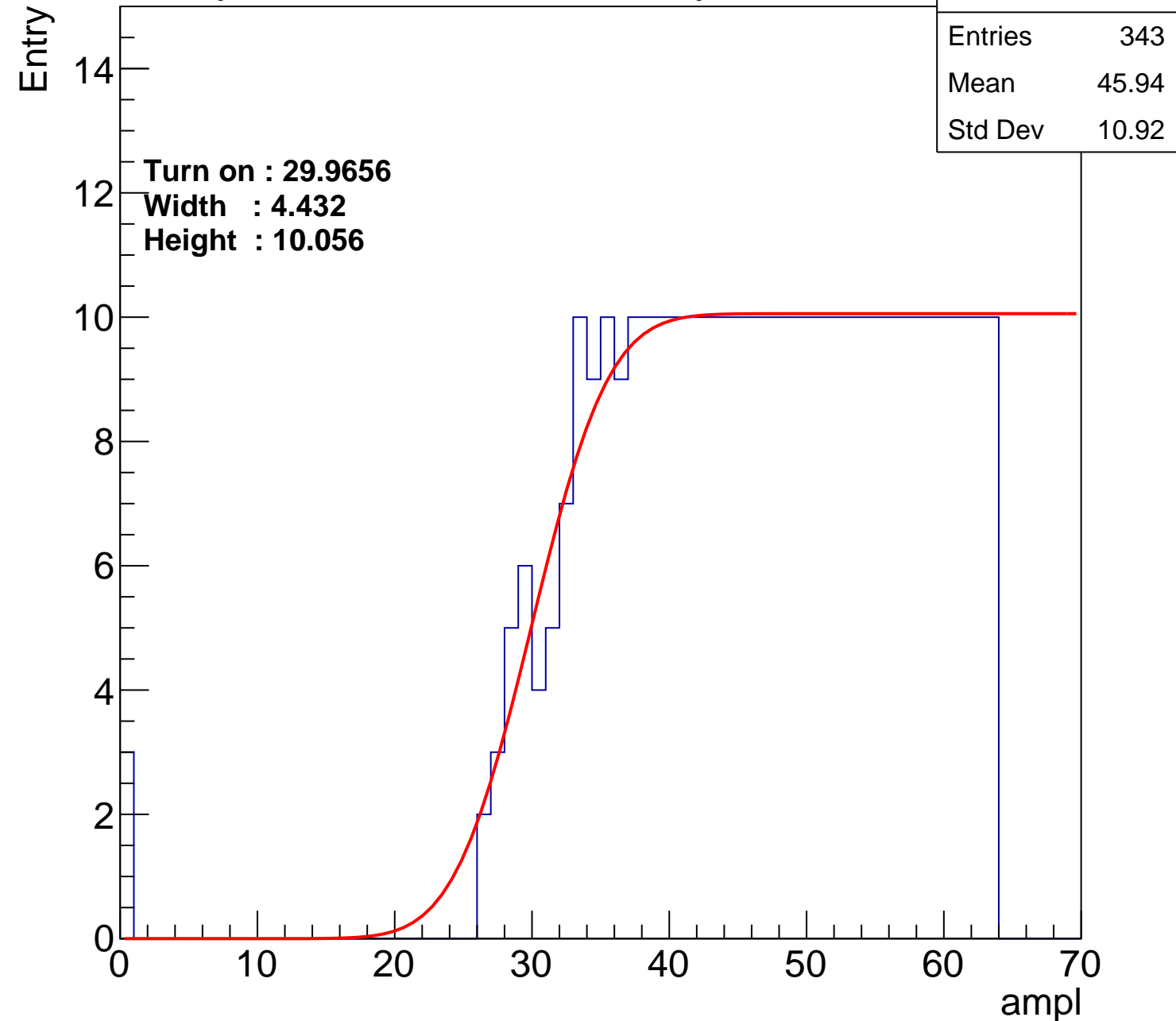
Width : 4.432

Height : 10.056

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch40

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	377
Mean	44.31
Std Dev	11.68

Turn on : 27.1855

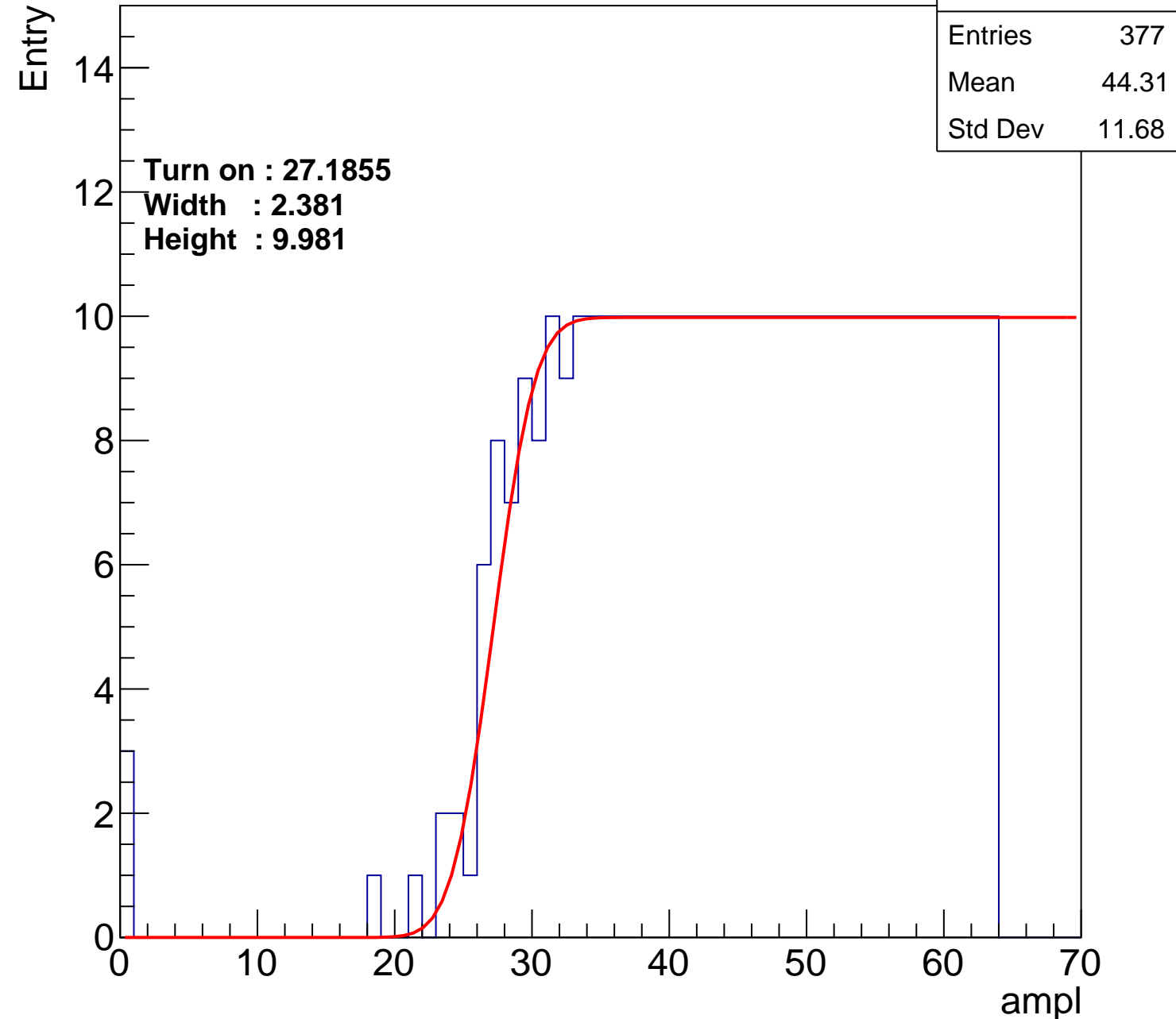
Width : 2.381

Height : 9.981

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch41

**calib\_packv5\_042523\_0143.root, FC#9, port A1**

Entries	348
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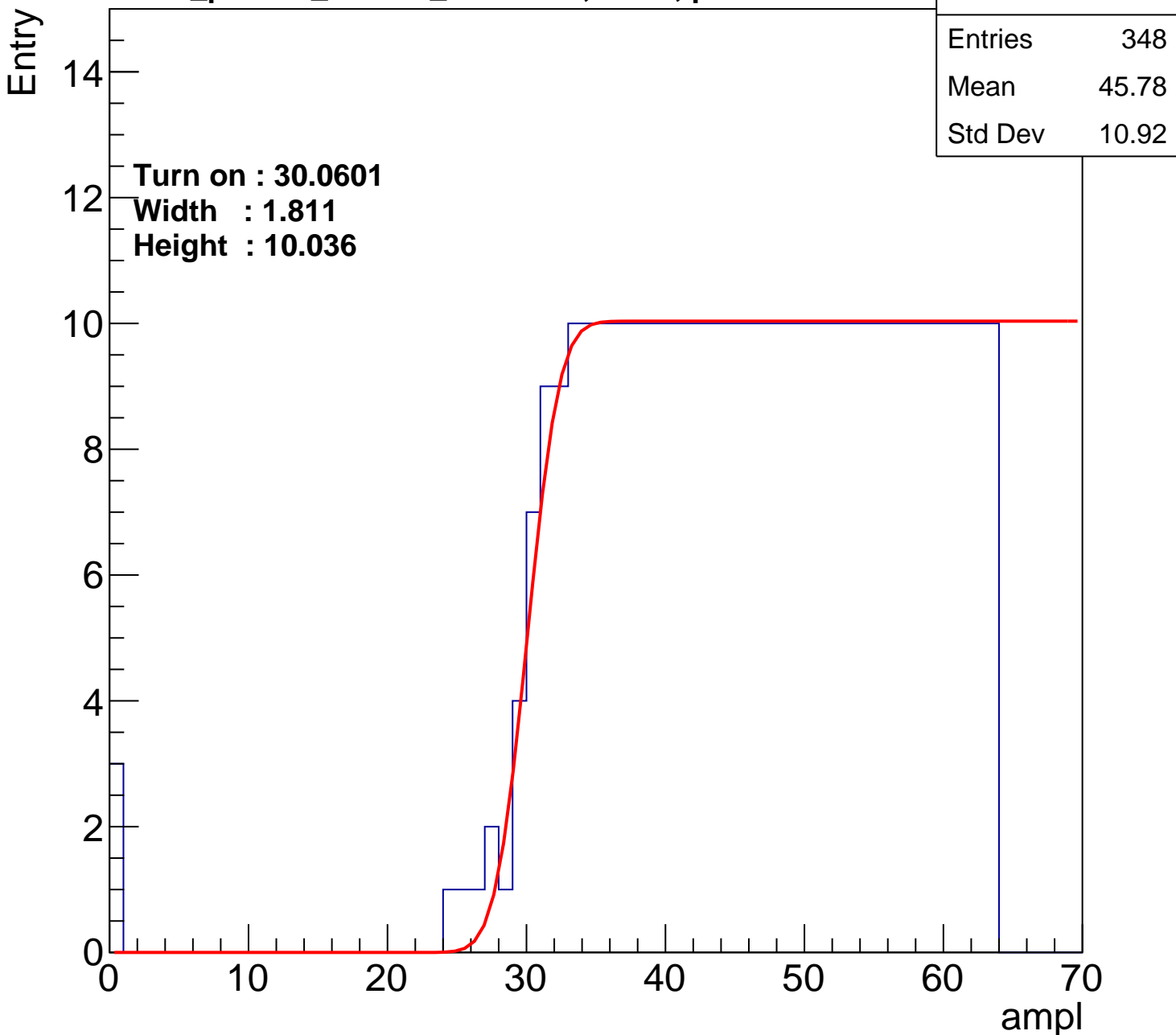
Mean	45.78
------	-------

Std Dev	10.92
---------	-------

**Turn on : 30.0601**

**Width : 1.811**

**Height : 10.036**



# B0L001S, U25-ch42

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	362
Mean	45.19
Std Dev	10.99

**Turn on : 27.9958**

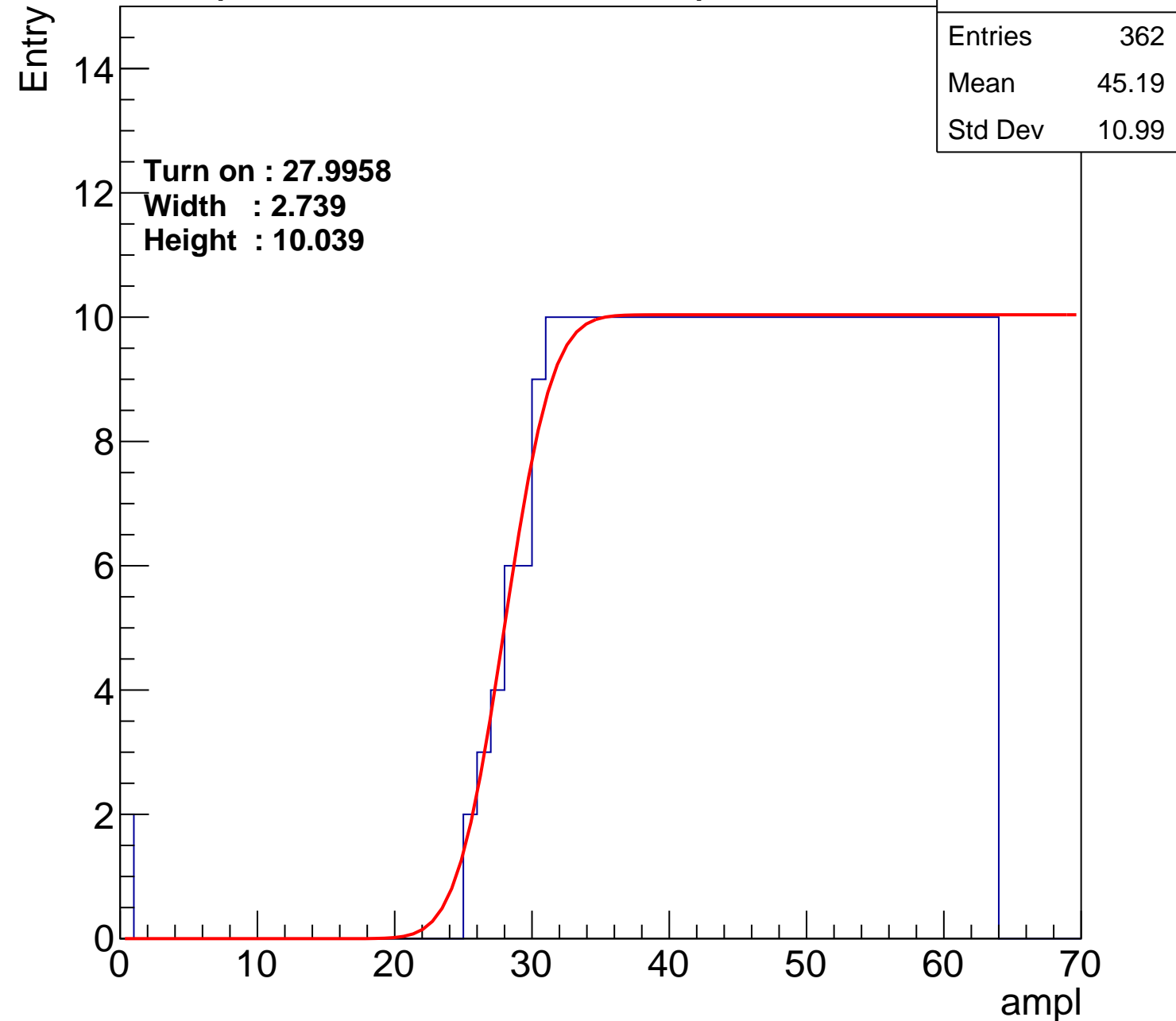
**Width : 2.739**

**Height : 10.039**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch43

calib\_packv5\_042523\_0143.root, FC#9, port A1

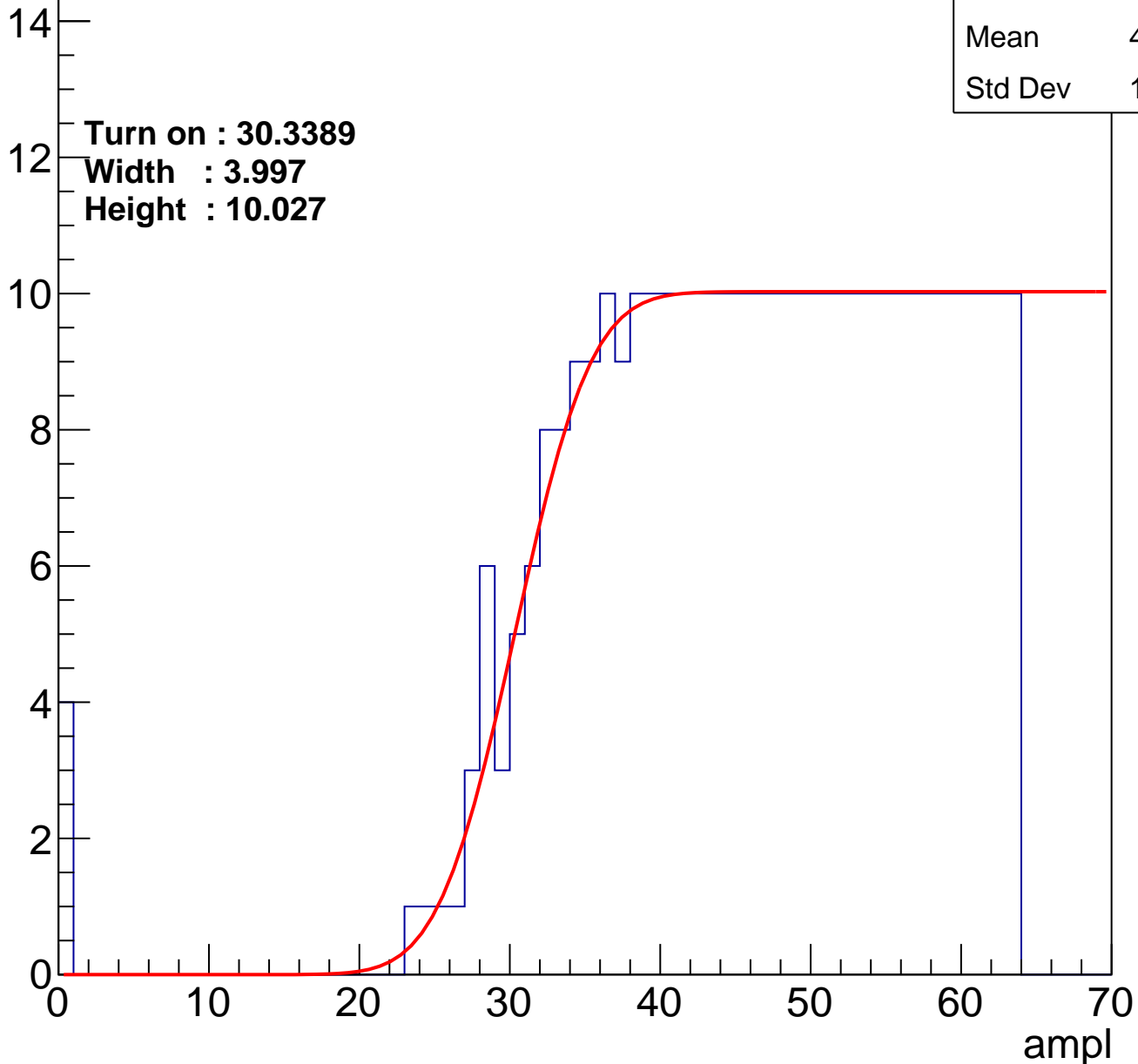
Entries	344
Mean	45.74
Std Dev	11.28

Turn on : 30.3389

Width : 3.997

Height : 10.027

Entry



**calib\_packv5\_042523\_0143.root, FC#9, port A1**

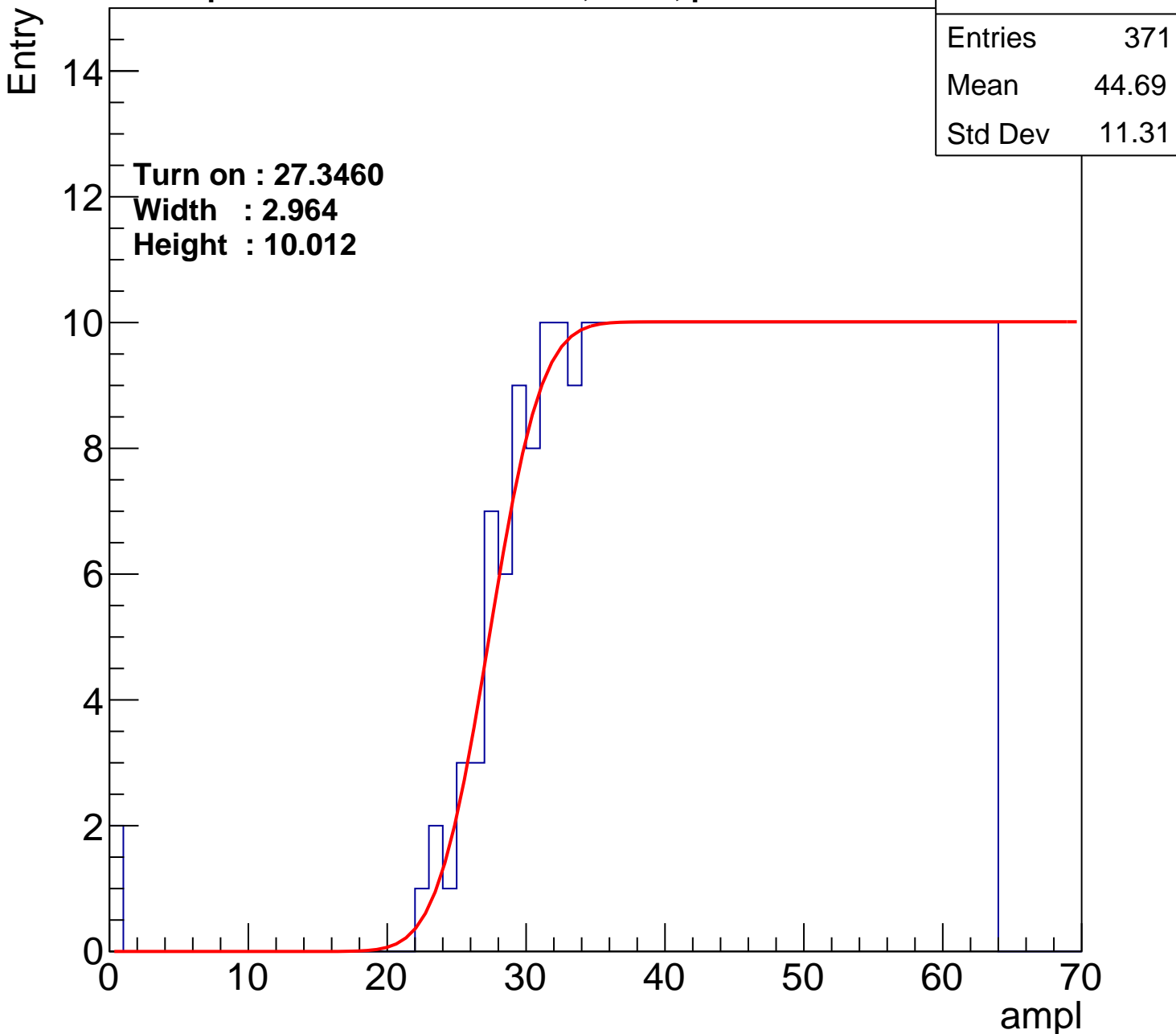
Entries	371
Mean	44.69
Std Dev	11.31

Mean	44.69
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Std Dev	11.31
---------	-------

**Width : 2.964**

**Height : 10.012**



# B0L001S, U25-ch45

calib\_packv5\_042523\_0143.root, FC#9, port A1

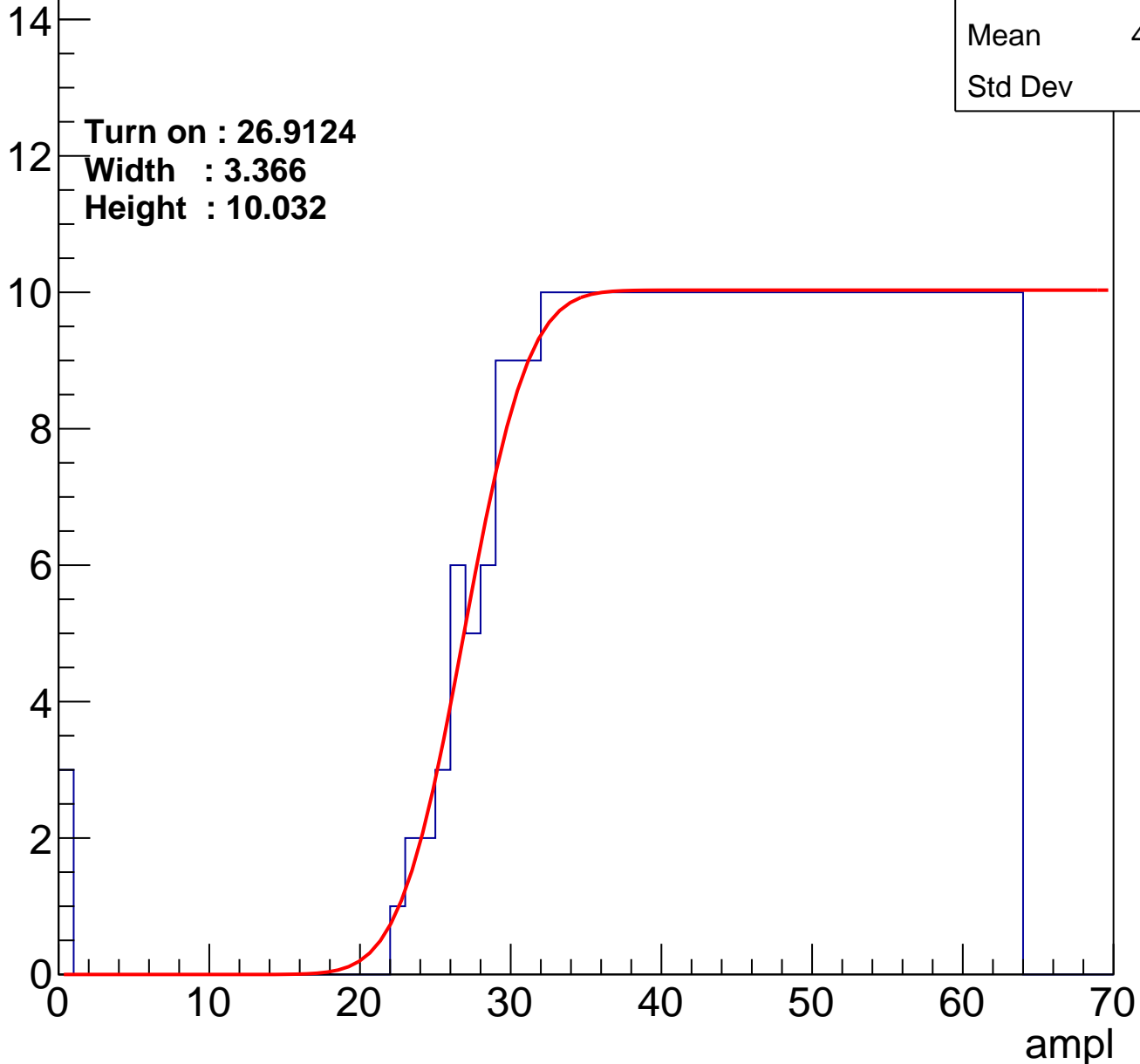
Entries	375
Mean	44.43
Std Dev	11.6

Turn on : 26.9124

Width : 3.366

Height : 10.032

Entry



# B0L001S, U25-ch46

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	342
Mean	46.07
Std Dev	10.78

Turn on : 30.2118

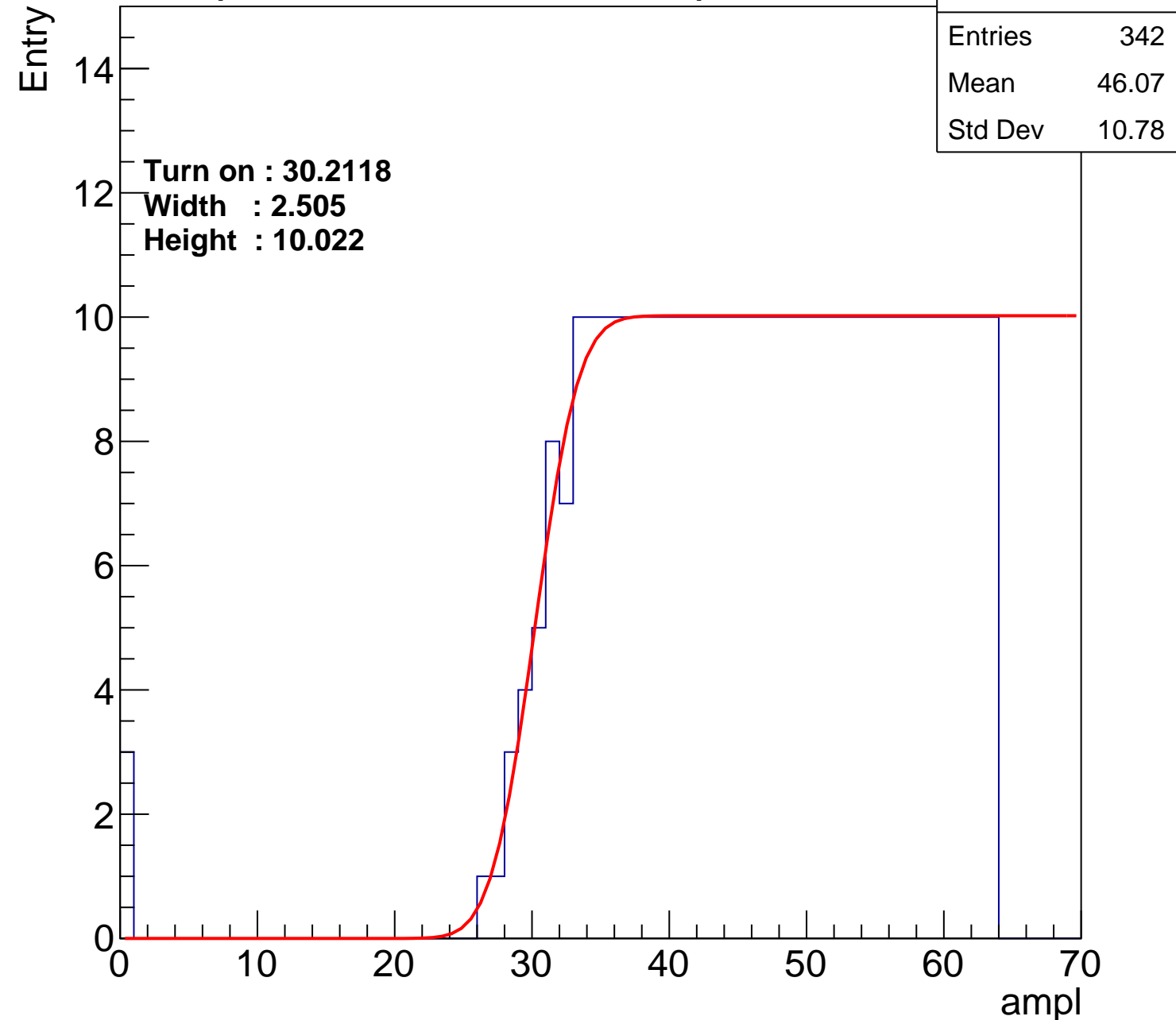
Width : 2.505

Height : 10.022

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U25-ch47

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	370
Mean	44.83
Std Dev	11.05

Turn on : 26.9636

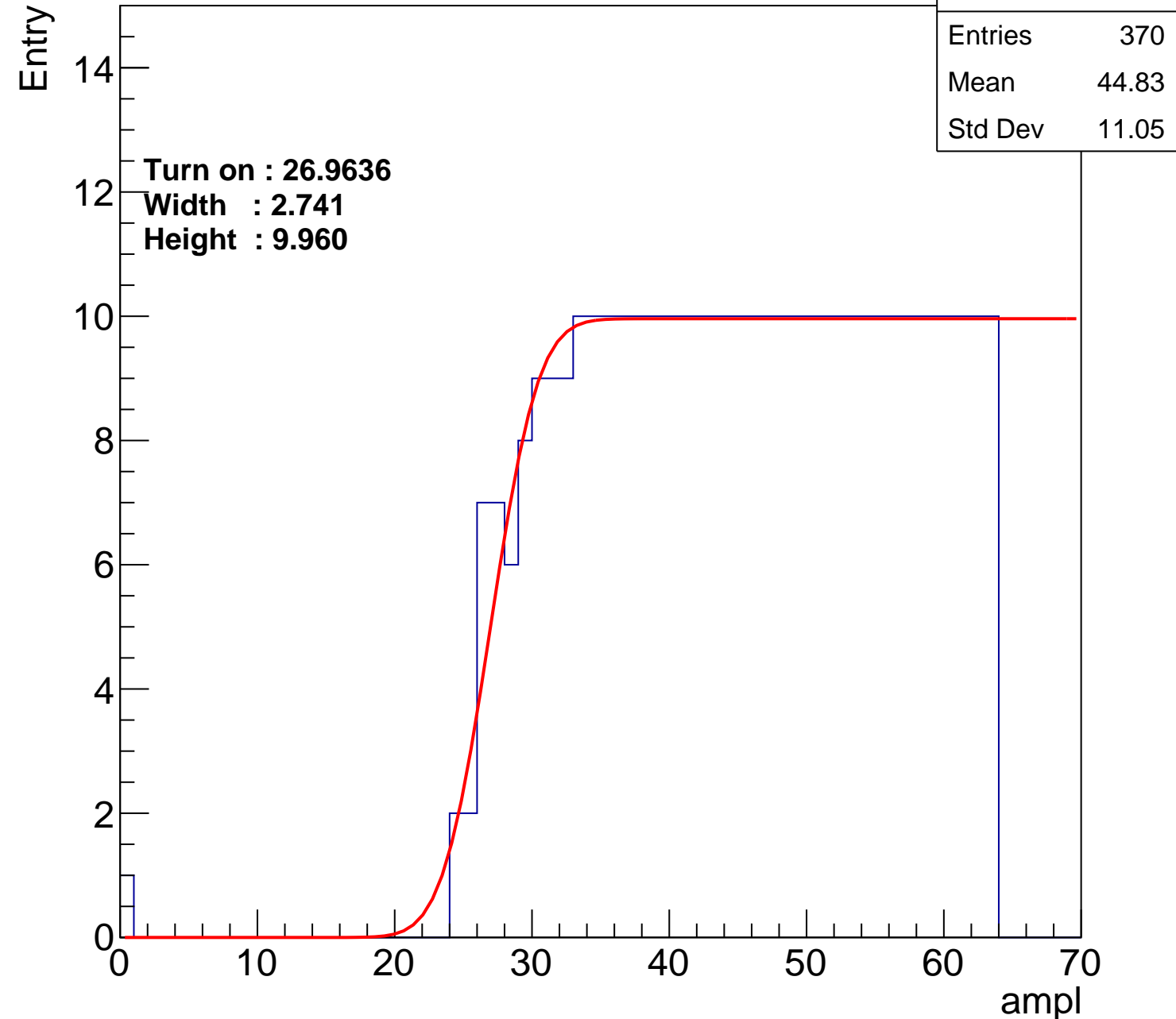
Width : 2.741

Height : 9.960

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch48

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	364
Mean	45.05
Std Dev	11.11

Turn on : 27.9249

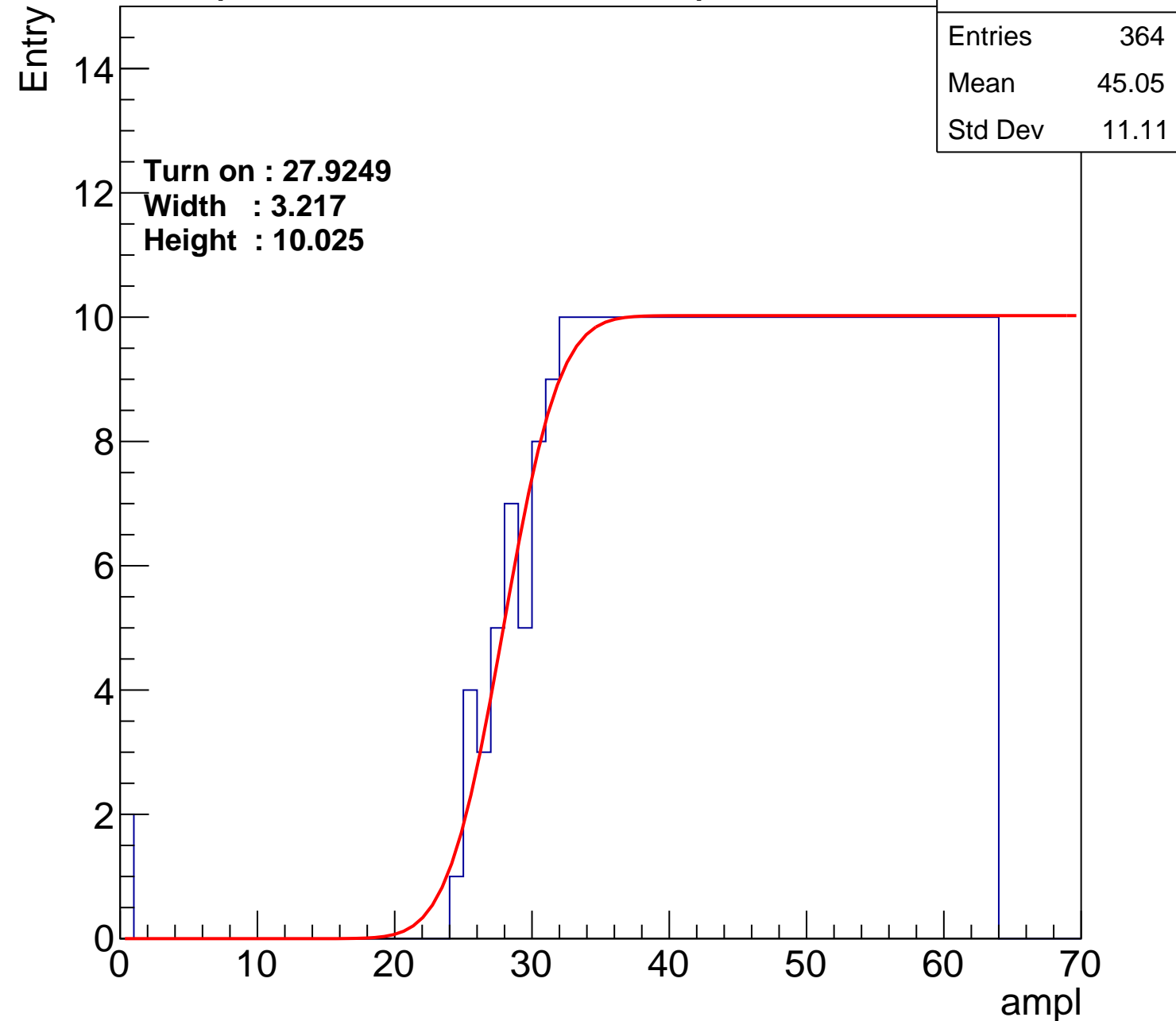
Width : 3.217

Height : 10.025

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch49

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	362
Mean	45.13
Std Dev	11.09

Turn on : 28.1374

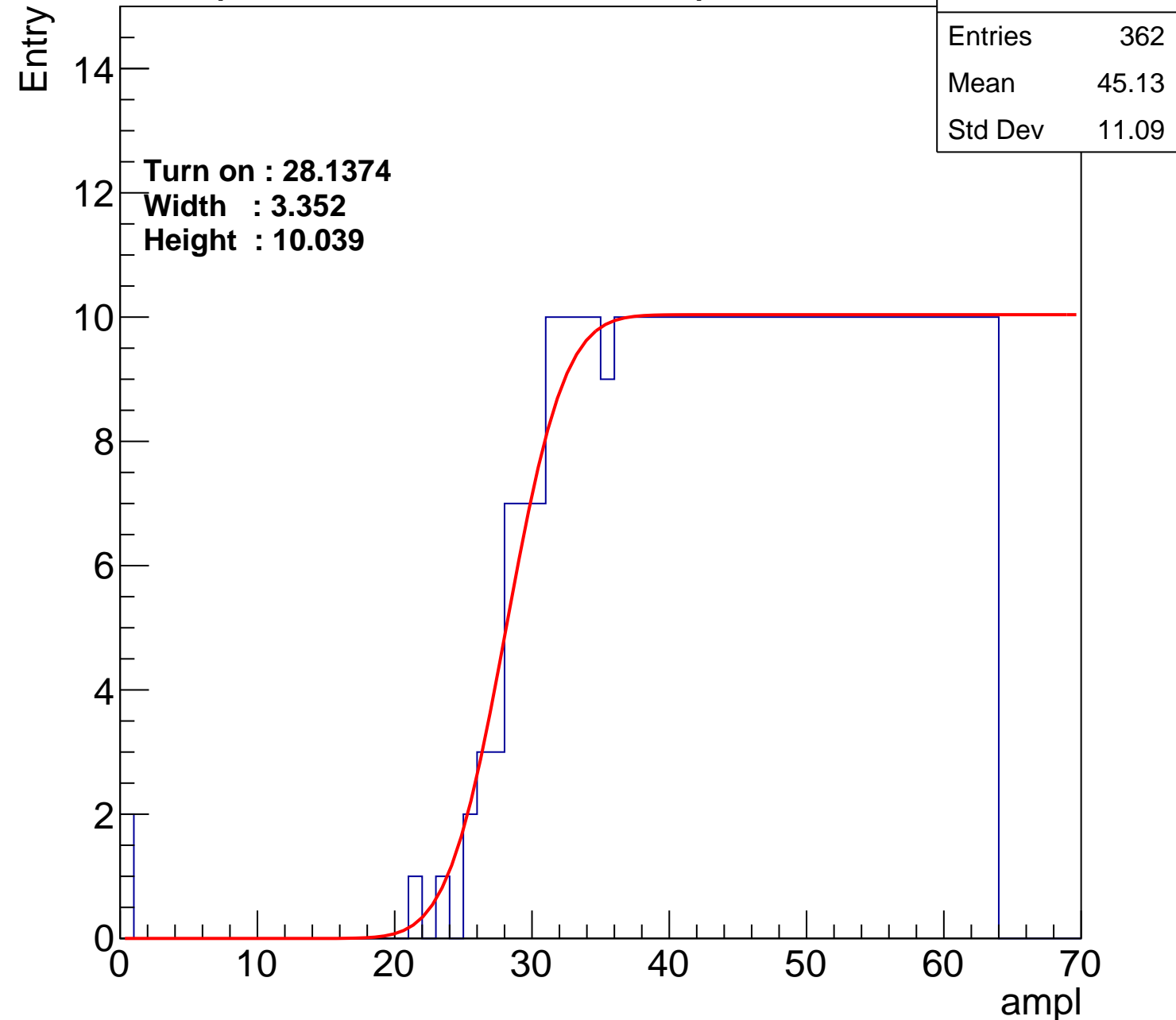
Width : 3.352

Height : 10.039

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch50

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	383
Mean	44.09
Std Dev	11.64

Turn on : 26.2421

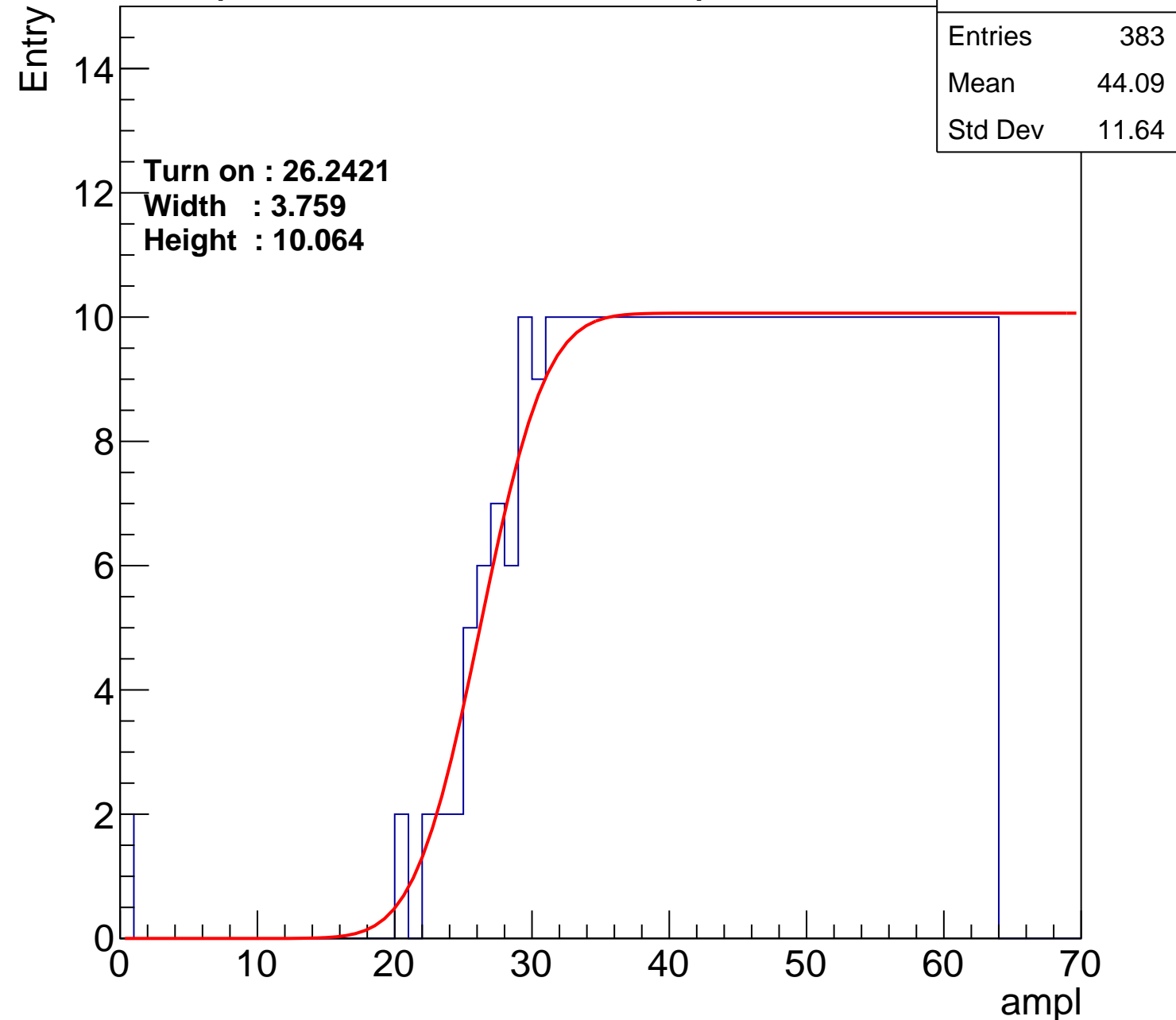
Width : 3.759

Height : 10.064

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch51

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	377
Mean	44.22
Std Dev	11.96

Turn on : 26.9586

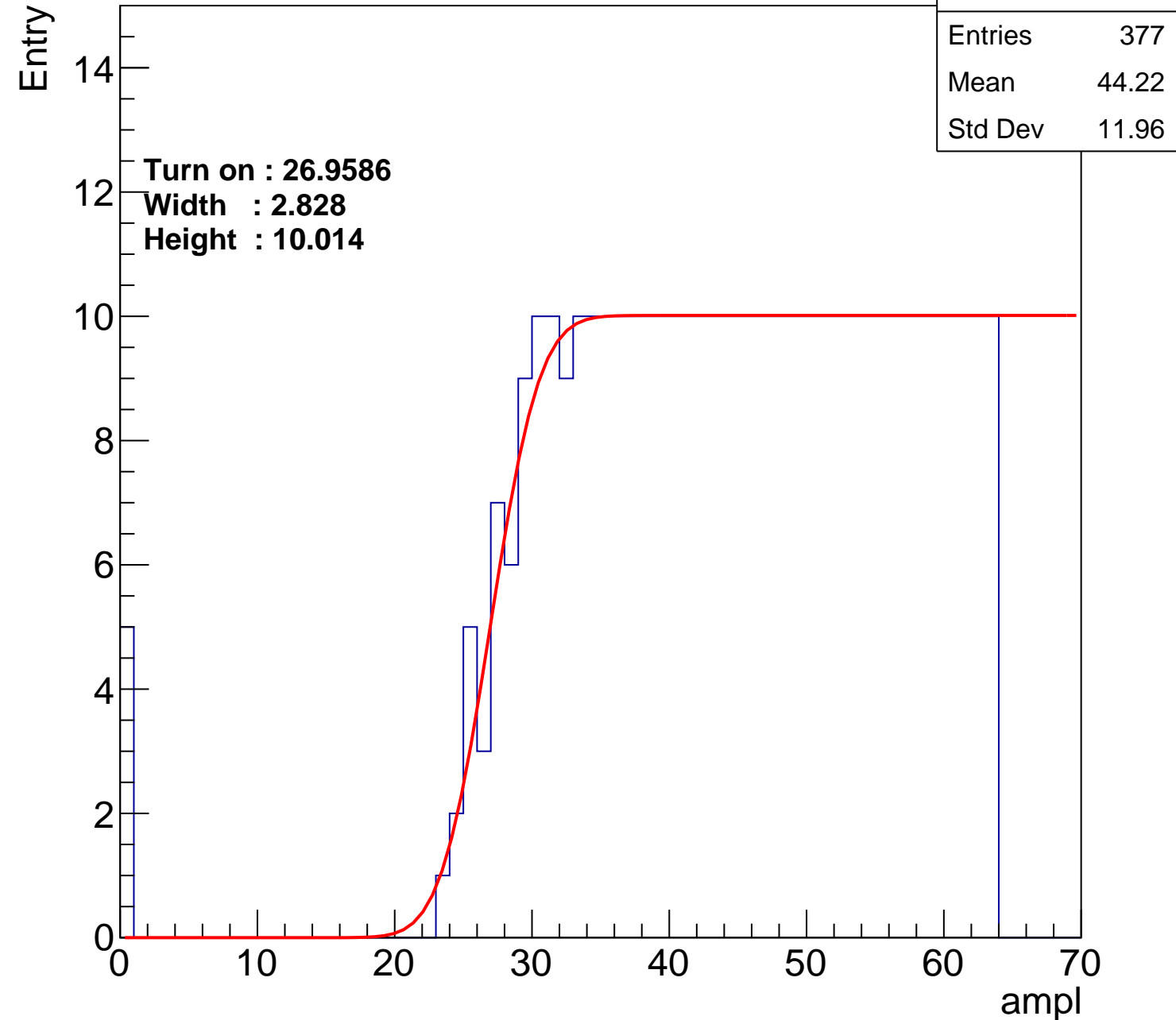
Width : 2.828

Height : 10.014

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch52

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	369
Mean	44.69
Std Dev	11.57

Turn on : 27.5980

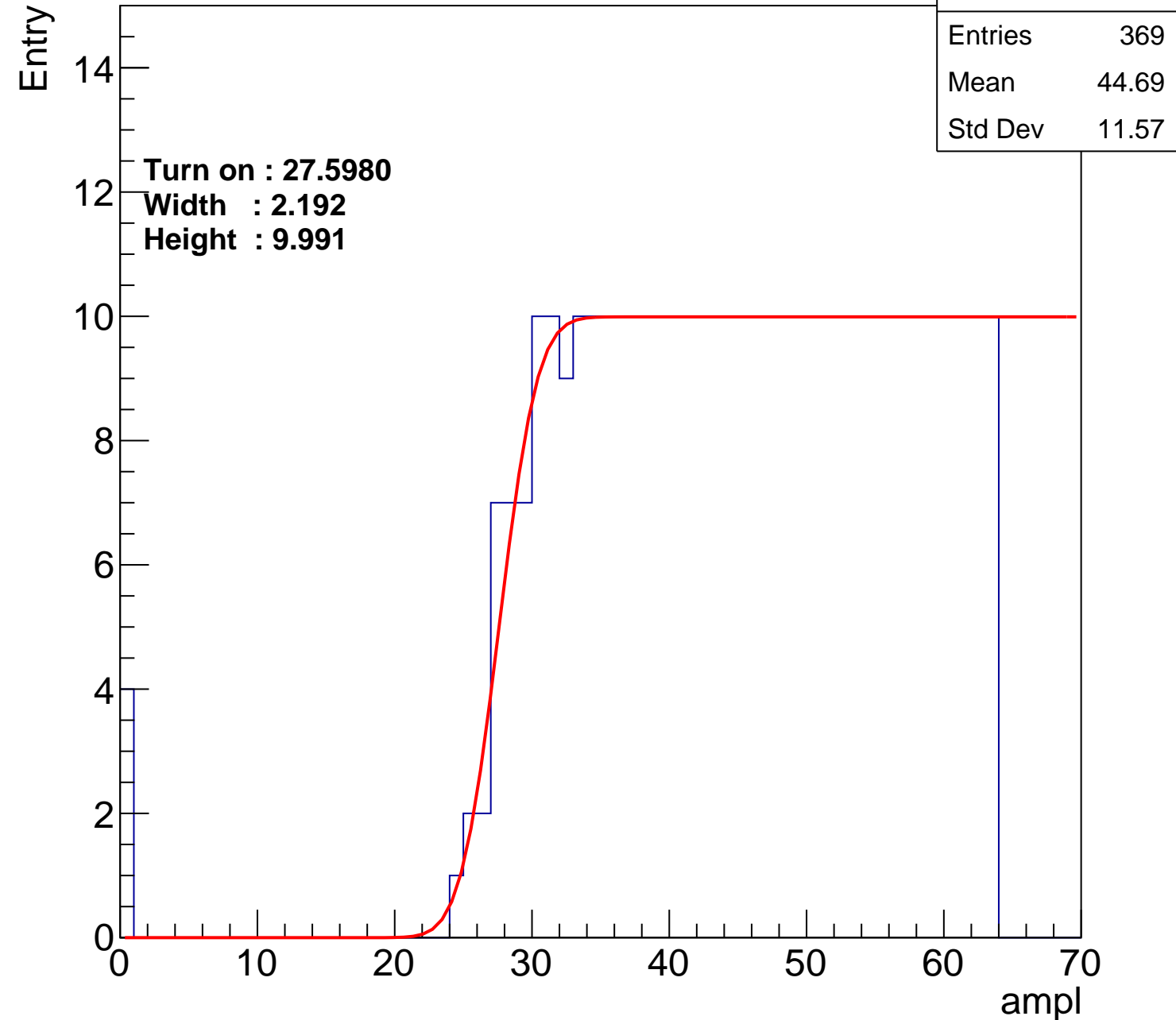
Width : 2.192

Height : 9.991

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch53

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	369
Mean	44.85
Std Dev	11.09

Turn on : 27.9919

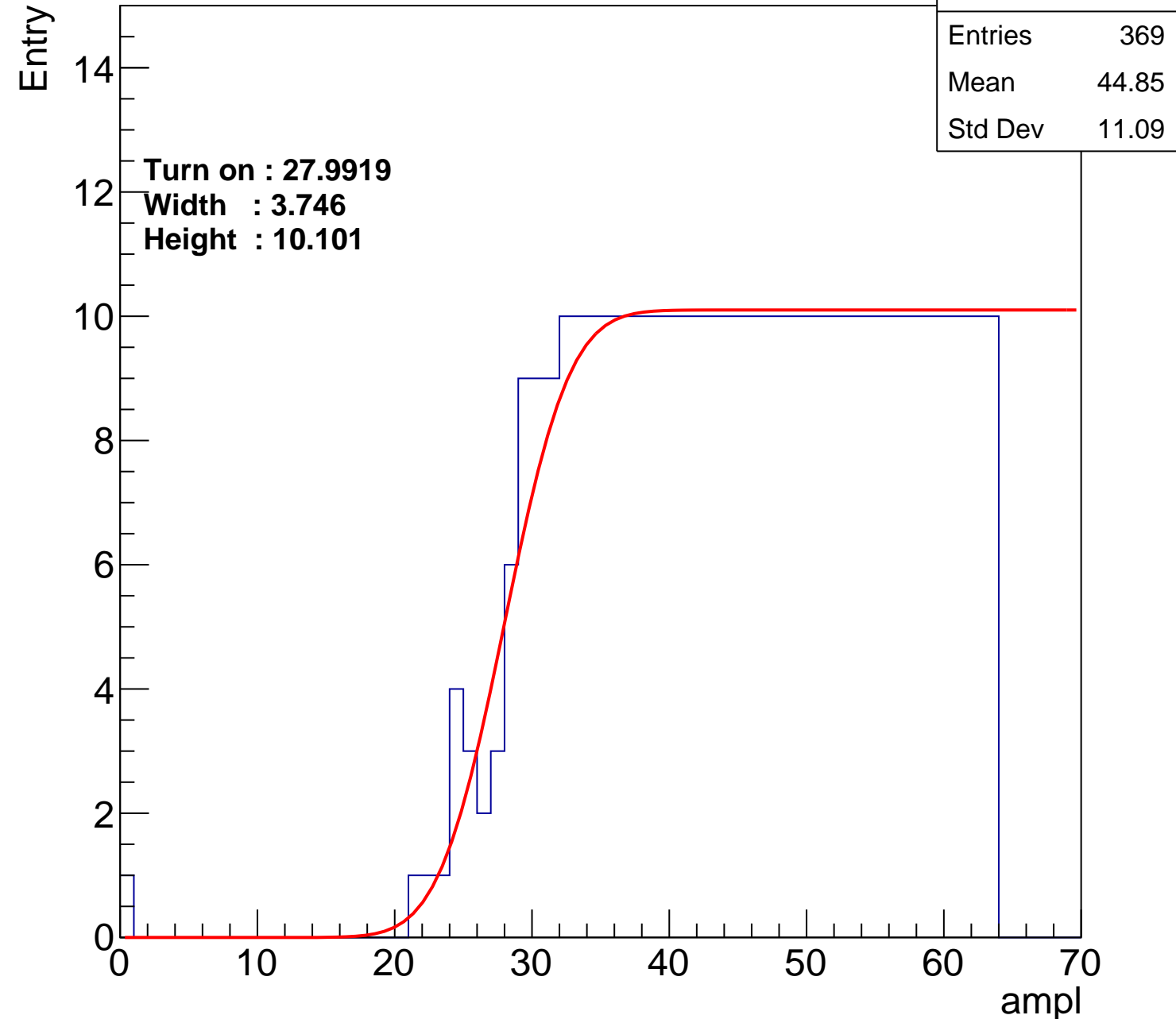
Width : 3.746

Height : 10.101

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch54

calib\_packv5\_042523\_0143.root, FC#9, port A1

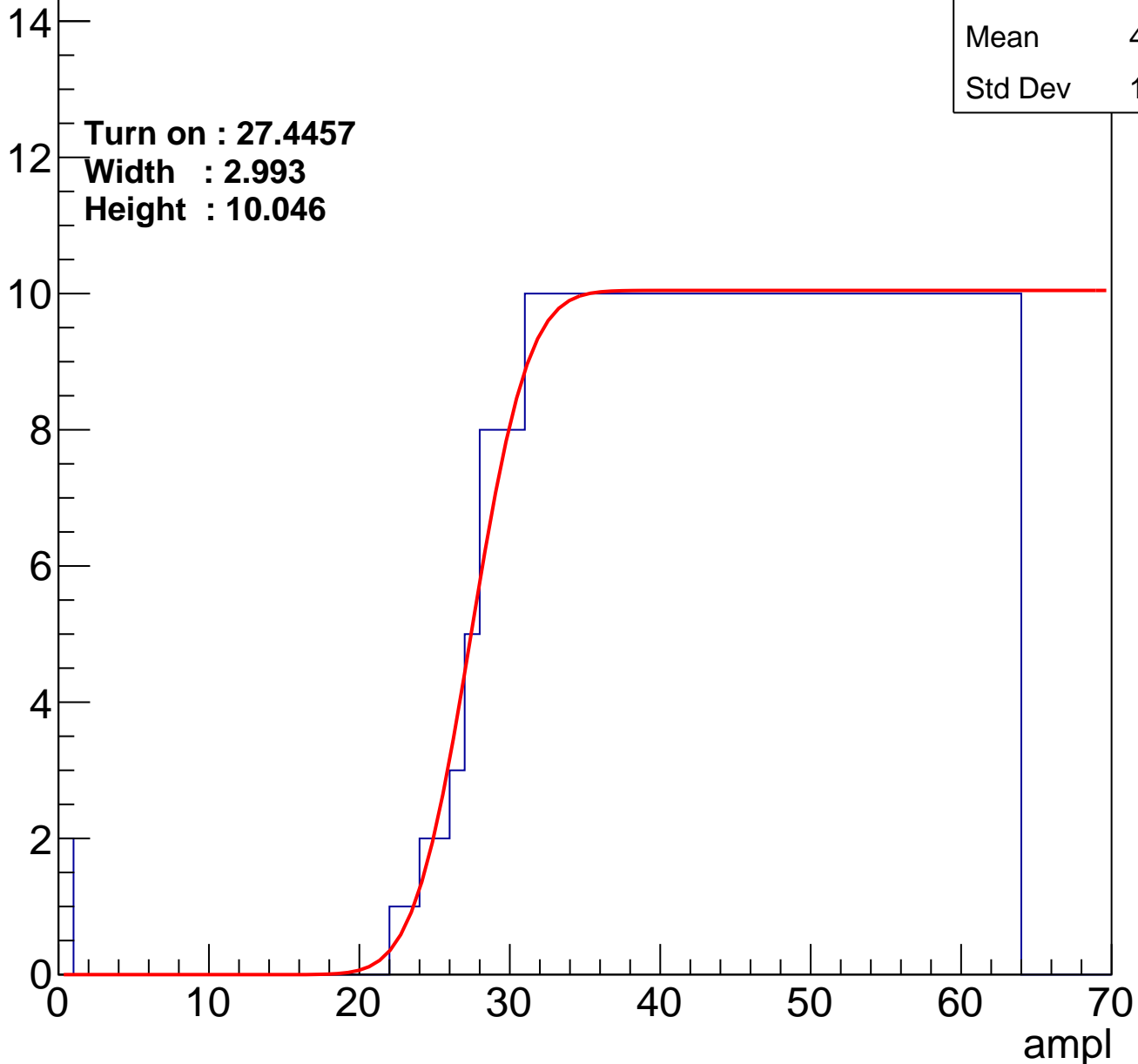
Entries	370
Mean	44.76
Std Dev	11.25

Turn on : 27.4457

Width : 2.993

Height : 10.046

Entry





# B0L001S, U25-ch55

calib\_packv5\_042523\_0143.root, FC#9, port A1

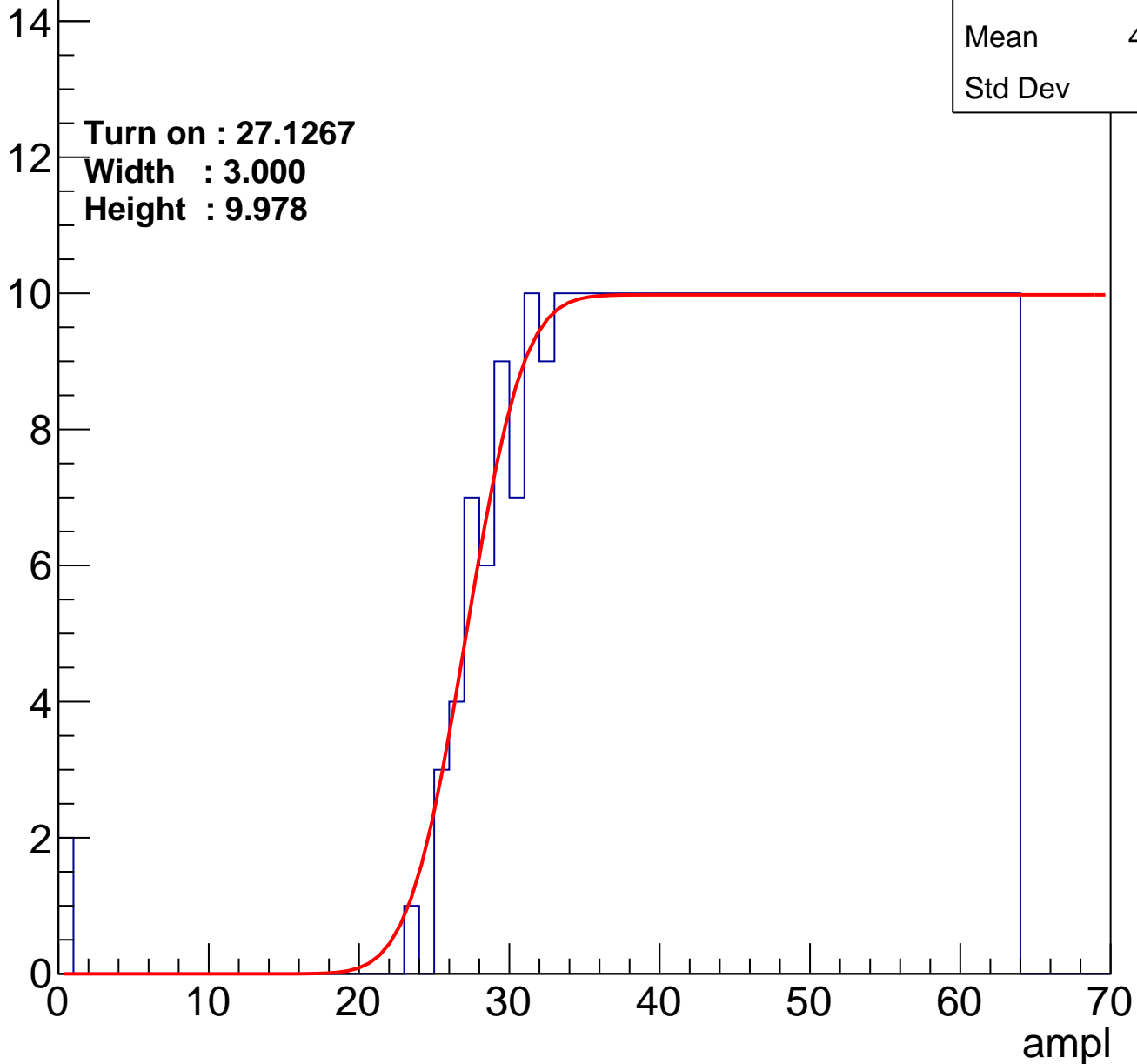
Entries	368
Mean	44.86
Std Dev	11.2

Turn on : 27.1267

Width : 3.000

Height : 9.978

Entry



# B0L001S, U25-ch56

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	376
Mean	44.23
Std Dev	12

Turn on : 27.0551

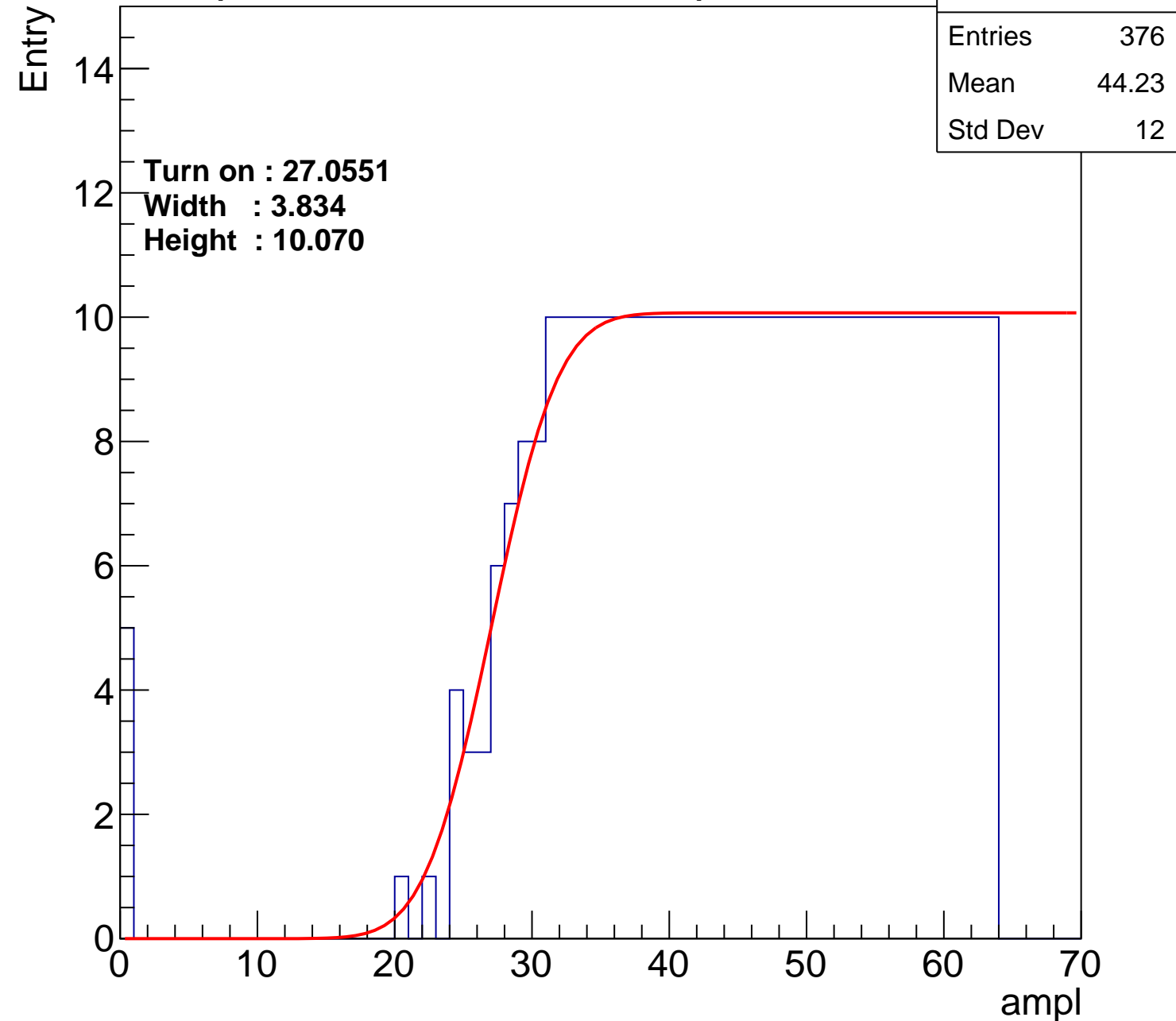
Width : 3.834

Height : 10.070

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch57

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	357
Mean	45.45
Std Dev	10.74

**Turn on : 29.1965**

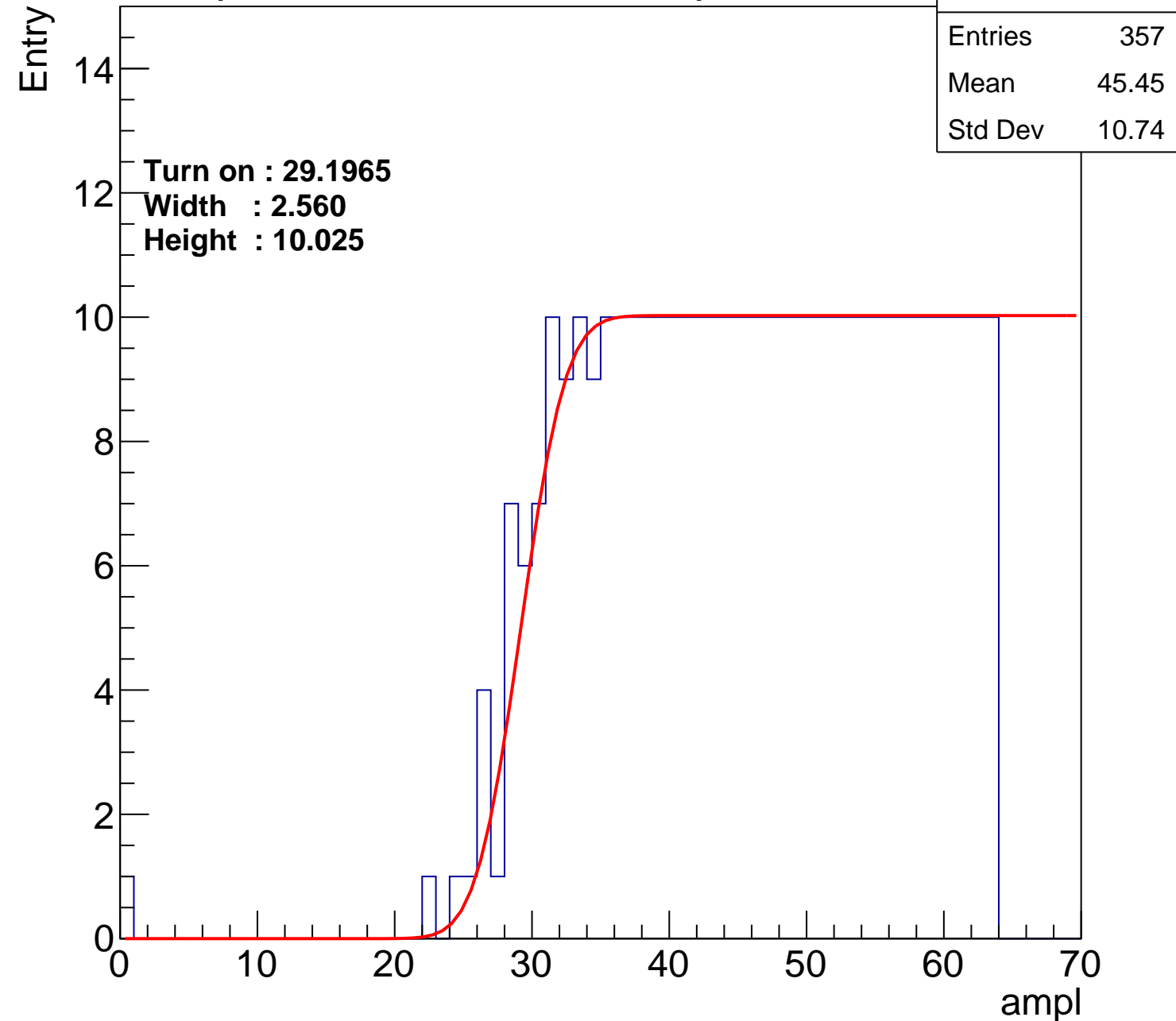
**Width : 2.560**

**Height : 10.025**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch58

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	371
Mean	44.69
Std Dev	11.24

Turn on : 27.1688

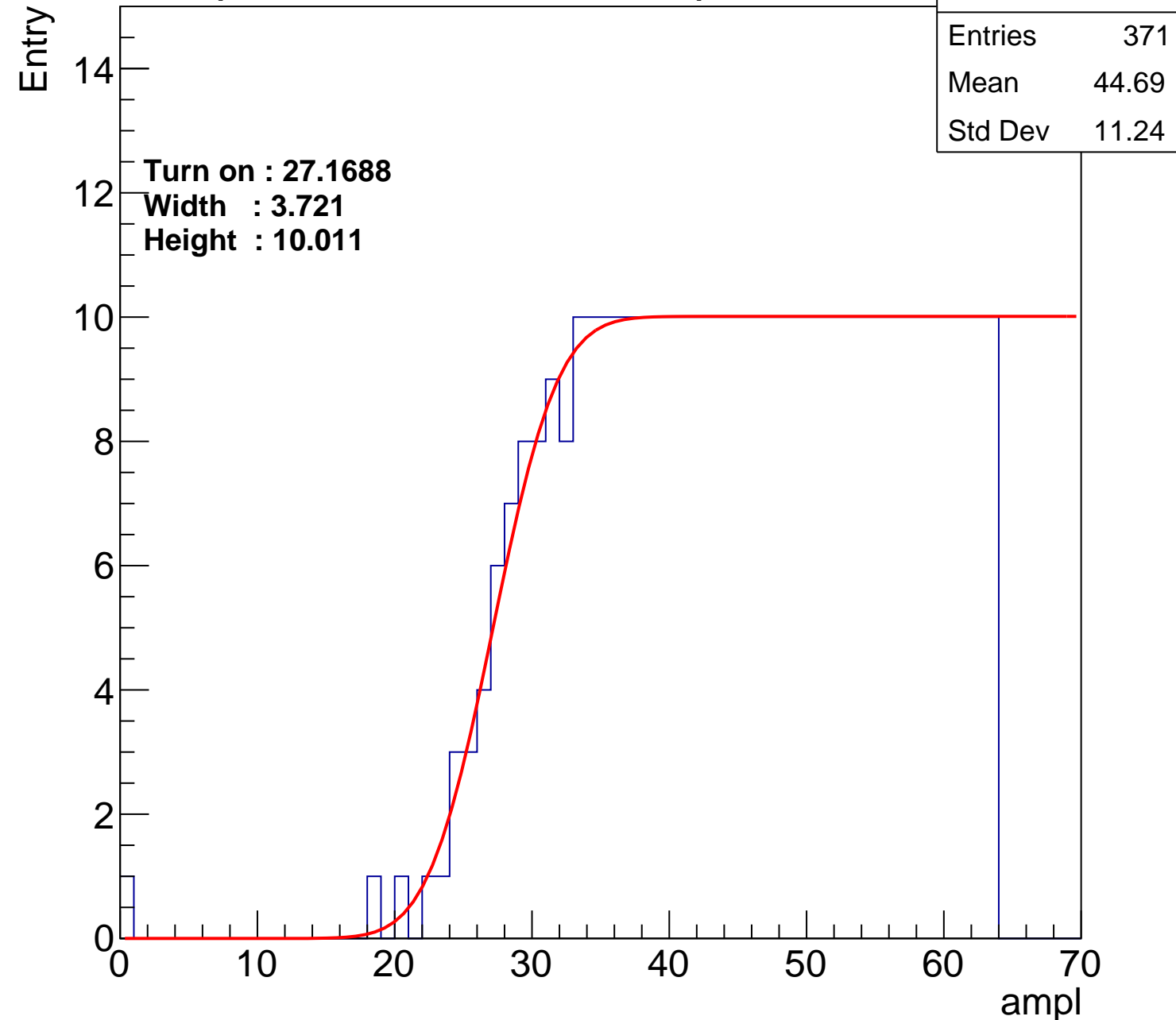
Width : 3.721

Height : 10.011

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch59

calib\_packv5\_042523\_0143.root, FC#9, port A1

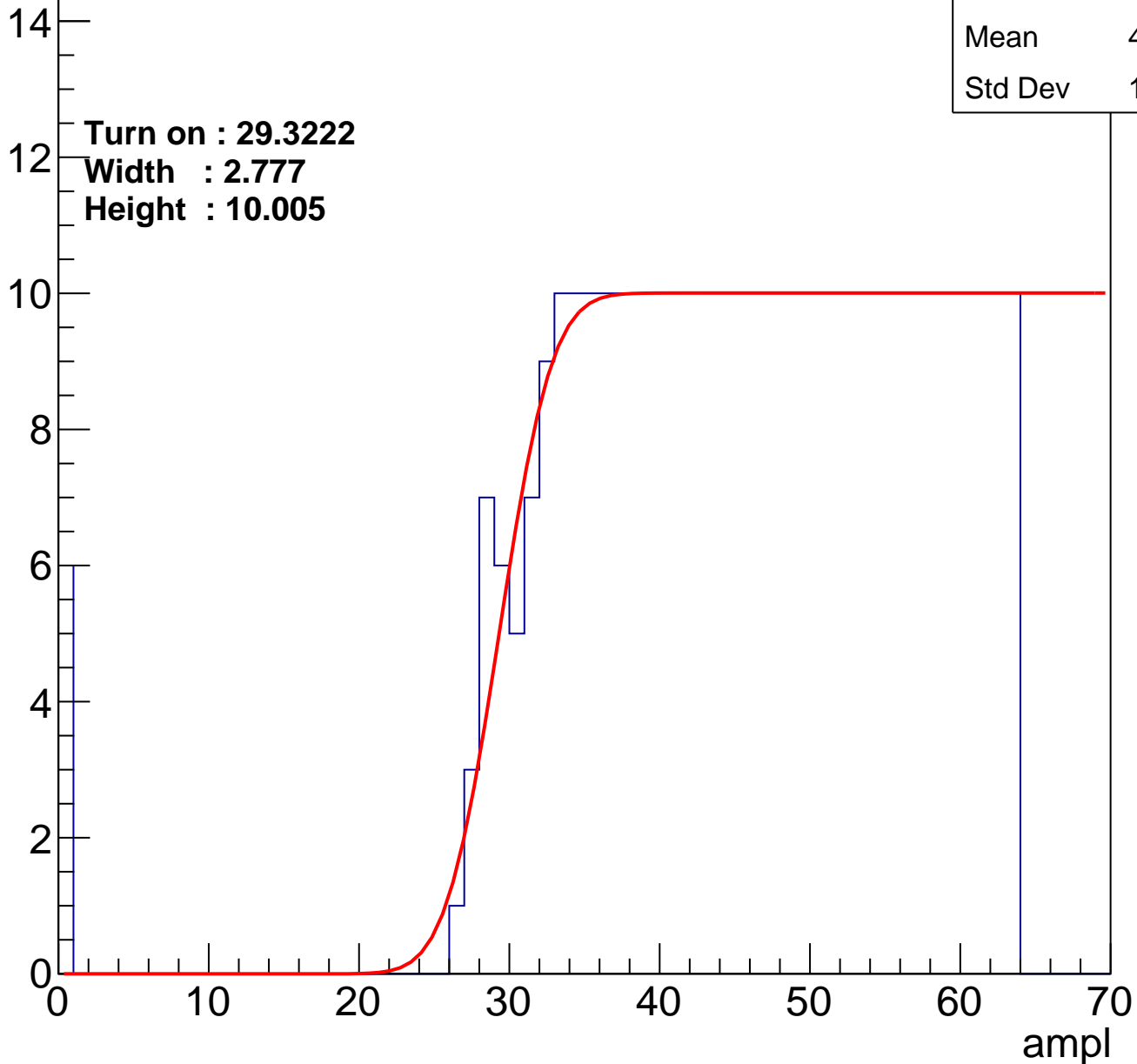
Entries	354
Mean	45.23
Std Dev	11.72

Turn on : 29.3222

Width : 2.777

Height : 10.005

Entry



# B0L001S, U25-ch60

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	369
Mean	44.75
Std Dev	11.31

Turn on : 27.1064

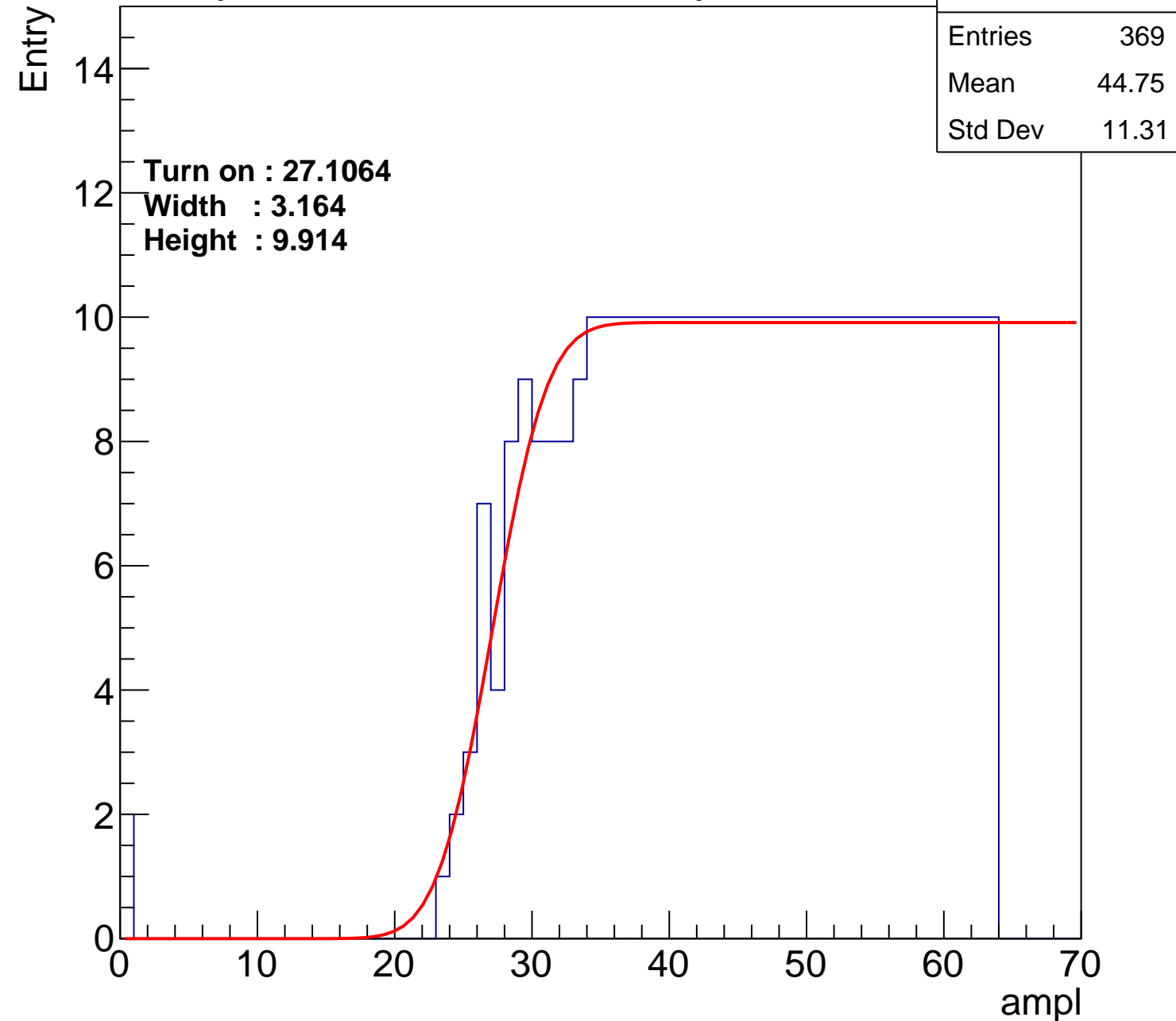
Width : 3.164

Height : 9.914

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch61

calib\_packv5\_042523\_0143.root, FC#9, port A1

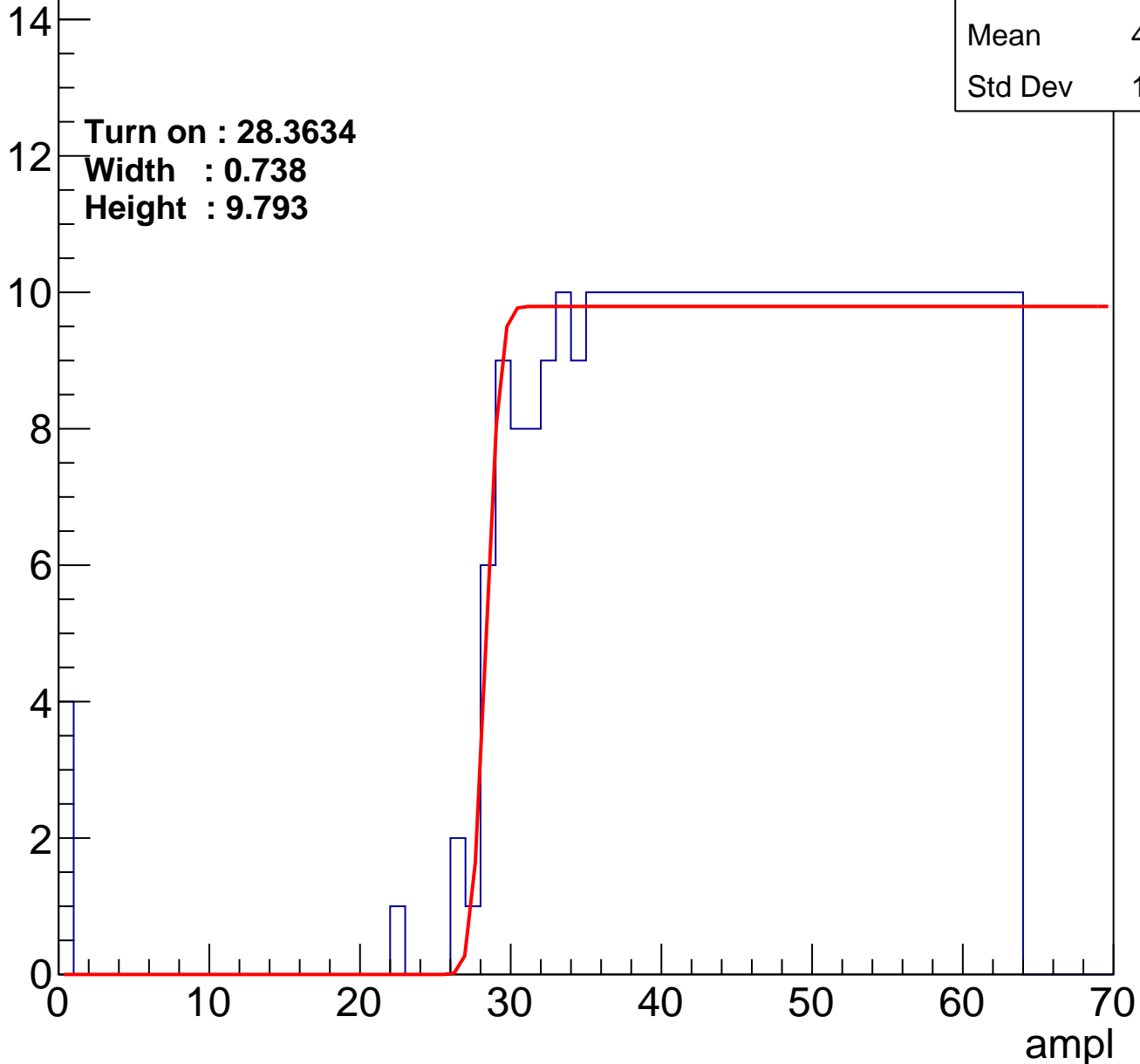
Entries	357
Mean	45.24
Std Dev	11.36

Turn on : 28.3634

Width : 0.738

Height : 9.793

Entry



# B0L001S, U25-ch62

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	350
Mean	45.48
Std Dev	11.37

Turn on : 29.9912

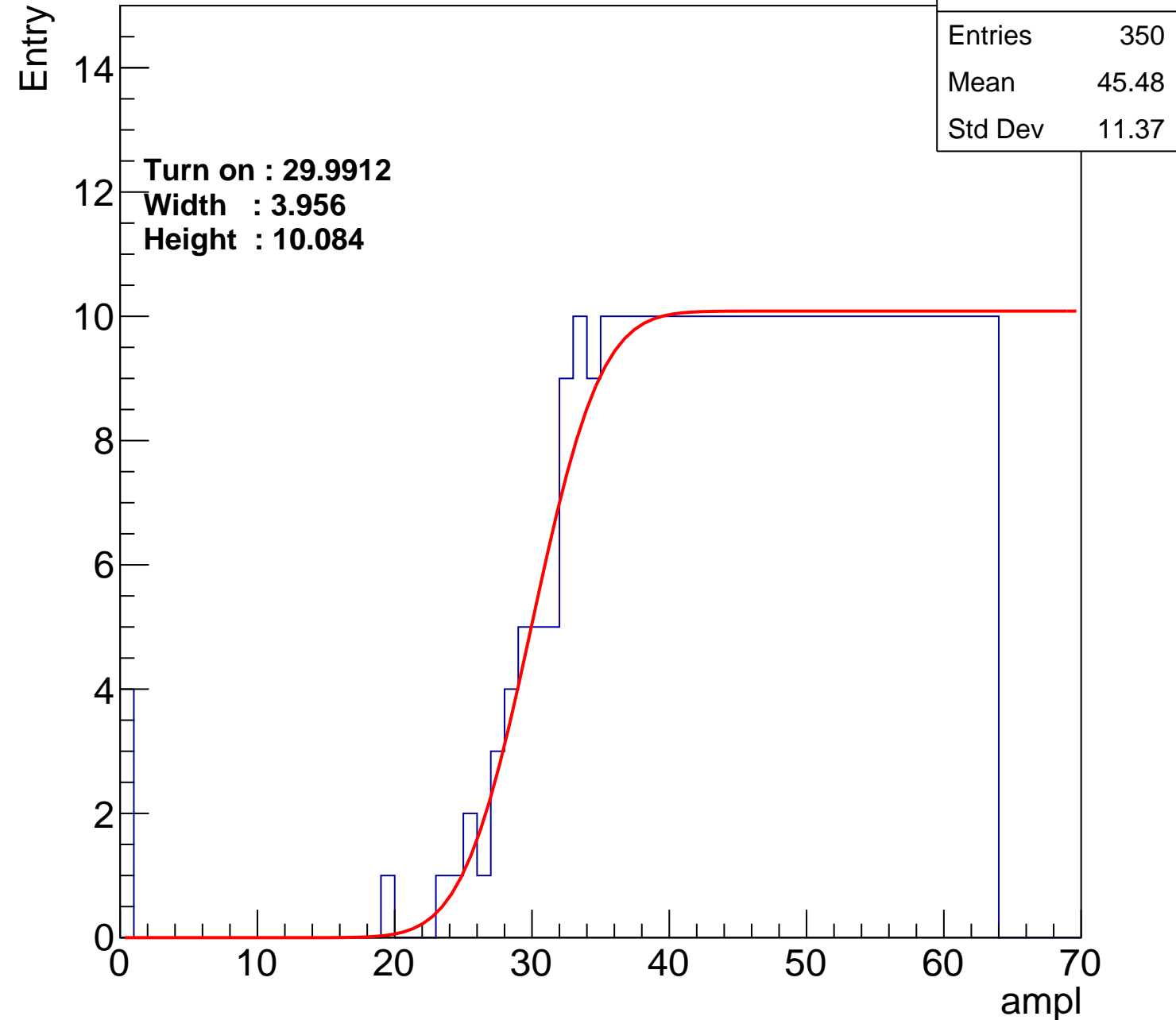
Width : 3.956

Height : 10.084

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U25-ch63

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	362
Mean	44.99
Std Dev	11.48

Turn on : 28.4577

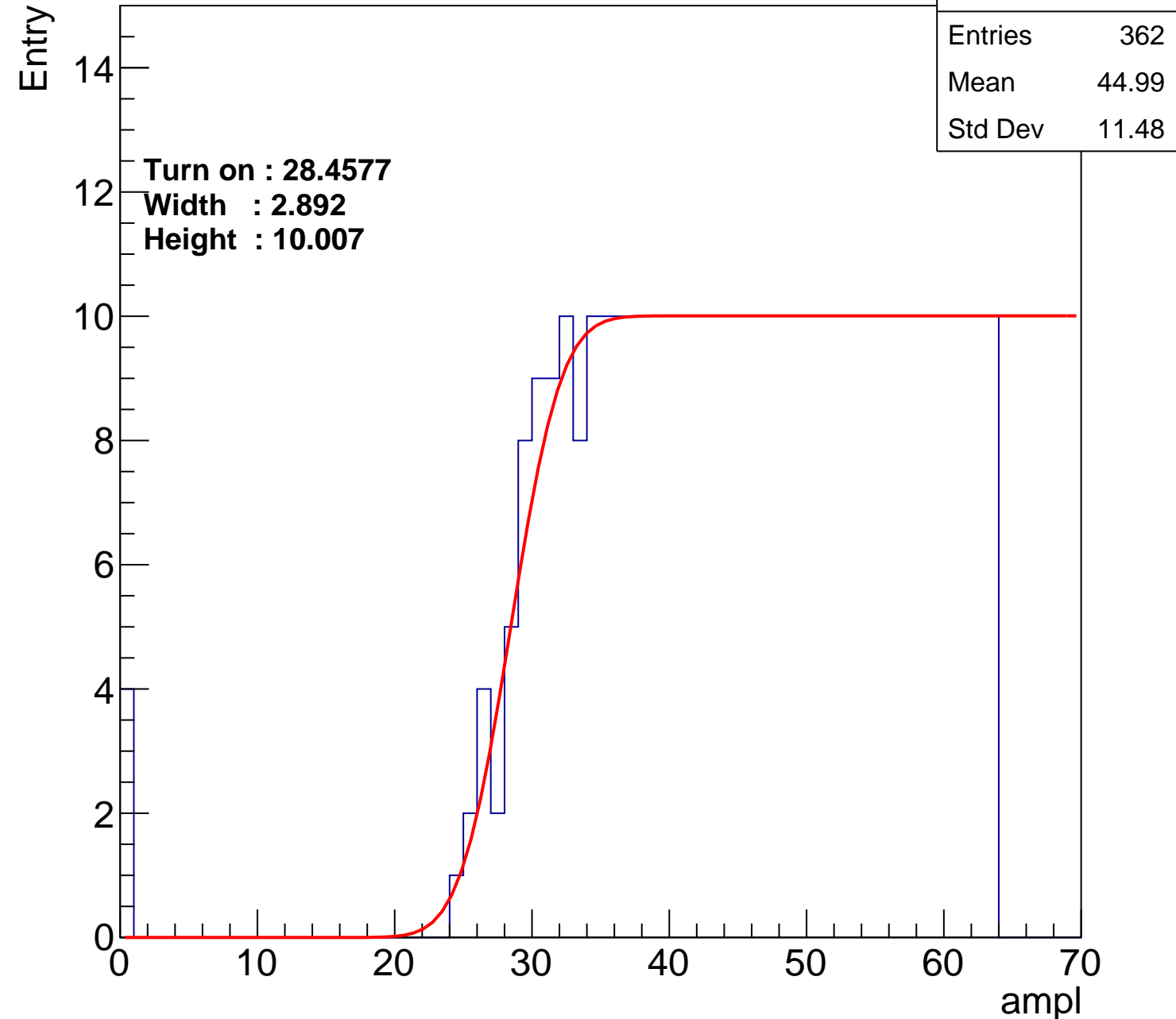
Width : 2.892

Height : 10.007

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch64

calib\_packv5\_042523\_0143.root, FC#9, port A1

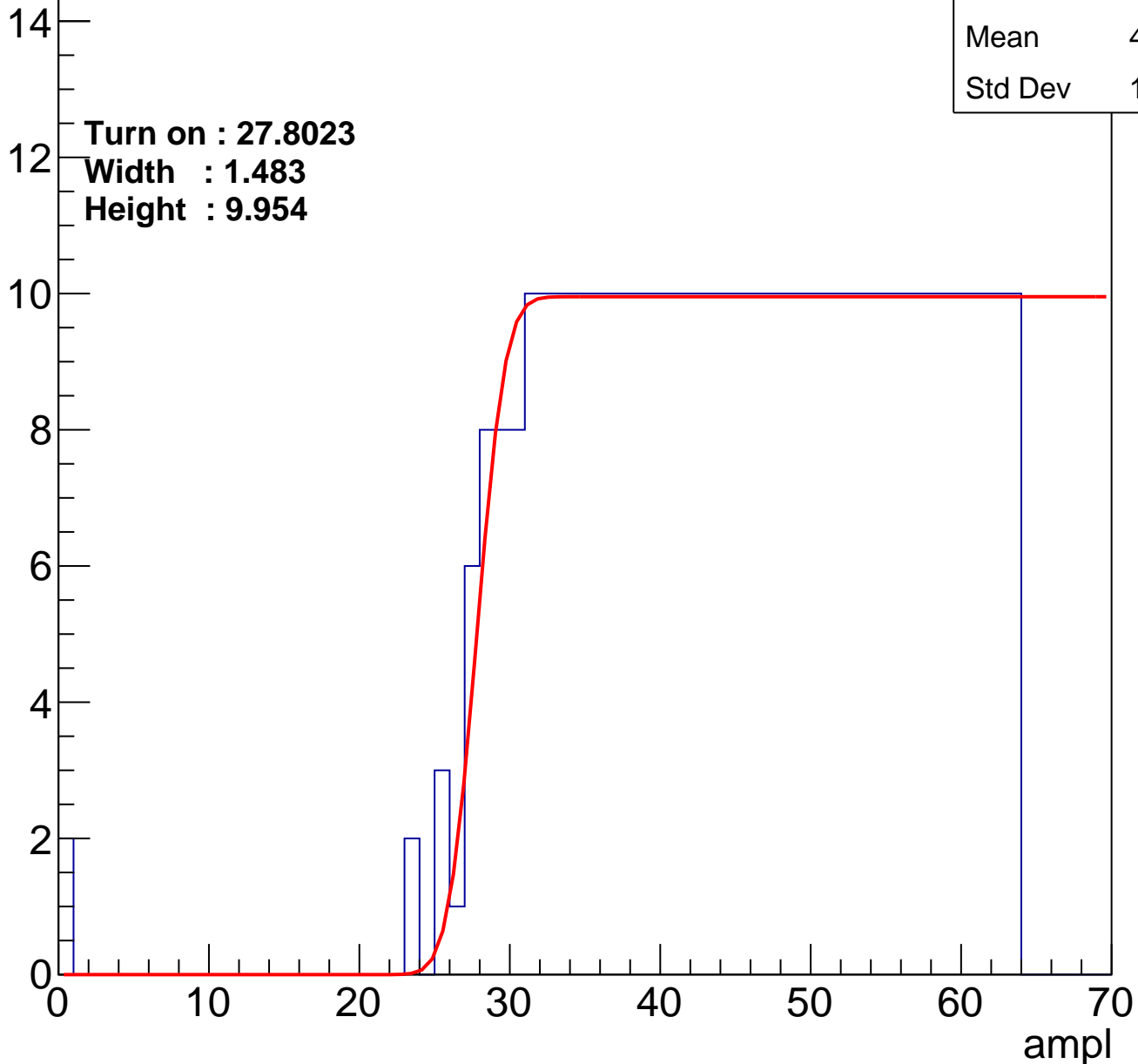
Entries	368
Mean	44.88
Std Dev	11.17

Turn on : 27.8023

Width : 1.483

Height : 9.954

Entry



# B0L001S, U25-ch65

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	359
Mean	45.34
Std Dev	10.91

**Turn on : 28.0540**

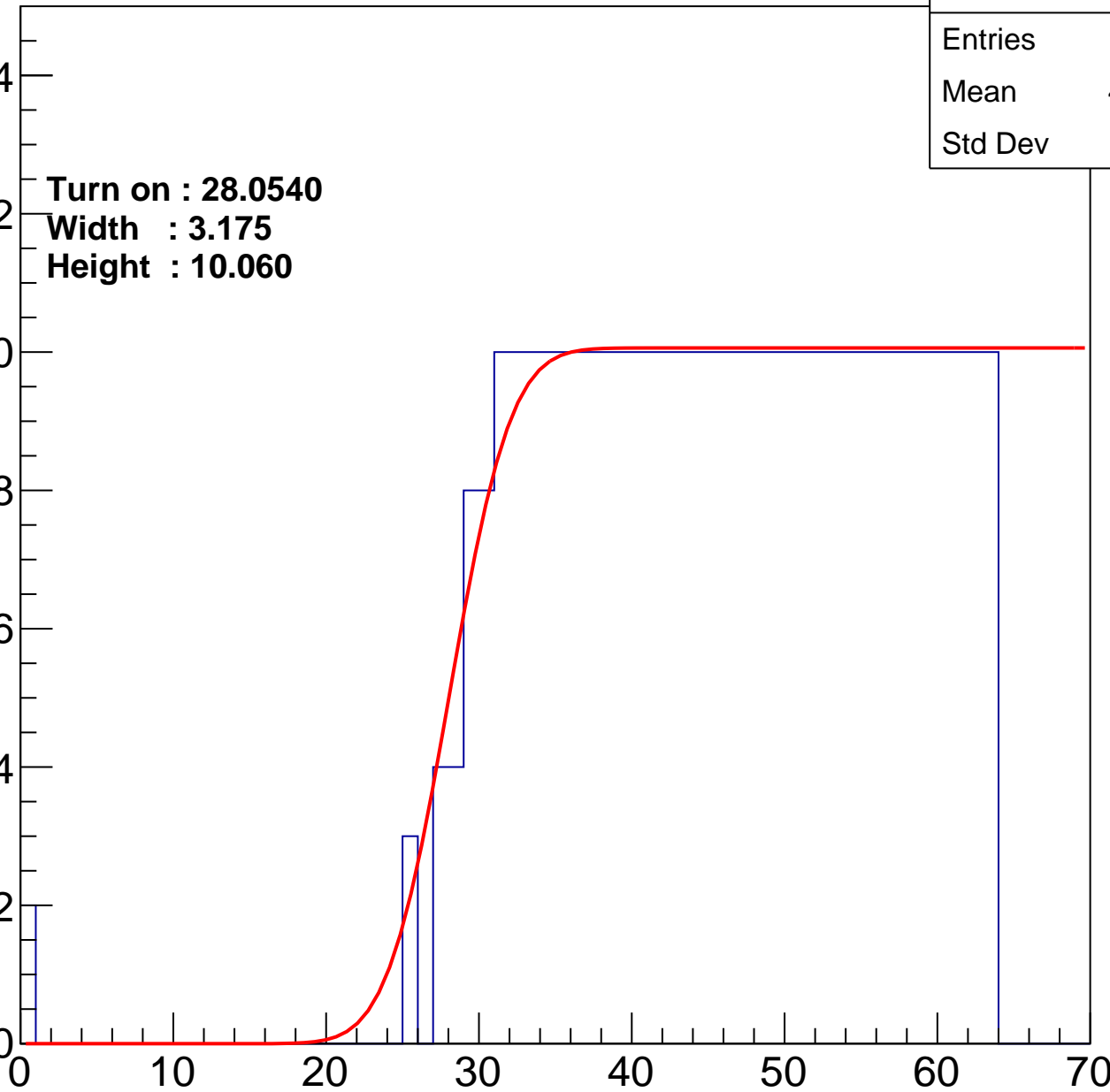
**Width : 3.175**

**Height : 10.060**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch66

calib\_packv5\_042523\_0143.root, FC#9, port A1

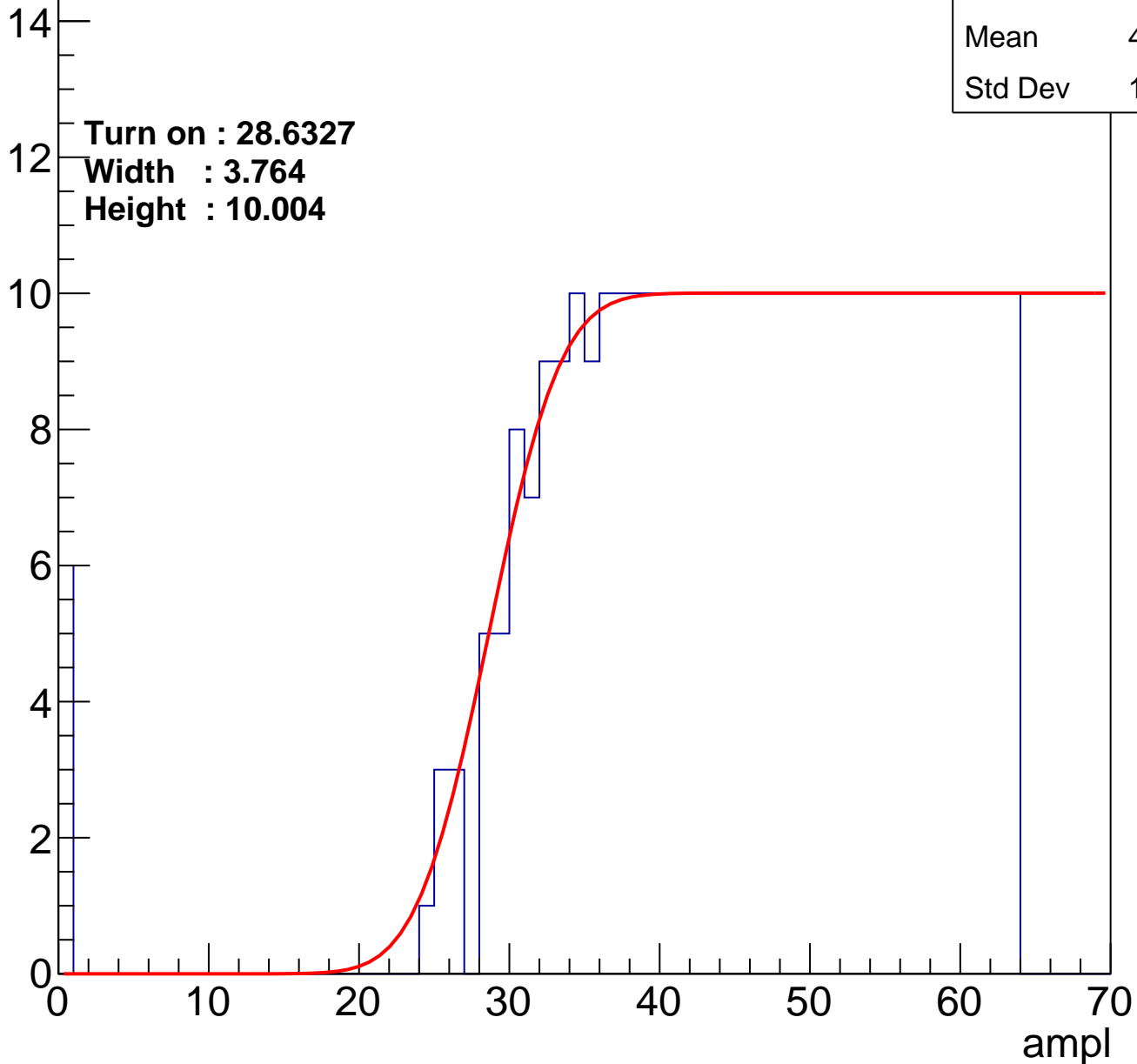
Entries	355
Mean	45.12
Std Dev	11.82

**Turn on : 28.6327**

**Width : 3.764**

**Height : 10.004**

Entry



# B0L001S, U25-ch67

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	357
Mean	45.07
Std Dev	11.81

Turn on : 29.1441

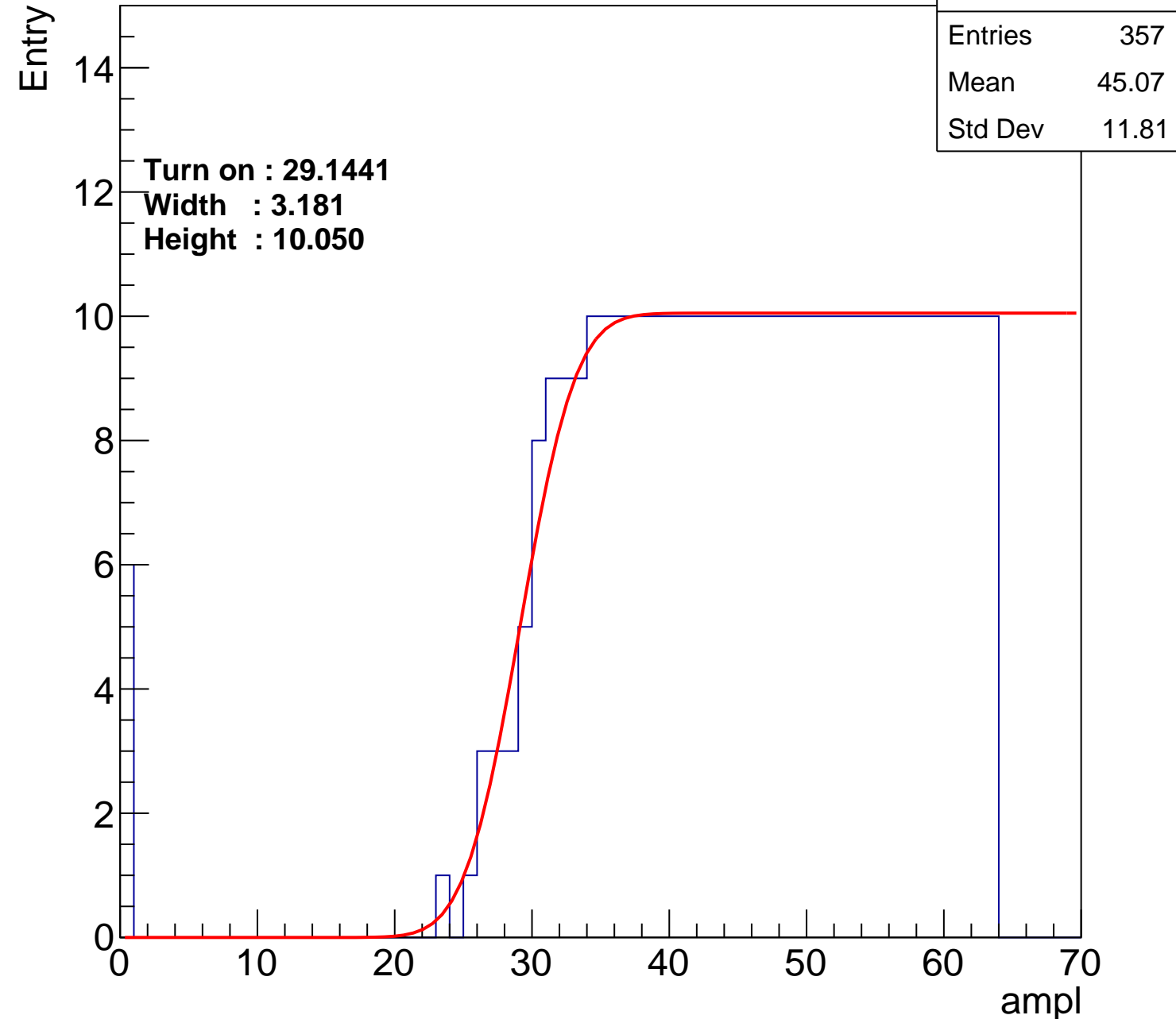
Width : 3.181

Height : 10.050

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch68

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	371
Mean	44.68
Std Dev	11.32

Turn on : 27.4423

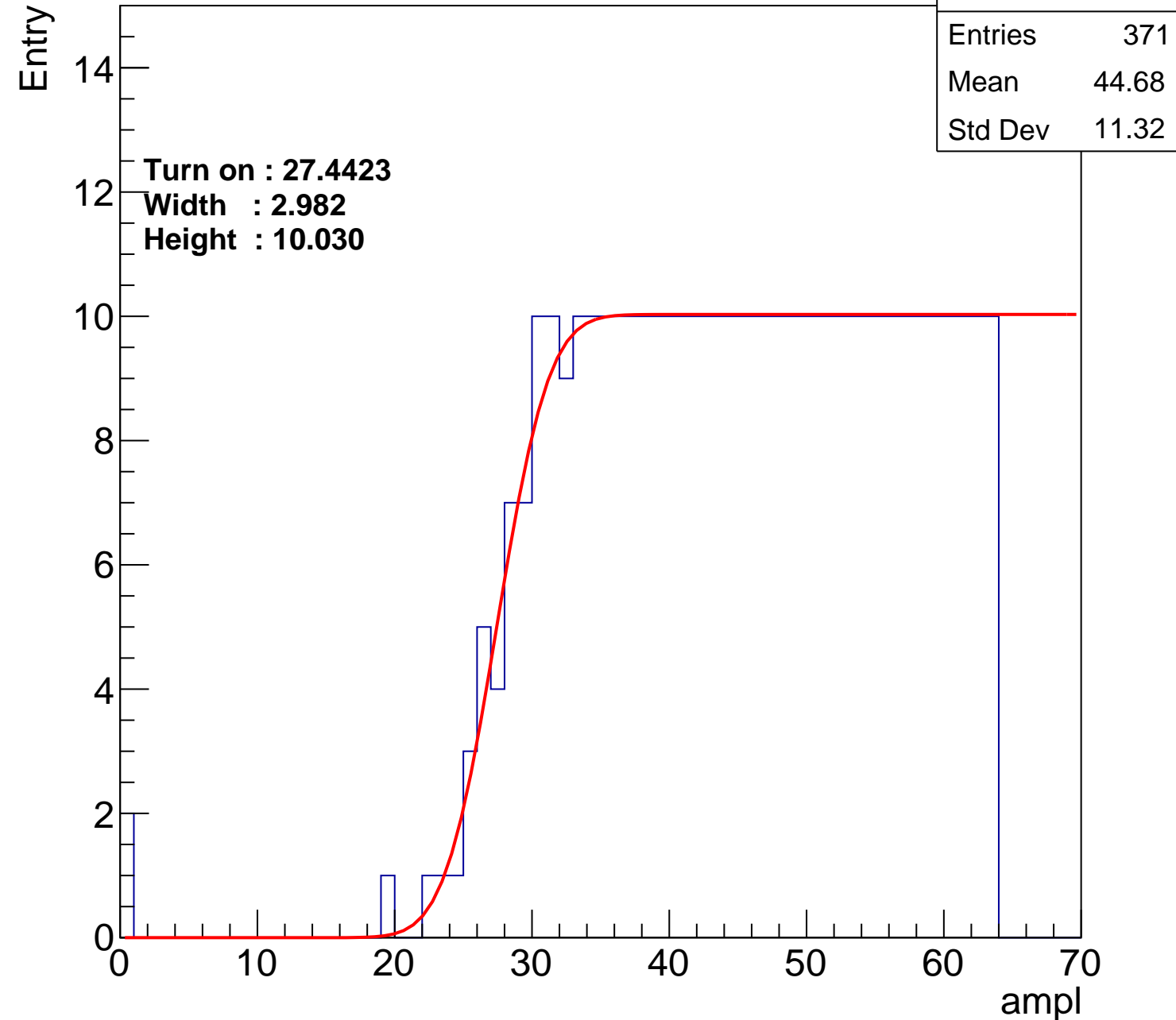
Width : 2.982

Height : 10.030

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch69

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	359
Mean	45.25
Std Dev	11.06

Turn on : 28.4850

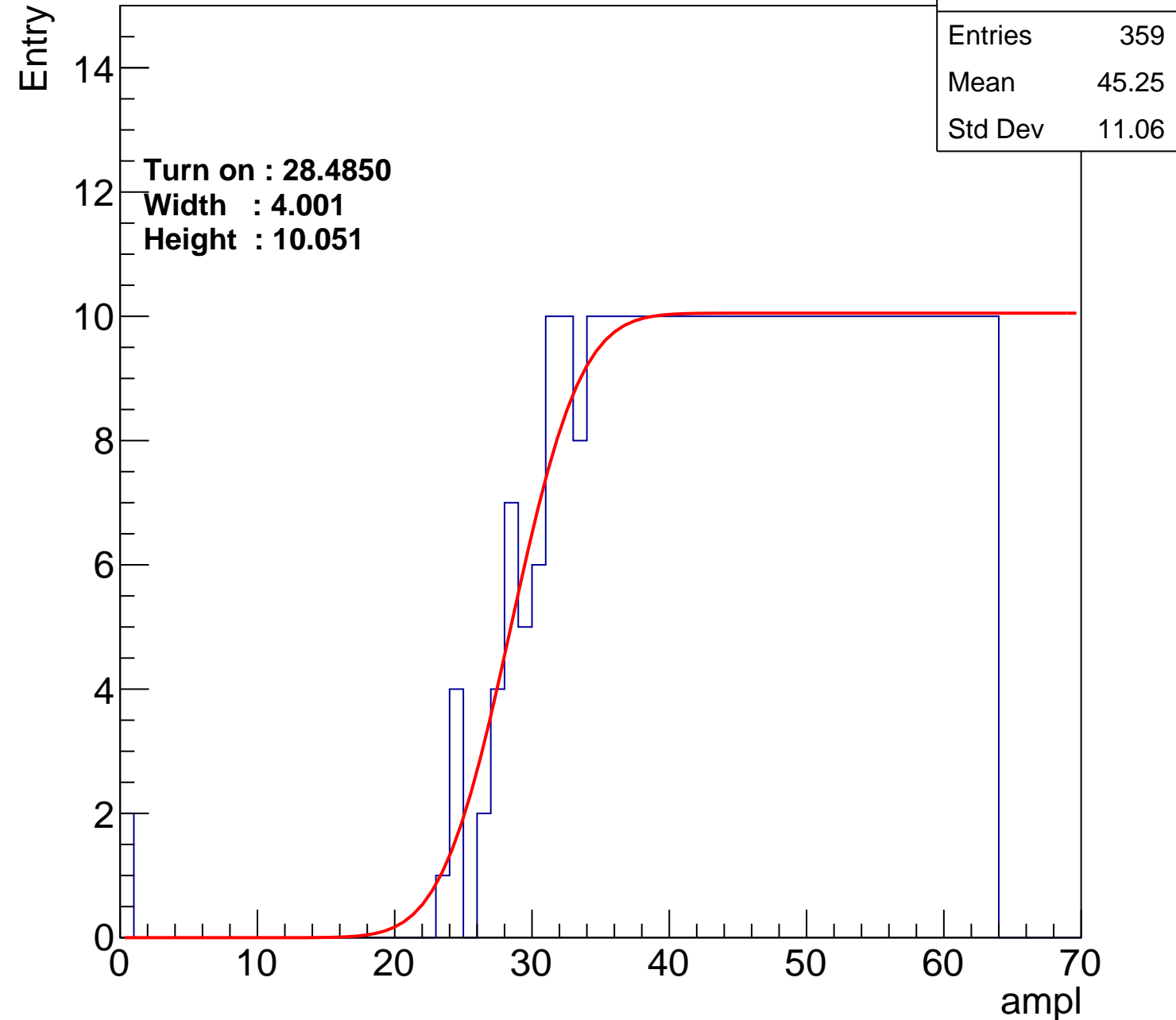
Width : 4.001

Height : 10.051

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch70

calib\_packv5\_042523\_0143.root, FC#9, port A1

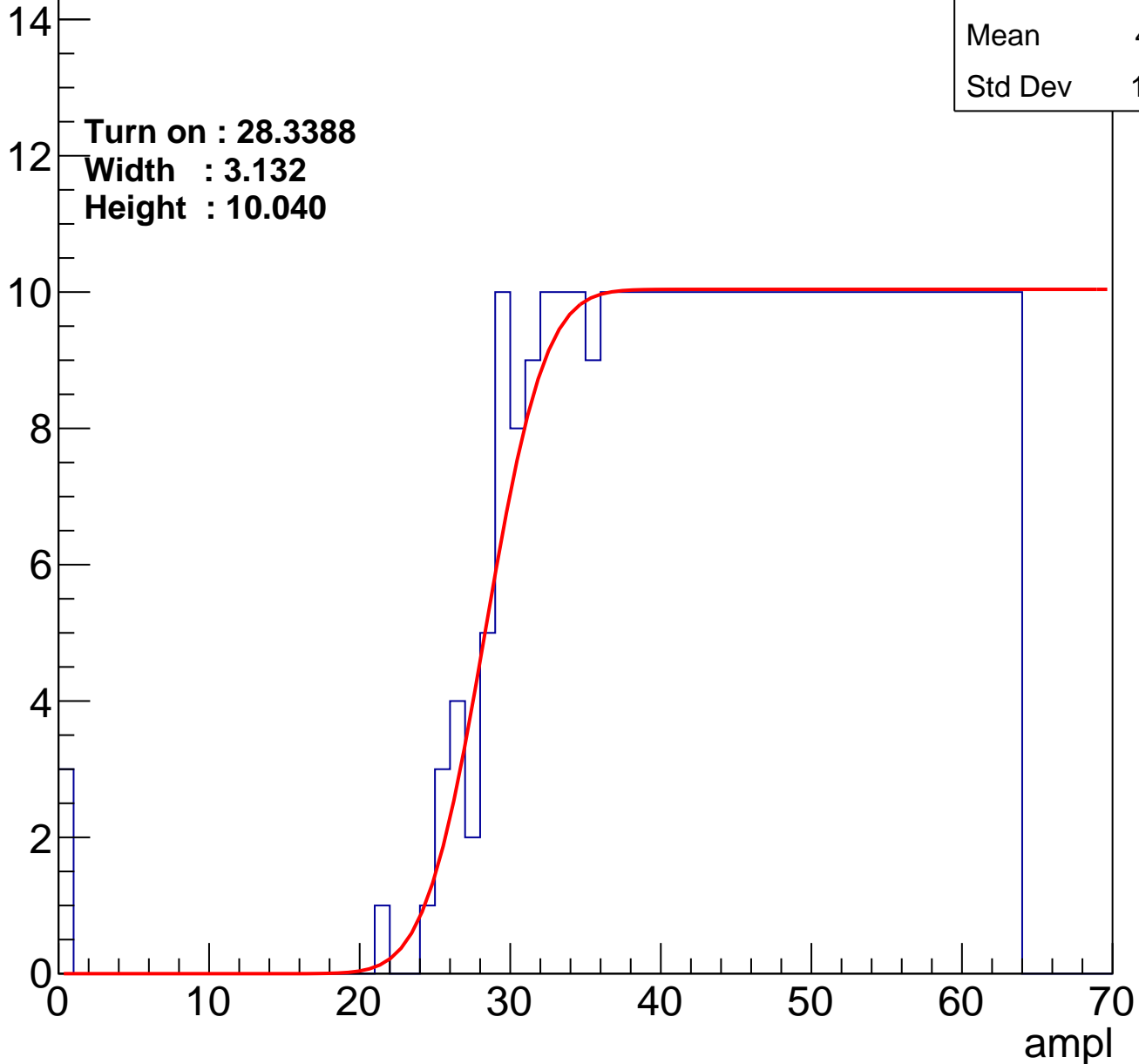
Entries	365
Mean	44.91
Std Dev	11.36

**Turn on : 28.3388**

**Width : 3.132**

**Height : 10.040**

Entry





# B0L001S, U25-ch71

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	370
Mean	44.74
Std Dev	11.29

Turn on : 27.3156

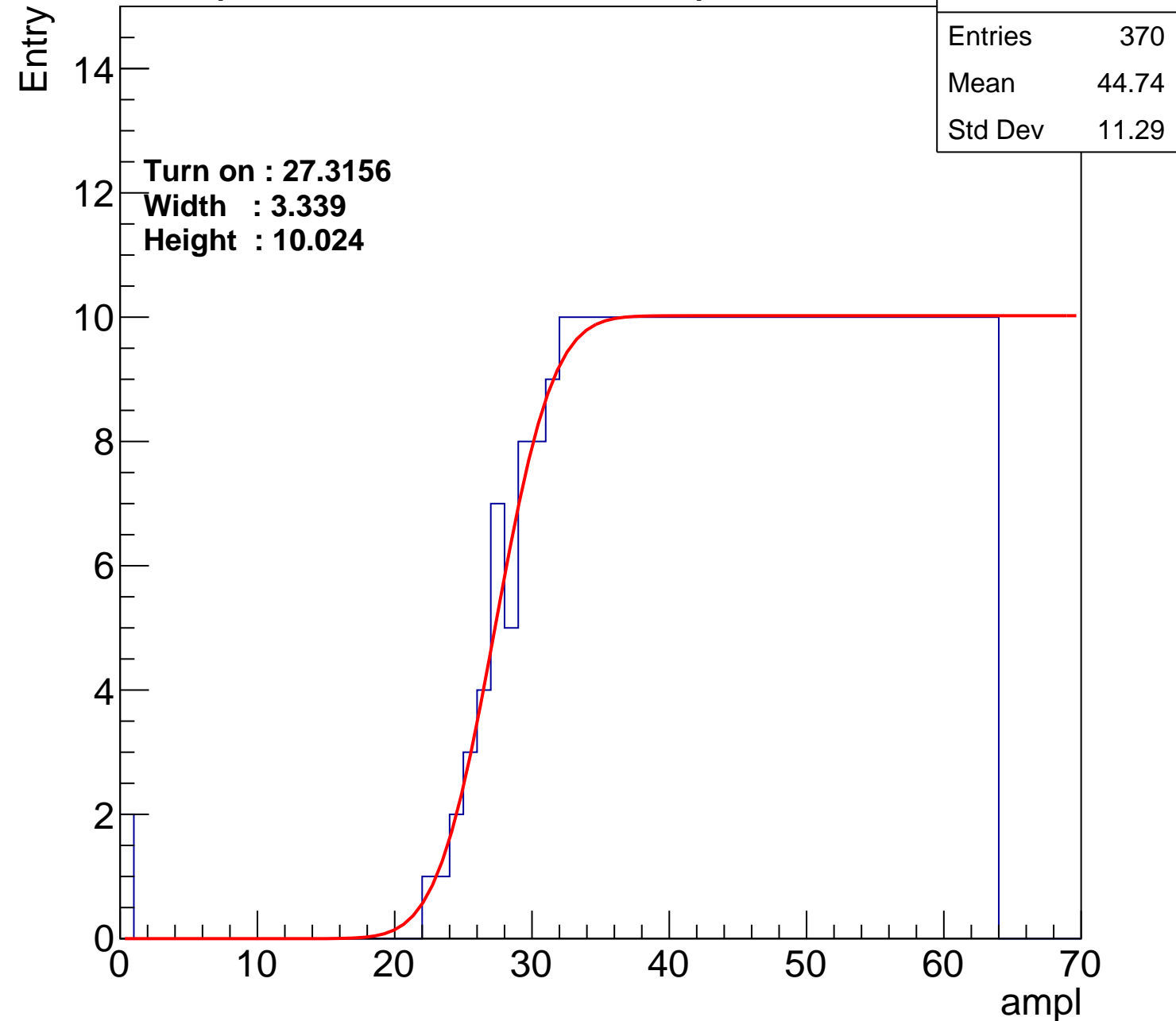
Width : 3.339

Height : 10.024

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch72

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	367
Mean	44.9
Std Dev	11.19

Turn on : 27.4090

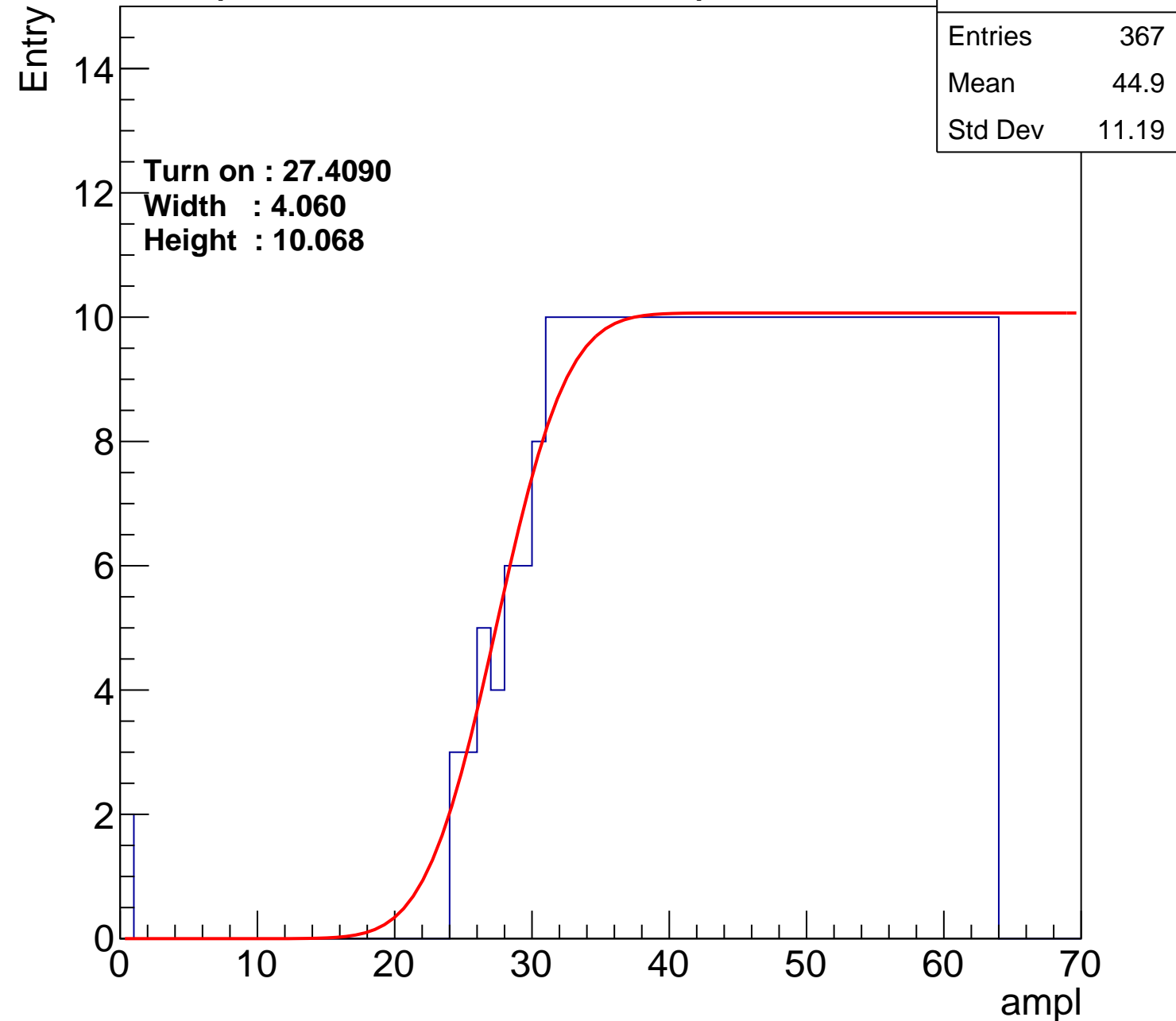
Width : 4.060

Height : 10.068

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch73

calib\_packv5\_042523\_0143.root, FC#9, port A1

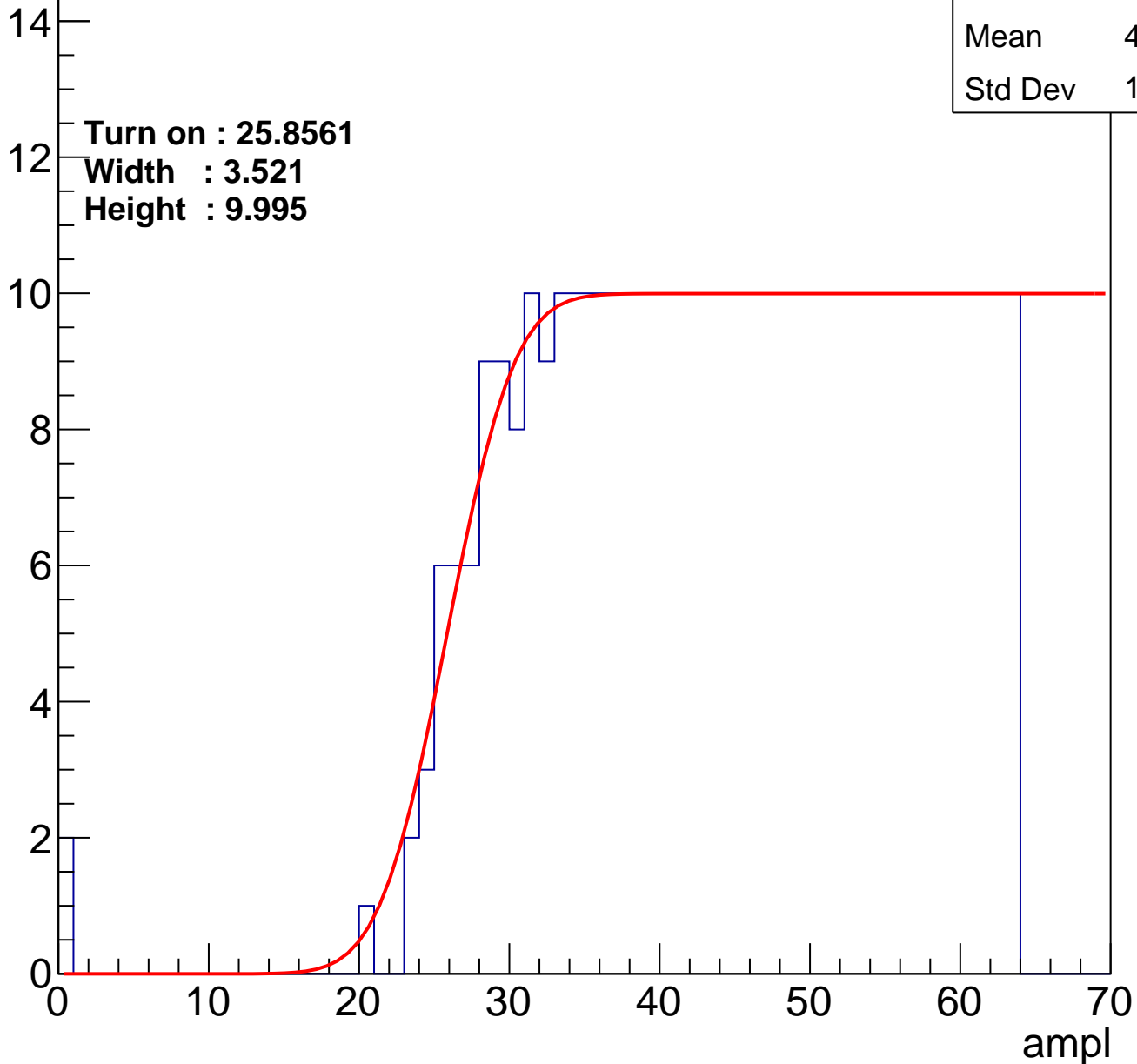
Entries	381
Mean	44.19
Std Dev	11.57

Turn on : 25.8561

Width : 3.521

Height : 9.995

Entry



# B0L001S, U25-ch74

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	356
Mean	45.45
Std Dev	10.89

**Turn on : 29.0276**

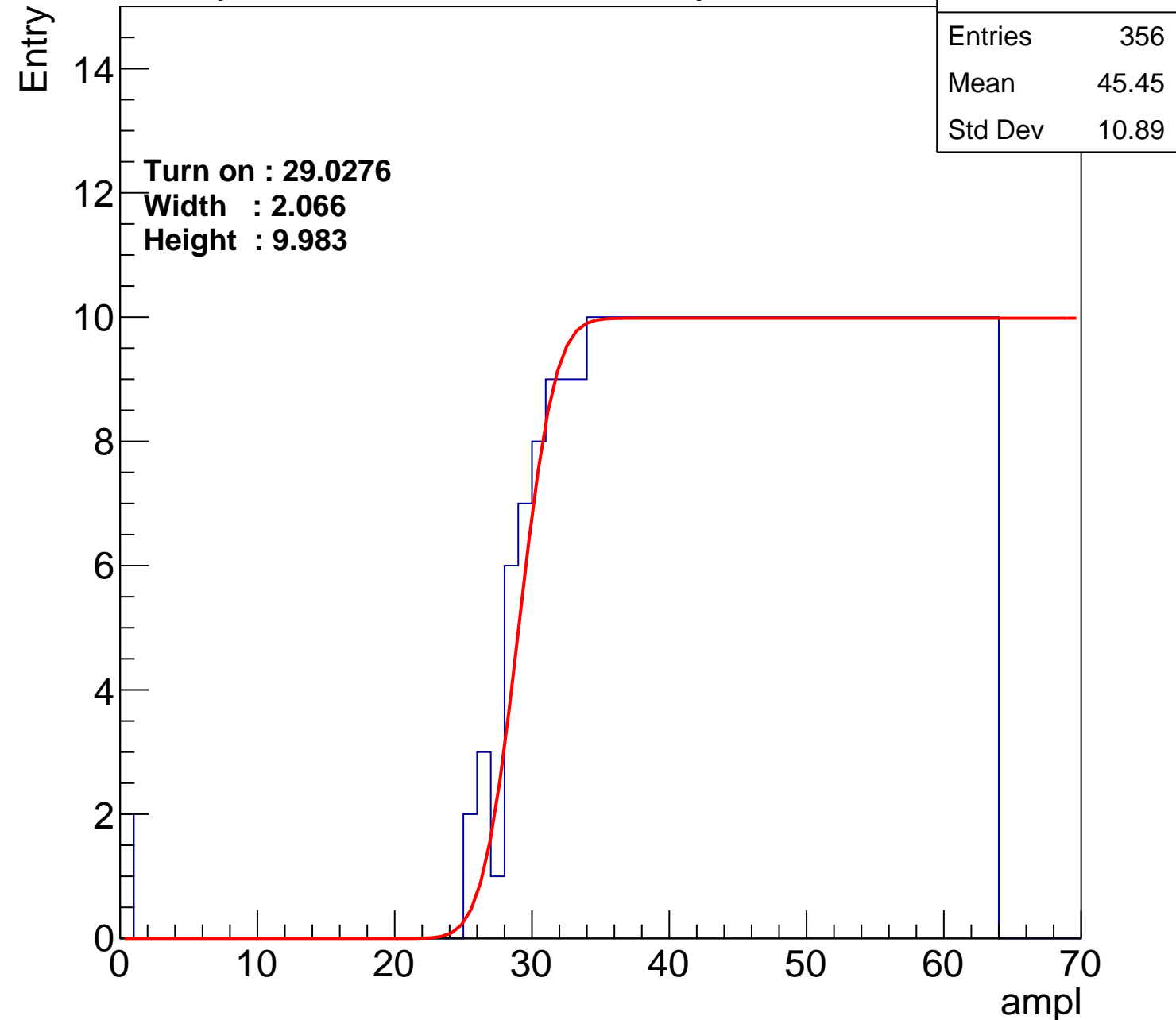
**Width : 2.066**

**Height : 9.983**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch75

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	353
Mean	45.43
Std Dev	11.29

Turn on : 28.9536

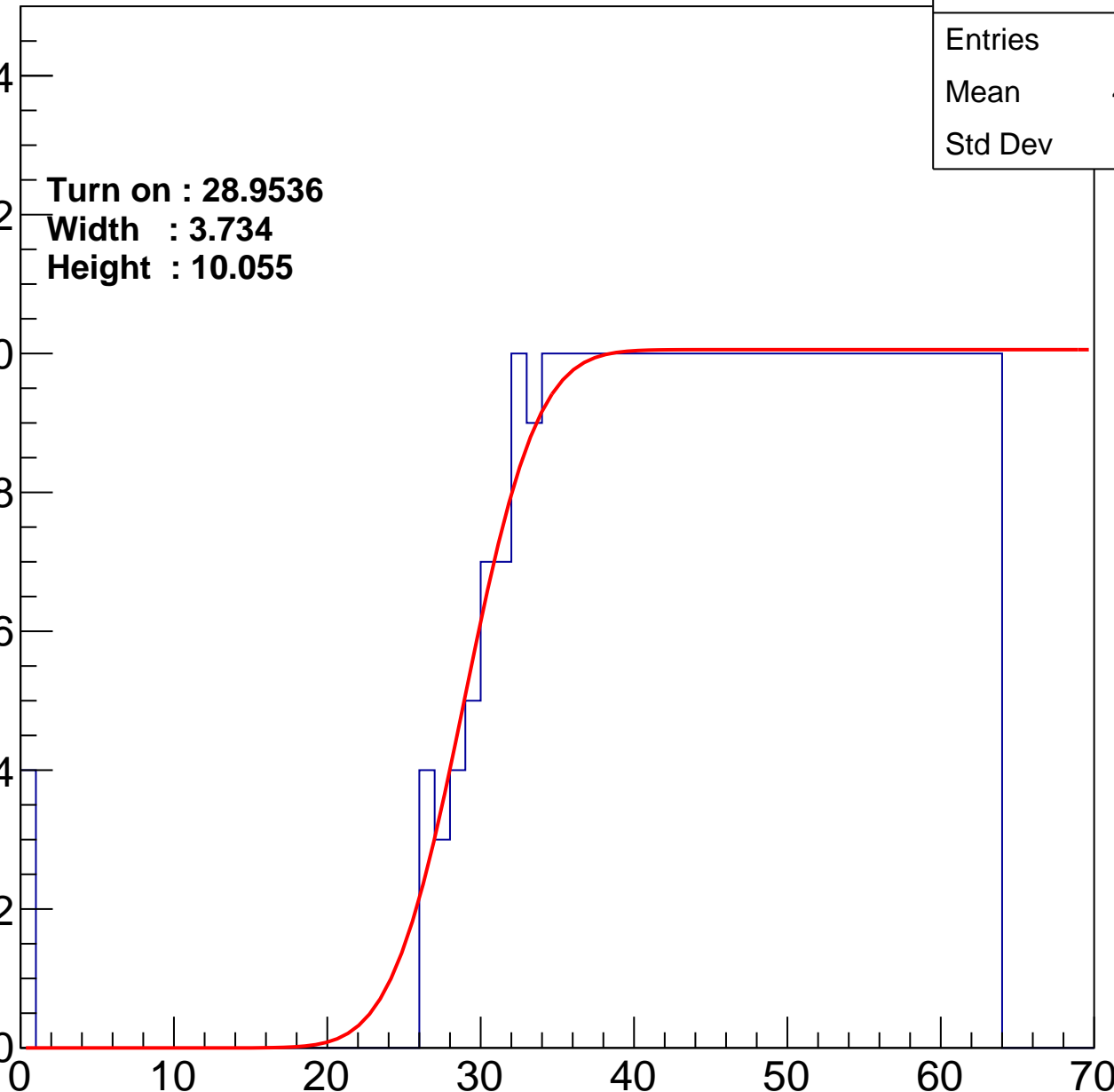
Width : 3.734

Height : 10.055

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch76

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	356
Mean	45.2
Std Dev	11.48

Turn on : 29.2666

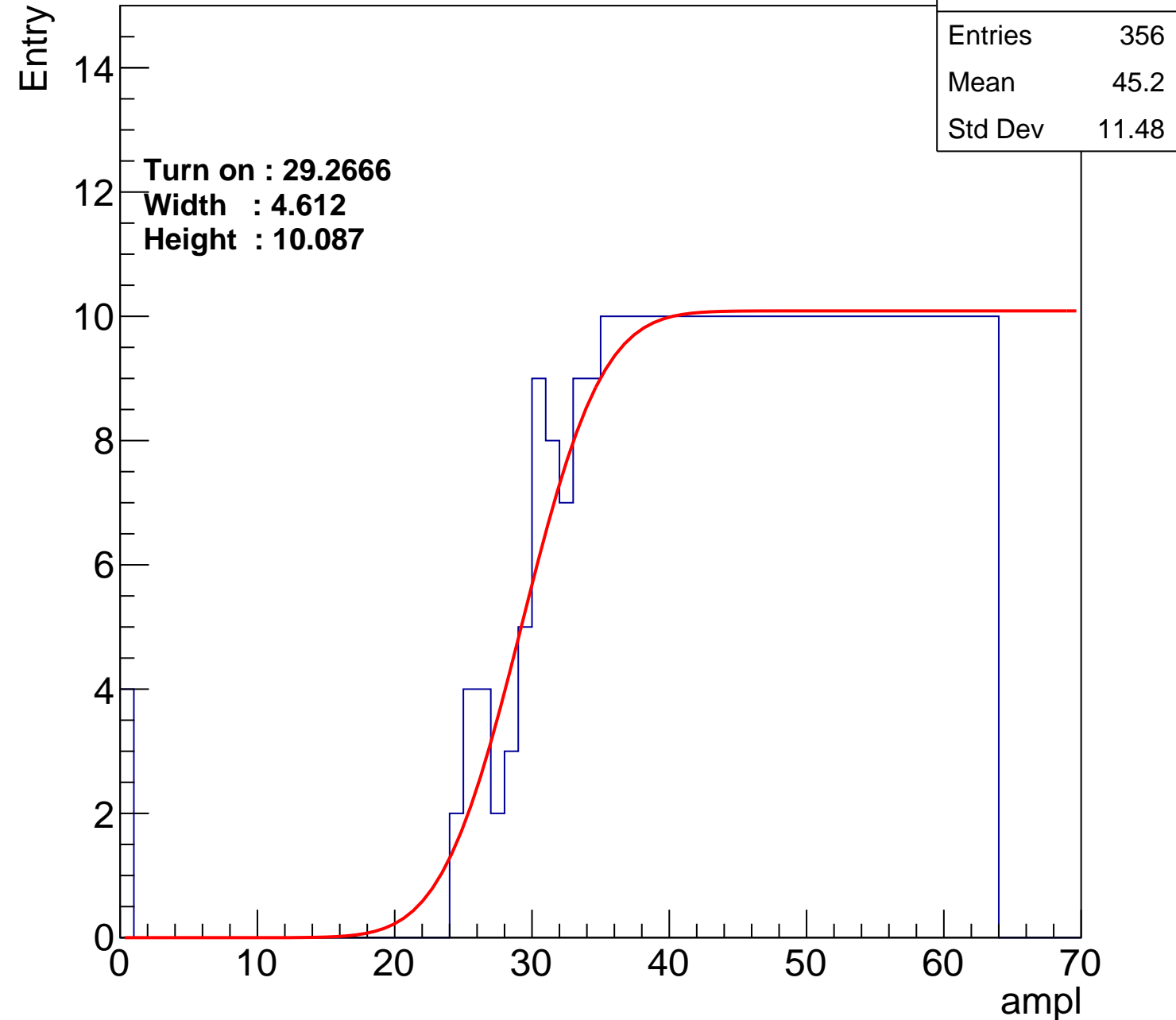
Width : 4.612

Height : 10.087

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch77

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	350
Mean	45.83
Std Dev	10.66

**Turn on : 29.7137**

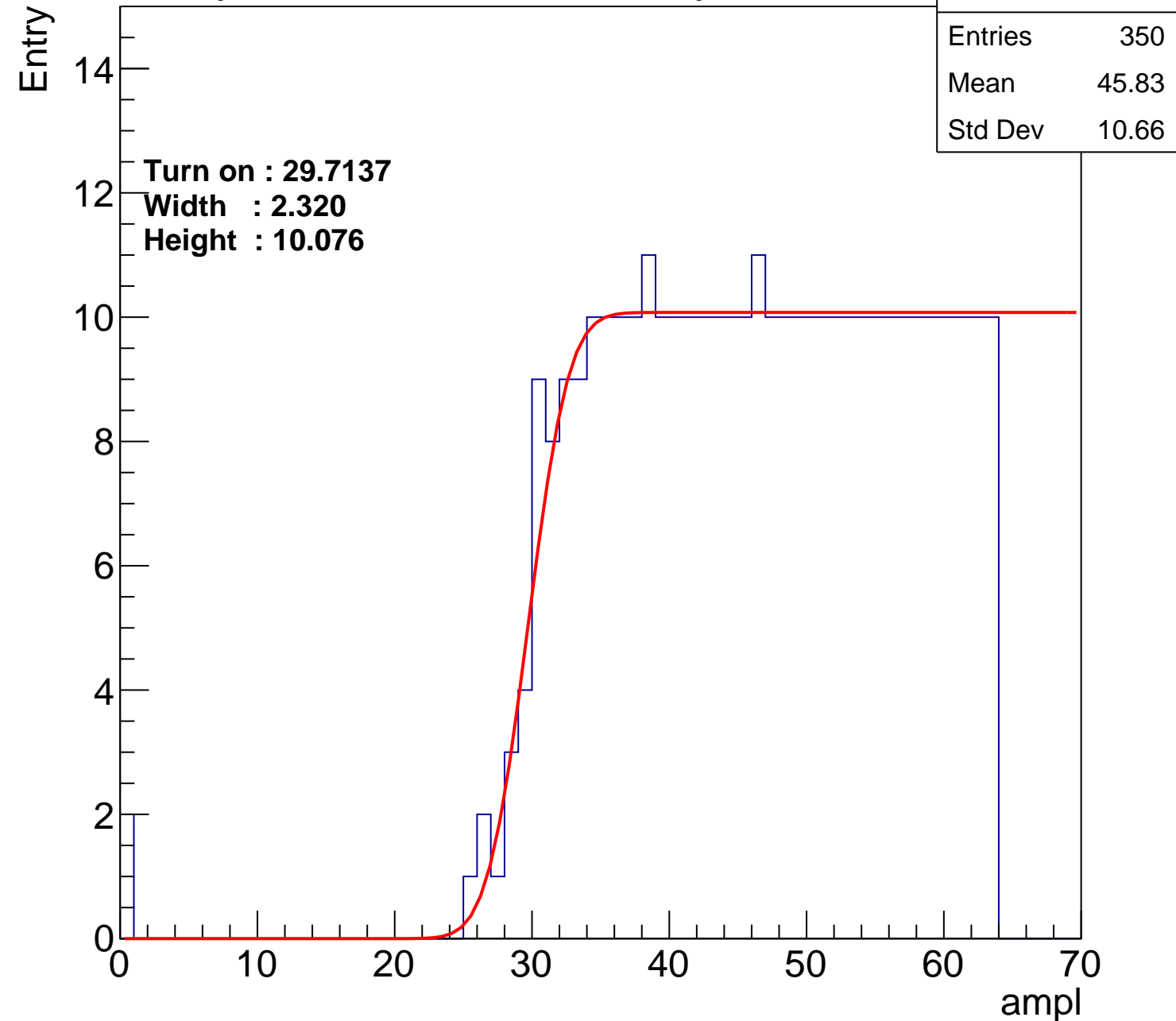
**Width : 2.320**

**Height : 10.076**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch78

calib\_packv5\_042523\_0143.root, FC#9, port A1

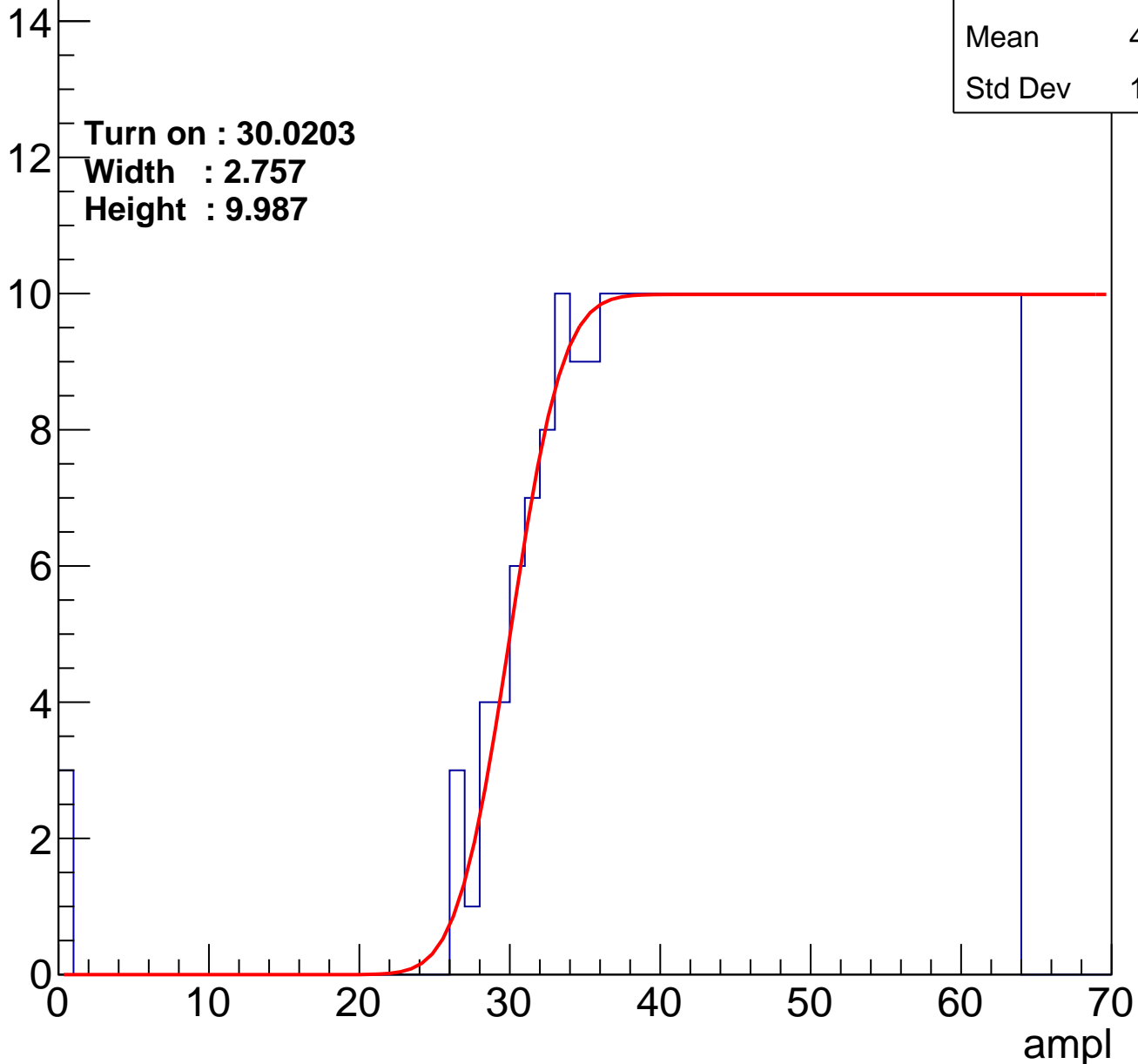
Entries	344
Mean	45.92
Std Dev	10.89

Turn on : 30.0203

Width : 2.757

Height : 9.987

Entry





# B0L001S, U25-ch79

calib\_packv5\_042523\_0143.root, FC#9, port A1

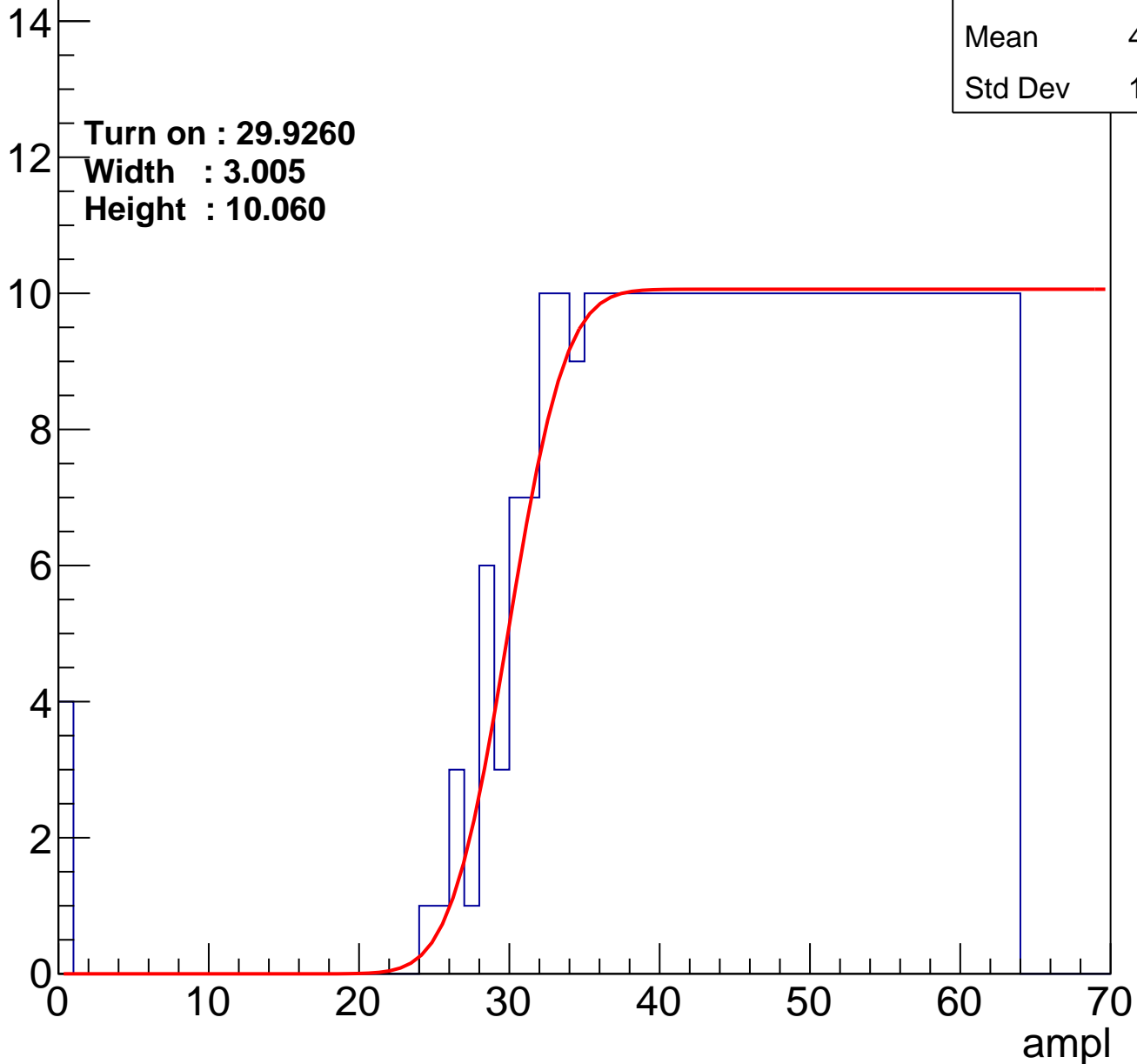
Entries	352
Mean	45.46
Std Dev	11.29

Turn on : 29.9260

Width : 3.005

Height : 10.060

Entry



# B0L001S, U25-ch80

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	370
Mean	44.46
Std Dev	12.04

Turn on : 27.8984

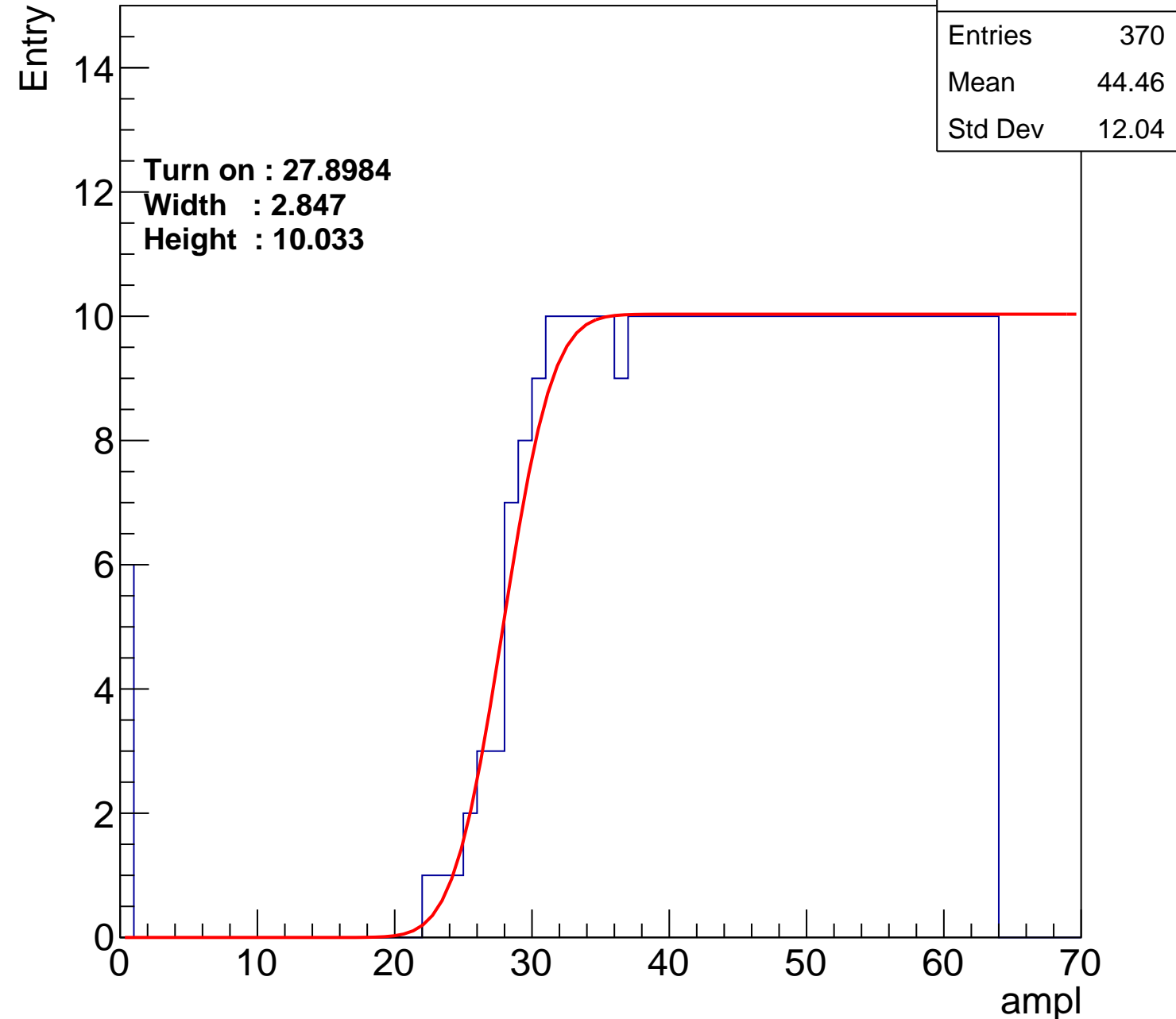
Width : 2.847

Height : 10.033

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch81

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	367
Mean	44.97
Std Dev	10.99

Turn on : 27.8648

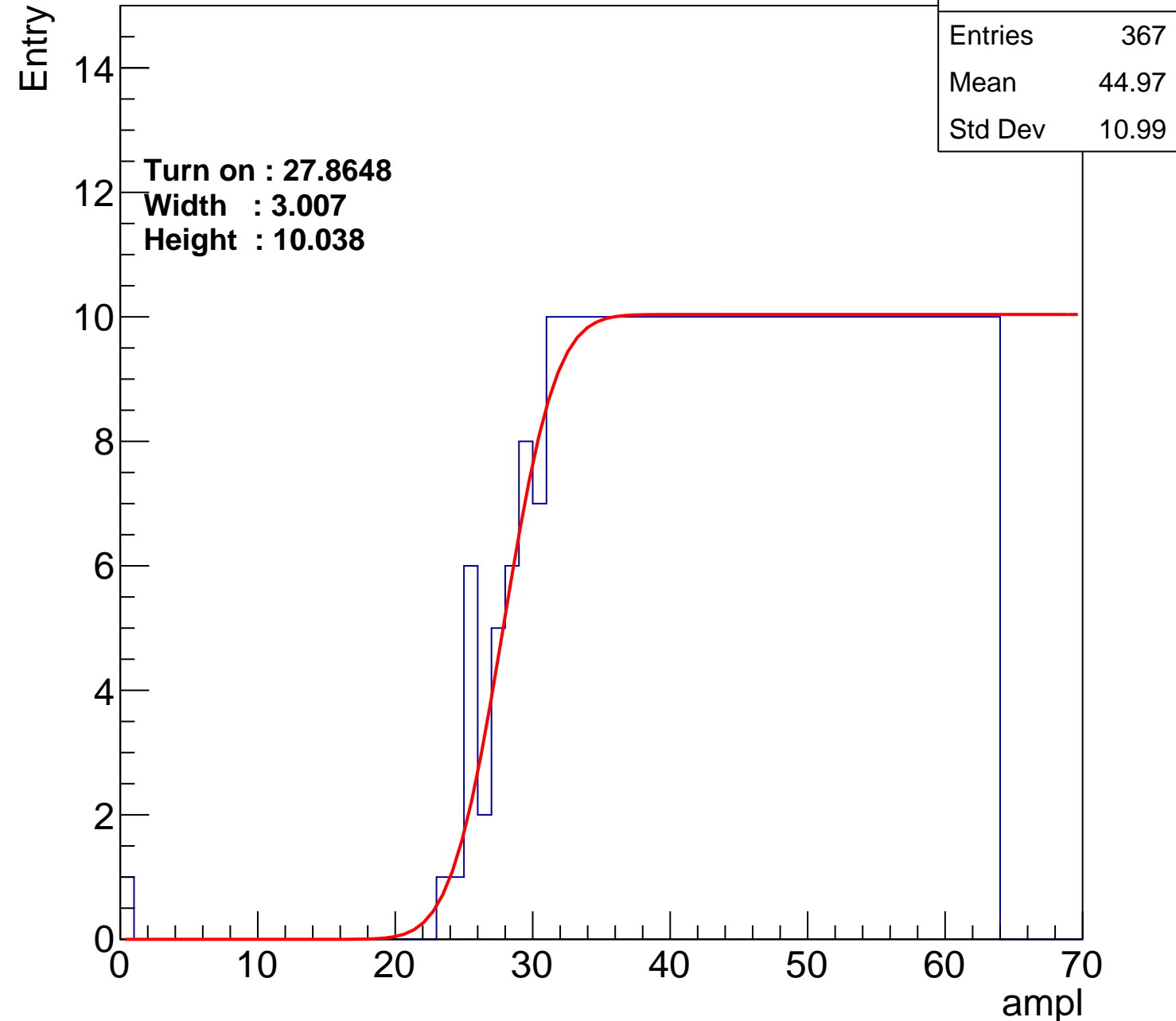
Width : 3.007

Height : 10.038

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch82

calib\_packv5\_042523\_0143.root, FC#9, port A1

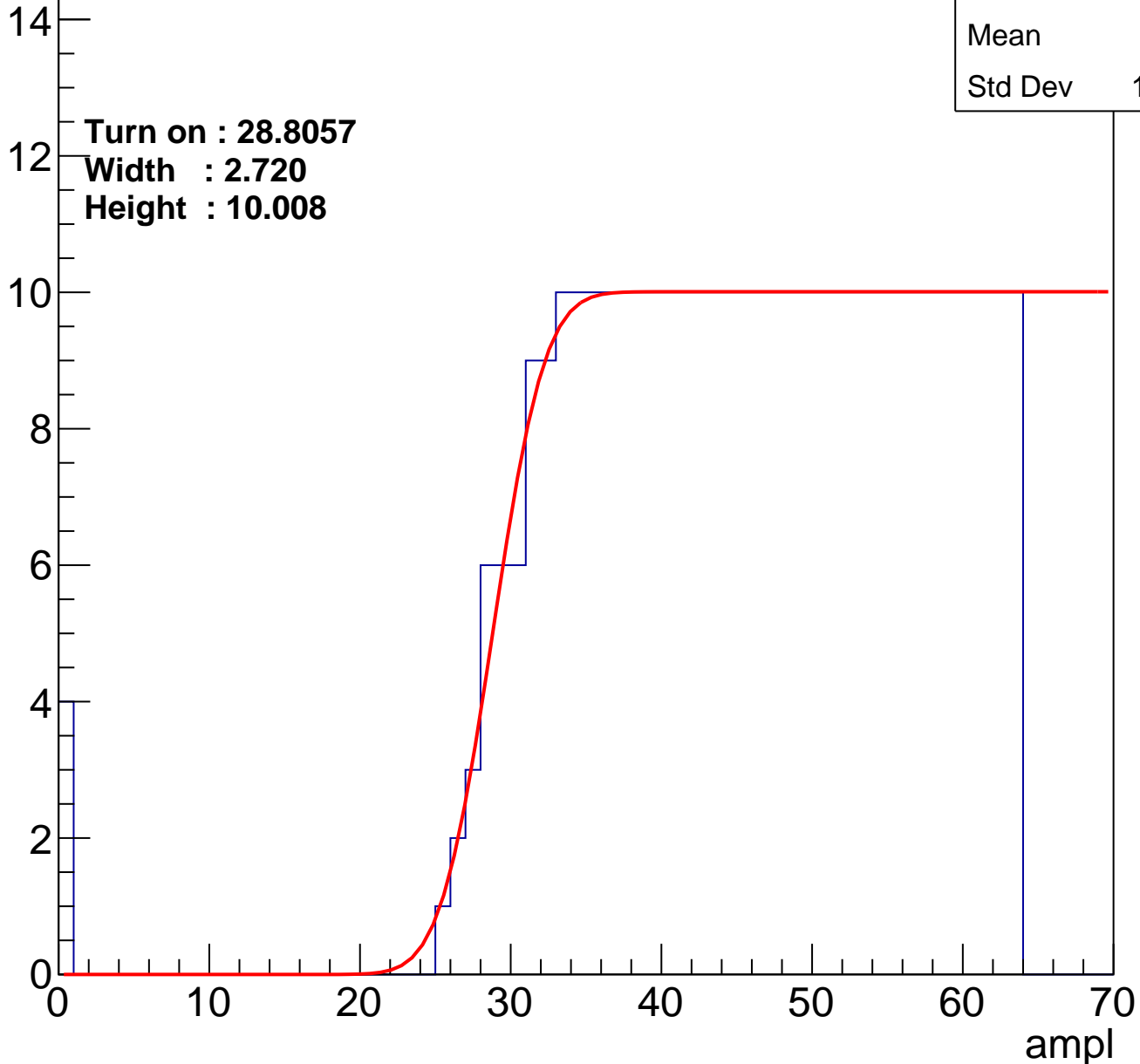
Entries	356
Mean	45.3
Std Dev	11.32

**Turn on : 28.8057**

**Width : 2.720**

**Height : 10.008**

Entry



# B0L001S, U25-ch83

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	381
Mean	44.22
Std Dev	11.53

**Turn on : 26.2404**

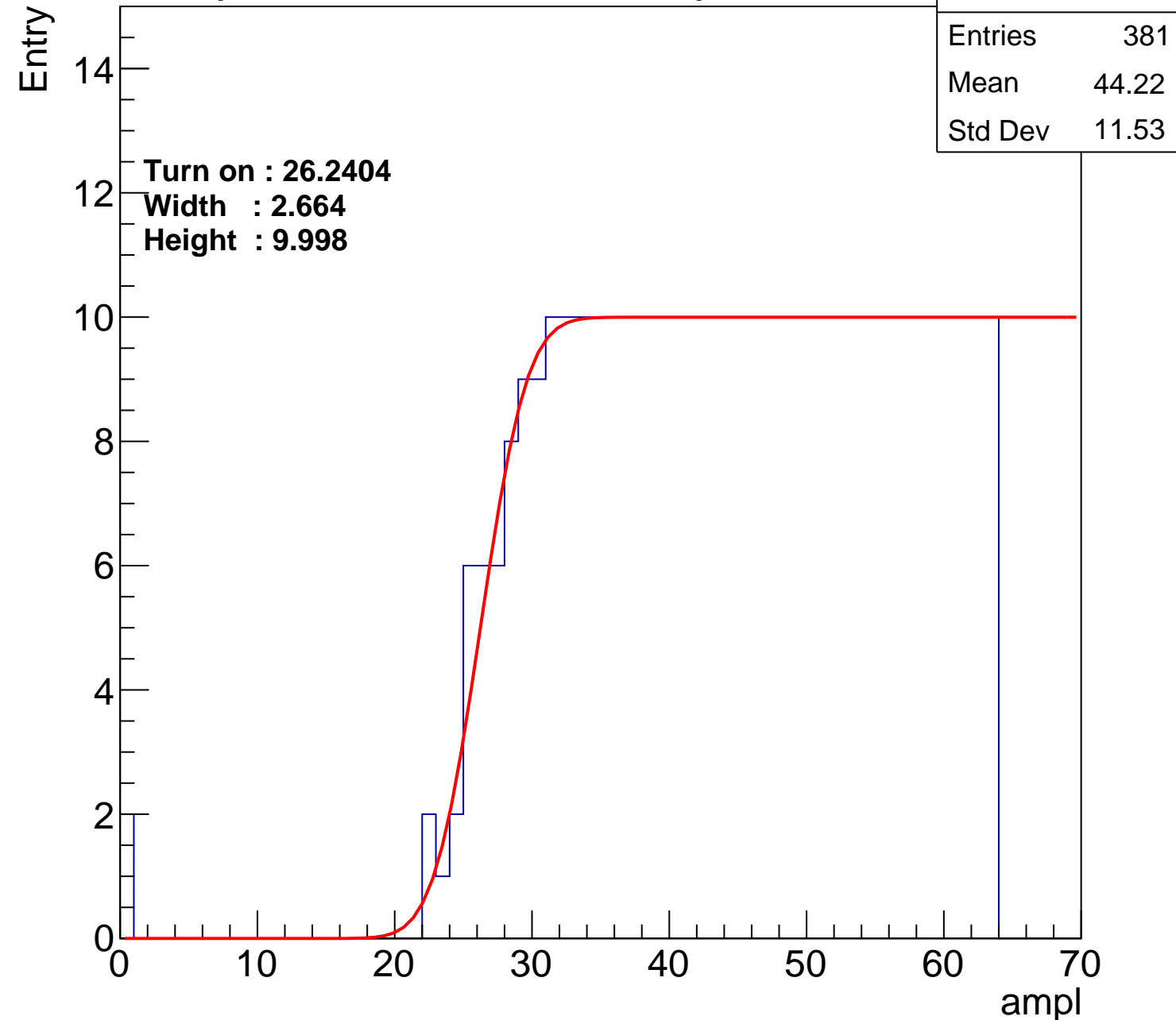
**Width : 2.664**

**Height : 9.998**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch84

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	372
Mean	44.74
Std Dev	11.1

Turn on : 27.1118

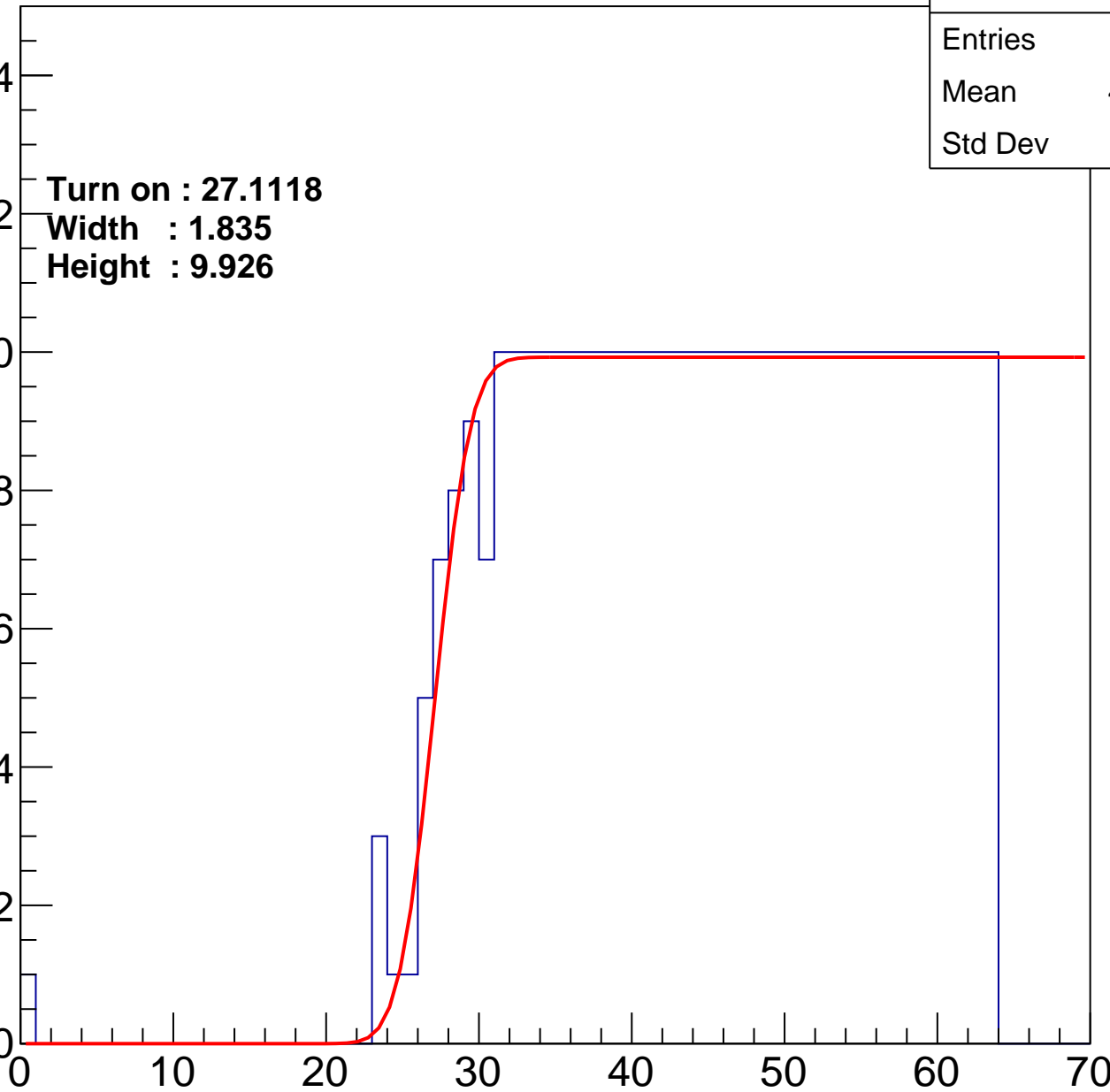
Width : 1.835

Height : 9.926

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch85

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	369
Mean	44.63
Std Dev	11.67

Turn on : 27.5417

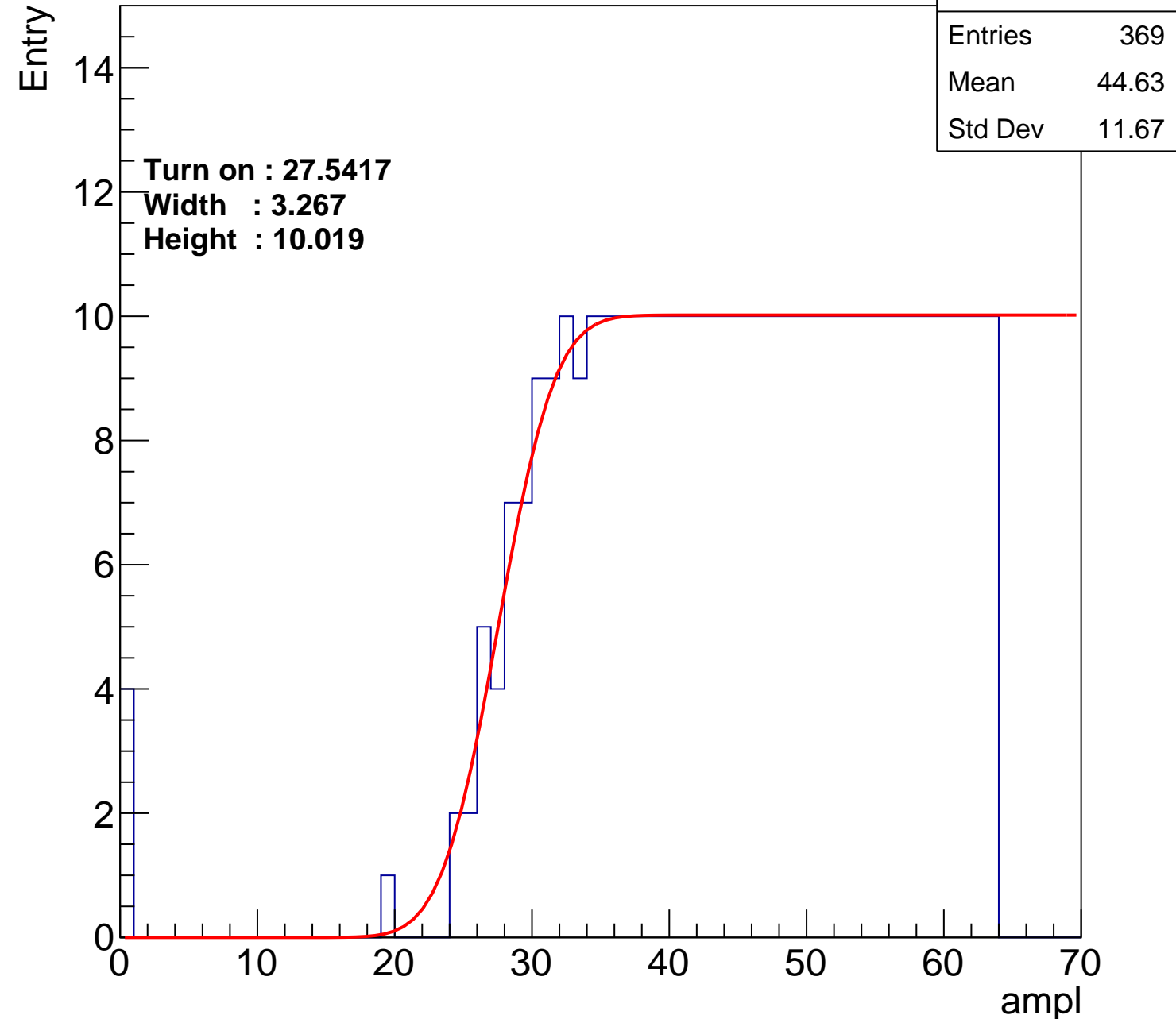
Width : 3.267

Height : 10.019

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch86

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	356
Mean	45.41
Std Dev	10.95

**Turn on : 28.7759**

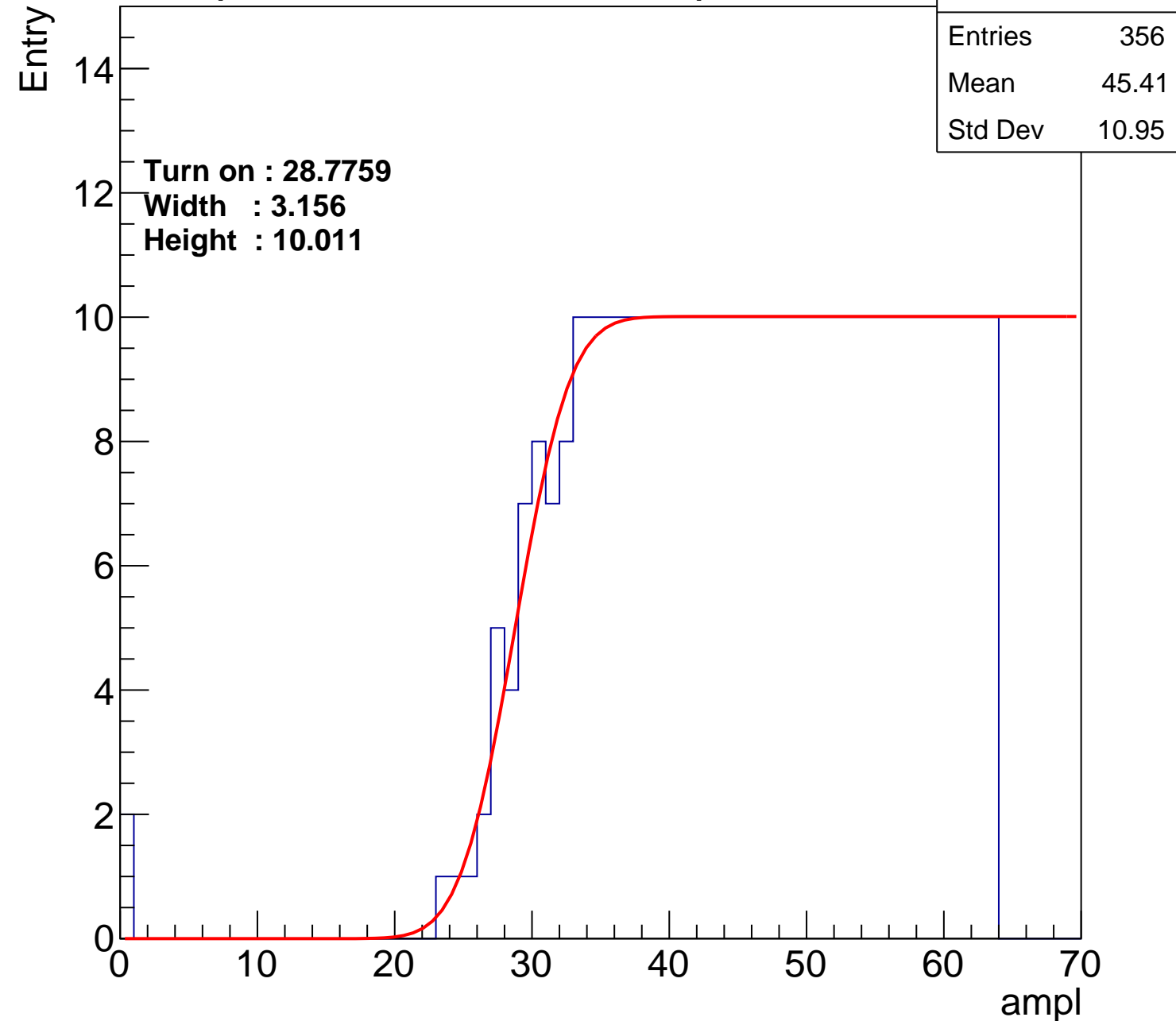
**Width : 3.156**

**Height : 10.011**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U25-ch87

calib\_packv5\_042523\_0143.root, FC#9, port A1

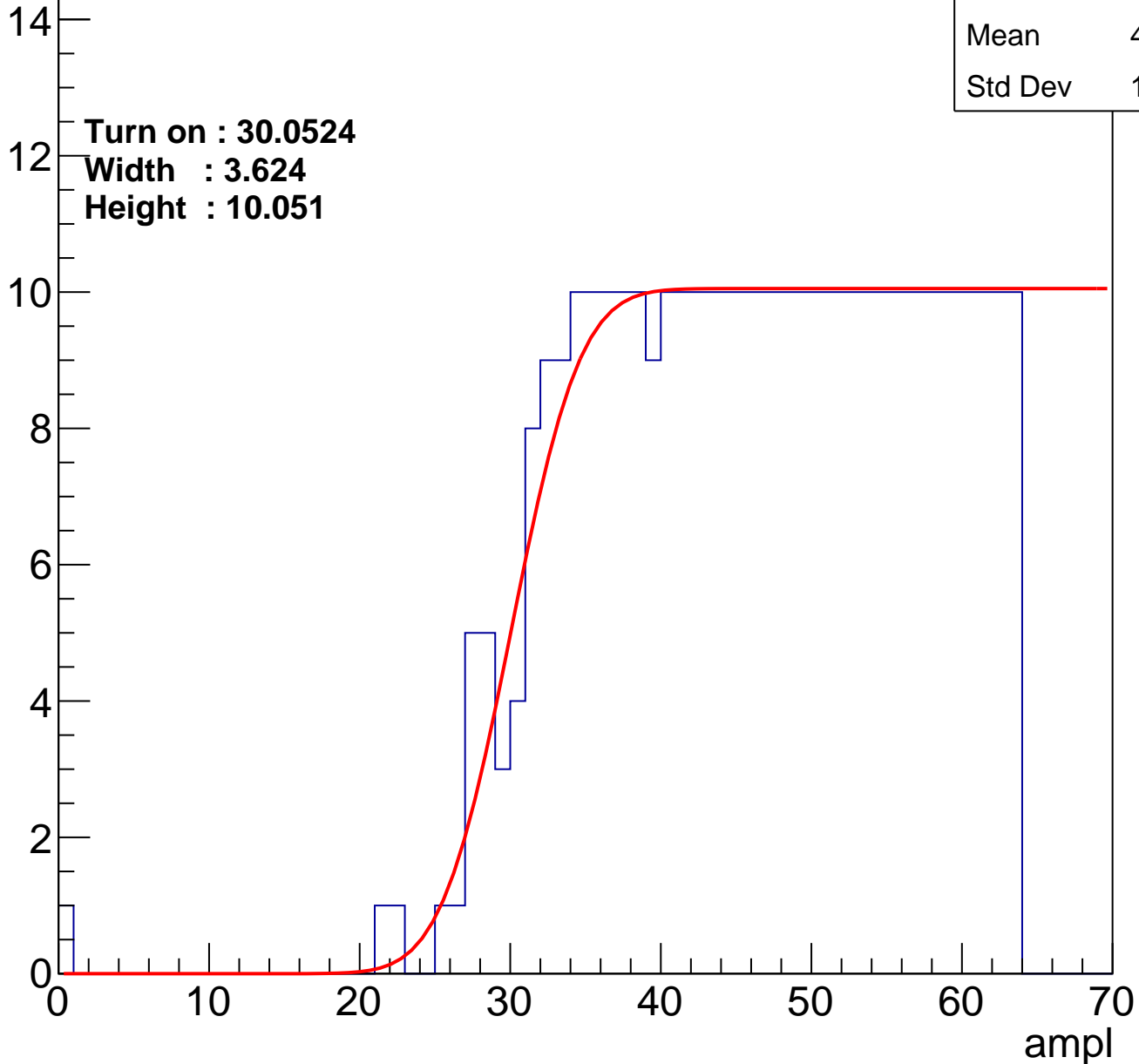
Entries	347
Mean	45.88
Std Dev	10.58

Turn on : 30.0524

Width : 3.624

Height : 10.051

Entry



# B0L001S, U25-ch88

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	374
Mean	44.46
Std Dev	11.84

Turn on : 27.6062

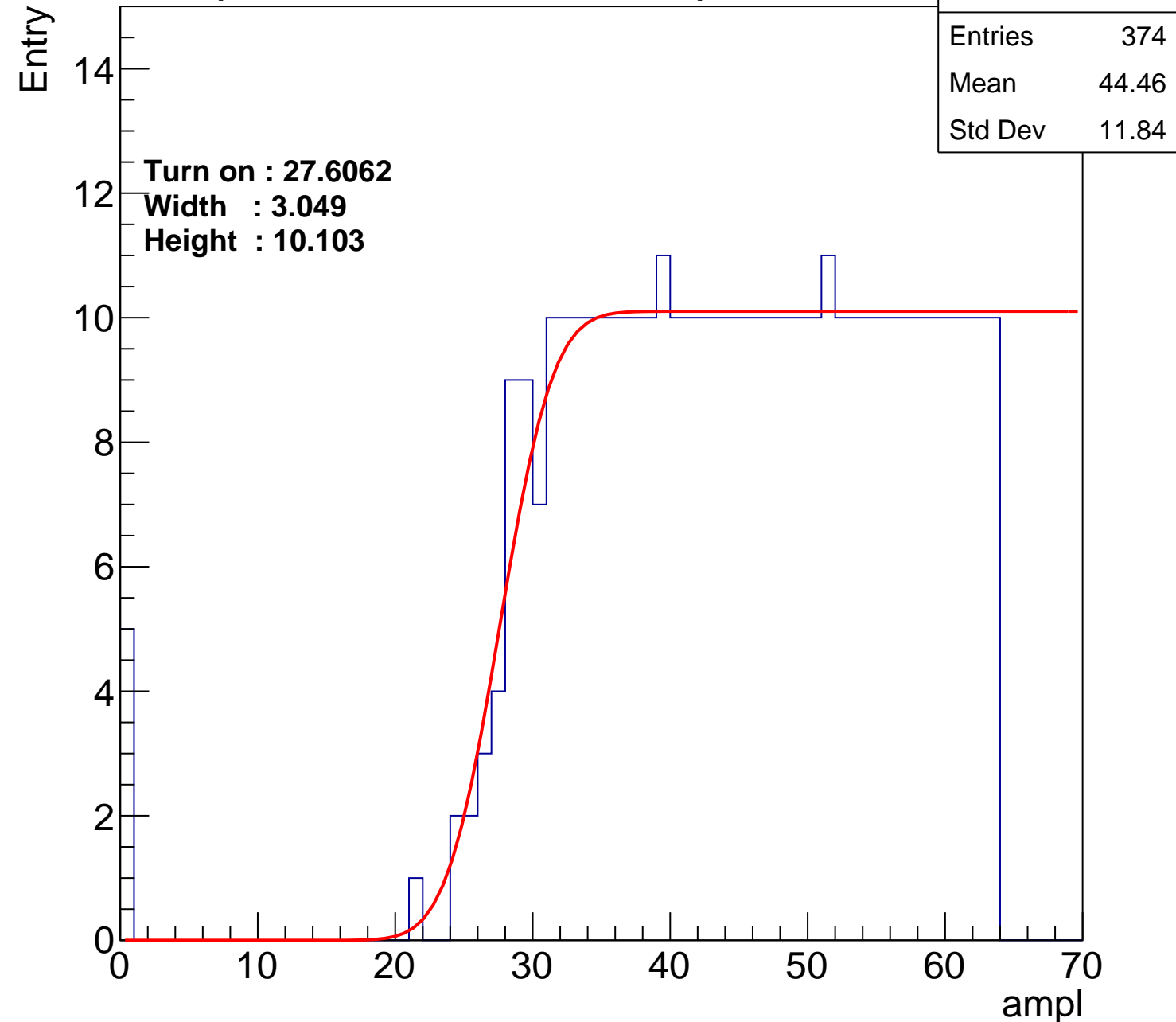
Width : 3.049

Height : 10.103

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



**calib\_packv5\_042523\_0143.root, FC#9, port A1**

Entries	357
Mean	45.43
Std Dev	10.78

Std Dev	10.78
---------	-------

**Height : 10.018**

0

70

ampl

# B0L001S, U25-ch90

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	357
Mean	45.35
Std Dev	11

**Turn on : 29.1453**

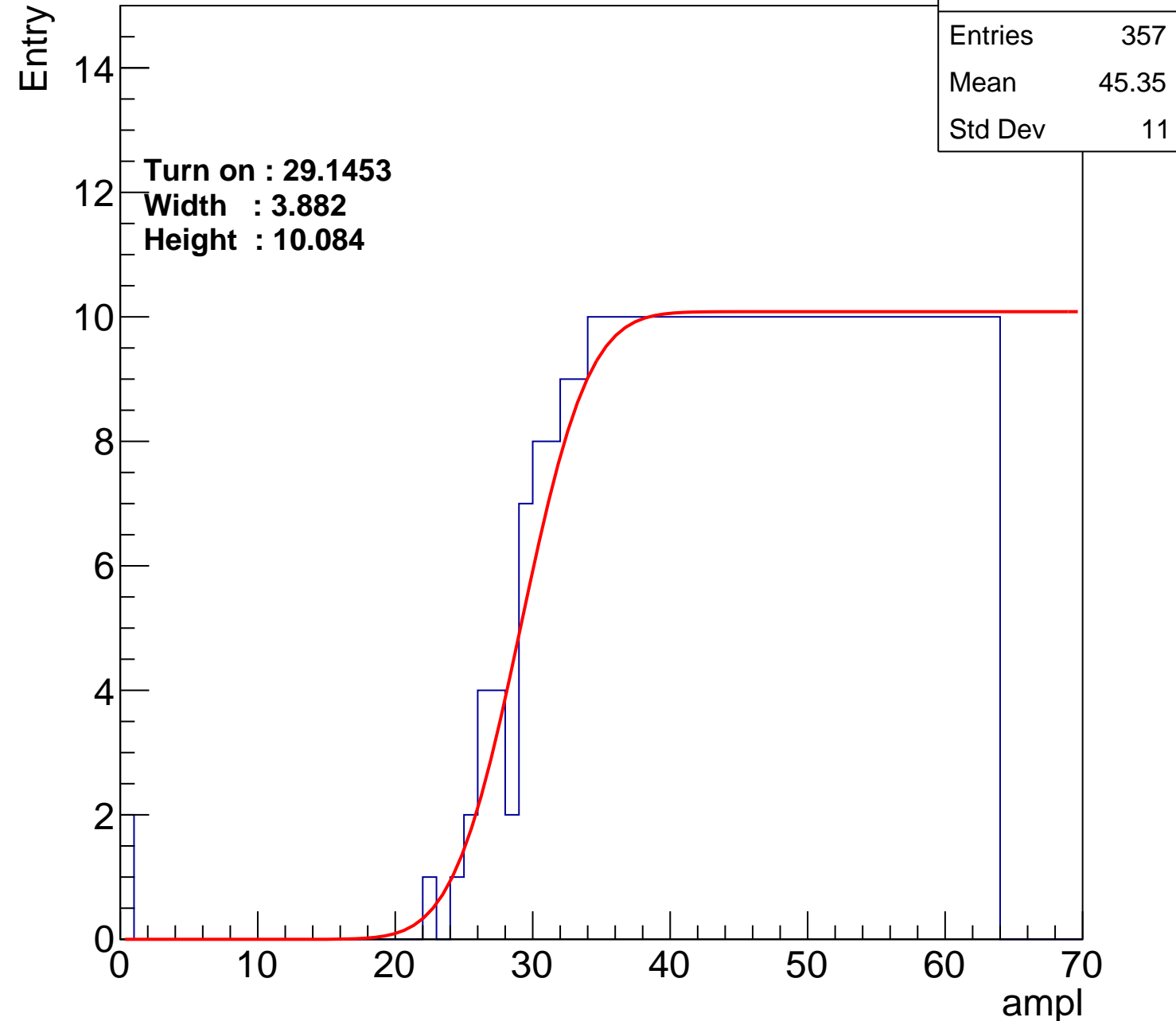
**Width : 3.882**

**Height : 10.084**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch91

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	345
Mean	45.92
Std Dev	10.85

**Turn on : 29.9158**

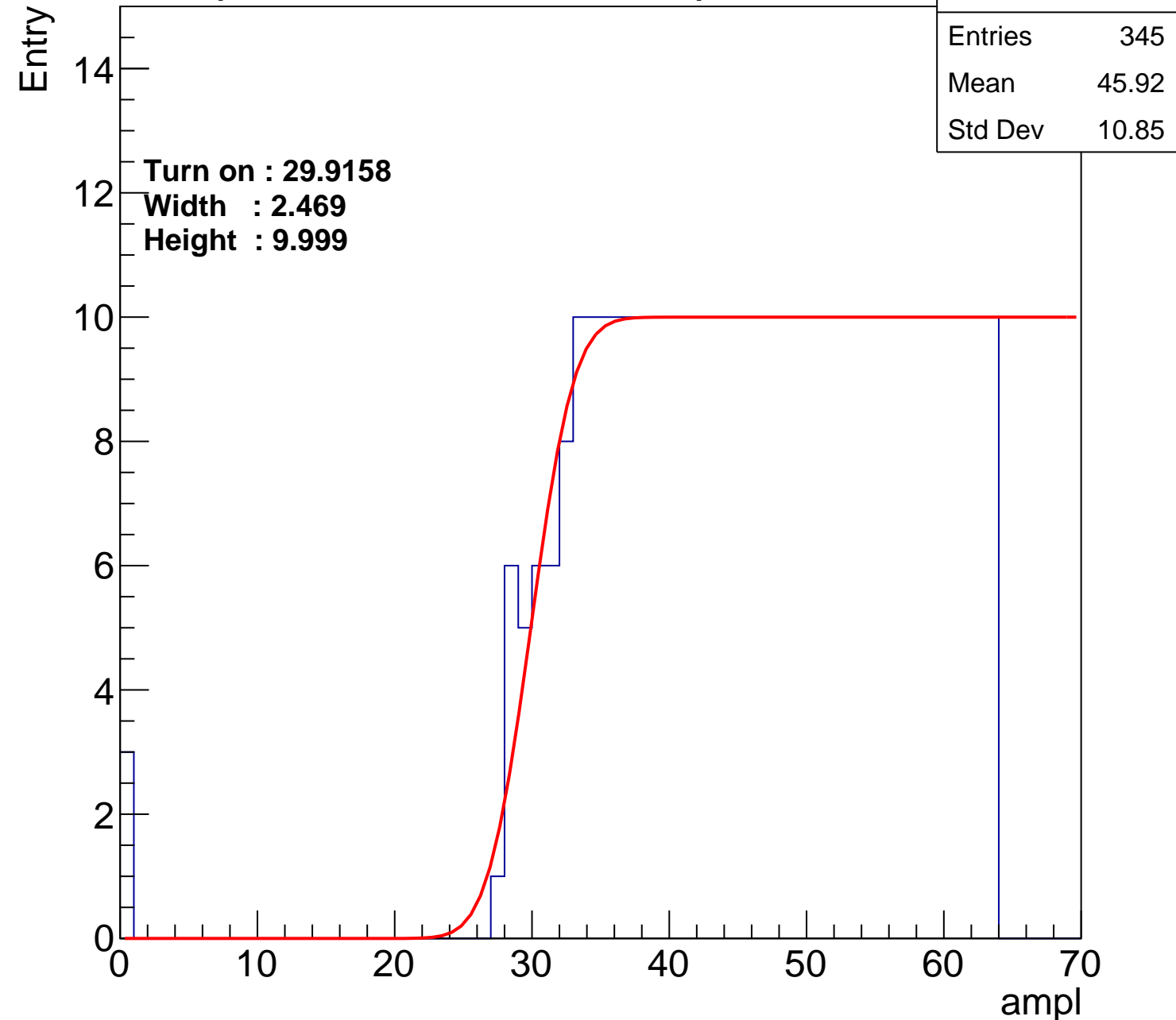
**Width : 2.469**

**Height : 9.999**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch92

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	359
Mean	45.26
Std Dev	11.14

Turn on : 28.5658

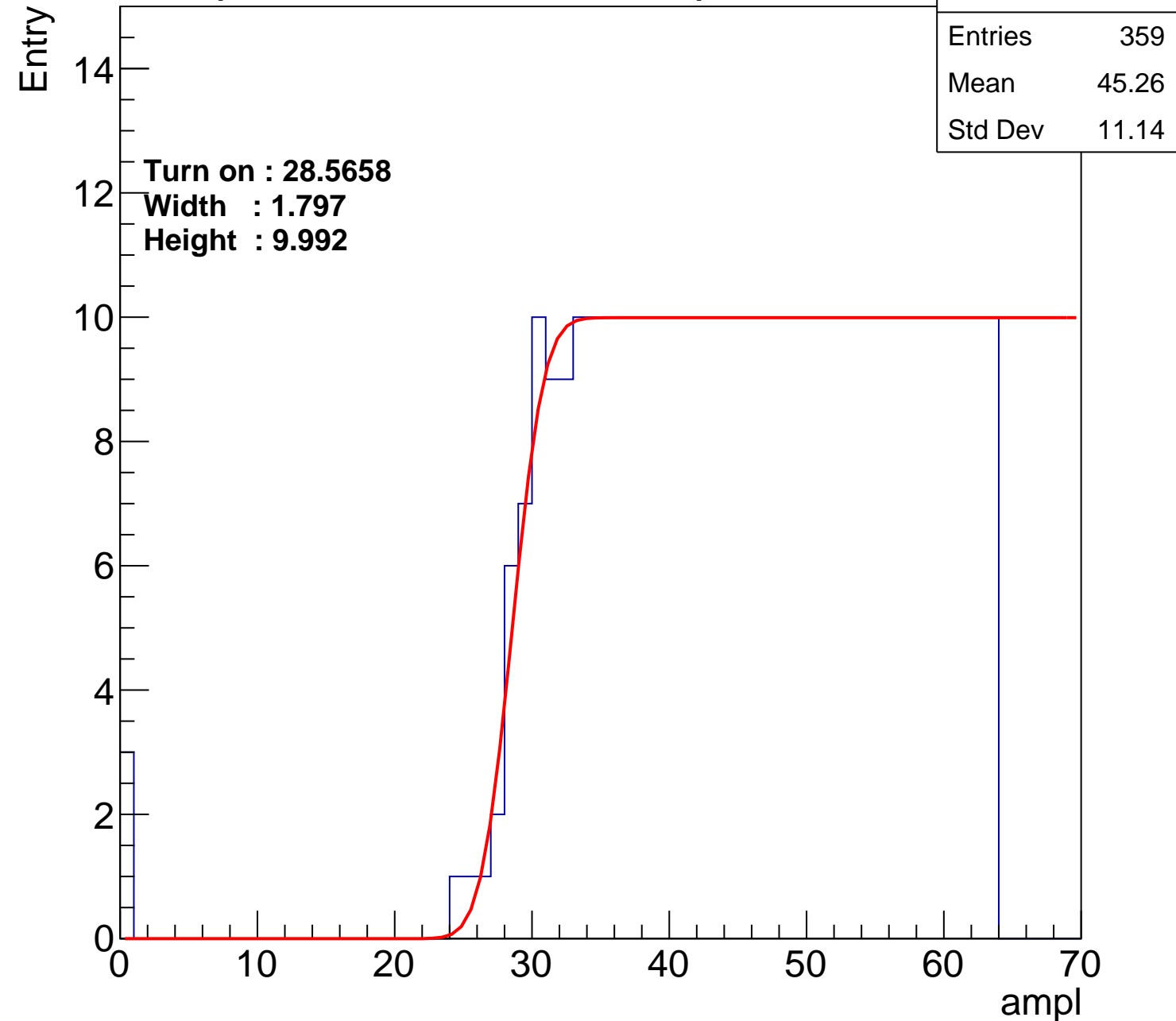
Width : 1.797

Height : 9.992

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch93

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	370
Mean	44.79
Std Dev	11.29

Turn on : 27.7869

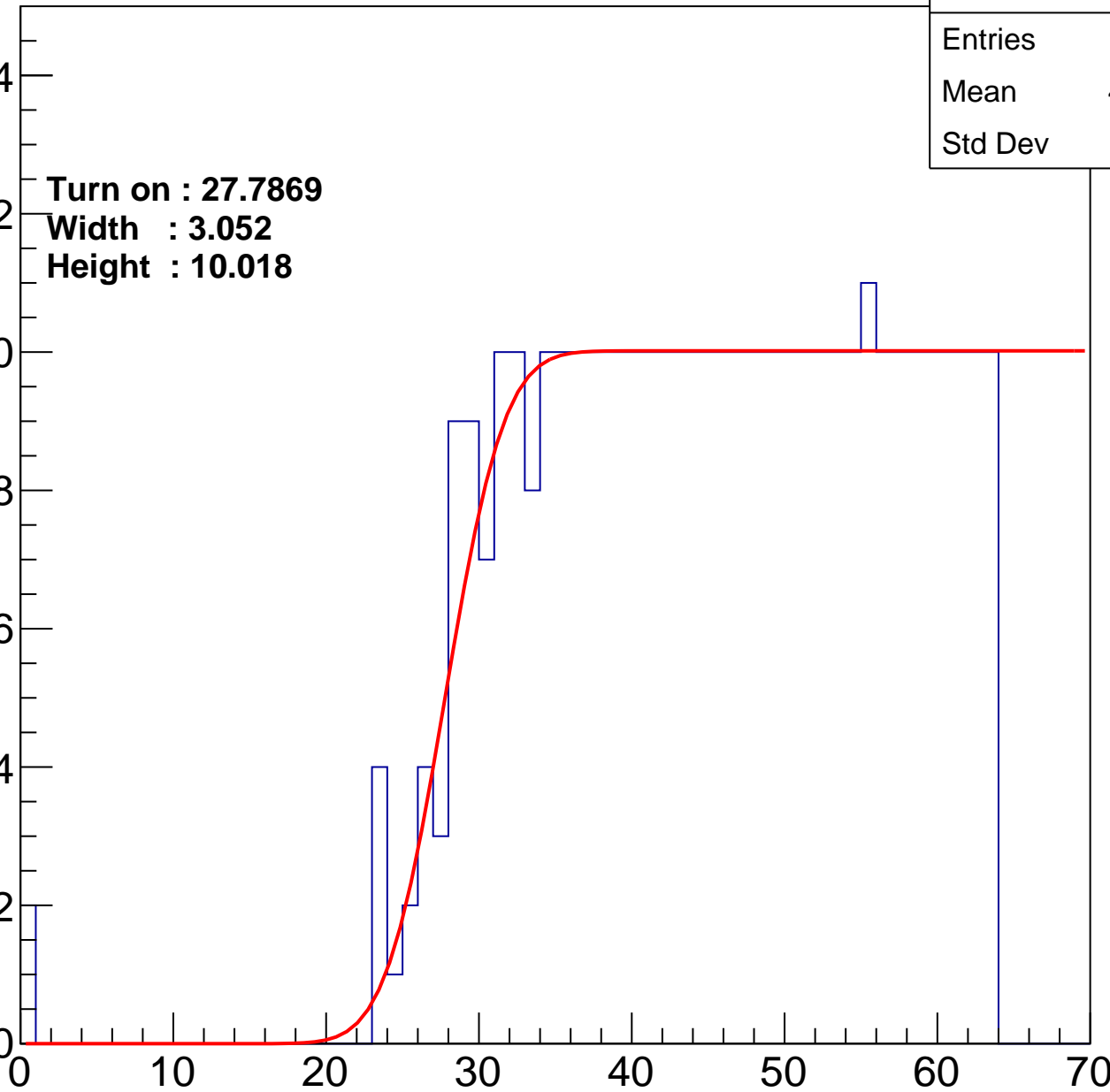
Width : 3.052

Height : 10.018

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch94

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	358
Mean	45.1
Std Dev	11.62

Turn on : 29.1527

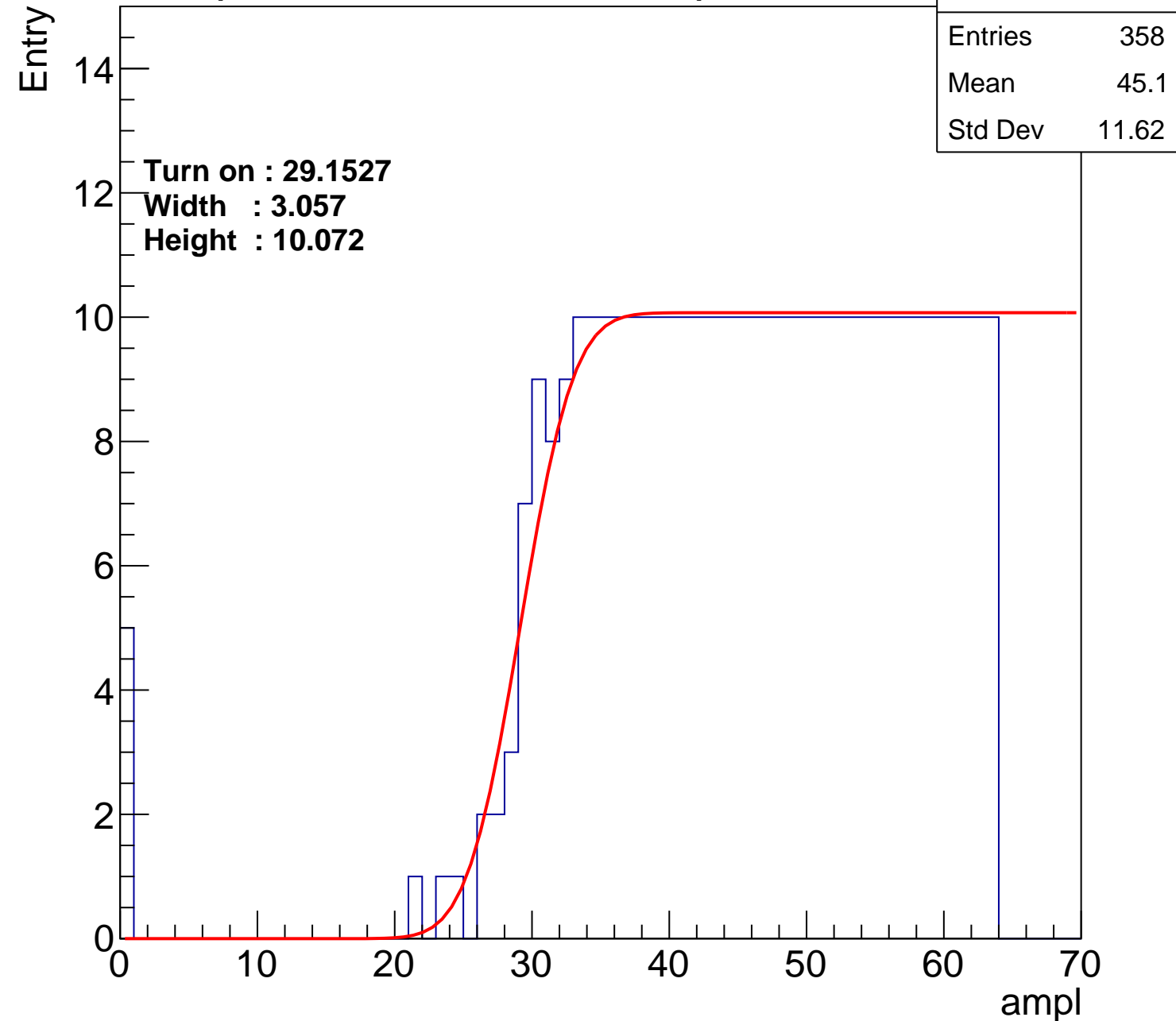
Width : 3.057

Height : 10.072

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U25-ch95

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	383
Mean	43.89
Std Dev	12.15

Turn on : 26.2897

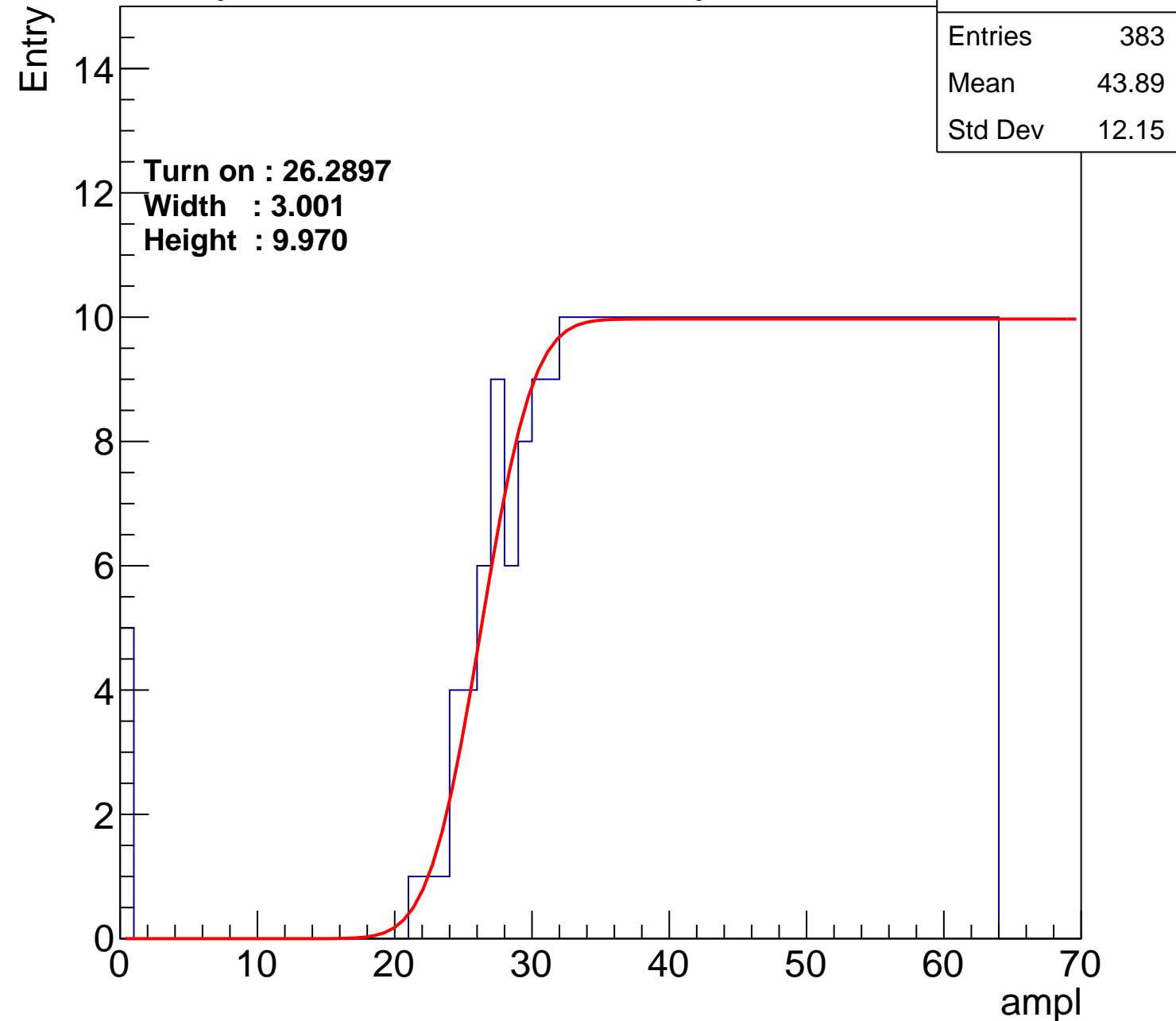
Width : 3.001

Height : 9.970

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch96

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	355
Mean	45.54
Std Dev	10.69

**Turn on : 29.0275**

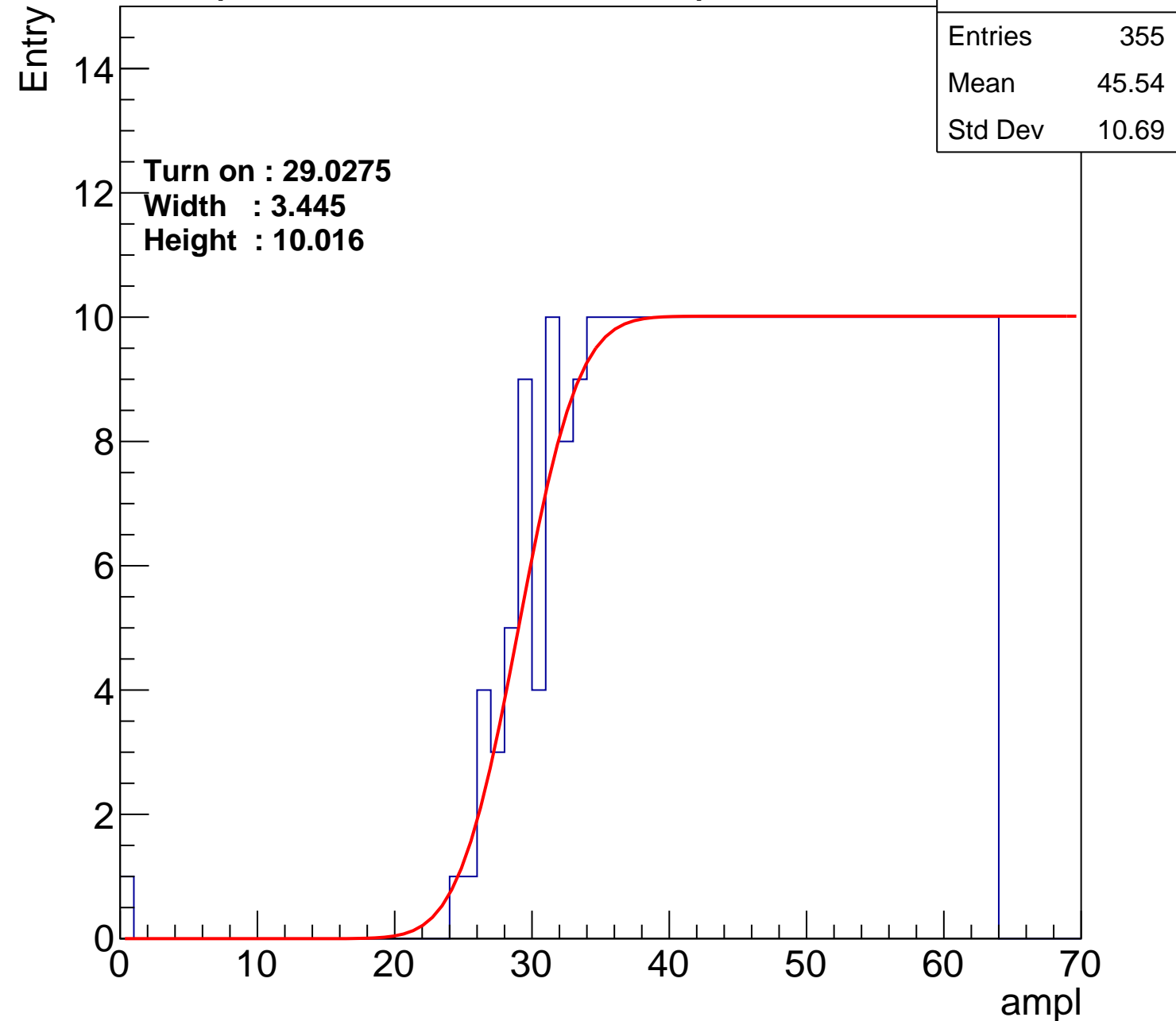
**Width : 3.445**

**Height : 10.016**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch97

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	344
Mean	46.02
Std Dev	10.63

**Turn on : 29.7908**

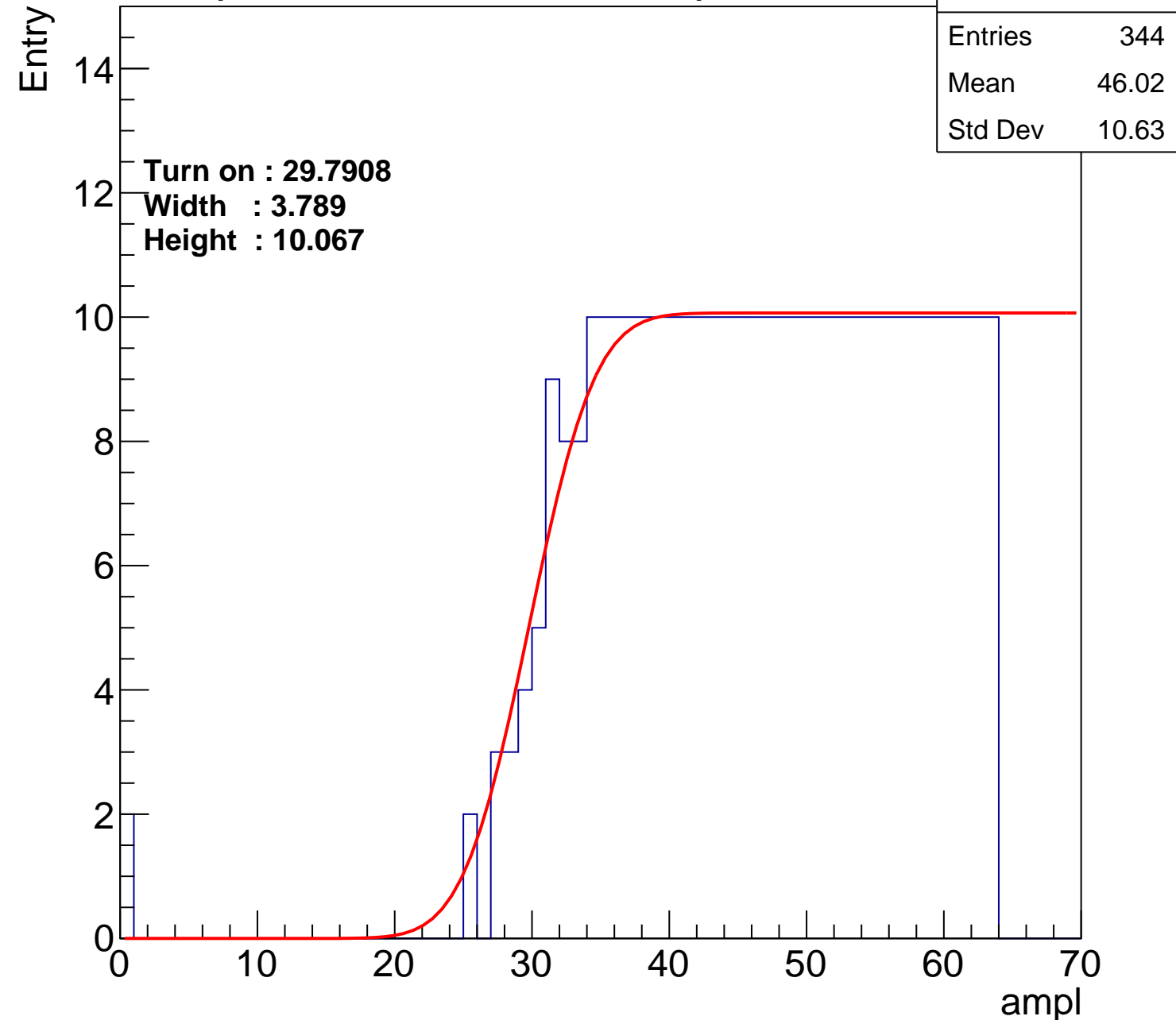
**Width : 3.789**

**Height : 10.067**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch98

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	361
Mean	44.94
Std Dev	11.7

**Turn on : 28.8155**

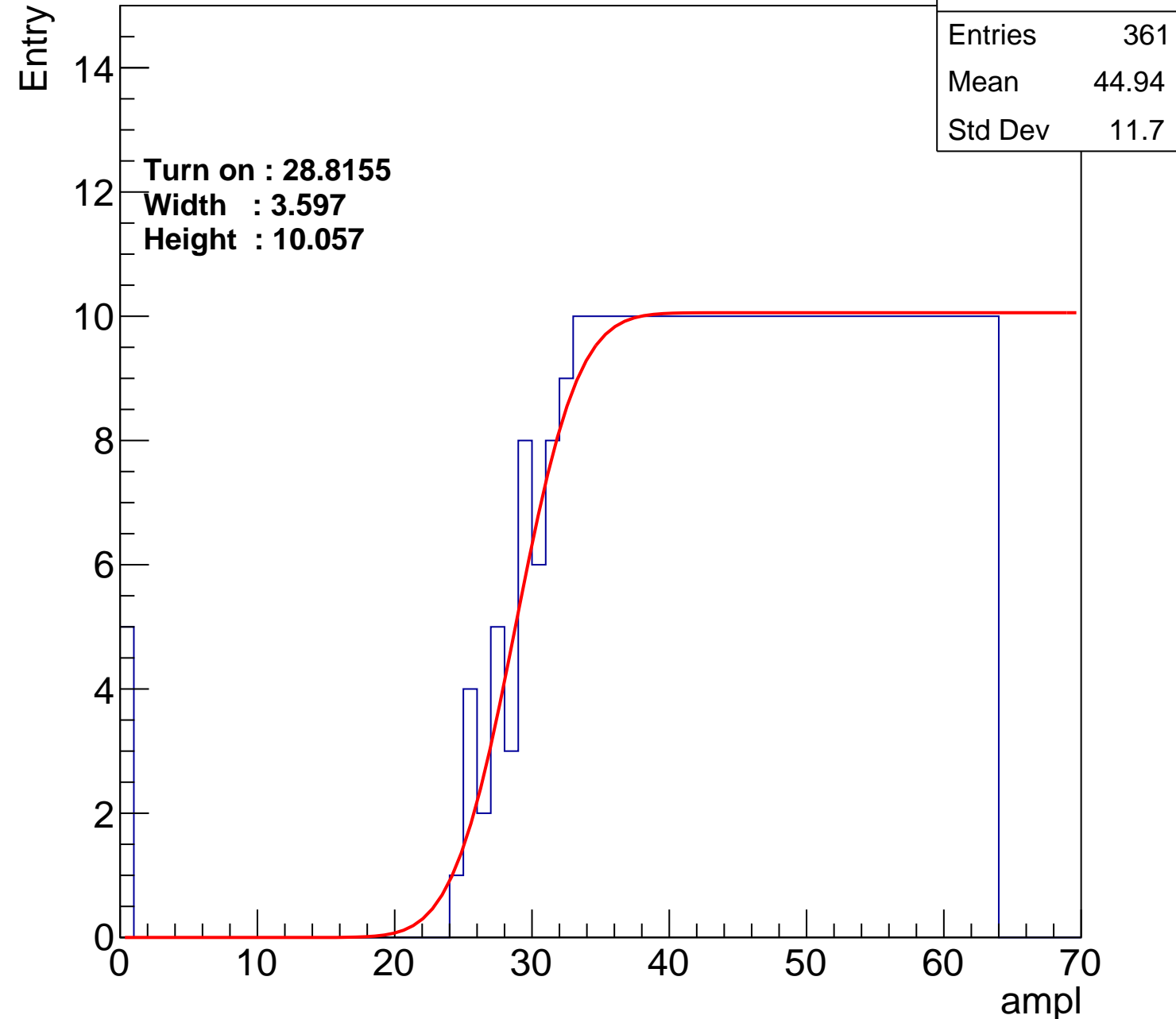
**Width : 3.597**

**Height : 10.057**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch99

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	345
Mean	45.9
Std Dev	10.75

Turn on : 29.8234

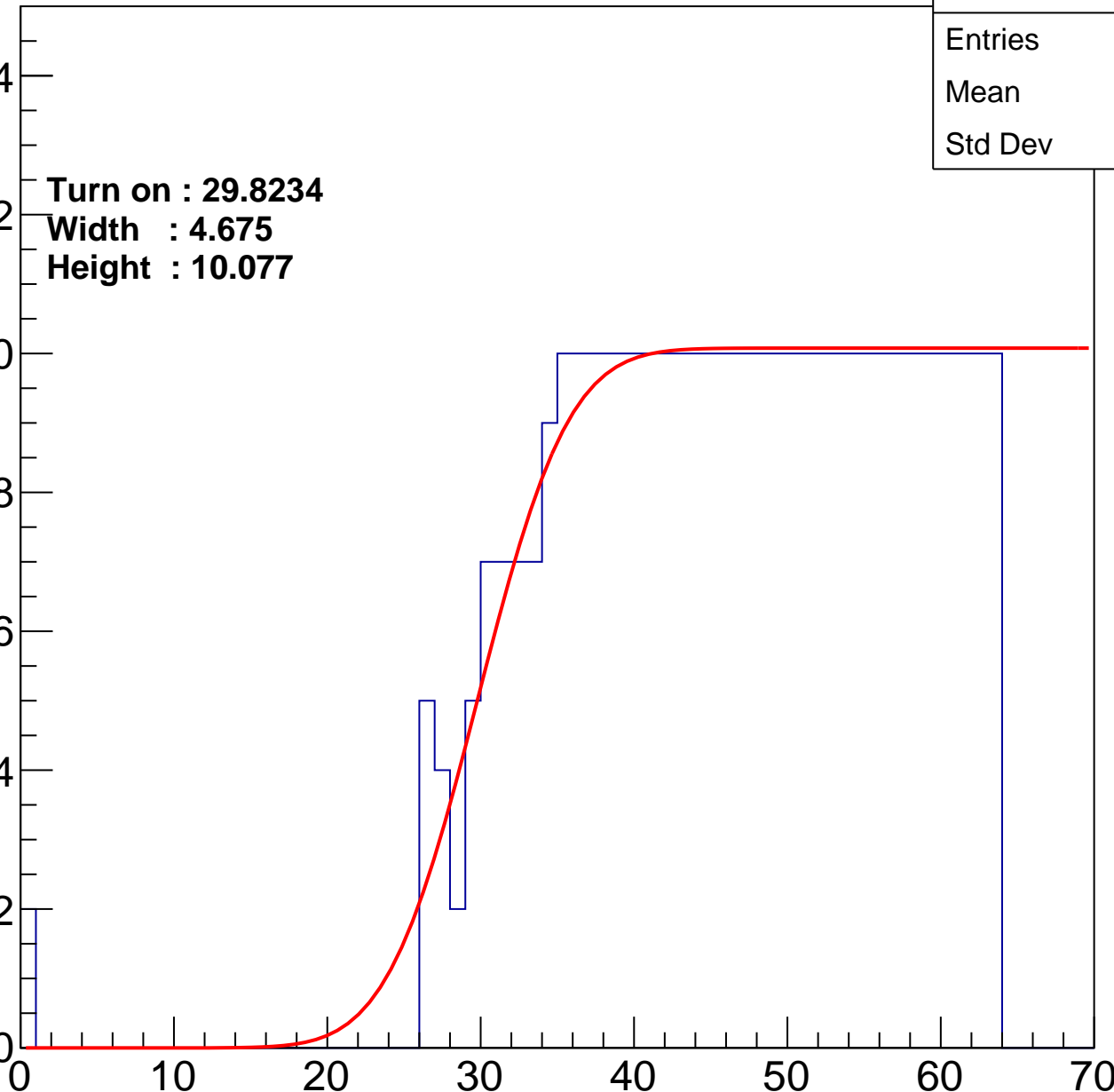
Width : 4.675

Height : 10.077

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch100

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	363
Mean	45.02
Std Dev	11.31

Turn on : 28.8534

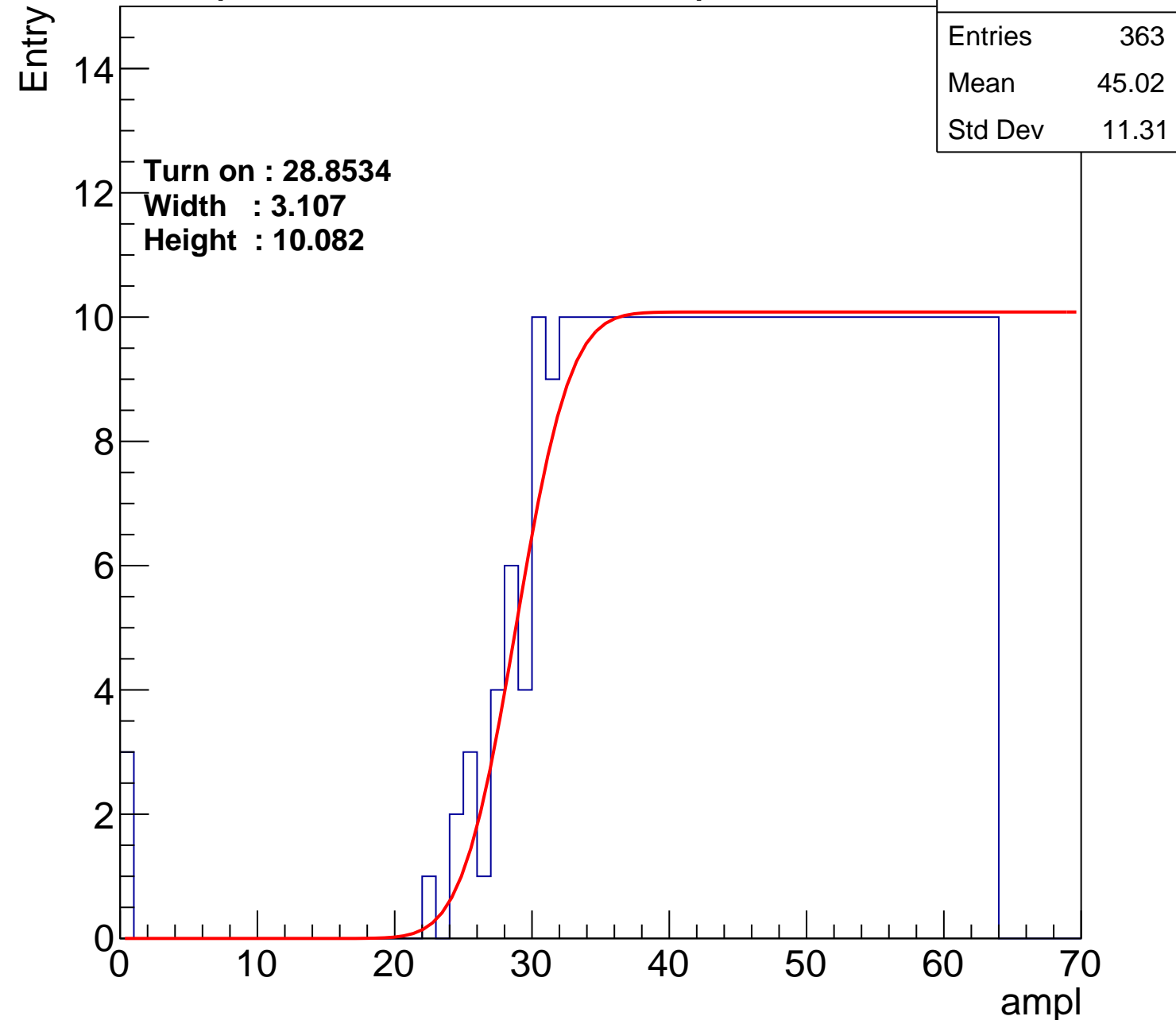
Width : 3.107

Height : 10.082

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch101

calib\_packv5\_042523\_0143.root, FC#9, port A1

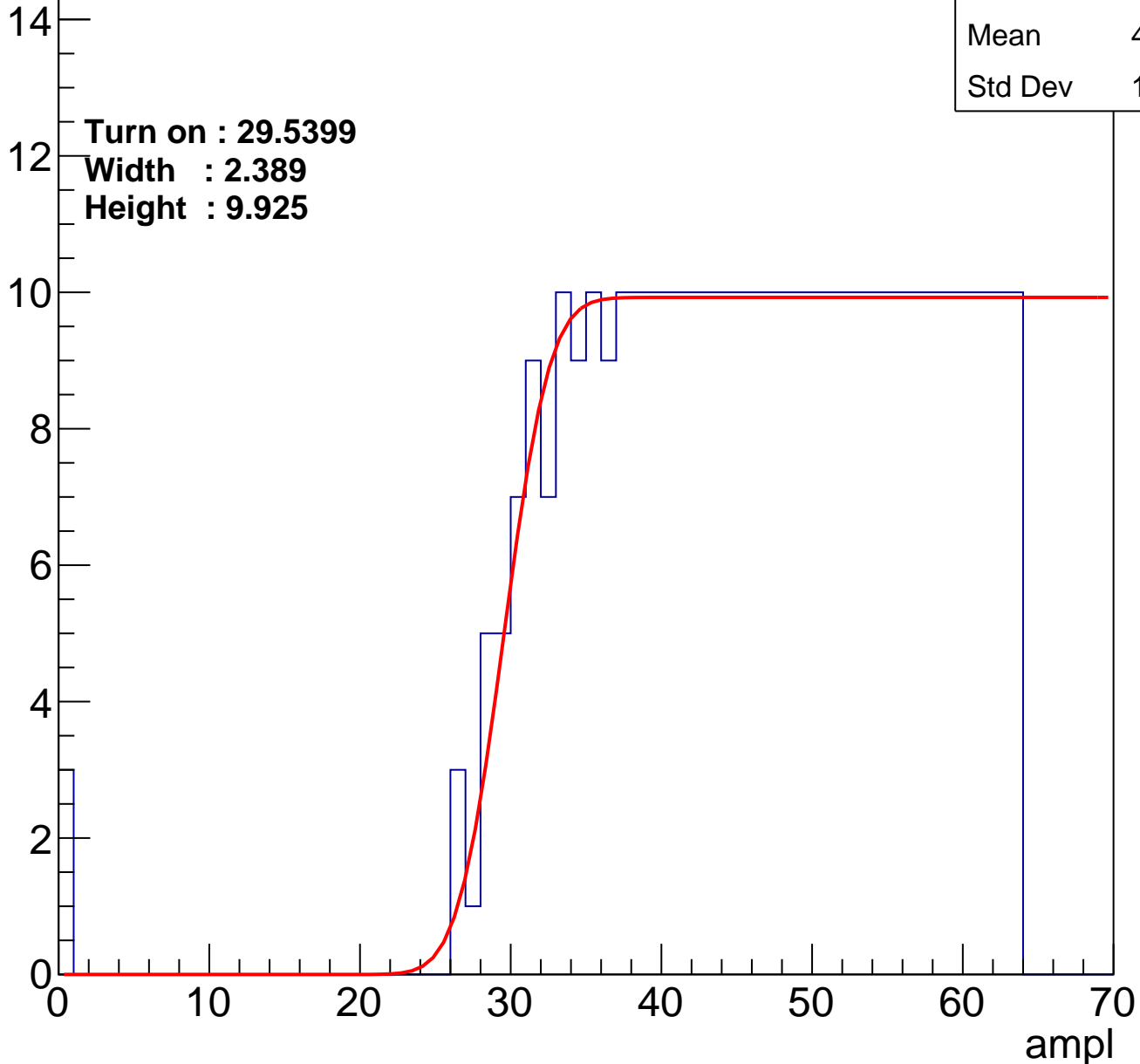
Entries	348
Mean	45.73
Std Dev	10.98

**Turn on : 29.5399**

**Width : 2.389**

**Height : 9.925**

Entry



# B0L001S, U25-ch102

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	380
Mean	44.02
Std Dev	12.11

Turn on : 27.0731

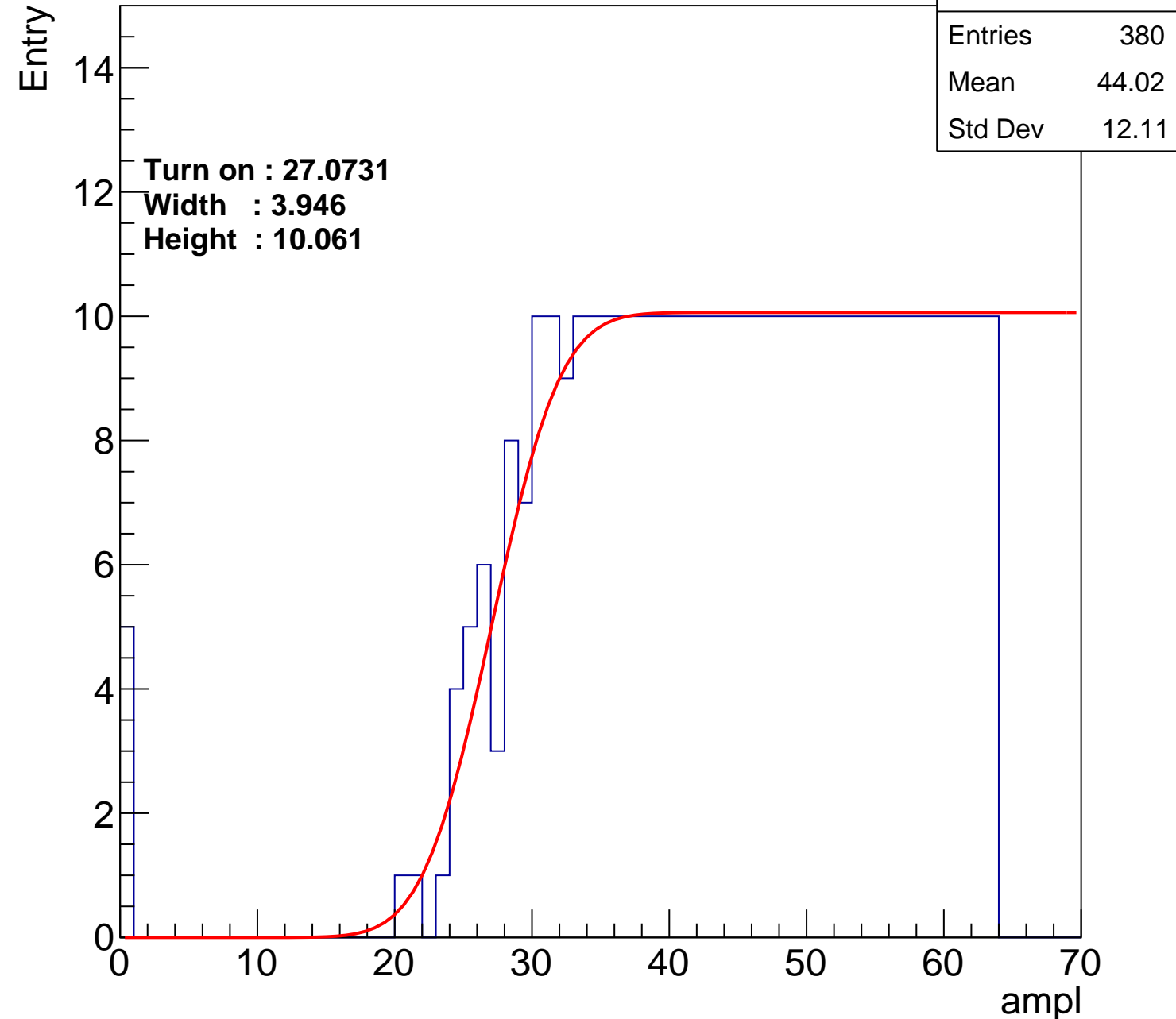
Width : 3.946

Height : 10.061

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U25-ch103

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	360
Mean	45.1
Std Dev	11.34

**Turn on : 28.9439**

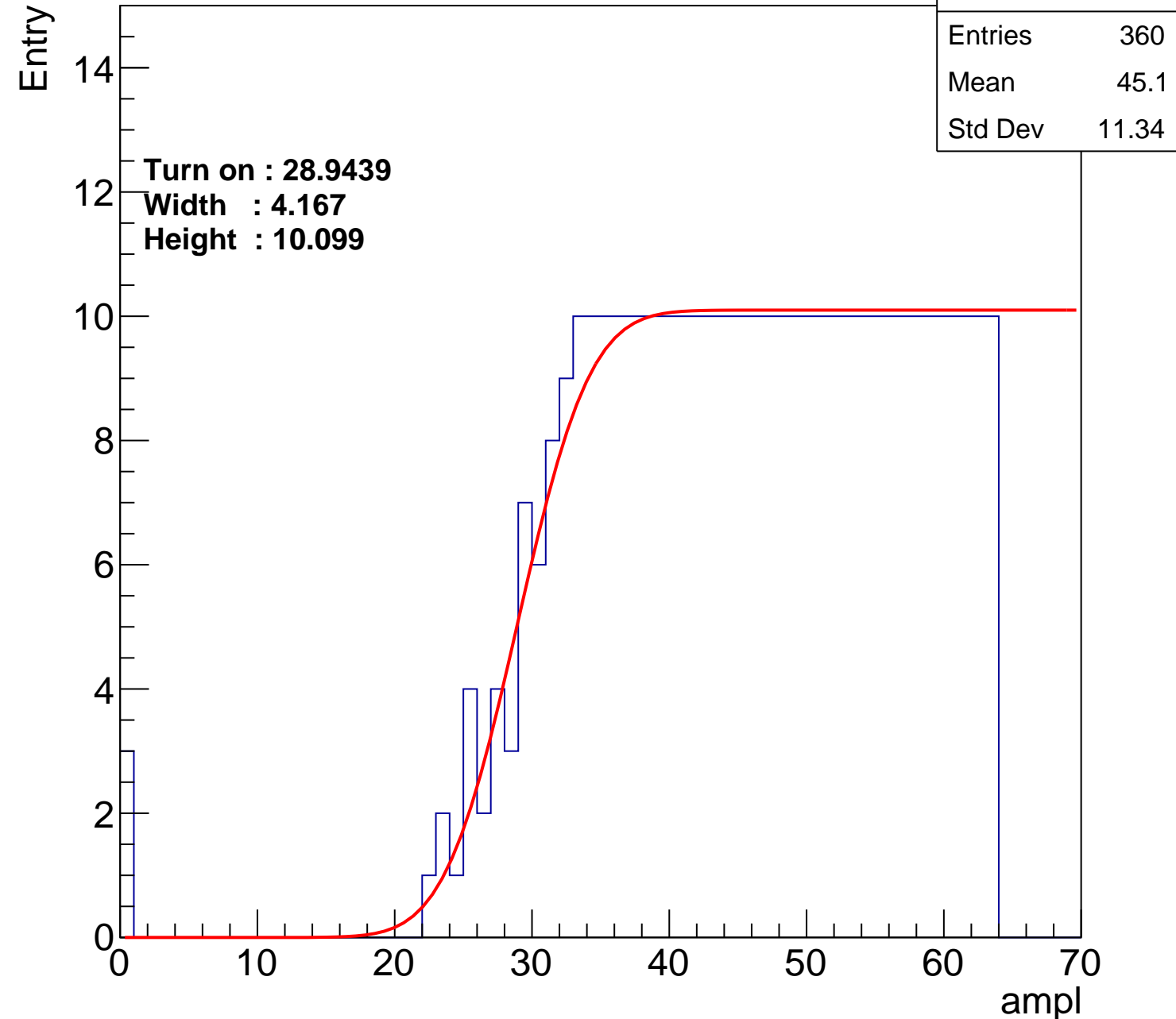
**Width : 4.167**

**Height : 10.099**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch104

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	372
Mean	44.37
Std Dev	12.08

**Turn on : 28.2940**

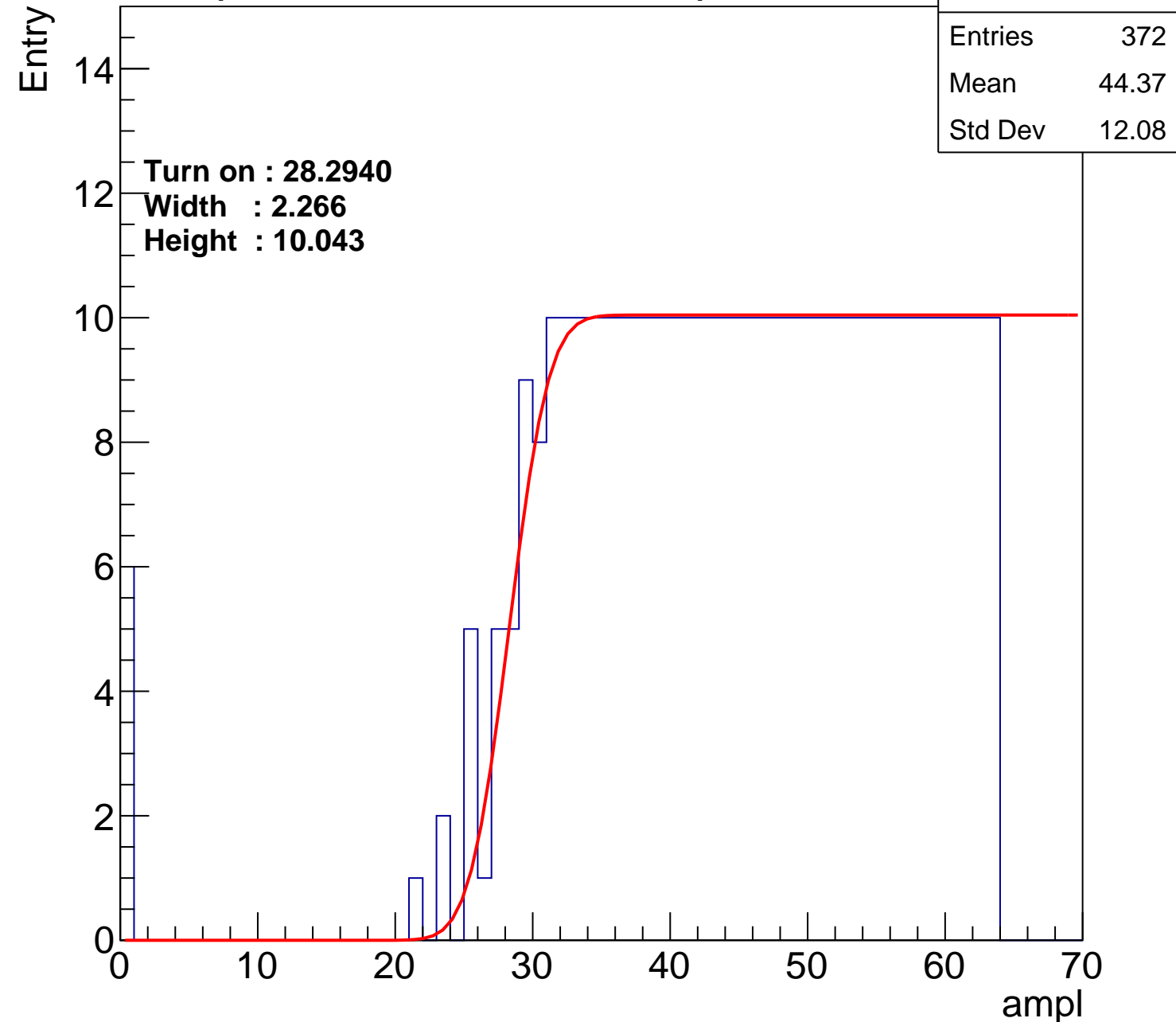
**Width : 2.266**

**Height : 10.043**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch105

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	354
Mean	45.26
Std Dev	11.59

**Turn on : 29.6707**

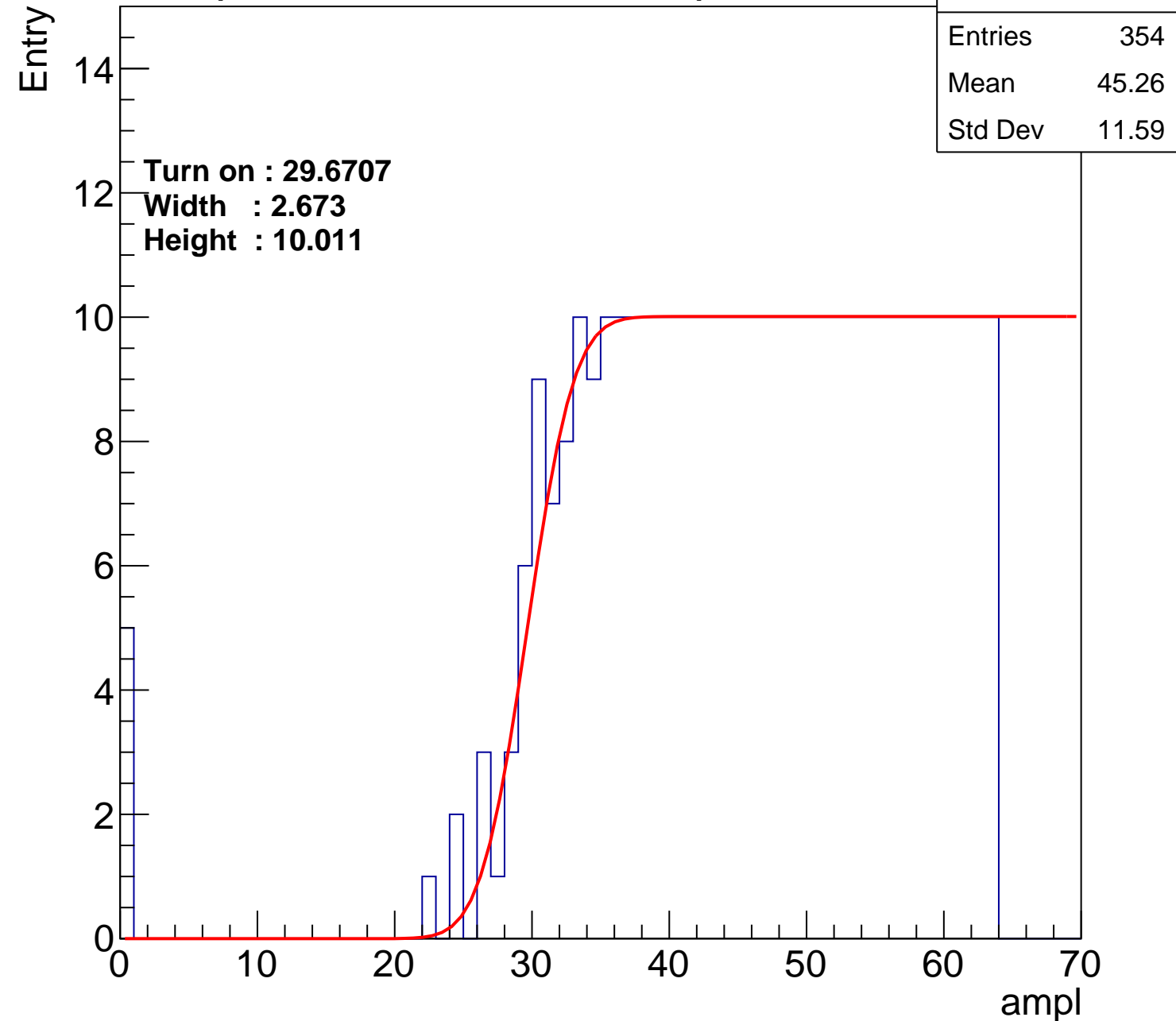
**Width : 2.673**

**Height : 10.011**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch106

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	371
Mean	44.66
Std Dev	11.36

**Turn on : 27.5677**

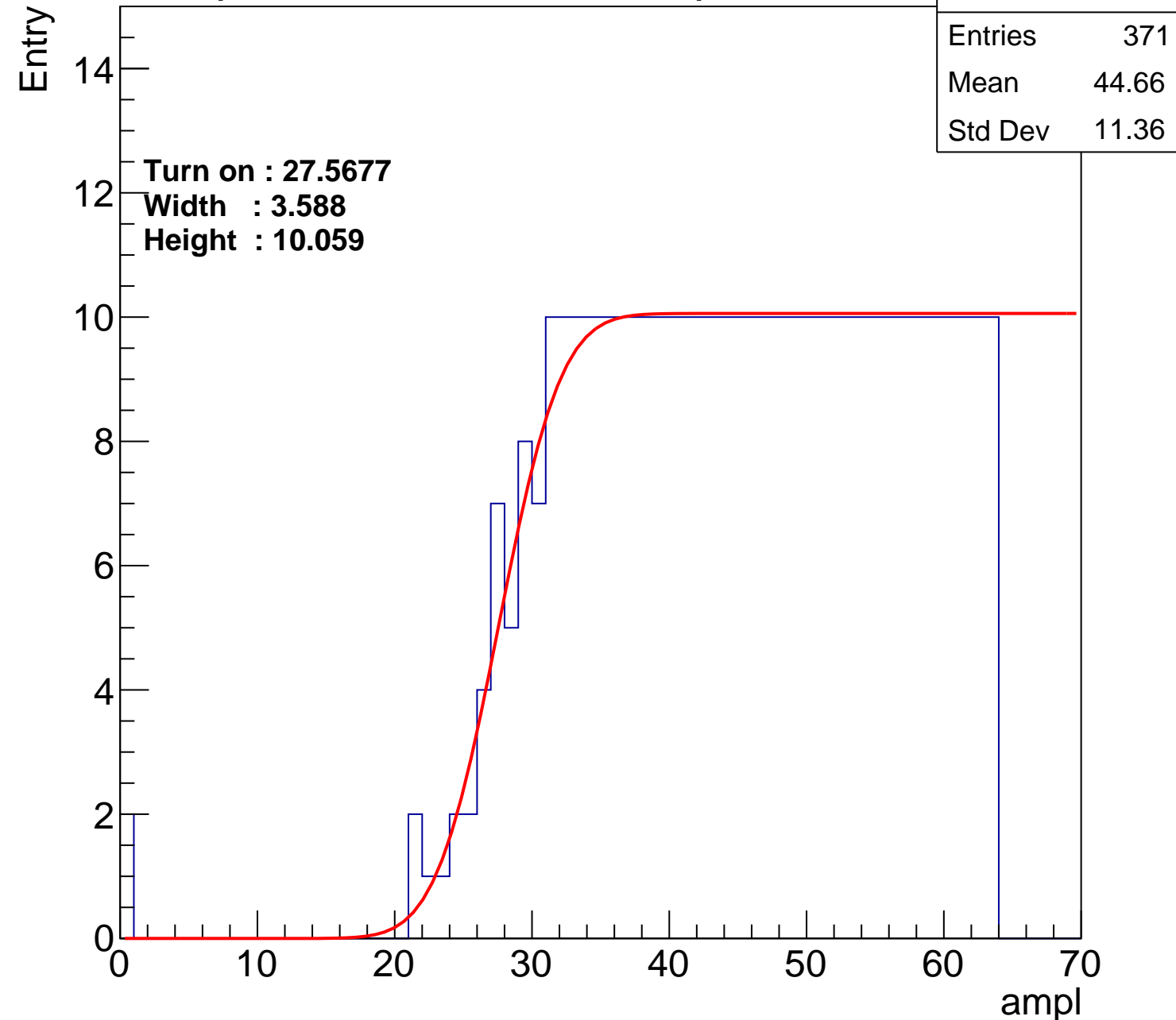
**Width : 3.588**

**Height : 10.059**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch107

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	380
Mean	44.15
Std Dev	11.84

Turn on : 26.7117

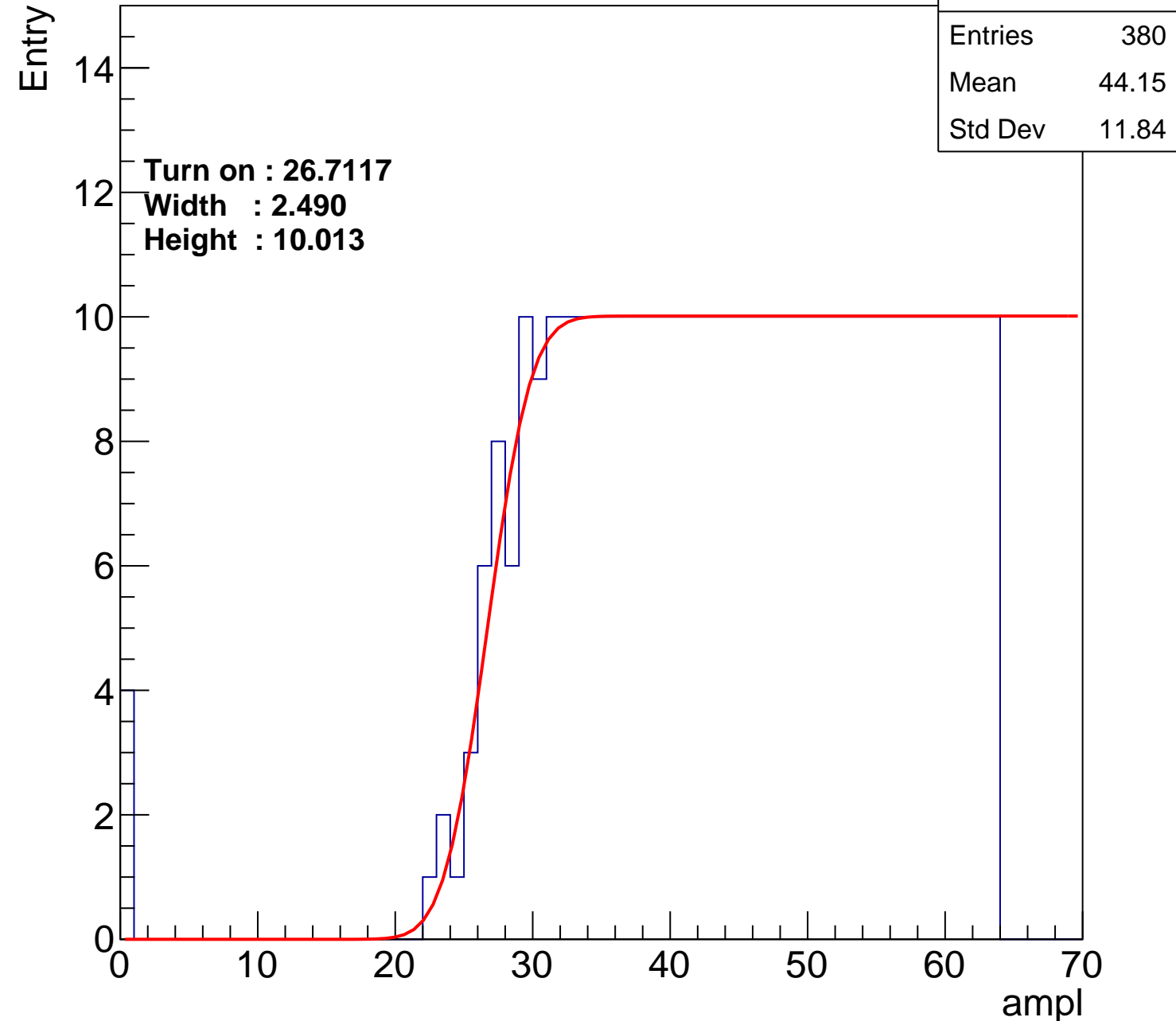
Width : 2.490

Height : 10.013

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch108

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	361
Mean	44.93
Std Dev	11.75

Turn on : 29.7958

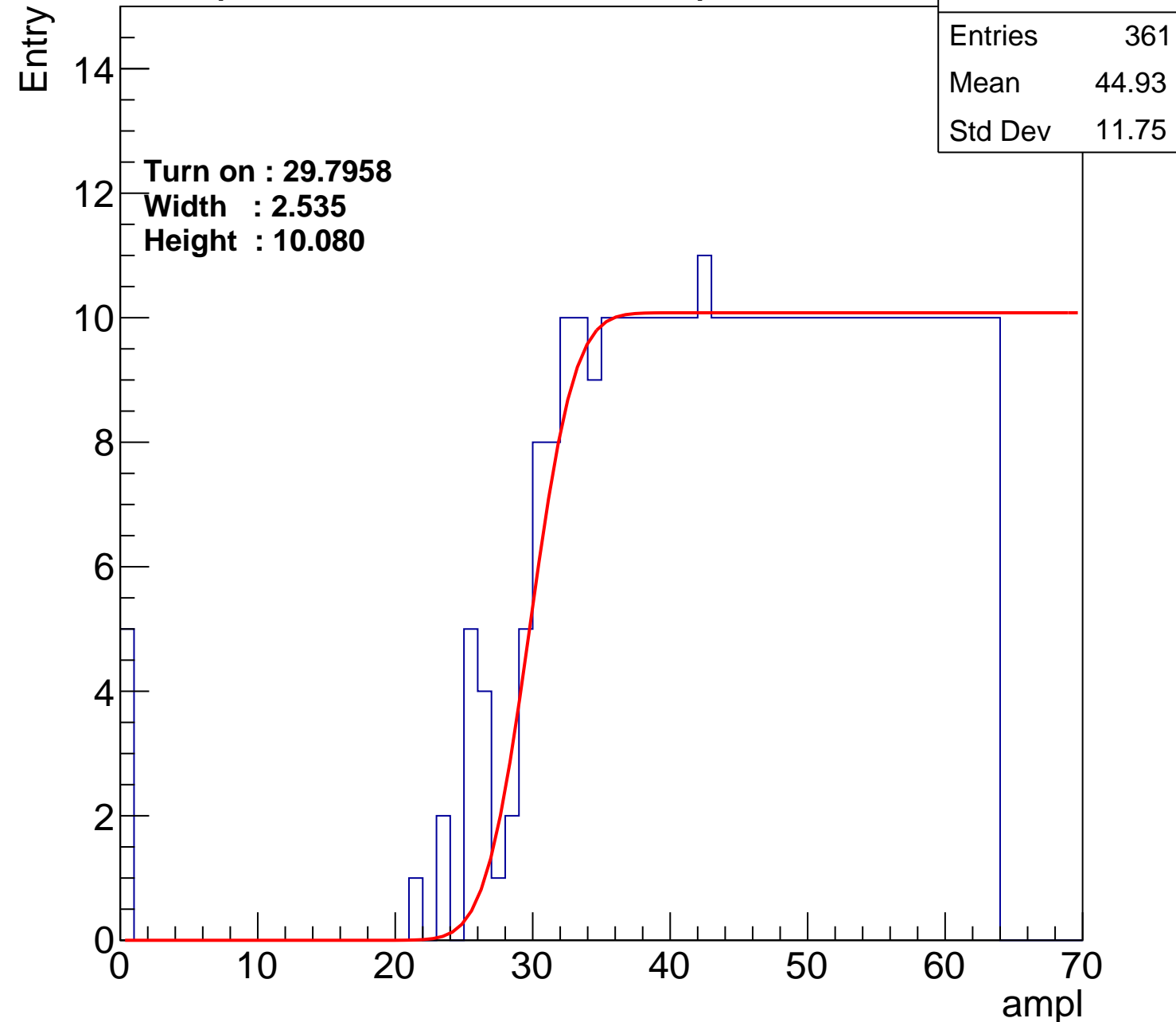
Width : 2.535

Height : 10.080

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch109

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	384
Mean	43.94
Std Dev	12.08

Turn on : 26.1802

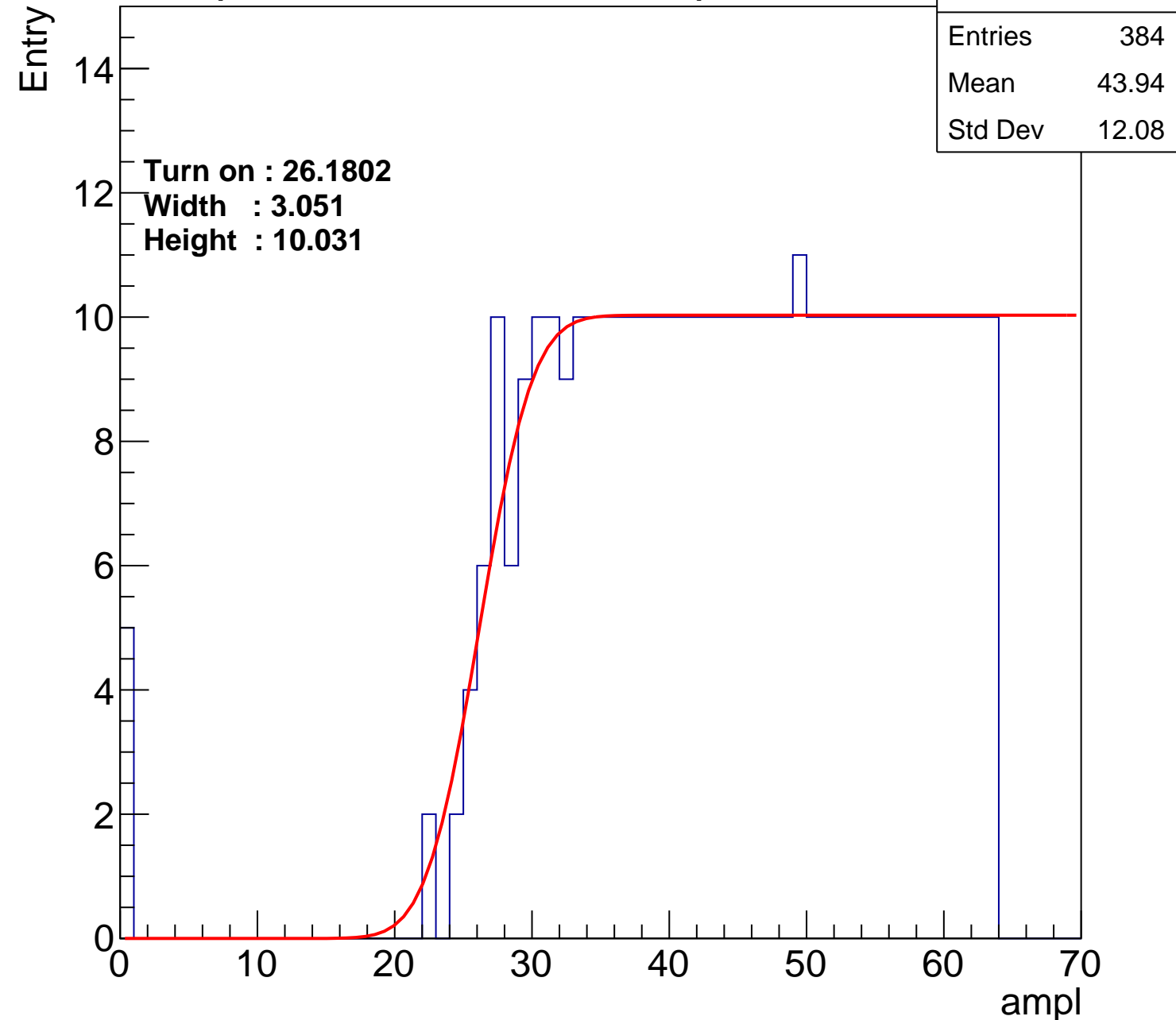
Width : 3.051

Height : 10.031

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch110

calib\_packv5\_042523\_0143.root, FC#9, port A1

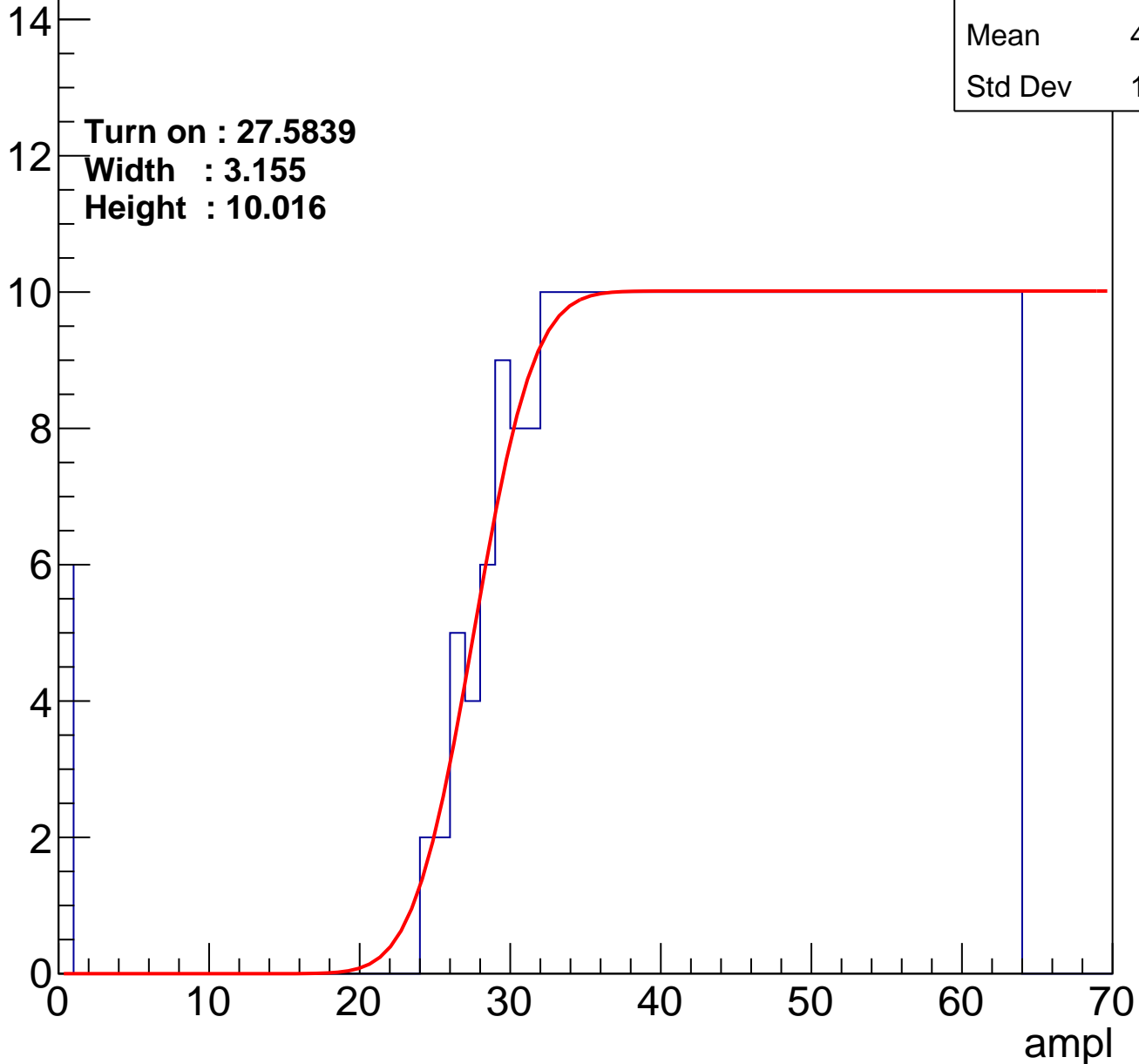
Entries	370
Mean	44.47
Std Dev	12.03

**Turn on : 27.5839**

**Width : 3.155**

**Height : 10.016**

Entry





# B0L001S, U25-ch111

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	381
Mean	44.26
Std Dev	11.64

**Turn on : 26.4217**

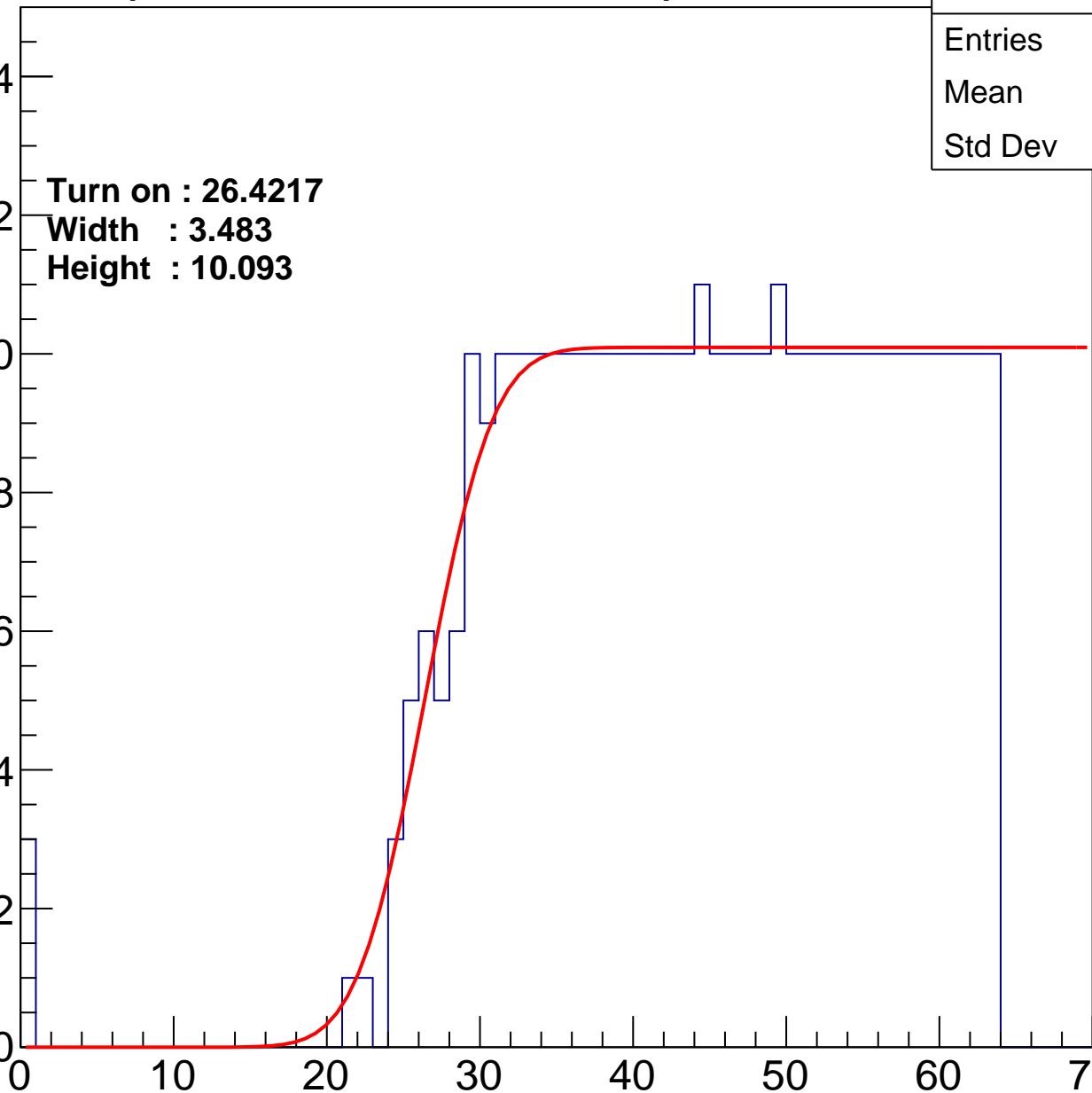
**Width : 3.483**

**Height : 10.093**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch112

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	336
Mean	46.21
Std Dev	10.98

Turn on : 30.9818

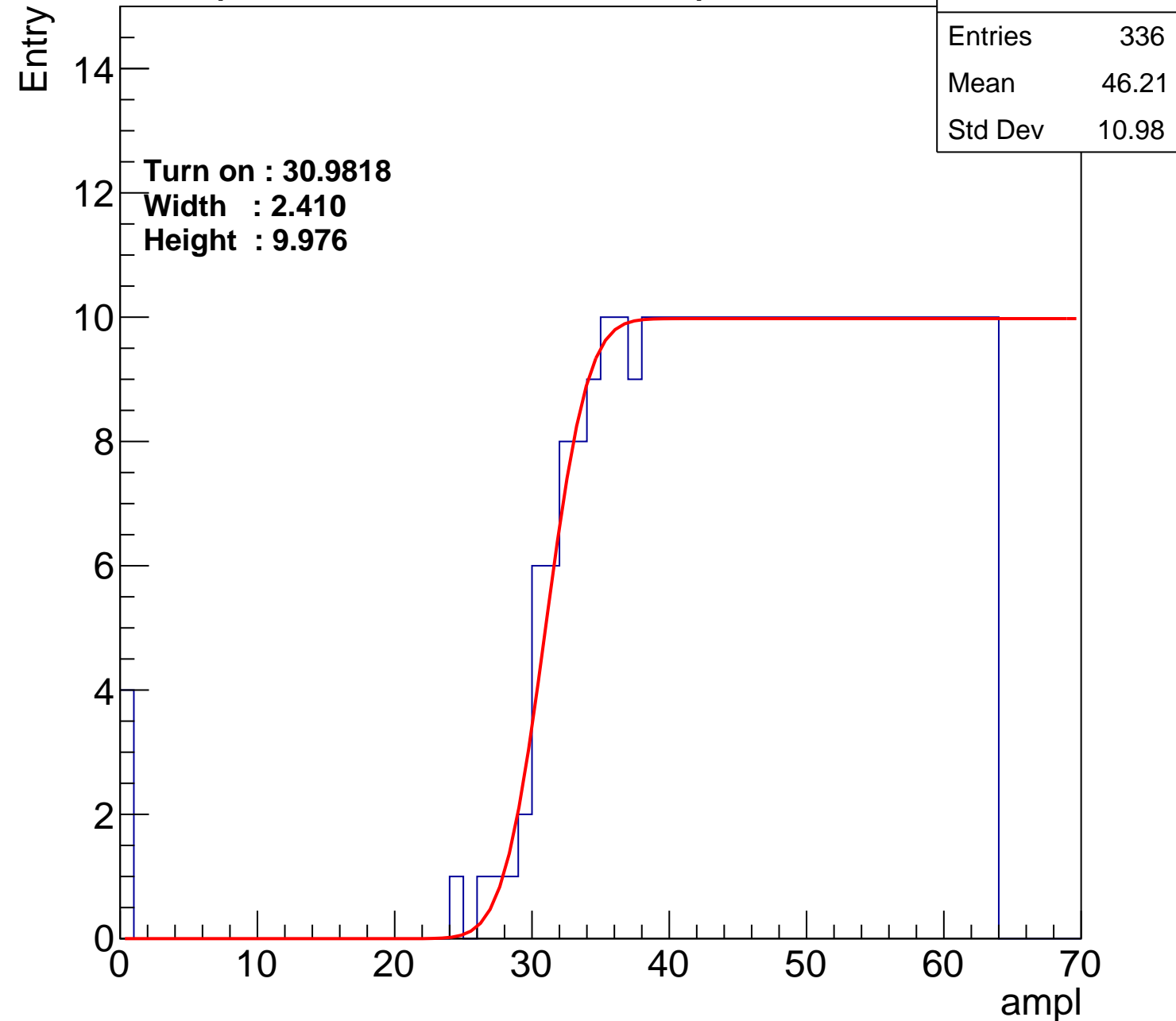
Width : 2.410

Height : 9.976

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch113

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	355
Mean	45.39
Std Dev	11.15

Turn on : 28.9206

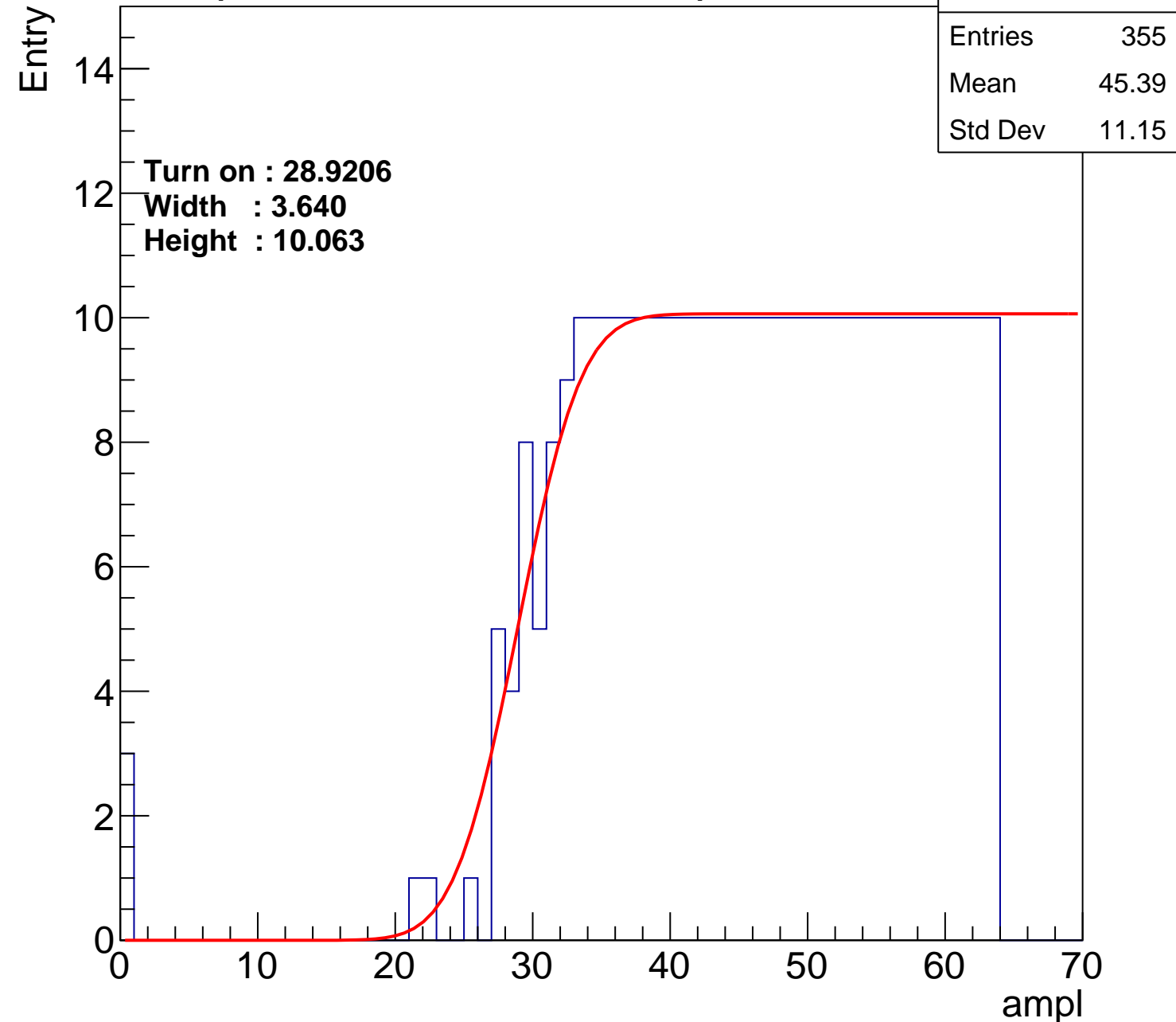
Width : 3.640

Height : 10.063

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch114

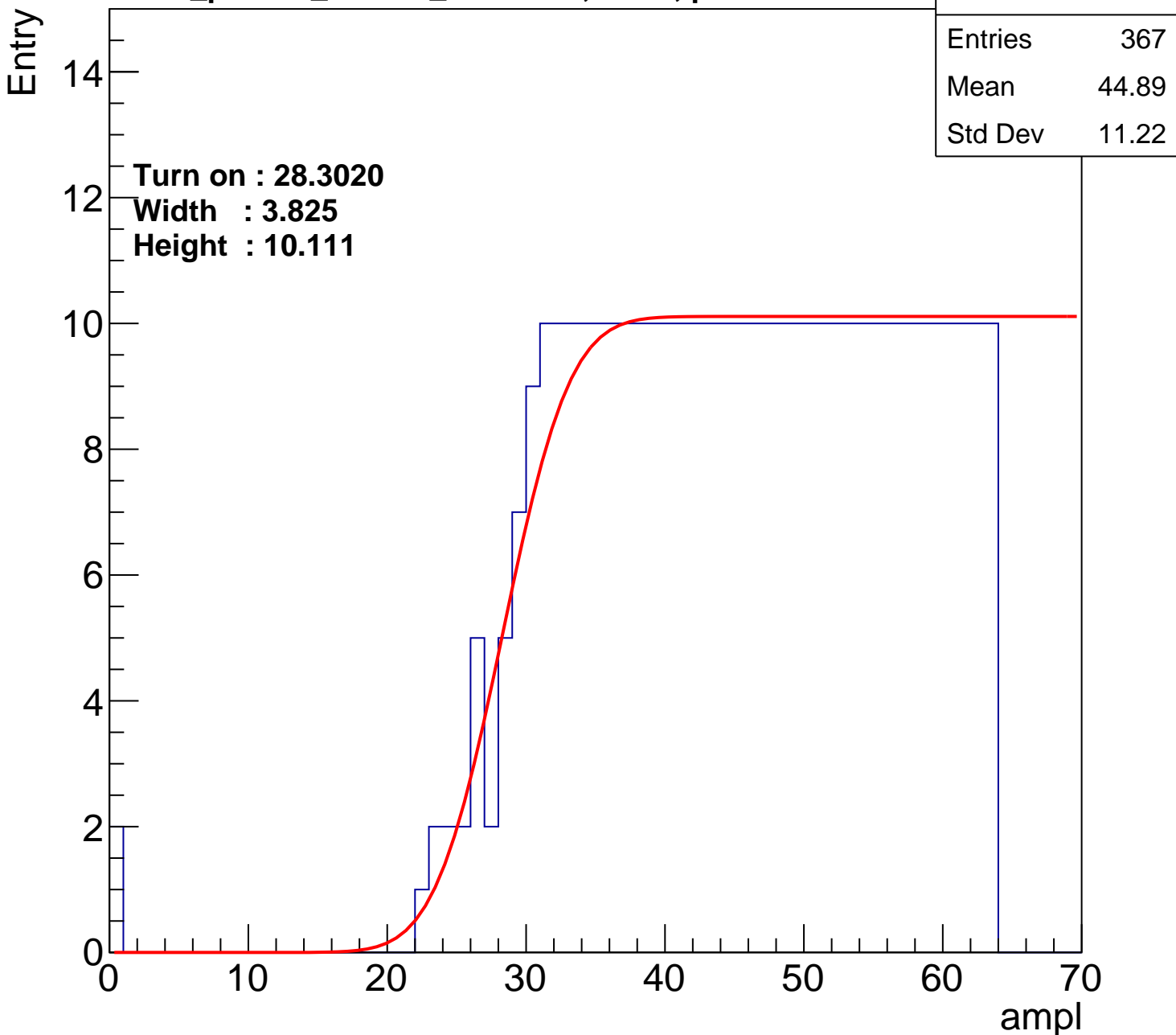
**calib\_packv5\_042523\_0143.root, FC#9, port A1**

**Turn on : 28.3020**

**Width : 3.825**

**Height : 10.111**

Entries	367
Mean	44.89
Std Dev	11.22



# B0L001S, U25-ch115

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	366
Mean	44.88
Std Dev	11.36

Turn on : 27.8873

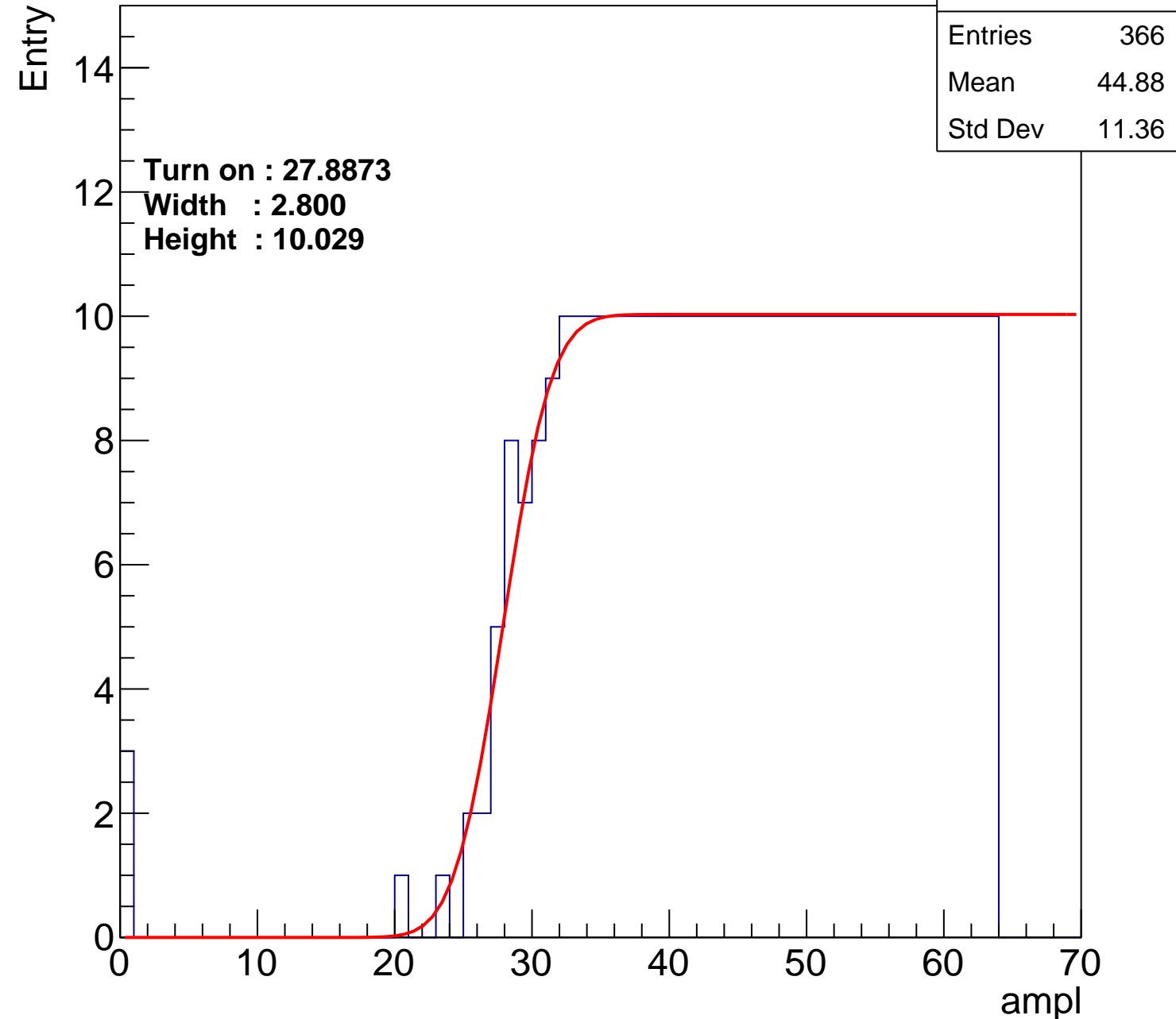
Width : 2.800

Height : 10.029

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch116

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	374
Mean	44.51
Std Dev	11.52

Turn on : 27.3195

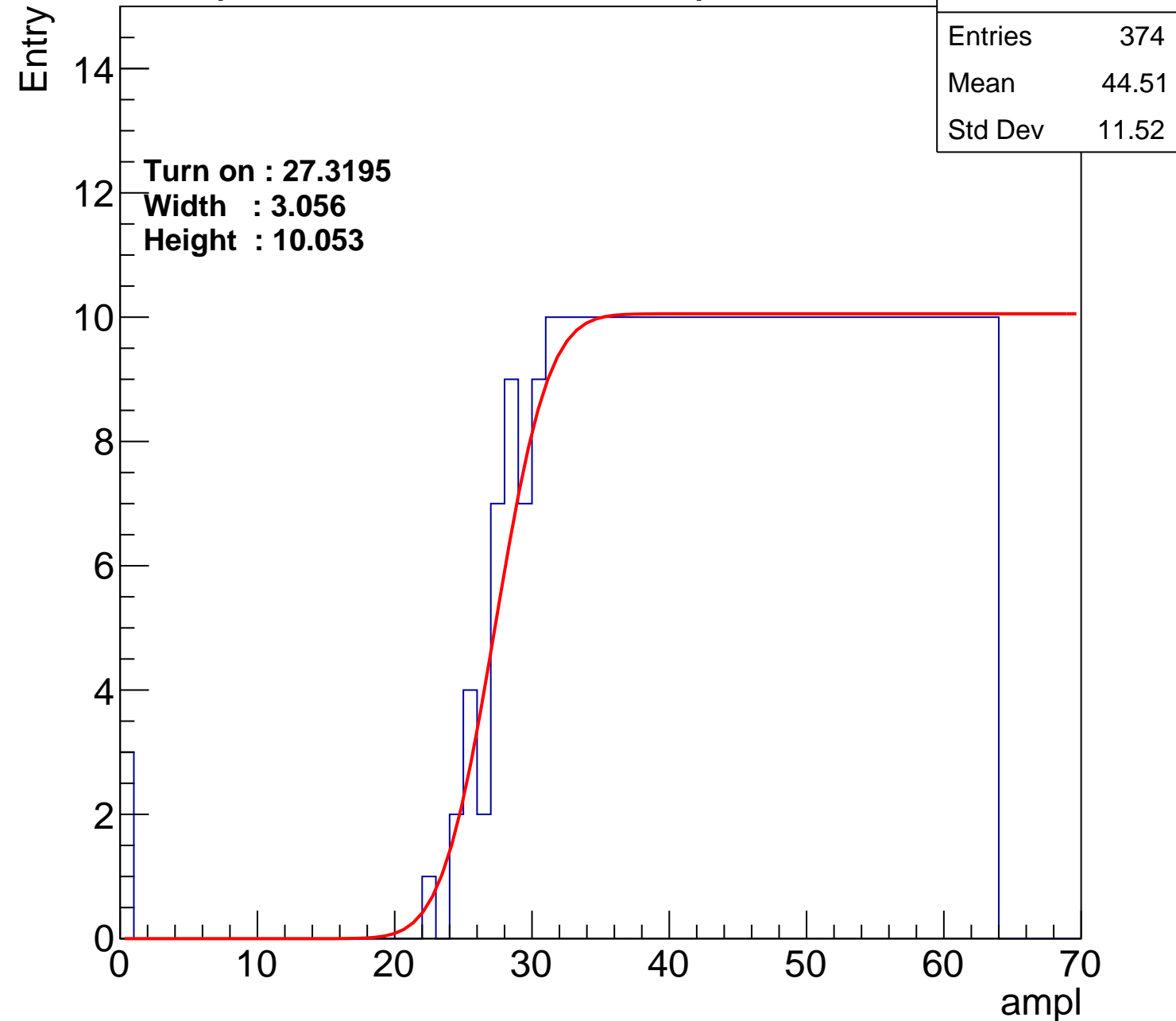
Width : 3.056

Height : 10.053

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch117

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	354
Mean	45.27
Std Dev	11.57

Turn on : 29.3015

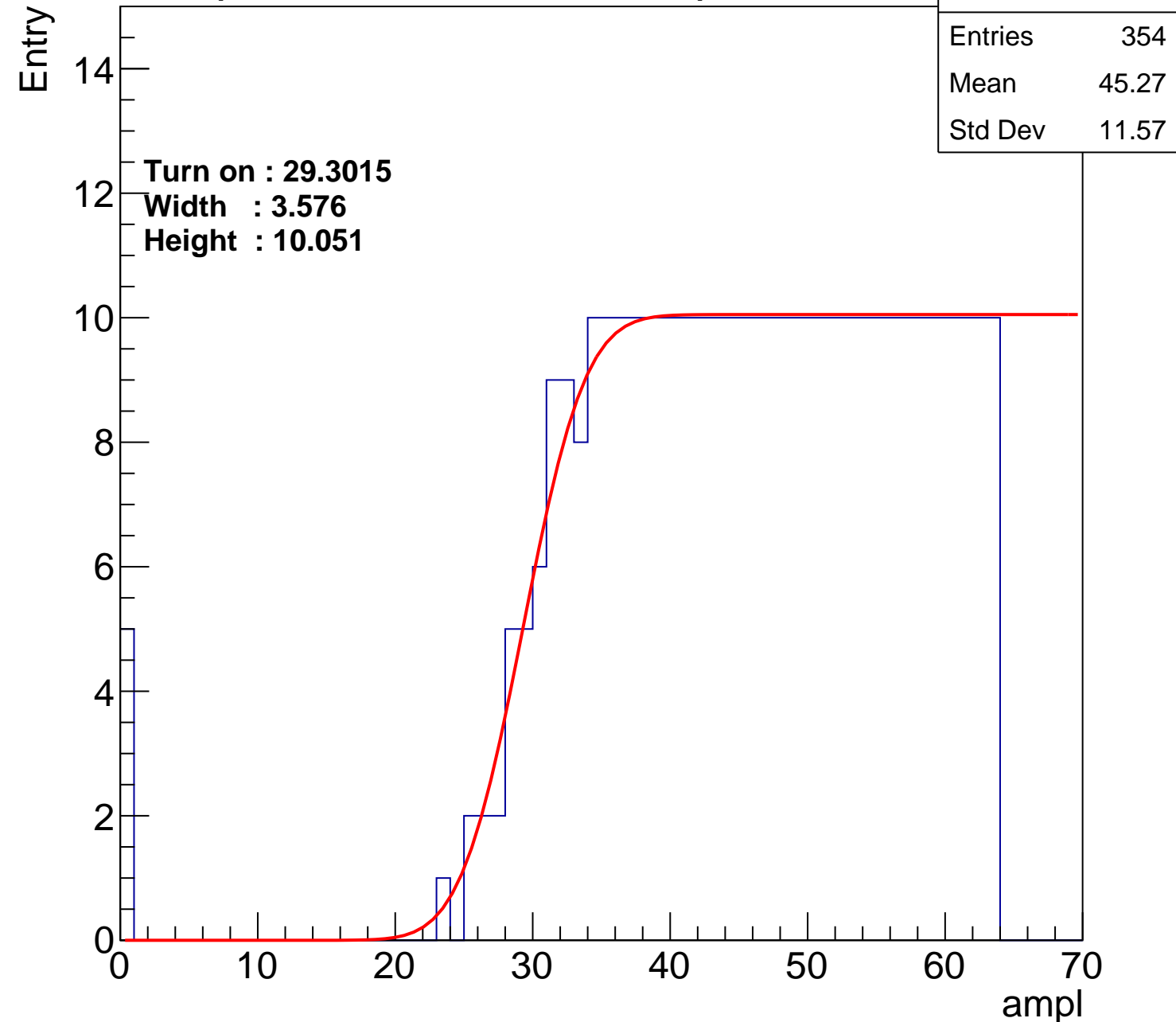
Width : 3.576

Height : 10.051

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch118

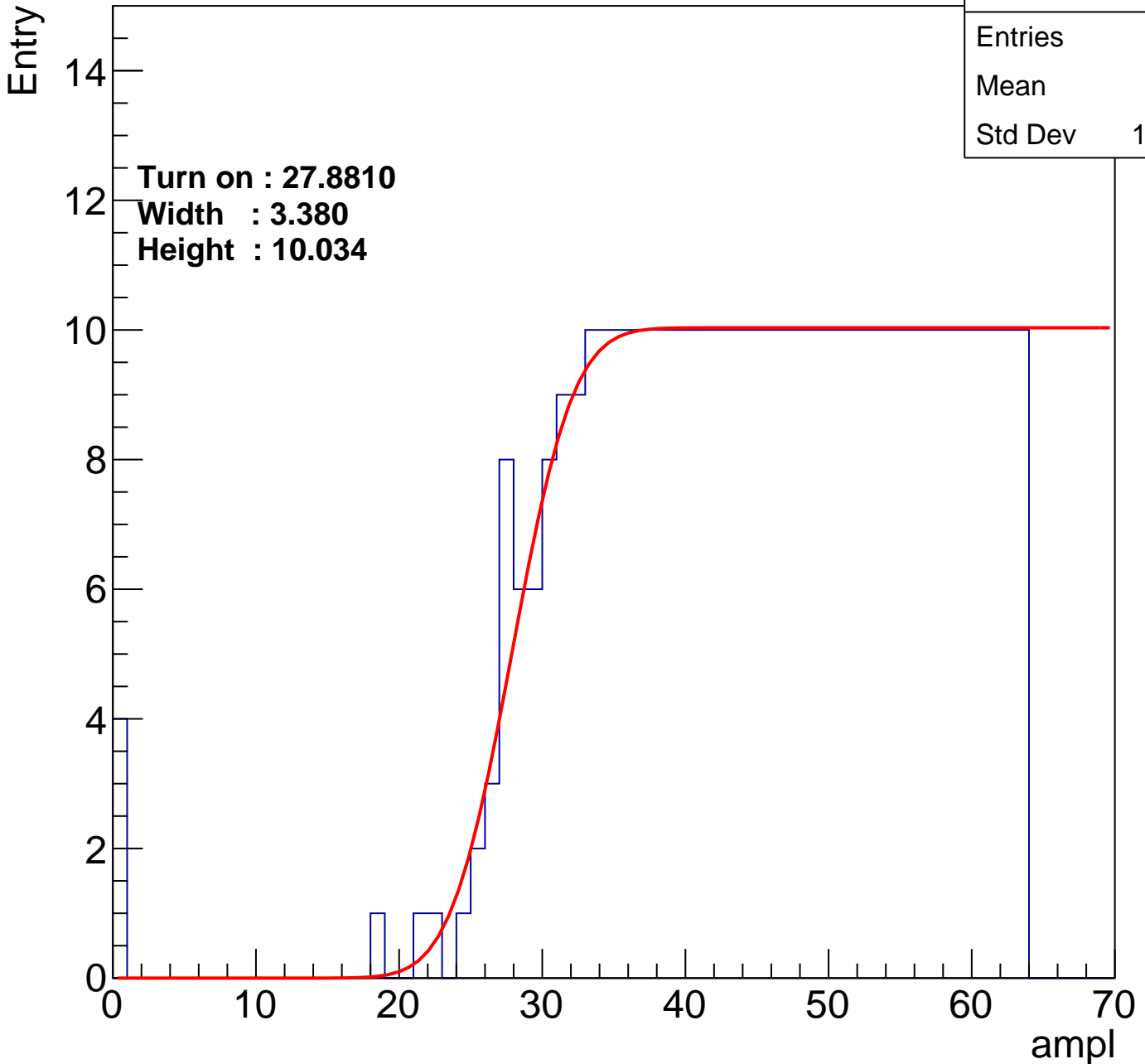
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	369
Mean	44.6
Std Dev	11.73

Turn on : 27.8810

Width : 3.380

Height : 10.034





# B0L001S, U25-ch119

calib\_packv5\_042523\_0143.root, FC#9, port A1

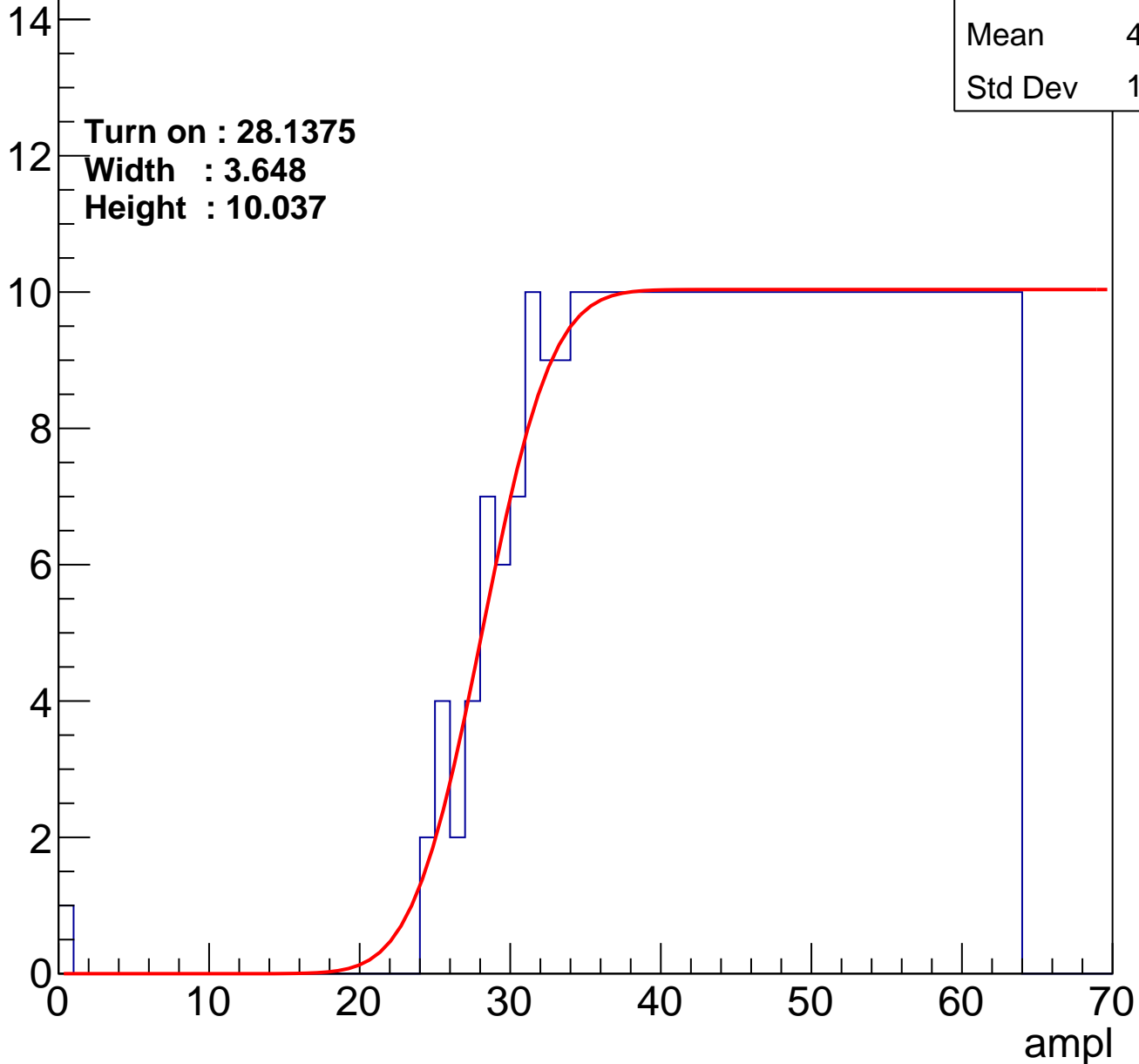
Entries	361
Mean	45.24
Std Dev	10.86

**Turn on : 28.1375**

**Width : 3.648**

**Height : 10.037**

Entry



# B0L001S, U25-ch120

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	370
Mean	44.59
Std Dev	11.69

**Turn on : 27.3308**

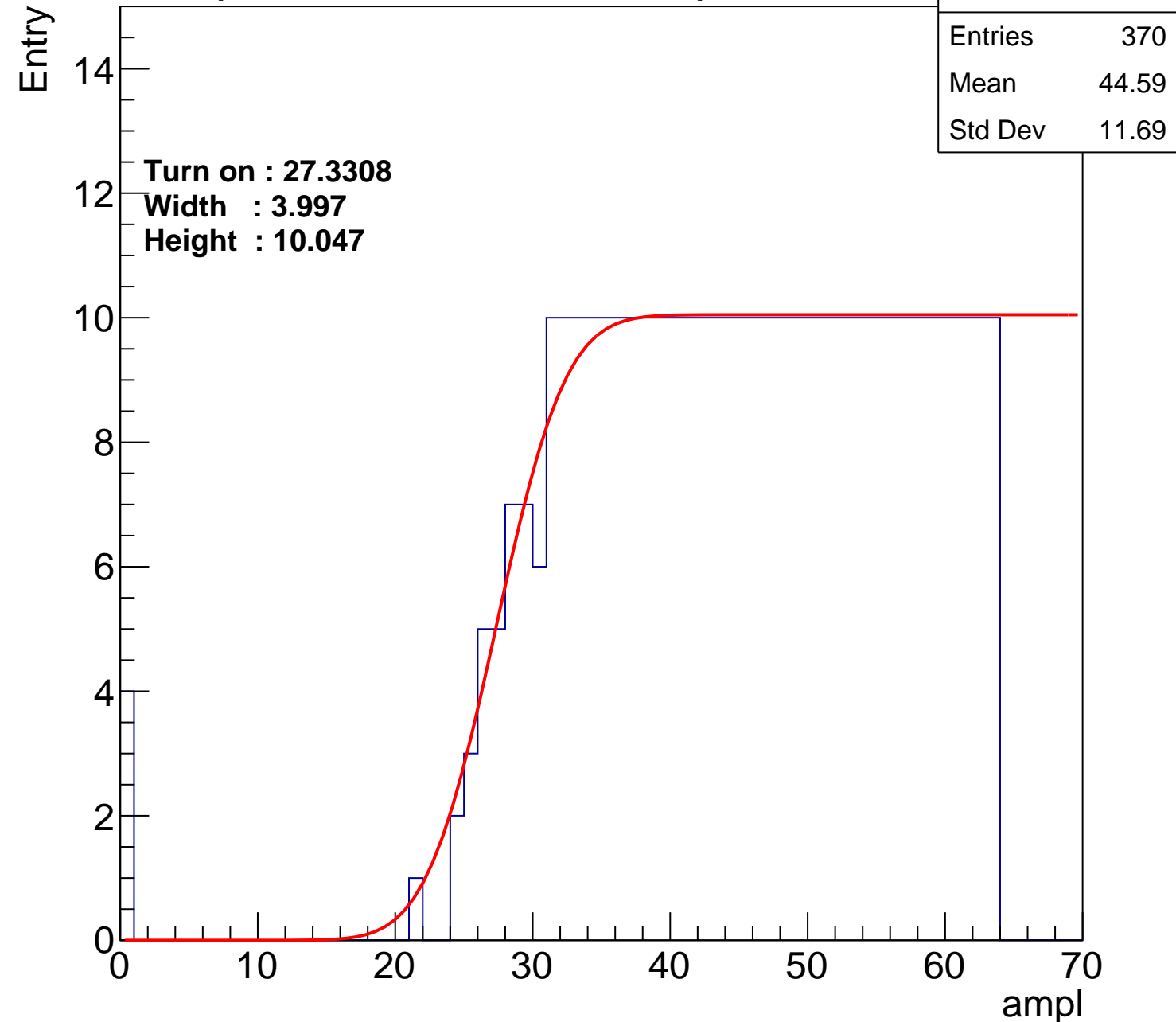
**Width : 3.997**

**Height : 10.047**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch121

calib\_packv5\_042523\_0143.root, FC#9, port A1

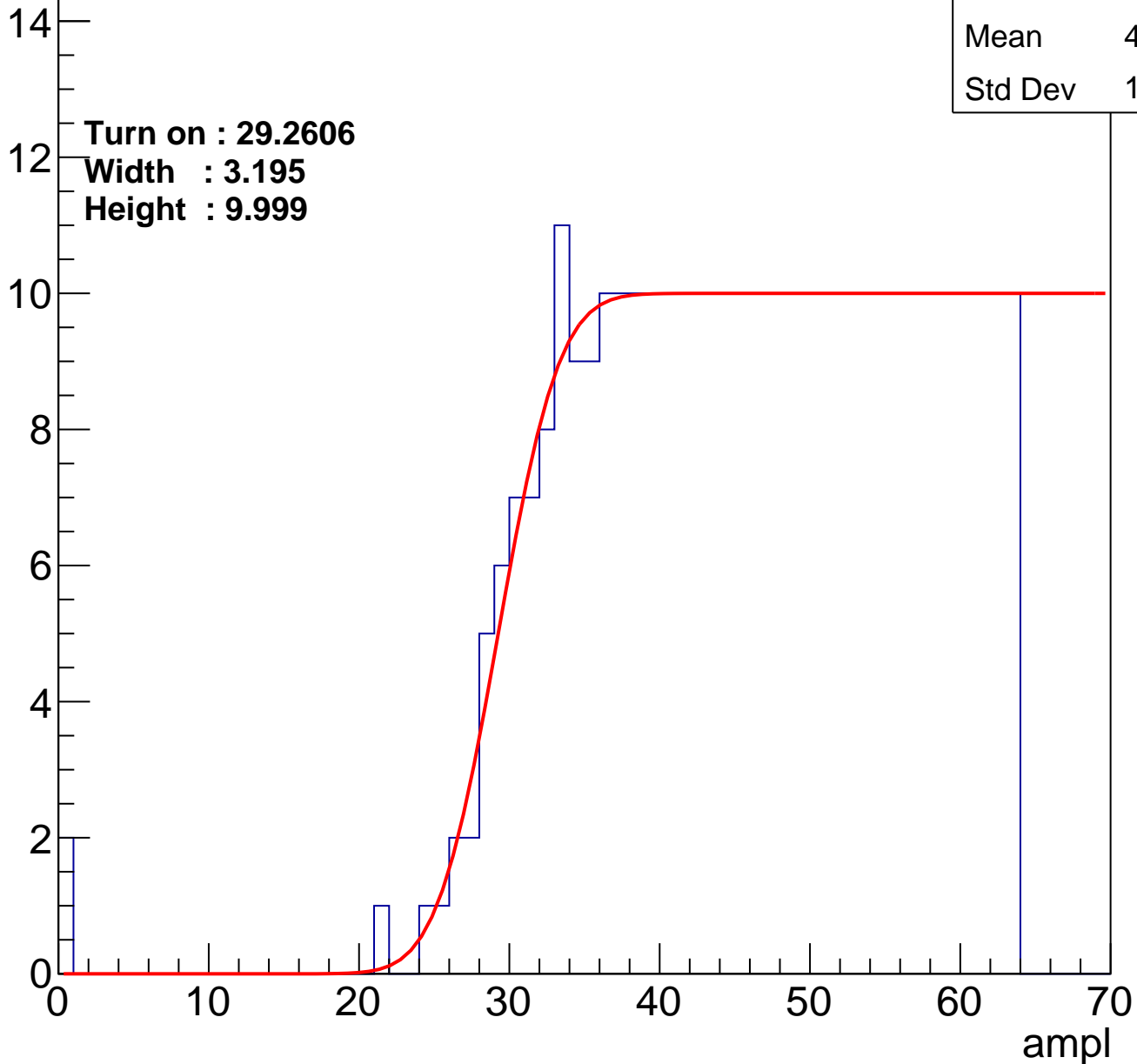
Entries	351
Mean	45.63
Std Dev	10.87

**Turn on : 29.2606**

**Width : 3.195**

**Height : 9.999**

Entry



# B0L001S, U25-ch122

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	344
Mean	45.93
Std Dev	10.88

Turn on : 30.5686

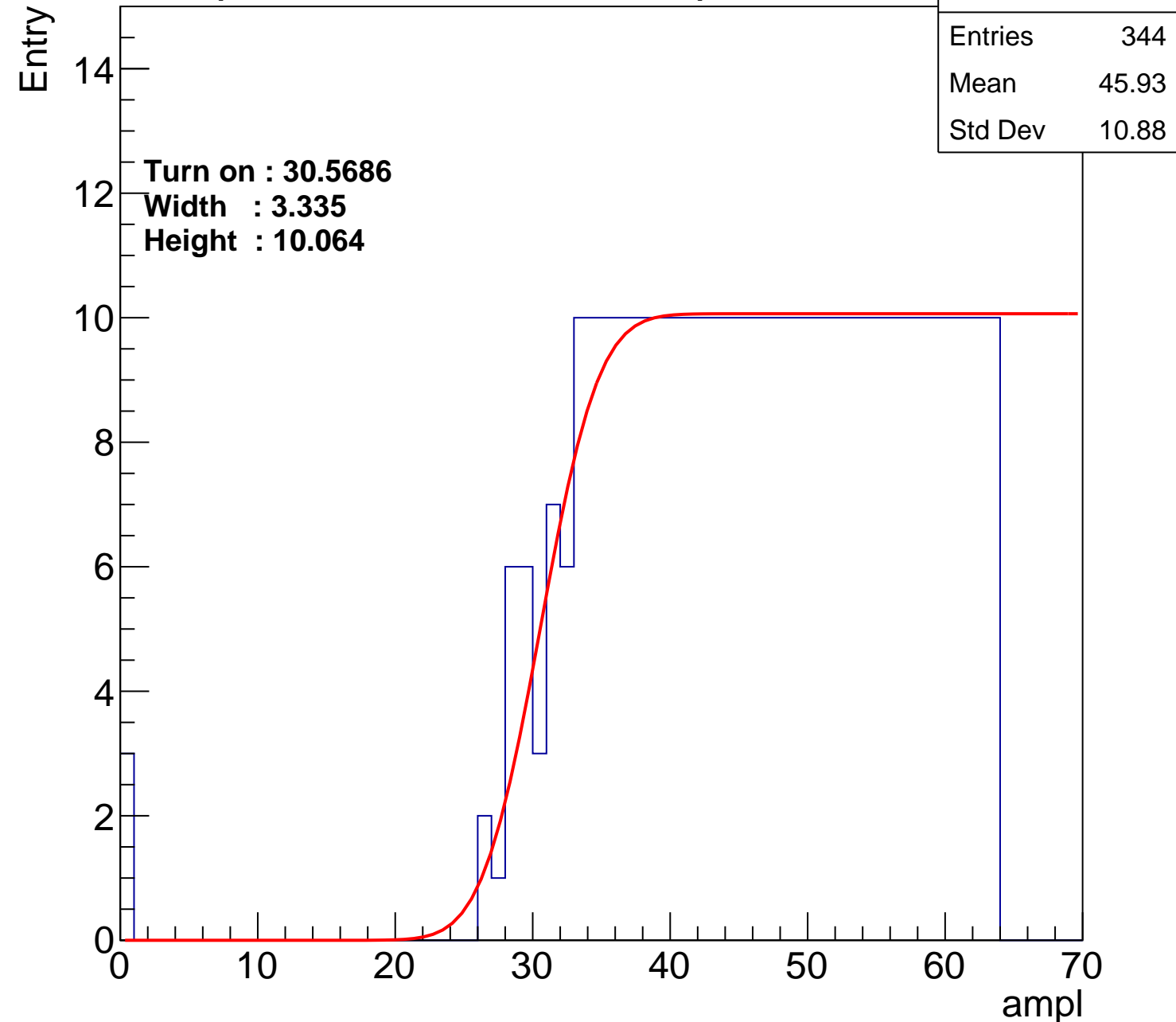
Width : 3.335

Height : 10.064

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch123

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	368
Mean	44.61
Std Dev	11.83

Turn on : 27.6625

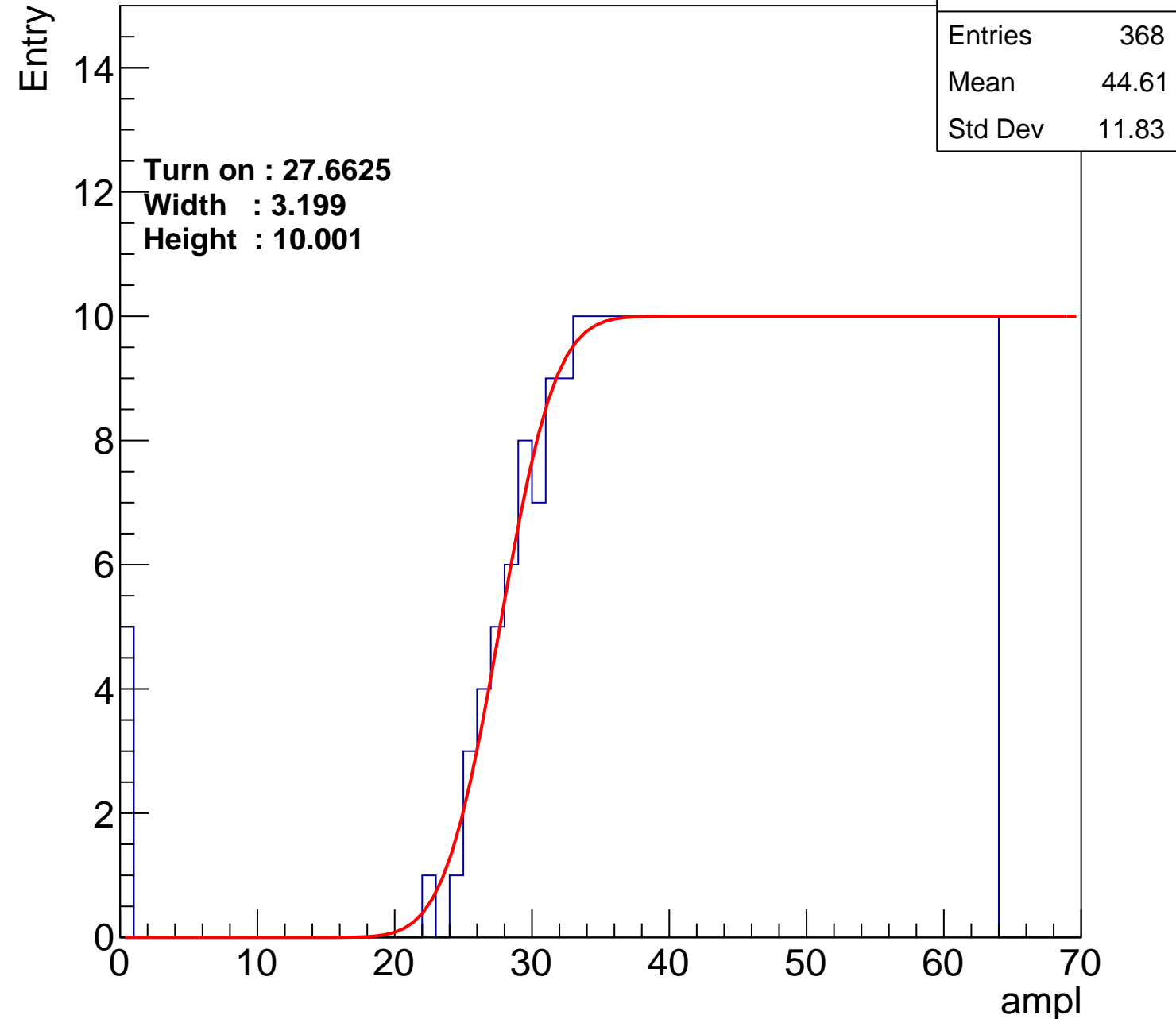
Width : 3.199

Height : 10.001

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch124

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	362
Mean	45.06
Std Dev	11.29

Turn on : 28.3584

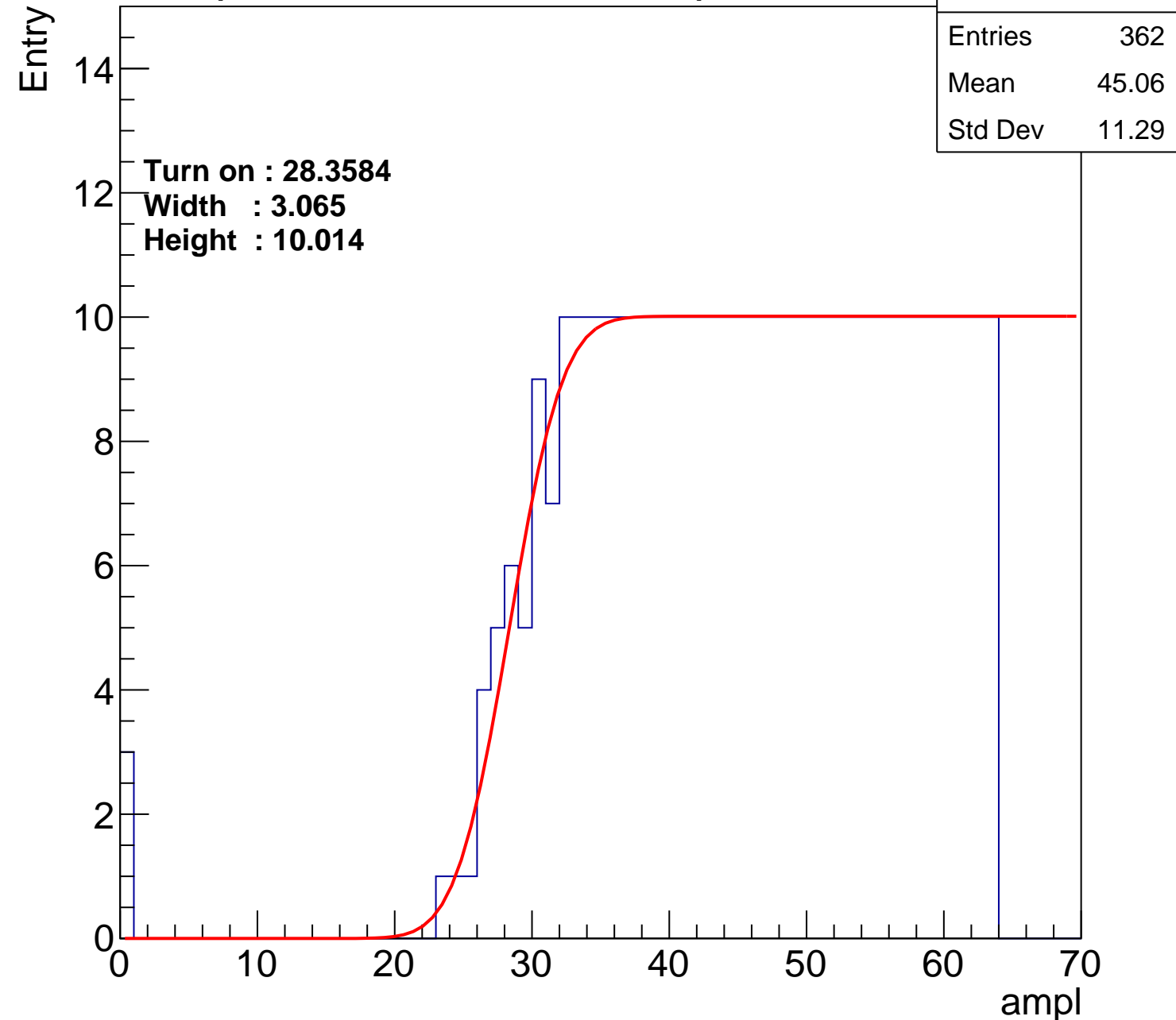
Width : 3.065

Height : 10.014

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch125

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	381
Mean	44.05
Std Dev	11.94

**Turn on : 26.7685**

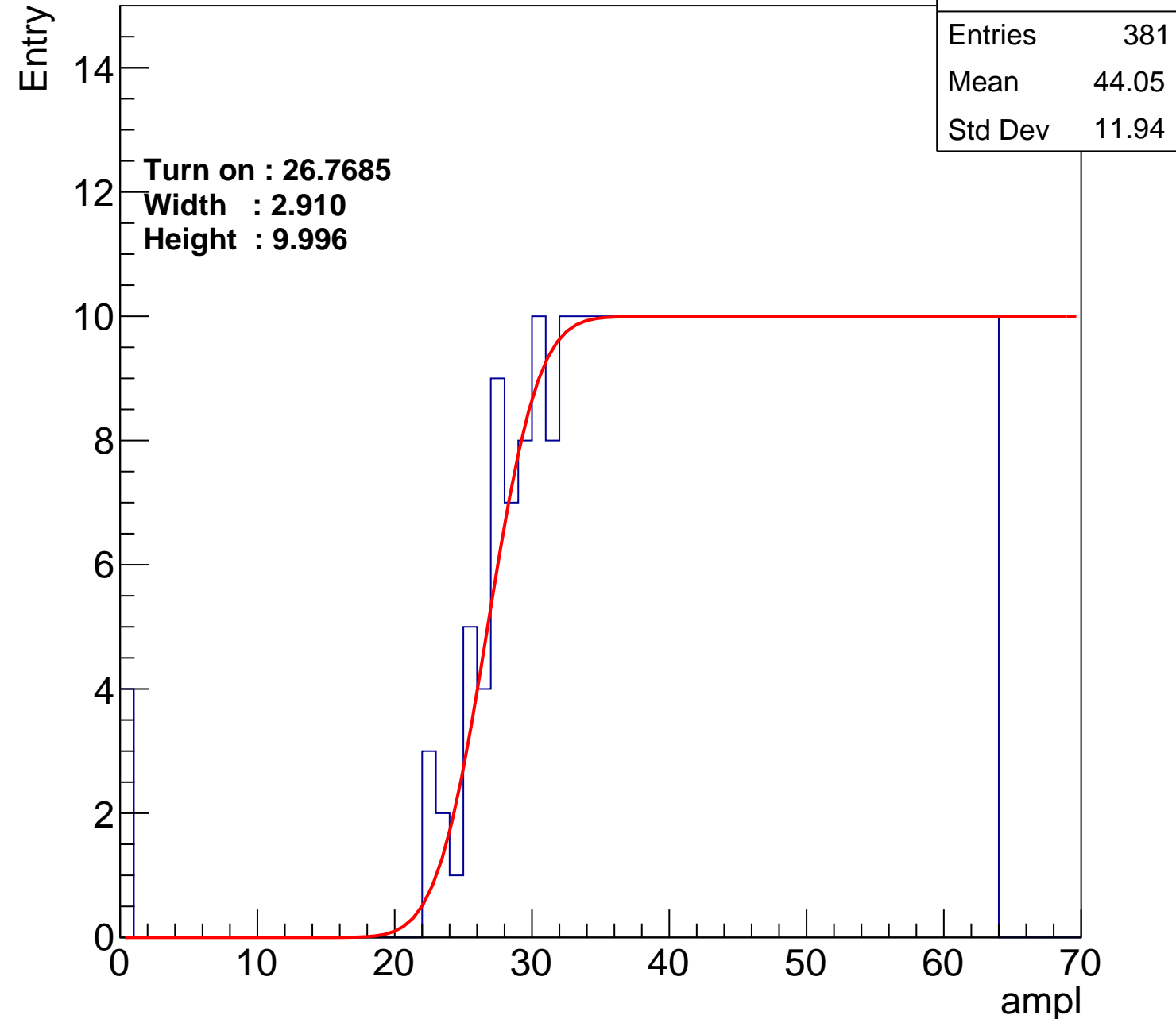
**Width : 2.910**

**Height : 9.996**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch126

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	387
Mean	43.84
Std Dev	11.88

Turn on : 25.8127

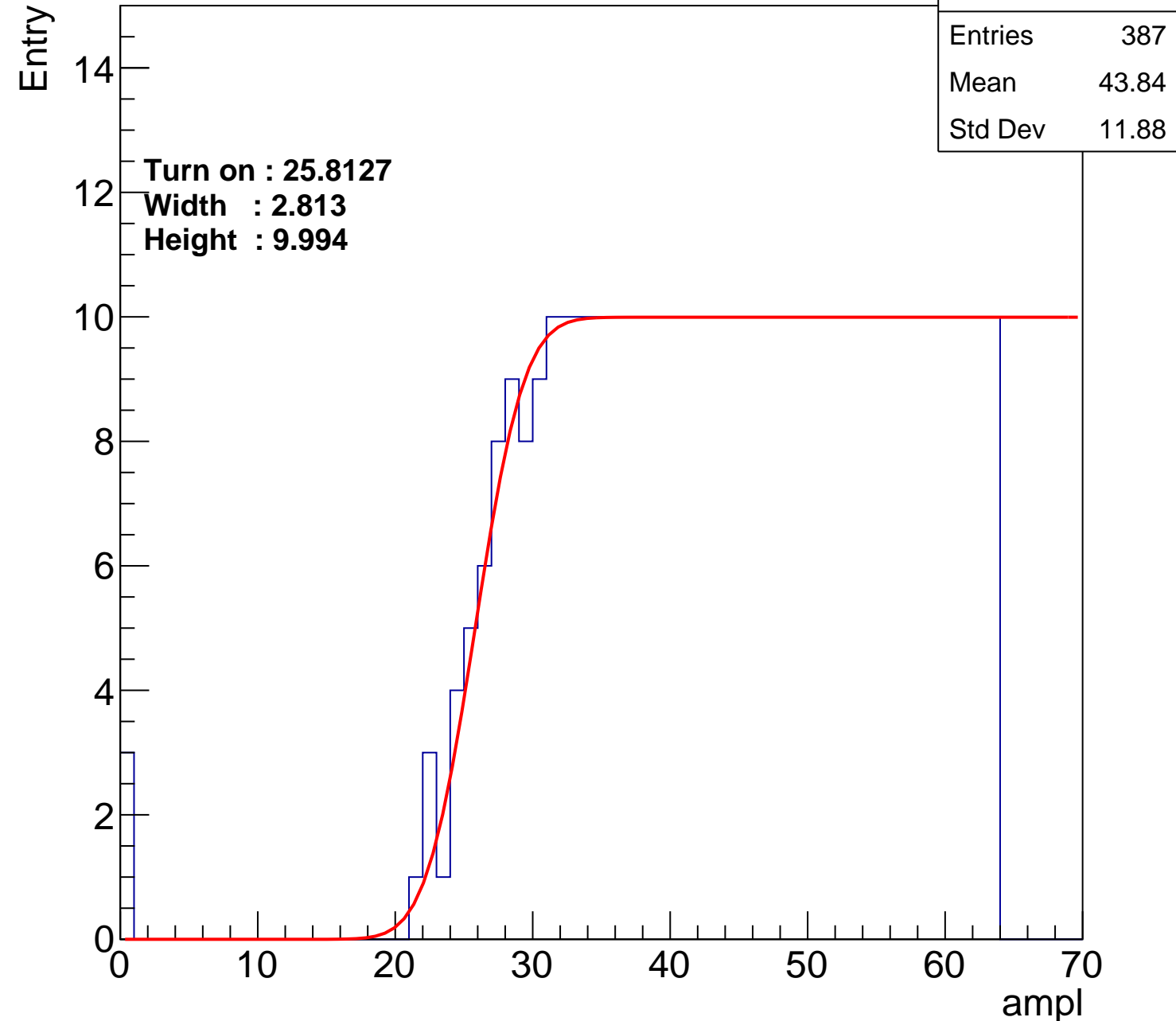
Width : 2.813

Height : 9.994

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U25-ch127

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	356
Mean	45.42
Std Dev	10.95

Turn on : 28.3456

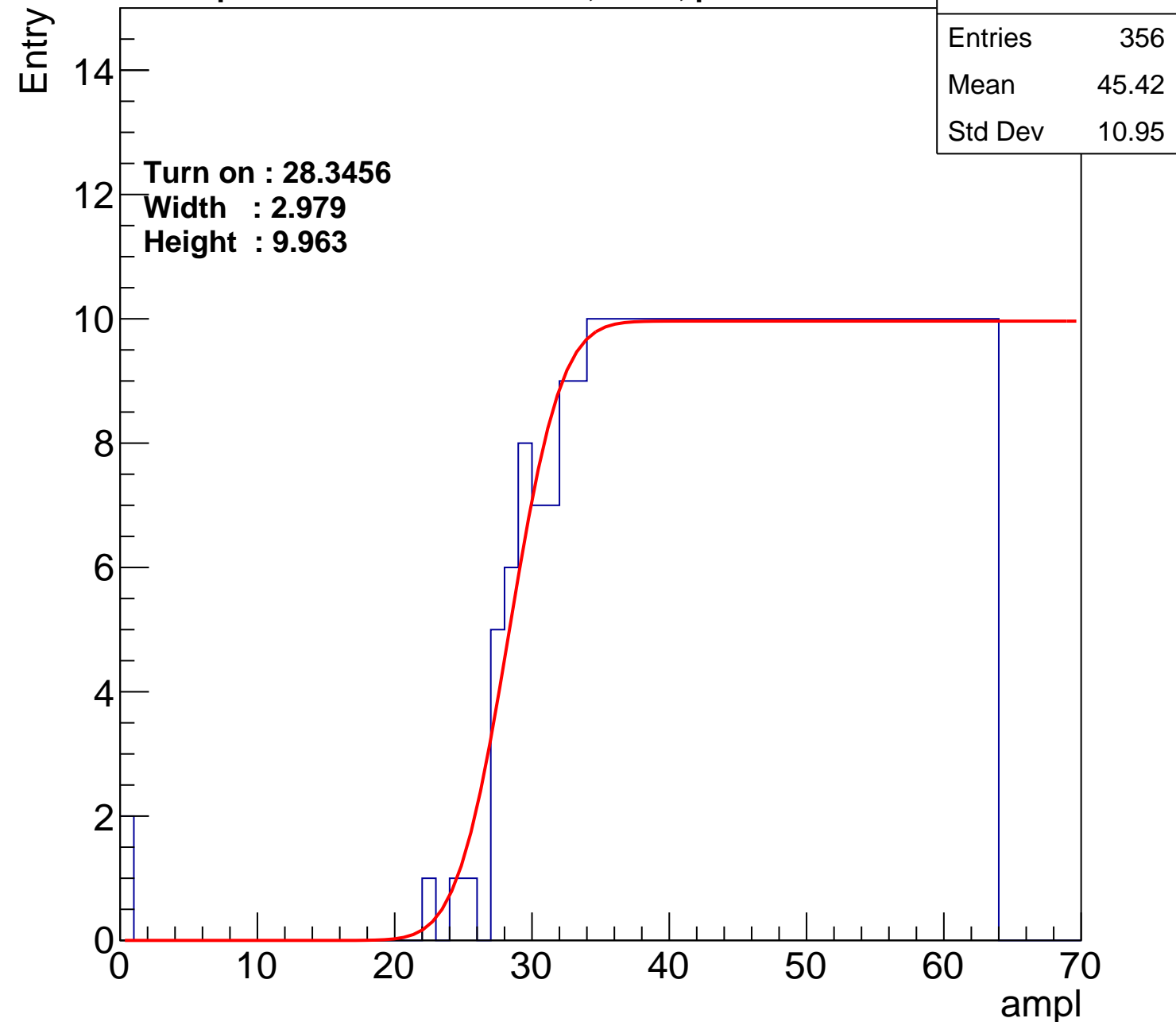
Width : 2.979

Height : 9.963

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U25-ch127

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	356
Mean	45.42
Std Dev	10.95

**Turn on : 28.3456**

**Width : 2.979**

**Height : 9.963**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

