B0L101S, U10-ch0

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch1

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch2

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0
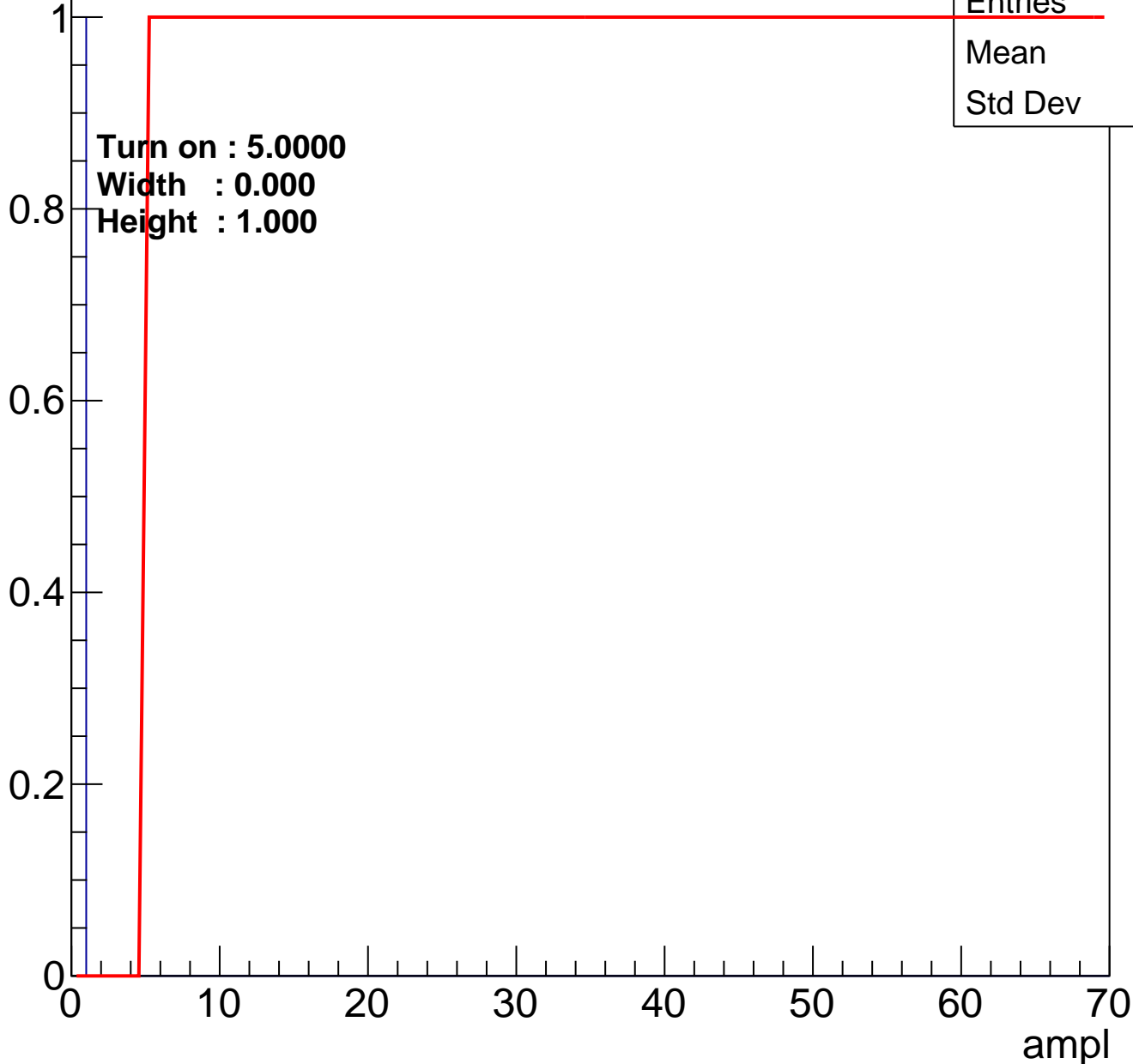
Turn on : 5.0000
Width   : 0.000
Height : 1.000

B0L101S, U10-ch3

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000
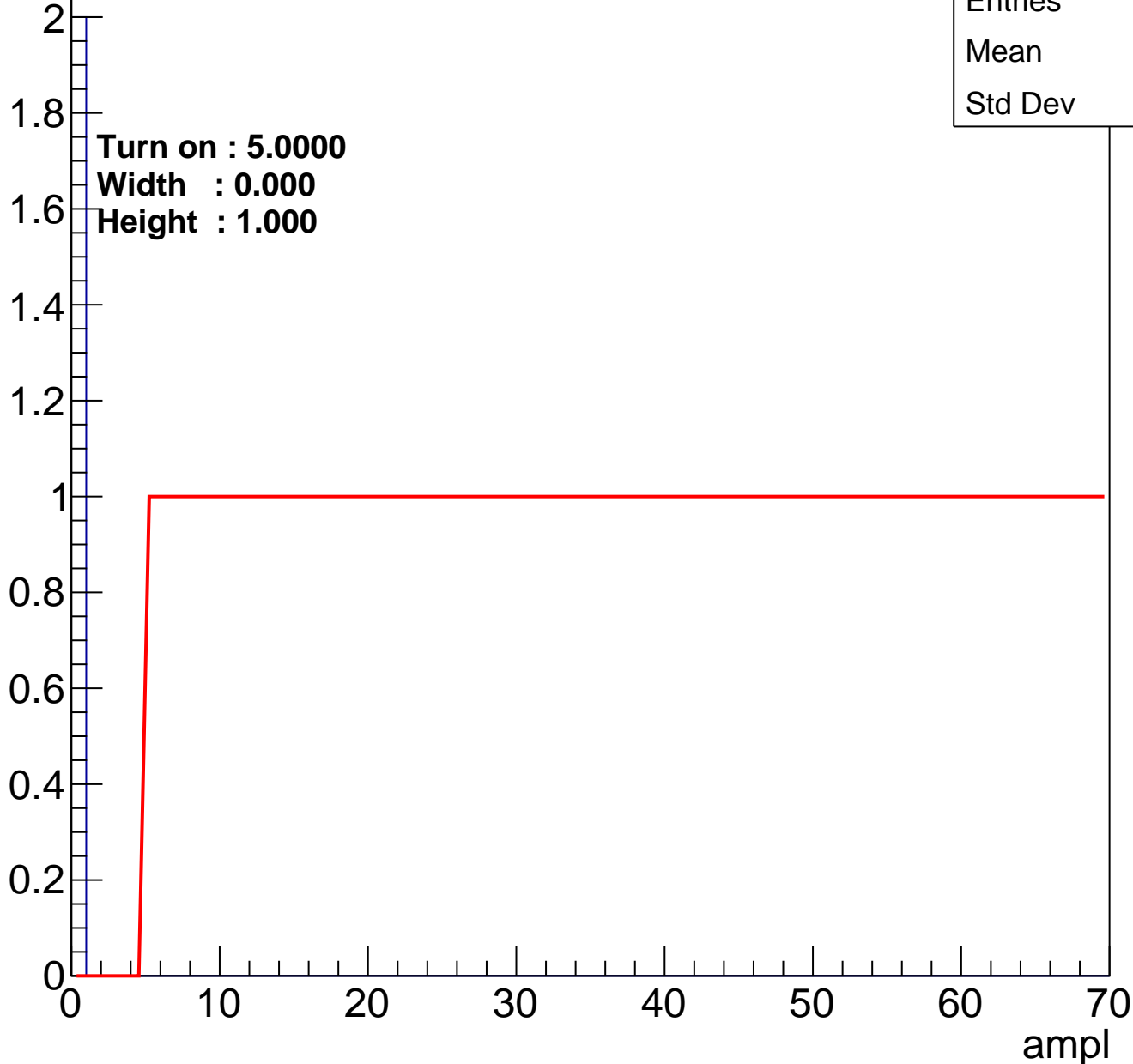
Entry

ampl

B0L101S, U10-ch4

calib_packv5_042523_0143.root, FC#1, port C1

Entry

Entries	3
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl
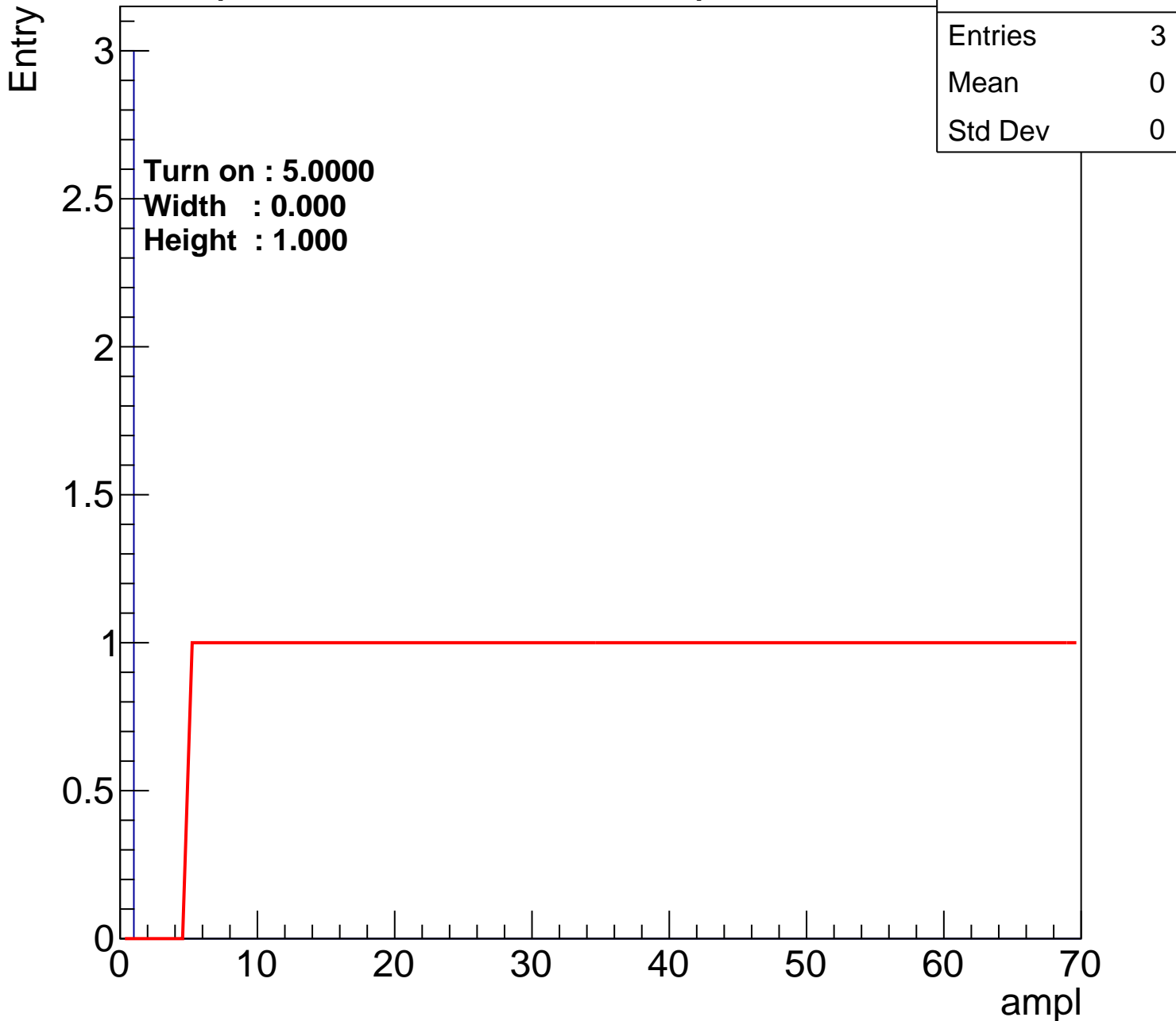
B0L101S, U10-ch5

calib_packv5_042523_0143.root, FC#1, port C1

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	2
Mean	0
Std Dev	0

B0L101S, U10-ch6

Entry

Entries		1
Mean		0
Std Dev		0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl

B0L101S, U10-ch7

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
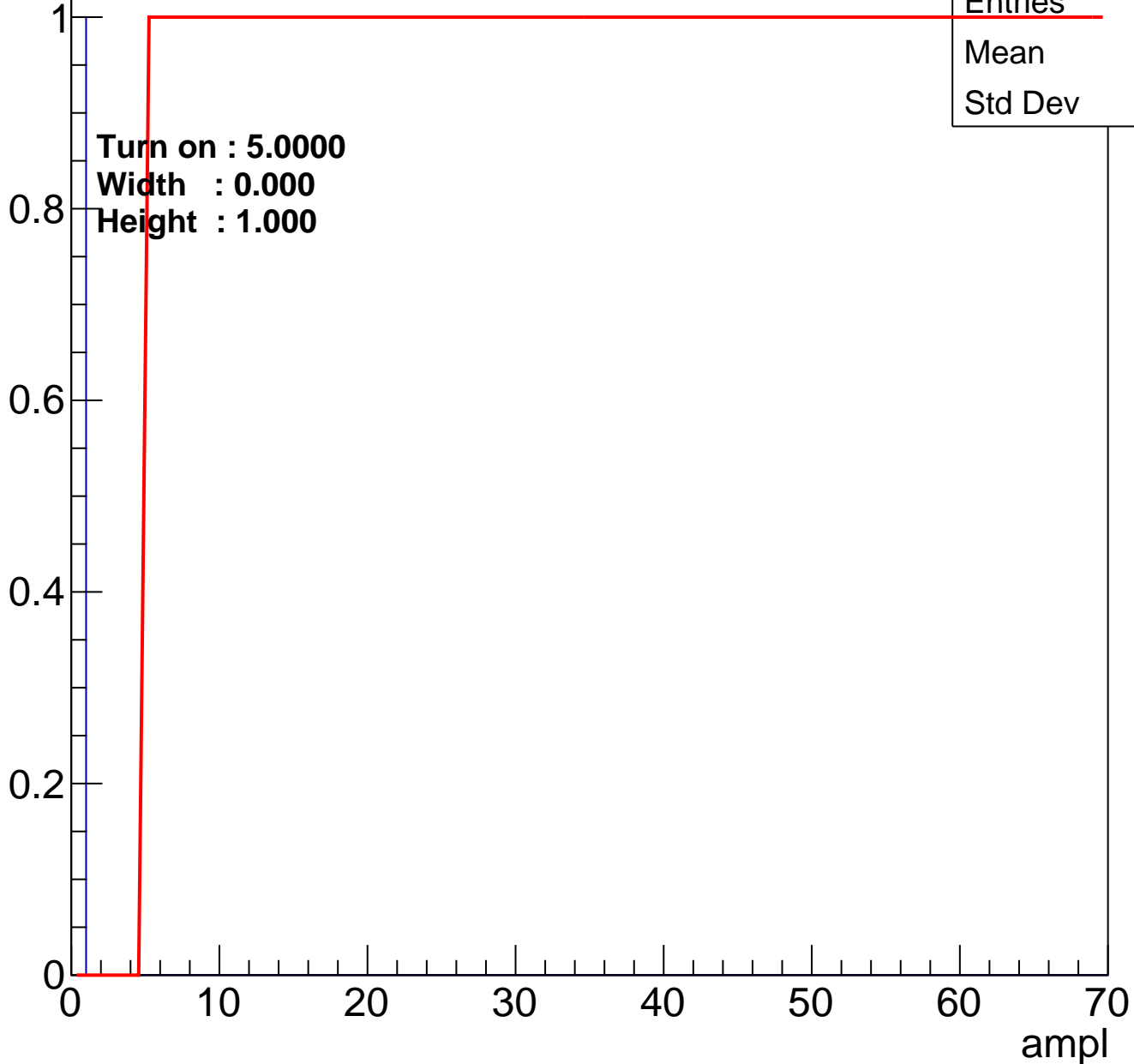
B0L101S, U10-ch8

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch9

calib_packv5_042523_0143.root, FC#1, port C1

Entries	0
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
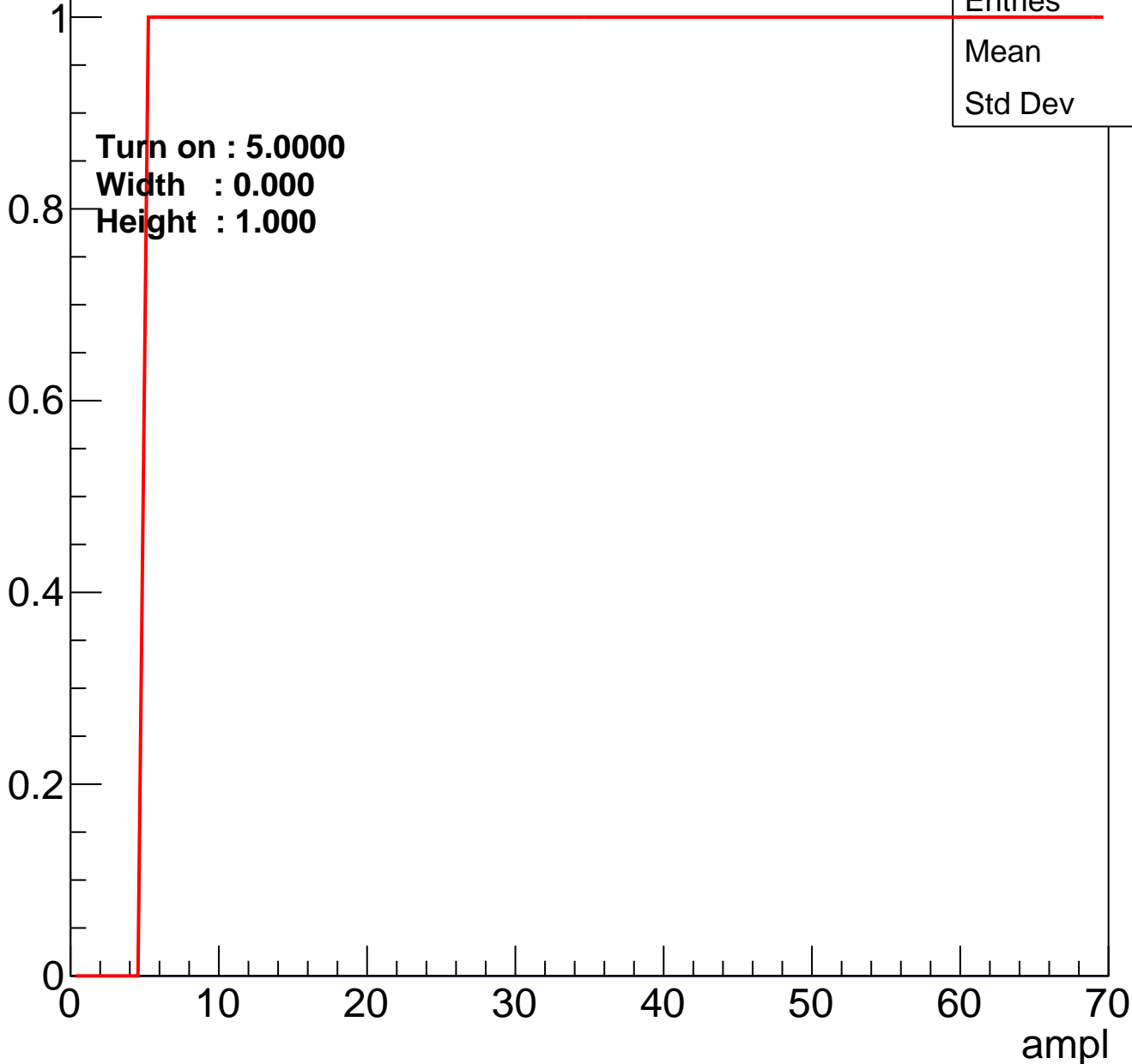
B0L101S, U10-ch10

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
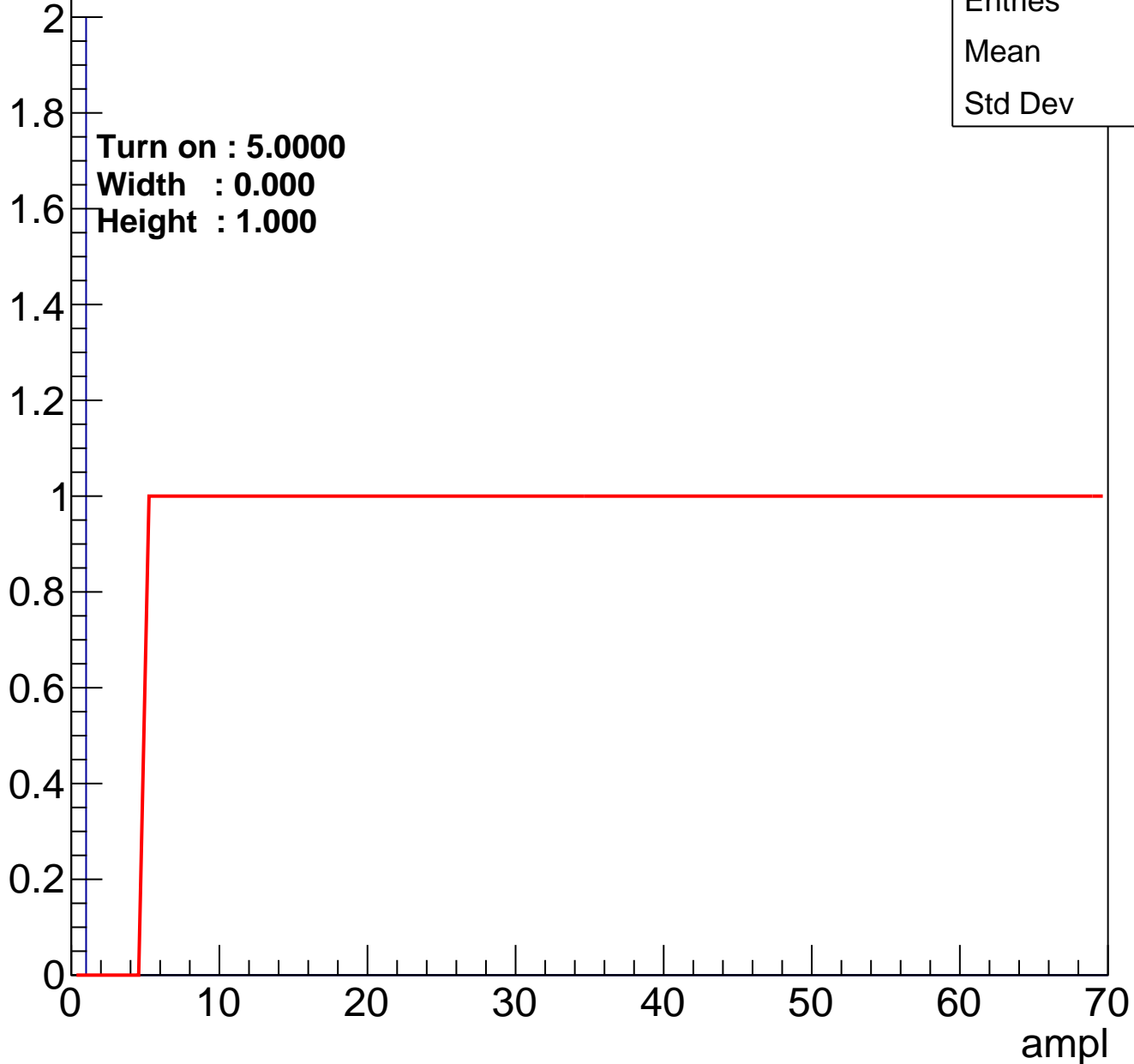
B0L101S, U10-ch11

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch12

calib_packv5_042523_0143.root, FC#1, port C1

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	1
Mean	0
Std Dev	0

B0L101S, U10-ch13

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch14

calib_packv5_042523_0143.root, FC#1, port C1

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	0
Mean	0
Std Dev	0

Entry

ampl

B0L101S, U10-ch15

calib_packv5_042523_0143.root, FC#1, port C1

Entries	3
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch16

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch17

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch18

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch19

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch20

calib_packv5_042523_0143.root, FC#1, port C1

Entry

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	1
Mean	0
Std Dev	0

ampl
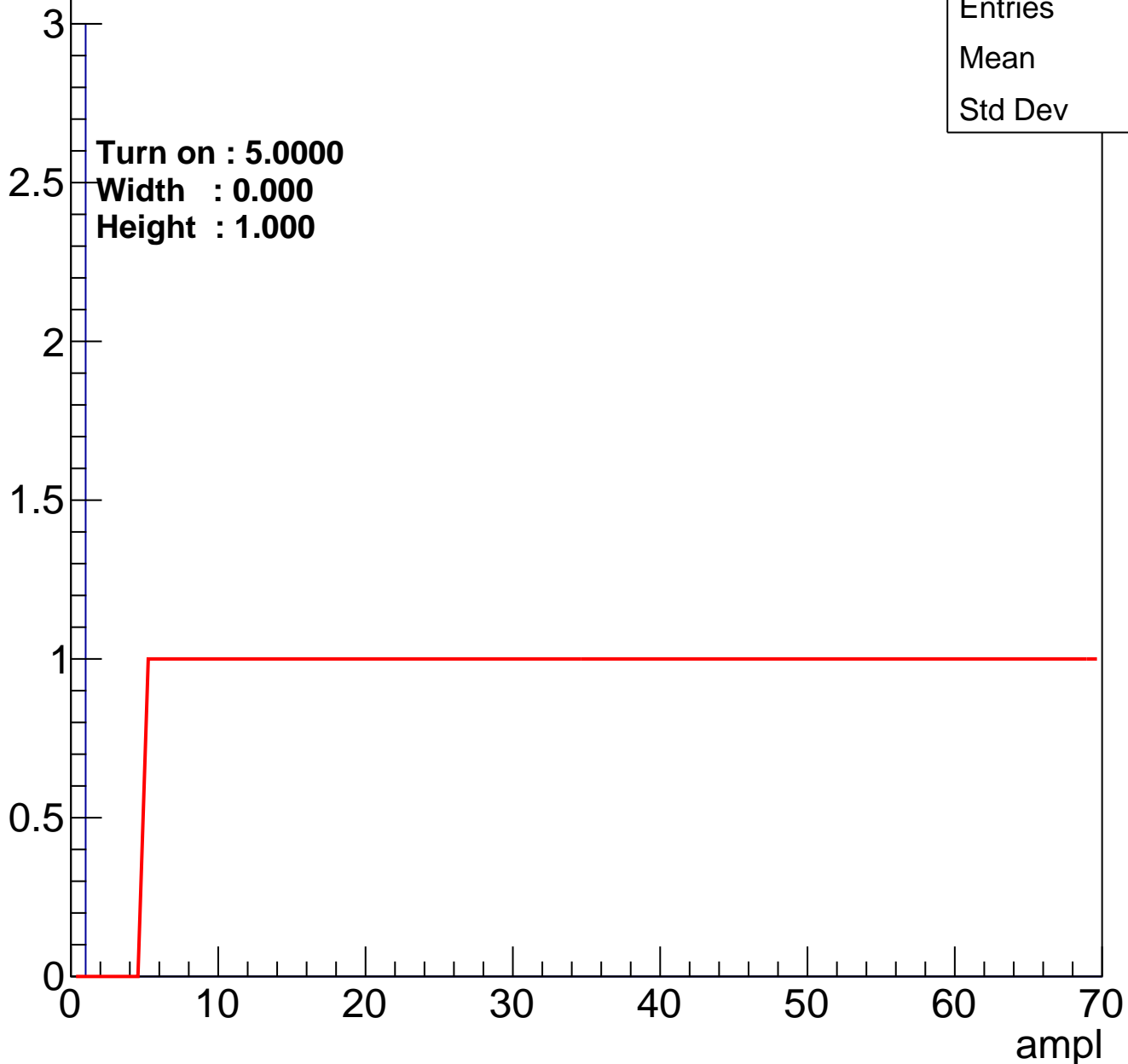
B0L101S, U10-ch21

calib_packv5_042523_0143.root, FC#1, port C1

Entries	3
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch22

calib_packv5_042523_0143.root, FC#1, port C1

Entries	0
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch23

calib_packv5_042523_0143.root, FC#1, port C1

Entries	4
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
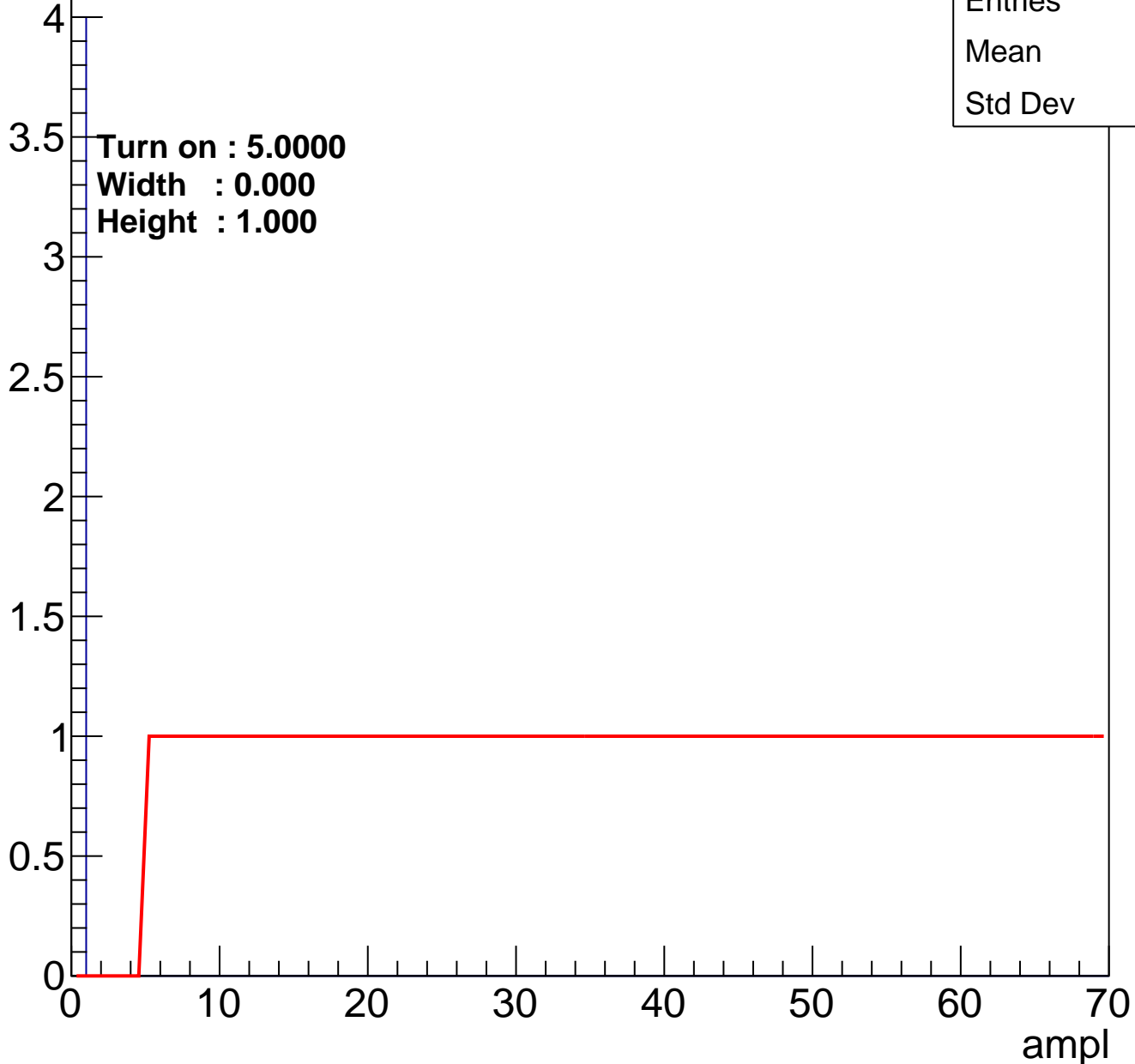
B0L101S, U10-ch24

calib_packv5_042523_0143.root, FC#1, port C1

Entries	3
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
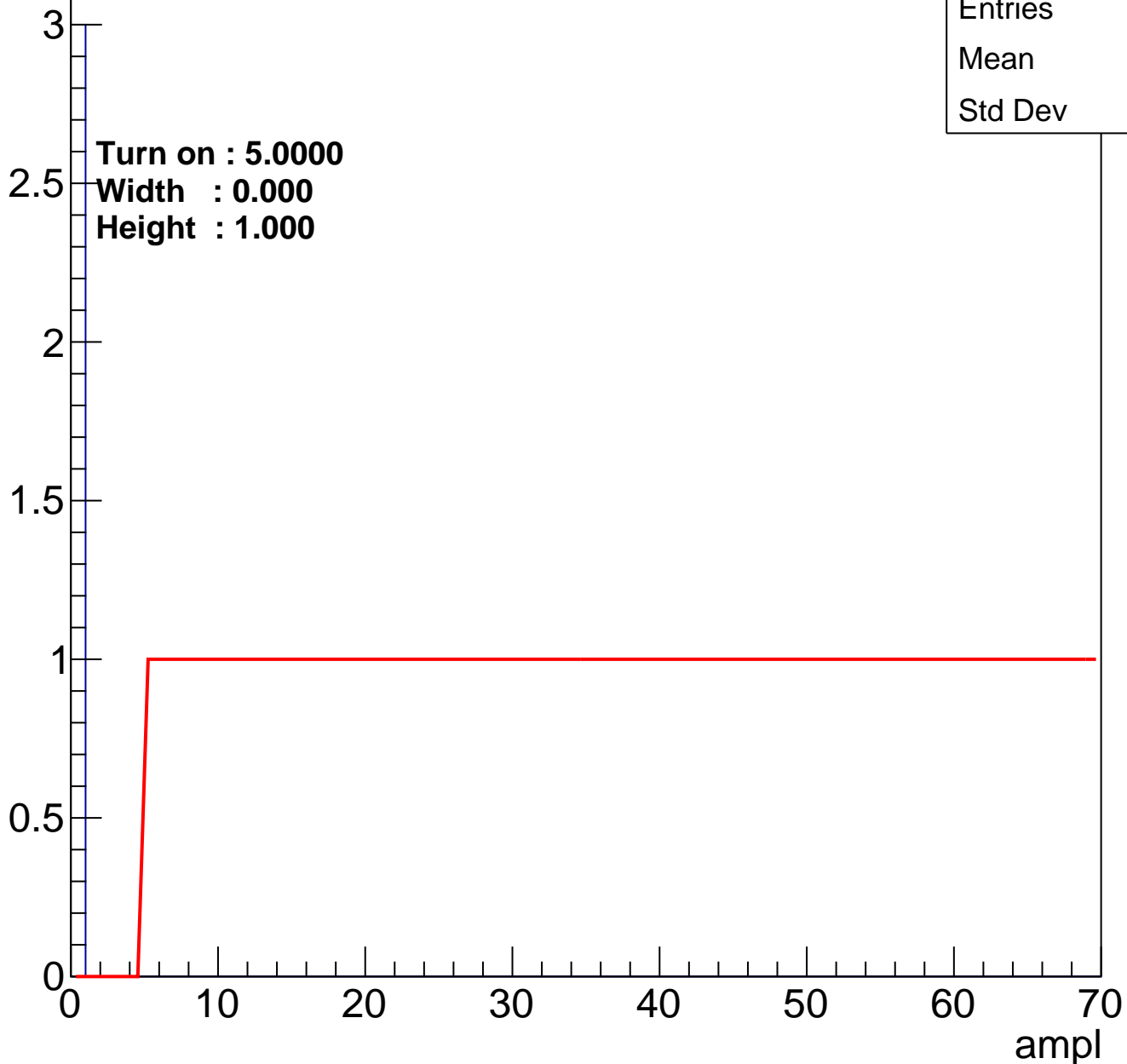
B0L101S, U10-ch25

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width : 0.000
Height : 1.000

B0L101S, U10-ch26

calib_packv5_042523_0143.root, FC#1, port C1

Entry

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl

B0L101S, U10-ch27

calib_packv5_042523_0143.root, FC#1, port C1

Entries	4
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
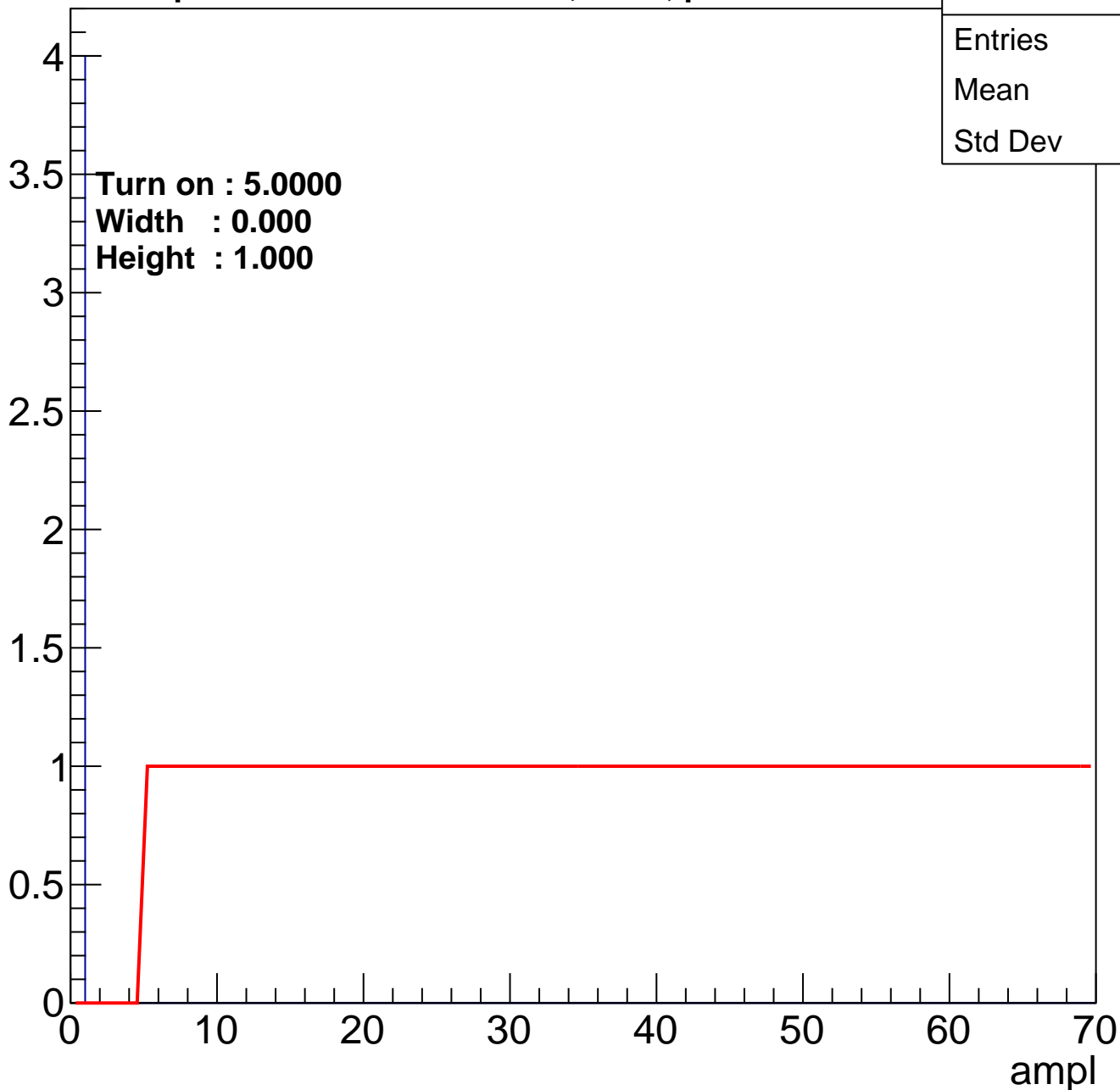
B0L101S, U10-ch28

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
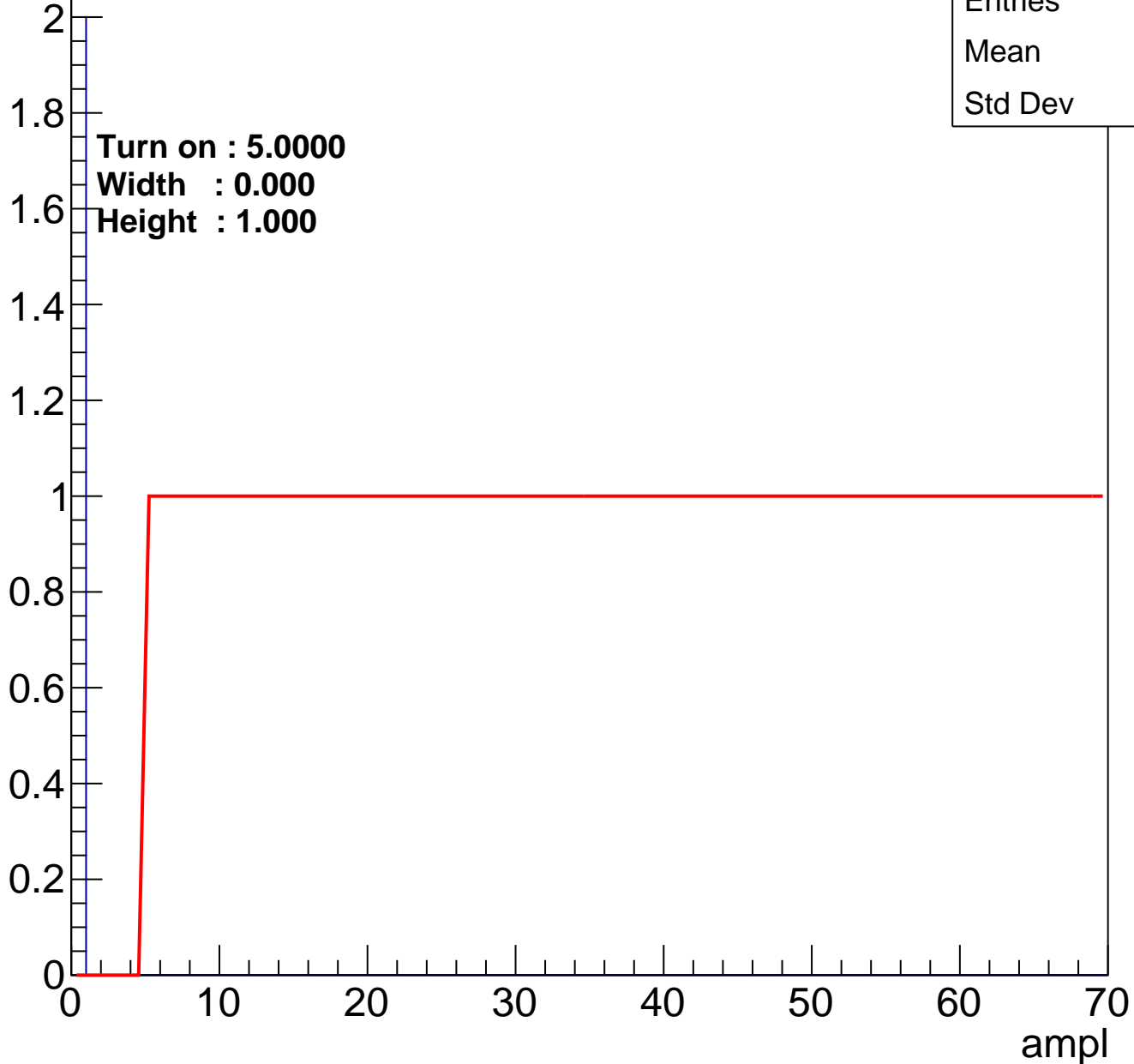
B0L101S, U10-ch29

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

B0L101S, U10-ch30

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch31

calib_packv5_042523_0143.root, FC#1, port C1

Entries	3
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch32

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000
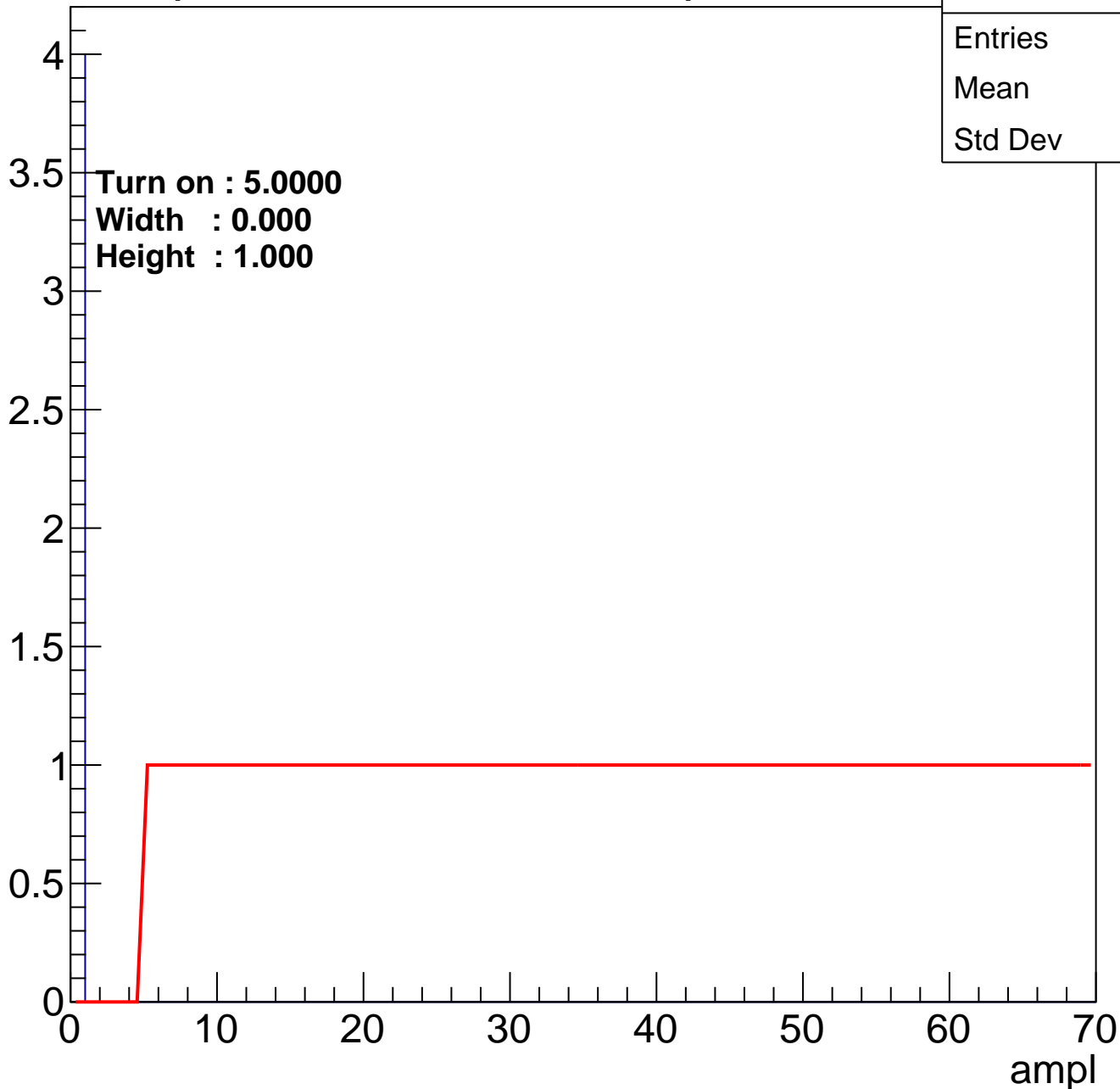
B0L101S, U10-ch33

calib_packv5_042523_0143.root, FC#1, port C1

Entries	4
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch34

calib_packv5_042523_0143.root, FC#1, port C1

Entries	3
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch35

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch36

calib_packv5_042523_0143.root, FC#1, port C1

Entries	0
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch37

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch38

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch39

calib_packv5_042523_0143.root, FC#1, port C1

Entries	0
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch40

calib_packv5_042523_0143.root, FC#1, port C1

Entries	3
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
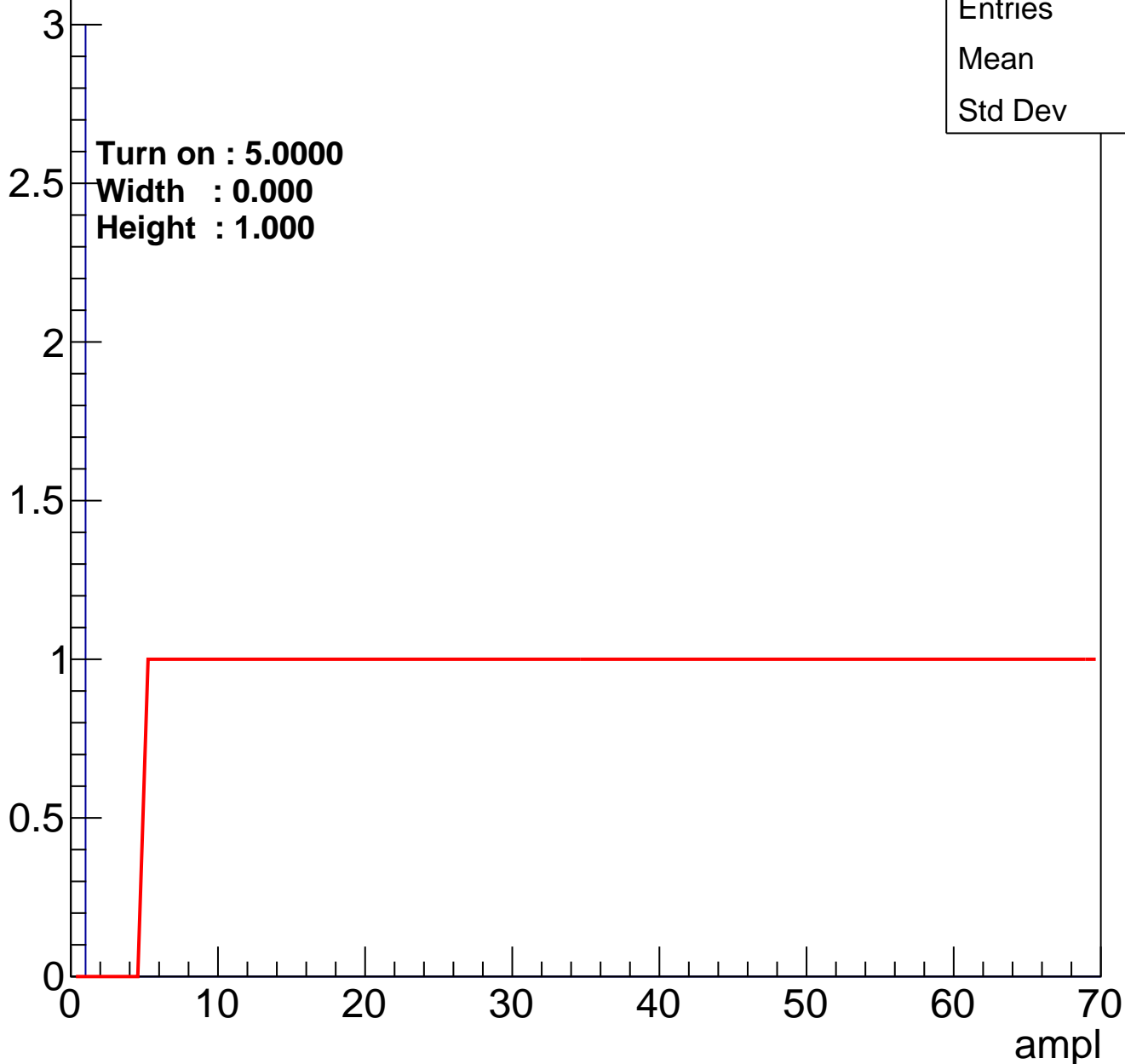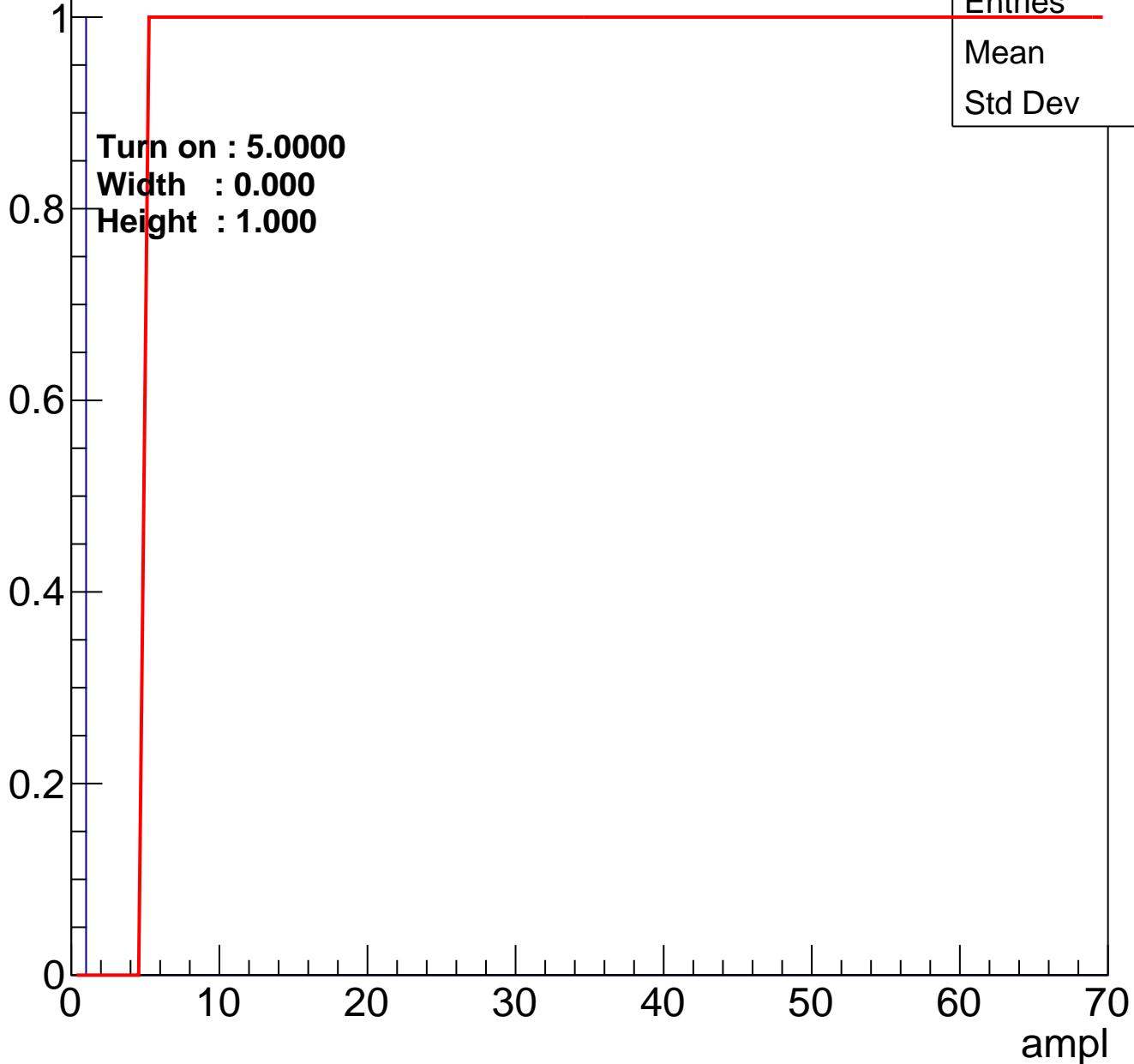
B0L101S, U10-ch41

calib_packv5_042523_0143.root, FC#1, port C1

Turn on : 5.0000
Width : 0.000
Height : 1.000

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B0L101S, U10-ch42

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch43

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch44

calib_packv5_042523_0143.root, FC#1, port C1

Entries	0
Mean	0
Std Dev	0

Turn on : 5.0000
Width : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch45

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	1
Mean	0
Std Dev	0

Entry

ampl
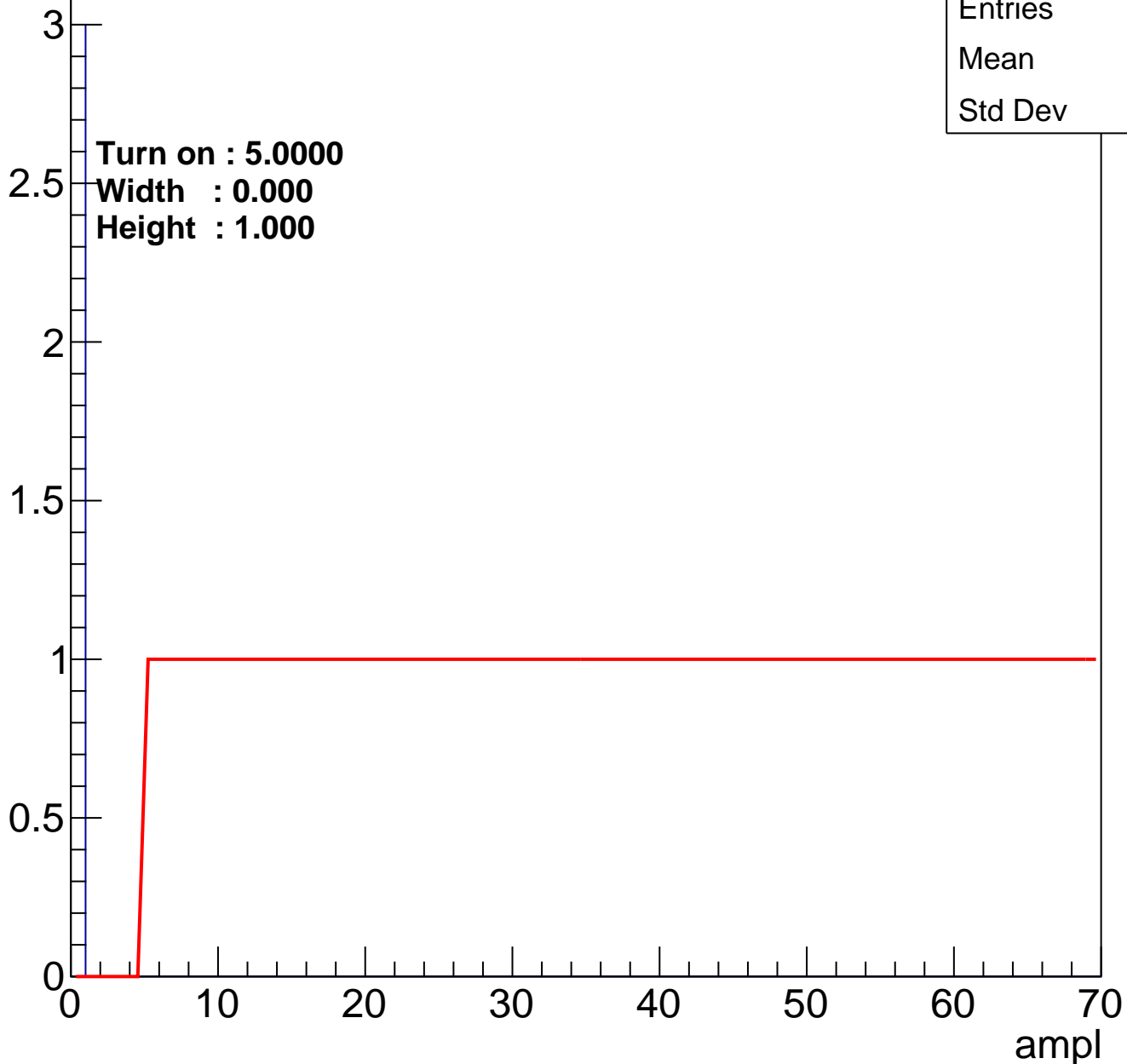
B0L101S, U10-ch46

calib_packv5_042523_0143.root, FC#1, port C1

Entry

Entries	3
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl

B0L101S, U10-ch47

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch48

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch49

calib_packv5_042523_0143.root, FC#1, port C1

Entries	0
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch50

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch51

calib_packv5_042523_0143.root, FC#1, port C1

Entry

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl

B0L101S, U10-ch52

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch53

Entry

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl

B0L101S, U10-ch54

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch55

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch56

calib_packv5_042523_0143.root, FC#1, port C1

Entries	11
Mean	6.182
Std Dev	8.178

Turn on : 15.3550
Width   : 0.420
Height : 2.000
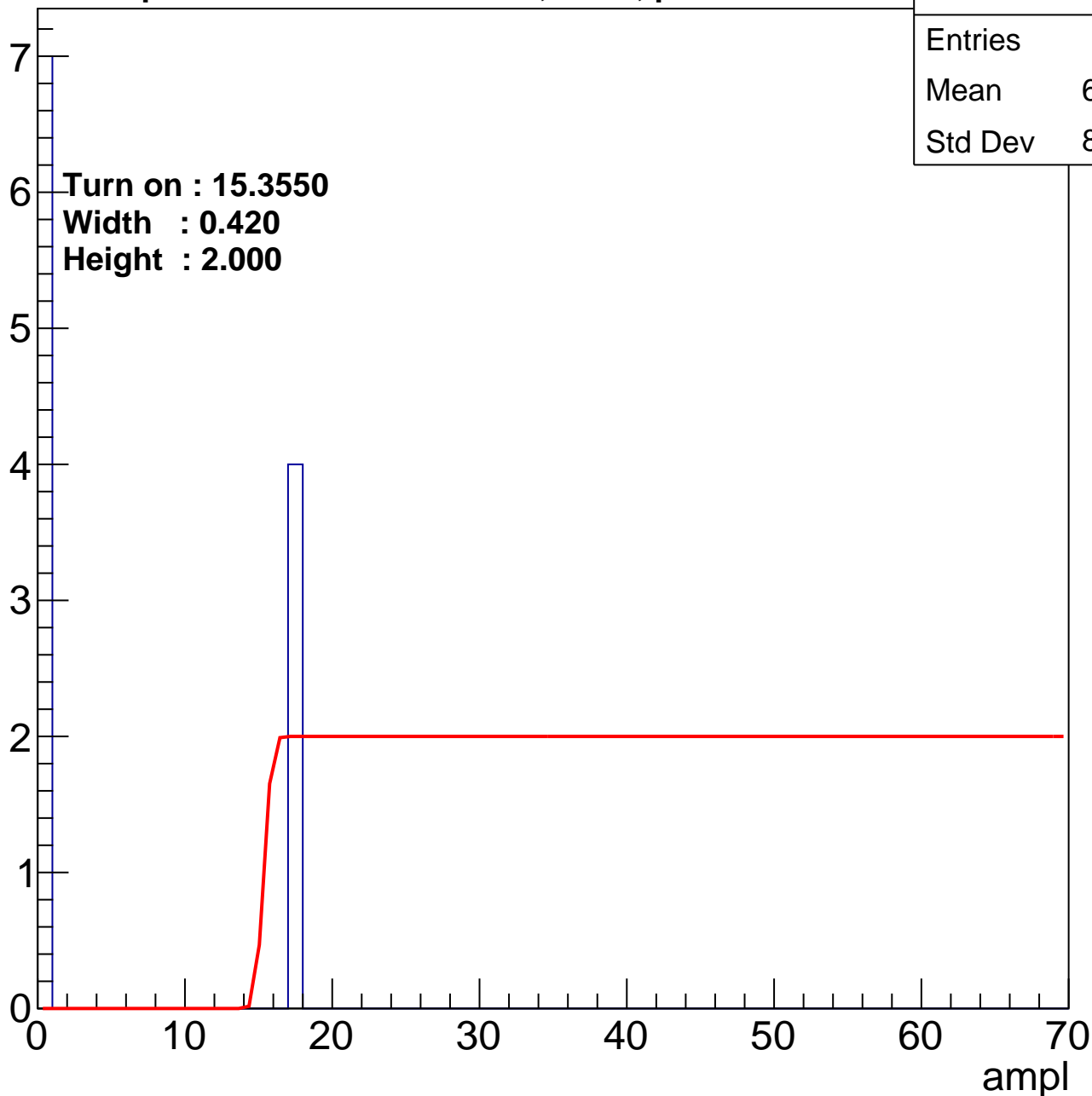
B0L101S, U10-ch57

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch58

calib_packv5_042523_0143.root, FC#1, port C1

Entries	0
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch59

calib_packv5_042523_0143.root, FC#1, port C1

Entries	4
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
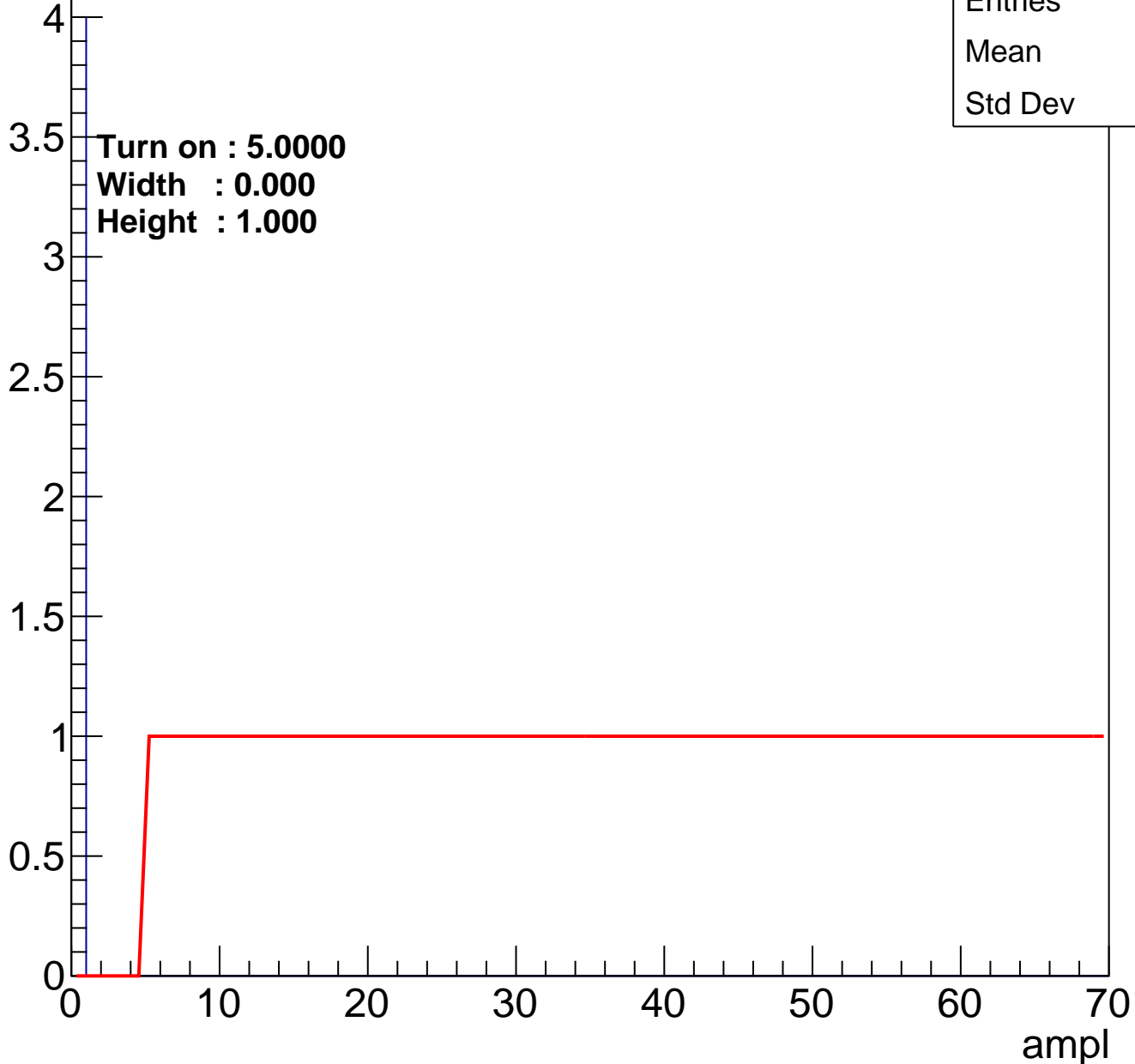
B0L101S, U10-ch60

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch61

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch62

calib_packv5_042523_0143.root, FC#1, port C1
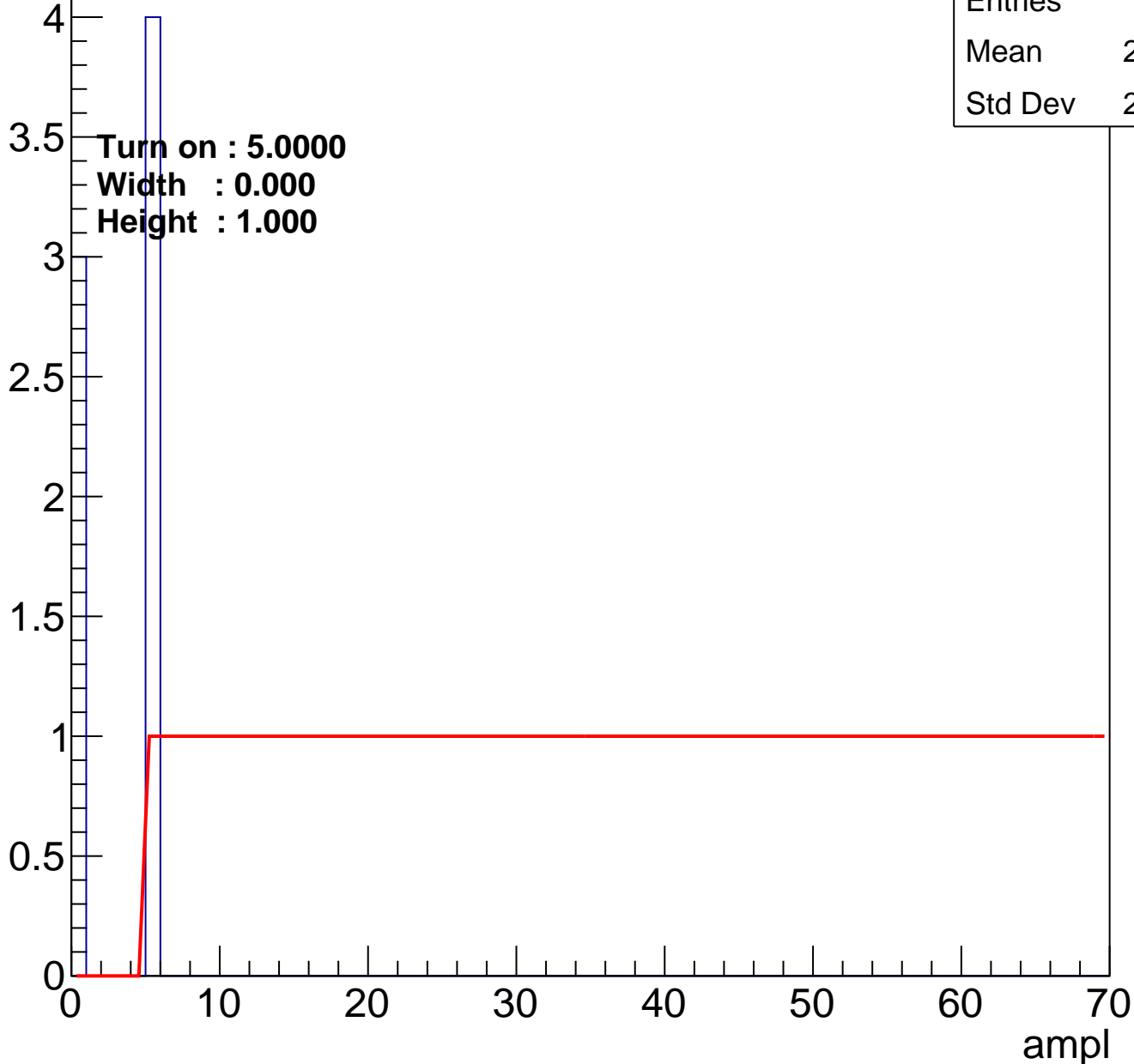
Entries	7
Mean	2.857
Std Dev	2.474

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch63

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch64

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch65

calib_packv5_042523_0143.root, FC#1, port C1

Entries	0
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch66

calib_packv5_042523_0143.root, FC#1, port C1
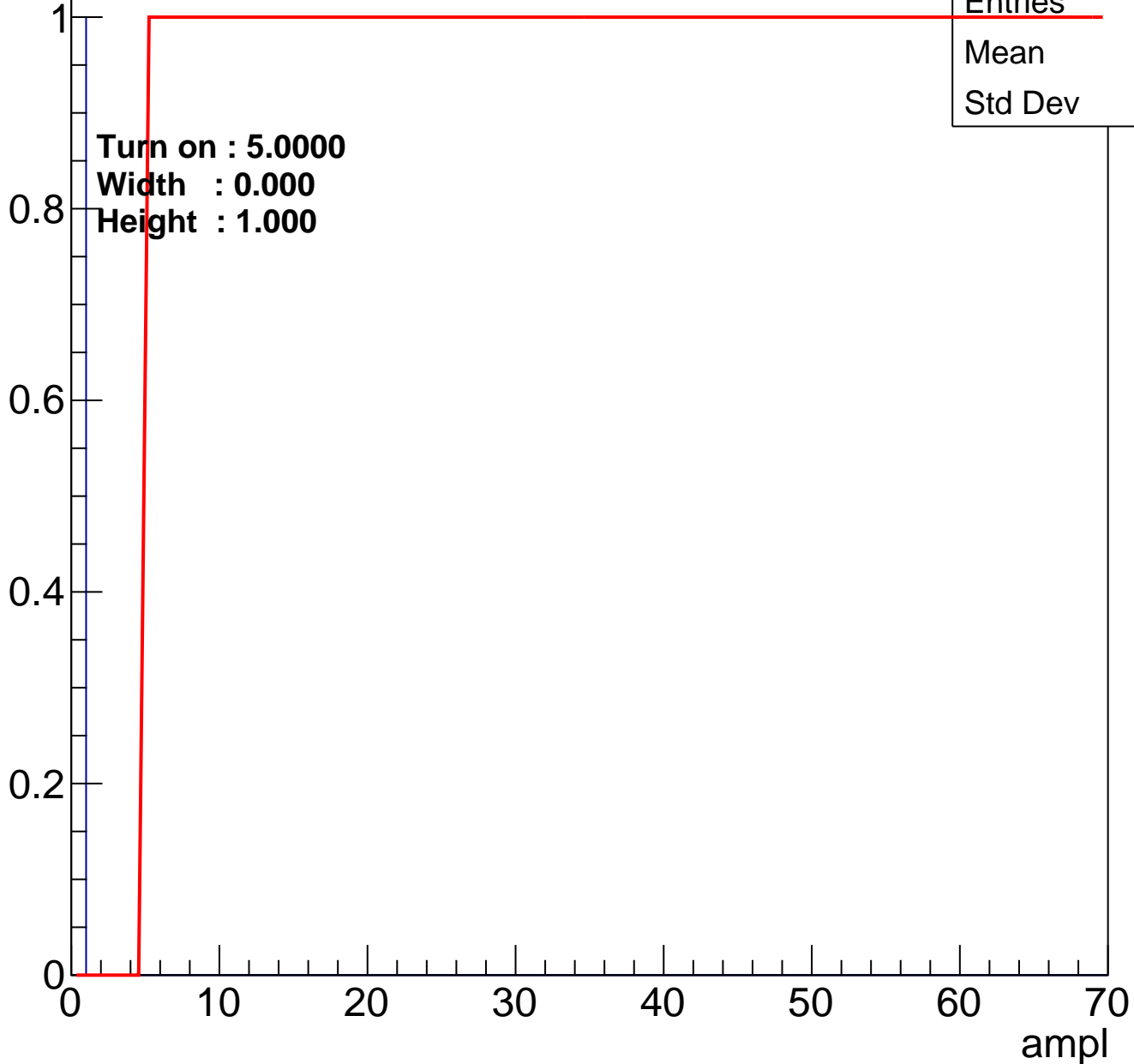
Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch67

Entry

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	2
Mean	0
Std Dev	0

ampl

B0L101S, U10-ch68

calib_packv5_042523_0143.root, FC#1, port C1

Entries	4
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
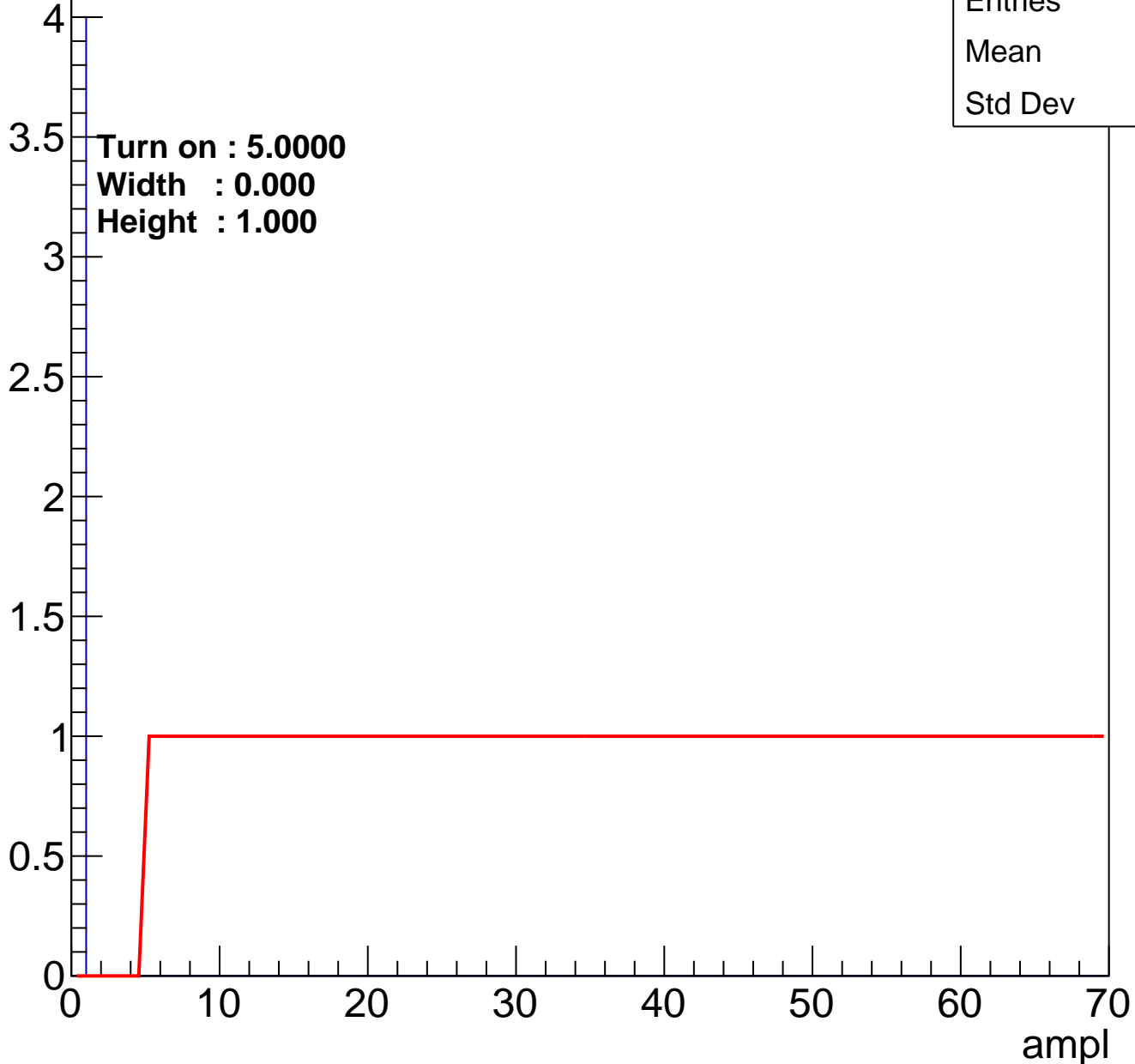
B0L101S, U10-ch69

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch70

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
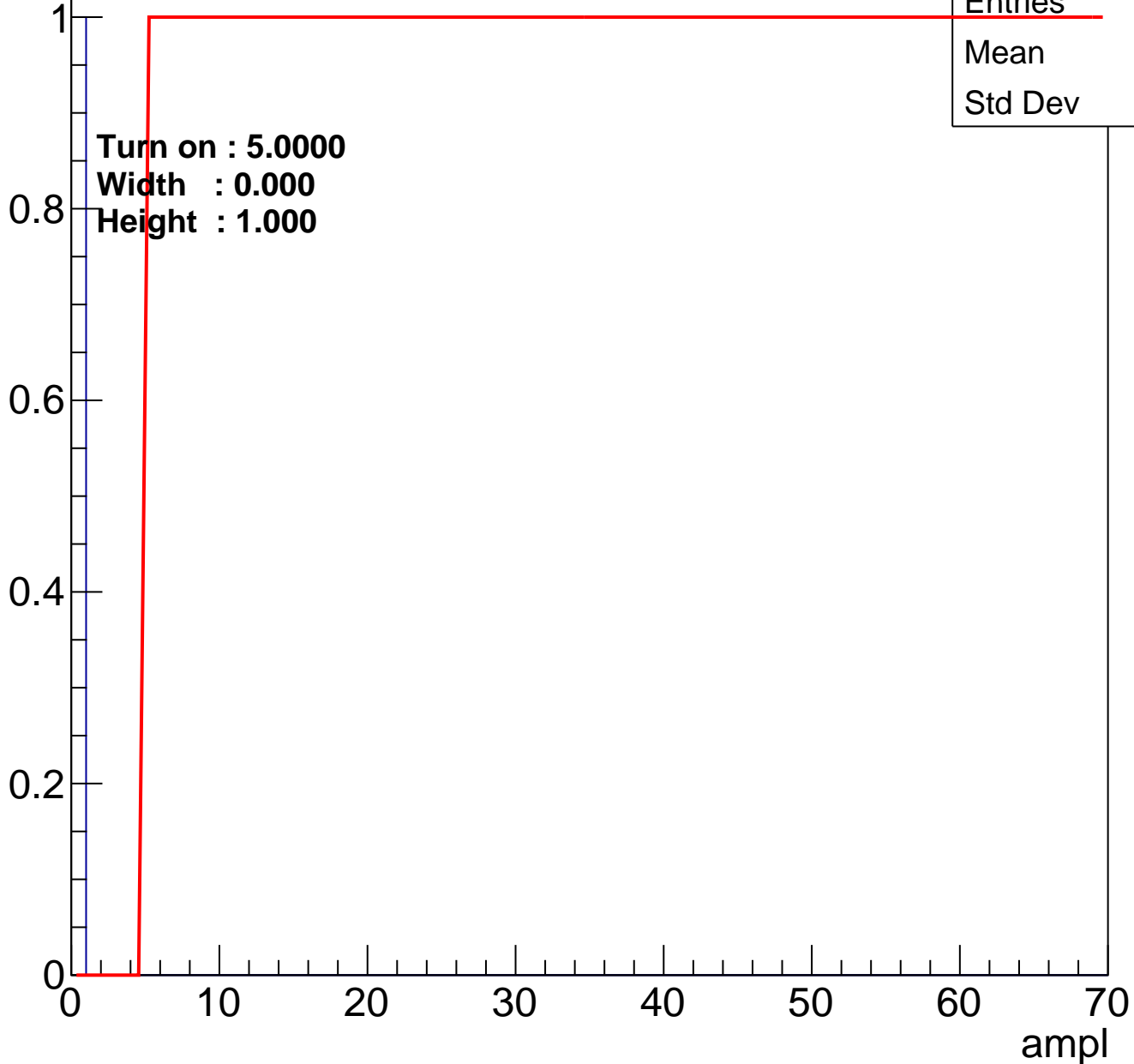
B0L101S, U10-ch71

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch72

calib_packv5_042523_0143.root, FC#1, port C1

Entries	0
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch73

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch74

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch75

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch76

calib_packv5_042523_0143.root, FC#1, port C1

Entries	3
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch77

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch78

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch79

calib_packv5_042523_0143.root, FC#1, port C1

Entries	3
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch80

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch81

calib_packv5_042523_0143.root, FC#1, port C1

Entries	4
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch82

calib_packv5_042523_0143.root, FC#1, port C1

Entries	5
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
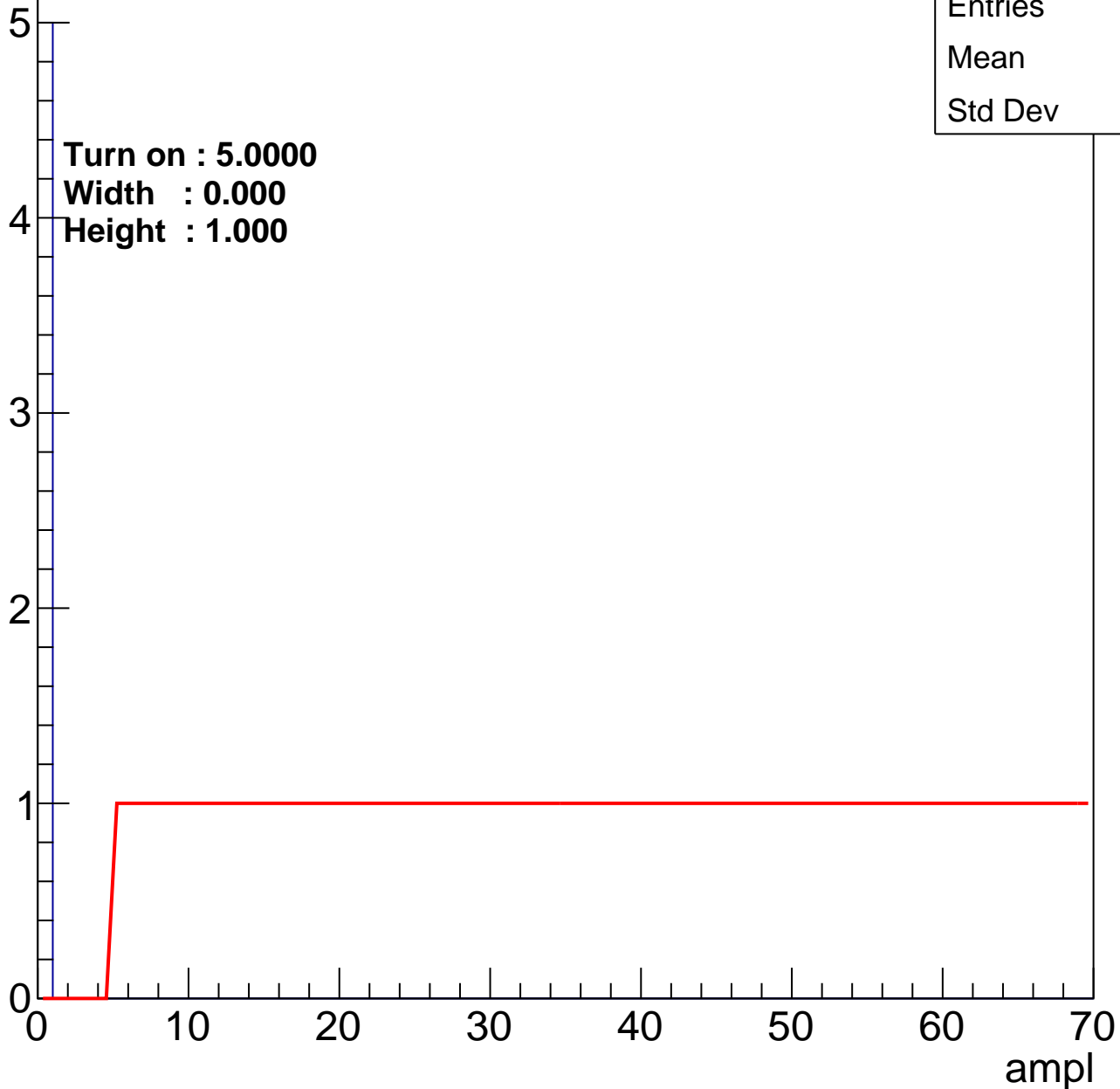
B0L101S, U10-ch83

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch84

calib_packv5_042523_0143.root, FC#1, port C1

Entry

Entries	3
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl

B0L101S, U10-ch85

calib_packv5_042523_0143.root, FC#1, port C1

Entries	4
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
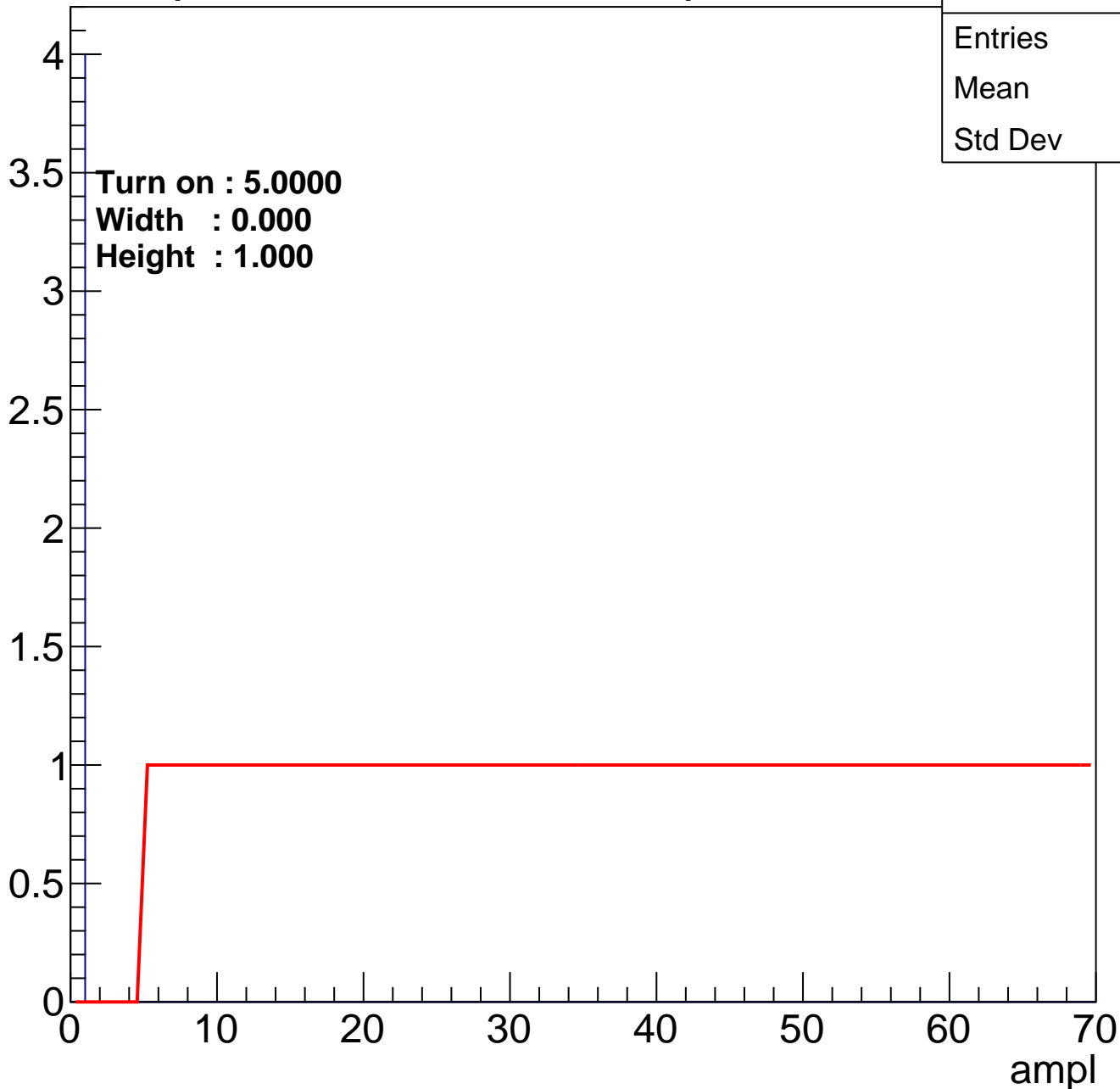
B0L101S, U10-ch86

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch87

calib_packv5_042523_0143.root, FC#1, port C1

Entries	3
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch88

calib_packv5_042523_0143.root, FC#1, port C1

Entries	5
Mean	5.8
Std Dev	11.6

Turn on : 5.0000
Width : 0.000
Height : 1.000

Entry

ampl
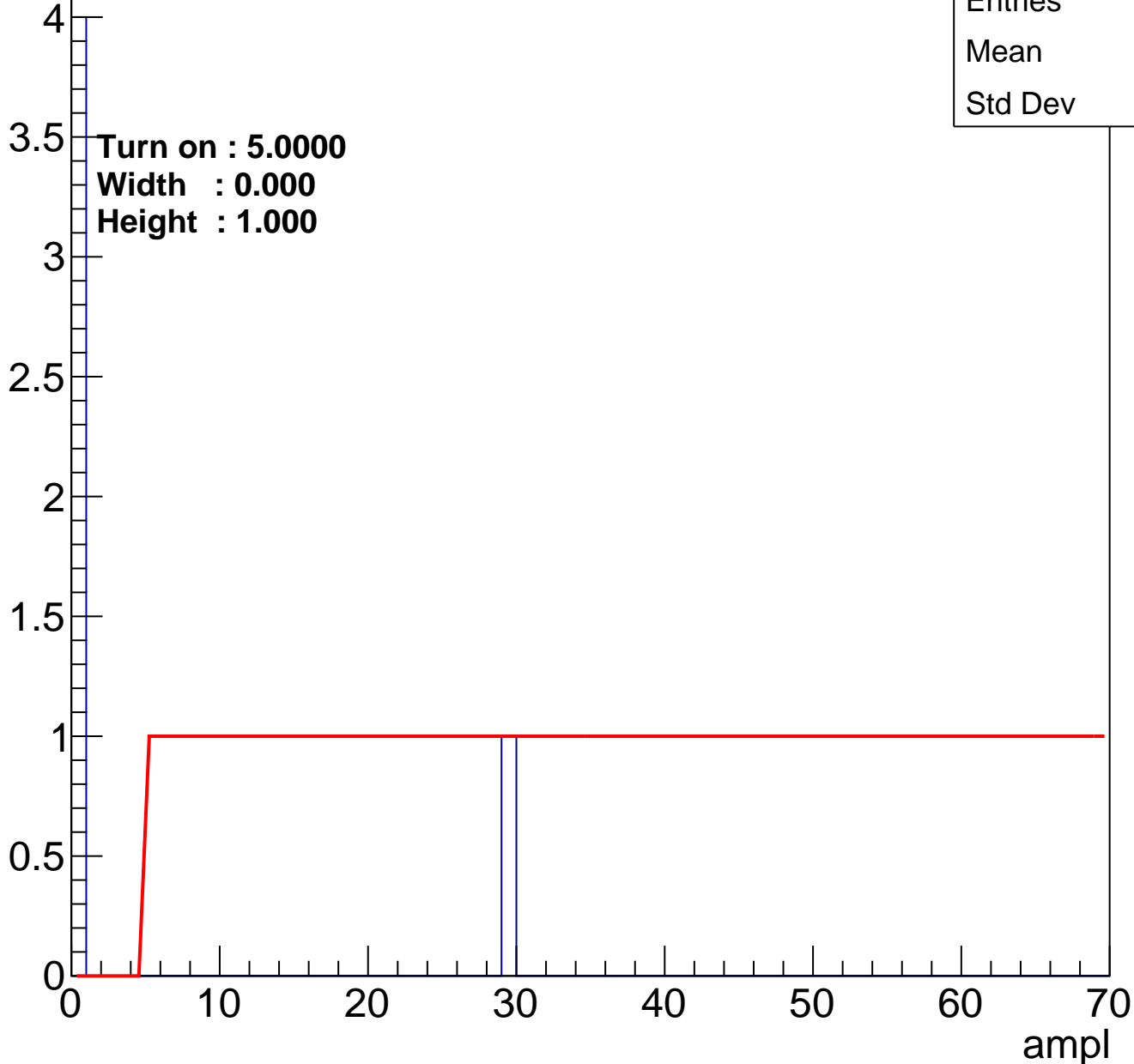
B0L101S, U10-ch89

calib_packv5_042523_0143.root, FC#1, port C1

Entries	0
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch90

calib_packv5_042523_0143.root, FC#1, port C1

Entries	0
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch91

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch92

calib_packv5_042523_0143.root, FC#1, port C1

Entries	3
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch93

calib_packv5_042523_0143.root, FC#1, port C1

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	1
Mean	0
Std Dev	0

Entry

ampl

B0L101S, U10-ch94

calib_packv5_042523_0143.root, FC#1, port C1

Entries	3
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch95

calib_packv5_042523_0143.root, FC#1, port C1

Entries	0
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch96

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch97

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch98

calib_packv5_042523_0143.root, FC#1, port C1
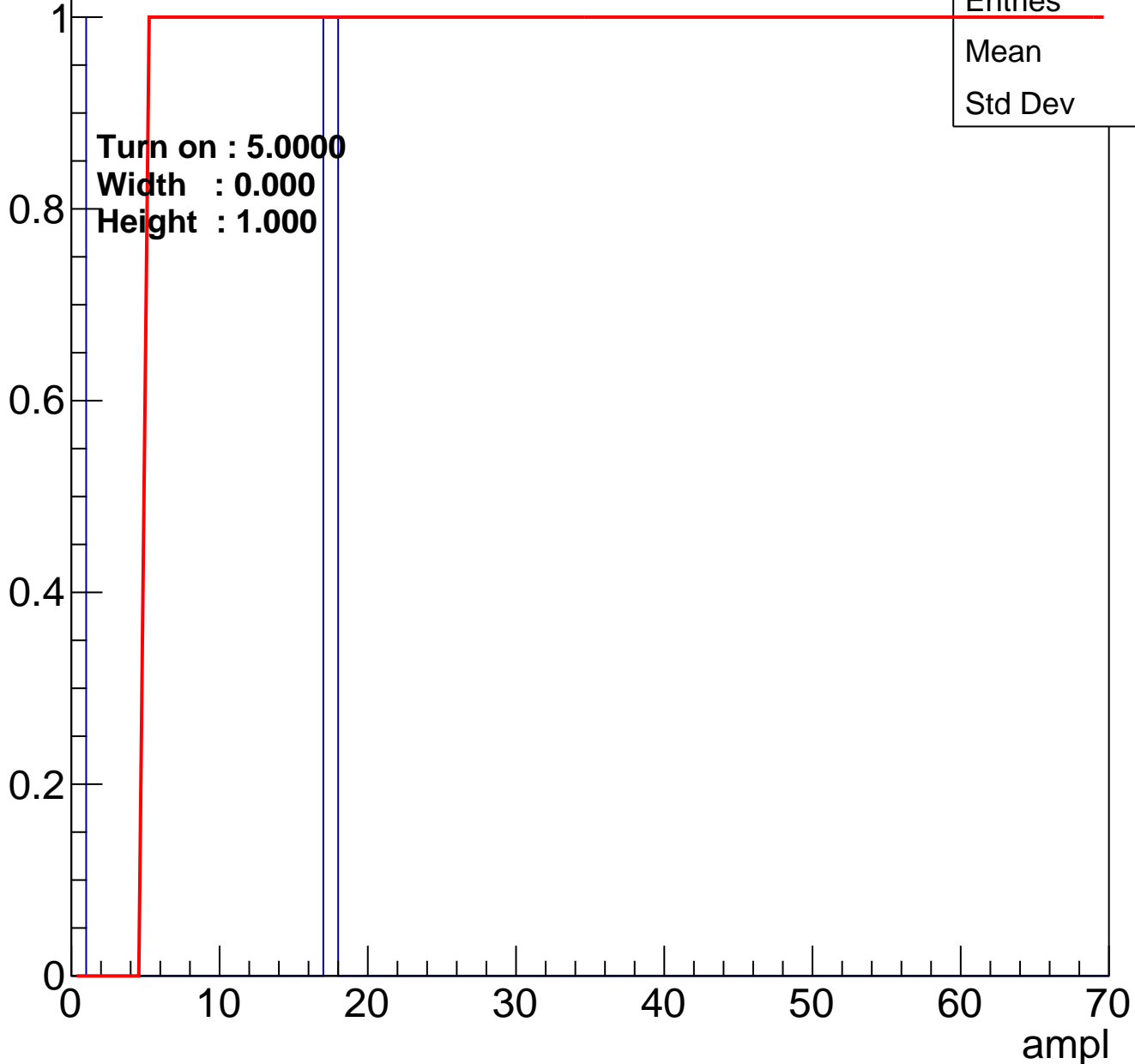
Entries	2
Mean	8.5
Std Dev	8.5

Turn on : 5.0000
Width   : 0.000
Height : 1.000

B0L101S, U10-ch99

calib_packv5_042523_0143.root, FC#1, port C1

Entries	3
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch100

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
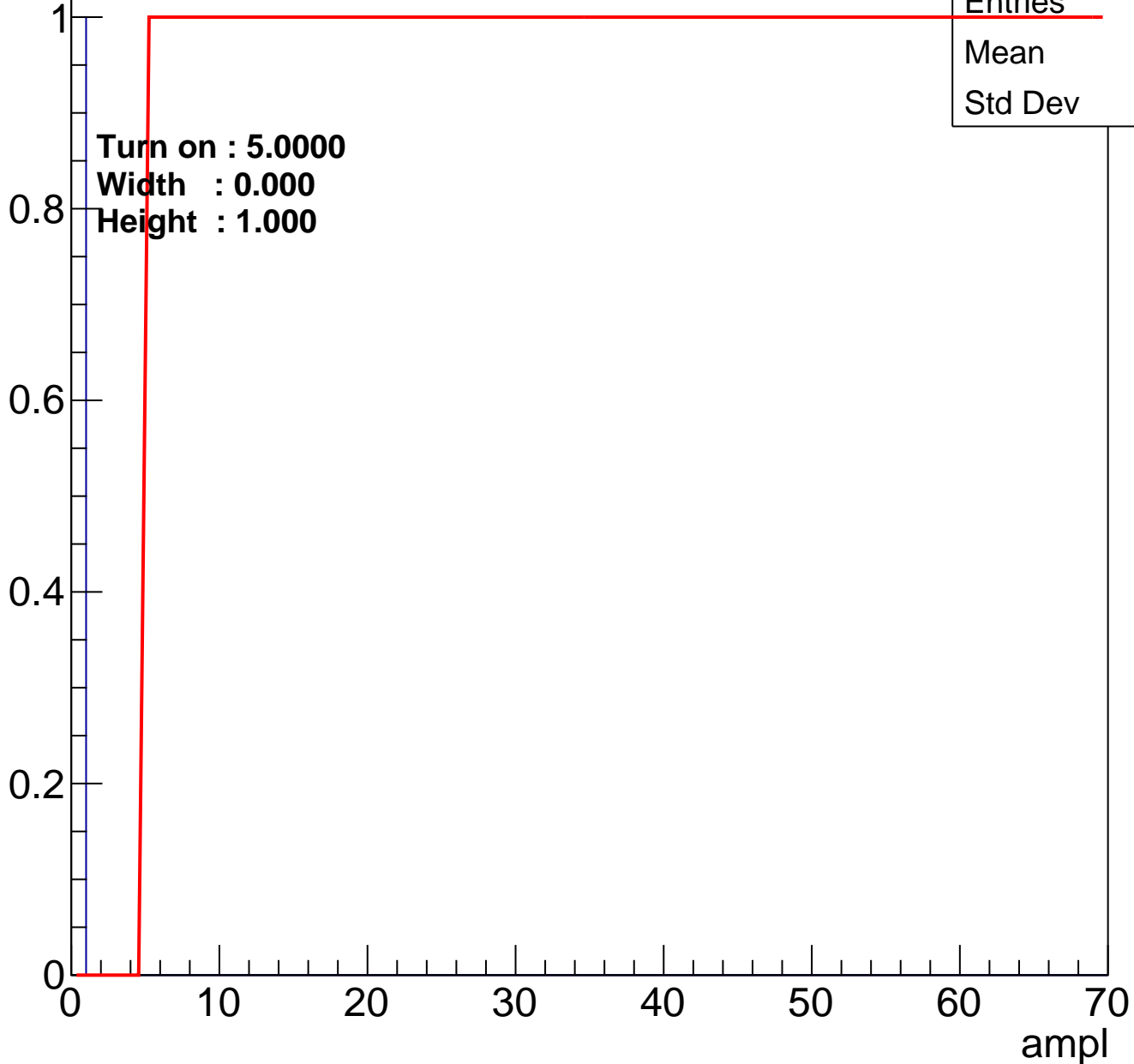
B0L101S, U10-ch101

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch102

Entry

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	4
Mean	18
Std Dev	10.39

ampl

B0L101S, U10-ch103

Entries	0
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
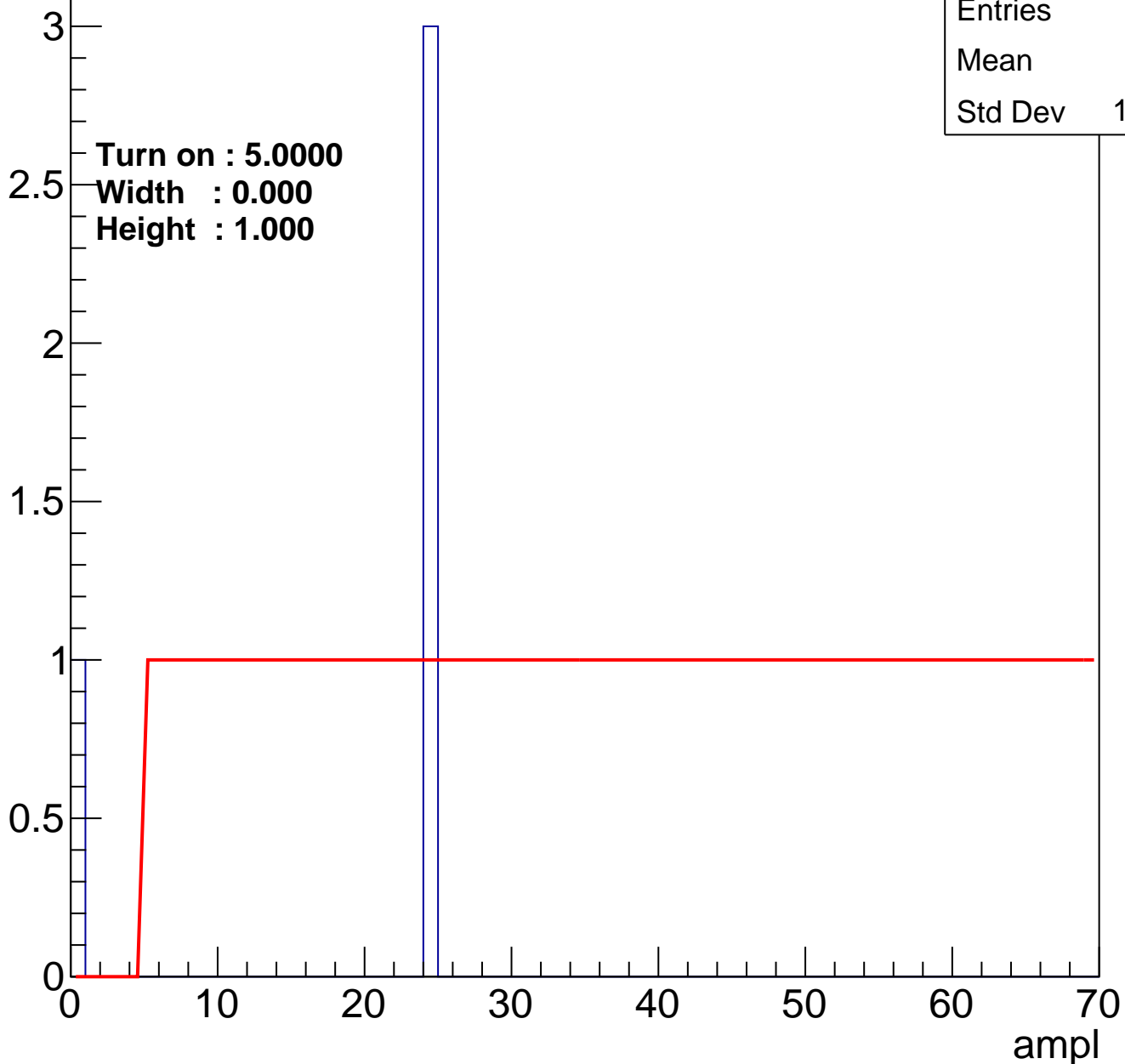
B0L101S, U10-ch104

calib_packv5_042523_0143.root, FC#1, port C1

Entries	0
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
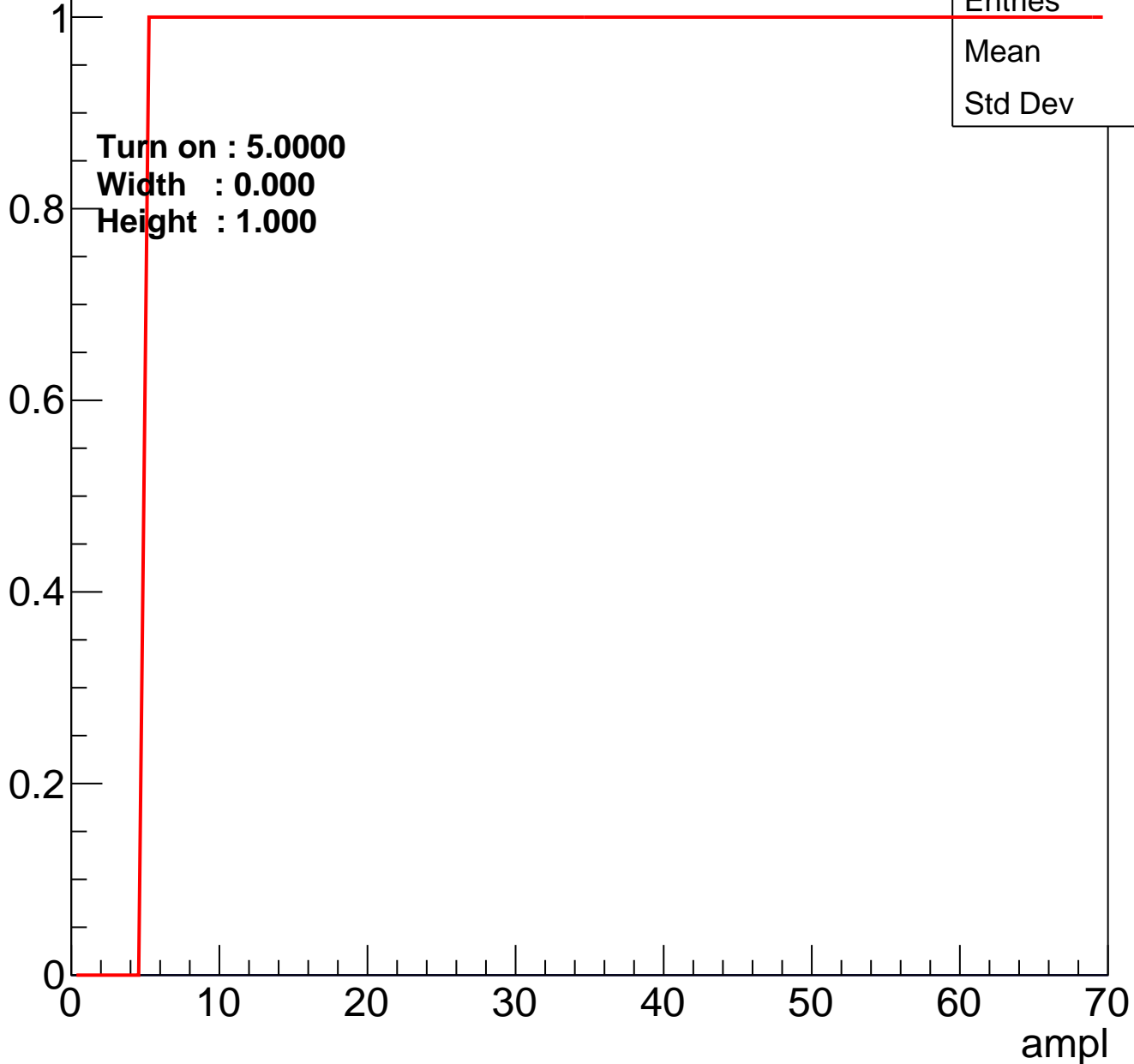
B0L101S, U10-ch105

calib_packv5_042523_0143.root, FC#1, port C1

Entries		2
Mean		0
Std Dev		0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch106

calib_packv5_042523_0143.root, FC#1, port C1

Entries	0
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch107

calib_packv5_042523_0143.root, FC#1, port C1

Entries	0
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch108

calib_packv5_042523_0143.root, FC#1, port C1

Entry

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	2
Mean	0
Std Dev	0

ampl

B0L101S, U10-ch109

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch110

calib_packv5_042523_0143.root, FC#1, port C1

Entry

Entries	3
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl
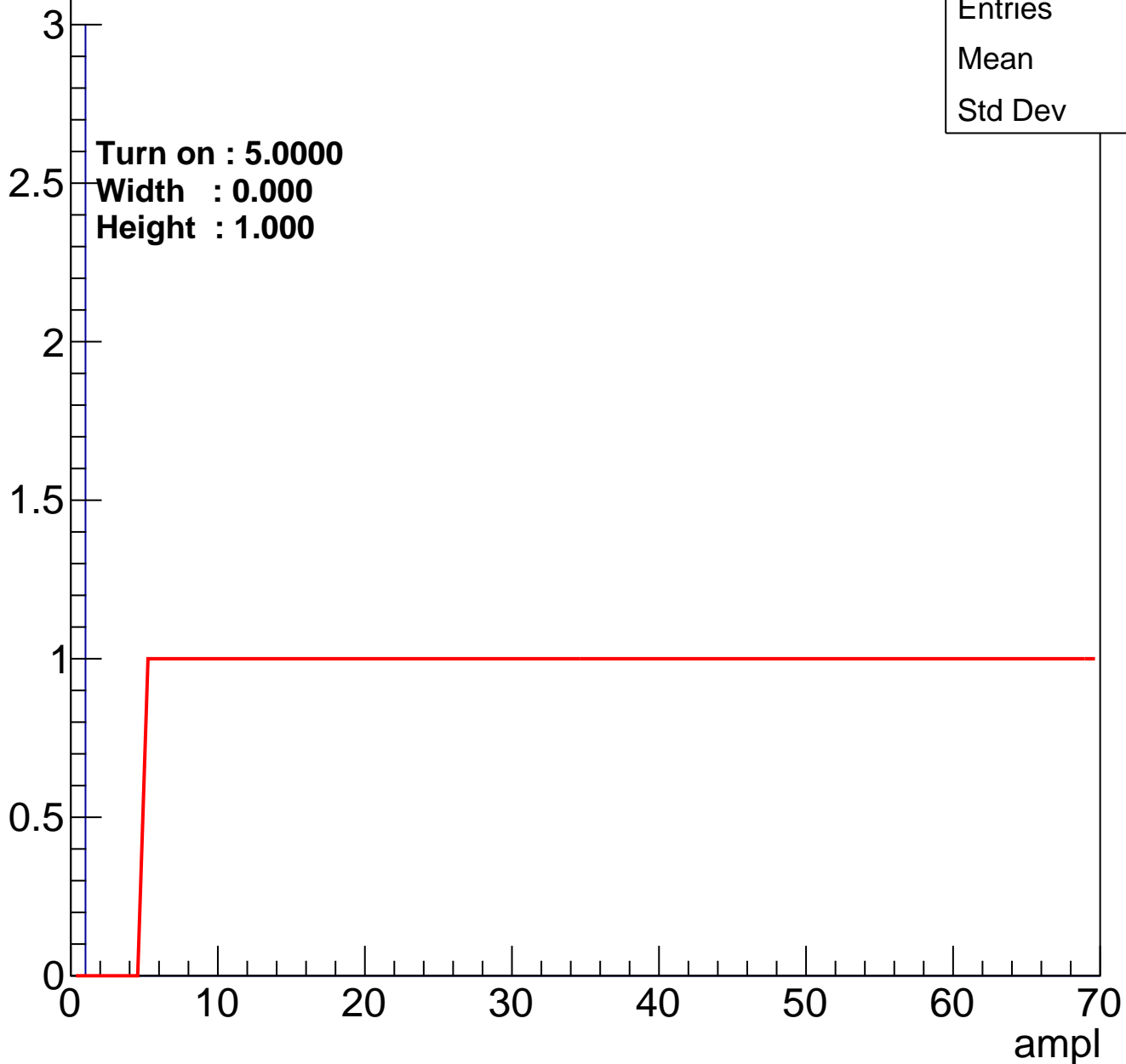
B0L101S, U10-ch111

calib_packv5_042523_0143.root, FC#1, port C1

Entries	3
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
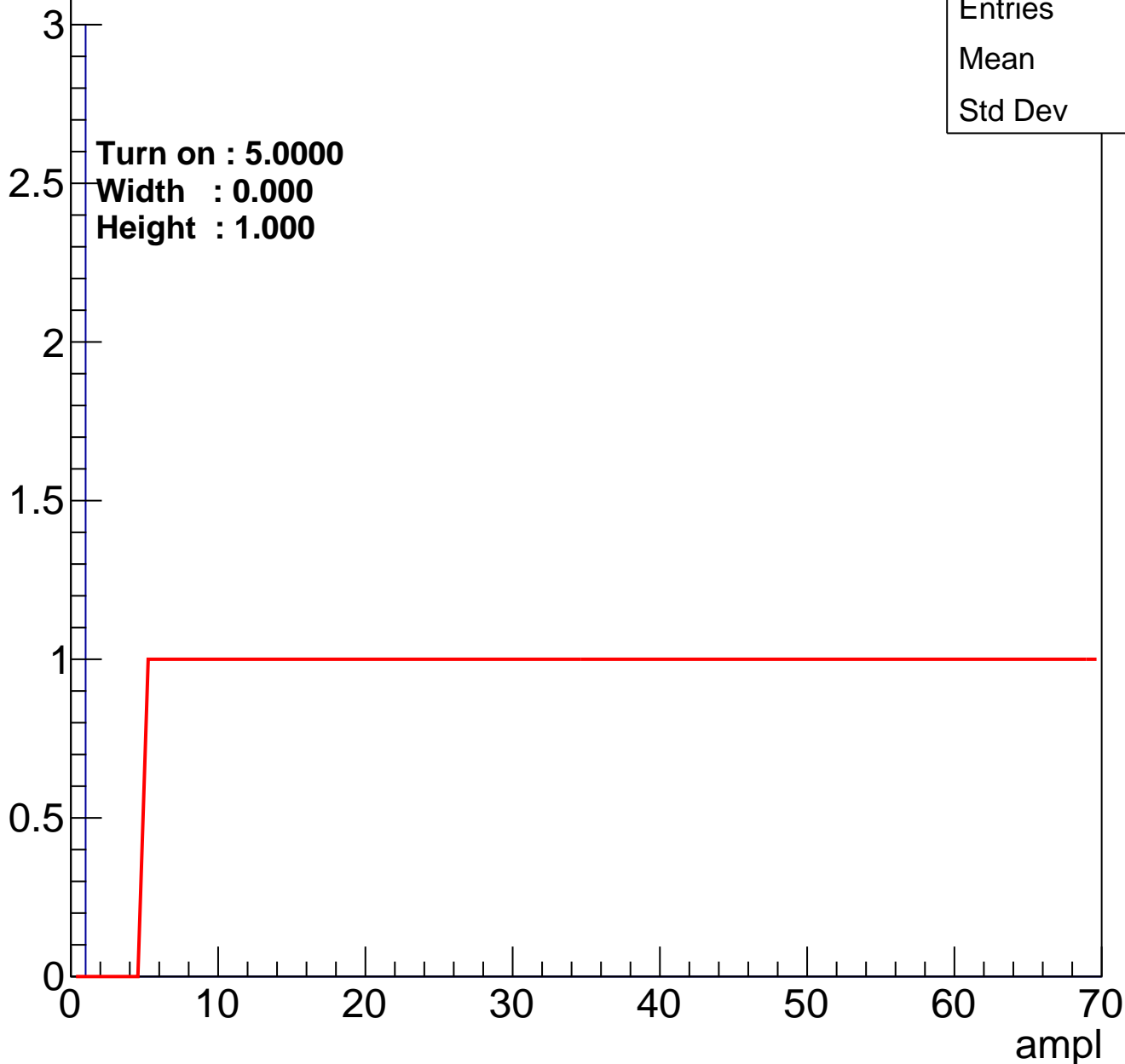
B0L101S, U10-ch112

calib_packv5_042523_0143.root, FC#1, port C1

Entries	7
Mean	14.29
Std Dev	18.12

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
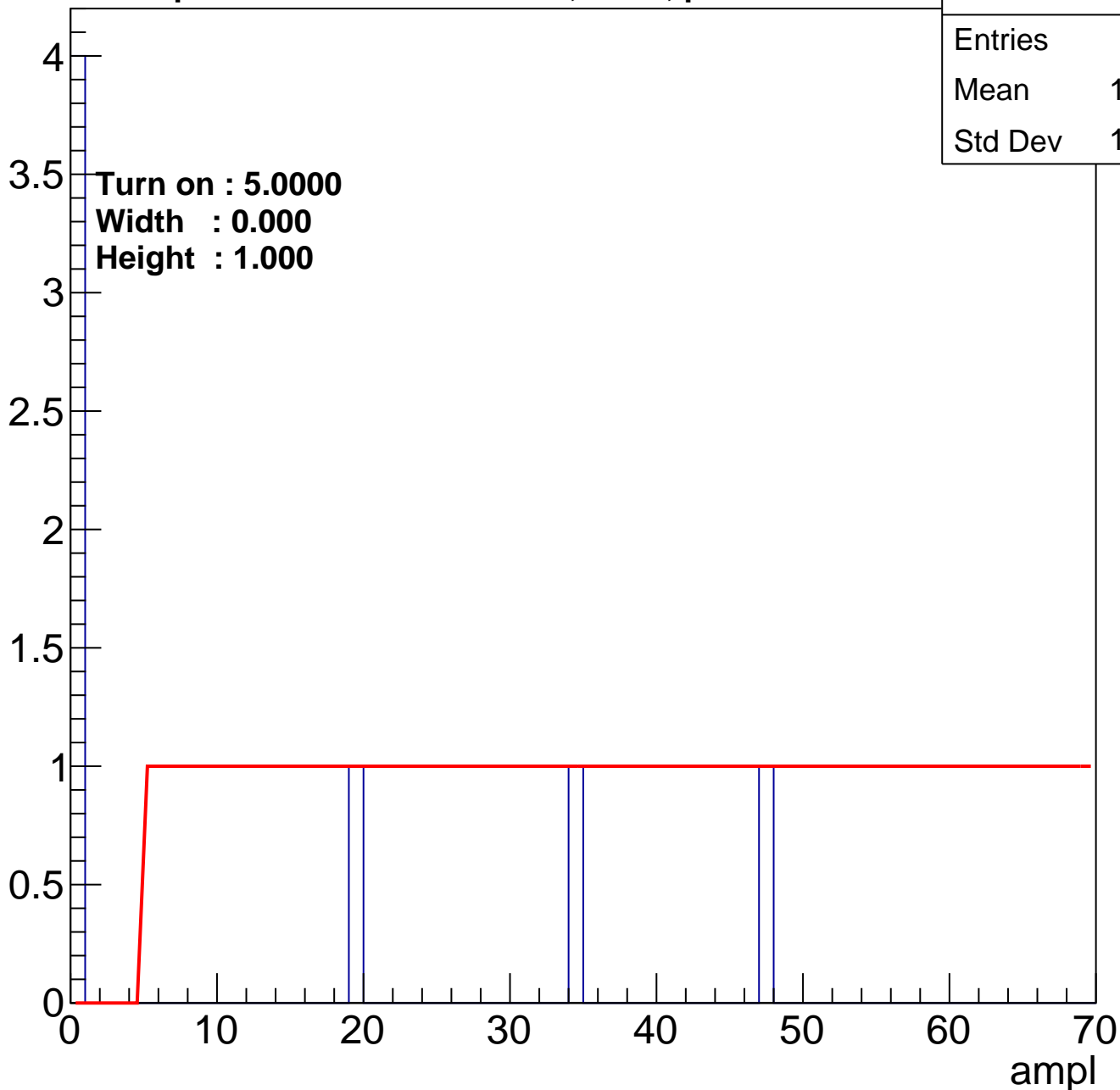
B0L101S, U10-ch113

calib_packv5_042523_0143.root, FC#1, port C1

Entry

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	3
Mean	0
Std Dev	0

ampl

B0L101S, U10-ch114

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	1.5
Std Dev	1.5

Turn on : 5.0000
Width   : 0.000
Height : 1.000
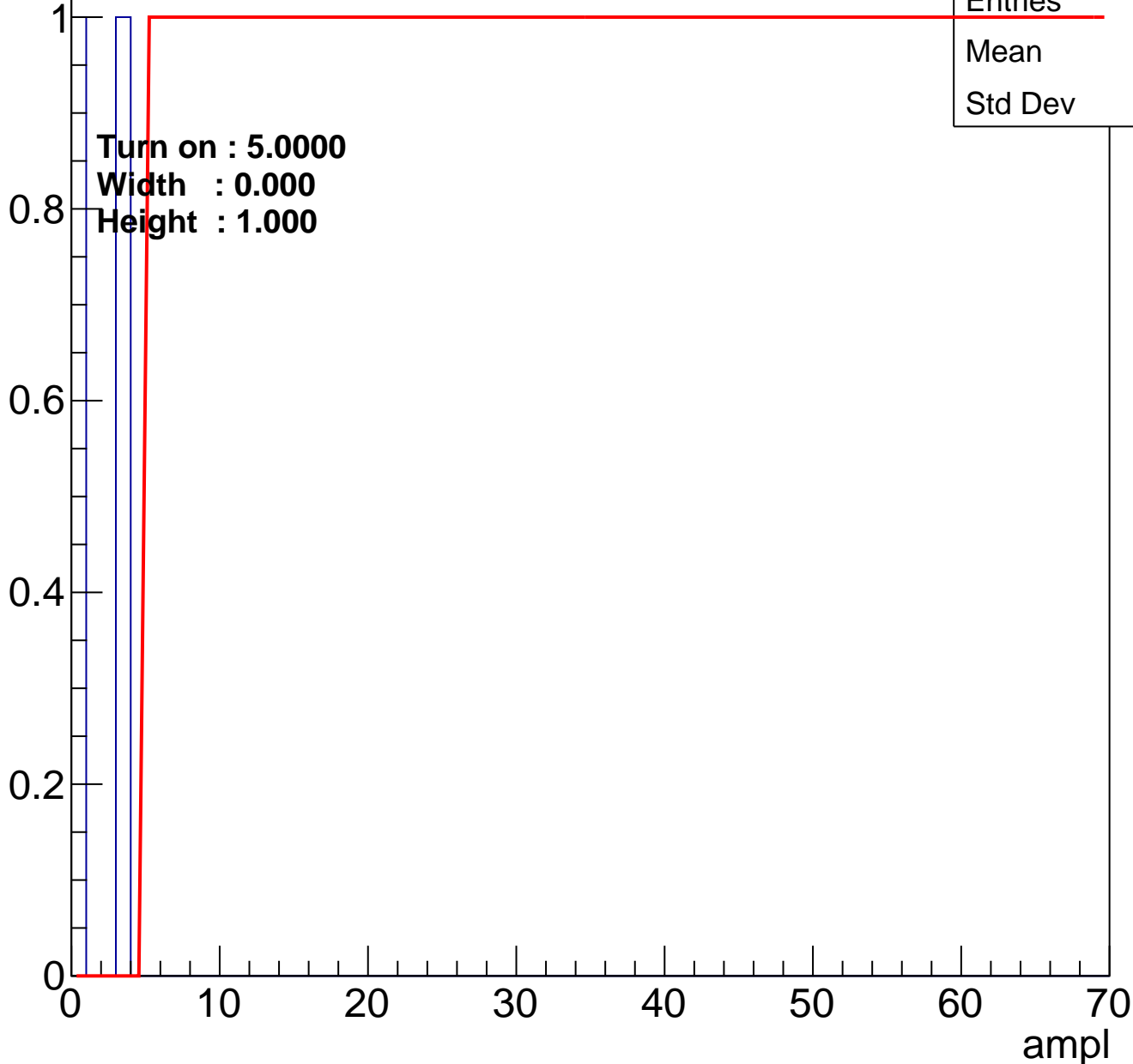
Entry

ampl

B0L101S, U10-ch115

calib_packv5_042523_0143.root, FC#1, port C1

Entries	3
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000
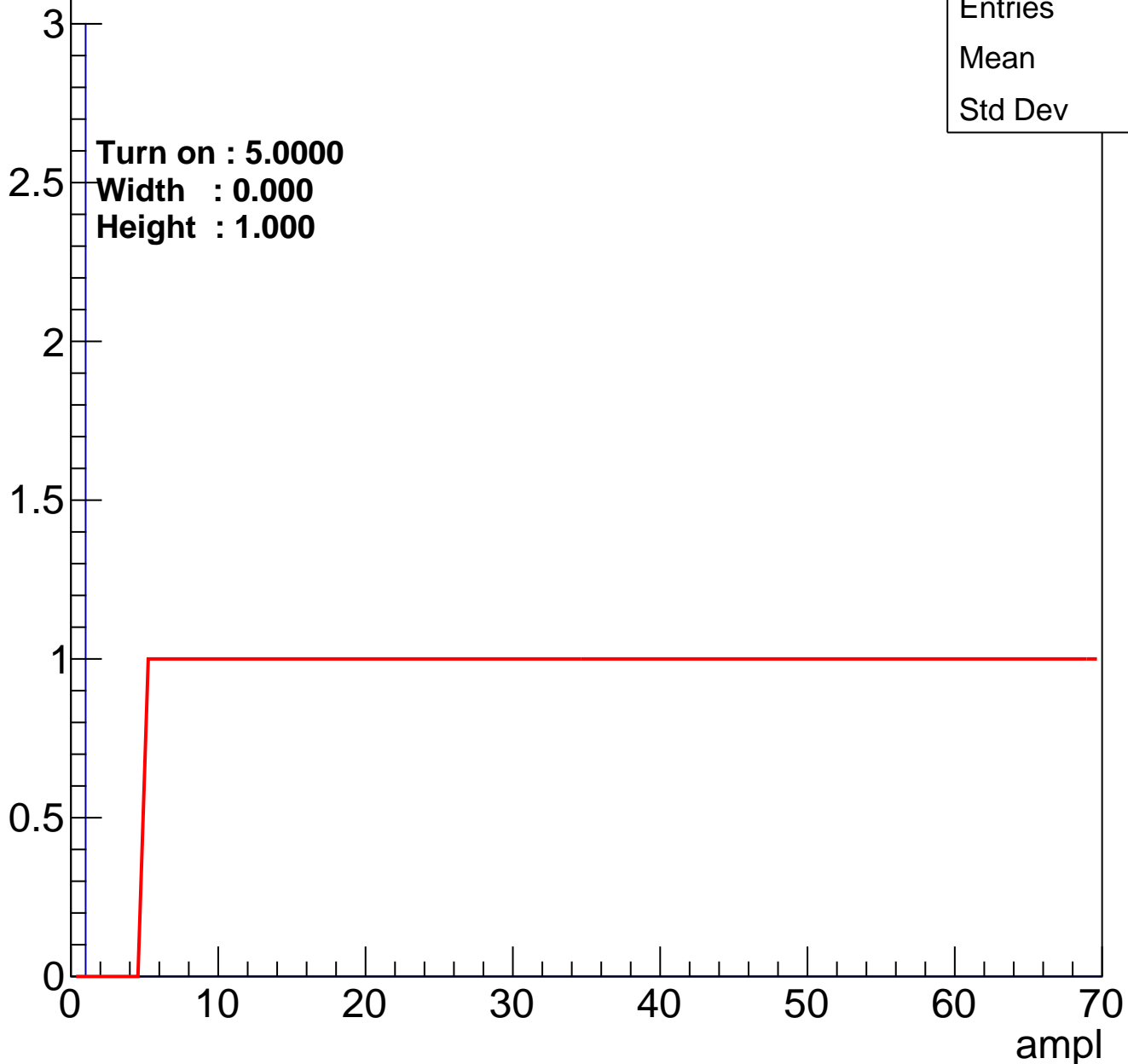
Entry

ampl

B0L101S, U10-ch116

calib_packv5_042523_0143.root, FC#1, port C1

Entries	3
Mean	21.33
Std Dev	16.82

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch117

calib_packv5_042523_0143.root, FC#1, port C1

Entries	3
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch118

Entry

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

ampl

B0L101S, U10-ch119

calib_packv5_042523_0143.root, FC#1, port C1

Entries	1
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
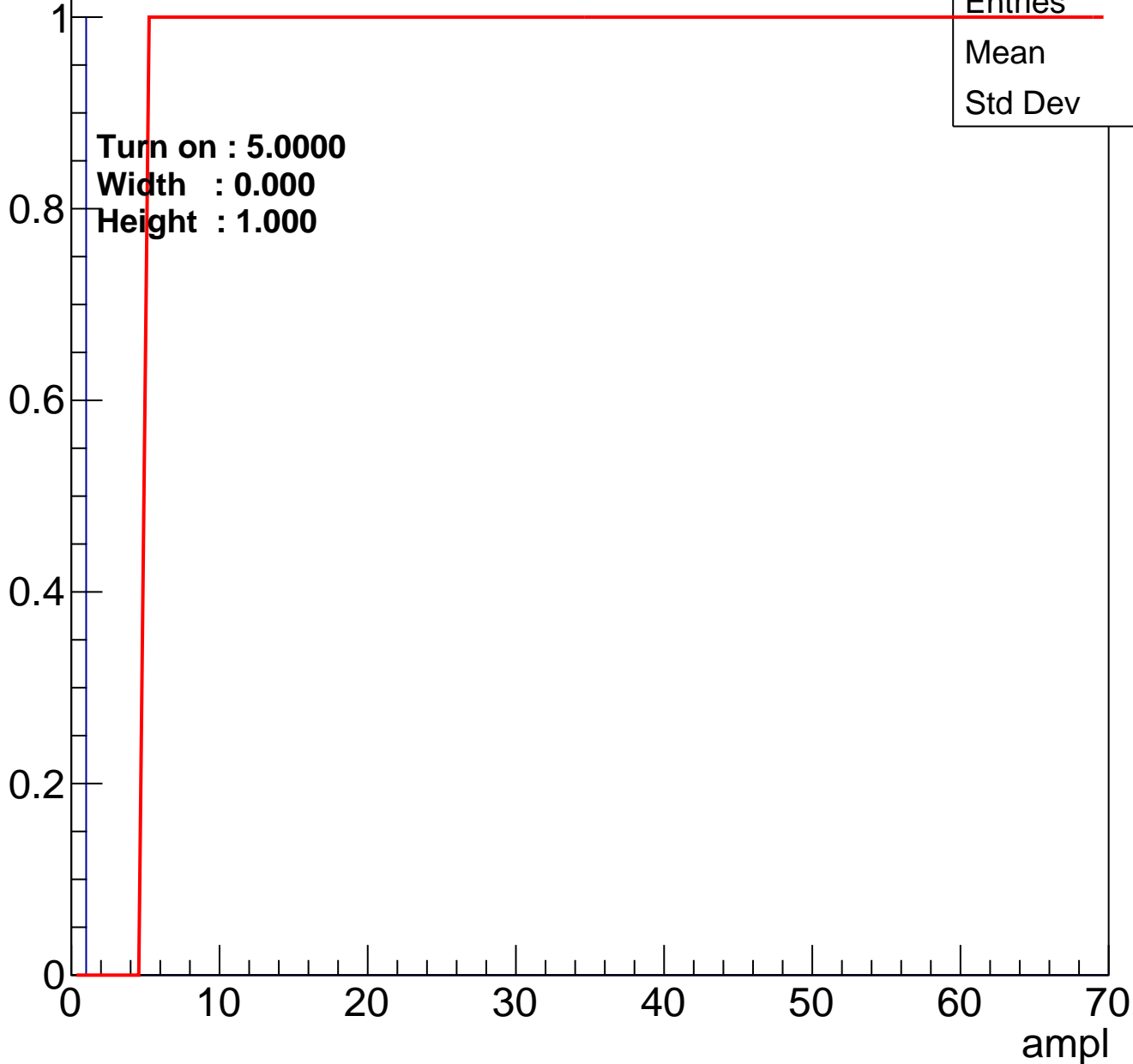
B0L101S, U10-ch120

calib_packv5_042523_0143.root, FC#1, port C1

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	1
Mean	5
Std Dev	0

Entry

ampl
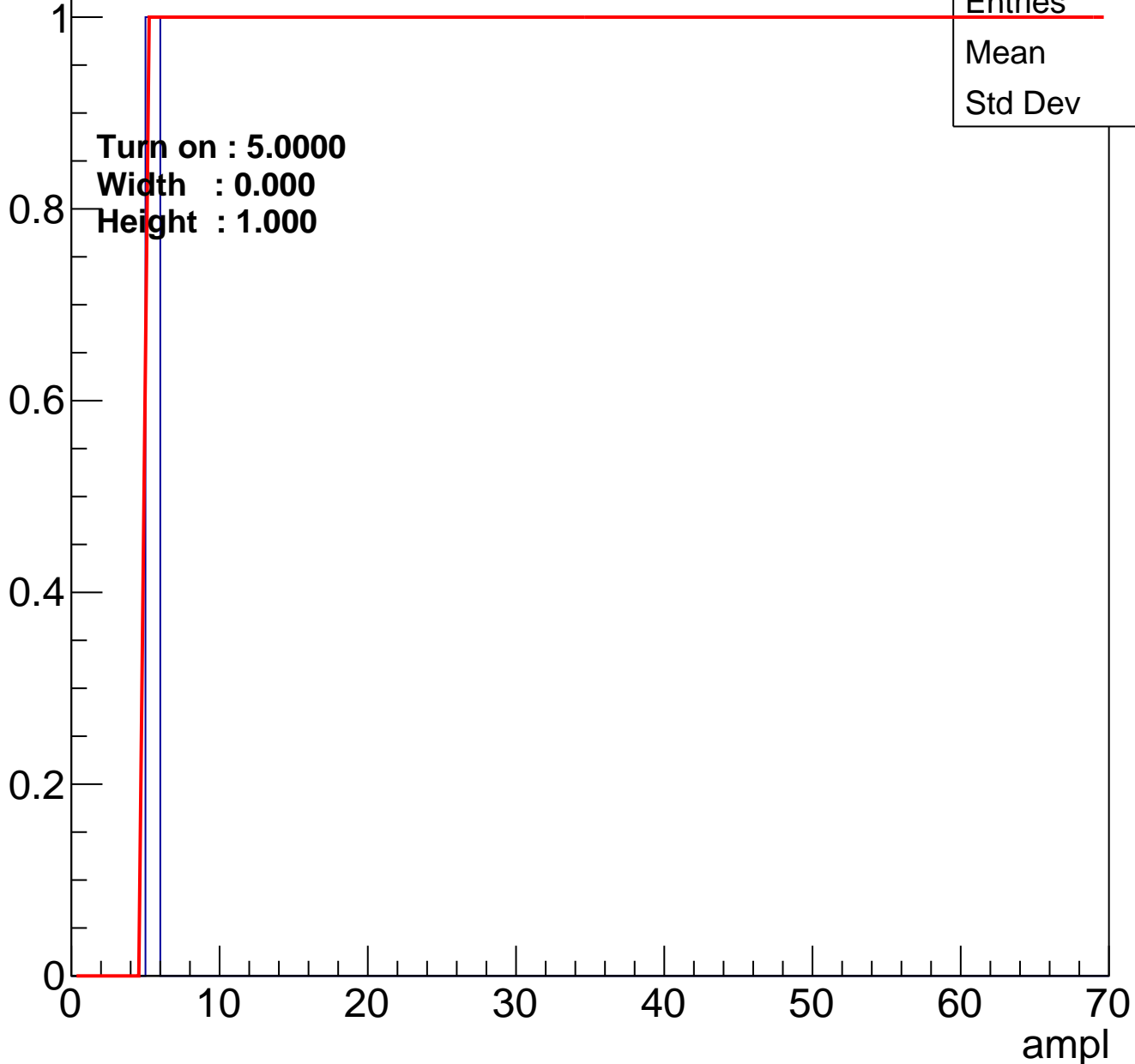
B0L101S, U10-ch121

calib_packv5_042523_0143.root, FC#1, port C1

Entry

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	4
Mean	0
Std Dev	0

ampl
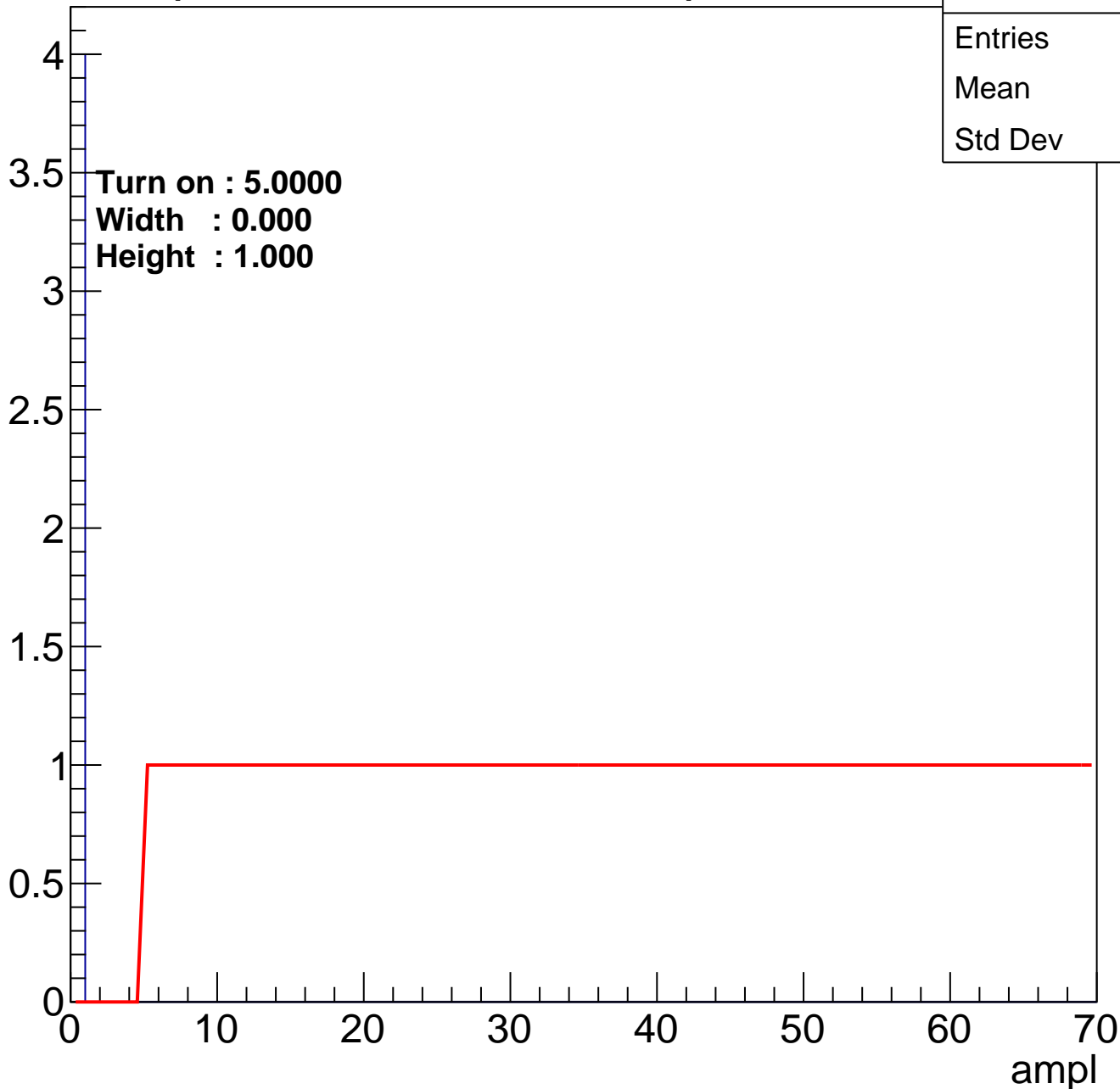
B0L101S, U10-ch122

calib_packv5_042523_0143.root, FC#1, port C1

Turn on : 5.0000
Width   : 0.000
Height : 1.000
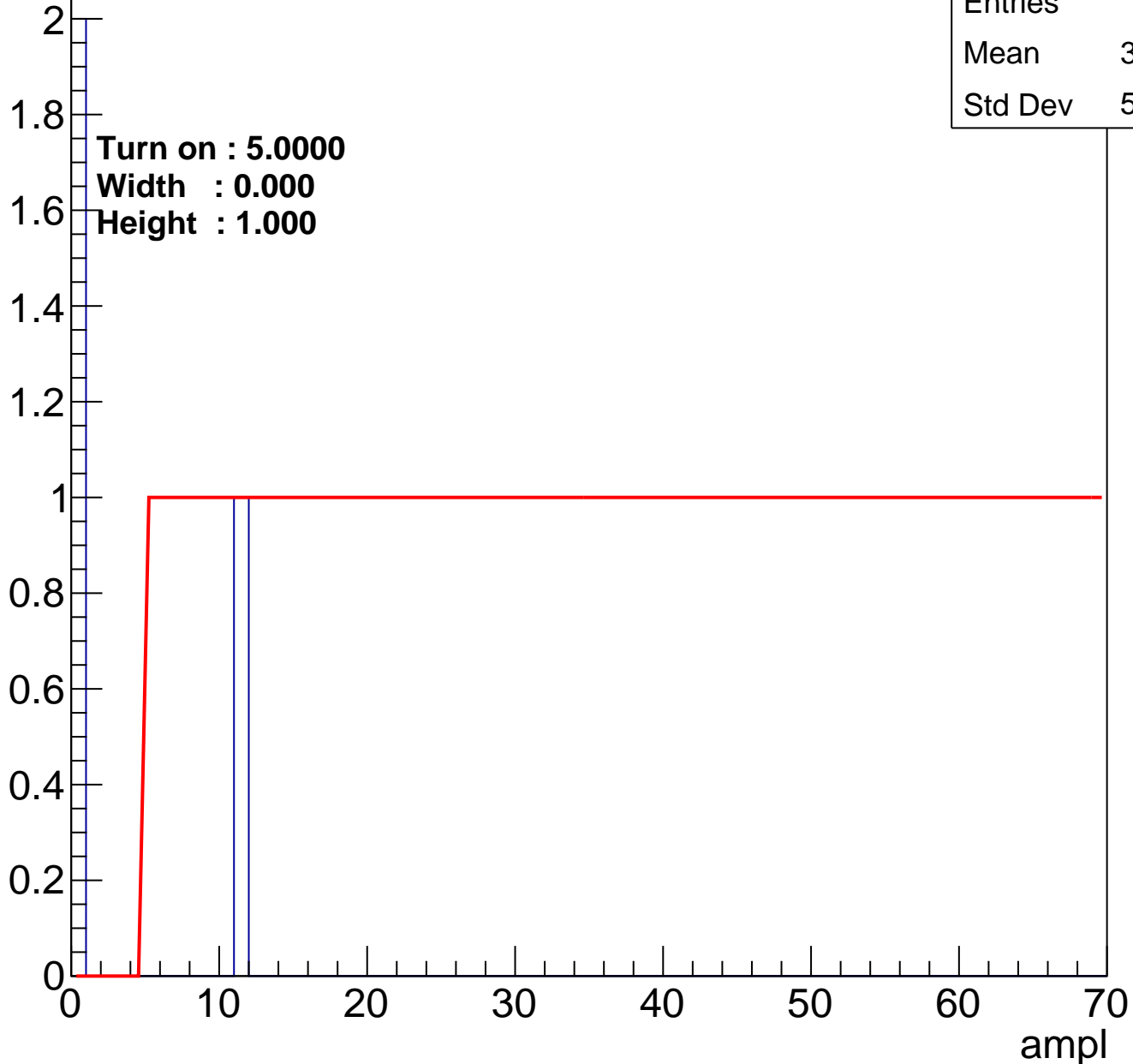
Entries	3
Mean	3.667
Std Dev	5.185

Entry

ampl

B0L101S, U10-ch123

calib_packv5_042523_0143.root, FC#1, port C1

Entries	2
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl

B0L101S, U10-ch124

calib_packv5_042523_0143.root, FC#1, port C1

Entries	8
Mean	3.125
Std Dev	5.418

Turn on : 5.0000
Width : 0.000
Height : 1.000
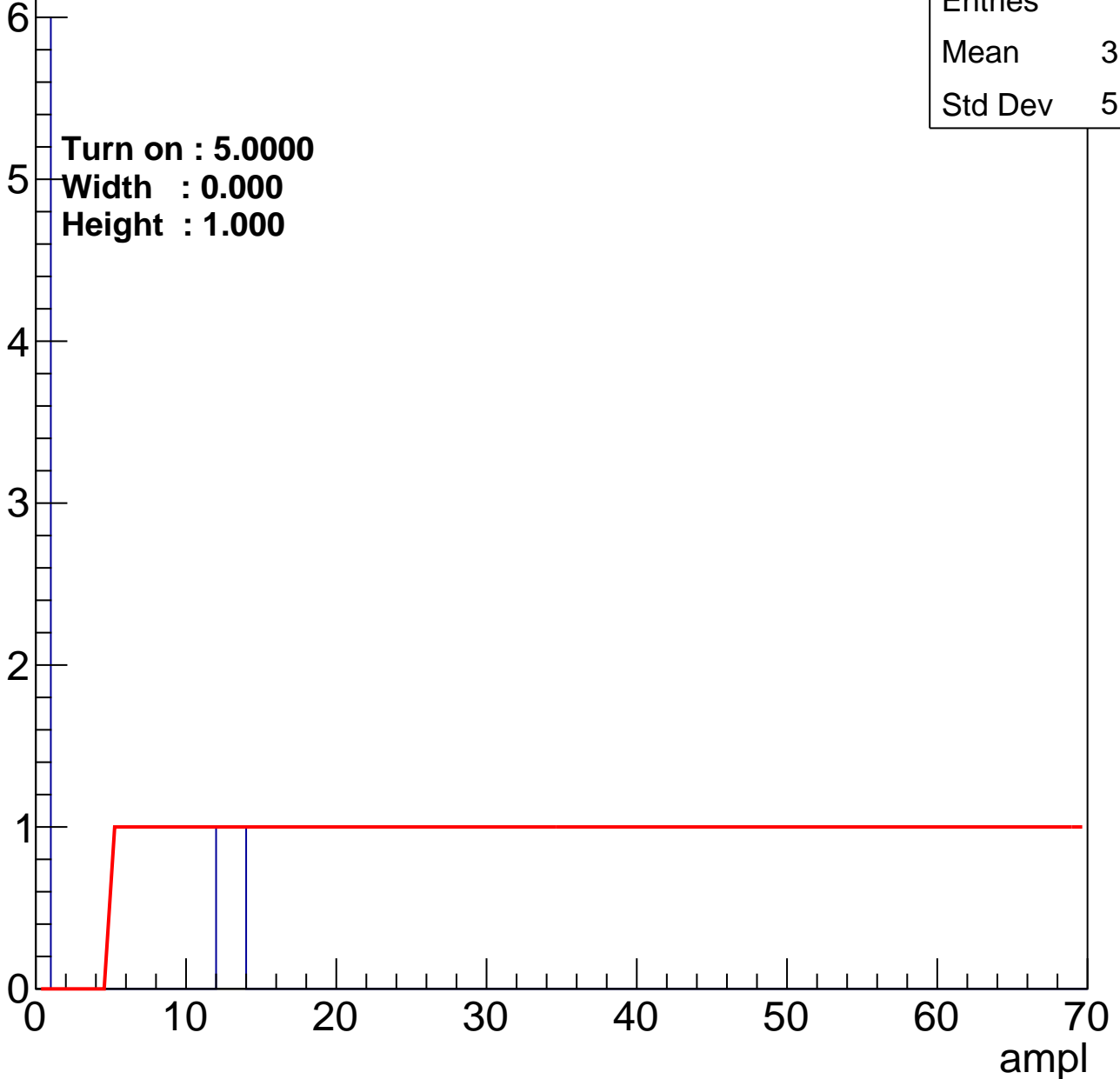
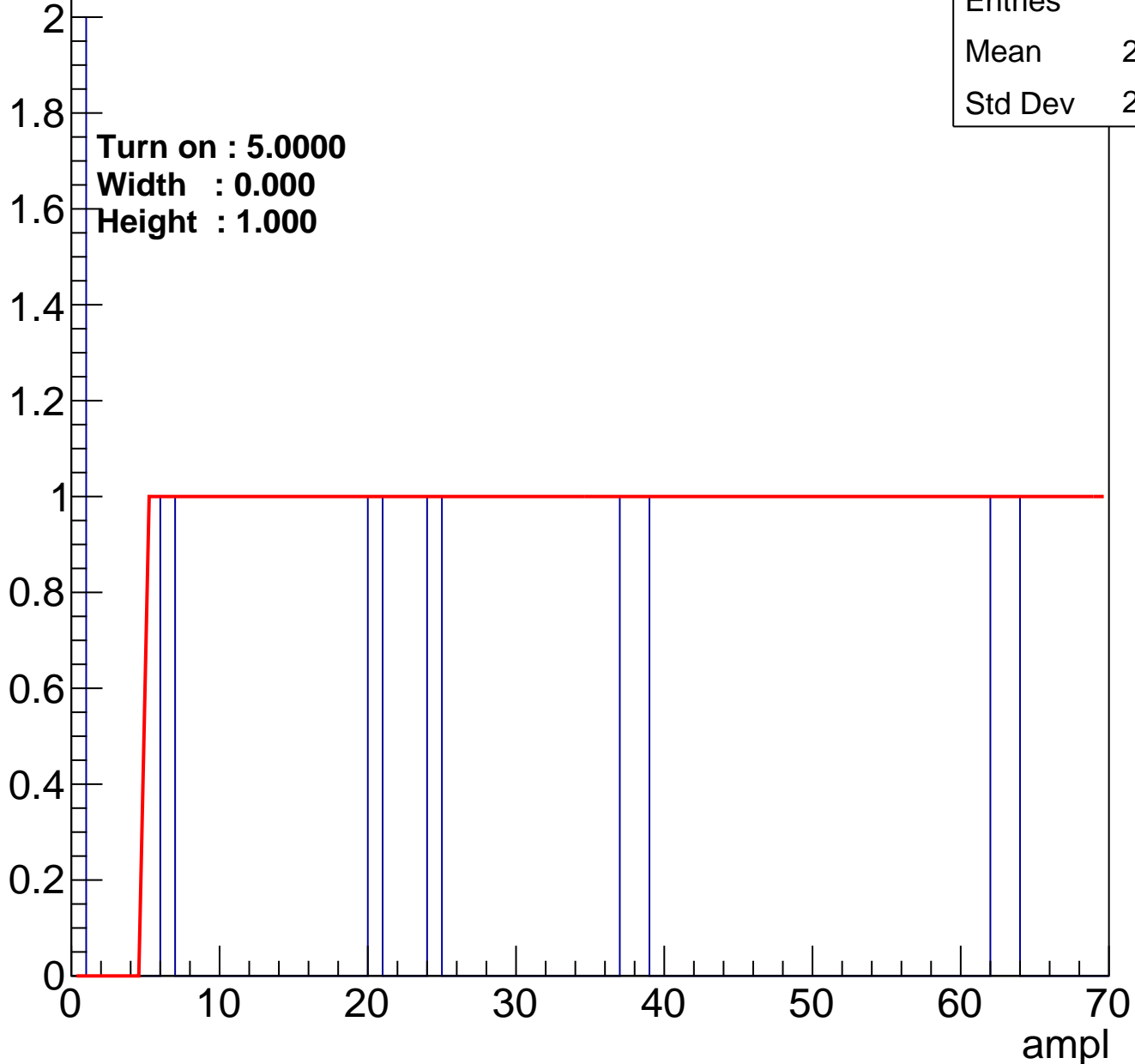# B0L101S, U10-ch125

calib_packv5_042523_0143.root, FC#1, port C1

Entries	3
Mean	0
Std Dev	0

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entry

ampl
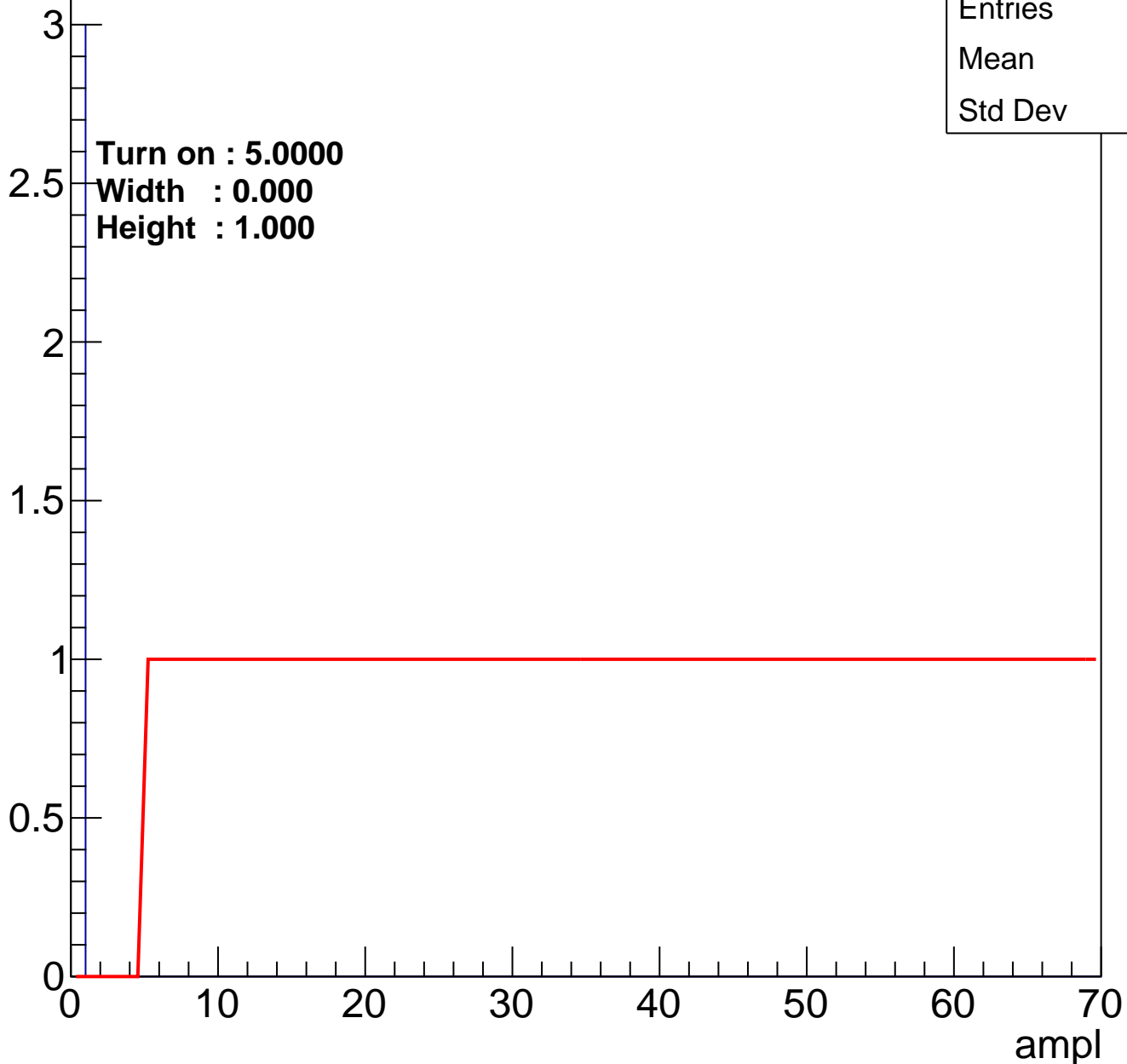
B0L101S, U10-ch126

calib_packv5_042523_0143.root, FC#1, port C1

Entries	9
Mean	27.78
Std Dev	22.84

Turn on : 5.0000
Width   : 0.000
Height : 1.000

B0L101S, U10-ch127

calib_packv5_042523_0143.root, FC#1, port C1

Entries	9
Mean	35
Std Dev	17.38

Turn on : 5.0000
Width   : 0.000
Height : 1.000

B0L101S, U10-ch127

calib_packv5_042523_0143.root, FC#1, port C1

Entry

Turn on : 5.0000
Width   : 0.000
Height : 1.000

Entries	9
Mean	35
Std Dev	17.38

ampl