

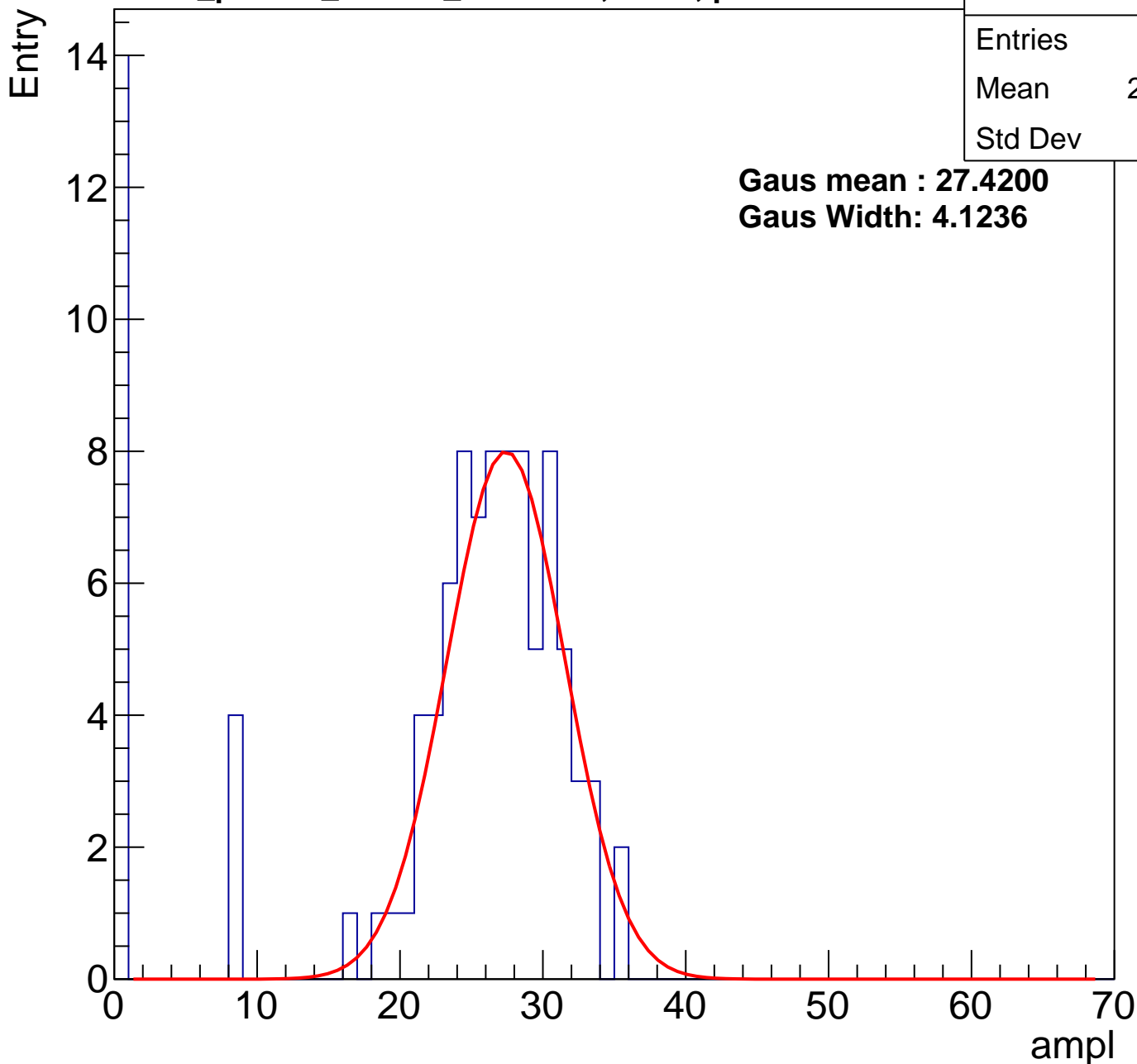
B1L103S, U7-ch0, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	101
Mean	22.13
Std Dev	10.2

Gaus mean : 27.4200

Gaus Width: 4.1236



B1L103S, U7-ch0, adc1

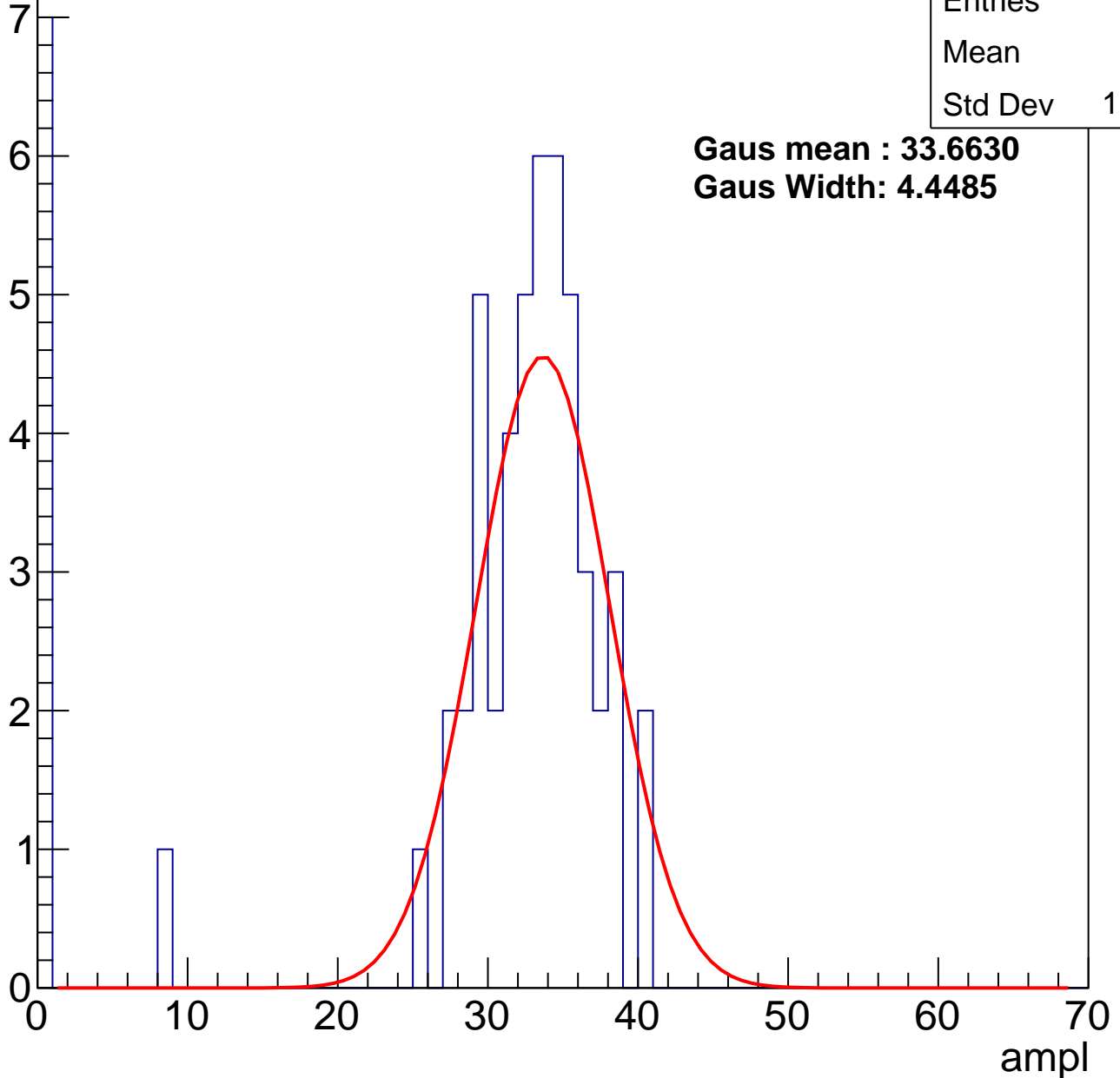
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	28.3
Std Dev	11.63

Gaus mean : 33.6630

Gaus Width: 4.4485



B1L103S, U7-ch0, adc2

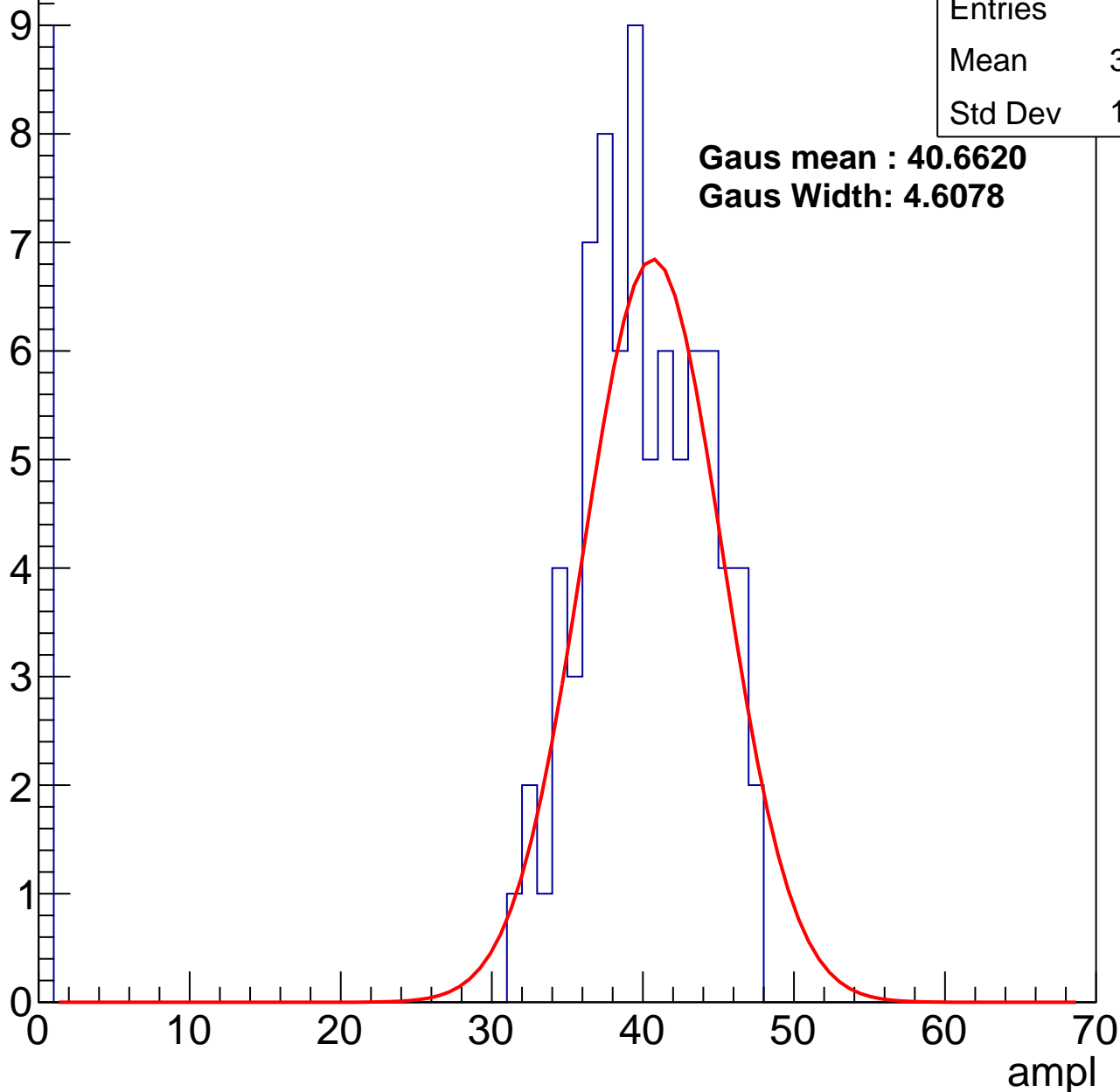
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	88
Mean	35.59
Std Dev	12.57

Gaus mean : 40.6620

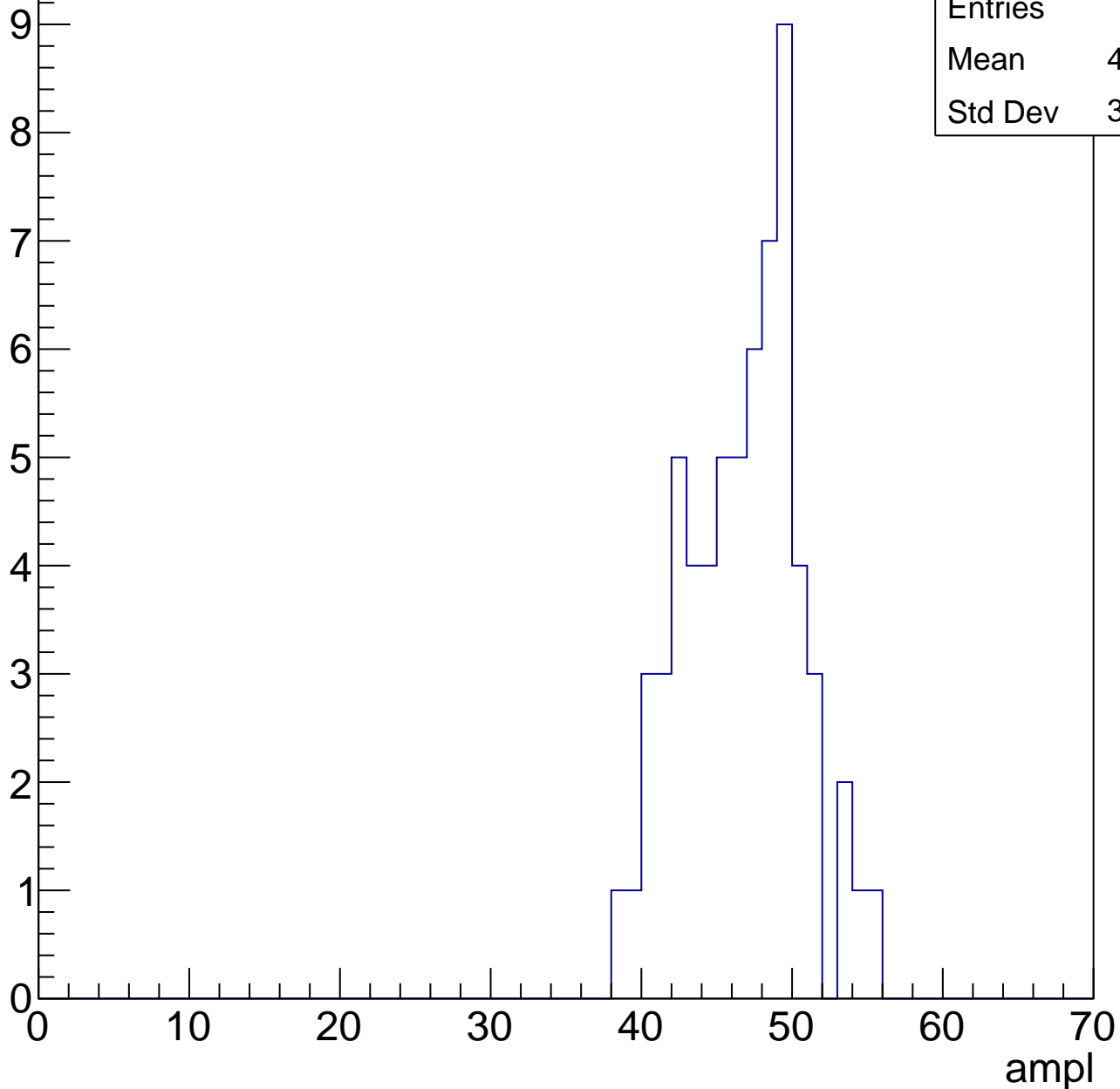
Gaus Width: 4.6078



B1L103S, U7-ch0, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry



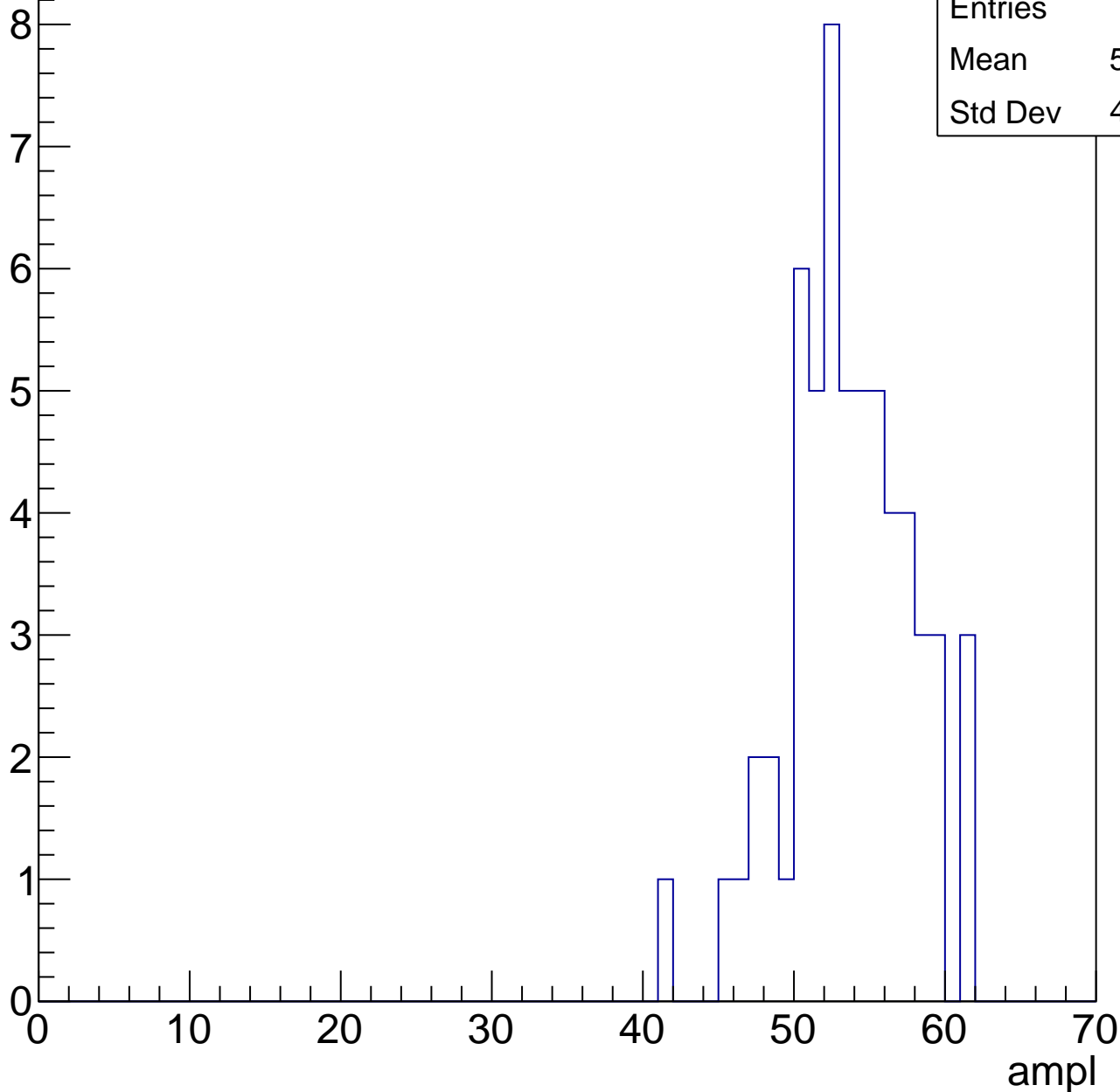
Entries	64
Mean	46.25
Std Dev	3.804

B1L103S, U7-ch0, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	53.19
Std Dev	4.065

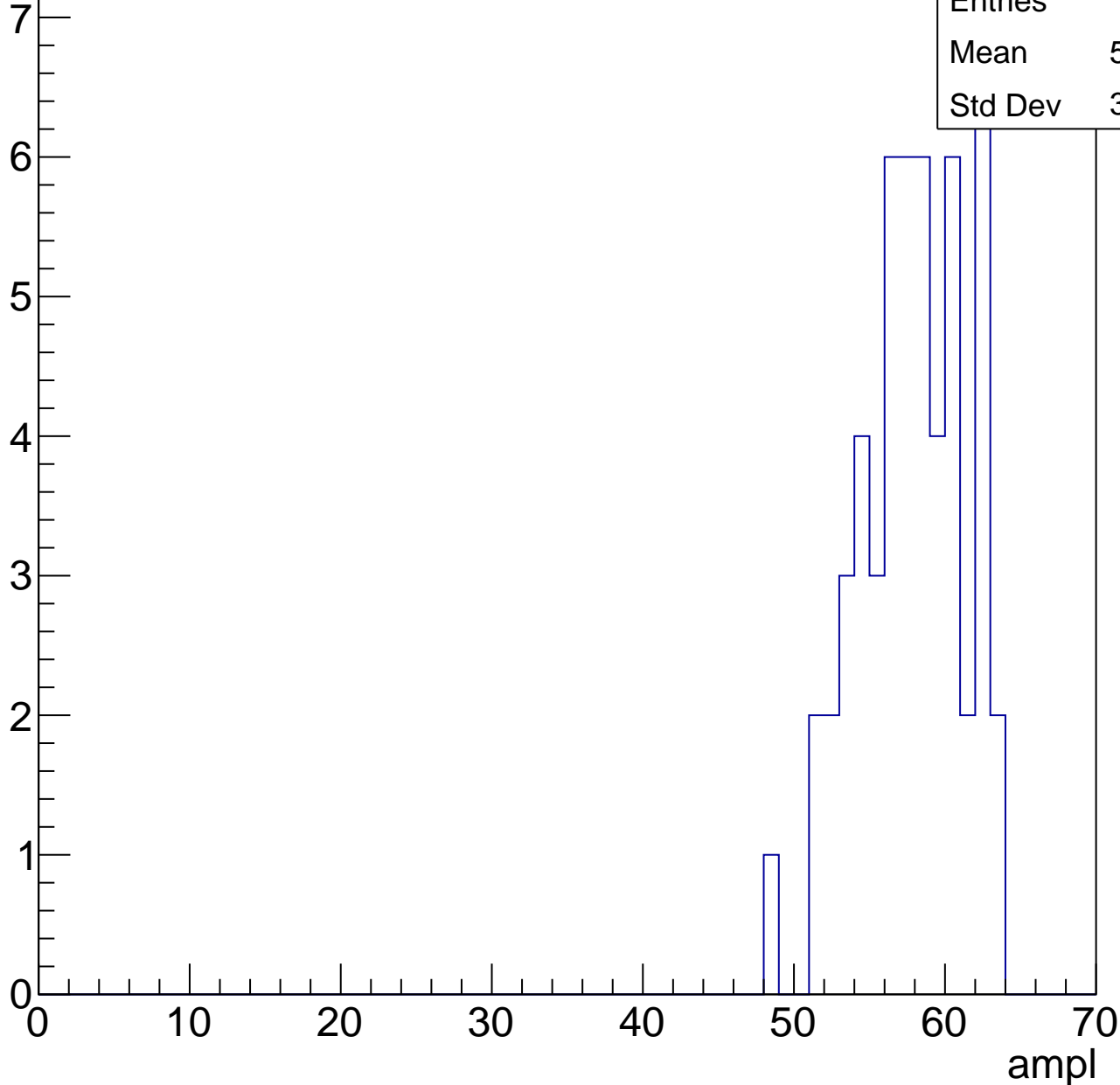


B1L103S, U7-ch0, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	57.37
Std Dev	3.476

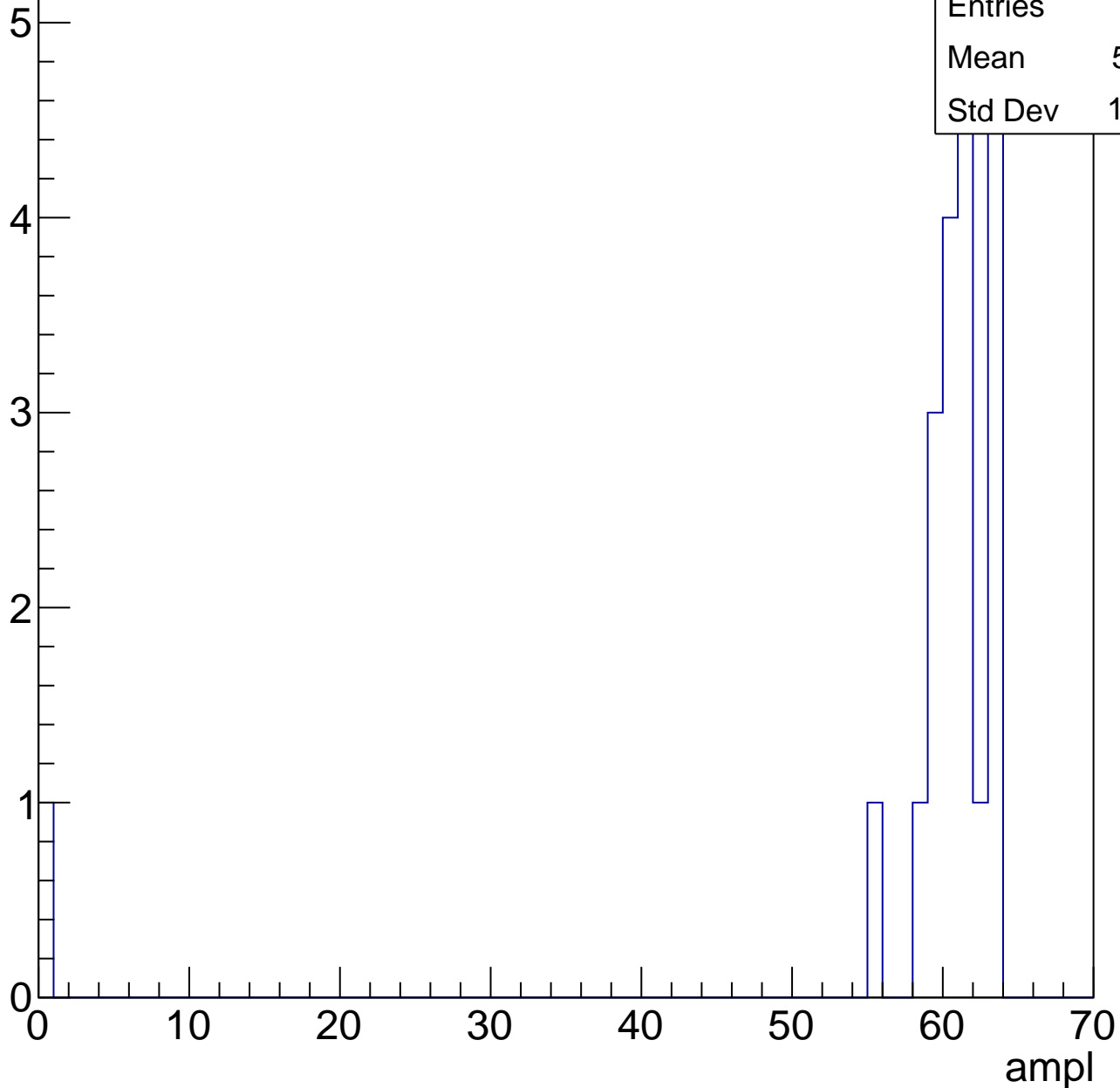


B1L103S, U7-ch0, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

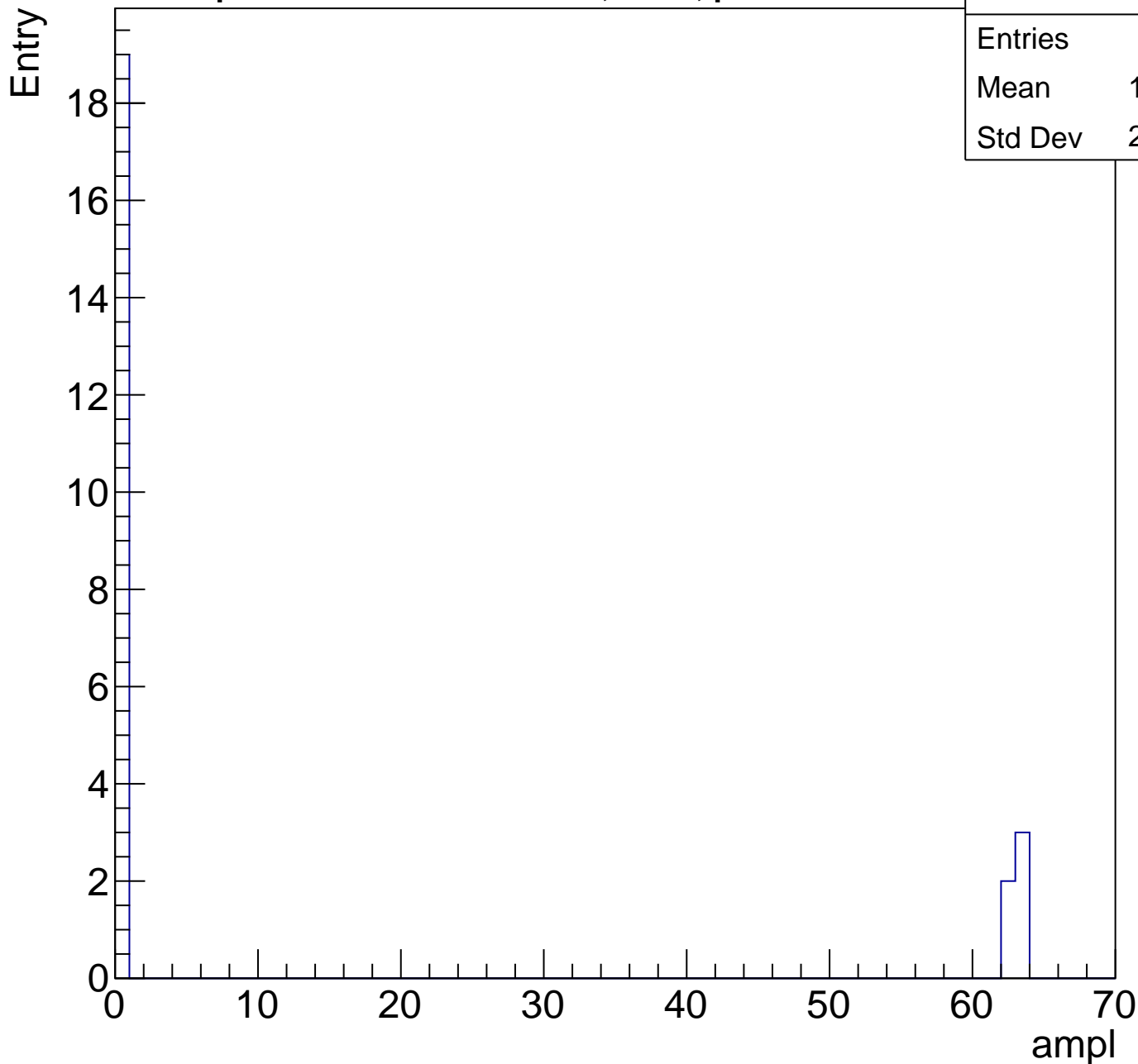
Entries	21
Mean	57.71
Std Dev	13.05



B1L103S, U7-ch0, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	24
Mean	13.04
Std Dev	25.42



B1L103S, U7-ch1, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	69
Mean	24.7
Std Dev	11.03

Gaus mean : 29.7139

Gaus Width: 2.8402

Entry

10

8

6

4

2

0

0

10

20

30

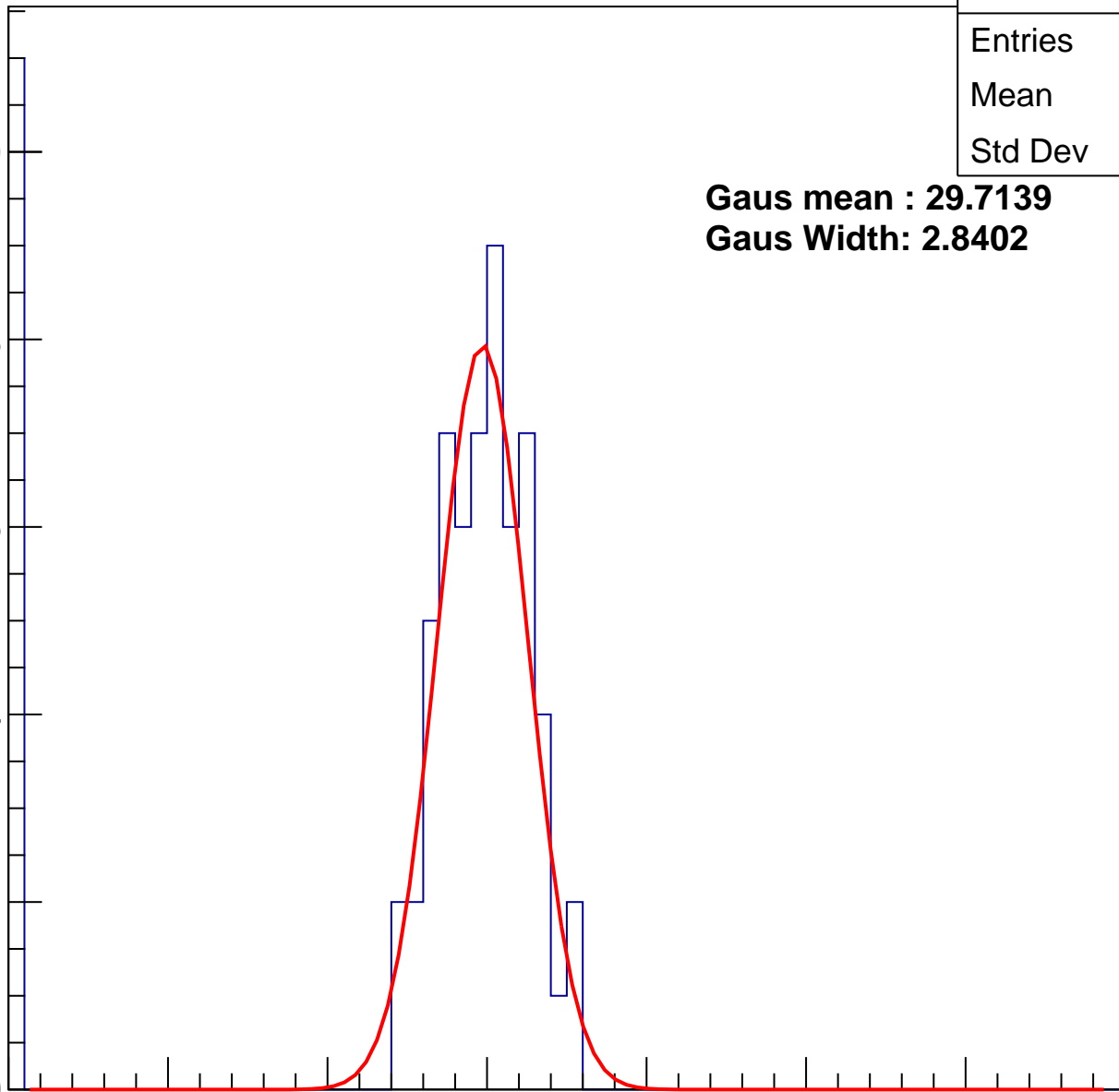
40

50

60

70

ampl



B1L103S, U7-ch1, adc1

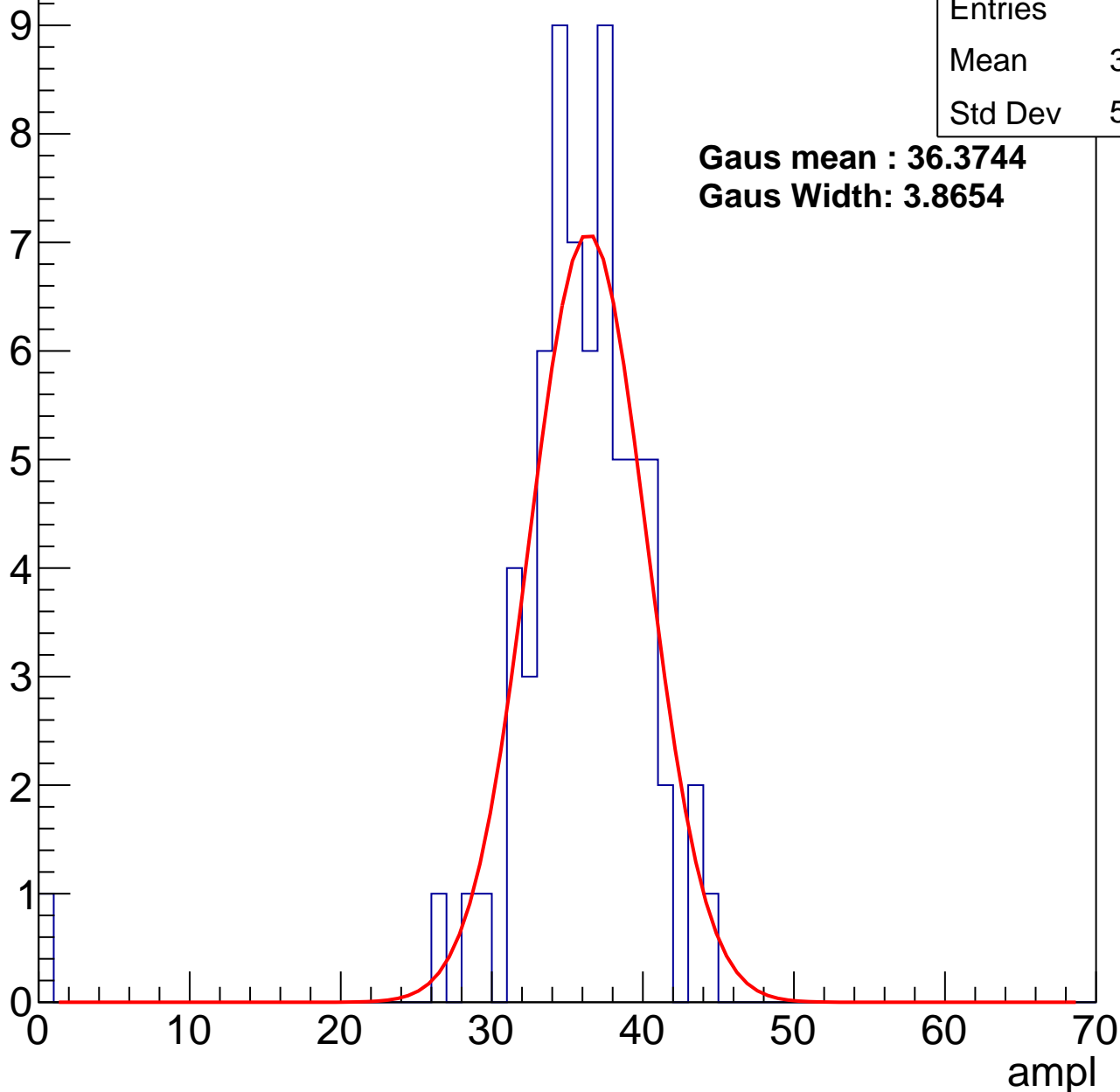
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	35.26
Std Dev	5.535

Gaus mean : 36.3744

Gaus Width: 3.8654



B1L103S, U7-ch1, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	97
Mean	38.9
Std Dev	13.76

Gaus mean : 44.0937

Gaus Width: 4.2144

Entry

10

8

6

4

2

0

0

10

20

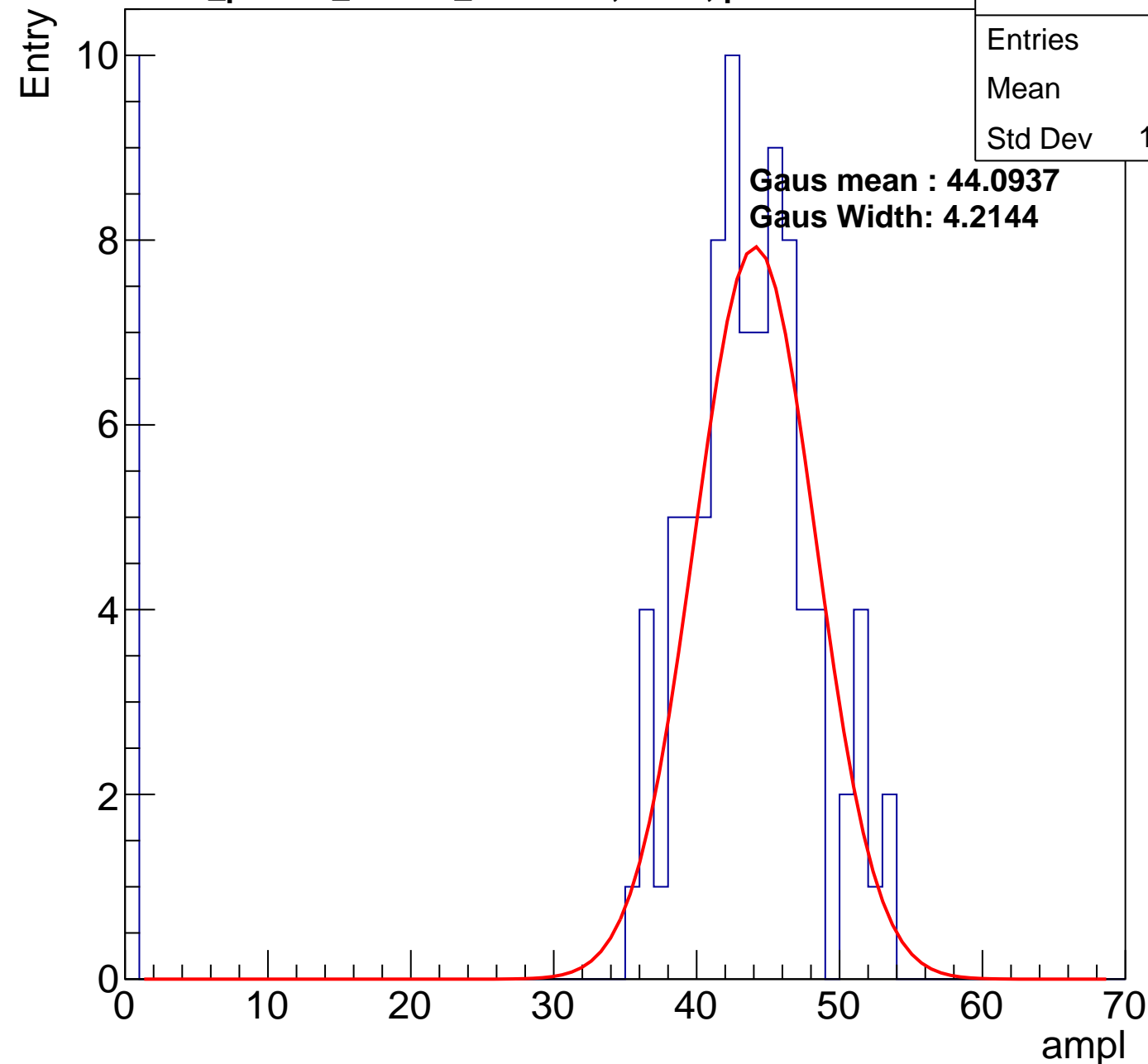
30

40

50

60

ampl



B1L103S, U7-ch1, adc3

calib_packv5_041523_1651.root, FC#0, port C2

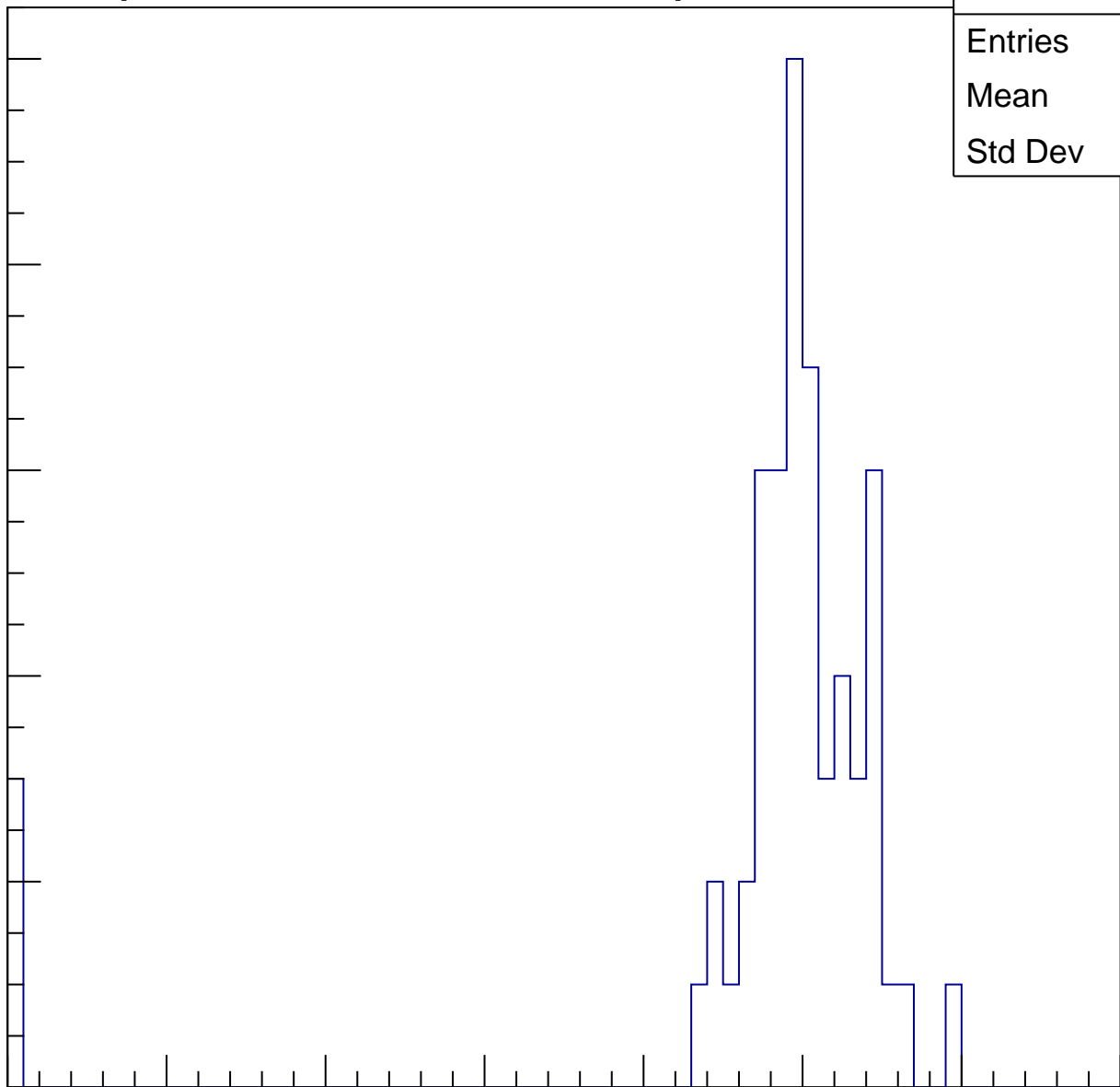
Entries	57
Mean	47.23
Std Dev	11.56

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

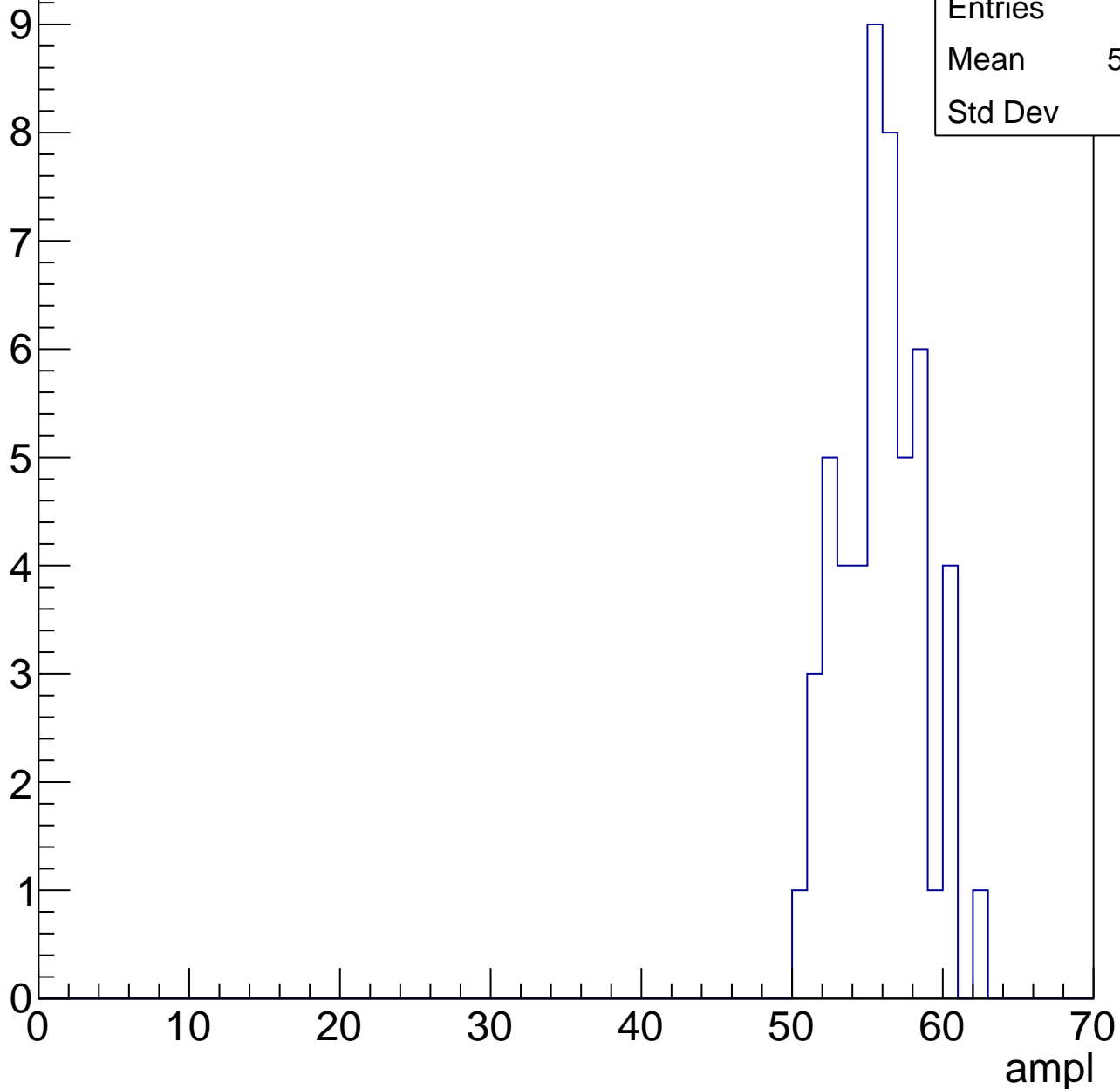
ampl



B1L103S, U7-ch1, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	51
Mean	55.45
Std Dev	2.71

B1L103S, U7-ch1, adc5

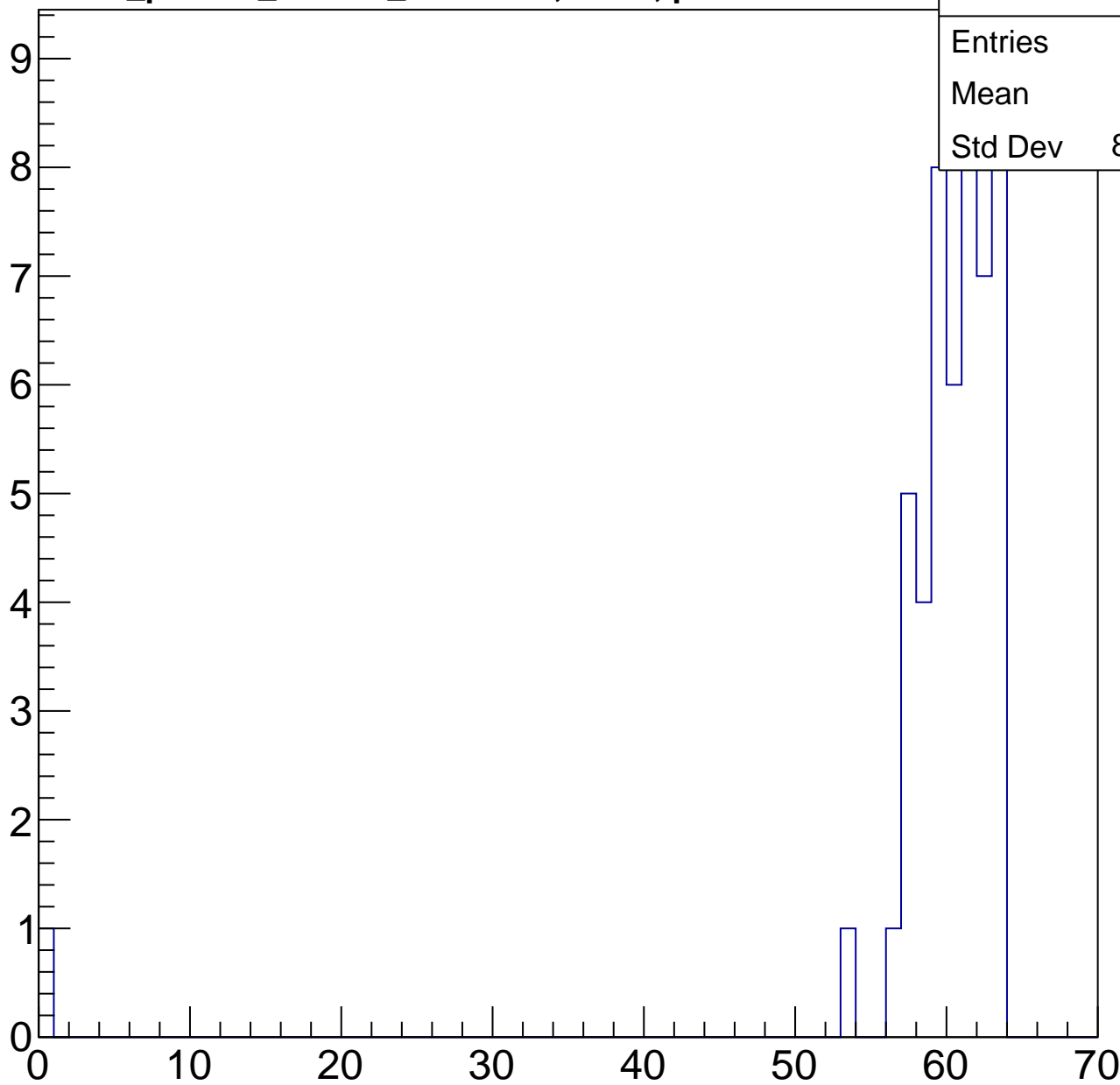
calib_packv5_041523_1651.root, FC#0, port C2

Entry

9
8
7
6
5
4
3
2
1
0

Entries	50
Mean	58.9
Std Dev	8.698

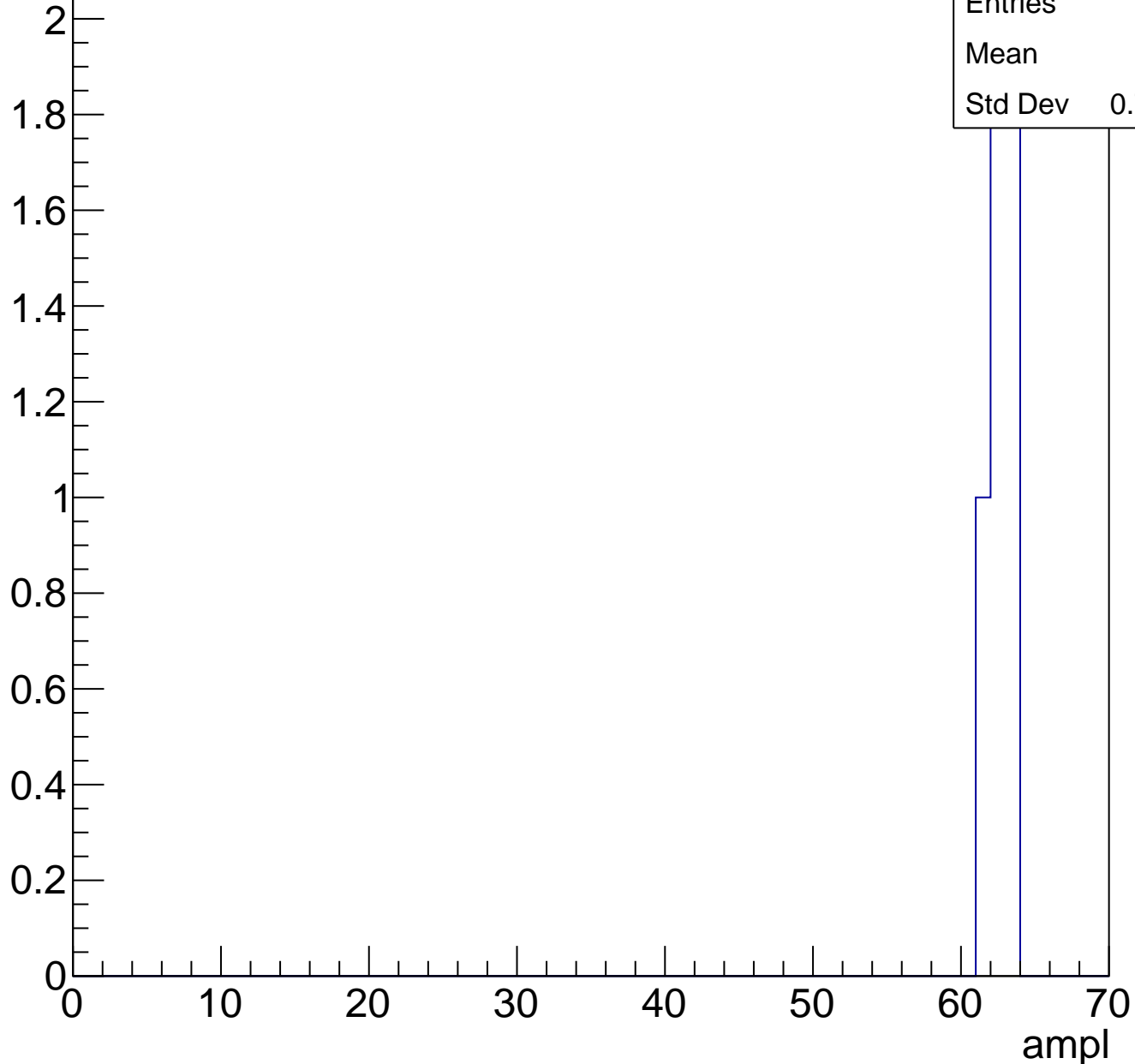
ampl



B1L103S, U7-ch1, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

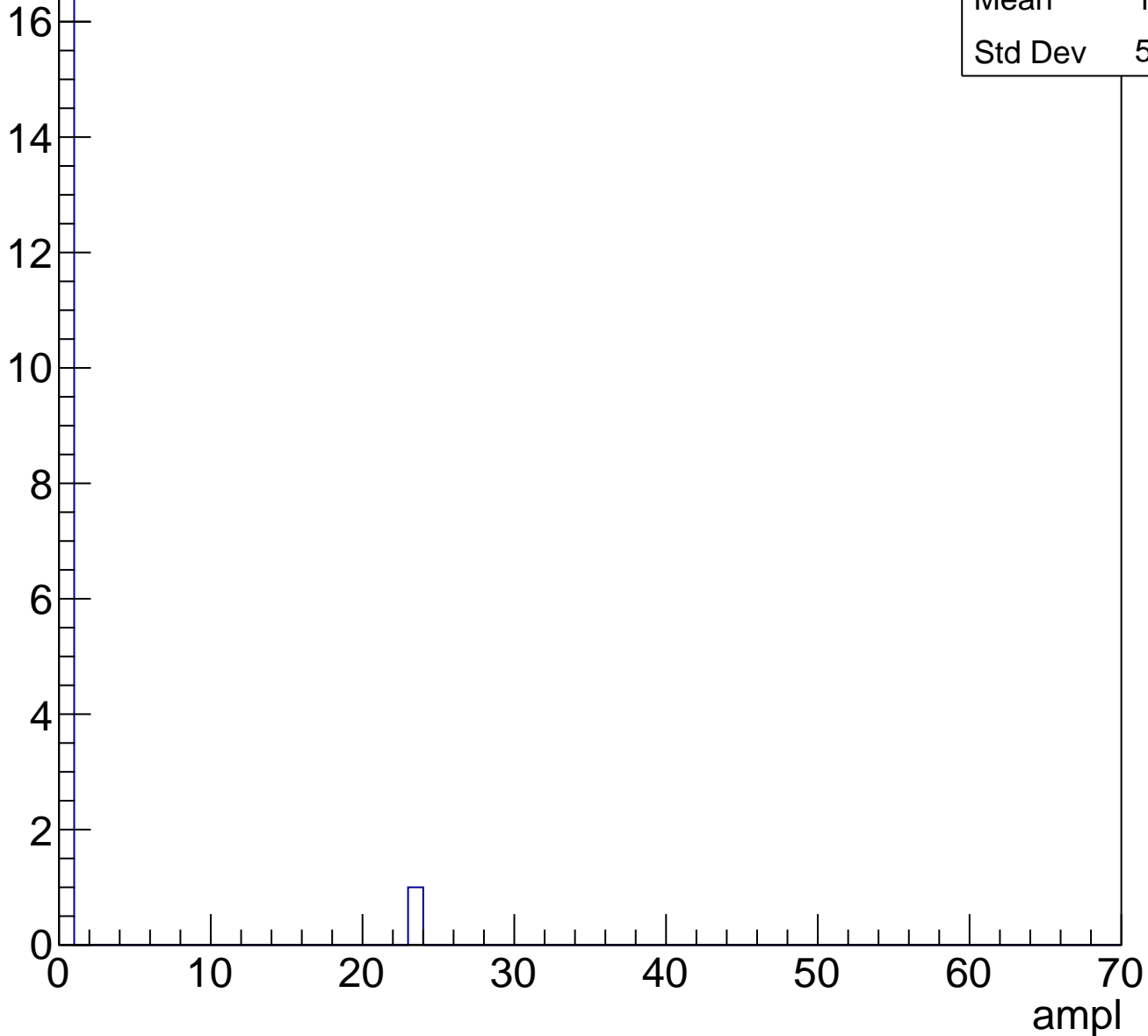


B1L103S, U7-ch1, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	18
Mean	1.278
Std Dev	5.268

Entry



B1L103S, U7-ch2, adc0

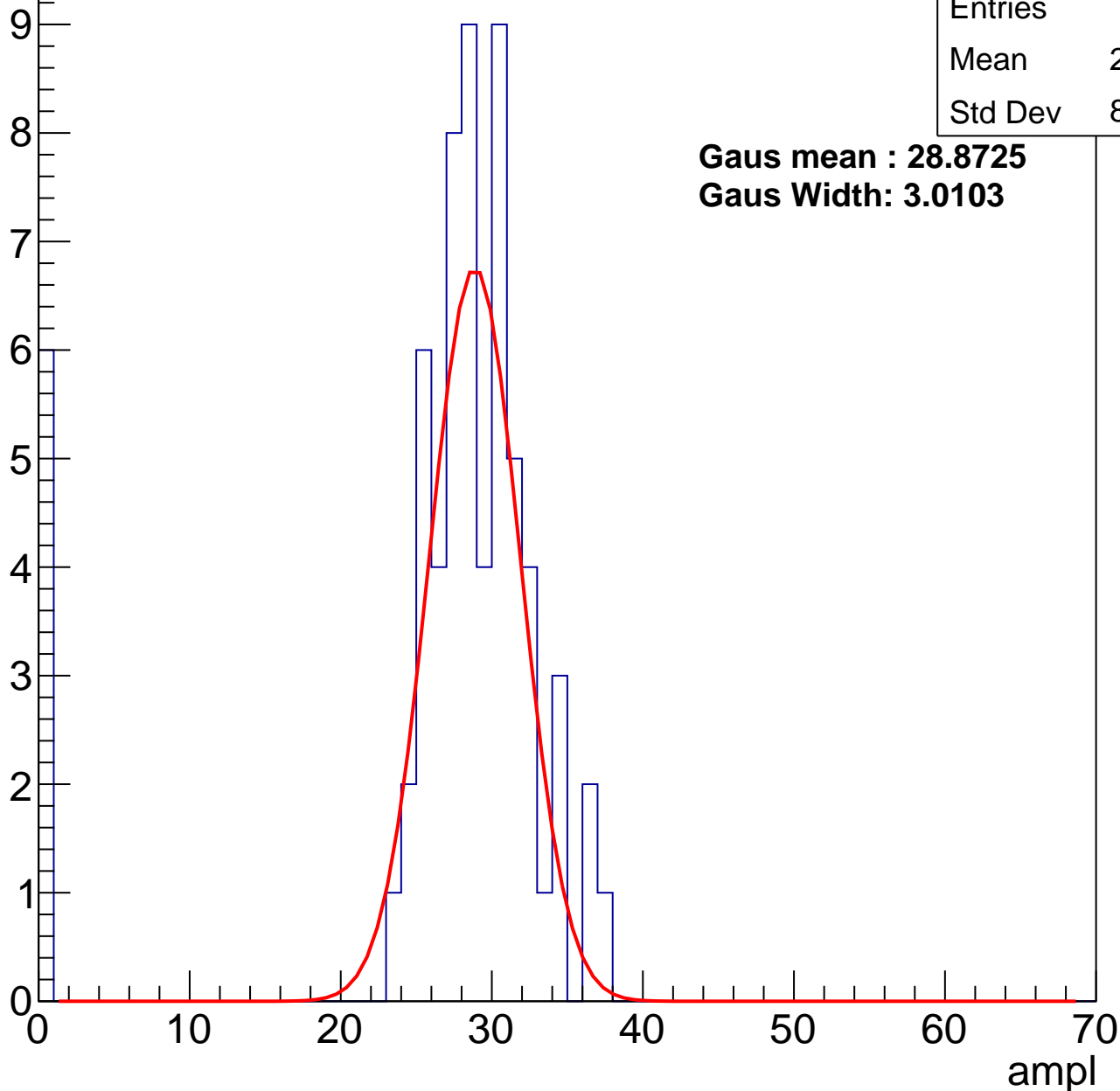
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	26.25
Std Dev	8.884

Gaus mean : 28.8725

Gaus Width: 3.0103



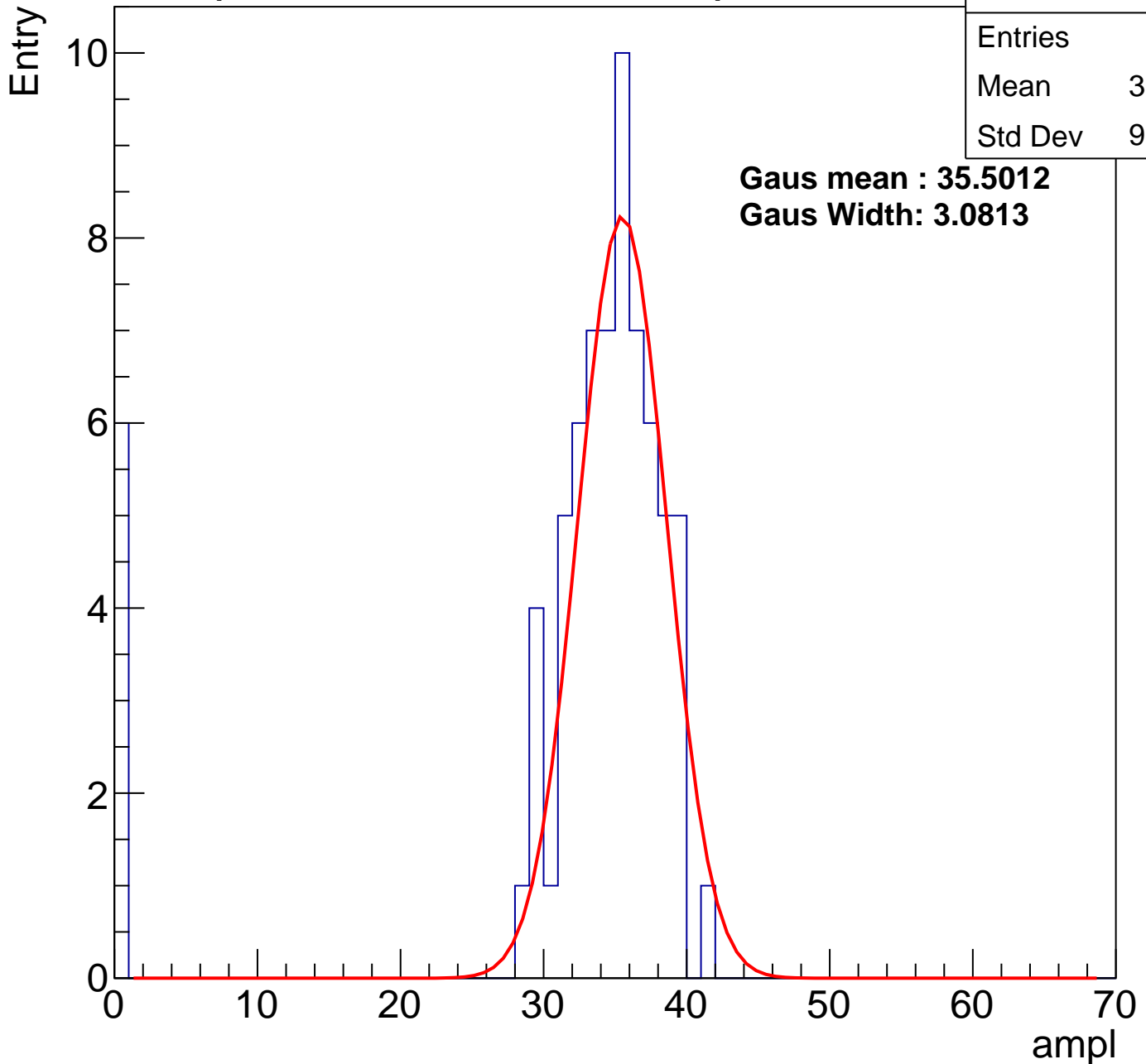
B1L103S, U7-ch2, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	71
Mean	31.55
Std Dev	9.988

Gaus mean : 35.5012

Gaus Width: 3.0813



B1L103S, U7-ch2, adc2

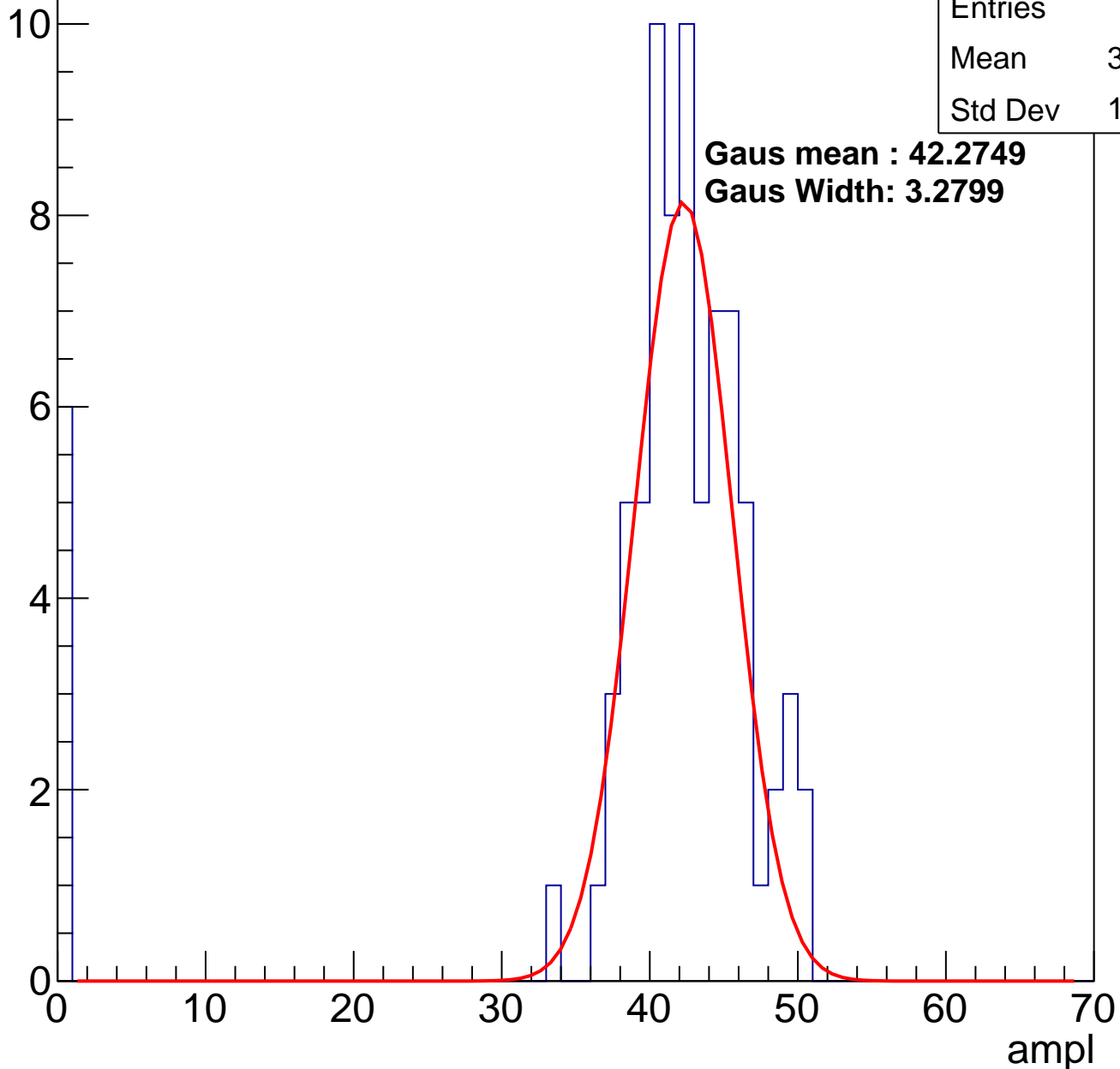
calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	39.15
Std Dev	11.57

Gaus mean : 42.2749

Gaus Width: 3.2799

Entry

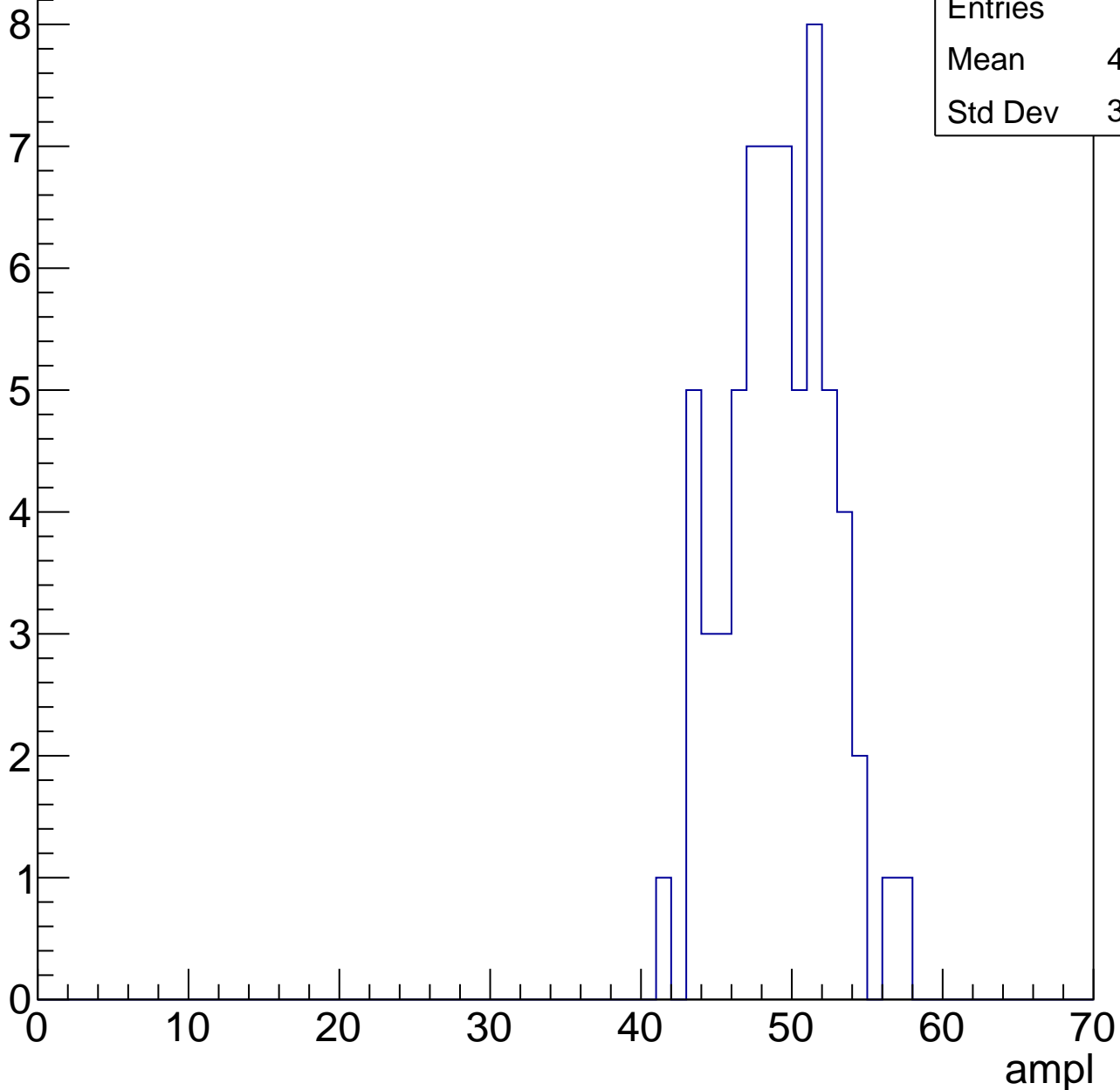


B1L103S, U7-ch2, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

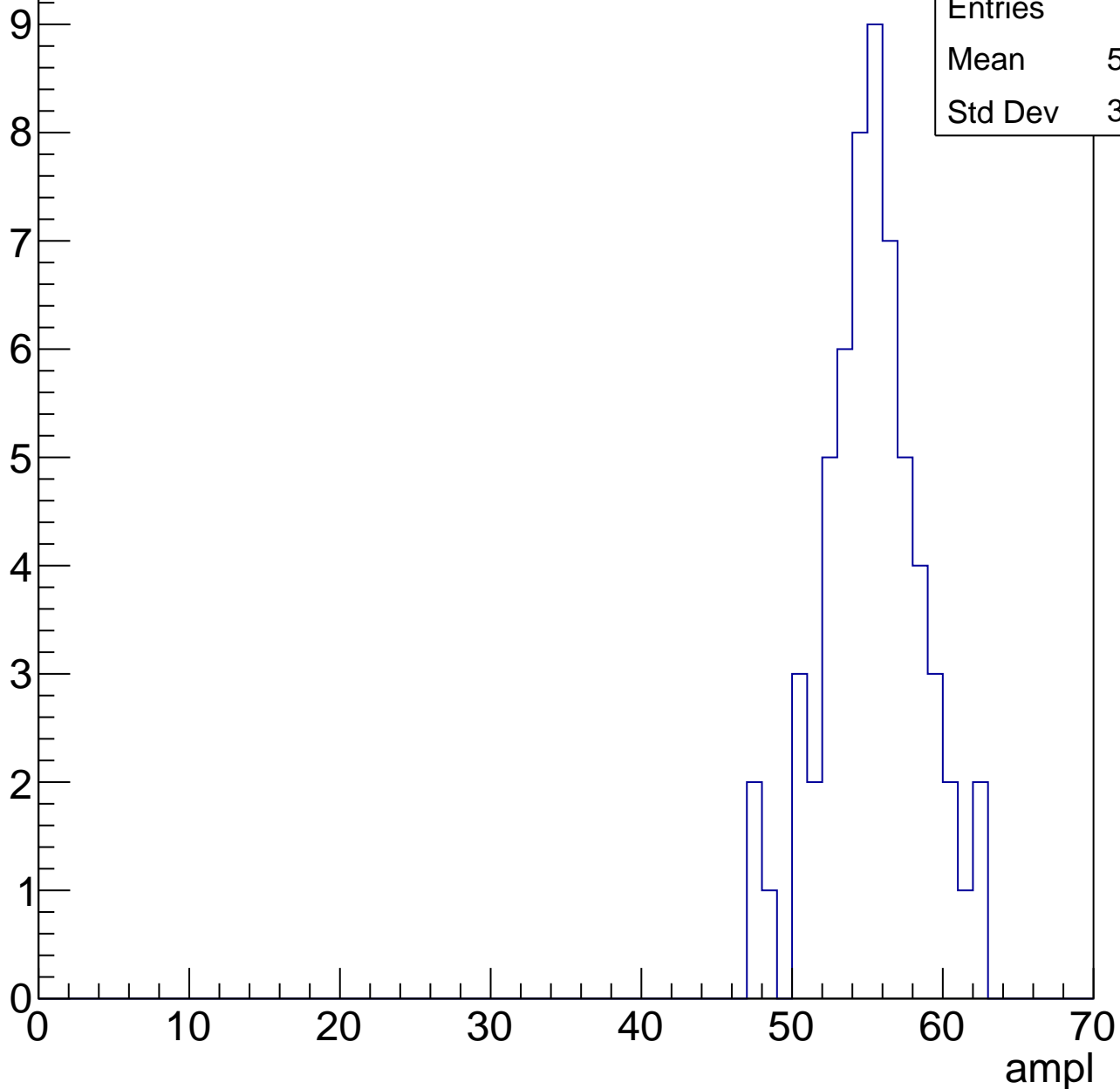
Entries	64
Mean	48.62
Std Dev	3.416



B1L103S, U7-ch2, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	60
Mean	54.83
Std Dev	3.302

B1L103S, U7-ch2, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

8
7
6
5
4
3
2
1
0

Entries	44
Mean	59.98
Std Dev	2.116

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

7

8

B1L103S, U7-ch2, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

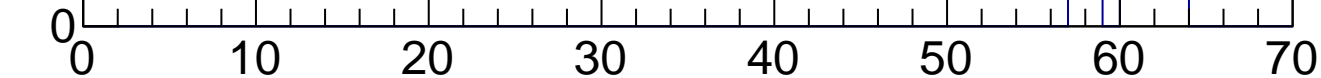
50

60

70

ampl

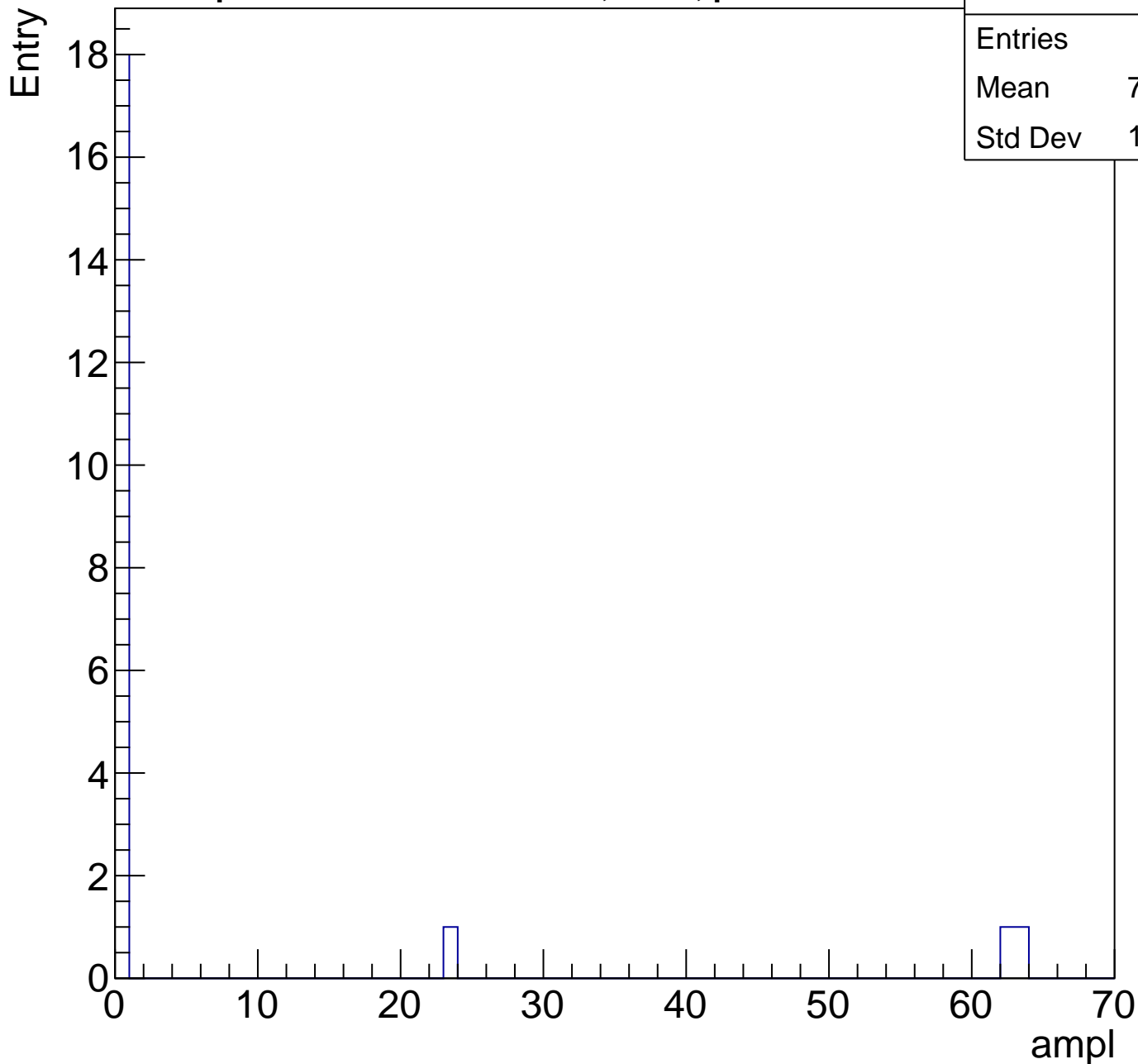
Entries	9
Mean	60.78
Std Dev	2.096



B1L103S, U7-ch2, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	7.048
Std Dev	18.64



B1L103S, U7-ch3, adc0

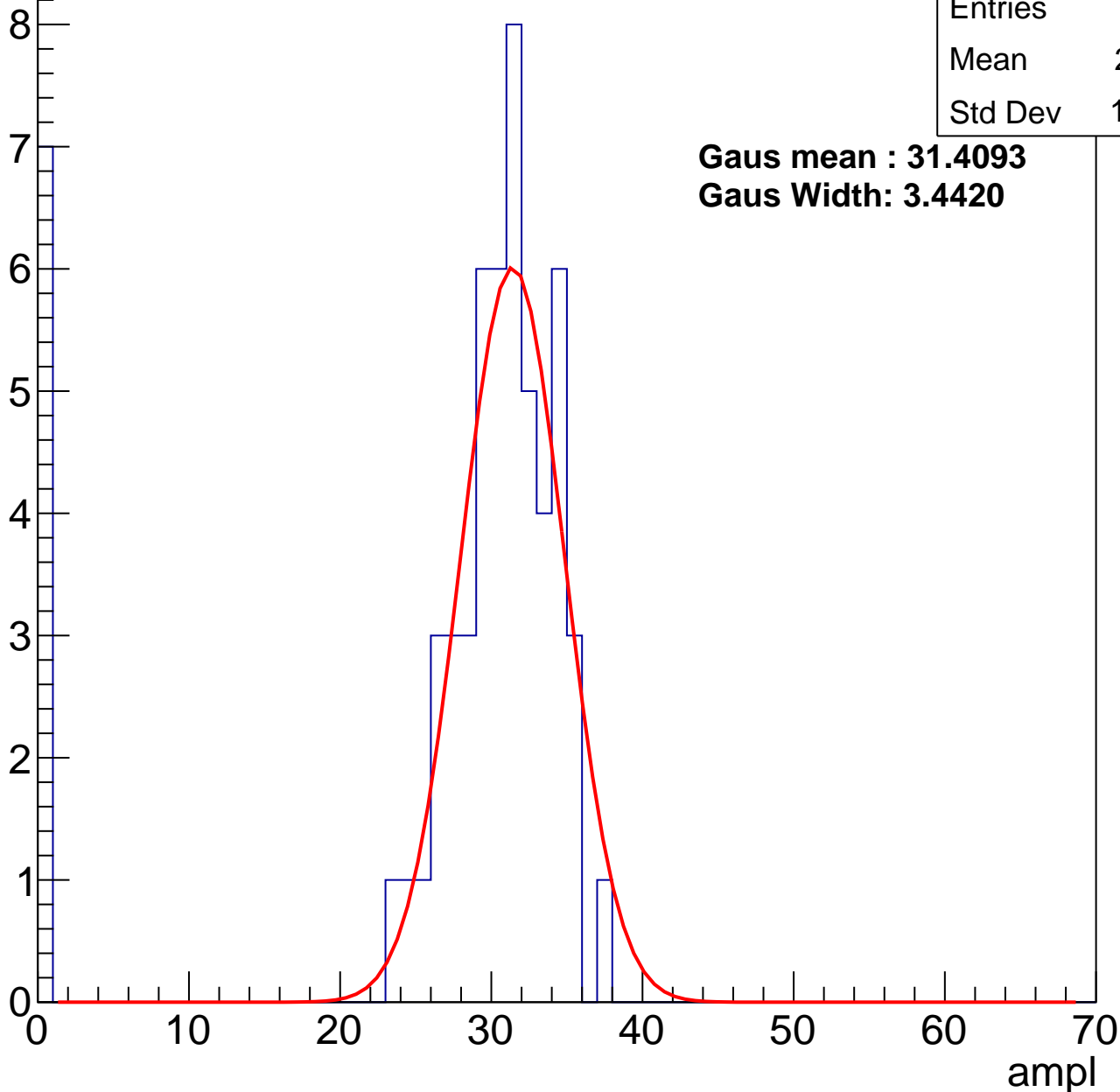
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	26.81
Std Dev	10.34

Gaus mean : 31.4093

Gaus Width: 3.4420

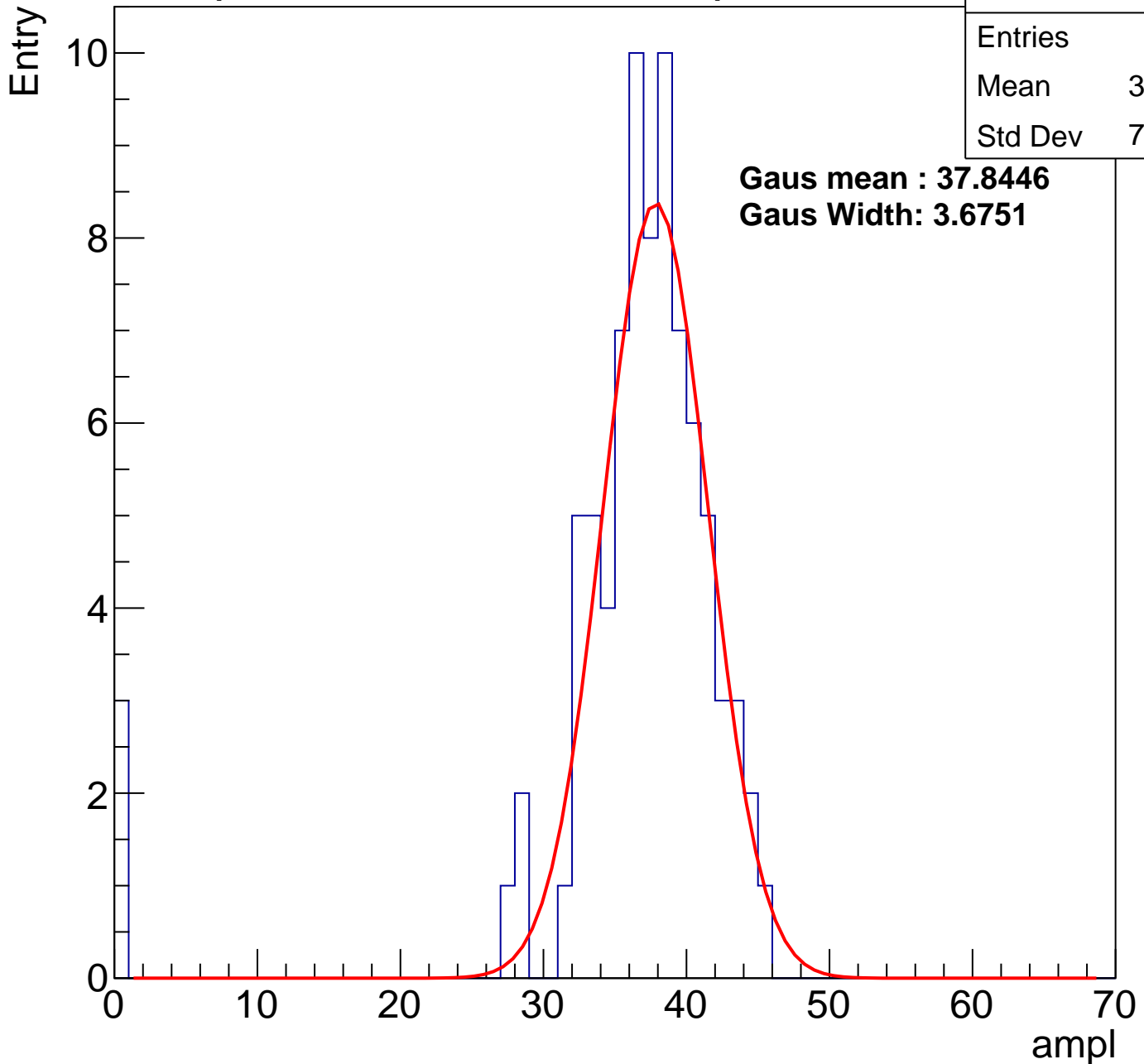


B1L103S, U7-ch3, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	83
Mean	35.69
Std Dev	7.806

Gaus mean : 37.8446
Gaus Width: 3.6751



B1L103S, U7-ch3, adc2

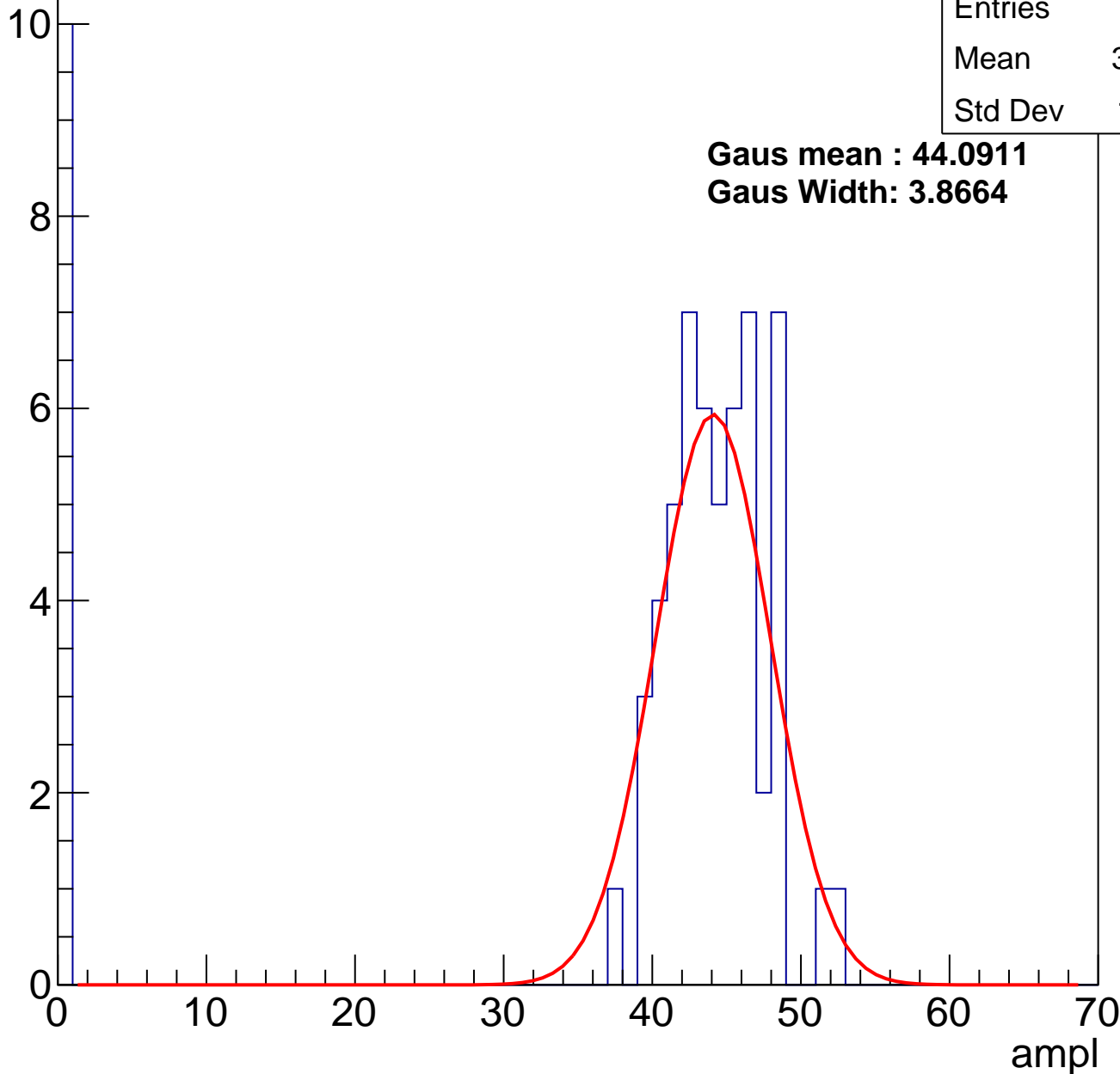
calib_packv5_041523_1651.root, FC#0, port C2

Entries	65
Mean	37.17
Std Dev	16.11

Gaus mean : 44.0911

Gaus Width: 3.8664

Entry

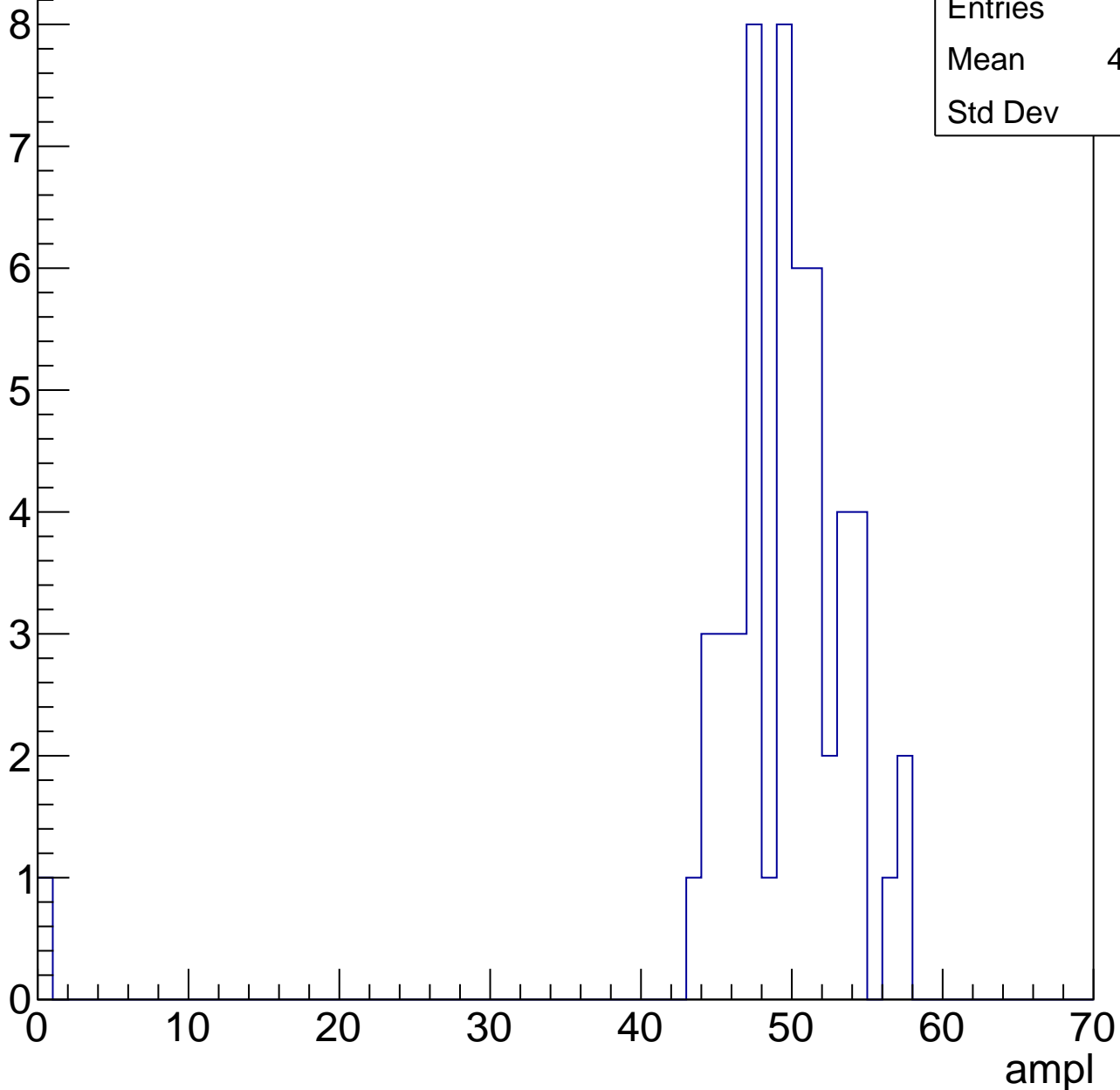


B1L103S, U7-ch3, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

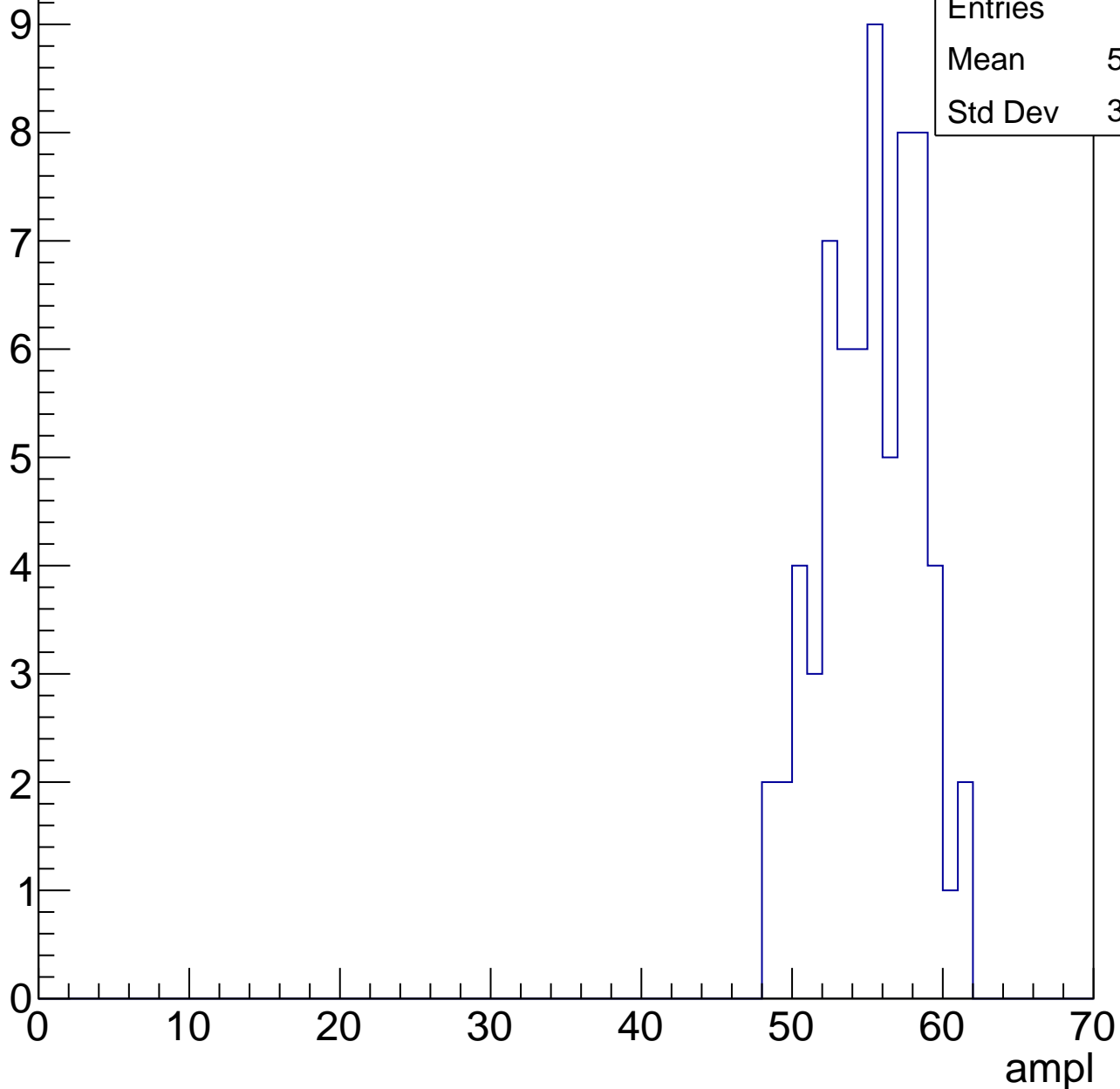
Entries	53
Mean	48.53
Std Dev	7.52



B1L103S, U7-ch3, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch3, adc5

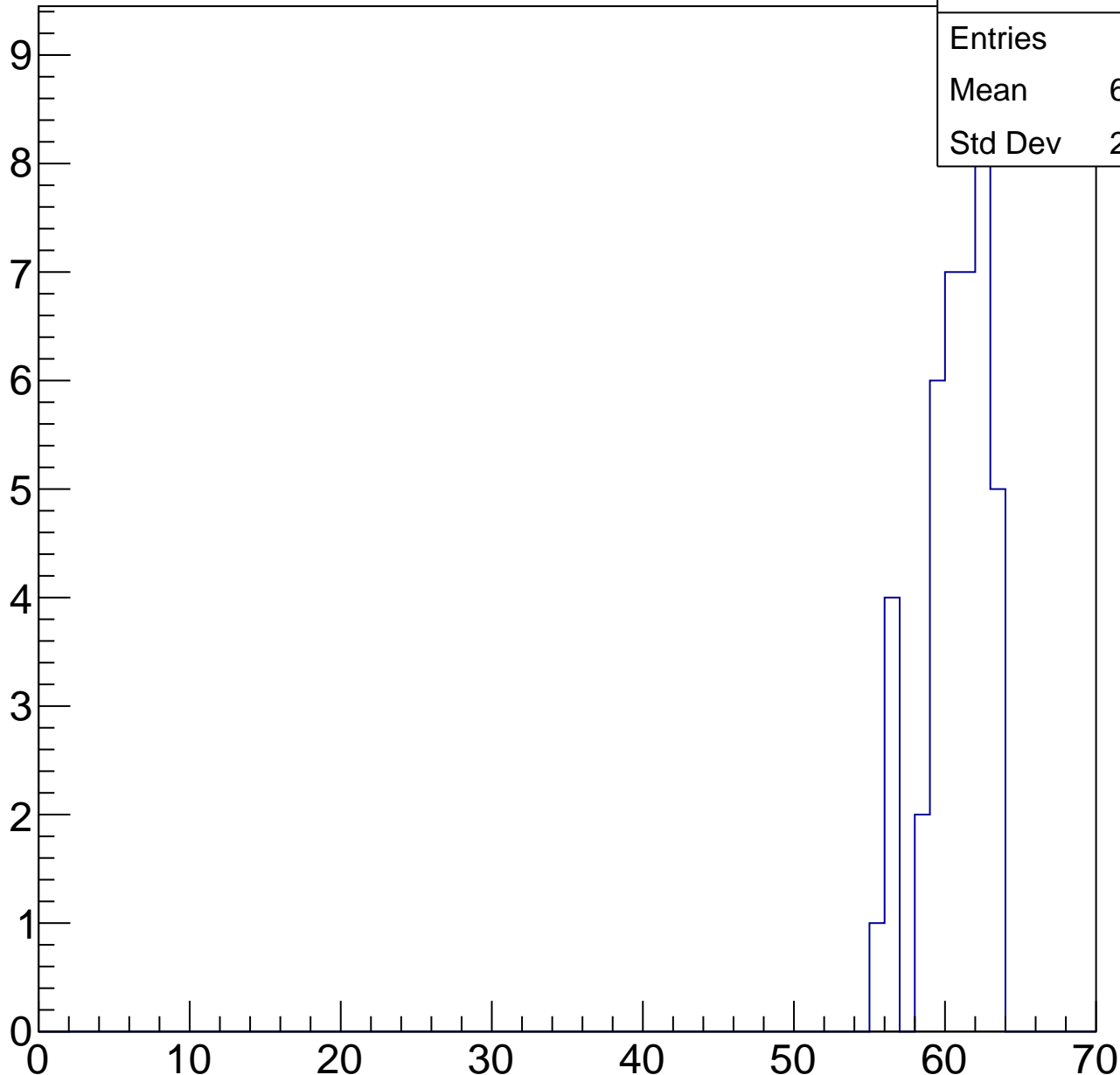
calib_packv5_041523_1651.root, FC#0, port C2

Entry

9
8
7
6
5
4
3
2
1
0

Entries	41
Mean	60.22
Std Dev	2.147

ampl

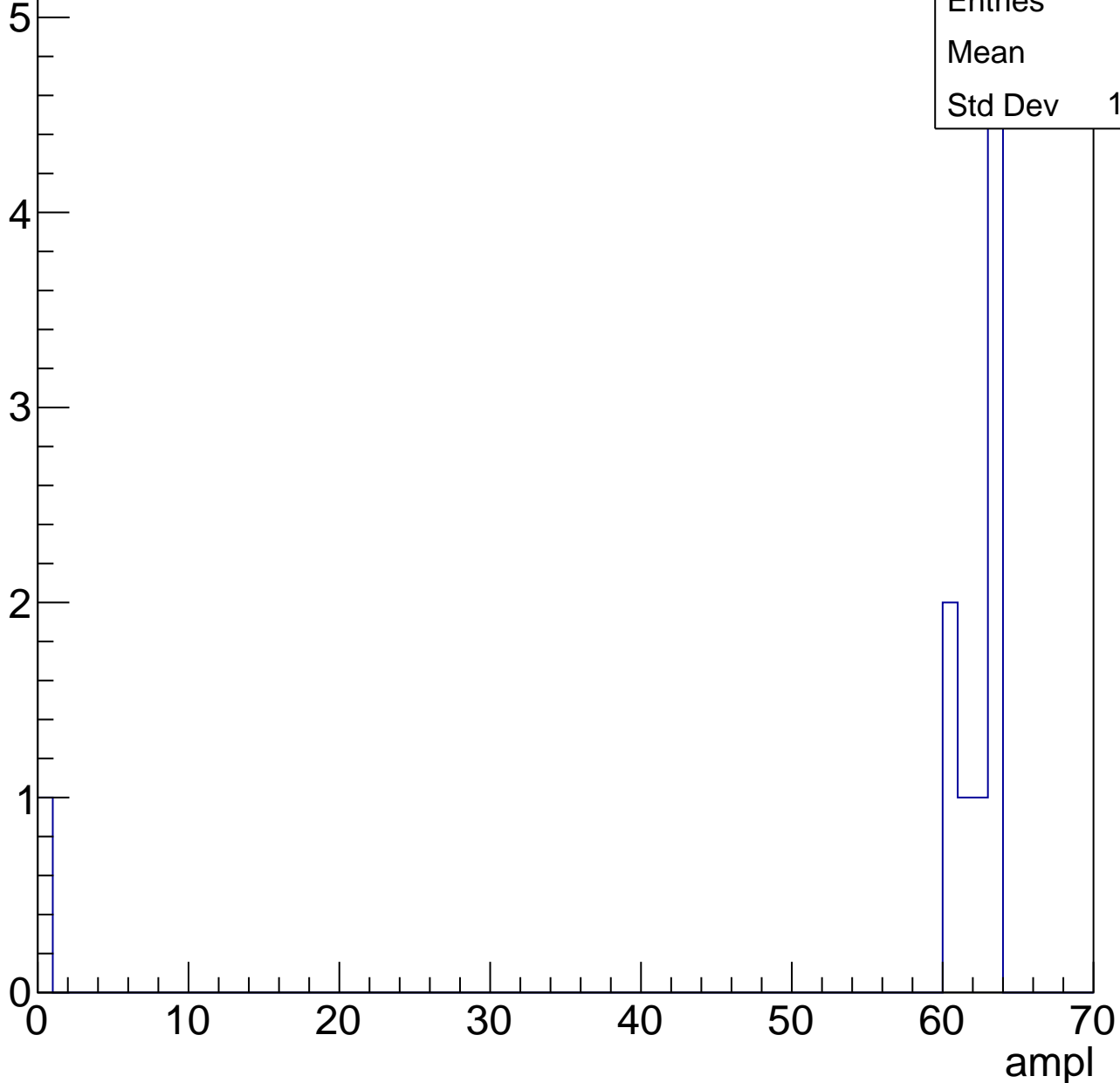


B1L103S, U7-ch3, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	10
Mean	55.8
Std Dev	18.64



B1L103S, U7-ch3, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	0
Std Dev	0



B1L103S, U7-ch4, adc0

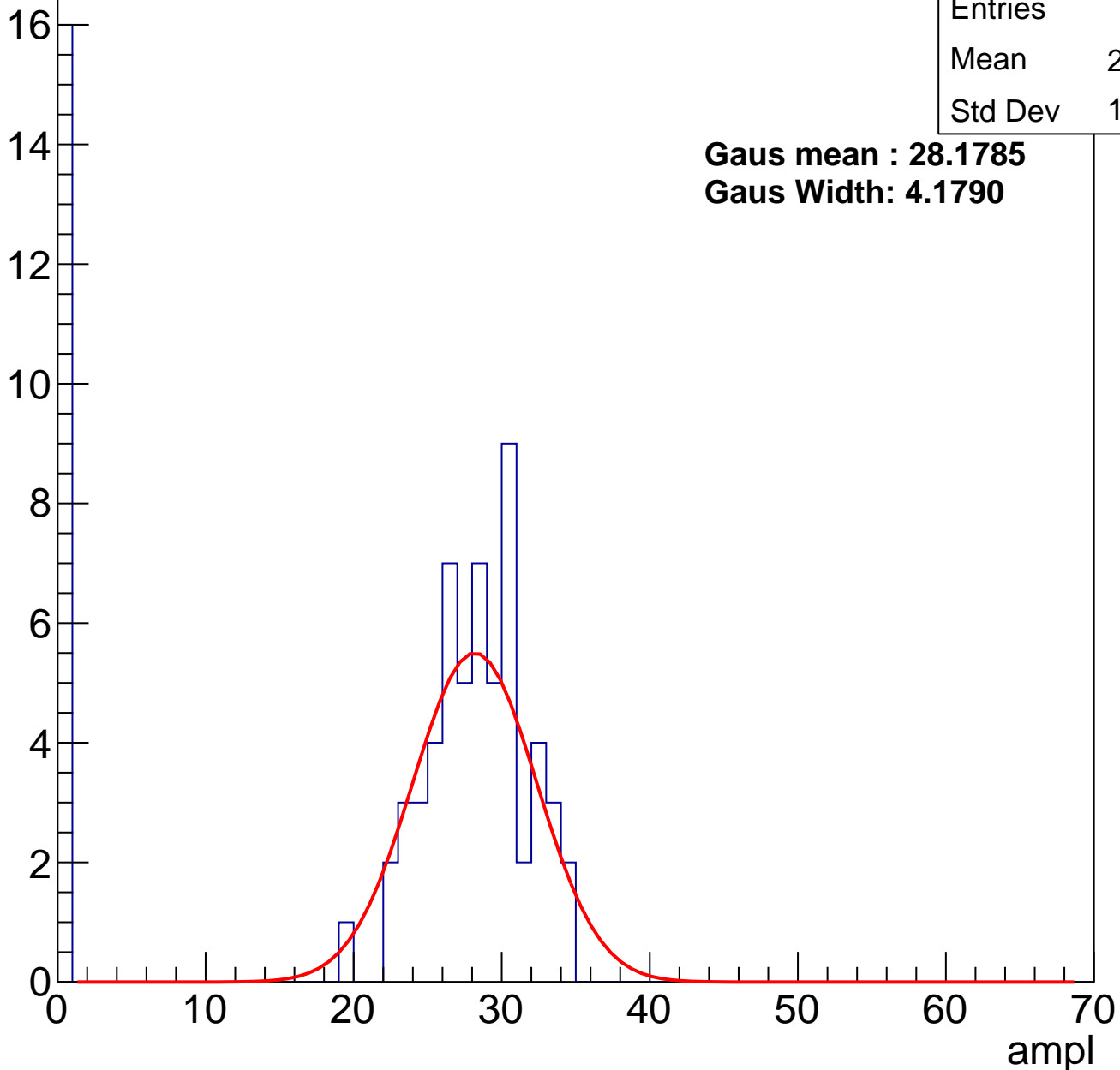
calib_packv5_041523_1651.root, FC#0, port C2

Entries	73
Mean	21.77
Std Dev	11.89

Gaus mean : 28.1785

Gaus Width: 4.1790

Entry

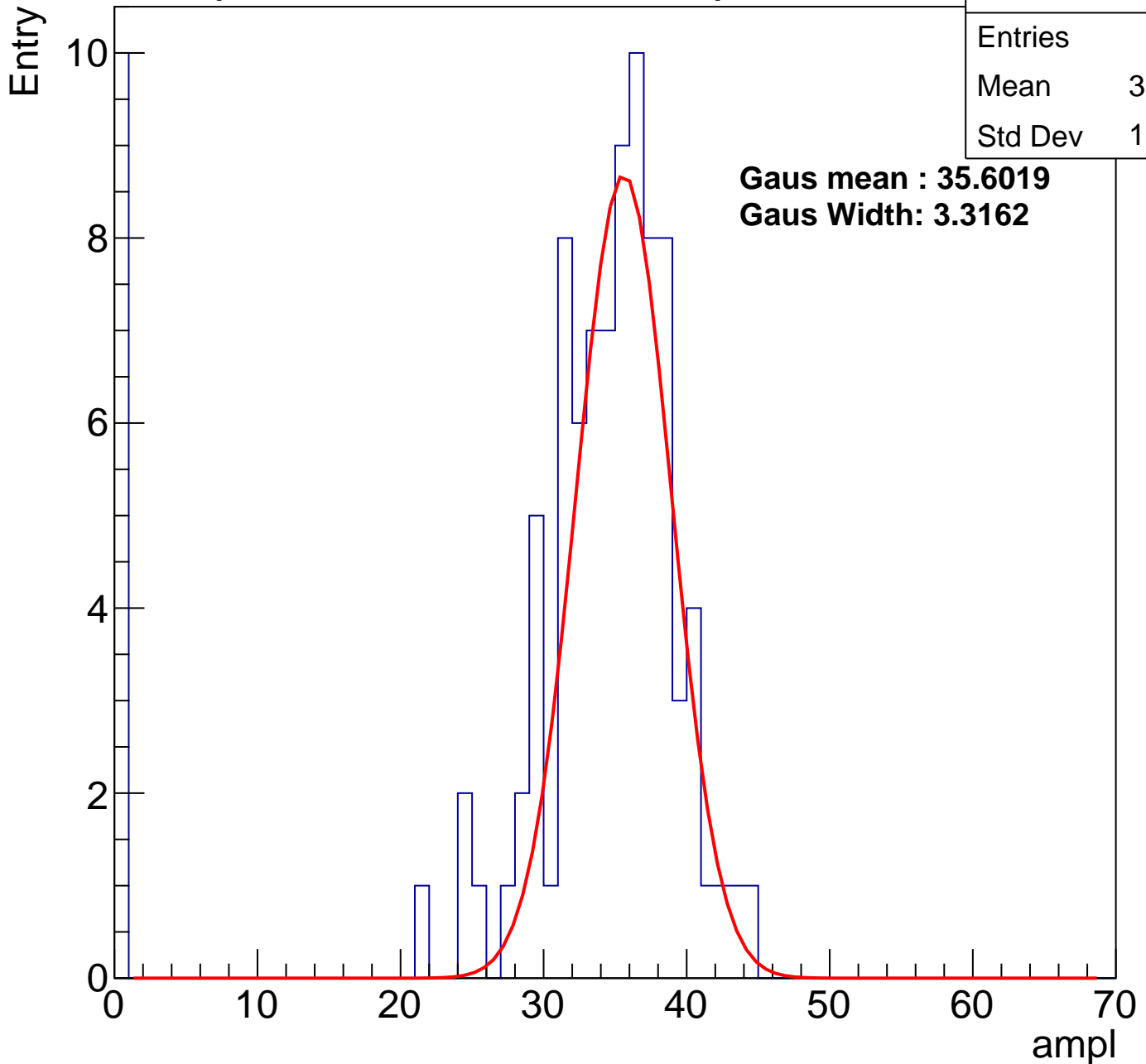


B1L103S, U7-ch4, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	97
Mean	30.75
Std Dev	11.18

Gaus mean : 35.6019
Gaus Width: 3.3162



B1L103S, U7-ch4, adc2

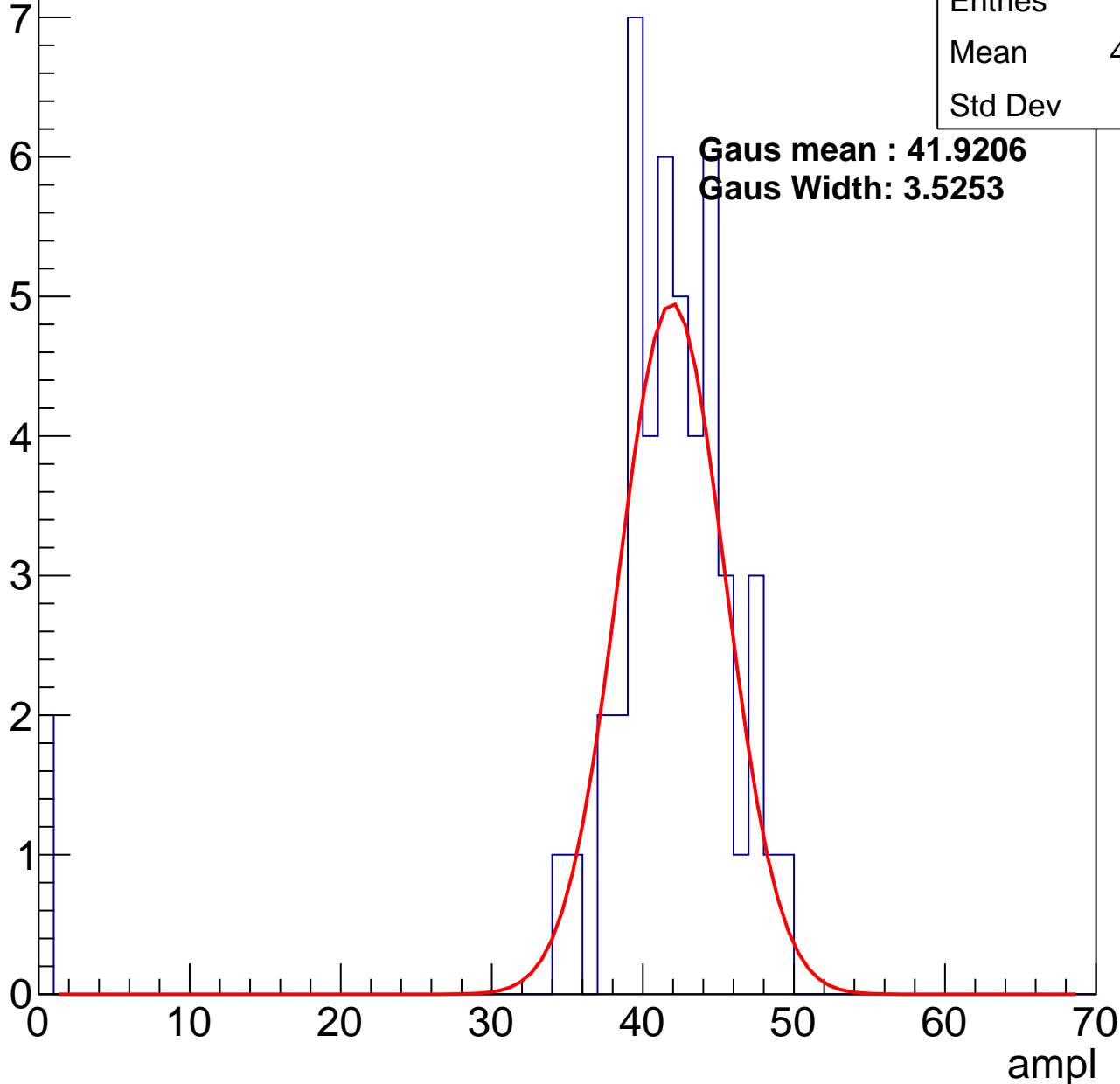
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	40.06
Std Dev	8.87

Gaus mean : 41.9206

Gaus Width: 3.5253

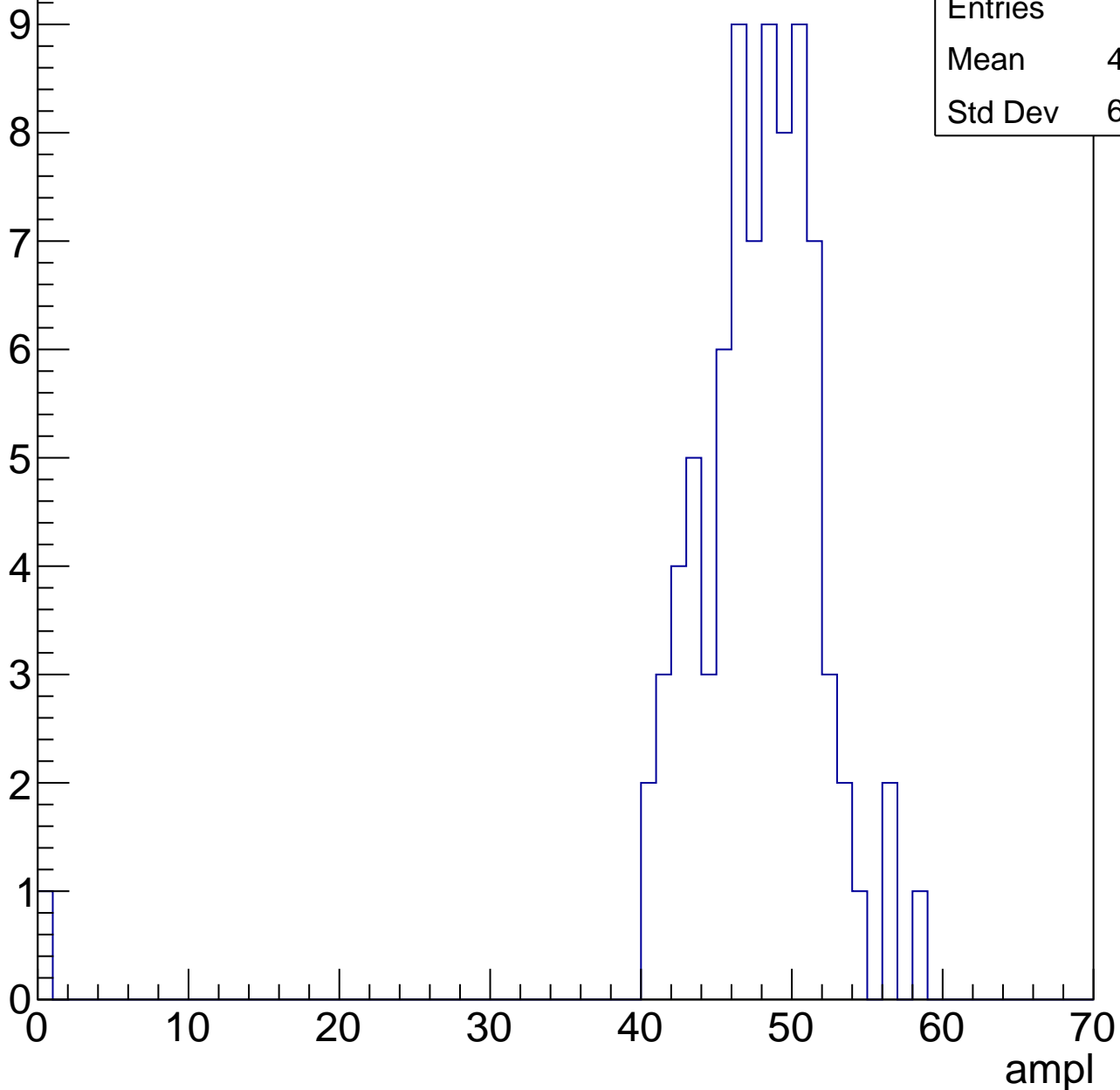


B1L103S, U7-ch4, adc3

calib_packv5_041523_1651.root, FC#0, port C2

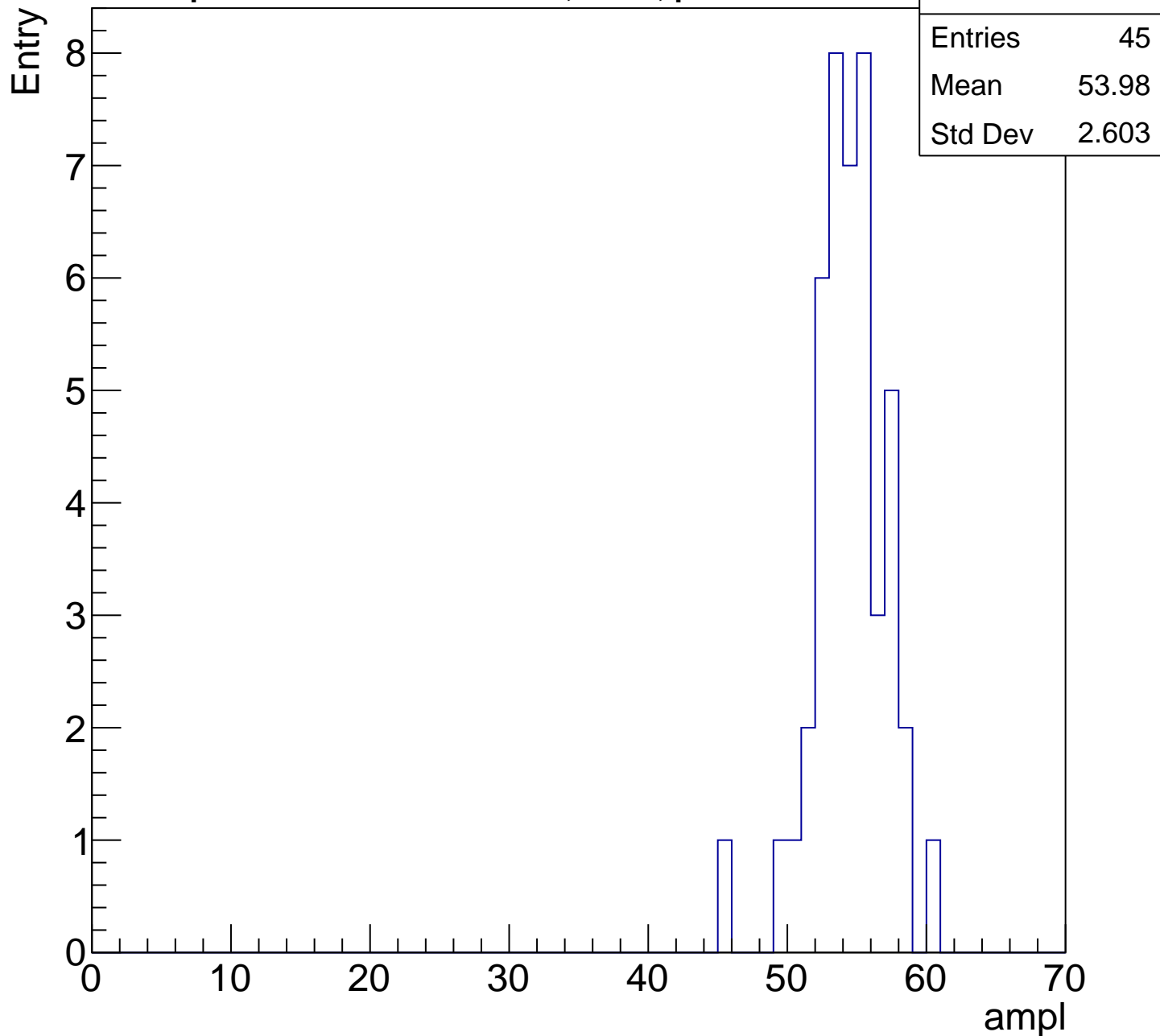
Entry

Entries	82
Mean	46.93
Std Dev	6.408



B1L103S, U7-ch4, adc4

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U7-ch4, adc5

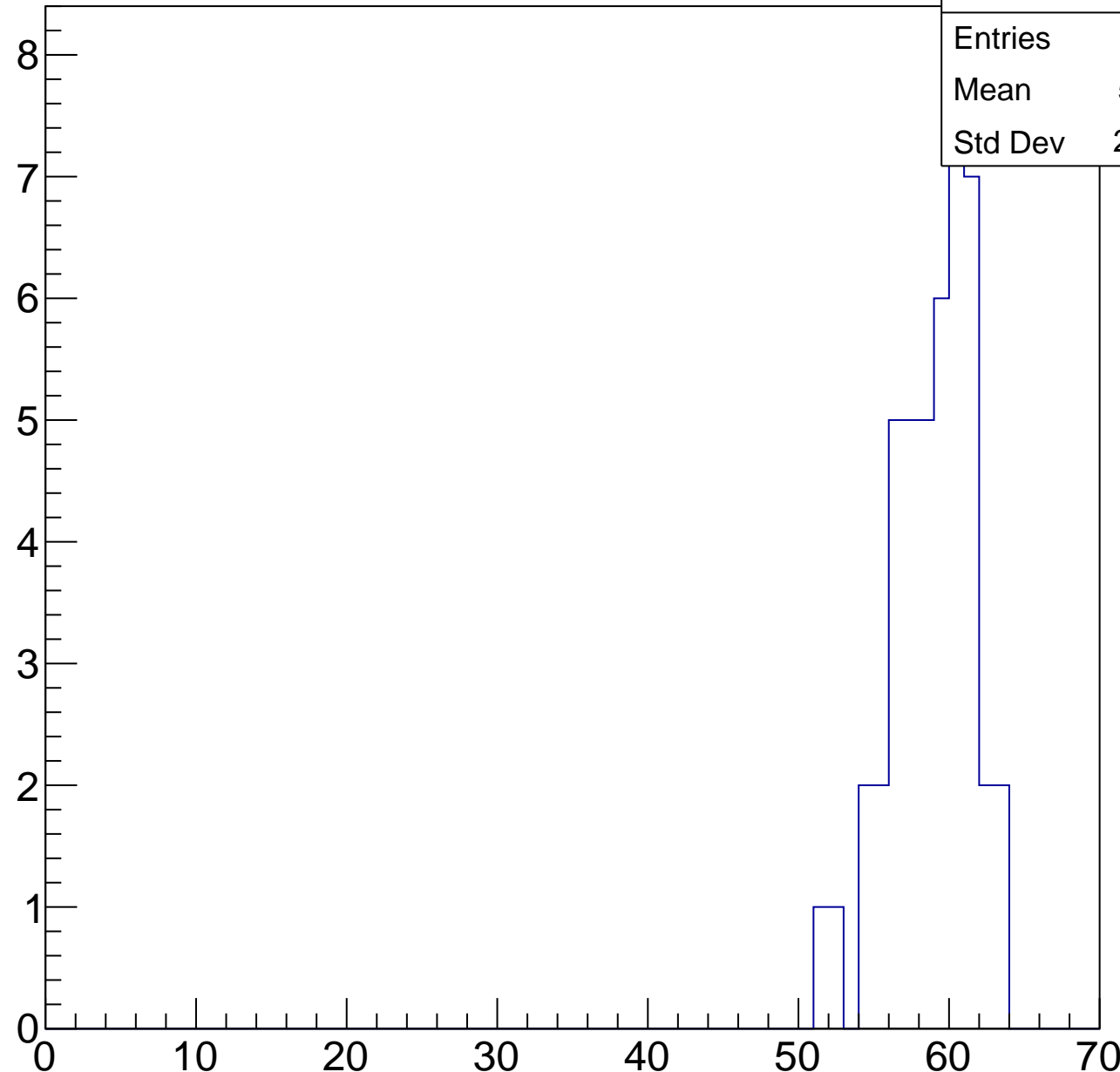
calib_packv5_041523_1651.root, FC#0, port C2

Entry

8
7
6
5
4
3
2
1
0

Entries	46
Mean	58.41
Std Dev	2.699

ampl

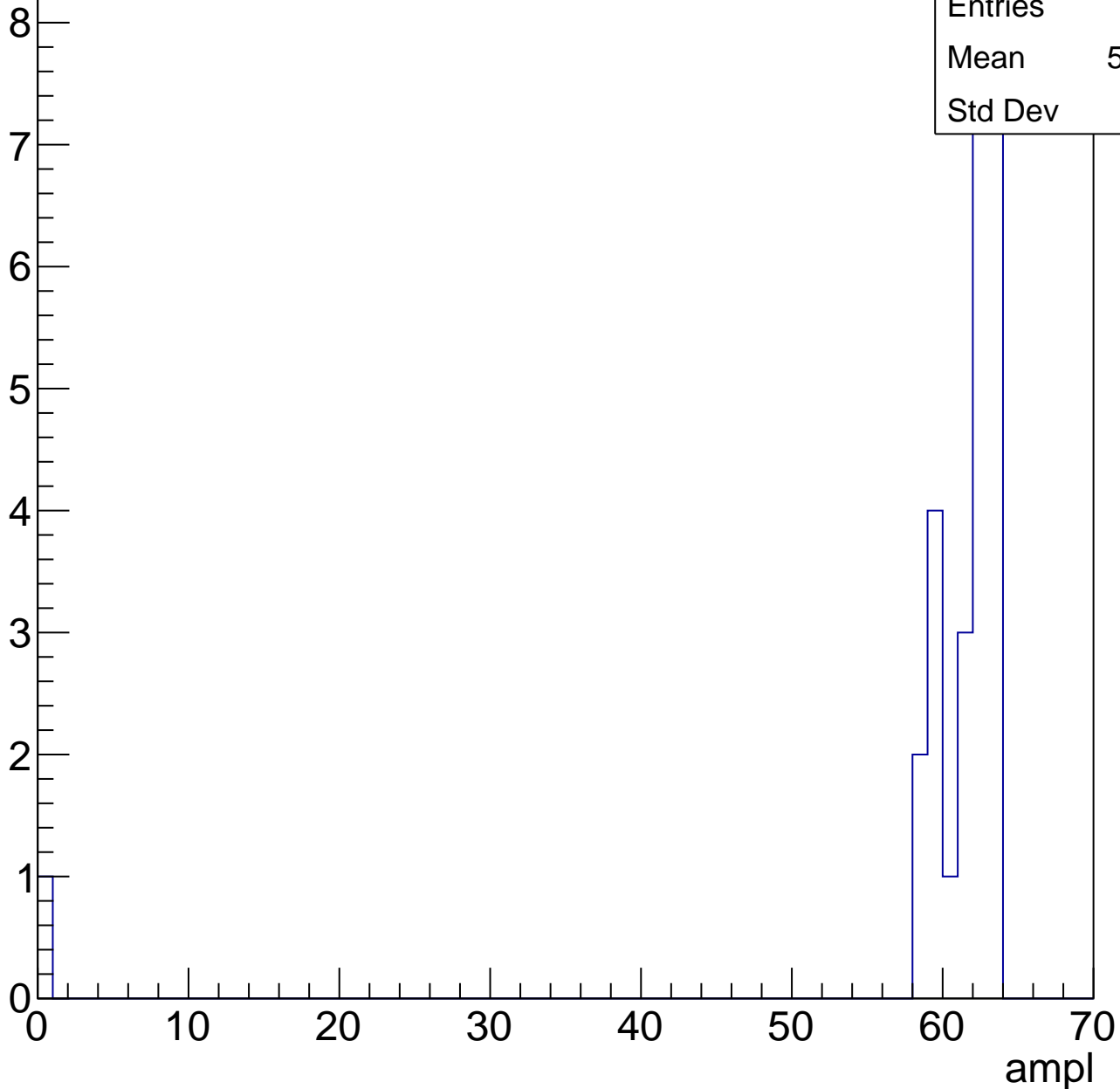


B1L103S, U7-ch4, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	27
Mean	59.07
Std Dev	11.7



B1L103S, U7-ch4, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	0
Std Dev	0



B1L103S, U7-ch5, adc0

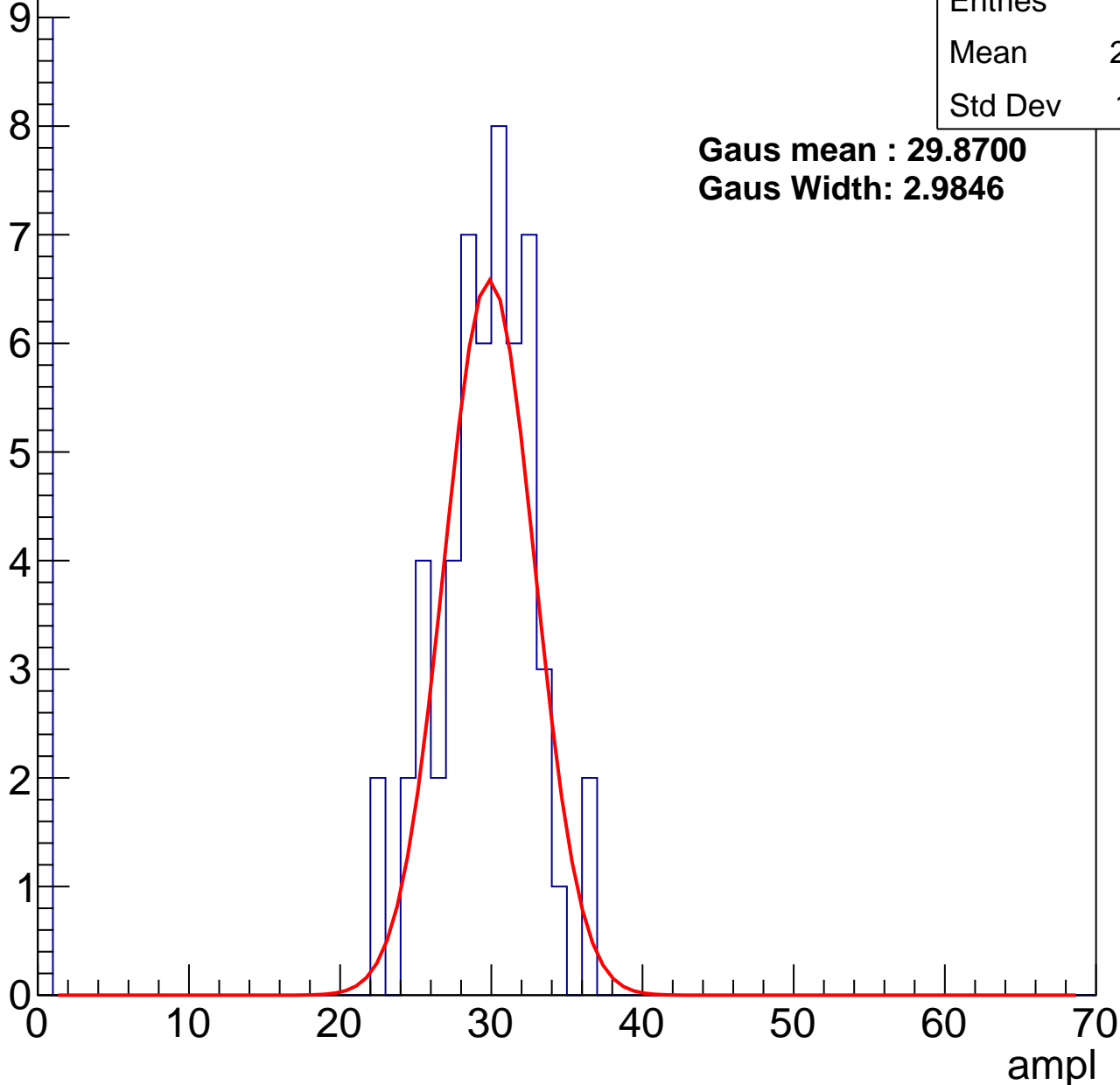
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	25.03
Std Dev	10.61

Gaus mean : 29.8700

Gaus Width: 2.9846



B1L103S, U7-ch5, adc1

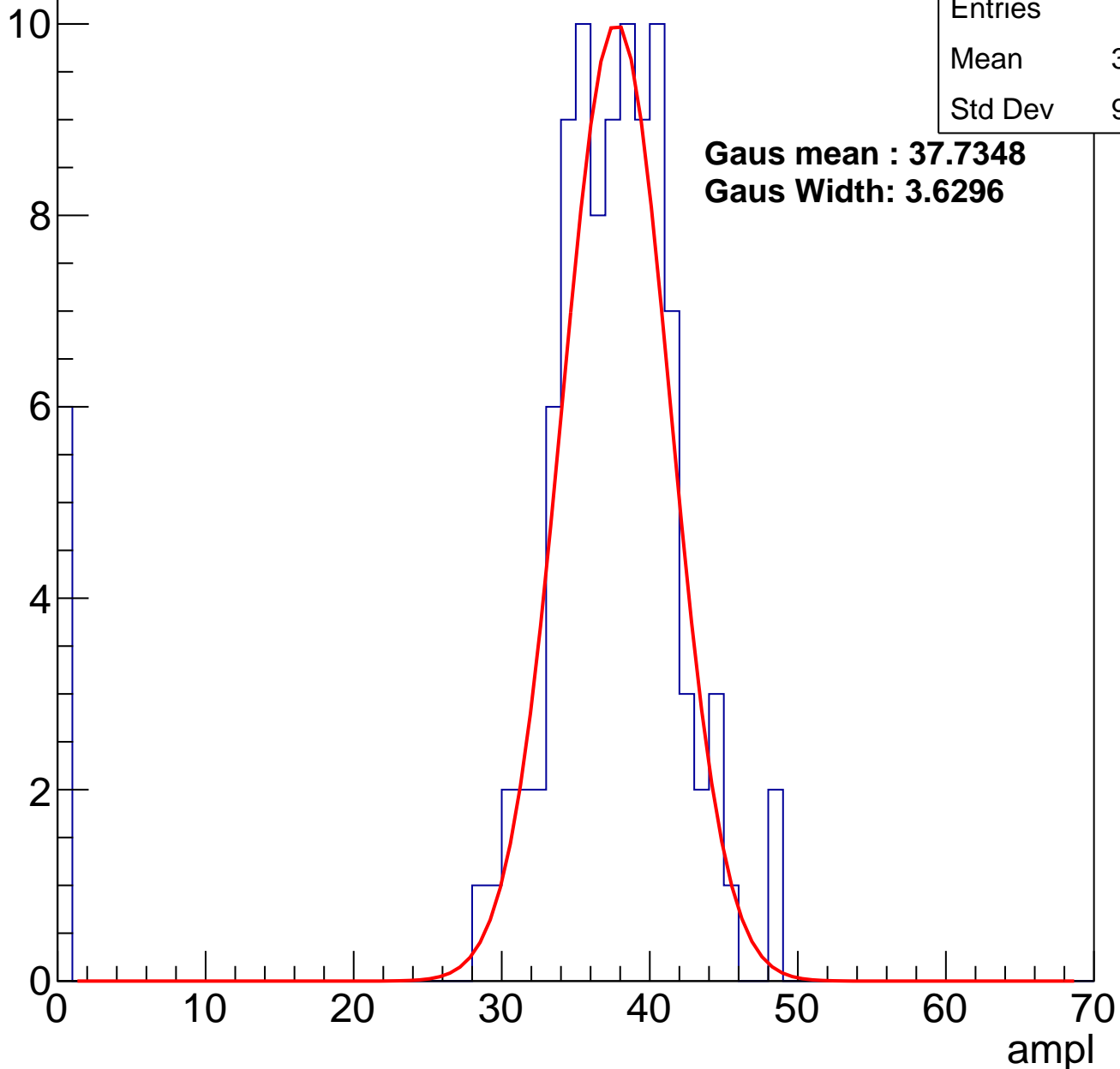
calib_packv5_041523_1651.root, FC#0, port C2

Entries	103
Mean	35.16
Std Dev	9.503

Gaus mean : 37.7348

Gaus Width: 3.6296

Entry



B1L103S, U7-ch5, adc2

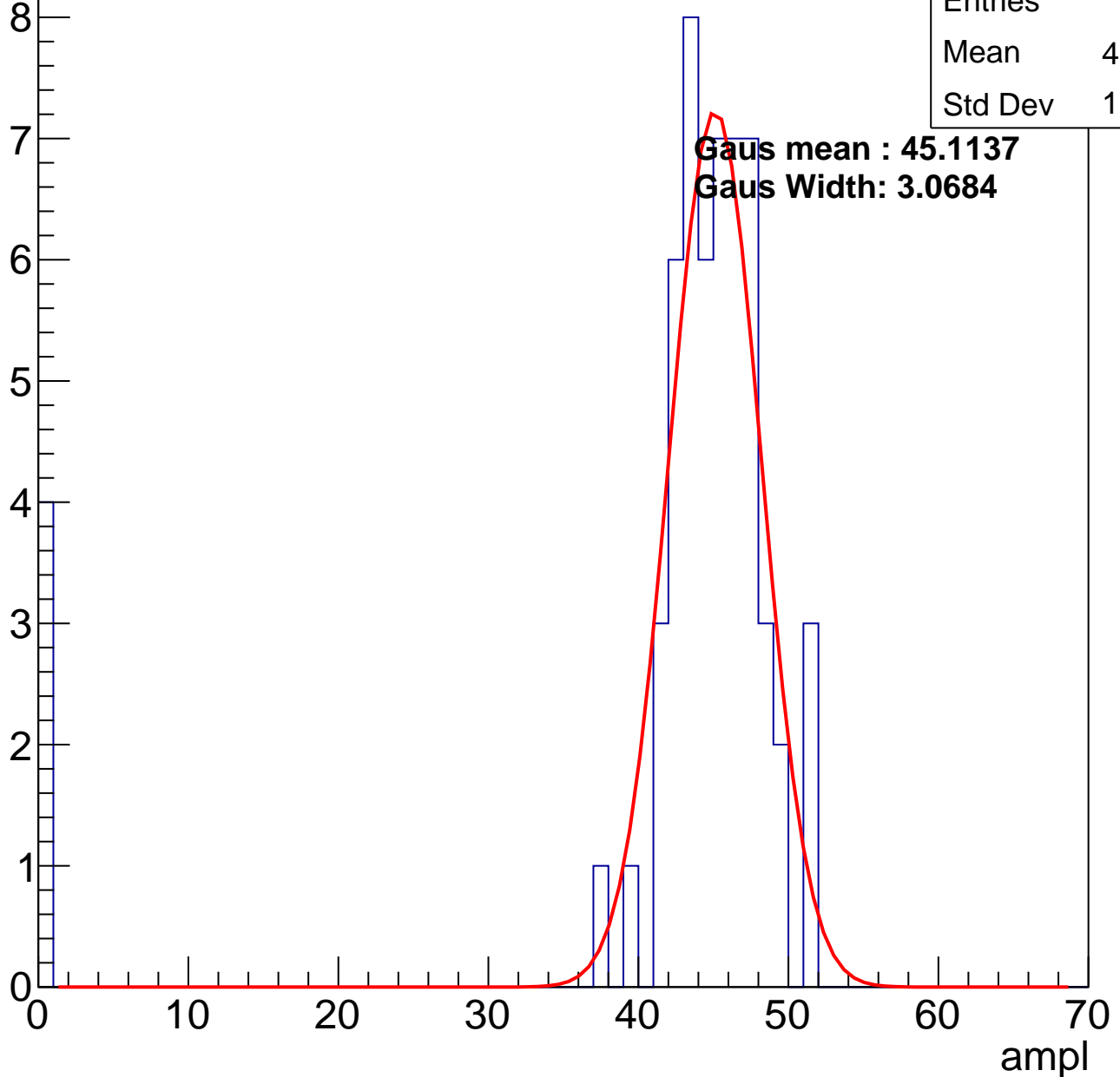
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	41.72
Std Dev	11.69

Gaus mean : 45.1137

Gaus Width: 3.0684

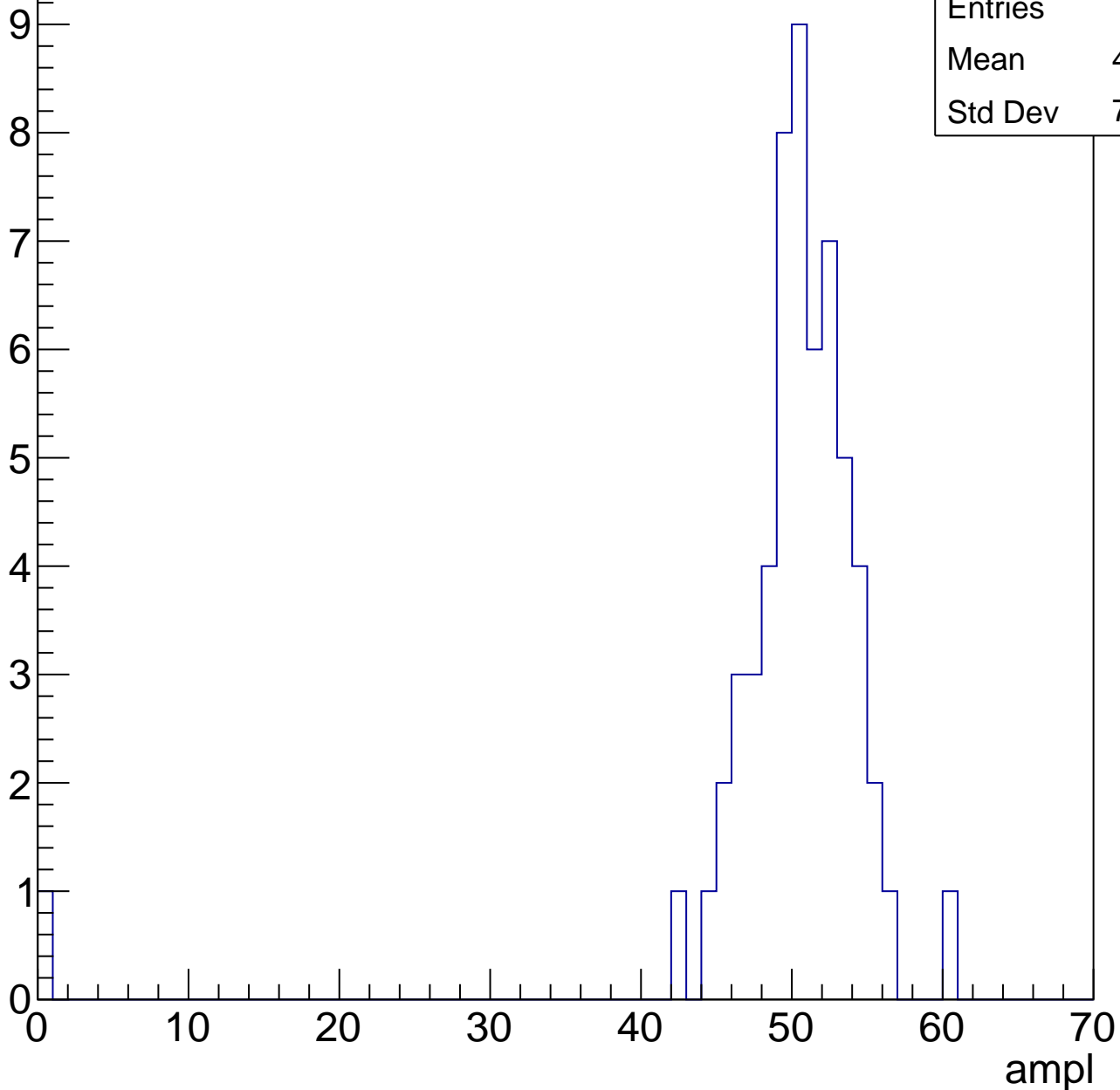


B1L103S, U7-ch5, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	49.41
Std Dev	7.261

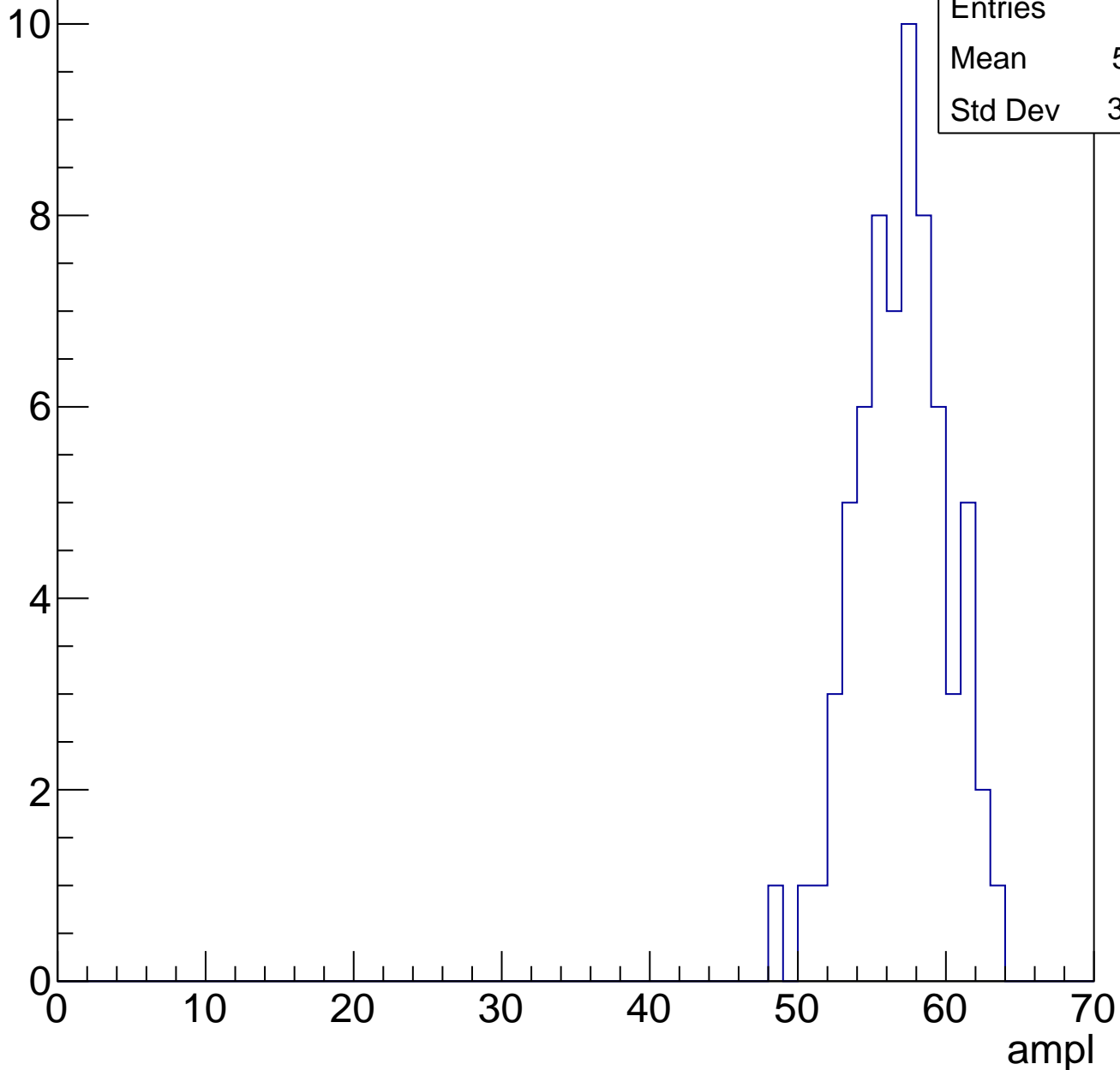


B1L103S, U7-ch5, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	67
Mean	56.51
Std Dev	3.049

Entry

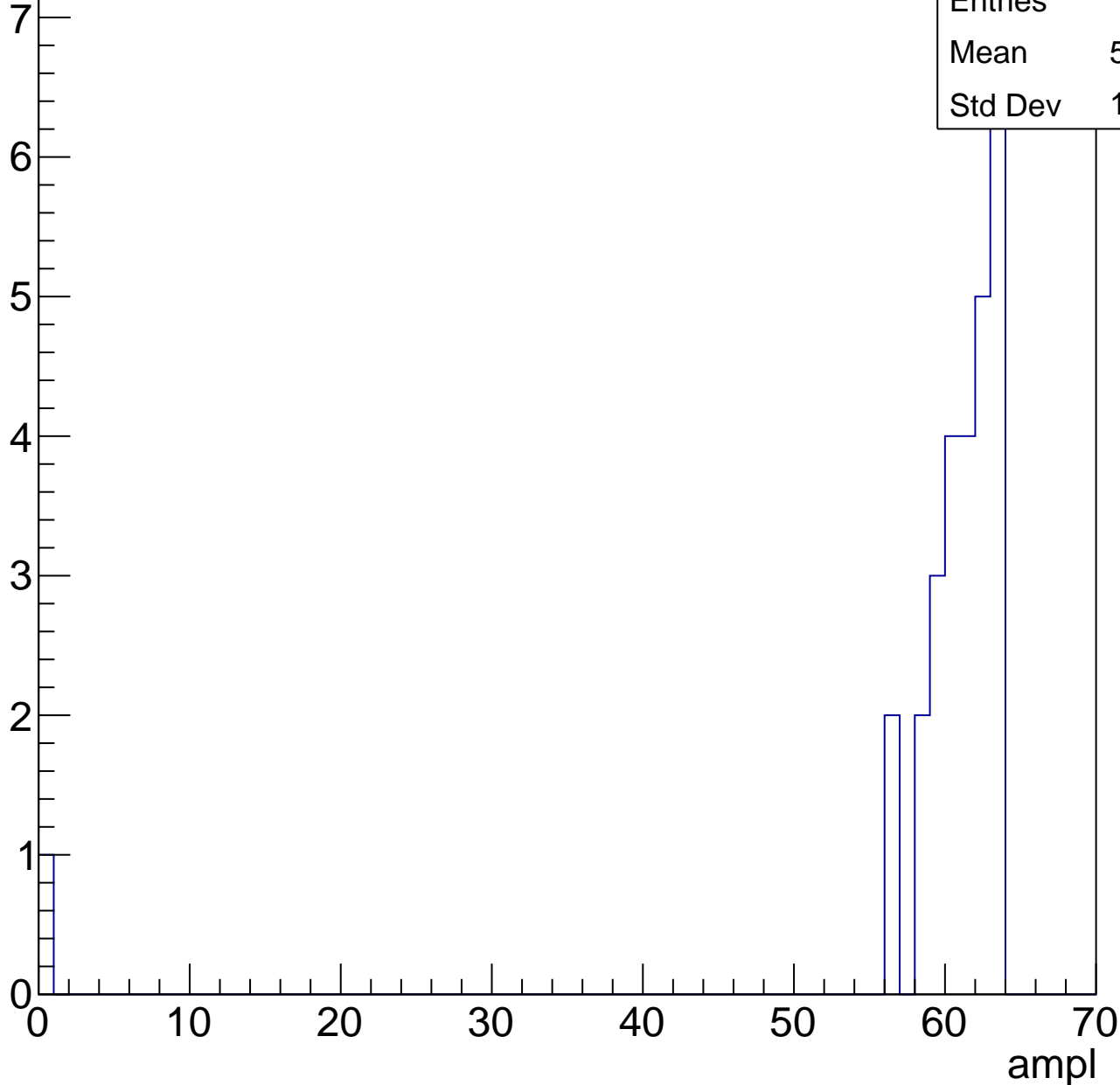


B1L103S, U7-ch5, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

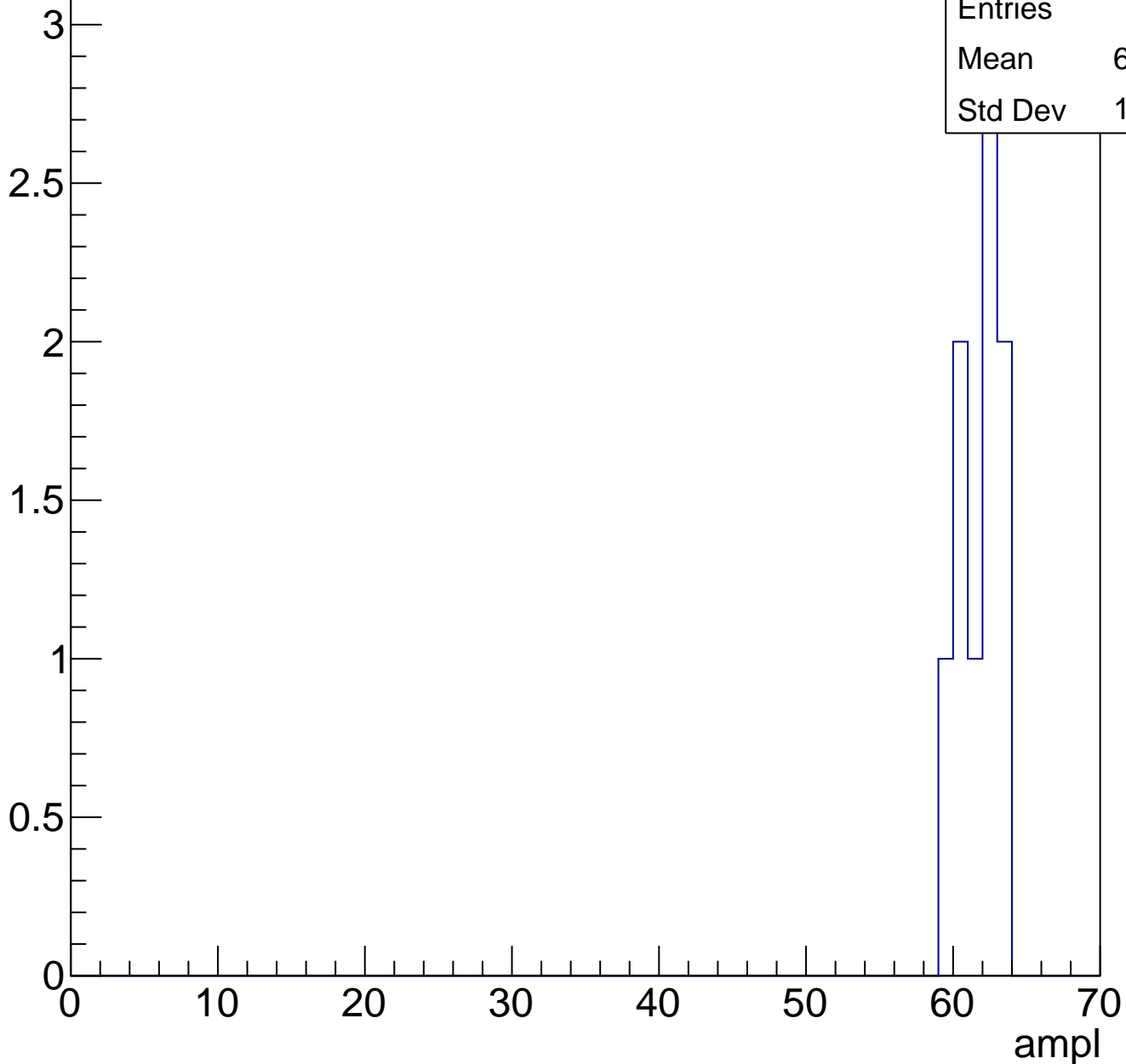
Entries	28
Mean	58.57
Std Dev	11.45



B1L103S, U7-ch5, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch5, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	0
Std Dev	0



B1L103S, U7-ch6, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	65
Mean	26.37
Std Dev	7.454

Gaus mean : 28.3175

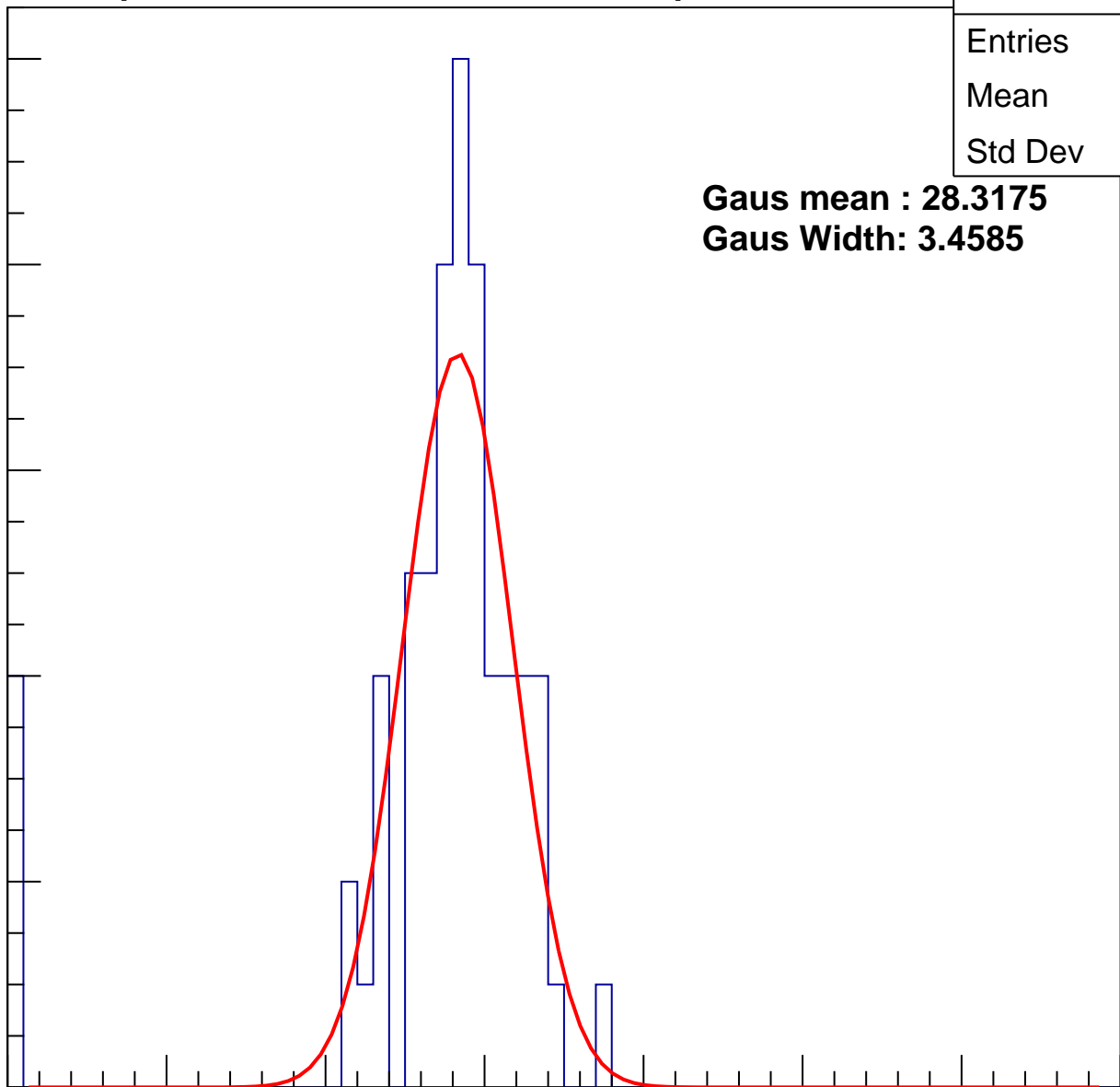
Gaus Width: 3.4585

Entry

10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U7-ch6, adc1

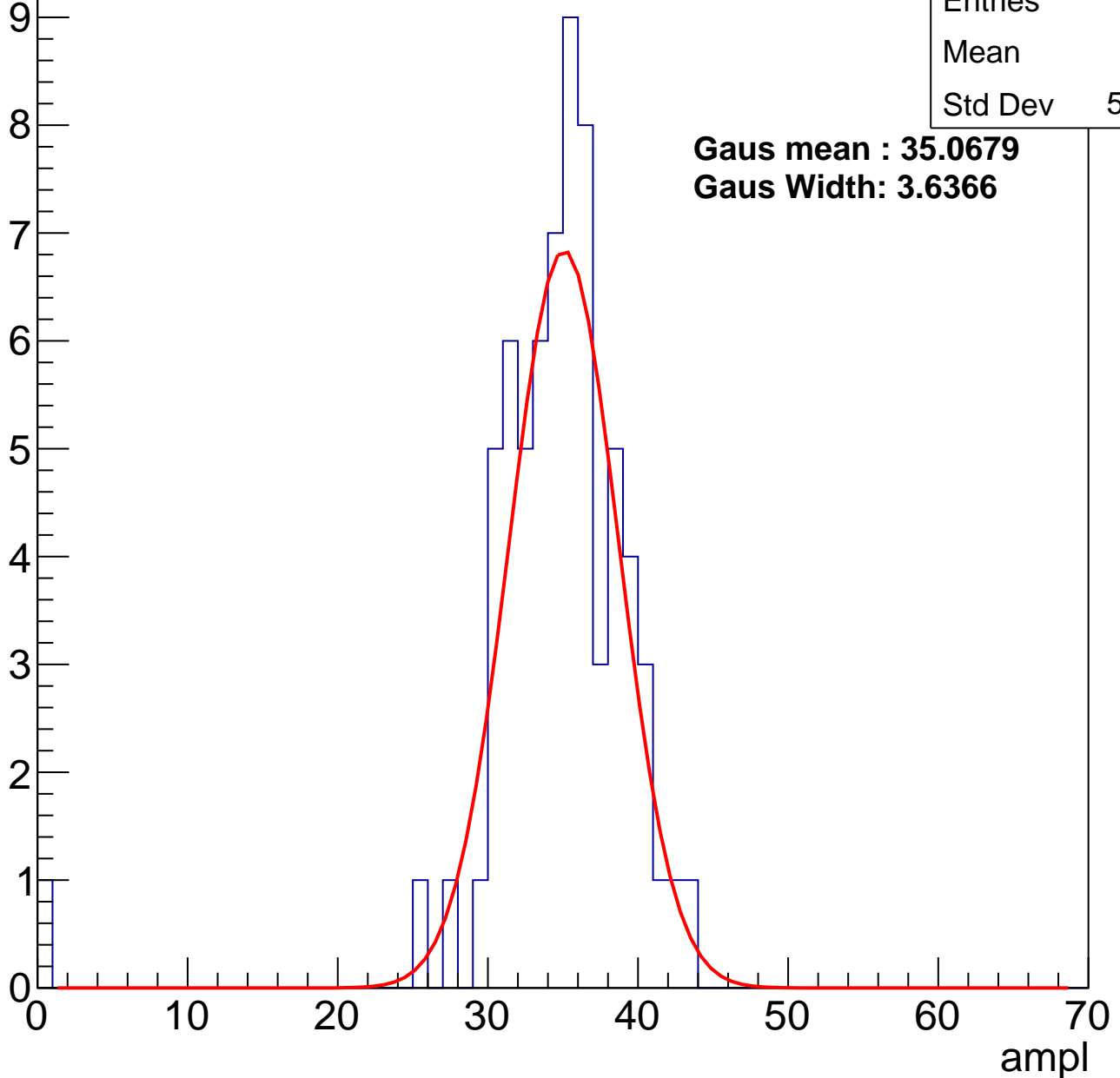
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	34.1
Std Dev	5.451

Gaus mean : 35.0679

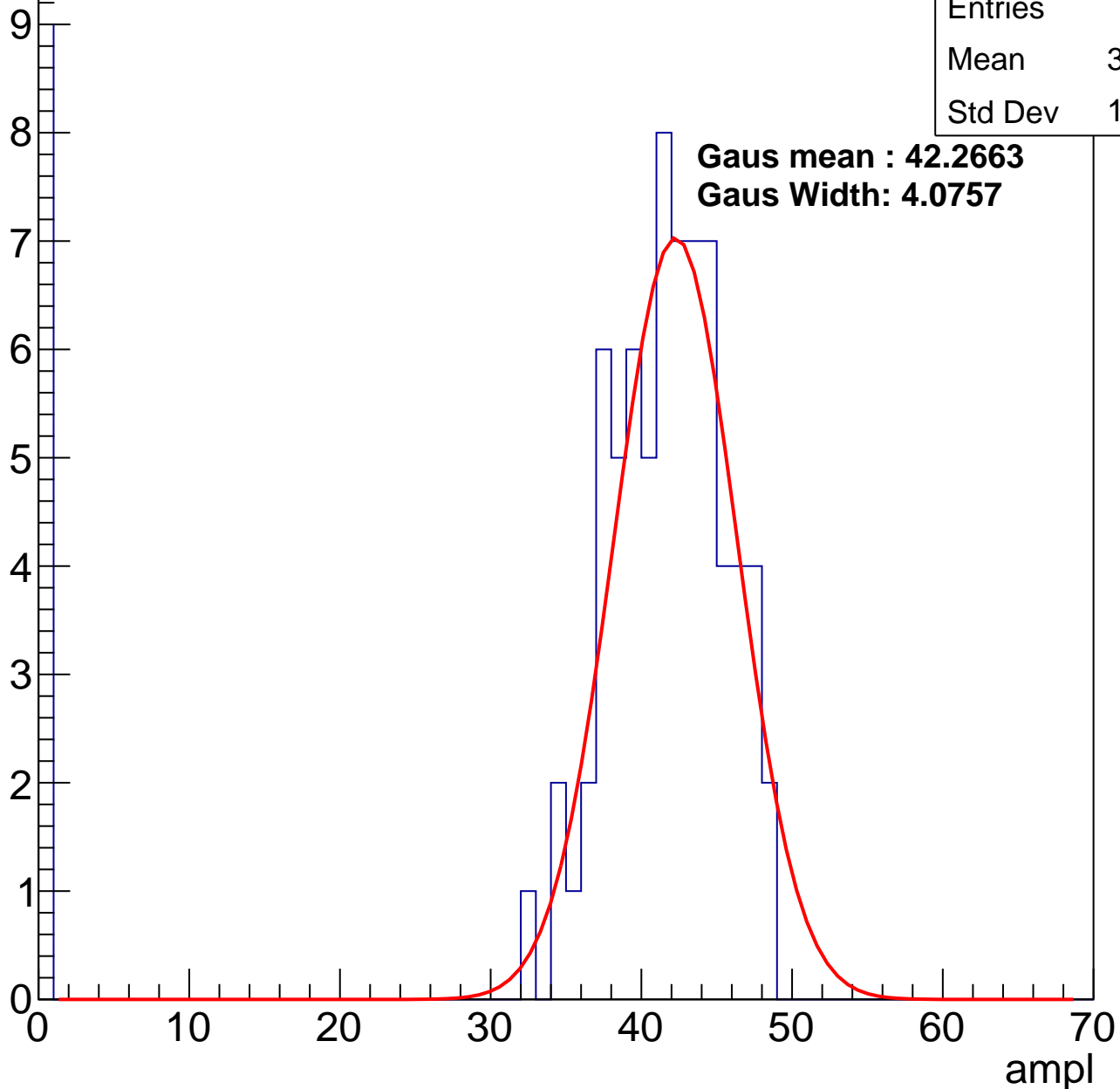
Gaus Width: 3.6366



B1L103S, U7-ch6, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	80
Mean	36.65
Std Dev	13.49

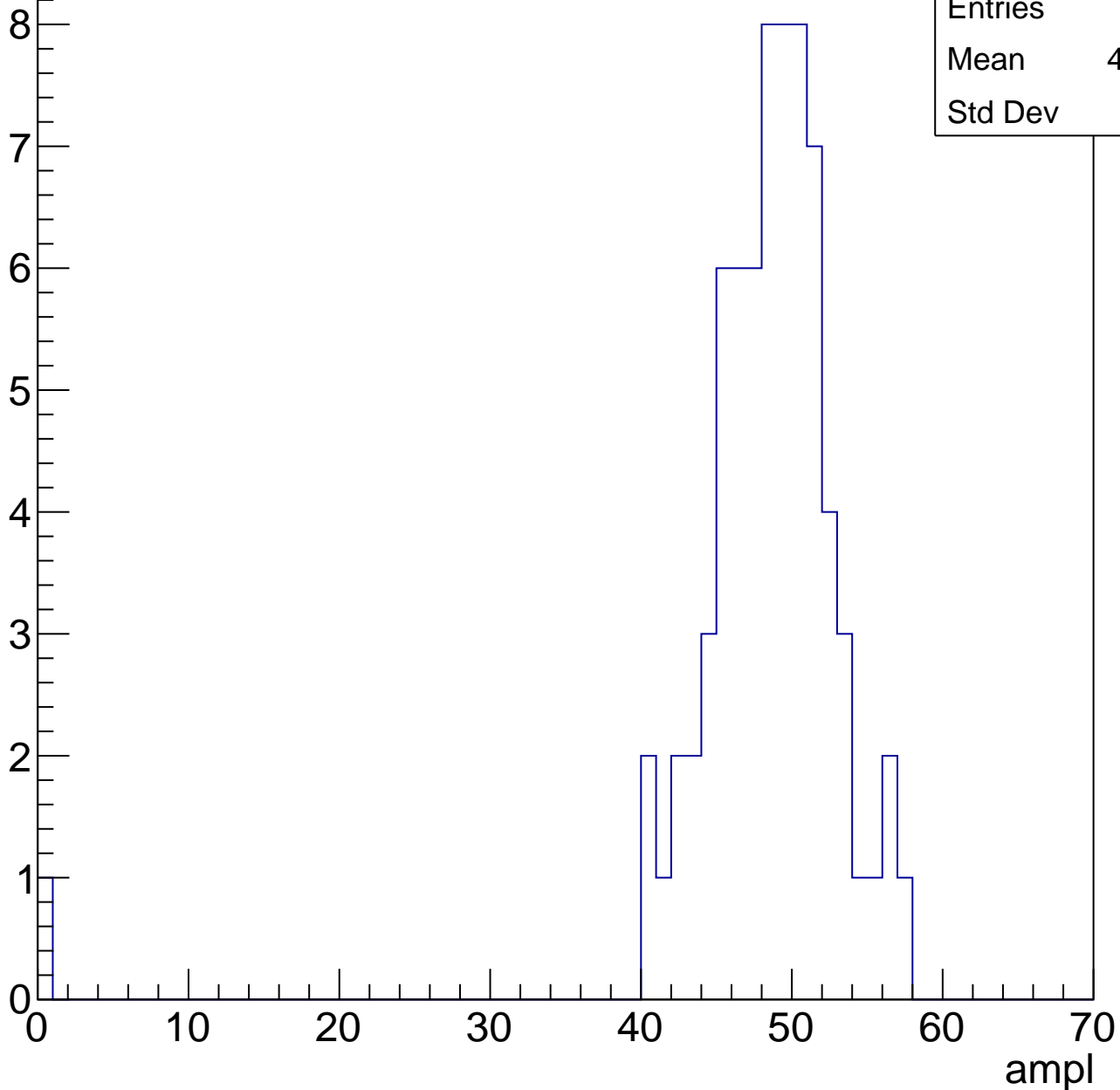
Gaus mean : 42.2663
Gaus Width: 4.0757

B1L103S, U7-ch6, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	47.62
Std Dev	6.73

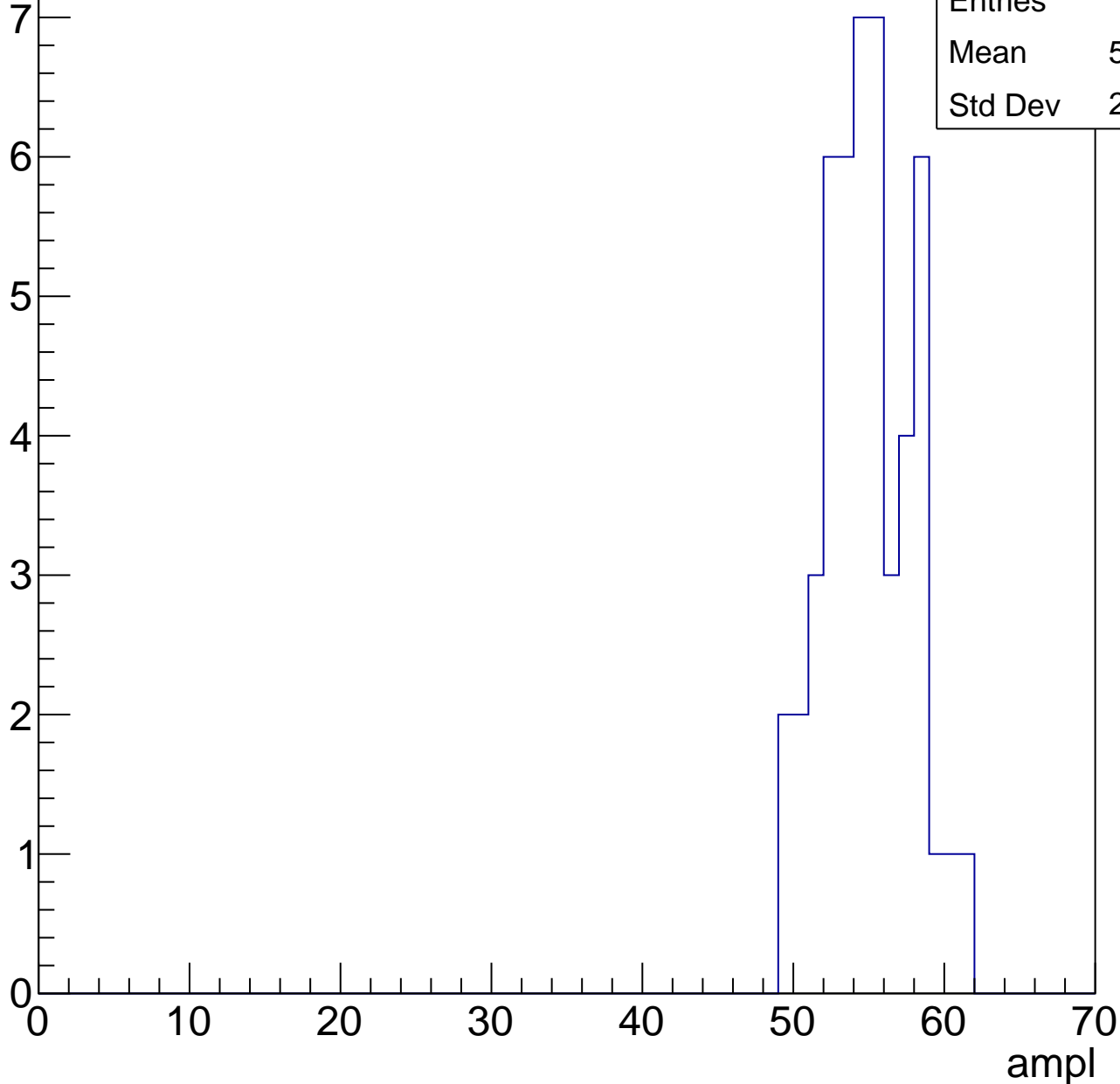


B1L103S, U7-ch6, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

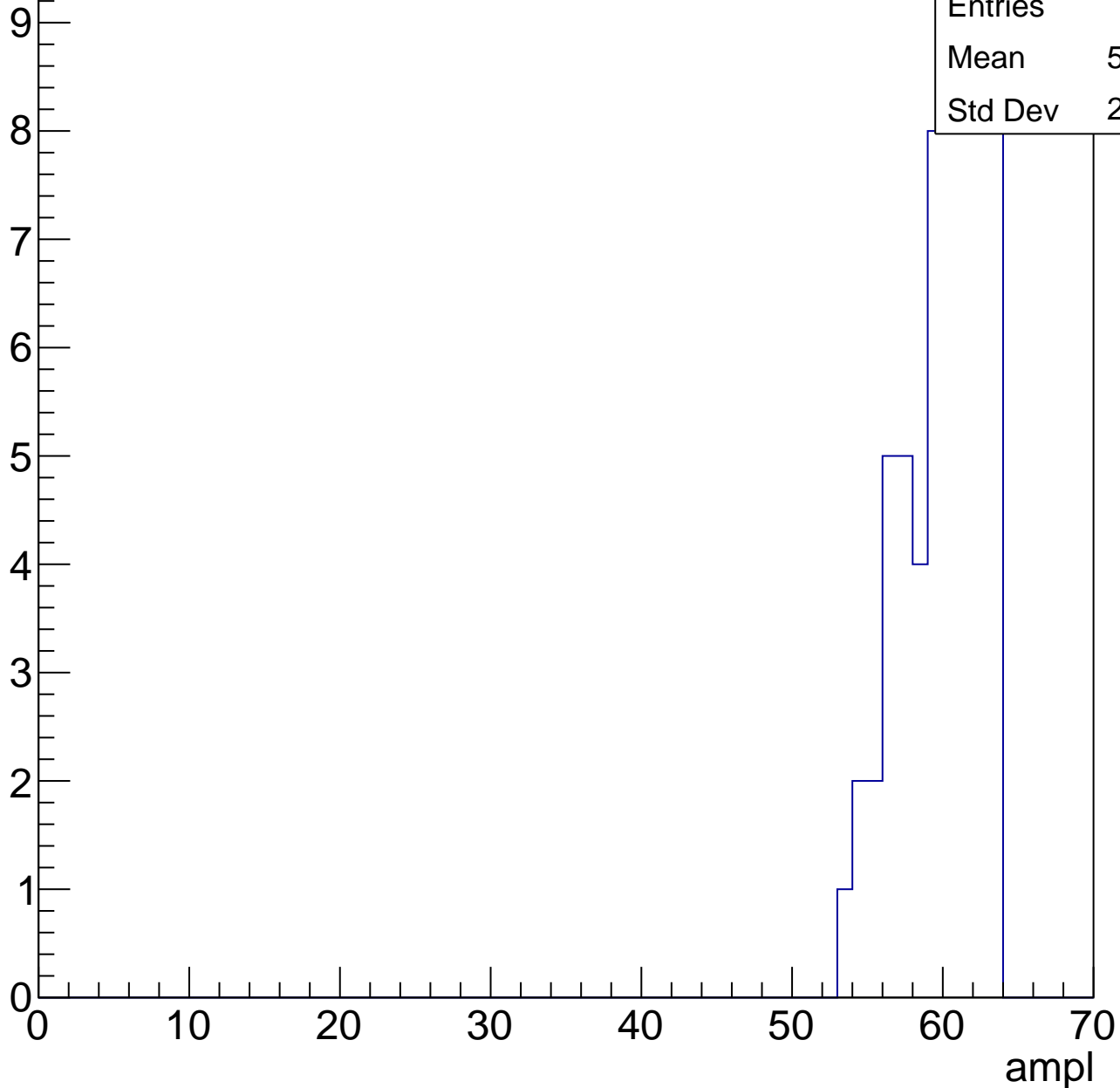
Entries	49
Mean	54.45
Std Dev	2.822



B1L103S, U7-ch6, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	61
Mean	59.52
Std Dev	2.646

B1L103S, U7-ch6, adc6

calib_packv5_041523_1651.root, FC#0, port C2

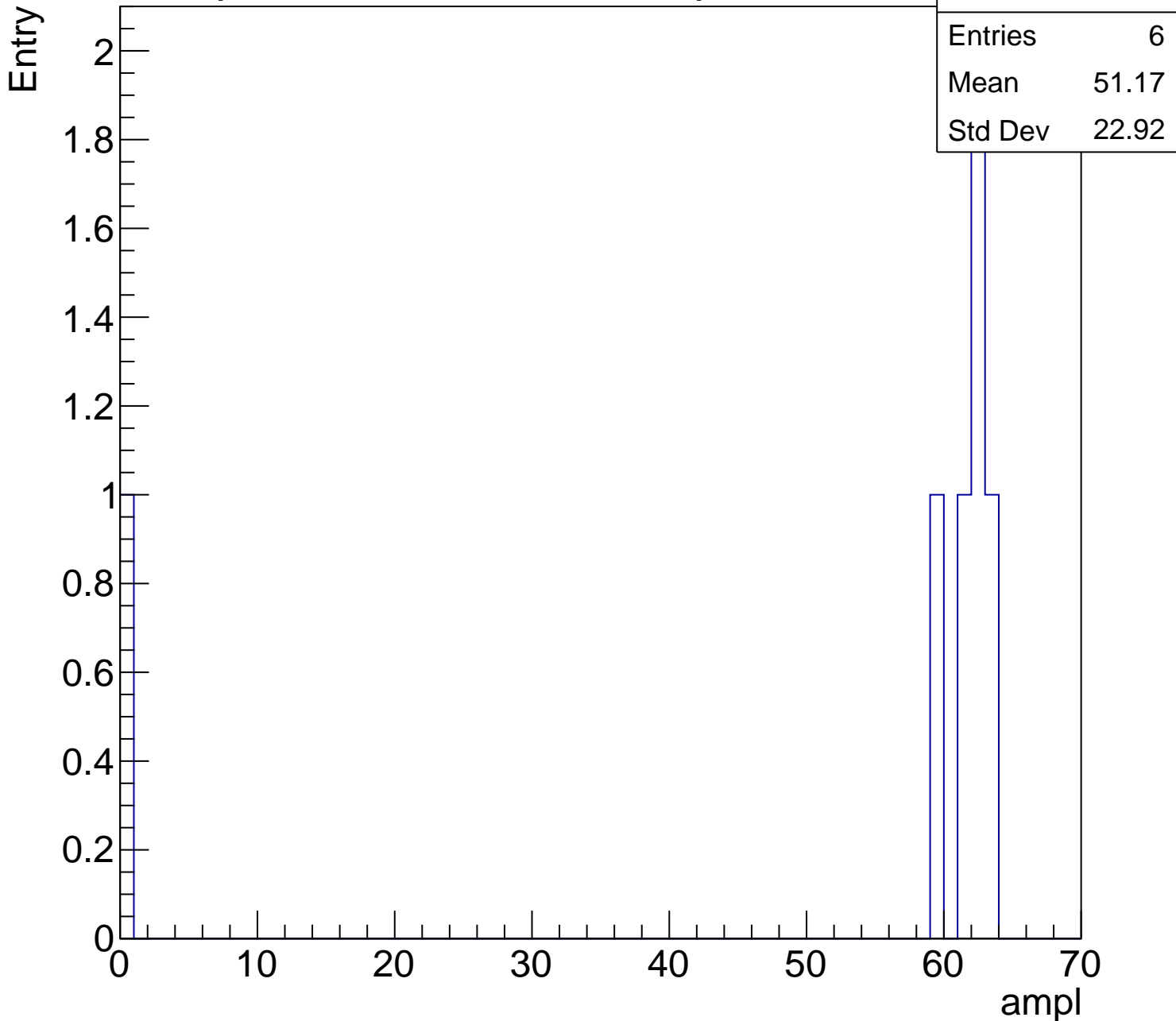
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	6
Mean	51.17
Std Dev	22.92

0 10 20 30 40 50 60 70

ampl



B1L103S, U7-ch6, adc7

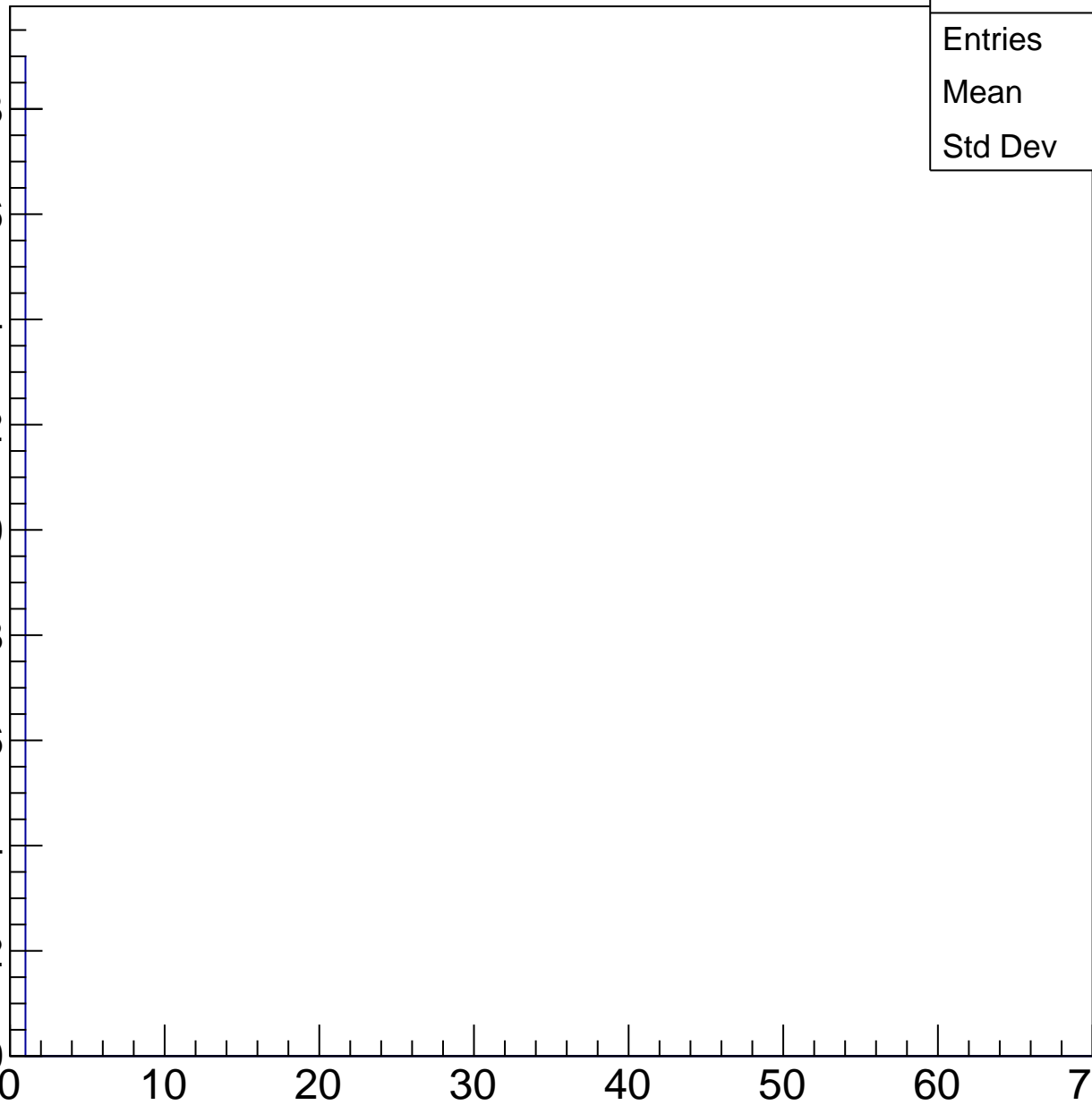
calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl



B1L103S, U7-ch7, adc0

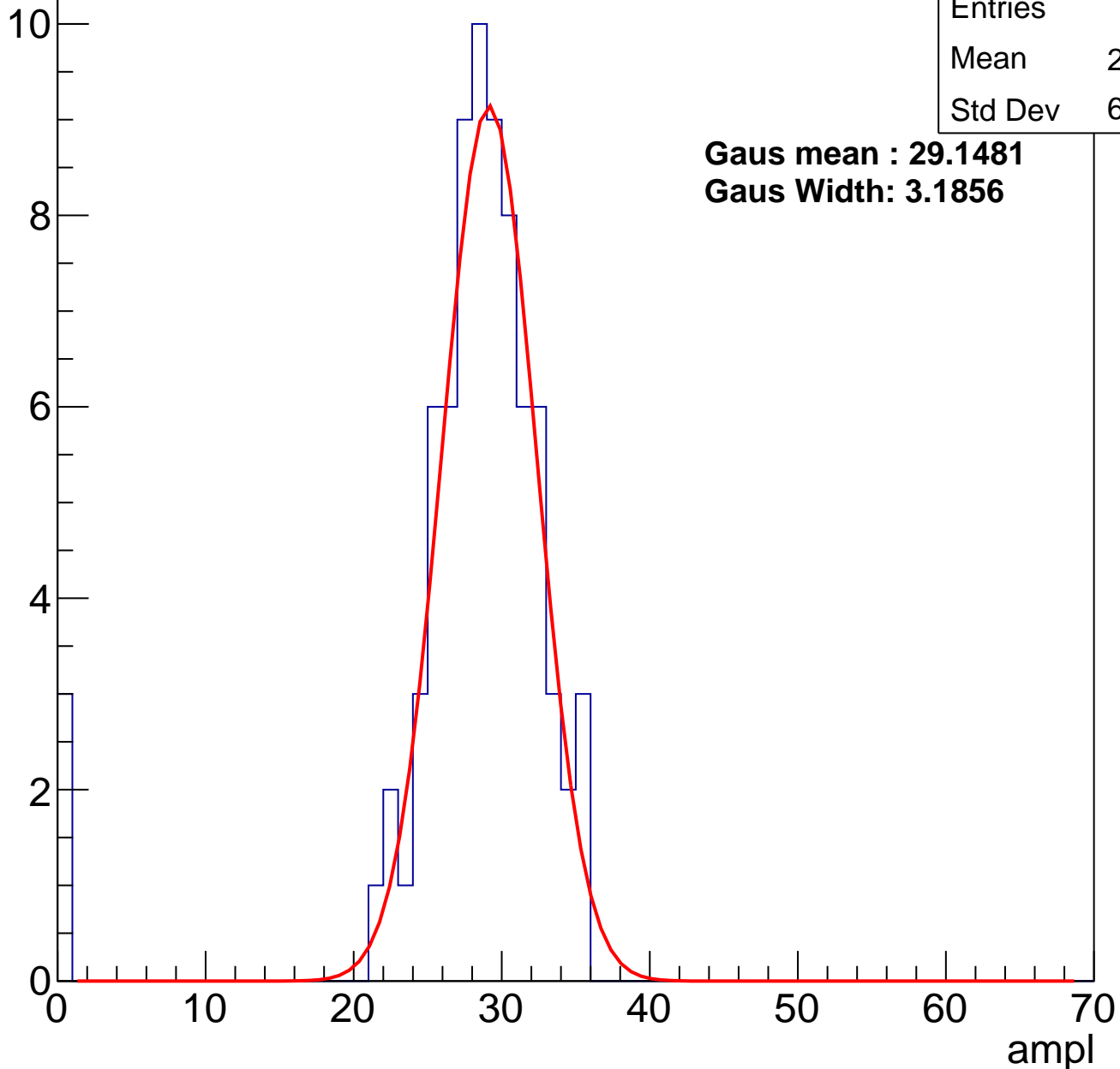
calib_packv5_041523_1651.root, FC#0, port C2

Entries	78
Mean	27.44
Std Dev	6.297

Gaus mean : 29.1481

Gaus Width: 3.1856

Entry



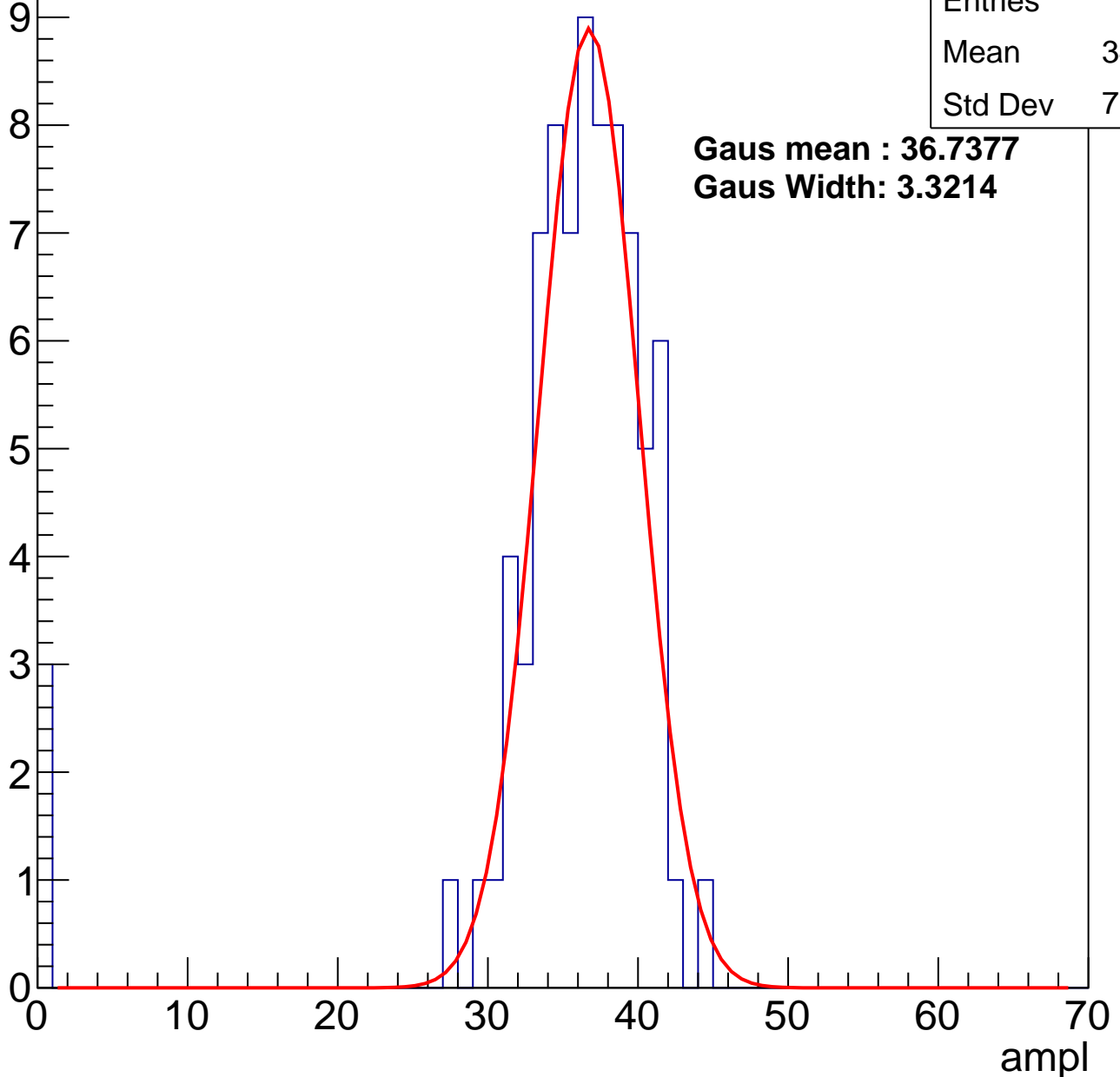
B1L103S, U7-ch7, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	80
Mean	34.79
Std Dev	7.599

Gaus mean : 36.7377
Gaus Width: 3.3214



B1L103S, U7-ch7, adc2

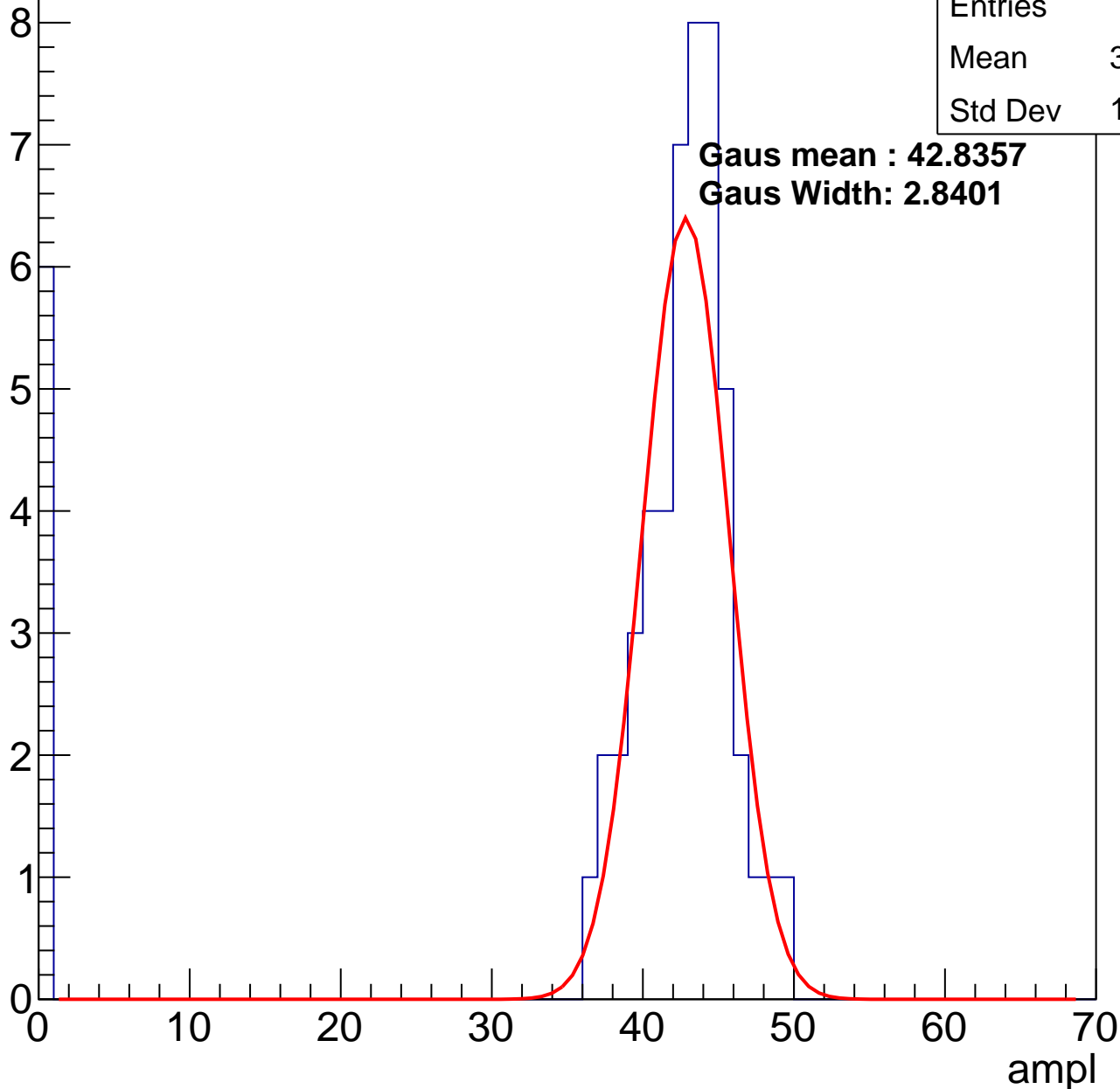
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	37.78
Std Dev	13.48

Gaus mean : 42.8357

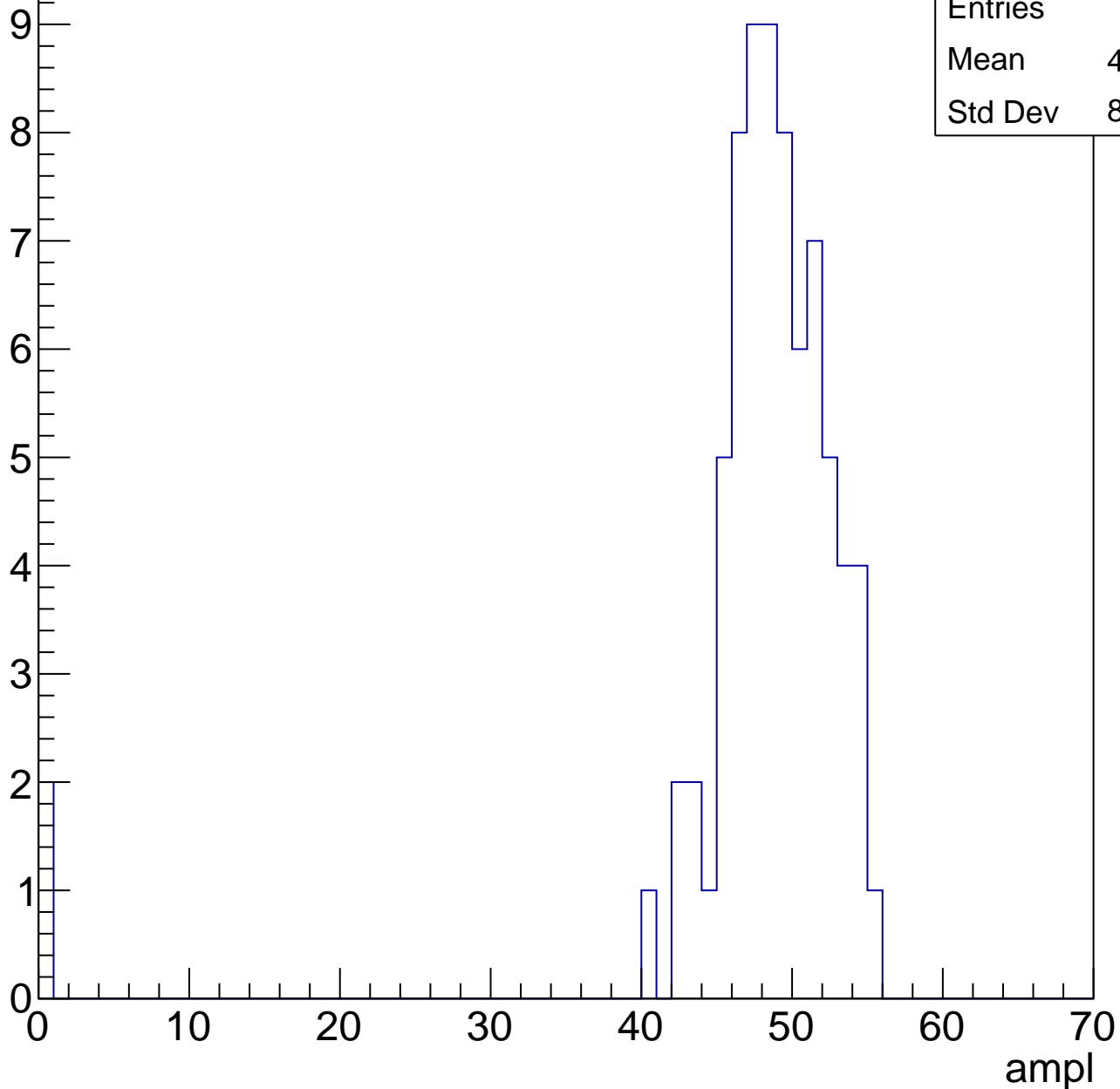
Gaus Width: 2.8401



B1L103S, U7-ch7, adc3

calib_packv5_041523_1651.root, FC#0, port C2

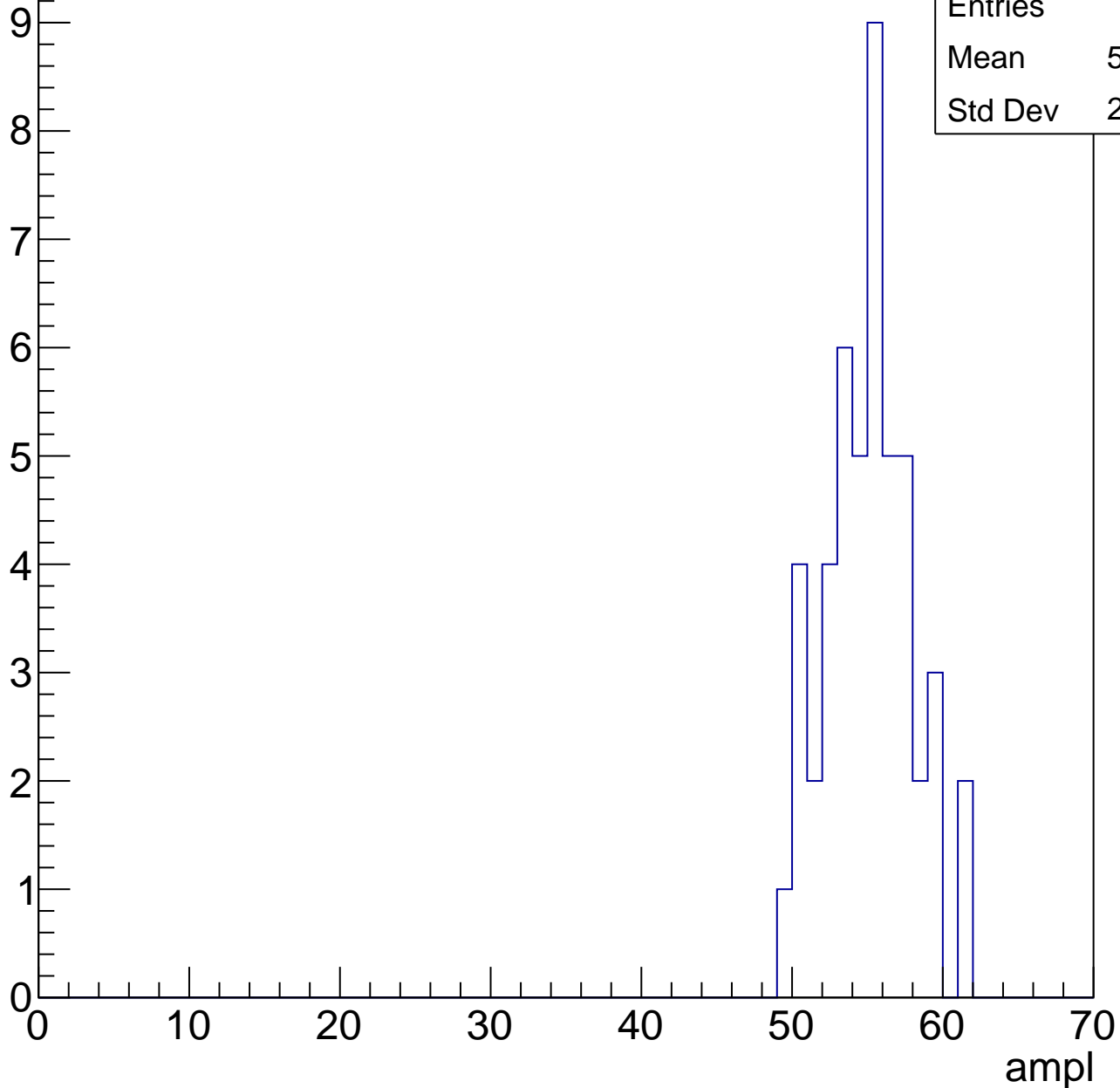
Entry



B1L103S, U7-ch7, adc4

calib_packv5_041523_1651.root, FC#0, port C2

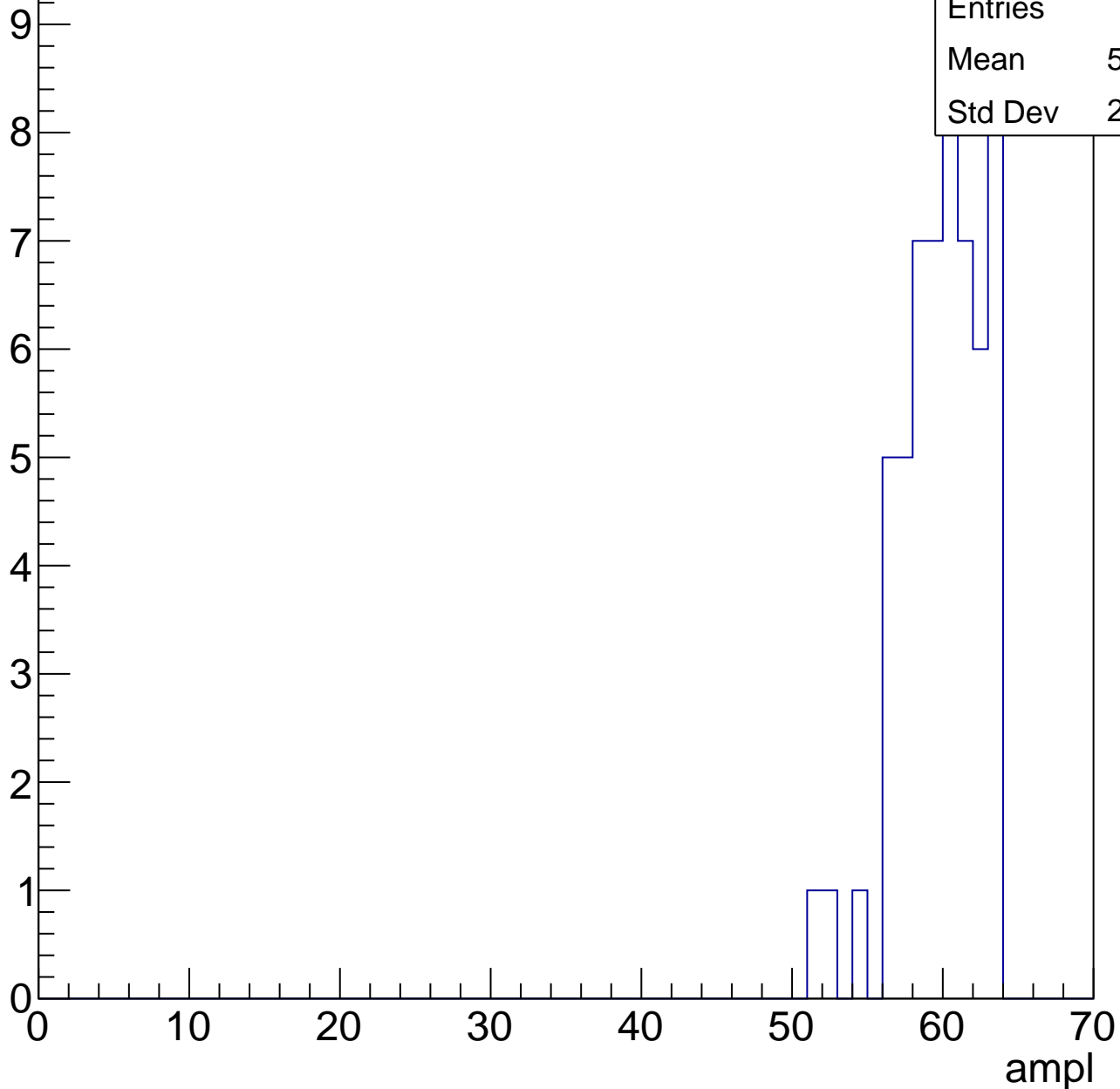
Entry



B1L103S, U7-ch7, adc5

calib_packv5_041523_1651.root, FC#0, port C2

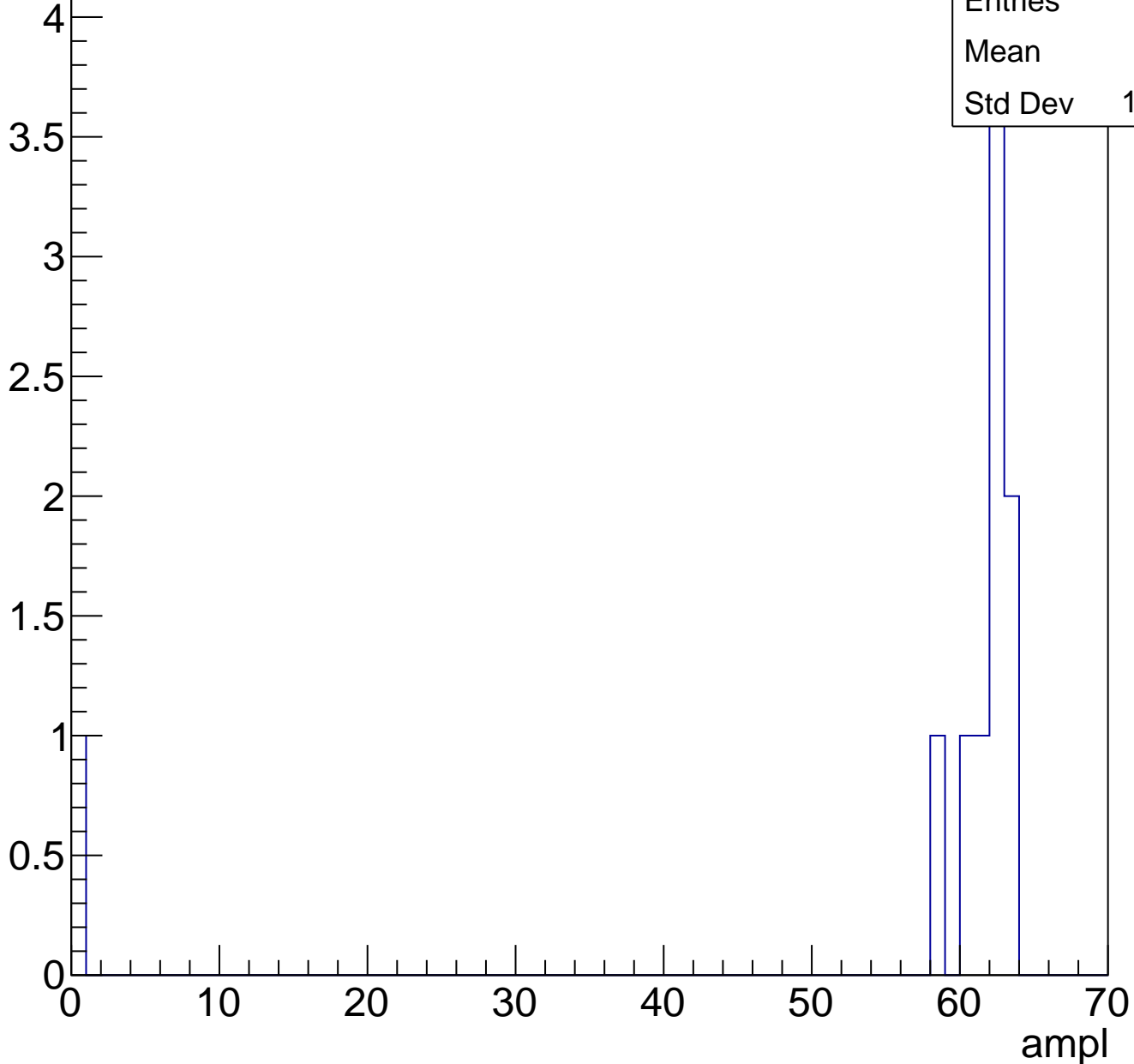
Entry



B1L103S, U7-ch7, adc6

calib_packv5_041523_1651.root, FC#0, port C2

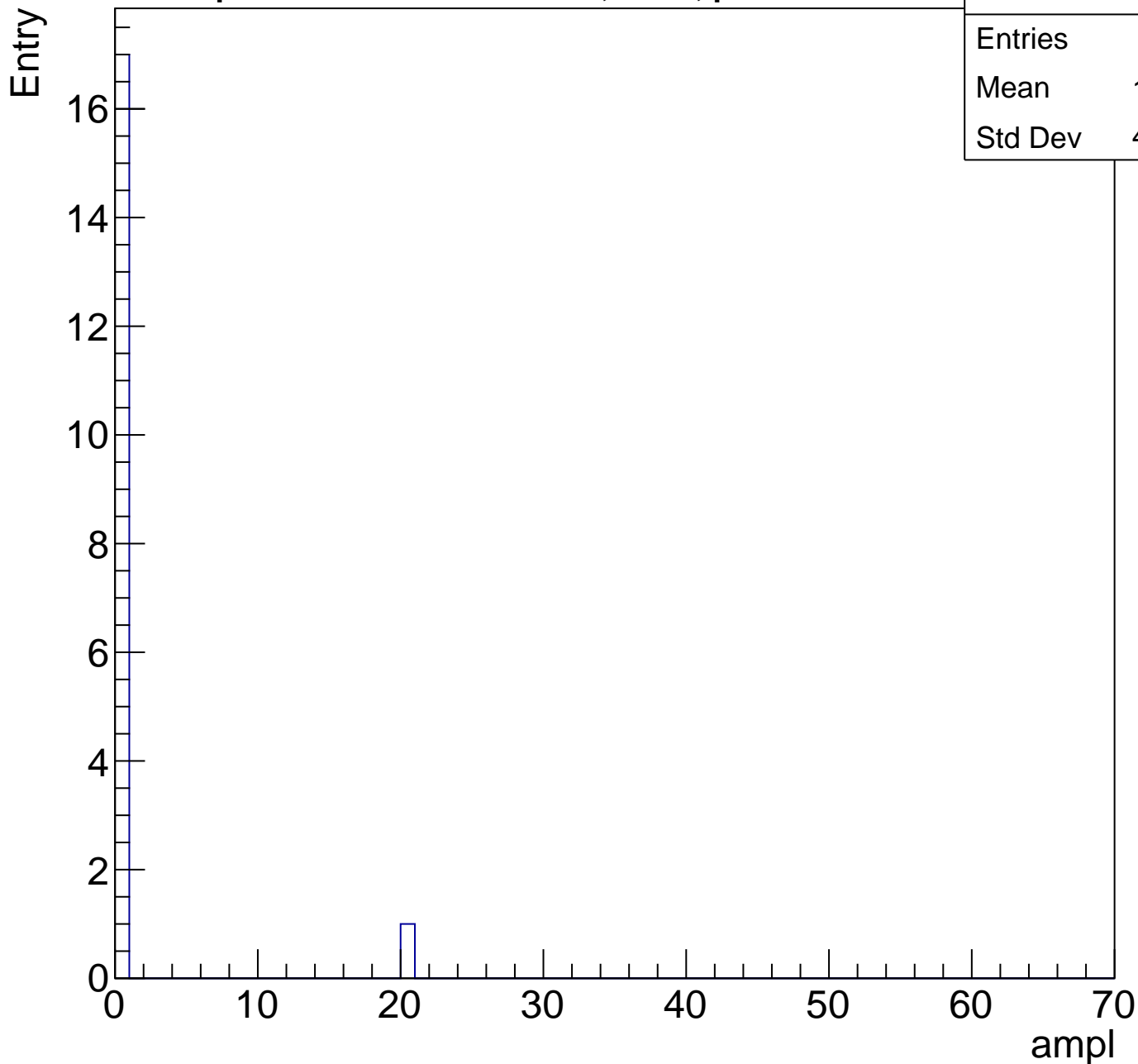
Entry



B1L103S, U7-ch7, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	18
Mean	1.111
Std Dev	4.581



B1L103S, U7-ch8, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	94
Mean	25.28
Std Dev	8.879

Gaus mean : 28.4573
Gaus Width: 3.8281

Entry

10

8

6

4

2

0

0

10

20

30

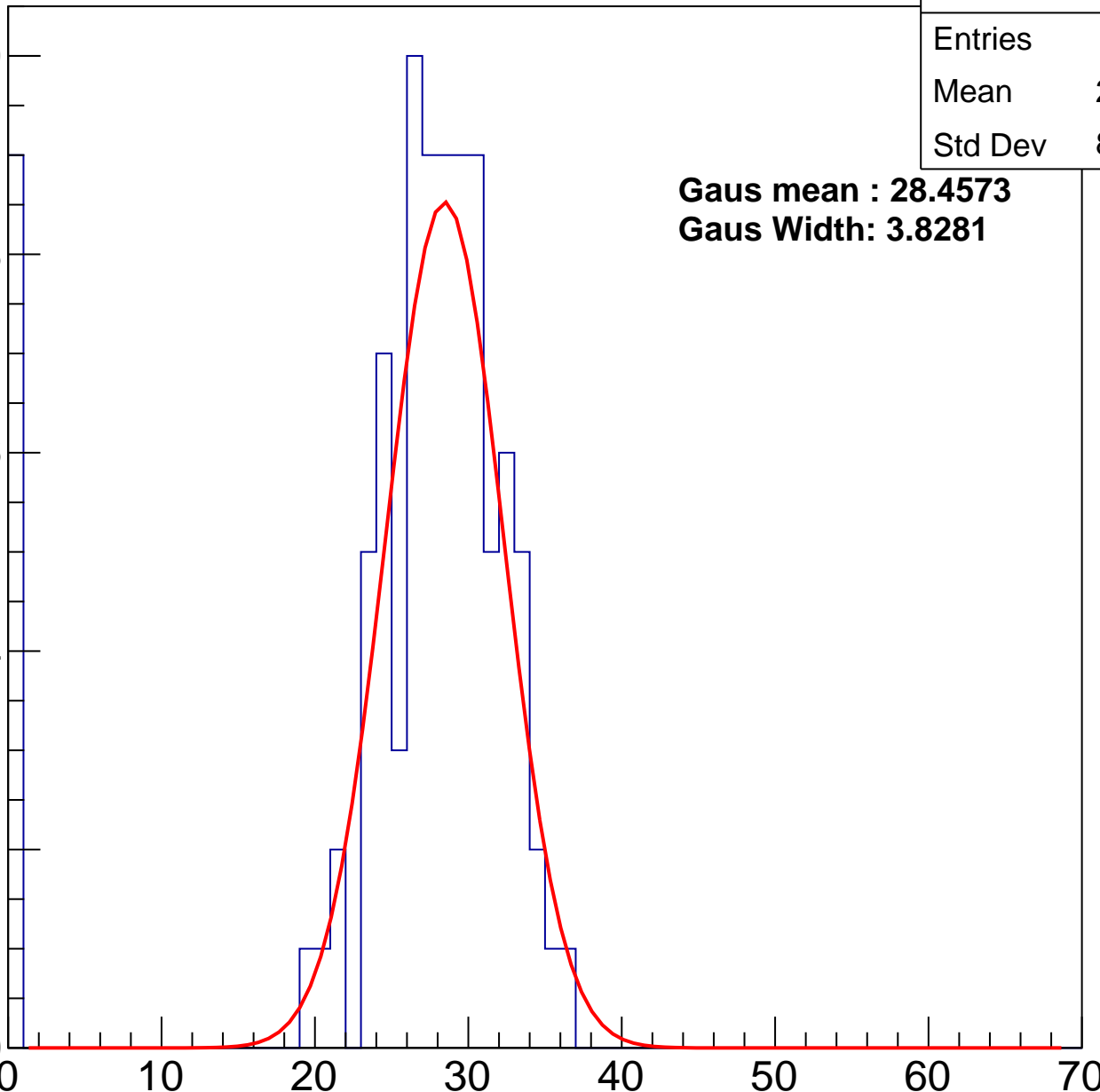
40

50

60

70

ampl



B1L103S, U7-ch8, adc1

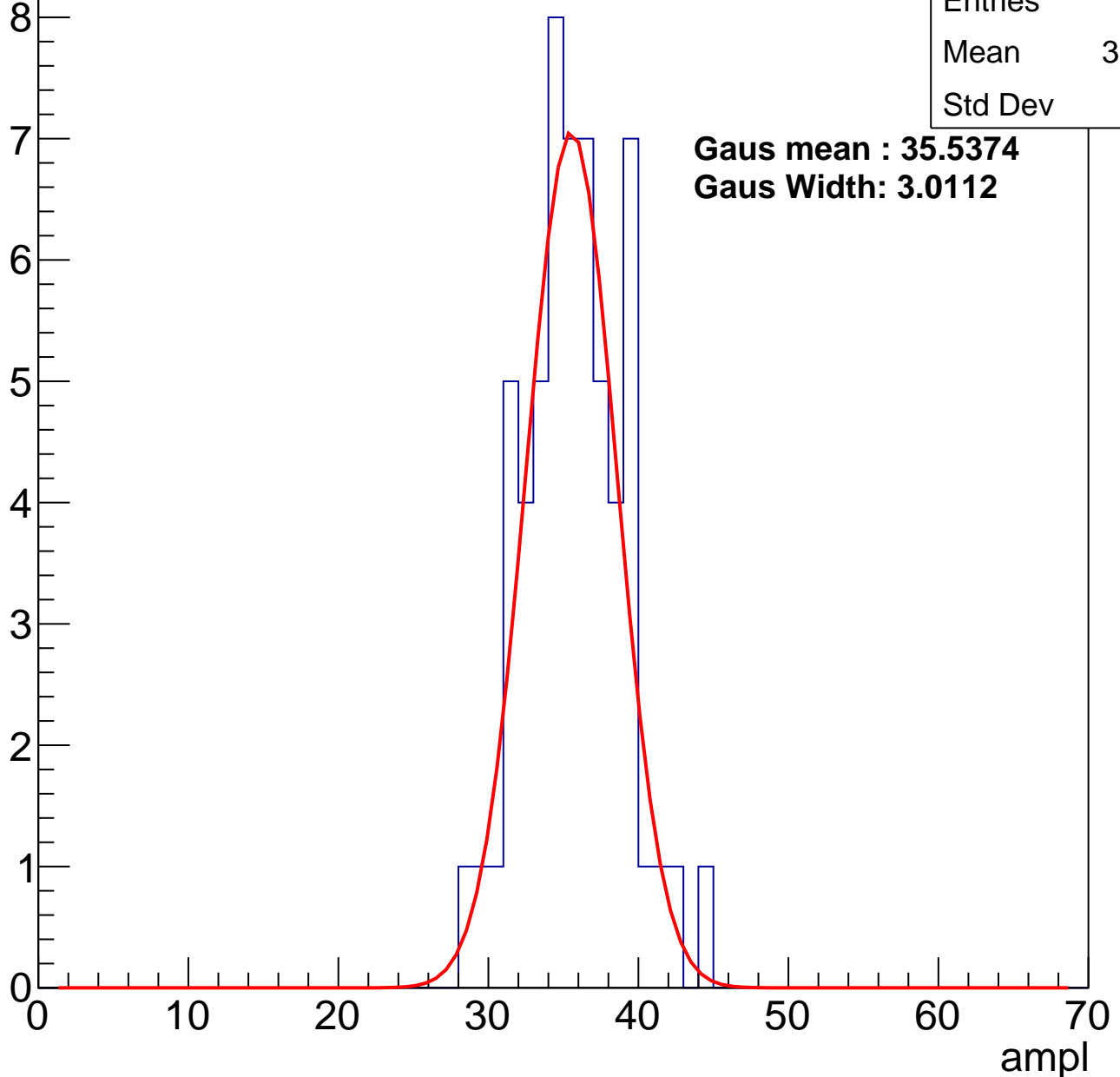
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	35.27
Std Dev	3.23

Gaus mean : 35.5374

Gaus Width: 3.0112



B1L103S, U7-ch8, adc2

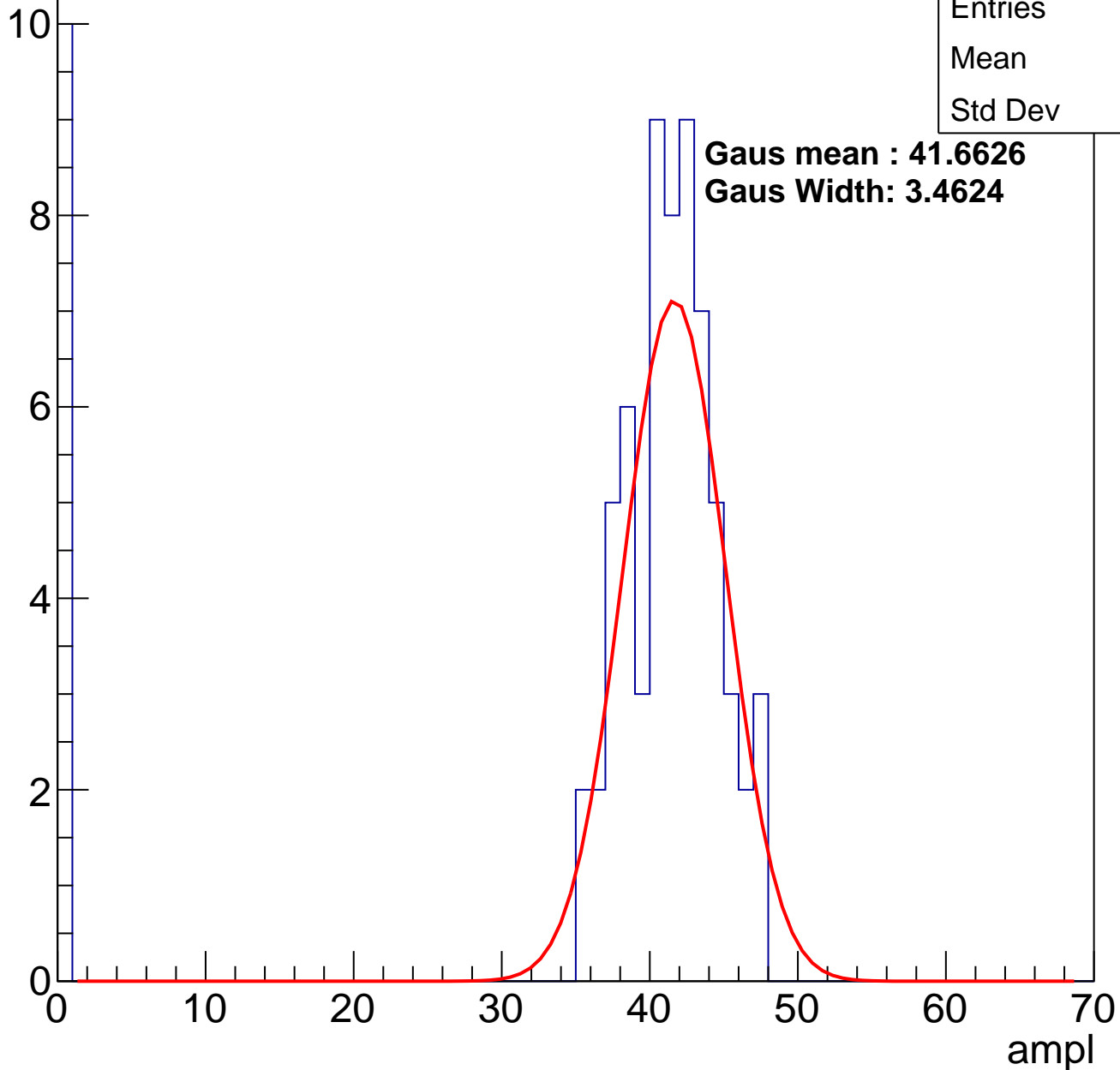
calib_packv5_041523_1651.root, FC#0, port C2

Entries	74
Mean	35.5
Std Dev	14.3

Gaus mean : 41.6626

Gaus Width: 3.4624

Entry

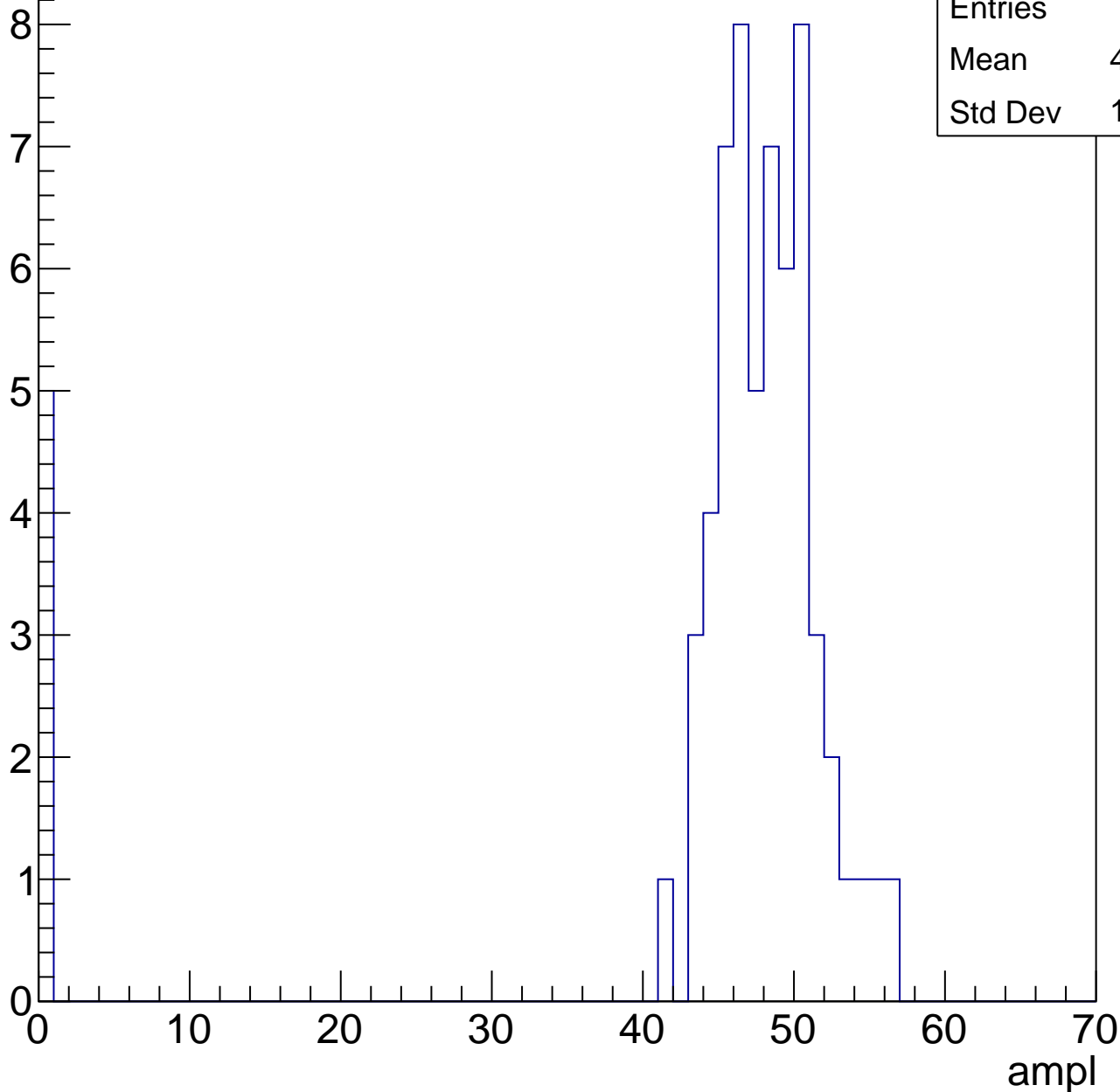


B1L103S, U7-ch8, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	43.95
Std Dev	13.24

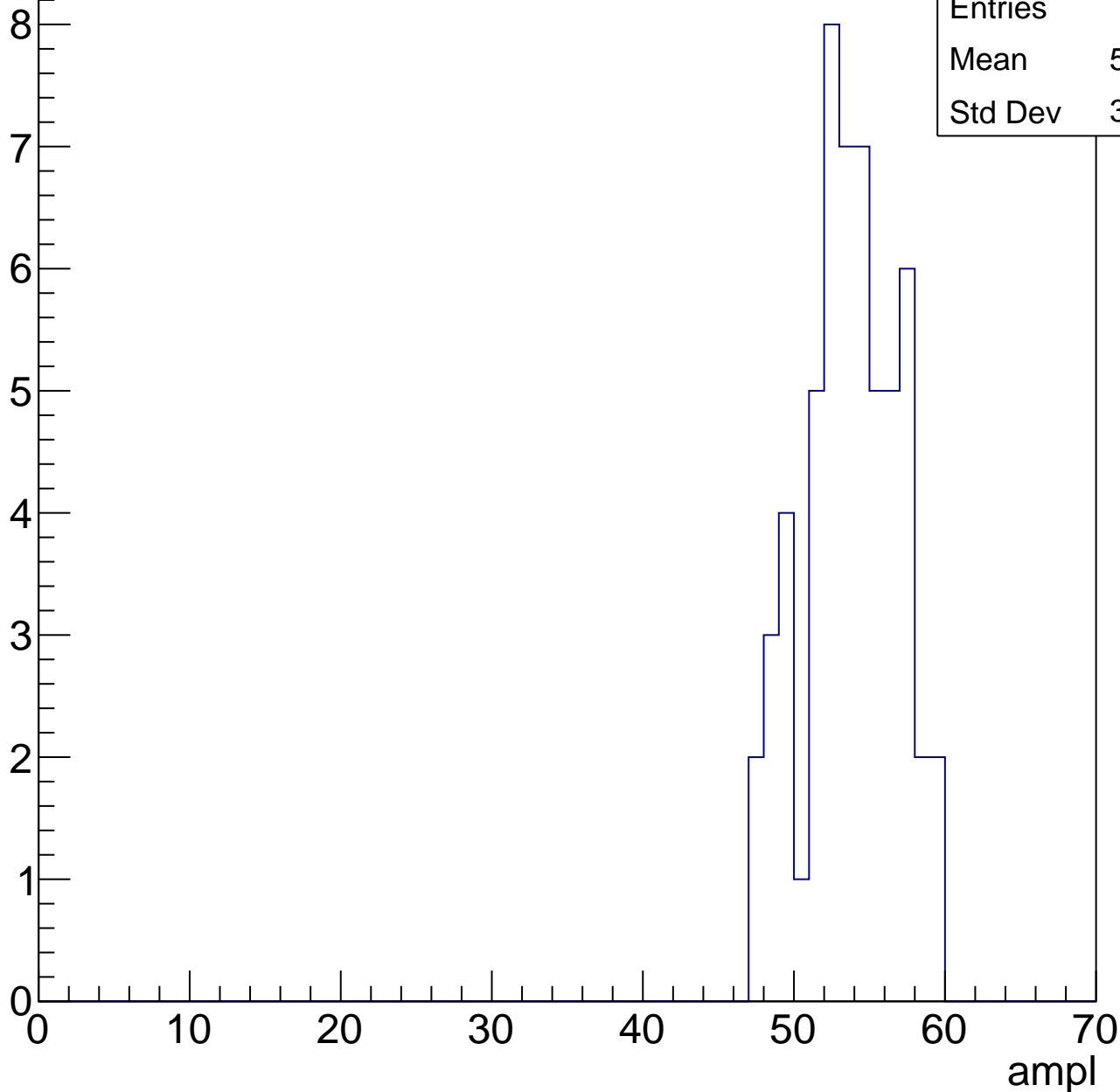


B1L103S, U7-ch8, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	53.25
Std Dev	3.062

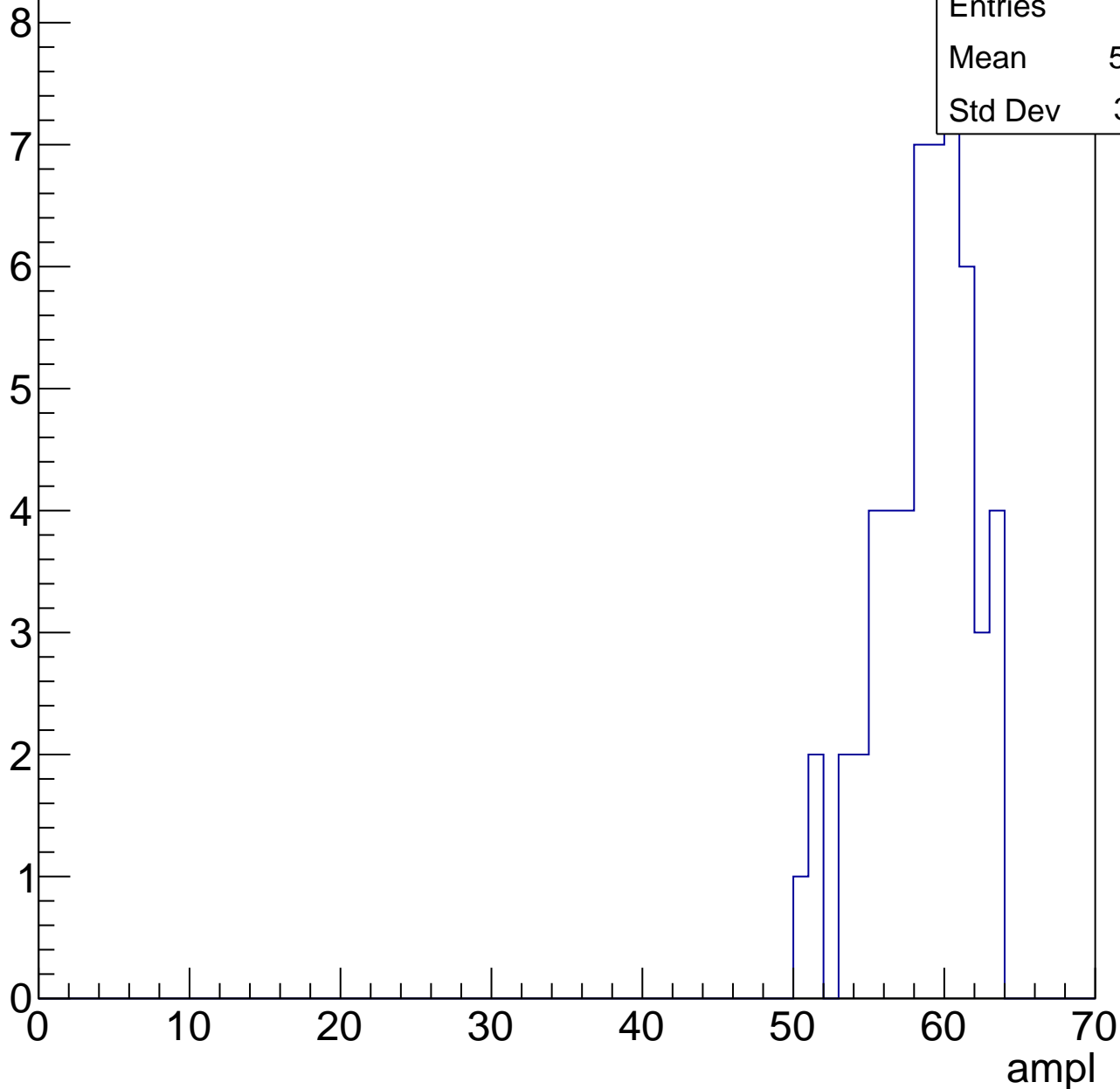


B1L103S, U7-ch8, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	58.17
Std Dev	3.161

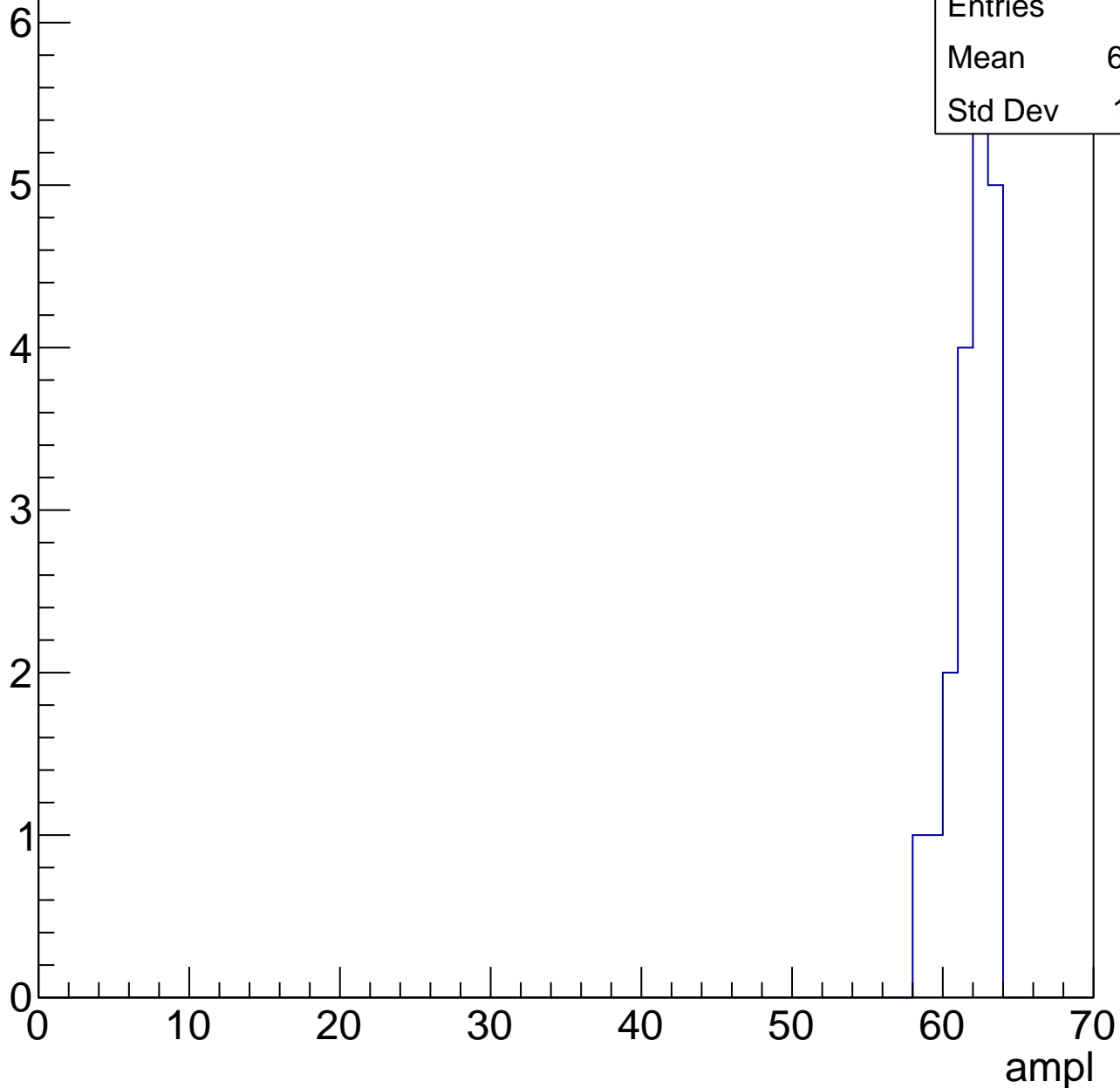


B1L103S, U7-ch8, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

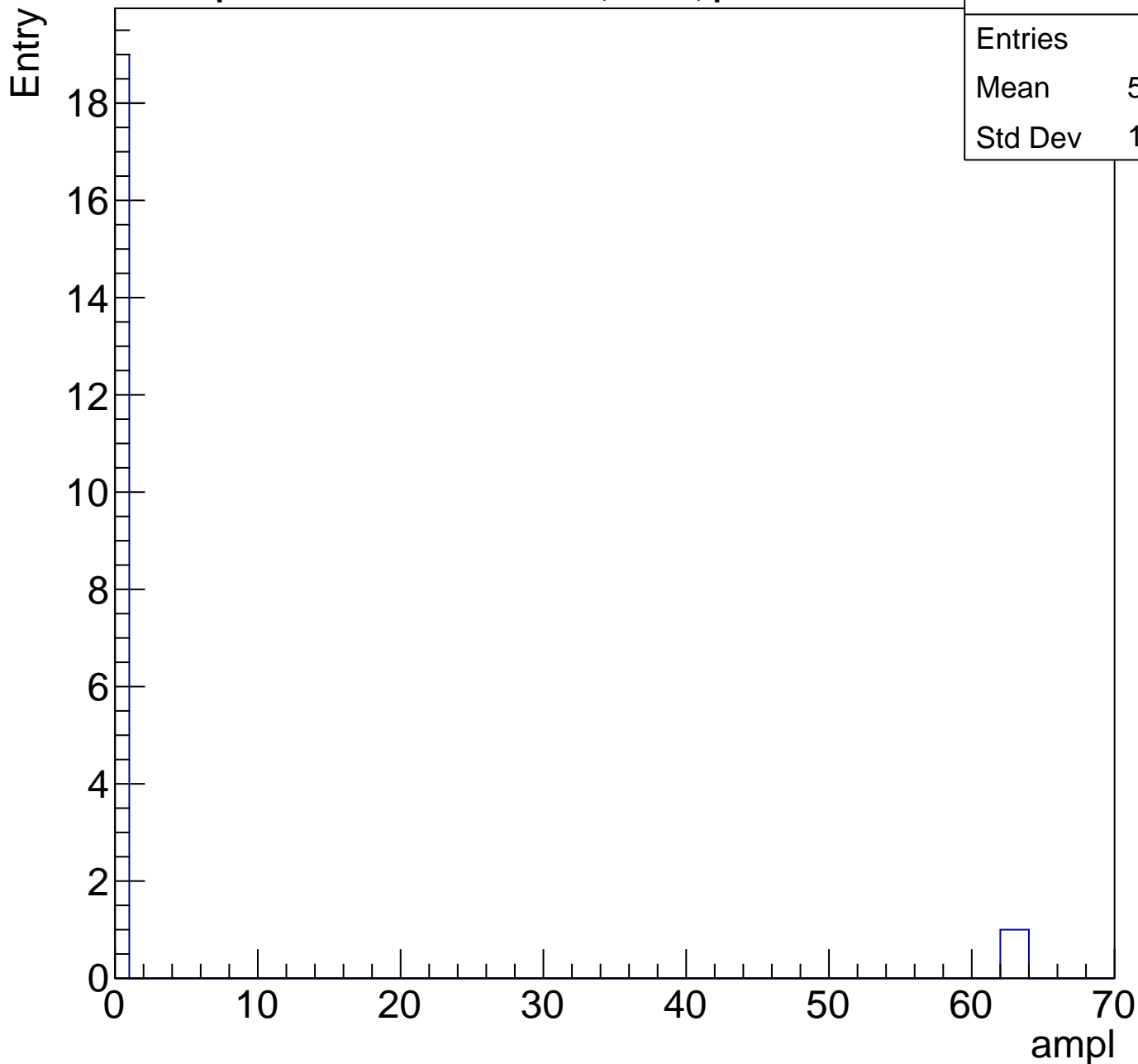
Entries	19
Mean	61.47
Std Dev	1.391



B1L103S, U7-ch8, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	5.952
Std Dev	18.35



B1L103S, U7-ch9, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	85
Mean	28.02
Std Dev	7.926

Gaus mean : 30.5197

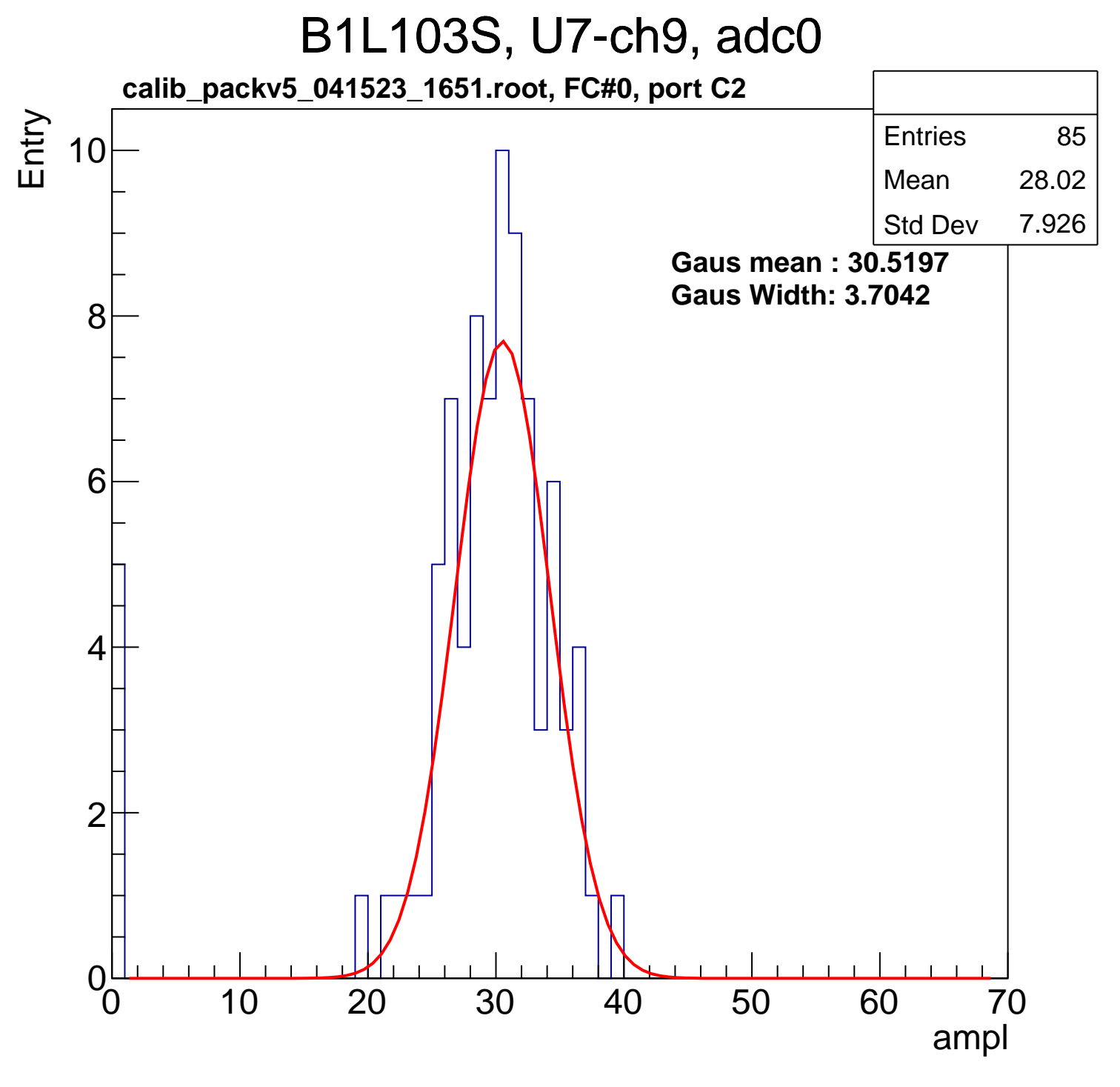
Gaus Width: 3.7042

Entry

10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U7-ch9, adc1

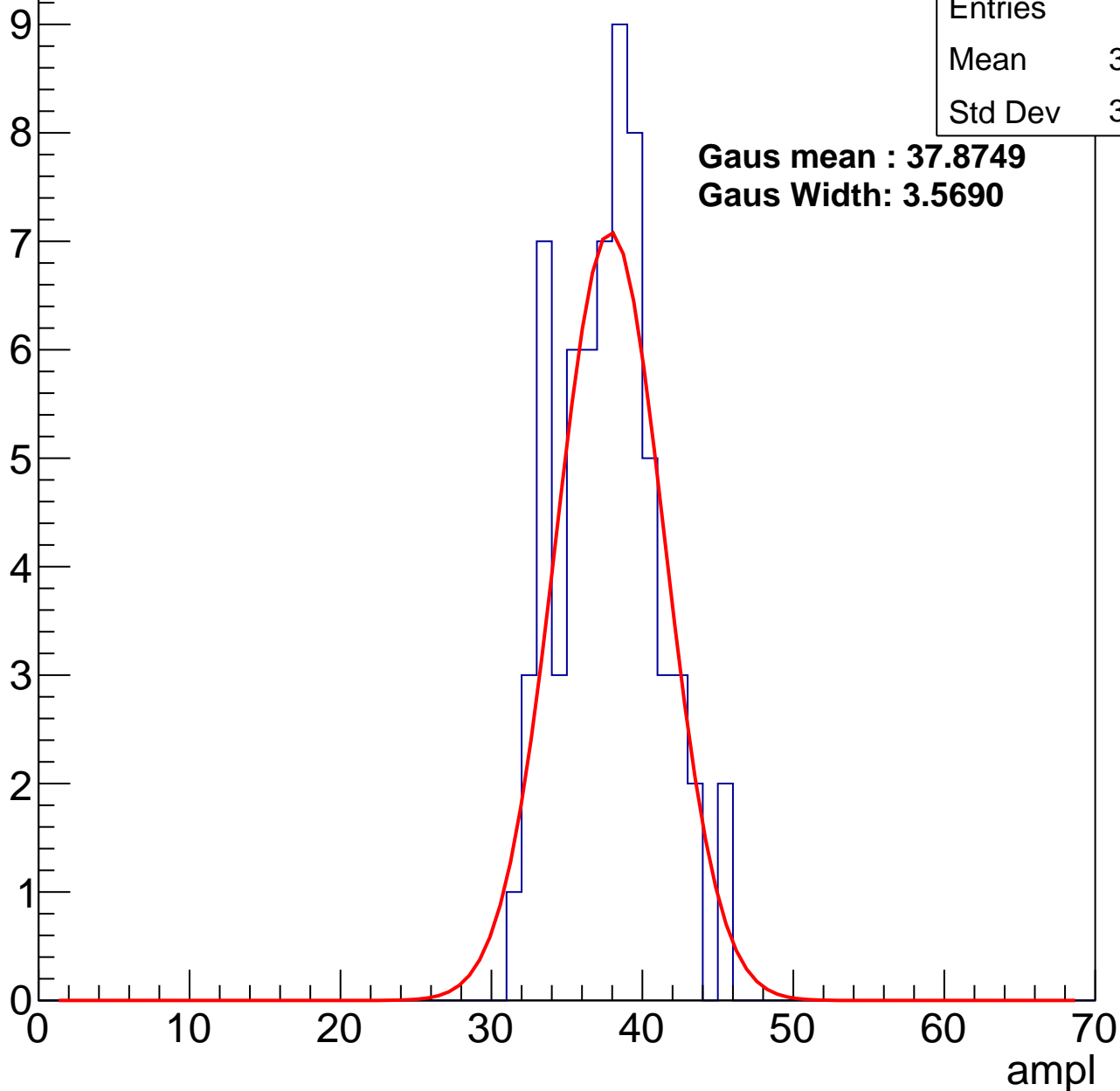
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	37.29
Std Dev	3.243

Gaus mean : 37.8749

Gaus Width: 3.5690



B1L103S, U7-ch9, adc2

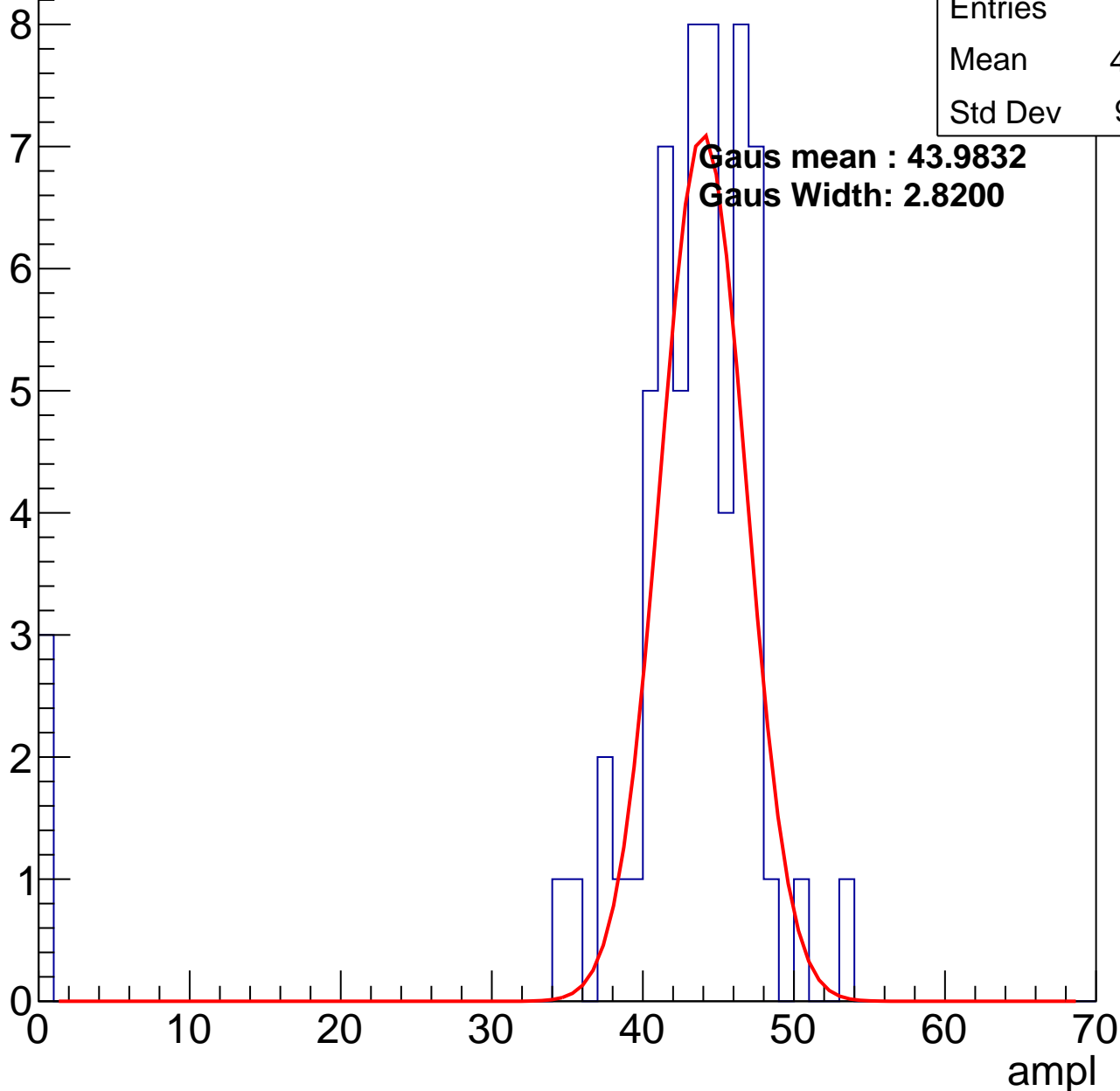
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	41.27
Std Dev	9.741

Gaus mean : 43.9832

Gaus Width: 2.8200

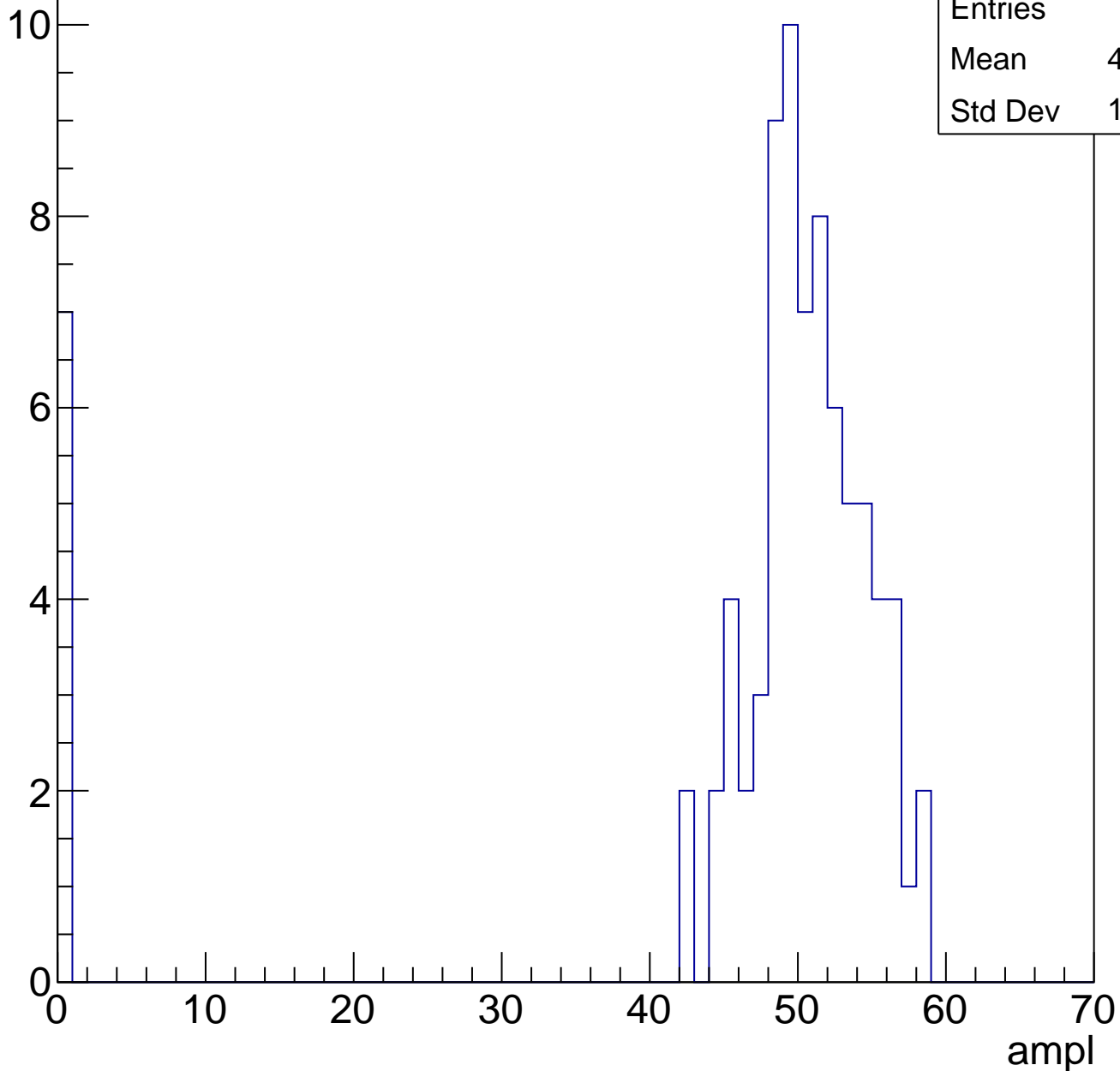


B1L103S, U7-ch9, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	46.04
Std Dev	14.58

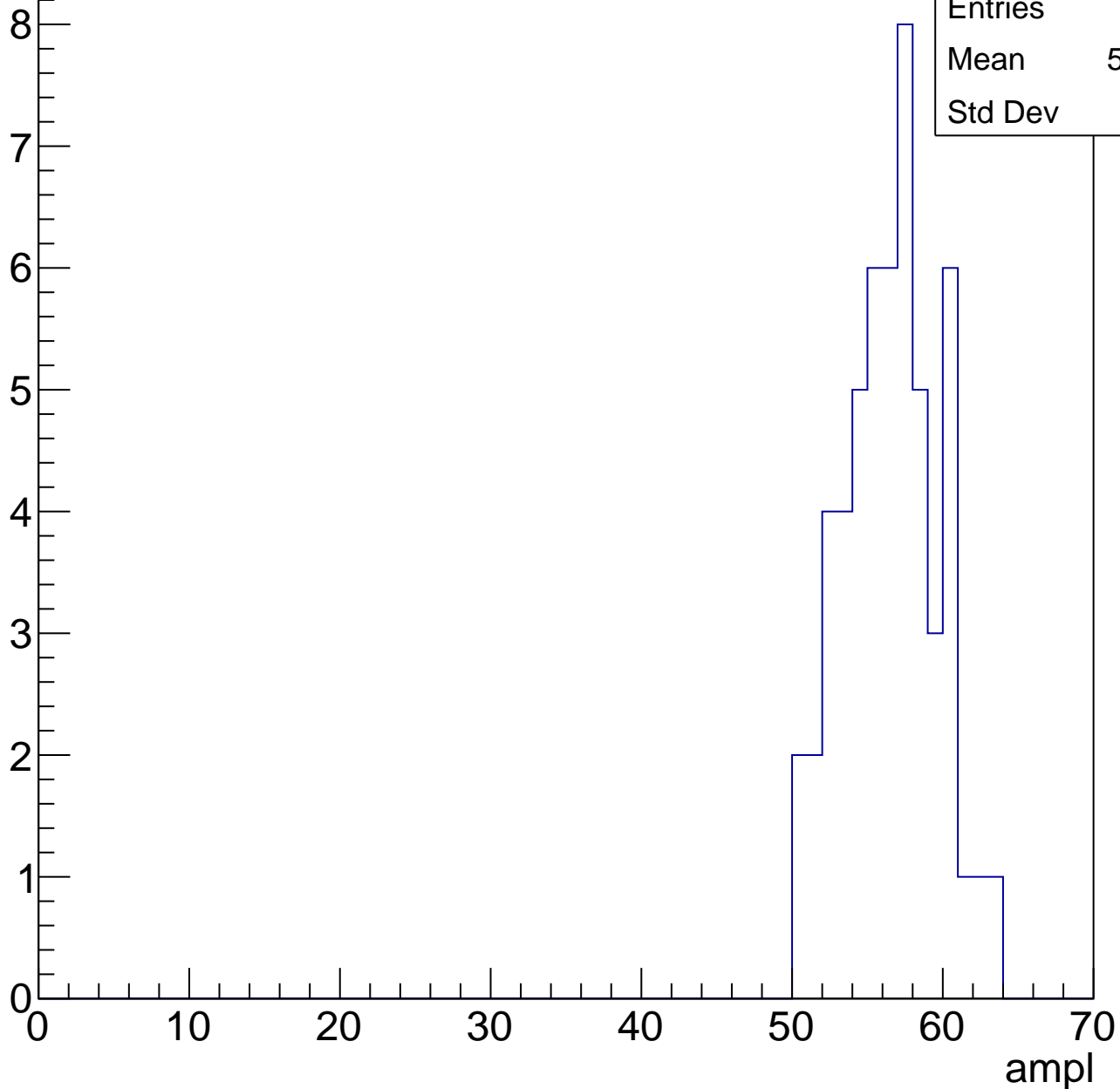
Entry



B1L103S, U7-ch9, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



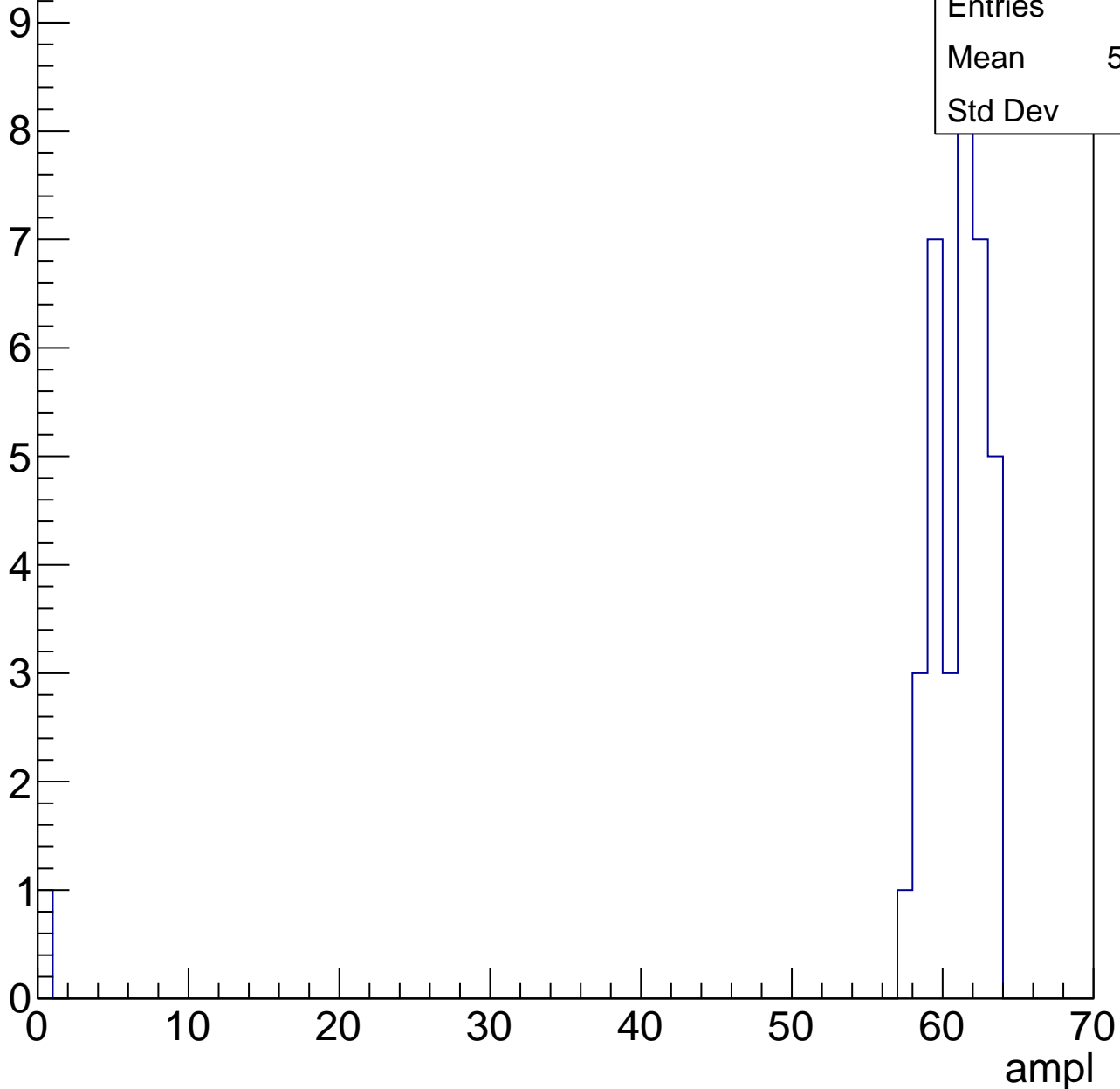
Entries	54
Mean	56.06
Std Dev	3.07

B1L103S, U7-ch9, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	36
Mean	58.94
Std Dev	10.1



B1L103S, U7-ch9, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch9, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73



B1L103S, U7-ch10, adc0

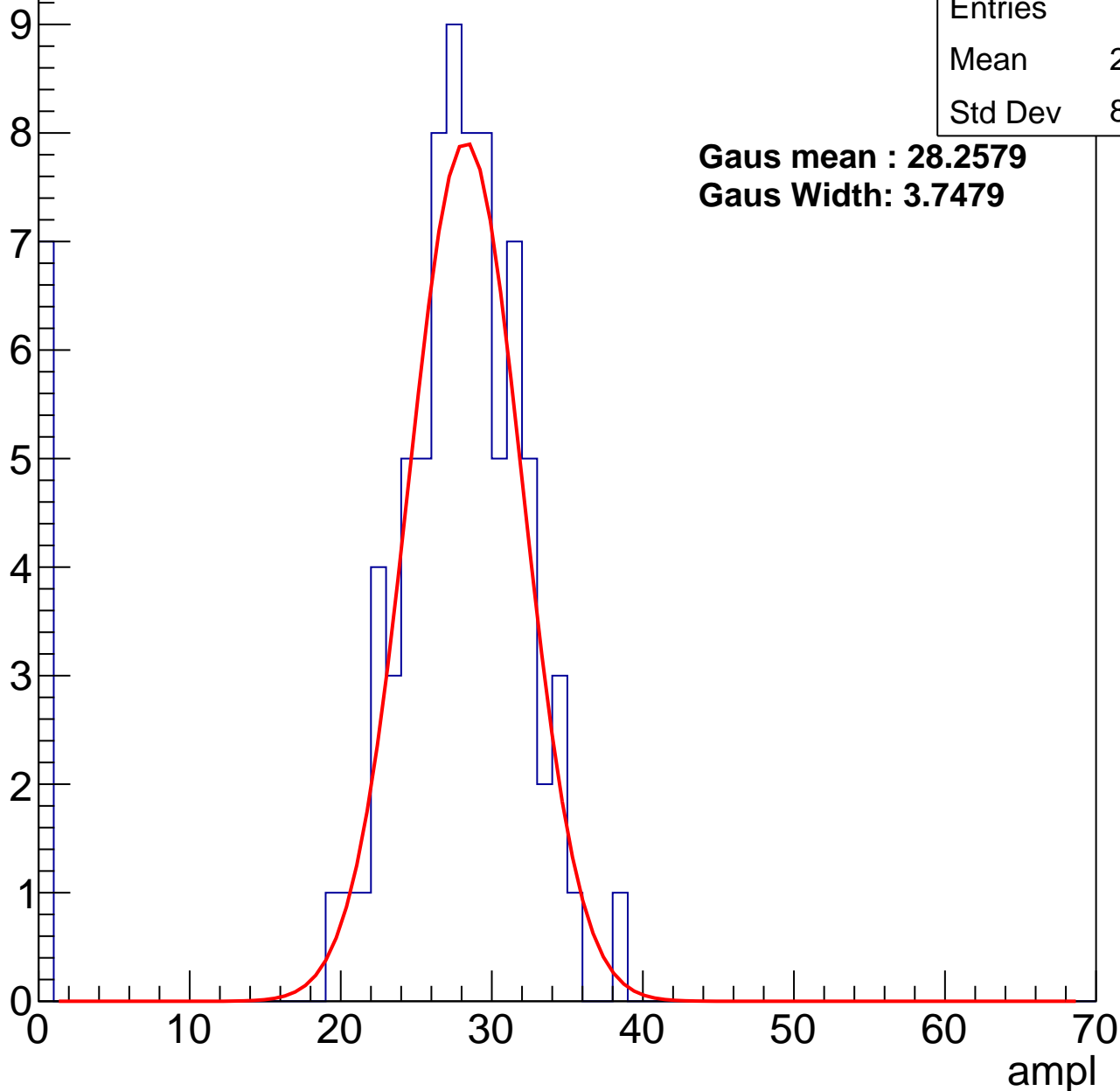
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	84
Mean	25.44
Std Dev	8.448

Gaus mean : 28.2579

Gaus Width: 3.7479



B1L103S, U7-ch10, adc1

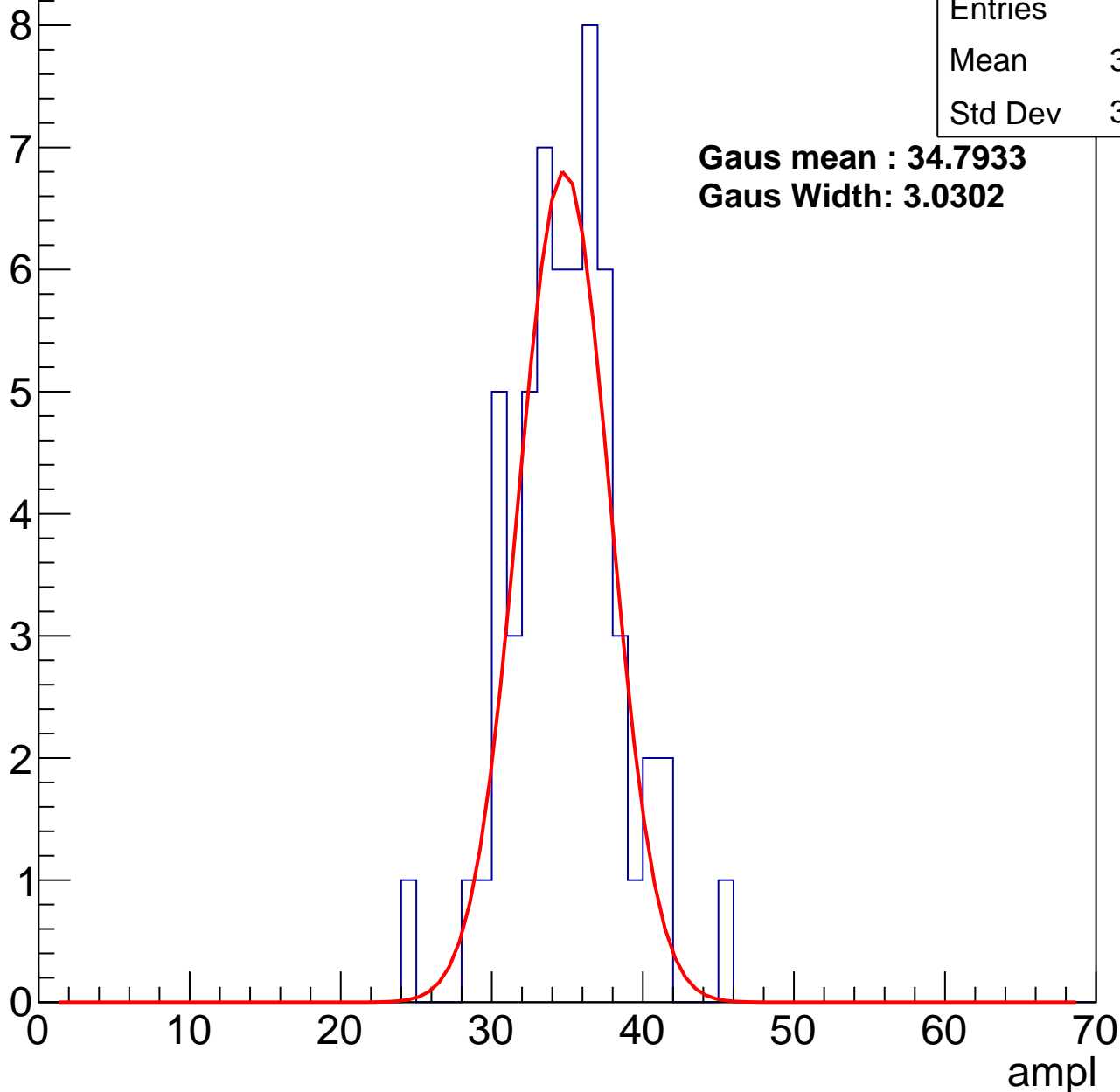
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	34.47
Std Dev	3.568

Gaus mean : 34.7933

Gaus Width: 3.0302



B1L103S, U7-ch10, adc2

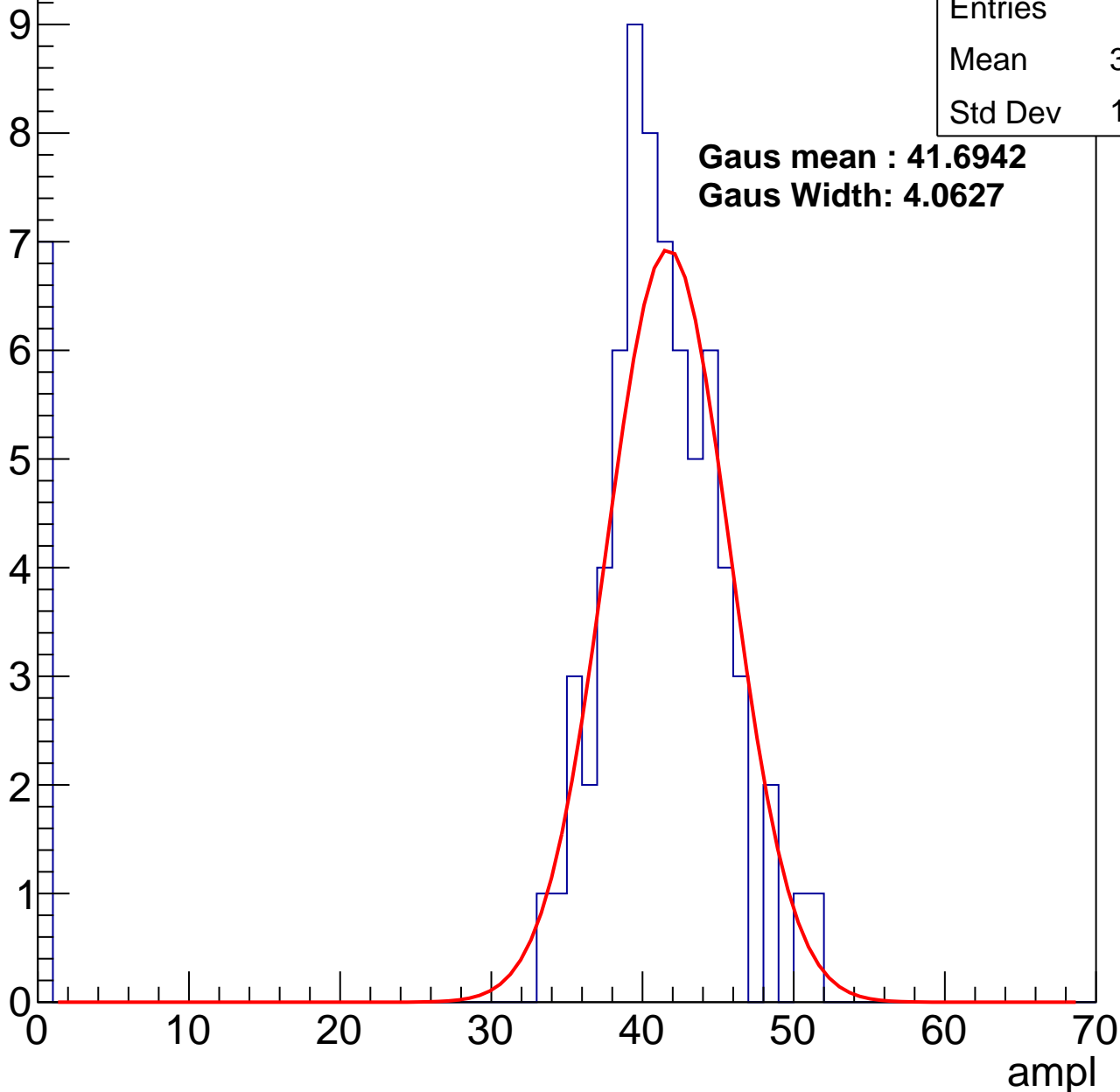
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	37.16
Std Dev	12.34

Gaus mean : 41.6942

Gaus Width: 4.0627

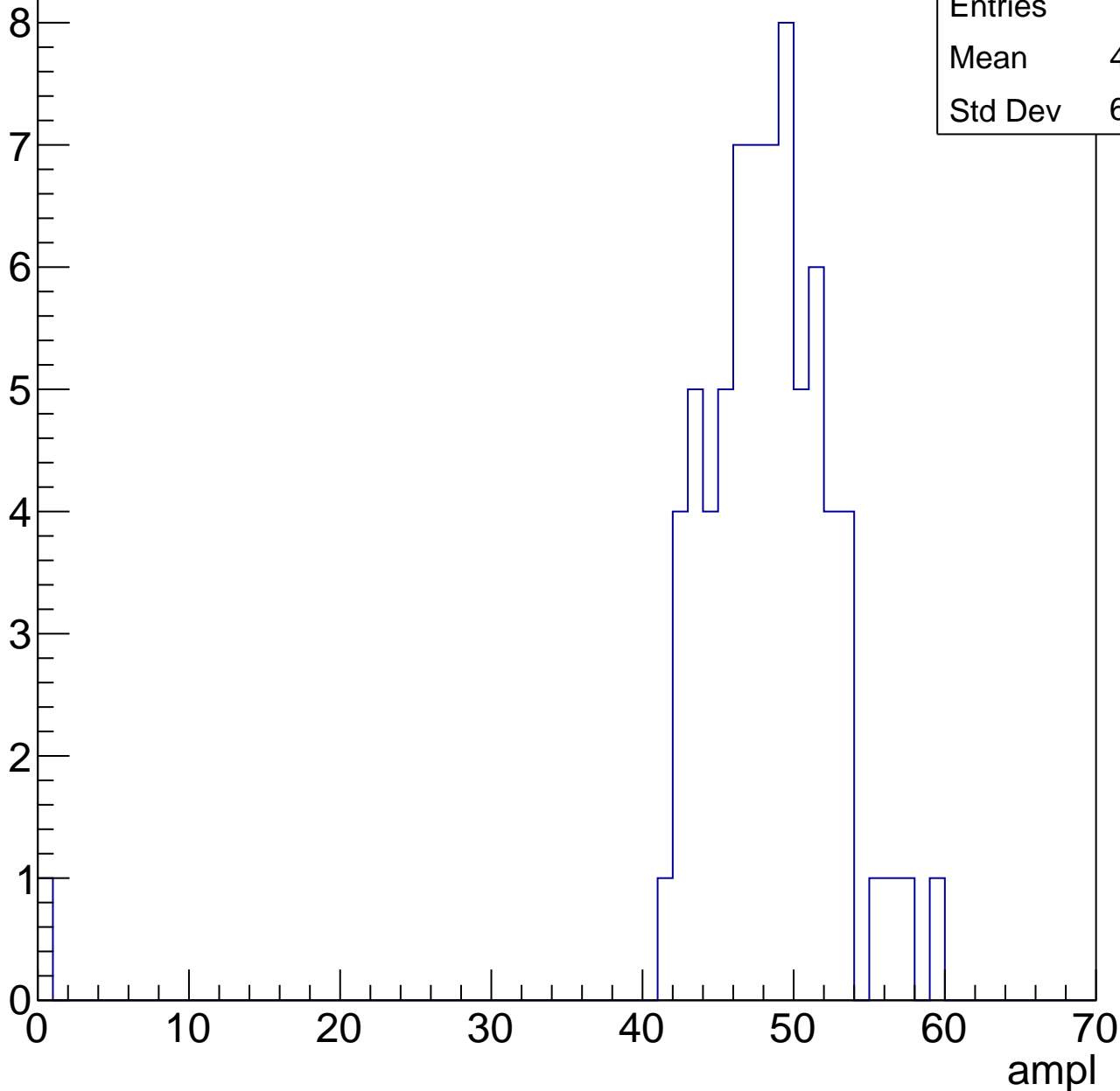


B1L103S, U7-ch10, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	47.32
Std Dev	6.764

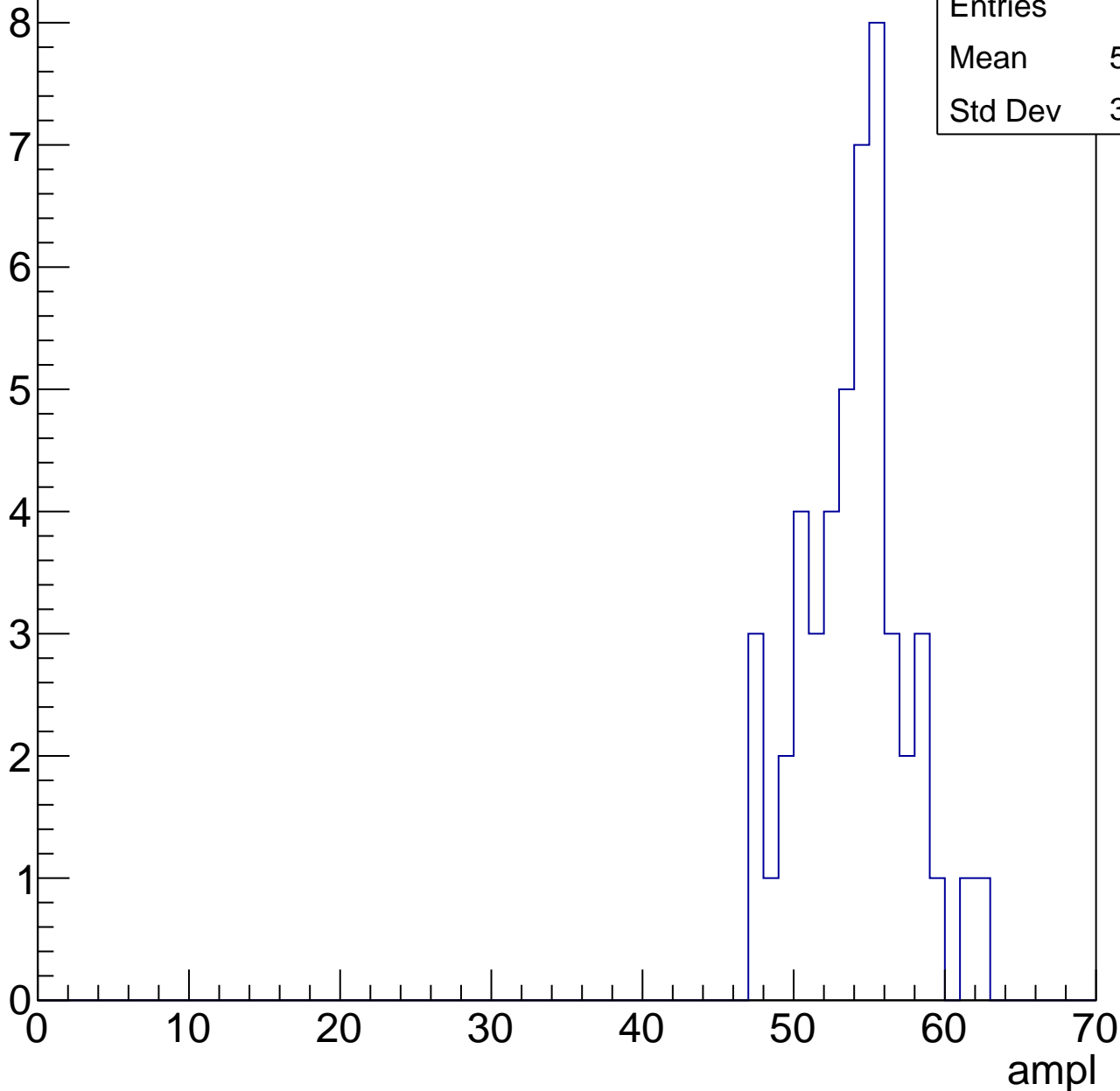


B1L103S, U7-ch10, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

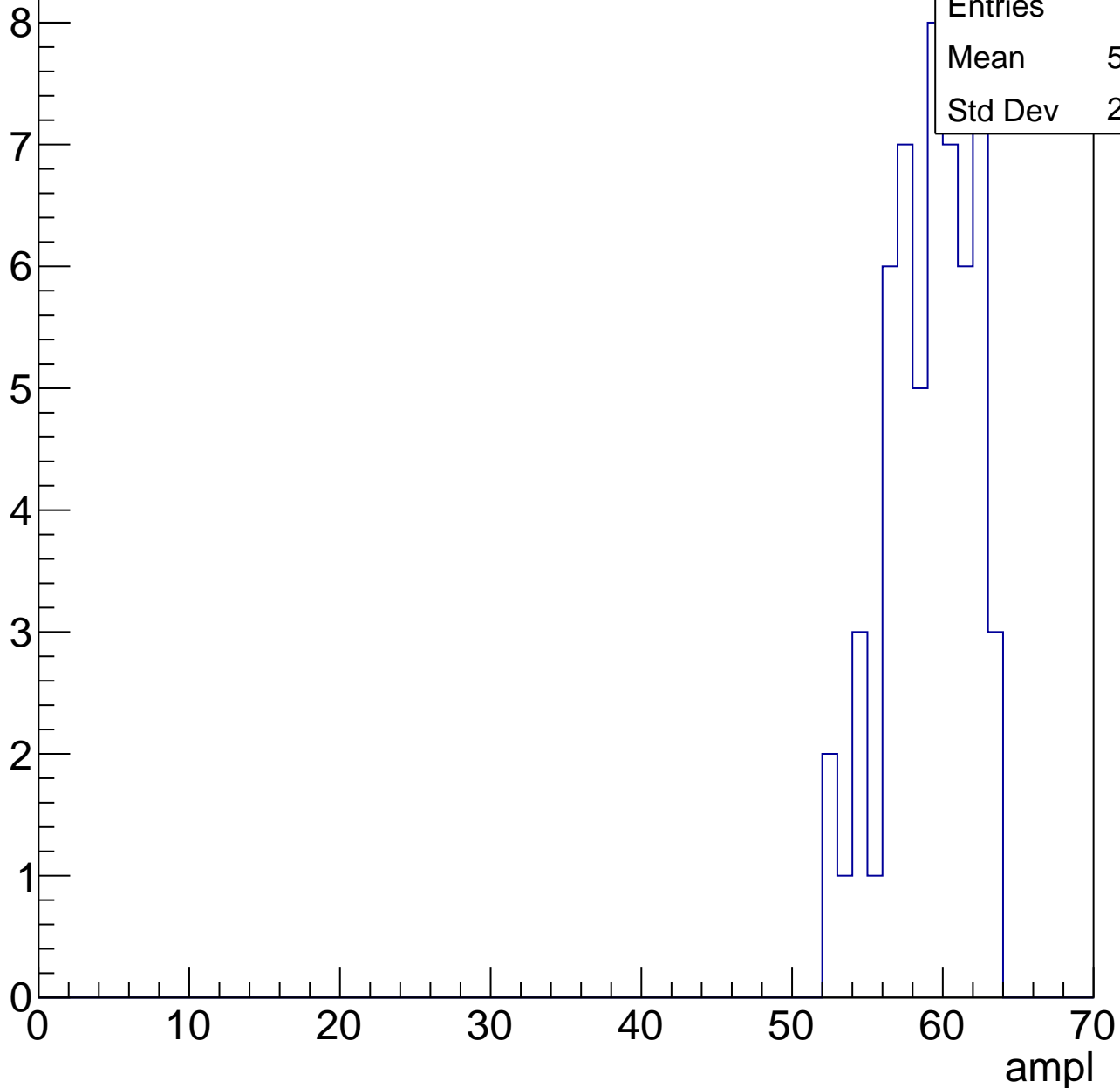
Entries	48
Mean	53.52
Std Dev	3.409



B1L103S, U7-ch10, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

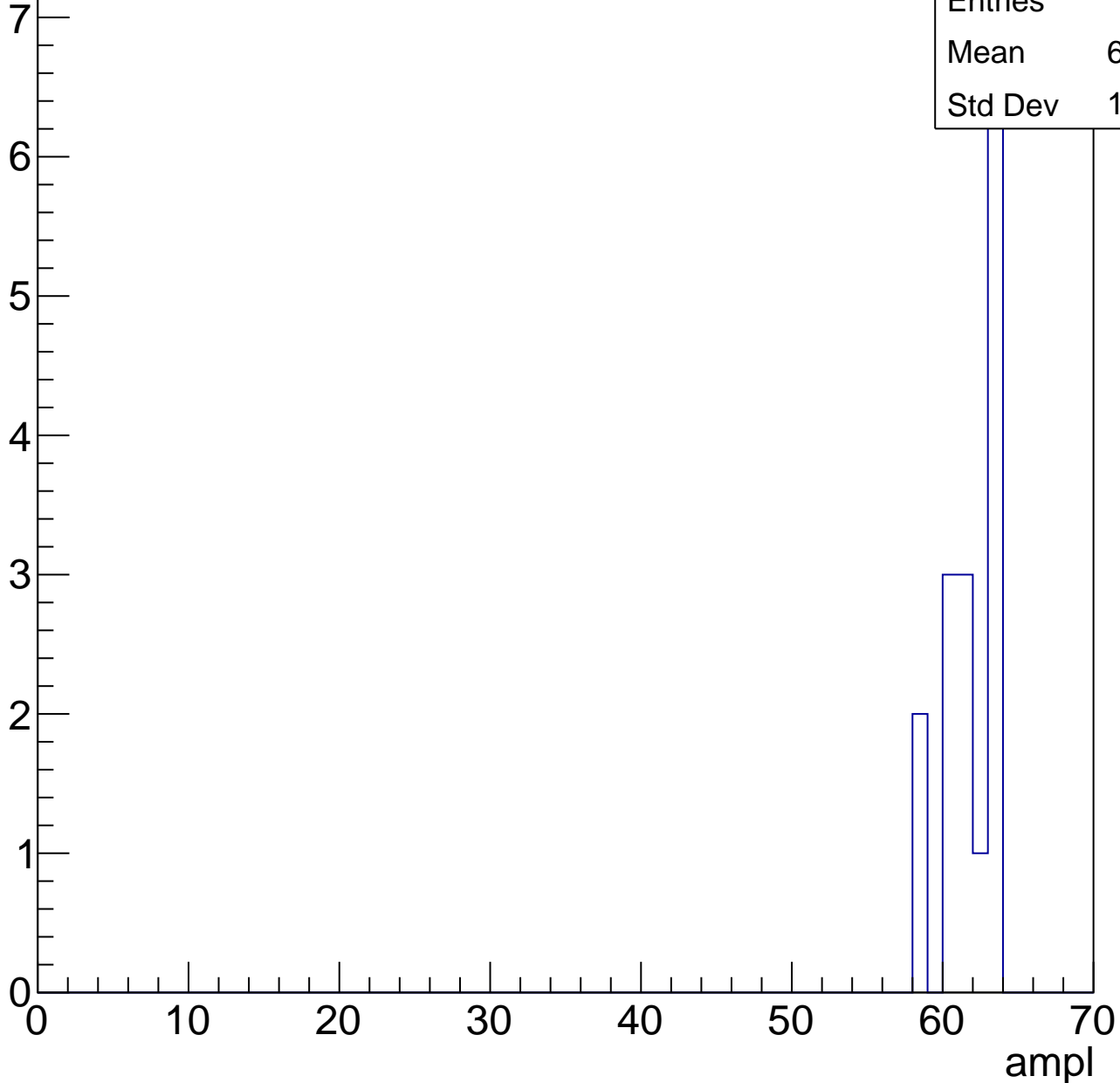


B1L103S, U7-ch10, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	16
Mean	61.38
Std Dev	1.728



B1L103S, U7-ch10, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

20
18
16
14
12
10
8
6
4
2
0

Entries	20
Mean	0
Std Dev	0

ampl

B1L103S, U7-ch11, adc0

calib_packv5_041523_1651.root, FC#0, port C2

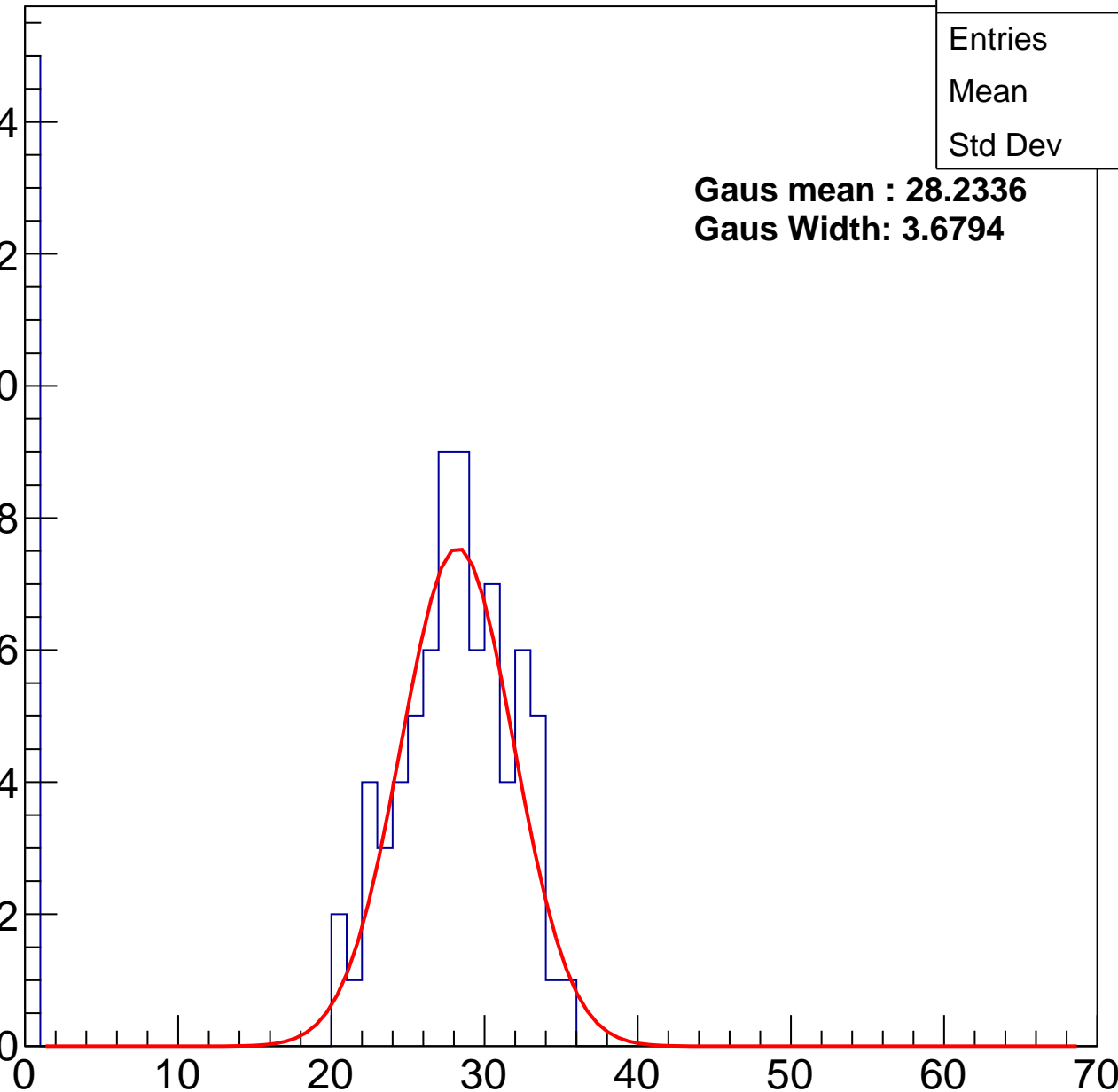
Entry

14
12
10
8
6
4
2
0

Entries	88
Mean	23
Std Dev	10.91

Gaus mean : 28.2336

Gaus Width: 3.6794



ampl

B1L103S, U7-ch11, adc1

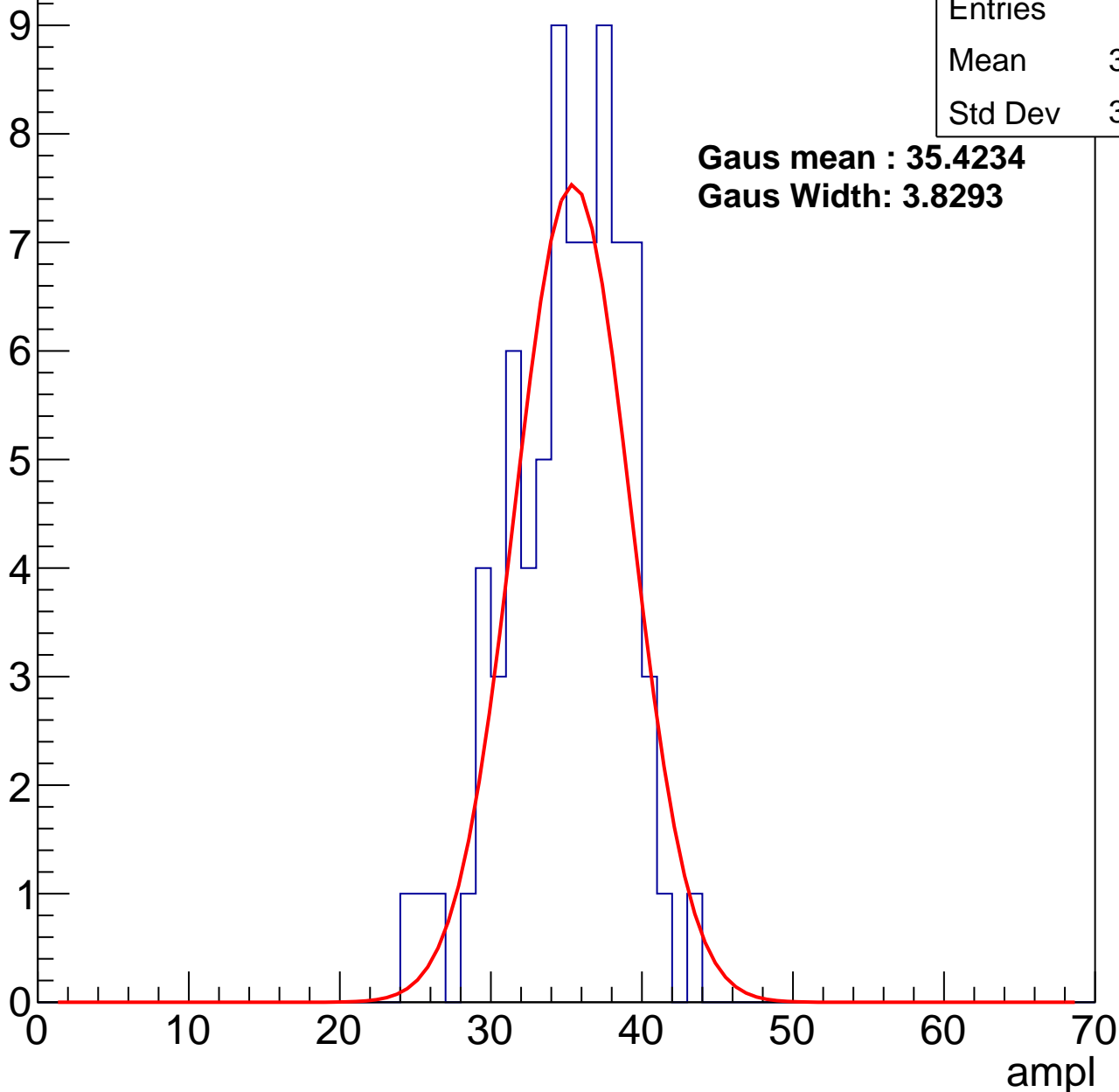
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	34.64
Std Dev	3.803

Gaus mean : 35.4234

Gaus Width: 3.8293



B1L103S, U7-ch11, adc2

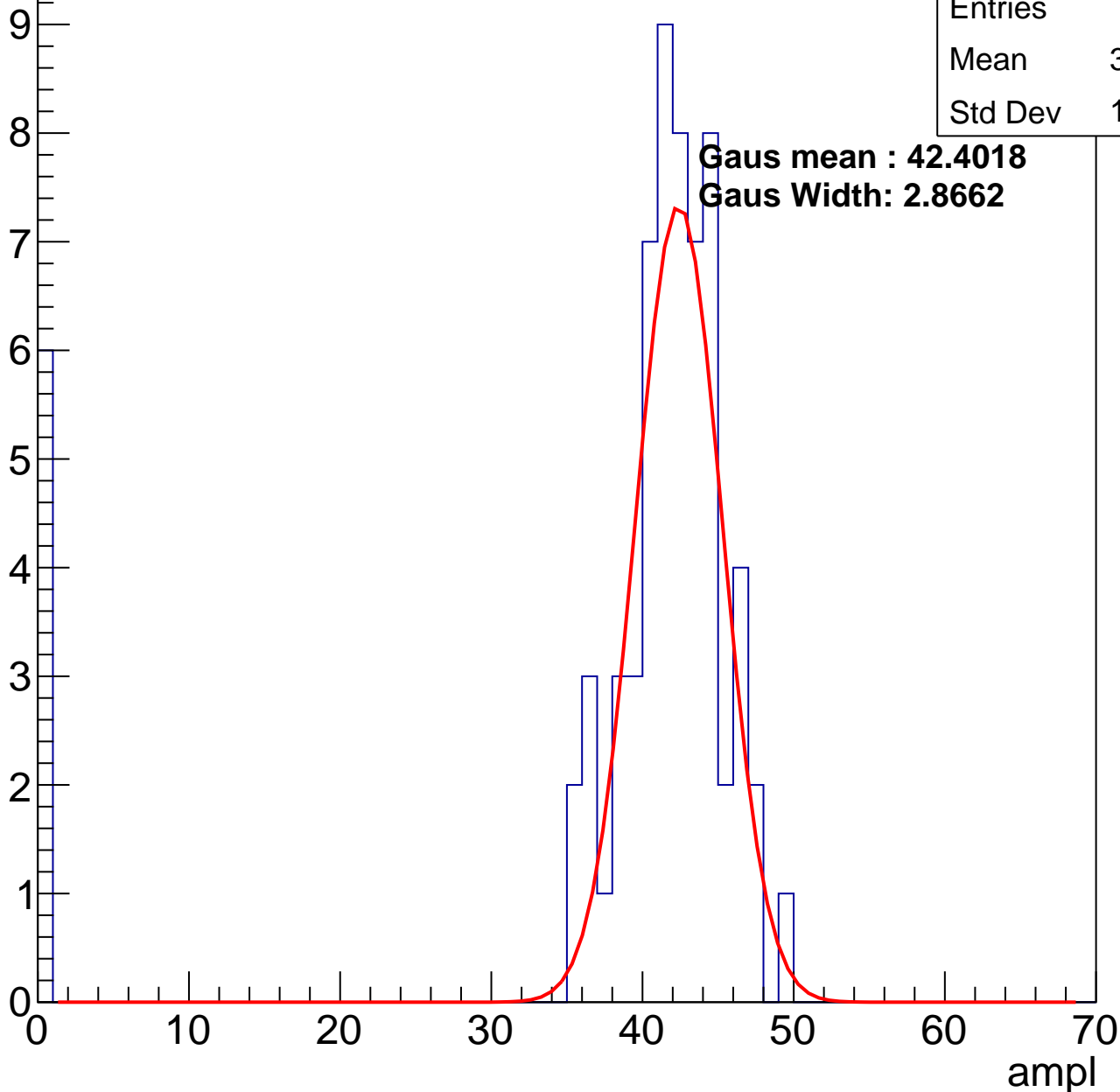
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	37.89
Std Dev	12.33

Gaus mean : 42.4018

Gaus Width: 2.8662

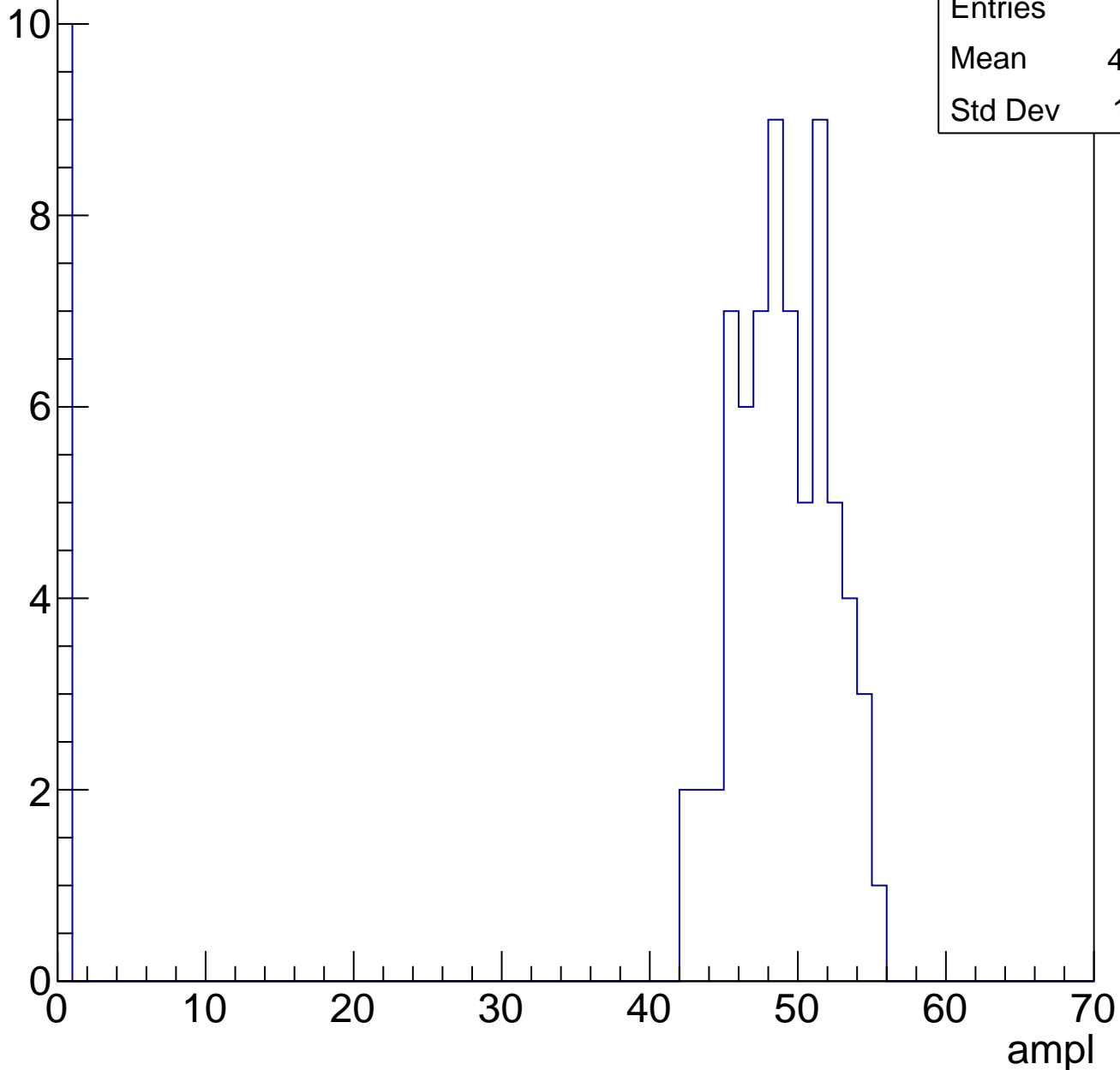


B1L103S, U7-ch11, adc3

calib_packv5_041523_1651.root, FC#0, port C2

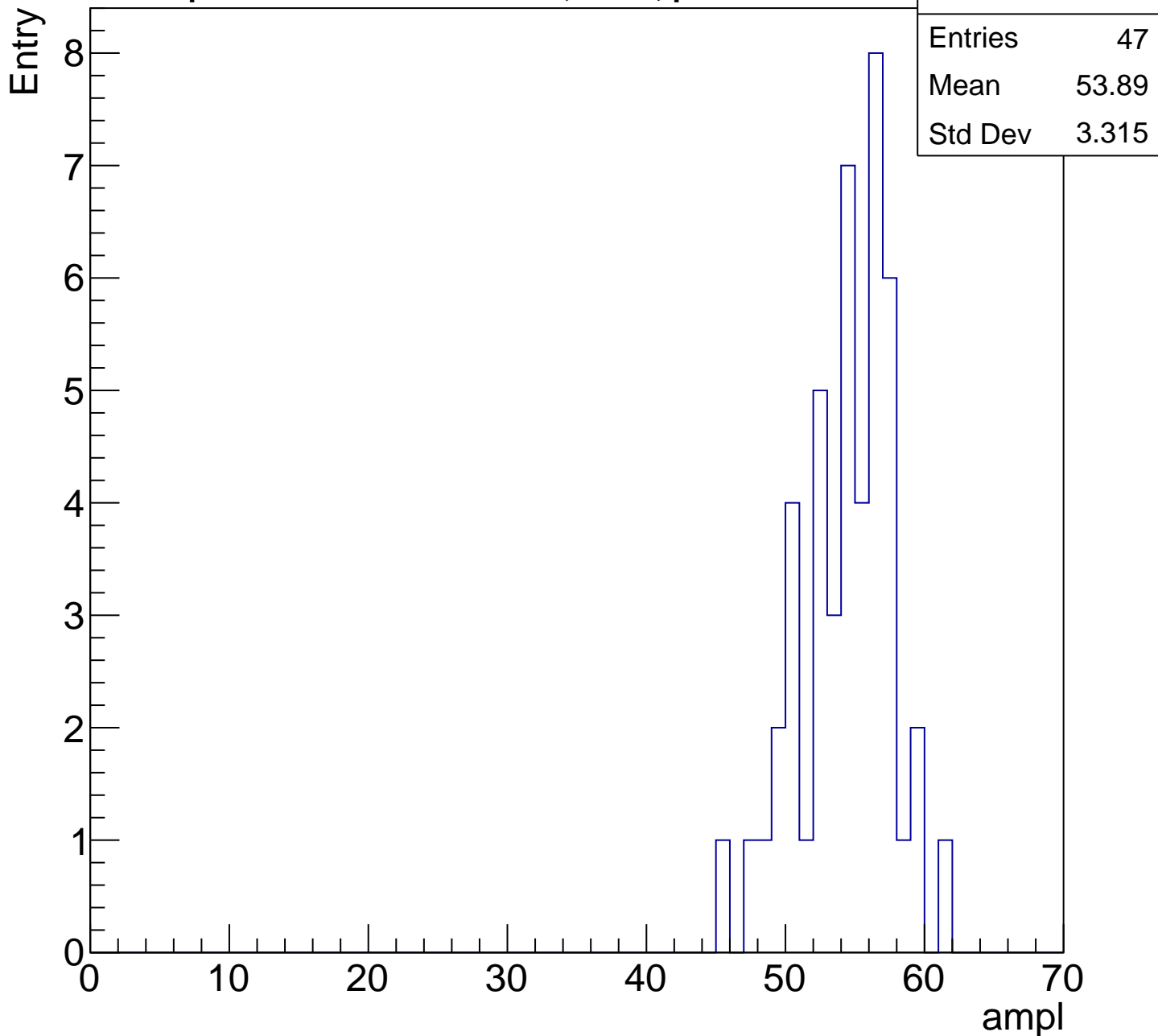
Entries	79
Mean	42.42
Std Dev	16.41

Entry



B1L103S, U7-ch11, adc4

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U7-ch11, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

8

6

4

2

0

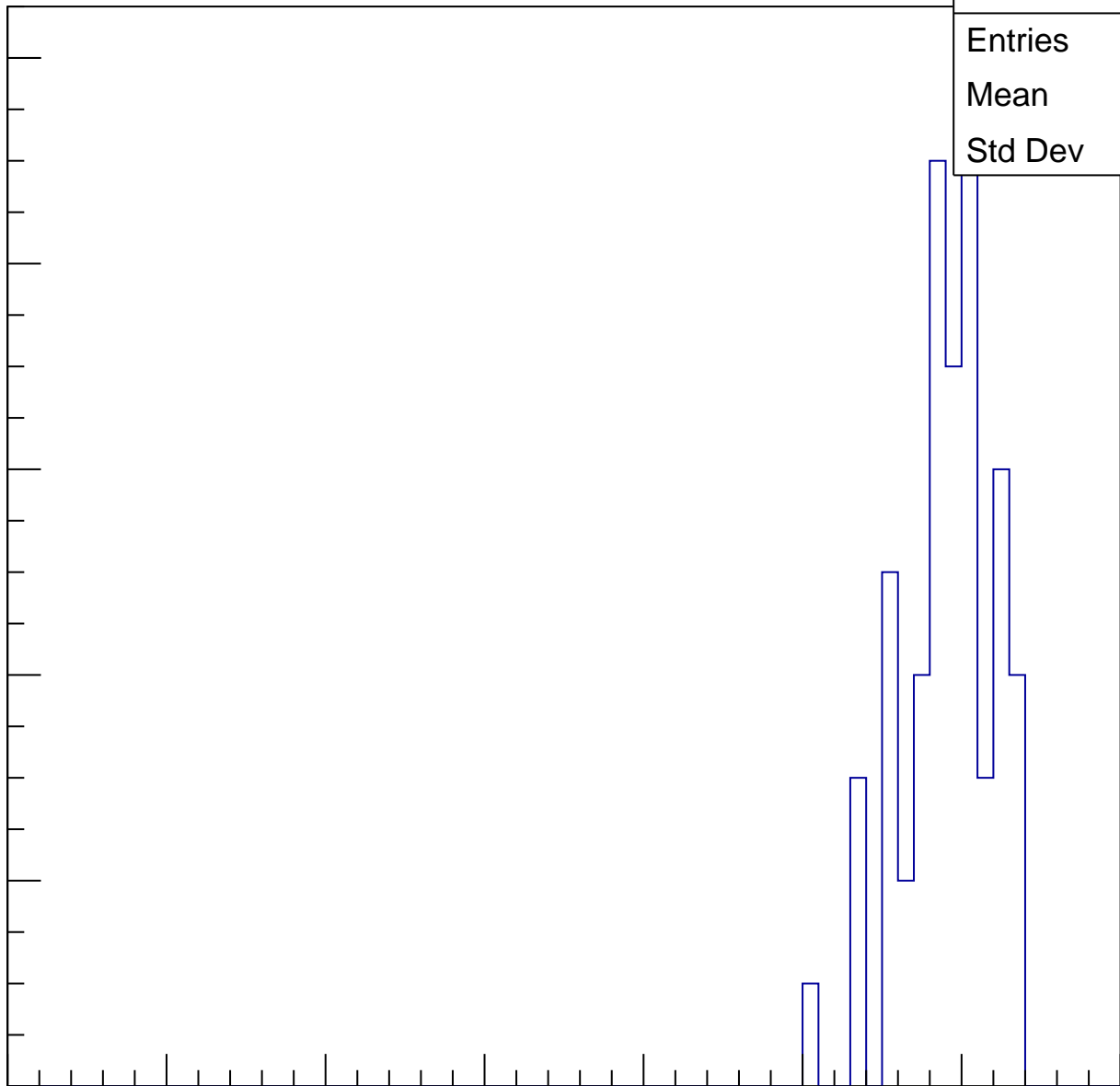
Entries 54

Mean 58.63

Std Dev 2.869

ampl

0 10 20 30 40 50 60 70

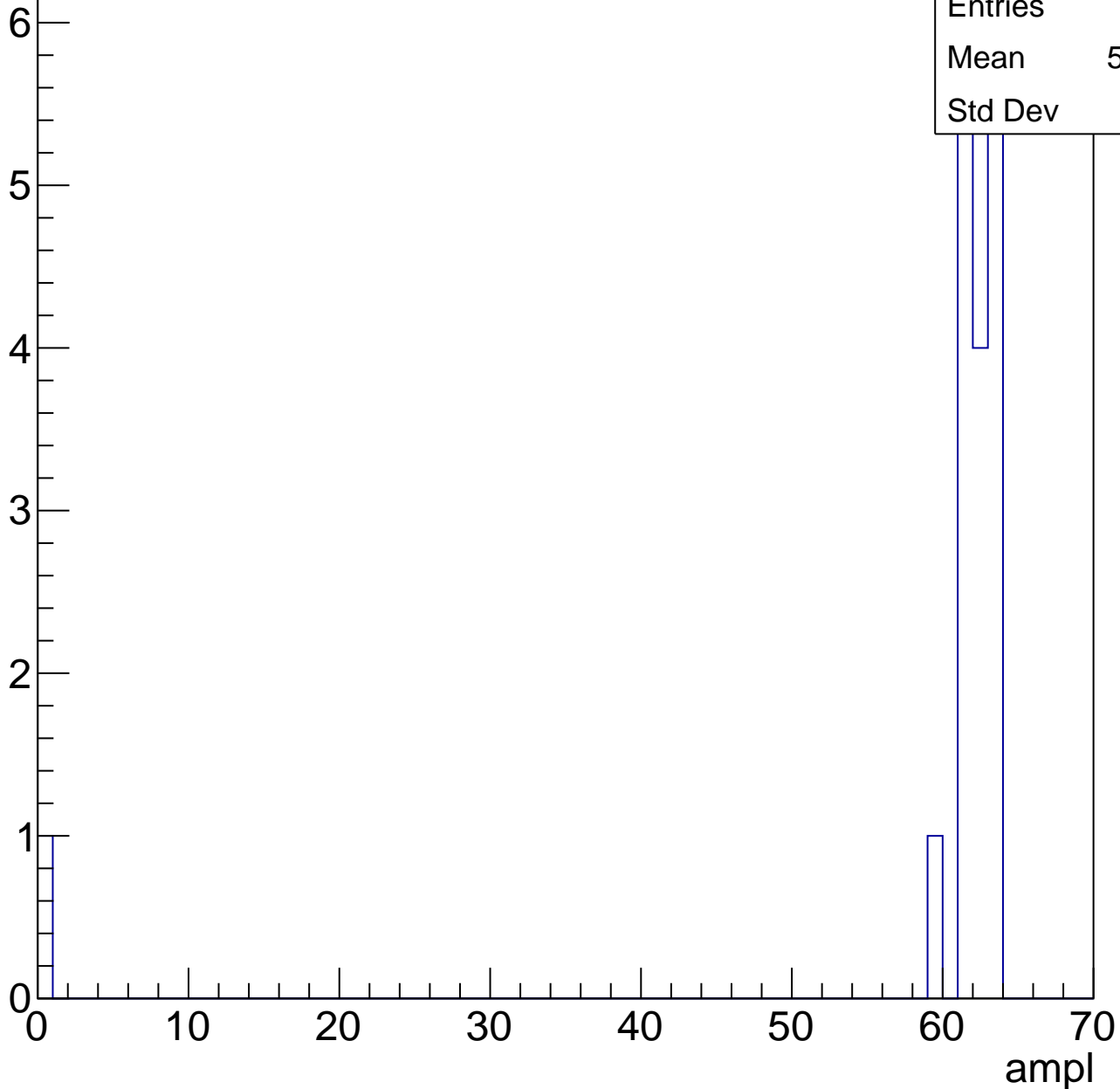


B1L103S, U7-ch11, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	18
Mean	58.39
Std Dev	14.2



B1L103S, U7-ch11, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U7-ch12, adc0

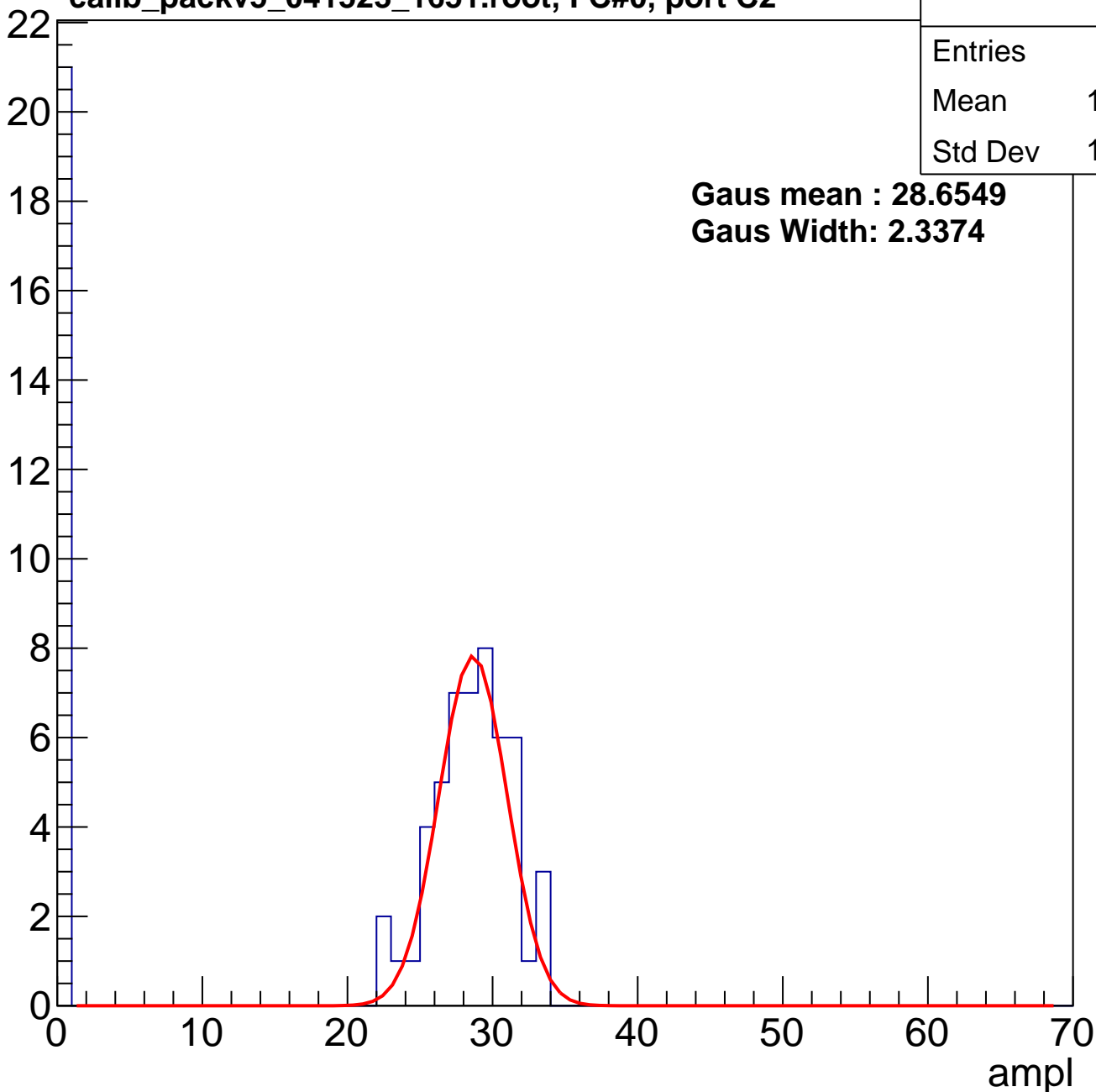
calib_packv5_041523_1651.root, FC#0, port C2

Entries	72
Mean	19.93
Std Dev	12.98

Gaus mean : 28.6549

Gaus Width: 2.3374

Entry



B1L103S, U7-ch12, adc1

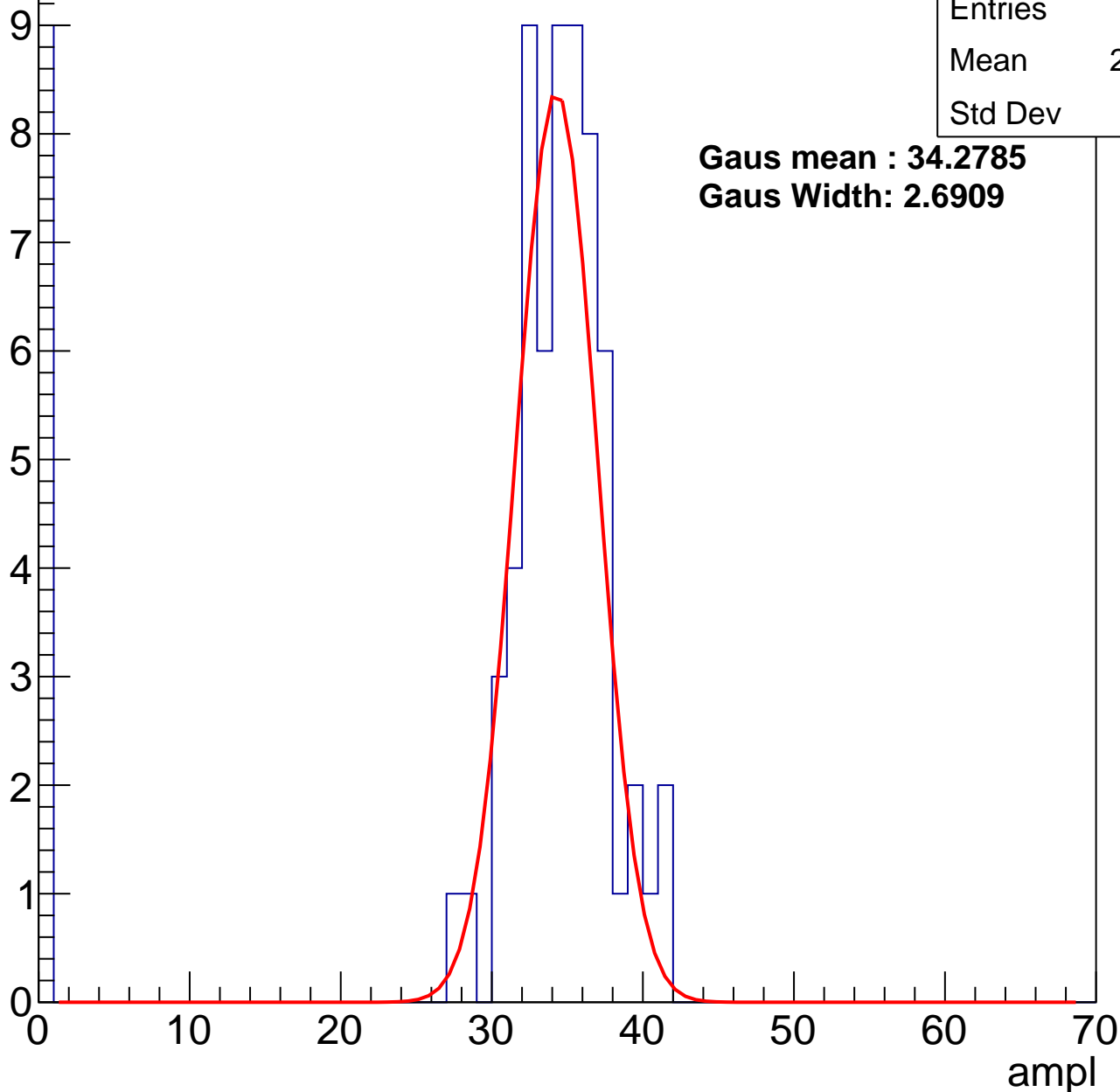
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	29.92
Std Dev	11.7

Gaus mean : 34.2785

Gaus Width: 2.6909



B1L103S, U7-ch12, adc2

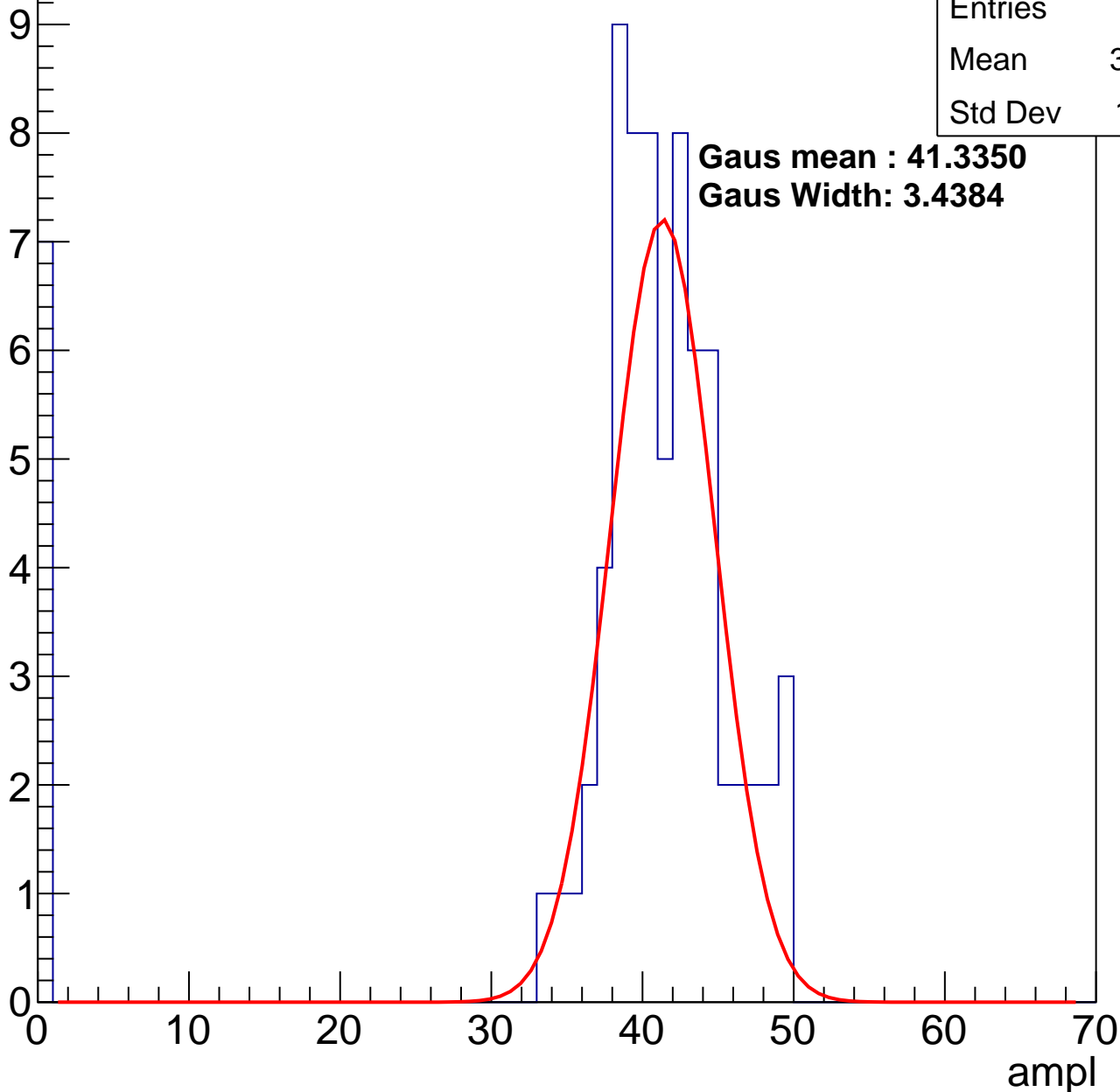
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	37.38
Std Dev	12.31

Gaus mean : 41.3350

Gaus Width: 3.4384

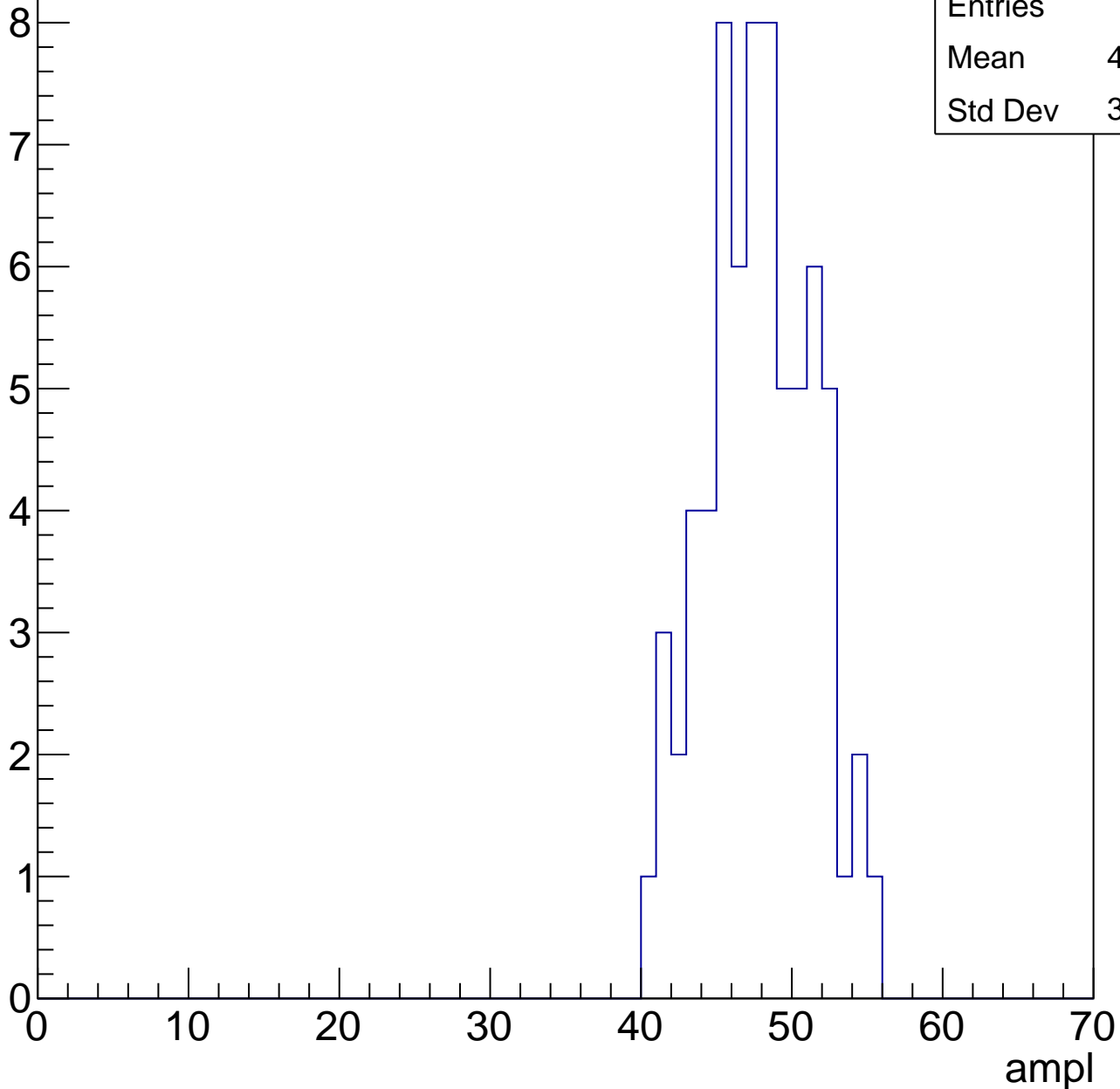


B1L103S, U7-ch12, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	47.36
Std Dev	3.464

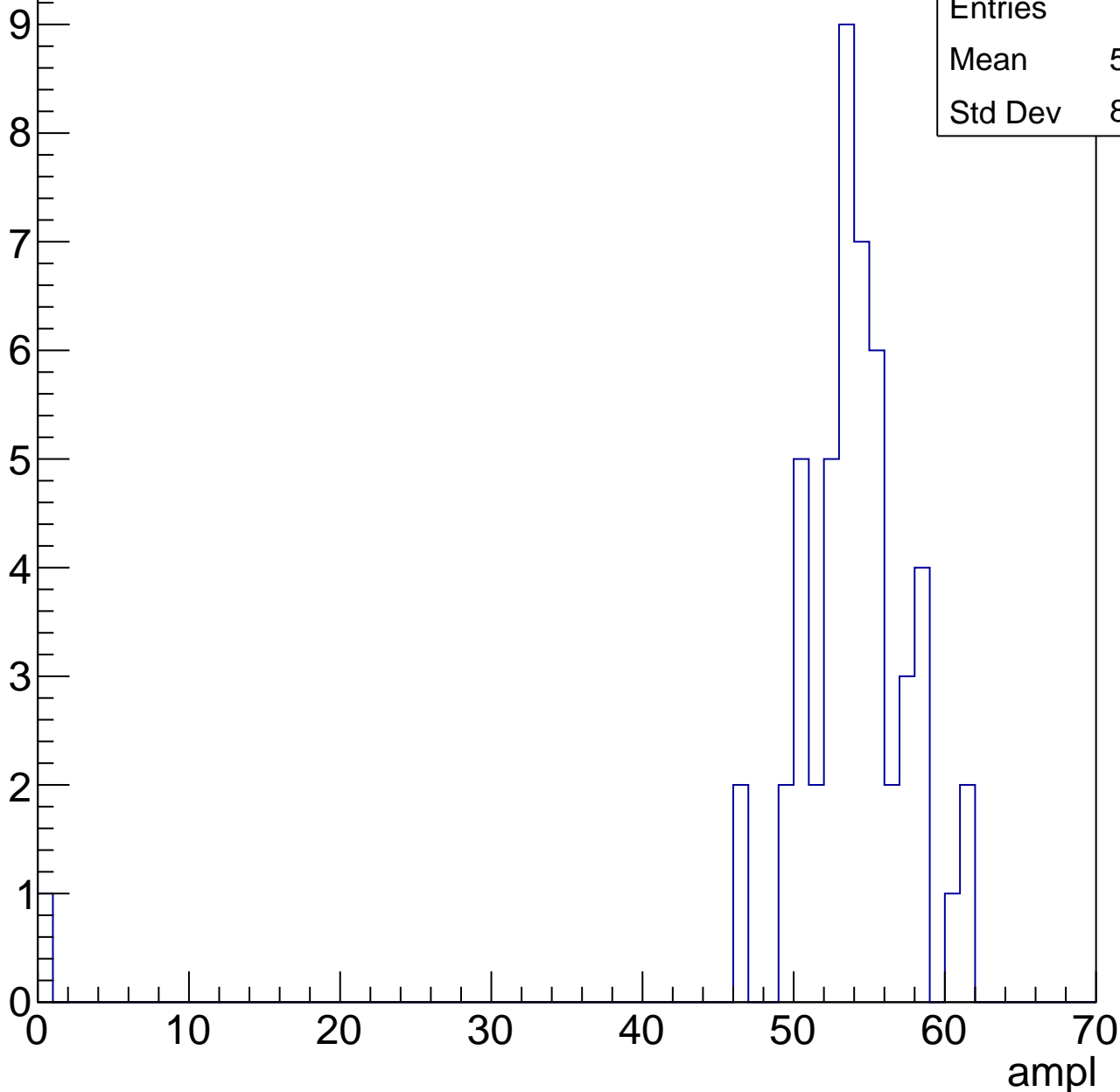


B1L103S, U7-ch12, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	52.63
Std Dev	8.122

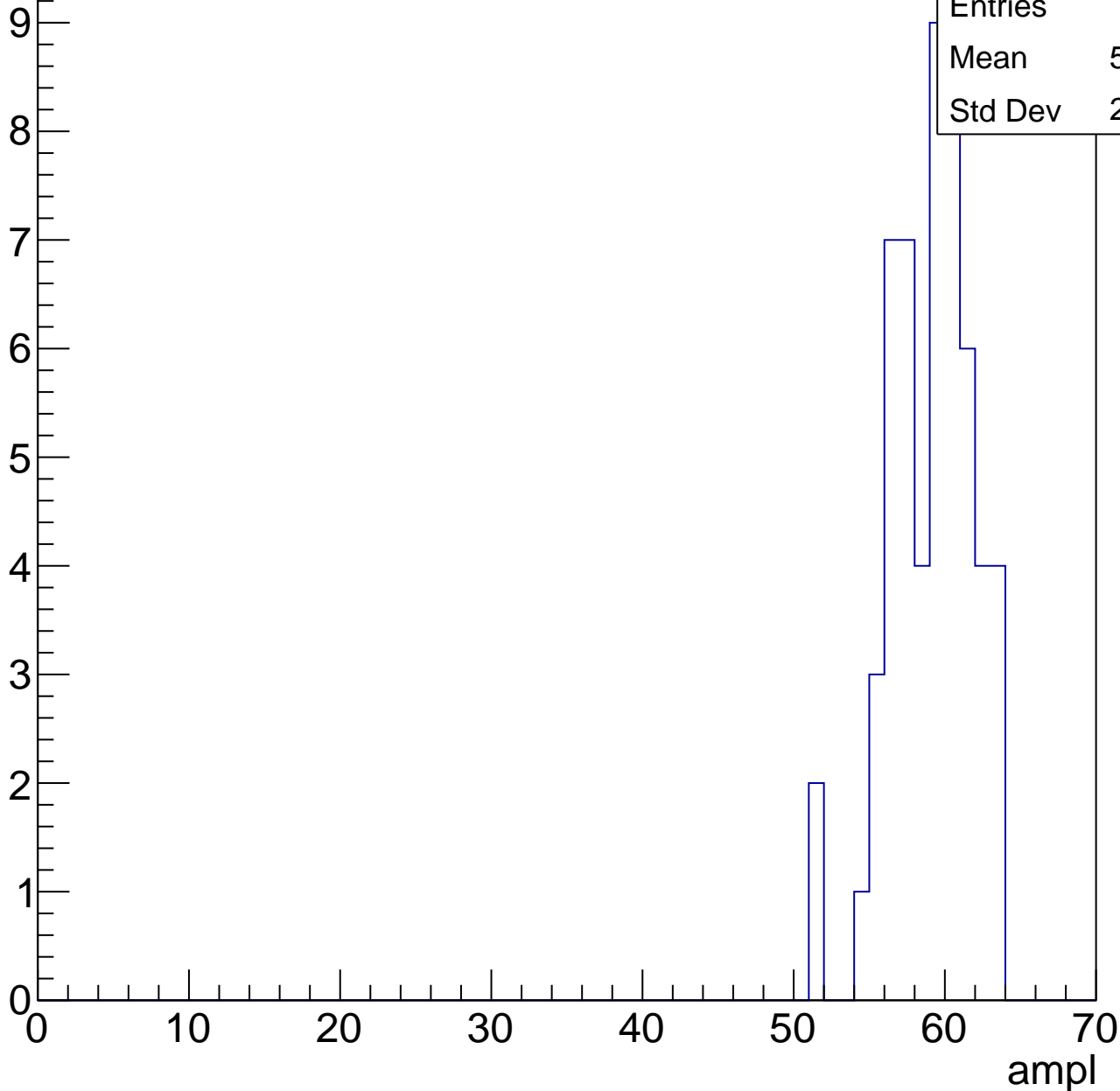


B1L103S, U7-ch12, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	58.56
Std Dev	2.755

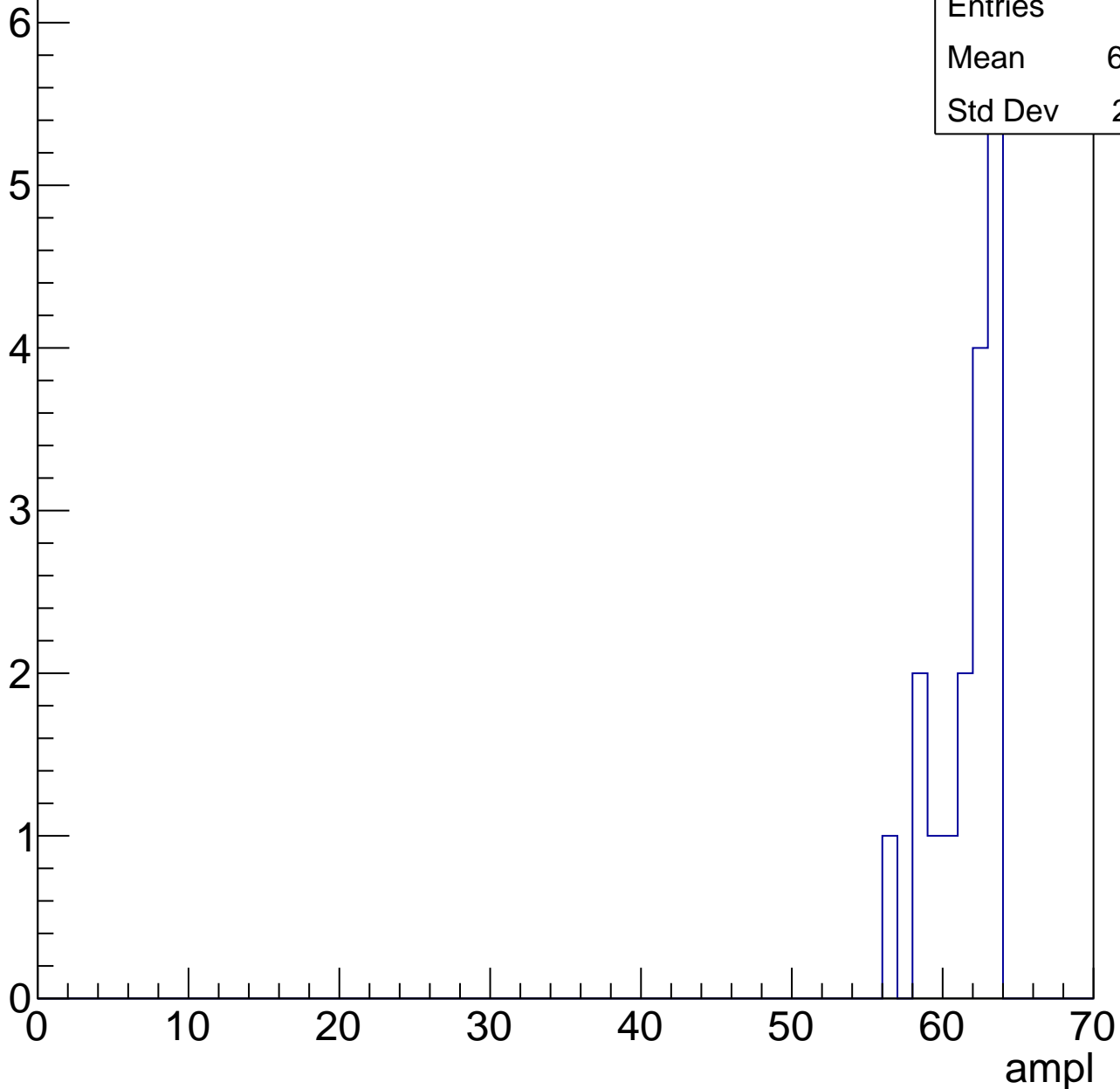


B1L103S, U7-ch12, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	17
Mean	61.12
Std Dev	2.111

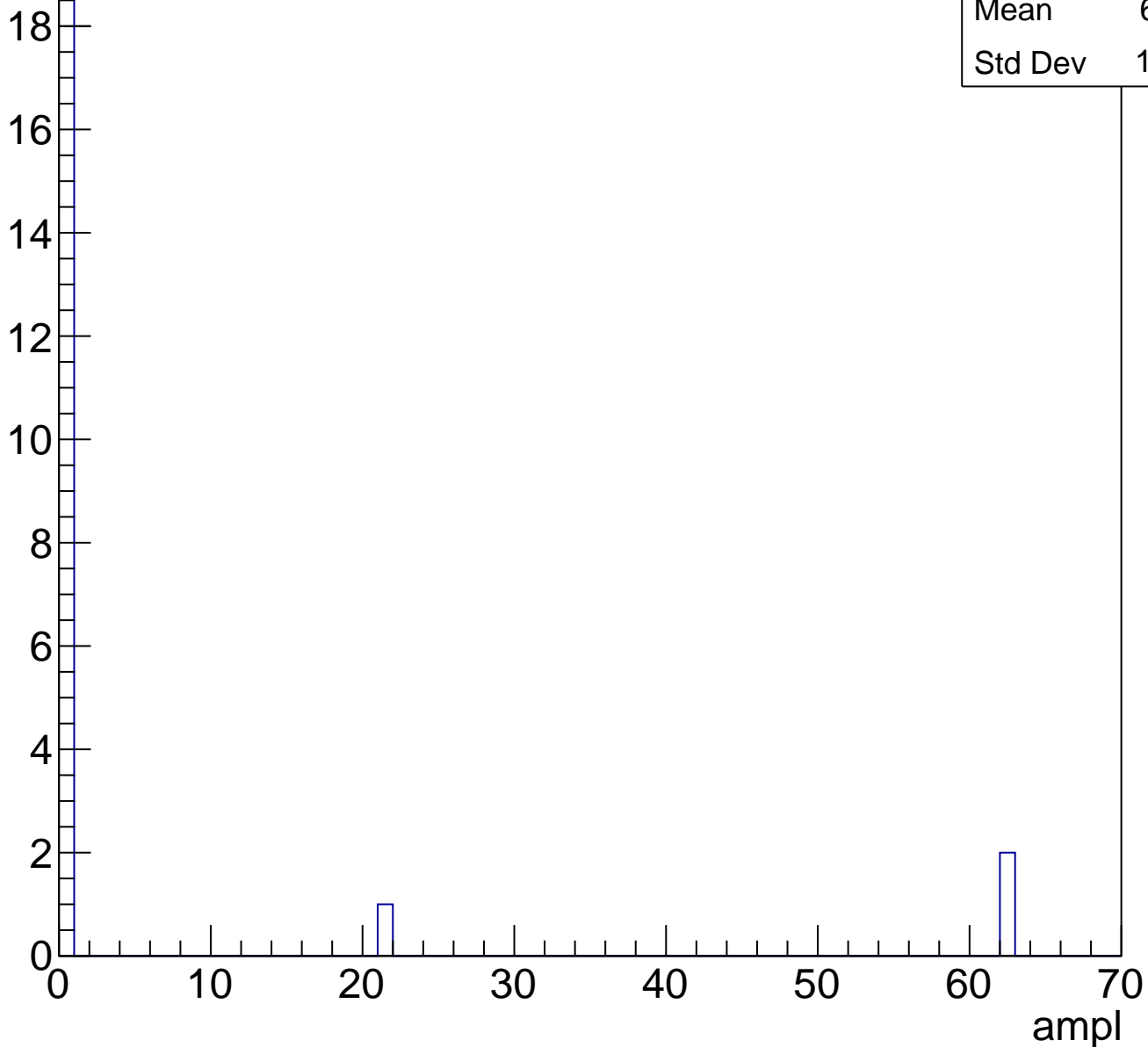


B1L103S, U7-ch12, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	22
Mean	6.591
Std Dev	18.06

Entry



B1L103S, U7-ch13, adc0

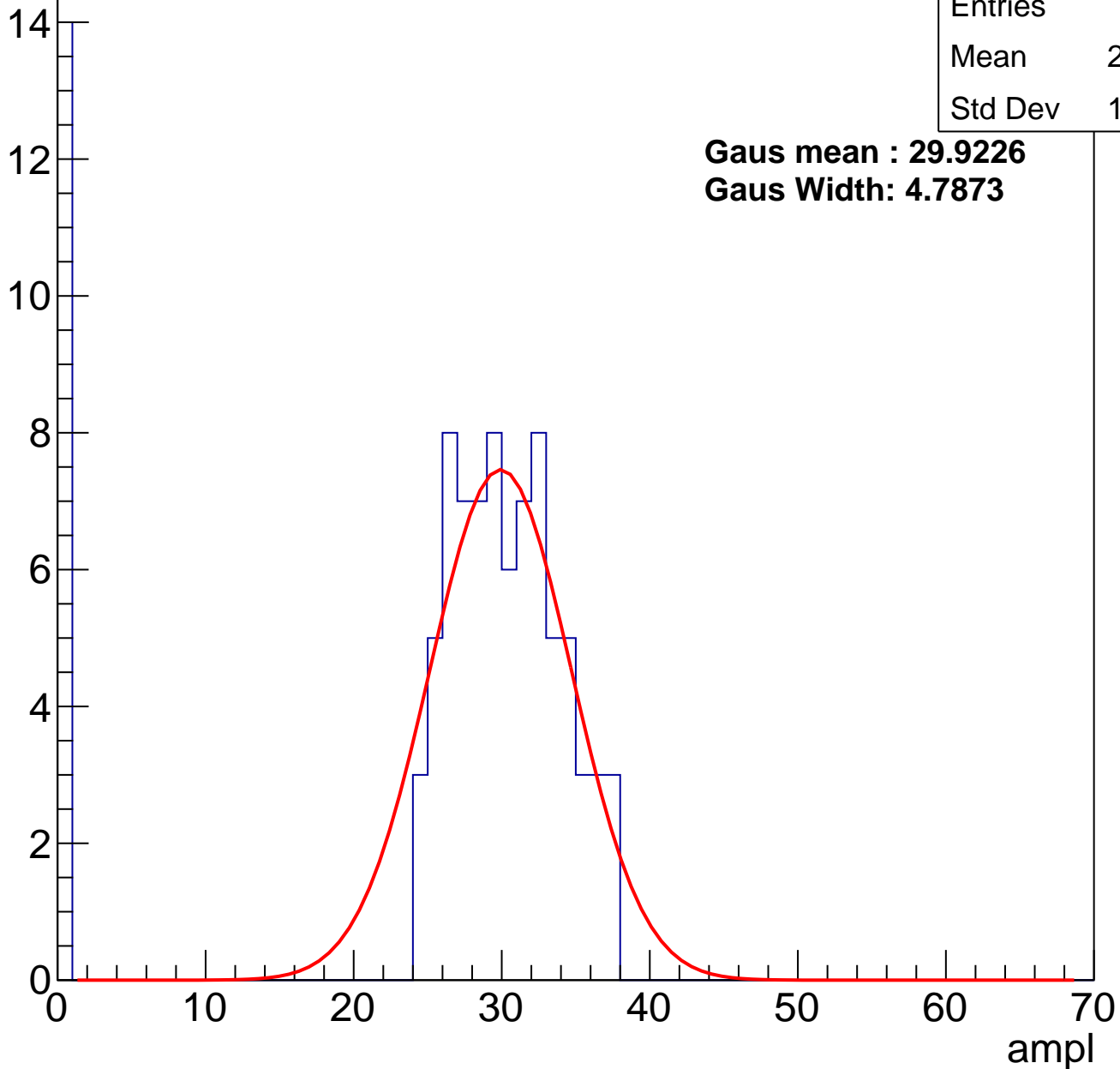
calib_packv5_041523_1651.root, FC#0, port C2

Entries	92
Mean	25.37
Std Dev	11.22

Gaus mean : 29.9226

Gaus Width: 4.7873

Entry



B1L103S, U7-ch13, adc1

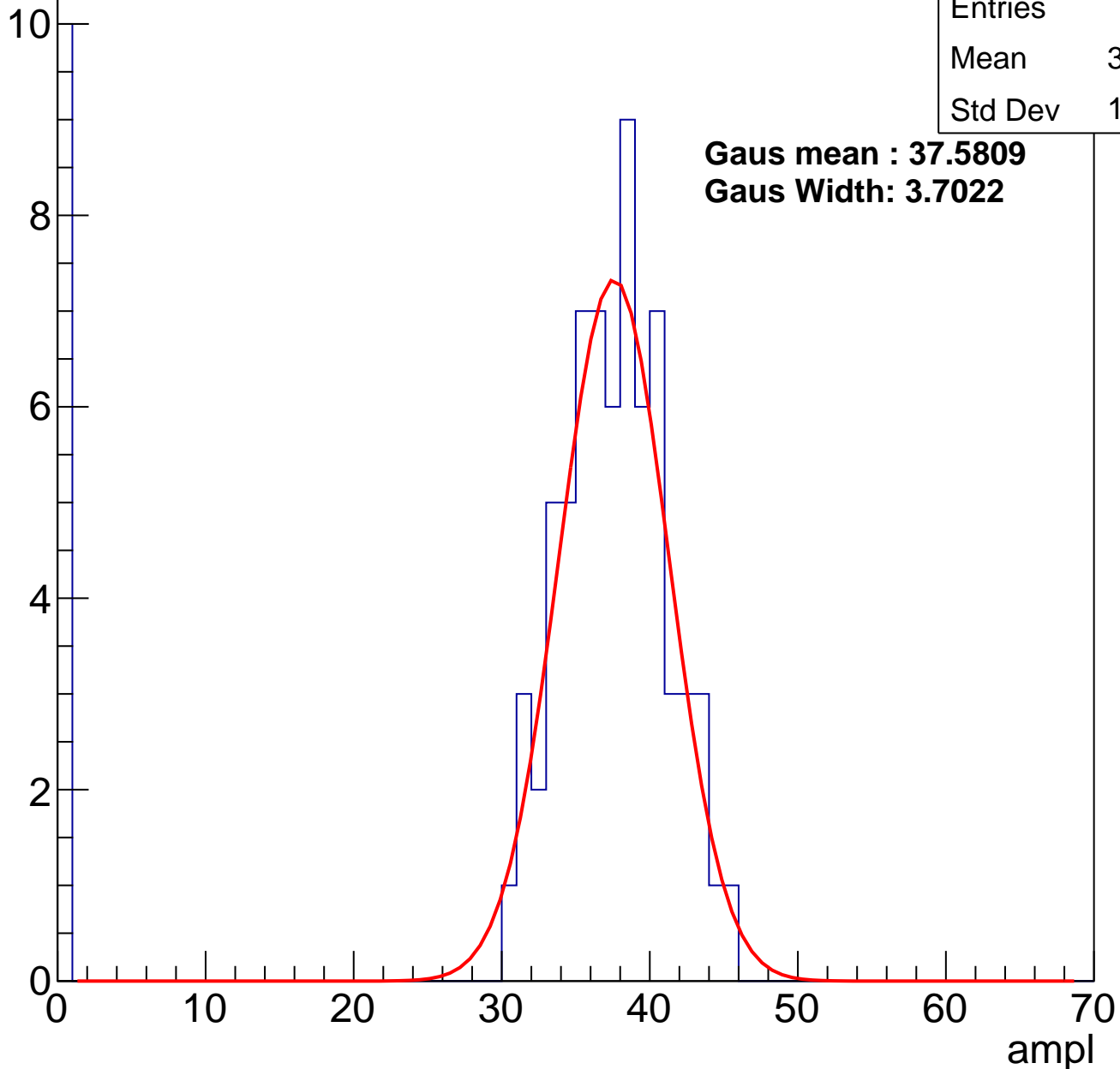
calib_packv5_041523_1651.root, FC#0, port C2

Entries	79
Mean	32.46
Std Dev	12.76

Gaus mean : 37.5809

Gaus Width: 3.7022

Entry



B1L103S, U7-ch13, adc2

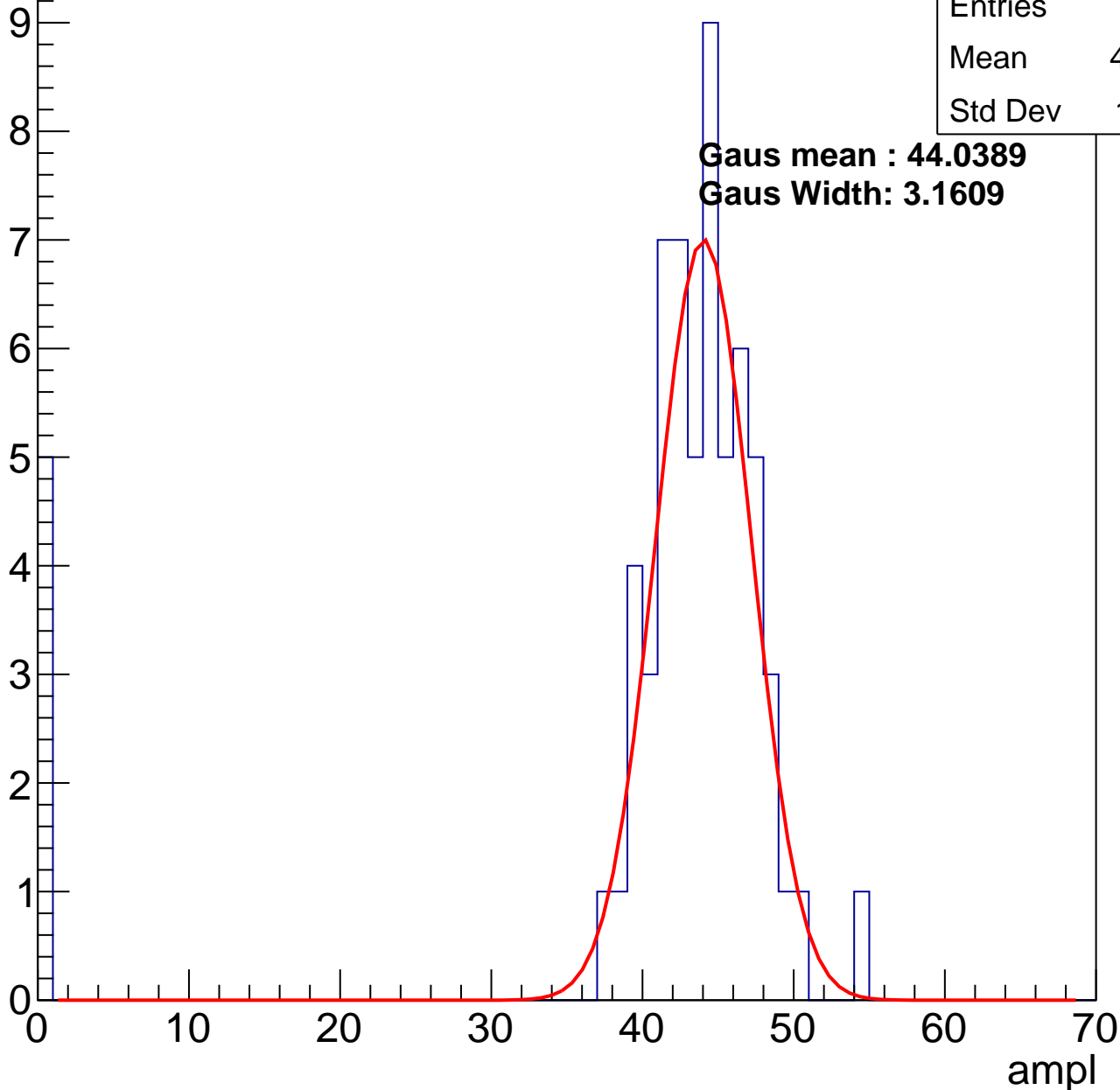
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	40.25
Std Dev	12.11

Gaus mean : 44.0389

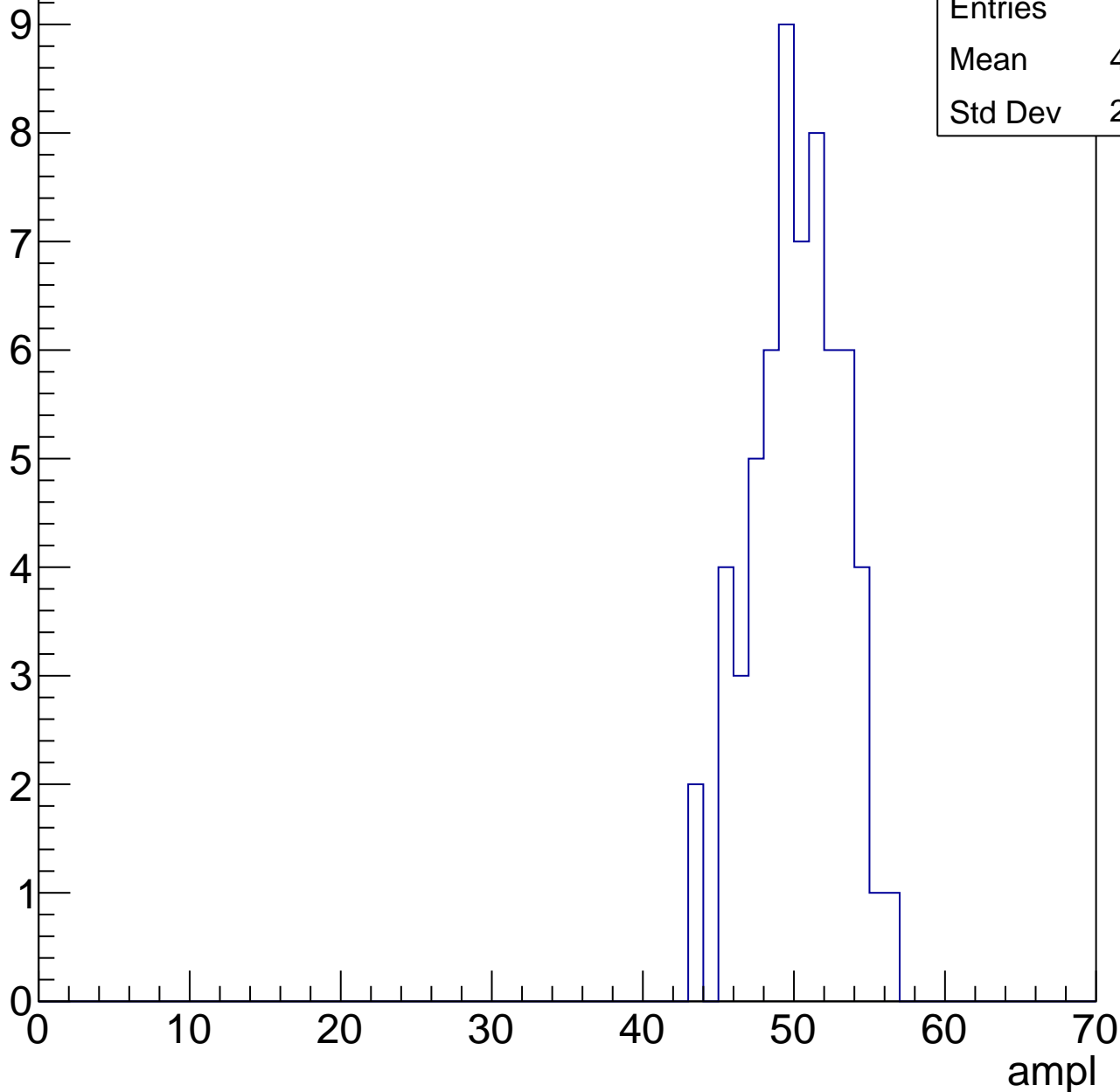
Gaus Width: 3.1609



B1L103S, U7-ch13, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

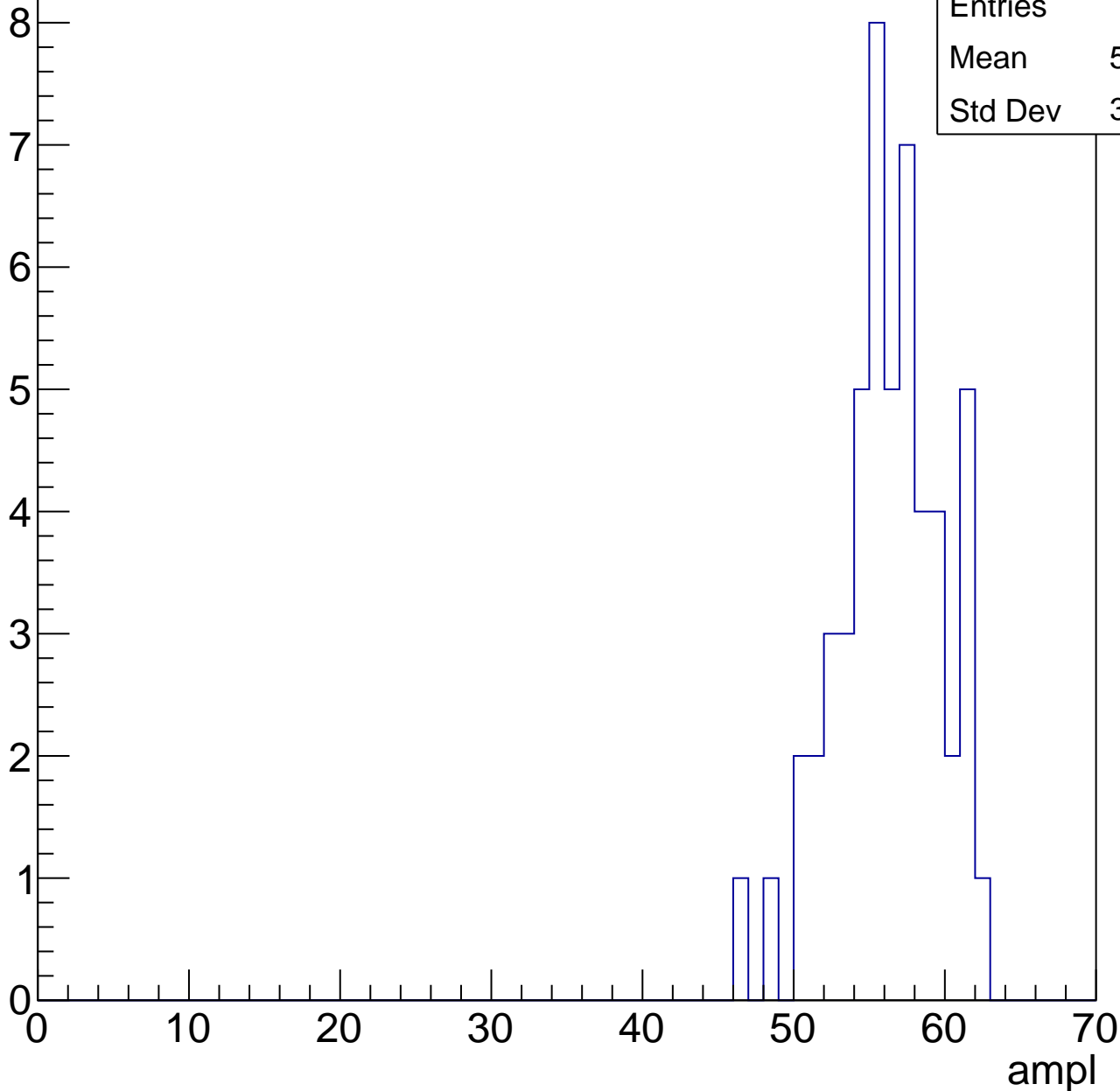


B1L103S, U7-ch13, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	55.75
Std Dev	3.469

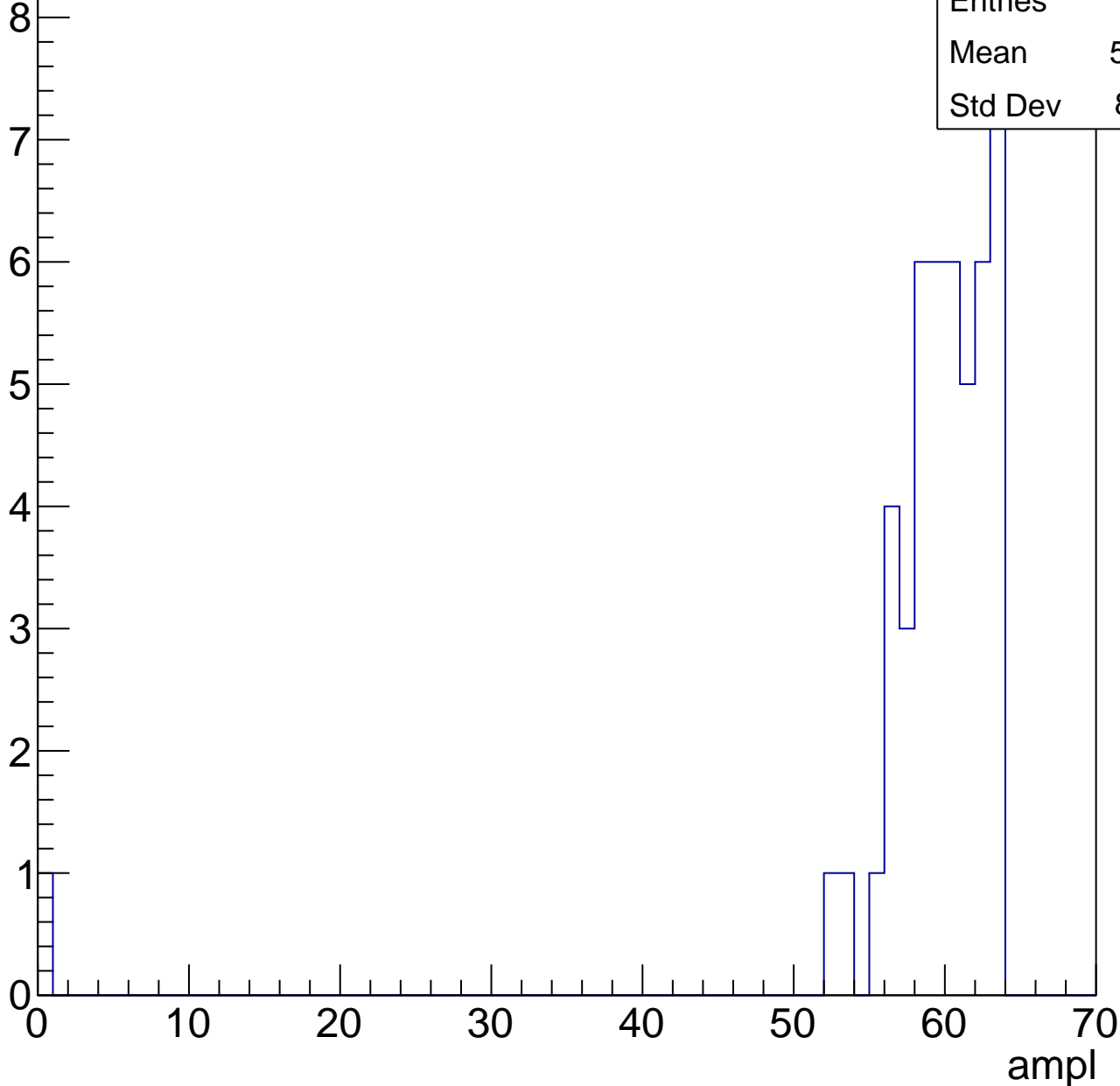


B1L103S, U7-ch13, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

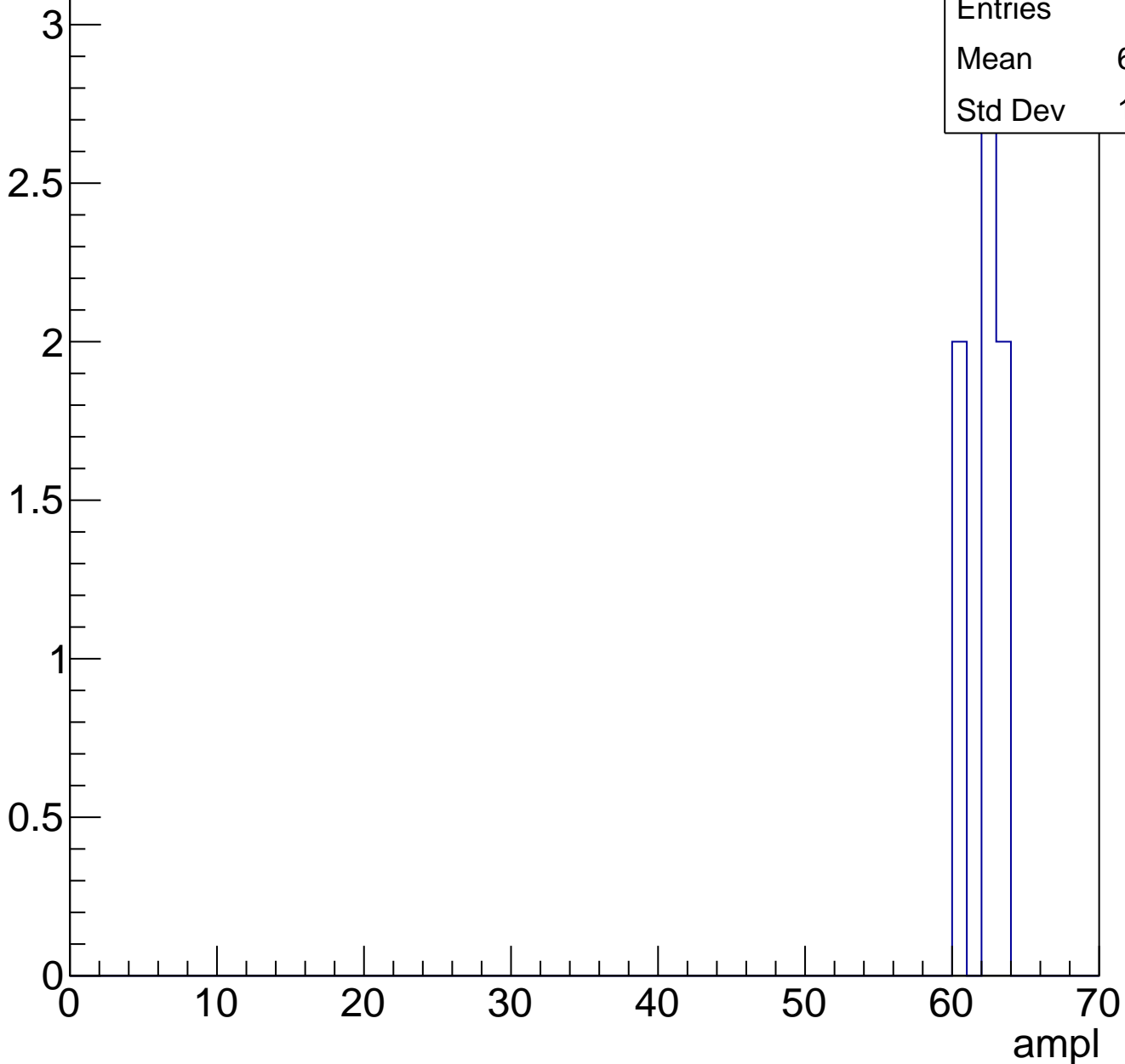
Entries	48
Mean	58.29
Std Dev	8.921



B1L103S, U7-ch13, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch13, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U7-ch14, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	22.11
Std Dev	11.77

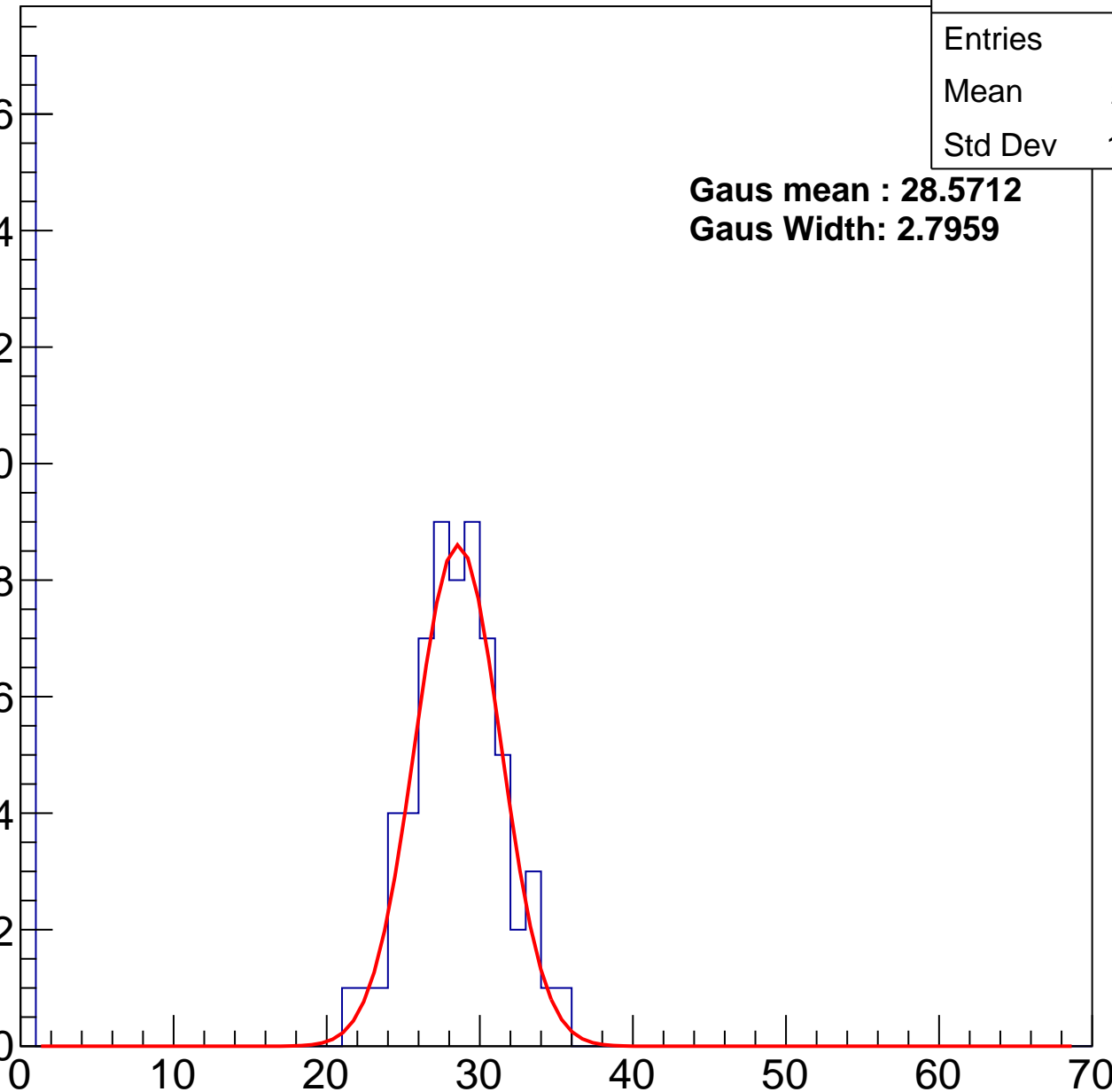
Gaus mean : 28.5712

Gaus Width: 2.7959

Entry

16
14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch14, adc1

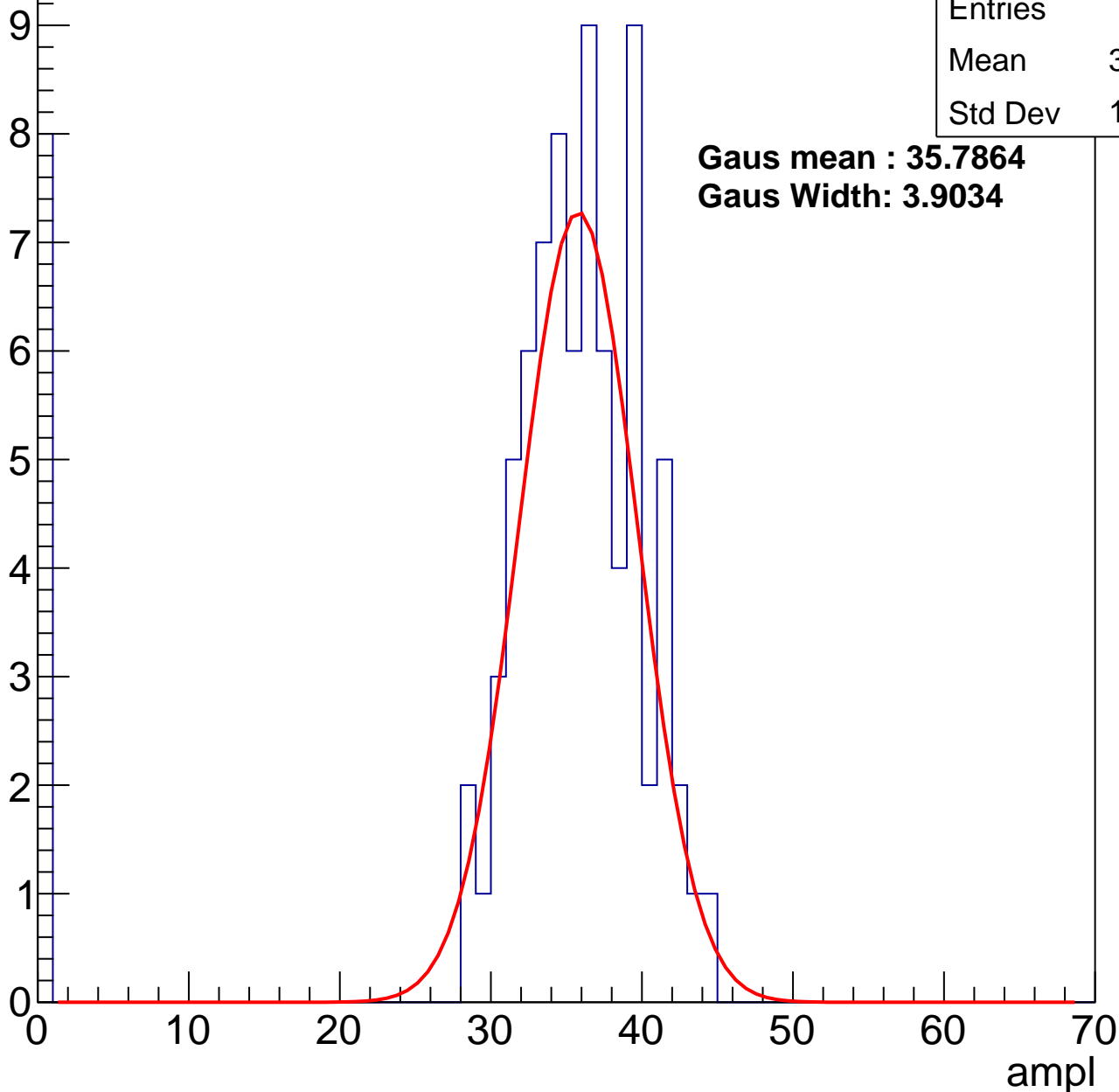
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	85
Mean	32.24
Std Dev	10.96

Gaus mean : 35.7864

Gaus Width: 3.9034



B1L103S, U7-ch14, adc2

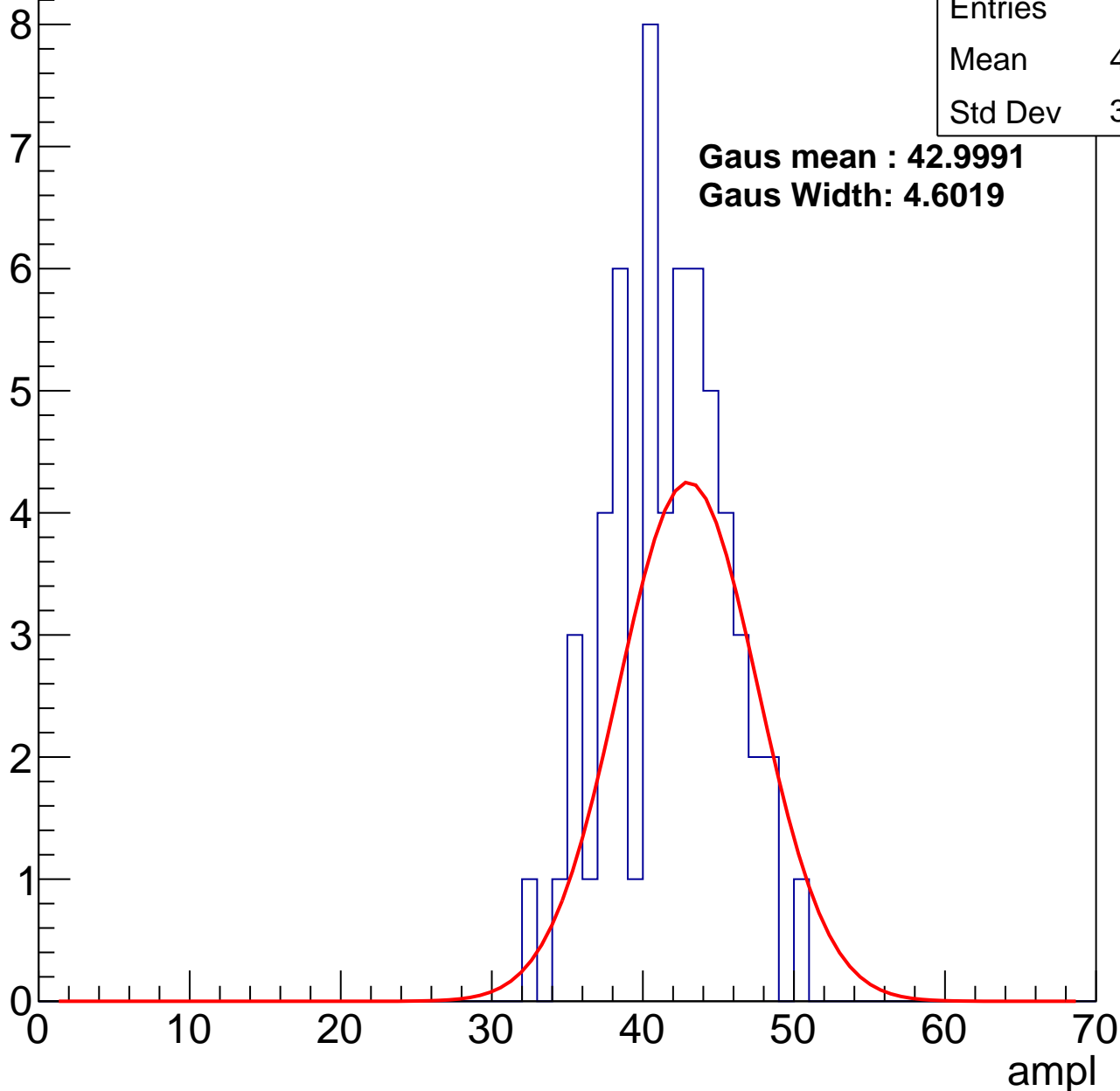
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	41.28
Std Dev	3.836

Gaus mean : 42.9991

Gaus Width: 4.6019

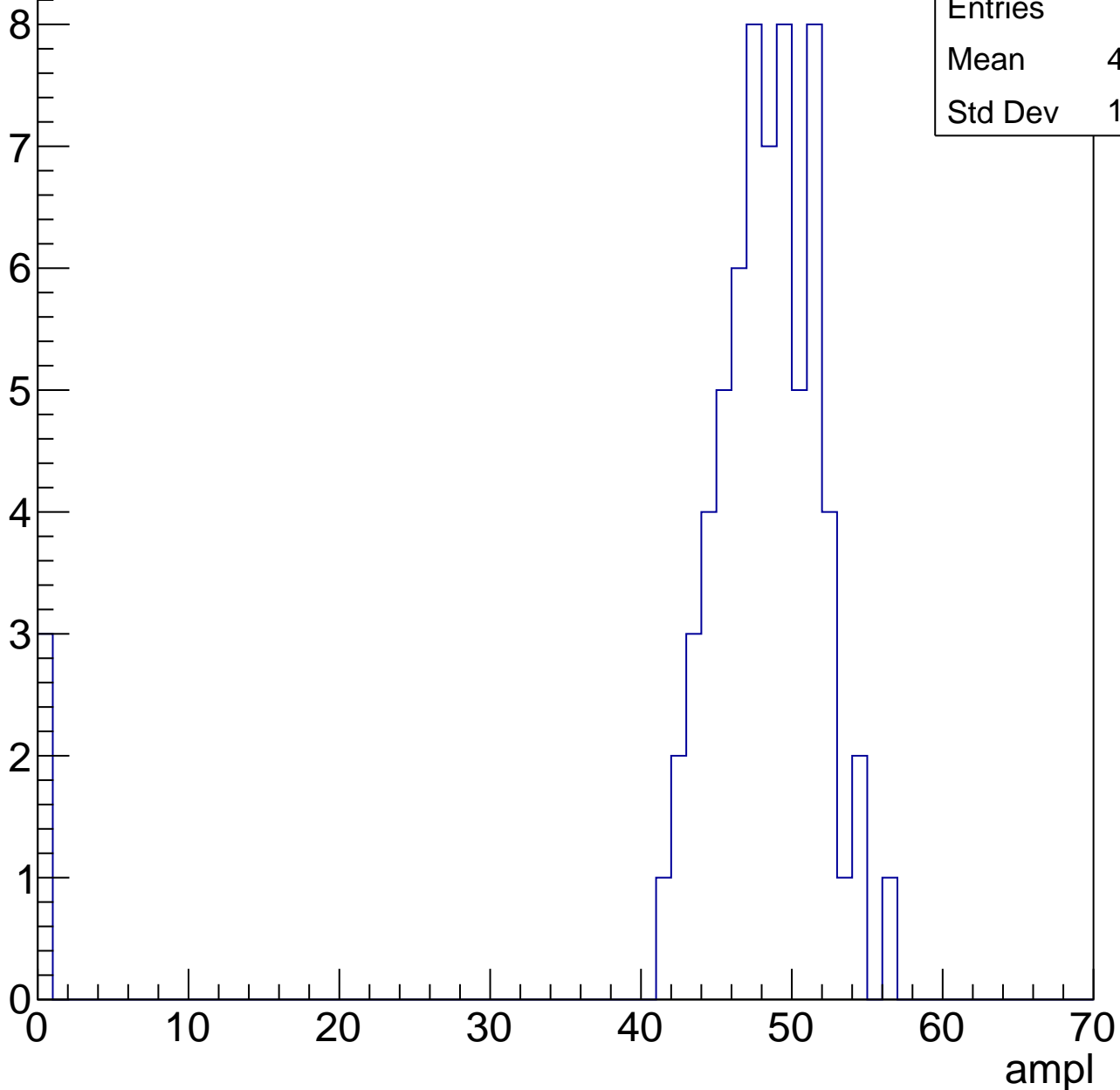


B1L103S, U7-ch14, adc3

calib_packv5_041523_1651.root, FC#0, port C2

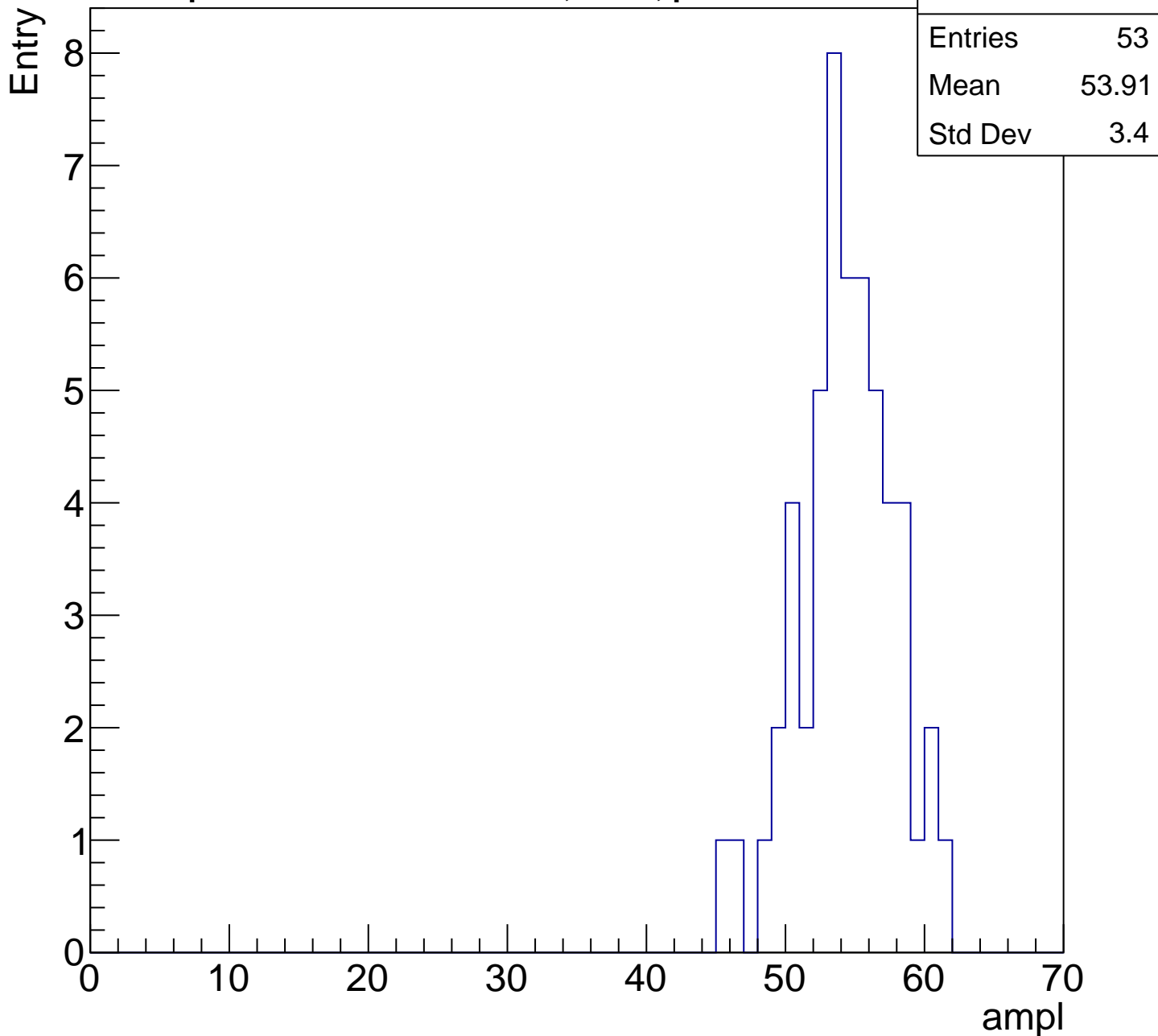
Entry

Entries	68
Mean	45.85
Std Dev	10.33



B1L103S, U7-ch14, adc4

calib_packv5_041523_1651.root, FC#0, port C2

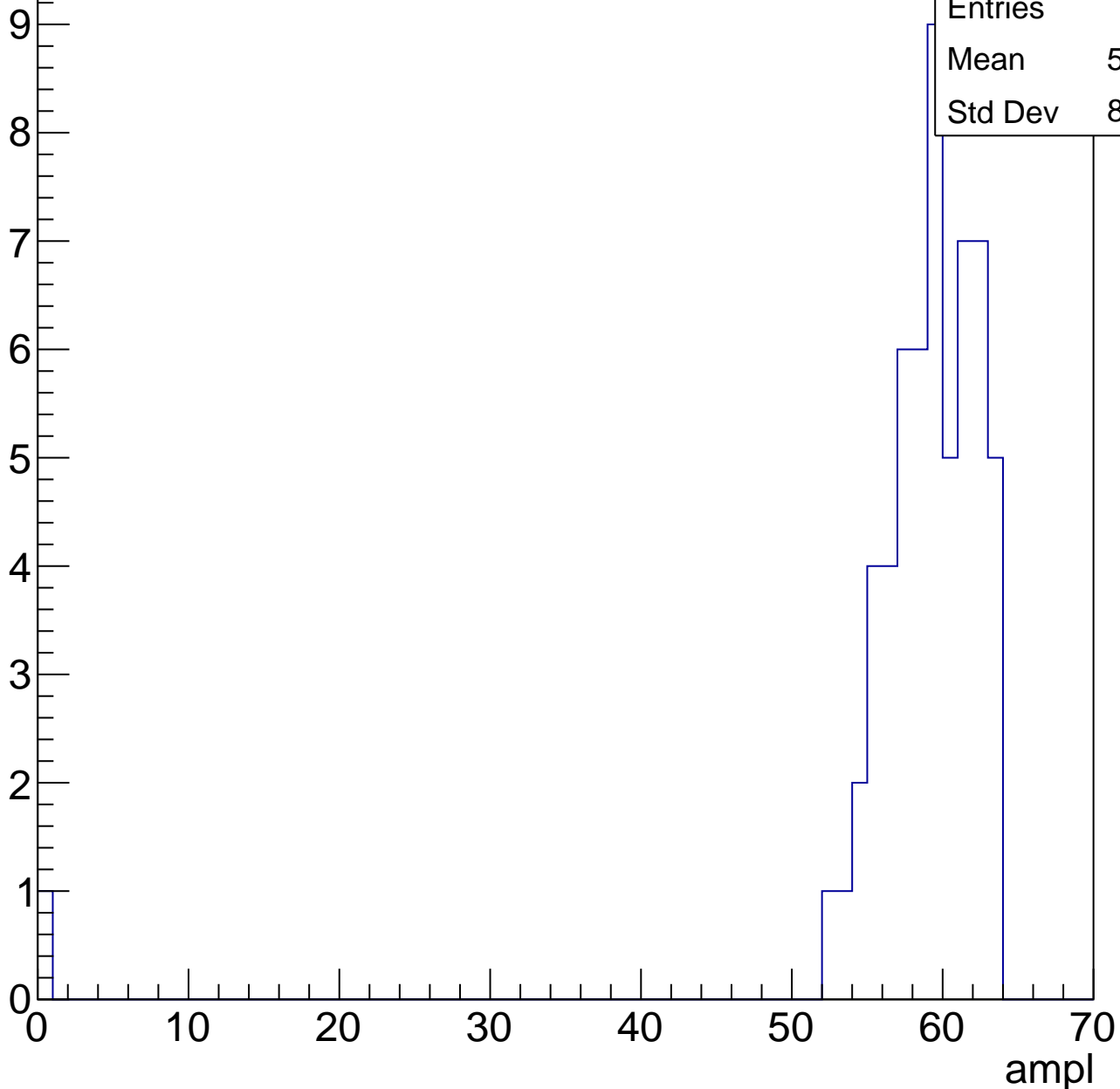


B1L103S, U7-ch14, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

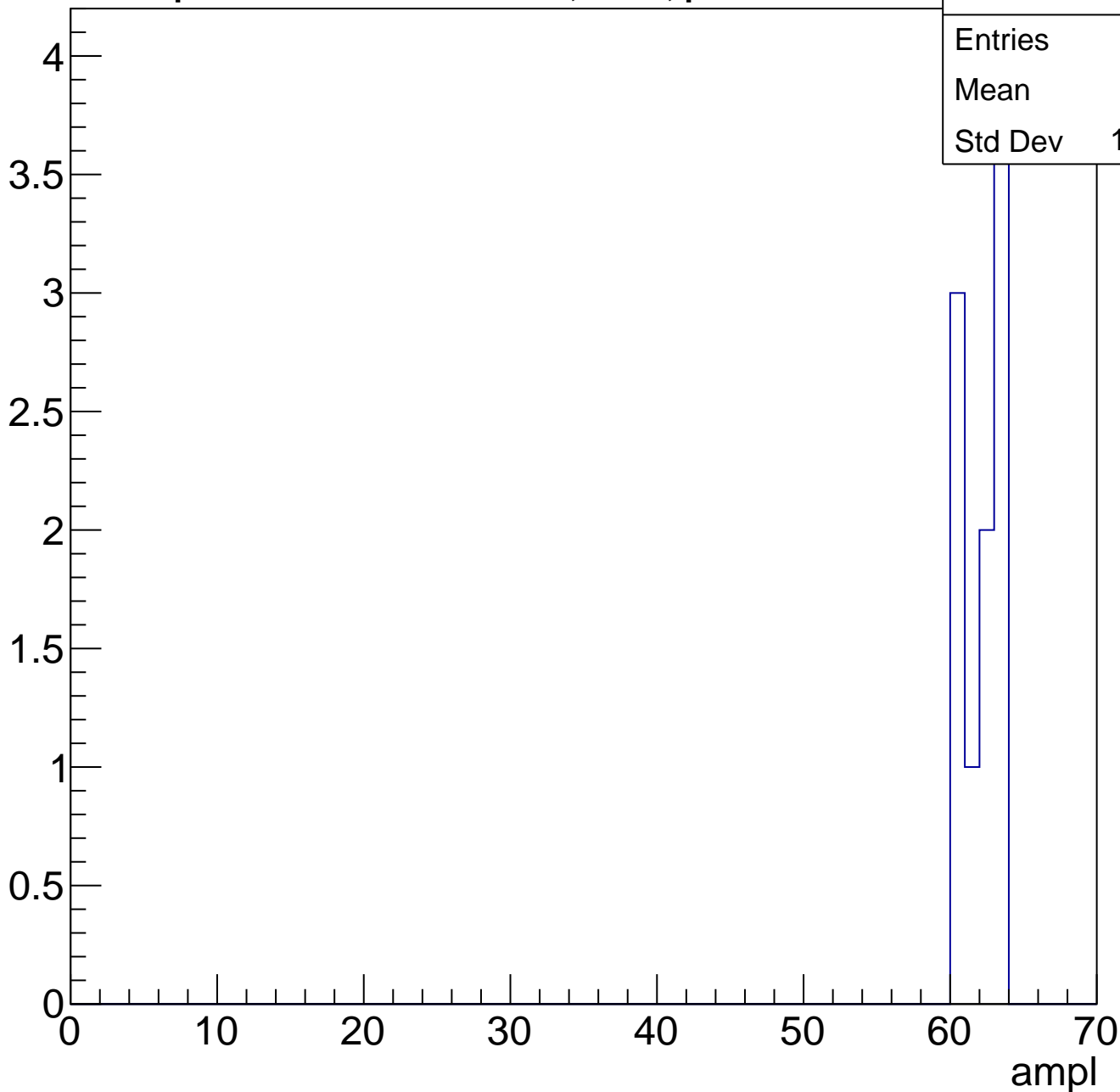
Entries	58
Mean	57.83
Std Dev	8.139



B1L103S, U7-ch14, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



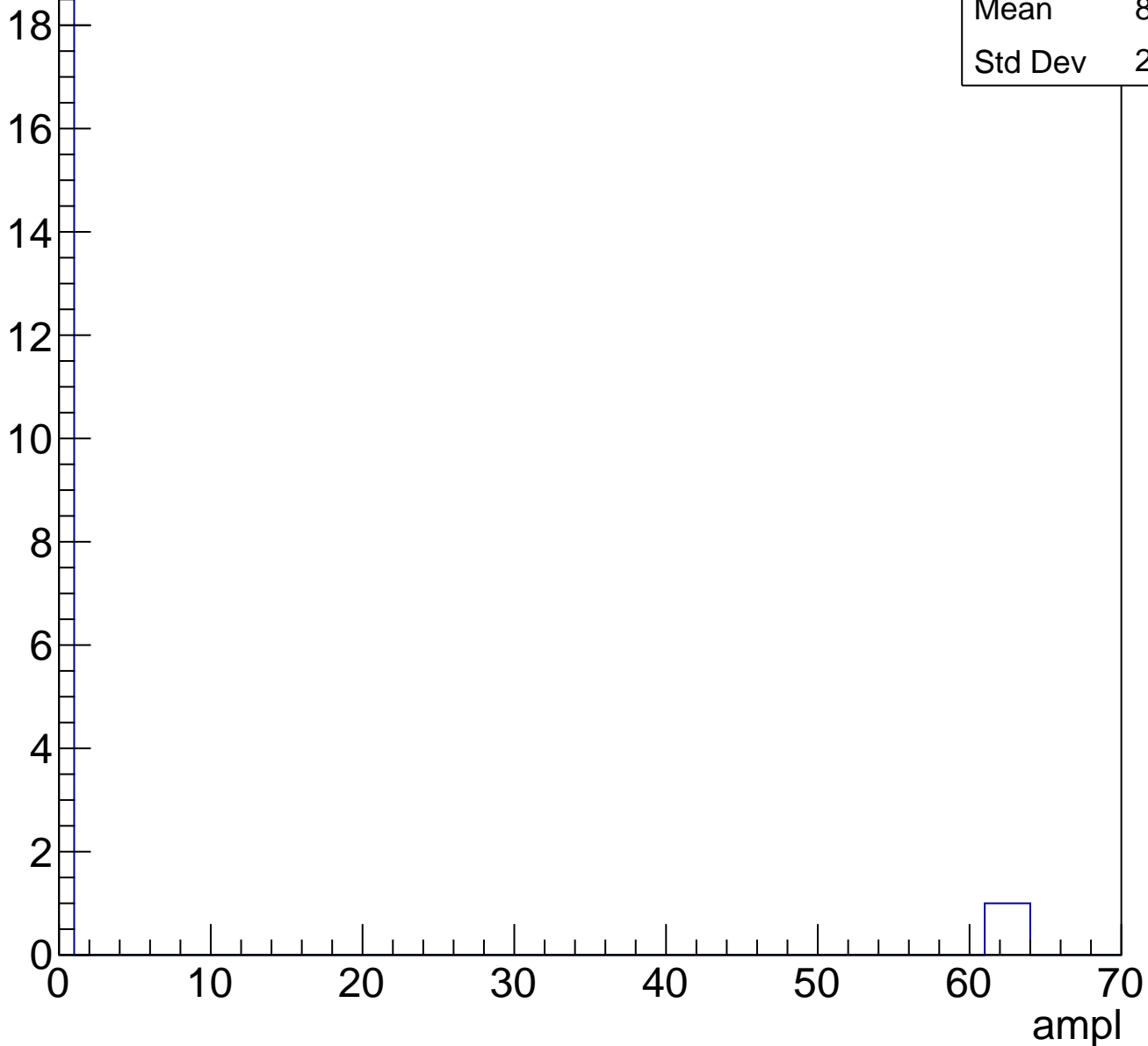
Entries	10
Mean	61.7
Std Dev	1.269

B1L103S, U7-ch14, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	22
Mean	8.455
Std Dev	21.28

Entry



B1L103S, U7-ch15, adc0

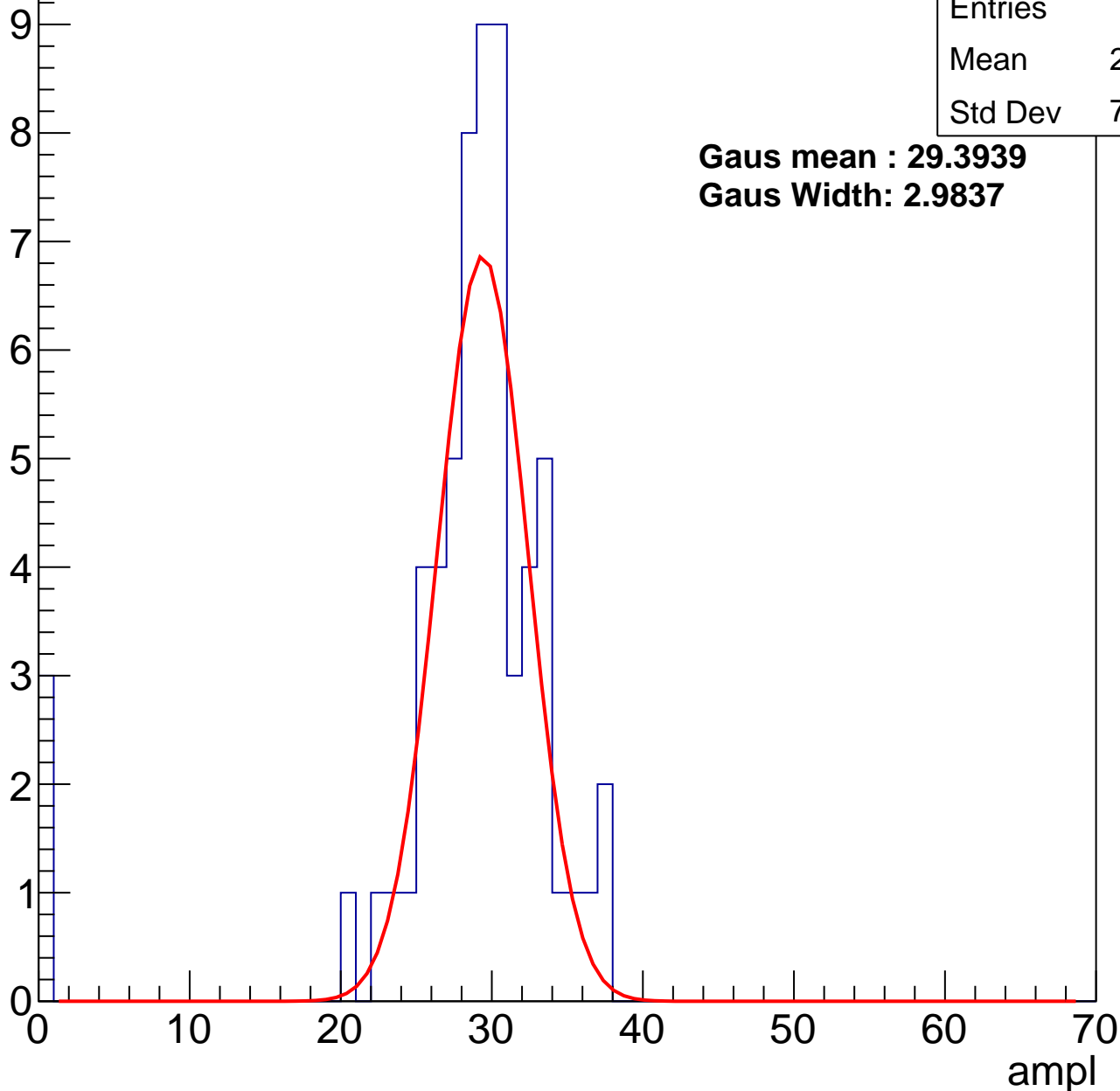
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	27.75
Std Dev	7.035

Gaus mean : 29.3939

Gaus Width: 2.9837



B1L103S, U7-ch15, adc1

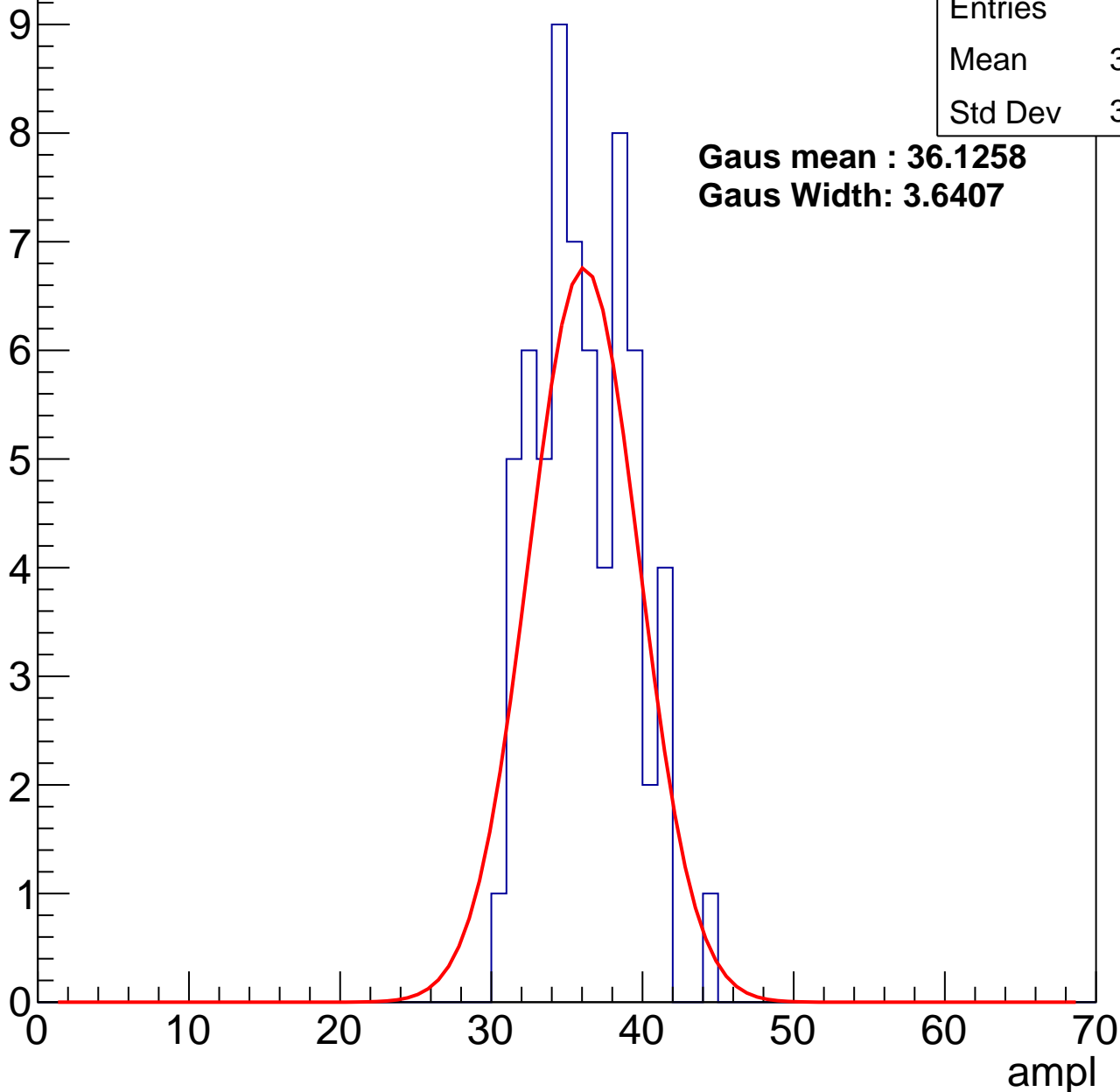
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	35.67
Std Dev	3.123

Gaus mean : 36.1258

Gaus Width: 3.6407



B1L103S, U7-ch15, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	78
Mean	37.91
Std Dev	13.26

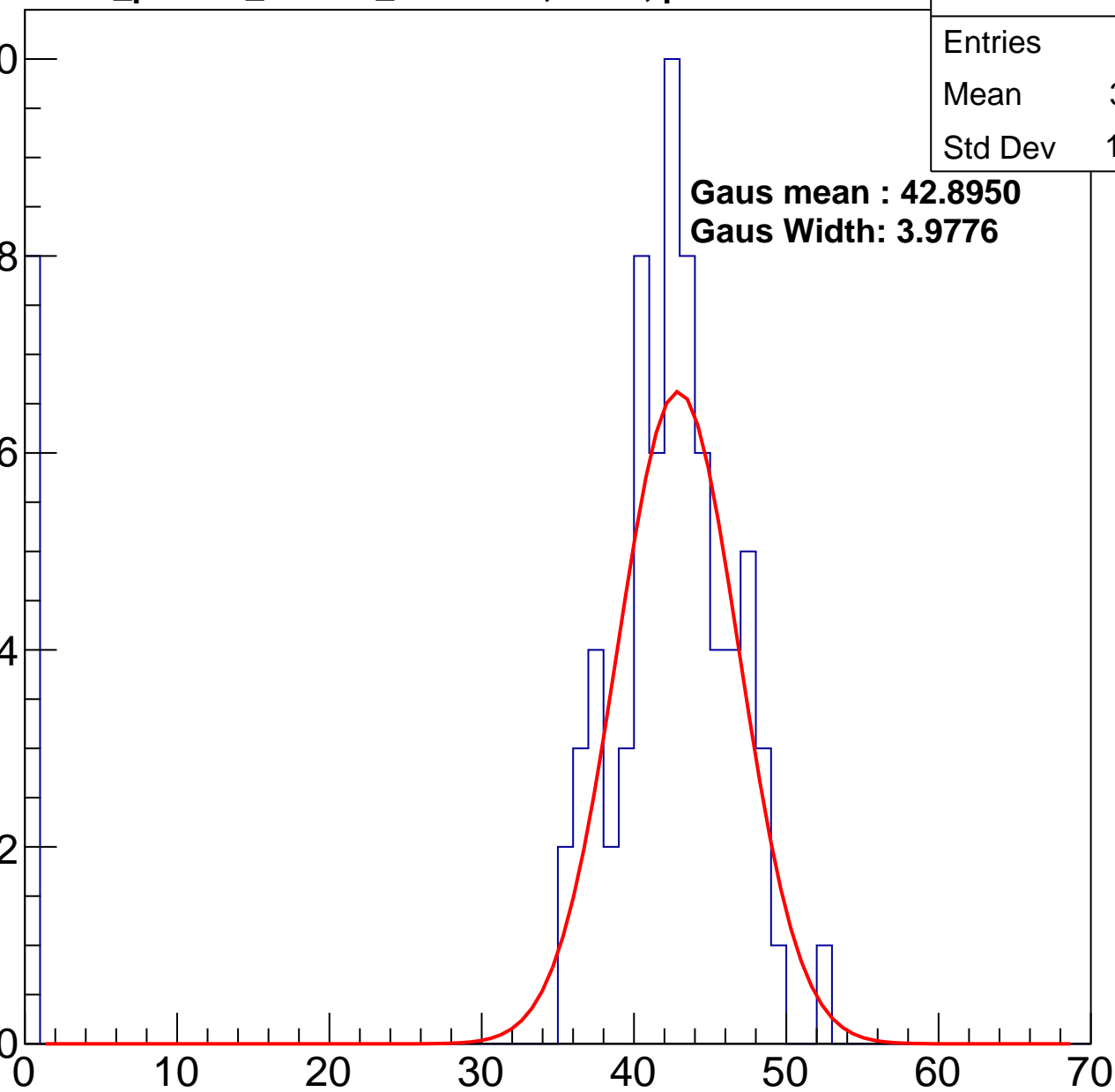
Gaus mean : 42.8950

Gaus Width: 3.9776

Entry

10
8
6
4
2
0

ampl

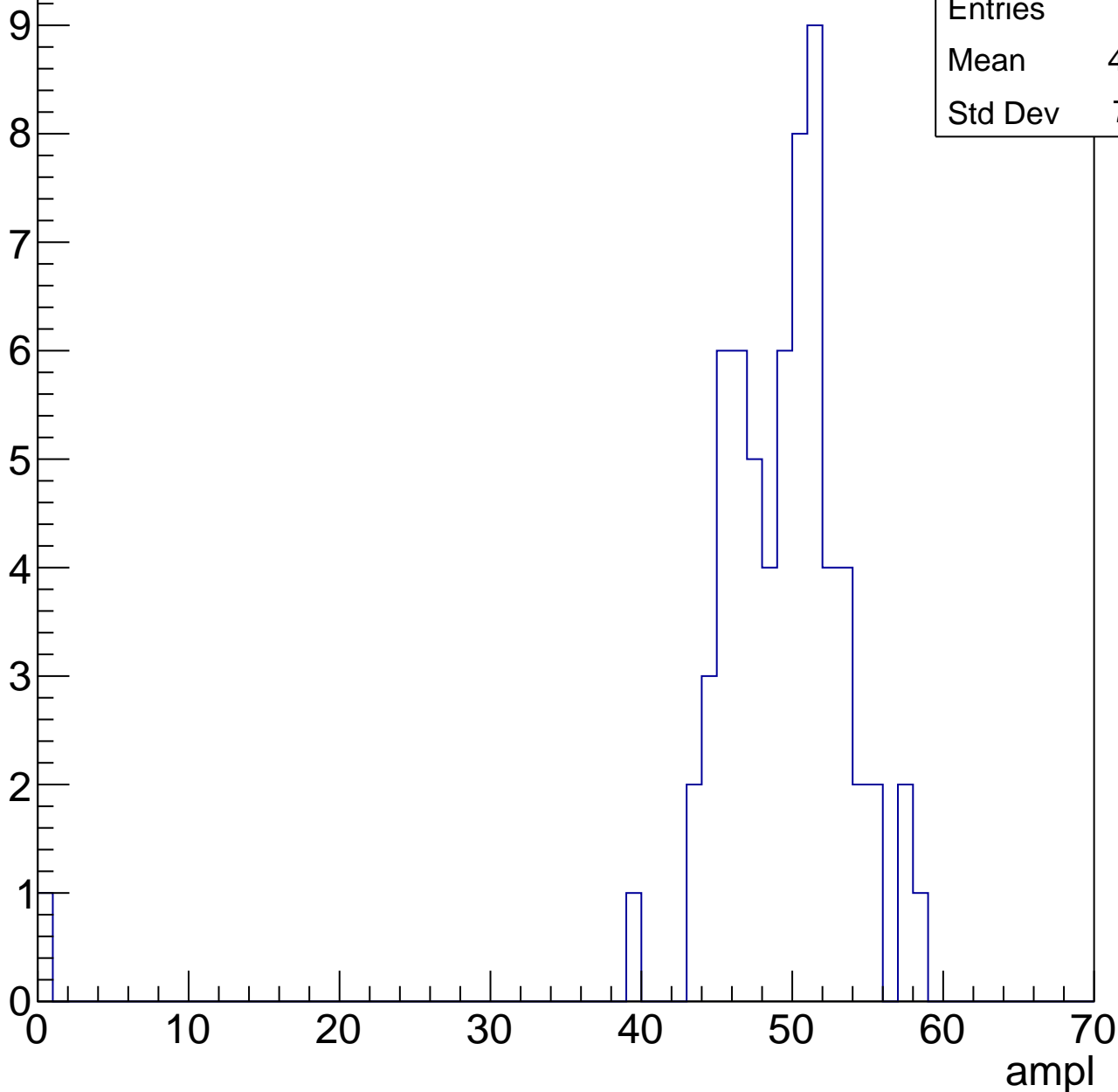


B1L103S, U7-ch15, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	48.38
Std Dev	7.041

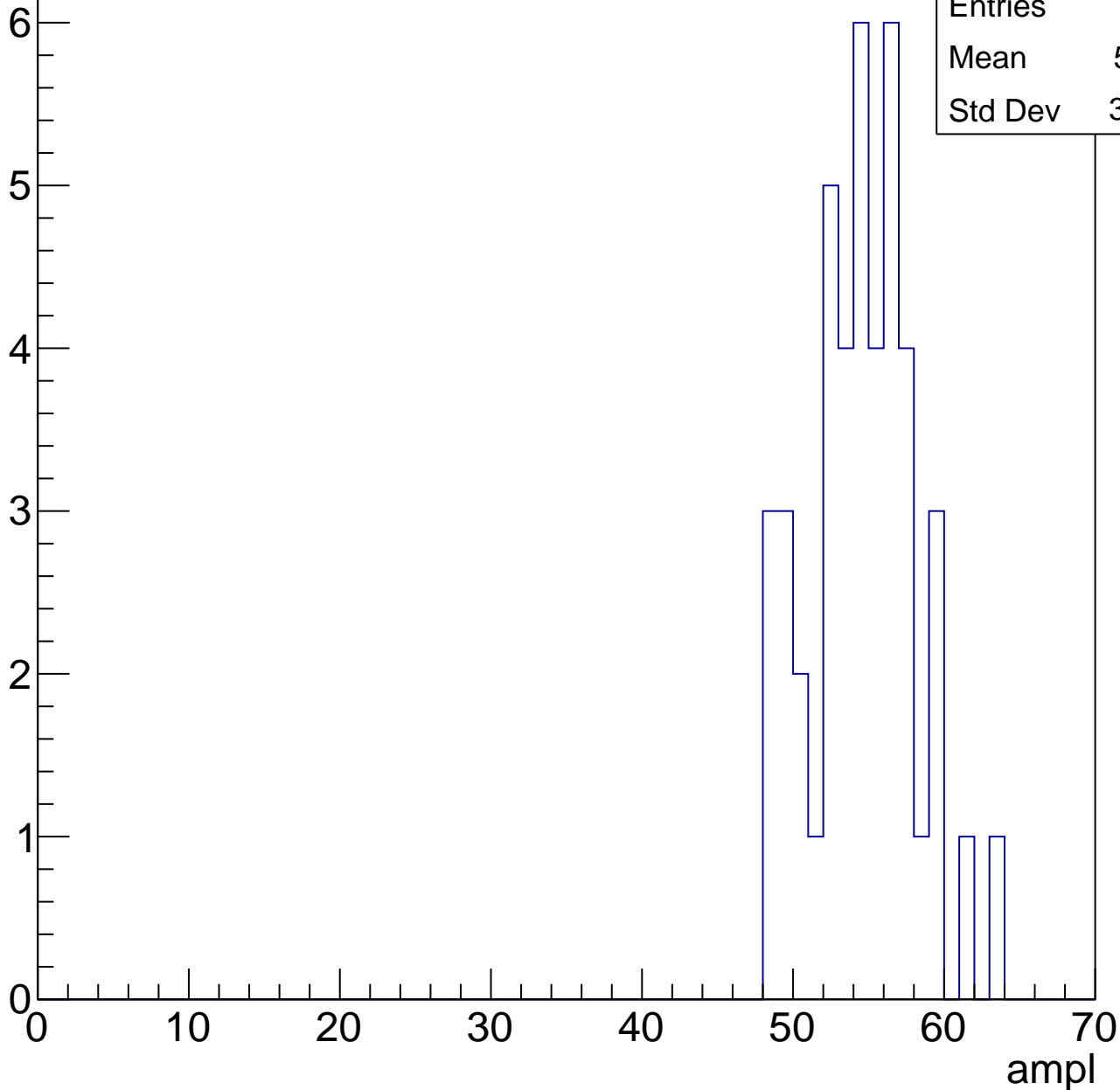


B1L103S, U7-ch15, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	44
Mean	54.11
Std Dev	3.479

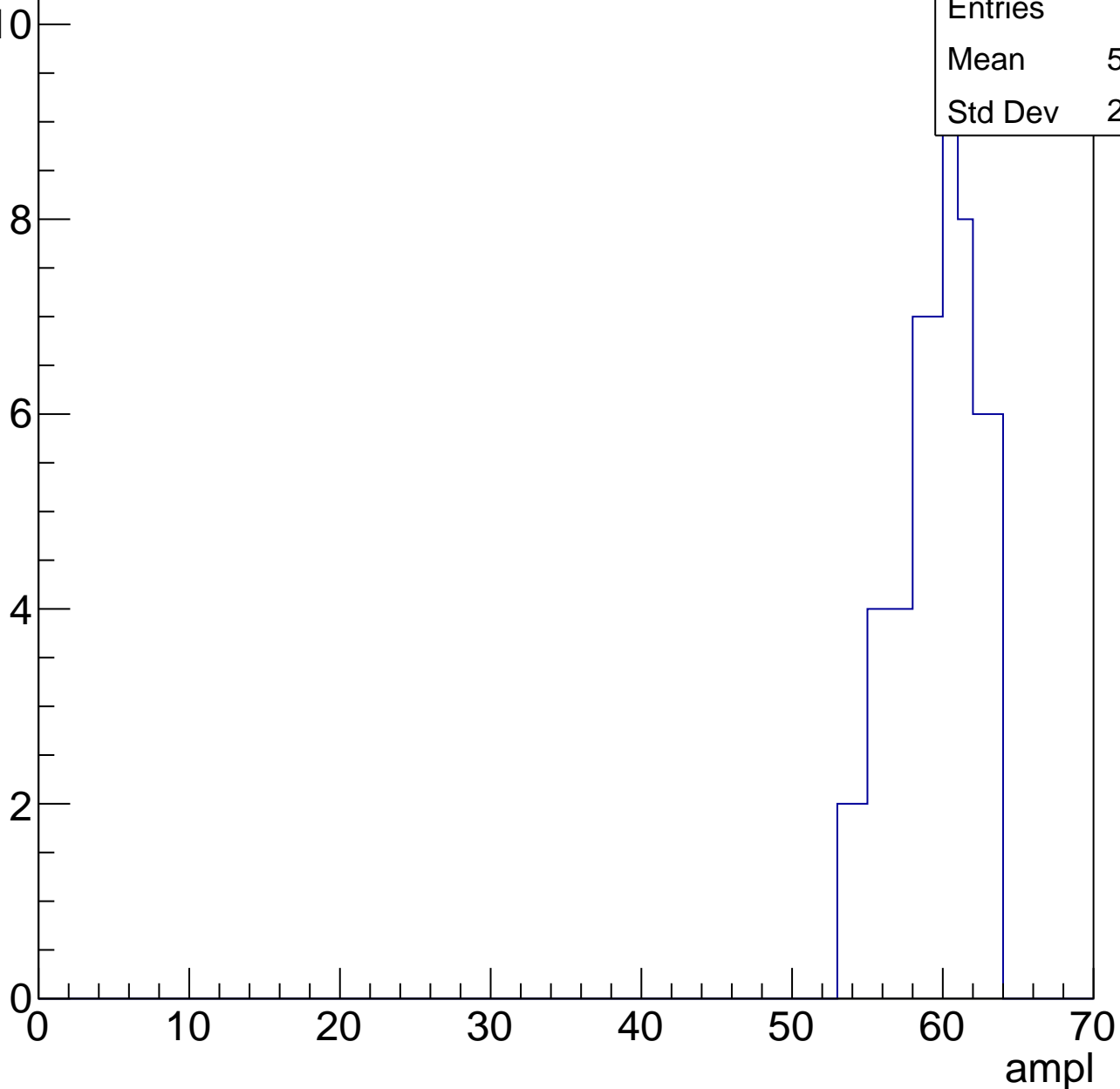


B1L103S, U7-ch15, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

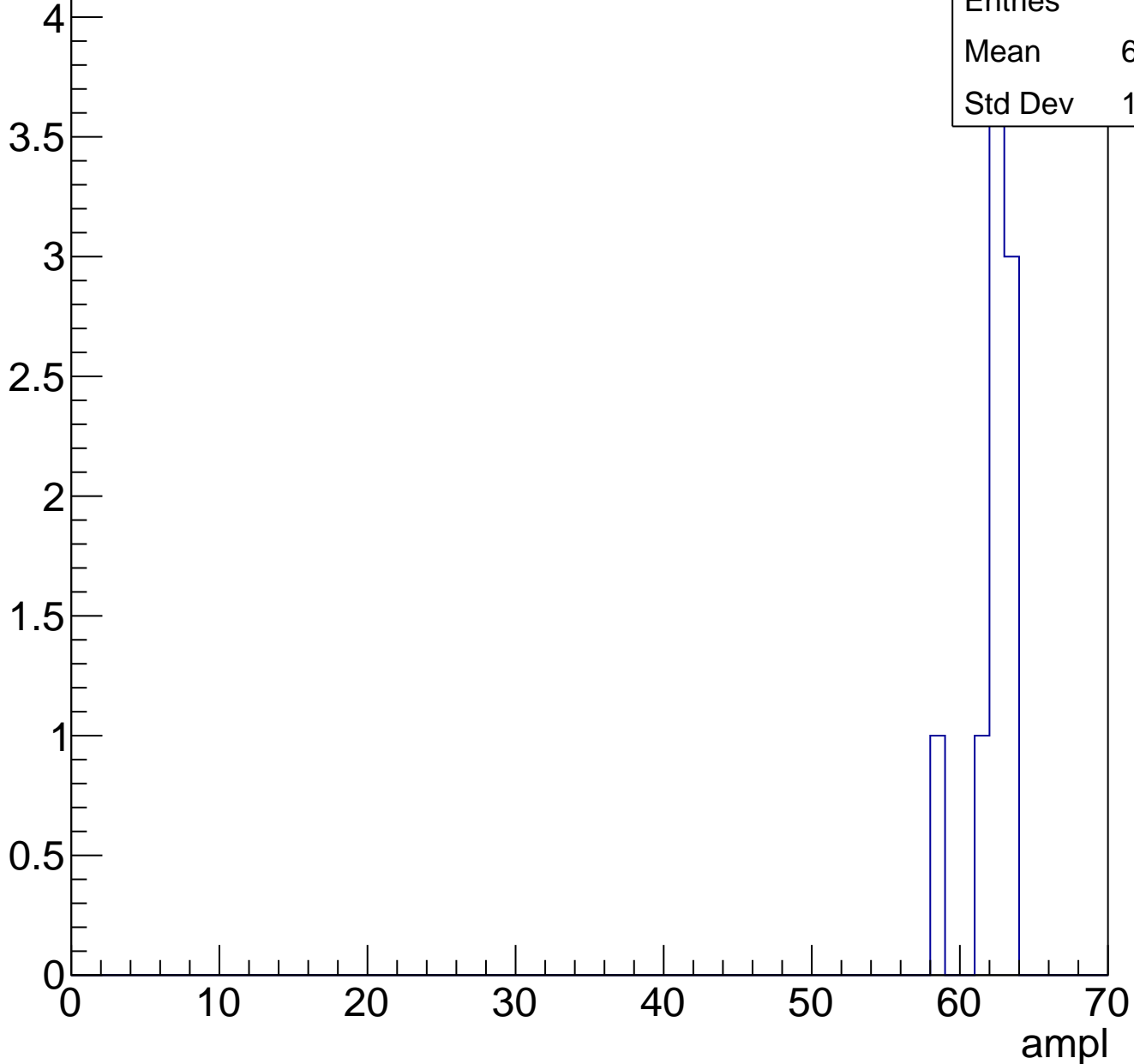
Entries	60
Mean	59.05
Std Dev	2.698



B1L103S, U7-ch15, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

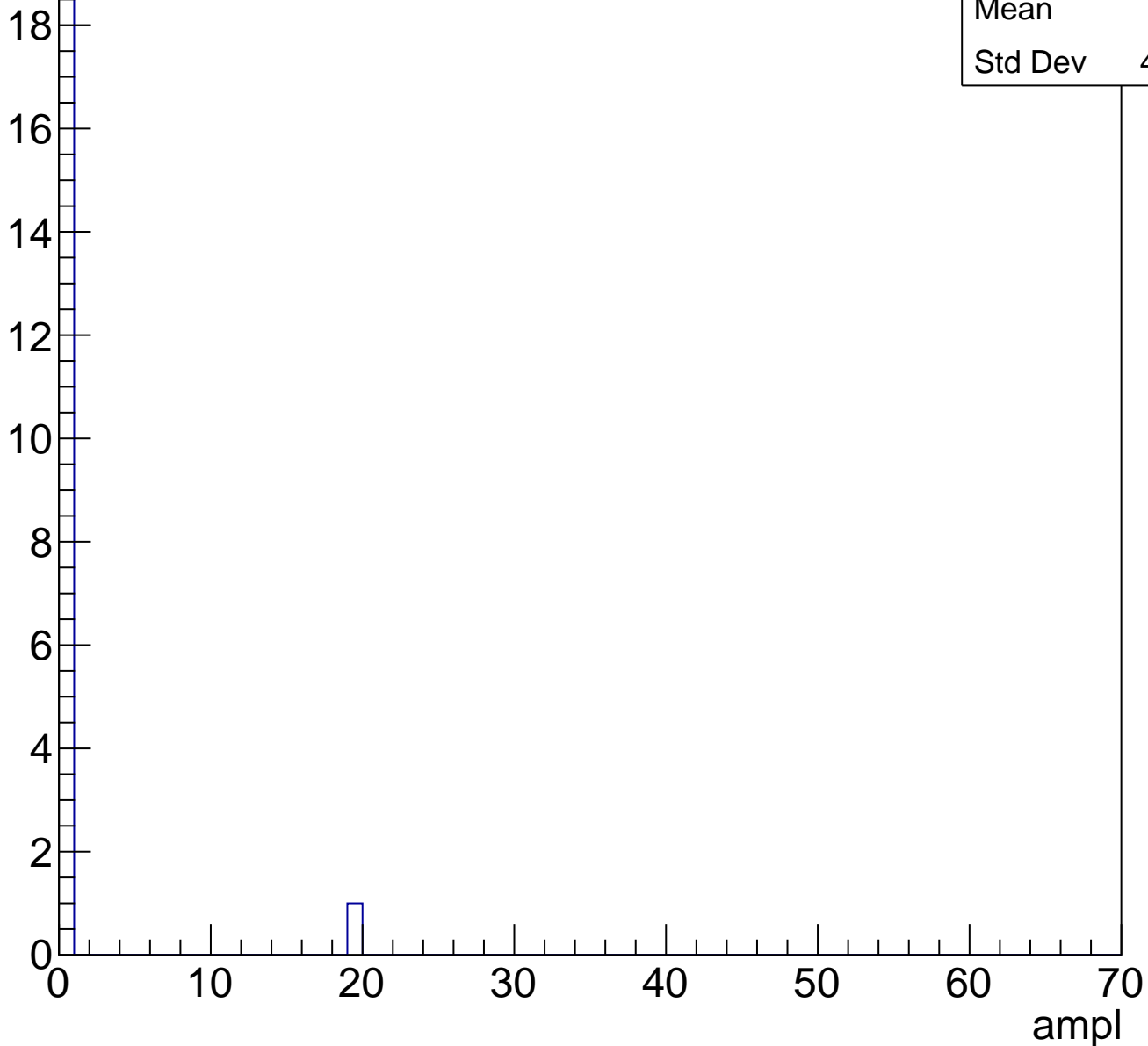


B1L103S, U7-ch15, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	0.95
Std Dev	4.141

Entry



B1L103S, U7-ch16, adc0

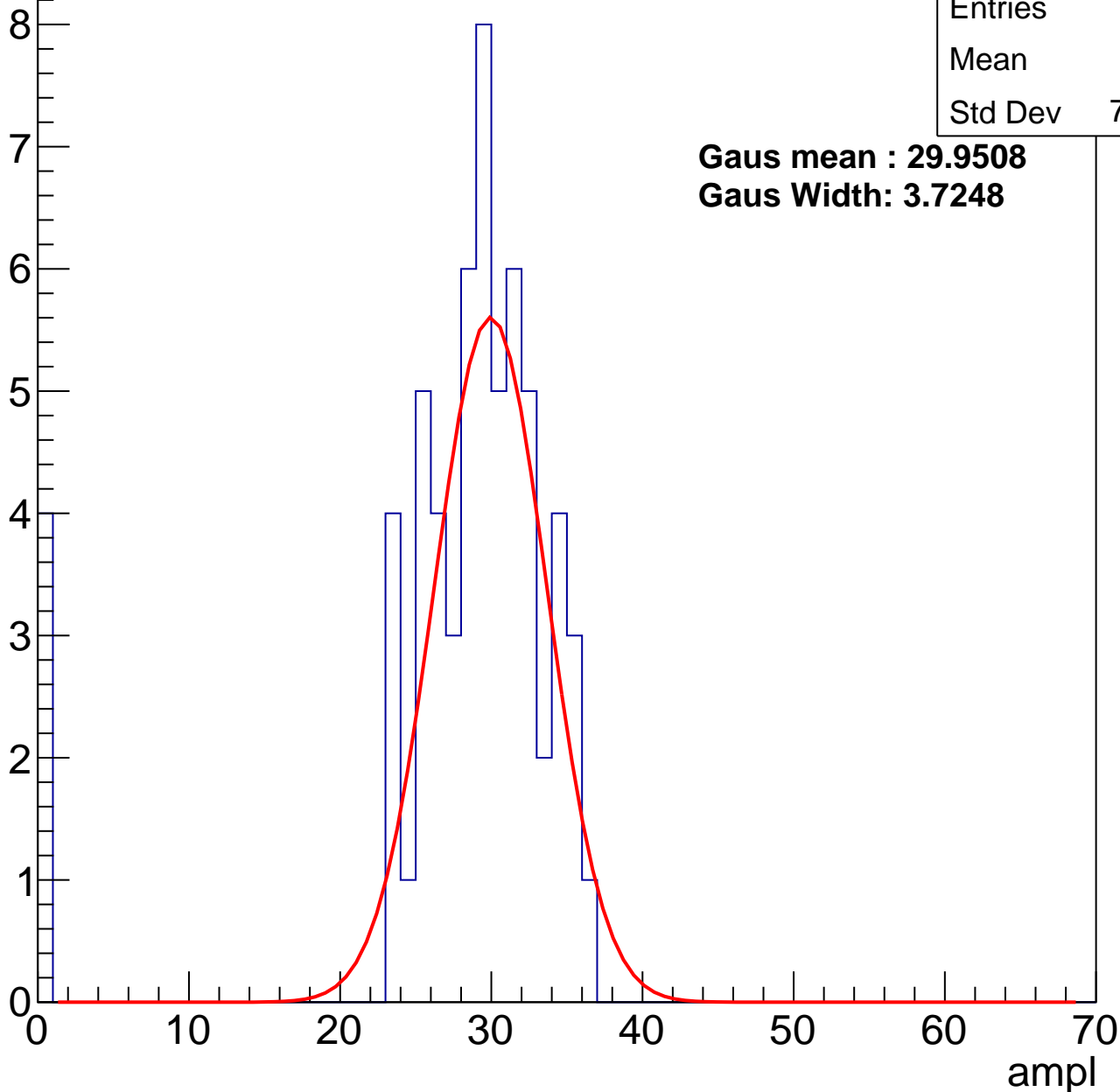
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	27.3
Std Dev	7.947

Gaus mean : 29.9508

Gaus Width: 3.7248



B1L103S, U7-ch16, adc1

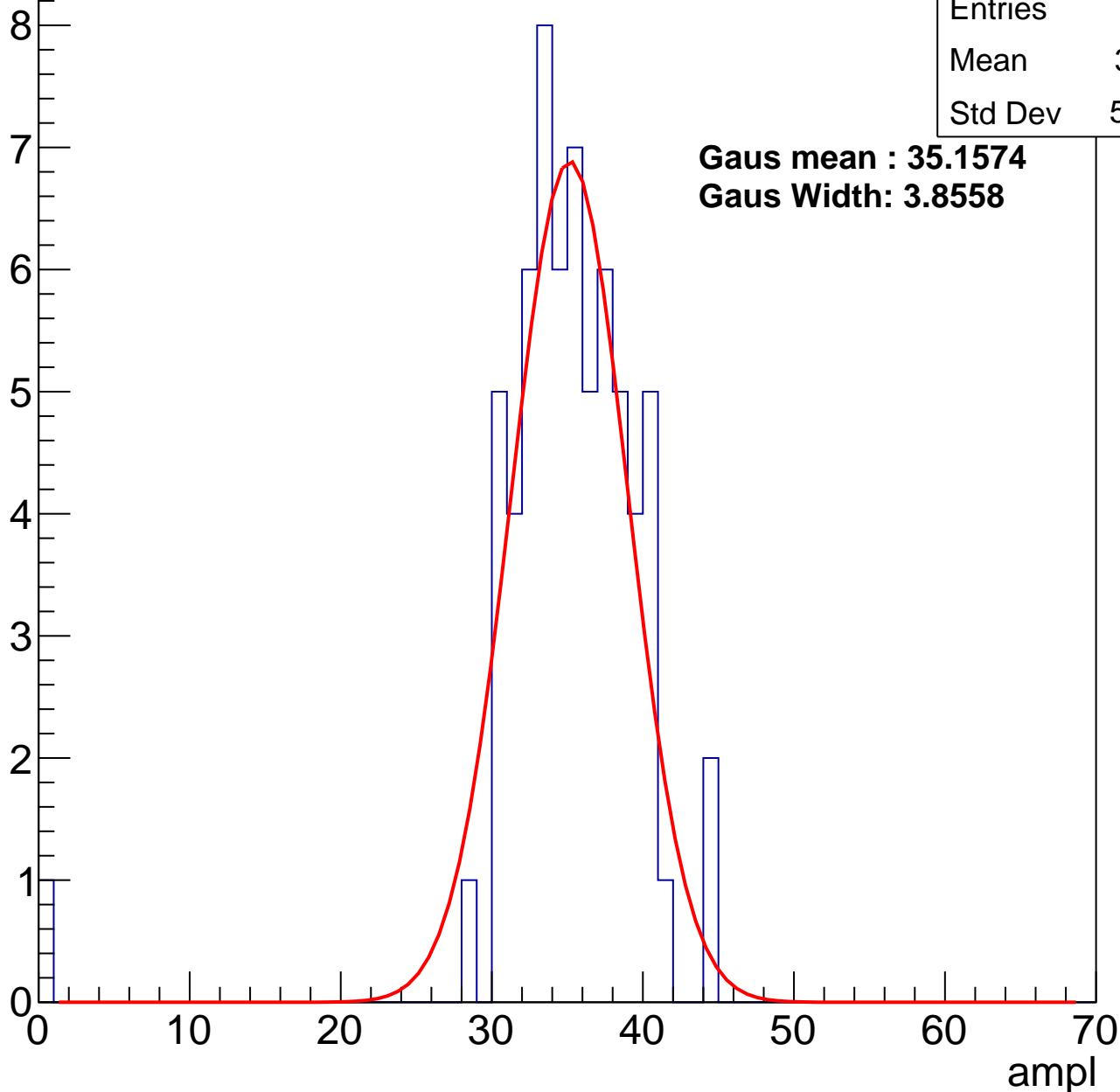
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	34.61
Std Dev	5.513

Gaus mean : 35.1574

Gaus Width: 3.8558



B1L103S, U7-ch16, adc2

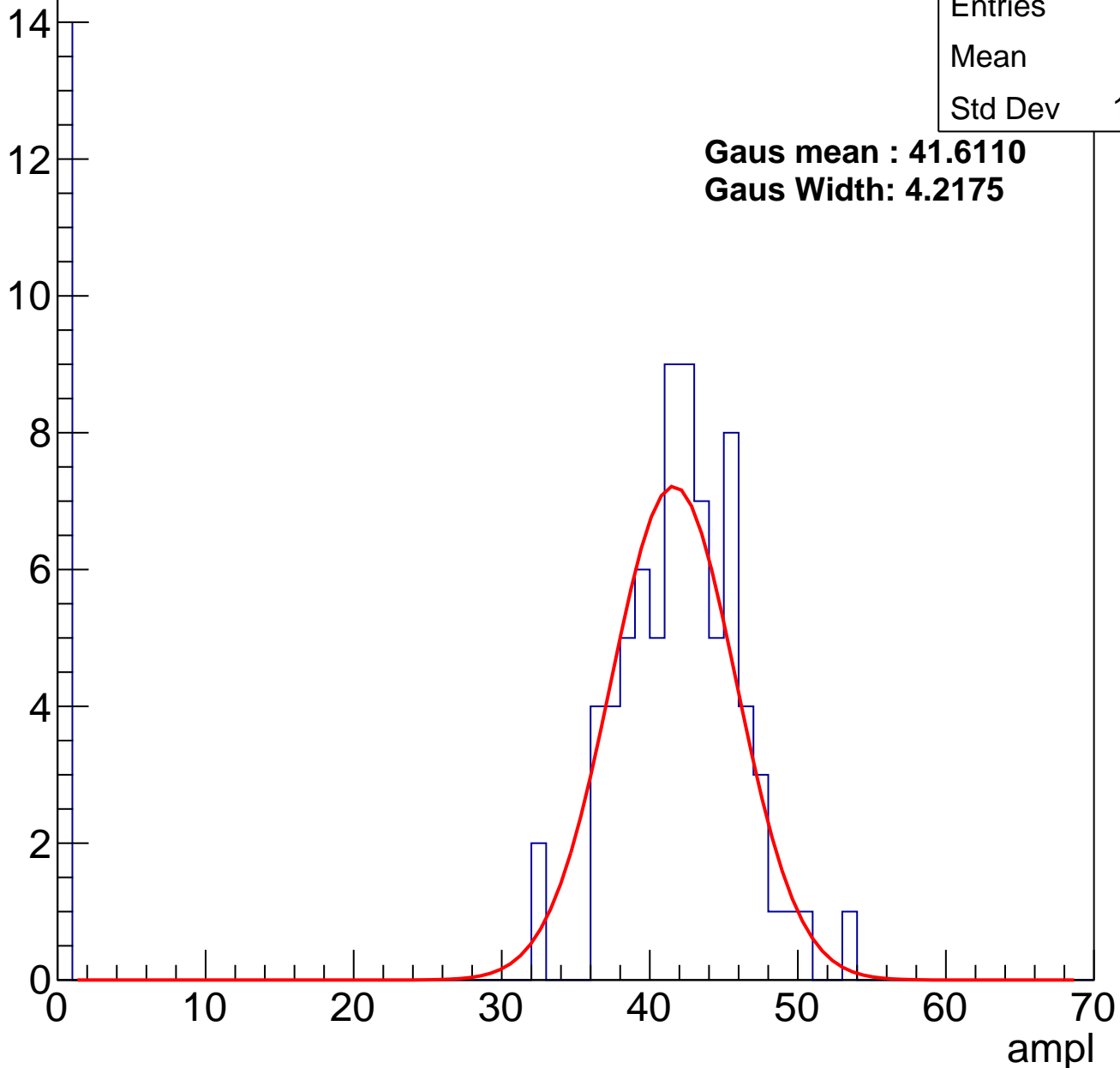
calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	35.2
Std Dev	15.61

Gaus mean : 41.6110

Gaus Width: 4.2175

Entry

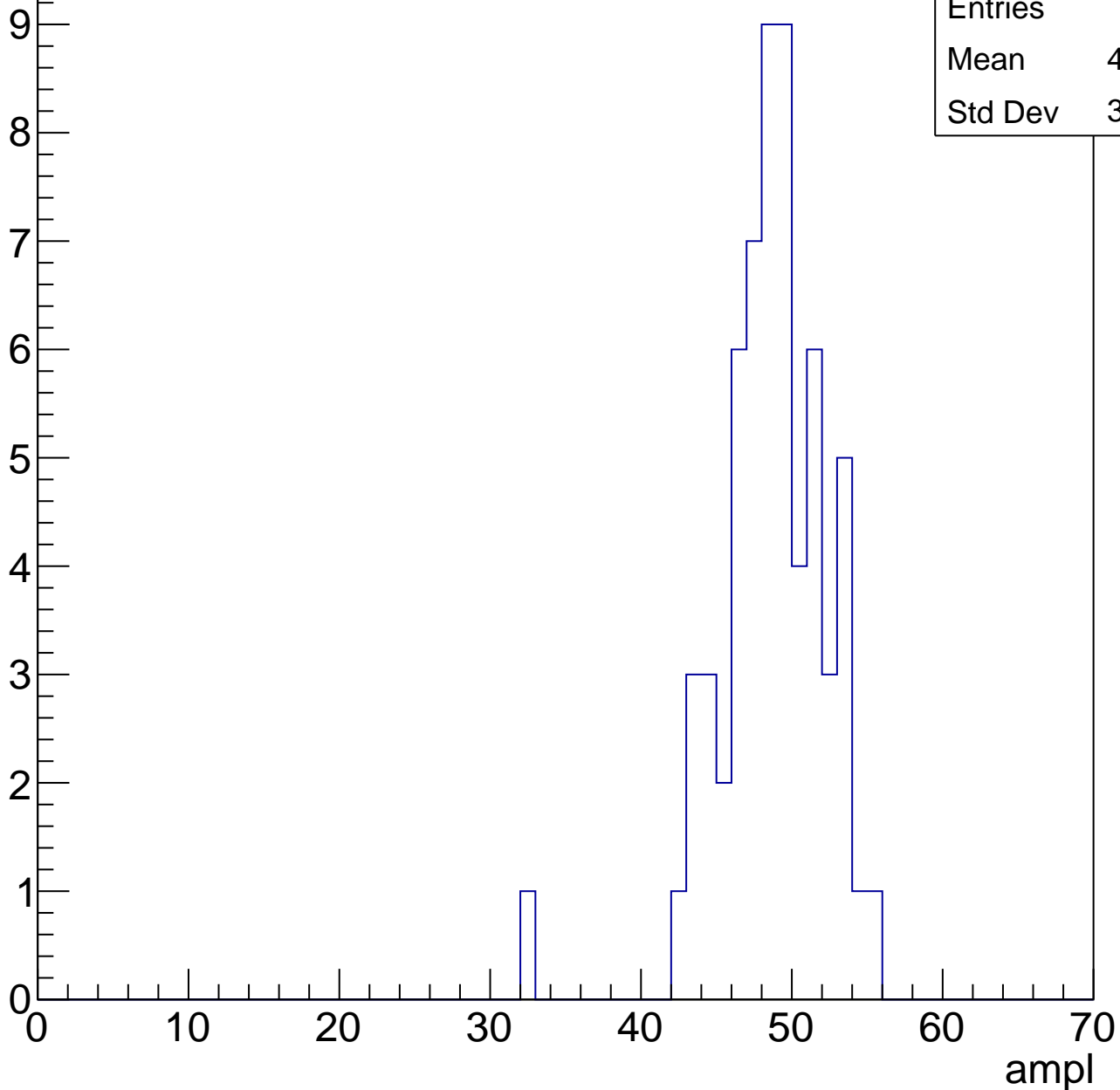


B1L103S, U7-ch16, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

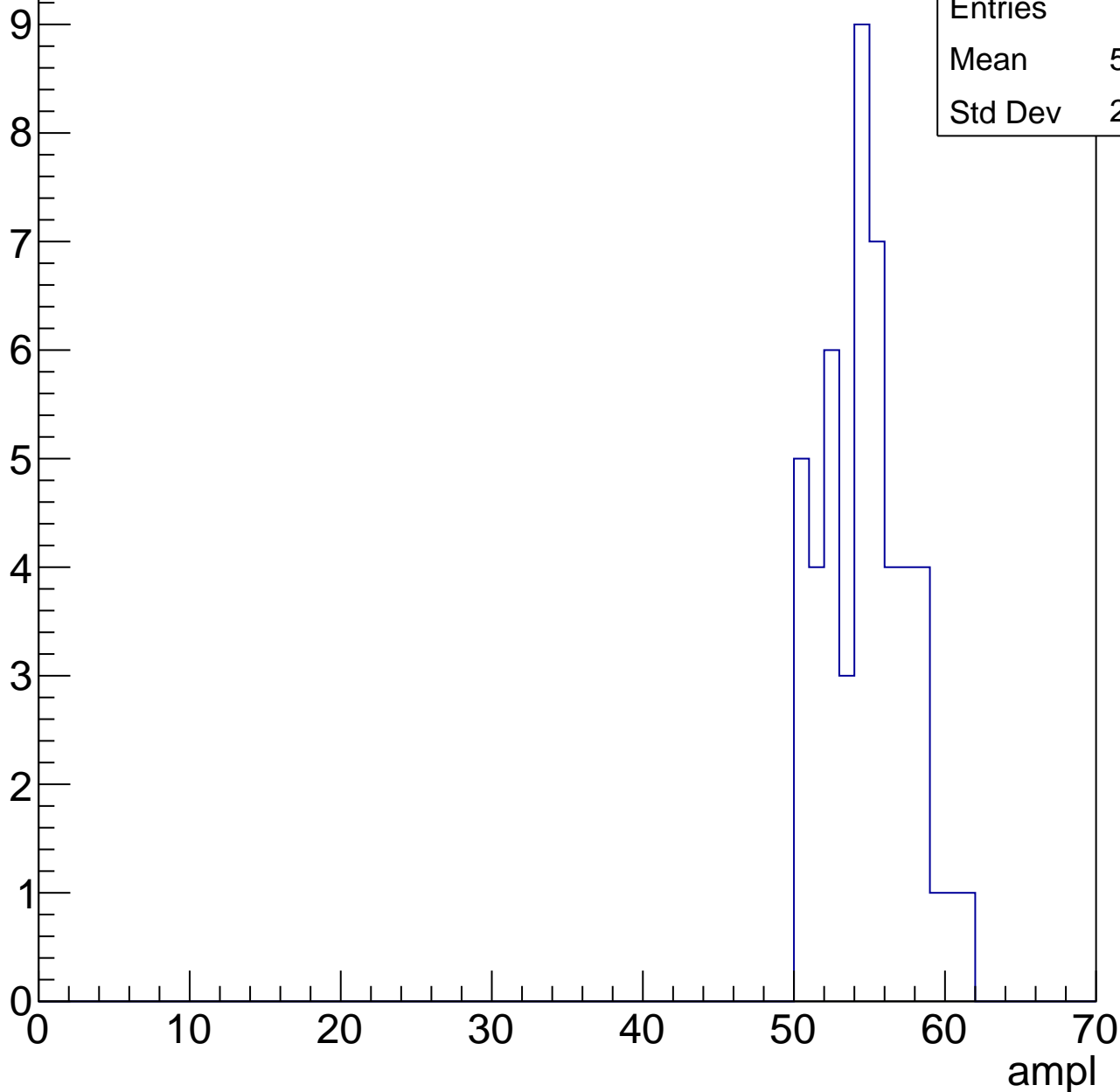
Entries	61
Mean	48.18
Std Dev	3.619



B1L103S, U7-ch16, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

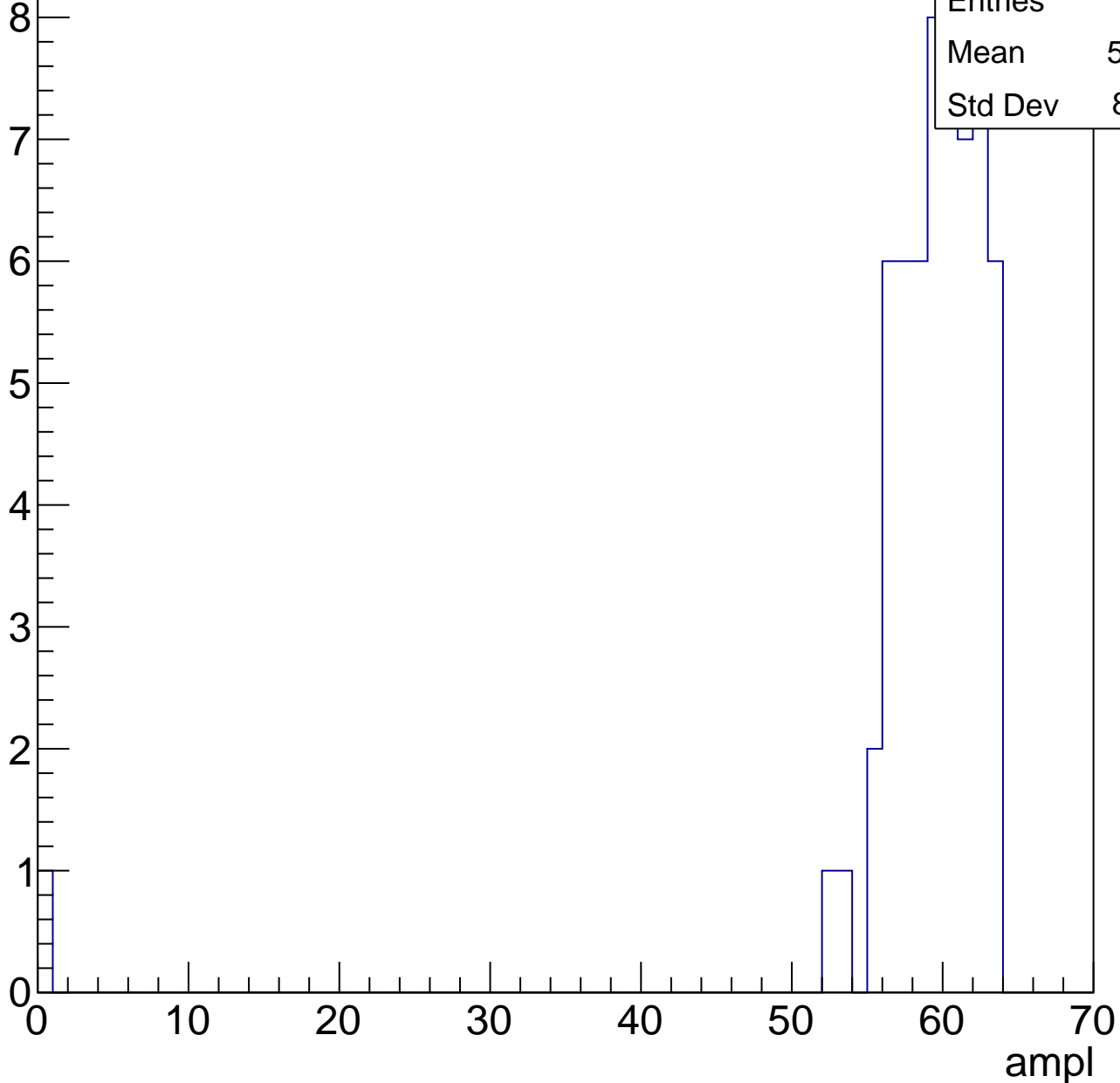


B1L103S, U7-ch16, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	58.23
Std Dev	8.011



B1L103S, U7-ch16, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

Entries

9

Mean

61.56

Std Dev

1.343

ampl

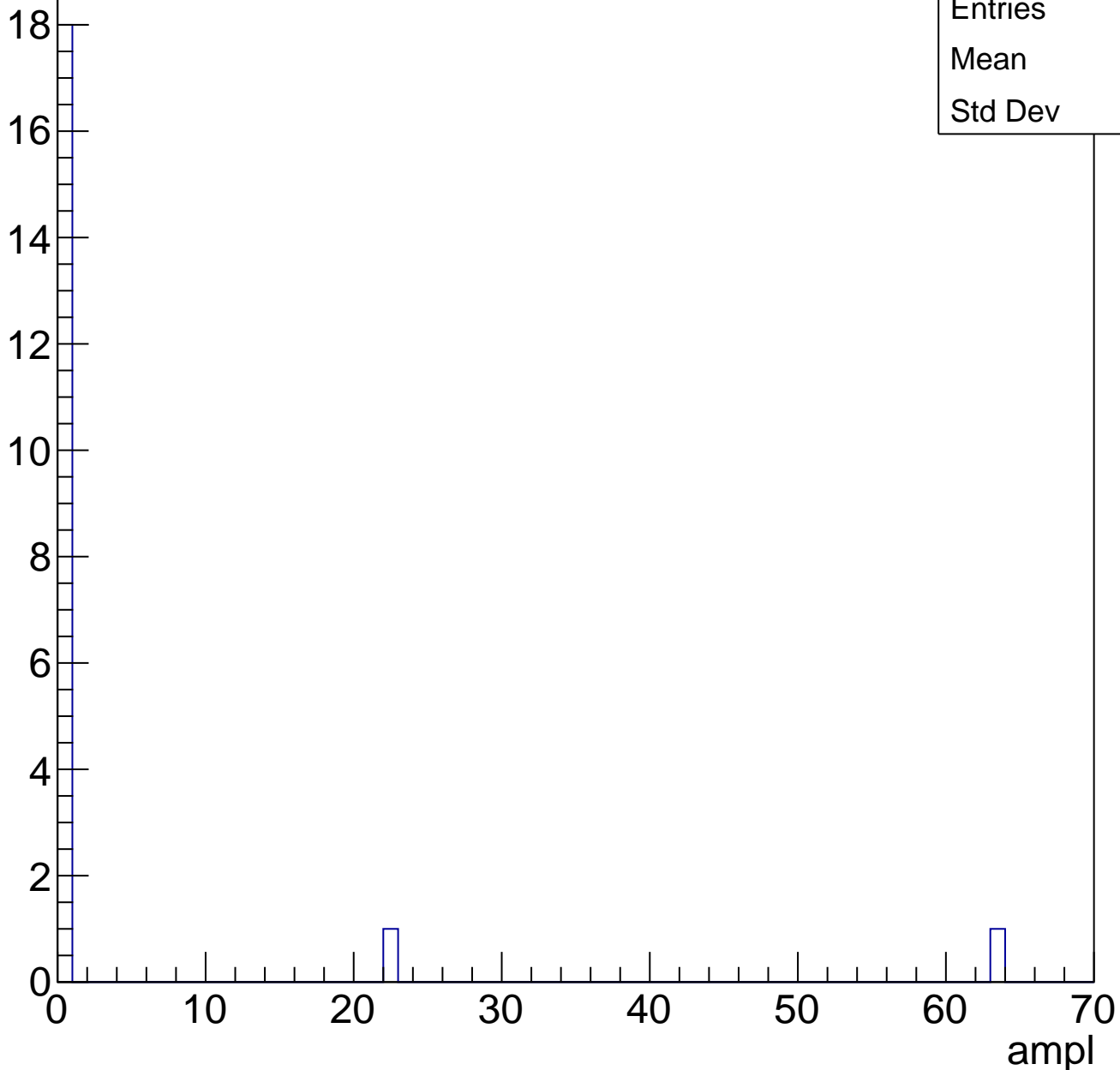
0 10 20 30 40 50 60 70

B1L103S, U7-ch16, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	4.25
Std Dev	14.3

Entry



B1L103S, U7-ch17, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	119
Mean	22.53
Std Dev	12.42

Gaus mean : 29.3256

Gaus Width: 4.0916

Entry

25

20

15

10

5

0

0

10

20

30

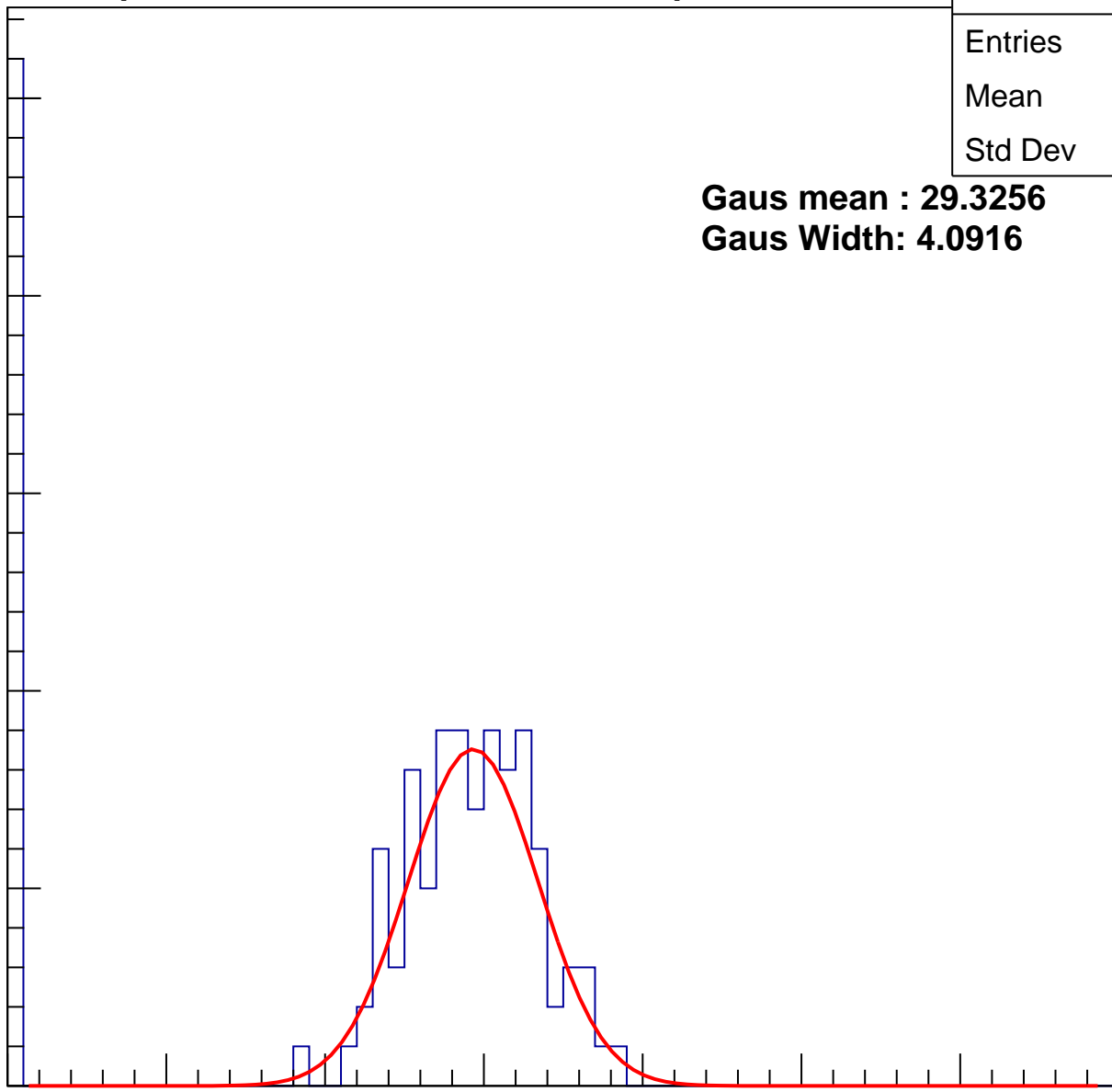
40

50

60

70

ampl



B1L103S, U7-ch17, adc1

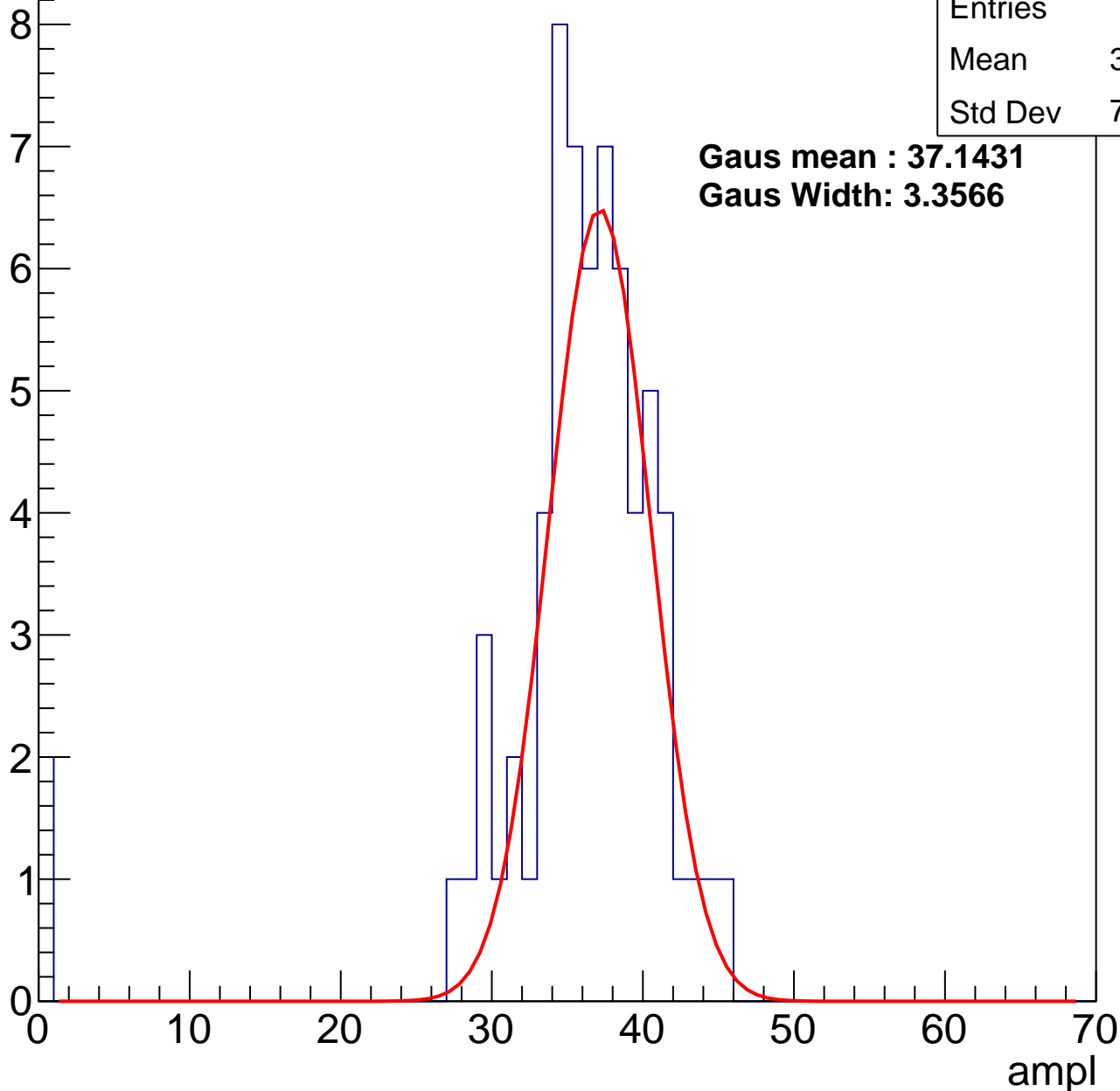
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	35.03
Std Dev	7.257

Gaus mean : 37.1431

Gaus Width: 3.3566



B1L103S, U7-ch17, adc2

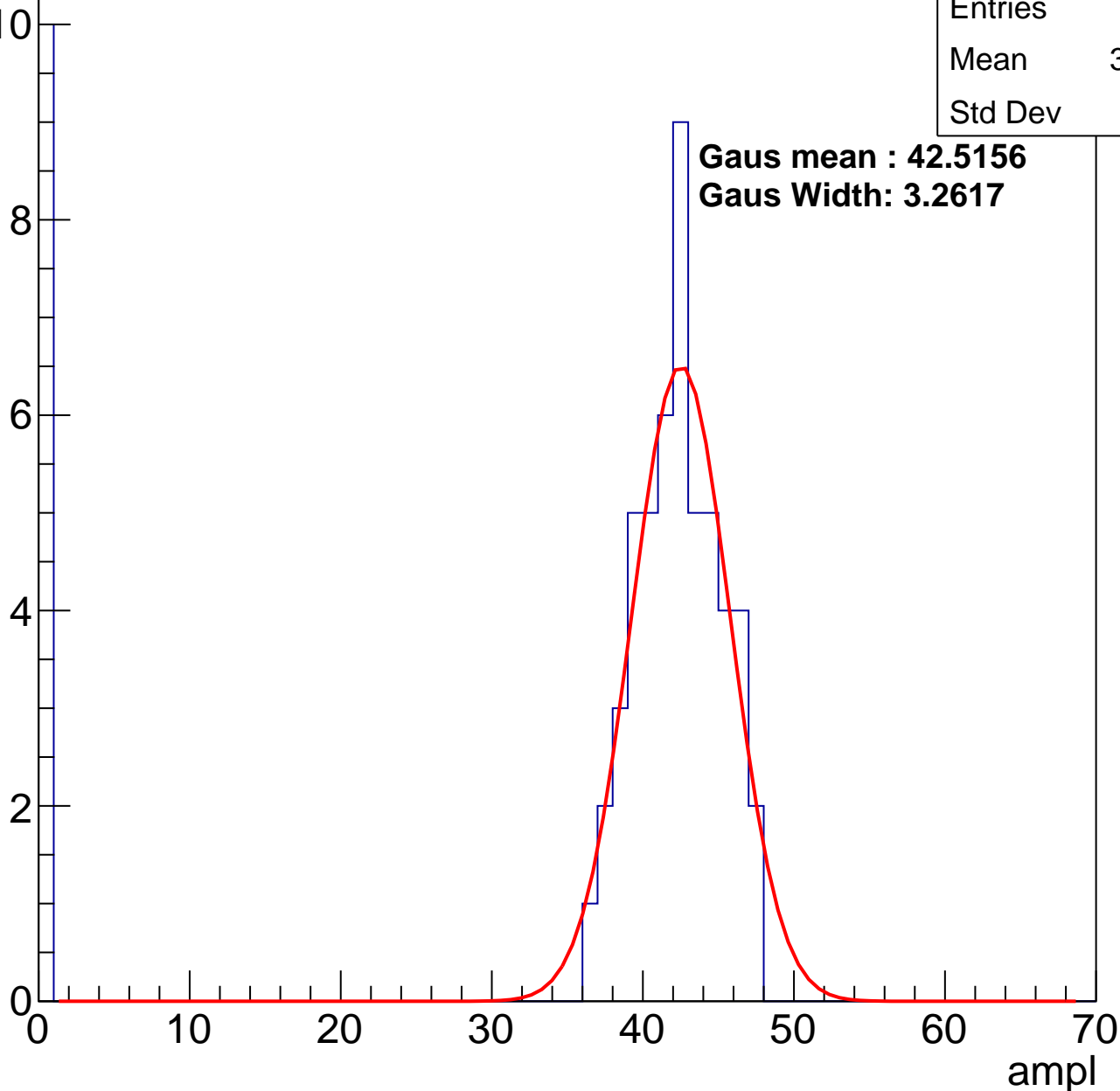
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	35.02
Std Dev	15.7

Gaus mean : 42.5156

Gaus Width: 3.2617



B1L103S, U7-ch17, adc3

calib_packv5_041523_1651.root, FC#0, port C2

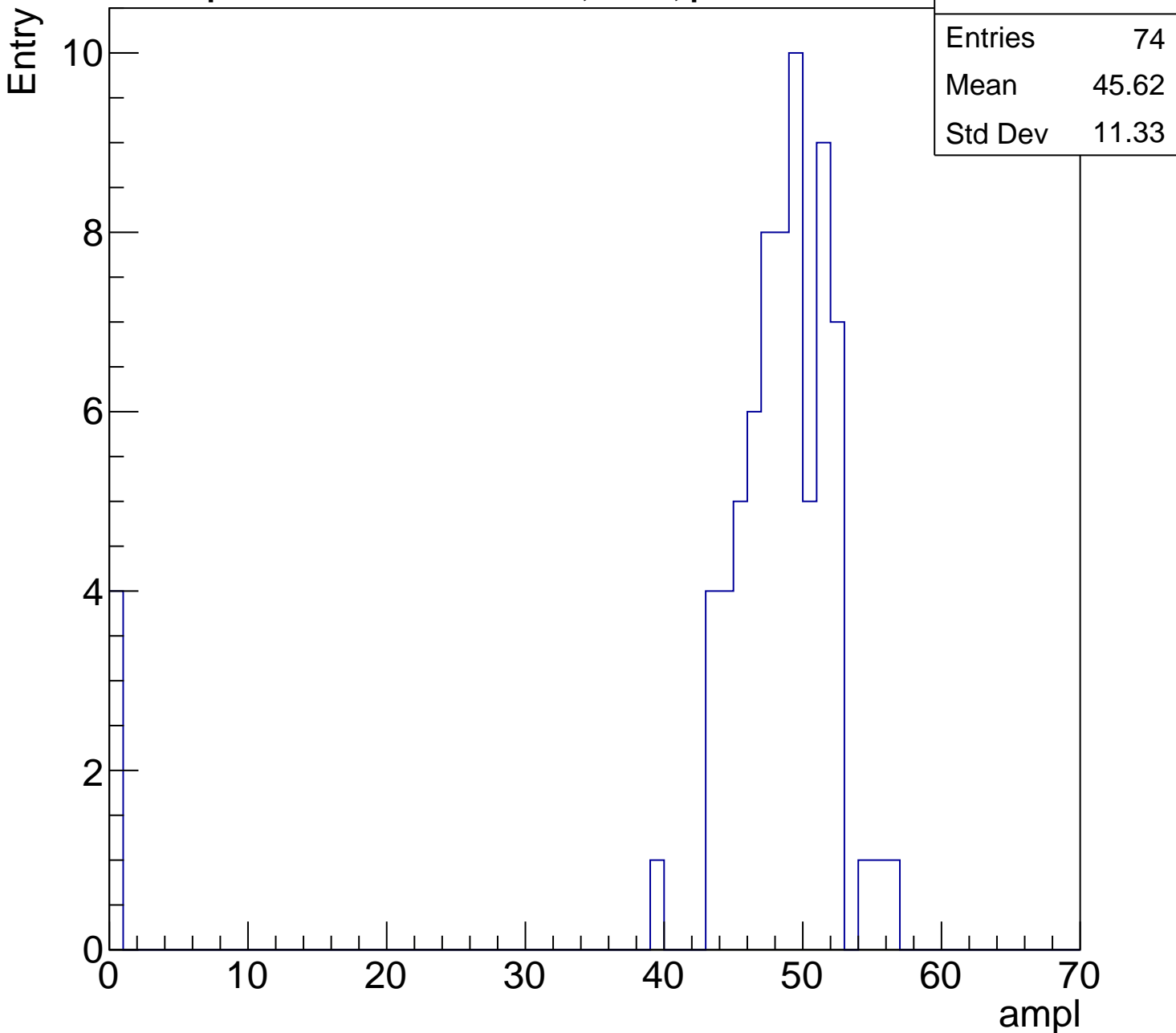
Entries	74
Mean	45.62
Std Dev	11.33

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

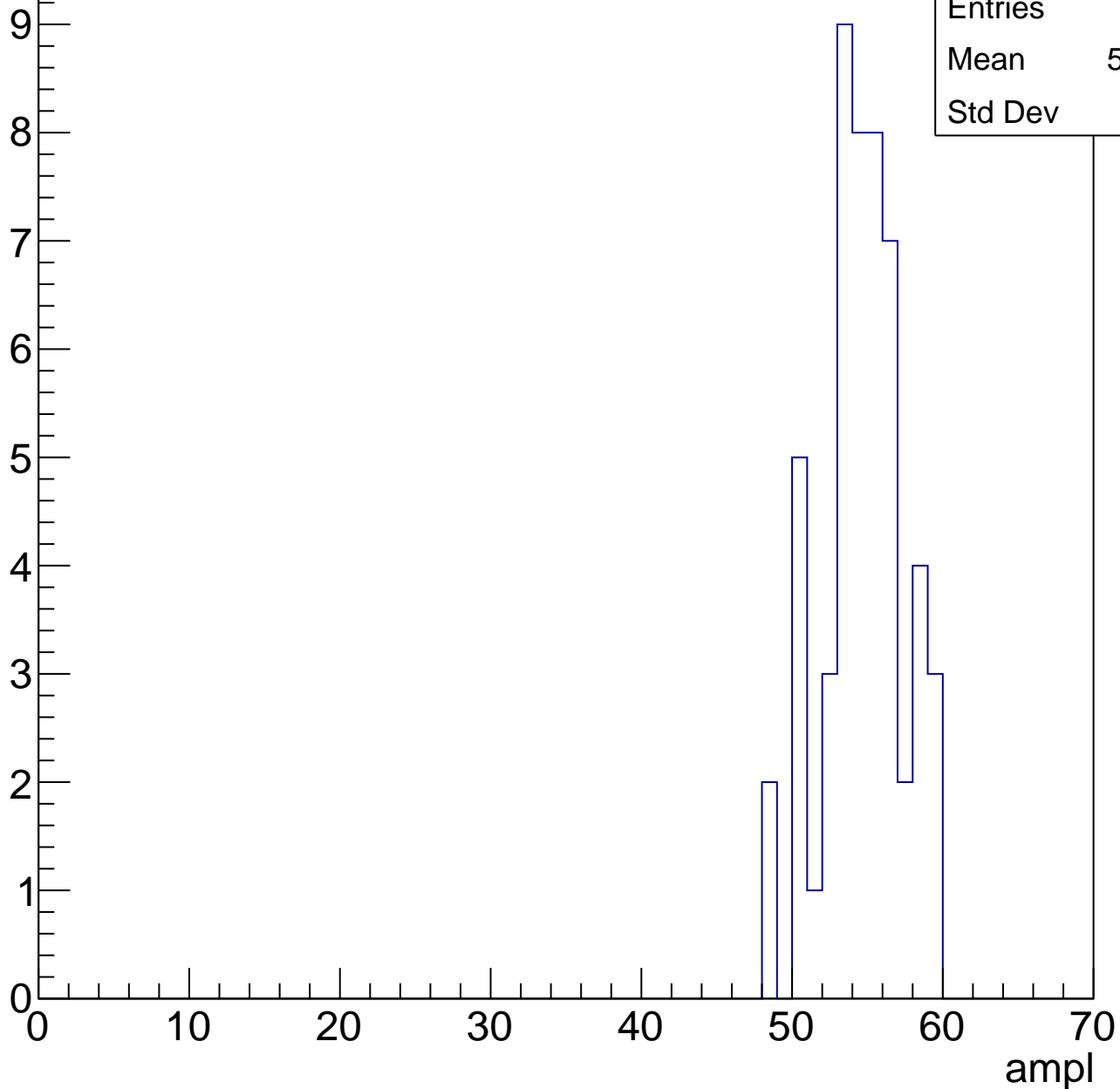
ampl



B1L103S, U7-ch17, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



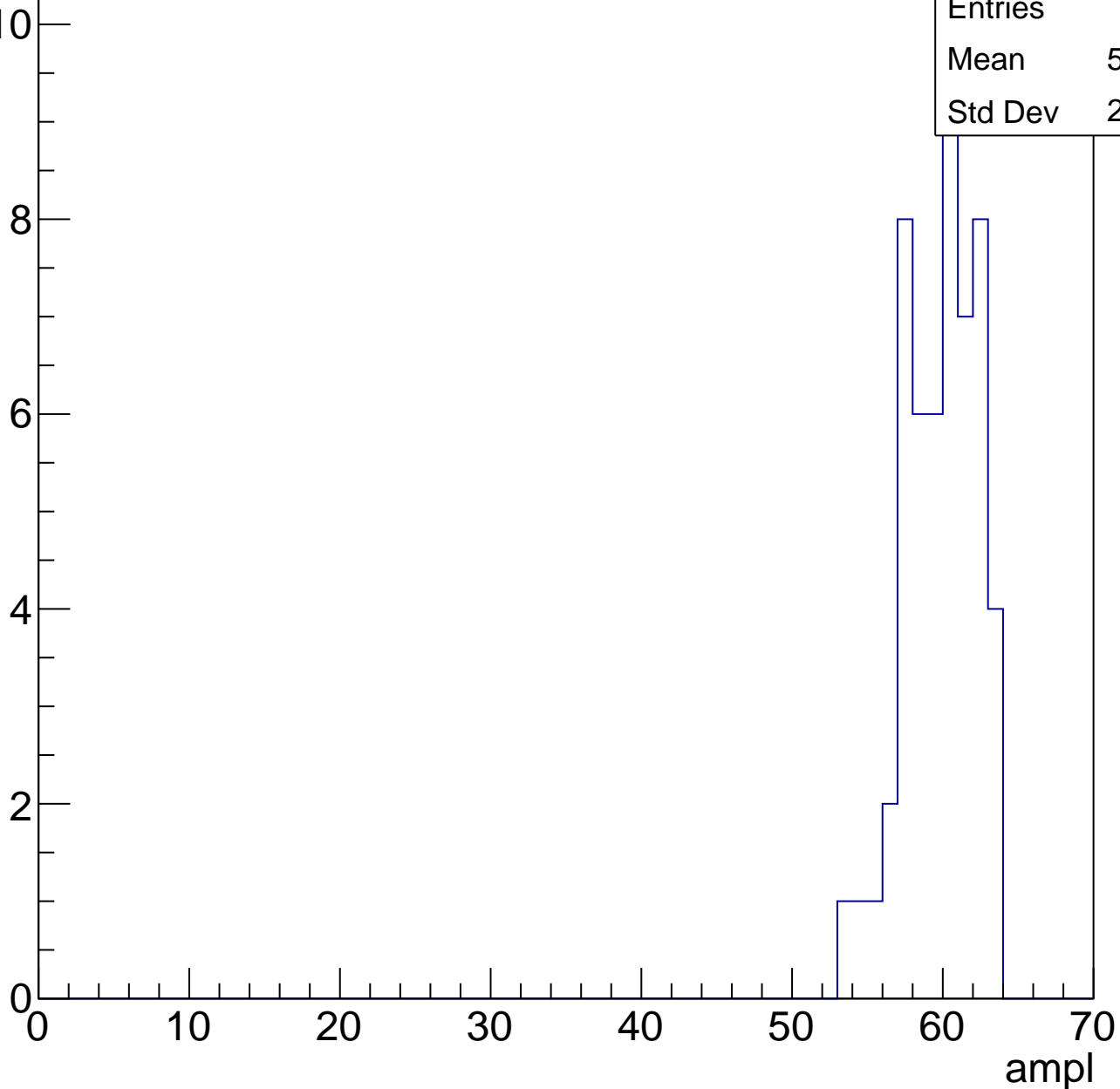
Entries	52
Mean	54.17
Std Dev	2.68

B1L103S, U7-ch17, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	59.39
Std Dev	2.352

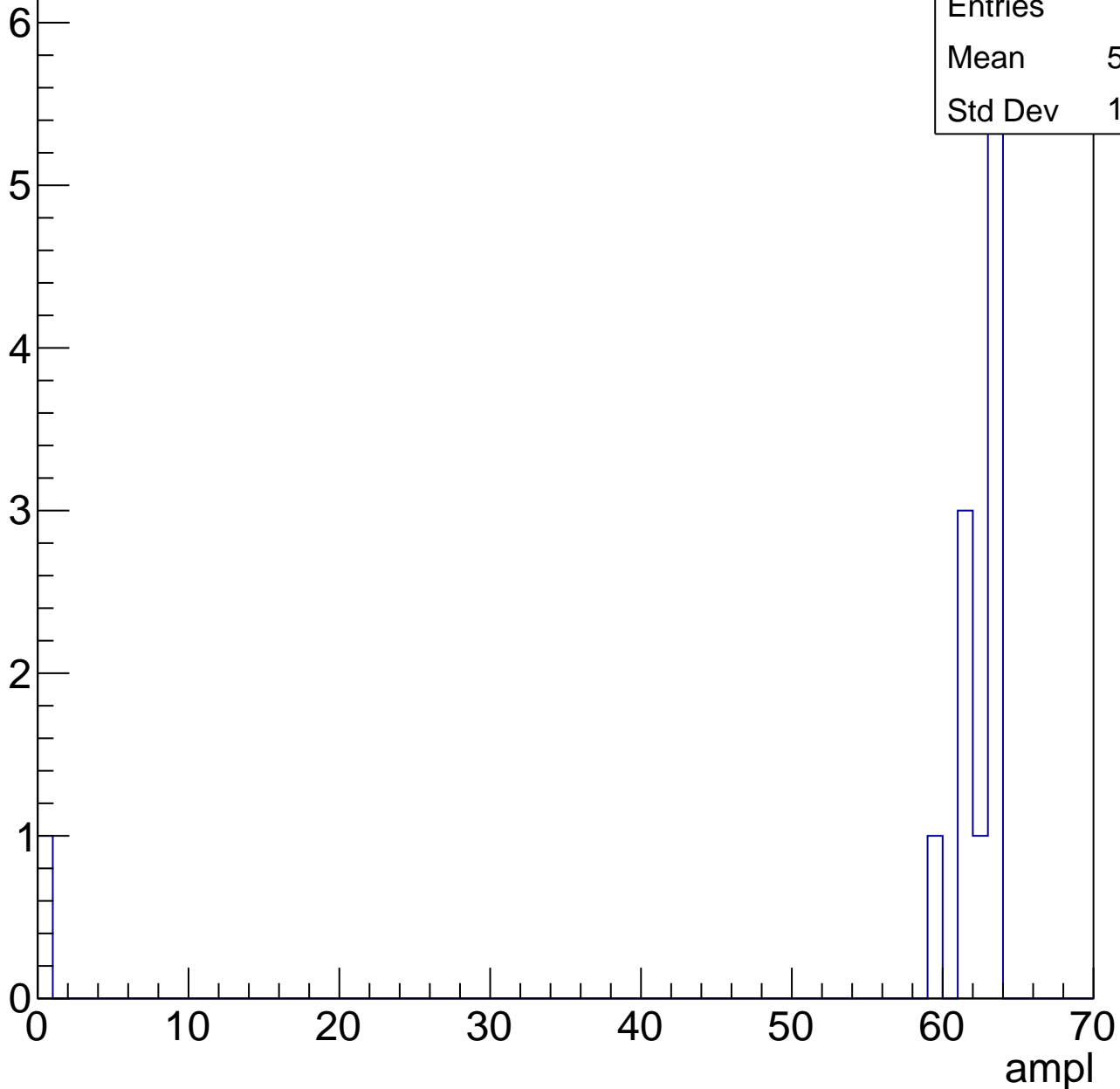


B1L103S, U7-ch17, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

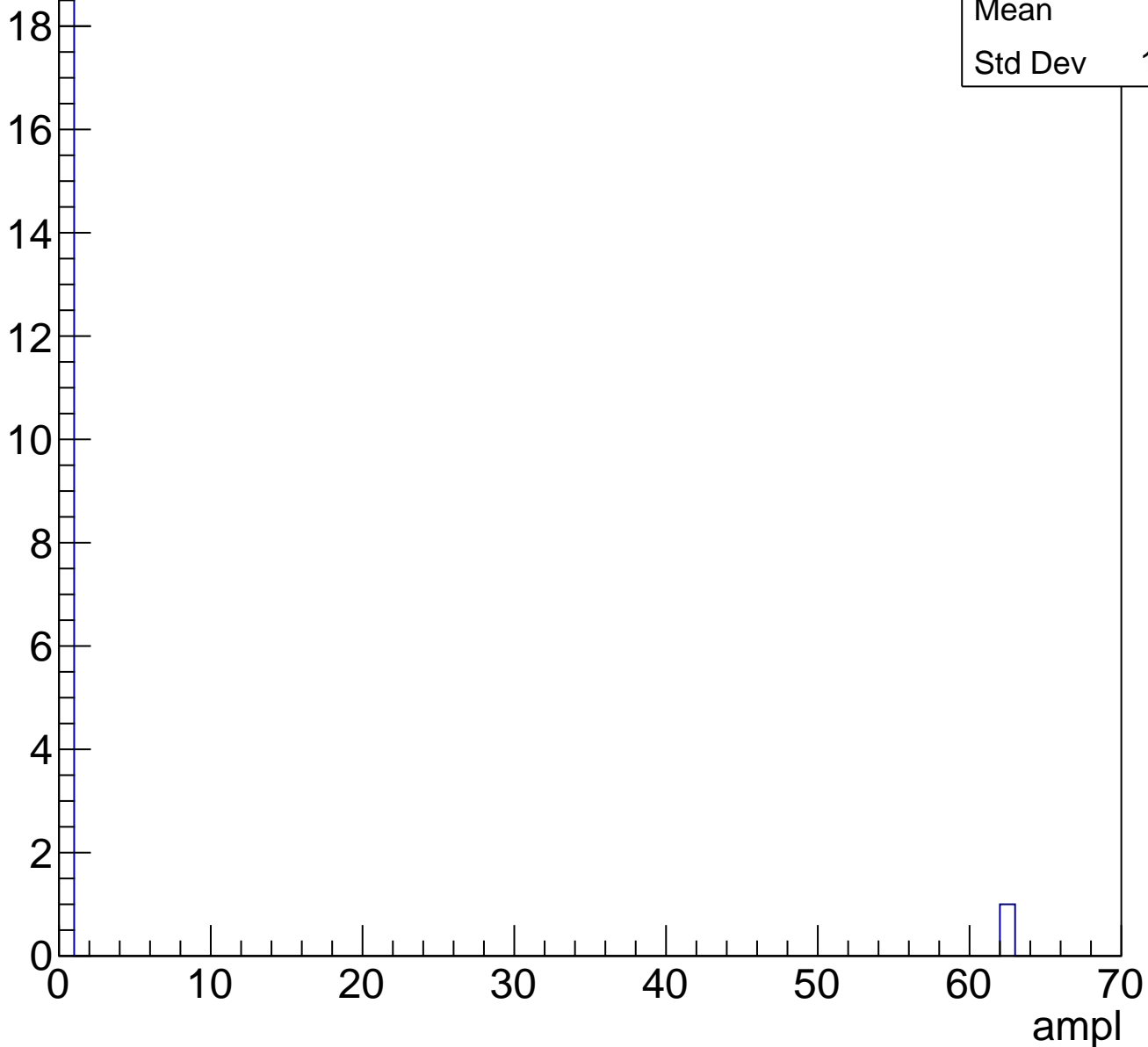
Entries	12
Mean	56.83
Std Dev	17.18



B1L103S, U7-ch17, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	20
Mean	3.1
Std Dev	13.51

B1L103S, U7-ch18, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	24.52
Std Dev	10.58

Gaus mean : 28.8500

Gaus Width: 3.9734

Entry

10

8

6

4

2

0

0

10

20

30

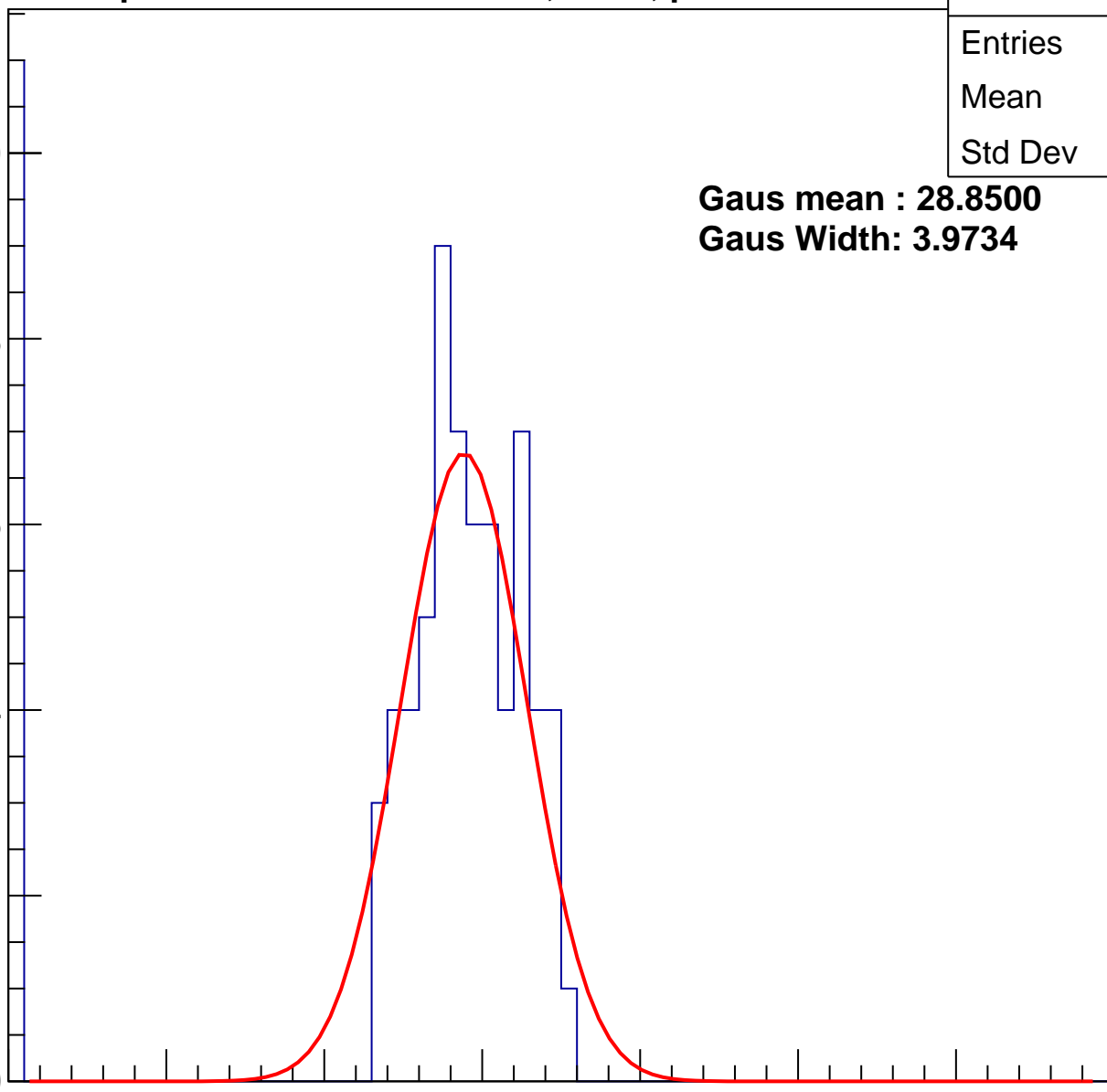
40

50

60

70

ampl



B1L103S, U7-ch18, adc1

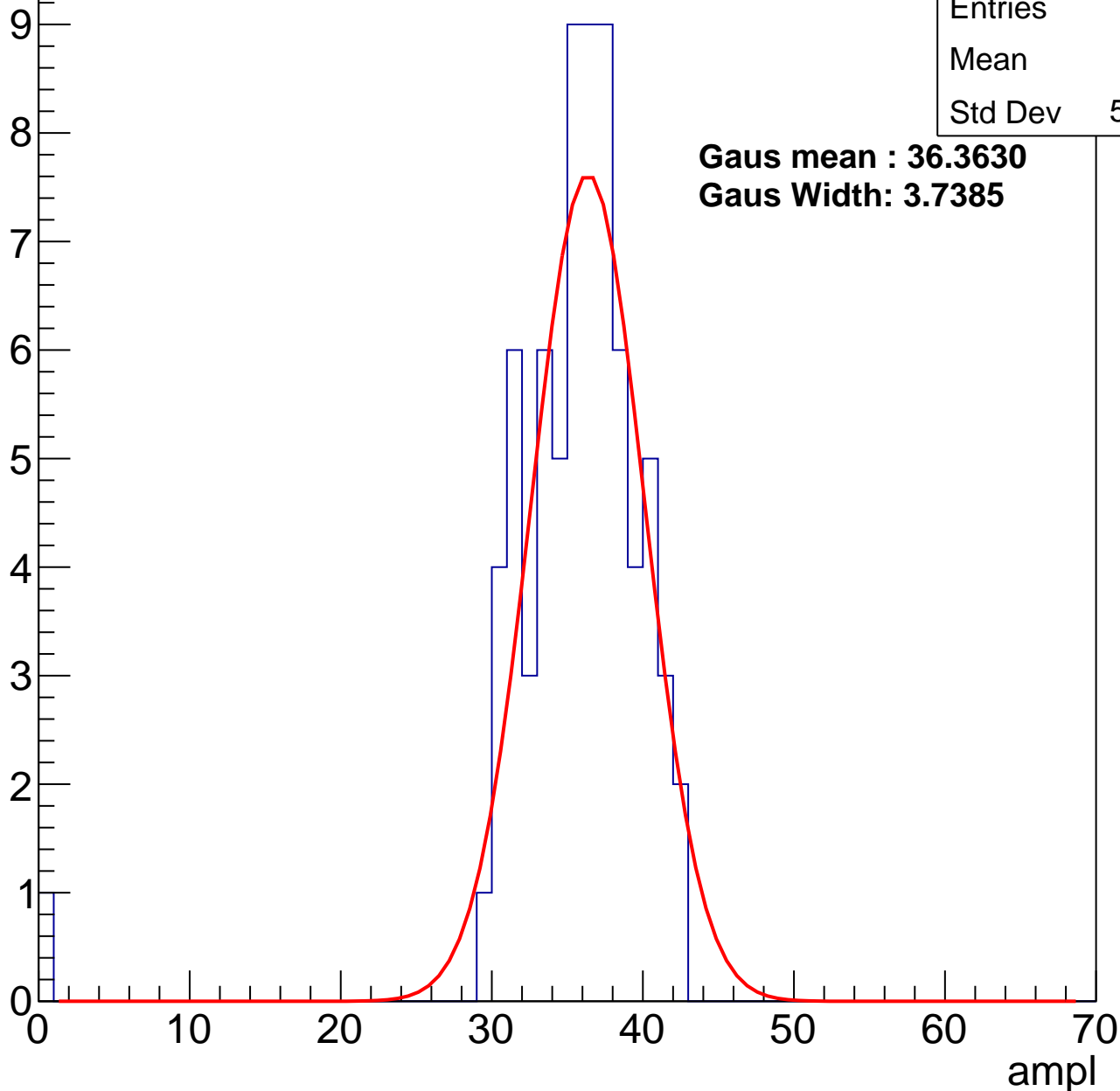
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	35.1
Std Dev	5.243

Gaus mean : 36.3630

Gaus Width: 3.7385



B1L103S, U7-ch18, adc2

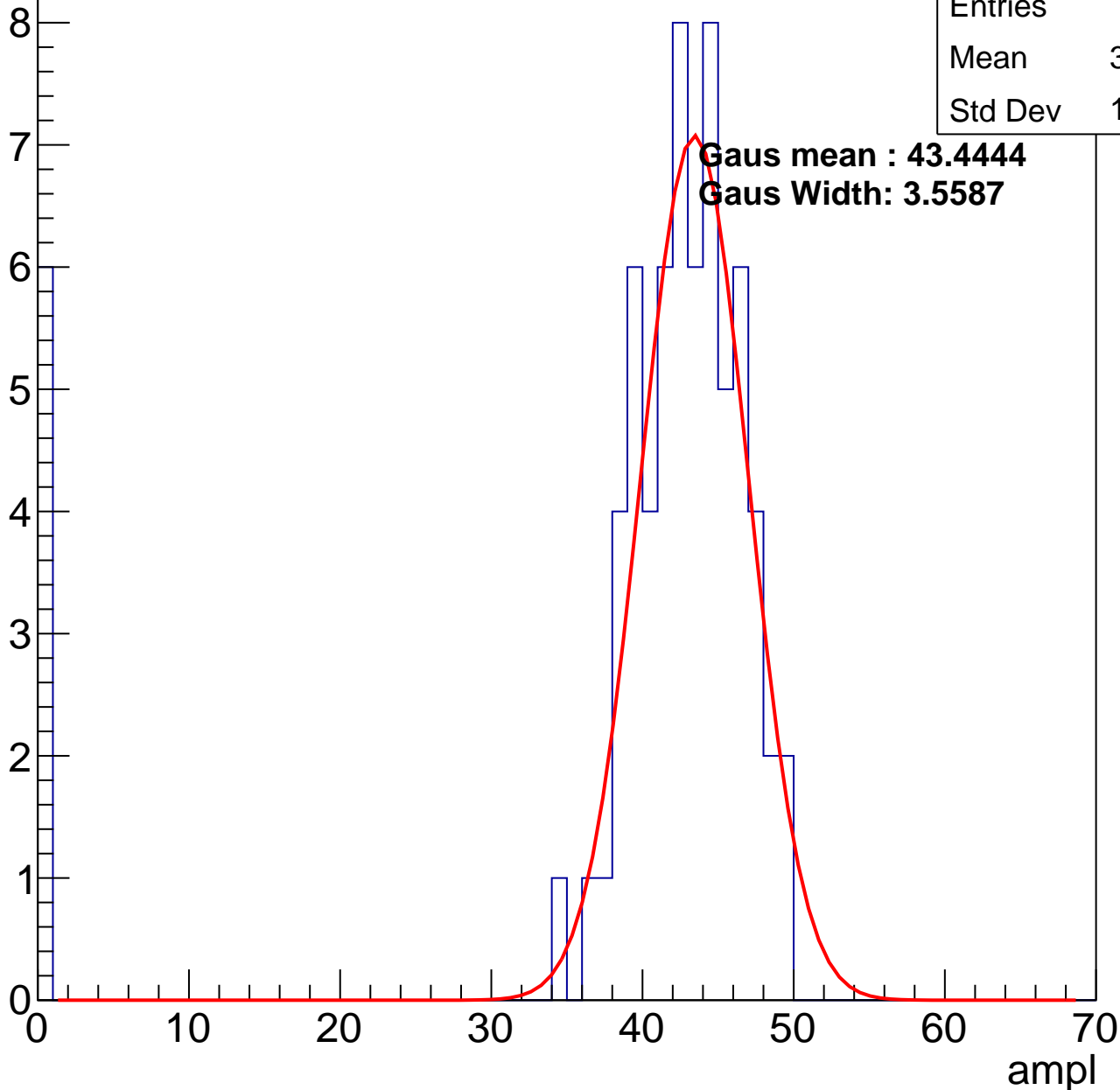
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	38.97
Std Dev	12.34

Gaus mean : 43.4444

Gaus Width: 3.5587

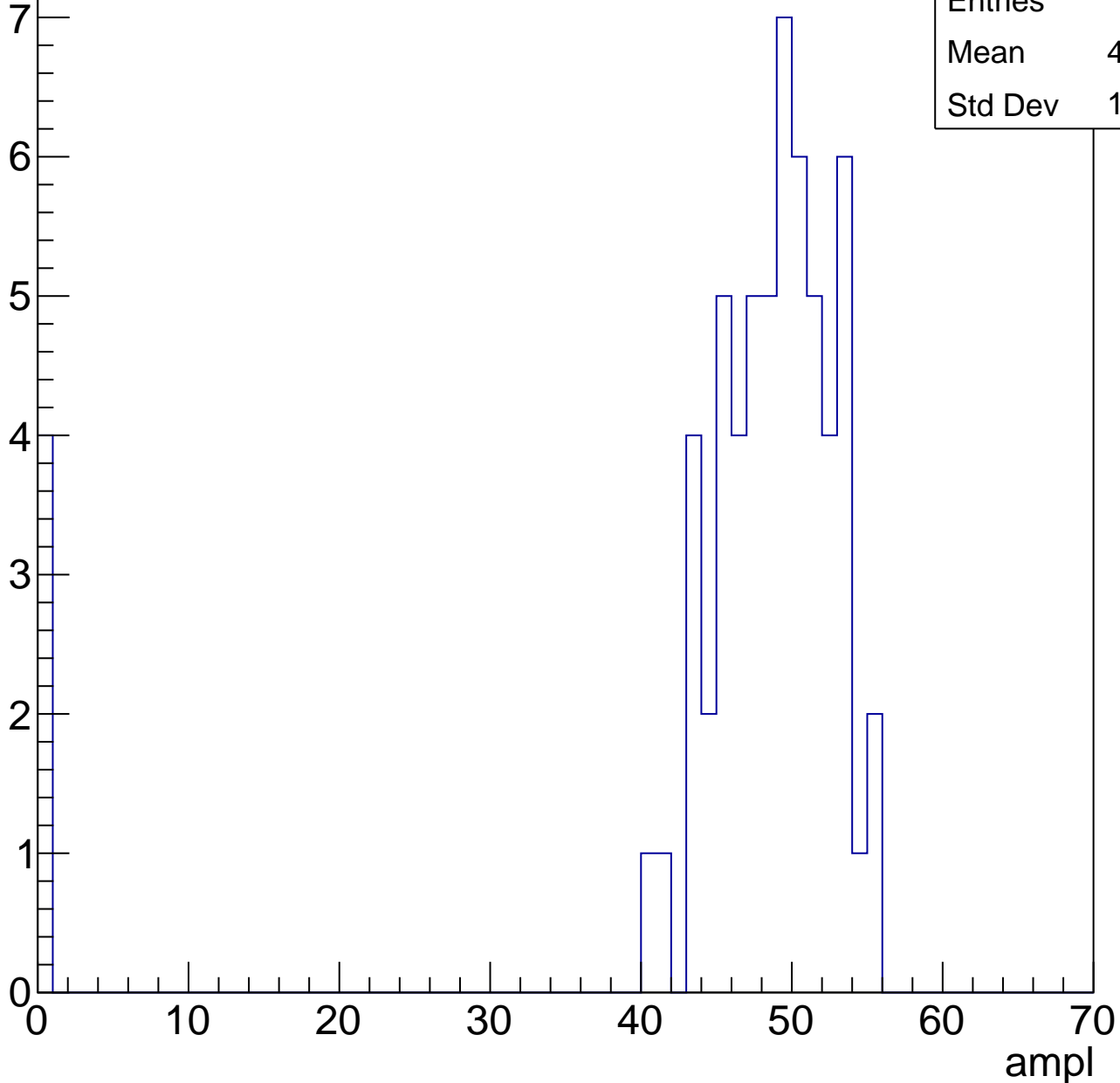


B1L103S, U7-ch18, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	45.37
Std Dev	12.39

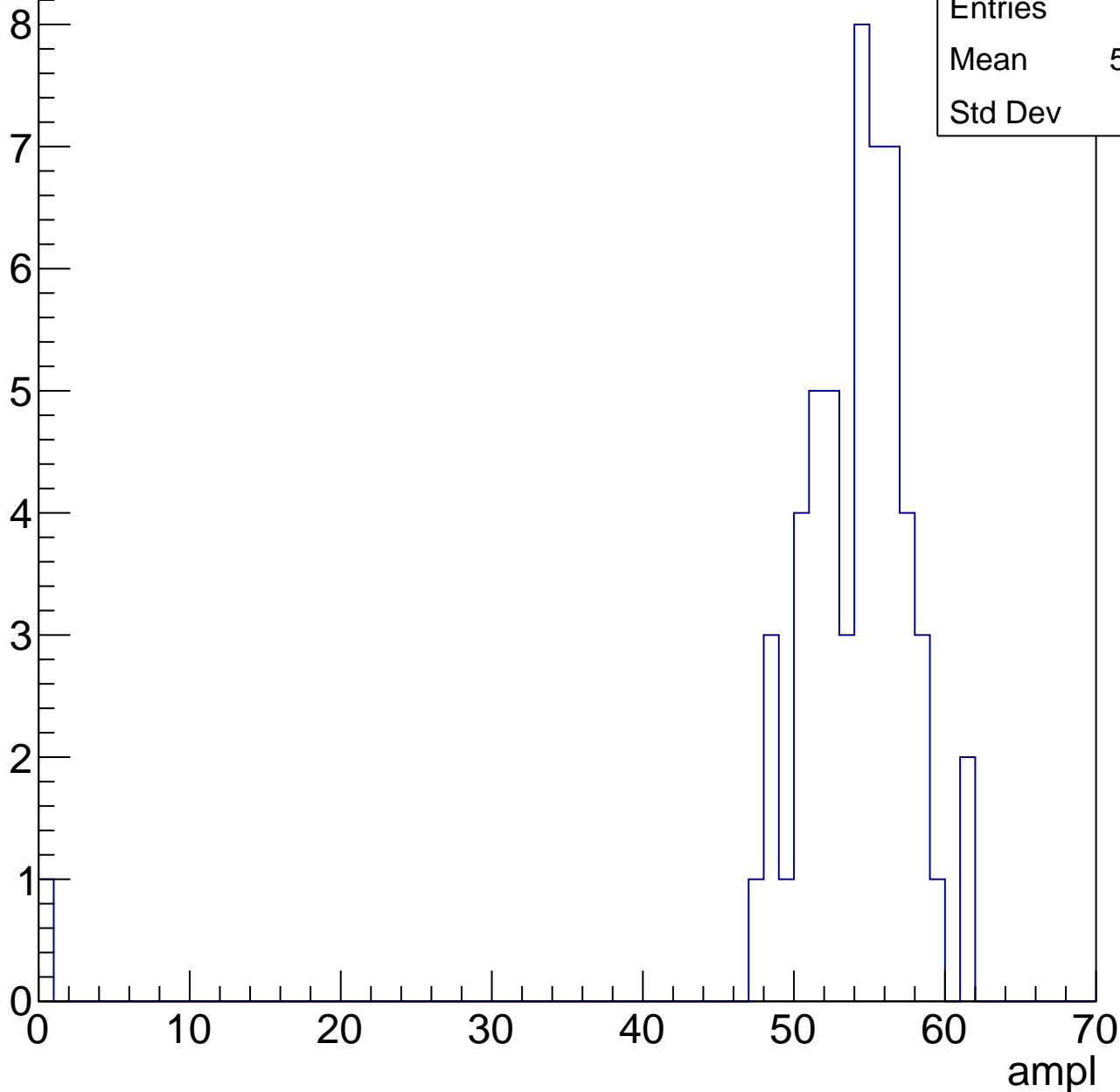


B1L103S, U7-ch18, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	52.84
Std Dev	7.86

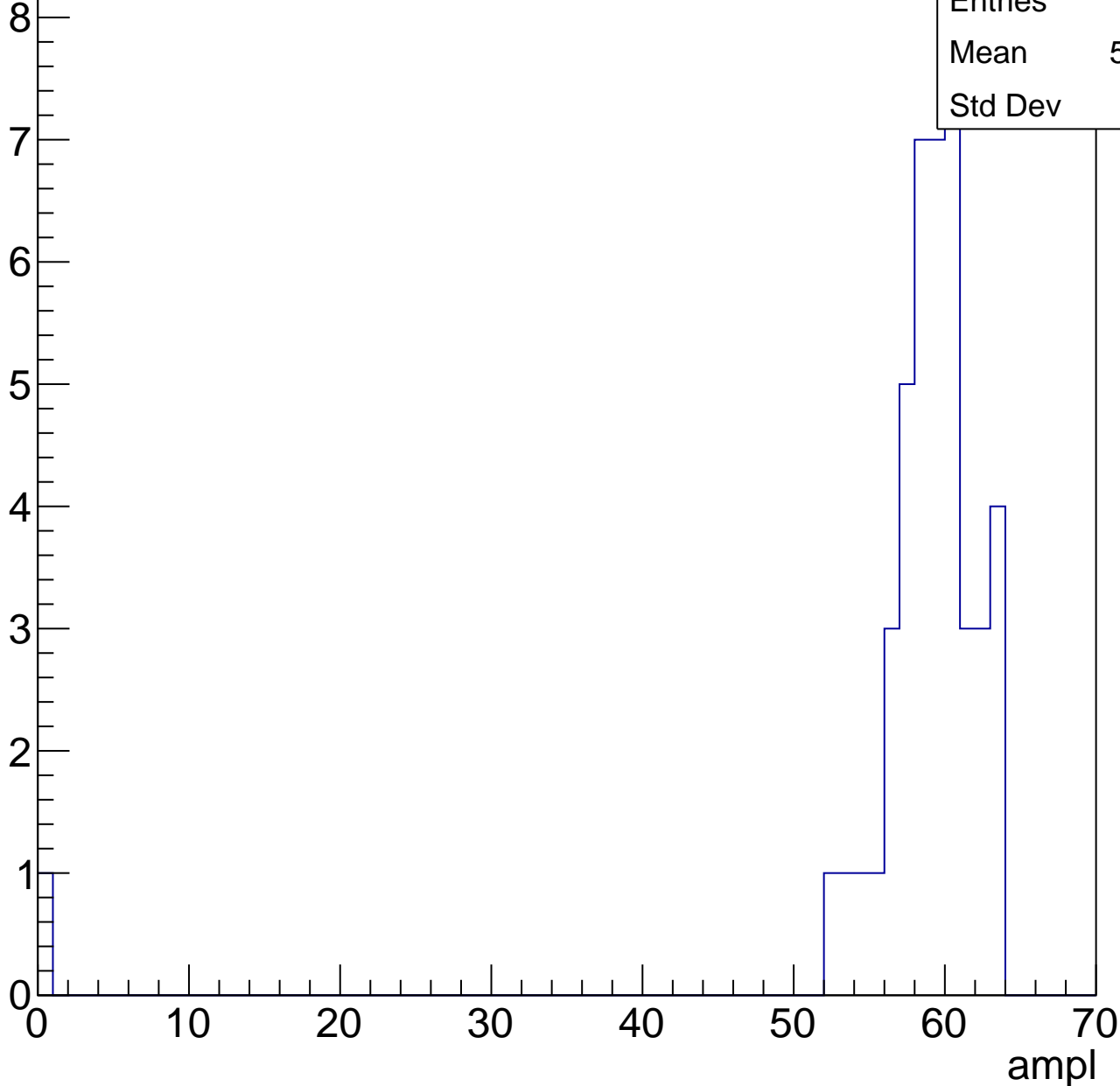


B1L103S, U7-ch18, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	45
Mean	57.49
Std Dev	9.03

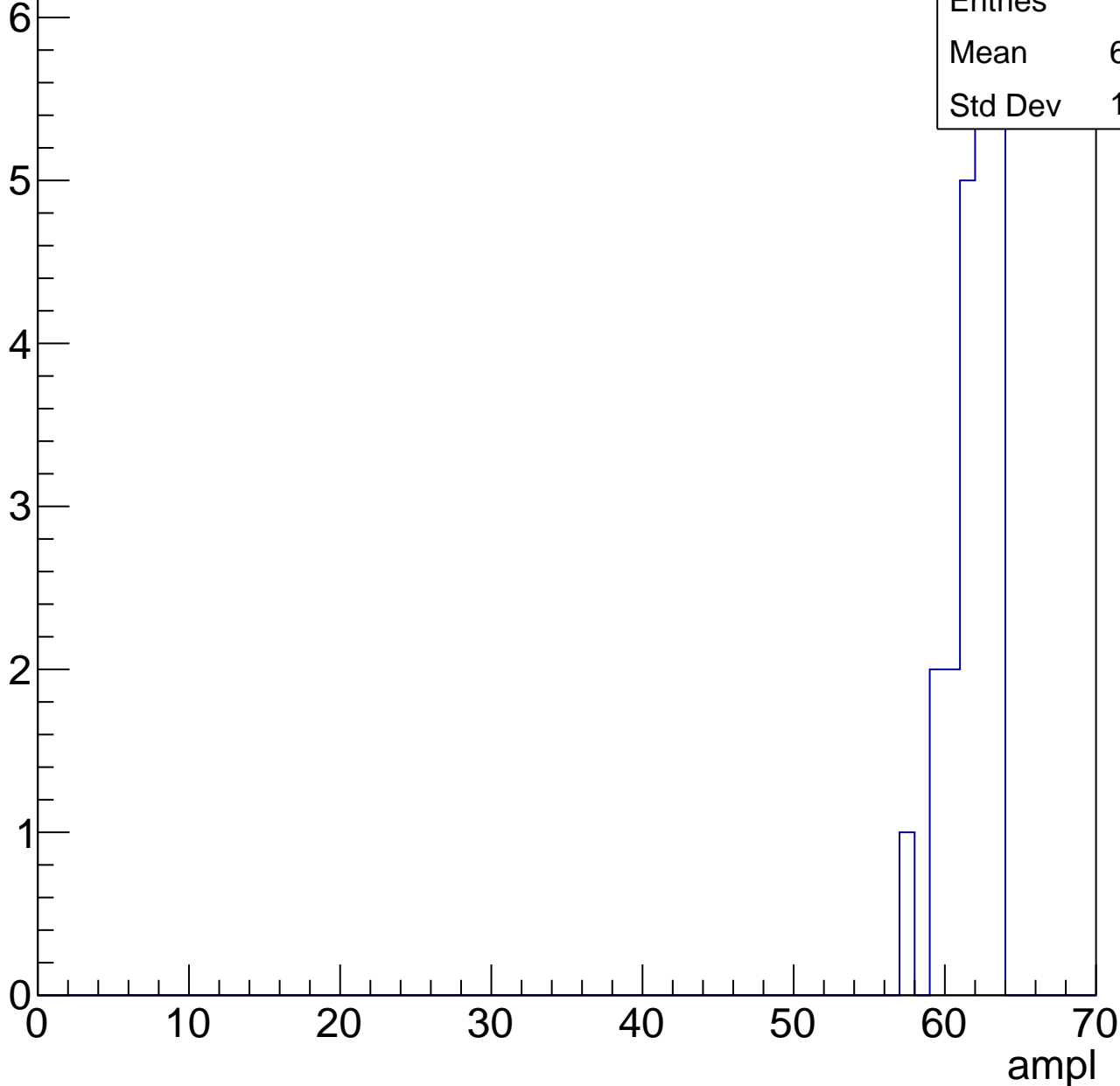


B1L103S, U7-ch18, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	22
Mean	61.36
Std Dev	1.553



B1L103S, U7-ch18, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51

Entry



B1L103S, U7-ch19, adc0

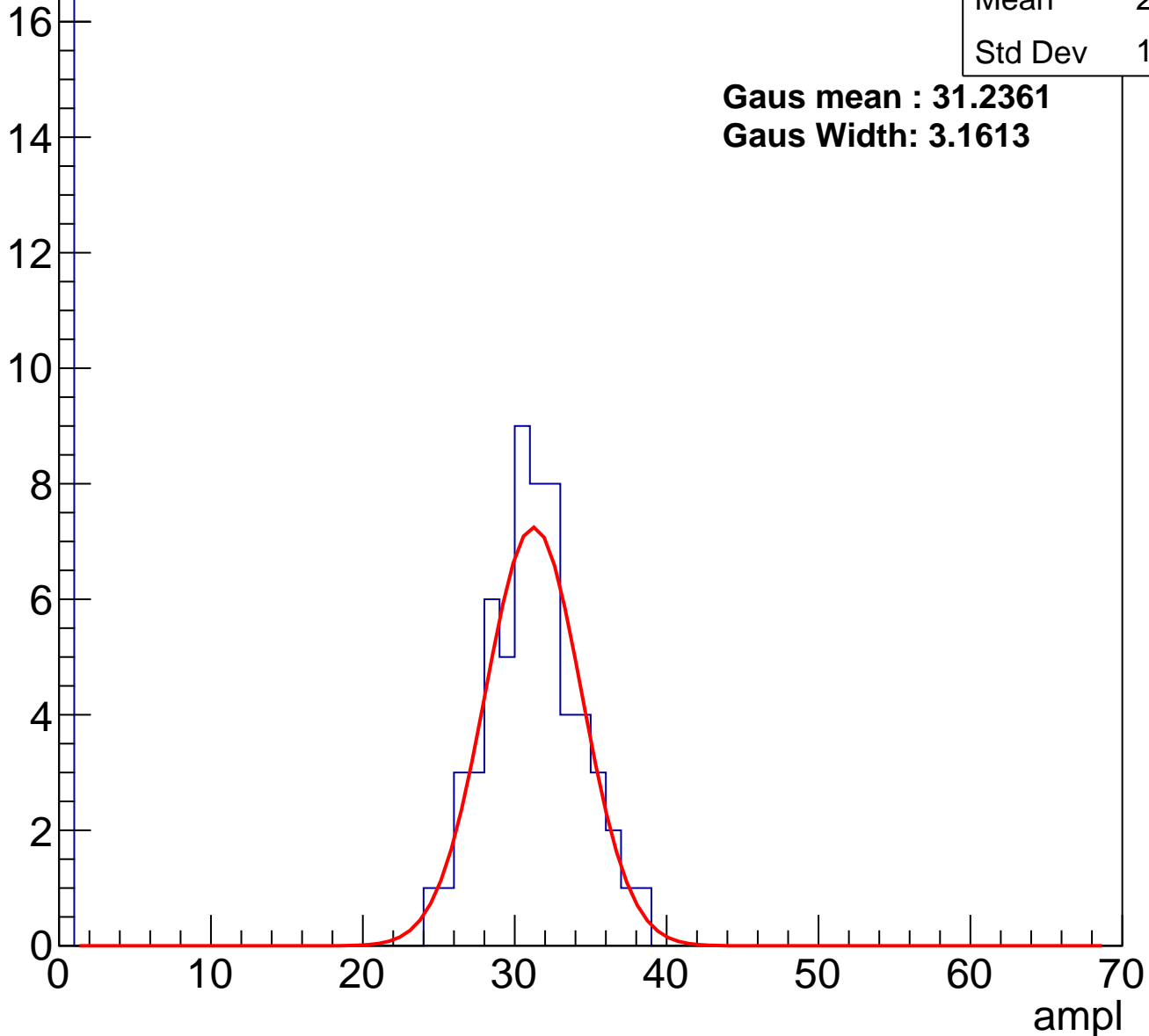
calib_packv5_041523_1651.root, FC#0, port C2

Entries	76
Mean	23.88
Std Dev	13.09

Gaus mean : 31.2361

Gaus Width: 3.1613

Entry



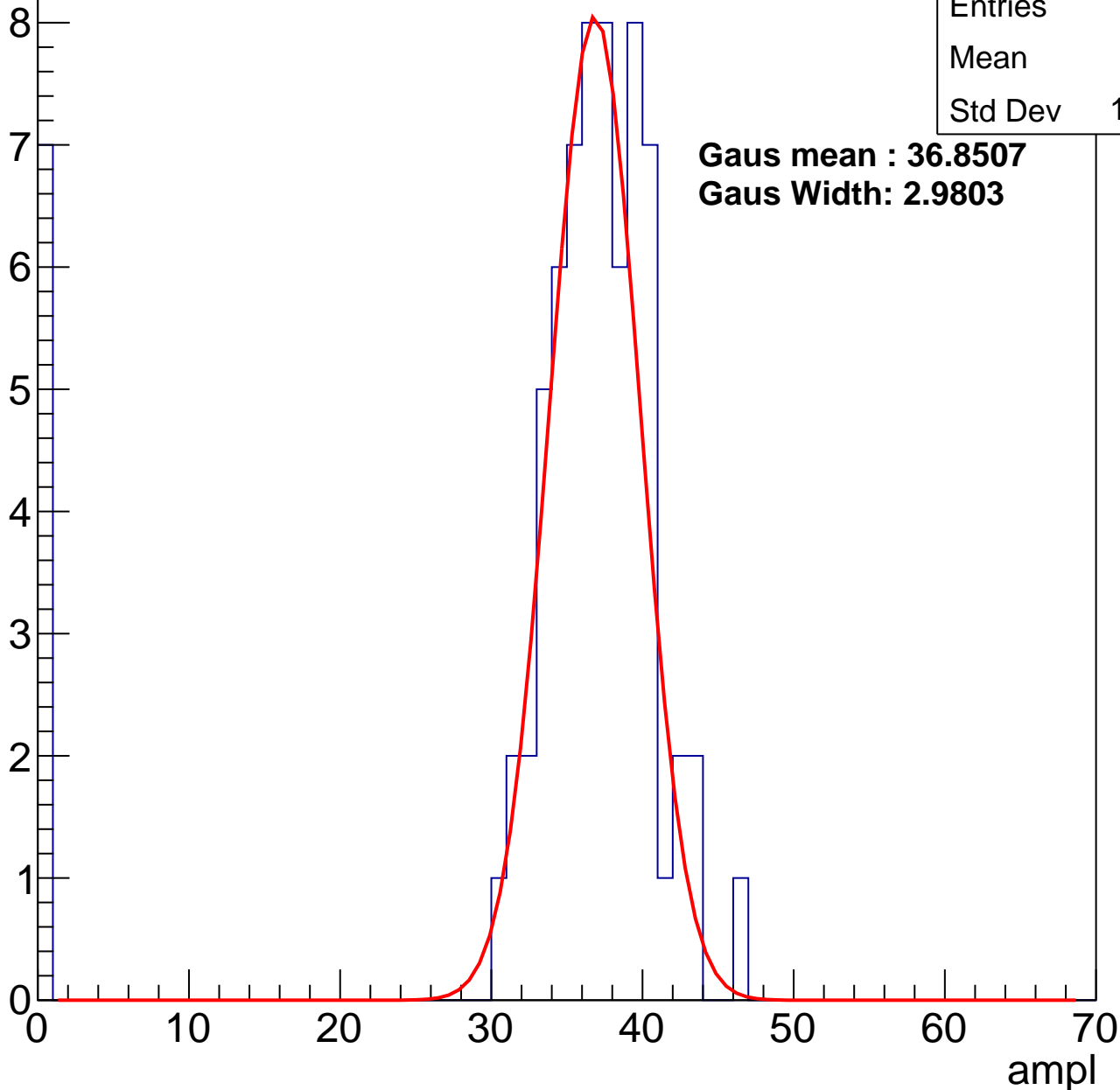
B1L103S, U7-ch19, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	33.3
Std Dev	11.25

Gaus mean : 36.8507
Gaus Width: 2.9803



B1L103S, U7-ch19, adc2

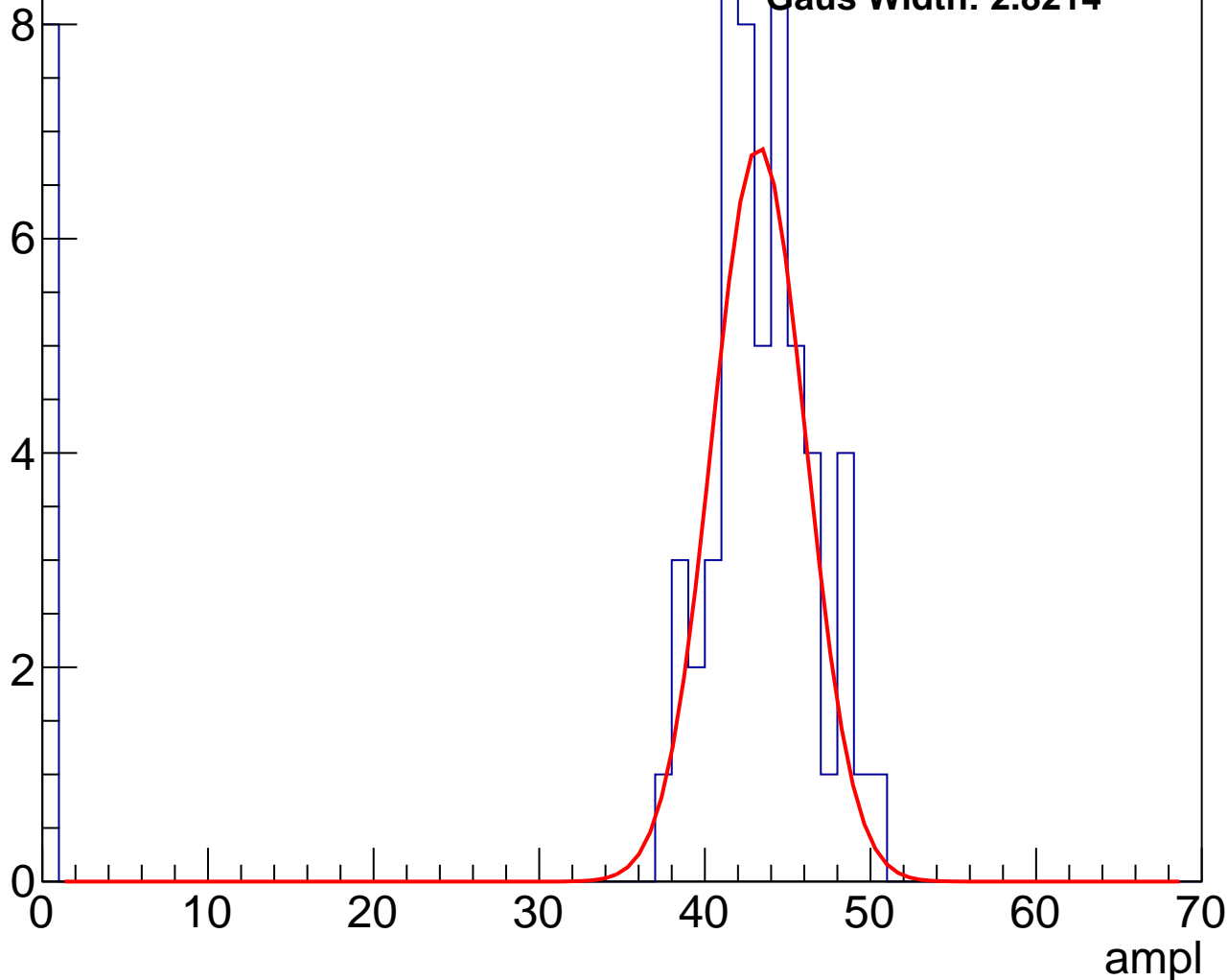
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	37.78
Std Dev	14.41

Gaus mean : 43.2579

Gaus Width: 2.8214



B1L103S, U7-ch19, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	76
Mean	49.64
Std Dev	3.085

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

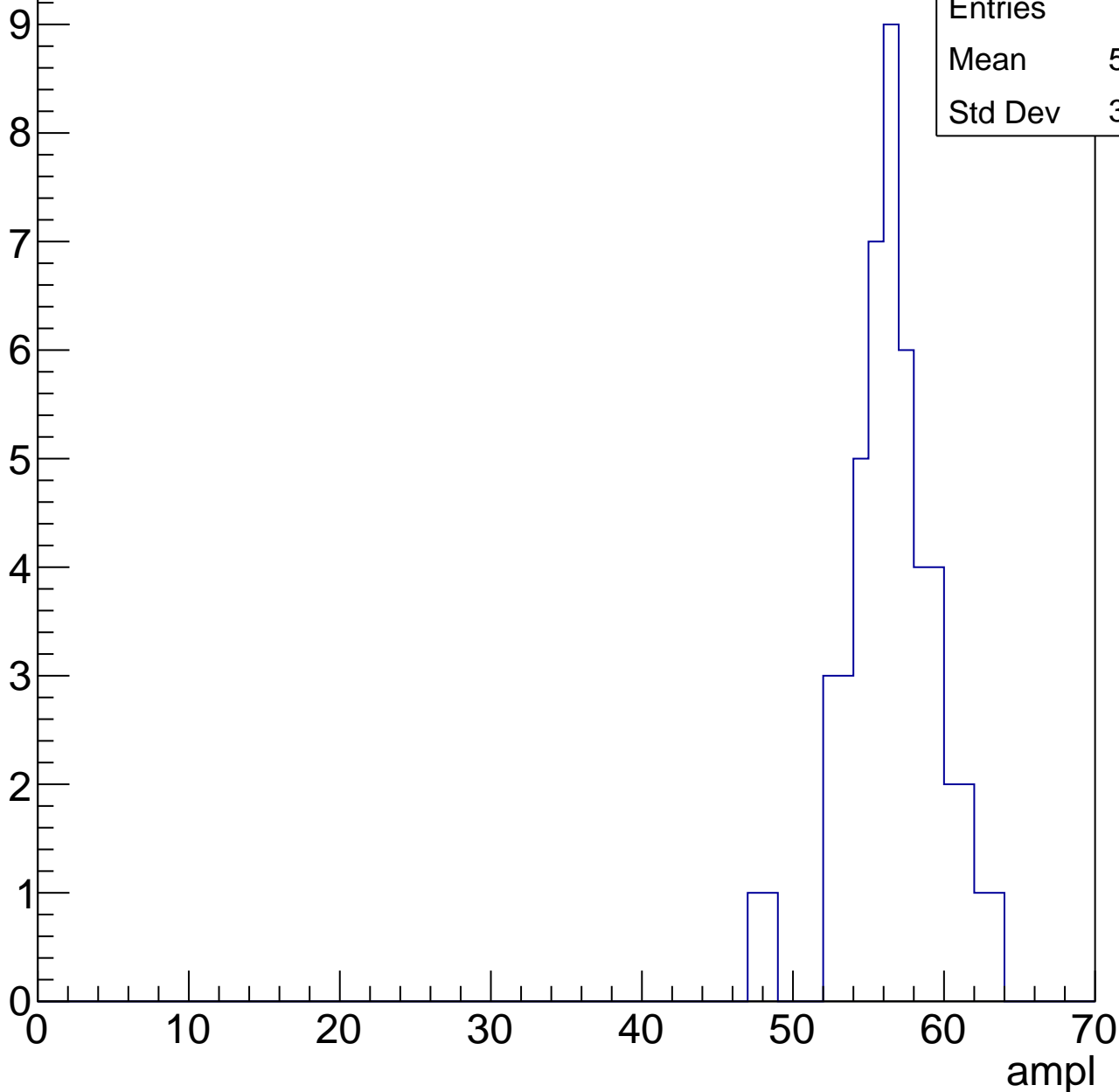


B1L103S, U7-ch19, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	56.04
Std Dev	3.103

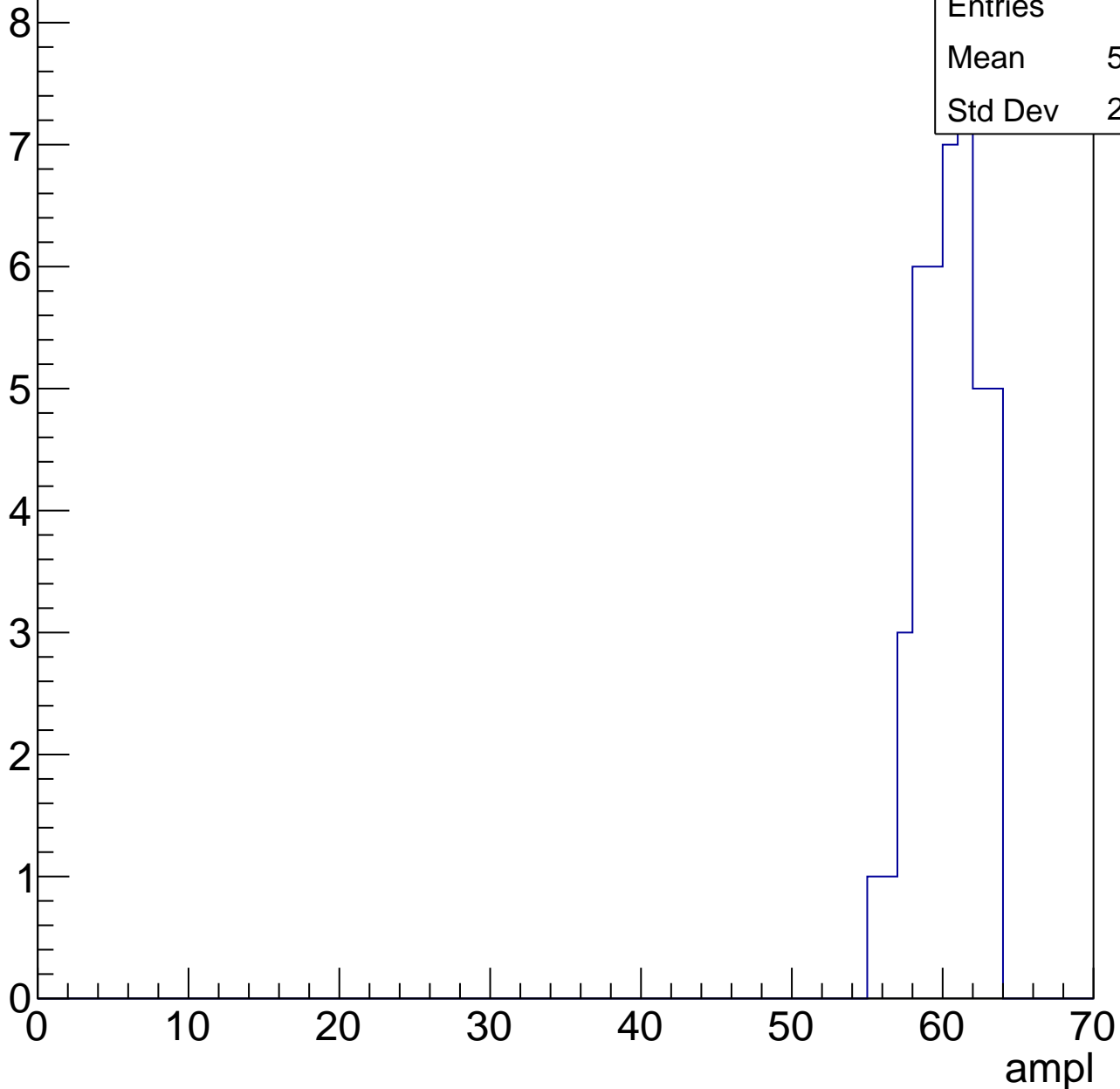


B1L103S, U7-ch19, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

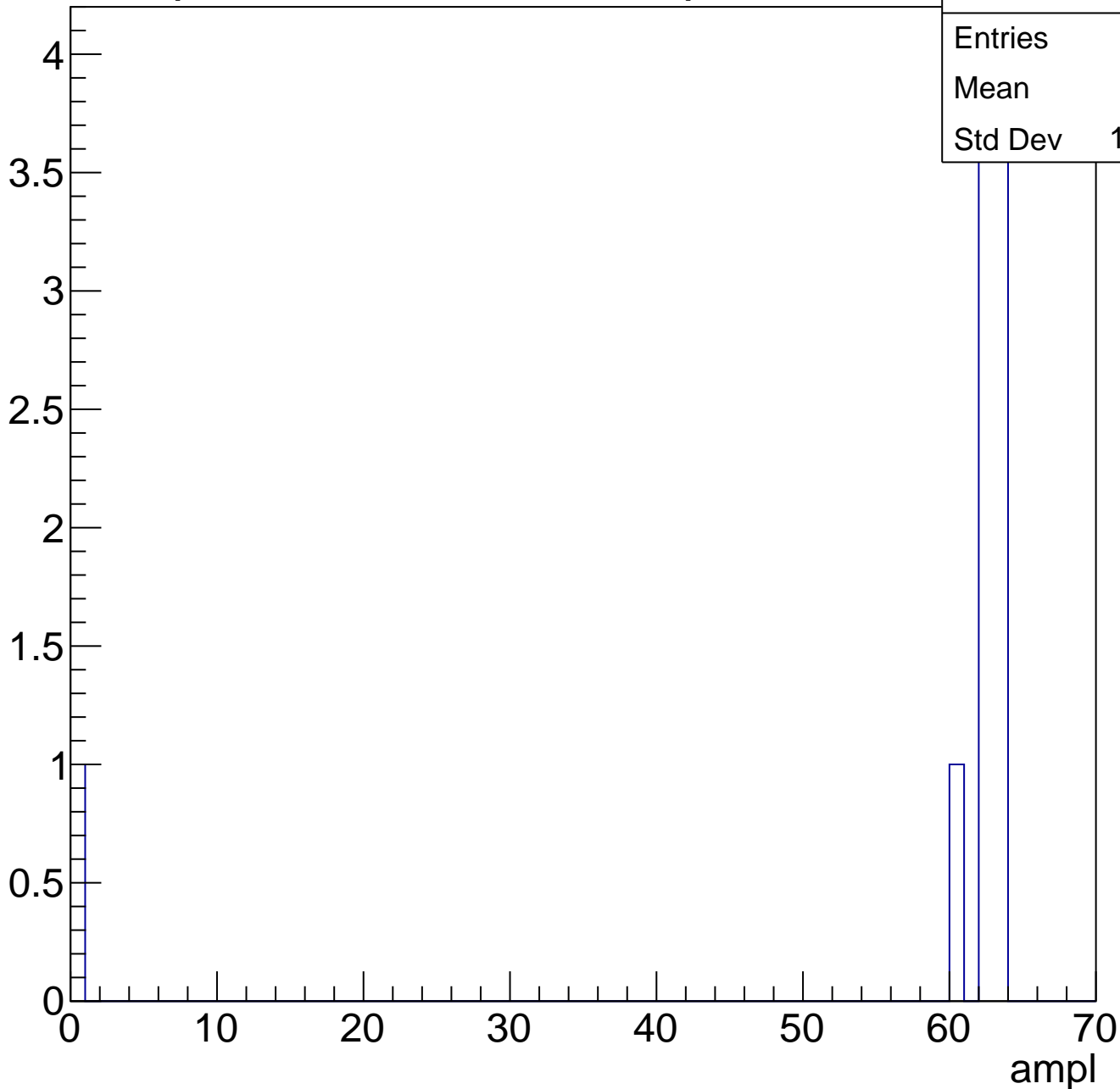
Entries	42
Mean	59.93
Std Dev	2.017



B1L103S, U7-ch19, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch19, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U7-ch20, adc0

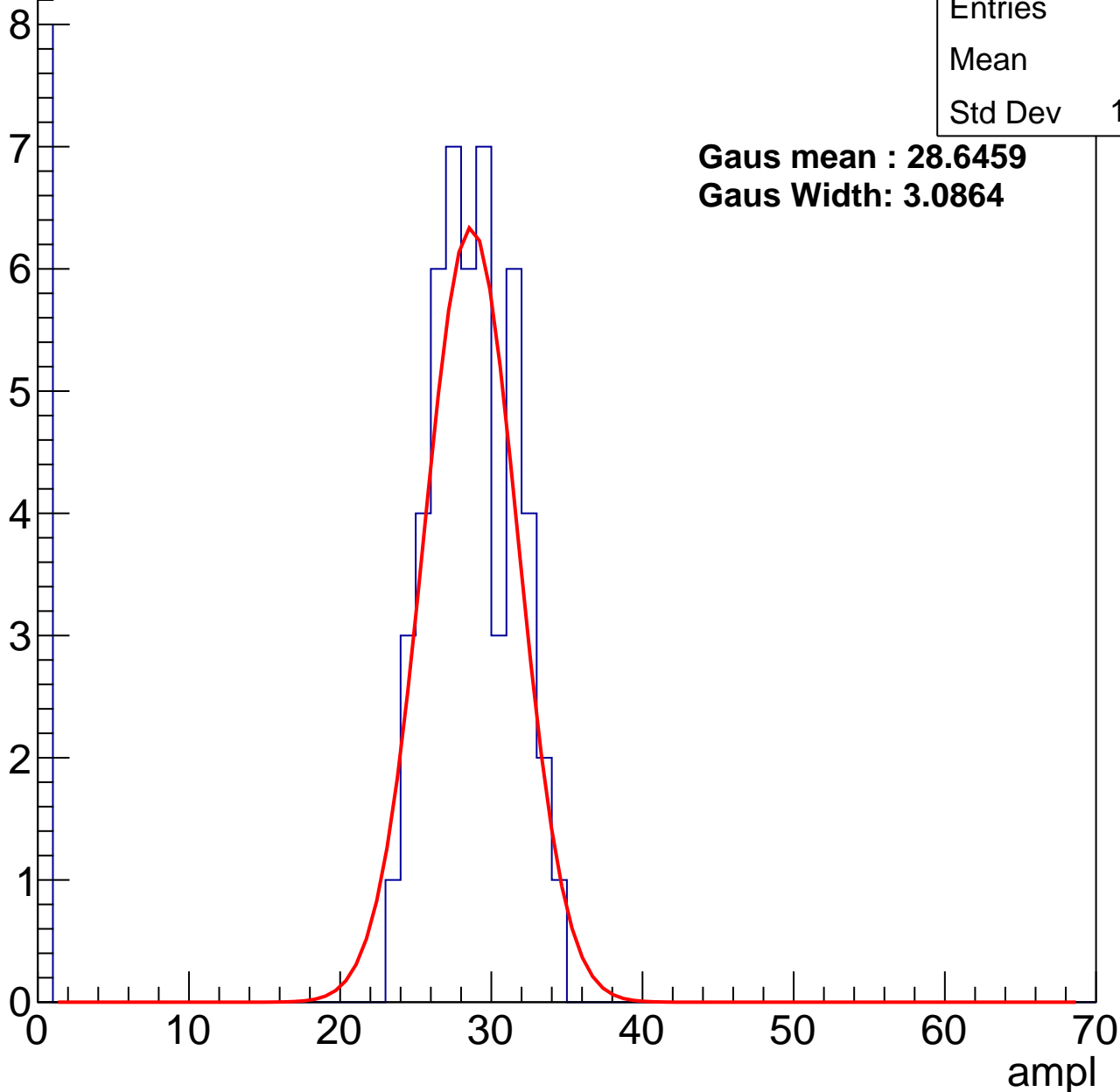
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	24.4
Std Dev	10.07

Gaus mean : 28.6459

Gaus Width: 3.0864

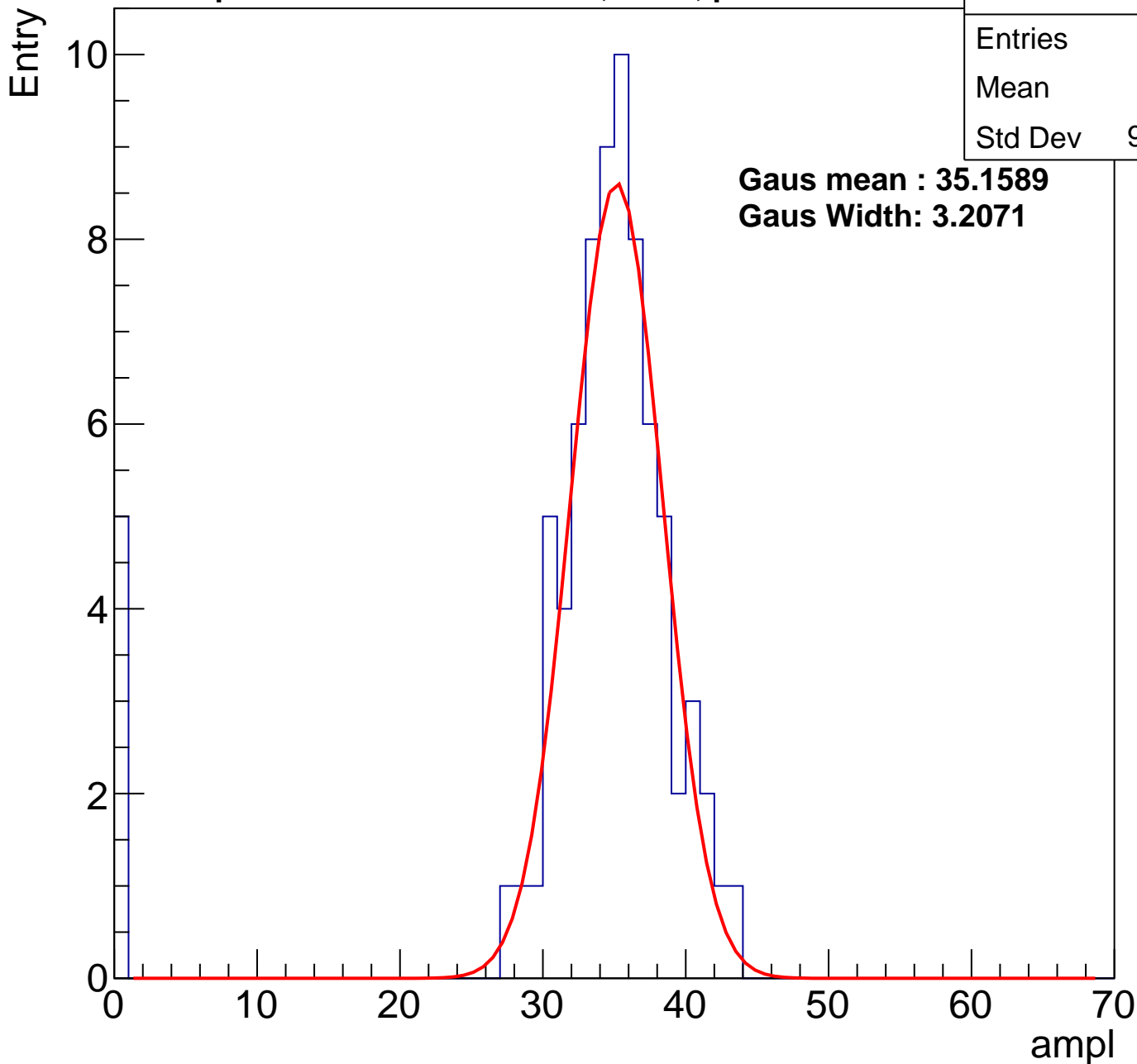


B1L103S, U7-ch20, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	78
Mean	32.5
Std Dev	9.086

Gaus mean : 35.1589
Gaus Width: 3.2071



B1L103S, U7-ch20, adc2

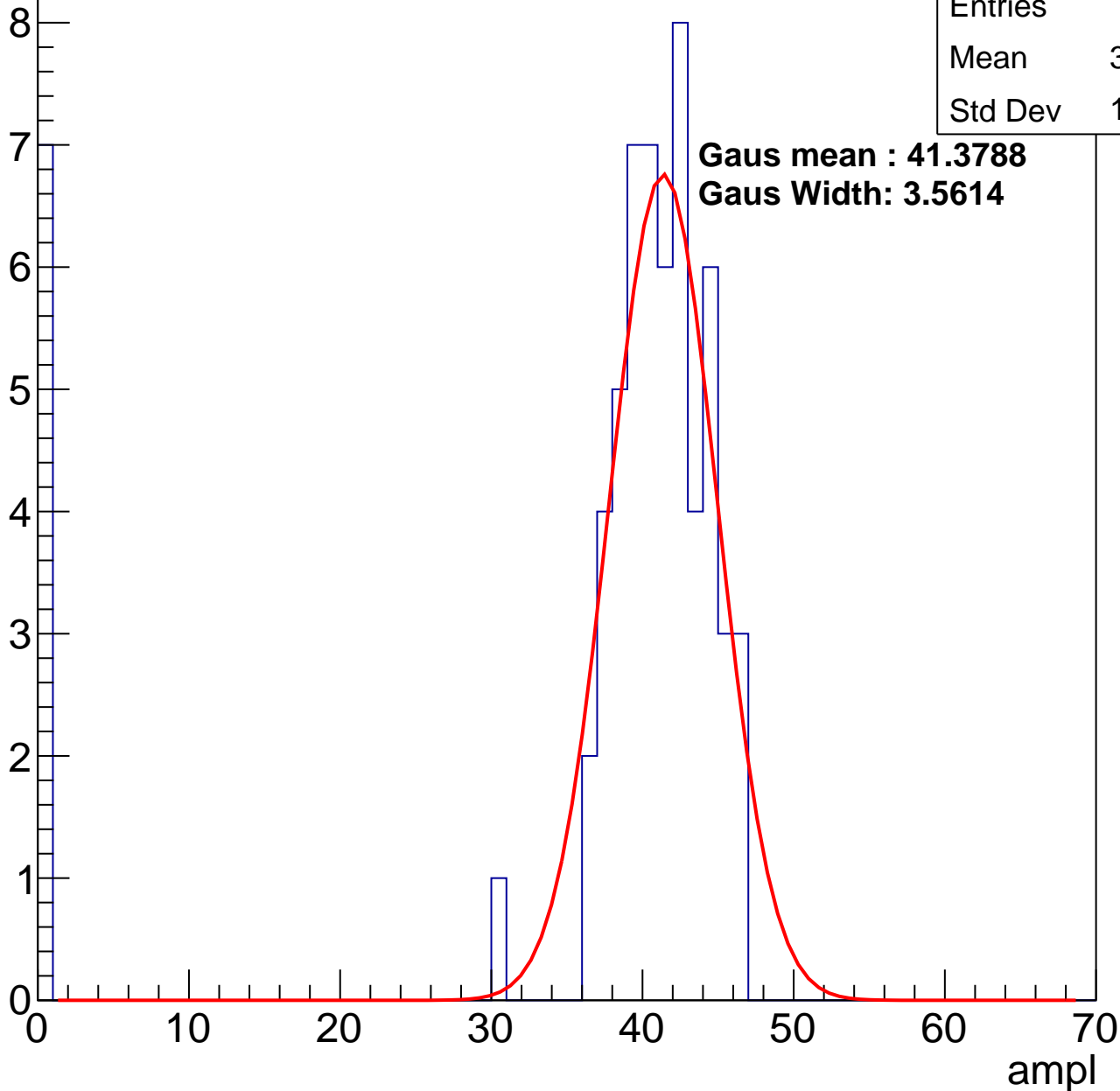
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	36.25
Std Dev	13.13

Gaus mean : 41.3788

Gaus Width: 3.5614

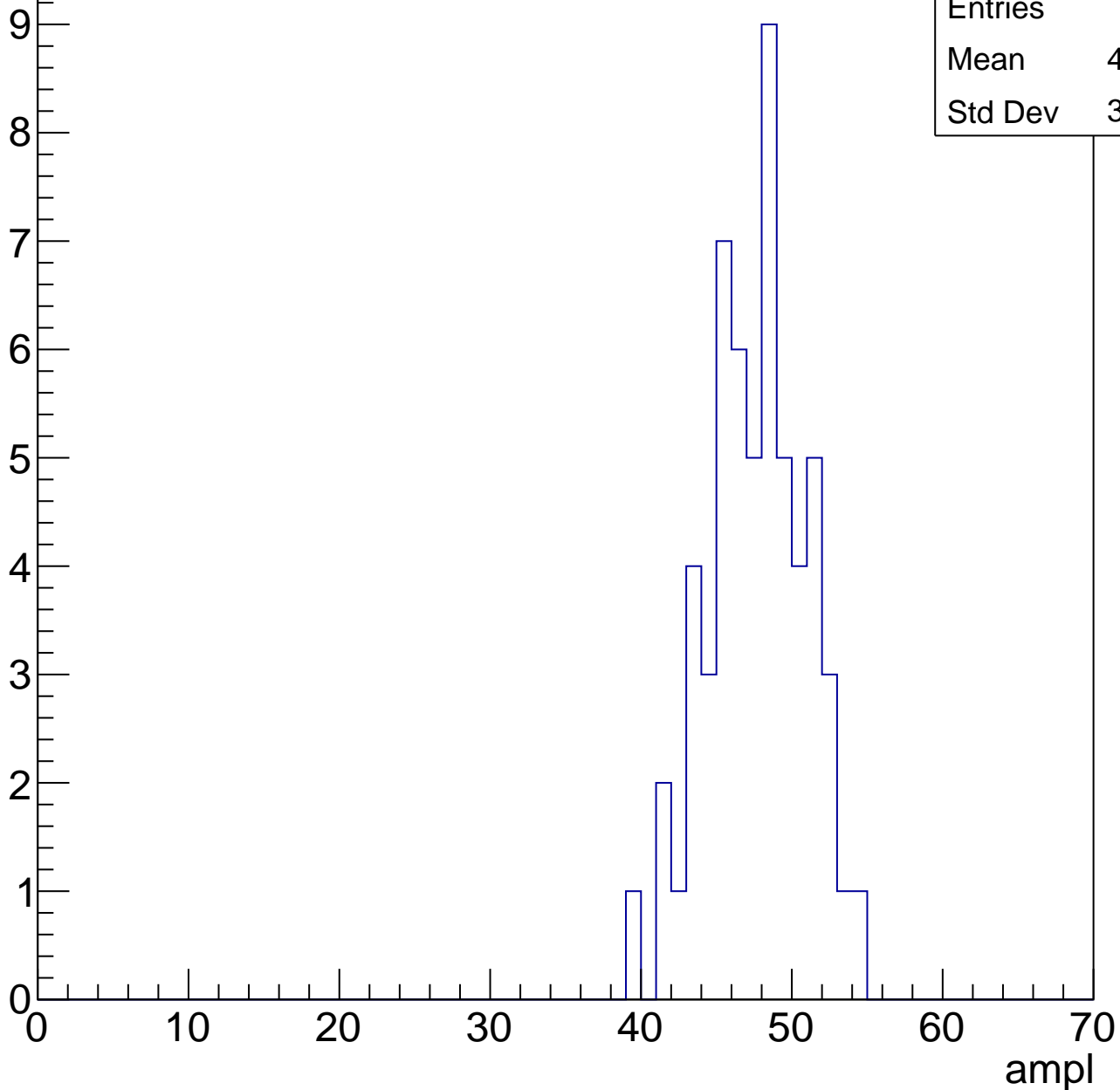


B1L103S, U7-ch20, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

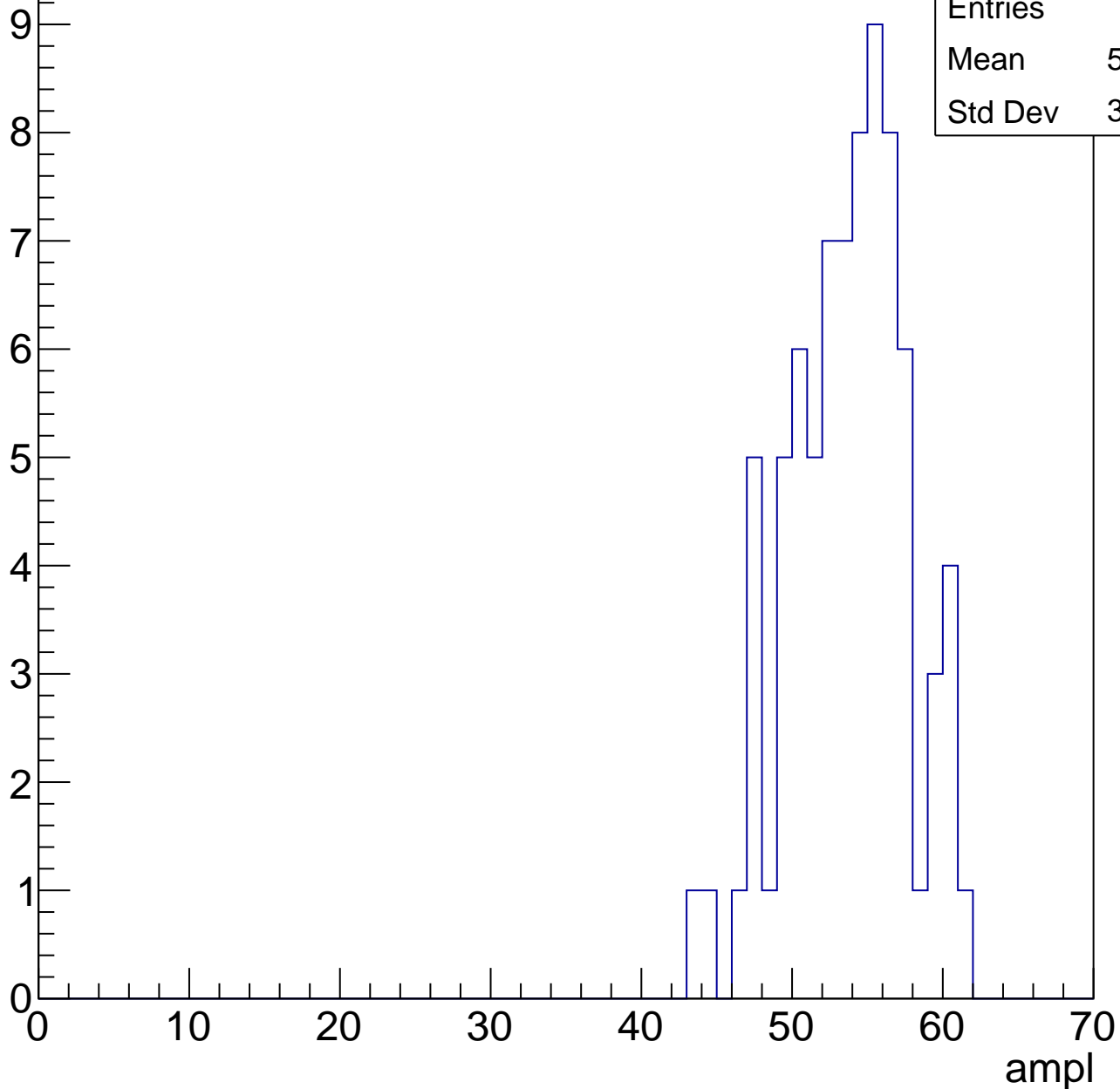
Entries	57
Mean	47.16
Std Dev	3.216



B1L103S, U7-ch20, adc4

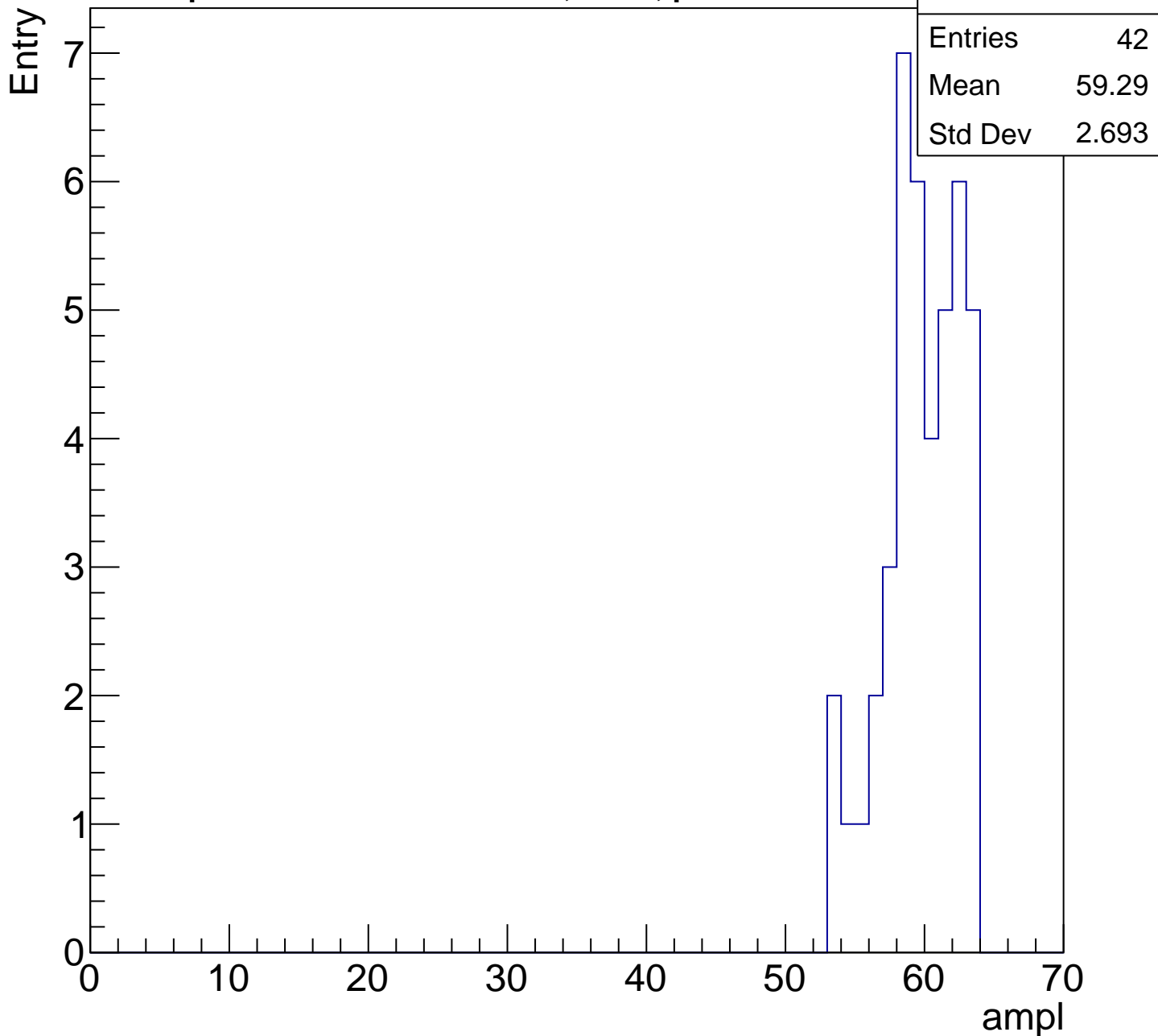
calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch20, adc5

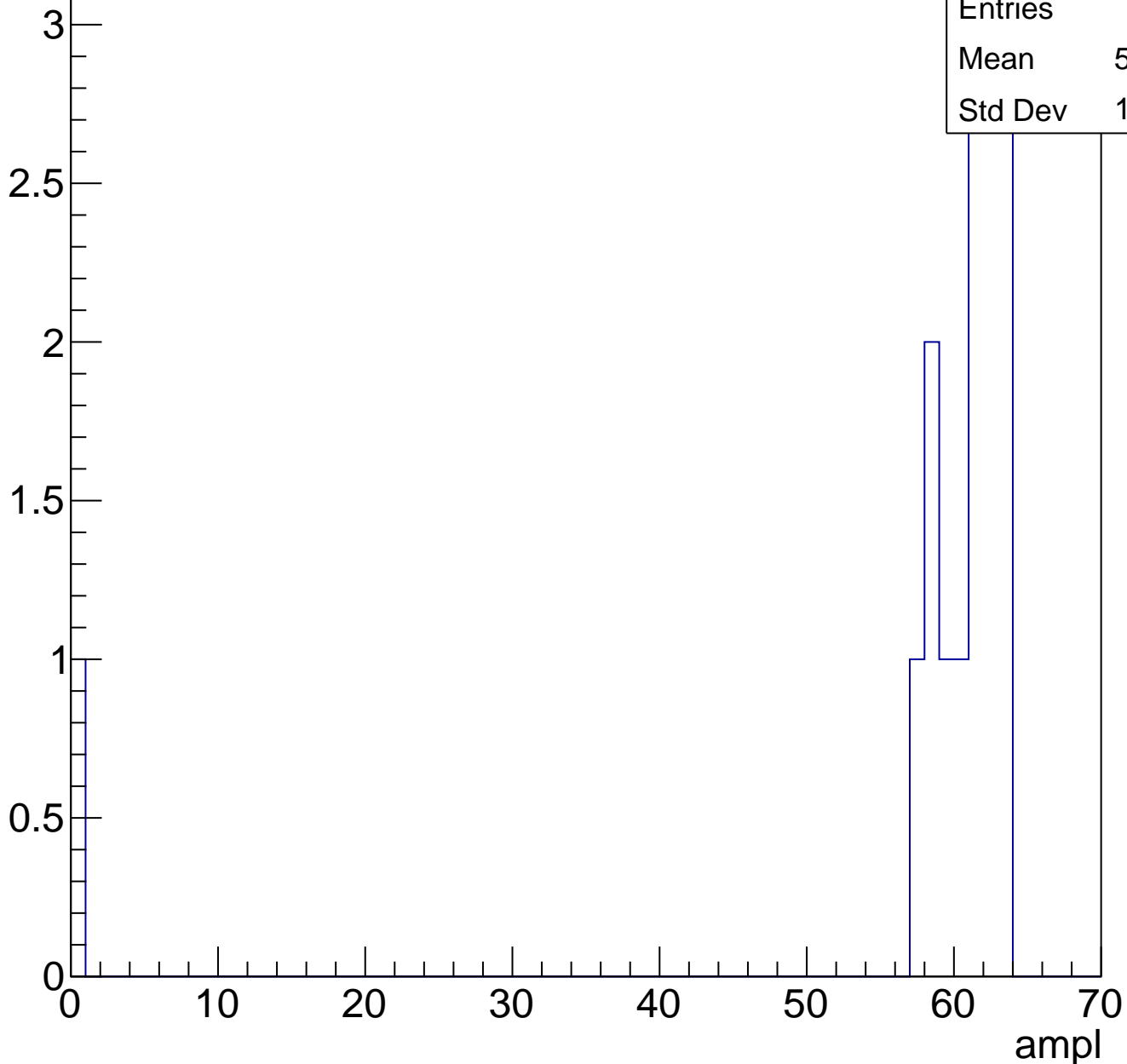
calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U7-ch20, adc6

calib_packv5_041523_1651.root, FC#0, port C2

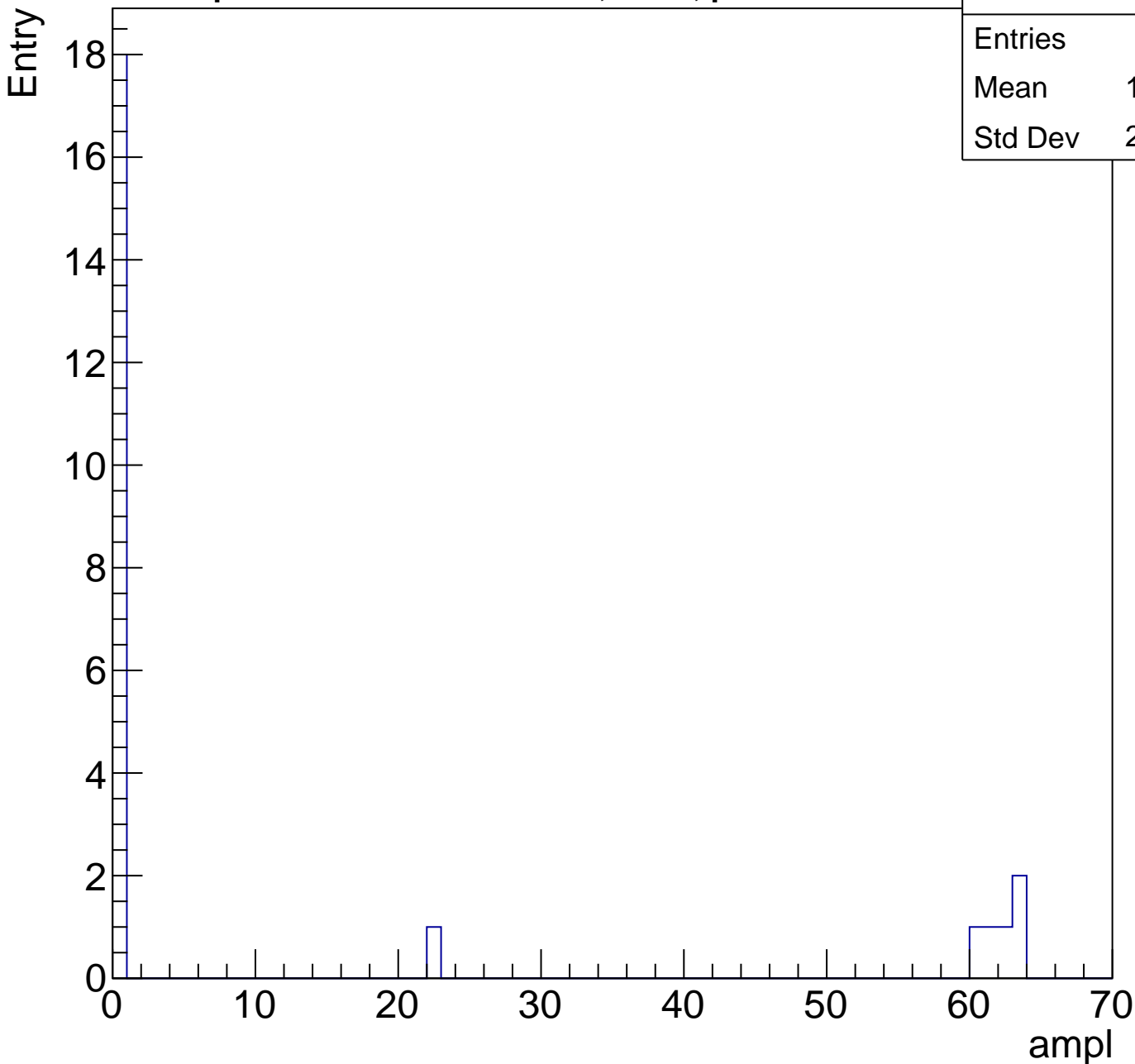
Entry



B1L103S, U7-ch20, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	24
Mean	13.79
Std Dev	25.02



B1L103S, U7-ch21, adc0

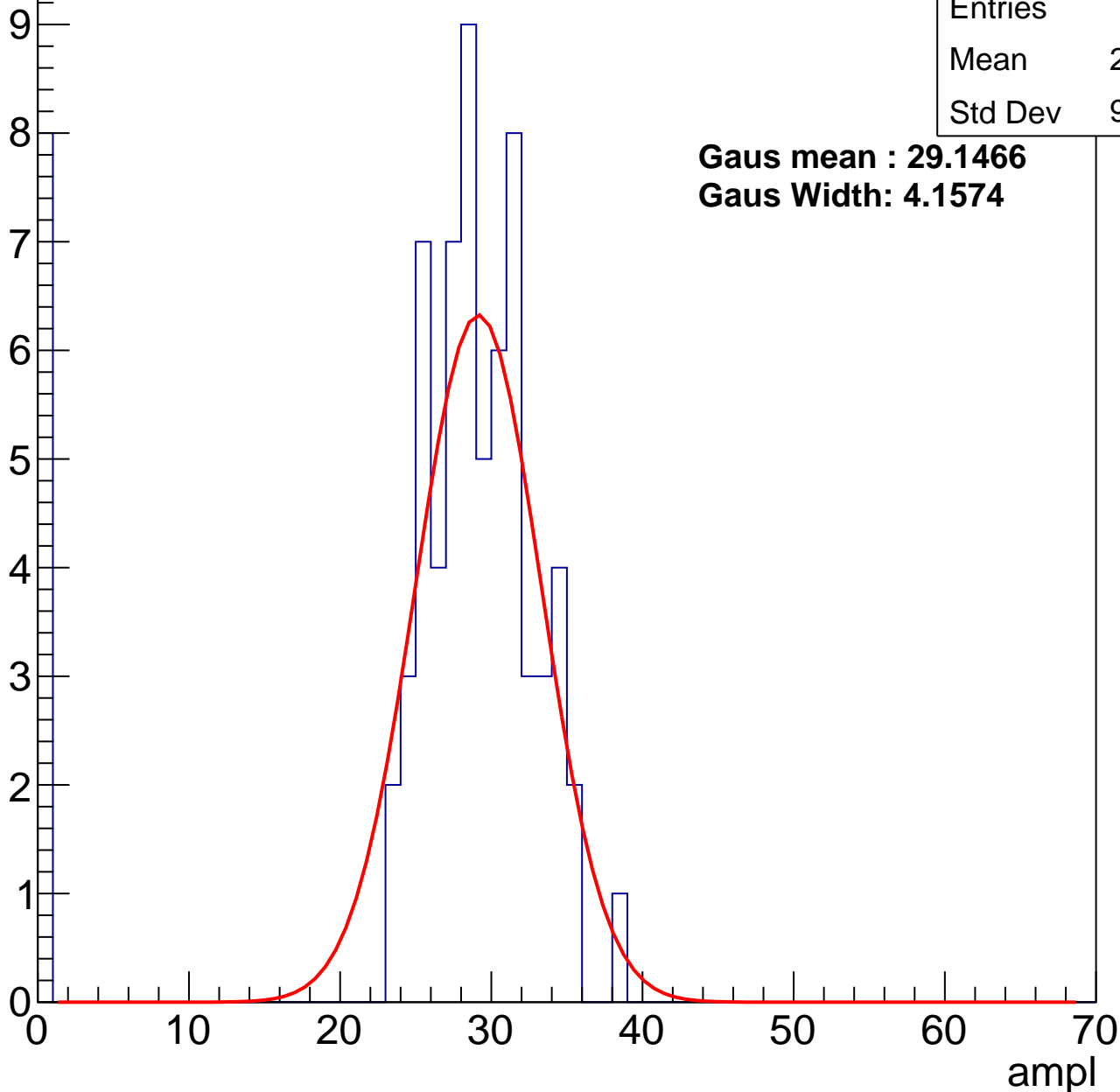
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	25.69
Std Dev	9.603

Gaus mean : 29.1466

Gaus Width: 4.1574



B1L103S, U7-ch21, adc1

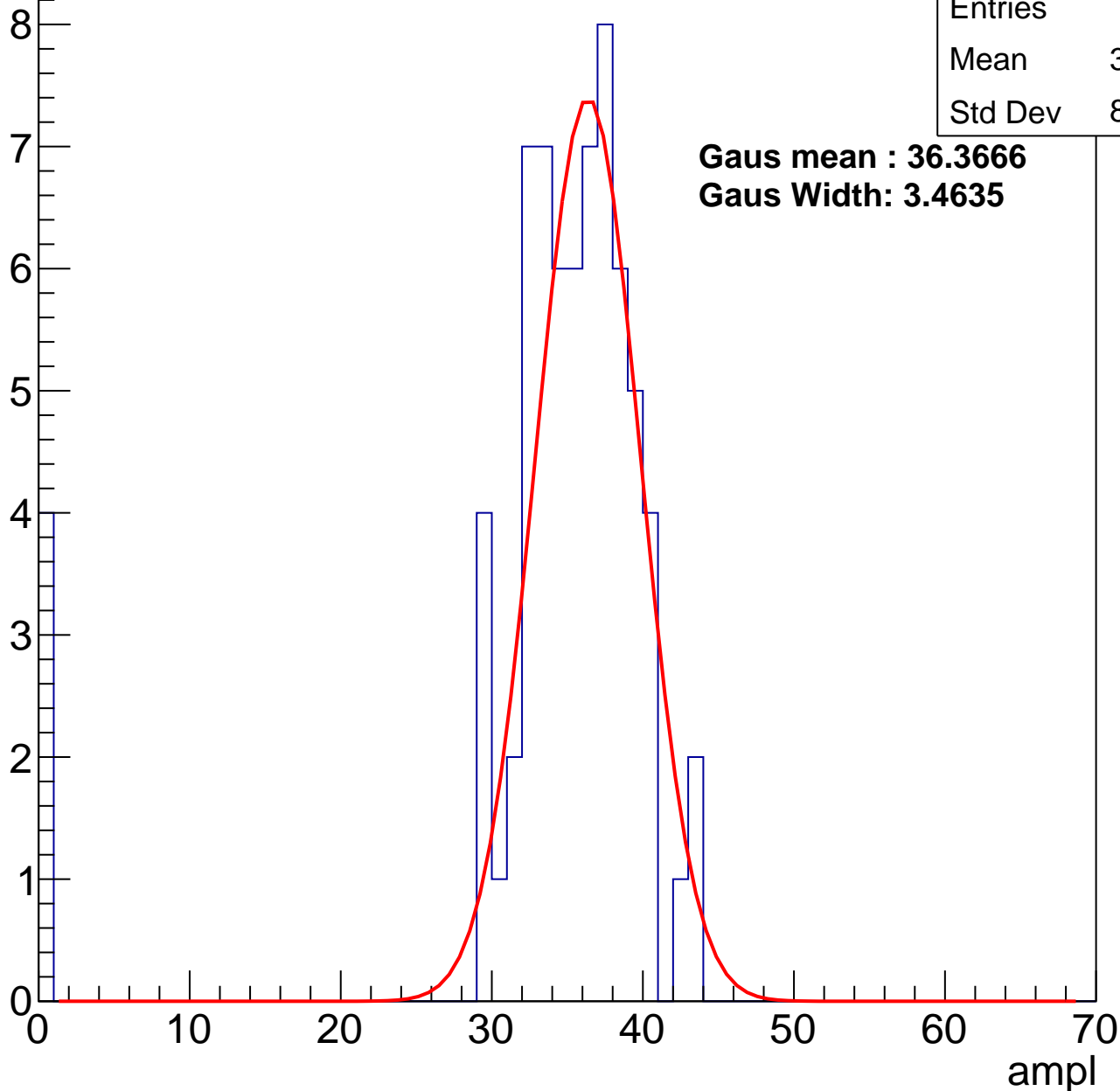
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	33.37
Std Dev	8.834

Gaus mean : 36.3666

Gaus Width: 3.4635



B1L103S, U7-ch21, adc2

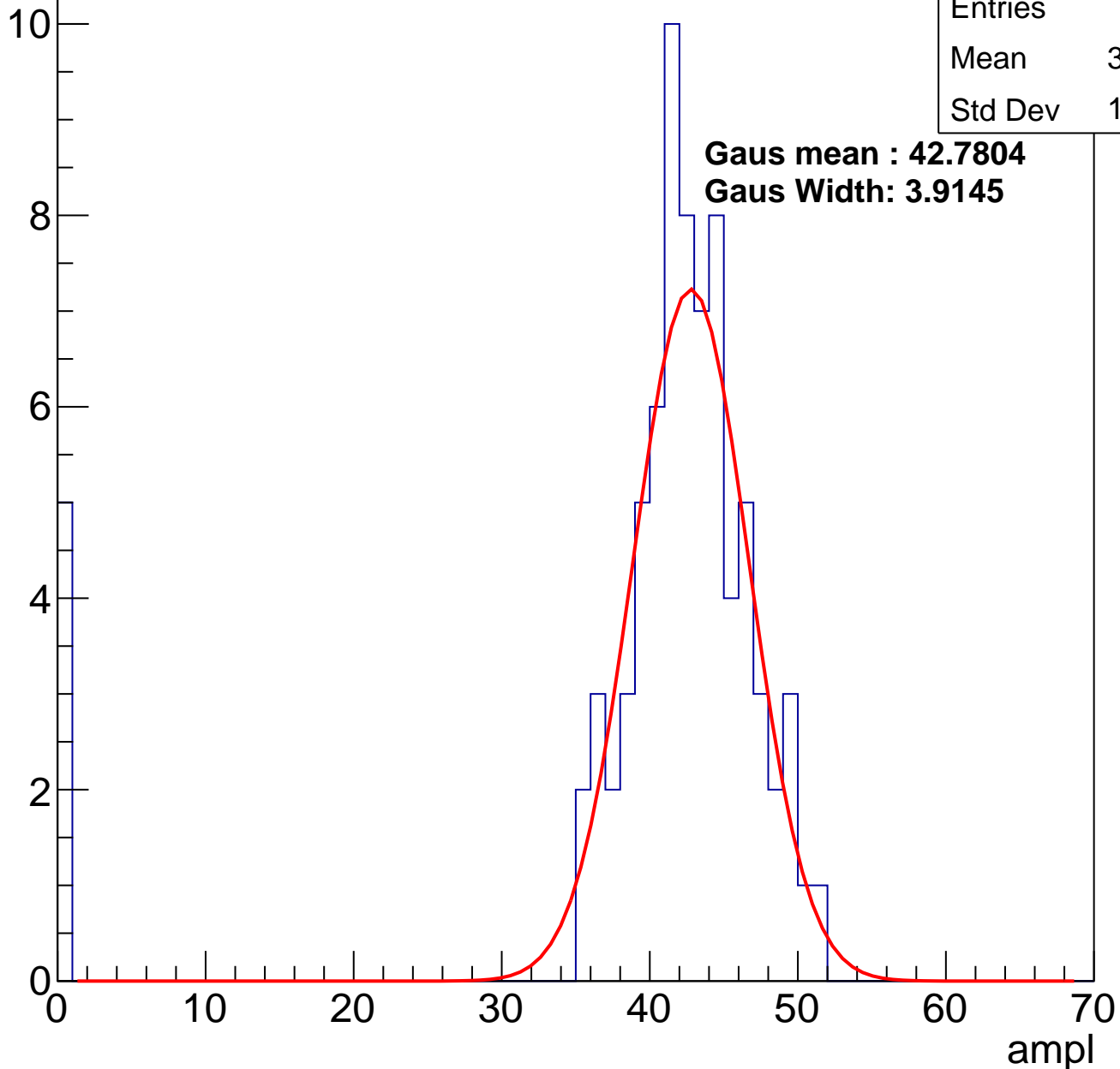
calib_packv5_041523_1651.root, FC#0, port C2

Entries	78
Mean	39.68
Std Dev	10.96

Gaus mean : 42.7804

Gaus Width: 3.9145

Entry

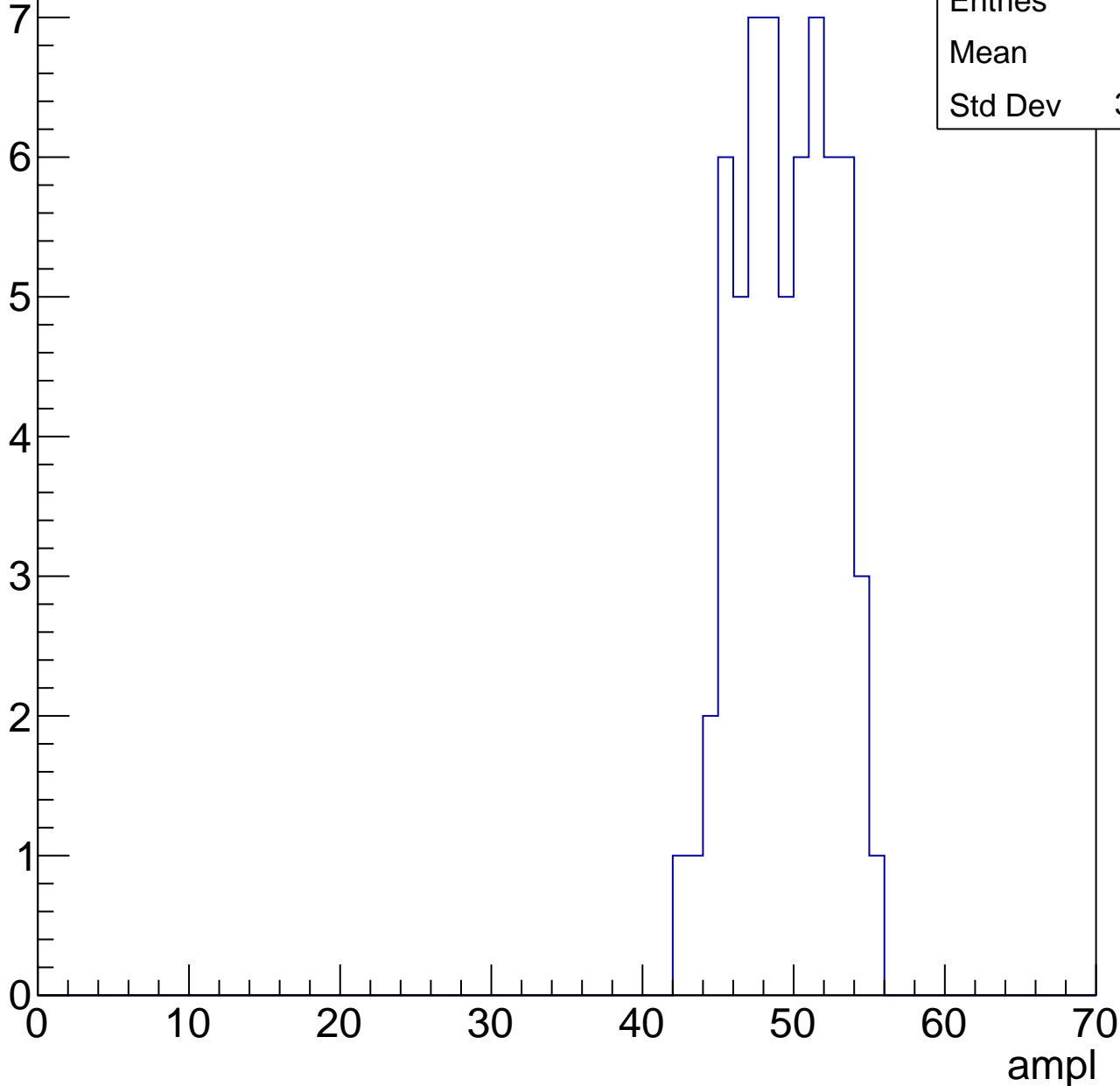


B1L103S, U7-ch21, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

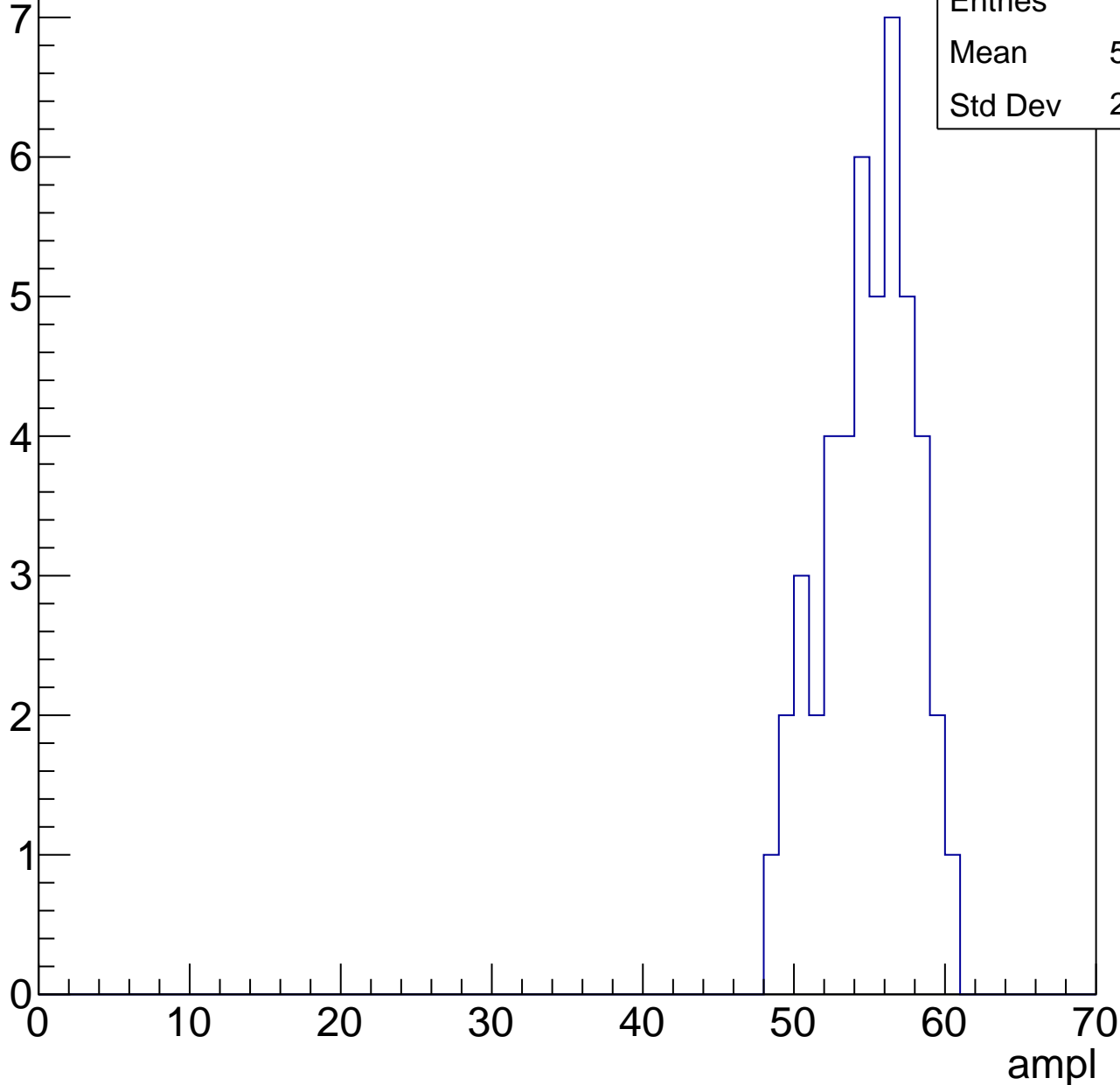
Entries	63
Mean	49
Std Dev	3.101



B1L103S, U7-ch21, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



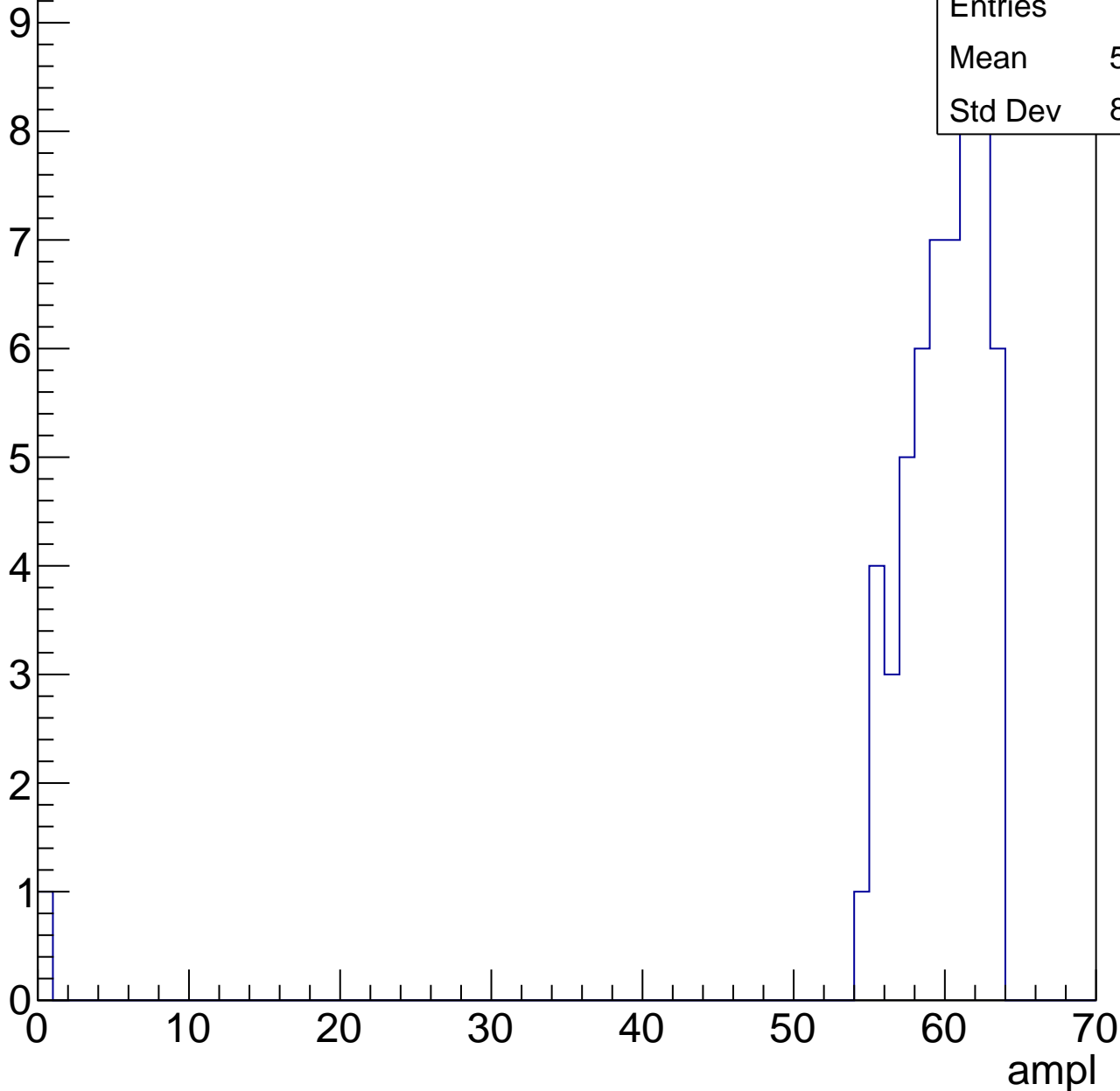
Entries	46
Mean	54.43
Std Dev	2.917

B1L103S, U7-ch21, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

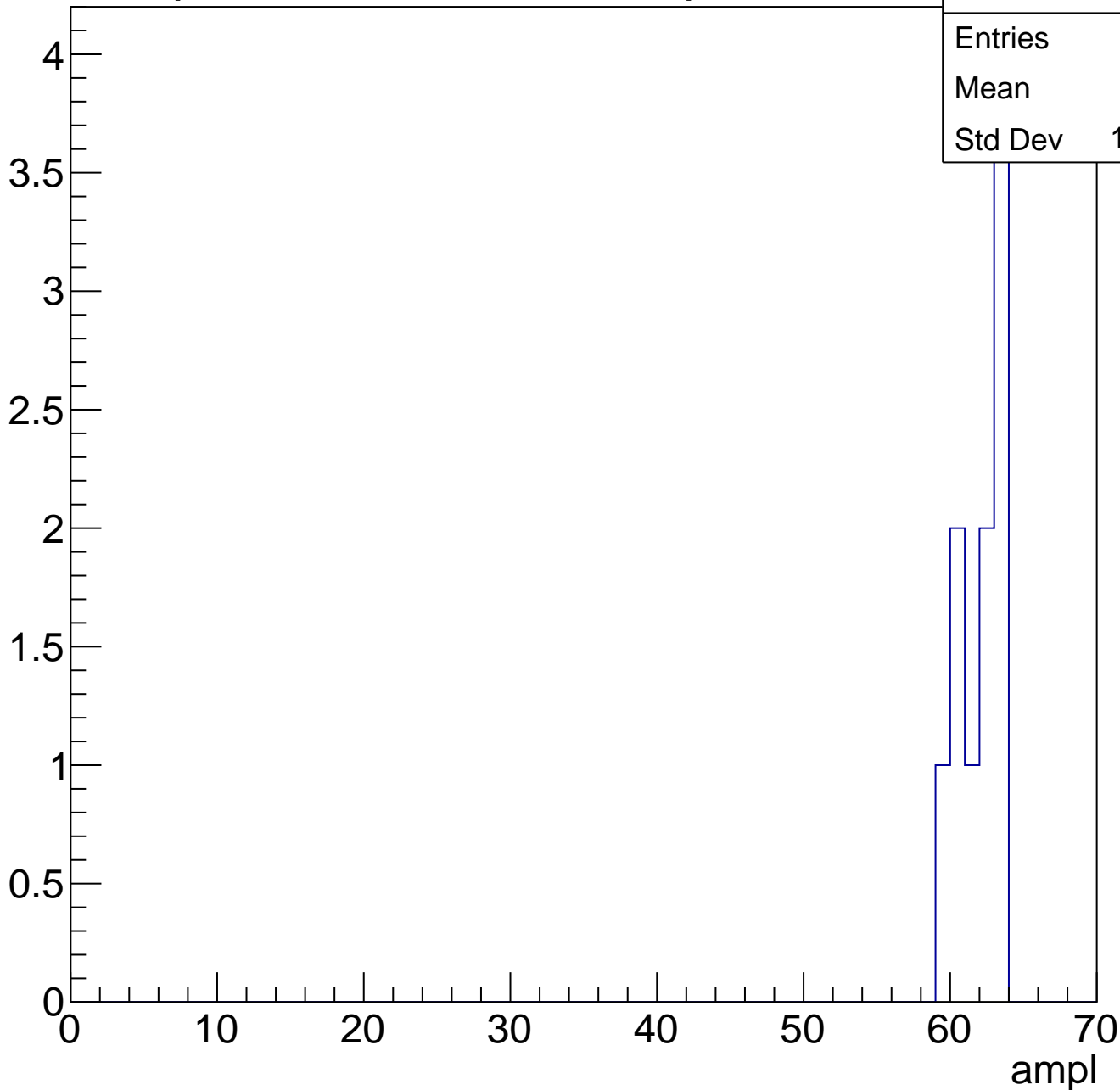
Entries	57
Mean	58.44
Std Dev	8.182



B1L103S, U7-ch21, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

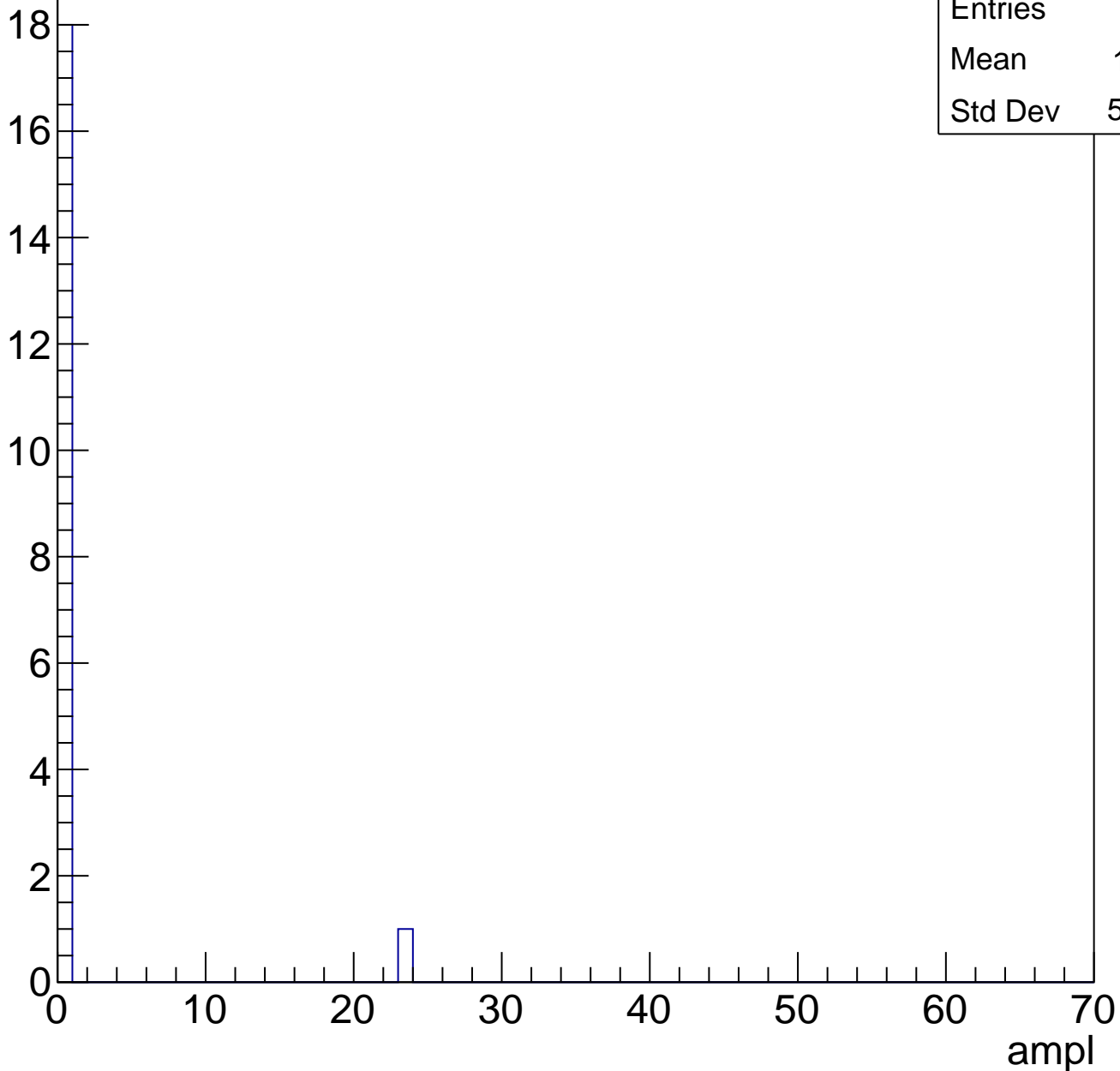


Entries	10
Mean	61.6
Std Dev	1.428

B1L103S, U7-ch21, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch22, adc0

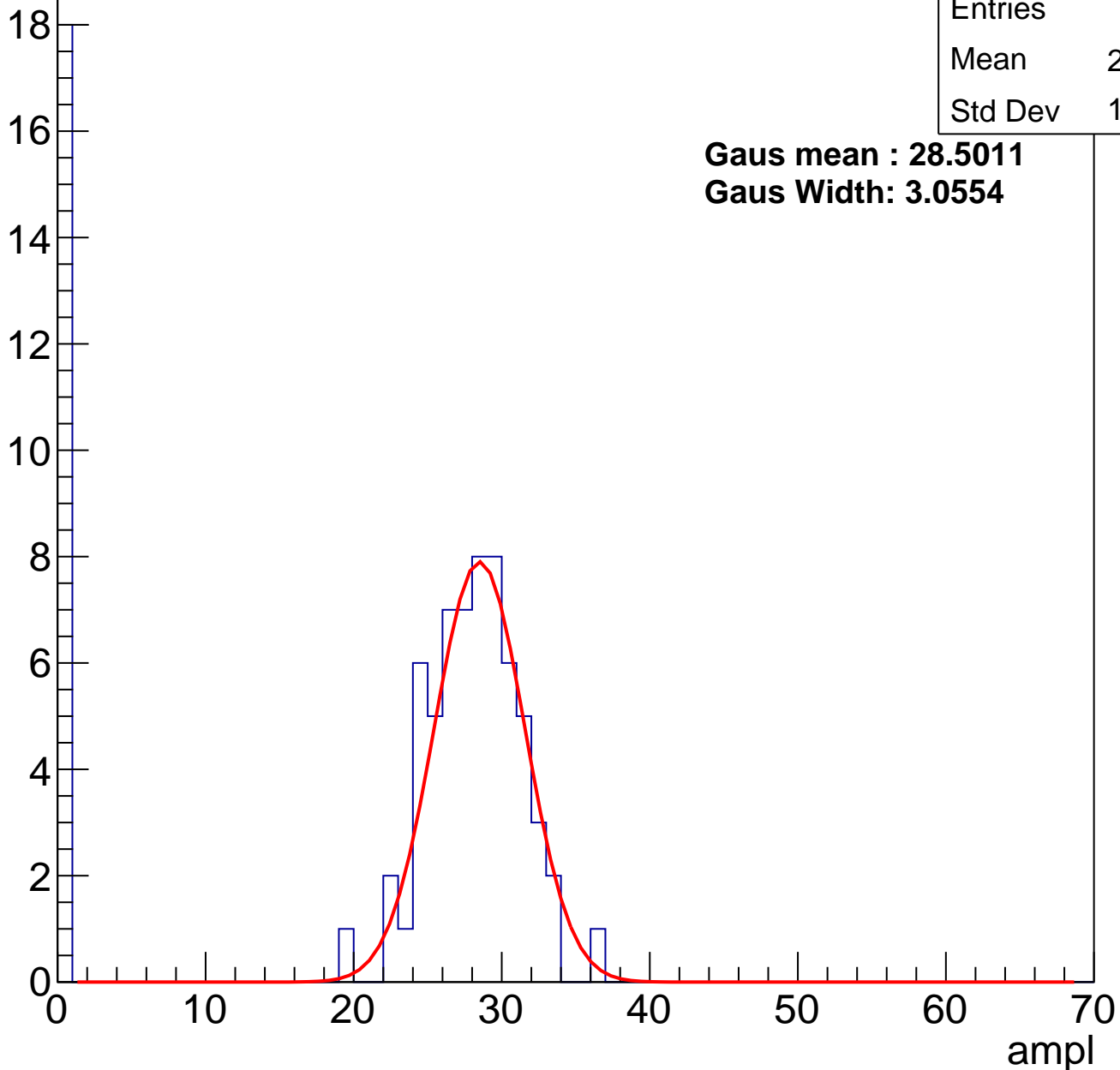
calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	21.44
Std Dev	11.86

Gaus mean : 28.5011

Gaus Width: 3.0554

Entry



B1L103S, U7-ch22, adc1

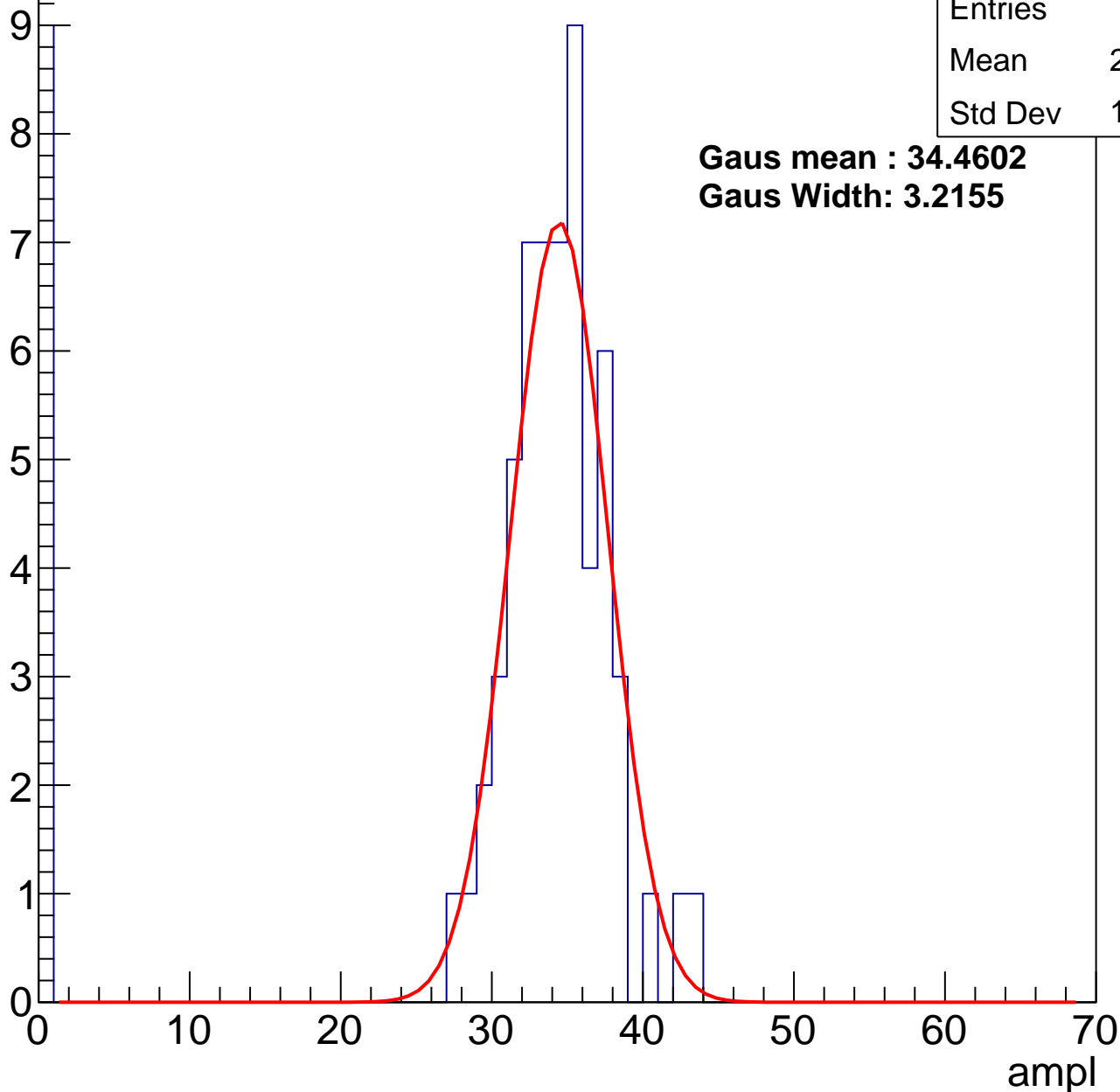
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	29.42
Std Dev	11.95

Gaus mean : 34.4602

Gaus Width: 3.2155



B1L103S, U7-ch22, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	86
Mean	39.15
Std Dev	8.236

Gaus mean : 41.3829

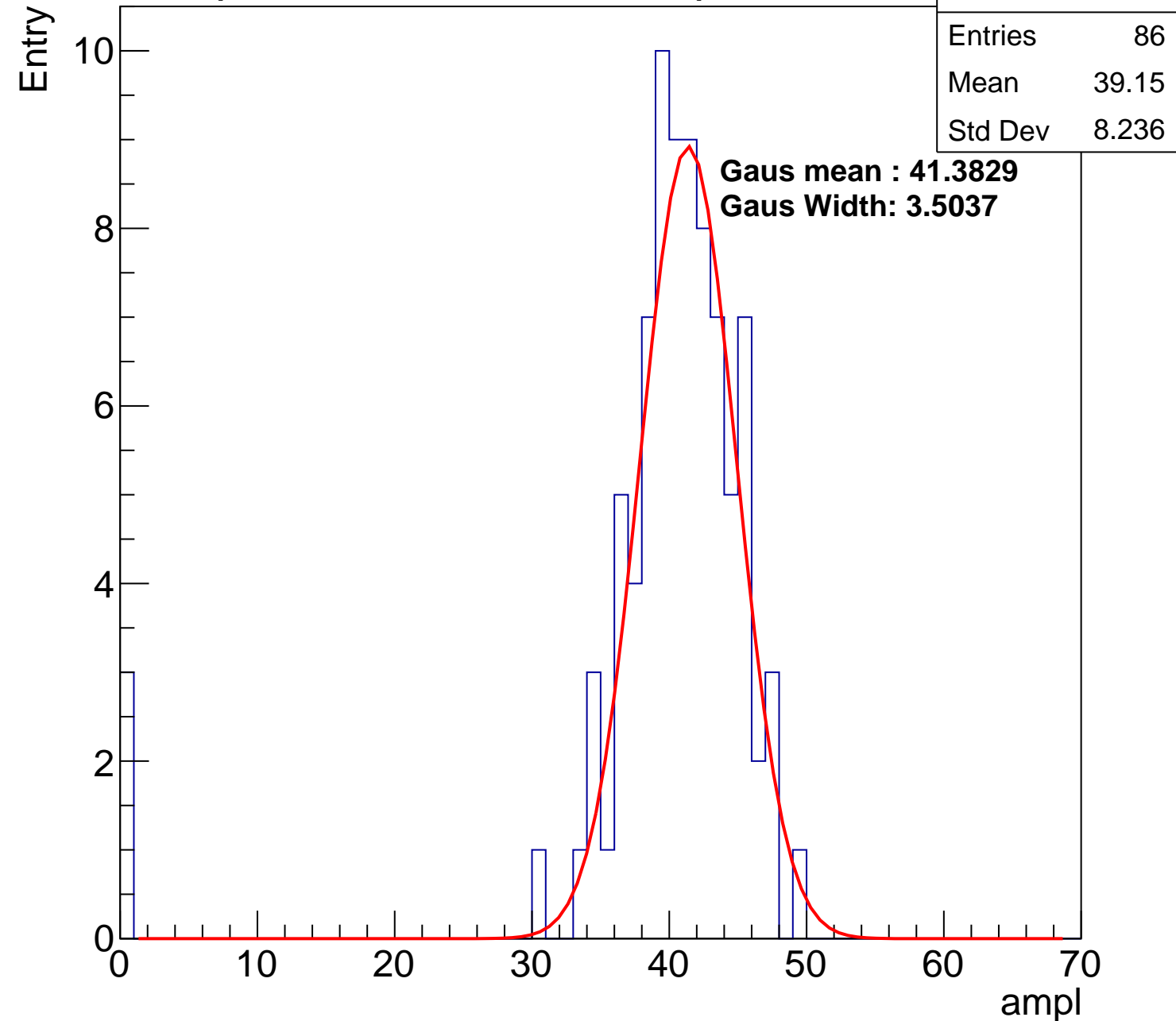
Gaus Width: 3.5037

Entry

10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

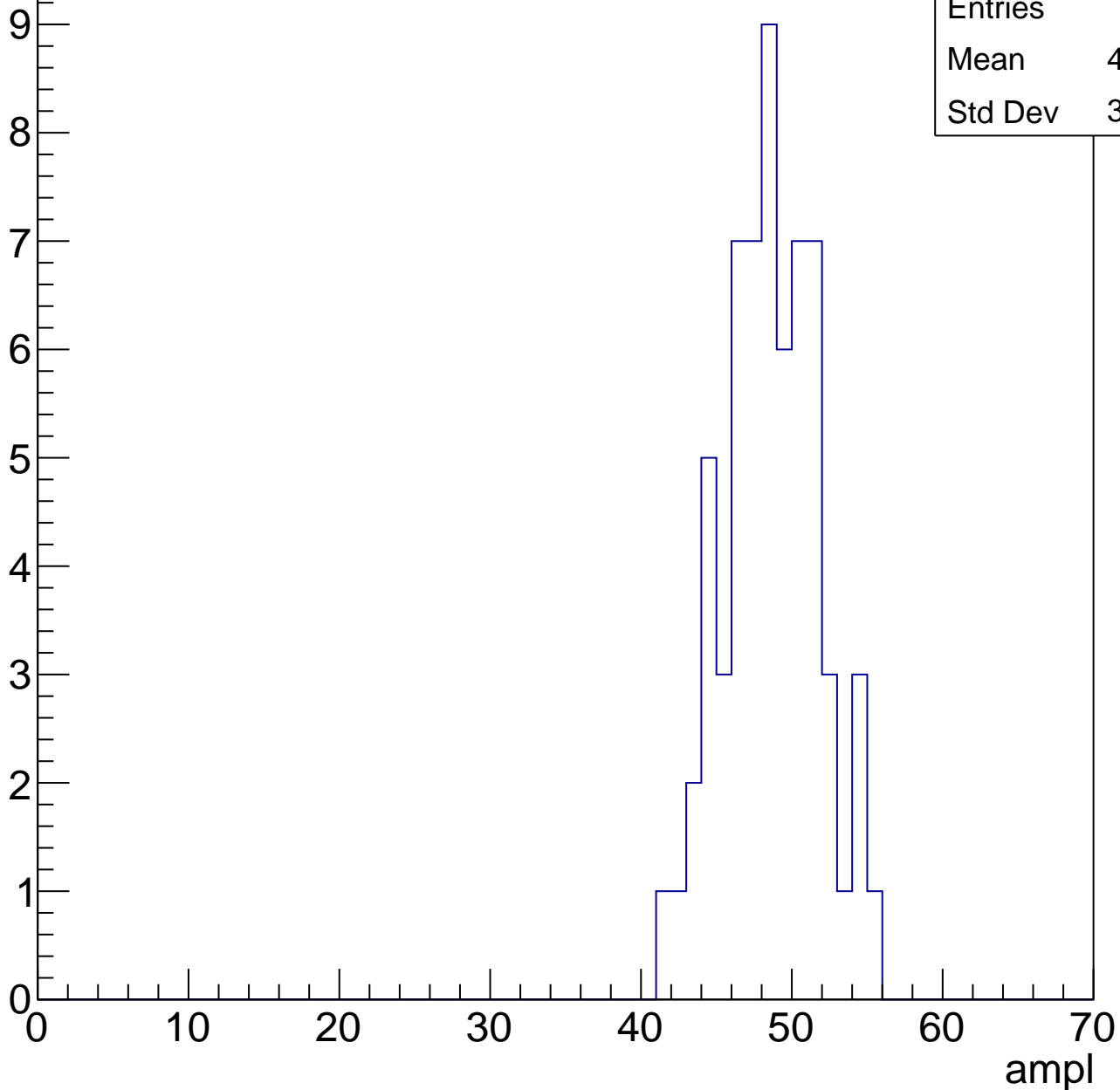


B1L103S, U7-ch22, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	48.16
Std Dev	3.092

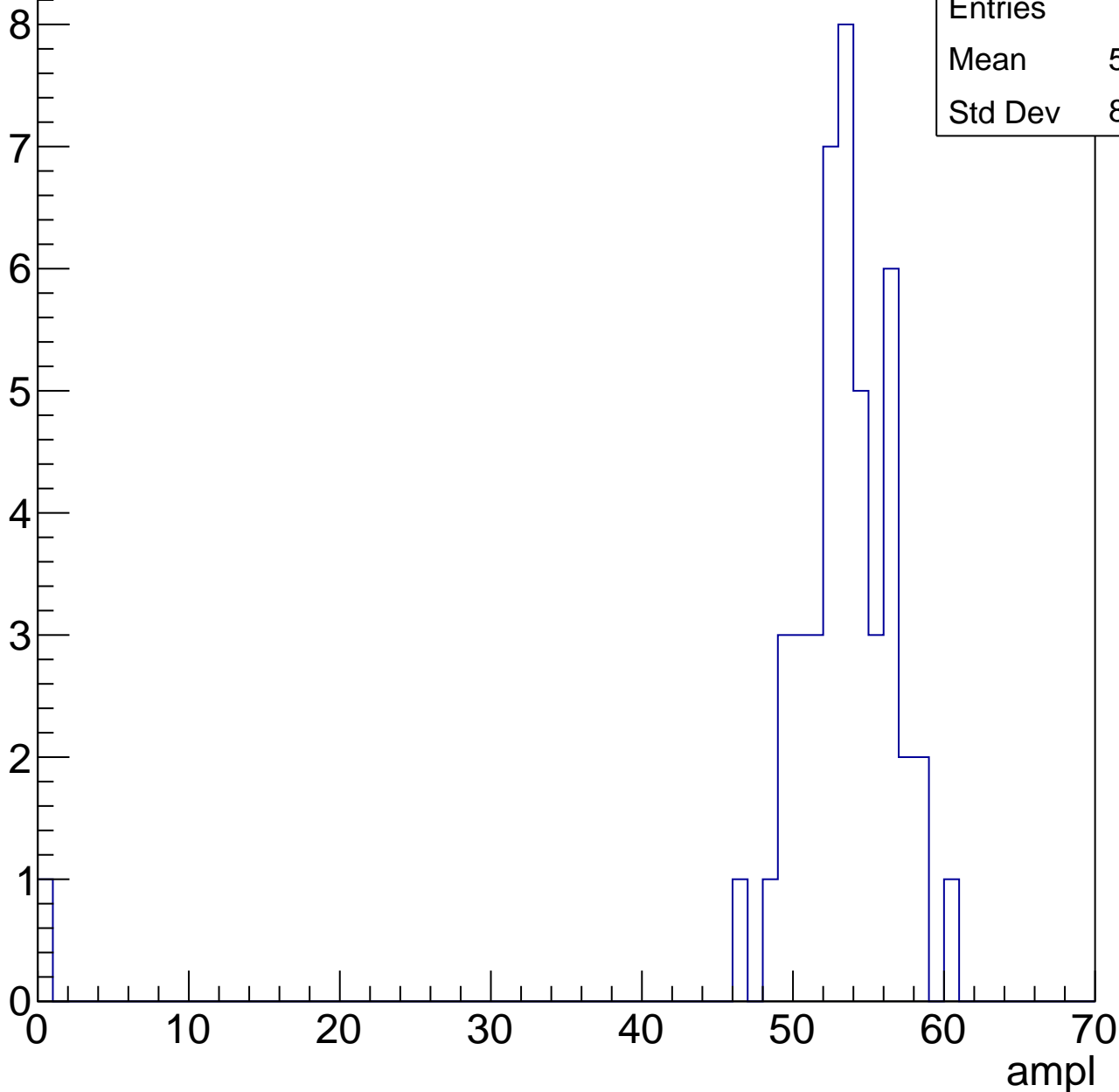


B1L103S, U7-ch22, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	46
Mean	52.02
Std Dev	8.255



B1L103S, U7-ch22, adc5

calib_packv5_041523_1651.root, FC#0, port C2

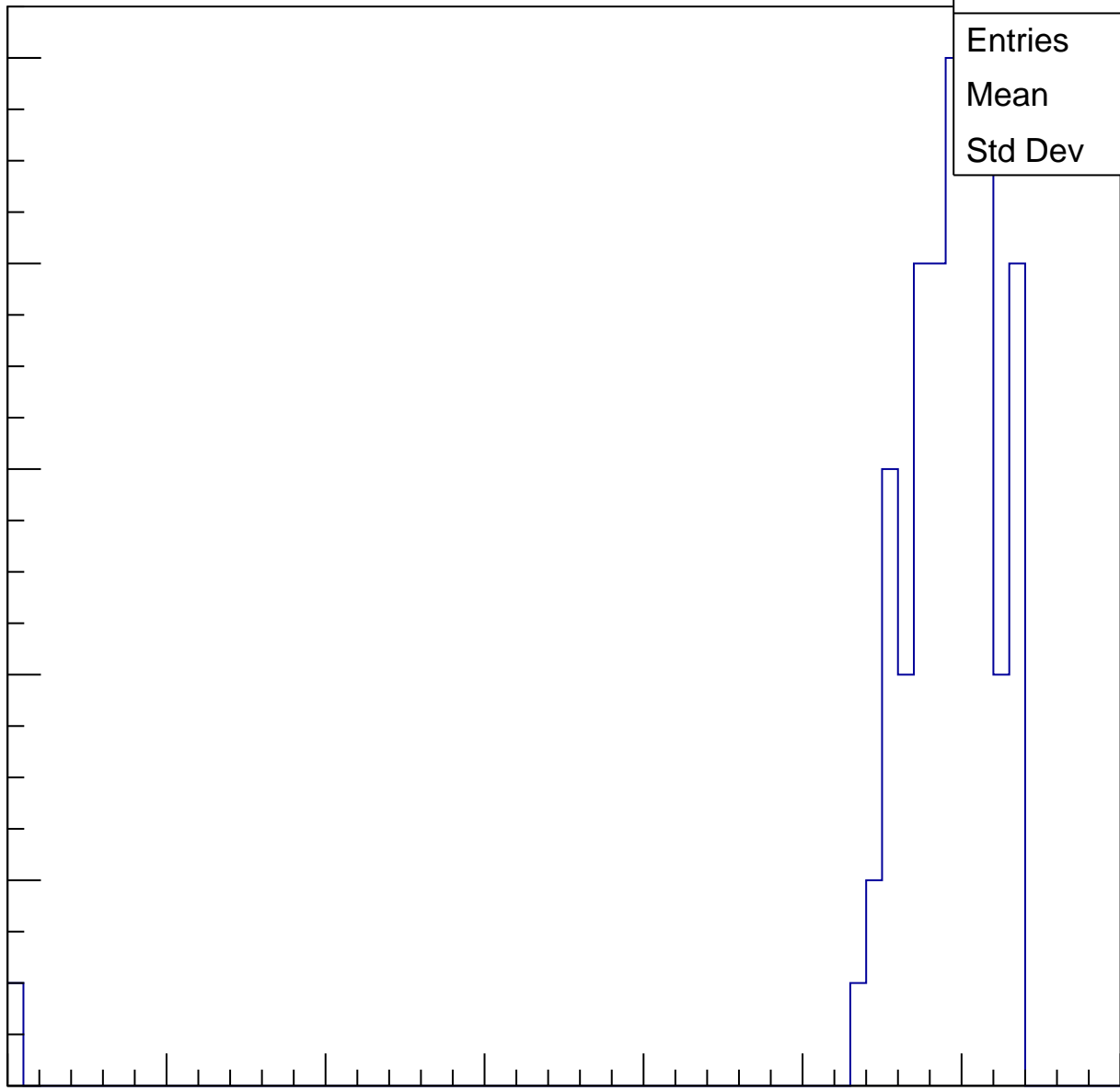
Entries	70
Mean	58.09
Std Dev	7.454

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

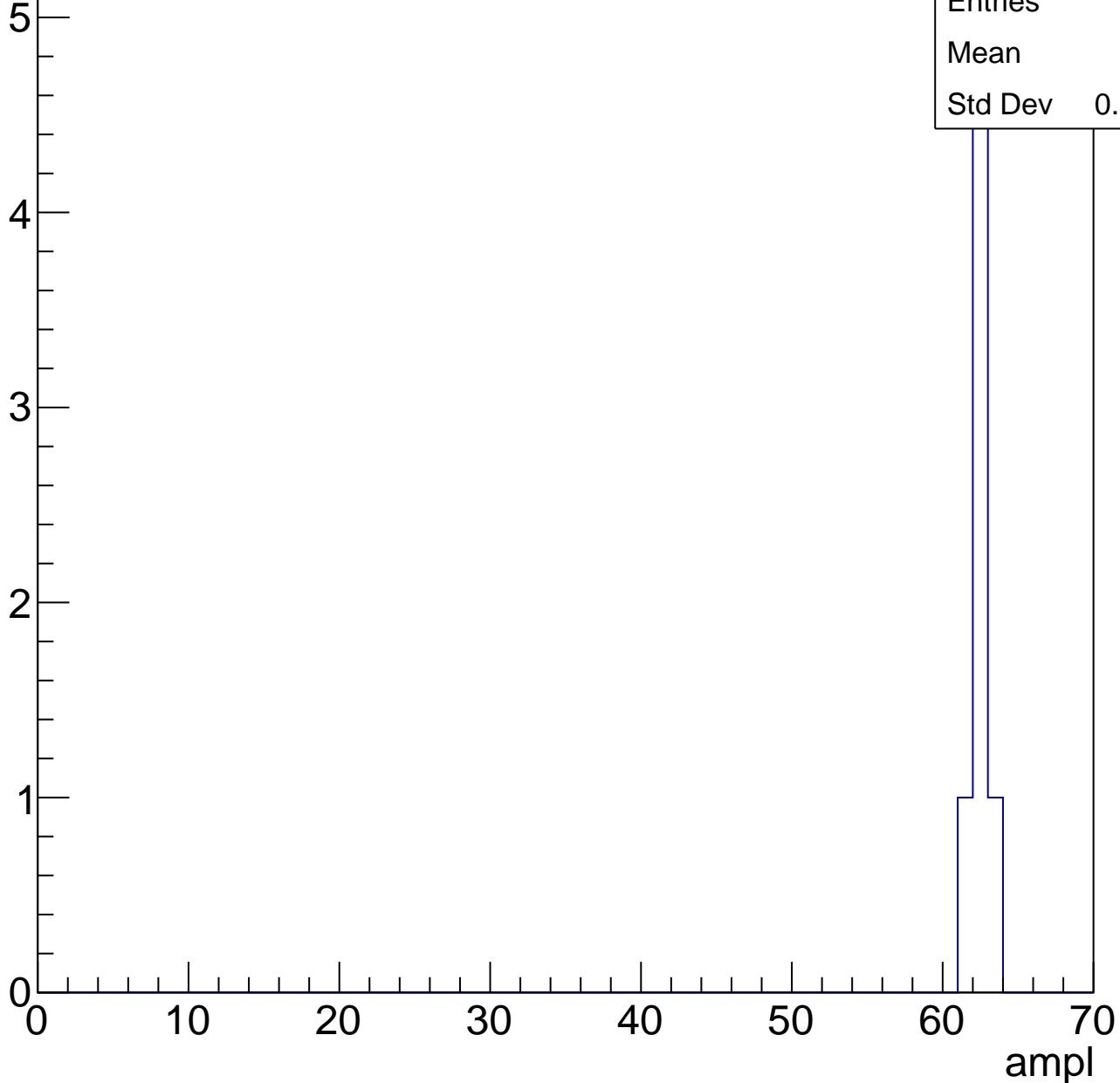


B1L103S, U7-ch22, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

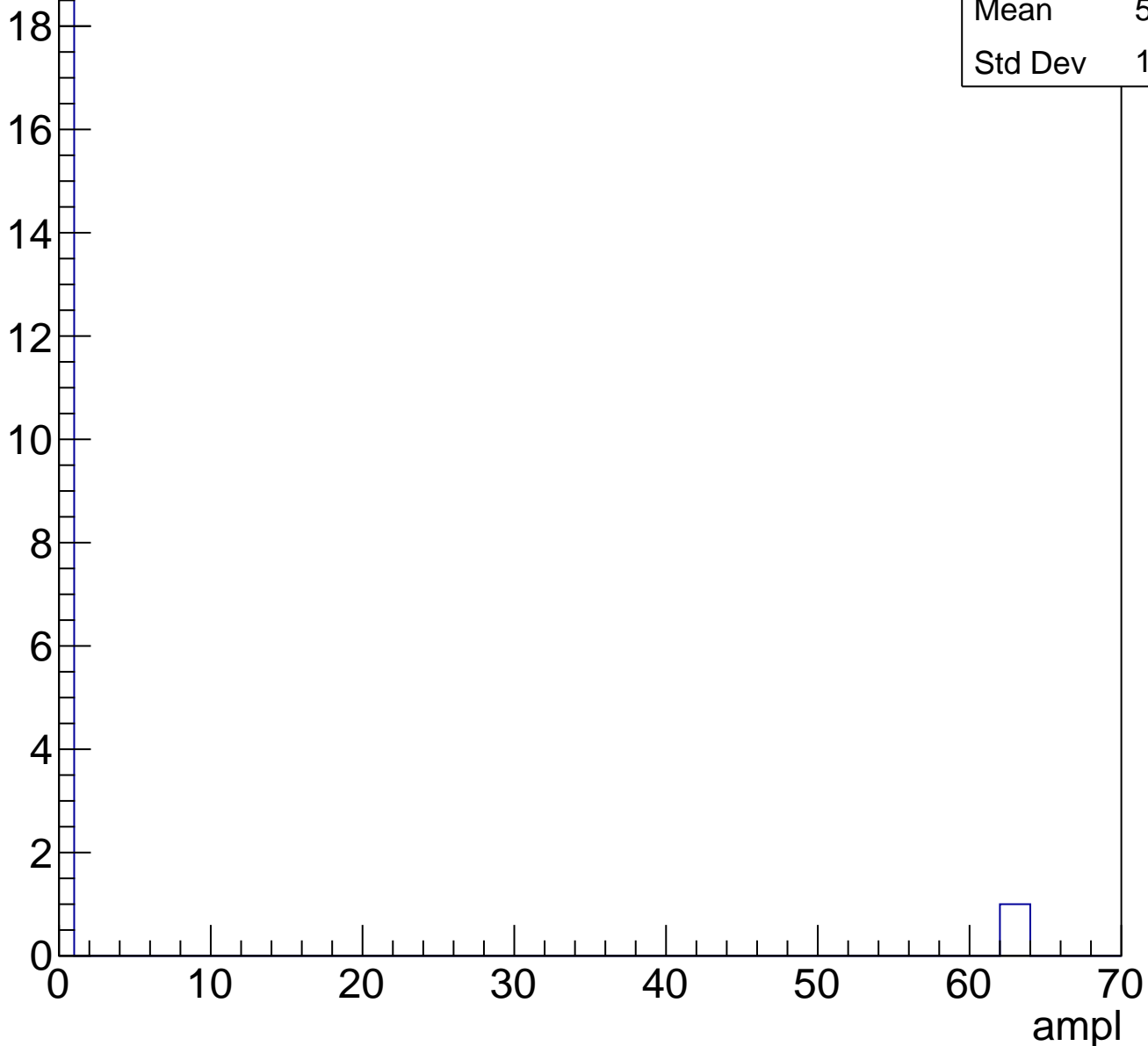
Entries	7
Mean	62
Std Dev	0.5345



B1L103S, U7-ch22, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



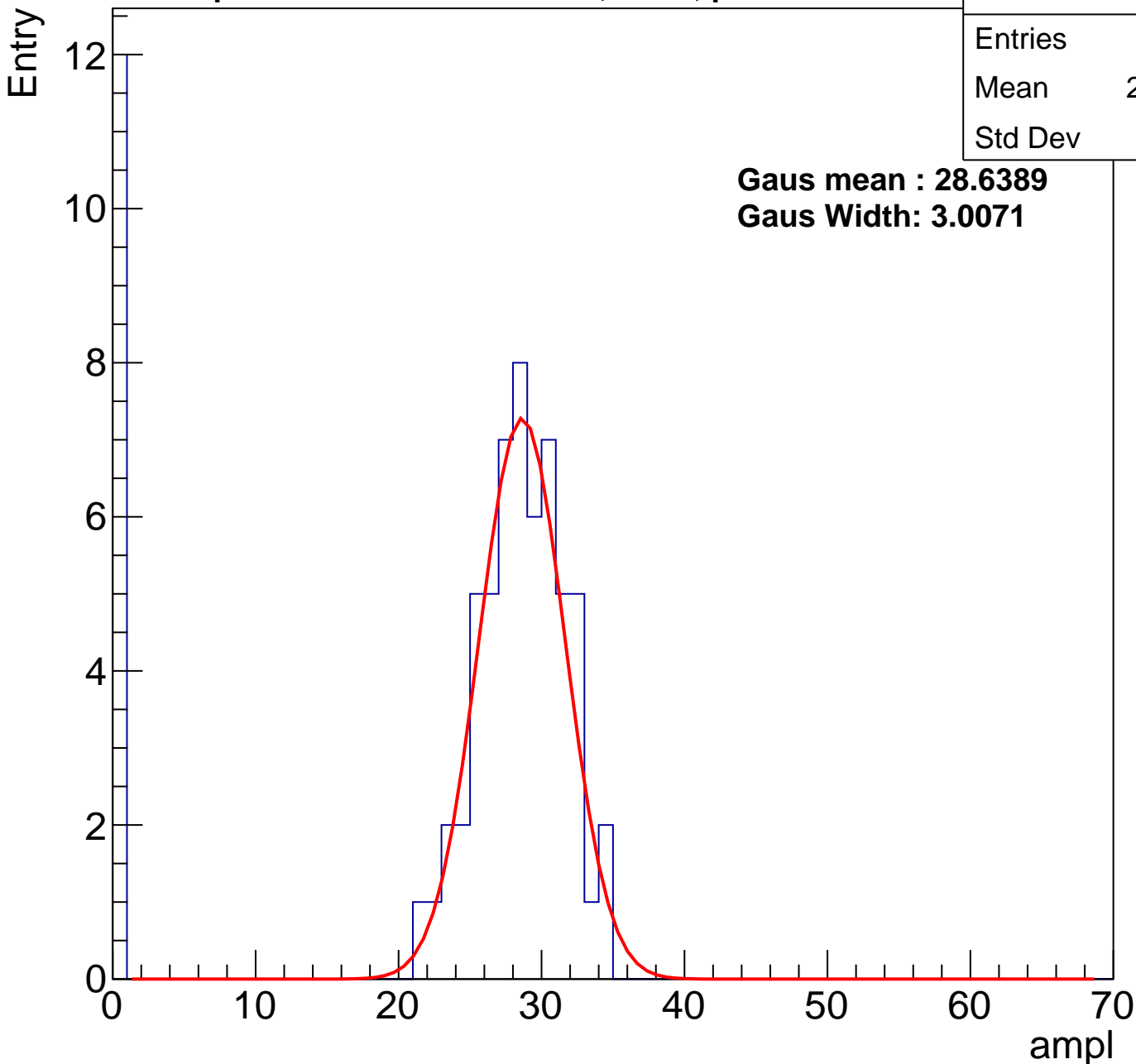
B1L103S, U7-ch23, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	69
Mean	23.26
Std Dev	11

Gaus mean : 28.6389

Gaus Width: 3.0071



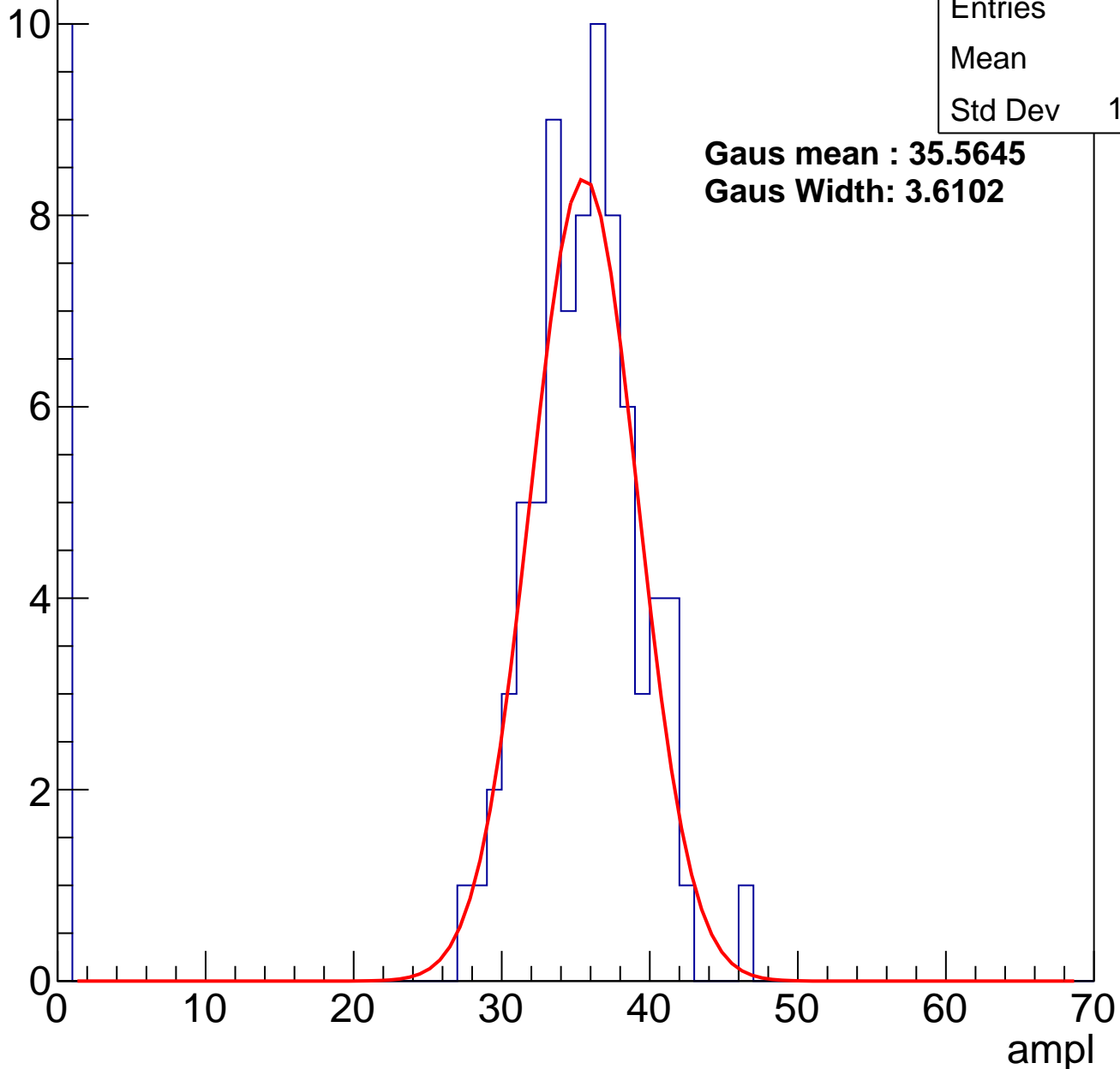
B1L103S, U7-ch23, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	88
Mean	31.2
Std Dev	11.66

Gaus mean : 35.5645
Gaus Width: 3.6102

Entry



B1L103S, U7-ch23, adc2

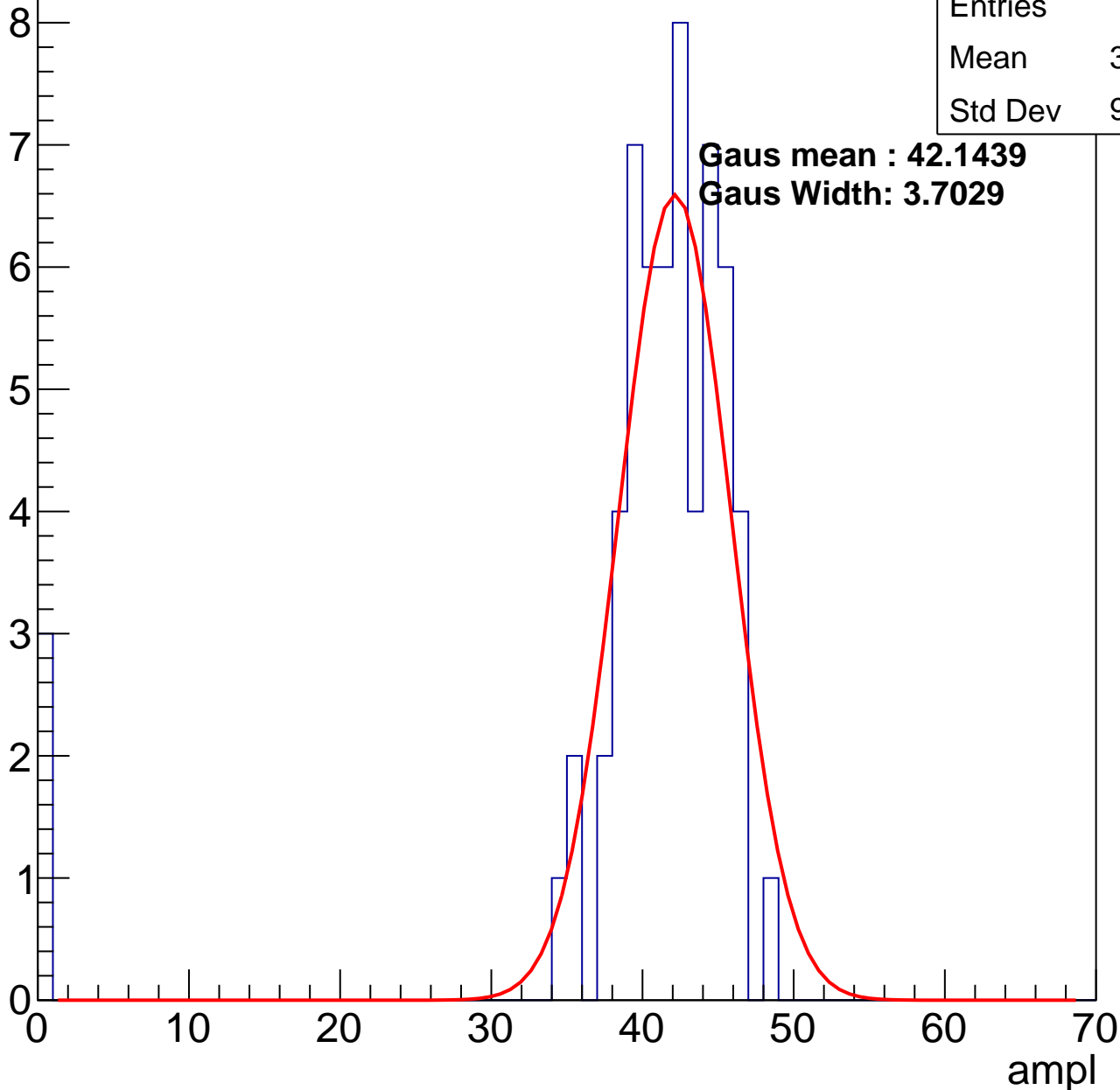
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	39.46
Std Dev	9.455

Gaus mean : 42.1439

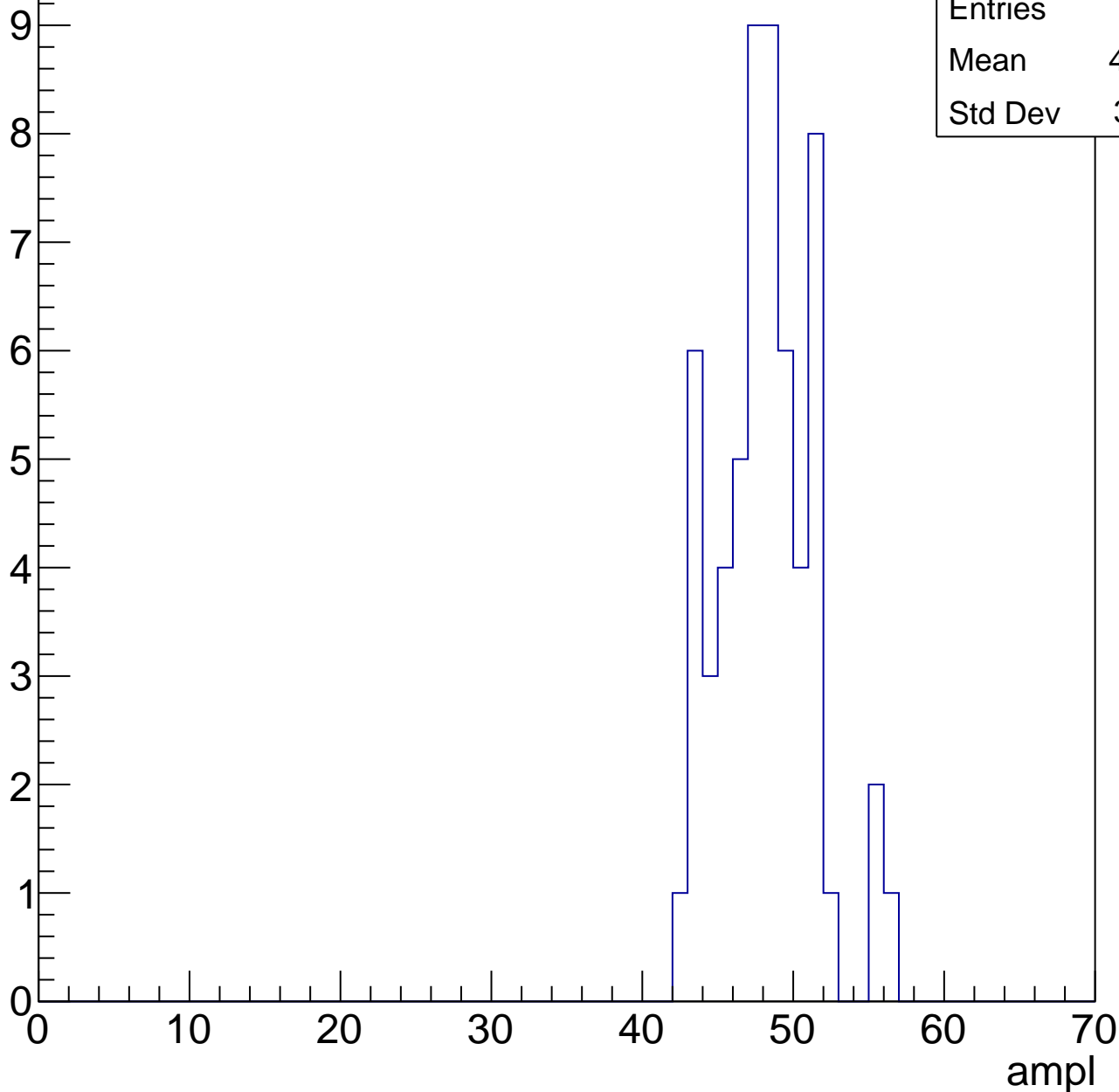
Gaus Width: 3.7029



B1L103S, U7-ch23, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

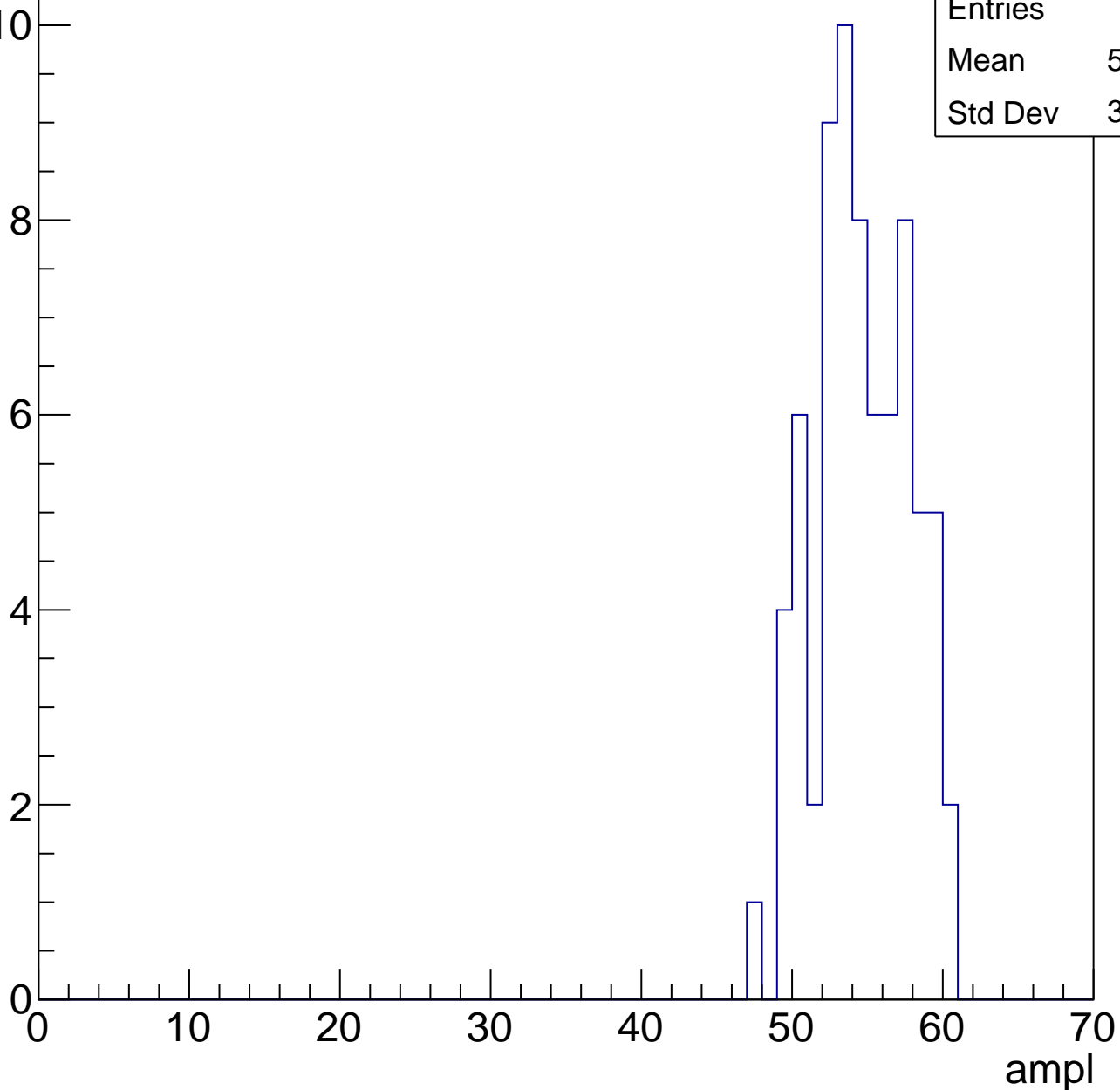


B1L103S, U7-ch23, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	54.19
Std Dev	3.085

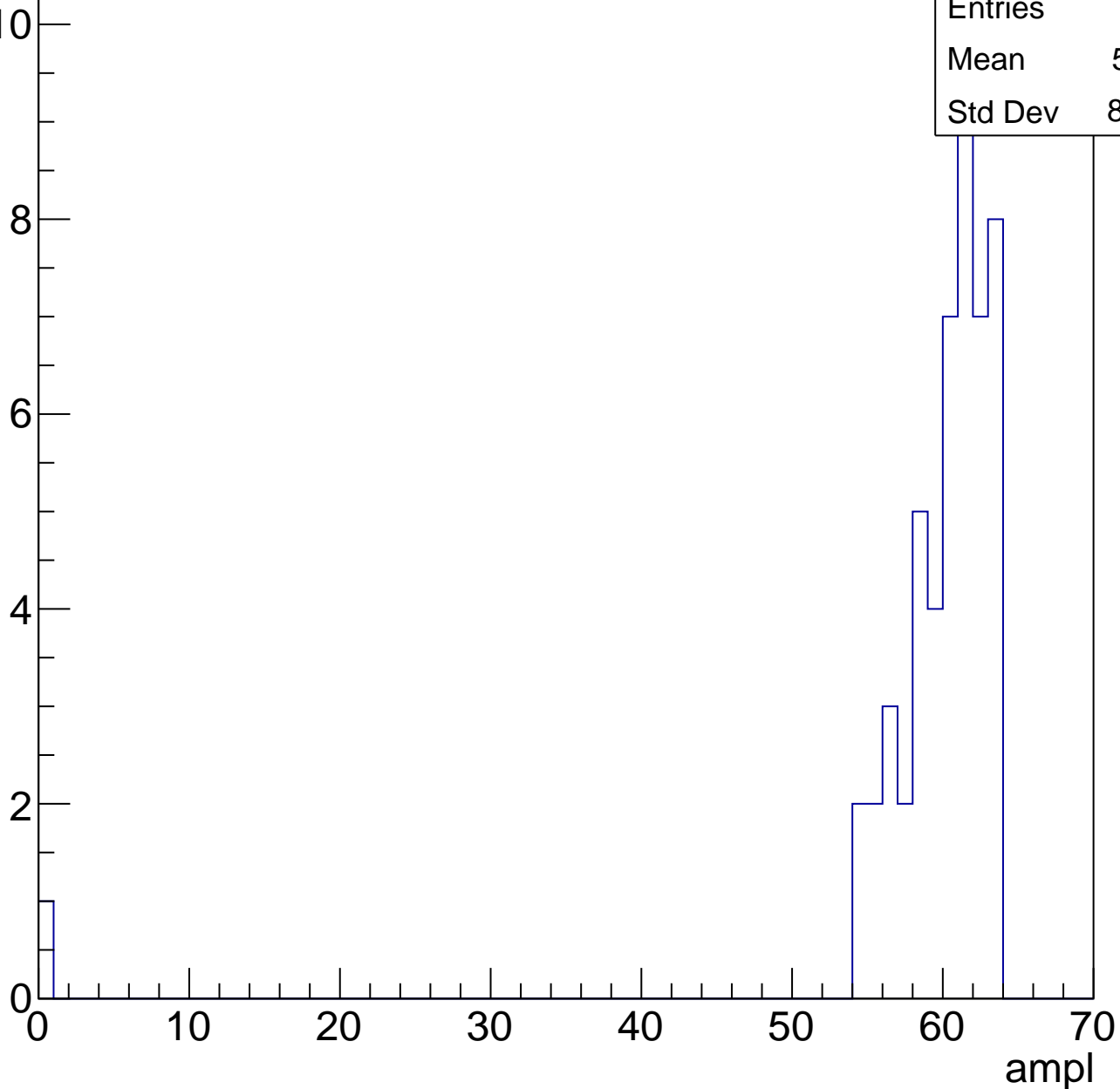


B1L103S, U7-ch23, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

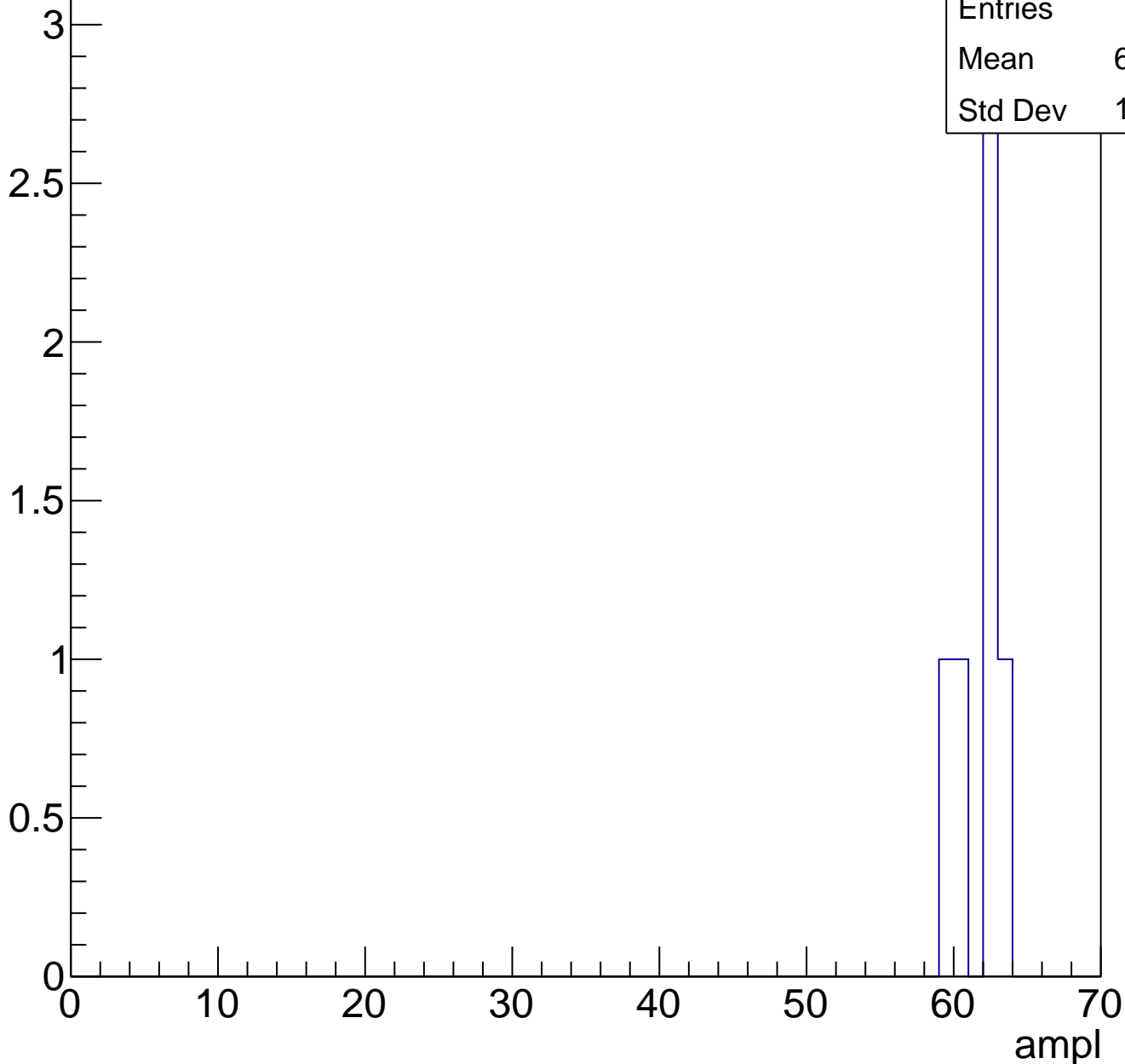
Entries	51
Mean	58.71
Std Dev	8.673



B1L103S, U7-ch23, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch23, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry



B1L103S, U7-ch24, adc0

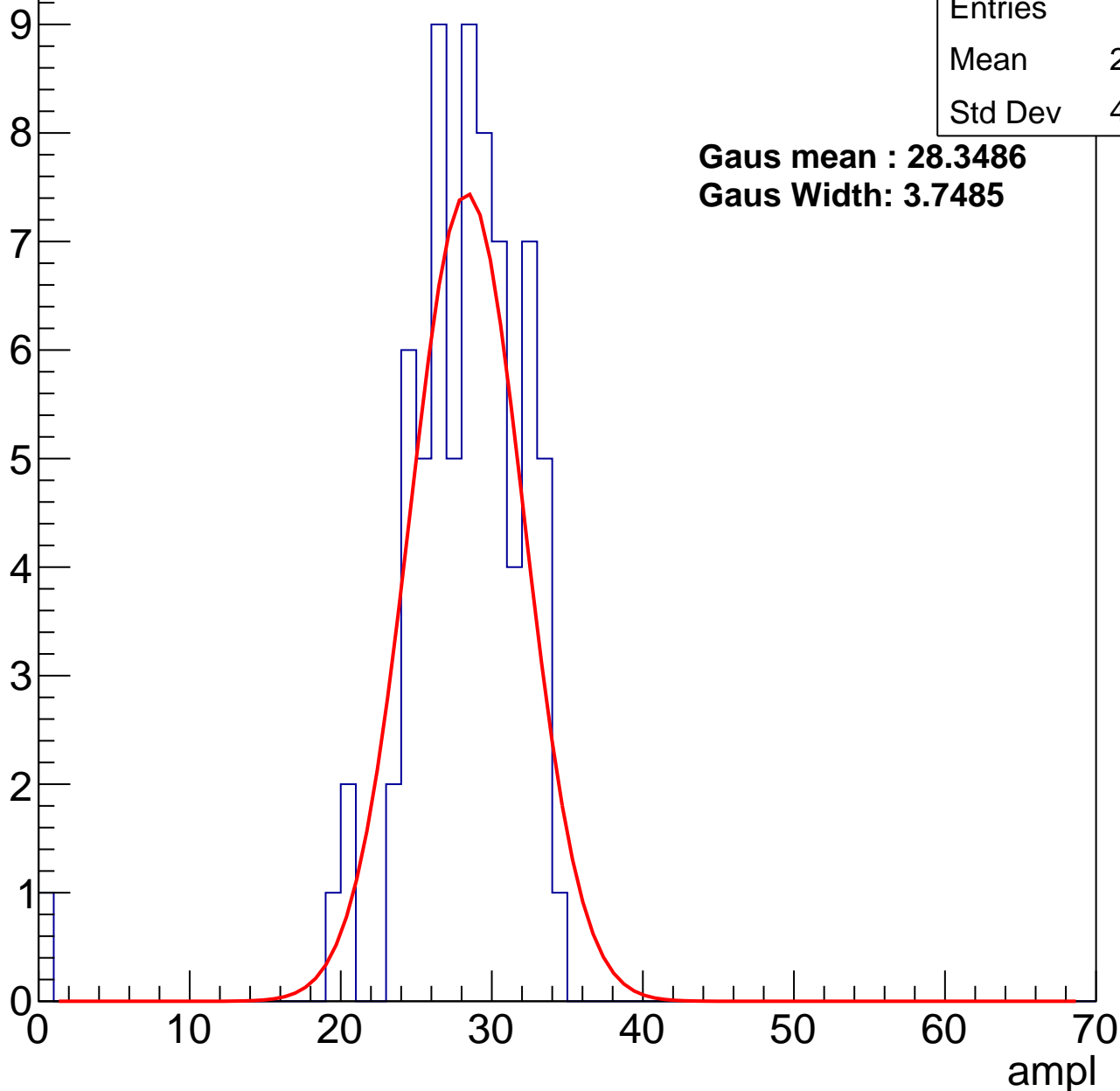
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	27.56
Std Dev	4.648

Gaus mean : 28.3486

Gaus Width: 3.7485



B1L103S, U7-ch24, adc1

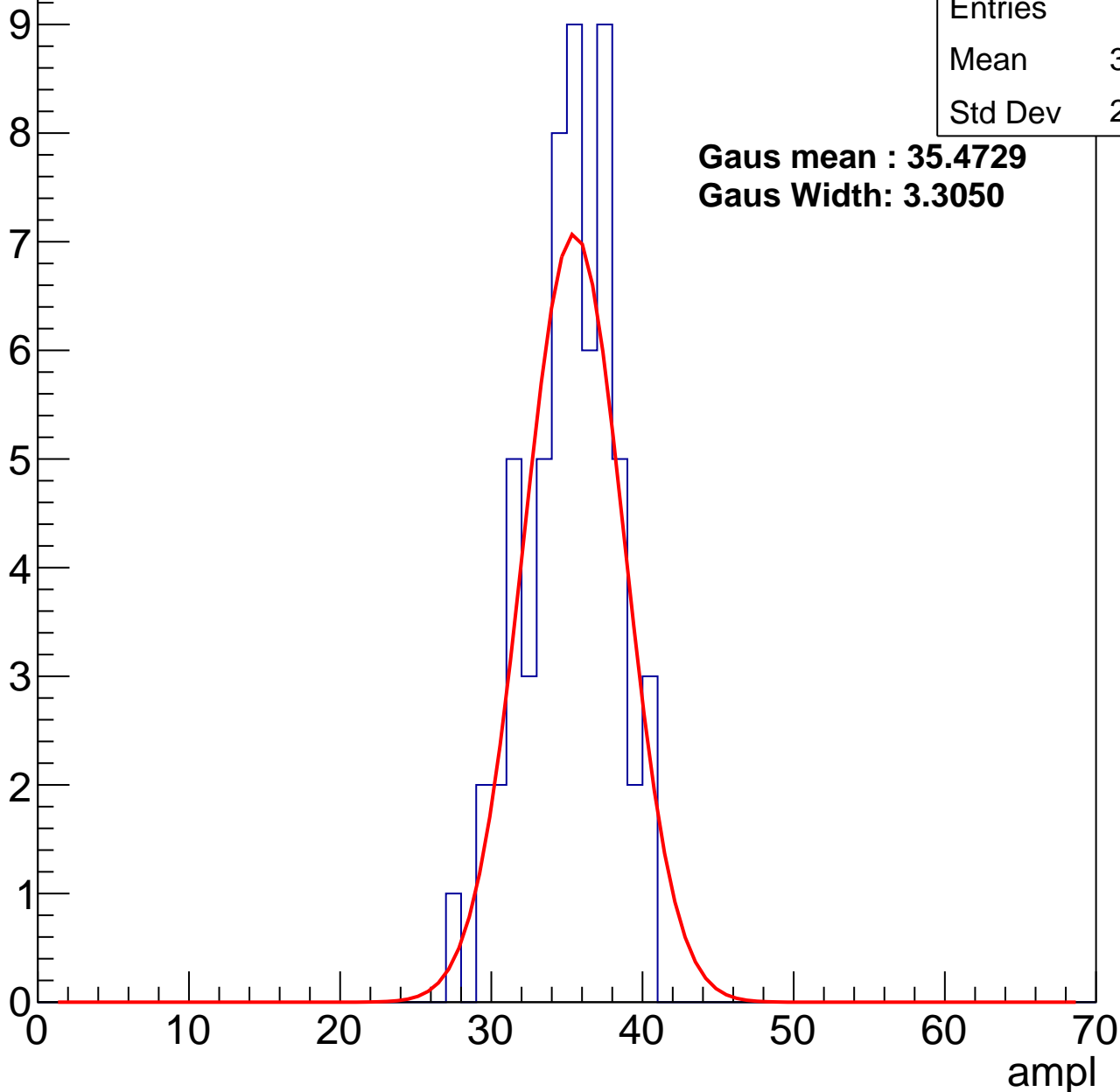
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	34.75
Std Dev	2.919

Gaus mean : 35.4729

Gaus Width: 3.3050



B1L103S, U7-ch24, adc2

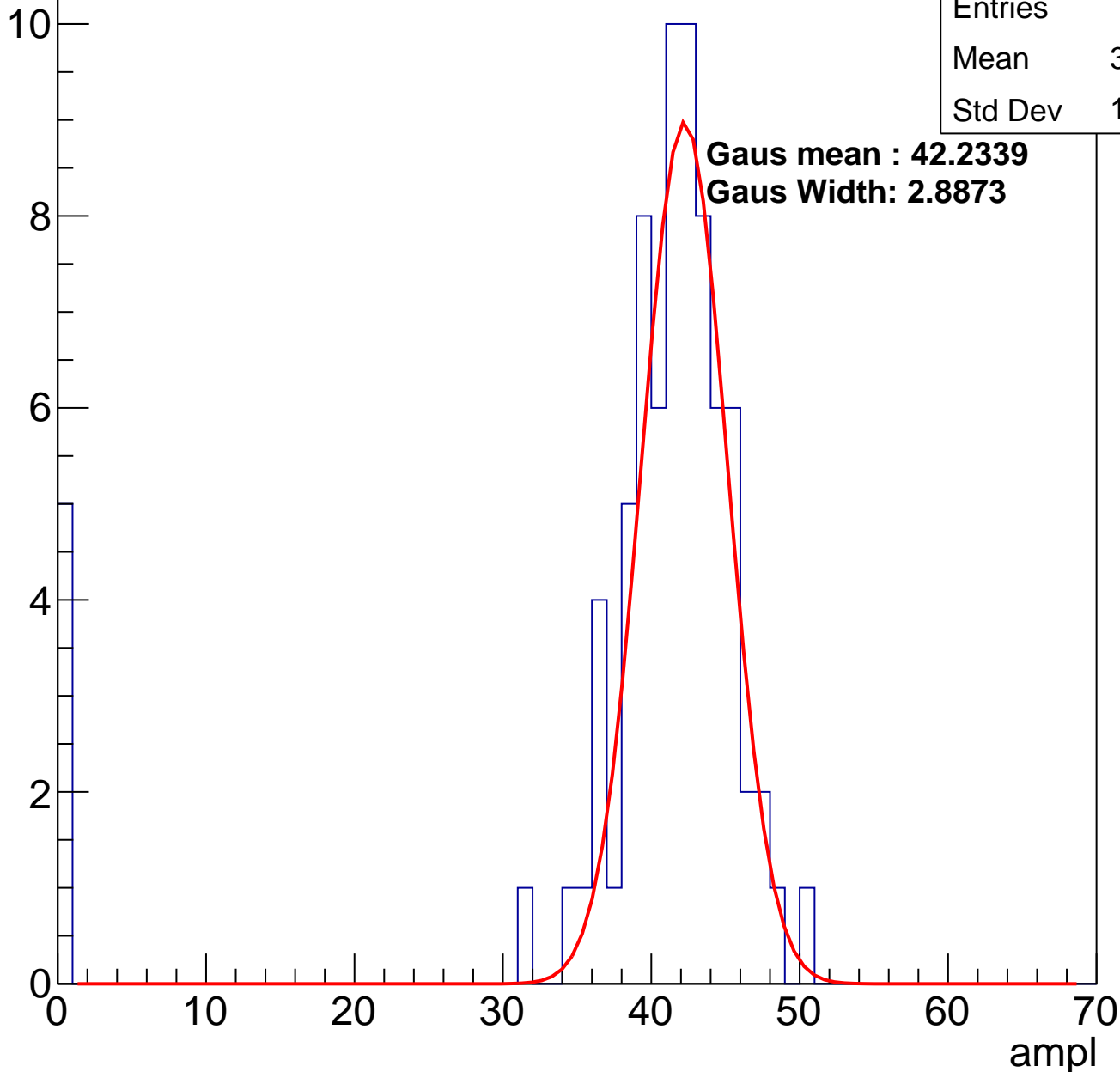
calib_packv5_041523_1651.root, FC#0, port C2

Entries	78
Mean	38.65
Std Dev	10.62

Gaus mean : 42.2339

Gaus Width: 2.8873

Entry

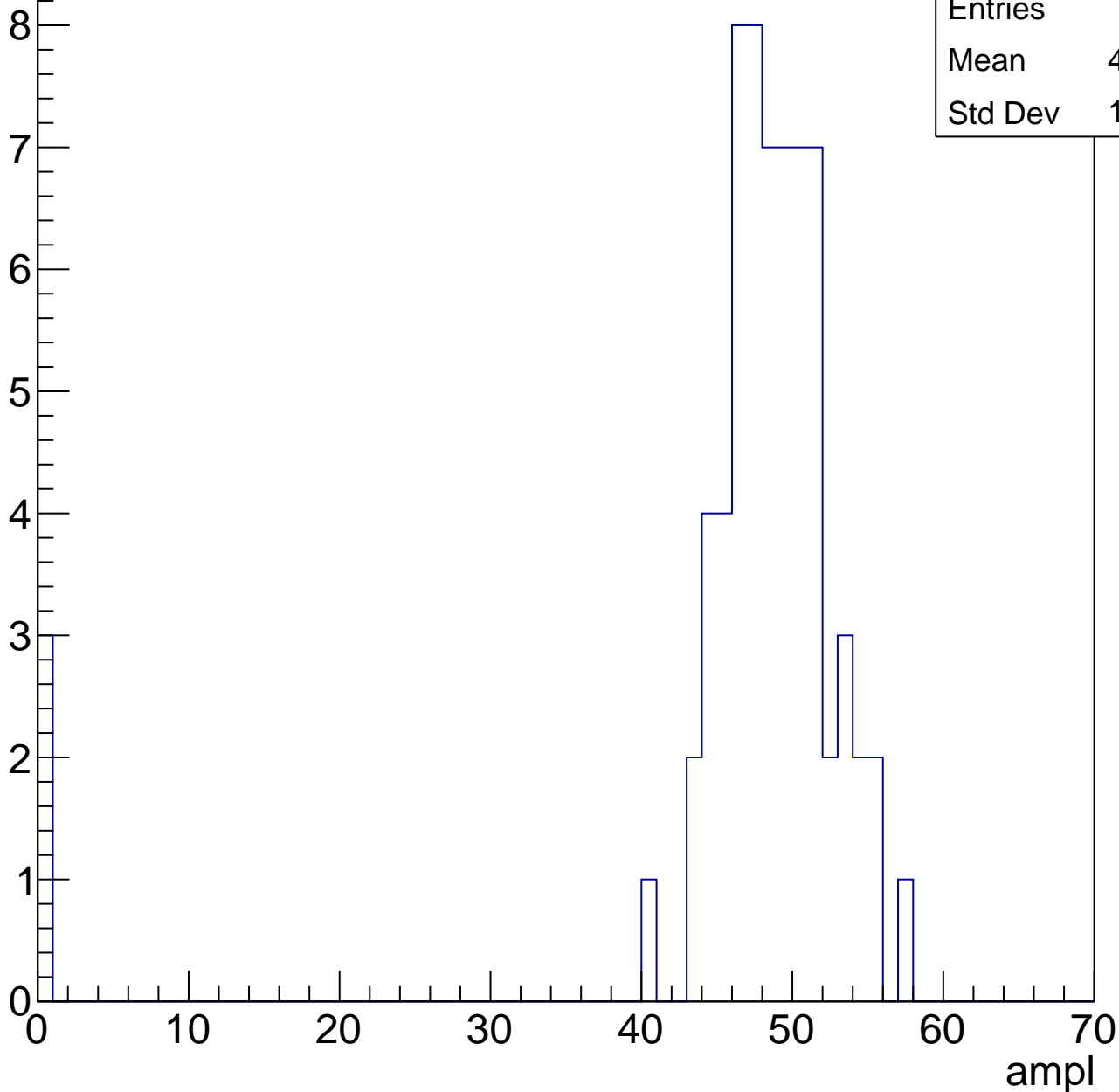


B1L103S, U7-ch24, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	46.32
Std Dev	10.45

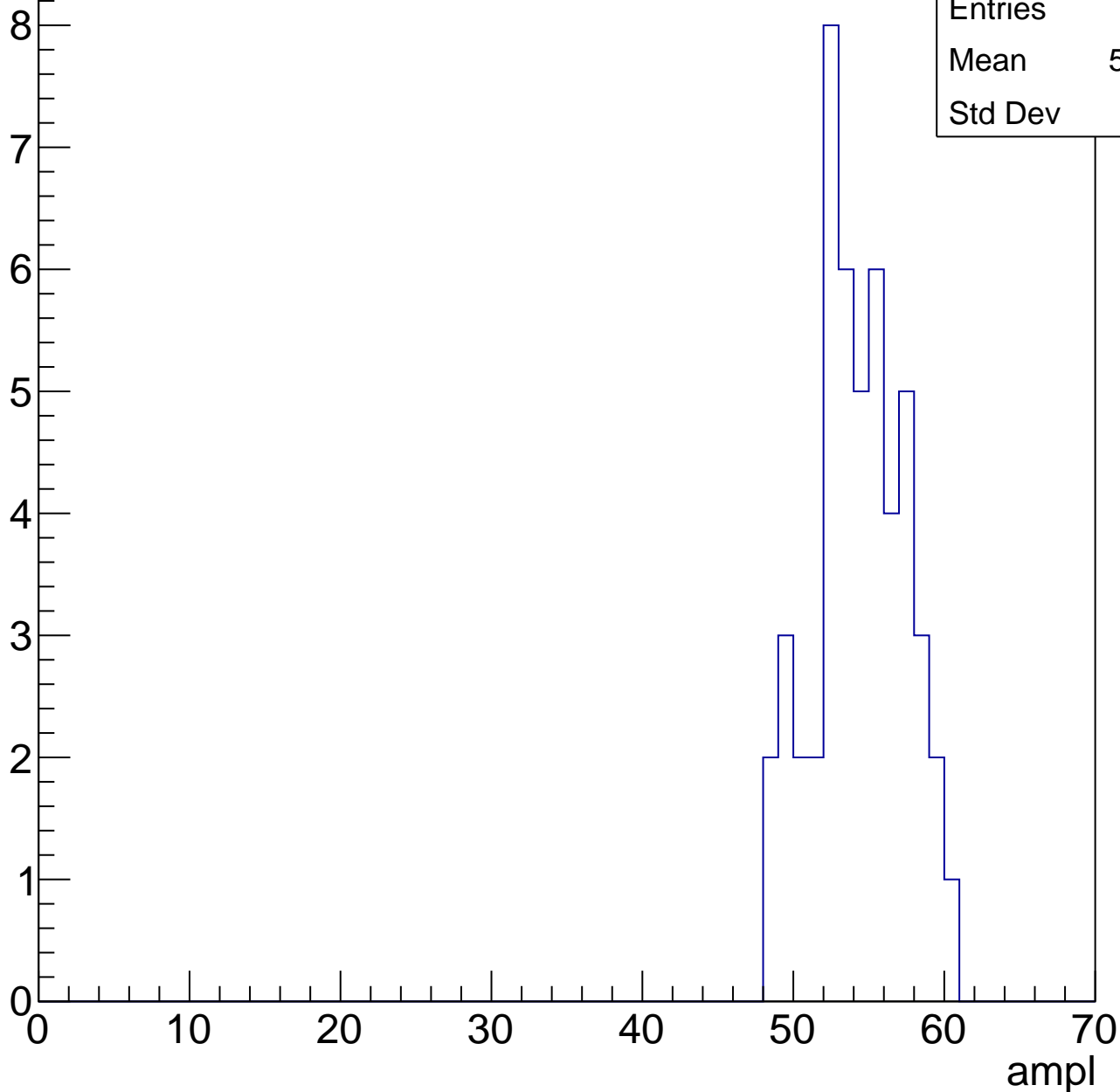


B1L103S, U7-ch24, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	53.88
Std Dev	2.98

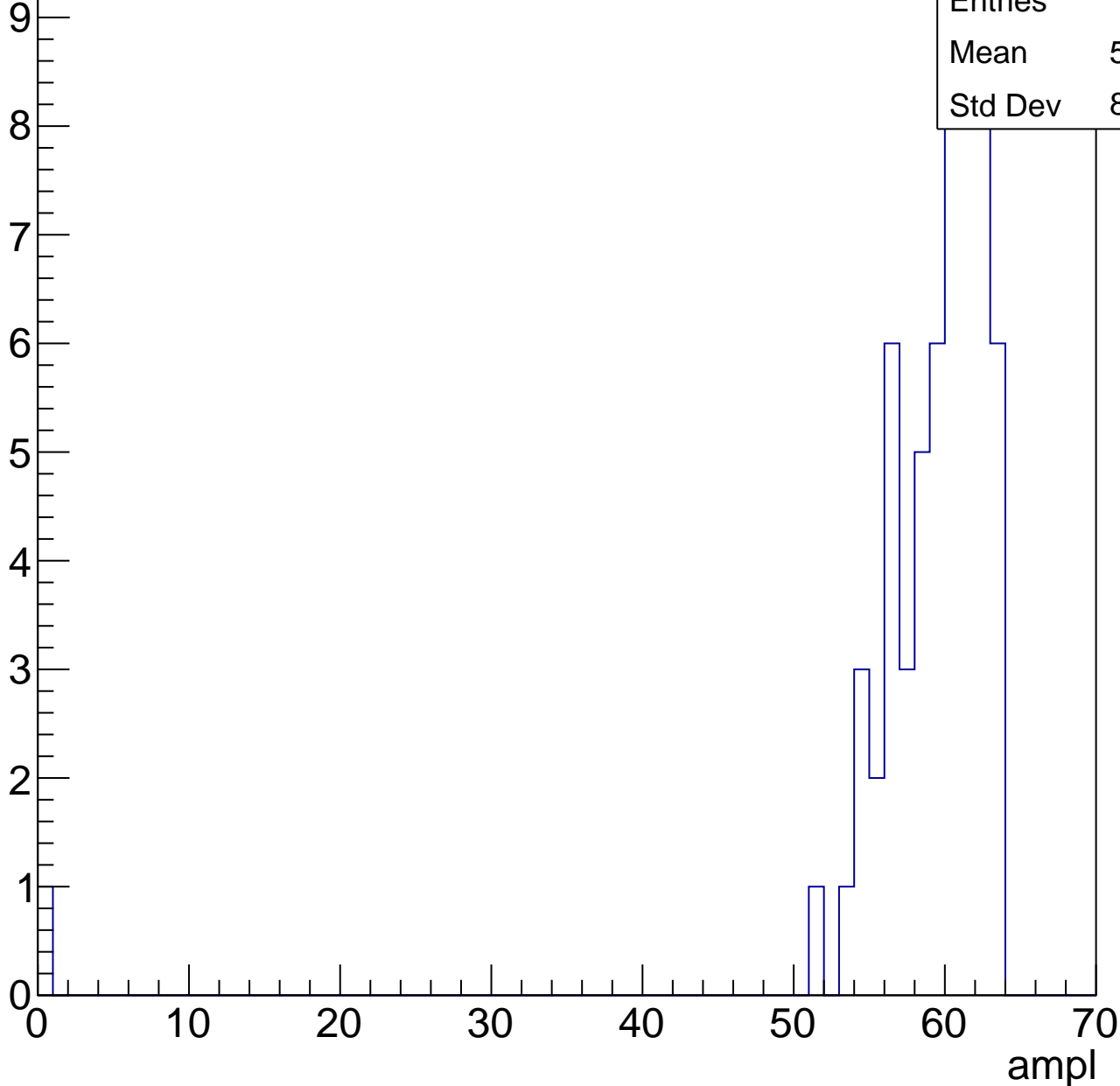


B1L103S, U7-ch24, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

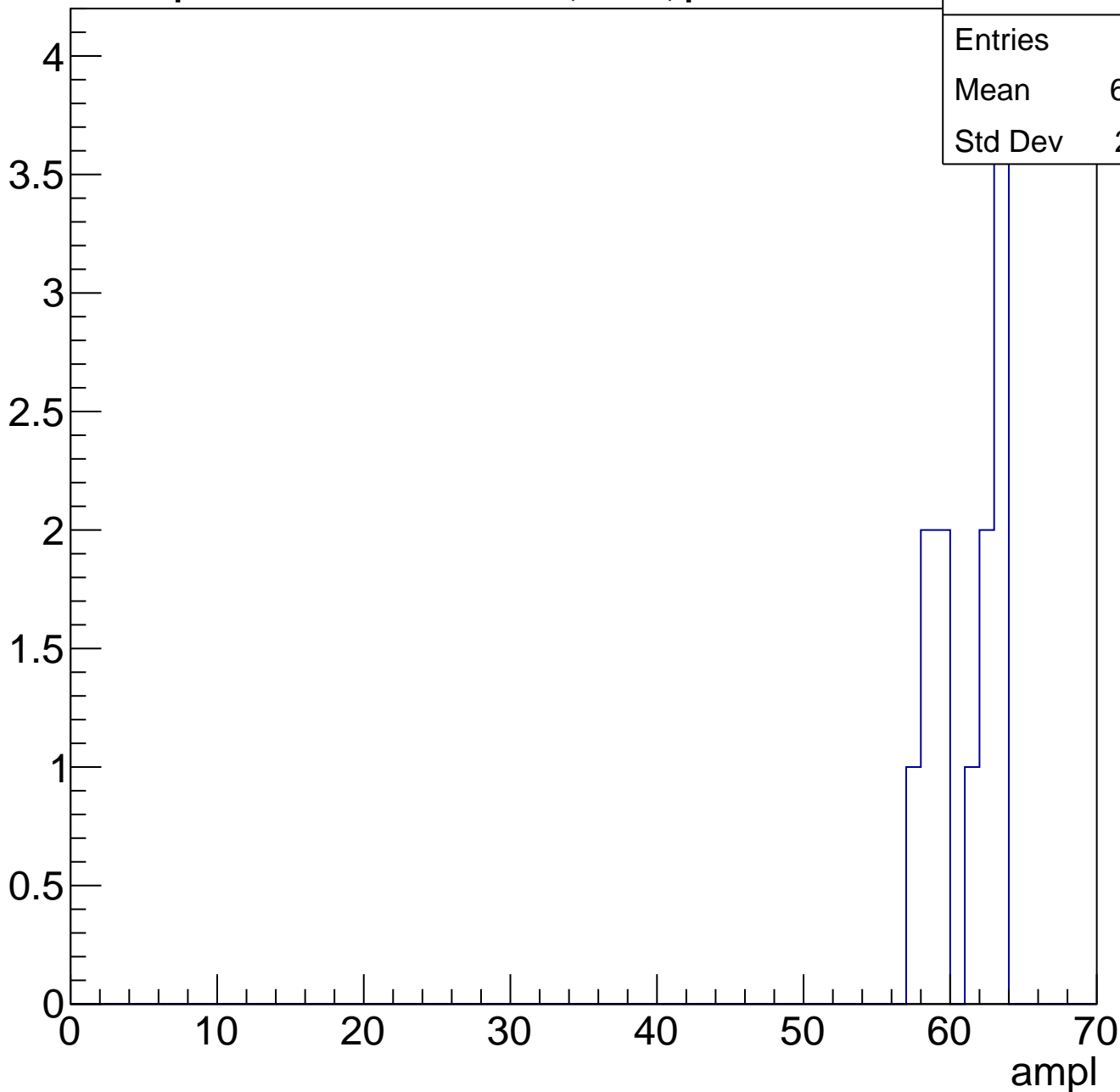
Entries	60
Mean	58.17
Std Dev	8.094



B1L103S, U7-ch24, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	12
Mean	60.67
Std Dev	2.211

B1L103S, U7-ch24, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch25, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	77
Mean	22.97
Std Dev	9.939

Gaus mean : 28.1137

Gaus Width: 4.3423

Entry

10

8

6

4

2

0

0

10

20

30

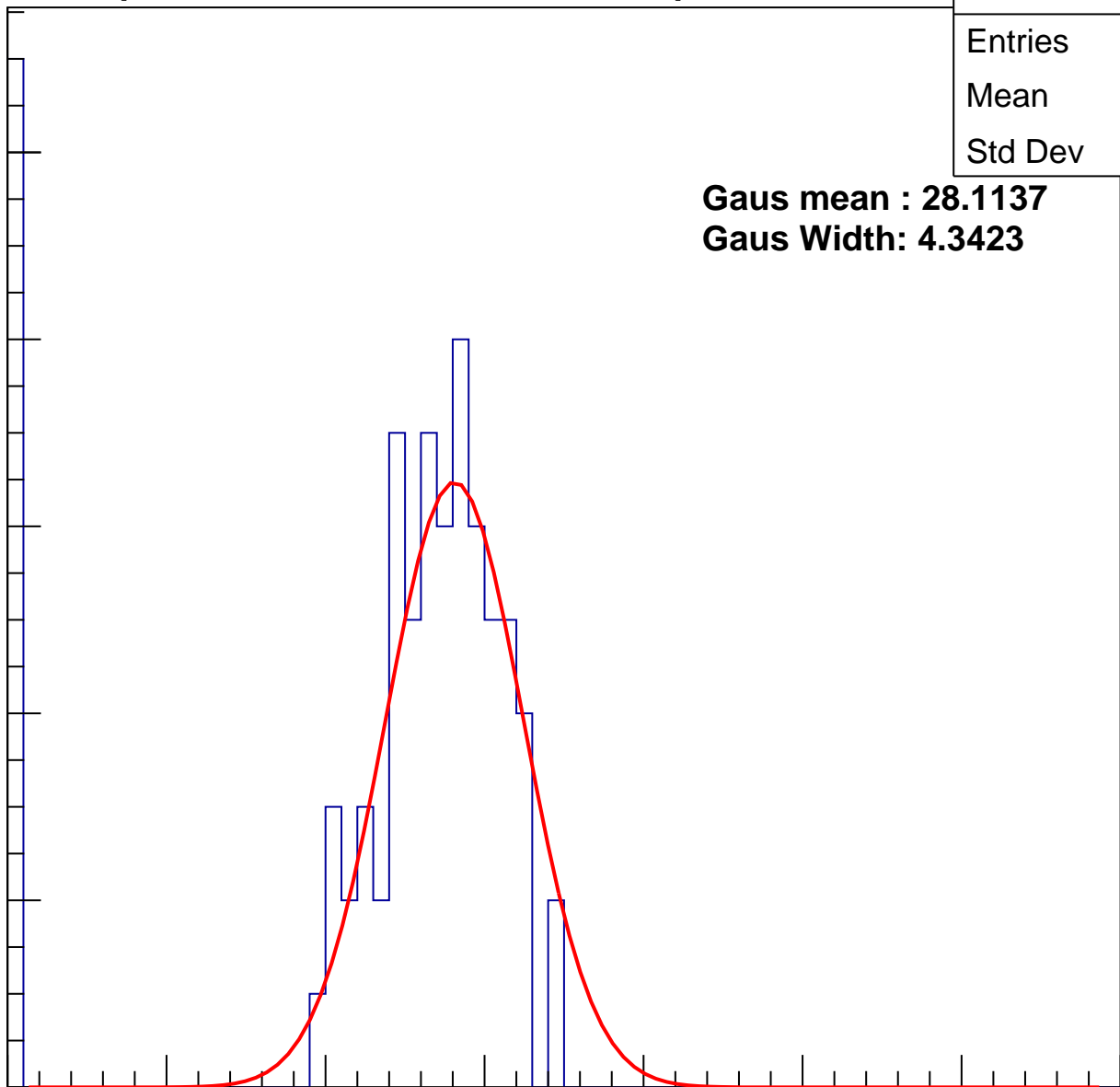
40

50

60

70

ampl



B1L103S, U7-ch25, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	32.36
Std Dev	8.188

Gaus mean : 34.5734

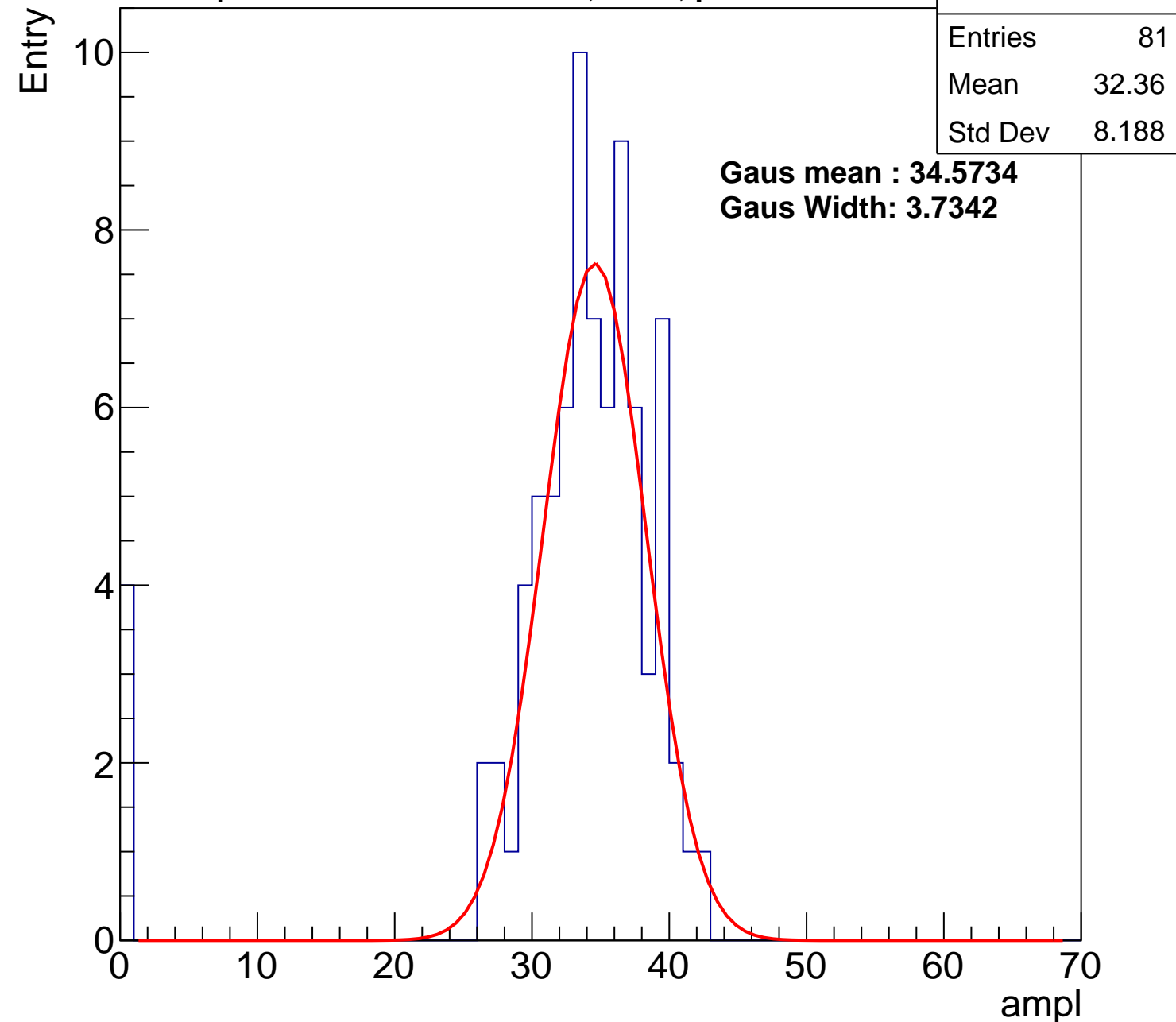
Gaus Width: 3.7342

Entry

10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U7-ch25, adc2

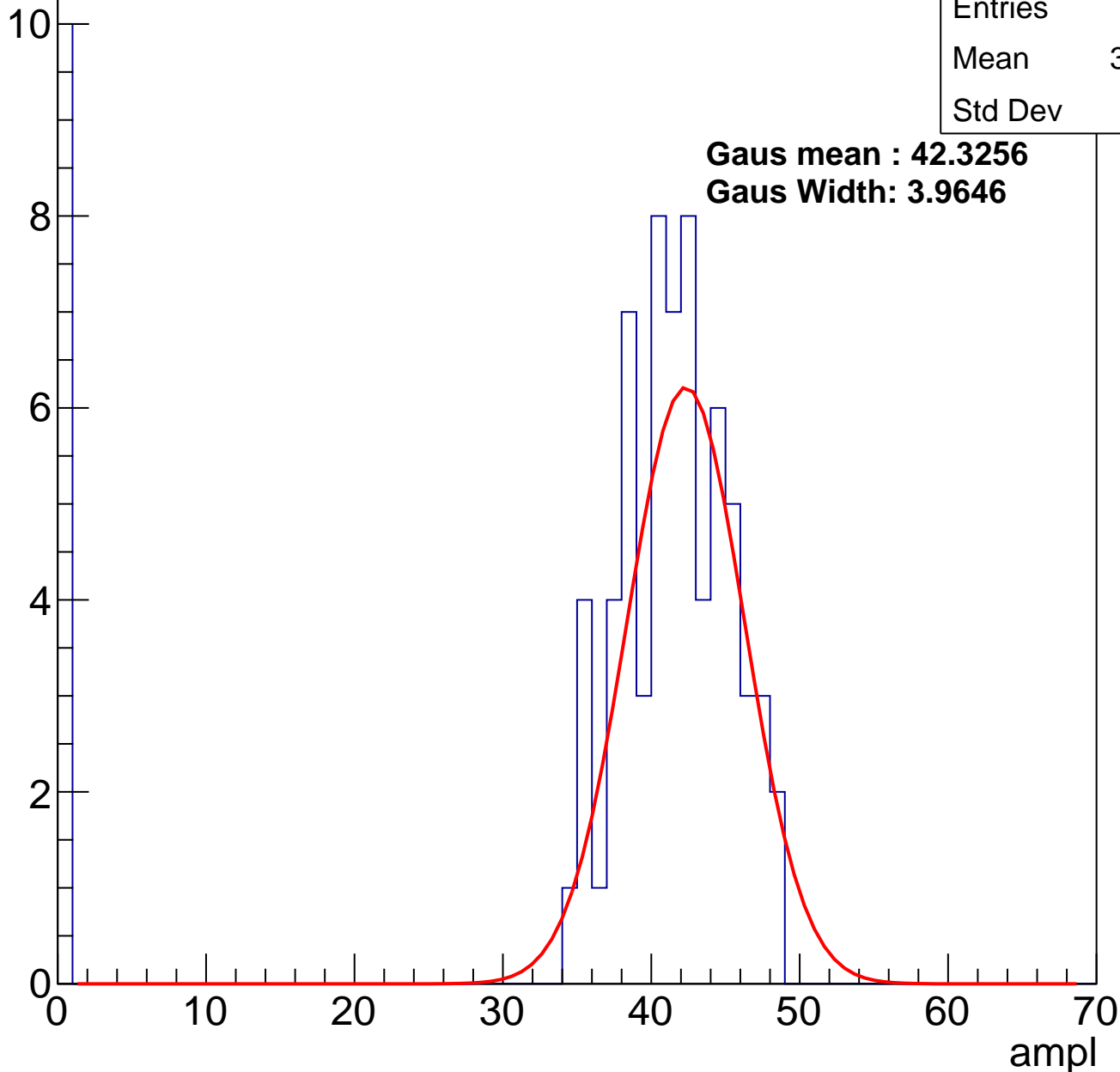
calib_packv5_041523_1651.root, FC#0, port C2

Entries	76
Mean	35.79
Std Dev	14.3

Gaus mean : 42.3256

Gaus Width: 3.9646

Entry

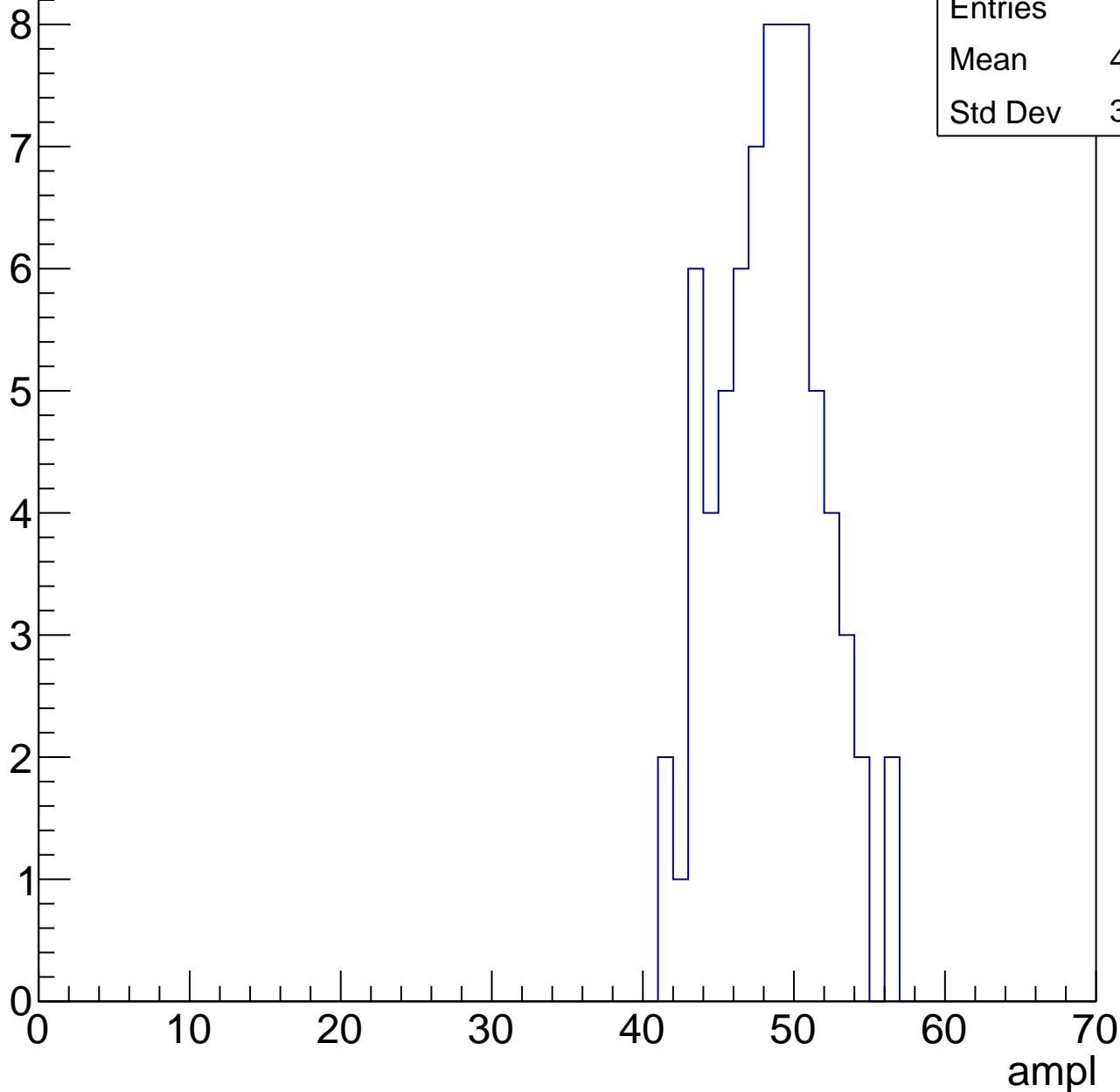


B1L103S, U7-ch25, adc3

calib_packv5_041523_1651.root, FC#0, port C2

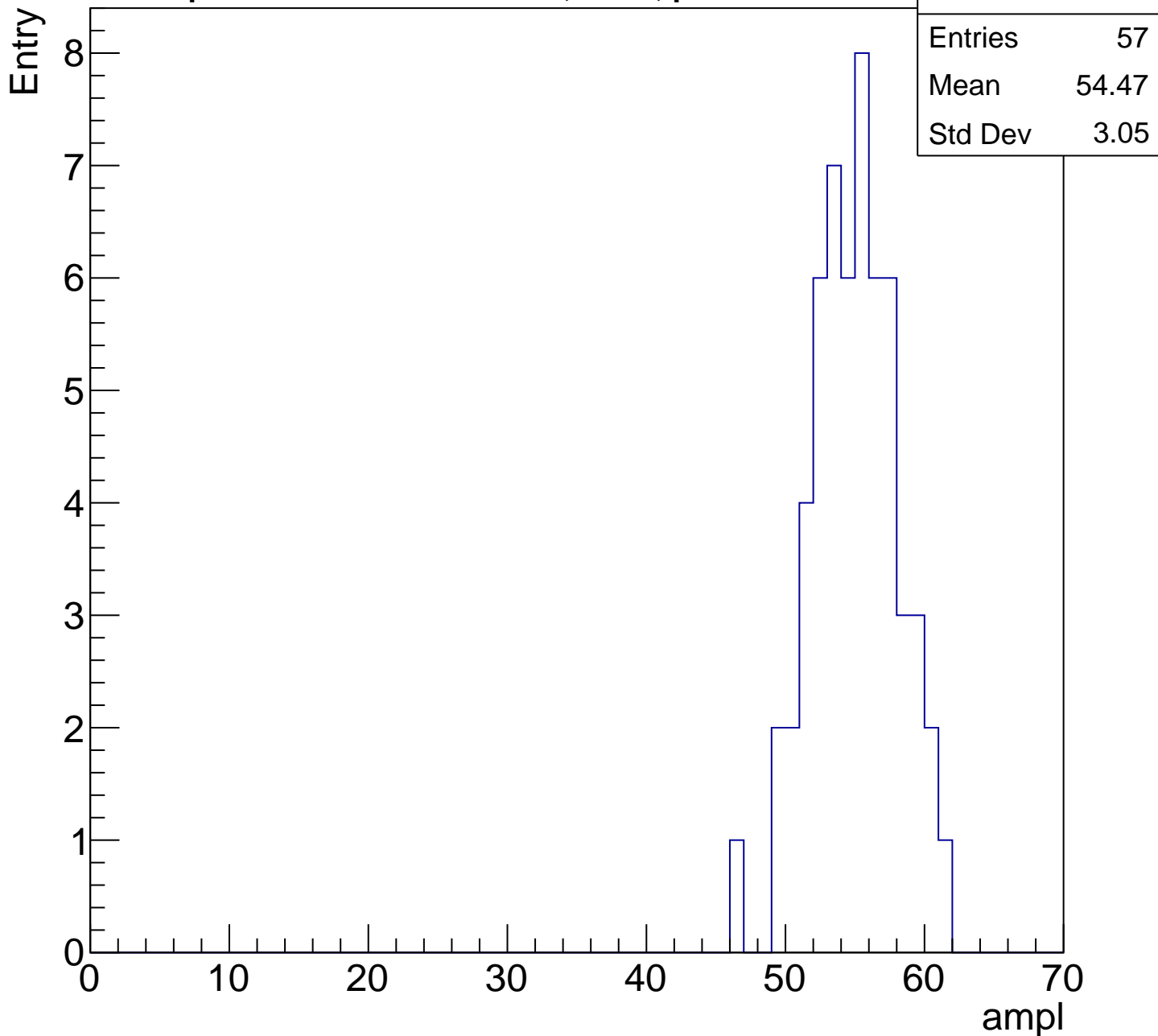
Entry

Entries	71
Mean	47.97
Std Dev	3.456



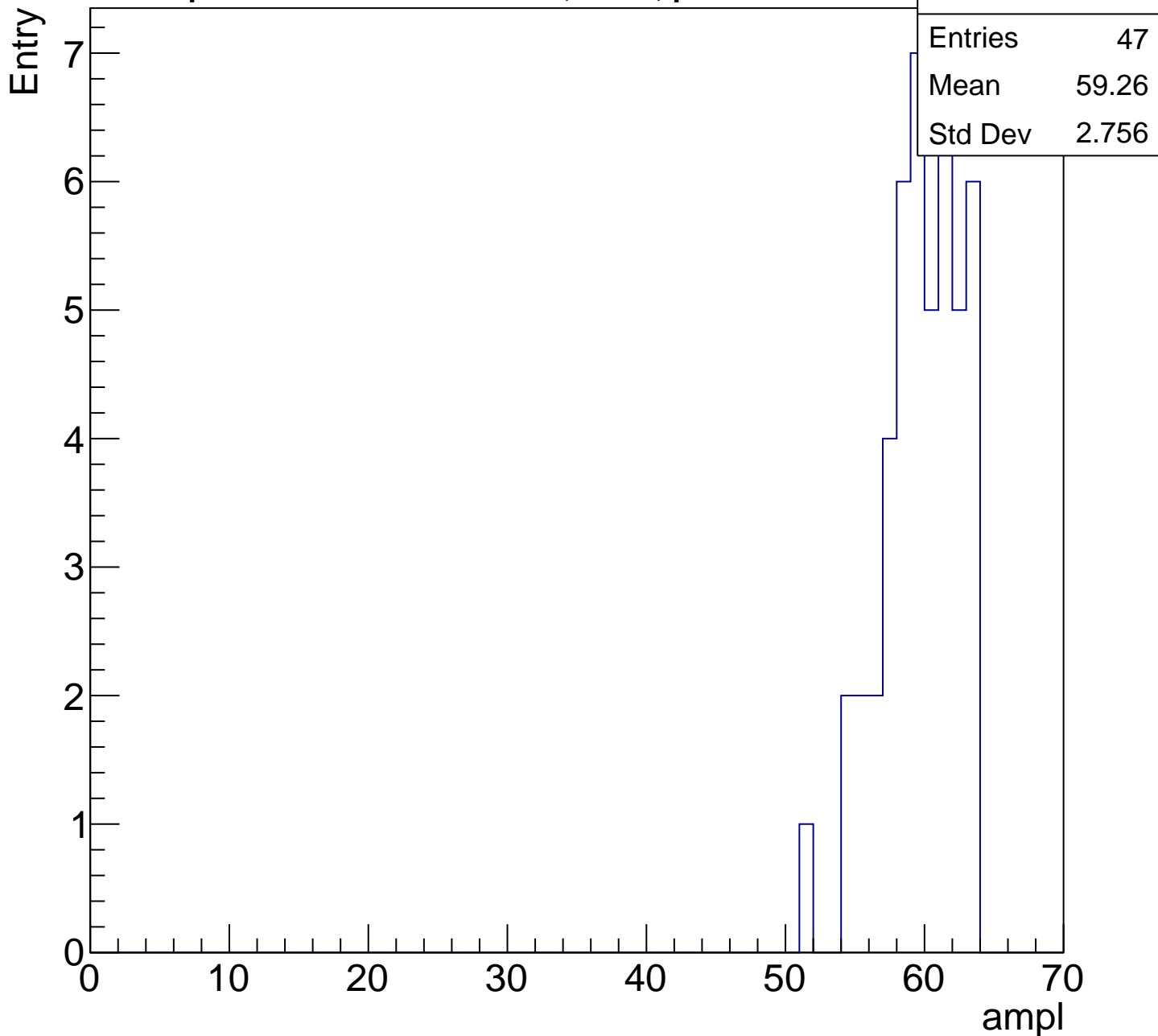
B1L103S, U7-ch25, adc4

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U7-ch25, adc5

calib_packv5_041523_1651.root, FC#0, port C2

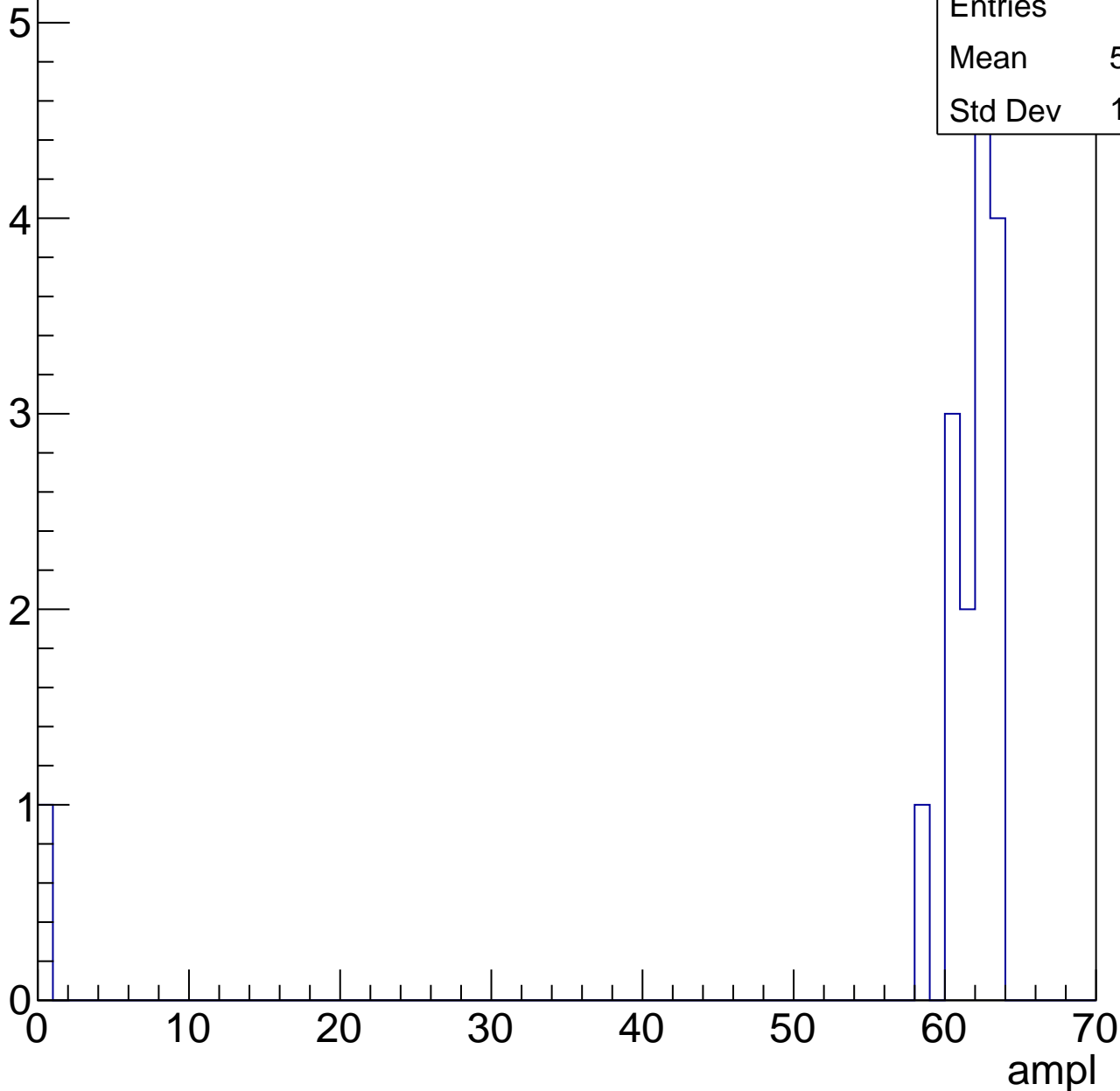


B1L103S, U7-ch25, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	16
Mean	57.62
Std Dev	14.94



B1L103S, U7-ch25, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U7-ch26, adc0

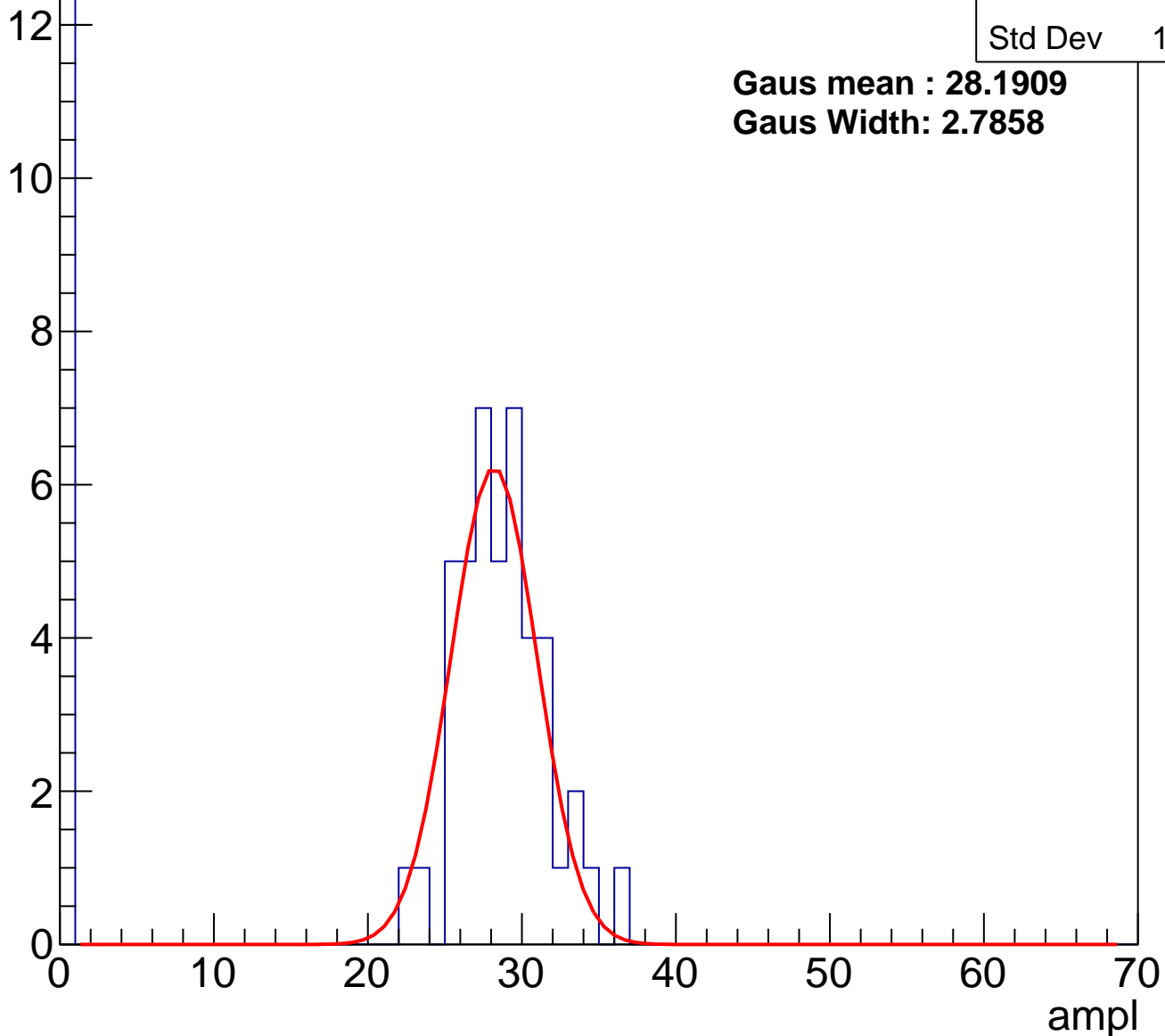
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	21.82
Std Dev	12.12

Gaus mean : 28.1909

Gaus Width: 2.7858



B1L103S, U7-ch26, adc1

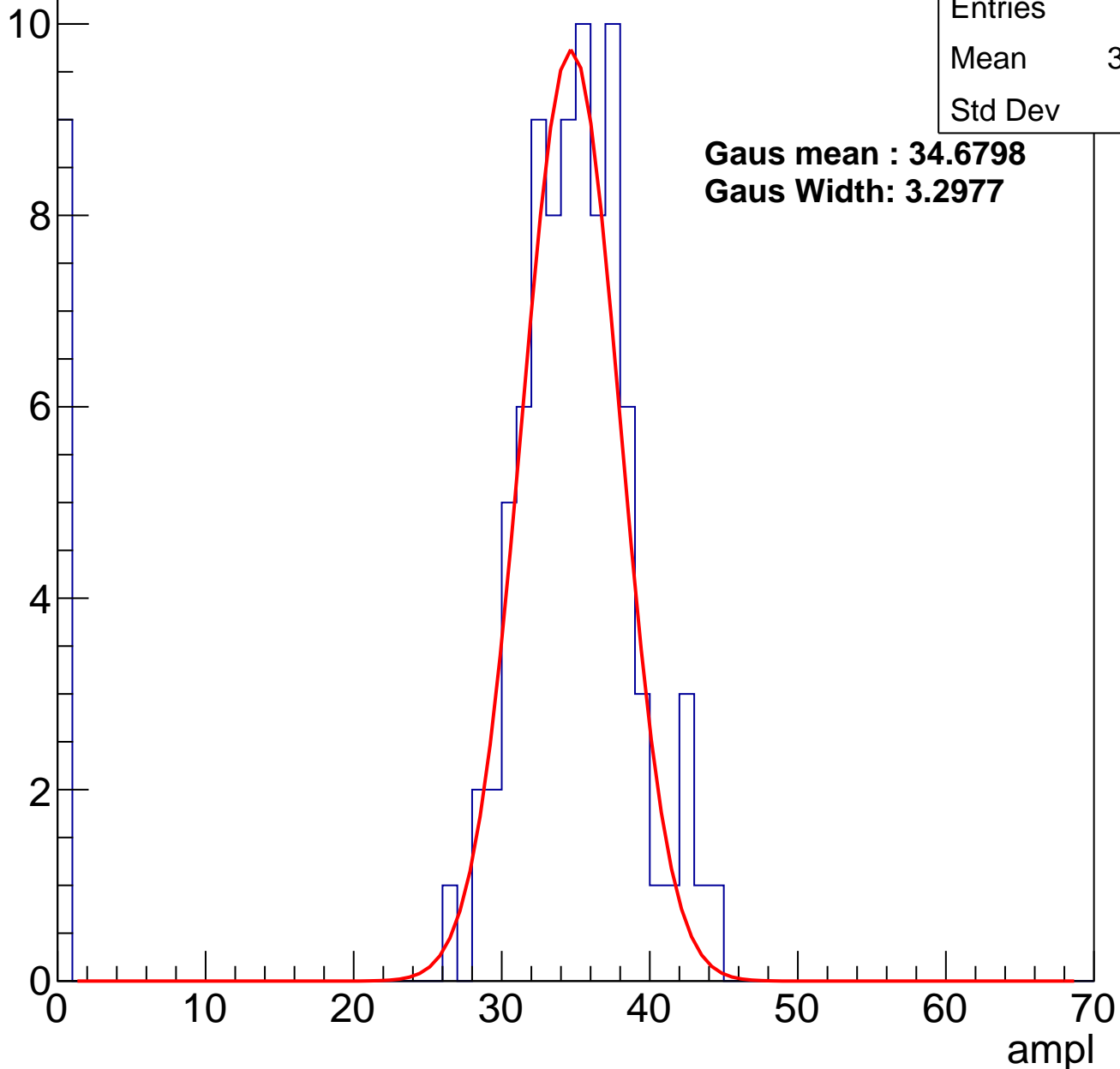
calib_packv5_041523_1651.root, FC#0, port C2

Entries	95
Mean	31.38
Std Dev	10.7

Gaus mean : 34.6798

Gaus Width: 3.2977

Entry



B1L103S, U7-ch26, adc2

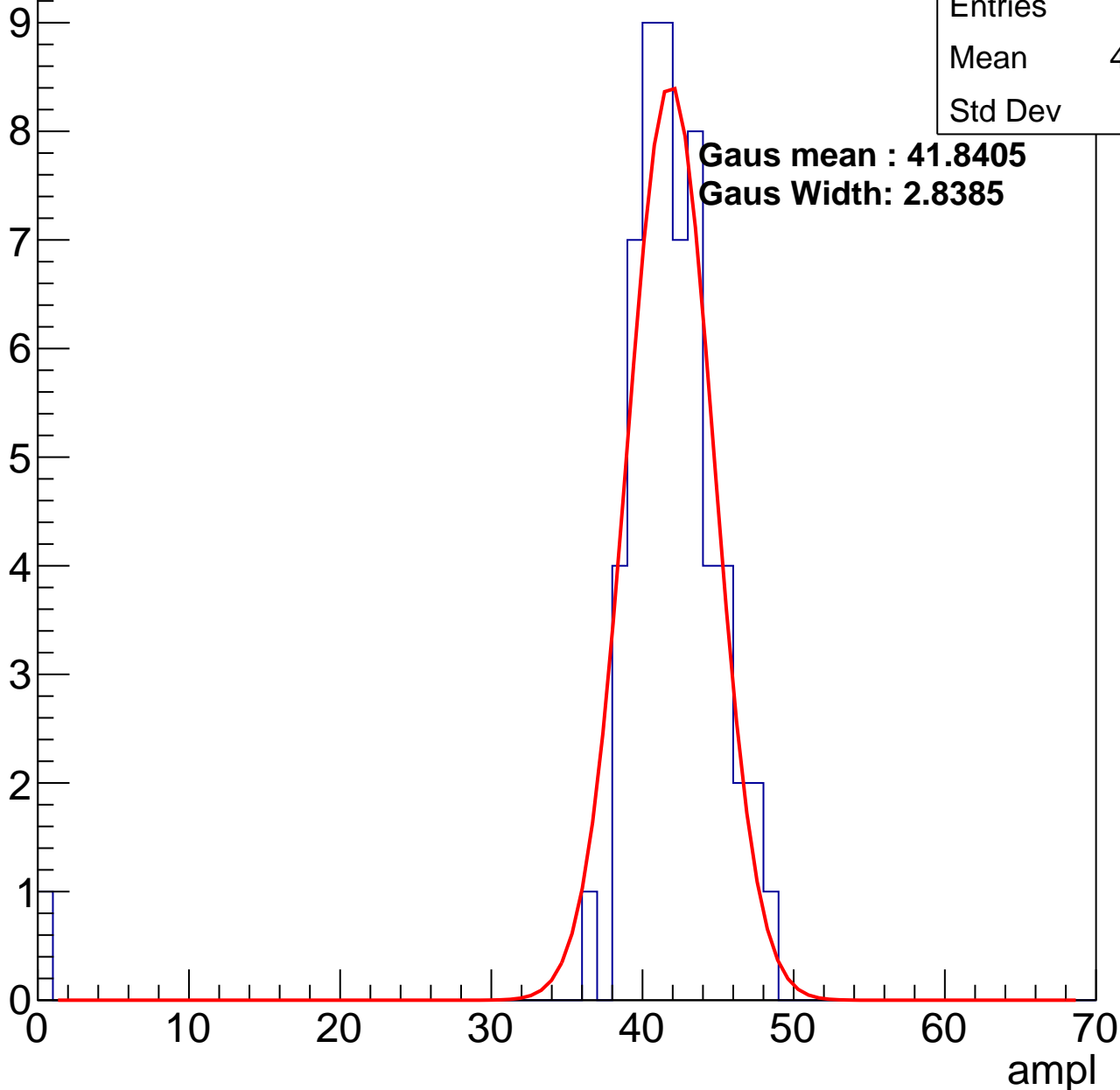
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	40.98
Std Dev	5.95

Gaus mean : 41.8405

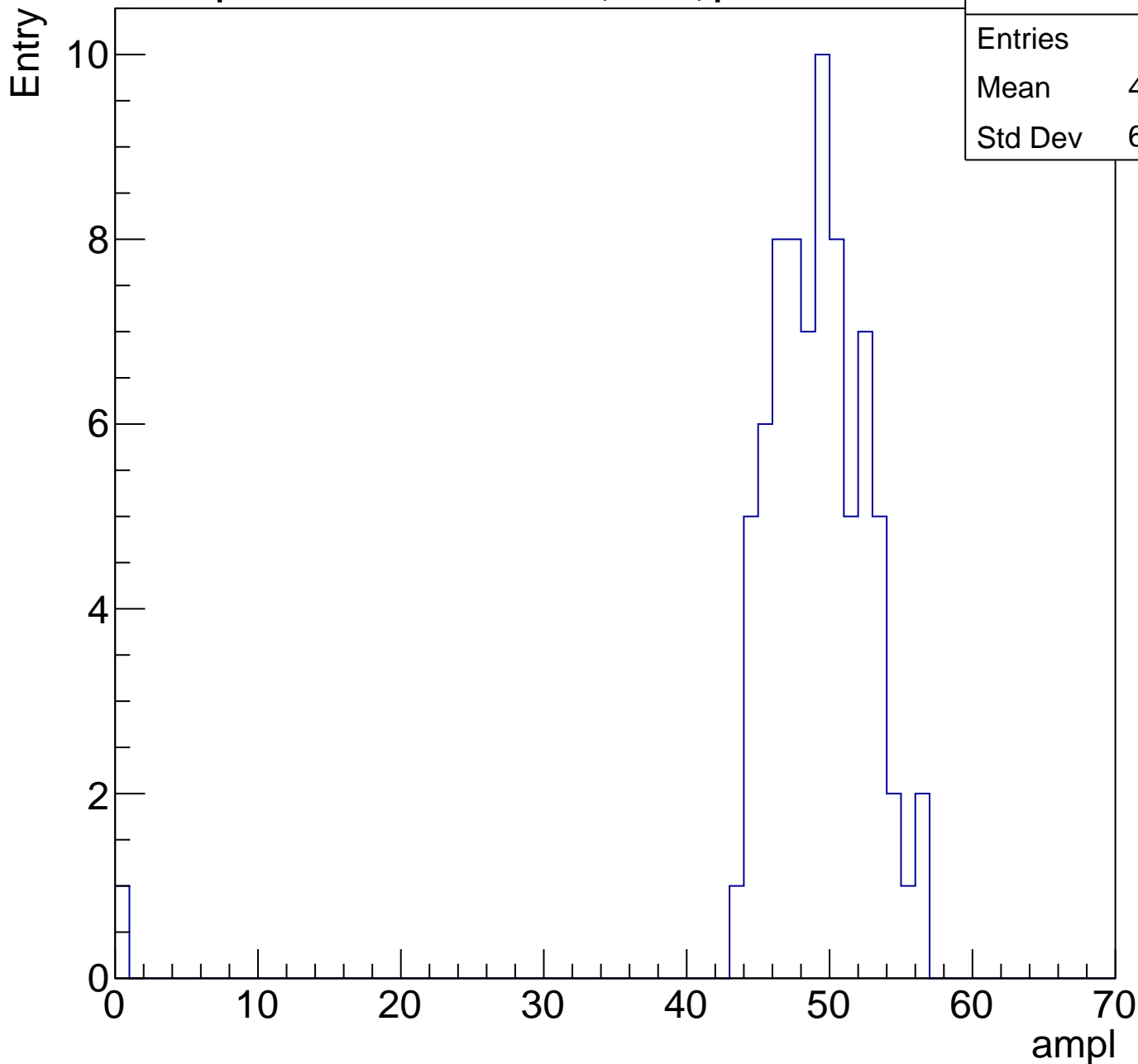
Gaus Width: 2.8385



B1L103S, U7-ch26, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	76
Mean	48.18
Std Dev	6.359

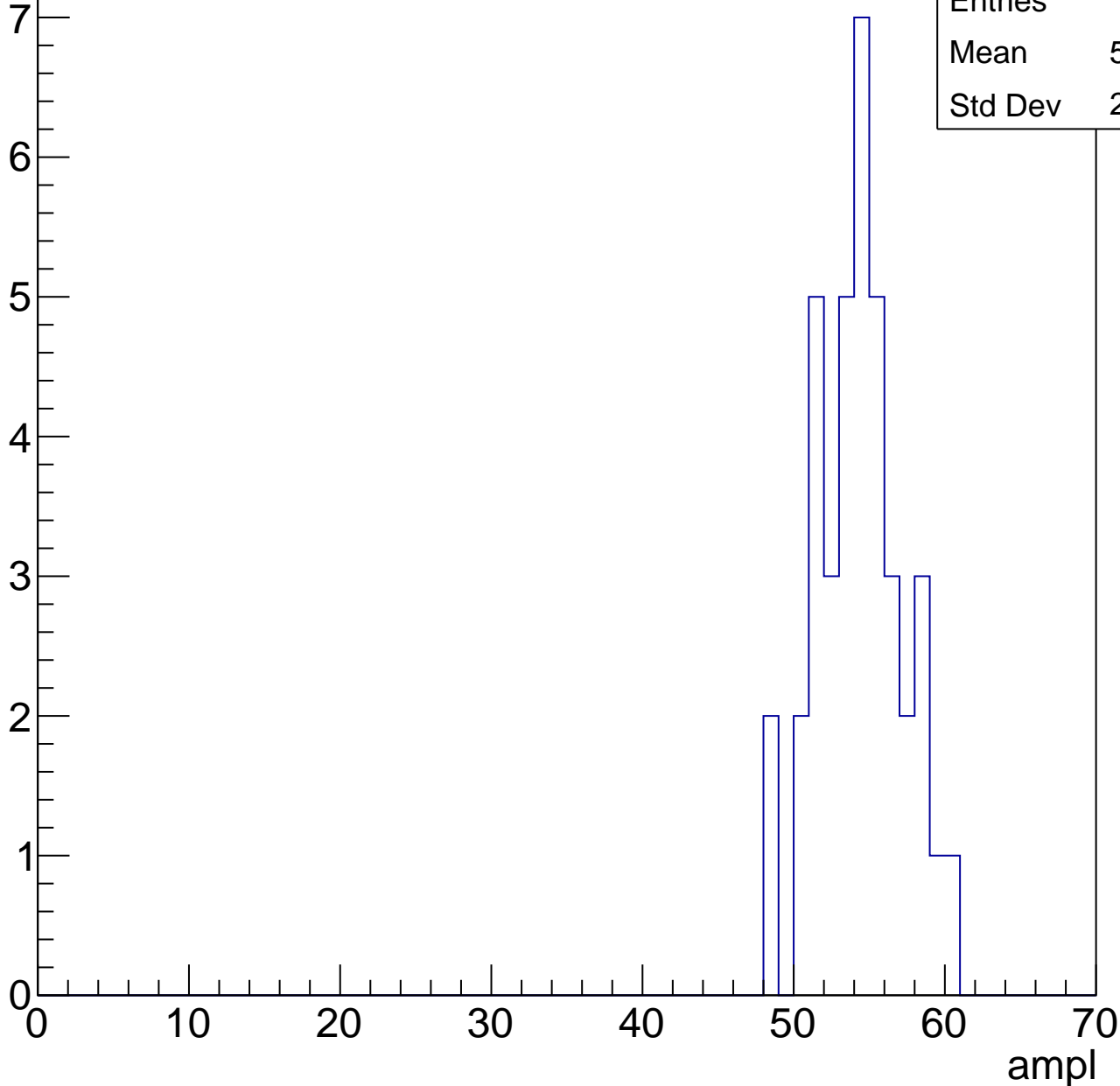


B1L103S, U7-ch26, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	53.85
Std Dev	2.815



B1L103S, U7-ch26, adc5

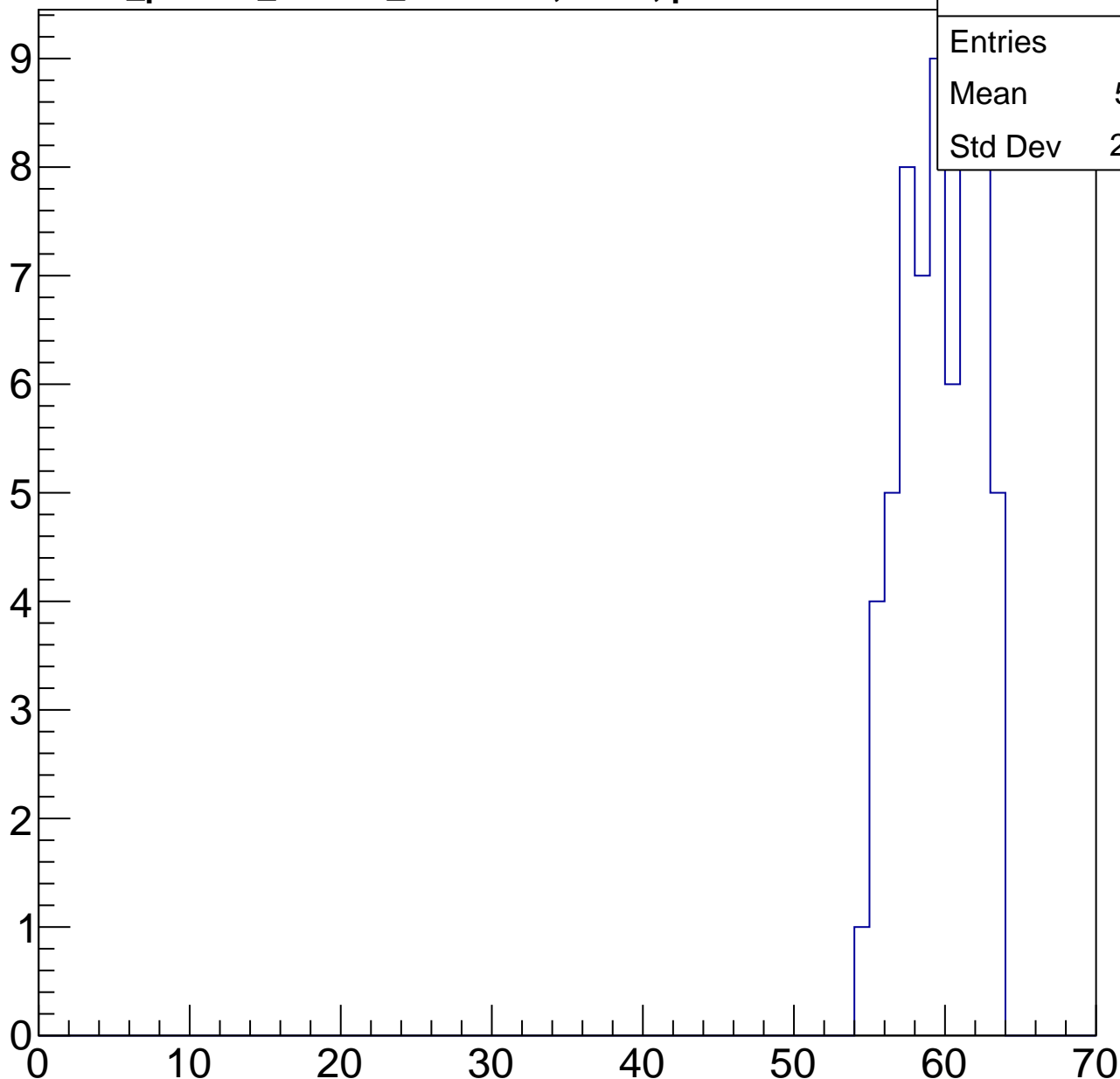
calib_packv5_041523_1651.root, FC#0, port C2

Entry

9
8
7
6
5
4
3
2
1
0

Entries	61
Mean	59.11
Std Dev	2.437

ampl



B1L103S, U7-ch26, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

8

Mean

61.62

Std Dev

1.317

B1L103S, U7-ch26, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

20
18
16
14
12
10
8
6
4
2
0

Entries	24
Mean	10.33
Std Dev	23.11

0 10 20 30 40 50 60 70

ampl



B1L103S, U7-ch27, adc0

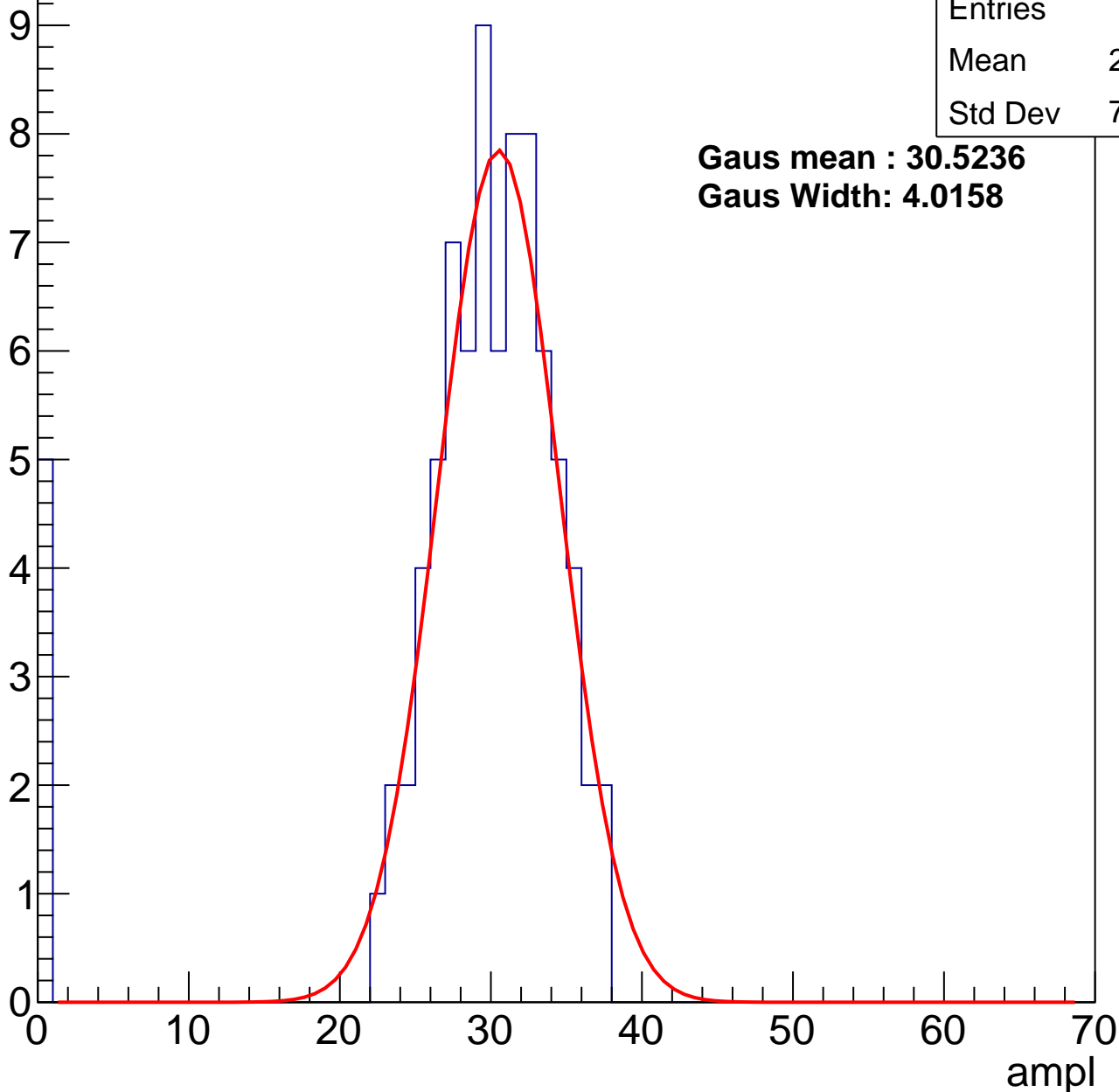
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	82
Mean	28.07
Std Dev	7.925

Gaus mean : 30.5236

Gaus Width: 4.0158



B1L103S, U7-ch27, adc1

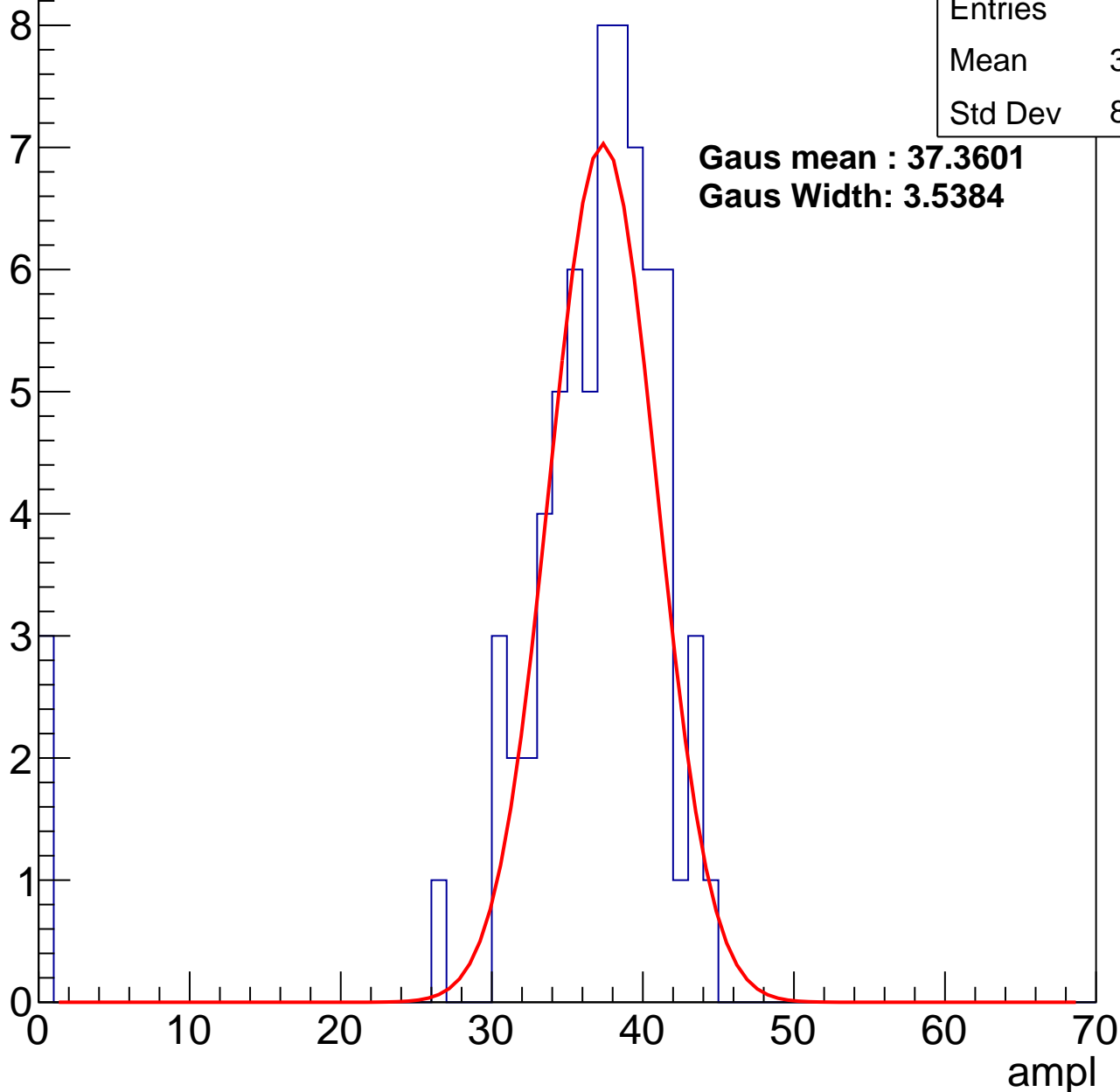
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	35.32
Std Dev	8.225

Gaus mean : 37.3601

Gaus Width: 3.5384



B1L103S, U7-ch27, adc2

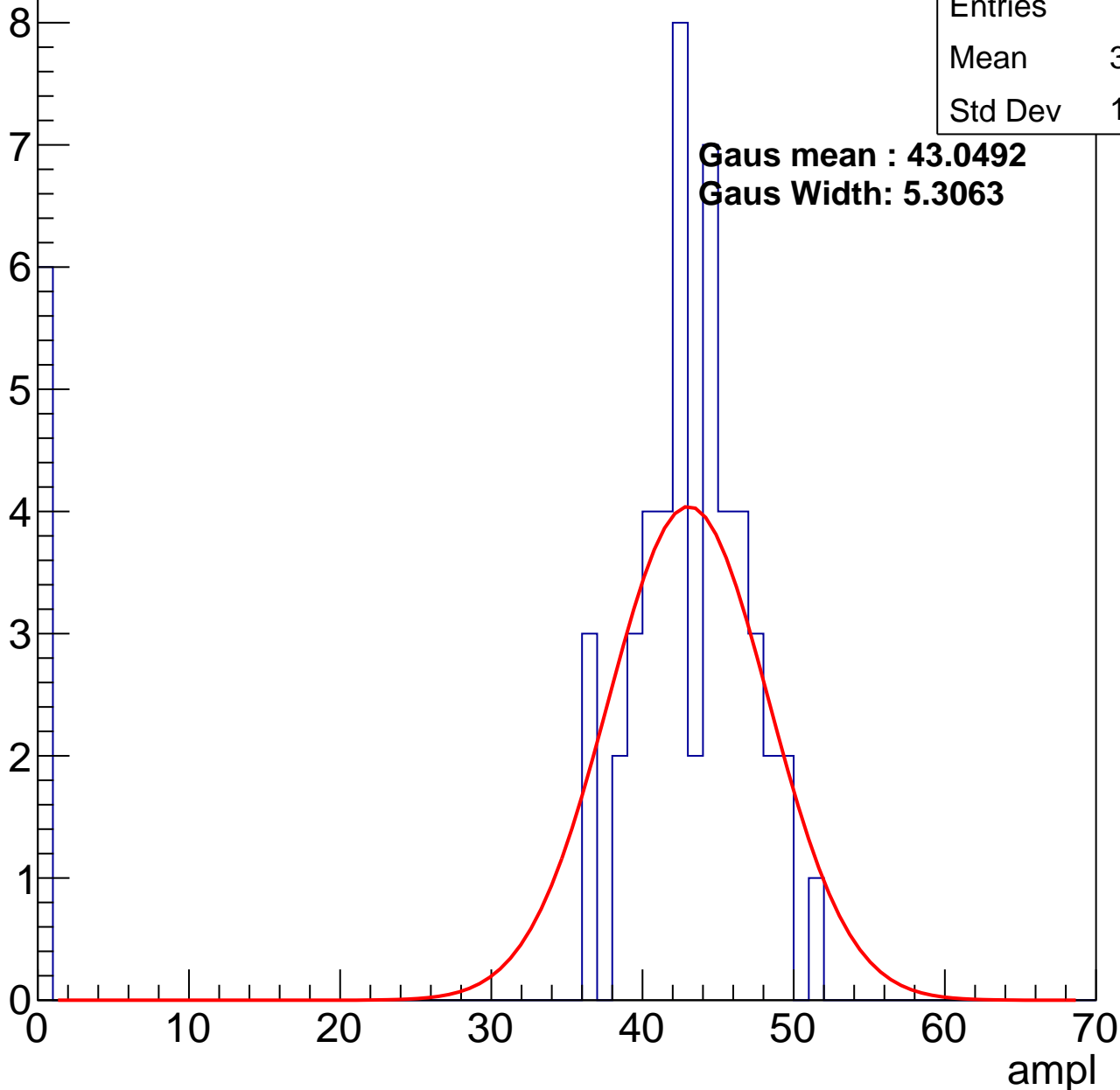
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	38.27
Std Dev	13.79

Gaus mean : 43.0492

Gaus Width: 5.3063

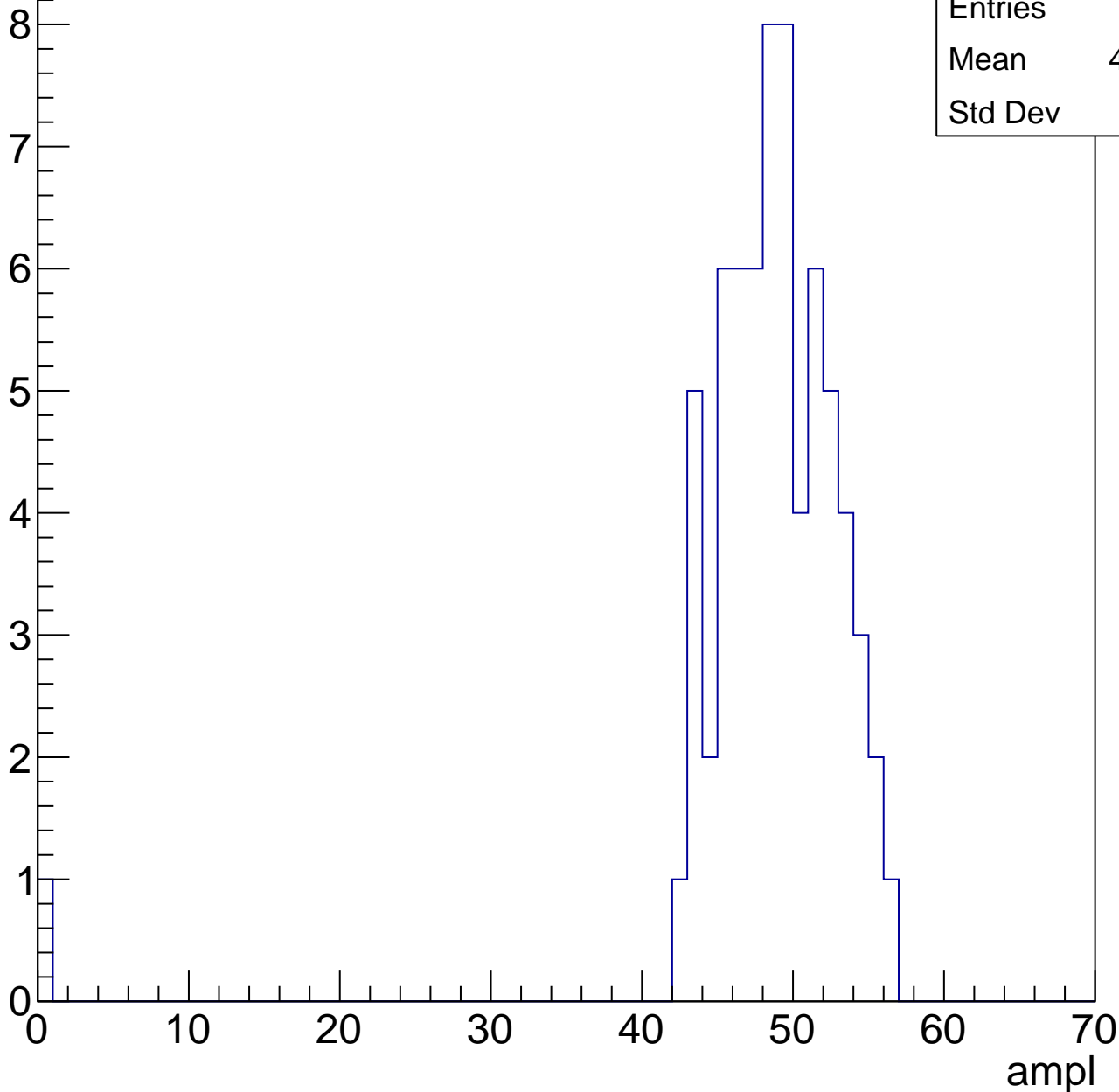


B1L103S, U7-ch27, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	47.87
Std Dev	6.76

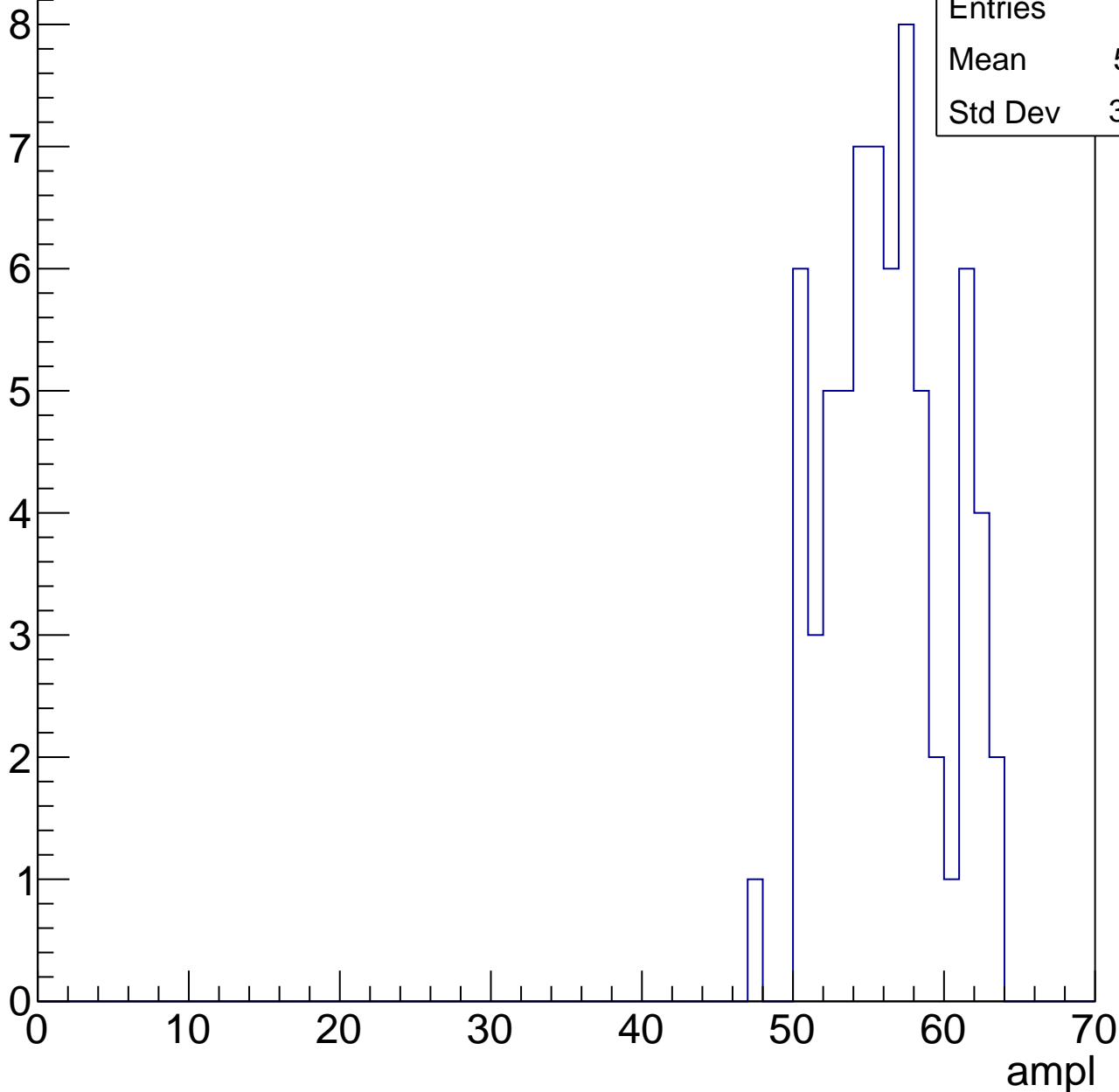


B1L103S, U7-ch27, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	55.71
Std Dev	3.797



B1L103S, U7-ch27, adc5

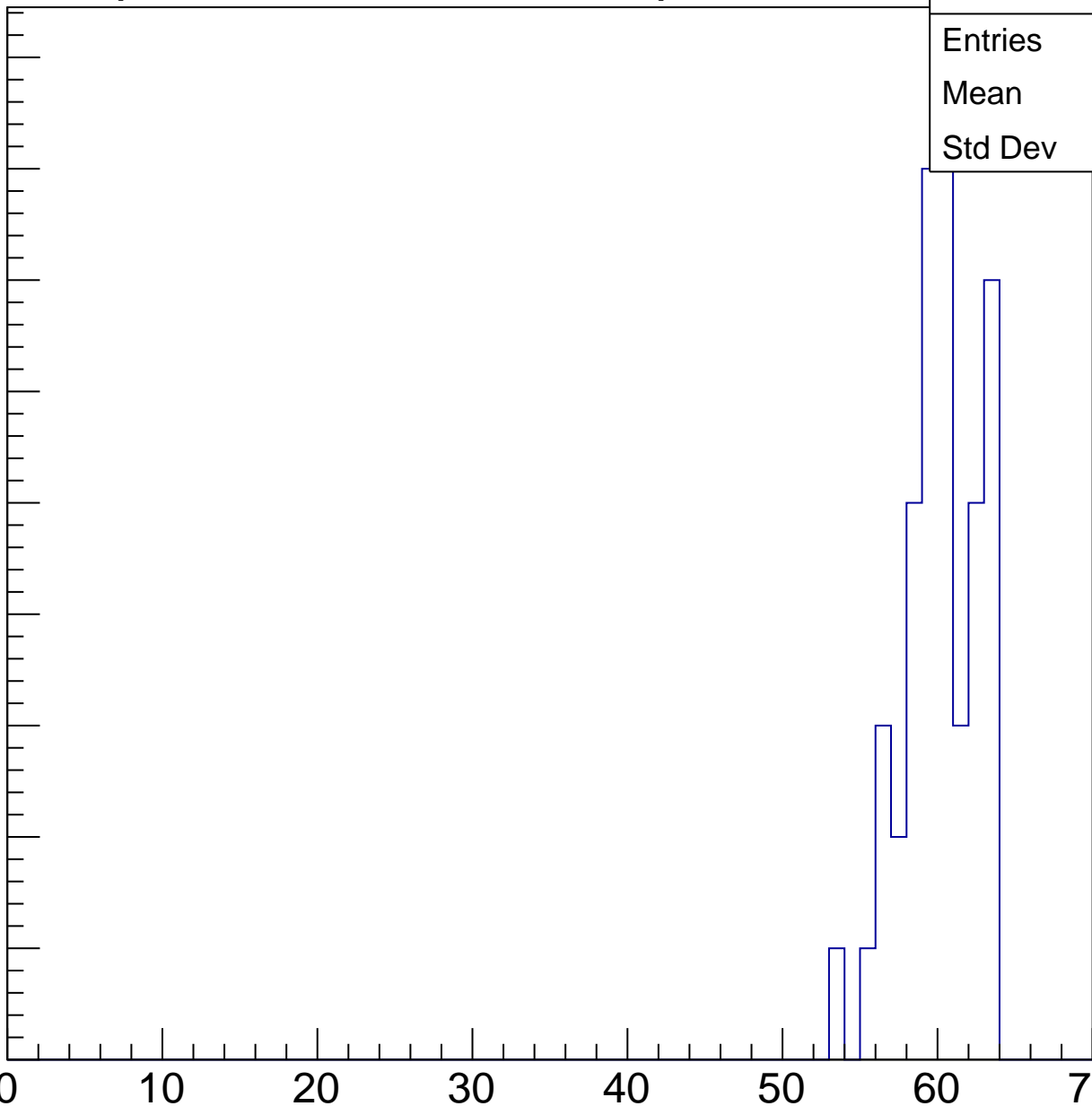
calib_packv5_041523_1651.root, FC#0, port C2

Entry

9
8
7
6
5
4
3
2
1
0

Entries	44
Mean	59.68
Std Dev	2.381

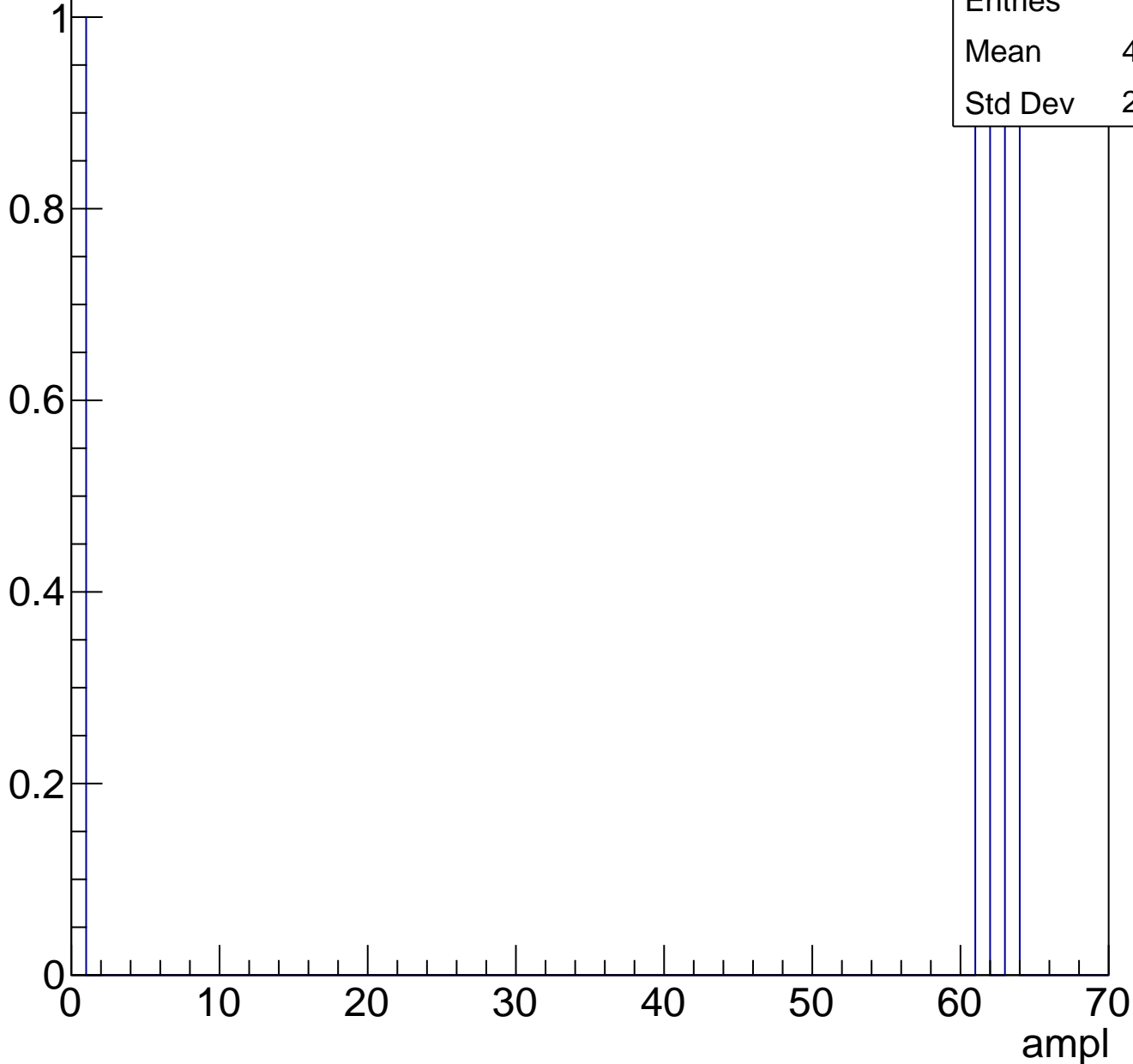
ampl



B1L103S, U7-ch27, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch27, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51

Entry



B1L103S, U7-ch28, adc0

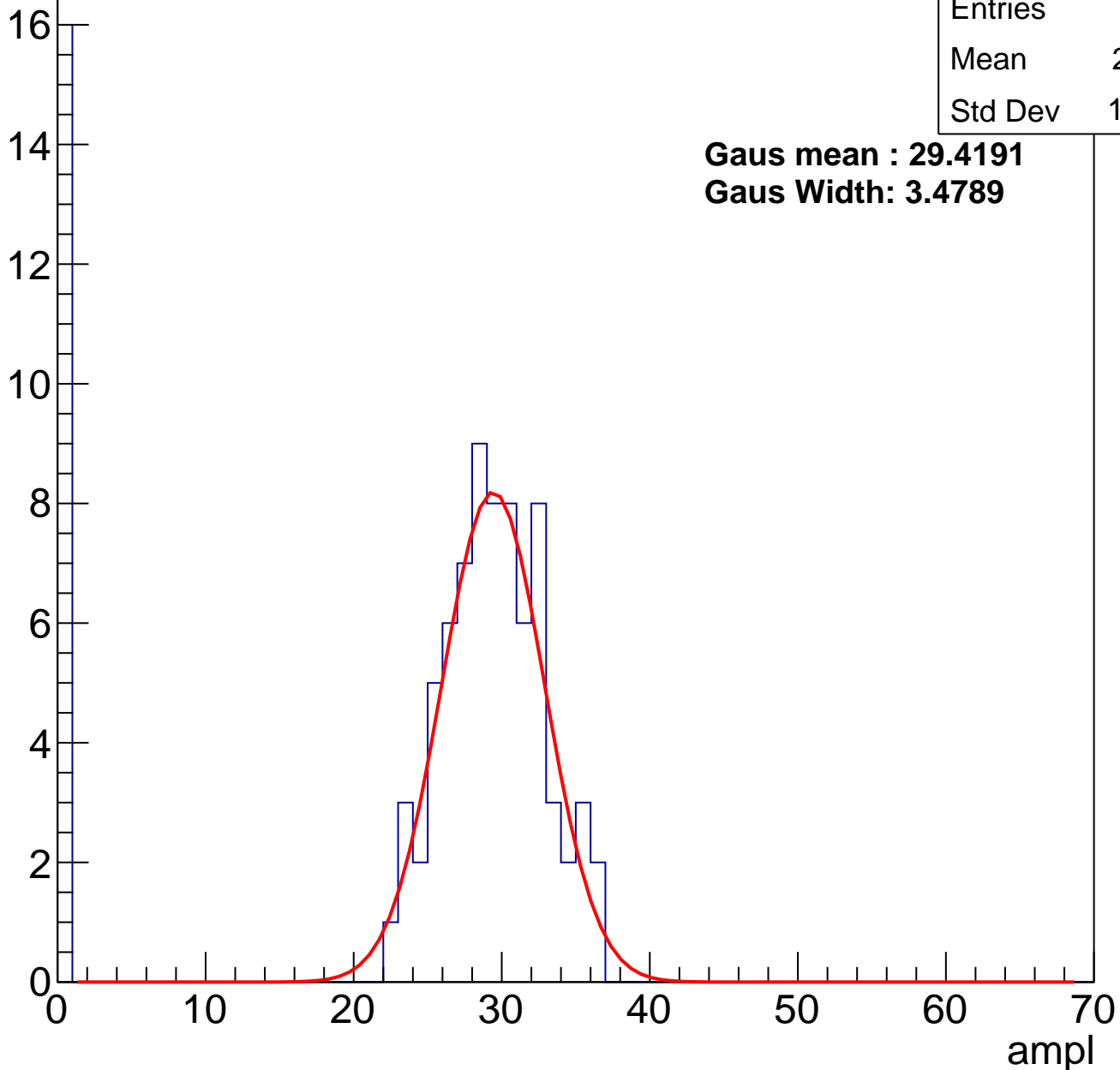
calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	23.81
Std Dev	11.54

Gaus mean : 29.4191

Gaus Width: 3.4789

Entry



B1L103S, U7-ch28, adc1

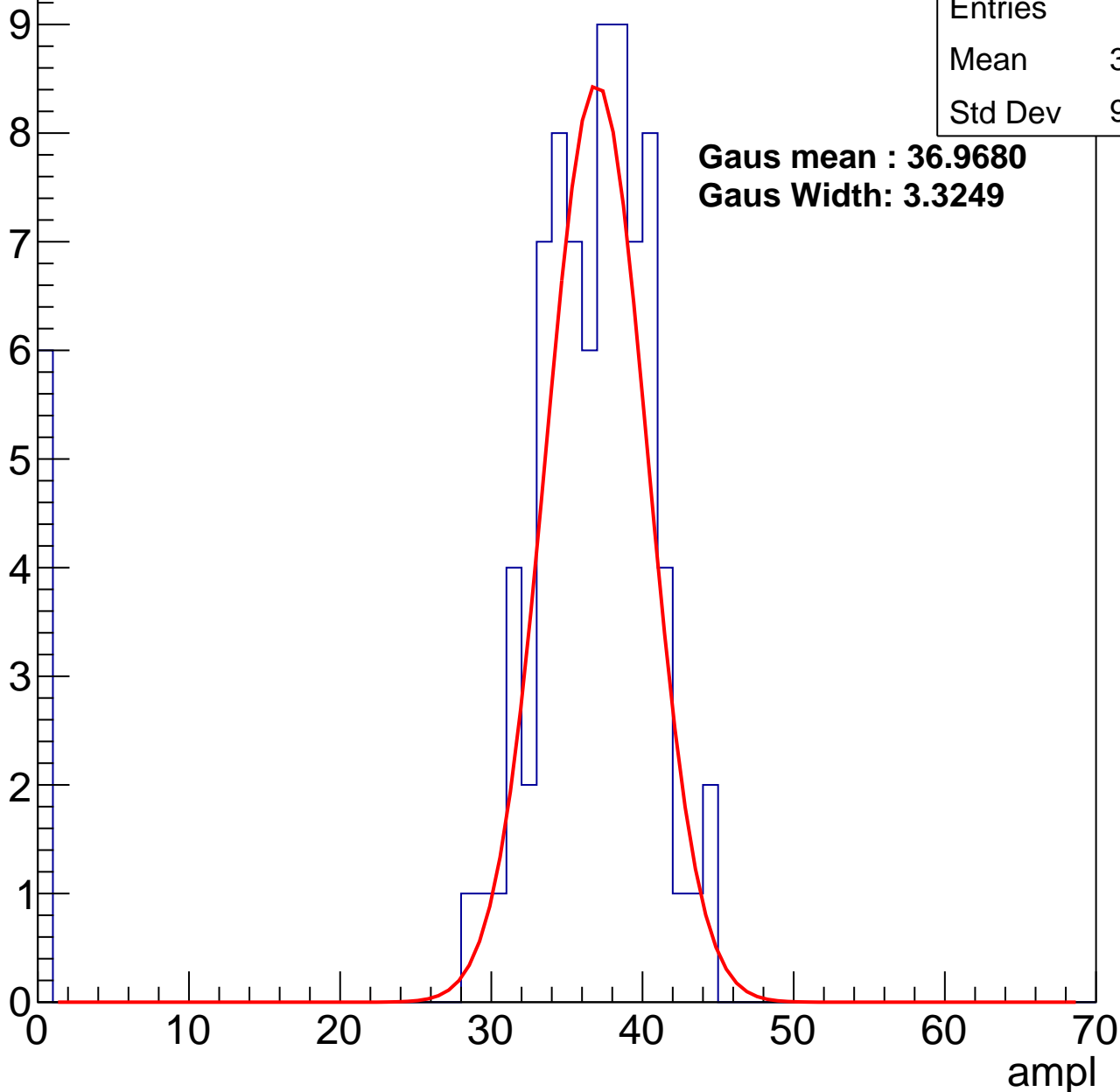
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	84
Mean	33.86
Std Dev	9.954

Gaus mean : 36.9680

Gaus Width: 3.3249



B1L103S, U7-ch28, adc2

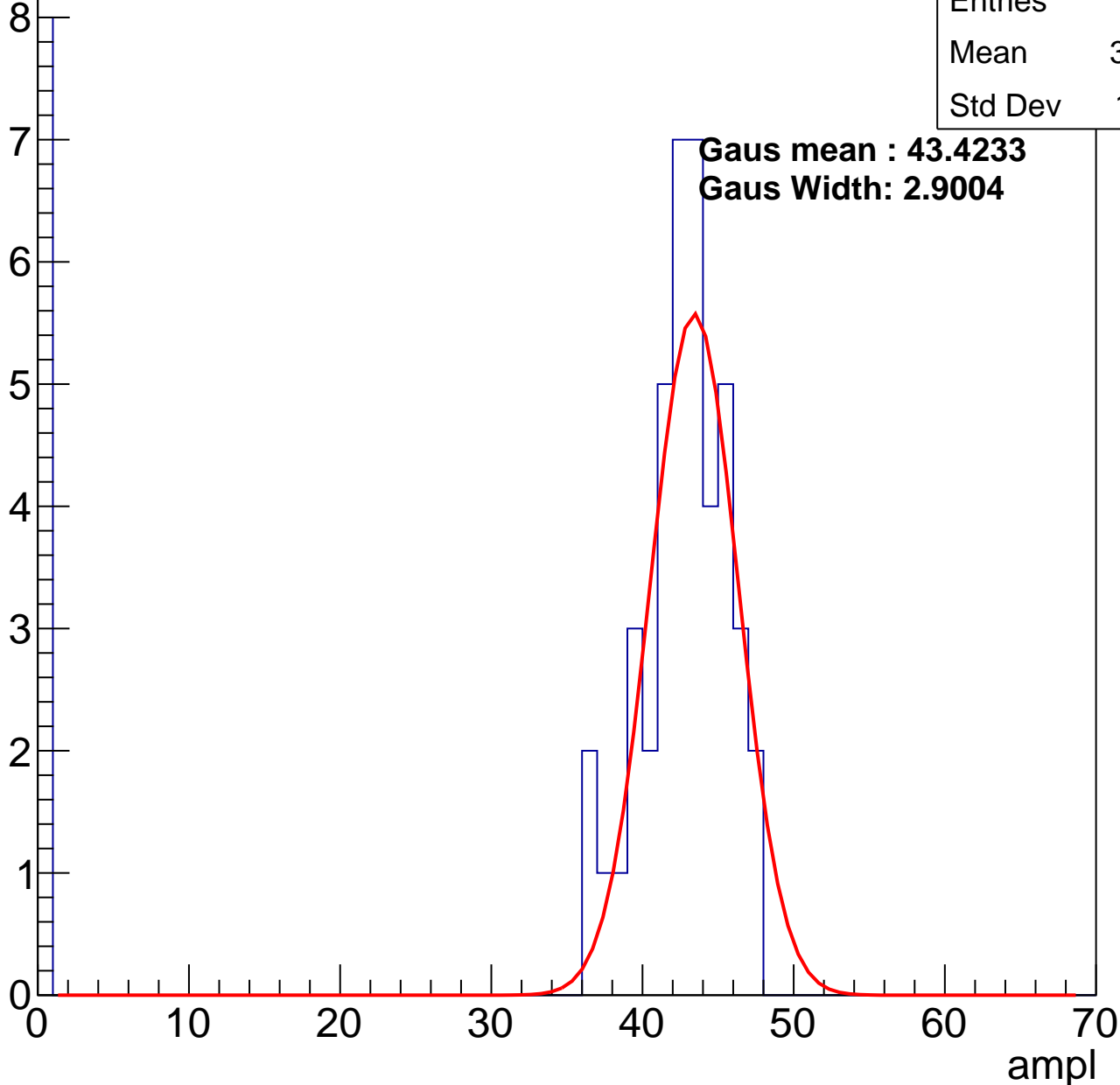
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	35.54
Std Dev	15.71

Gaus mean : 43.4233

Gaus Width: 2.9004



B1L103S, U7-ch28, adc3

calib_packv5_041523_1651.root, FC#0, port C2

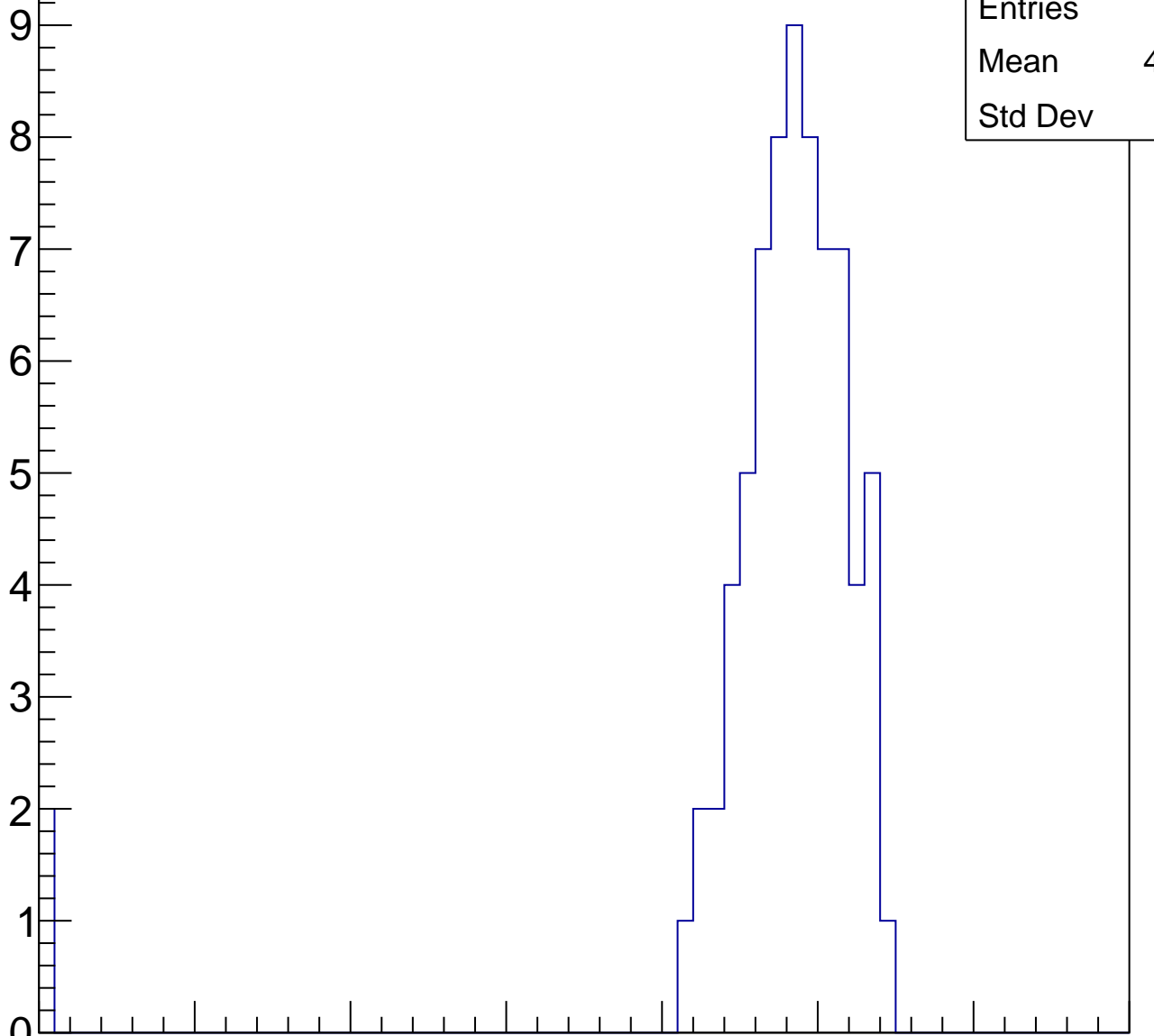
Entry

9
8
7
6
5
4
3
2
1
0

Entries	72
Mean	46.78
Std Dev	8.45

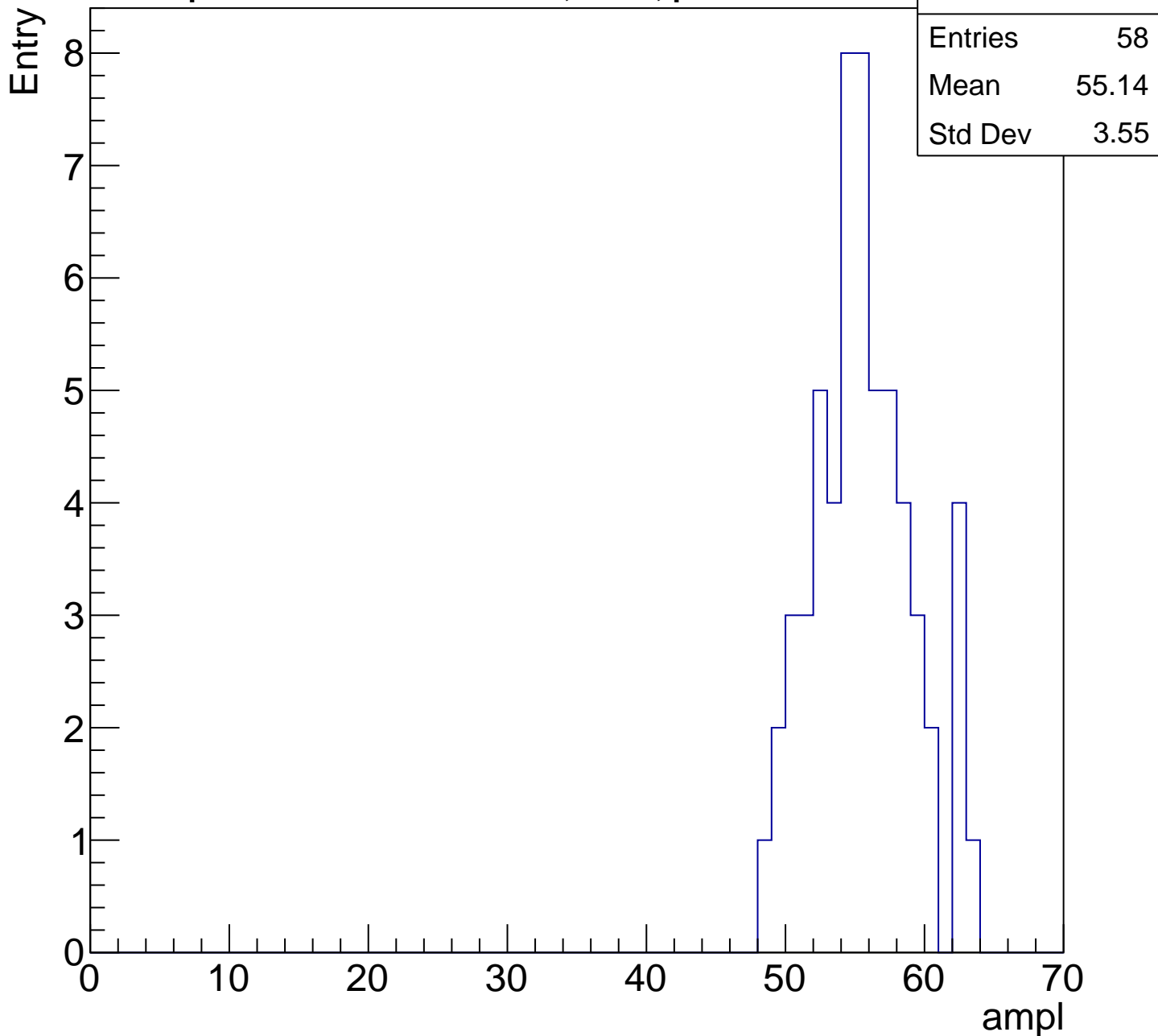
ampl

0 10 20 30 40 50 60 70



B1L103S, U7-ch28, adc4

calib_packv5_041523_1651.root, FC#0, port C2

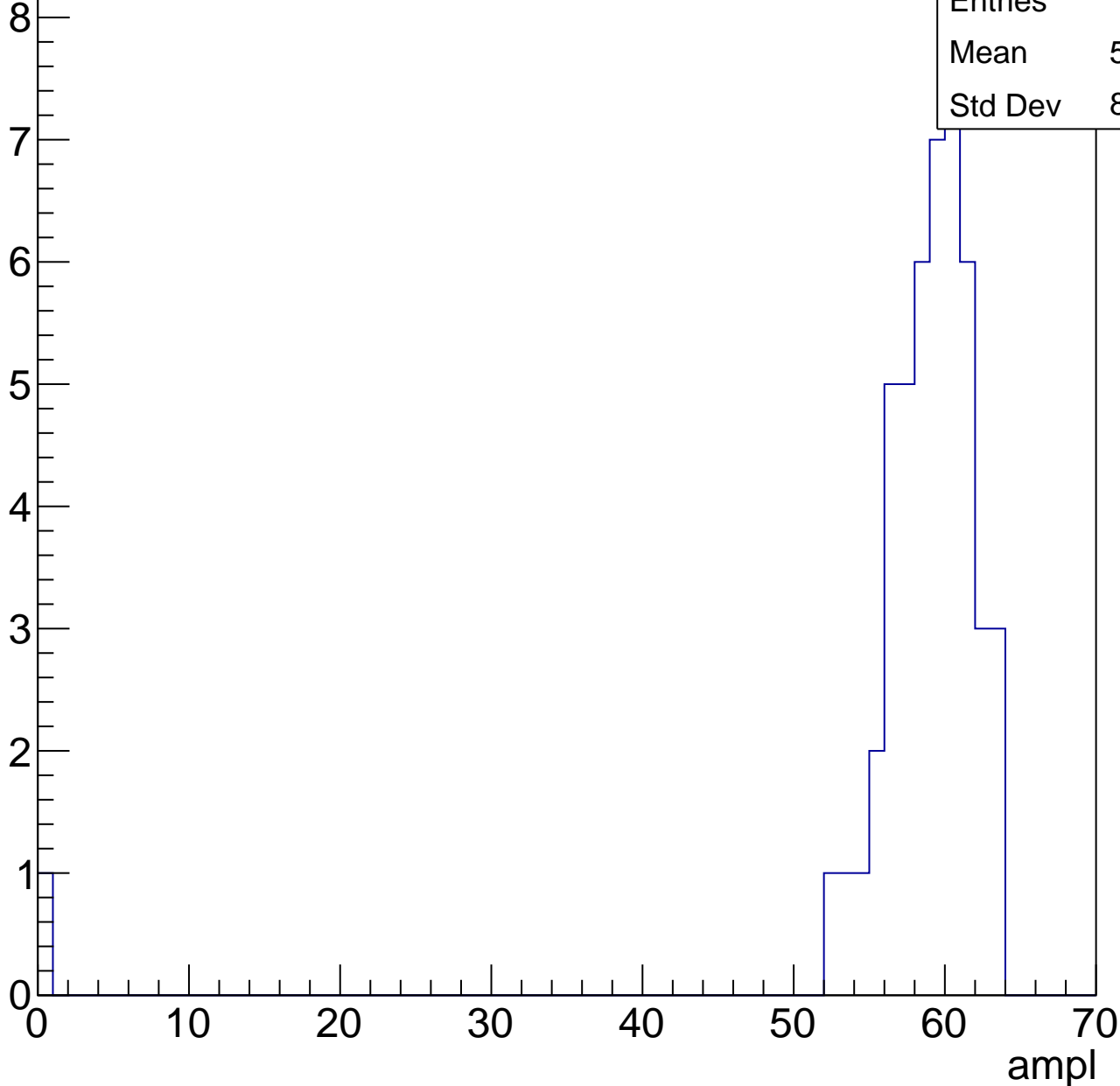


B1L103S, U7-ch28, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	57.47
Std Dev	8.673

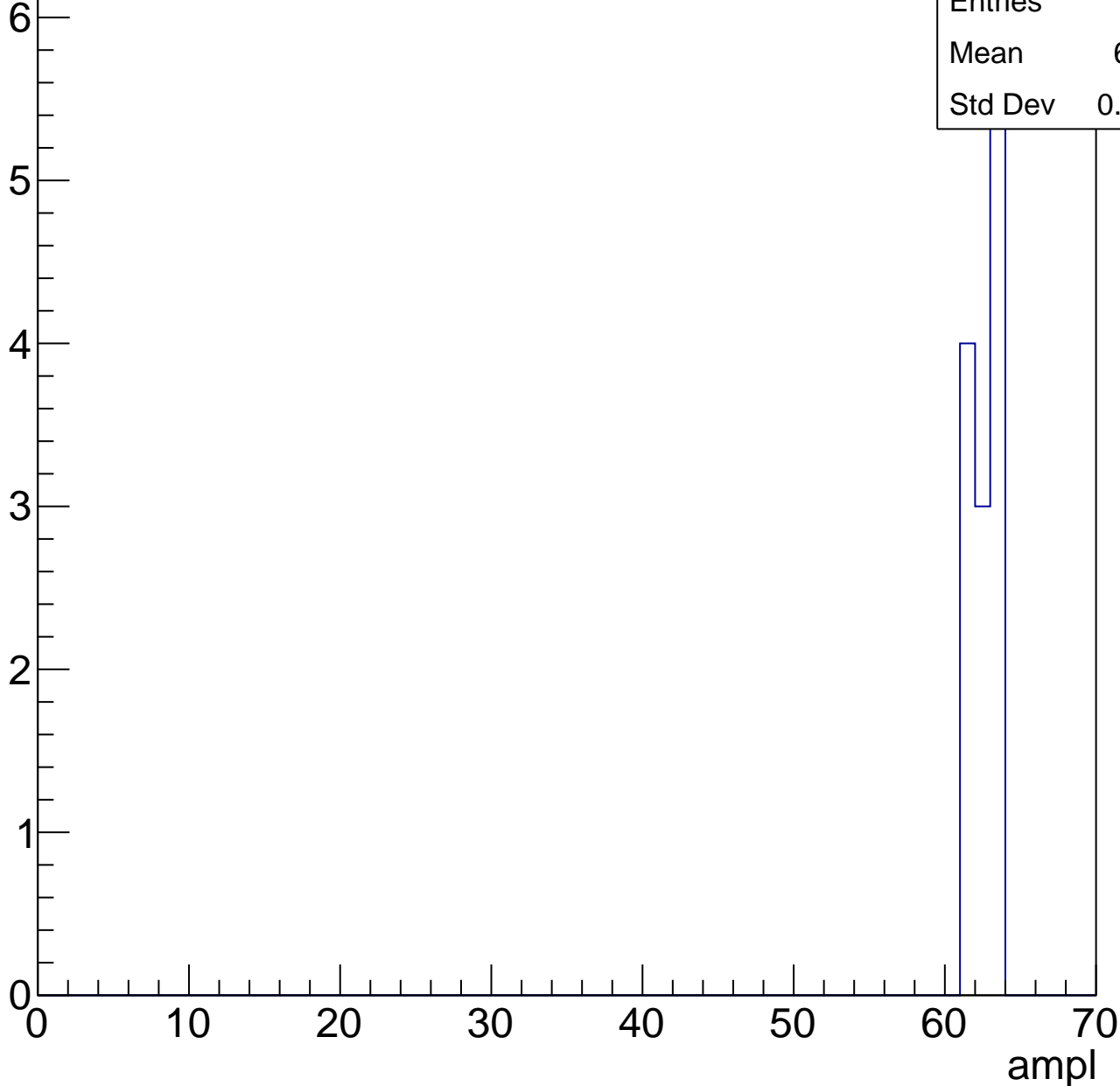


B1L103S, U7-ch28, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	13
Mean	62.15
Std Dev	0.8635



B1L103S, U7-ch28, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U7-ch29, adc0

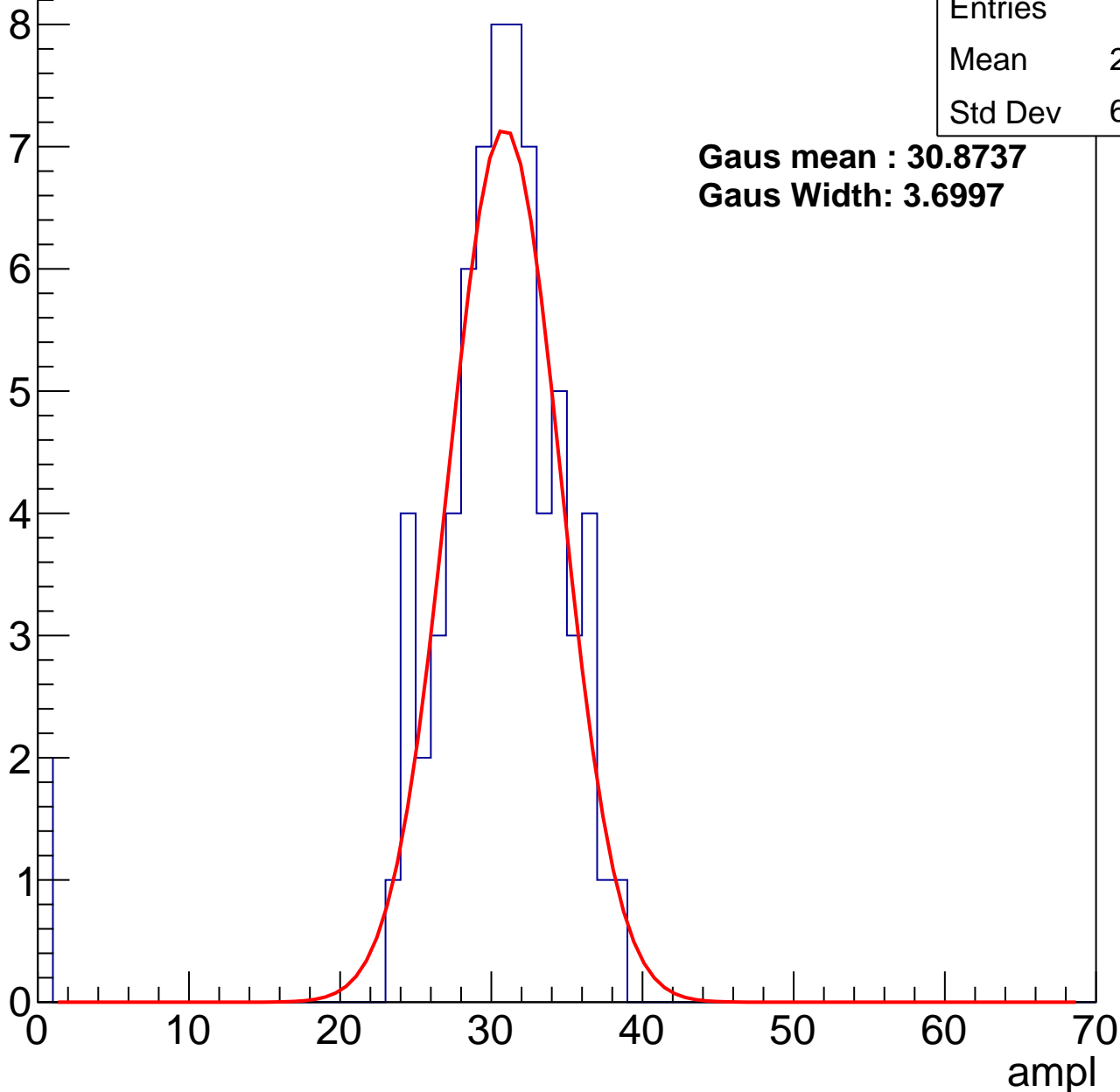
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	29.49
Std Dev	6.122

Gaus mean : 30.8737

Gaus Width: 3.6997



B1L103S, U7-ch29, adc1

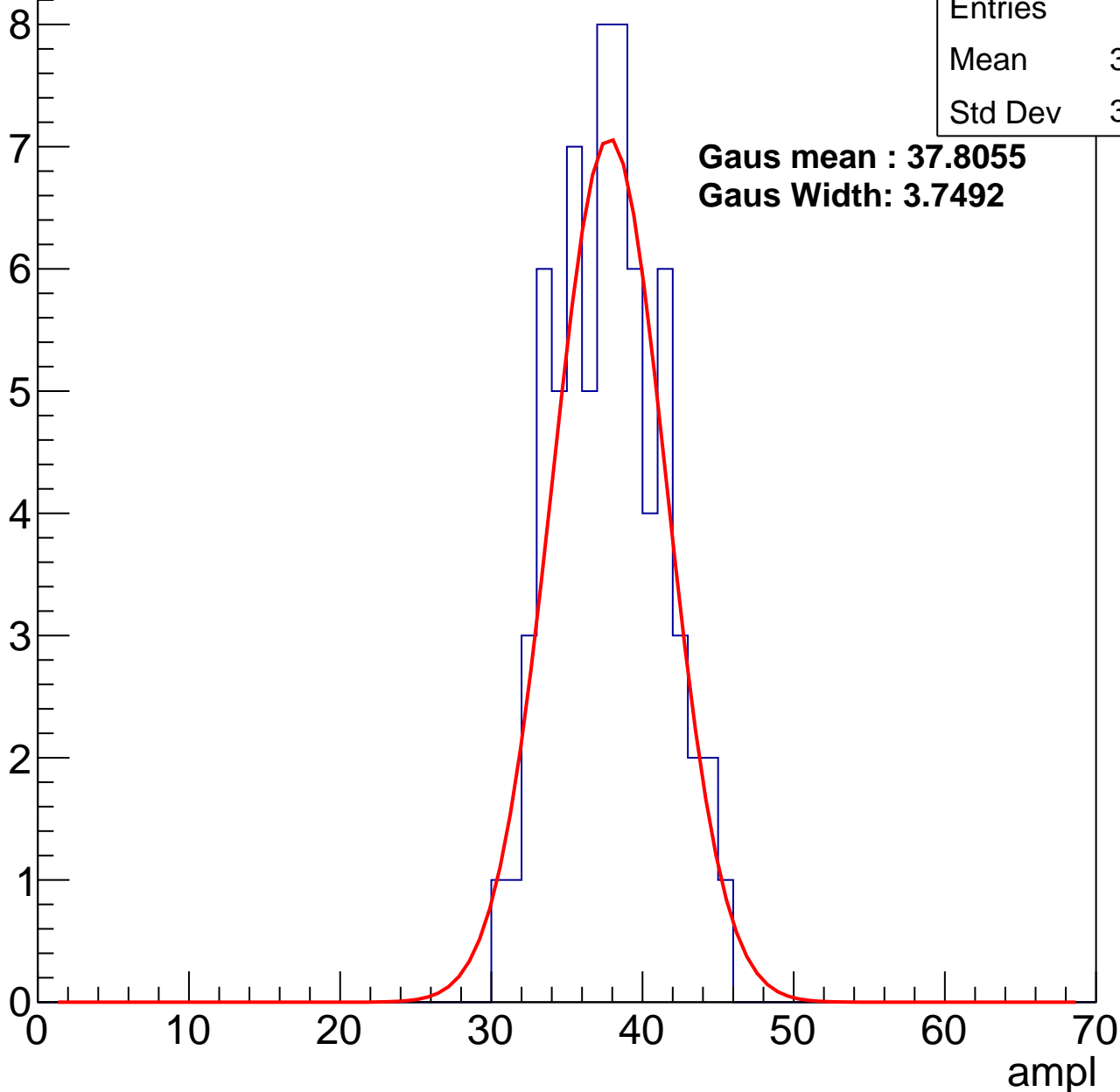
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	37.28
Std Dev	3.434

Gaus mean : 37.8055

Gaus Width: 3.7492



B1L103S, U7-ch29, adc2

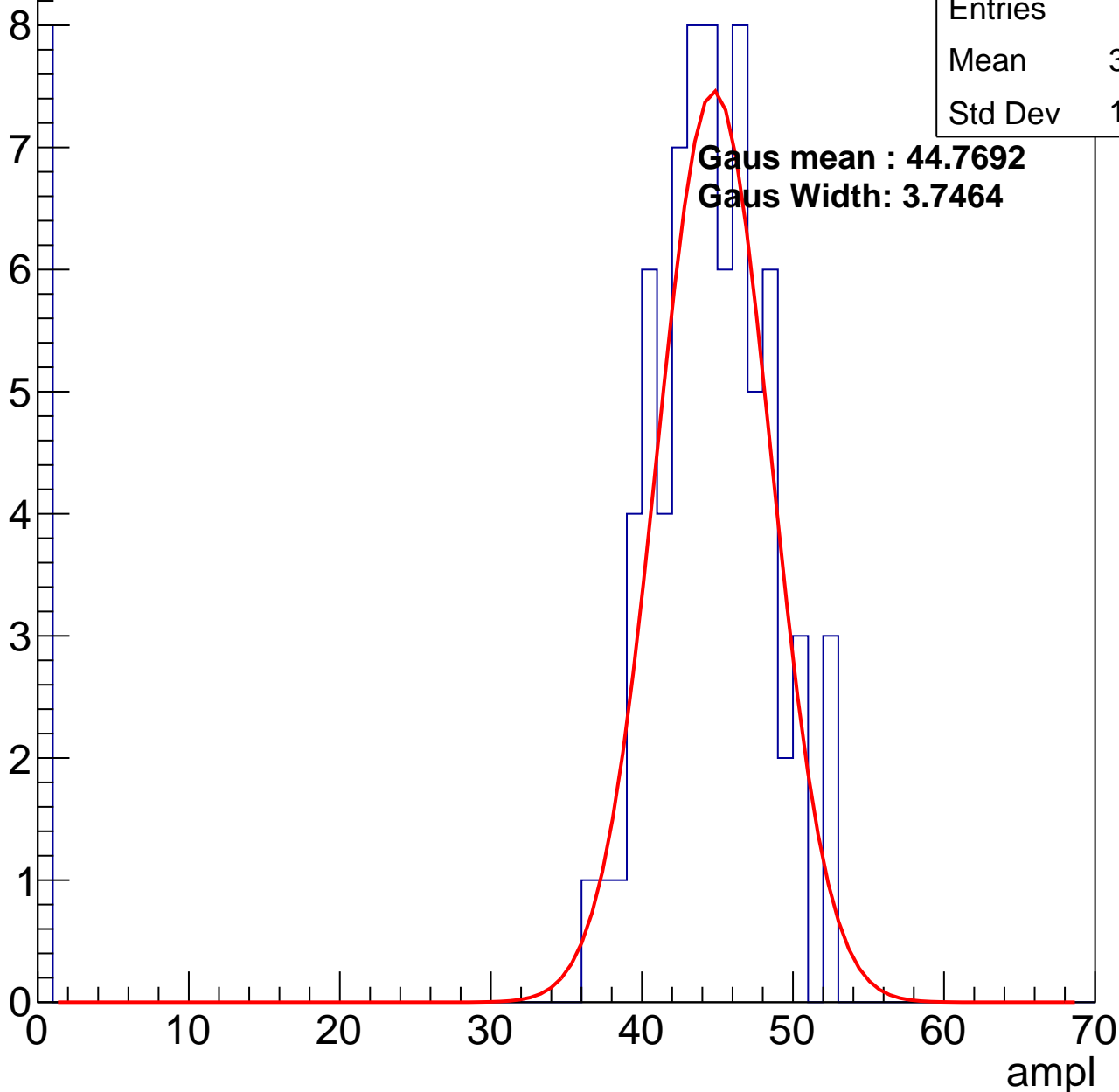
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	81
Mean	39.83
Std Dev	13.62

Gaus mean : 44.7692

Gaus Width: 3.7464

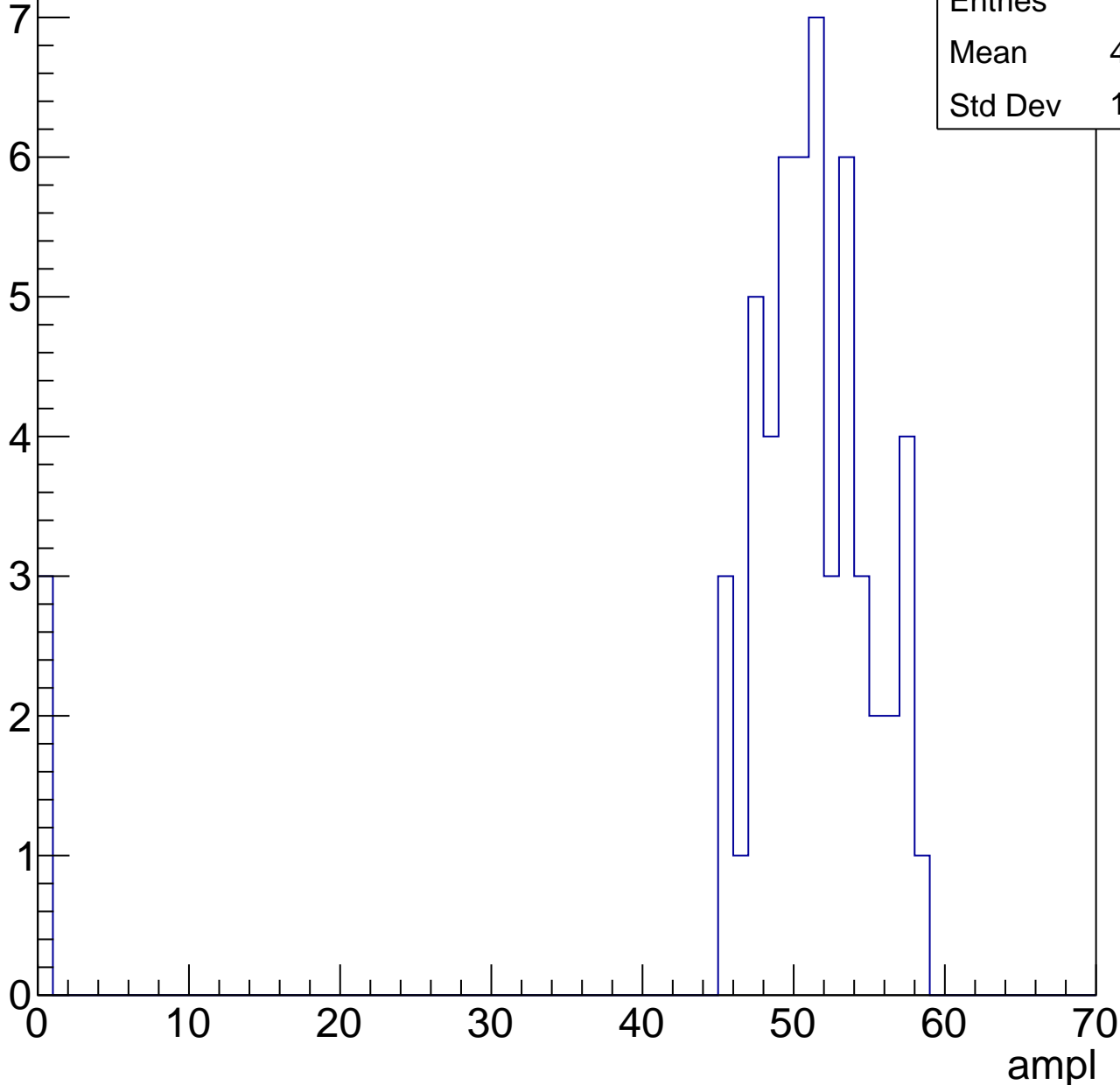


B1L103S, U7-ch29, adc3

calib_packv5_041523_1651.root, FC#0, port C2

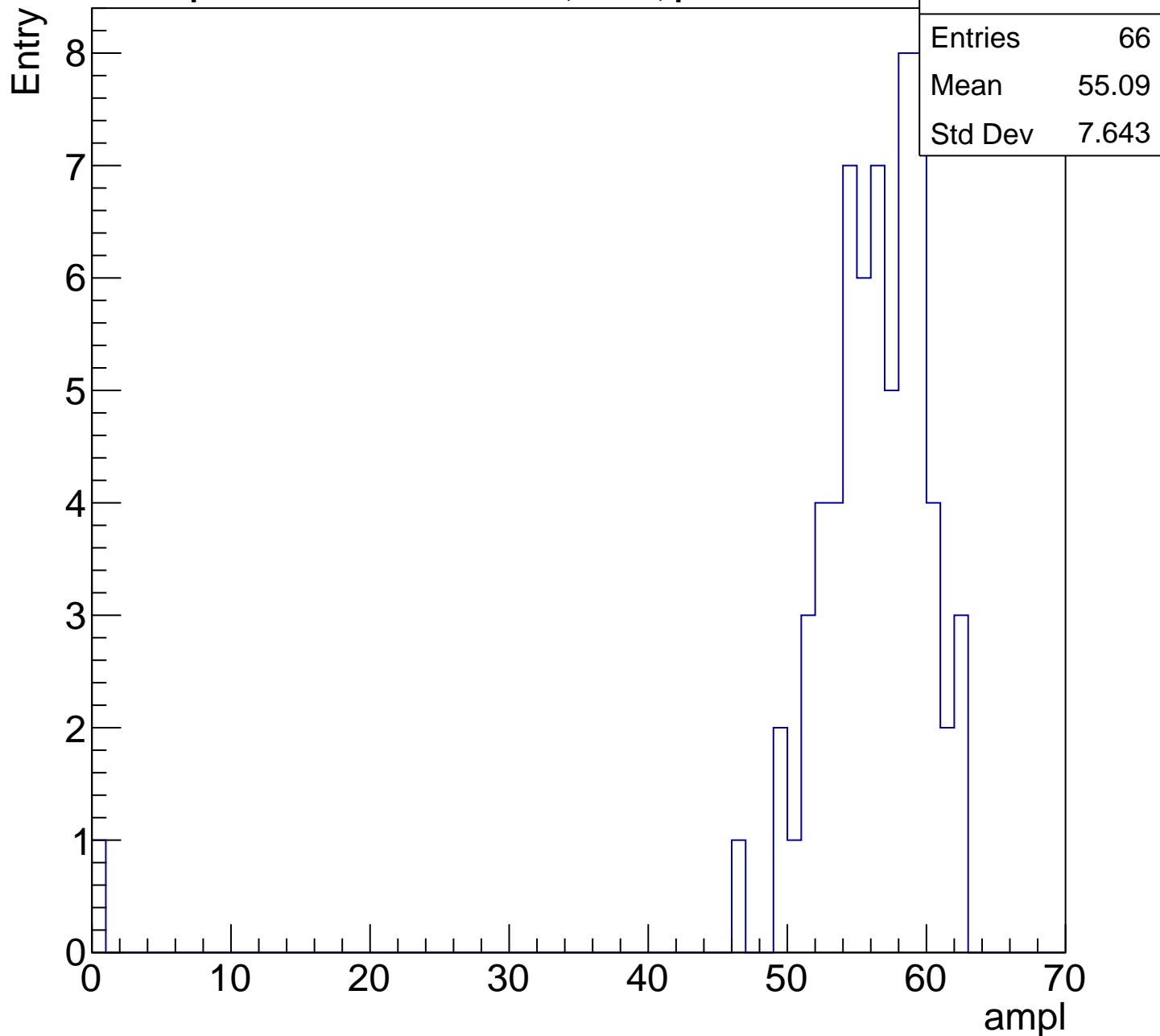
Entry

Entries	56
Mean	48.27
Std Dev	11.95



B1L103S, U7-ch29, adc4

calib_packv5_041523_1651.root, FC#0, port C2

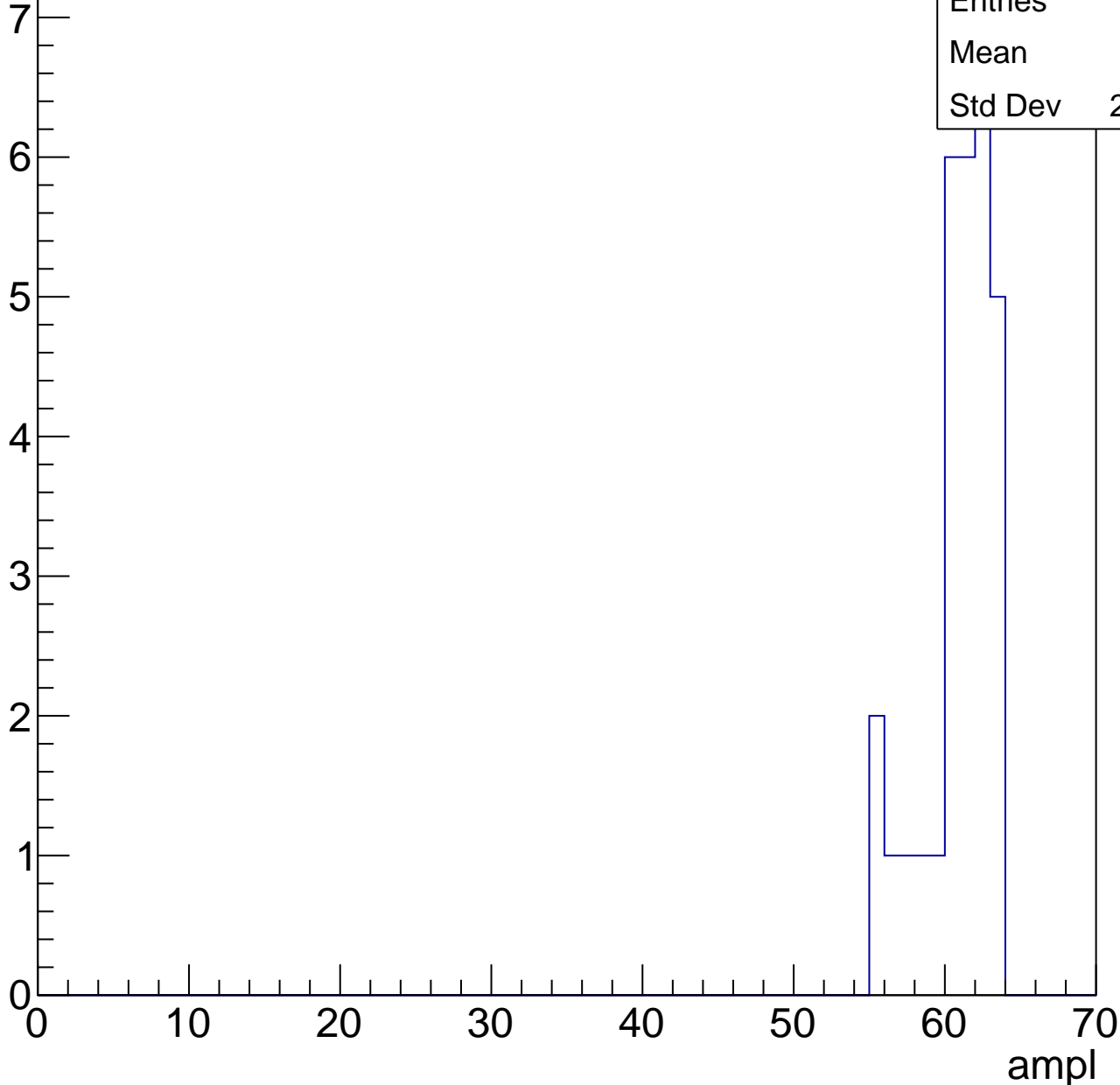


B1L103S, U7-ch29, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	30
Mean	60.5
Std Dev	2.247

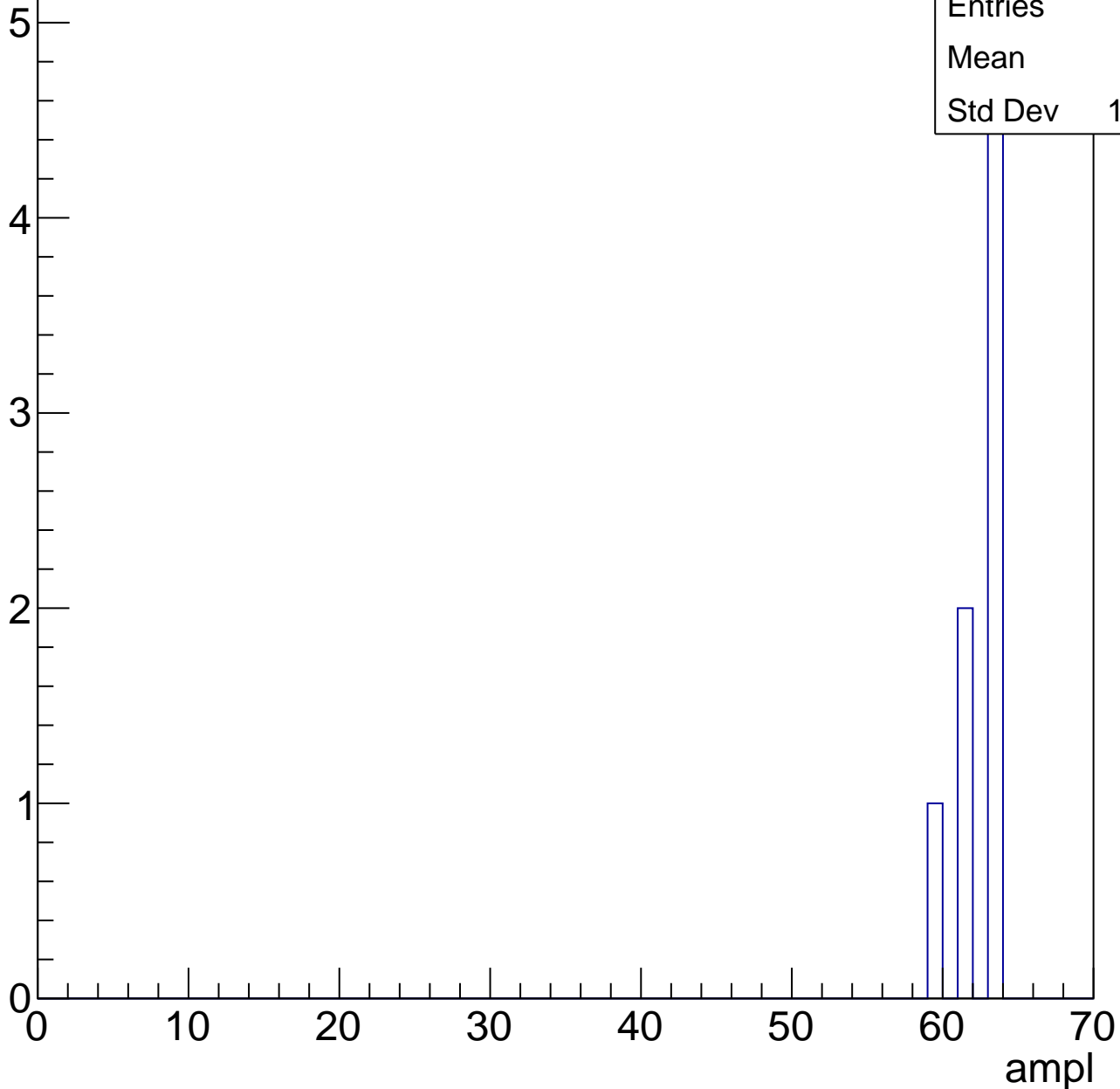


B1L103S, U7-ch29, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	8
Mean	62
Std Dev	1.414



B1L103S, U7-ch29, adc7

calib_packv5_041523_1651.root, FC#0, port C2

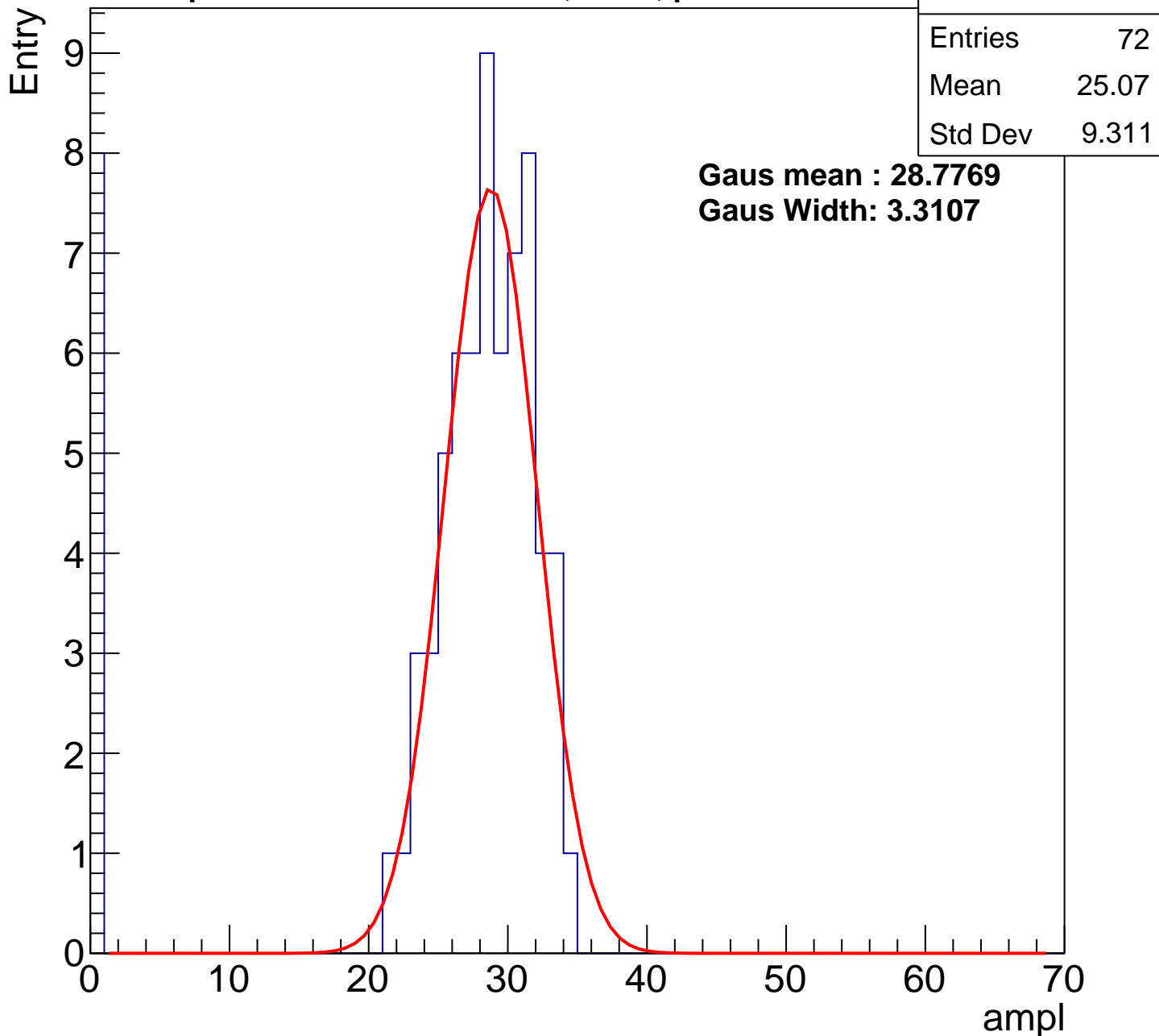
Entries	19
Mean	1.211
Std Dev	5.136

Entry



B1L103S, U7-ch30, adc0

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U7-ch30, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	74
Mean	30.22
Std Dev	12.27

Gaus mean : 35.4736

Gaus Width: 2.9273

Entry

10

8

6

4

2

0

0

10

20

30

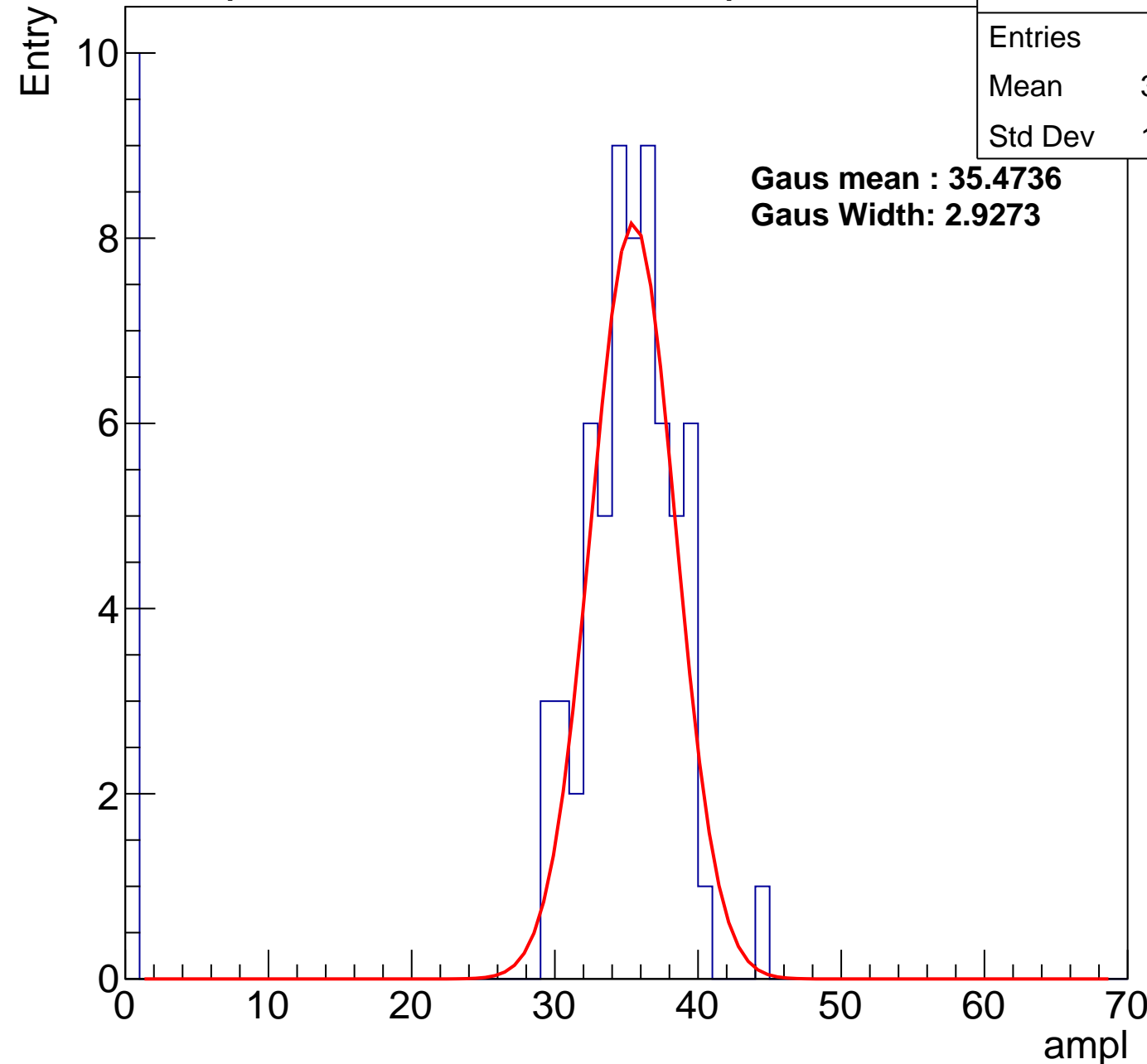
40

50

60

70

ampl



B1L103S, U7-ch30, adc2

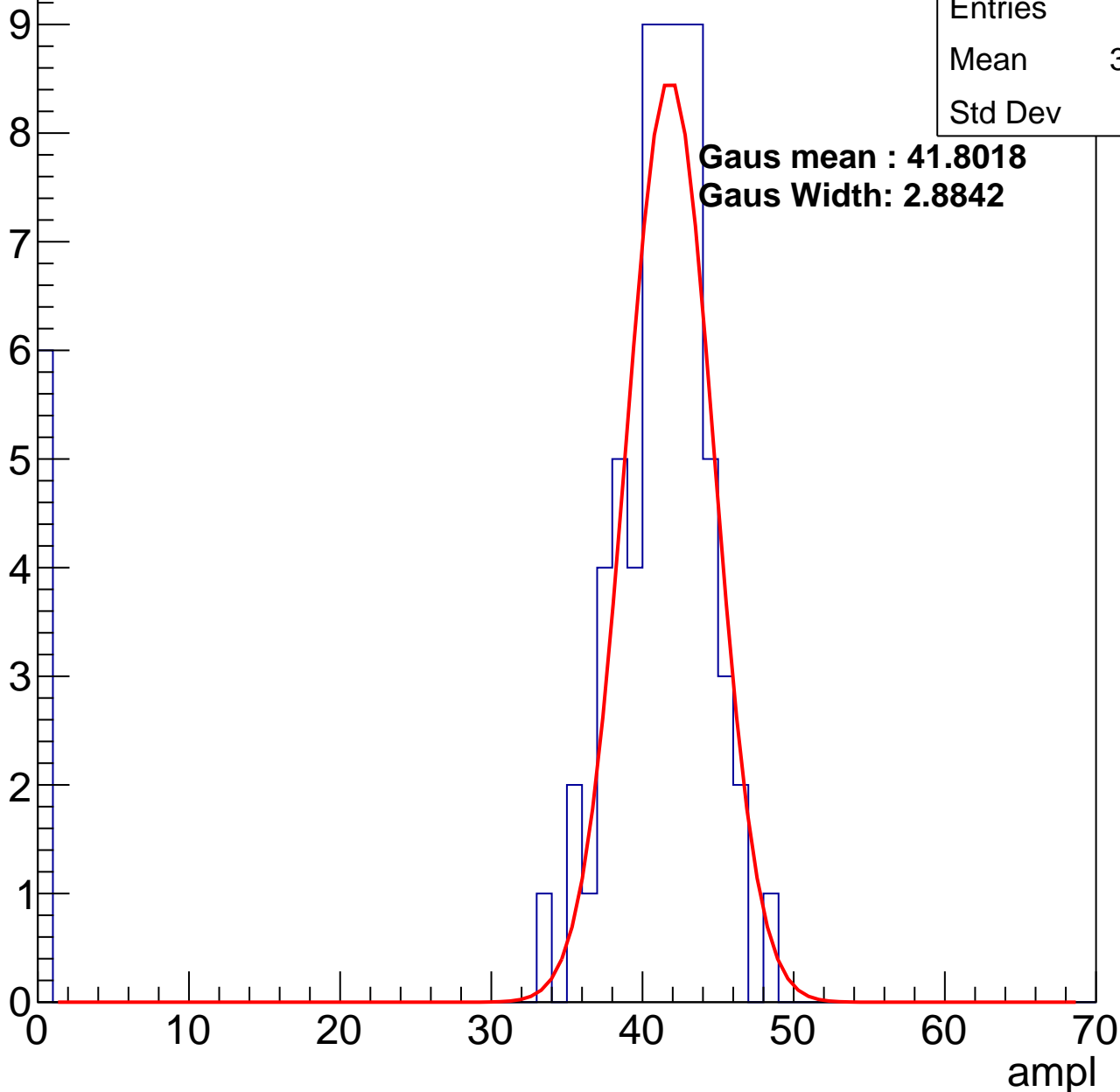
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	37.46
Std Dev	11.8

Gaus mean : 41.8018

Gaus Width: 2.8842

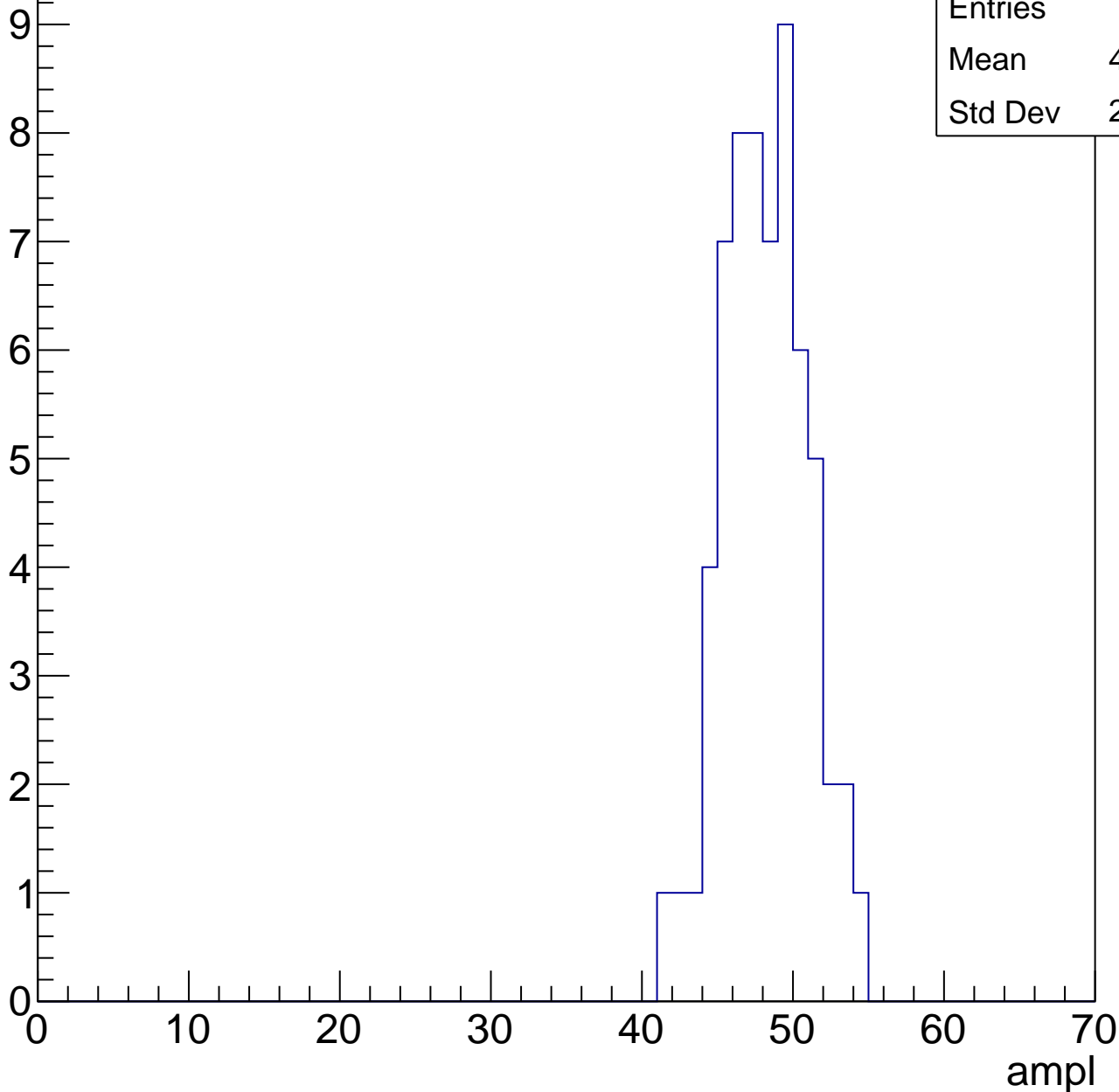


B1L103S, U7-ch30, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	47.69
Std Dev	2.745

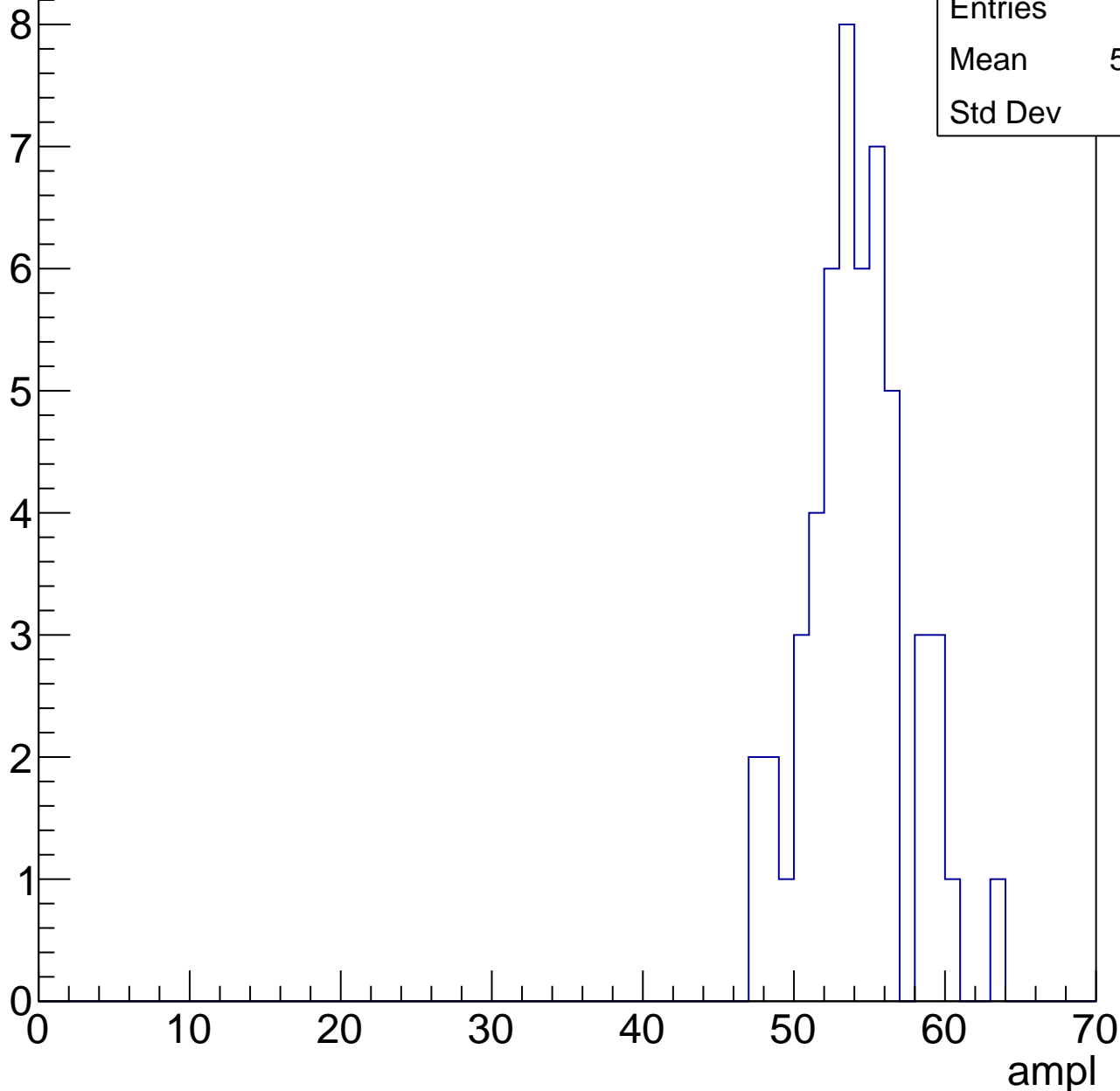


B1L103S, U7-ch30, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	53.69
Std Dev	3.32

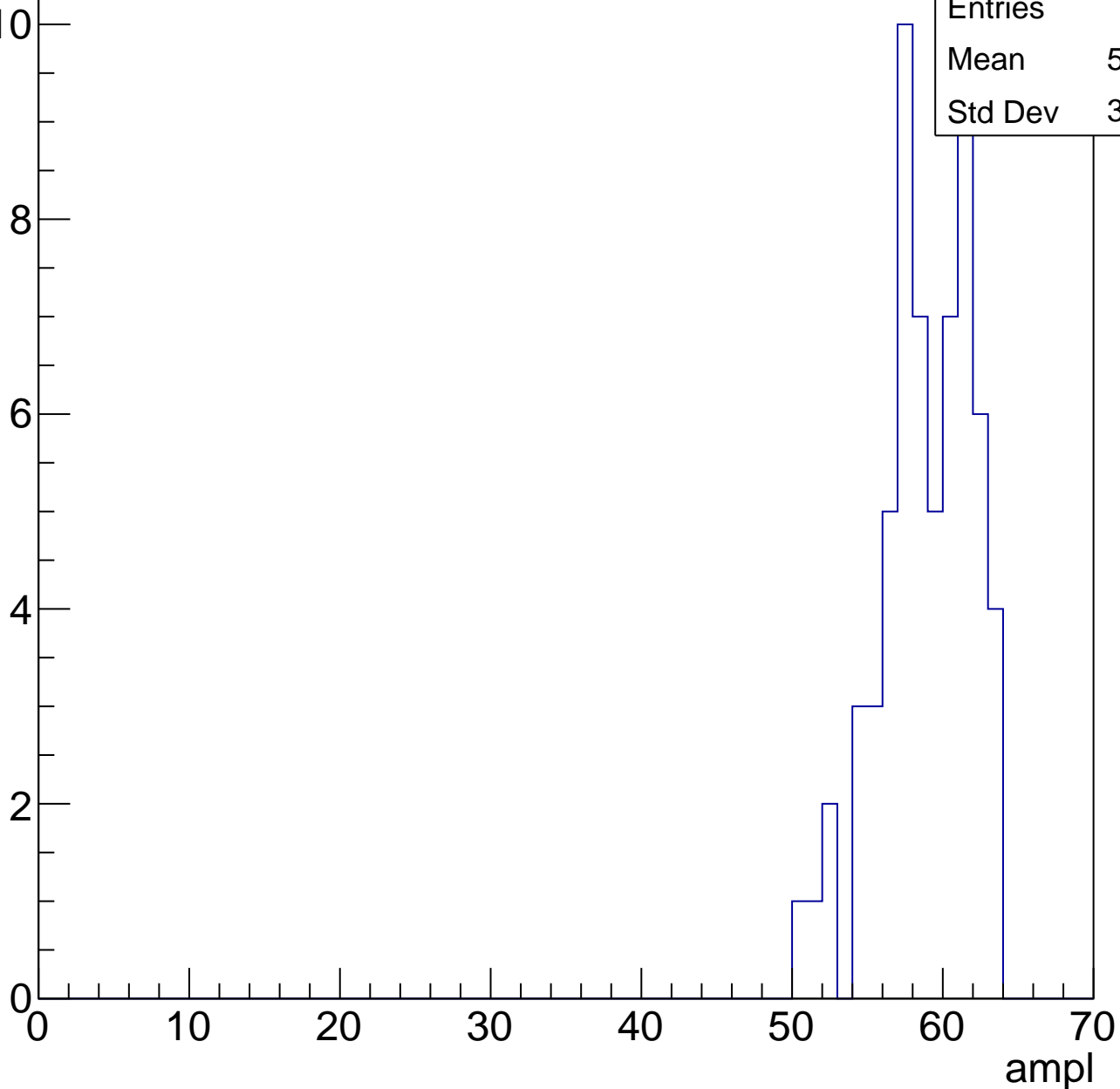


B1L103S, U7-ch30, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	58.35
Std Dev	3.066

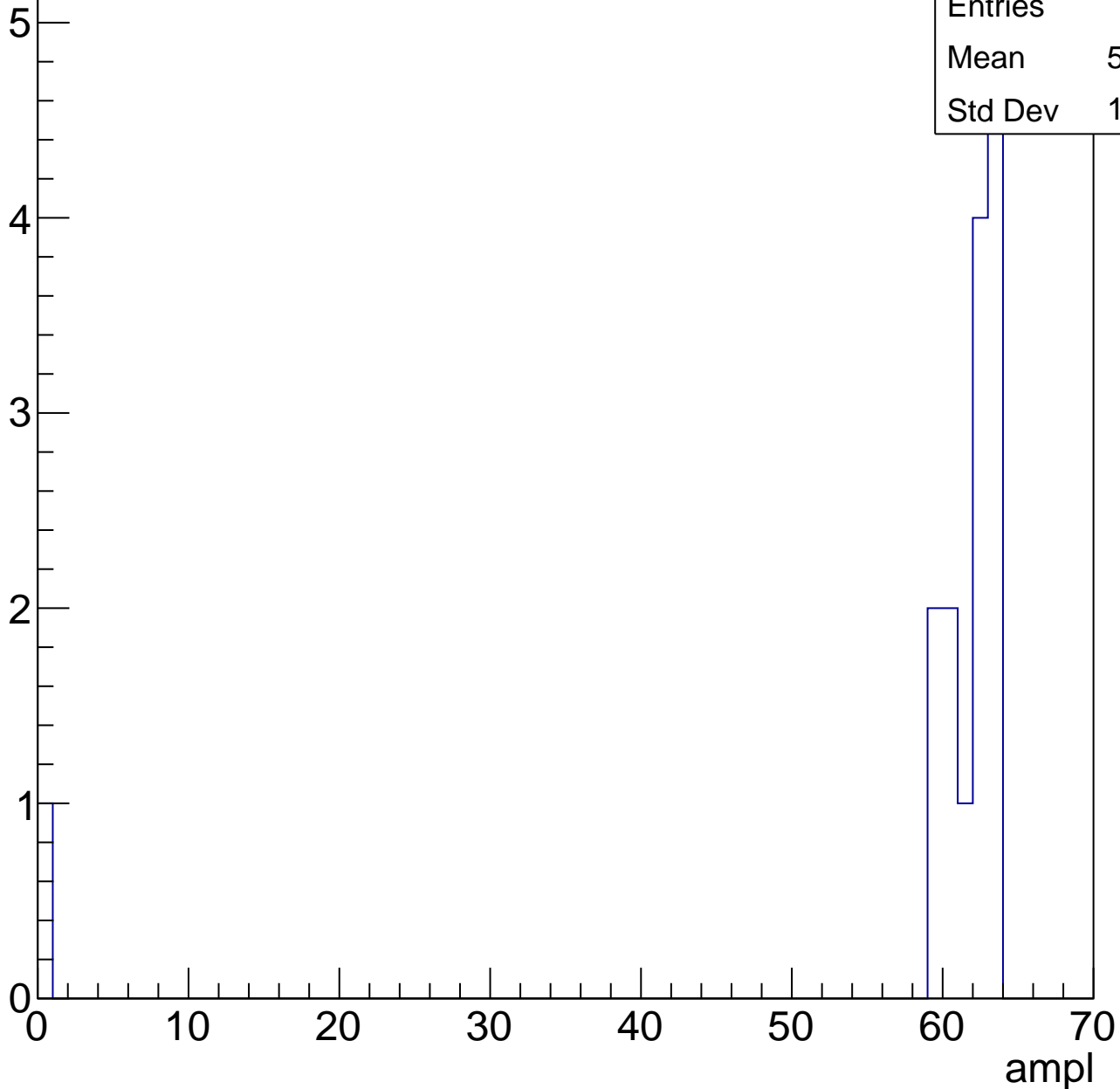


B1L103S, U7-ch30, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	15
Mean	57.47
Std Dev	15.42



B1L103S, U7-ch30, adc7

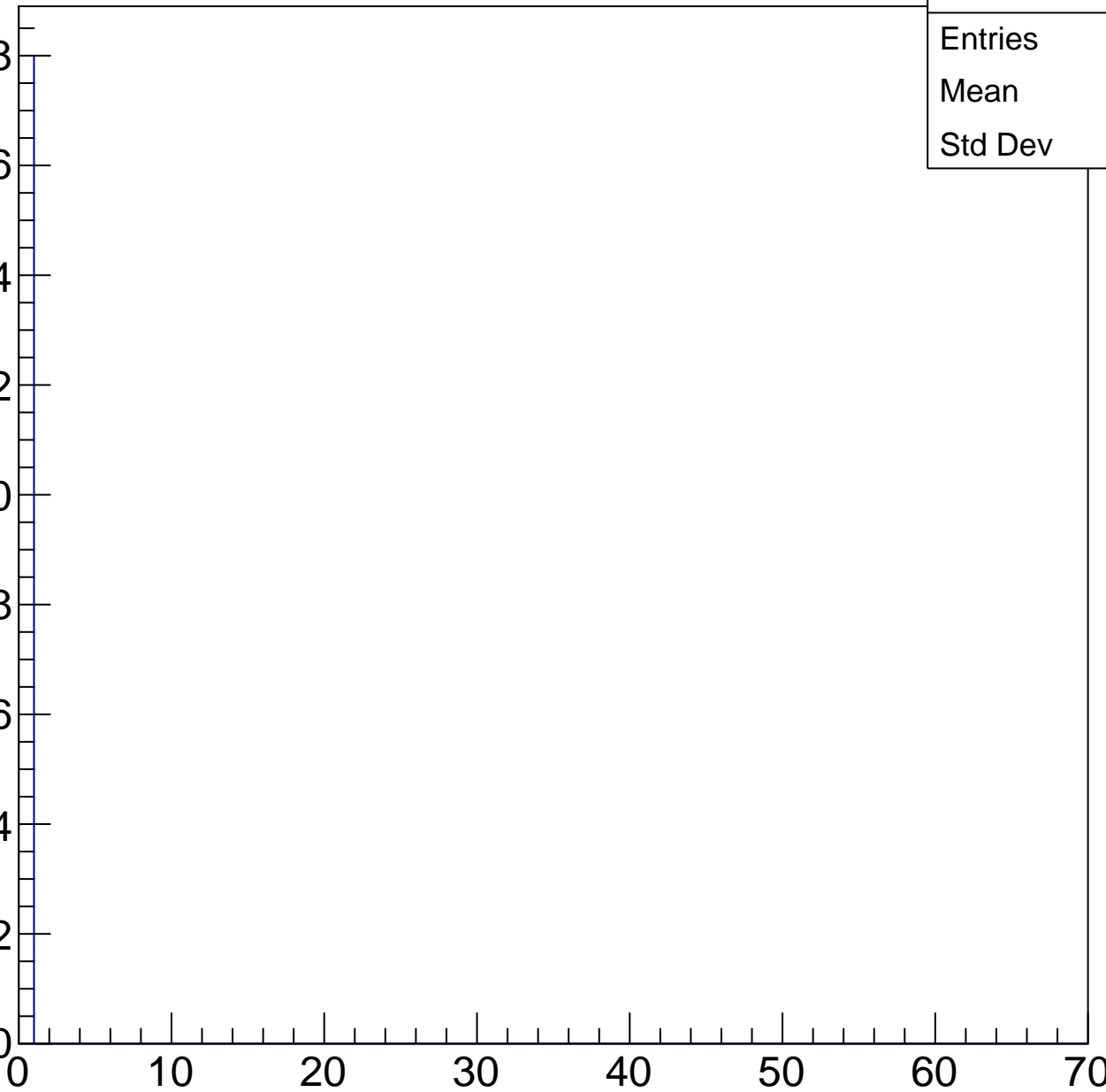
calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	18
Mean	0
Std Dev	0

ampl



B1L103S, U7-ch31, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entry

12
10
8
6
4
2
0

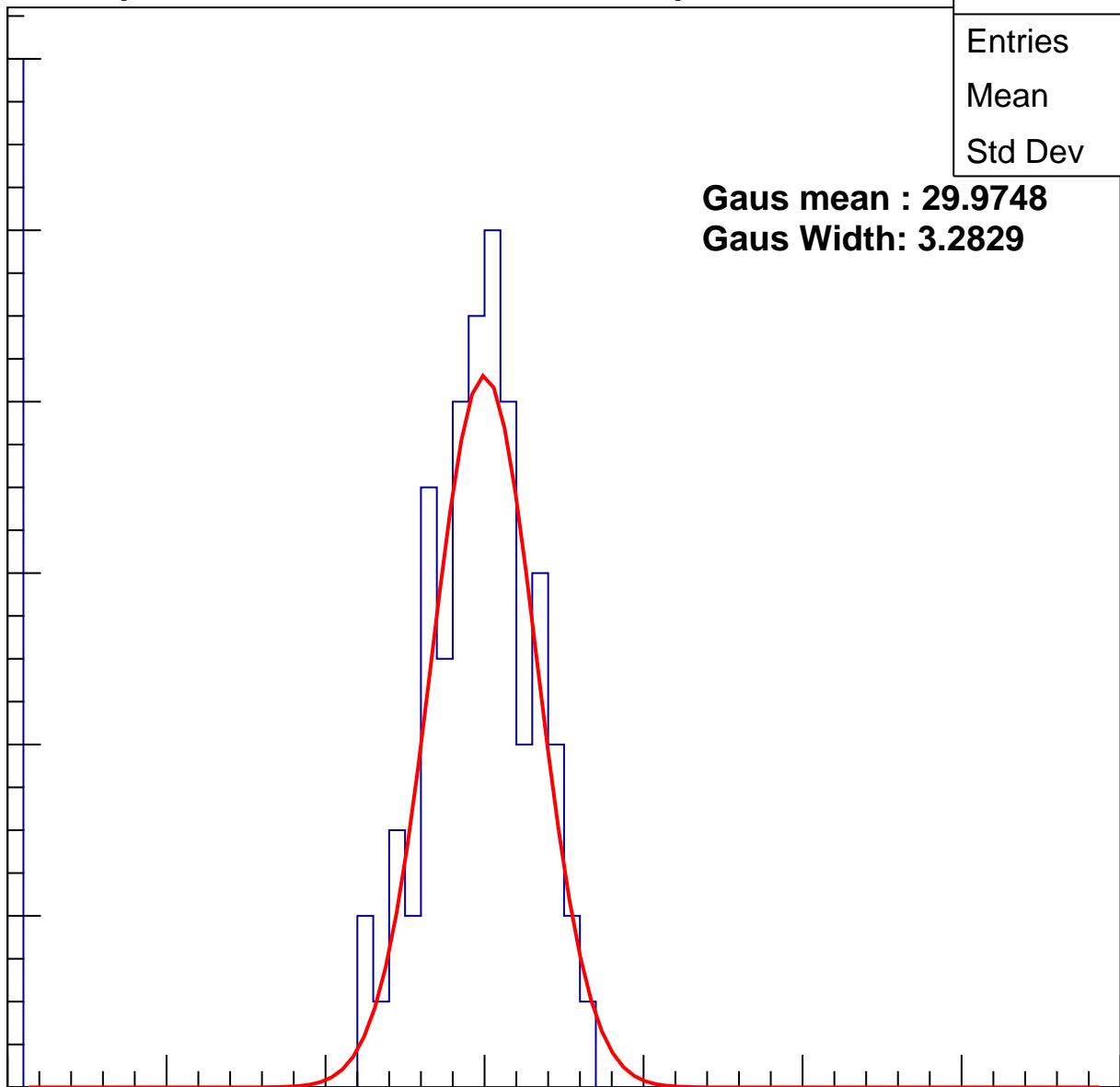
Entries	84
Mean	25.08
Std Dev	10.65

Gaus mean : 29.9748

Gaus Width: 3.2829

0 10 20 30 40 50 60 70

ampl



B1L103S, U7-ch31, adc1

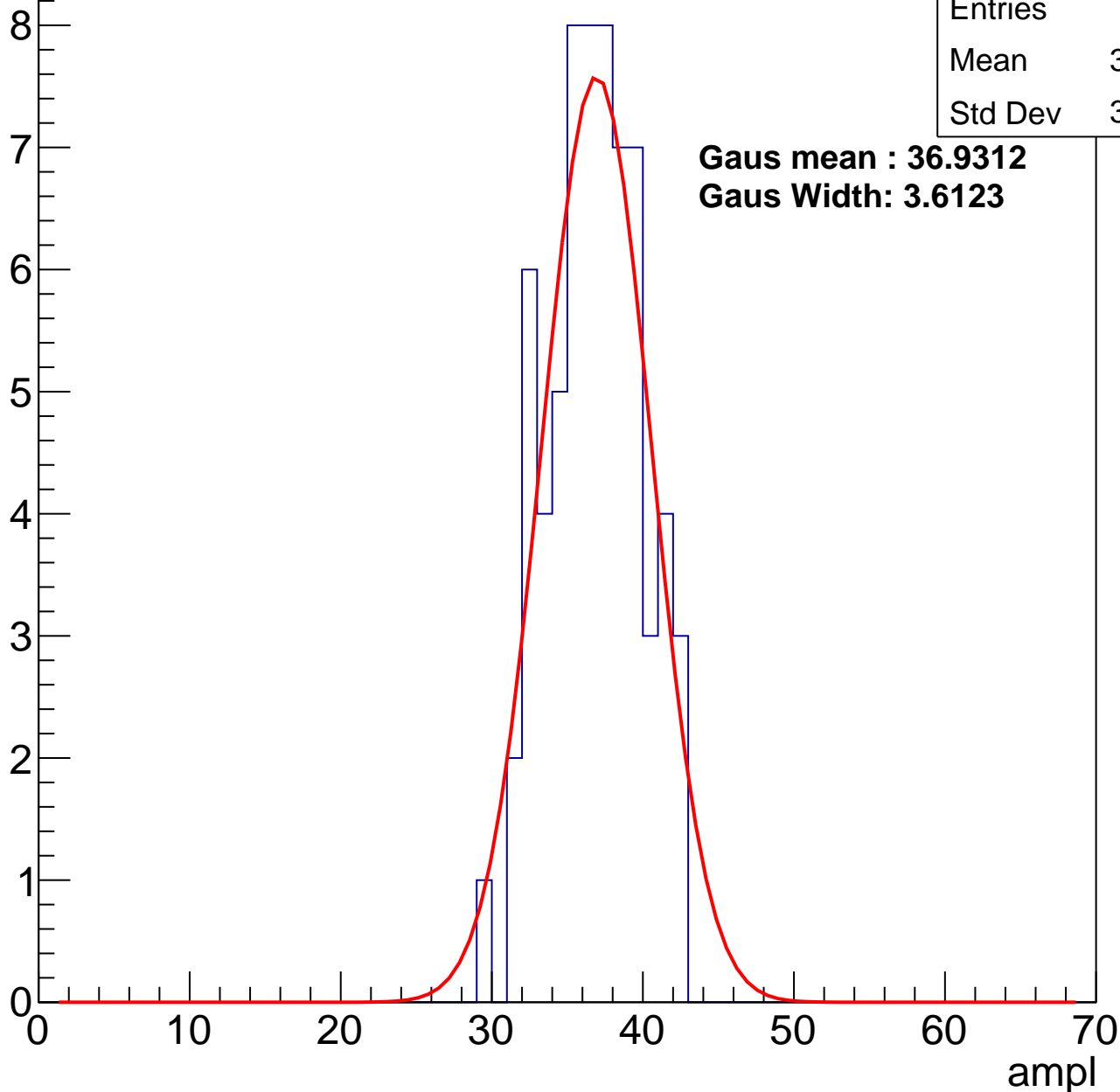
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	36.33
Std Dev	3.032

Gaus mean : 36.9312

Gaus Width: 3.6123



B1L103S, U7-ch31, adc2

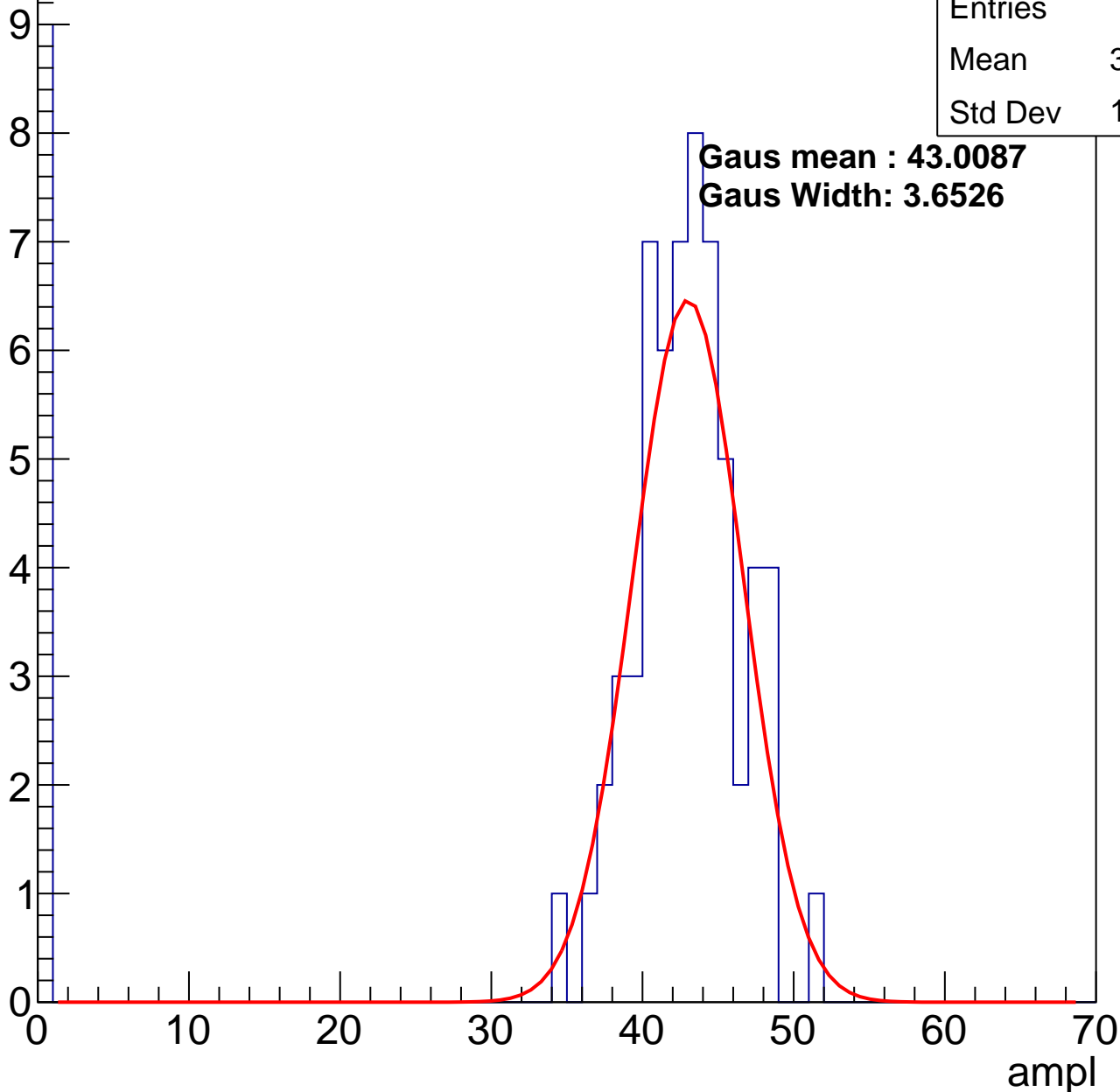
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	37.07
Std Dev	14.58

Gaus mean : 43.0087

Gaus Width: 3.6526

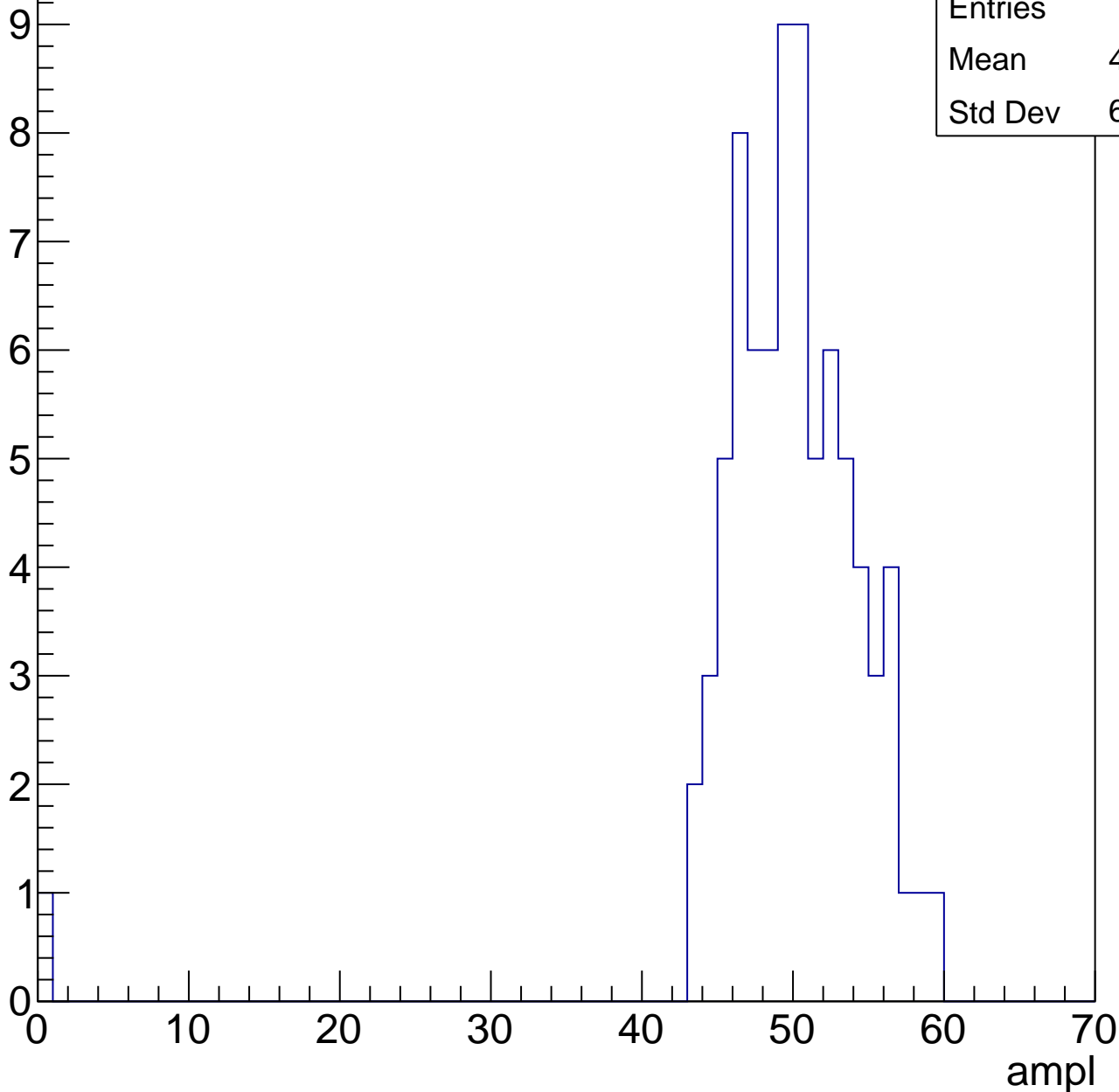


B1L103S, U7-ch31, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	79
Mean	49.15
Std Dev	6.694

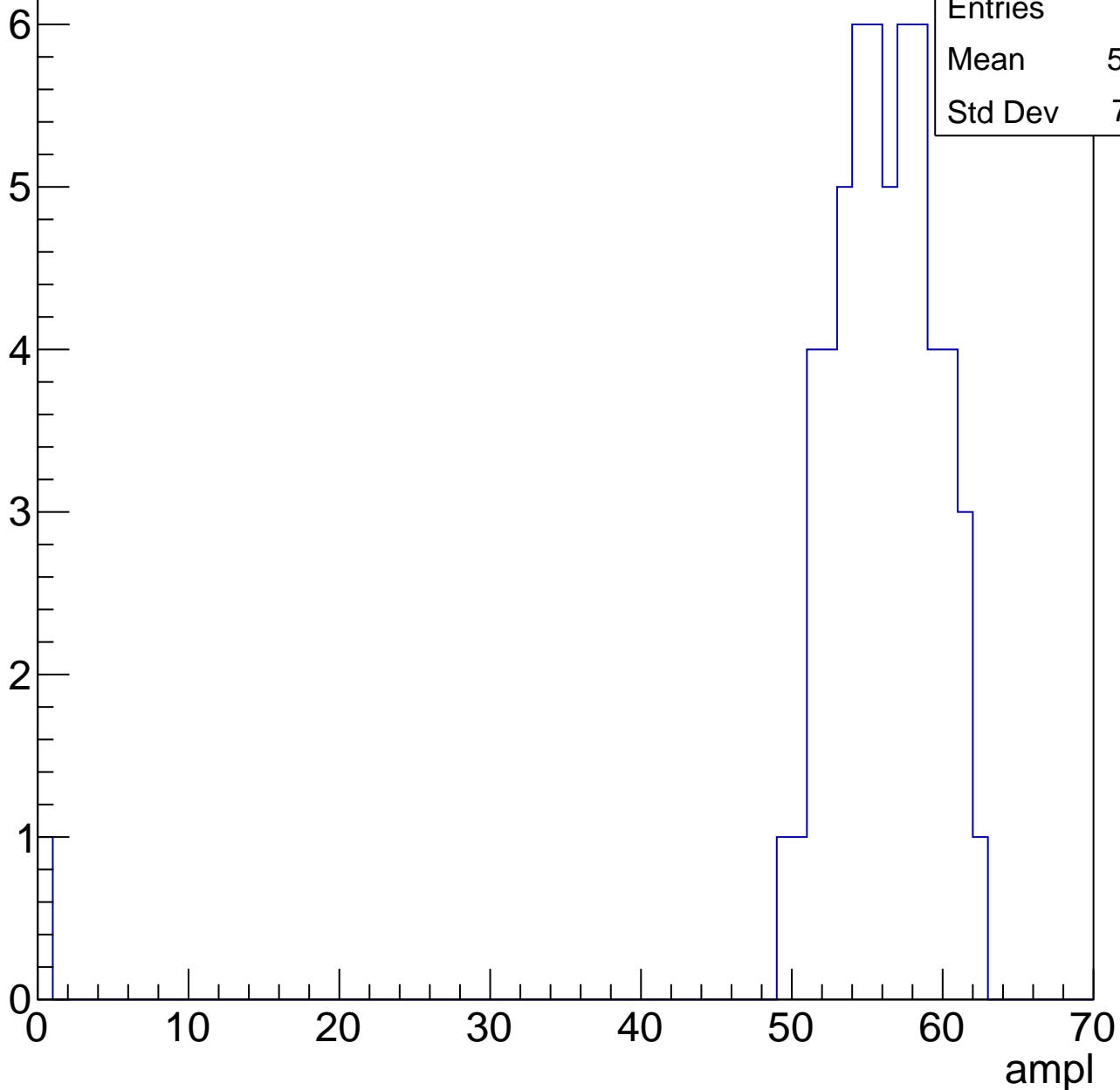


B1L103S, U7-ch31, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	54.75
Std Dev	7.961



B1L103S, U7-ch31, adc5

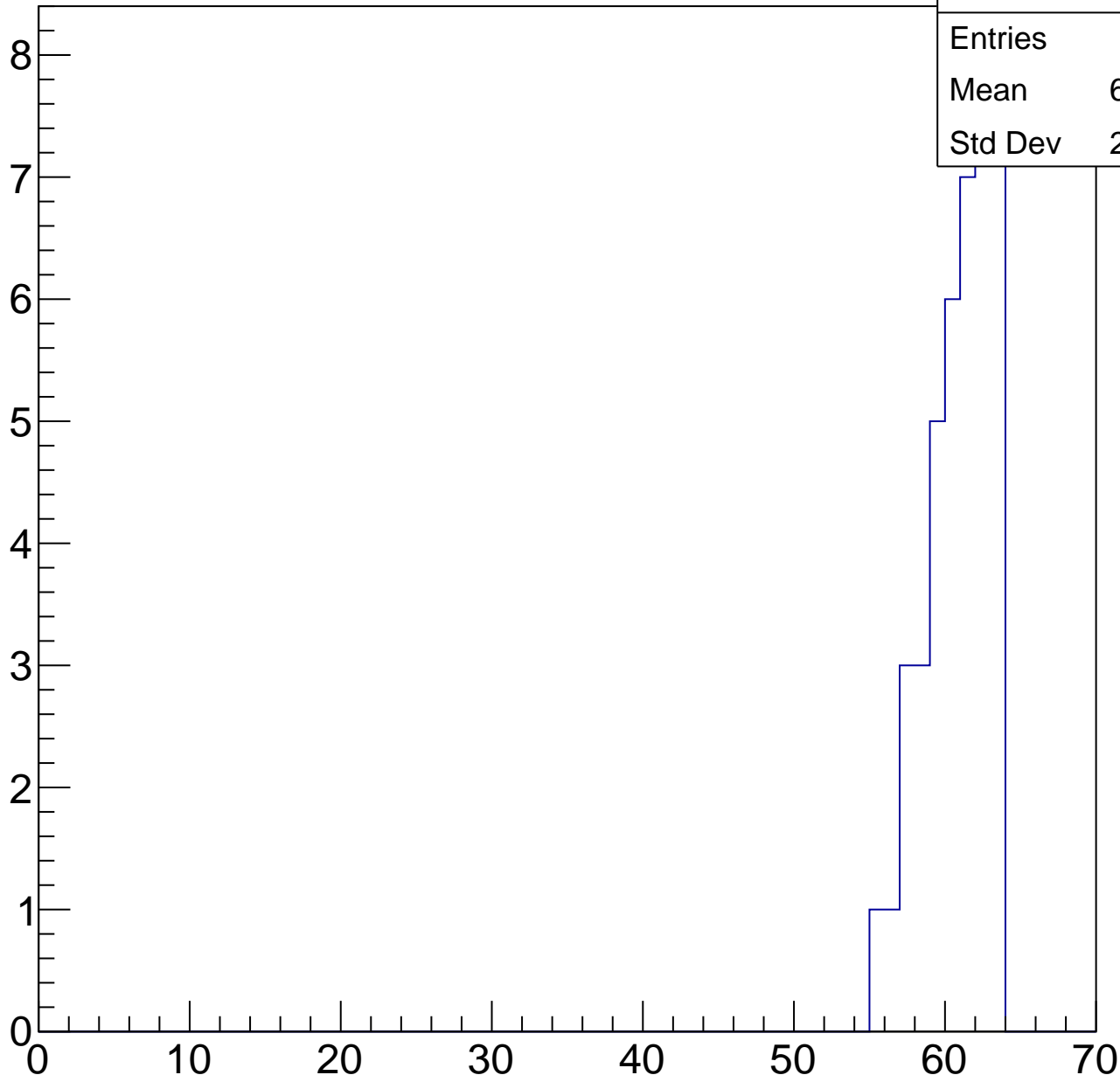
calib_packv5_041523_1651.root, FC#0, port C2

Entry

8
7
6
5
4
3
2
1
0

Entries	42
Mean	60.43
Std Dev	2.117

ampl



B1L103S, U7-ch31, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70

B1L103S, U7-ch31, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U7-ch32, adc0

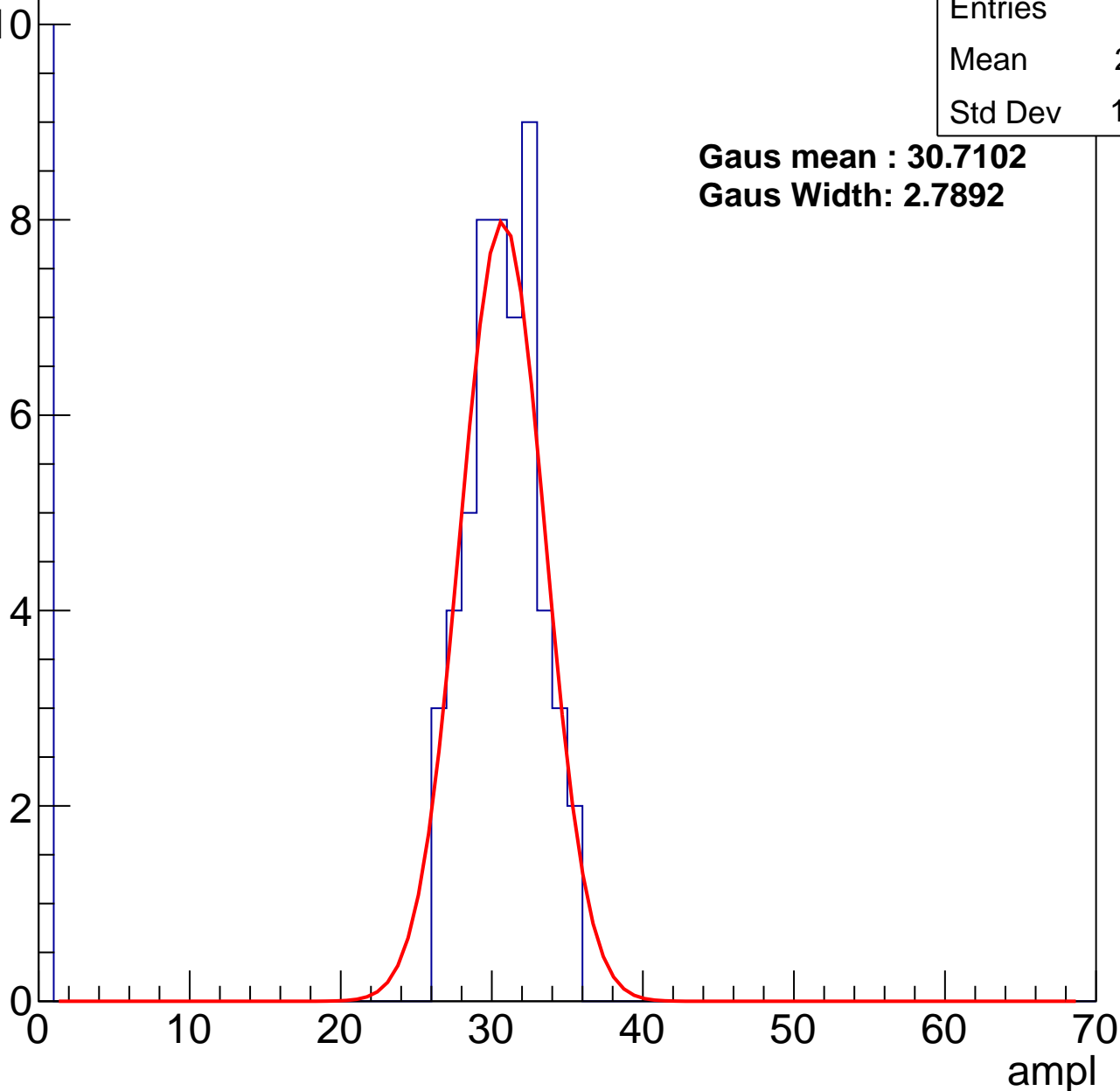
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	25.51
Std Dev	11.28

Gaus mean : 30.7102

Gaus Width: 2.7892



B1L103S, U7-ch32, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	88
Mean	33.94
Std Dev	10.42

Gaus mean : 37.7003

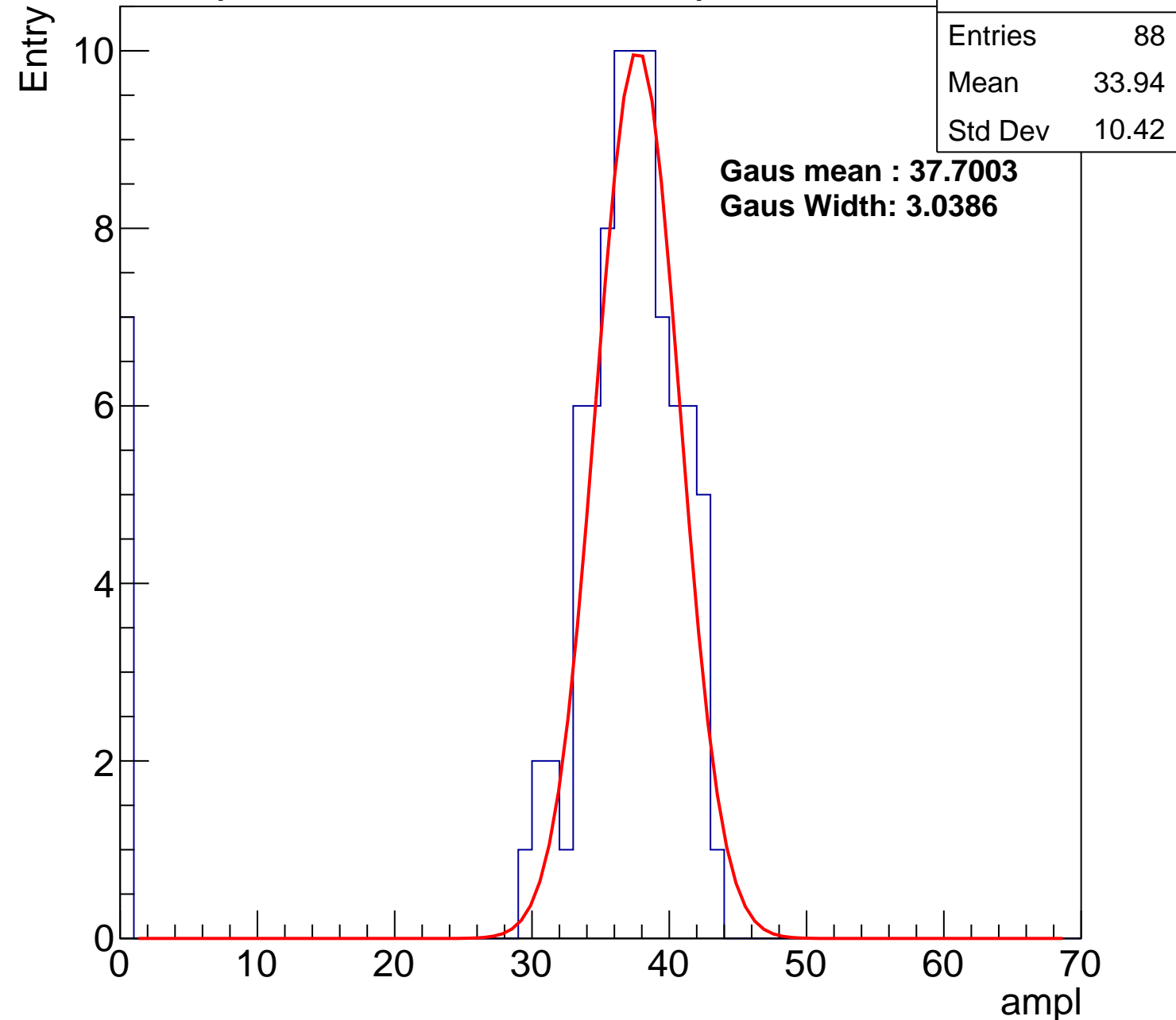
Gaus Width: 3.0386

Entry

10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U7-ch32, adc2

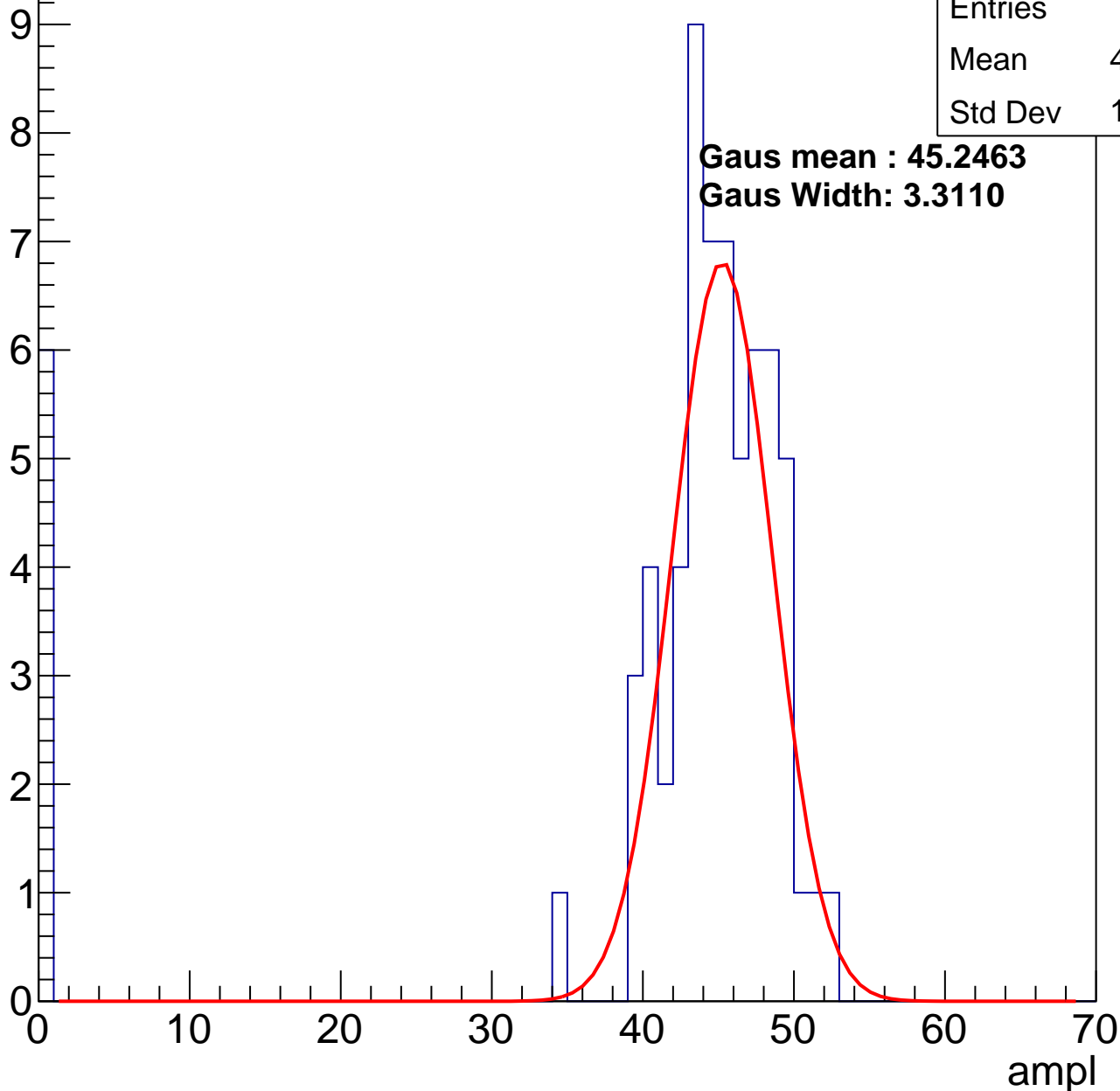
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	40.72
Std Dev	13.07

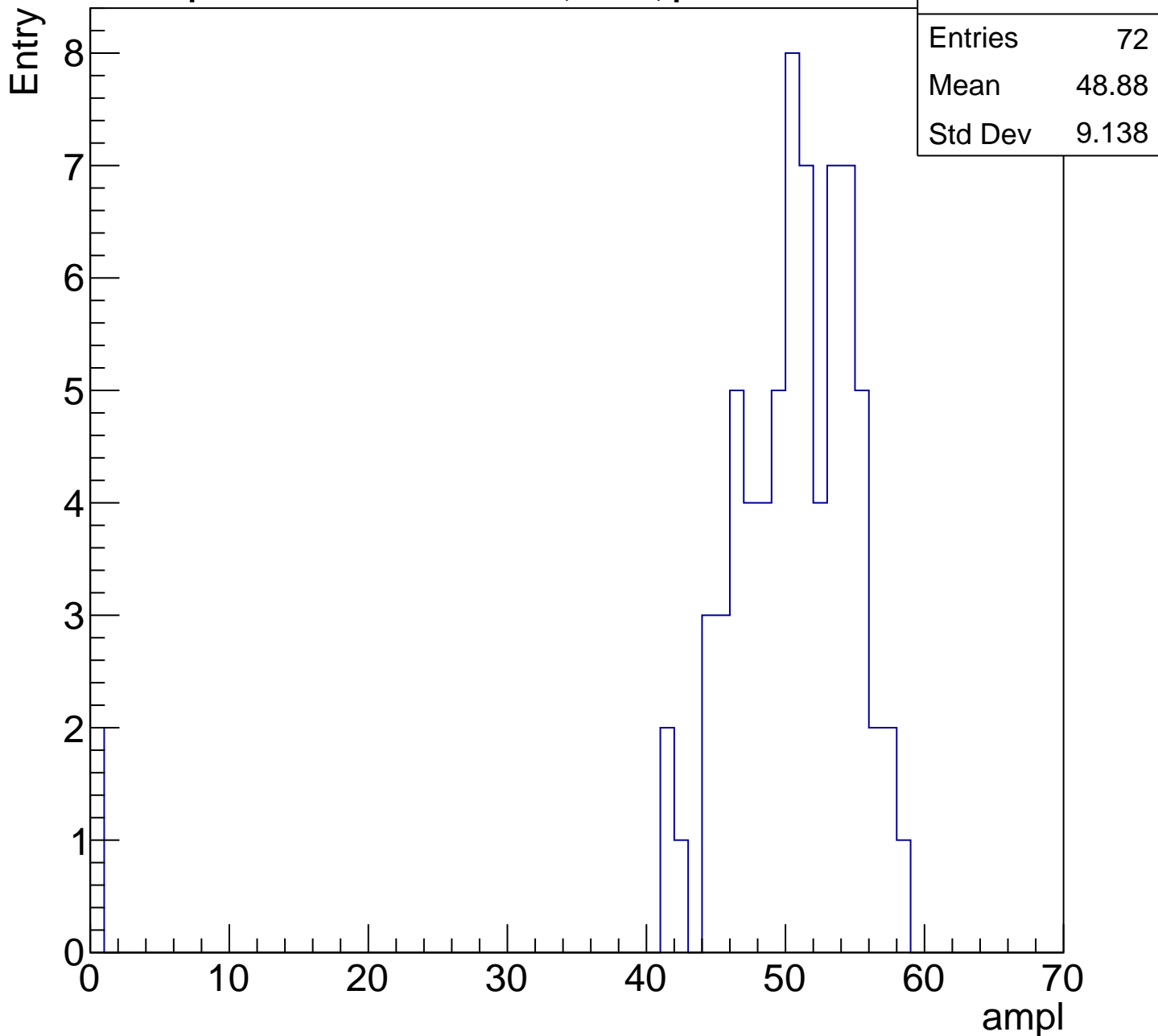
Gaus mean : 45.2463

Gaus Width: 3.3110



B1L103S, U7-ch32, adc3

calib_packv5_041523_1651.root, FC#0, port C2

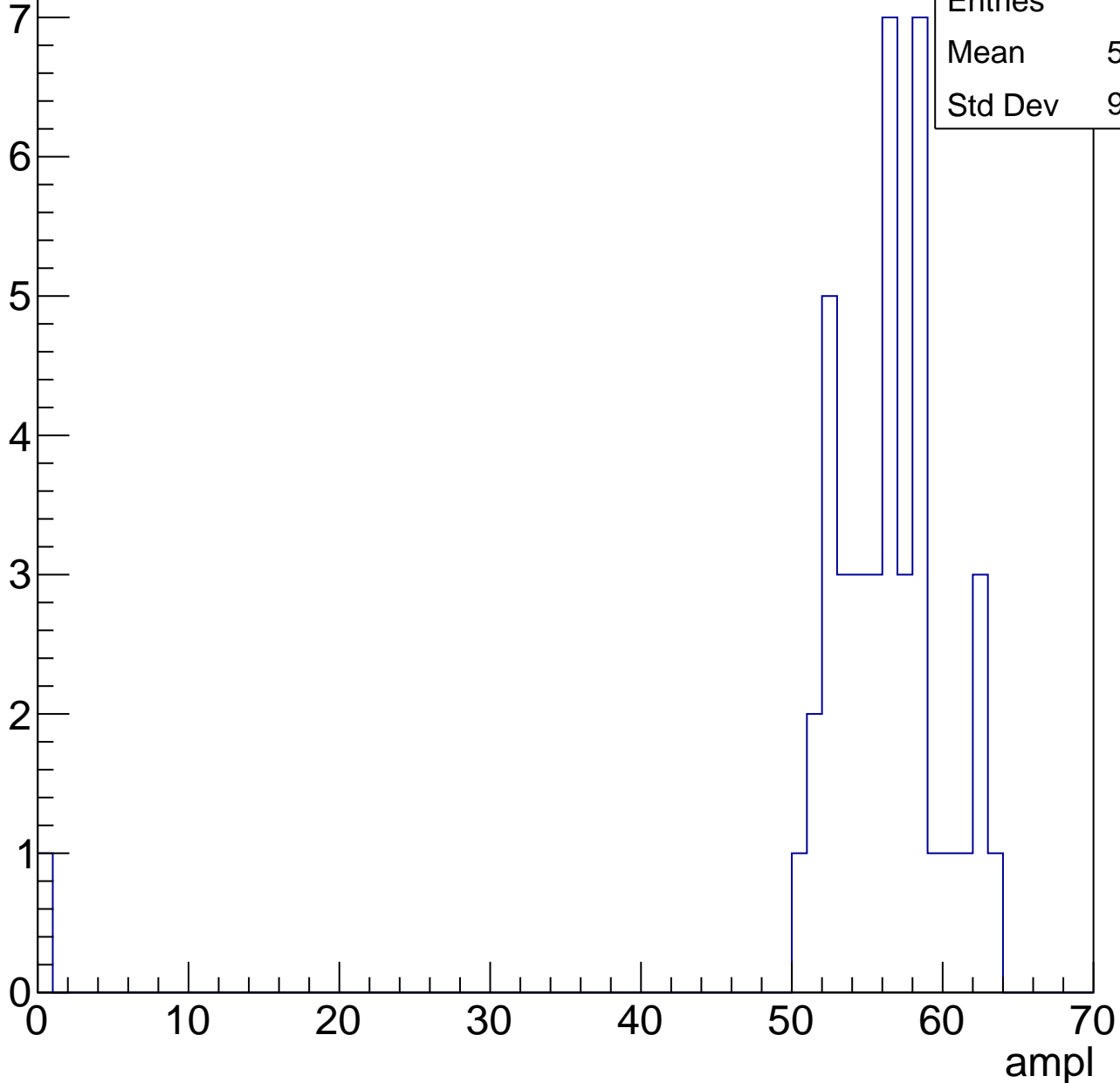


B1L103S, U7-ch32, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	42
Mean	54.67
Std Dev	9.138

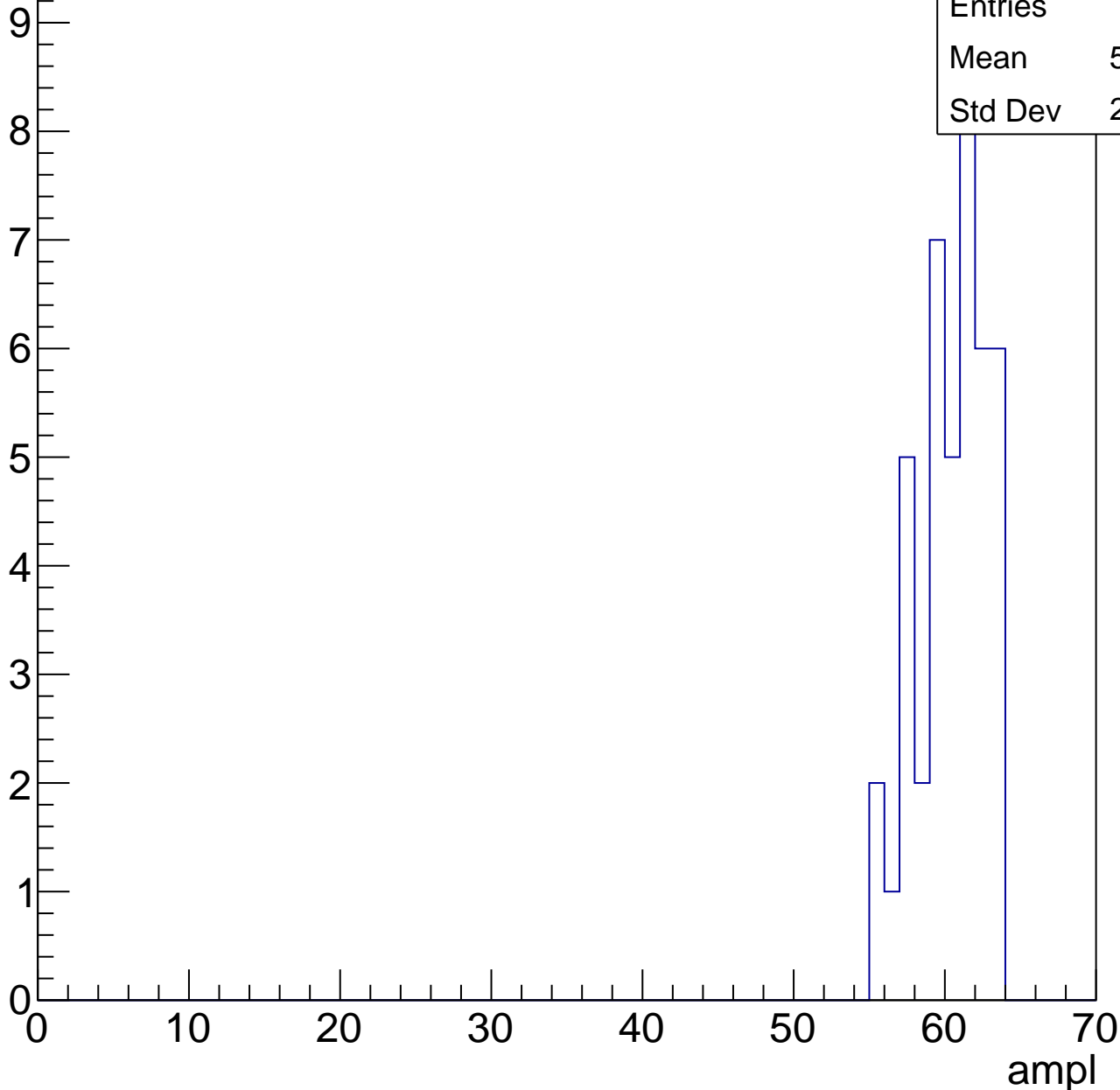


B1L103S, U7-ch32, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

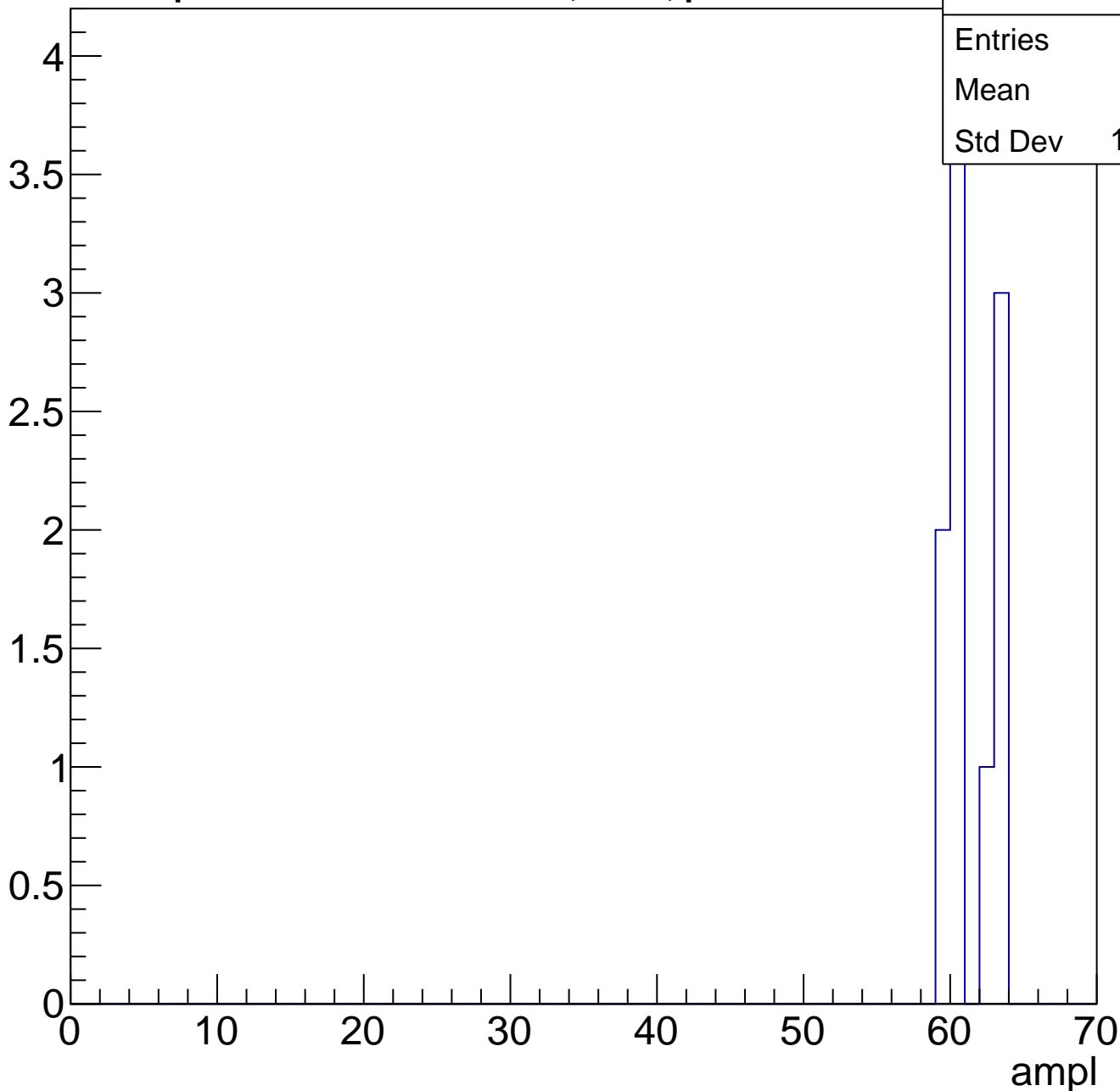
Entries	43
Mean	59.98
Std Dev	2.226



B1L103S, U7-ch32, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



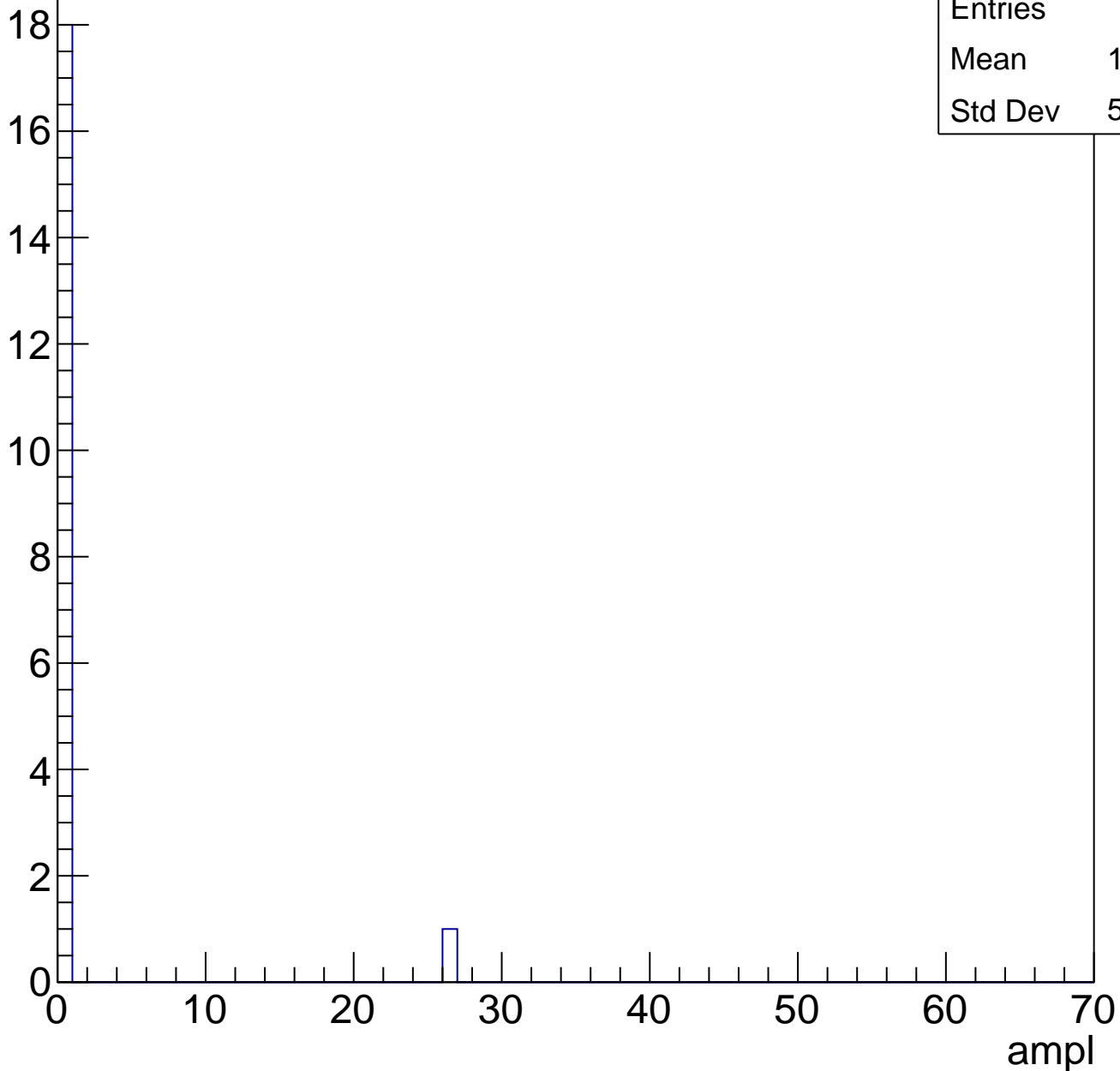
Entries	10
Mean	60.9
Std Dev	1.578

B1L103S, U7-ch32, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.368
Std Dev	5.806

Entry



B1L103S, U7-ch33, adc0

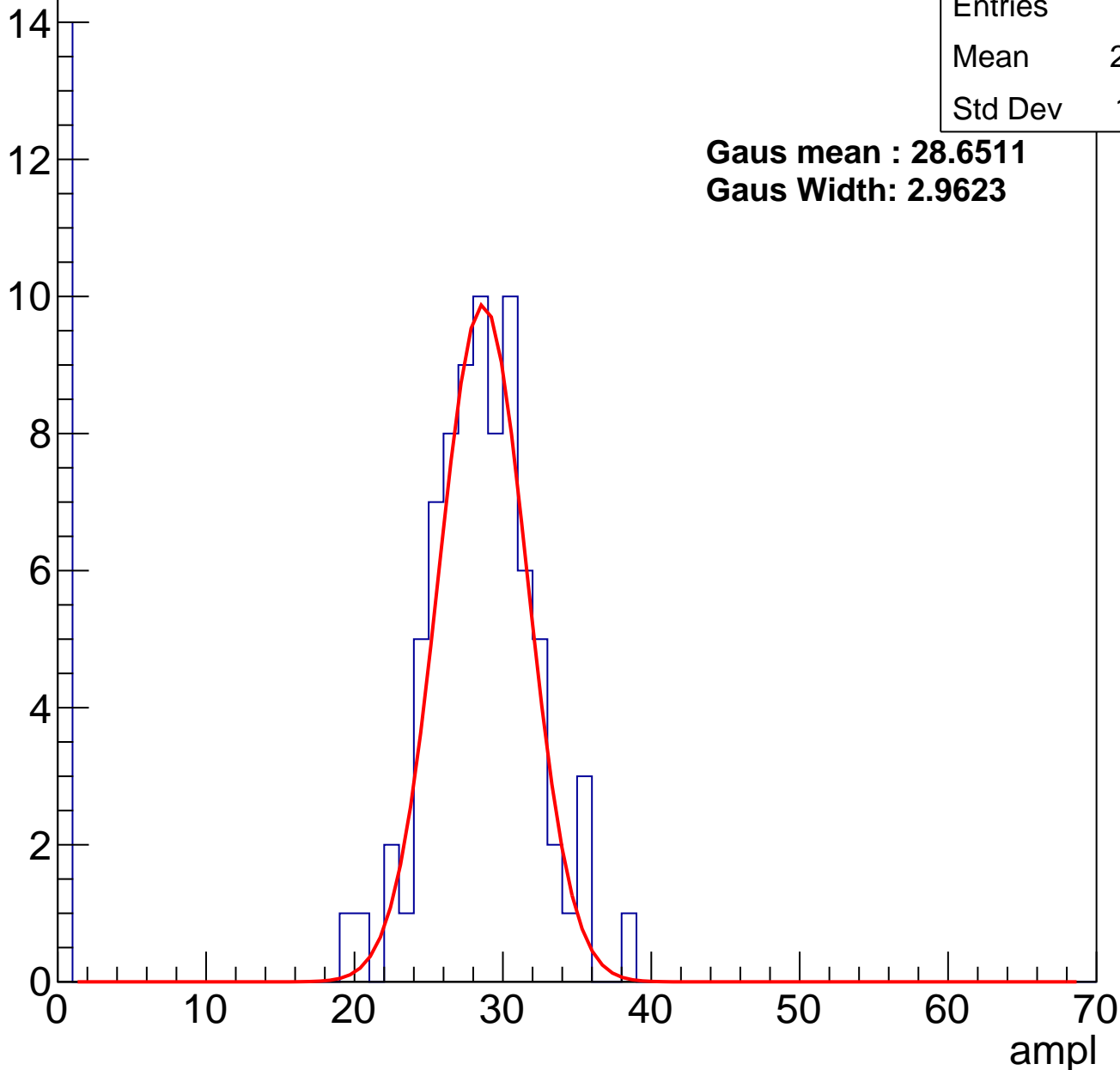
calib_packv5_041523_1651.root, FC#0, port C2

Entries	94
Mean	23.97
Std Dev	10.51

Gaus mean : 28.6511

Gaus Width: 2.9623

Entry



B1L103S, U7-ch33, adc1

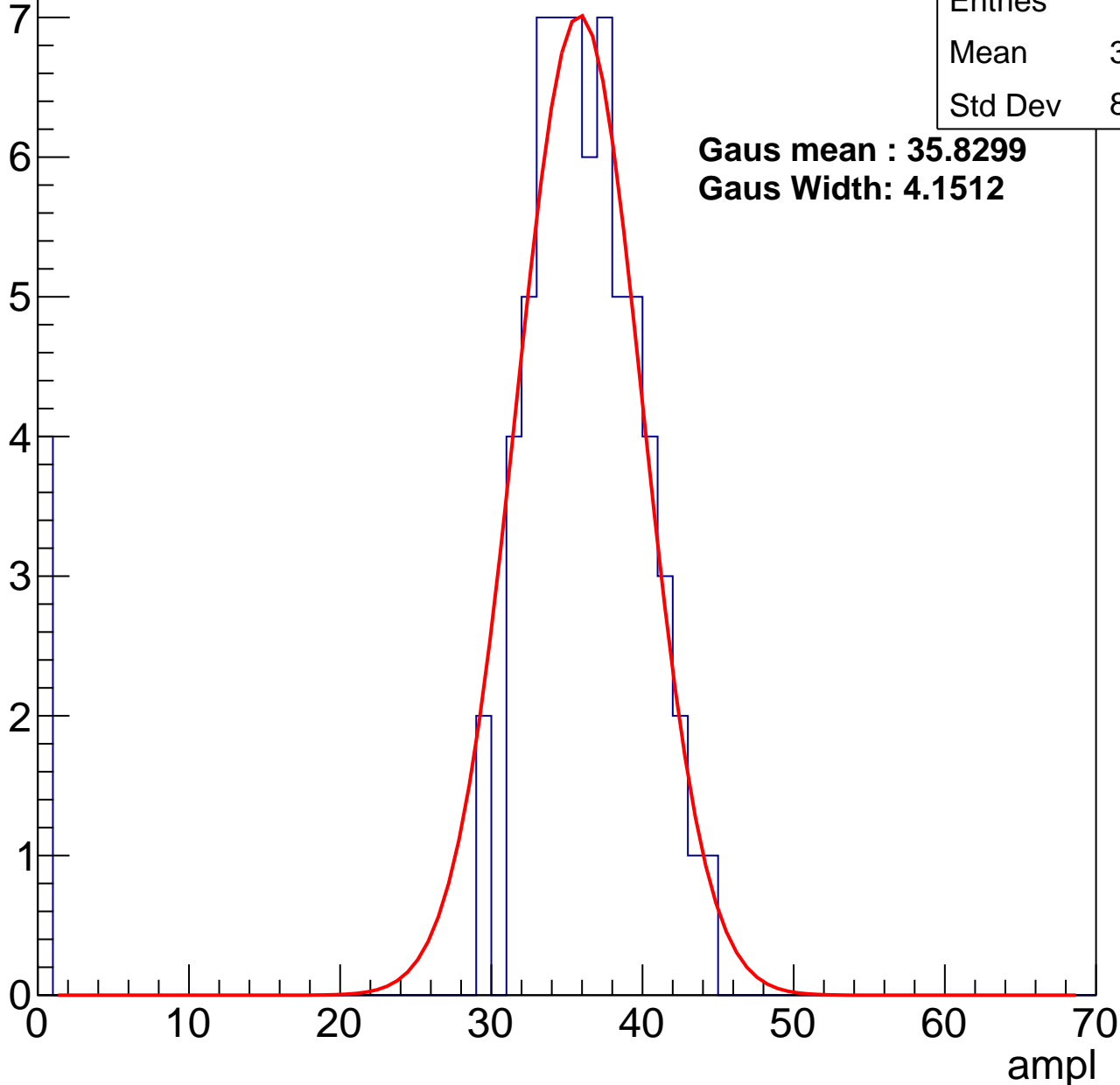
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	33.86
Std Dev	8.972

Gaus mean : 35.8299

Gaus Width: 4.1512



B1L103S, U7-ch33, adc2

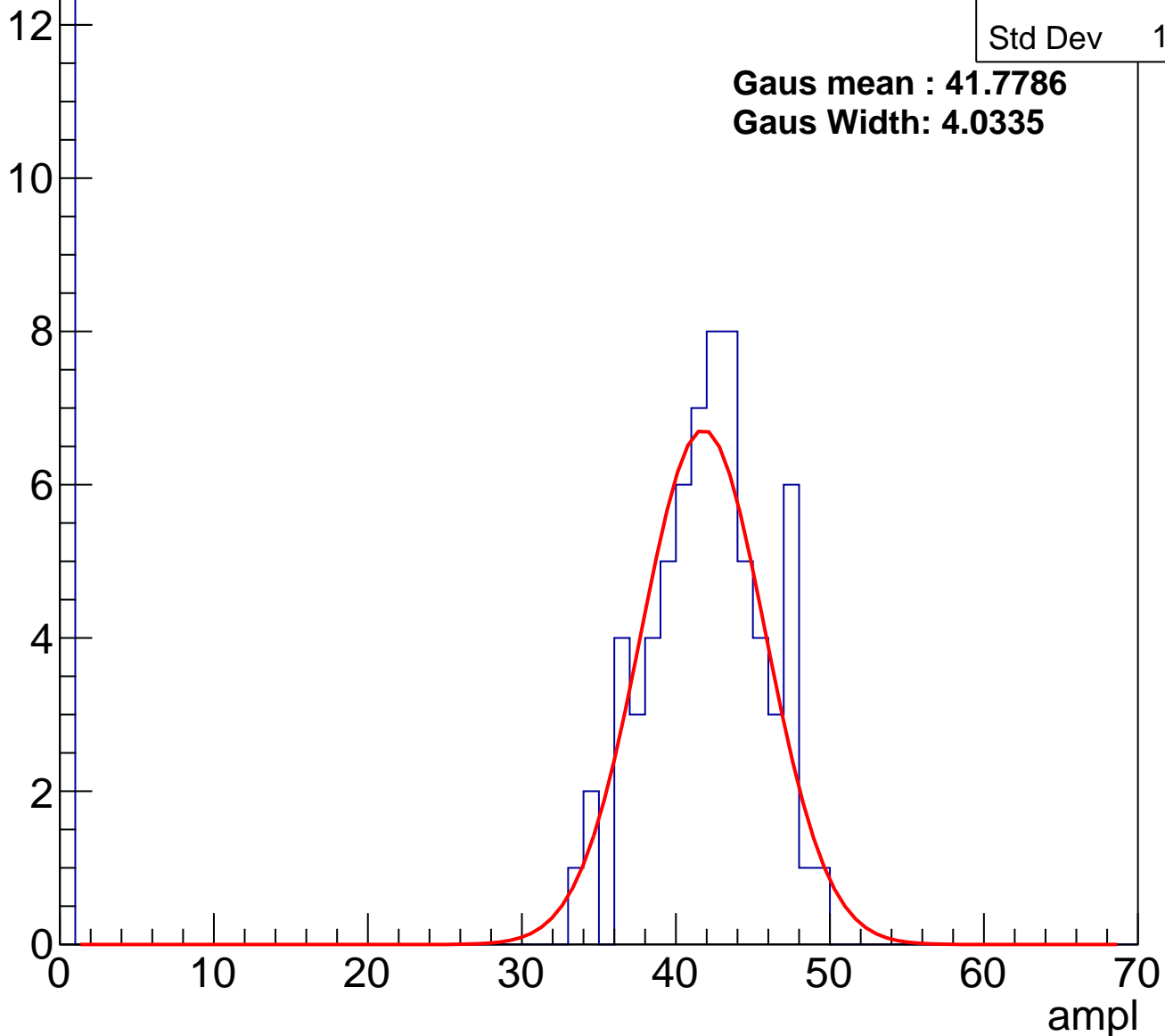
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	81
Mean	34.9
Std Dev	15.62

Gaus mean : 41.7786

Gaus Width: 4.0335

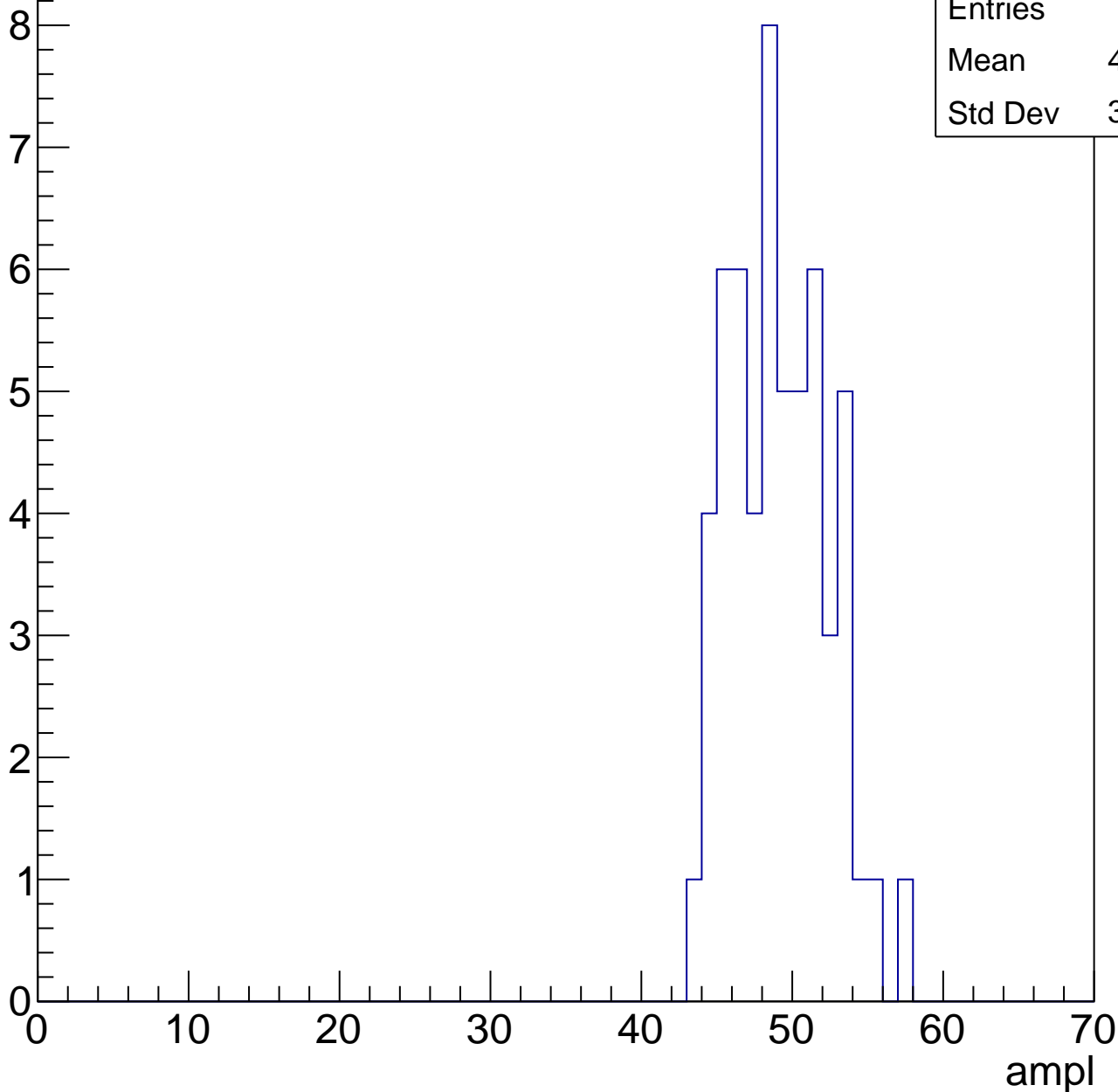


B1L103S, U7-ch33, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	48.66
Std Dev	3.175

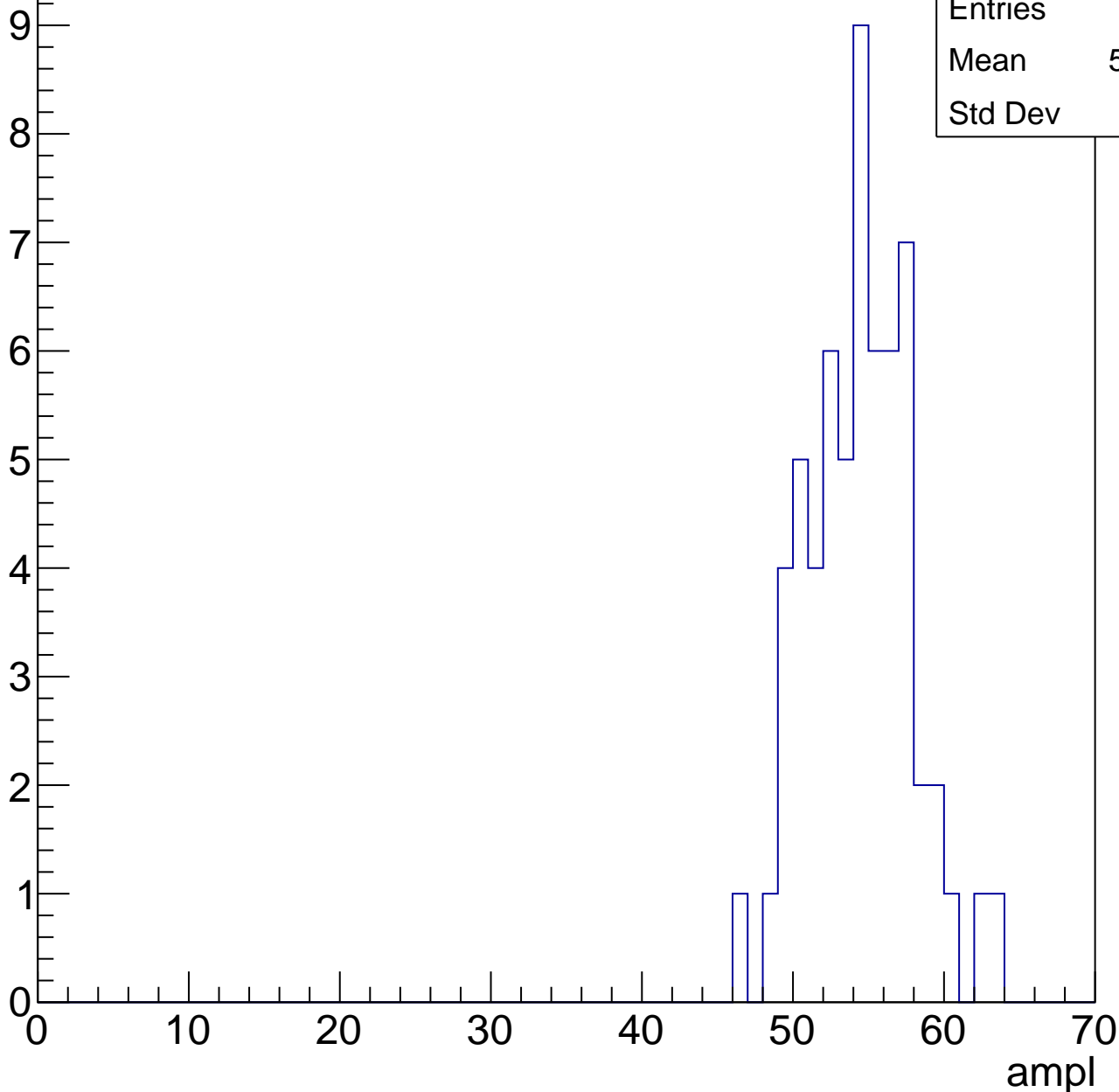


B1L103S, U7-ch33, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	53.95
Std Dev	3.39

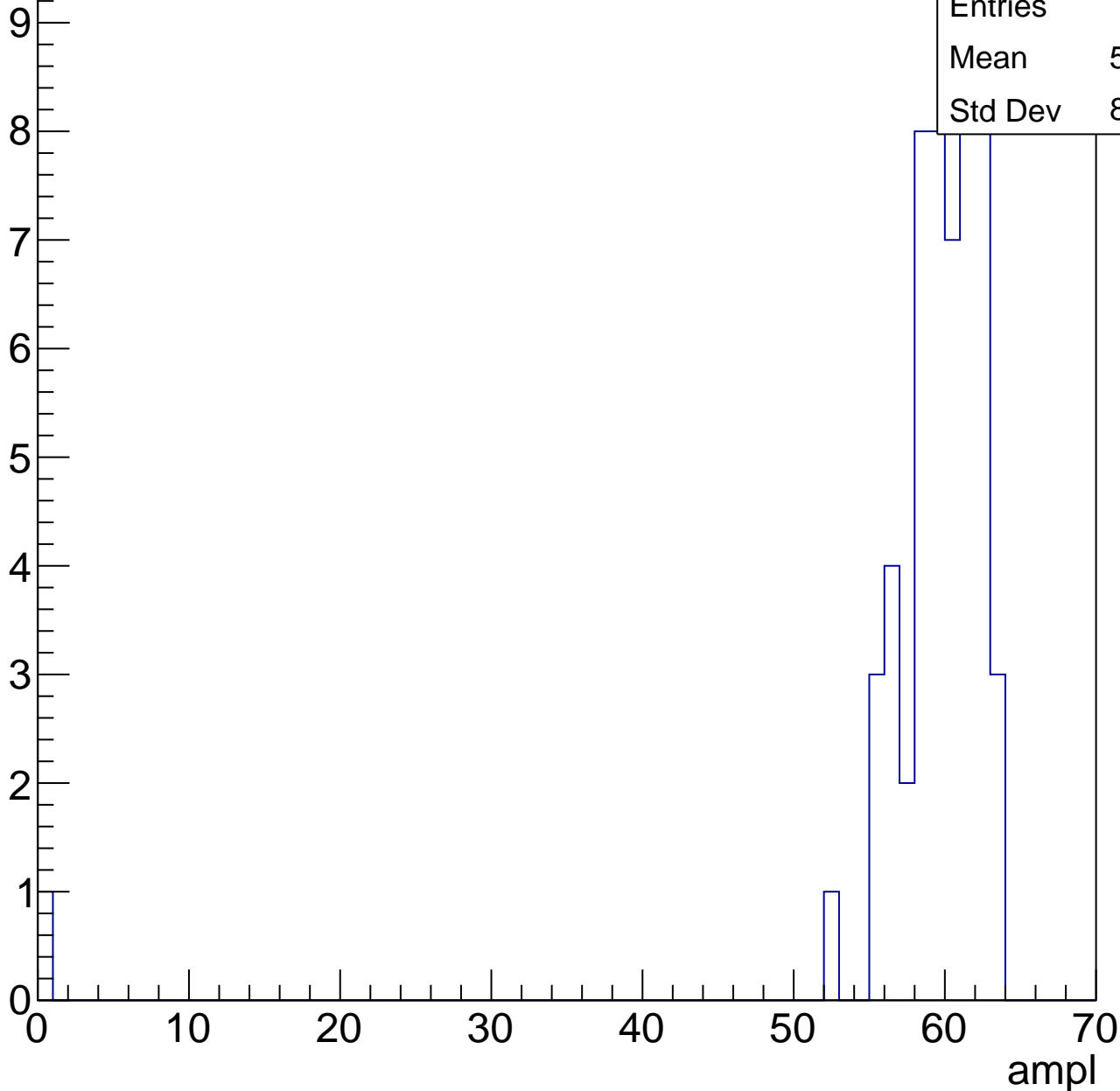


B1L103S, U7-ch33, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	58.24
Std Dev	8.347

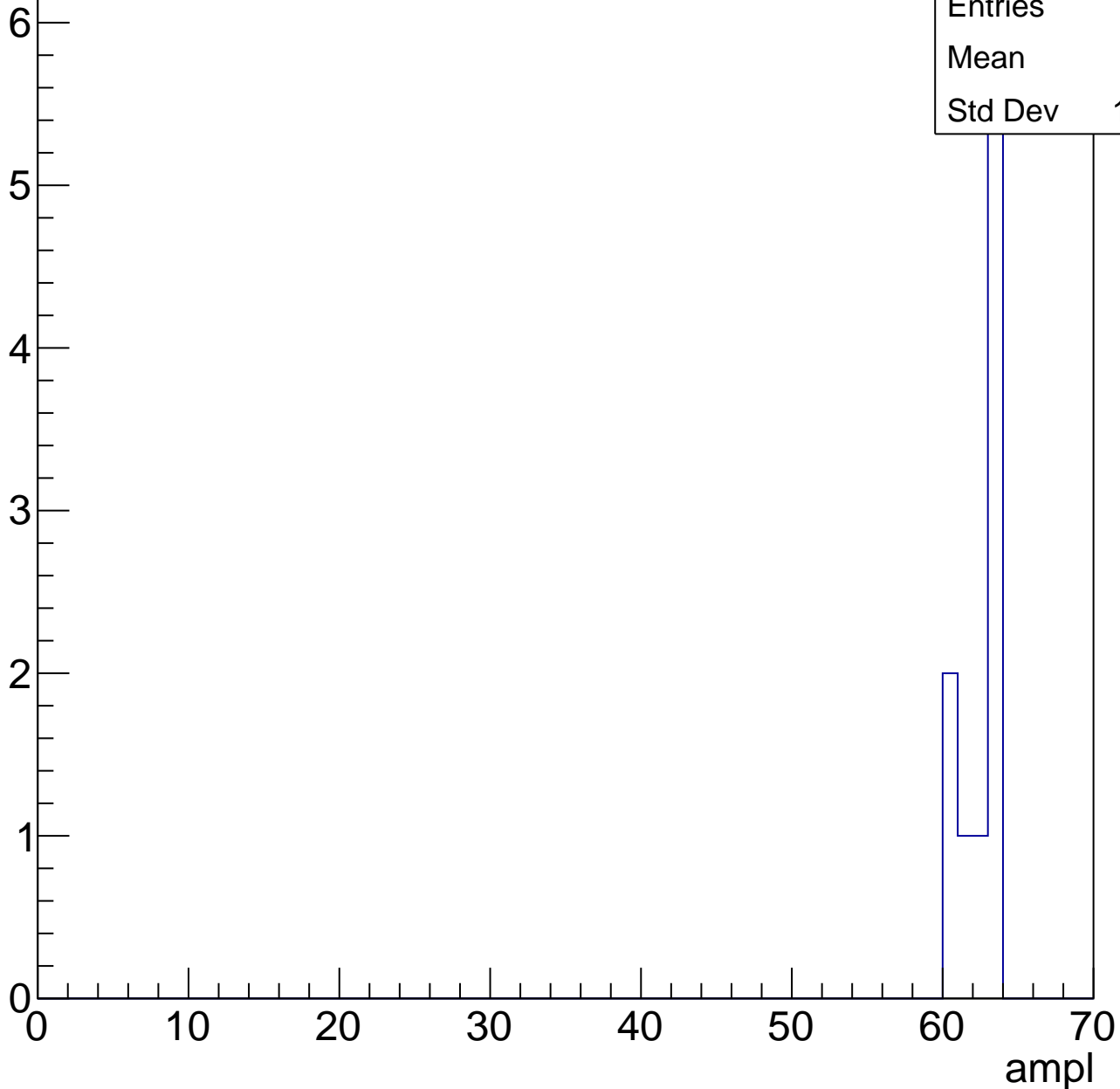


B1L103S, U7-ch33, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	10
Mean	62.1
Std Dev	1.221



B1L103S, U7-ch33, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U7-ch34, adc0

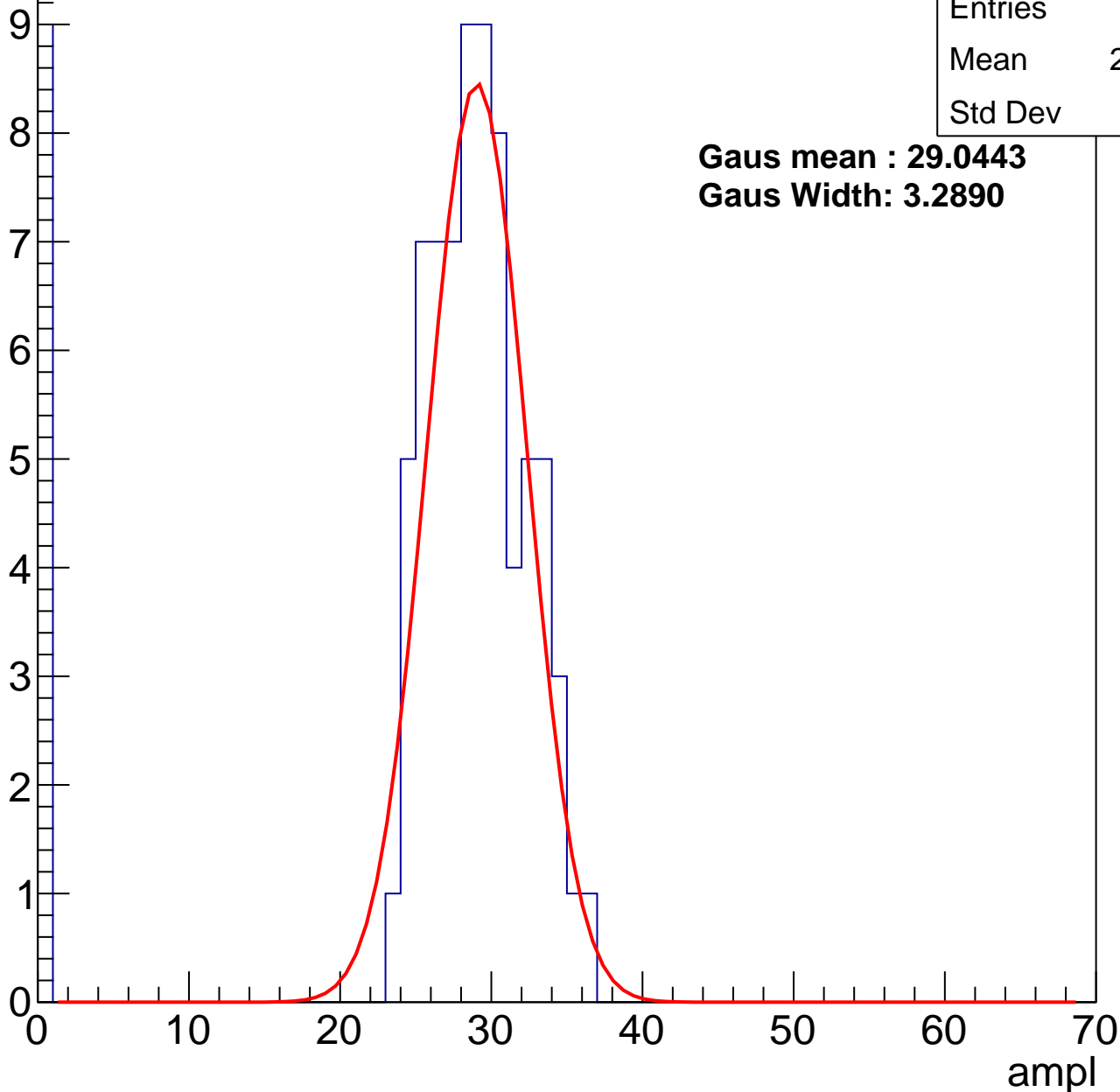
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	81
Mean	25.48
Std Dev	9.46

Gaus mean : 29.0443

Gaus Width: 3.2890



B1L103S, U7-ch34, adc1

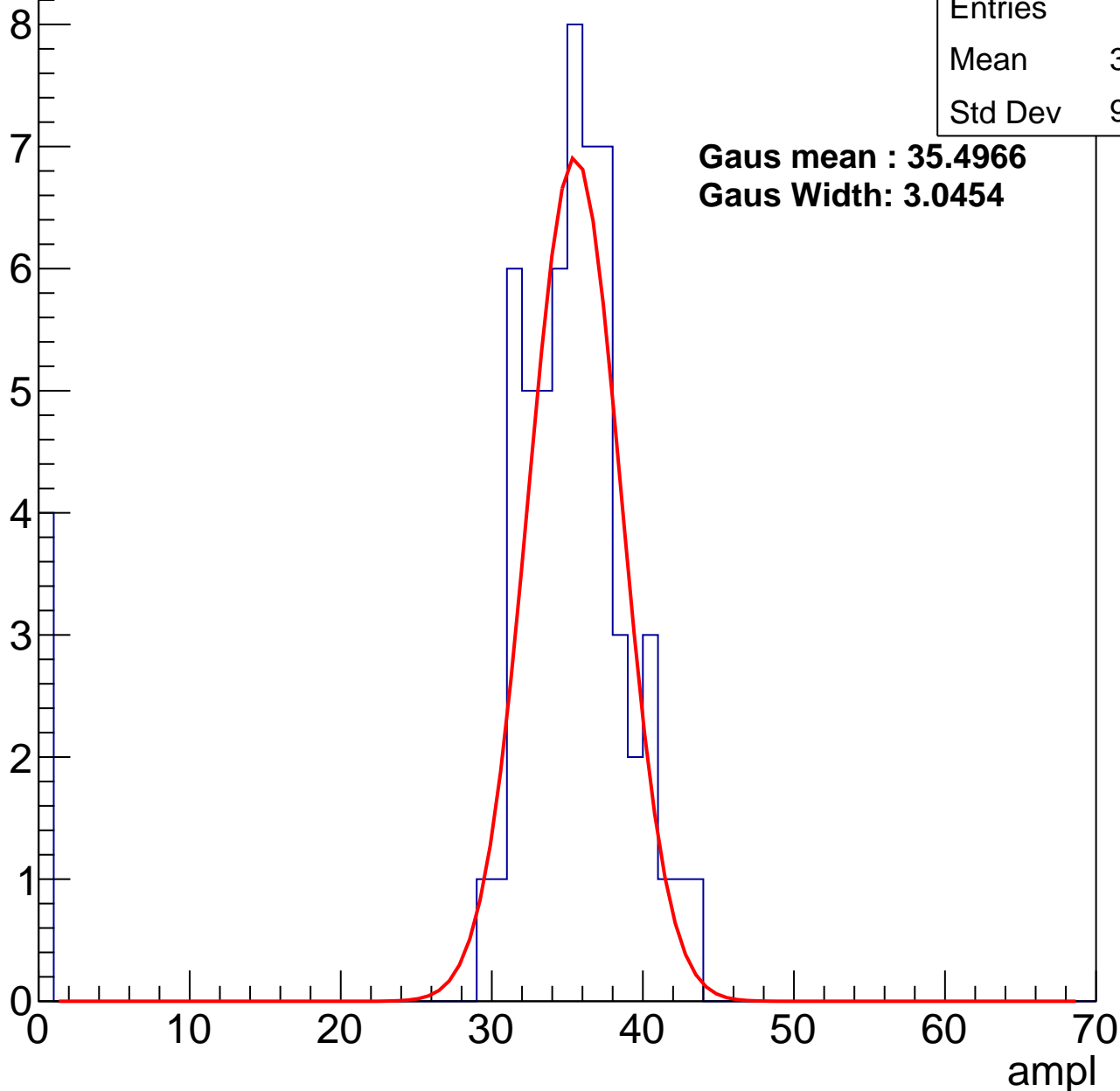
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	32.84
Std Dev	9.198

Gaus mean : 35.4966

Gaus Width: 3.0454



B1L103S, U7-ch34, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	85
Mean	36.66
Std Dev	13.72

Gaus mean : 42.0298

Gaus Width: 3.3782

Entry

10

8

6

4

2

0

0

10

20

30

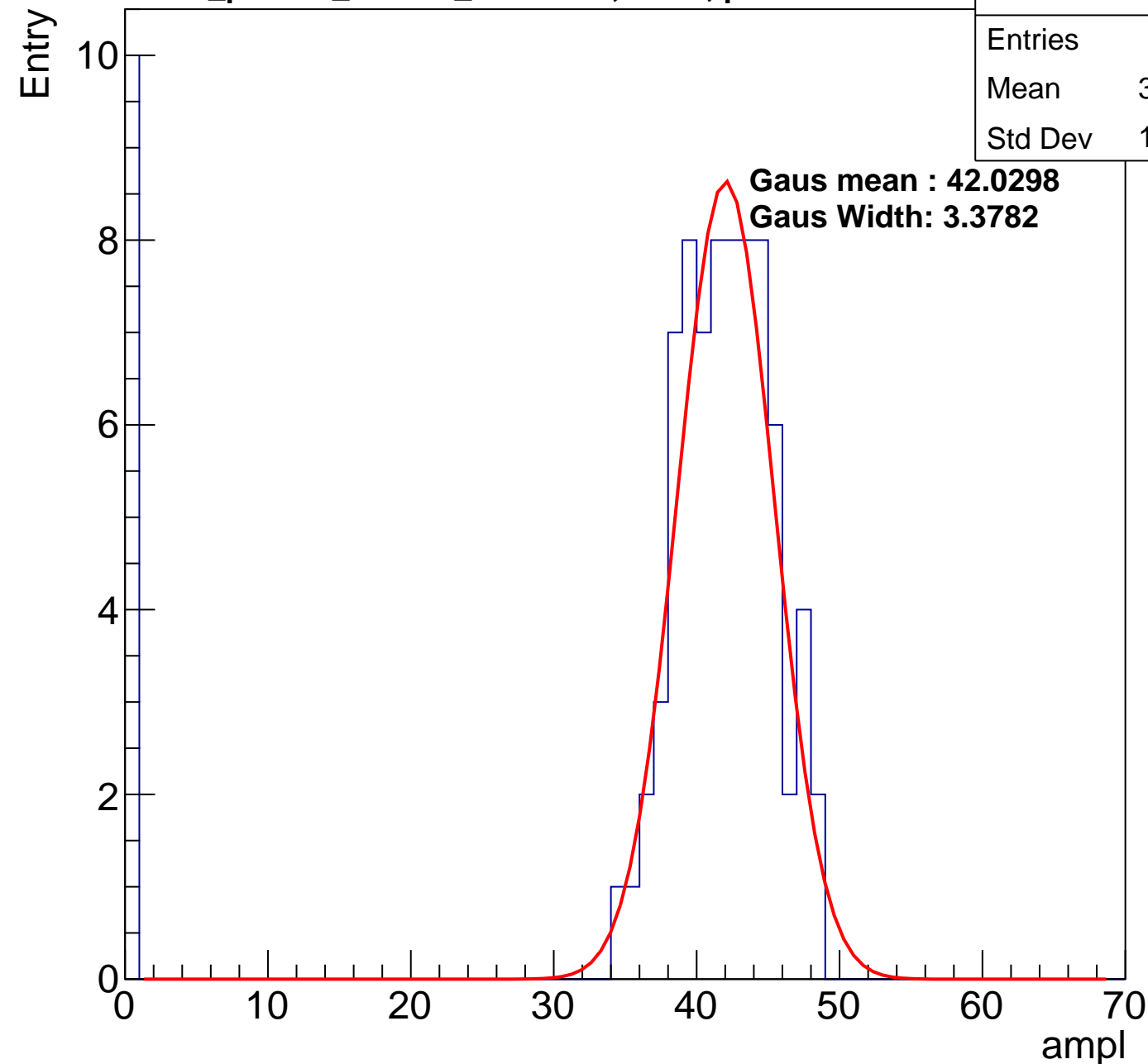
40

50

60

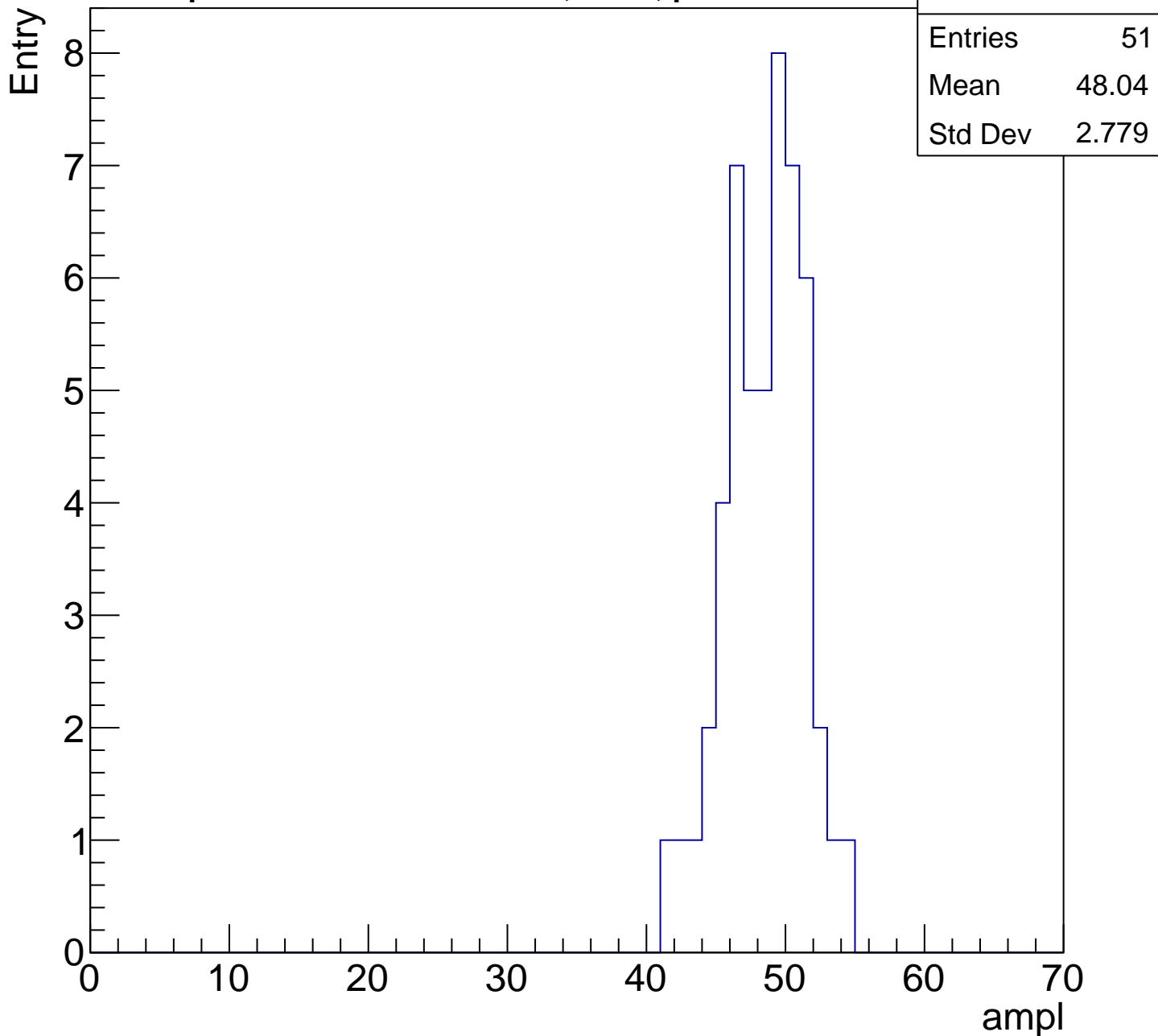
70

ampl



B1L103S, U7-ch34, adc3

calib_packv5_041523_1651.root, FC#0, port C2

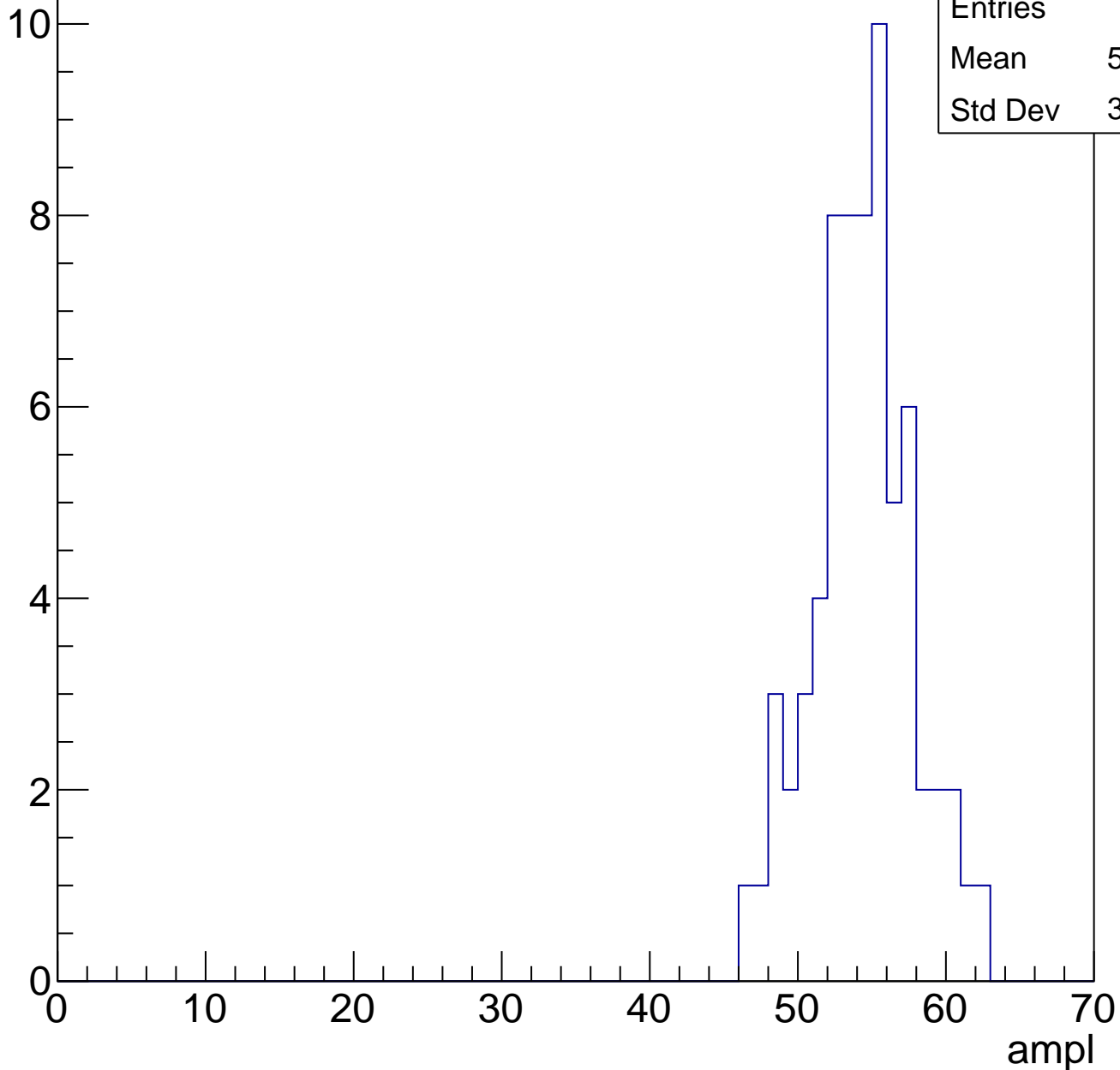


B1L103S, U7-ch34, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	67
Mean	53.88
Std Dev	3.335

Entry



B1L103S, U7-ch34, adc5

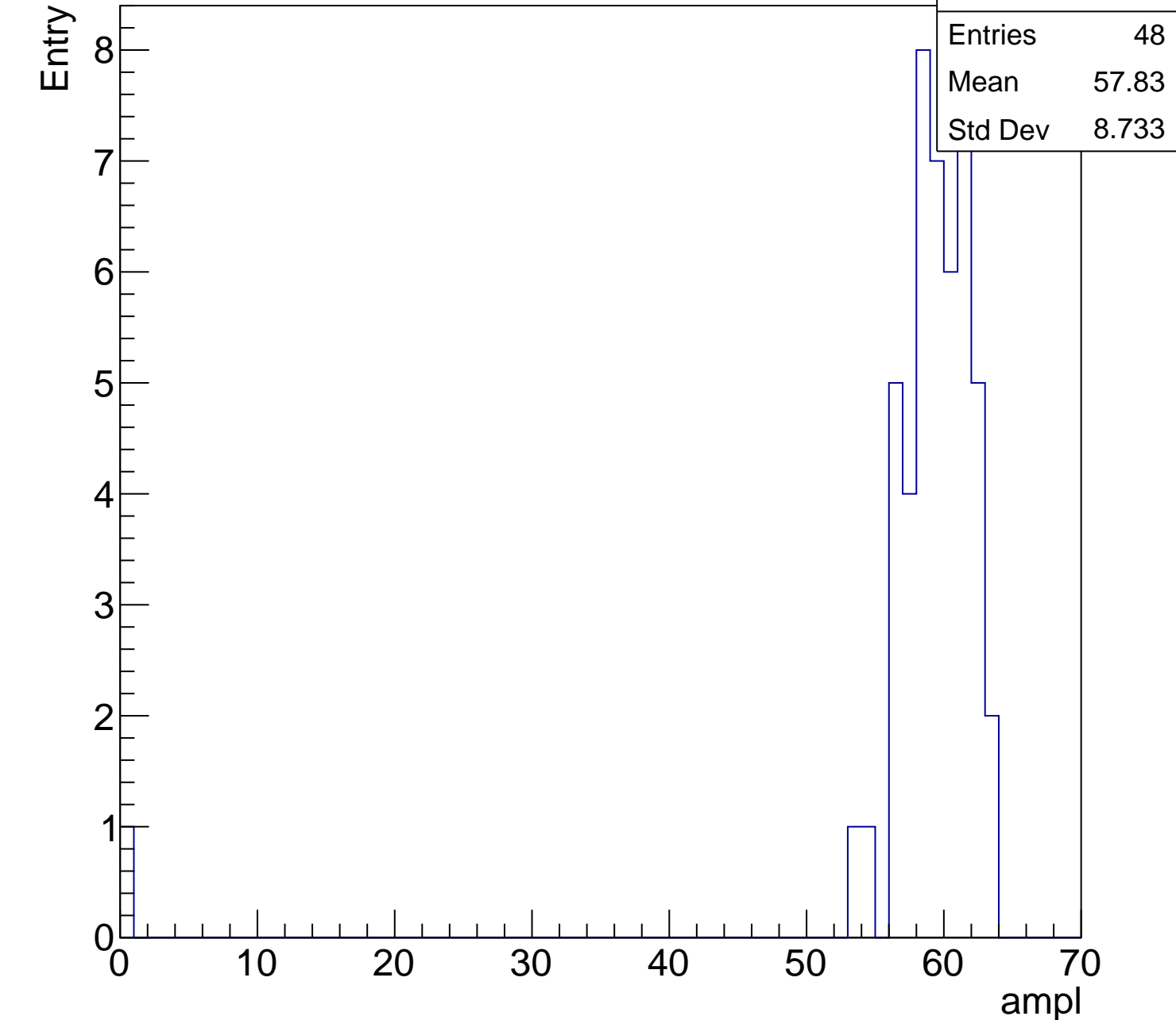
calib_packv5_041523_1651.root, FC#0, port C2

Entry

8
7
6
5
4
3
2
1
0

Entries	48
Mean	57.83
Std Dev	8.733

ampl

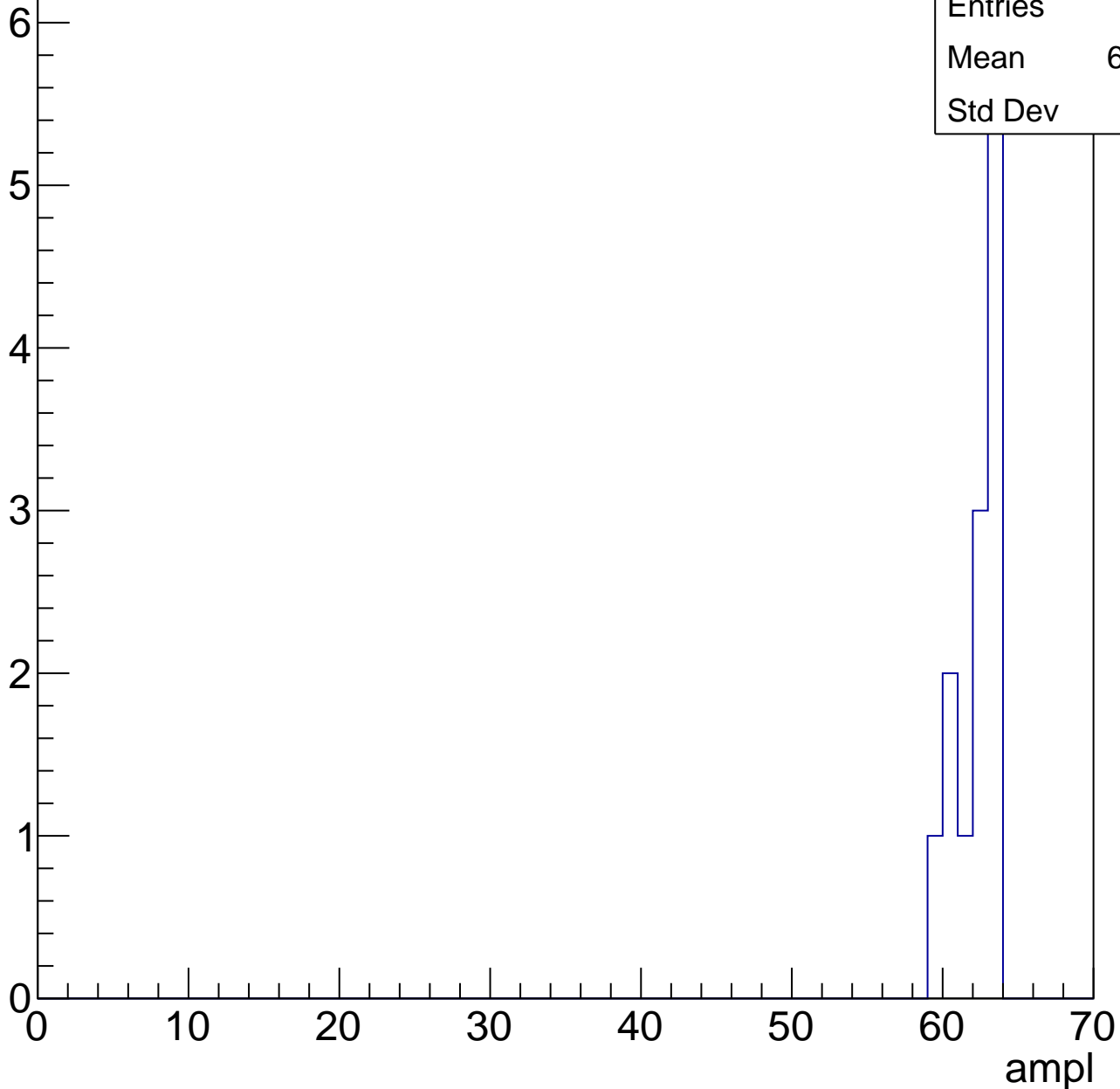


B1L103S, U7-ch34, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	13
Mean	61.85
Std Dev	1.35



B1L103S, U7-ch34, adc7

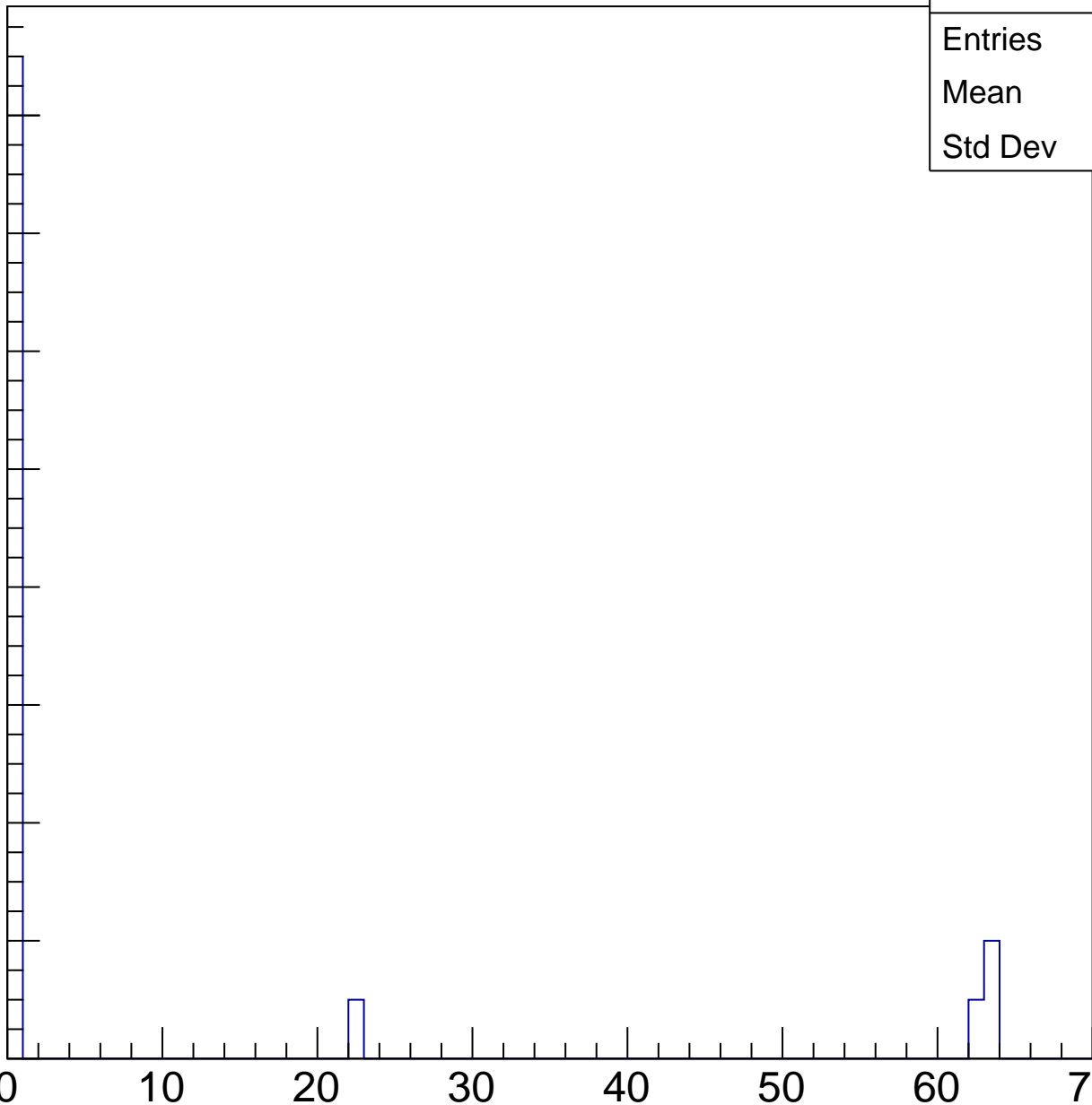
calib_packv5_041523_1651.root, FC#0, port C2

Entry

16
14
12
10
8
6
4
2
0

Entries	21
Mean	10
Std Dev	22

ampl



B1L103S, U7-ch35, adc0

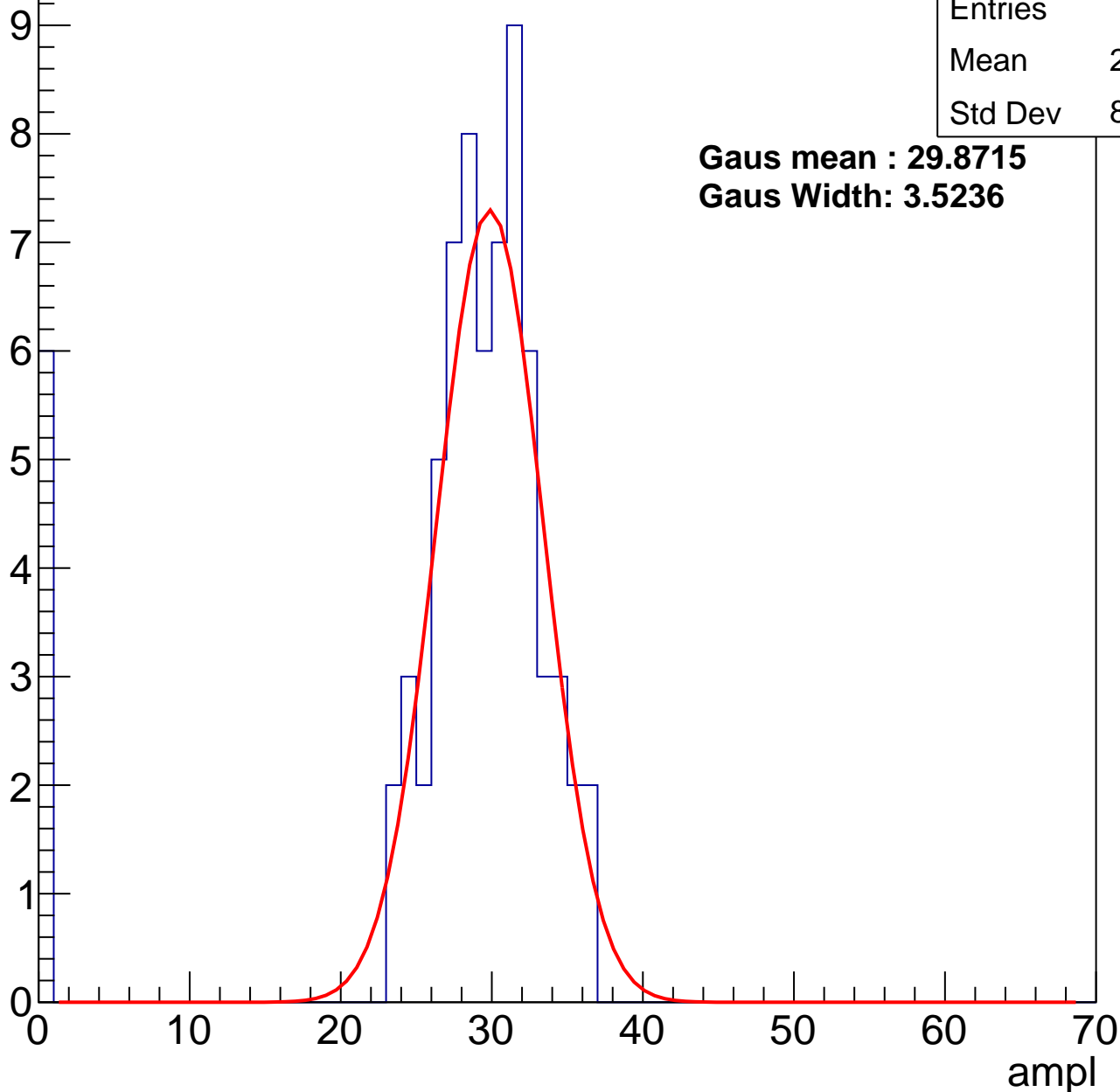
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	26.89
Std Dev	8.704

Gaus mean : 29.8715

Gaus Width: 3.5236



B1L103S, U7-ch35, adc1

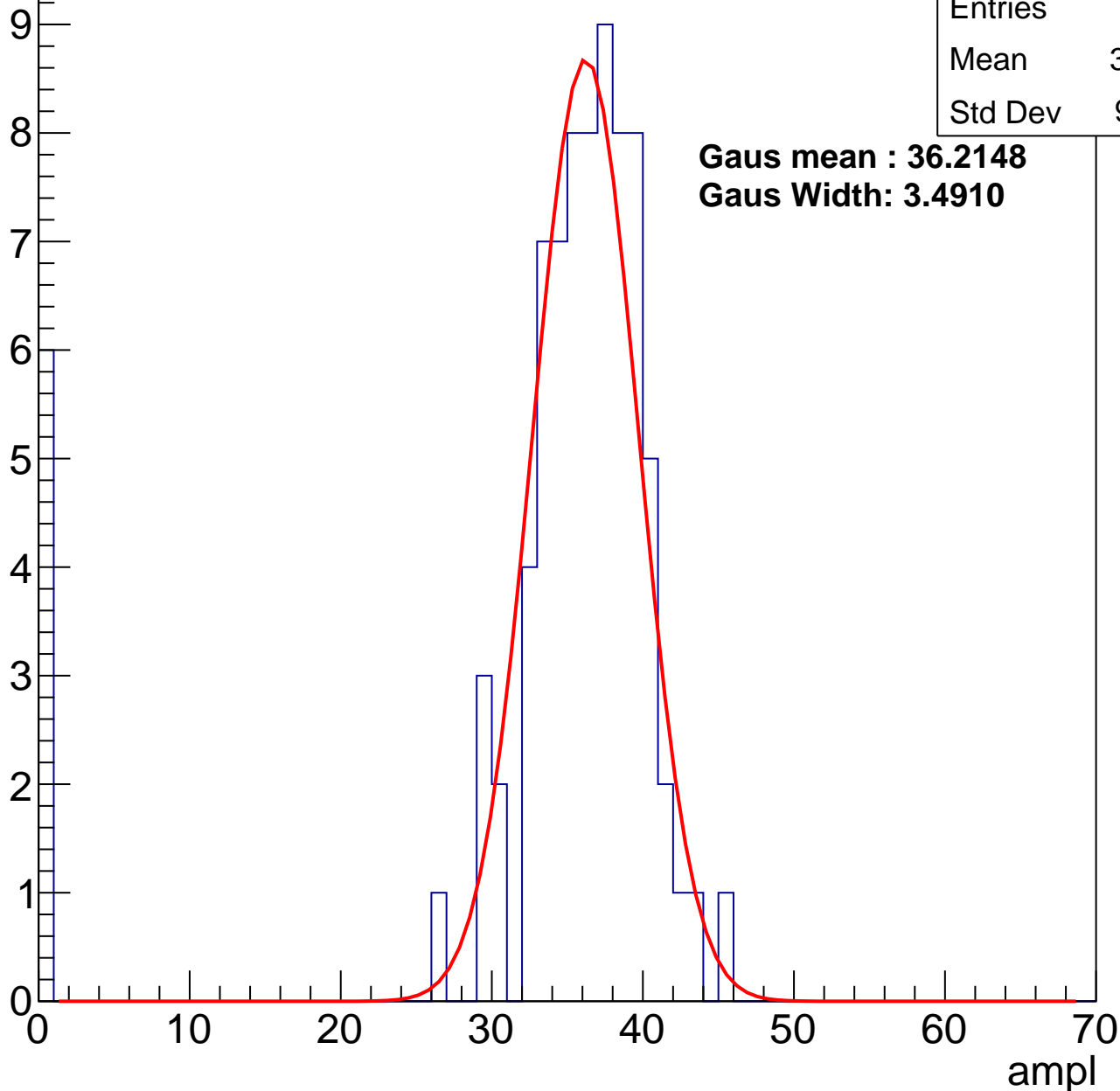
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	81
Mean	33.32
Std Dev	9.991

Gaus mean : 36.2148

Gaus Width: 3.4910



B1L103S, U7-ch35, adc2

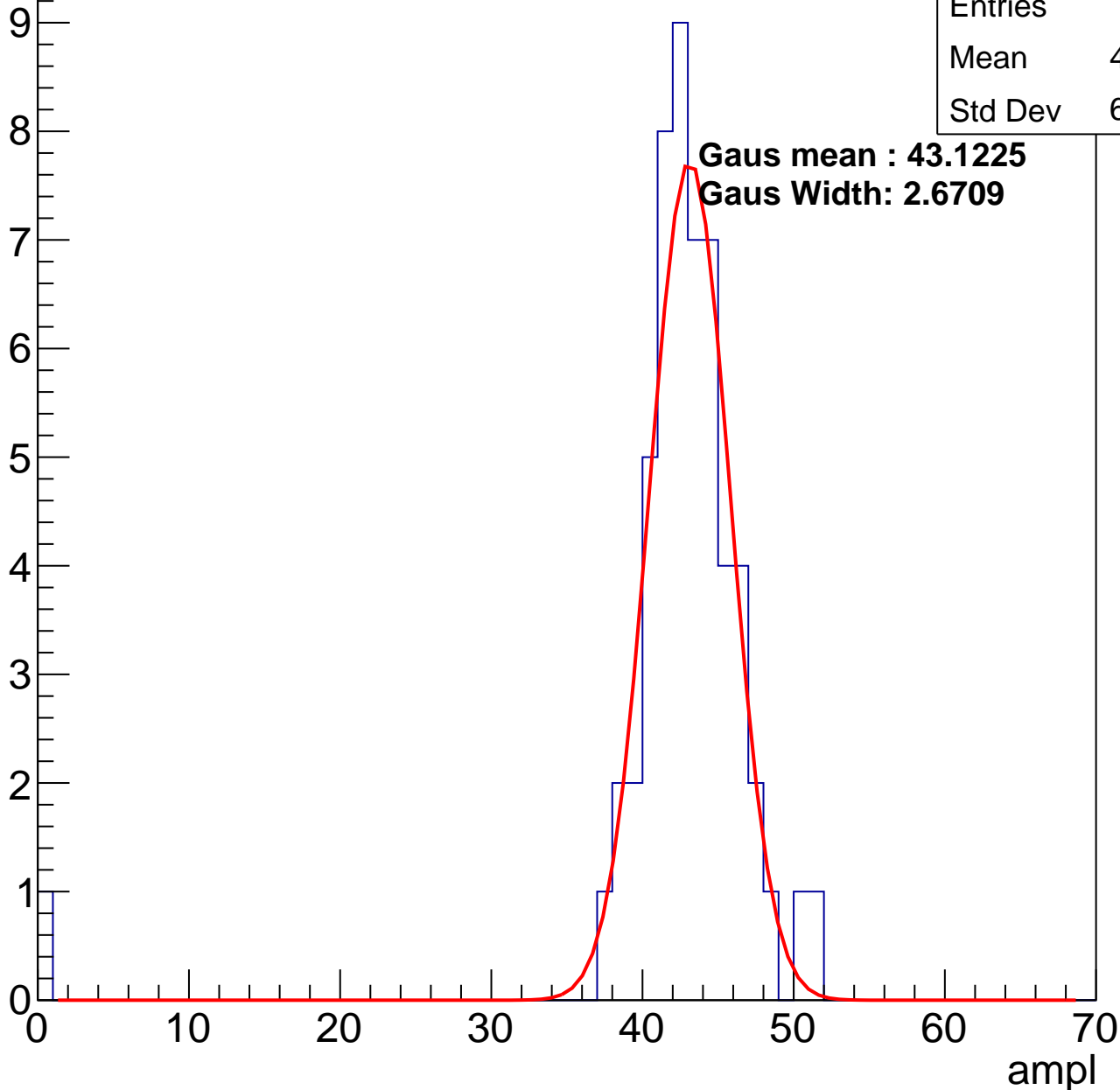
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	42.05
Std Dev	6.372

Gaus mean : 43.1225

Gaus Width: 2.6709

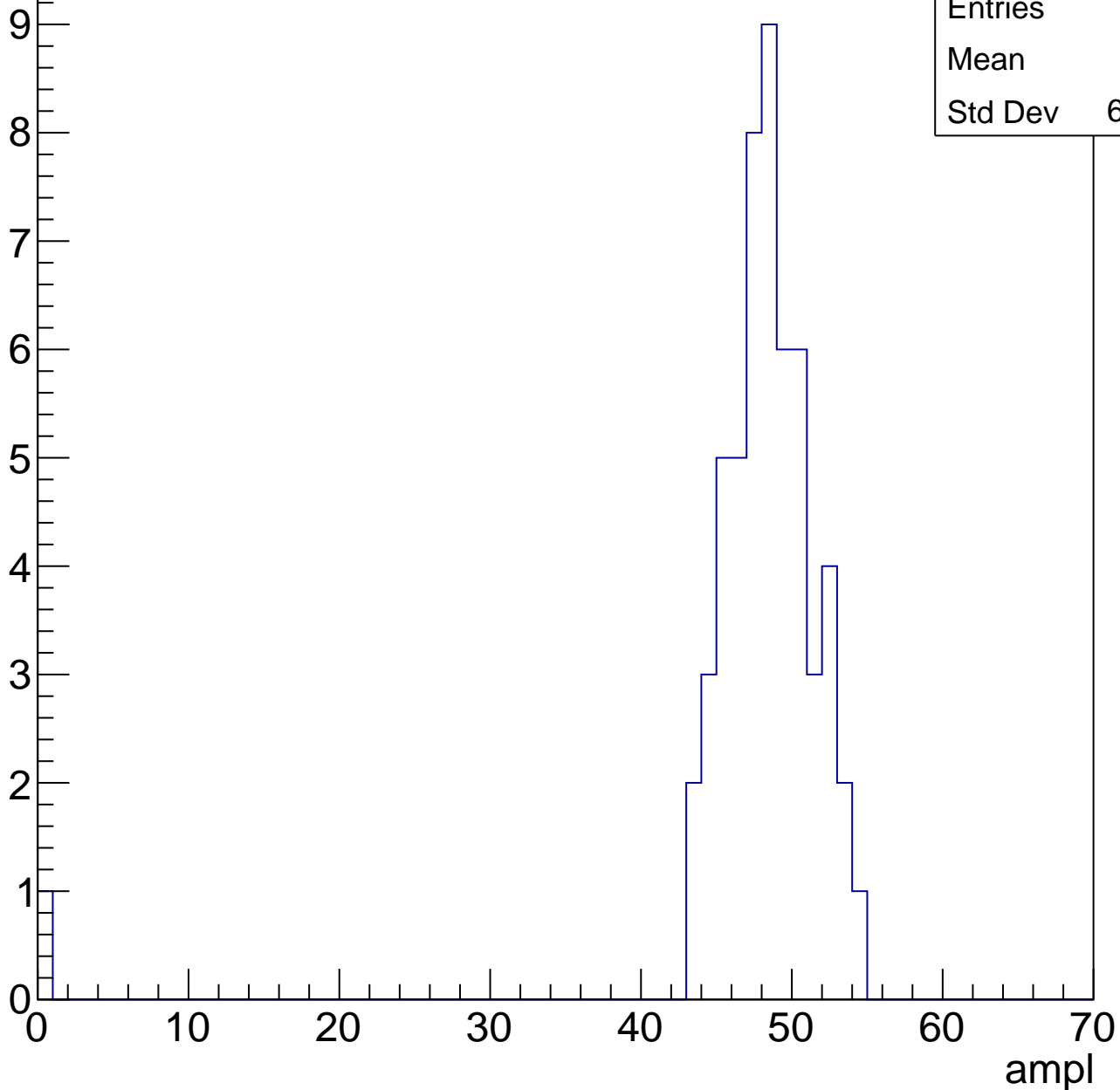


B1L103S, U7-ch35, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	47.2
Std Dev	6.937

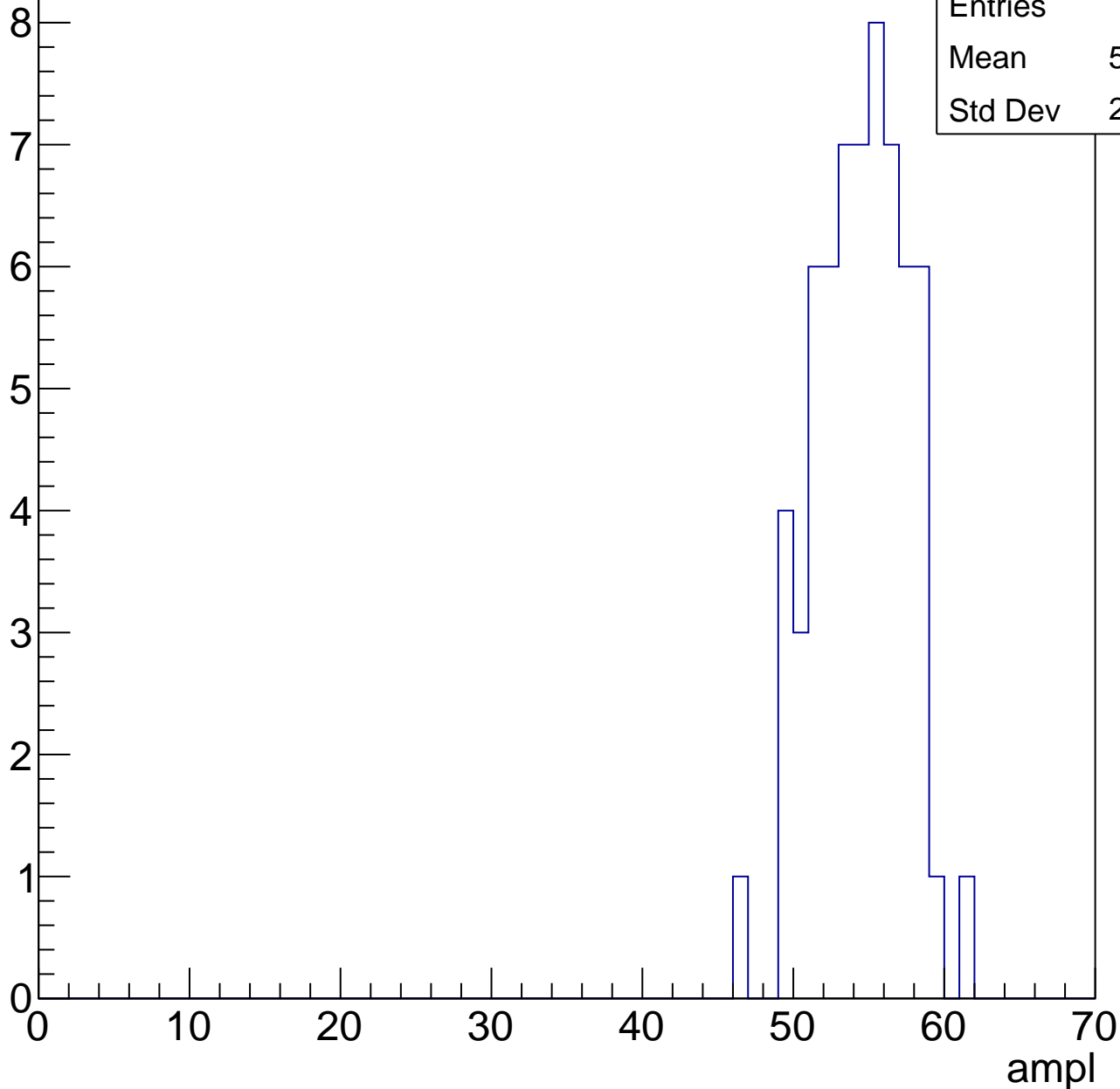


B1L103S, U7-ch35, adc4

calib_packv5_041523_1651.root, FC#0, port C2

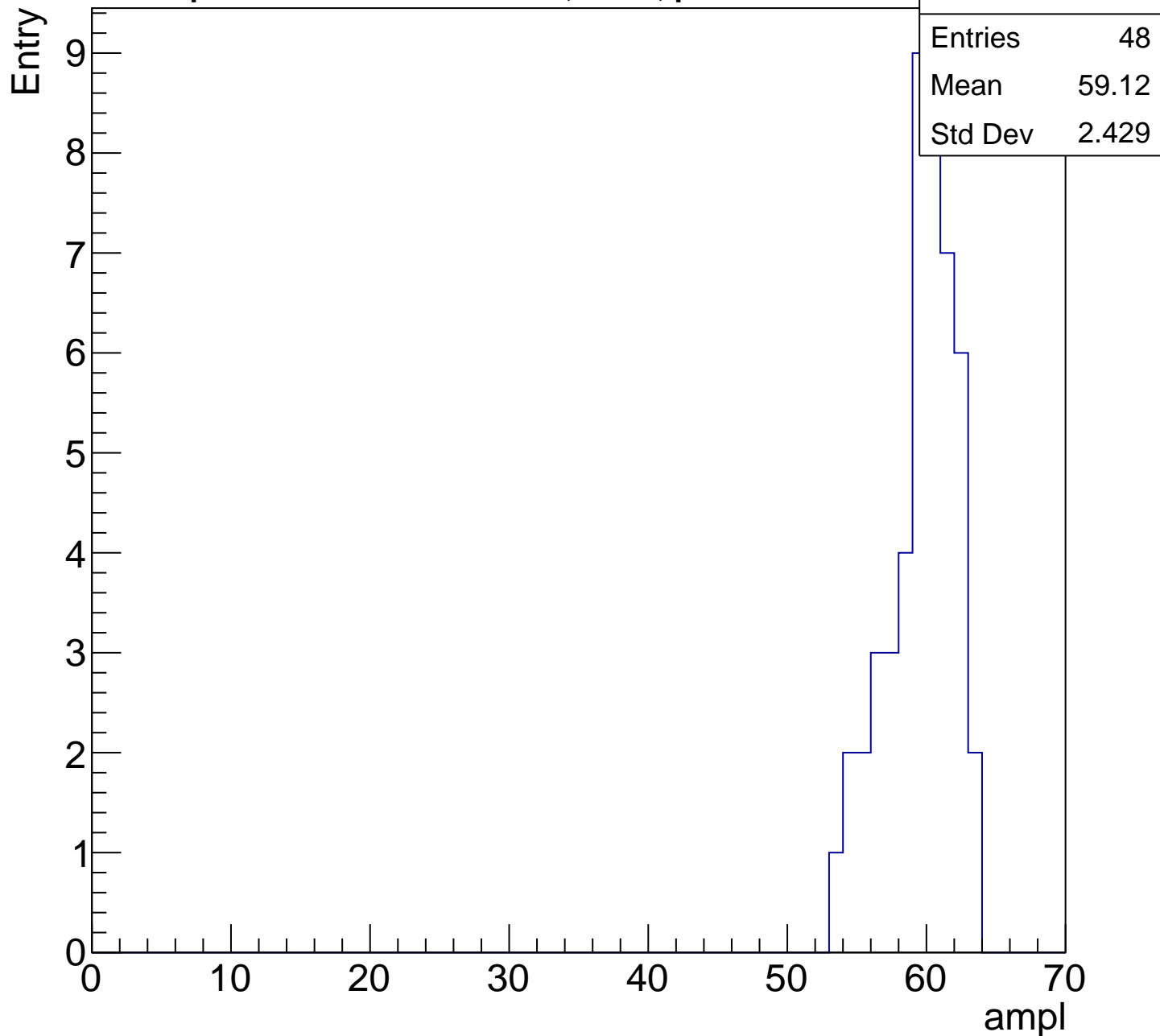
Entry

Entries	63
Mean	53.98
Std Dev	2.973



B1L103S, U7-ch35, adc5

calib_packv5_041523_1651.root, FC#0, port C2

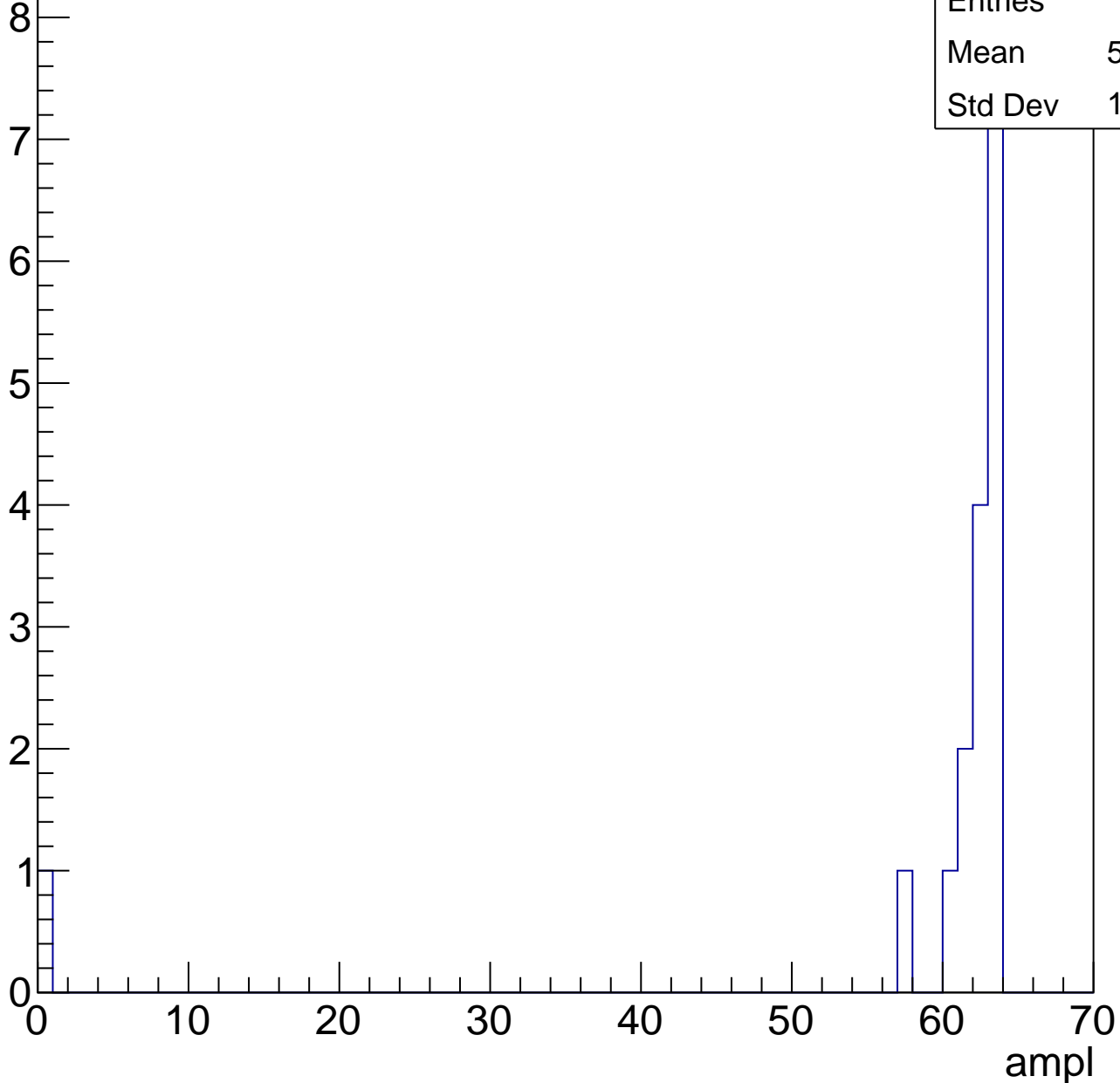


B1L103S, U7-ch35, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	17
Mean	58.29
Std Dev	14.65



B1L103S, U7-ch35, adc7

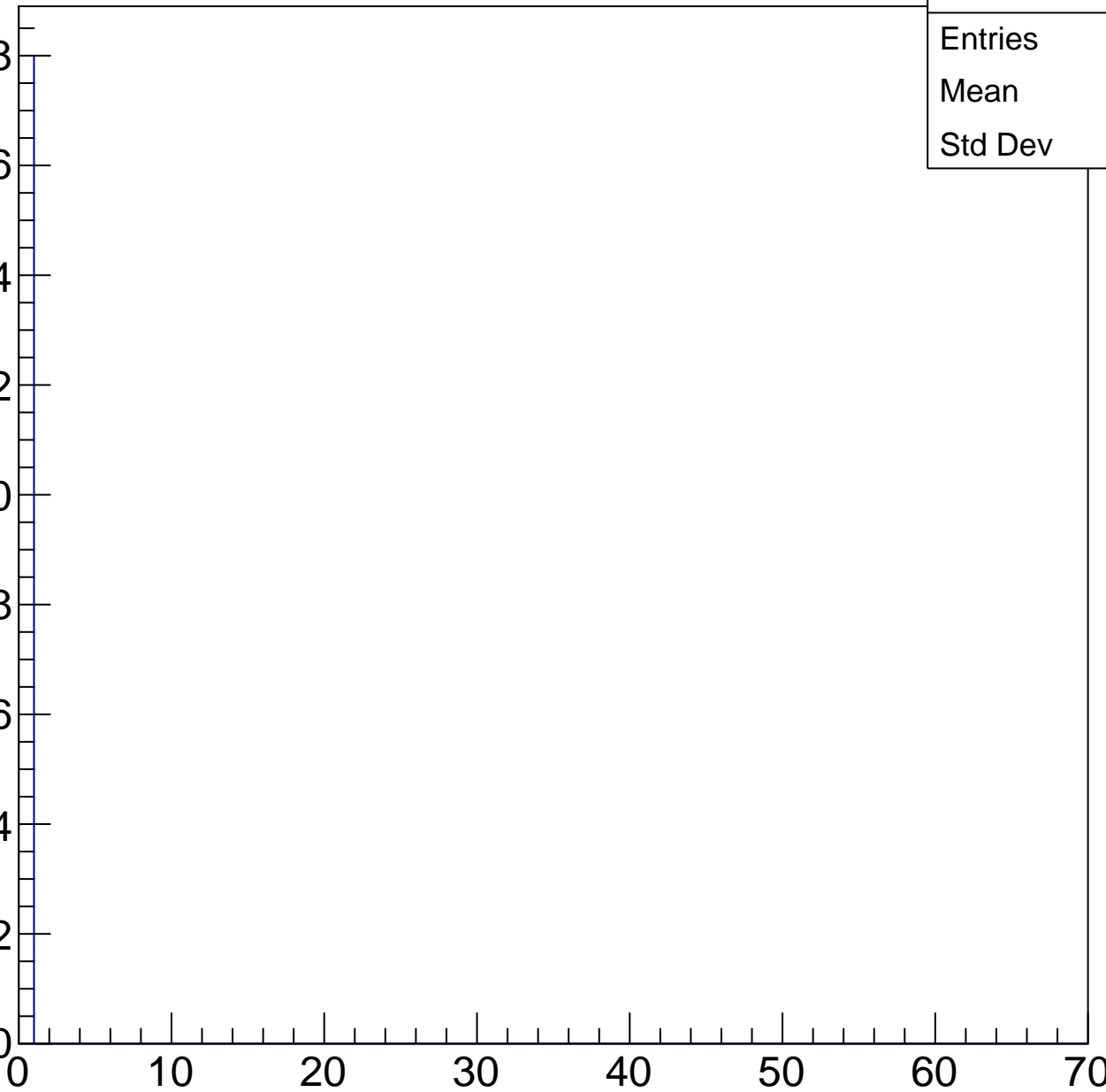
calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

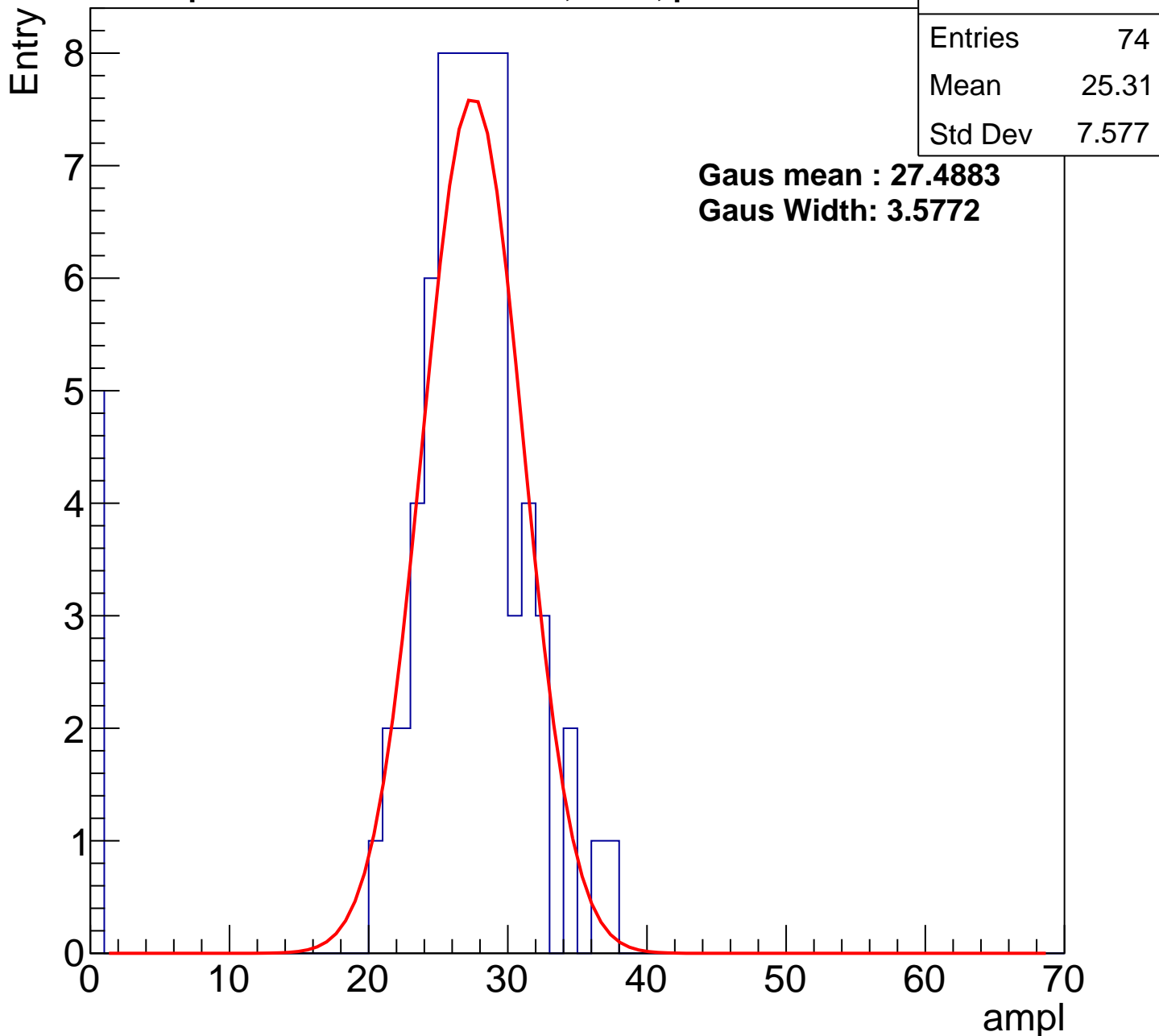
Entries	18
Mean	0
Std Dev	0

ampl



B1L103S, U7-ch36, adc0

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U7-ch36, adc1

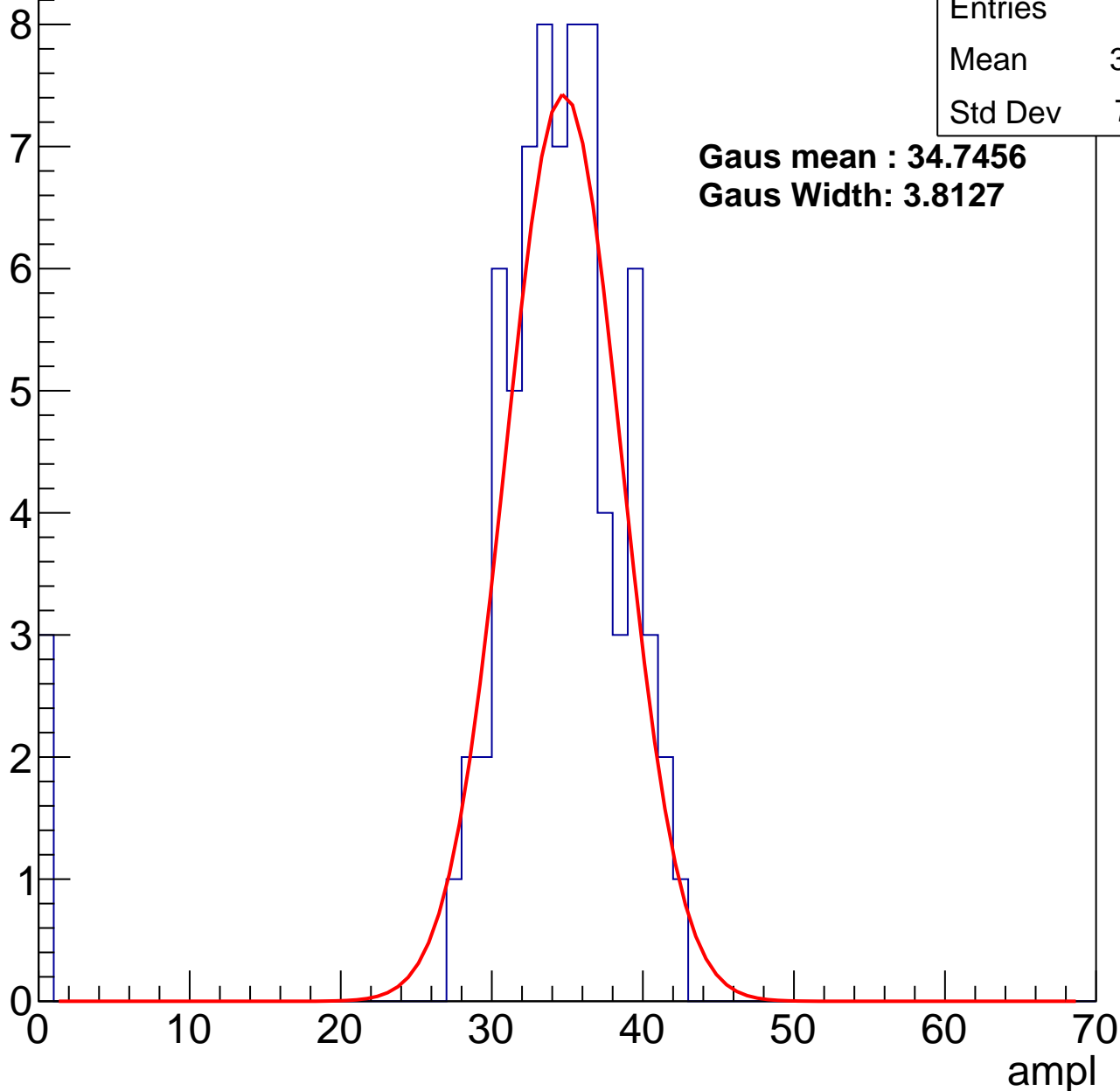
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	33.03
Std Dev	7.511

Gaus mean : 34.7456

Gaus Width: 3.8127



B1L103S, U7-ch36, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	73
Mean	37.92
Std Dev	10.96

Gaus mean : 41.8252

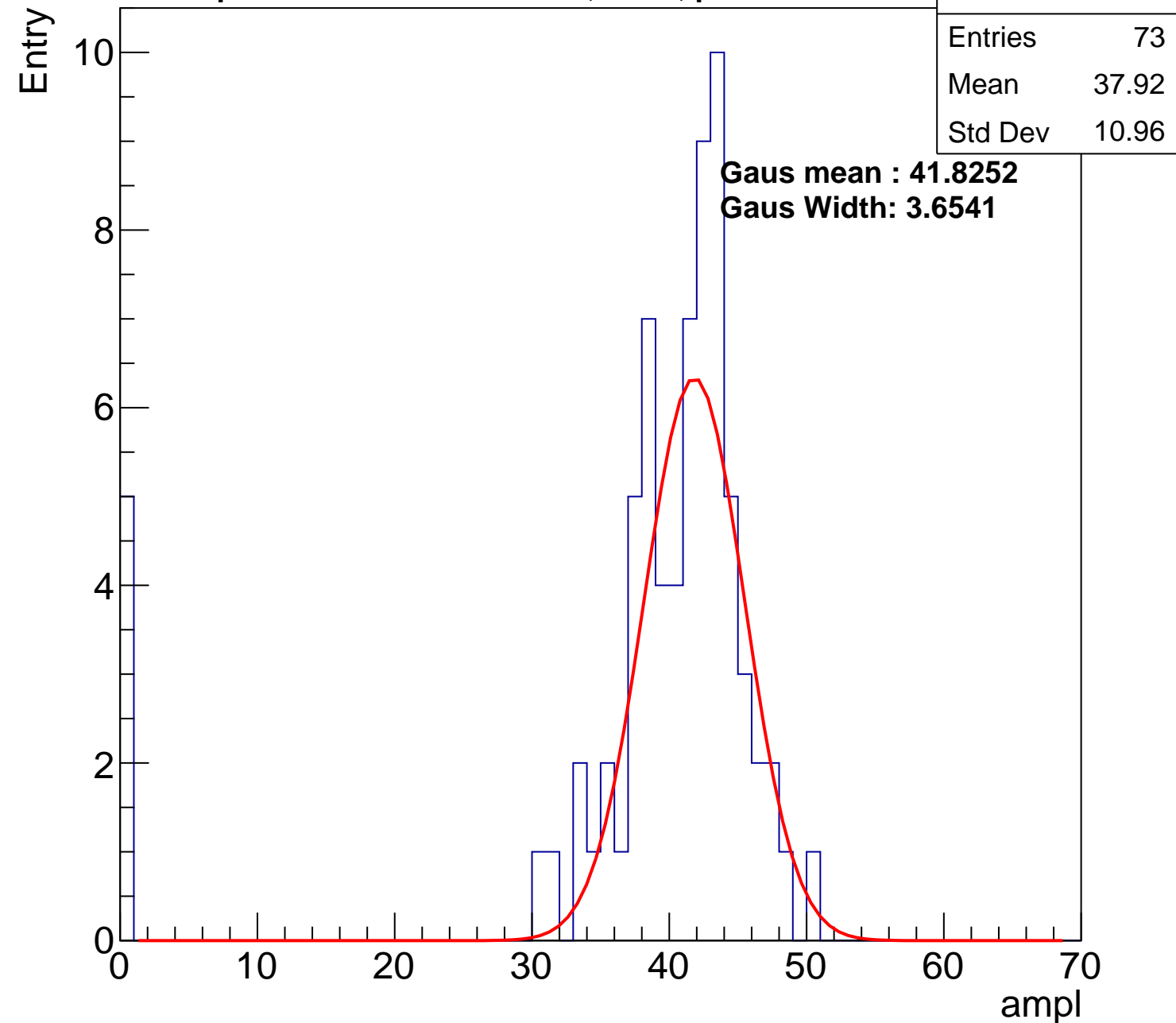
Gaus Width: 3.6541

Entry

10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

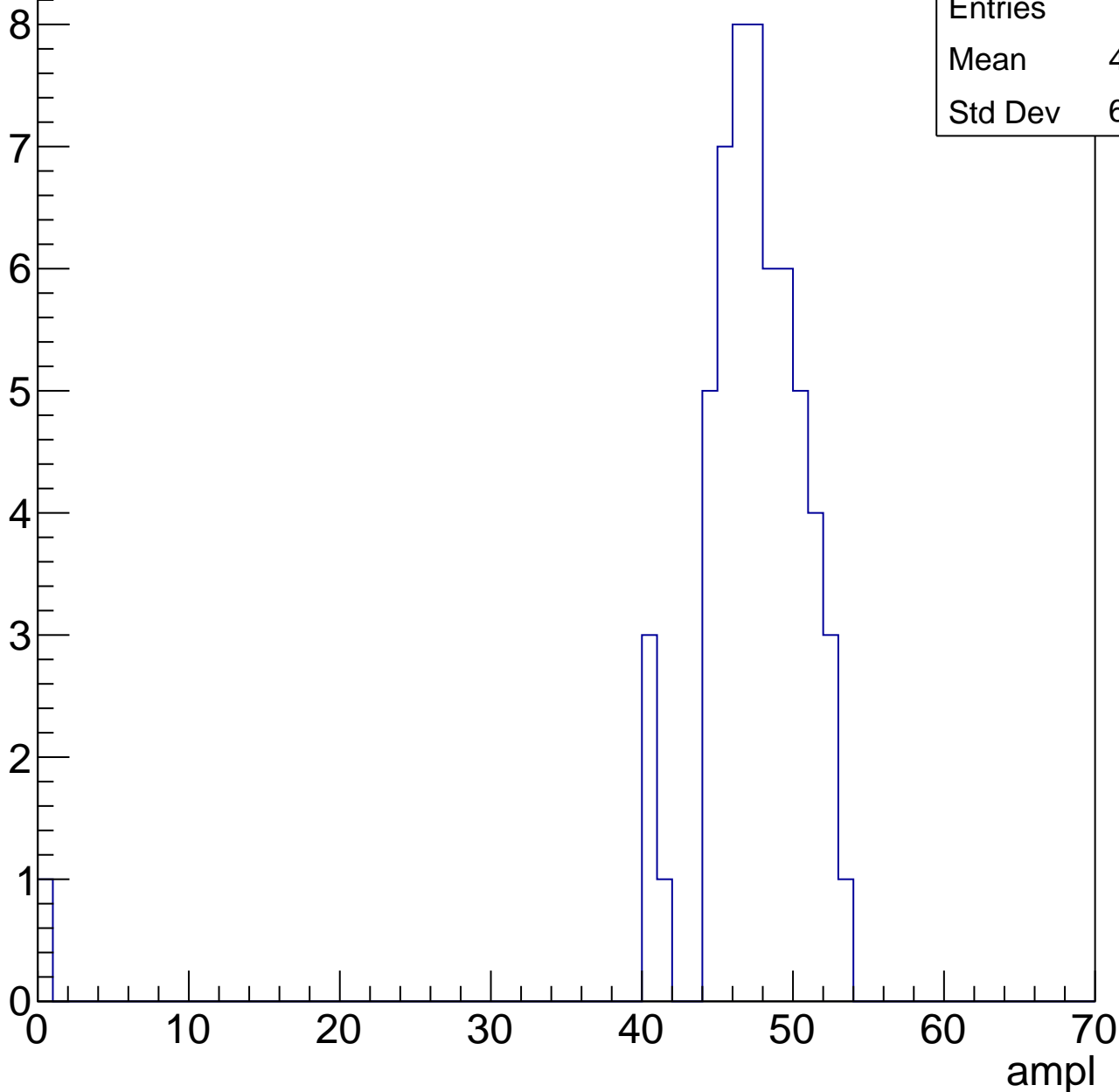


B1L103S, U7-ch36, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	46.29
Std Dev	6.815

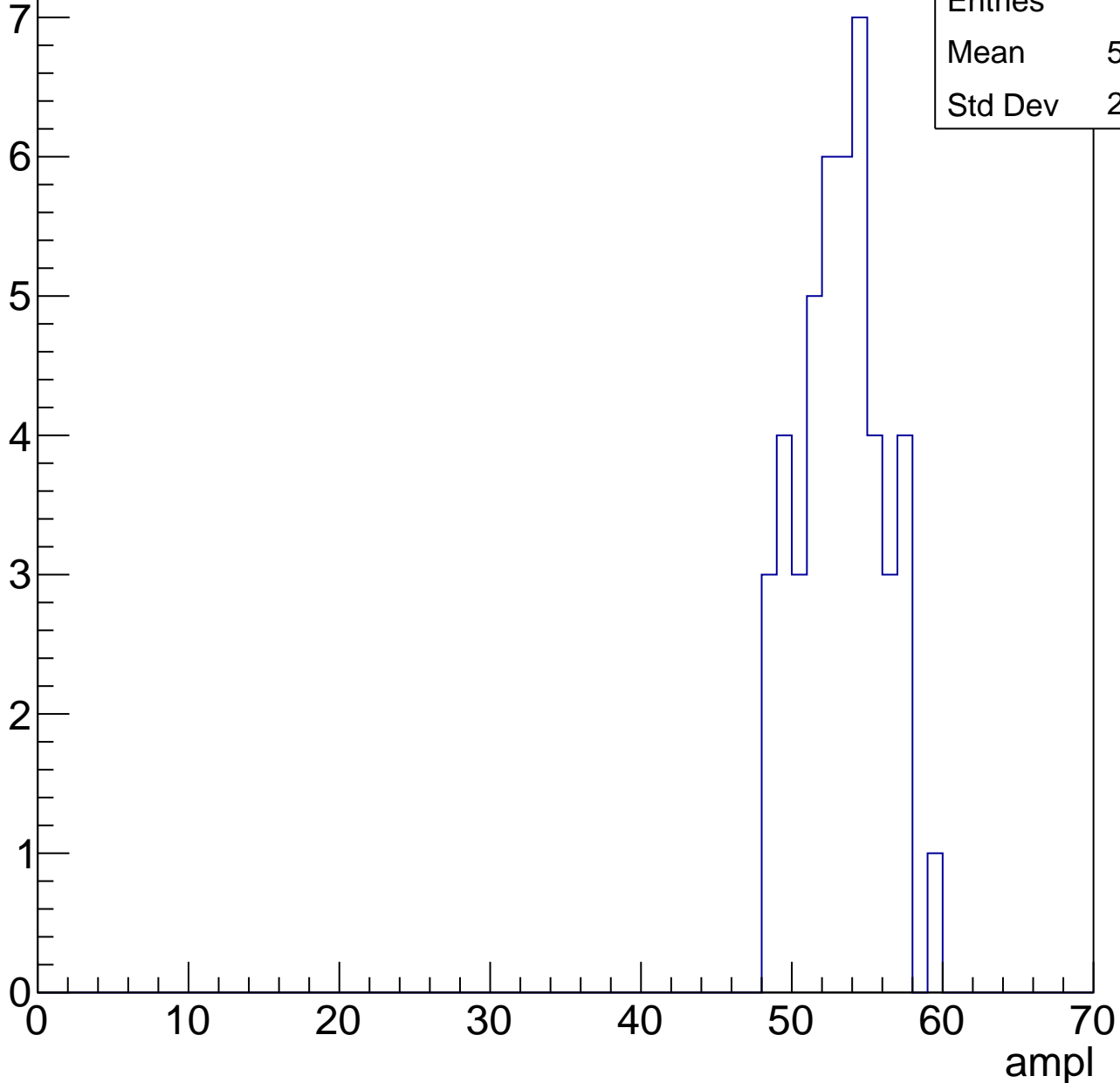


B1L103S, U7-ch36, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	46
Mean	52.78
Std Dev	2.718



B1L103S, U7-ch36, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

Entries 75

Mean 58.24

Std Dev 3.115

8

6

4

2

0

0

10

20

30

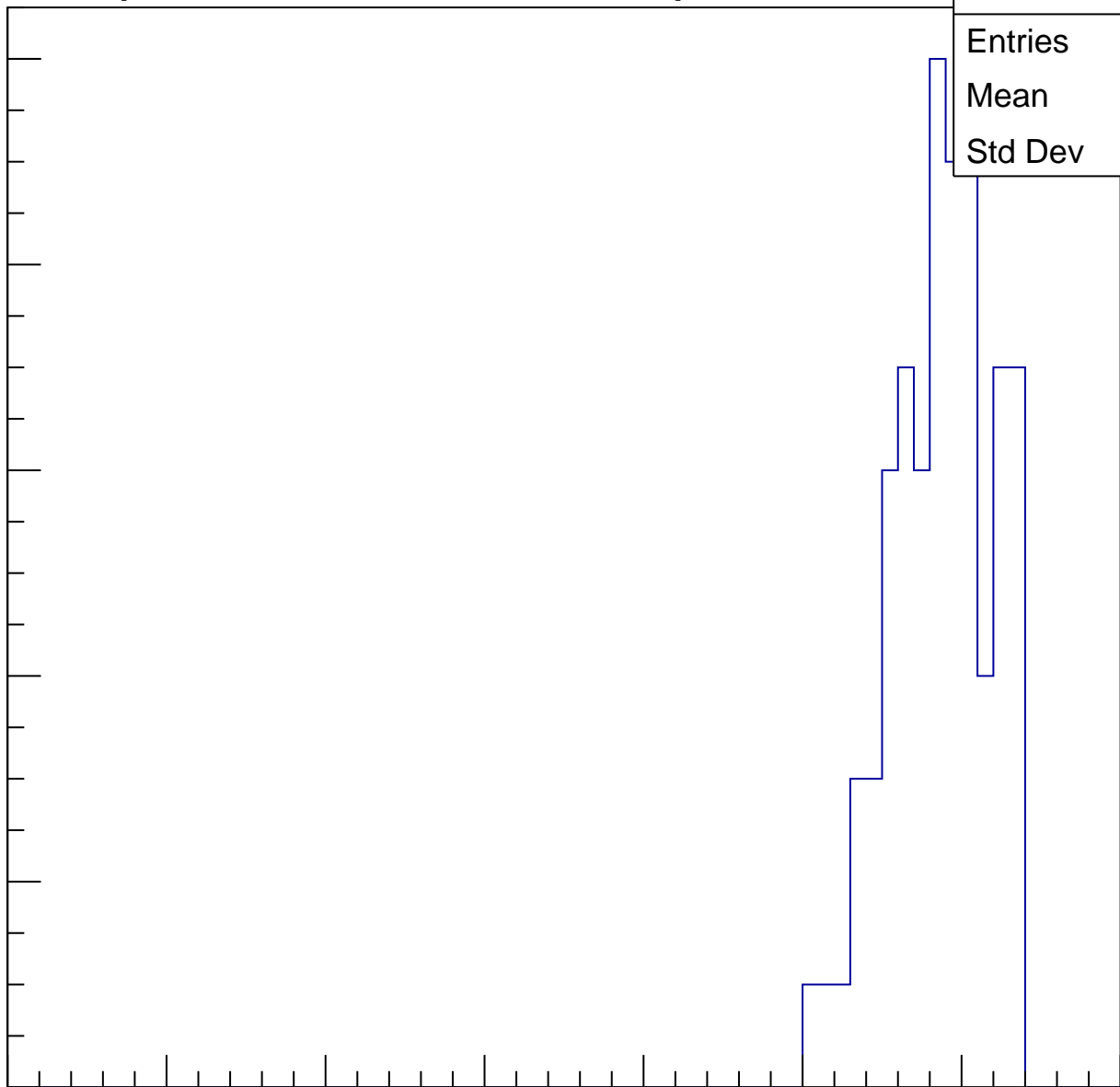
40

50

60

70

ampl

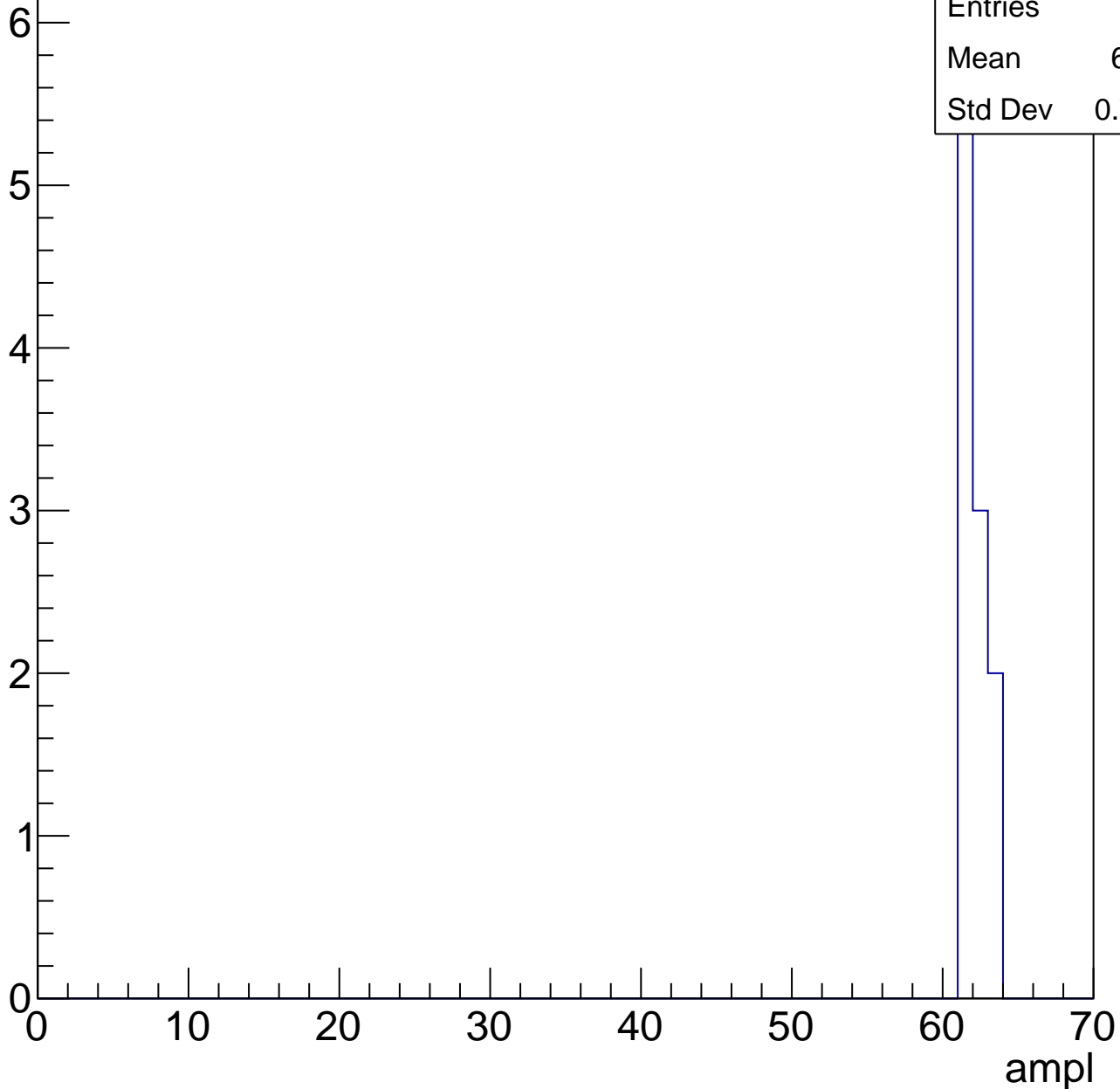


B1L103S, U7-ch36, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	11
Mean	61.64
Std Dev	0.7714

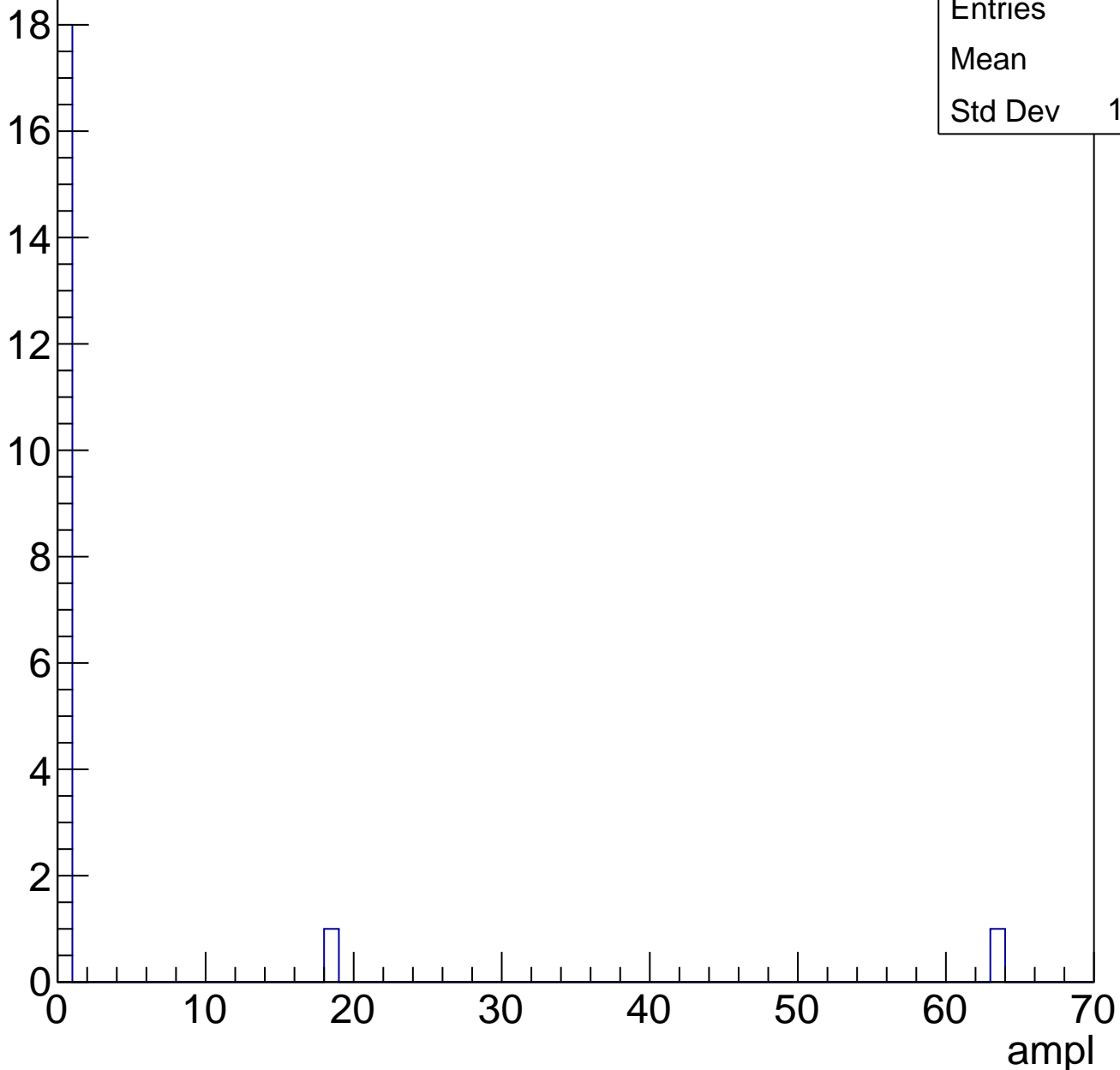


B1L103S, U7-ch36, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	4.05
Std Dev	14.08

Entry



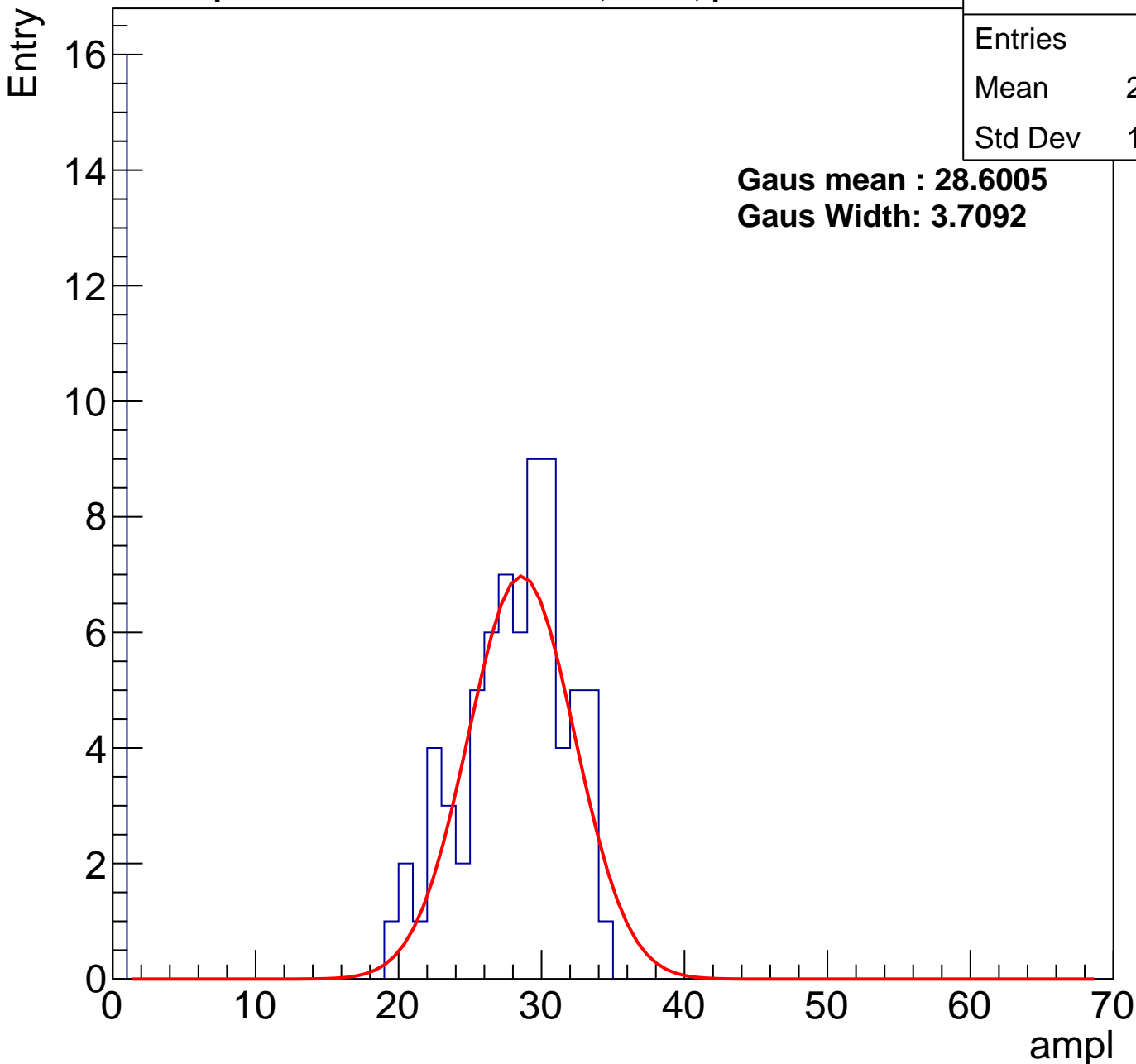
B1L103S, U7-ch37, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	86
Mean	22.52
Std Dev	11.24

Gaus mean : 28.6005

Gaus Width: 3.7092



B1L103S, U7-ch37, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	67
Mean	35.48
Std Dev	3.387

Gaus mean : 36.0097

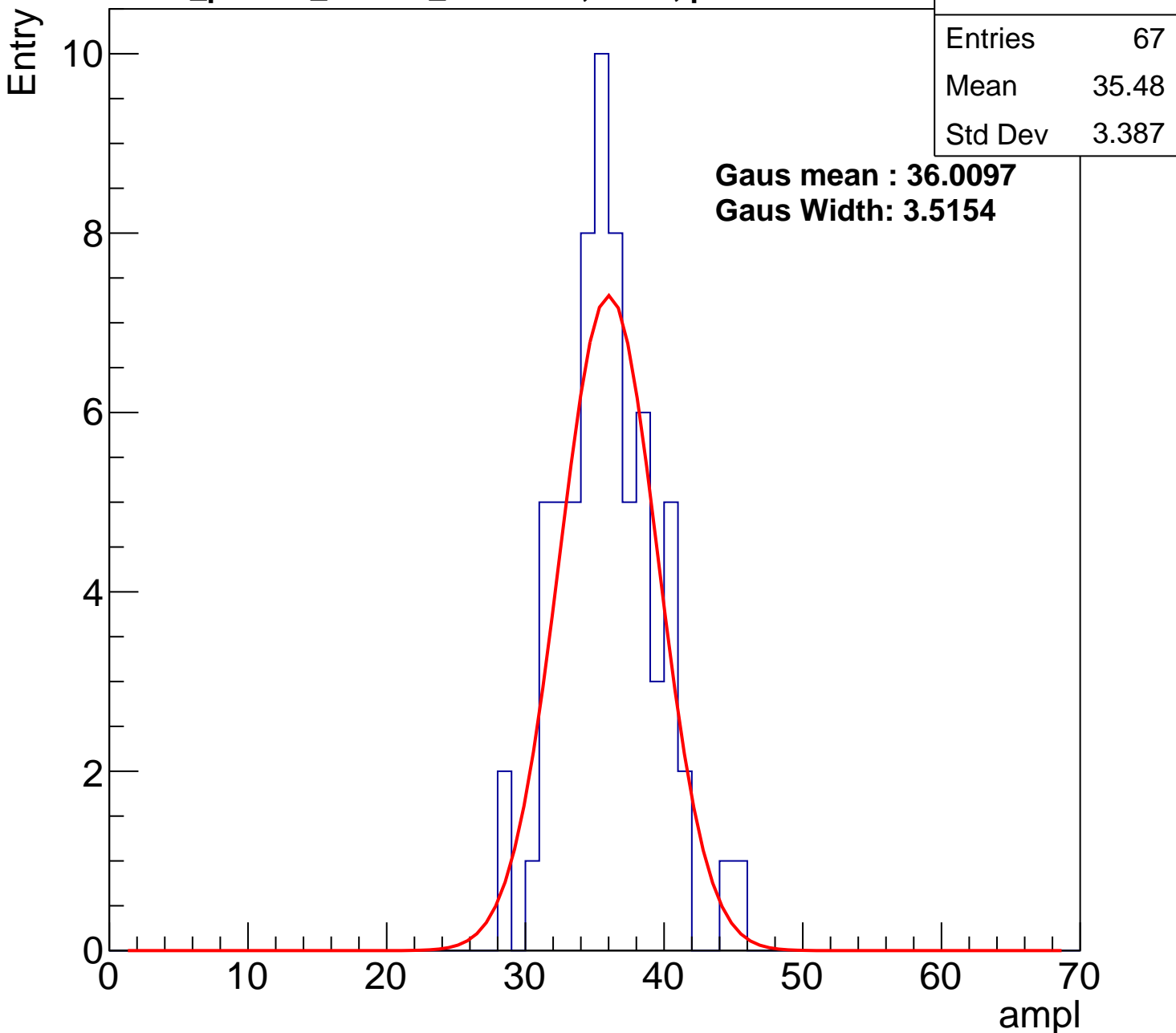
Gaus Width: 3.5154

Entry

10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U7-ch37, adc2

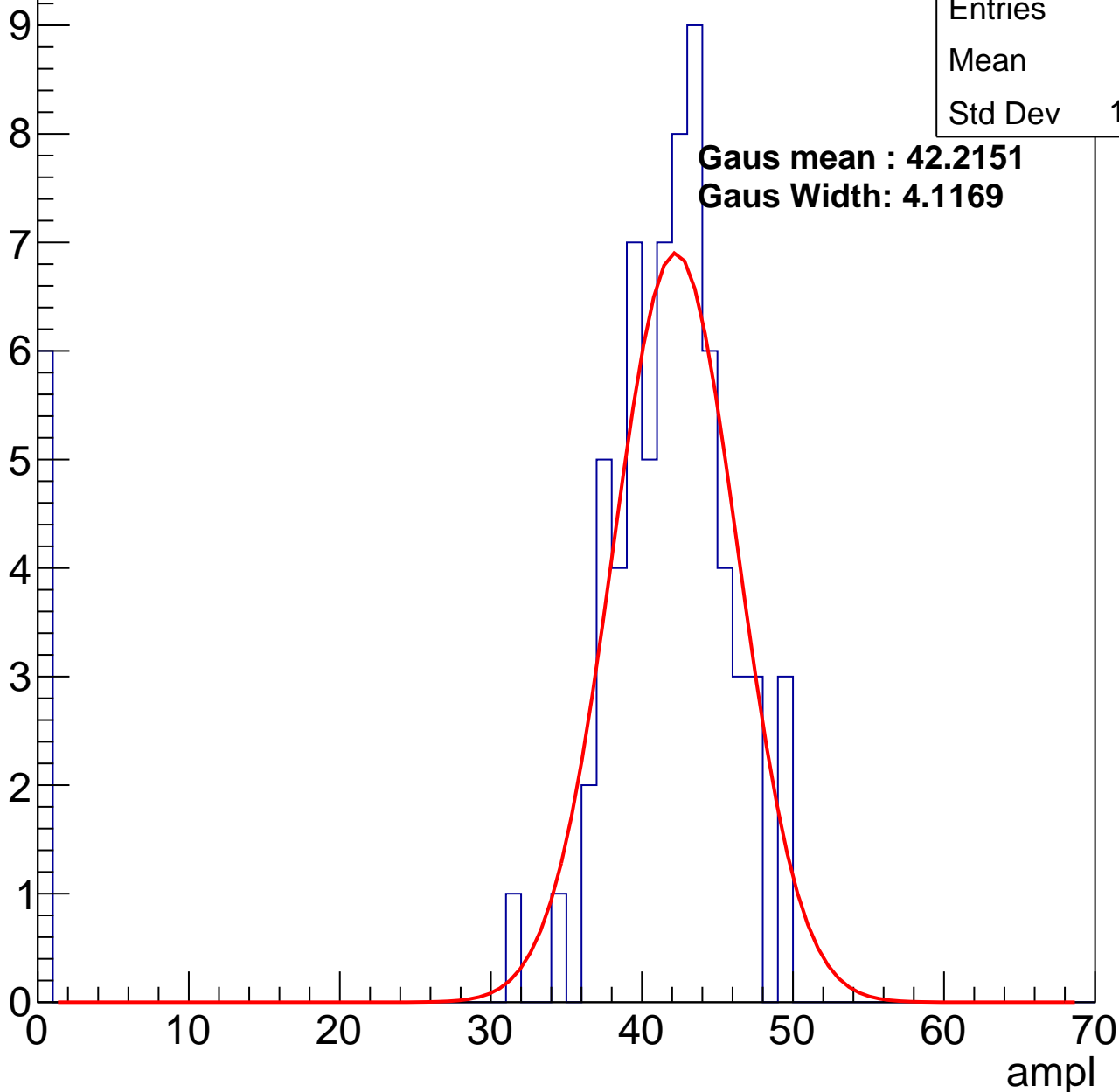
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	38.2
Std Dev	11.85

Gaus mean : 42.2151

Gaus Width: 4.1169



B1L103S, U7-ch37, adc3

calib_packv5_041523_1651.root, FC#0, port C2

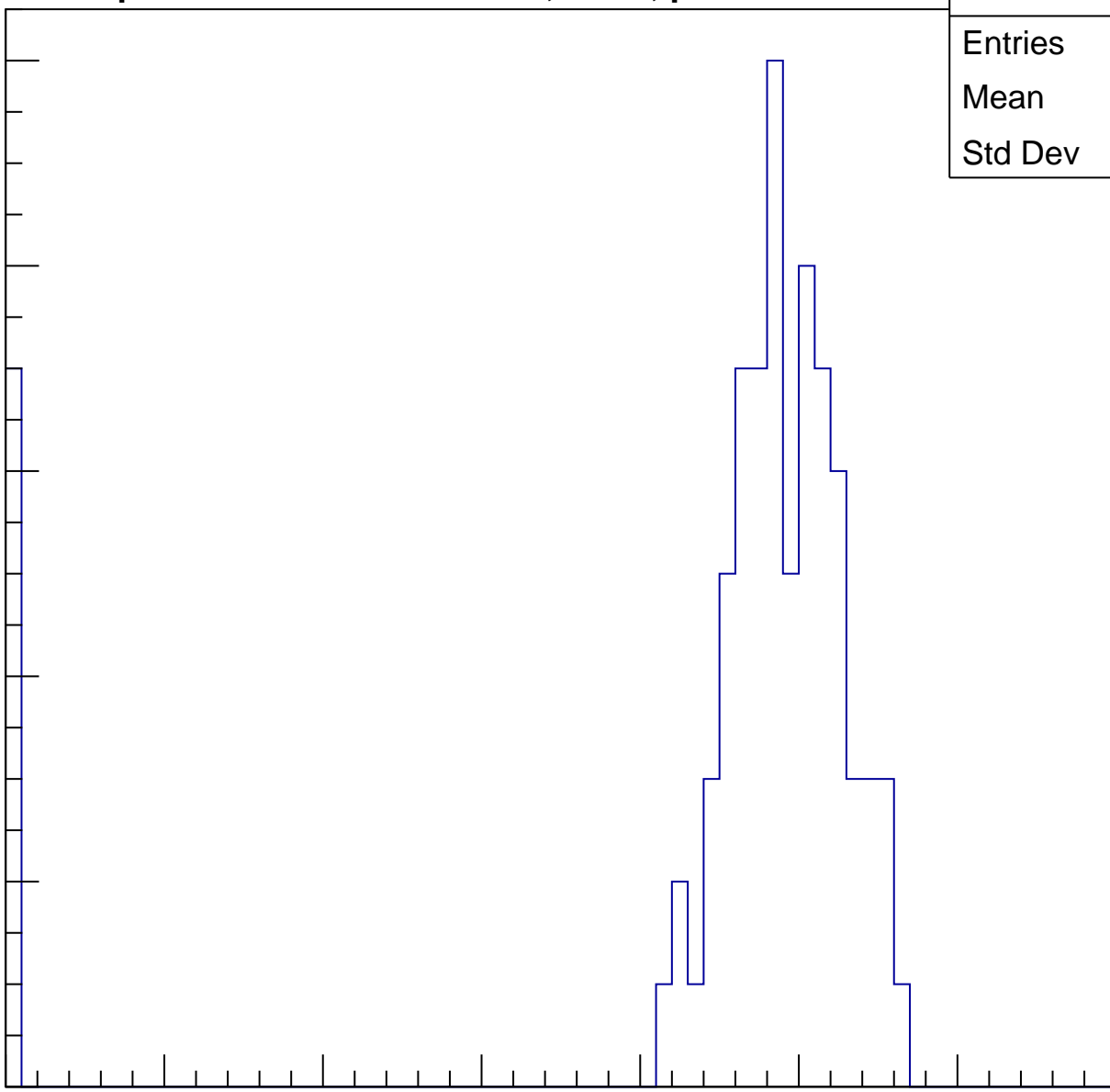
Entries	79
Mean	44.46
Std Dev	14.23

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

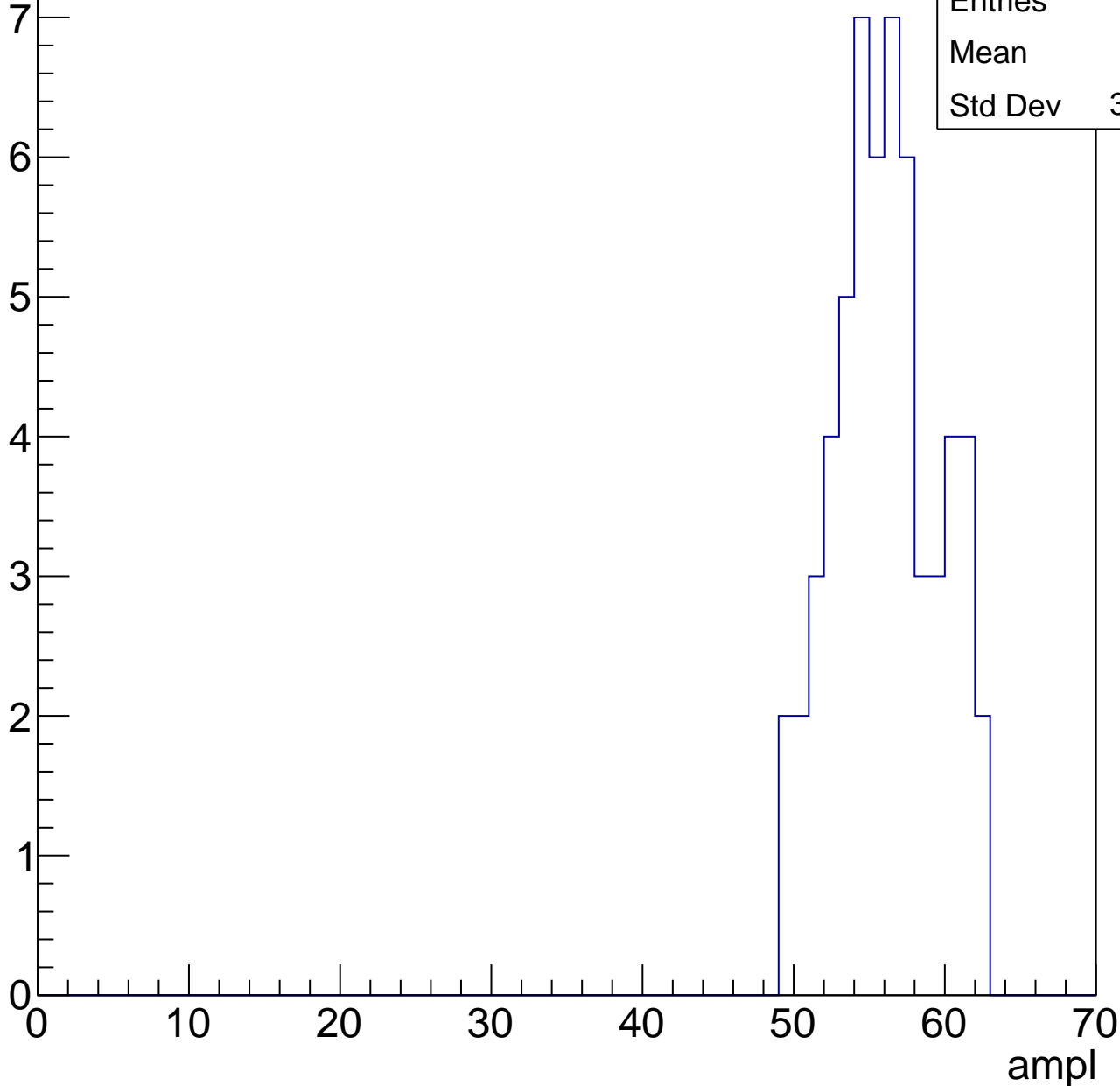


B1L103S, U7-ch37, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

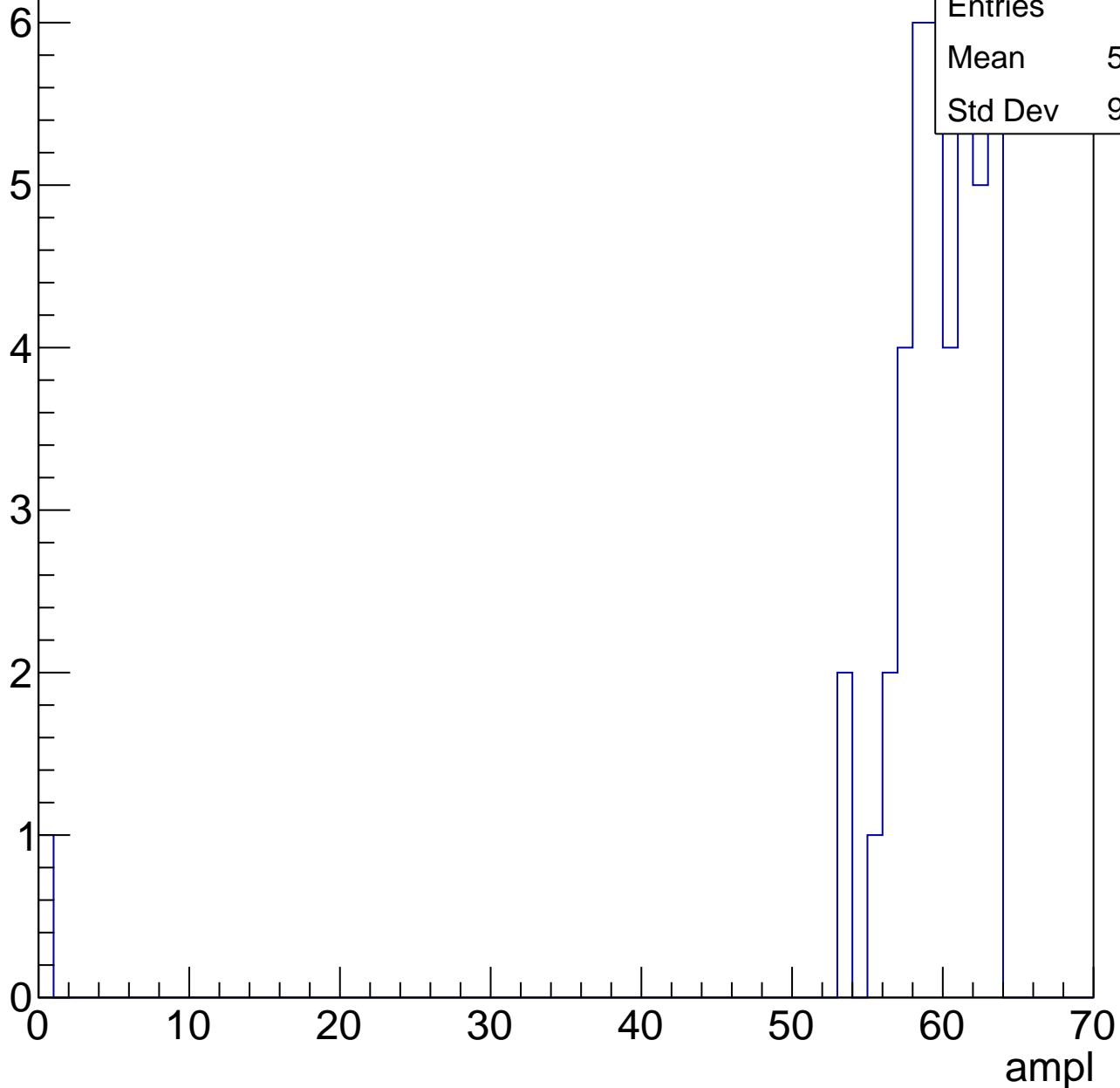
Entries	58
Mean	55.6
Std Dev	3.373



B1L103S, U7-ch37, adc5

calib_packv5_041523_1651.root, FC#0, port C2

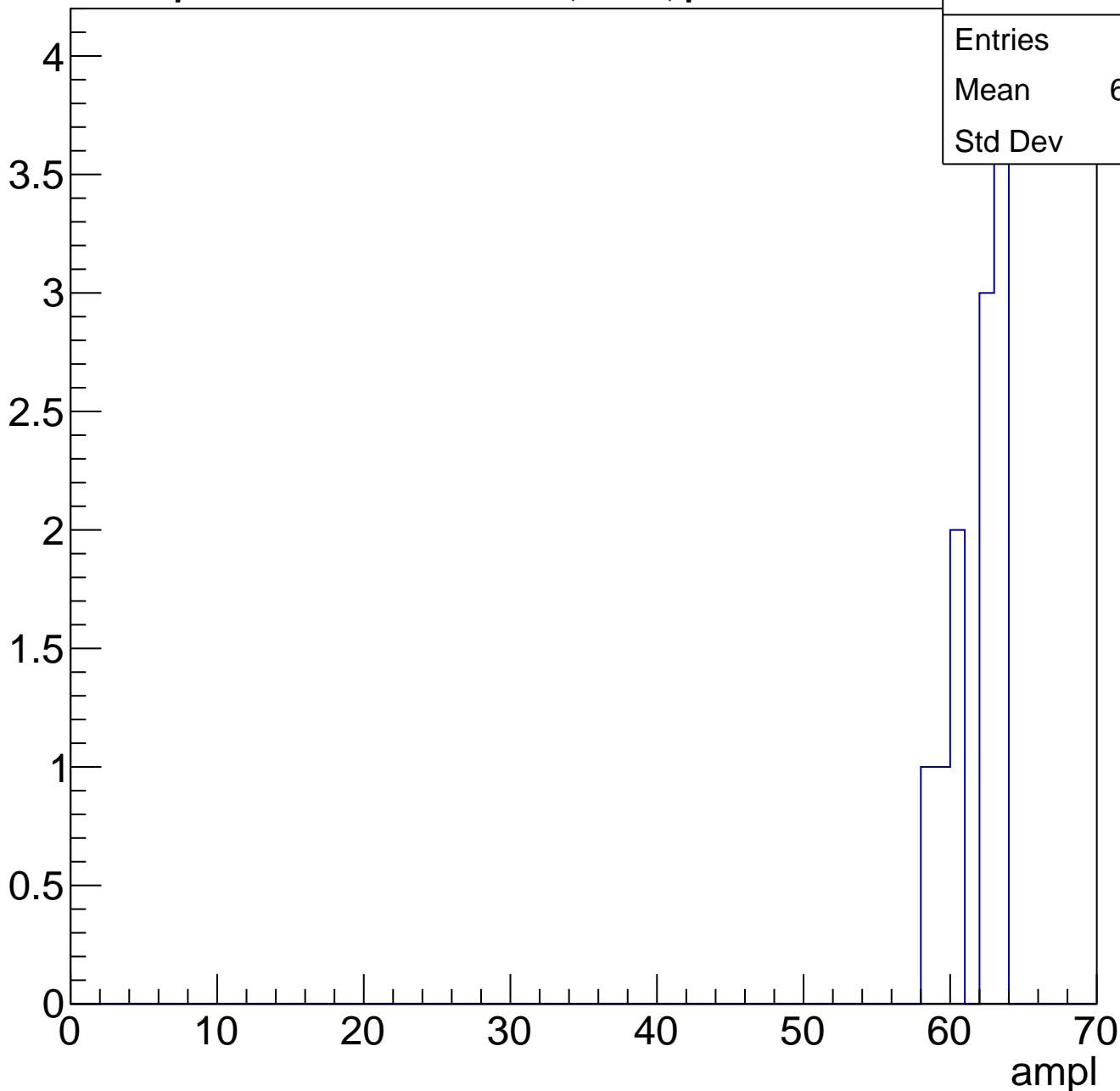
Entry



B1L103S, U7-ch37, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch37, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch38, adc0

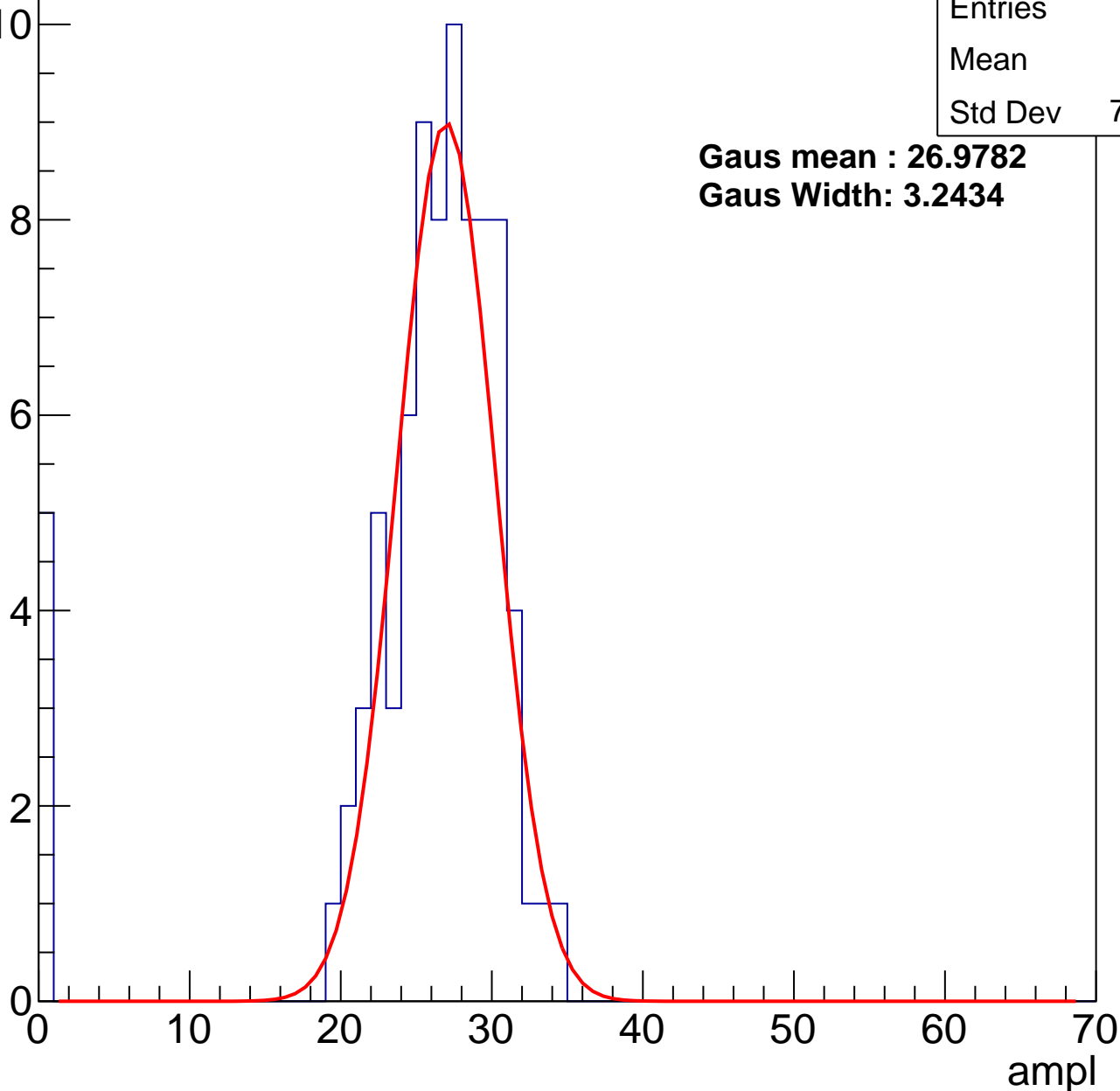
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	83
Mean	24.9
Std Dev	7.035

Gaus mean : 26.9782

Gaus Width: 3.2434



B1L103S, U7-ch38, adc1

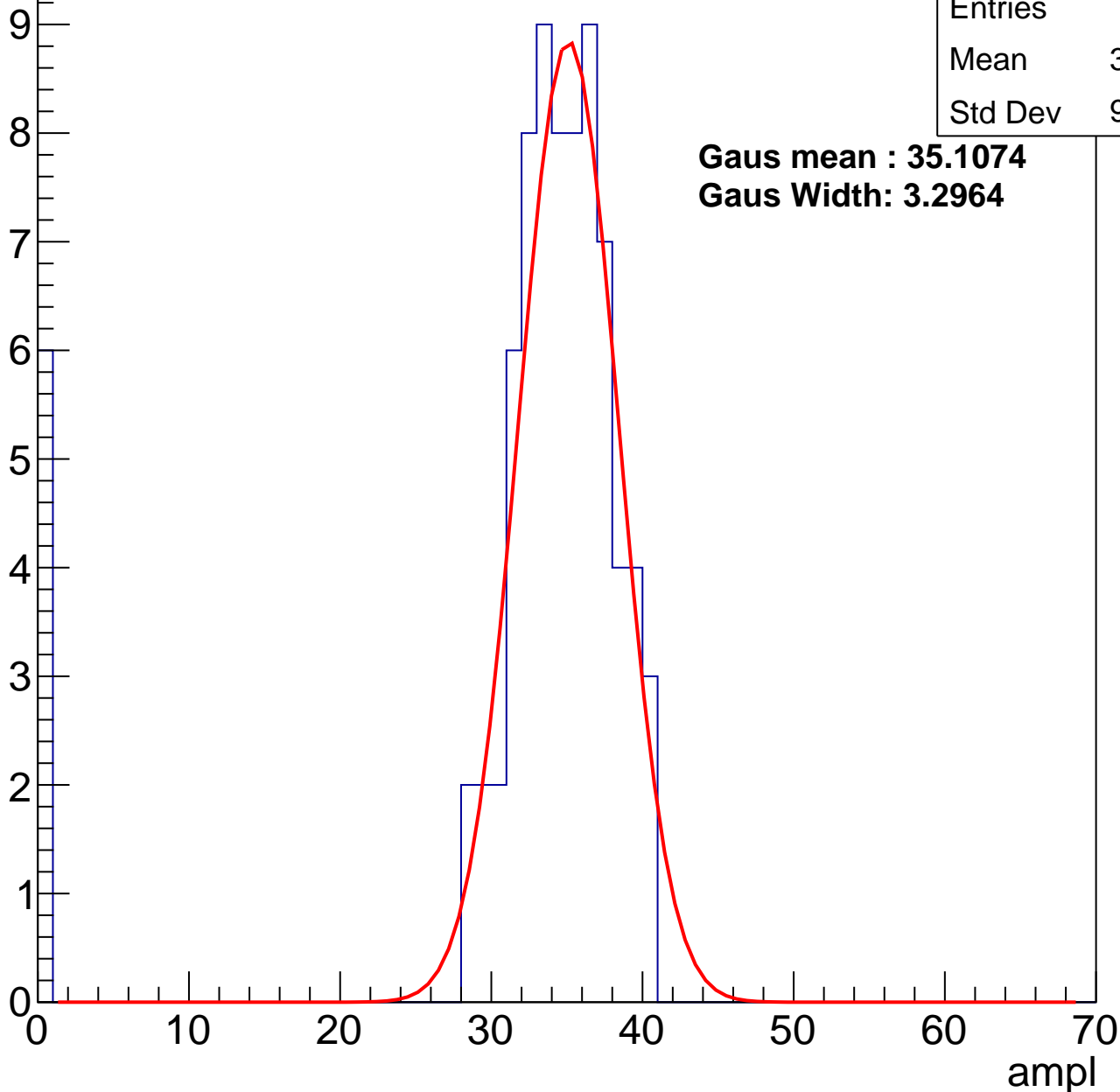
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	31.74
Std Dev	9.586

Gaus mean : 35.1074

Gaus Width: 3.2964



B1L103S, U7-ch38, adc2

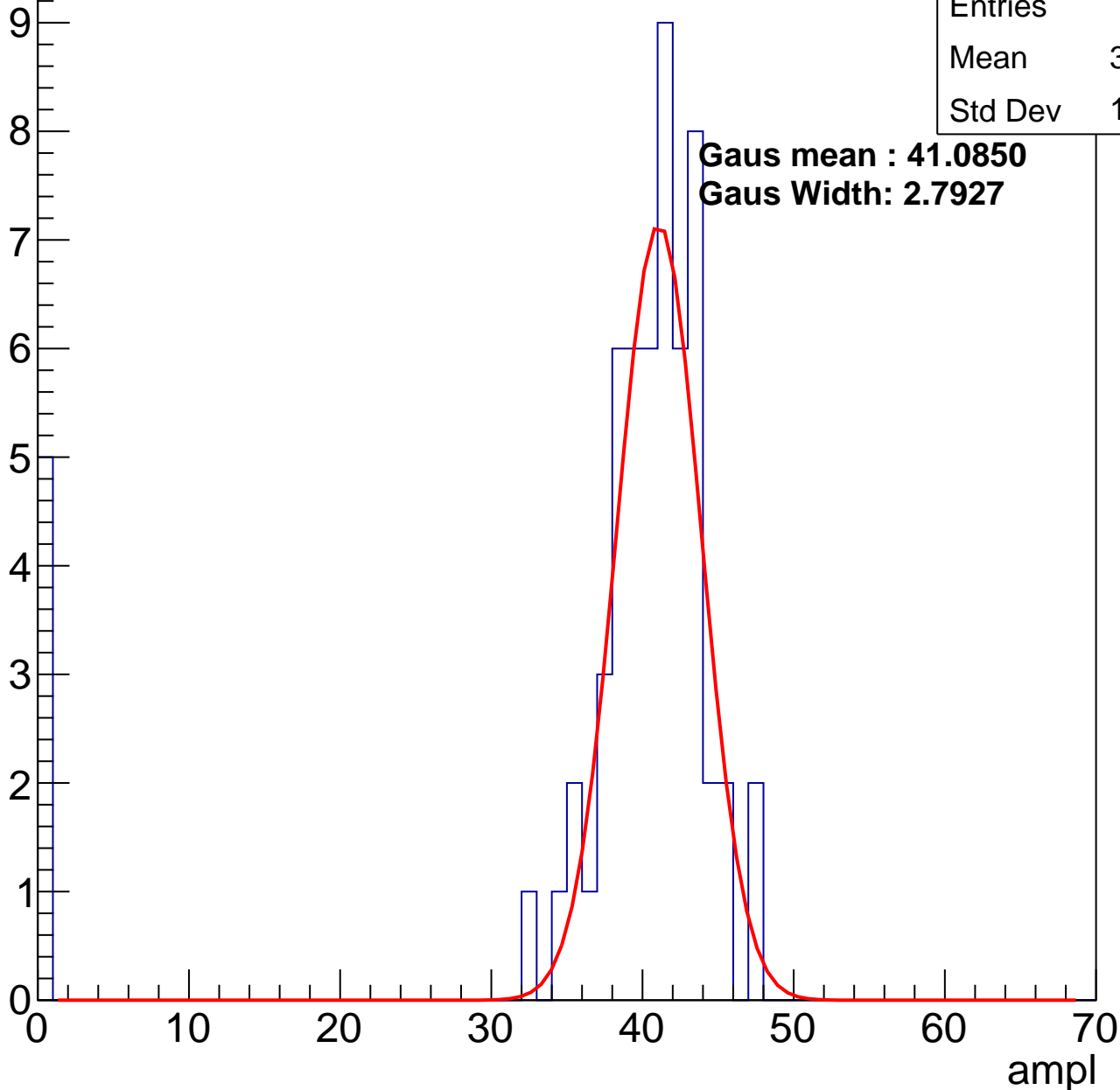
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	37.03
Std Dev	11.53

Gaus mean : 41.0850

Gaus Width: 2.7927

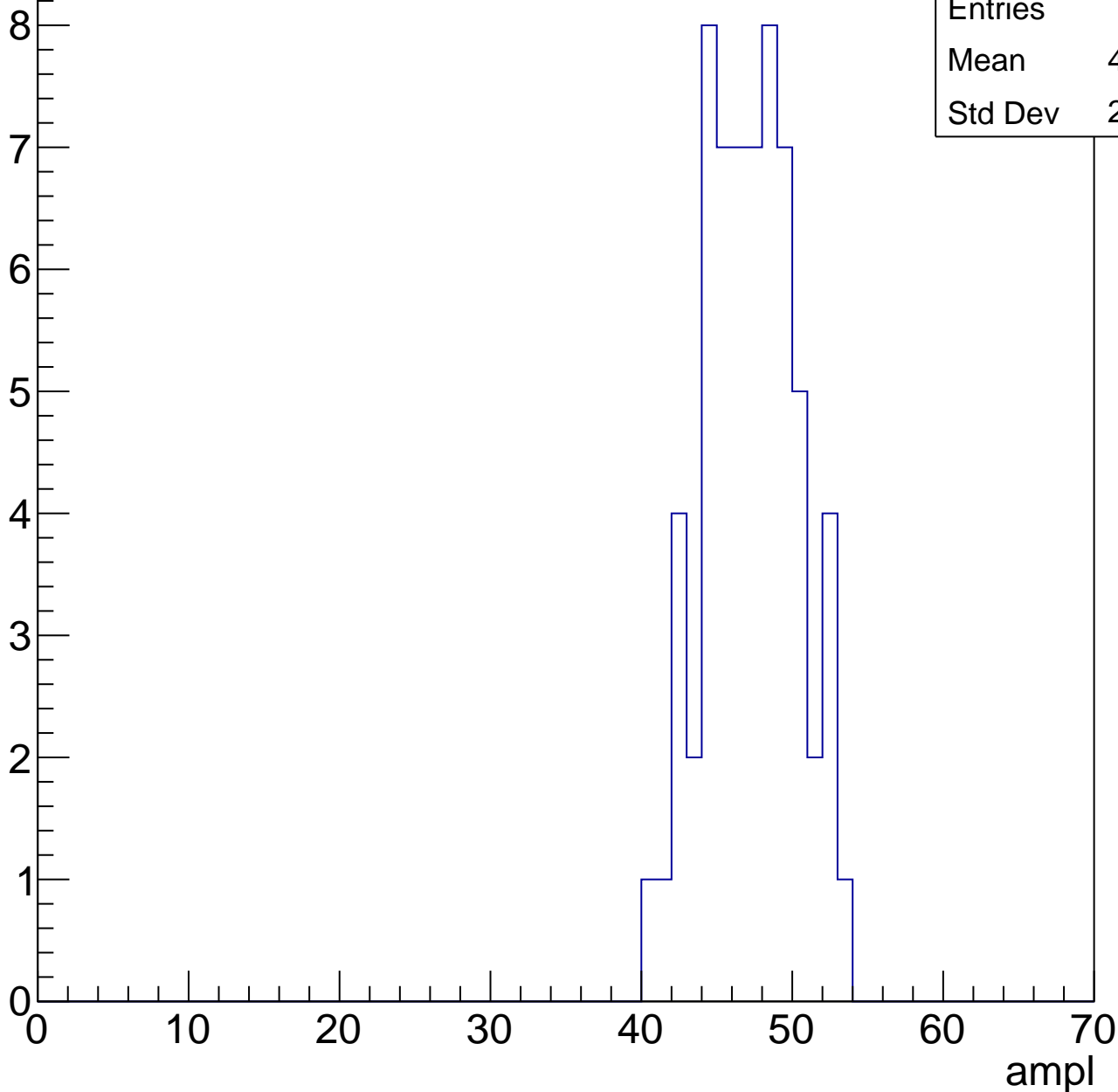


B1L103S, U7-ch38, adc3

calib_packv5_041523_1651.root, FC#0, port C2

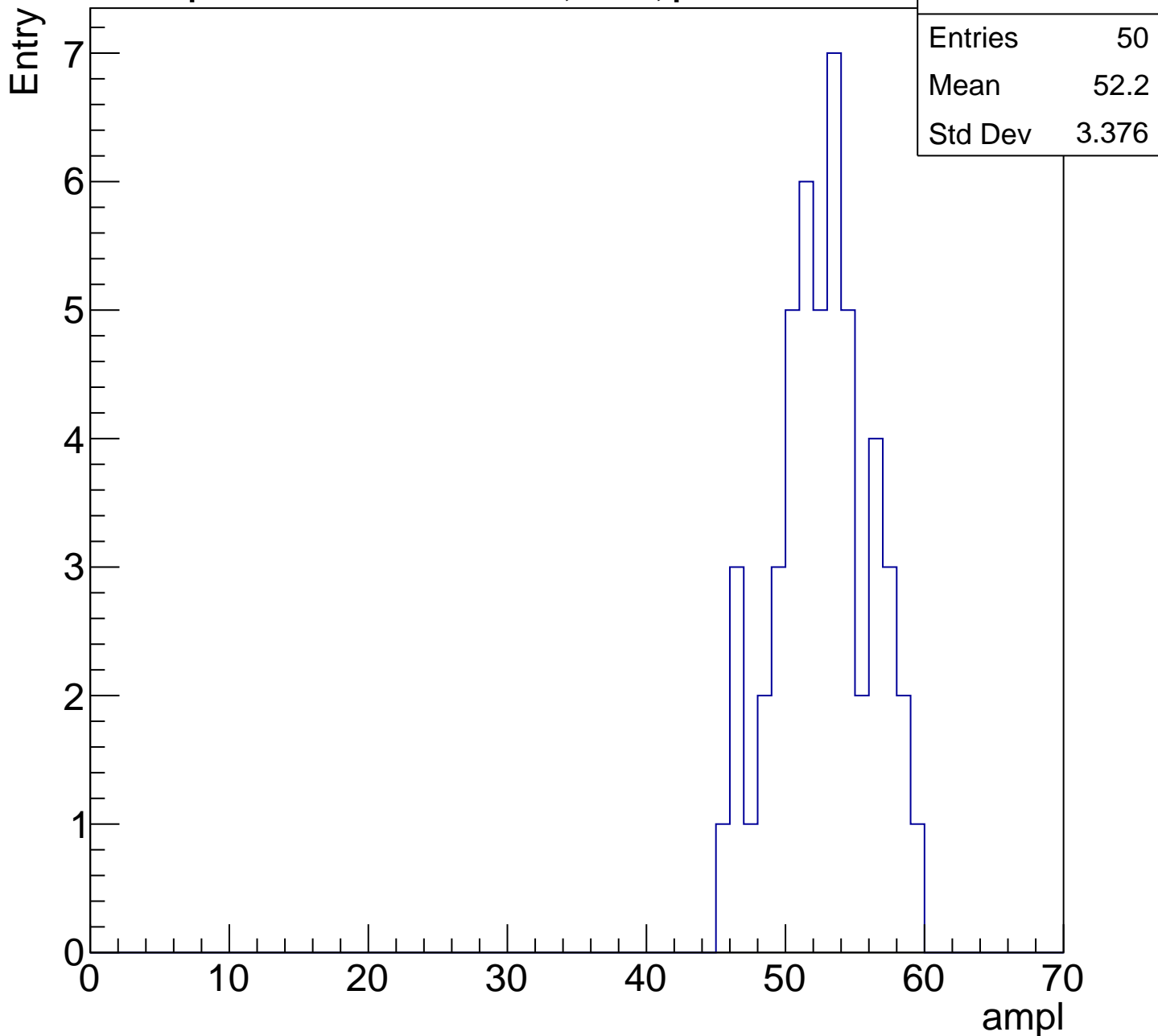
Entry

Entries	64
Mean	46.77
Std Dev	2.983



B1L103S, U7-ch38, adc4

calib_packv5_041523_1651.root, FC#0, port C2

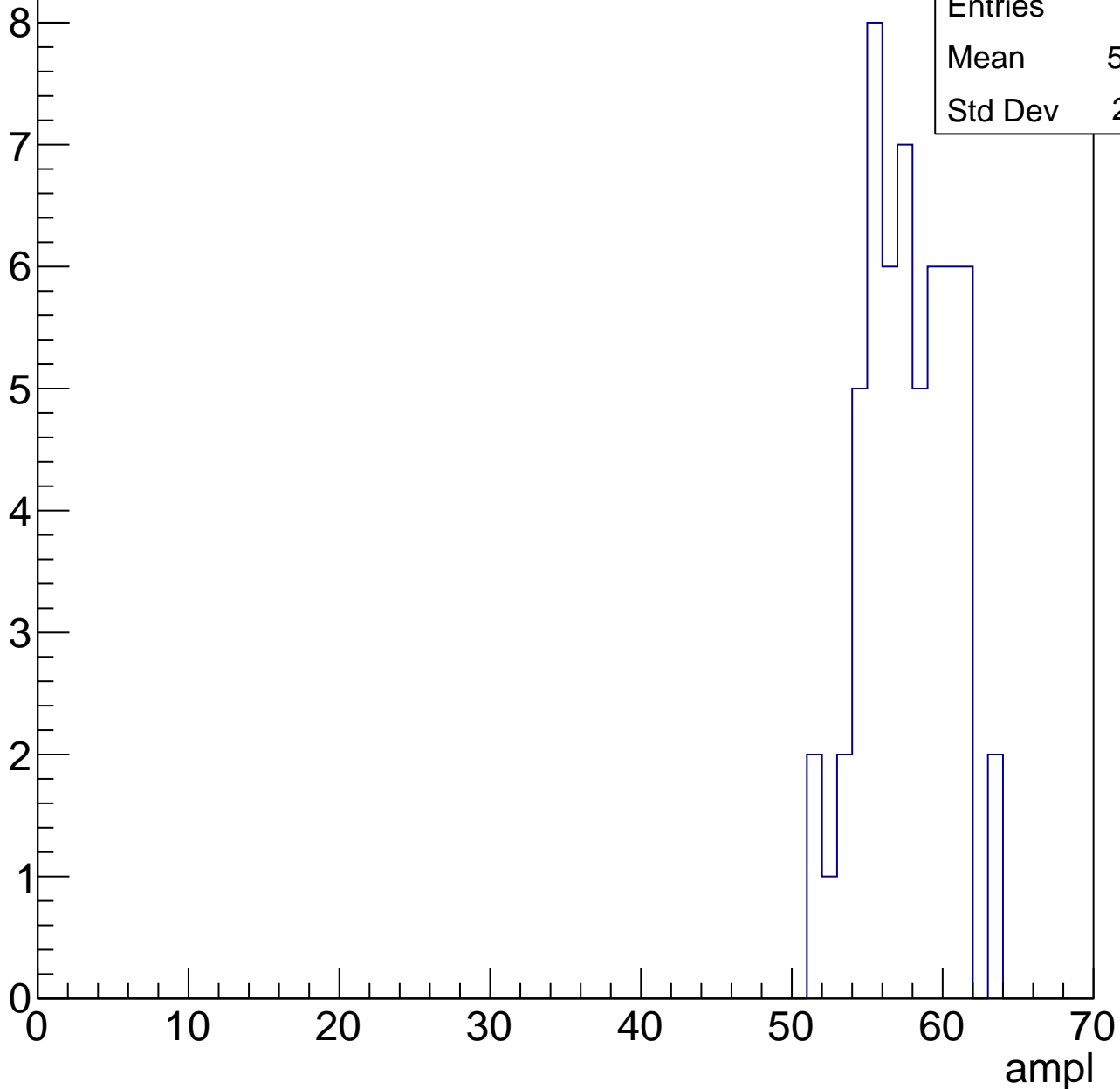


B1L103S, U7-ch38, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	57.16
Std Dev	2.871

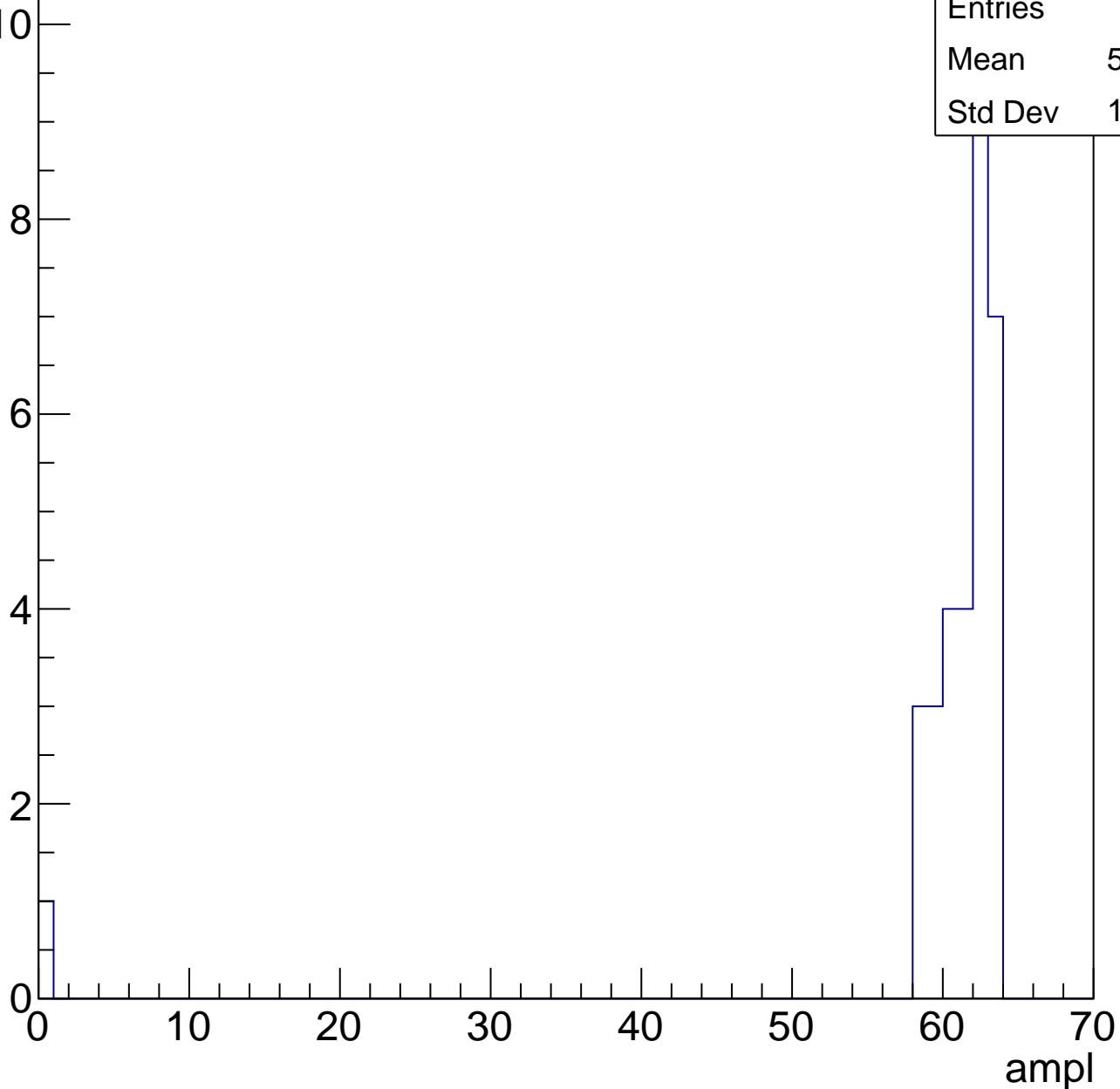


B1L103S, U7-ch38, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	32
Mean	59.25
Std Dev	10.76

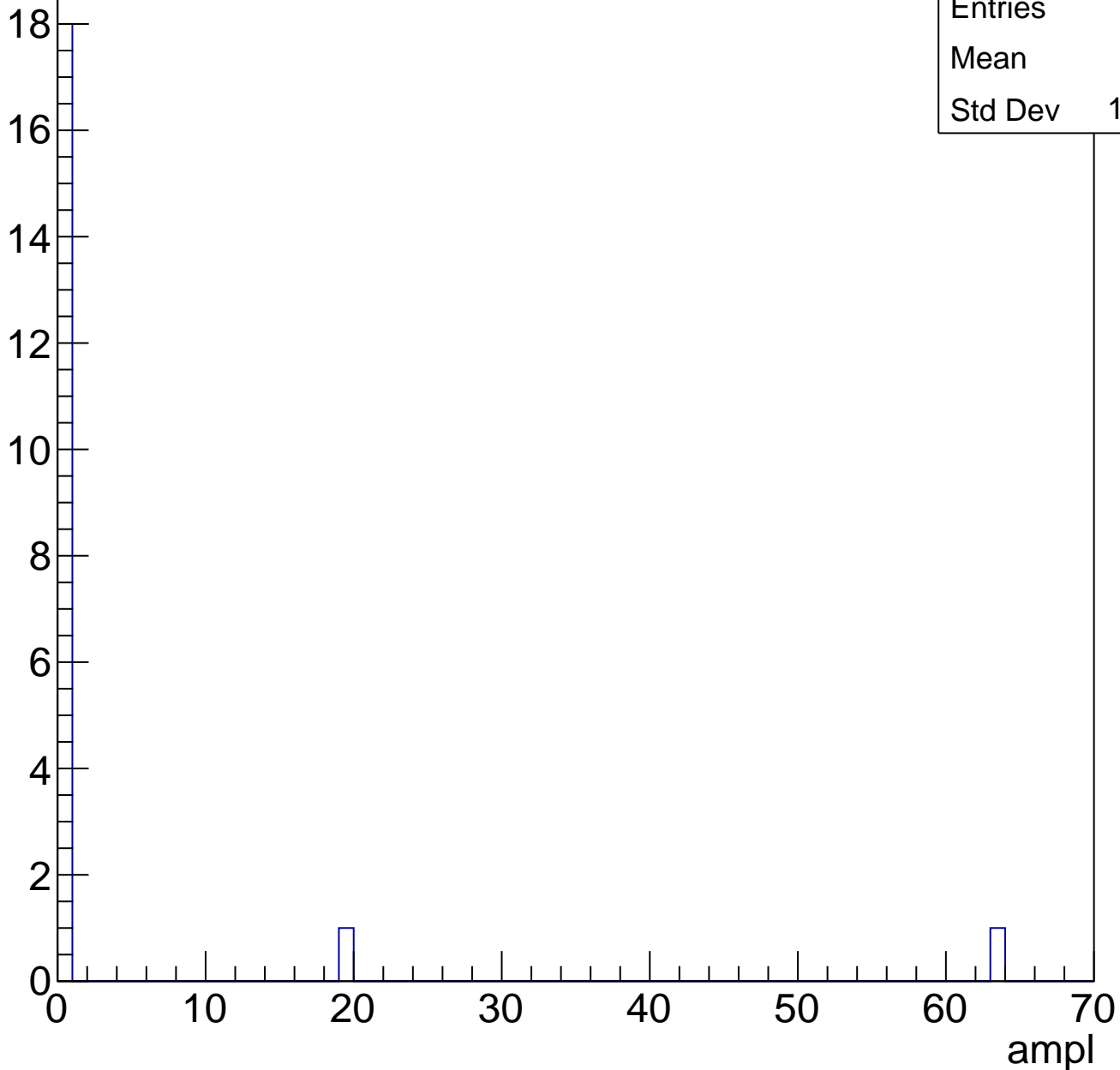


B1L103S, U7-ch38, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	4.1
Std Dev	14.13

Entry



B1L103S, U7-ch39, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	22.15
Std Dev	13.19

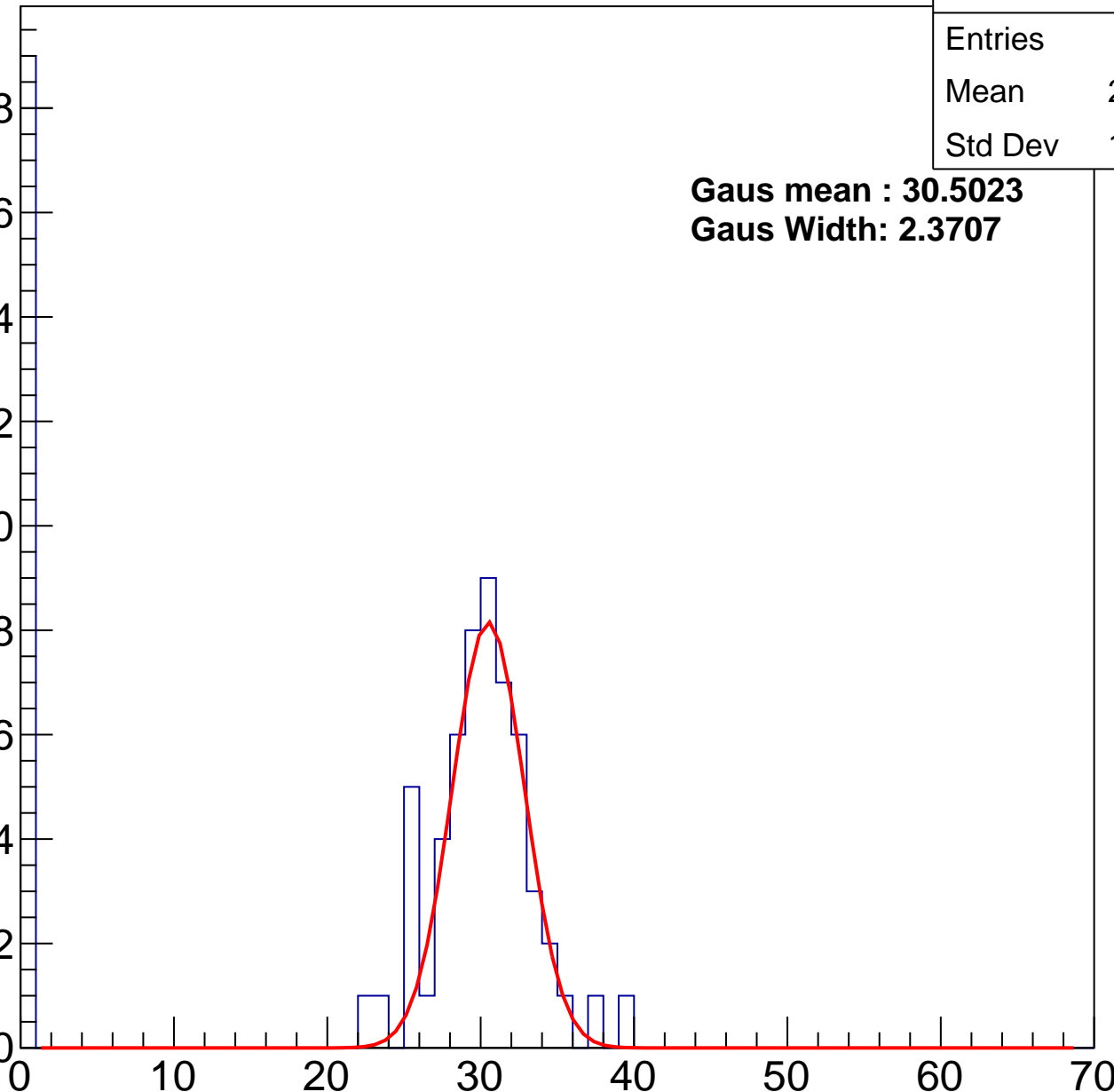
Gaus mean : 30.5023

Gaus Width: 2.3707

Entry

18
16
14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch39, adc1

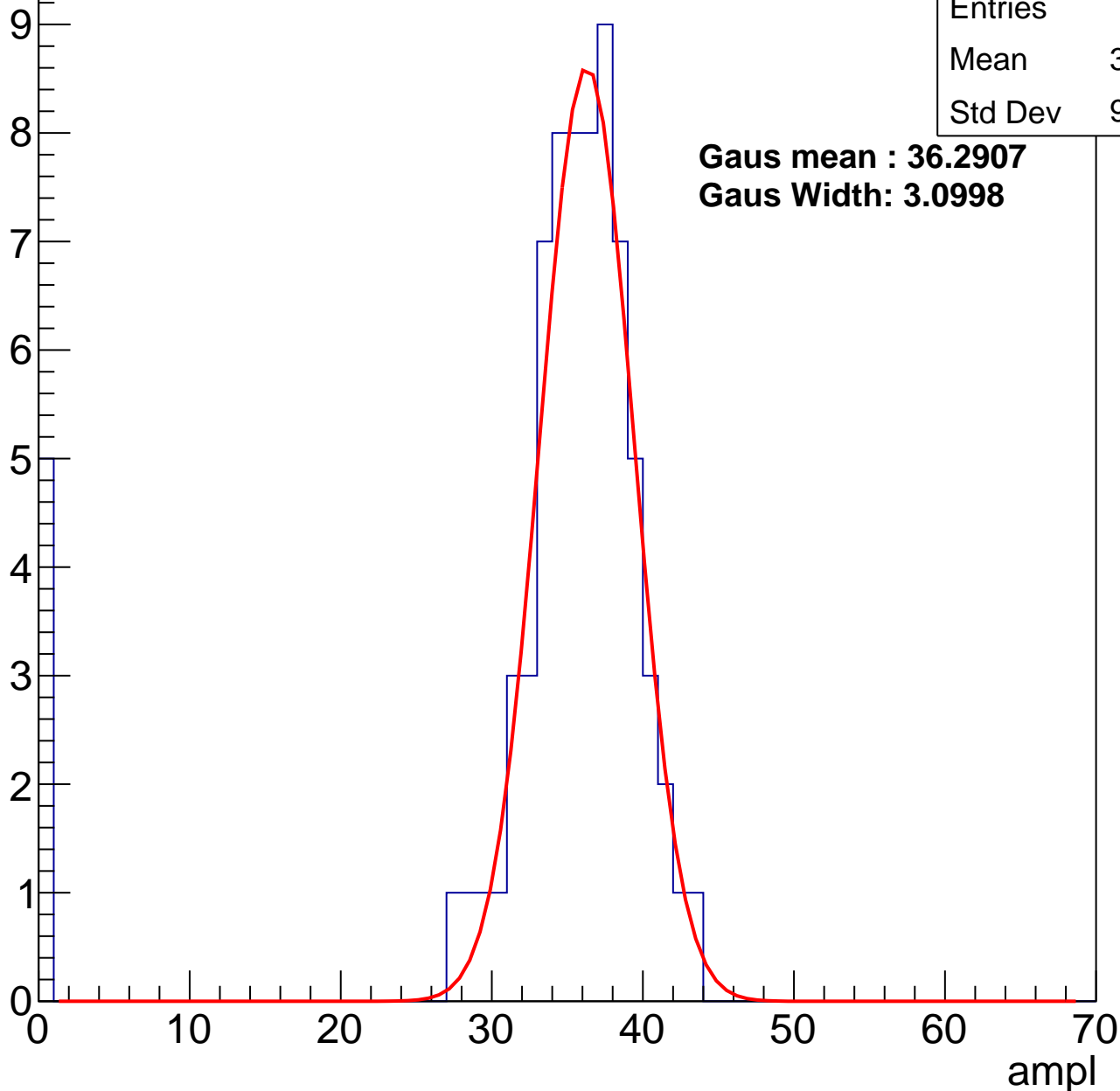
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	33.18
Std Dev	9.452

Gaus mean : 36.2907

Gaus Width: 3.0998



B1L103S, U7-ch39, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

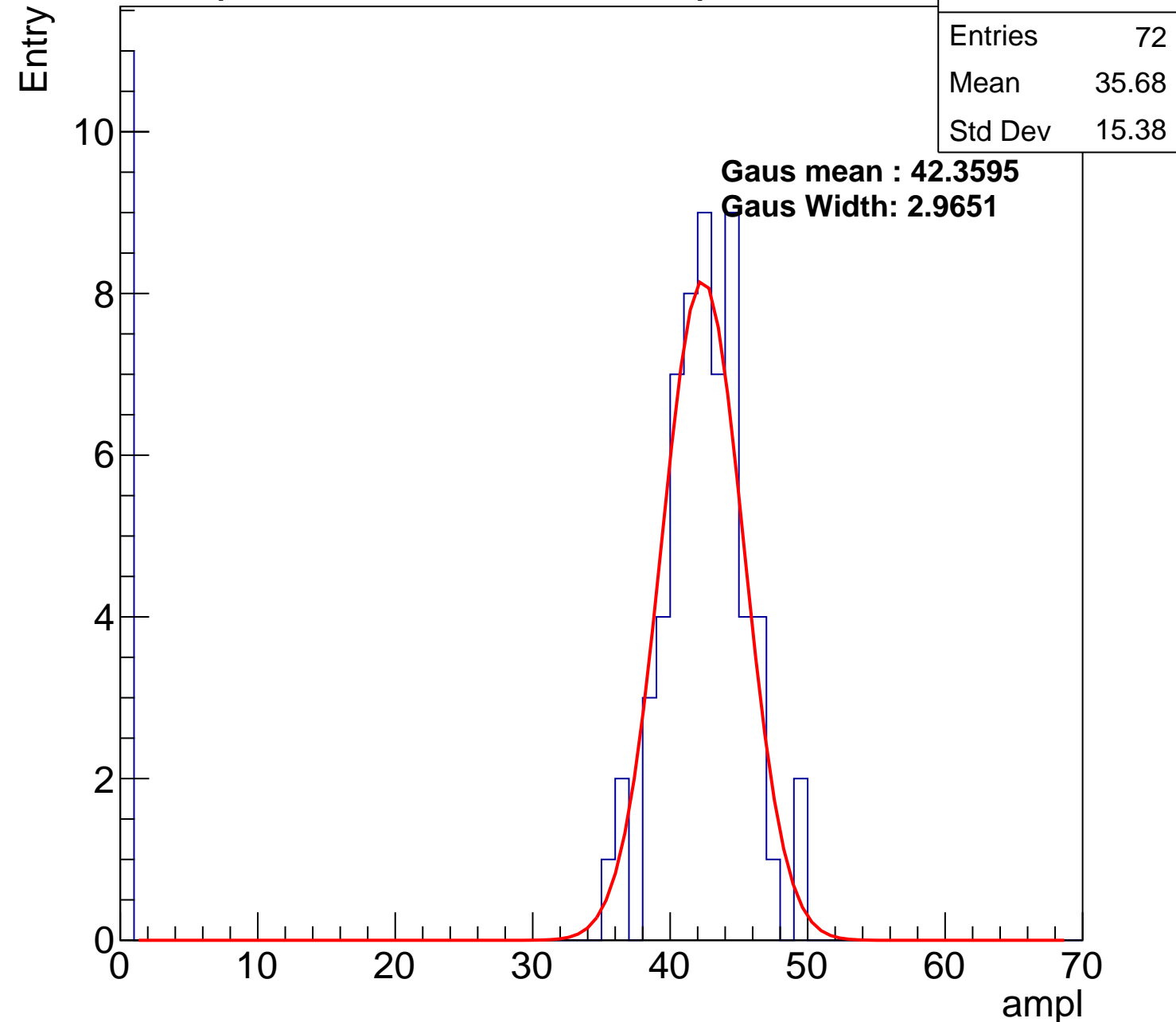
70

ampl

Entries	72
Mean	35.68
Std Dev	15.38

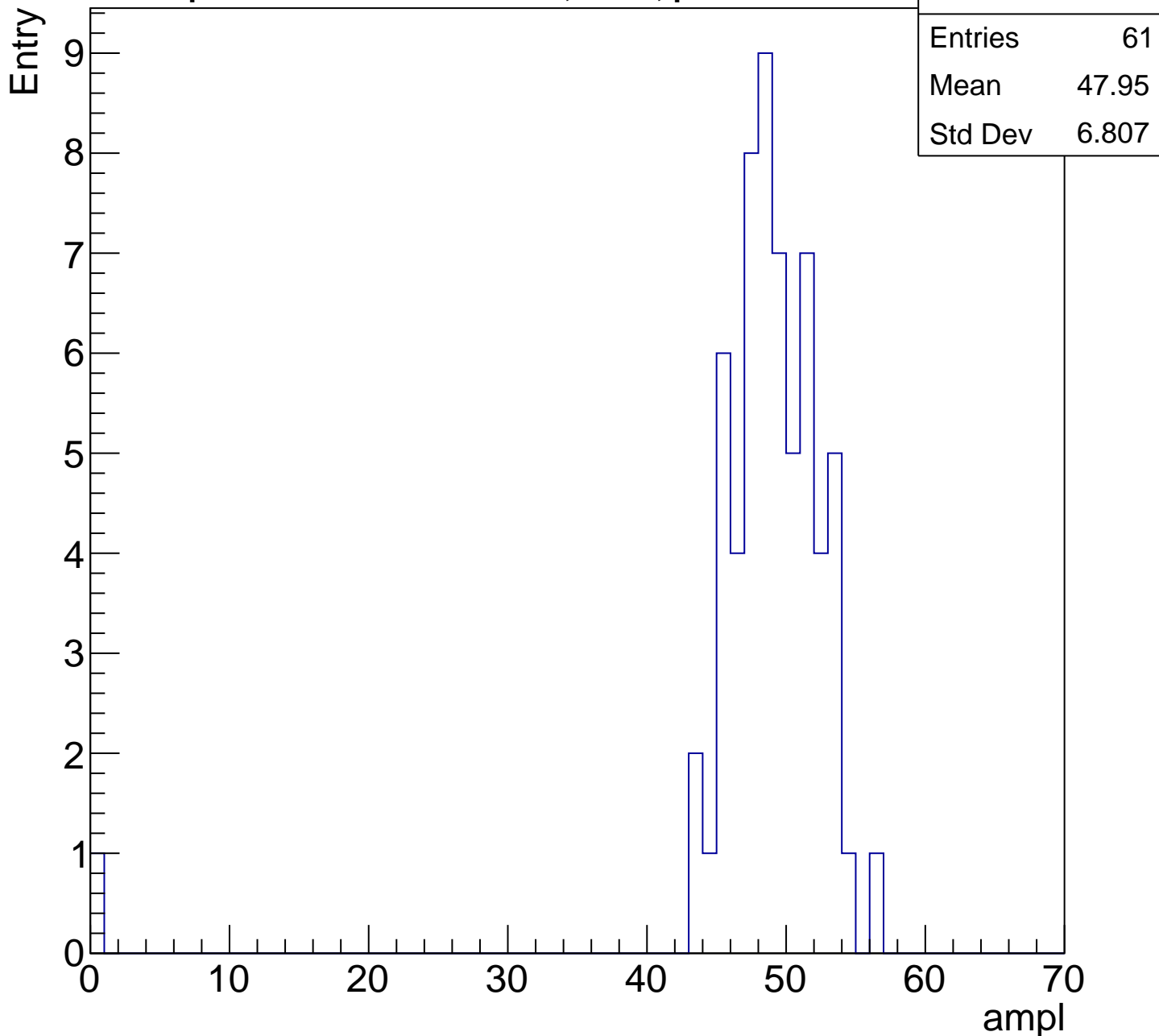
Gaus mean : 42.3595

Gaus Width: 2.9651



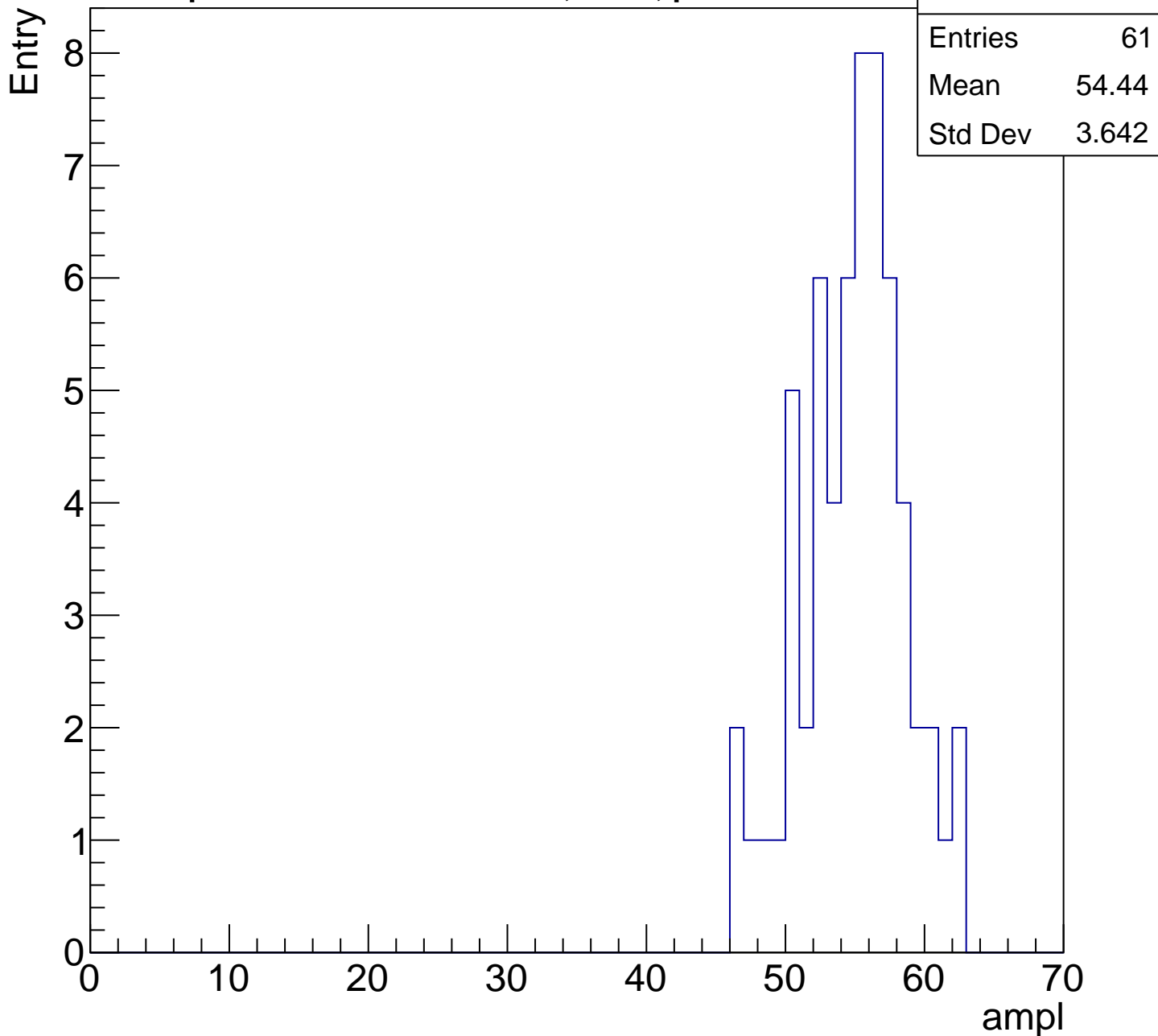
B1L103S, U7-ch39, adc3

calib_packv5_041523_1651.root, FC#0, port C2



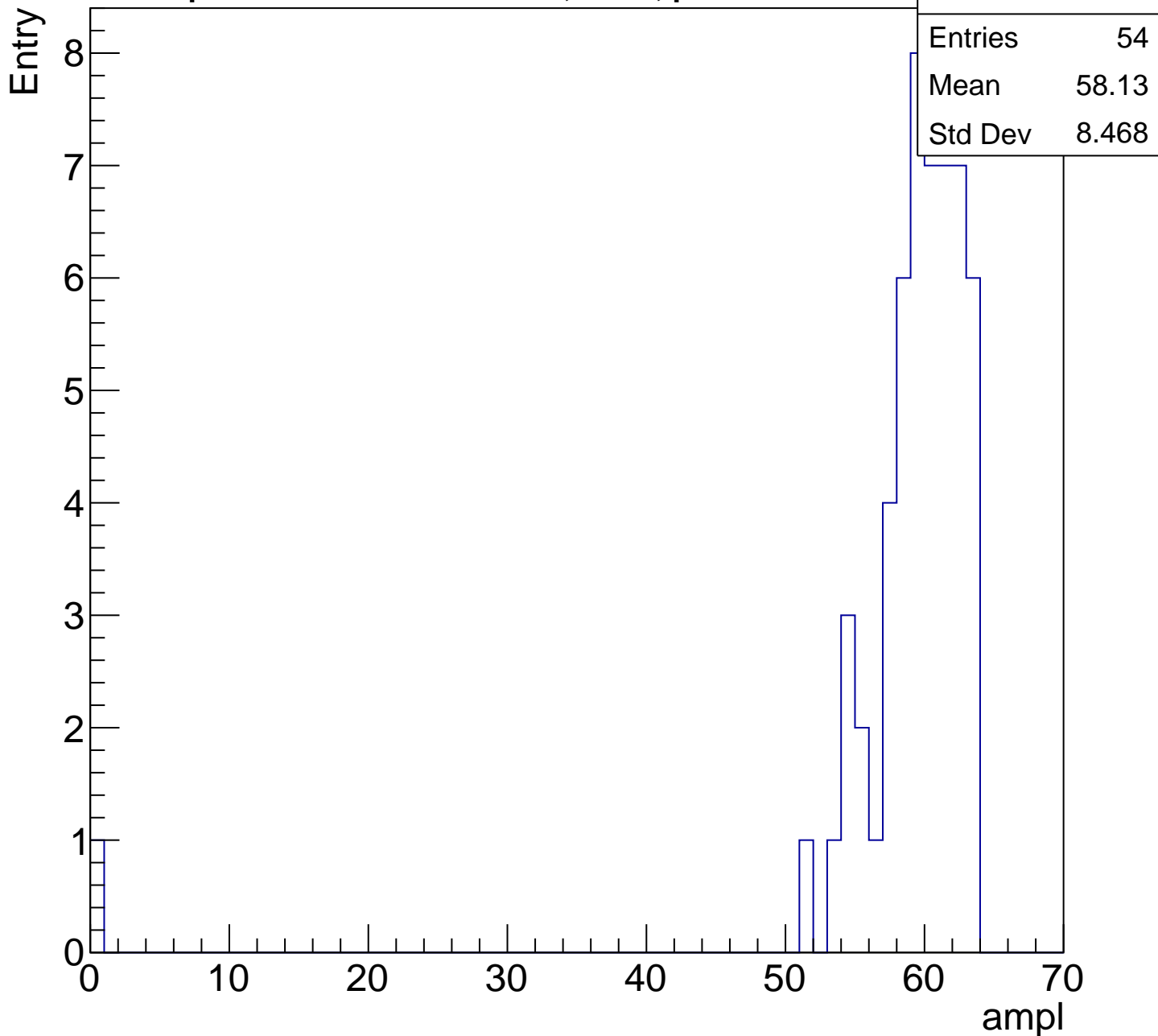
B1L103S, U7-ch39, adc4

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U7-ch39, adc5

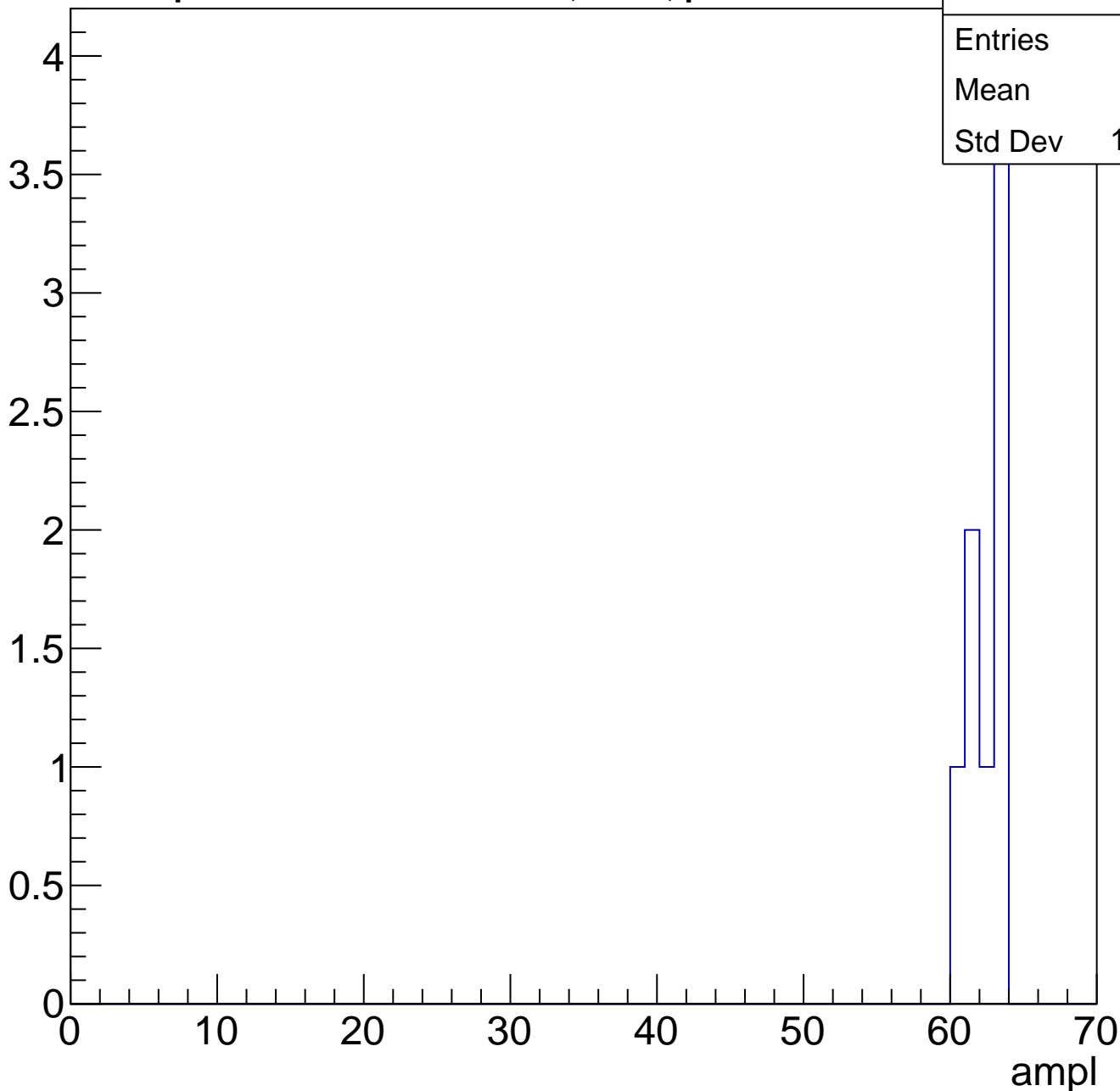
calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U7-ch39, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch39, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U7-ch40, adc0

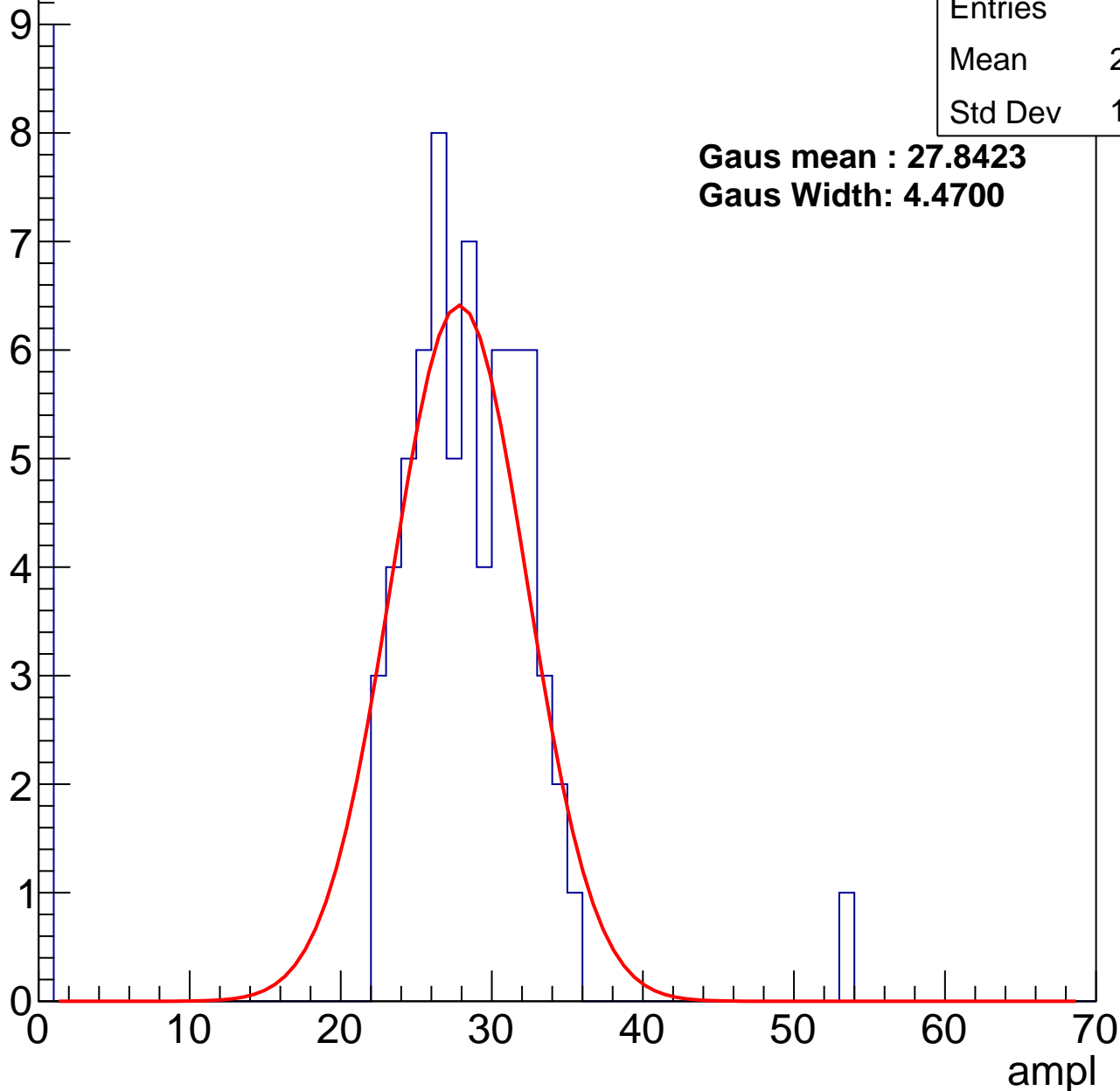
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	24.95
Std Dev	10.08

Gaus mean : 27.8423

Gaus Width: 4.4700



B1L103S, U7-ch40, adc1

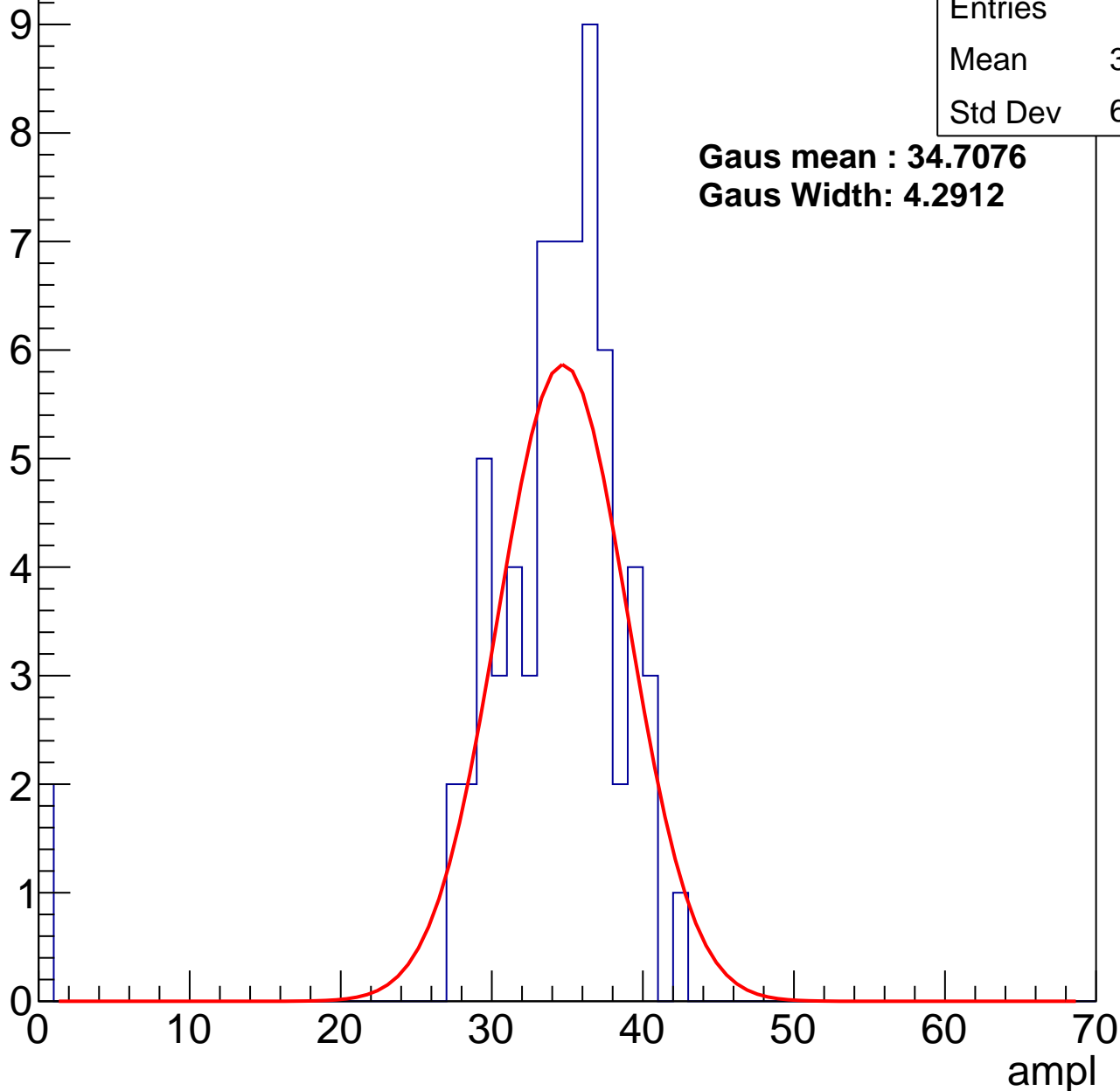
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	33.12
Std Dev	6.757

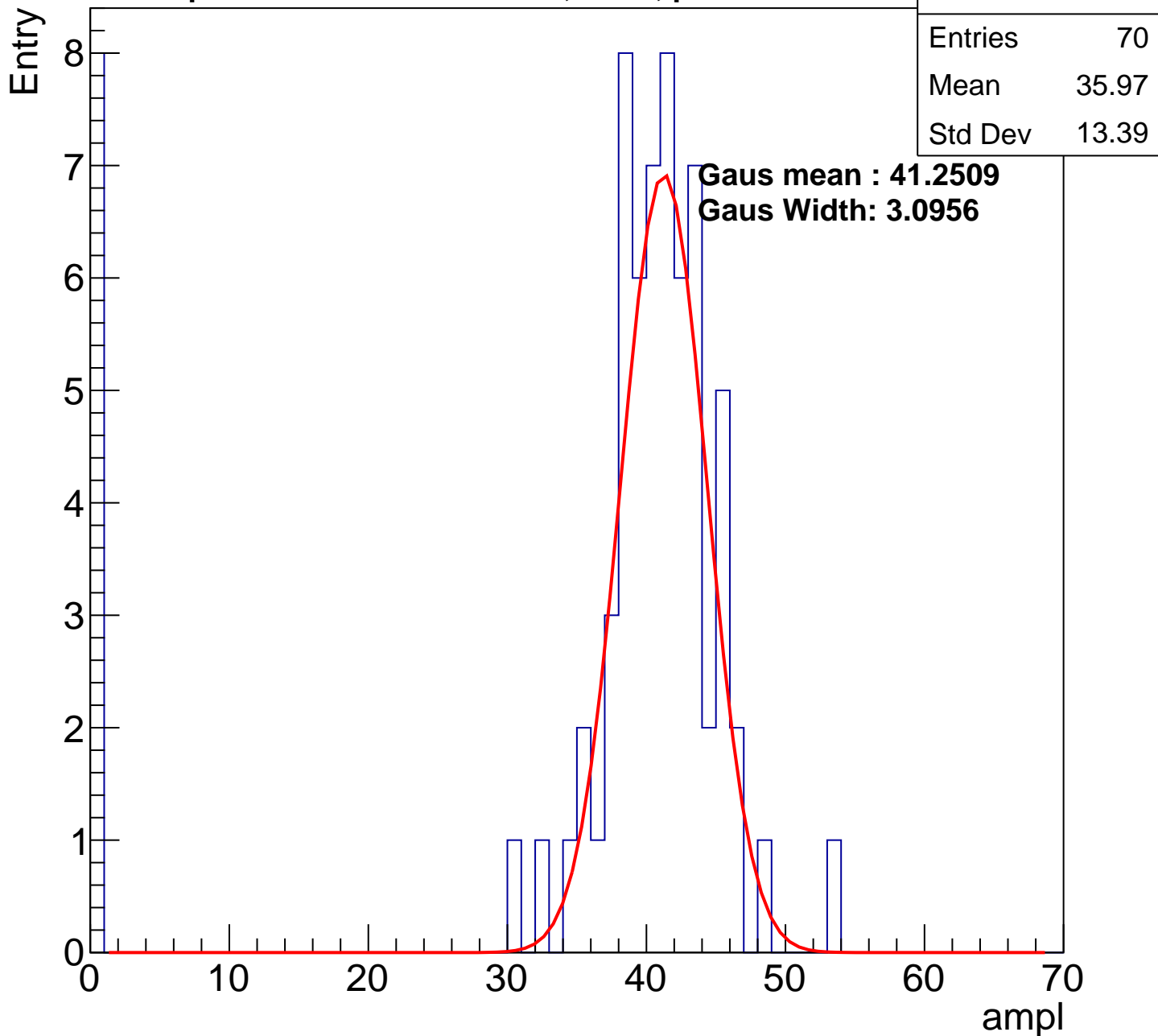
Gaus mean : 34.7076

Gaus Width: 4.2912



B1L103S, U7-ch40, adc2

calib_packv5_041523_1651.root, FC#0, port C2

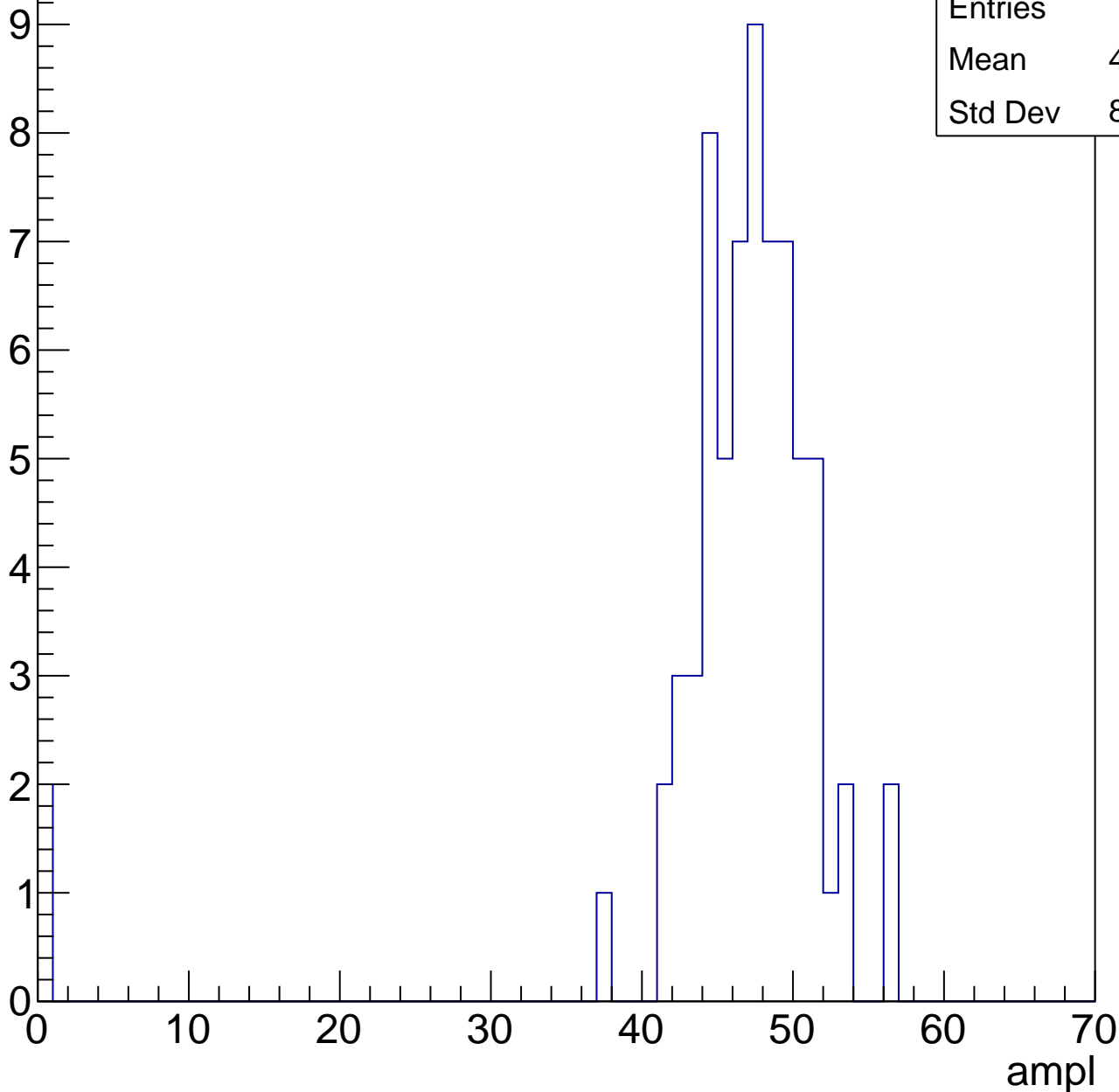


B1L103S, U7-ch40, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	45.65
Std Dev	8.602

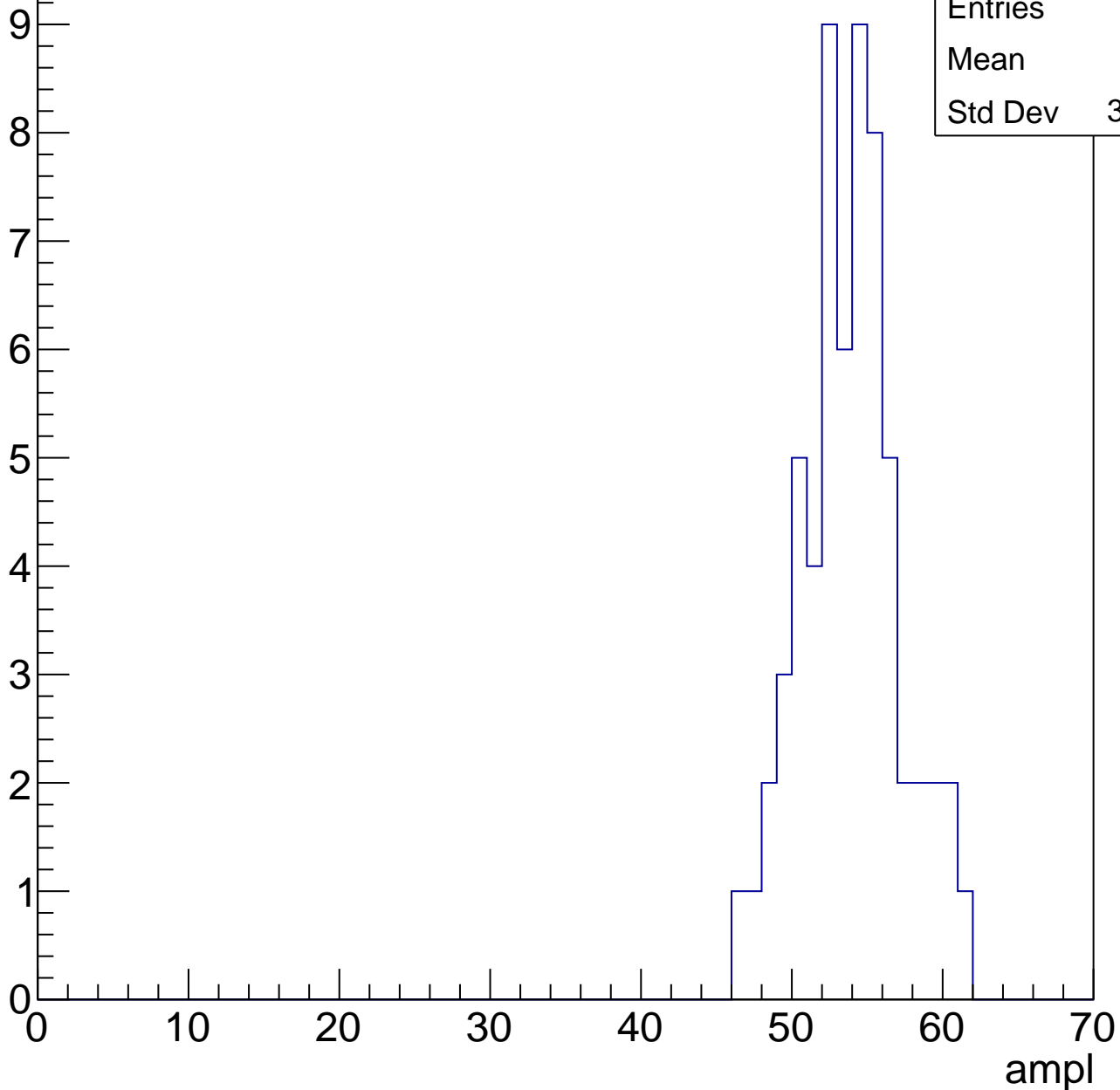


B1L103S, U7-ch40, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	53.4
Std Dev	3.225

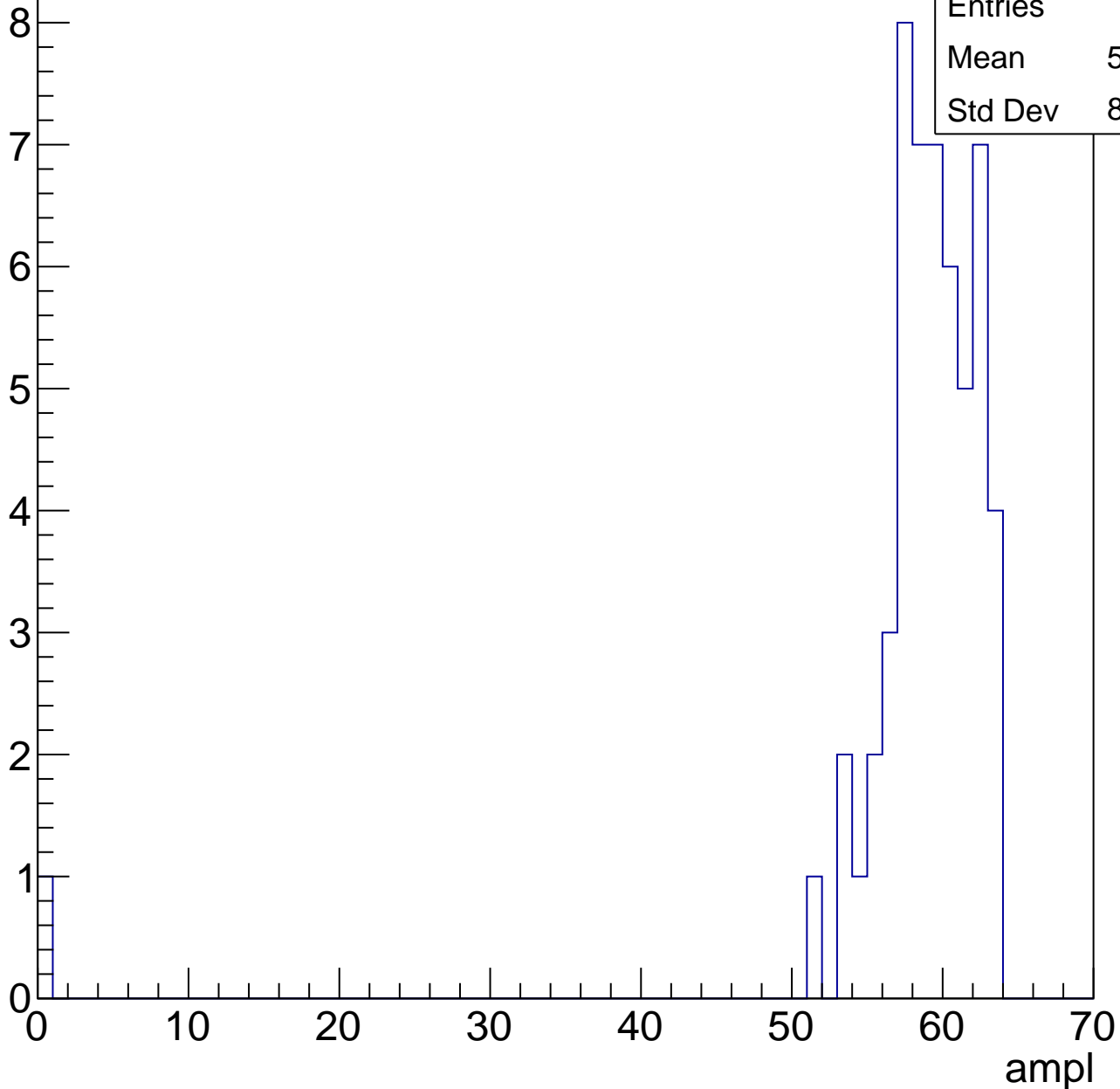


B1L103S, U7-ch40, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	57.69
Std Dev	8.388

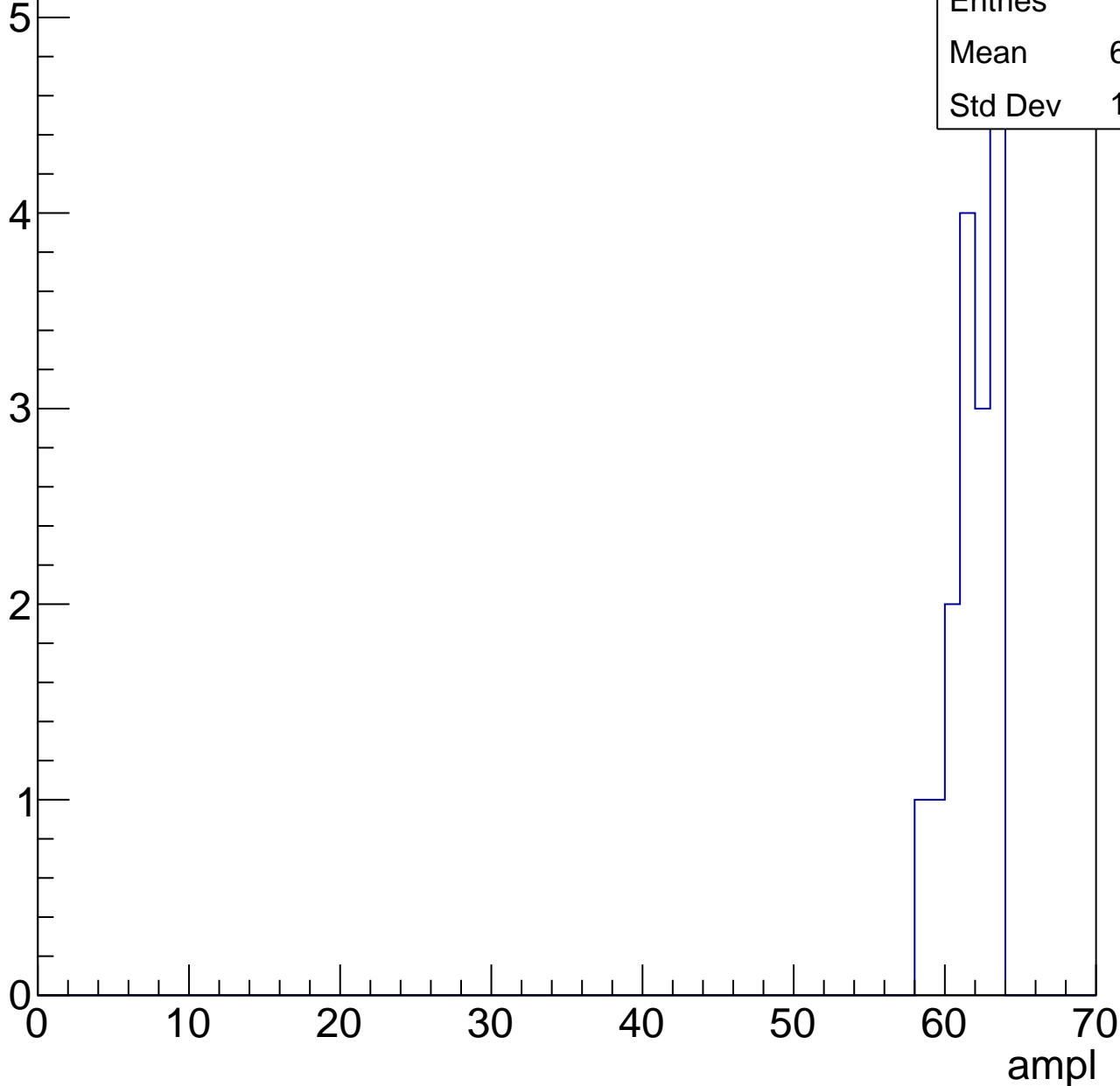


B1L103S, U7-ch40, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	16
Mean	61.38
Std Dev	1.495



B1L103S, U7-ch40, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry



B1L103S, U7-ch41, adc0

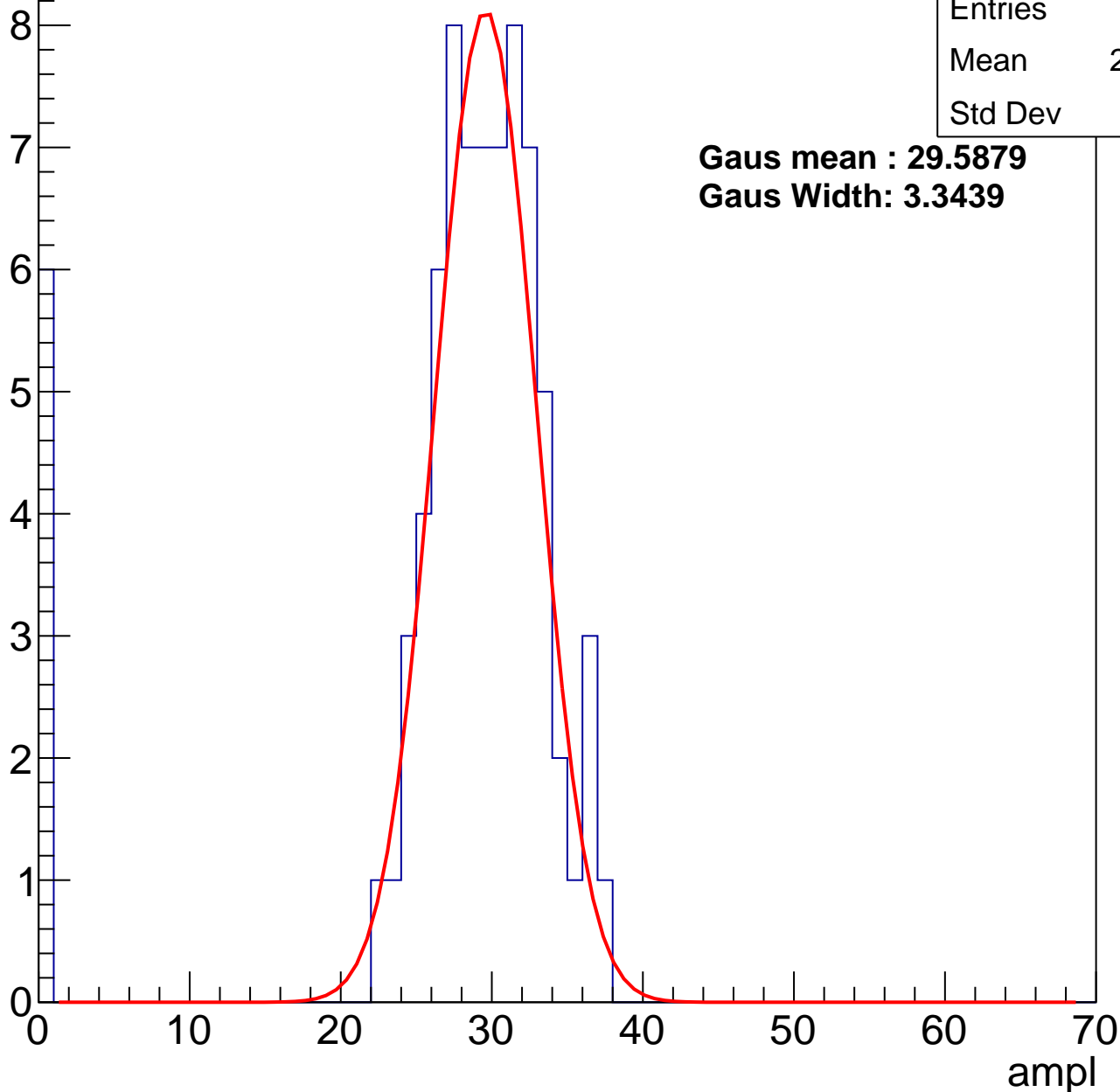
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	27.05
Std Dev	8.49

Gaus mean : 29.5879

Gaus Width: 3.3439



B1L103S, U7-ch41, adc1

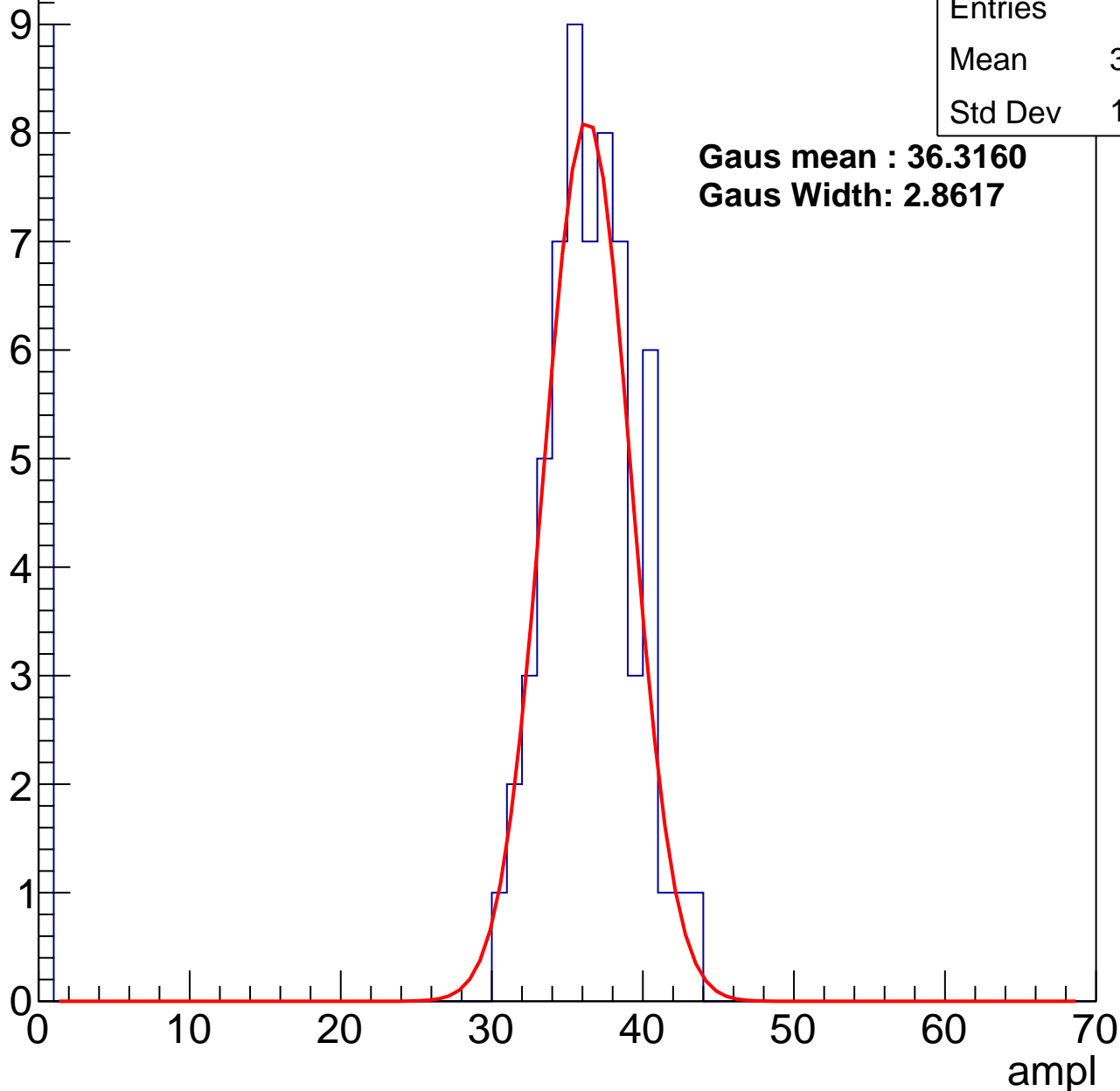
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	31.47
Std Dev	12.37

Gaus mean : 36.3160

Gaus Width: 2.8617



B1L103S, U7-ch41, adc2

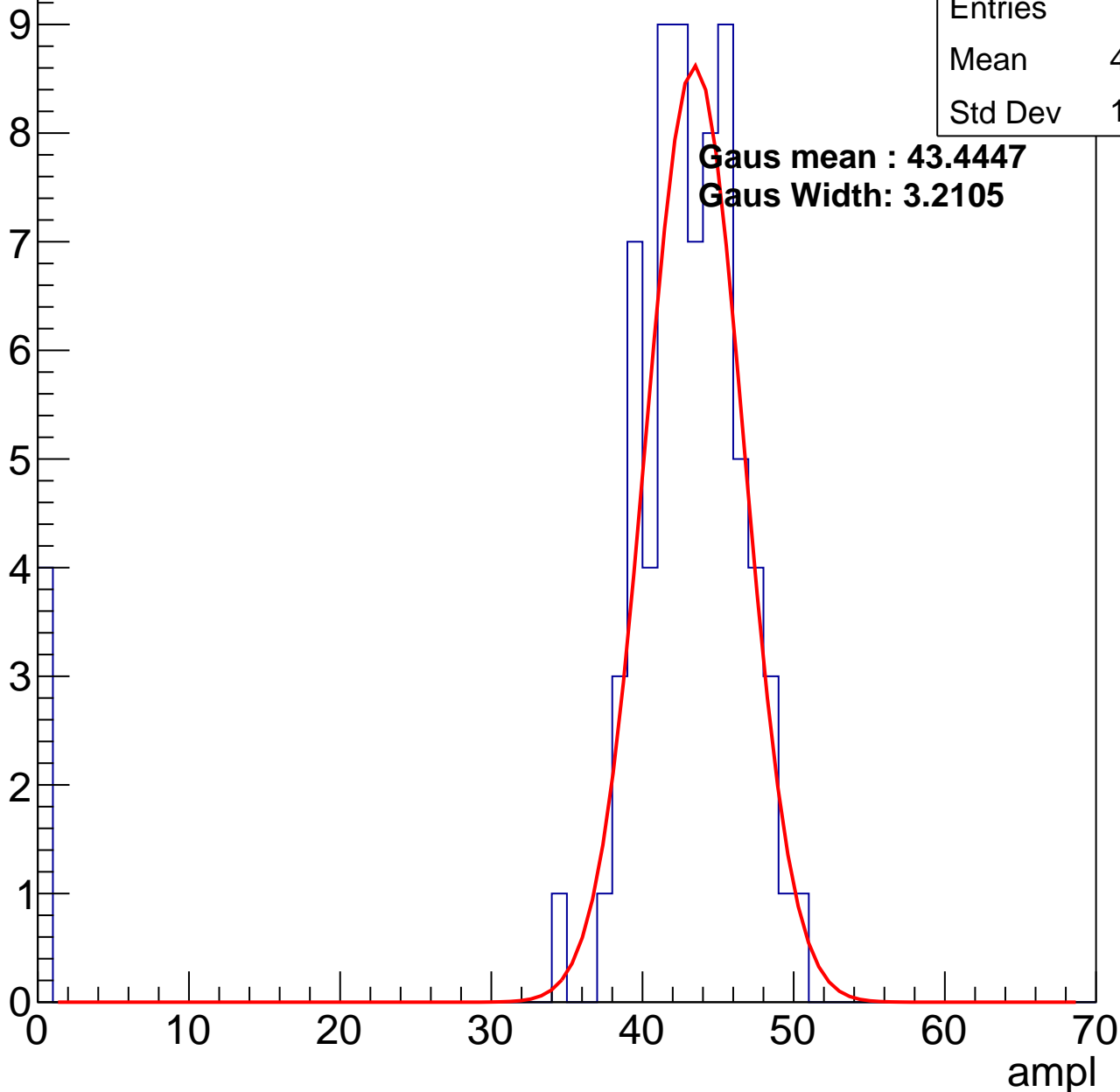
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	40.58
Std Dev	10.03

Gaus mean : 43.4447

Gaus Width: 3.2105



B1L103S, U7-ch41, adc3

calib_packv5_041523_1651.root, FC#0, port C2

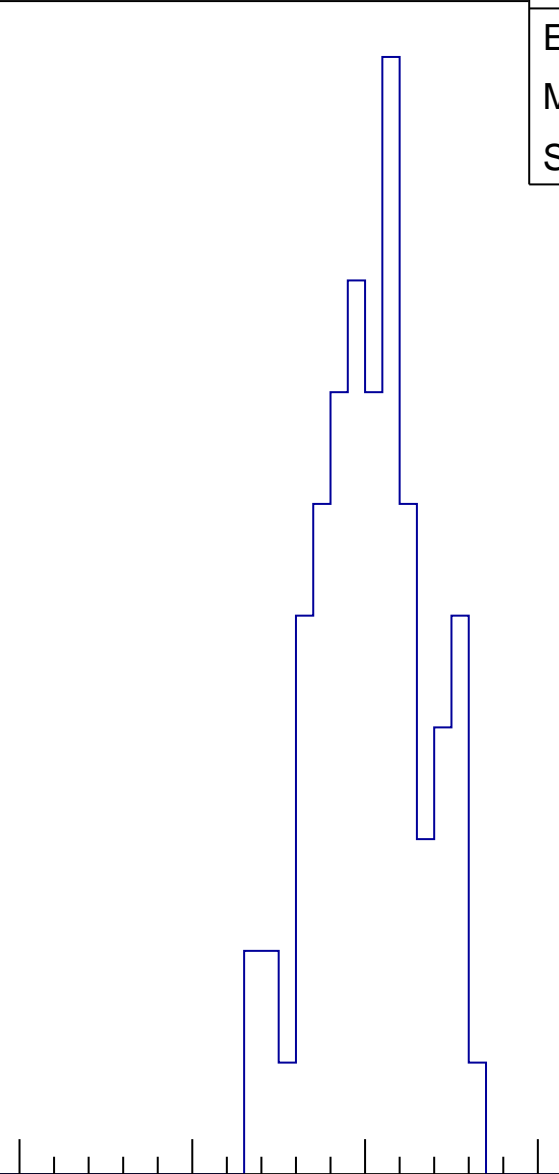
Entries	67
Mean	49.81
Std Dev	3.111

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

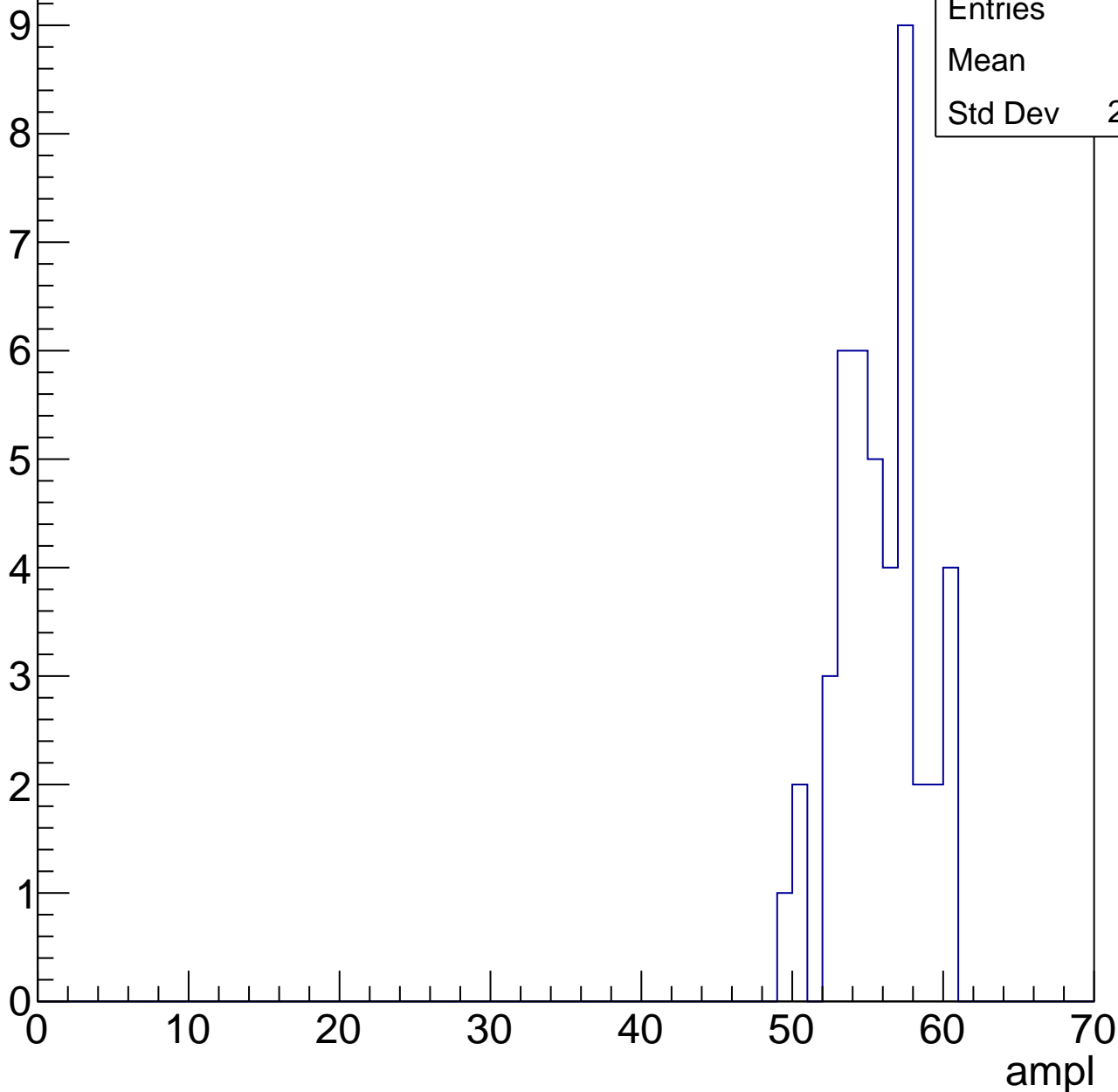


B1L103S, U7-ch41, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	44
Mean	55.3
Std Dev	2.735

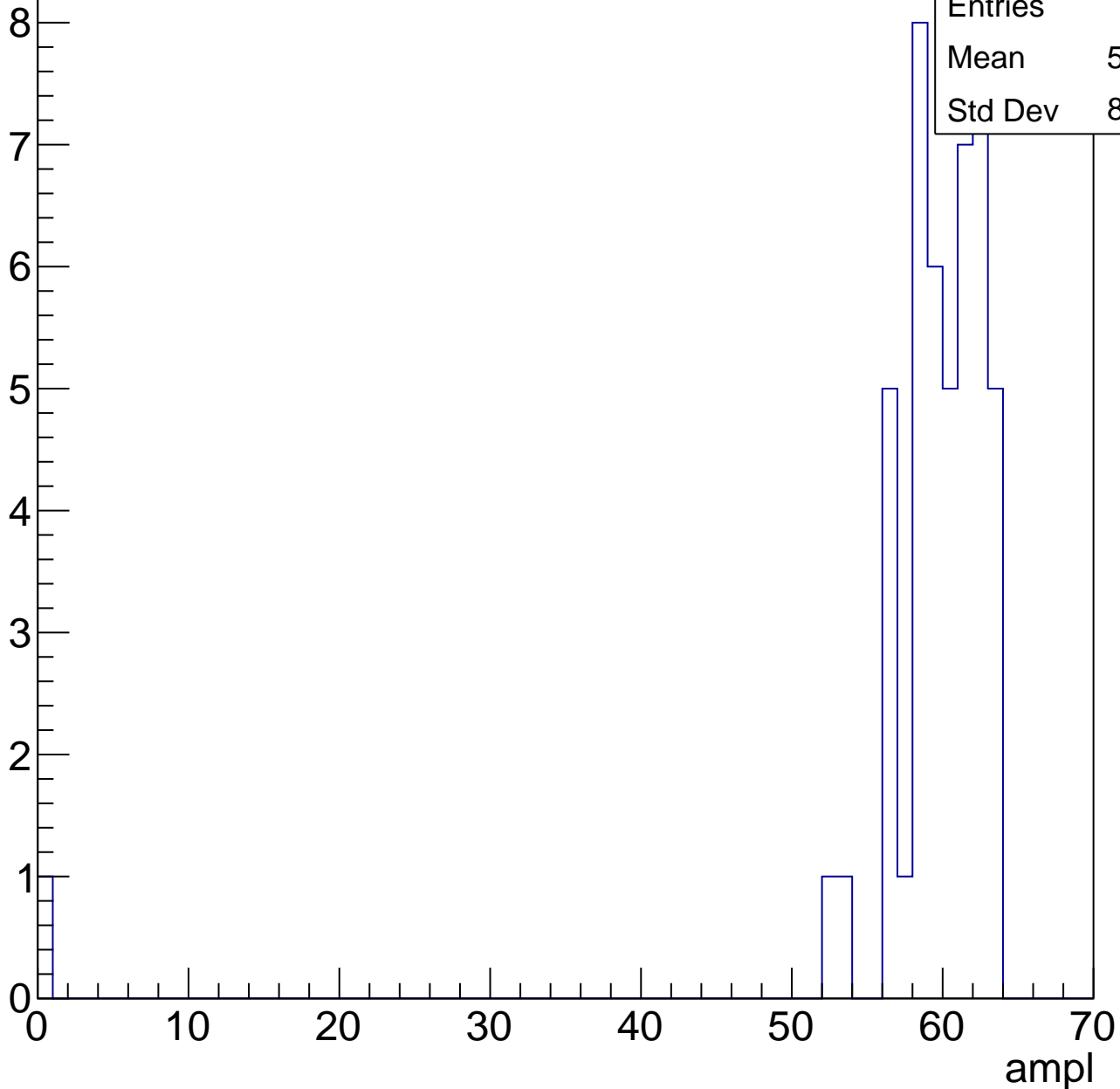


B1L103S, U7-ch41, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	48
Mean	58.29
Std Dev	8.879

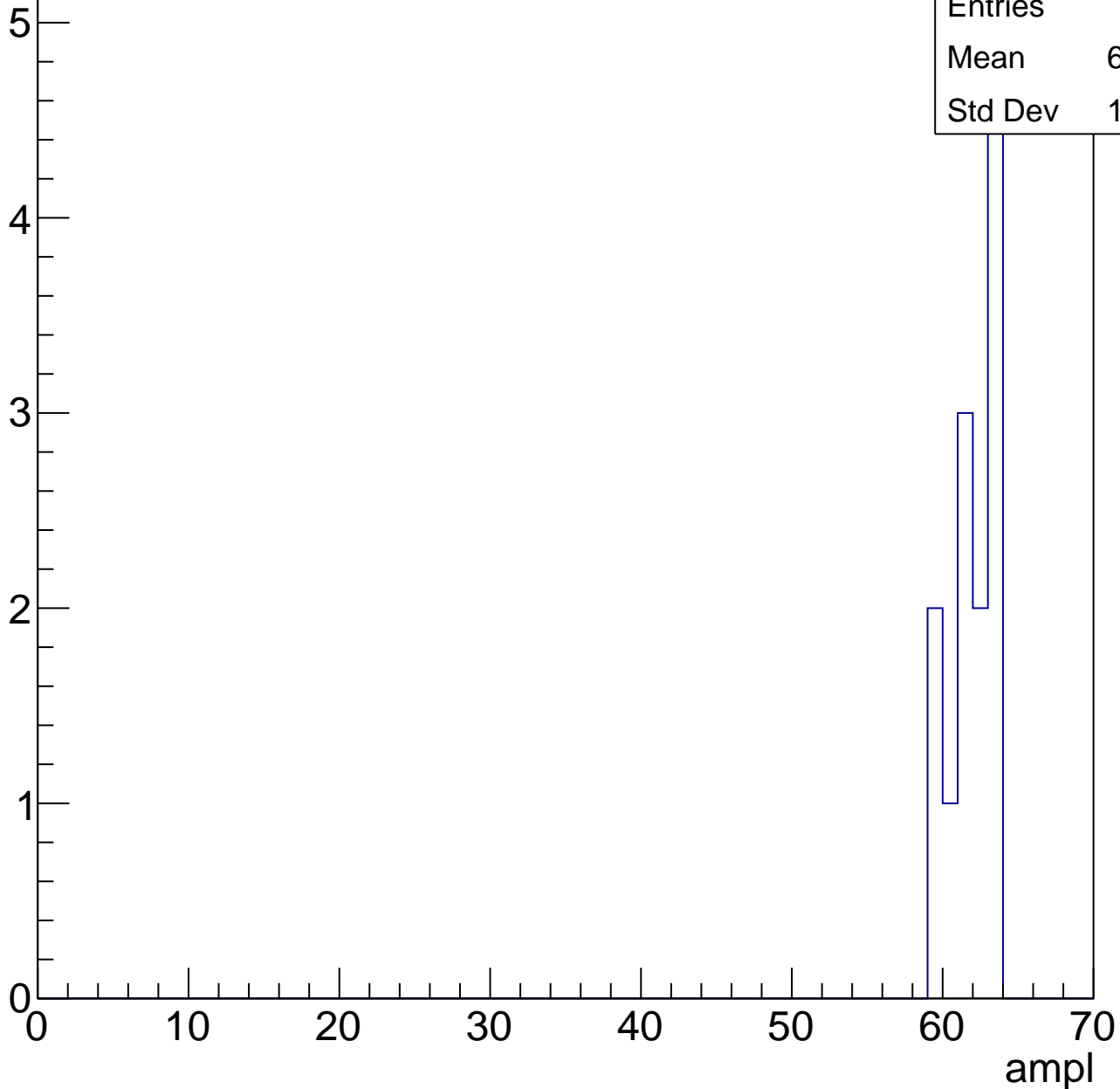


B1L103S, U7-ch41, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	13
Mean	61.54
Std Dev	1.447



B1L103S, U7-ch41, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.105
Std Dev	4.689

Entry



B1L103S, U7-ch42, adc0

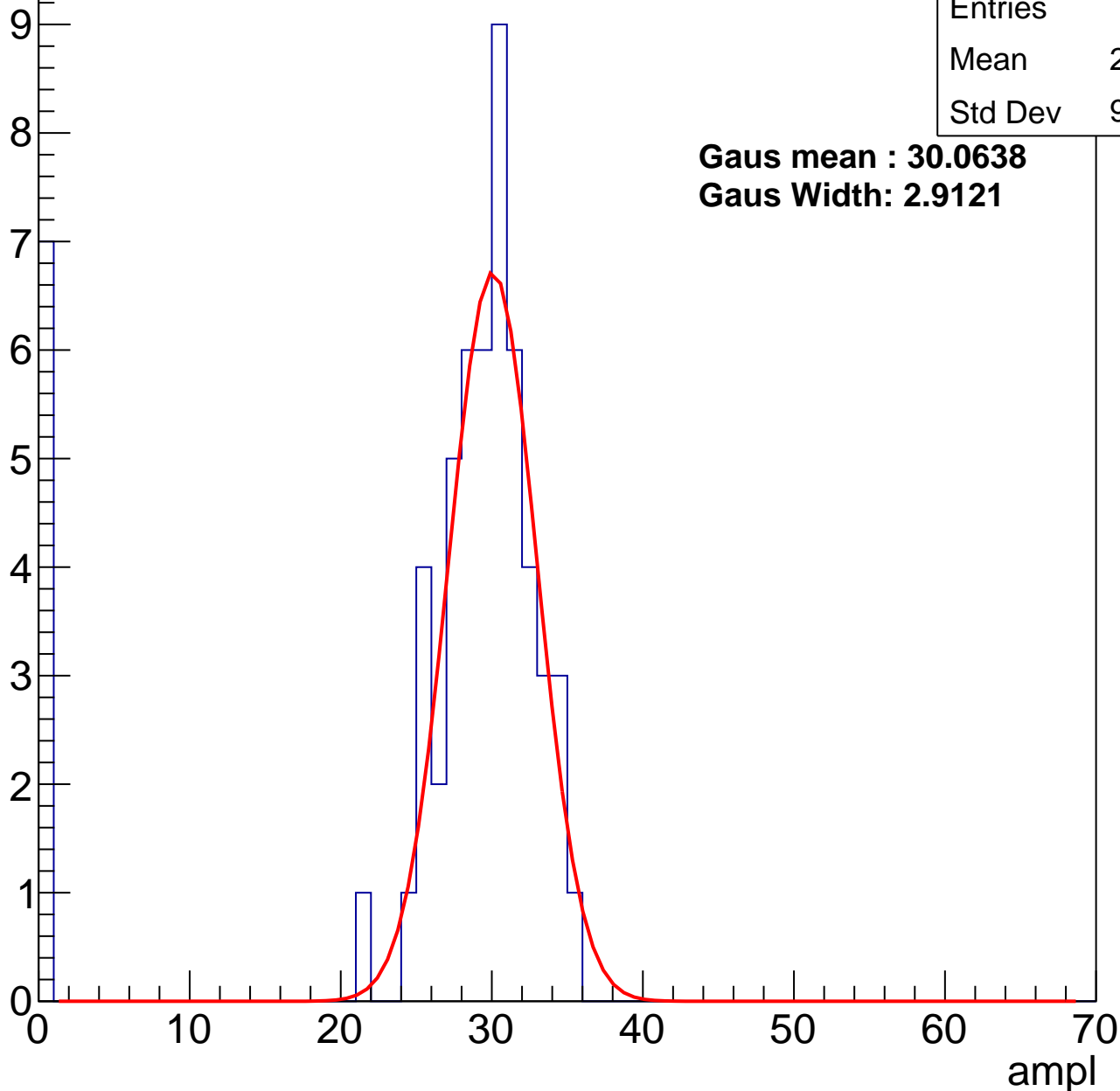
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	25.76
Std Dev	9.916

Gaus mean : 30.0638

Gaus Width: 2.9121



B1L103S, U7-ch42, adc1

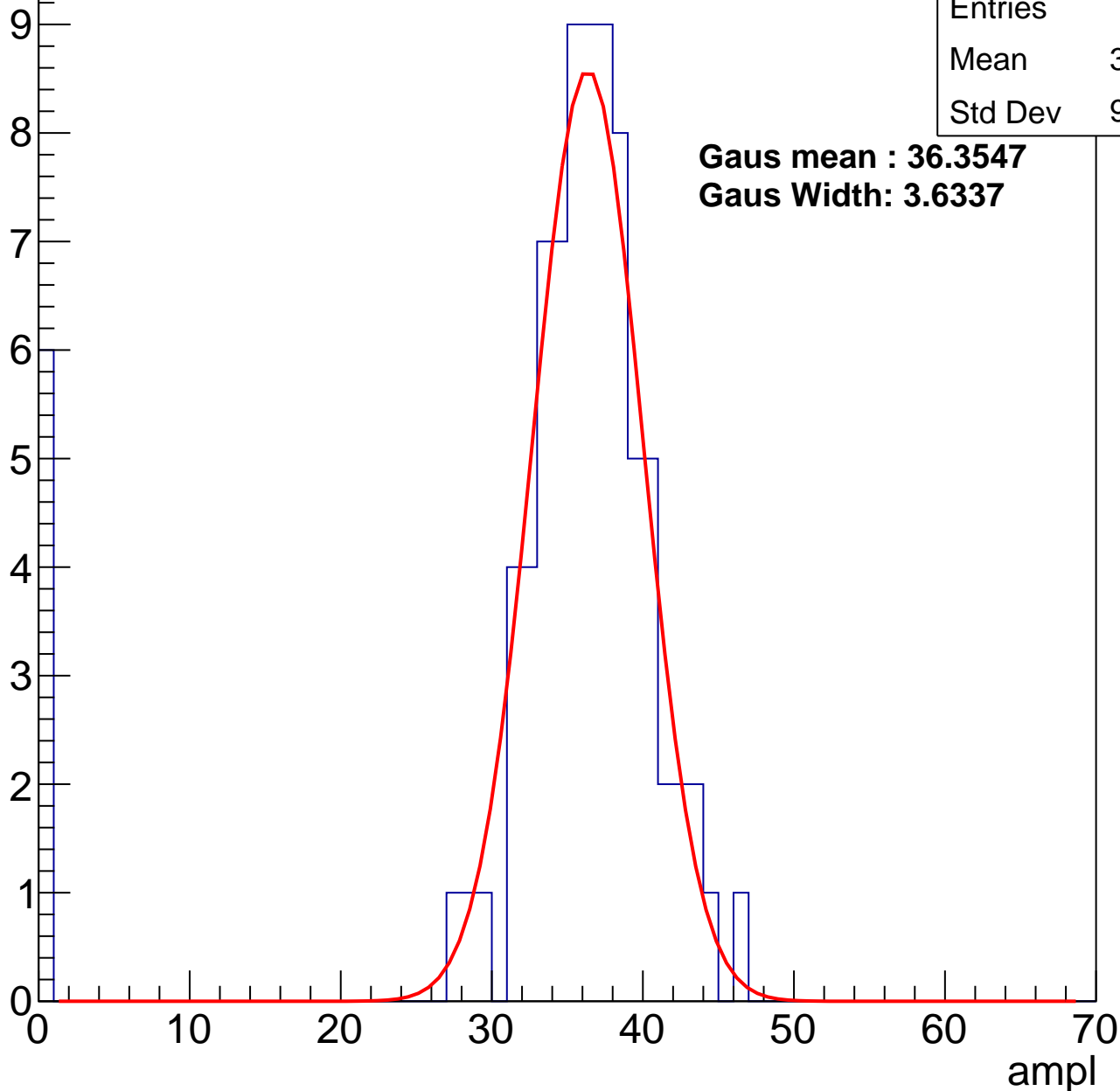
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	84
Mean	33.55
Std Dev	9.928

Gaus mean : 36.3547

Gaus Width: 3.6337



B1L103S, U7-ch42, adc2

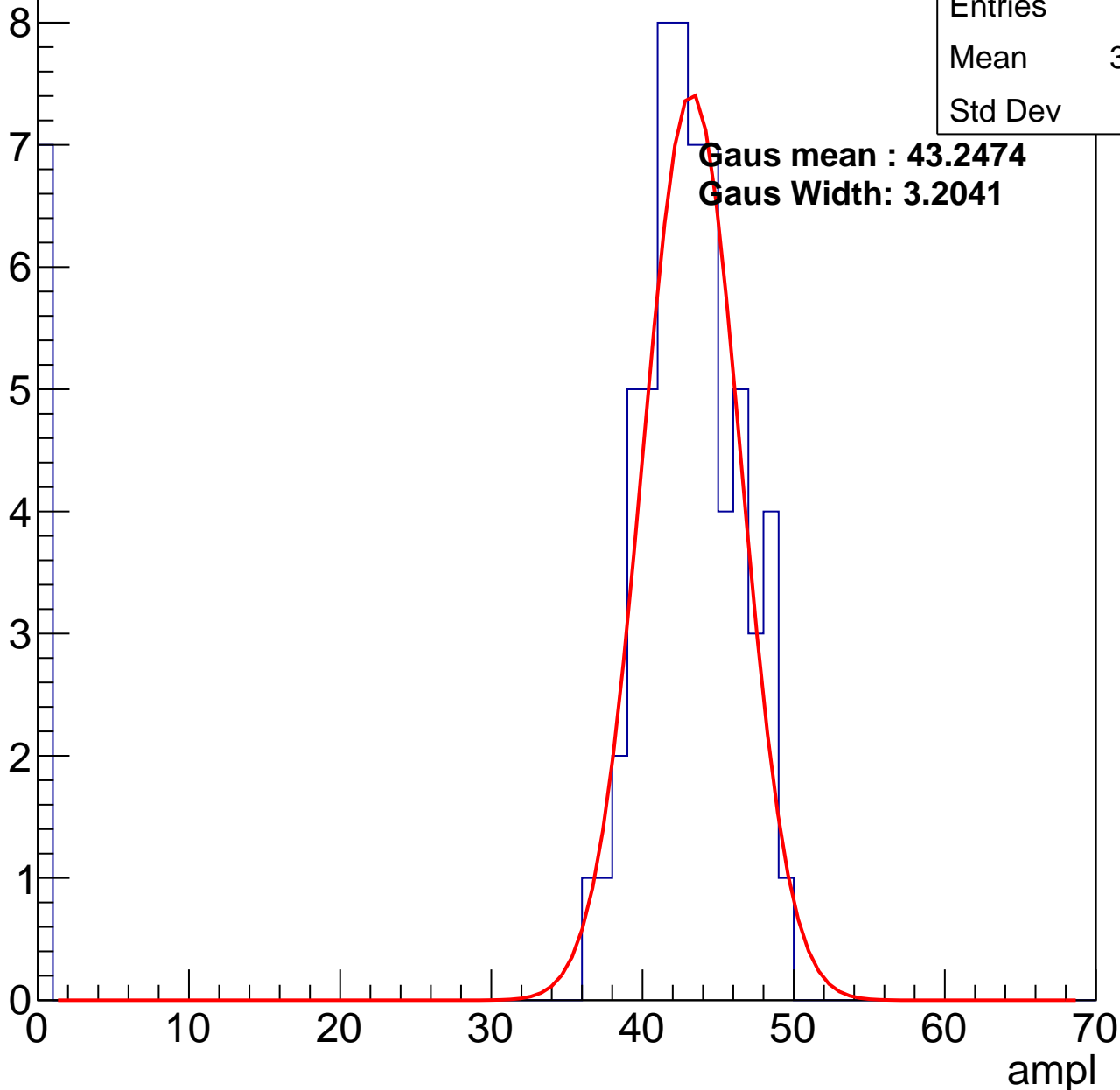
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	38.37
Std Dev	13.3

Gaus mean : 43.2474

Gaus Width: 3.2041

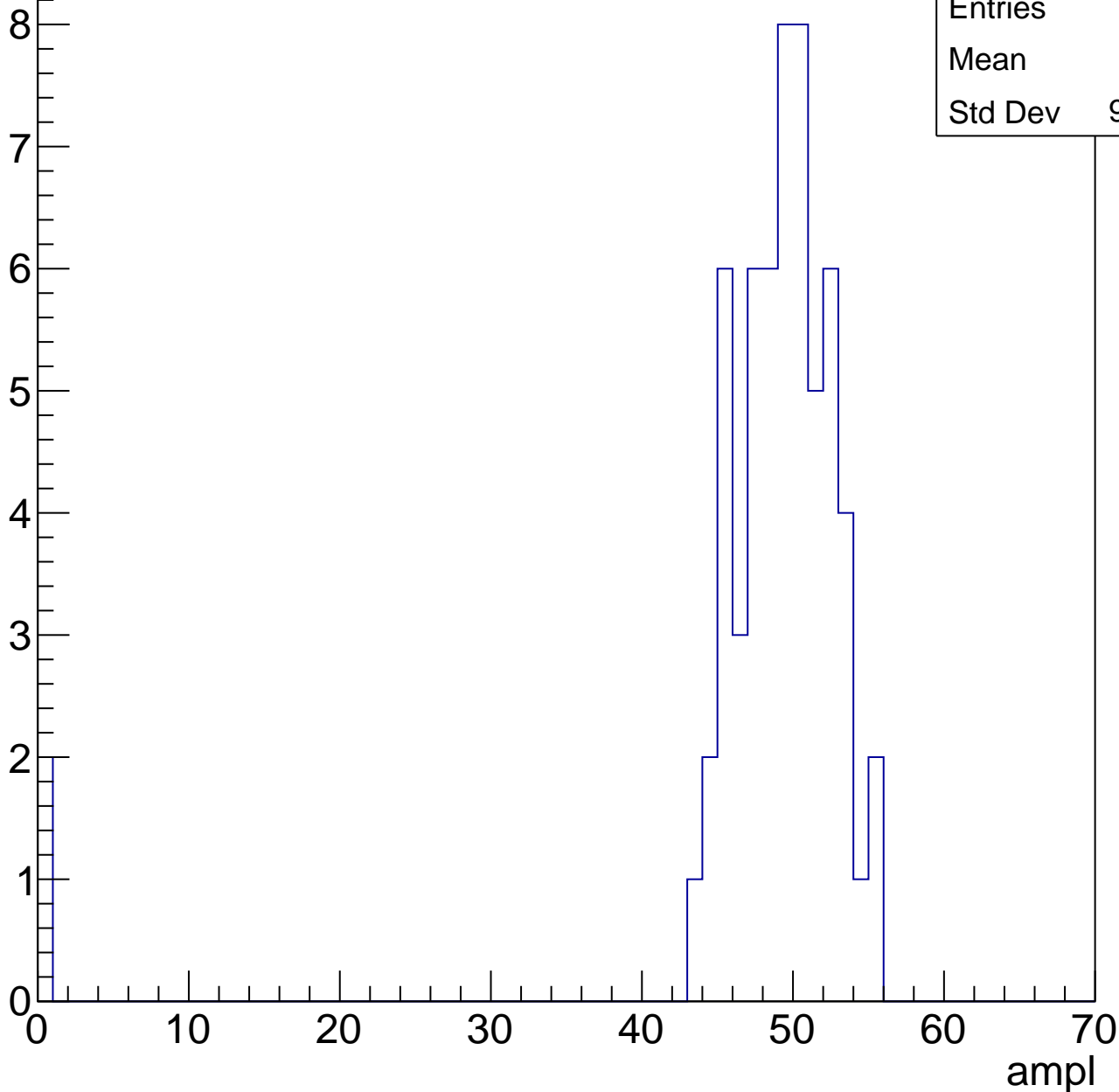


B1L103S, U7-ch42, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	47.4
Std Dev	9.247

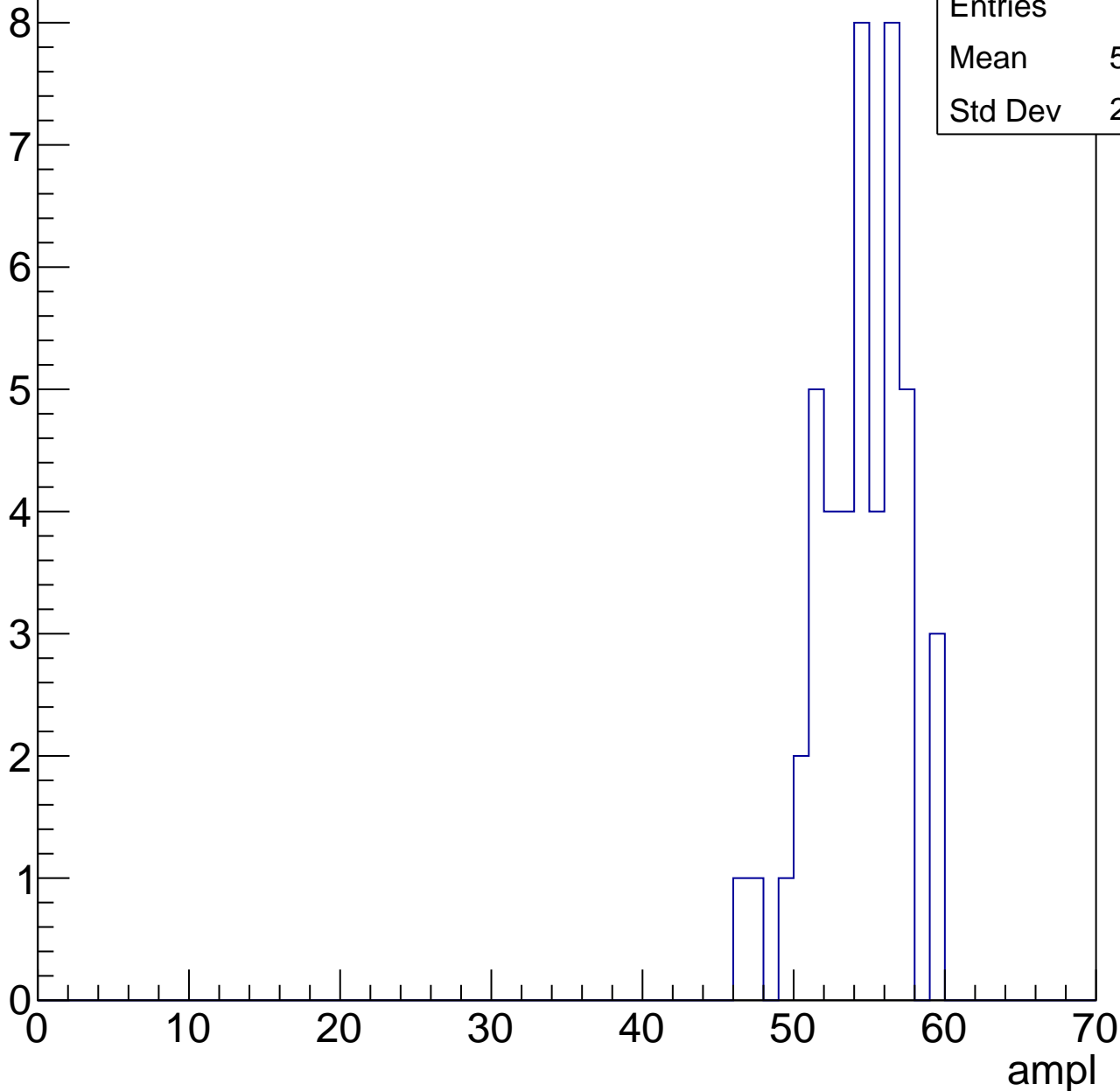


B1L103S, U7-ch42, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	46
Mean	53.89
Std Dev	2.913

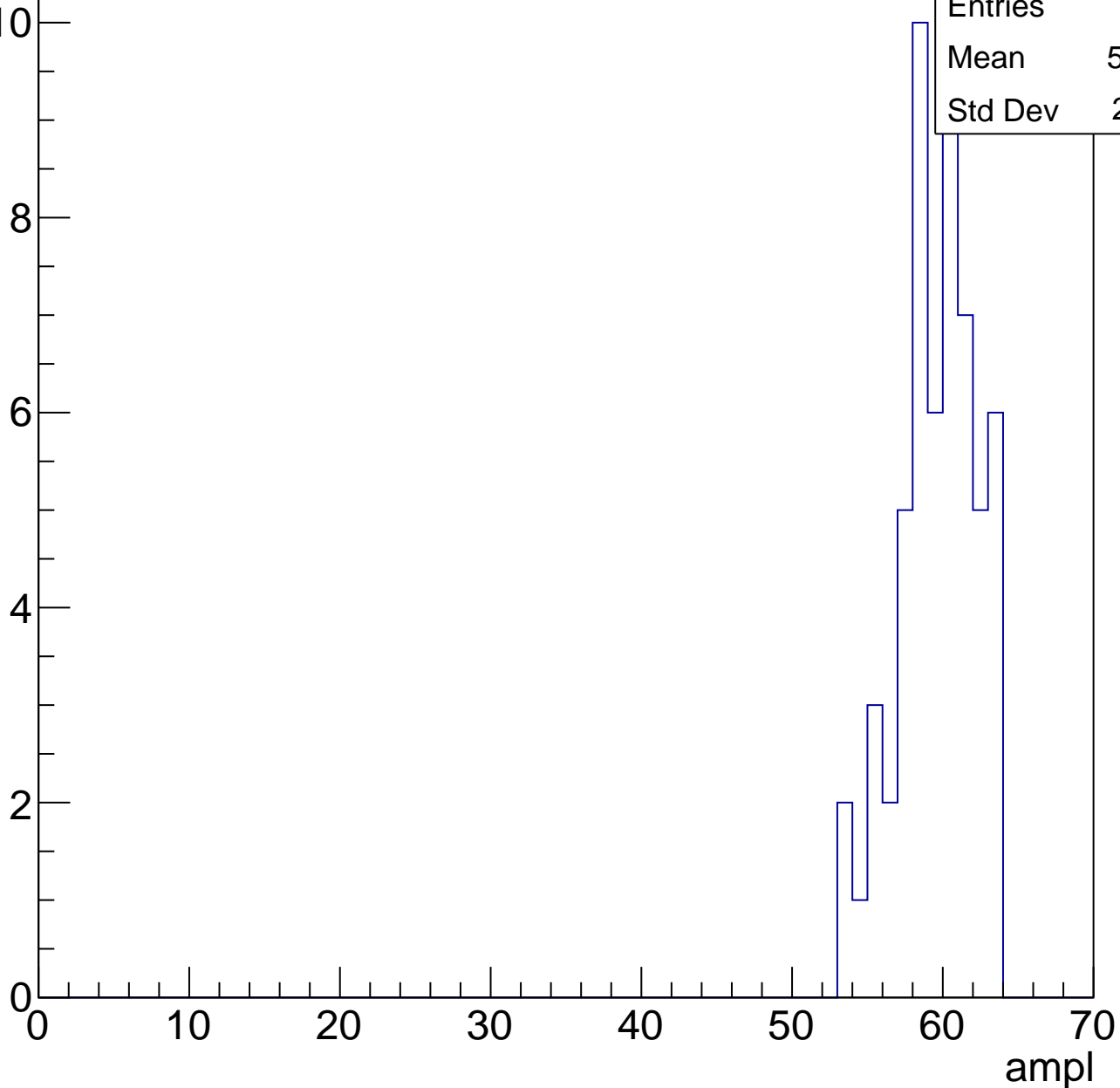


B1L103S, U7-ch42, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	59.12
Std Dev	2.571

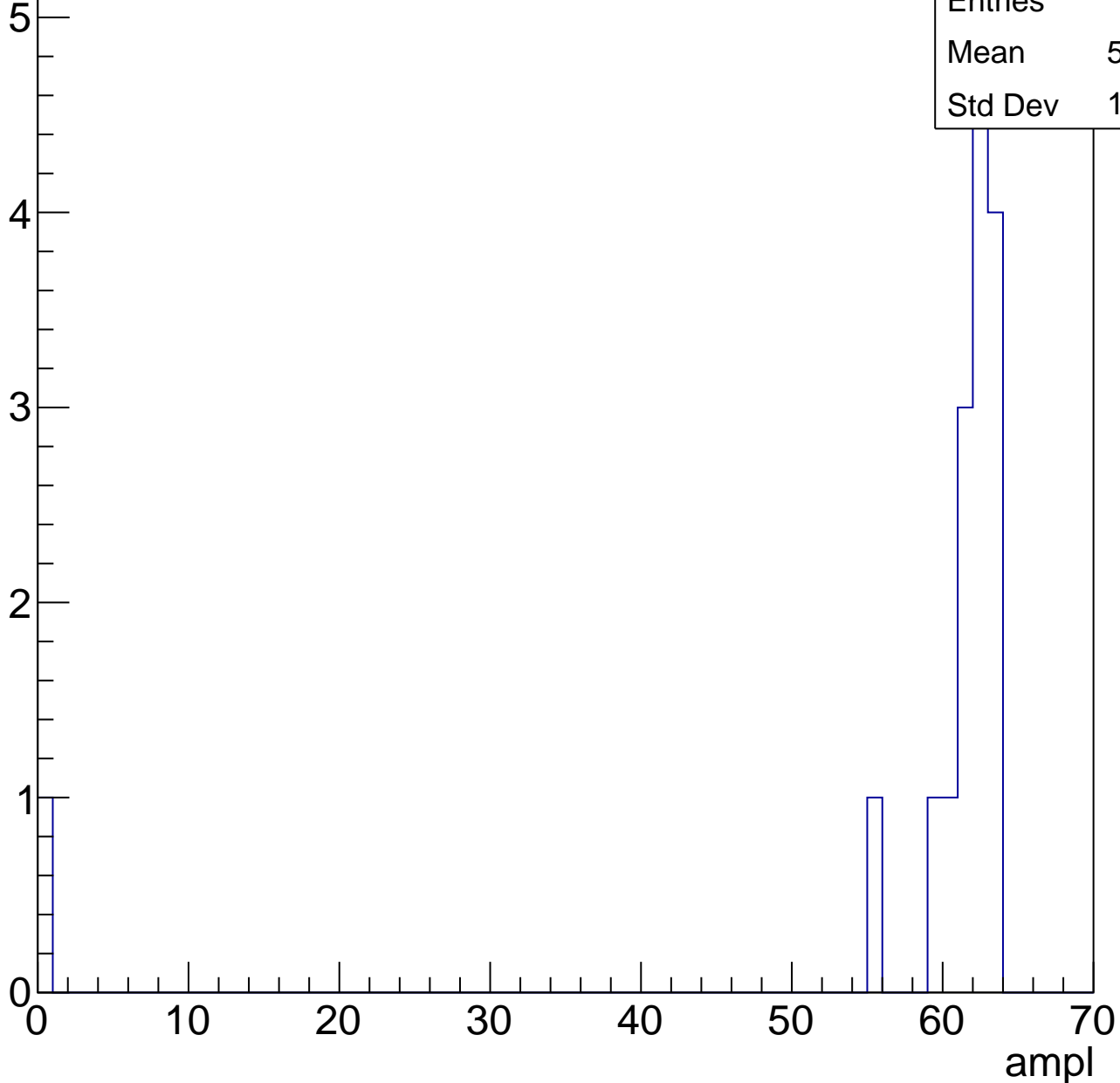


B1L103S, U7-ch42, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	16
Mean	57.44
Std Dev	14.96

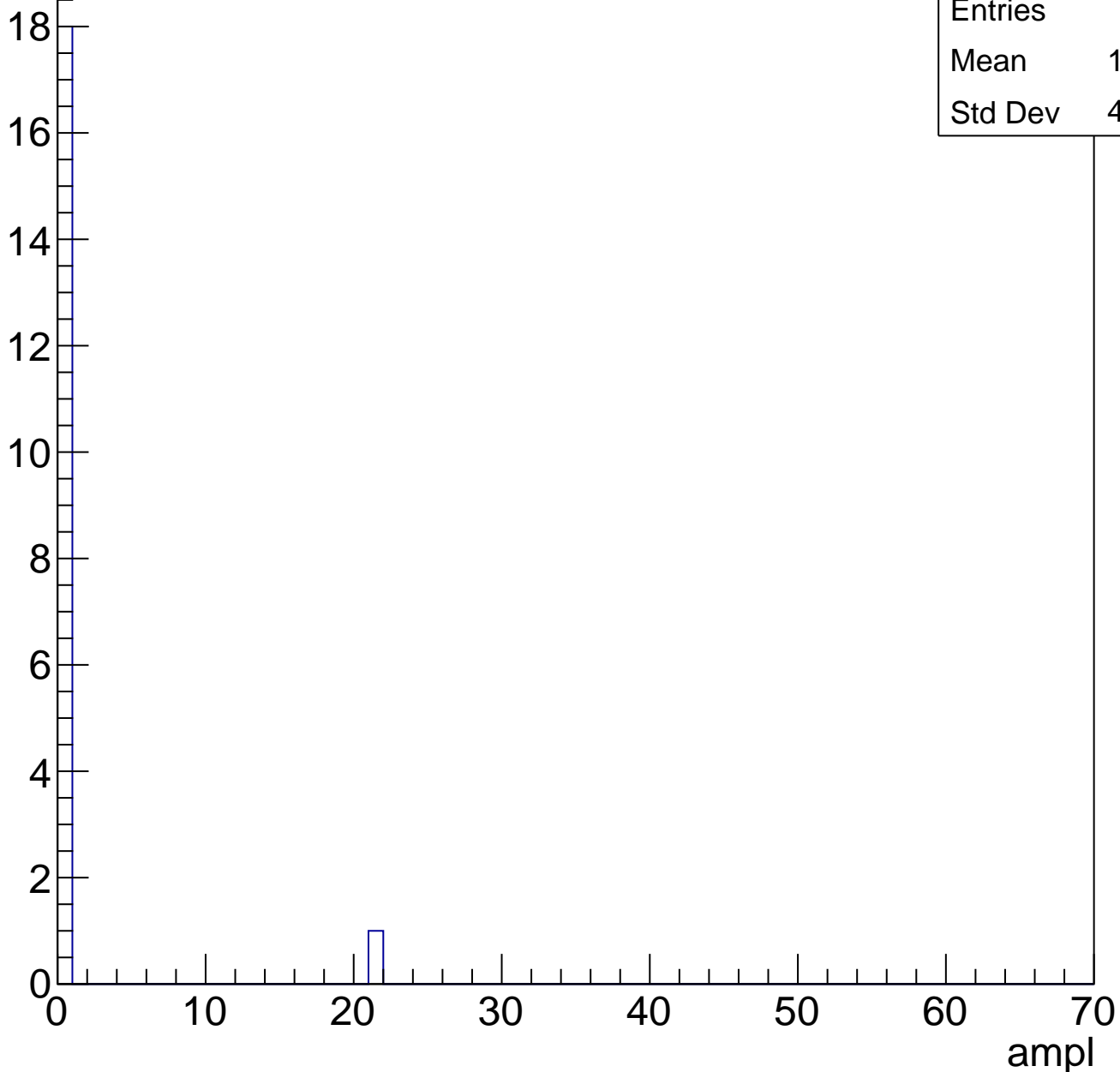


B1L103S, U7-ch42, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.105
Std Dev	4.689

Entry



B1L103S, U7-ch43, adc0

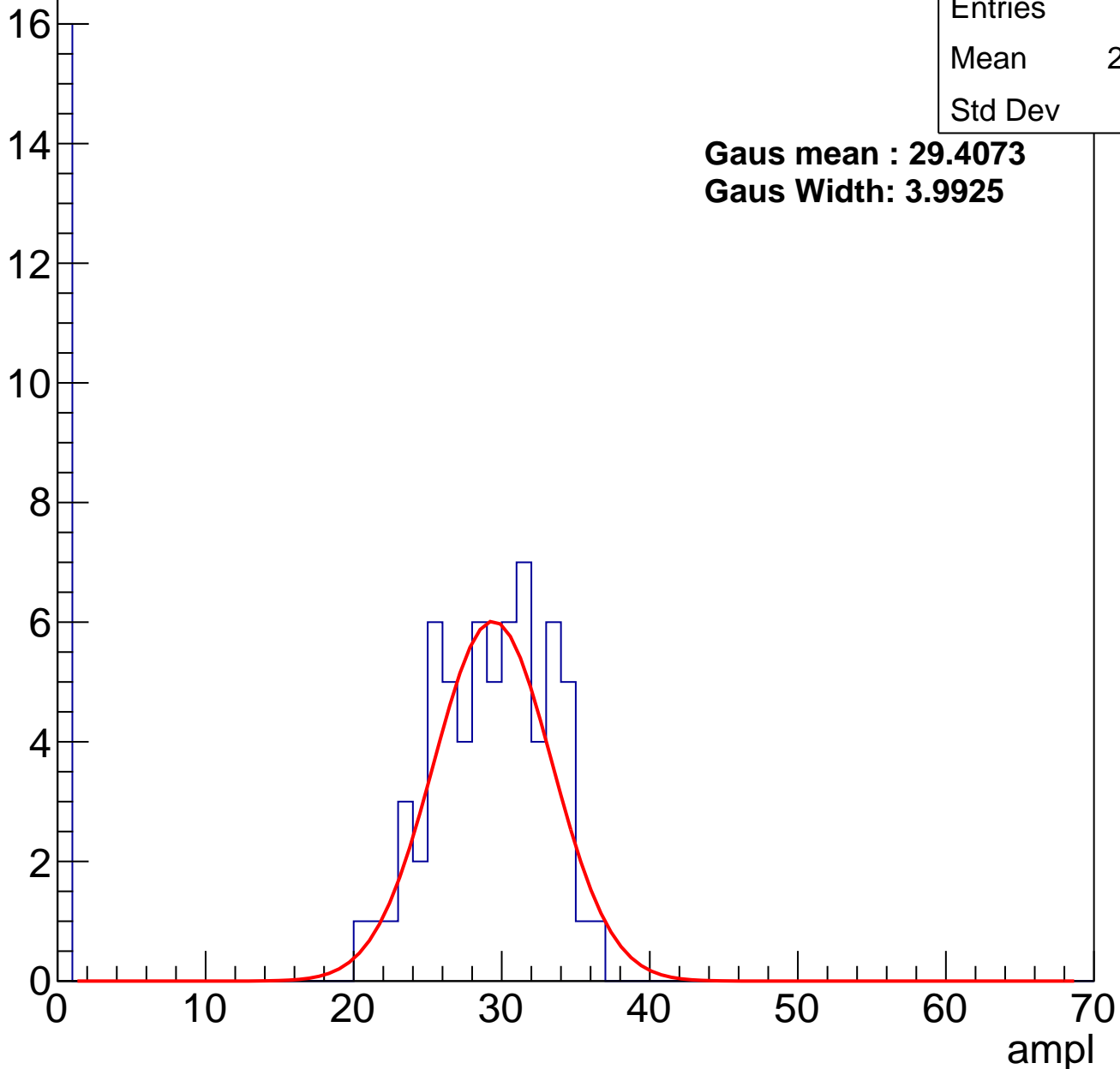
calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	23.06
Std Dev	12

Gaus mean : 29.4073

Gaus Width: 3.9925

Entry



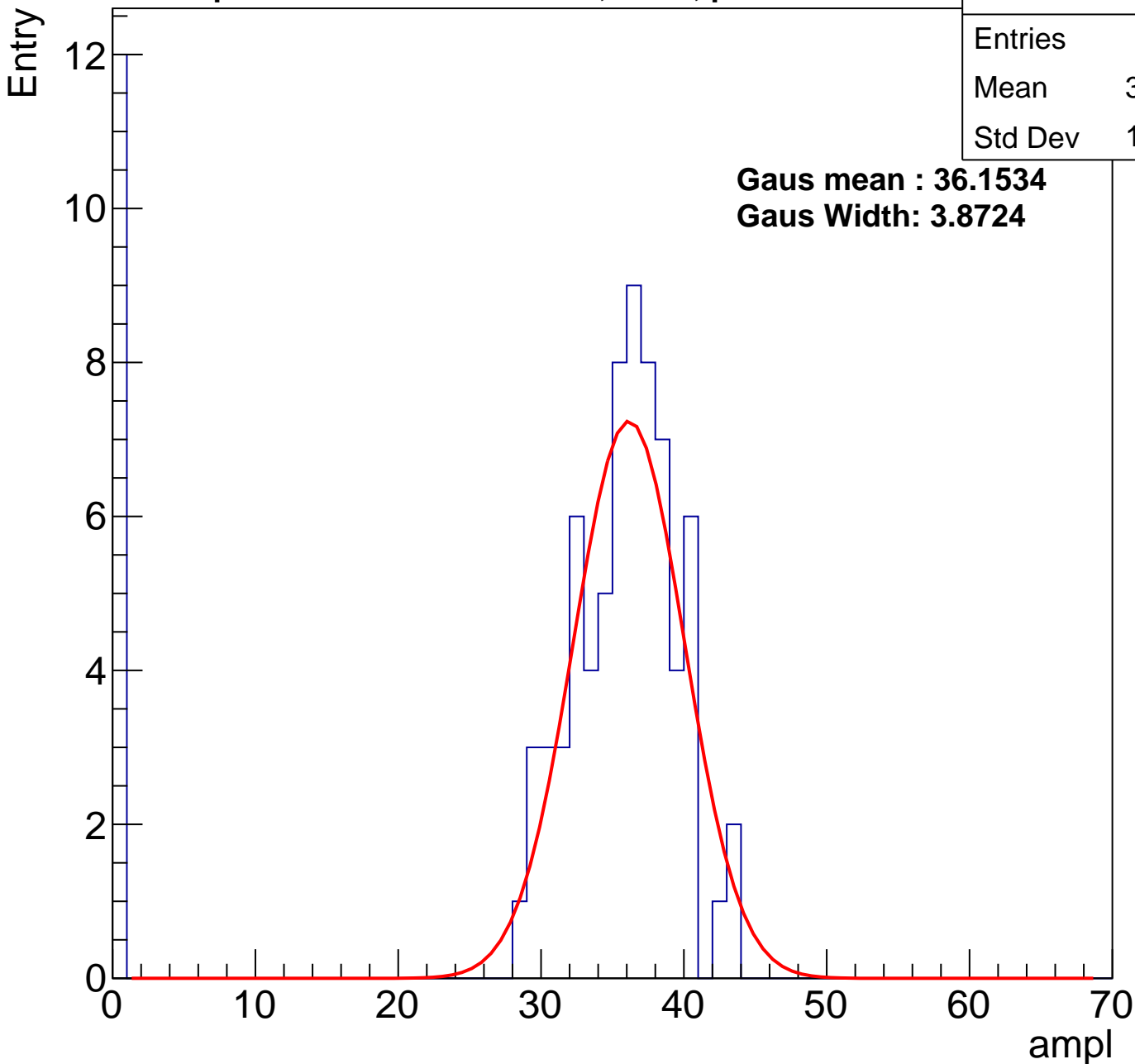
B1L103S, U7-ch43, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	30.27
Std Dev	12.93

Gaus mean : 36.1534

Gaus Width: 3.8724



B1L103S, U7-ch43, adc2

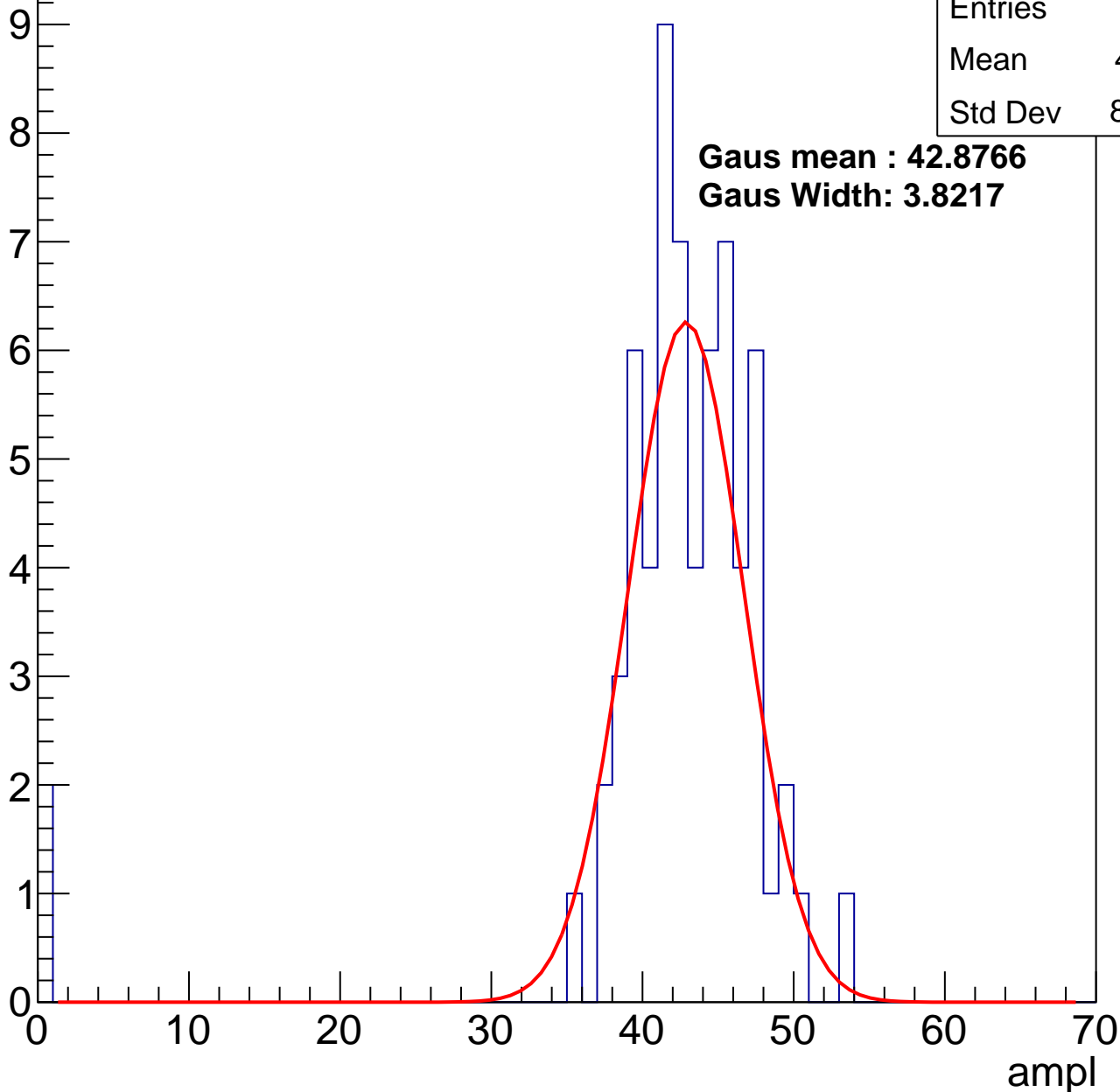
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	41.61
Std Dev	8.135

Gaus mean : 42.8766

Gaus Width: 3.8217

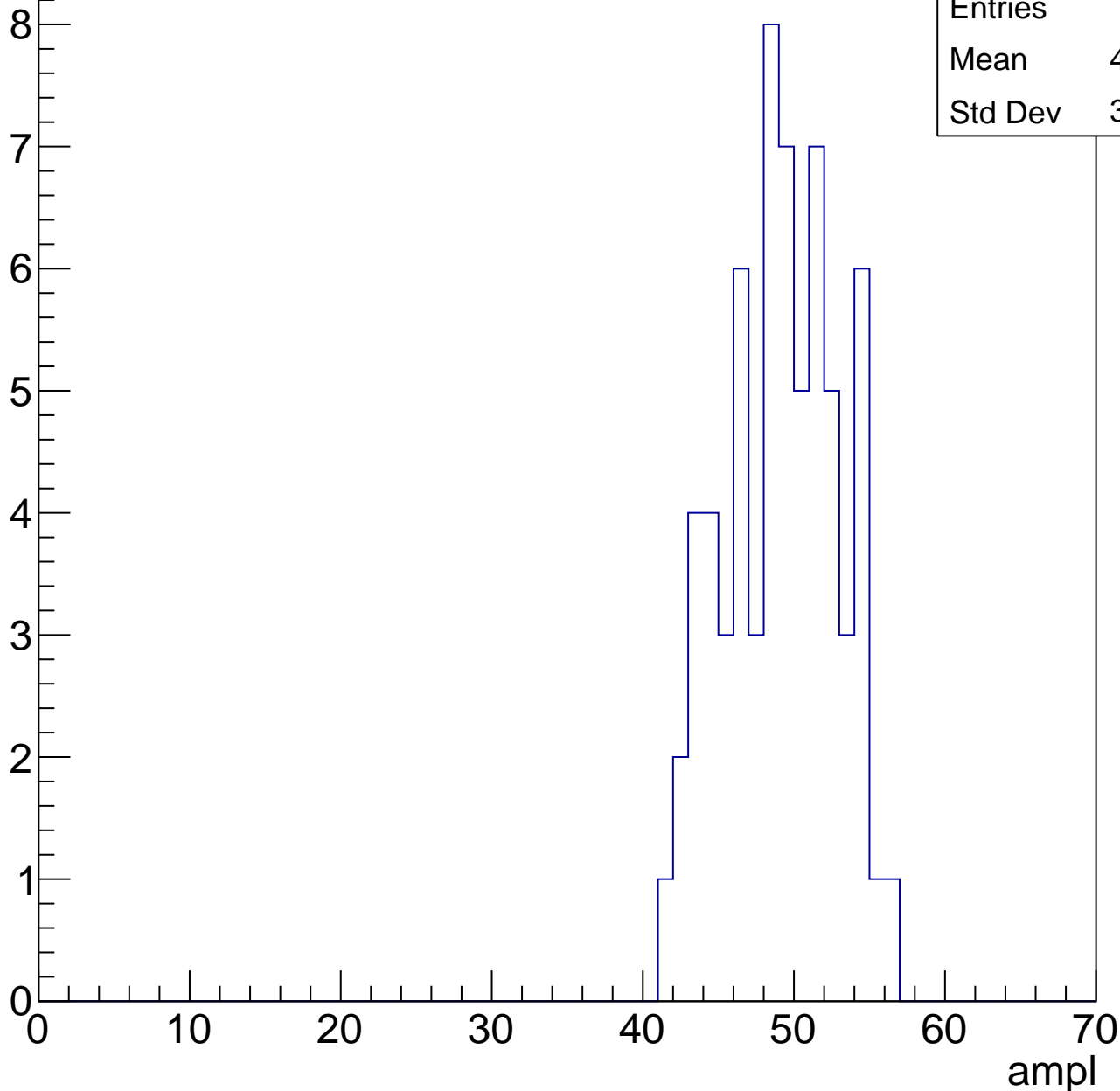


B1L103S, U7-ch43, adc3

calib_packv5_041523_1651.root, FC#0, port C2

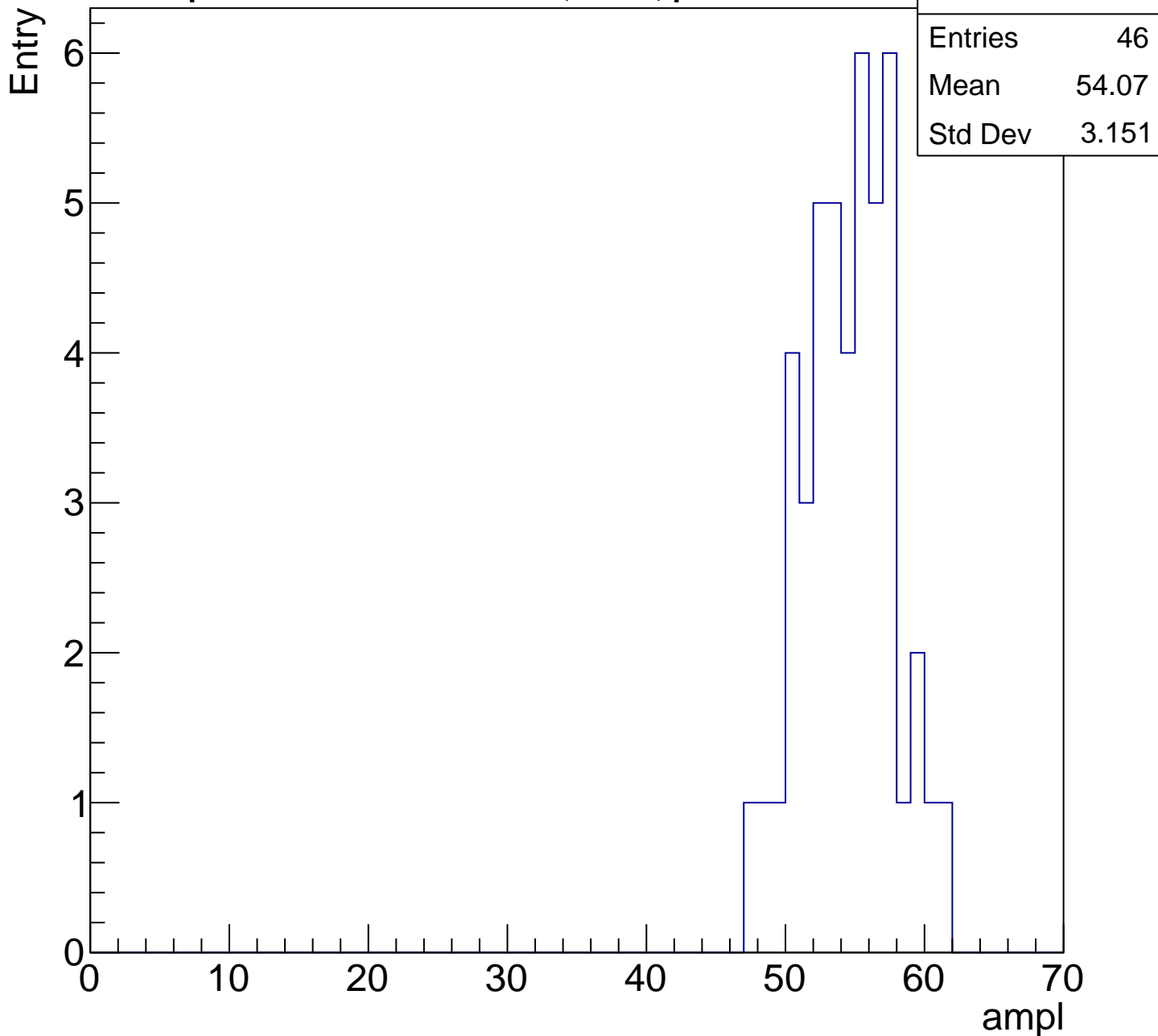
Entry

Entries	66
Mean	48.68
Std Dev	3.656



B1L103S, U7-ch43, adc4

calib_packv5_041523_1651.root, FC#0, port C2

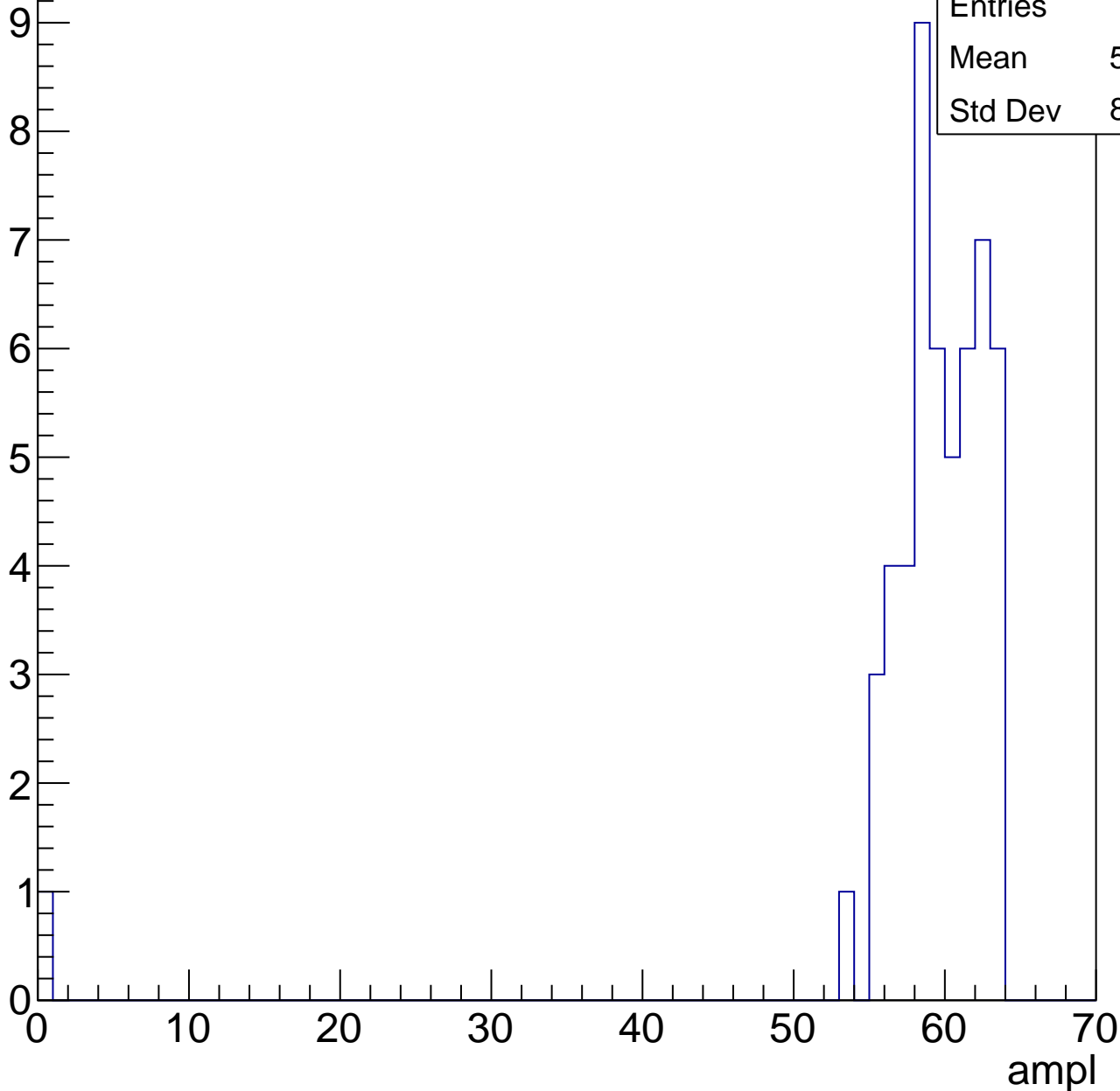


B1L103S, U7-ch43, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	58.15
Std Dev	8.522



B1L103S, U7-ch43, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

4
3.5
3
2.5
2
1.5
1
0.5
0

Entries	15
Mean	61.13
Std Dev	1.408

ampl

0 10 20 30 40 50 60 70

B1L103S, U7-ch43, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51

Entry



B1L103S, U7-ch44, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	21.68
Std Dev	11.21

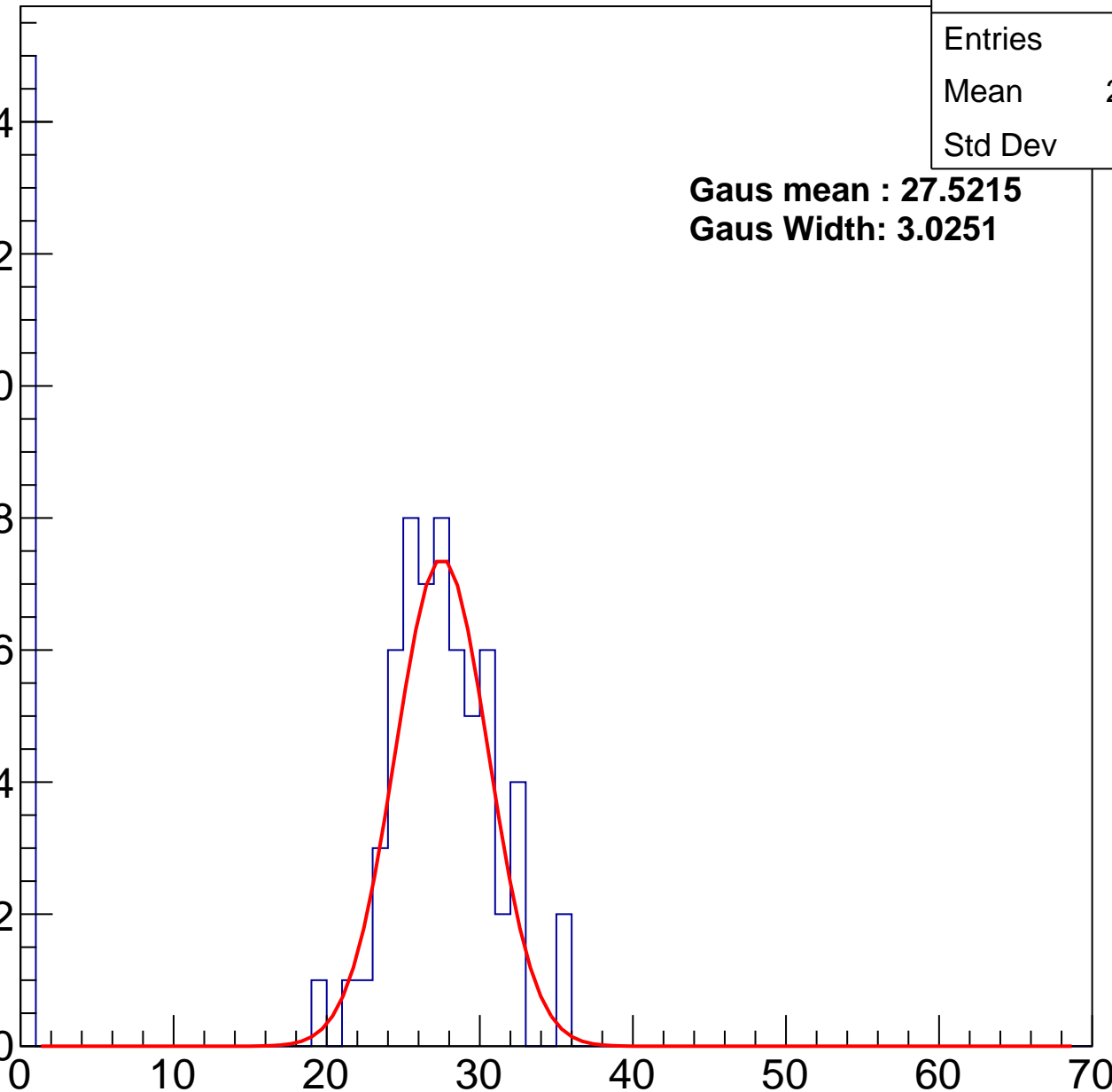
Gaus mean : 27.5215

Gaus Width: 3.0251

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch44, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	29.18
Std Dev	11.93

Gaus mean : 34.0011

Gaus Width: 3.6260

Entry

10

8

6

4

2

0

0

10

20

30

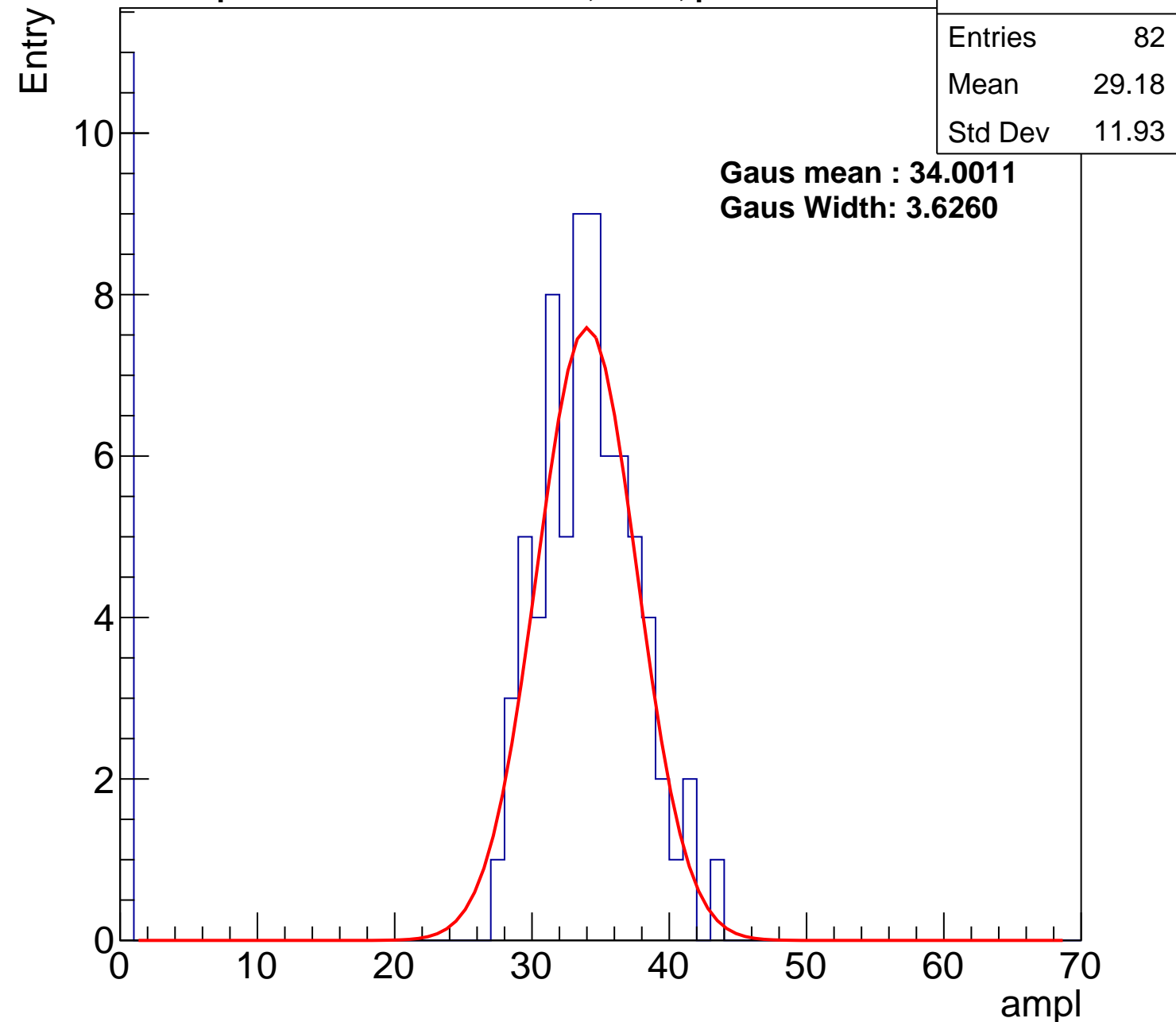
40

50

60

70

ampl



B1L103S, U7-ch44, adc2

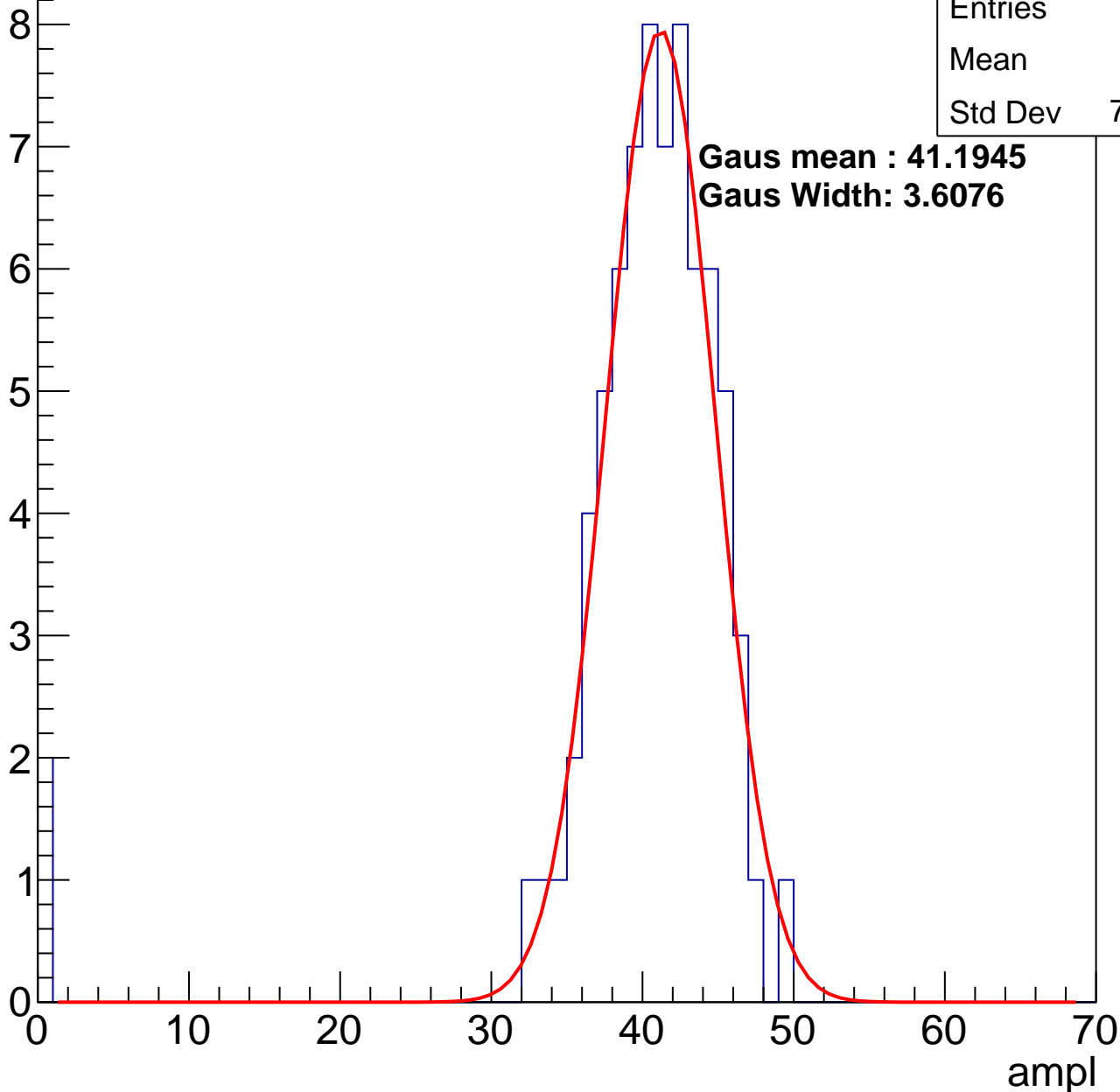
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	39.5
Std Dev	7.418

Gaus mean : 41.1945

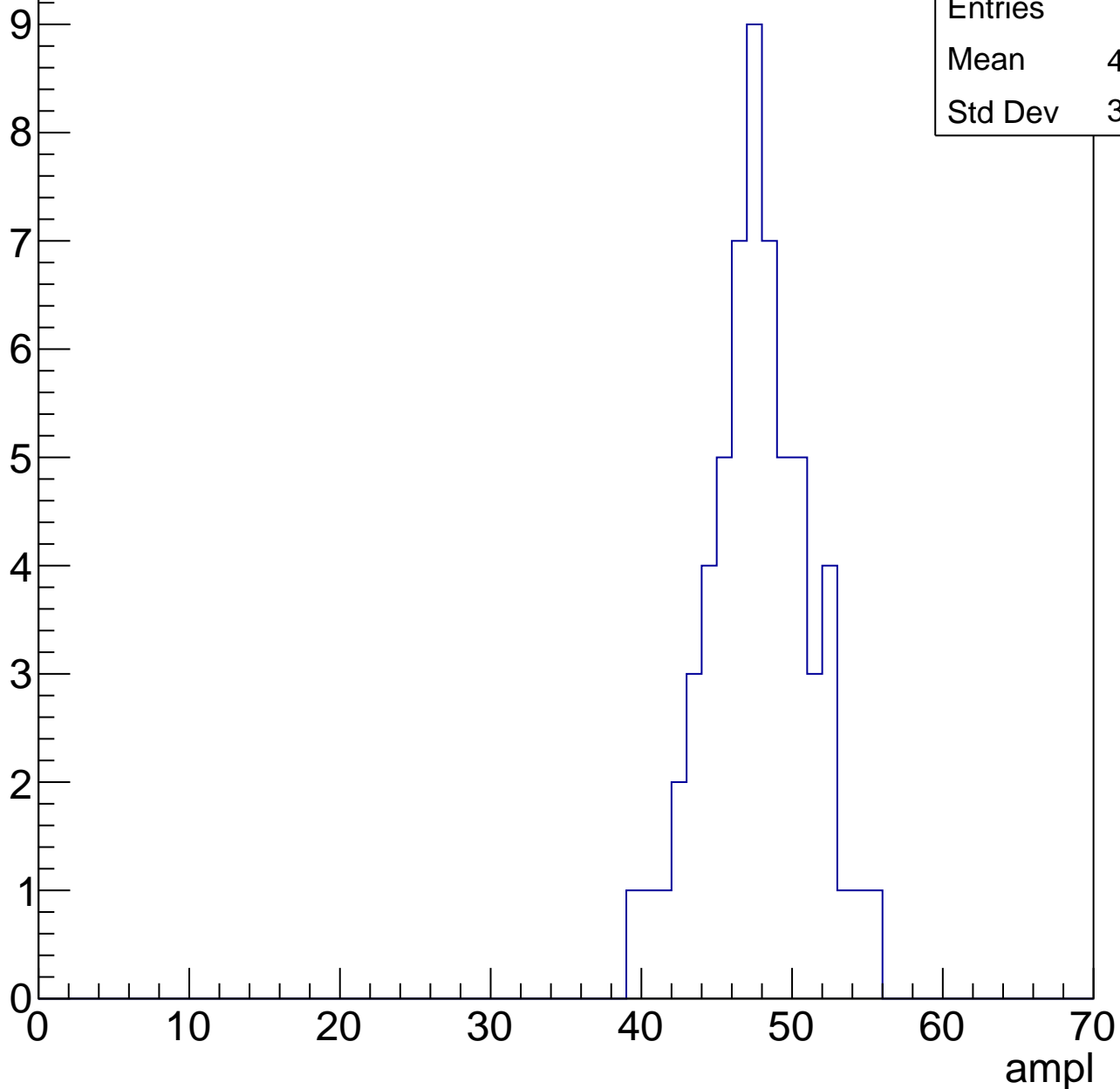
Gaus Width: 3.6076



B1L103S, U7-ch44, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

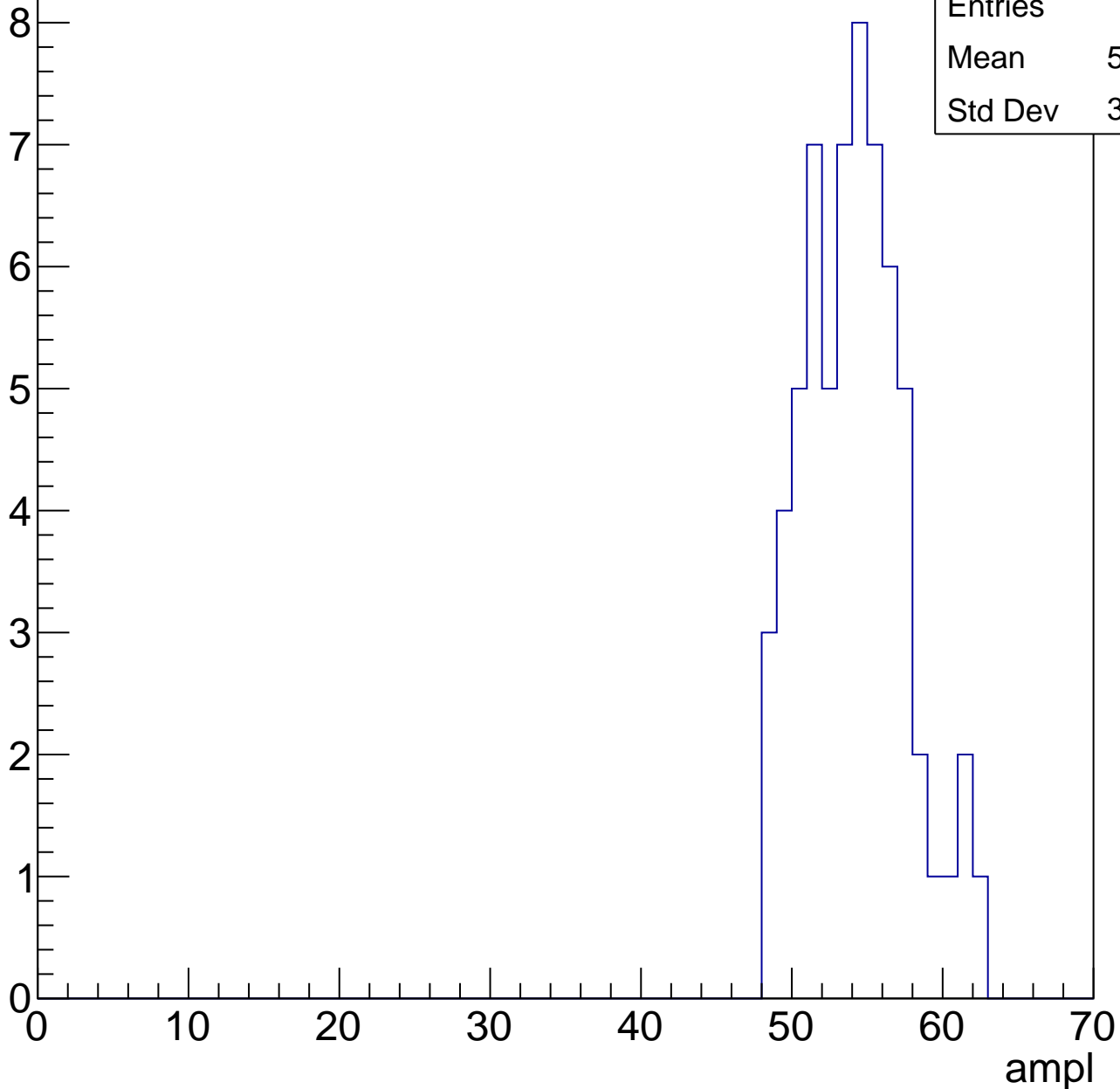


B1L103S, U7-ch44, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	53.67
Std Dev	3.312



B1L103S, U7-ch44, adc5

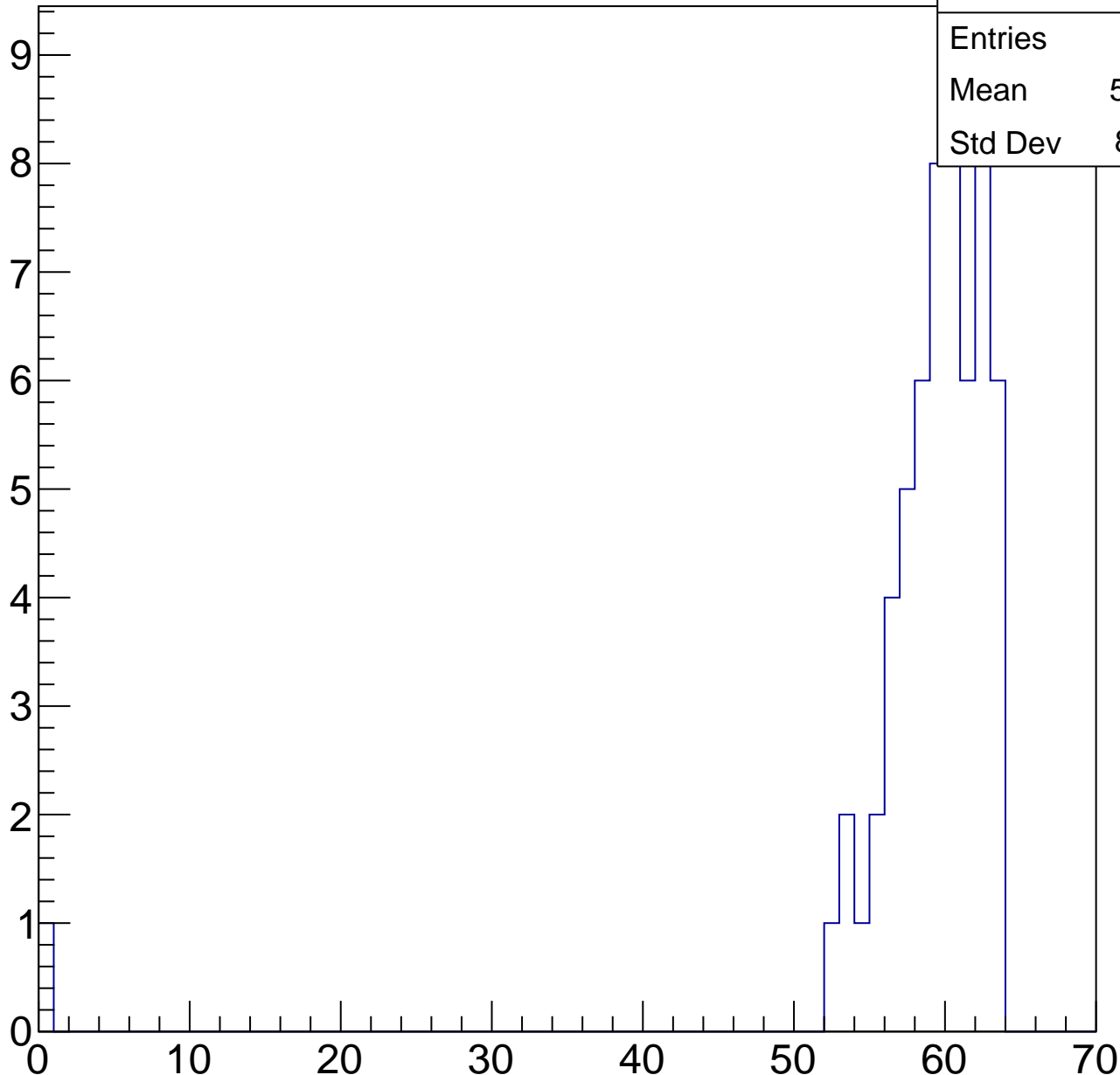
calib_packv5_041523_1651.root, FC#0, port C2

Entry

9
8
7
6
5
4
3
2
1
0

Entries	59
Mean	58.19
Std Dev	8.121

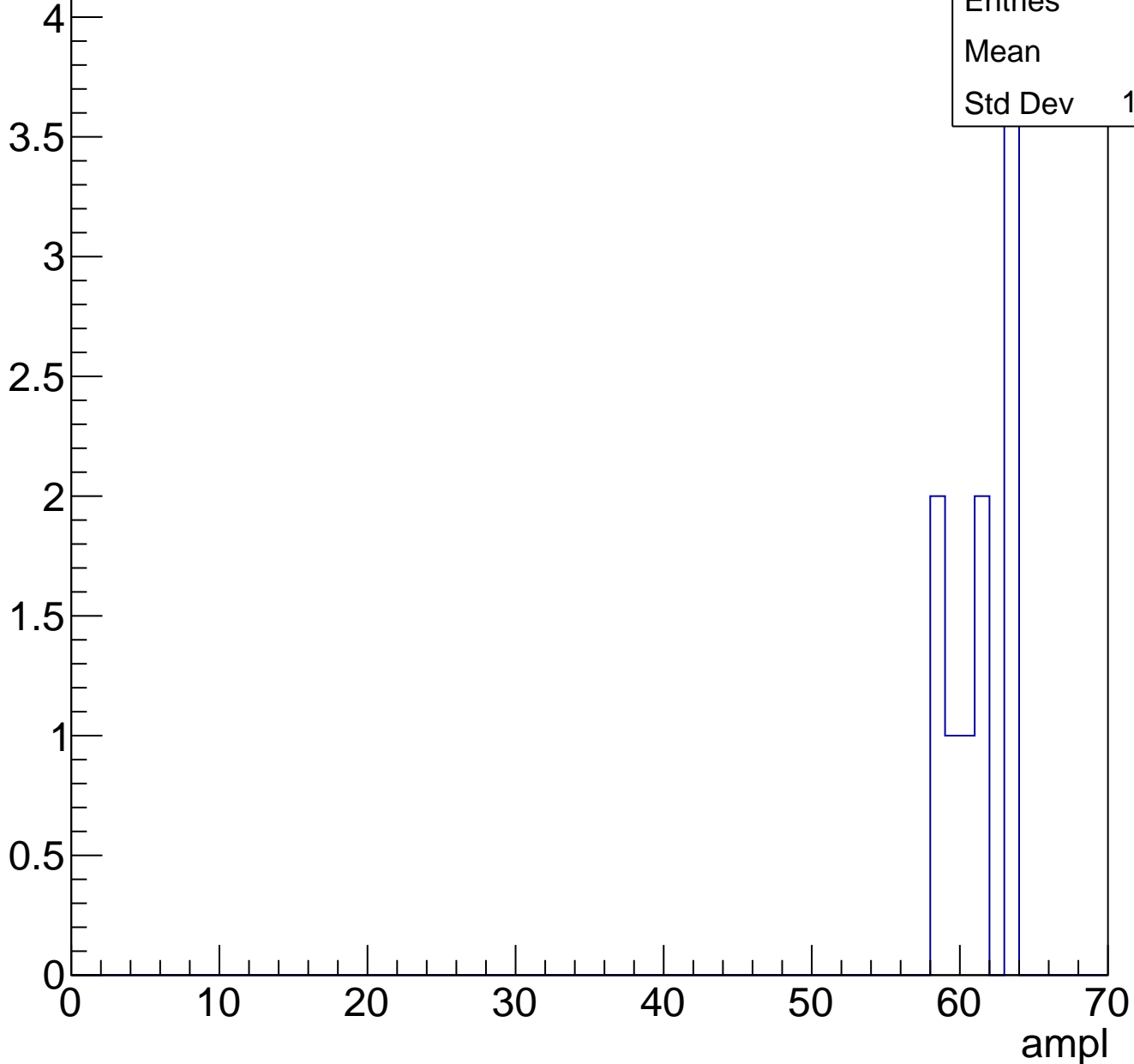
ampl



B1L103S, U7-ch44, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch44, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U7-ch45, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	70
Mean	27.54
Std Dev	9.714

Gaus mean : 30.5318

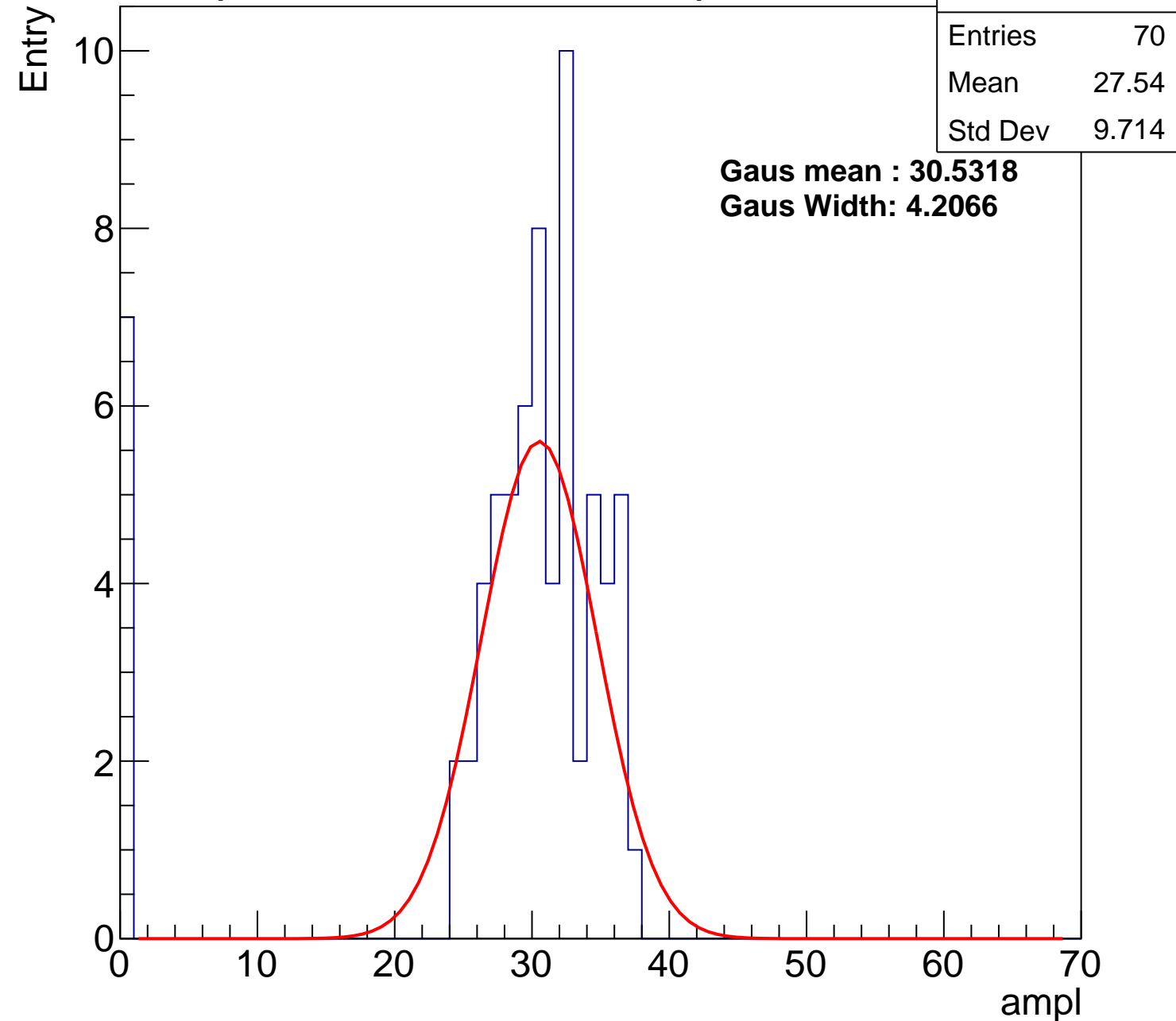
Gaus Width: 4.2066

Entry

10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U7-ch45, adc1

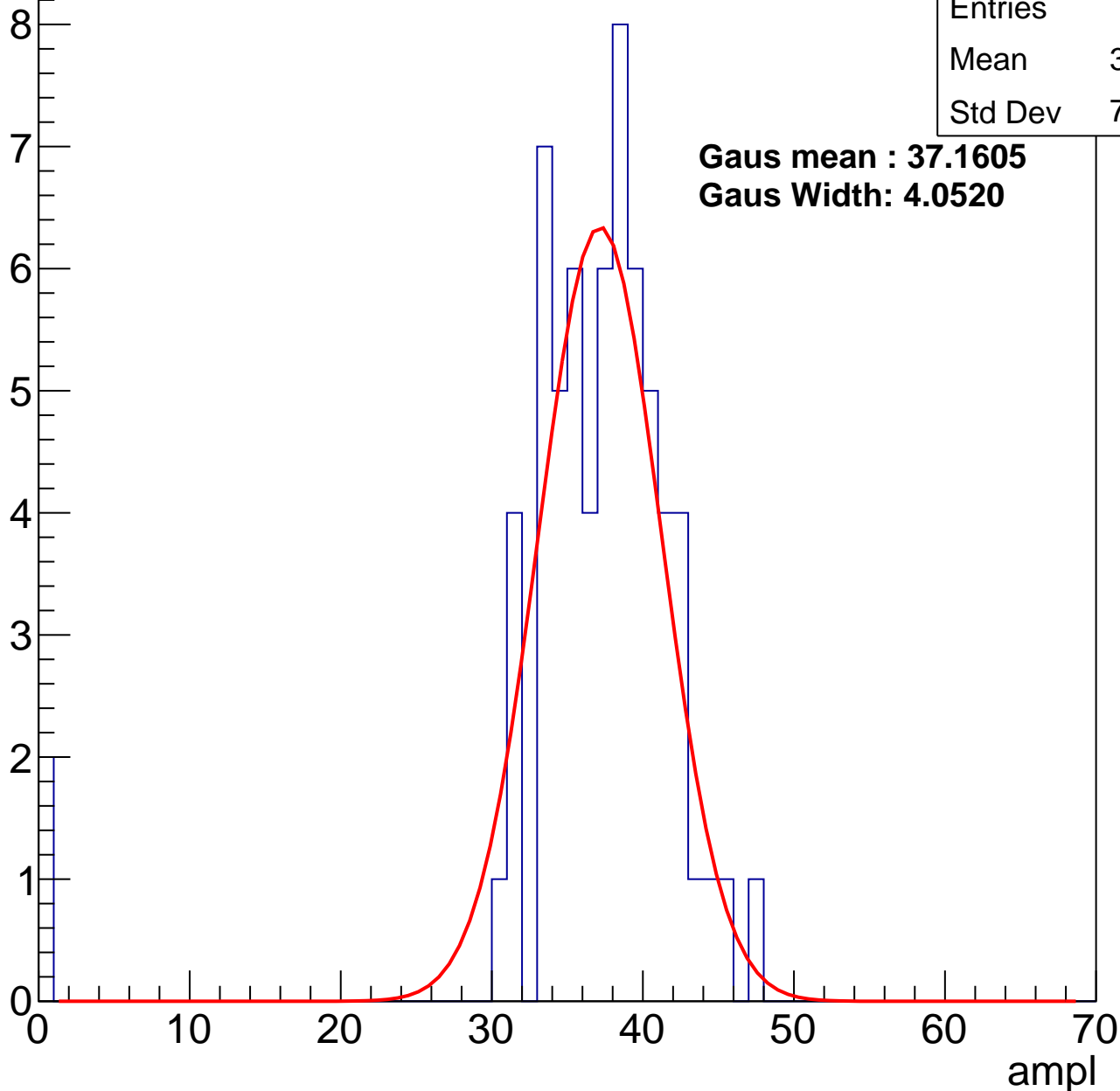
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	36.06
Std Dev	7.332

Gaus mean : 37.1605

Gaus Width: 4.0520



B1L103S, U7-ch45, adc2

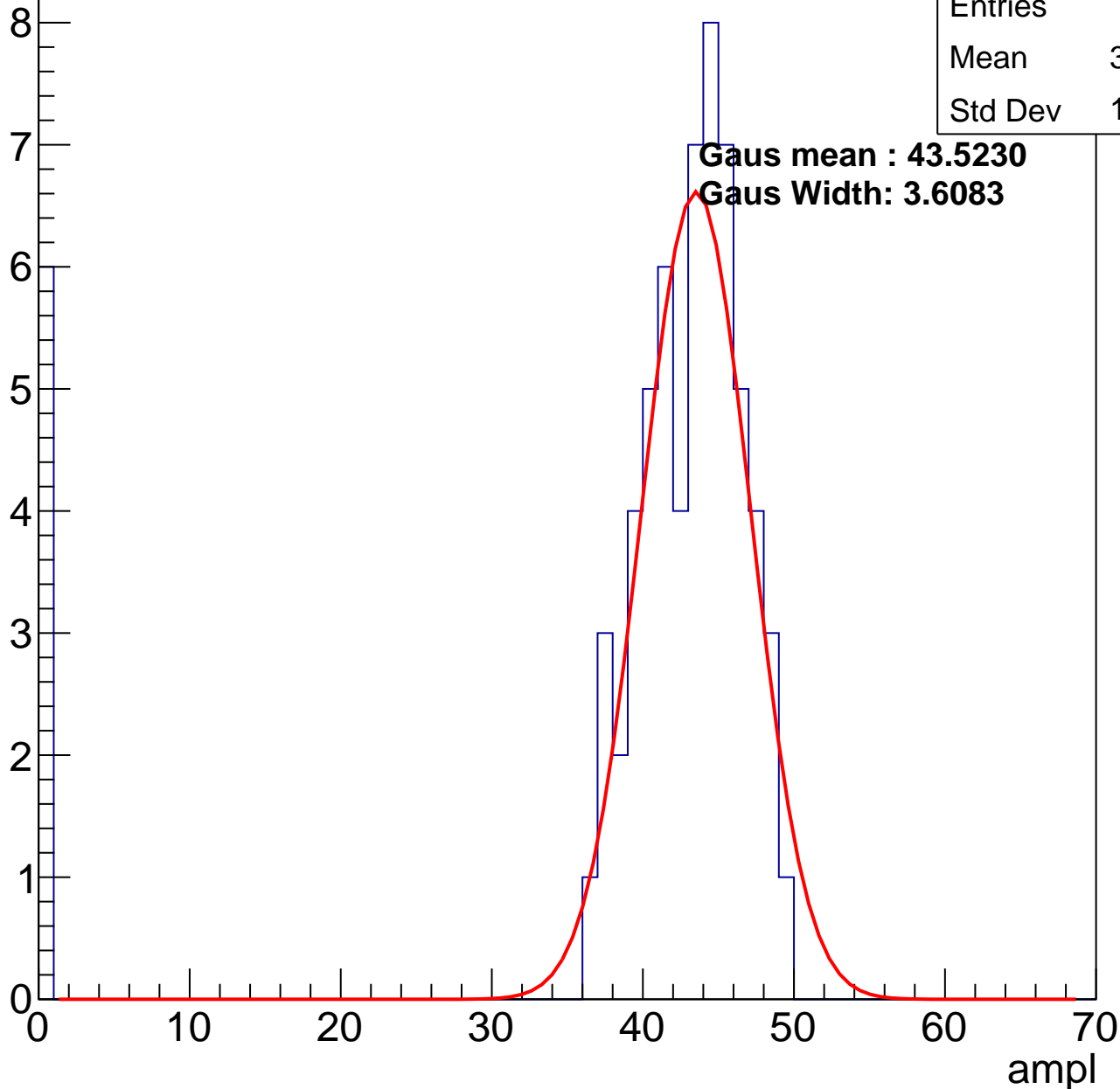
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	38.97
Std Dev	12.69

Gaus mean : 43.5230

Gaus Width: 3.6083

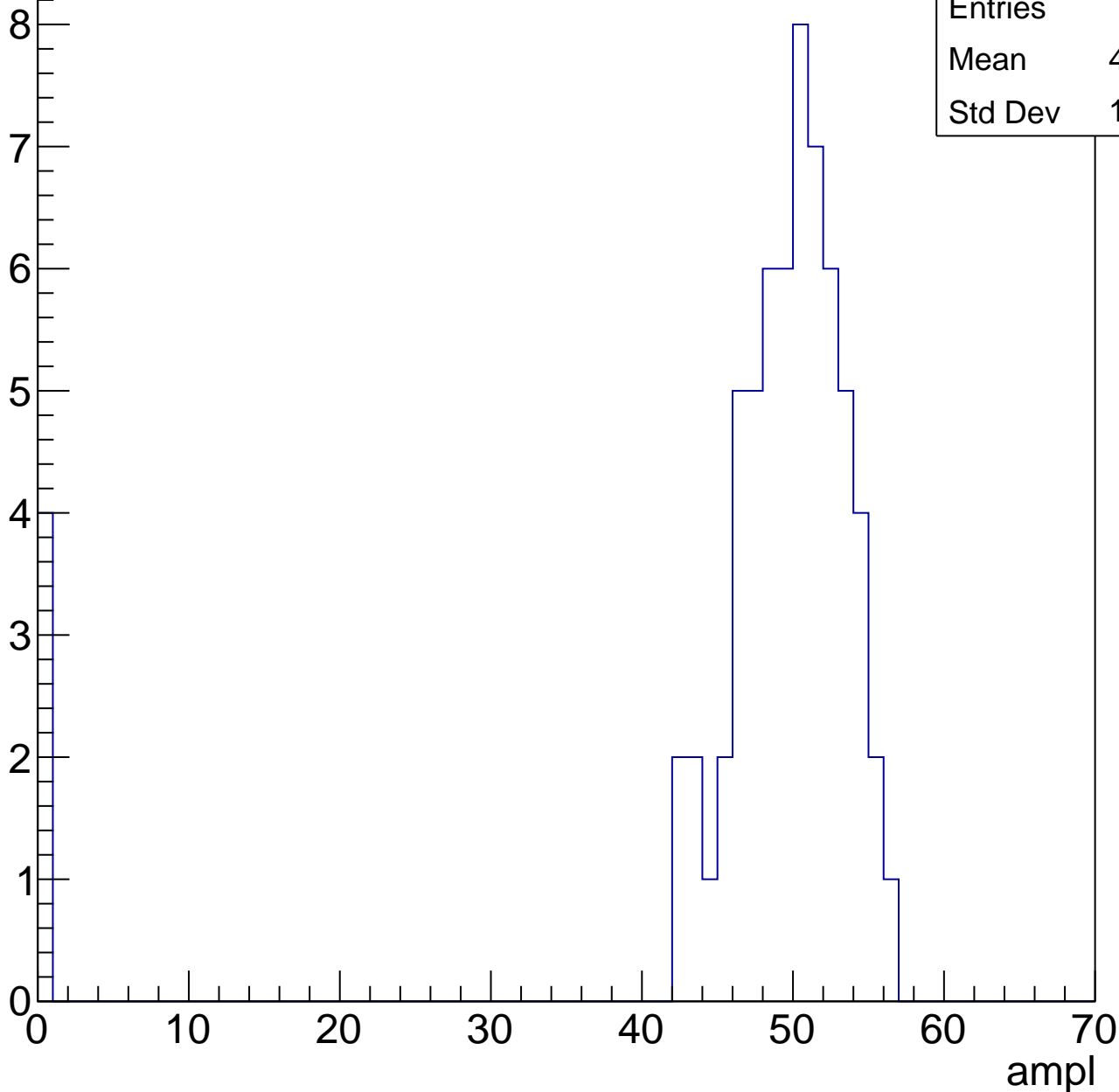


B1L103S, U7-ch45, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	46.47
Std Dev	12.23

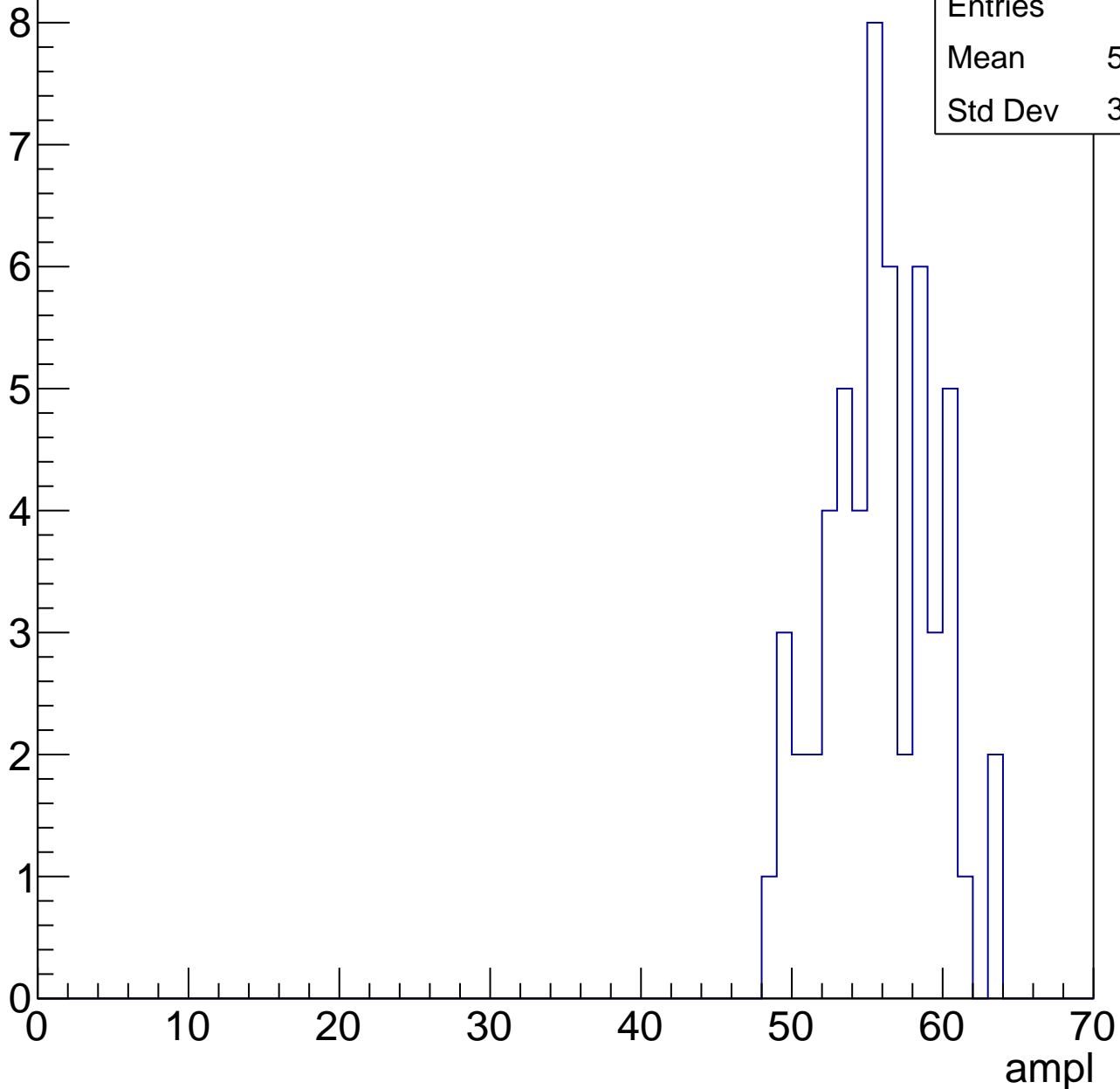


B1L103S, U7-ch45, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	55.33
Std Dev	3.595

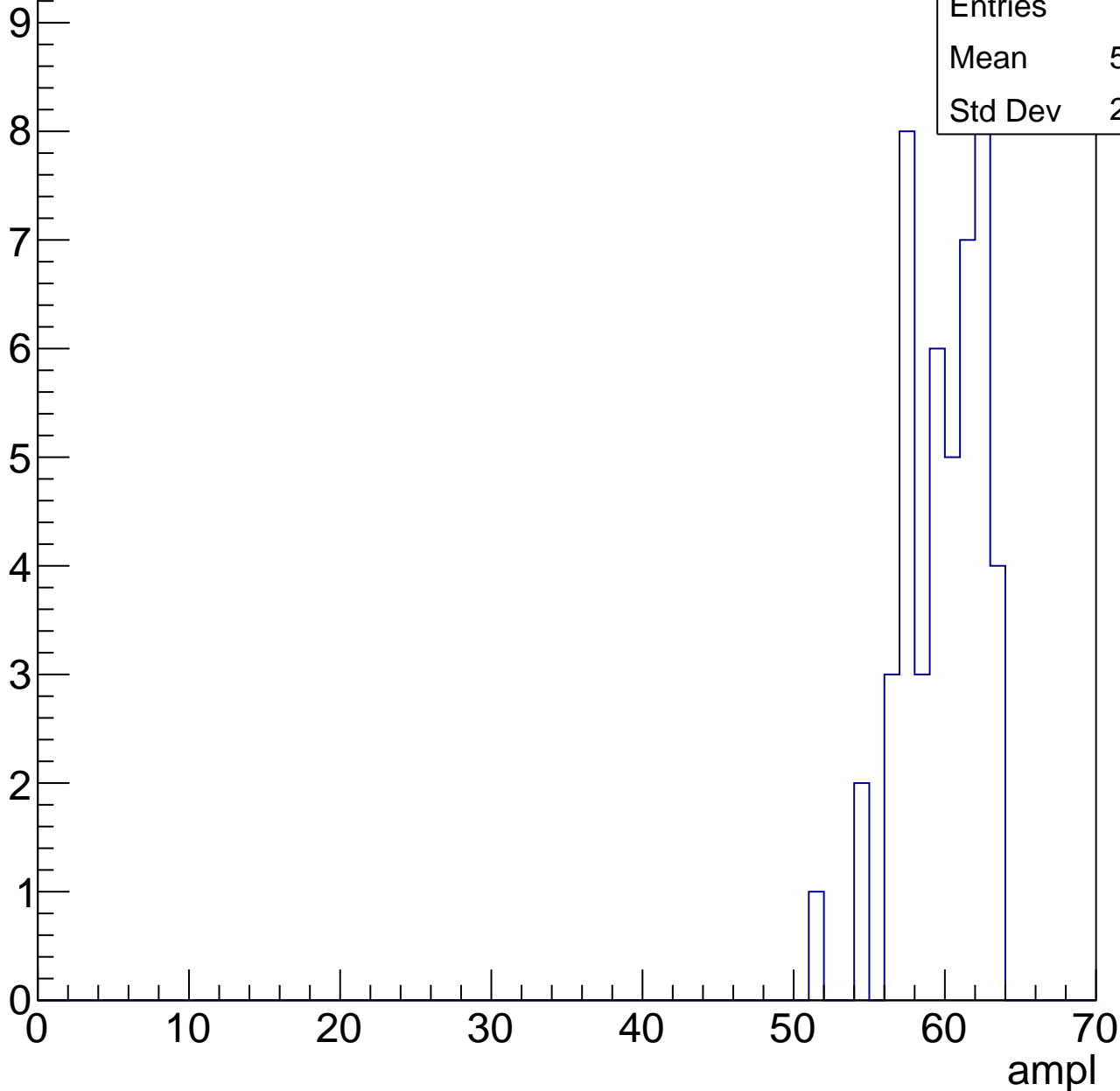


B1L103S, U7-ch45, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

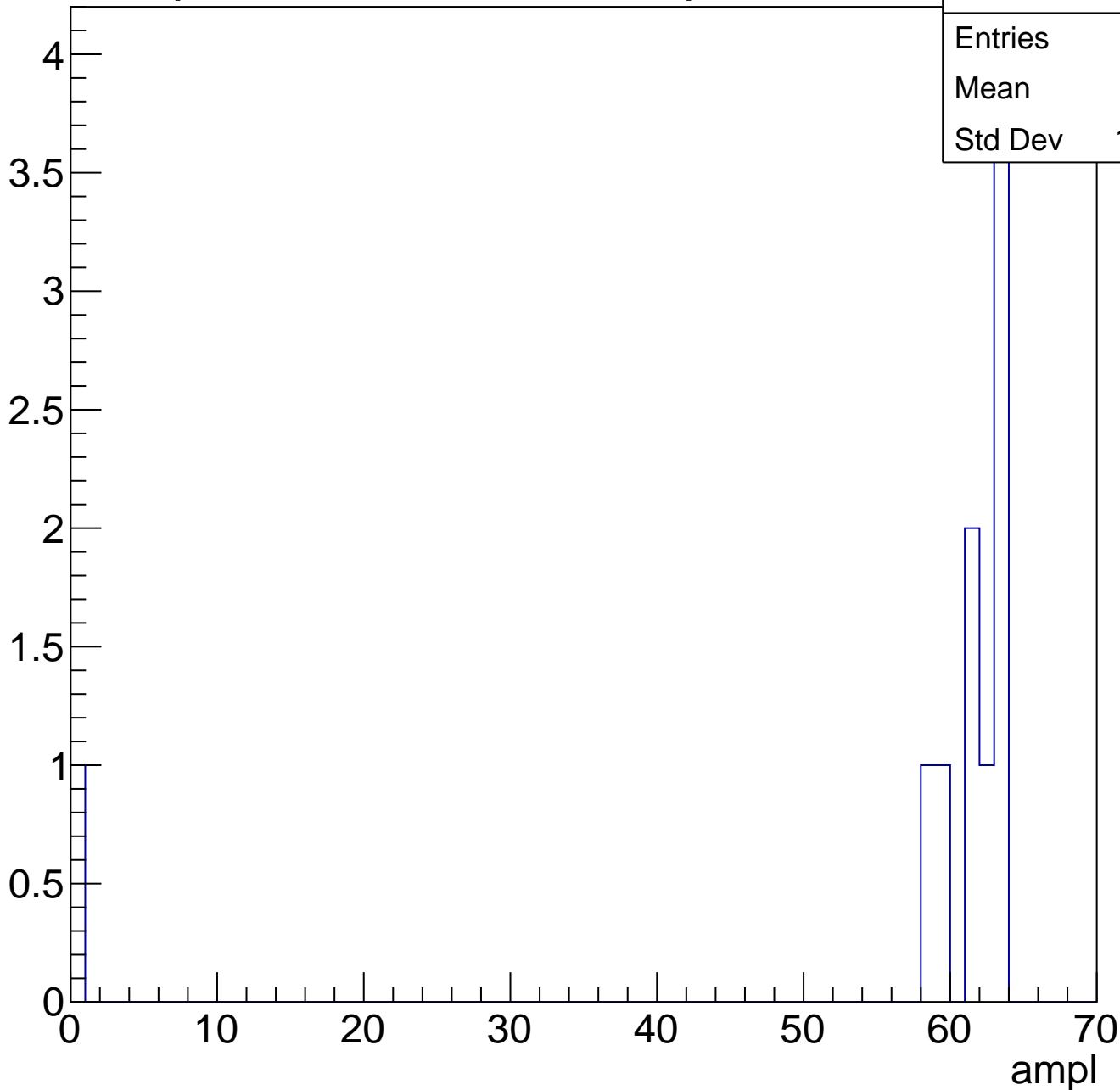
Entries	48
Mean	59.33
Std Dev	2.695



B1L103S, U7-ch45, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch45, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U7-ch46, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	72
Mean	22.76
Std Dev	10.24

Gaus mean : 27.7741

Gaus Width: 3.5333

Entry

10

8

6

4

2

0

0

10

20

30

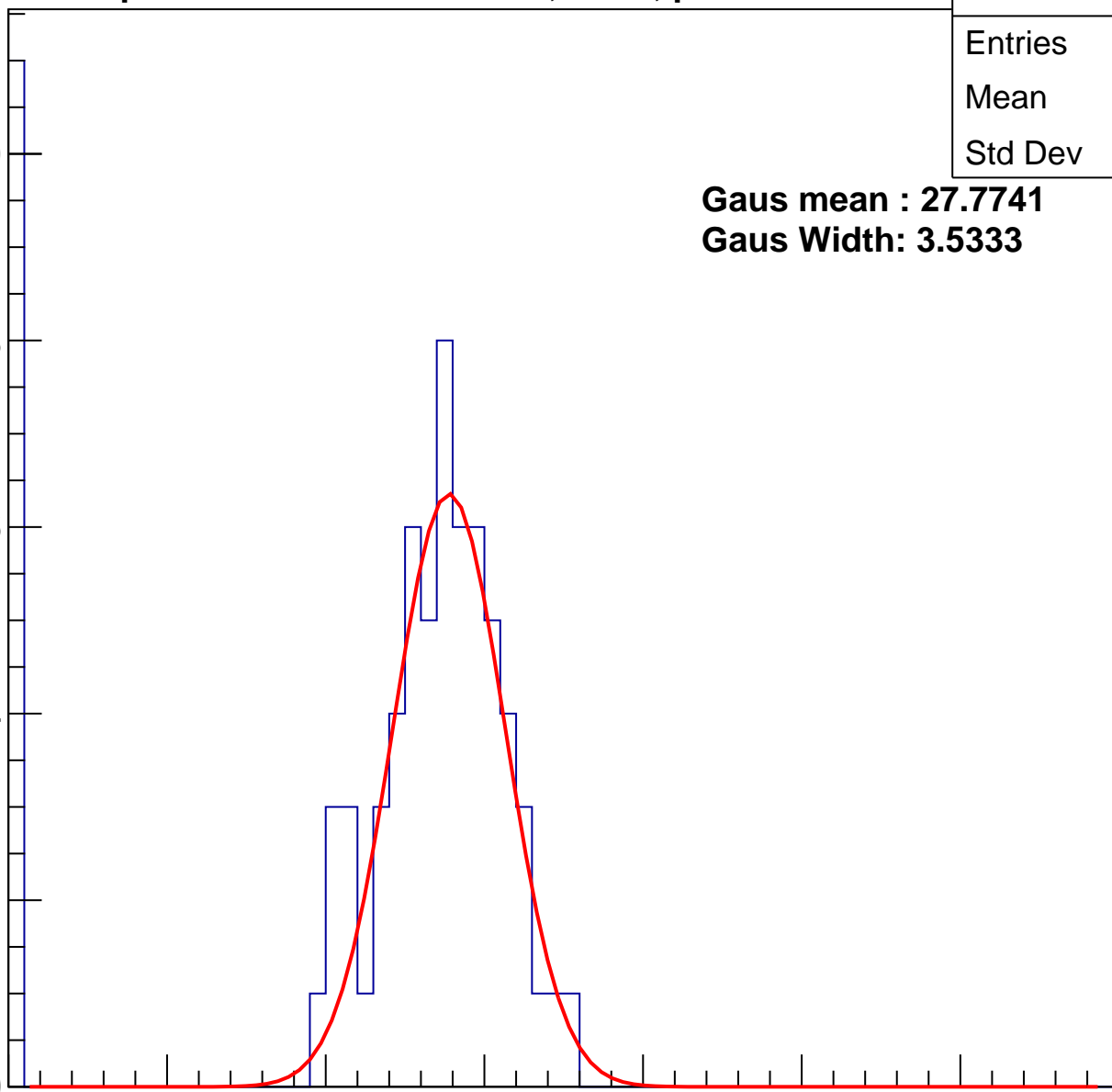
40

50

60

70

ampl



B1L103S, U7-ch46, adc1

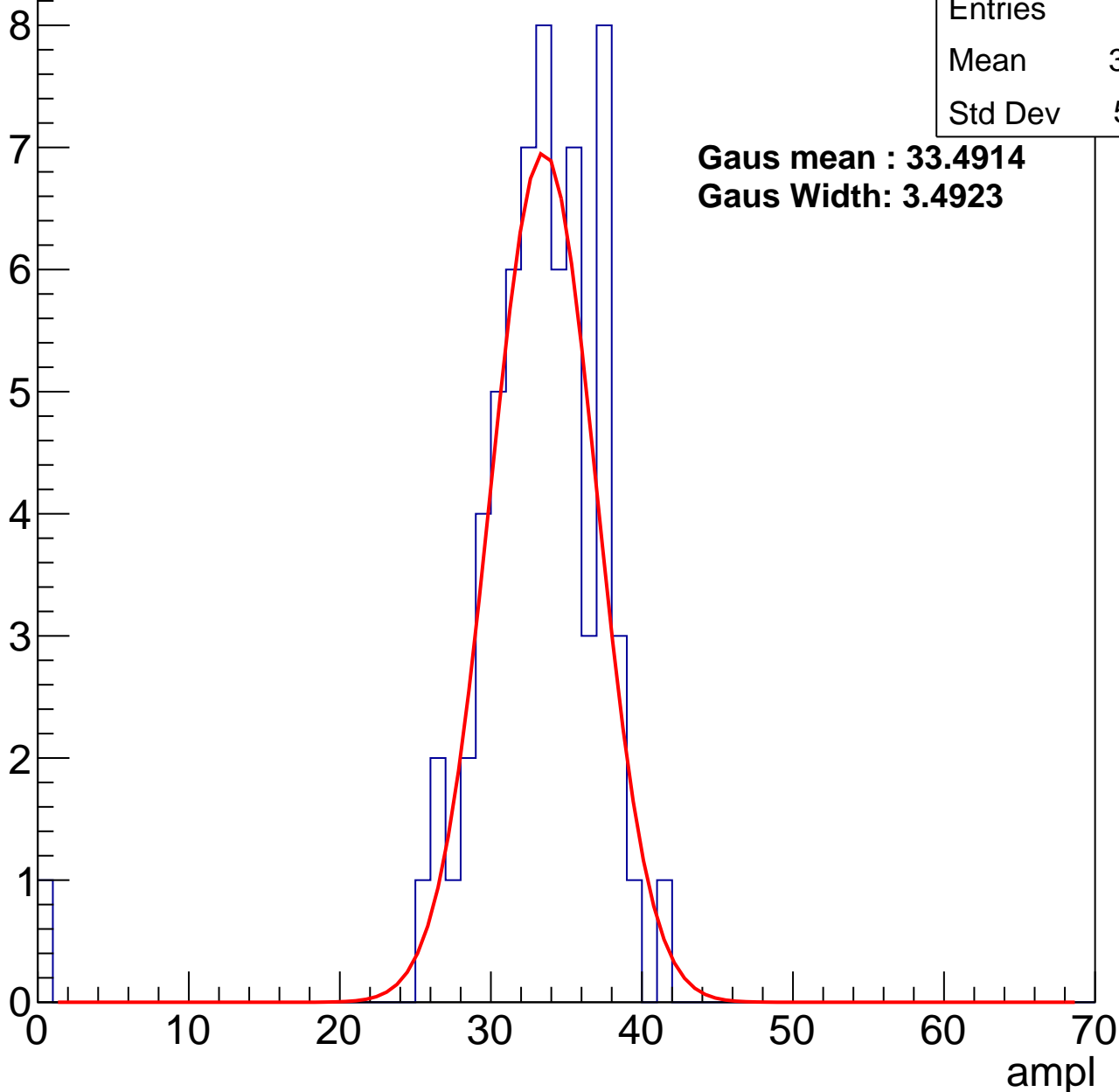
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	32.53
Std Dev	5.261

Gaus mean : 33.4914

Gaus Width: 3.4923



B1L103S, U7-ch46, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	70
Mean	33.9
Std Dev	14.14

Gaus mean : 40.4262

Gaus Width: 3.4862

Entry

10

8

6

4

2

0

0

10

20

30

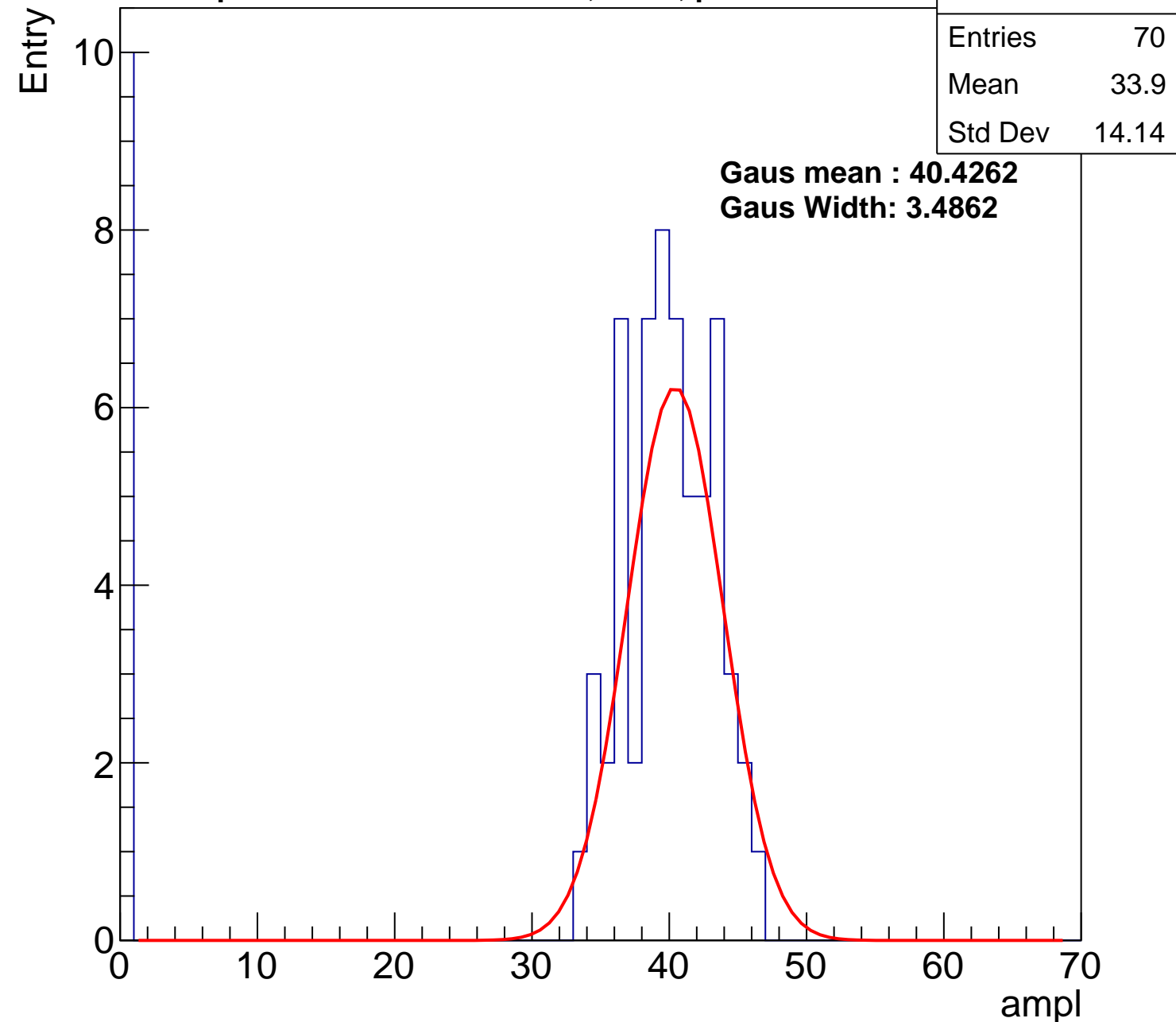
40

50

60

70

ampl

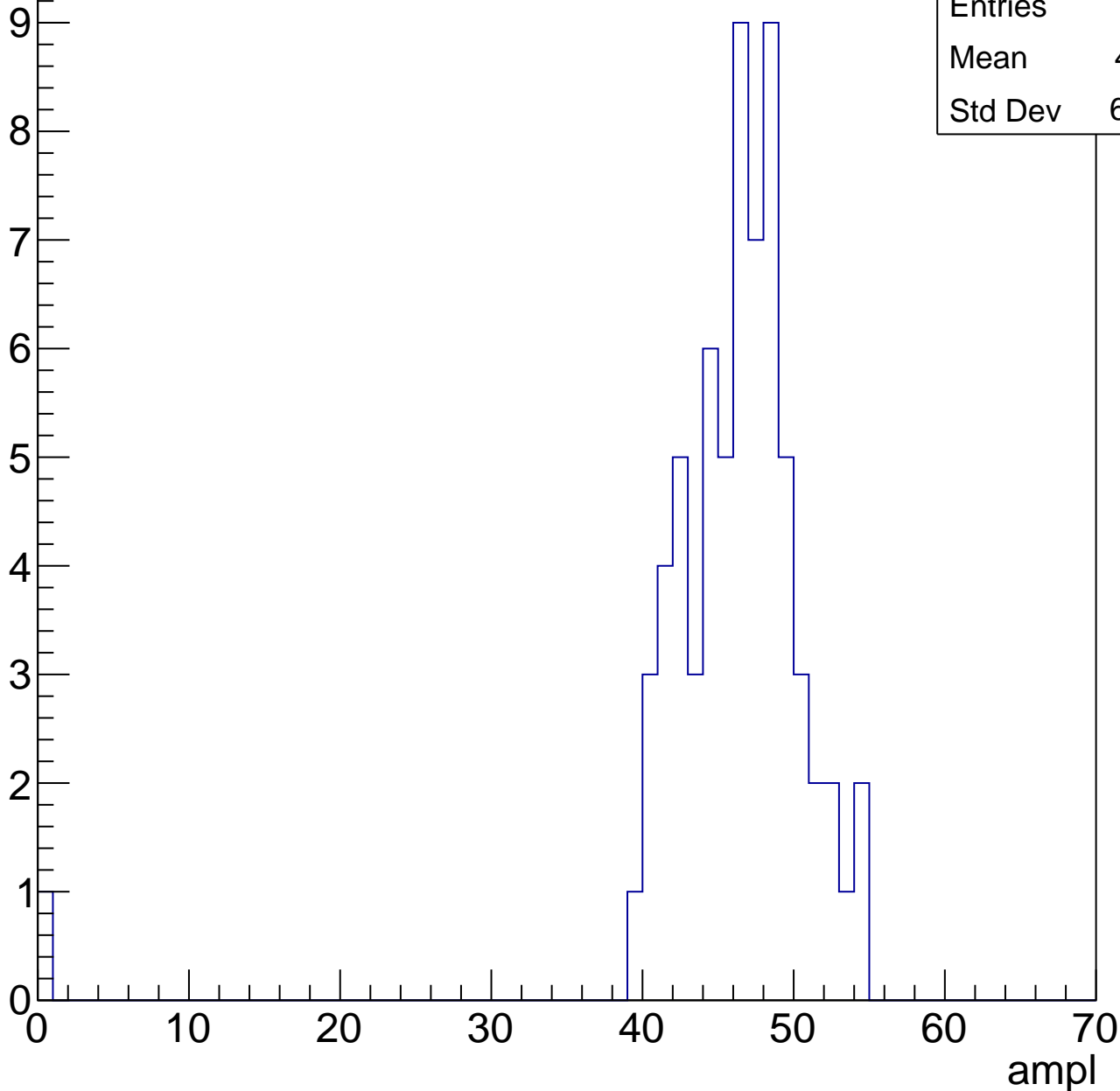


B1L103S, U7-ch46, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	45.41
Std Dev	6.553

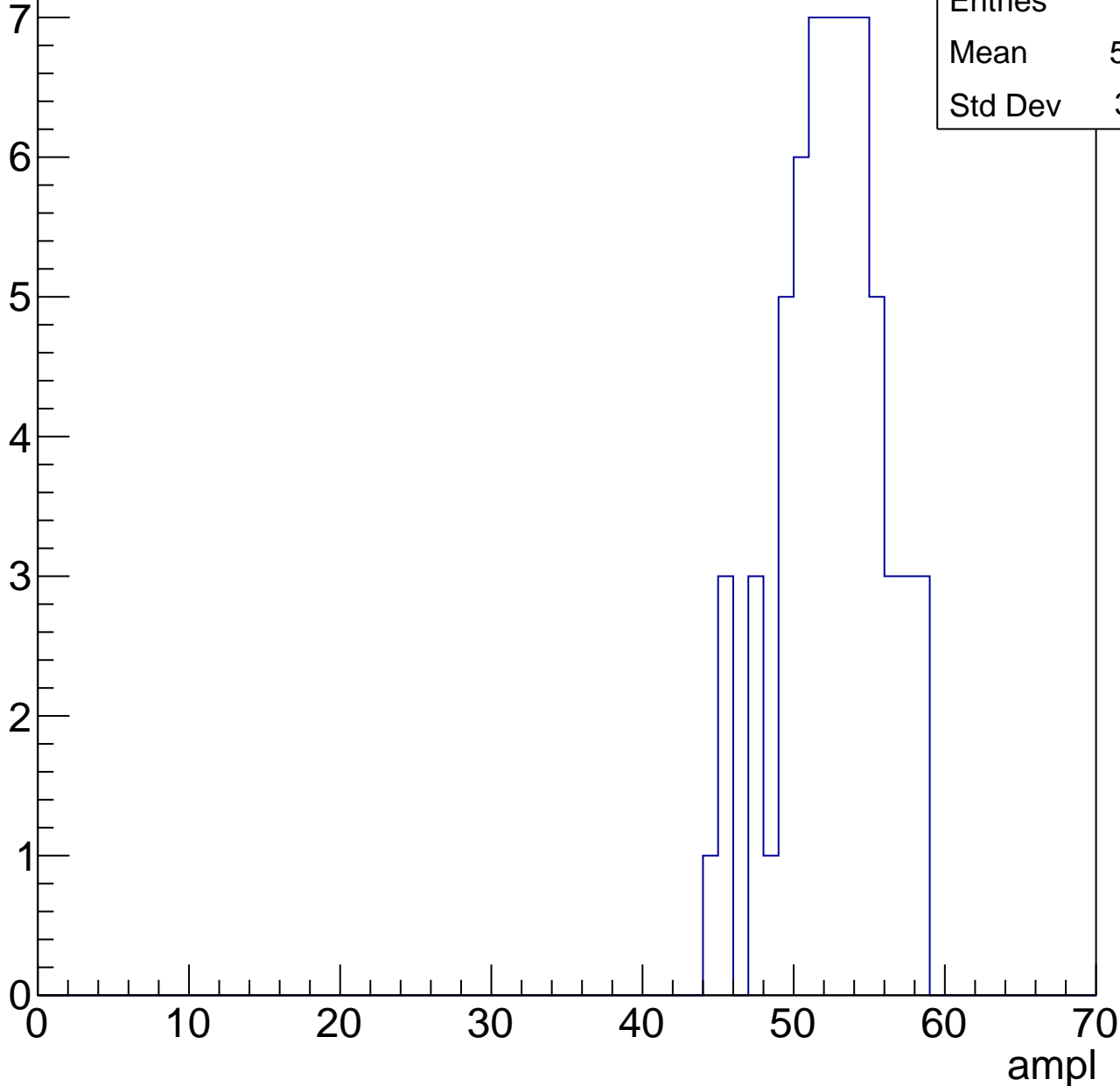


B1L103S, U7-ch46, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

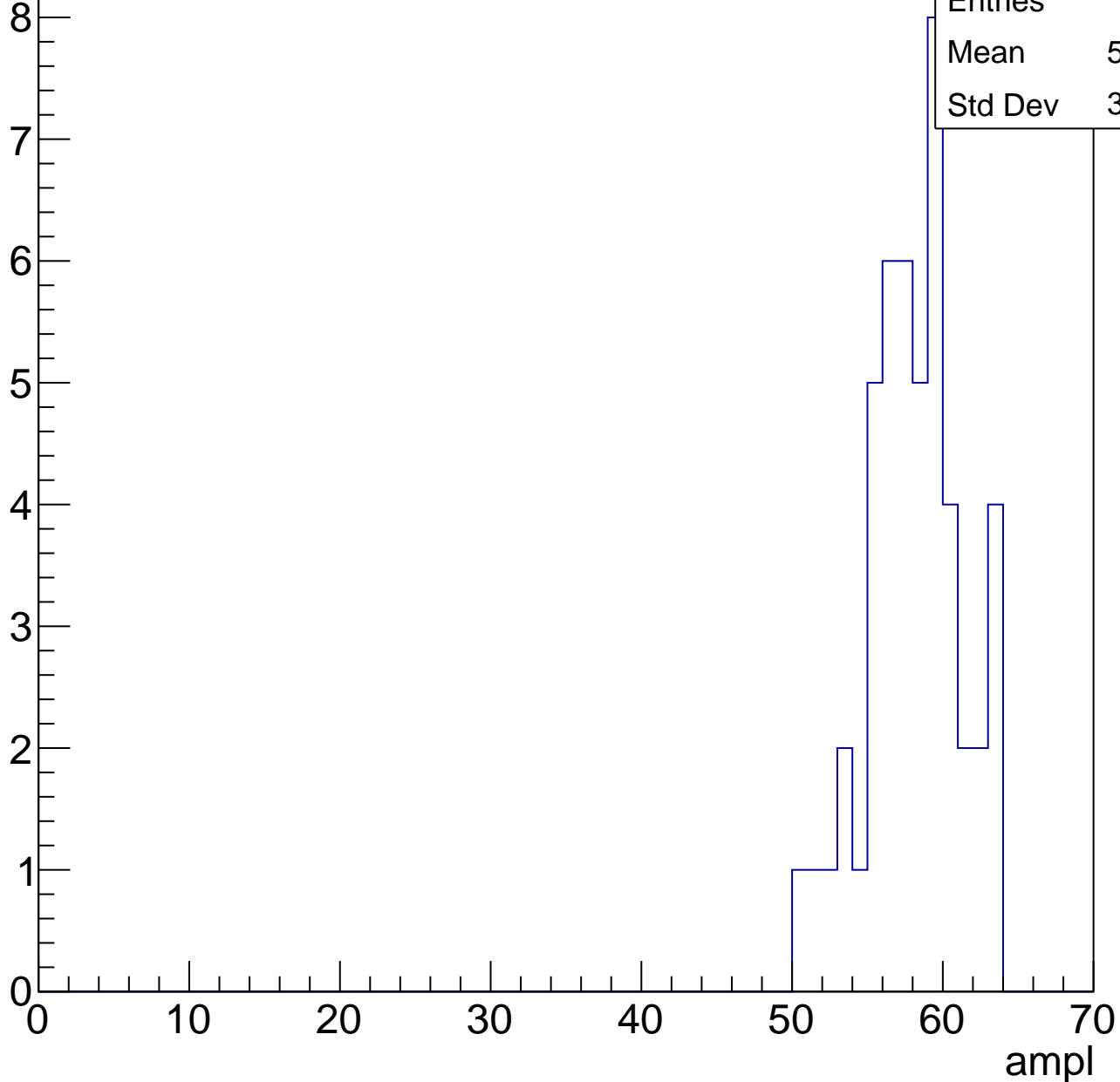
Entries	61
Mean	51.98
Std Dev	3.361



B1L103S, U7-ch46, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



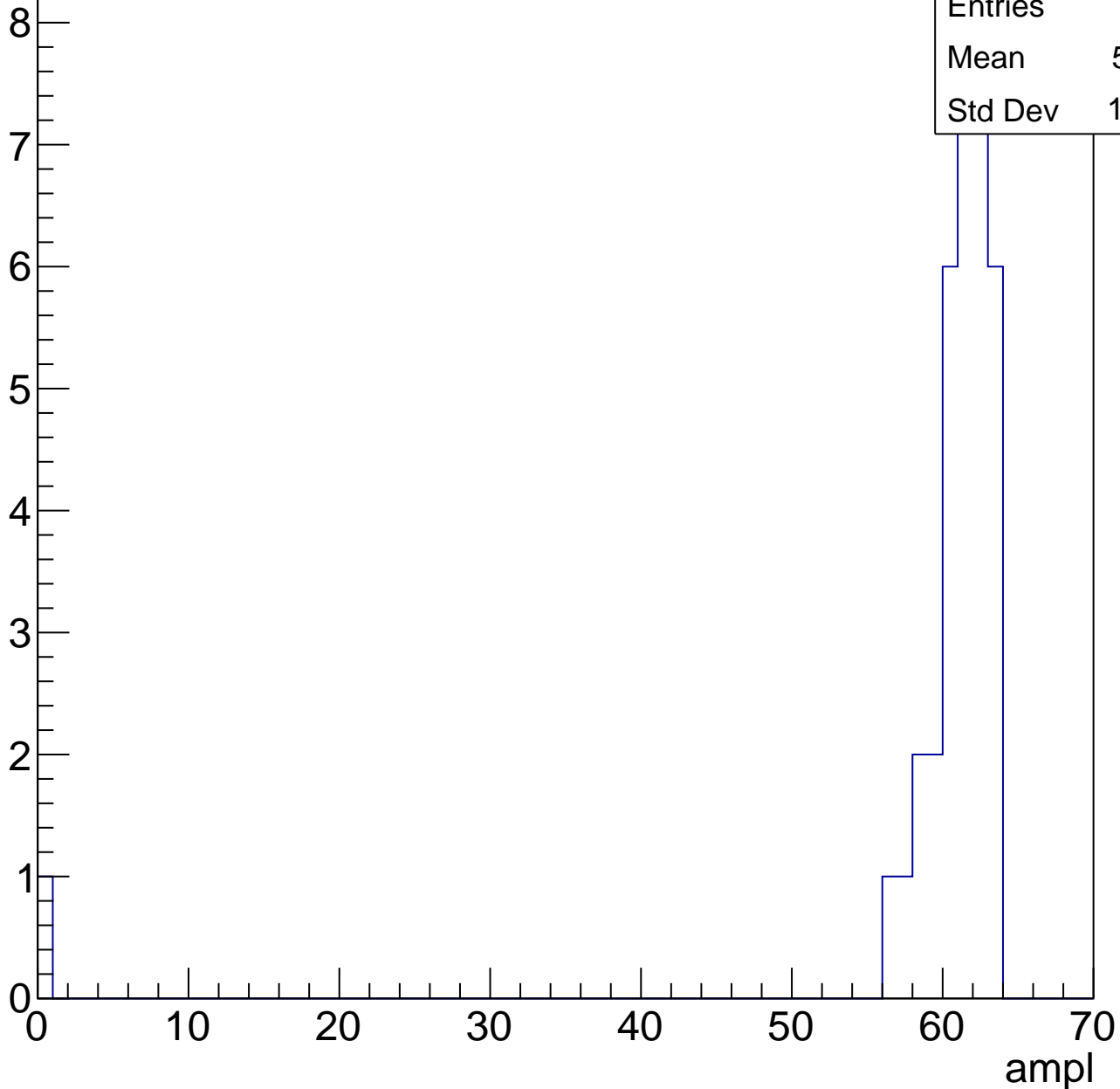
Entries	48
Mean	57.62
Std Dev	3.086

B1L103S, U7-ch46, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	35
Mean	59.11
Std Dev	10.28



B1L103S, U7-ch46, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch47, adc0

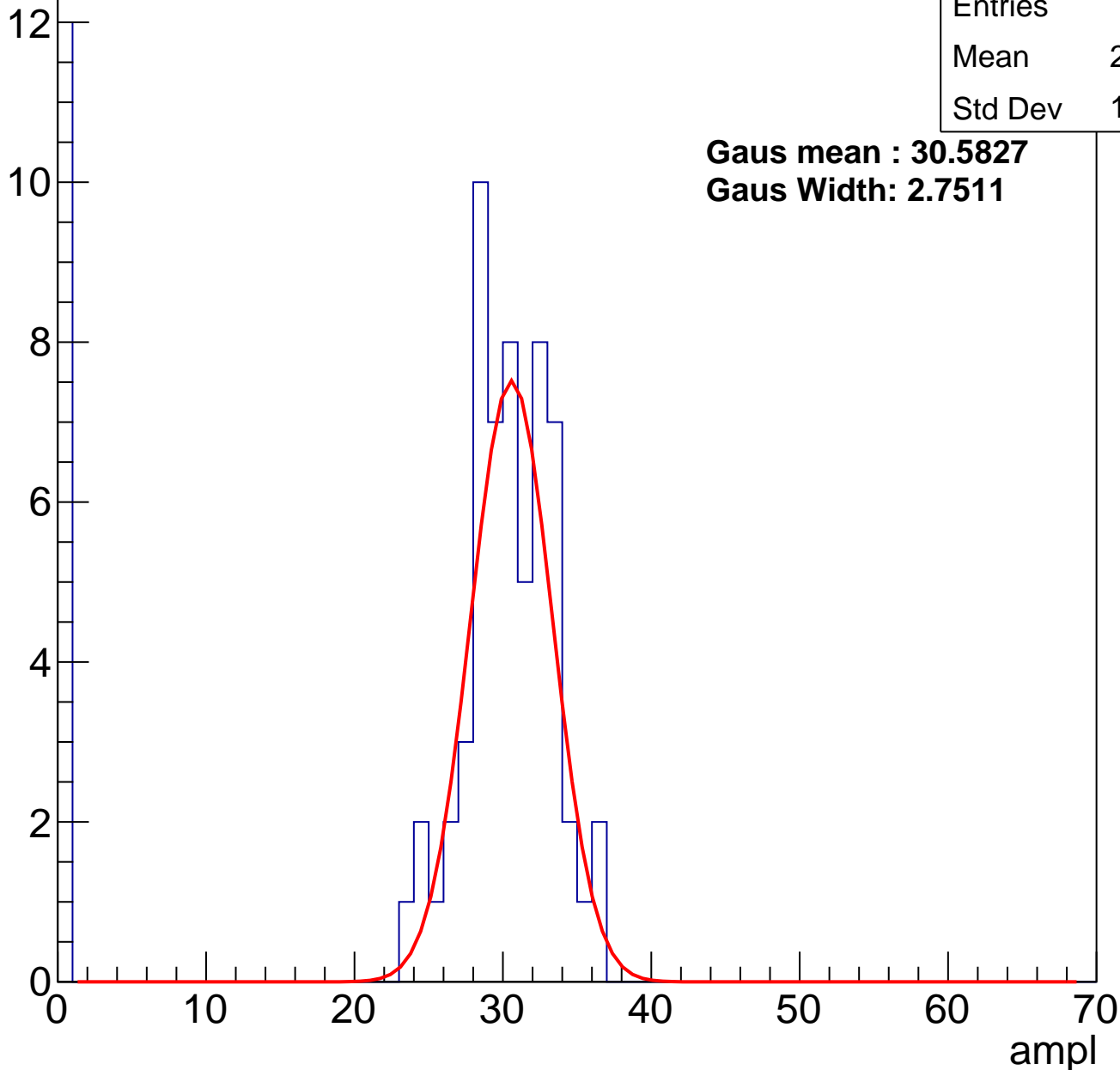
calib_packv5_041523_1651.root, FC#0, port C2

Entries	71
Mean	24.92
Std Dev	11.53

Gaus mean : 30.5827

Gaus Width: 2.7511

Entry



B1L103S, U7-ch47, adc1

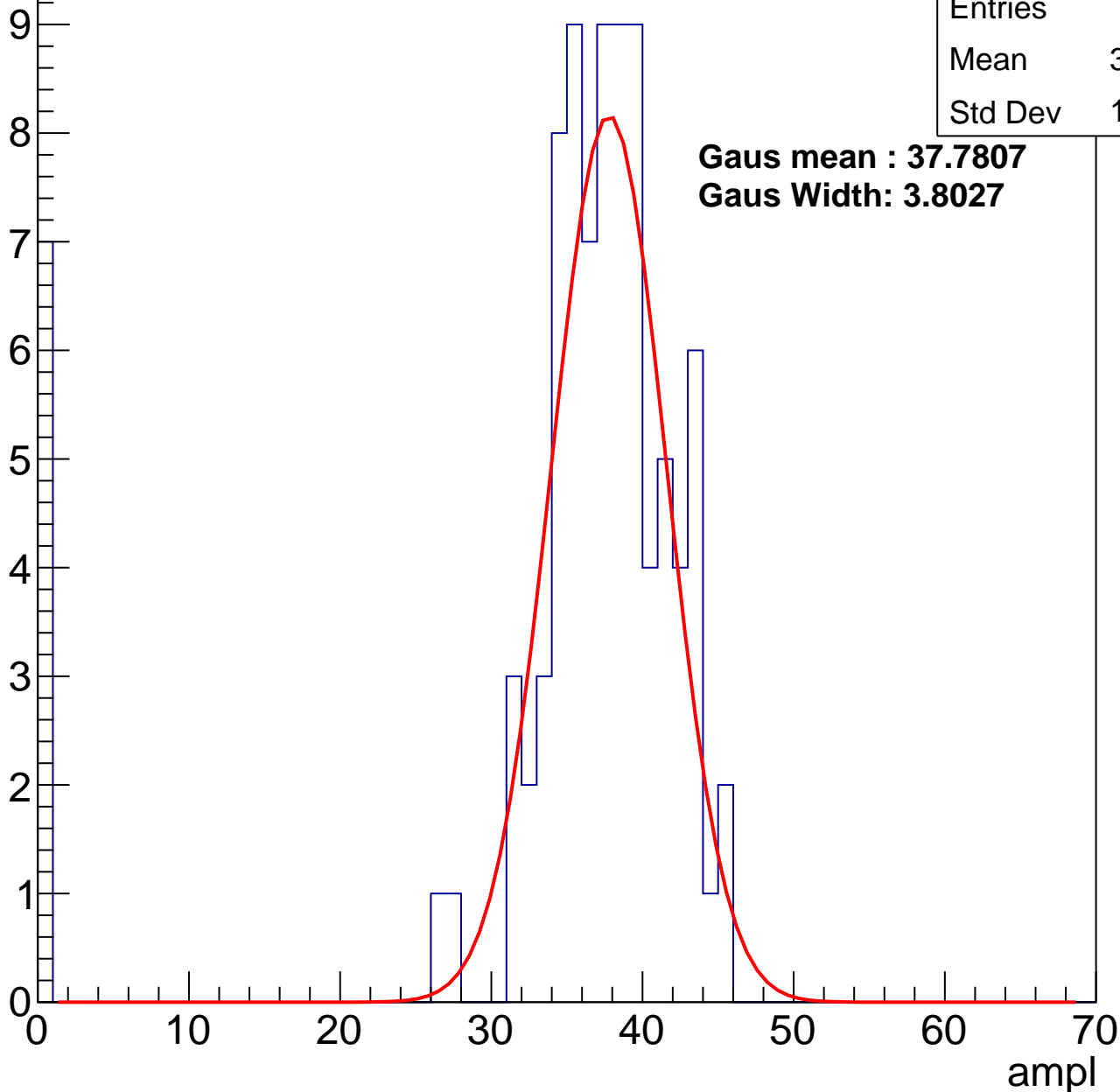
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	90
Mean	34.43
Std Dev	10.64

Gaus mean : 37.7807

Gaus Width: 3.8027



B1L103S, U7-ch47, adc2

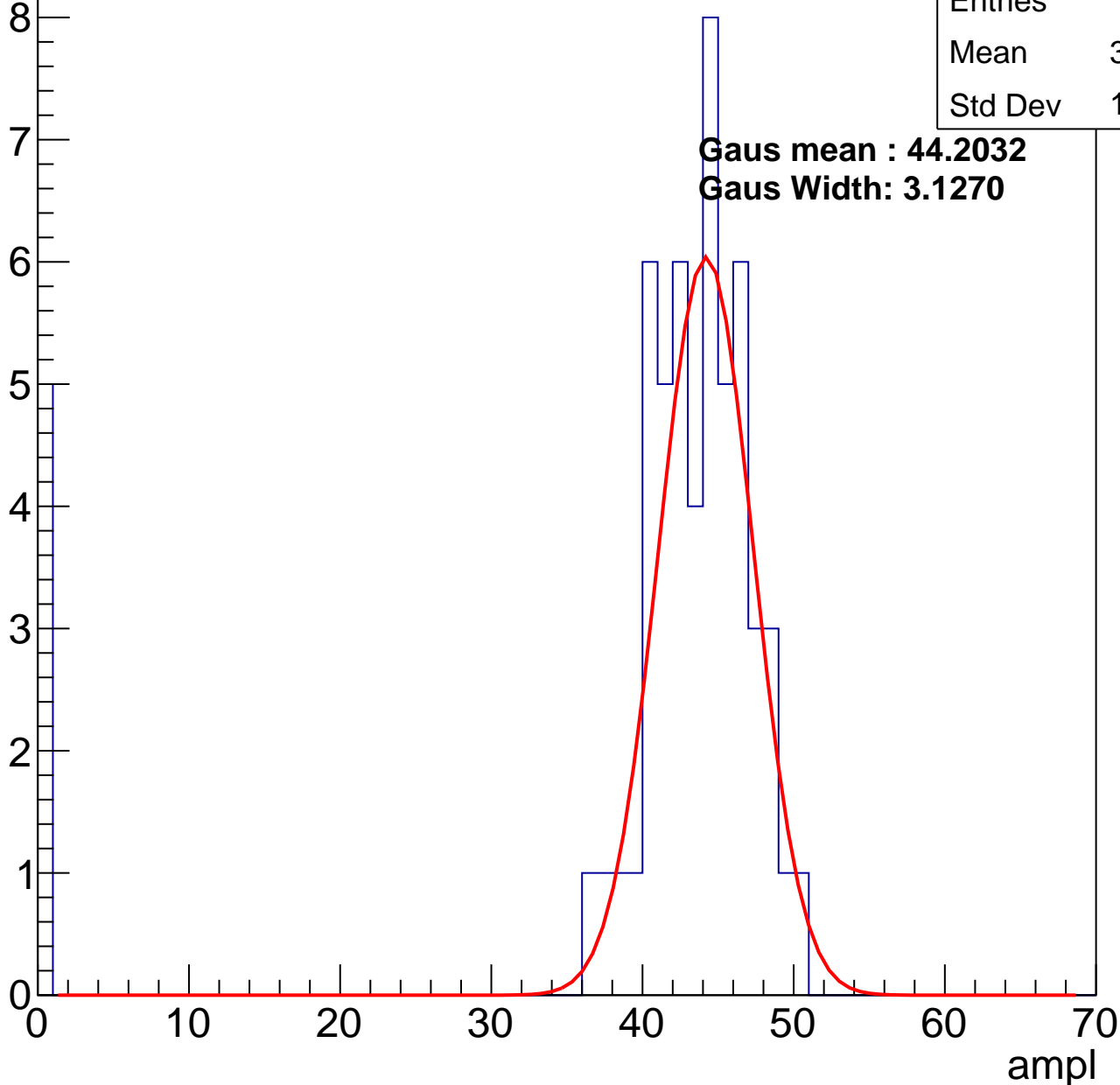
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	39.58
Std Dev	12.62

Gaus mean : 44.2032

Gaus Width: 3.1270

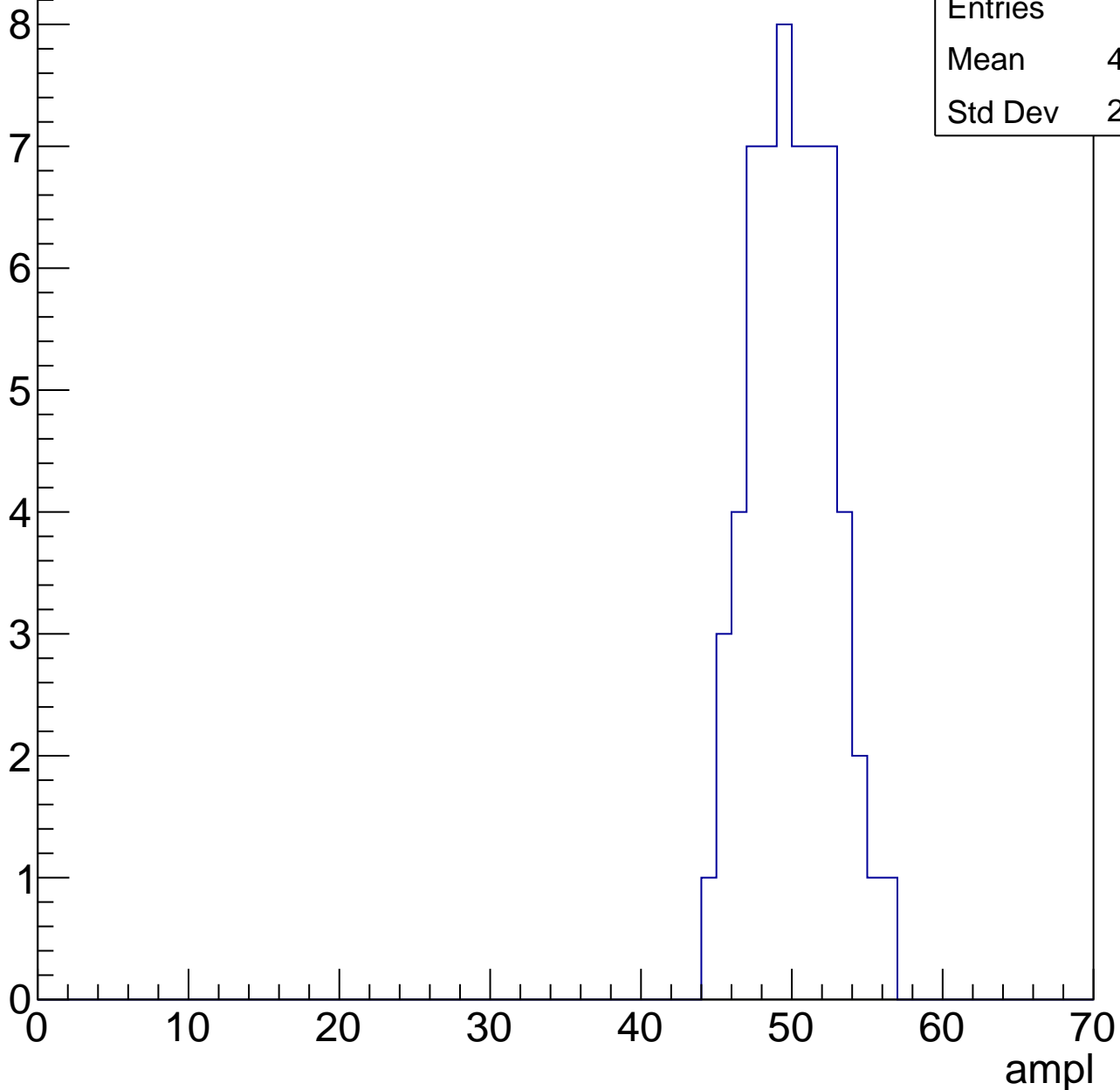


B1L103S, U7-ch47, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	49.53
Std Dev	2.683

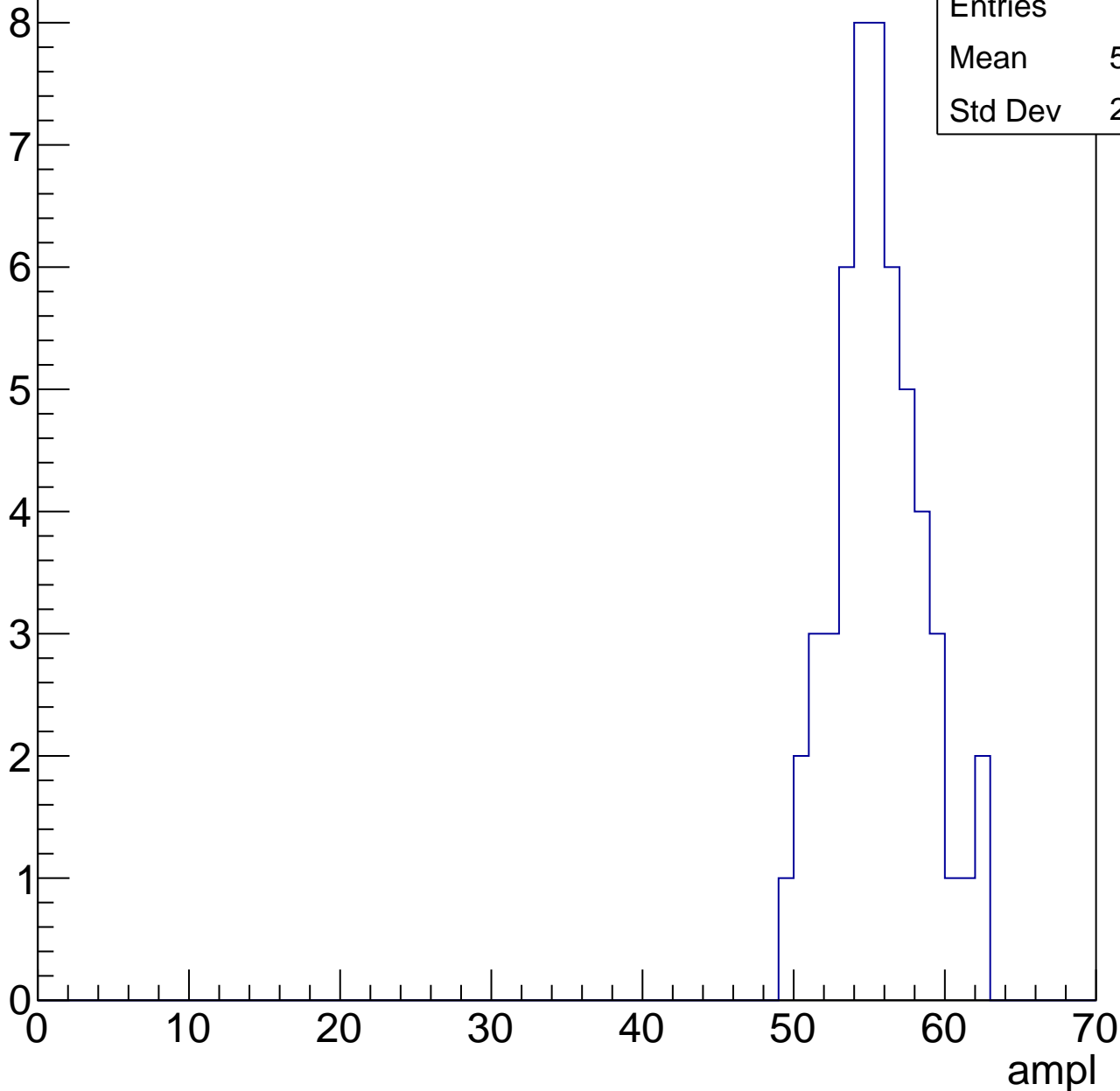


B1L103S, U7-ch47, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

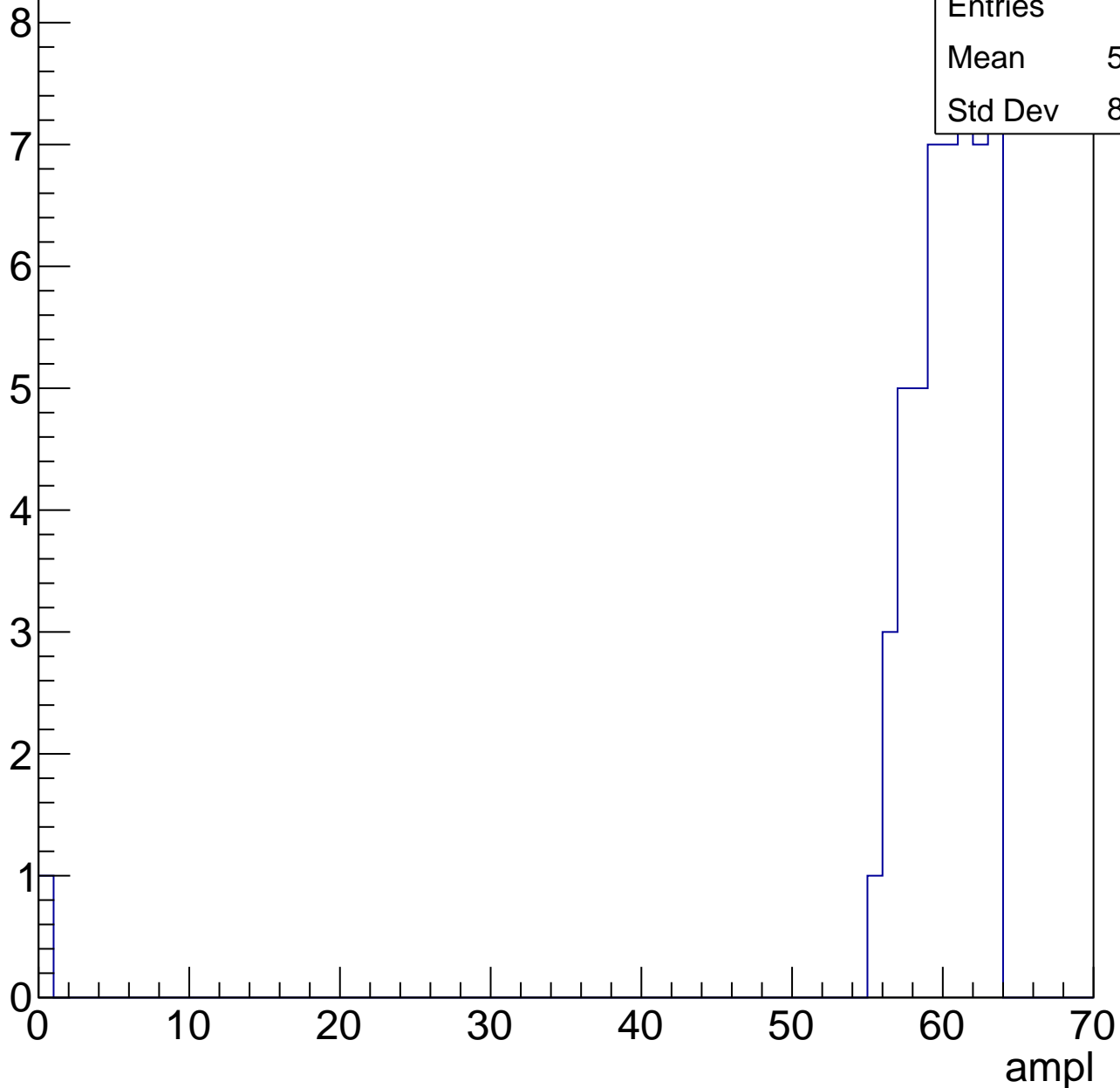
Entries	53
Mean	55.15
Std Dev	2.949



B1L103S, U7-ch47, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch47, adc6

calib_packv5_041523_1651.root, FC#0, port C2

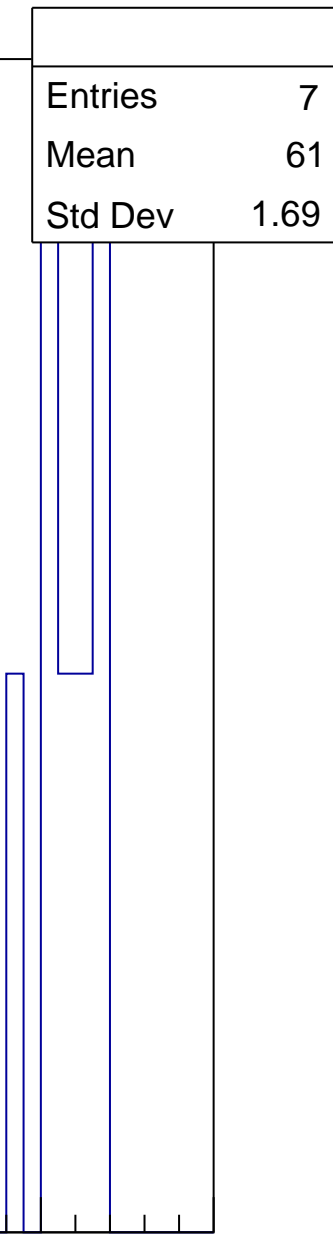
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	7
Mean	61
Std Dev	1.69

0 10 20 30 40 50 60 70

ampl



B1L103S, U7-ch47, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U7-ch48, adc0

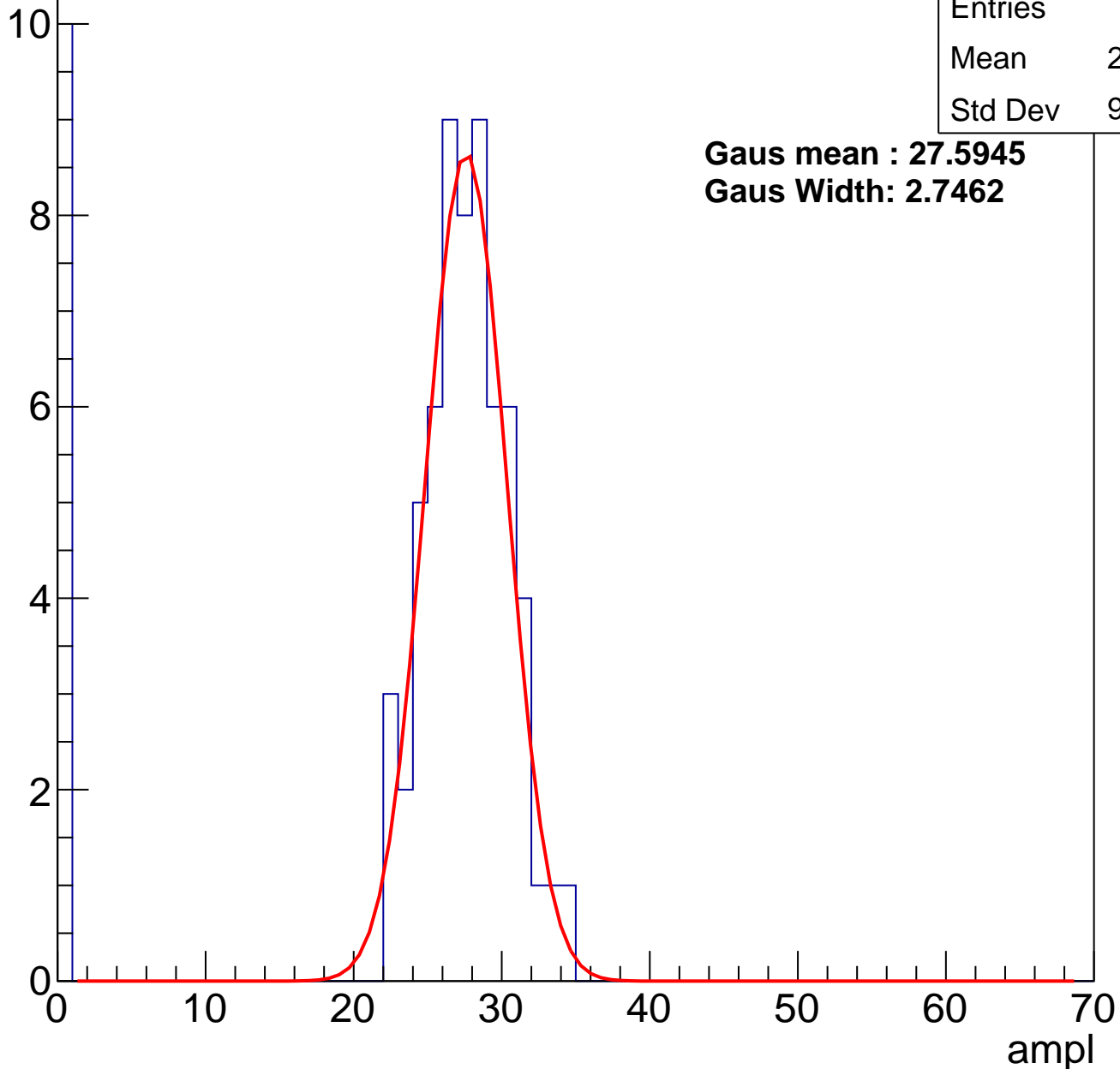
calib_packv5_041523_1651.root, FC#0, port C2

Entries	71
Mean	23.39
Std Dev	9.796

Gaus mean : 27.5945

Gaus Width: 2.7462

Entry



B1L103S, U7-ch48, adc1

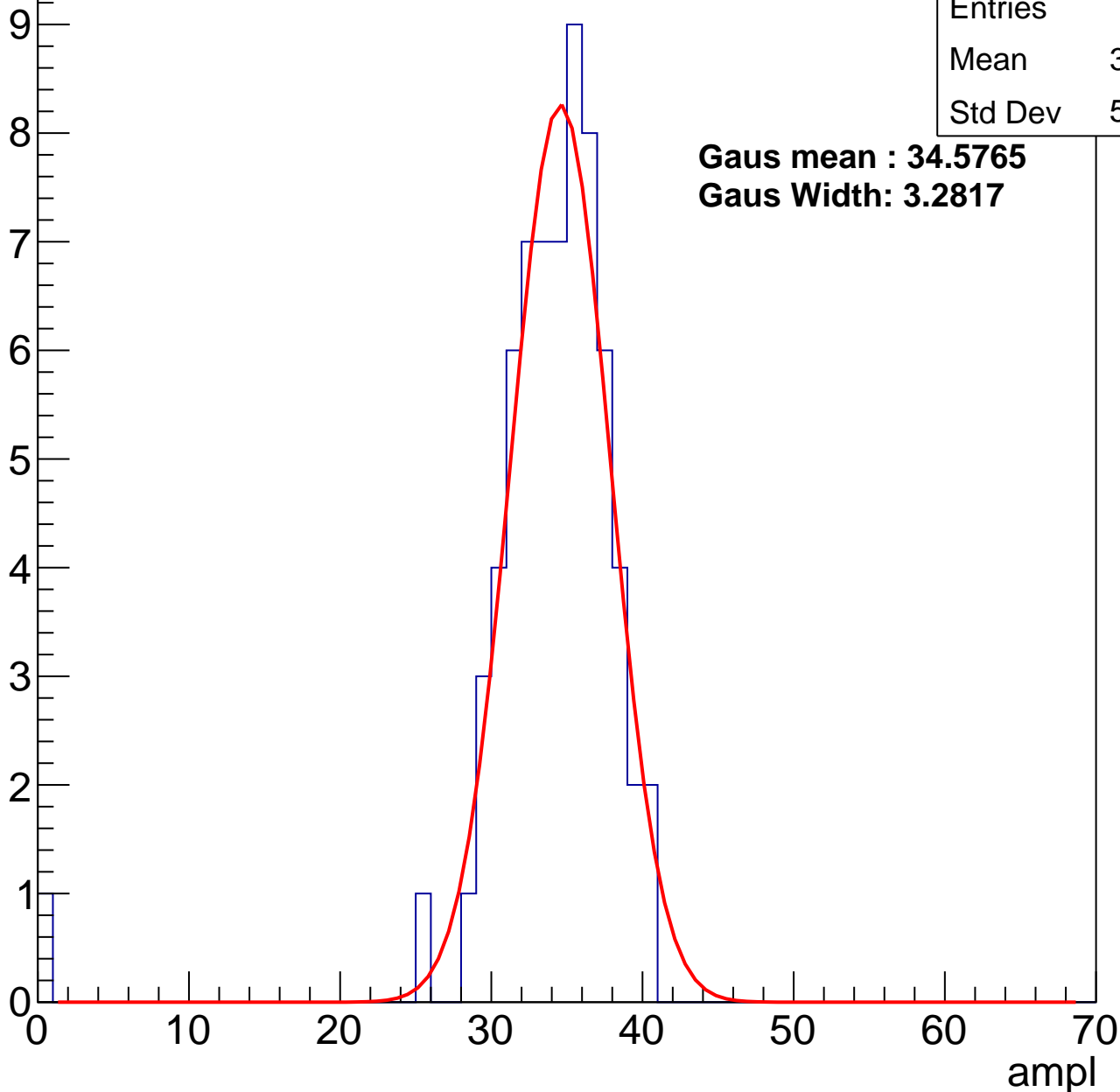
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	33.44
Std Dev	5.089

Gaus mean : 34.5765

Gaus Width: 3.2817



B1L103S, U7-ch48, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

12
10
8
6
4
2
0

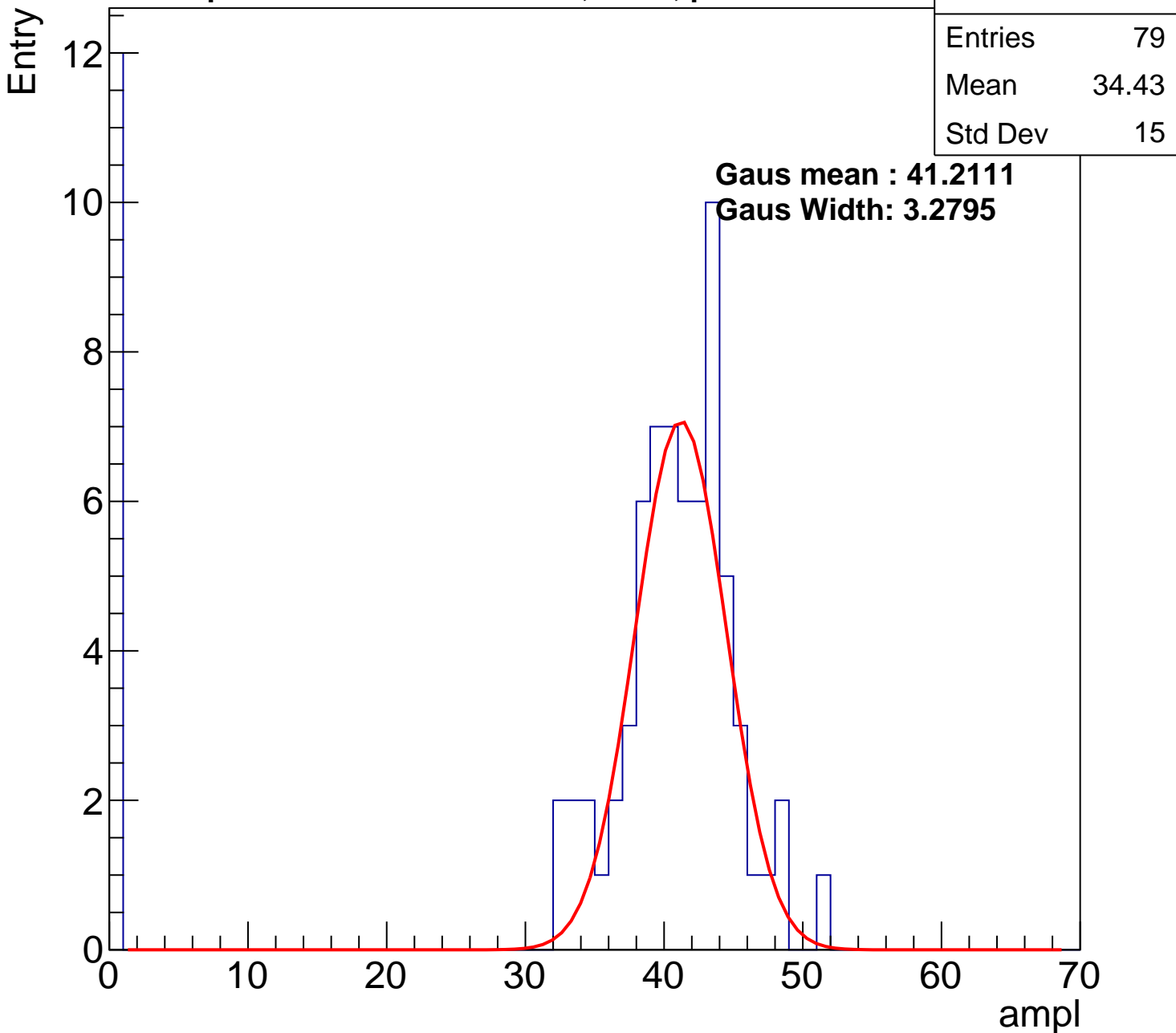
Entries	79
Mean	34.43
Std Dev	15

Gaus mean : 41.2111

Gaus Width: 3.2795

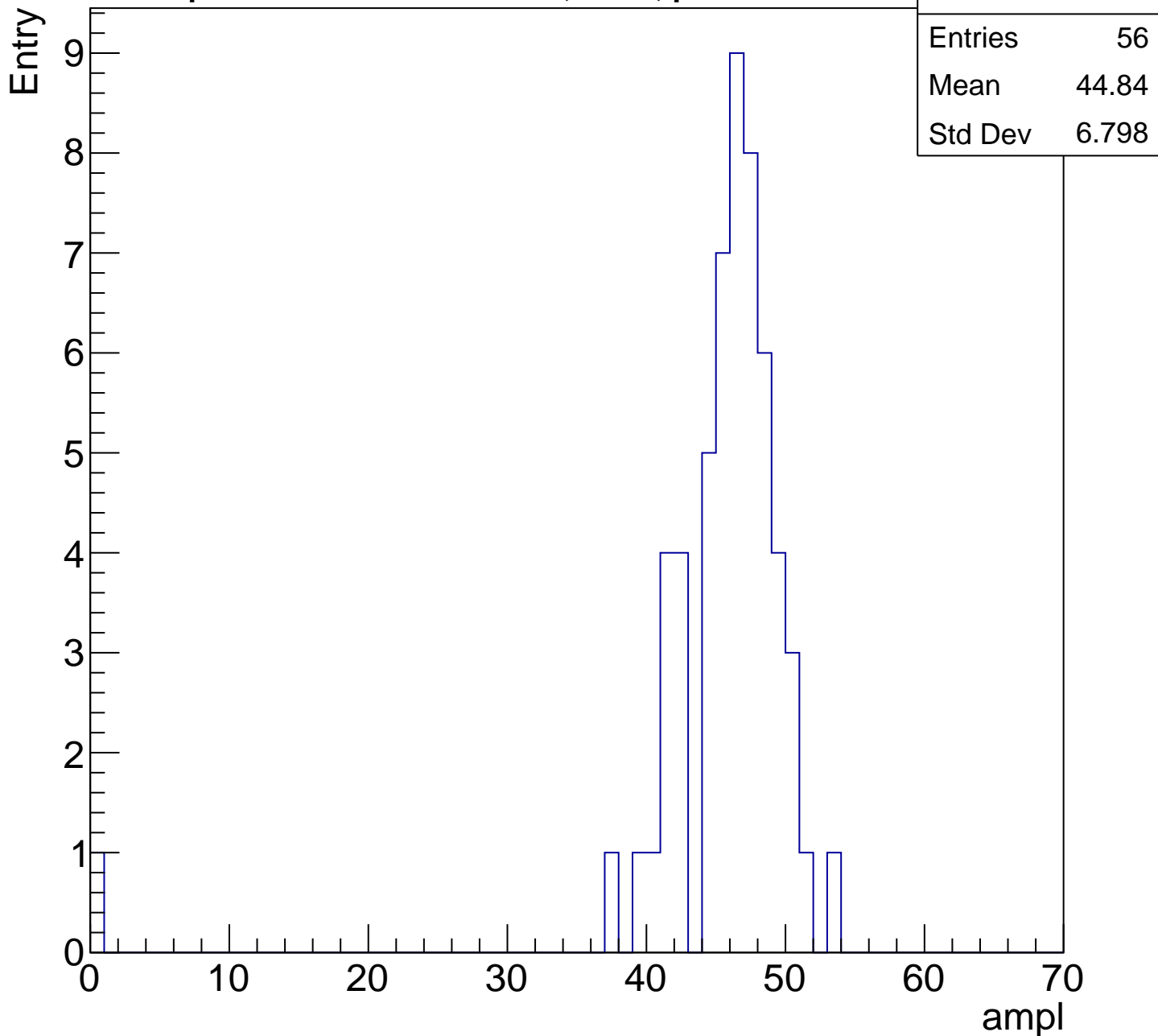
ampl

0 10 20 30 40 50 60 70



B1L103S, U7-ch48, adc3

calib_packv5_041523_1651.root, FC#0, port C2

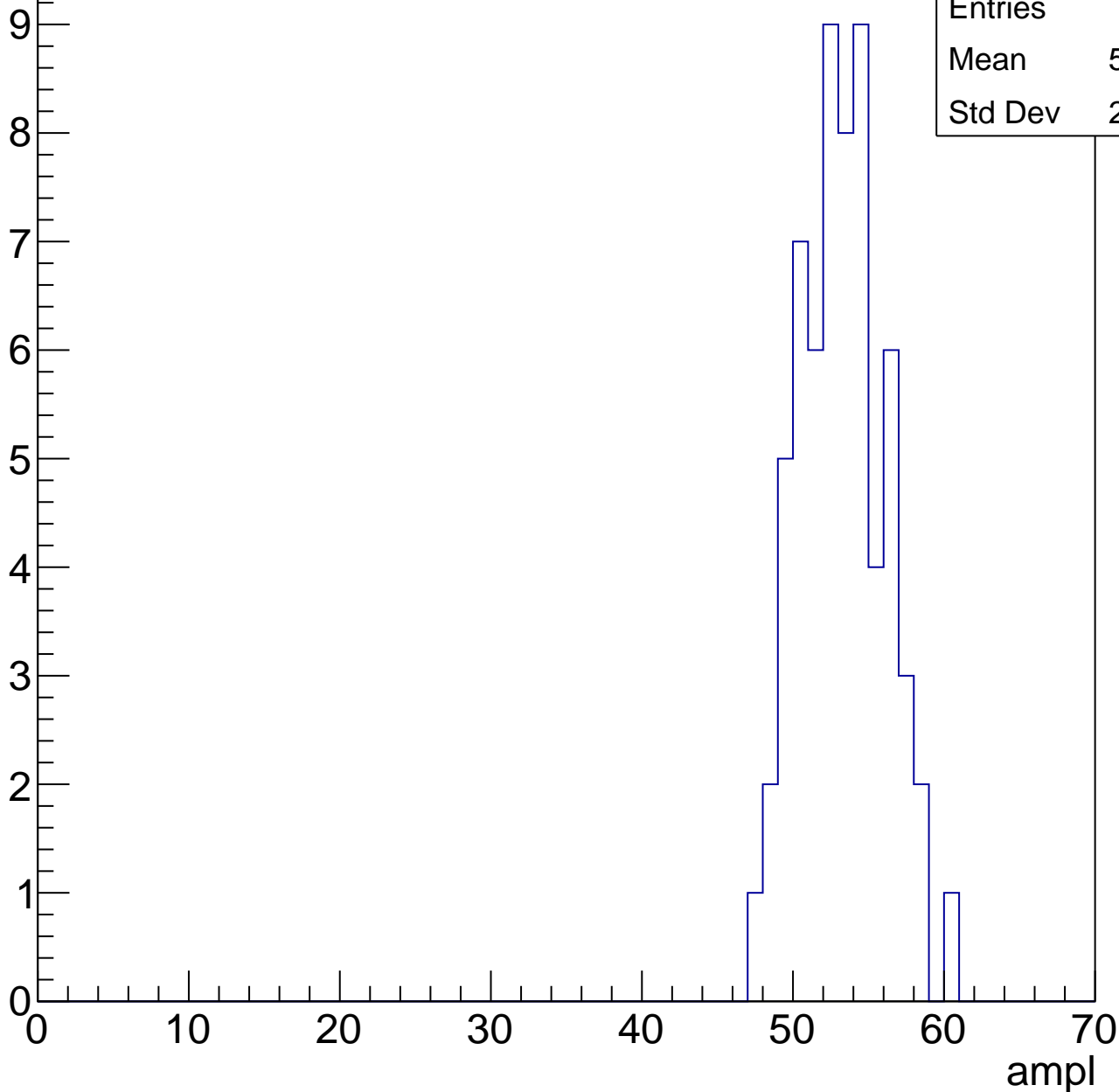


B1L103S, U7-ch48, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	52.78
Std Dev	2.774

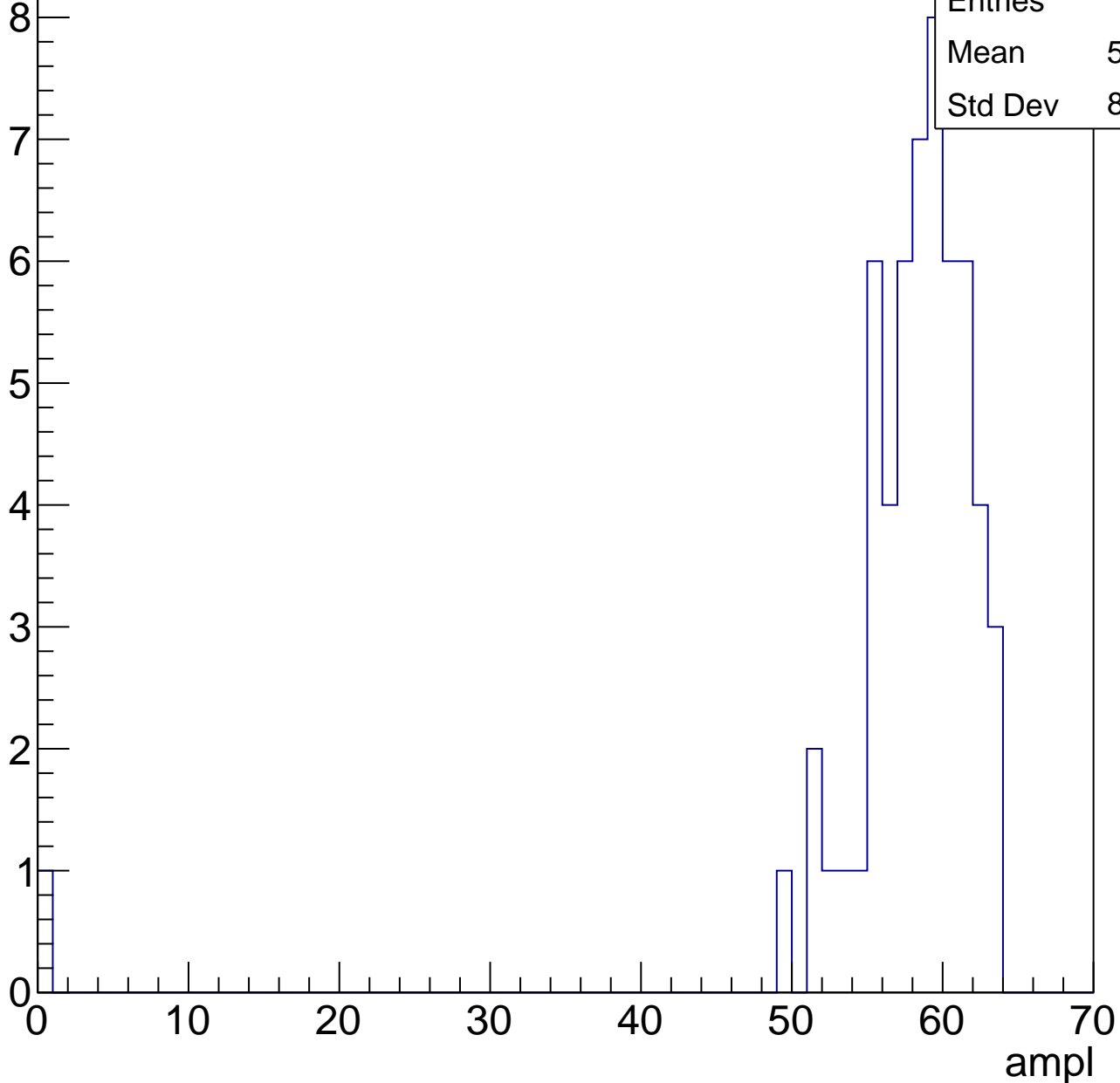


B1L103S, U7-ch48, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	56.96
Std Dev	8.229

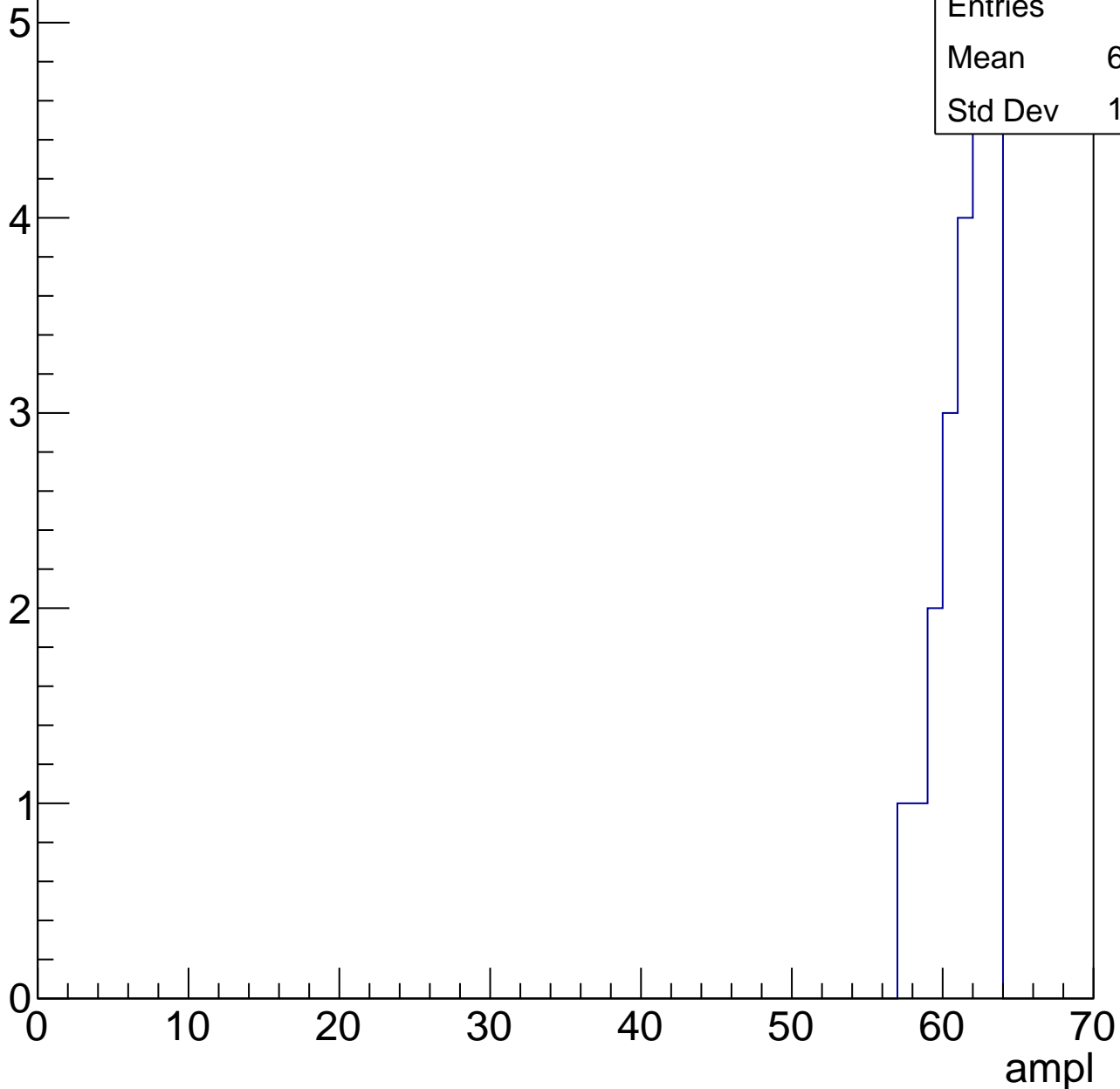


B1L103S, U7-ch48, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

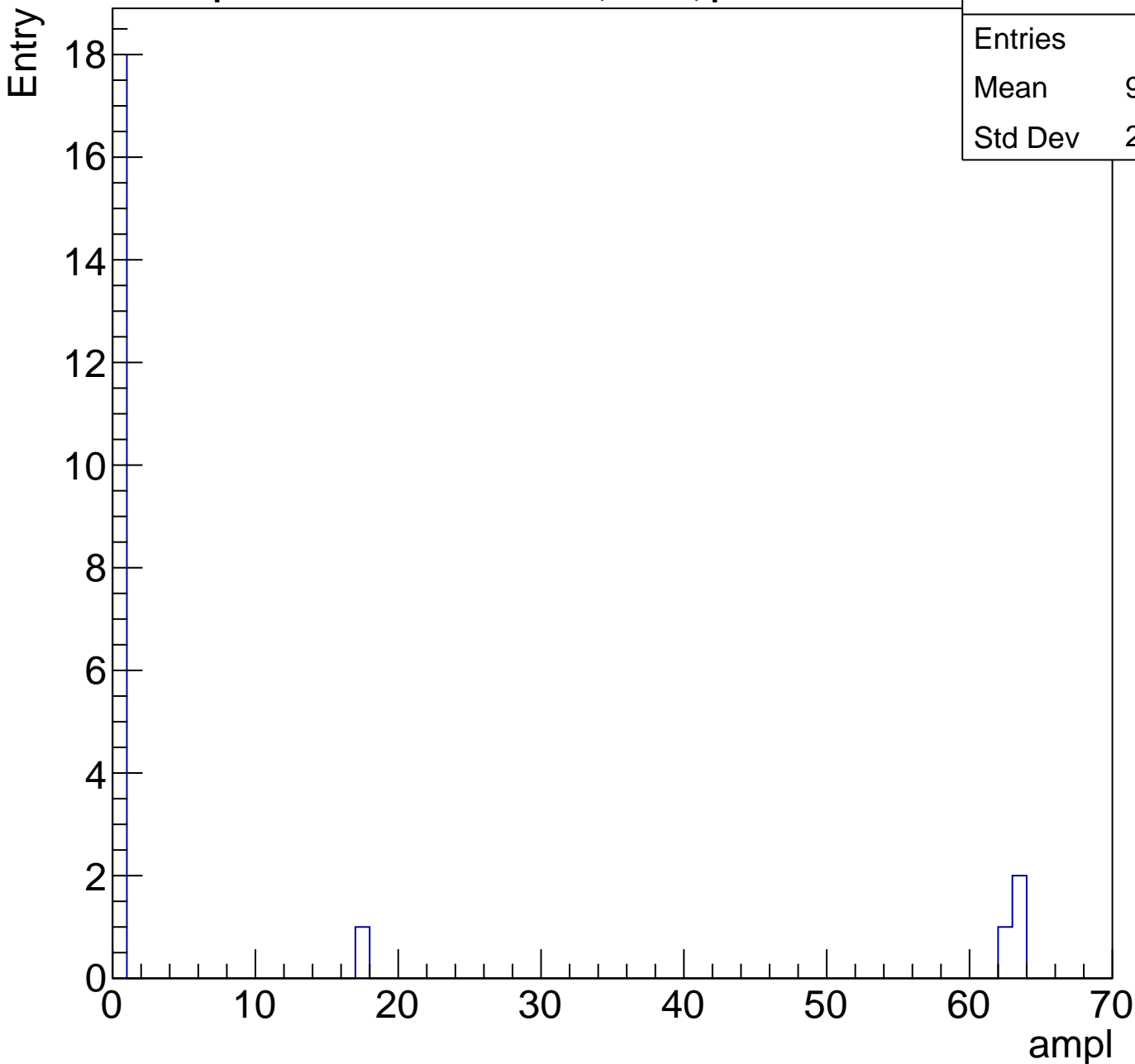
Entries	21
Mean	61.05
Std Dev	1.704



B1L103S, U7-ch48, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	22
Mean	9.318
Std Dev	21.49



B1L103S, U7-ch49, adc0

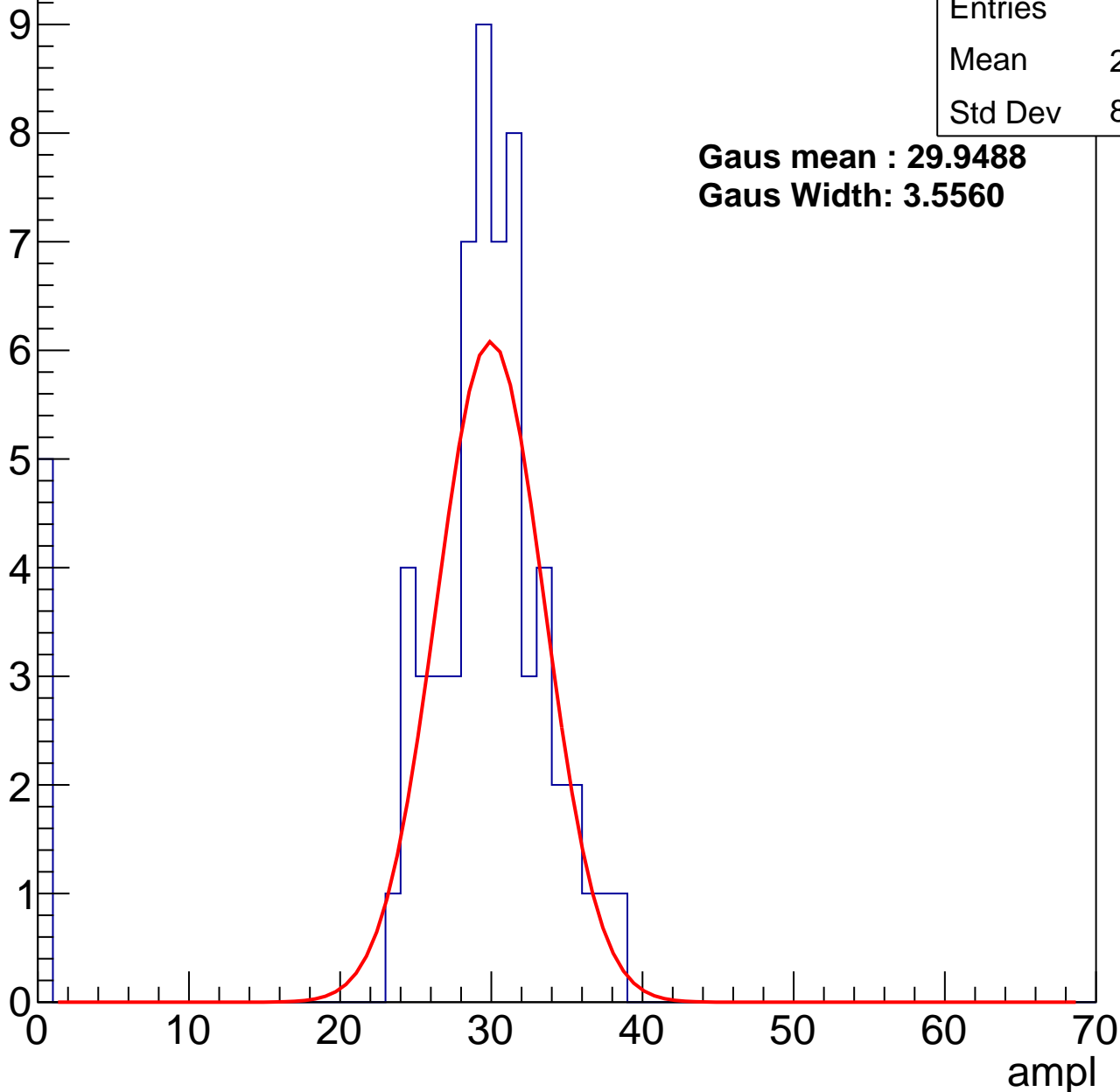
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	27.27
Std Dev	8.559

Gaus mean : 29.9488

Gaus Width: 3.5560



B1L103S, U7-ch49, adc1

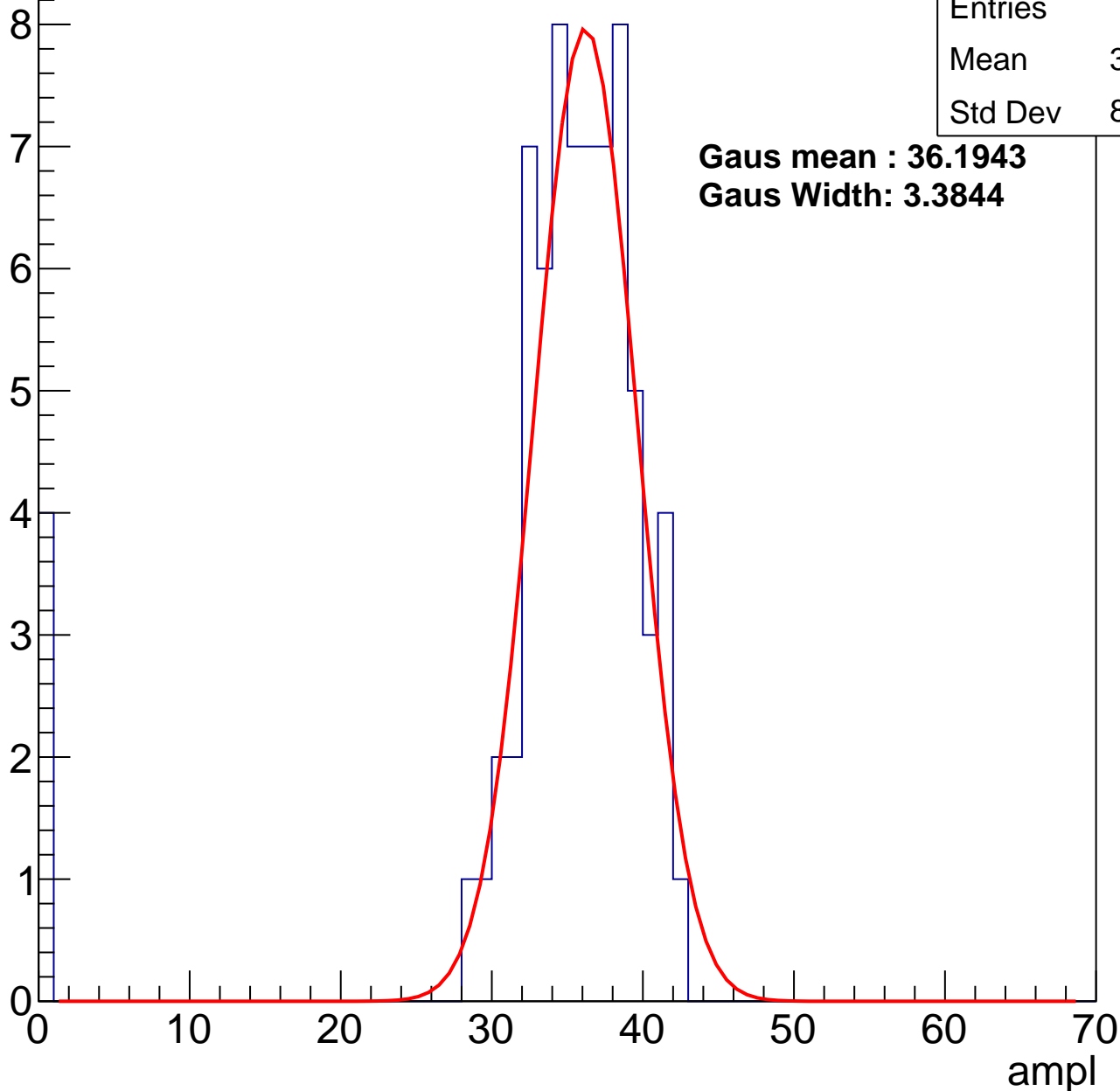
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	33.62
Std Dev	8.662

Gaus mean : 36.1943

Gaus Width: 3.3844



B1L103S, U7-ch49, adc2

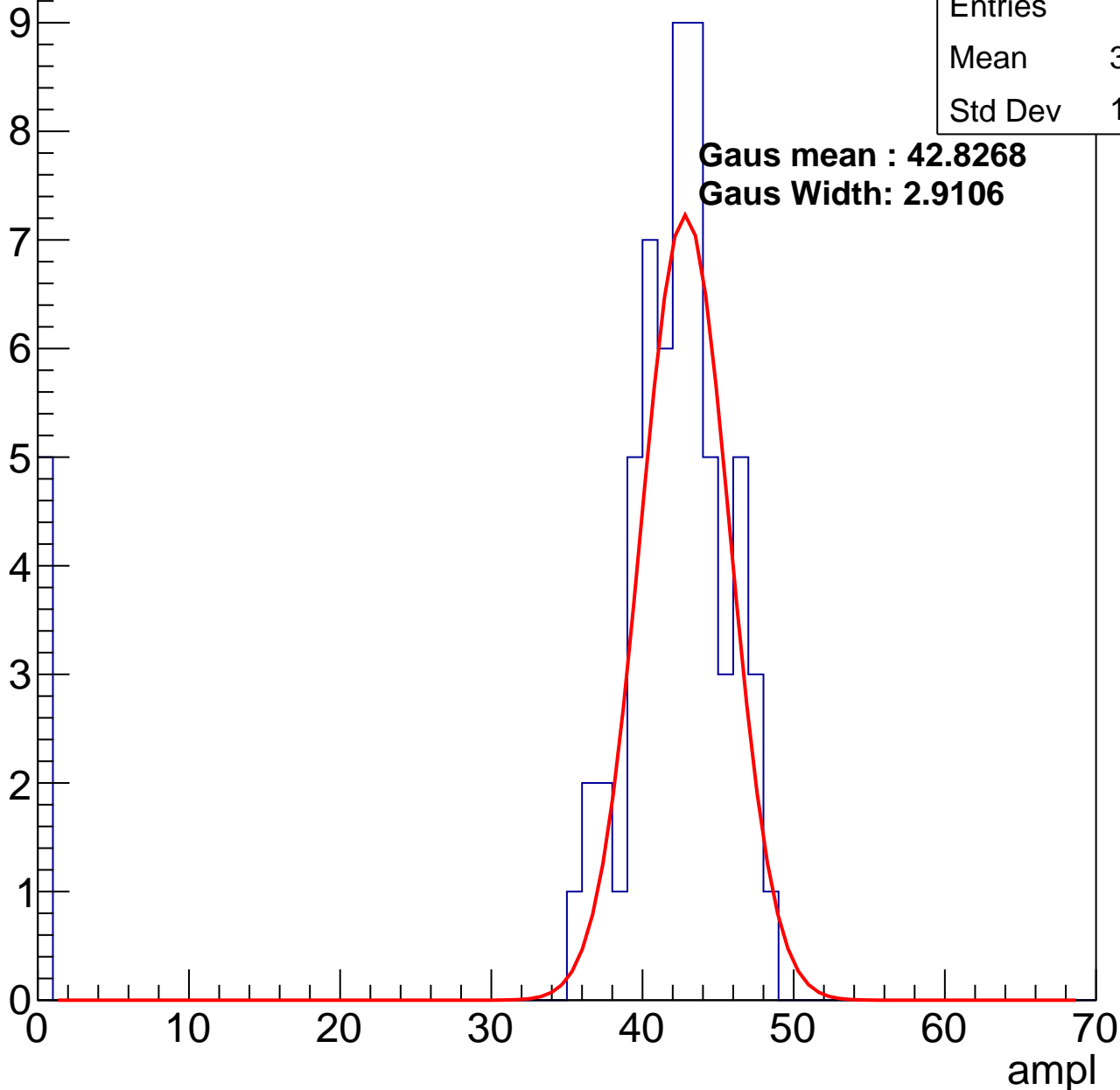
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	38.73
Std Dev	11.63

Gaus mean : 42.8268

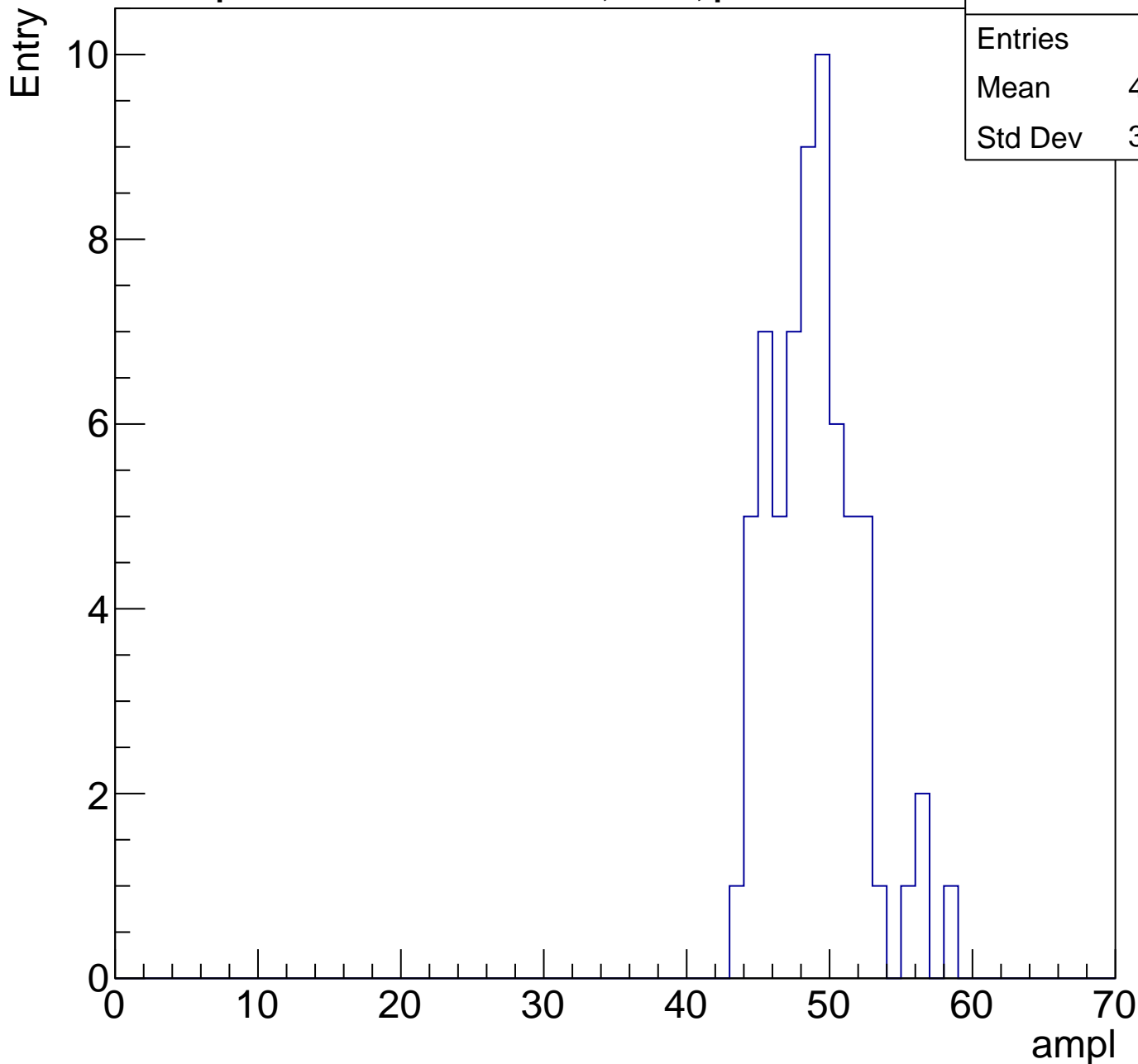
Gaus Width: 2.9106



B1L103S, U7-ch49, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	65
Mean	48.49
Std Dev	3.138

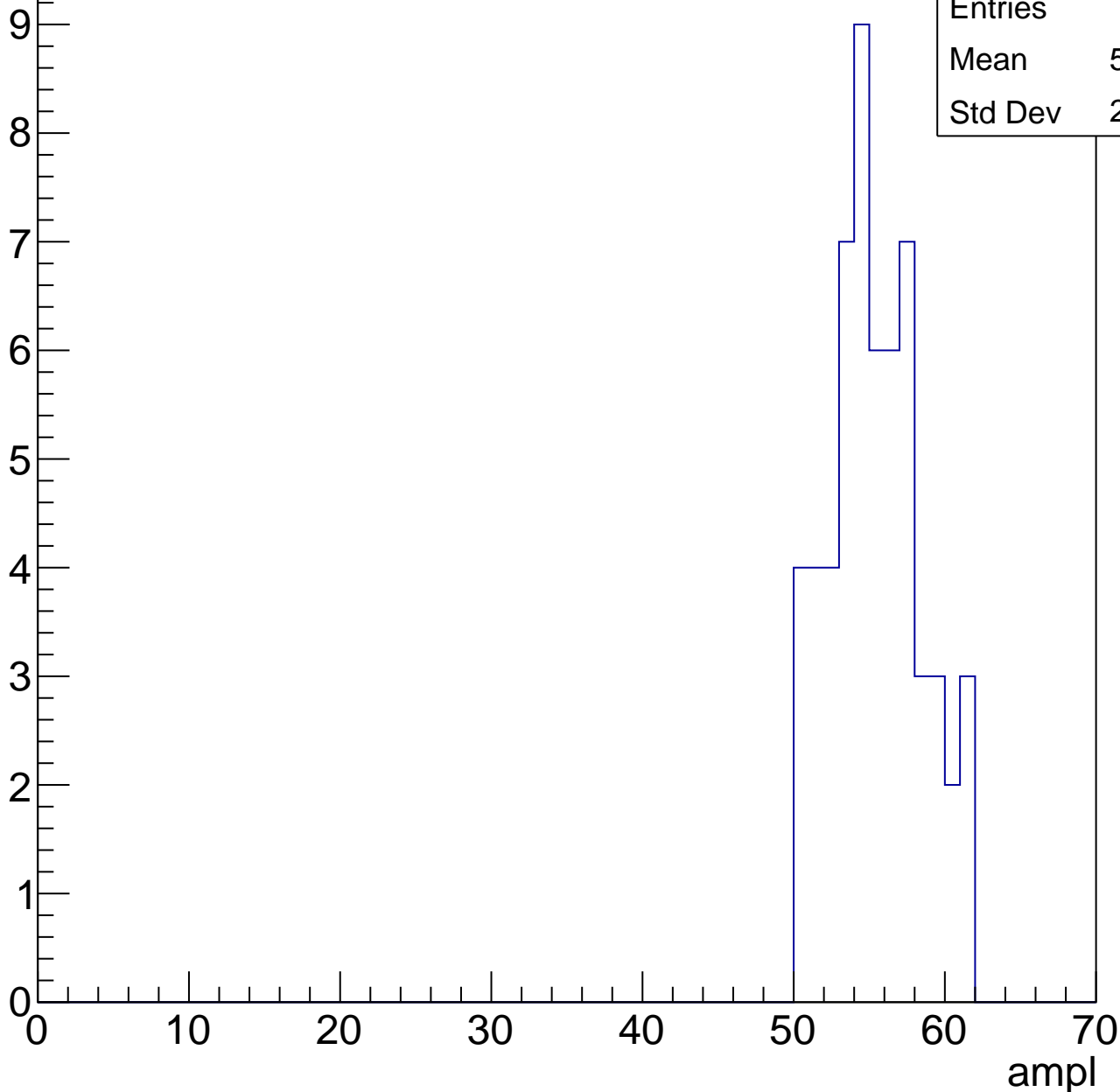


B1L103S, U7-ch49, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	54.97
Std Dev	2.948

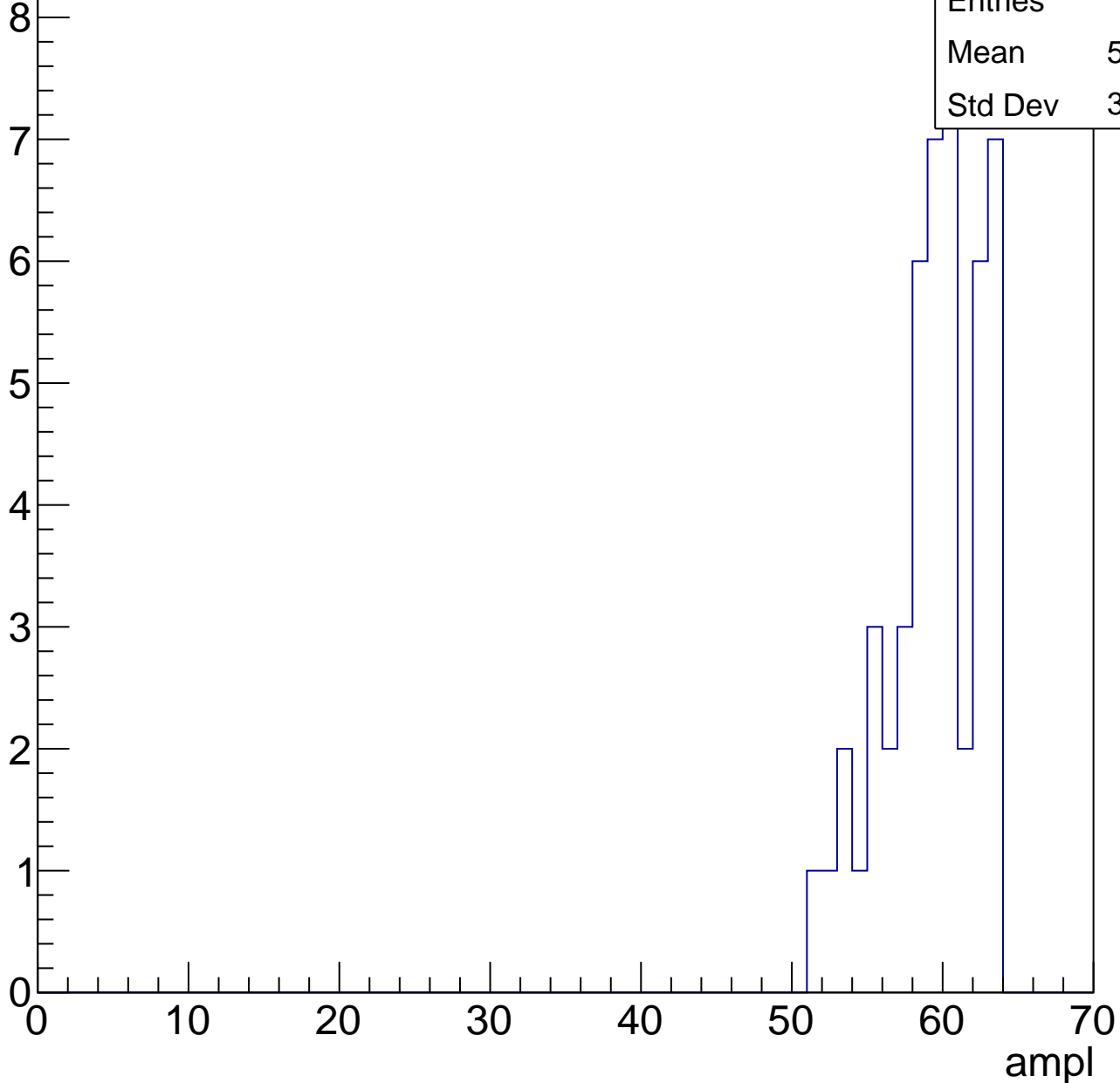


B1L103S, U7-ch49, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	58.92
Std Dev	3.116

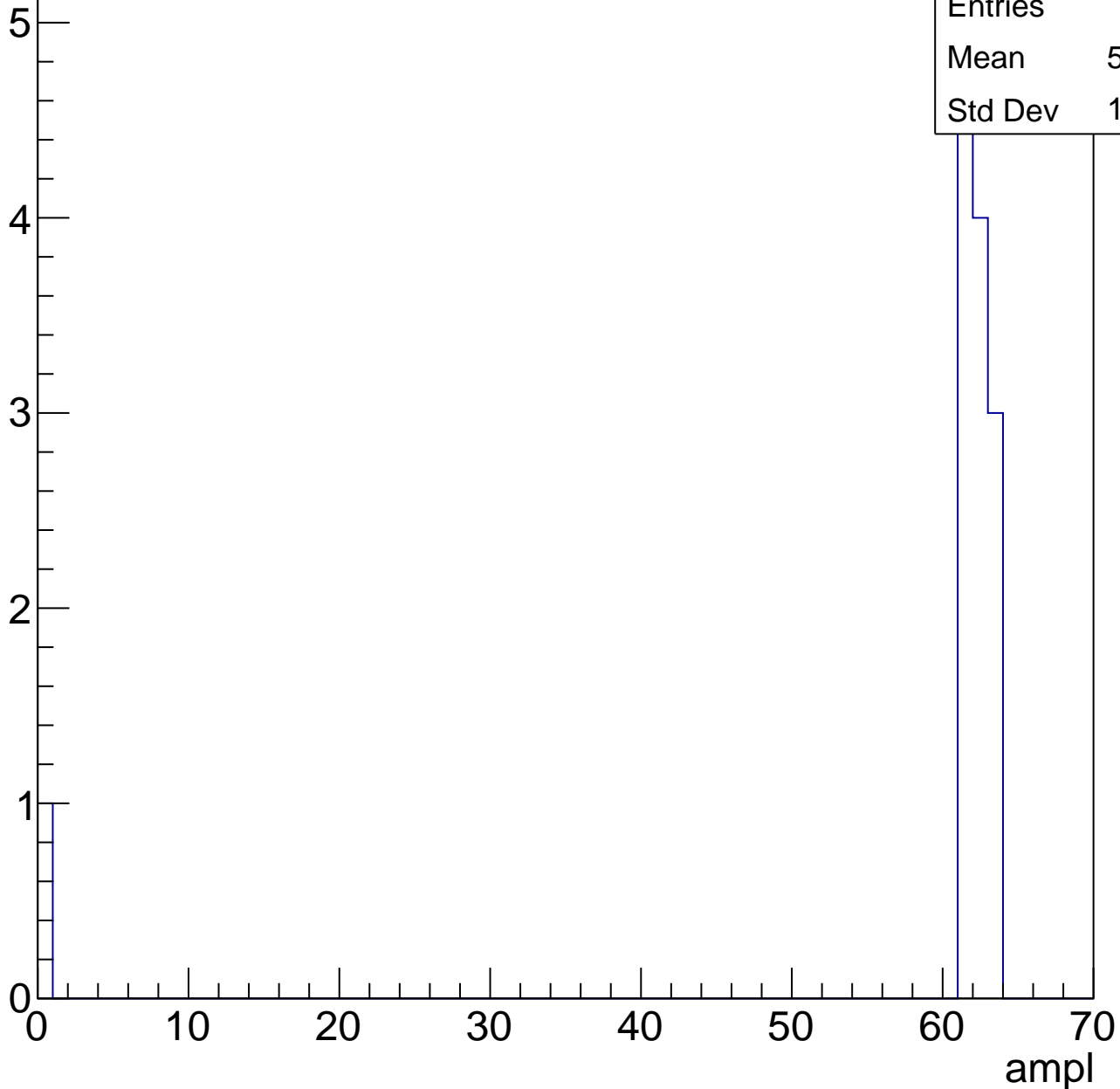


B1L103S, U7-ch49, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	13
Mean	57.08
Std Dev	16.49



B1L103S, U7-ch49, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U7-ch50, adc0

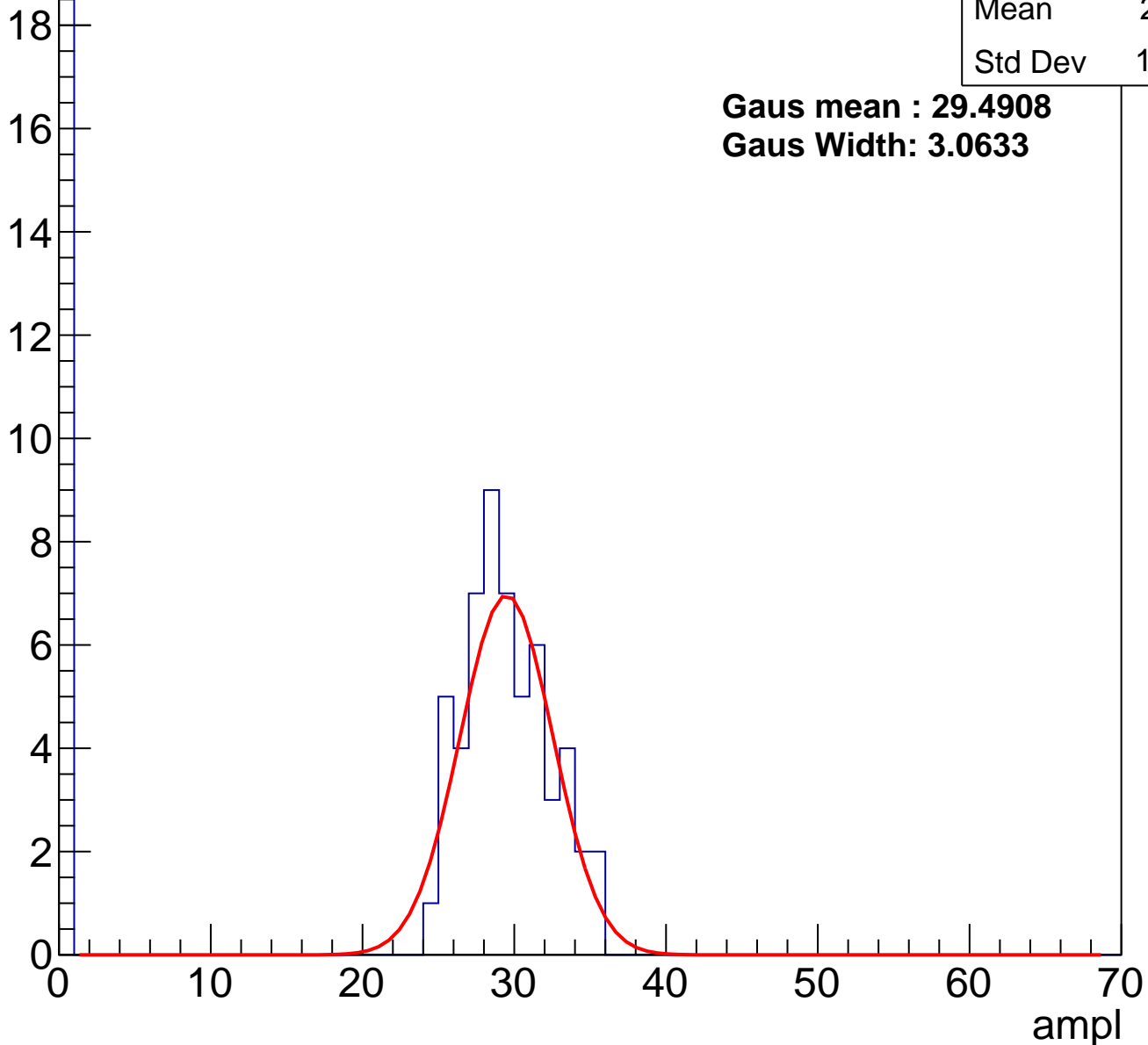
calib_packv5_041523_1651.root, FC#0, port C2

Entries	74
Mean	21.61
Std Dev	12.92

Gaus mean : 29.4908

Gaus Width: 3.0633

Entry



B1L103S, U7-ch50, adc1

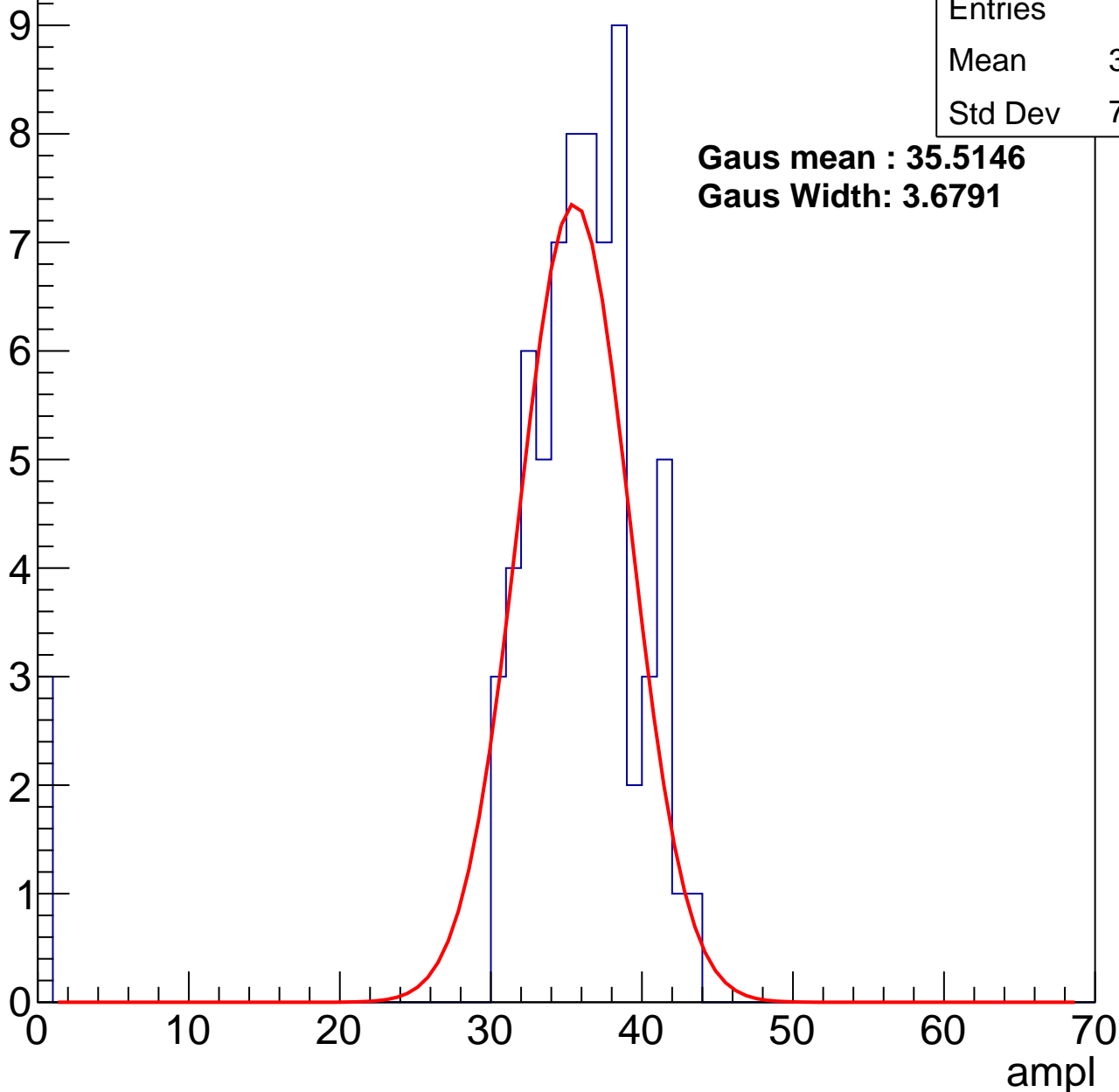
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	34.25
Std Dev	7.792

Gaus mean : 35.5146

Gaus Width: 3.6791



B1L103S, U7-ch50, adc2

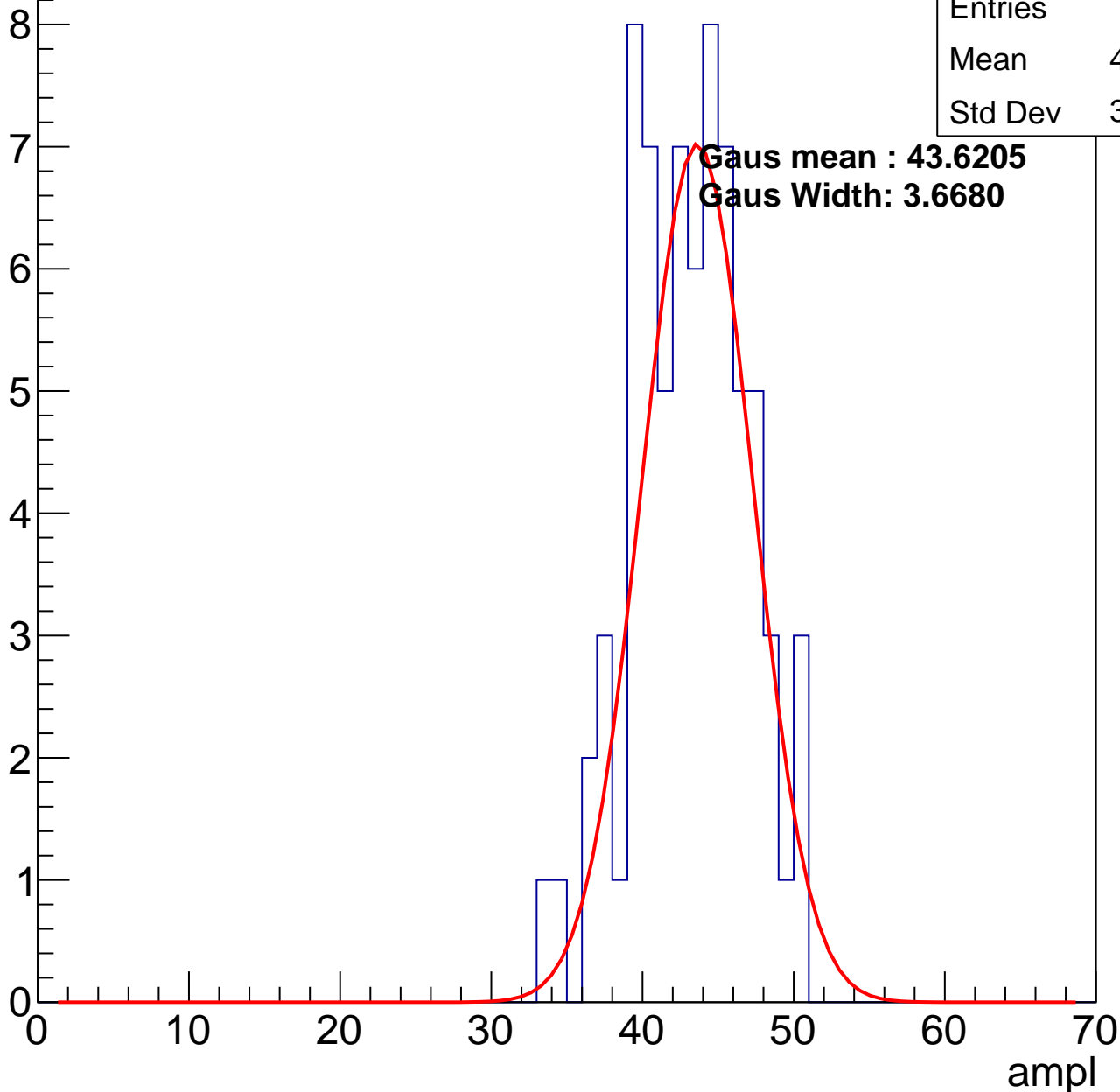
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	42.63
Std Dev	3.773

Gaus mean : 43.6205

Gaus Width: 3.6680

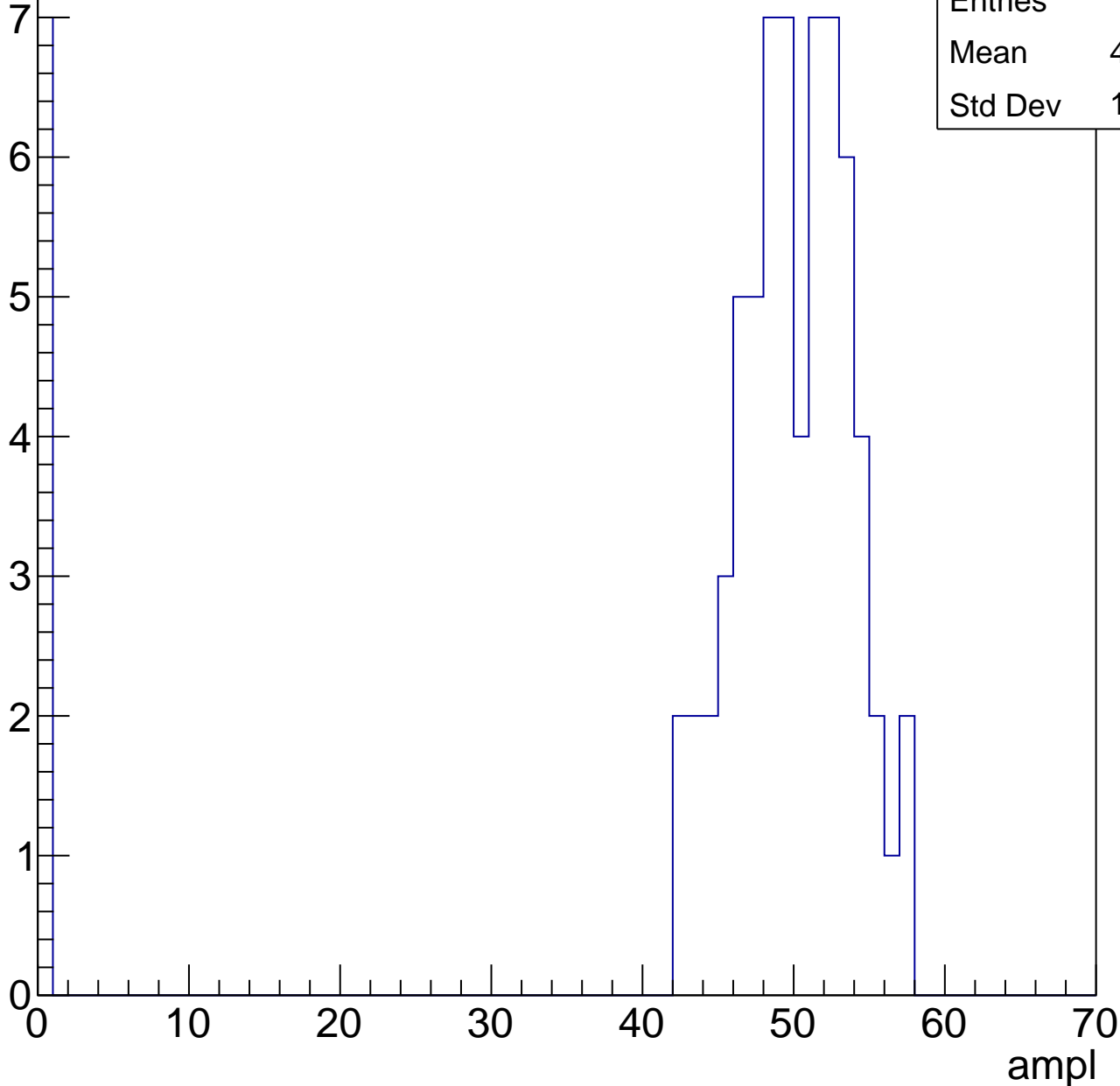


B1L103S, U7-ch50, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	44.82
Std Dev	14.99

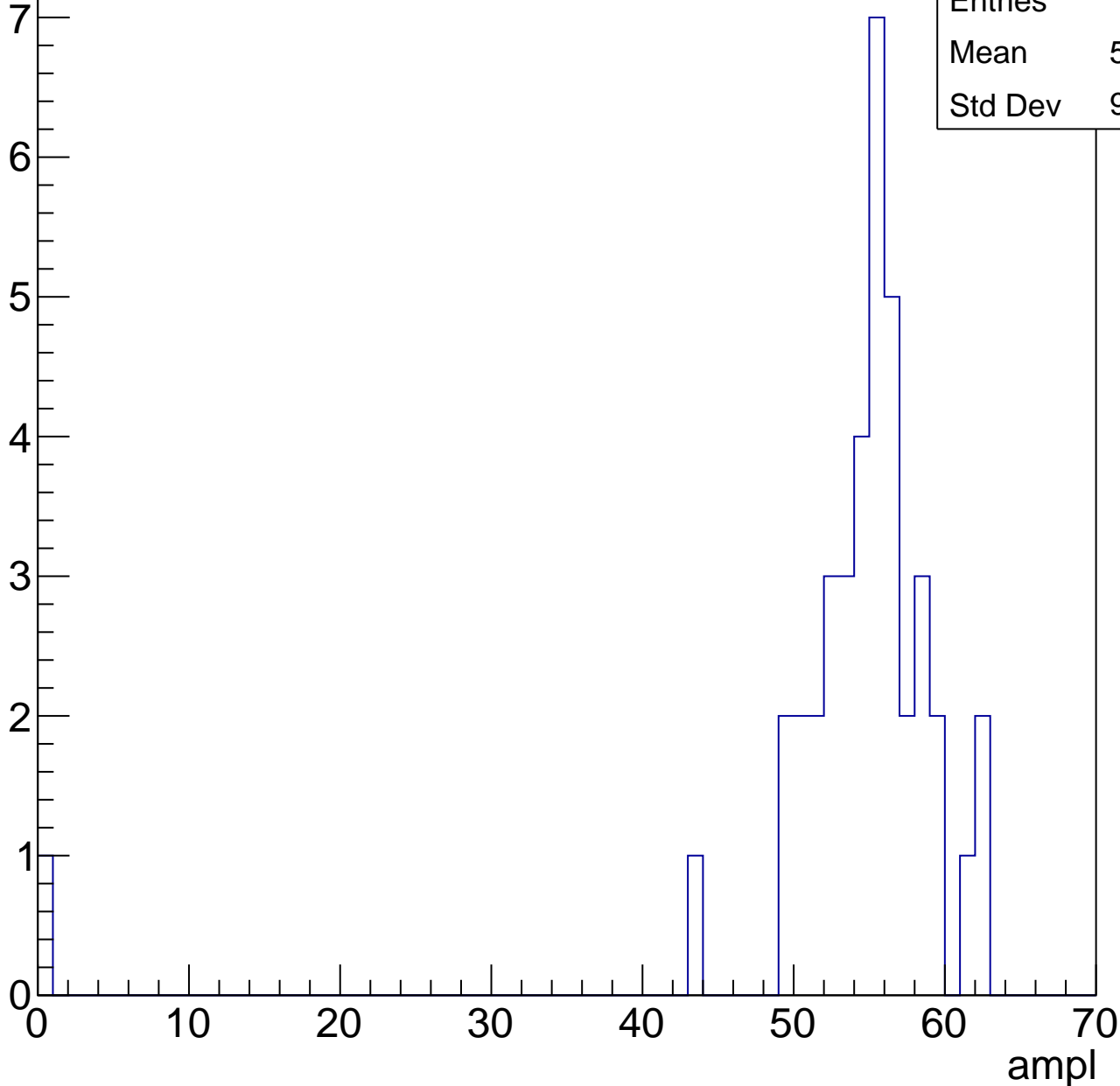


B1L103S, U7-ch50, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	53.25
Std Dev	9.286



B1L103S, U7-ch50, adc5

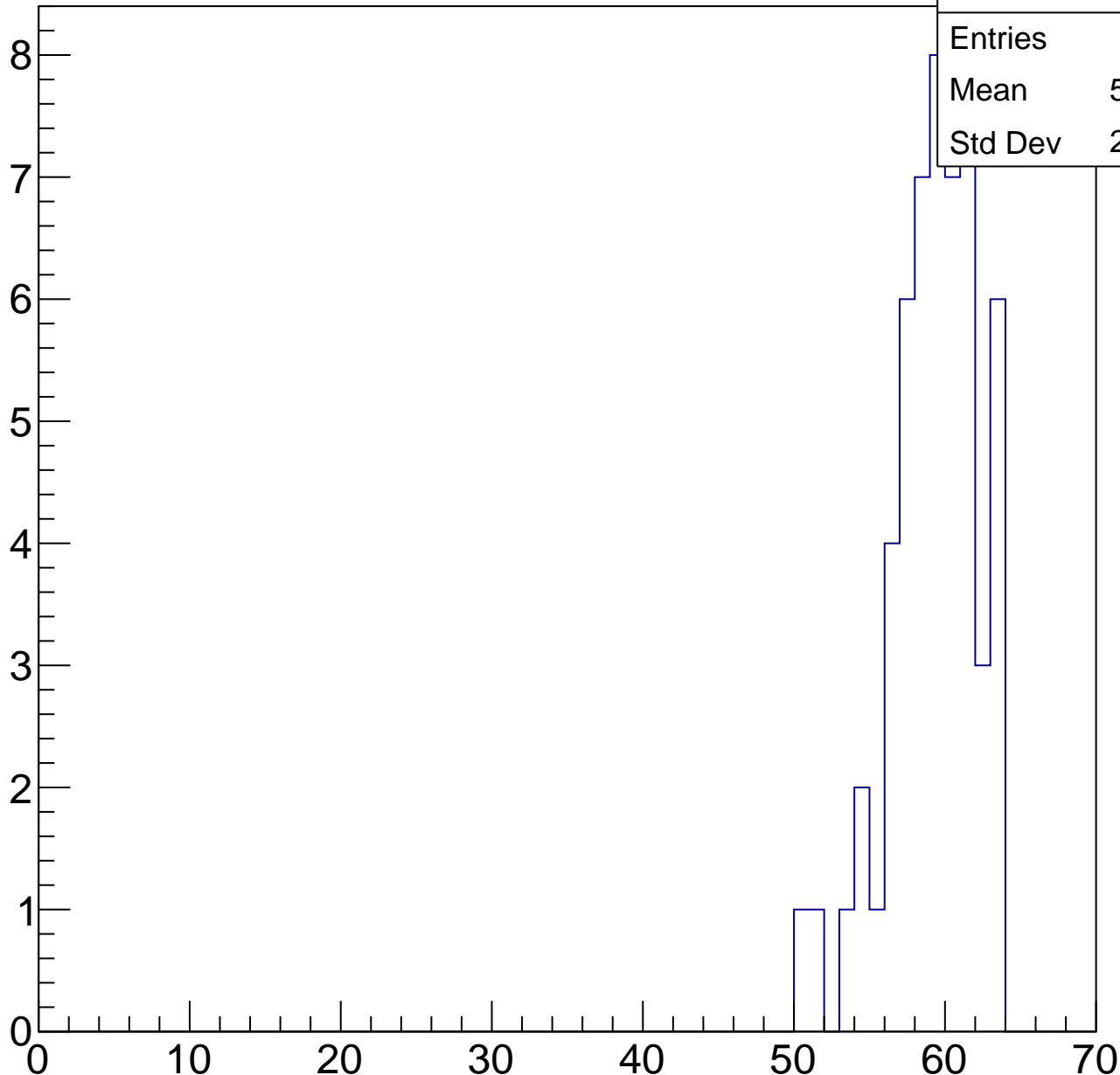
calib_packv5_041523_1651.root, FC#0, port C2

Entry

8
7
6
5
4
3
2
1
0

Entries	55
Mean	58.78
Std Dev	2.934

ampl

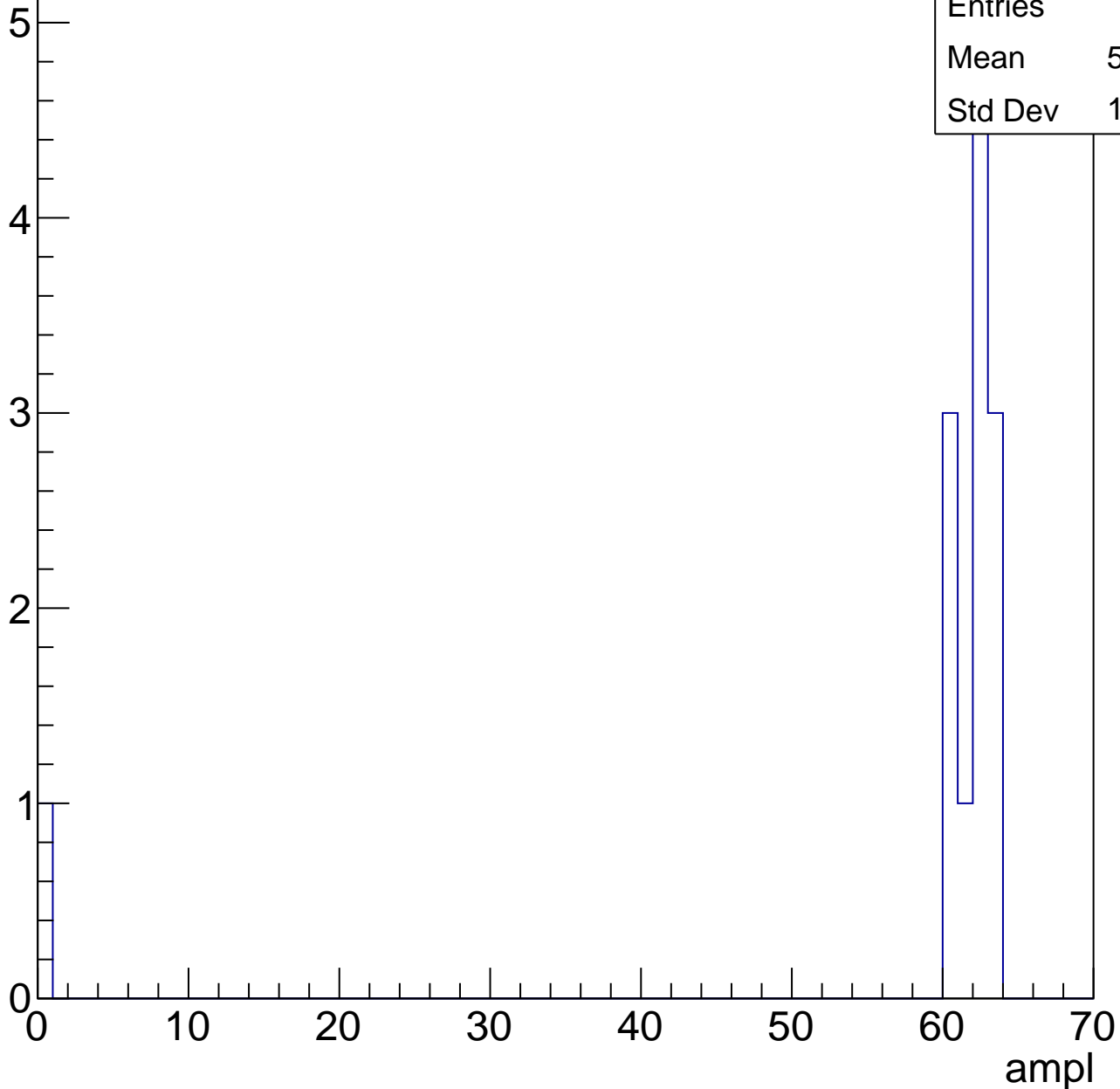


B1L103S, U7-ch50, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

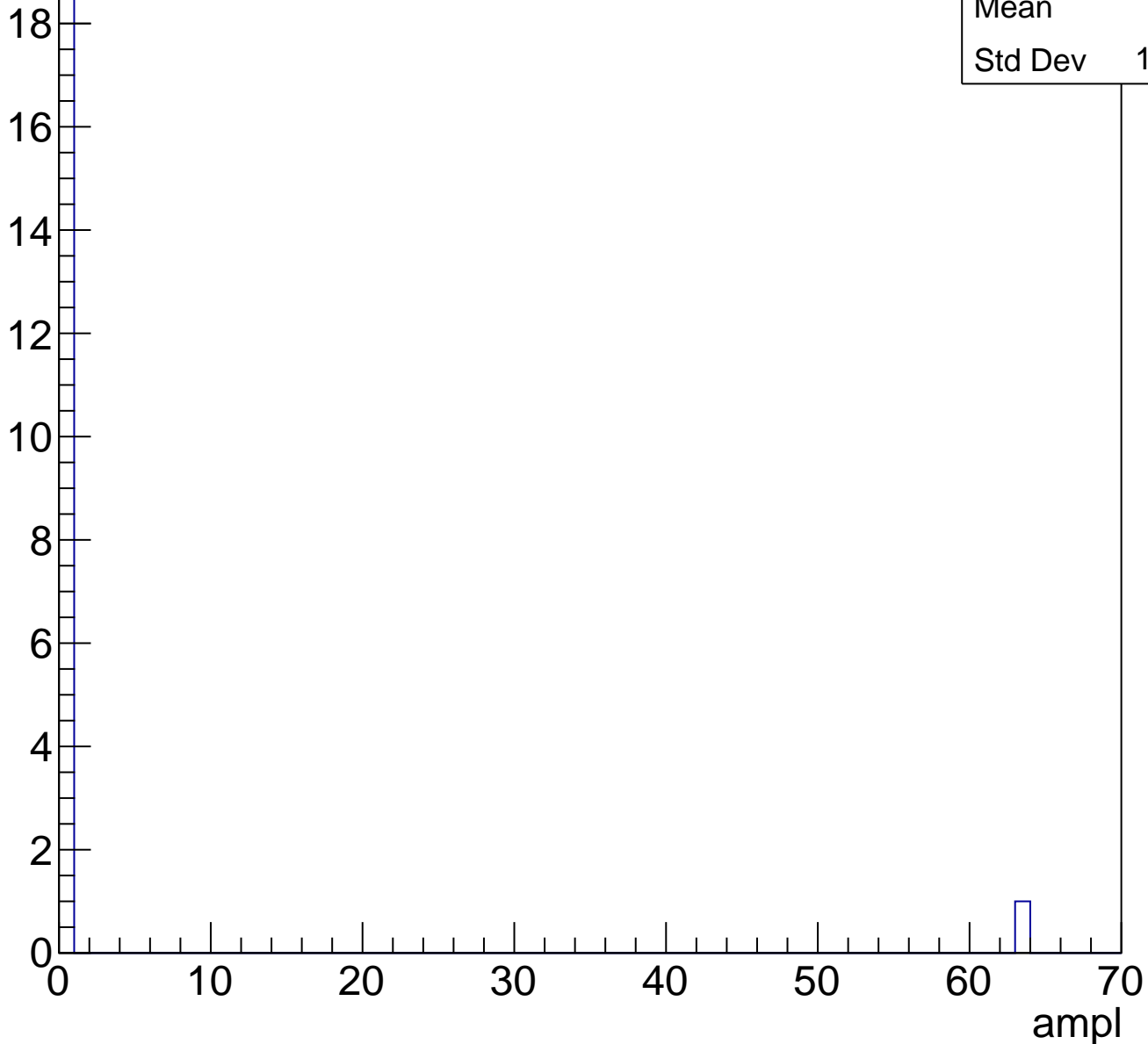
Entries	13
Mean	56.92
Std Dev	16.47



B1L103S, U7-ch50, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	20
Mean	3.15
Std Dev	13.73

B1L103S, U7-ch51, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	69
Mean	26.7
Std Dev	8.829

Gaus mean : 30.6504

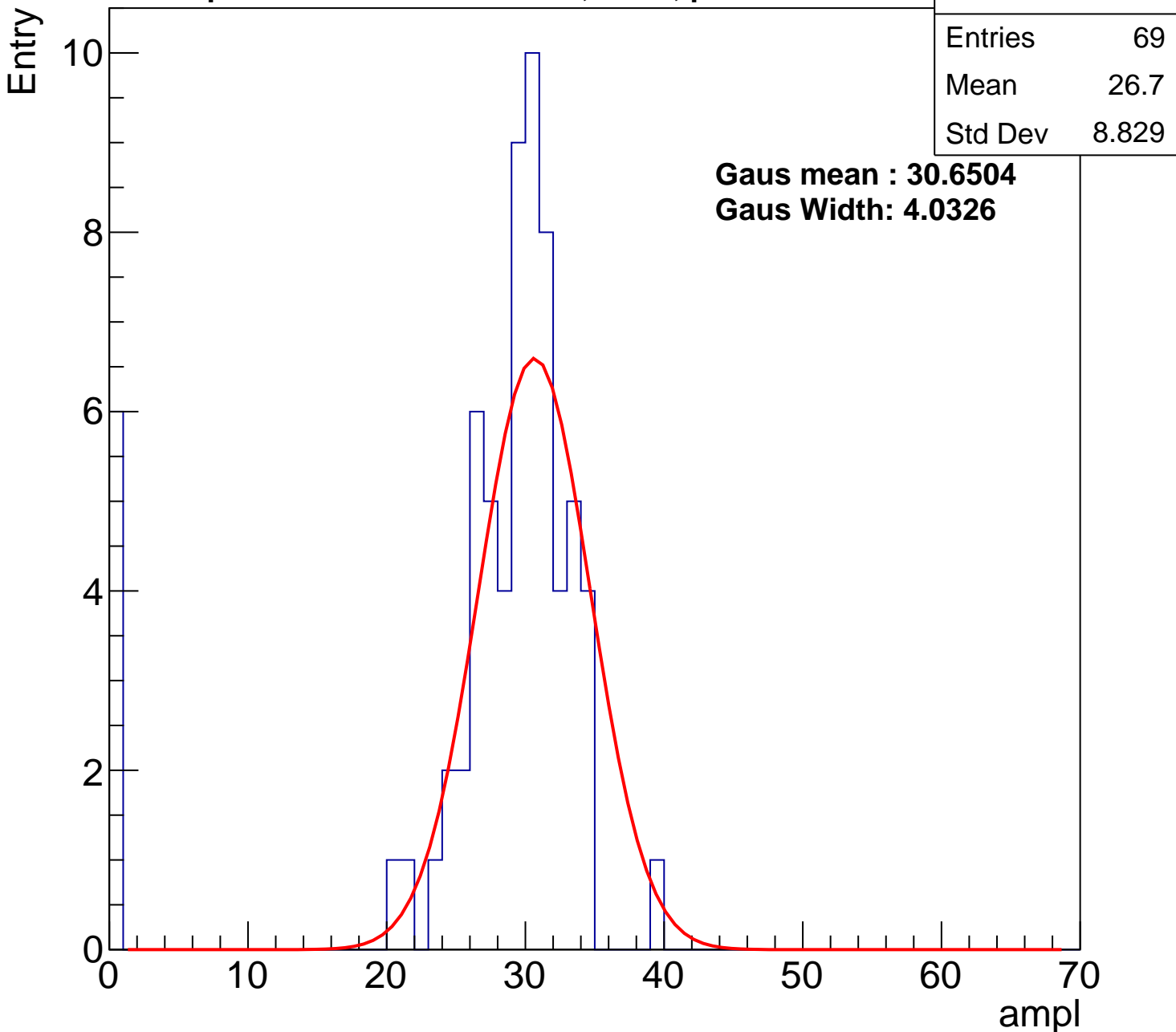
Gaus Width: 4.0326

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl



B1L103S, U7-ch51, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	84
Mean	35.17
Std Dev	8.552

Gaus mean : 36.9090

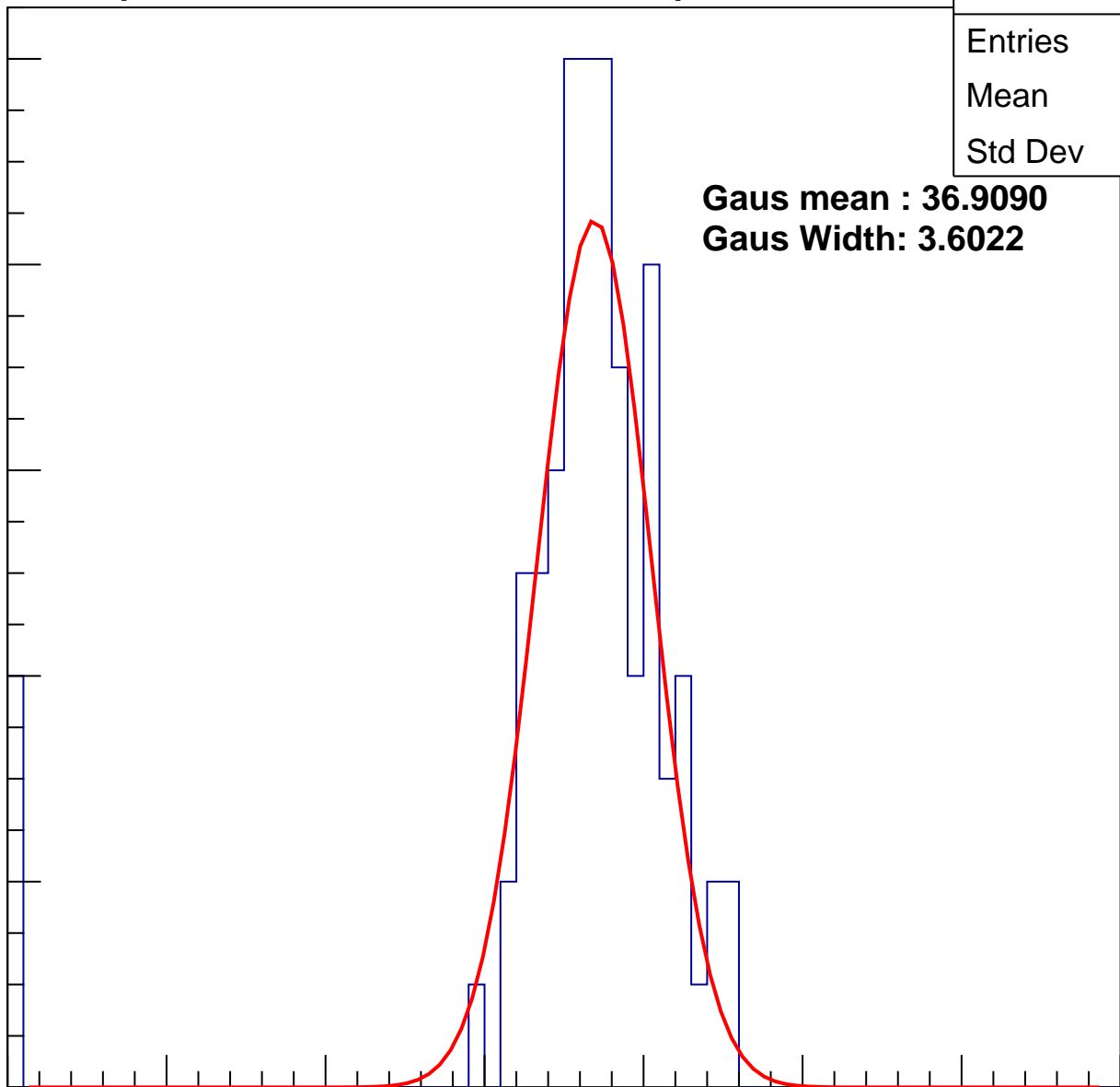
Gaus Width: 3.6022

Entry

10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U7-ch51, adc2

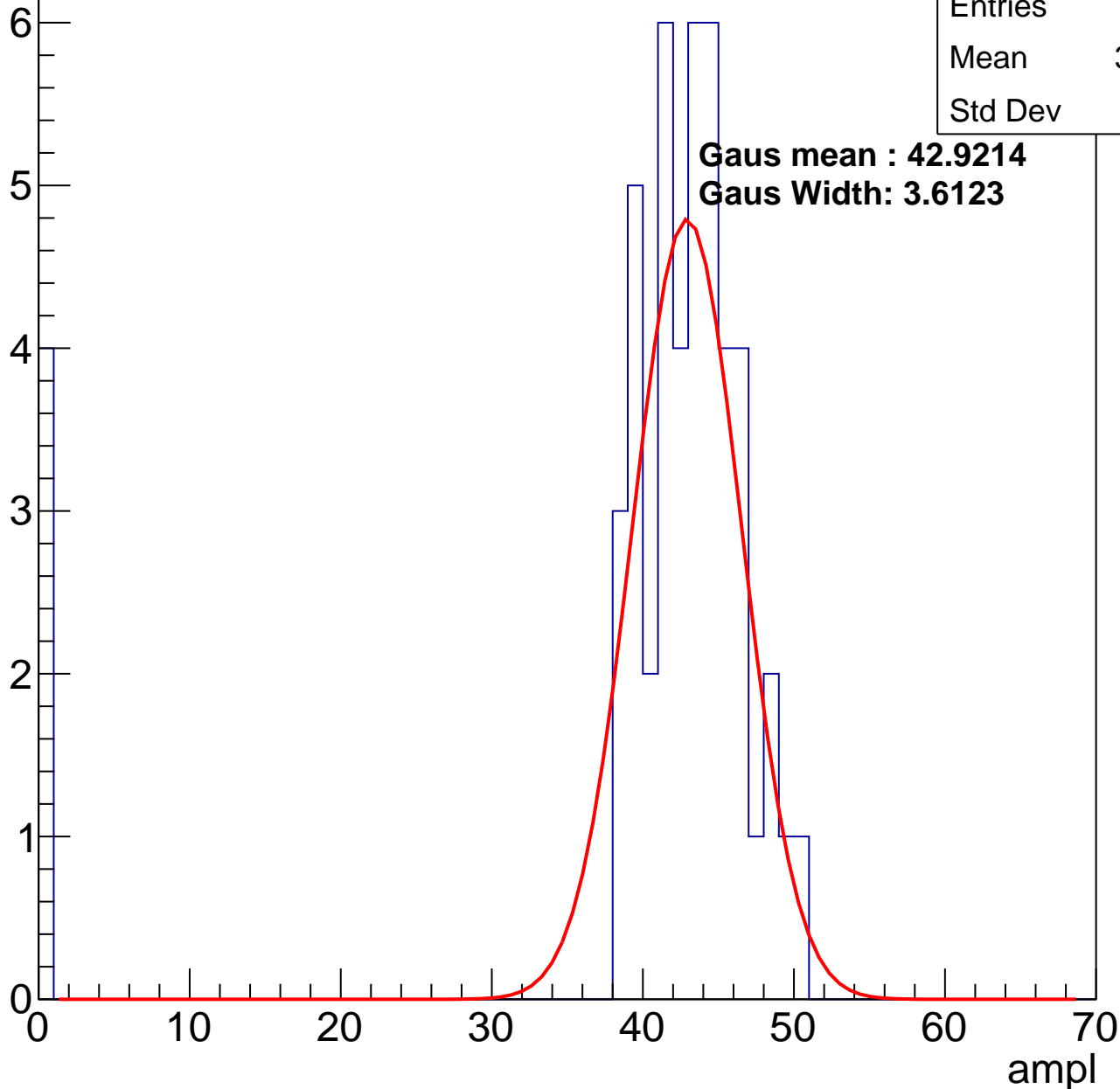
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	39.41
Std Dev	12.1

Gaus mean : 42.9214

Gaus Width: 3.6123

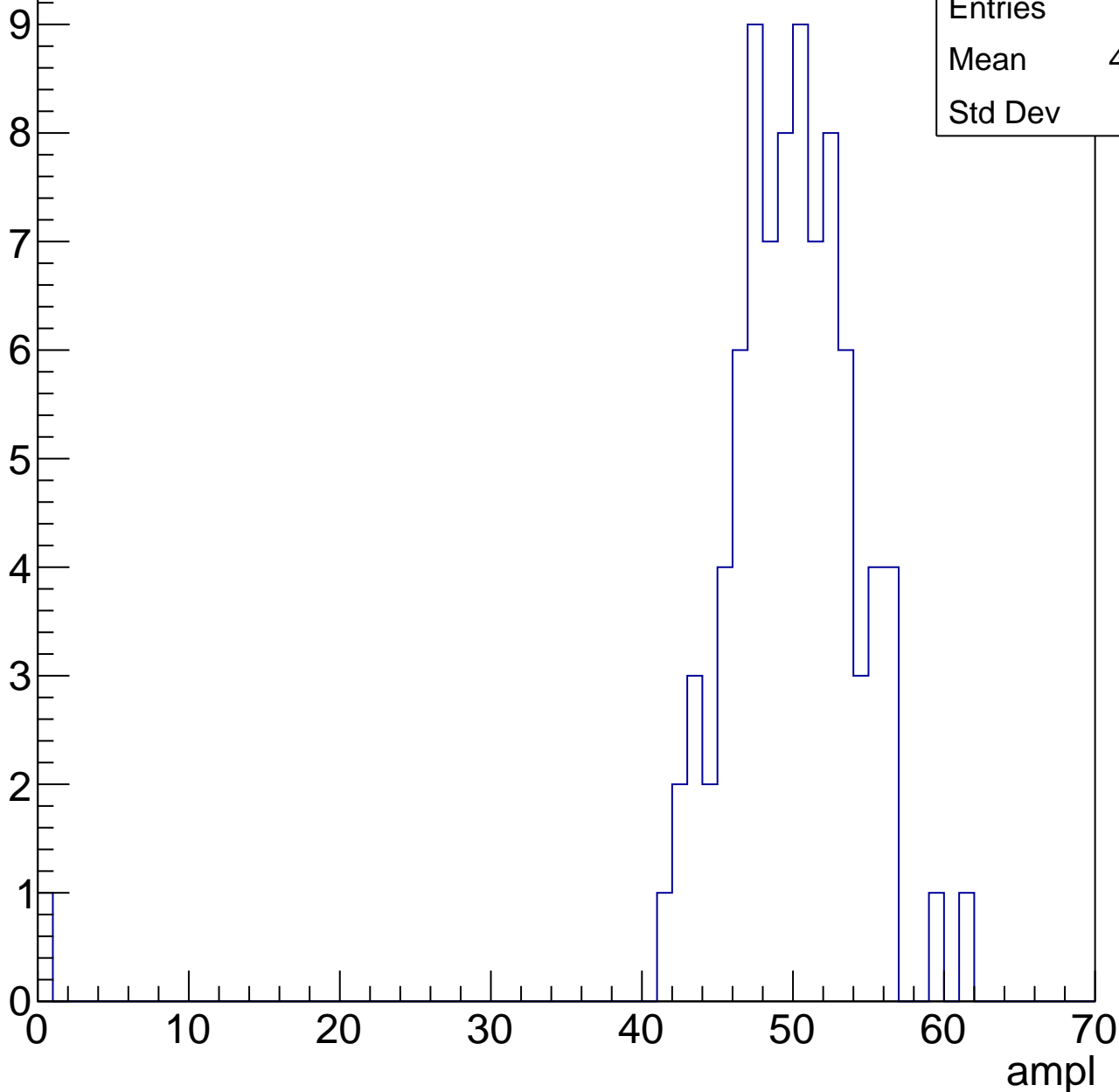


B1L103S, U7-ch51, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	86
Mean	49.02
Std Dev	6.6

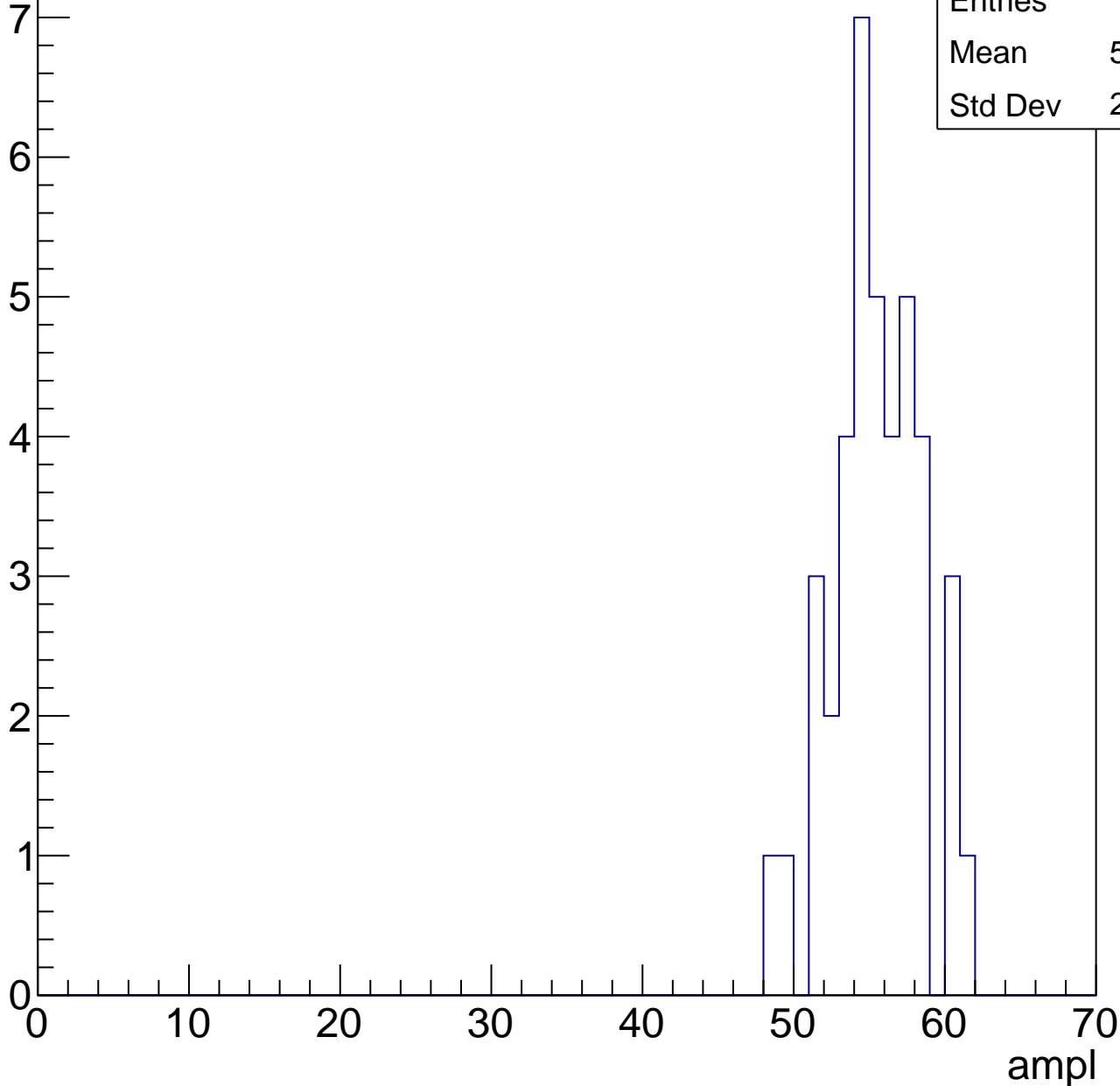


B1L103S, U7-ch51, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	55.02
Std Dev	2.937



B1L103S, U7-ch51, adc5

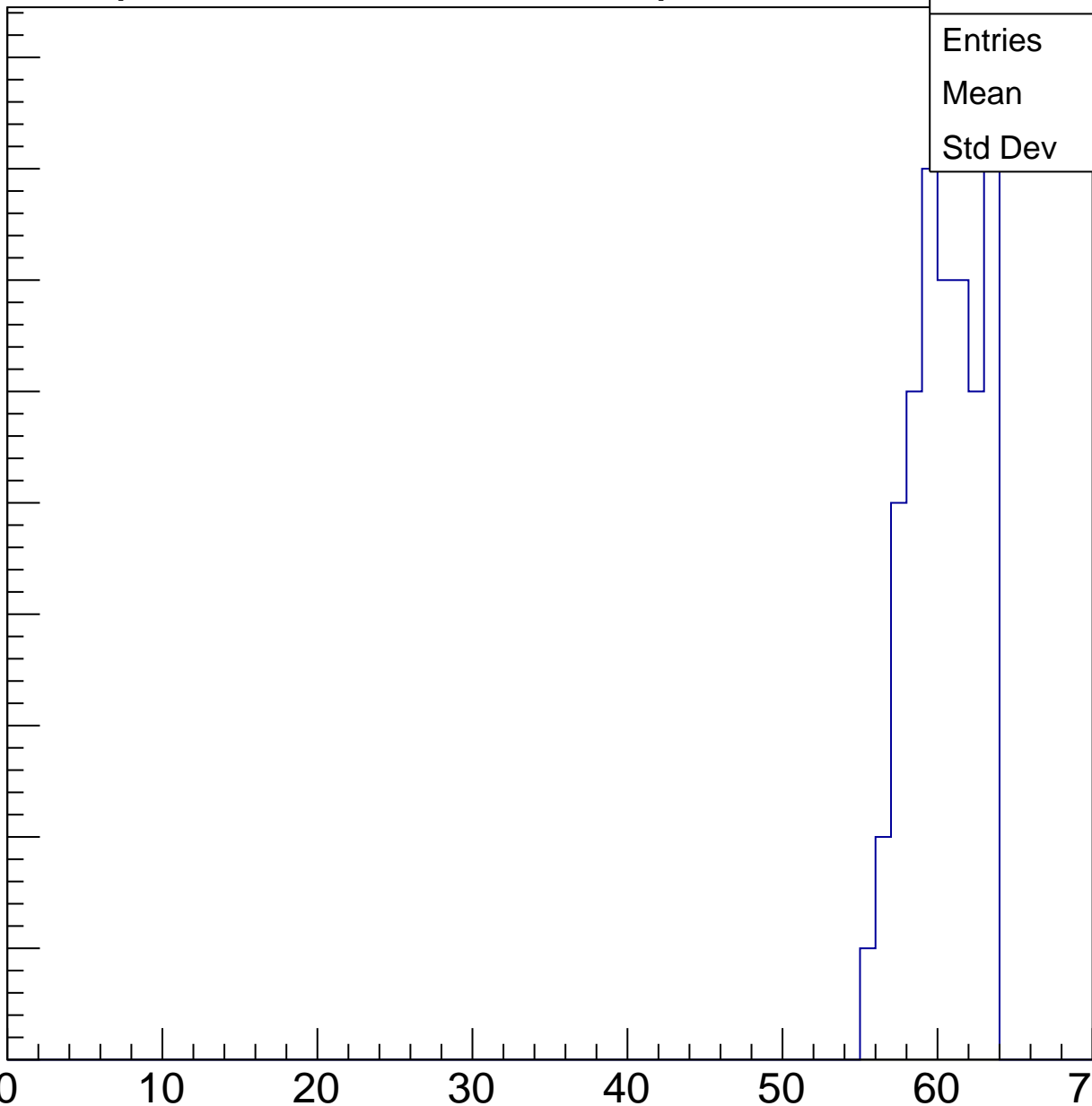
calib_packv5_041523_1651.root, FC#0, port C2

Entry

9
8
7
6
5
4
3
2
1
0

Entries	51
Mean	59.96
Std Dev	2.196

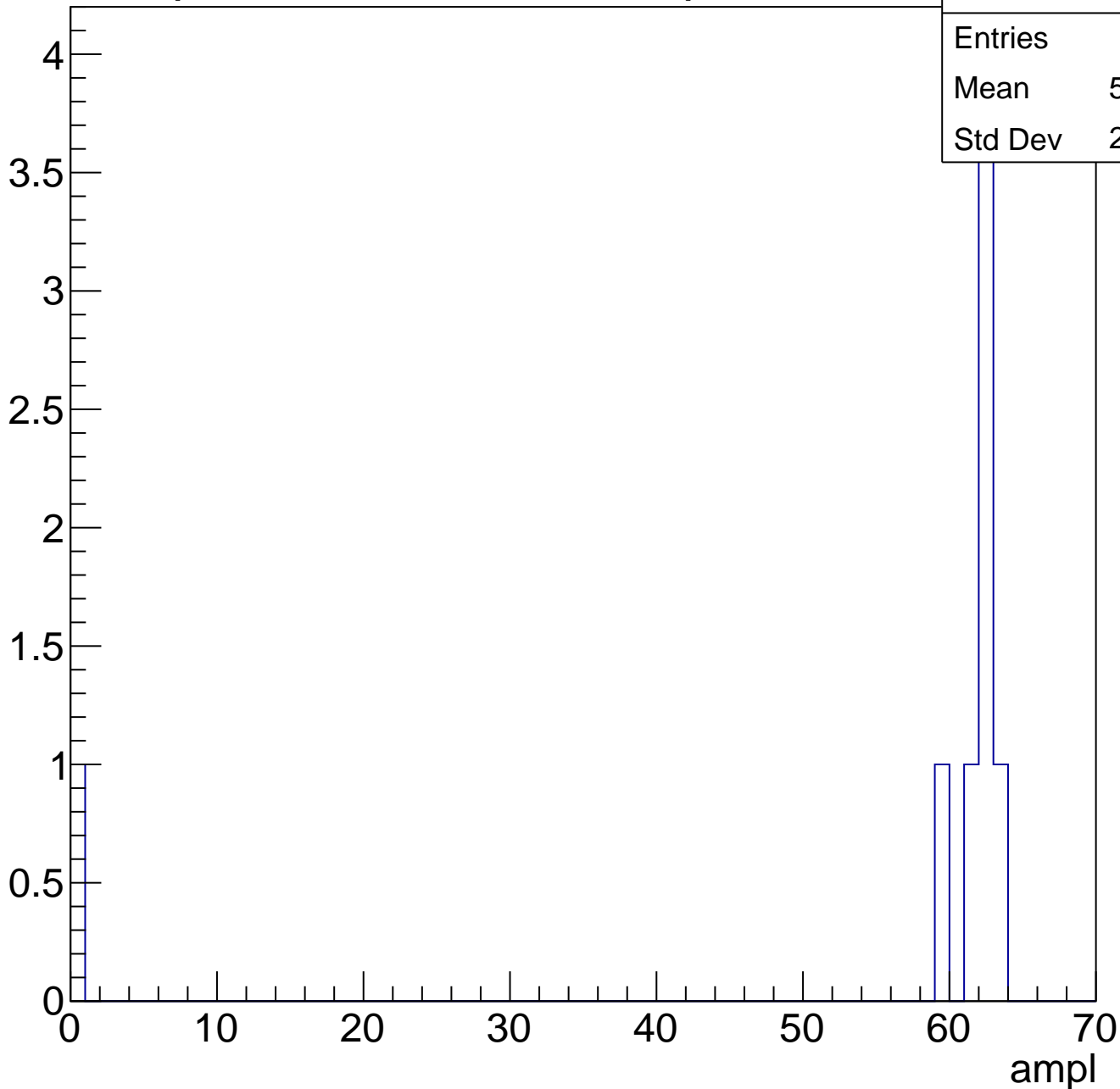
ampl



B1L103S, U7-ch51, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch51, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch52, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	95
Mean	18.18
Std Dev	11.79

Gaus mean : 25.3755

Gaus Width: 3.2569

Entry

25

20

15

10

5

0

0

10

20

30

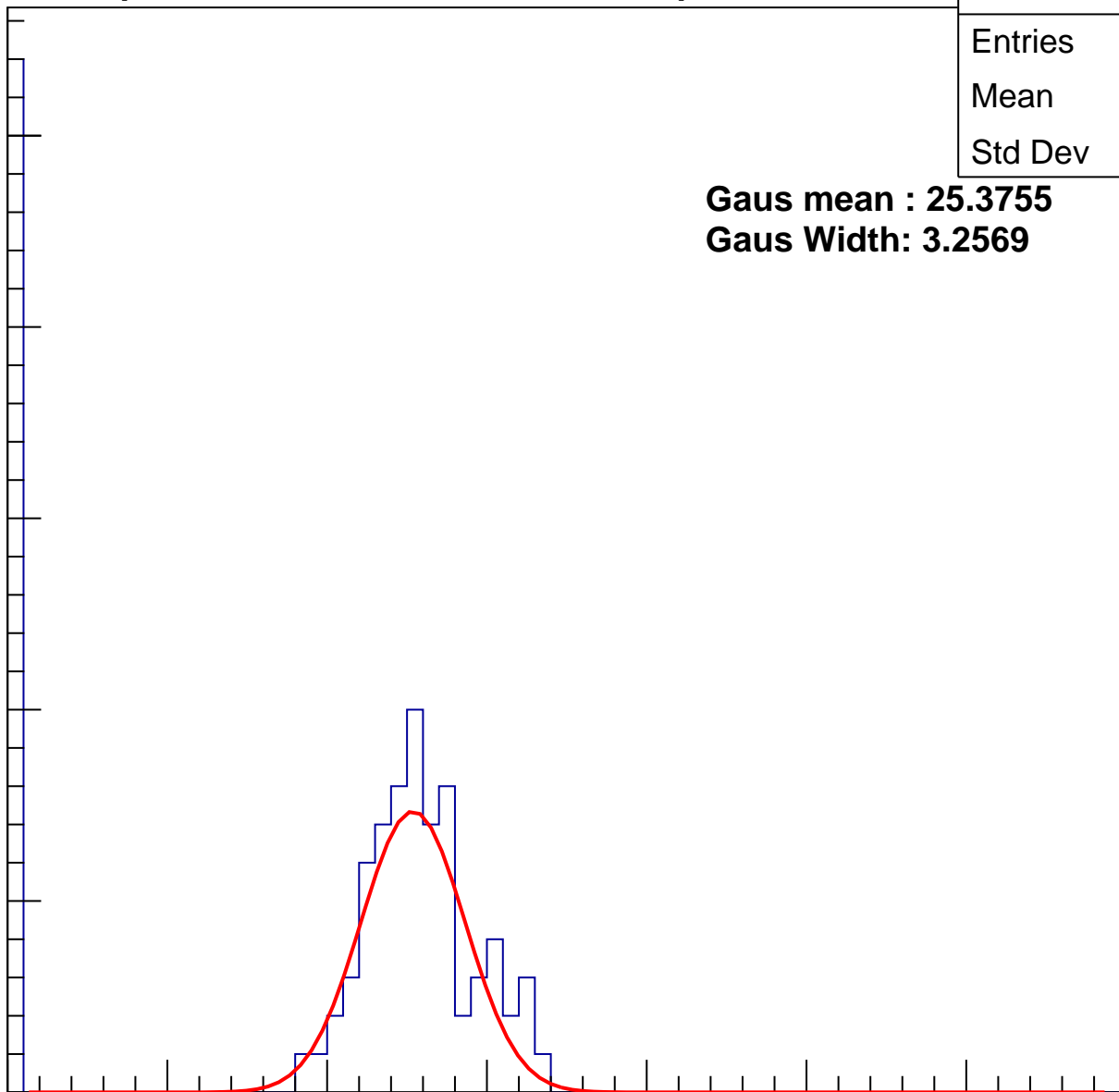
40

50

60

70

ampl



B1L103S, U7-ch52, adc1

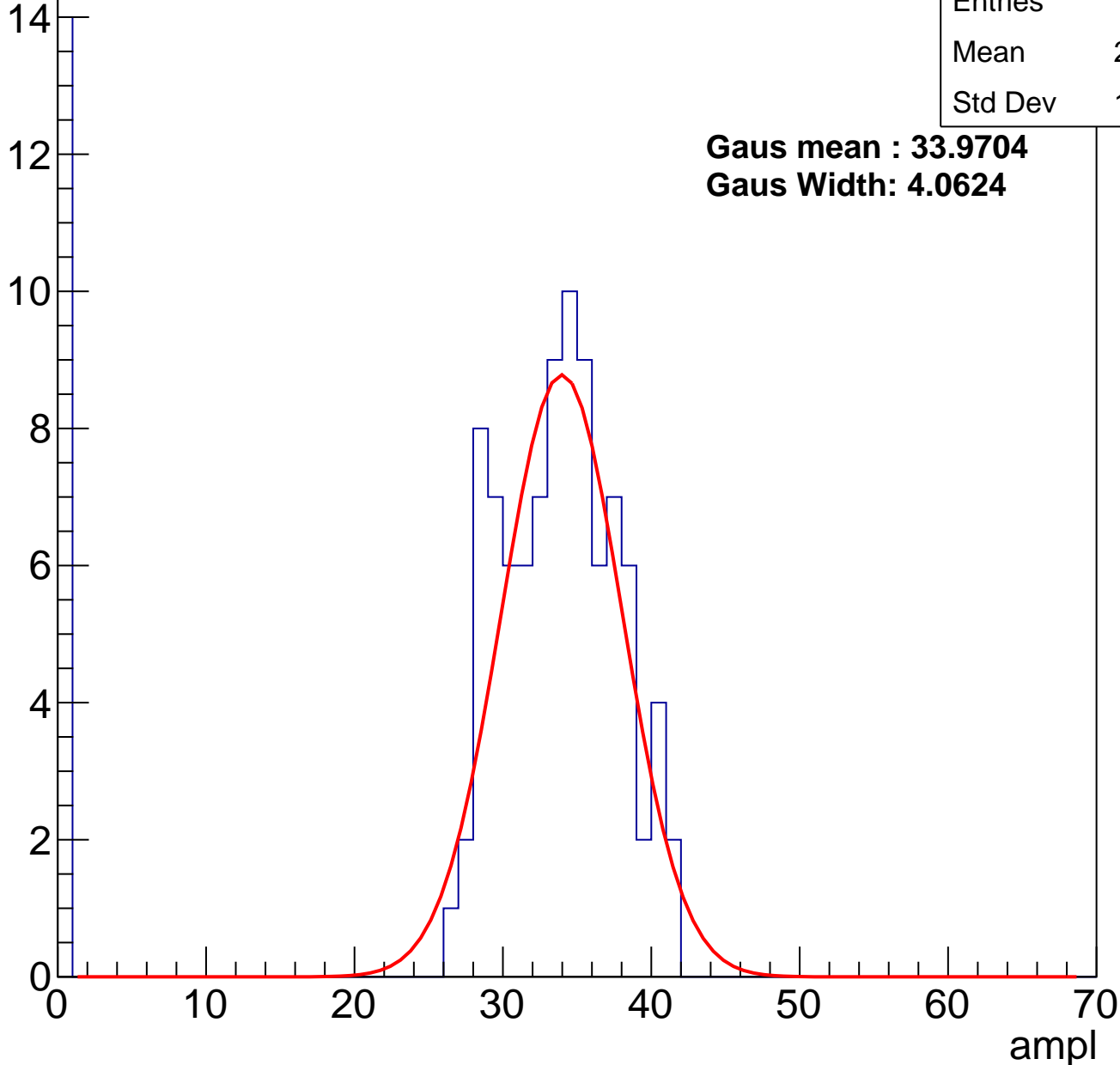
calib_packv5_041523_1651.root, FC#0, port C2

Entries	106
Mean	28.98
Std Dev	11.82

Gaus mean : 33.9704

Gaus Width: 4.0624

Entry



B1L103S, U7-ch52, adc2

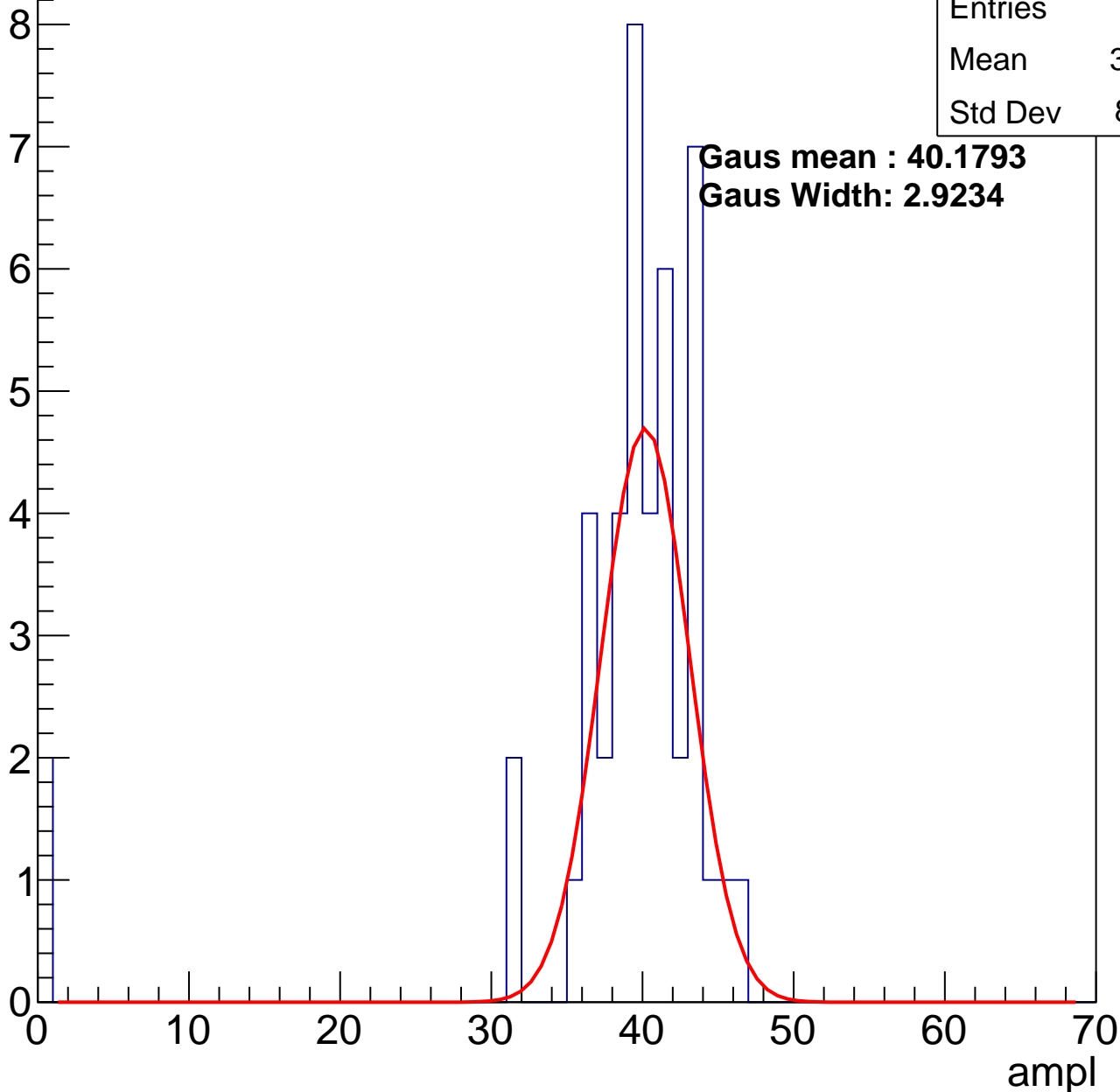
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	45
Mean	37.89
Std Dev	8.751

Gaus mean : 40.1793

Gaus Width: 2.9234

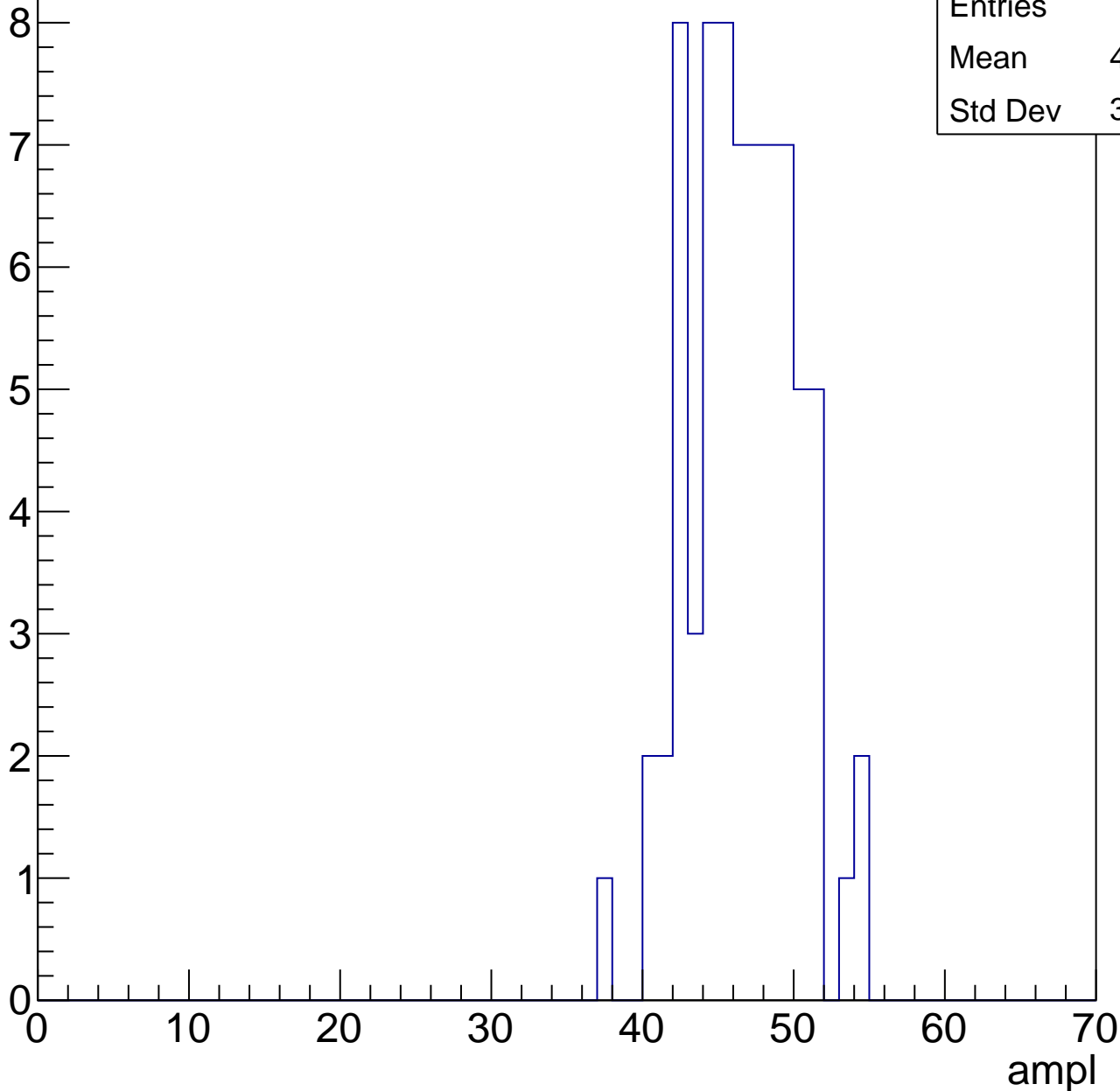


B1L103S, U7-ch52, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	46.19
Std Dev	3.463

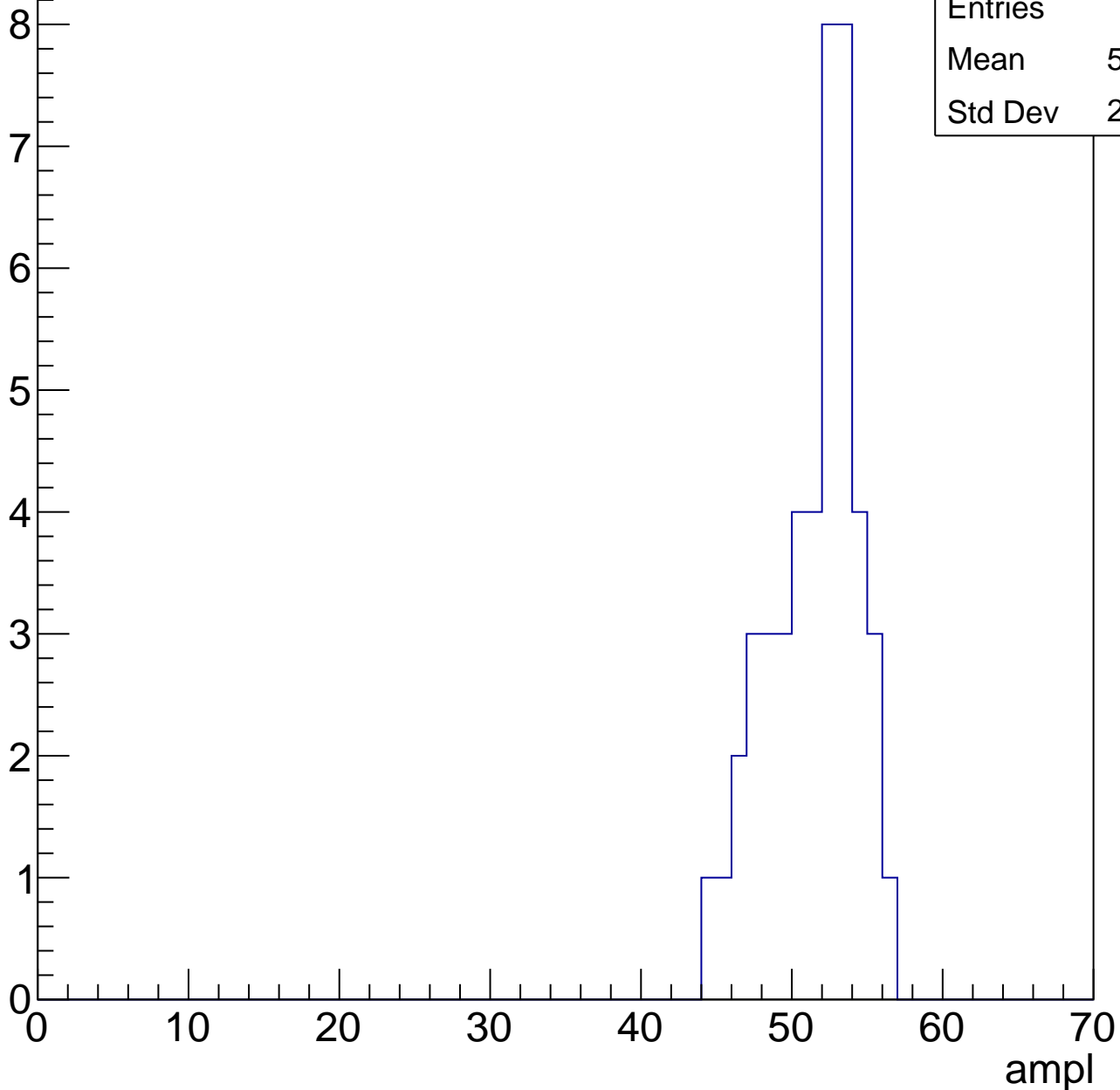


B1L103S, U7-ch52, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	45
Mean	50.98
Std Dev	2.887

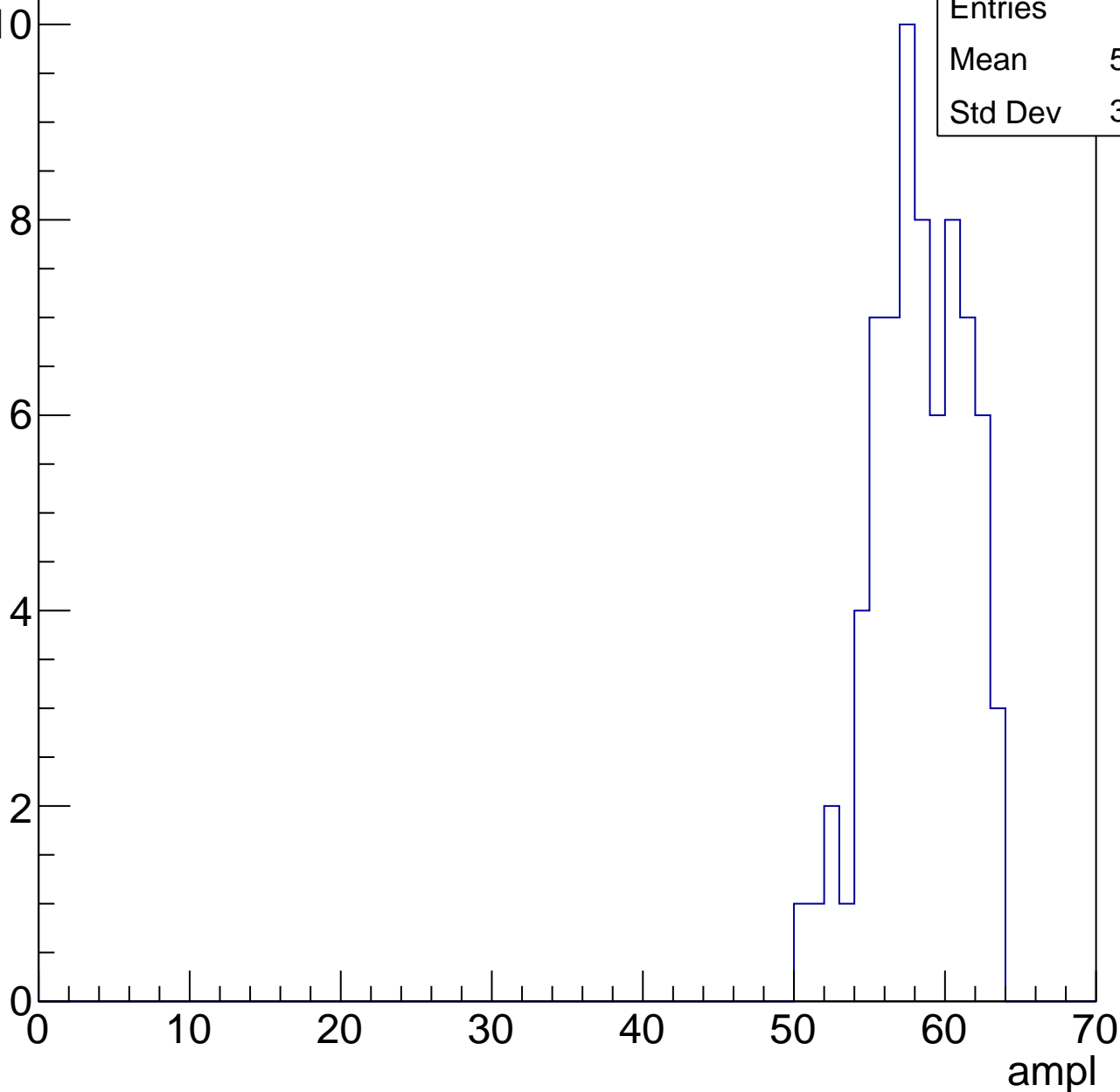


B1L103S, U7-ch52, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	57.85
Std Dev	3.015

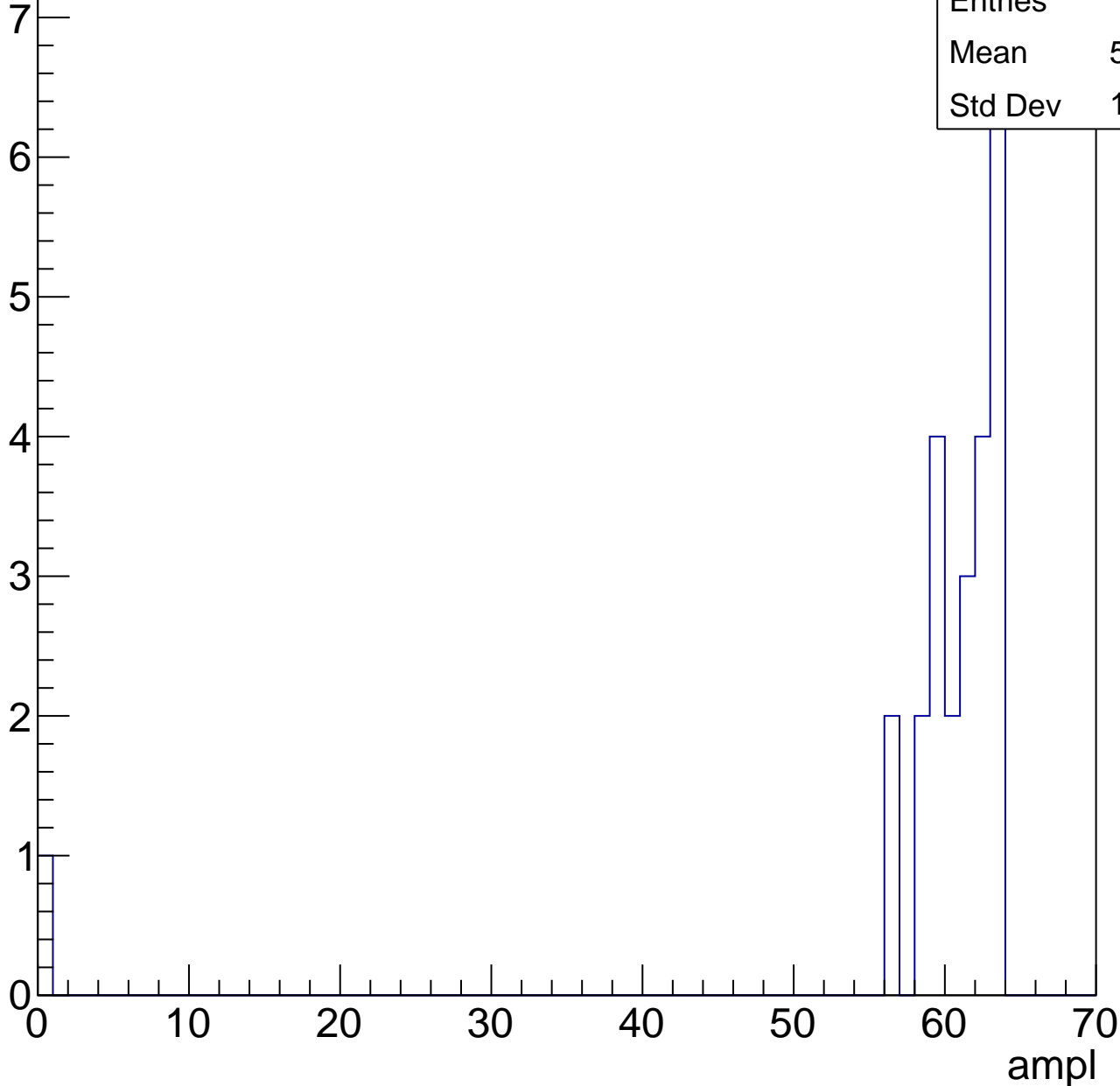


B1L103S, U7-ch52, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	25
Mean	58.24
Std Dev	12.08



B1L103S, U7-ch52, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U7-ch53, adc0

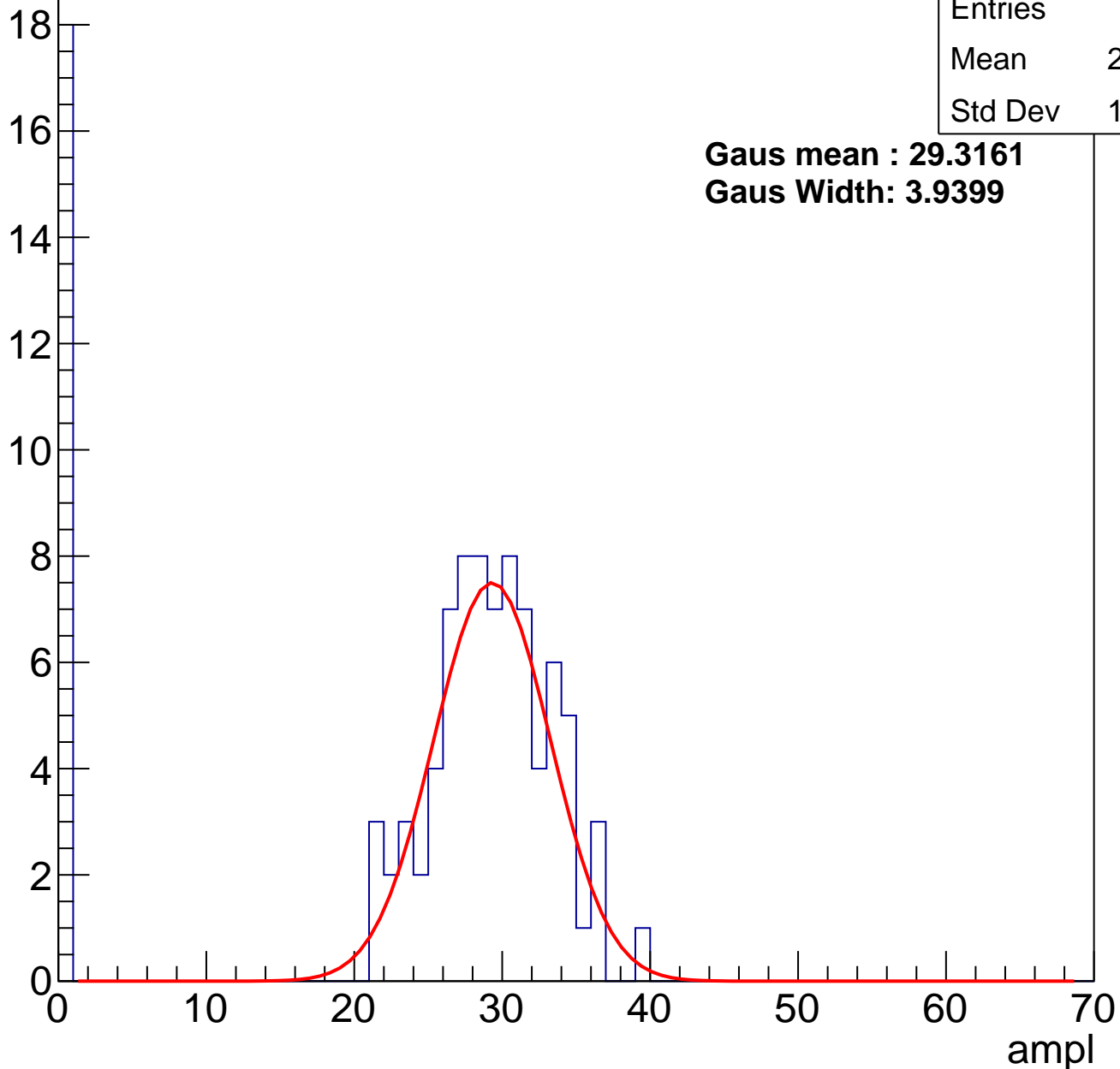
calib_packv5_041523_1651.root, FC#0, port C2

Entries	97
Mean	23.55
Std Dev	11.77

Gaus mean : 29.3161

Gaus Width: 3.9399

Entry



B1L103S, U7-ch53, adc1

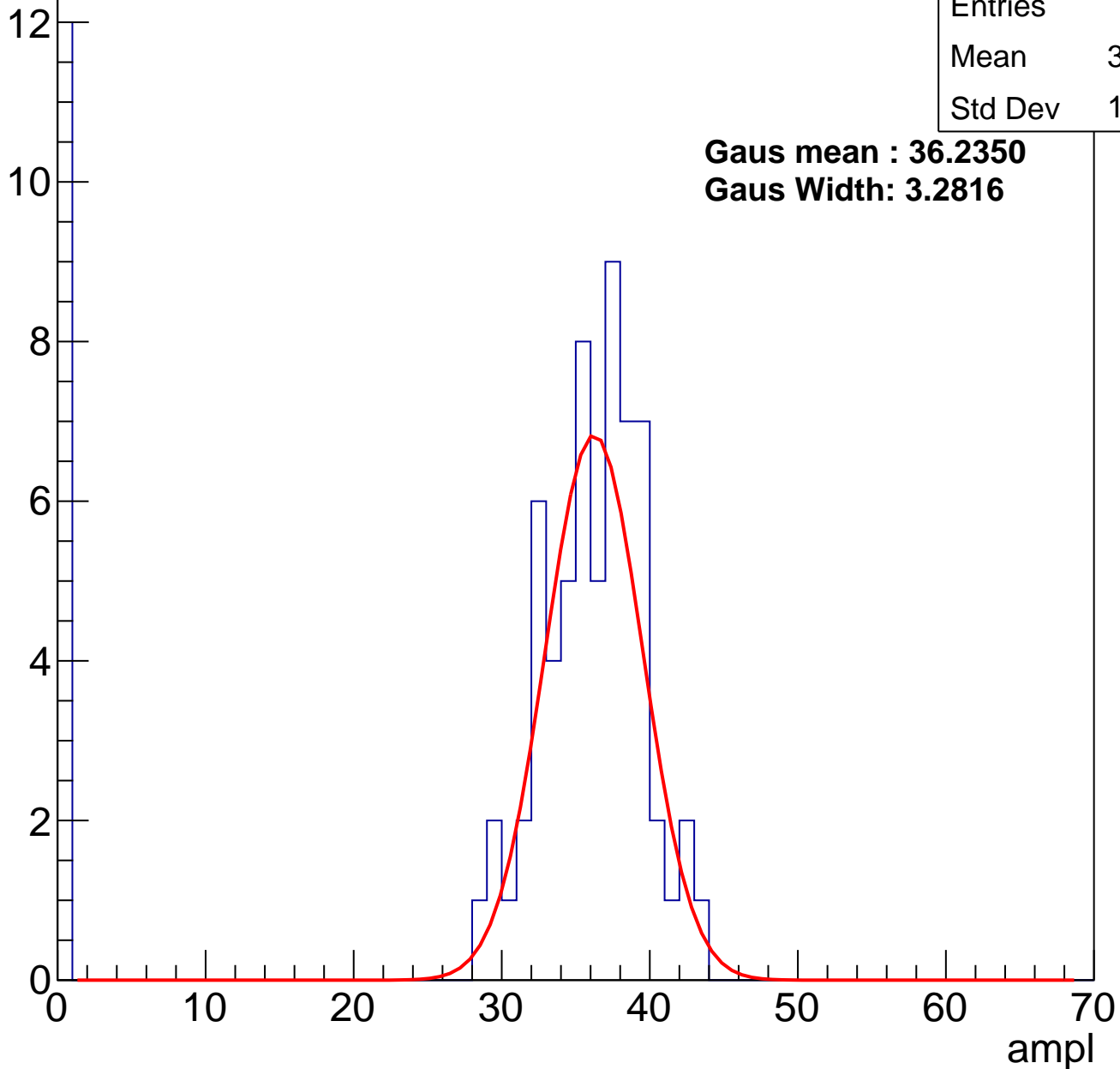
calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	30.03
Std Dev	13.45

Gaus mean : 36.2350

Gaus Width: 3.2816

Entry



B1L103S, U7-ch53, adc2

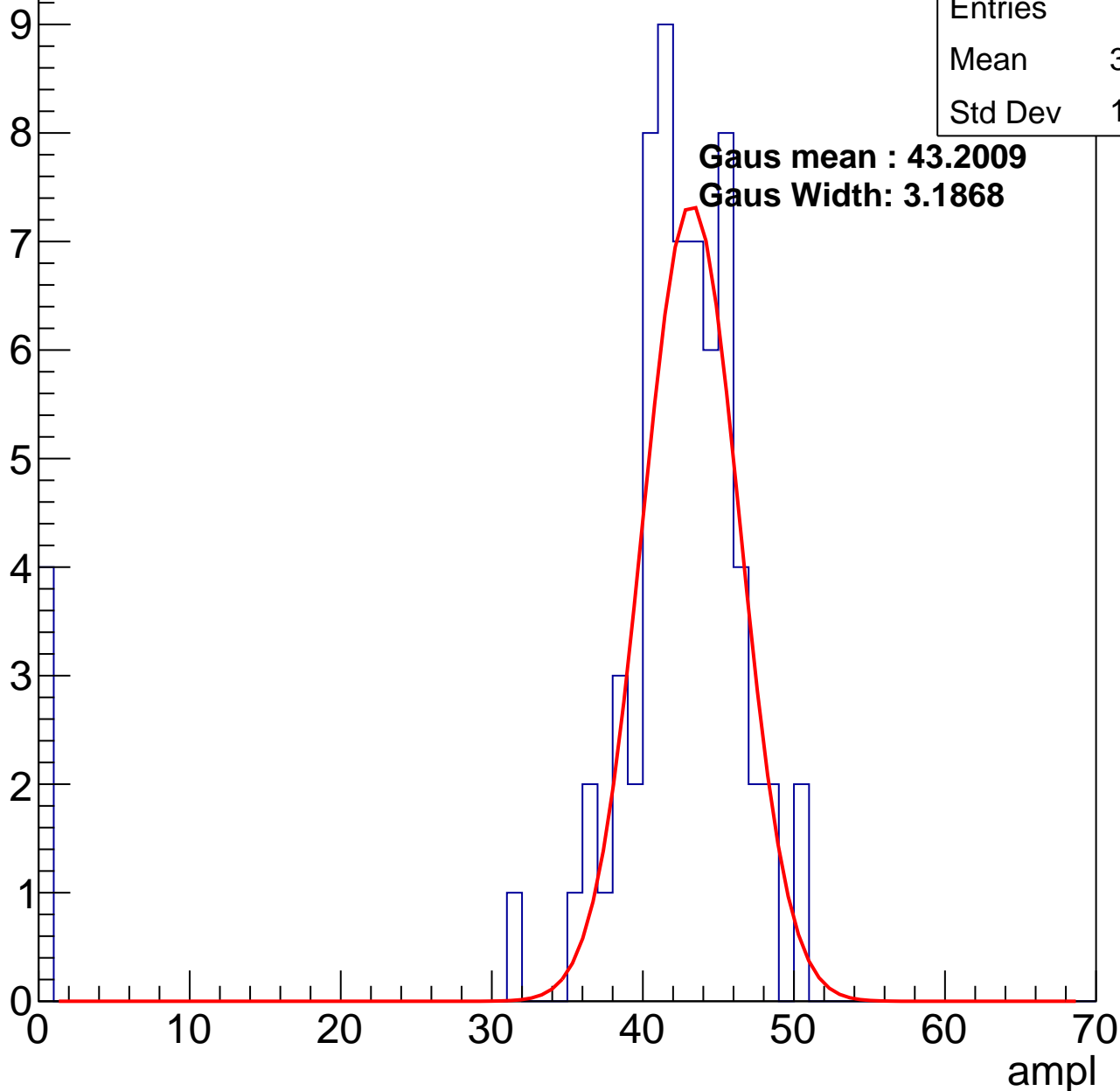
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	39.84
Std Dev	10.44

Gaus mean : 43.2009

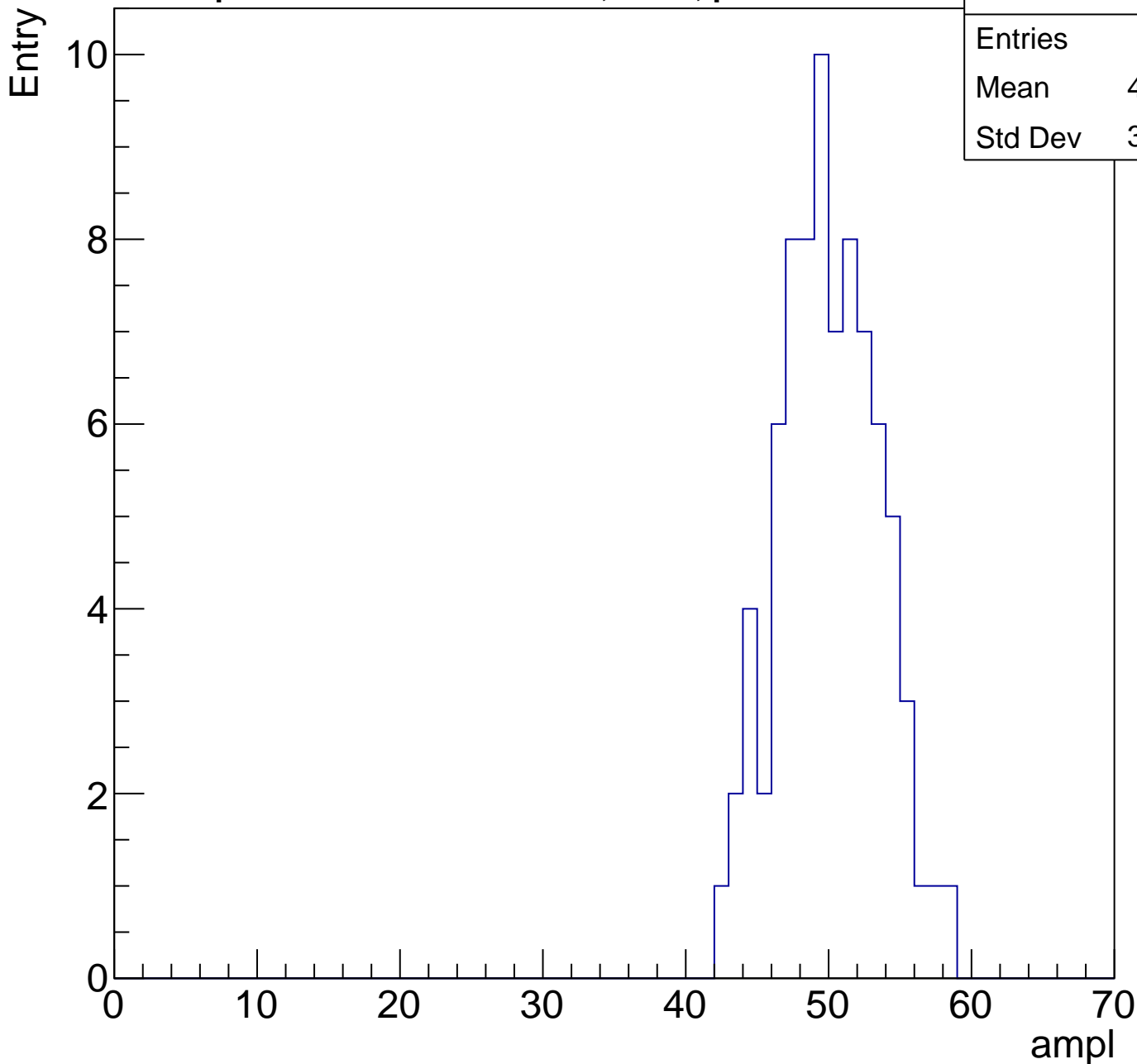
Gaus Width: 3.1868



B1L103S, U7-ch53, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	49.58
Std Dev	3.438

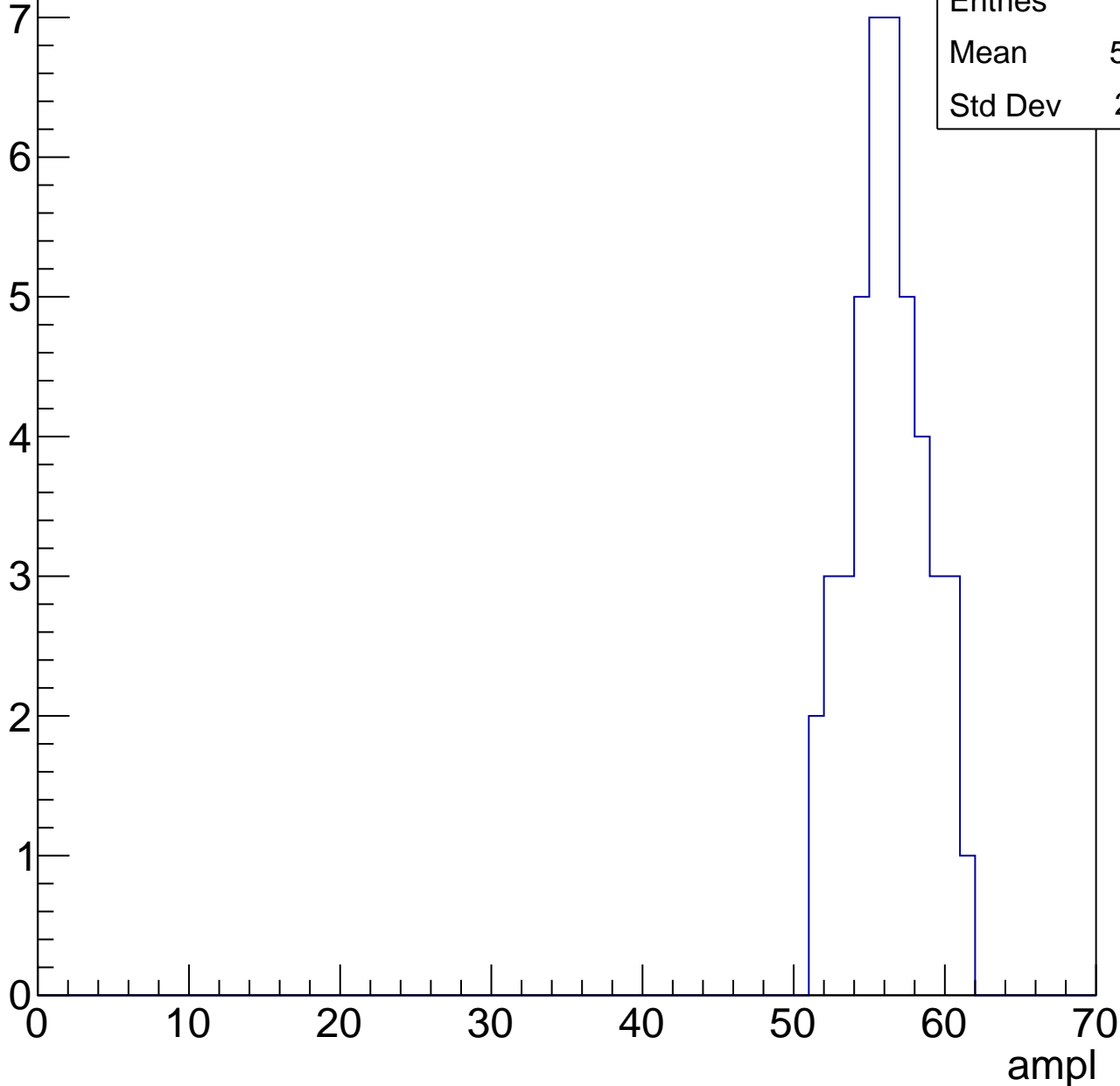


B1L103S, U7-ch53, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	43
Mean	55.79
Std Dev	2.511

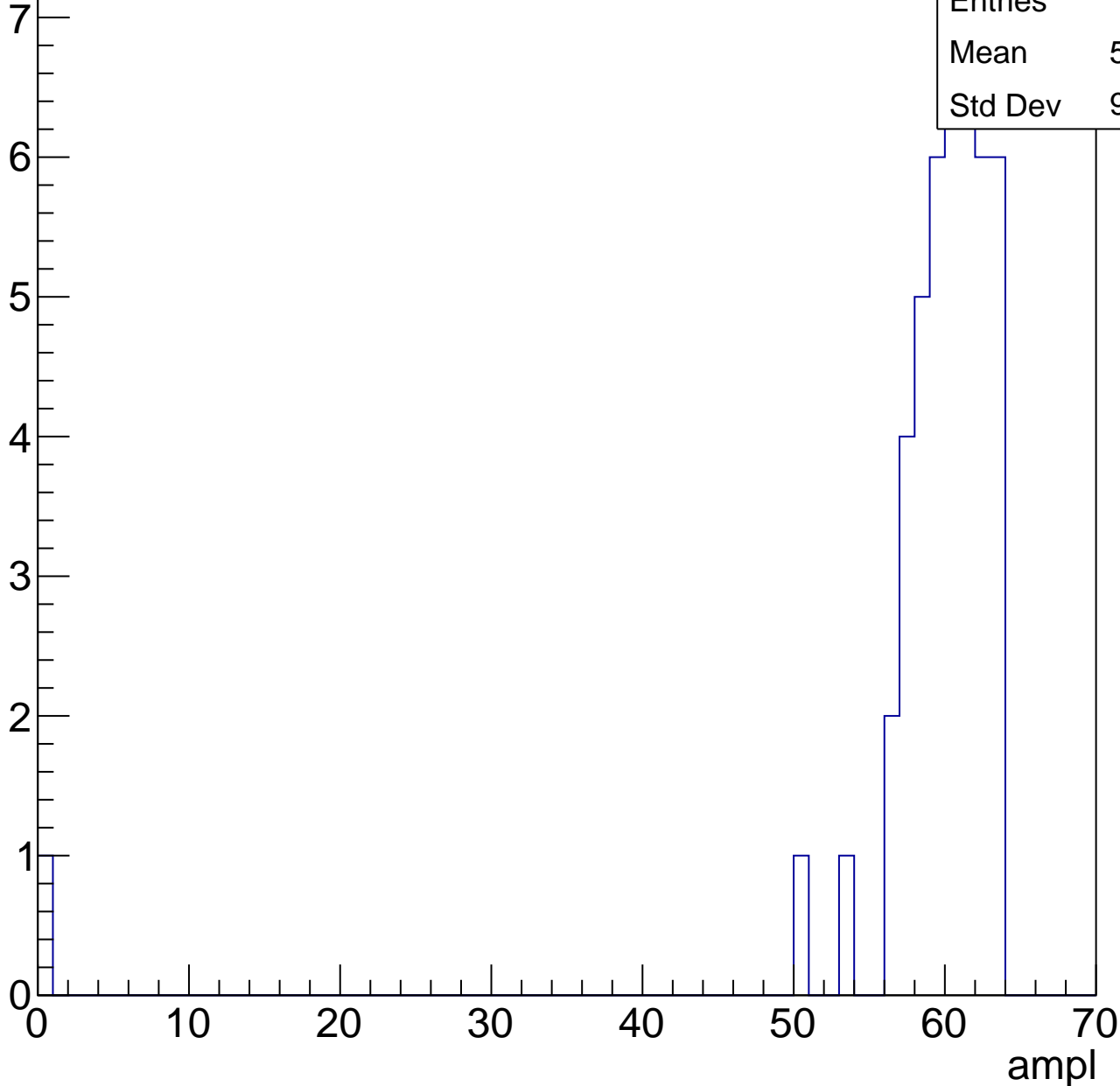


B1L103S, U7-ch53, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

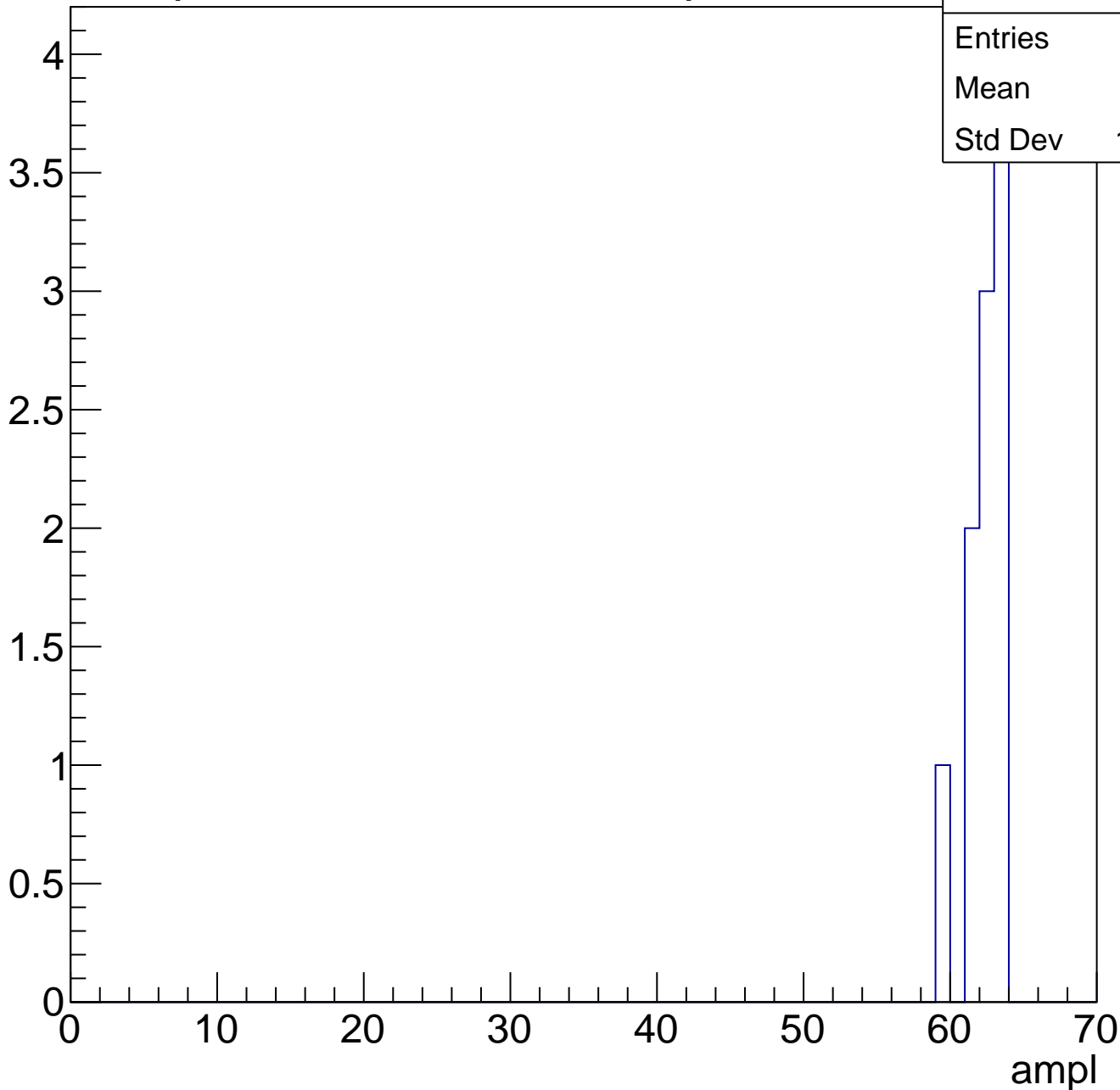
Entries	46
Mean	58.35
Std Dev	9.092



B1L103S, U7-ch53, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

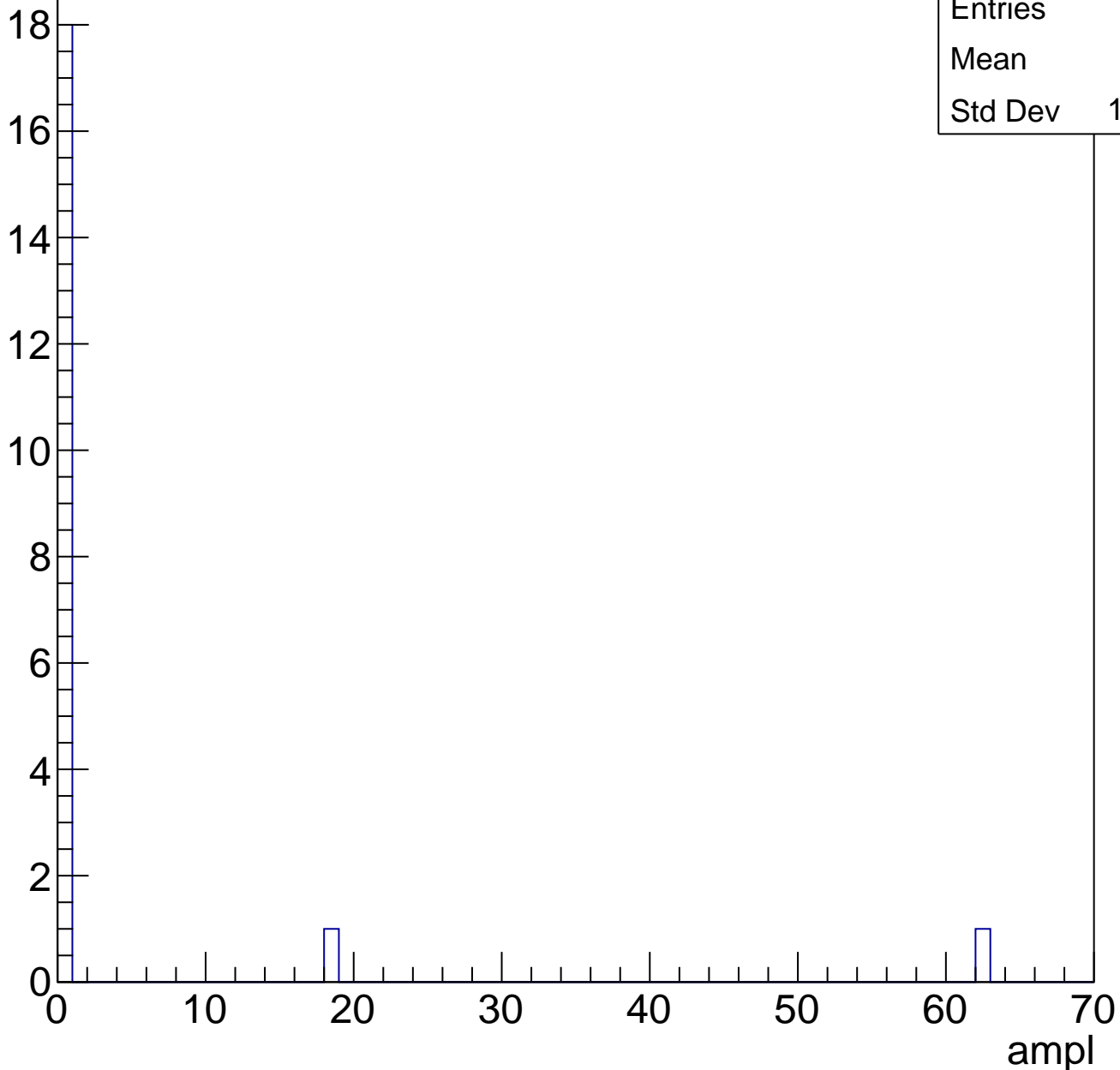


B1L103S, U7-ch53, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	4
Std Dev	13.87

Entry



B1L103S, U7-ch54, adc0

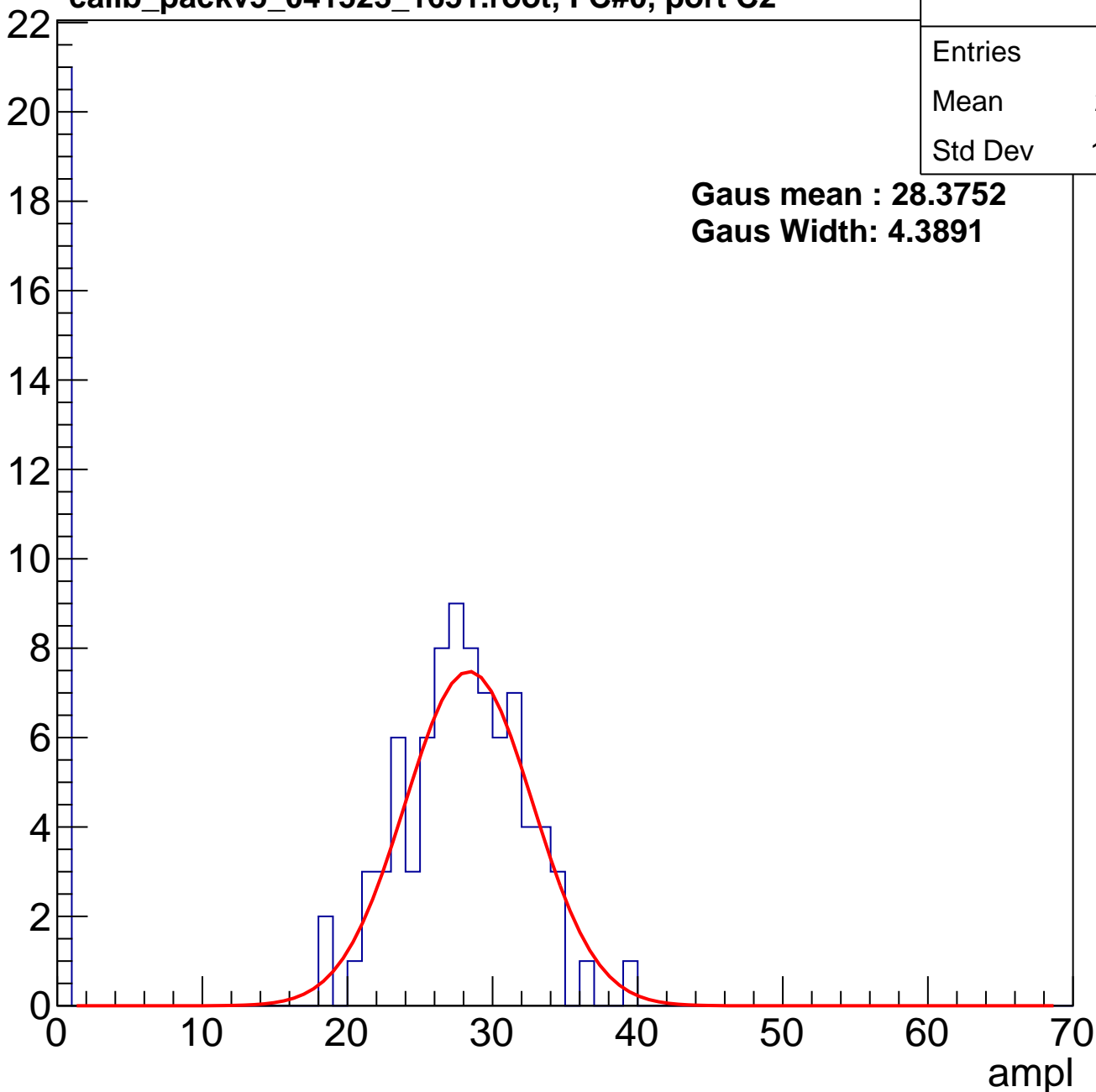
calib_packv5_041523_1651.root, FC#0, port C2

Entries	103
Mean	21.91
Std Dev	11.66

Gaus mean : 28.3752

Gaus Width: 4.3891

Entry



B1L103S, U7-ch54, adc1

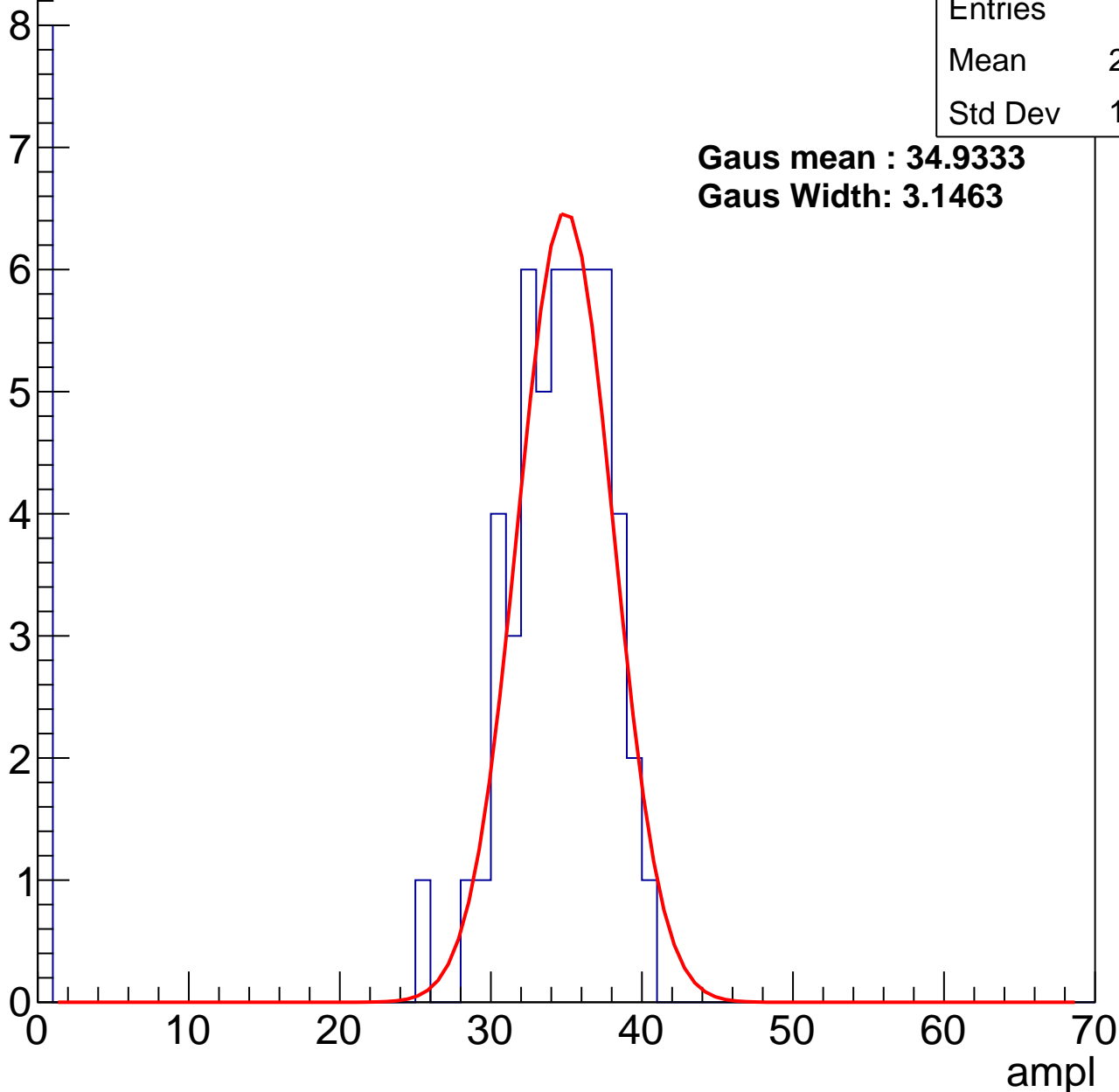
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	29.57
Std Dev	11.95

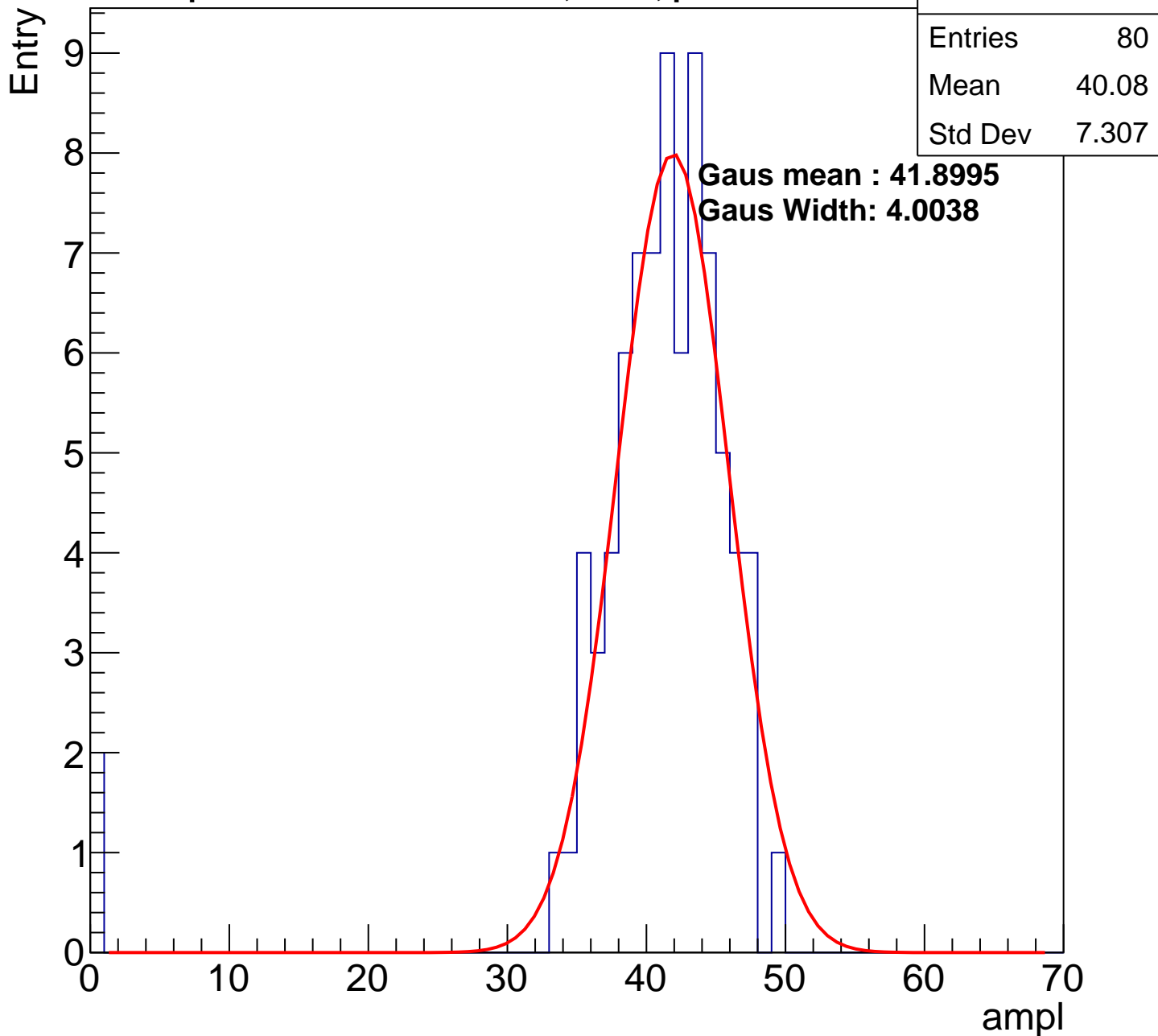
Gaus mean : 34.9333

Gaus Width: 3.1463



B1L103S, U7-ch54, adc2

calib_packv5_041523_1651.root, FC#0, port C2

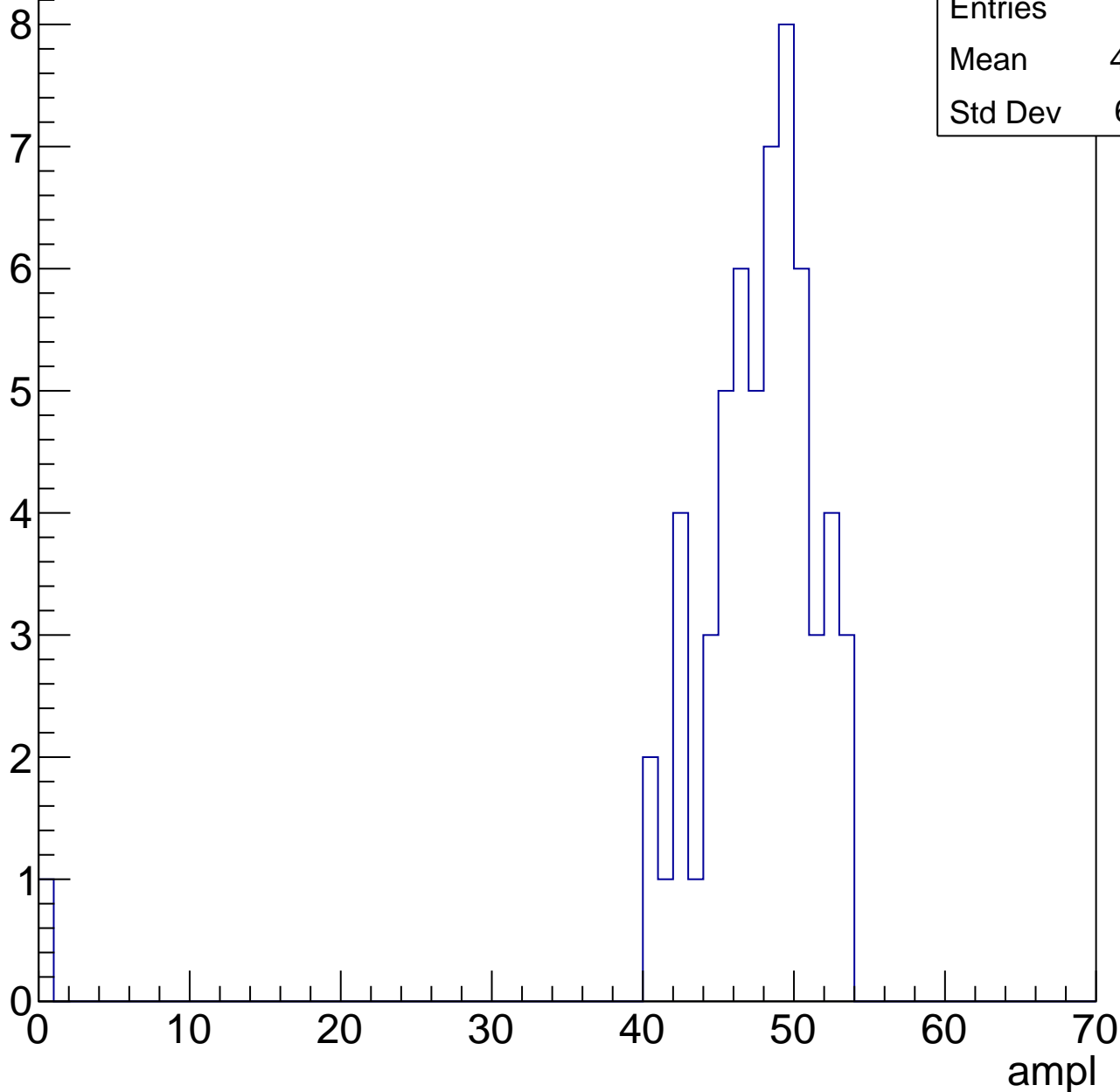


B1L103S, U7-ch54, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	46.58
Std Dev	6.951

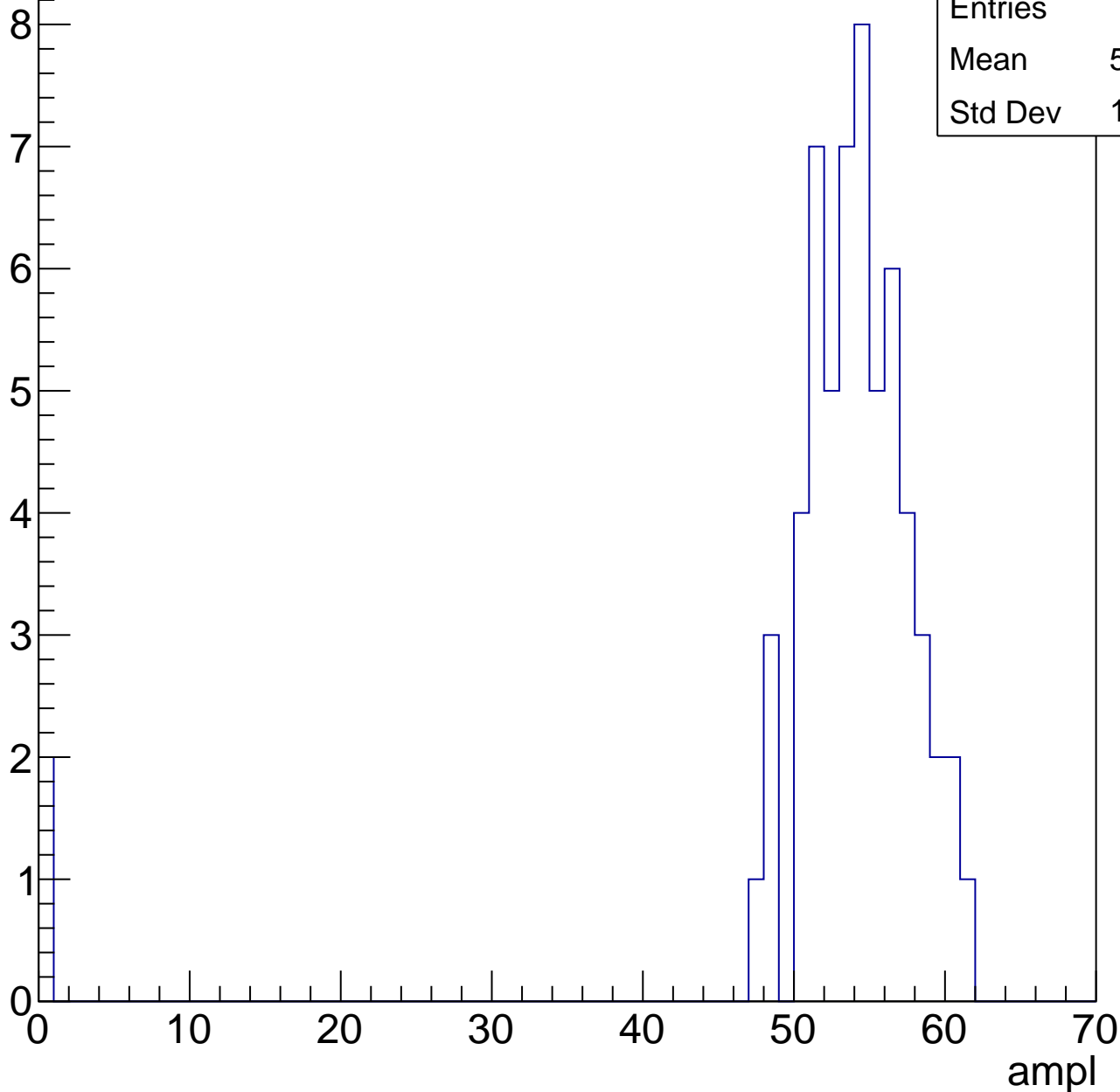


B1L103S, U7-ch54, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	52.05
Std Dev	10.16

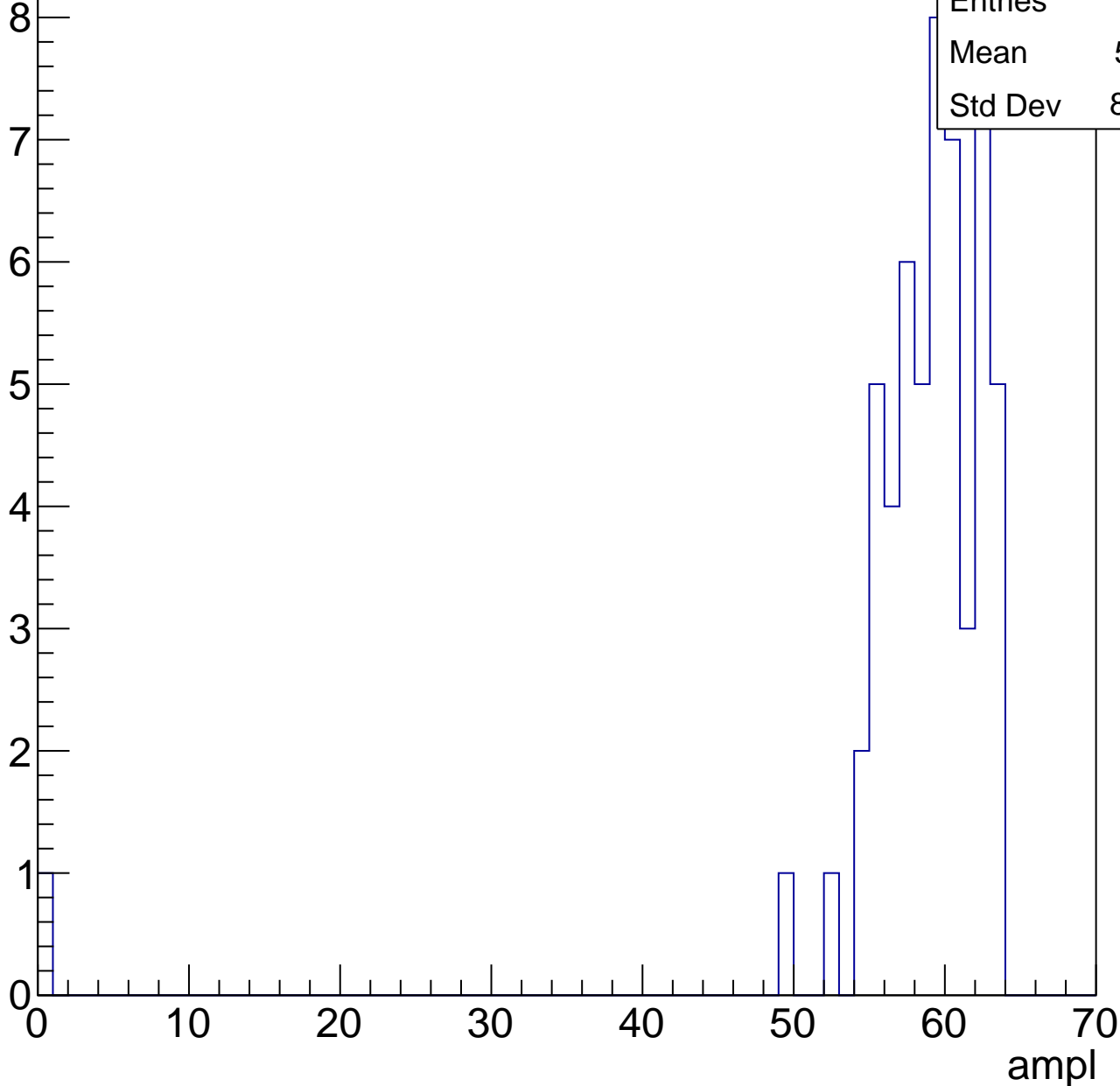


B1L103S, U7-ch54, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	57.61
Std Dev	8.332

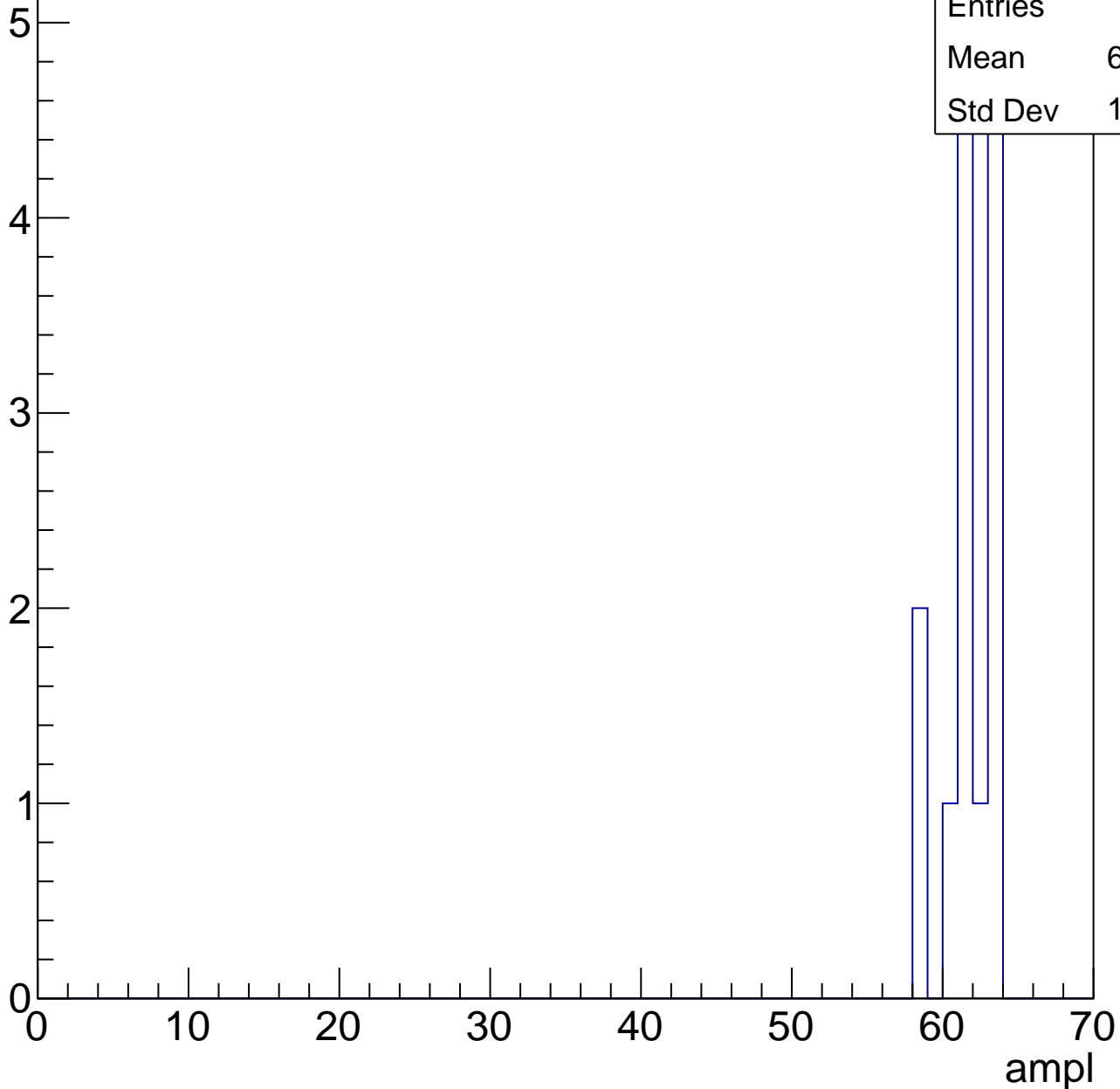


B1L103S, U7-ch54, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	14
Mean	61.29
Std Dev	1.666



B1L103S, U7-ch54, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	21
Mean	5.857
Std Dev	18.05

ampl

0 10 20 30 40 50 60 70

B1L103S, U7-ch55, adc0

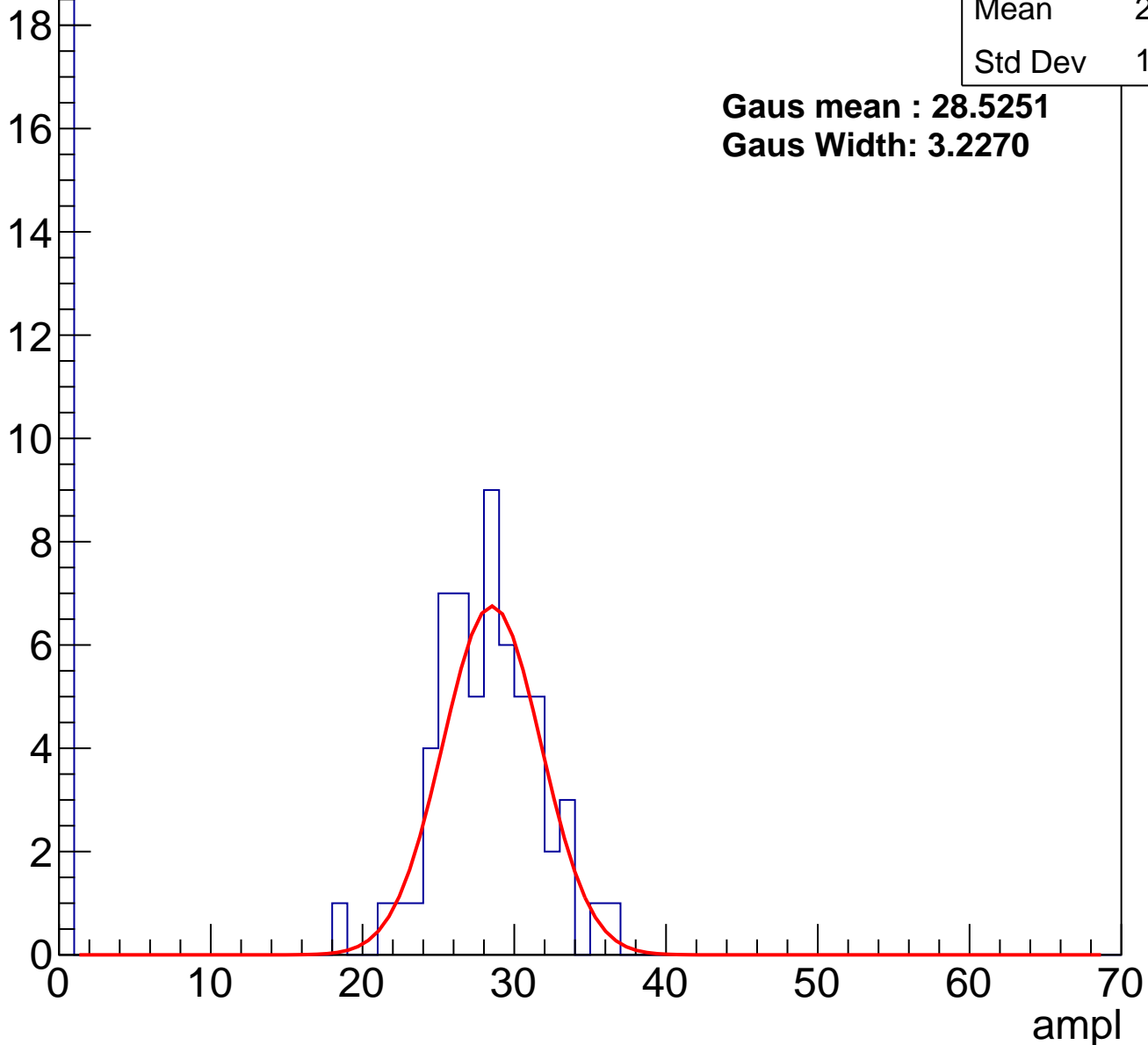
calib_packv5_041523_1651.root, FC#0, port C2

Entries	78
Mean	20.99
Std Dev	12.26

Gaus mean : 28.5251

Gaus Width: 3.2270

Entry



B1L103S, U7-ch55, adc1

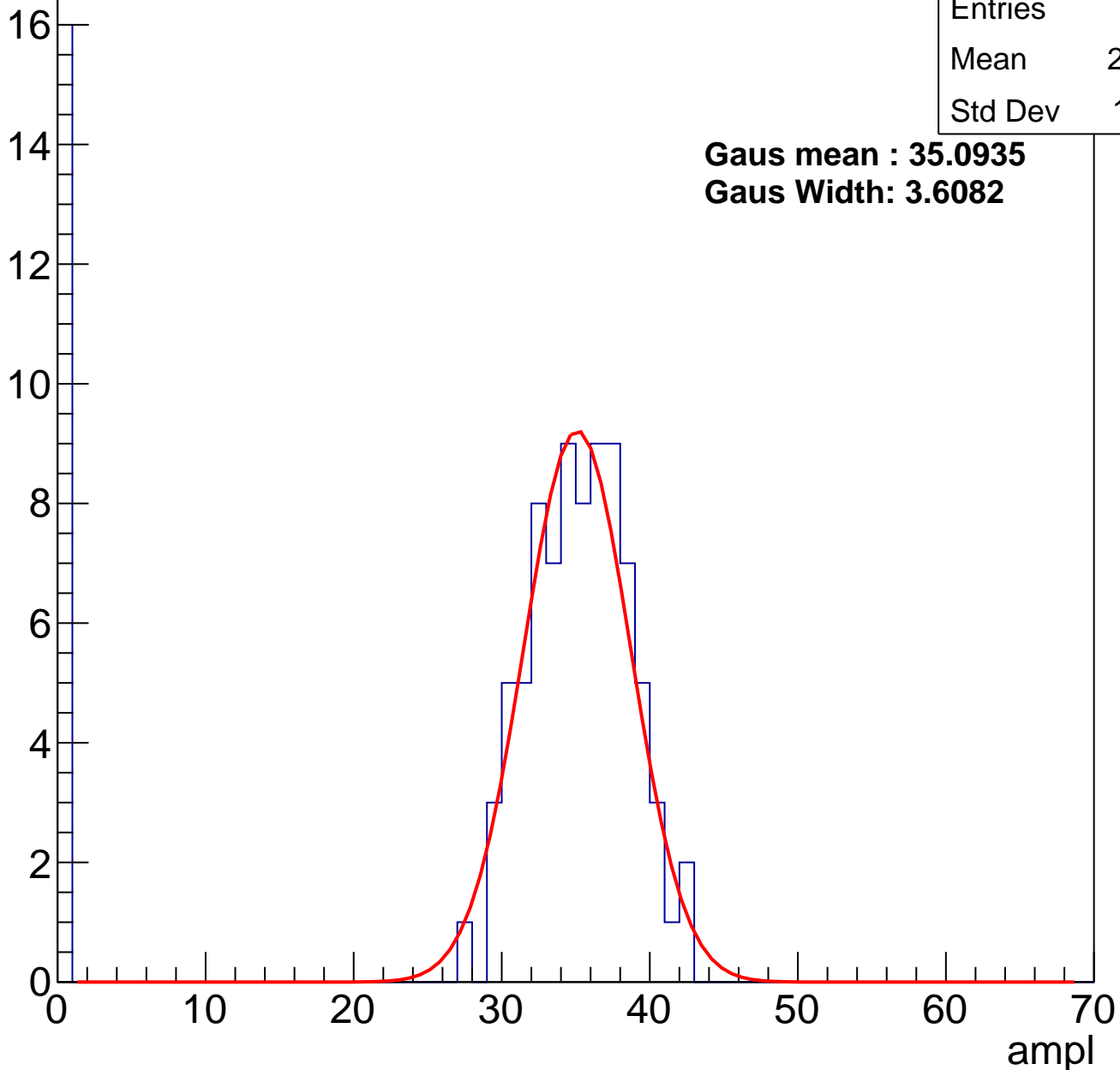
calib_packv5_041523_1651.root, FC#0, port C2

Entries	98
Mean	29.13
Std Dev	13.21

Gaus mean : 35.0935

Gaus Width: 3.6082

Entry



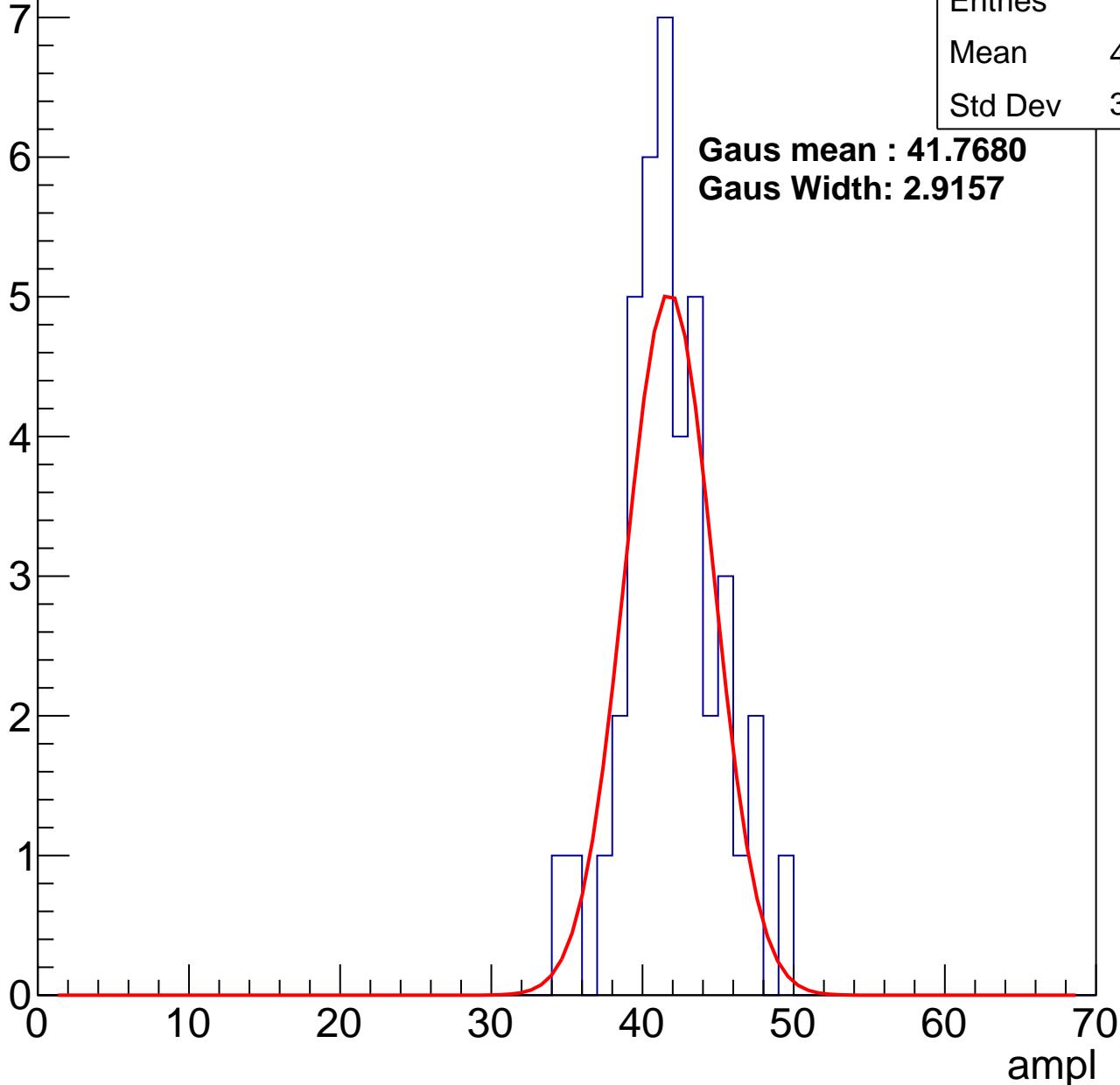
B1L103S, U7-ch55, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	41
Mean	41.44
Std Dev	3.077

Gaus mean : 41.7680
Gaus Width: 2.9157

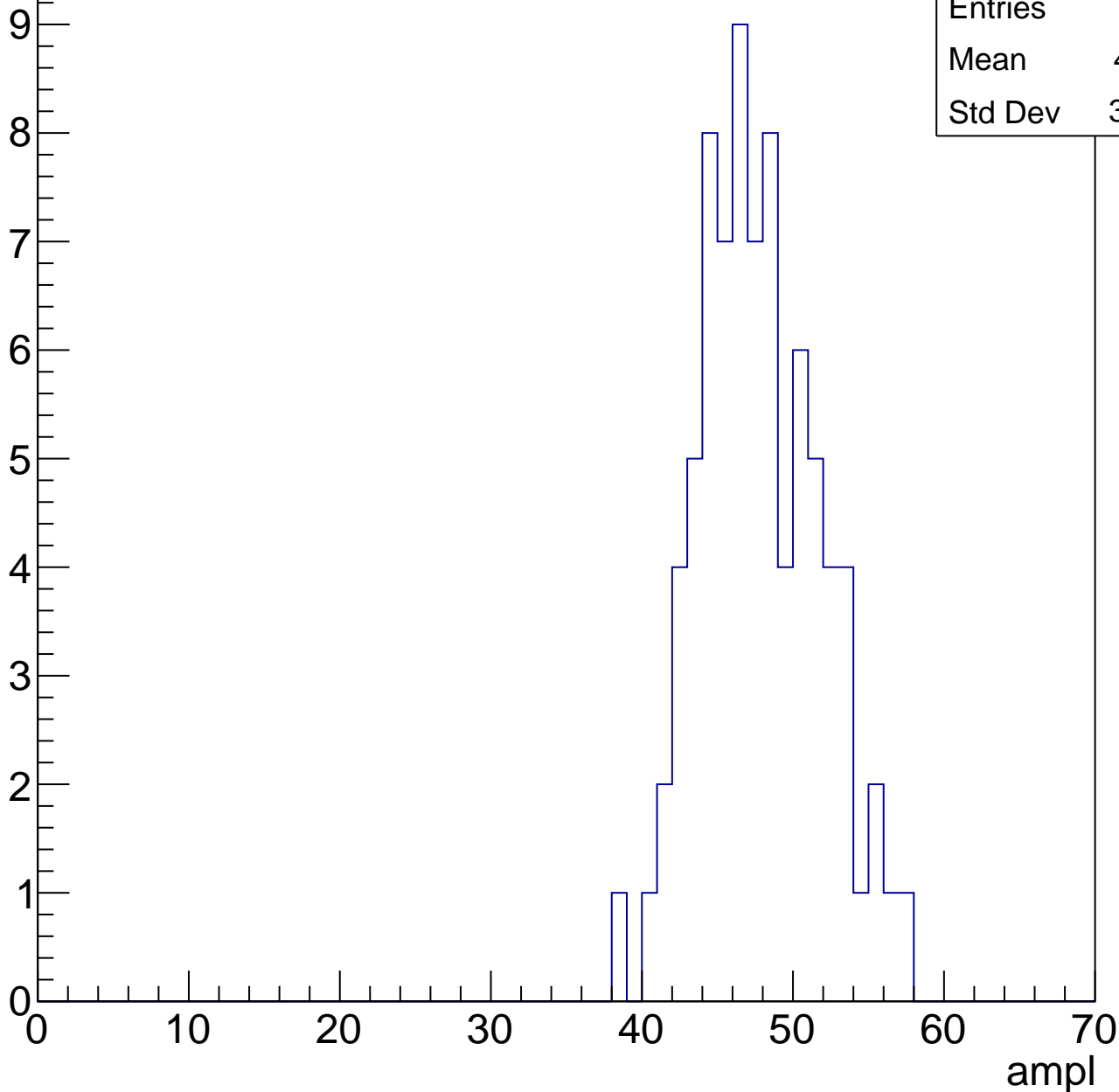


B1L103S, U7-ch55, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	80
Mean	47.31
Std Dev	3.942

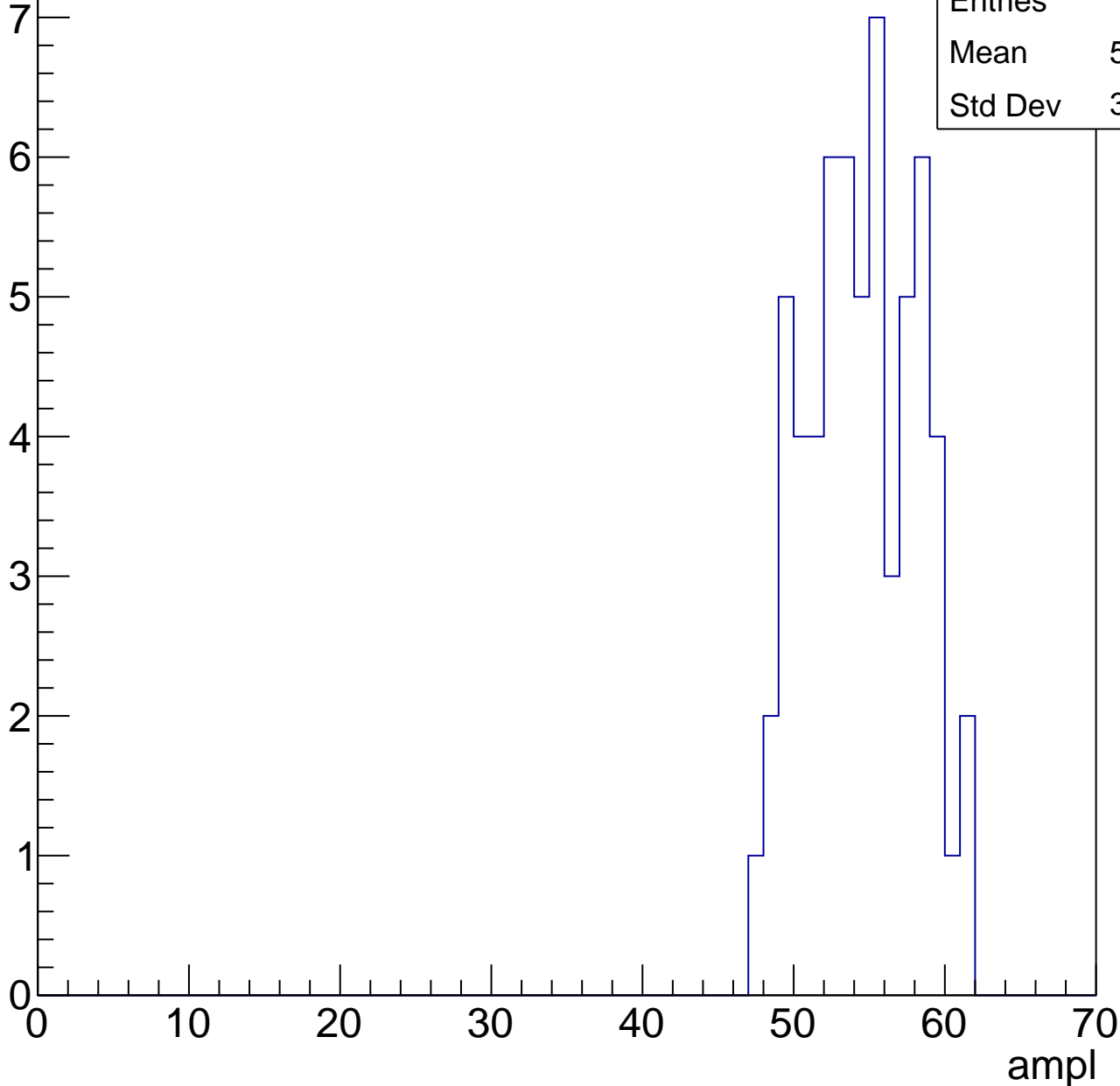


B1L103S, U7-ch55, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	54.03
Std Dev	3.553

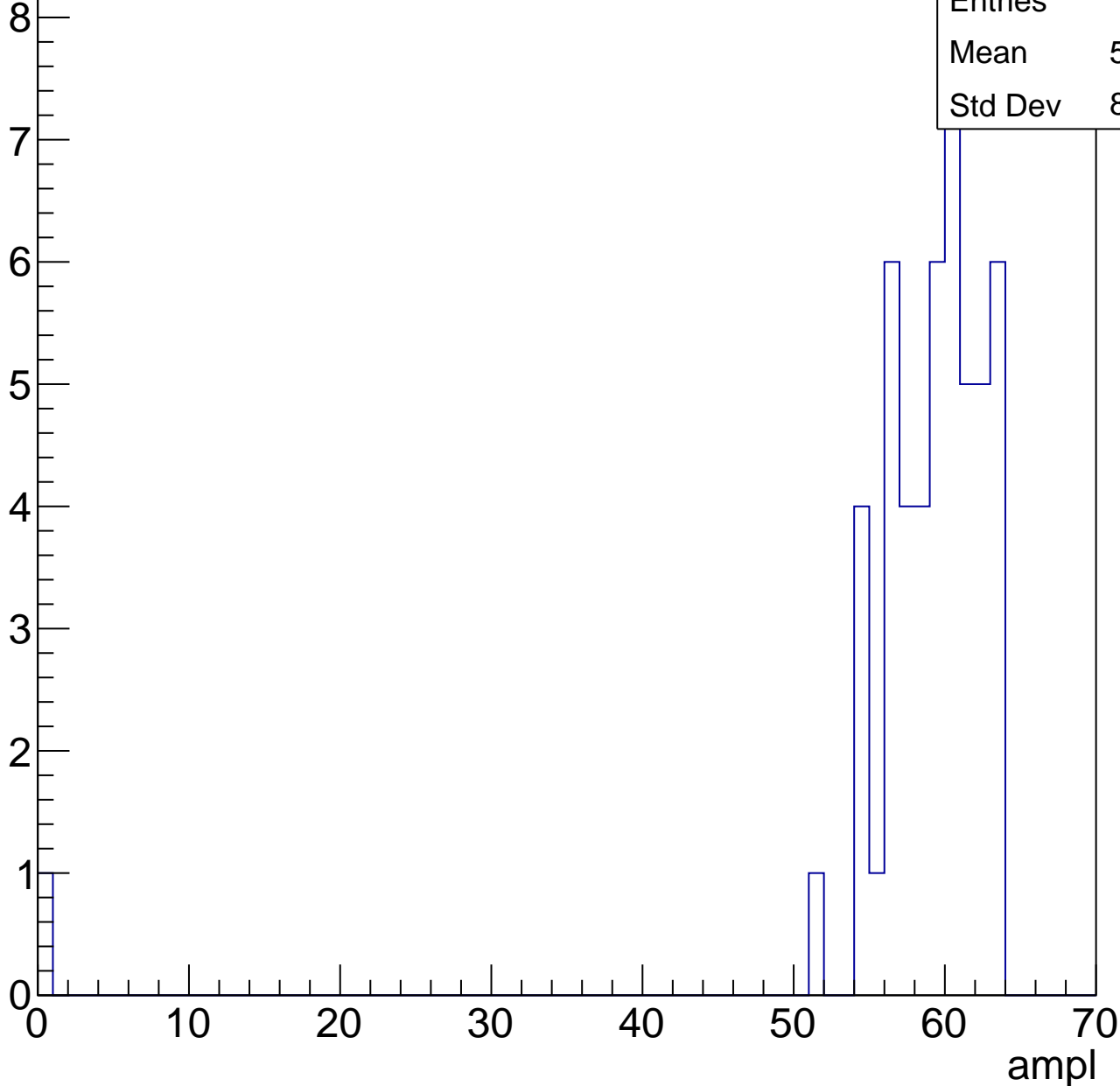


B1L103S, U7-ch55, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

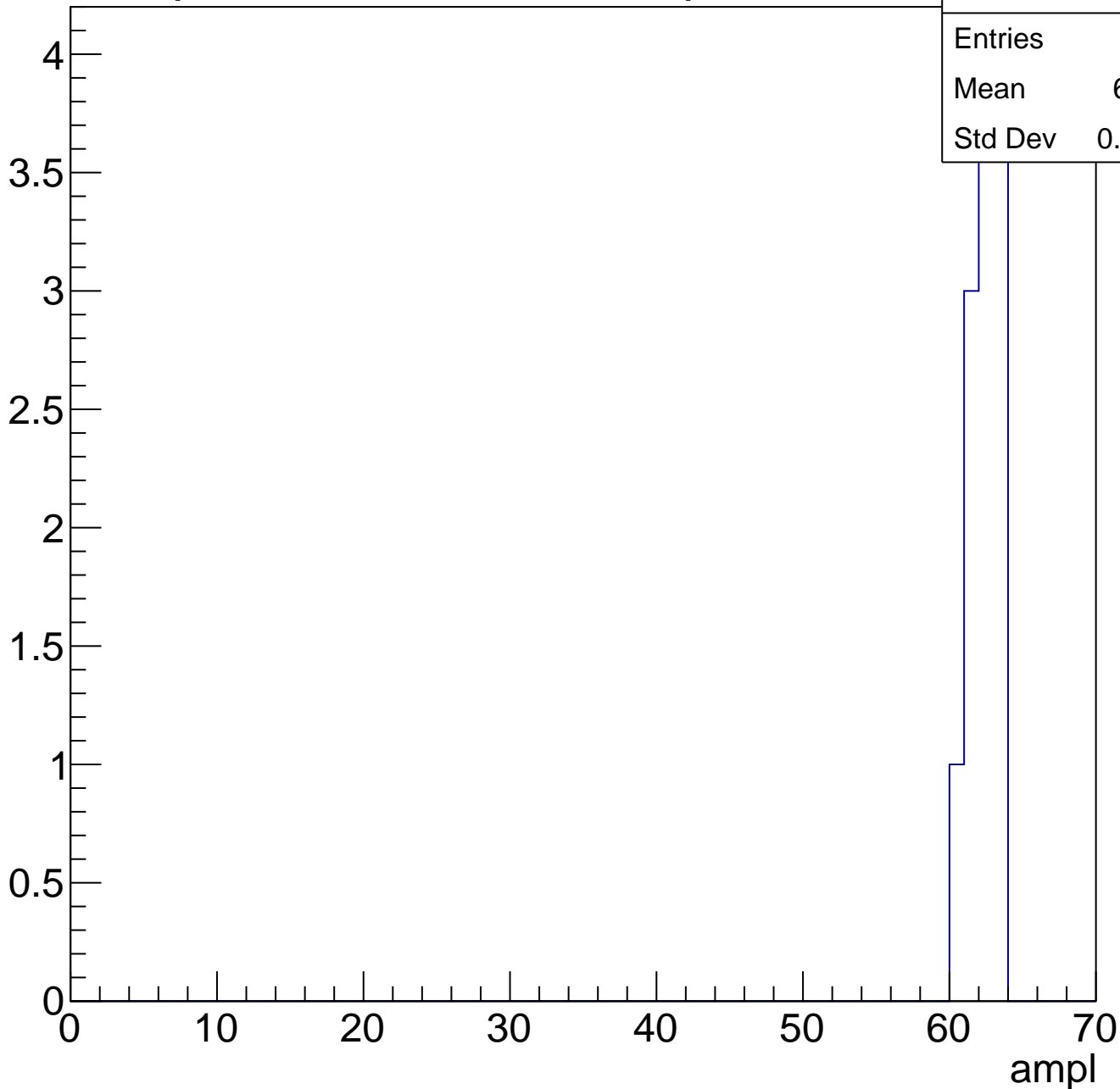
Entries	51
Mean	57.75
Std Dev	8.659



B1L103S, U7-ch55, adc6

calib_packv5_041523_1651.root, FC#0, port C2

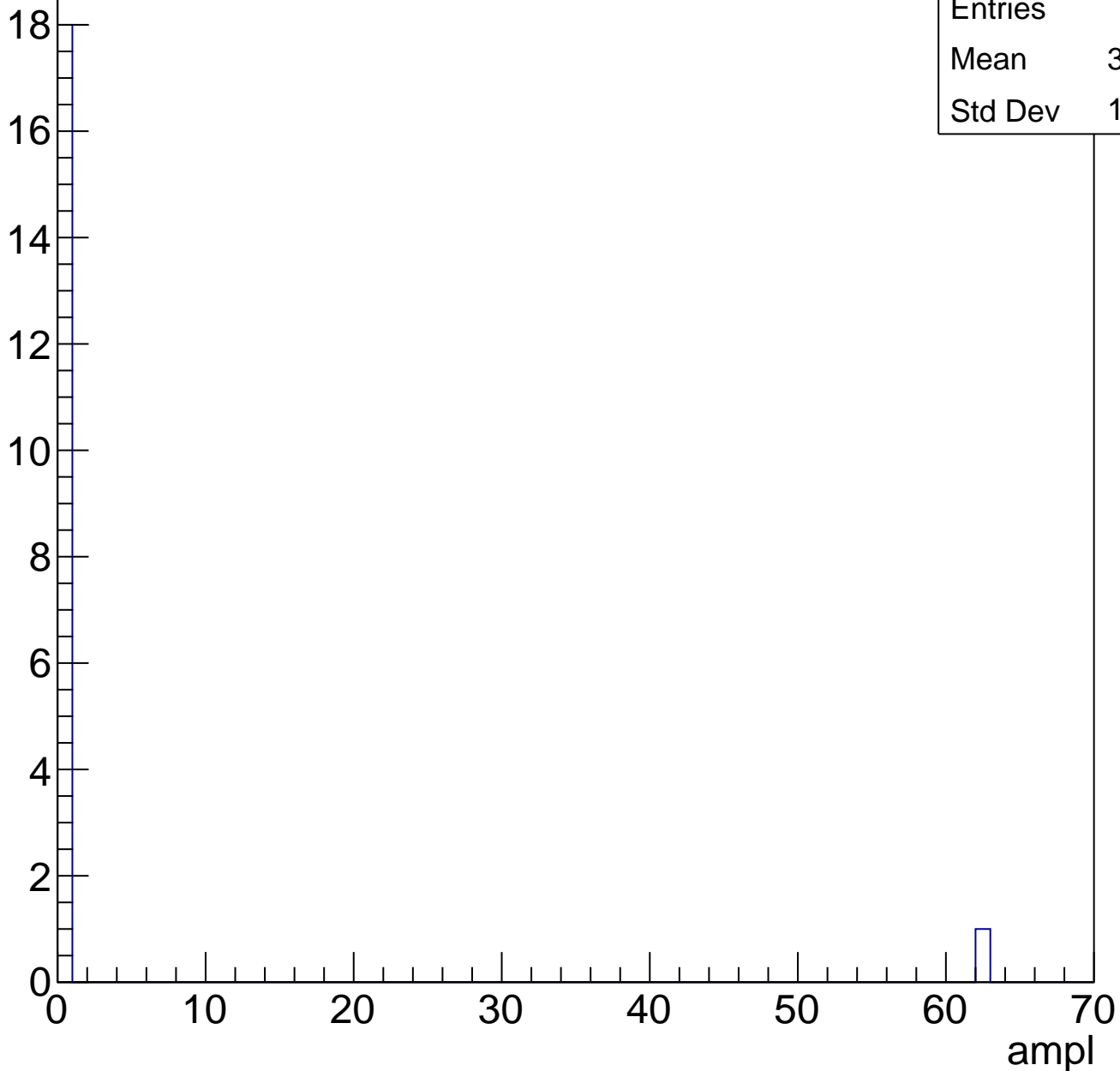
Entry



B1L103S, U7-ch55, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	19
Mean	3.263
Std Dev	13.84

B1L103S, U7-ch56, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	104
Mean	23.39
Std Dev	10.29

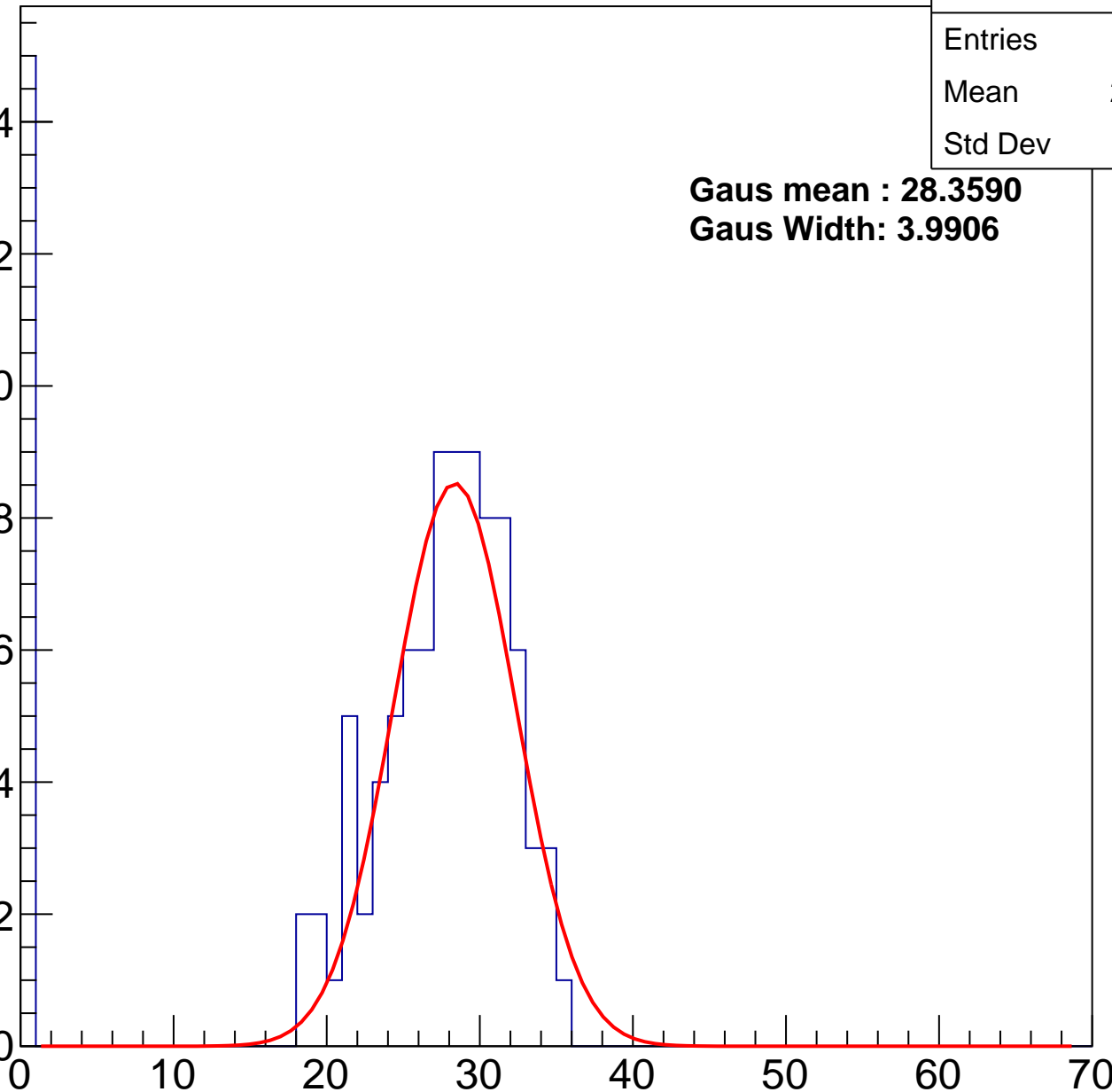
Gaus mean : 28.3590

Gaus Width: 3.9906

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch56, adc1

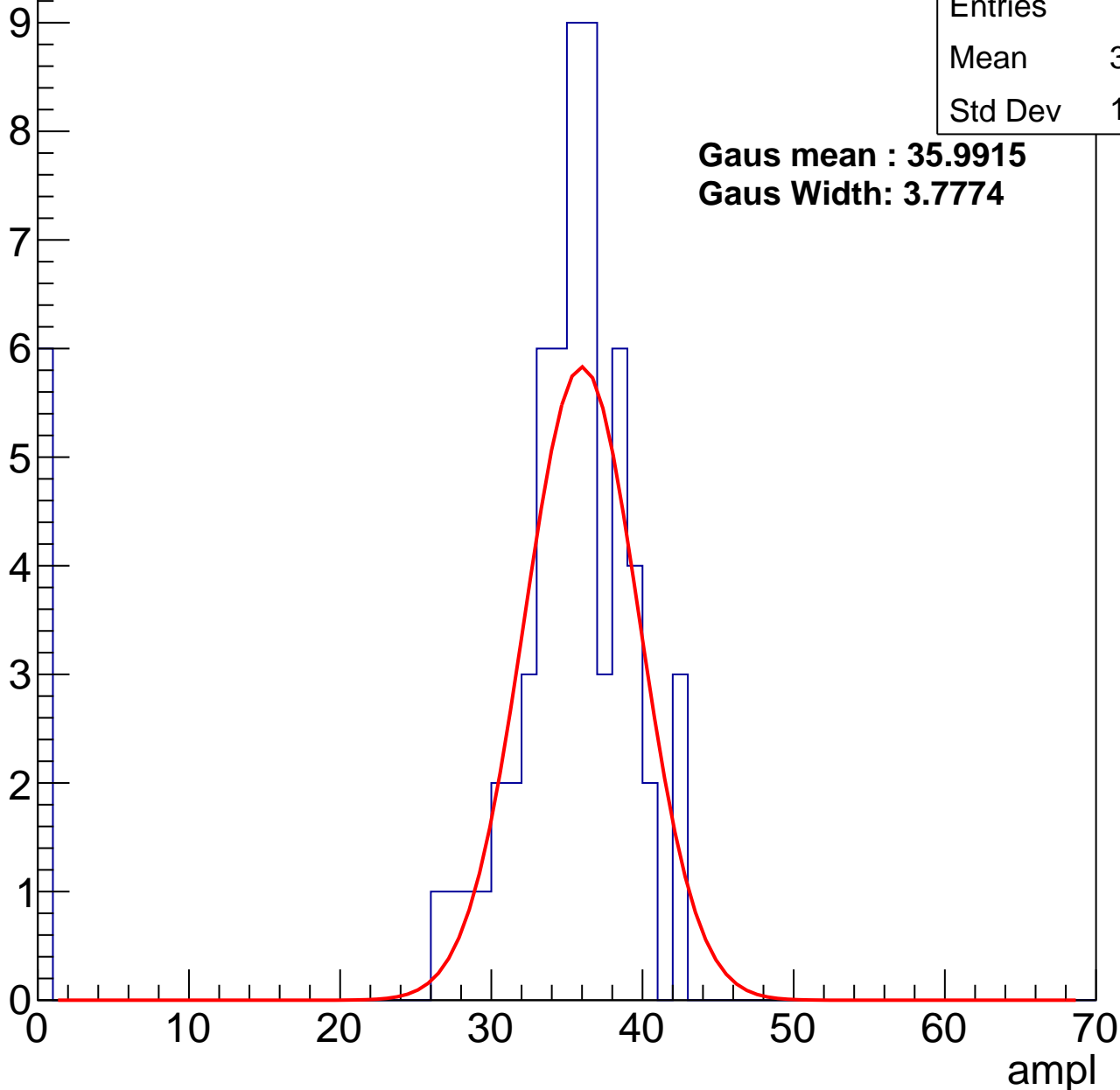
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	31.85
Std Dev	10.68

Gaus mean : 35.9915

Gaus Width: 3.7774



B1L103S, U7-ch56, adc2

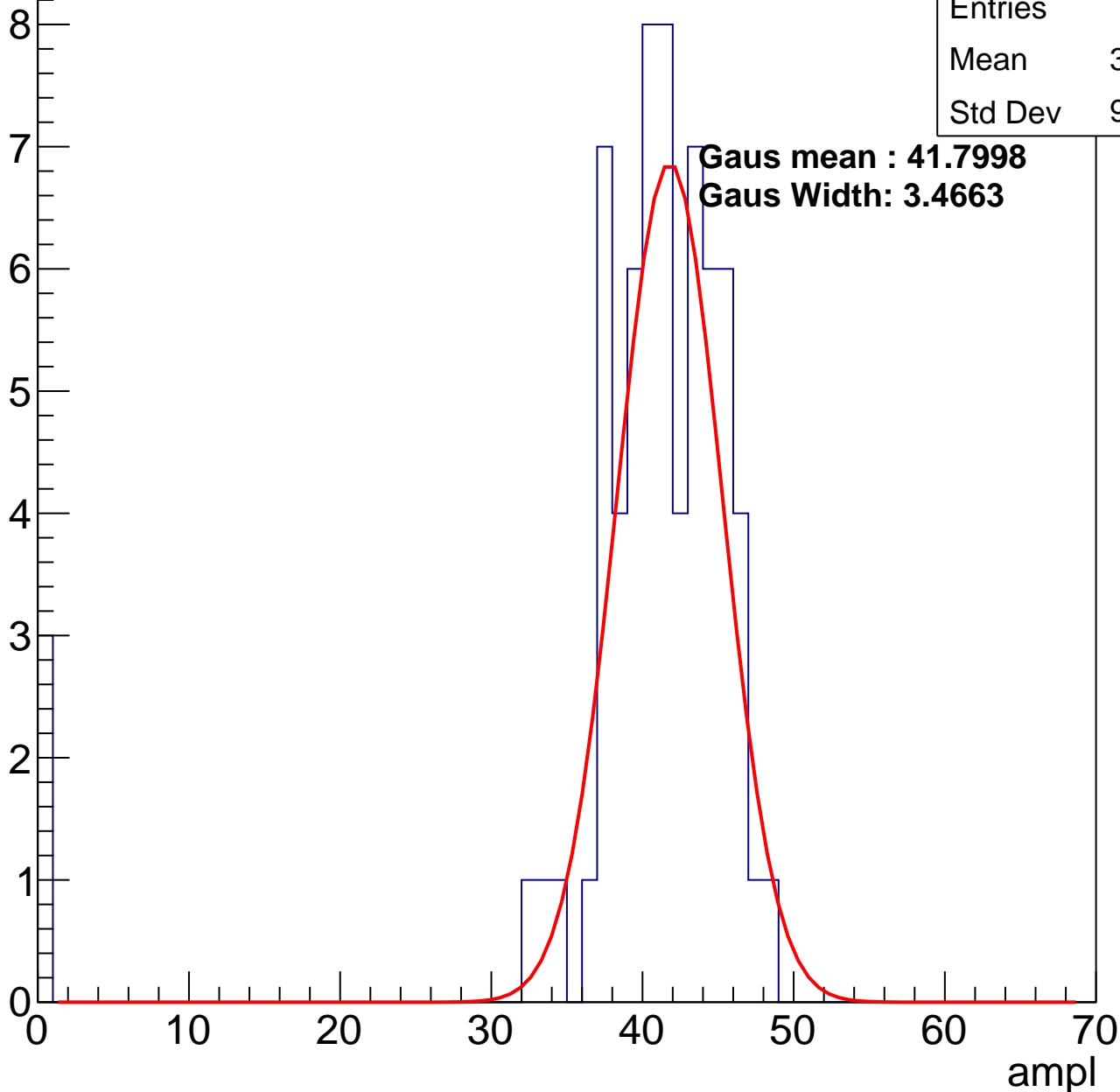
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	39.28
Std Dev	9.012

Gaus mean : 41.7998

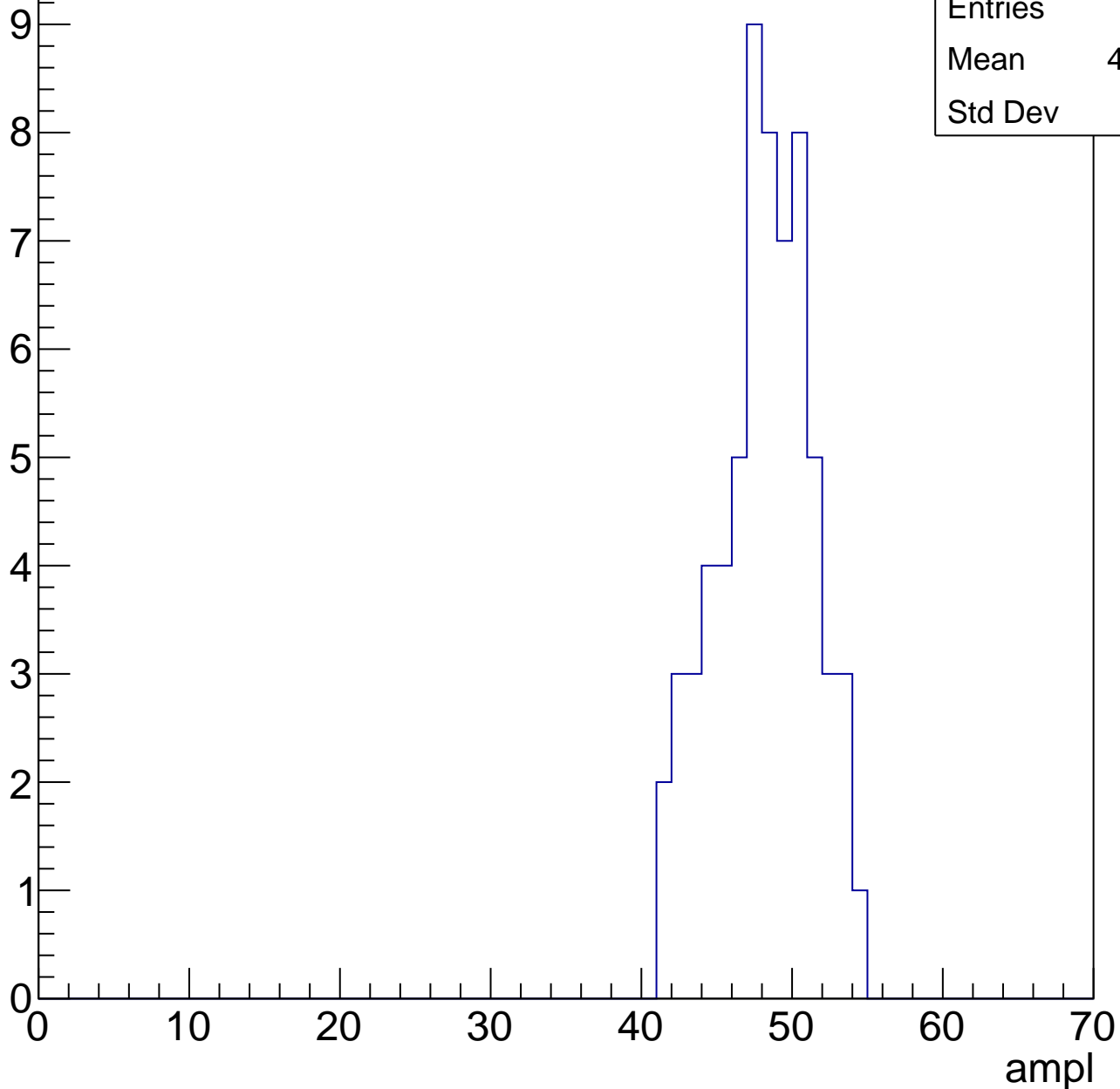
Gaus Width: 3.4663



B1L103S, U7-ch56, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

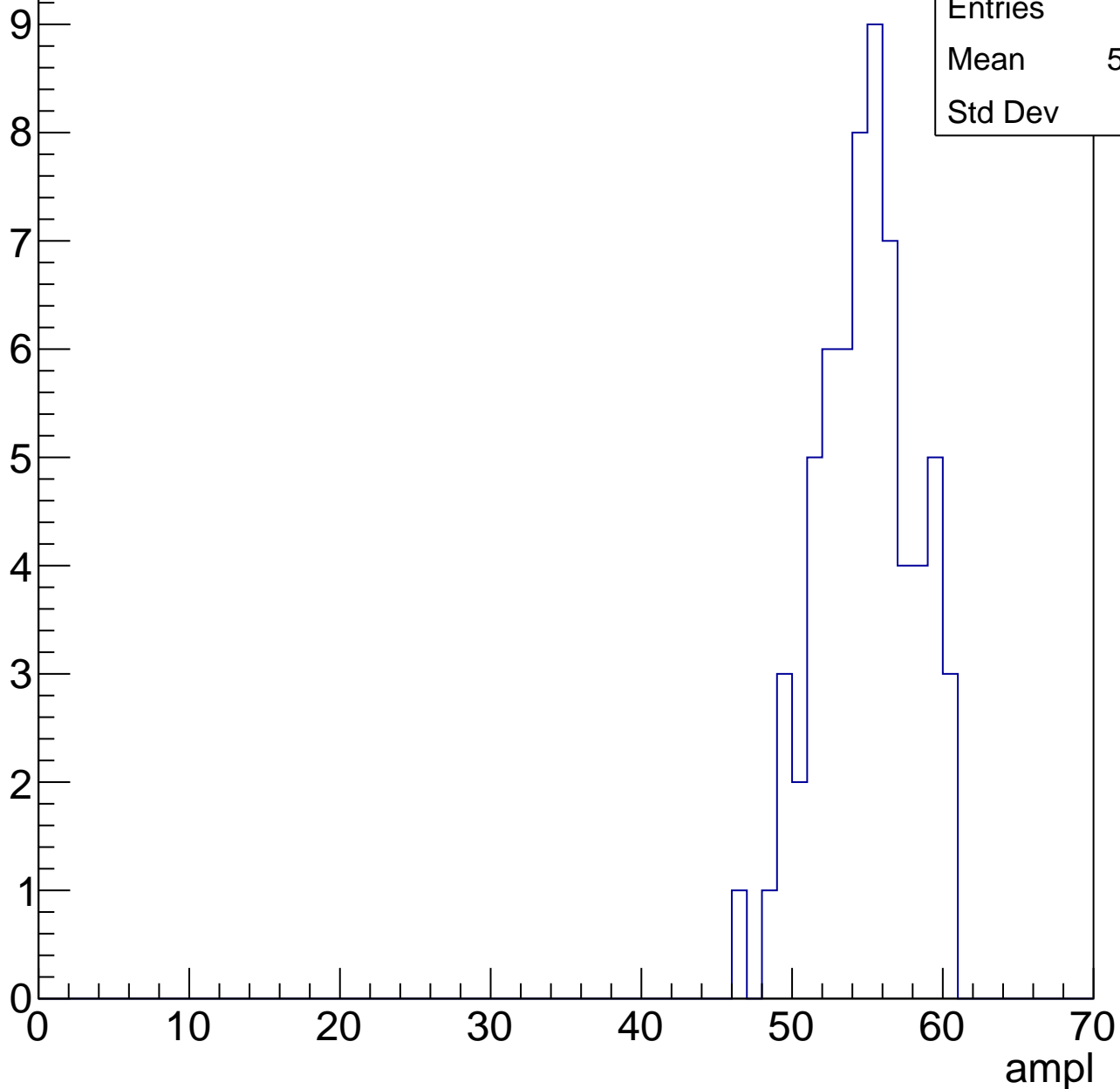


Entries	65
Mean	47.65
Std Dev	3.15

B1L103S, U7-ch56, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

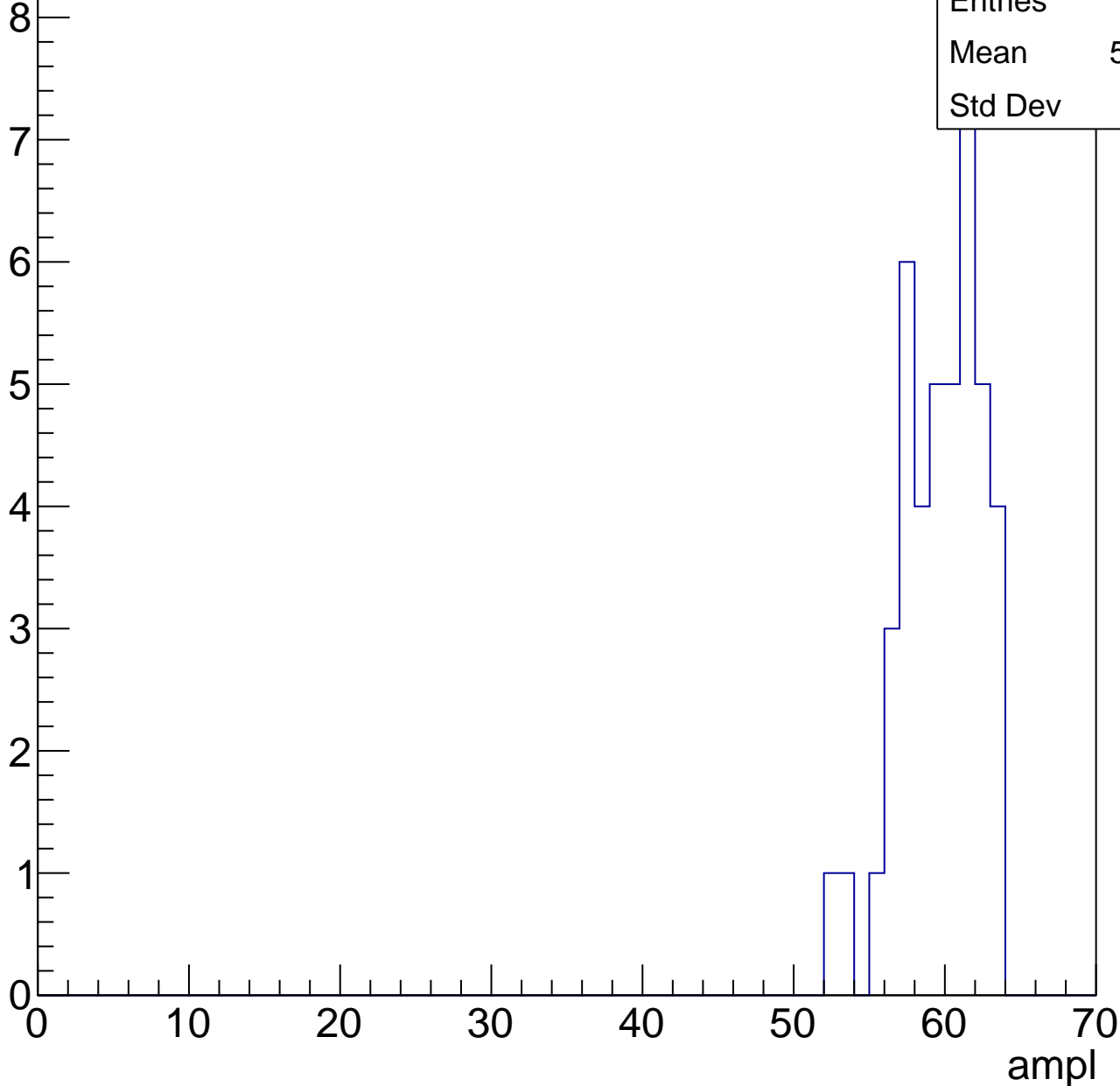


B1L103S, U7-ch56, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	43
Mean	59.23
Std Dev	2.64

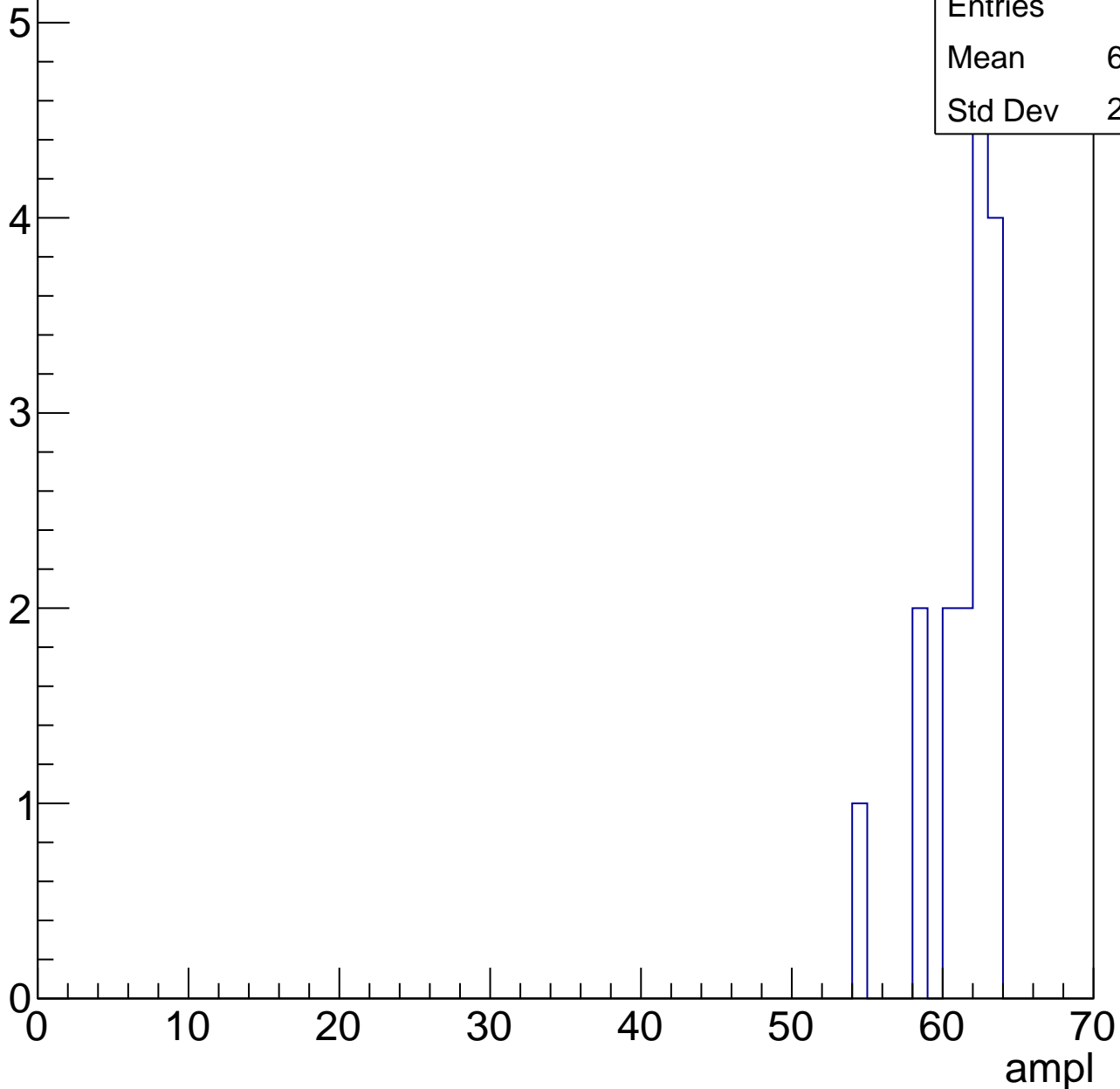


B1L103S, U7-ch56, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	16
Mean	60.88
Std Dev	2.368



B1L103S, U7-ch56, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

20
18
16
14
12
10
8
6
4
2
0

Entries	22
Mean	5.727
Std Dev	18.11

0 10 20 30 40 50 60 70

ampl

2

B1L103S, U7-ch57, adc0

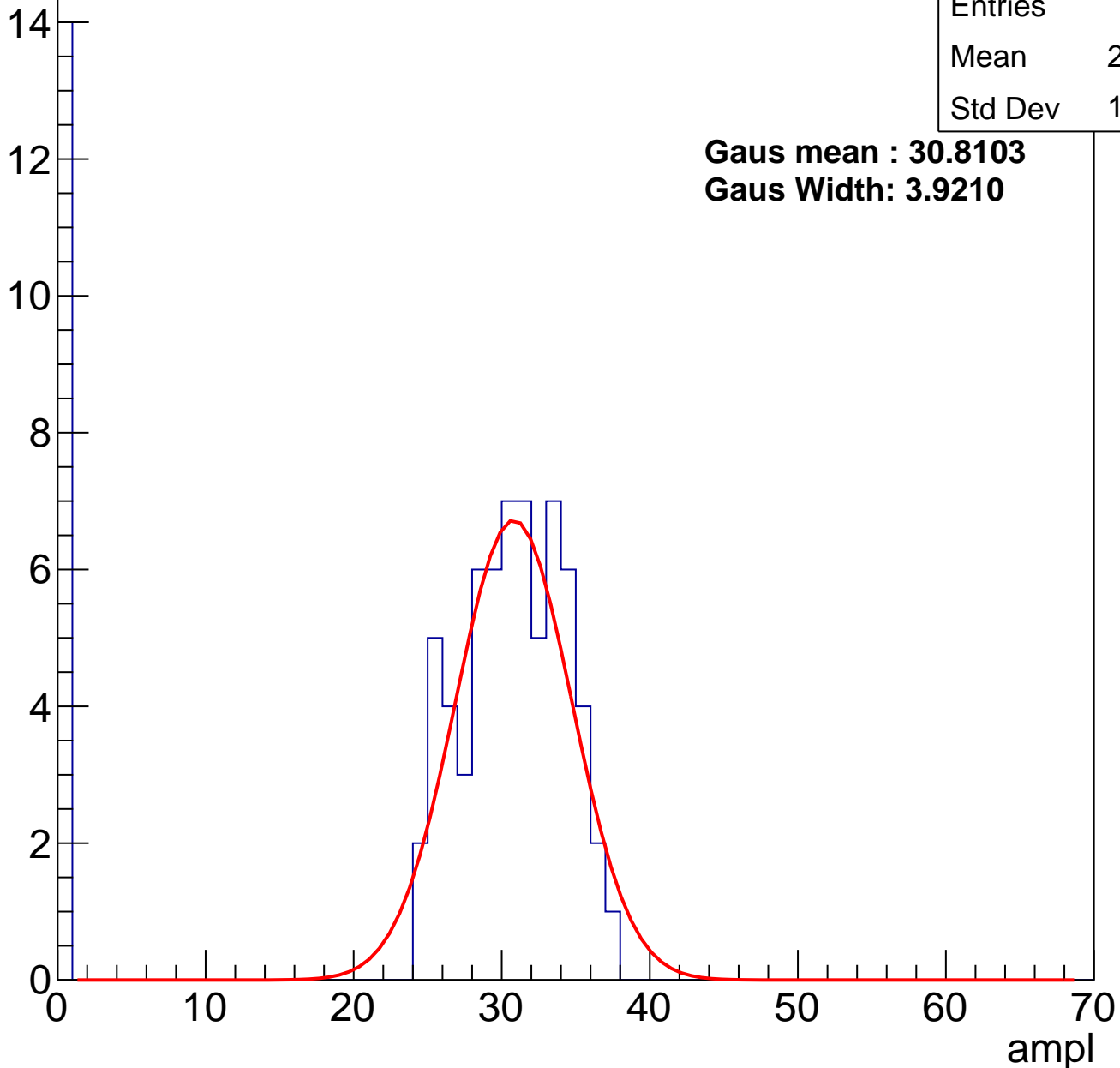
calib_packv5_041523_1651.root, FC#0, port C2

Entries	79
Mean	24.95
Std Dev	11.97

Gaus mean : 30.8103

Gaus Width: 3.9210

Entry



B1L103S, U7-ch57, adc1

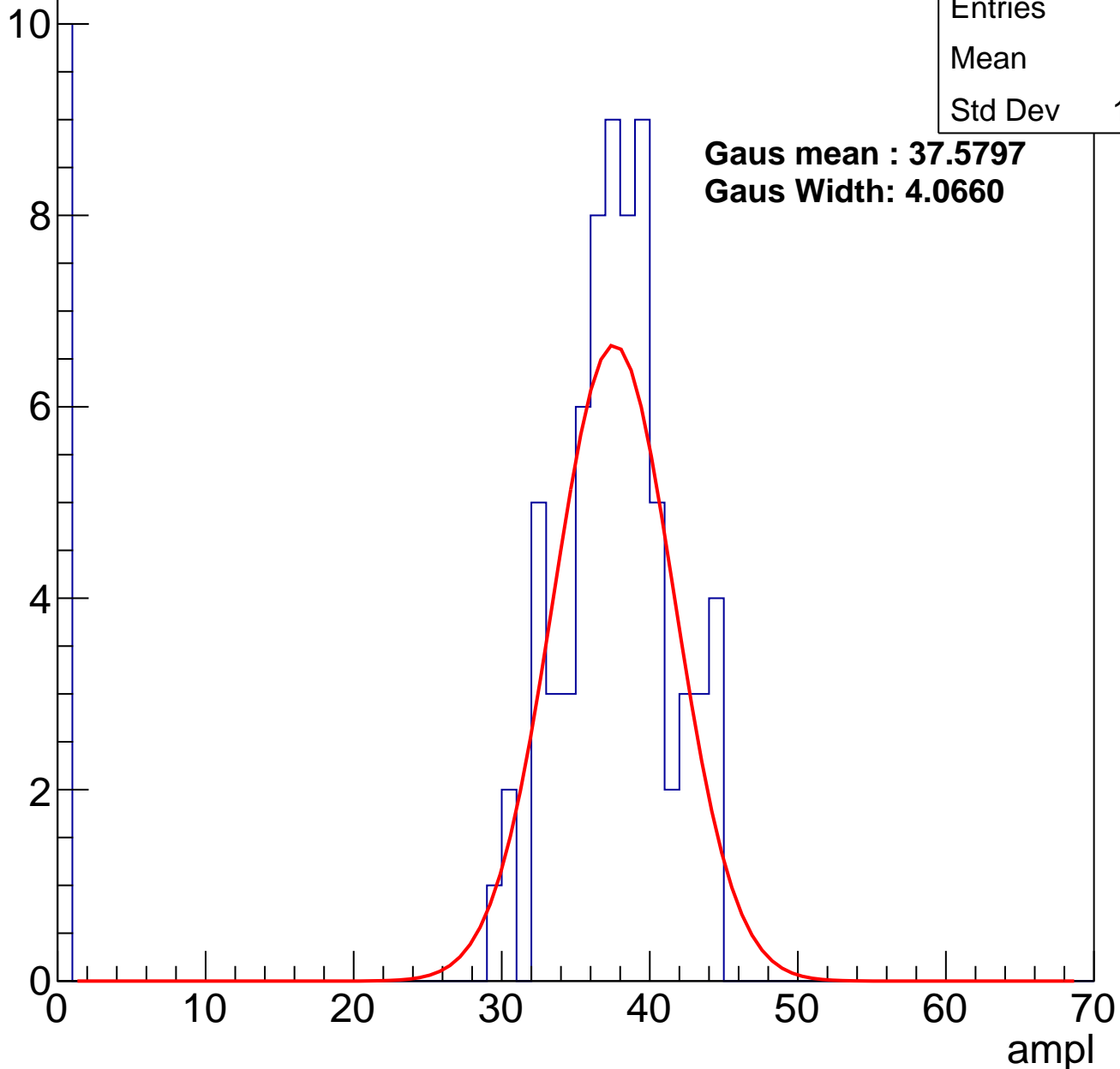
calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	32.7
Std Dev	12.71

Gaus mean : 37.5797

Gaus Width: 4.0660

Entry



B1L103S, U7-ch57, adc2

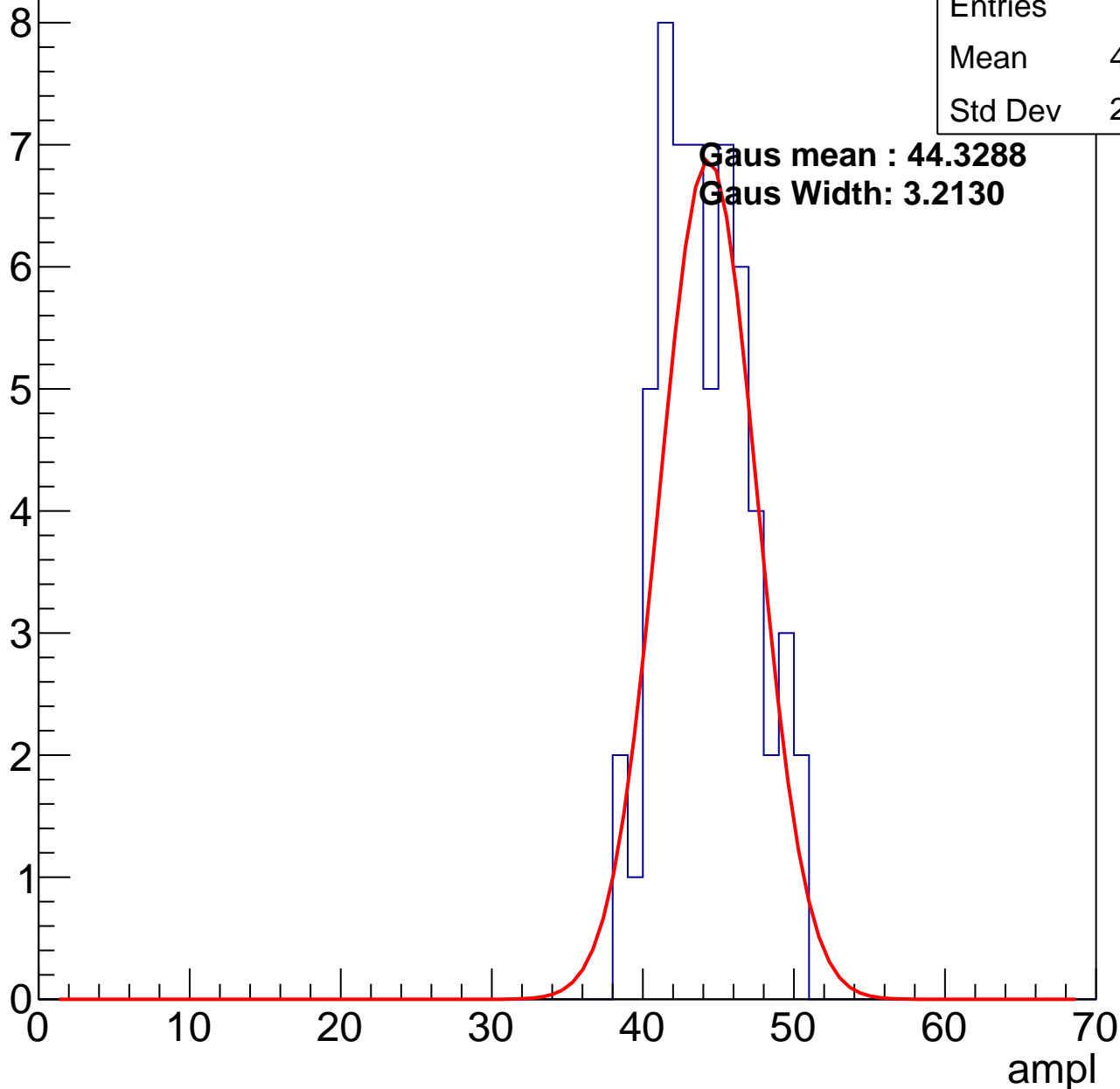
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	43.73
Std Dev	2.985

Gaus mean : 44.3288

Gaus Width: 3.2130

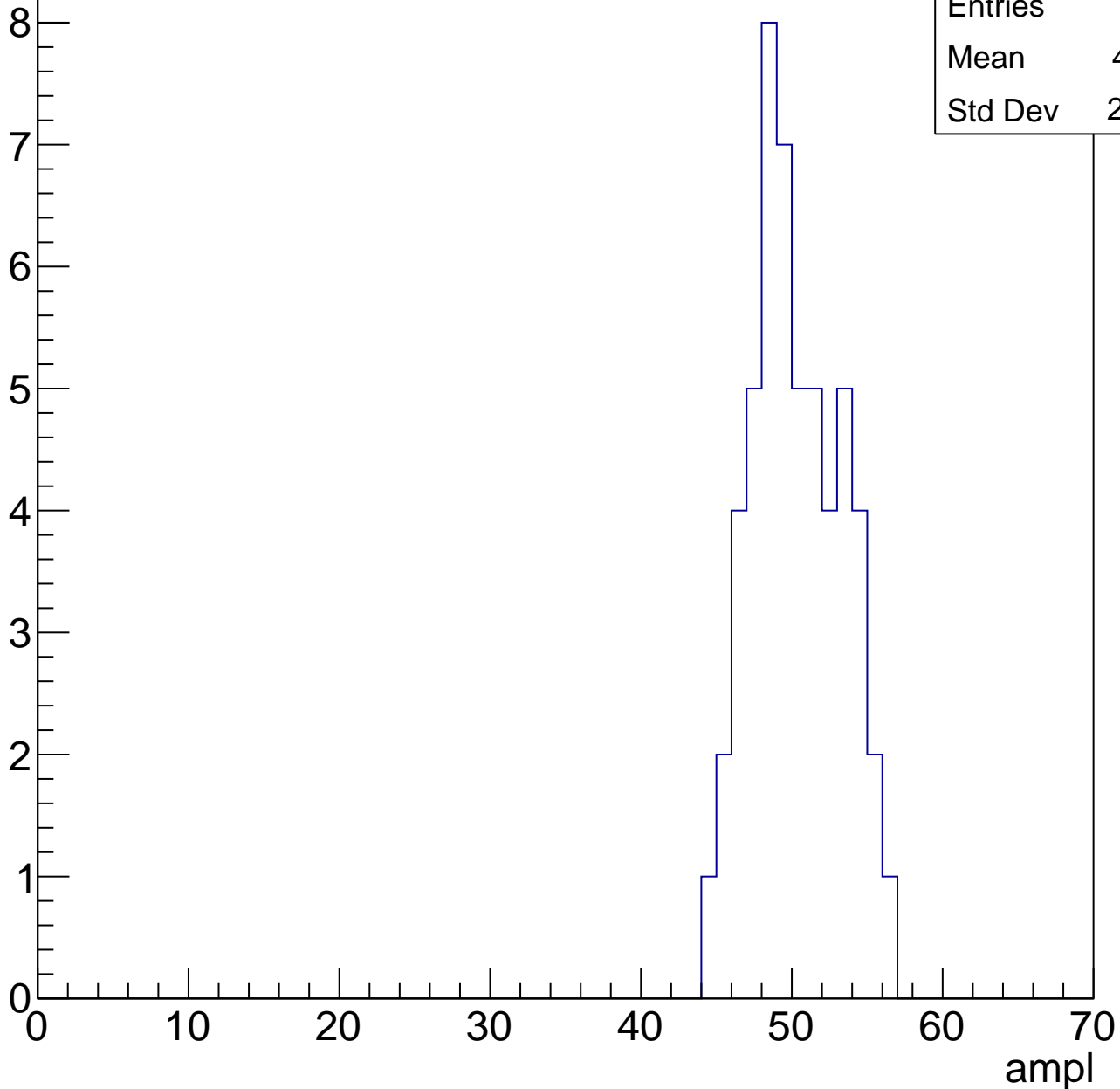


B1L103S, U7-ch57, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	49.81
Std Dev	2.908

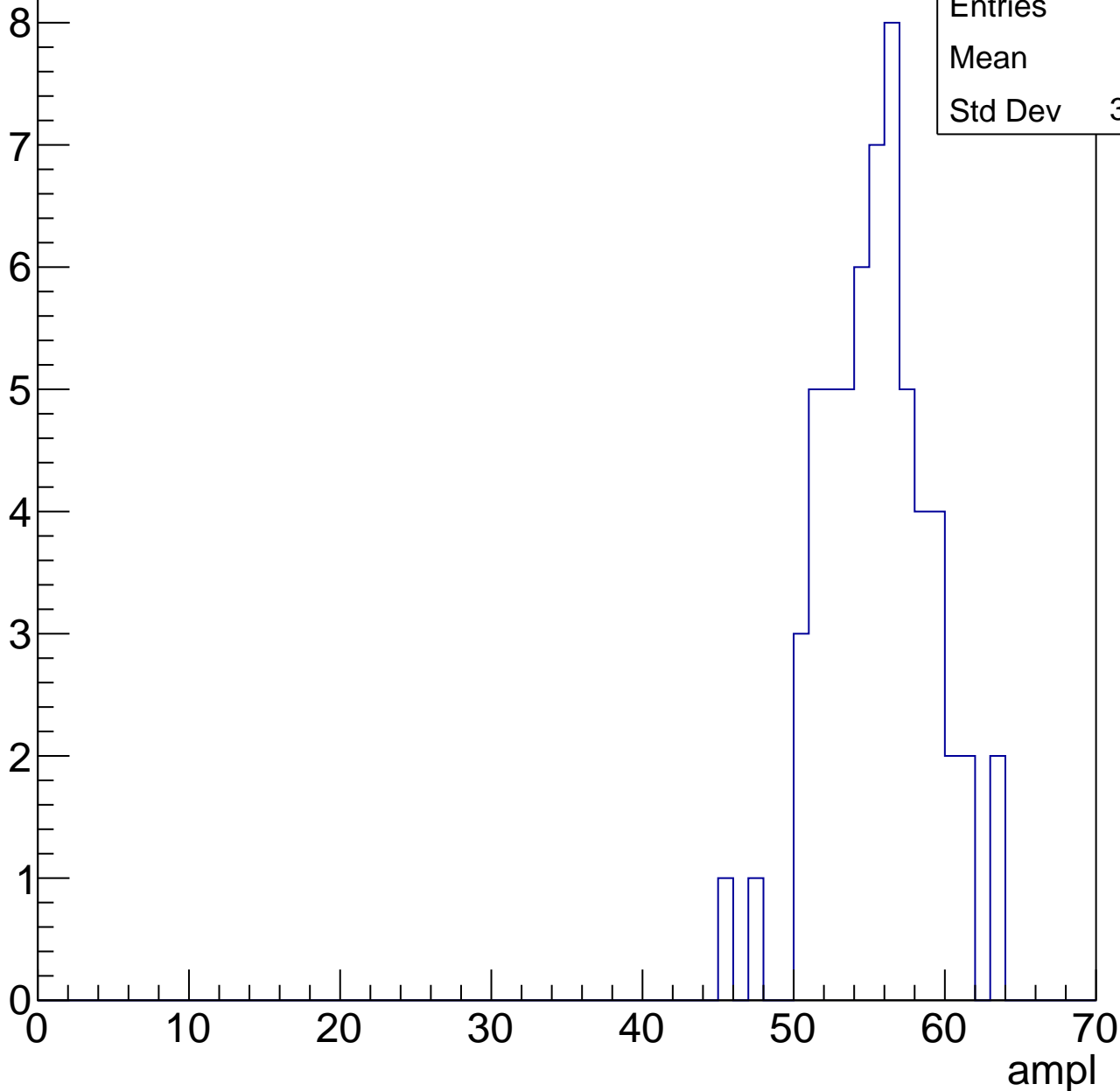


B1L103S, U7-ch57, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	55
Std Dev	3.578

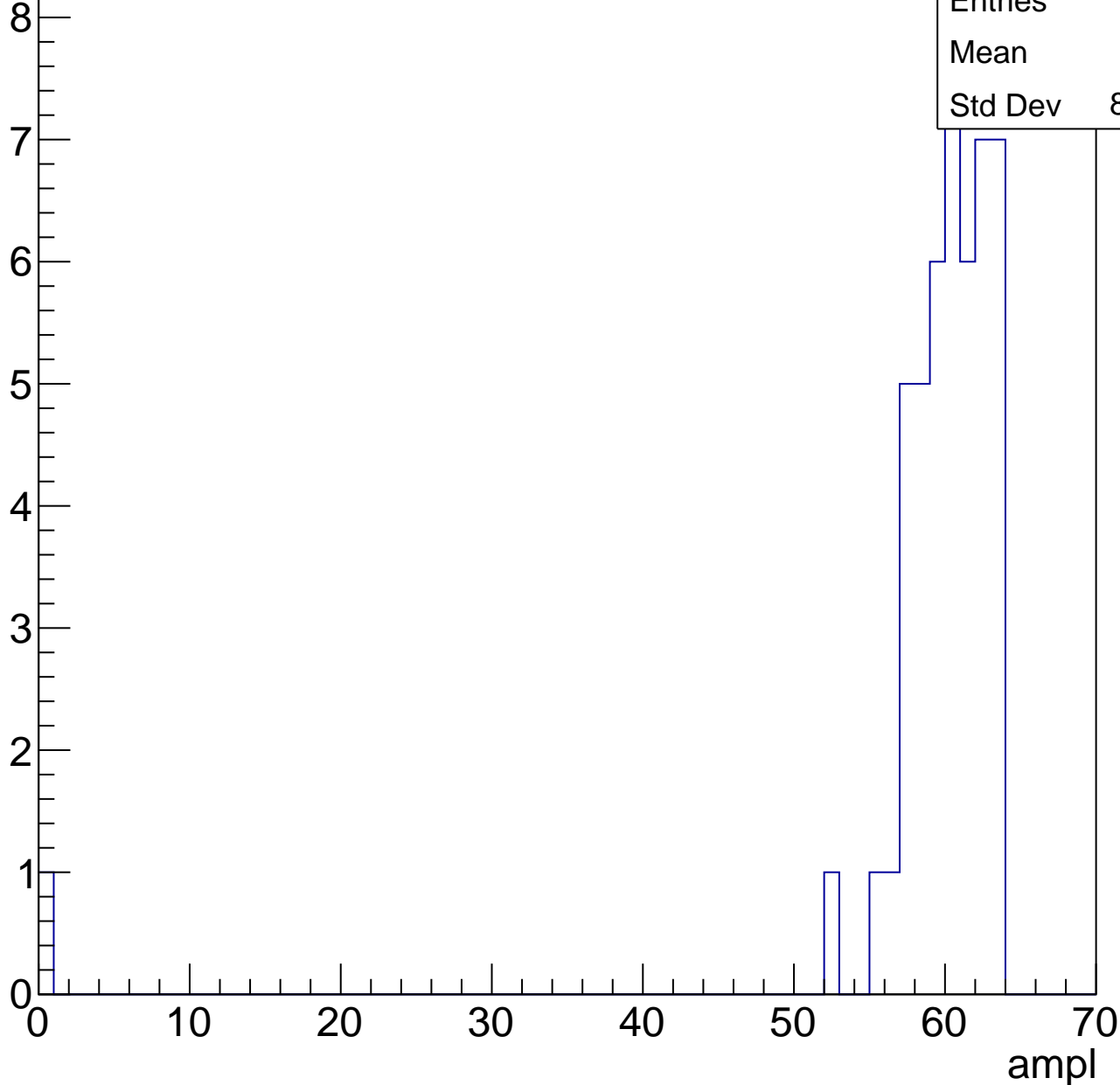


B1L103S, U7-ch57, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

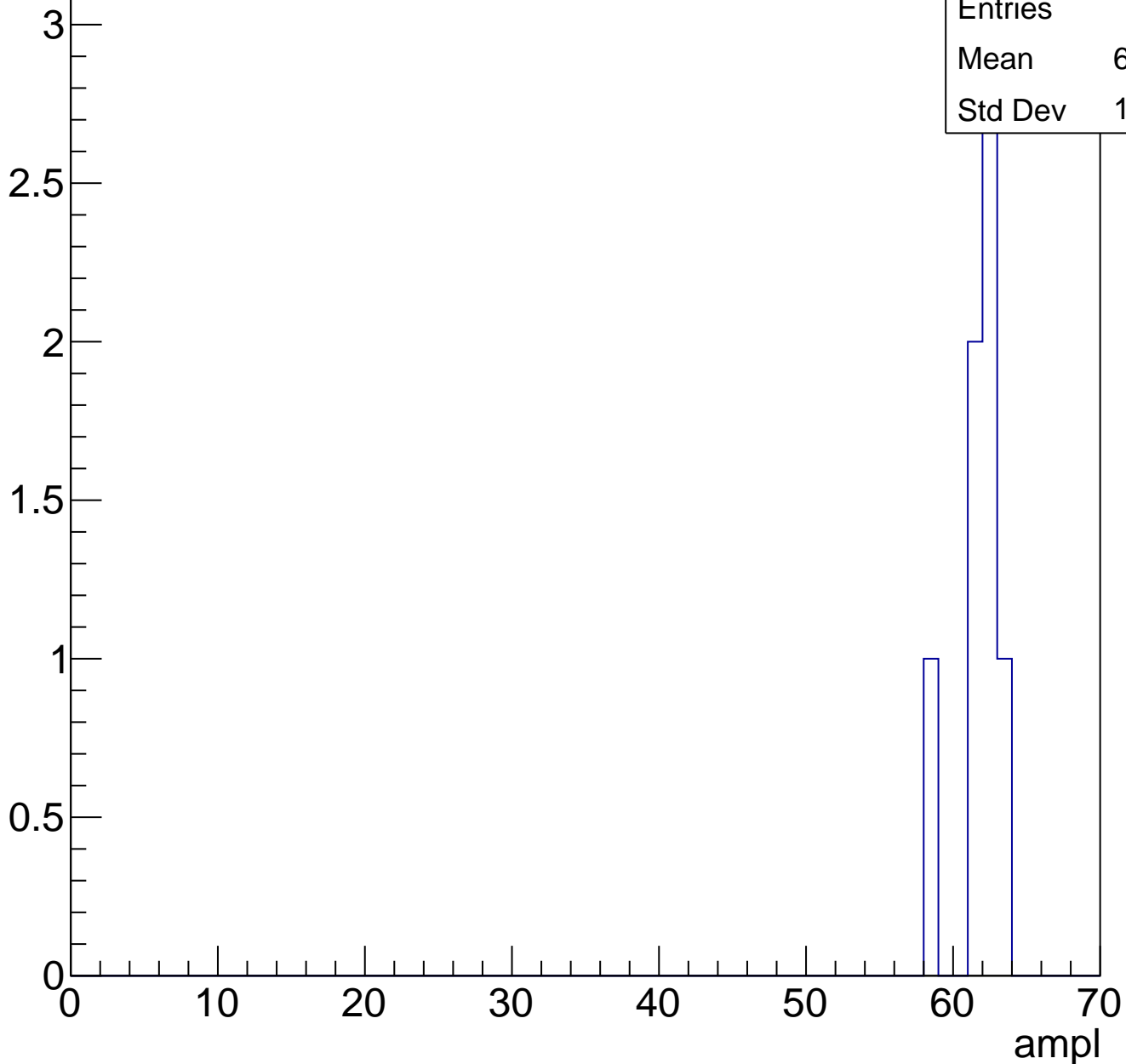
Entries	48
Mean	58.6
Std Dev	8.874



B1L103S, U7-ch57, adc6

calib_packv5_041523_1651.root, FC#0, port C2

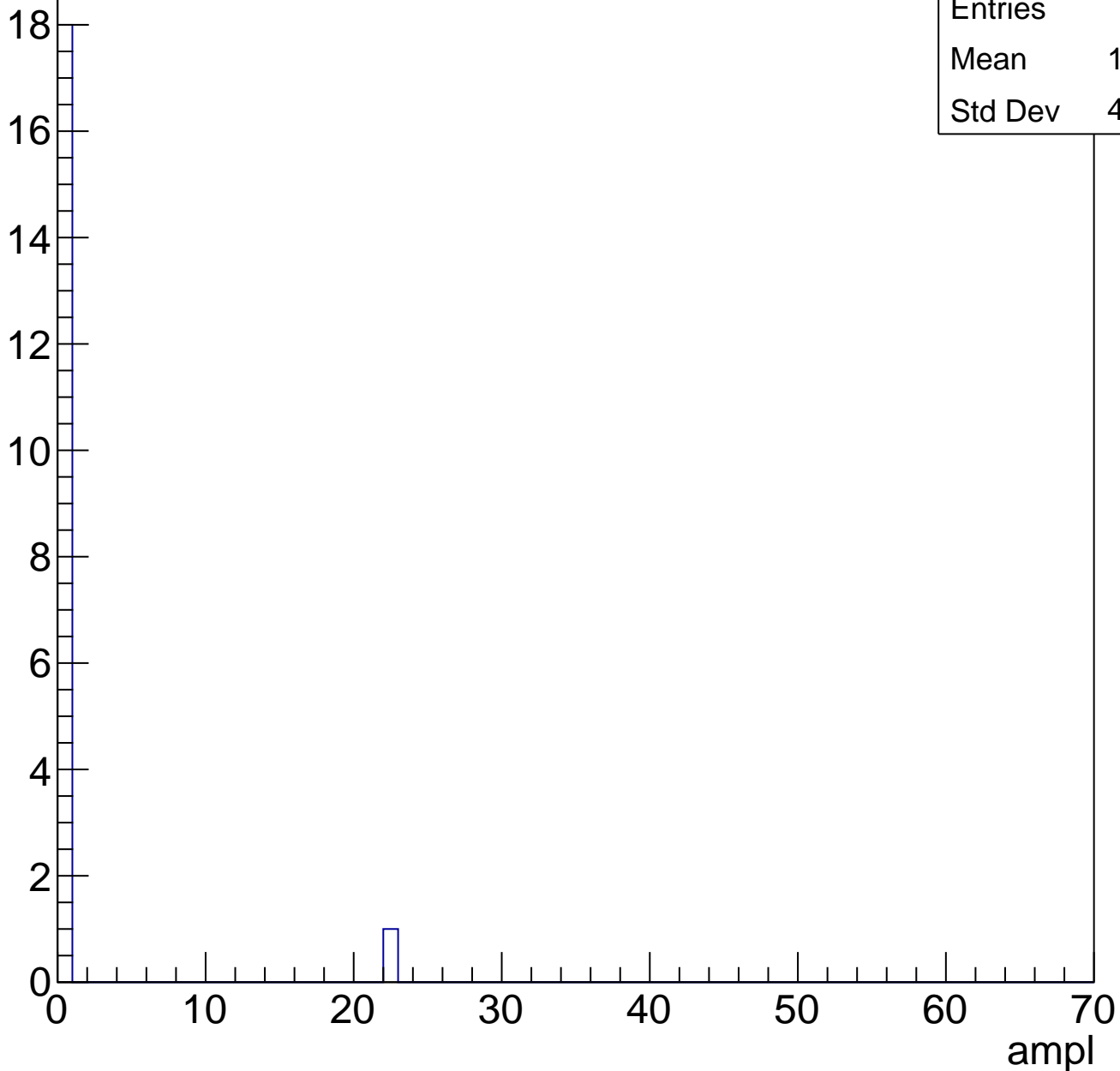
Entry



B1L103S, U7-ch57, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	19
Mean	1.158
Std Dev	4.913

B1L103S, U7-ch58, adc0

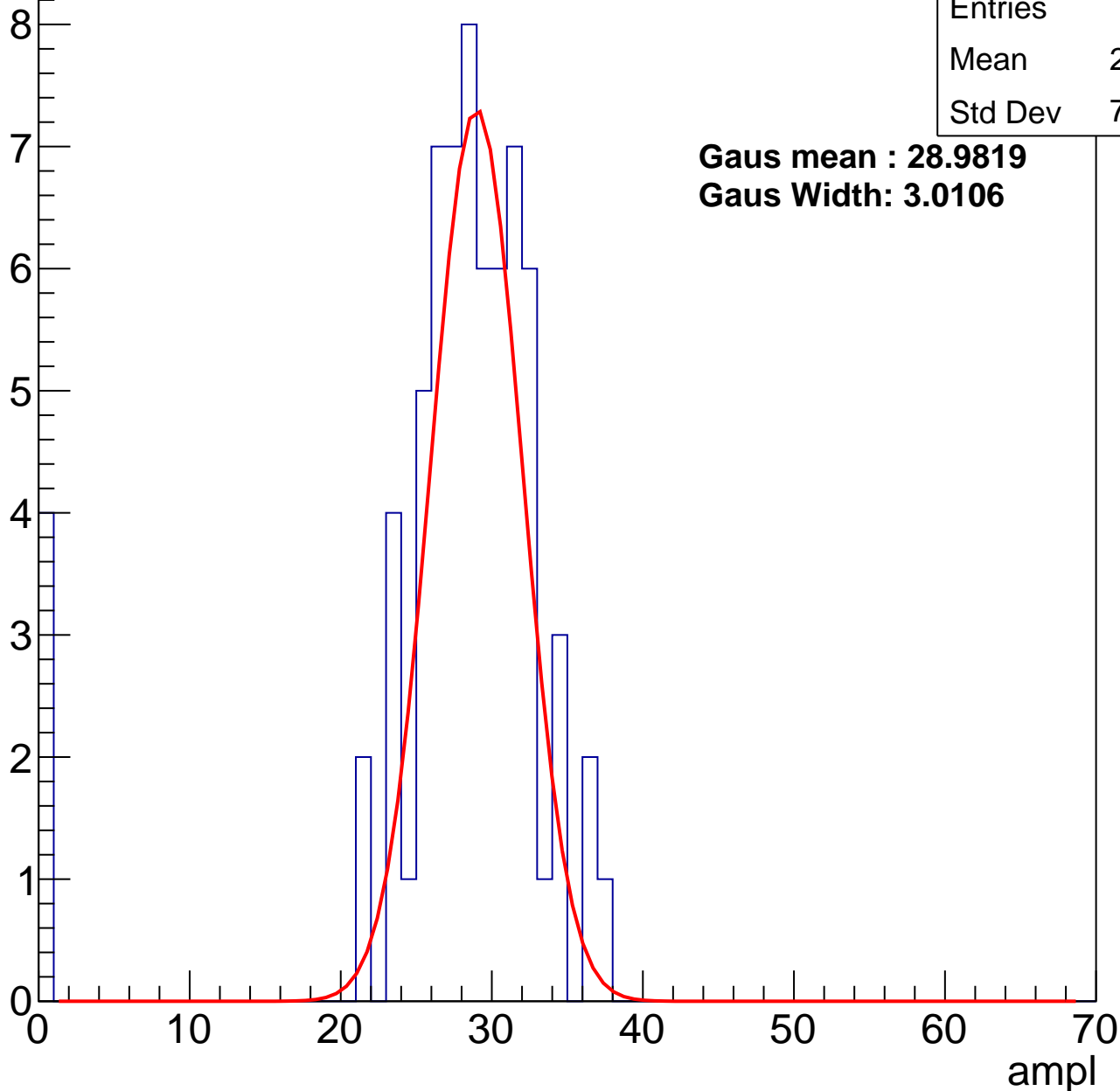
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	26.93
Std Dev	7.446

Gaus mean : 28.9819

Gaus Width: 3.0106



B1L103S, U7-ch58, adc1

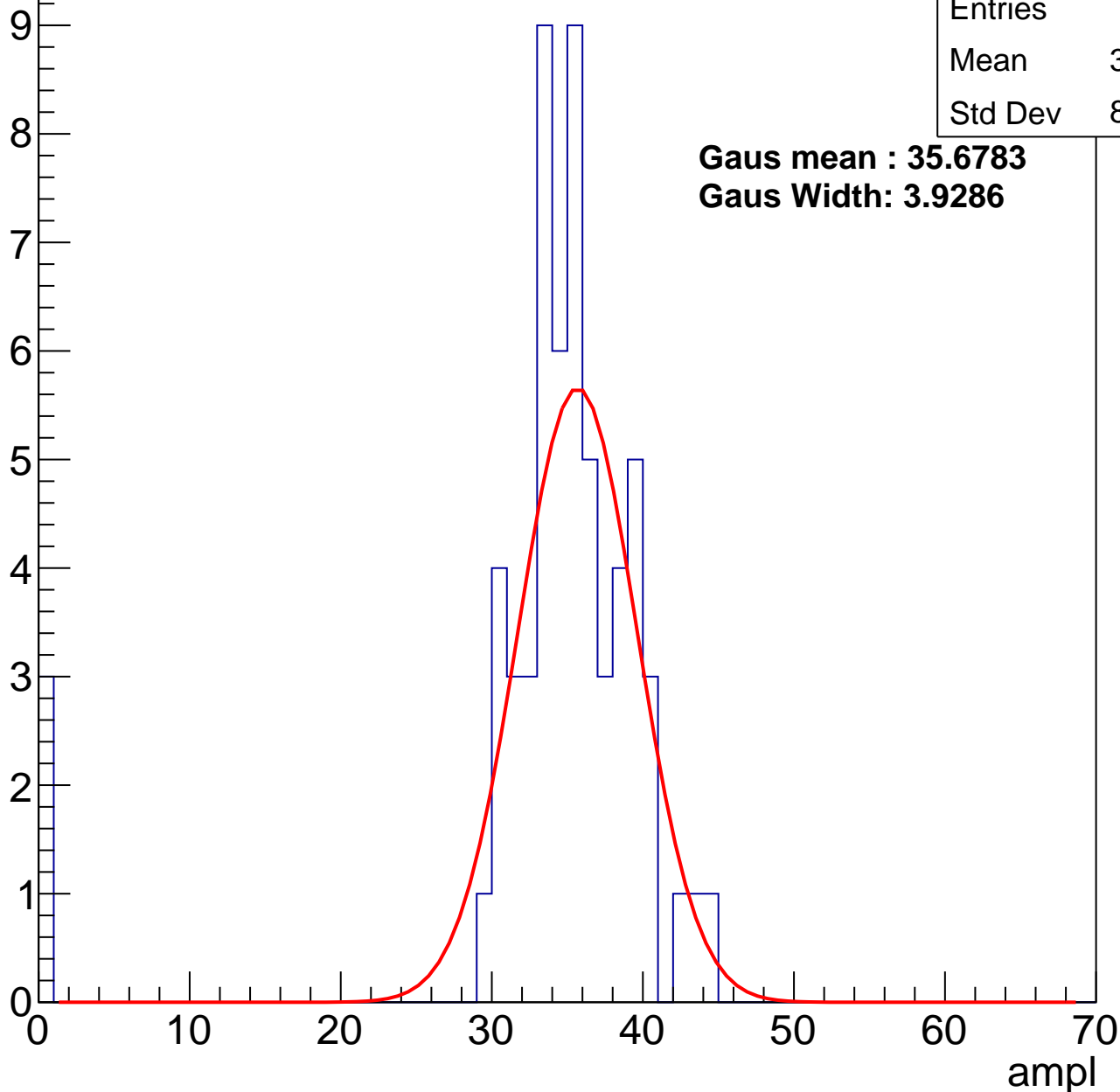
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	33.46
Std Dev	8.283

Gaus mean : 35.6783

Gaus Width: 3.9286



B1L103S, U7-ch58, adc2

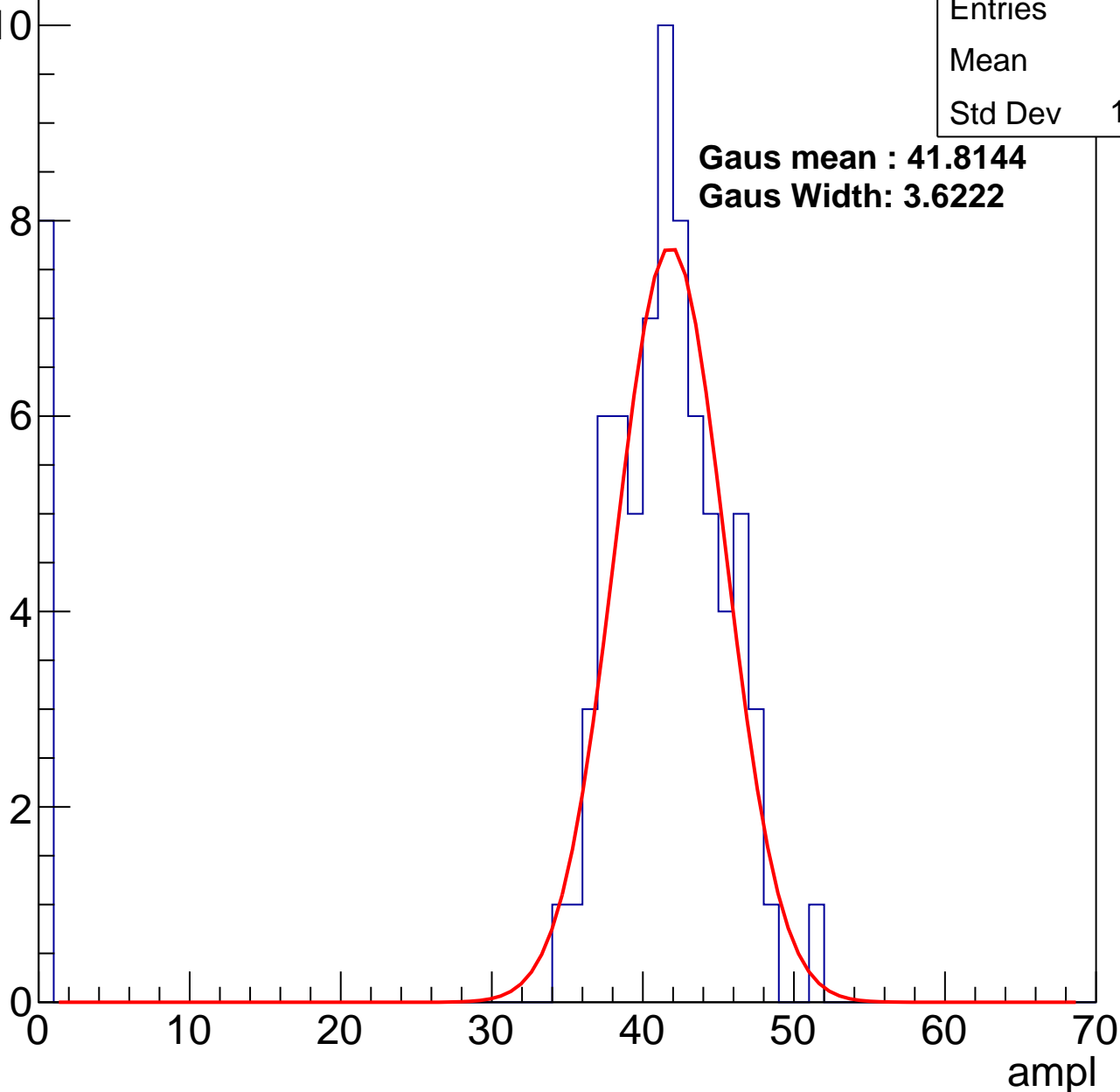
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	80
Mean	37.2
Std Dev	12.82

Gaus mean : 41.8144

Gaus Width: 3.6222

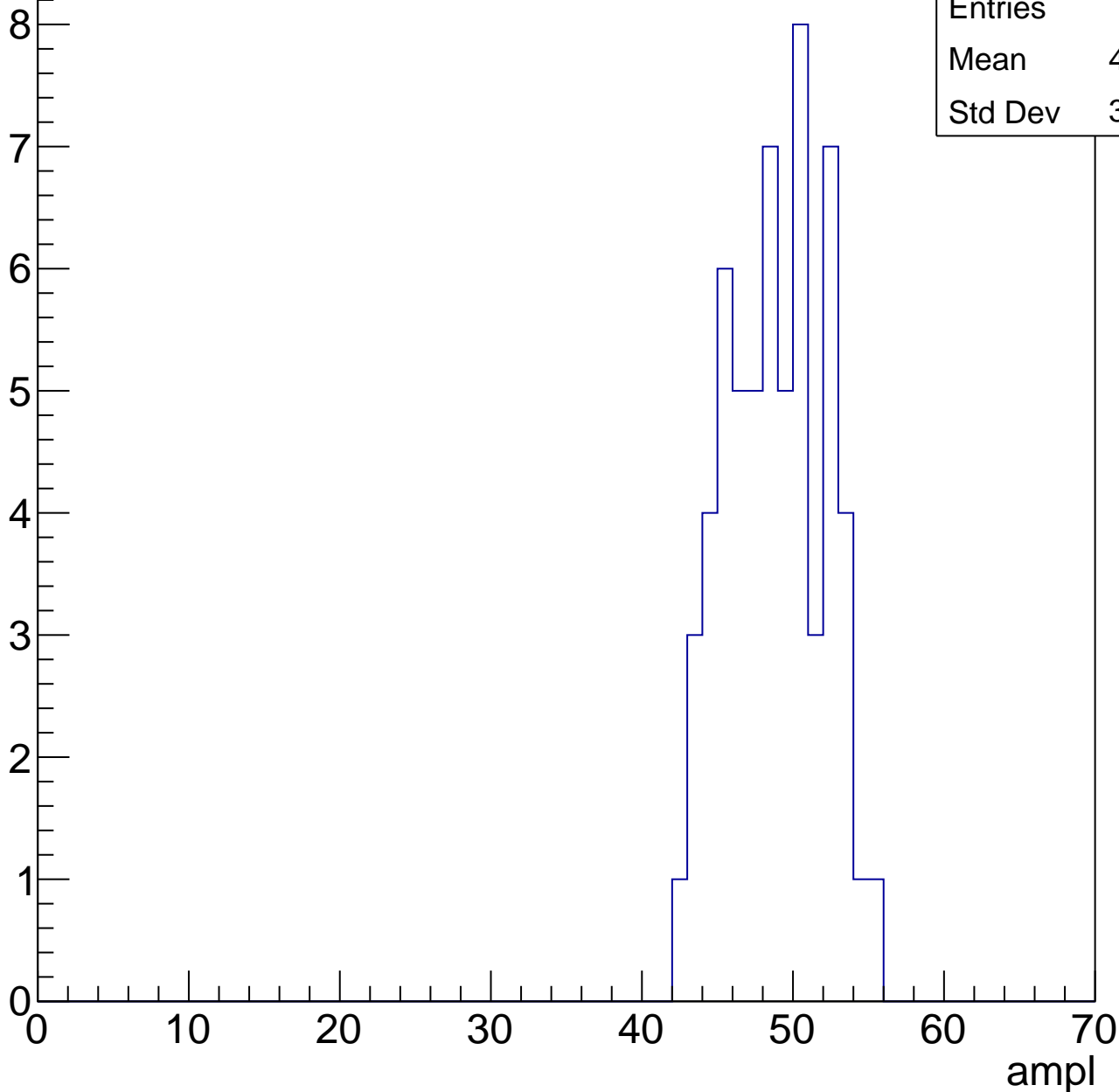


B1L103S, U7-ch58, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	48.35
Std Dev	3.182

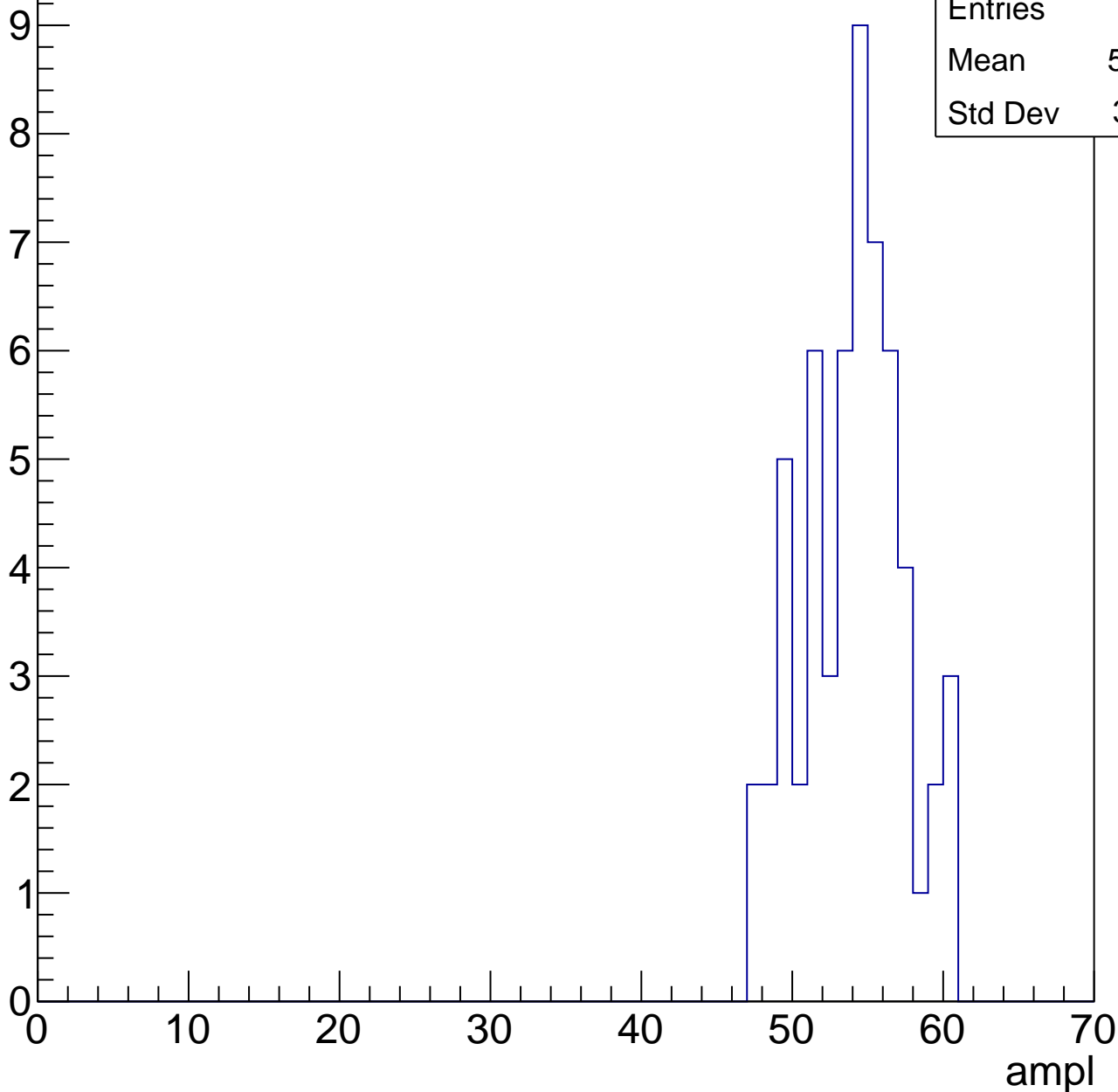


B1L103S, U7-ch58, adc4

calib_packv5_041523_1651.root, FC#0, port C2

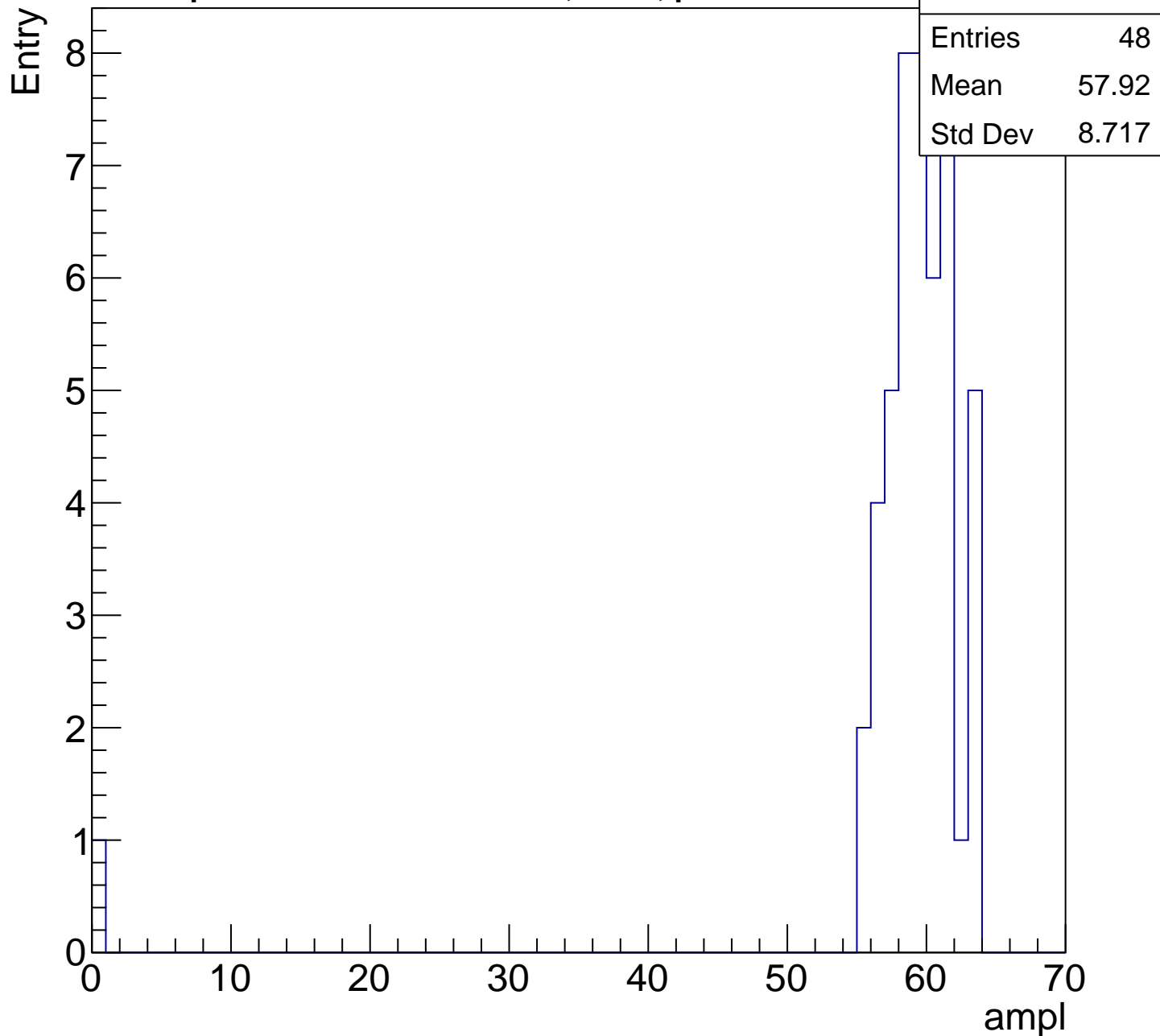
Entry

Entries	58
Mean	53.55
Std Dev	3.291



B1L103S, U7-ch58, adc5

calib_packv5_041523_1651.root, FC#0, port C2

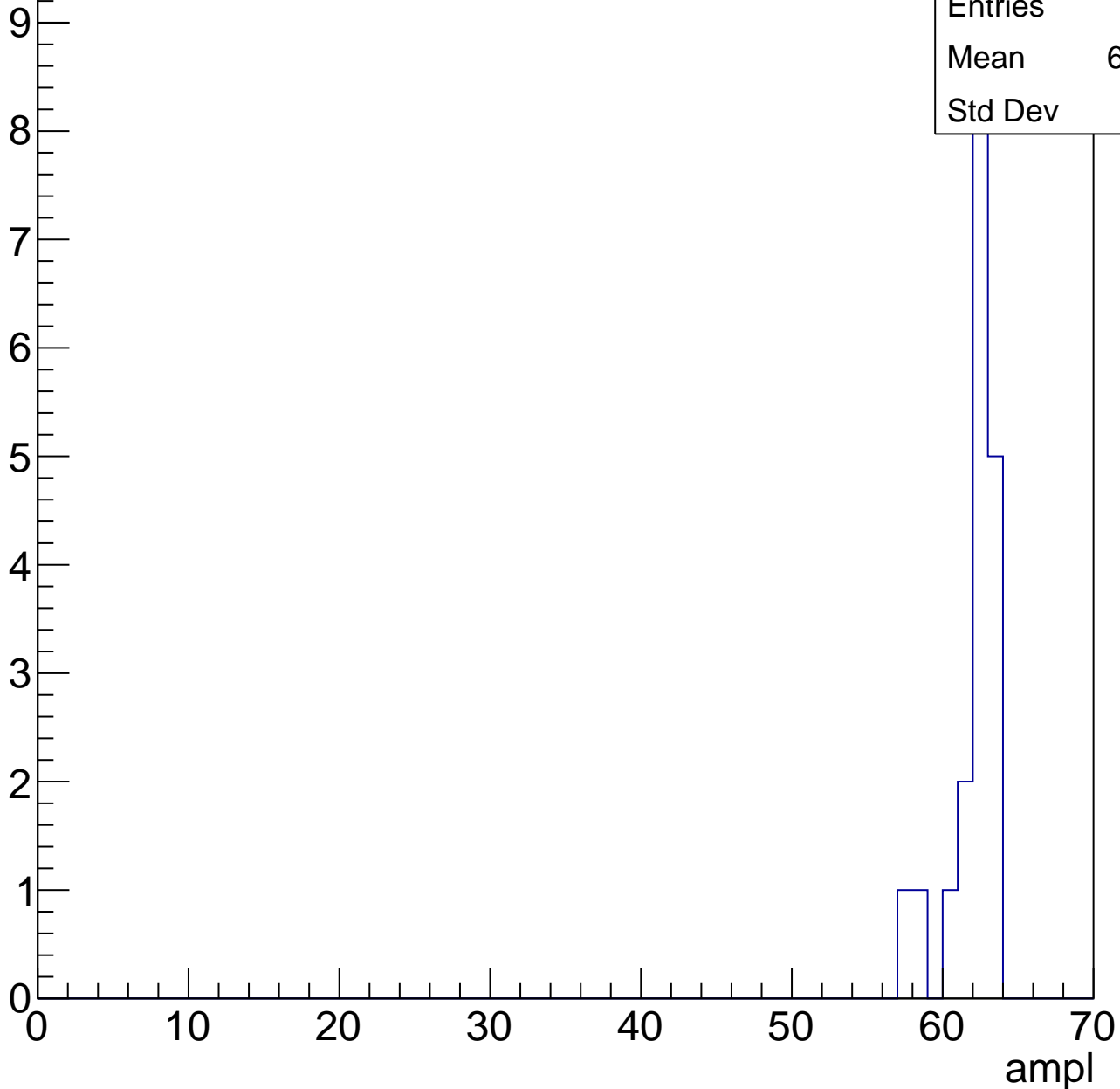


B1L103S, U7-ch58, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	19
Mean	61.58
Std Dev	1.6



B1L103S, U7-ch58, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch59, adc0

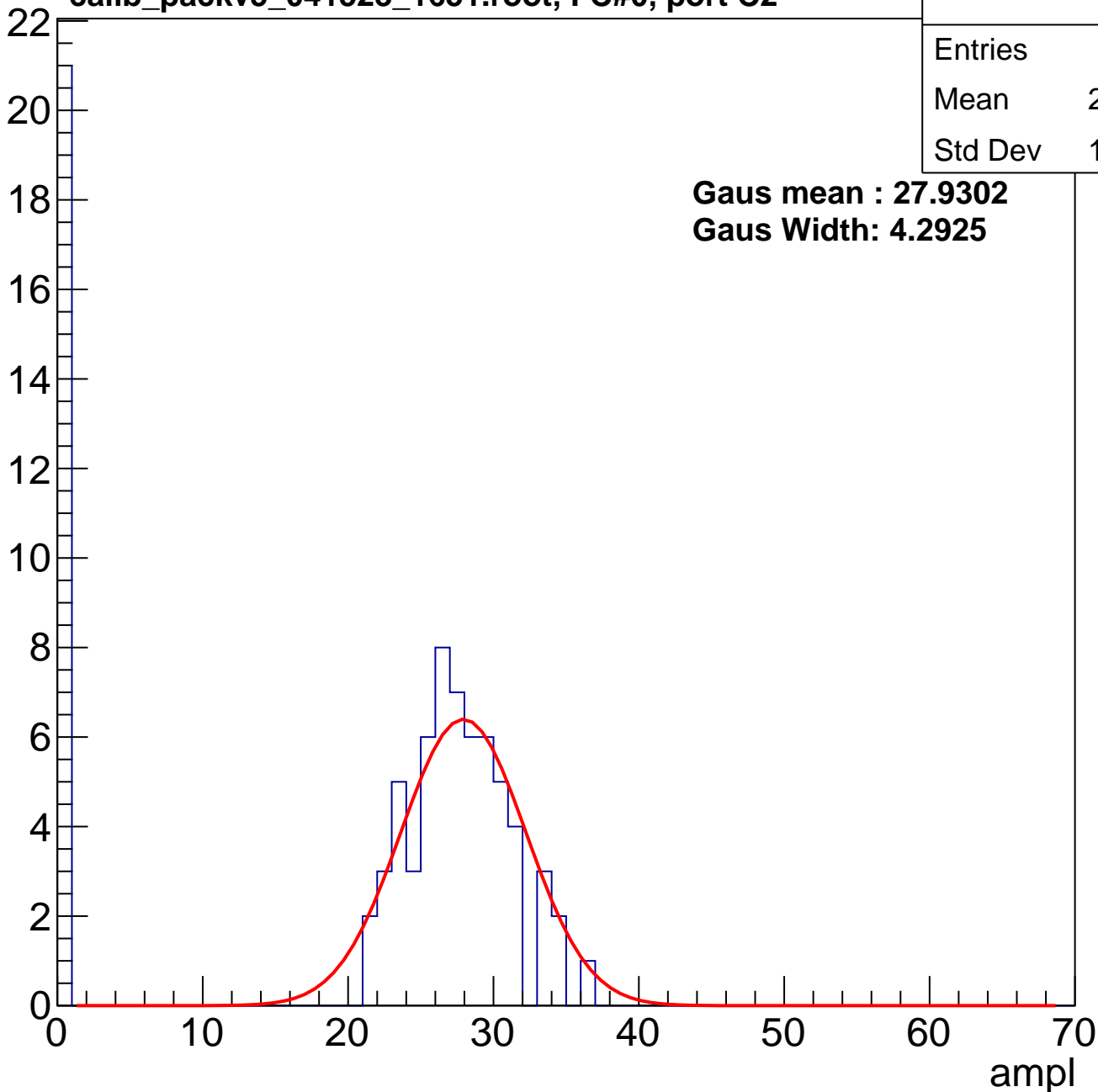
calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	20.26
Std Dev	12.24

Gaus mean : 27.9302

Gaus Width: 4.2925

Entry



B1L103S, U7-ch59, adc1

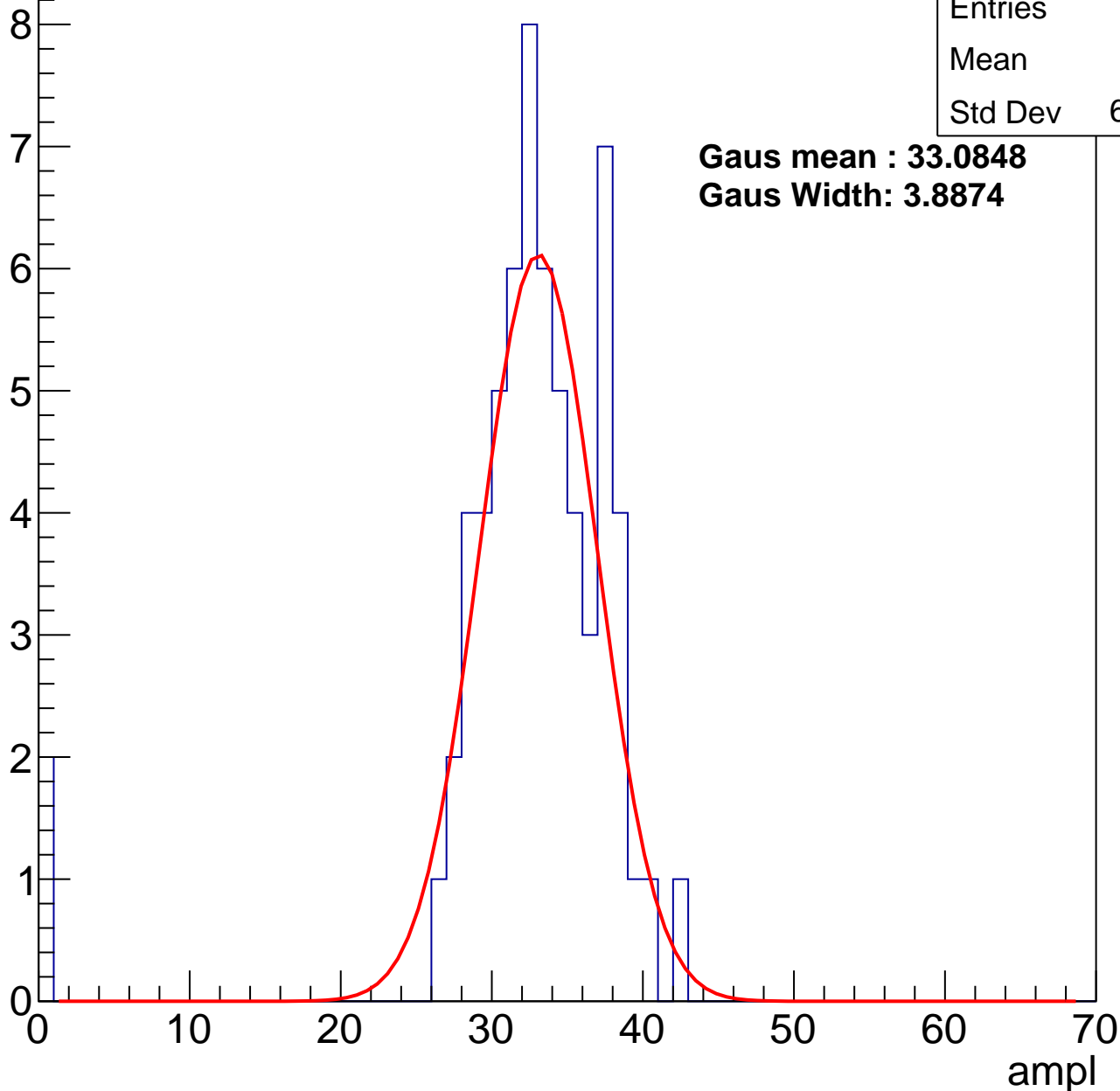
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	32
Std Dev	6.734

Gaus mean : 33.0848

Gaus Width: 3.8874



B1L103S, U7-ch59, adc2

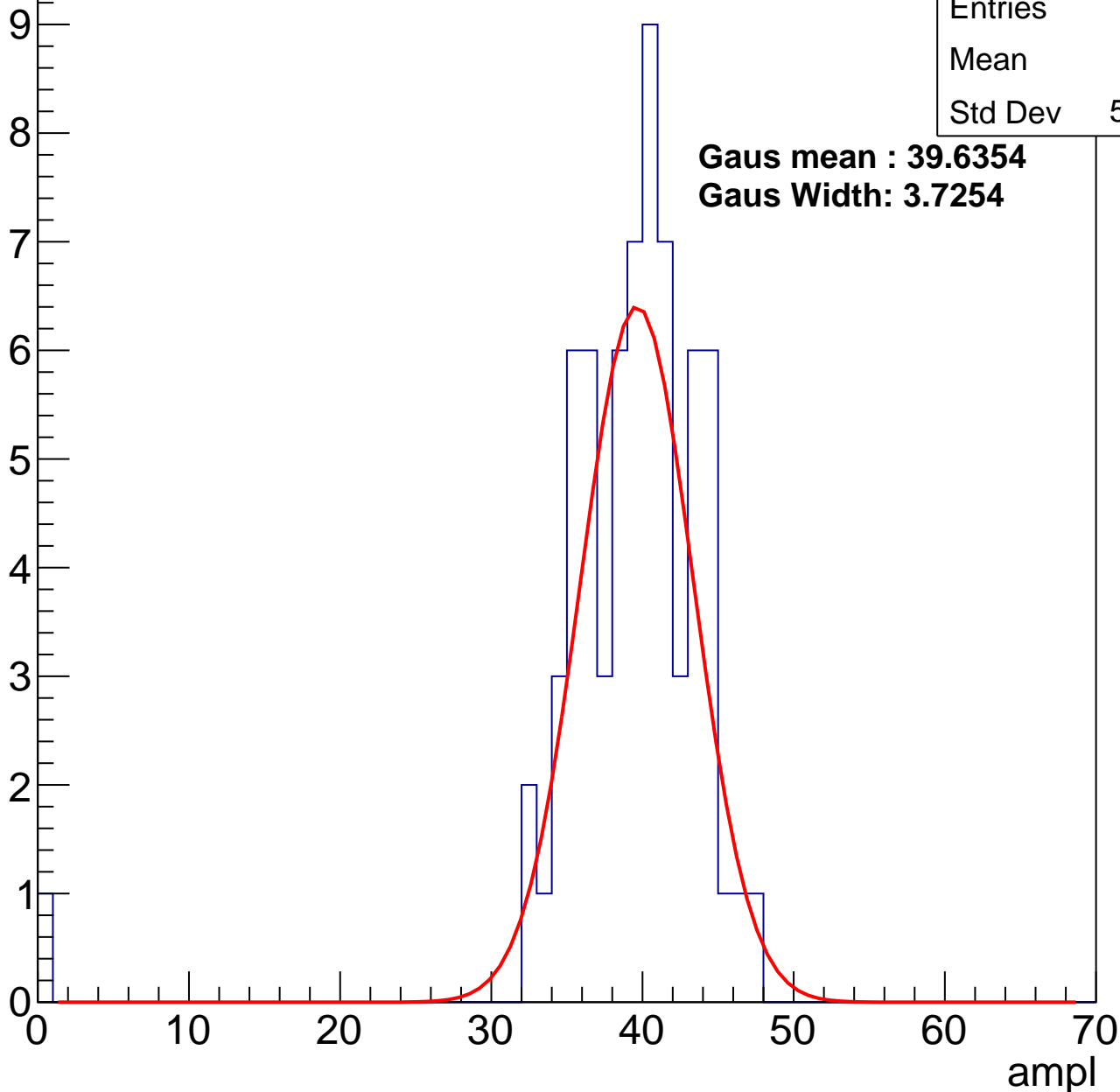
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	38.7
Std Dev	5.837

Gaus mean : 39.6354

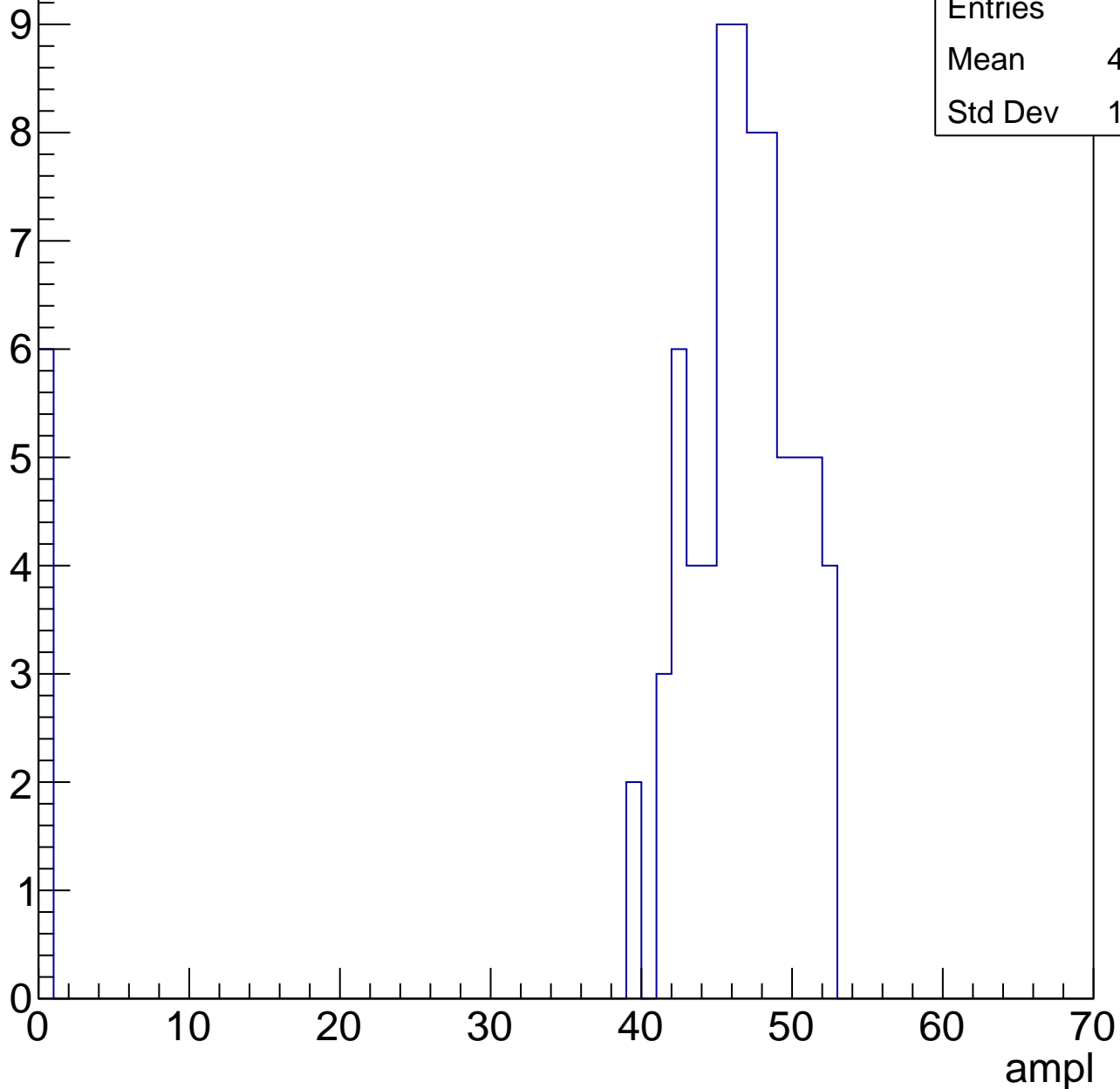
Gaus Width: 3.7254



B1L103S, U7-ch59, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry



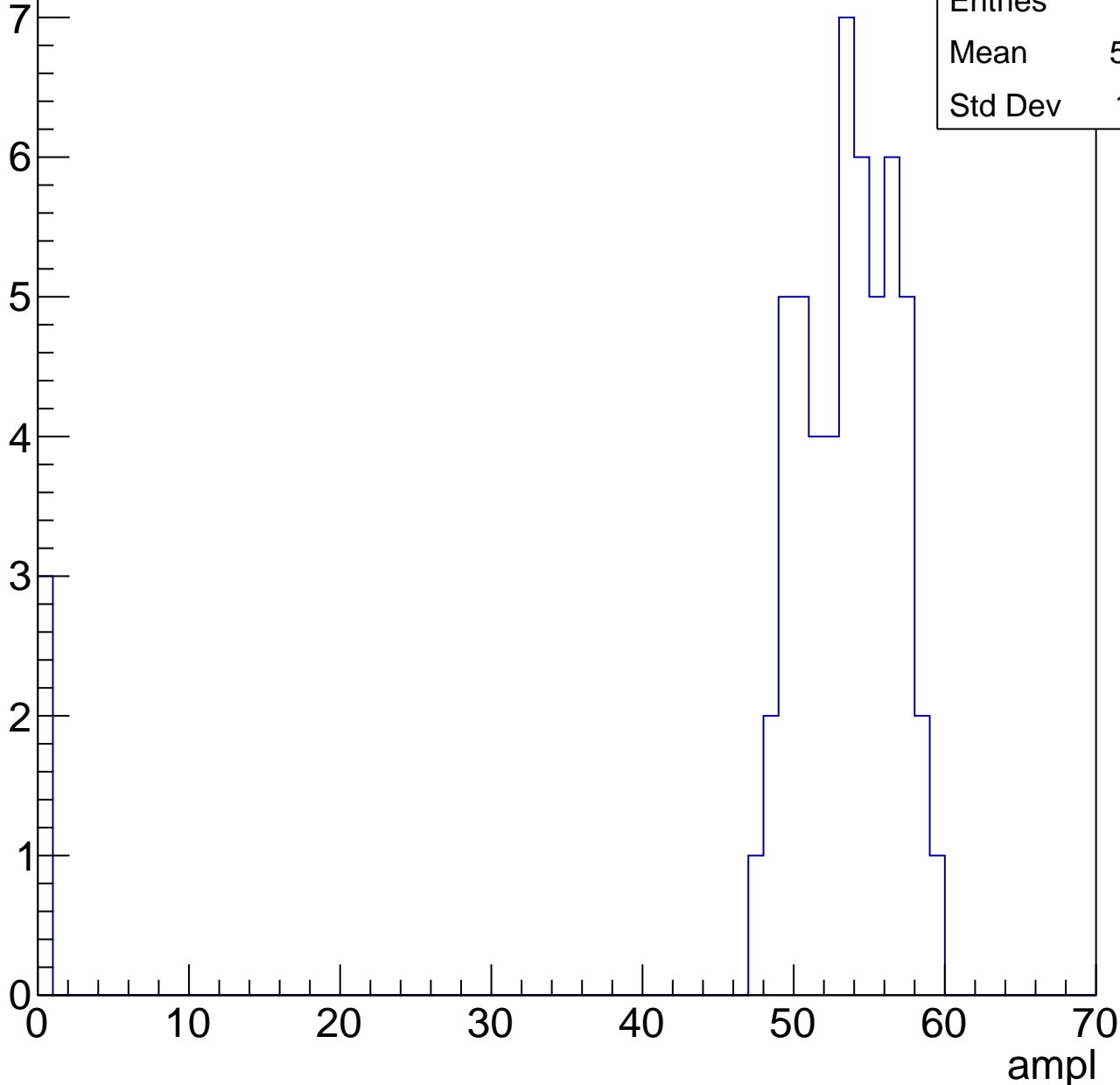
Entries	78
Mean	42.79
Std Dev	12.74

B1L103S, U7-ch59, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	50.29
Std Dev	12.31

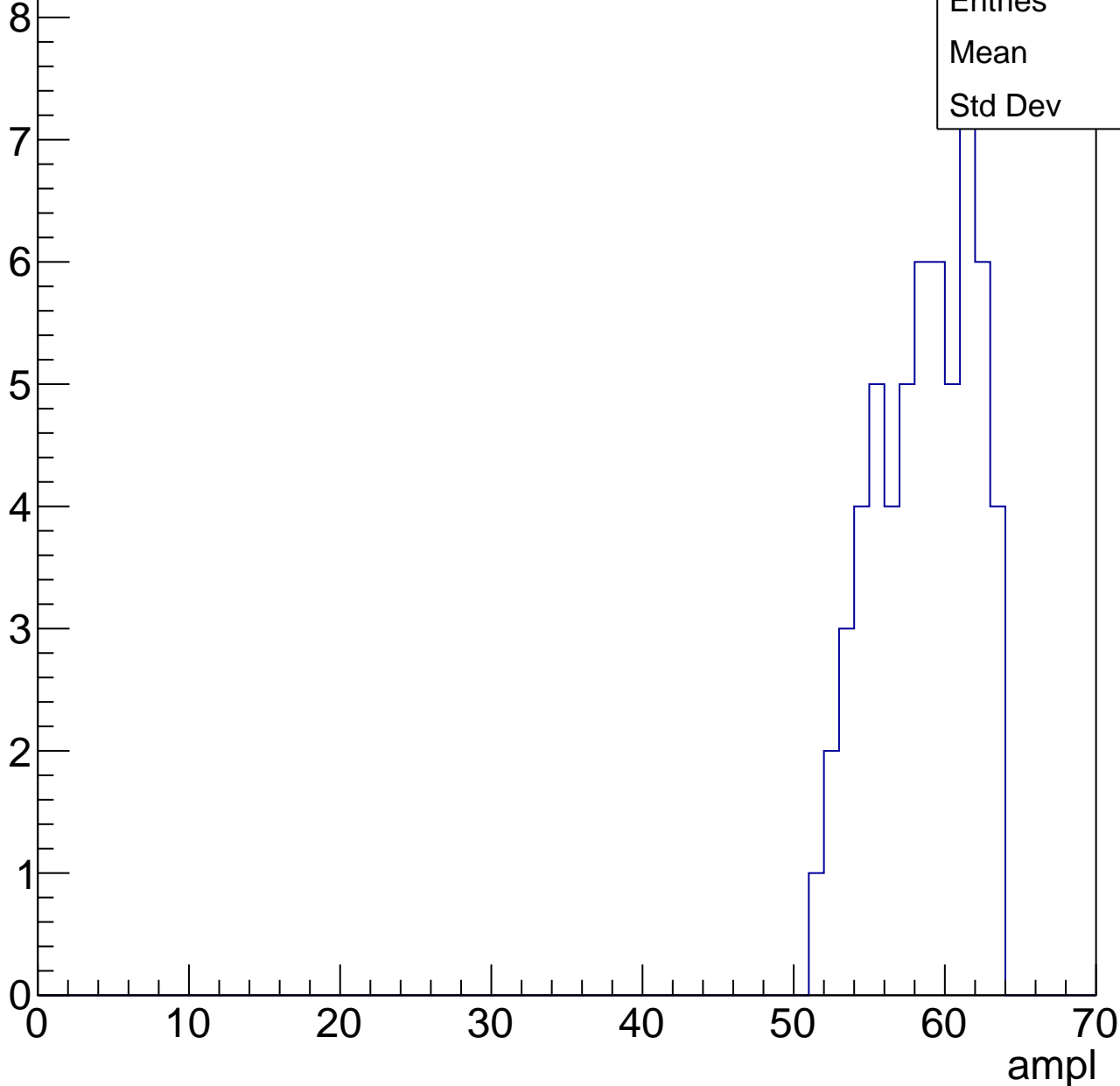


B1L103S, U7-ch59, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	58.1
Std Dev	3.24

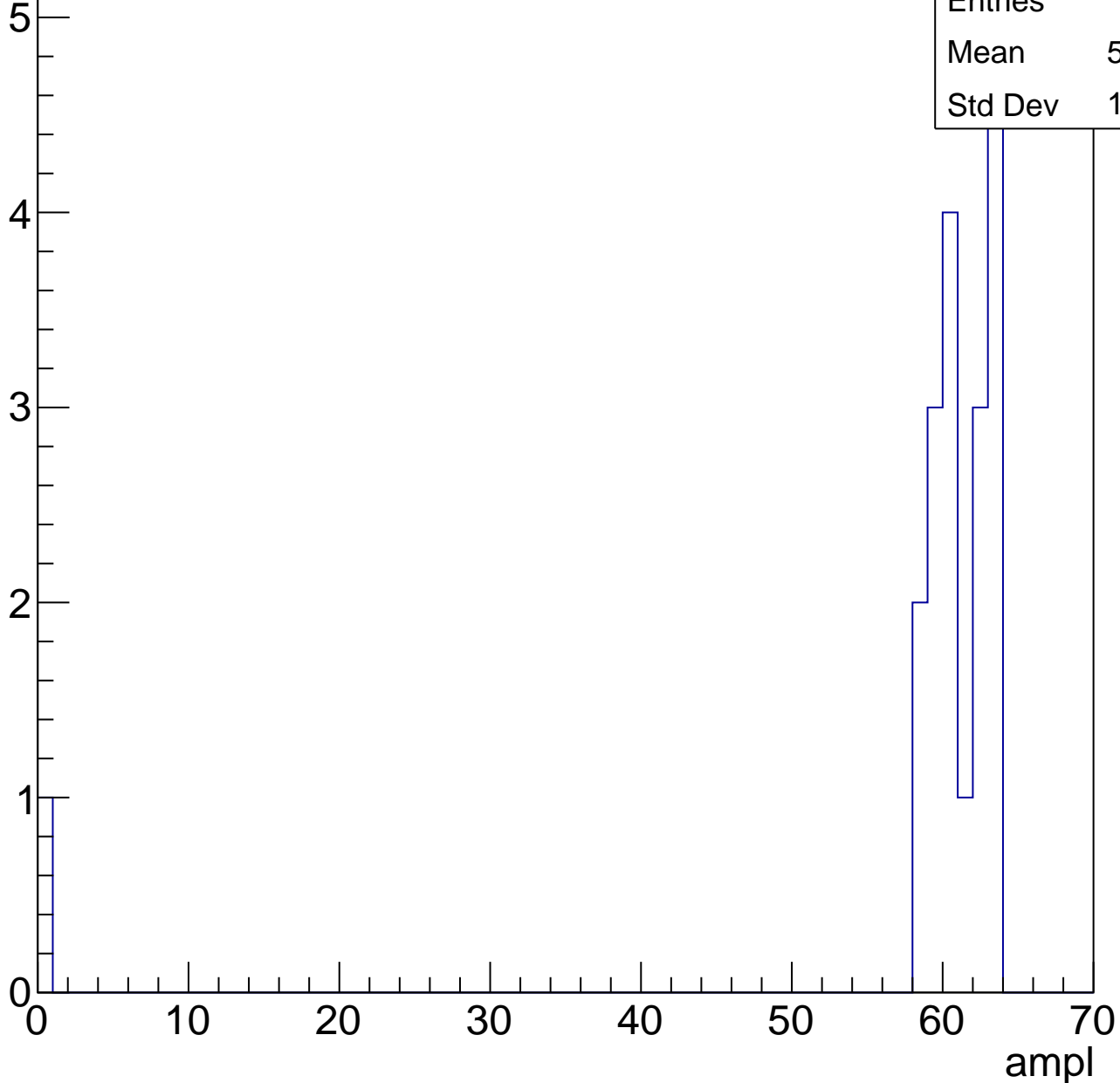


B1L103S, U7-ch59, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	19
Mean	57.63
Std Dev	13.69

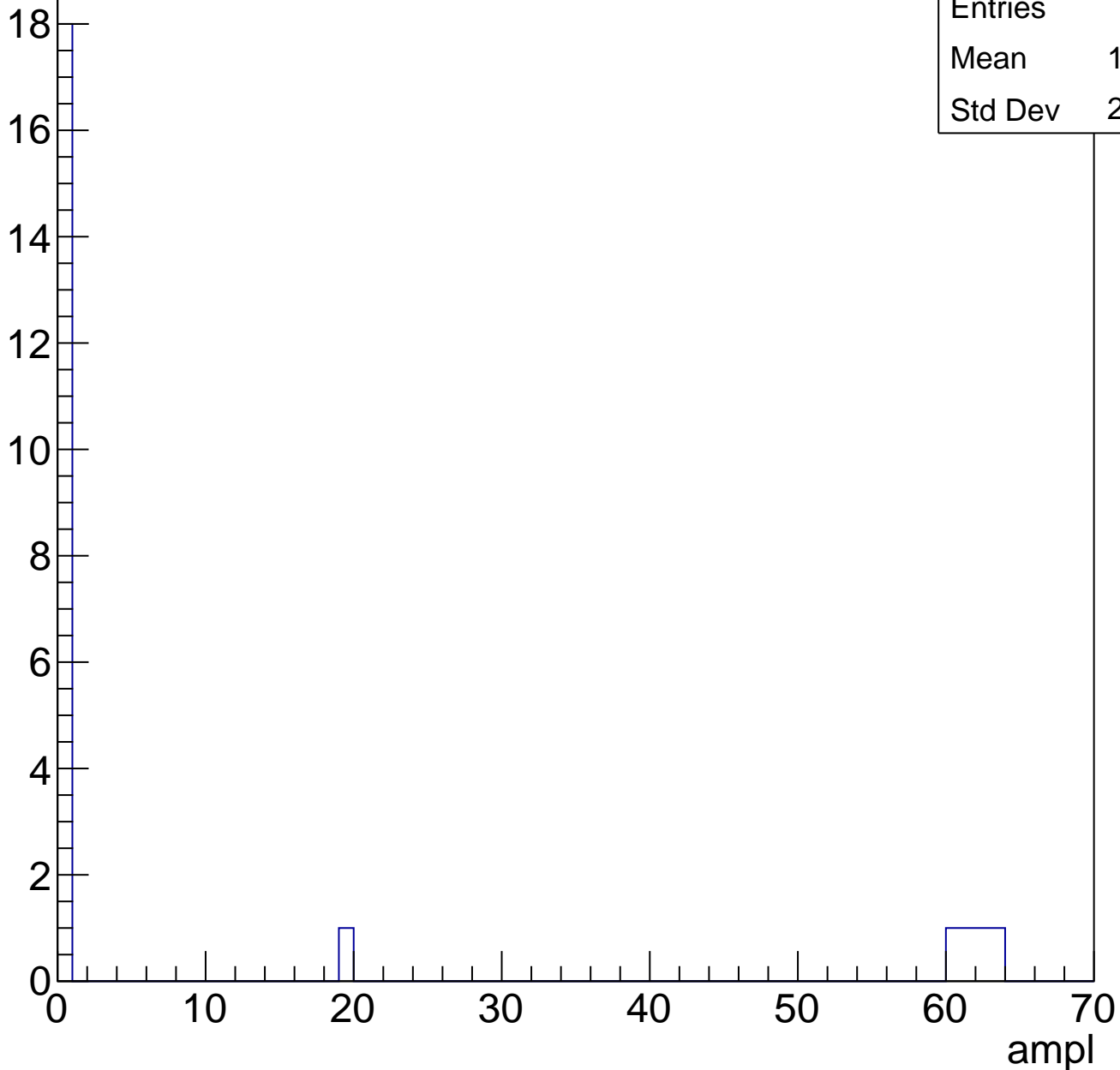


B1L103S, U7-ch59, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	23
Mean	11.52
Std Dev	23.26

Entry



B1L103S, U7-ch60, adc0

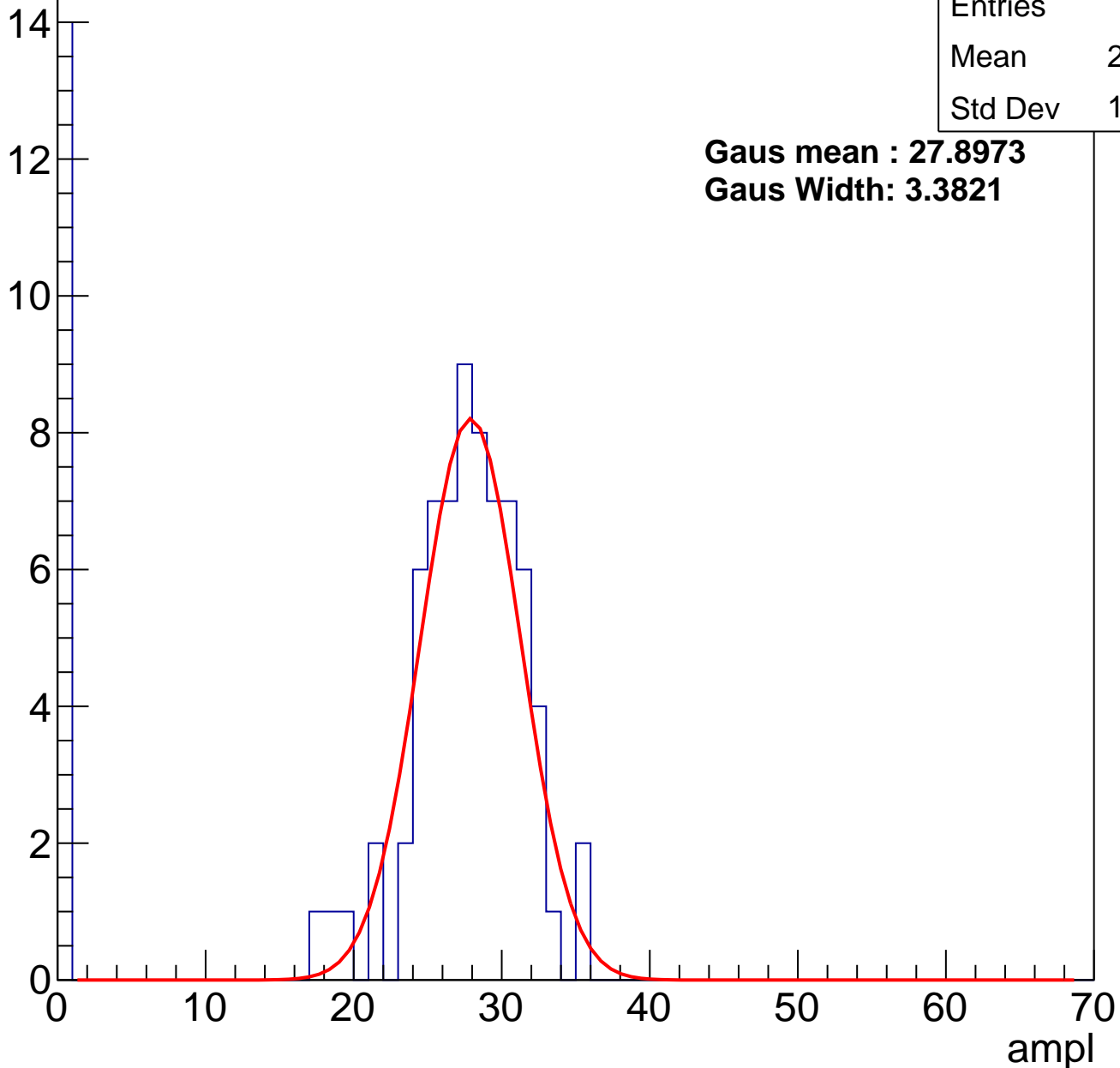
calib_packv5_041523_1651.root, FC#0, port C2

Entries	85
Mean	22.82
Std Dev	10.64

Gaus mean : 27.8973

Gaus Width: 3.3821

Entry



B1L103S, U7-ch60, adc1

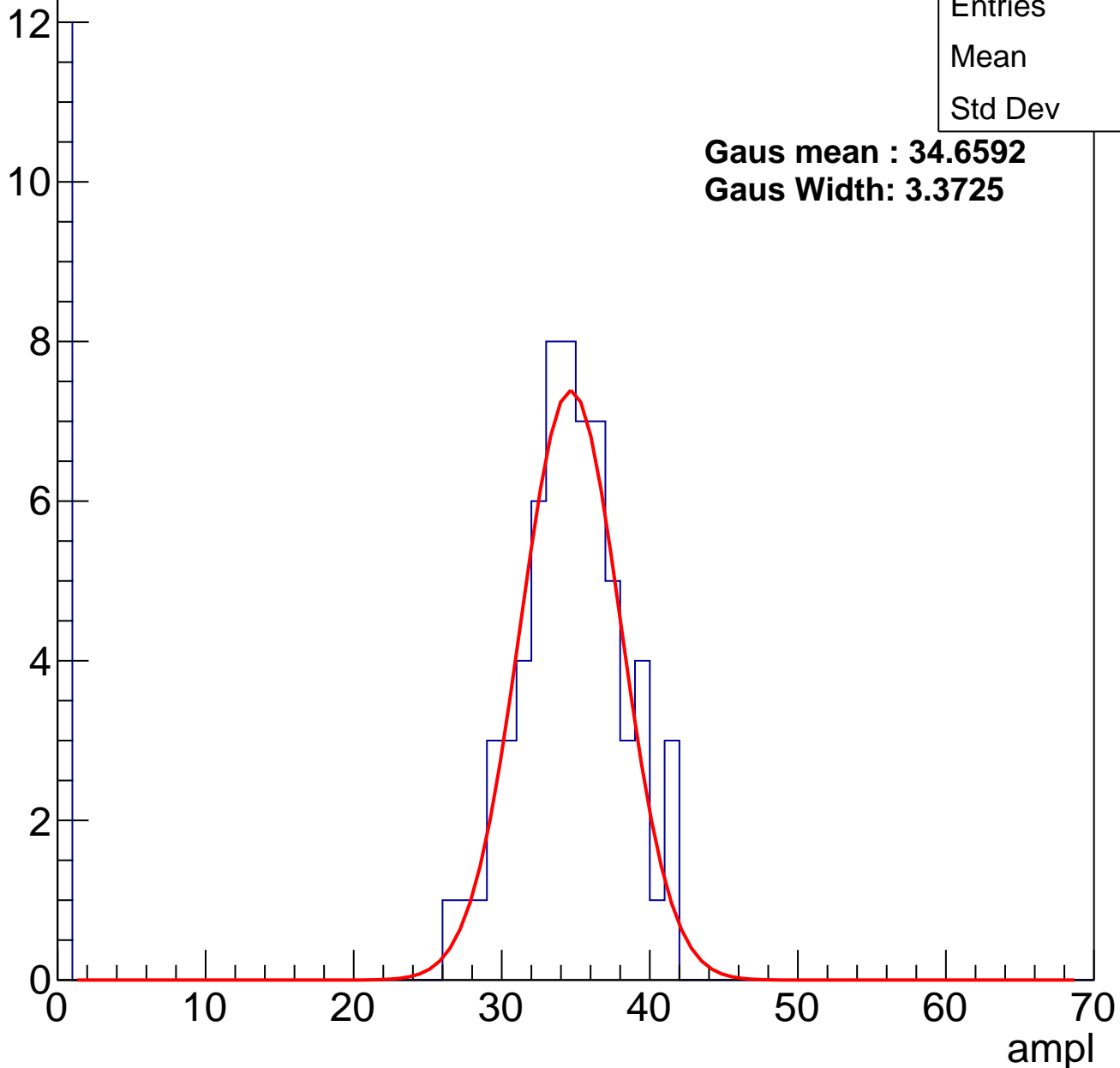
calib_packv5_041523_1651.root, FC#0, port C2

Entries	77
Mean	28.9
Std Dev	12.8

Gaus mean : 34.6592

Gaus Width: 3.3725

Entry



B1L103S, U7-ch60, adc2

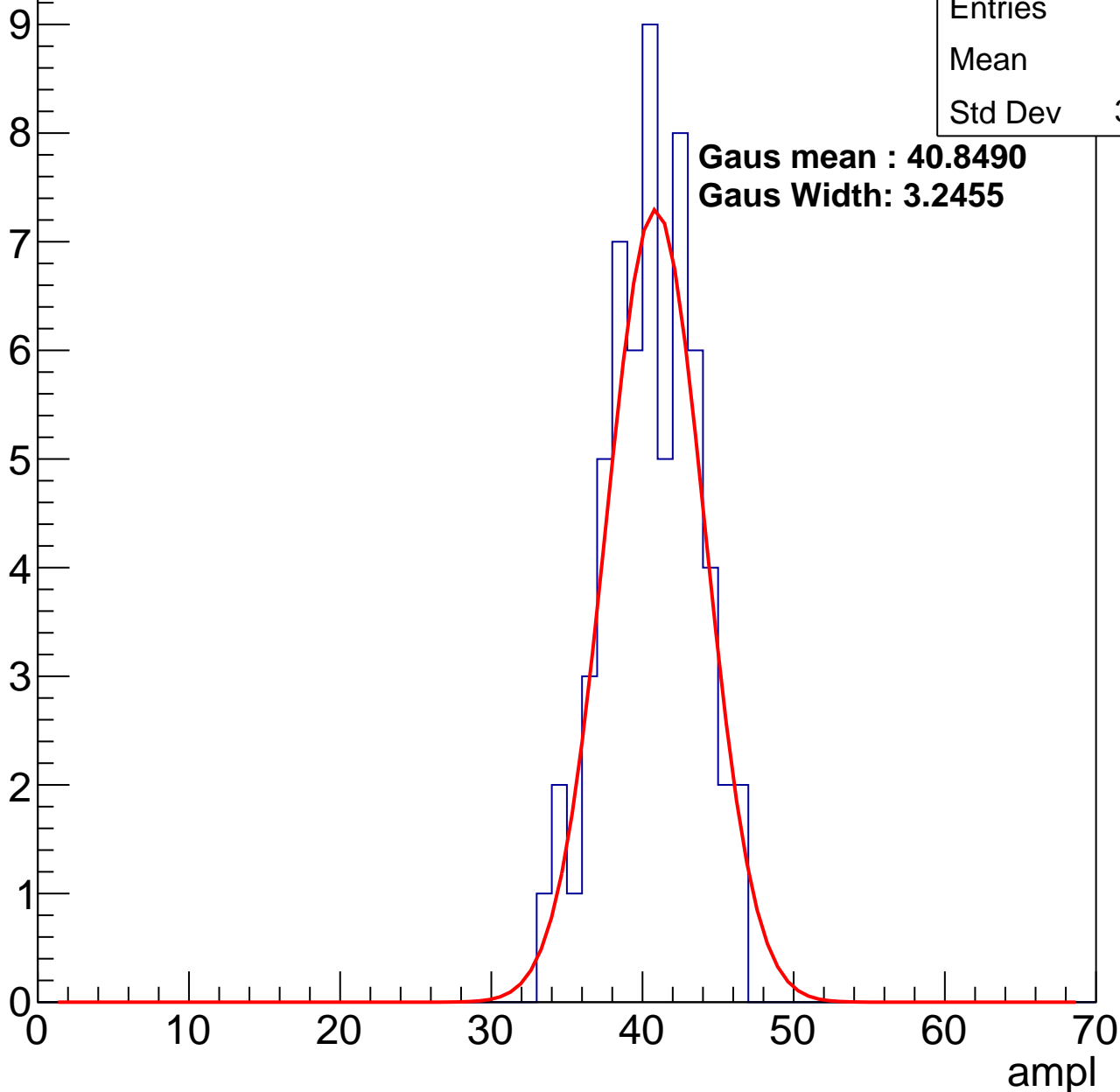
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	40.1
Std Dev	3.001

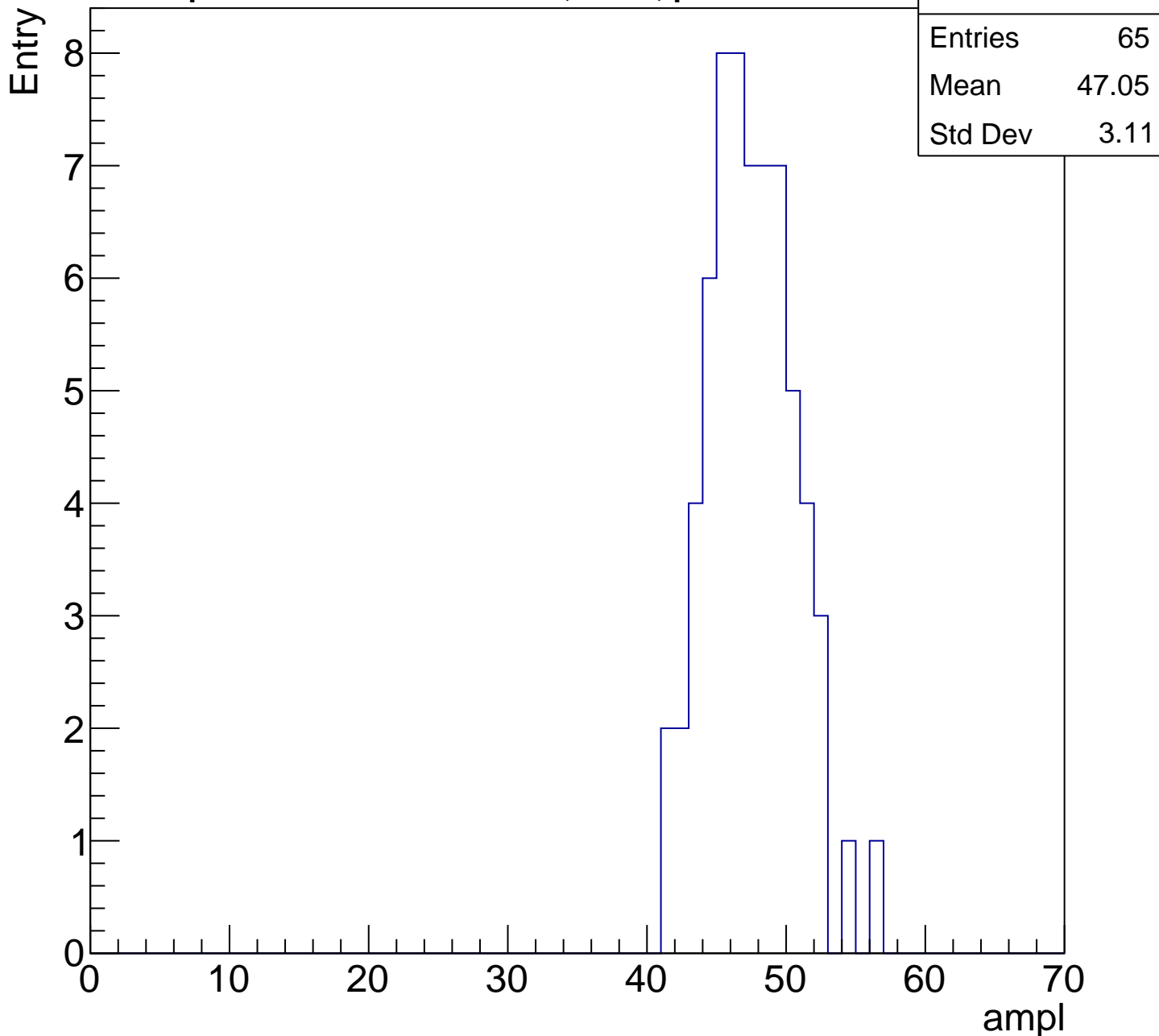
Gaus mean : 40.8490

Gaus Width: 3.2455



B1L103S, U7-ch60, adc3

calib_packv5_041523_1651.root, FC#0, port C2

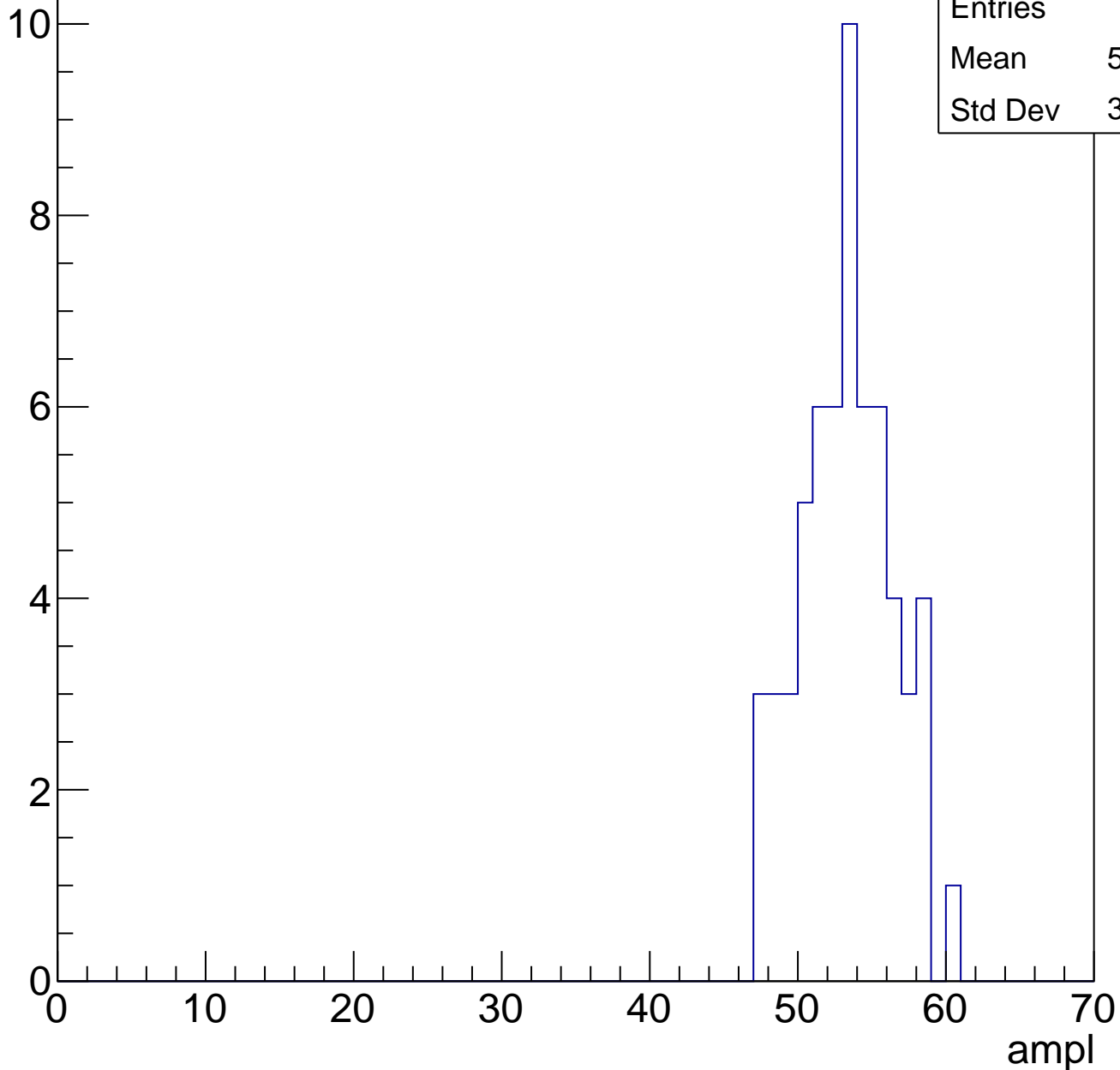


B1L103S, U7-ch60, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	60
Mean	52.85
Std Dev	3.076

Entry

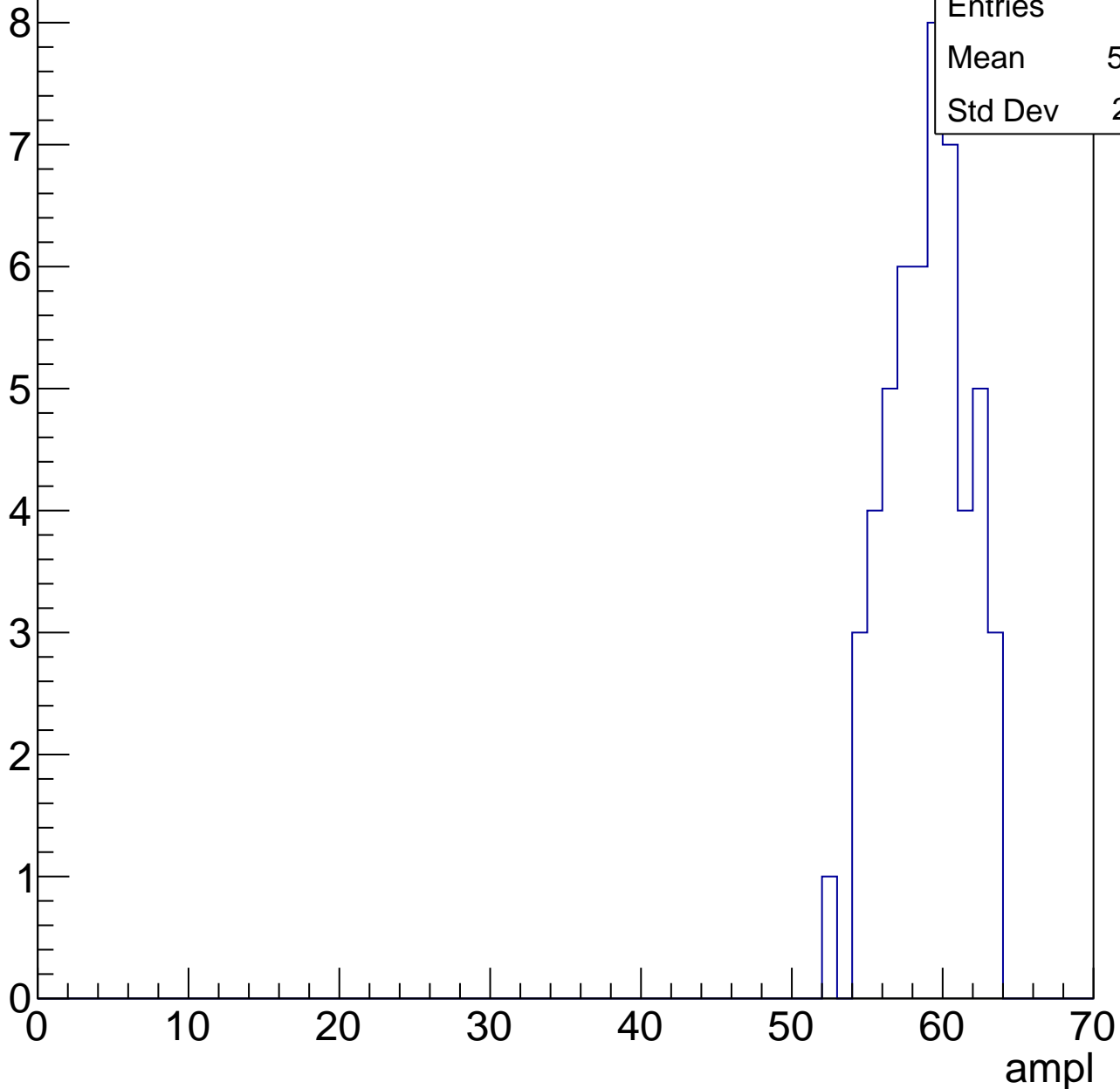


B1L103S, U7-ch60, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	58.44
Std Dev	2.641

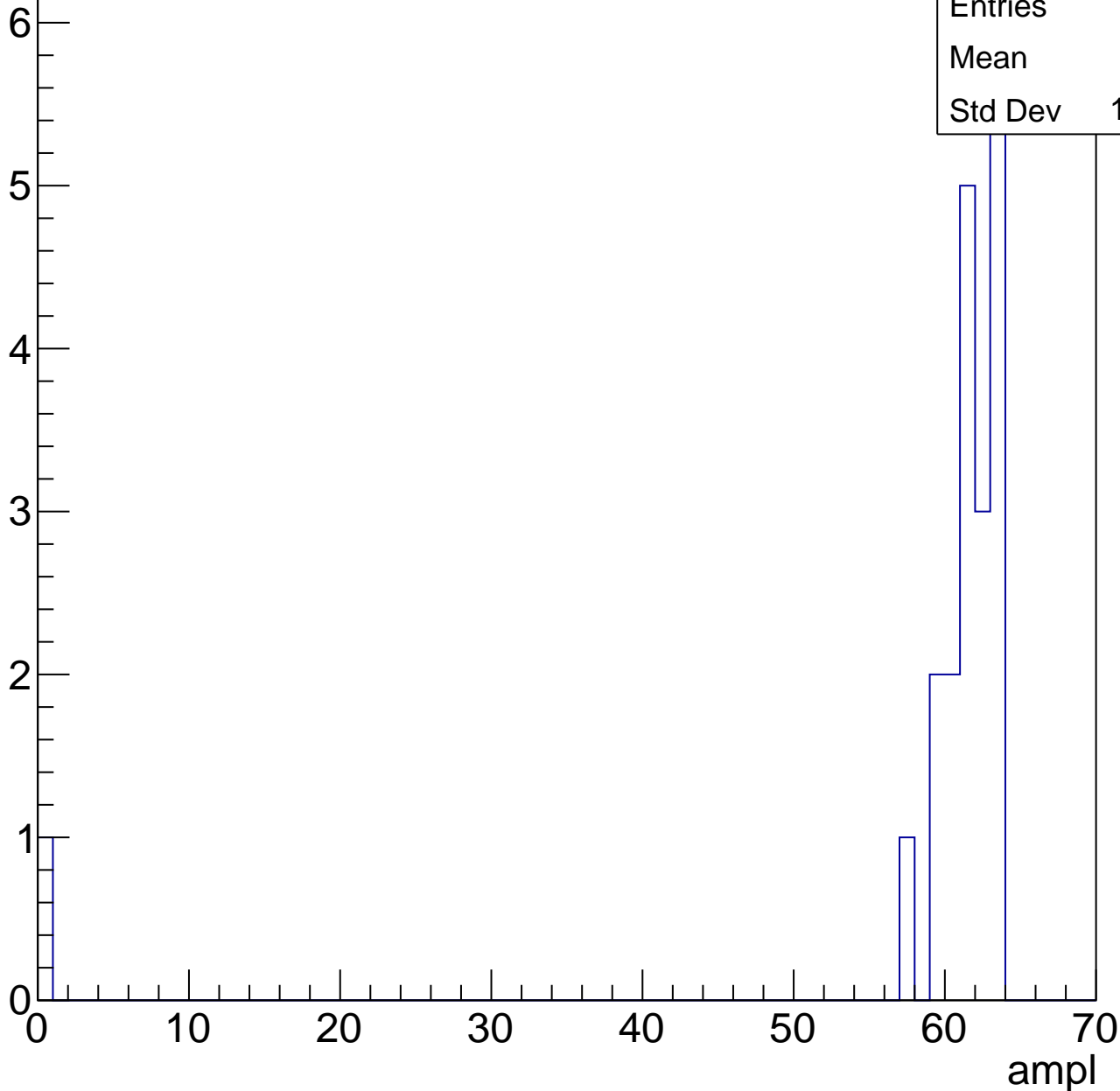


B1L103S, U7-ch60, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	20
Mean	58.2
Std Dev	13.45

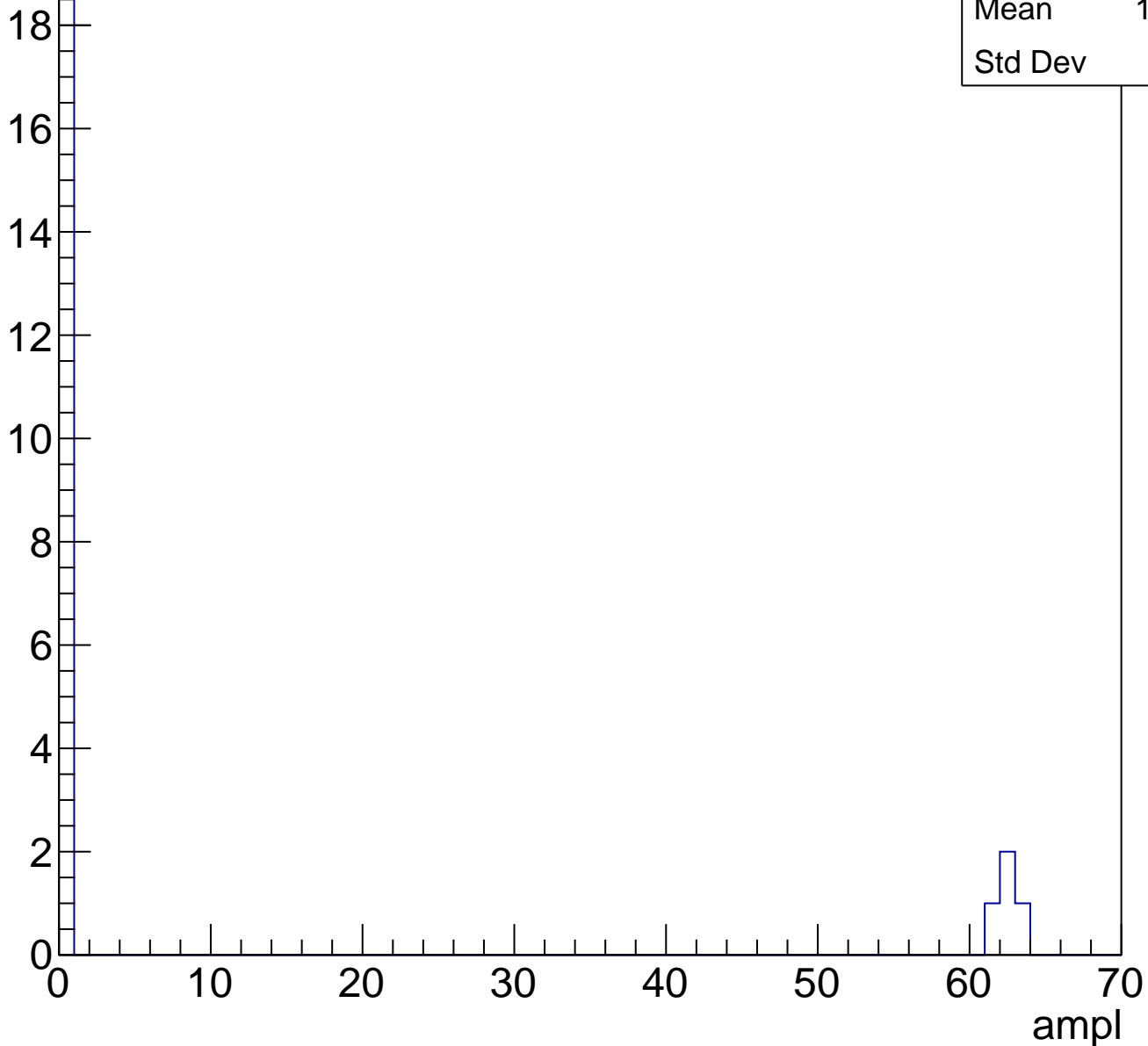


B1L103S, U7-ch60, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	23
Mean	10.78
Std Dev	23.5

Entry



B1L103S, U7-ch61, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	76
Mean	27.68
Std Dev	7.994

Gaus mean : 30.1347

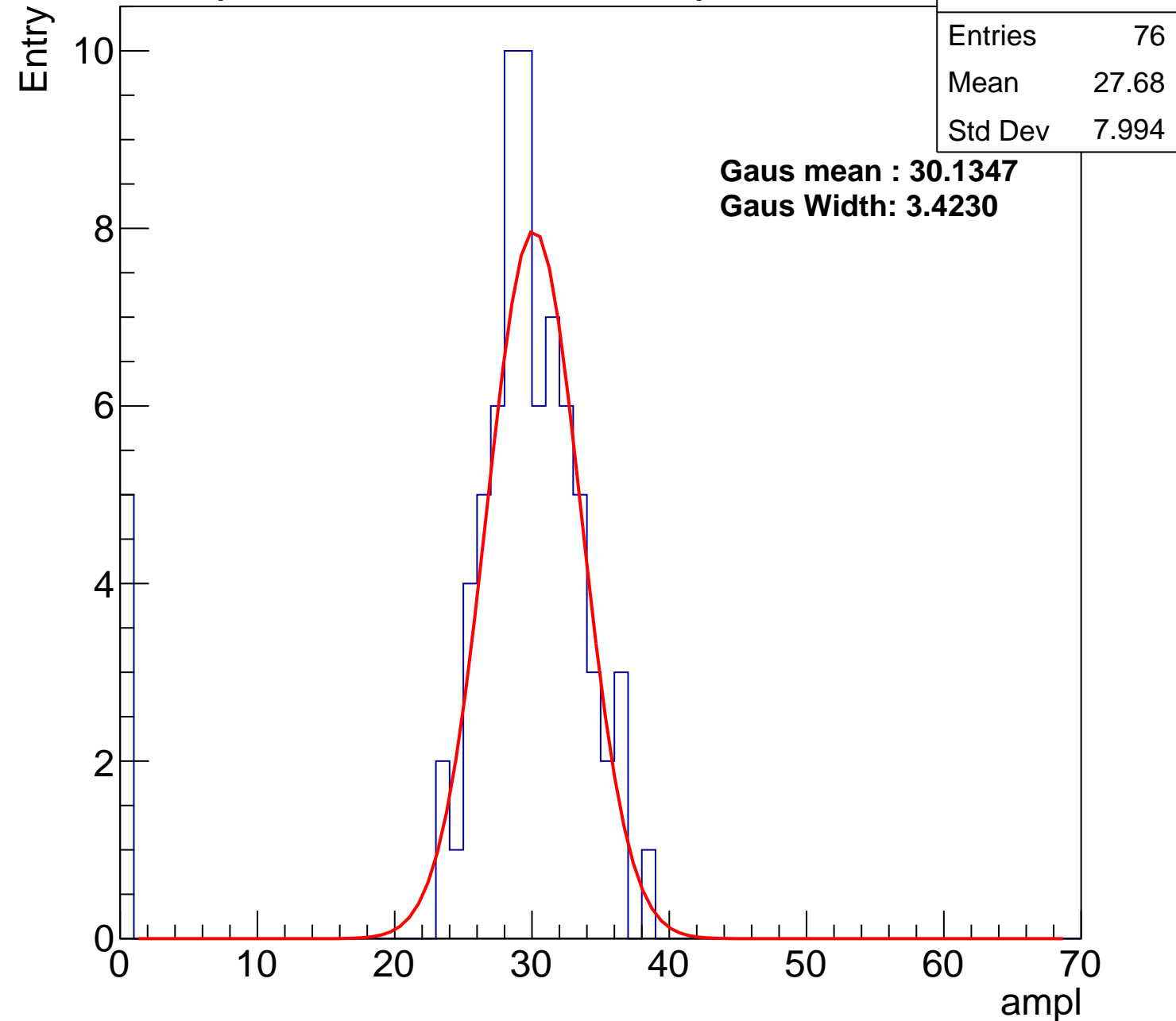
Gaus Width: 3.4230

Entry

10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U7-ch61, adc1

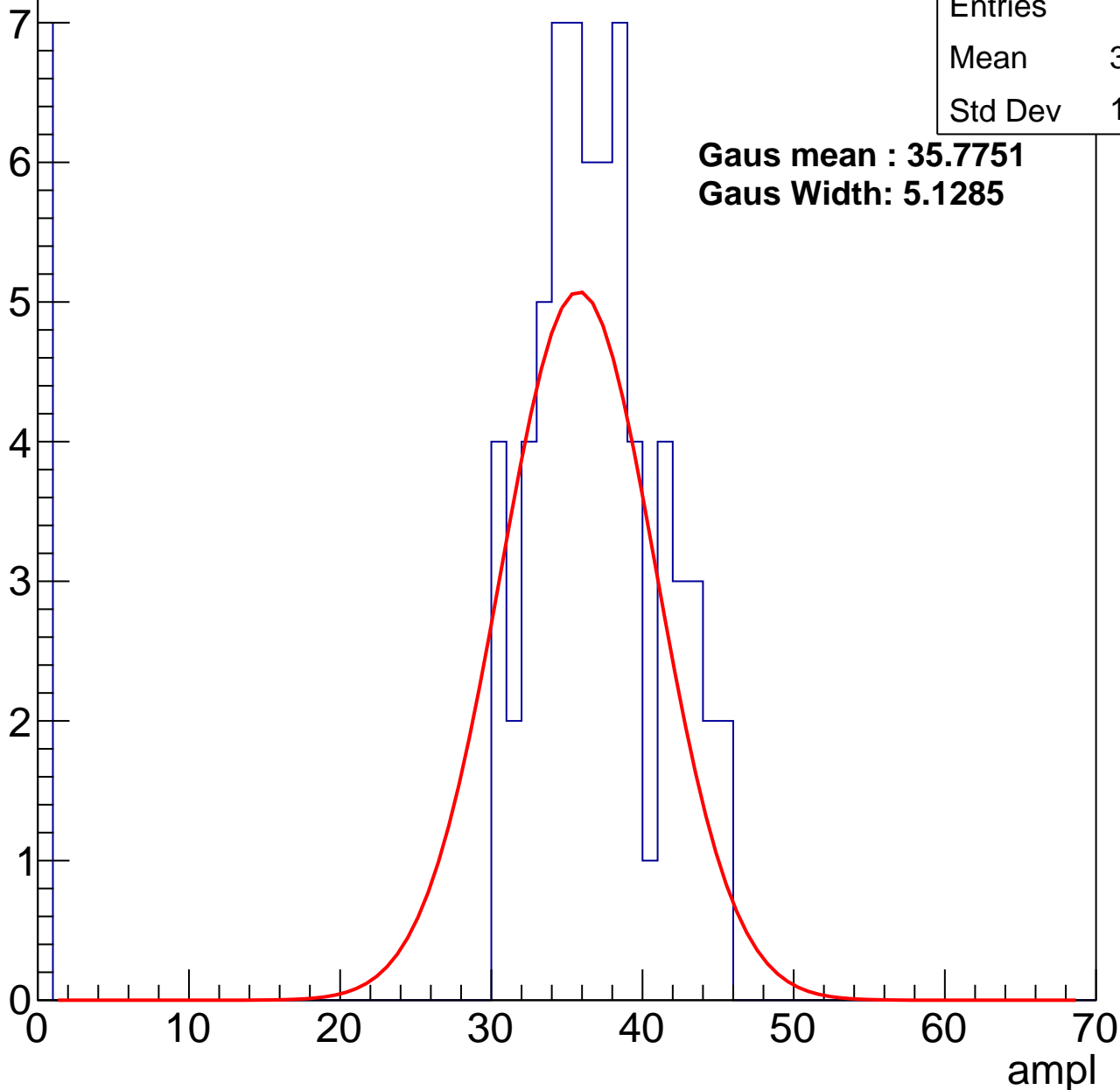
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	33.18
Std Dev	11.36

Gaus mean : 35.7751

Gaus Width: 5.1285



B1L103S, U7-ch61, adc2

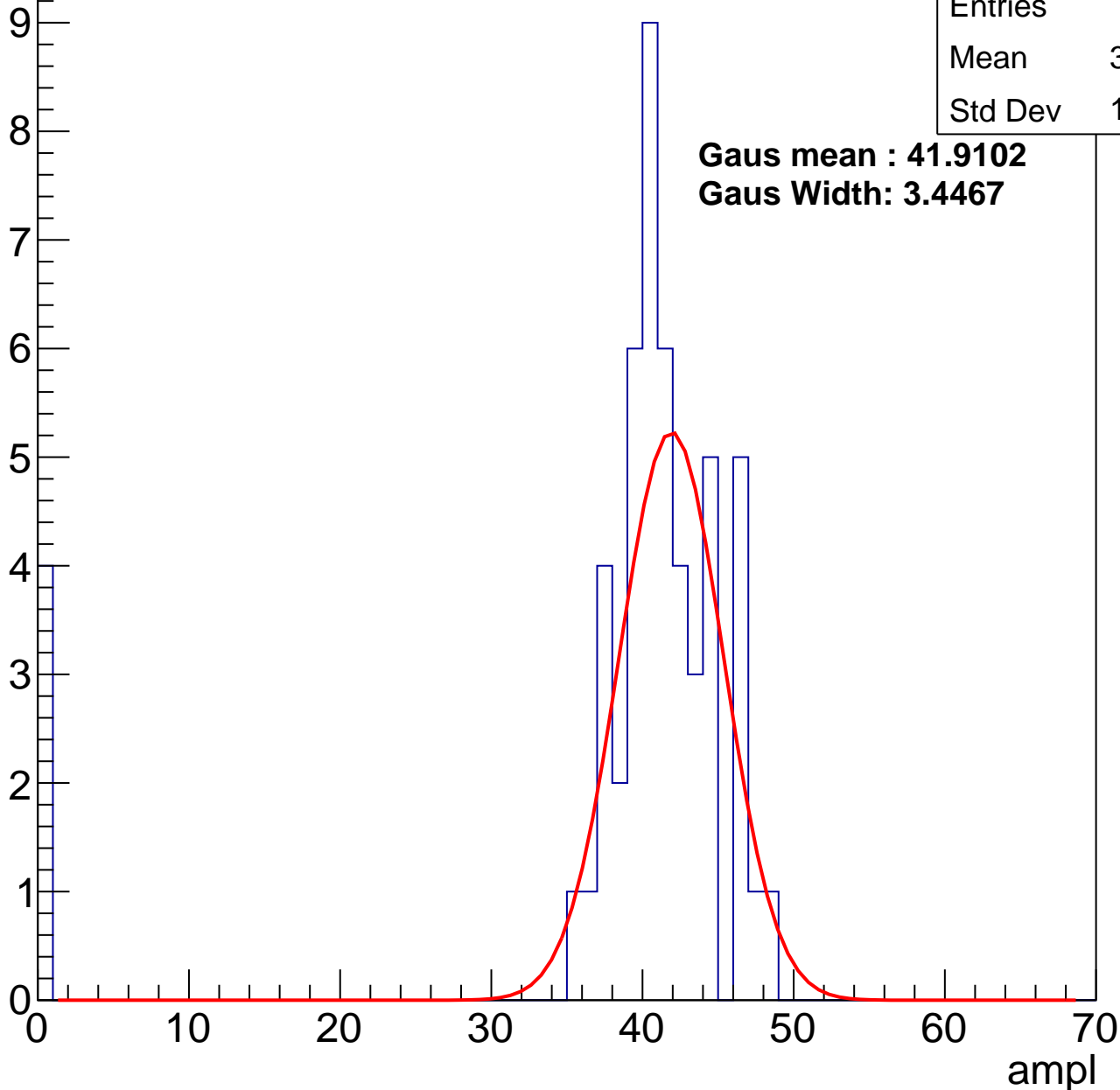
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	38.02
Std Dev	11.36

Gaus mean : 41.9102

Gaus Width: 3.4467

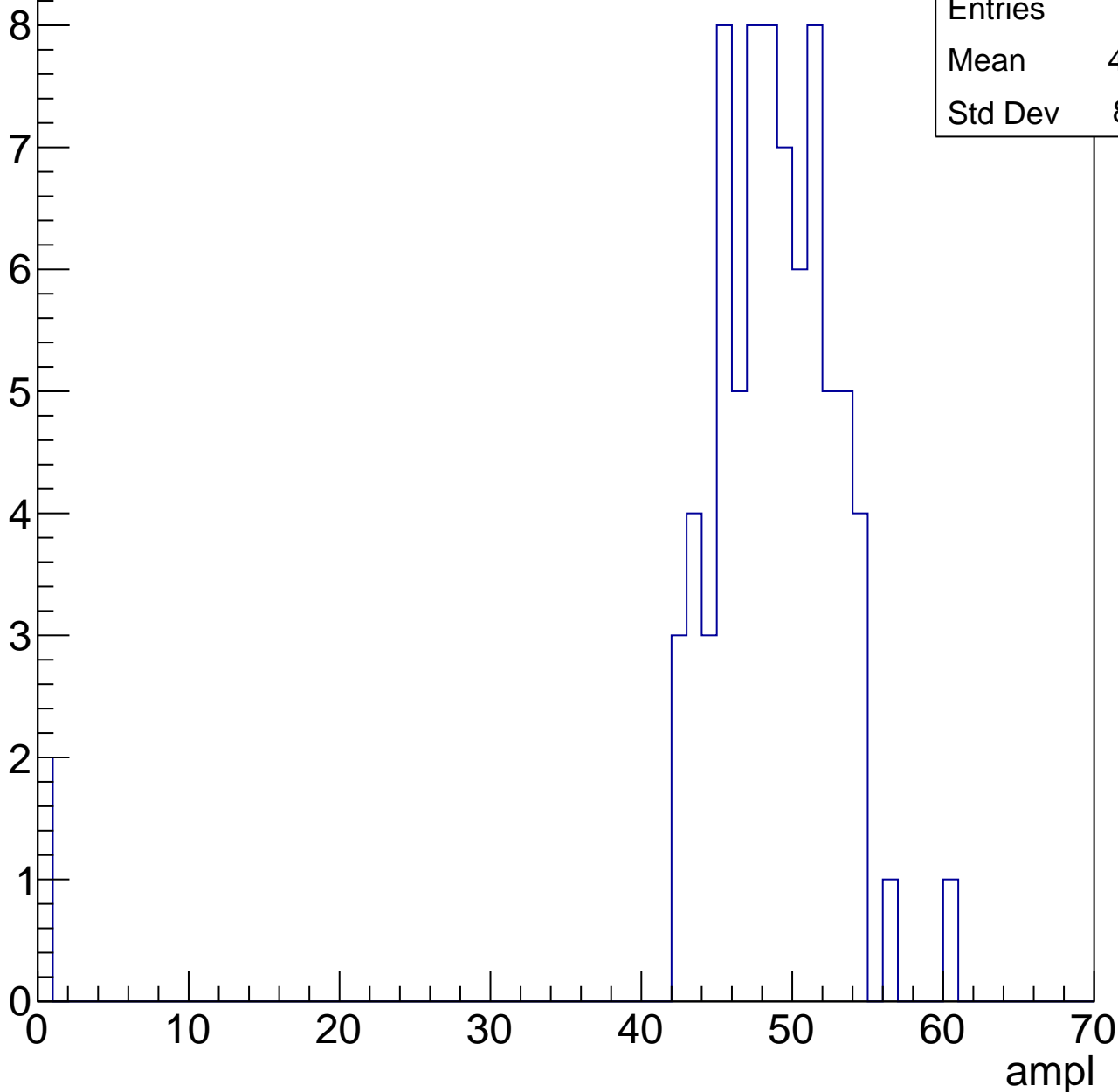


B1L103S, U7-ch61, adc3

calib_packv5_041523_1651.root, FC#0, port C2

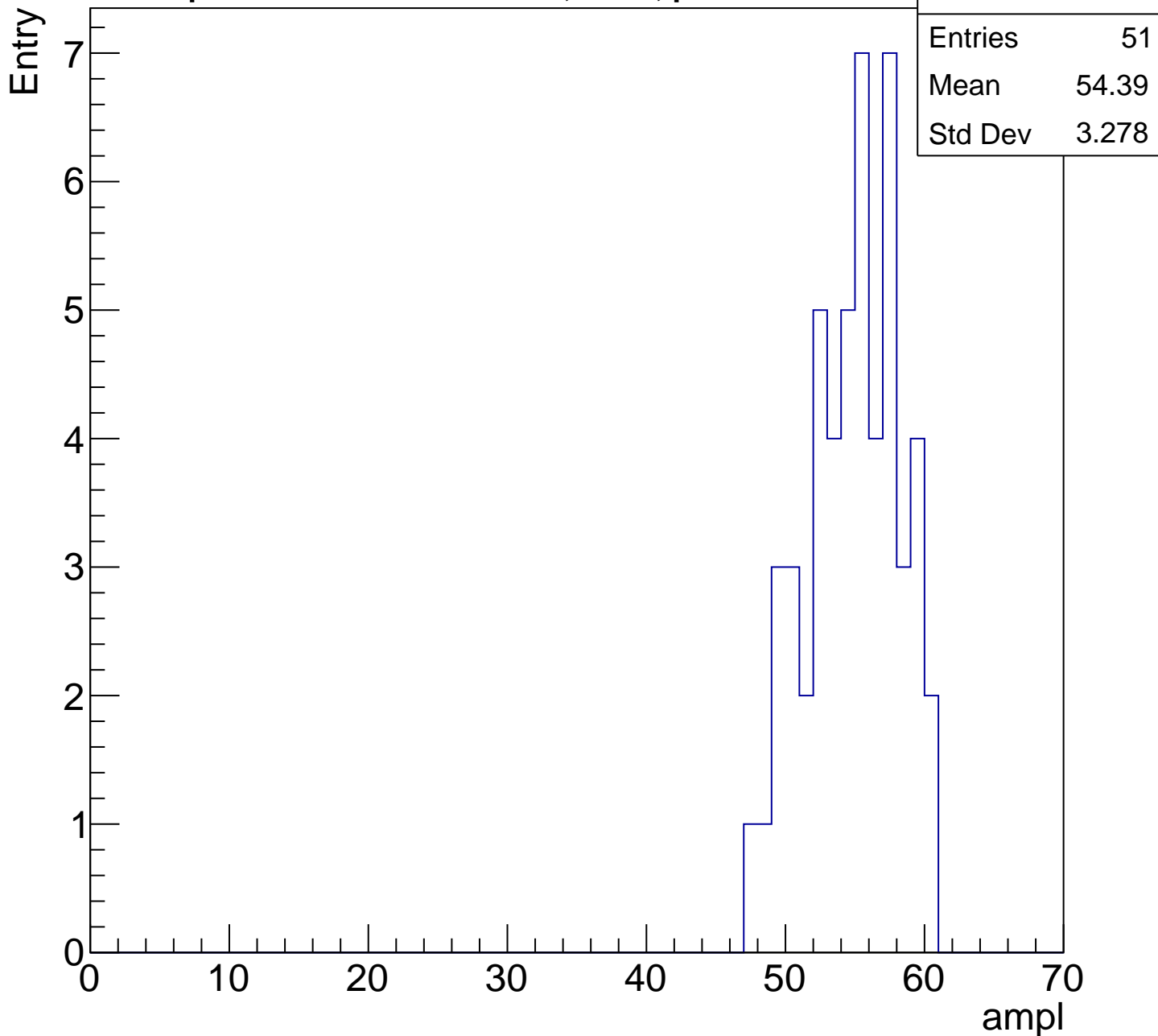
Entry

Entries	78
Mean	47.28
Std Dev	8.461



B1L103S, U7-ch61, adc4

calib_packv5_041523_1651.root, FC#0, port C2

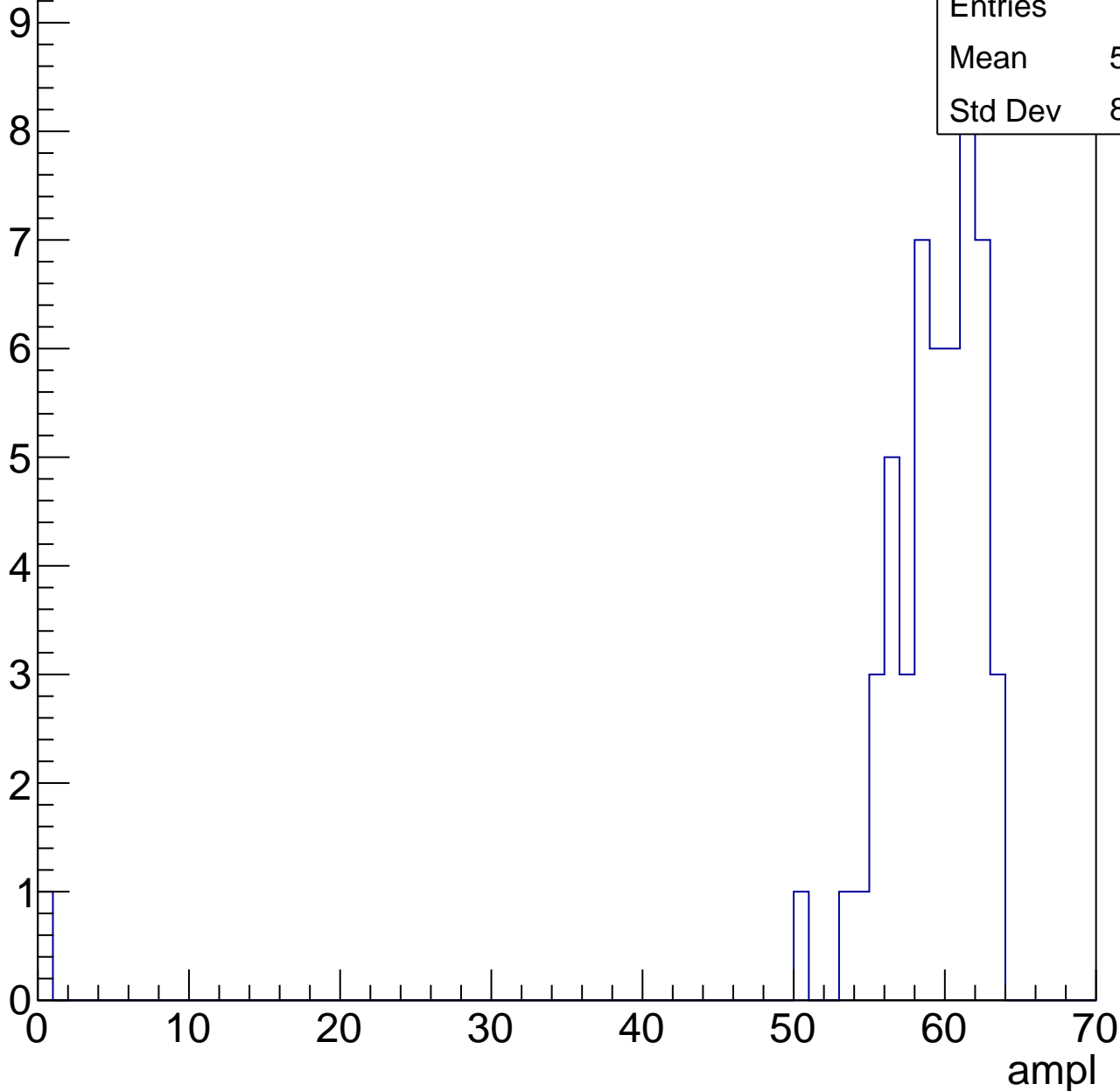


B1L103S, U7-ch61, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	57.83
Std Dev	8.485

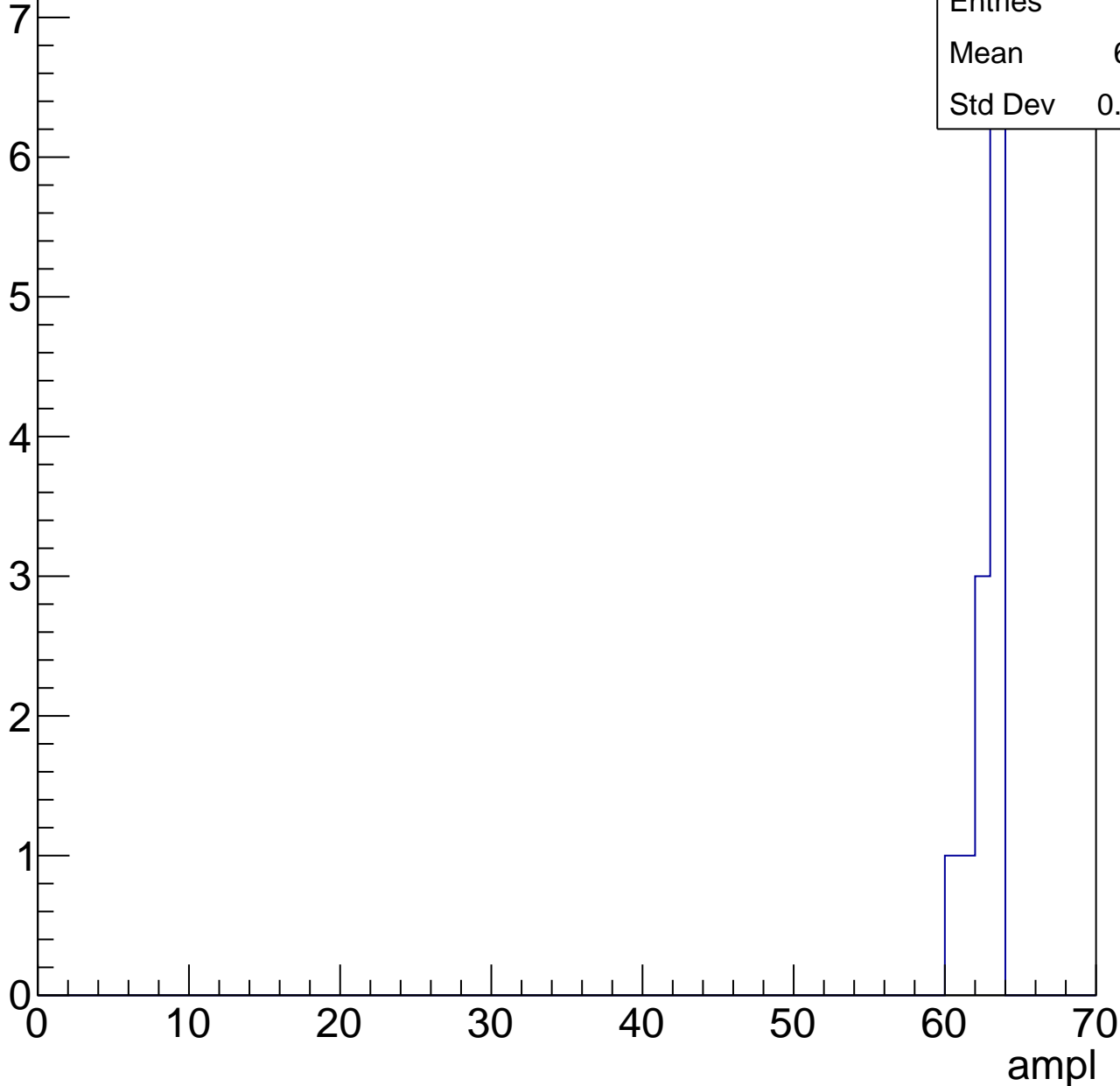


B1L103S, U7-ch61, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	12
Mean	62.33
Std Dev	0.9428



B1L103S, U7-ch61, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	18
Mean	1.222
Std Dev	5.039

Entry

16
14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

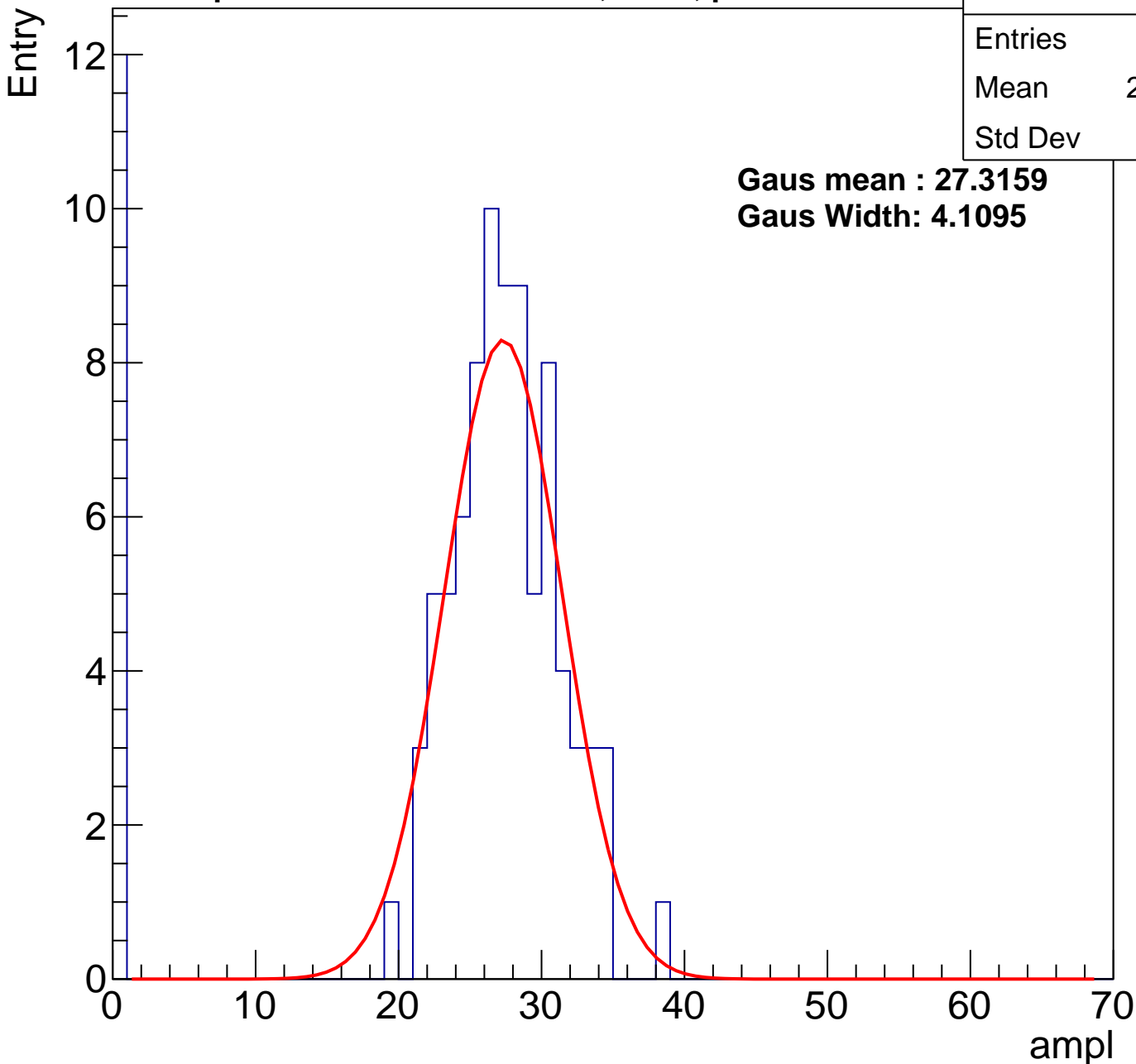
B1L103S, U7-ch62, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	95
Mean	23.68
Std Dev	9.62

Gaus mean : 27.3159

Gaus Width: 4.1095



B1L103S, U7-ch62, adc1

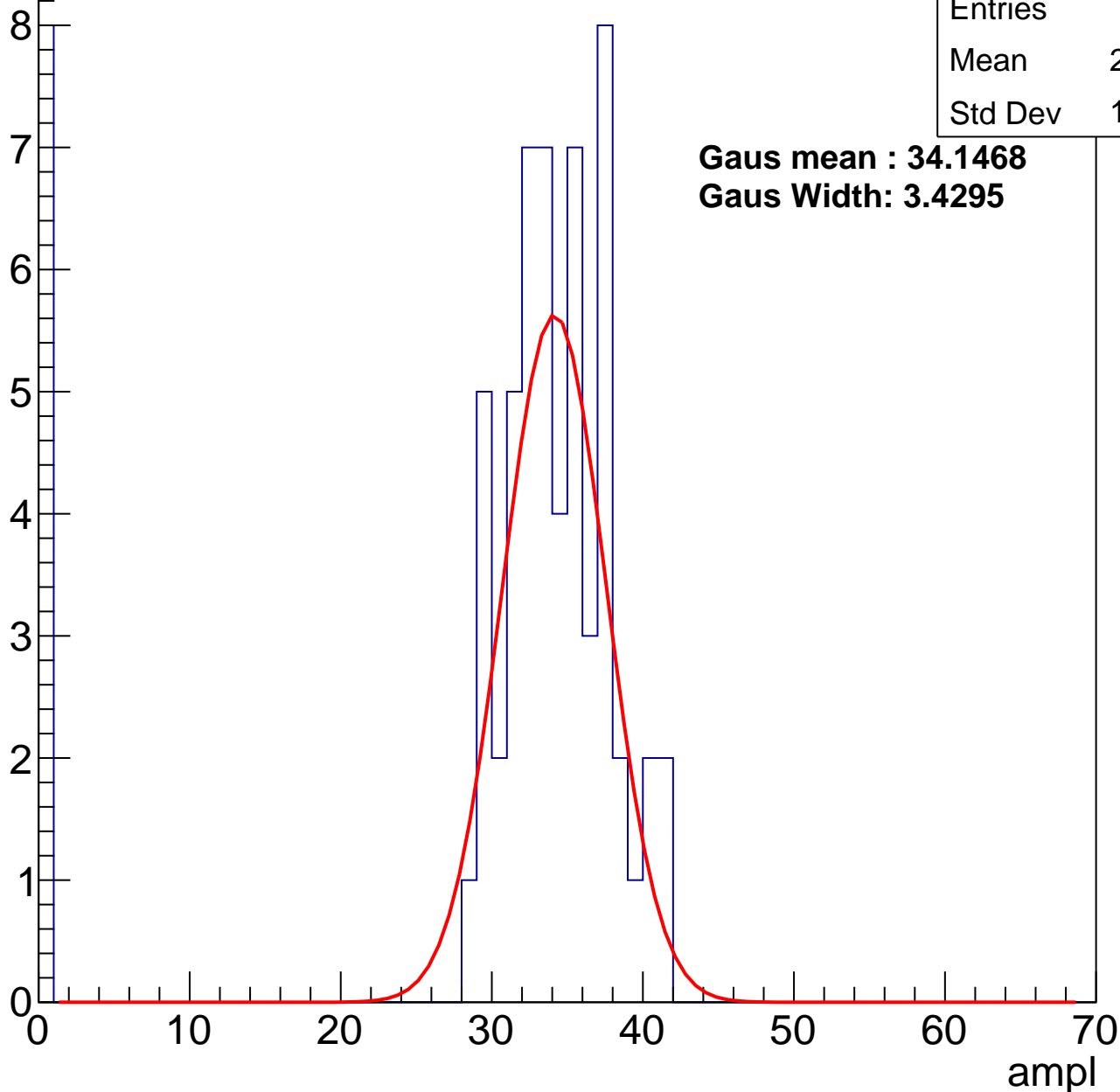
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	29.77
Std Dev	11.65

Gaus mean : 34.1468

Gaus Width: 3.4295



B1L103S, U7-ch62, adc2

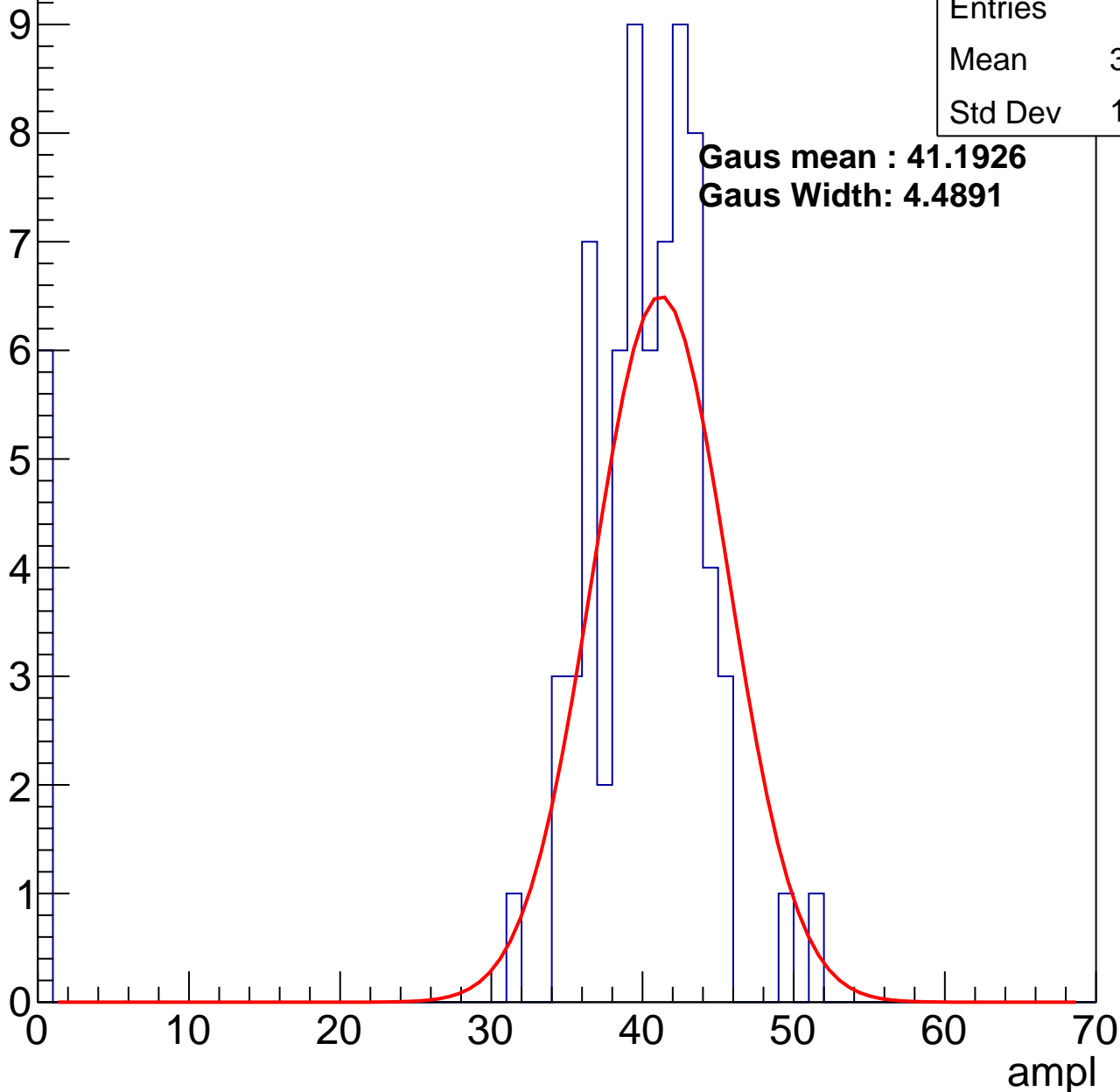
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	36.88
Std Dev	11.32

Gaus mean : 41.1926

Gaus Width: 4.4891



B1L103S, U7-ch62, adc3

calib_packv5_041523_1651.root, FC#0, port C2

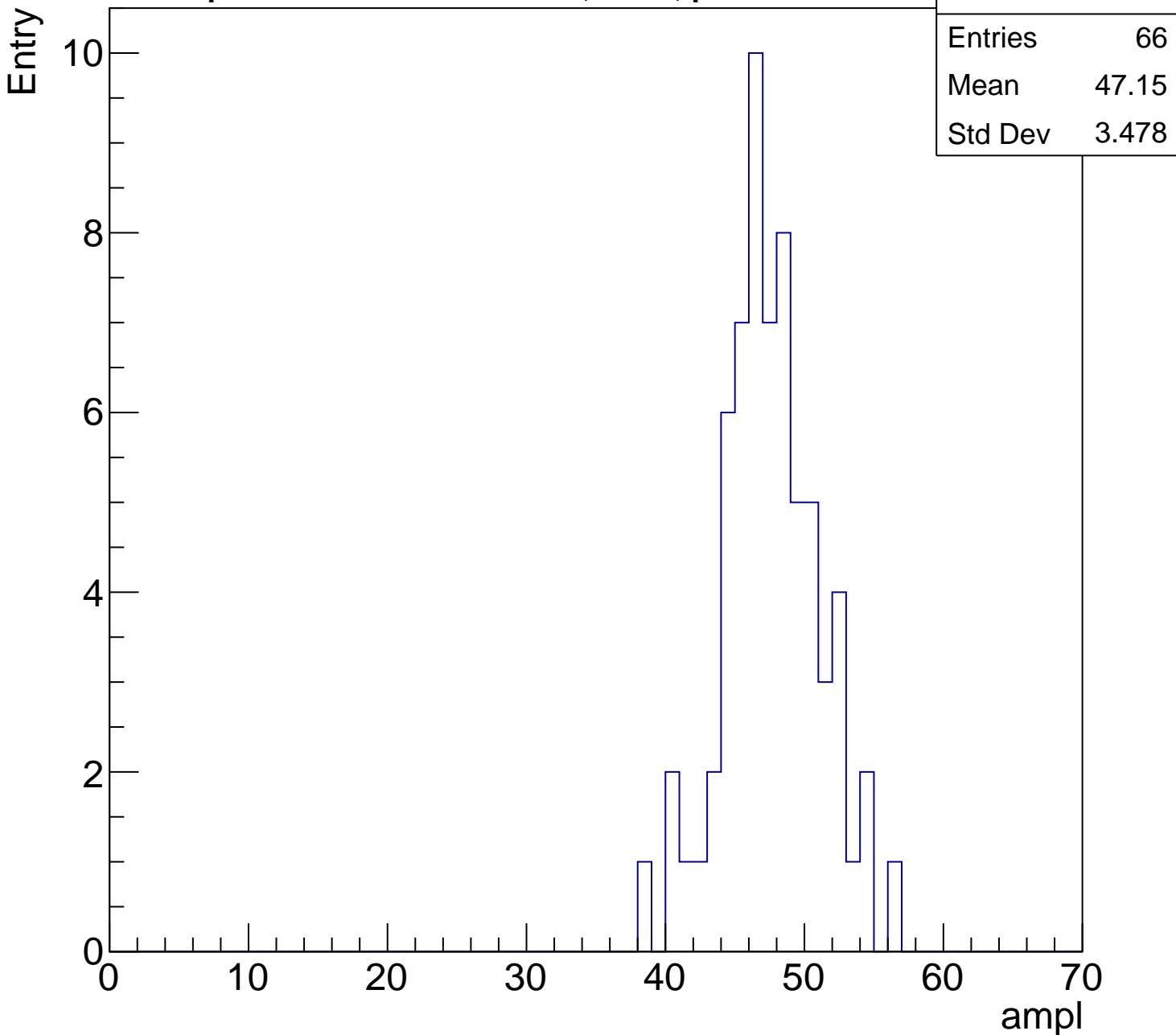
Entries	66
Mean	47.15
Std Dev	3.478

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

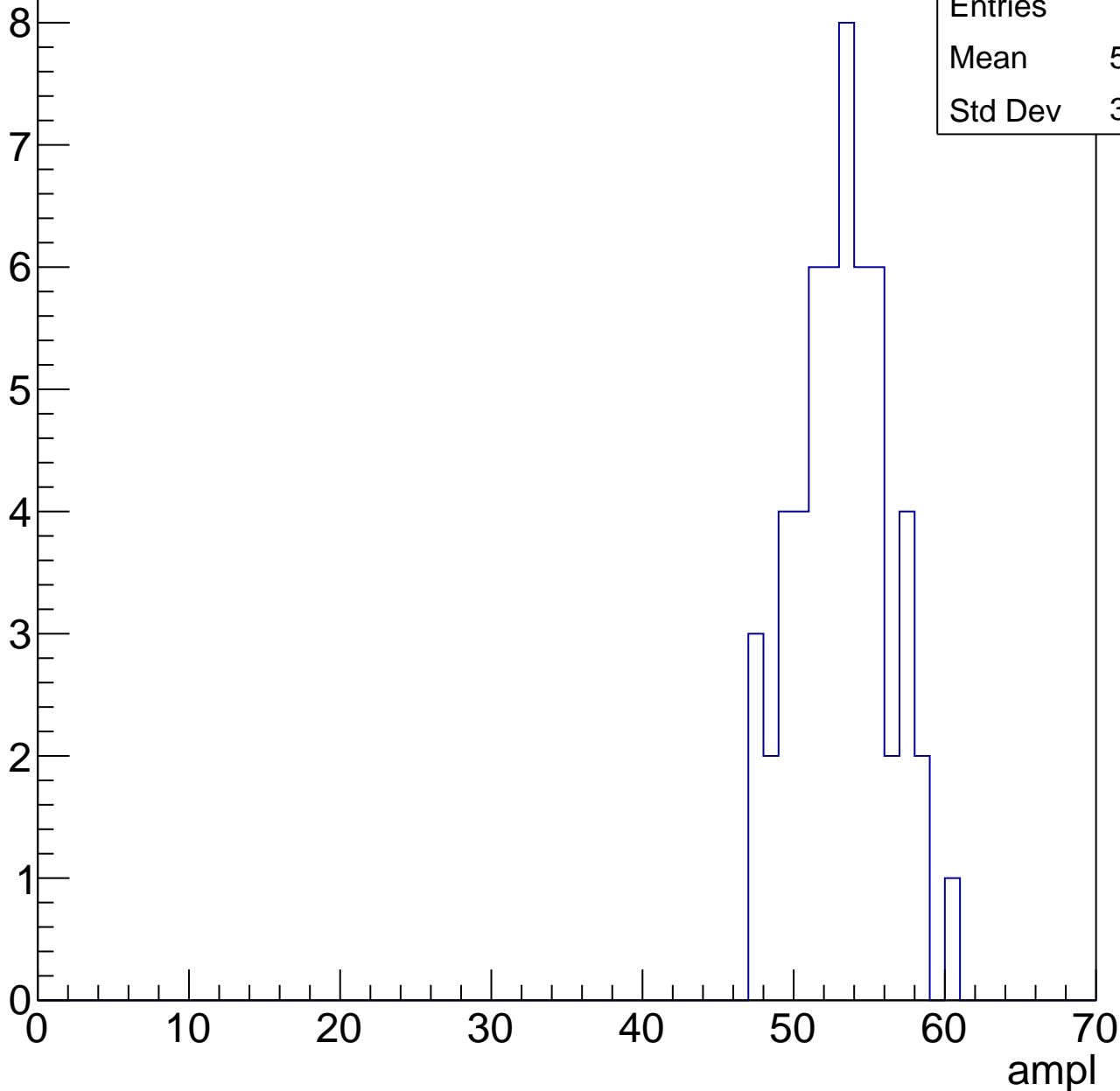


B1L103S, U7-ch62, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	52.69
Std Dev	3.024

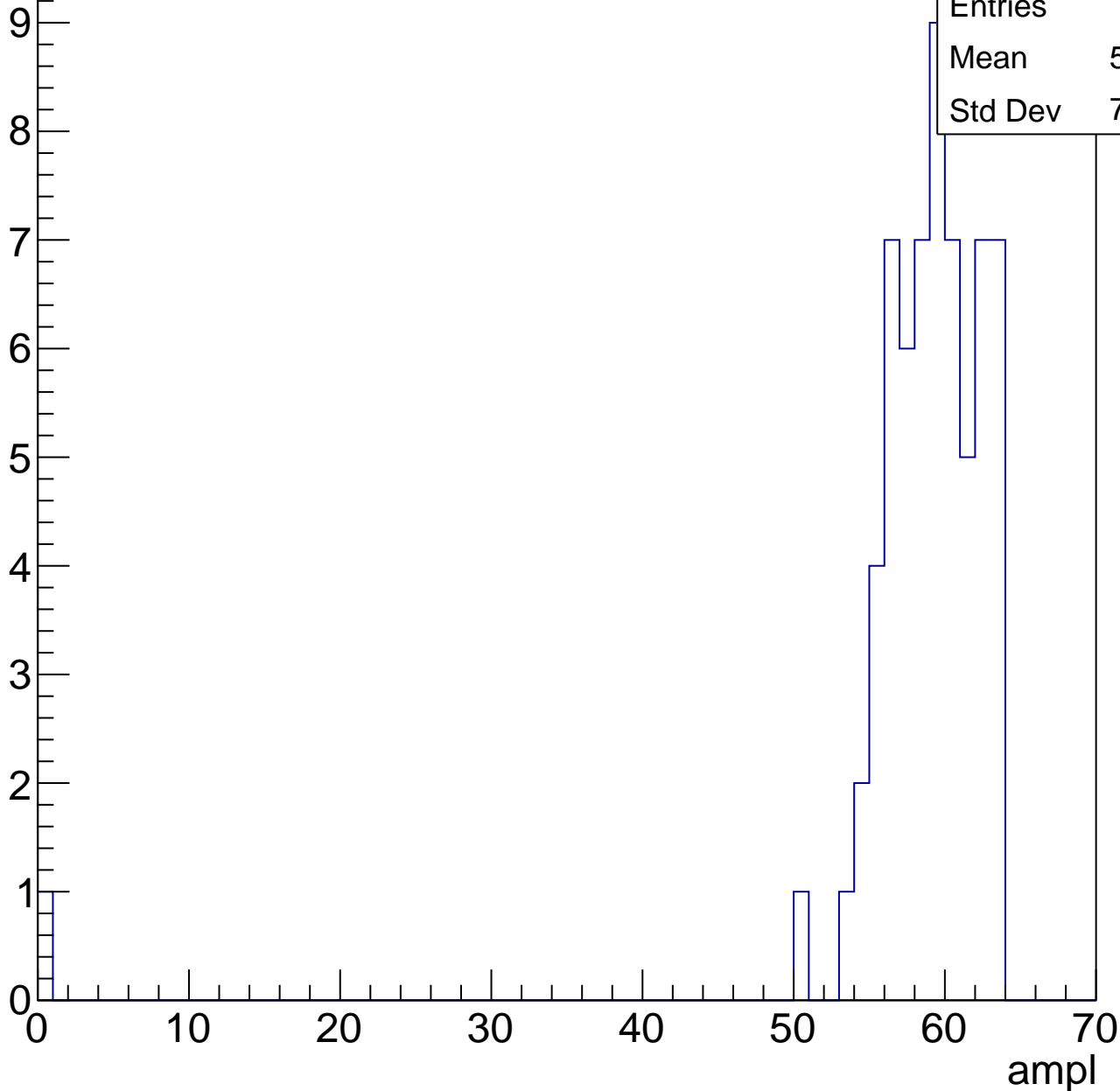


B1L103S, U7-ch62, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	57.84
Std Dev	7.829

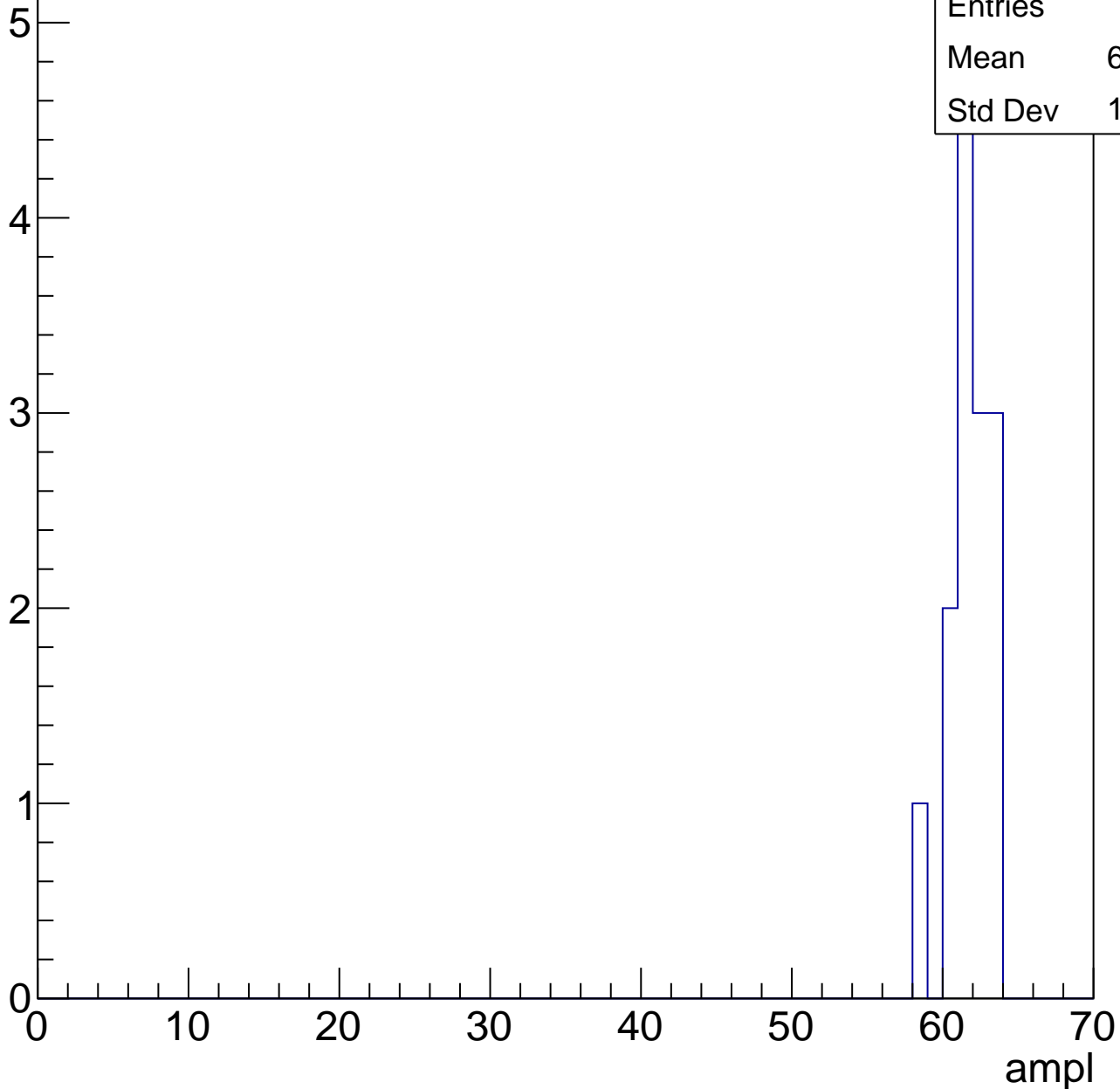


B1L103S, U7-ch62, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	14
Mean	61.29
Std Dev	1.332

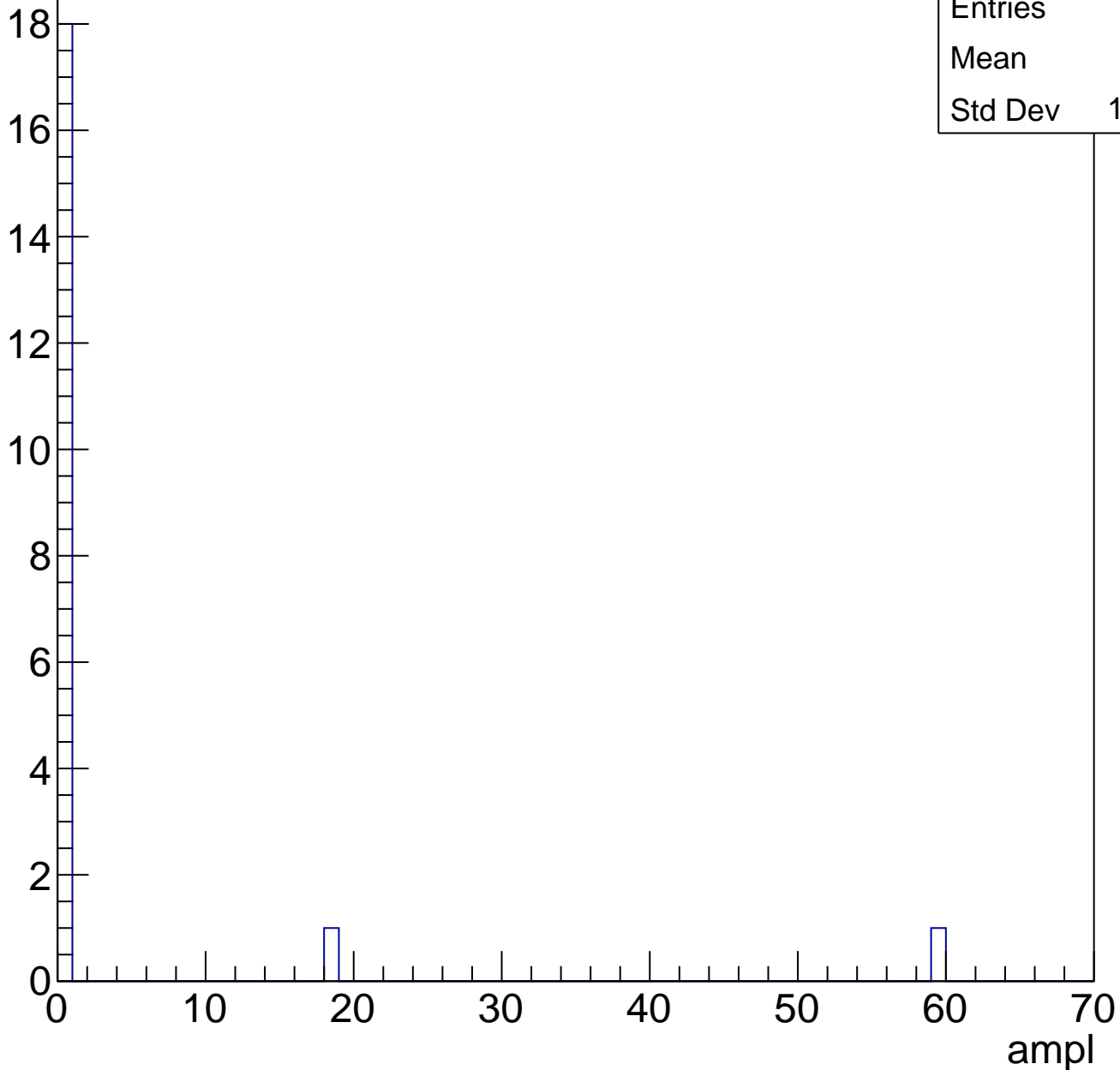


B1L103S, U7-ch62, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.85
Std Dev	13.24

Entry



B1L103S, U7-ch63, adc0

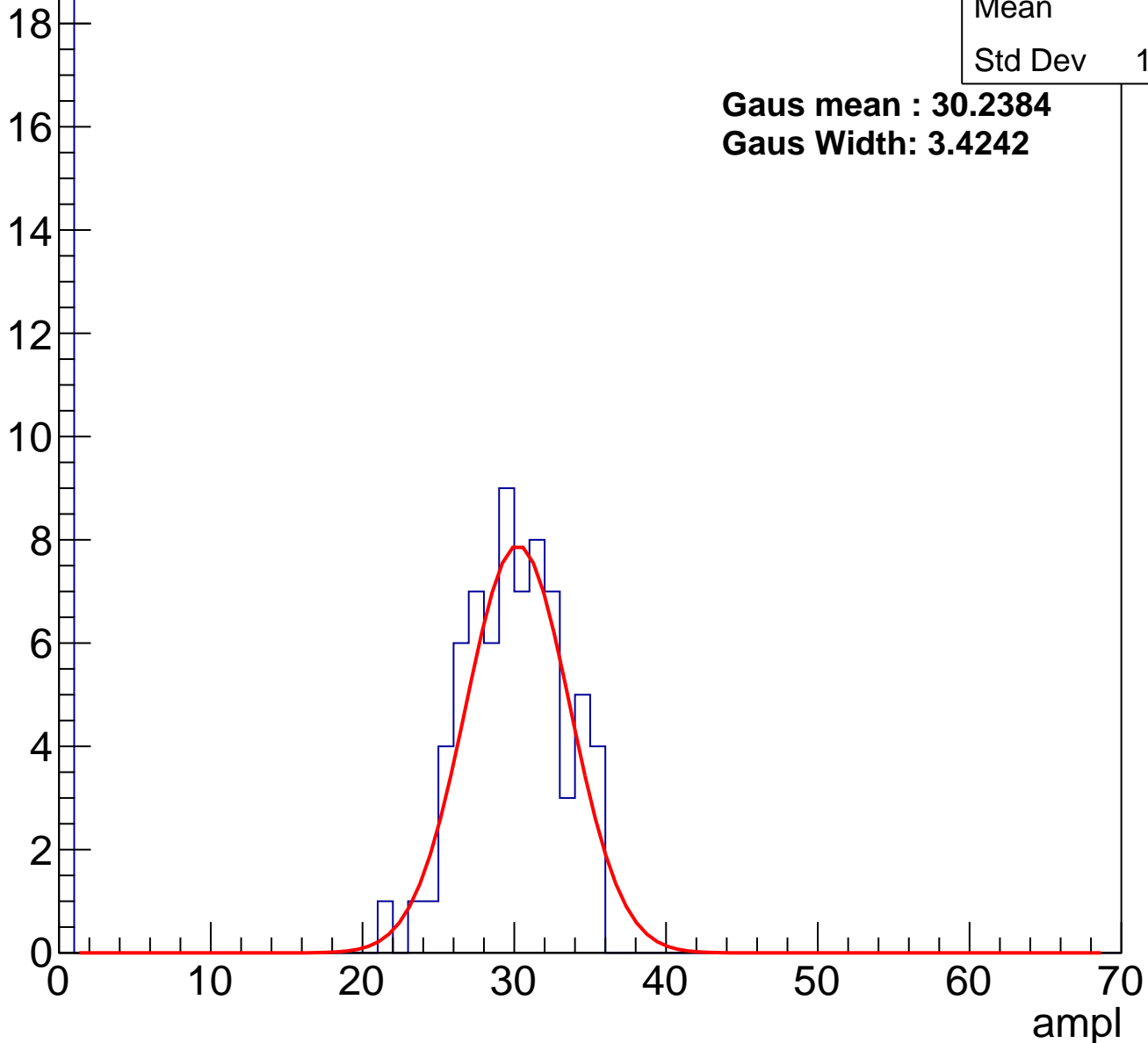
calib_packv5_041523_1651.root, FC#0, port C2

Entries	88
Mean	23.1
Std Dev	12.44

Gaus mean : 30.2384

Gaus Width: 3.4242

Entry



B1L103S, U7-ch63, adc1

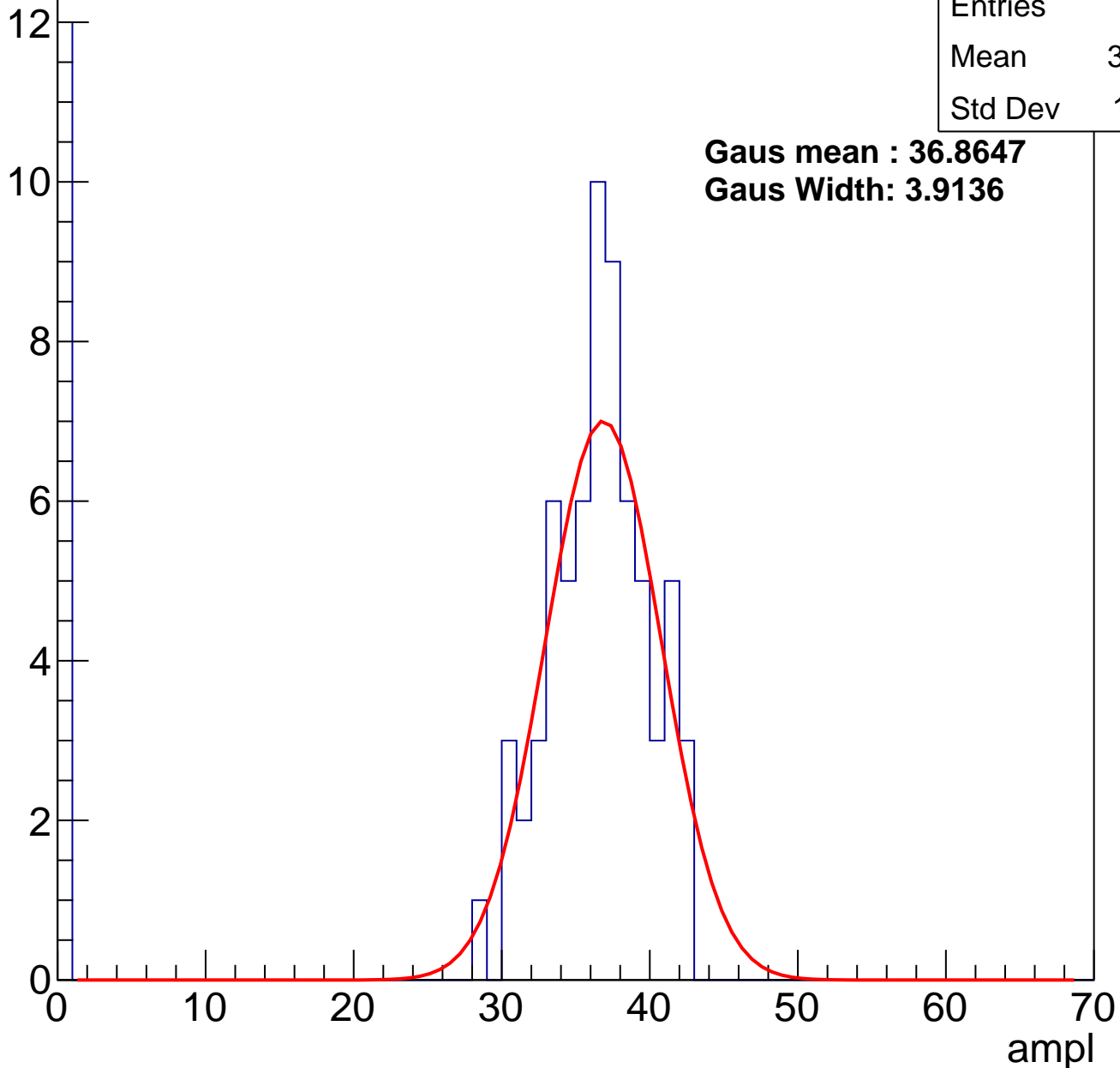
calib_packv5_041523_1651.root, FC#0, port C2

Entries	79
Mean	30.65
Std Dev	13.31

Gaus mean : 36.8647

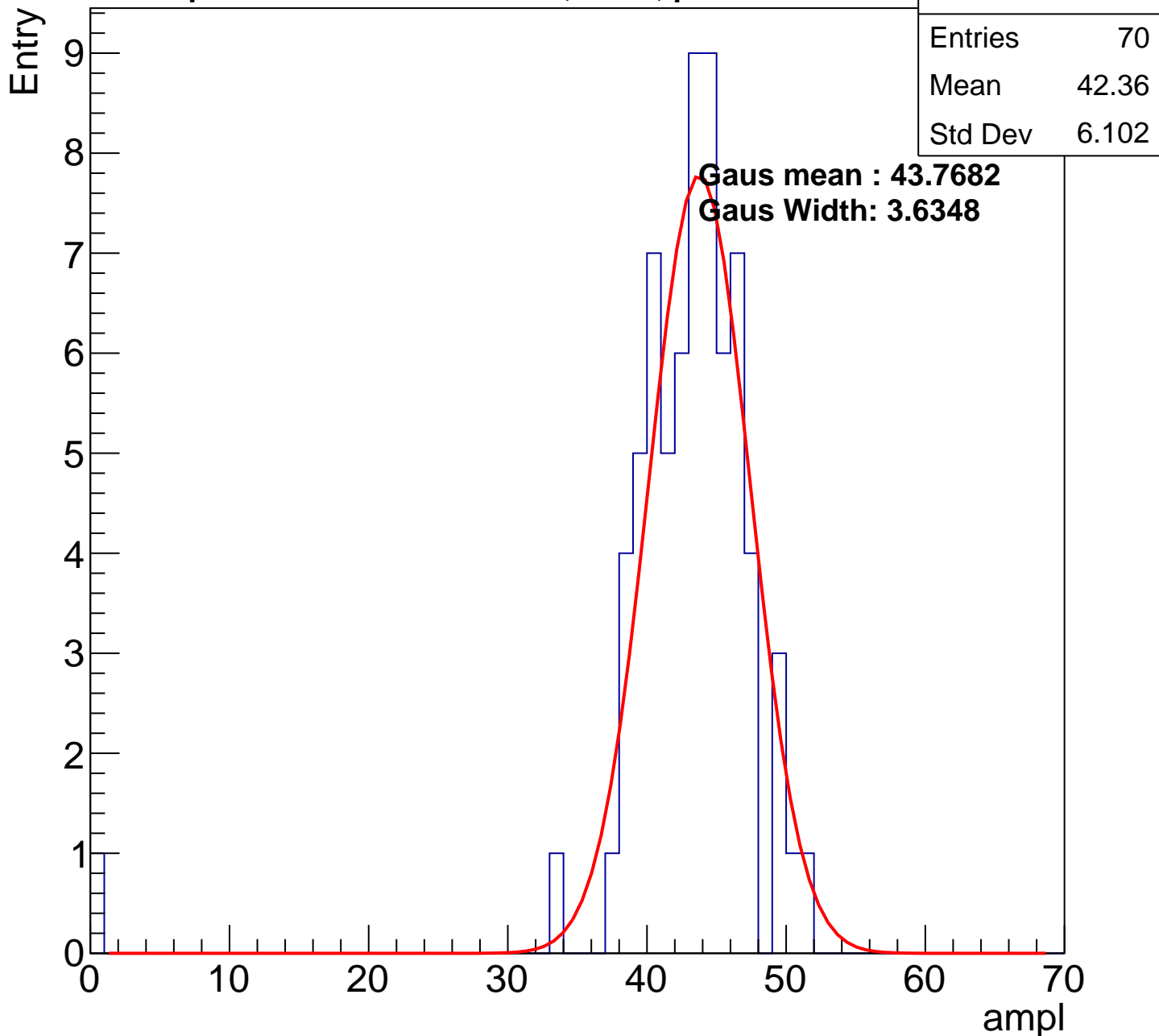
Gaus Width: 3.9136

Entry



B1L103S, U7-ch63, adc2

calib_packv5_041523_1651.root, FC#0, port C2

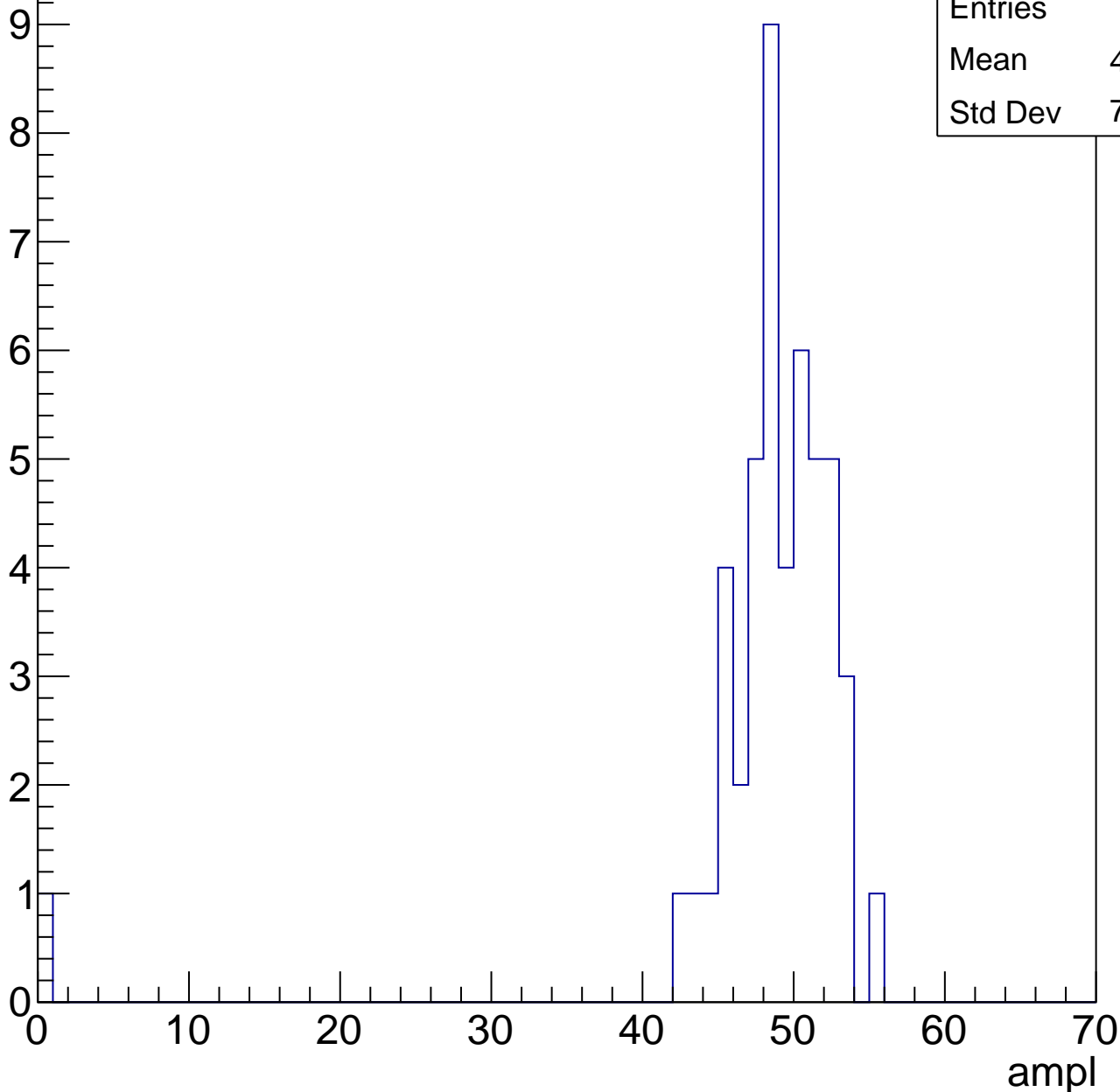


B1L103S, U7-ch63, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	48
Mean	47.77
Std Dev	7.506

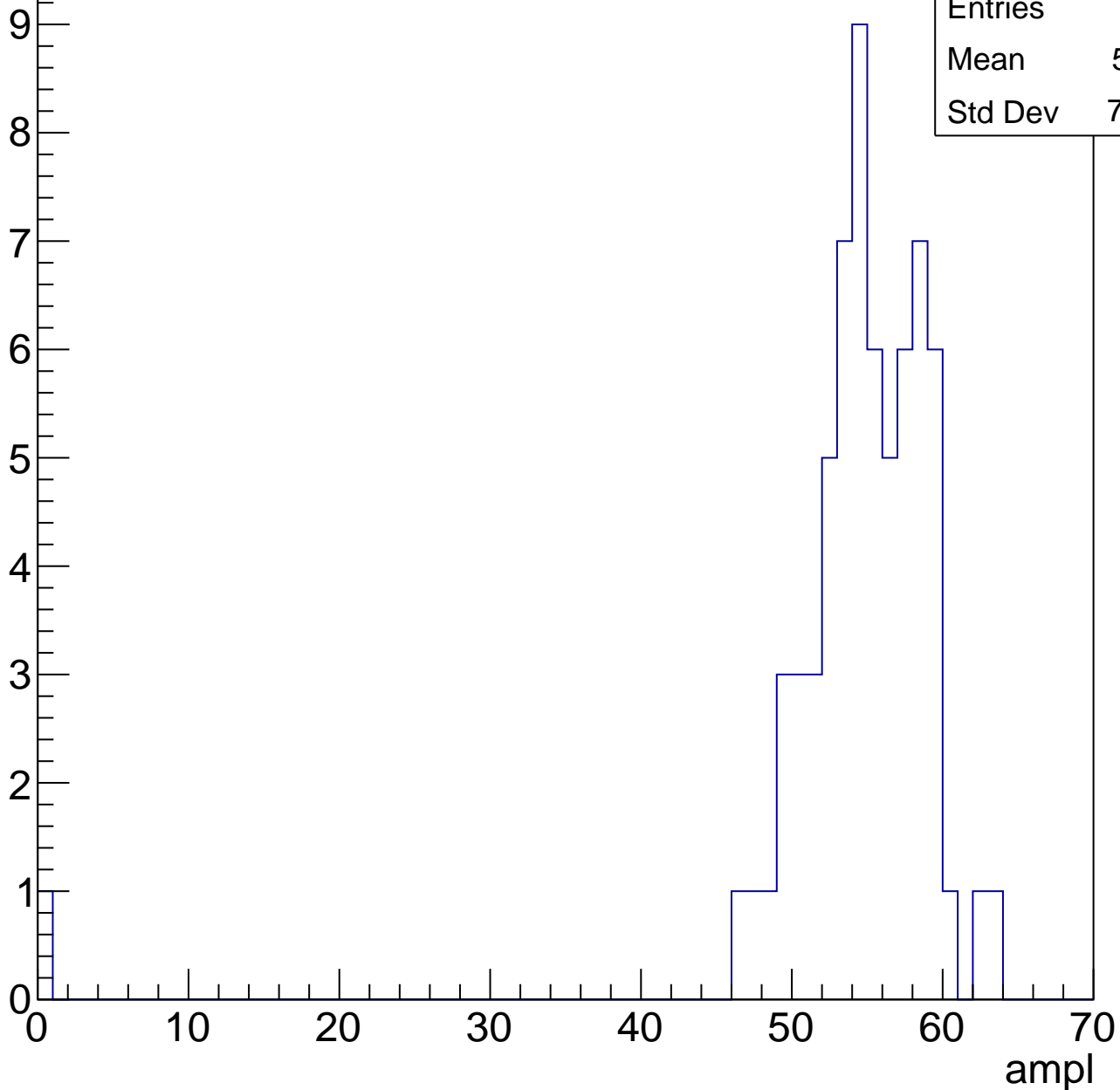


B1L103S, U7-ch63, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	53.81
Std Dev	7.494

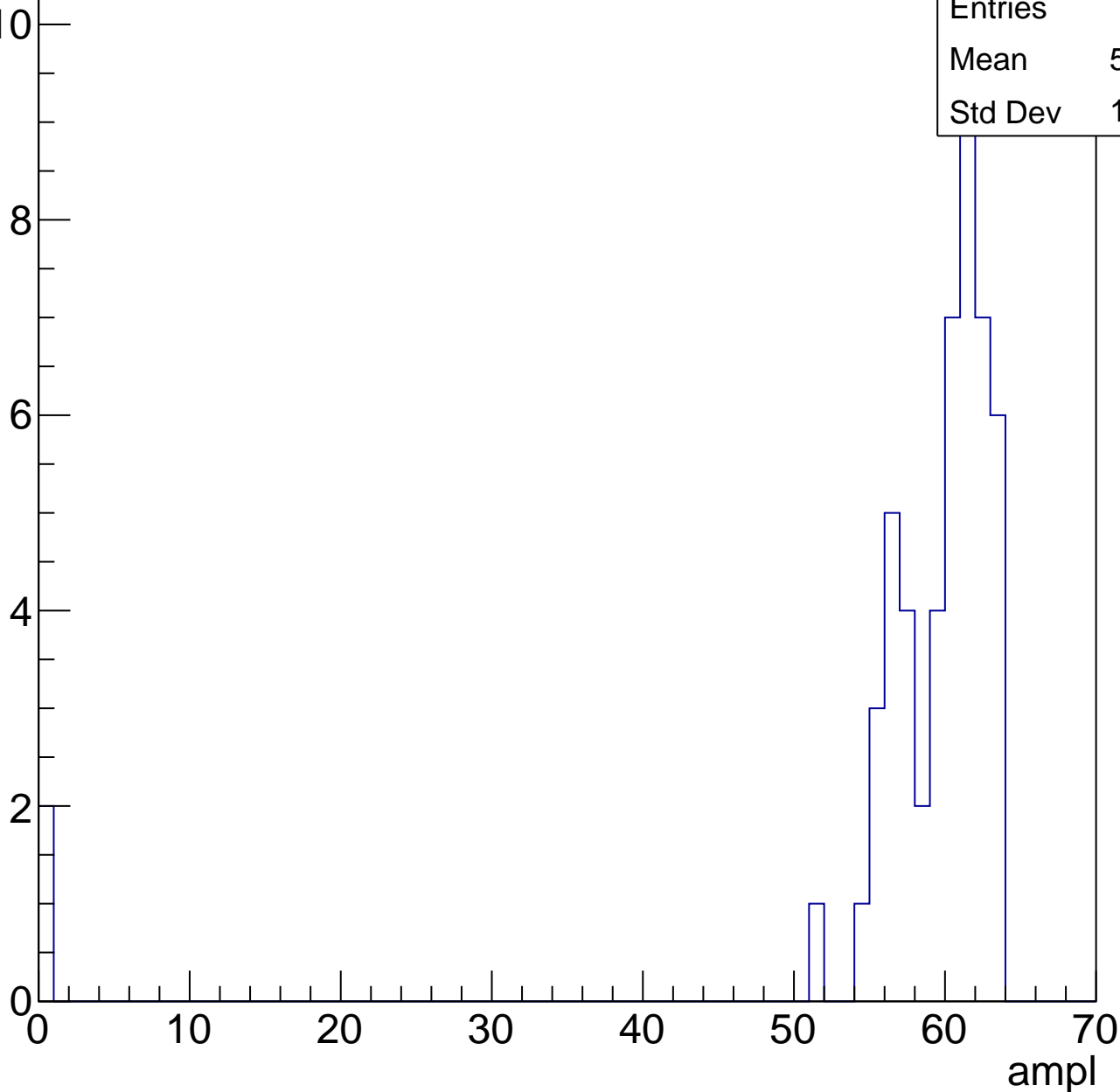


B1L103S, U7-ch63, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

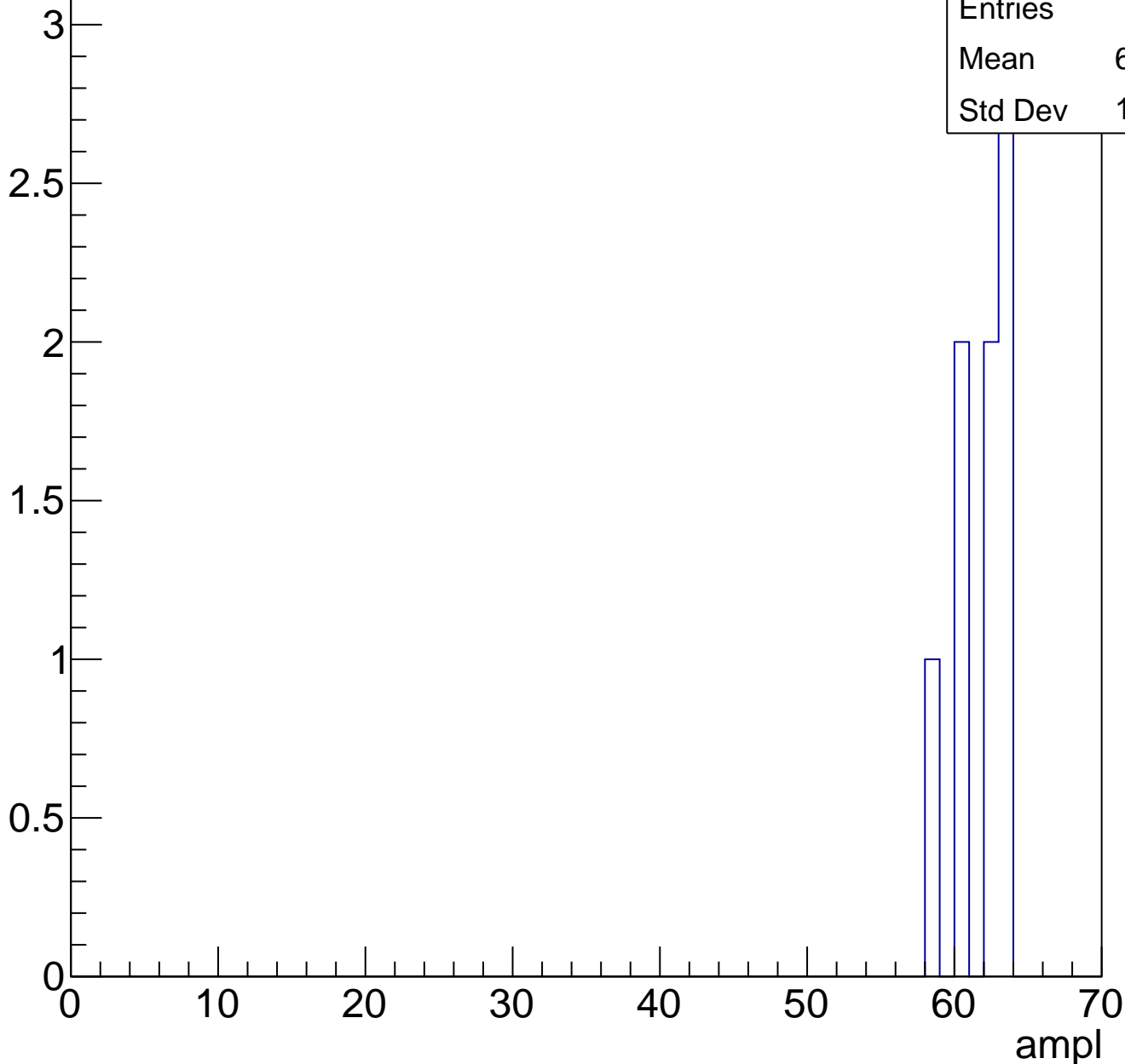
Entries	52
Mean	57.15
Std Dev	11.76



B1L103S, U7-ch63, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch63, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U7-ch64, adc0

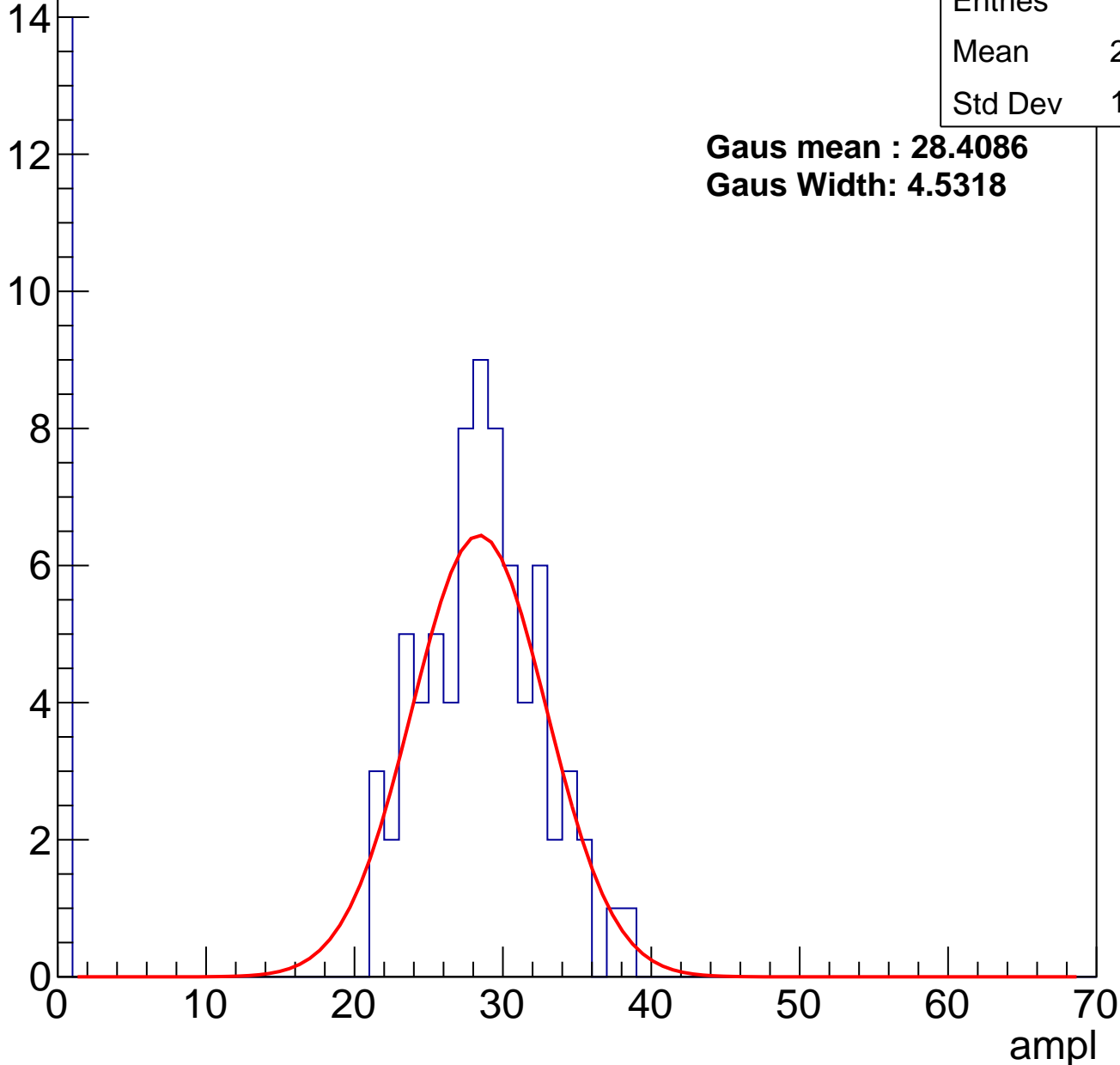
calib_packv5_041523_1651.root, FC#0, port C2

Entries	87
Mean	23.63
Std Dev	10.93

Gaus mean : 28.4086

Gaus Width: 4.5318

Entry



B1L103S, U7-ch64, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	90
Mean	30.81
Std Dev	12.04

Gaus mean : 35.4263

Gaus Width: 3.8671

Entry

10

8

6

4

2

0

0

10

20

30

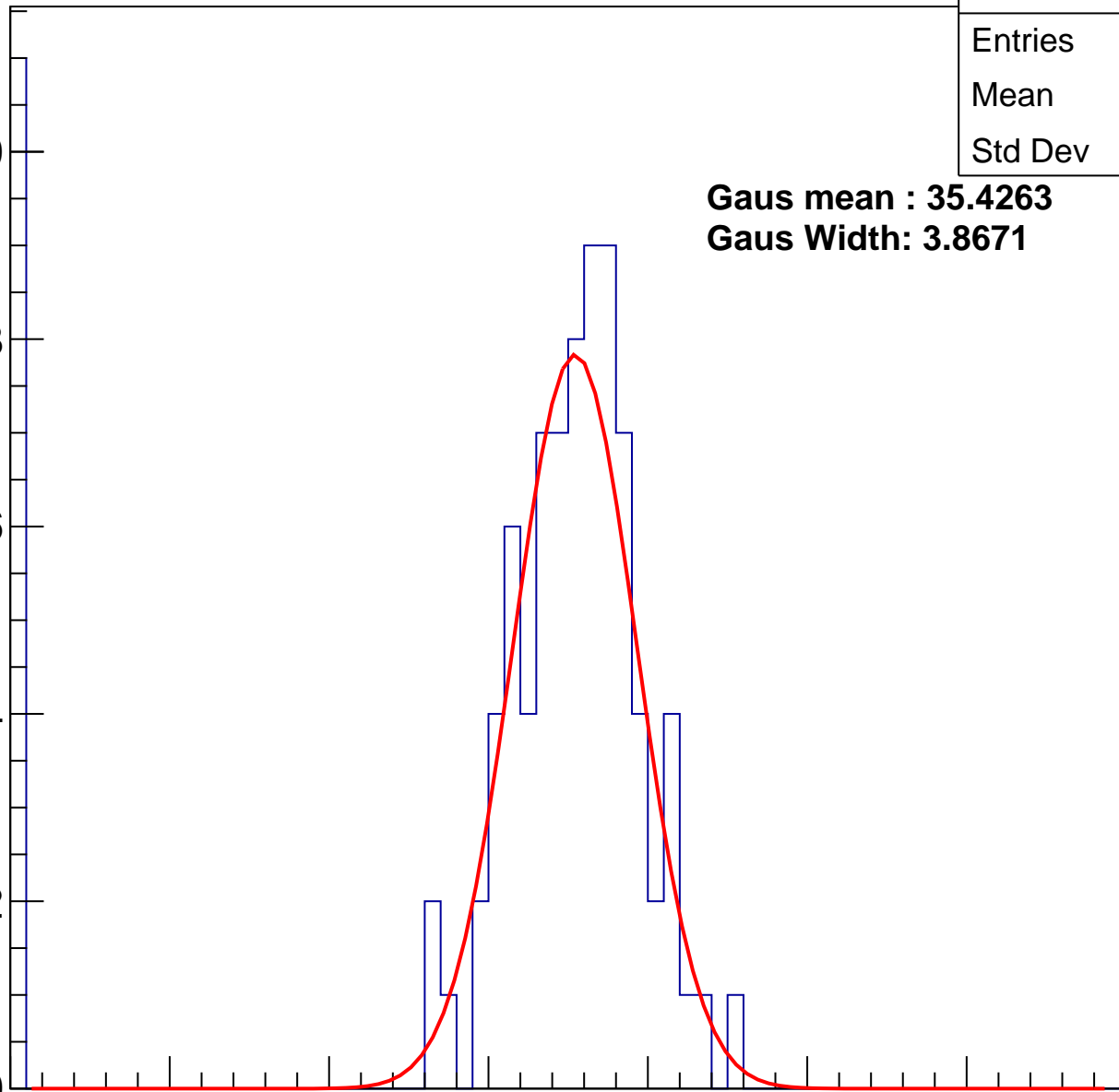
40

50

60

70

ampl



B1L103S, U7-ch64, adc2

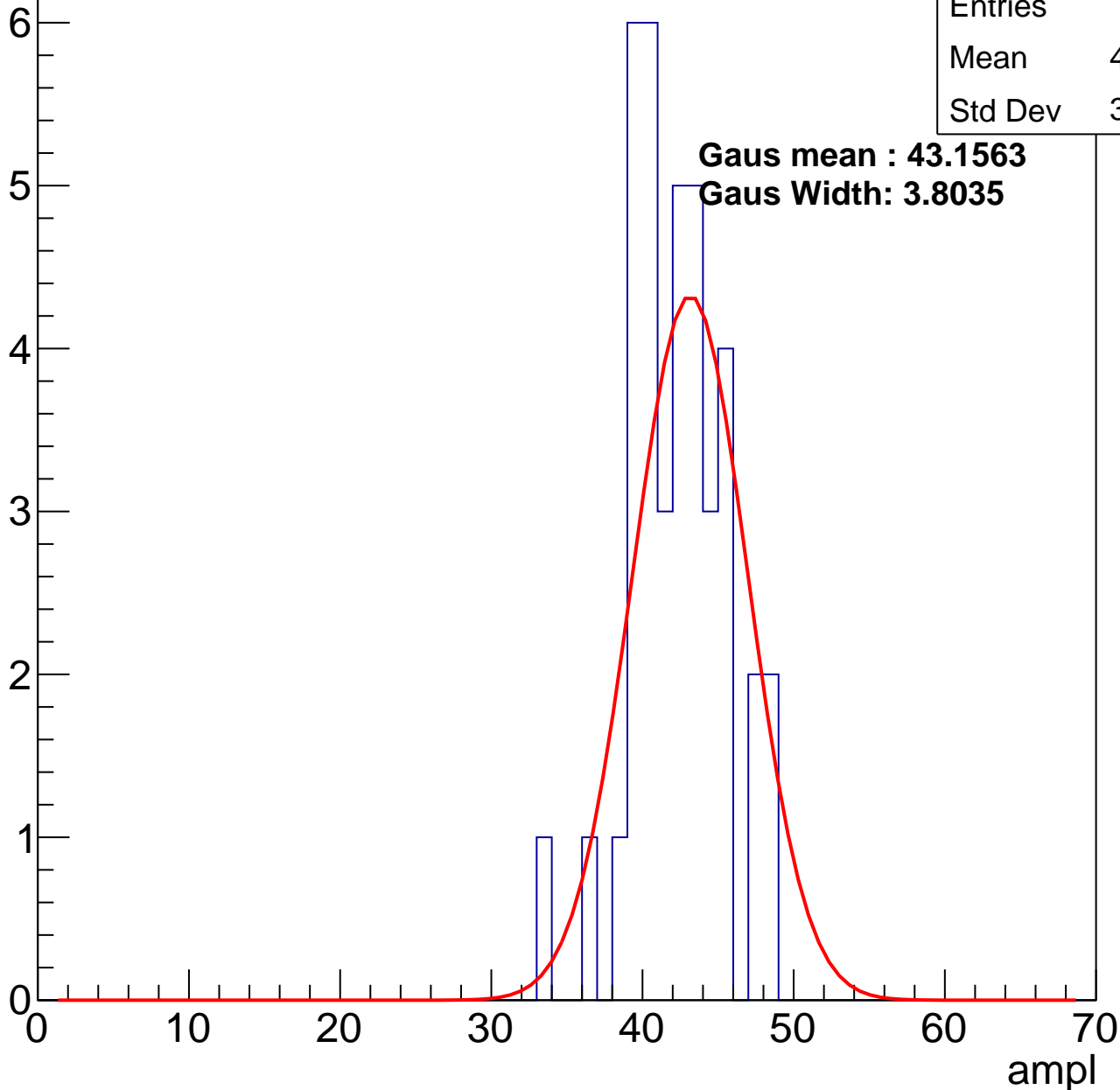
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	39
Mean	41.82
Std Dev	3.153

Gaus mean : 43.1563

Gaus Width: 3.8035

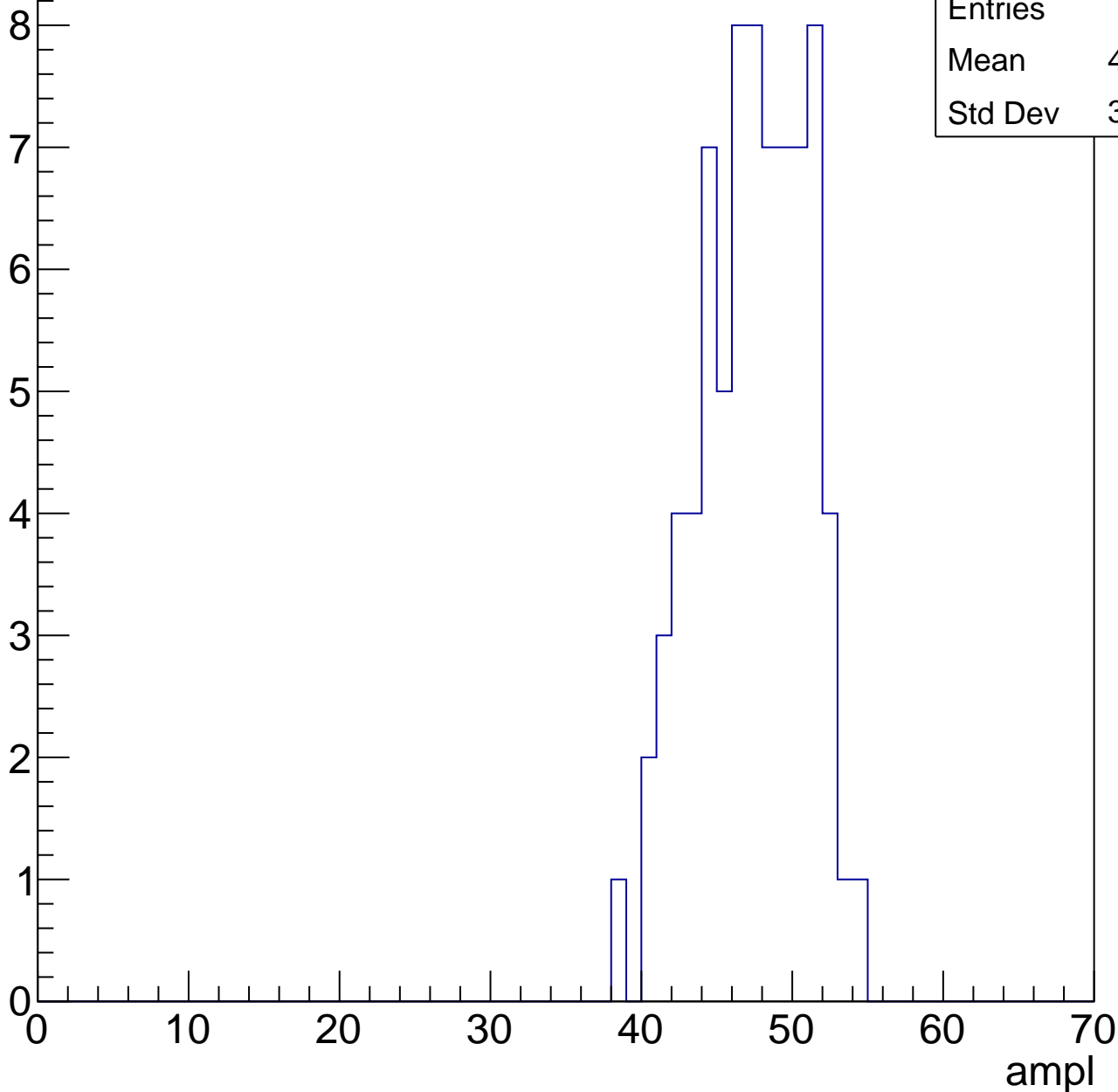


B1L103S, U7-ch64, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	46.88
Std Dev	3.516

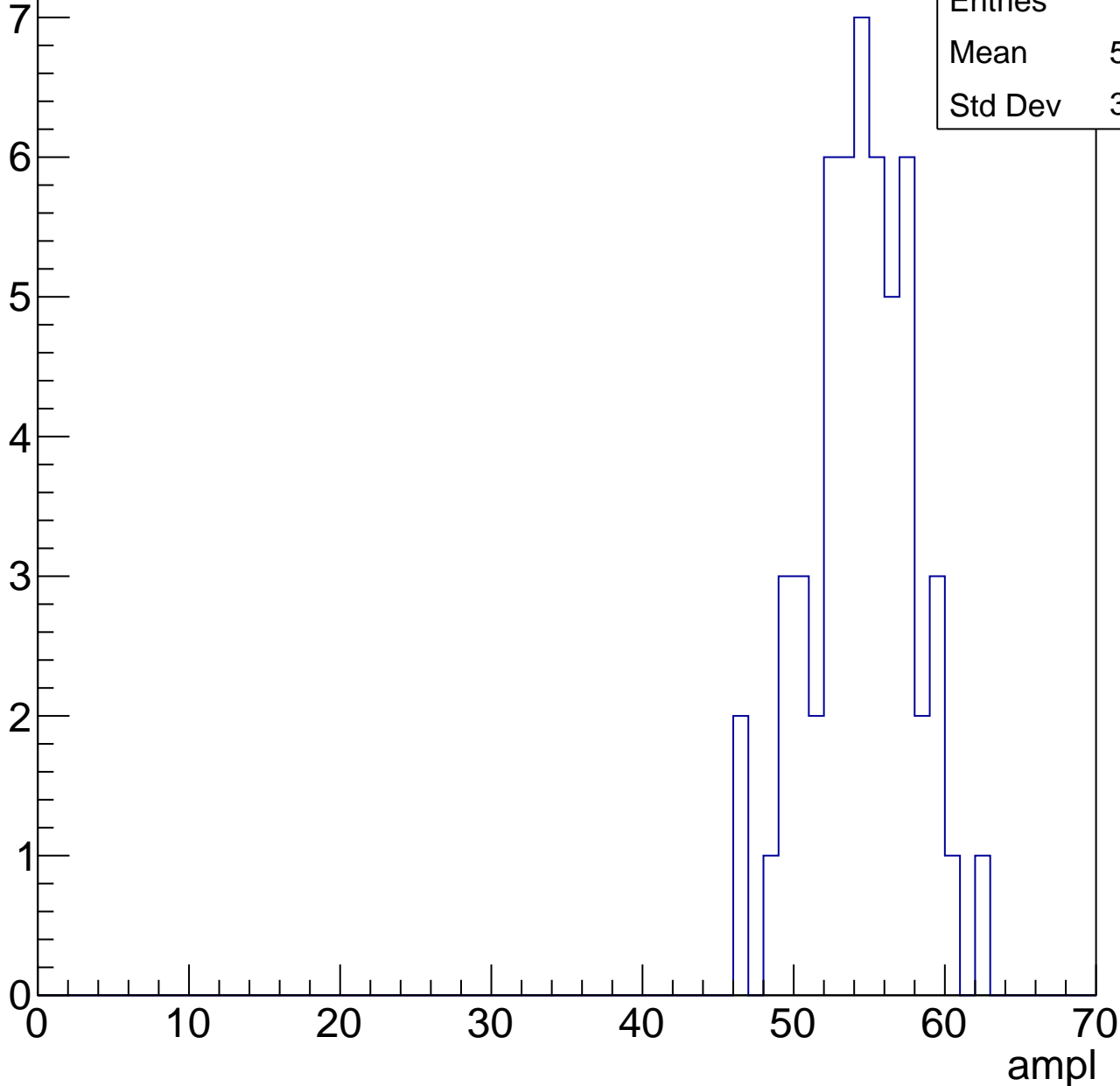


B1L103S, U7-ch64, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	53.96
Std Dev	3.394



B1L103S, U7-ch64, adc5

calib_packv5_041523_1651.root, FC#0, port C2

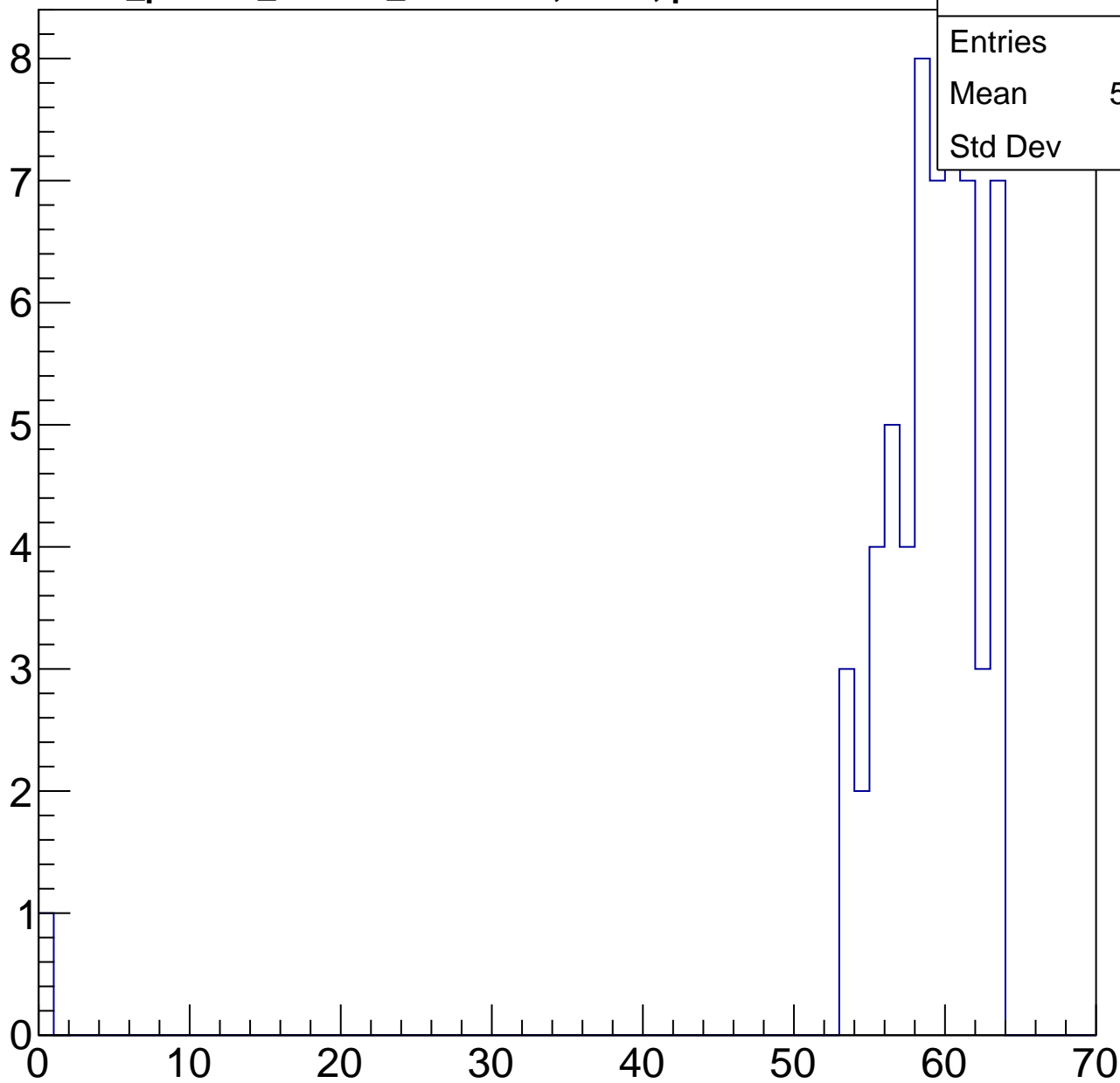
Entry

8
7
6
5
4
3
2
1
0

Entries	59
Mean	57.73
Std Dev	8.08

ampl

0 10 20 30 40 50 60 70

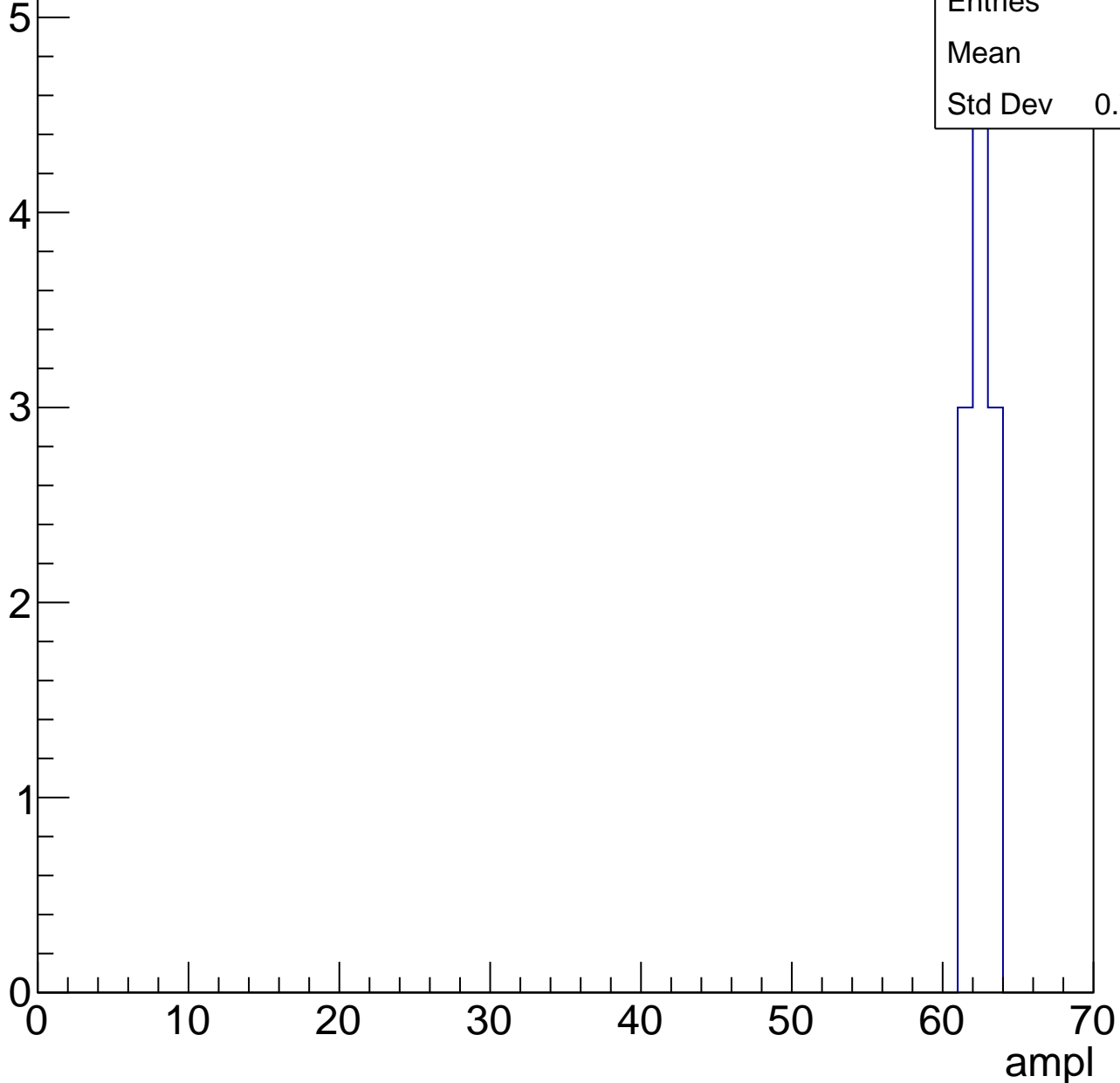


B1L103S, U7-ch64, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

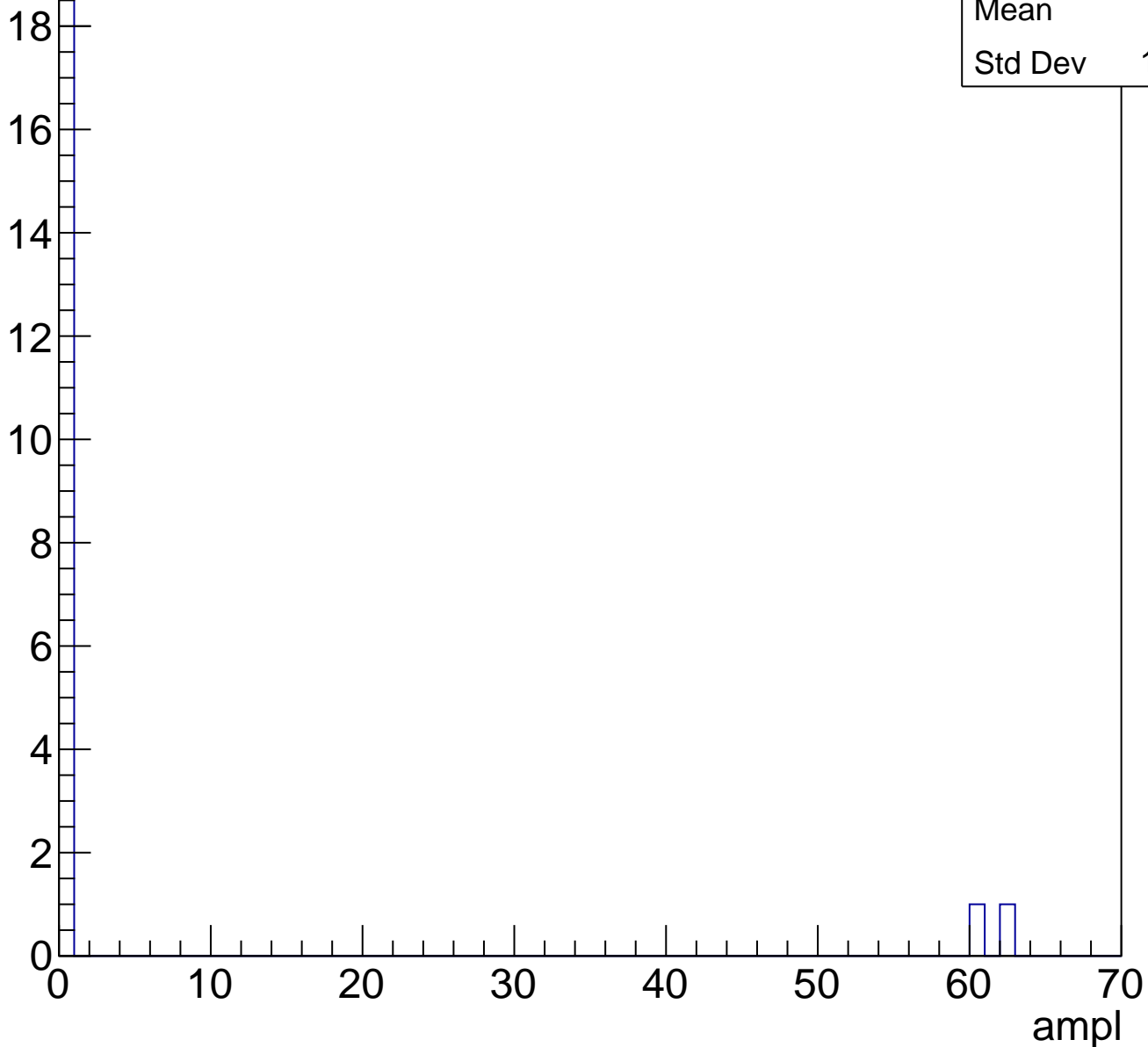
Entries	11
Mean	62
Std Dev	0.7385



B1L103S, U7-ch64, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	21
Mean	5.81
Std Dev	17.91

B1L103S, U7-ch65, adc0

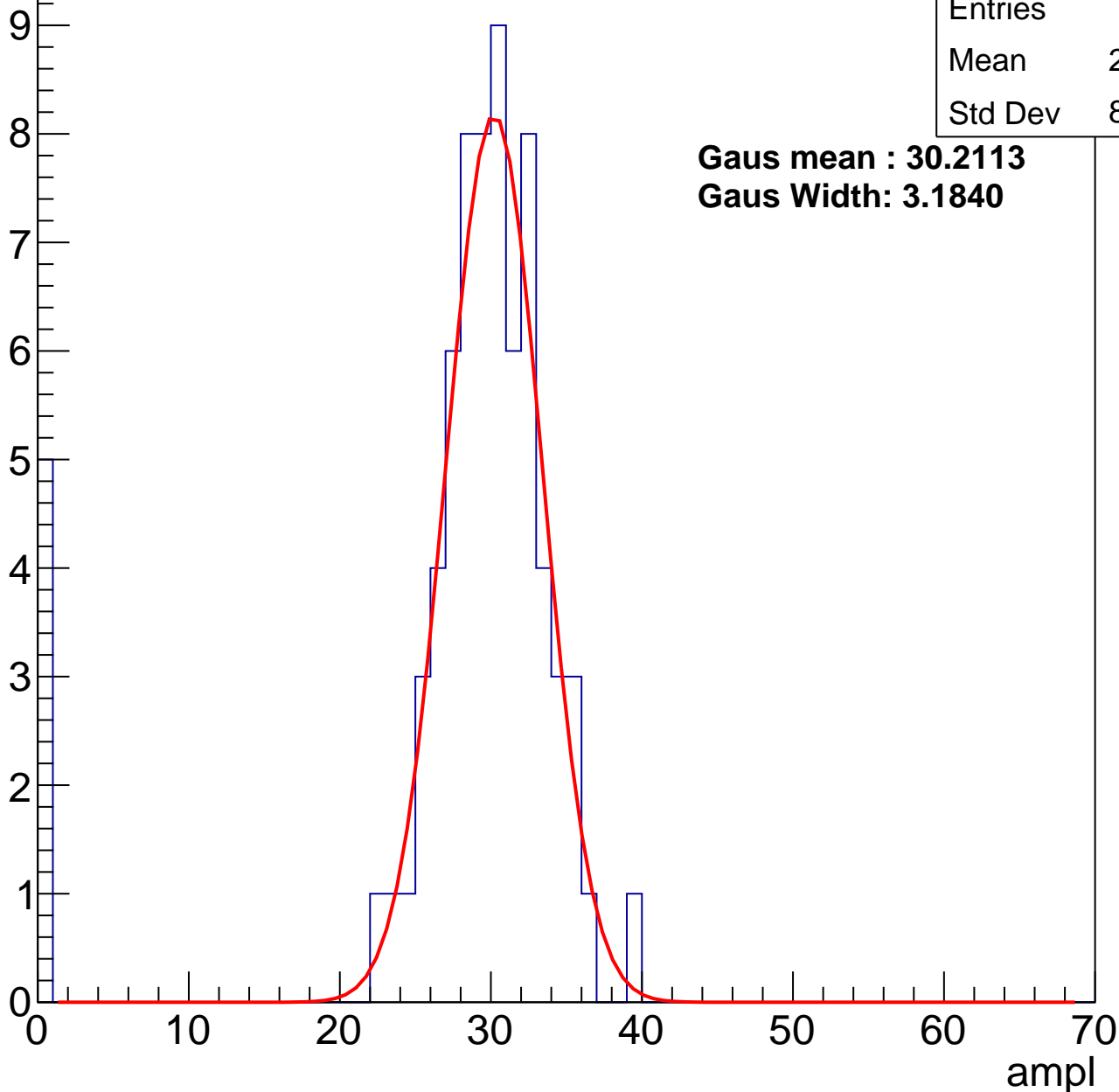
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	27.67
Std Dev	8.168

Gaus mean : 30.2113

Gaus Width: 3.1840



B1L103S, U7-ch65, adc1

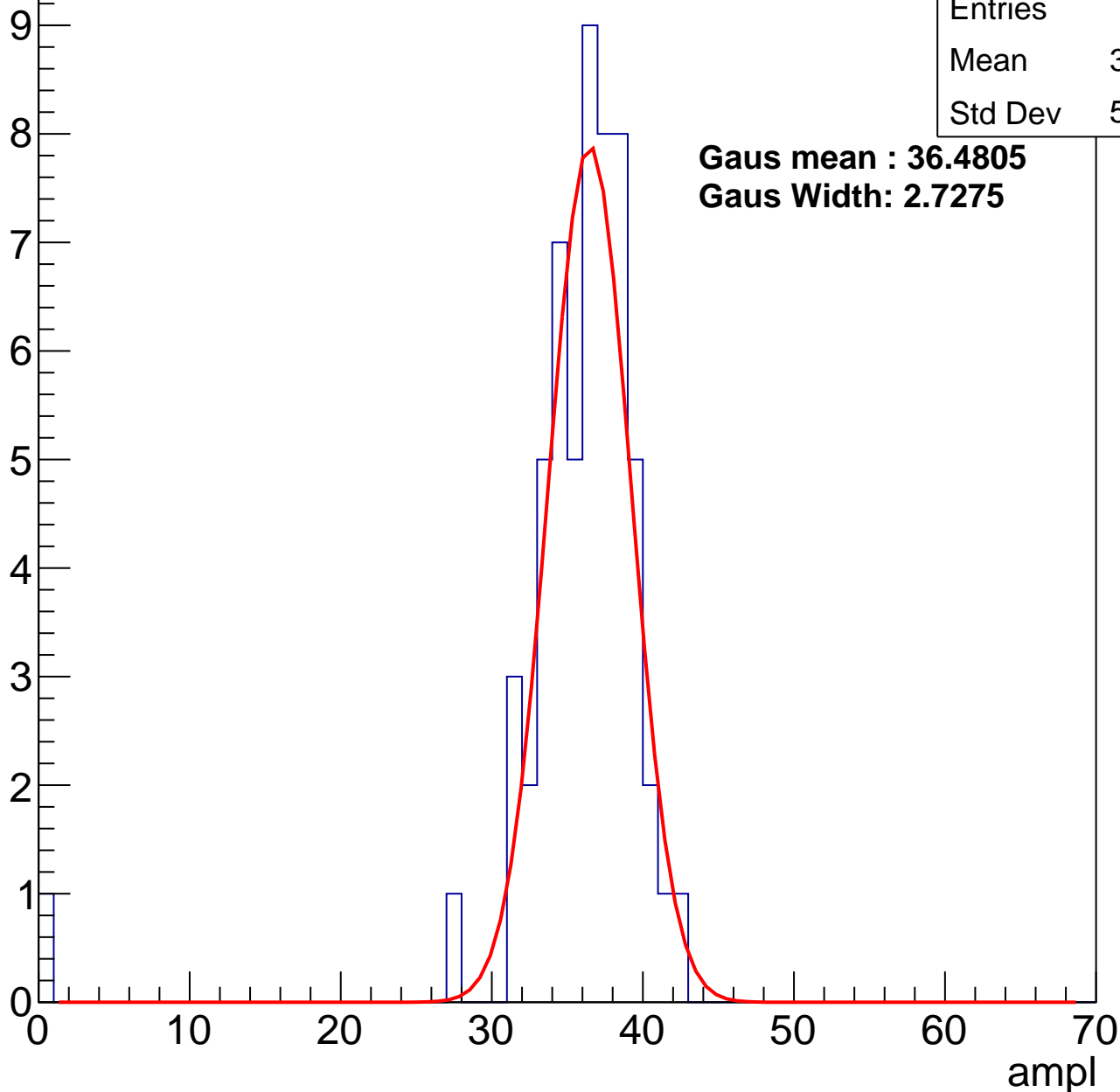
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	35.24
Std Dev	5.424

Gaus mean : 36.4805

Gaus Width: 2.7275



B1L103S, U7-ch65, adc2

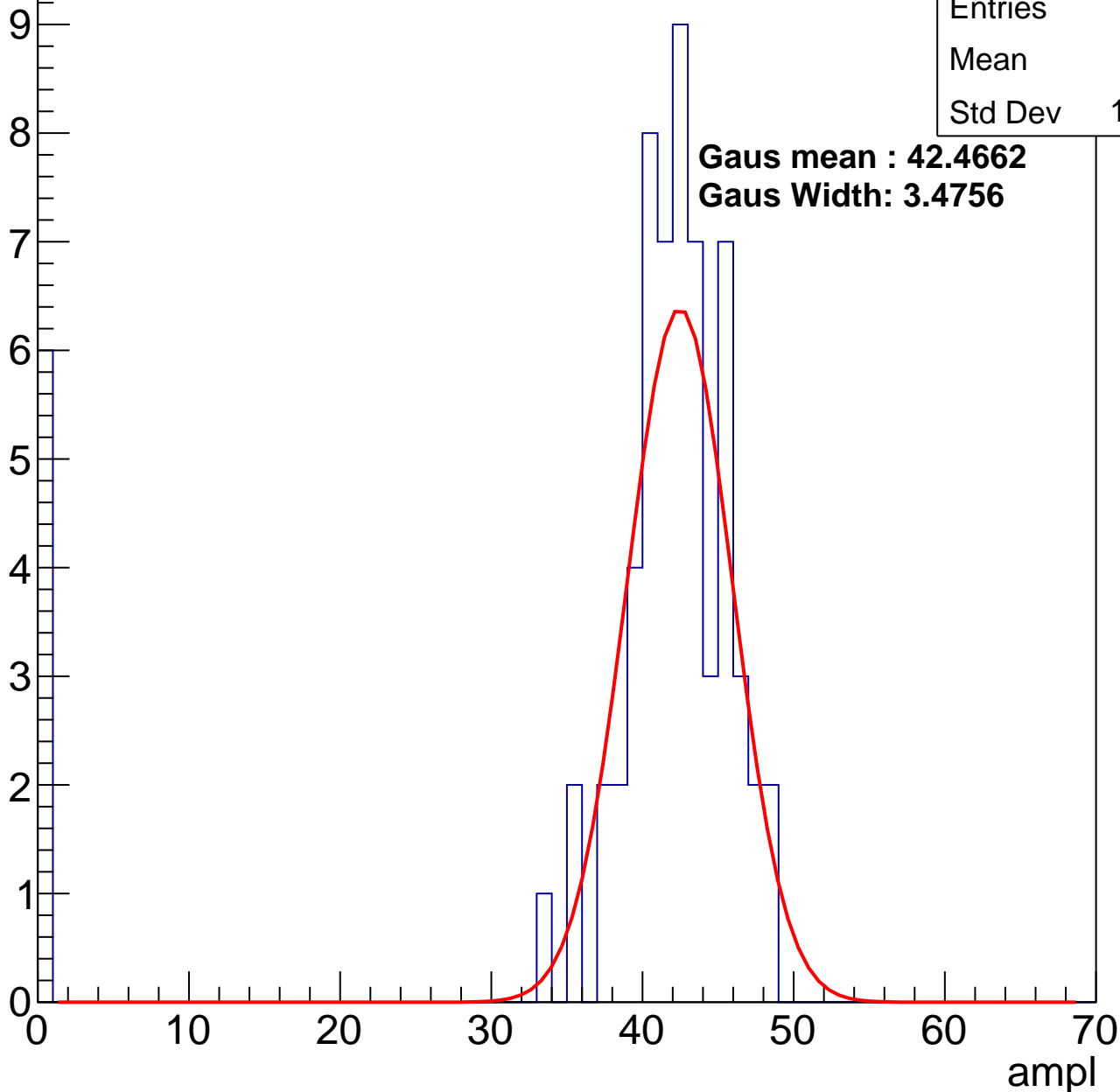
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	38
Std Dev	12.49

Gaus mean : 42.4662

Gaus Width: 3.4756

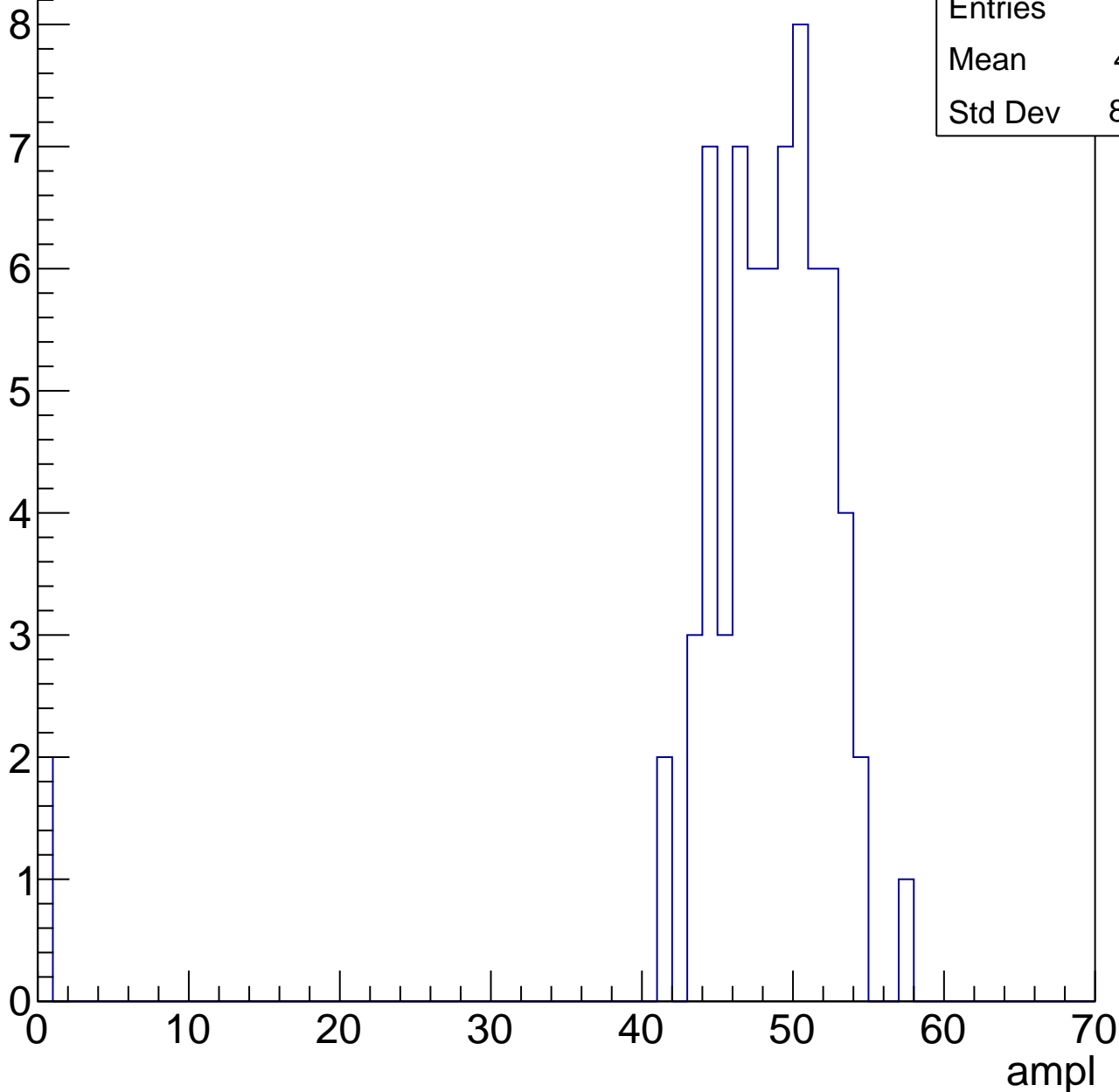


B1L103S, U7-ch65, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	46.91
Std Dev	8.712

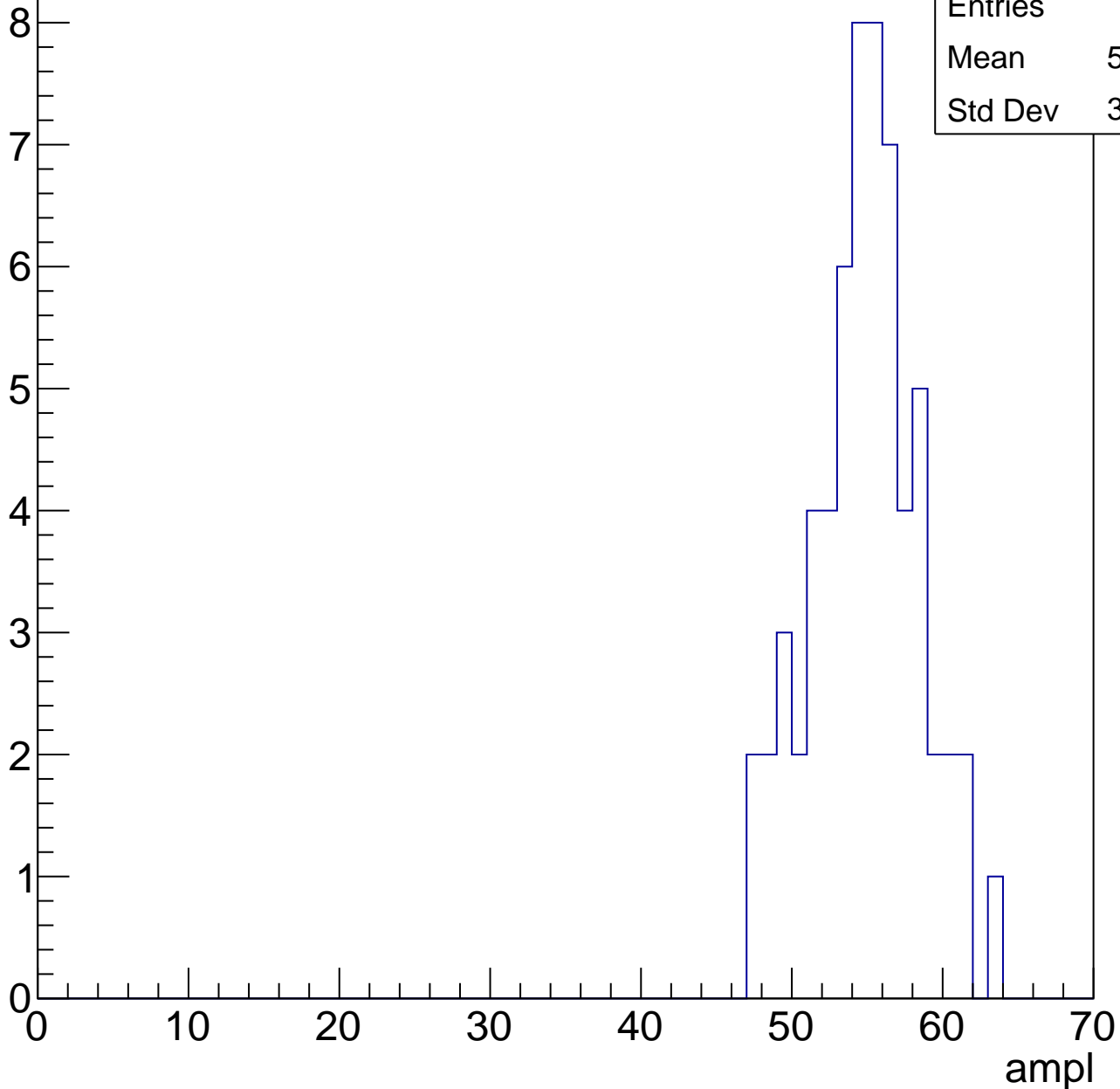


B1L103S, U7-ch65, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	54.39
Std Dev	3.544



B1L103S, U7-ch65, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

8
7
6
5
4
3
2
1
0

Entries	54
Mean	58.7
Std Dev	8.37

ampl

0

10

20

30

40

50

60

70

B1L103S, U7-ch65, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	4
Mean	62
Std Dev	1.225

ampl

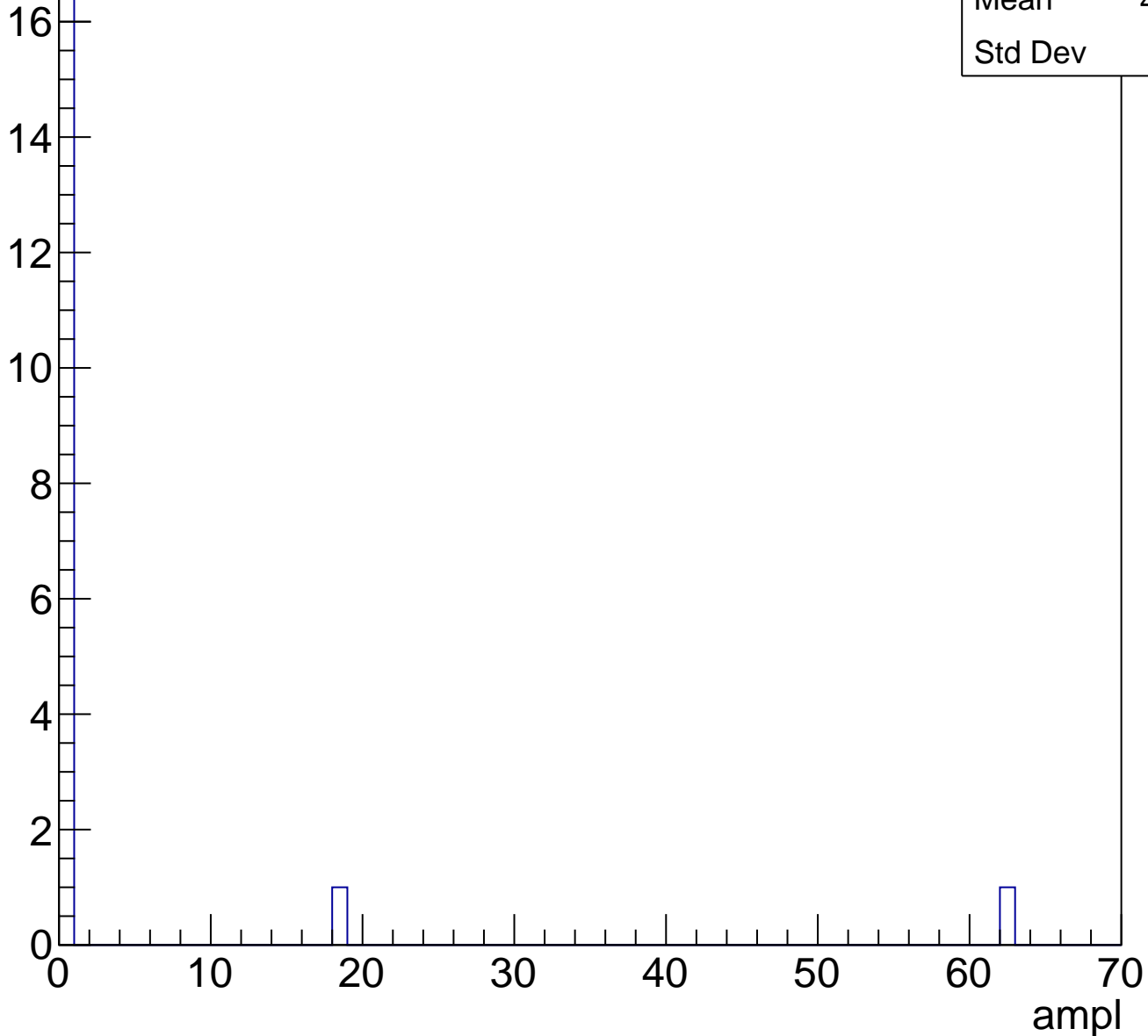
0 10 20 30 40 50 60 70

B1L103S, U7-ch65, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	4.211
Std Dev	14.2

Entry



B1L103S, U7-ch66, adc0

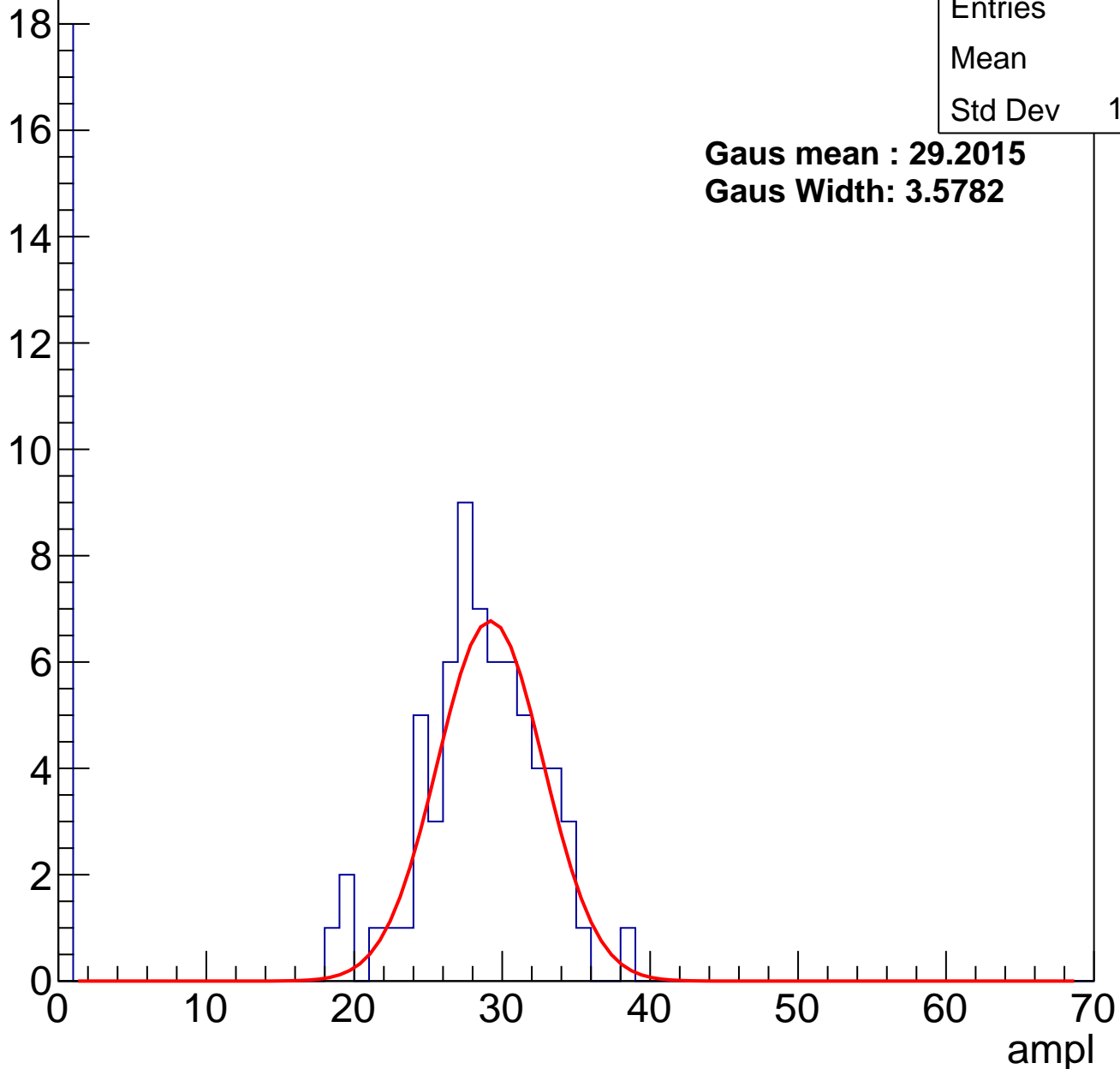
calib_packv5_041523_1651.root, FC#0, port C2

Entries	84
Mean	22.1
Std Dev	12.05

Gaus mean : 29.2015

Gaus Width: 3.5782

Entry



B1L103S, U7-ch66, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	95
Mean	30.52
Std Dev	13.08

Gaus mean : 36.4728

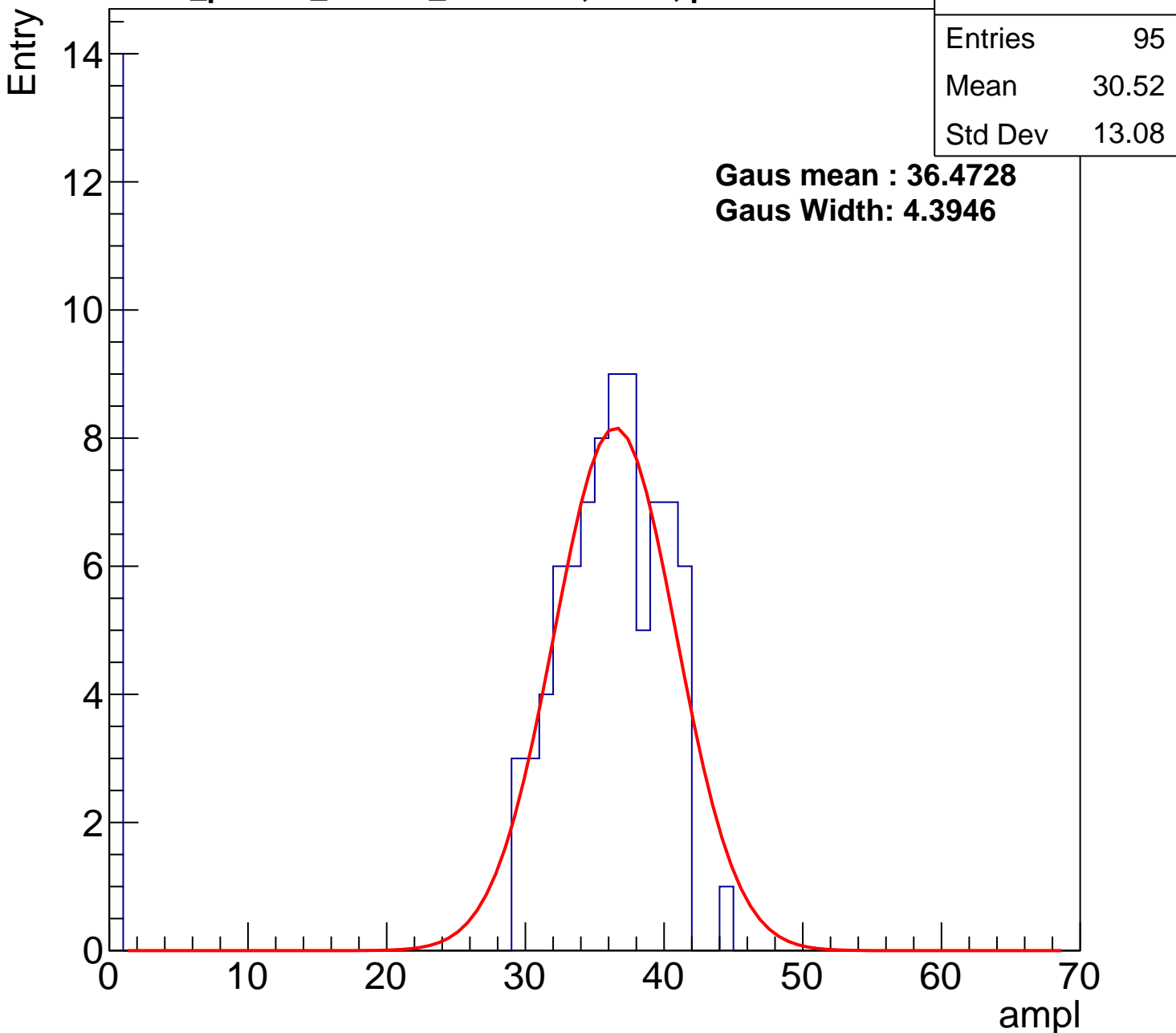
Gaus Width: 4.3946

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U7-ch66, adc2

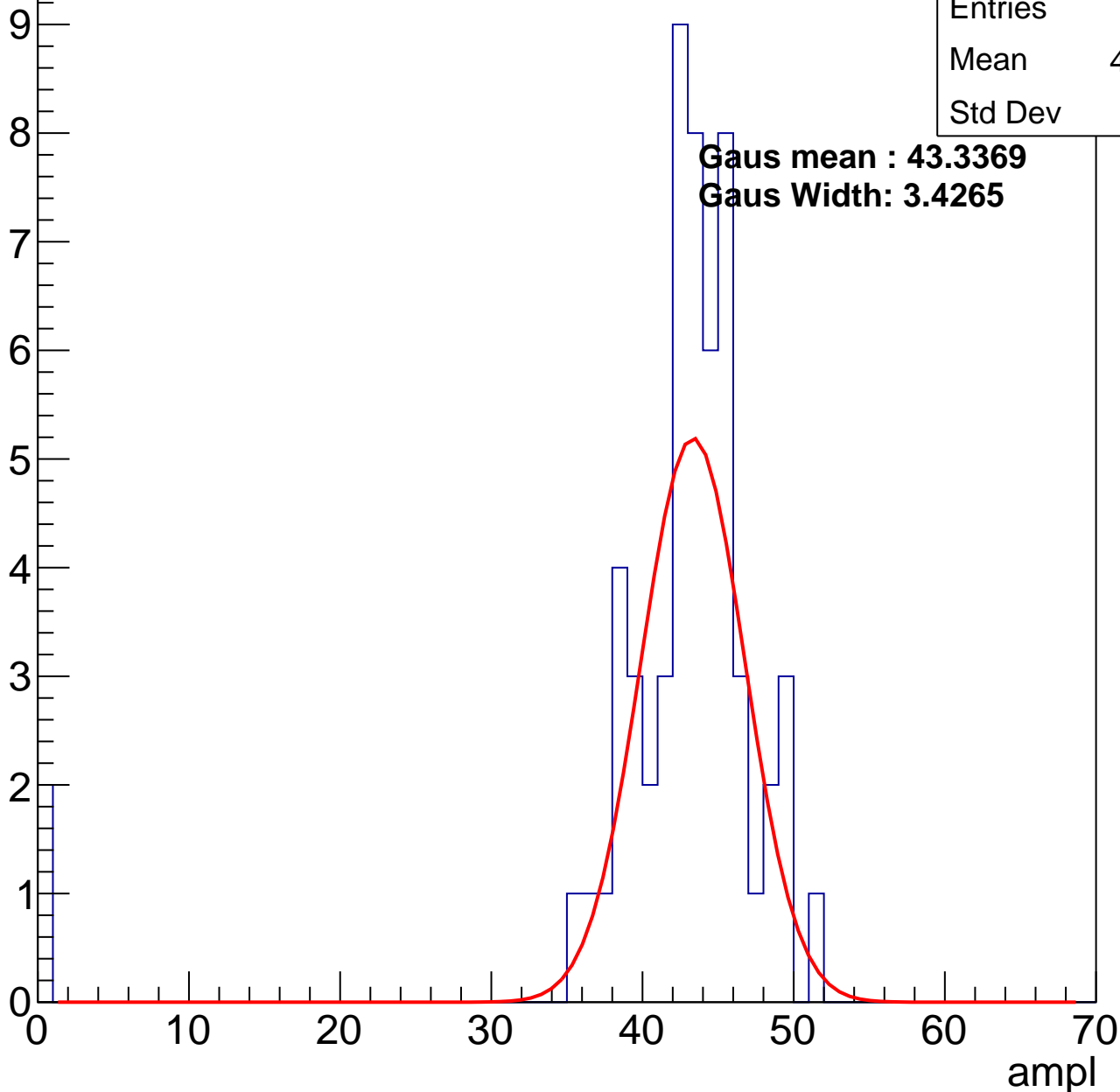
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	41.47
Std Dev	8.51

Gaus mean : 43.3369

Gaus Width: 3.4265

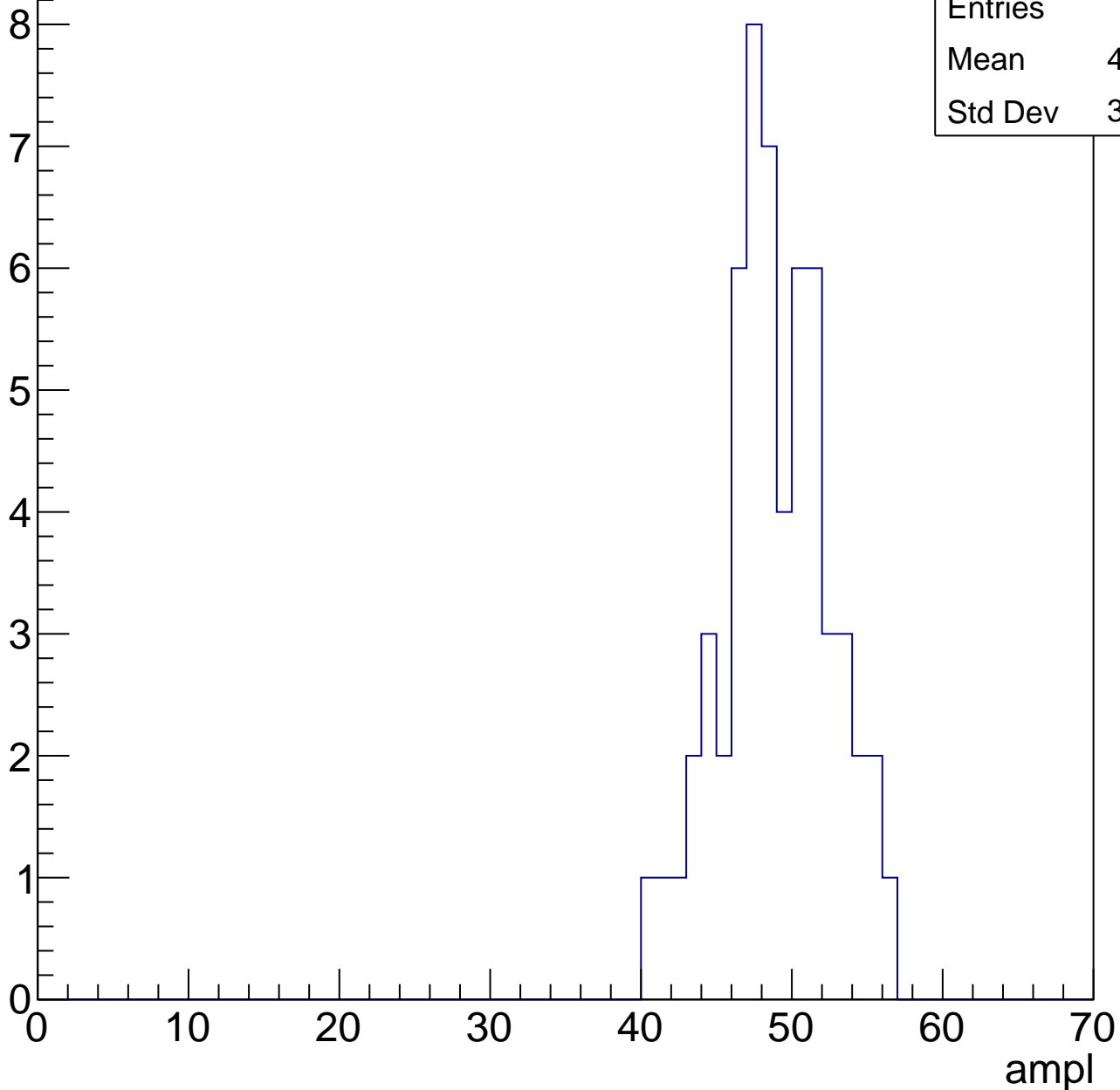


B1L103S, U7-ch66, adc3

calib_packv5_041523_1651.root, FC#0, port C2

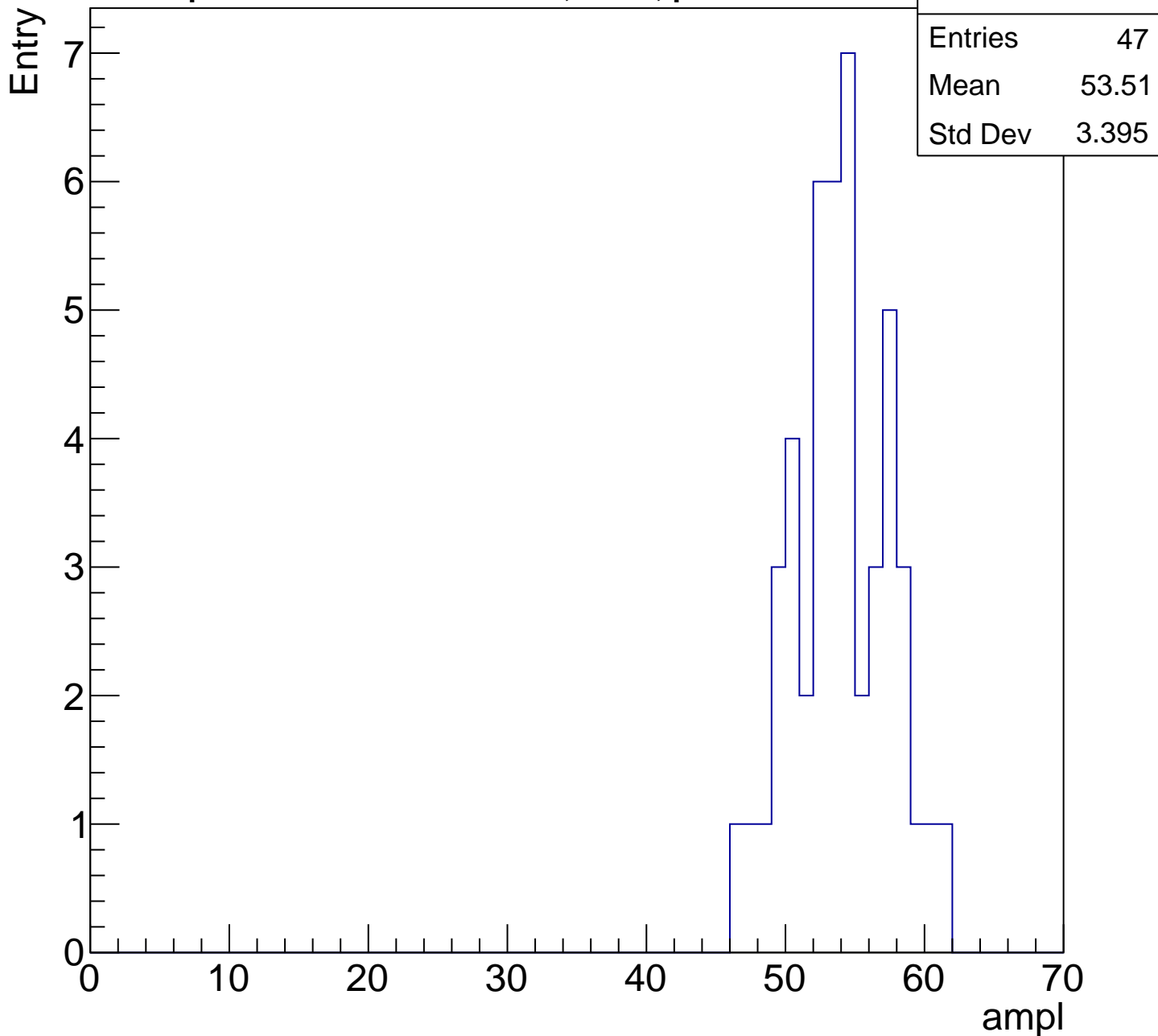
Entry

Entries	58
Mean	48.45
Std Dev	3.534



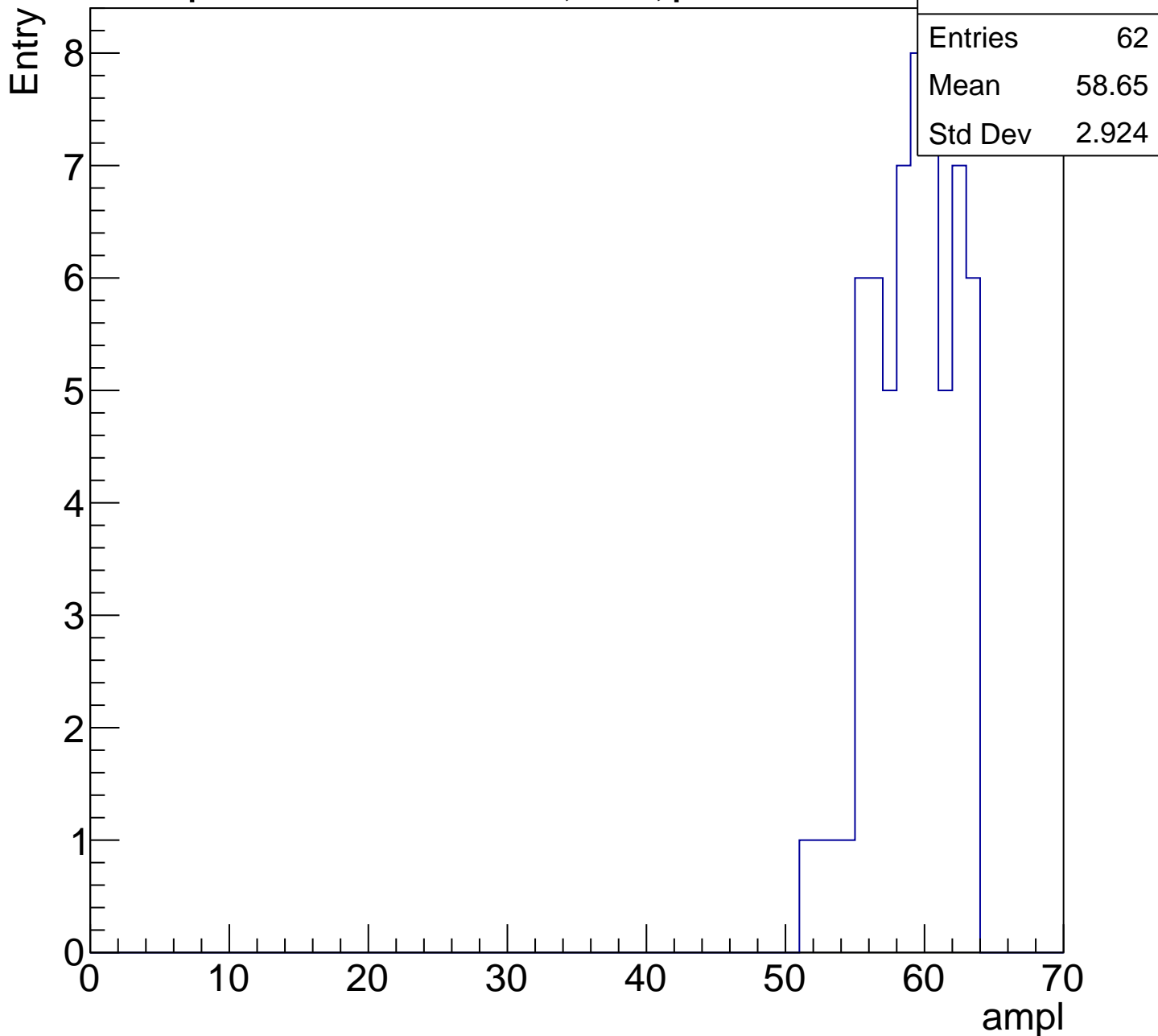
B1L103S, U7-ch66, adc4

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U7-ch66, adc5

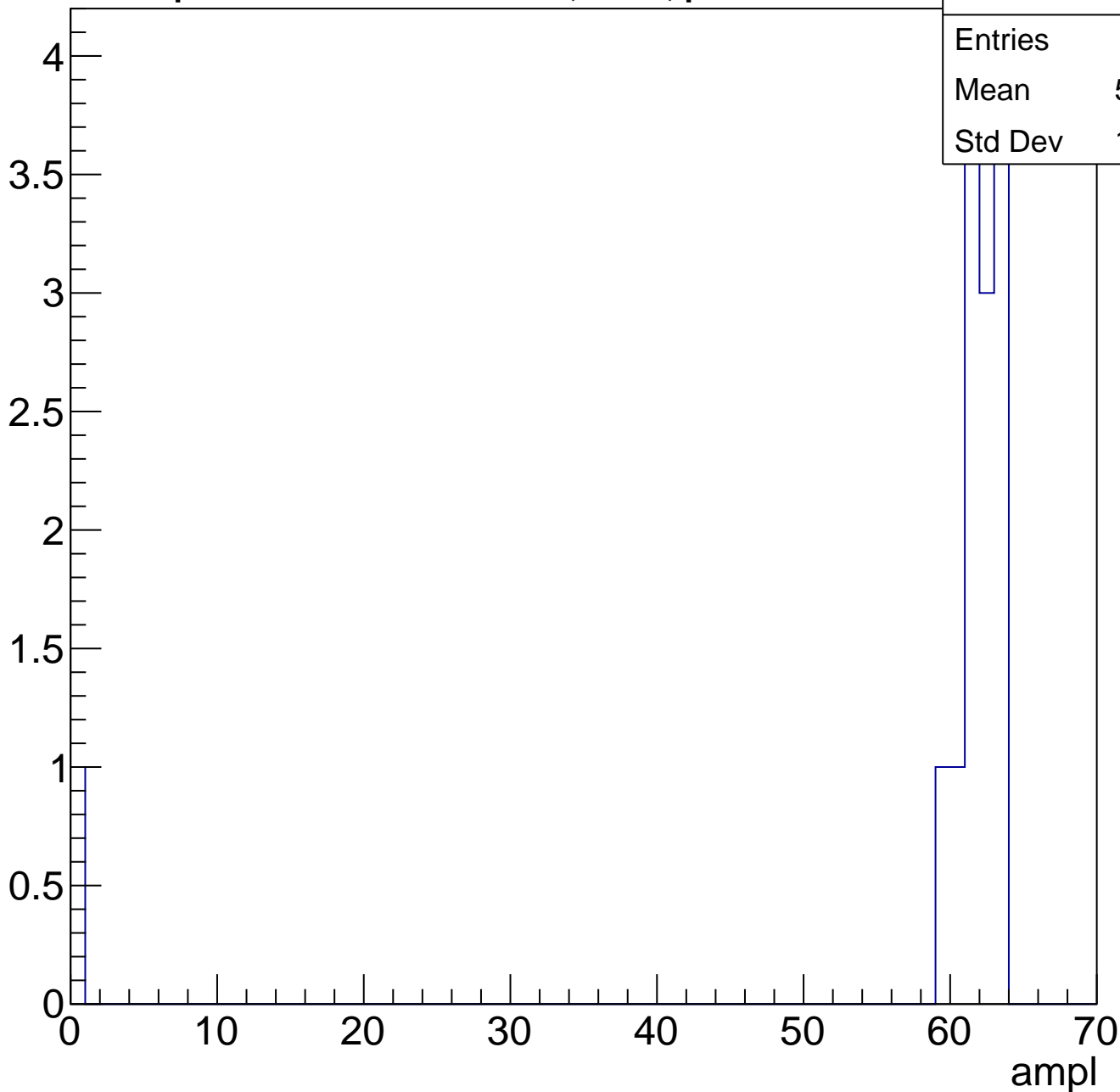
calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U7-ch66, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch66, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U7-ch67, adc0

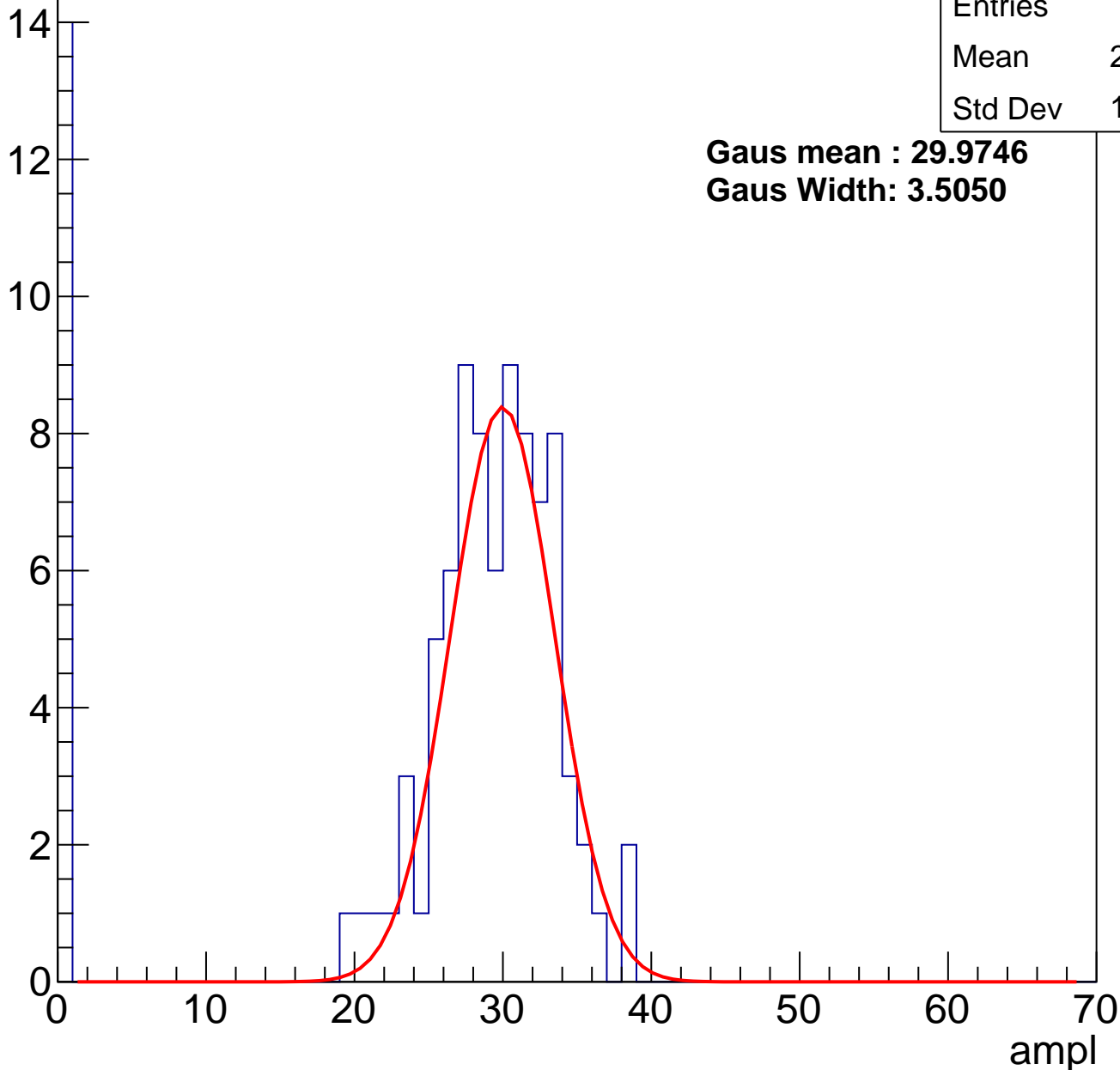
calib_packv5_041523_1651.root, FC#0, port C2

Entries	96
Mean	24.86
Std Dev	10.86

Gaus mean : 29.9746

Gaus Width: 3.5050

Entry



B1L103S, U7-ch67, adc1

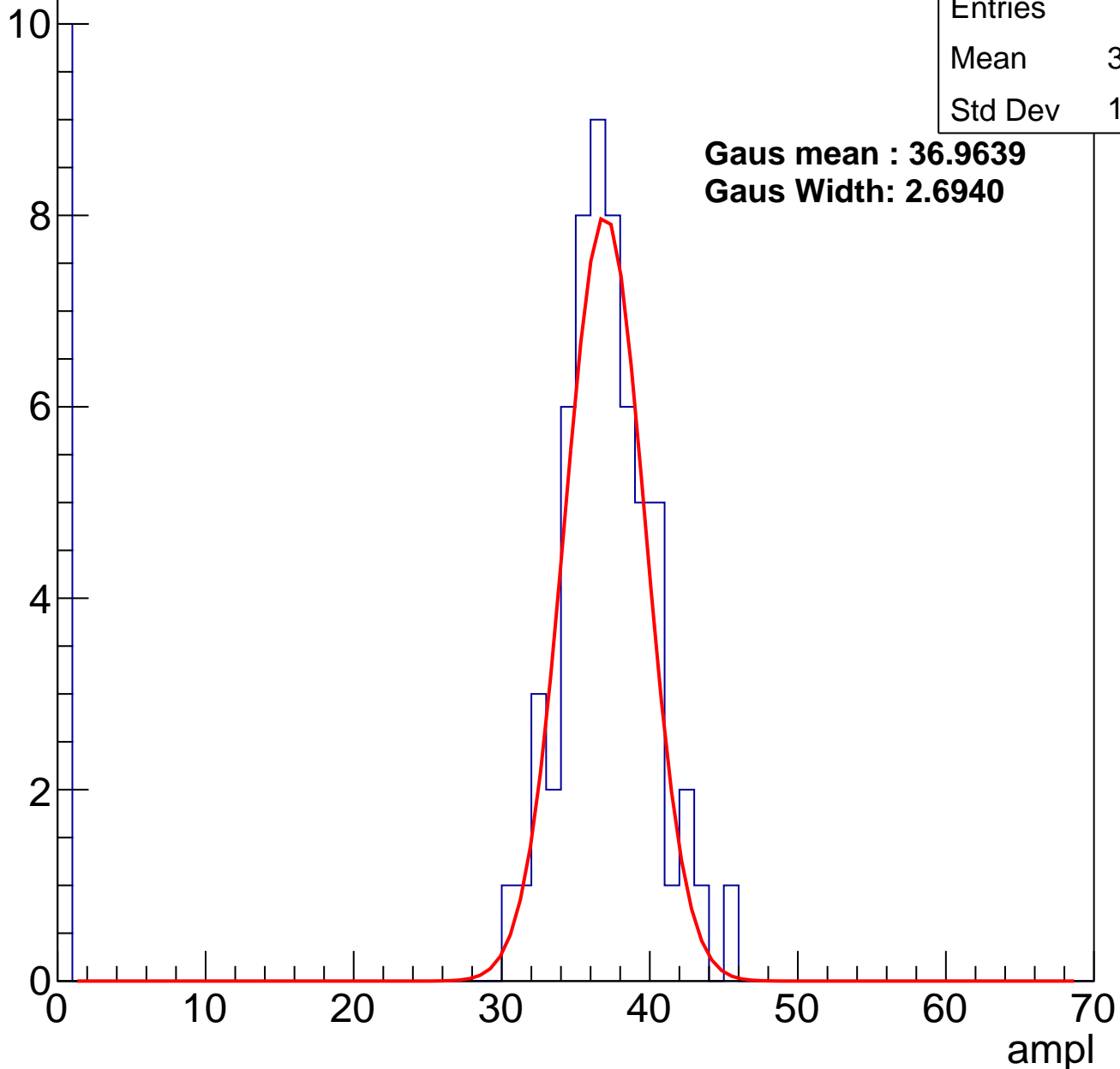
calib_packv5_041523_1651.root, FC#0, port C2

Entries	69
Mean	31.35
Std Dev	13.19

Gaus mean : 36.9639

Gaus Width: 2.6940

Entry



B1L103S, U7-ch67, adc2

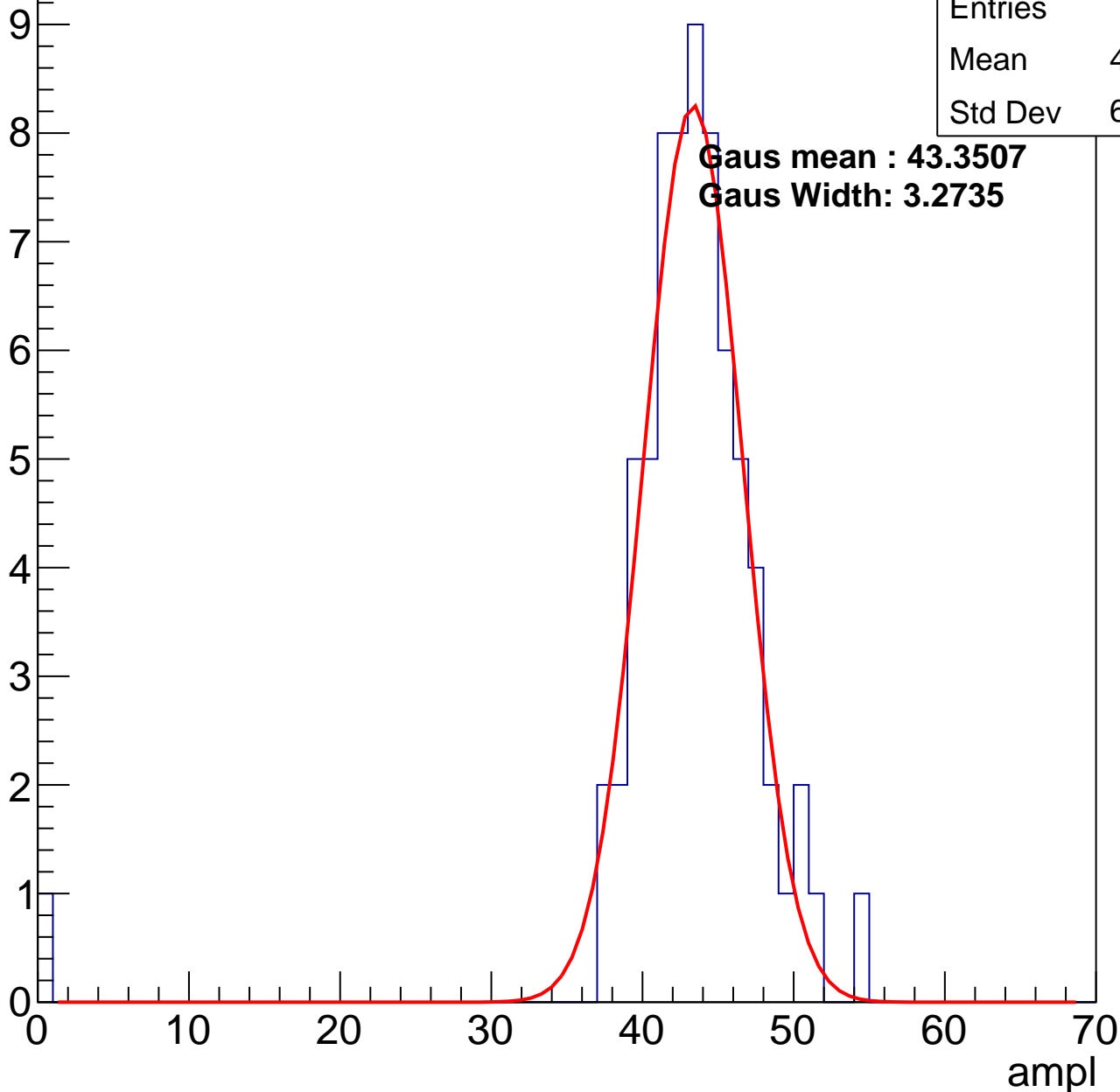
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	42.66
Std Dev	6.139

Gaus mean : 43.3507

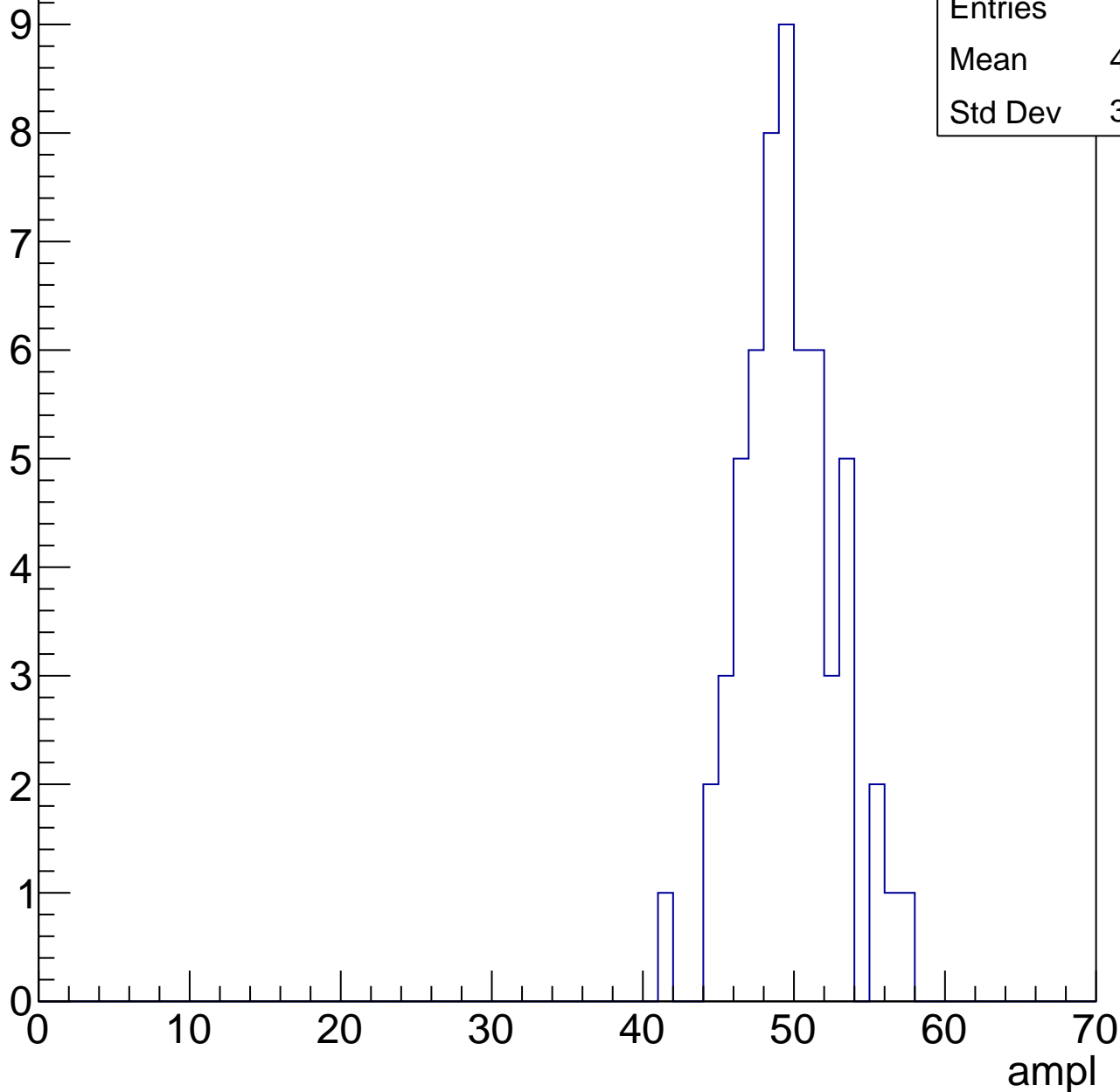
Gaus Width: 3.2735



B1L103S, U7-ch67, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry



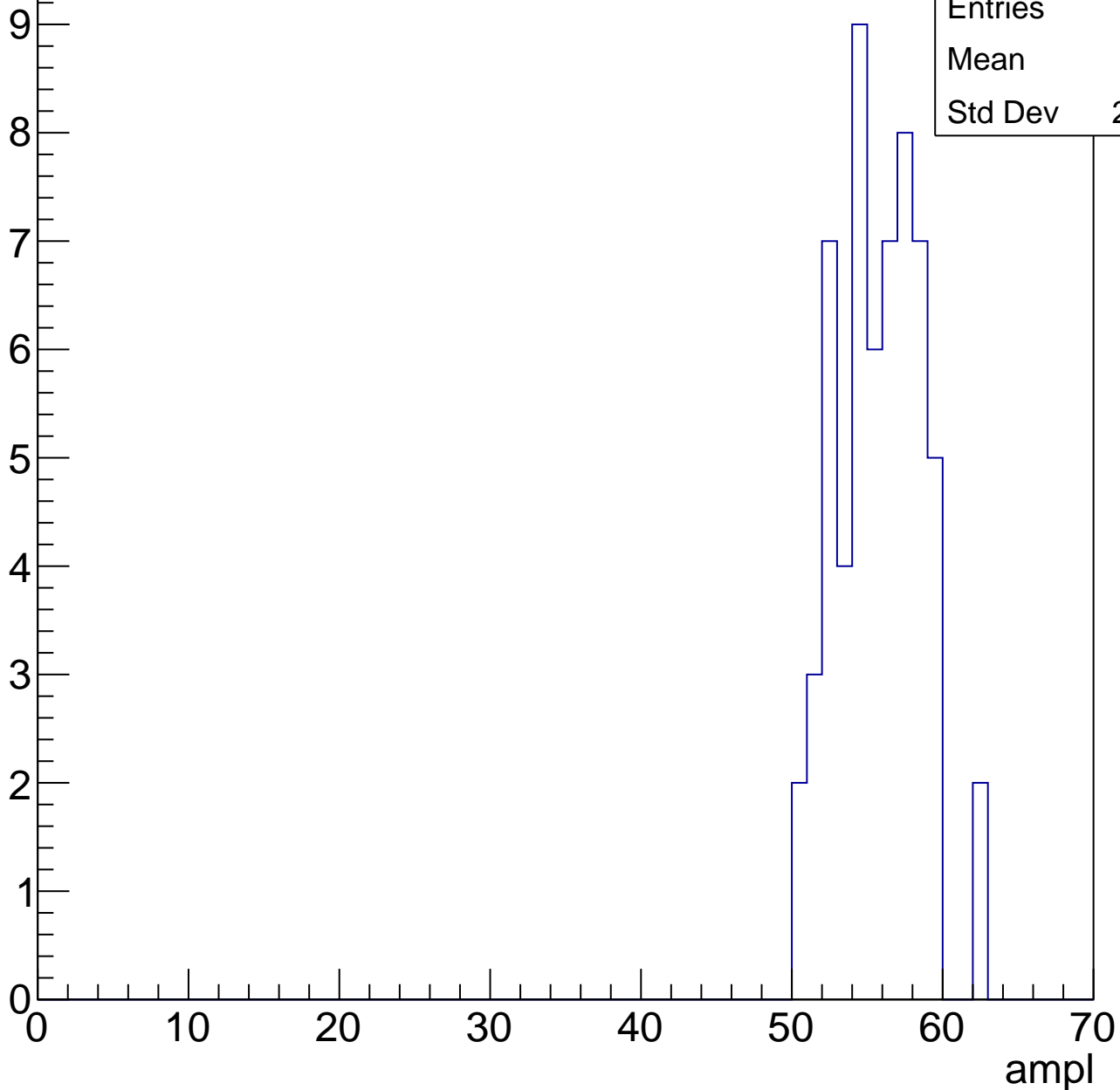
Entries	58
Mean	49.16
Std Dev	3.106

B1L103S, U7-ch67, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	55.3
Std Dev	2.771



B1L103S, U7-ch67, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

10

Entries 45

Mean 58.69

Std Dev 9.15

8

6

4

2

0

0

10

20

30

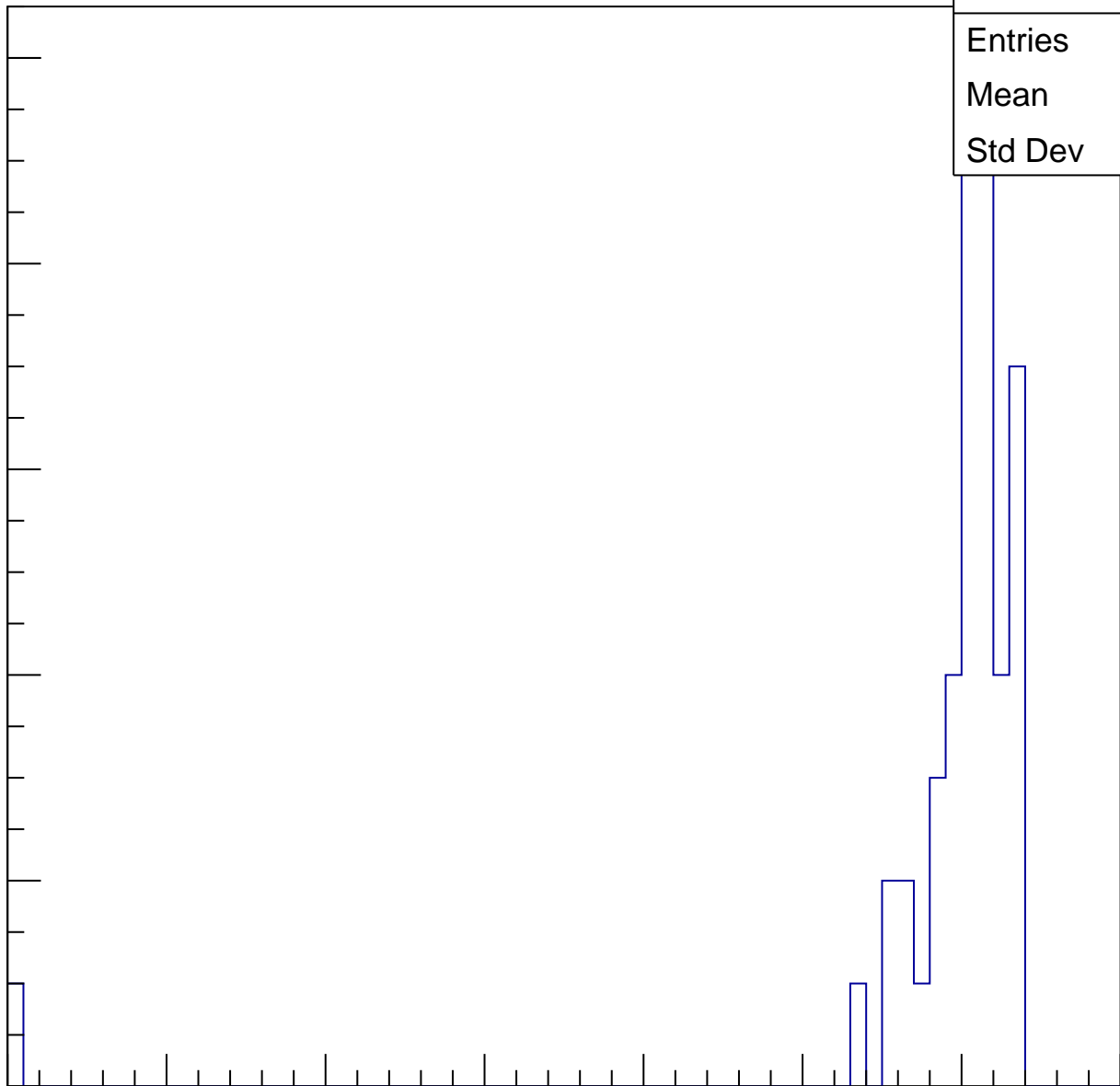
40

50

60

70

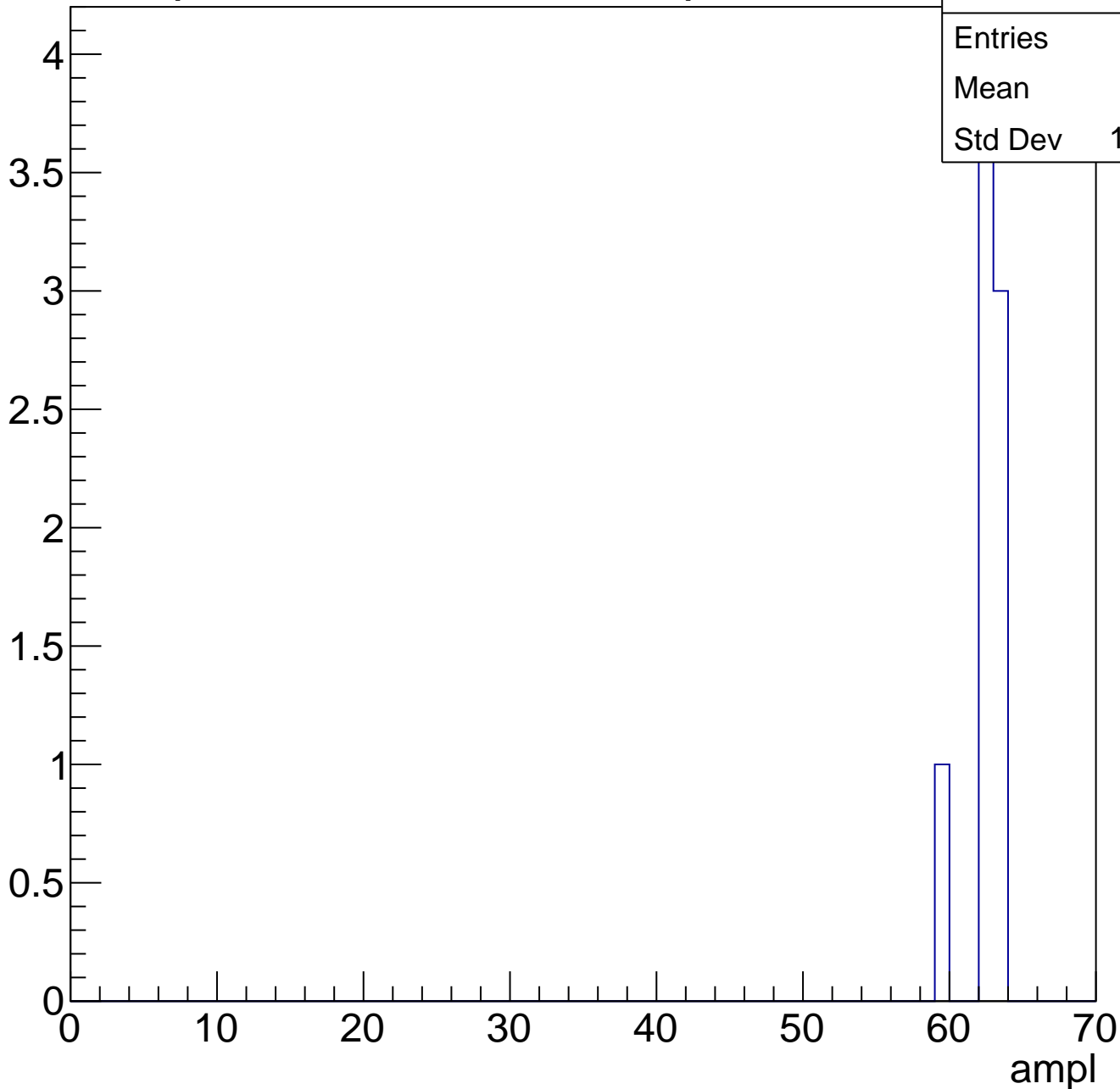
ampl



B1L103S, U7-ch67, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch67, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch68, adc0

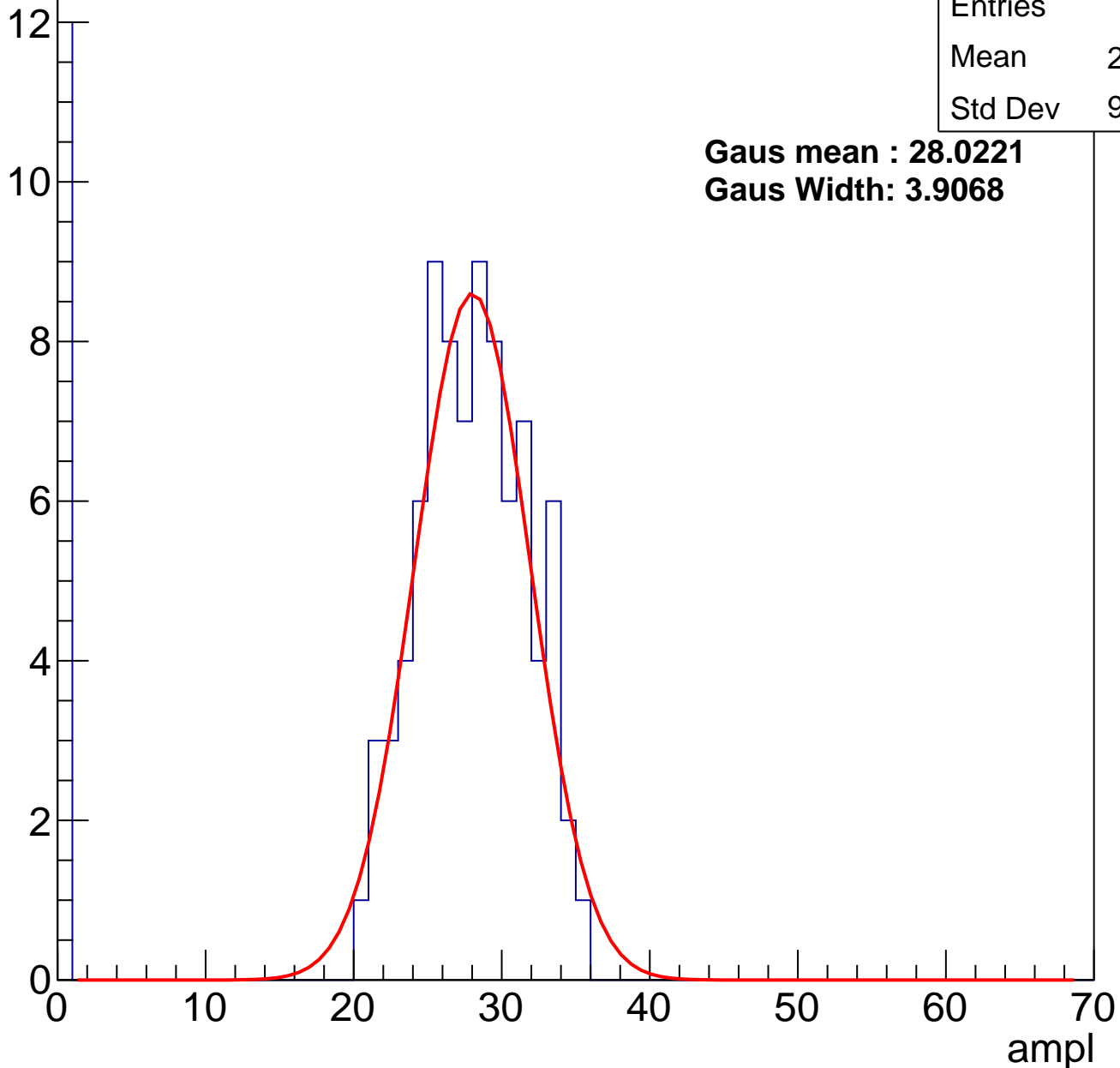
calib_packv5_041523_1651.root, FC#0, port C2

Entries	96
Mean	24.14
Std Dev	9.704

Gaus mean : 28.0221

Gaus Width: 3.9068

Entry



B1L103S, U7-ch68, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	73
Mean	29.85
Std Dev	12.93

Gaus mean : 35.7725

Gaus Width: 3.5500

Entry

10

8

6

4

2

0

0

10

20

30

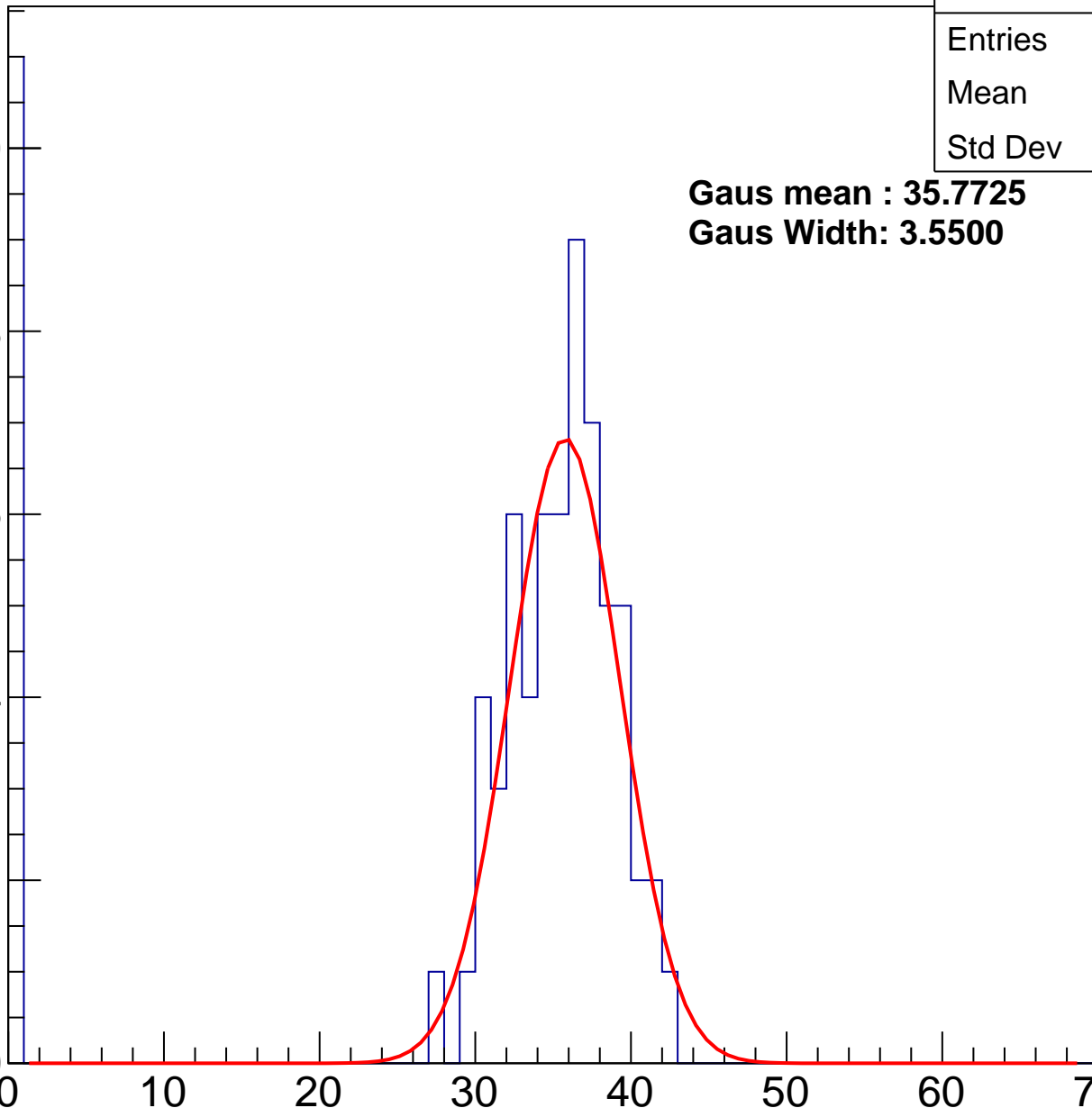
40

50

60

70

ampl



B1L103S, U7-ch68, adc2

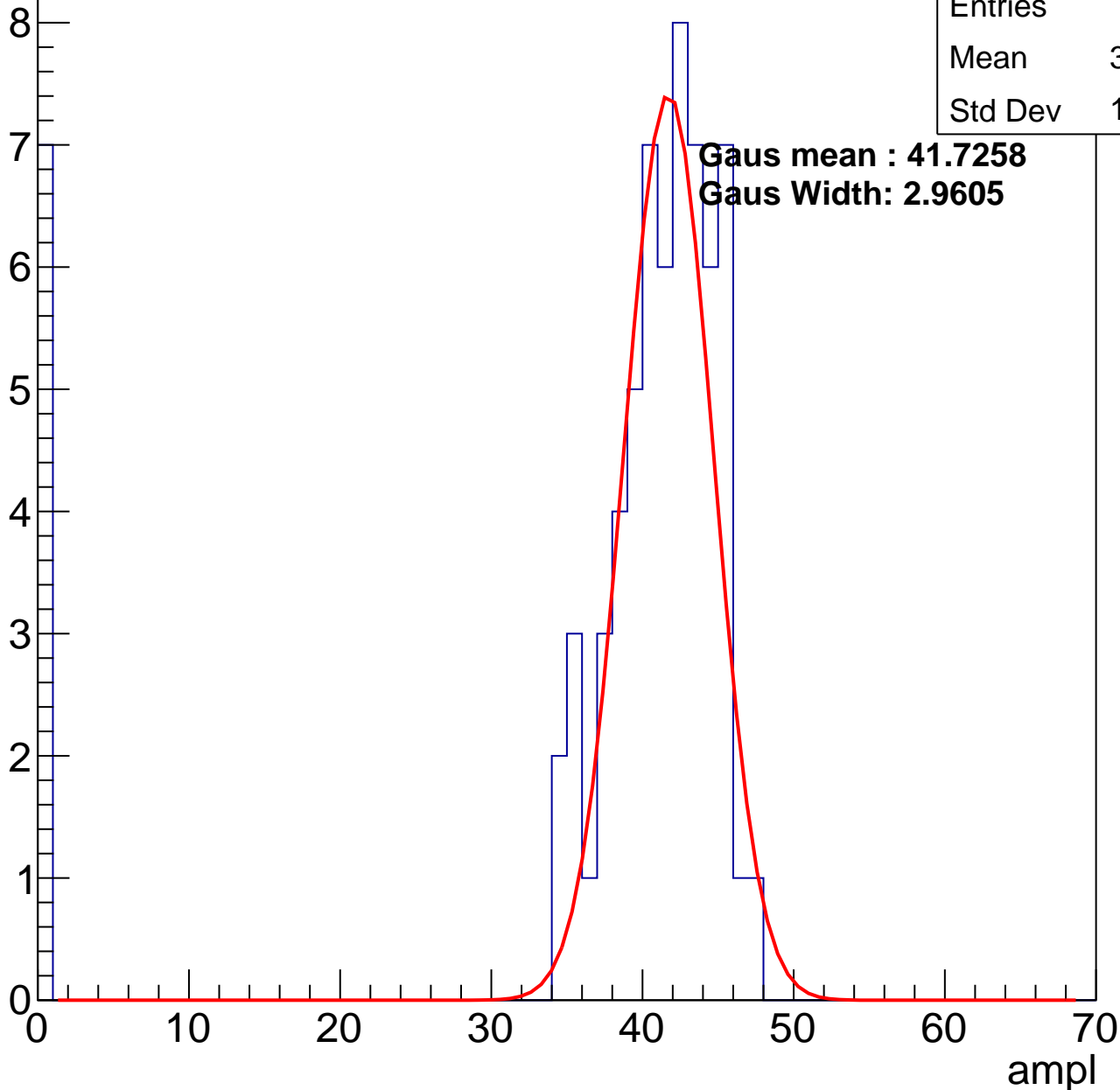
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	36.79
Std Dev	12.82

Gaus mean : 41.7258

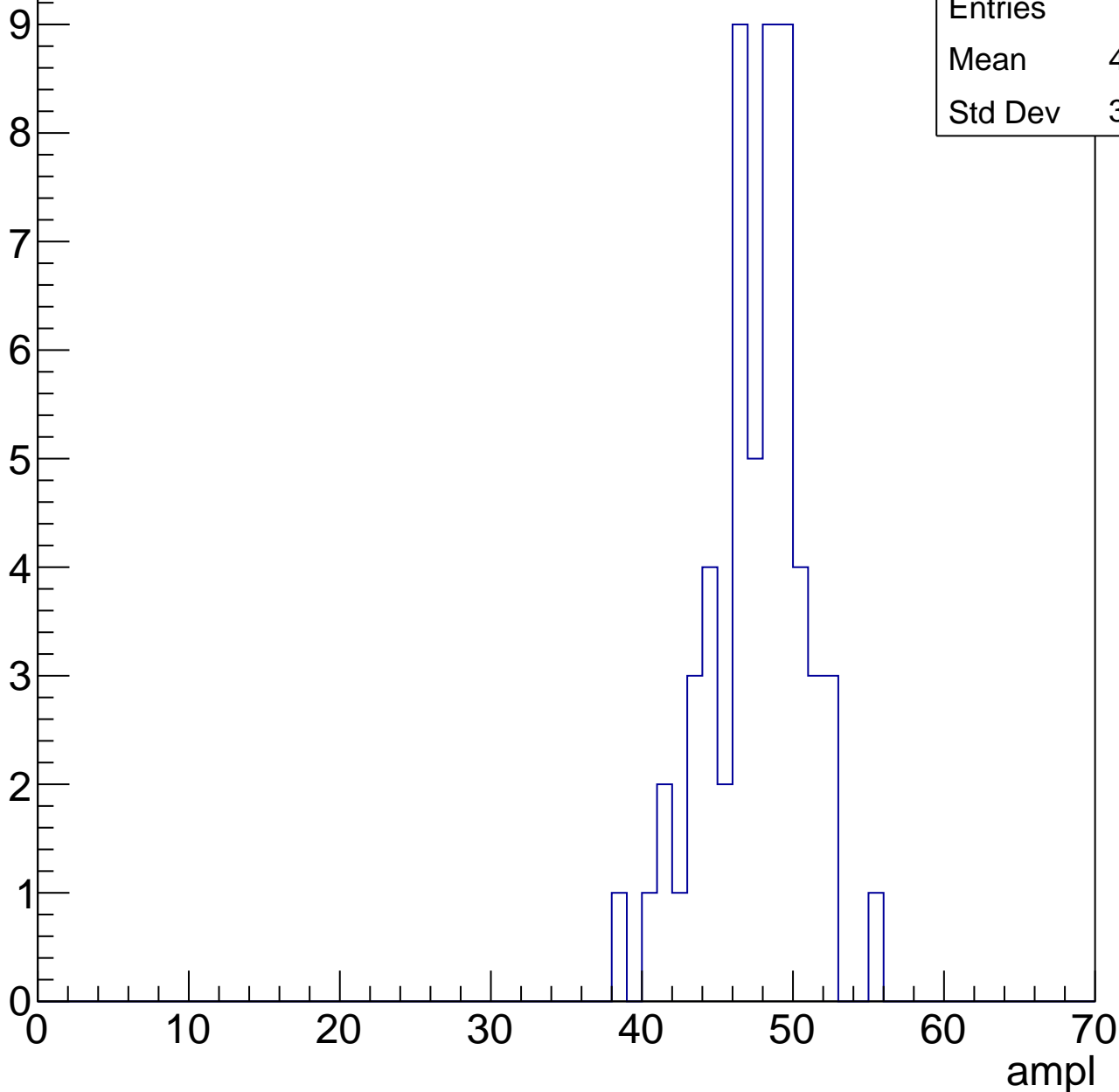
Gaus Width: 2.9605



B1L103S, U7-ch68, adc3

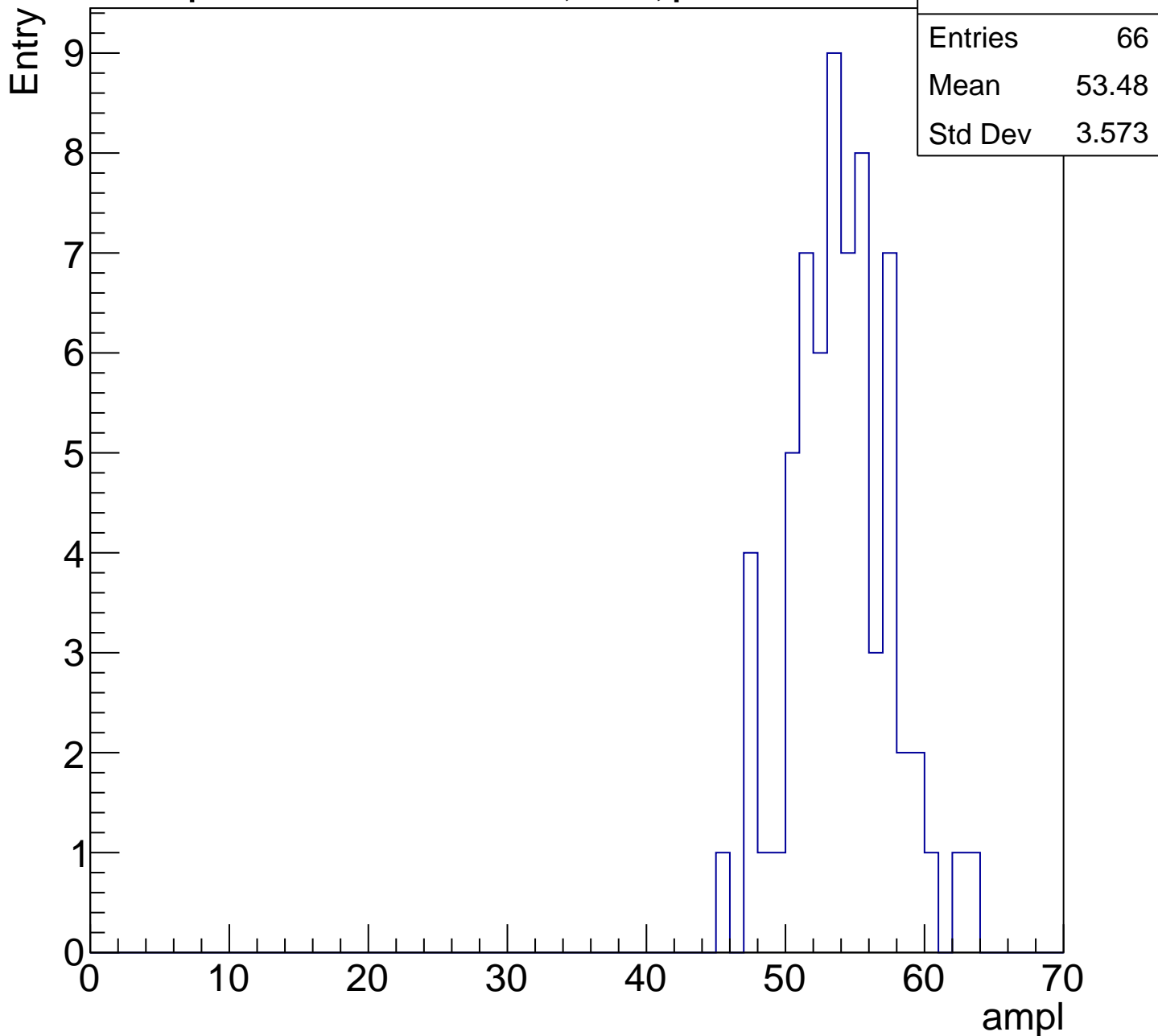
calib_packv5_041523_1651.root, FC#0, port C2

Entry



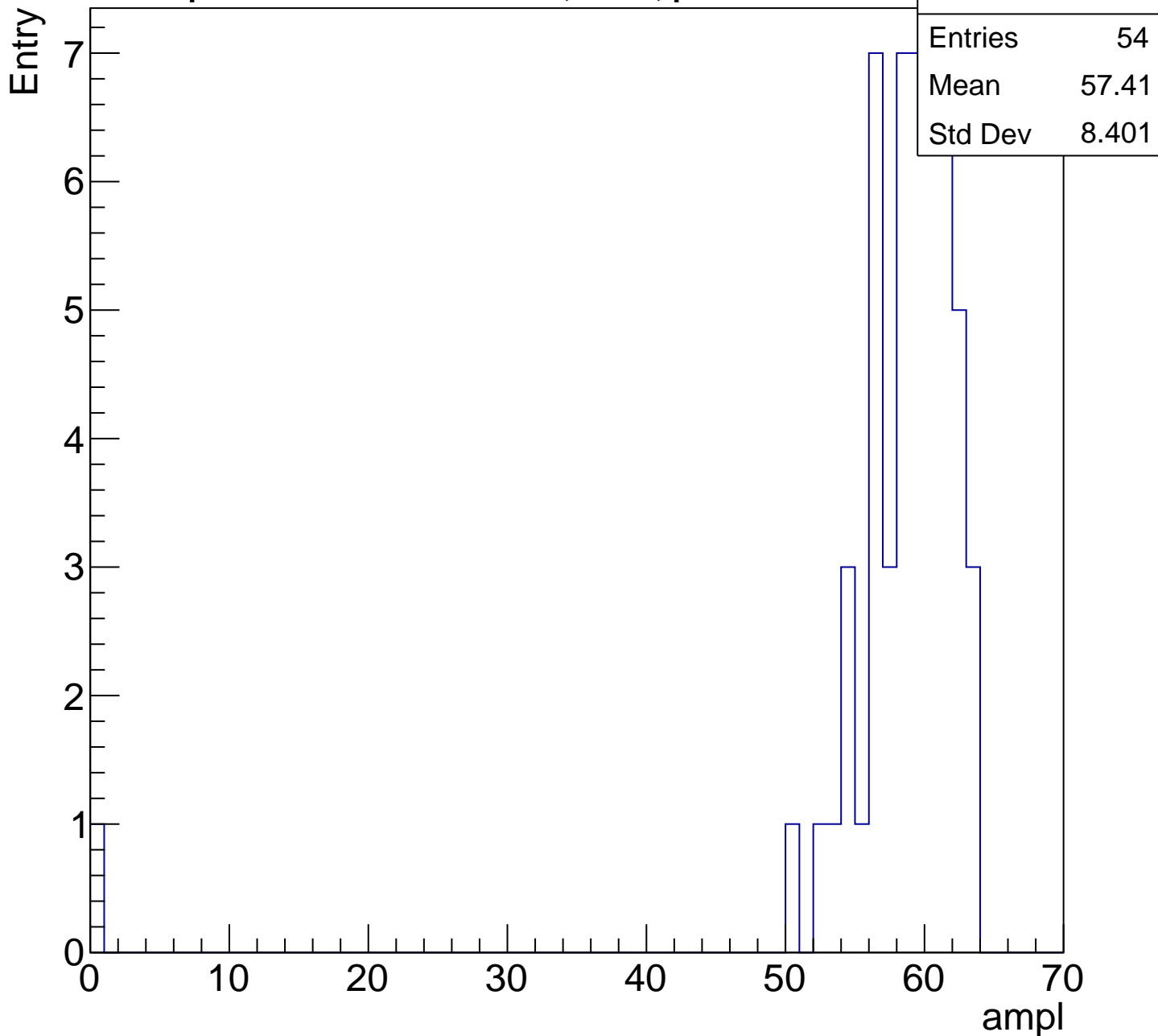
B1L103S, U7-ch68, adc4

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U7-ch68, adc5

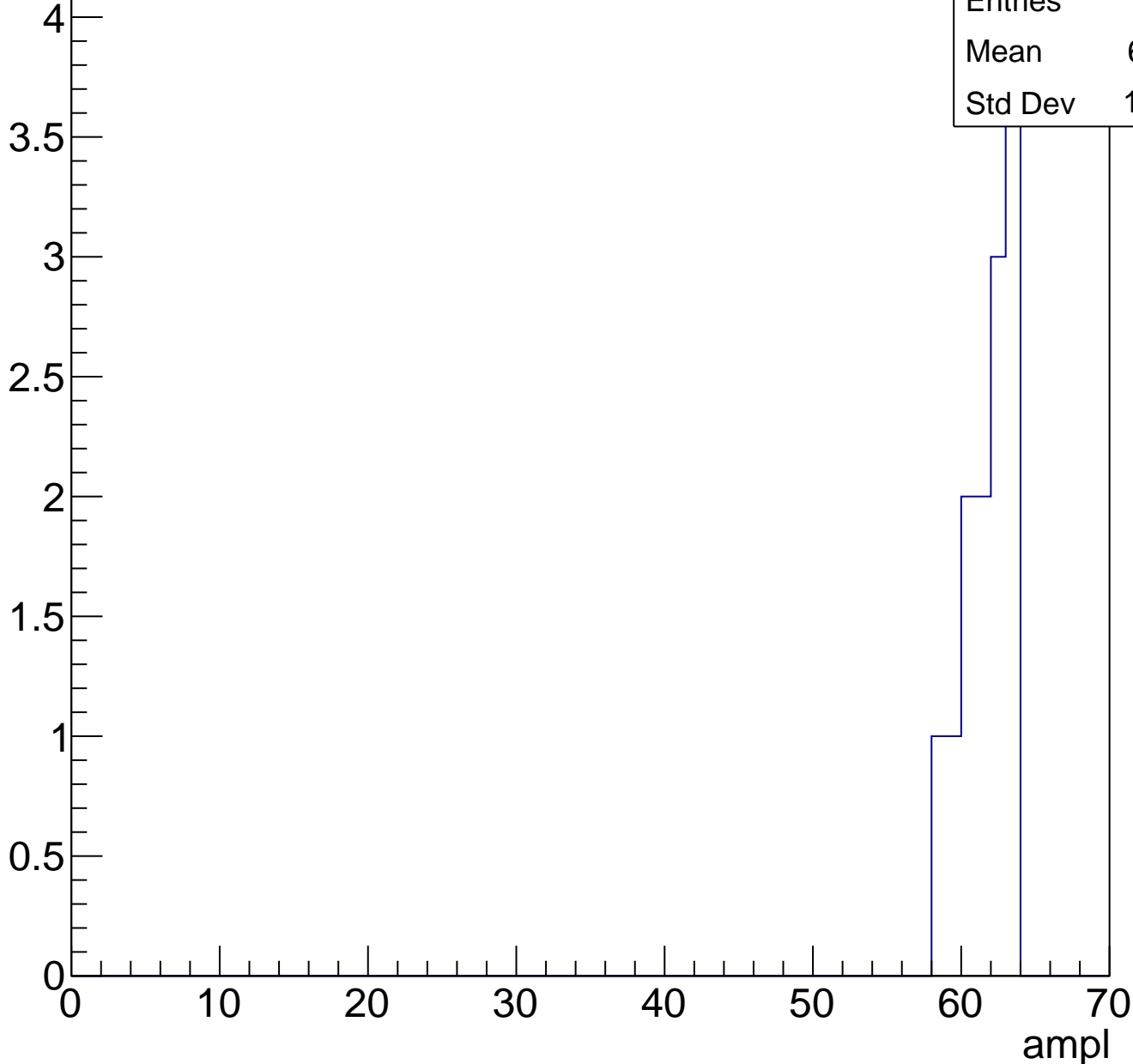
calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U7-ch68, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

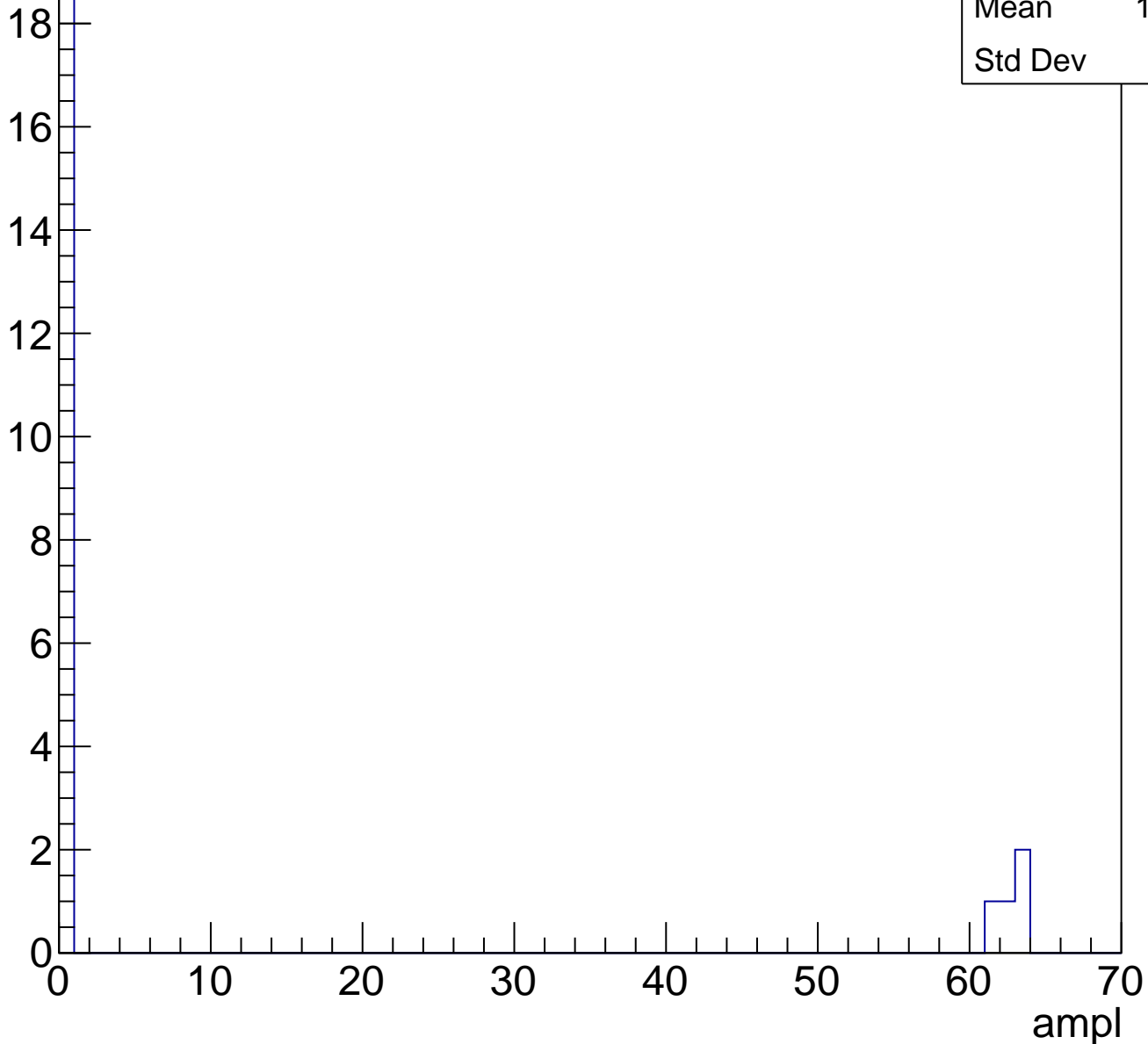


B1L103S, U7-ch68, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	23
Mean	10.83
Std Dev	23.6

Entry



B1L103S, U7-ch69, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	84
Mean	25.12
Std Dev	10.29

Gaus mean : 28.9178

Gaus Width: 3.9394

Entry

10

8

6

4

2

0

0

10

20

30

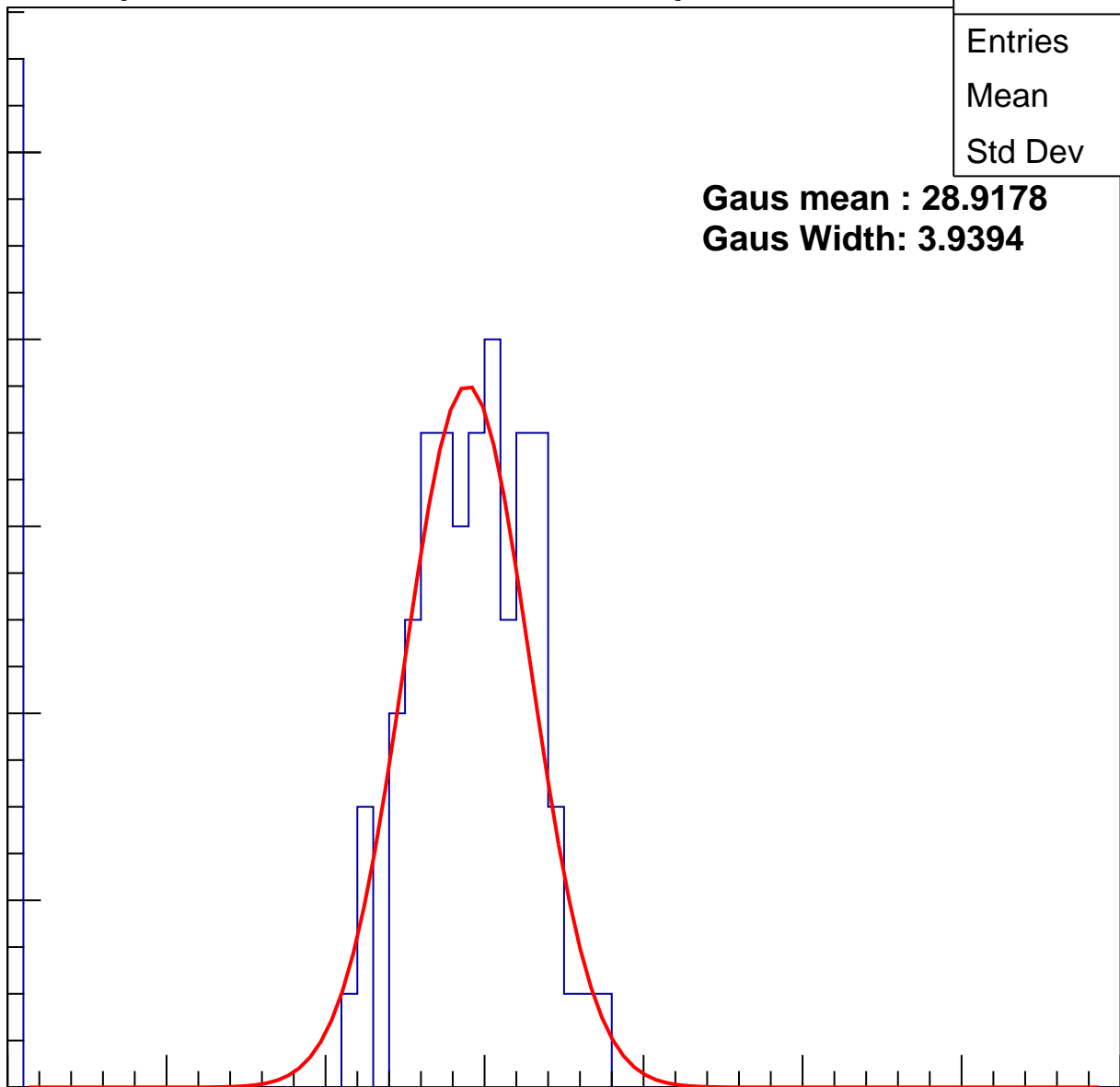
40

50

60

70

ampl



B1L103S, U7-ch69, adc1

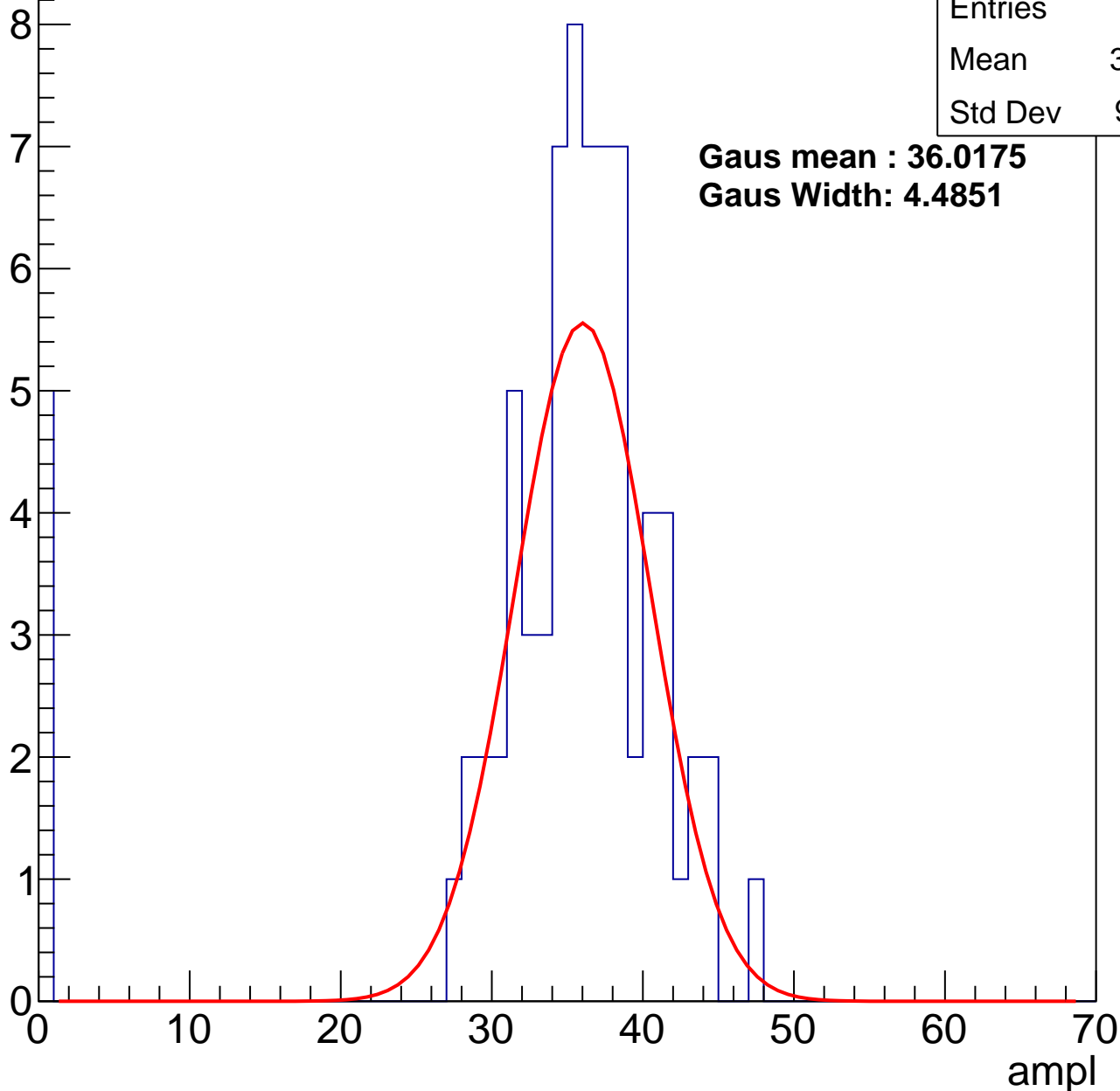
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	33.48
Std Dev	9.811

Gaus mean : 36.0175

Gaus Width: 4.4851



B1L103S, U7-ch69, adc2

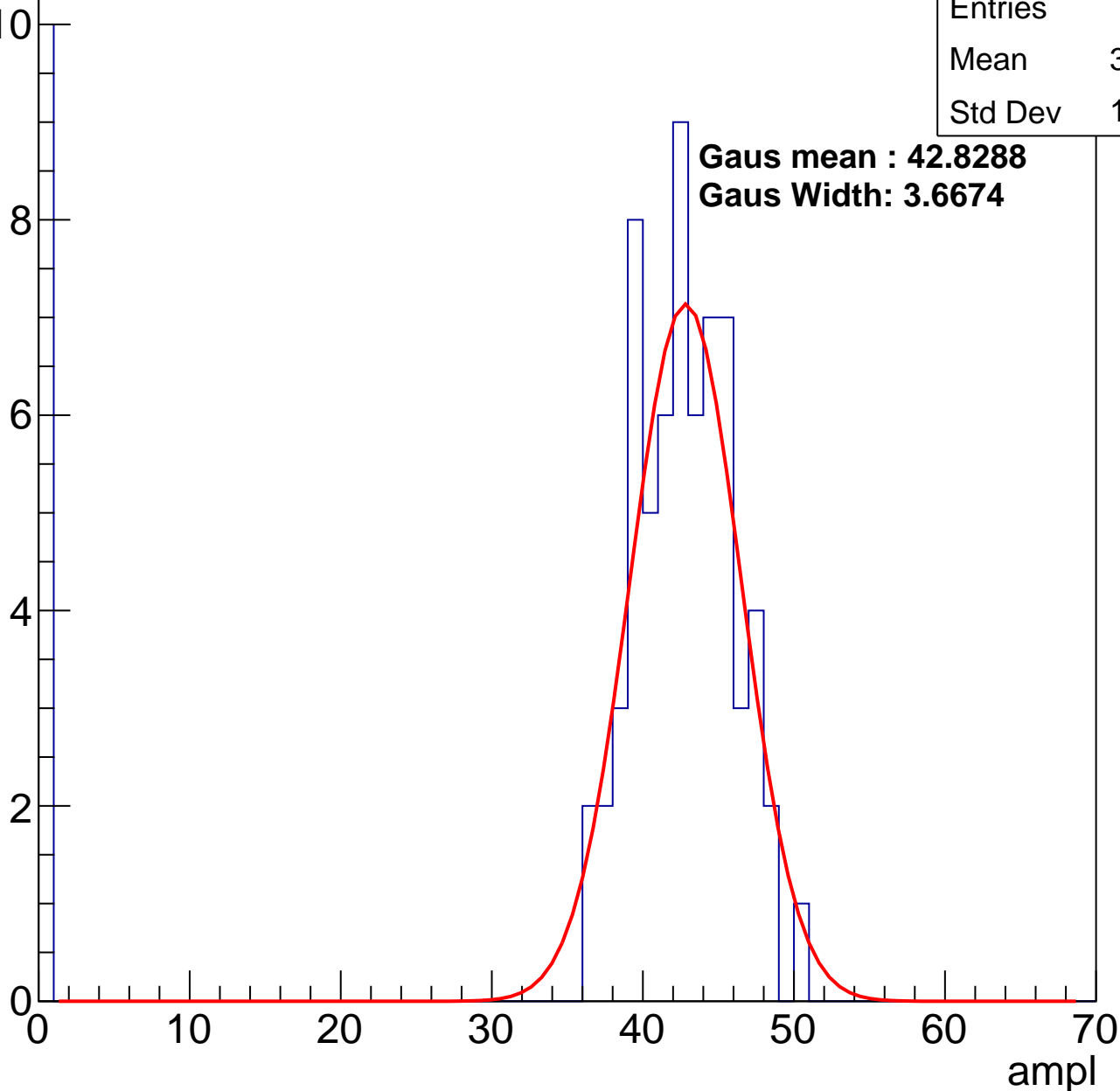
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	36.65
Std Dev	14.67

Gaus mean : 42.8288

Gaus Width: 3.6674

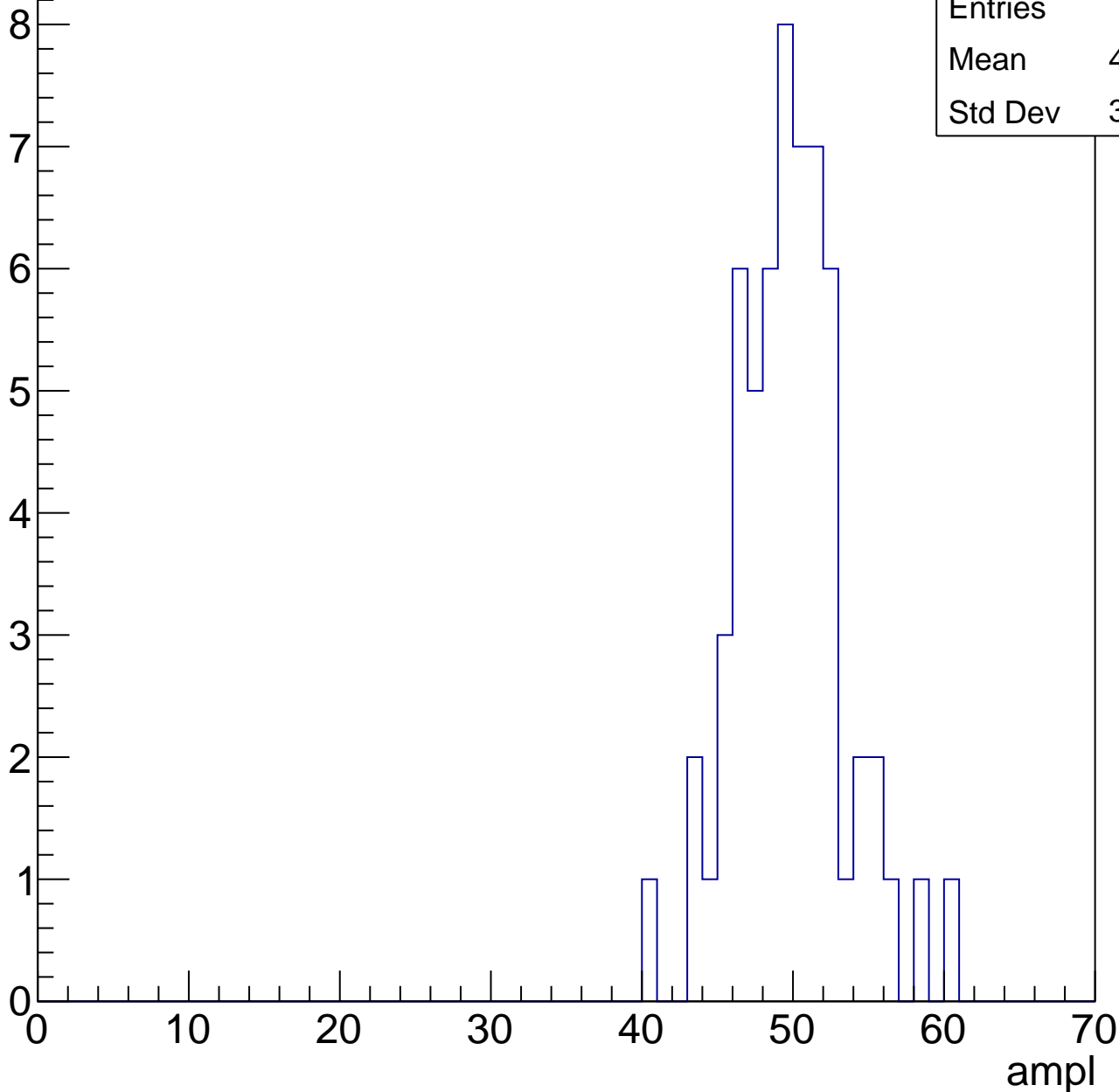


B1L103S, U7-ch69, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	49.33
Std Dev	3.599

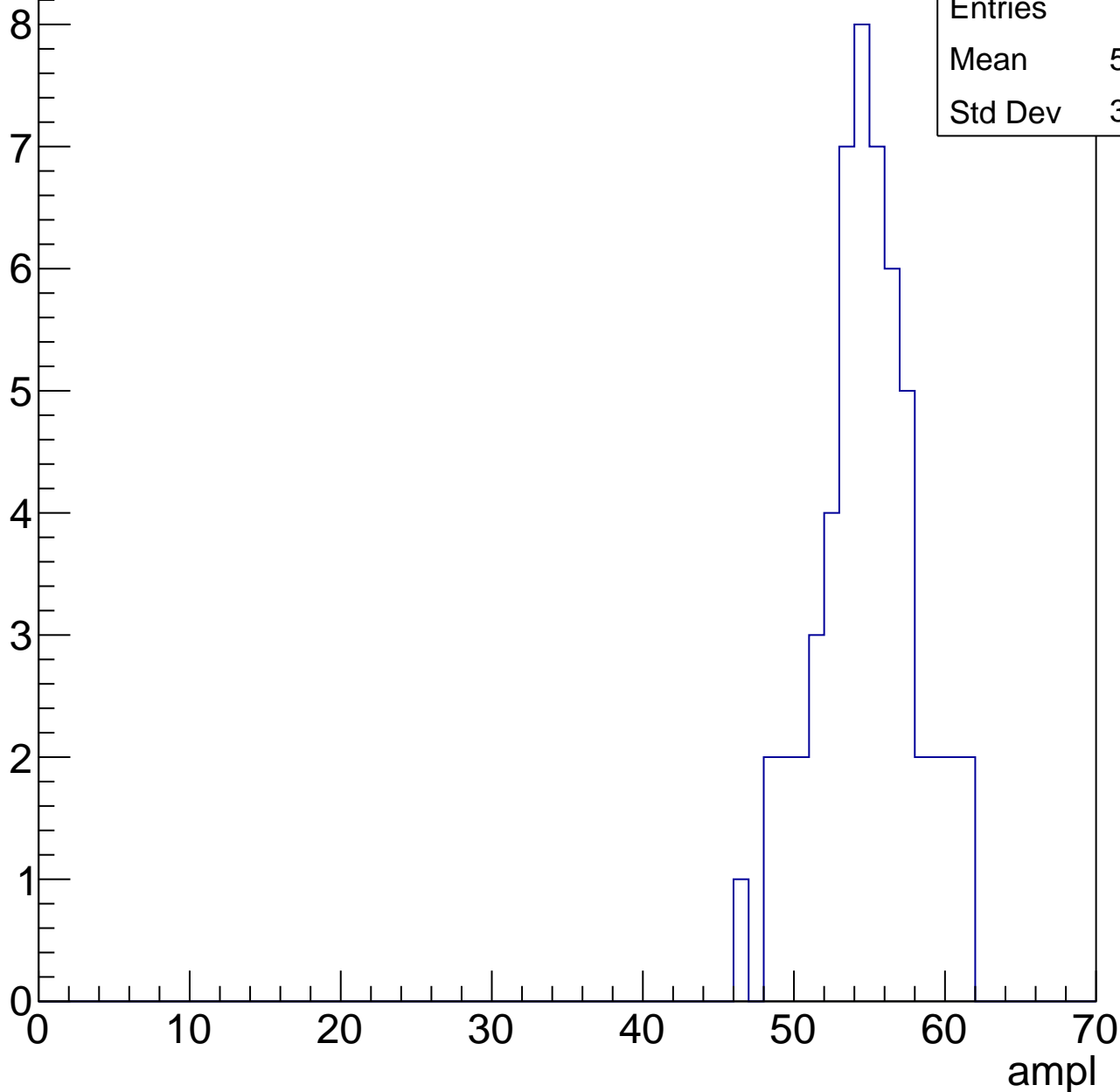


B1L103S, U7-ch69, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	54.29
Std Dev	3.279

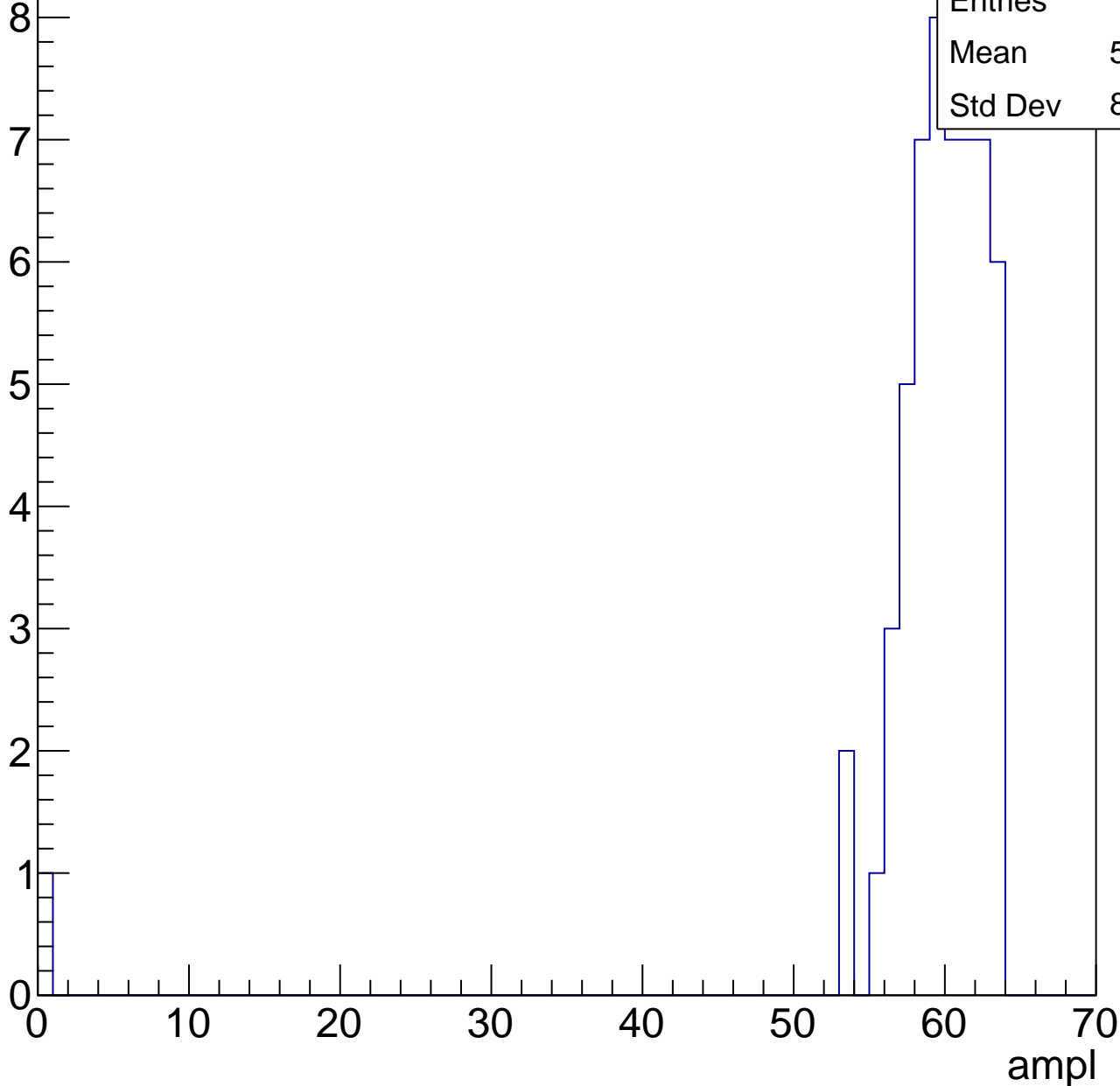


B1L103S, U7-ch69, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

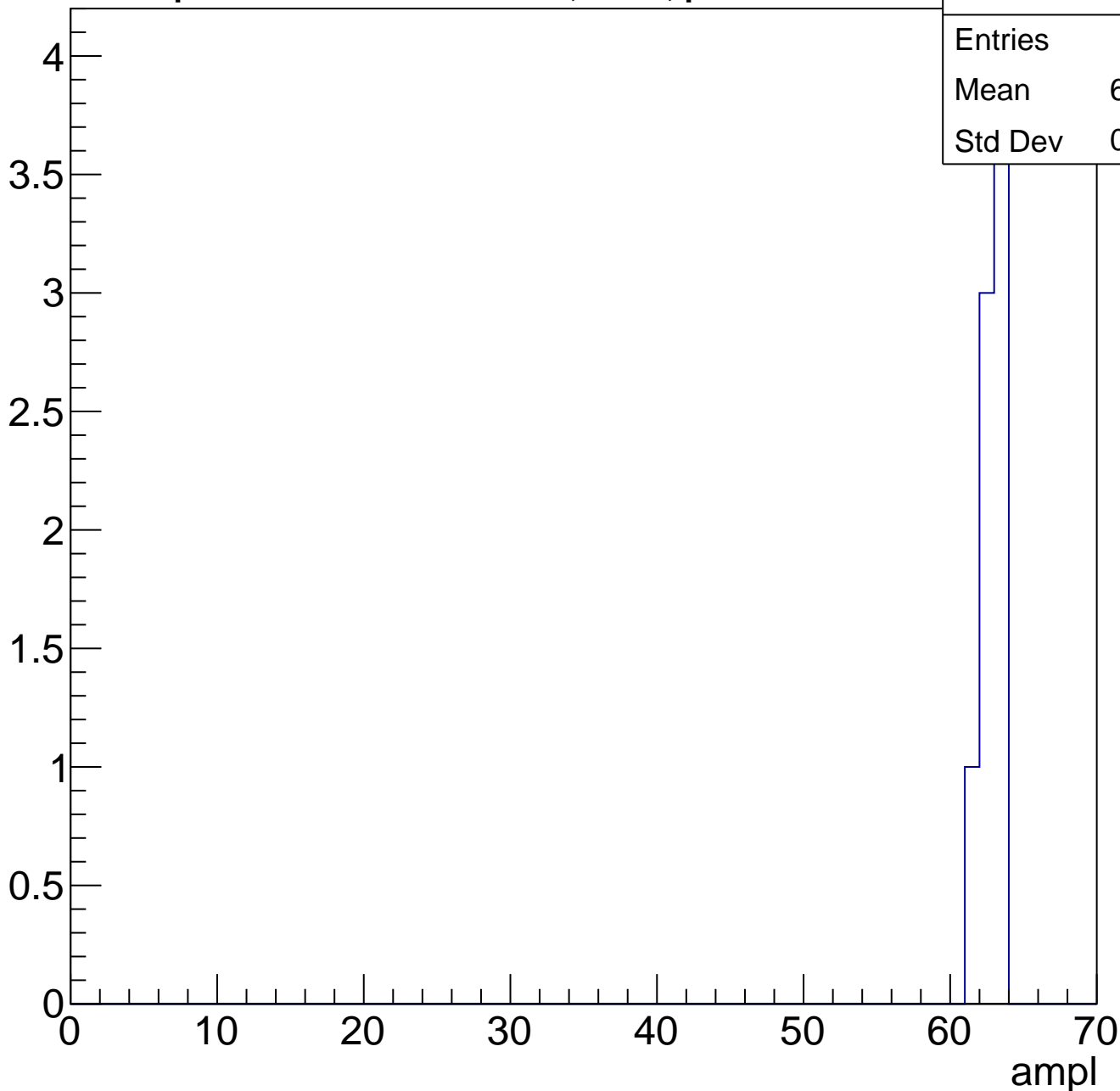
Entries	54
Mean	58.35
Std Dev	8.382



B1L103S, U7-ch69, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

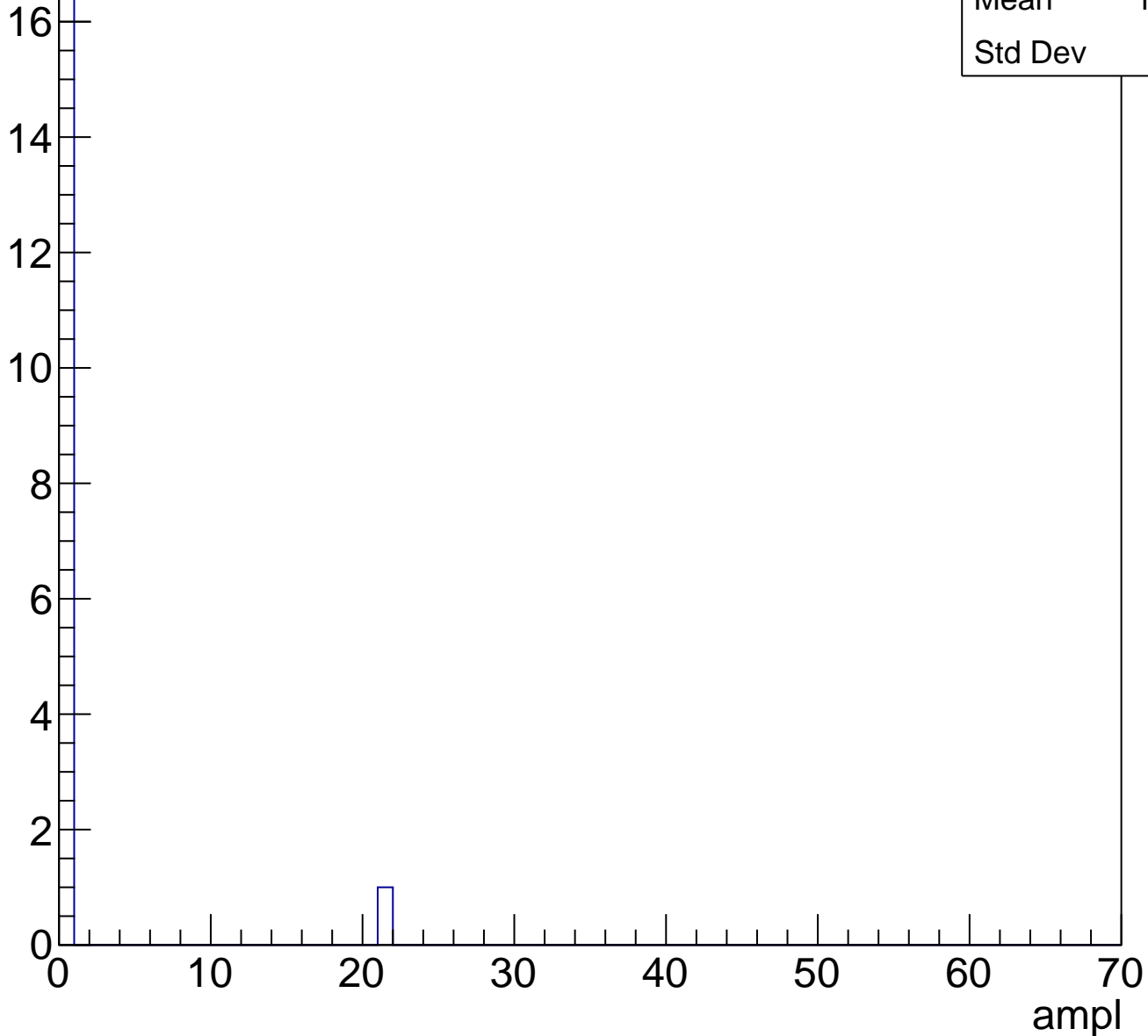


B1L103S, U7-ch69, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	18
Mean	1.167
Std Dev	4.81

Entry



B1L103S, U7-ch70, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	90
Mean	23.21
Std Dev	10.82

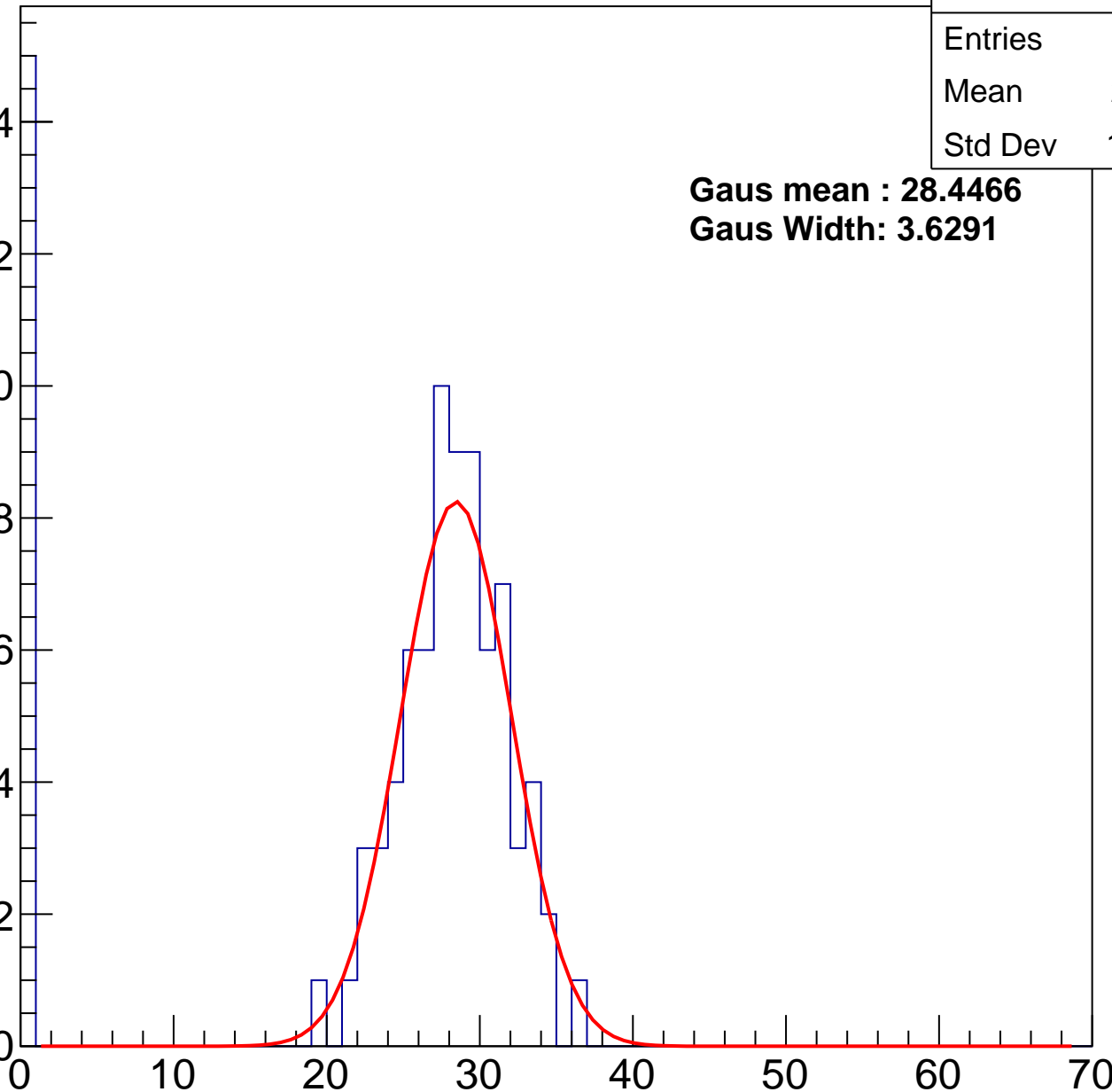
Gaus mean : 28.4466

Gaus Width: 3.6291

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch70, adc1

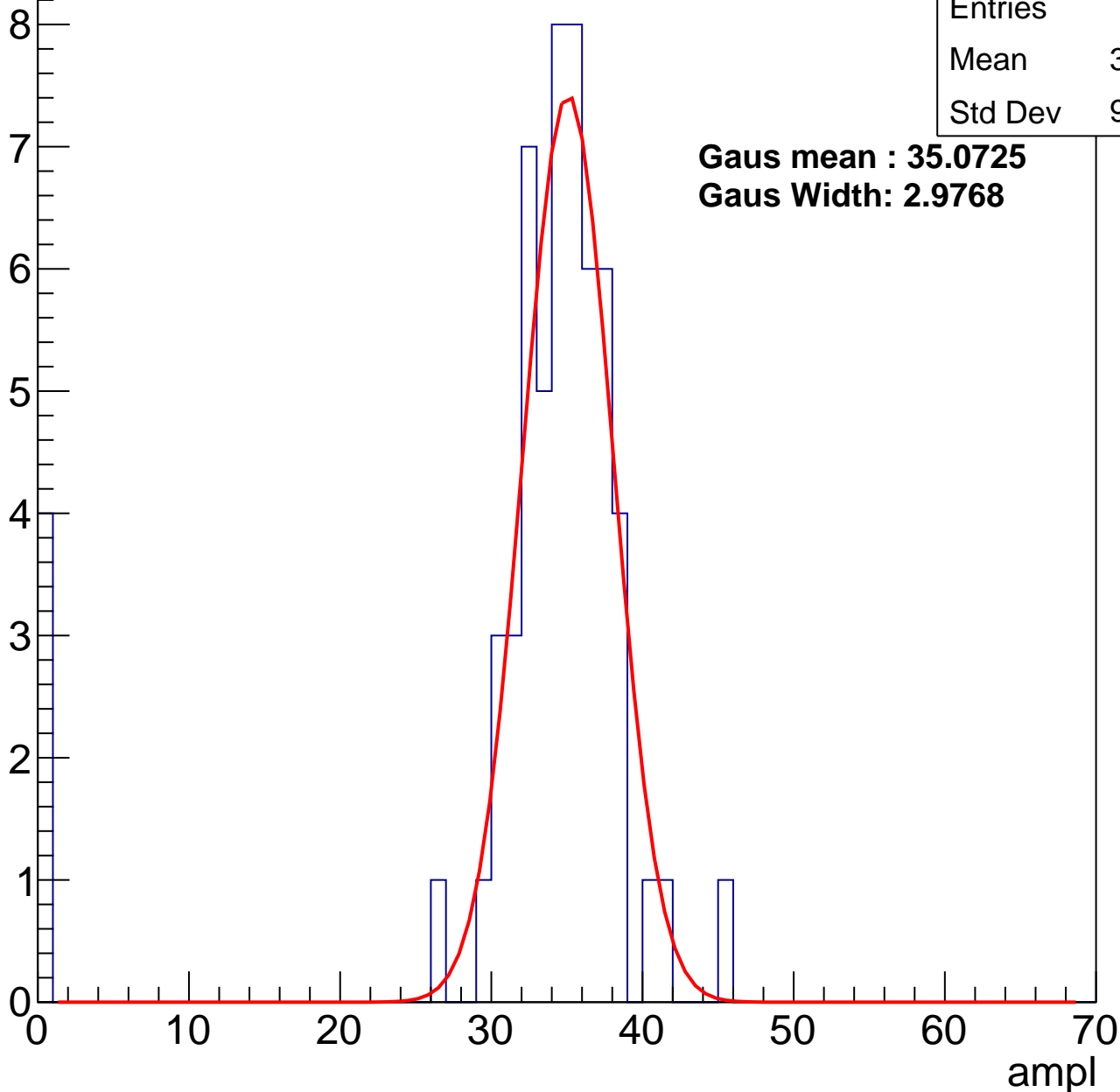
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	32.12
Std Dev	9.176

Gaus mean : 35.0725

Gaus Width: 2.9768



B1L103S, U7-ch70, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	72
Mean	40.07
Std Dev	5.598

Gaus mean : 40.8905

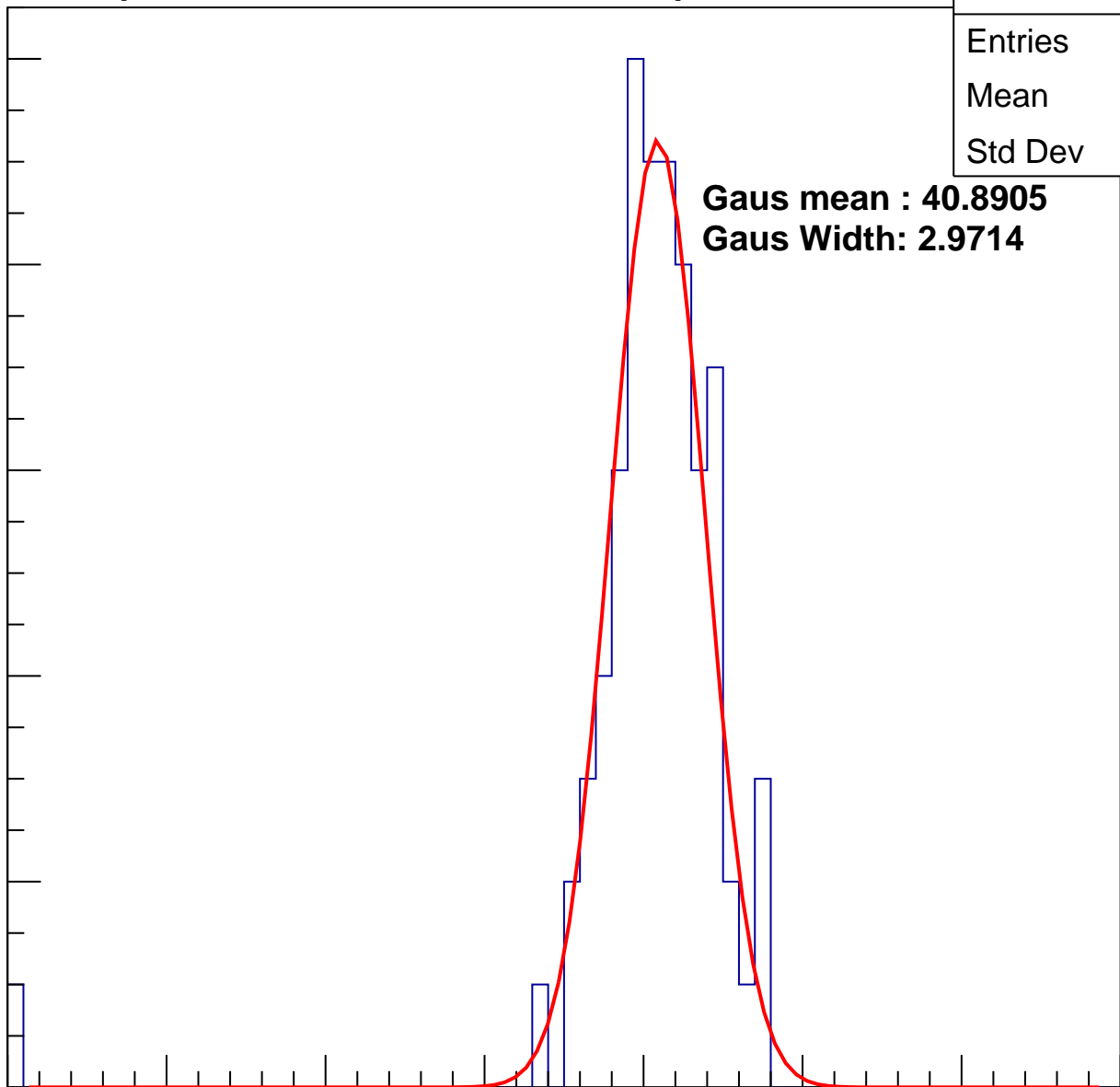
Gaus Width: 2.9714

Entry

10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

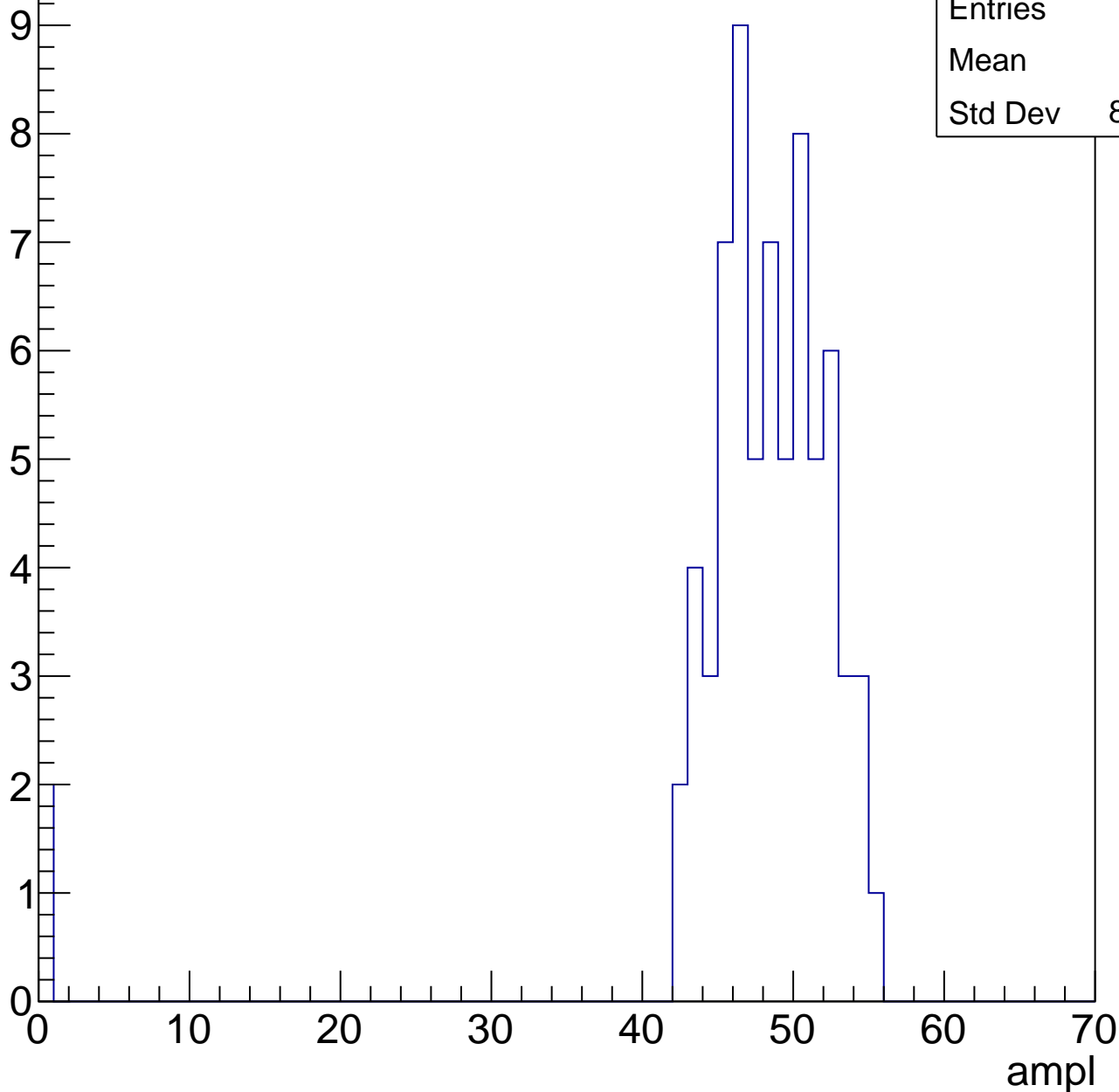


B1L103S, U7-ch70, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	46.8
Std Dev	8.653

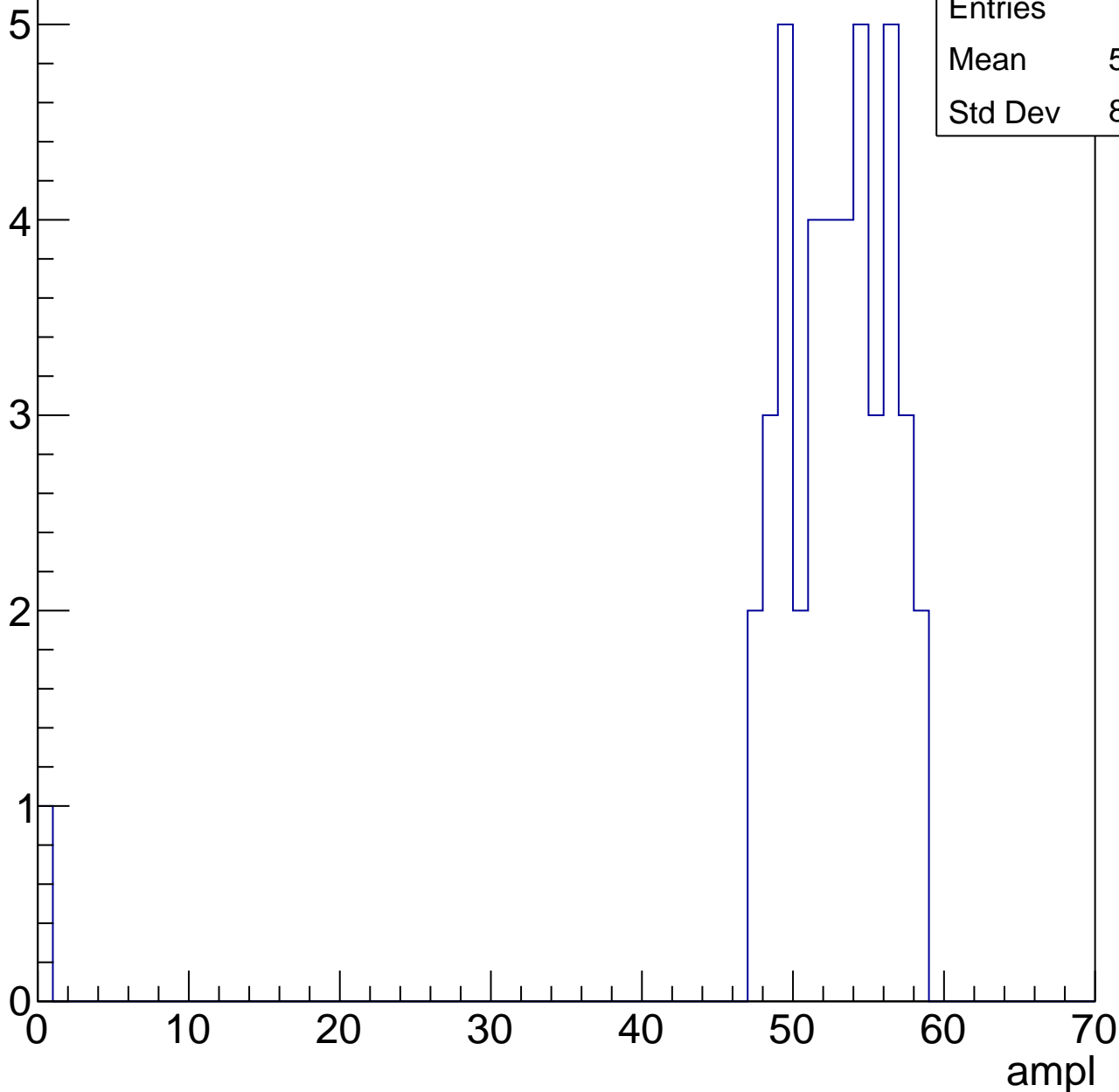


B1L103S, U7-ch70, adc4

calib_packv5_041523_1651.root, FC#0, port C2

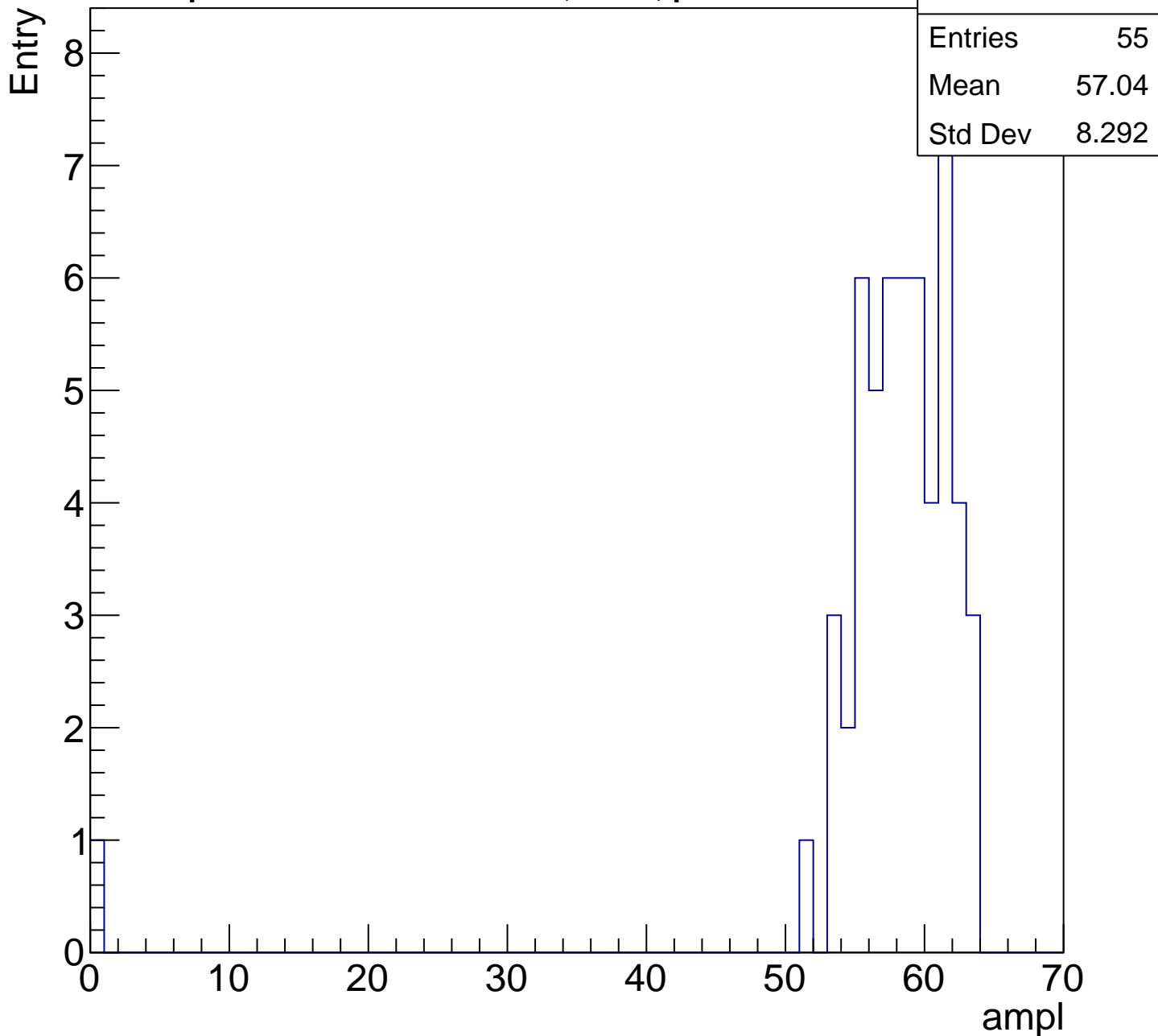
Entry

Entries	43
Mean	51.37
Std Dev	8.518



B1L103S, U7-ch70, adc5

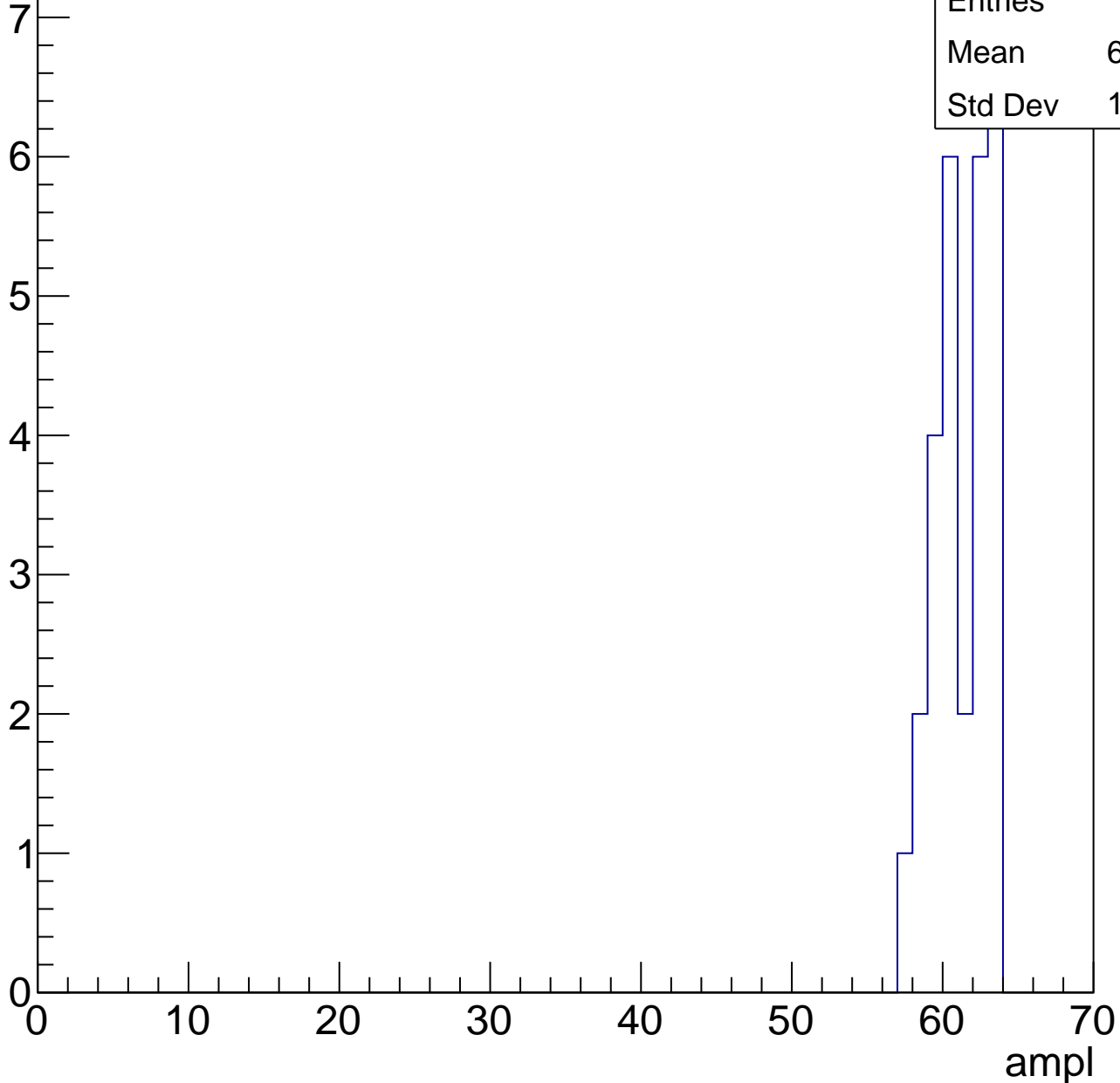
calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U7-ch70, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch70, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U7-ch71, adc0

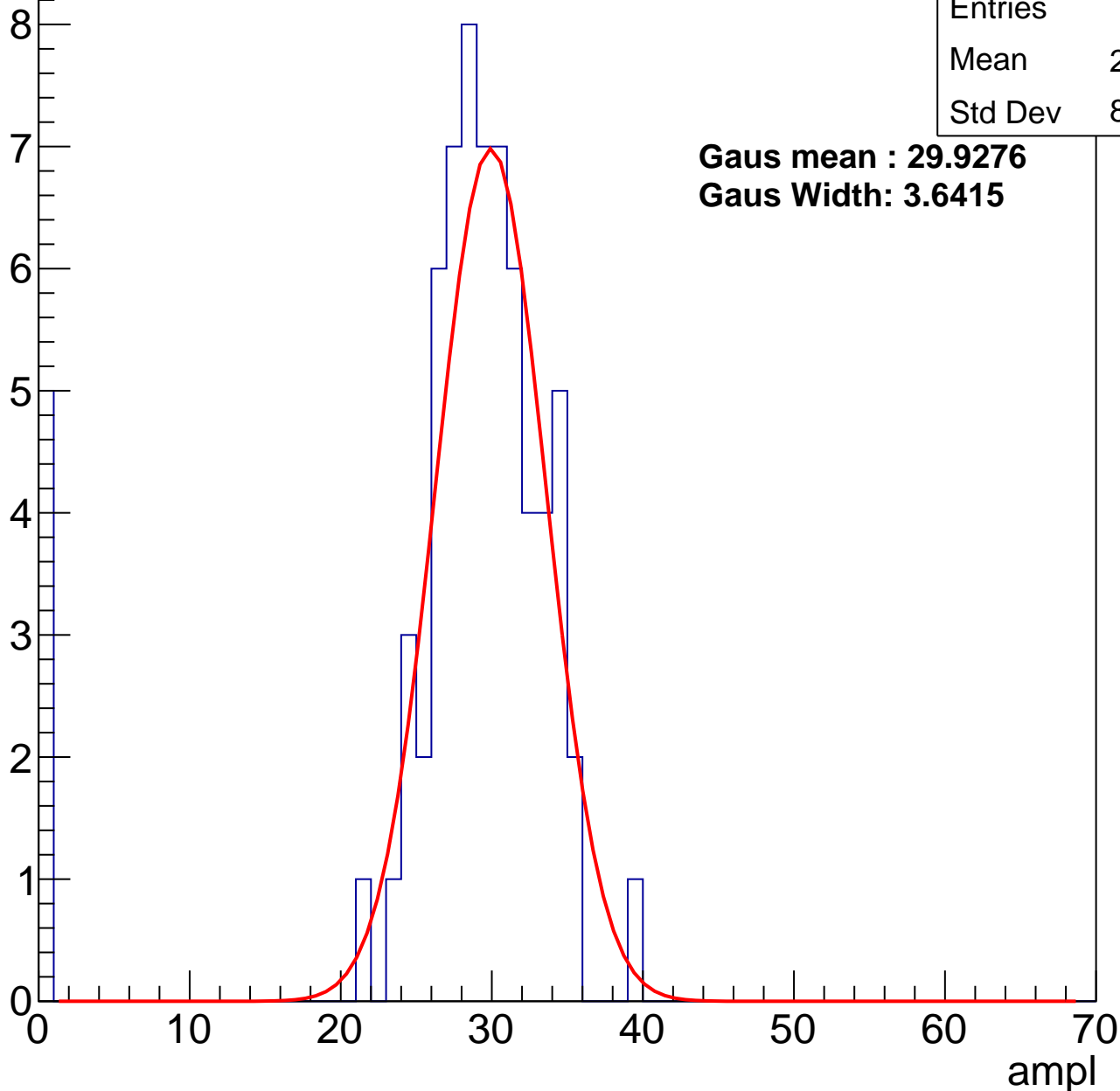
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	27.14
Std Dev	8.247

Gaus mean : 29.9276

Gaus Width: 3.6415



B1L103S, U7-ch71, adc1

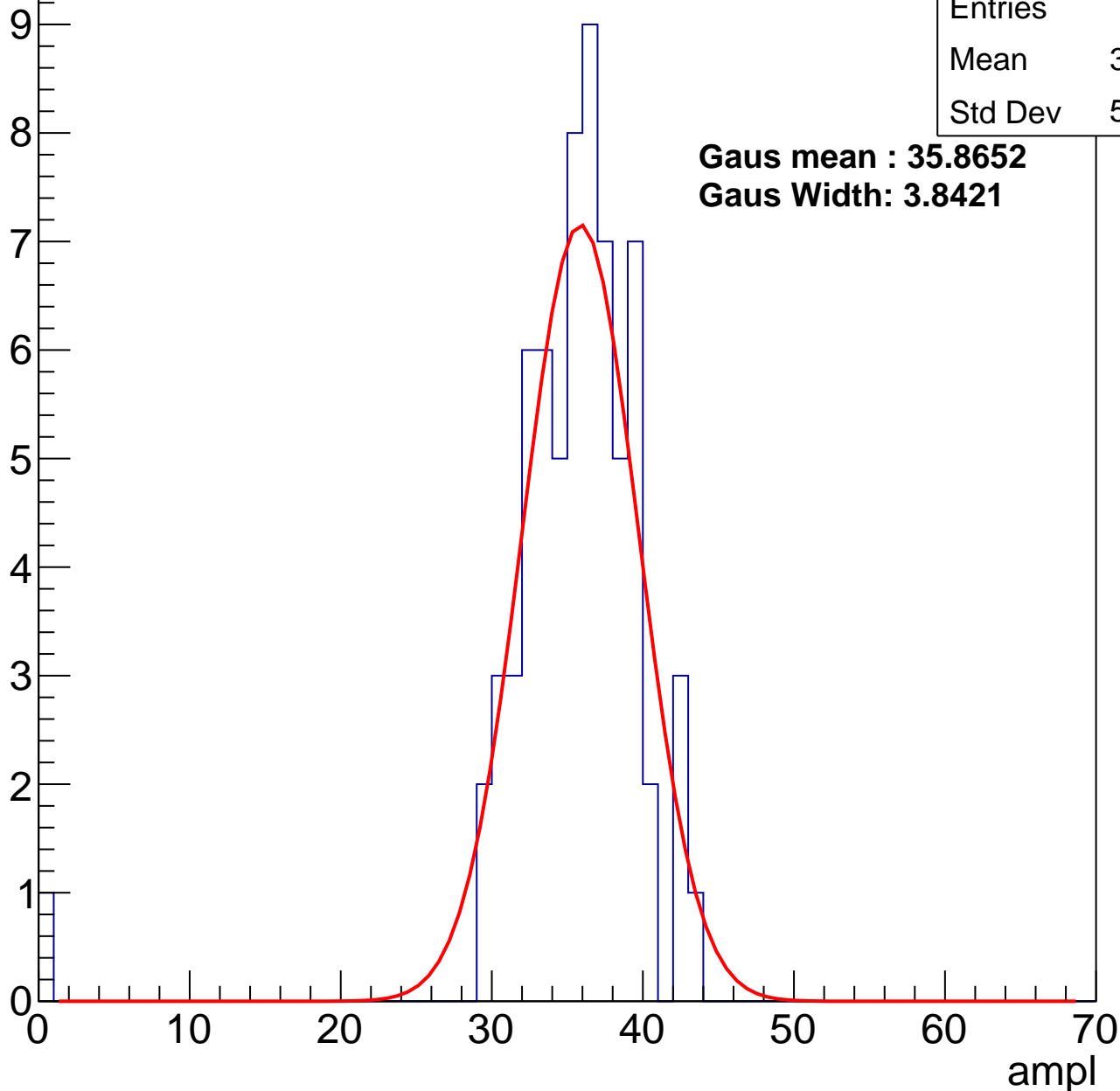
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	34.94
Std Dev	5.366

Gaus mean : 35.8652

Gaus Width: 3.8421



B1L103S, U7-ch71, adc2

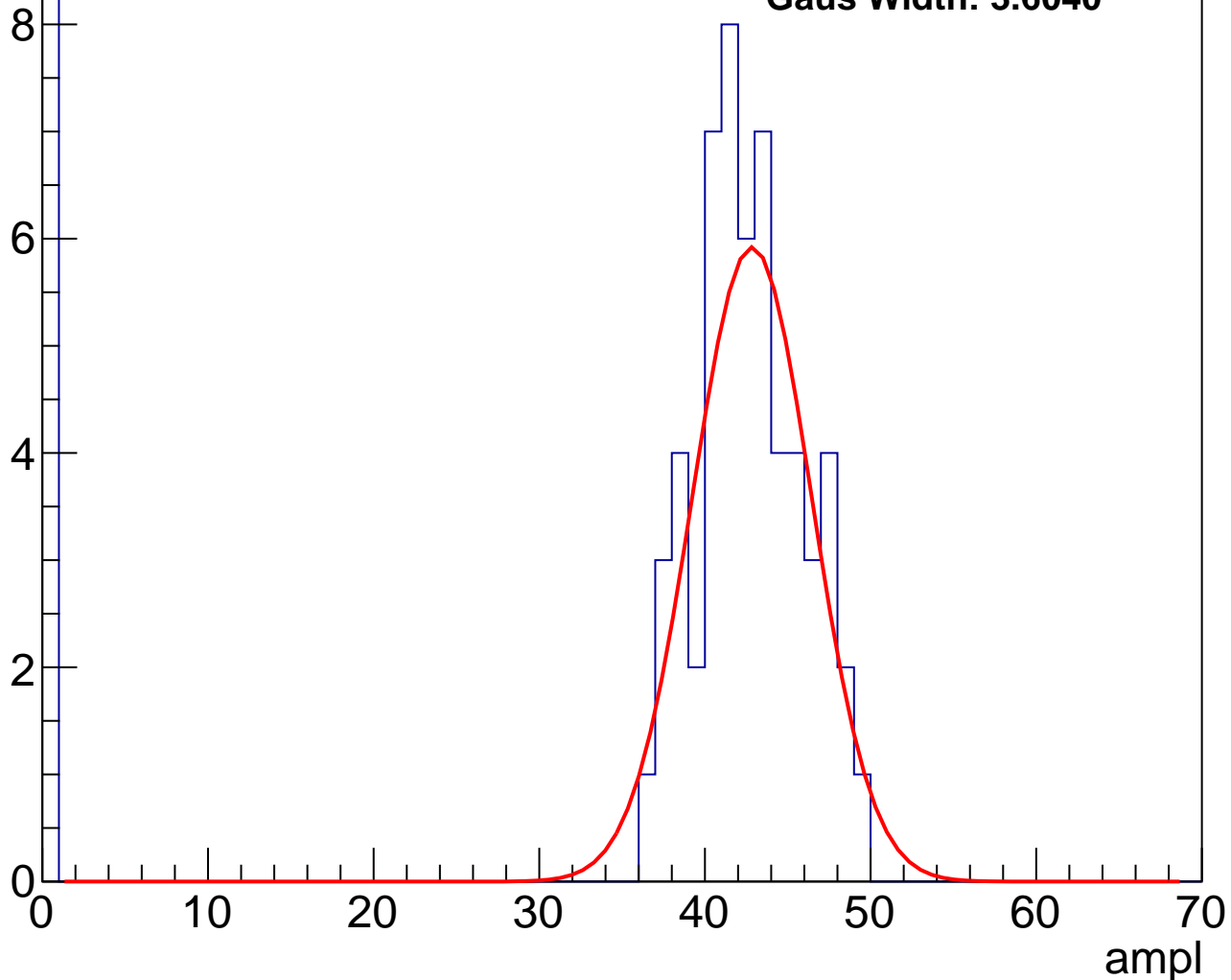
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	35.83
Std Dev	15.42

Gaus mean : 42.8402

Gaus Width: 3.6040

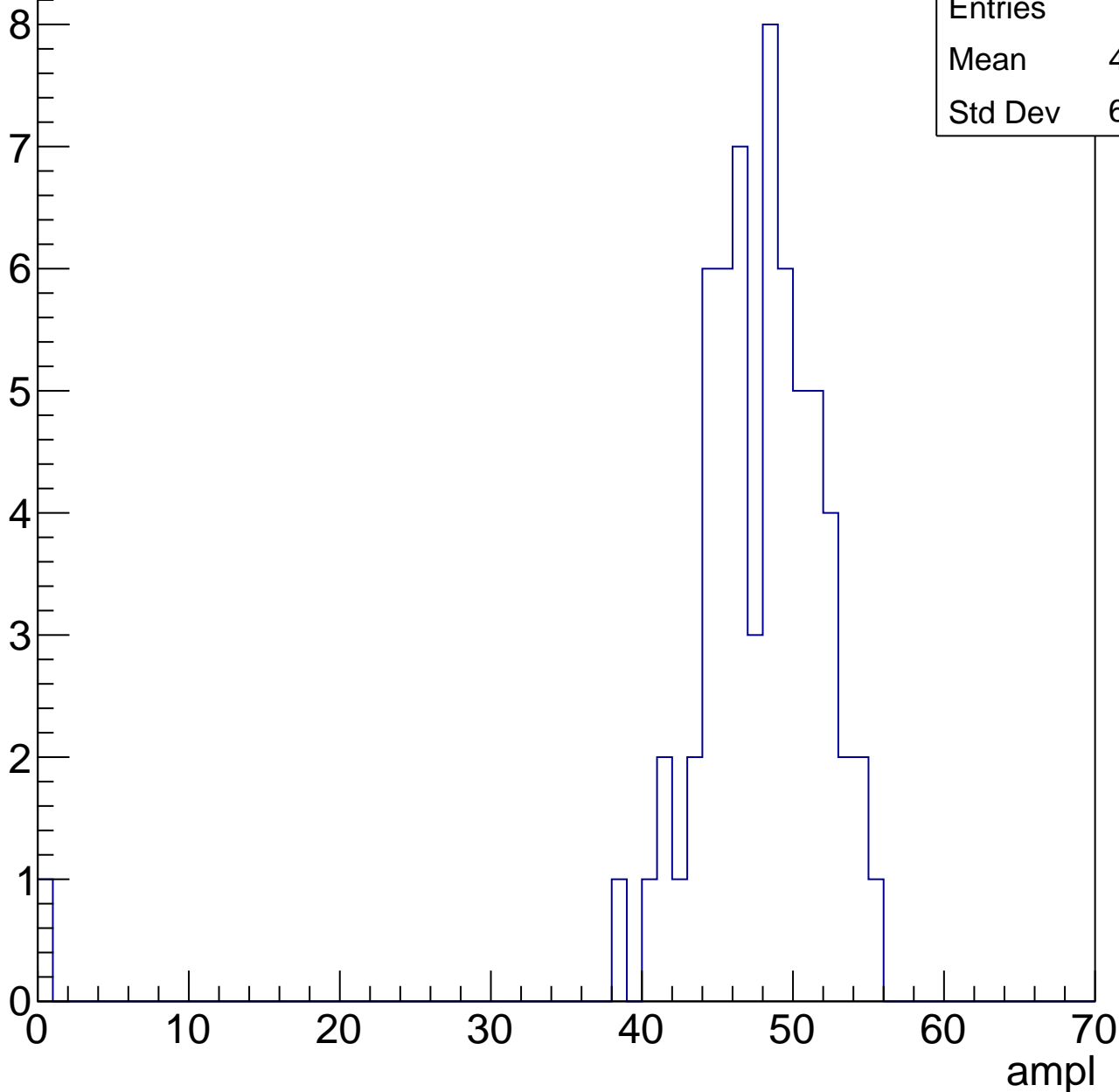


B1L103S, U7-ch71, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	46.75
Std Dev	6.946

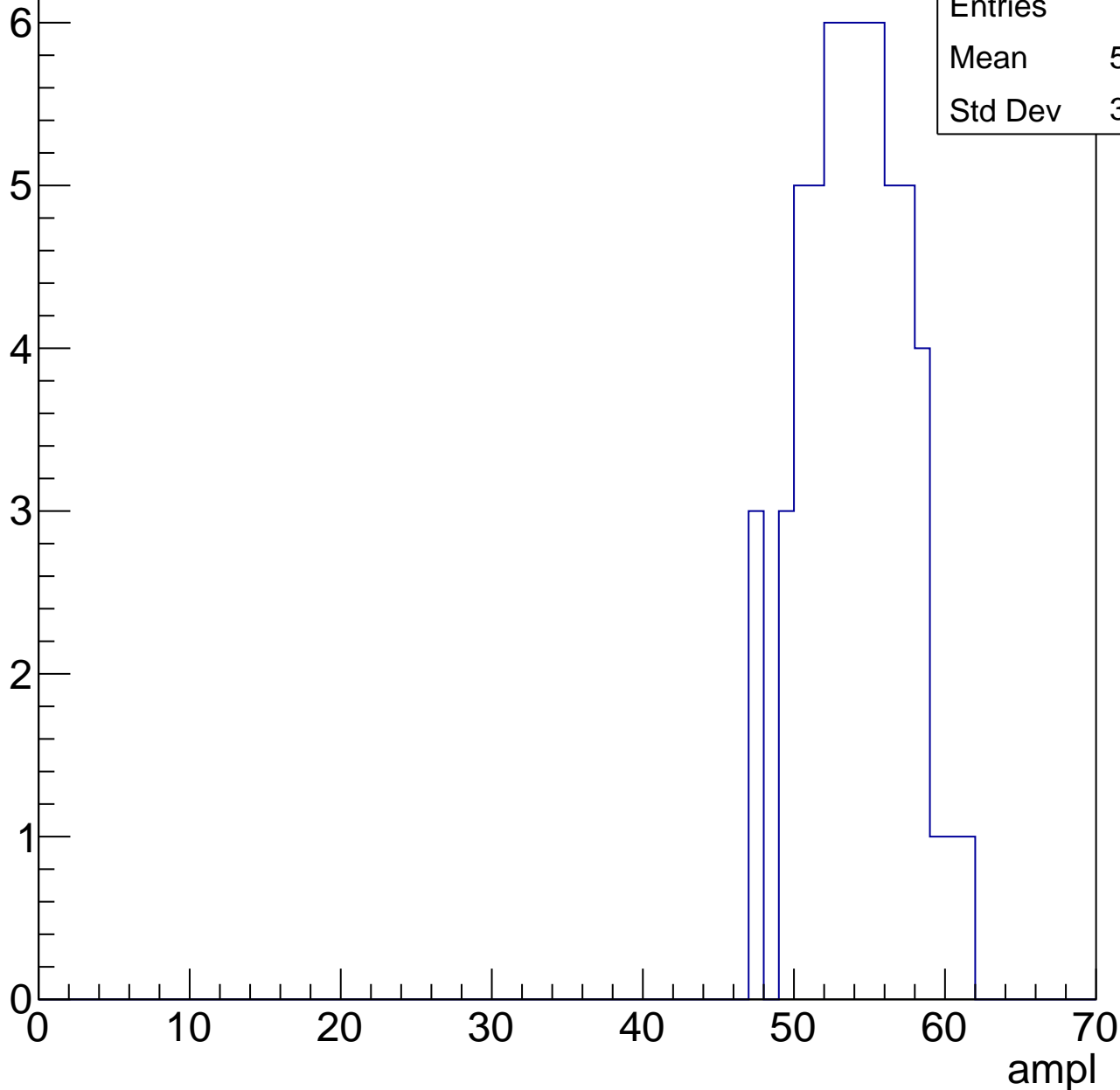


B1L103S, U7-ch71, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	53.58
Std Dev	3.276



B1L103S, U7-ch71, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

8
7
6
5
4
3
2
1
0

Entries	57
Mean	58.98
Std Dev	2.711

ampl

0

10

20

30

40

50

60

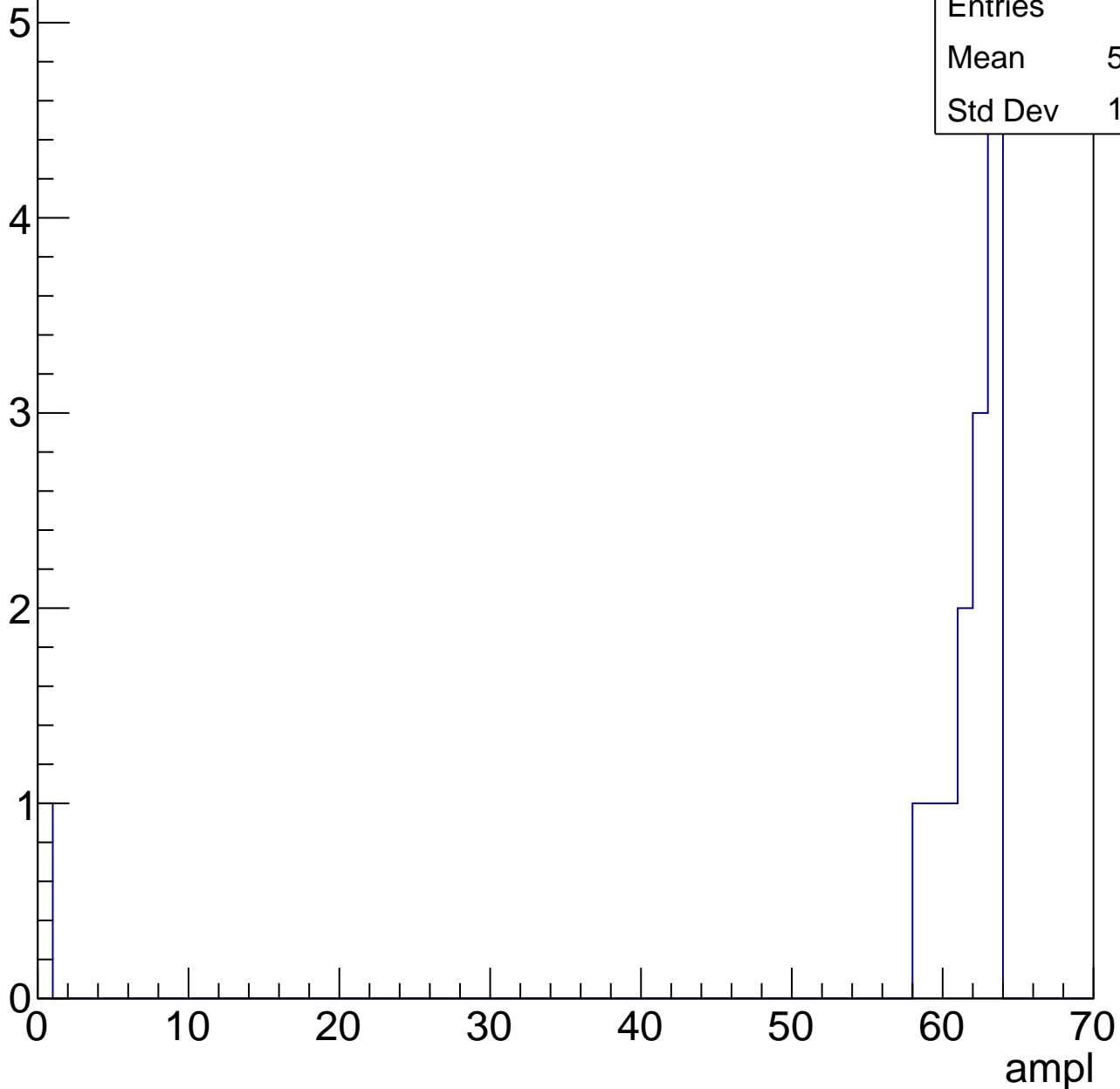
70

B1L103S, U7-ch71, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	14
Mean	57.14
Std Dev	15.92



B1L103S, U7-ch71, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U7-ch72, adc0

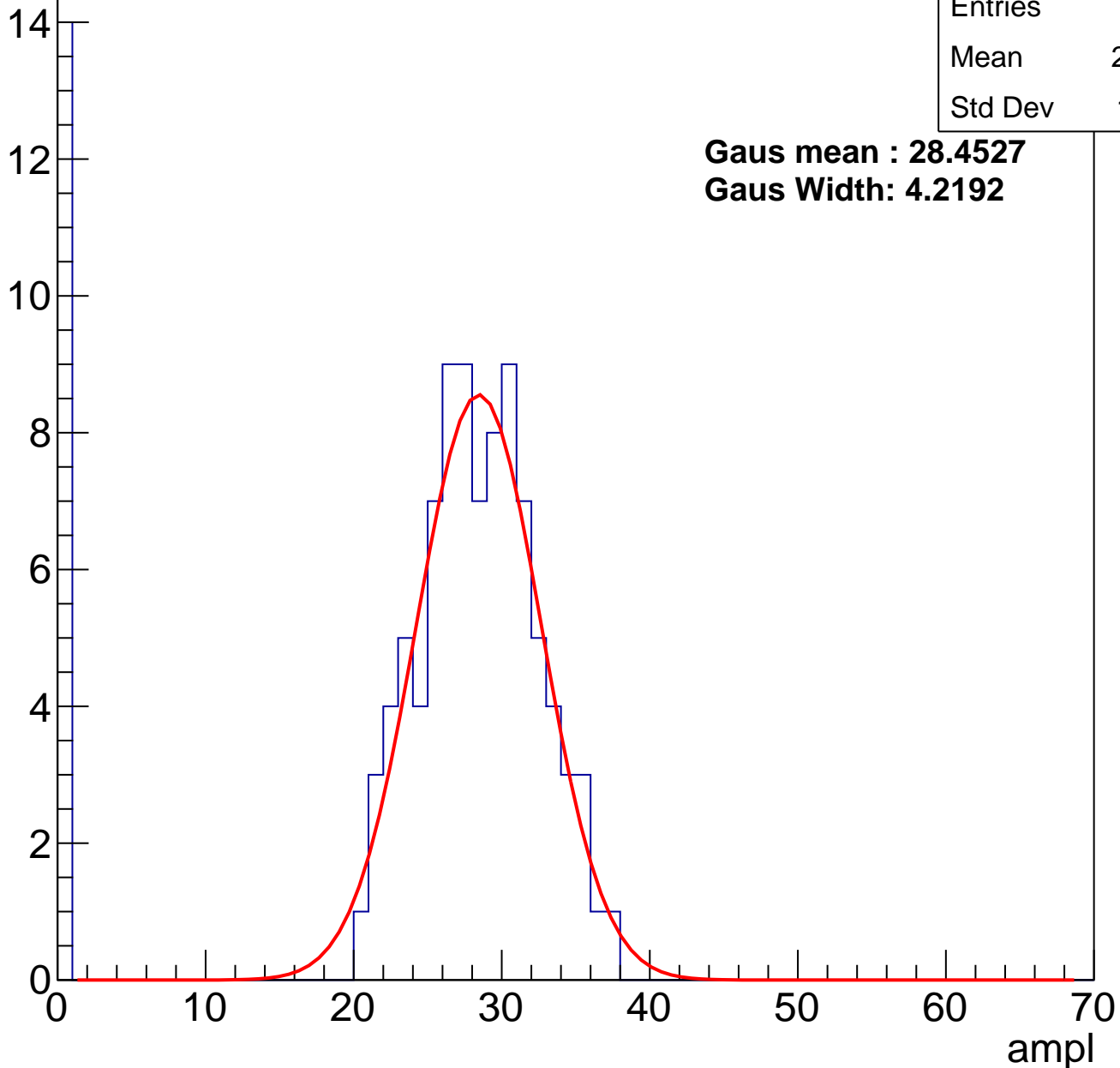
calib_packv5_041523_1651.root, FC#0, port C2

Entries	104
Mean	24.24
Std Dev	10.21

Gaus mean : 28.4527

Gaus Width: 4.2192

Entry



B1L103S, U7-ch72, adc1

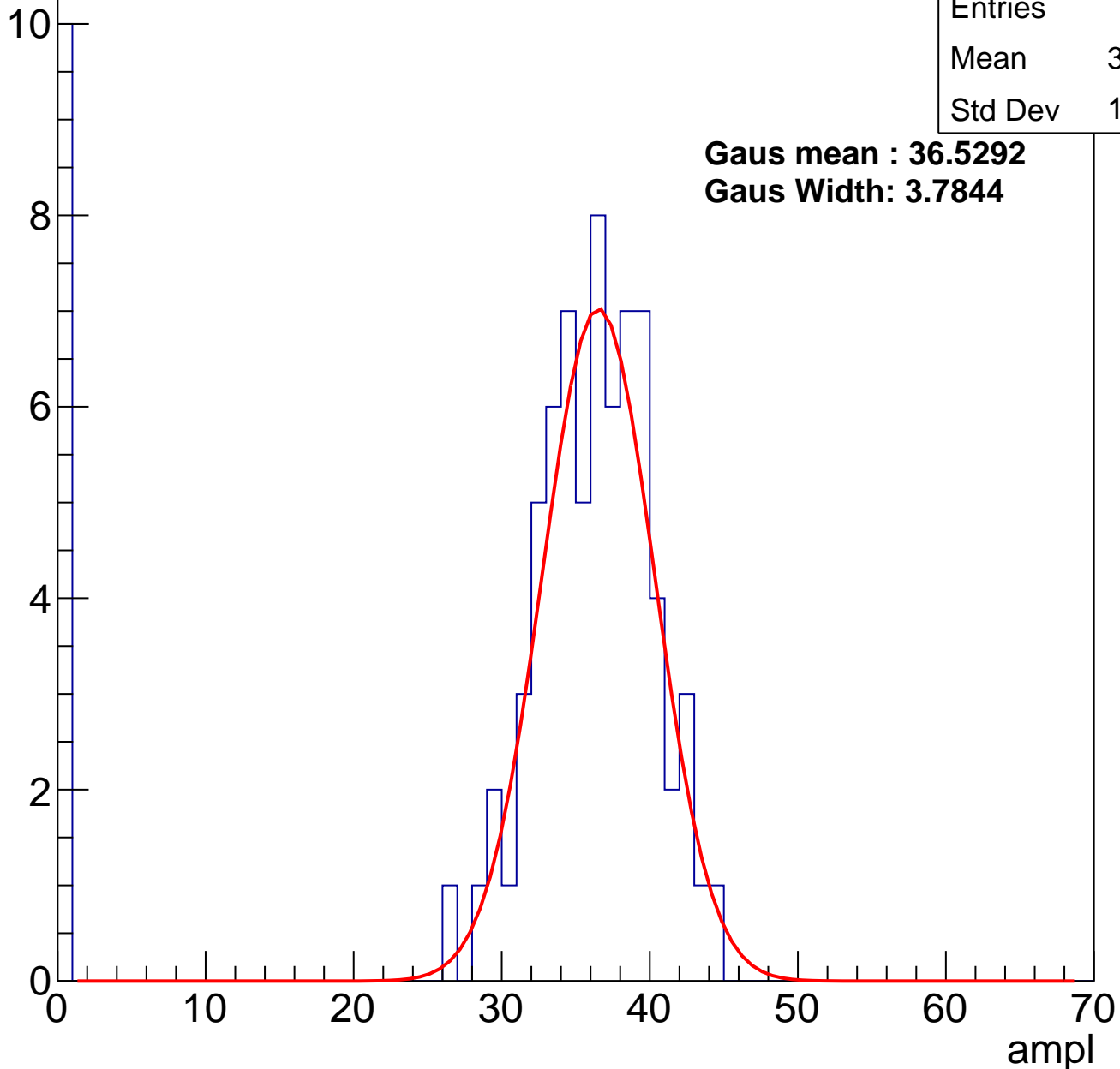
calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	31.38
Std Dev	12.36

Gaus mean : 36.5292

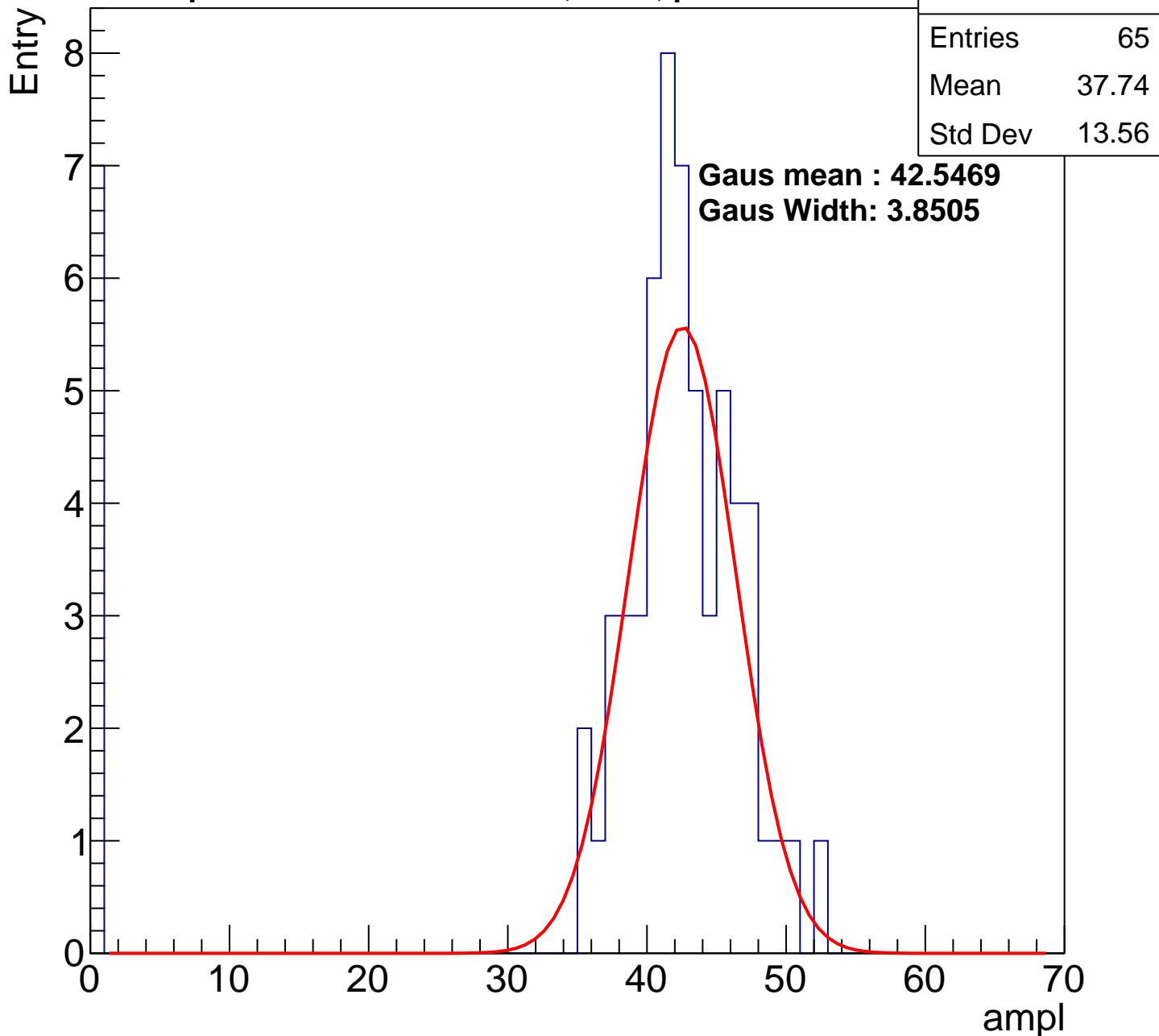
Gaus Width: 3.7844

Entry



B1L103S, U7-ch72, adc2

calib_packv5_041523_1651.root, FC#0, port C2

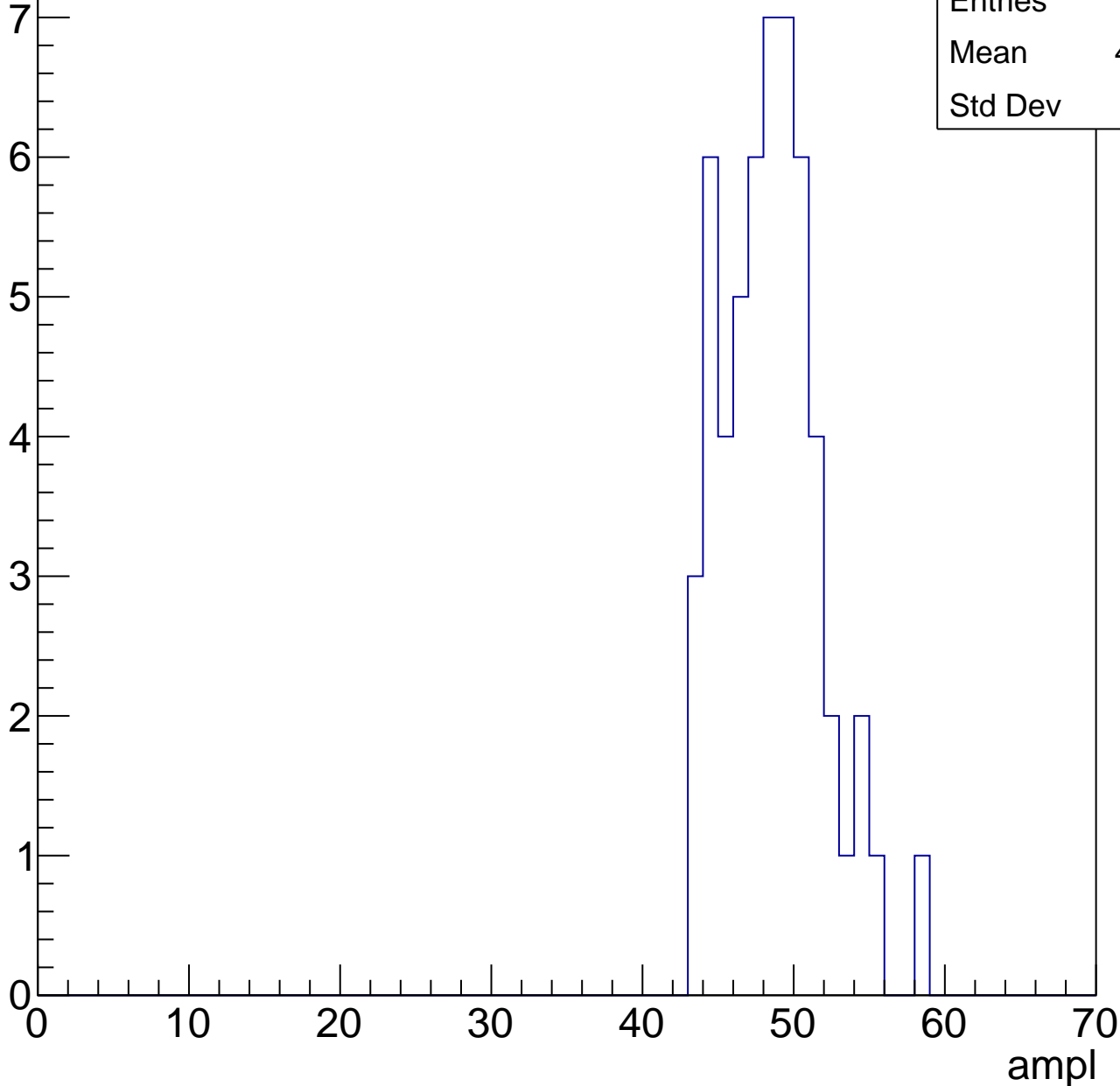


B1L103S, U7-ch72, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	48.11
Std Dev	3.24

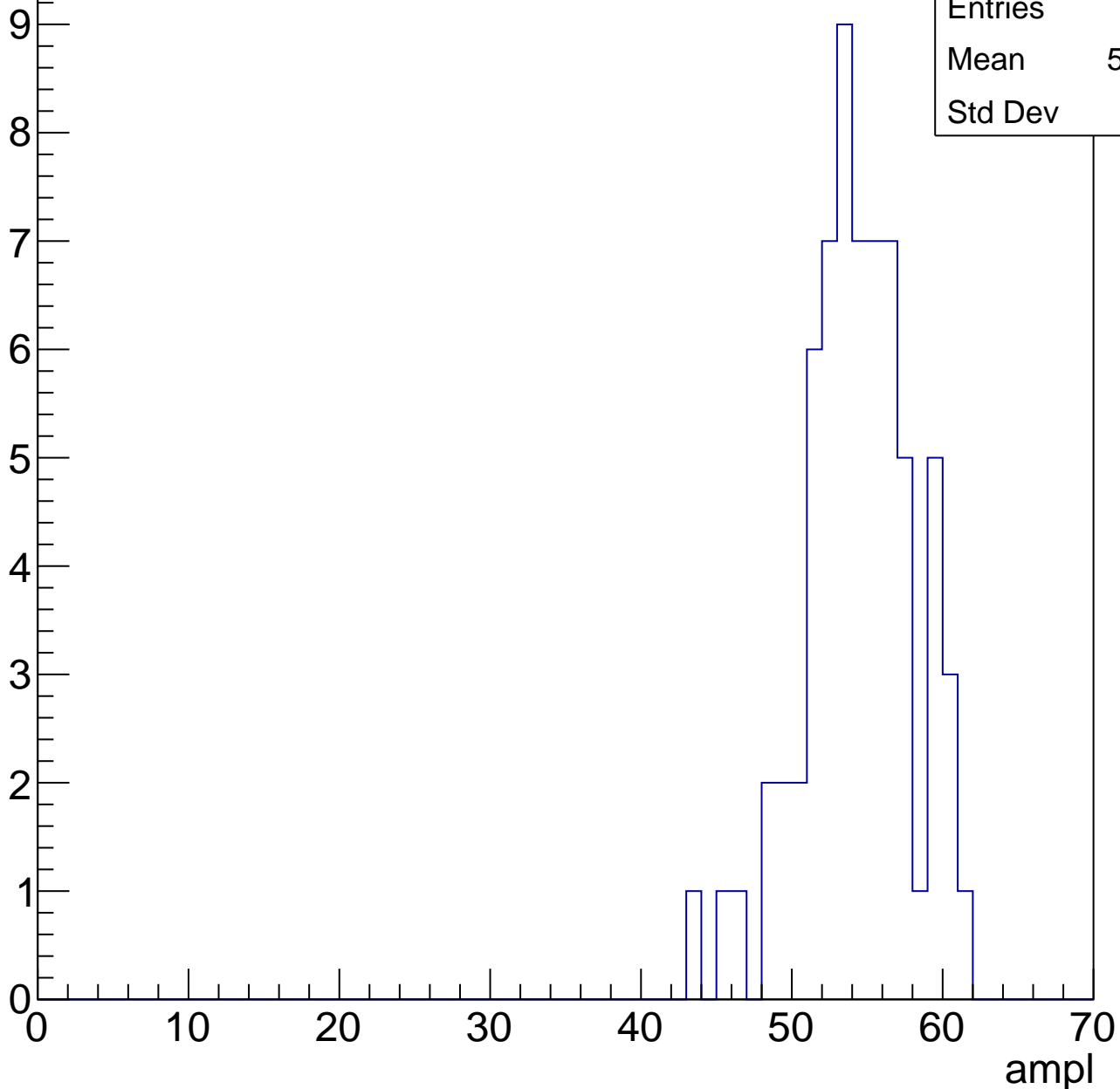


B1L103S, U7-ch72, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	53.87
Std Dev	3.64

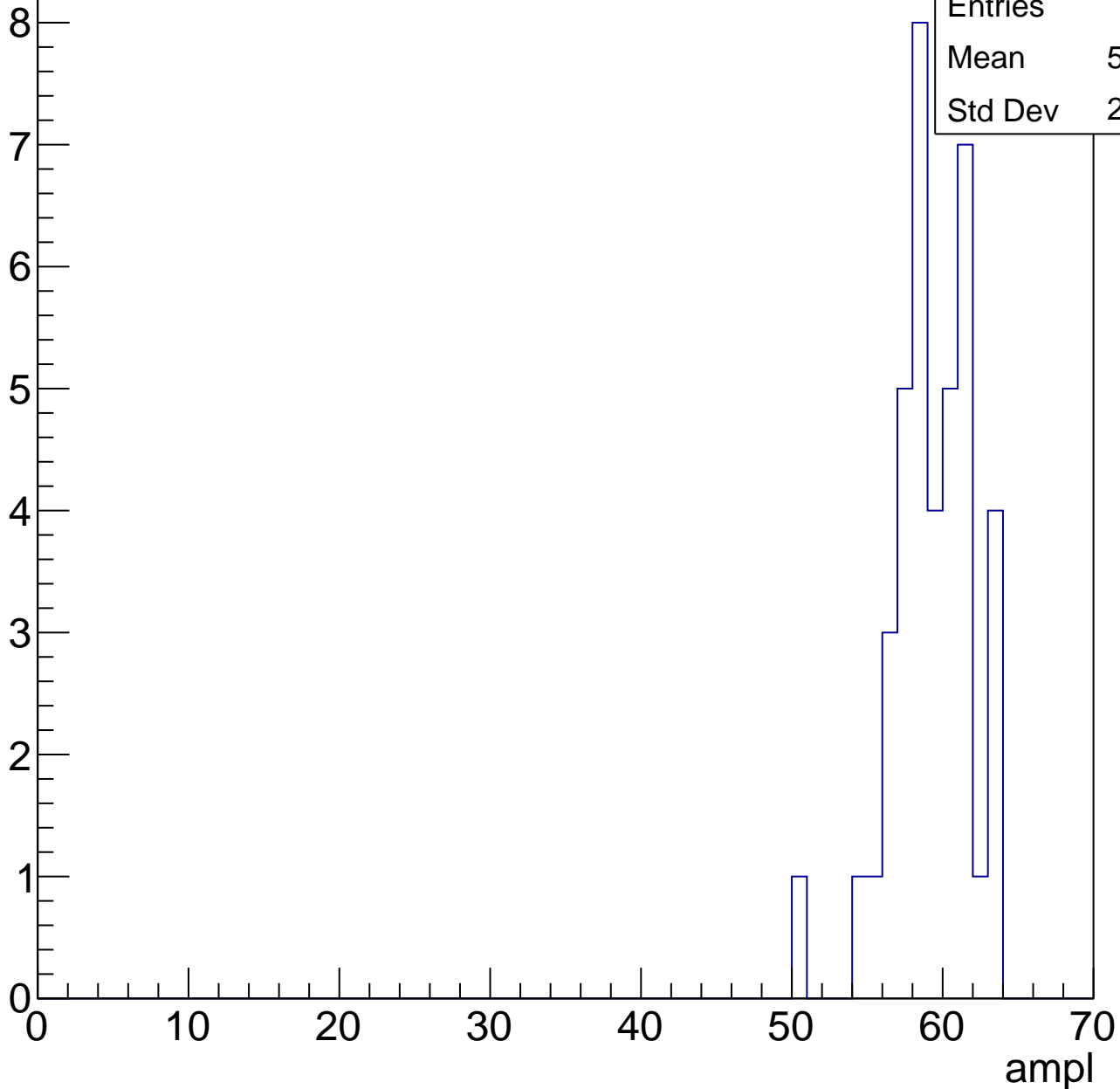


B1L103S, U7-ch72, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	58.83
Std Dev	2.654

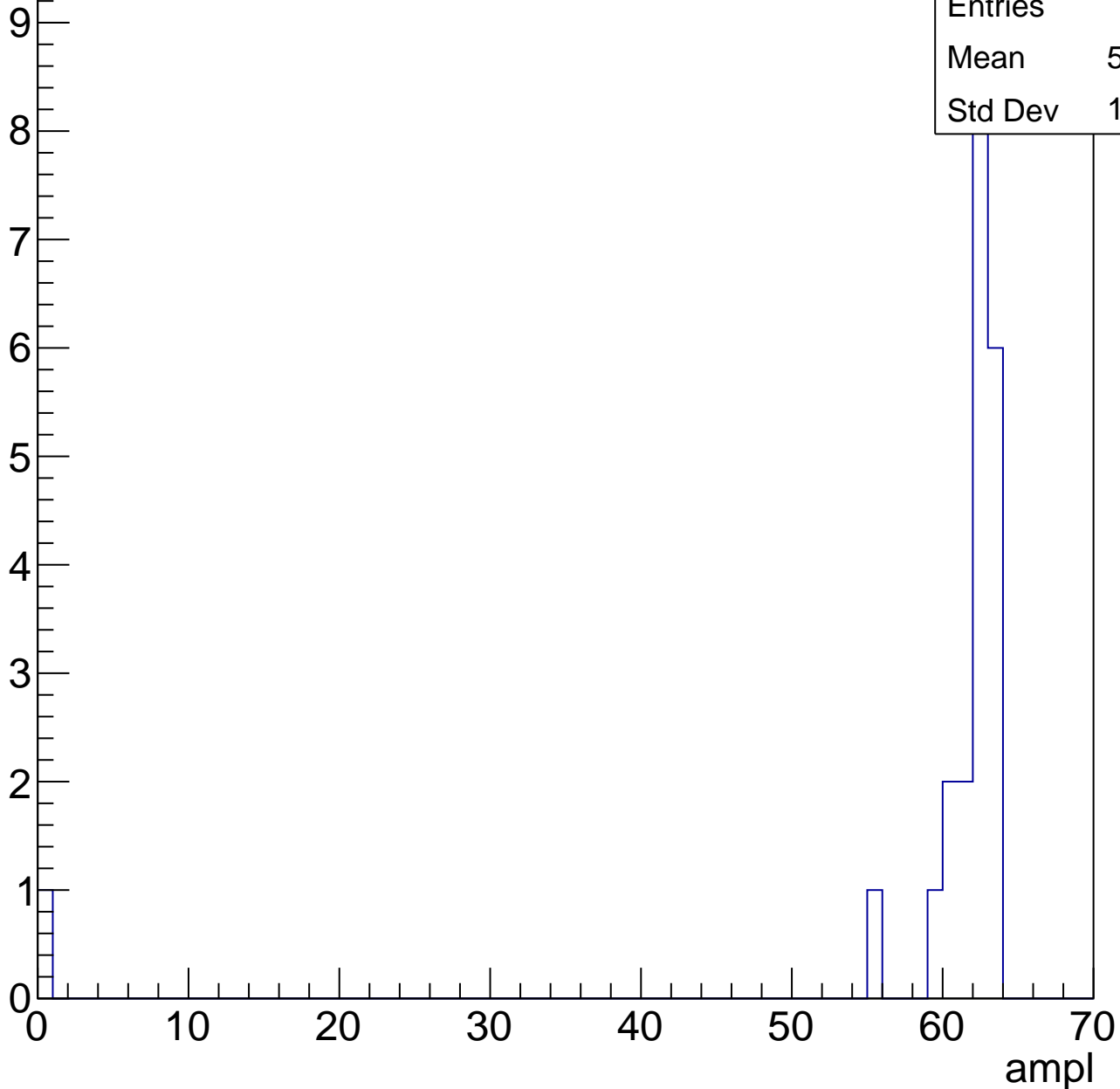


B1L103S, U7-ch72, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	22
Mean	58.73
Std Dev	12.94



B1L103S, U7-ch72, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U7-ch73, adc0

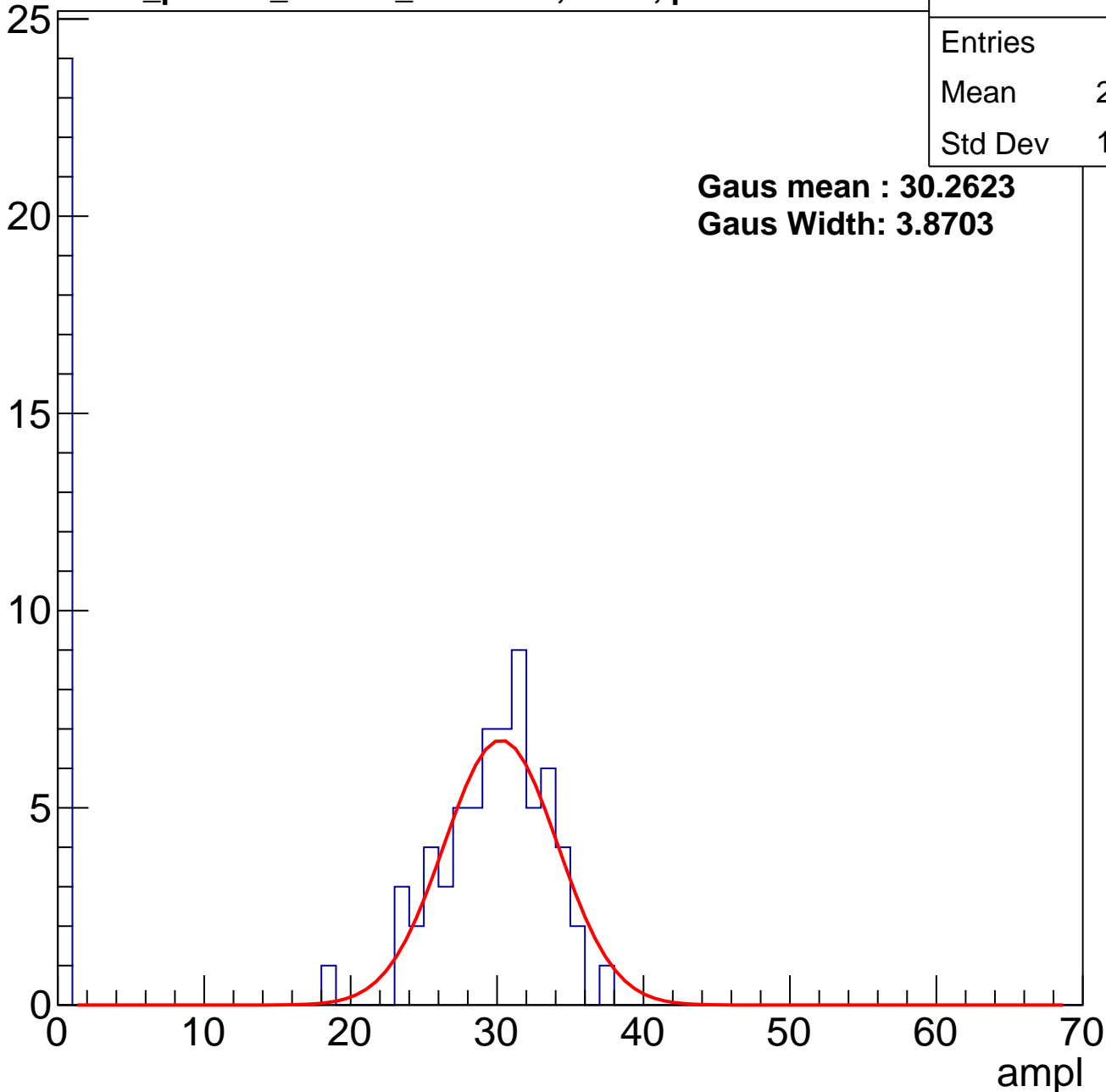
calib_packv5_041523_1651.root, FC#0, port C2

Entries	88
Mean	21.38
Std Dev	13.43

Gaus mean : 30.2623

Gaus Width: 3.8703

Entry



B1L103S, U7-ch73, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	83
Mean	31.24
Std Dev	12.69

Gaus mean : 36.8194

Gaus Width: 3.5246

Entry

10

8

6

4

2

0

0

10

20

30

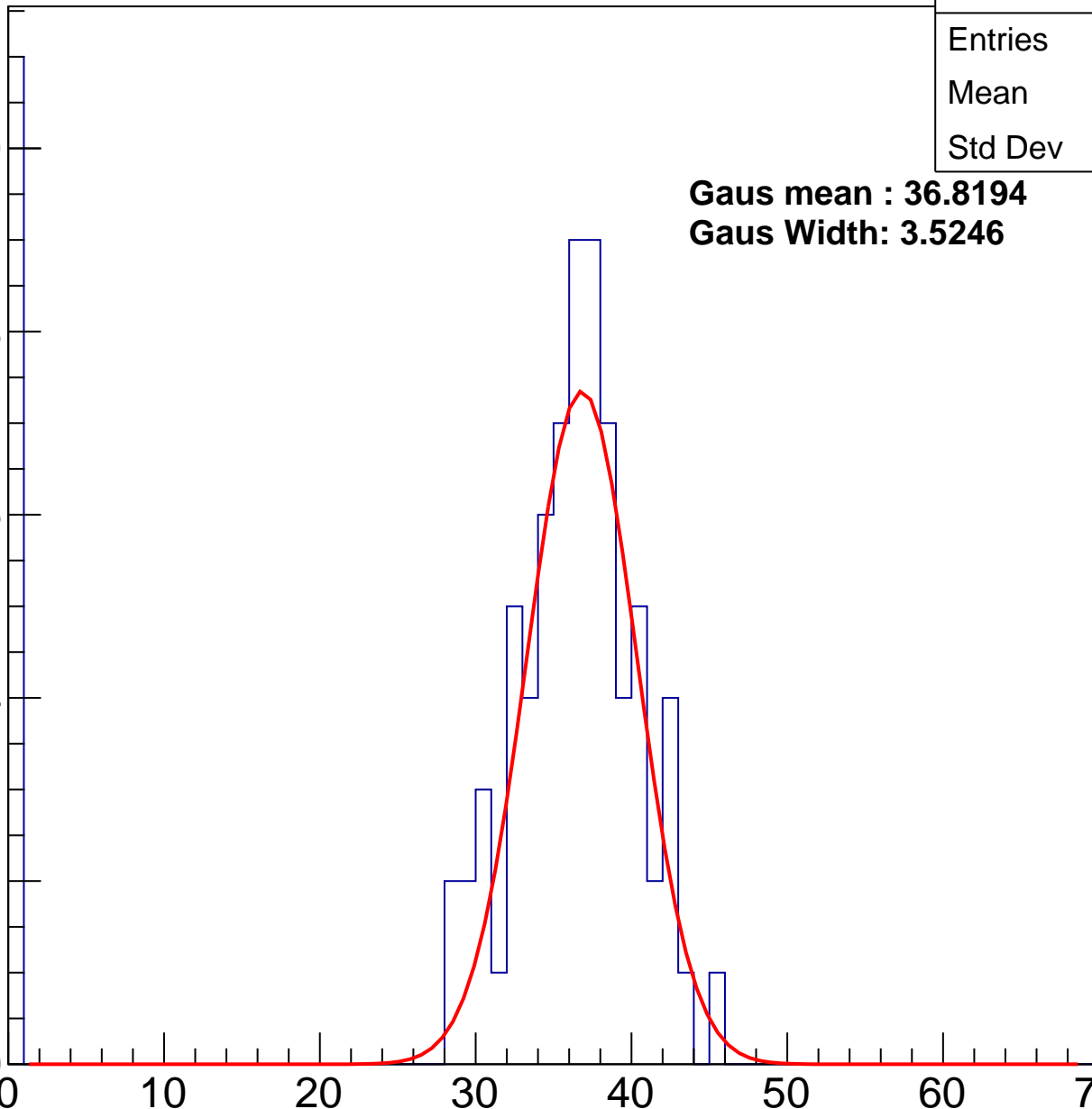
40

50

60

70

ampl



B1L103S, U7-ch73, adc2

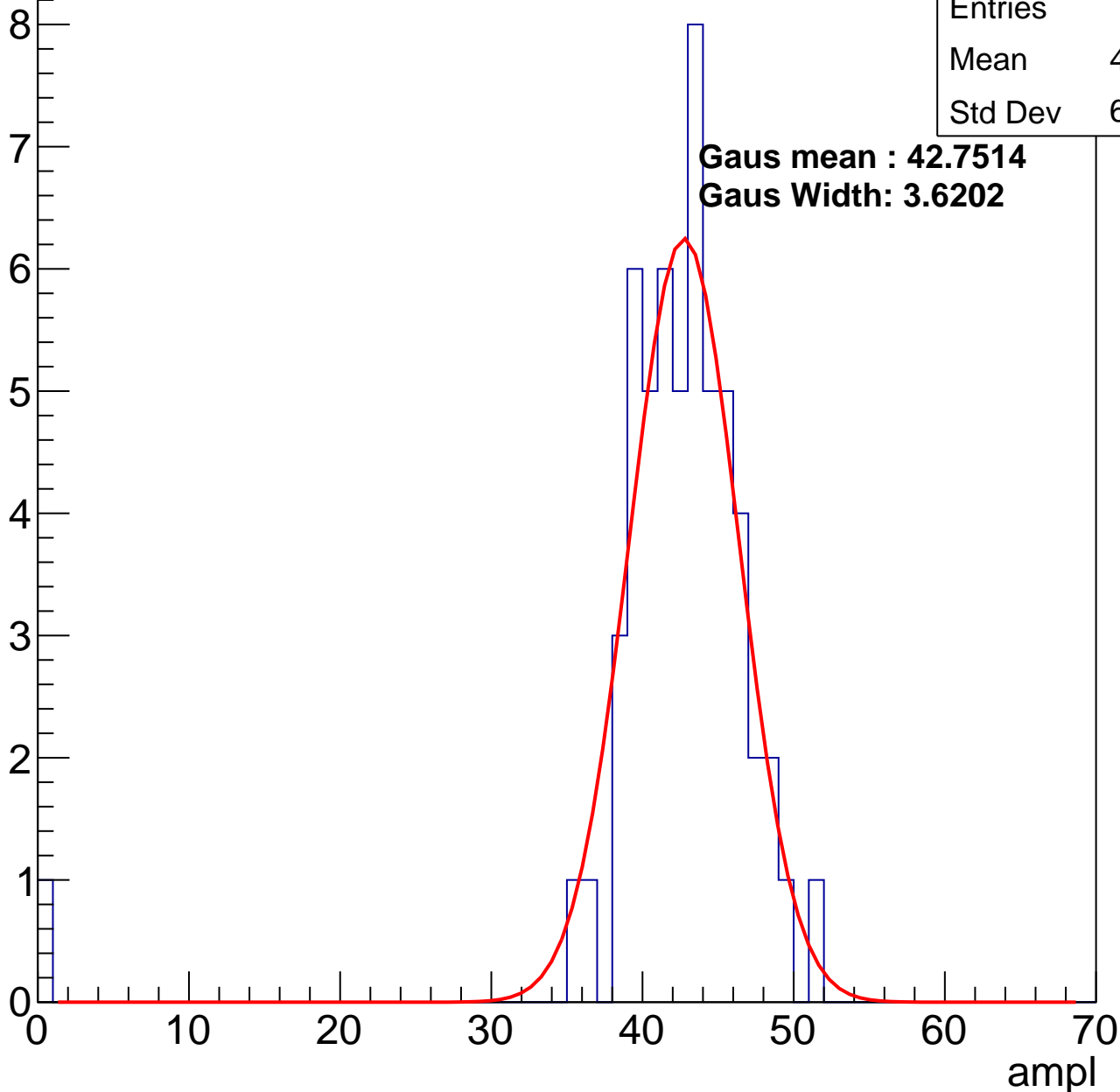
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	41.75
Std Dev	6.495

Gaus mean : 42.7514

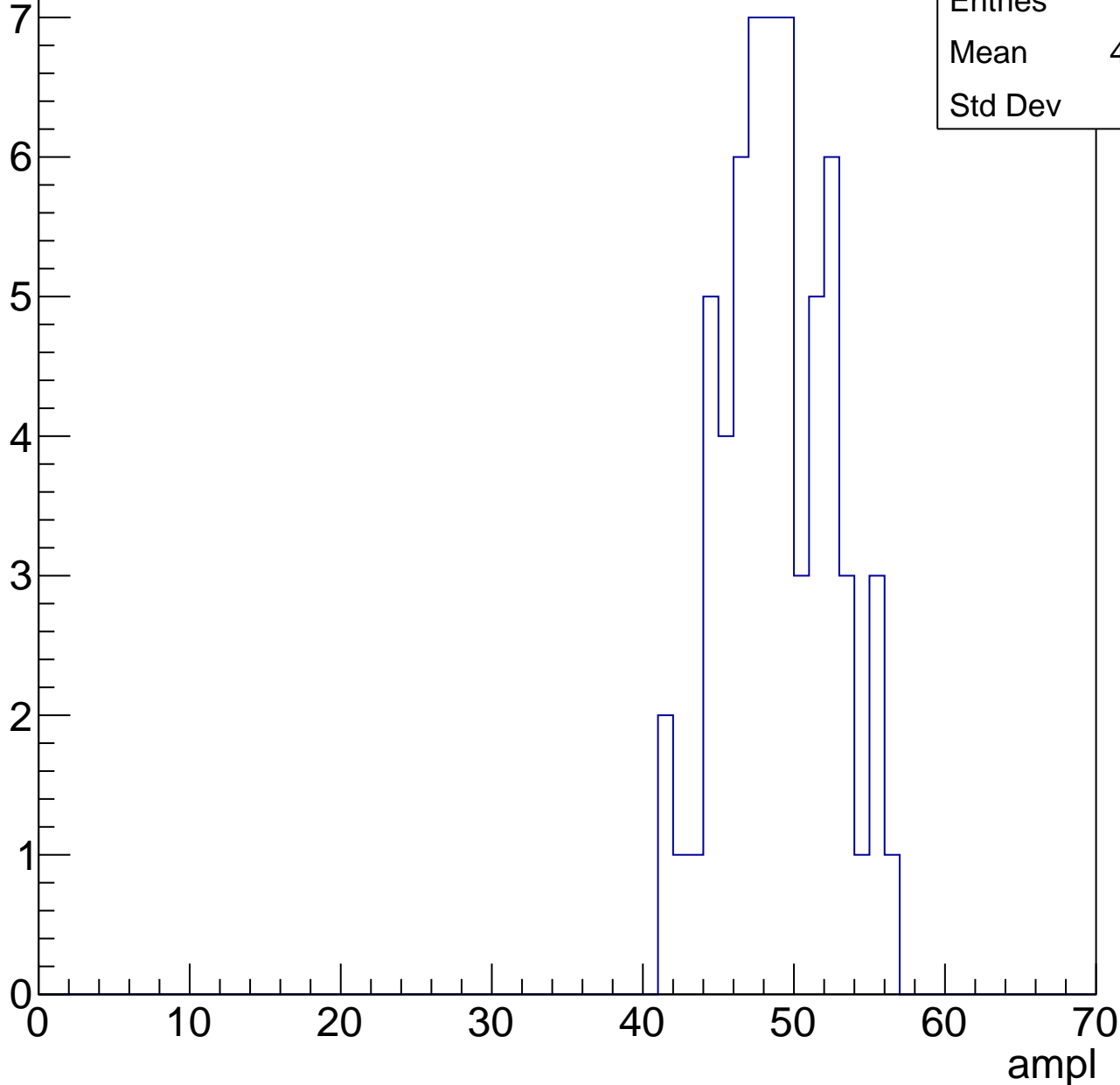
Gaus Width: 3.6202



B1L103S, U7-ch73, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

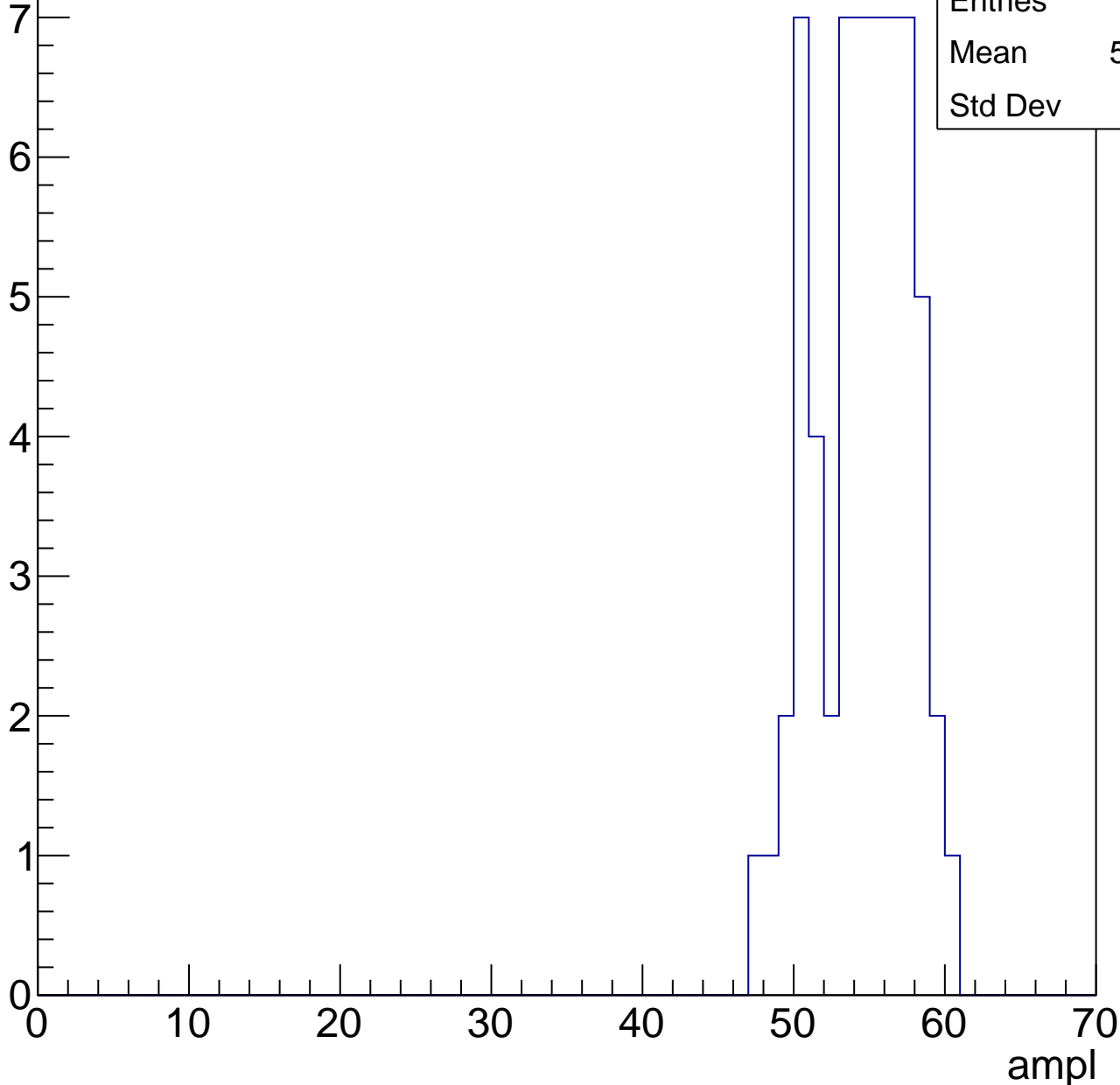


B1L103S, U7-ch73, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	54.07
Std Dev	3.06



B1L103S, U7-ch73, adc5

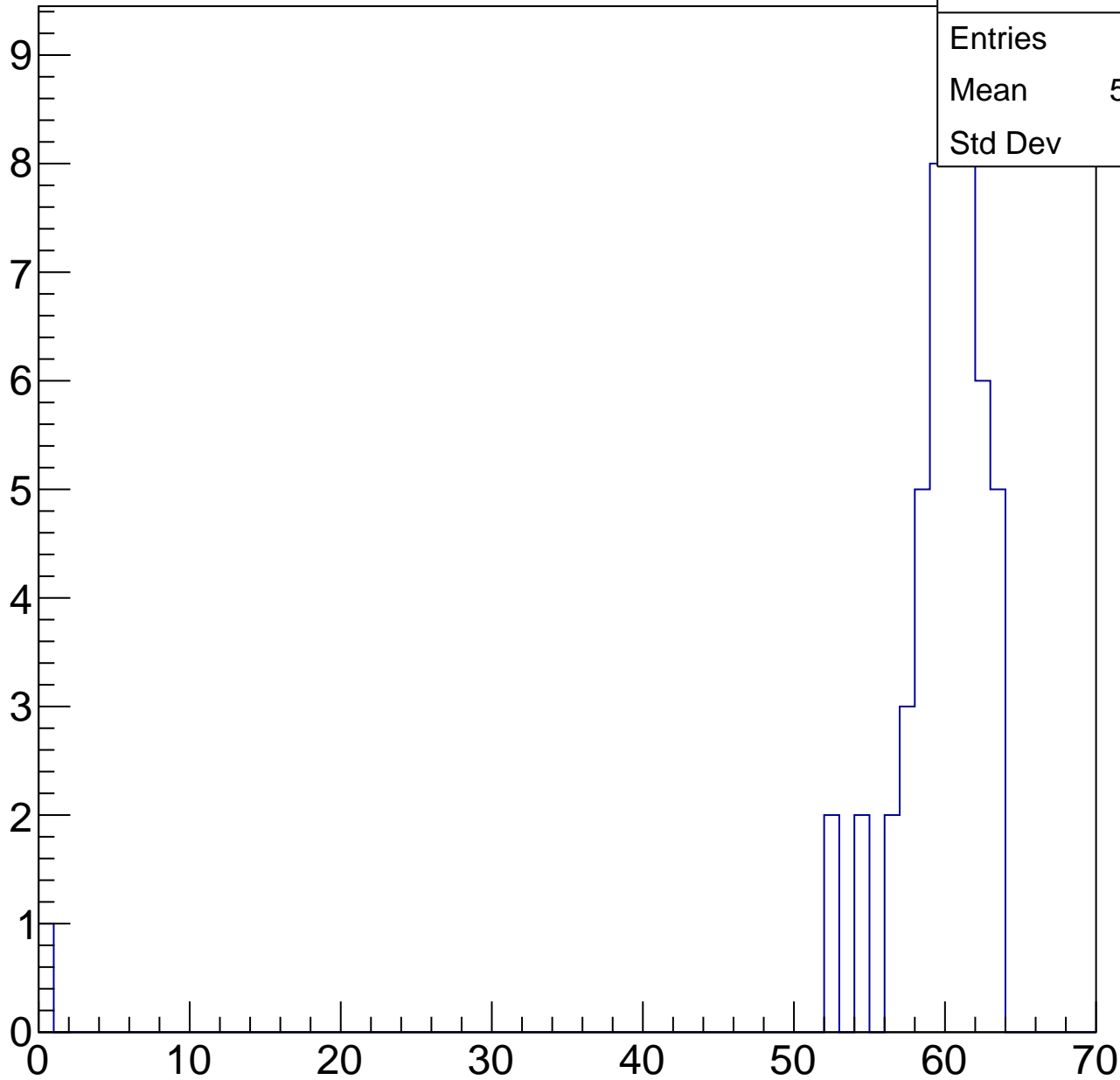
calib_packv5_041523_1651.root, FC#0, port C2

Entry

9
8
7
6
5
4
3
2
1
0

Entries	52
Mean	58.33
Std Dev	8.57

ampl

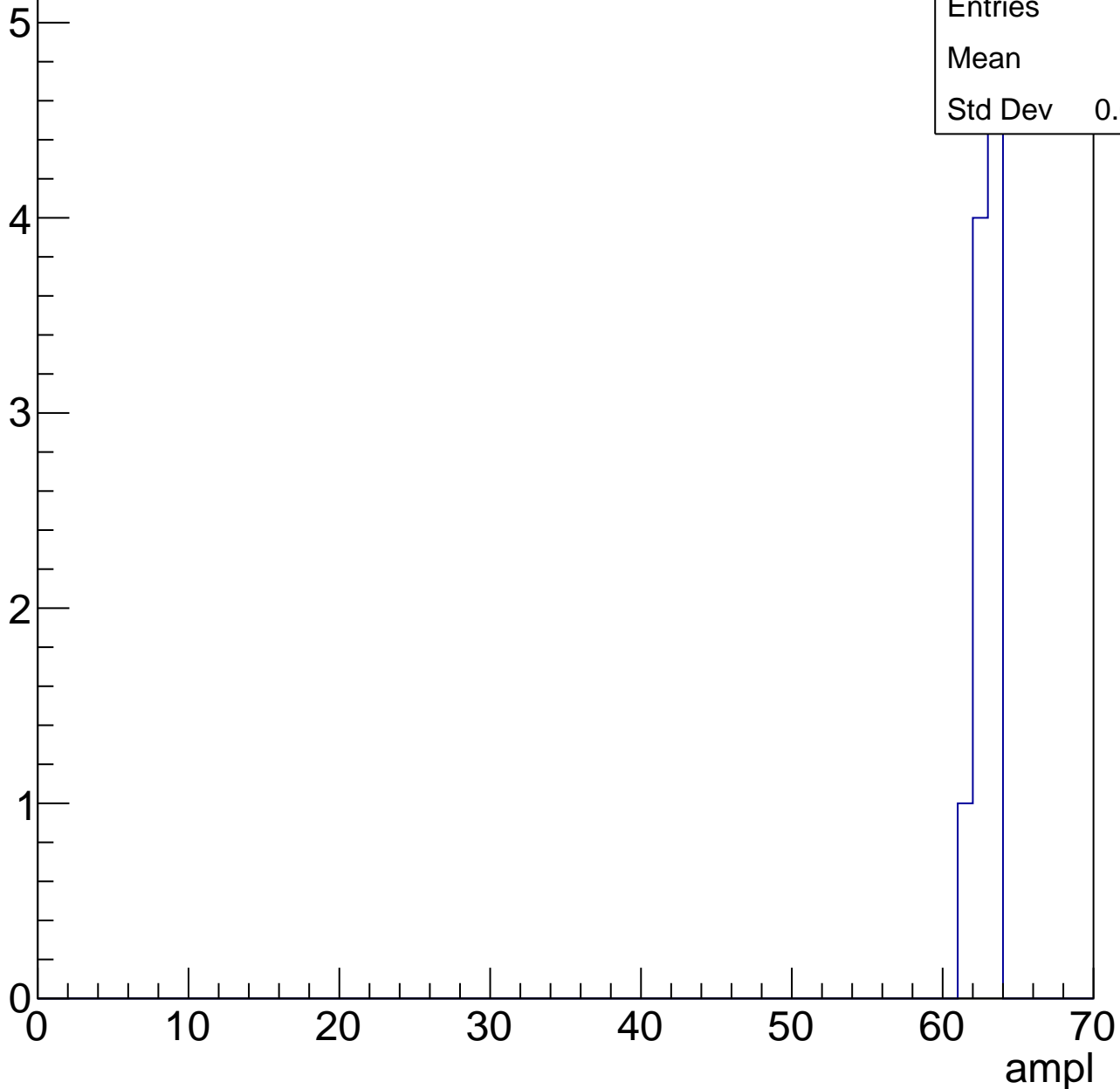


B1L103S, U7-ch73, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	10
Mean	62.4
Std Dev	0.6633



B1L103S, U7-ch73, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U7-ch74, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	69
Mean	22.51
Std Dev	11.21

Gaus mean : 28.9899

Gaus Width: 3.1784

Entry

12

10

8

6

4

2

0

0

10

20

30

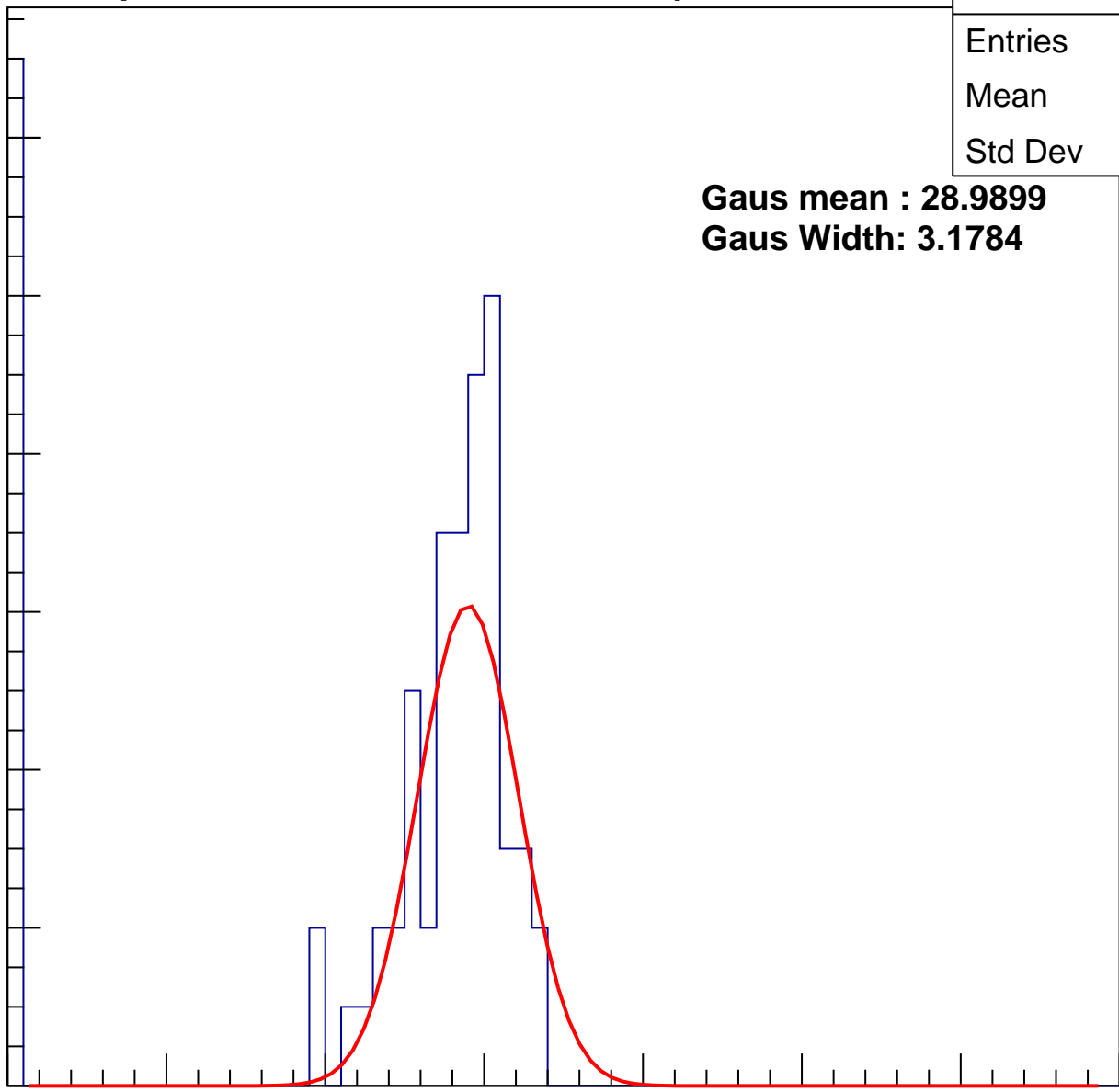
40

50

60

70

ampl



B1L103S, U7-ch74, adc1

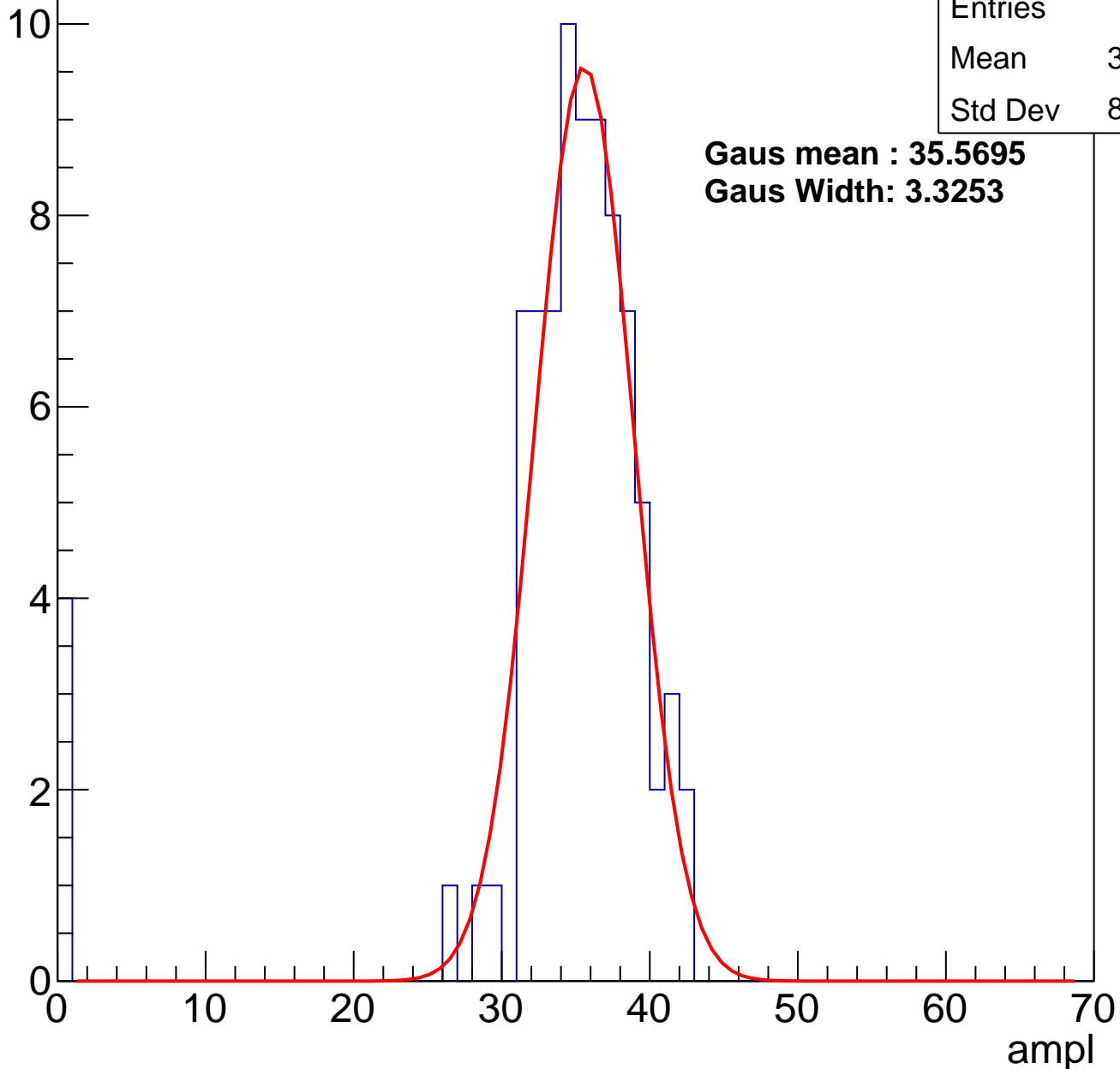
calib_packv5_041523_1651.root, FC#0, port C2

Entries	83
Mean	33.47
Std Dev	8.159

Gaus mean : 35.5695

Gaus Width: 3.3253

Entry



B1L103S, U7-ch74, adc2

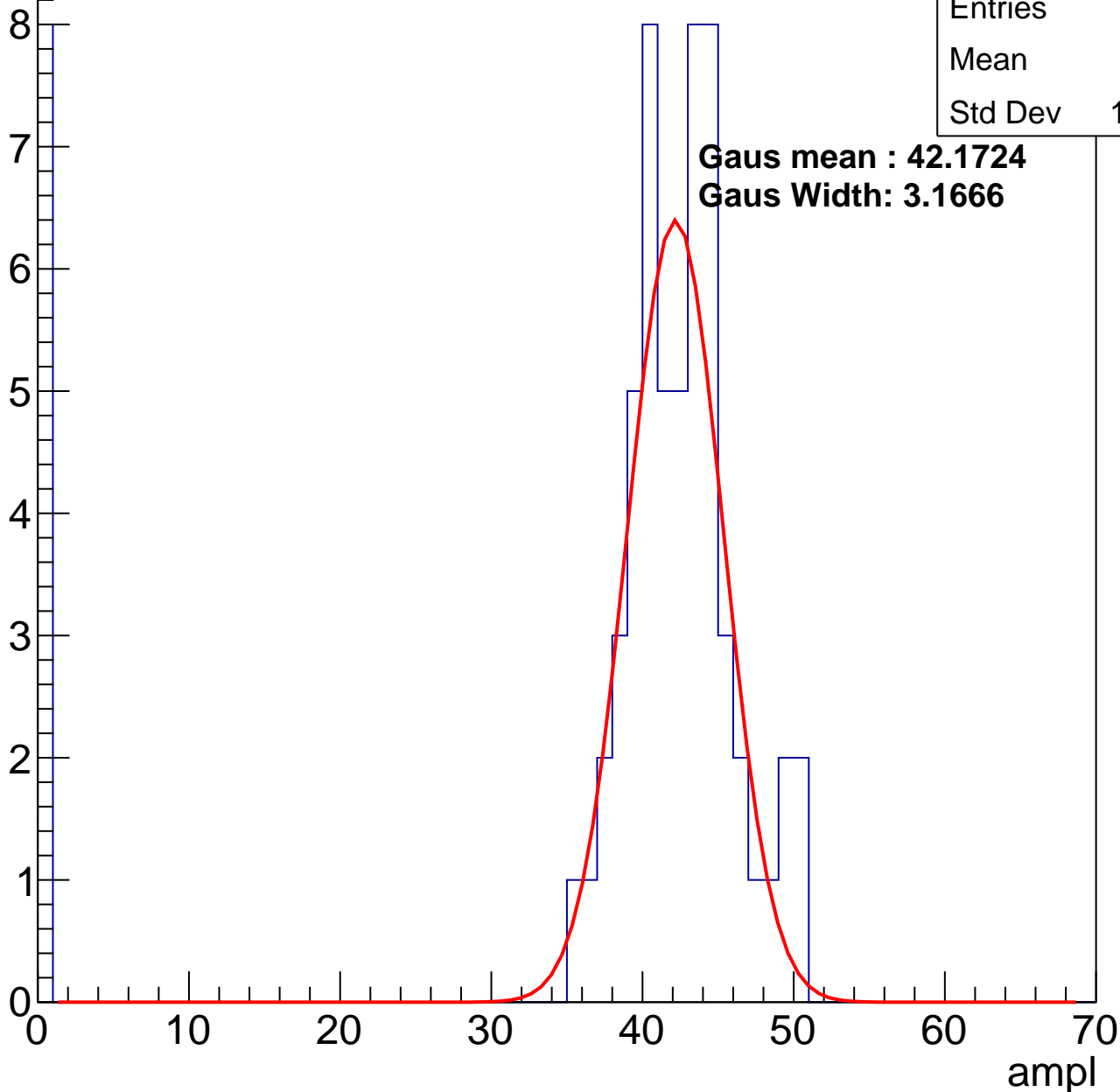
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	37
Std Dev	14.22

Gaus mean : 42.1724

Gaus Width: 3.1666

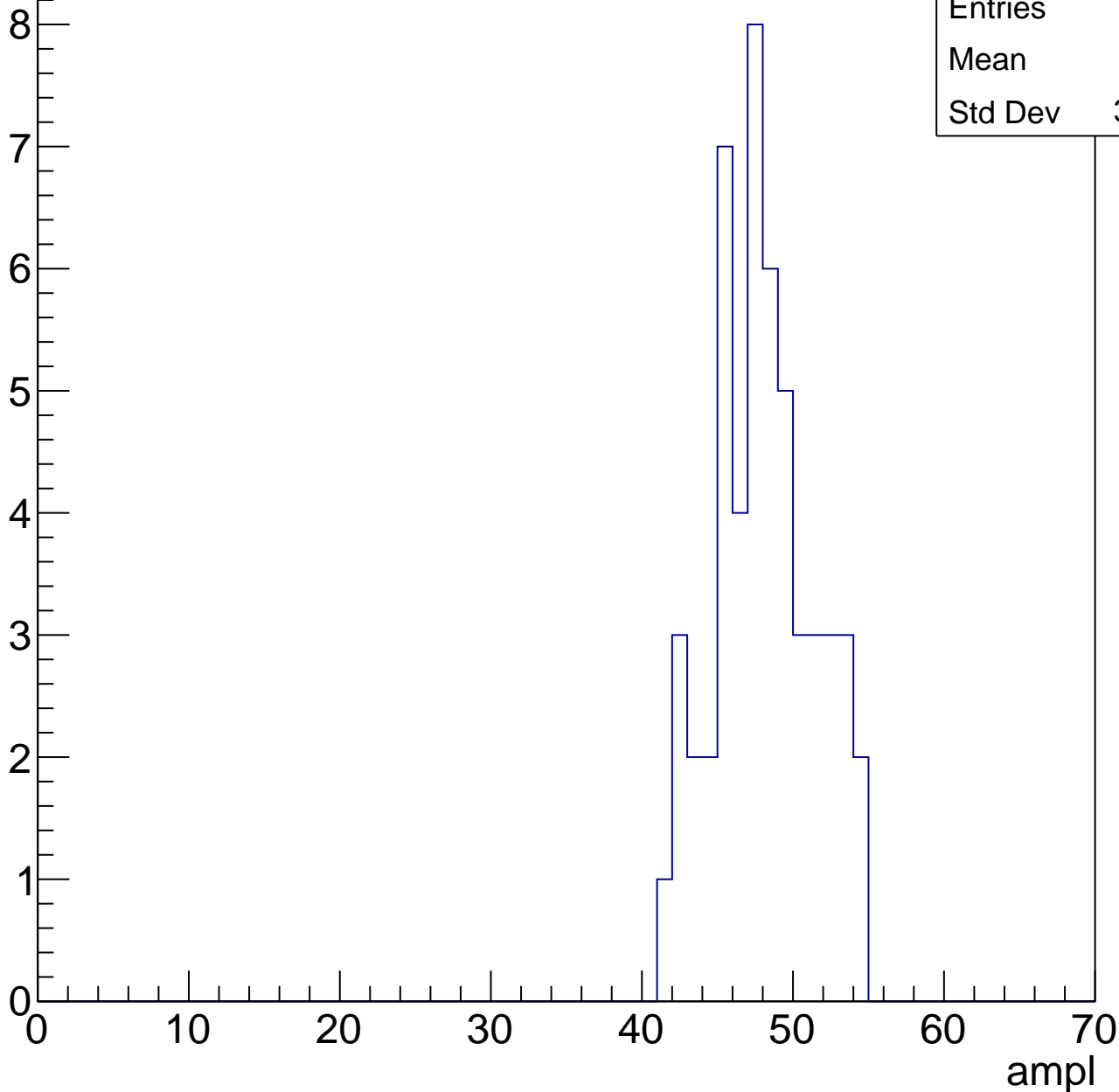


B1L103S, U7-ch74, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	47.6
Std Dev	3.271

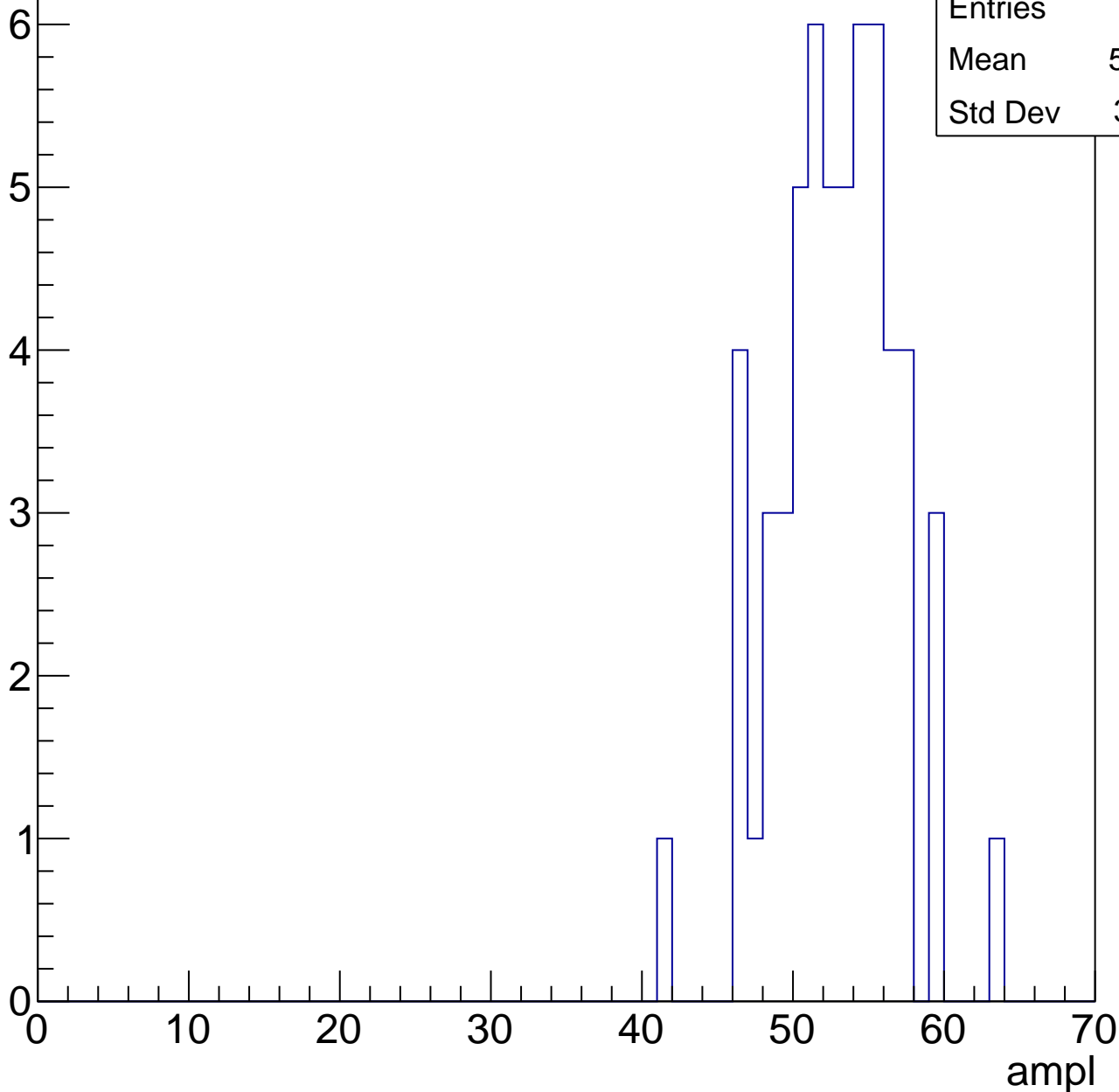


B1L103S, U7-ch74, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	52.46
Std Dev	3.961

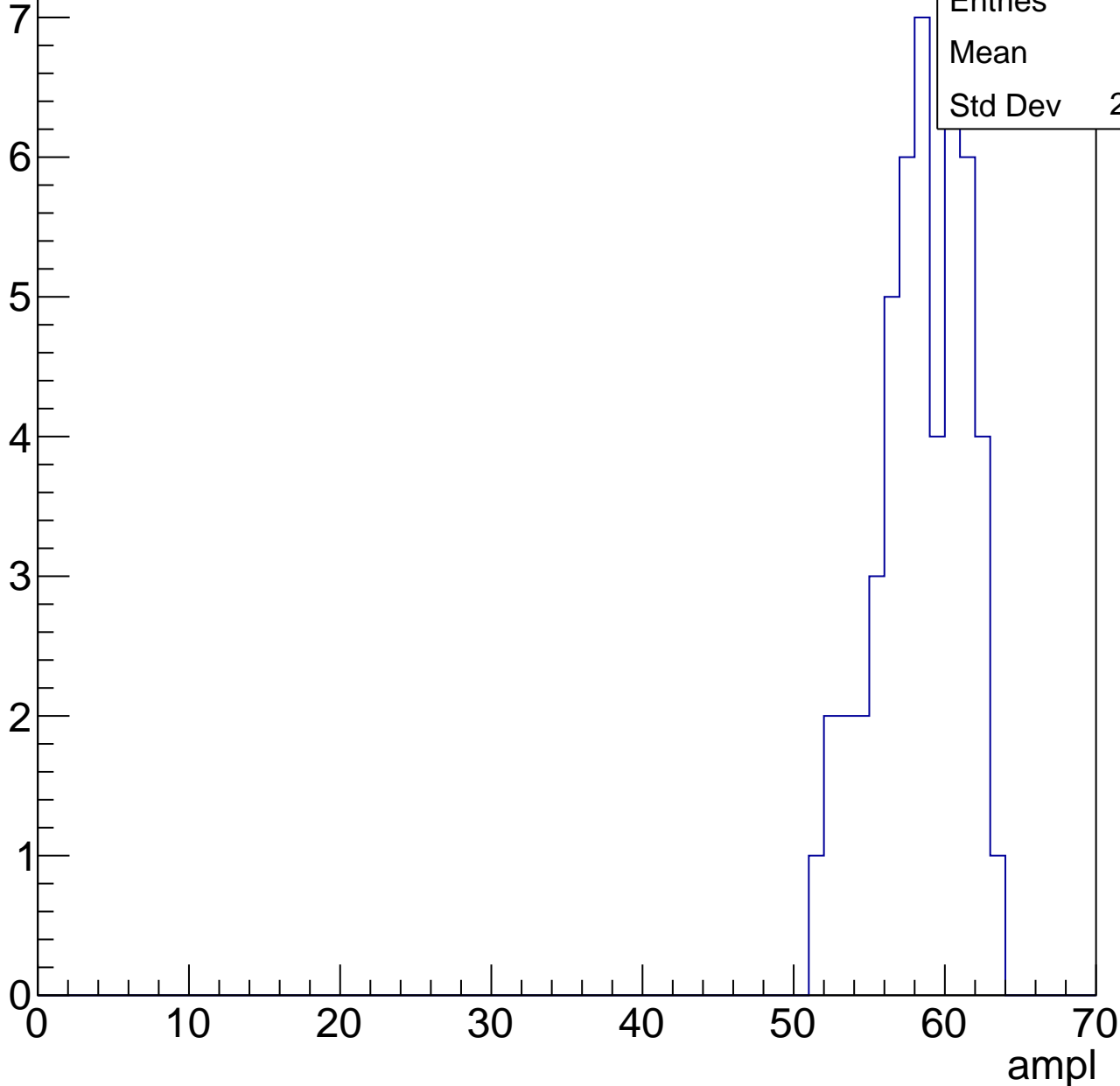


B1L103S, U7-ch74, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	57.9
Std Dev	2.934

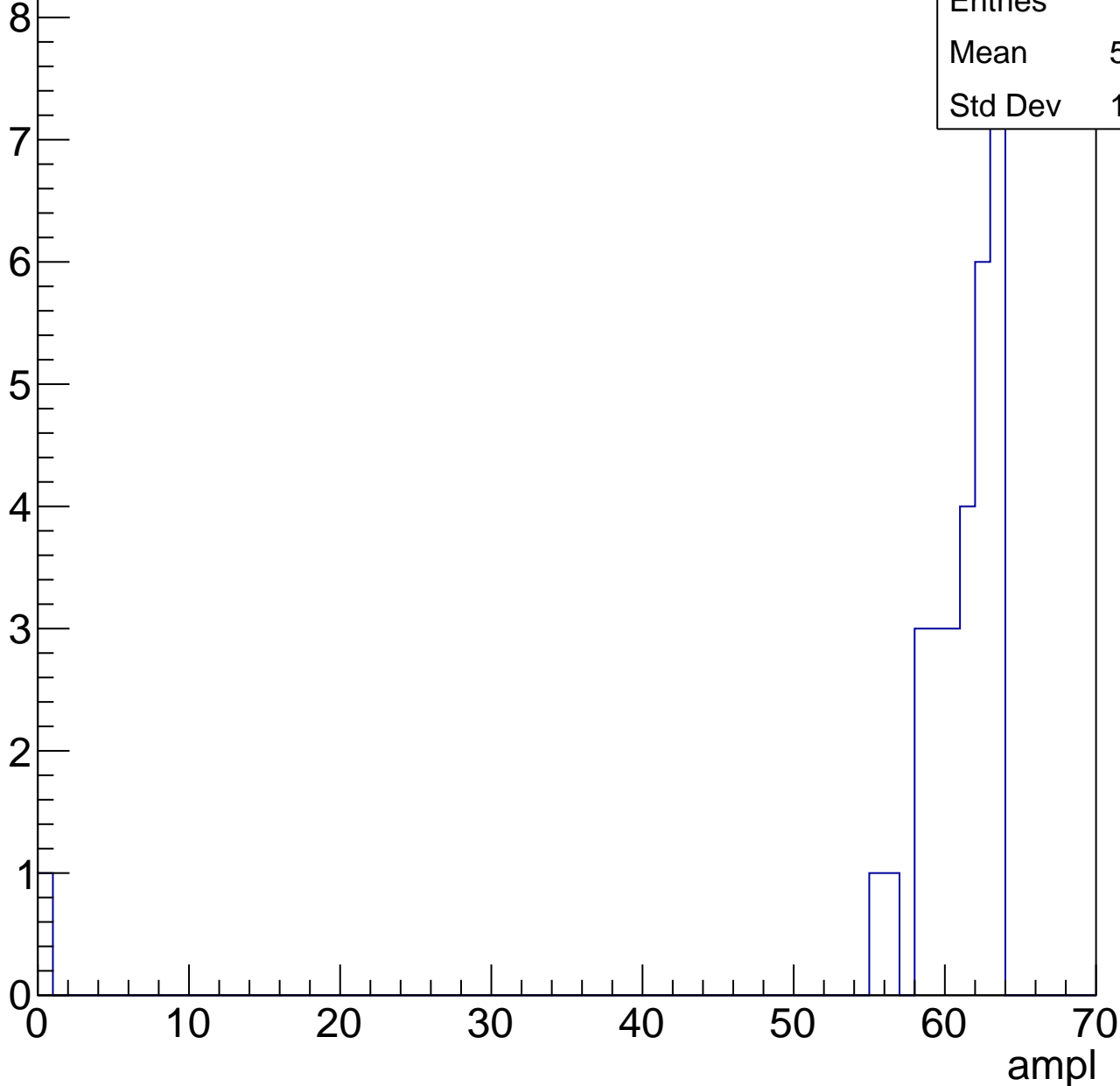


B1L103S, U7-ch74, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	30
Mean	58.73
Std Dev	11.12



B1L103S, U7-ch74, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

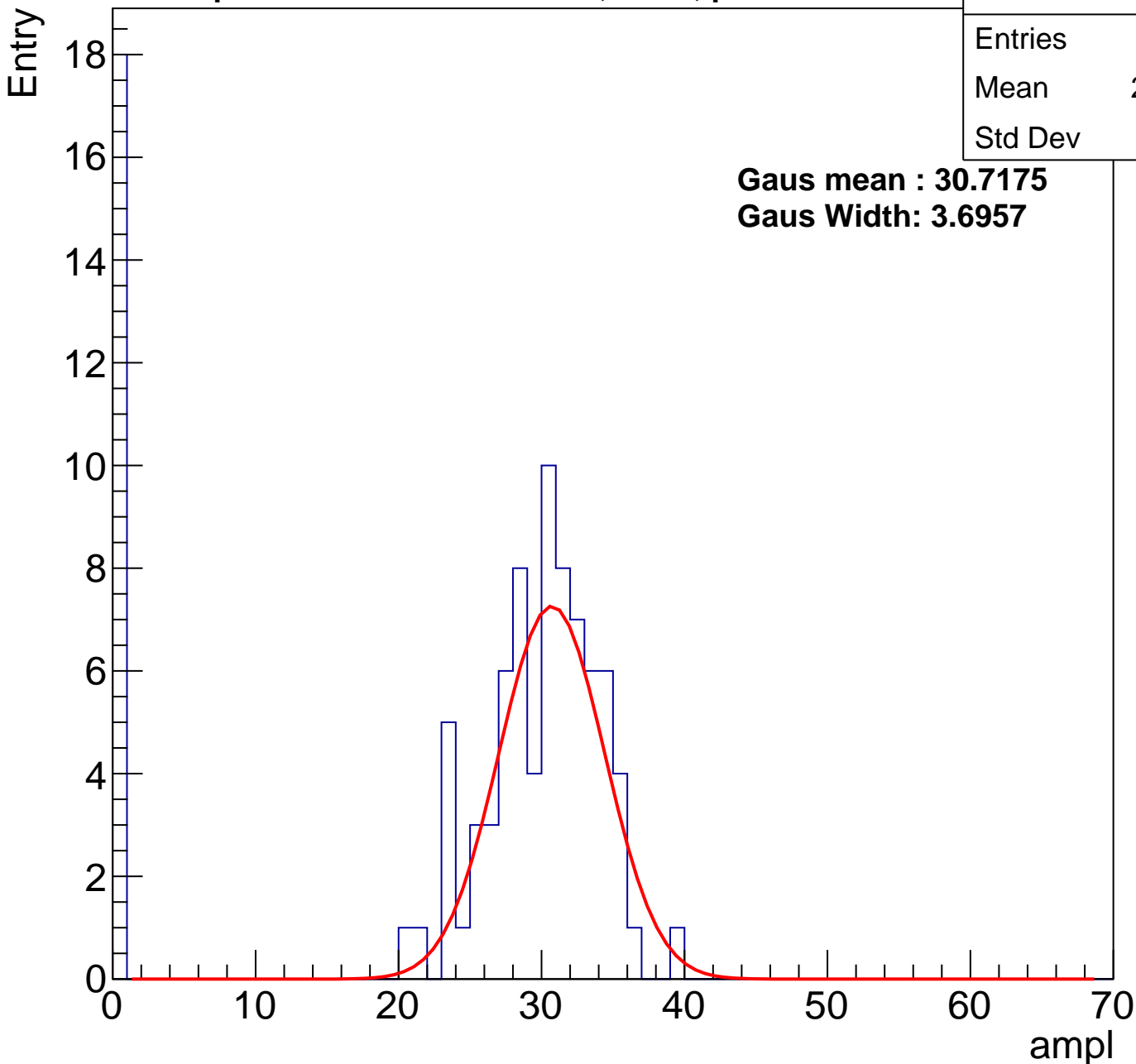
B1L103S, U7-ch75, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	93
Mean	23.91
Std Dev	12.2

Gaus mean : 30.7175

Gaus Width: 3.6957



B1L103S, U7-ch75, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	74
Mean	31.07
Std Dev	13.36

Gaus mean : 36.9849

Gaus Width: 3.6917

Entry

10

8

6

4

2

0

0

10

20

30

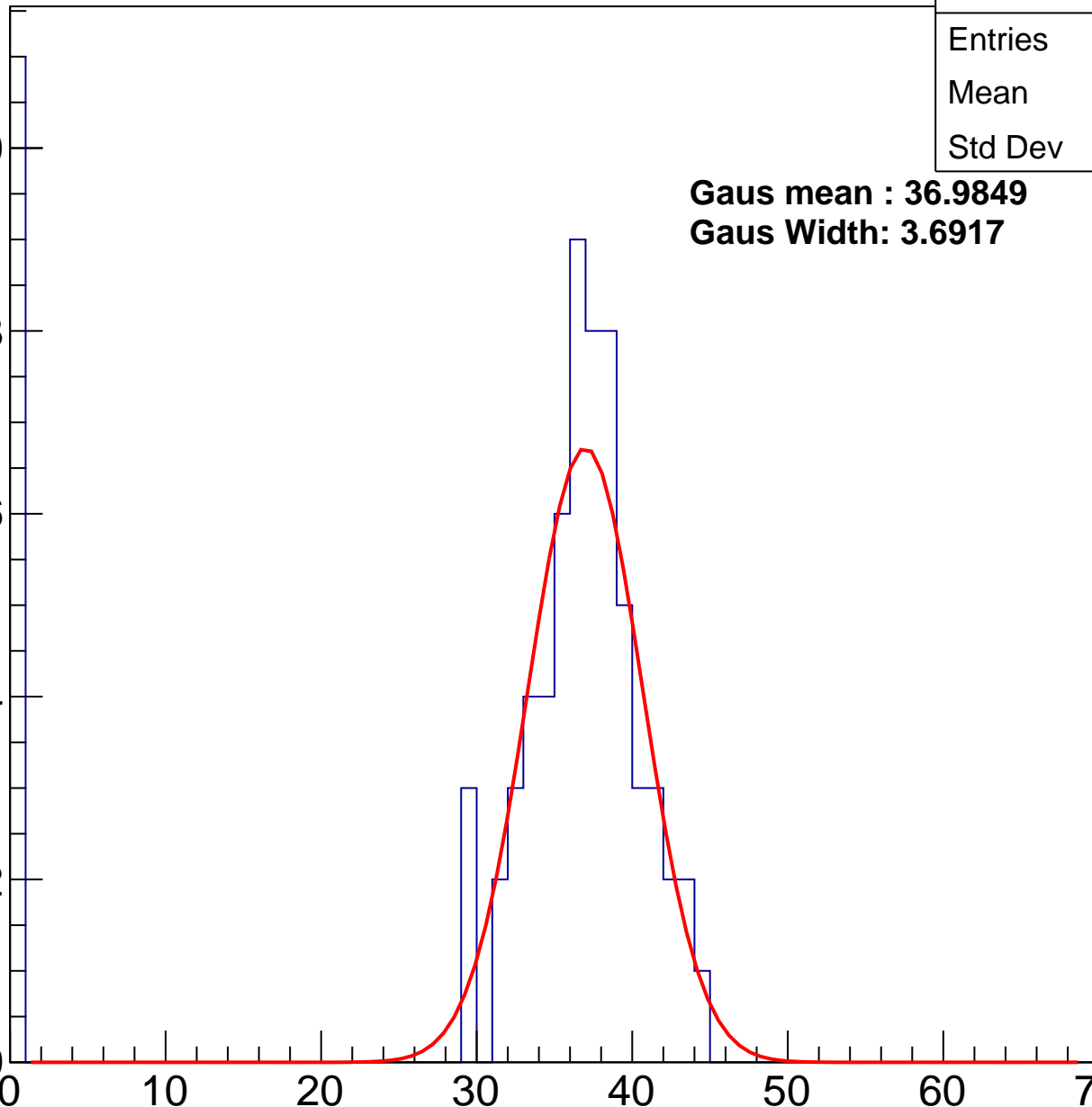
40

50

60

70

ampl



B1L103S, U7-ch75, adc2

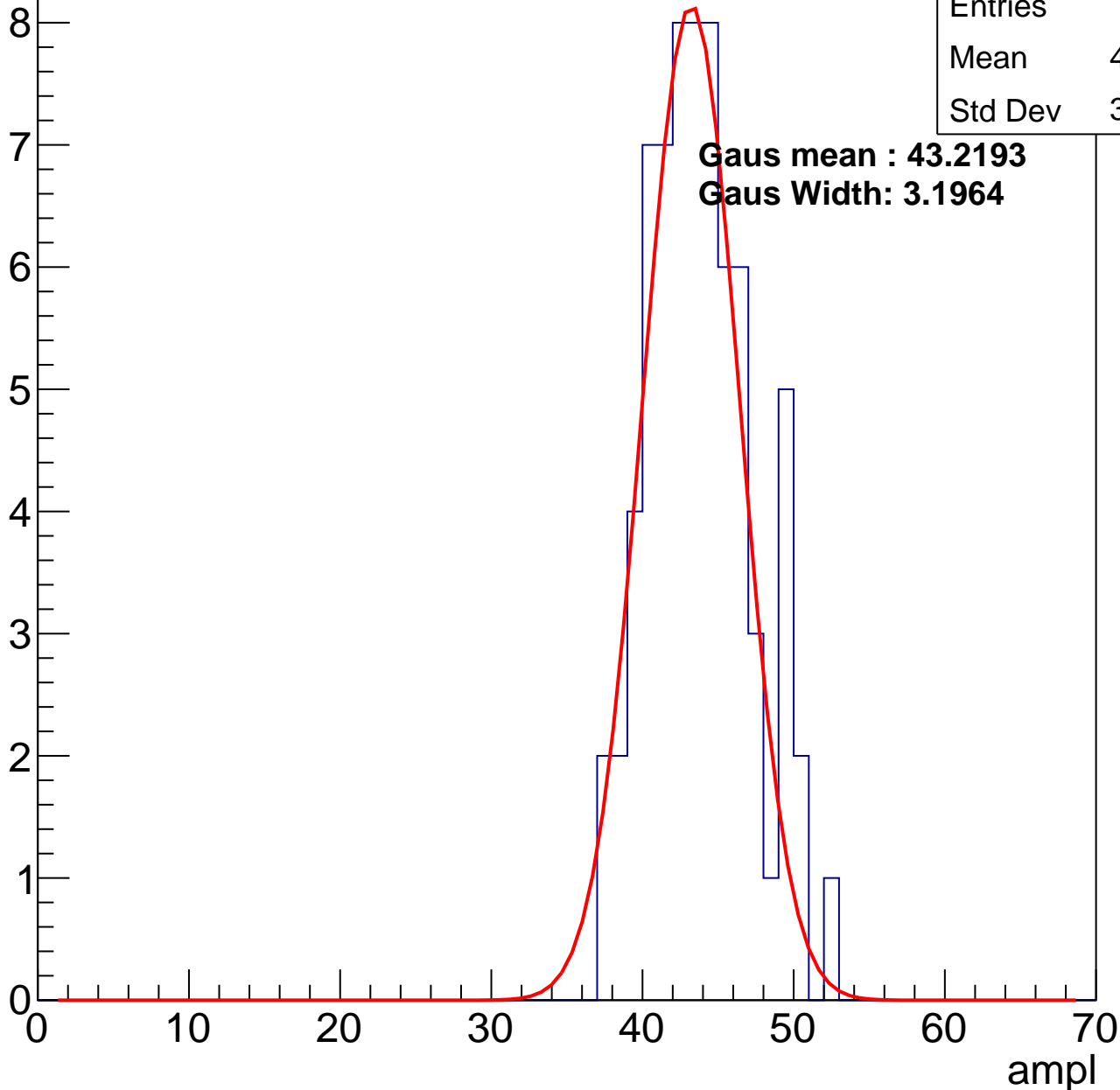
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	43.39
Std Dev	3.365

Gaus mean : 43.2193

Gaus Width: 3.1964

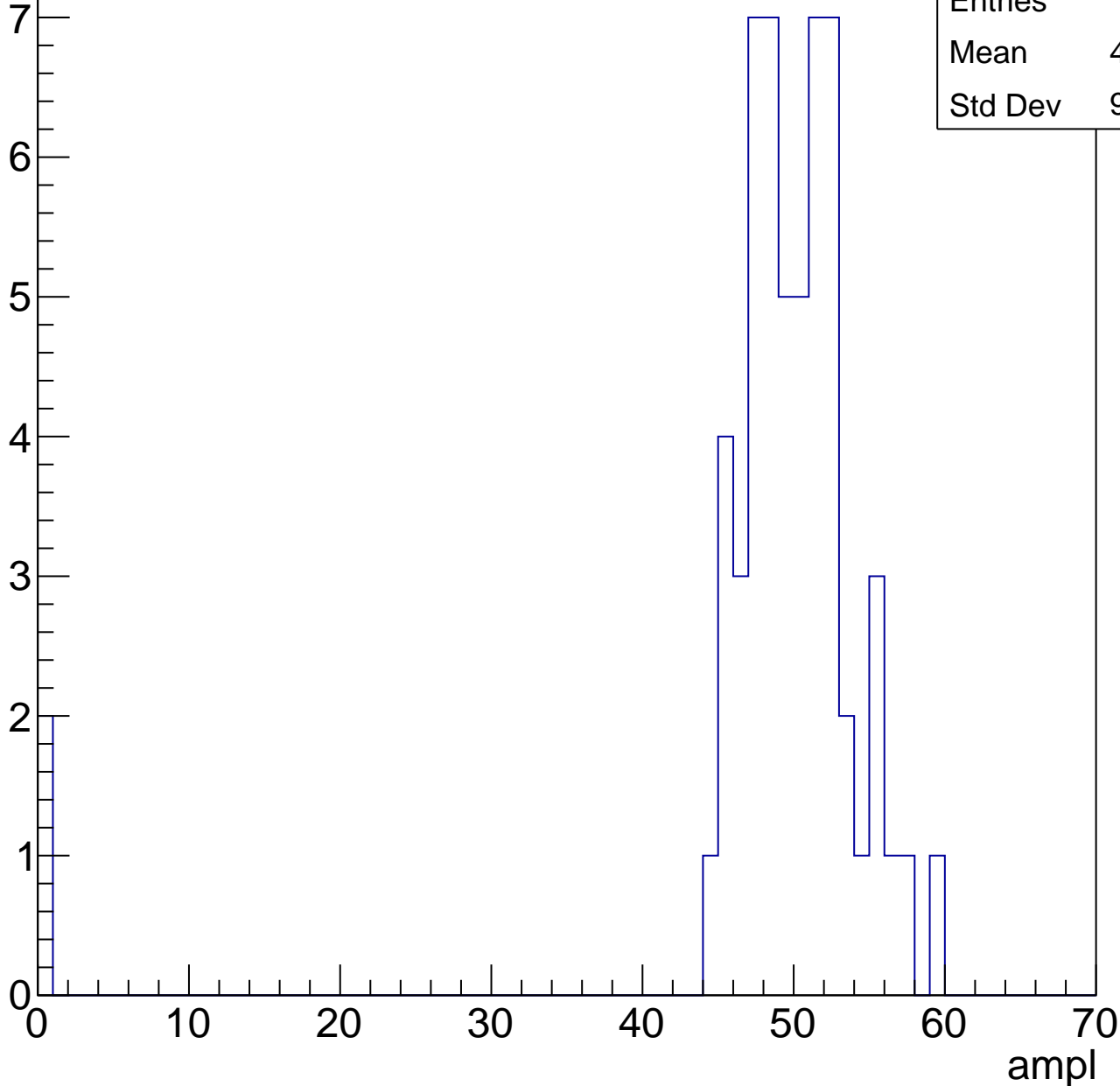


B1L103S, U7-ch75, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	48.07
Std Dev	9.713

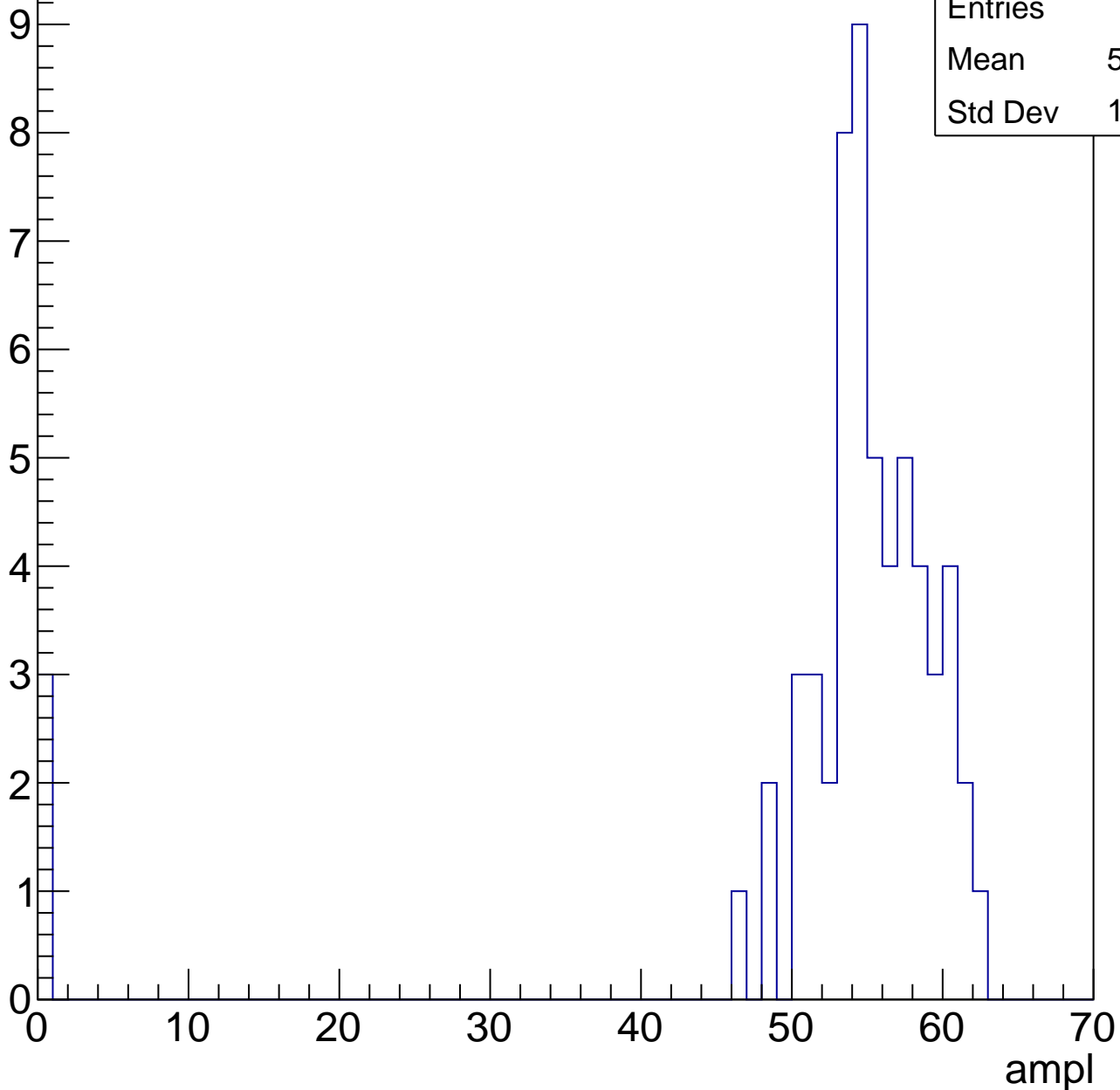


B1L103S, U7-ch75, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	52.14
Std Dev	12.54



B1L103S, U7-ch75, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

7

6

5

4

3

2

1

0

Entries

41

Mean

59.44

Std Dev

2.42

0

ampl

0

10

20

30

40

50

60

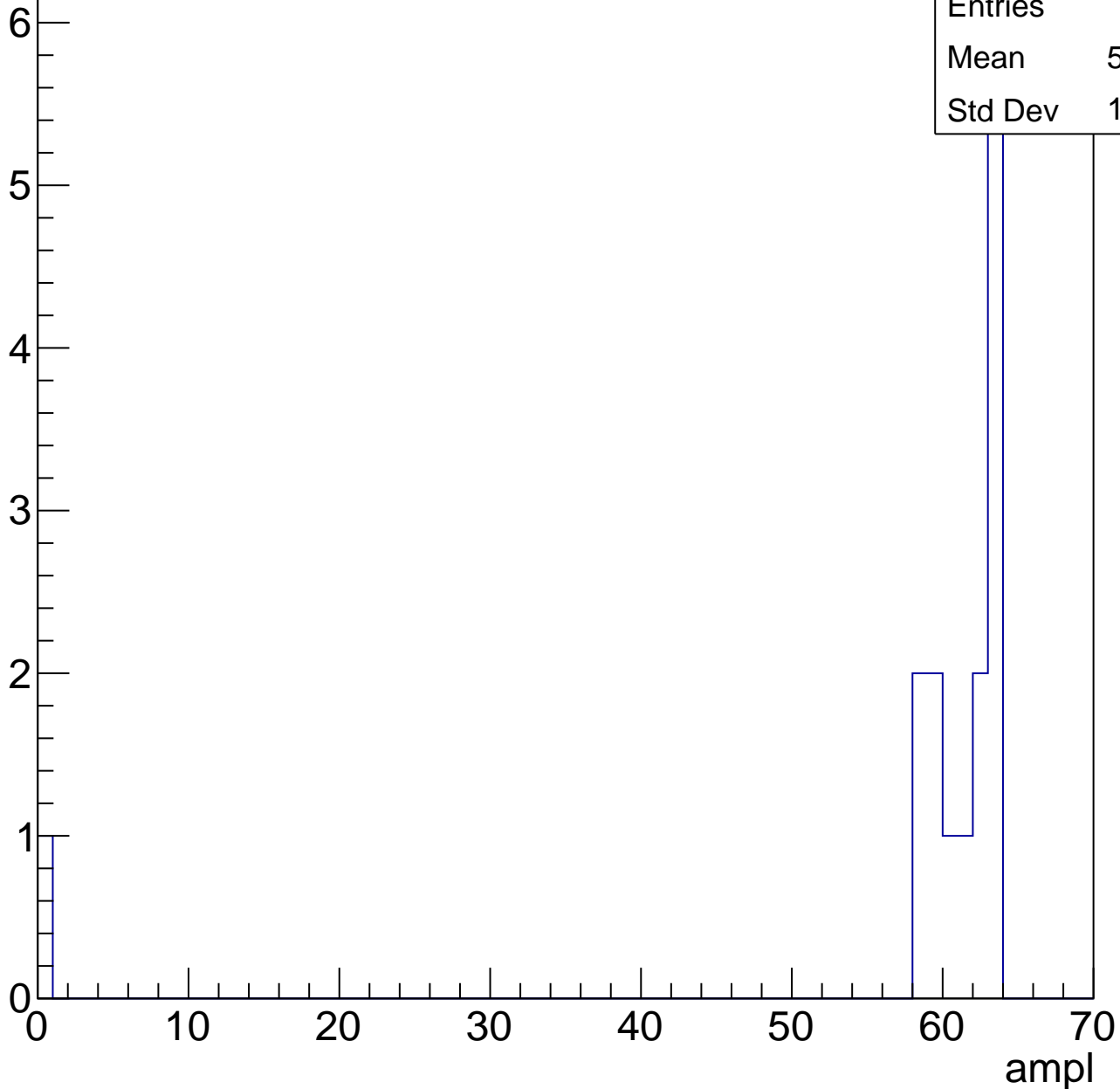
70

B1L103S, U7-ch75, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	15
Mean	57.13
Std Dev	15.38



B1L103S, U7-ch75, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	20
Mean	3.1
Std Dev	13.51

ampl

0 10 20 30 40 50 60 70

B1L103S, U7-ch76, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	79
Mean	24.99
Std Dev	10.49

Gaus mean : 29.4748

Gaus Width: 3.3483

Entry

10

8

6

4

2

0

0

10

20

30

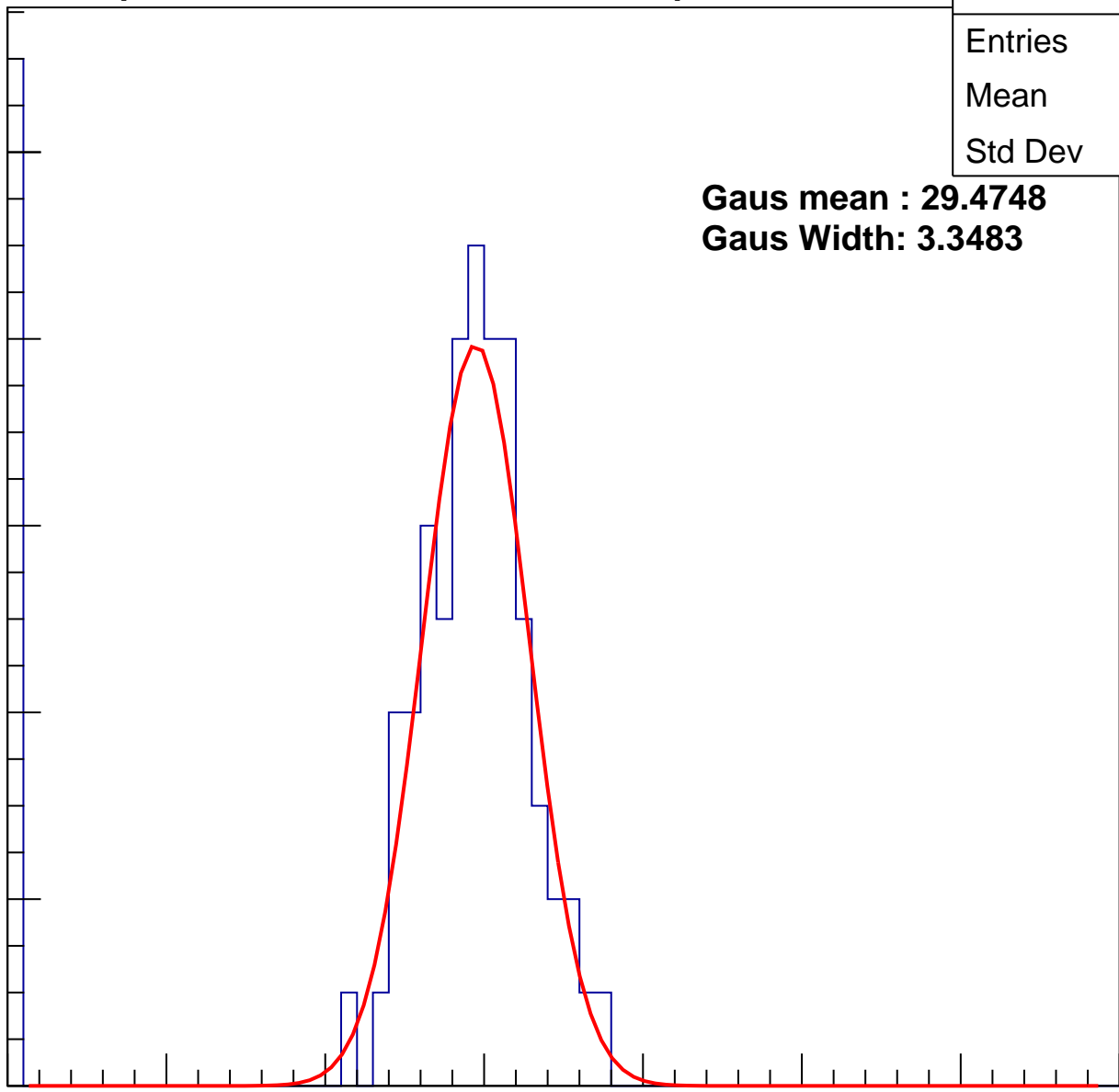
40

50

60

70

ampl



B1L103S, U7-ch76, adc1

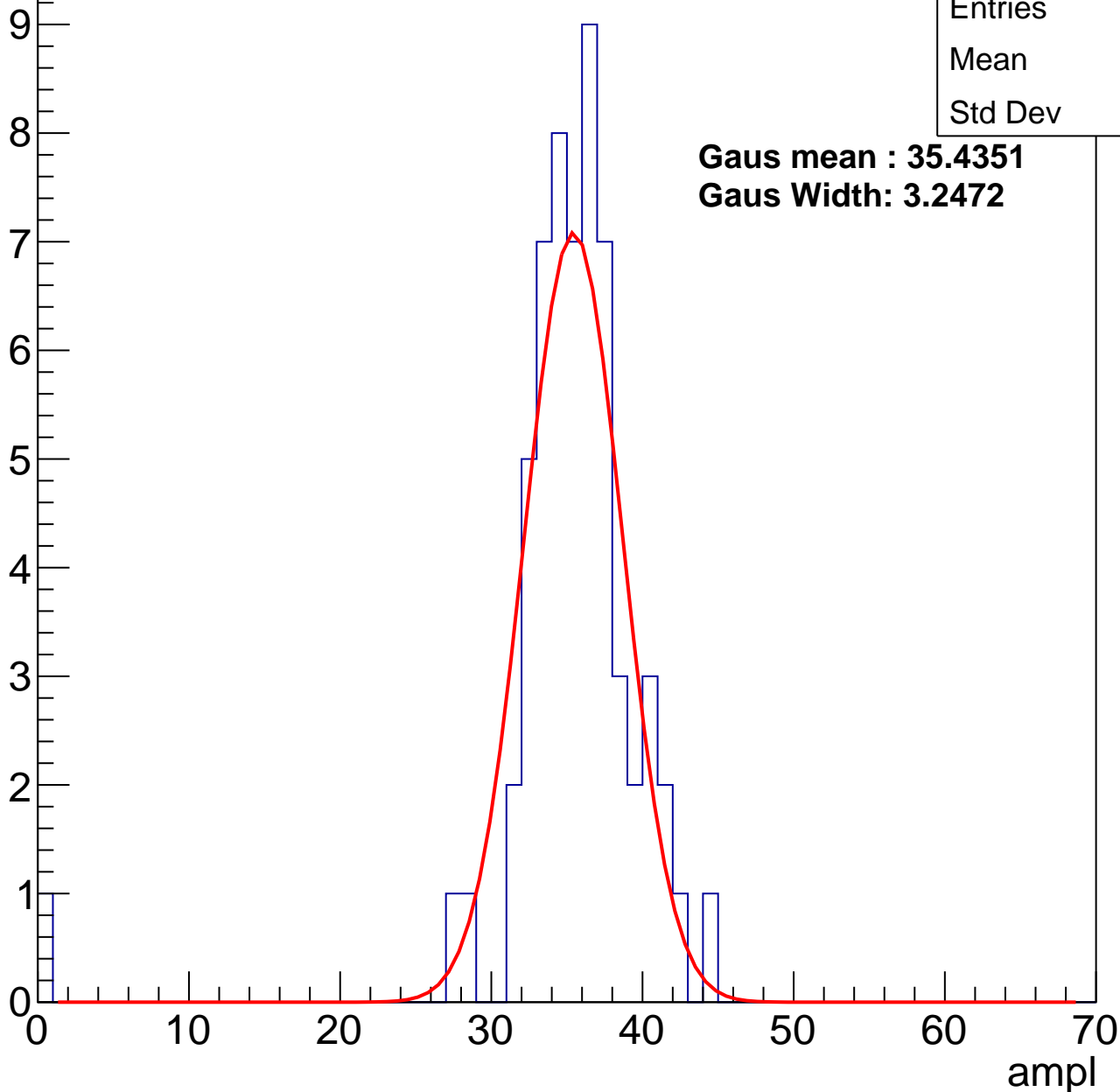
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	34.8
Std Dev	5.51

Gaus mean : 35.4351

Gaus Width: 3.2472



B1L103S, U7-ch76, adc2

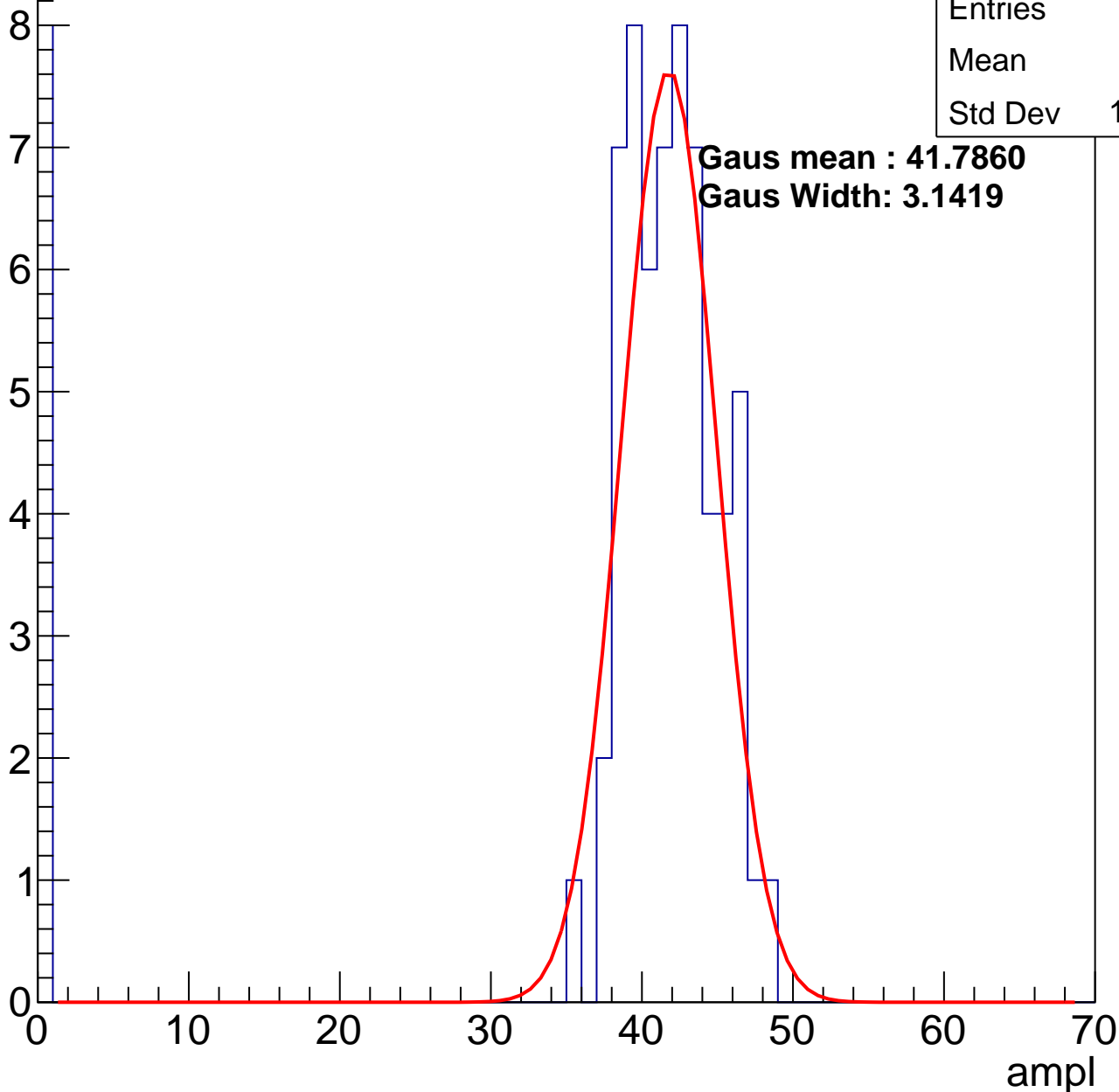
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	36.7
Std Dev	13.56

Gaus mean : 41.7860

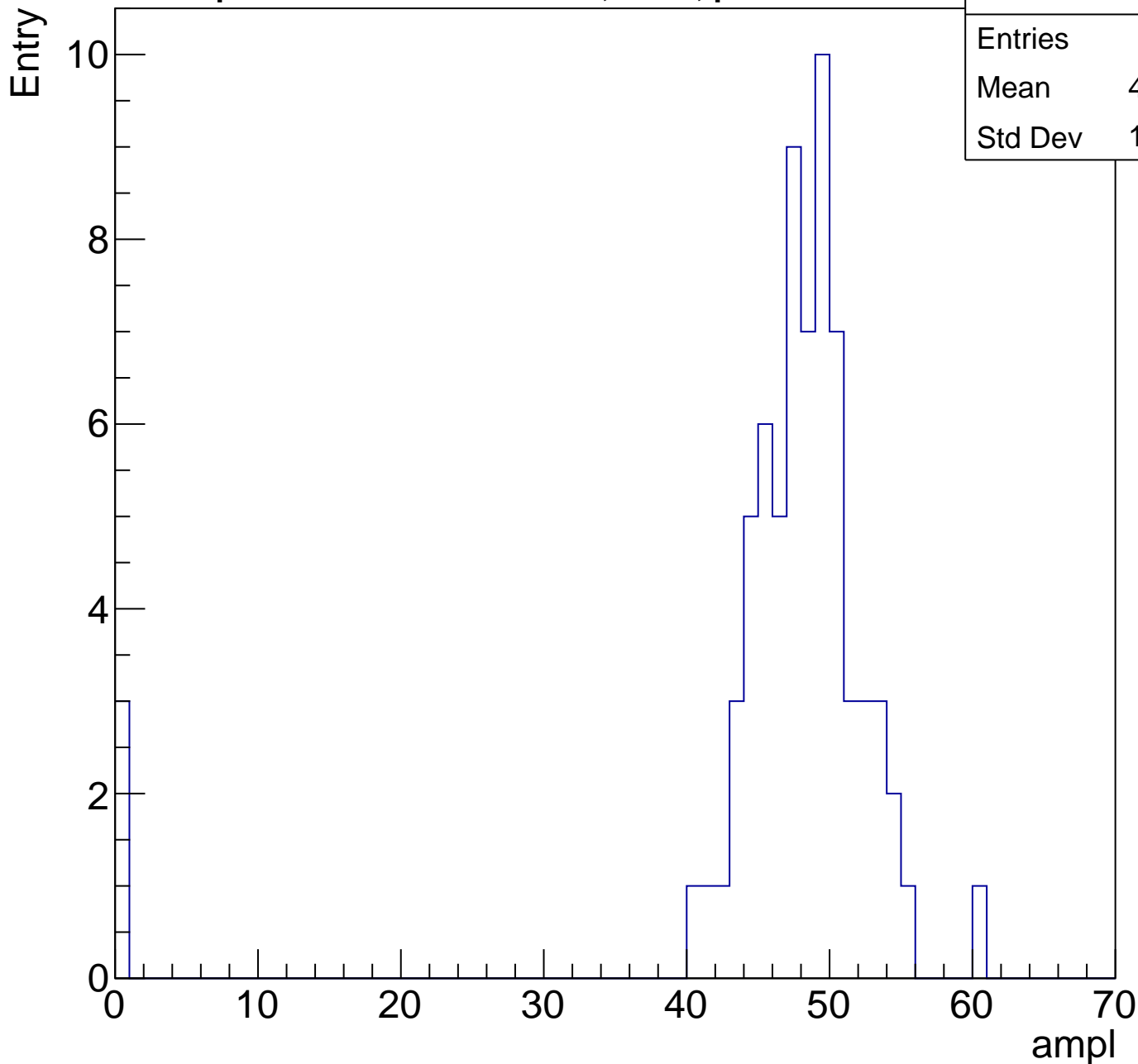
Gaus Width: 3.1419



B1L103S, U7-ch76, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	71
Mean	45.94
Std Dev	10.24

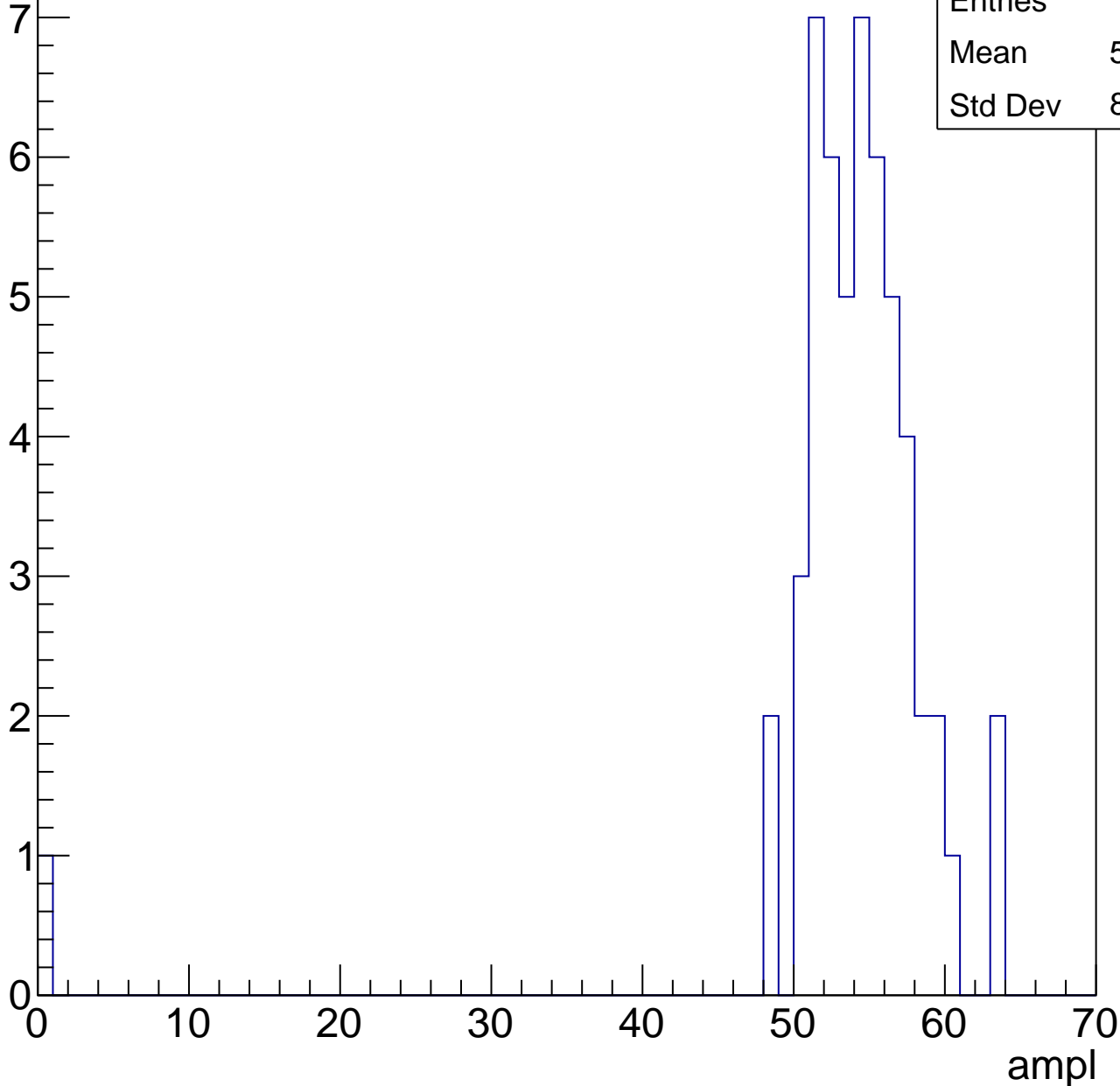


B1L103S, U7-ch76, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	53.13
Std Dev	8.045



B1L103S, U7-ch76, adc5

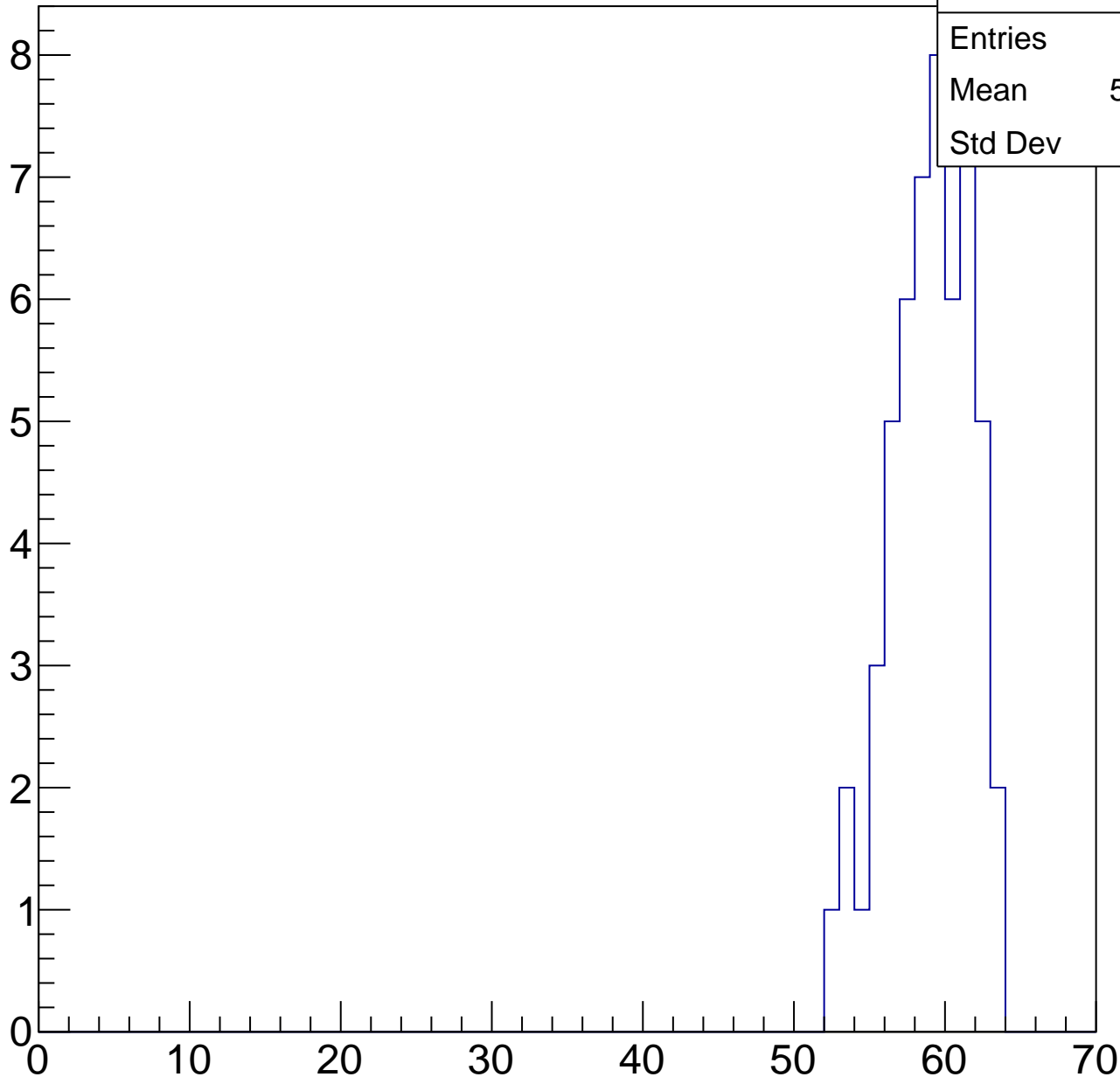
calib_packv5_041523_1651.root, FC#0, port C2

Entry

8
7
6
5
4
3
2
1
0

Entries	54
Mean	58.54
Std Dev	2.63

ampl

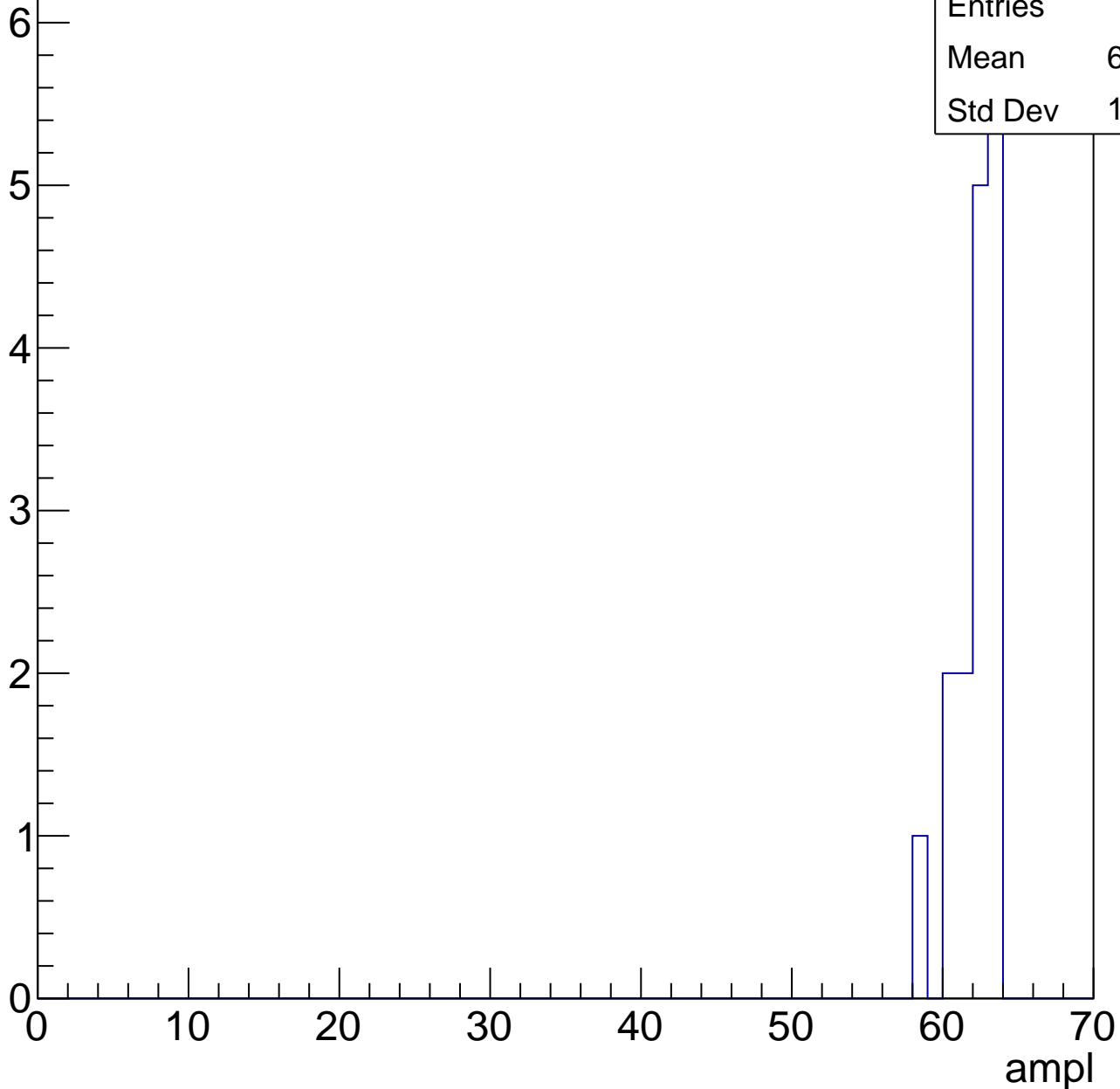


B1L103S, U7-ch76, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	16
Mean	61.75
Std Dev	1.392



B1L103S, U7-ch76, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

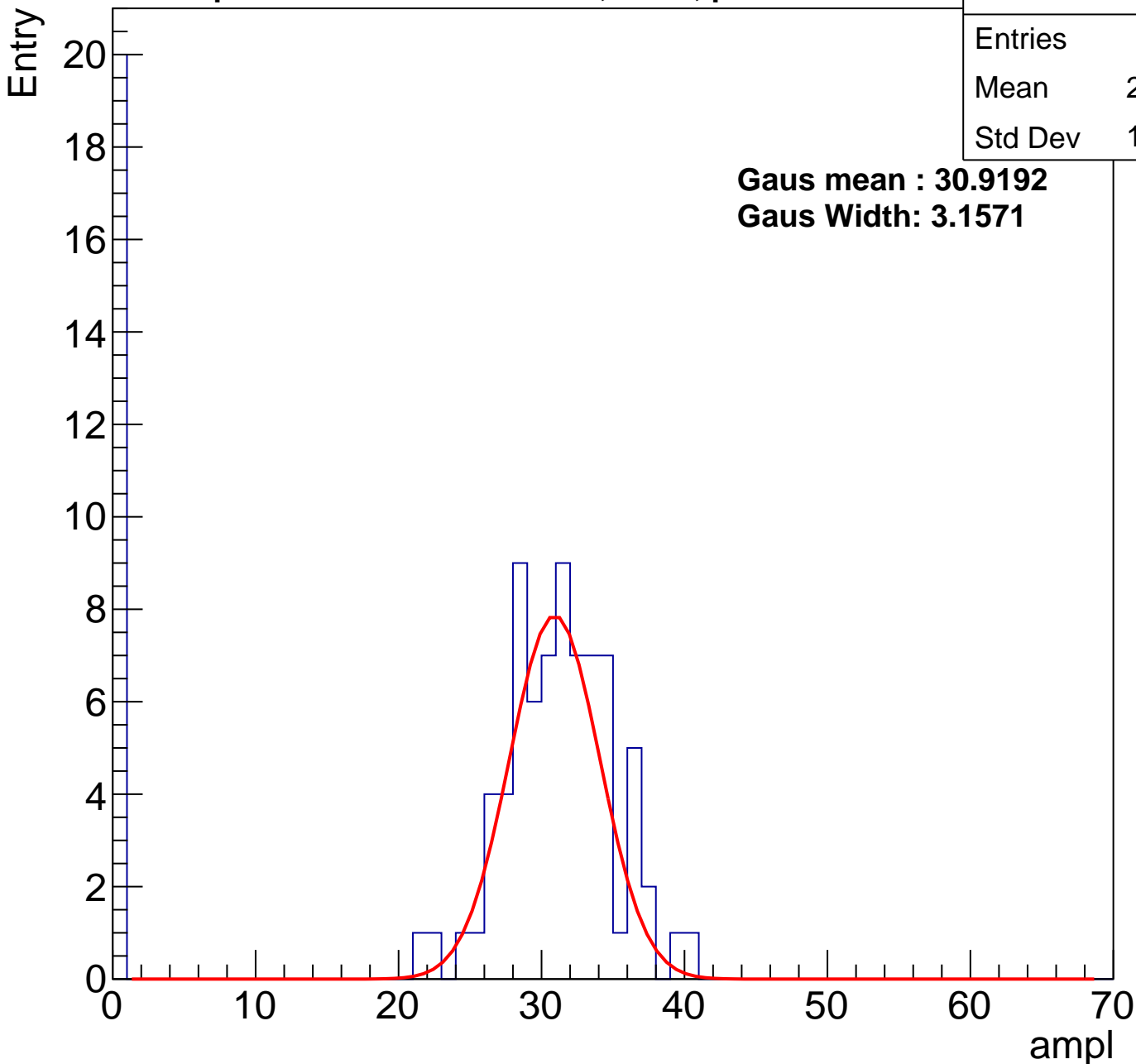
B1L103S, U7-ch77, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	94
Mean	24.26
Std Dev	13.02

Gaus mean : 30.9192

Gaus Width: 3.1571



B1L103S, U7-ch77, adc1

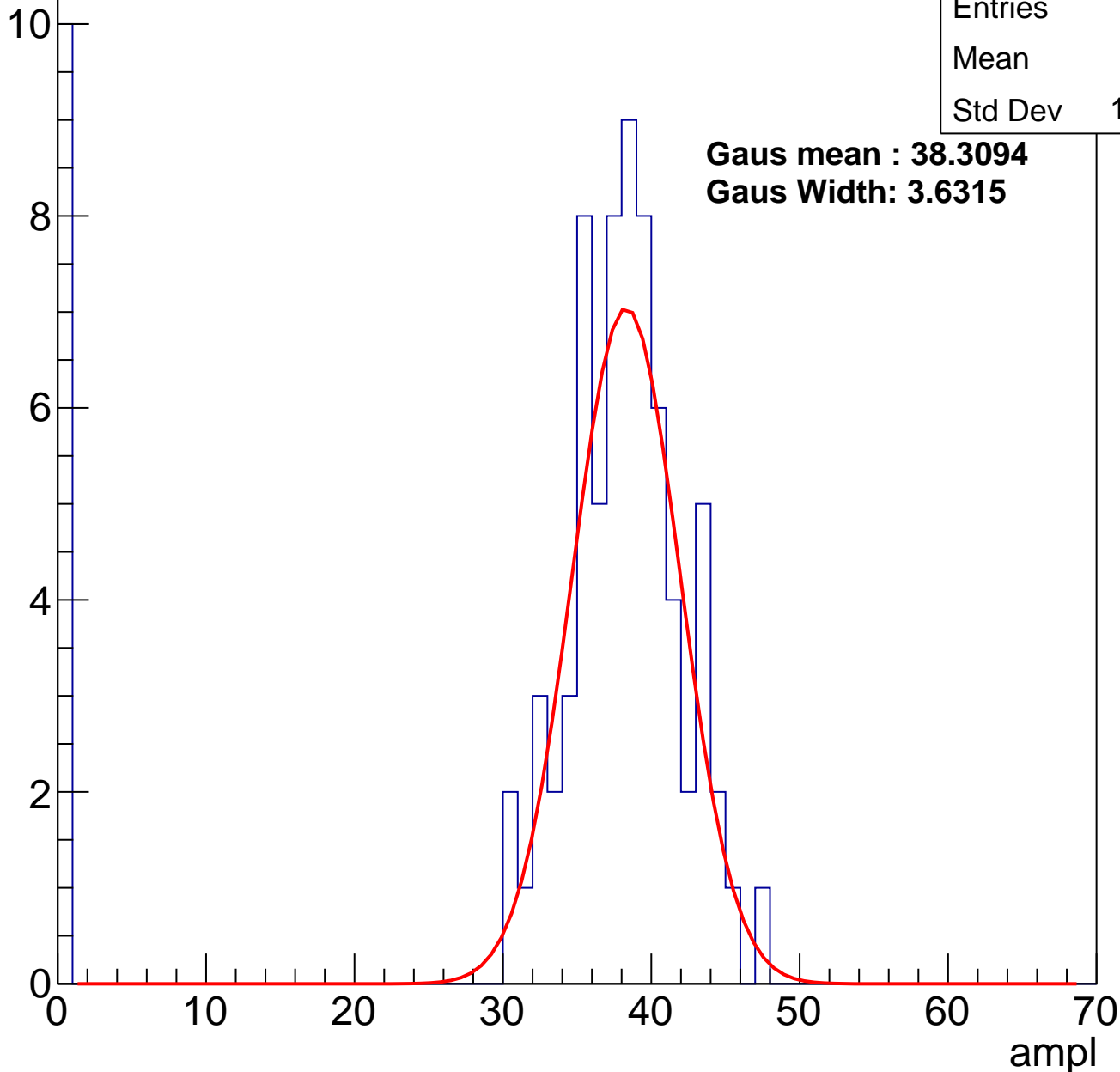
calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	33.1
Std Dev	12.96

Gaus mean : 38.3094

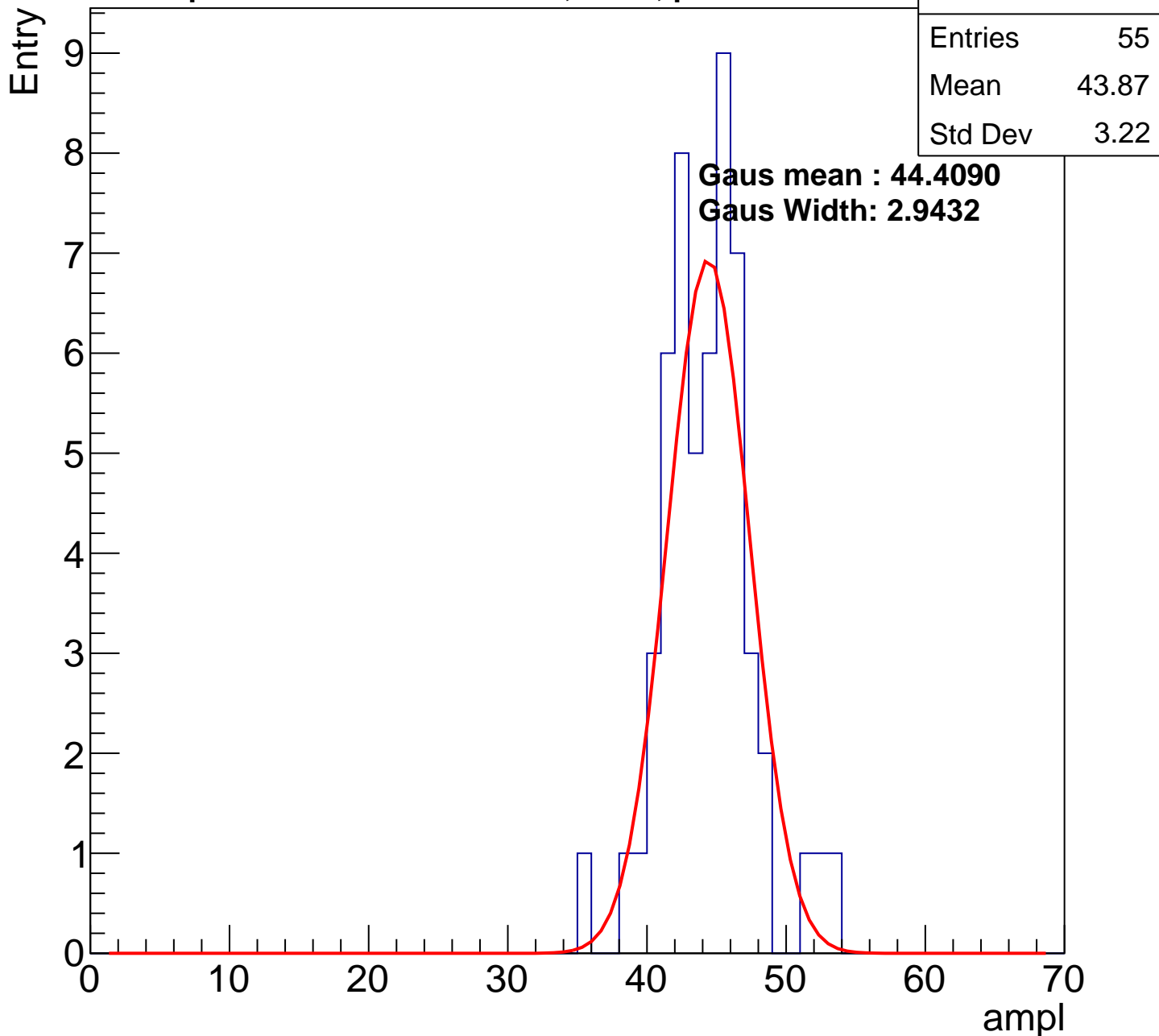
Gaus Width: 3.6315

Entry



B1L103S, U7-ch77, adc2

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U7-ch77, adc3

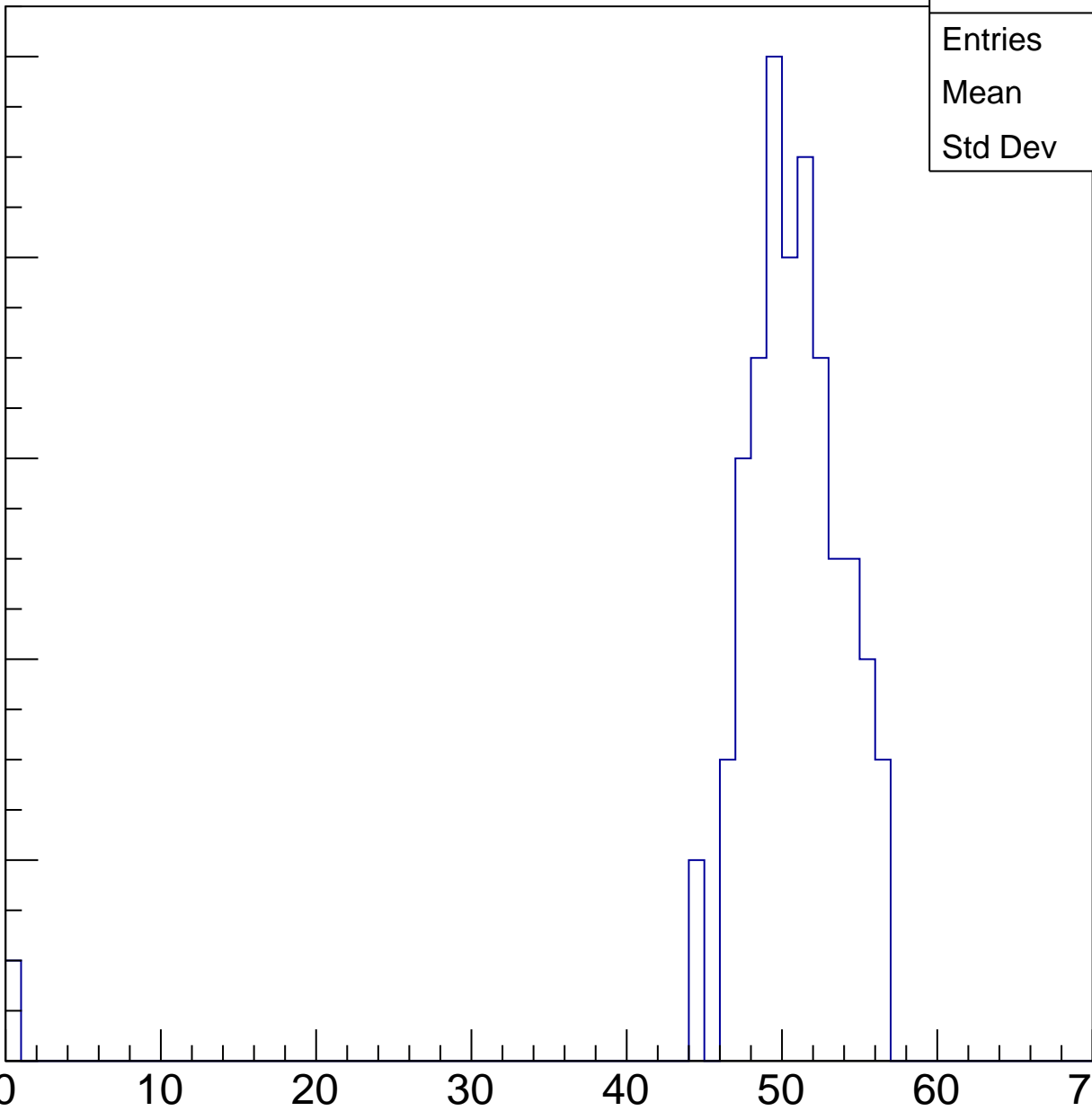
calib_packv5_041523_1651.root, FC#0, port C2

Entries	70
Mean	49.71
Std Dev	6.629

Entry

10
8
6
4
2
0

ampl

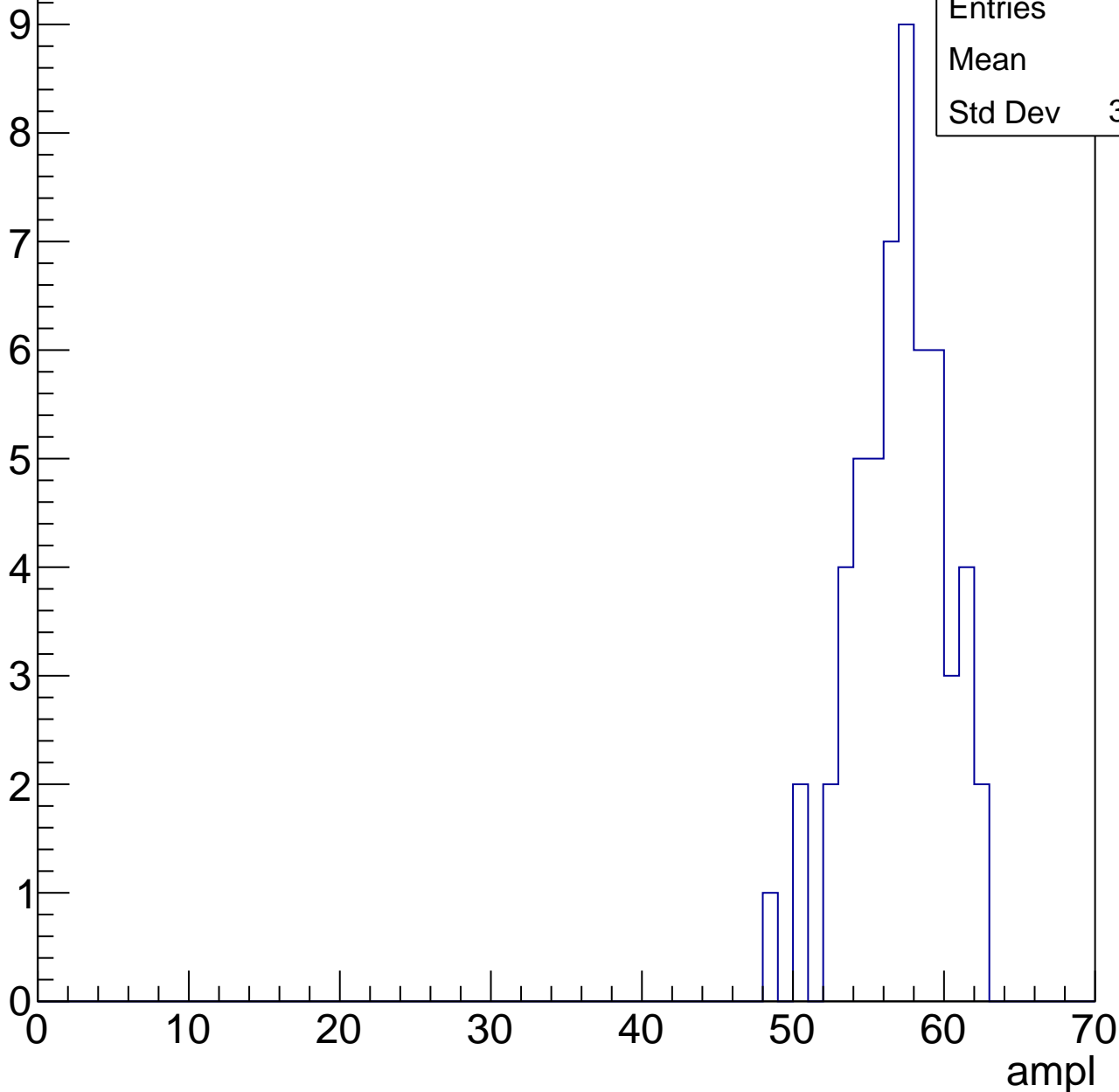


B1L103S, U7-ch77, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	56.5
Std Dev	3.053

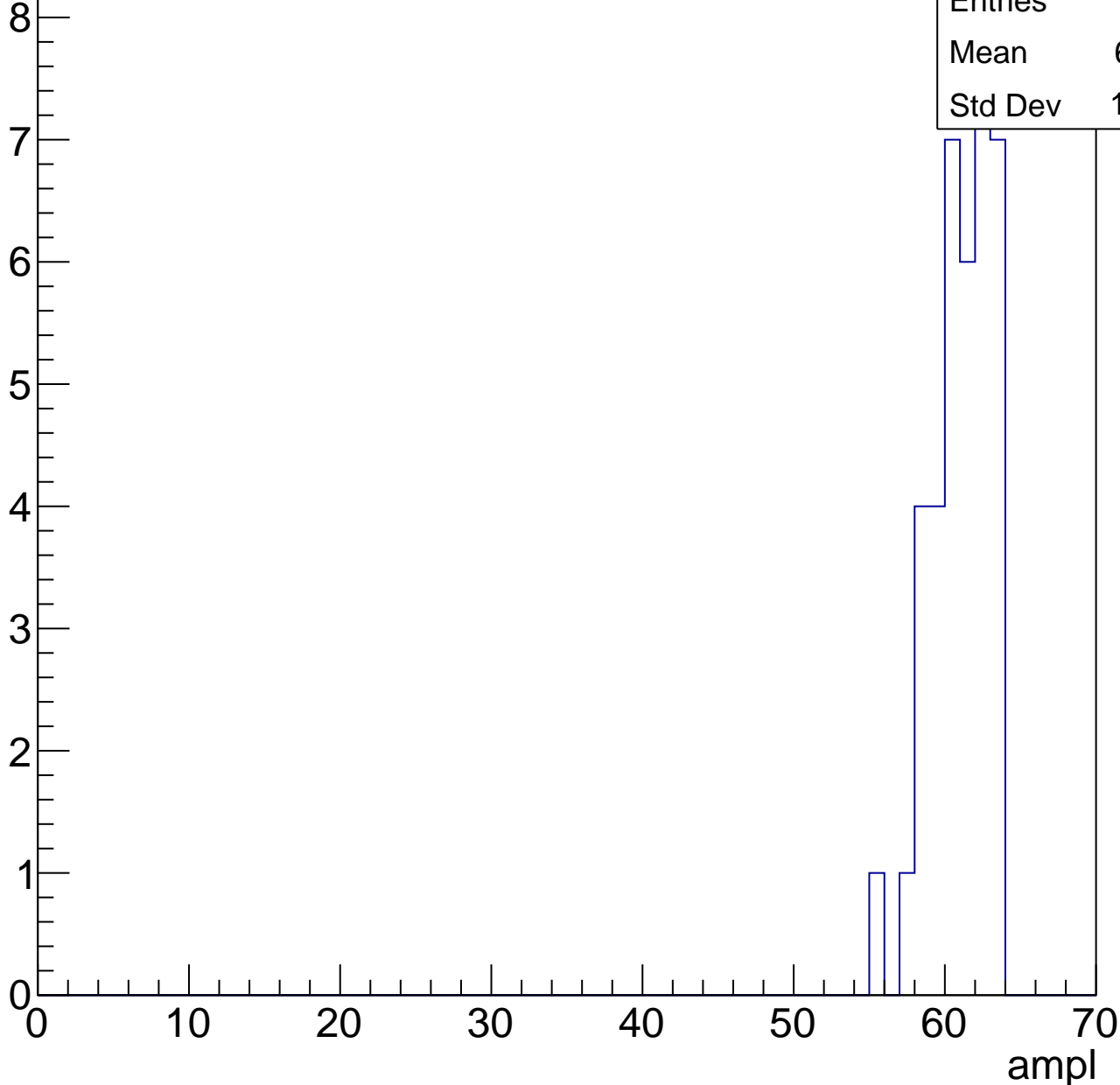


B1L103S, U7-ch77, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

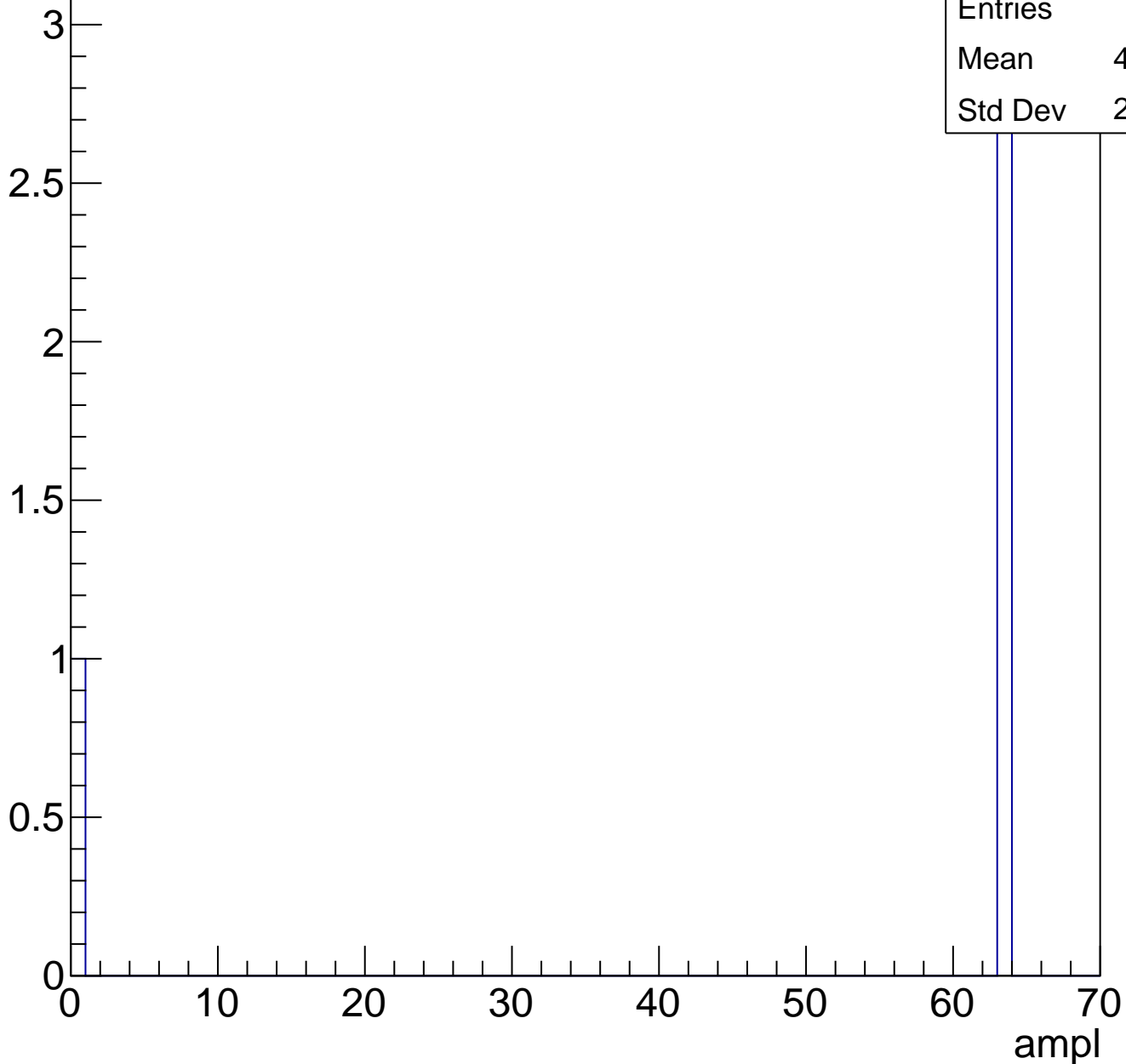
Entries	38
Mean	60.61
Std Dev	1.927



B1L103S, U7-ch77, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch77, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

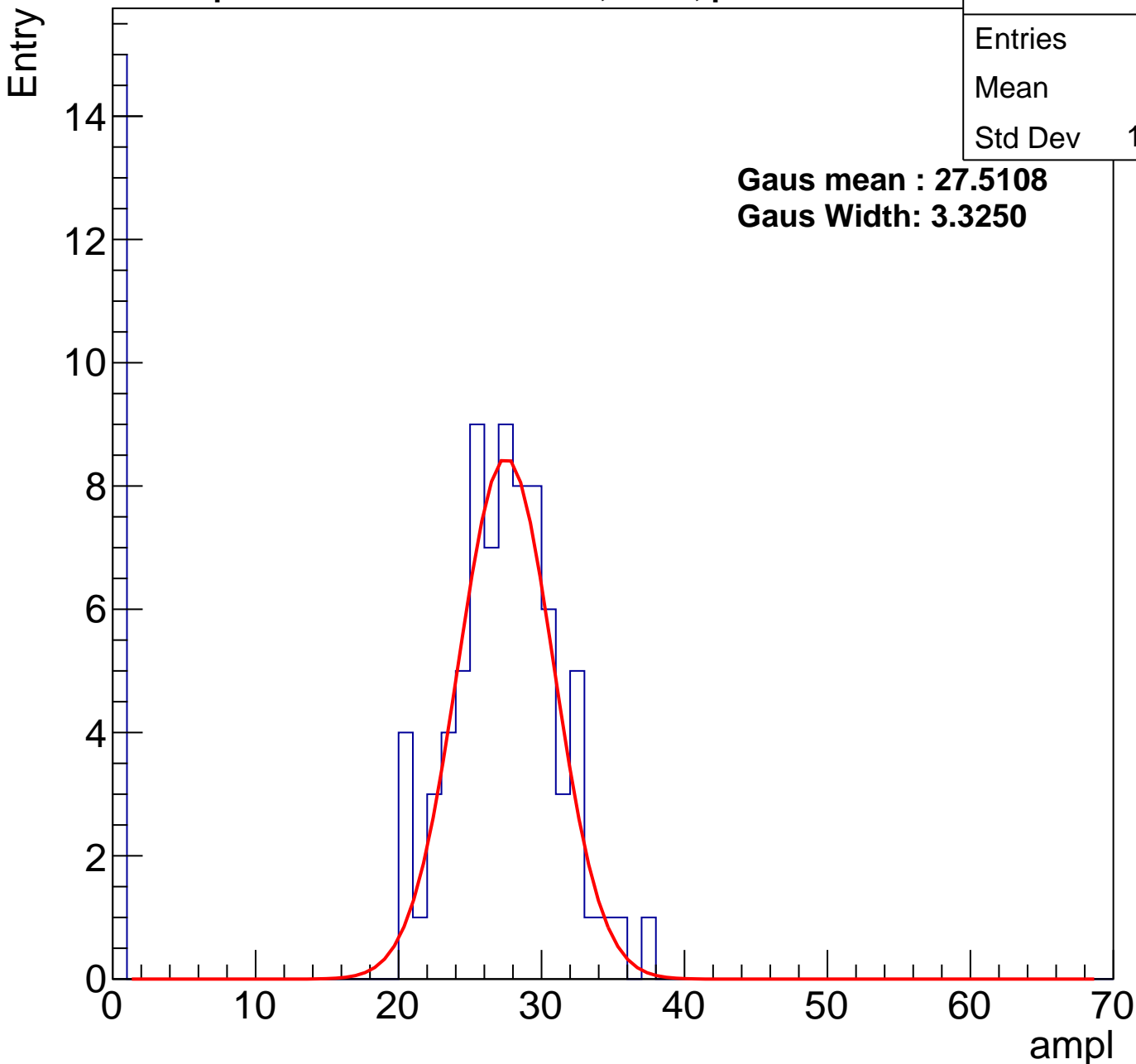
B1L103S, U7-ch78, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	91
Mean	22.6
Std Dev	10.56

Gaus mean : 27.5108

Gaus Width: 3.3250



B1L103S, U7-ch78, adc1

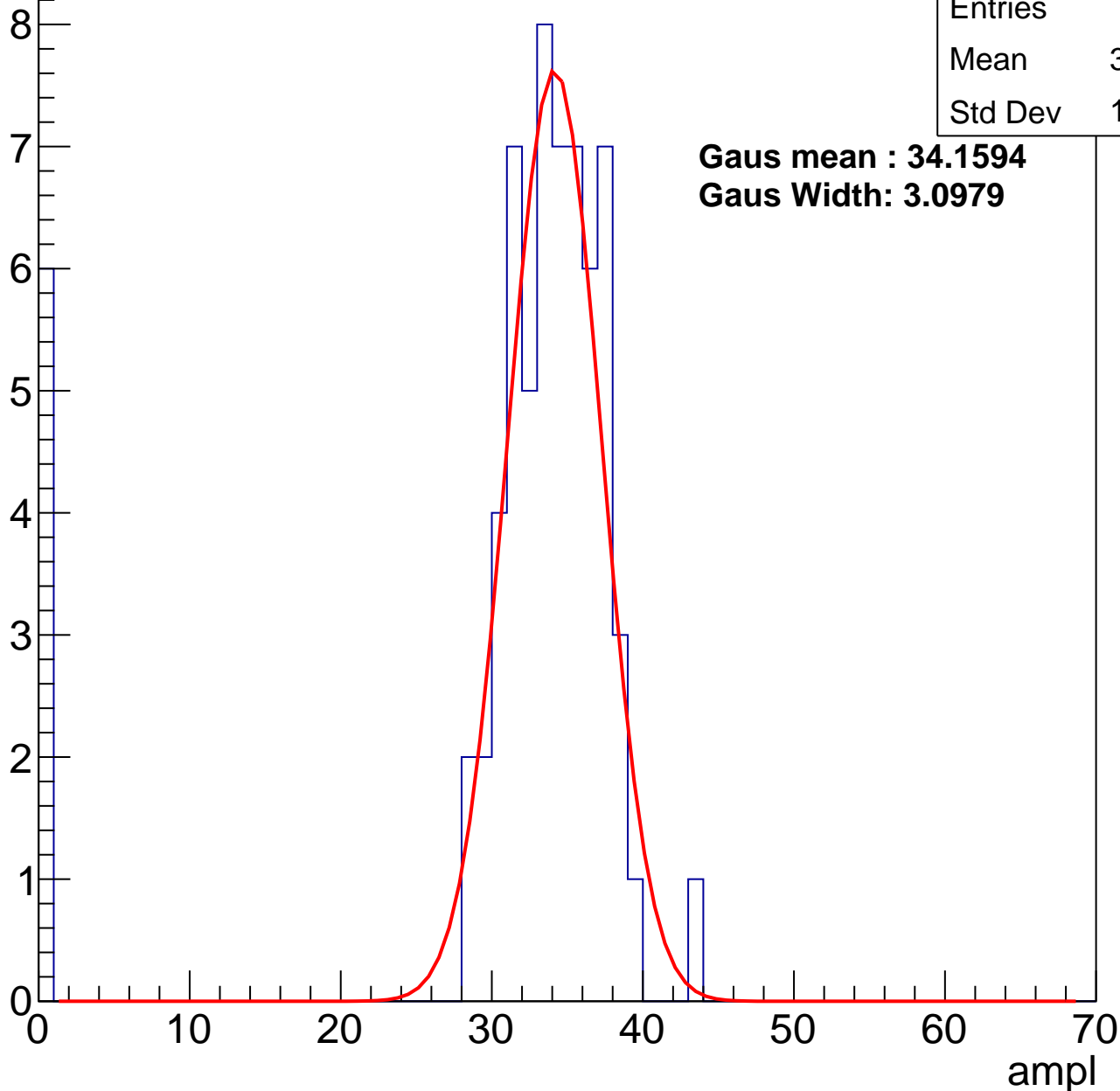
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	30.74
Std Dev	10.12

Gaus mean : 34.1594

Gaus Width: 3.0979



B1L103S, U7-ch78, adc2

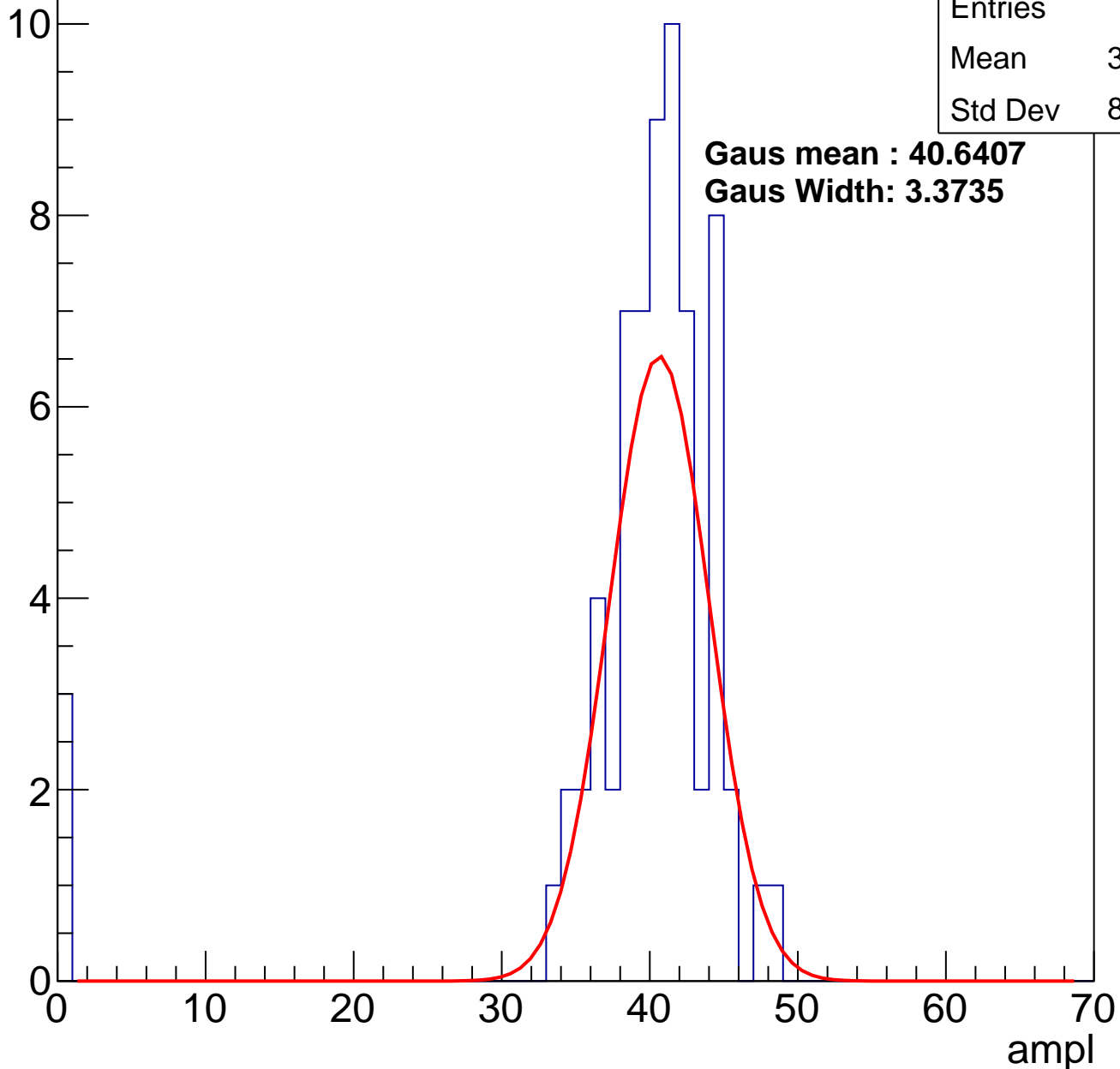
calib_packv5_041523_1651.root, FC#0, port C2

Entries	68
Mean	38.46
Std Dev	8.806

Gaus mean : 40.6407

Gaus Width: 3.3735

Entry

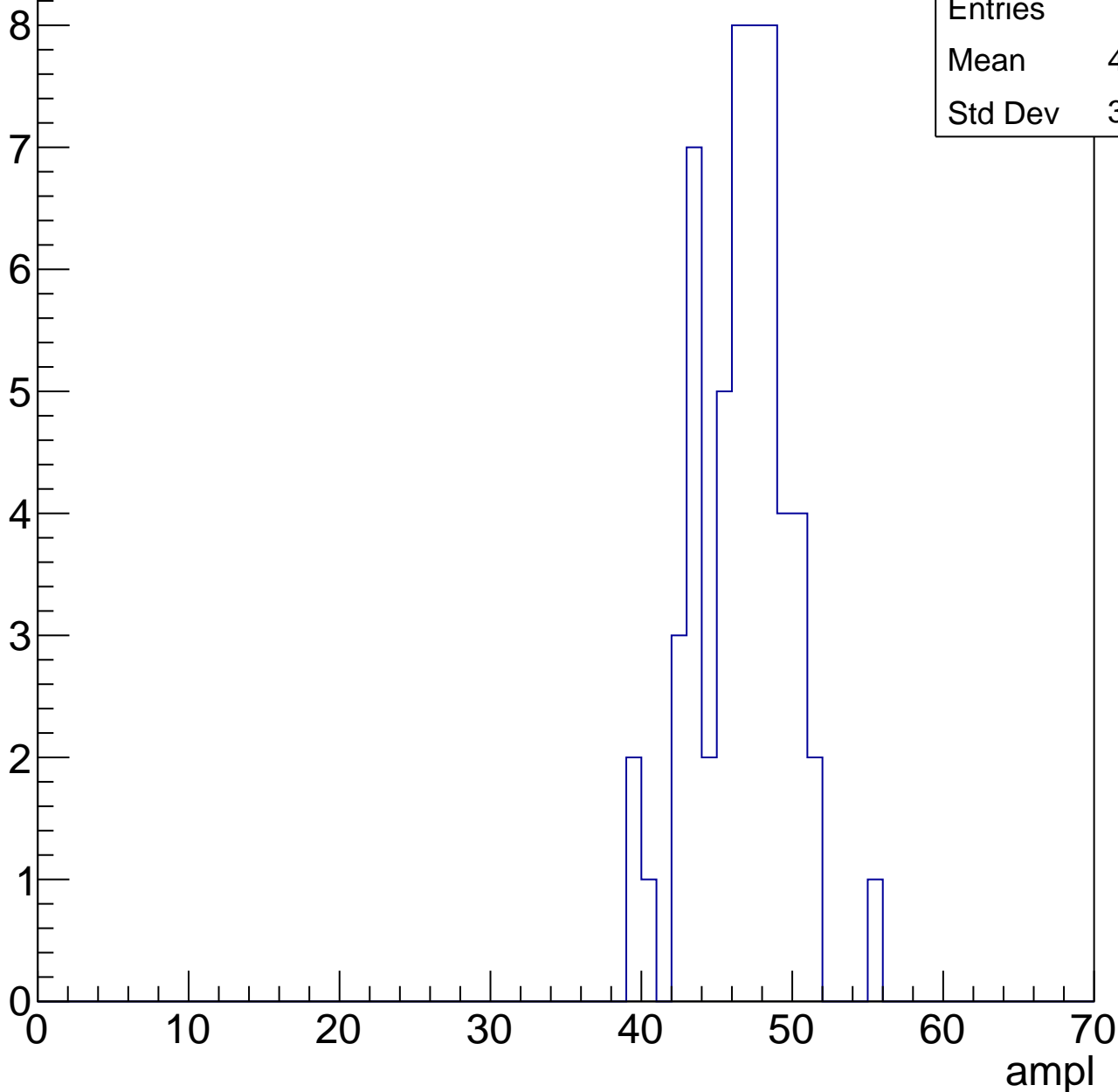


B1L103S, U7-ch78, adc3

calib_packv5_041523_1651.root, FC#0, port C2

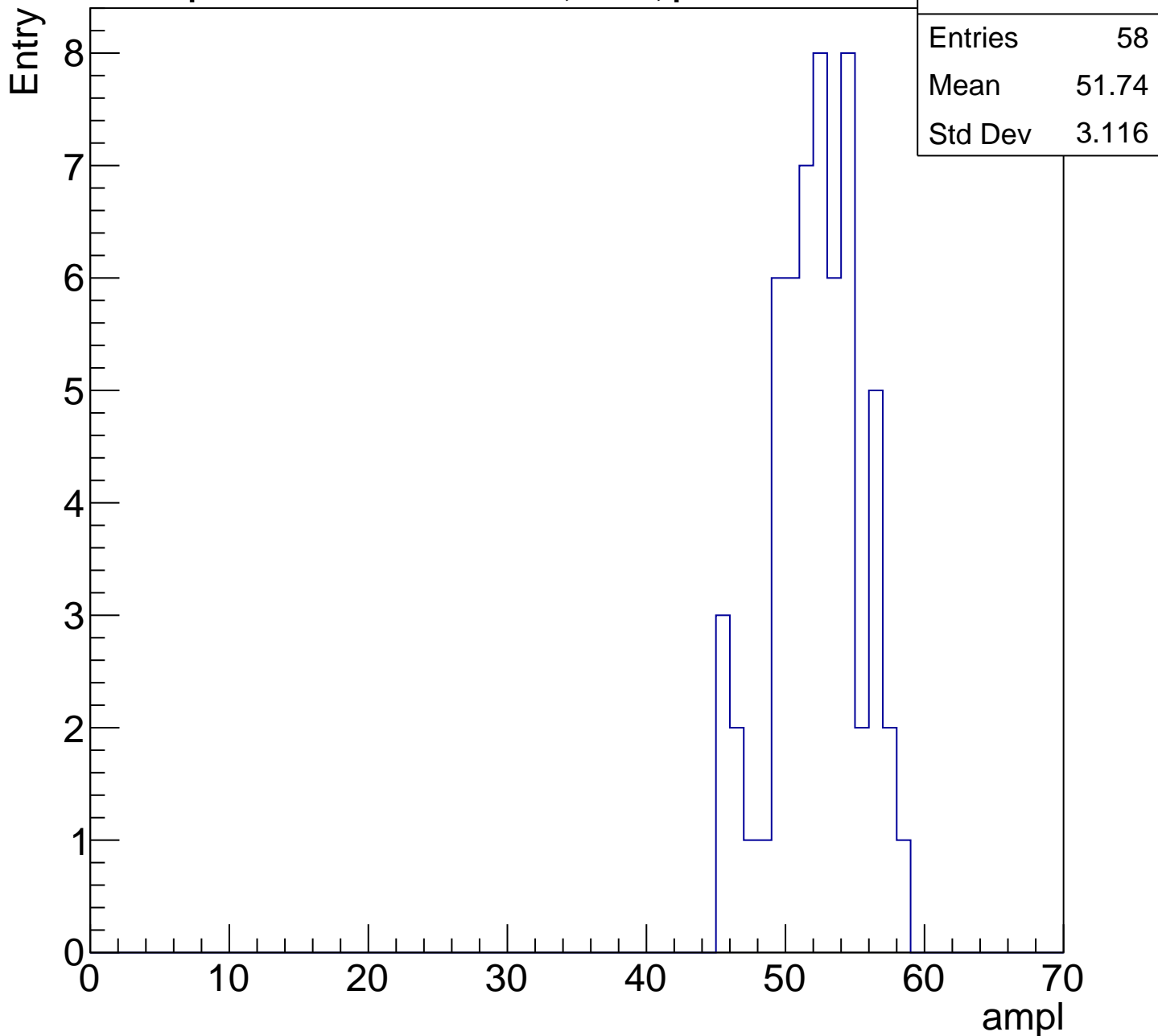
Entry

Entries	55
Mean	46.16
Std Dev	3.097



B1L103S, U7-ch78, adc4

calib_packv5_041523_1651.root, FC#0, port C2

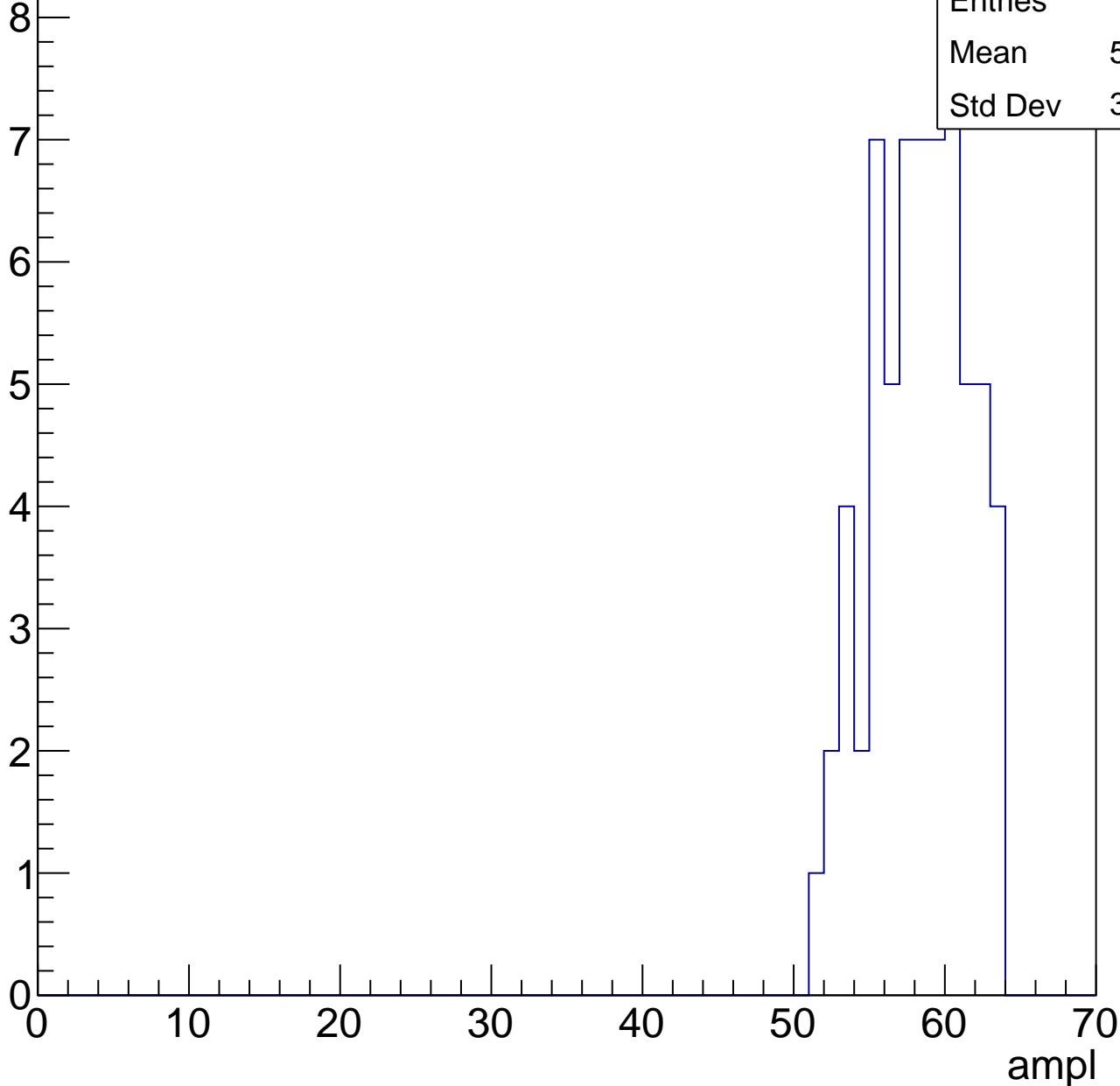


B1L103S, U7-ch78, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	57.89
Std Dev	3.078

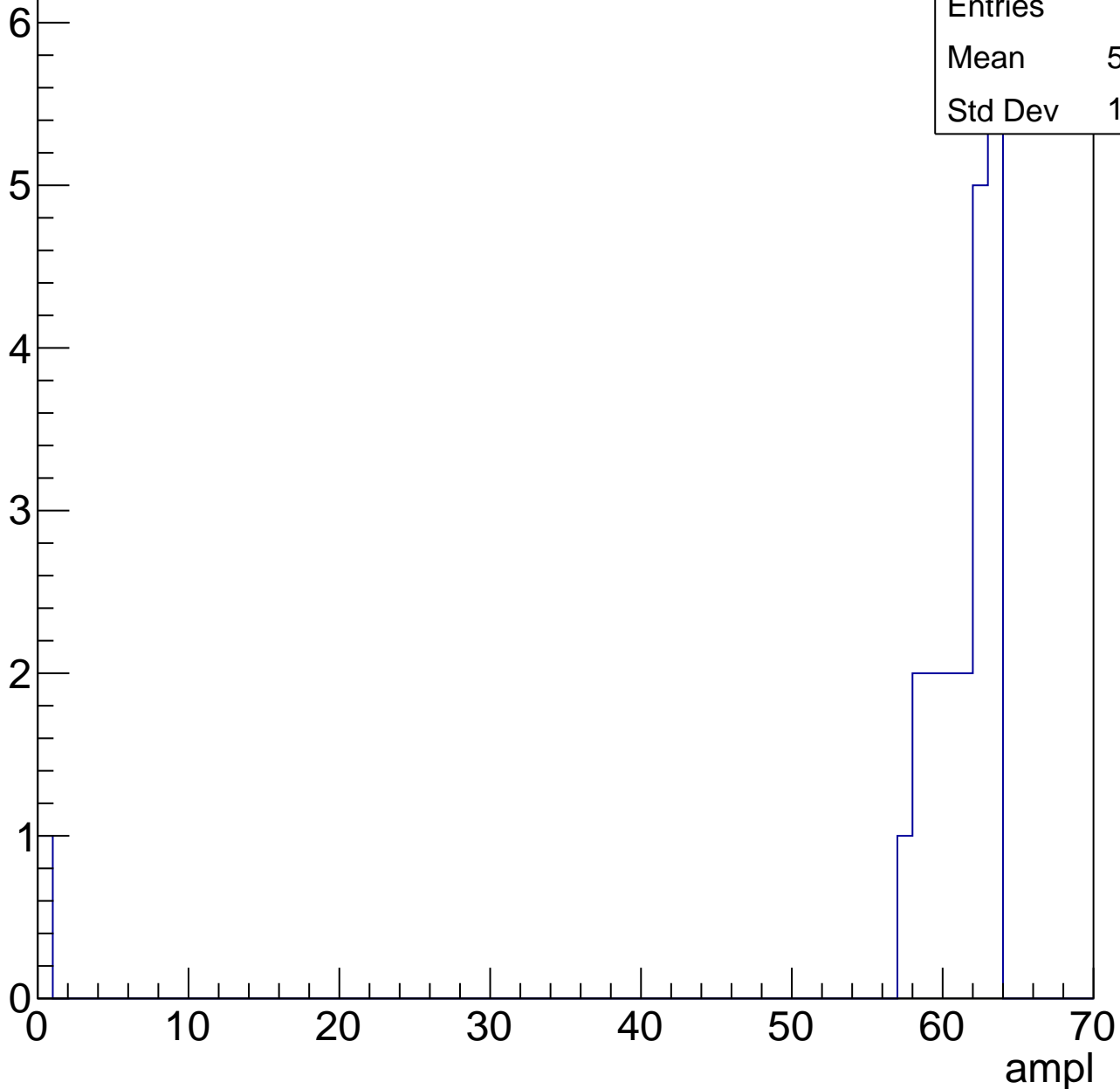


B1L103S, U7-ch78, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	21
Mean	58.14
Std Dev	13.13

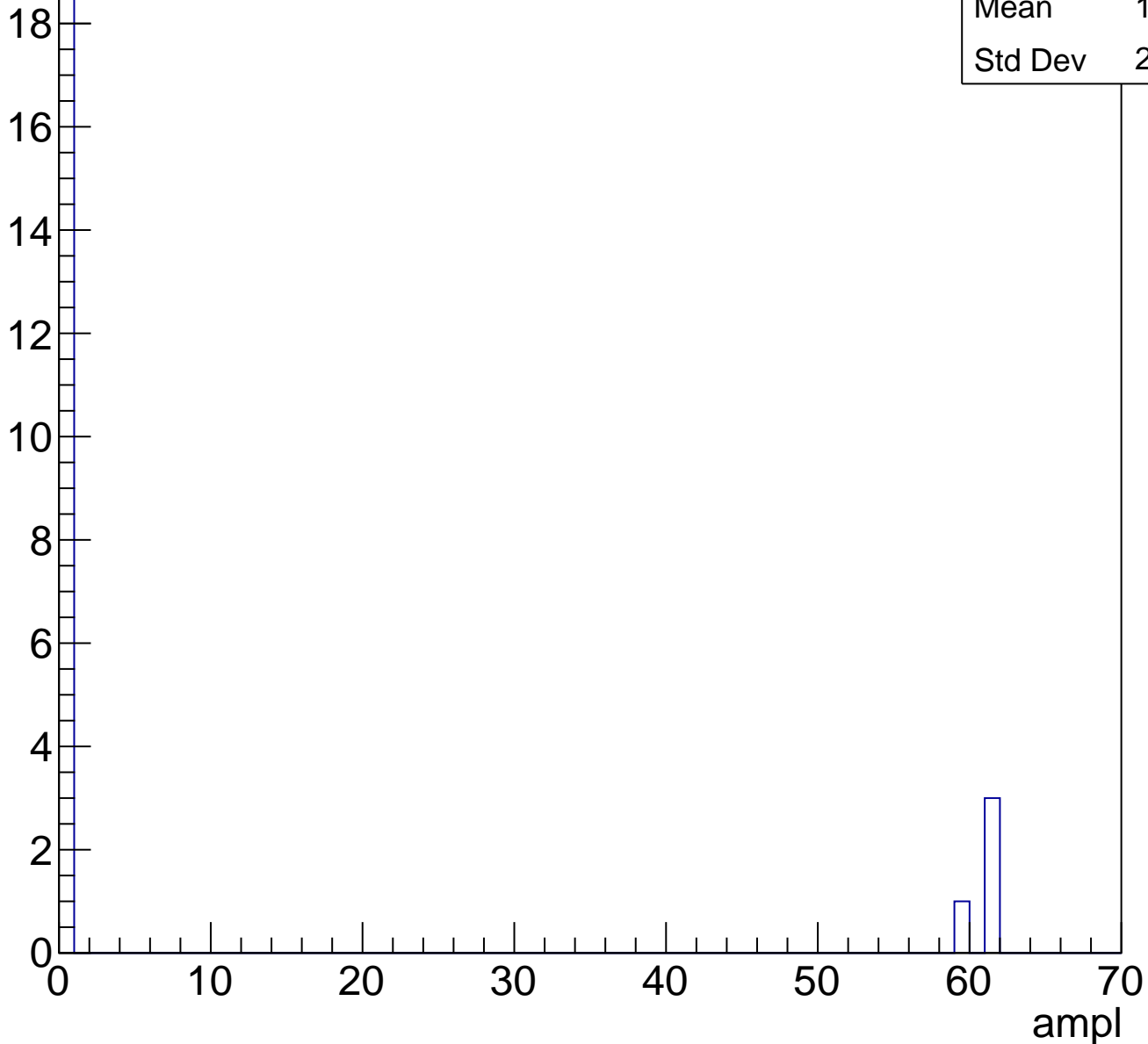


B1L103S, U7-ch78, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	23
Mean	10.52
Std Dev	22.93

Entry



B1L103S, U7-ch79, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	23.08
Std Dev	11.87

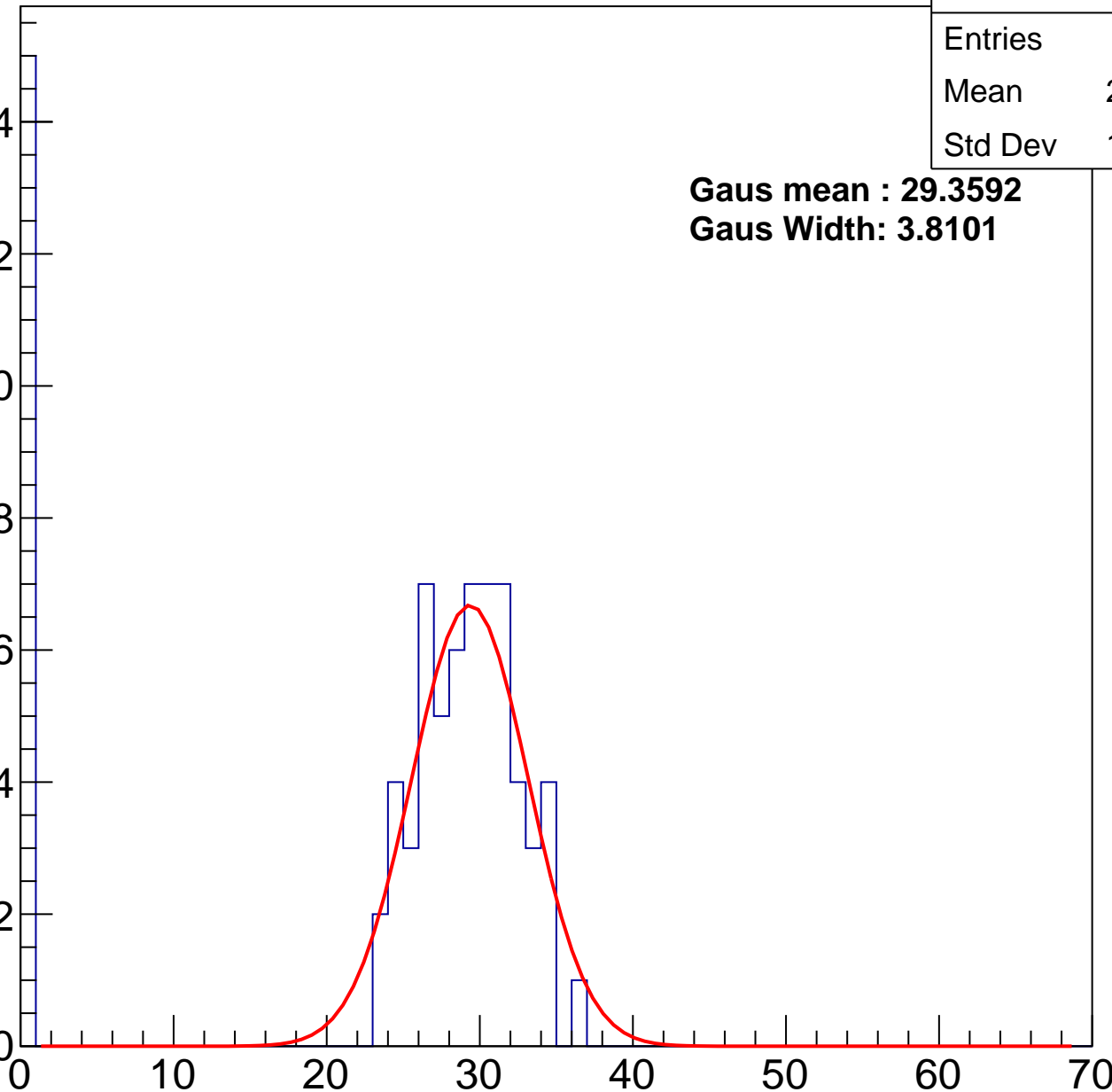
Gaus mean : 29.3592

Gaus Width: 3.8101

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch79, adc1

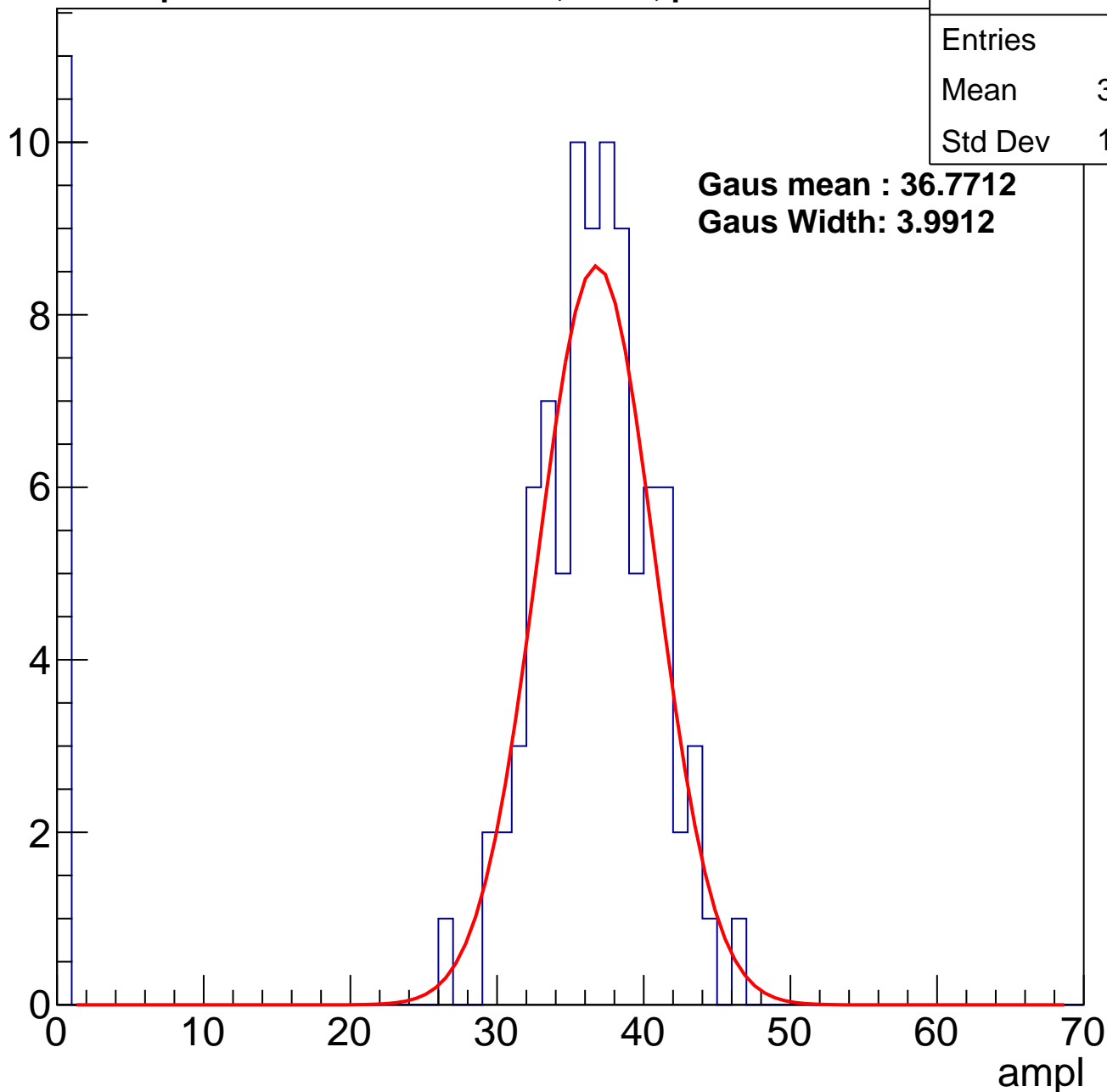
calib_packv5_041523_1651.root, FC#0, port C2

Entries	99
Mean	32.32
Std Dev	11.96

Gaus mean : 36.7712

Gaus Width: 3.9912

Entry



B1L103S, U7-ch79, adc2

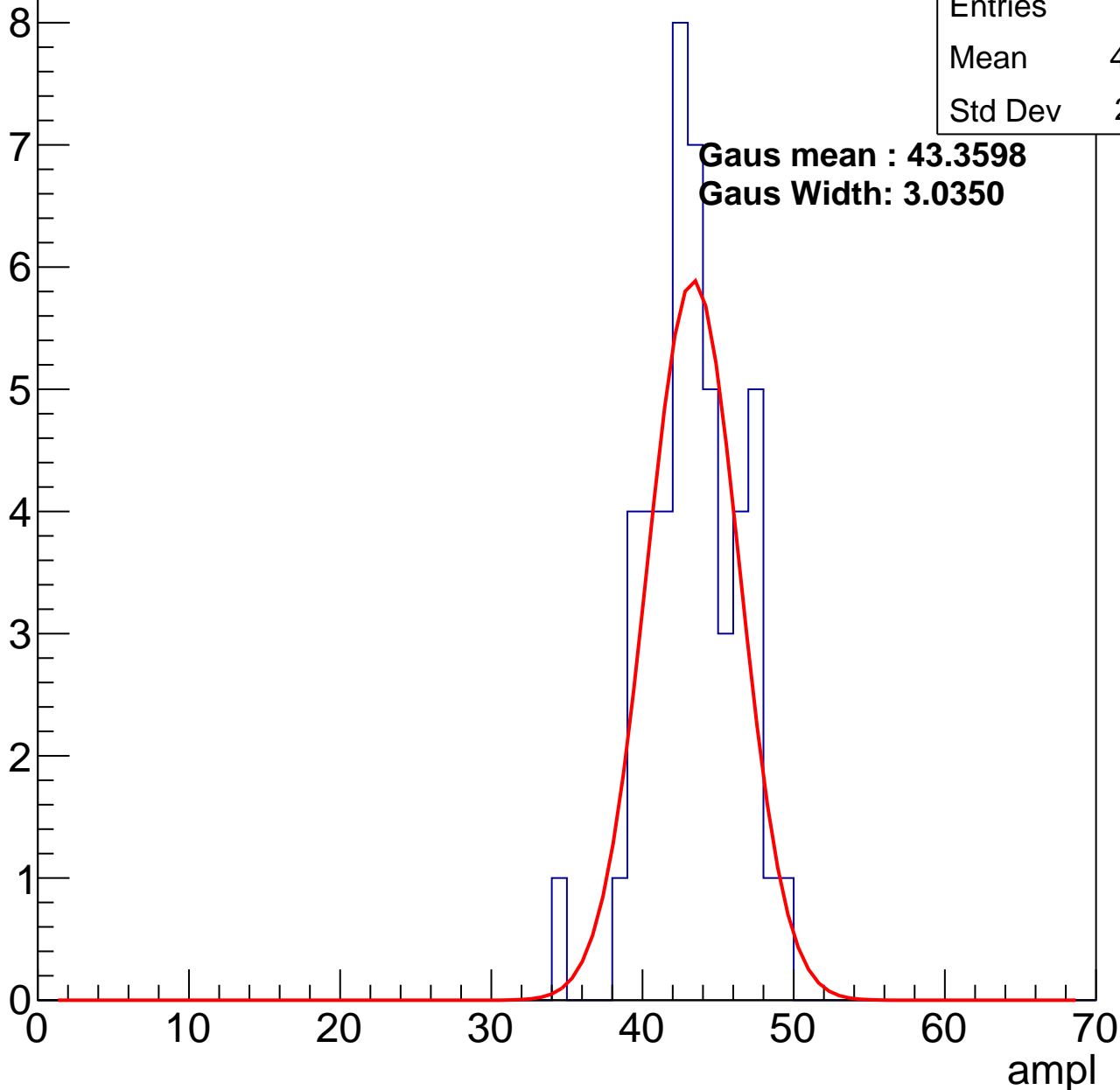
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	48
Mean	42.92
Std Dev	2.971

Gaus mean : 43.3598

Gaus Width: 3.0350

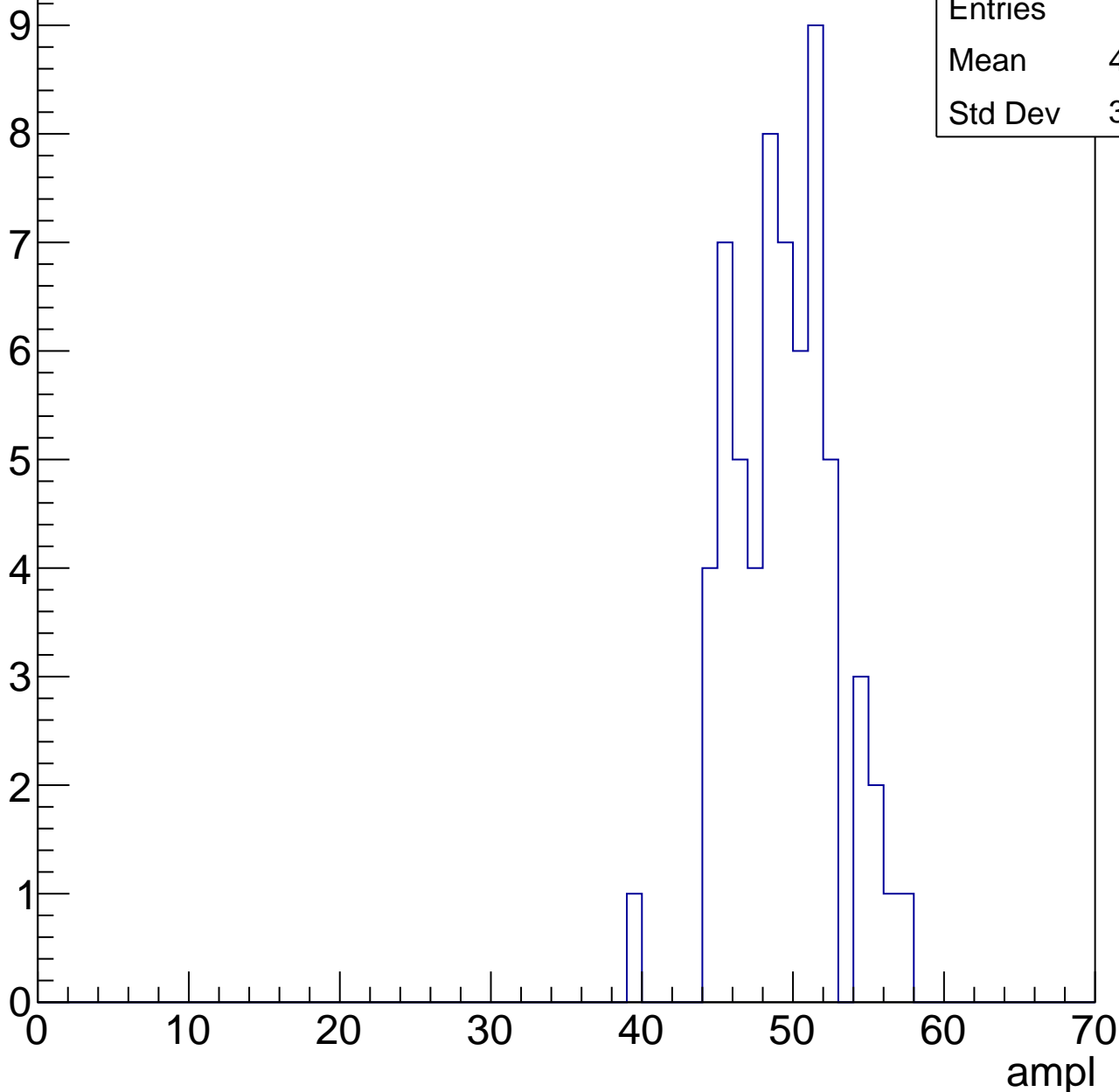


B1L103S, U7-ch79, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	48.87
Std Dev	3.397



B1L103S, U7-ch79, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	69
Mean	55.16
Std Dev	3.433

Entry

10

8

6

4

2

0

0

10

20

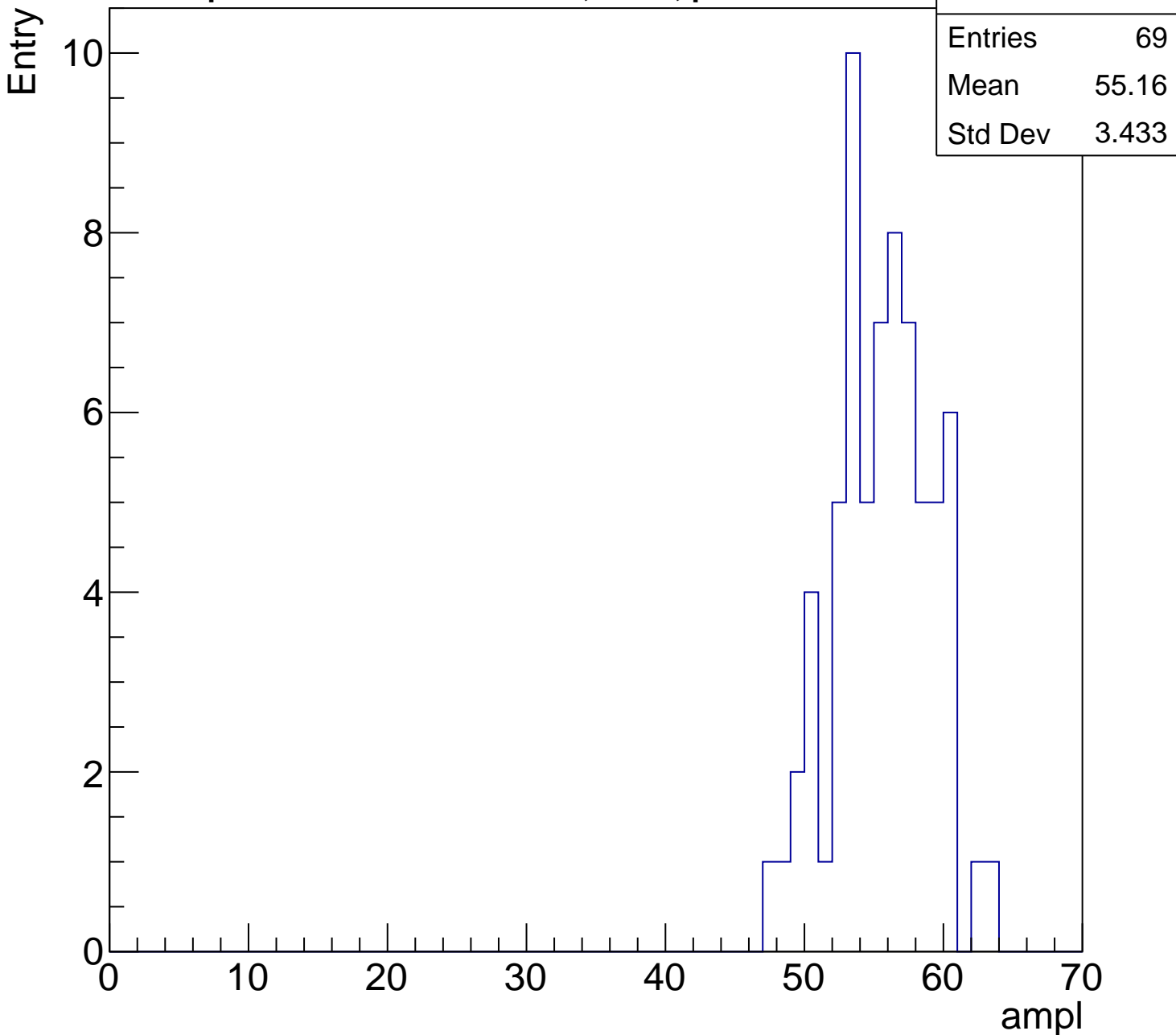
30

40

50

60

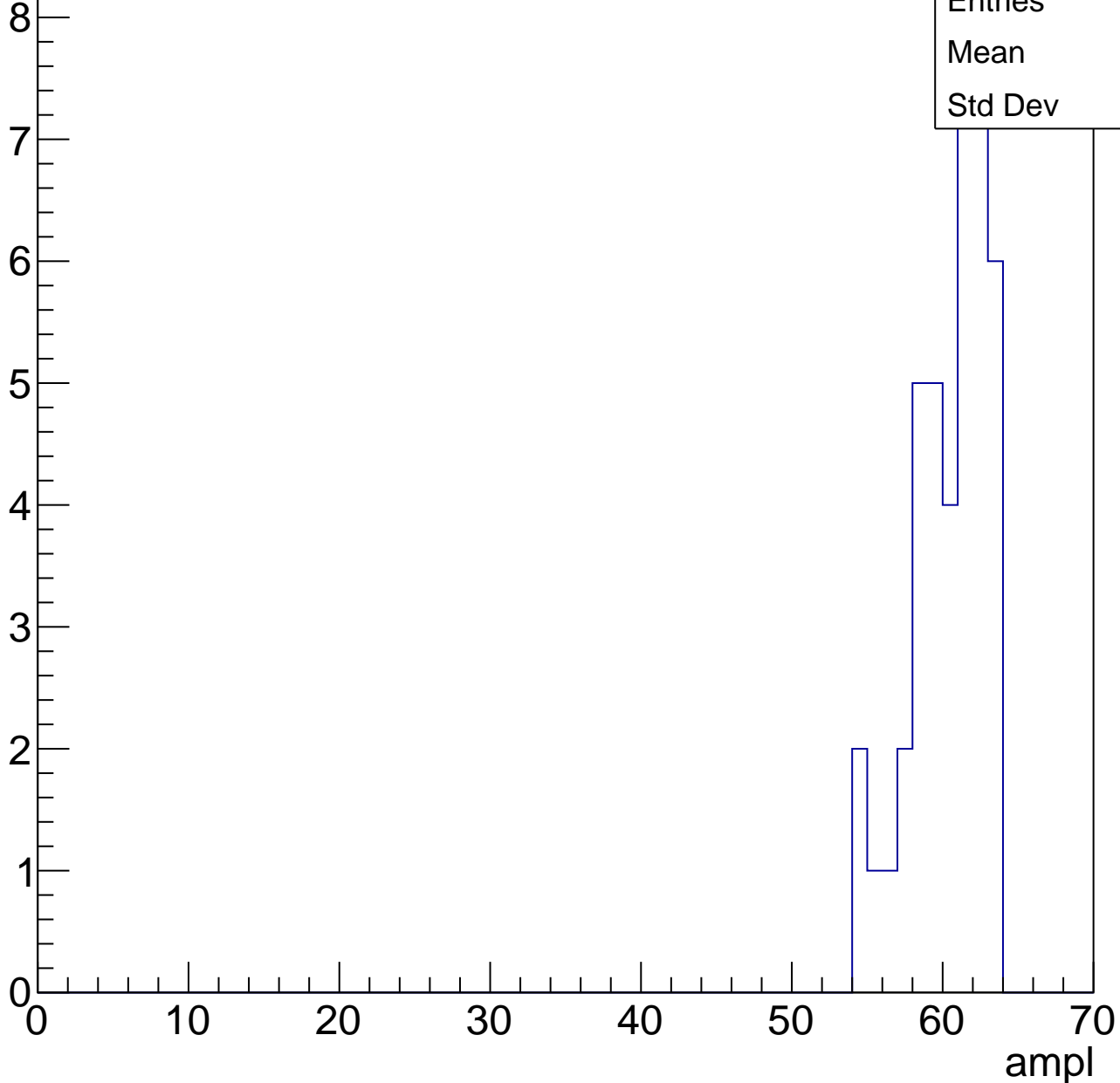
ampl



B1L103S, U7-ch79, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

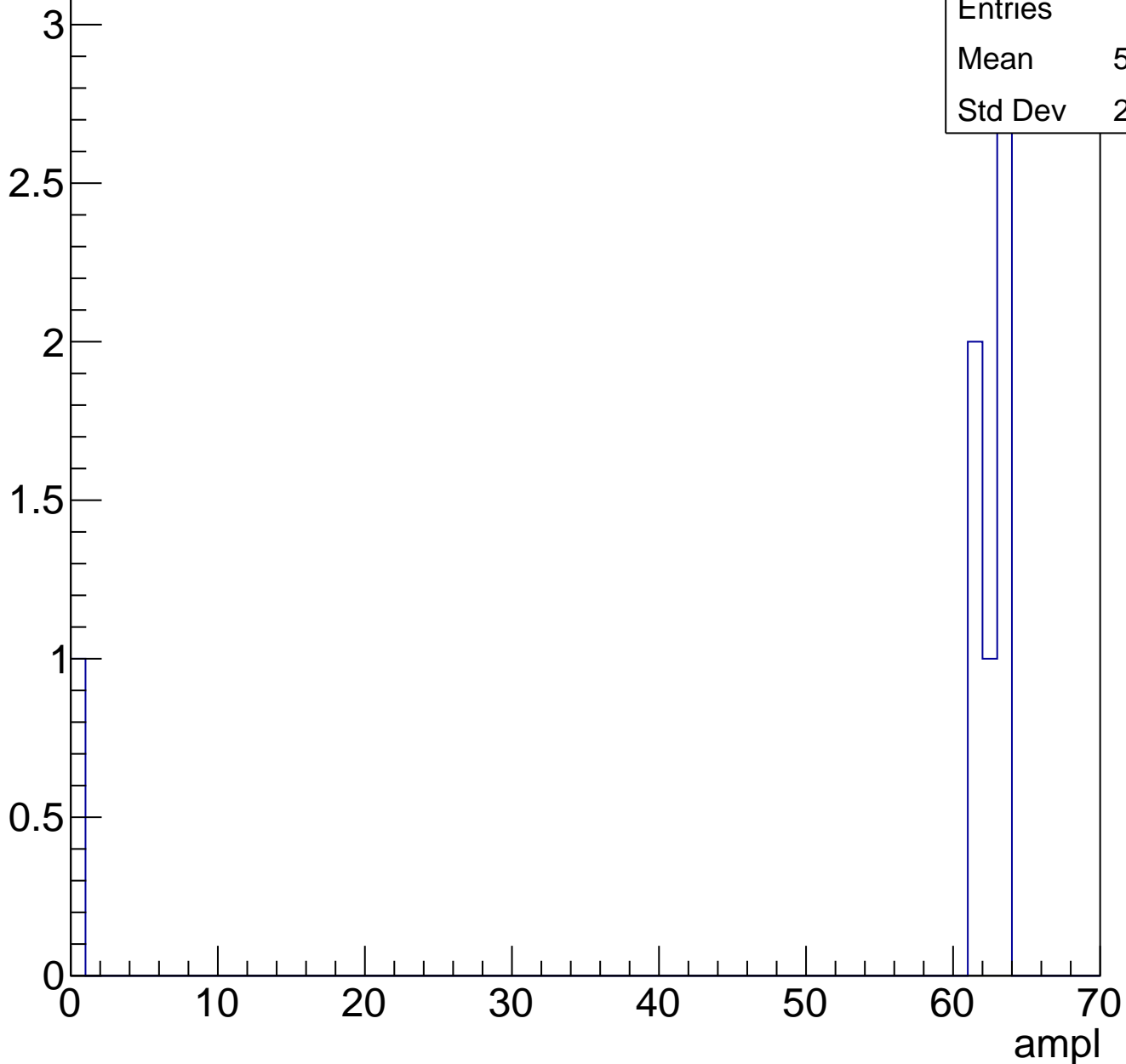


Entries	42
Mean	60
Std Dev	2.44

B1L103S, U7-ch79, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch79, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U7-ch80, adc0

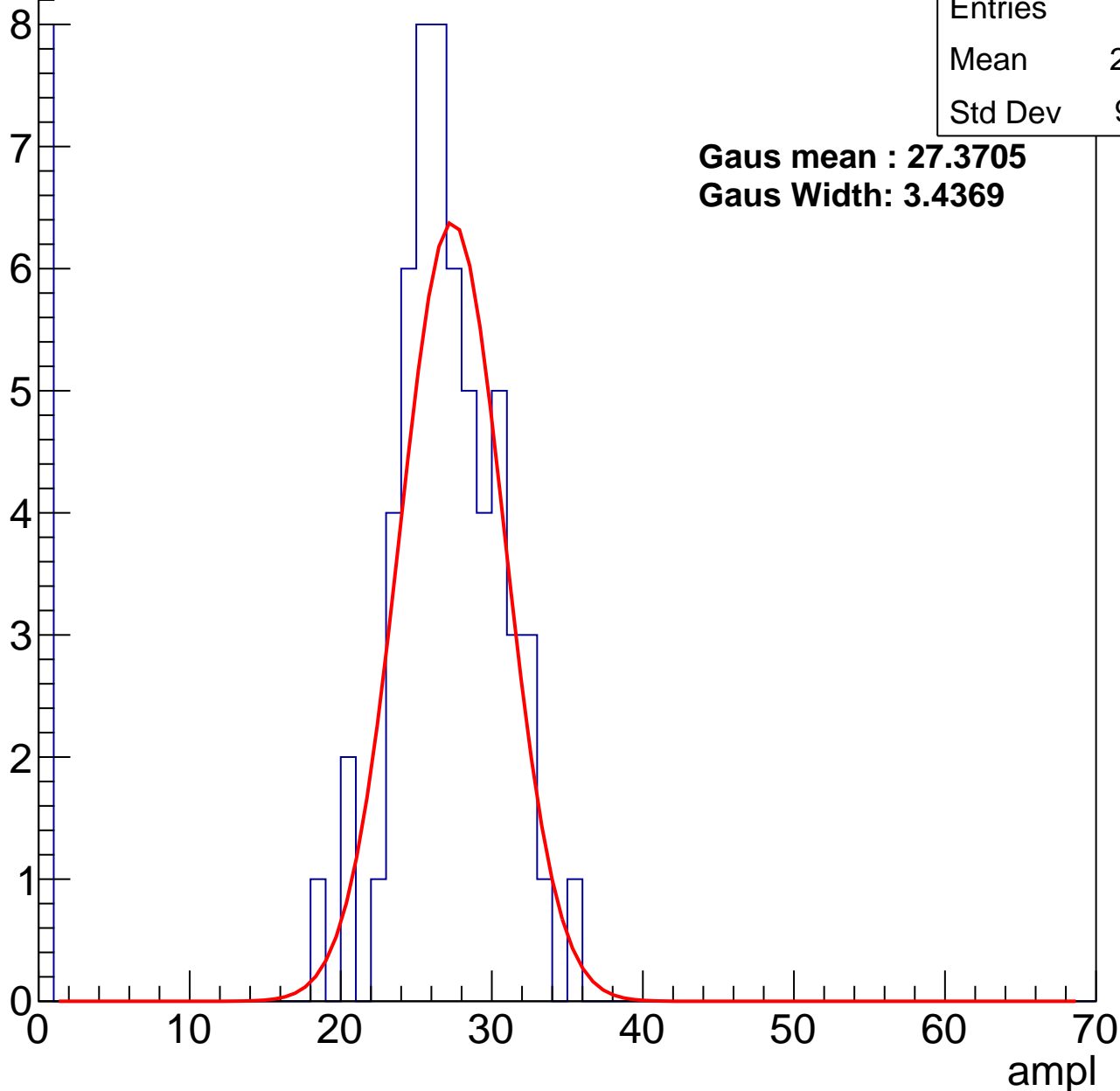
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	23.47
Std Dev	9.261

Gaus mean : 27.3705

Gaus Width: 3.4369



B1L103S, U7-ch80, adc1

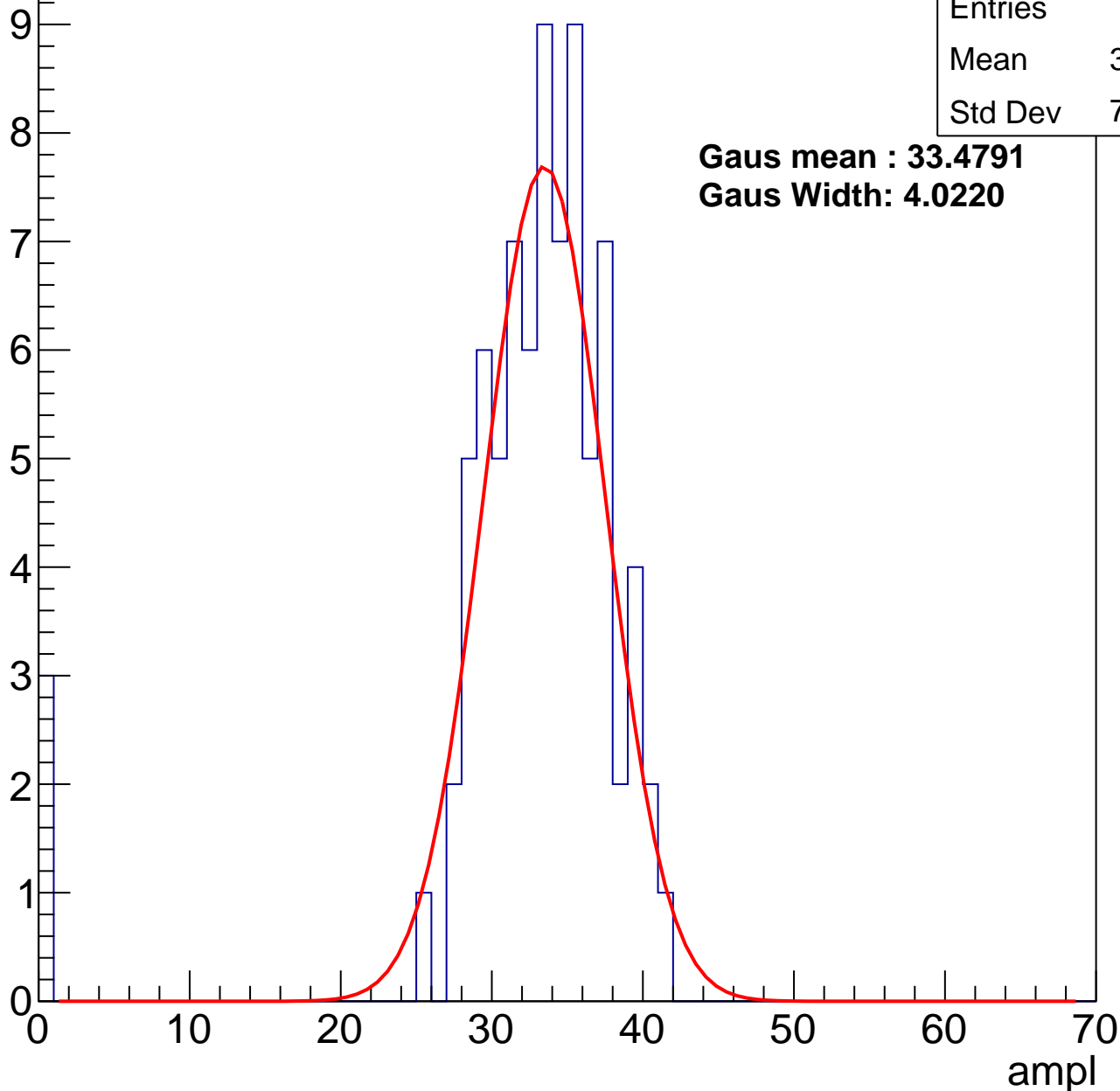
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	81
Mean	32.02
Std Dev	7.185

Gaus mean : 33.4791

Gaus Width: 4.0220



B1L103S, U7-ch80, adc2

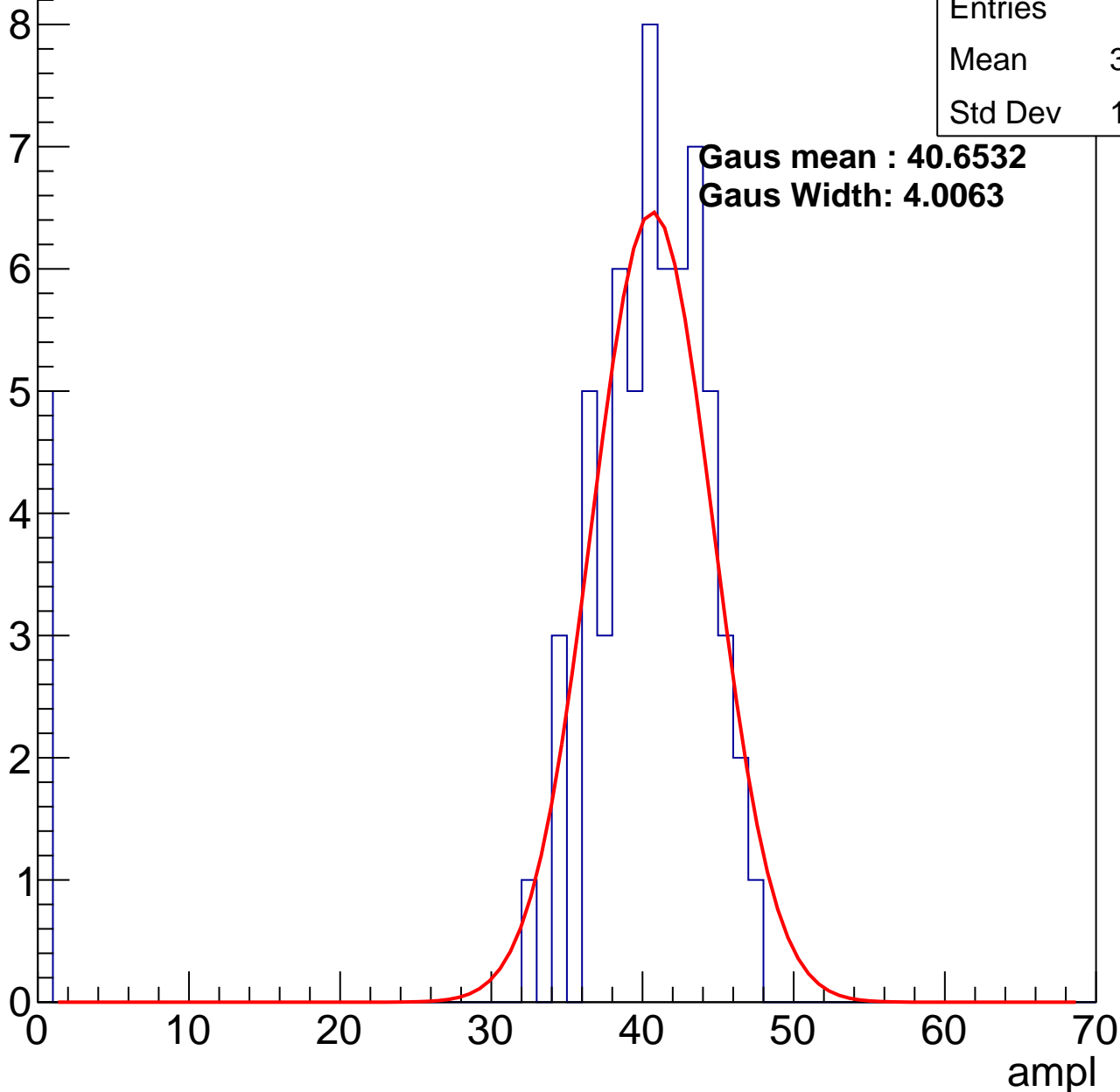
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	37.29
Std Dev	11.14

Gaus mean : 40.6532

Gaus Width: 4.0063

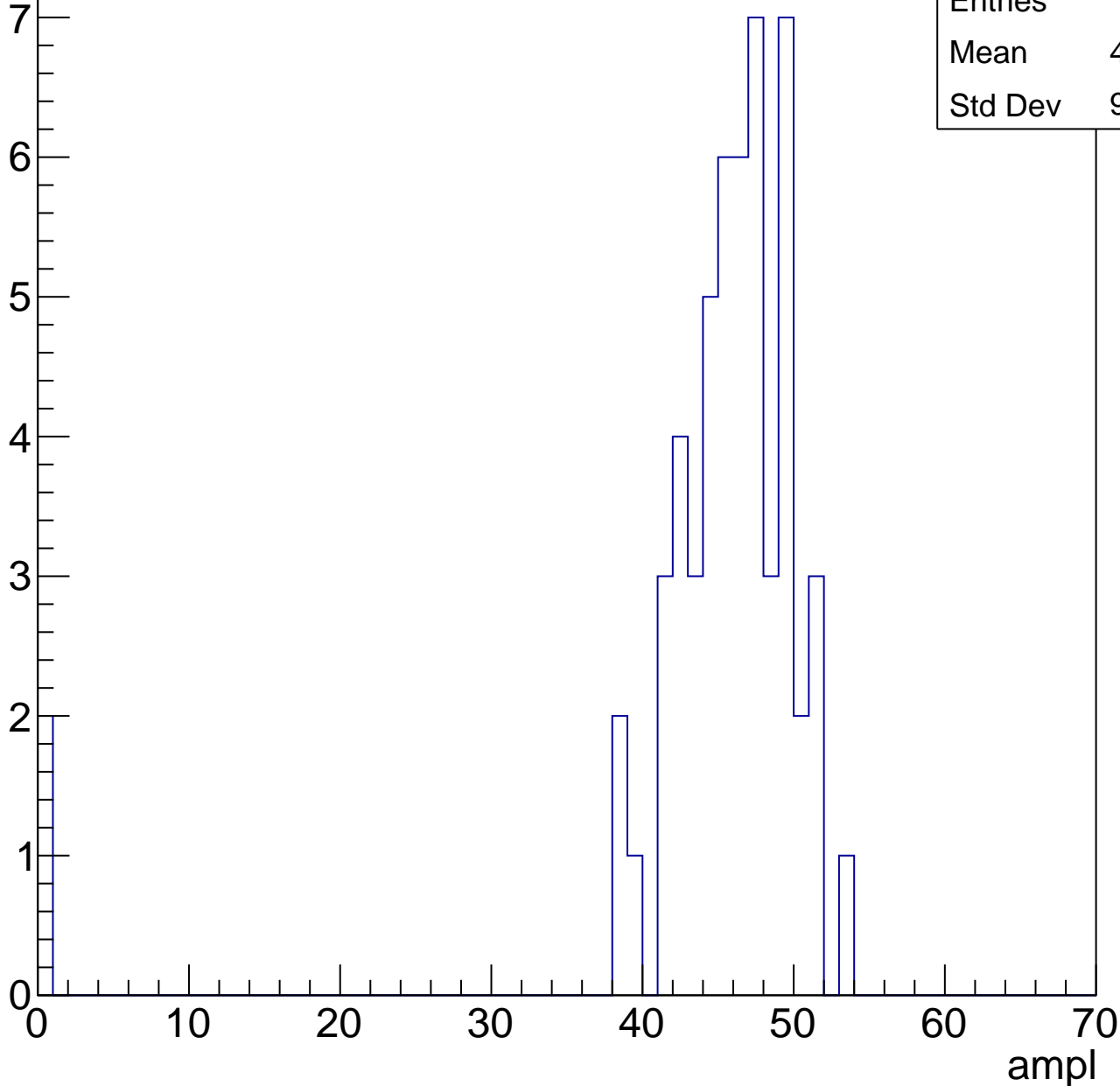


B1L103S, U7-ch80, adc3

calib_packv5_041523_1651.root, FC#0, port C2

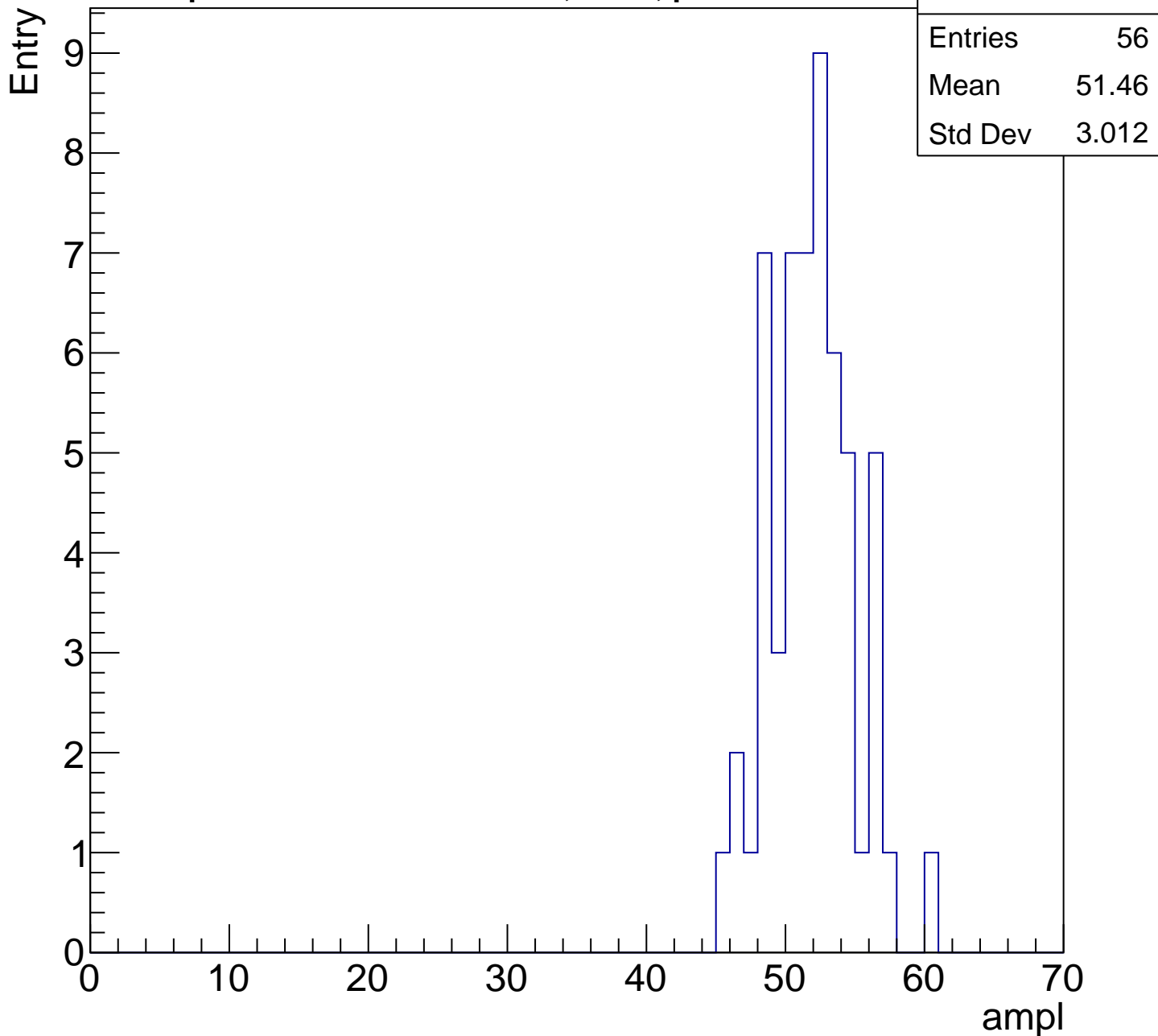
Entry

Entries	55
Mean	44.05
Std Dev	9.176



B1L103S, U7-ch80, adc4

calib_packv5_041523_1651.root, FC#0, port C2

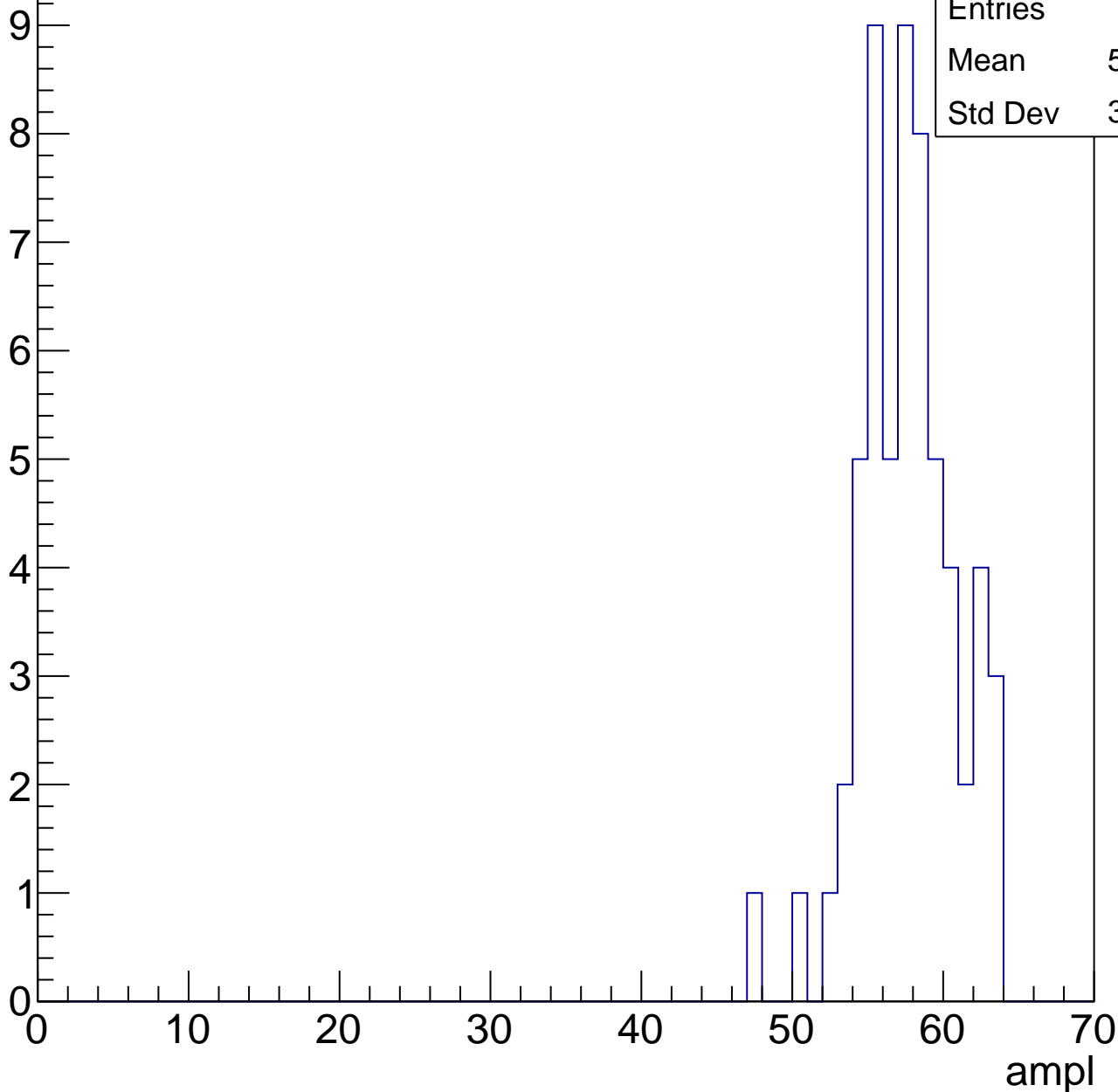


B1L103S, U7-ch80, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	57.14
Std Dev	3.175

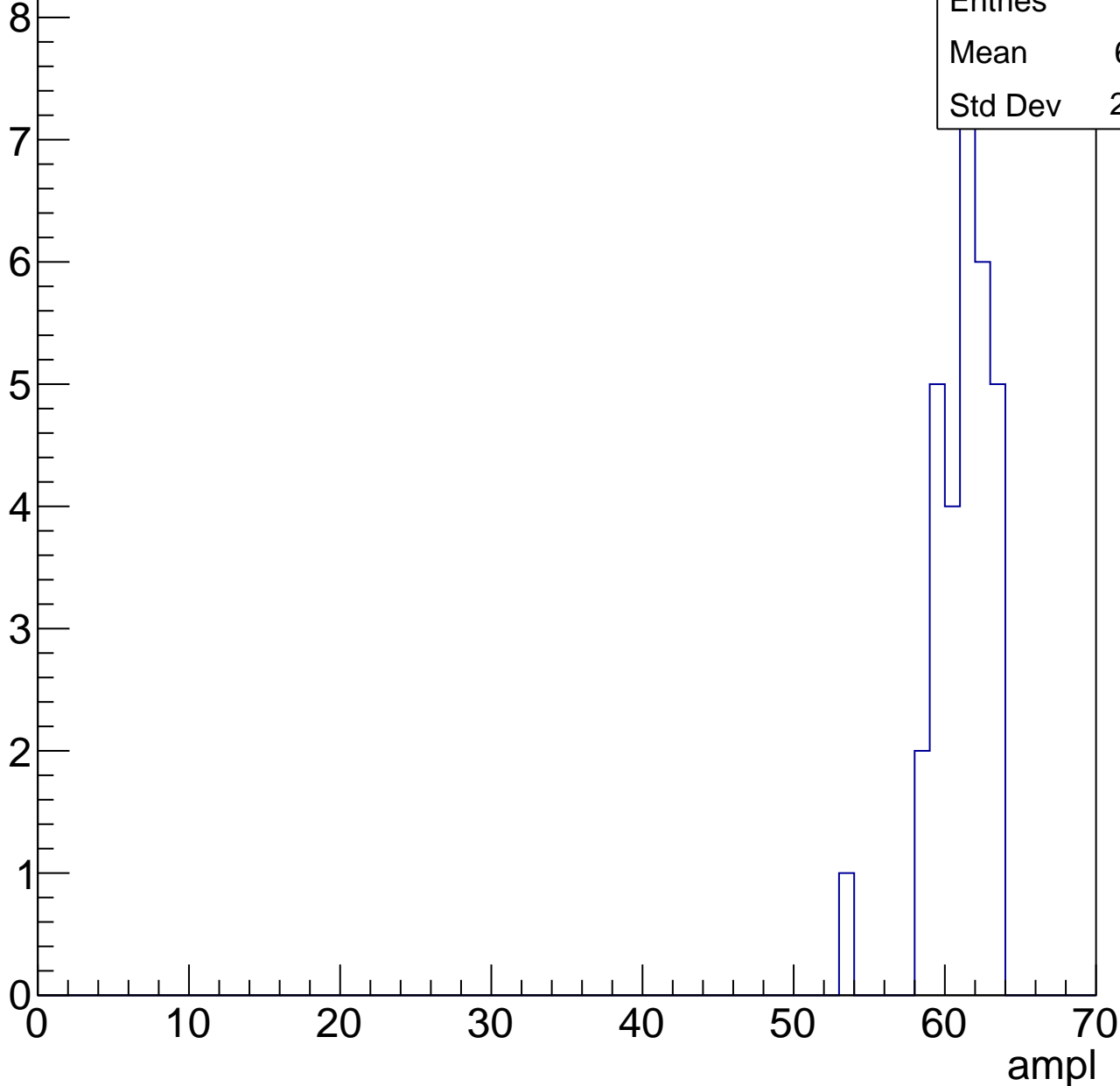


B1L103S, U7-ch80, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	31
Mean	60.61
Std Dev	2.027



B1L103S, U7-ch80, adc7

calib_packv5_041523_1651.root, FC#0, port C2

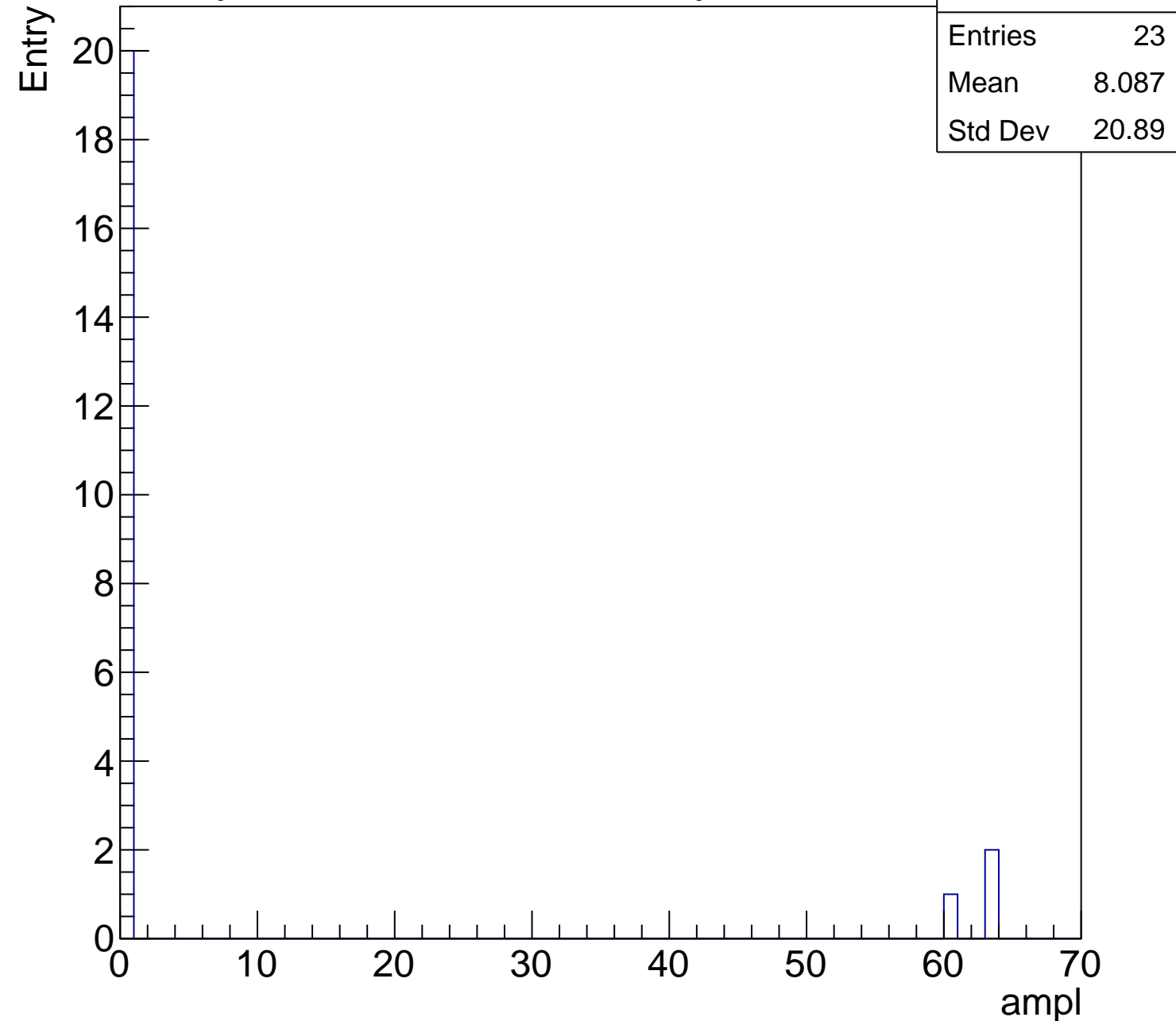
Entry

20
18
16
14
12
10
8
6
4
2
0

Entries	23
Mean	8.087
Std Dev	20.89

0 10 20 30 40 50 60 70

ampl



B1L103S, U7-ch81, adc0

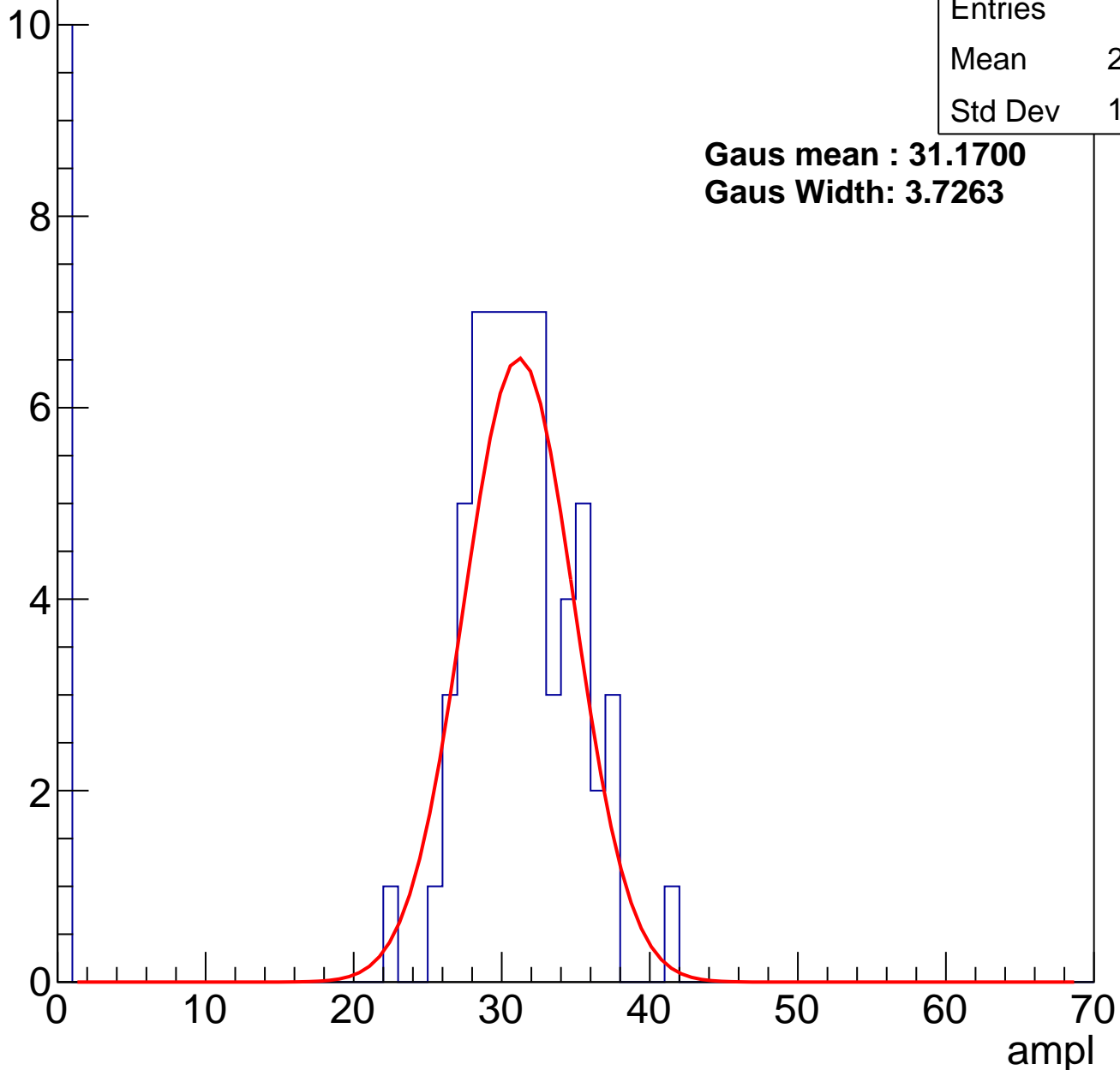
calib_packv5_041523_1651.root, FC#0, port C2

Entries	73
Mean	26.63
Std Dev	11.09

Gaus mean : 31.1700

Gaus Width: 3.7263

Entry



B1L103S, U7-ch81, adc1

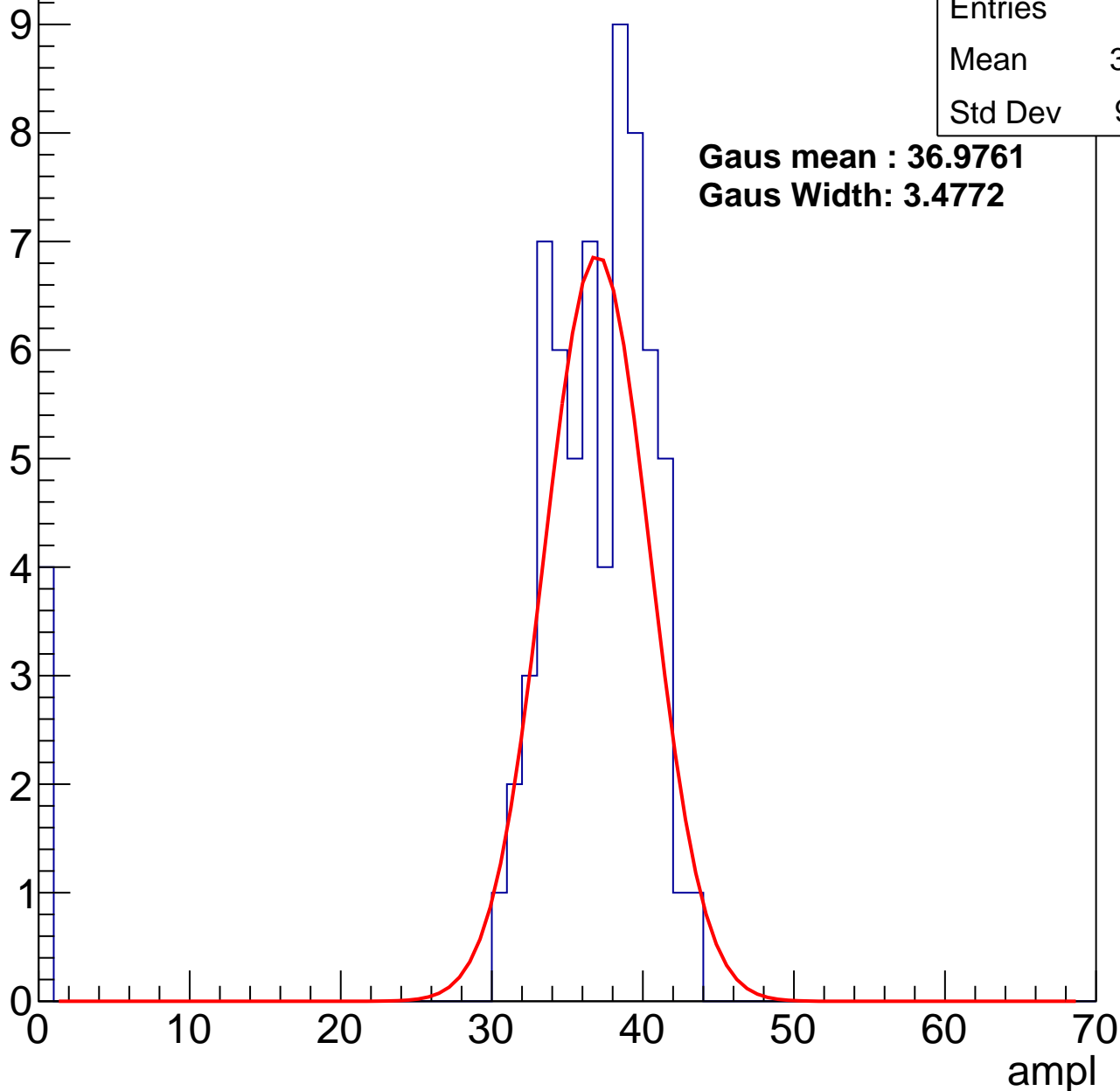
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	34.52
Std Dev	9.071

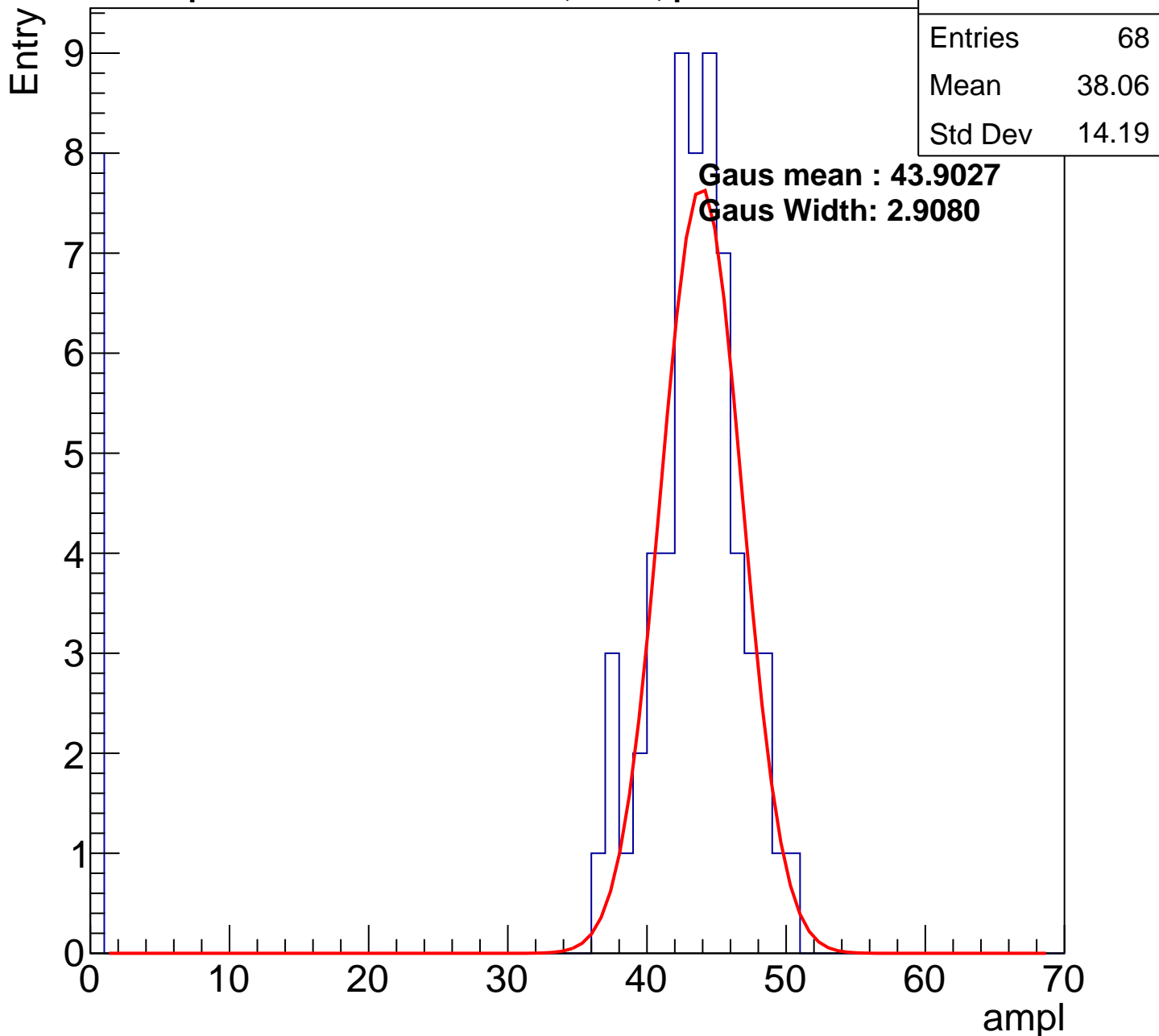
Gaus mean : 36.9761

Gaus Width: 3.4772



B1L103S, U7-ch81, adc2

calib_packv5_041523_1651.root, FC#0, port C2

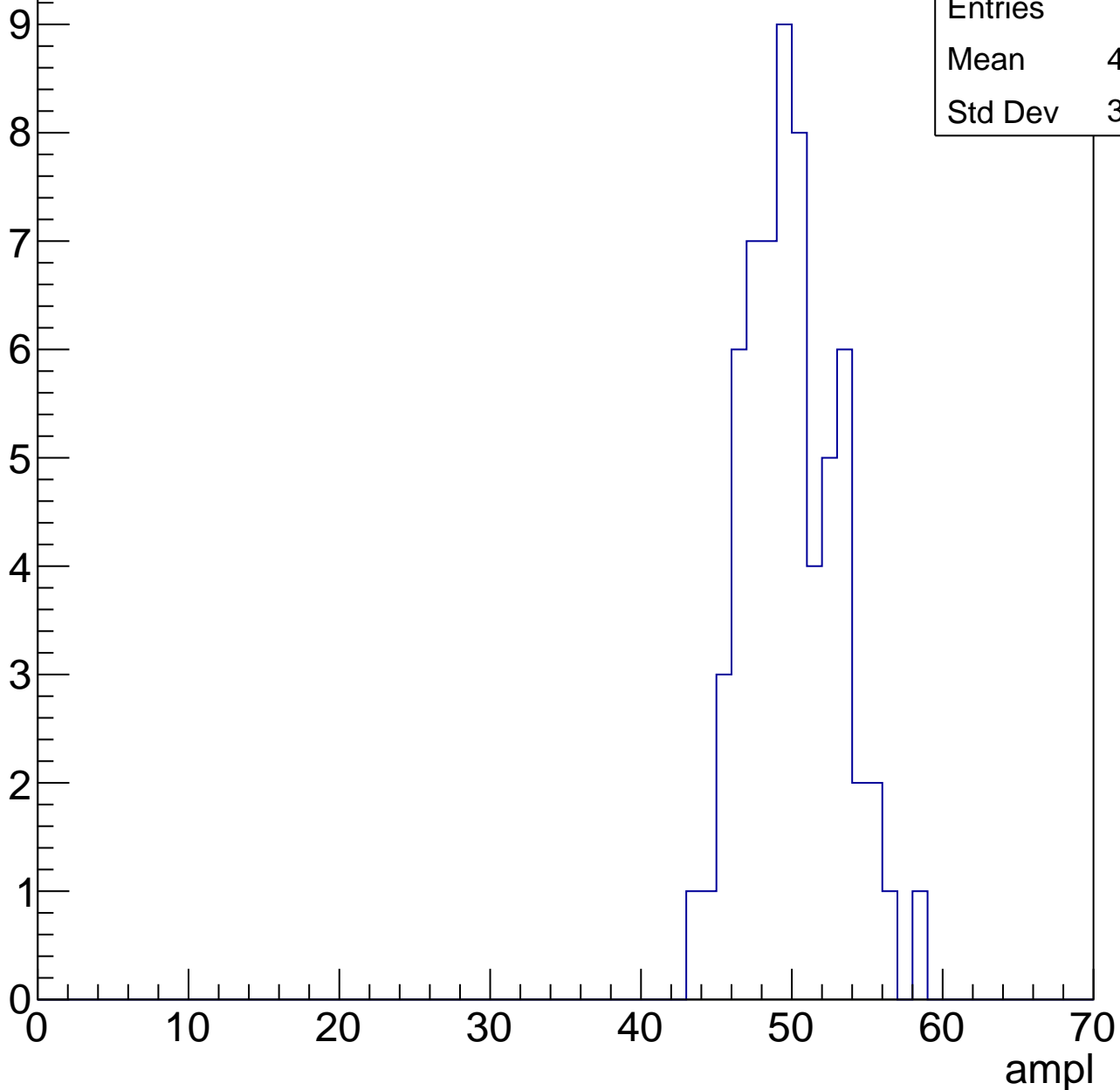


B1L103S, U7-ch81, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

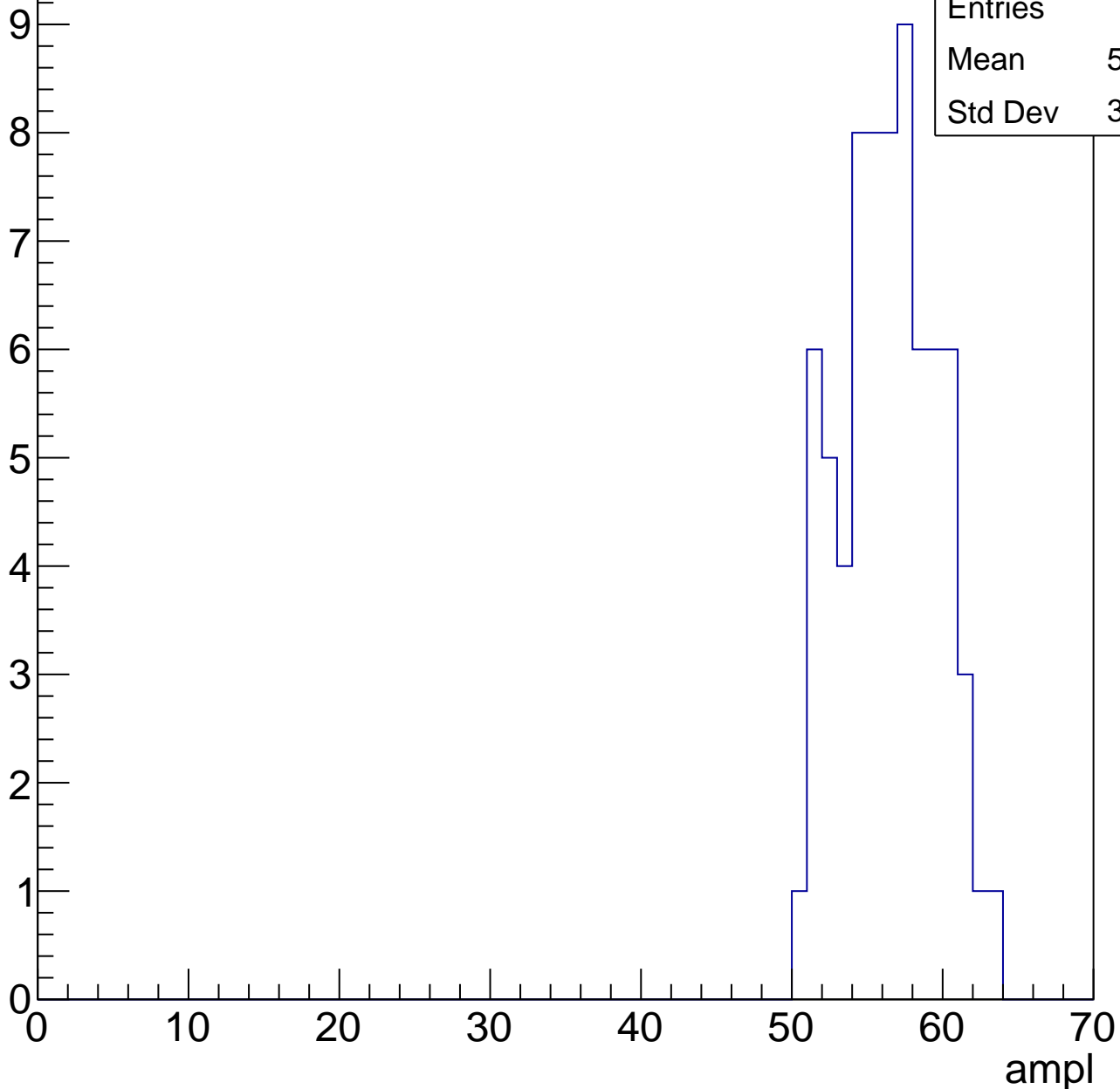
Entries	63
Mean	49.49
Std Dev	3.085



B1L103S, U7-ch81, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



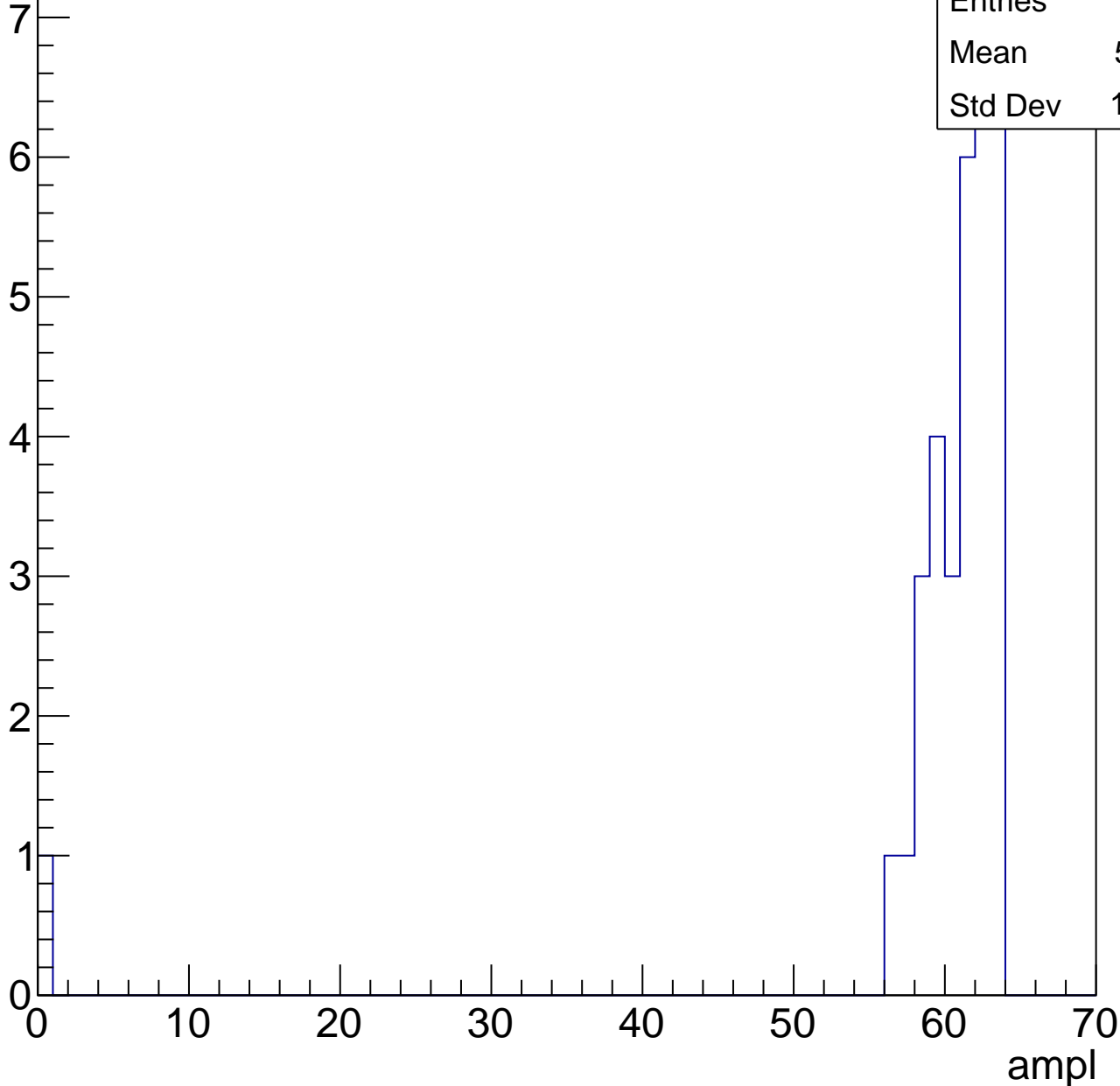
Entries	72
Mean	55.99
Std Dev	3.084

B1L103S, U7-ch81, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

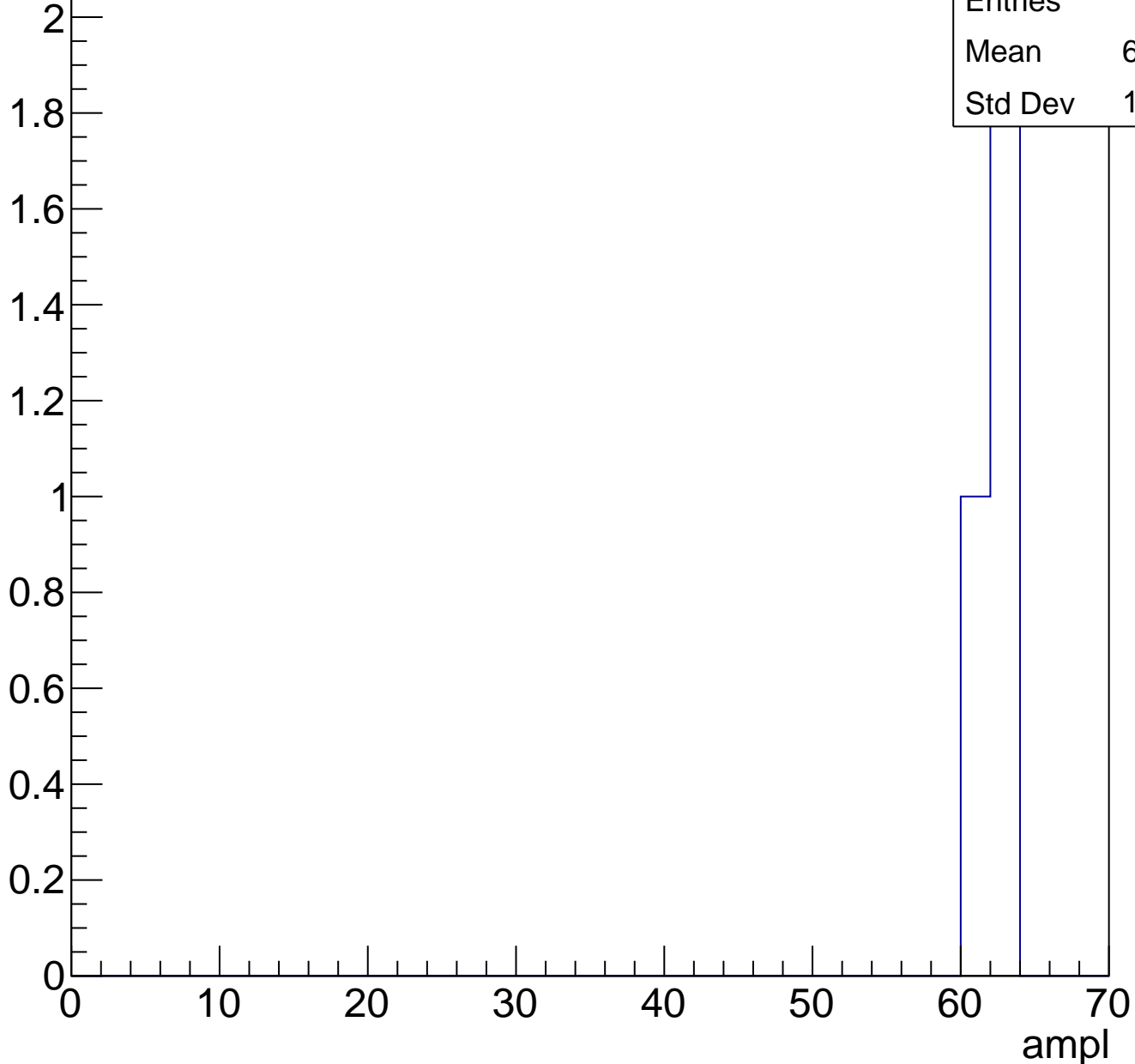
Entries	33
Mean	58.91
Std Dev	10.59



B1L103S, U7-ch81, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	6
Mean	61.83
Std Dev	1.067

B1L103S, U7-ch81, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

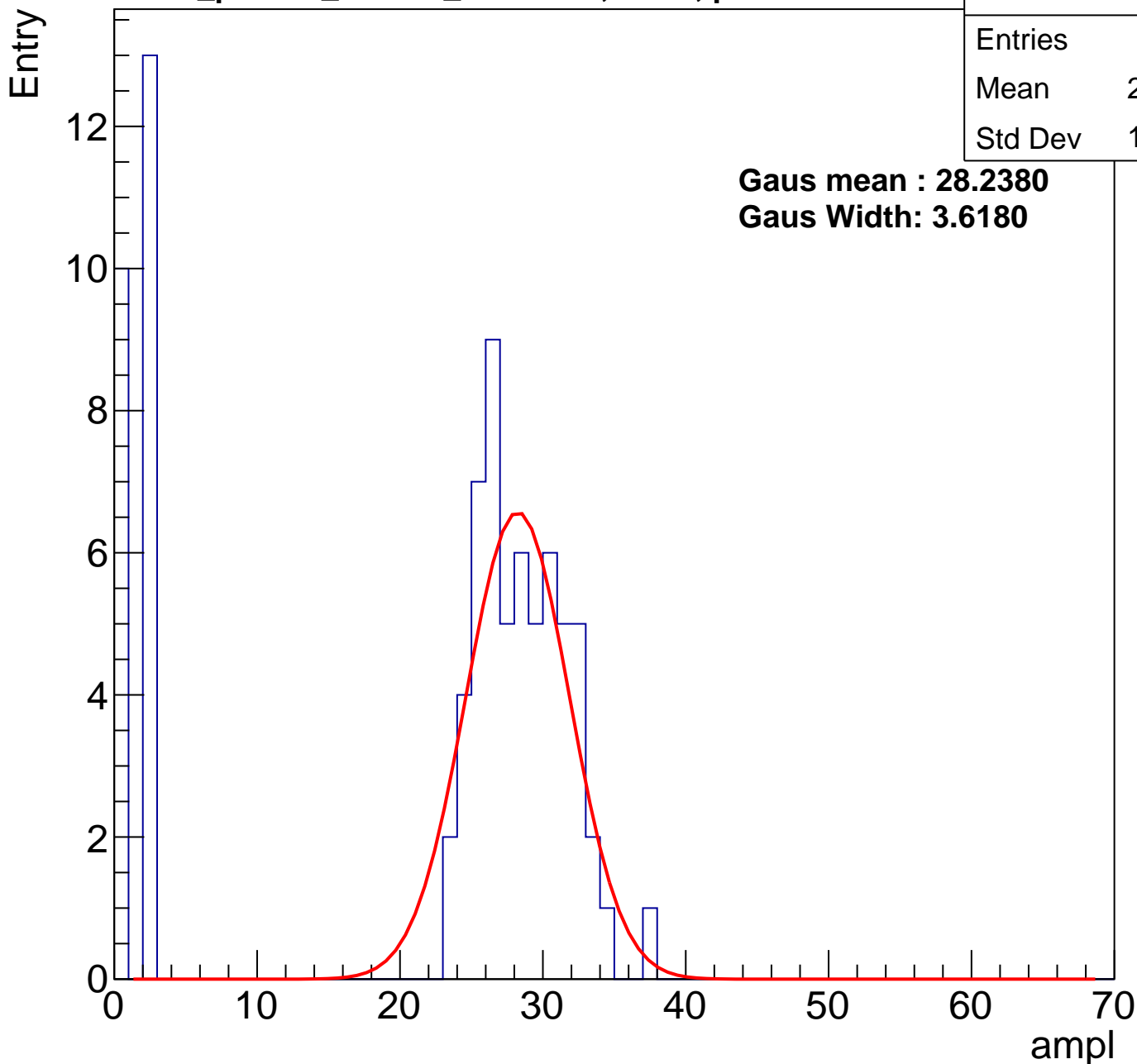
B1L103S, U7-ch82, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	20.46
Std Dev	12.45

Gaus mean : 28.2380

Gaus Width: 3.6180



B1L103S, U7-ch82, adc1

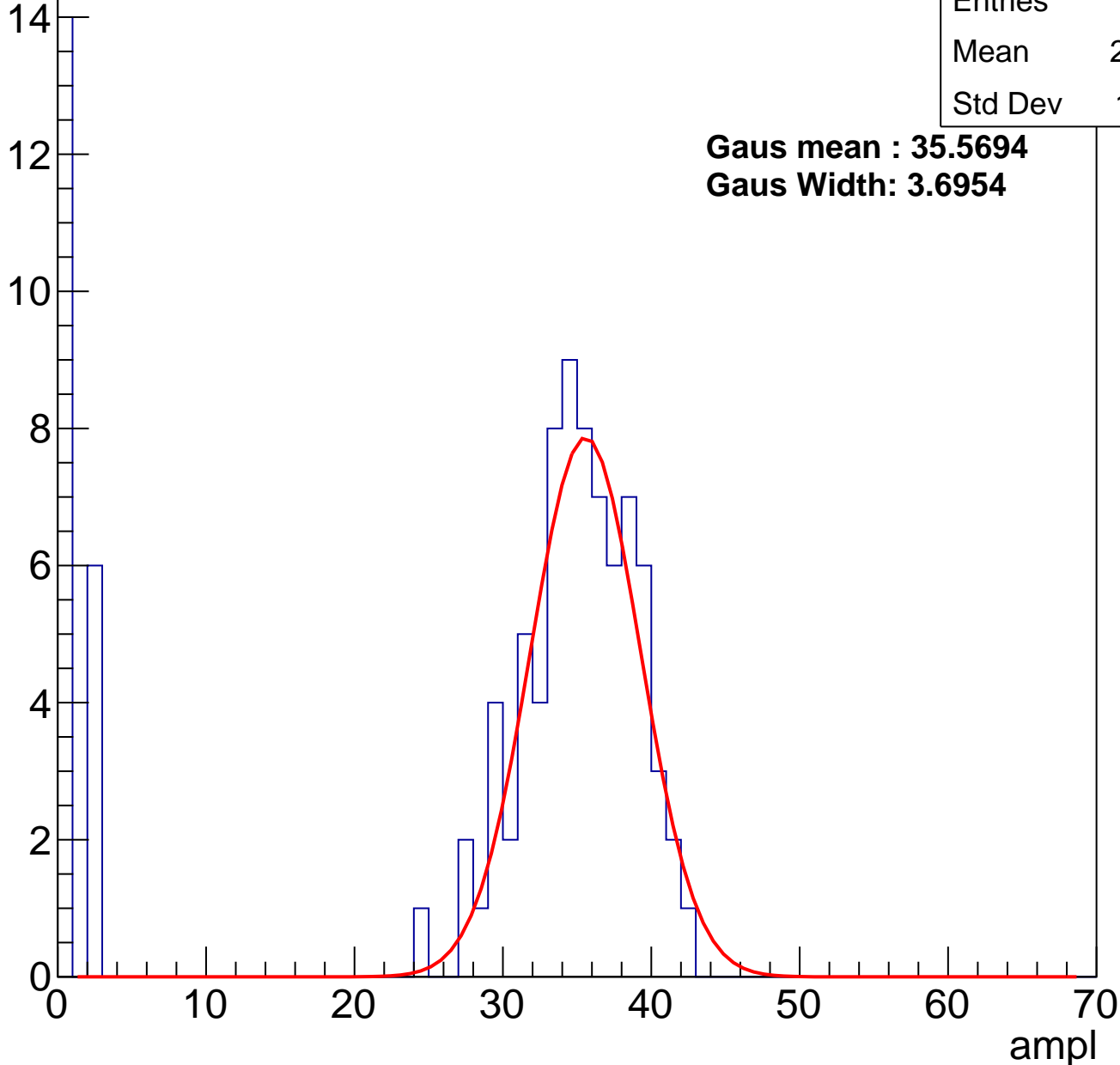
calib_packv5_041523_1651.root, FC#0, port C2

Entries	96
Mean	27.55
Std Dev	14.21

Gaus mean : 35.5694

Gaus Width: 3.6954

Entry



B1L103S, U7-ch82, adc2

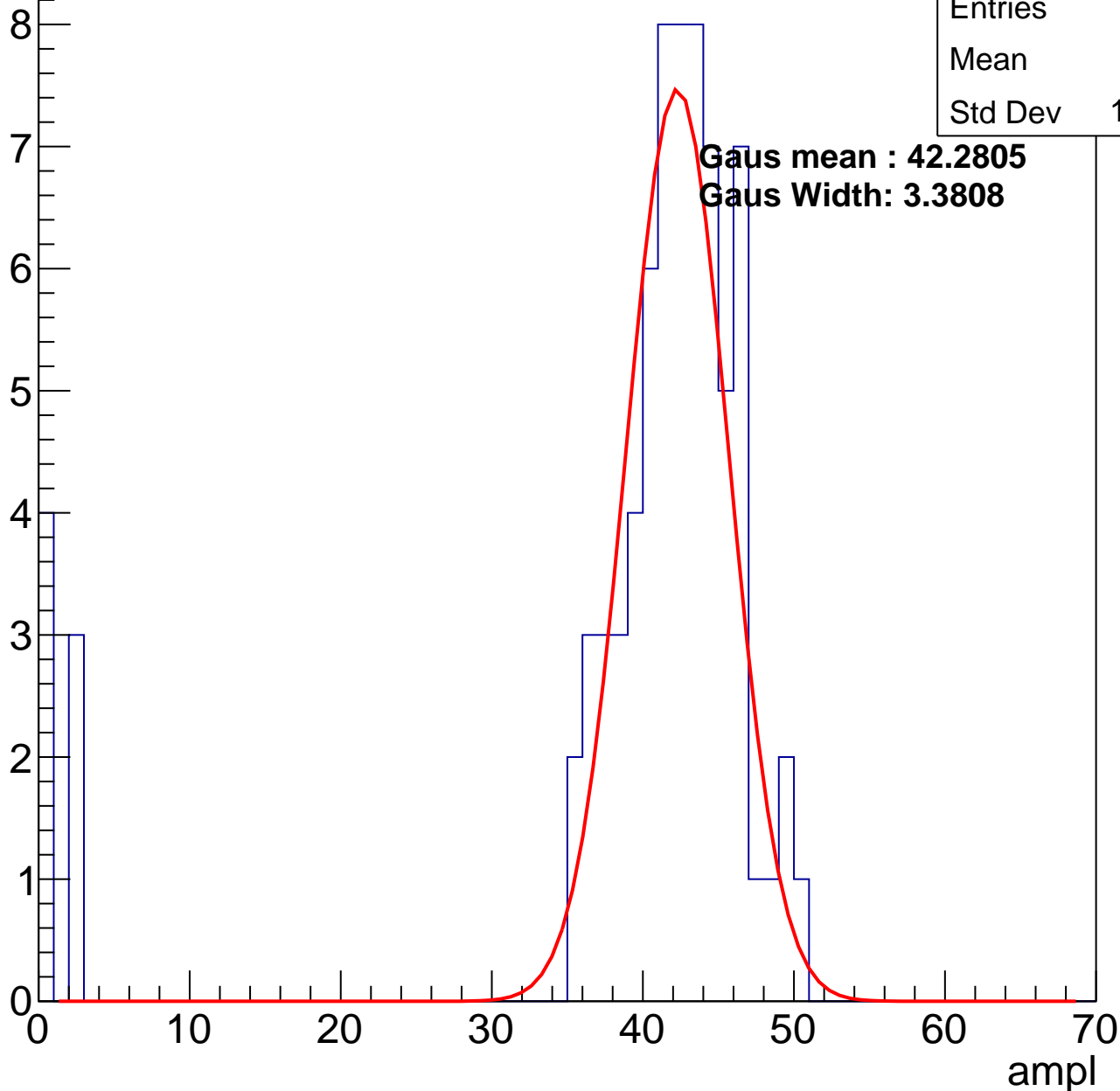
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	38.3
Std Dev	12.37

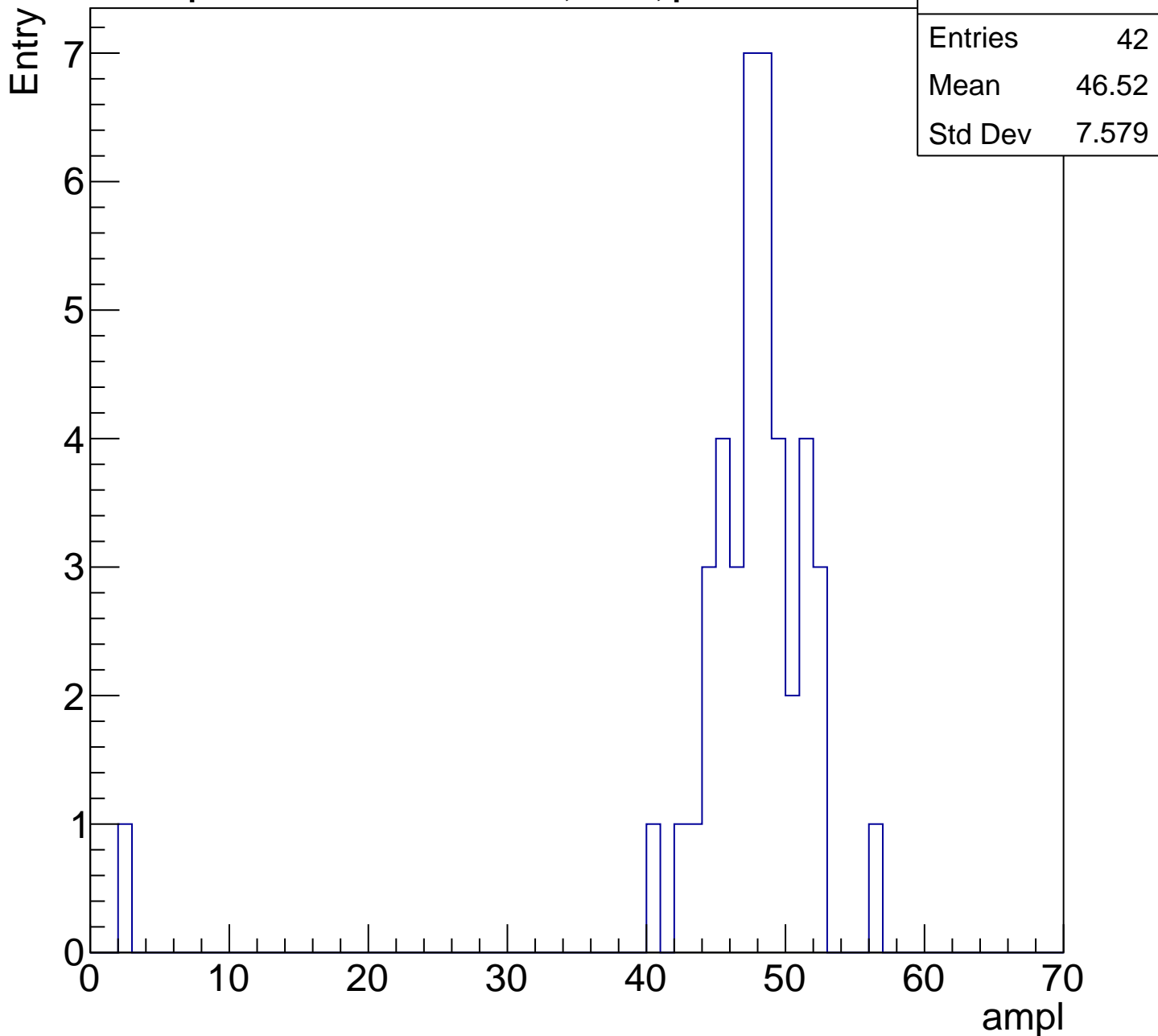
Gaus mean : 42.2805

Gaus Width: 3.3808



B1L103S, U7-ch82, adc3

calib_packv5_041523_1651.root, FC#0, port C2

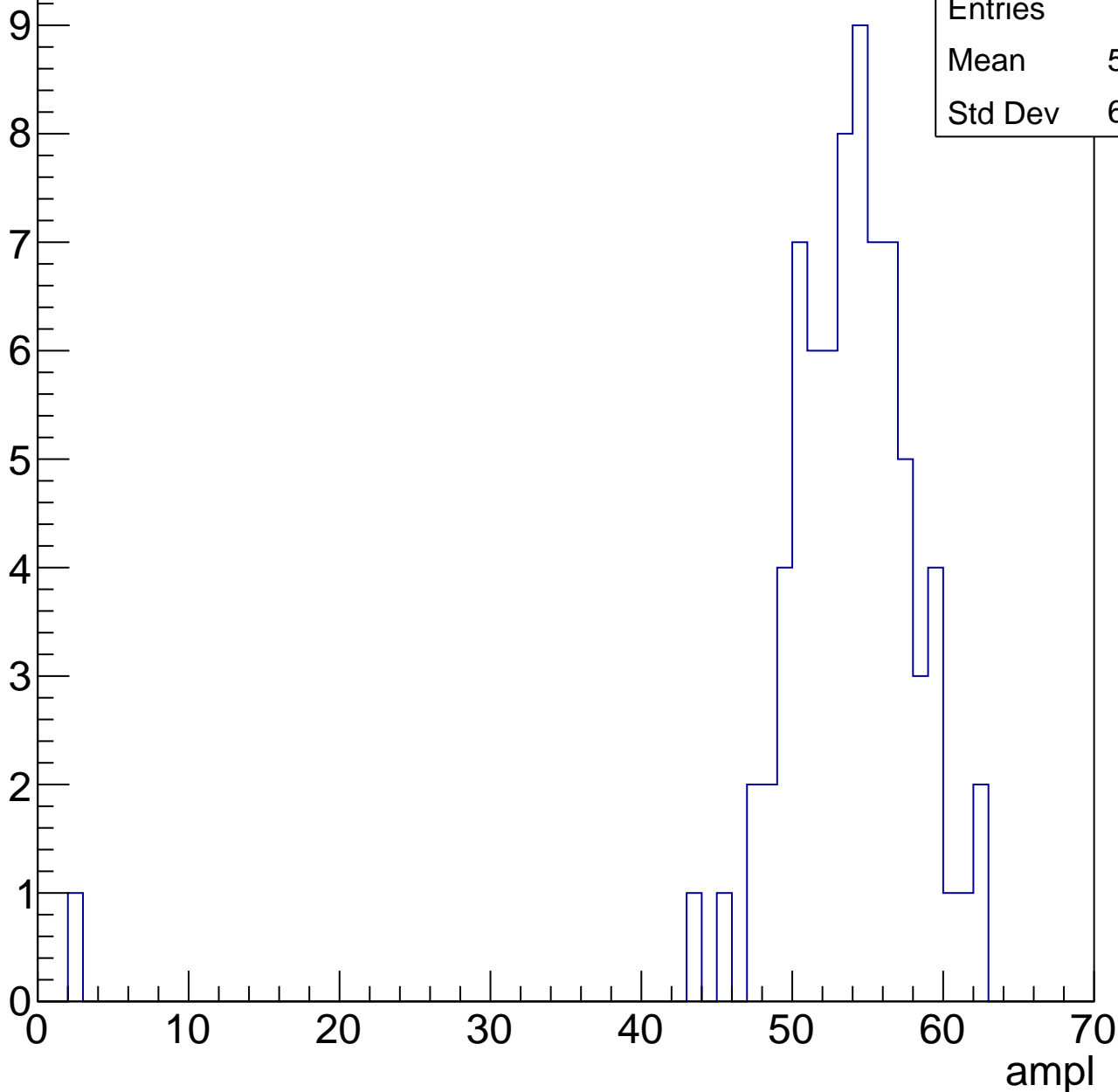


B1L103S, U7-ch82, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	52.87
Std Dev	6.948



B1L103S, U7-ch82, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

7

6

5

4

3

2

1

0

Entries 45

Mean 58.76

Std Dev 2.876

ampl

0

10

20

30

40

50

60

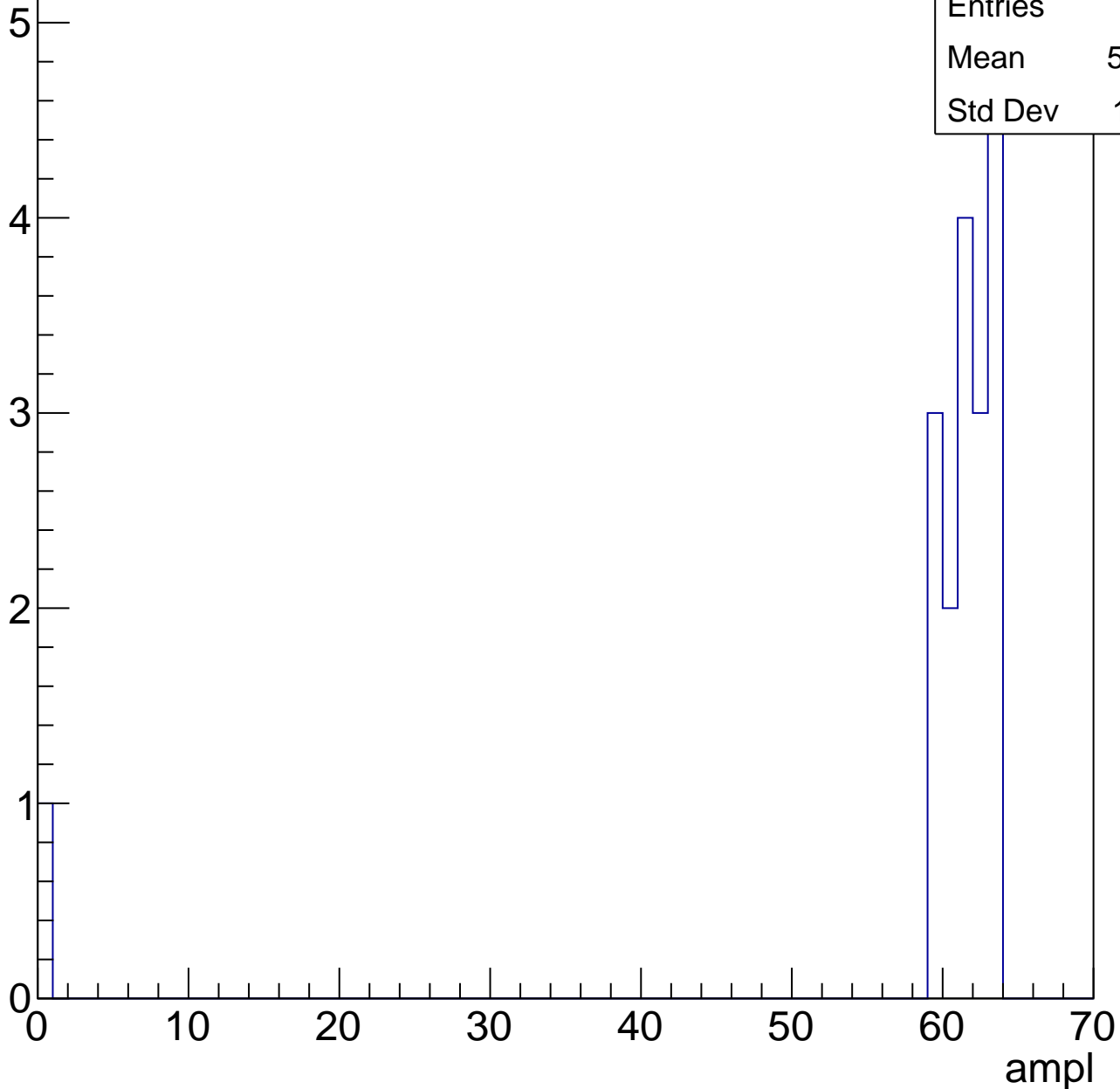
70

B1L103S, U7-ch82, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

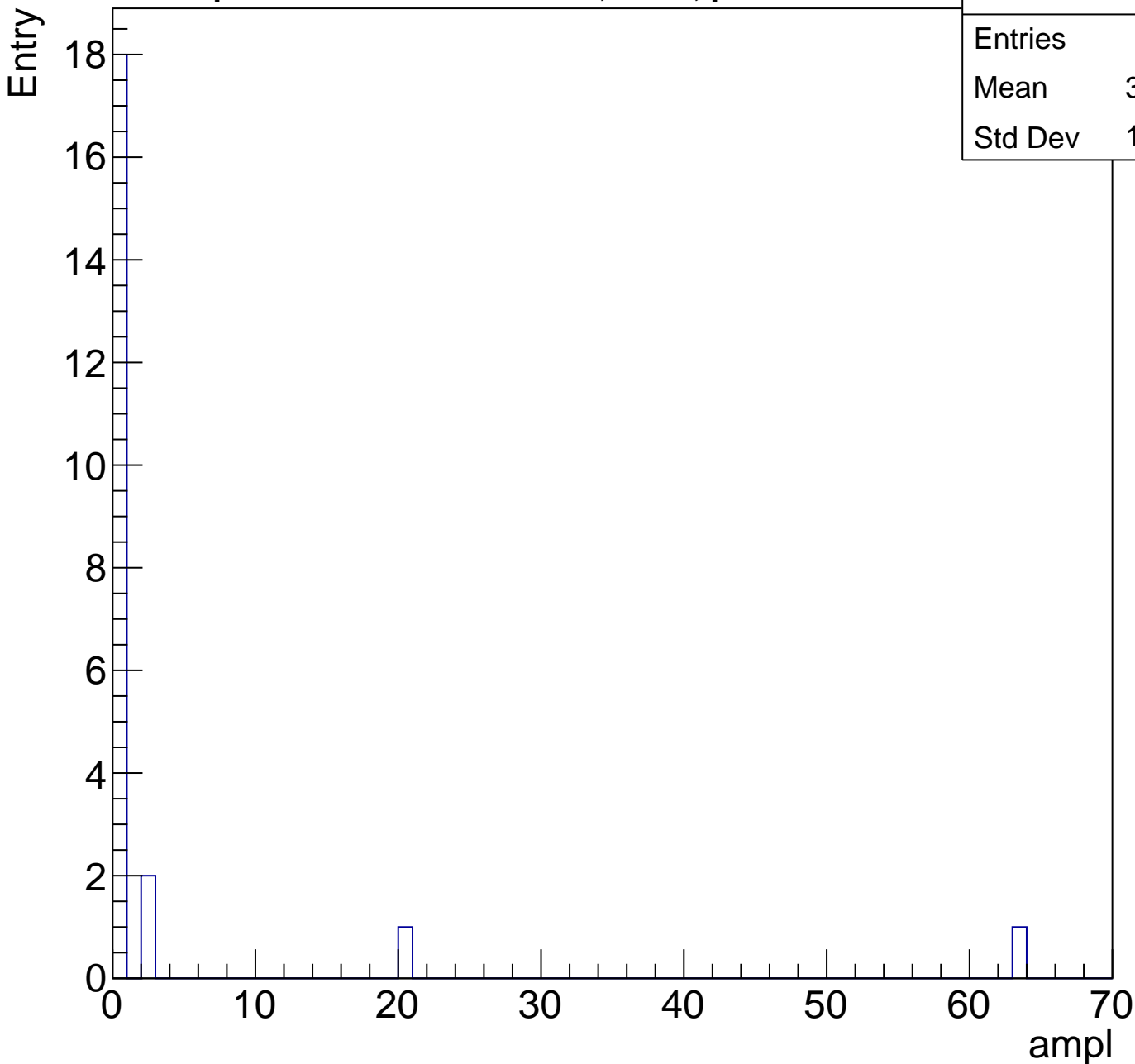
Entries	18
Mean	57.89
Std Dev	14.11



B1L103S, U7-ch82, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	22
Mean	3.955
Std Dev	13.54



B1L103S, U7-ch83, adc0

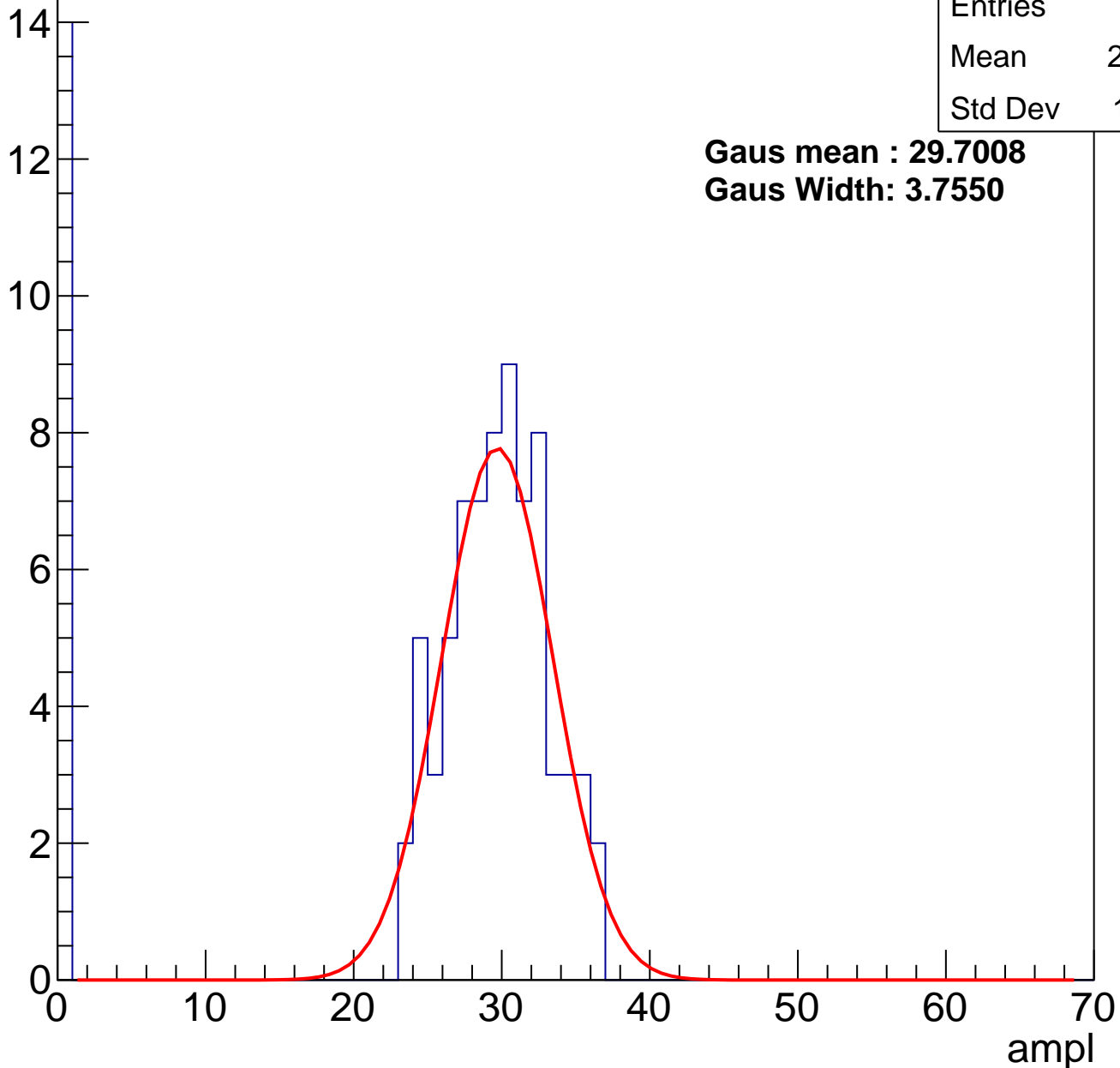
calib_packv5_041523_1651.root, FC#0, port C2

Entries	86
Mean	24.52
Std Dev	11.21

Gaus mean : 29.7008

Gaus Width: 3.7550

Entry



B1L103S, U7-ch83, adc1

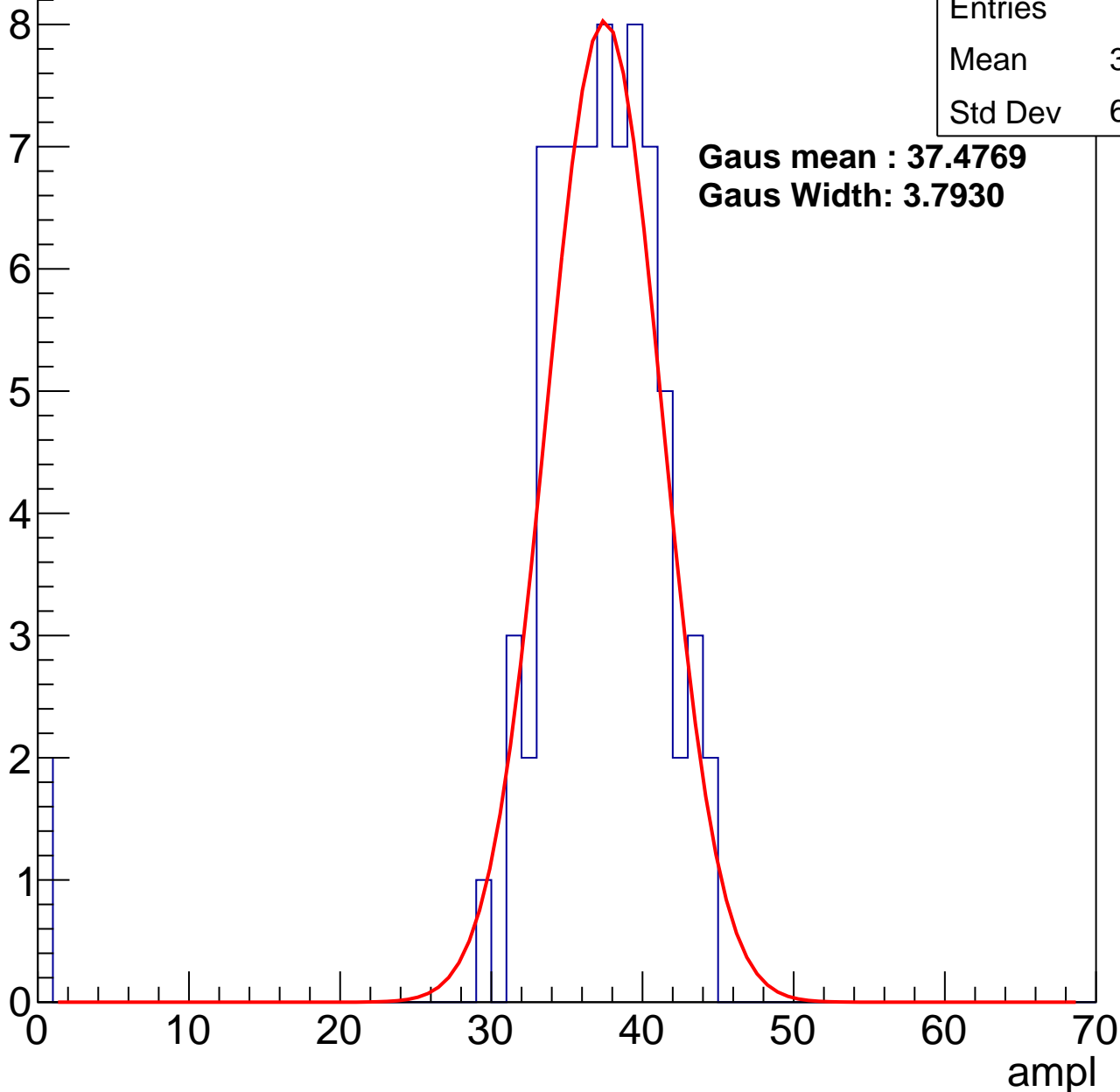
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	36.05
Std Dev	6.735

Gaus mean : 37.4769

Gaus Width: 3.7930



B1L103S, U7-ch83, adc2

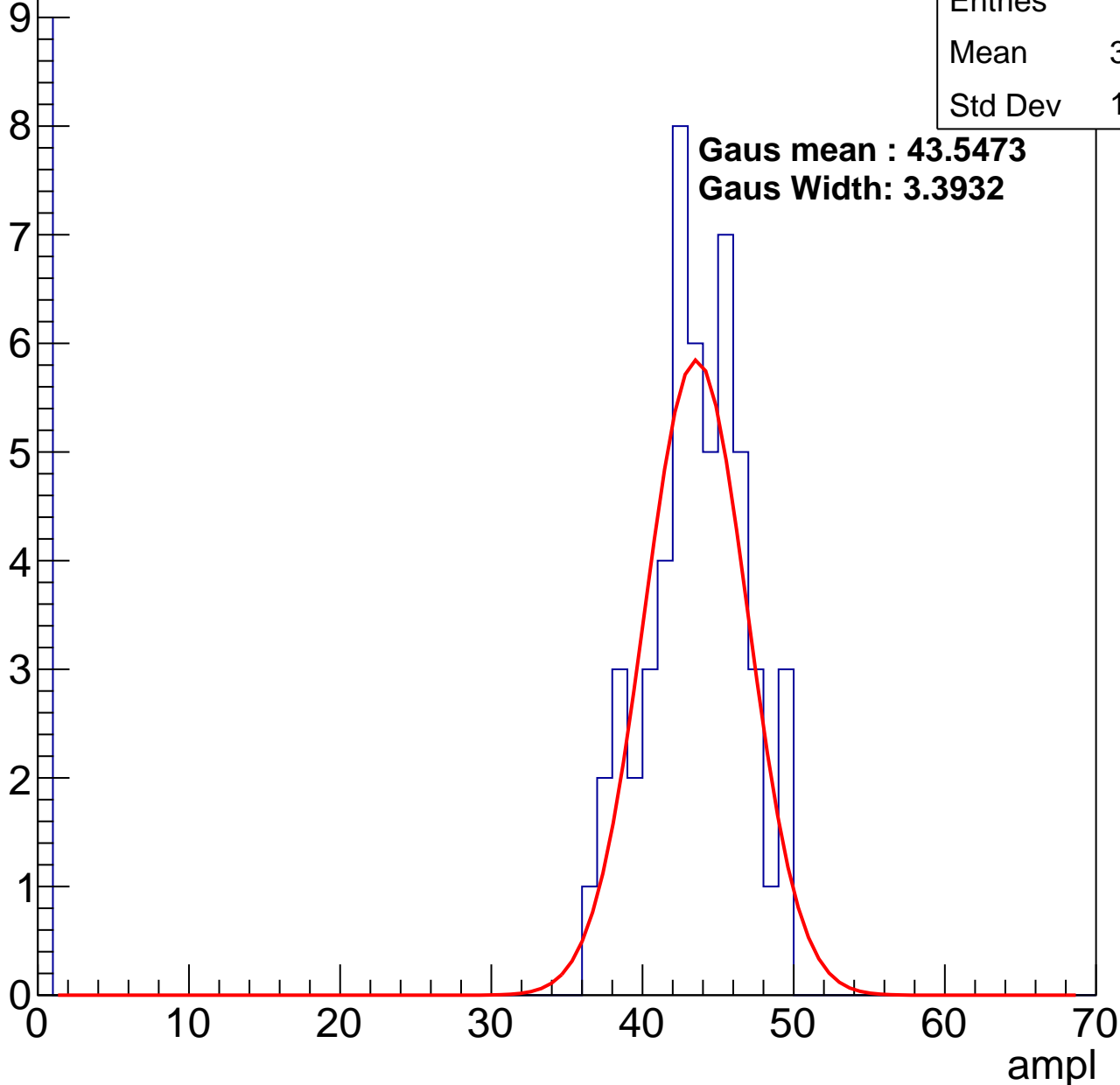
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	36.79
Std Dev	15.44

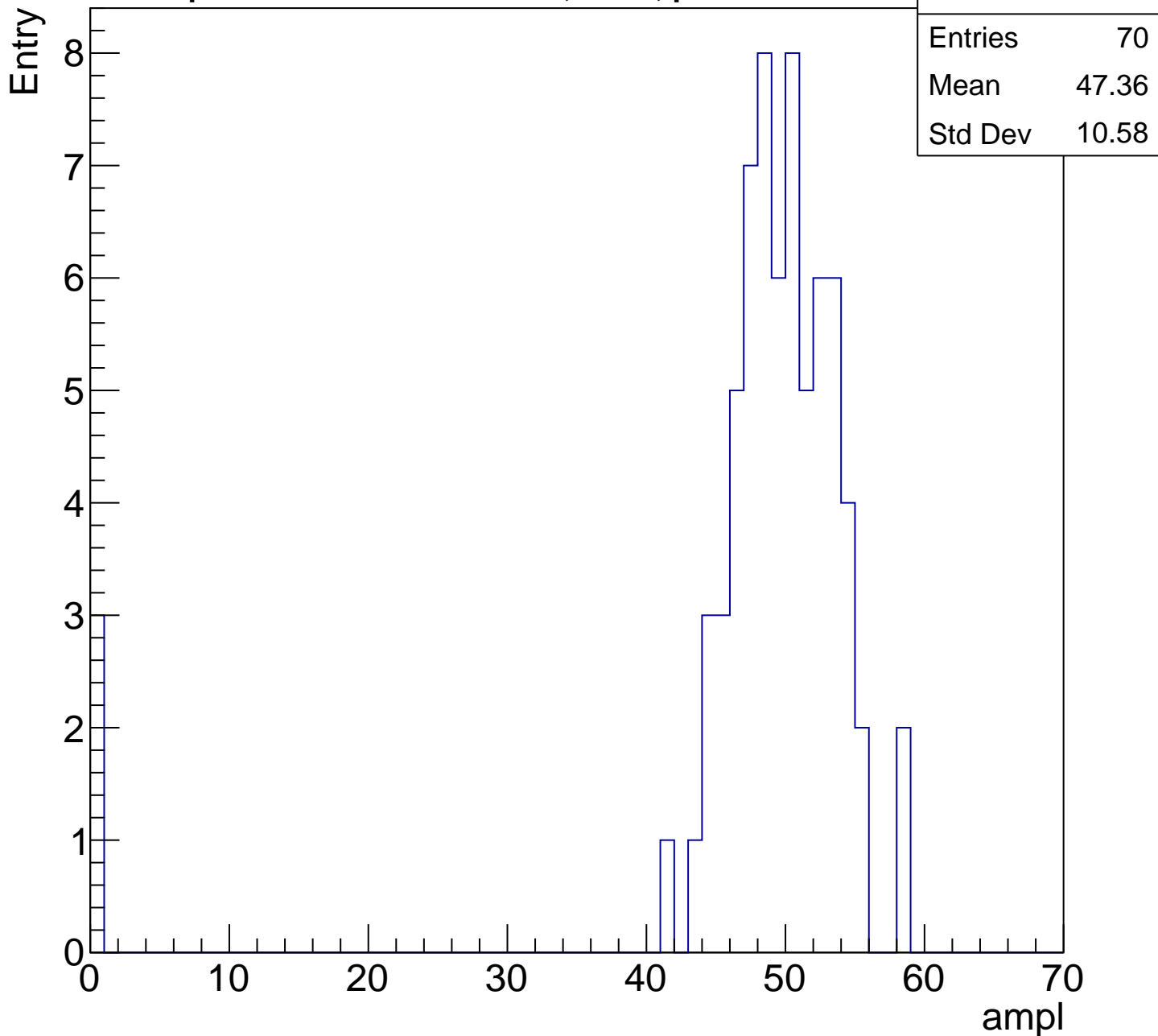
Gaus mean : 43.5473

Gaus Width: 3.3932



B1L103S, U7-ch83, adc3

calib_packv5_041523_1651.root, FC#0, port C2

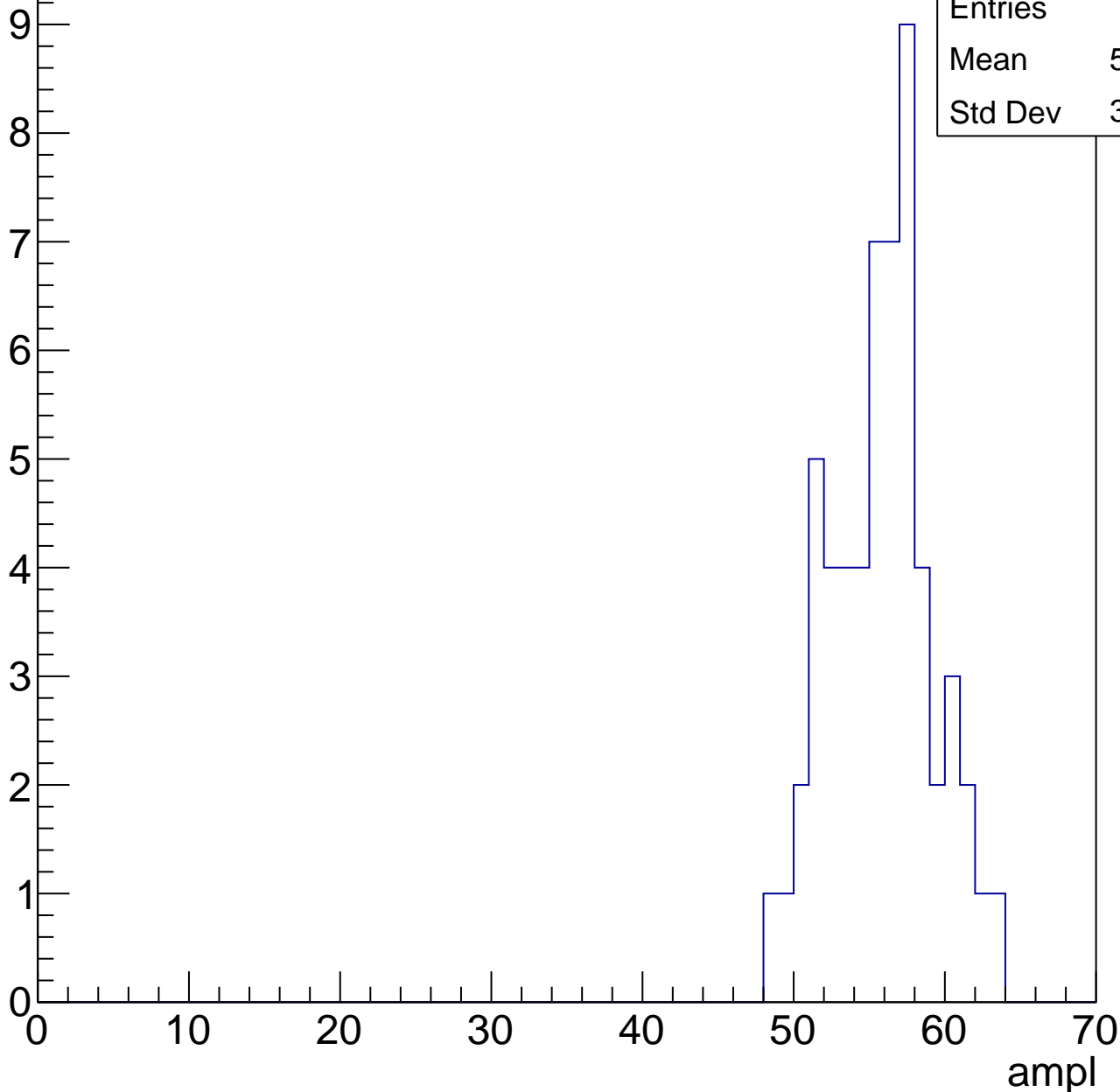


B1L103S, U7-ch83, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	55.35
Std Dev	3.338



B1L103S, U7-ch83, adc5

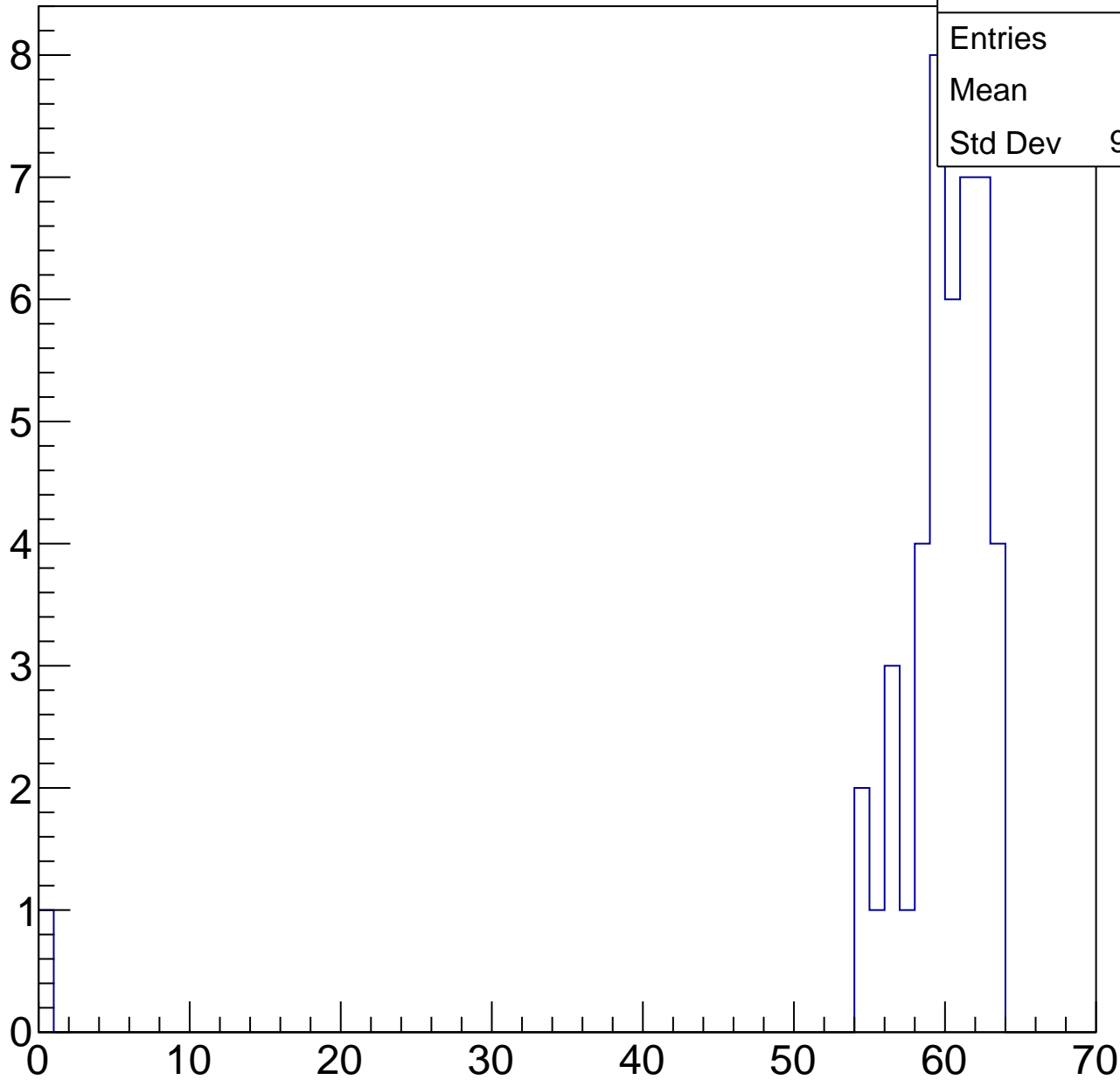
calib_packv5_041523_1651.root, FC#0, port C2

Entry

8
7
6
5
4
3
2
1
0

Entries	44
Mean	58.3
Std Dev	9.196

ampl

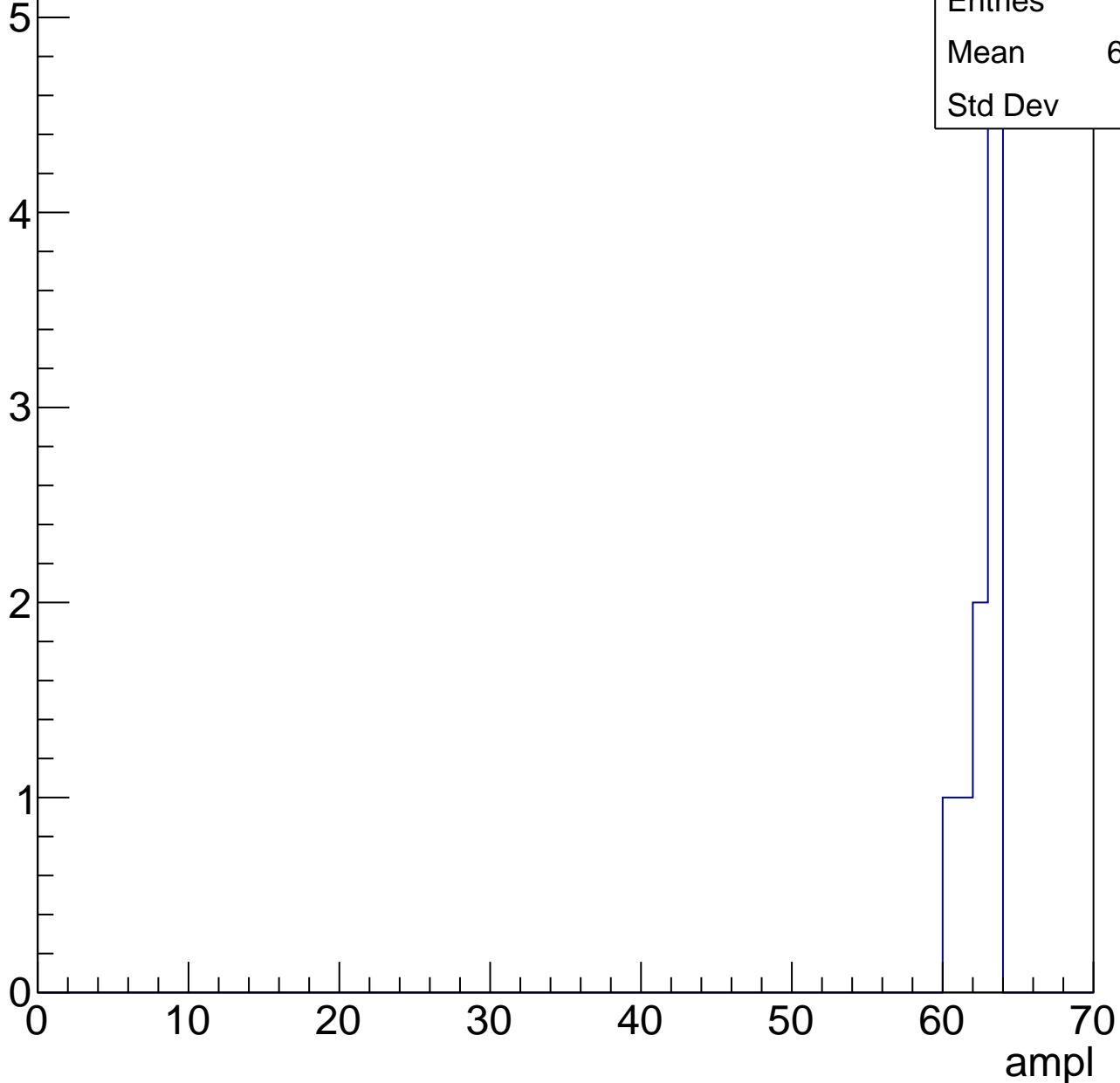


B1L103S, U7-ch83, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	9
Mean	62.22
Std Dev	1.03



B1L103S, U7-ch83, adc7

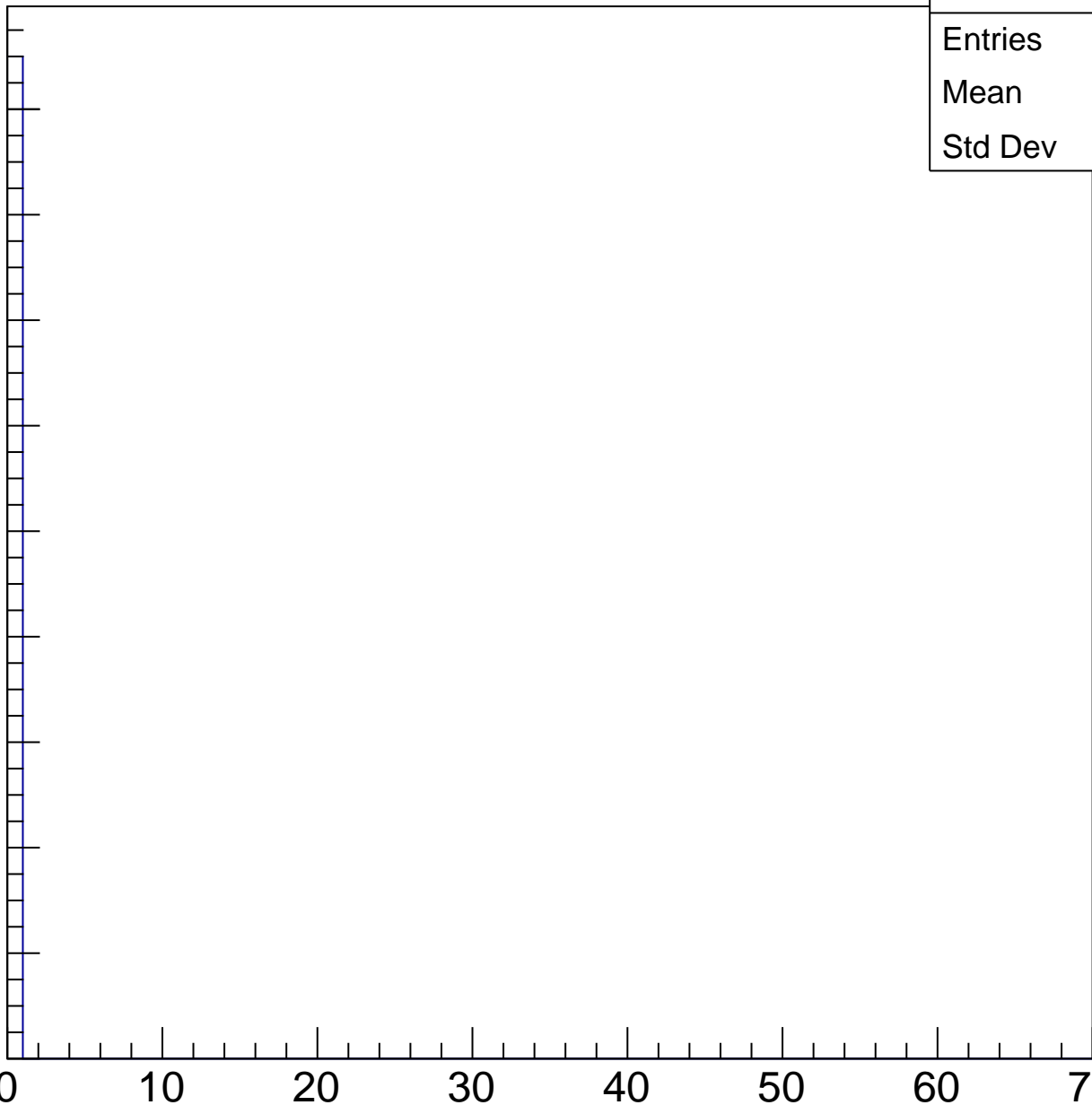
calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl



B1L103S, U7-ch84, adc0

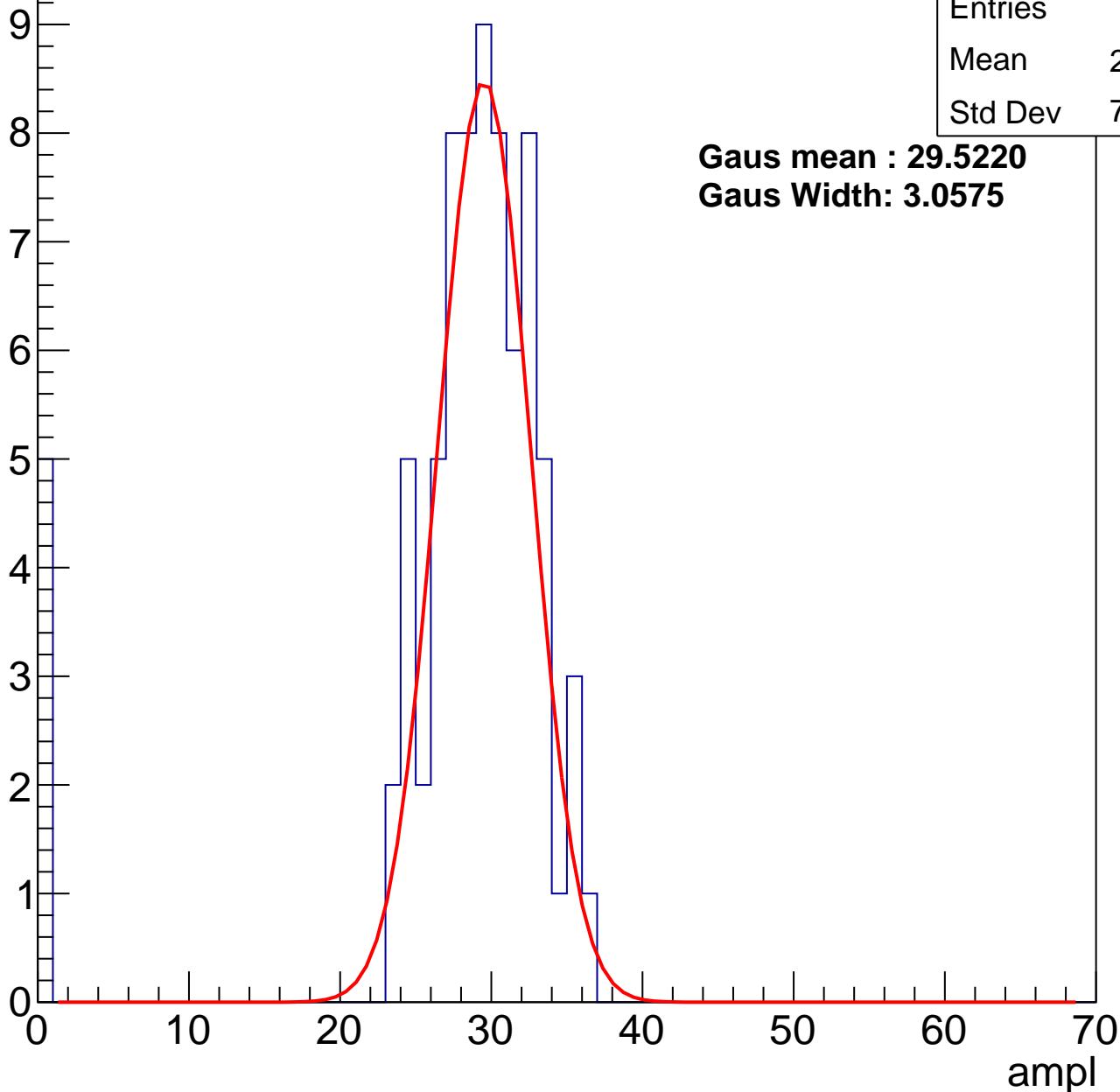
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	76
Mean	27.22
Std Dev	7.818

Gaus mean : 29.5220

Gaus Width: 3.0575



B1L103S, U7-ch84, adc1

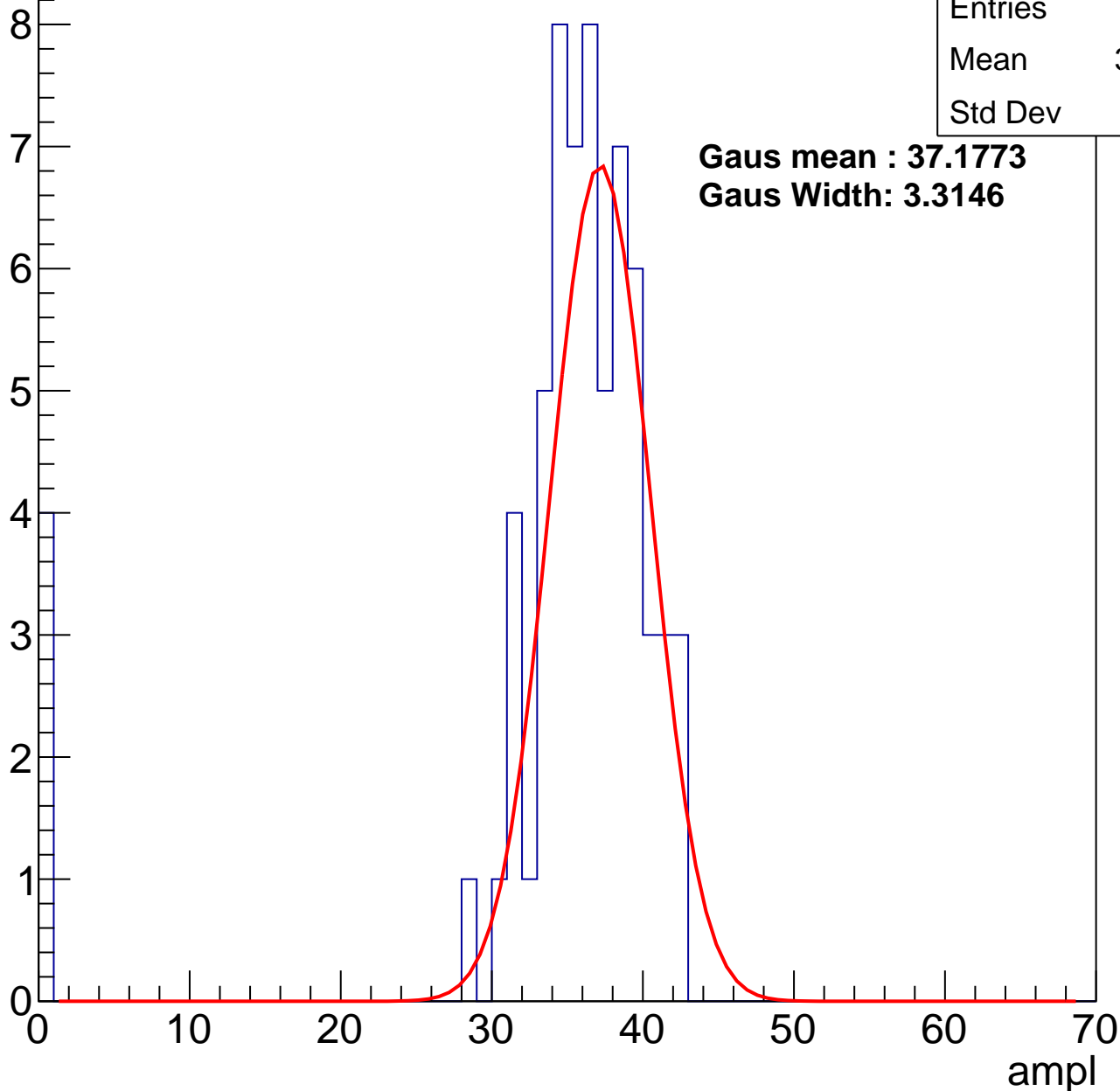
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	33.91
Std Dev	9.14

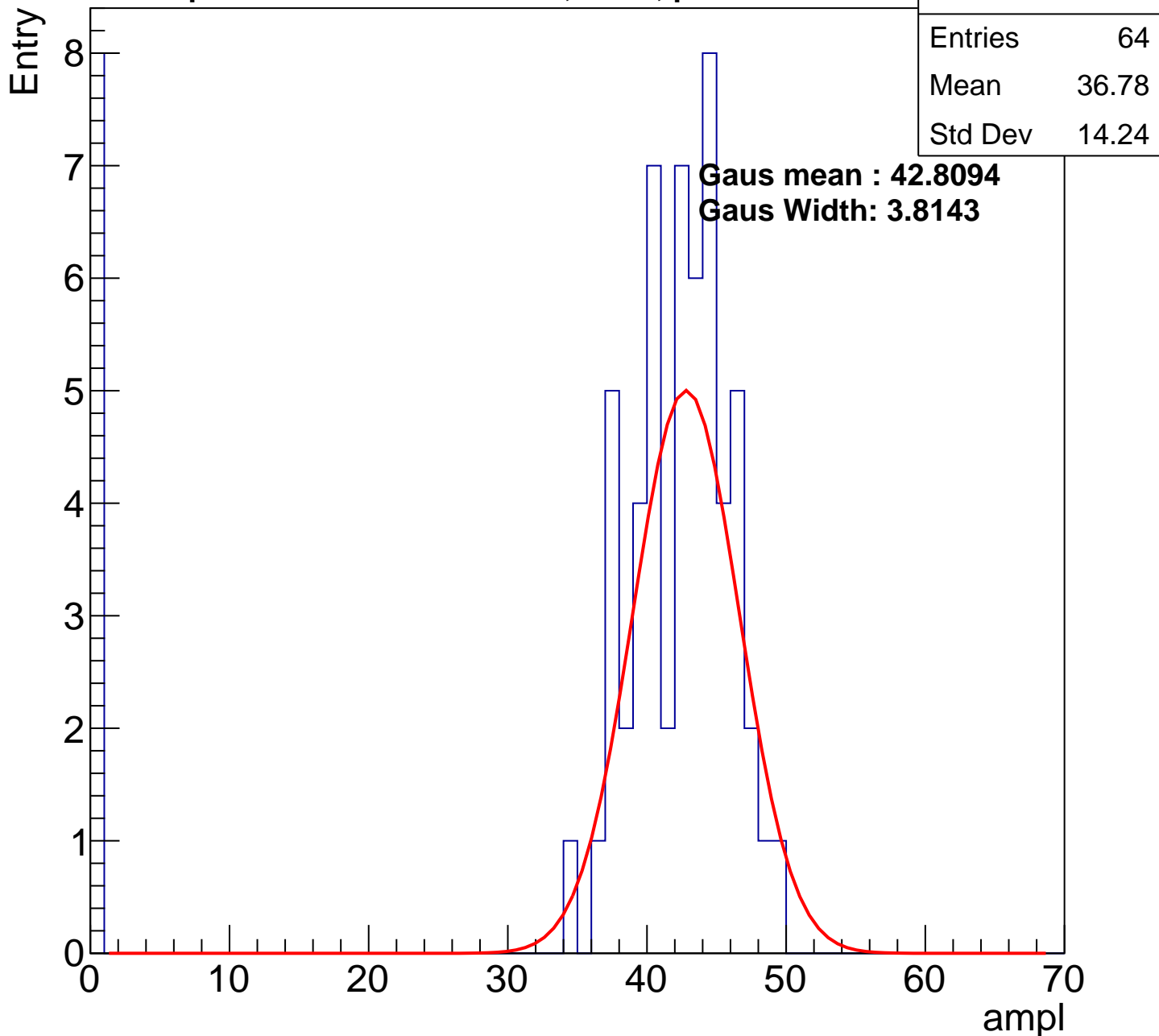
Gaus mean : 37.1773

Gaus Width: 3.3146



B1L103S, U7-ch84, adc2

calib_packv5_041523_1651.root, FC#0, port C2

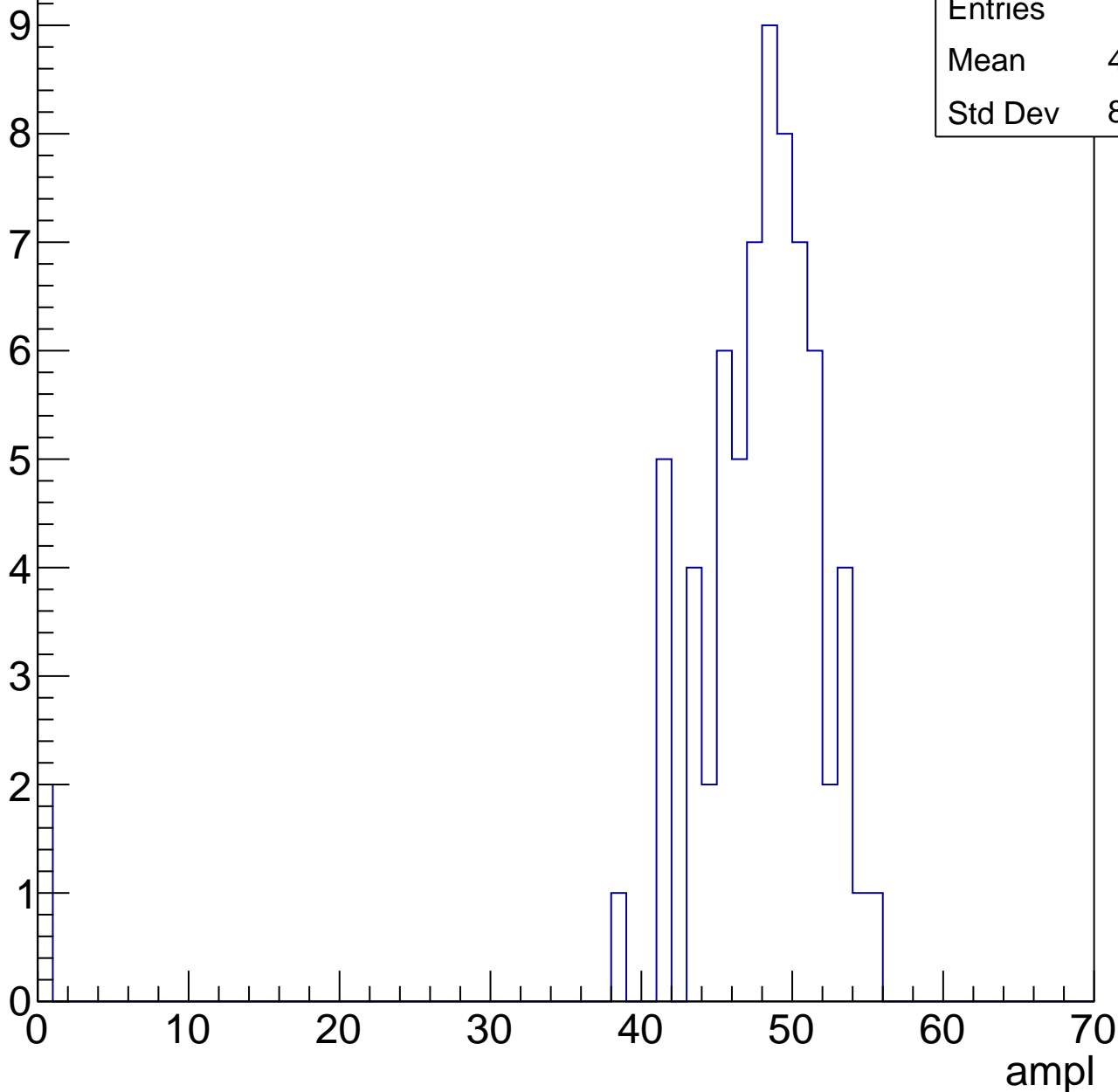


B1L103S, U7-ch84, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	46.24
Std Dev	8.666

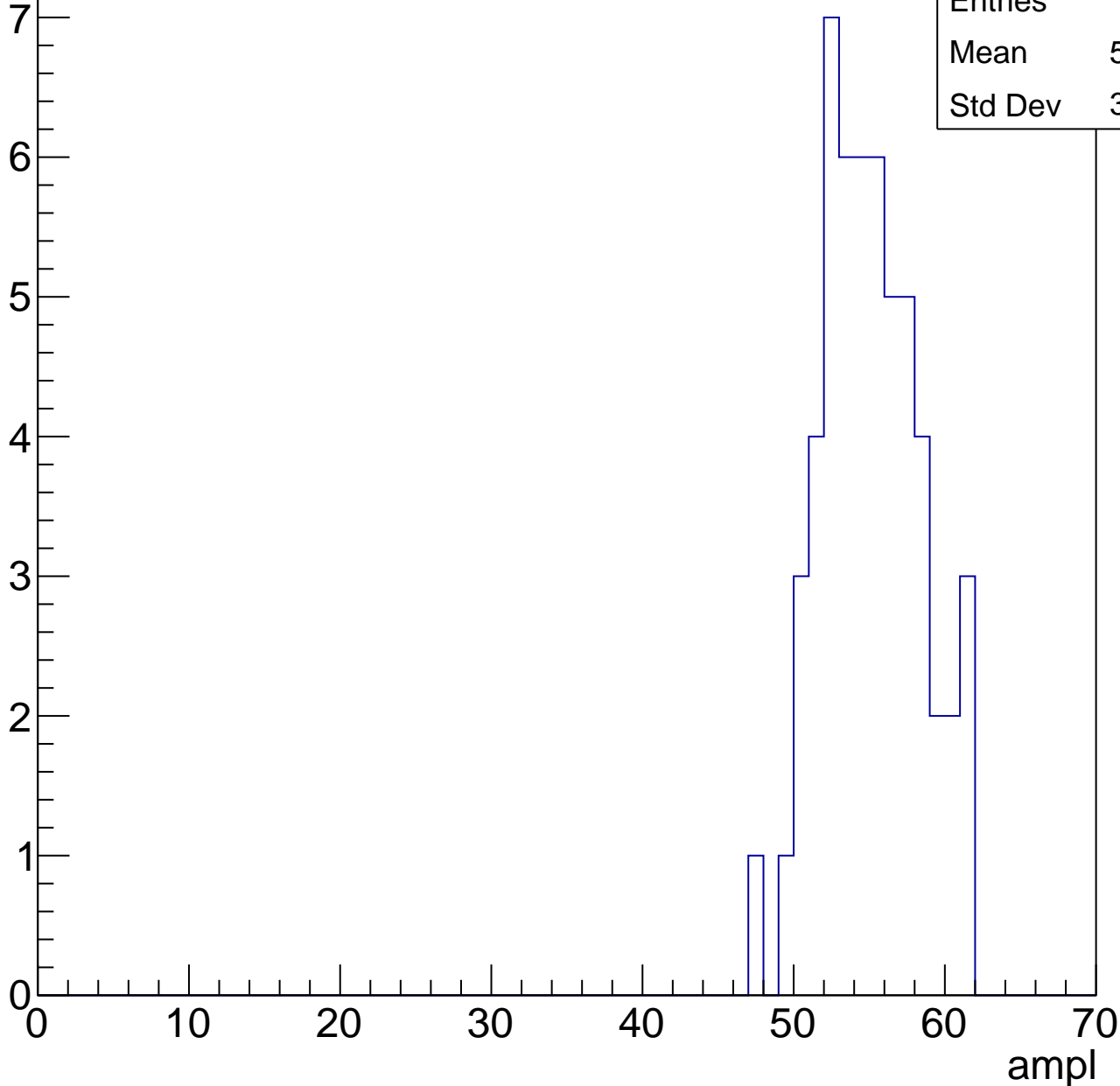


B1L103S, U7-ch84, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	54.62
Std Dev	3.233

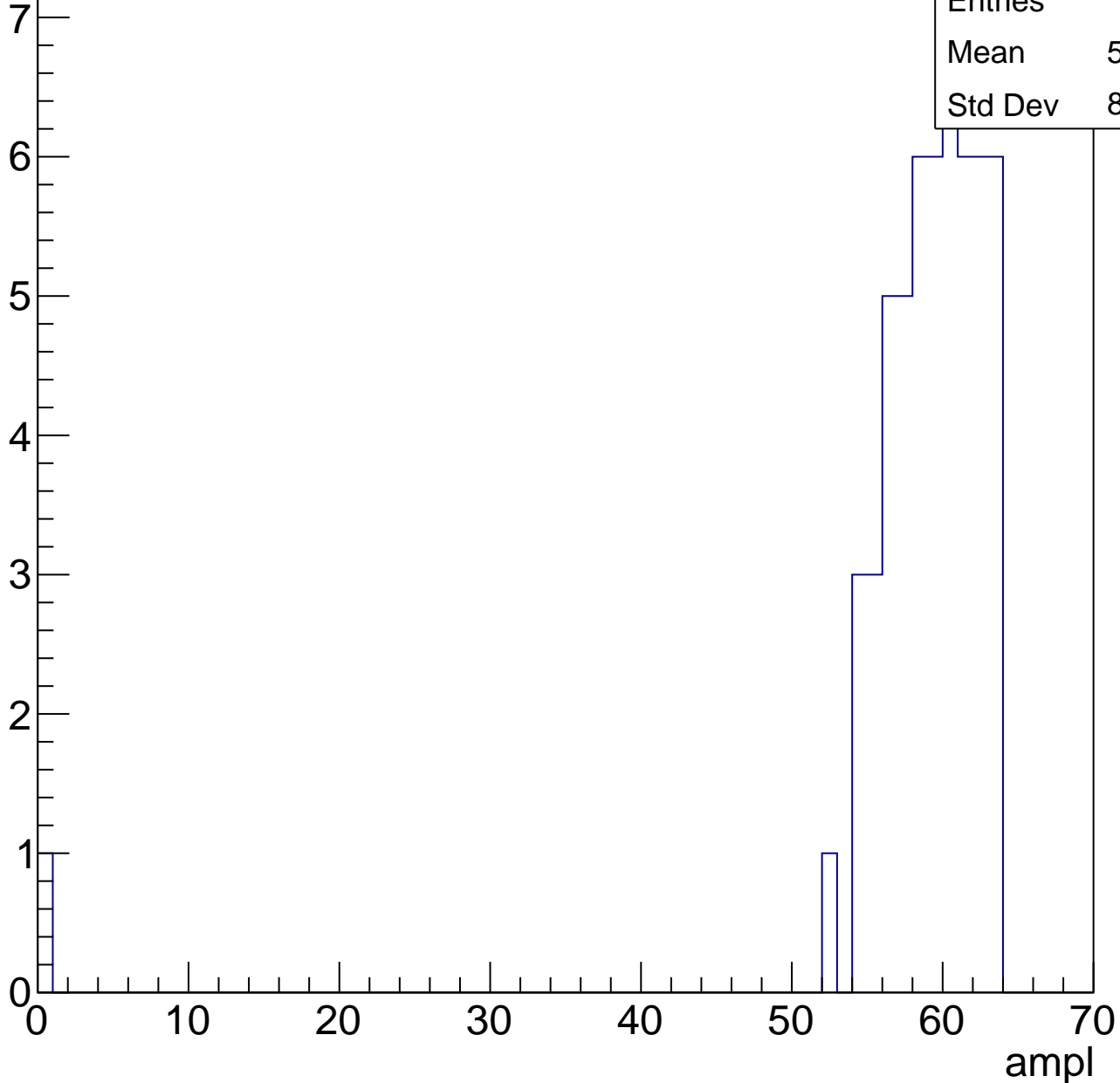


B1L103S, U7-ch84, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

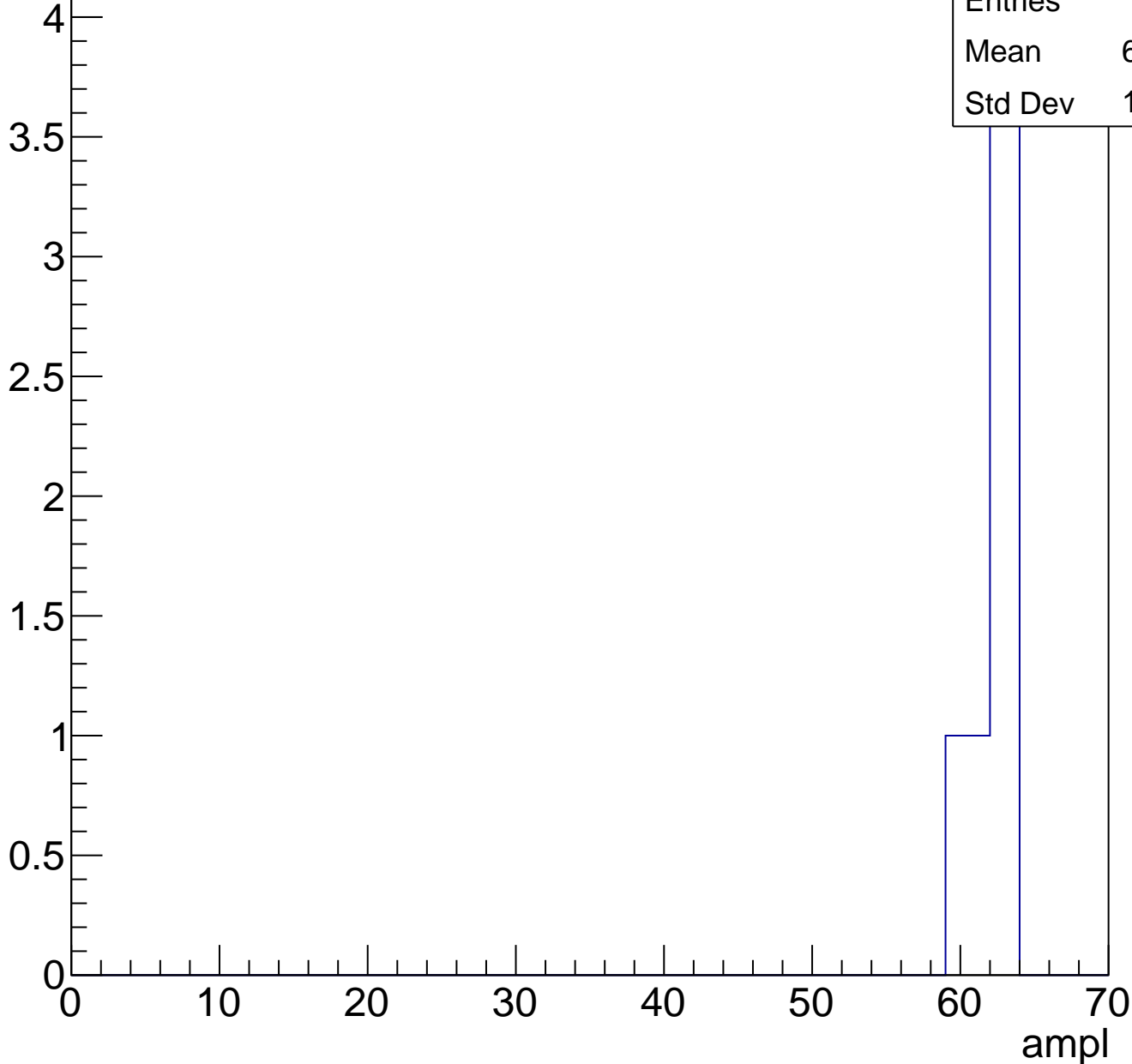
Entries	55
Mean	57.85
Std Dev	8.348



B1L103S, U7-ch84, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

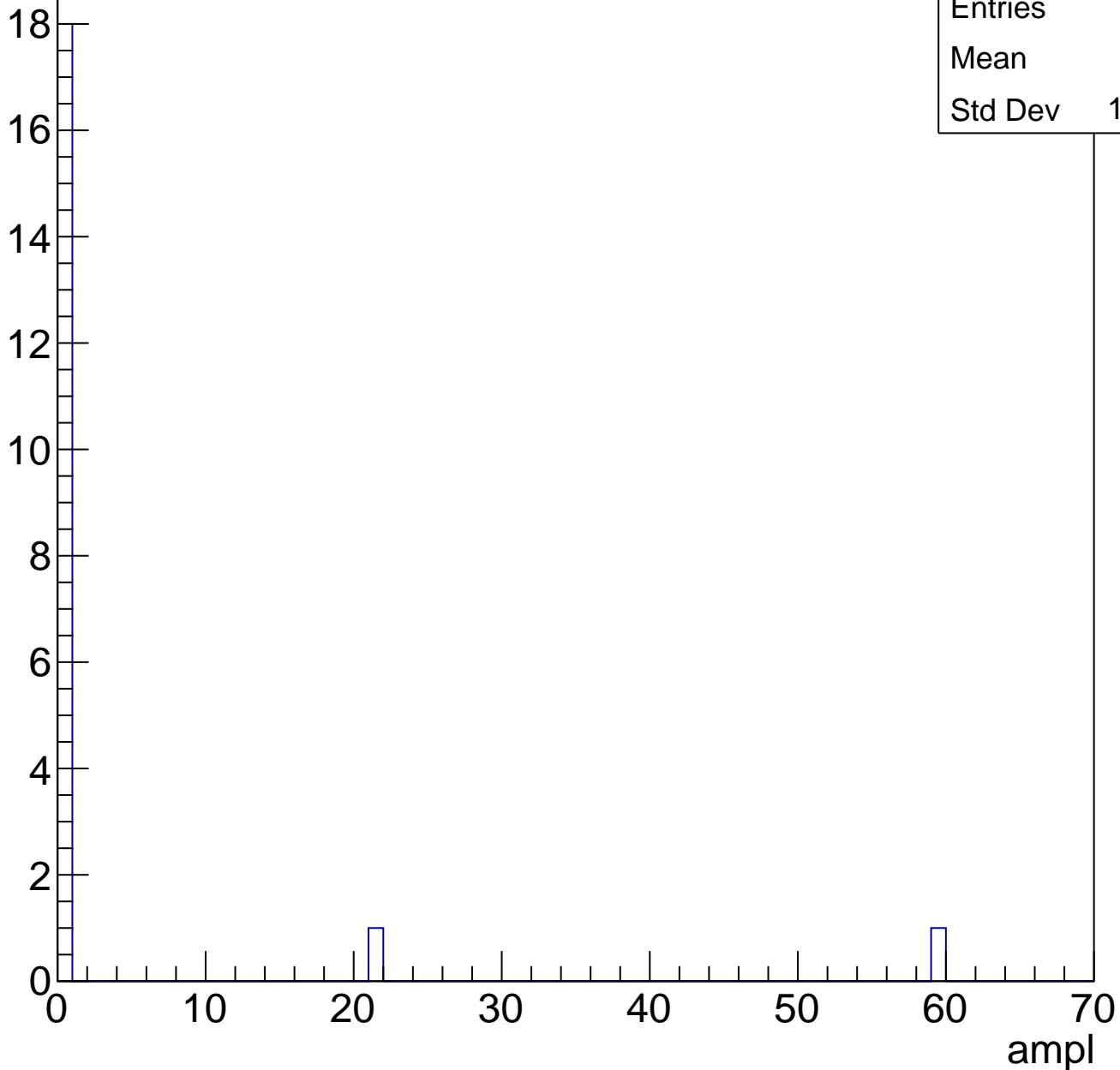


B1L103S, U7-ch84, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	4
Std Dev	13.42

Entry



B1L103S, U7-ch85, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	90
Mean	24.84
Std Dev	10.68

Gaus mean : 29.4538

Gaus Width: 3.7668

Entry

12

10

8

6

4

2

0

0

10

20

30

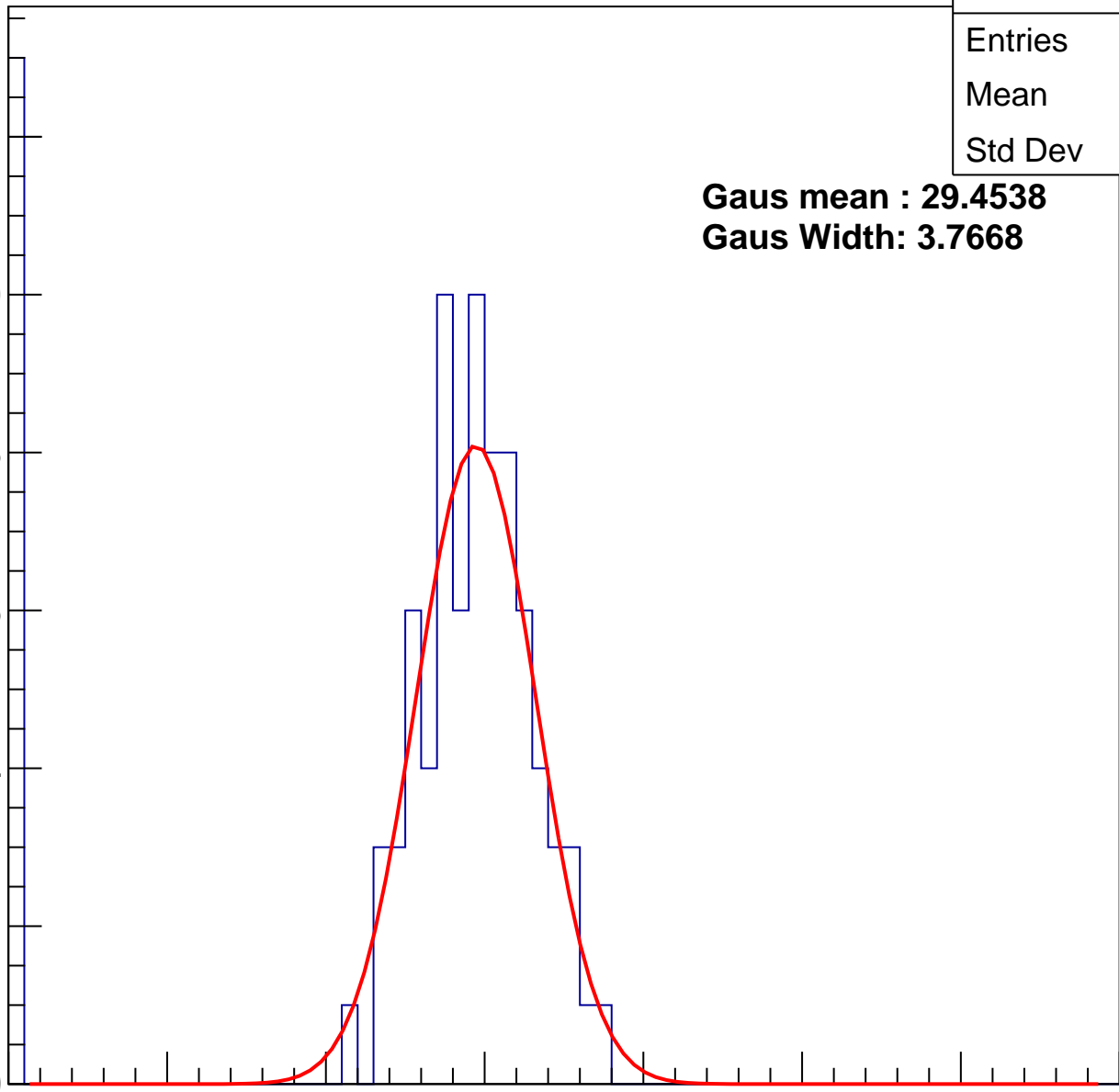
40

50

60

70

ampl



B1L103S, U7-ch85, adc1

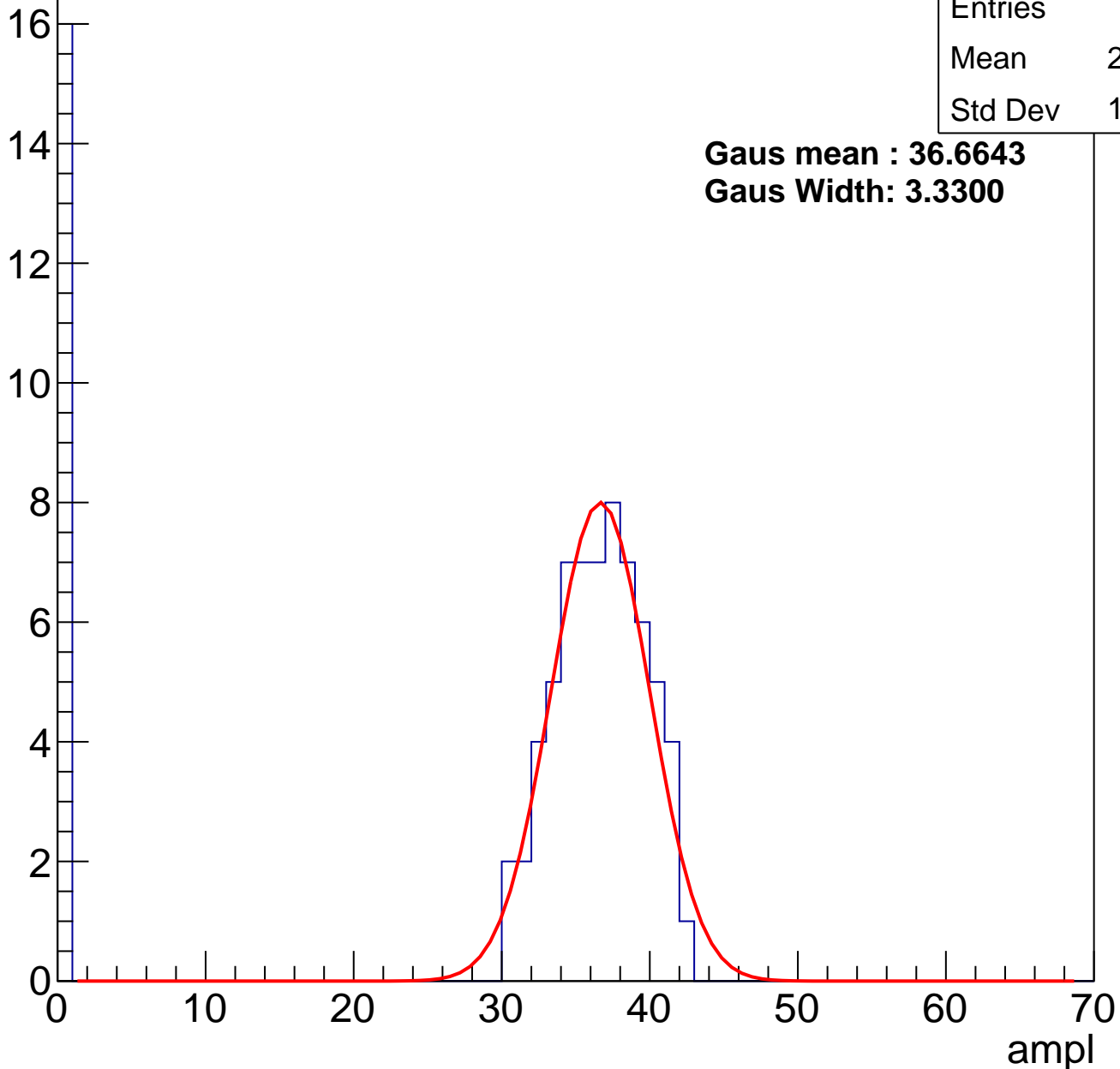
calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	29.04
Std Dev	14.65

Gaus mean : 36.6643

Gaus Width: 3.3300

Entry



B1L103S, U7-ch85, adc2

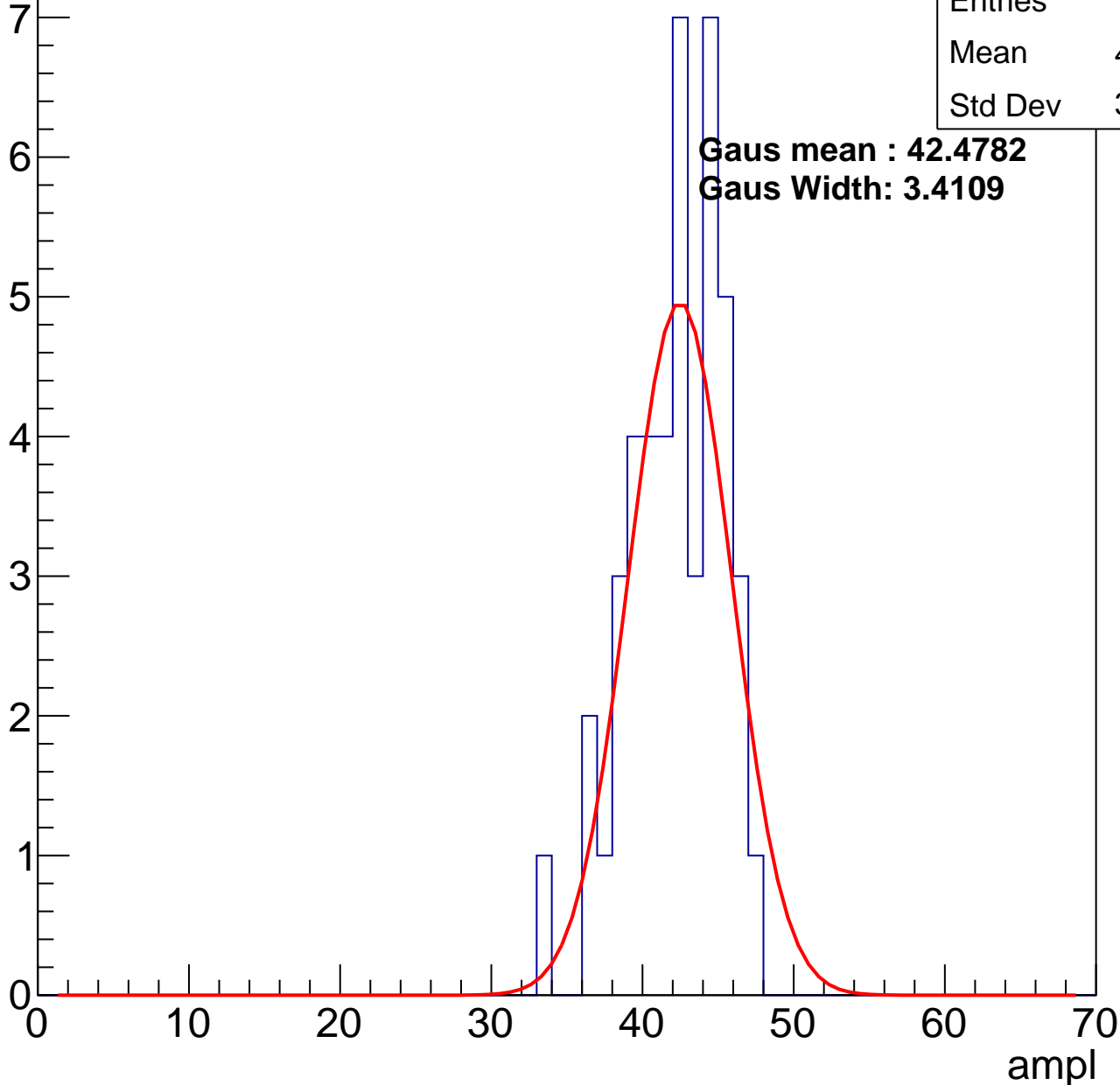
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	45
Mean	41.71
Std Dev	3.081

Gaus mean : 42.4782

Gaus Width: 3.4109

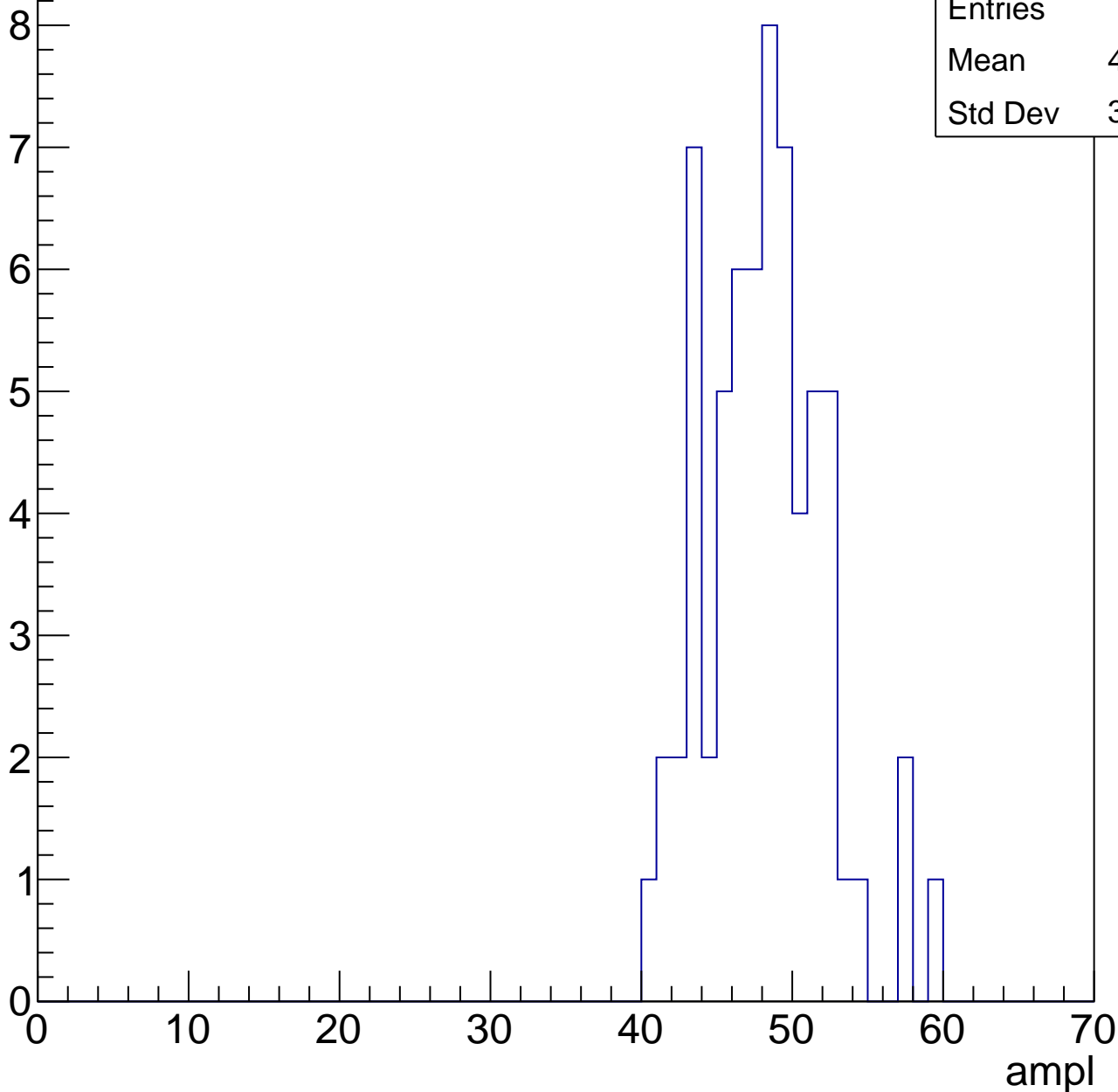


B1L103S, U7-ch85, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	47.69
Std Dev	3.926

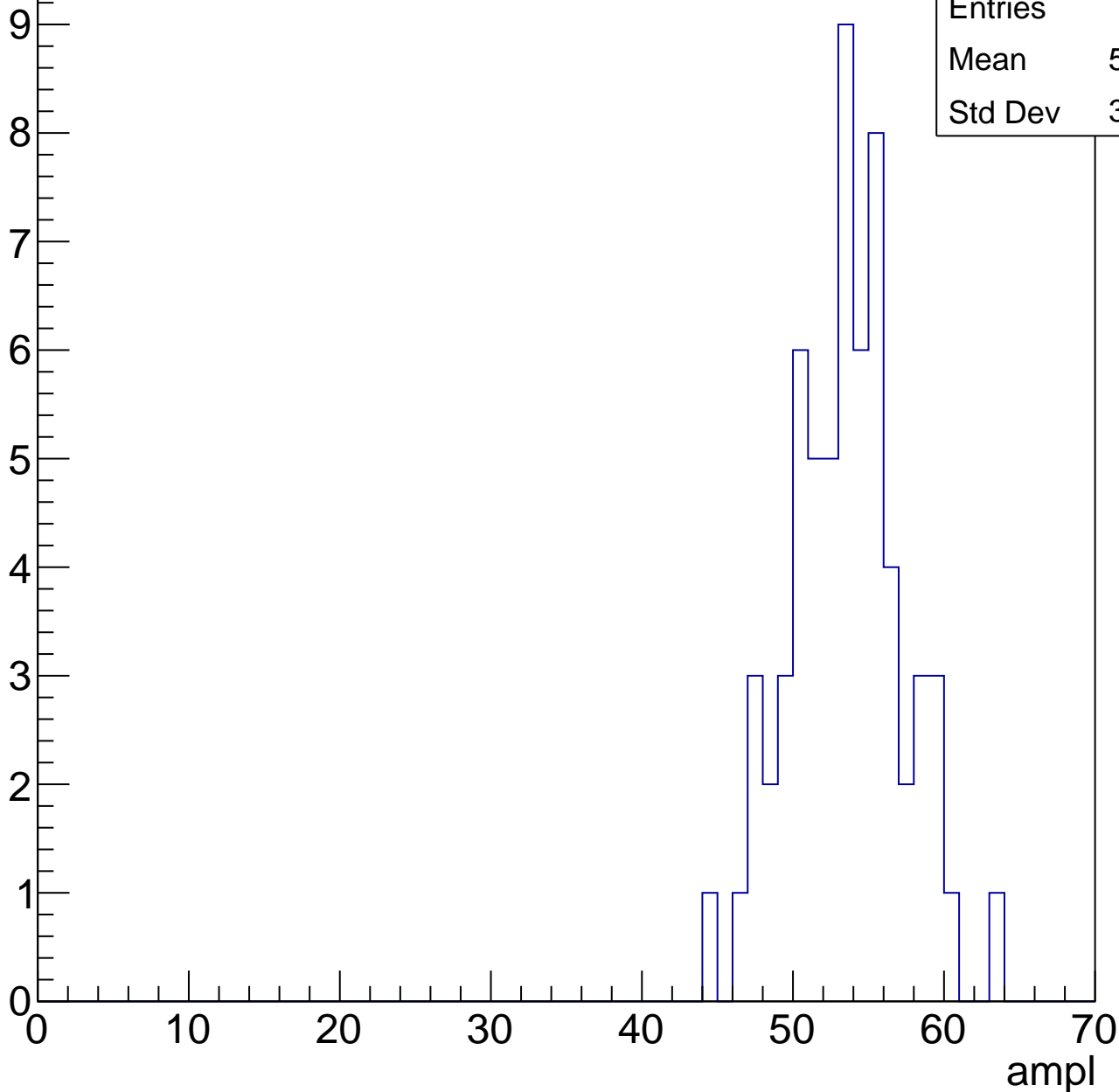


B1L103S, U7-ch85, adc4

calib_packv5_041523_1651.root, FC#0, port C2

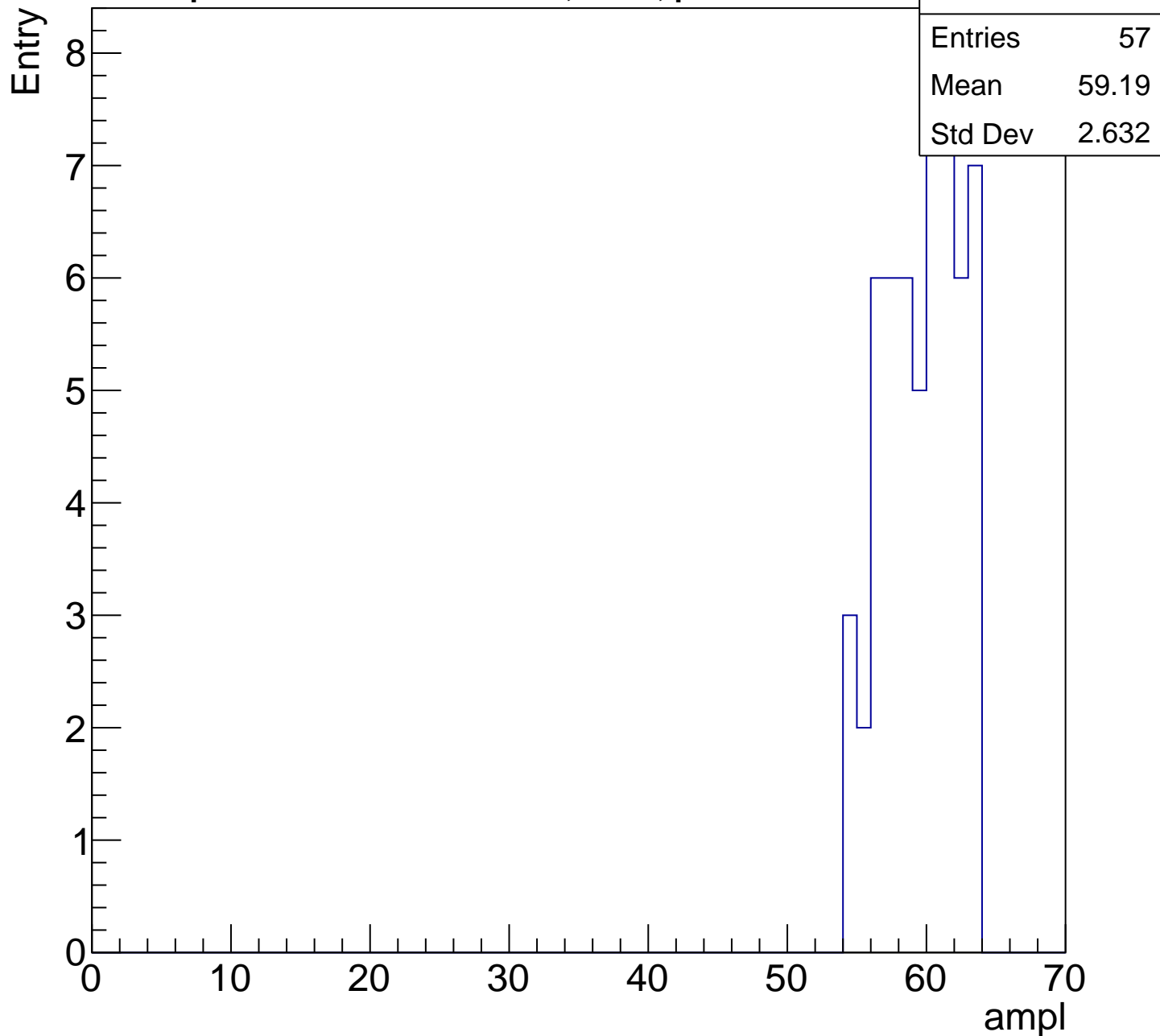
Entry

Entries	63
Mean	53.05
Std Dev	3.679



B1L103S, U7-ch85, adc5

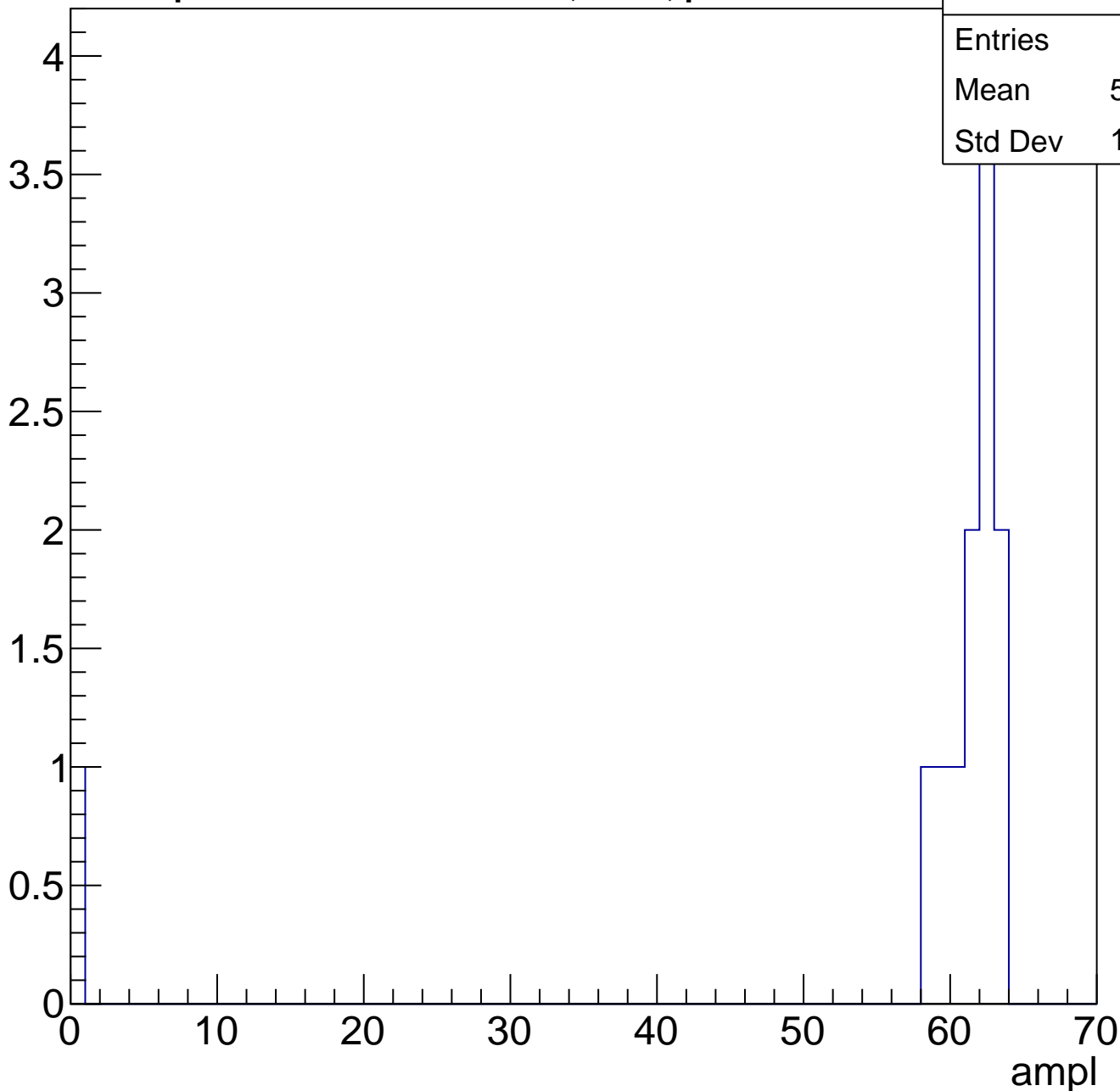
calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U7-ch85, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	12
Mean	56.08
Std Dev	16.97

B1L103S, U7-ch85, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

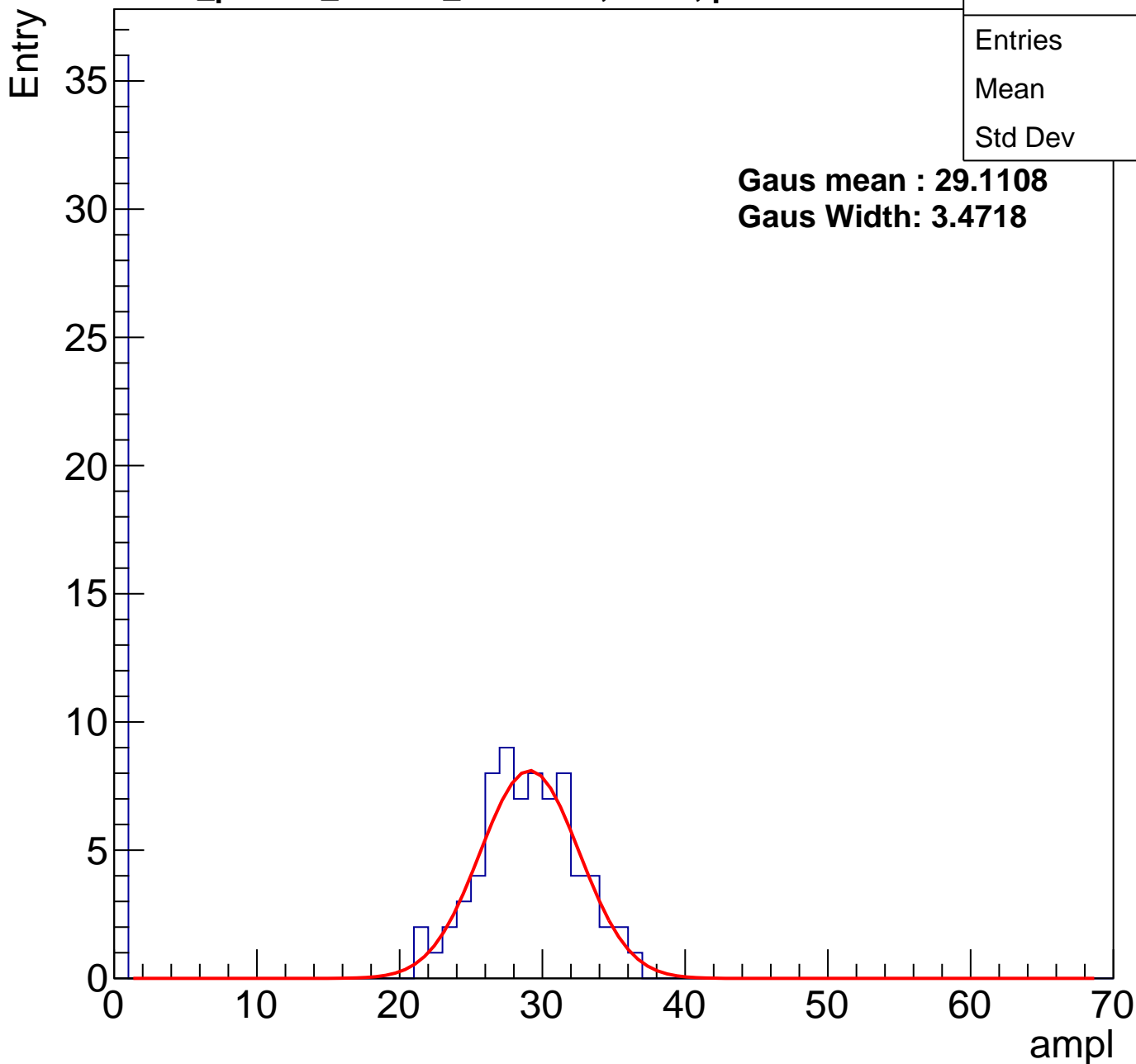
B1L103S, U7-ch86, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	108
Mean	19.01
Std Dev	13.71

Gaus mean : 29.1108

Gaus Width: 3.4718



B1L103S, U7-ch86, adc1

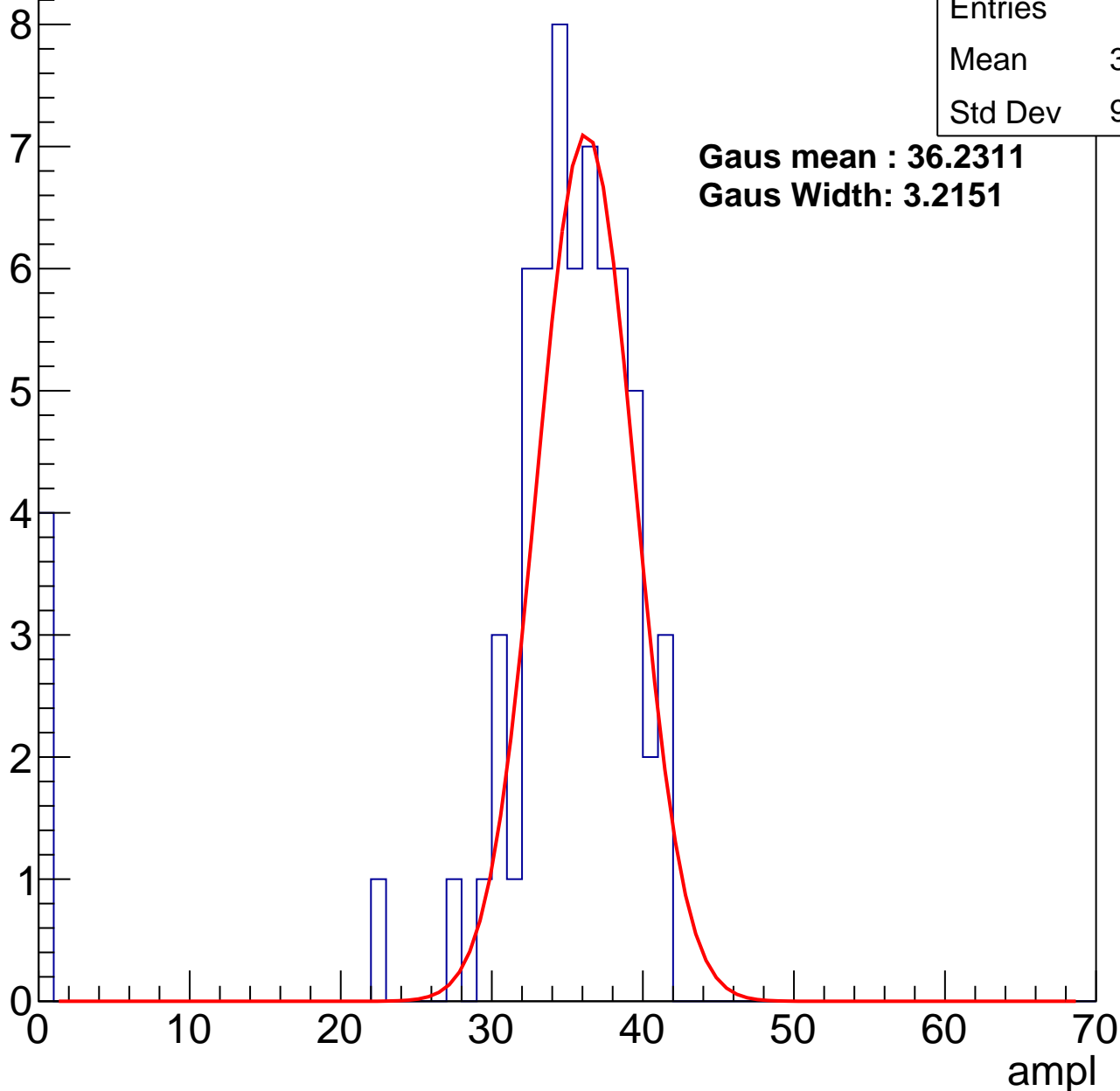
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	32.89
Std Dev	9.025

Gaus mean : 36.2311

Gaus Width: 3.2151



B1L103S, U7-ch86, adc2

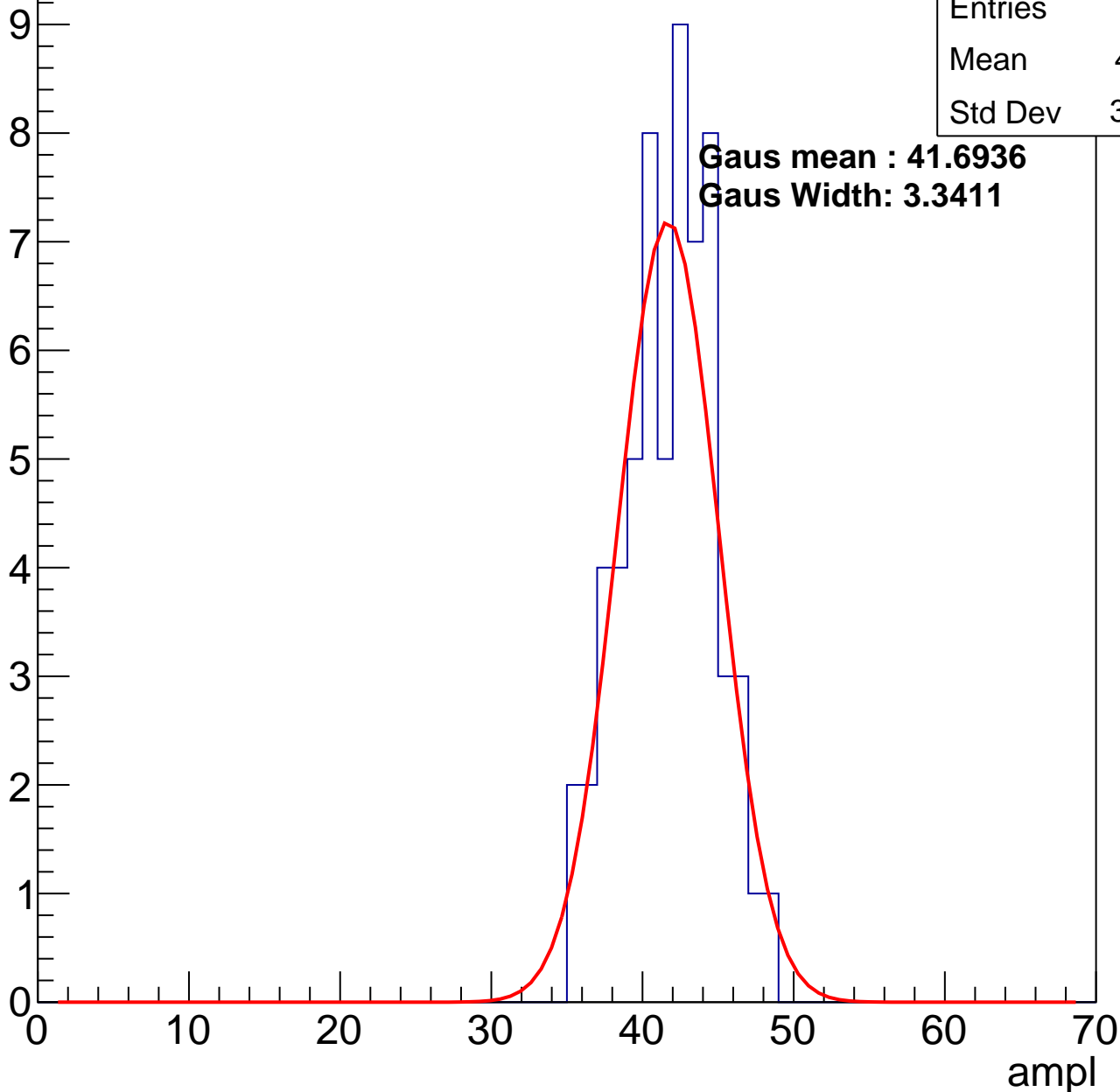
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	41.31
Std Dev	3.009

Gaus mean : 41.6936

Gaus Width: 3.3411

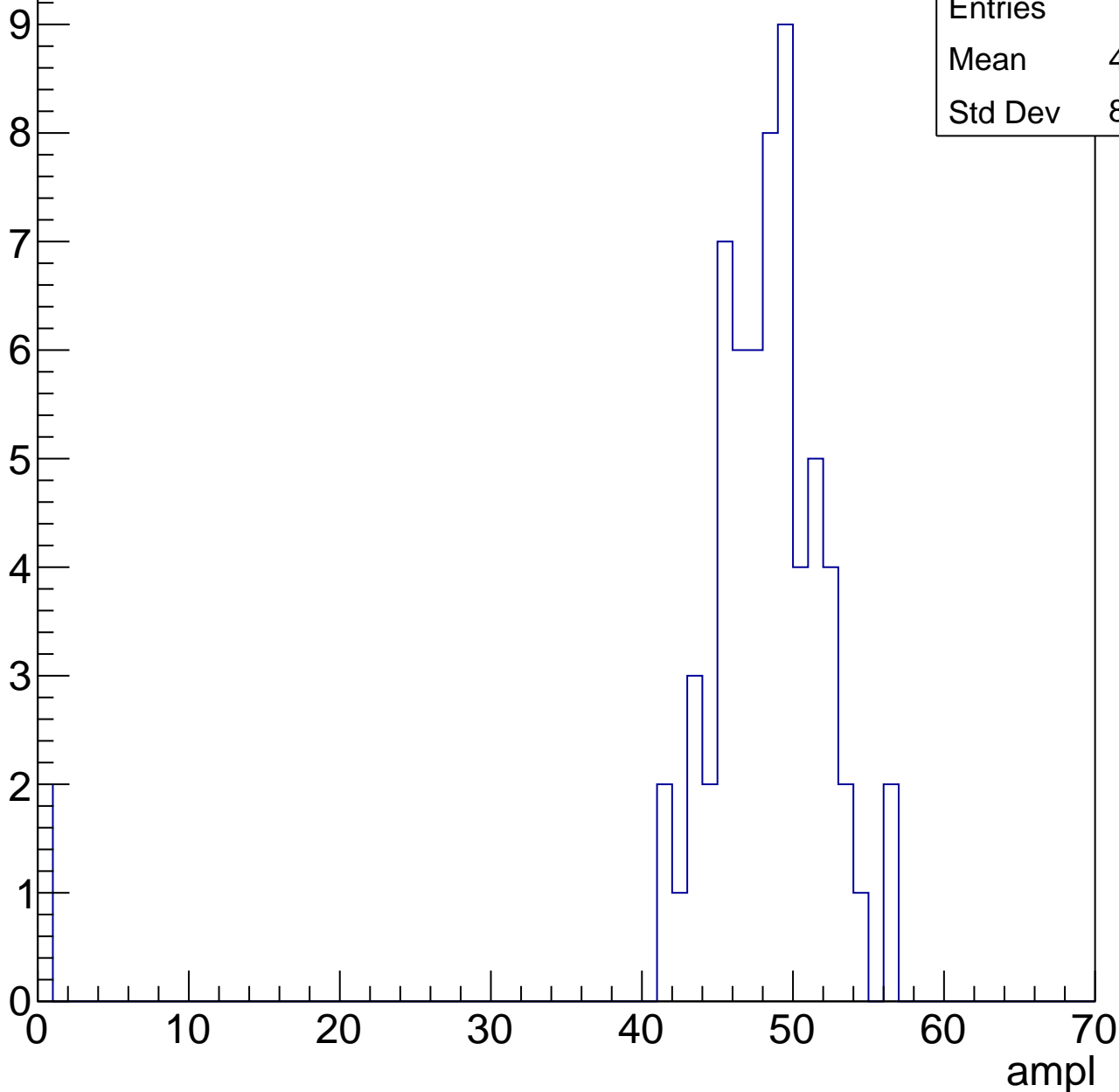


B1L103S, U7-ch86, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	64
Mean	46.47
Std Dev	8.962

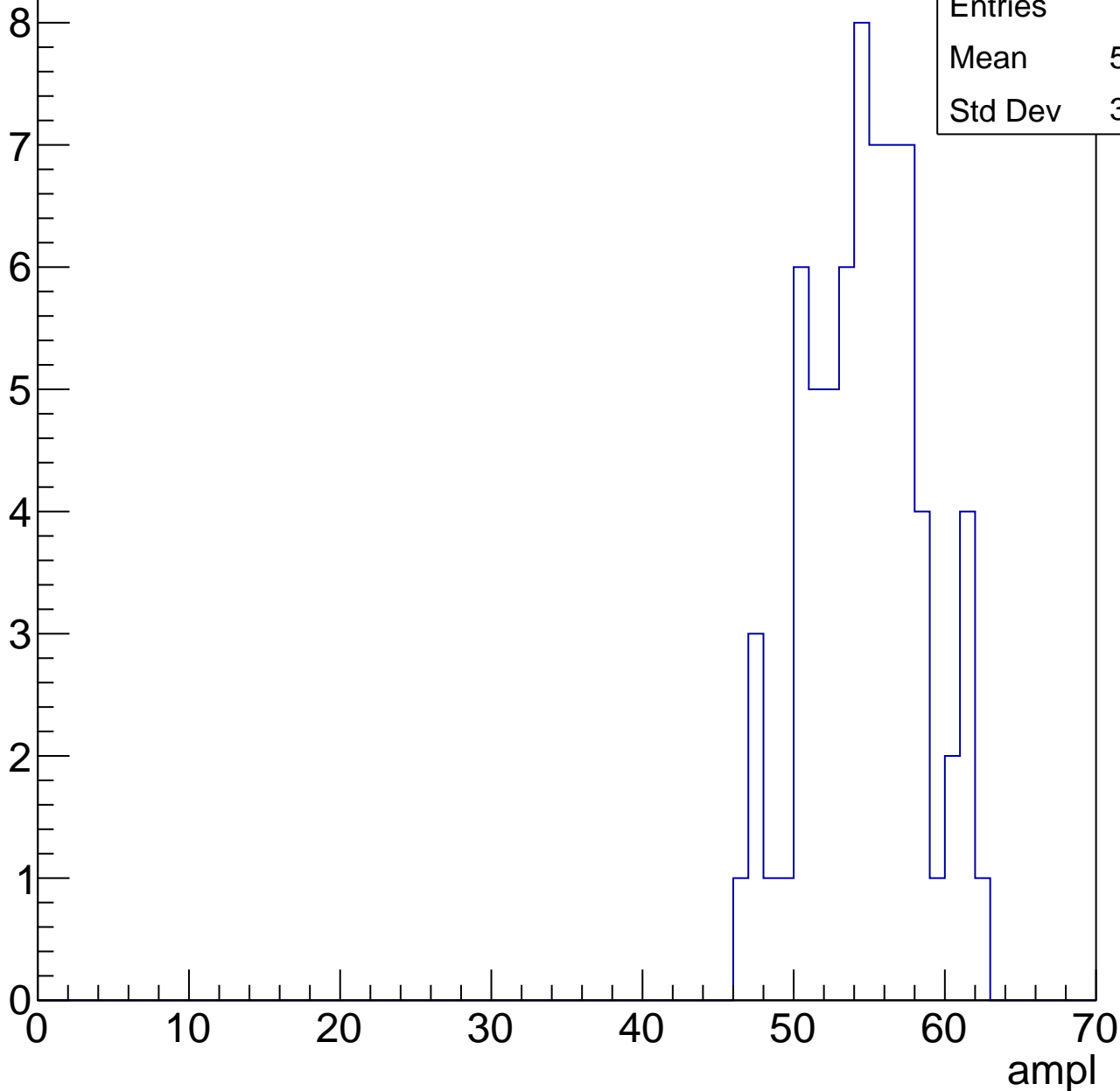


B1L103S, U7-ch86, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

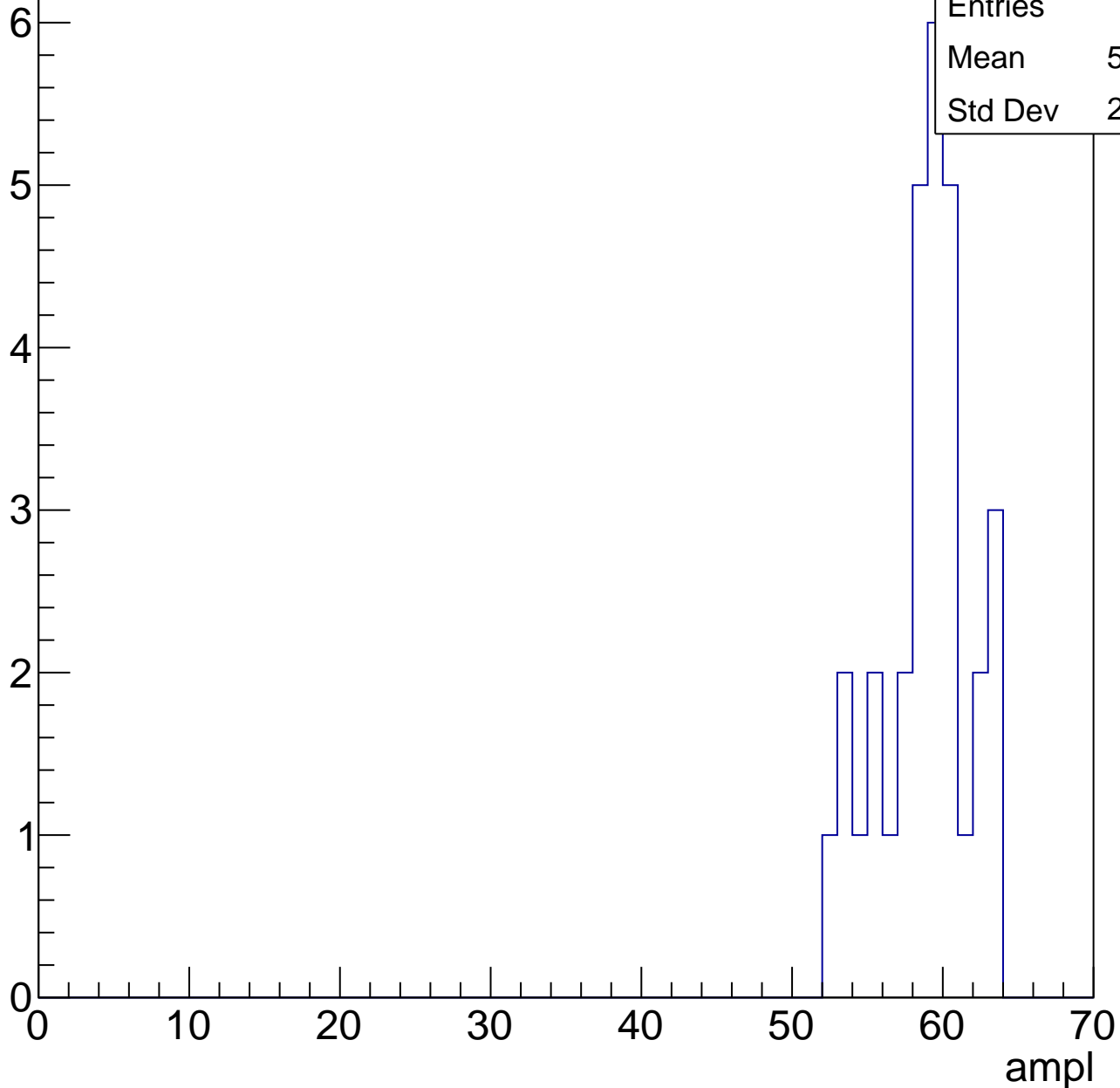
Entries	69
Mean	54.23
Std Dev	3.719



B1L103S, U7-ch86, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



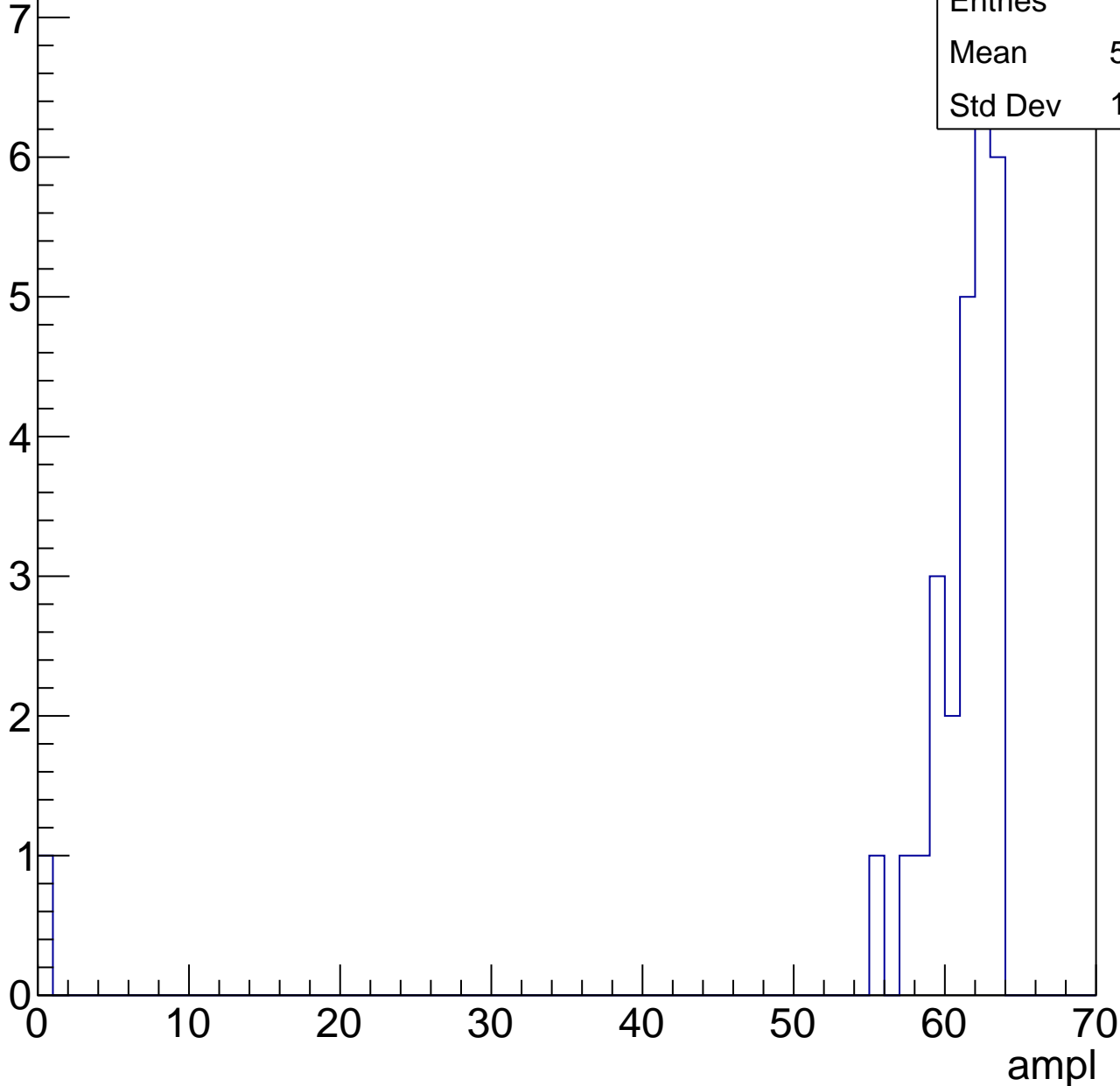
Entries	31
Mean	58.39
Std Dev	2.915

B1L103S, U7-ch86, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

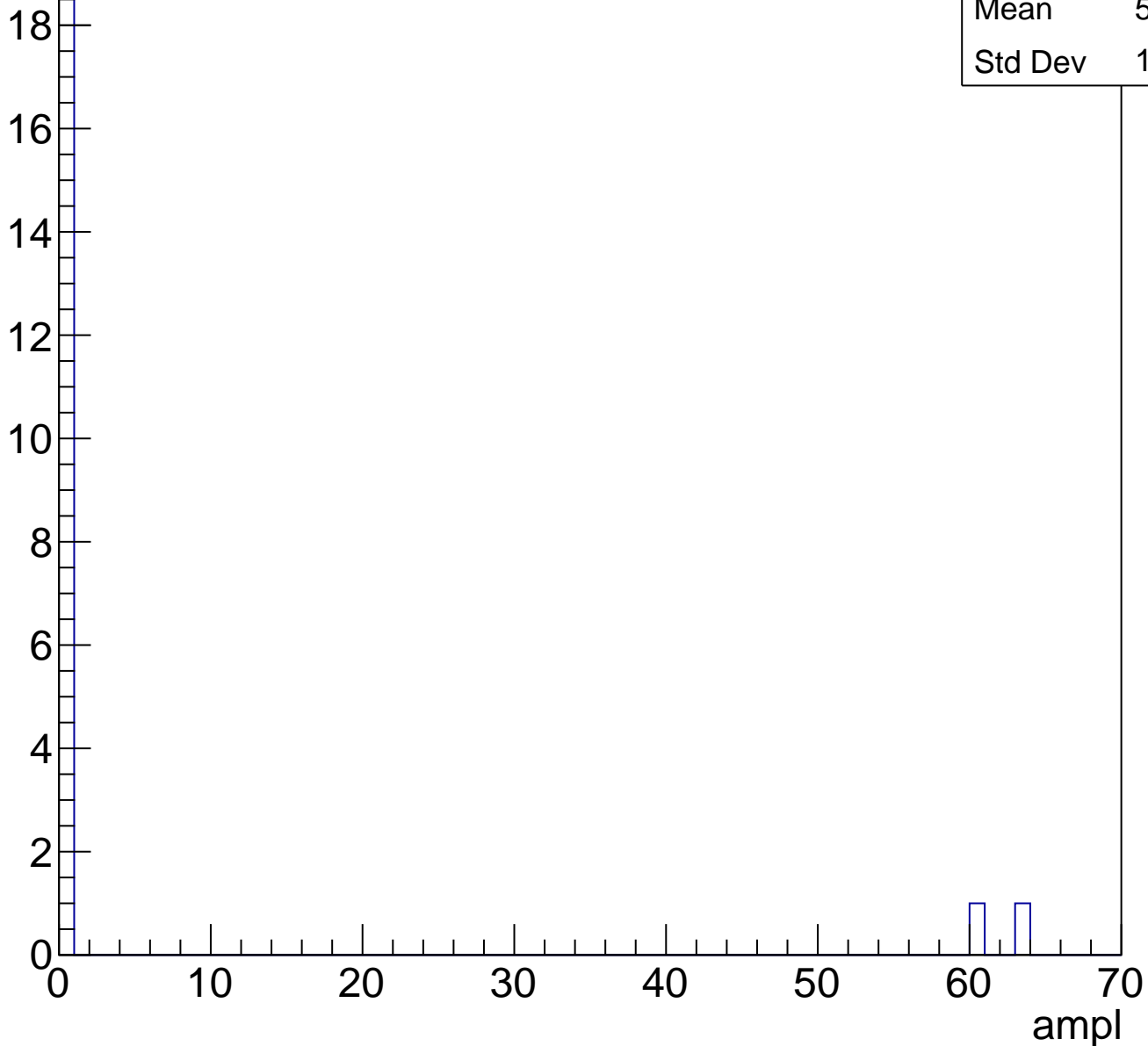
Entries	27
Mean	58.67
Std Dev	11.67



B1L103S, U7-ch86, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	21
Mean	5.857
Std Dev	18.06

B1L103S, U7-ch87, adc0

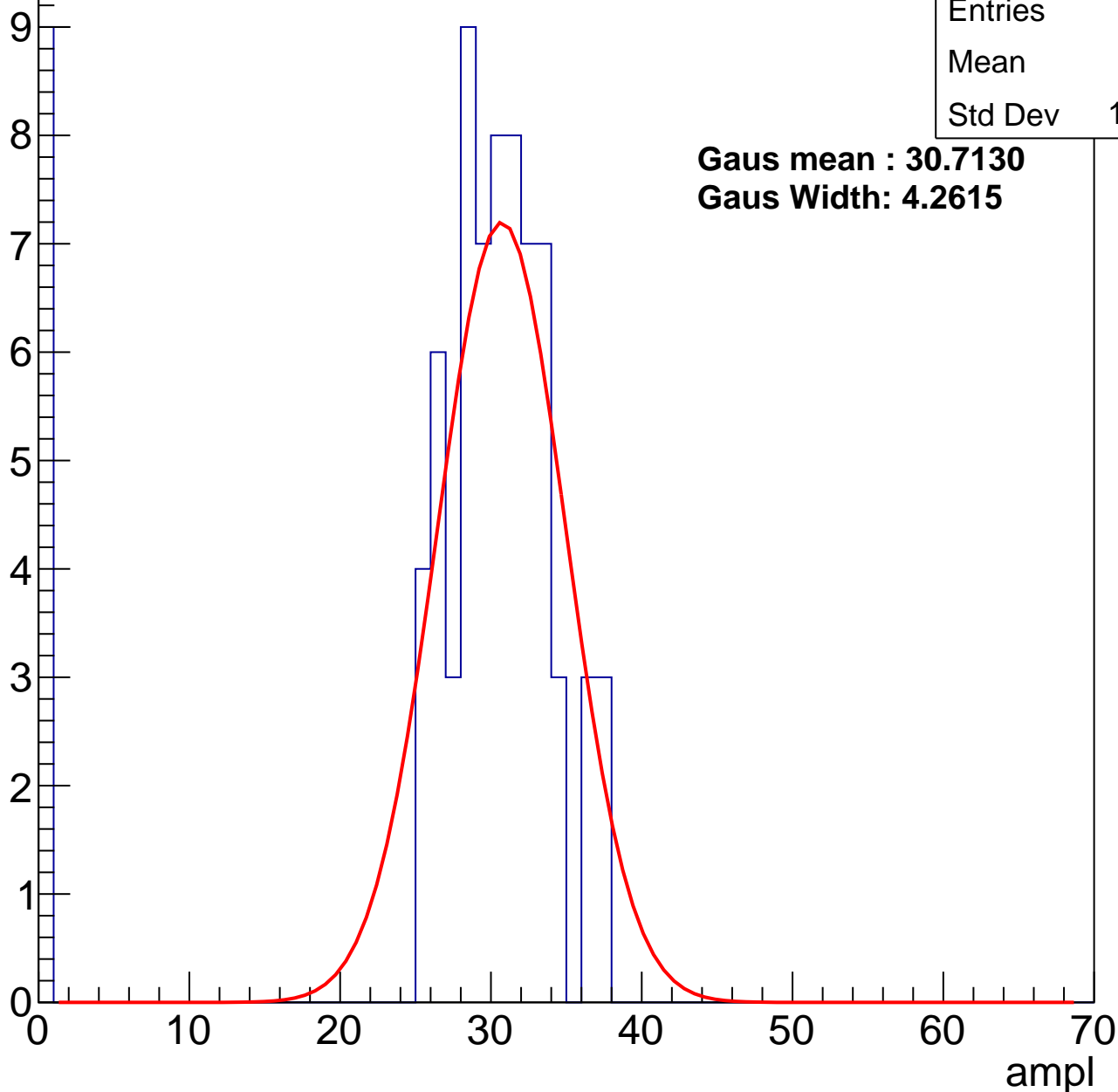
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	26.7
Std Dev	10.15

Gaus mean : 30.7130

Gaus Width: 4.2615



B1L103S, U7-ch87, adc1

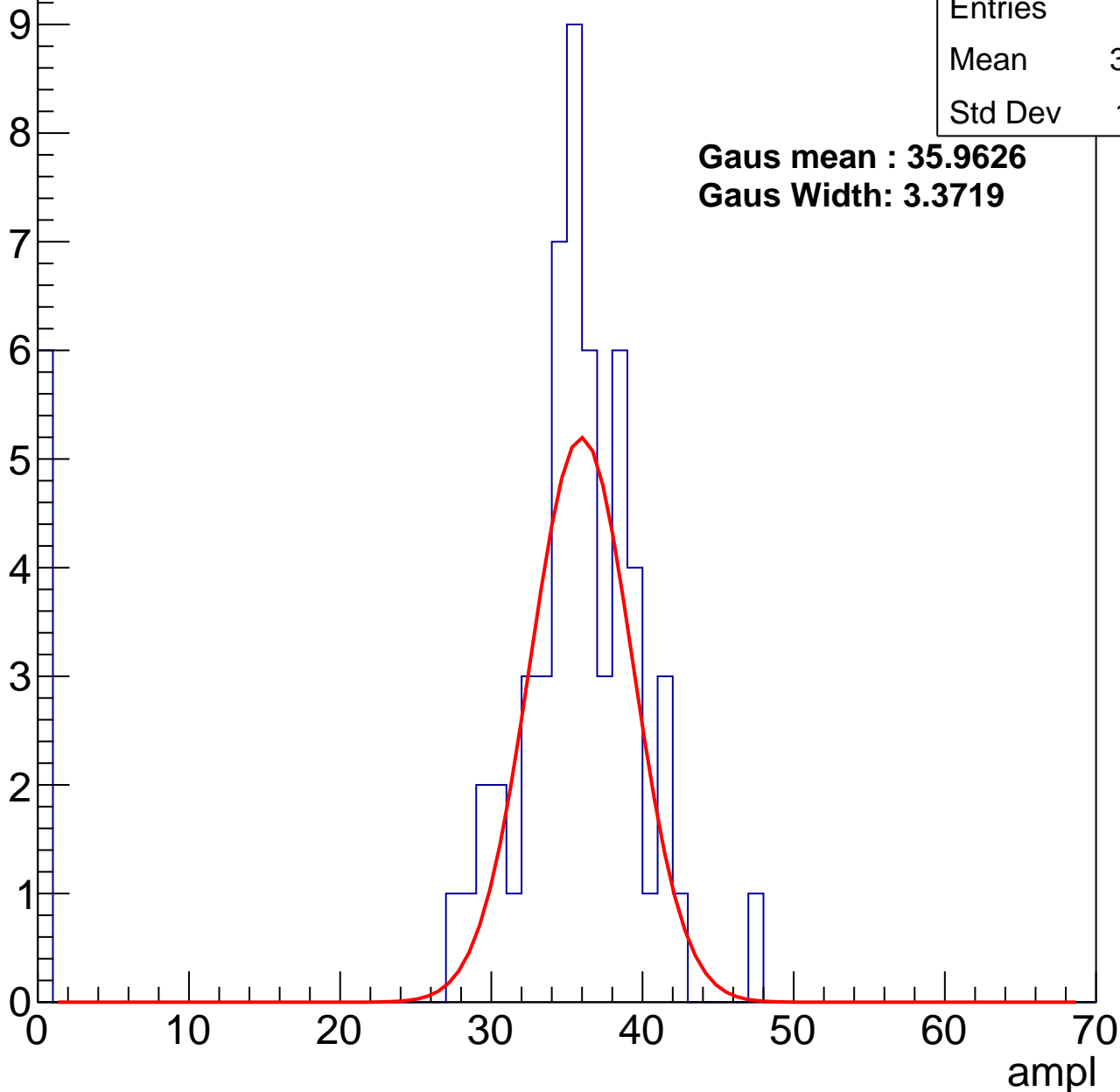
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	31.92
Std Dev	11.21

Gaus mean : 35.9626

Gaus Width: 3.3719



B1L103S, U7-ch87, adc2

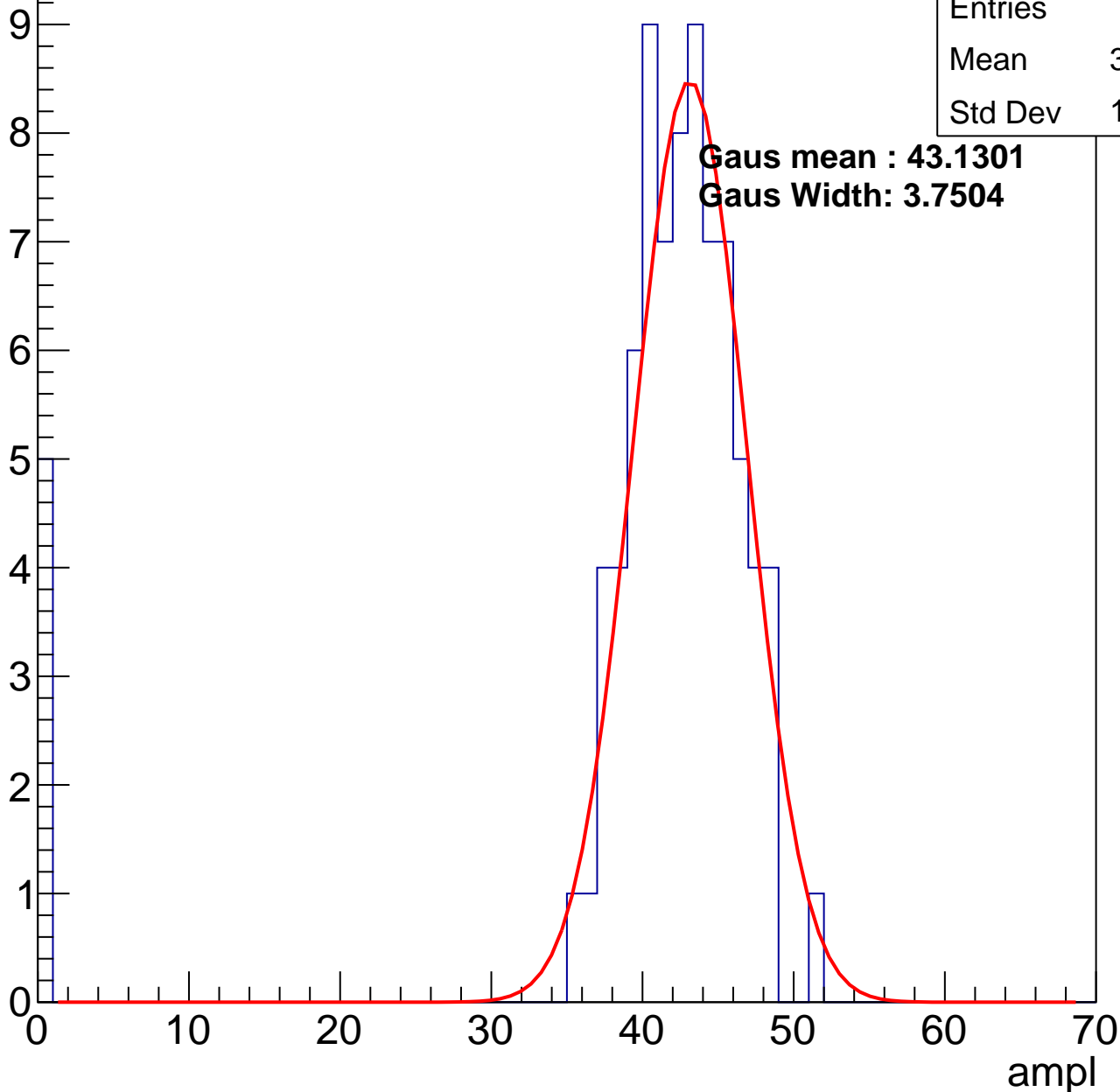
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	82
Mean	39.74
Std Dev	10.62

Gaus mean : 43.1301

Gaus Width: 3.7504

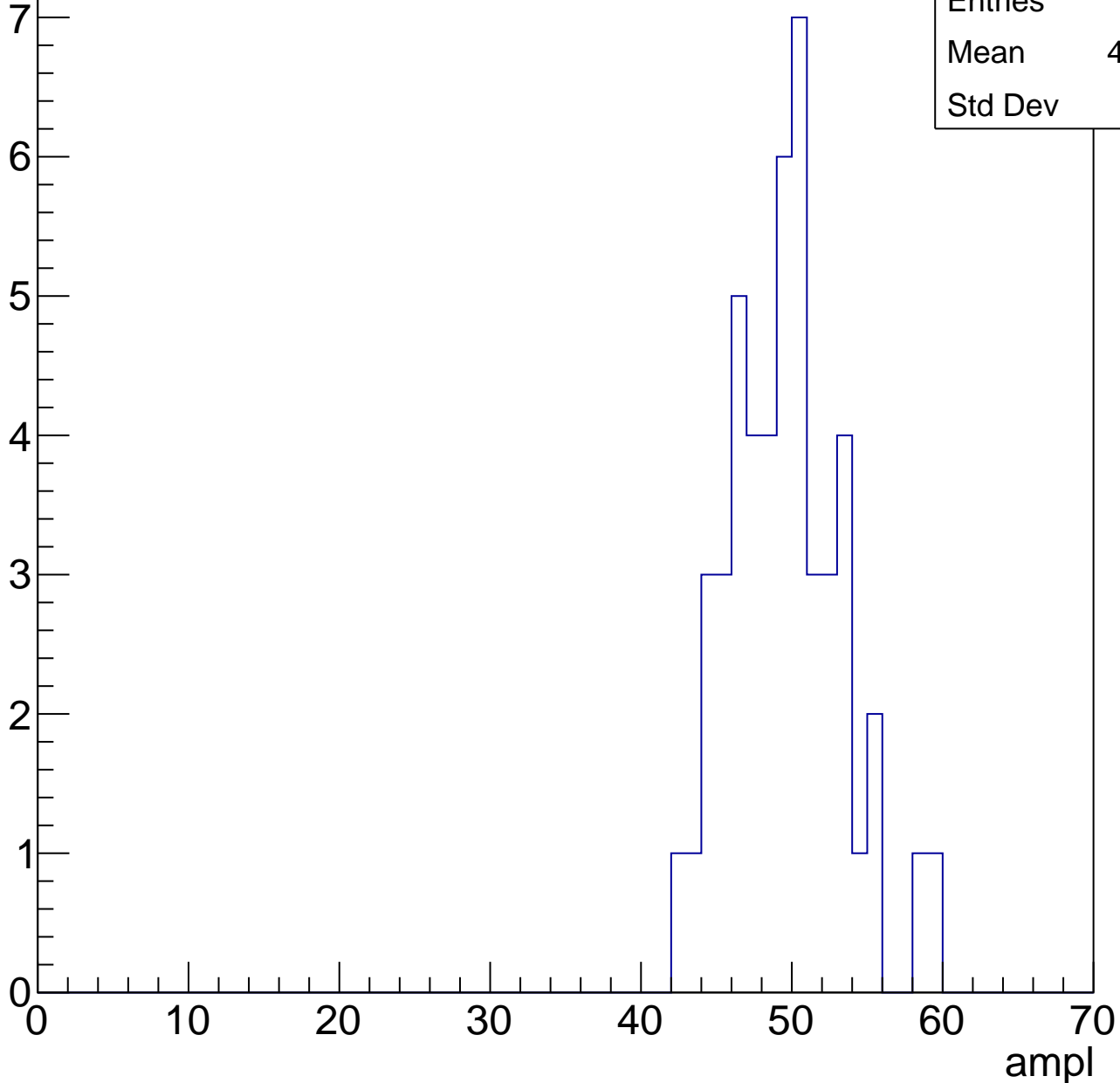


B1L103S, U7-ch87, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	49.14
Std Dev	3.67

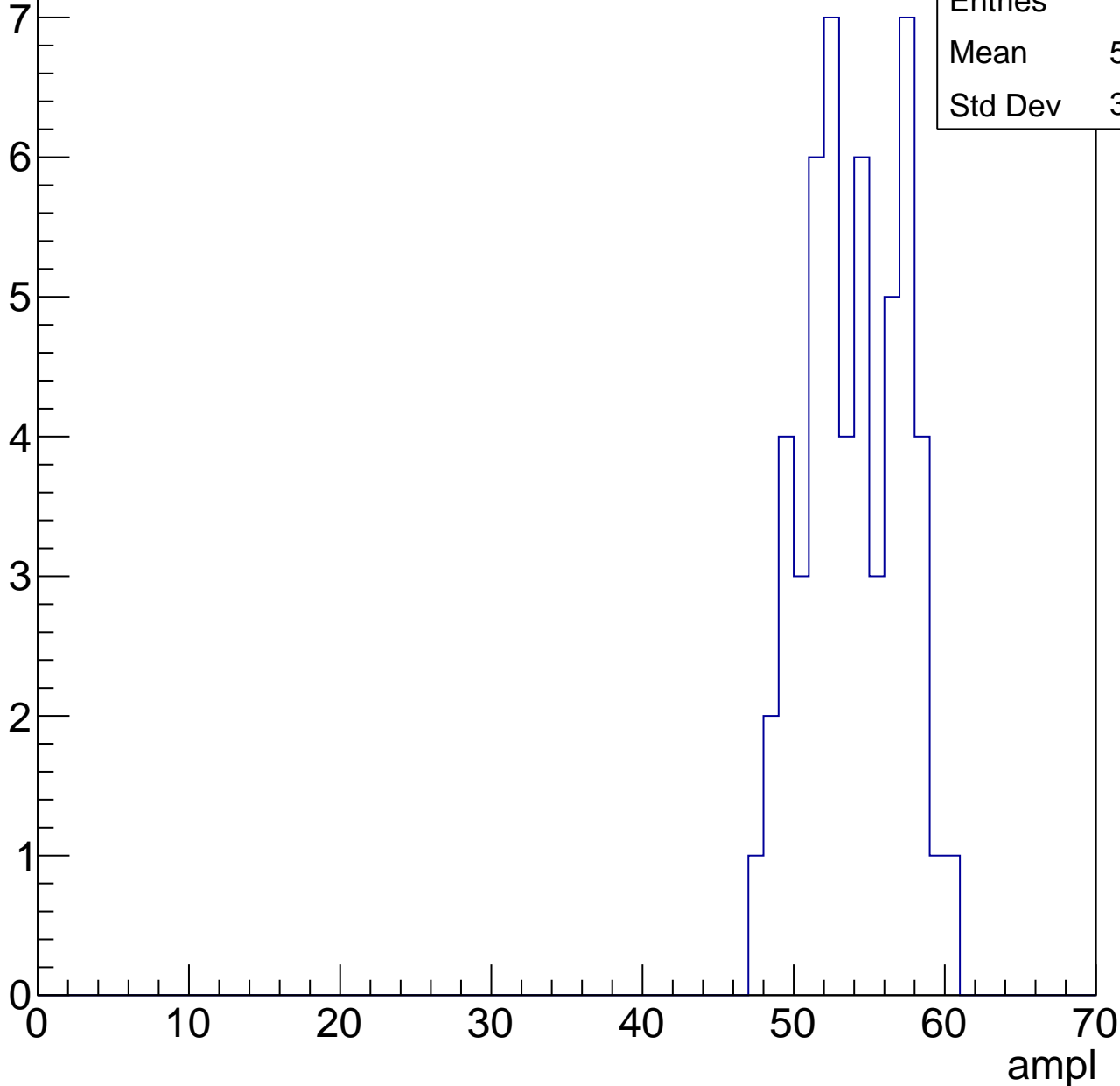


B1L103S, U7-ch87, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	54
Mean	53.52
Std Dev	3.202



B1L103S, U7-ch87, adc5

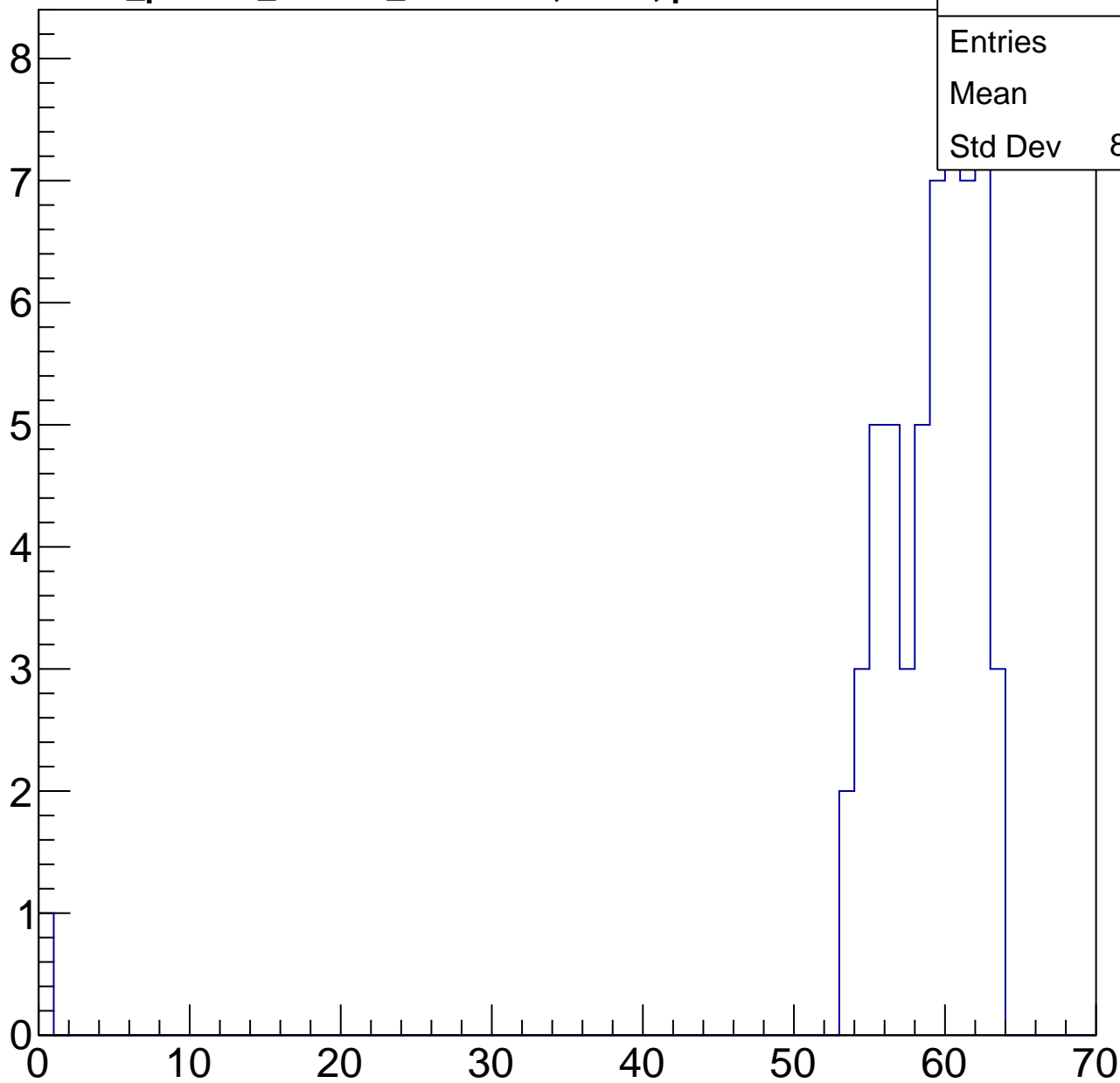
calib_packv5_041523_1651.root, FC#0, port C2

Entry

8
7
6
5
4
3
2
1
0

Entries	57
Mean	57.7
Std Dev	8.197

ampl

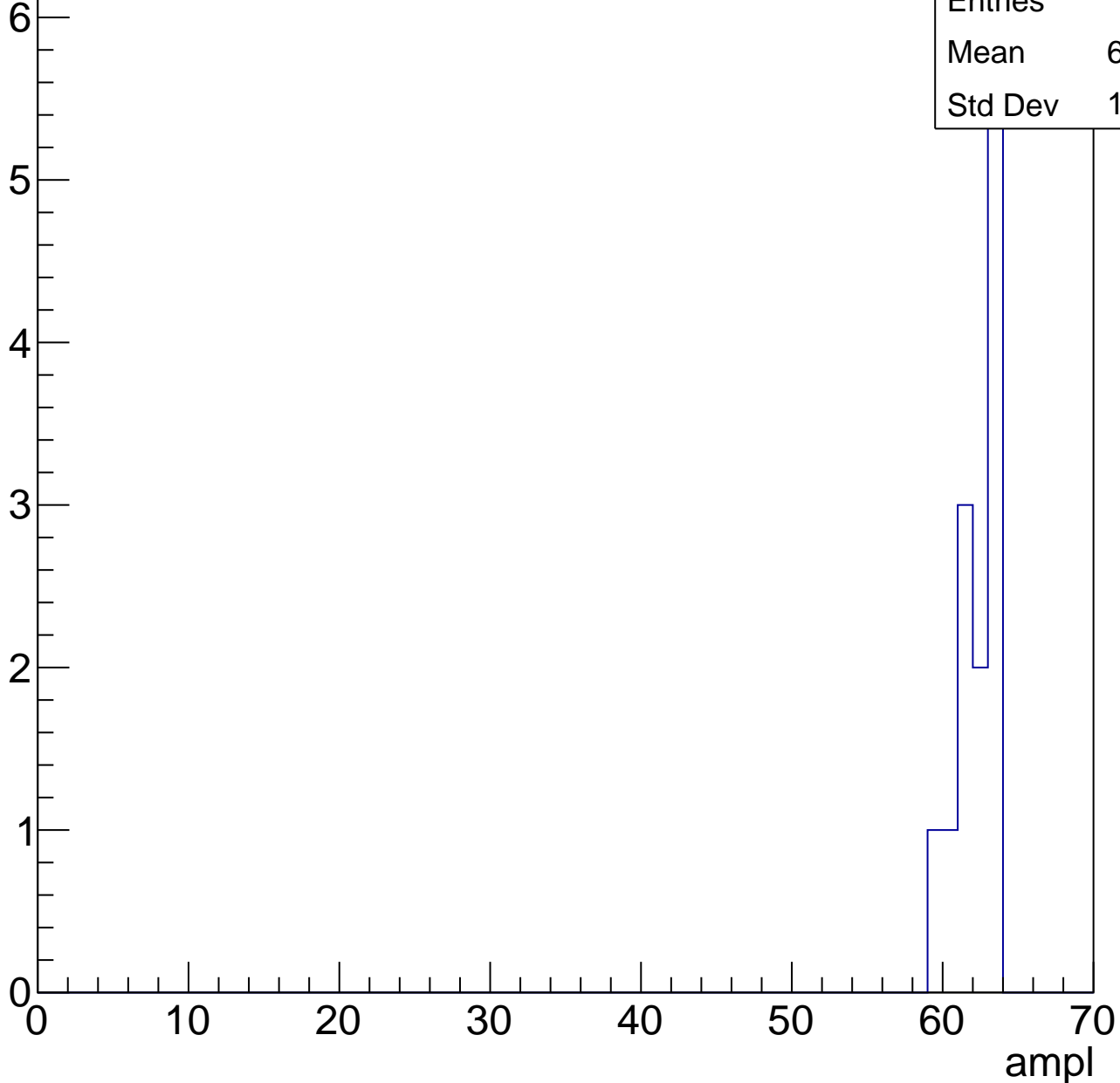


B1L103S, U7-ch87, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	13
Mean	61.85
Std Dev	1.292



B1L103S, U7-ch87, adc7

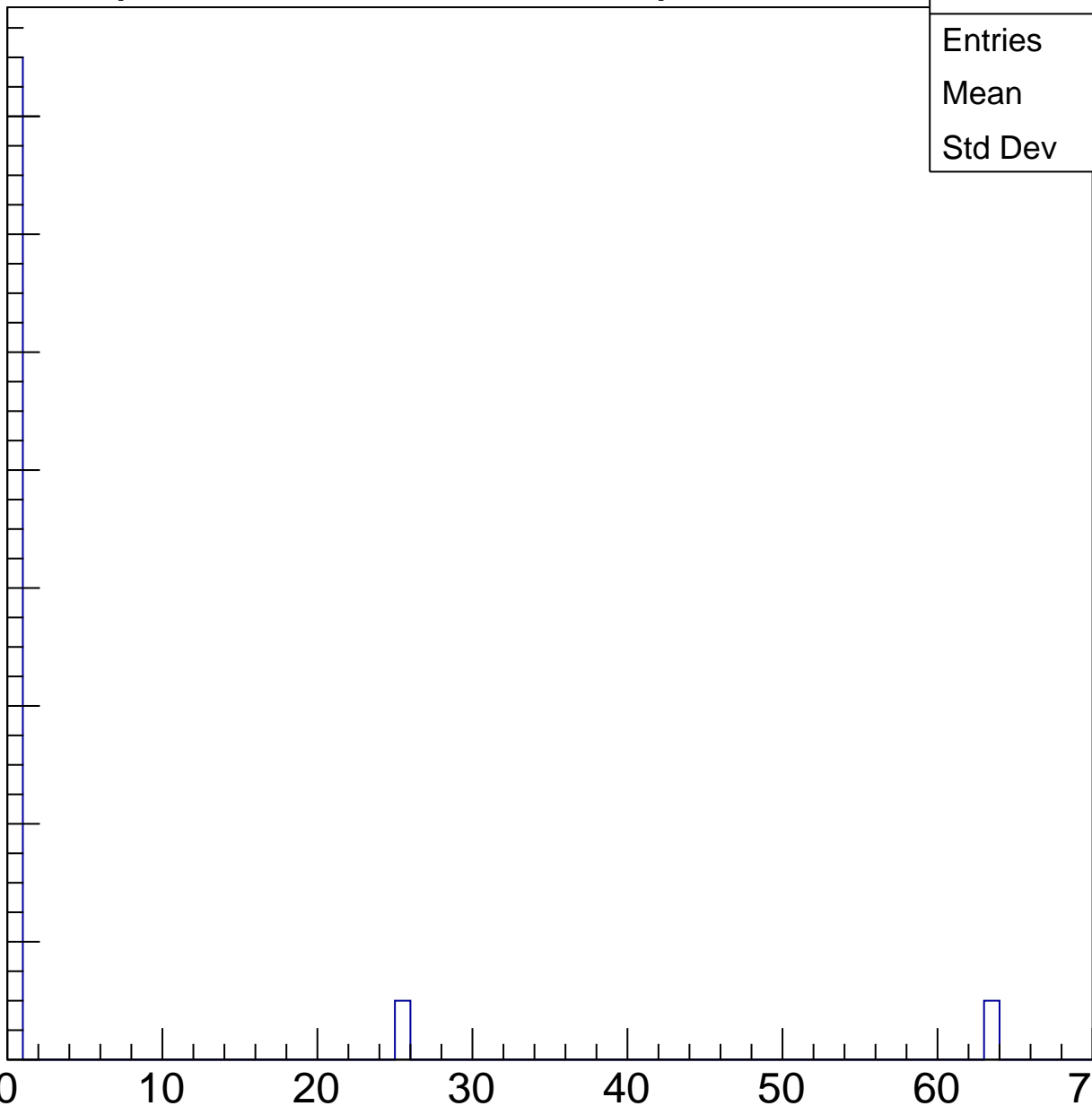
calib_packv5_041523_1651.root, FC#0, port C2

Entry

16
14
12
10
8
6
4
2
0

Entries	19
Mean	4.632
Std Dev	14.84

ampl



B1L103S, U7-ch88, adc0

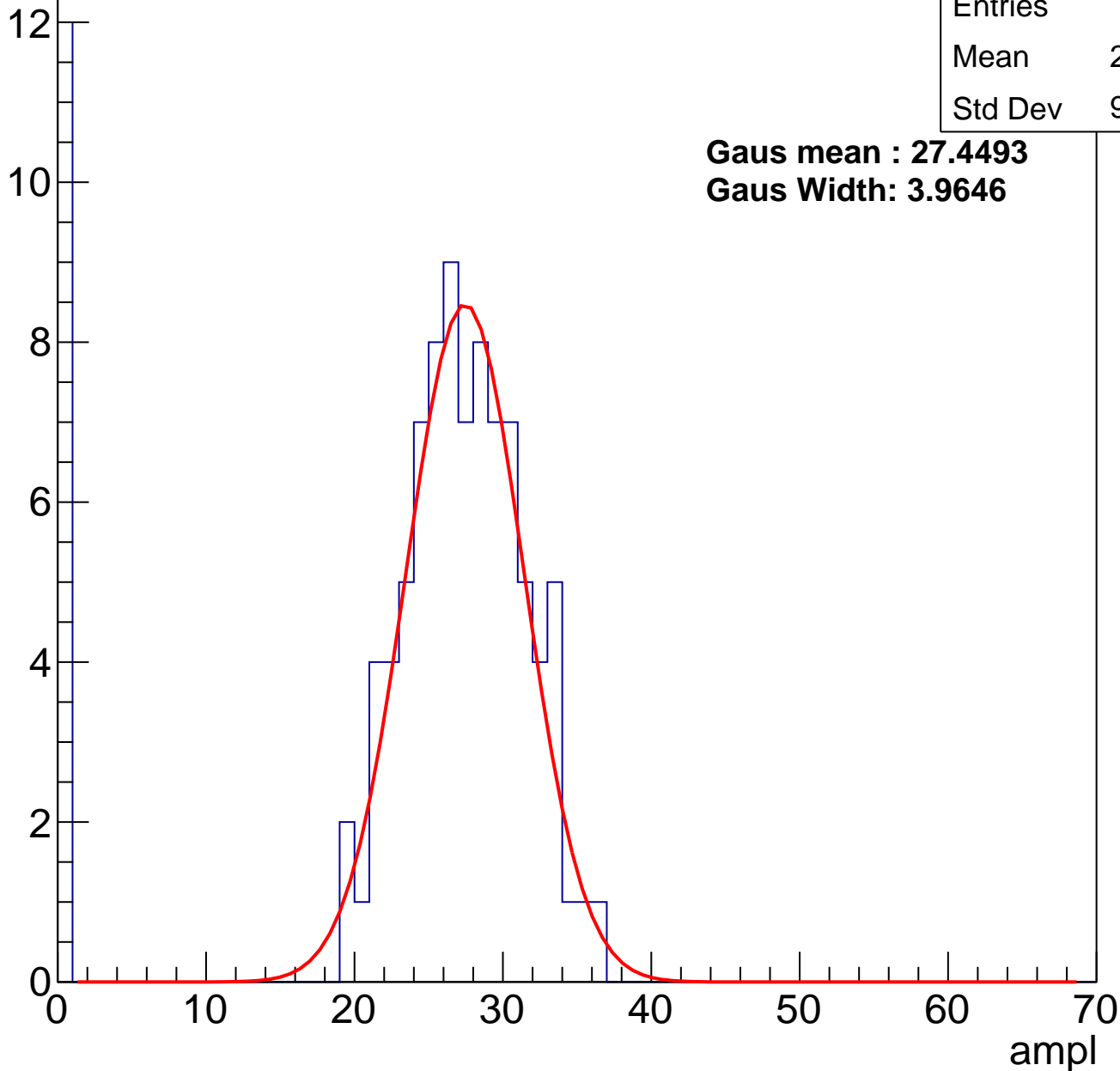
calib_packv5_041523_1651.root, FC#0, port C2

Entries	98
Mean	23.73
Std Dev	9.562

Gaus mean : 27.4493

Gaus Width: 3.9646

Entry



B1L103S, U7-ch88, adc1

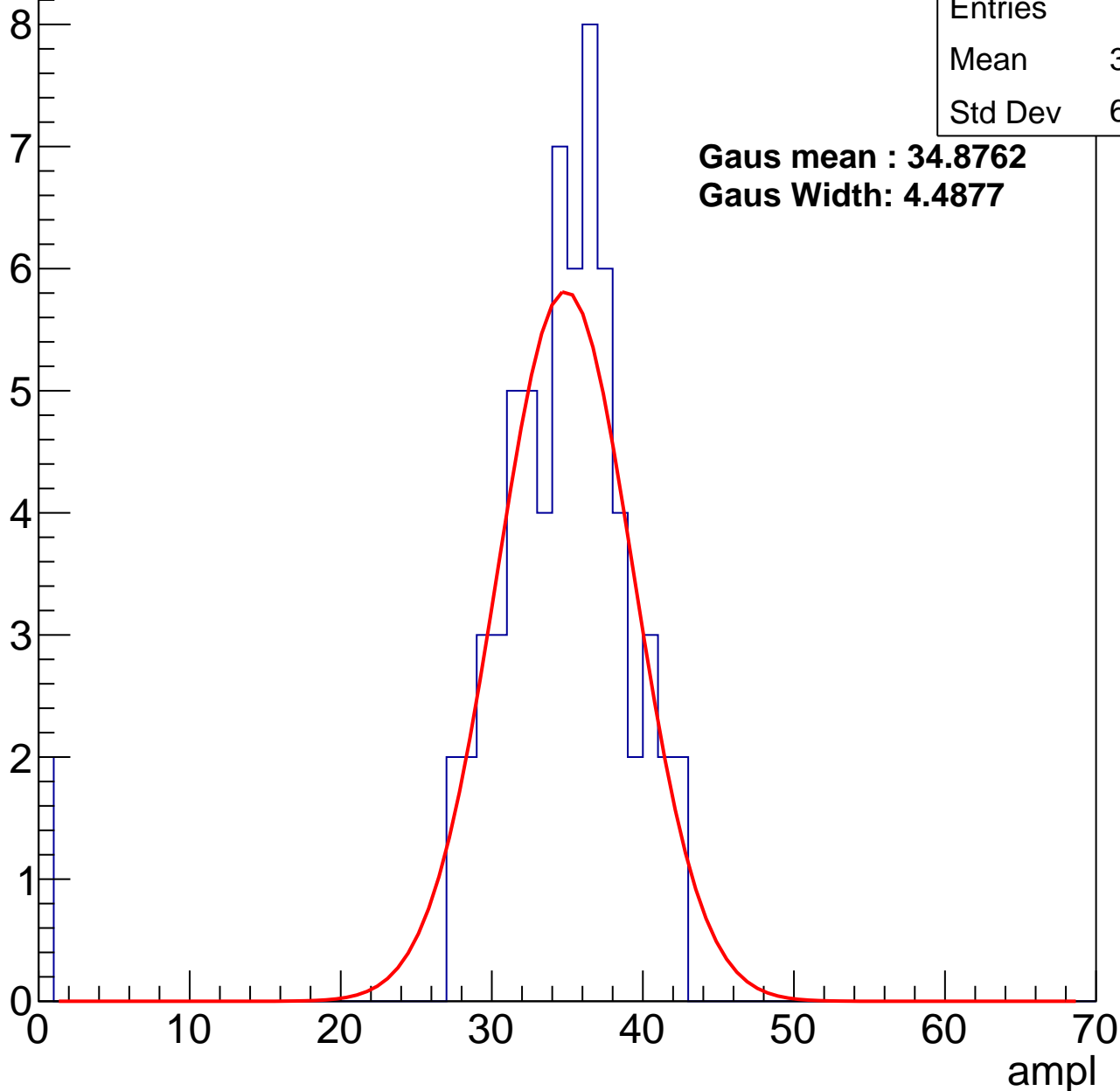
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	33.45
Std Dev	6.957

Gaus mean : 34.8762

Gaus Width: 4.4877



B1L103S, U7-ch88, adc2

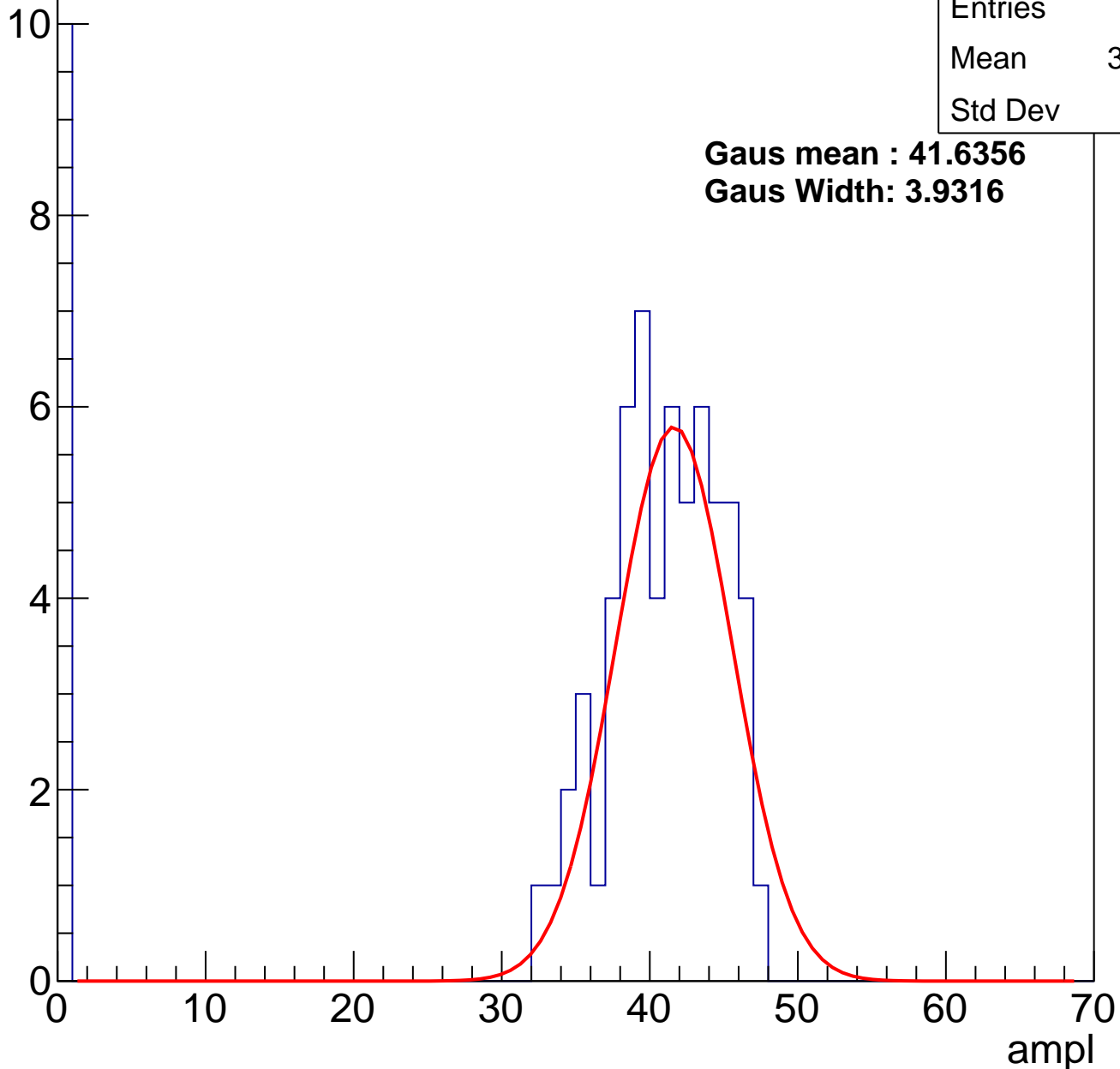
calib_packv5_041523_1651.root, FC#0, port C2

Entries	71
Mean	34.83
Std Dev	14.5

Gaus mean : 41.6356

Gaus Width: 3.9316

Entry

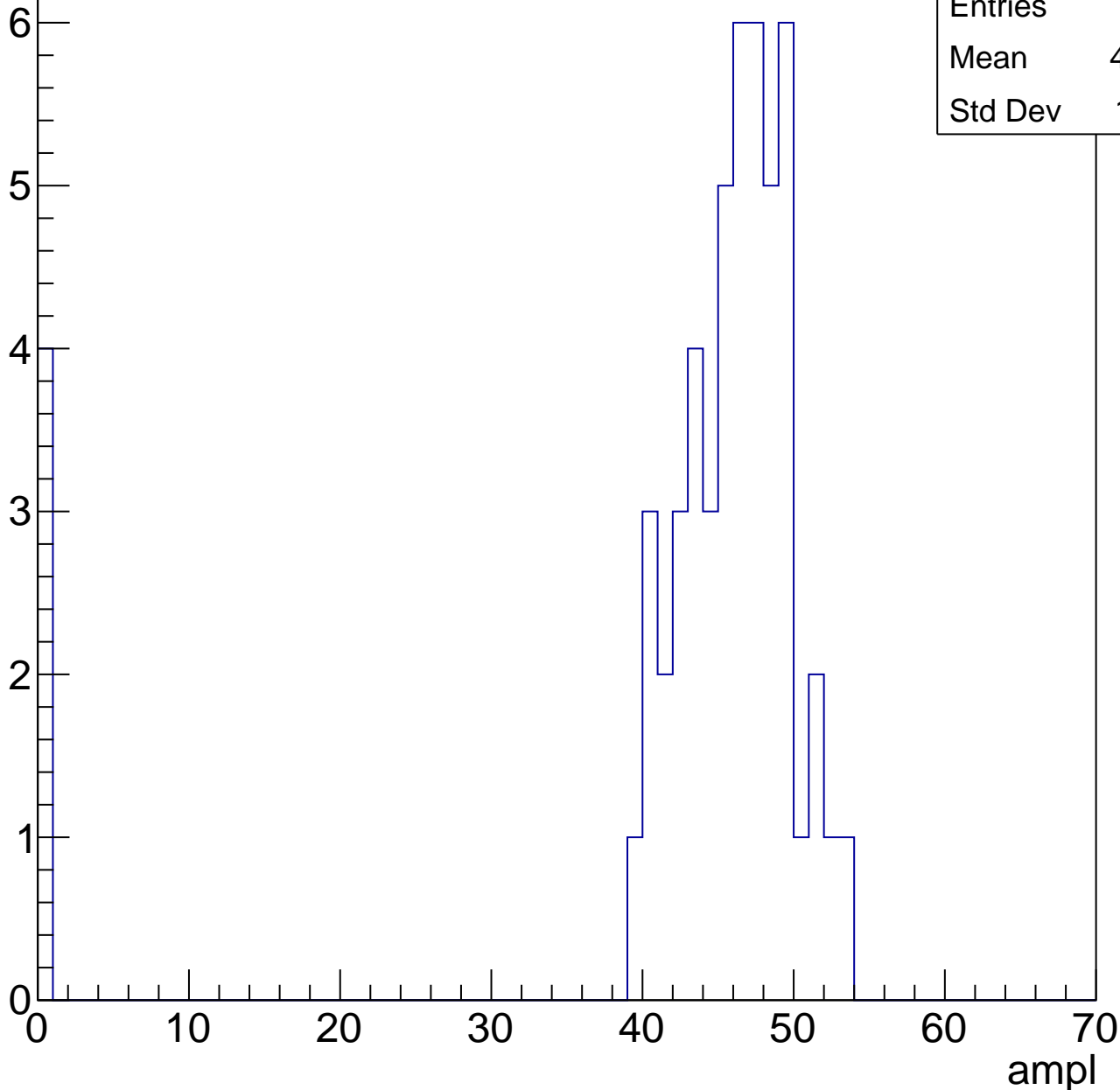


B1L103S, U7-ch88, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	42.36
Std Dev	12.51

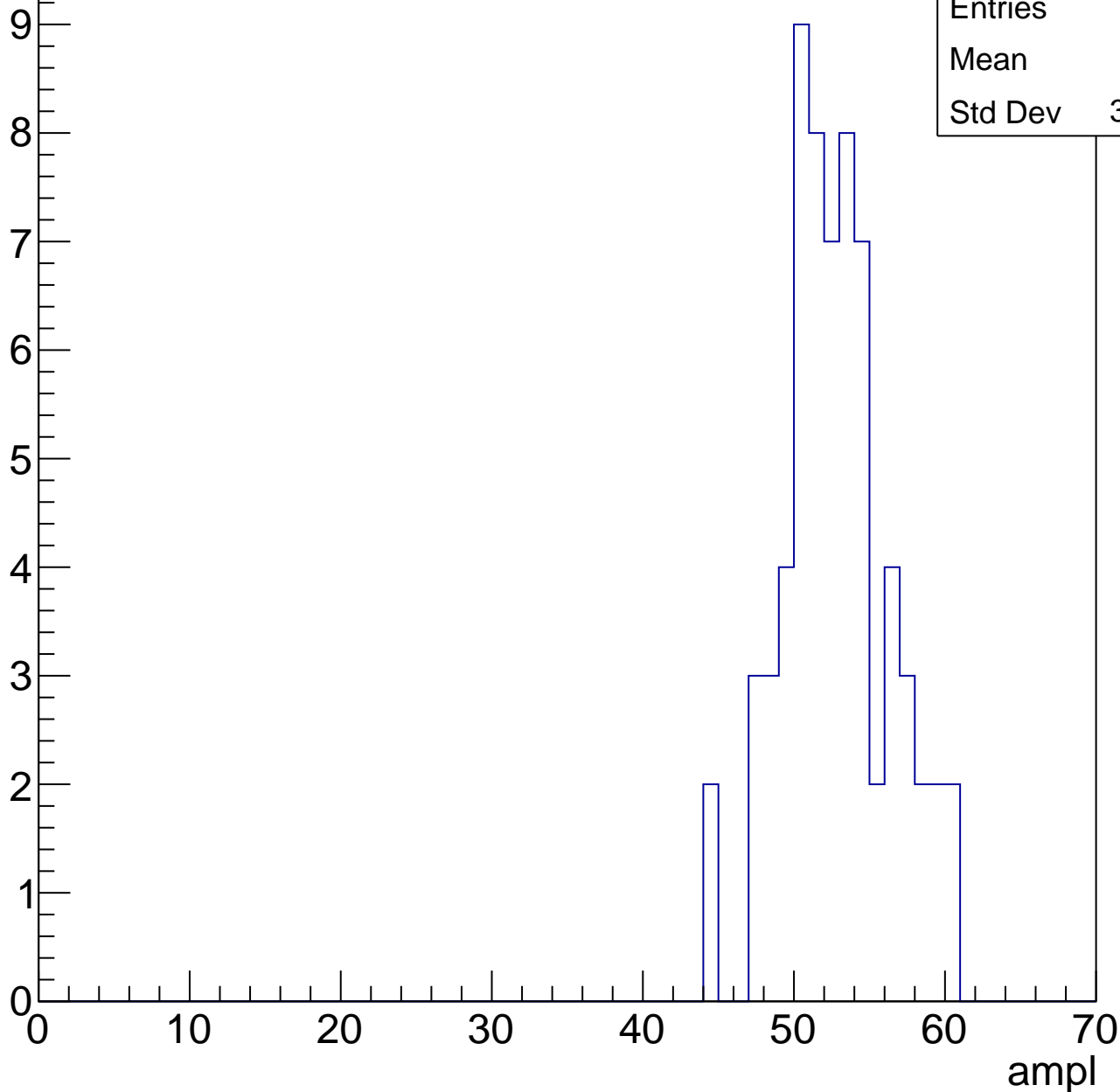


B1L103S, U7-ch88, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	52.3
Std Dev	3.516

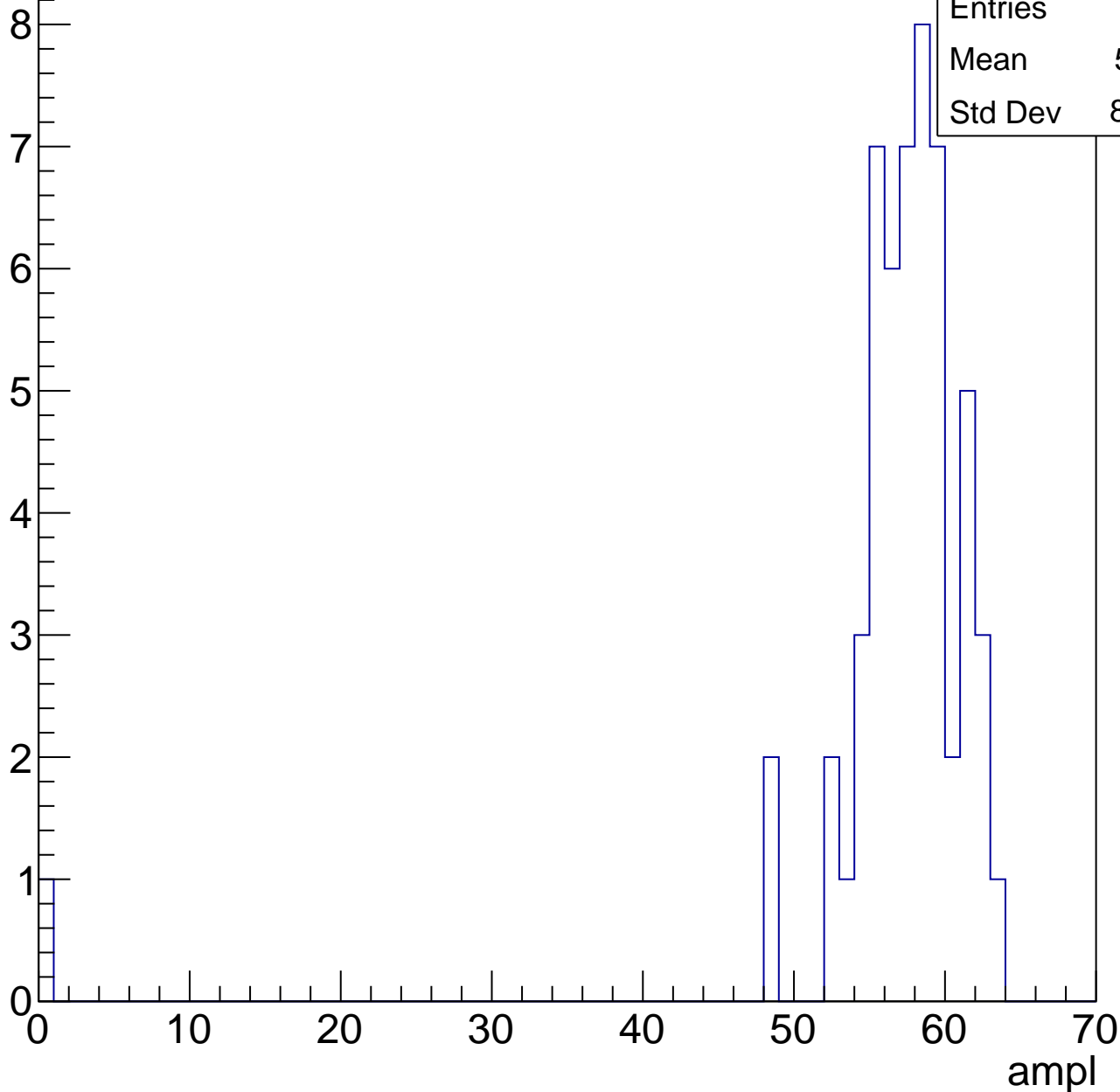


B1L103S, U7-ch88, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	56.11
Std Dev	8.245

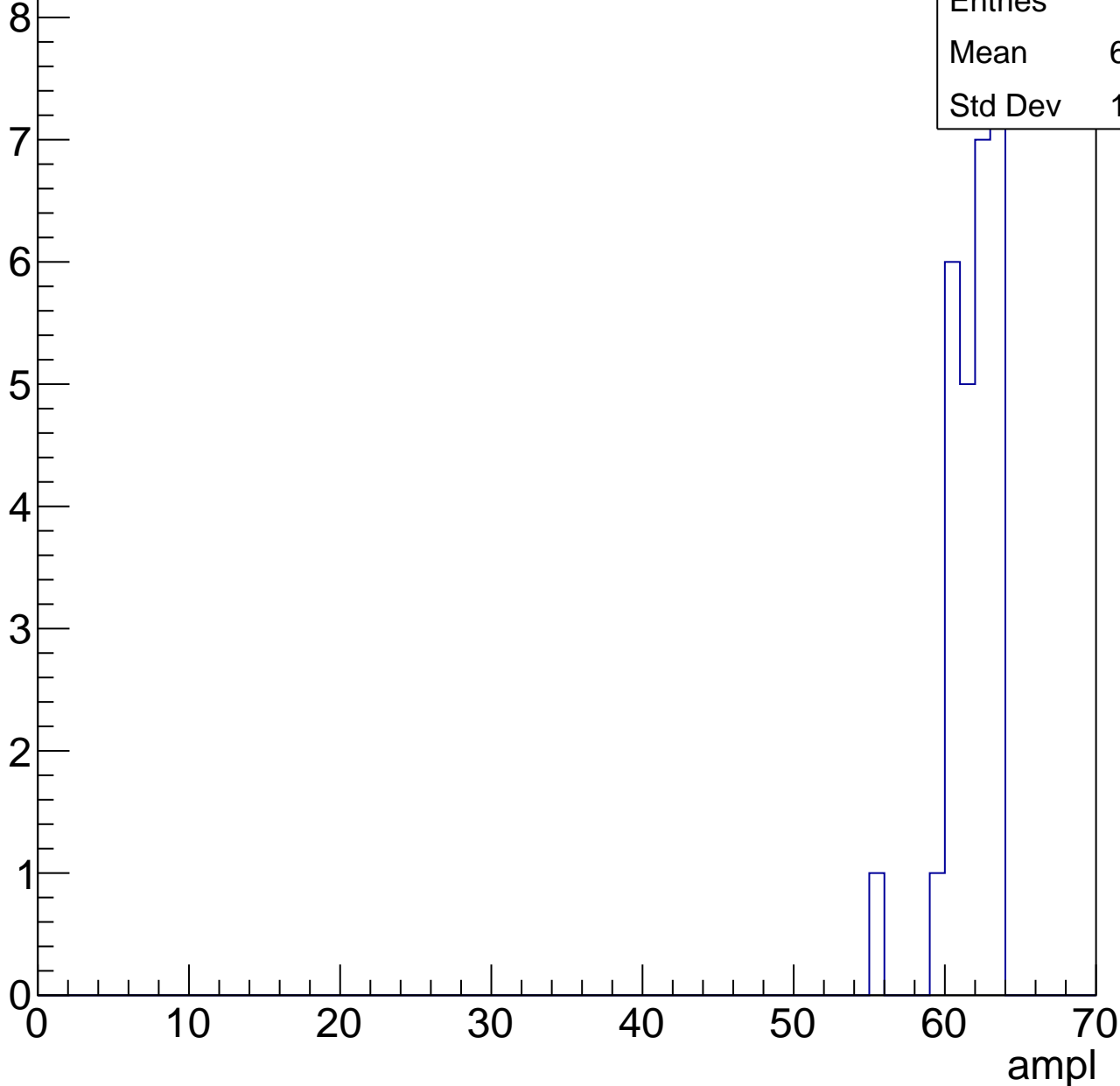


B1L103S, U7-ch88, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	28
Mean	61.32
Std Dev	1.712



B1L103S, U7-ch88, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry



B1L103S, U7-ch89, adc0

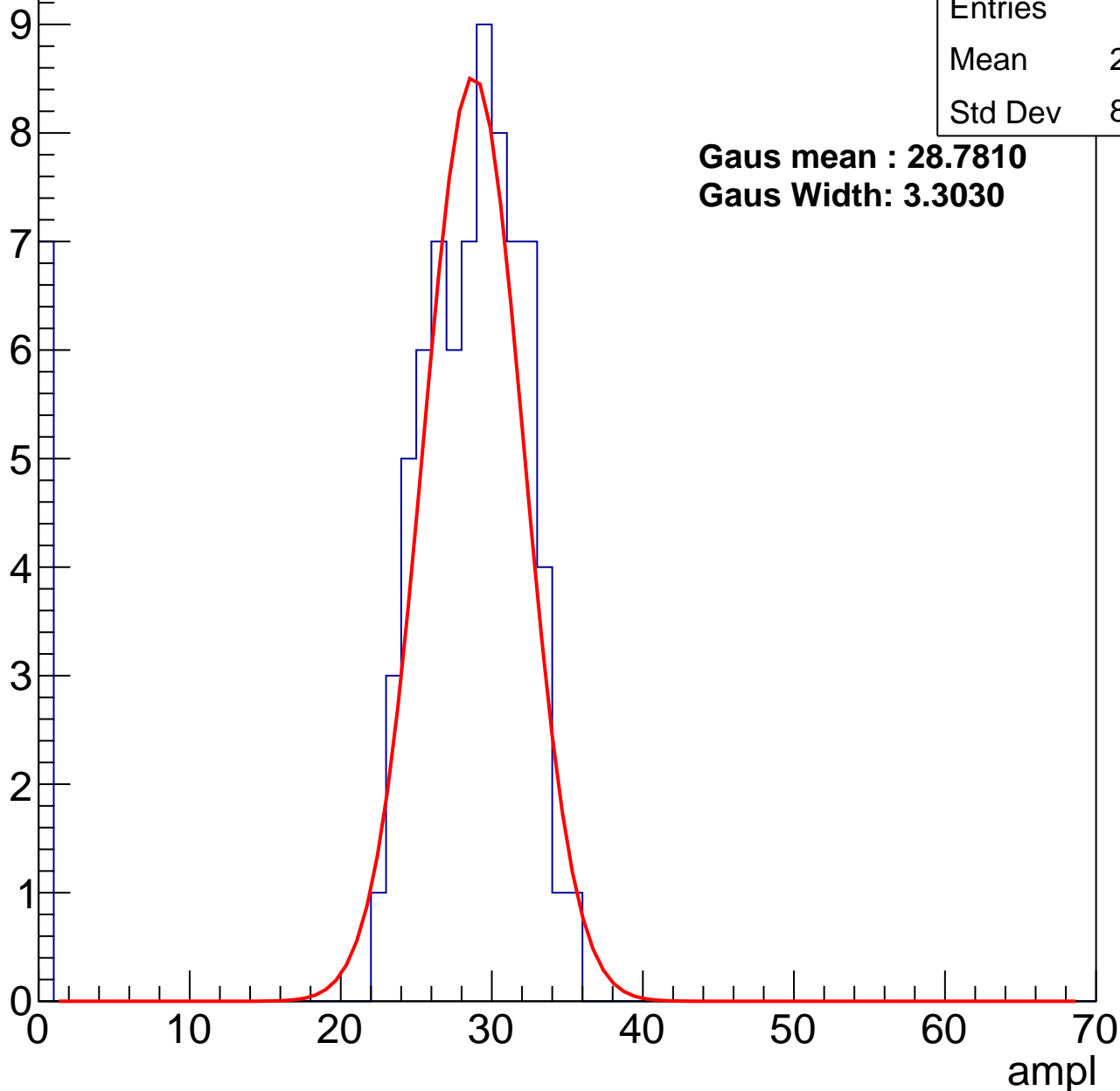
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	79
Mean	25.87
Std Dev	8.576

Gaus mean : 28.7810

Gaus Width: 3.3030



B1L103S, U7-ch89, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	83
Mean	34.04
Std Dev	10

Gaus mean : 37.0503

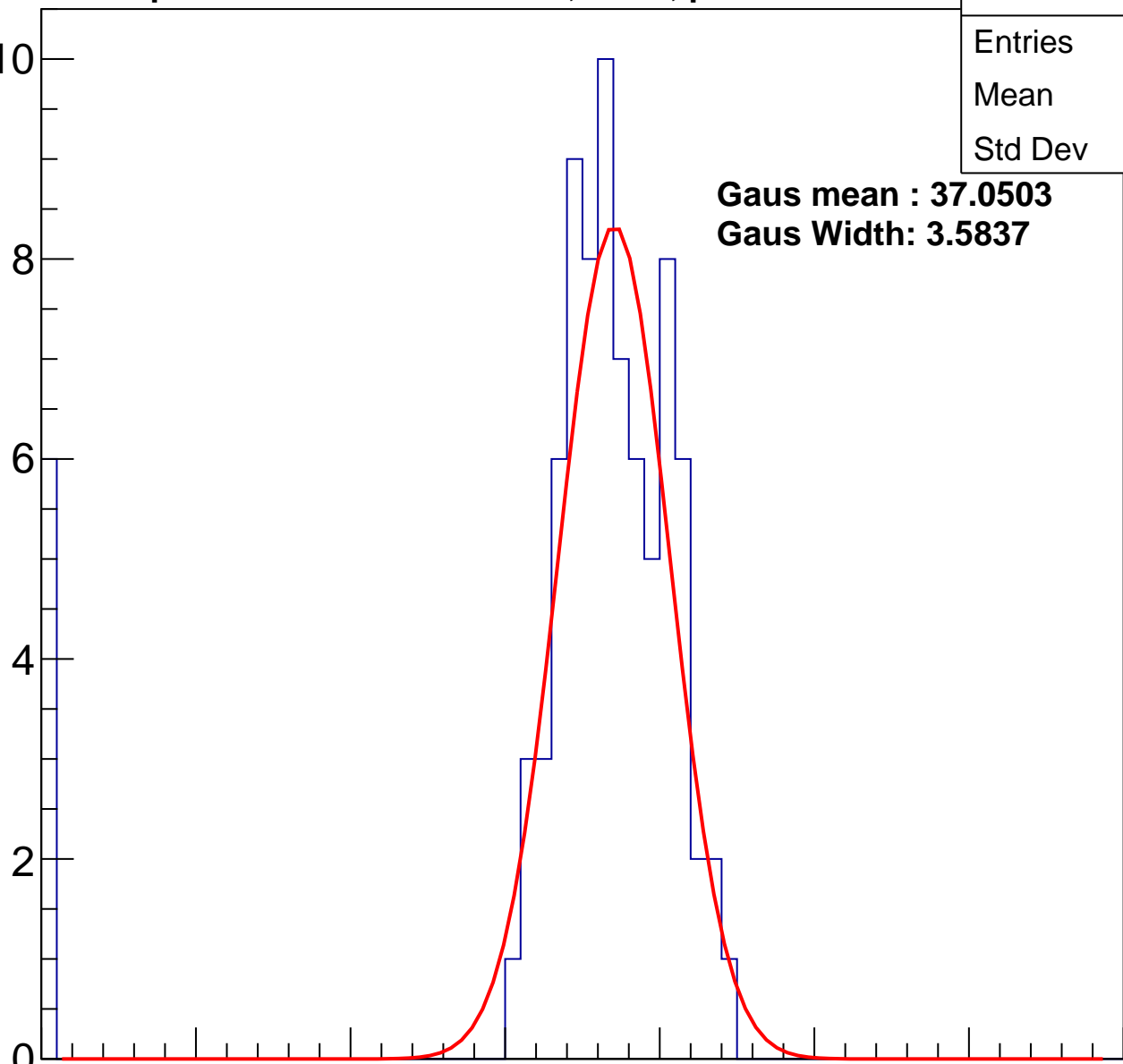
Gaus Width: 3.5837

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl



B1L103S, U7-ch89, adc2

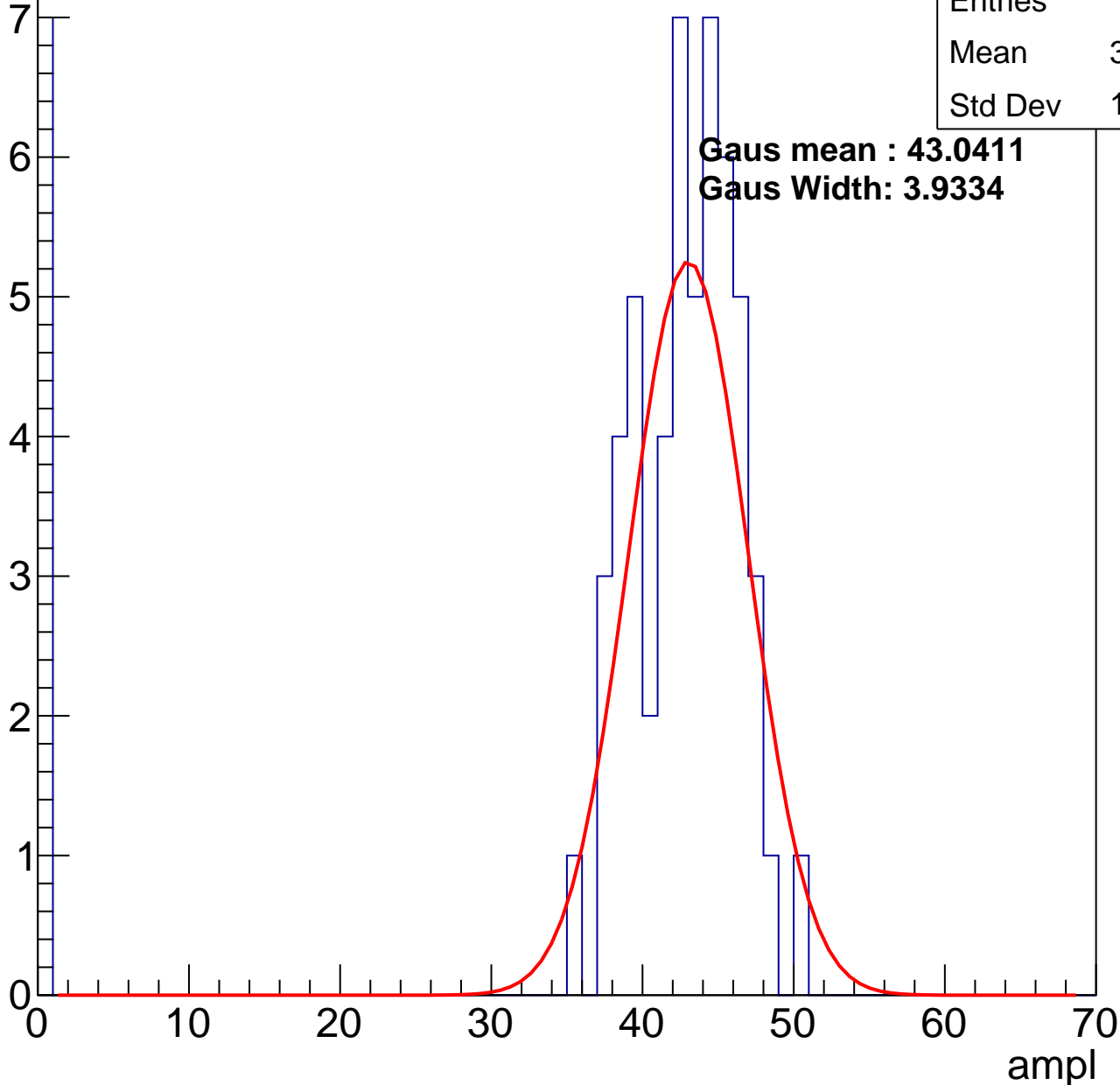
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	37.59
Std Dev	13.88

Gaus mean : 43.0411

Gaus Width: 3.9334

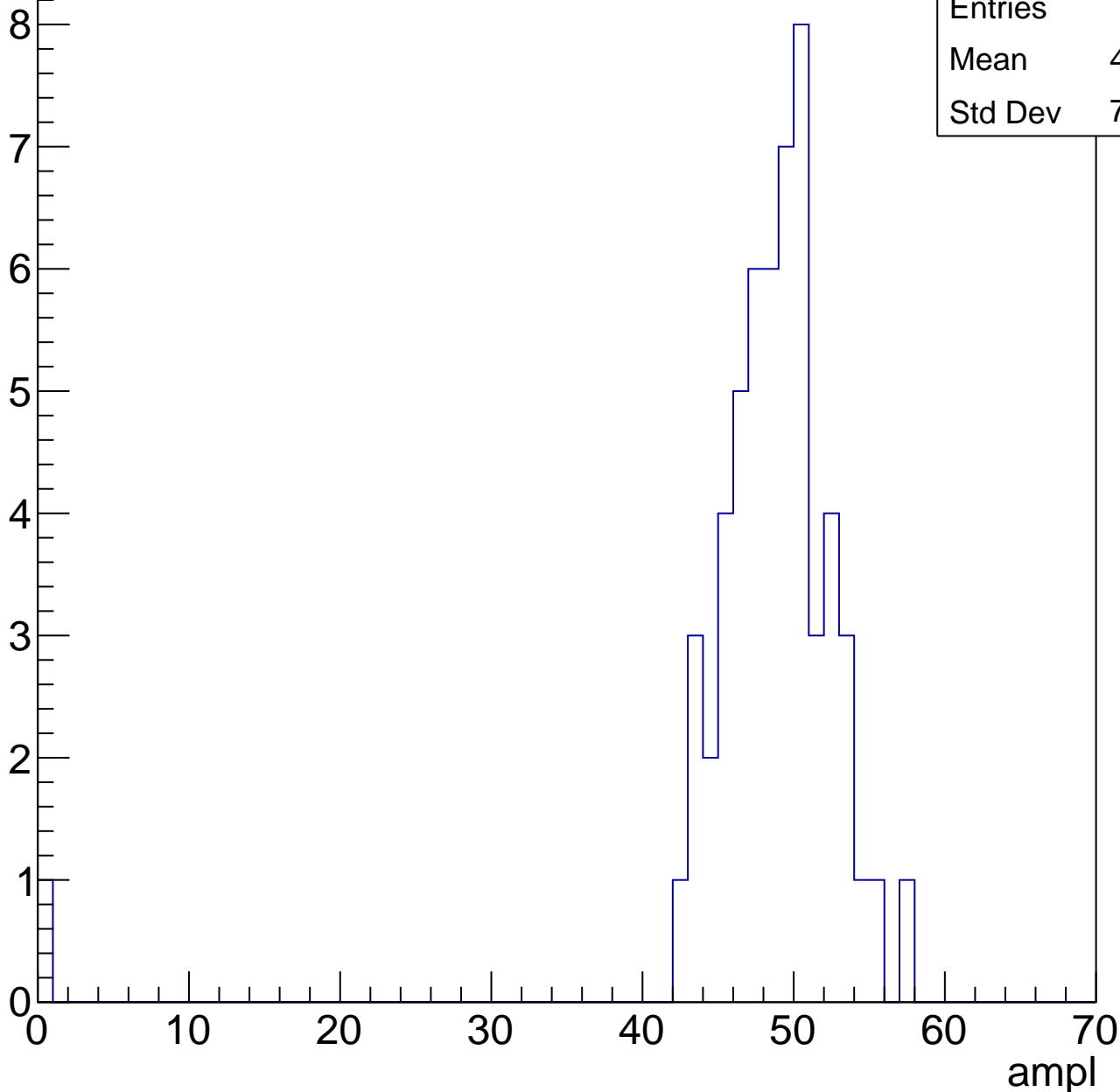


B1L103S, U7-ch89, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	47.64
Std Dev	7.162

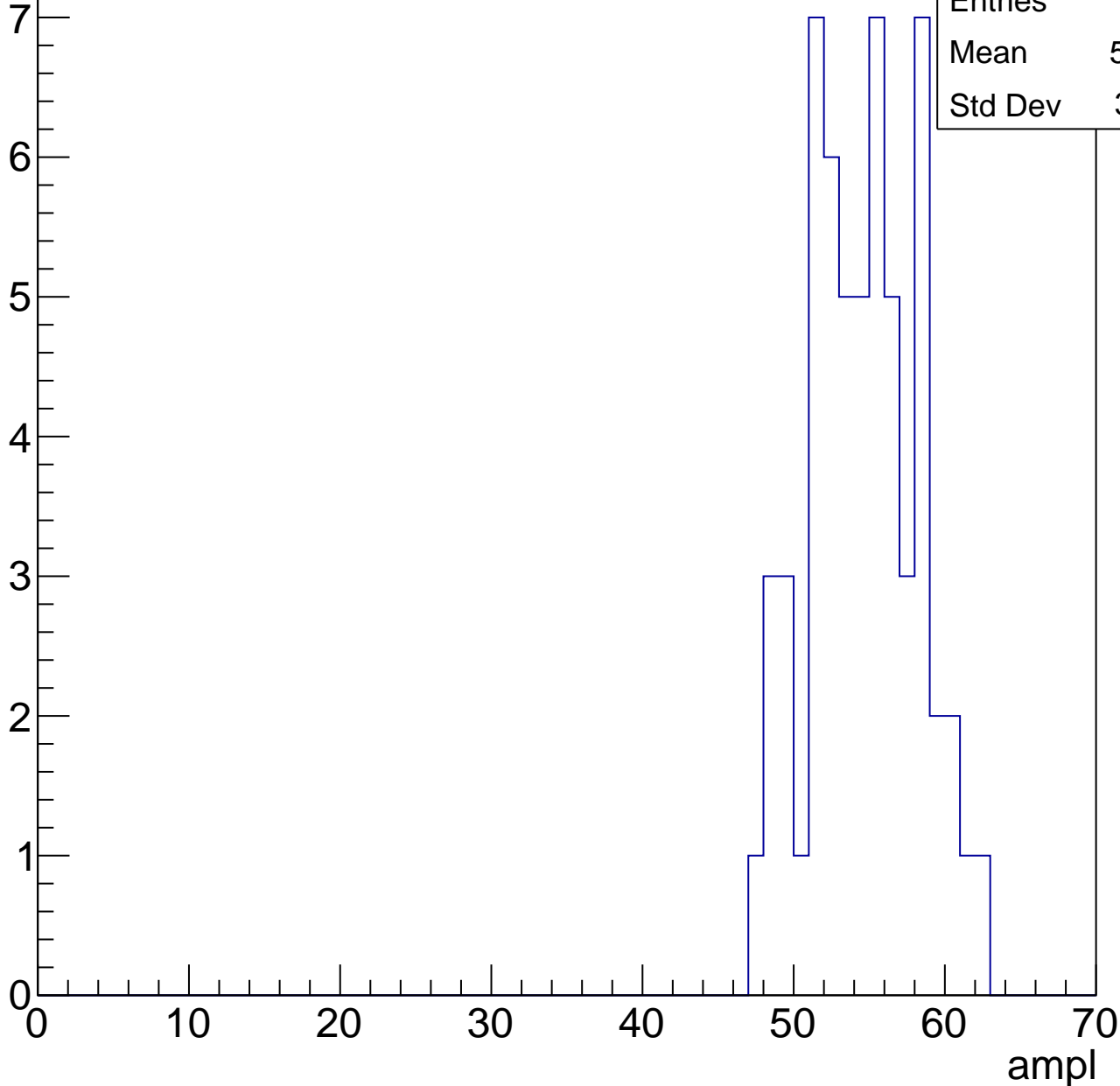


B1L103S, U7-ch89, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	54.15
Std Dev	3.541



B1L103S, U7-ch89, adc5

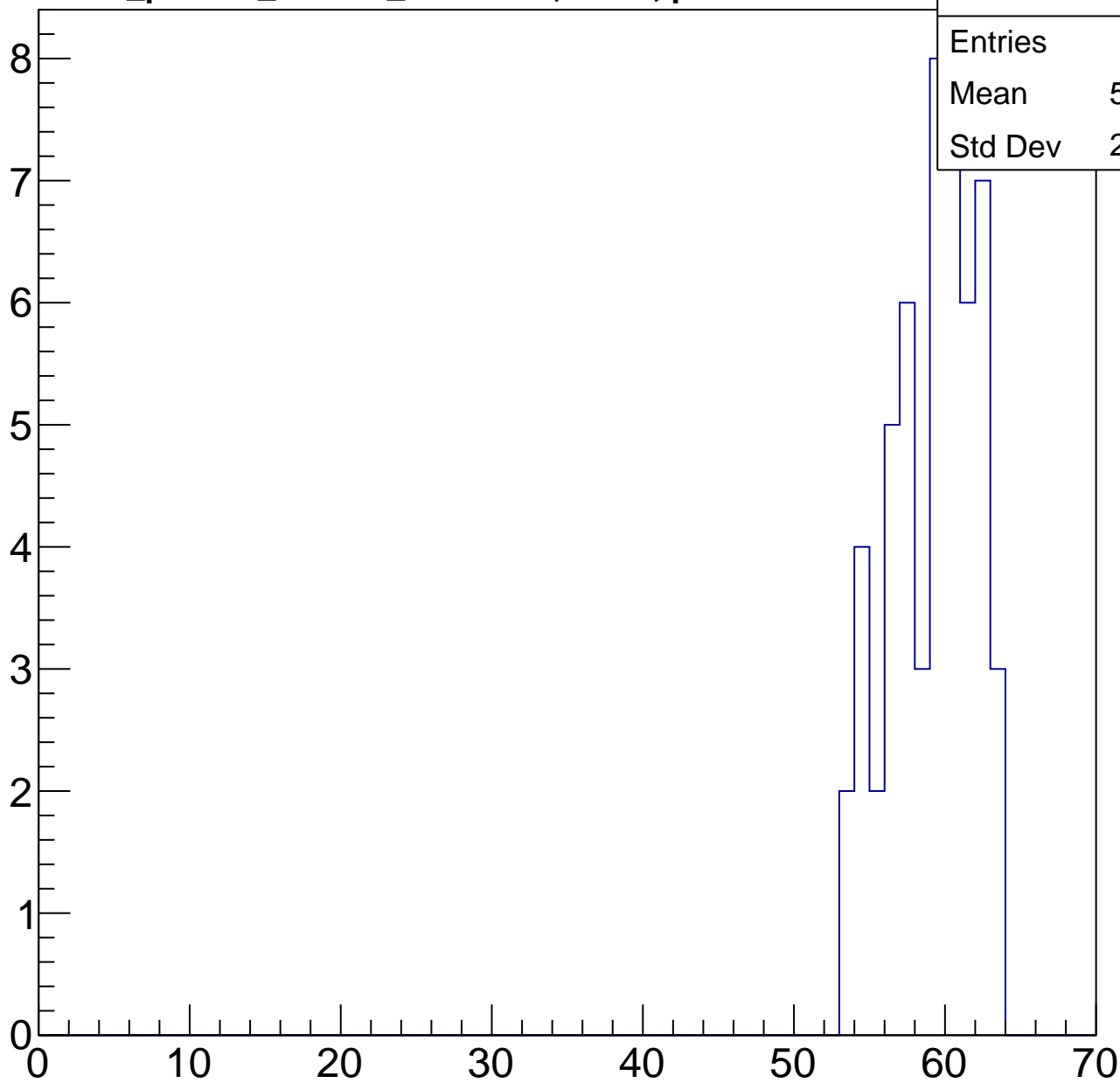
calib_packv5_041523_1651.root, FC#0, port C2

Entry

8
7
6
5
4
3
2
1
0

Entries	54
Mean	58.69
Std Dev	2.768

ampl

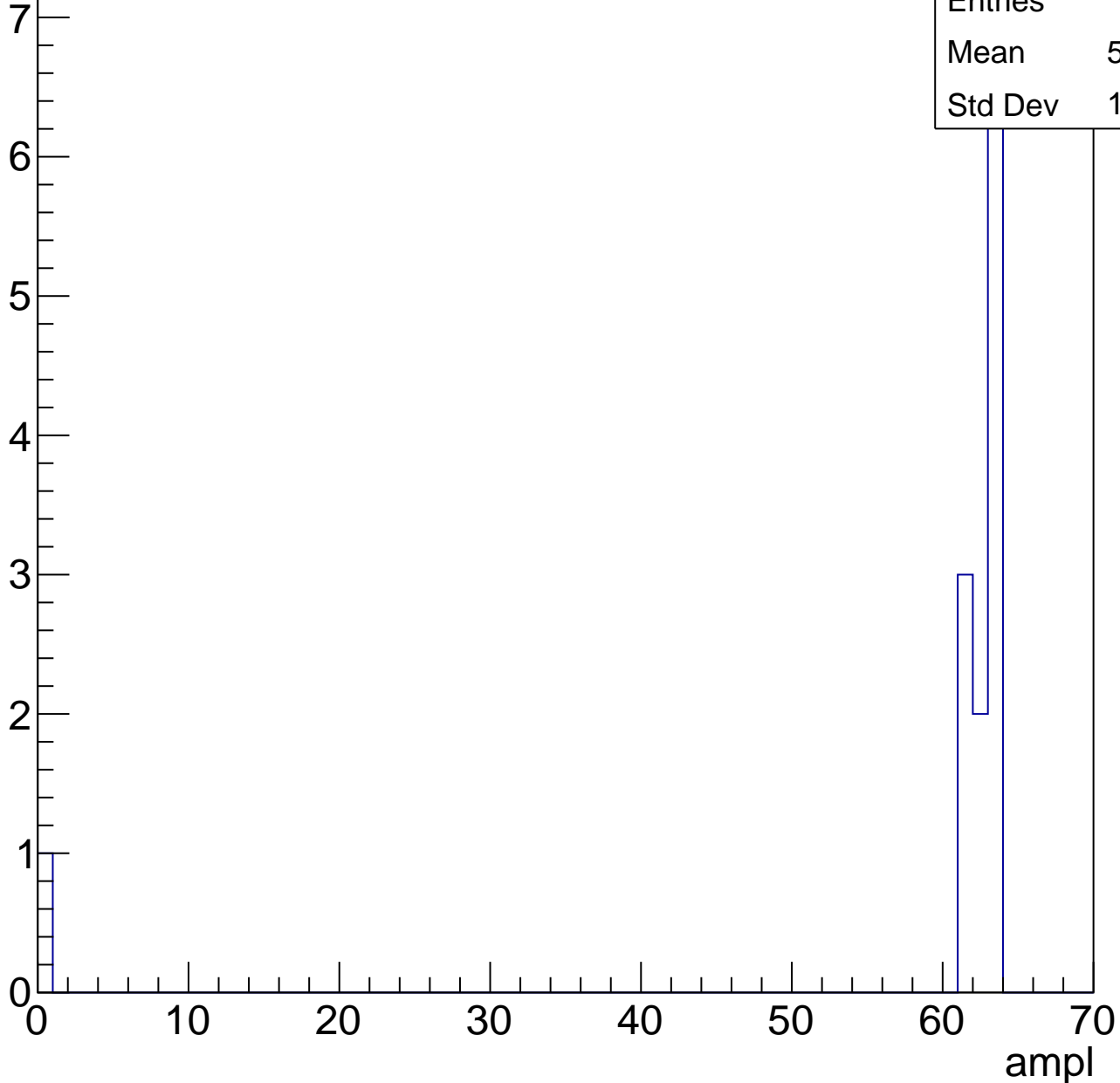


B1L103S, U7-ch89, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	13
Mean	57.54
Std Dev	16.63



B1L103S, U7-ch89, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch90, adc0

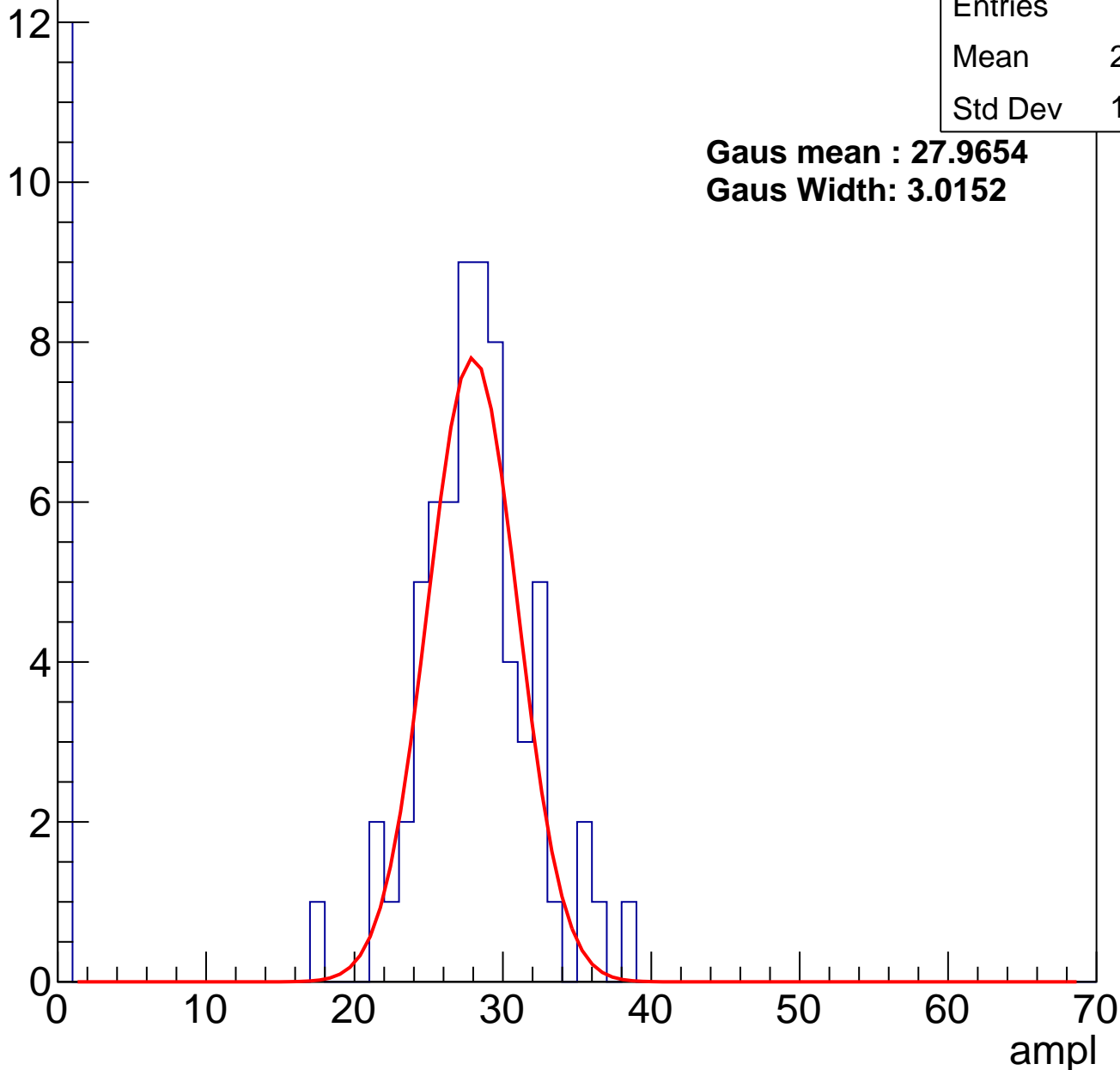
calib_packv5_041523_1651.root, FC#0, port C2

Entries	78
Mean	23.46
Std Dev	10.56

Gaus mean : 27.9654

Gaus Width: 3.0152

Entry



B1L103S, U7-ch90, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	104
Mean	30.16
Std Dev	13.4

Gaus mean : 35.4732

Gaus Width: 4.3468

Entry

16
14
12
10
8
6
4
2
0

ampl

0

10

20

30

40

50

60

70

B1L103S, U7-ch90, adc2

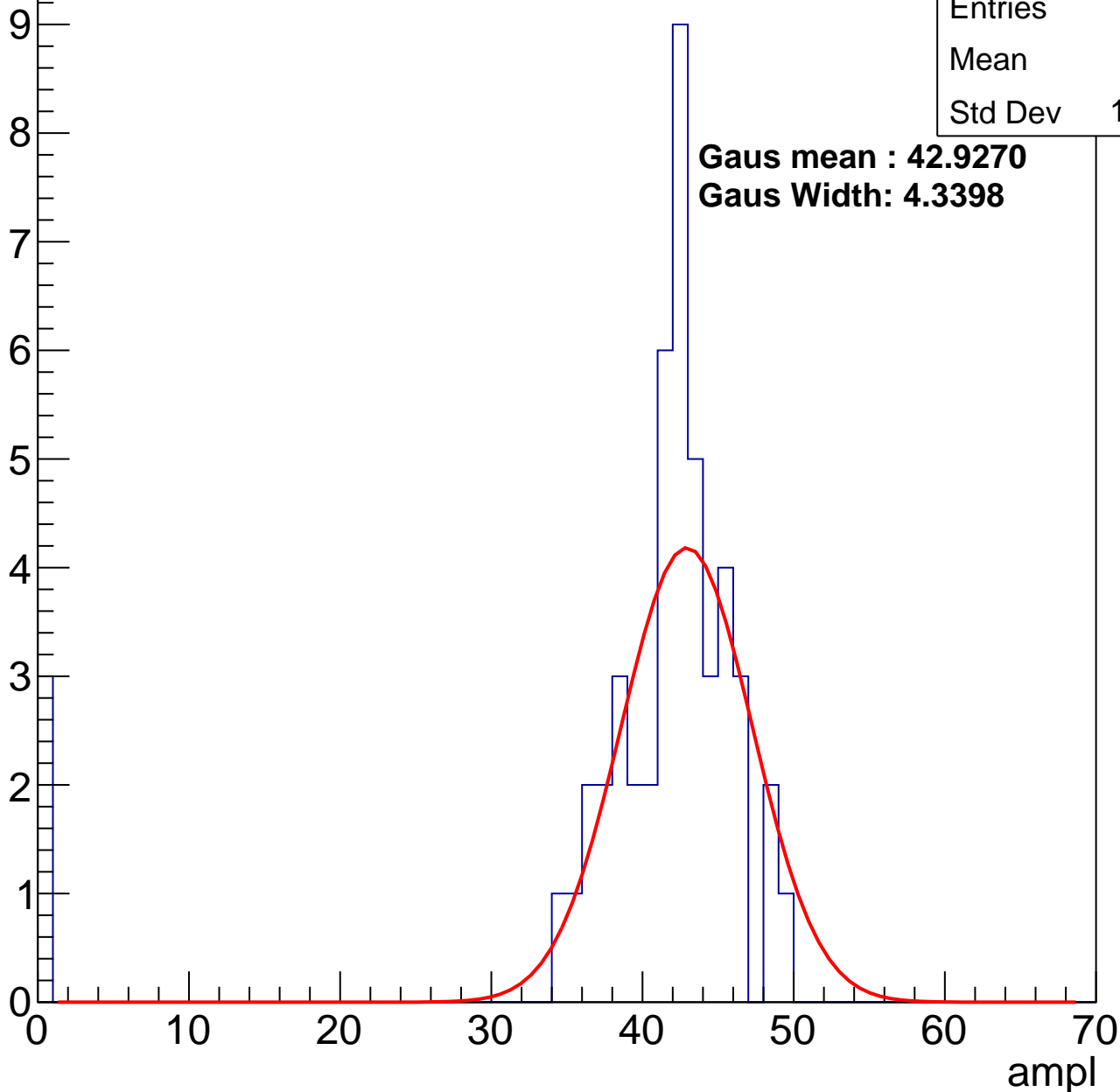
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	39.2
Std Dev	10.54

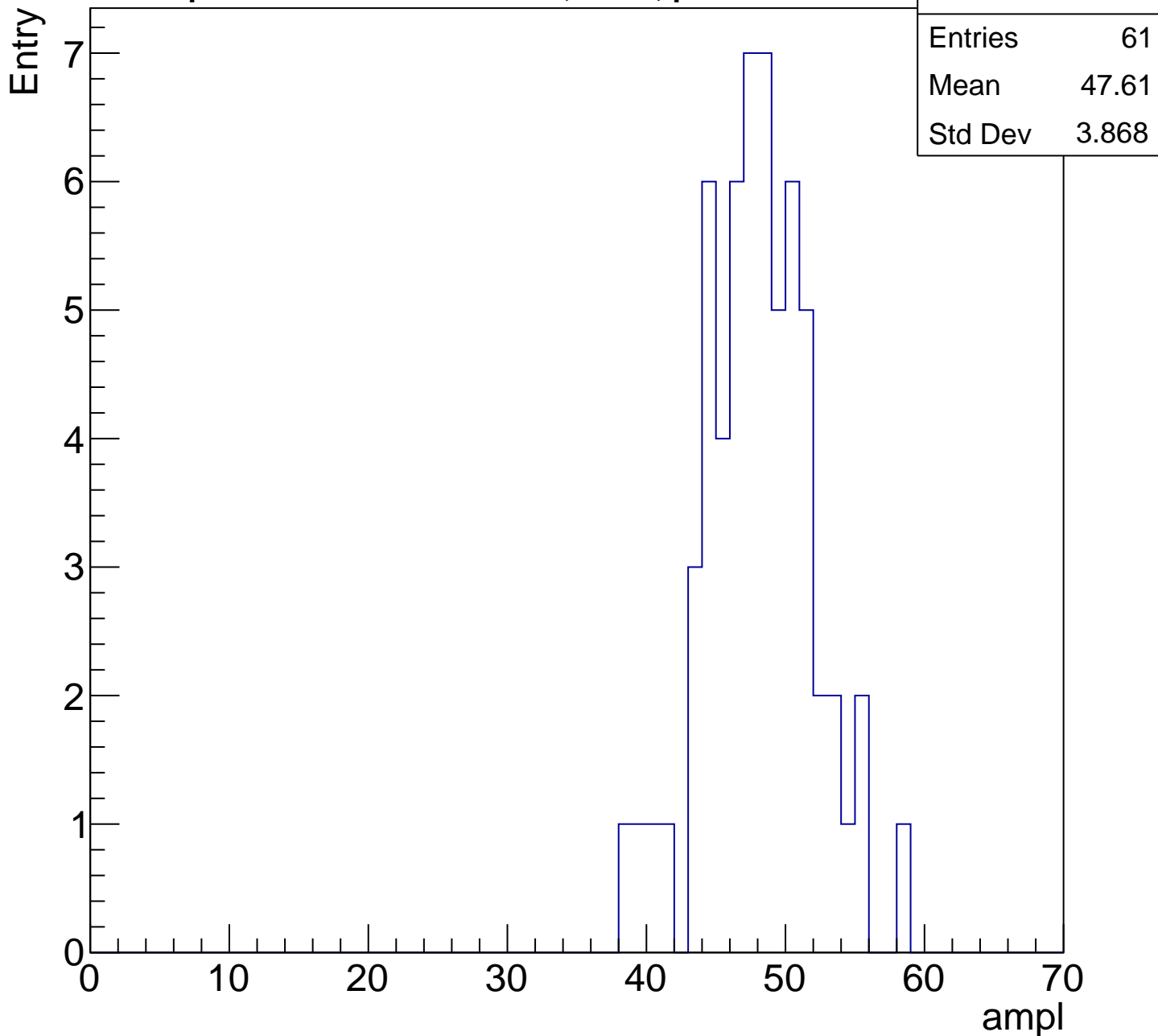
Gaus mean : 42.9270

Gaus Width: 4.3398



B1L103S, U7-ch90, adc3

calib_packv5_041523_1651.root, FC#0, port C2

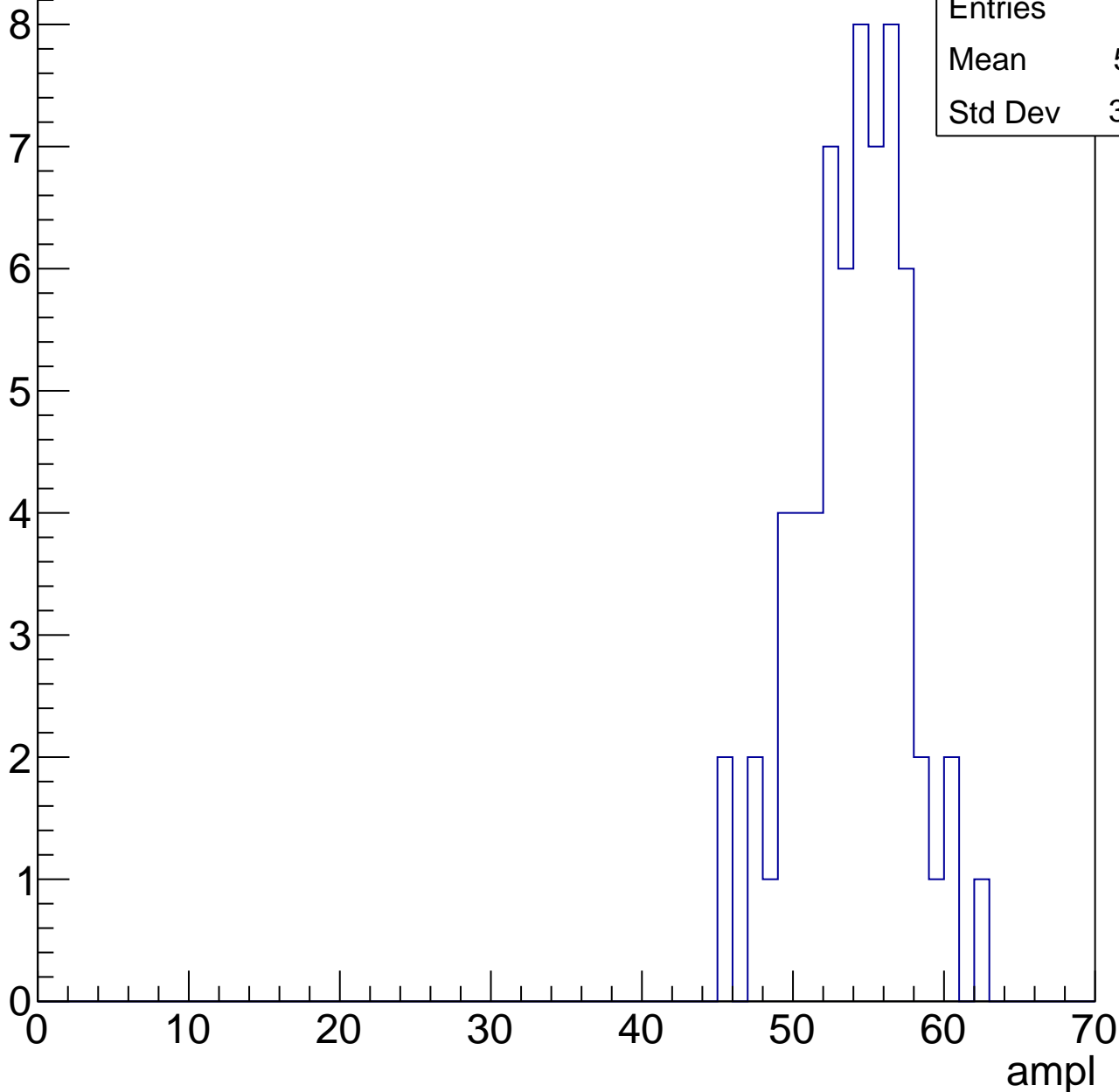


B1L103S, U7-ch90, adc4

calib_packv5_041523_1651.root, FC#0, port C2

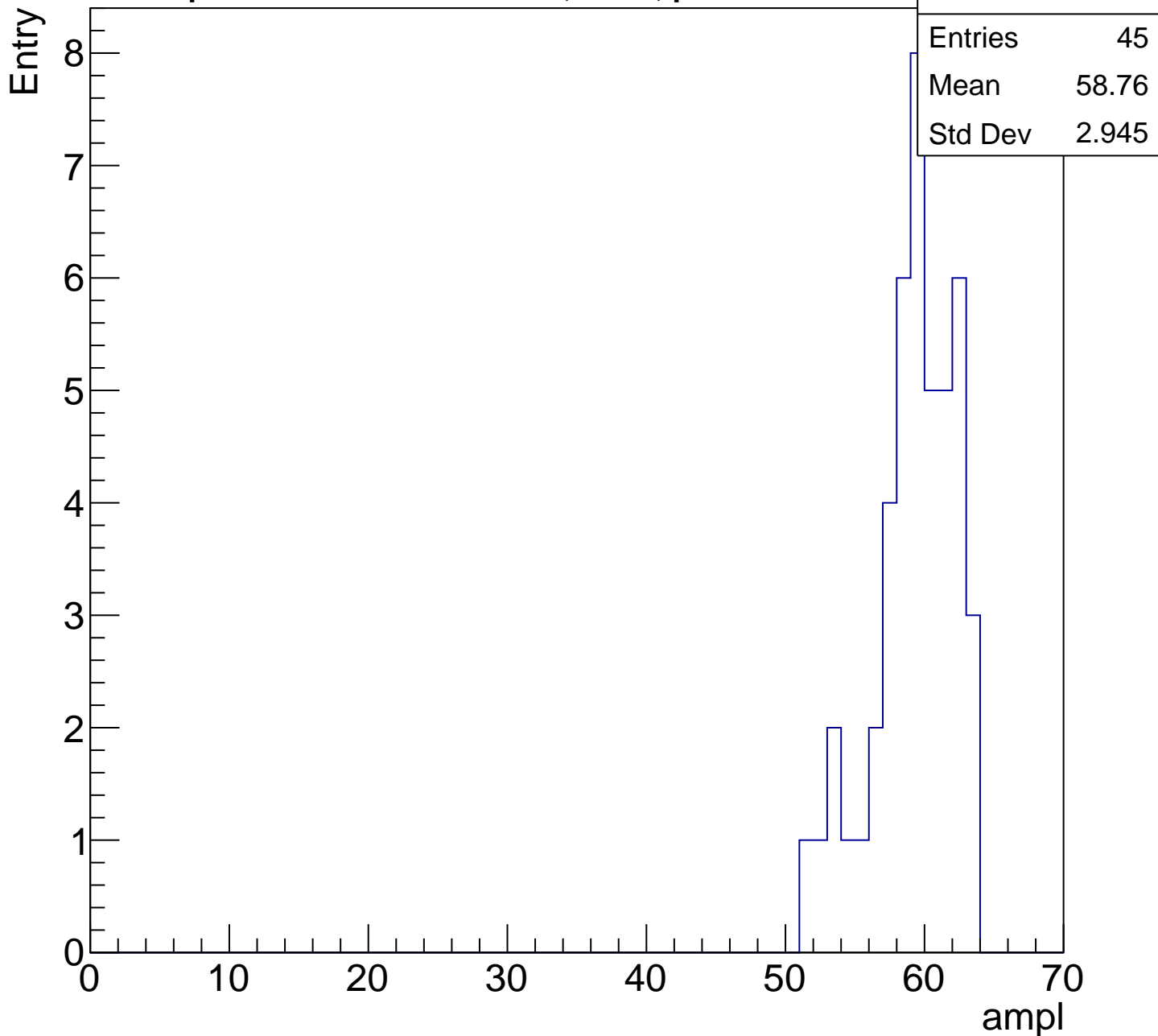
Entry

Entries	65
Mean	53.51
Std Dev	3.509



B1L103S, U7-ch90, adc5

calib_packv5_041523_1651.root, FC#0, port C2

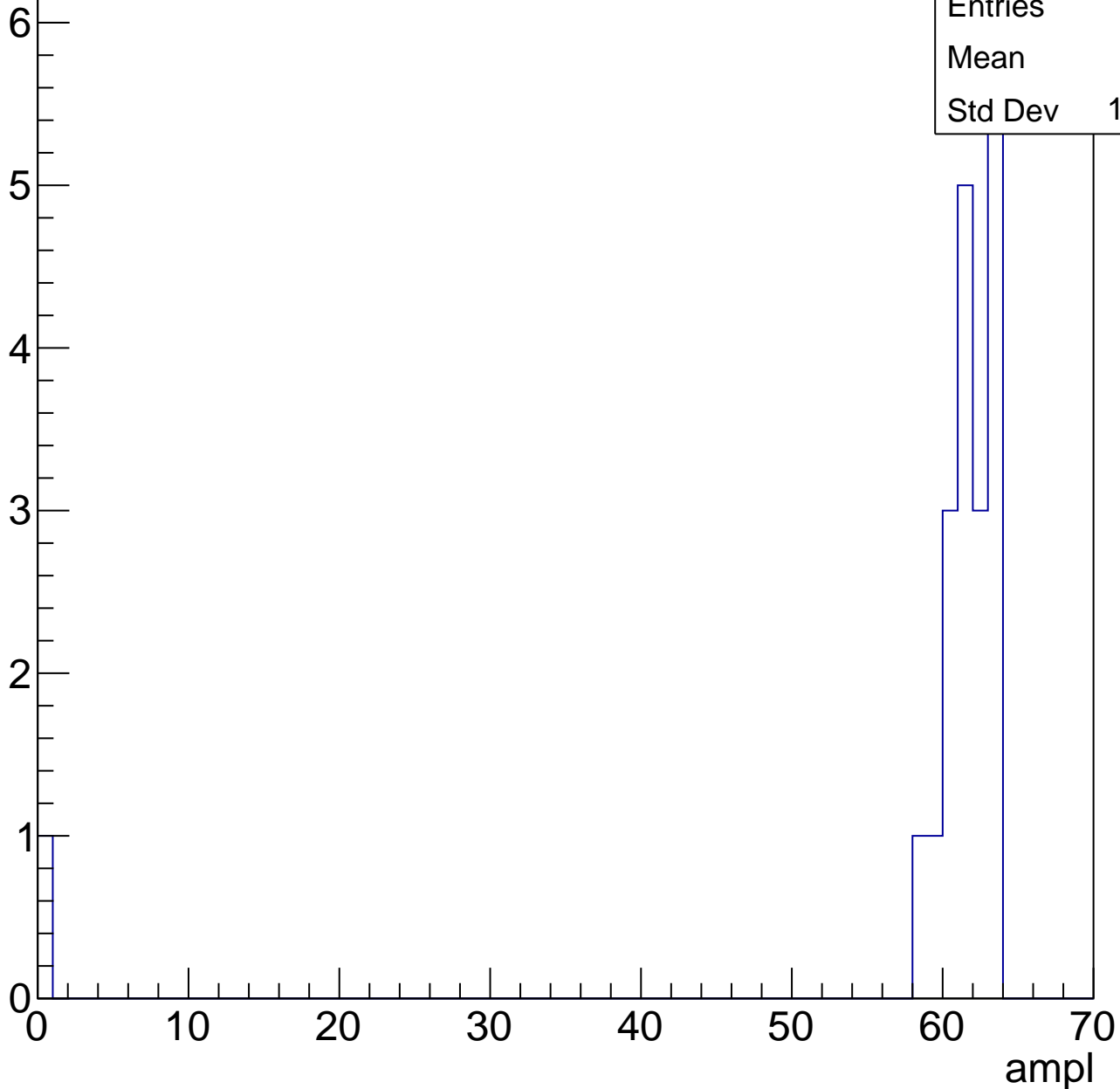


B1L103S, U7-ch90, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	20
Mean	58.3
Std Dev	13.45



B1L103S, U7-ch90, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	20
Mean	3.15
Std Dev	13.73

B1L103S, U7-ch91, adc0

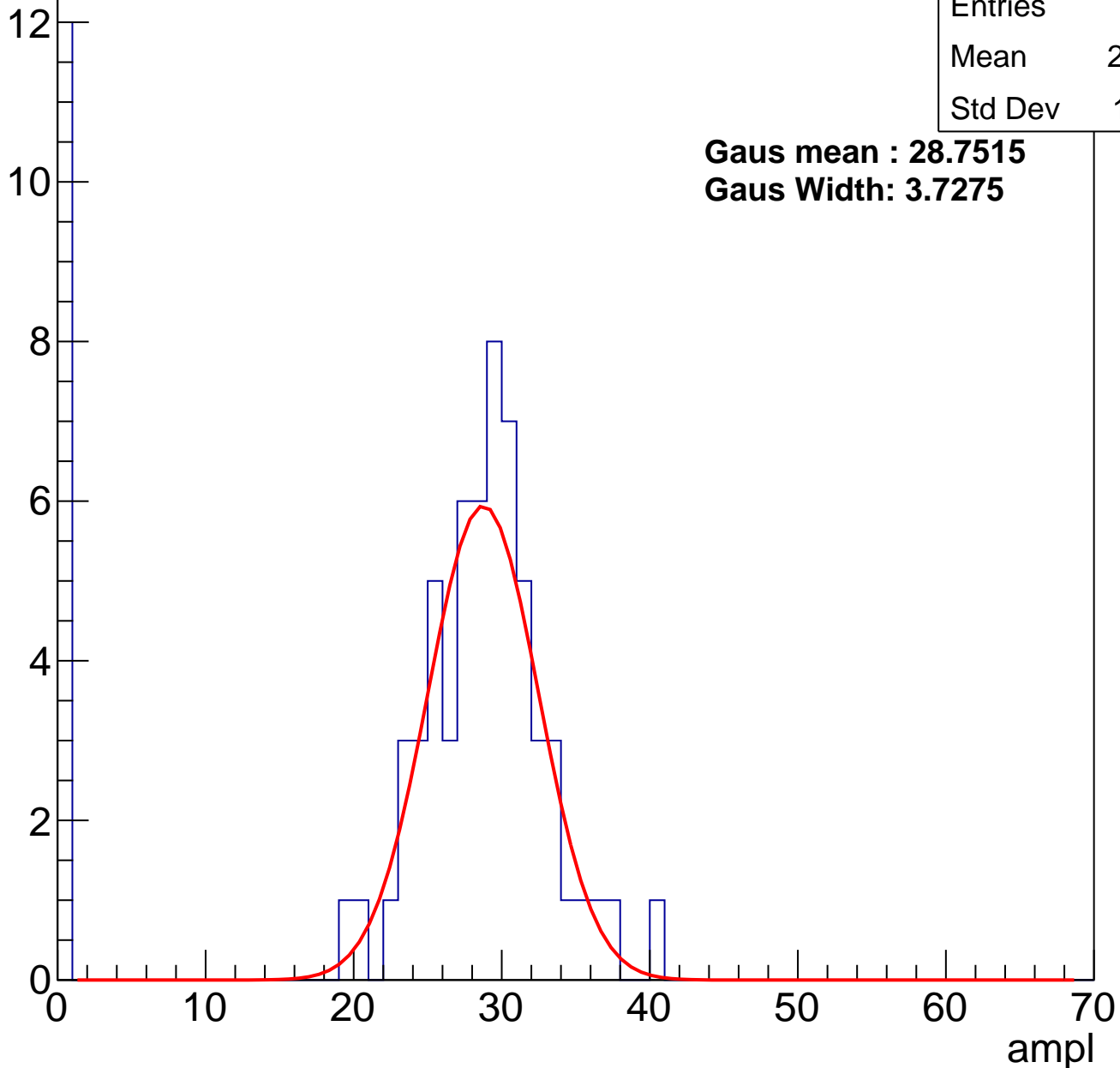
calib_packv5_041523_1651.root, FC#0, port C2

Entries	72
Mean	23.74
Std Dev	11.21

Gaus mean : 28.7515

Gaus Width: 3.7275

Entry



B1L103S, U7-ch91, adc1

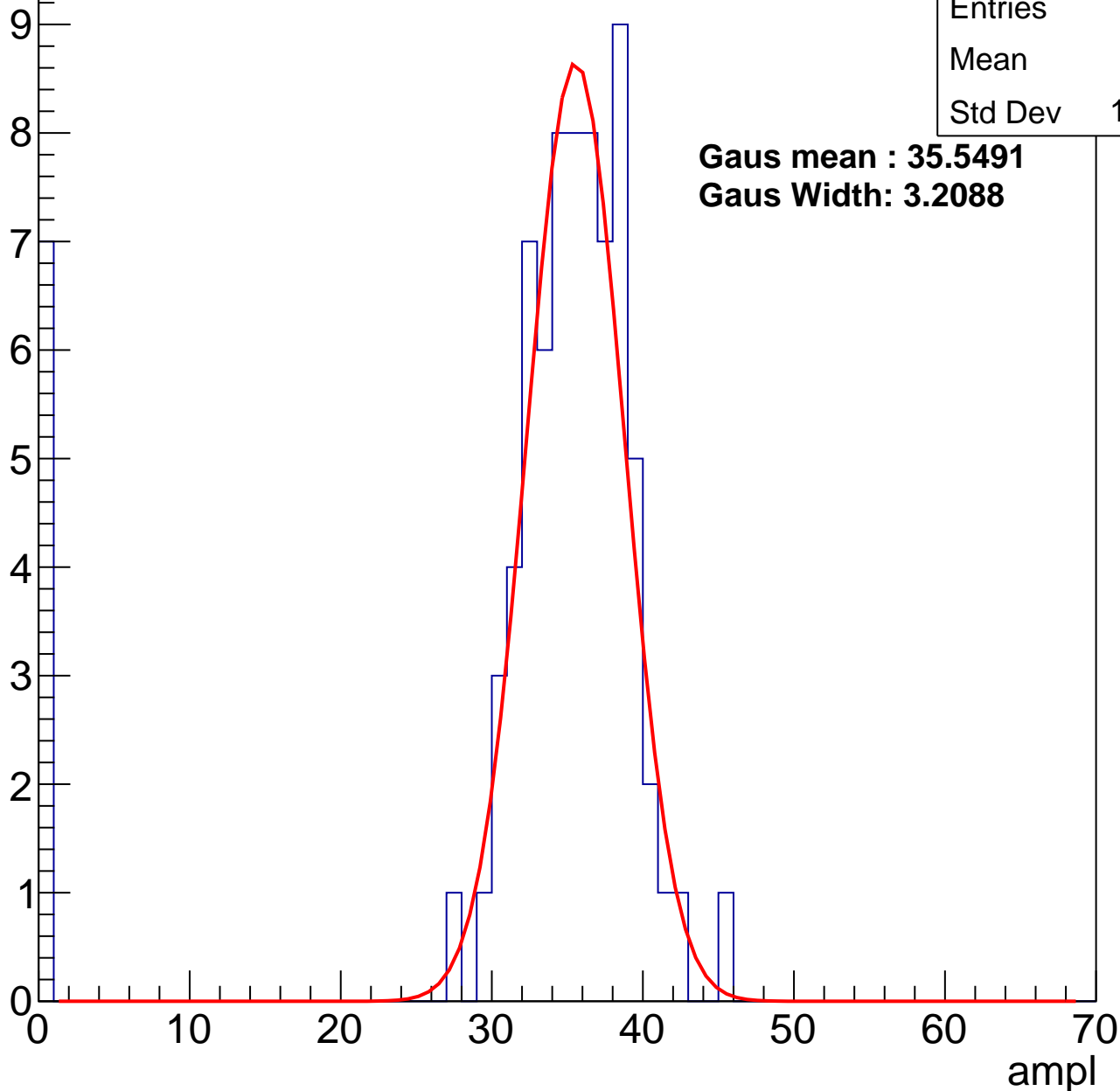
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	79
Mean	32.1
Std Dev	10.48

Gaus mean : 35.5491

Gaus Width: 3.2088



B1L103S, U7-ch91, adc2

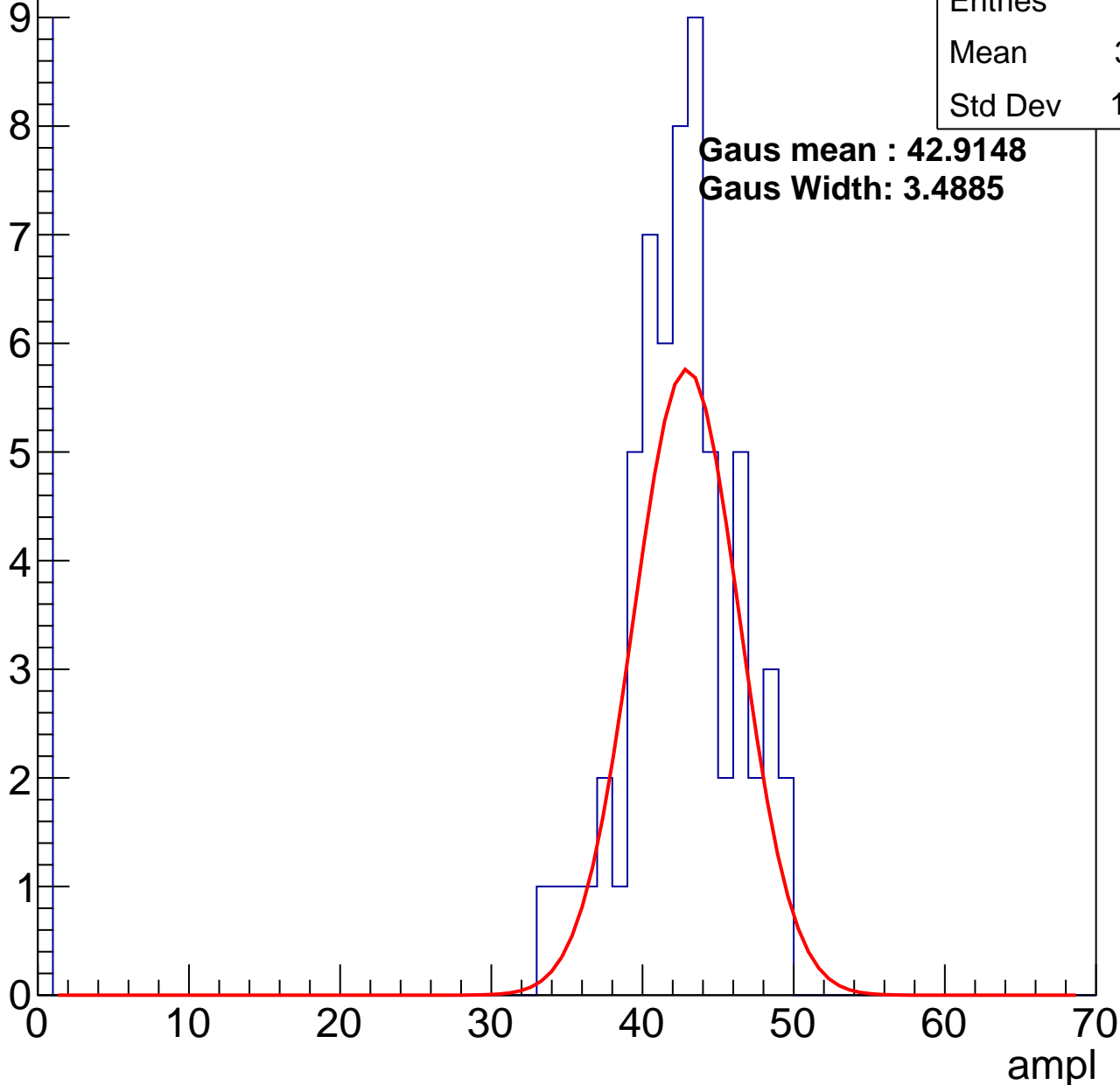
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	36.71
Std Dev	14.48

Gaus mean : 42.9148

Gaus Width: 3.4885

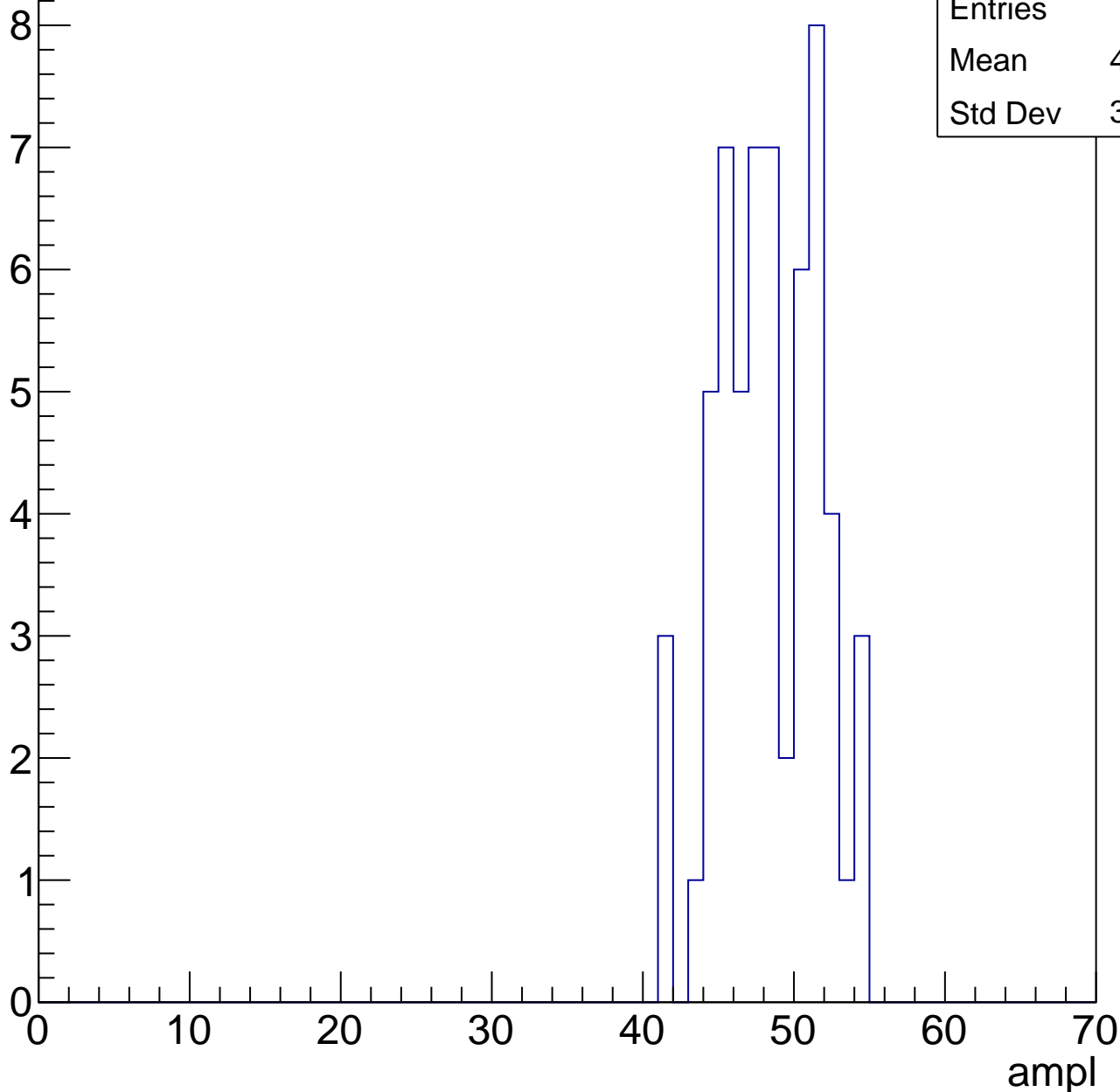


B1L103S, U7-ch91, adc3

calib_packv5_041523_1651.root, FC#0, port C2

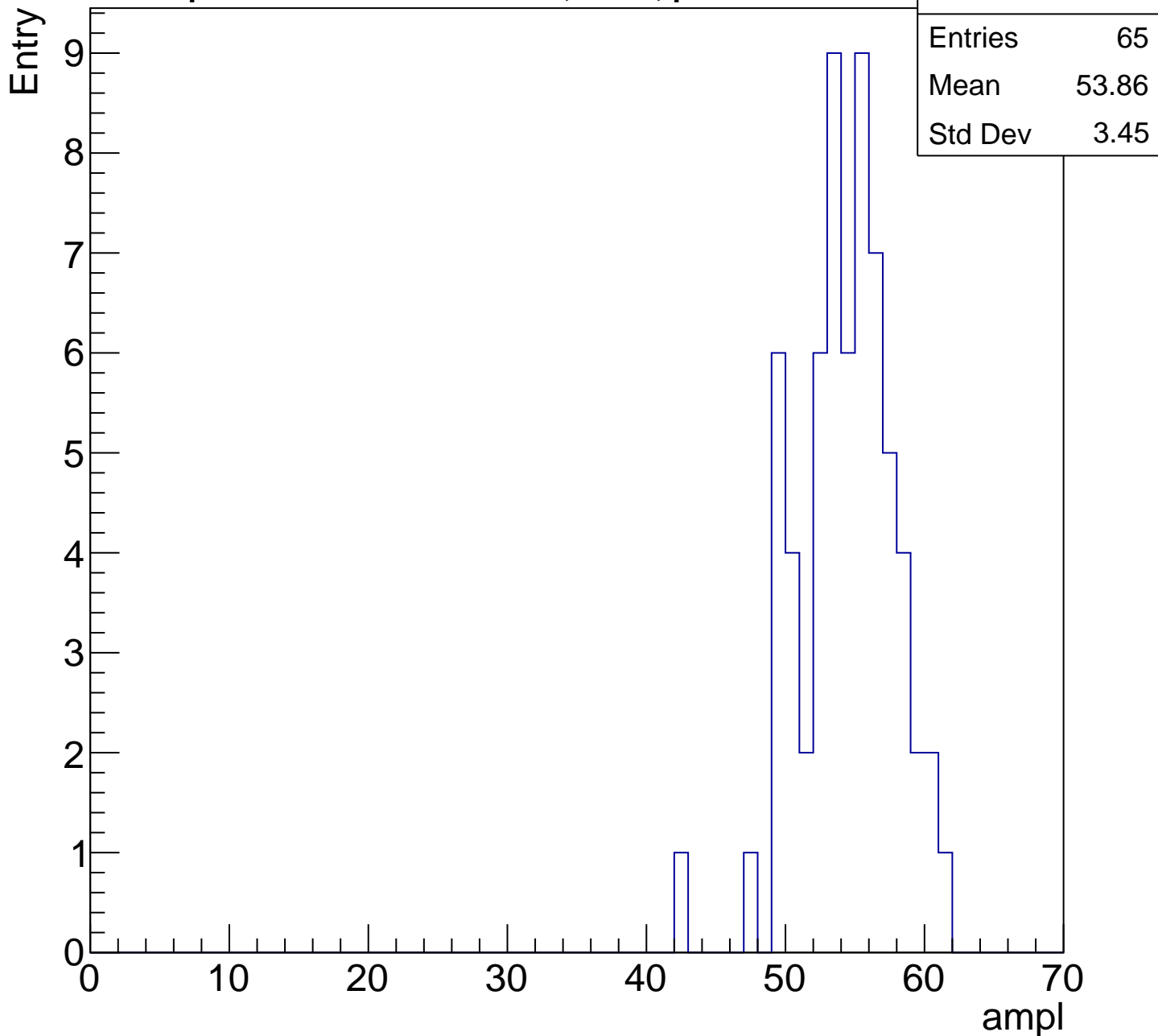
Entry

Entries	59
Mean	47.88
Std Dev	3.284



B1L103S, U7-ch91, adc4

calib_packv5_041523_1651.root, FC#0, port C2



B1L103S, U7-ch91, adc5

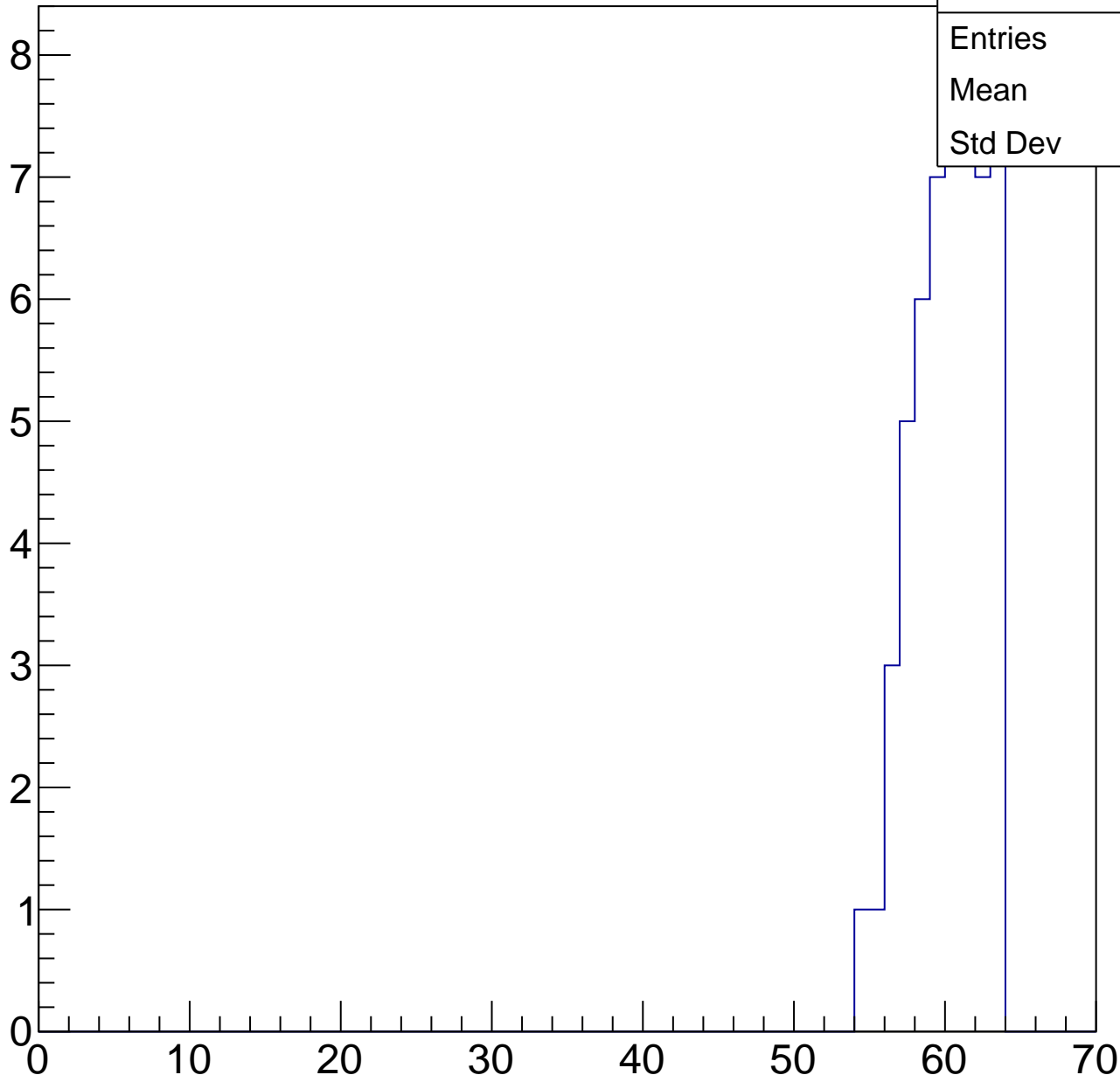
calib_packv5_041523_1651.root, FC#0, port C2

Entry

8
7
6
5
4
3
2
1
0

Entries	54
Mean	59.8
Std Dev	2.32

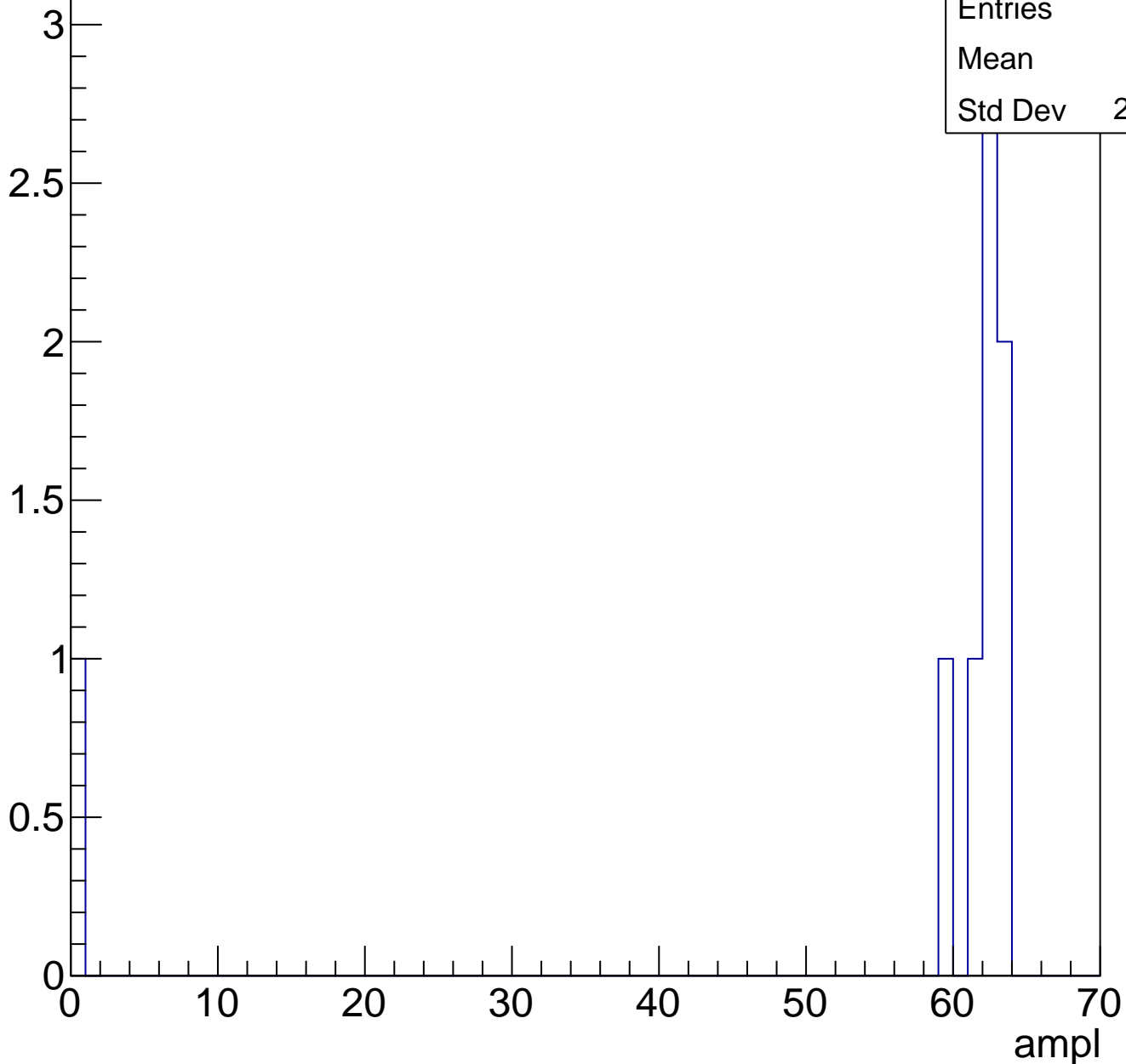
ampl



B1L103S, U7-ch91, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch91, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U7-ch92, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	94
Mean	22.64
Std Dev	9.73

Gaus mean : 26.6608

Gaus Width: 4.0797

Entry

12

10

8

6

4

2

0

0

10

20

30

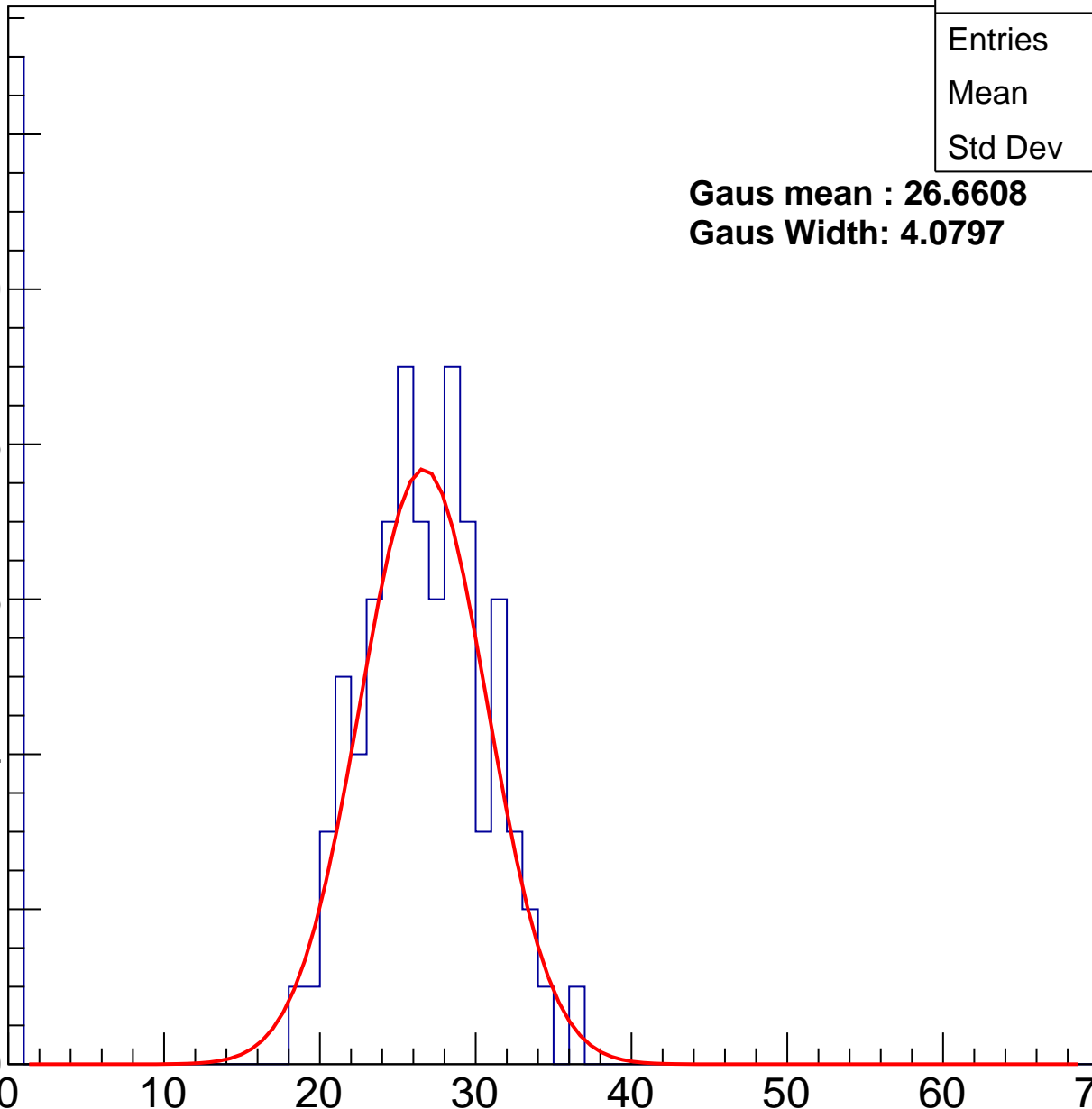
40

50

60

70

ampl



B1L103S, U7-ch92, adc1

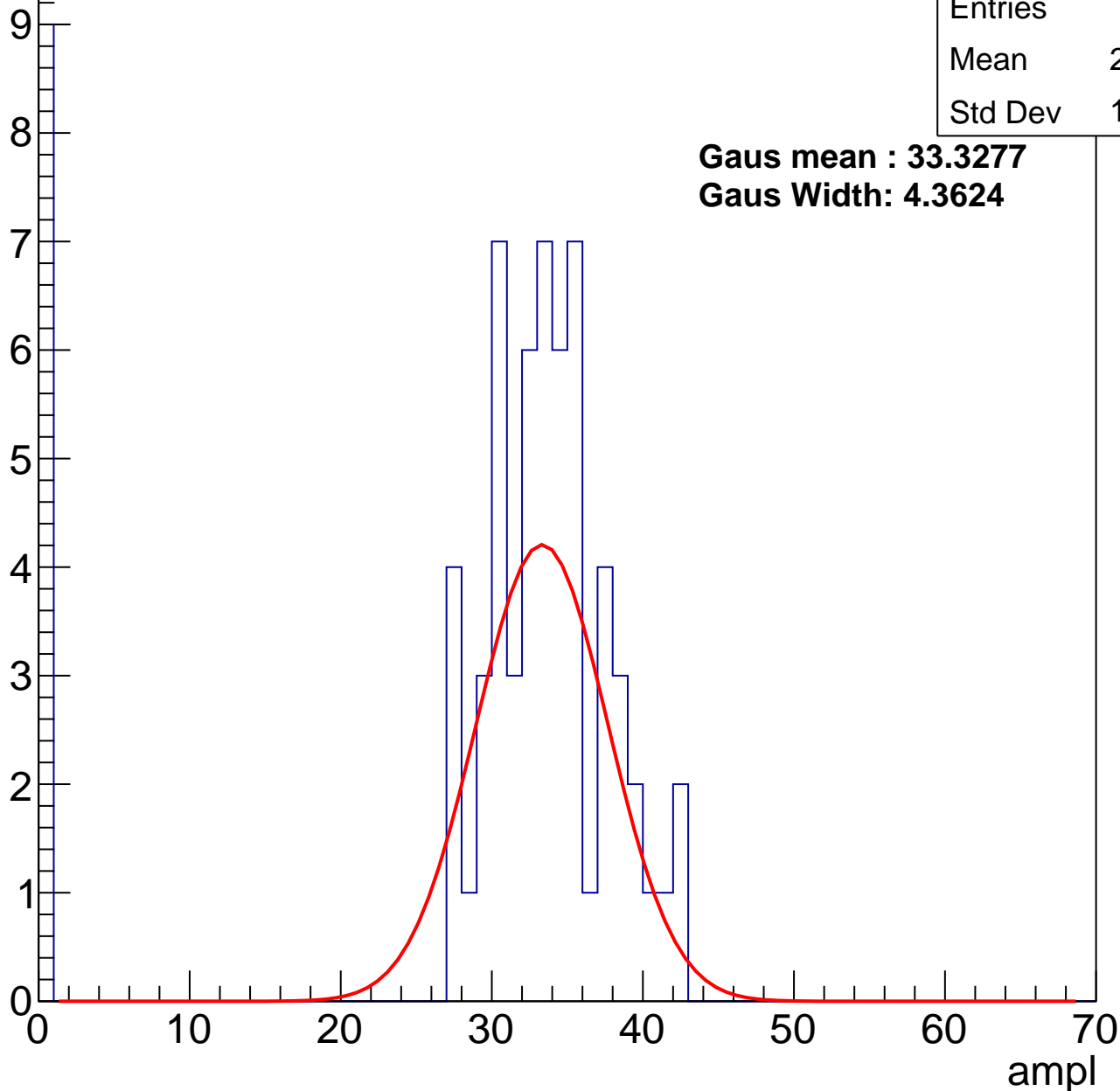
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	28.94
Std Dev	11.92

Gaus mean : 33.3277

Gaus Width: 4.3624



B1L103S, U7-ch92, adc2

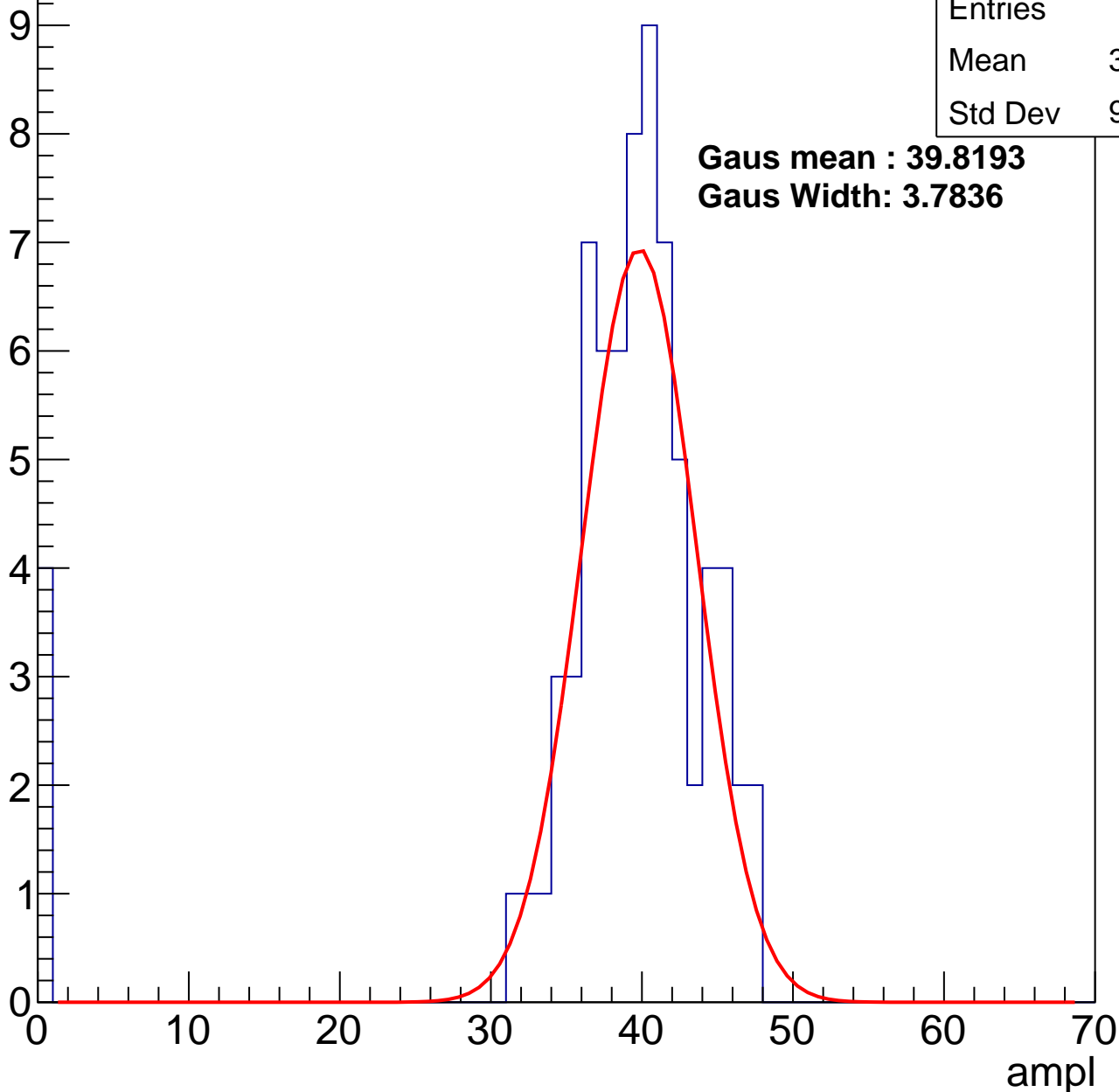
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	37.36
Std Dev	9.544

Gaus mean : 39.8193

Gaus Width: 3.7836

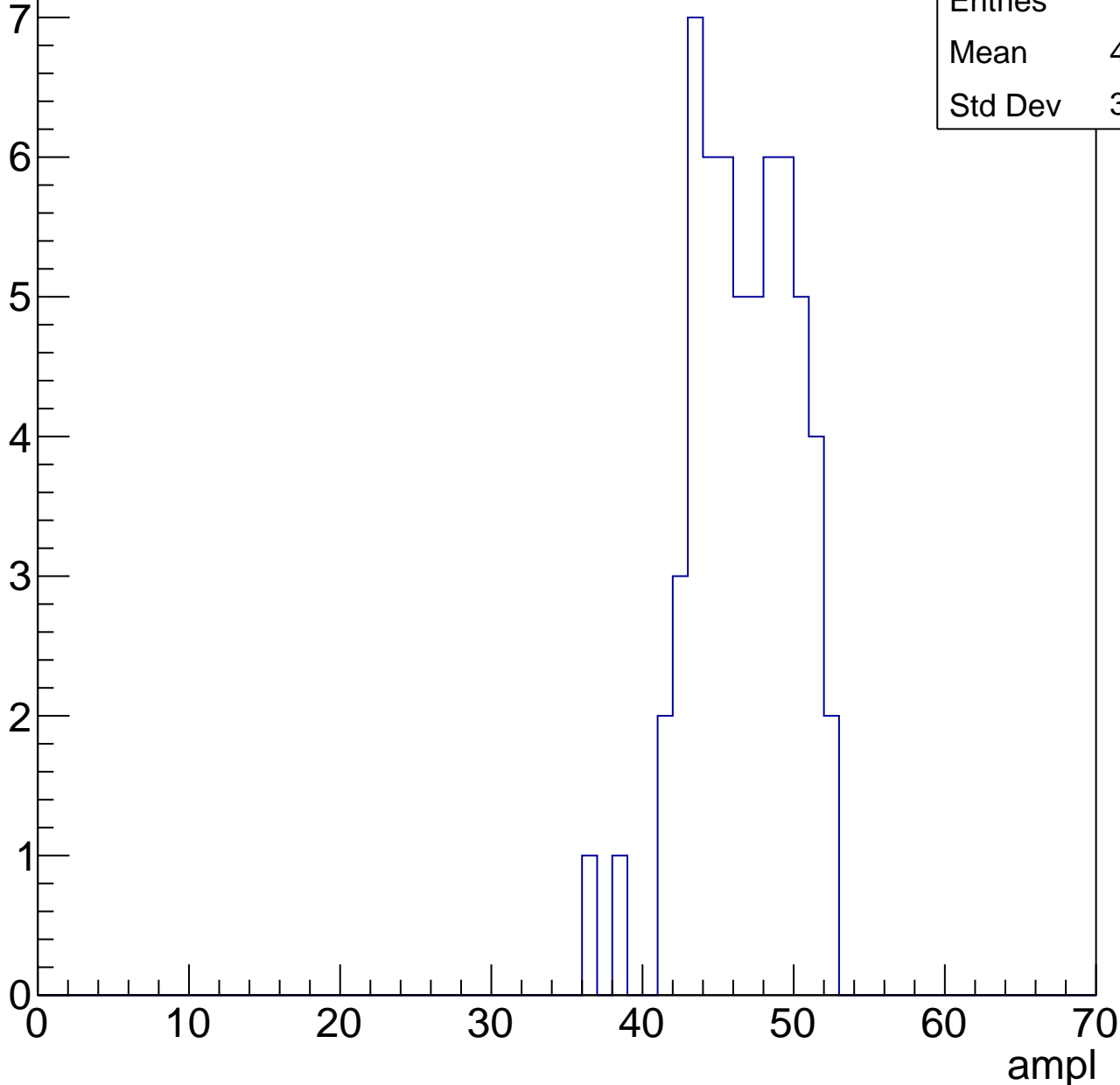


B1L103S, U7-ch92, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	46.14
Std Dev	3.417

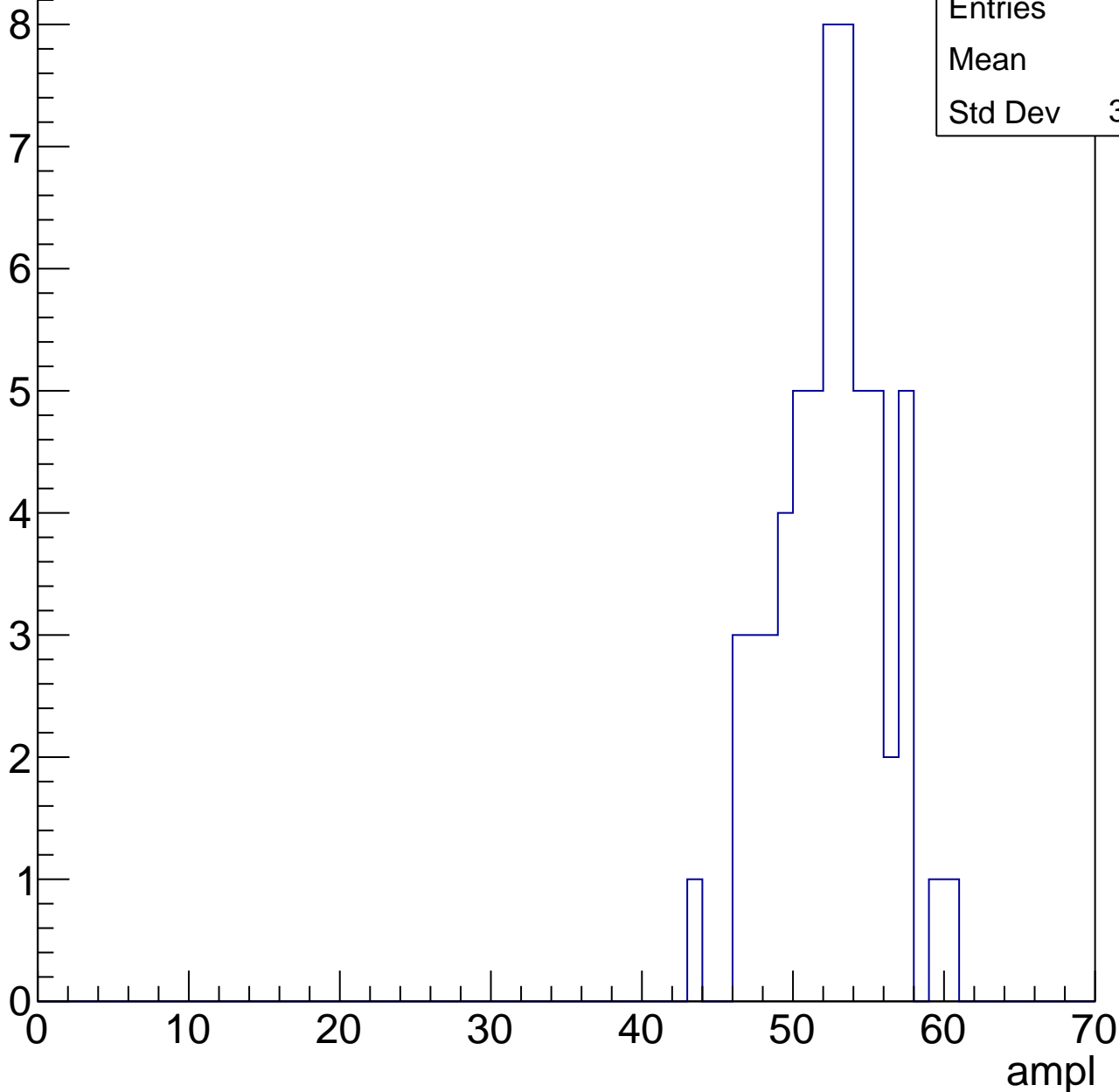


B1L103S, U7-ch92, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	52
Std Dev	3.484

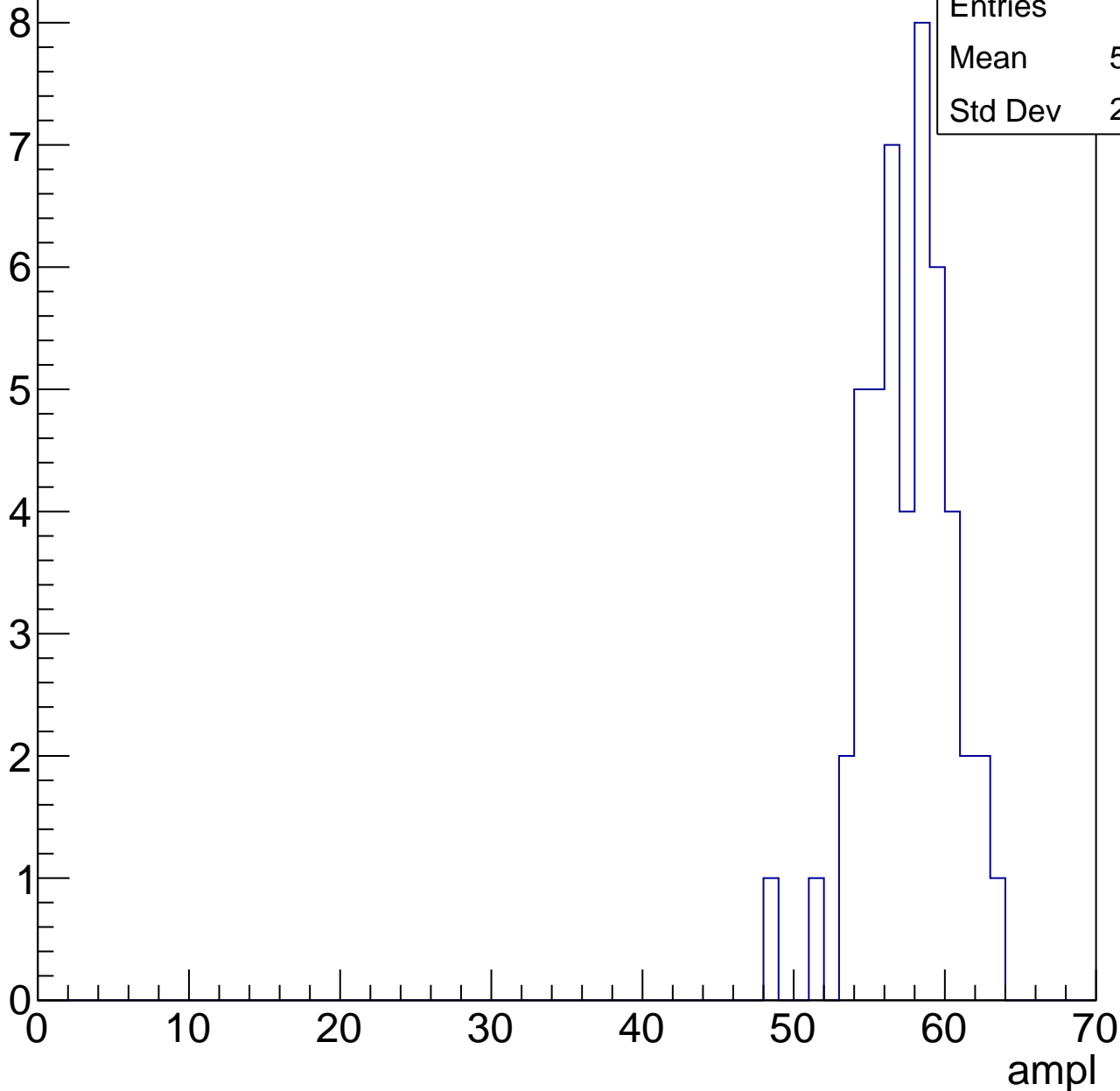


B1L103S, U7-ch92, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	48
Mean	57.02
Std Dev	2.912

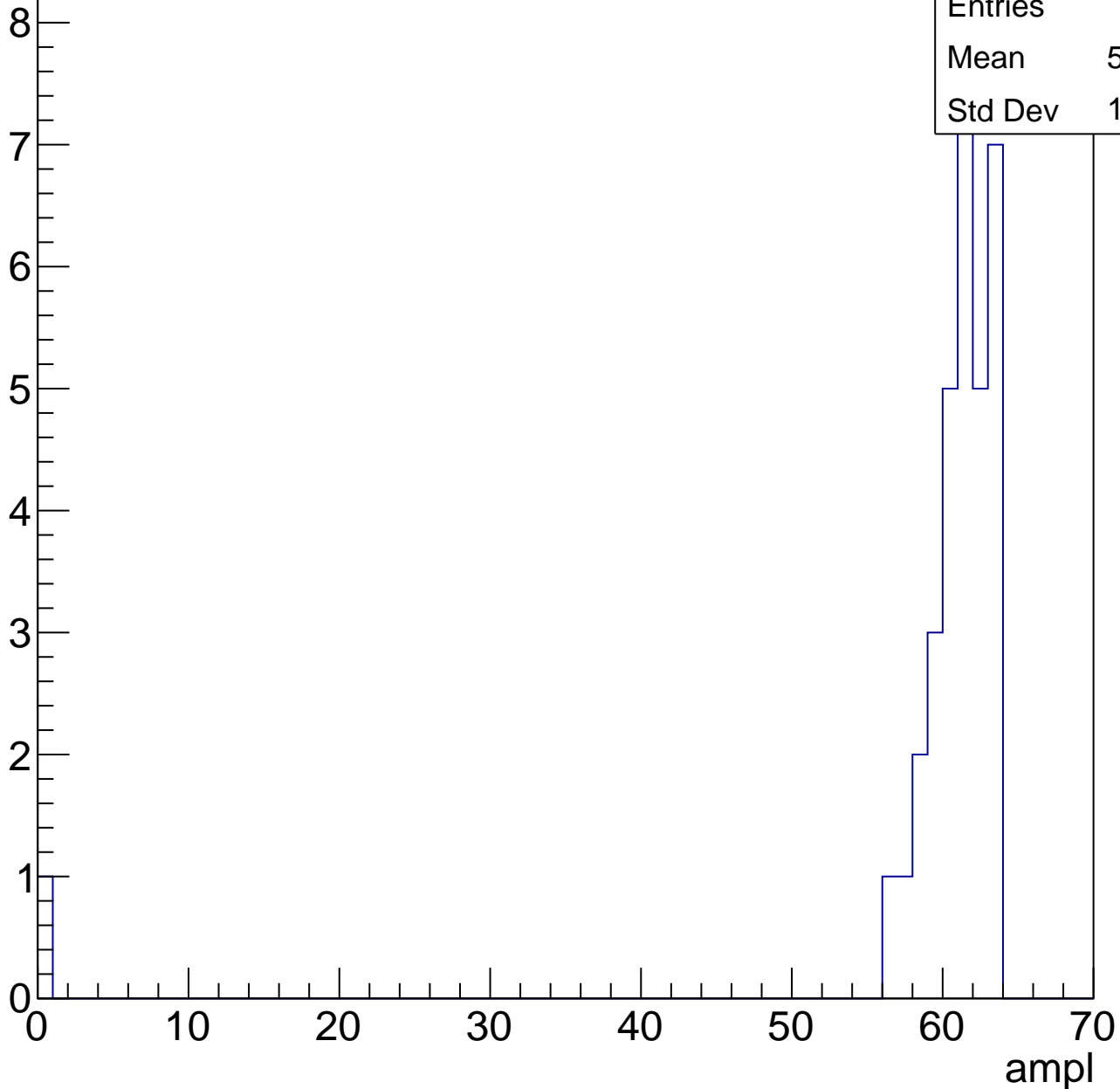


B1L103S, U7-ch92, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	33
Mean	58.94
Std Dev	10.57



B1L103S, U7-ch92, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	24
Mean	13
Std Dev	25.34

ampl

0 10 20 30 40 50 60 70

B1L103S, U7-ch93, adc0

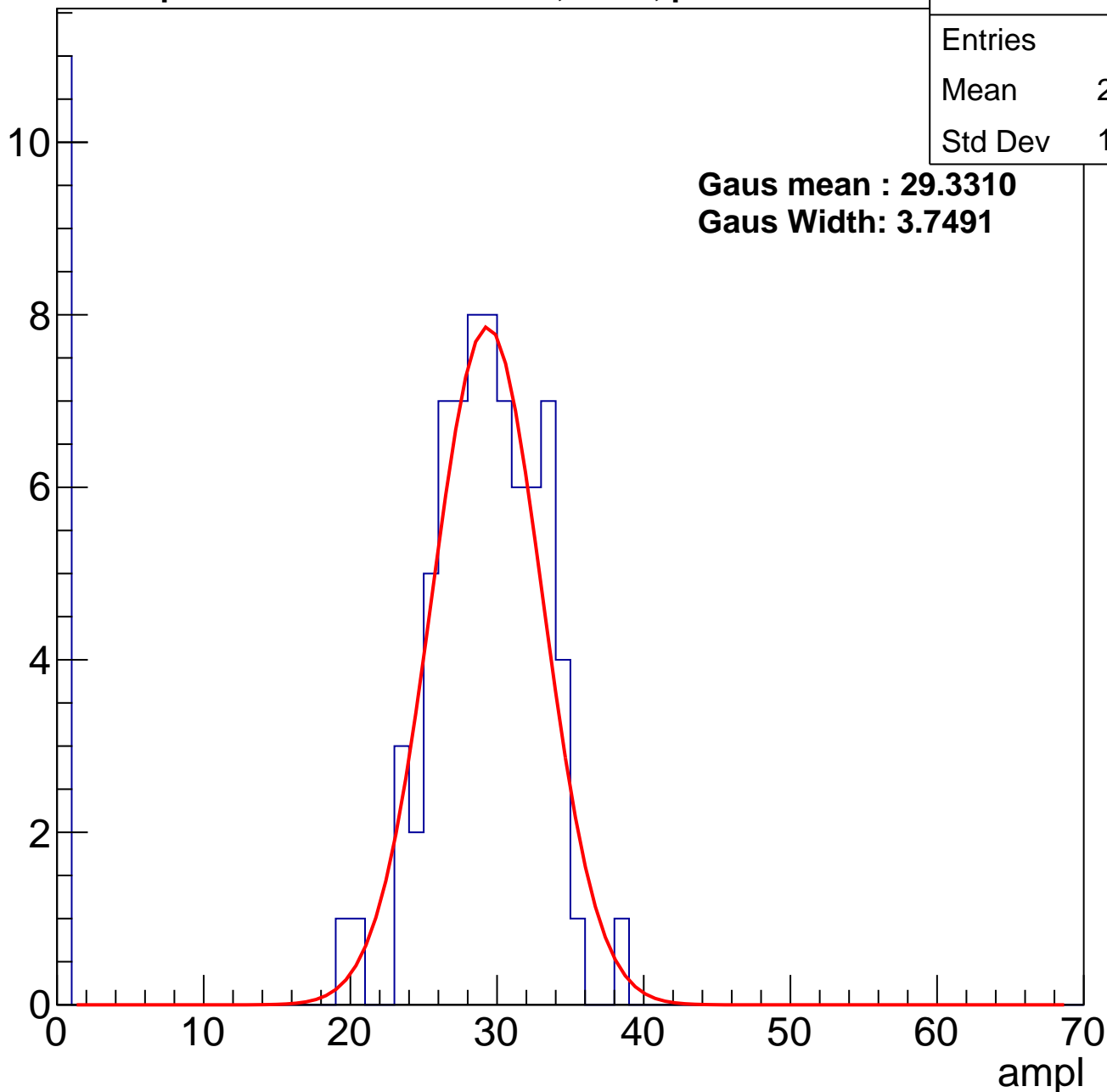
calib_packv5_041523_1651.root, FC#0, port C2

Entries	85
Mean	25.13
Std Dev	10.24

Gaus mean : 29.3310

Gaus Width: 3.7491

Entry



B1L103S, U7-ch93, adc1

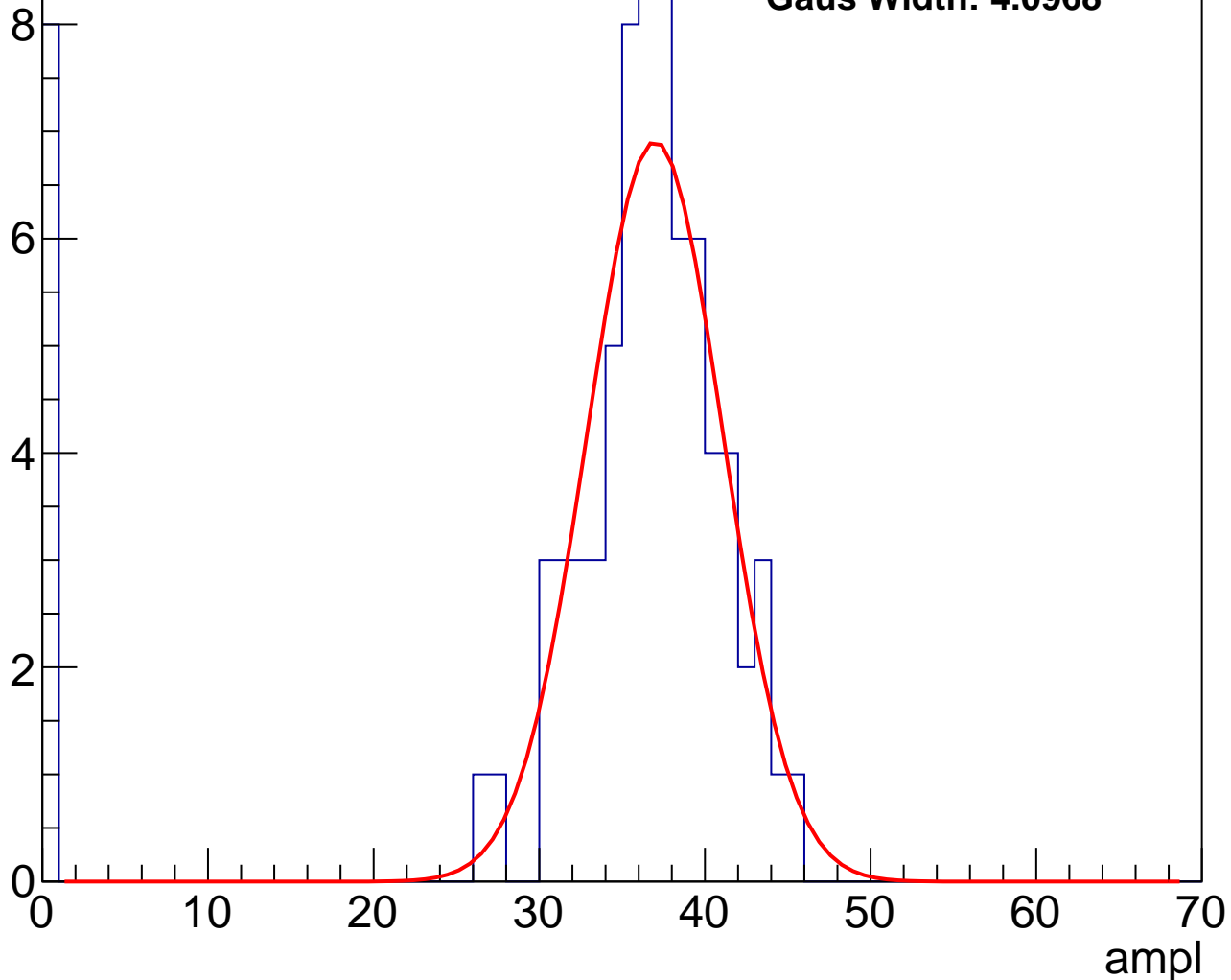
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	81
Mean	32.88
Std Dev	11.47

Gaus mean : 36.9885

Gaus Width: 4.0968



B1L103S, U7-ch93, adc2

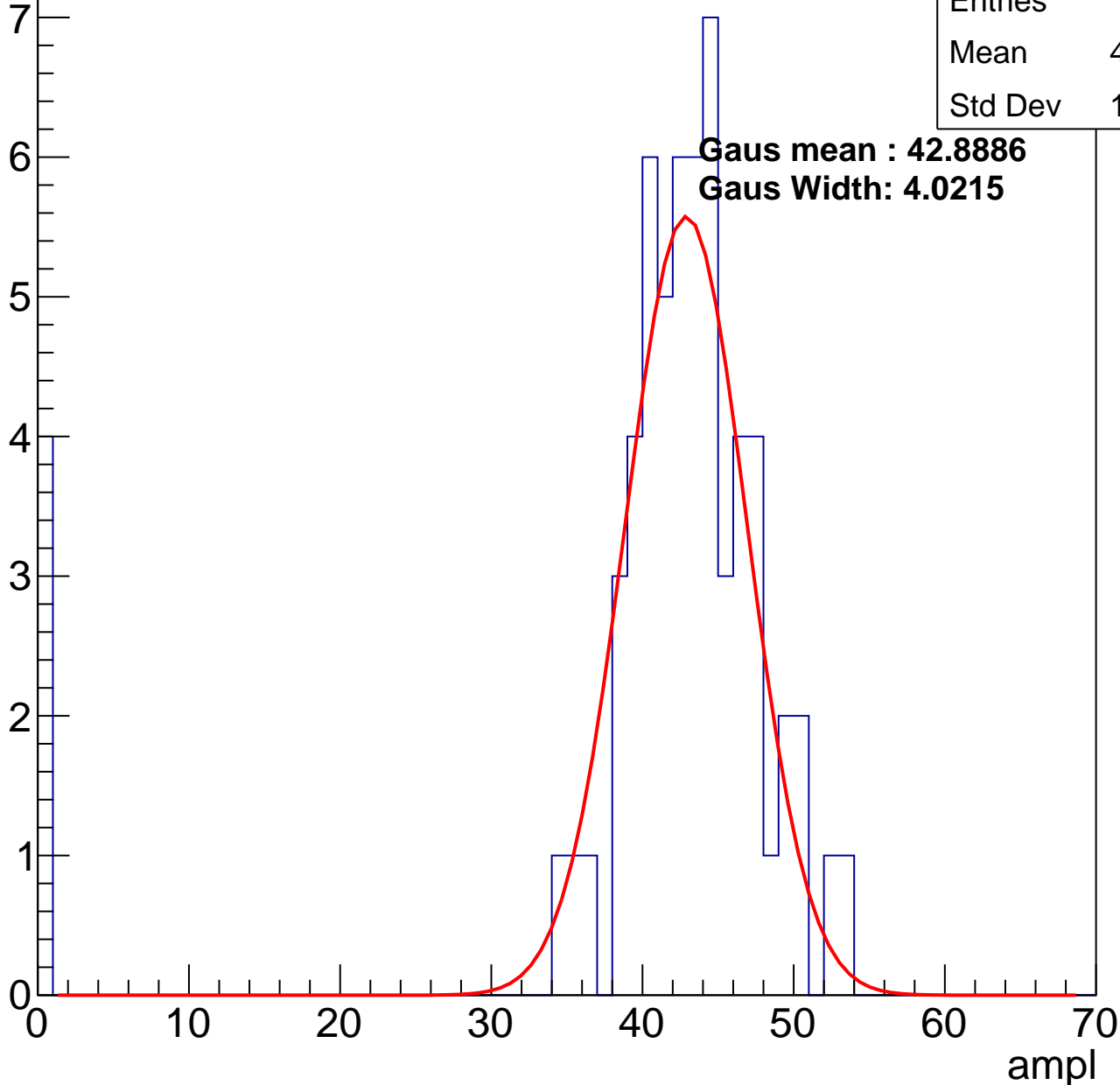
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	40.26
Std Dev	11.24

Gaus mean : 42.8886

Gaus Width: 4.0215

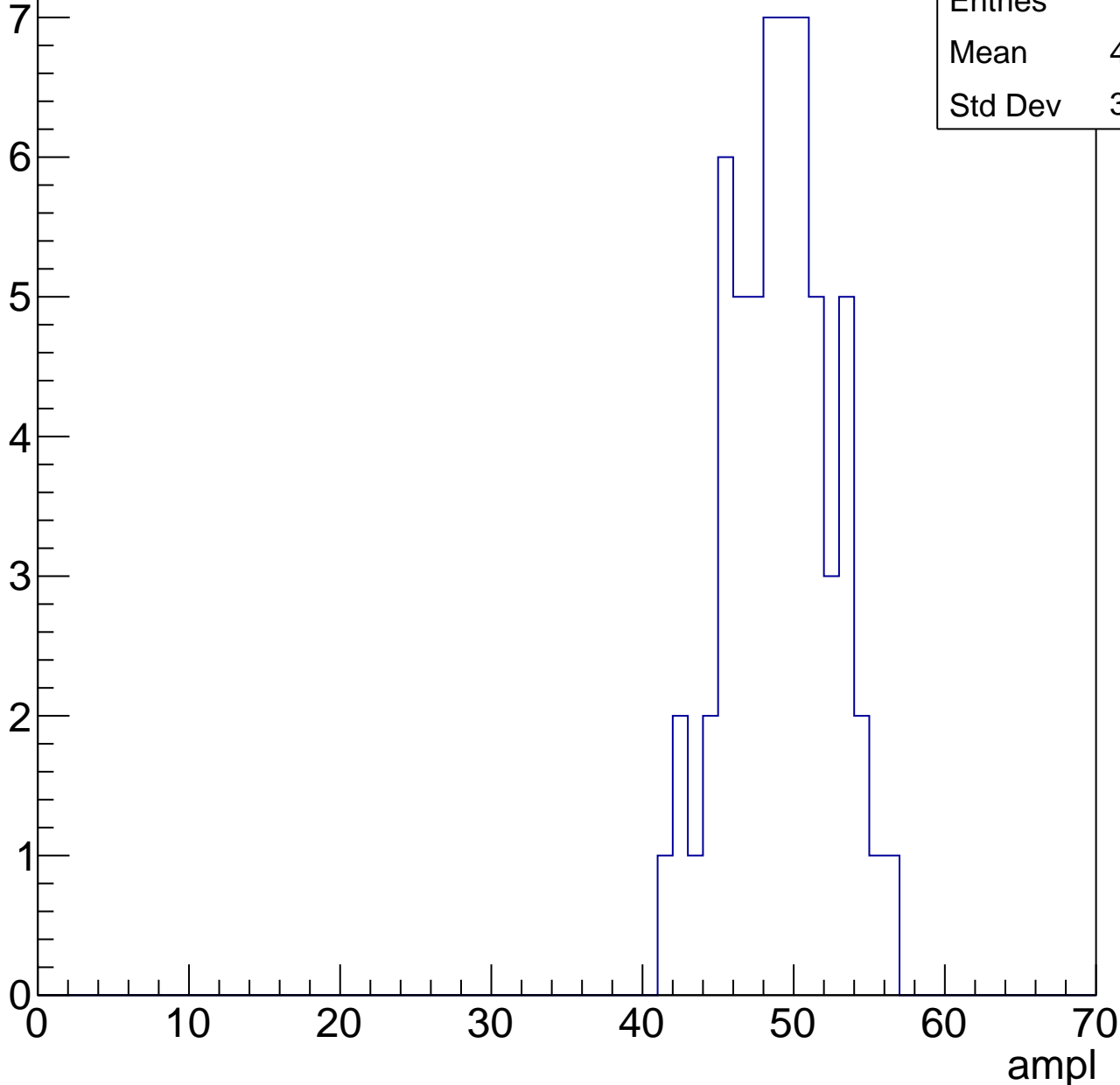


B1L103S, U7-ch93, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	48.58
Std Dev	3.353

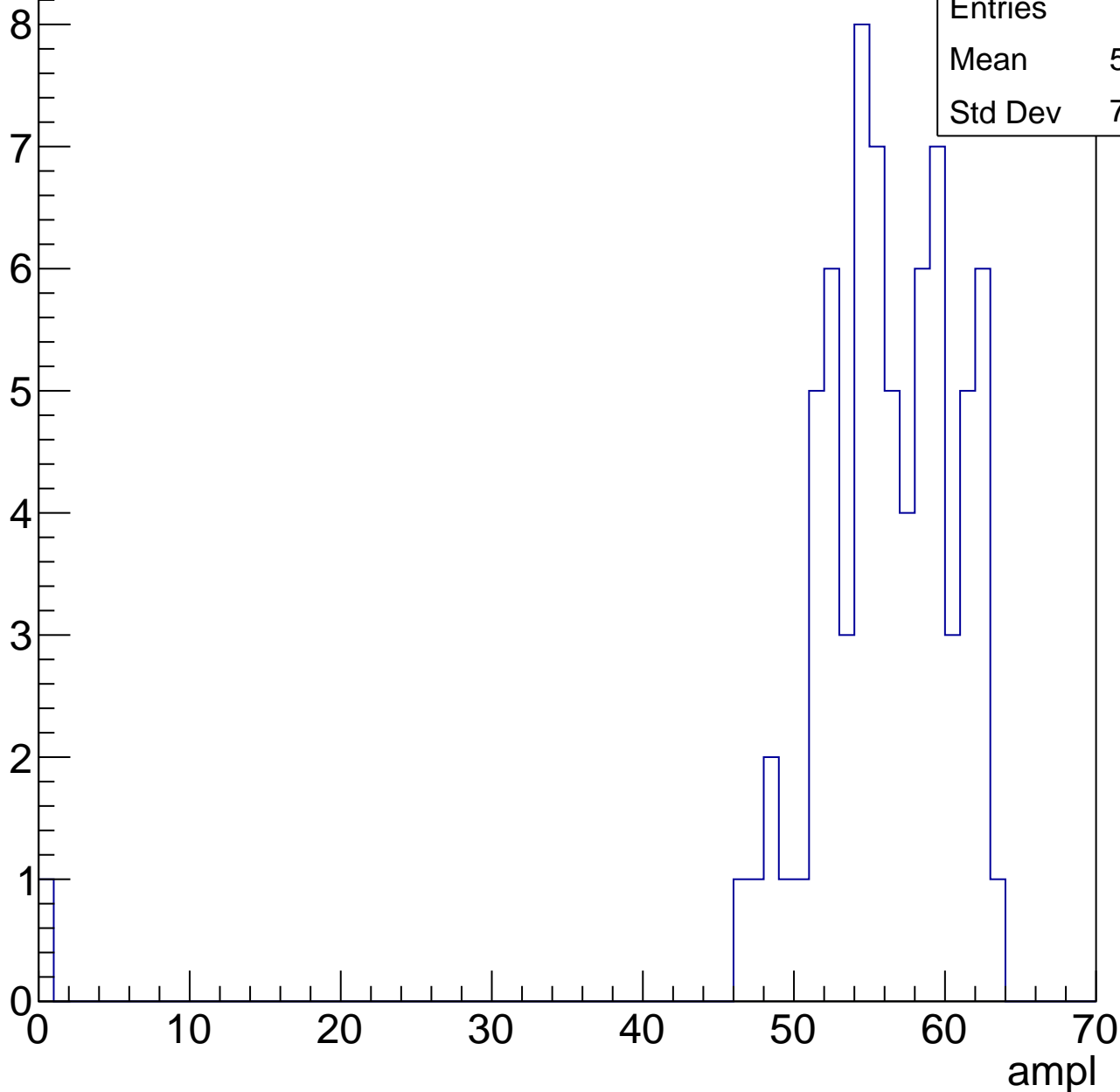


B1L103S, U7-ch93, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	55.07
Std Dev	7.659

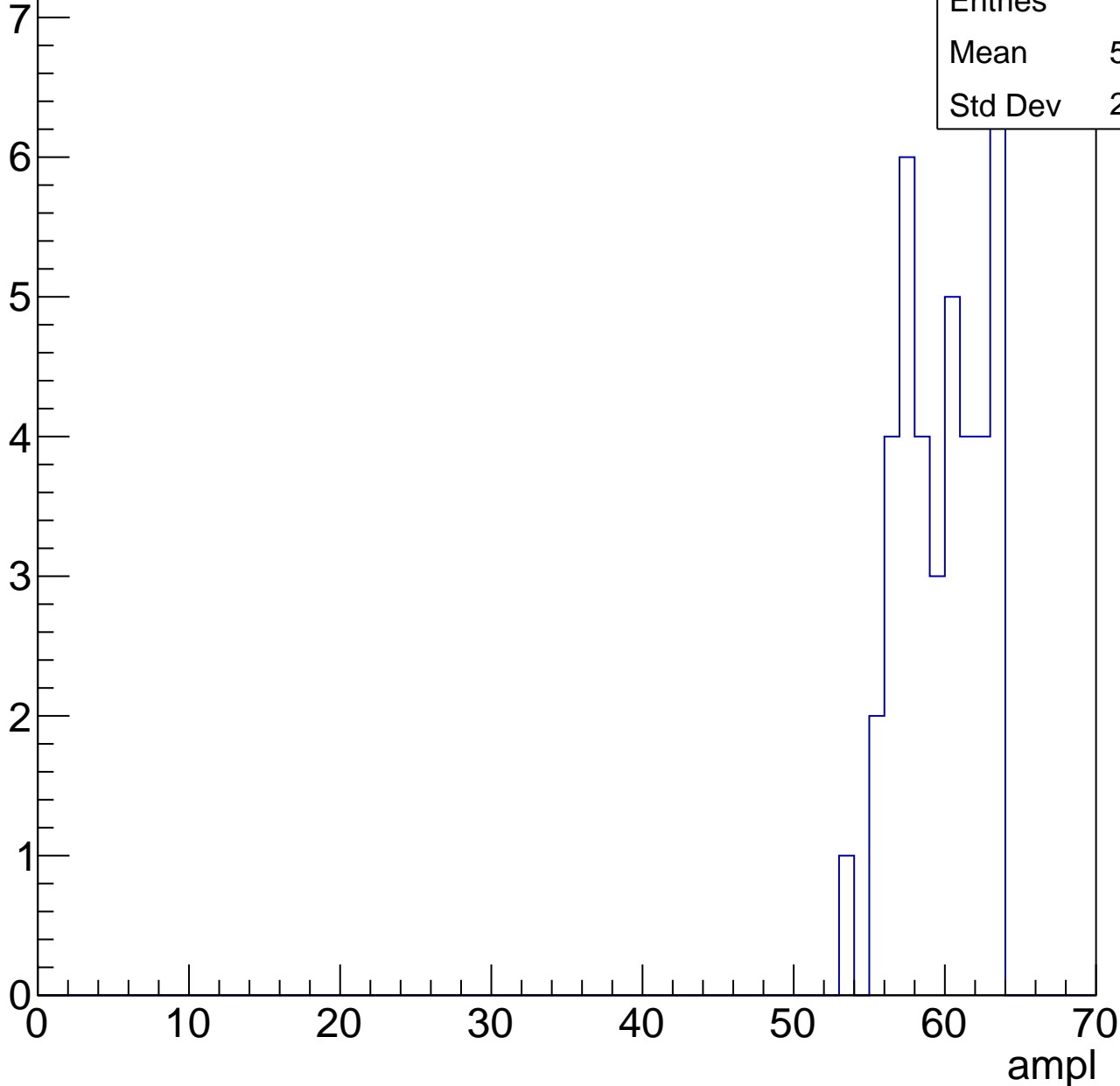


B1L103S, U7-ch93, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	40
Mean	59.27
Std Dev	2.729



B1L103S, U7-ch93, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	5
Mean	61.4
Std Dev	1.356

ampl

0 10 20 30 40 50 60 70

B1L103S, U7-ch93, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U7-ch94, adc0

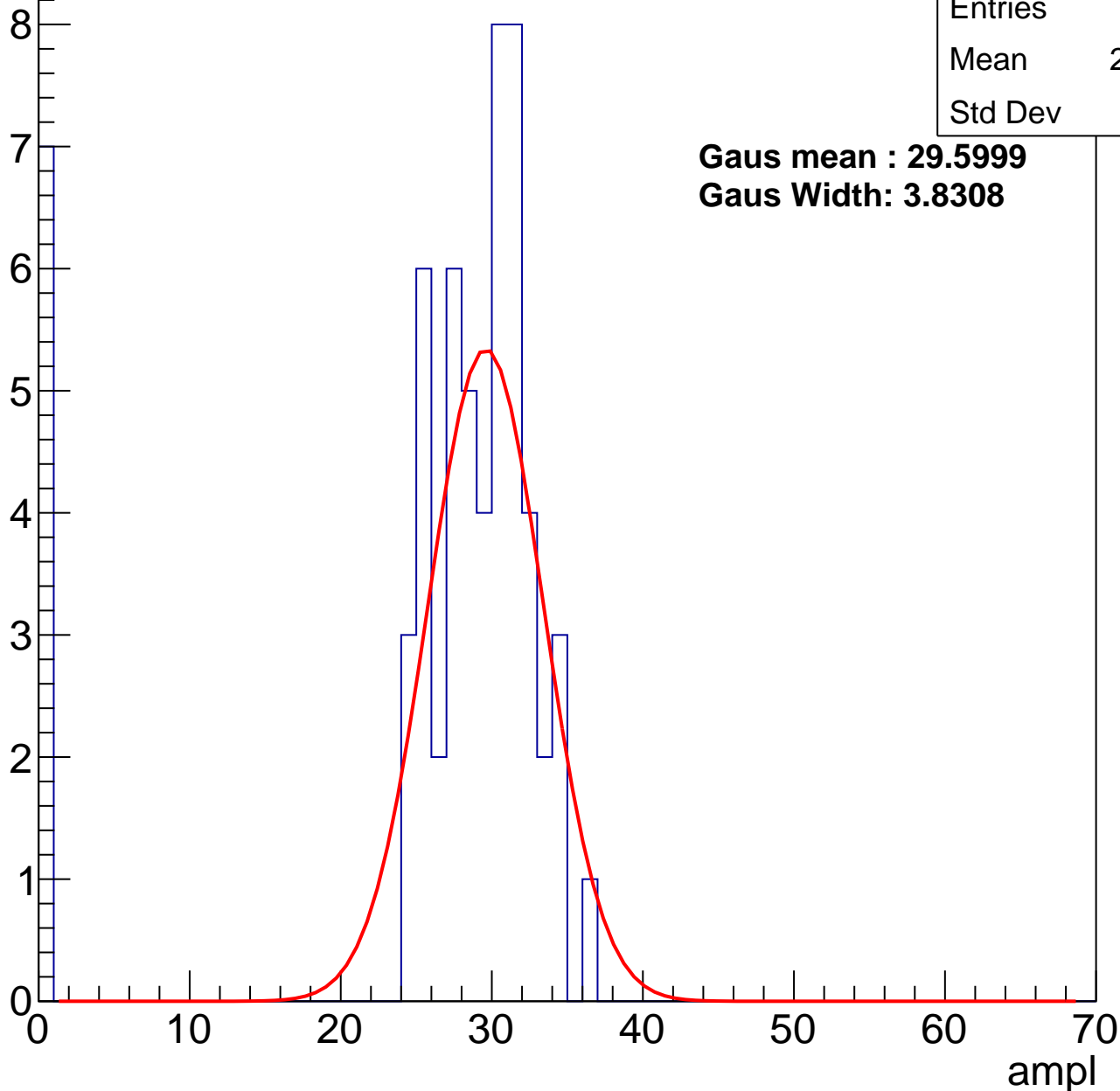
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	25.63
Std Dev	9.8

Gaus mean : 29.5999

Gaus Width: 3.8308



B1L103S, U7-ch94, adc1

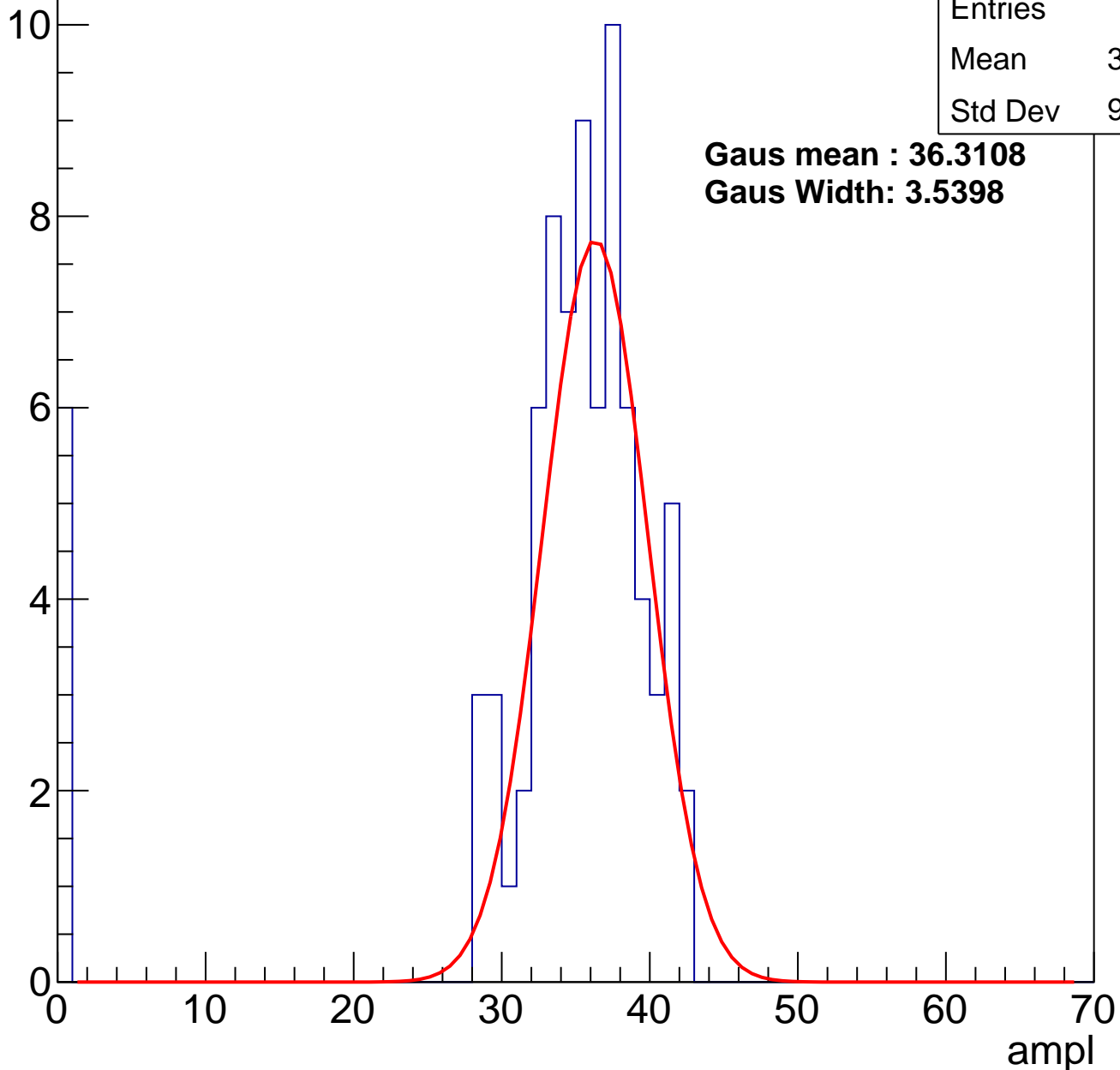
calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	32.73
Std Dev	9.847

Gaus mean : 36.3108

Gaus Width: 3.5398

Entry



B1L103S, U7-ch94, adc2

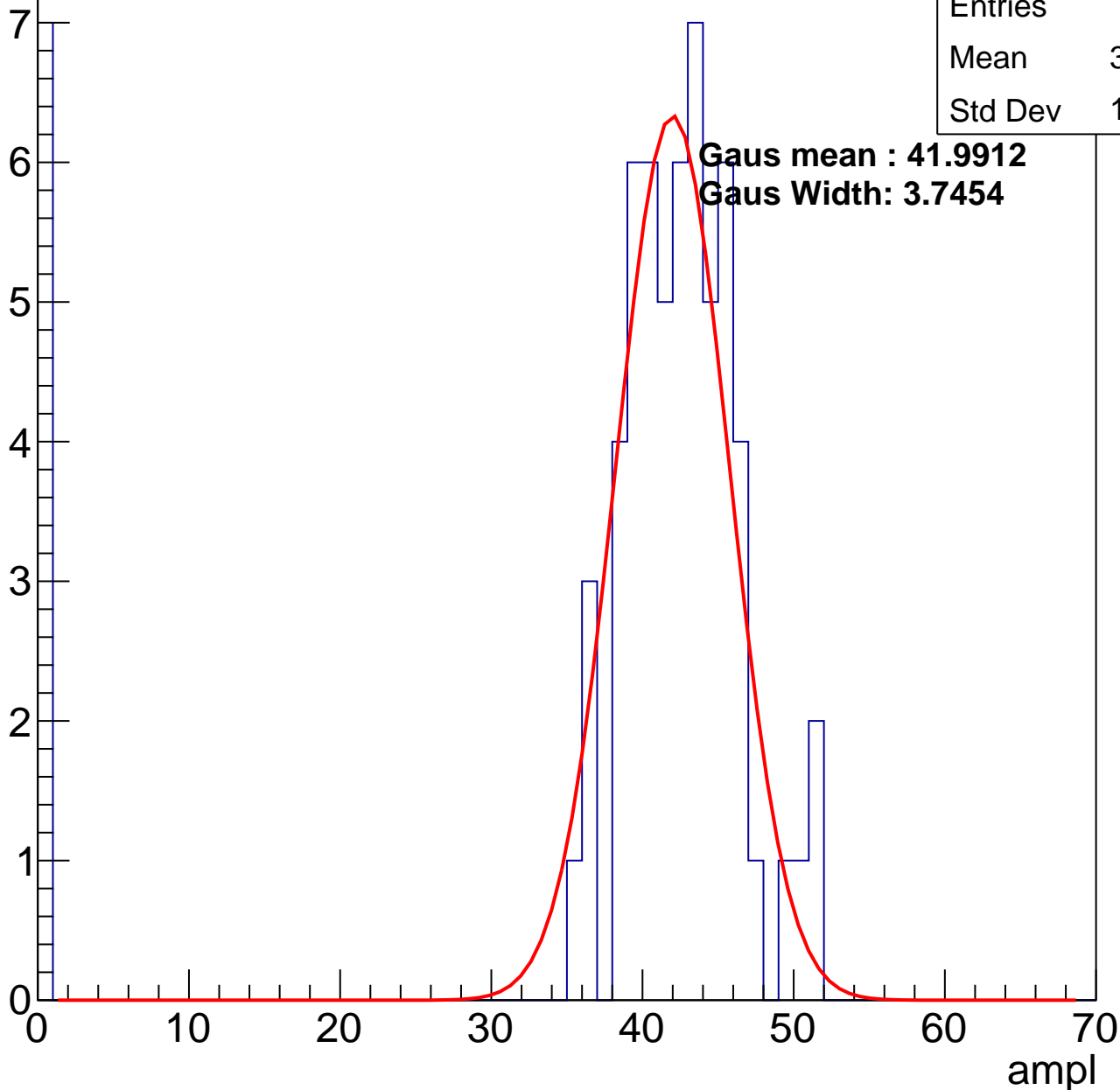
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	37.68
Std Dev	13.52

Gaus mean : 41.9912

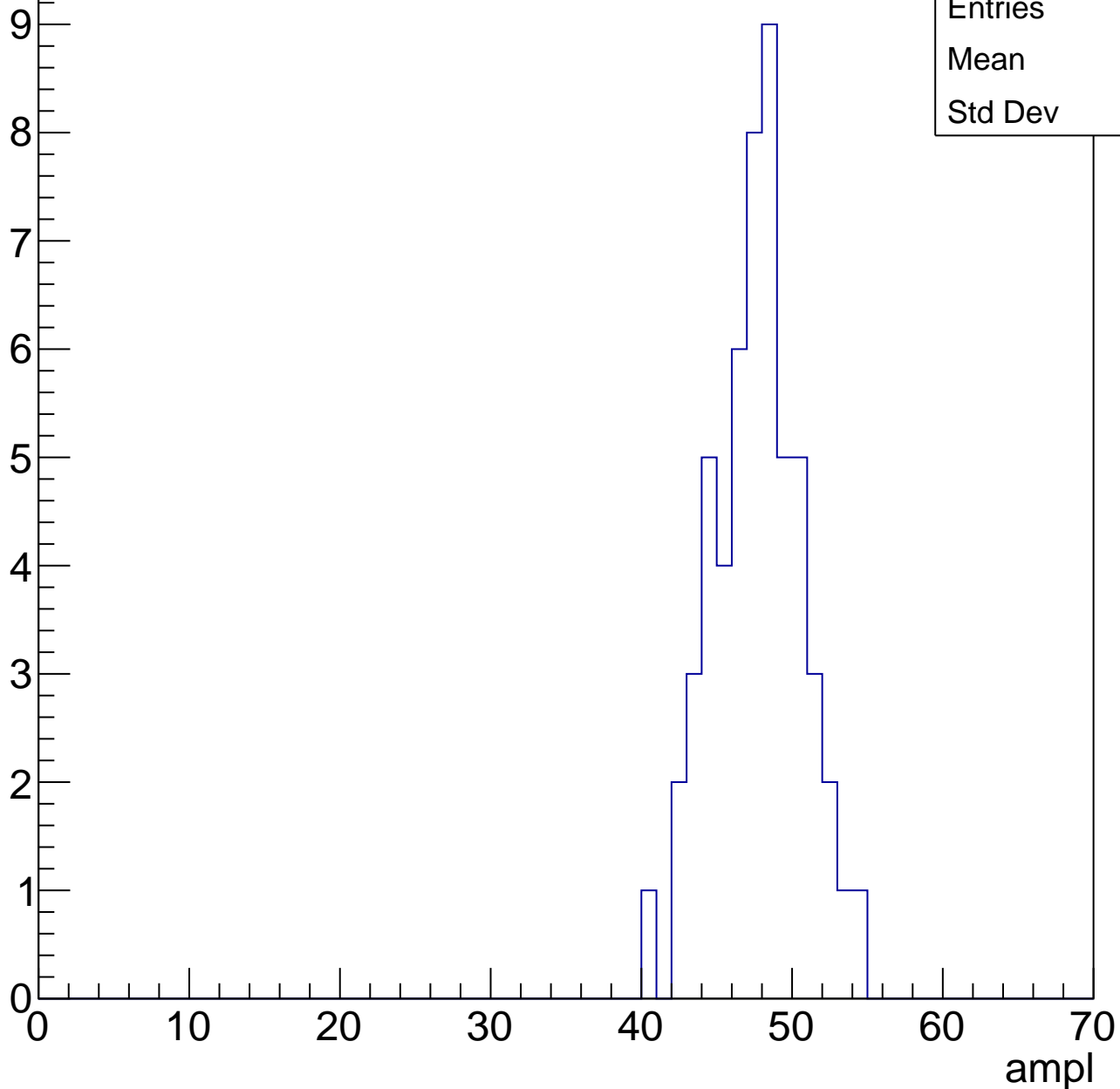
Gaus Width: 3.7454



B1L103S, U7-ch94, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

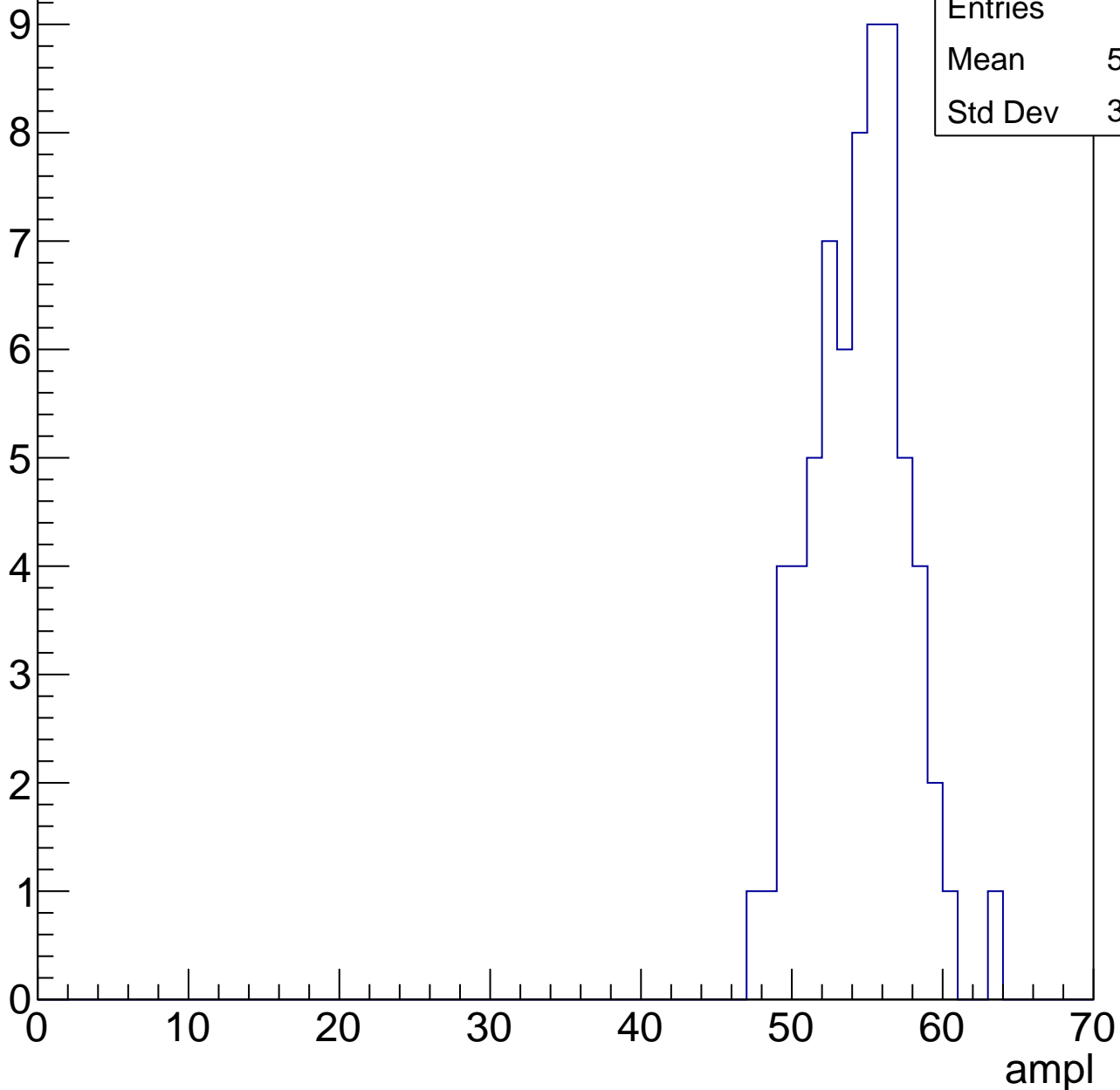


B1L103S, U7-ch94, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	53.99
Std Dev	3.112

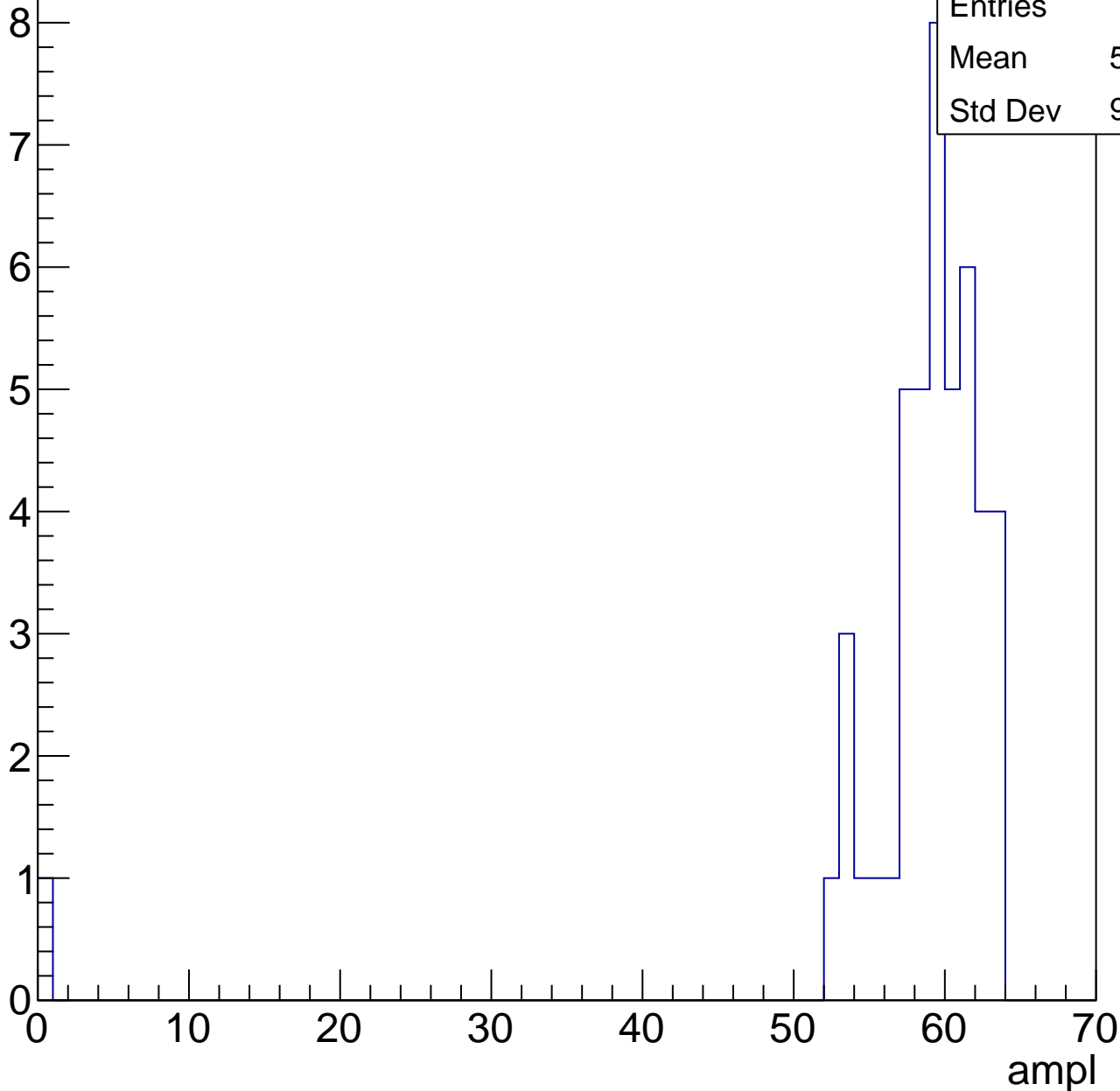


B1L103S, U7-ch94, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	45
Mean	57.53
Std Dev	9.123

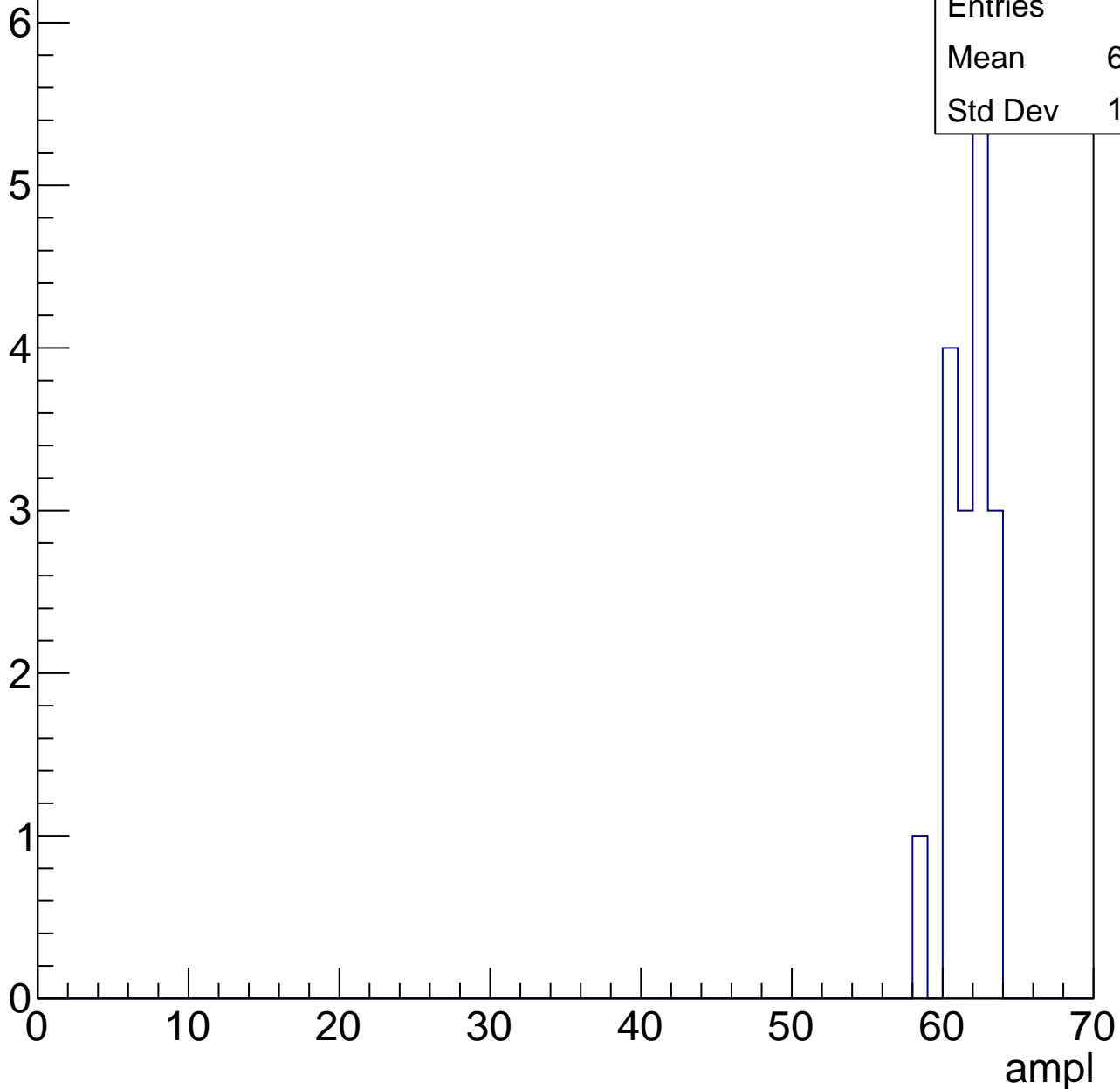


B1L103S, U7-ch94, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

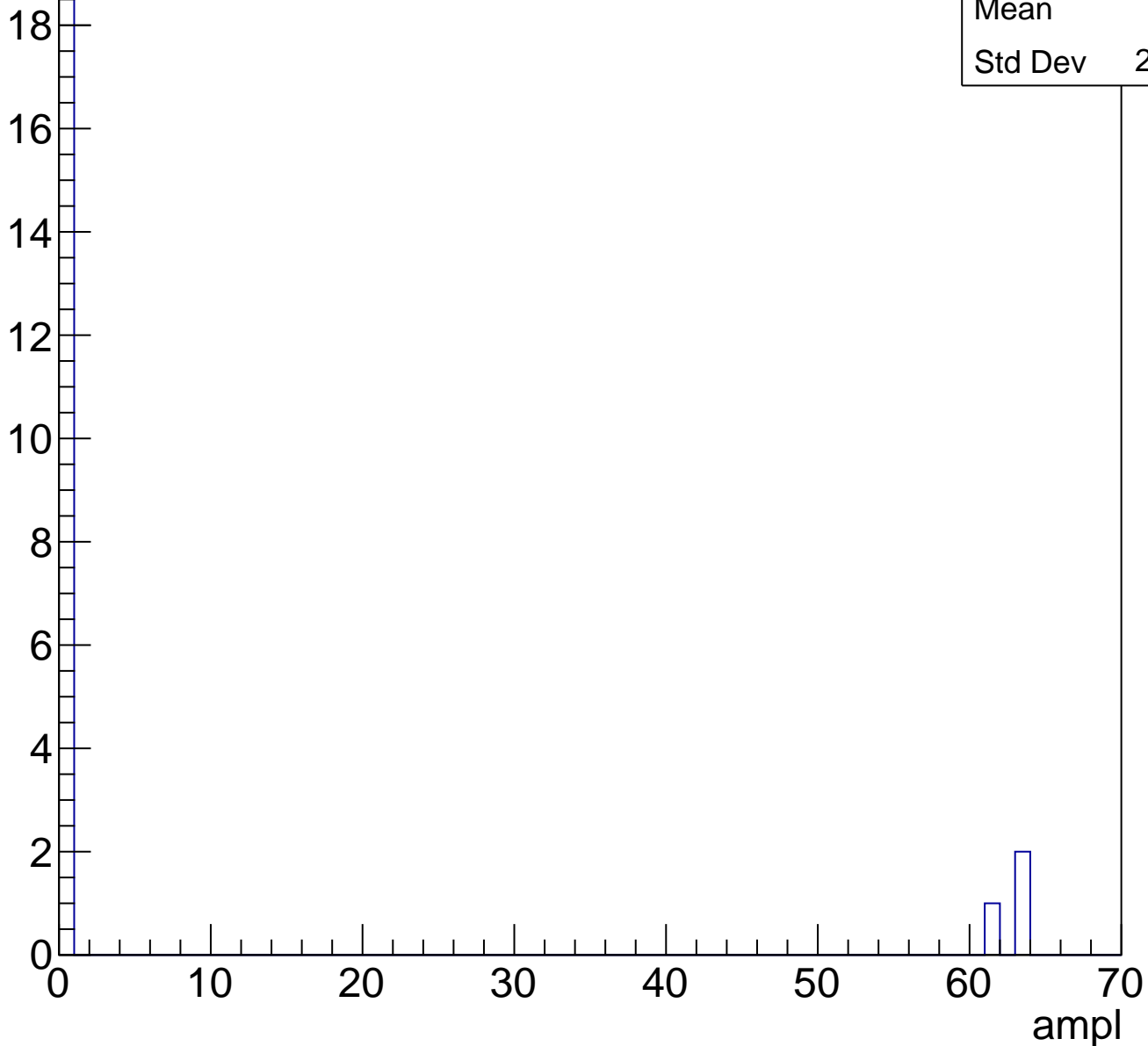
Entries	17
Mean	61.29
Std Dev	1.318



B1L103S, U7-ch94, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	22
Mean	8.5
Std Dev	21.39

B1L103S, U7-ch95, adc0

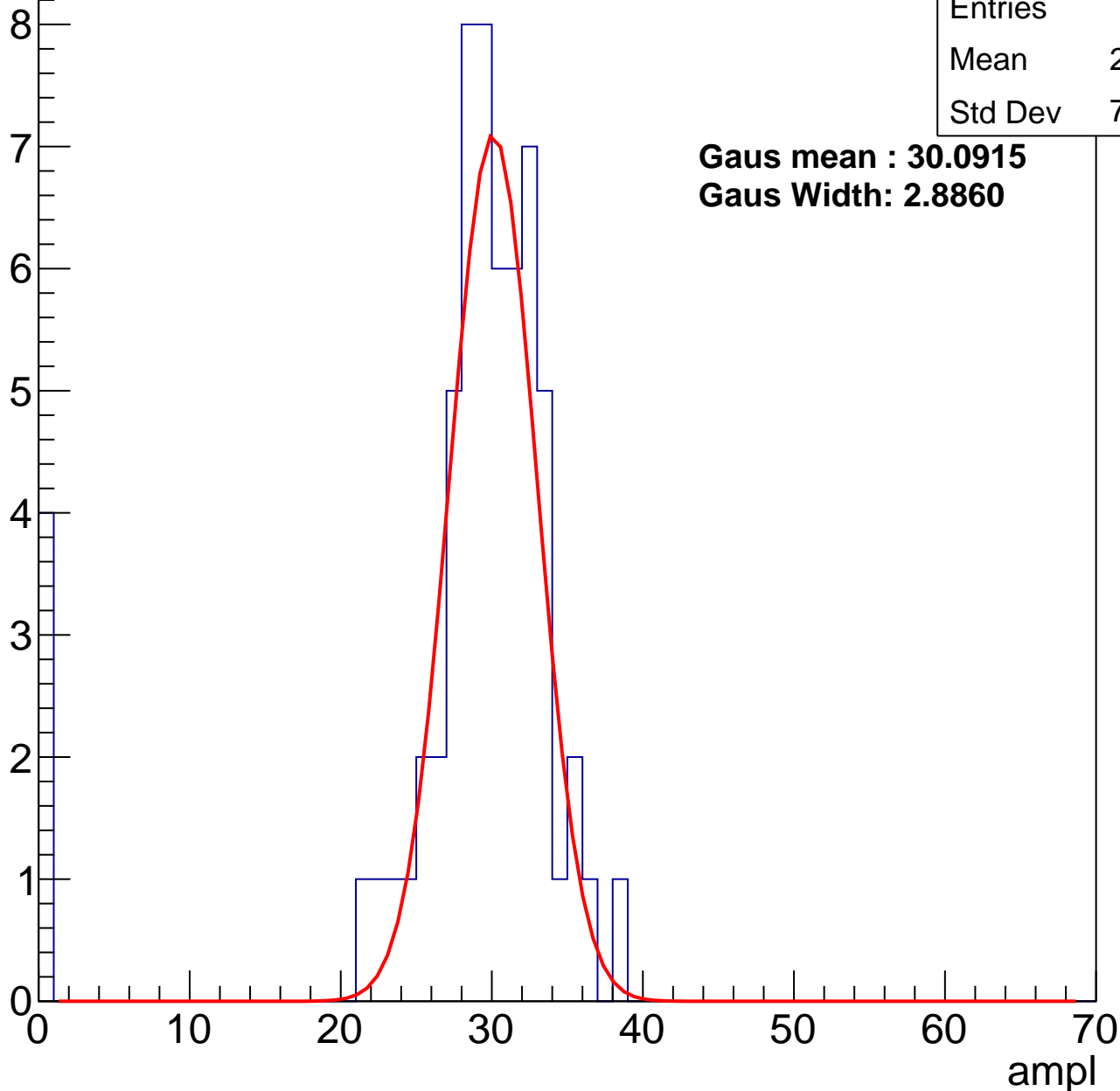
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	27.68
Std Dev	7.939

Gaus mean : 30.0915

Gaus Width: 2.8860



B1L103S, U7-ch95, adc1

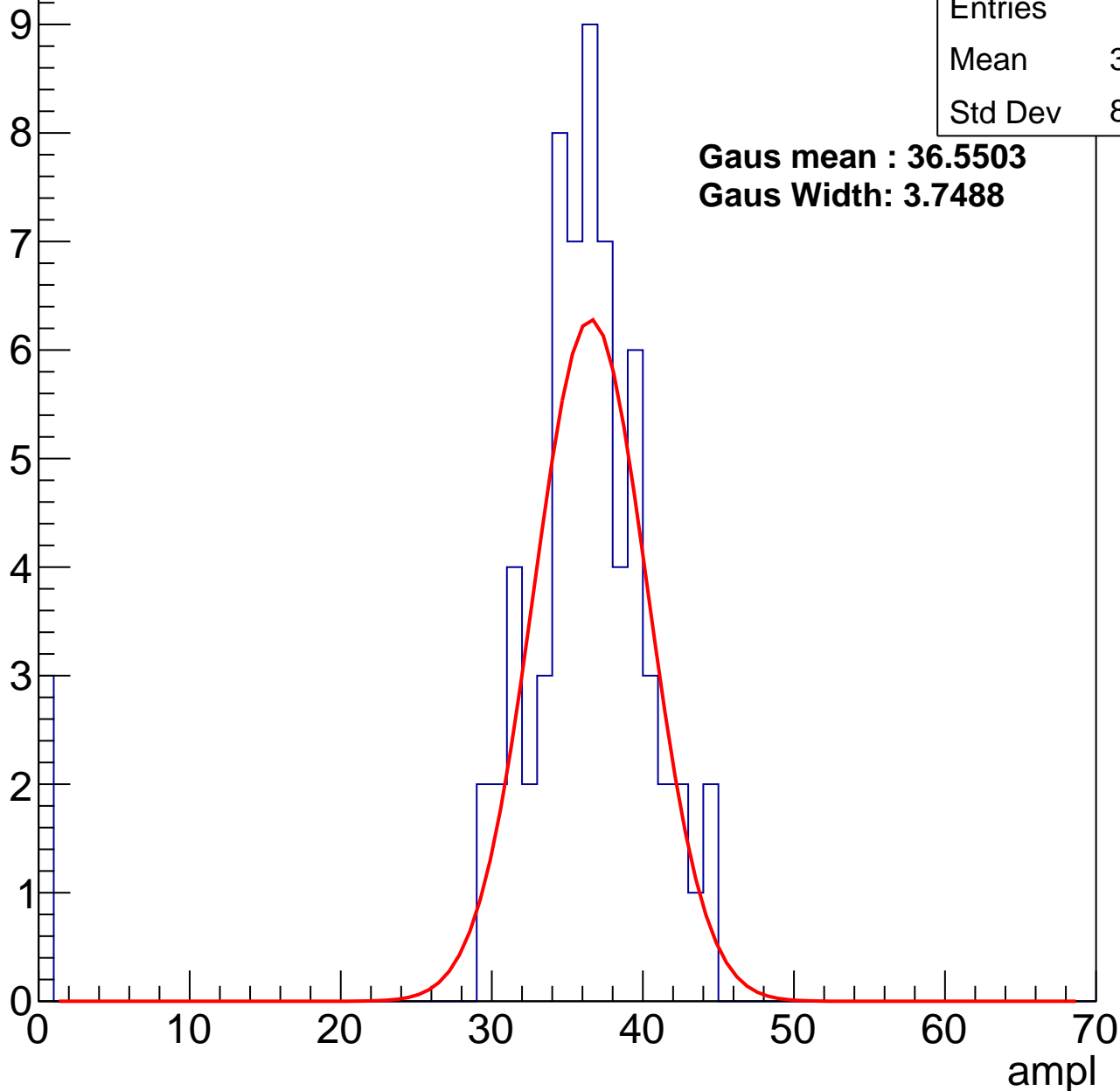
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	34.45
Std Dev	8.212

Gaus mean : 36.5503

Gaus Width: 3.7488



B1L103S, U7-ch95, adc2

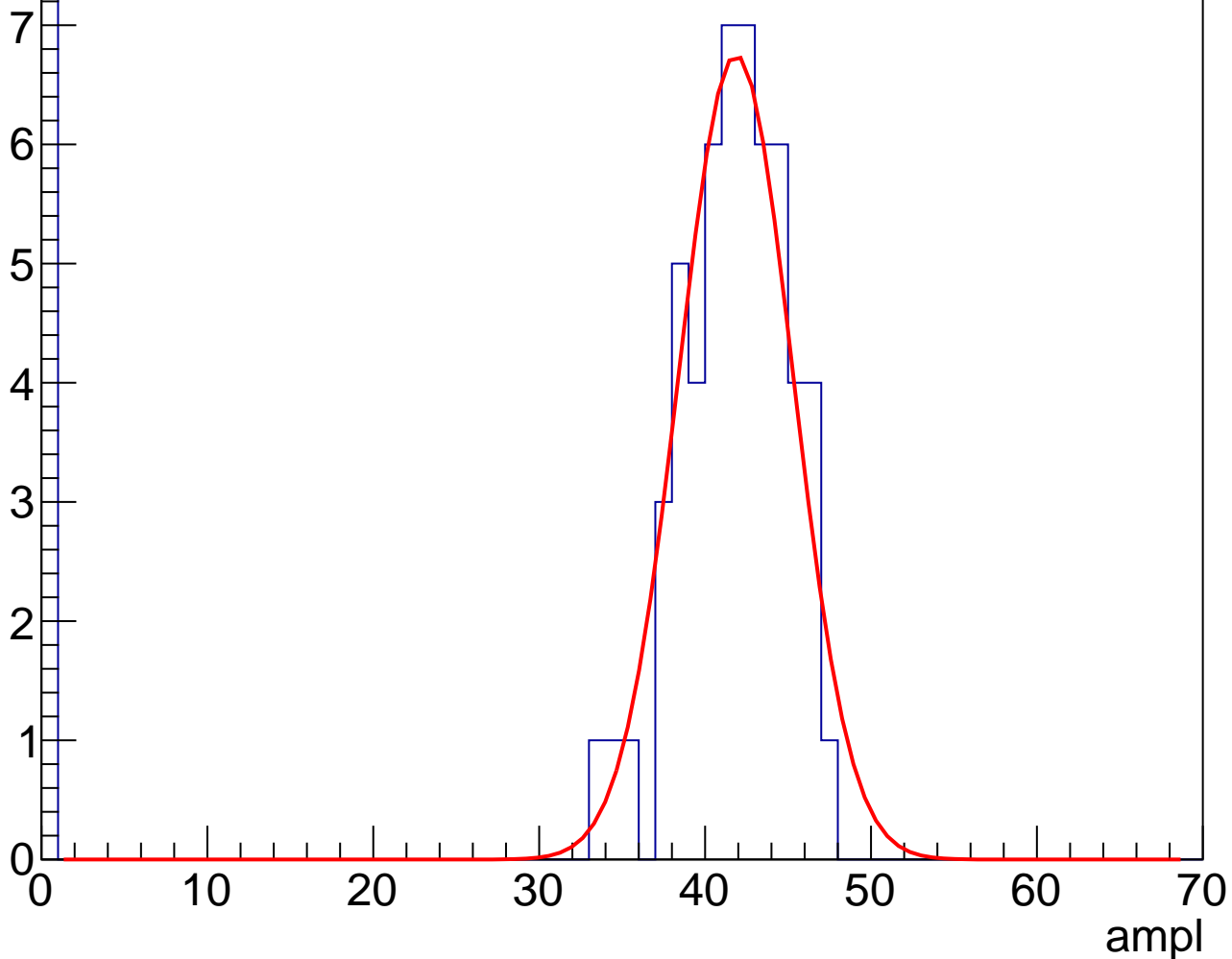
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	35.58
Std Dev	14.56

Gaus mean : 41.8566

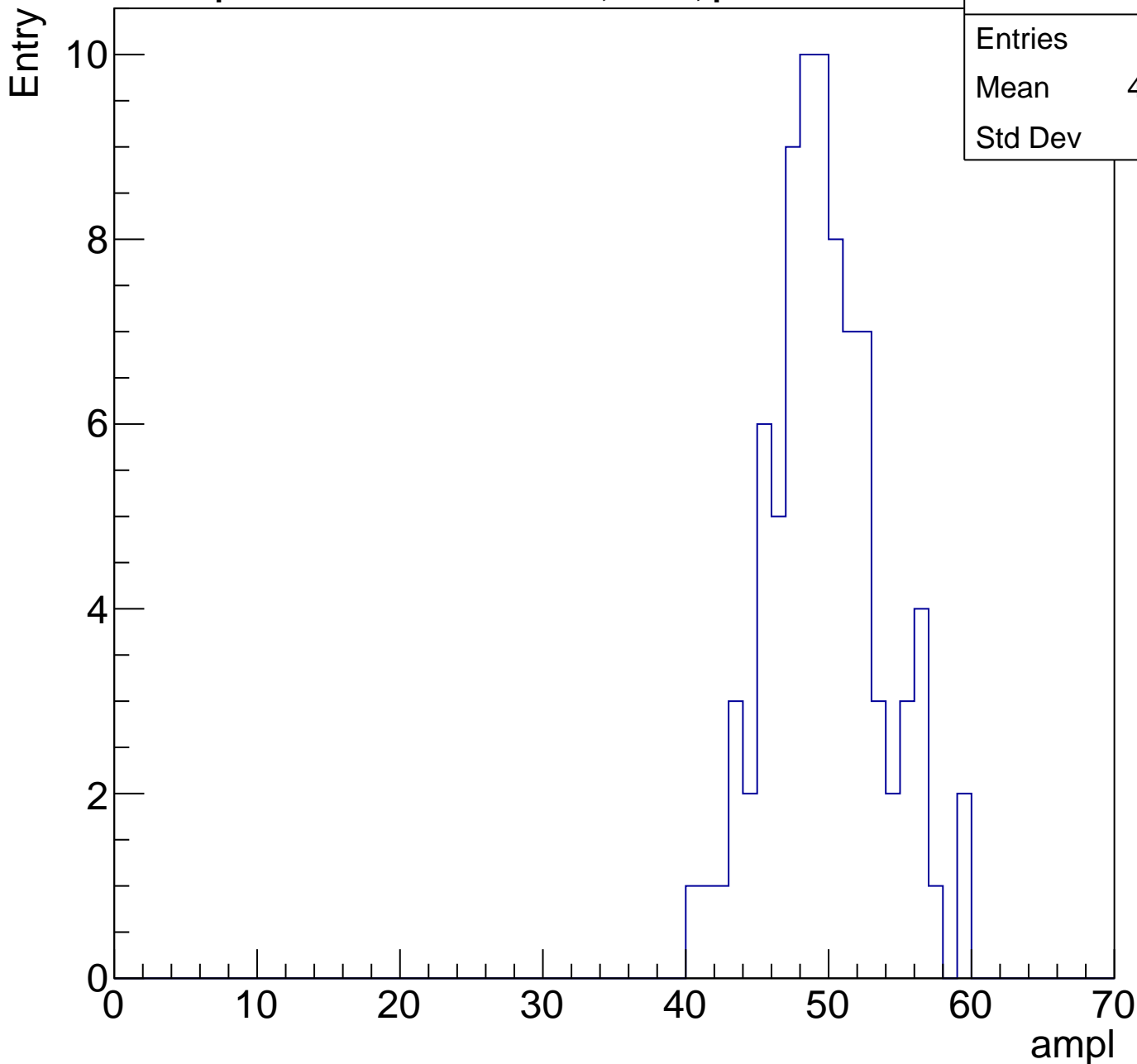
Gaus Width: 3.4301



B1L103S, U7-ch95, adc3

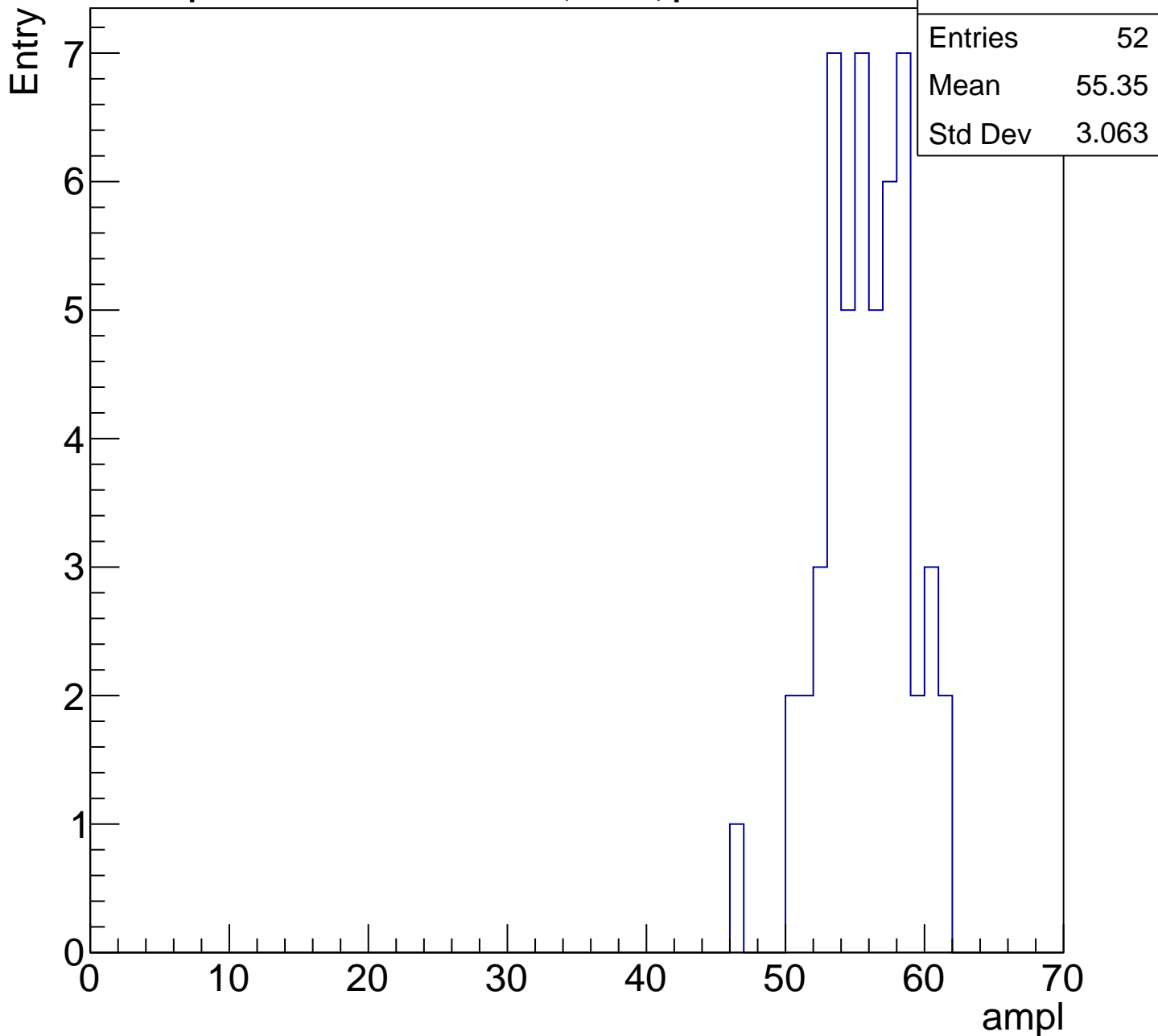
calib_packv5_041523_1651.root, FC#0, port C2

Entries	85
Mean	49.24
Std Dev	3.91



B1L103S, U7-ch95, adc4

calib_packv5_041523_1651.root, FC#0, port C2

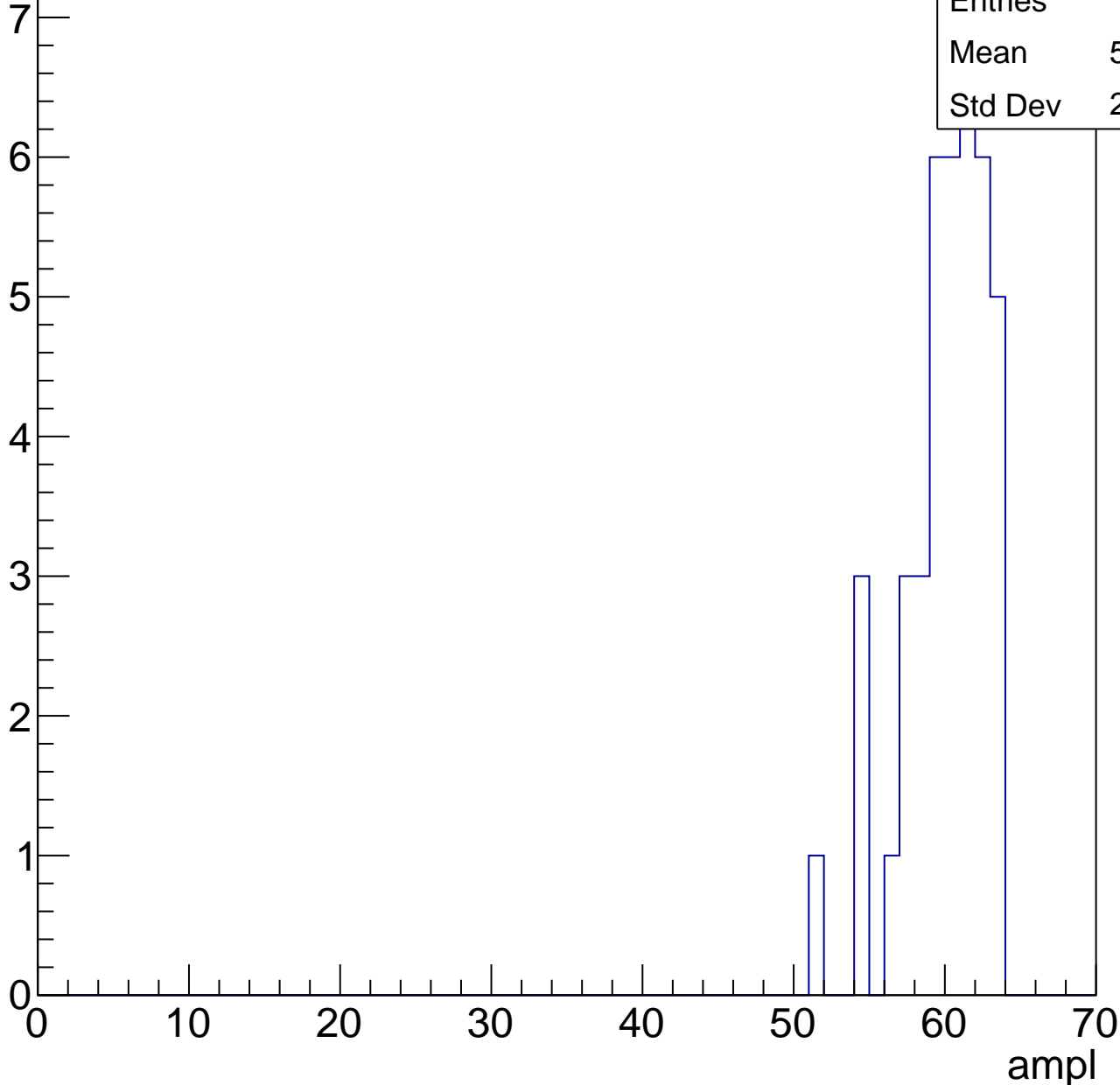


B1L103S, U7-ch95, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	41
Mean	59.56
Std Dev	2.785

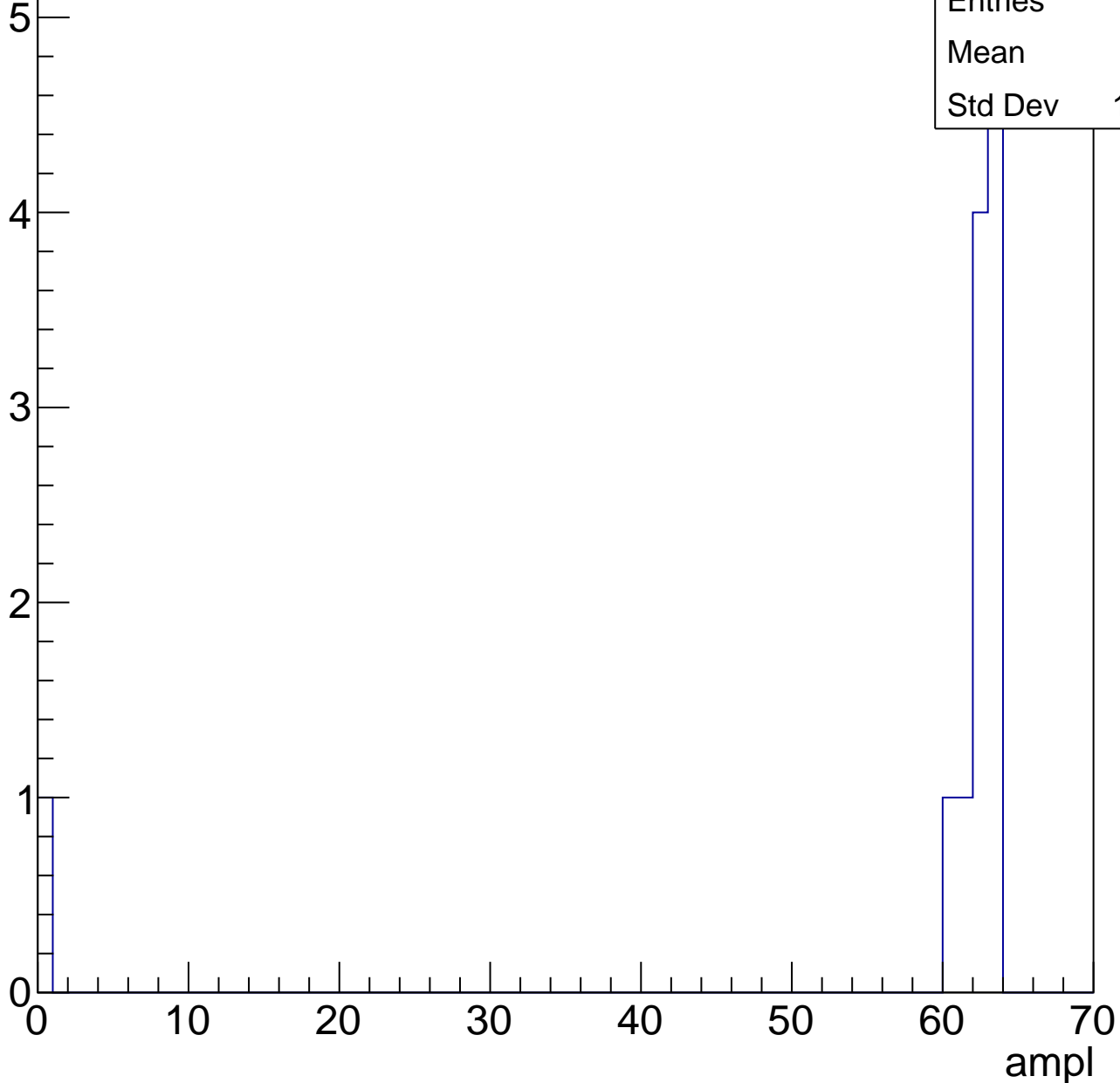


B1L103S, U7-ch95, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	12
Mean	57
Std Dev	17.21



B1L103S, U7-ch95, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U7-ch96, adc0

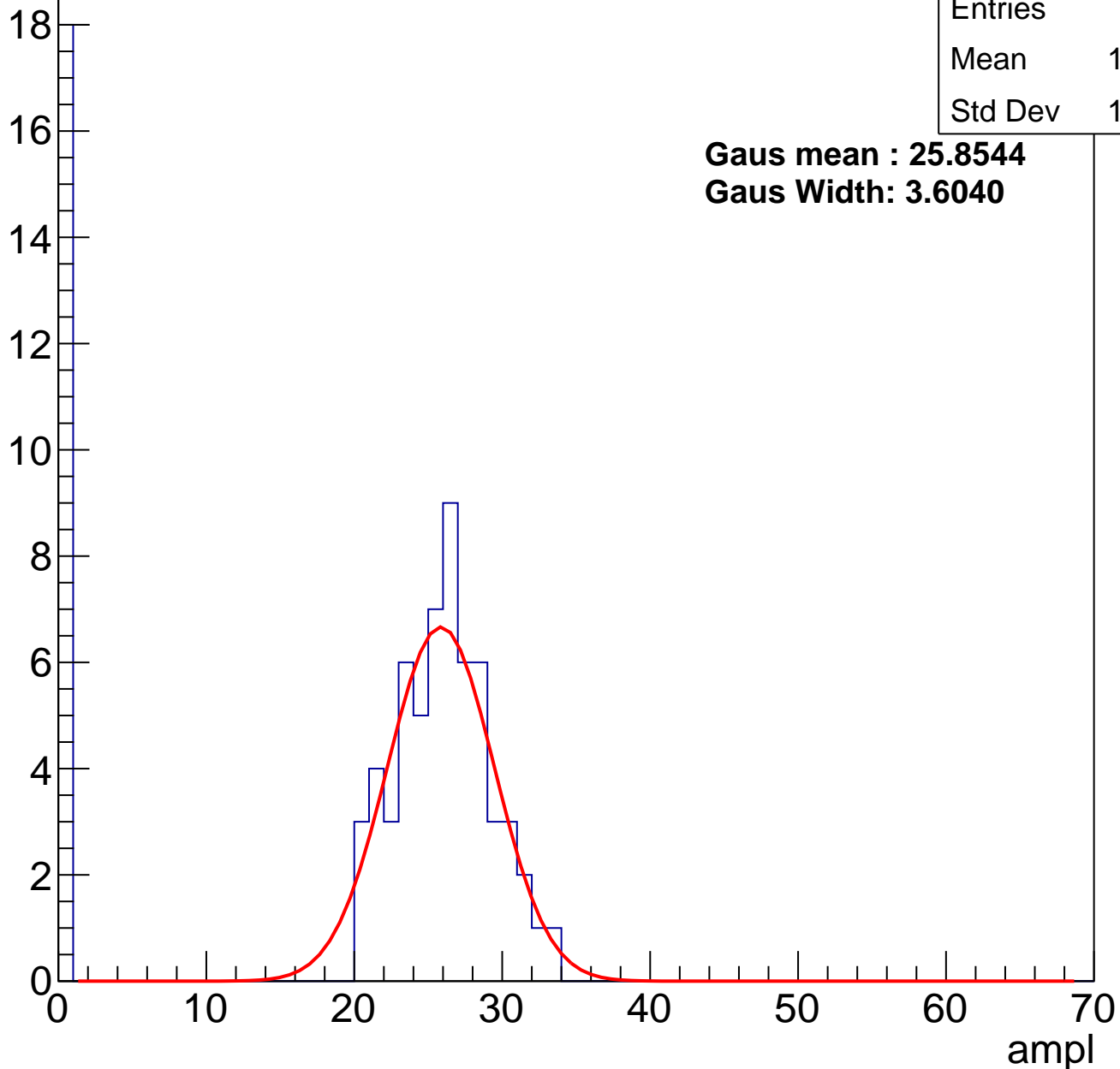
calib_packv5_041523_1651.root, FC#0, port C2

Entries	77
Mean	19.62
Std Dev	11.17

Gaus mean : 25.8544

Gaus Width: 3.6040

Entry



B1L103S, U7-ch96, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	93
Mean	28.06
Std Dev	11.88

Gaus mean : 33.1173

Gaus Width: 4.0495

Entry

12

10

8

6

4

2

0

0

10

20

30

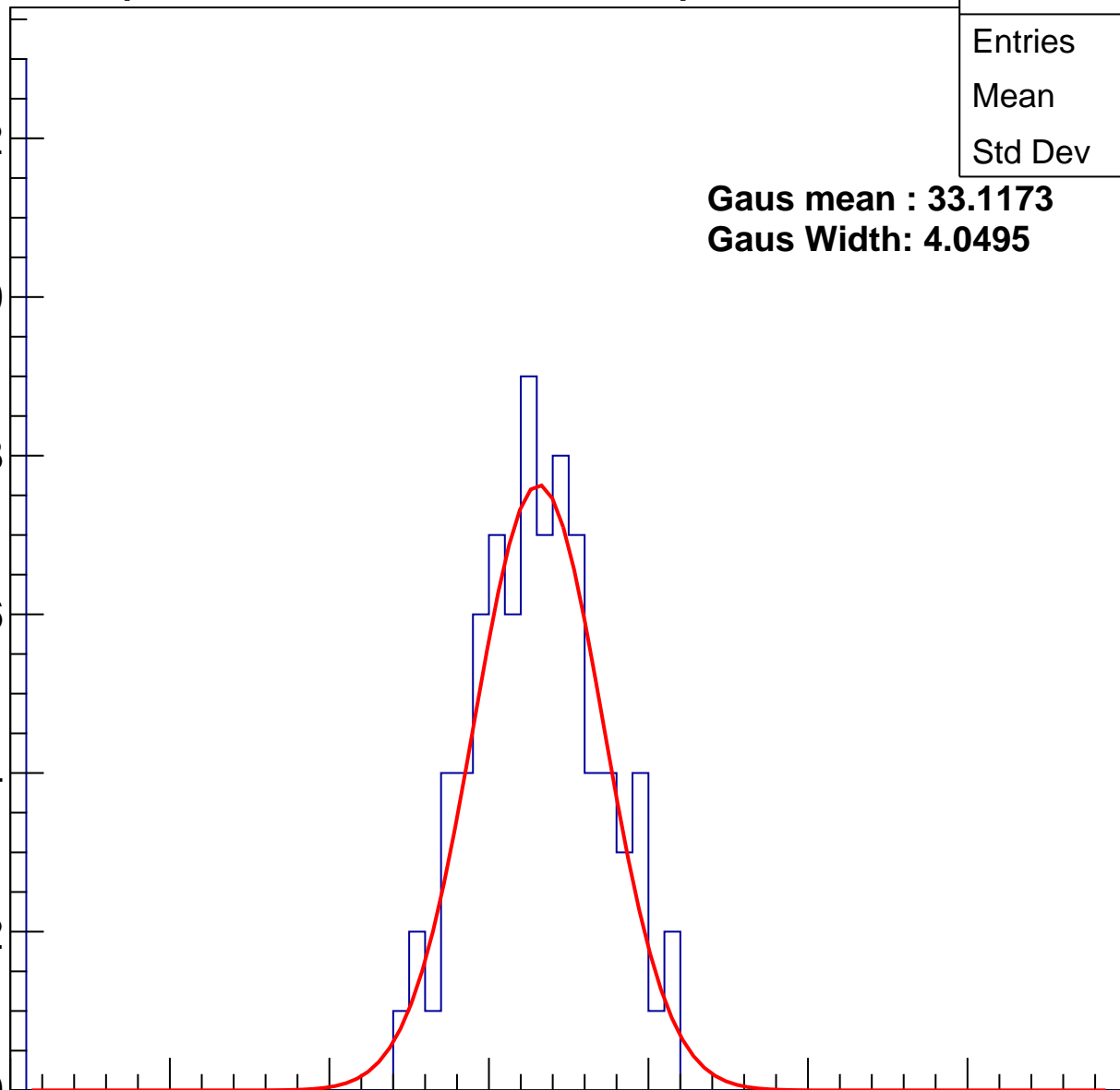
40

50

60

70

ampl



B1L103S, U7-ch96, adc2

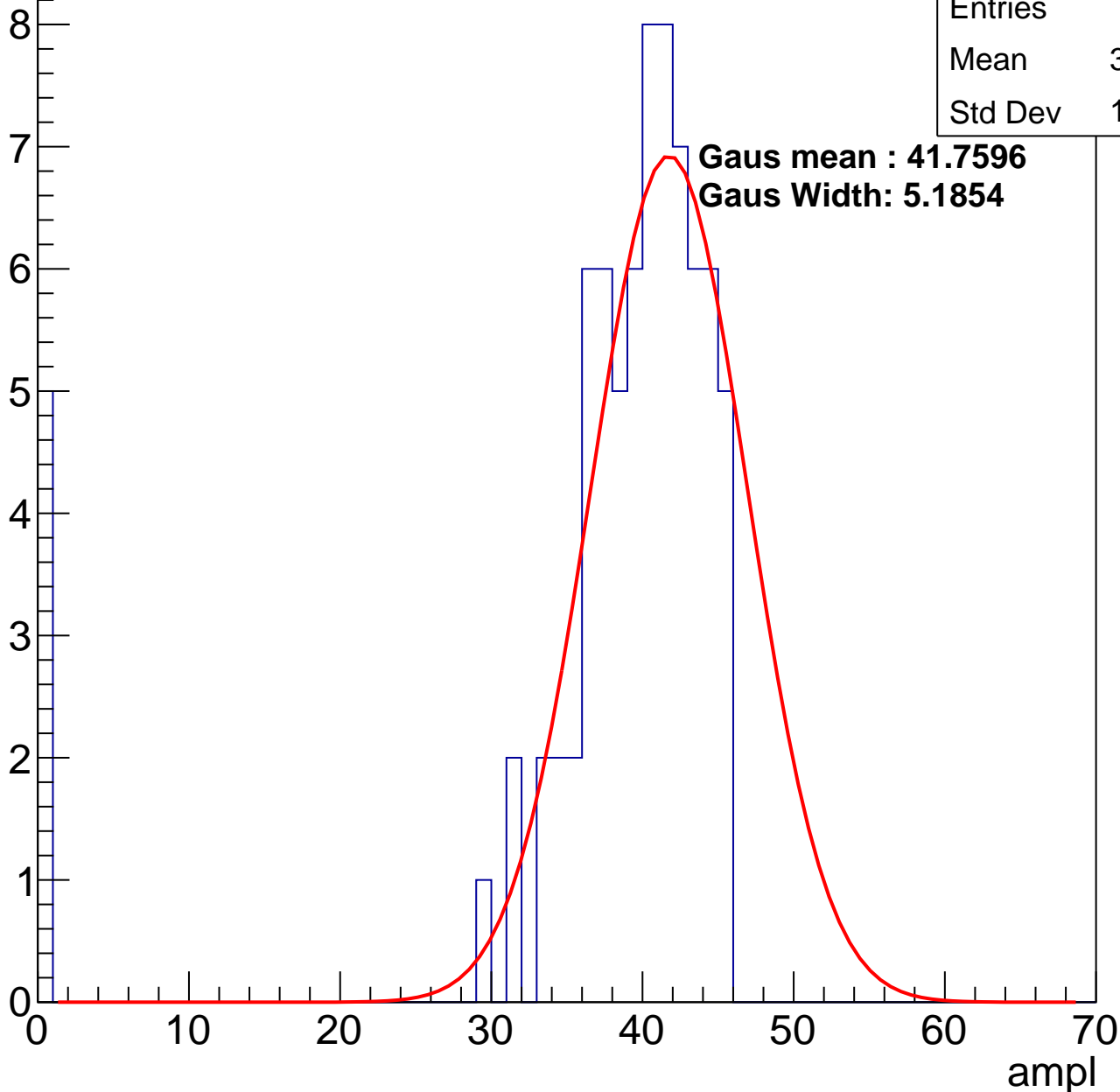
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	36.96
Std Dev	10.37

Gaus mean : 41.7596

Gaus Width: 5.1854

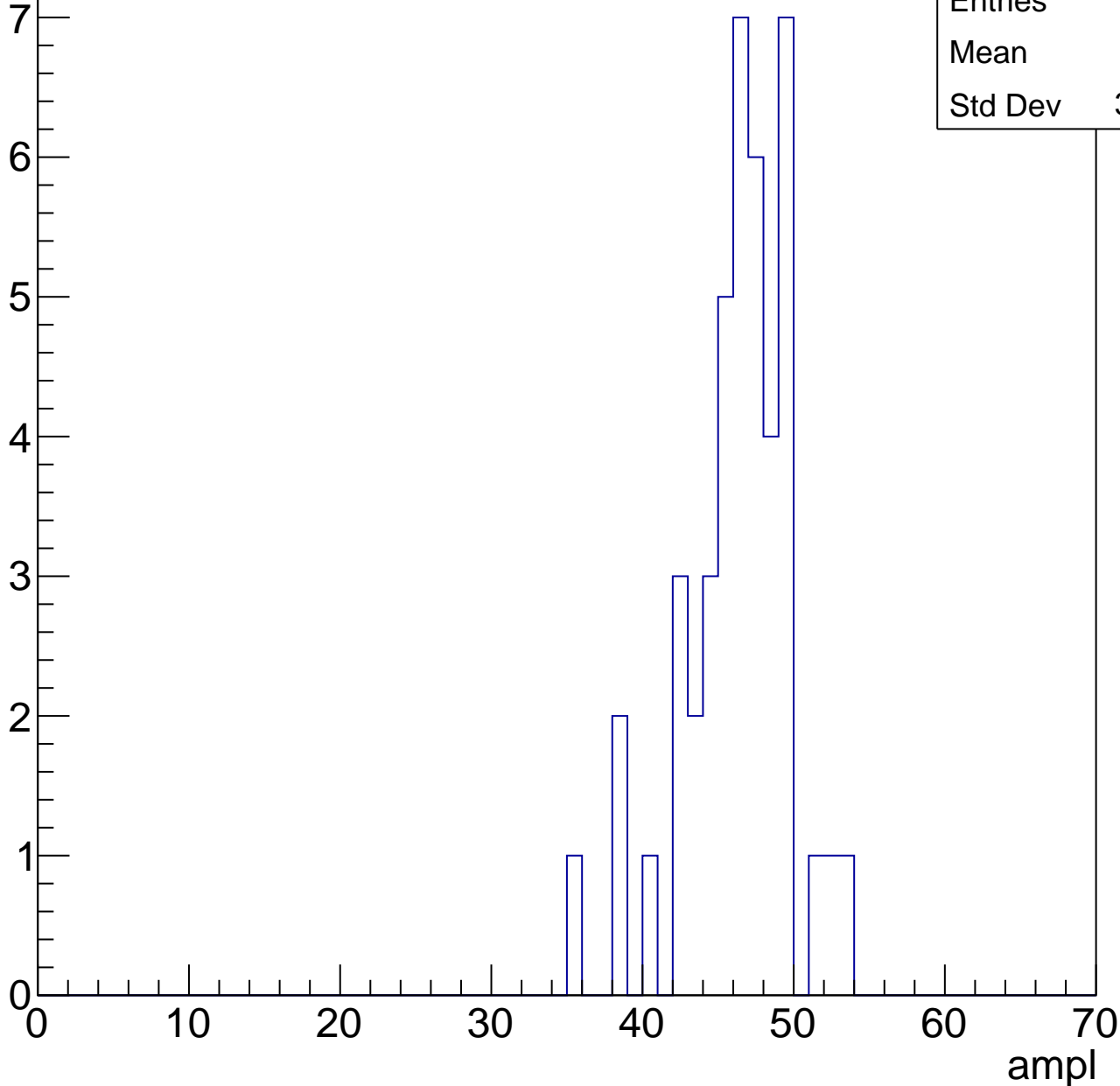


B1L103S, U7-ch96, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	44
Mean	45.8
Std Dev	3.571



B1L103S, U7-ch96, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	77
Mean	51.52
Std Dev	3.436

Entry

10

8

6

4

2

0

0

10

20

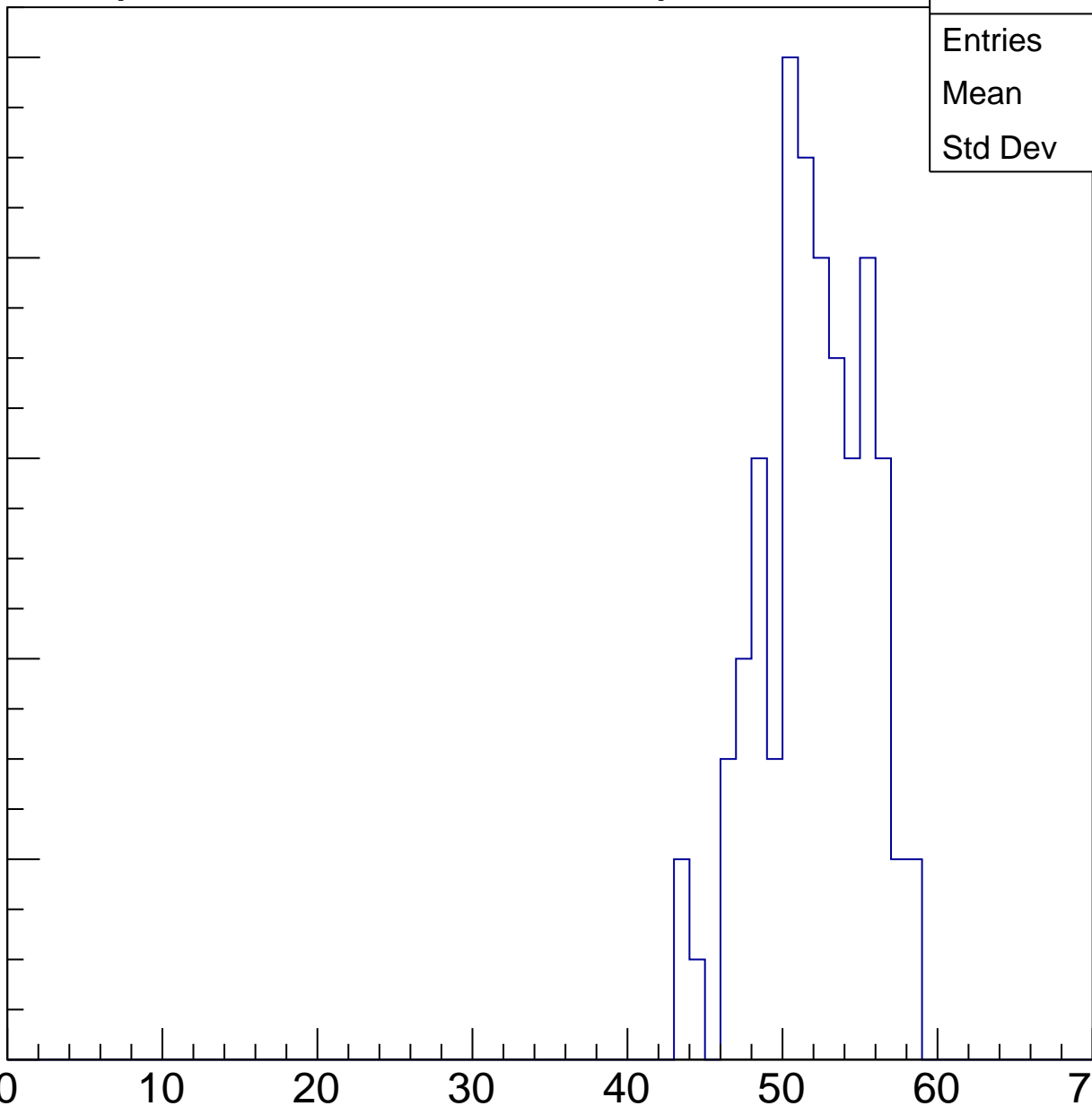
30

40

50

60

ampl

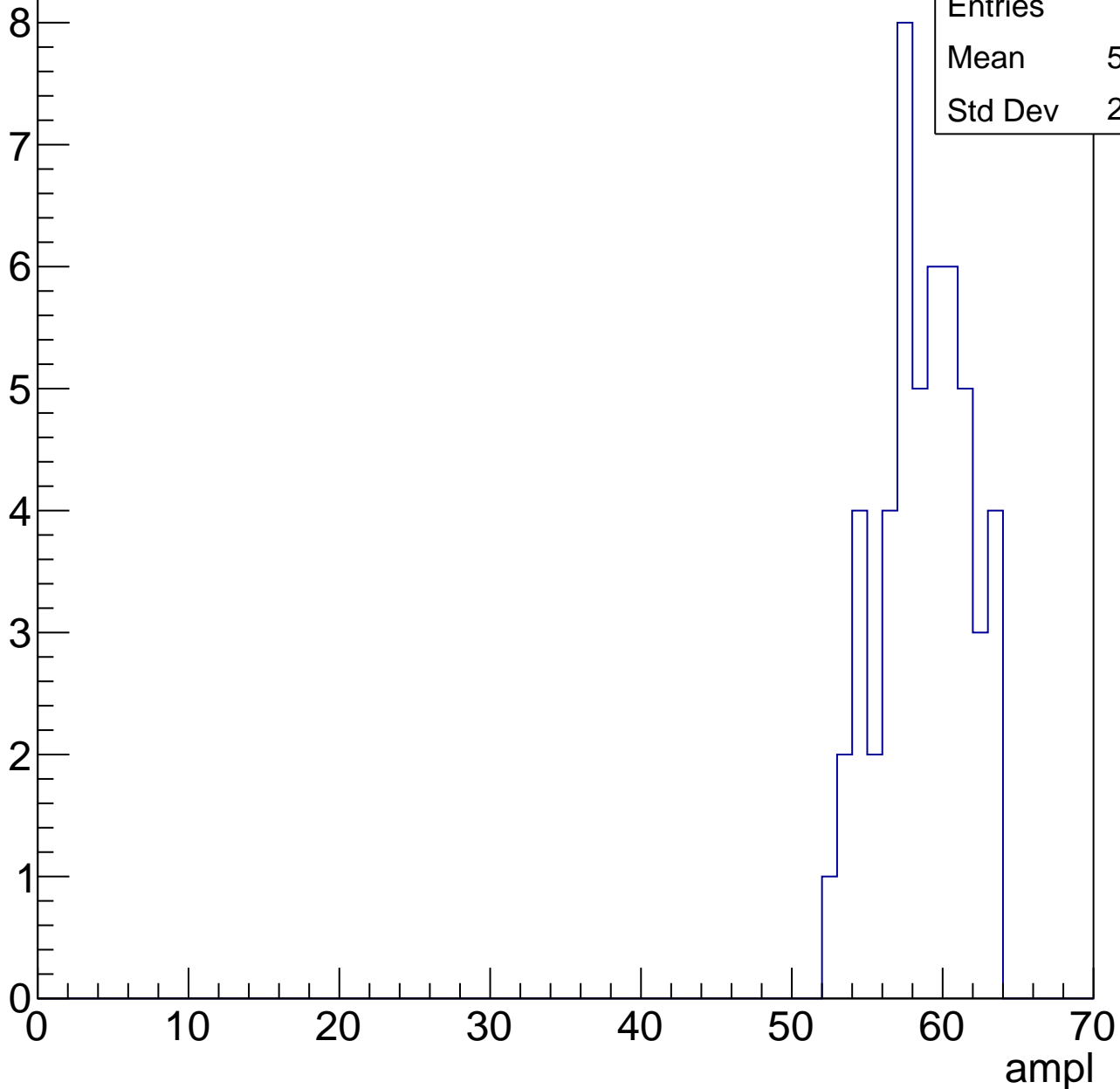


B1L103S, U7-ch96, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	58.22
Std Dev	2.873

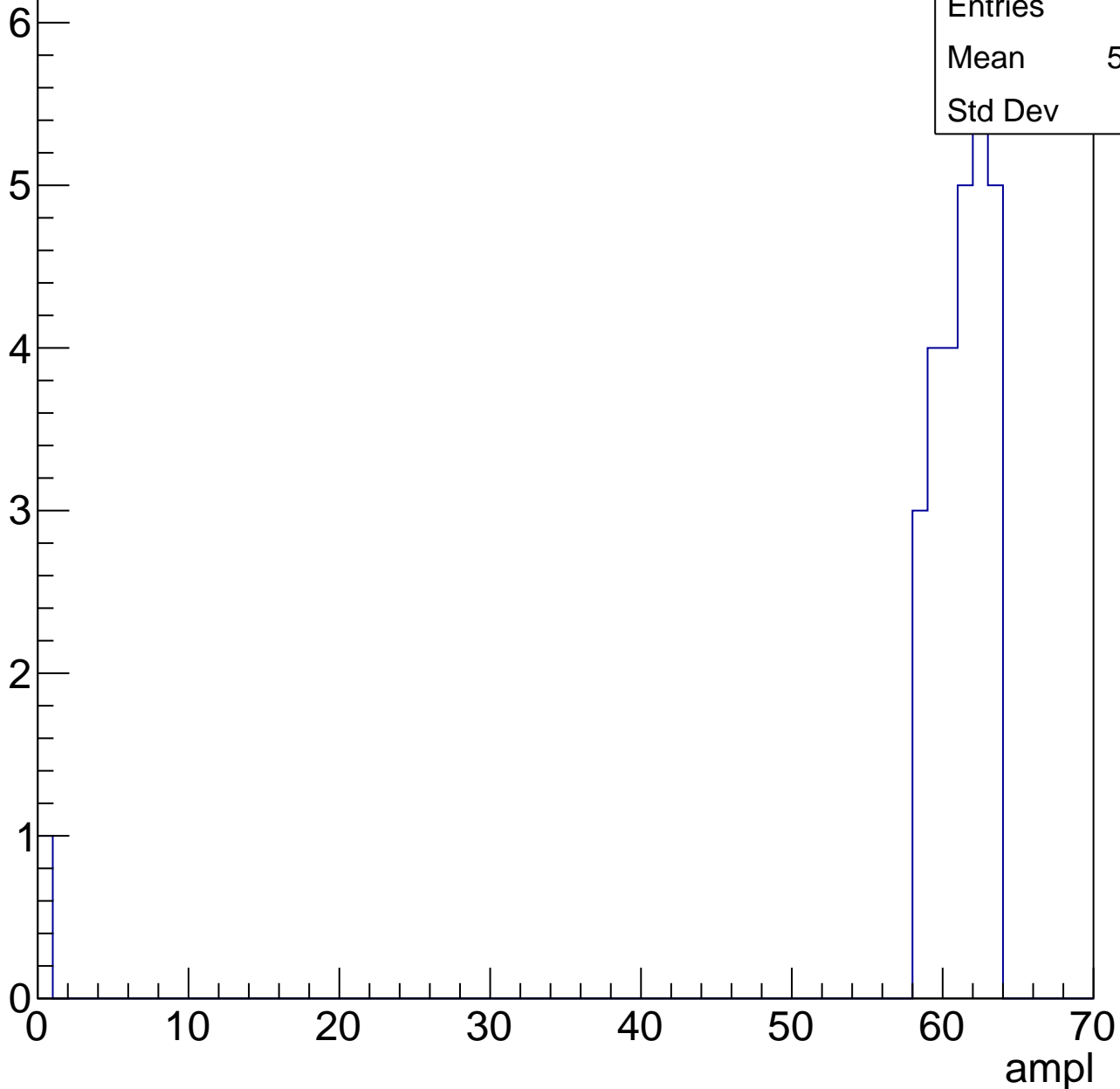


B1L103S, U7-ch96, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	28
Mean	58.64
Std Dev	11.4



B1L103S, U7-ch96, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	5.952
Std Dev	18.35

Entry



B1L103S, U7-ch97, adc0

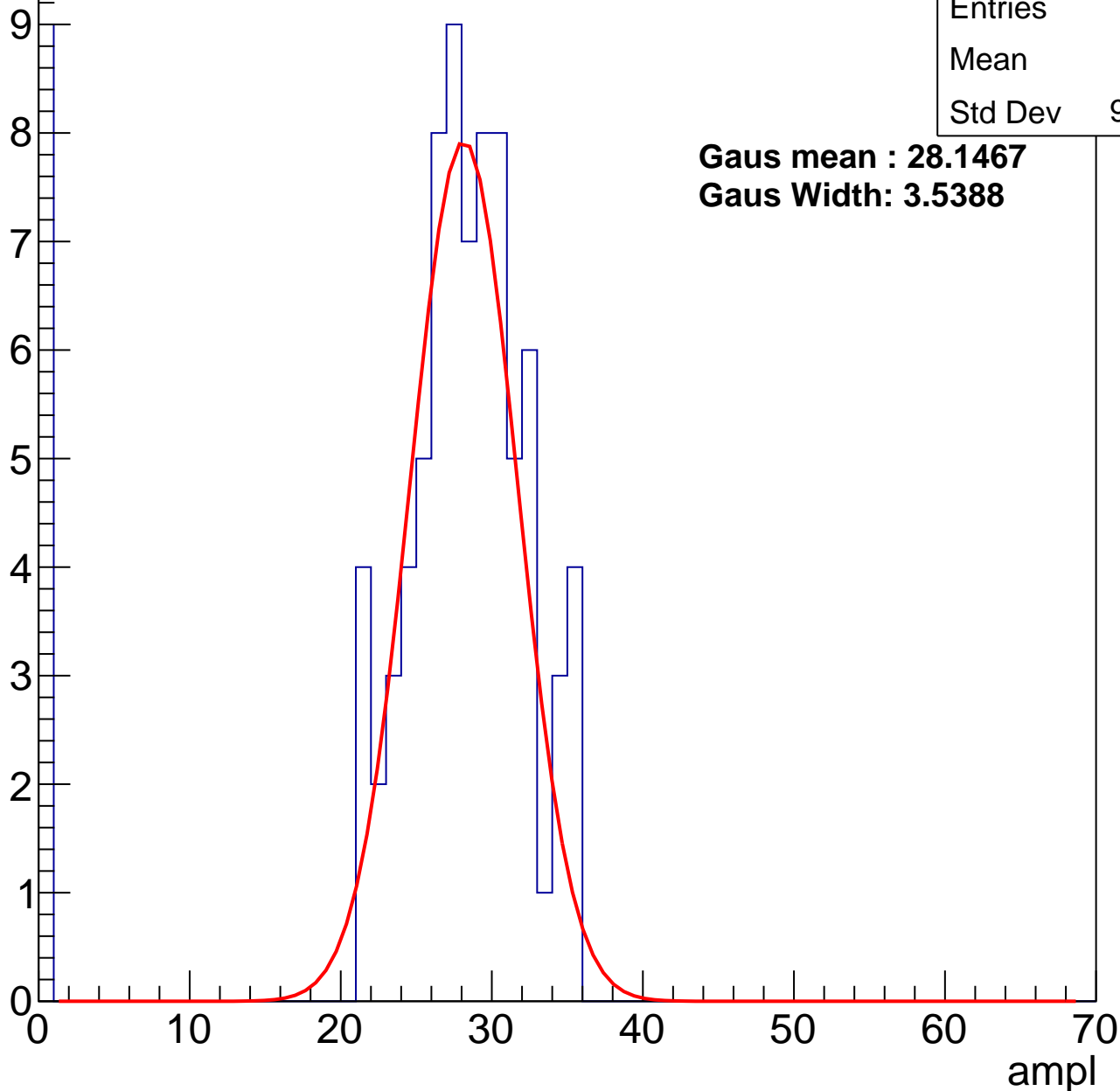
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	86
Mean	25.1
Std Dev	9.237

Gaus mean : 28.1467

Gaus Width: 3.5388



B1L103S, U7-ch97, adc1

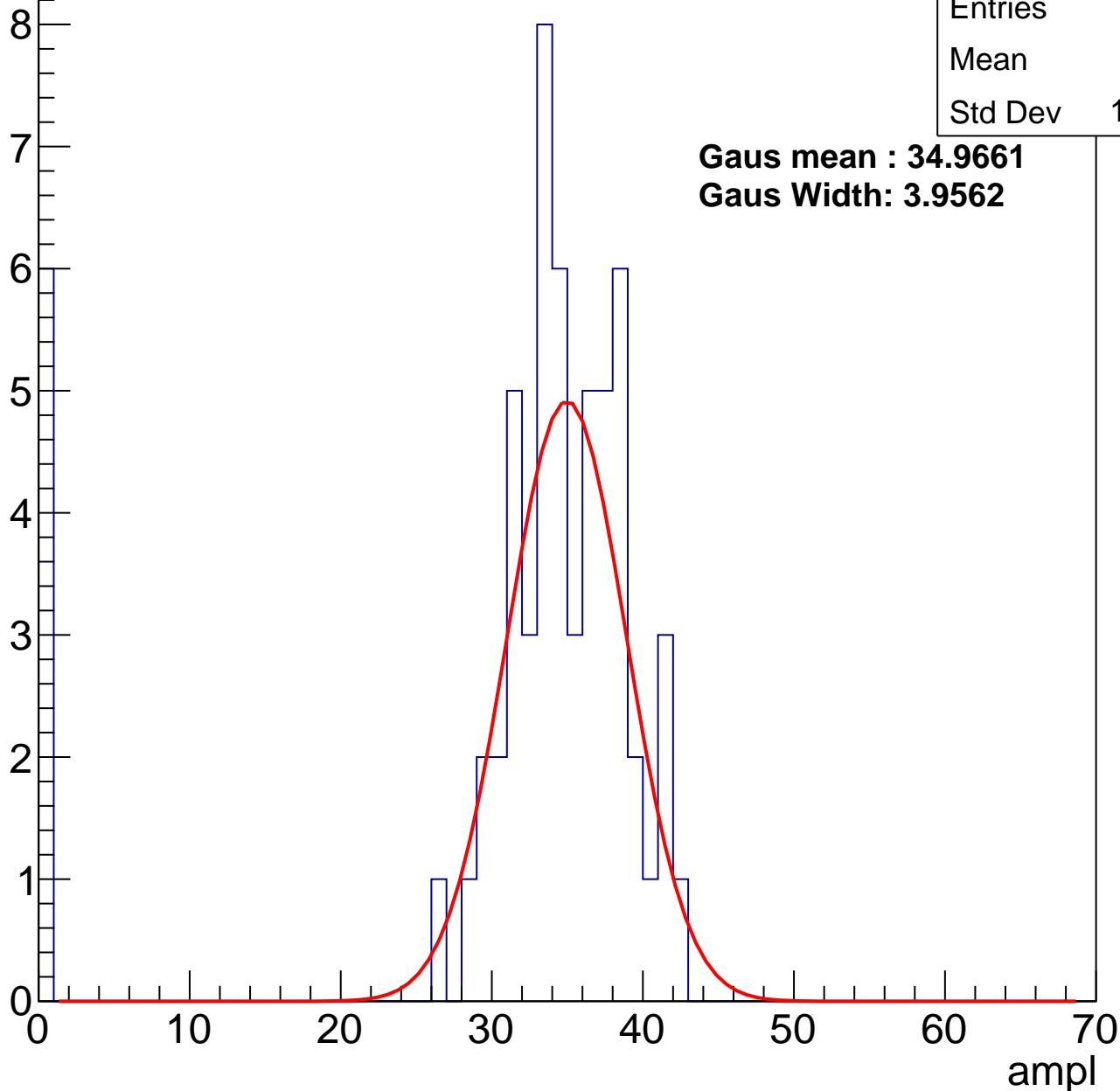
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	31.2
Std Dev	10.93

Gaus mean : 34.9661

Gaus Width: 3.9562



B1L103S, U7-ch97, adc2

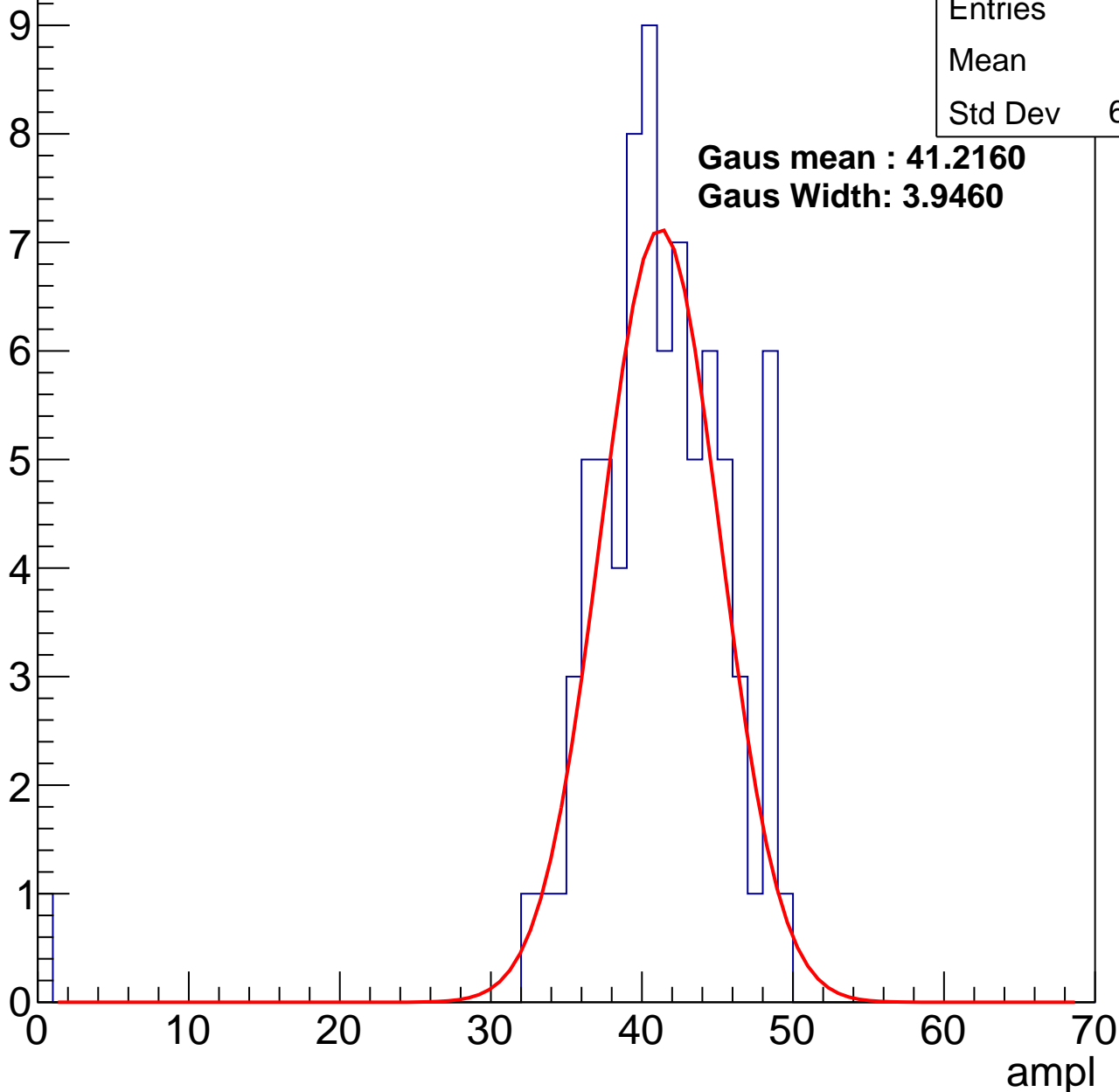
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	40.5
Std Dev	6.072

Gaus mean : 41.2160

Gaus Width: 3.9460

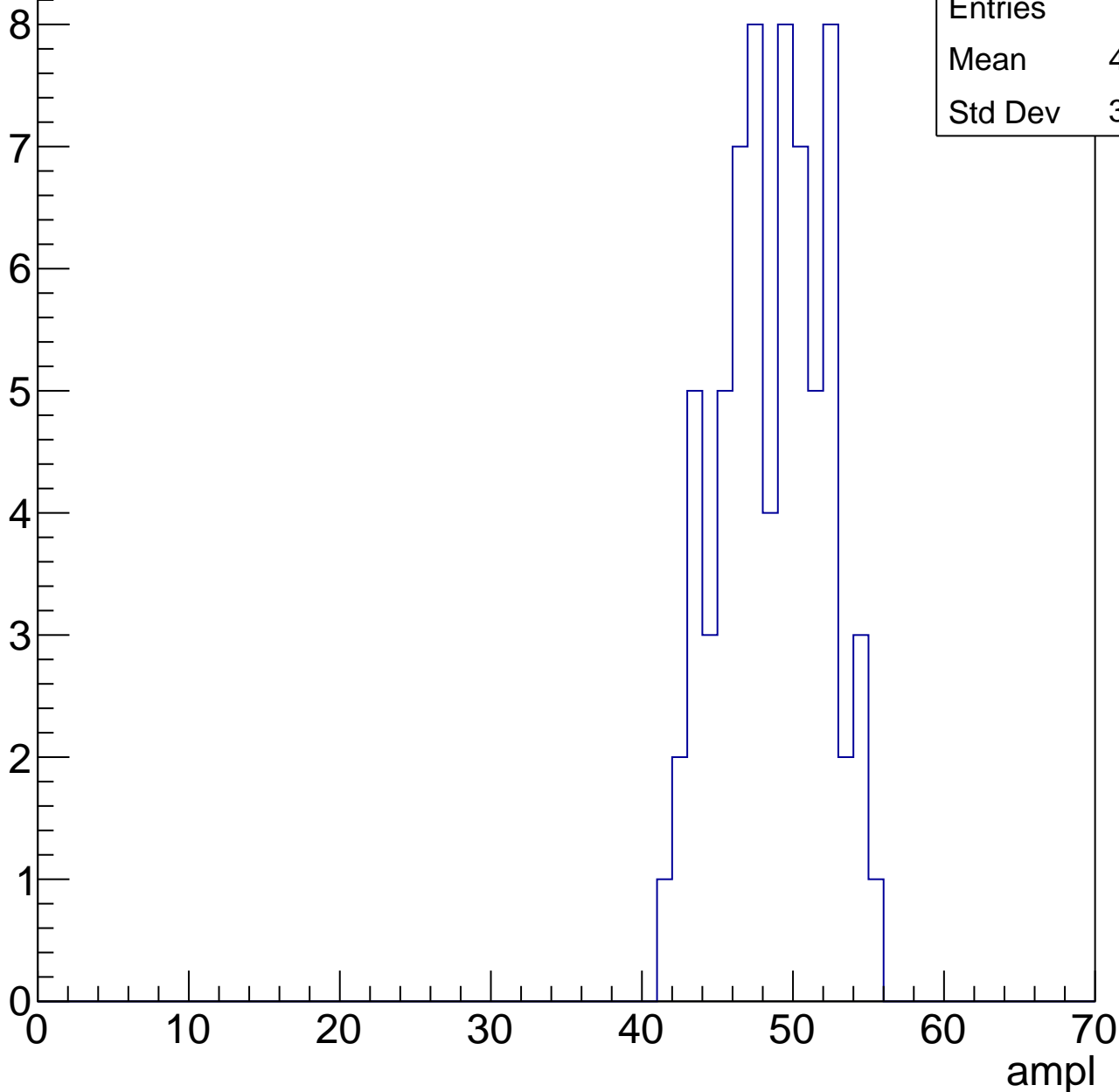


B1L103S, U7-ch97, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	48.16
Std Dev	3.382

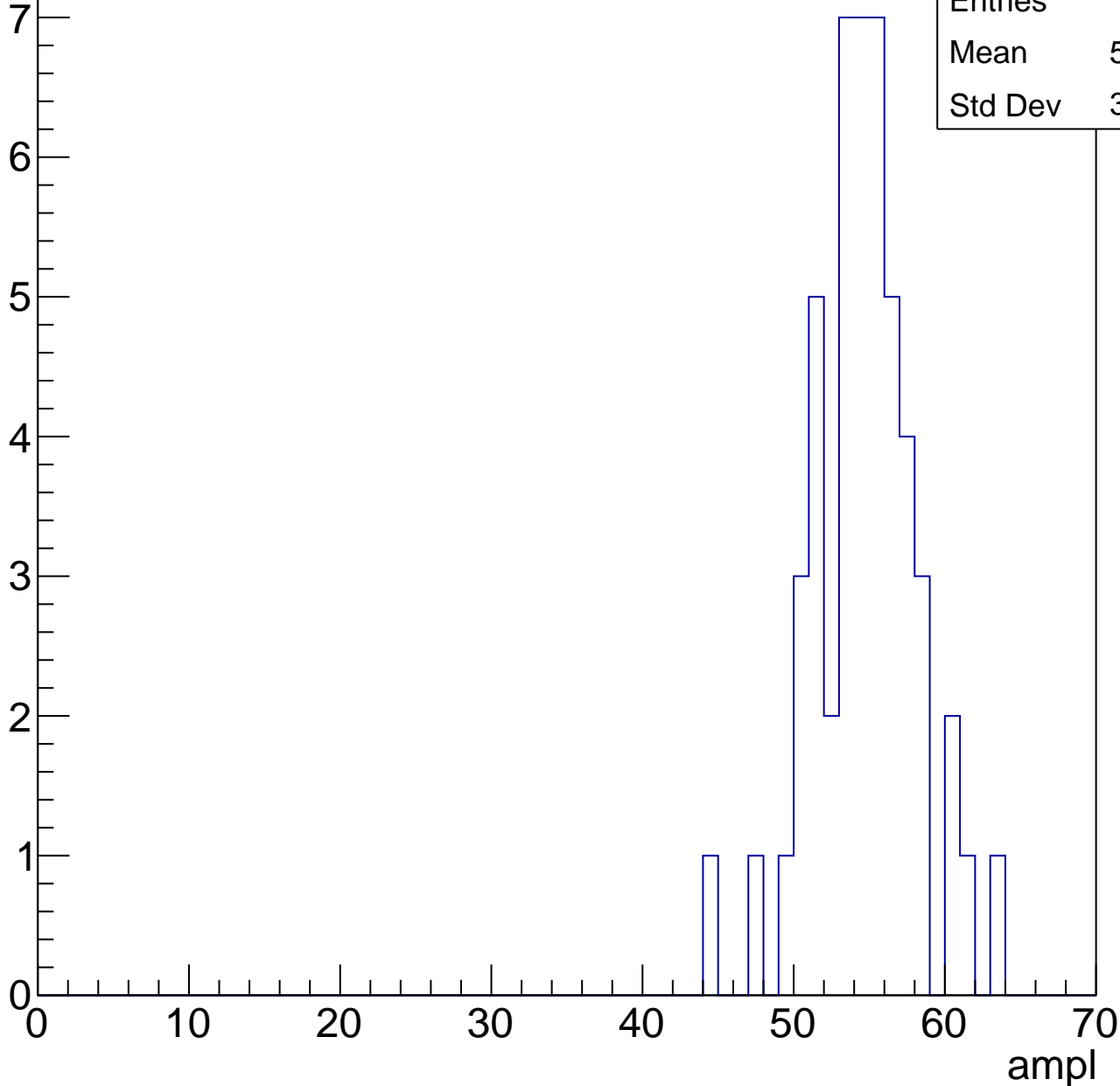


B1L103S, U7-ch97, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	54.18
Std Dev	3.445

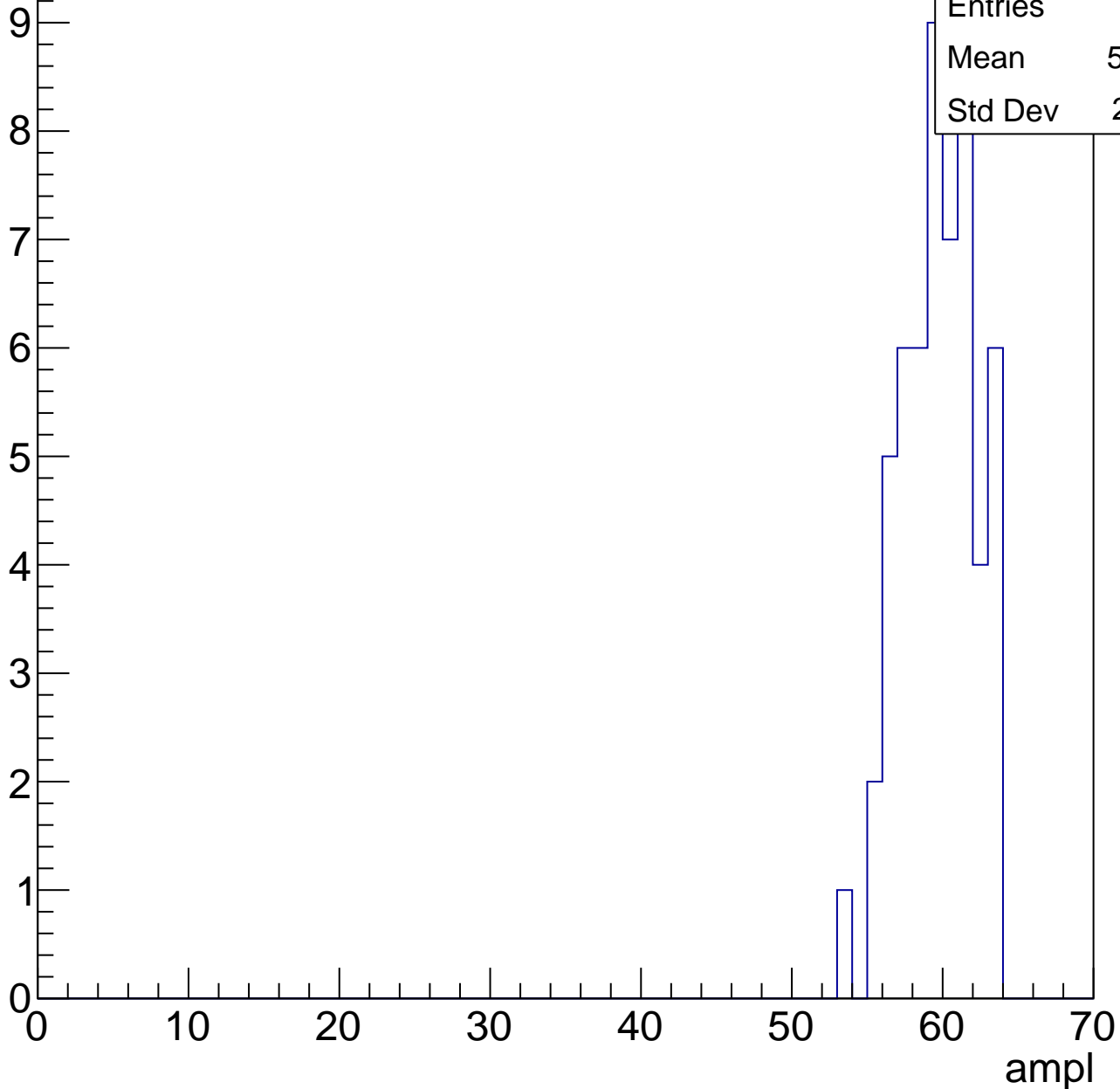


B1L103S, U7-ch97, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

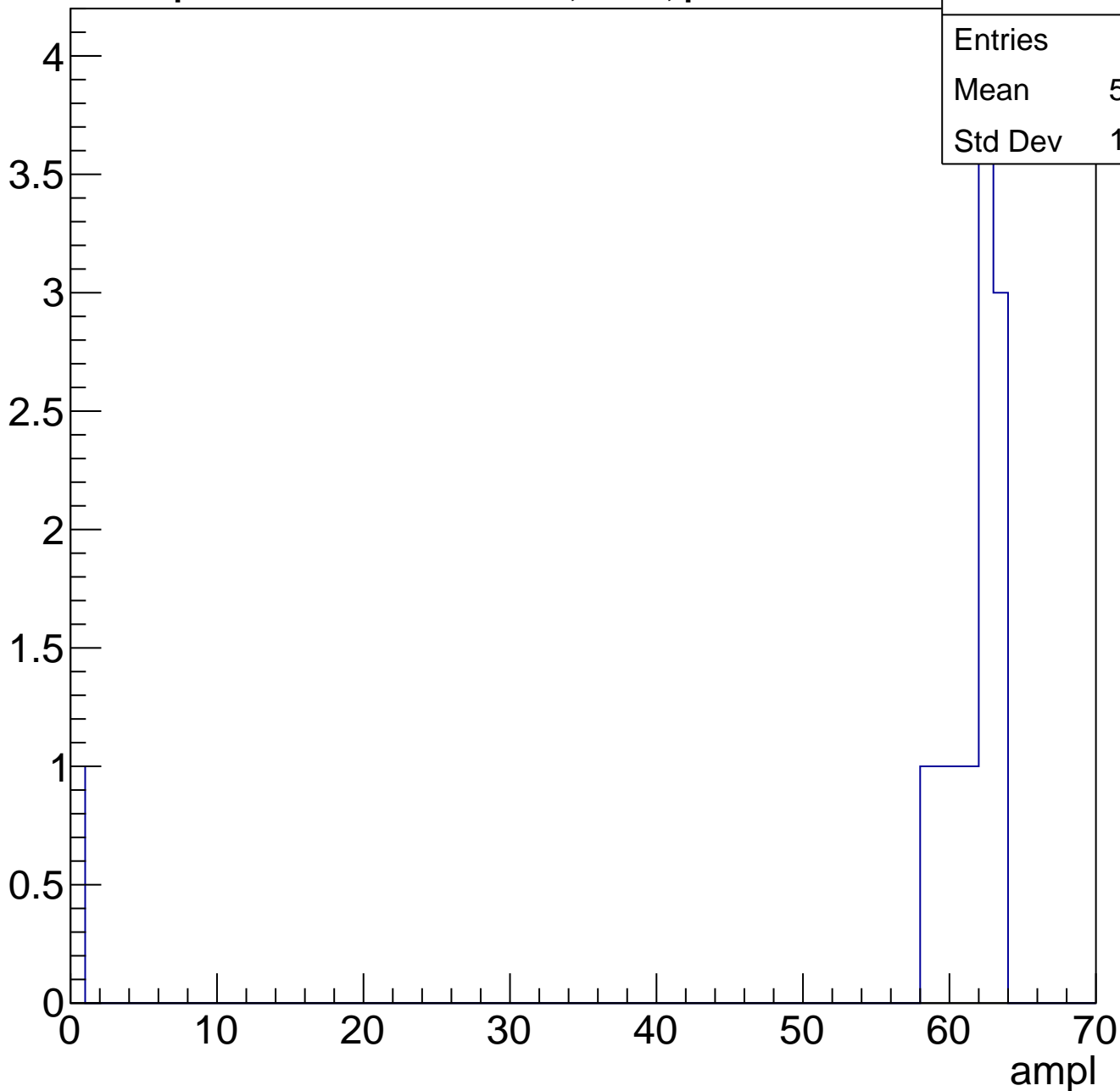
Entries	54
Mean	59.22
Std Dev	2.401



B1L103S, U7-ch97, adc6

calib_packv5_041523_1651.root, FC#0, port C2

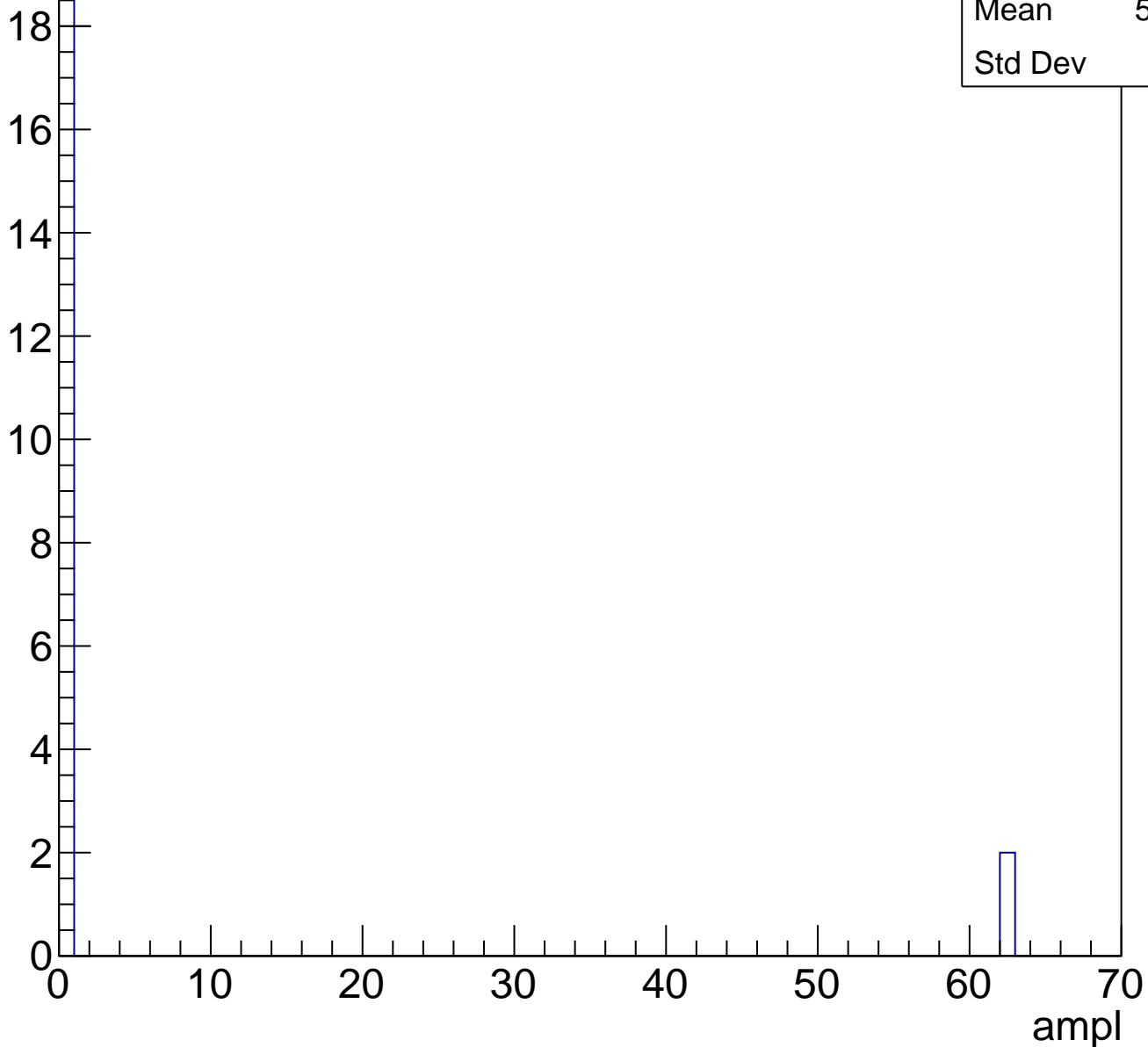
Entry



B1L103S, U7-ch97, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch98, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	86
Mean	22.31
Std Dev	11.13

Gaus mean : 28.3016

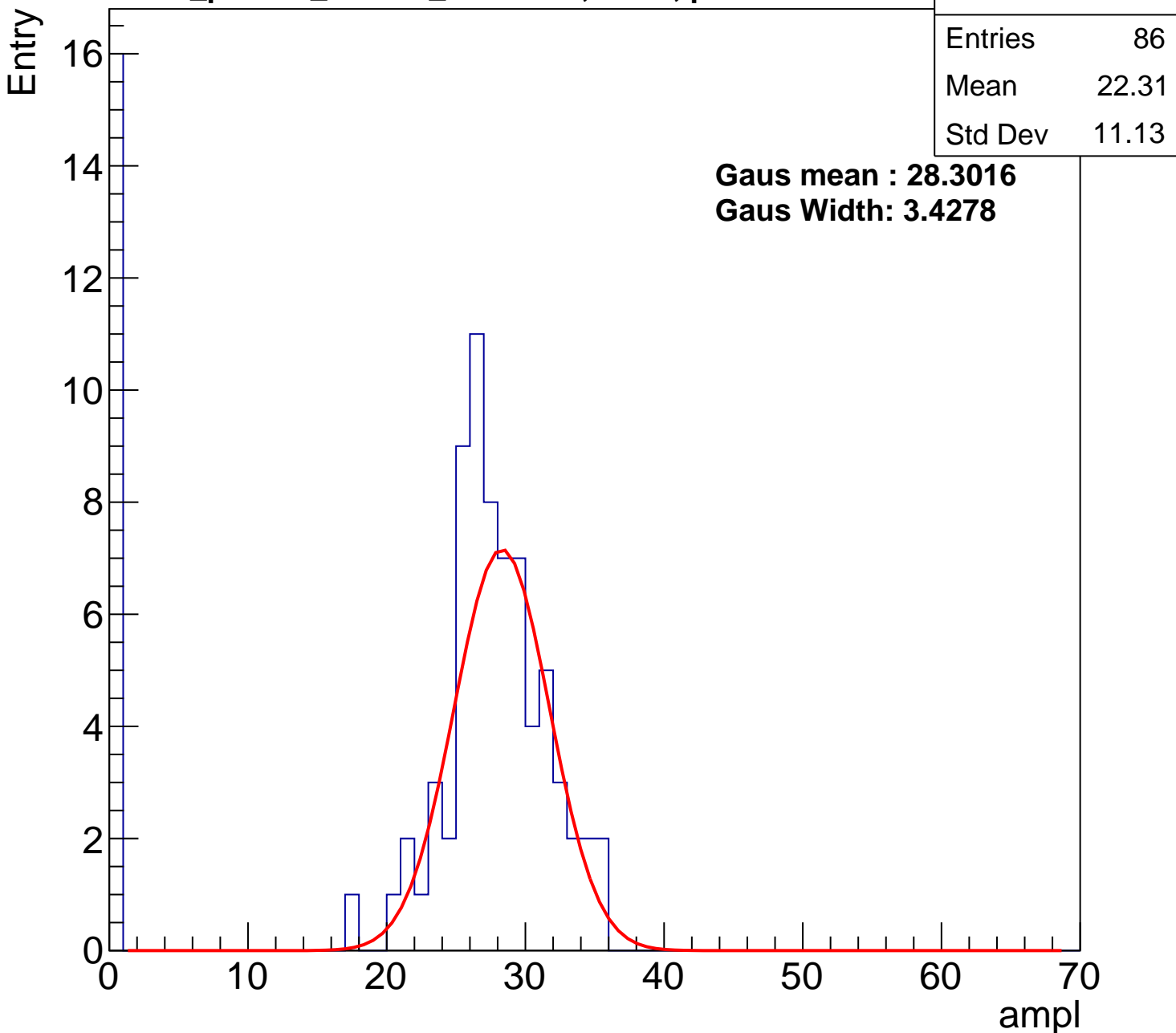
Gaus Width: 3.4278

Entry

16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl



B1L103S, U7-ch98, adc1

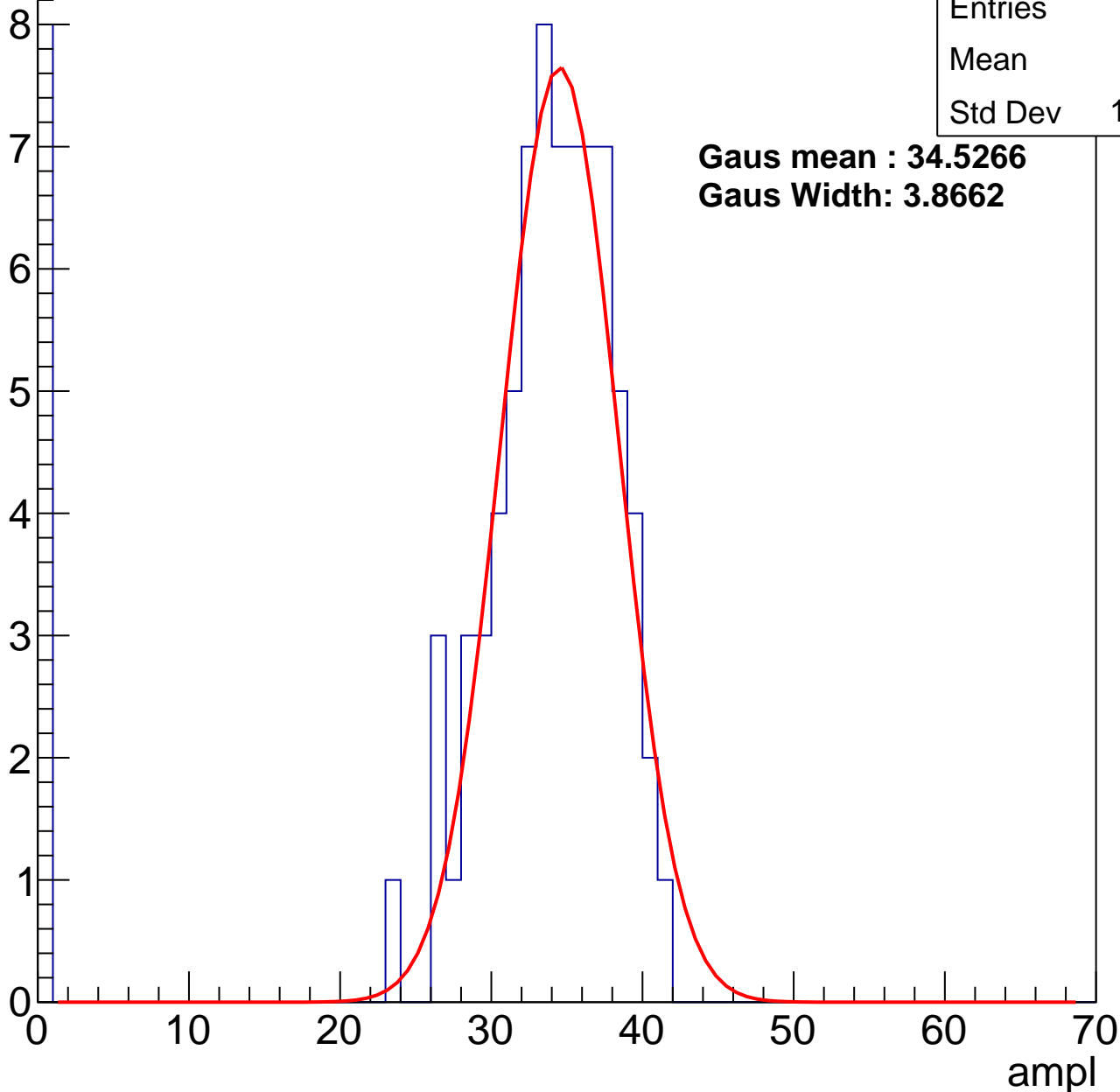
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	83
Mean	30.4
Std Dev	10.56

Gaus mean : 34.5266

Gaus Width: 3.8662



B1L103S, U7-ch98, adc2

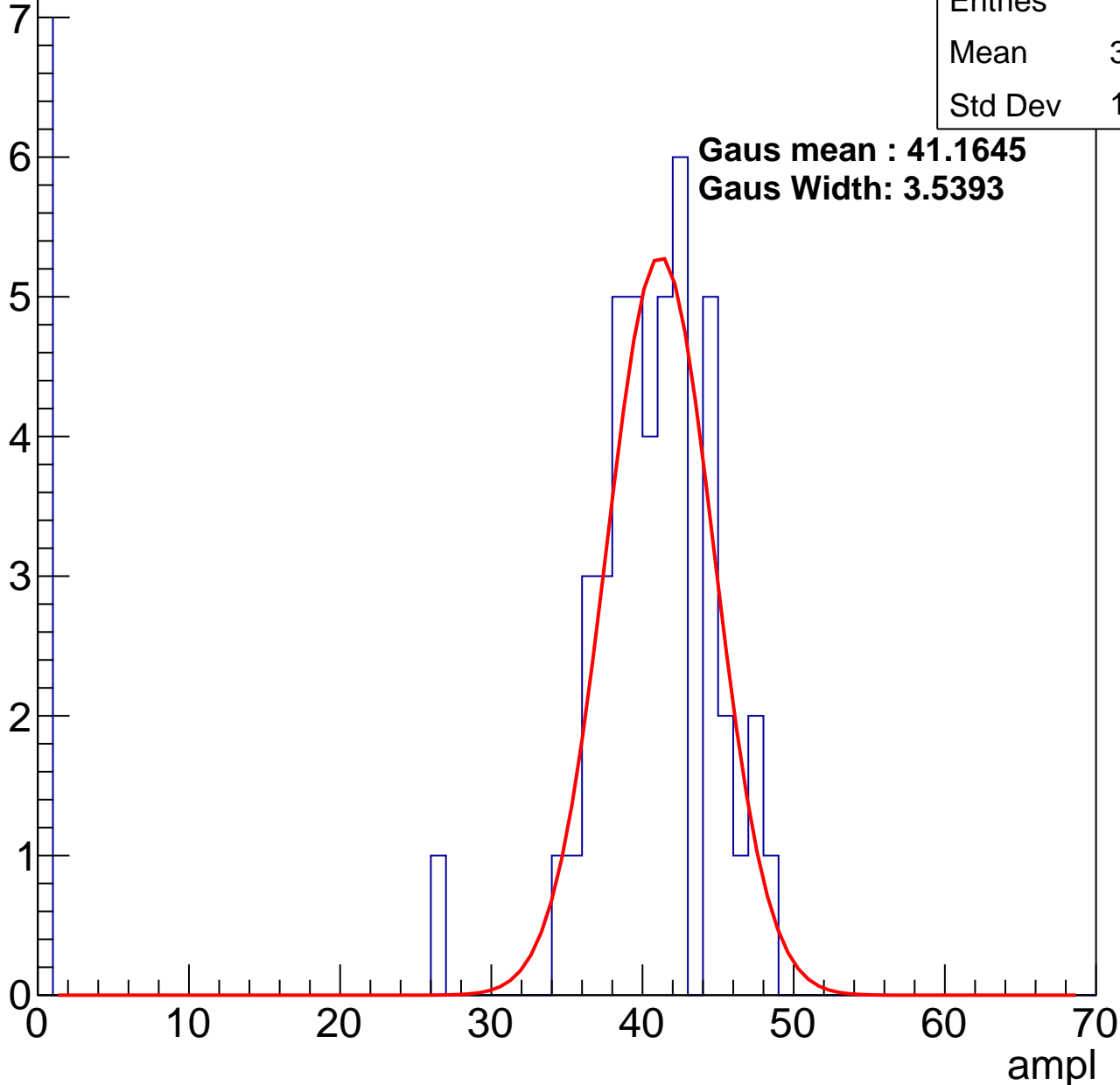
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	34.88
Std Dev	14.25

Gaus mean : 41.1645

Gaus Width: 3.5393



B1L103S, U7-ch98, adc3

calib_packv5_041523_1651.root, FC#0, port C2

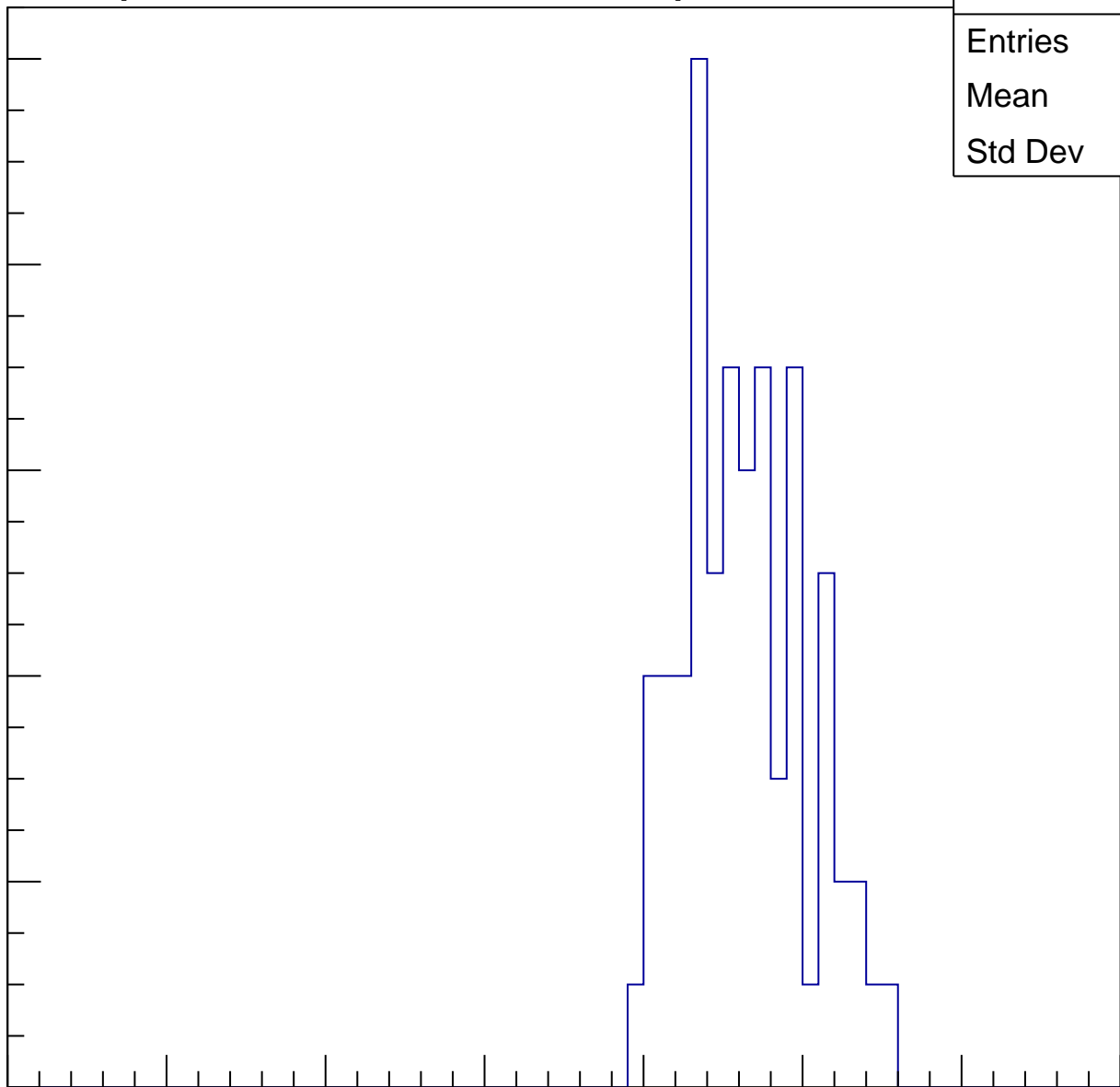
Entries	70
Mean	45.89
Std Dev	3.801

Entry

10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

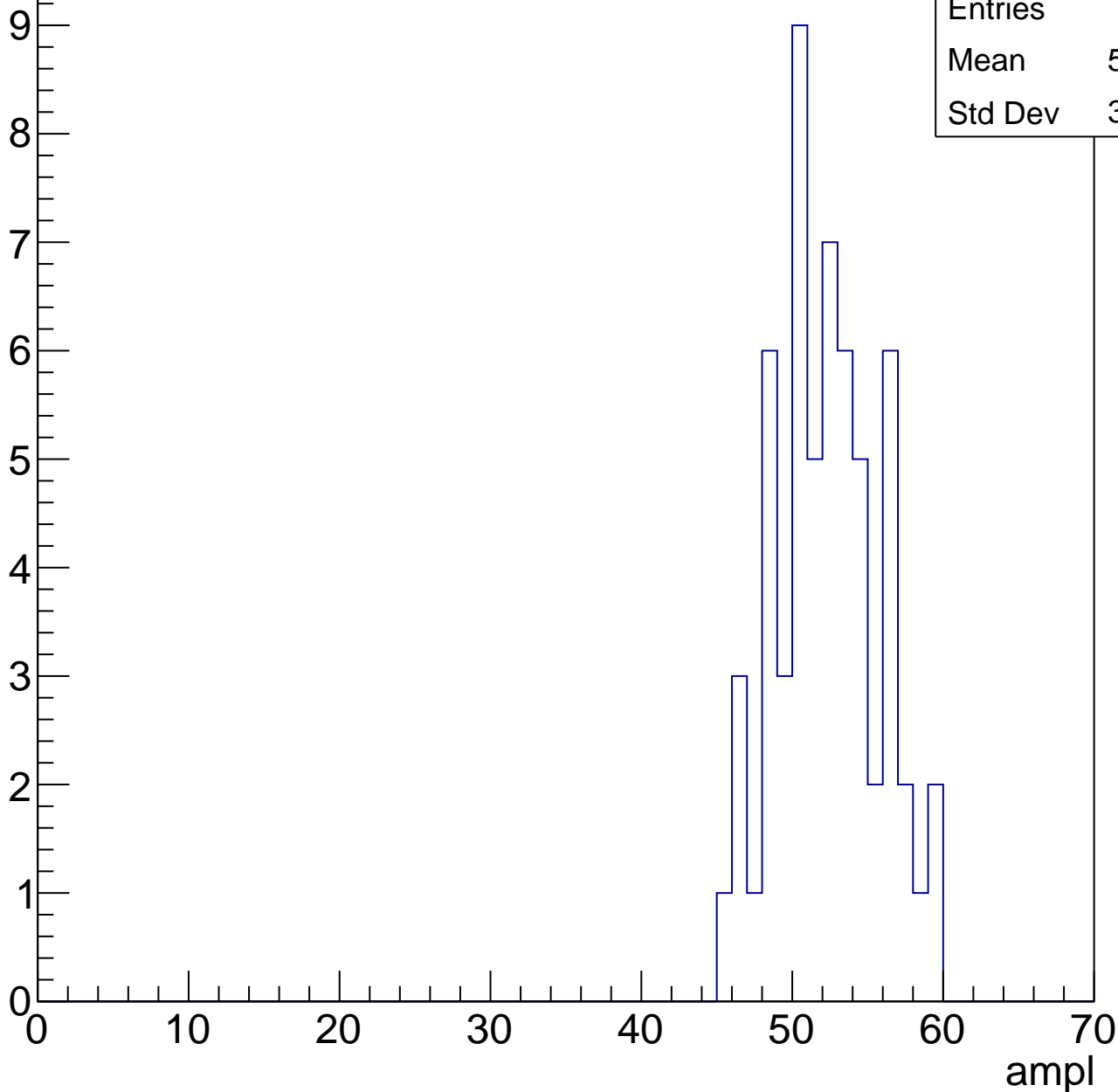


B1L103S, U7-ch98, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	51.83
Std Dev	3.366

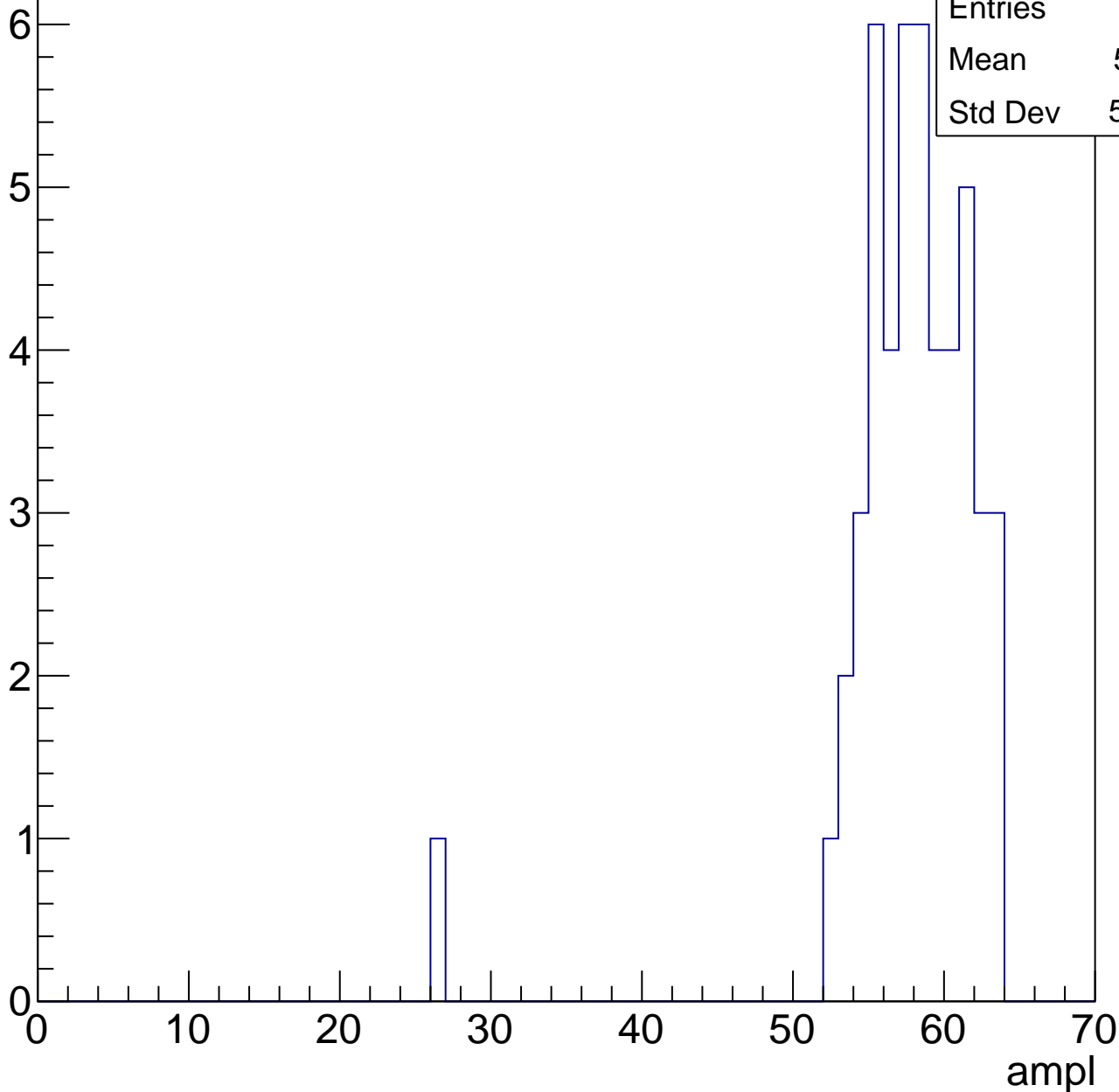


B1L103S, U7-ch98, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	48
Mean	57.21
Std Dev	5.385

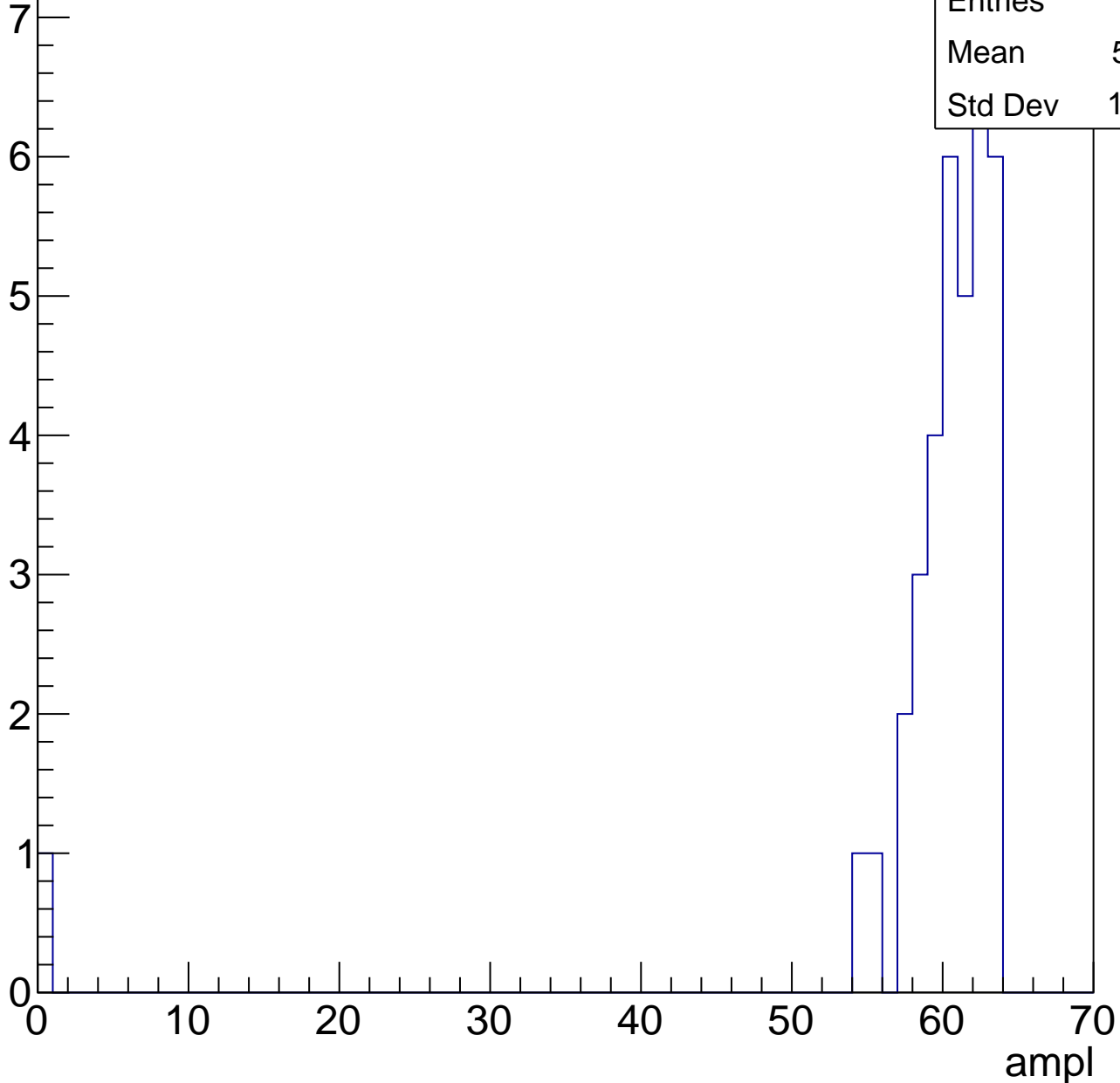


B1L103S, U7-ch98, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	36
Mean	58.61
Std Dev	10.16



B1L103S, U7-ch98, adc7

calib_packv5_041523_1651.root, FC#0, port C2

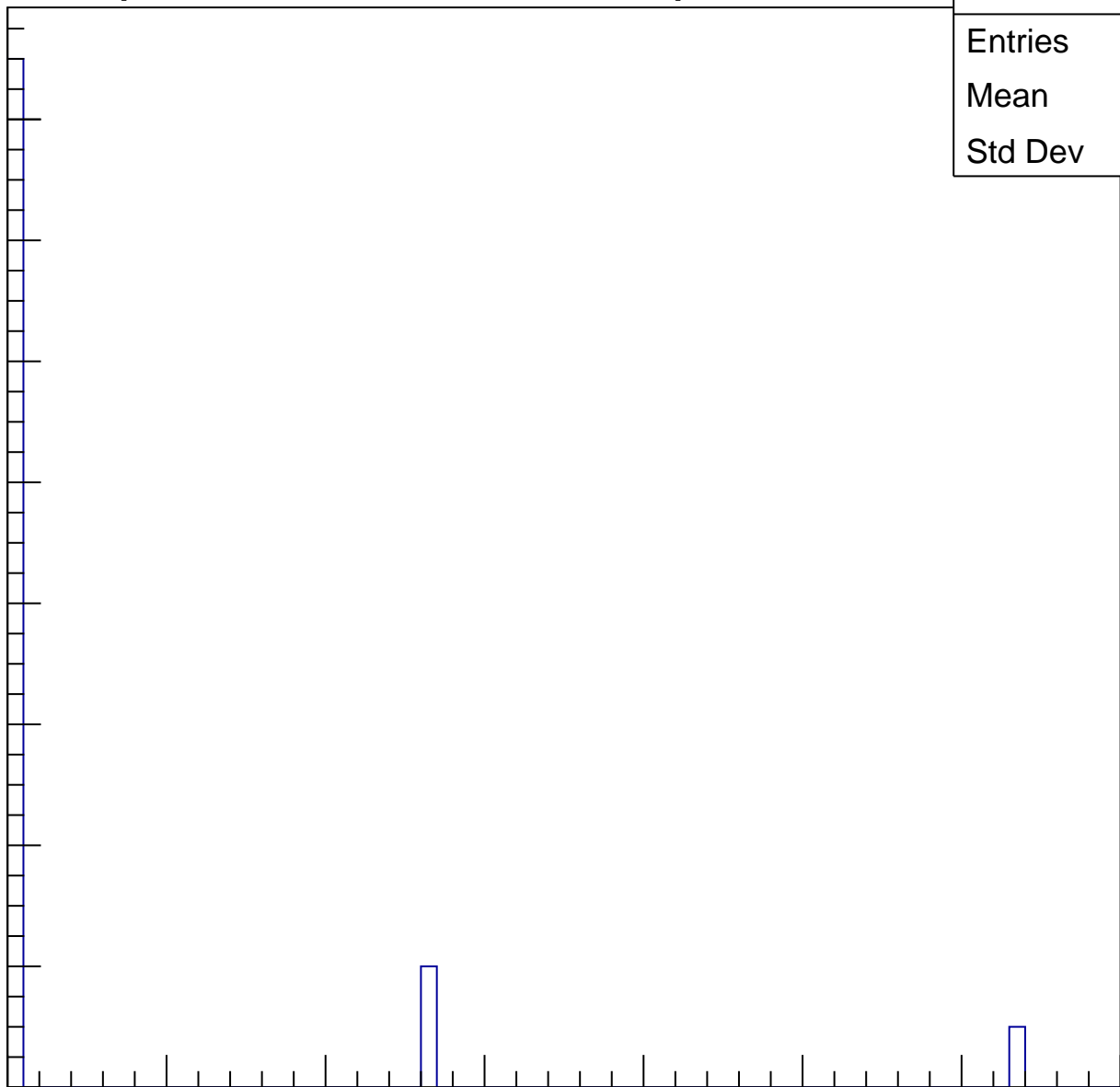
Entries	20
Mean	5.75
Std Dev	15.26

Entry

16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl



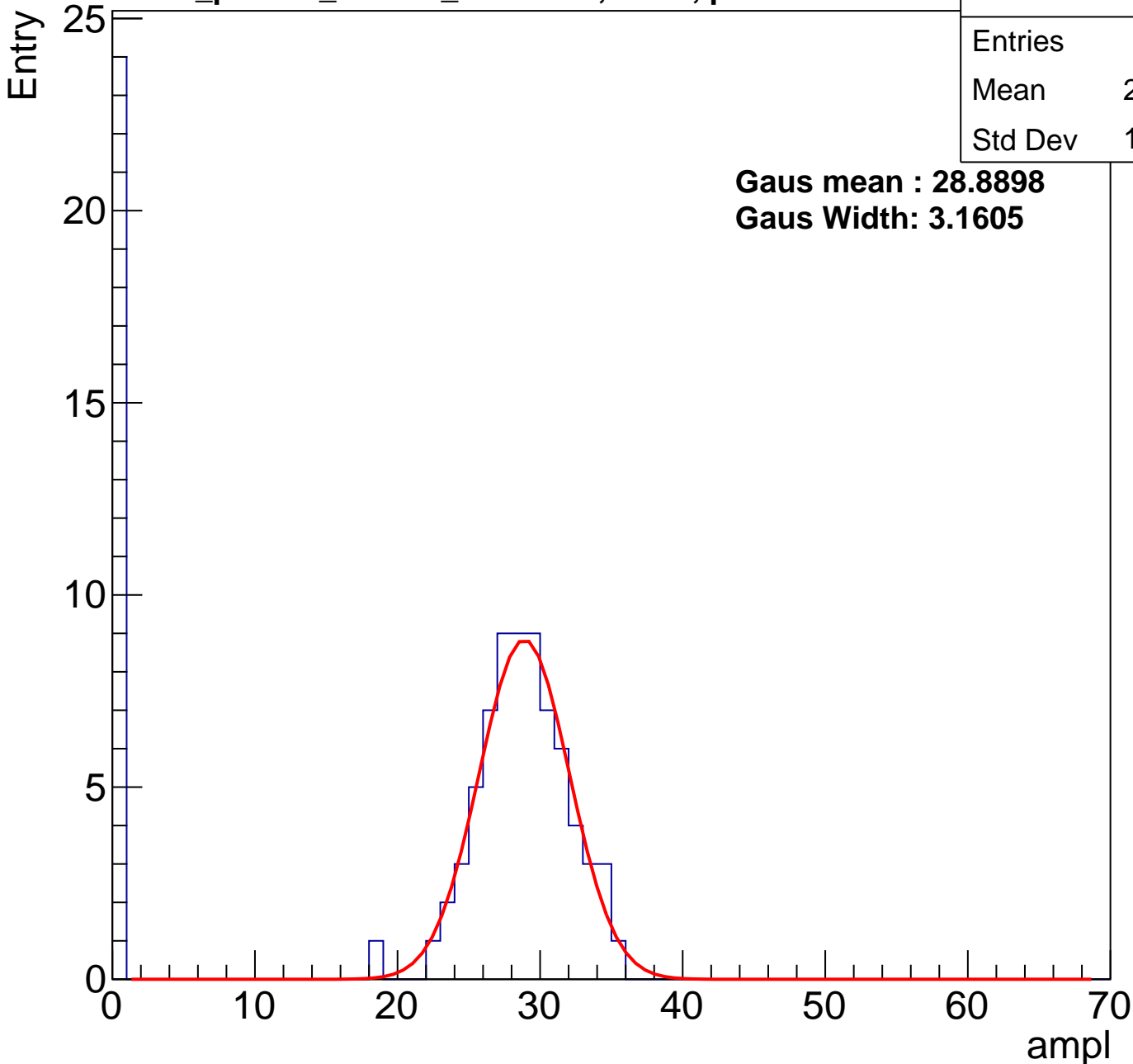
B1L103S, U7-ch99, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	94
Mean	21.07
Std Dev	12.64

Gaus mean : 28.8898

Gaus Width: 3.1605



B1L103S, U7-ch99, adc1

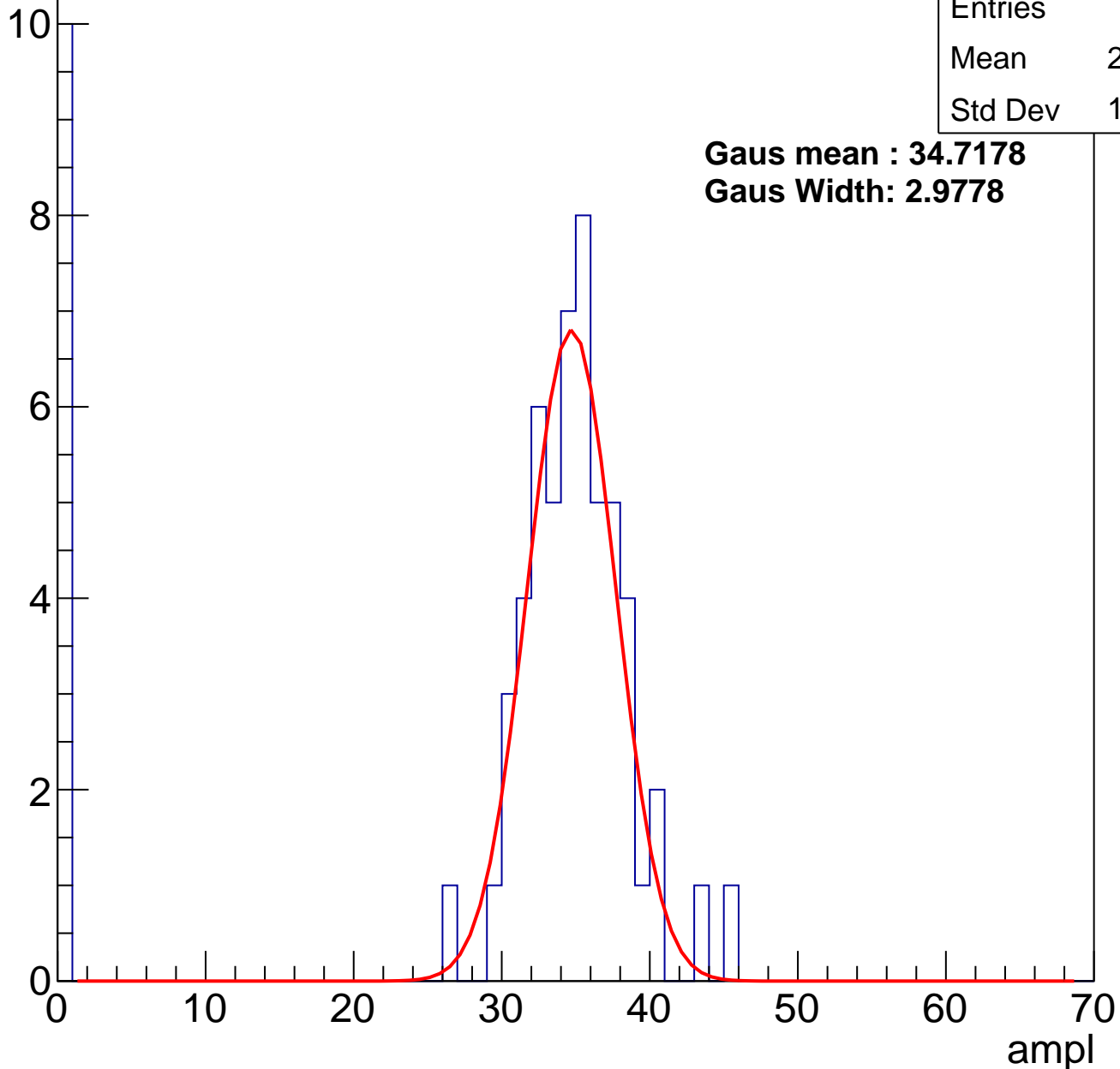
calib_packv5_041523_1651.root, FC#0, port C2

Entries	64
Mean	29.19
Std Dev	12.94

Gaus mean : 34.7178

Gaus Width: 2.9778

Entry



B1L103S, U7-ch99, adc2

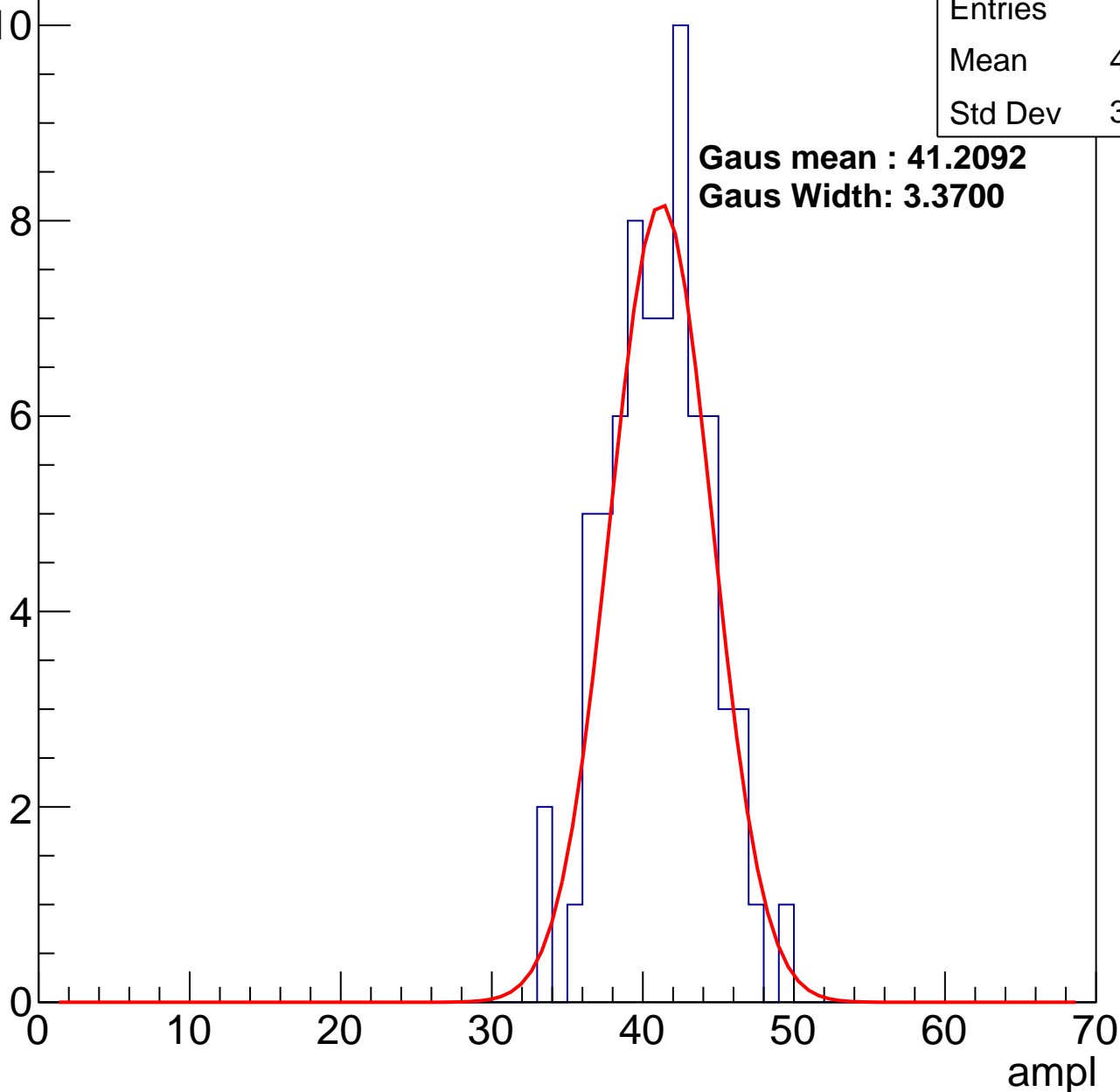
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	40.62
Std Dev	3.278

Gaus mean : 41.2092

Gaus Width: 3.3700



B1L103S, U7-ch99, adc3

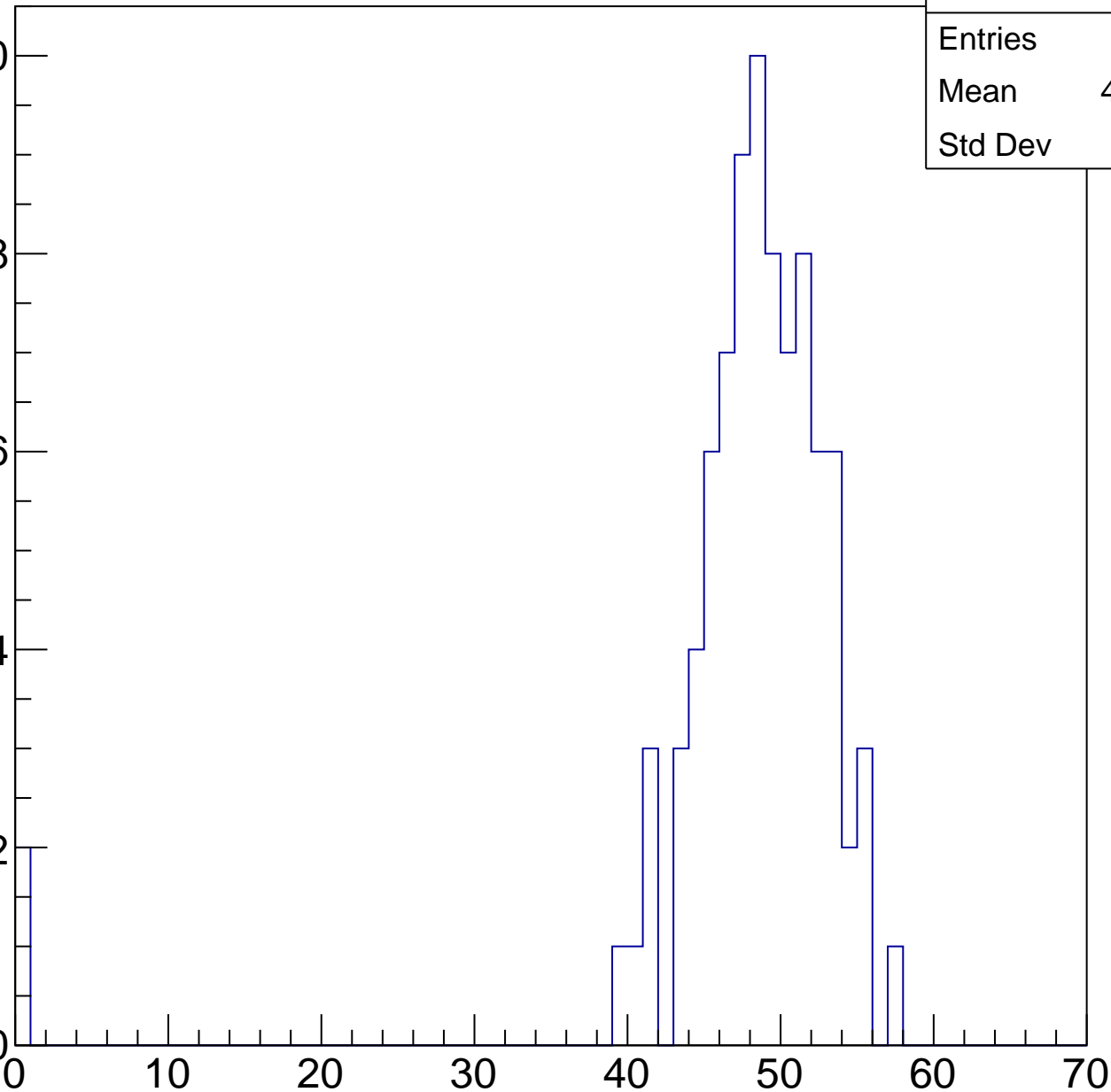
calib_packv5_041523_1651.root, FC#0, port C2

Entries	87
Mean	47.26
Std Dev	8.12

Entry

10
8
6
4
2
0

ampl

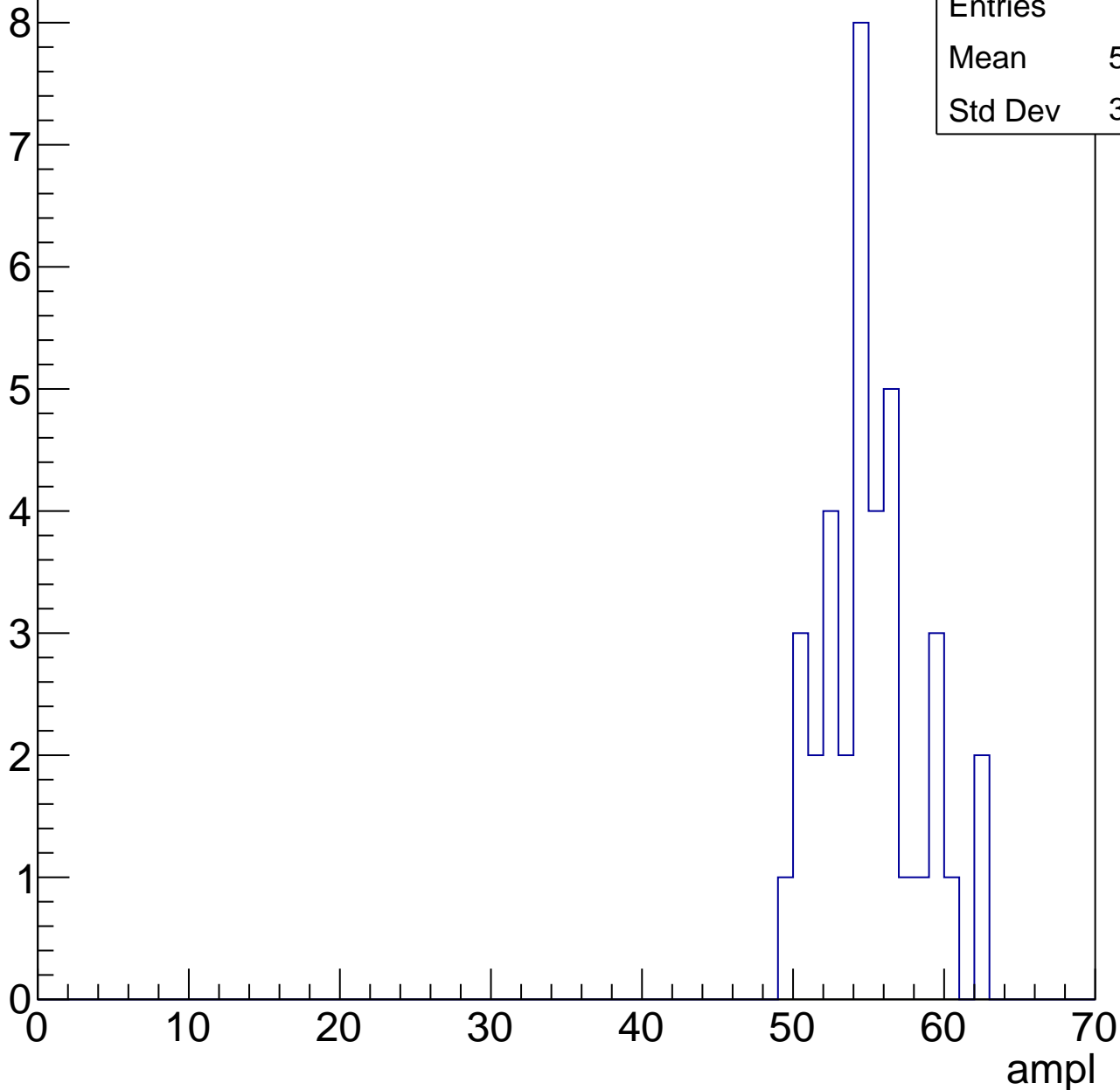


B1L103S, U7-ch99, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	37
Mean	54.68
Std Dev	3.205

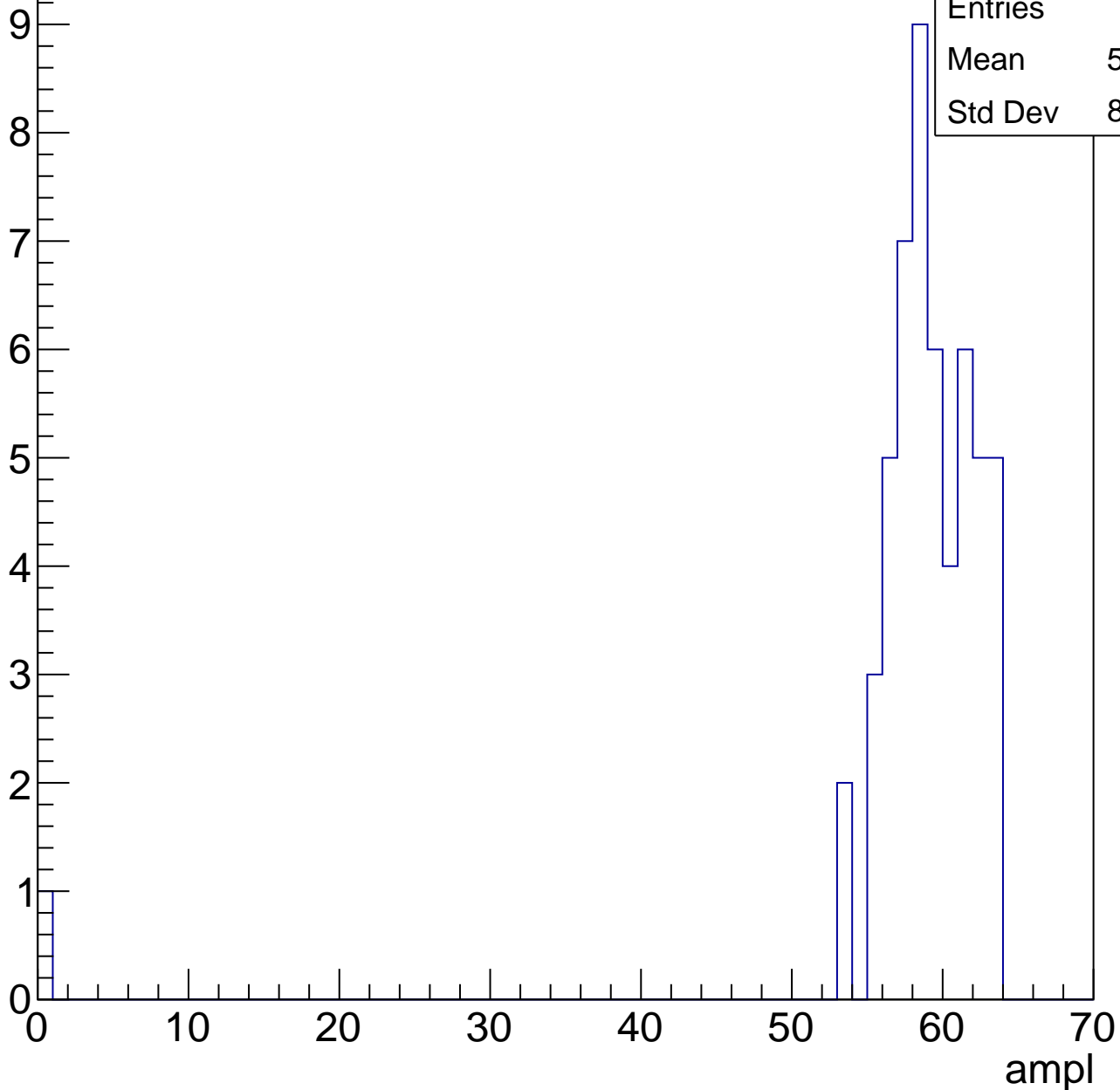


B1L103S, U7-ch99, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	53
Mean	57.68
Std Dev	8.404



B1L103S, U7-ch99, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

5

4

3

2

1

0

Entries	19
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Mean	61.11
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Std Dev	1.586
---------	-------

ampl

0

10

20

30

40

50

60

70

B1L103S, U7-ch99, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

Entries	19
Mean	0
Std Dev	0

ampl

B1L103S, U7-ch100, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	17.07
Std Dev	13.27

Gaus mean : 27.7438

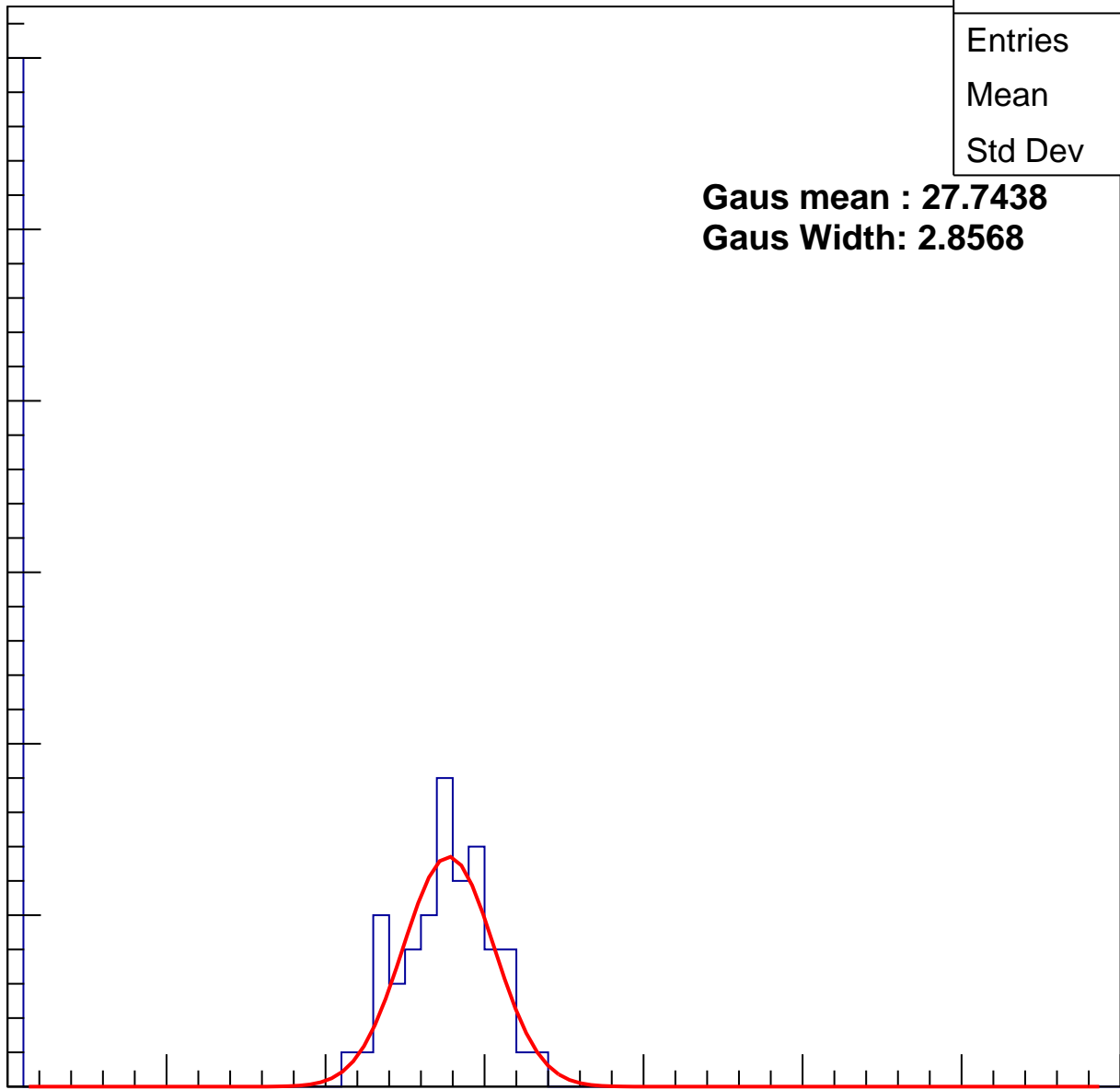
Gaus Width: 2.8568

Entry

30
25
20
15
10
5
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U7-ch100, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	87
Mean	30.13
Std Dev	11.4

Gaus mean : 34.6939

Gaus Width: 4.1109

Entry

10

8

6

4

2

0

0

10

20

30

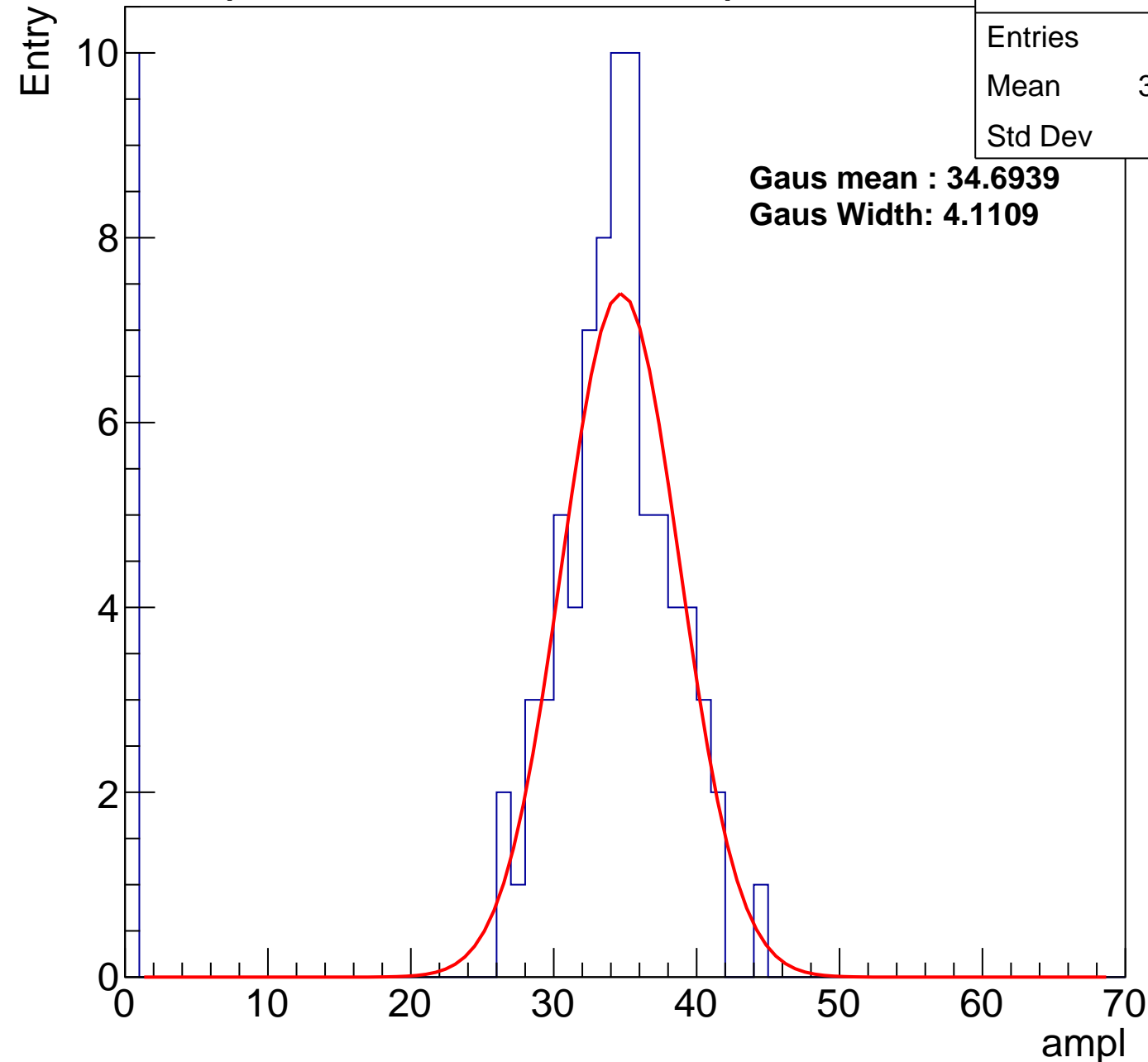
40

50

60

70

ampl



B1L103S, U7-ch100, adc2

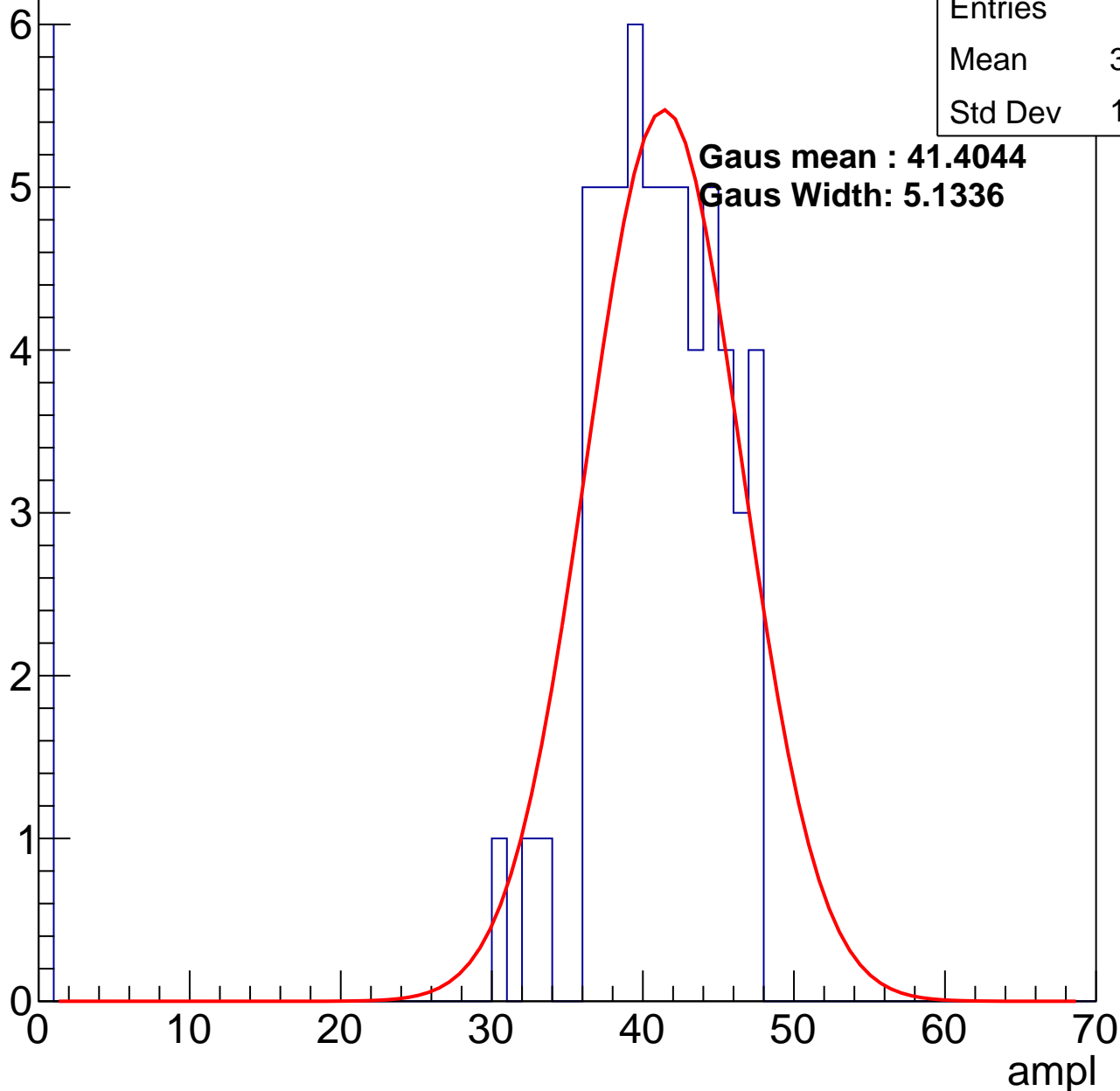
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	36.88
Std Dev	12.33

Gaus mean : 41.4044

Gaus Width: 5.1336

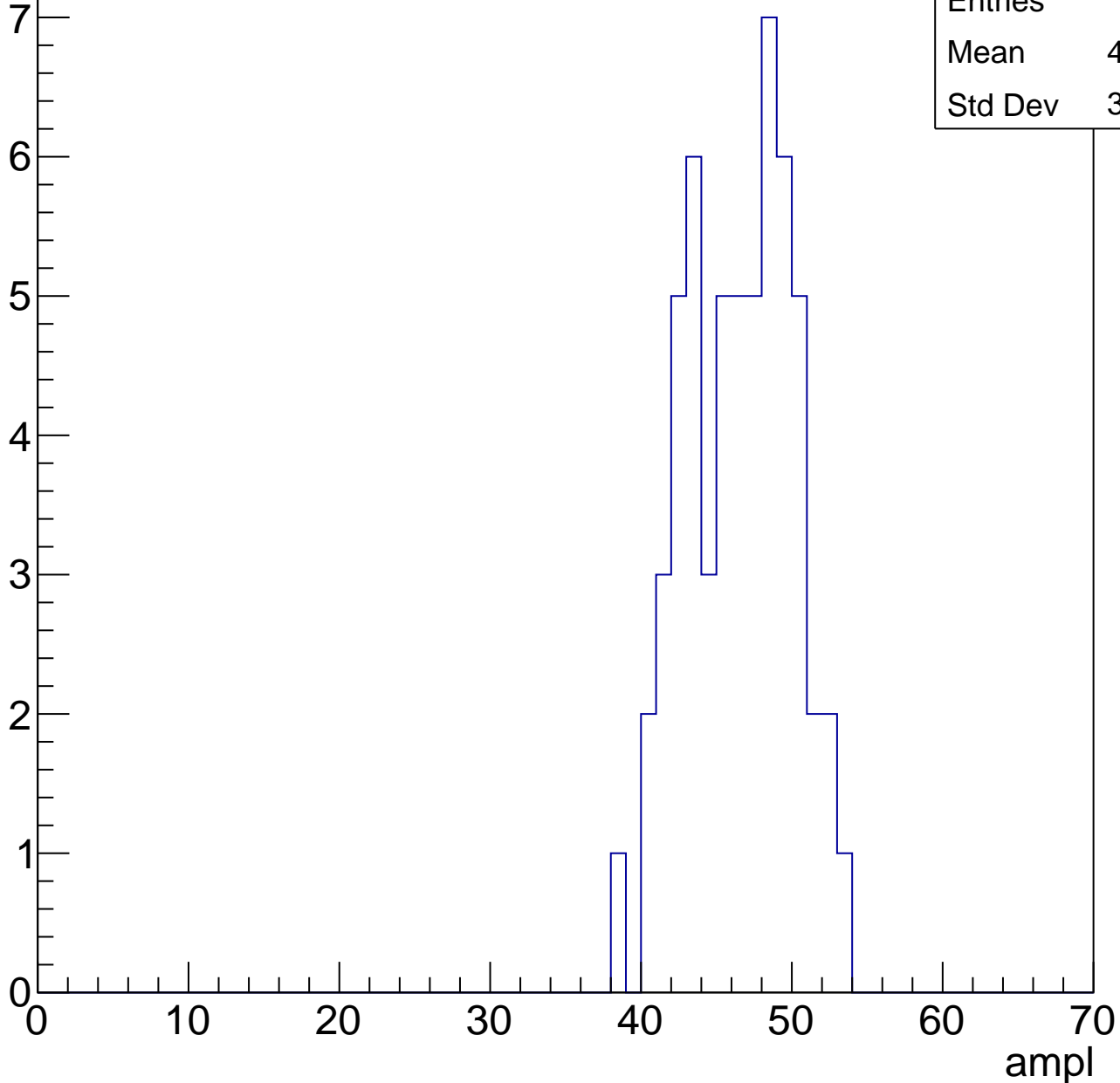


B1L103S, U7-ch100, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	46.03
Std Dev	3.474

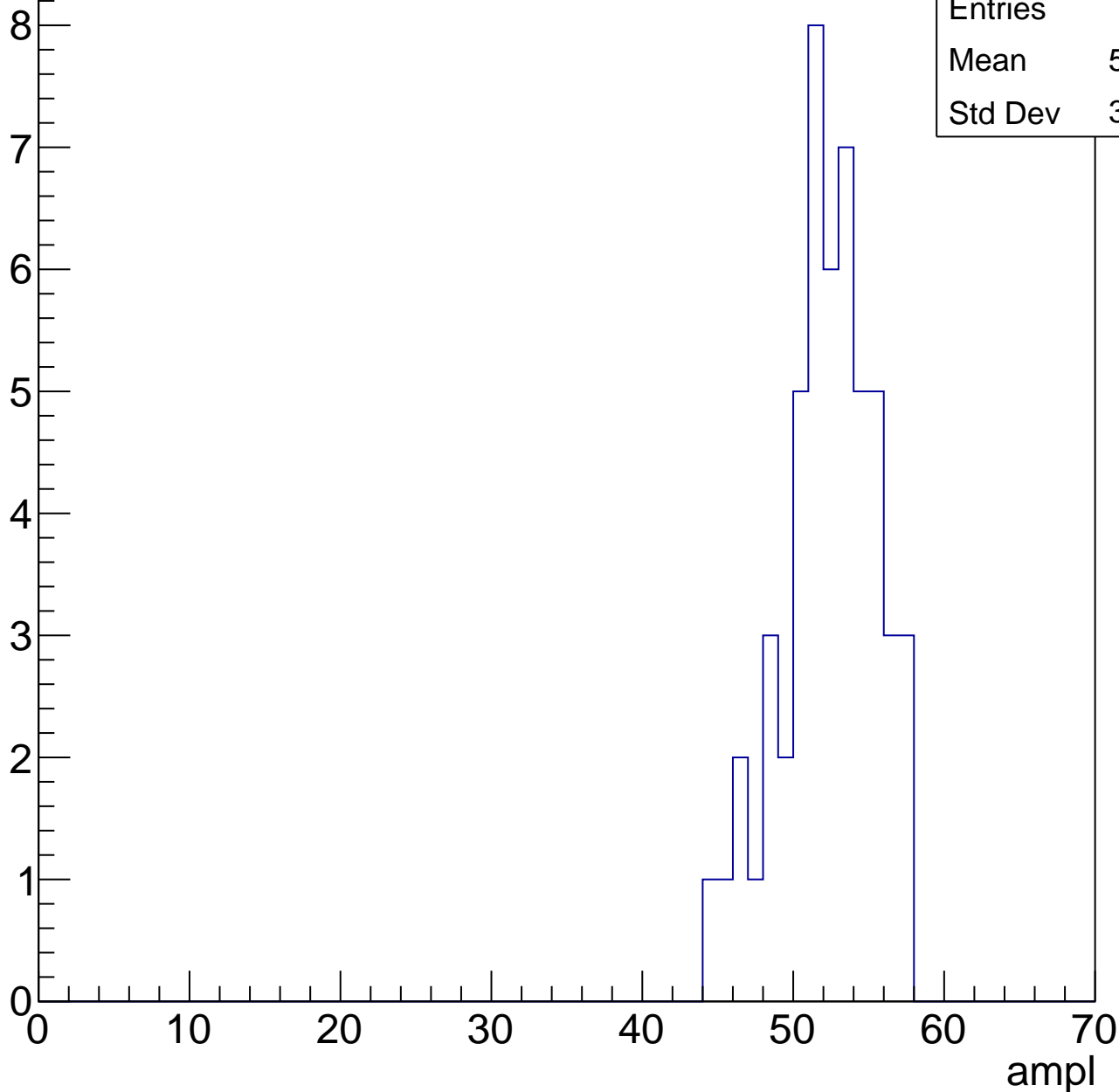


B1L103S, U7-ch100, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

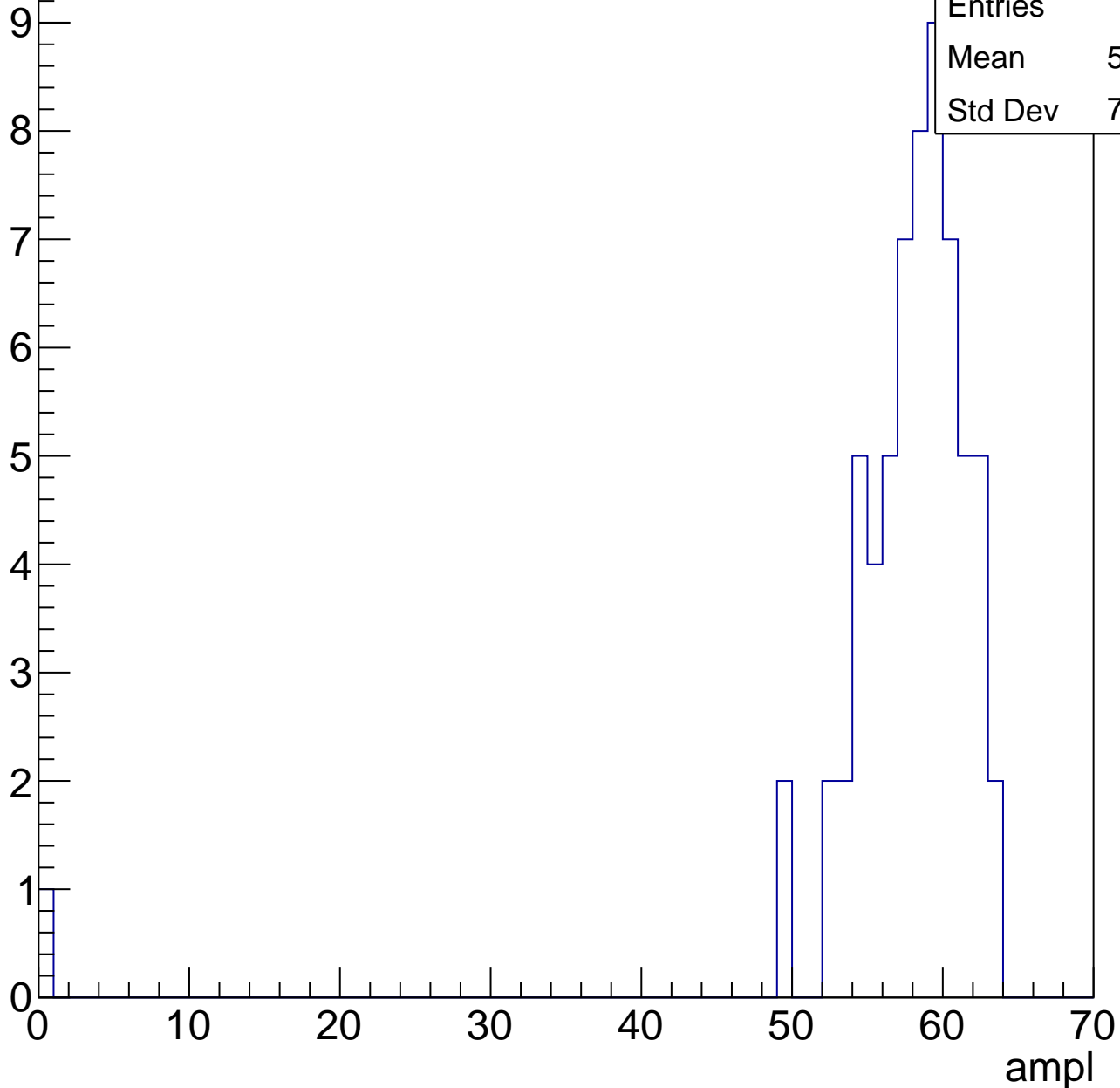
Entries	52
Mean	51.83
Std Dev	3.093



B1L103S, U7-ch100, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

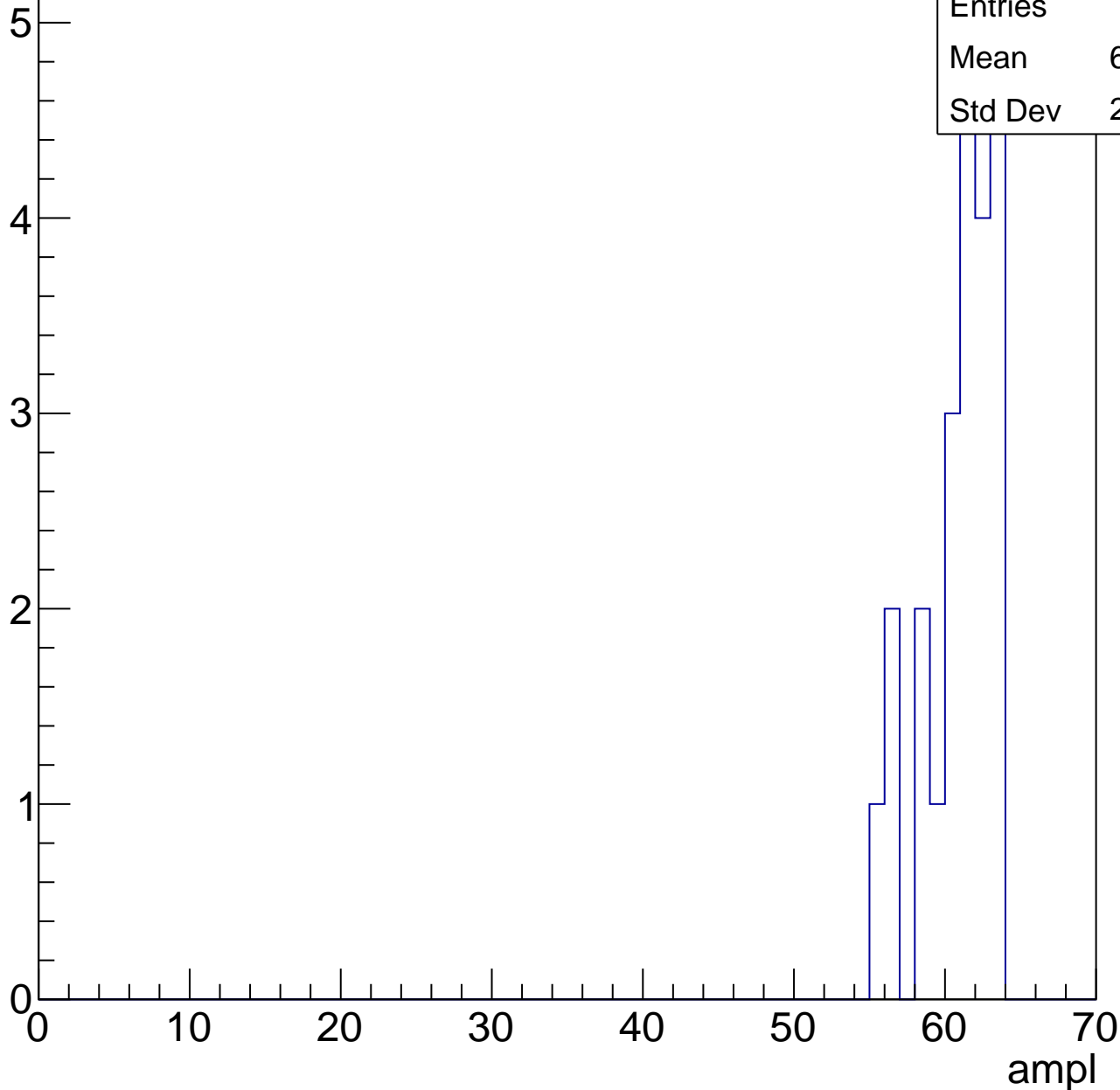


B1L103S, U7-ch100, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	23
Mean	60.43
Std Dev	2.356

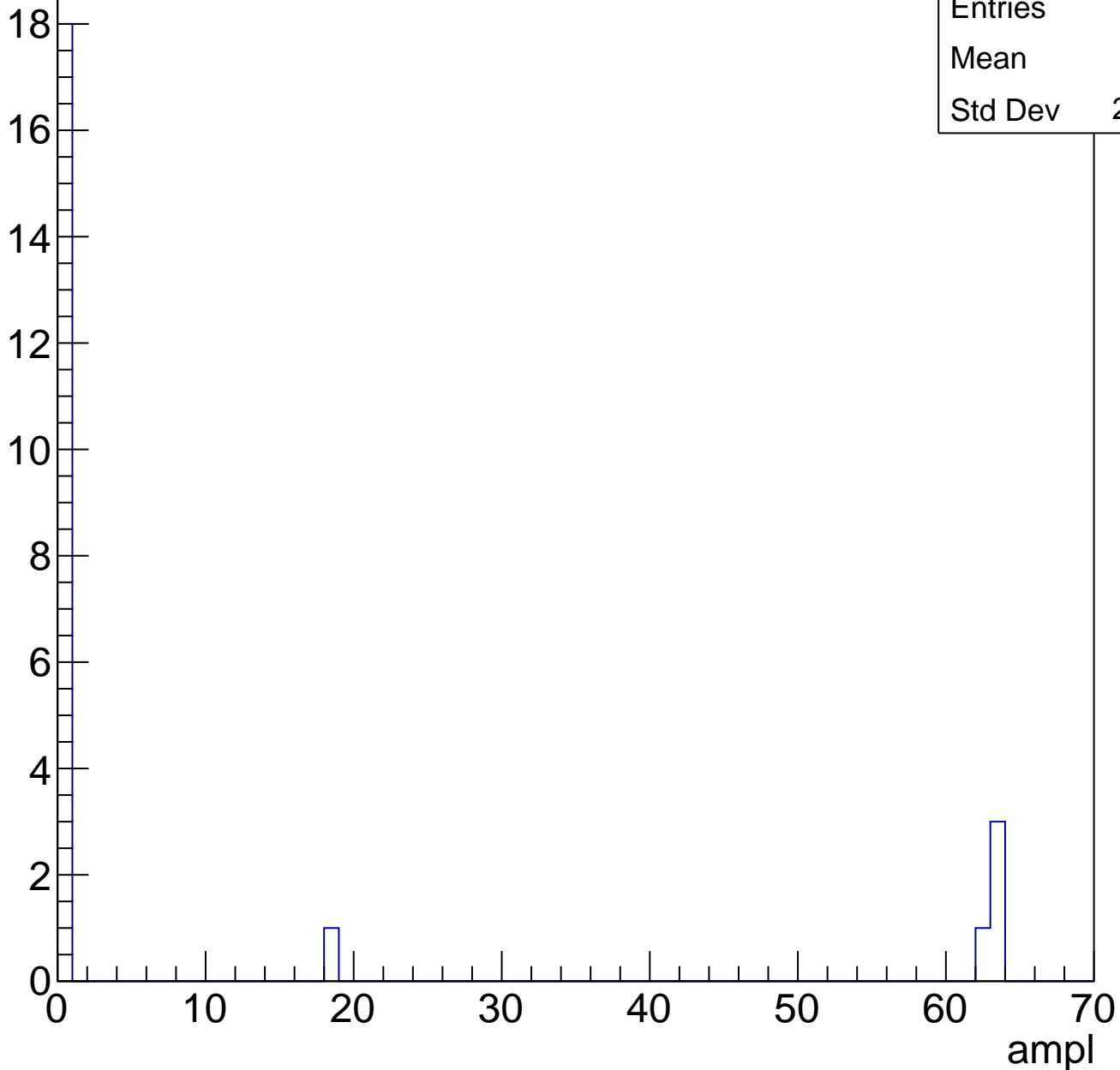


B1L103S, U7-ch100, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	23
Mean	11.7
Std Dev	23.71

Entry



B1L103S, U7-ch101, adc0

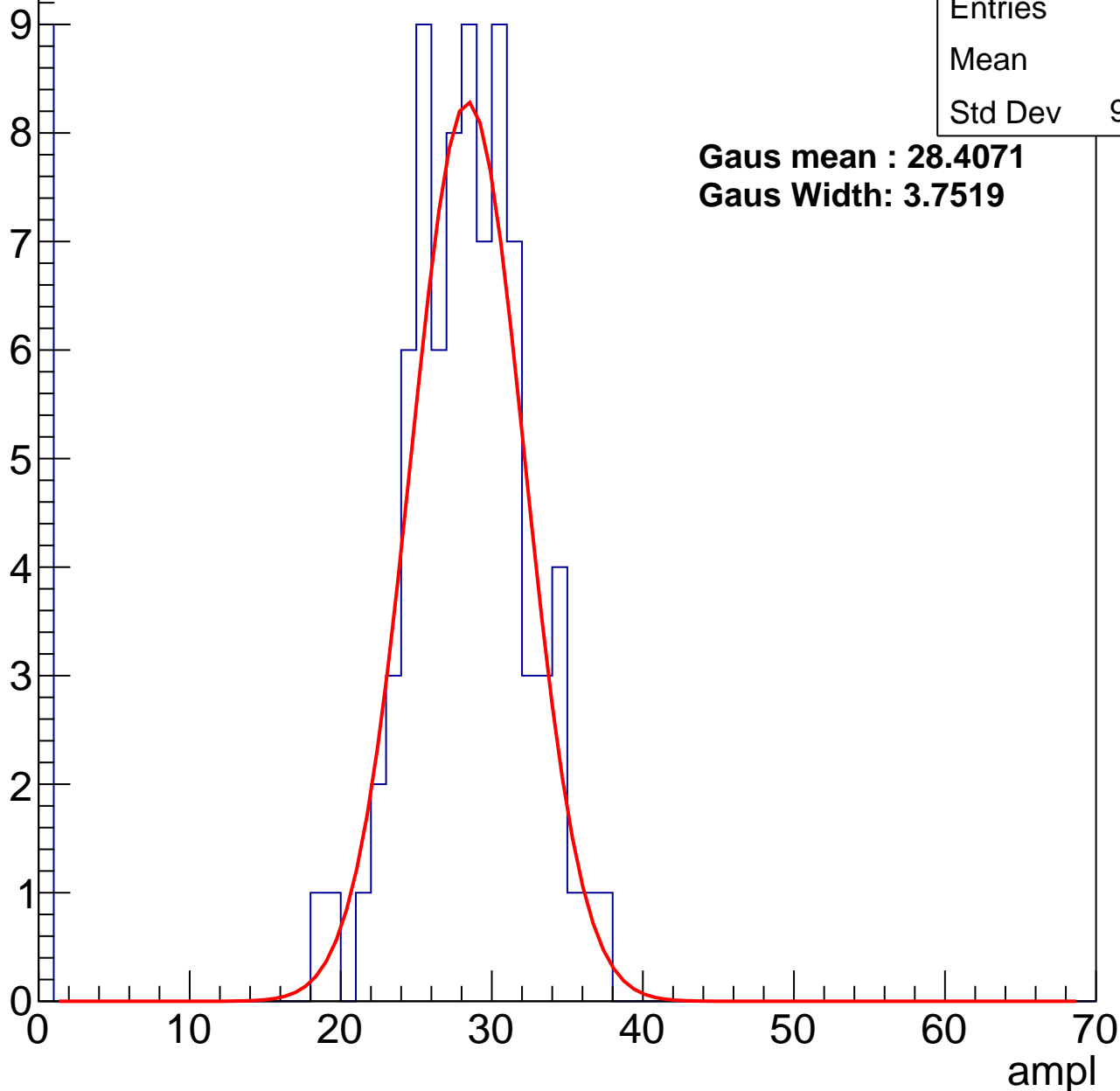
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	91
Mean	25.2
Std Dev	9.075

Gaus mean : 28.4071

Gaus Width: 3.7519



B1L103S, U7-ch101, adc1

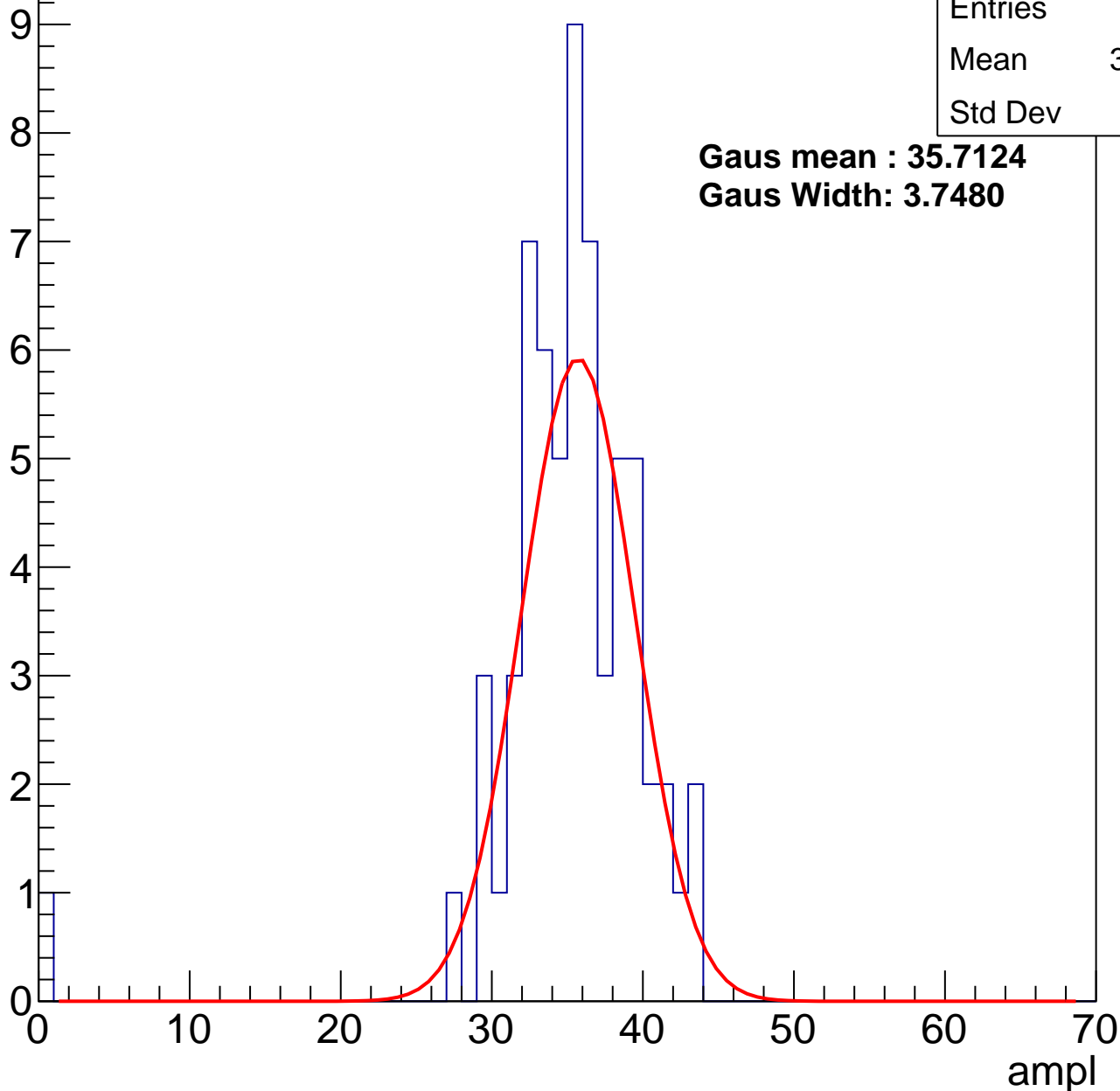
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	34.63
Std Dev	5.63

Gaus mean : 35.7124

Gaus Width: 3.7480



B1L103S, U7-ch101, adc2

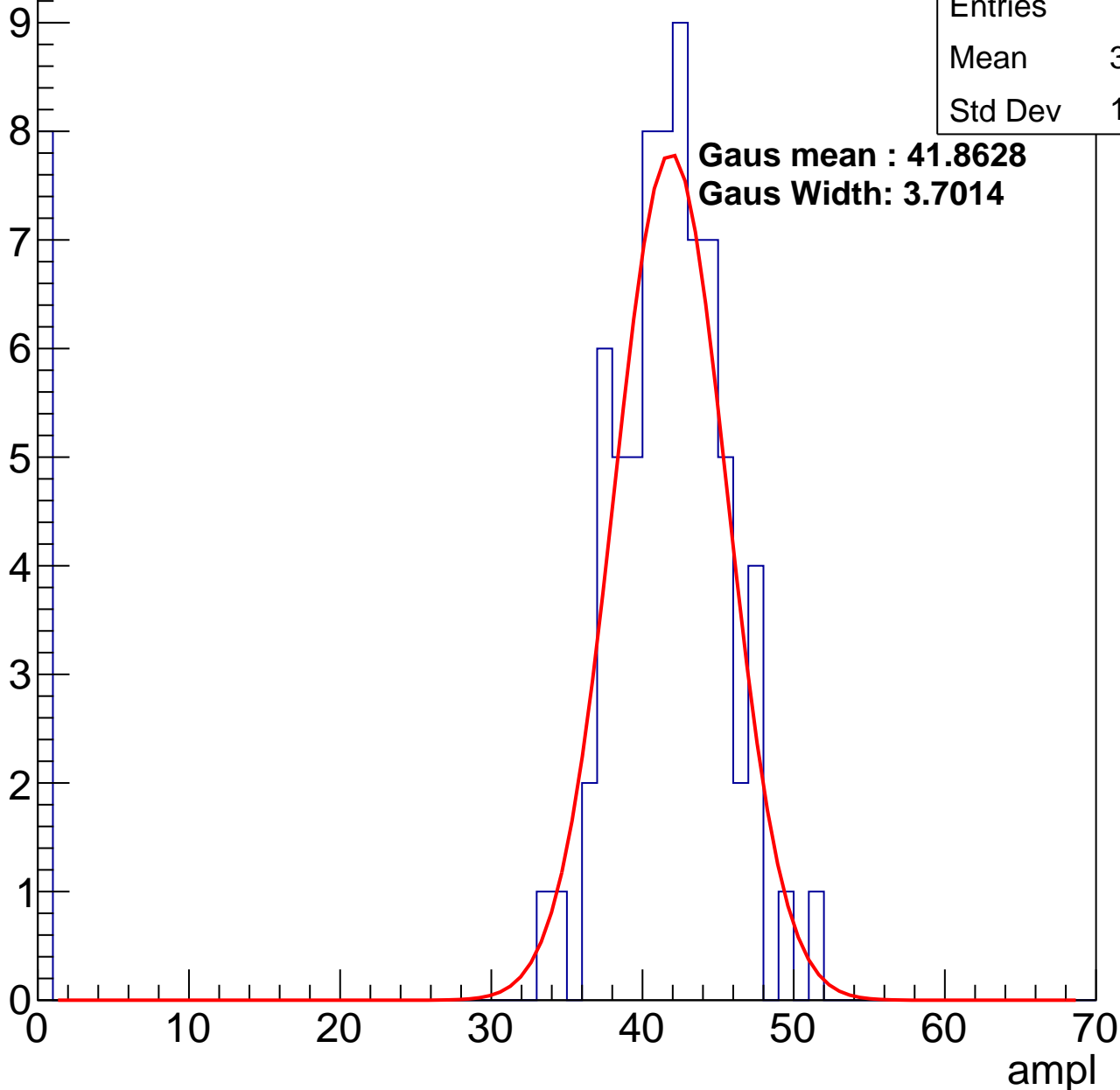
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	80
Mean	37.33
Std Dev	12.86

Gaus mean : 41.8628

Gaus Width: 3.7014

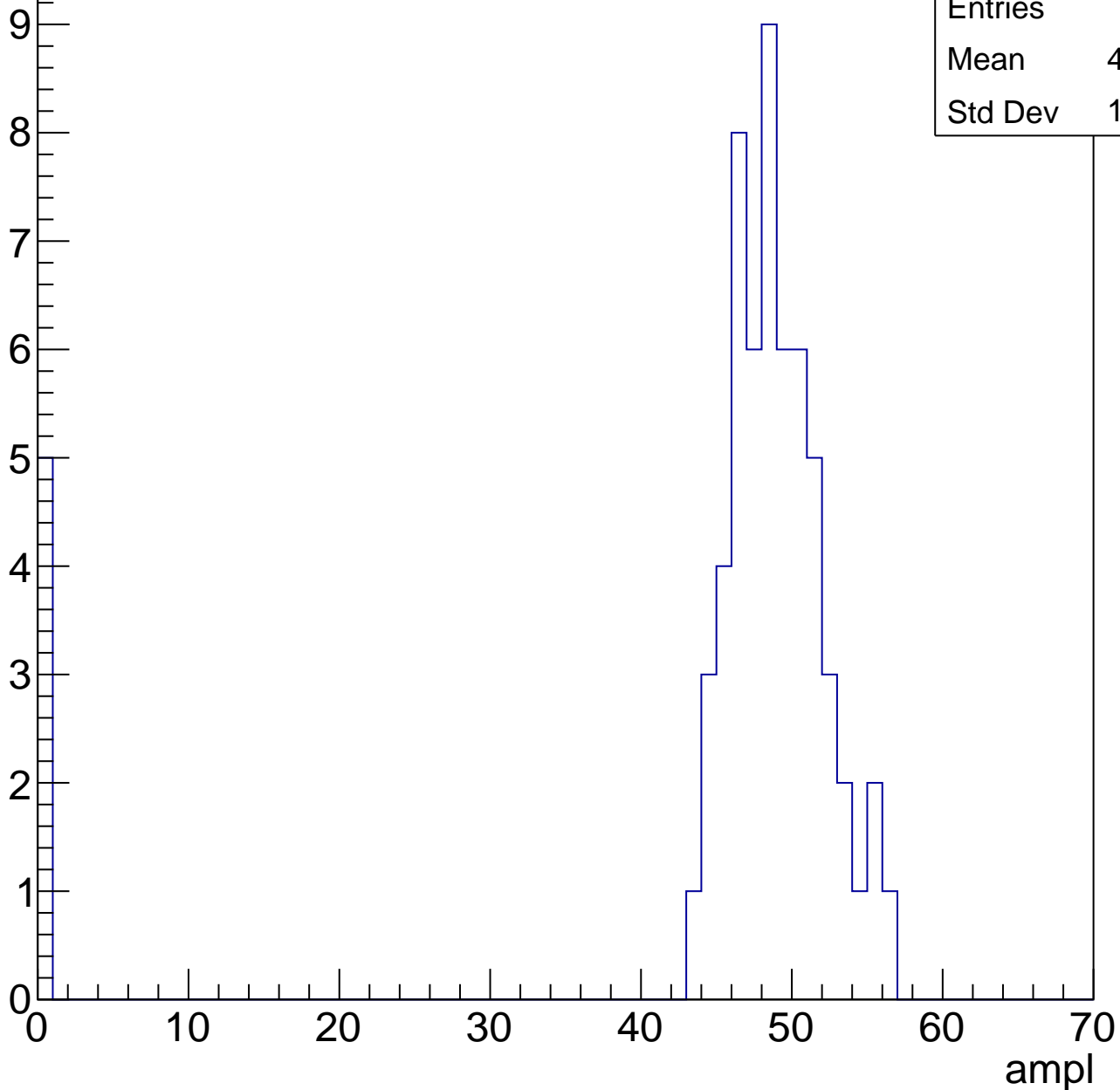


B1L103S, U7-ch101, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	44.65
Std Dev	13.52

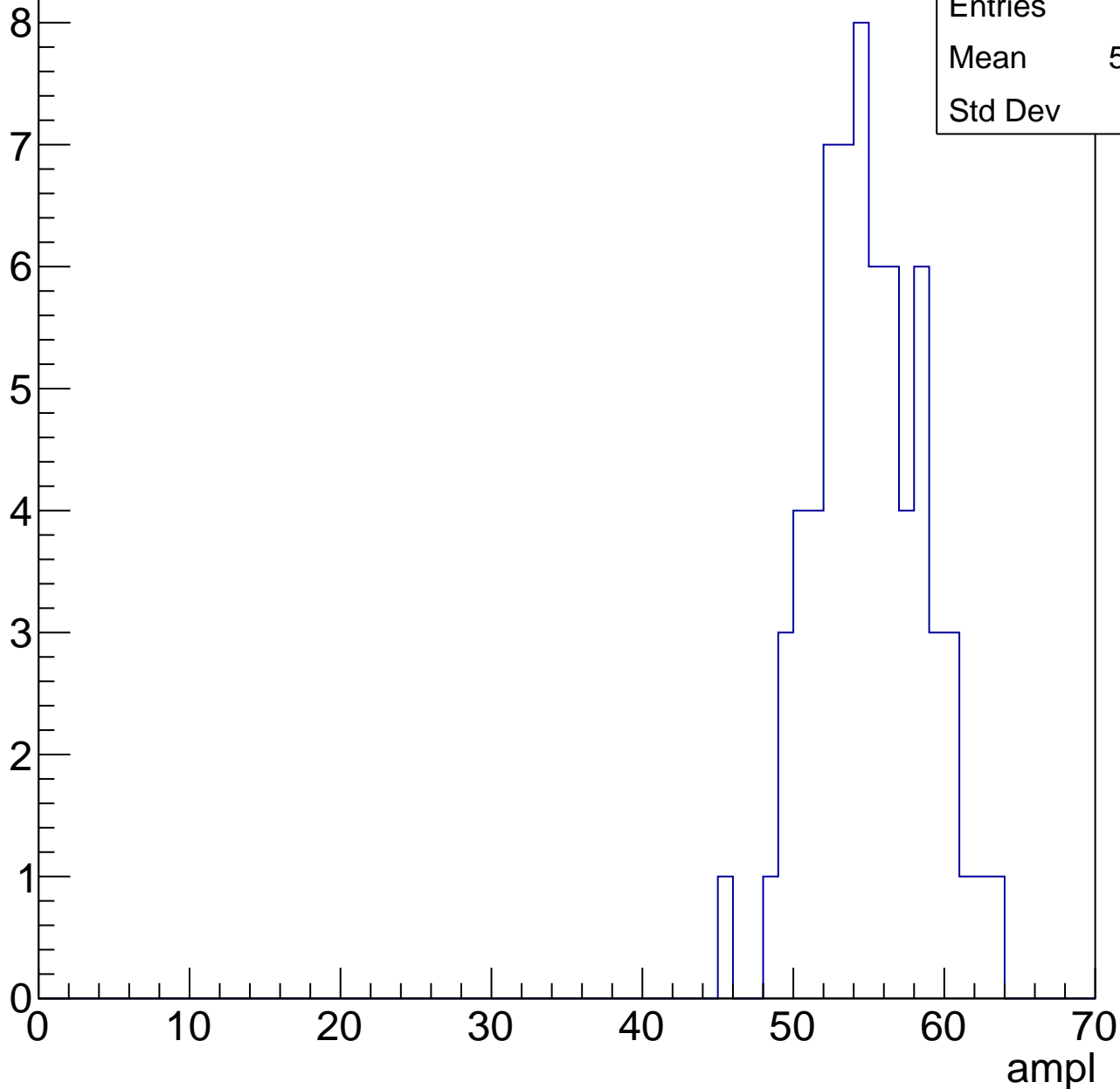


B1L103S, U7-ch101, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

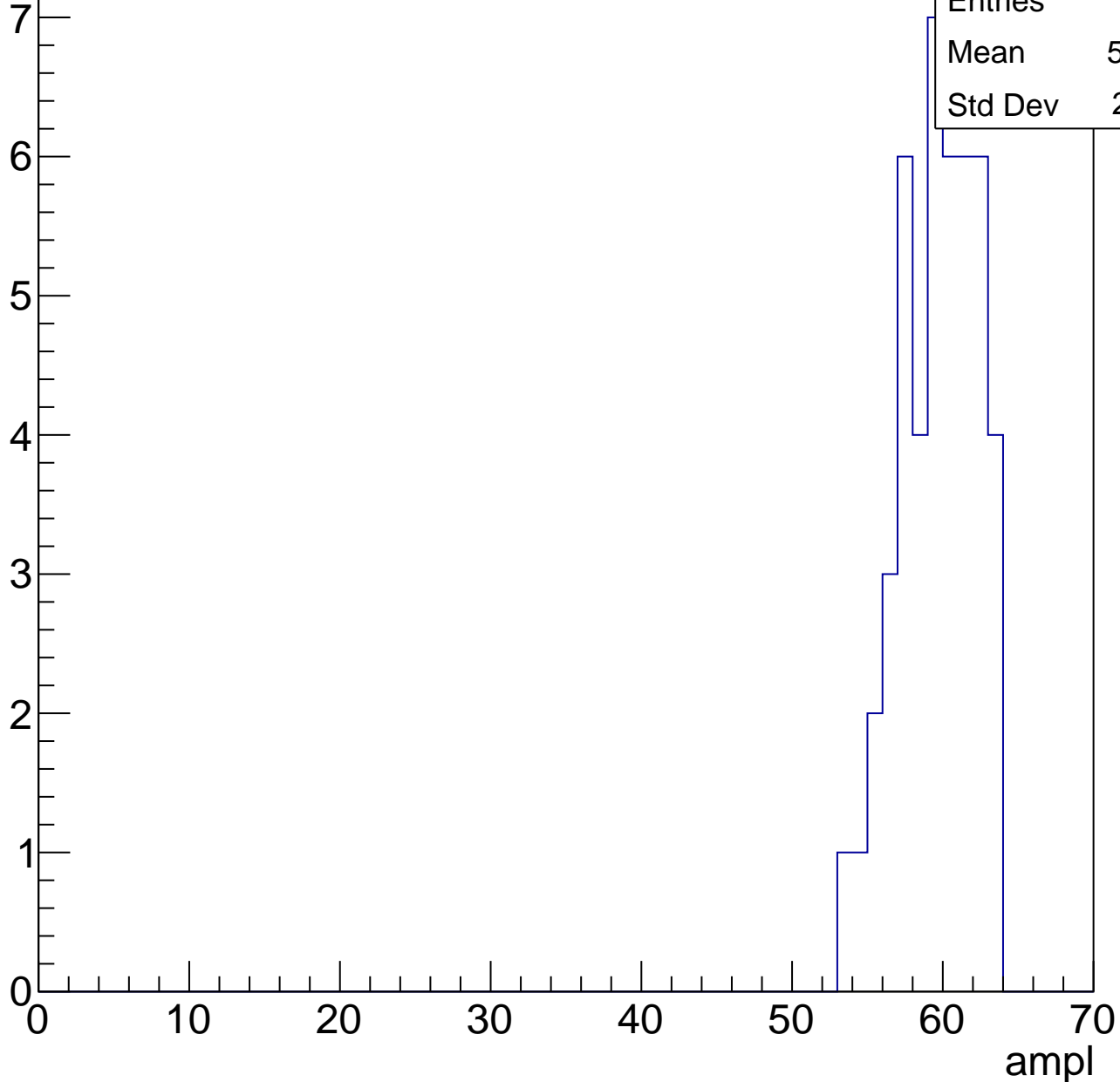
Entries	66
Mean	54.48
Std Dev	3.59



B1L103S, U7-ch101, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

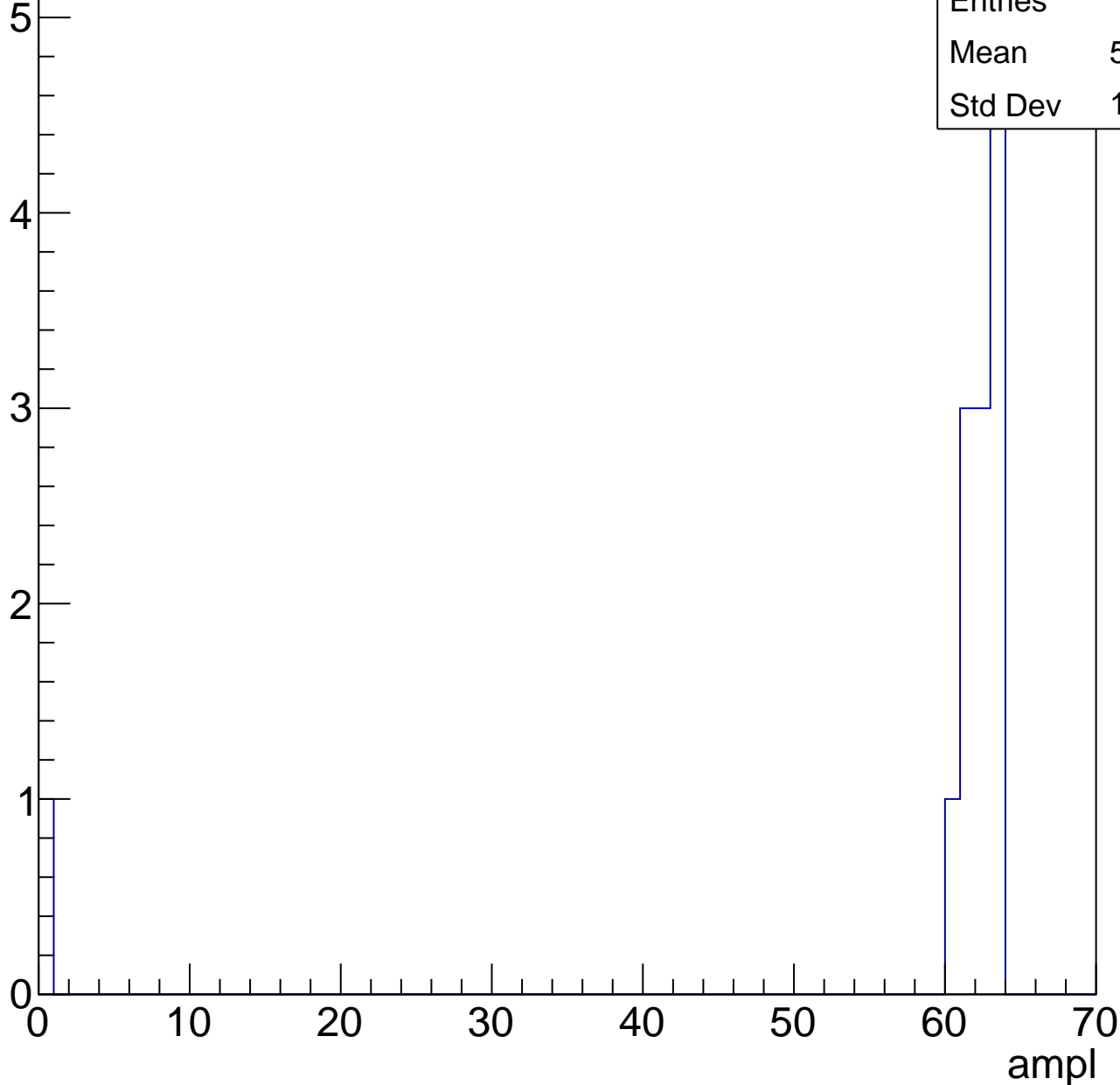


B1L103S, U7-ch101, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	13
Mean	57.23
Std Dev	16.55



B1L103S, U7-ch101, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U7-ch102, adc0

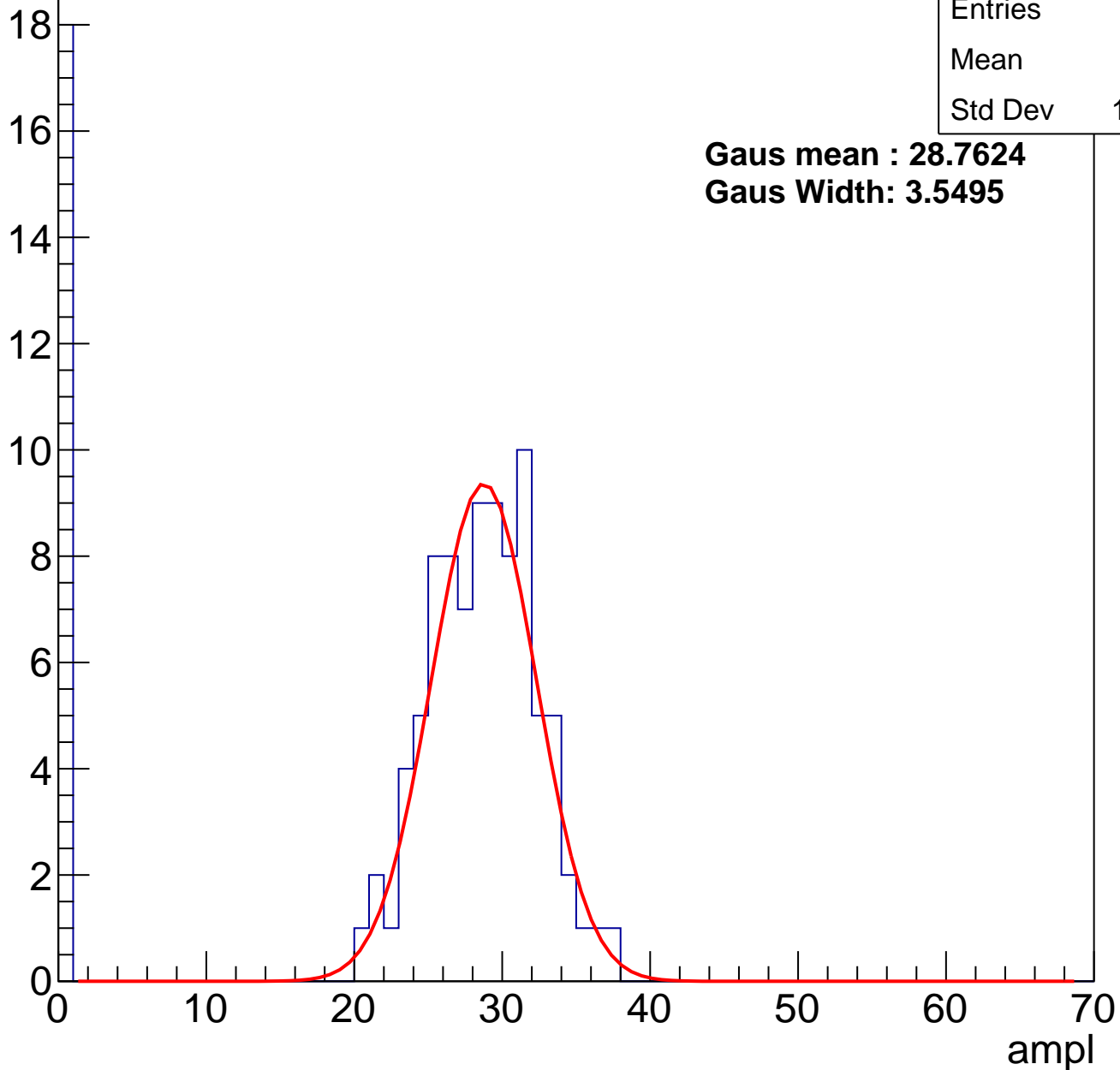
calib_packv5_041523_1651.root, FC#0, port C2

Entries	105
Mean	23.4
Std Dev	11.12

Gaus mean : 28.7624

Gaus Width: 3.5495

Entry



B1L103S, U7-ch102, adc1

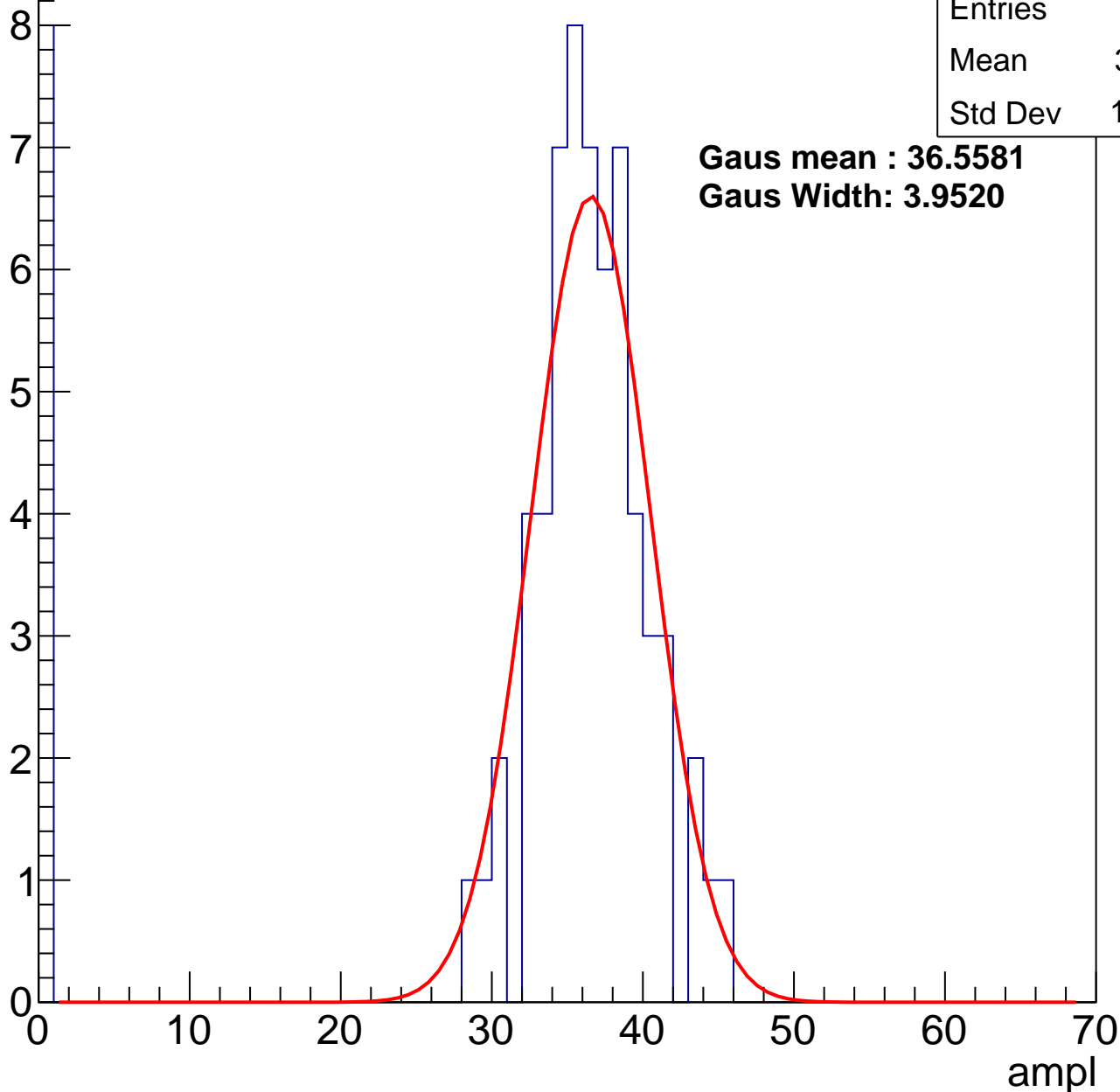
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	32.01
Std Dev	12.06

Gaus mean : 36.5581

Gaus Width: 3.9520



B1L103S, U7-ch102, adc2

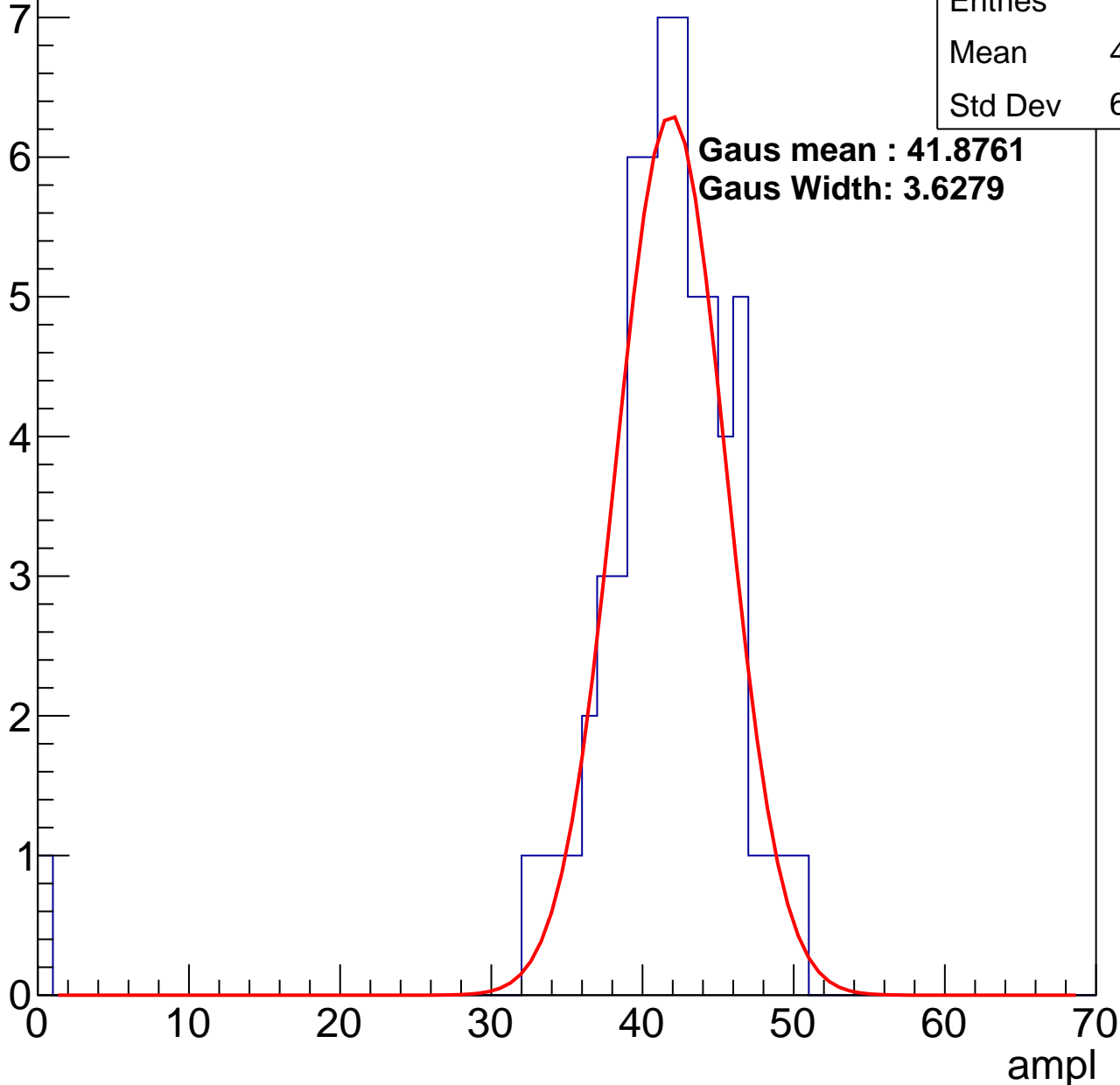
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	40.73
Std Dev	6.416

Gaus mean : 41.8761

Gaus Width: 3.6279

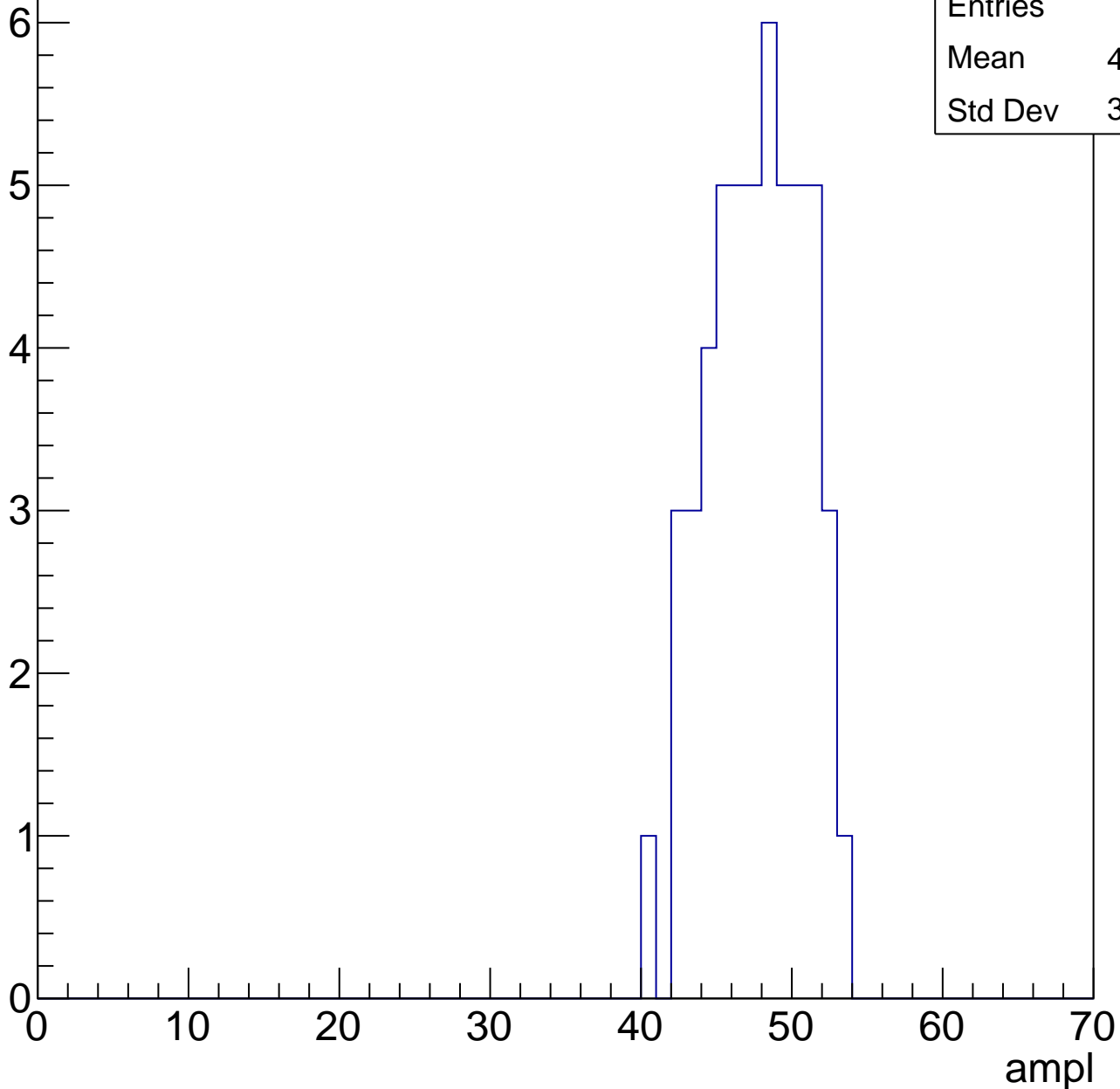


B1L103S, U7-ch102, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

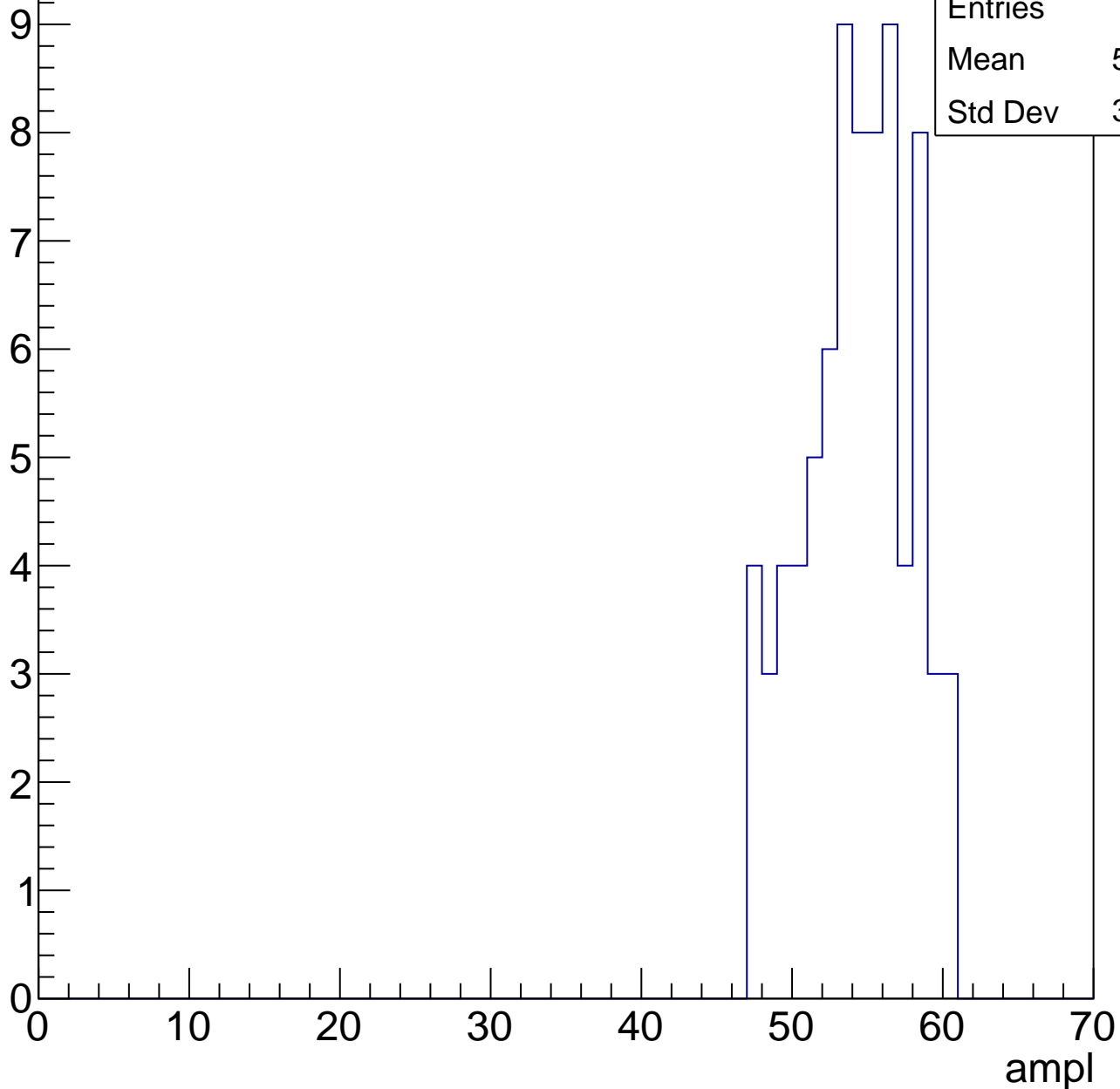
Entries	51
Mean	47.22
Std Dev	3.108



B1L103S, U7-ch102, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch102, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

6

5

4

3

2

1

0

Entries	36
Mean	59
Std Dev	2.819

ampl

0

10

20

30

40

50

60

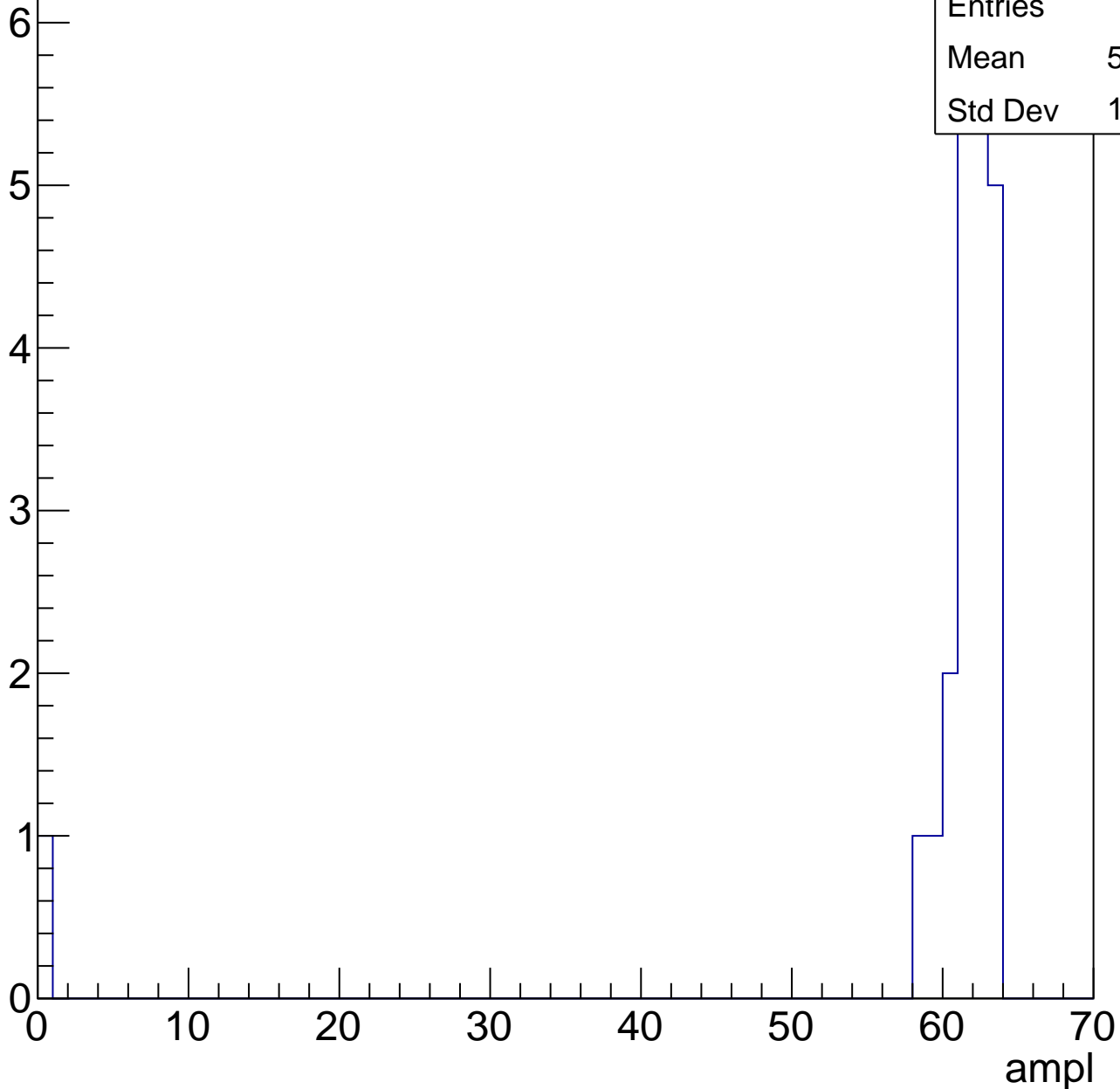
70

B1L103S, U7-ch102, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	22
Mean	58.64
Std Dev	12.86



B1L103S, U7-ch102, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry



B1L103S, U7-ch103, adc0

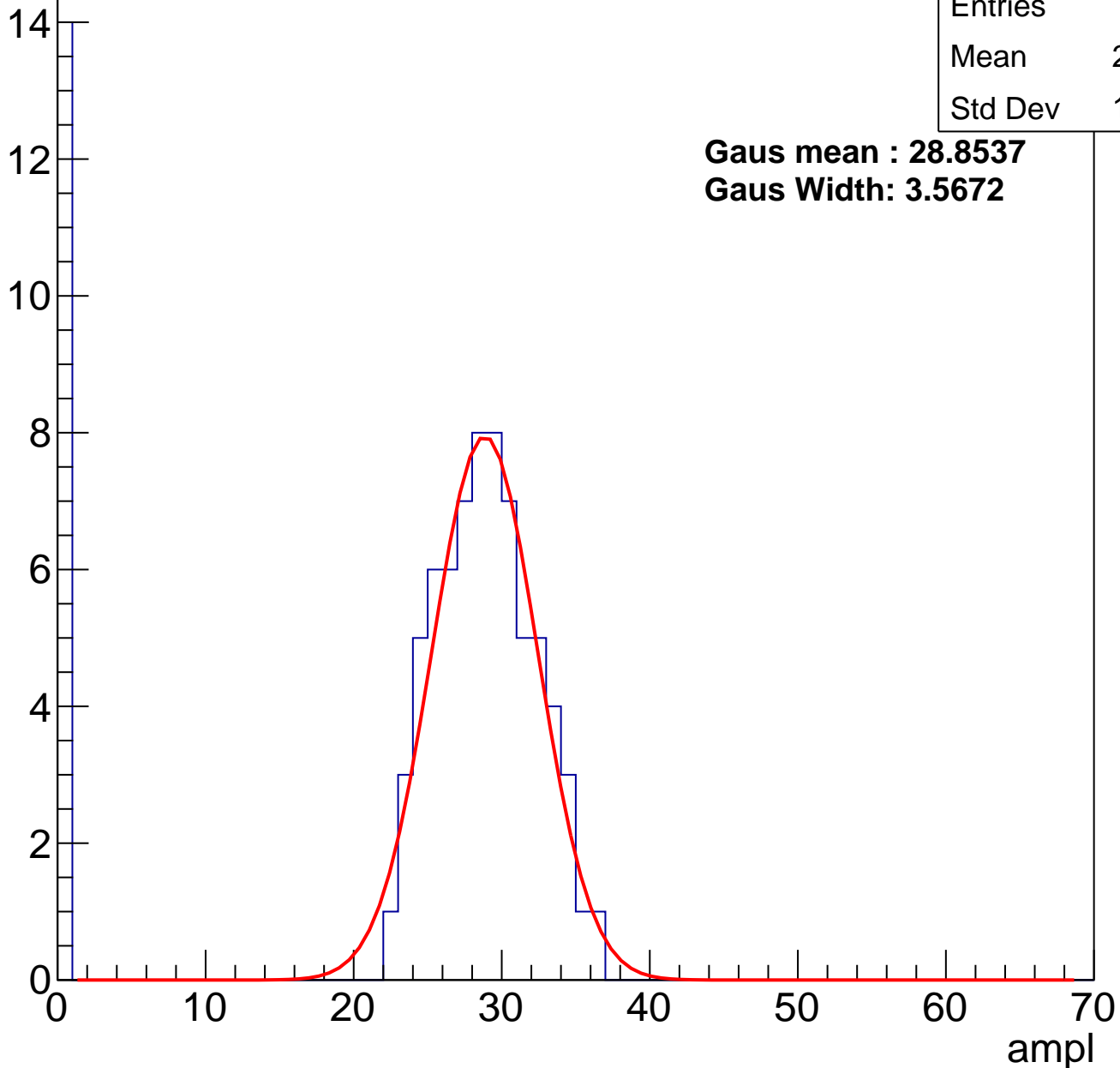
calib_packv5_041523_1651.root, FC#0, port C2

Entries	84
Mean	23.71
Std Dev	11.01

Gaus mean : 28.8537

Gaus Width: 3.5672

Entry



B1L103S, U7-ch103, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	92
Mean	30.64
Std Dev	12.79

Gaus mean : 36.2847

Gaus Width: 3.5113

Entry

12

10

8

6

4

2

0

0

10

20

30

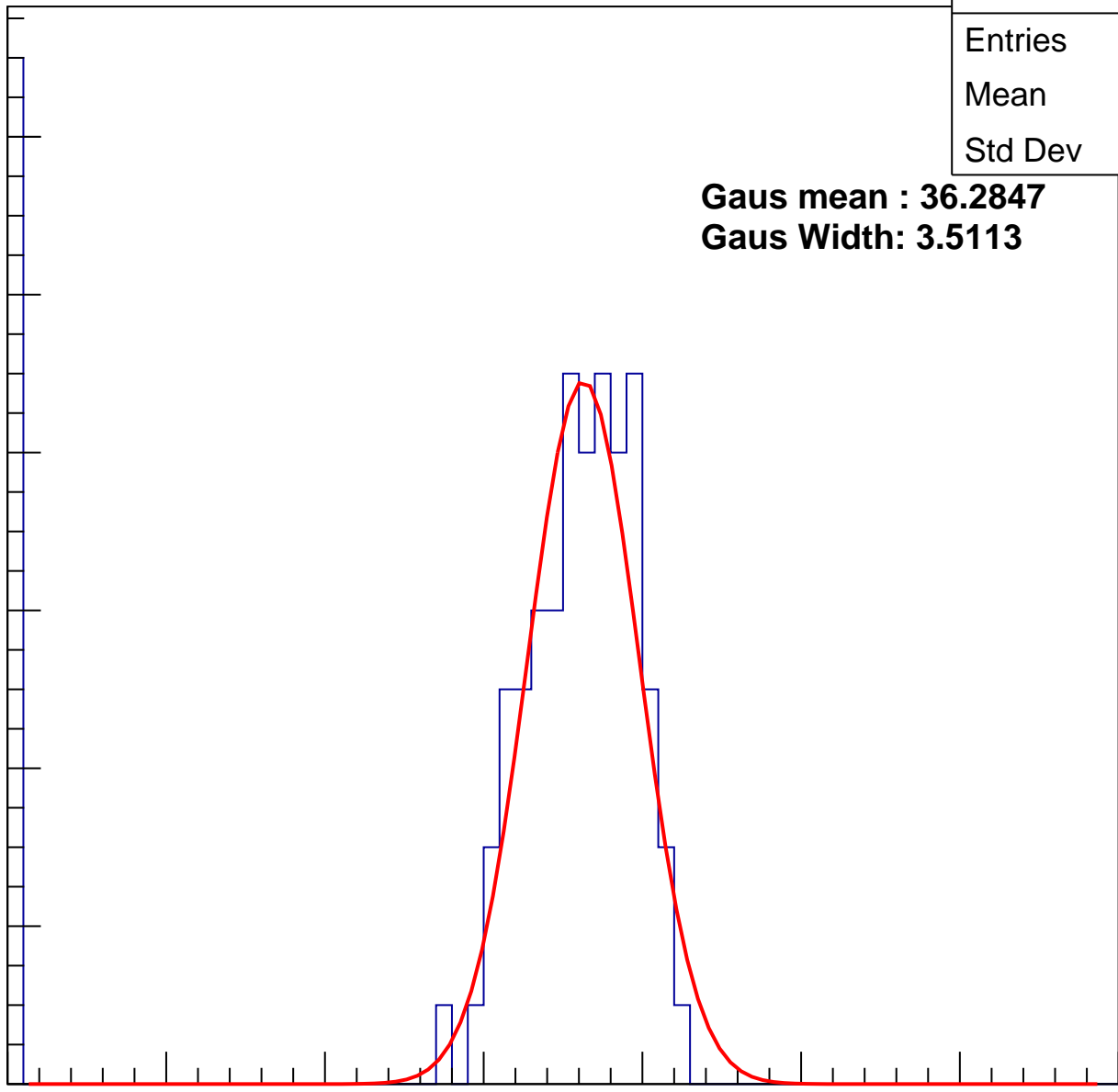
40

50

60

70

ampl



B1L103S, U7-ch103, adc2

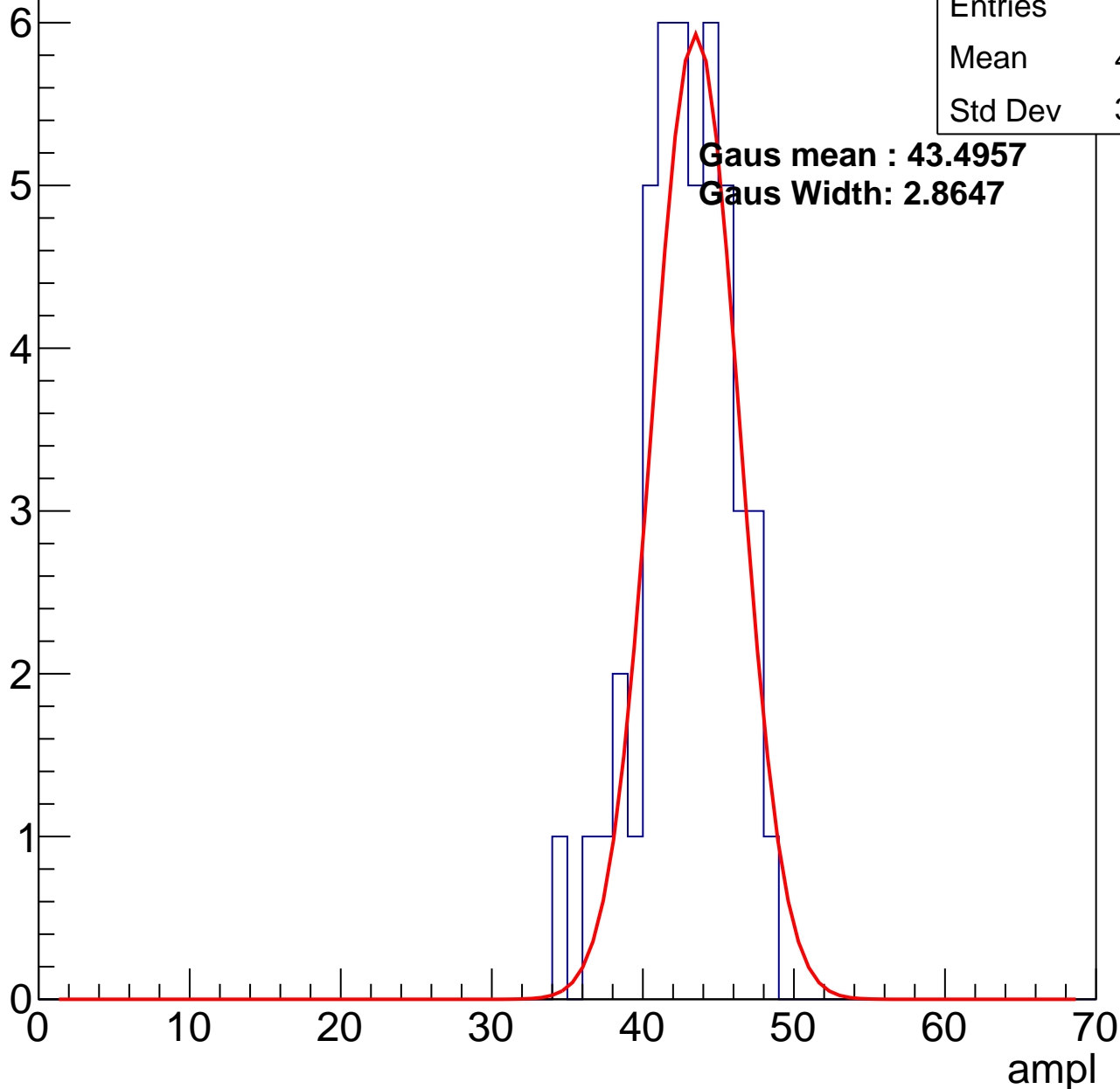
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	46
Mean	42.41
Std Dev	3.011

Gaus mean : 43.4957

Gaus Width: 2.8647

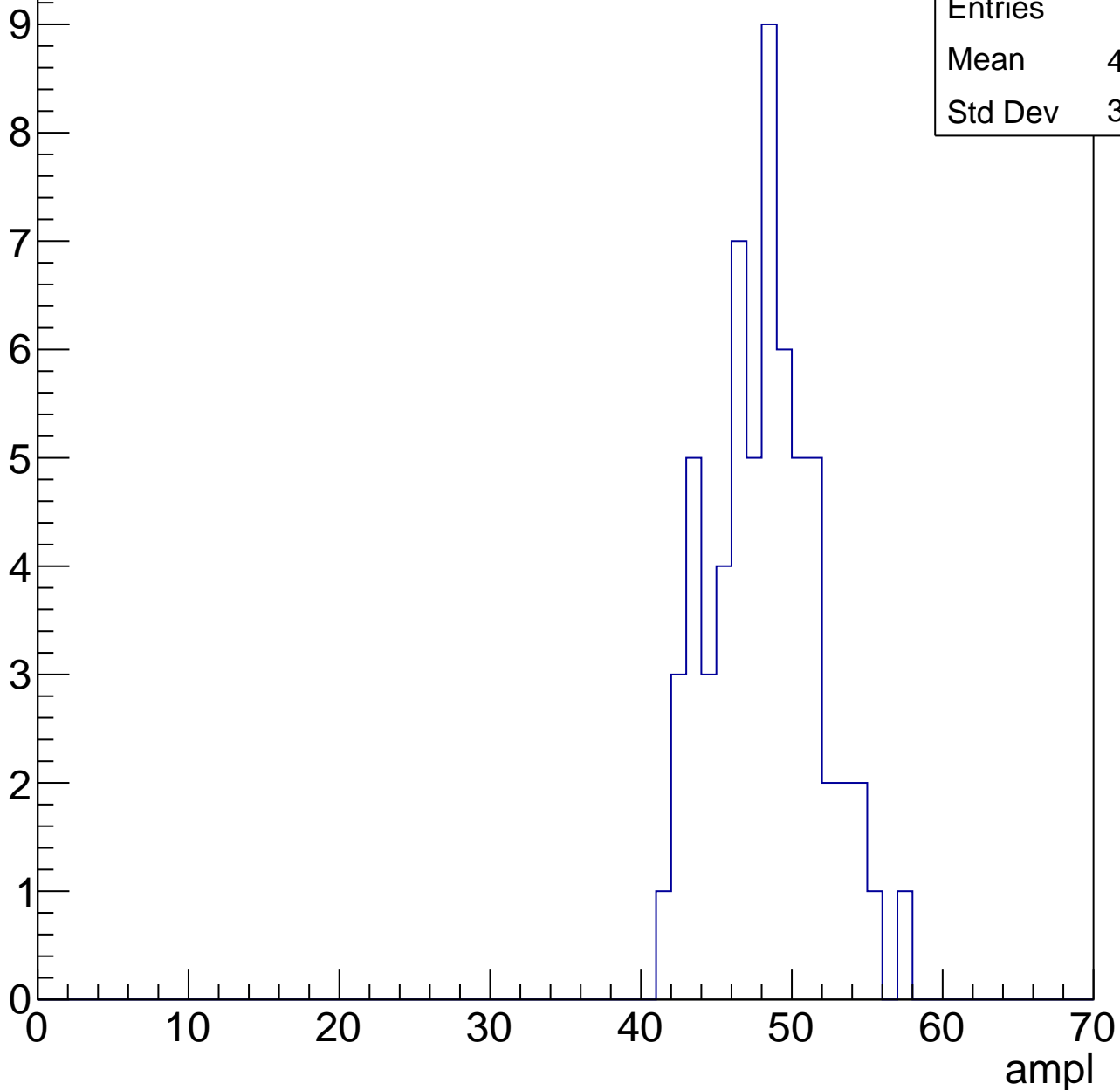


B1L103S, U7-ch103, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

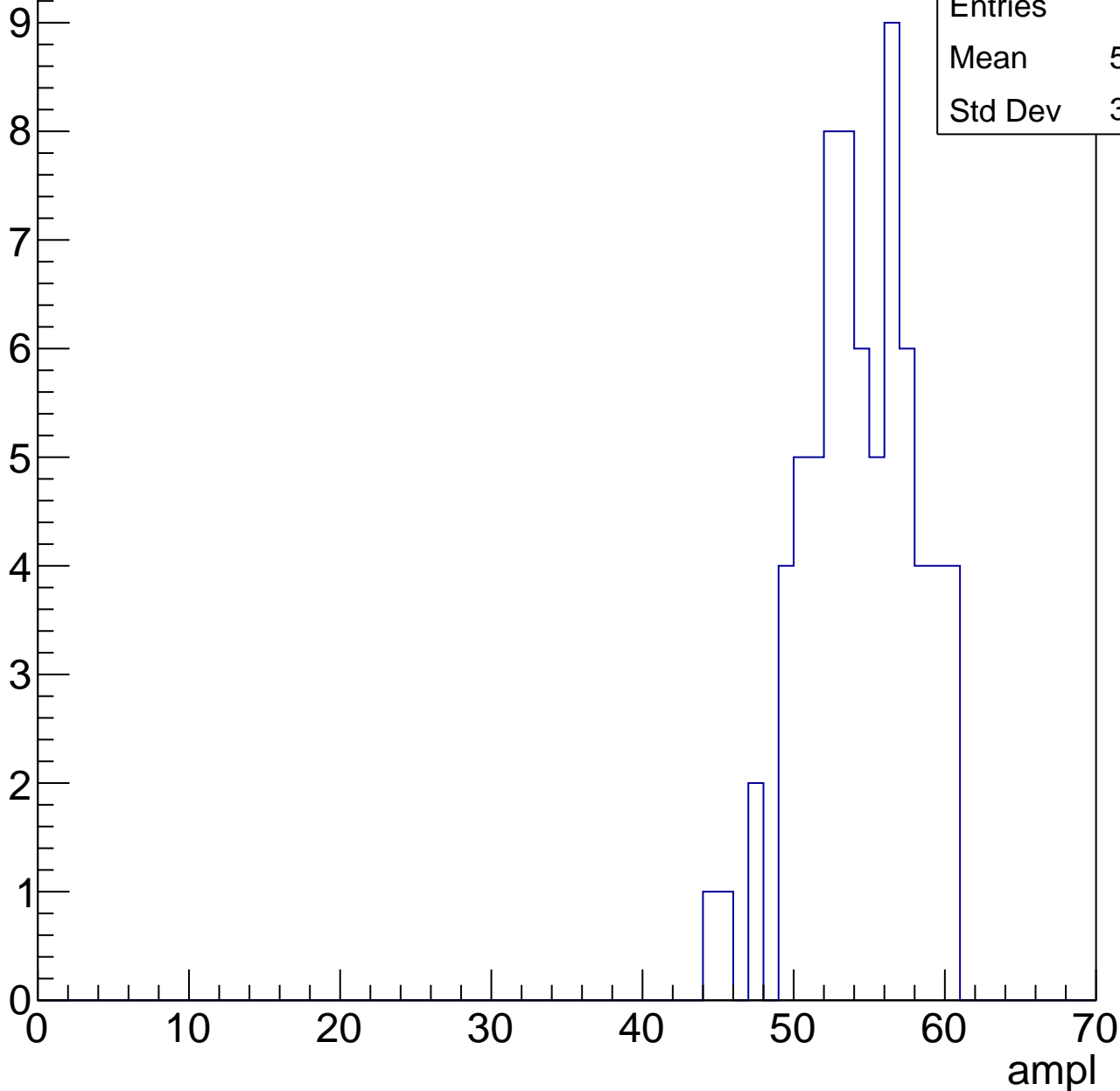
Entries	61
Mean	47.74
Std Dev	3.506



B1L103S, U7-ch103, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch103, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

7

6

5

4

3

2

1

0

Entries	48
Mean	57.04
Std Dev	12.17

ampl

0

10

20

30

40

50

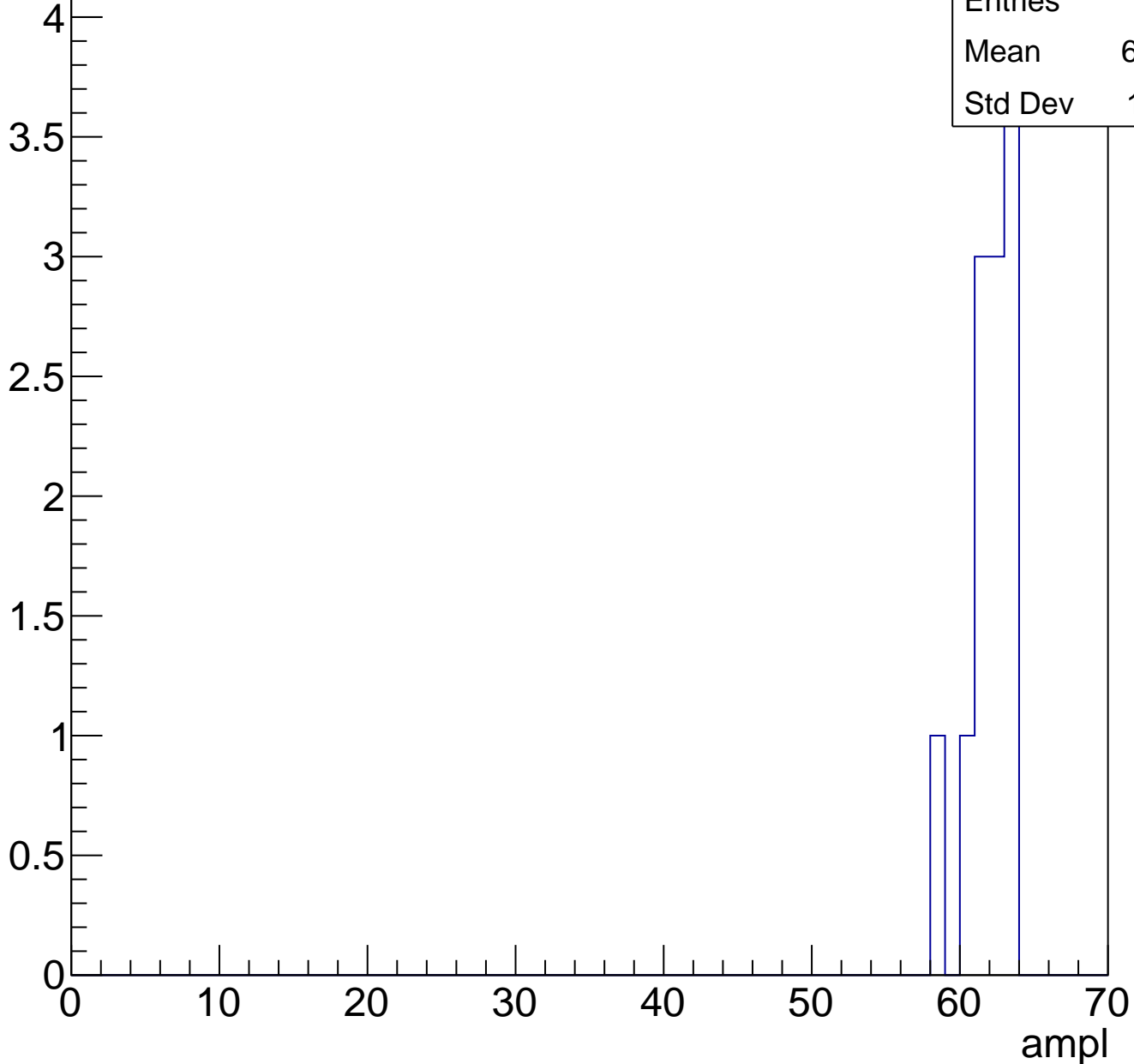
60

70

B1L103S, U7-ch103, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch103, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch104, adc0

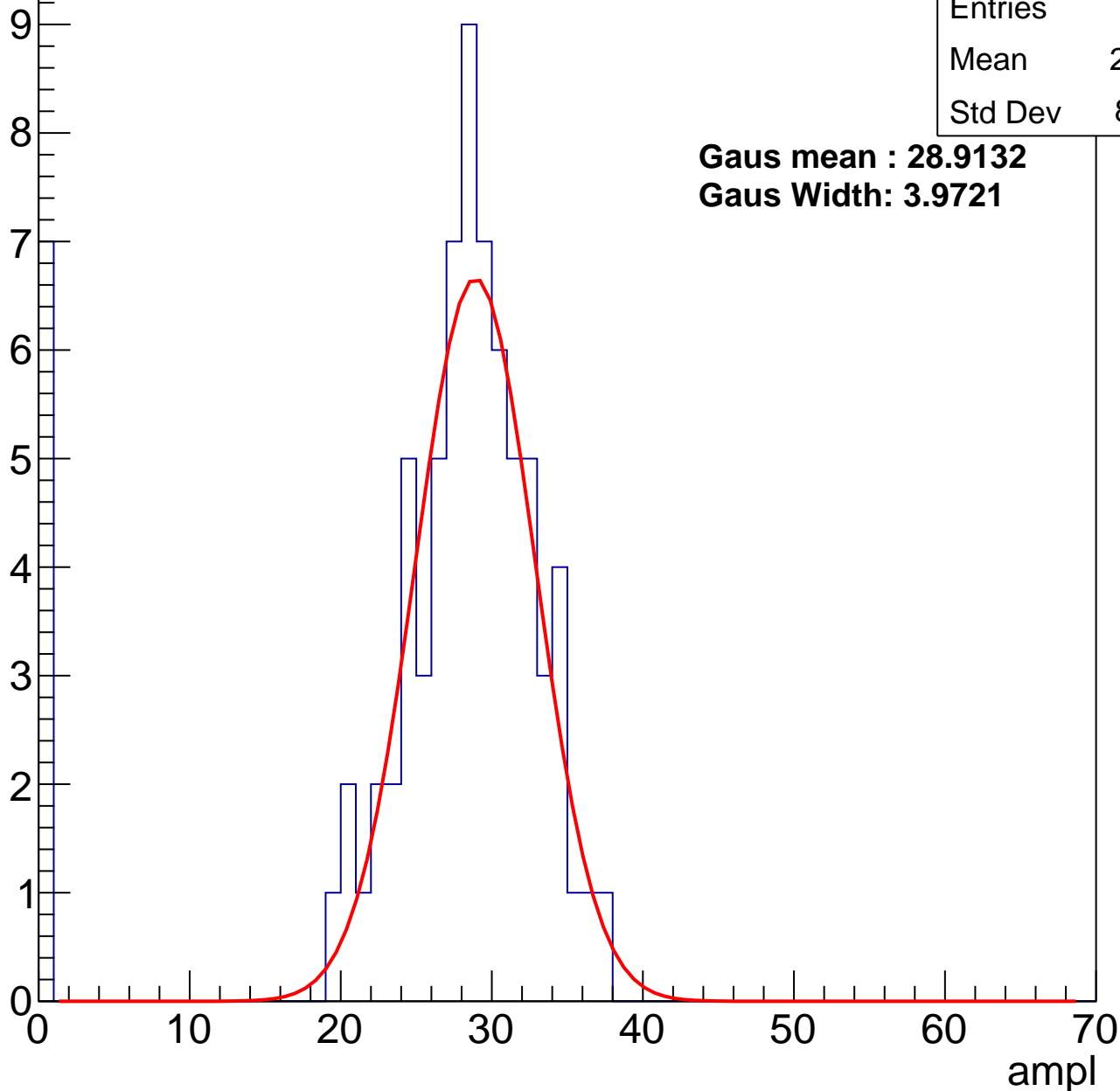
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	77
Mean	25.68
Std Dev	8.941

Gaus mean : 28.9132

Gaus Width: 3.9721



B1L103S, U7-ch104, adc1

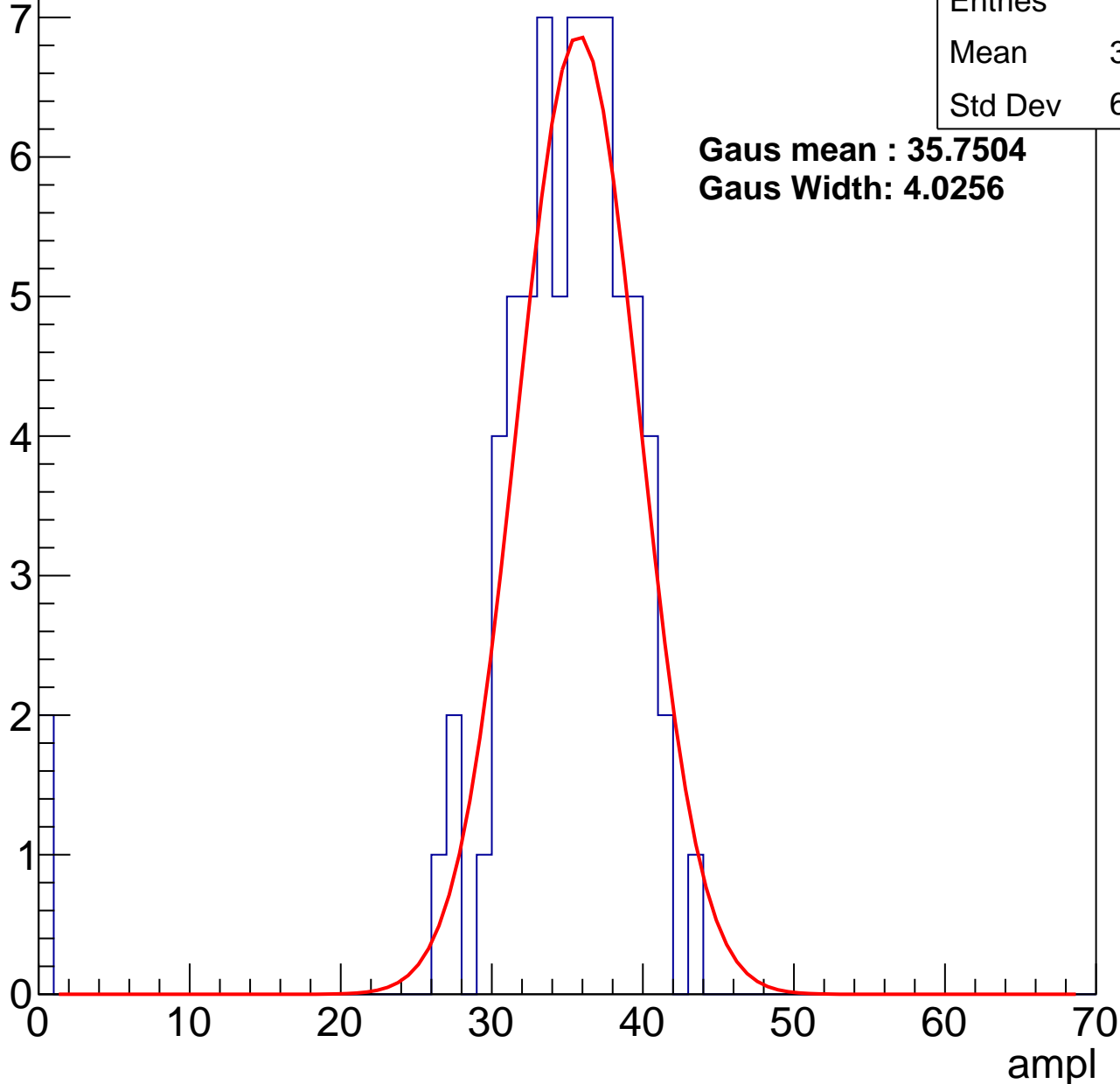
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	33.87
Std Dev	6.824

Gaus mean : 35.7504

Gaus Width: 4.0256



B1L103S, U7-ch104, adc2

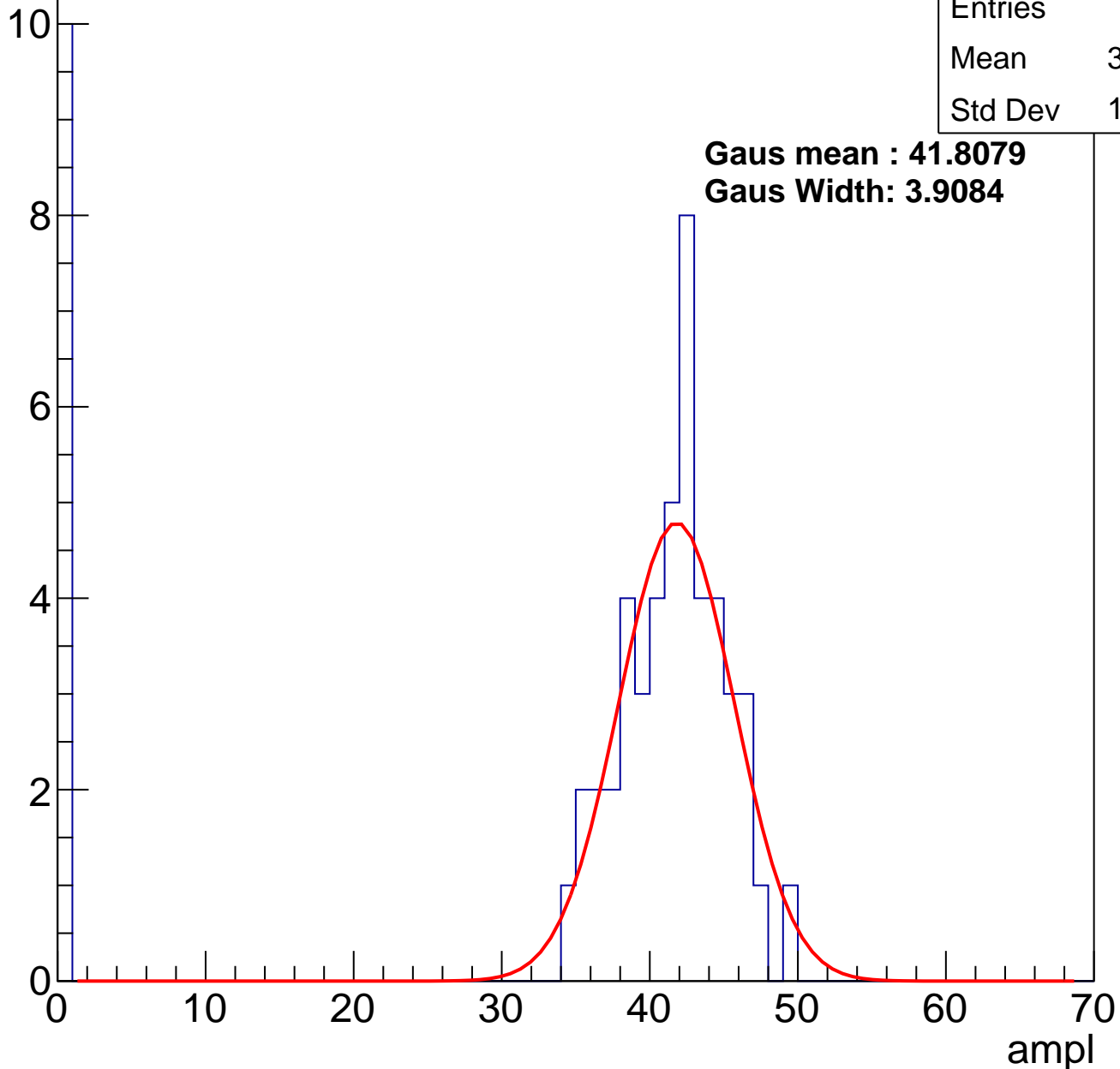
calib_packv5_041523_1651.root, FC#0, port C2

Entries	57
Mean	33.98
Std Dev	15.97

Gaus mean : 41.8079

Gaus Width: 3.9084

Entry

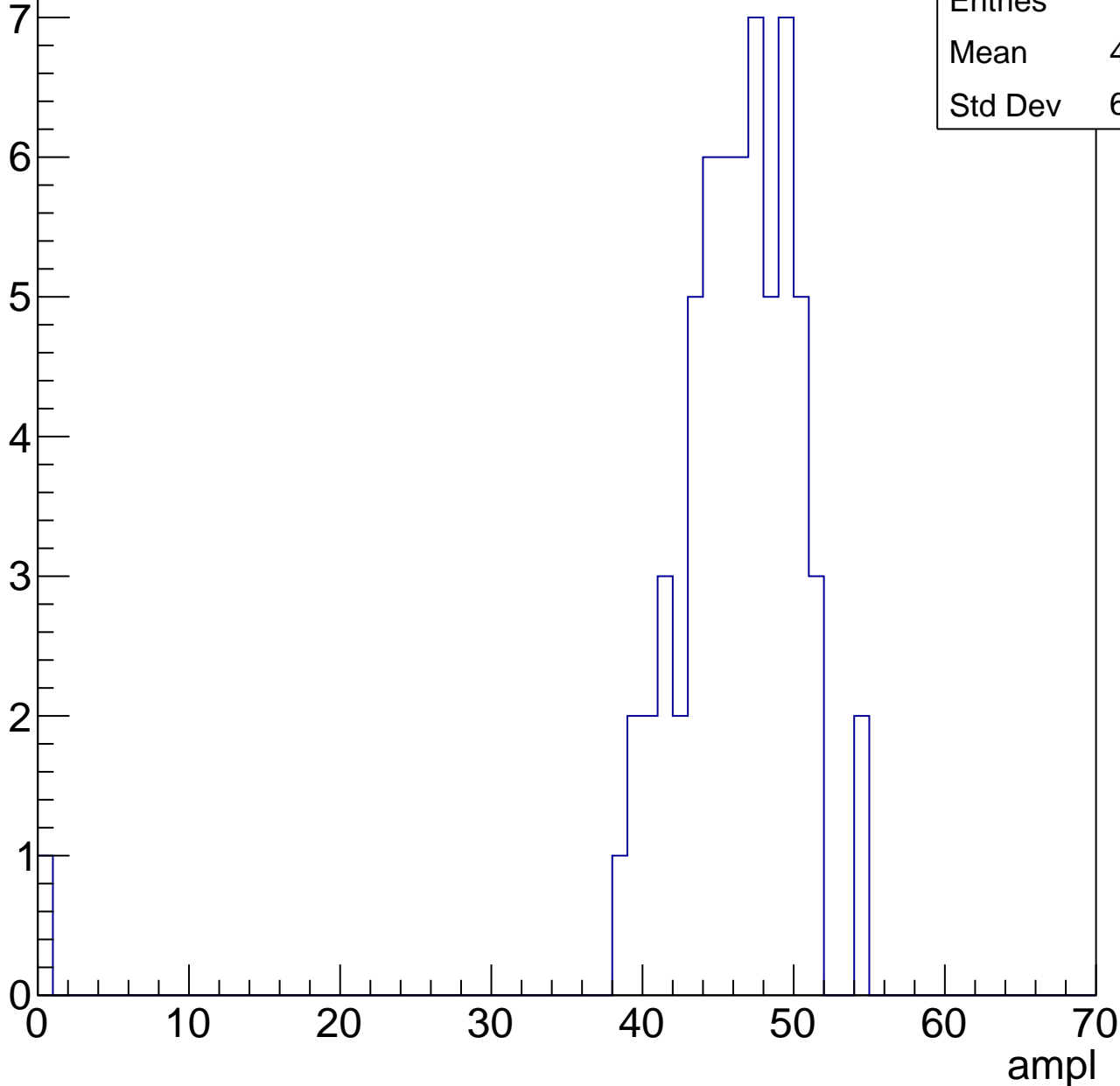


B1L103S, U7-ch104, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

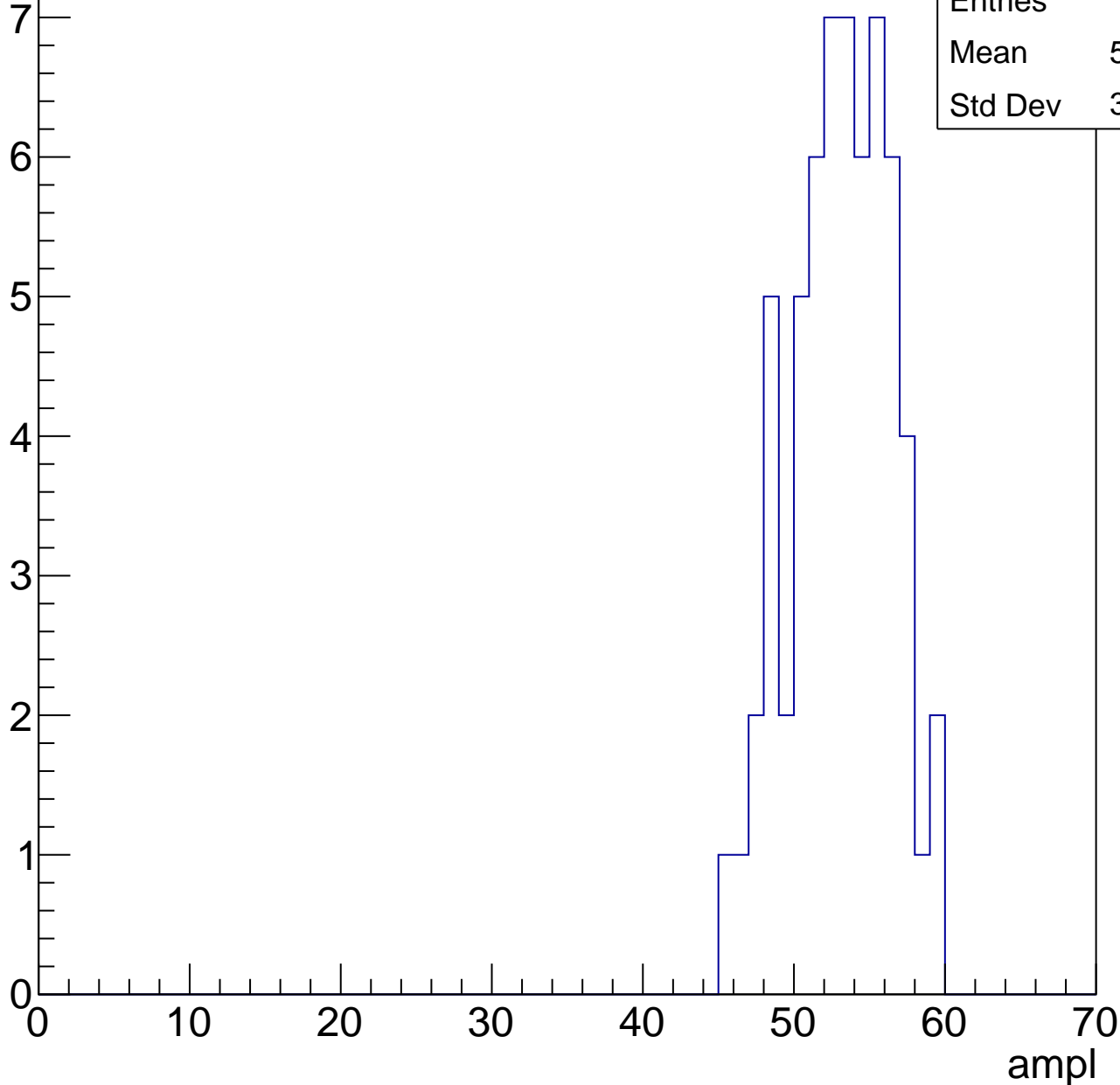
Entries	63
Mean	45.25
Std Dev	6.749



B1L103S, U7-ch104, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



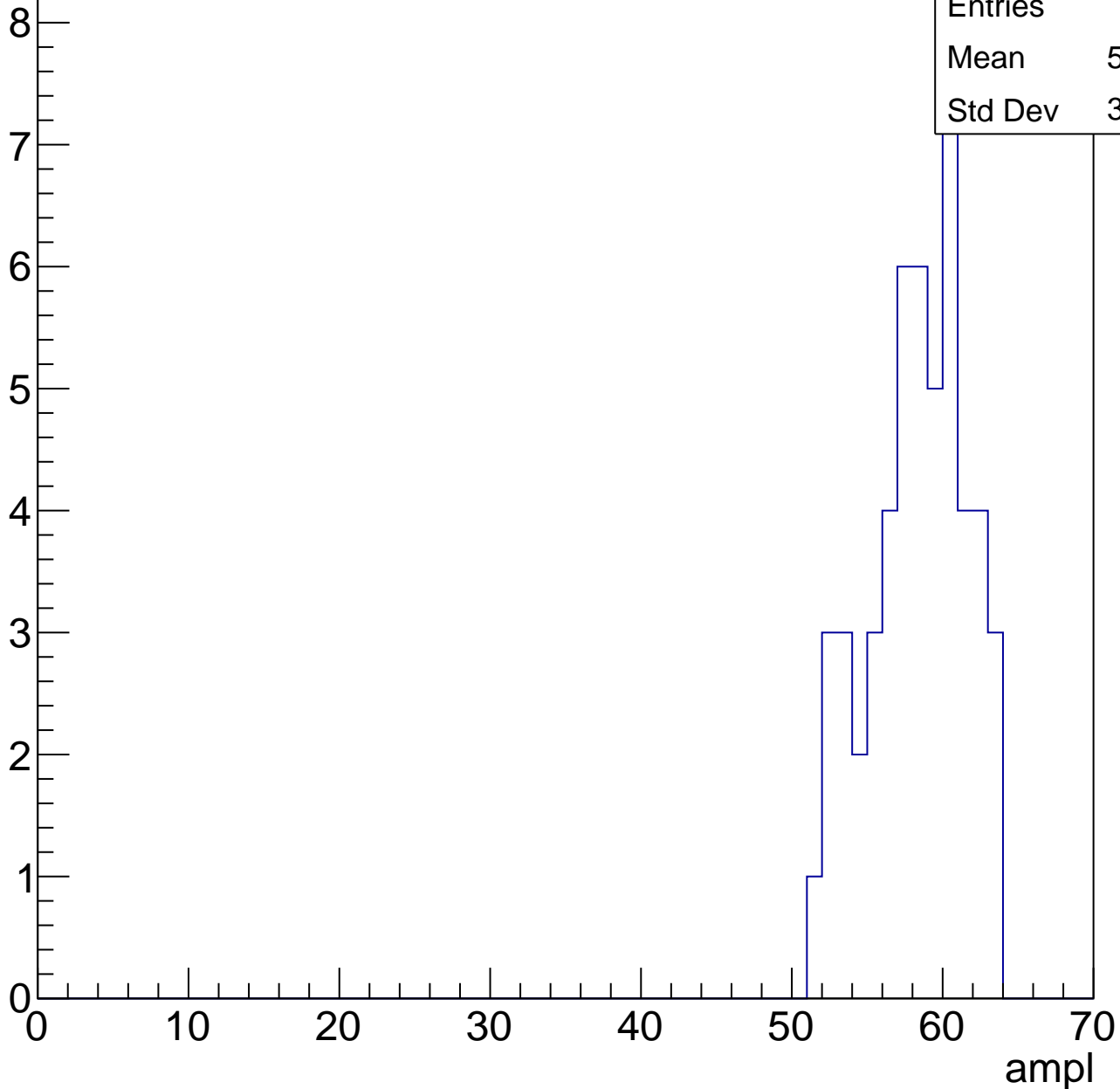
Entries	62
Mean	52.63
Std Dev	3.259

B1L103S, U7-ch104, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	57.87
Std Dev	3.175

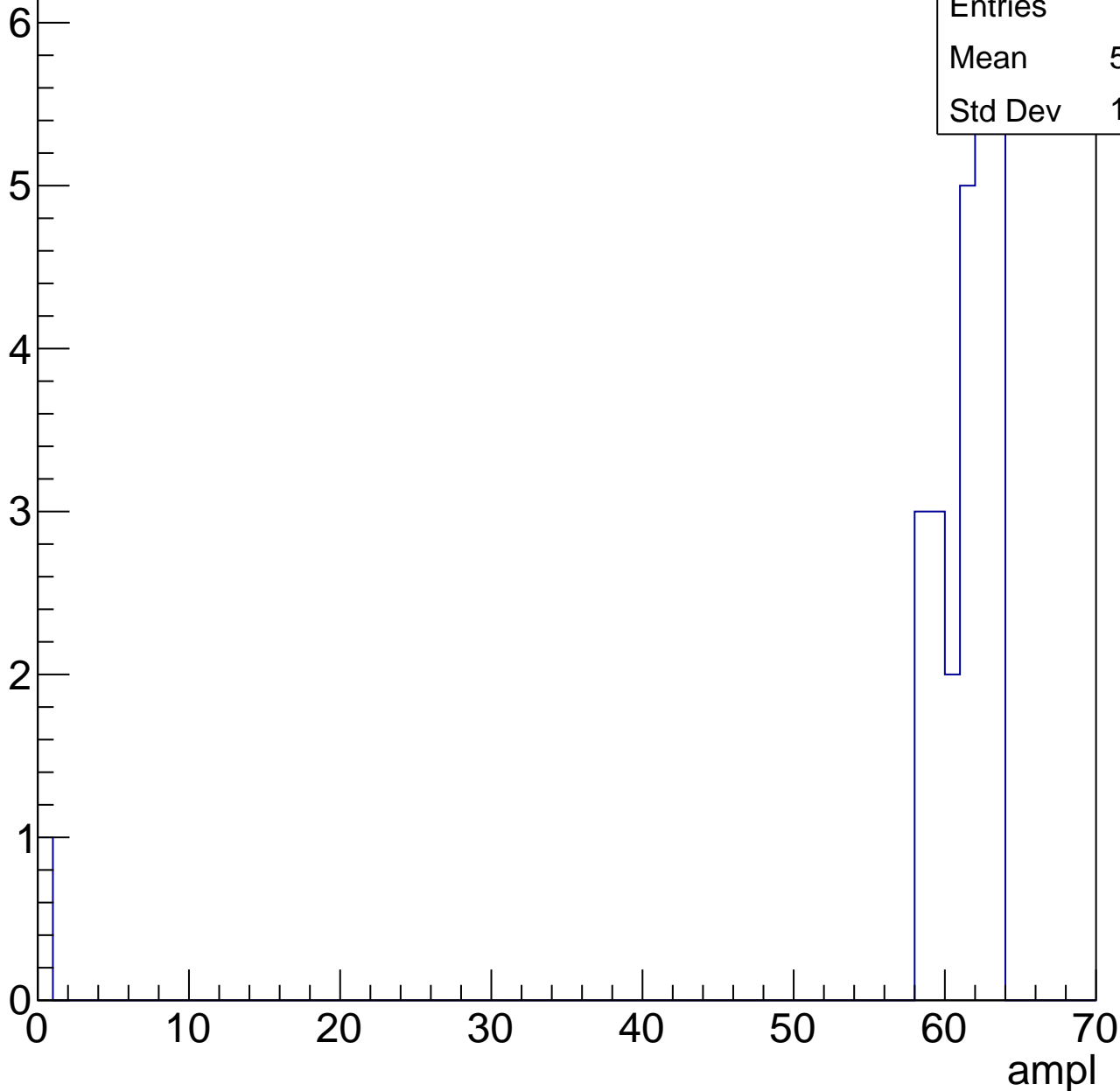


B1L103S, U7-ch104, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	26
Mean	58.69
Std Dev	11.85

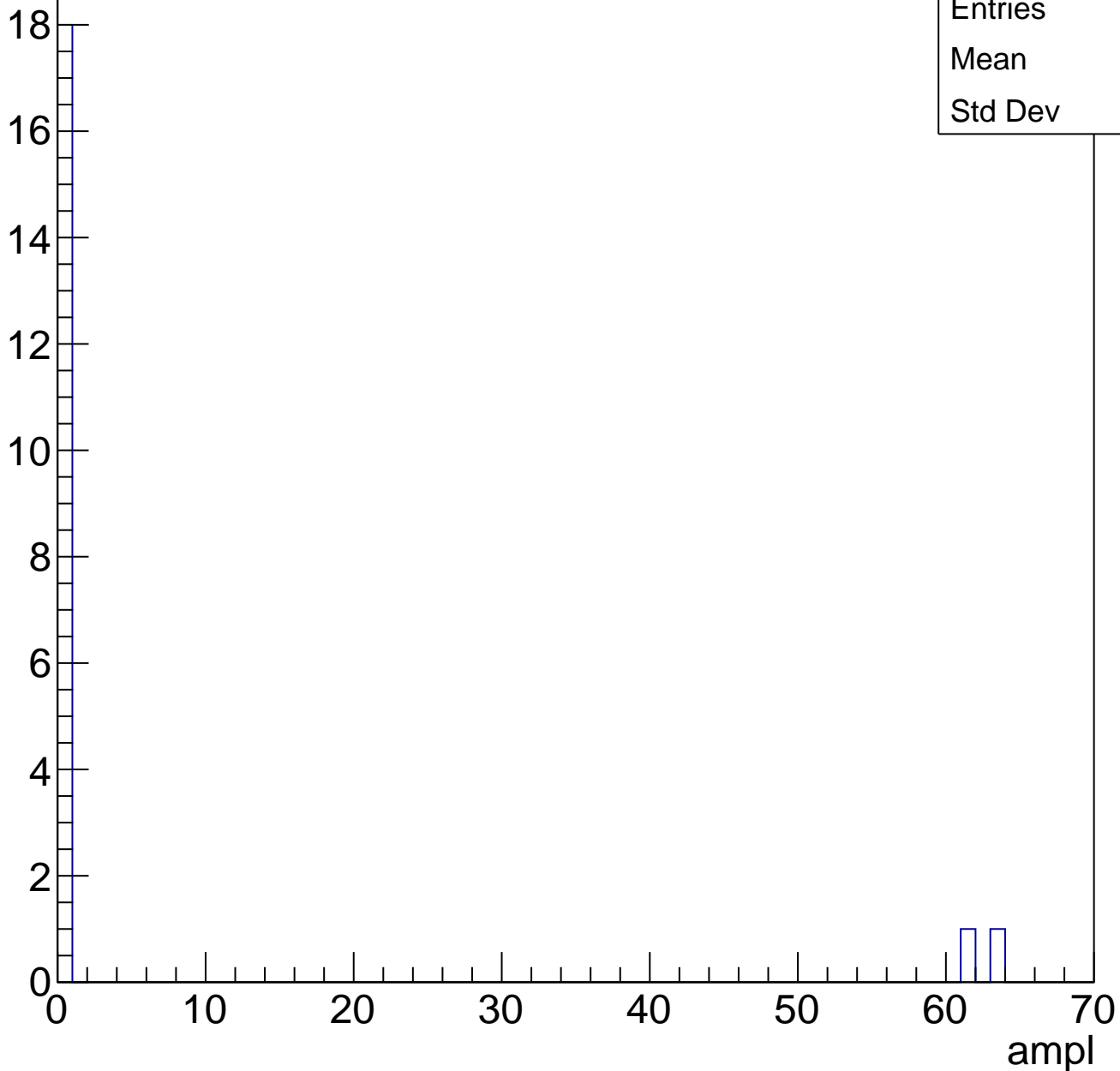


B1L103S, U7-ch104, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	6.2
Std Dev	18.6

Entry



B1L103S, U7-ch105, adc0

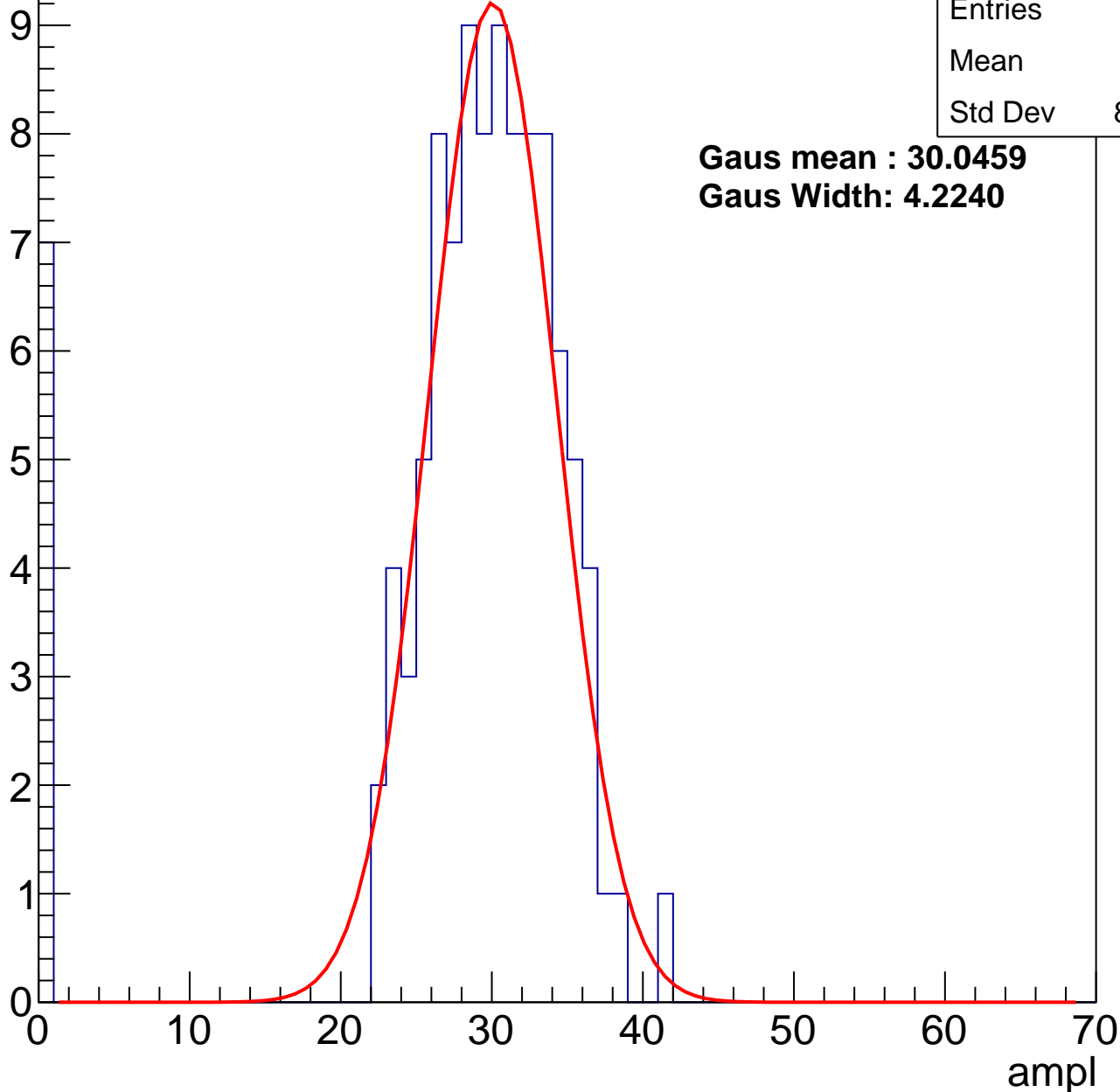
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	104
Mean	27.8
Std Dev	8.377

Gaus mean : 30.0459

Gaus Width: 4.2240



B1L103S, U7-ch105, adc1

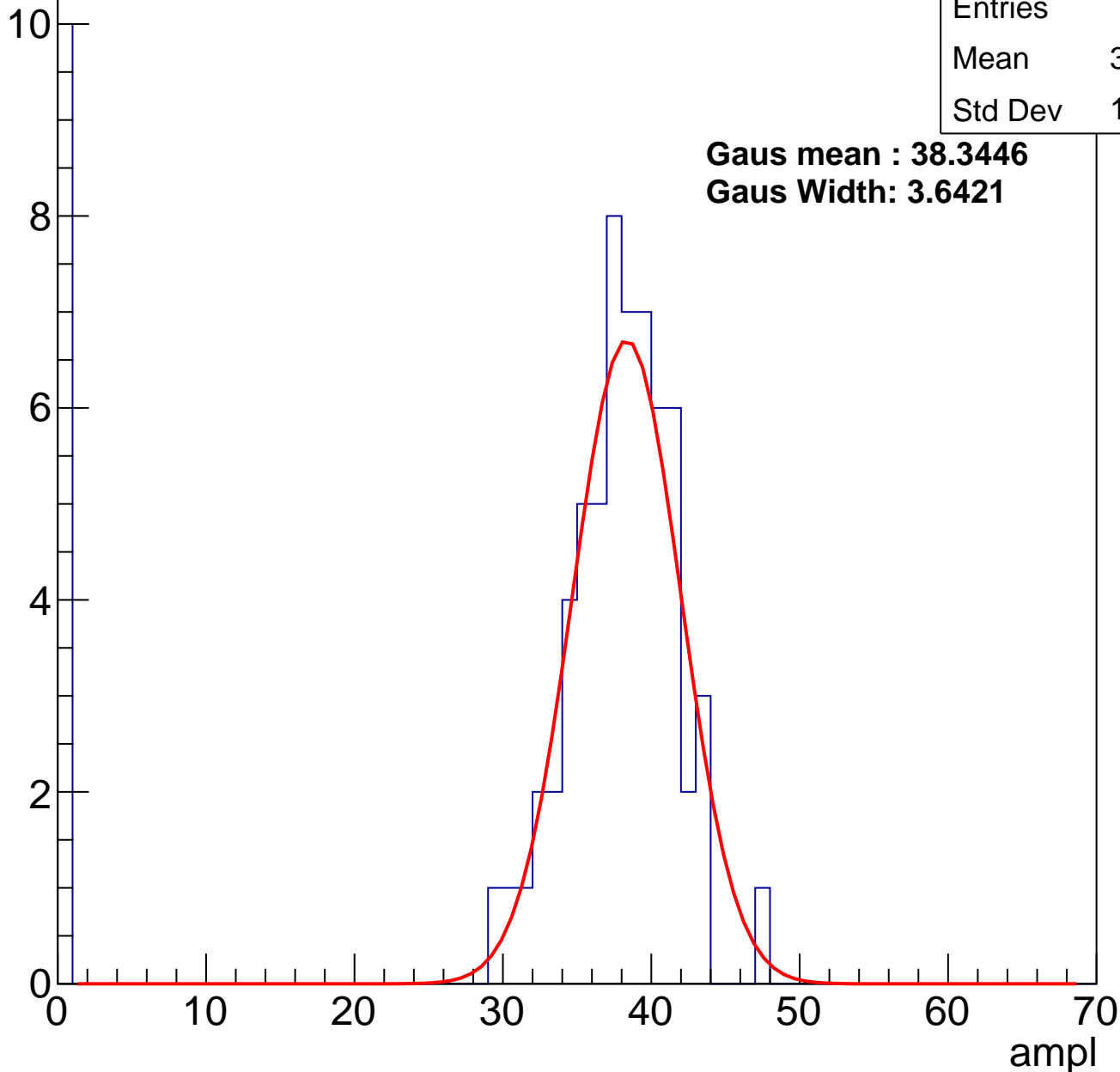
calib_packv5_041523_1651.root, FC#0, port C2

Entries	71
Mean	32.28
Std Dev	13.45

Gaus mean : 38.3446

Gaus Width: 3.6421

Entry



B1L103S, U7-ch105, adc2

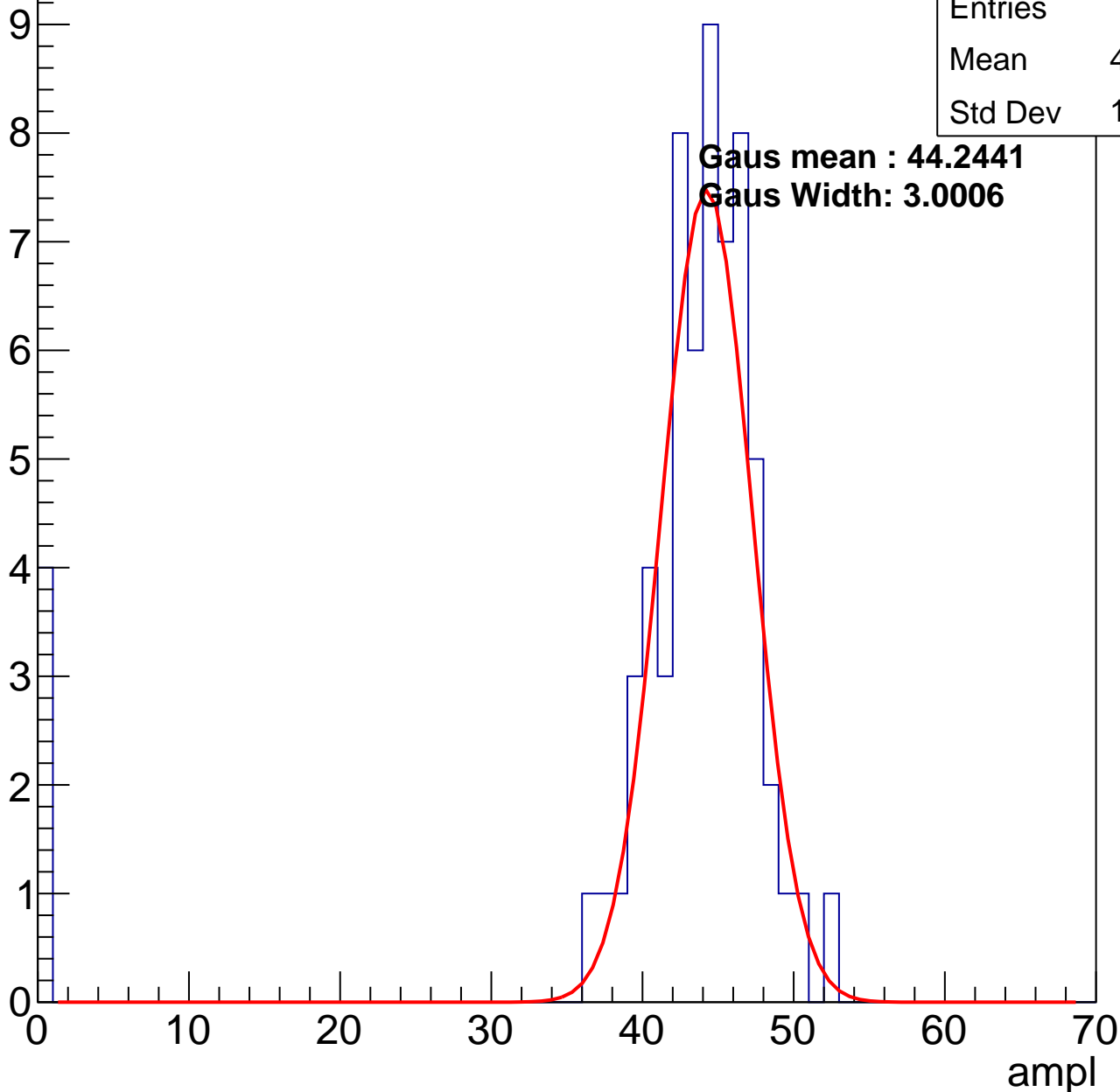
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	41.02
Std Dev	10.93

Gaus mean : 44.2441

Gaus Width: 3.0006

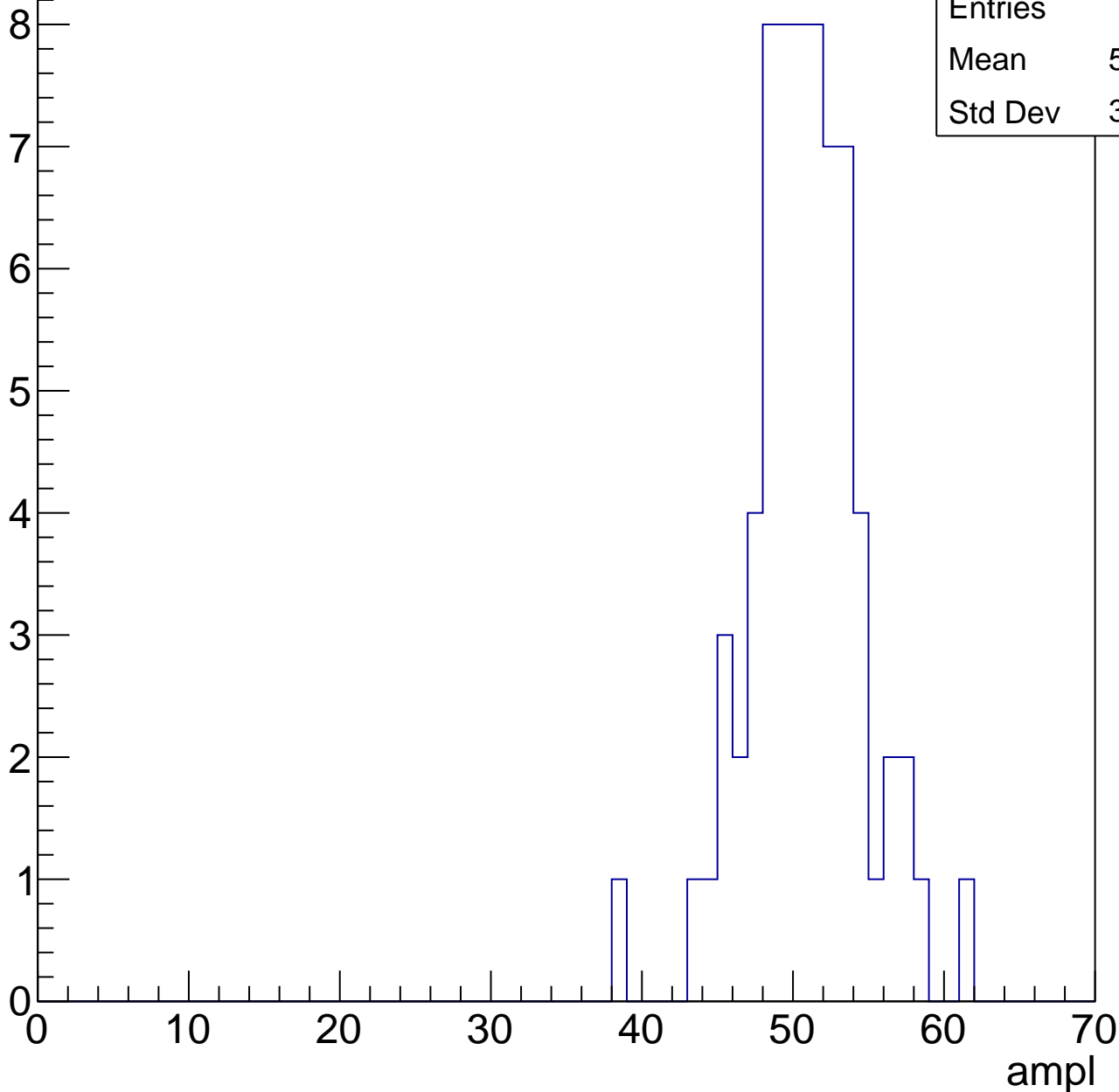


B1L103S, U7-ch105, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	50.36
Std Dev	3.703

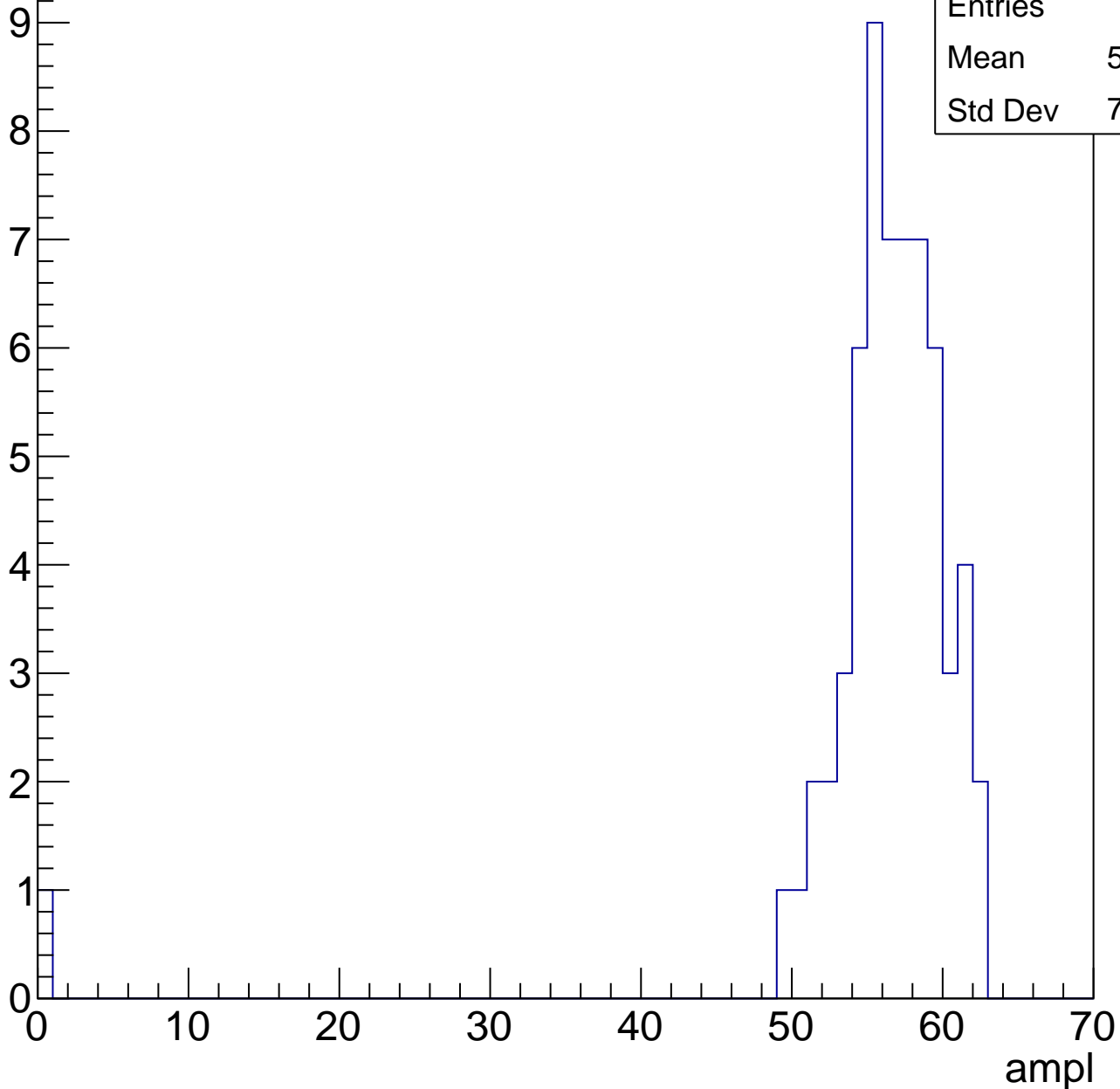


B1L103S, U7-ch105, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	55.44
Std Dev	7.739

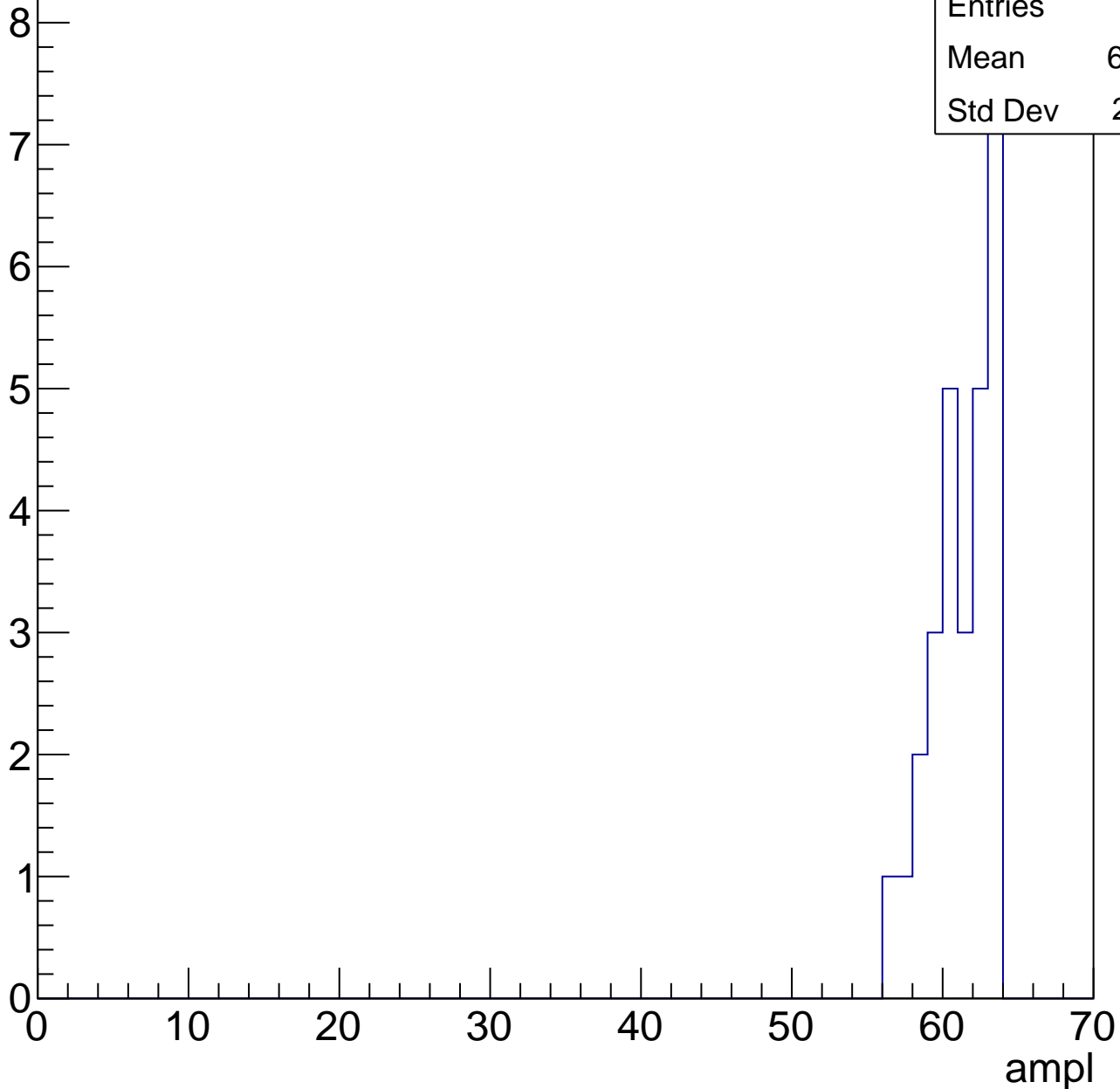


B1L103S, U7-ch105, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

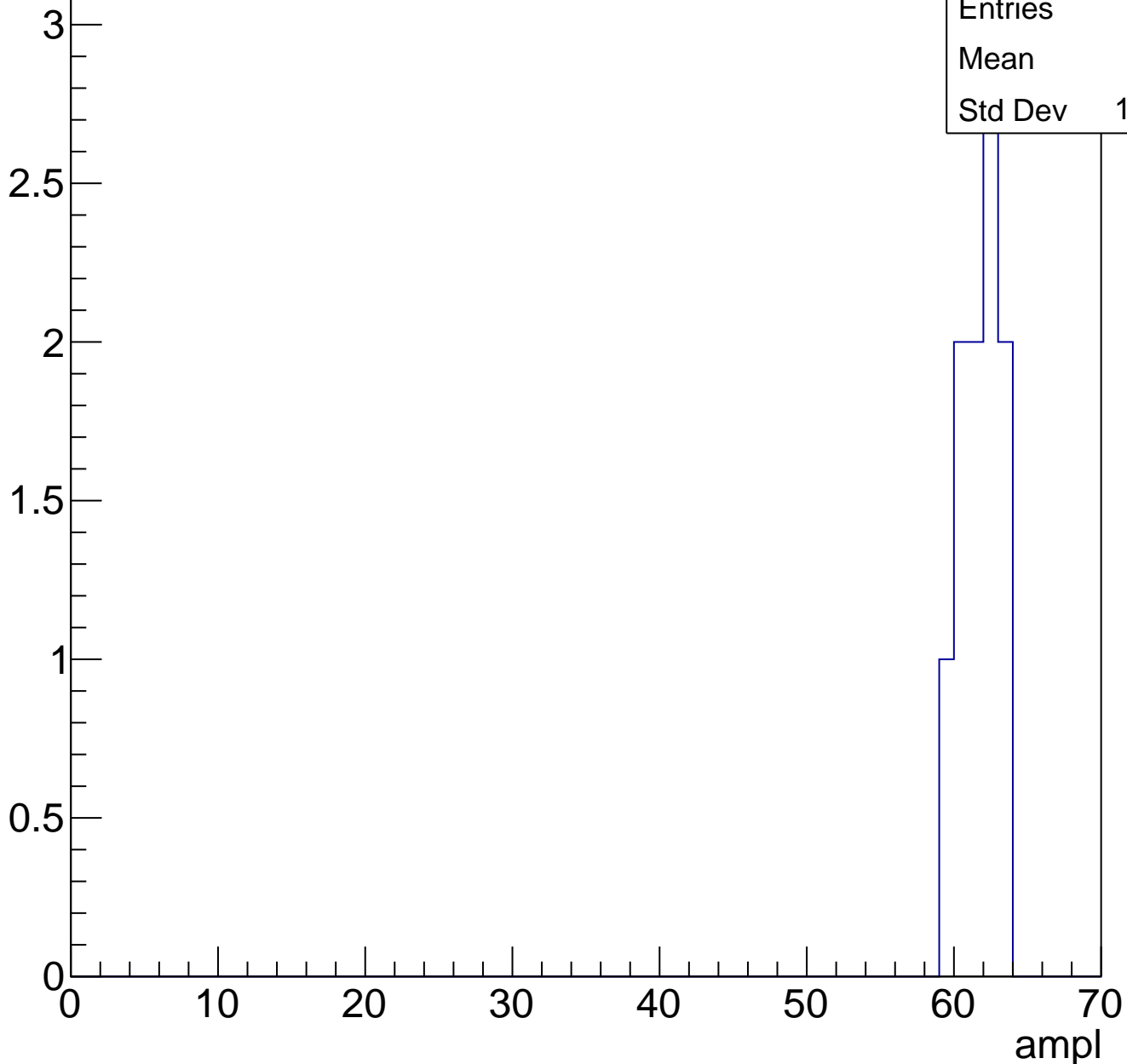
Entries	28
Mean	60.82
Std Dev	2.001



B1L103S, U7-ch105, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

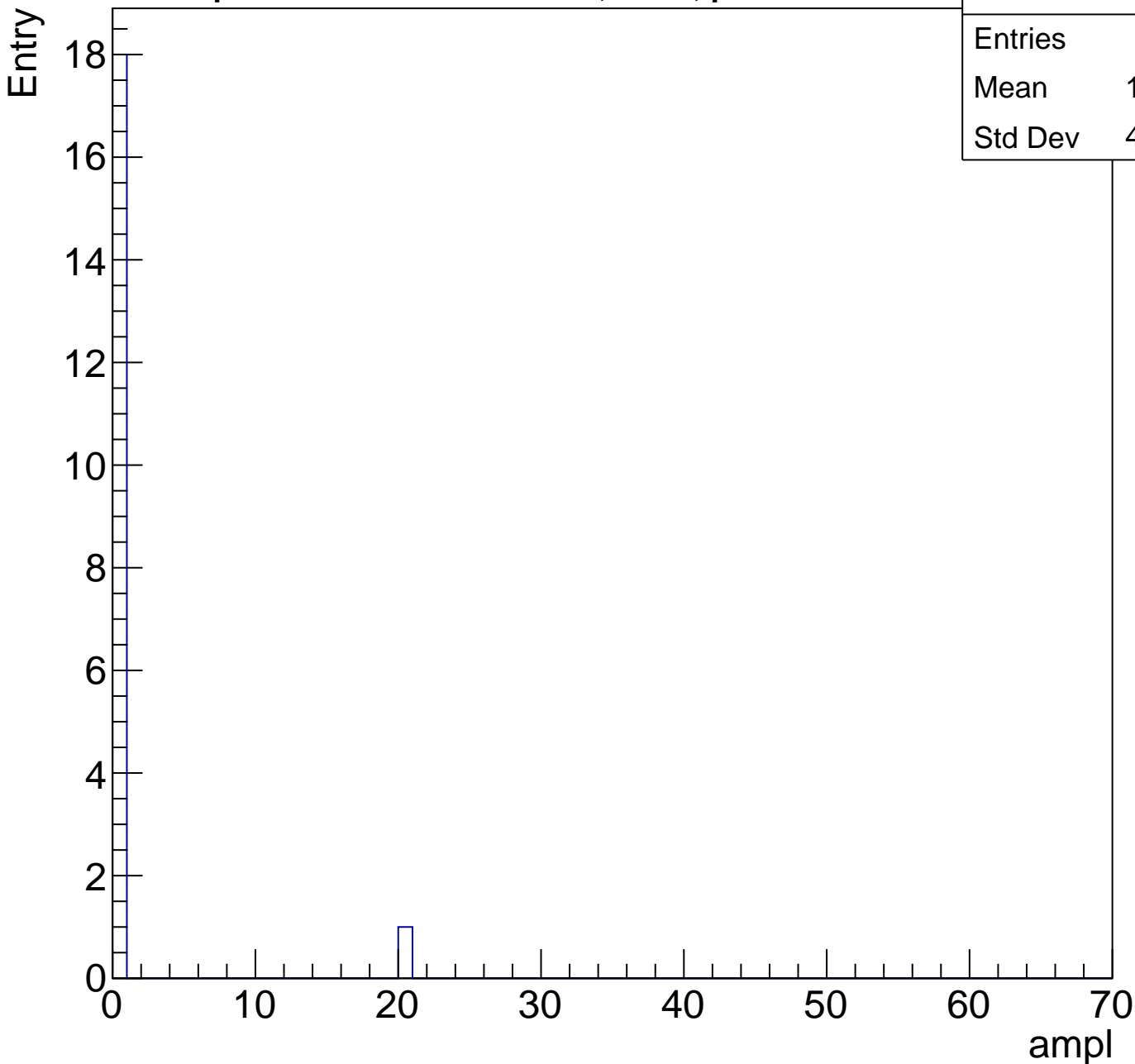


Entries	10
Mean	61.3
Std Dev	1.269

B1L103S, U7-ch105, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.053
Std Dev	4.466



B1L103S, U7-ch106, adc0

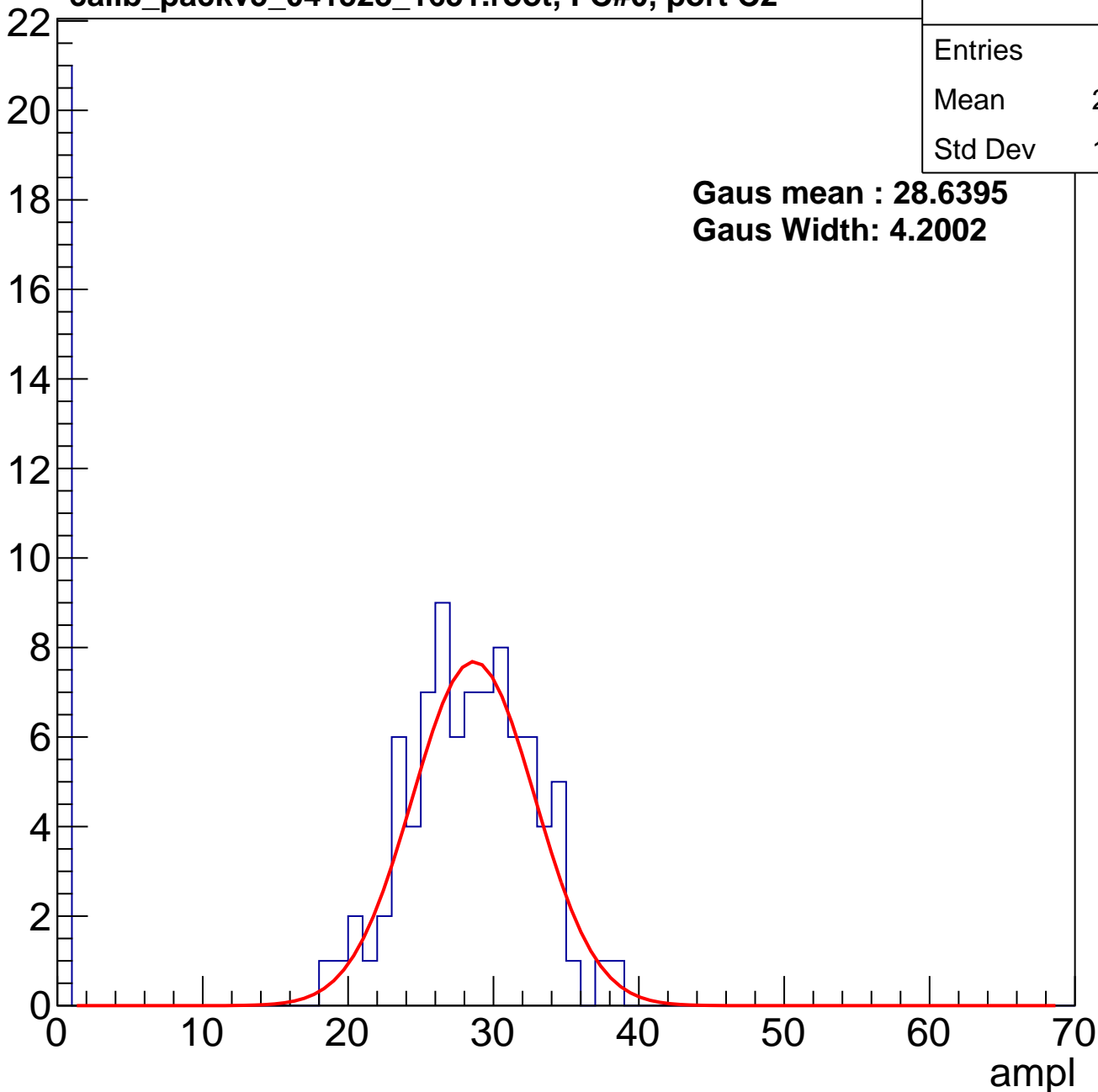
calib_packv5_041523_1651.root, FC#0, port C2

Entries	106
Mean	22.42
Std Dev	11.74

Gaus mean : 28.6395

Gaus Width: 4.2002

Entry



B1L103S, U7-ch106, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	78
Mean	30.37
Std Dev	12.97

Gaus mean : 37.6245

Gaus Width: 7.6677

Entry

10

8

6

4

2

0

0

10

20

30

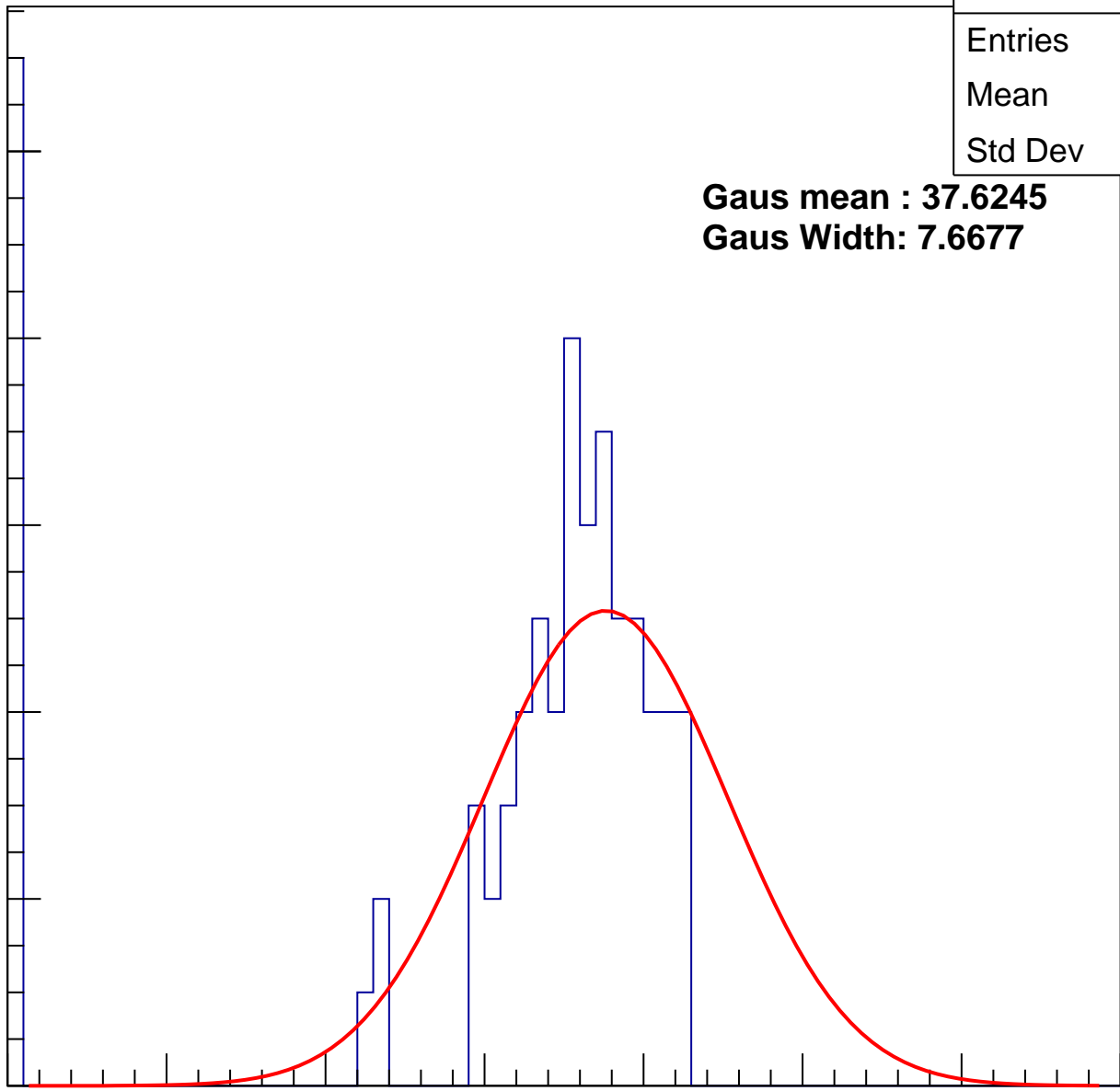
40

50

60

70

ampl



B1L103S, U7-ch106, adc2

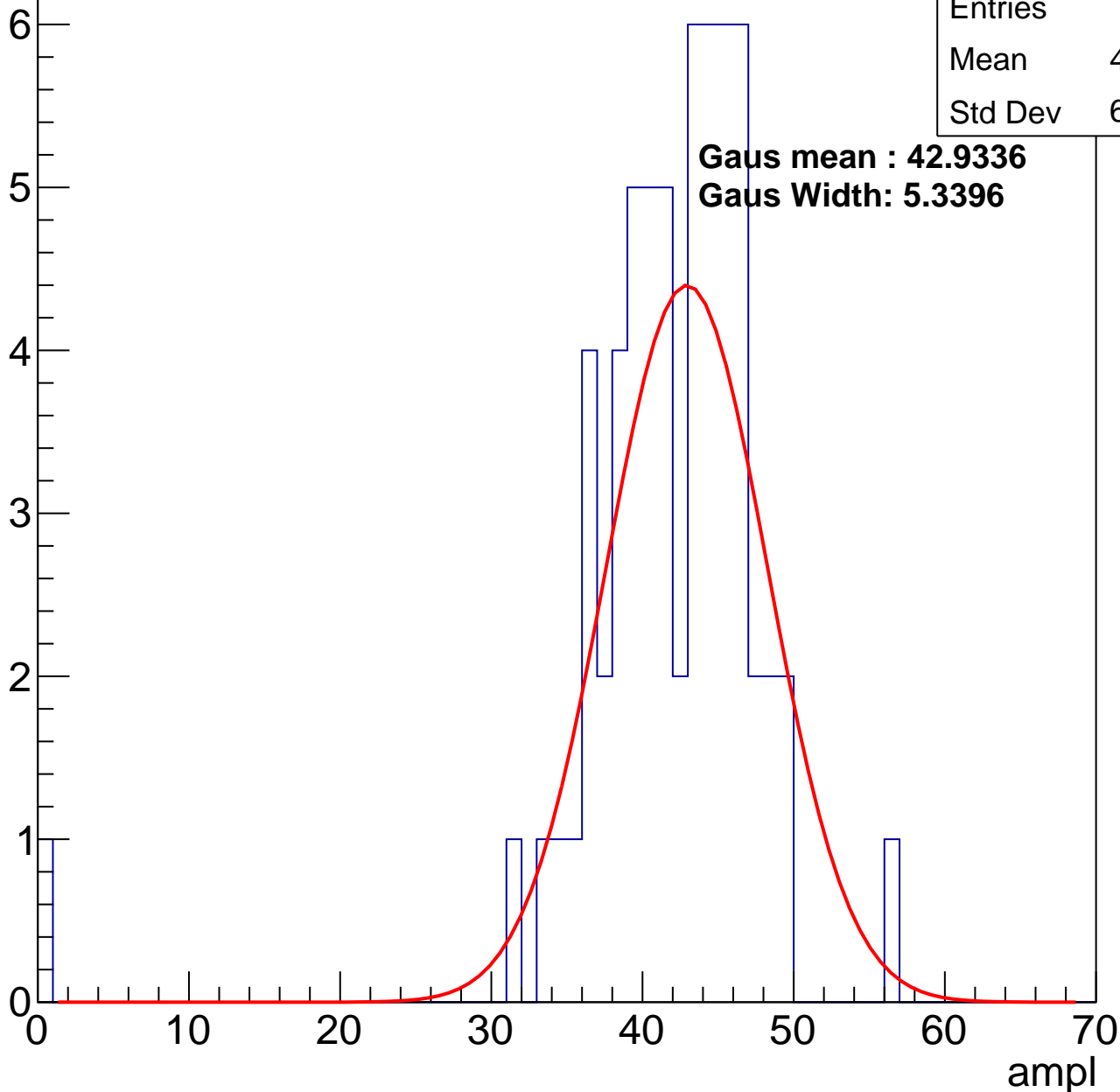
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	41.25
Std Dev	6.864

Gaus mean : 42.9336

Gaus Width: 5.3396

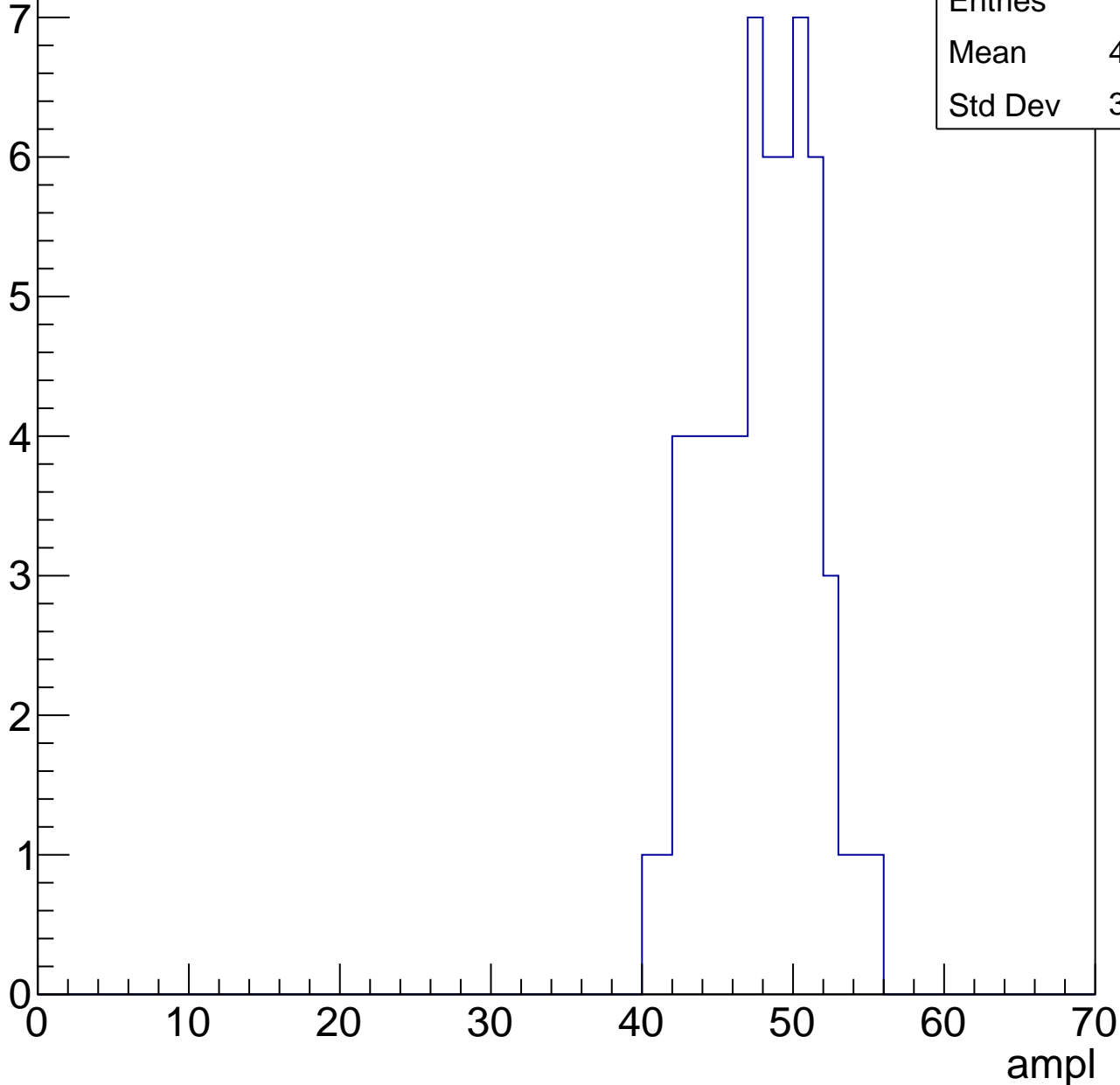


B1L103S, U7-ch106, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	47.43
Std Dev	3.432

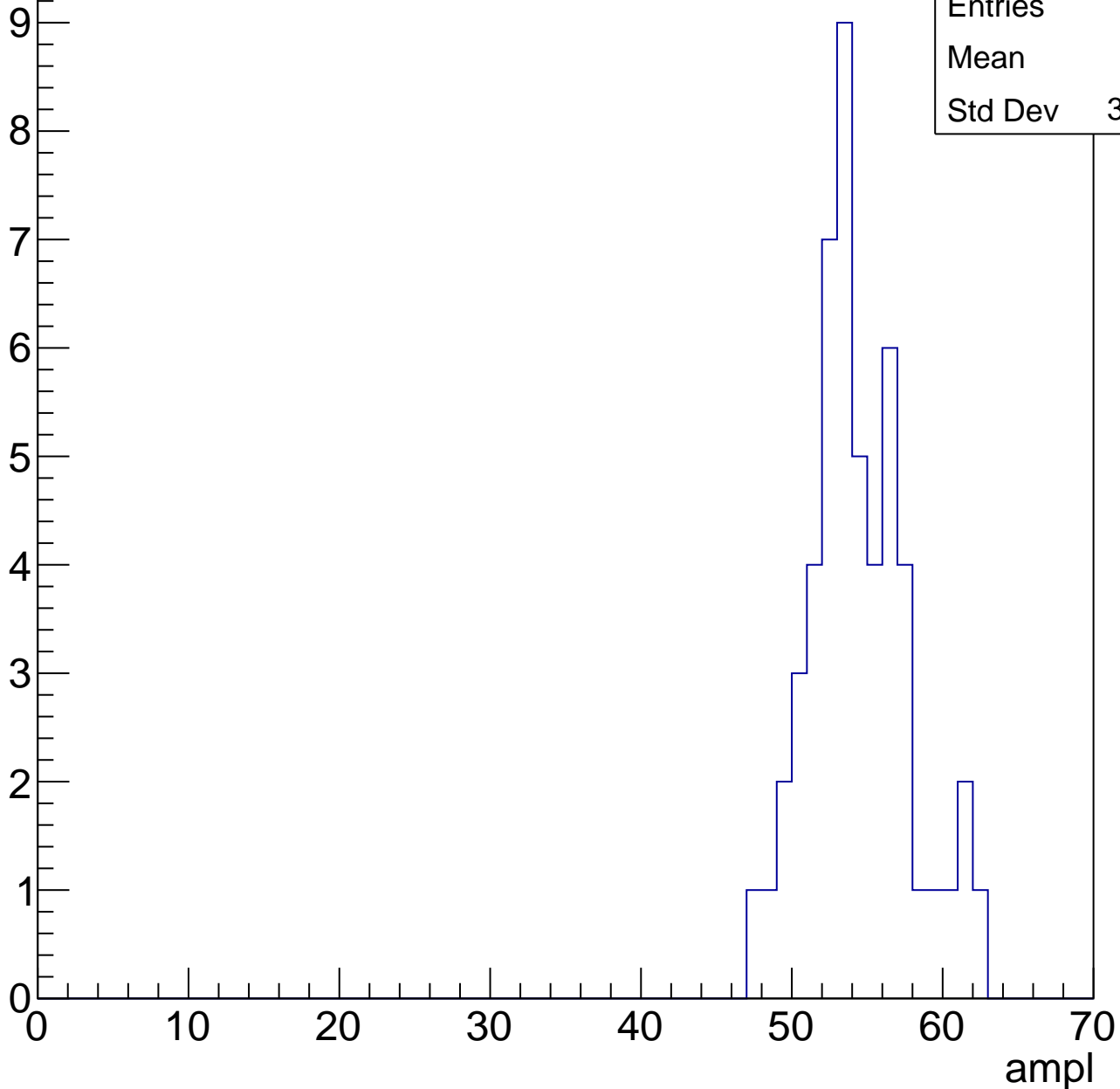


B1L103S, U7-ch106, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

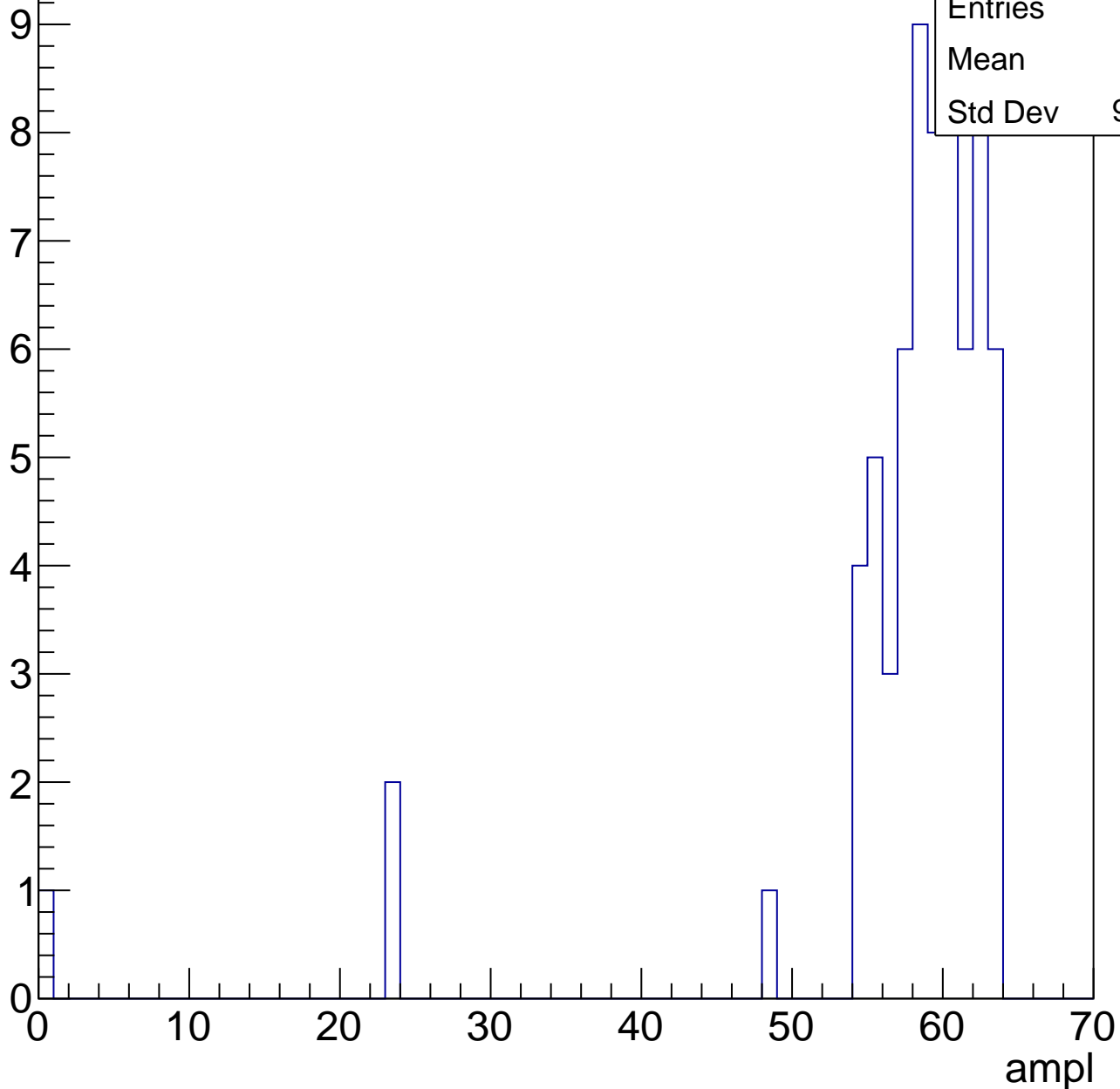
Entries	52
Mean	53.9
Std Dev	3.277



B1L103S, U7-ch106, adc5

calib_packv5_041523_1651.root, FC#0, port C2

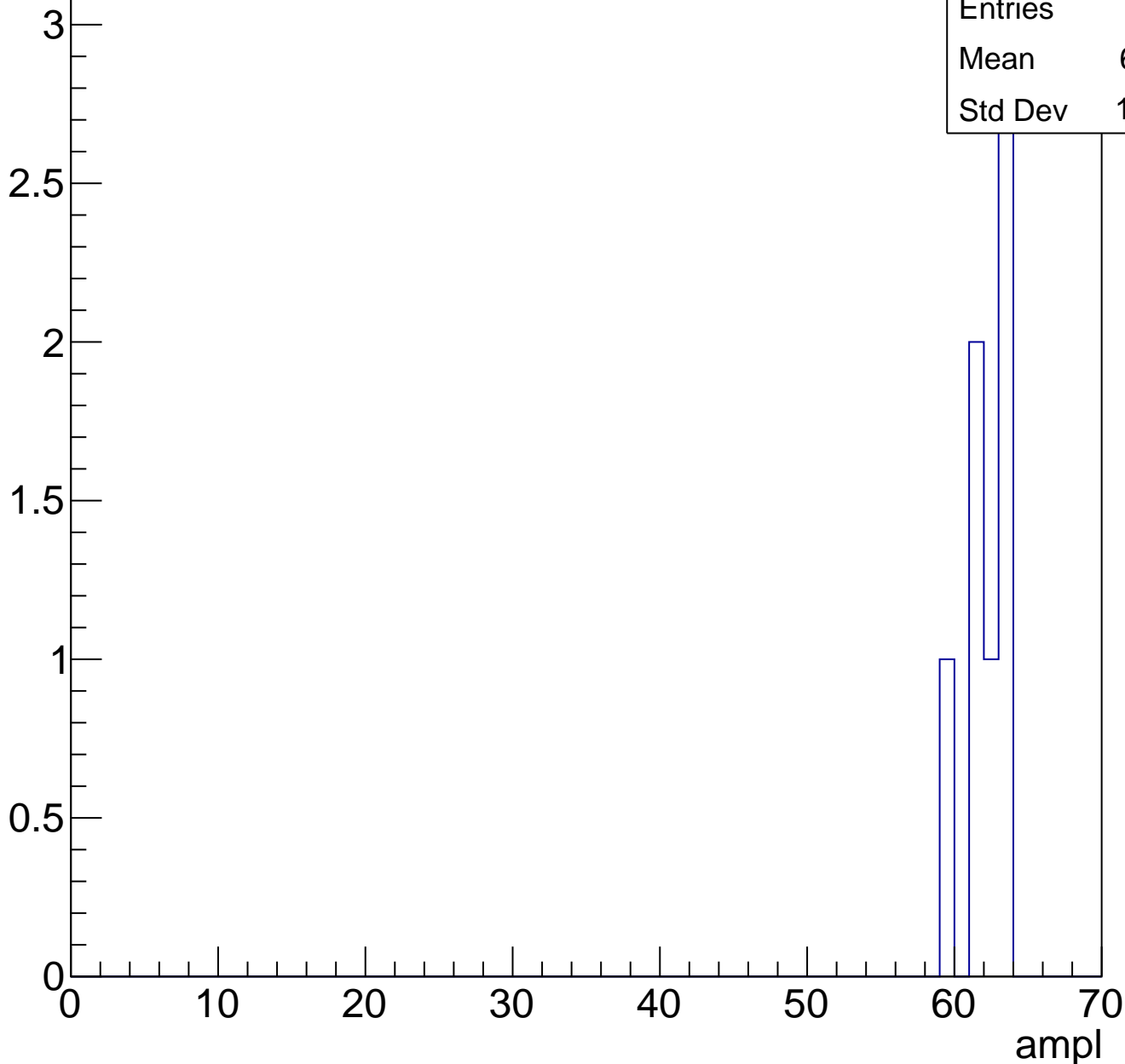
Entry



B1L103S, U7-ch106, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch106, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry



B1L103S, U7-ch107, adc0

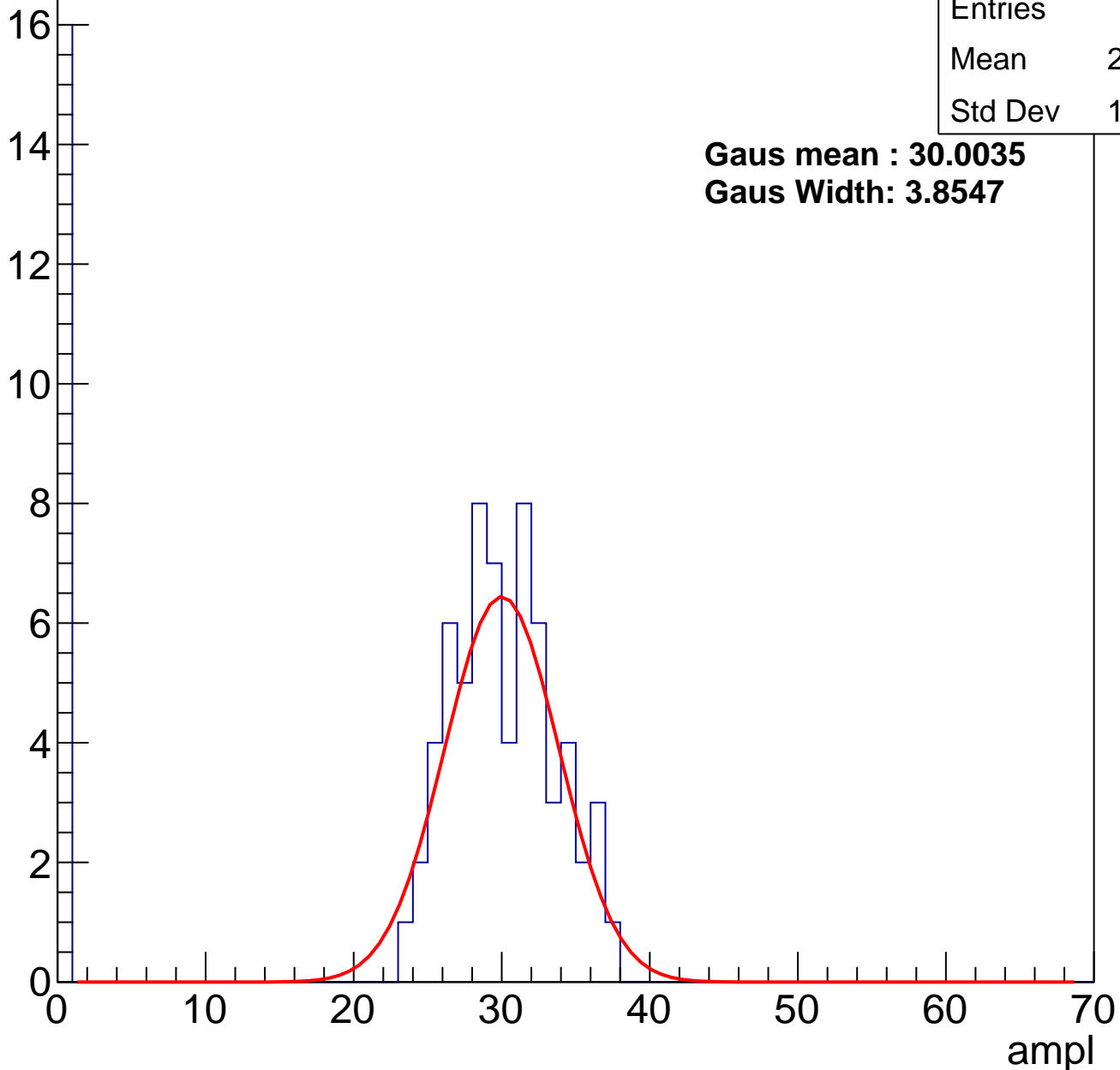
calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	23.74
Std Dev	12.24

Gaus mean : 30.0035

Gaus Width: 3.8547

Entry



B1L103S, U7-ch107, adc1

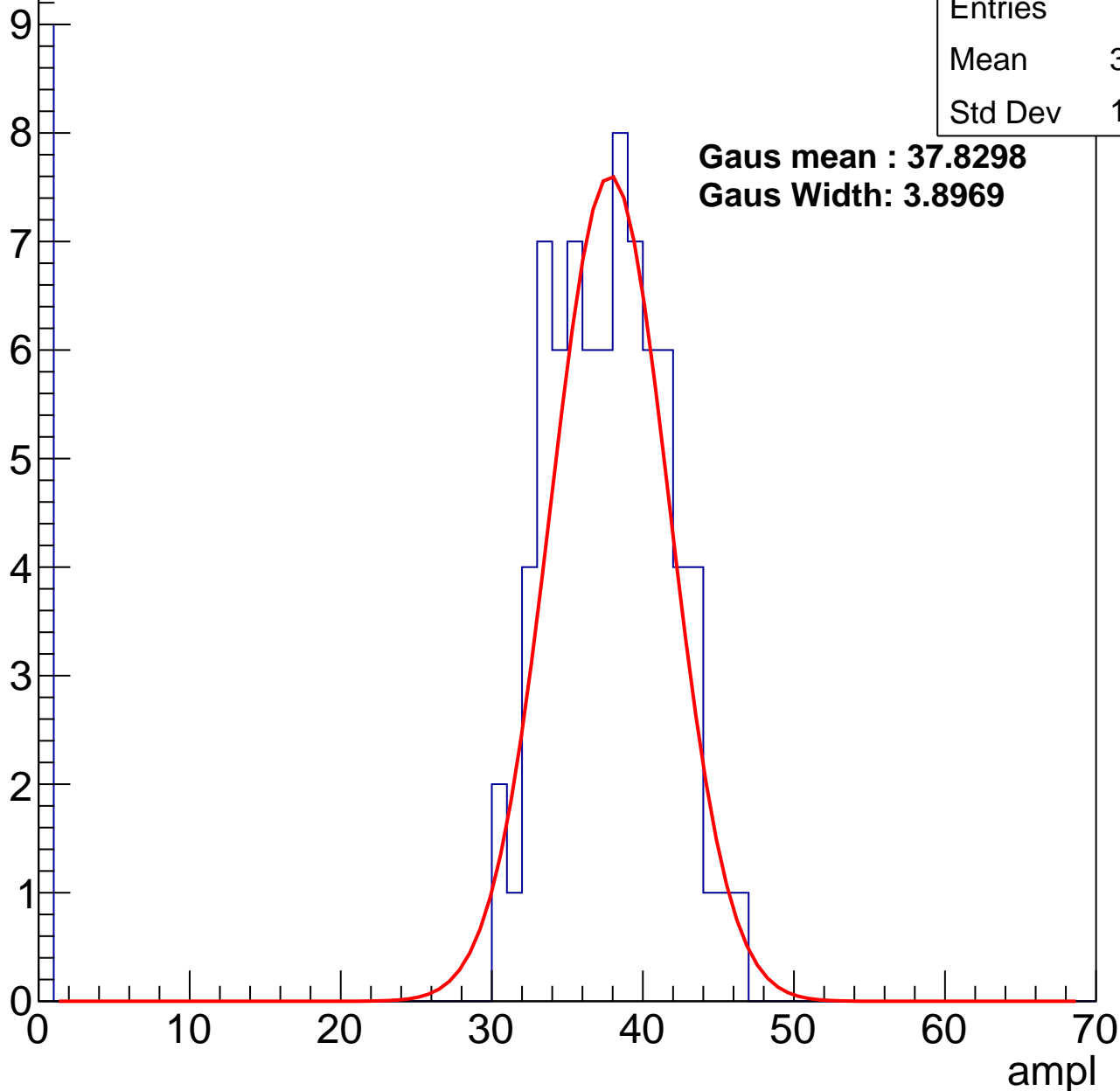
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	86
Mean	33.43
Std Dev	11.95

Gaus mean : 37.8298

Gaus Width: 3.8969



B1L103S, U7-ch107, adc2

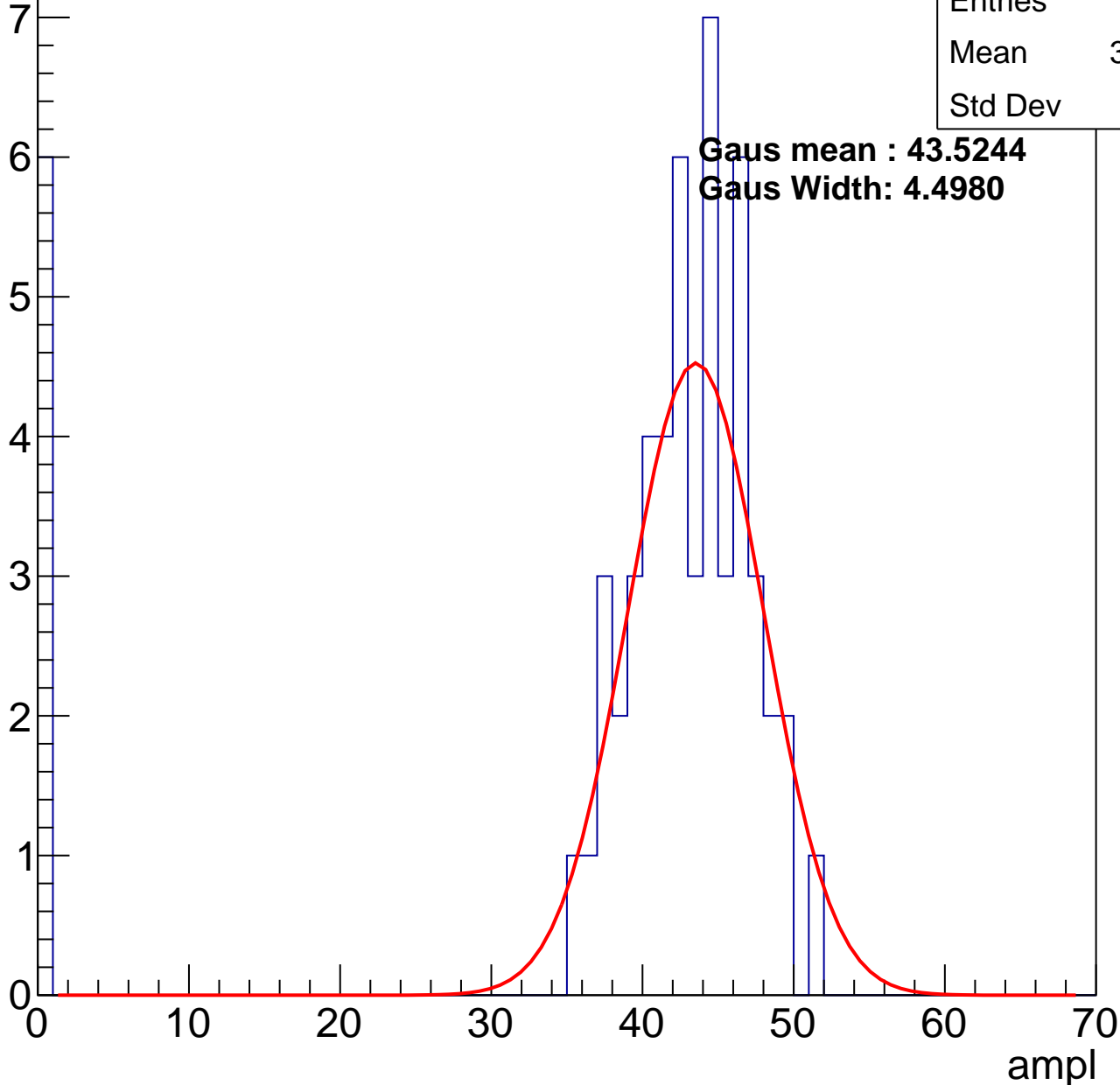
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	38.33
Std Dev	13.6

Gaus mean : 43.5244

Gaus Width: 4.4980

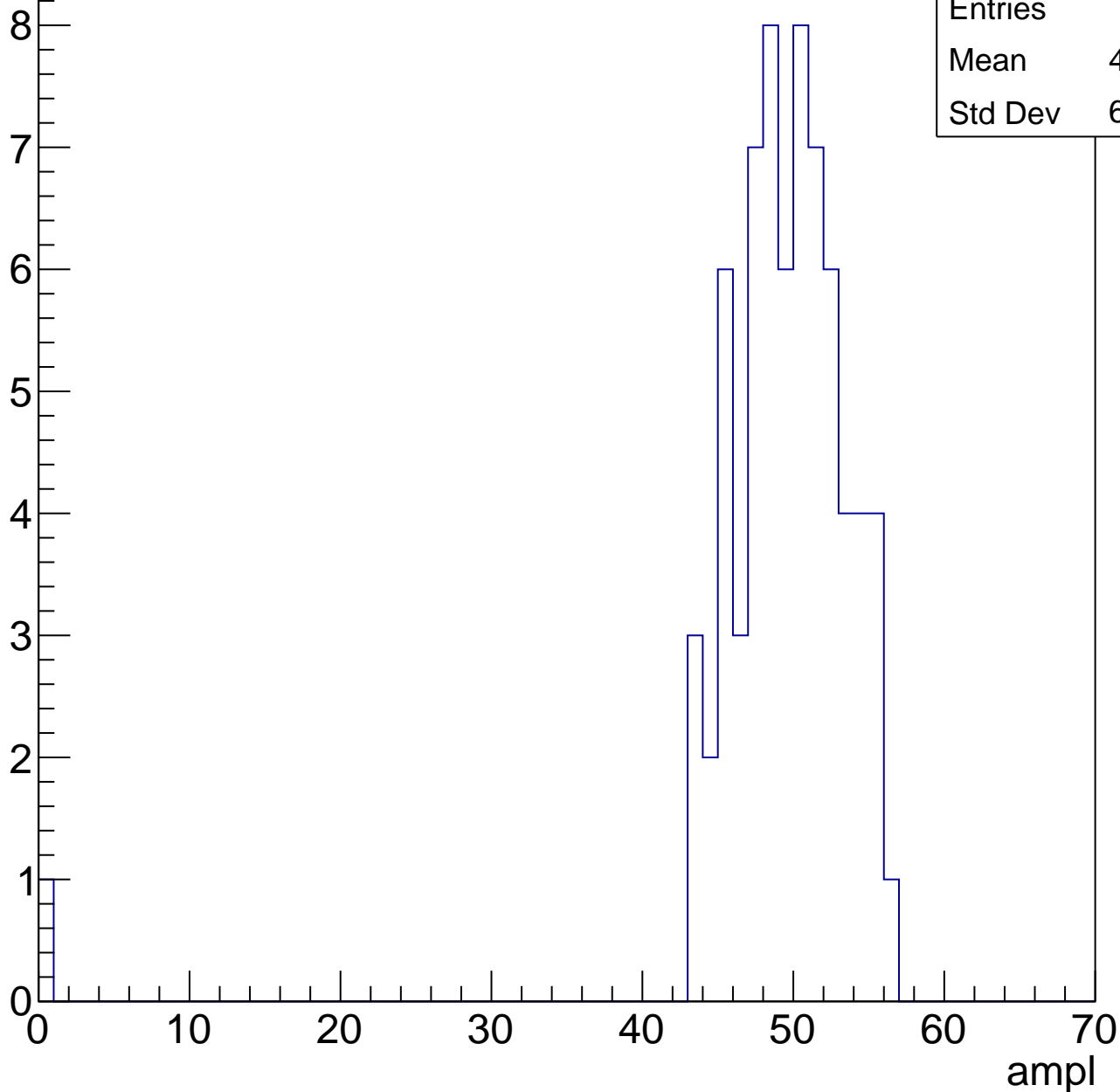


B1L103S, U7-ch107, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

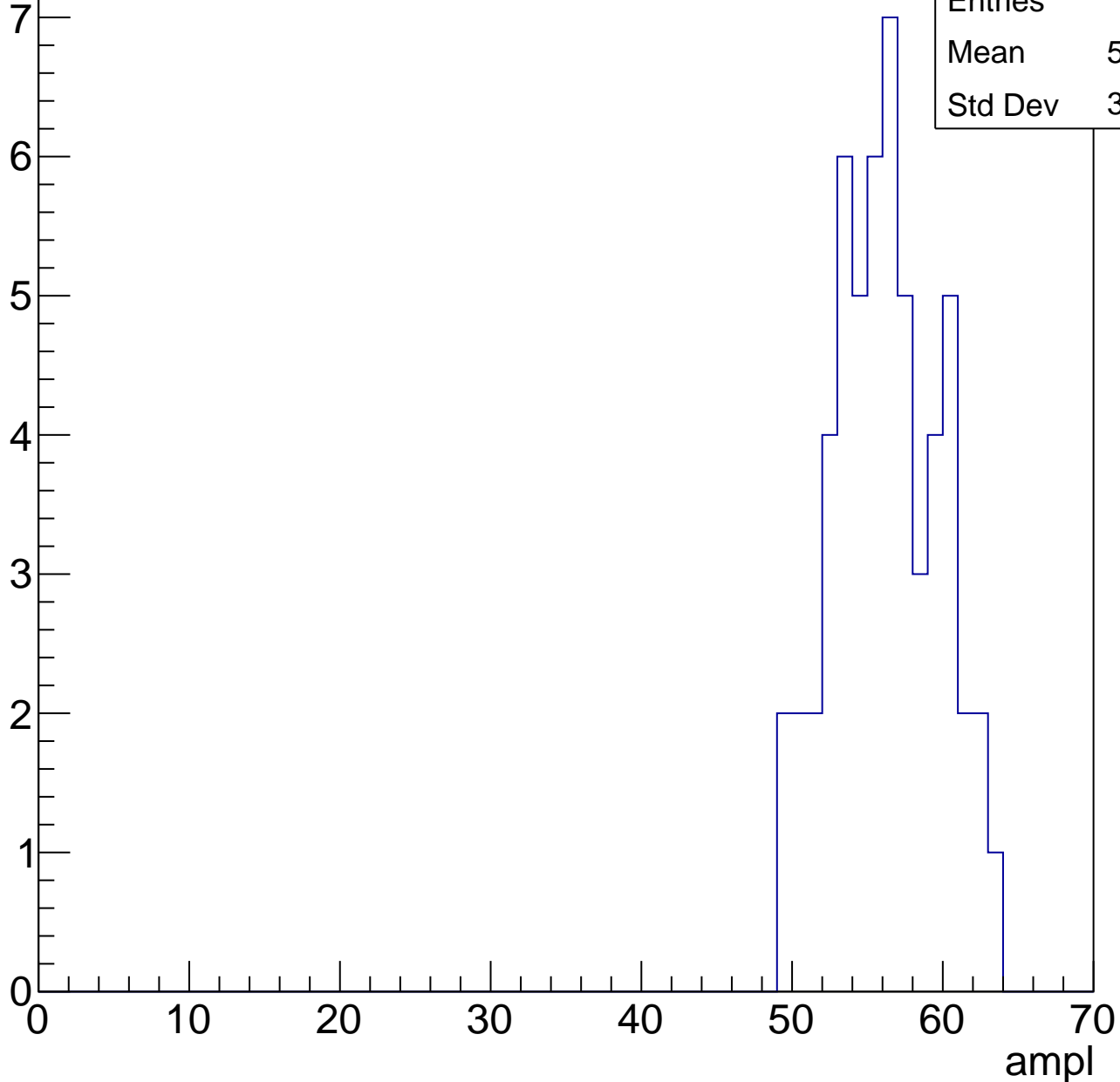
Entries	70
Mean	48.64
Std Dev	6.715



B1L103S, U7-ch107, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

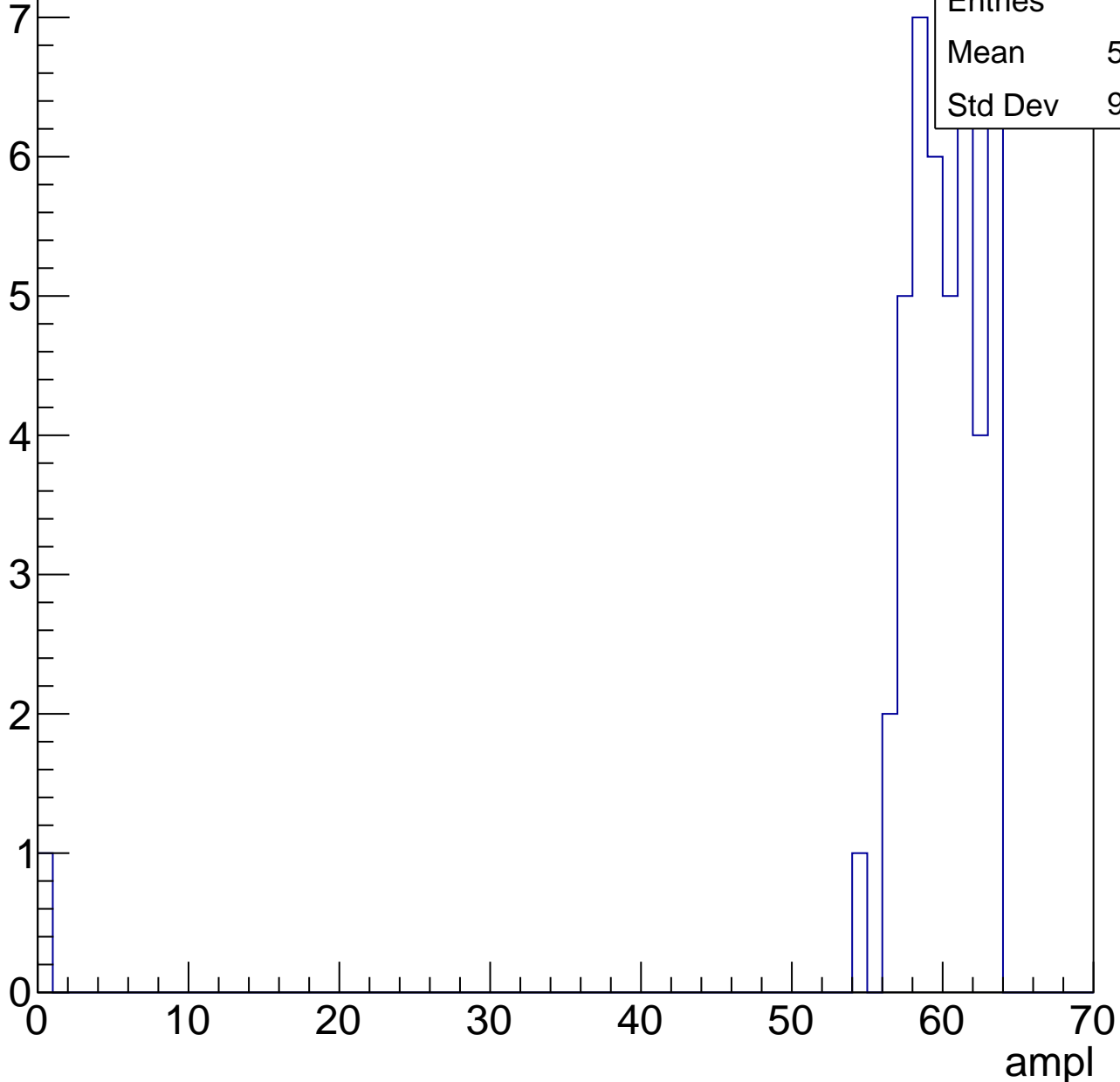


B1L103S, U7-ch107, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	45
Mean	58.38
Std Dev	9.085



B1L103S, U7-ch107, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch107, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

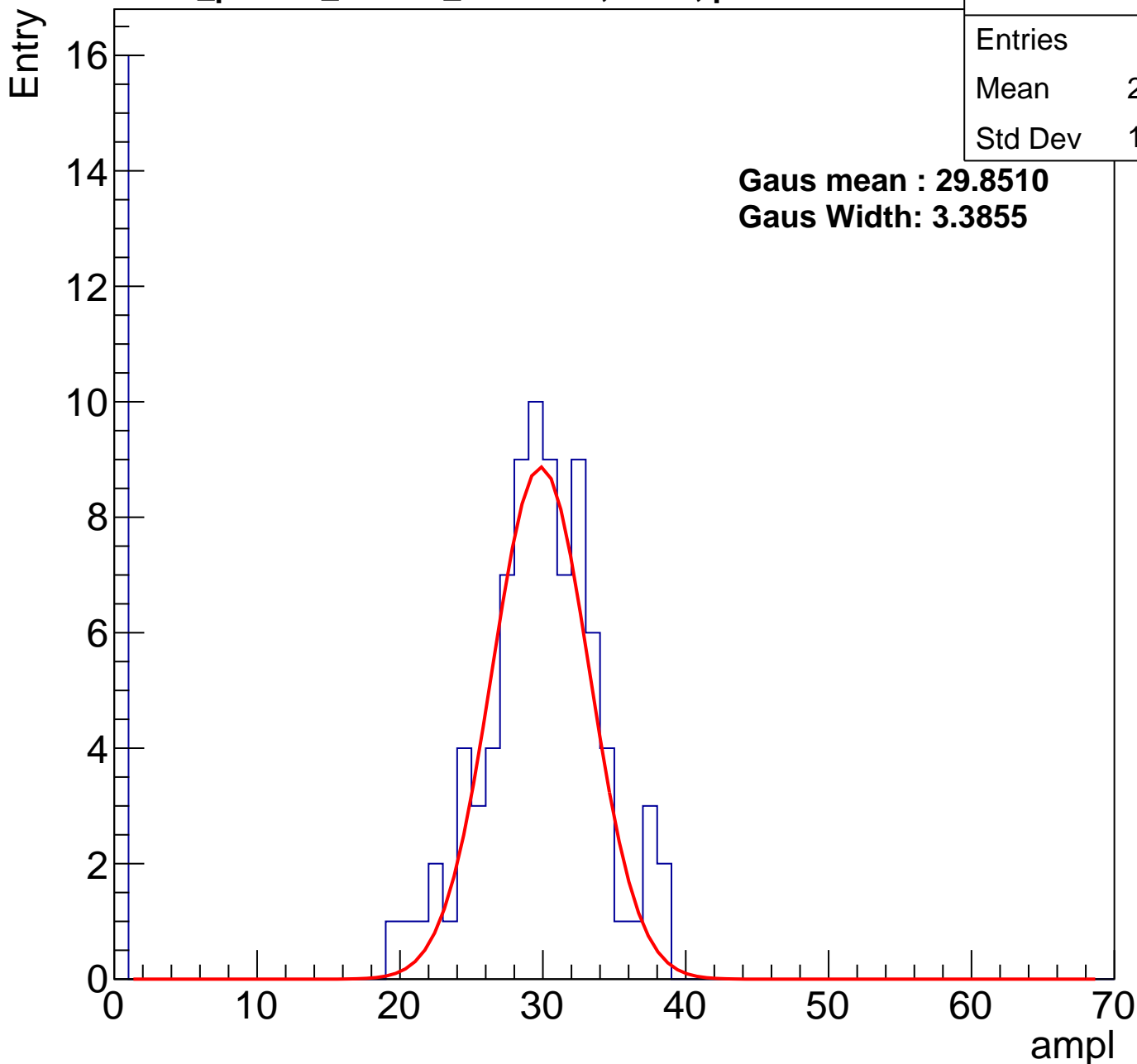
B1L103S, U7-ch108, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	101
Mean	24.75
Std Dev	11.34

Gaus mean : 29.8510

Gaus Width: 3.3855



B1L103S, U7-ch108, adc1

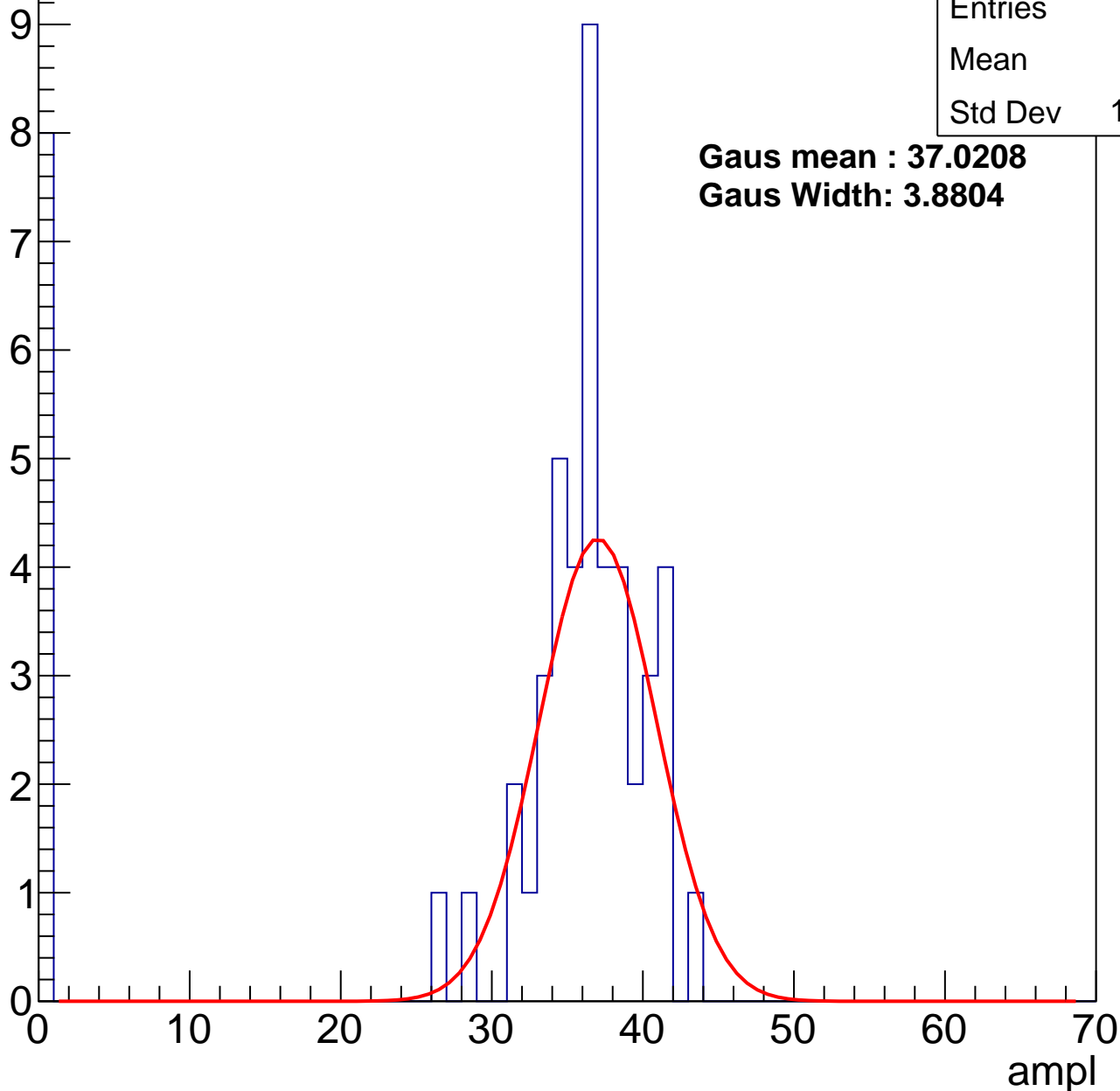
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	30.5
Std Dev	13.38

Gaus mean : 37.0208

Gaus Width: 3.8804



B1L103S, U7-ch108, adc2

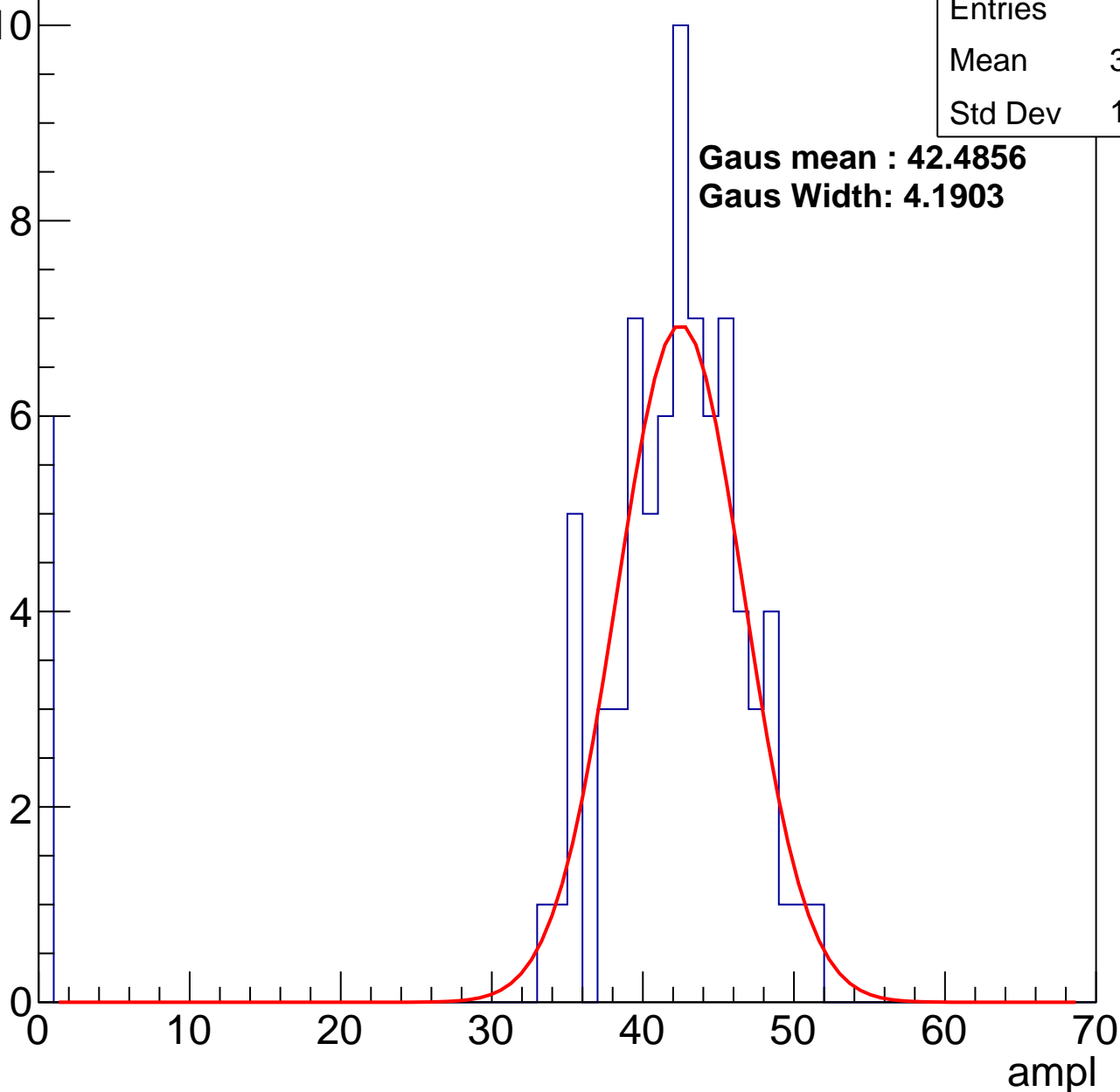
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	81
Mean	38.93
Std Dev	11.65

Gaus mean : 42.4856

Gaus Width: 4.1903

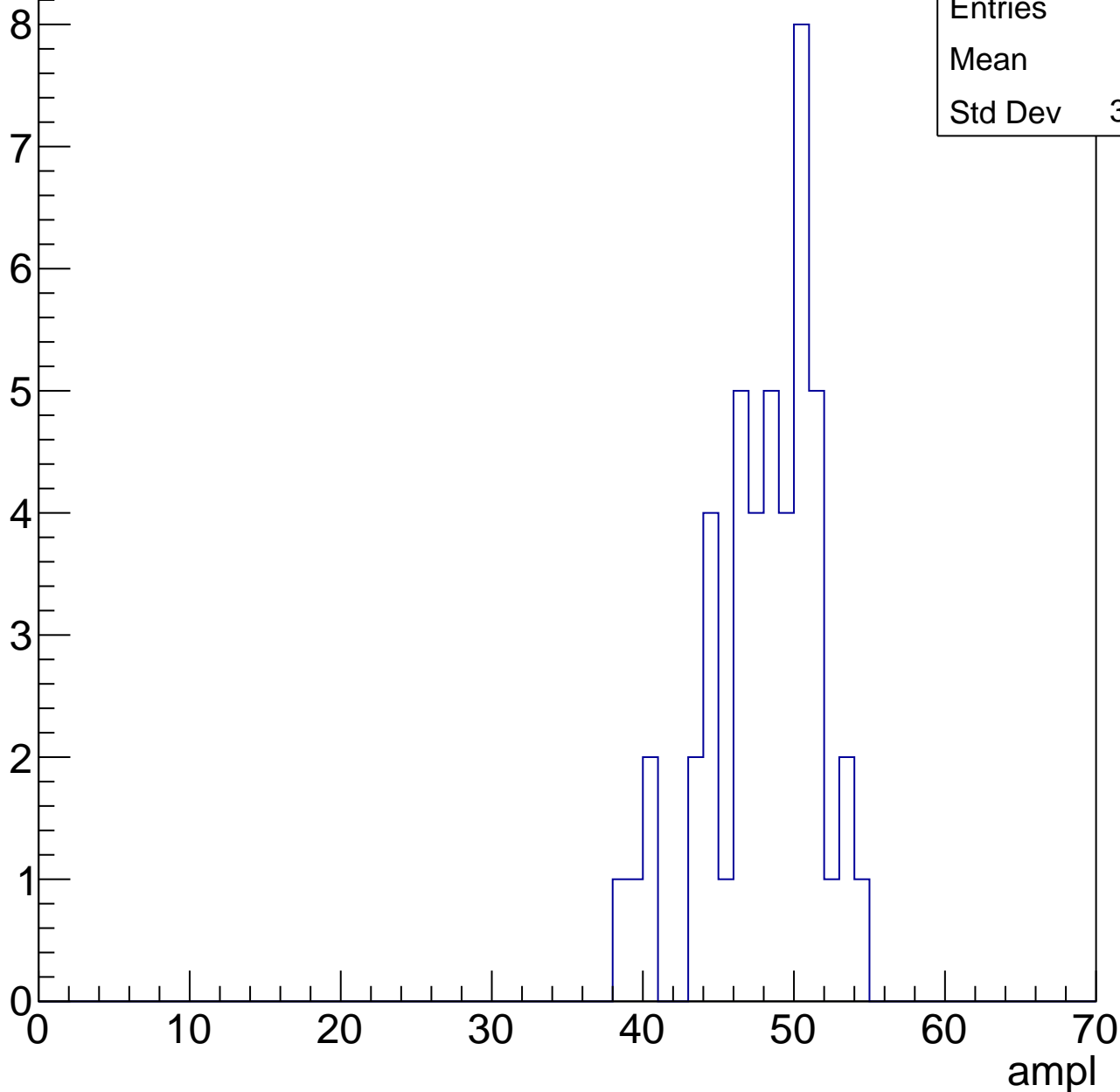


B1L103S, U7-ch108, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

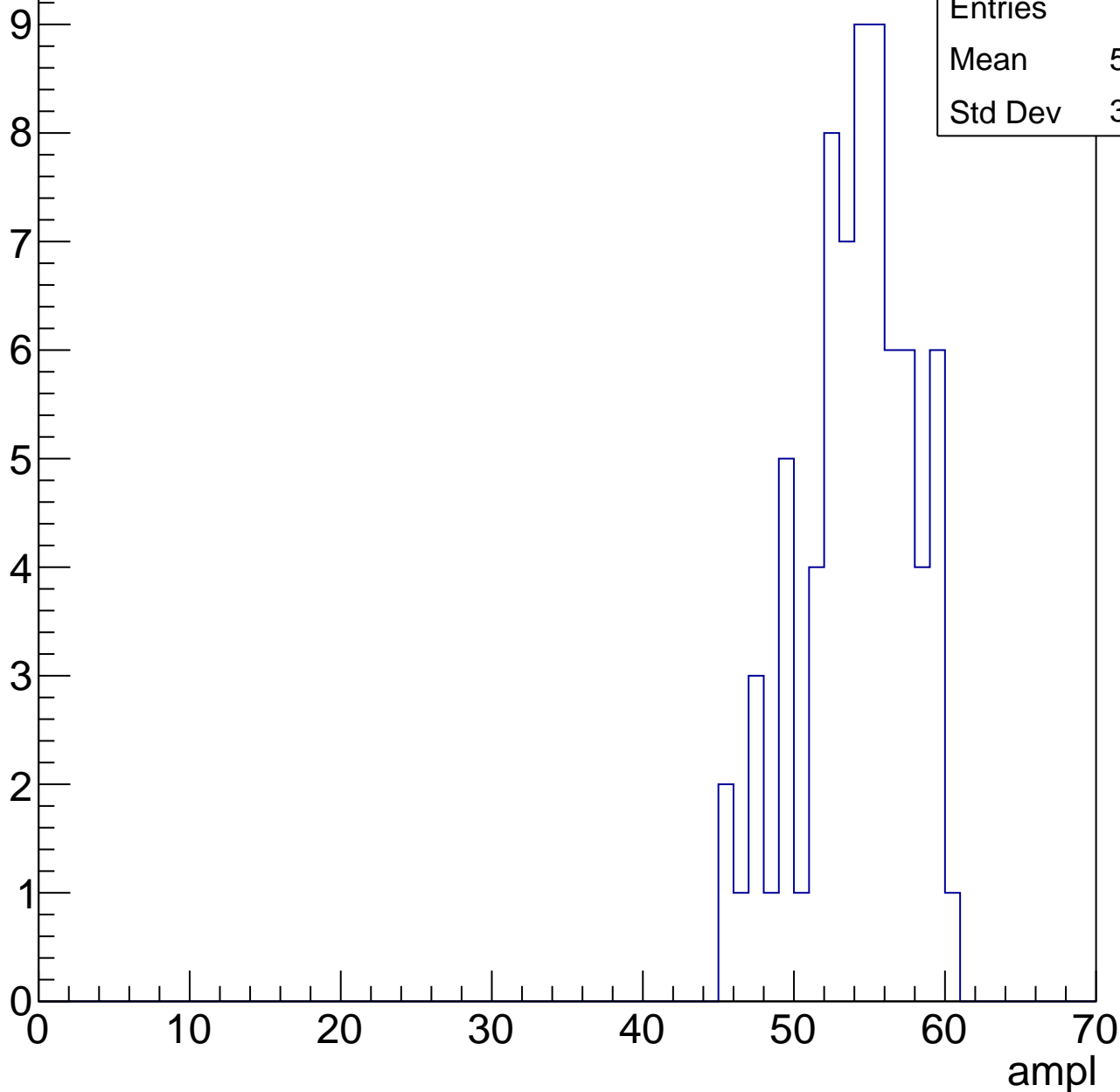
Entries	46
Mean	47.5
Std Dev	3.693



B1L103S, U7-ch108, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

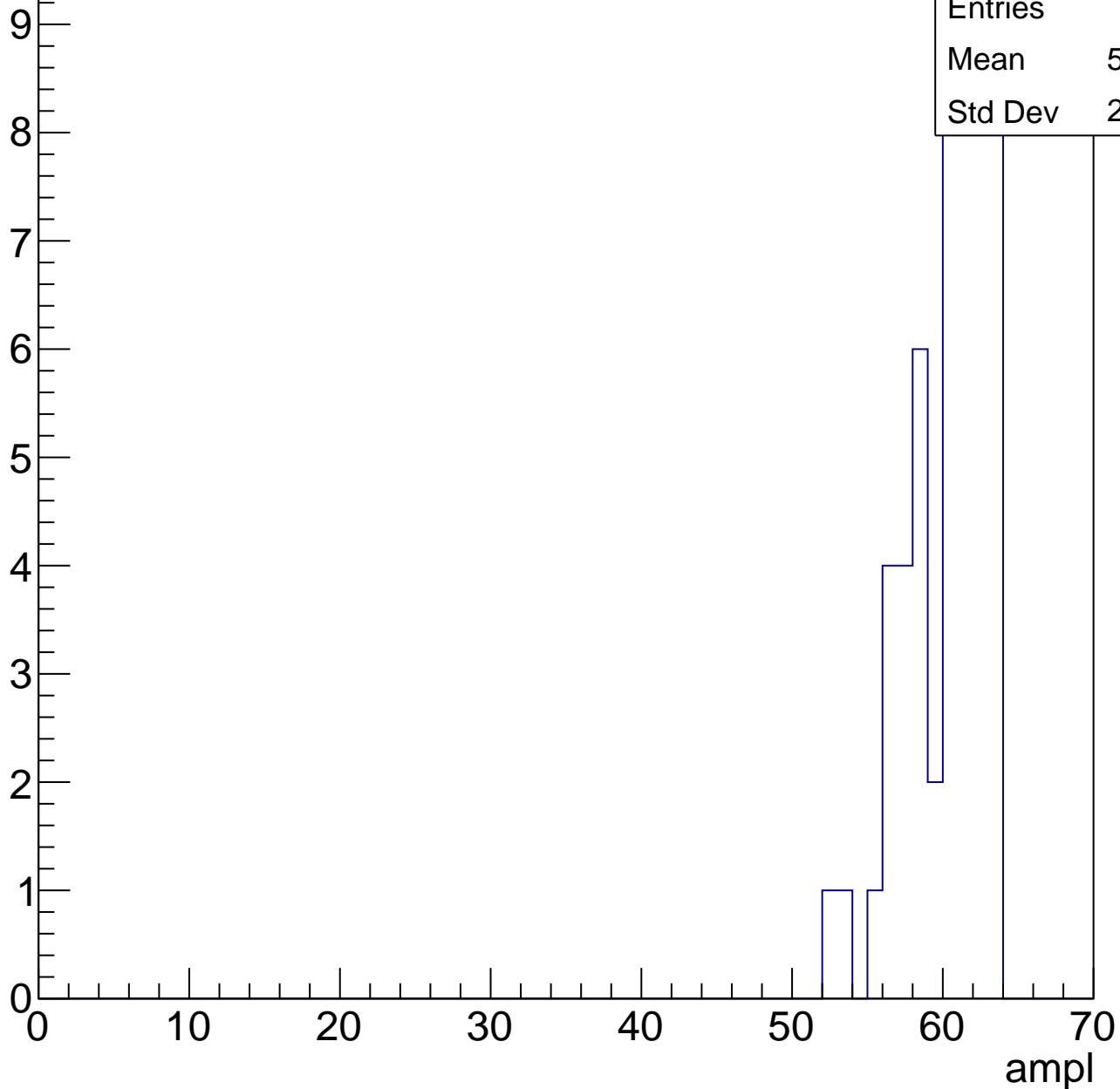


Entries	73
Mean	53.64
Std Dev	3.613

B1L103S, U7-ch108, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch108, adc6

calib_packv5_041523_1651.root, FC#0, port C2

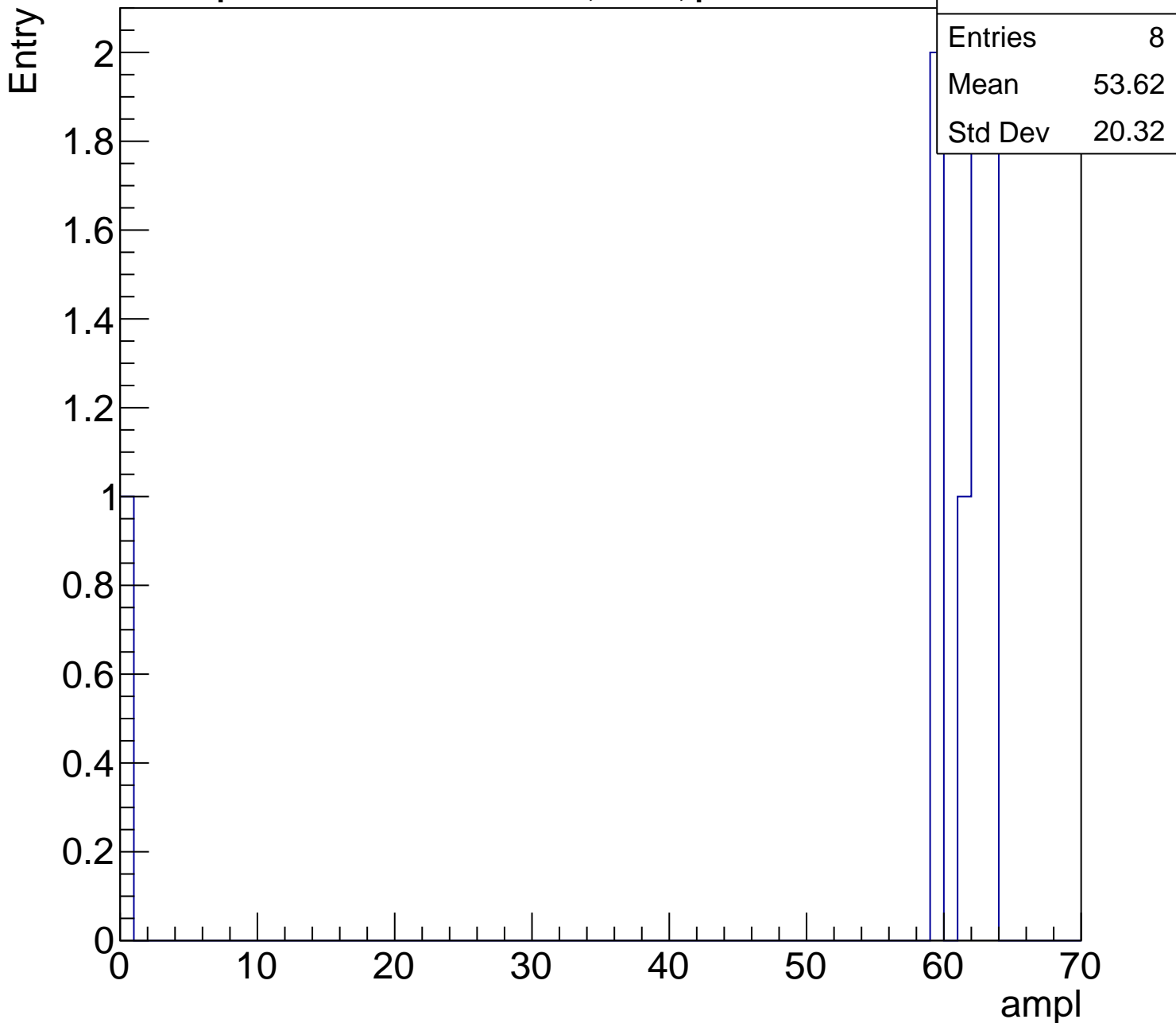
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	8
Mean	53.62
Std Dev	20.32

0 10 20 30 40 50 60 70

ampl



B1L103S, U7-ch108, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	19
Mean	0
Std Dev	0

B1L103S, U7-ch109, adc0

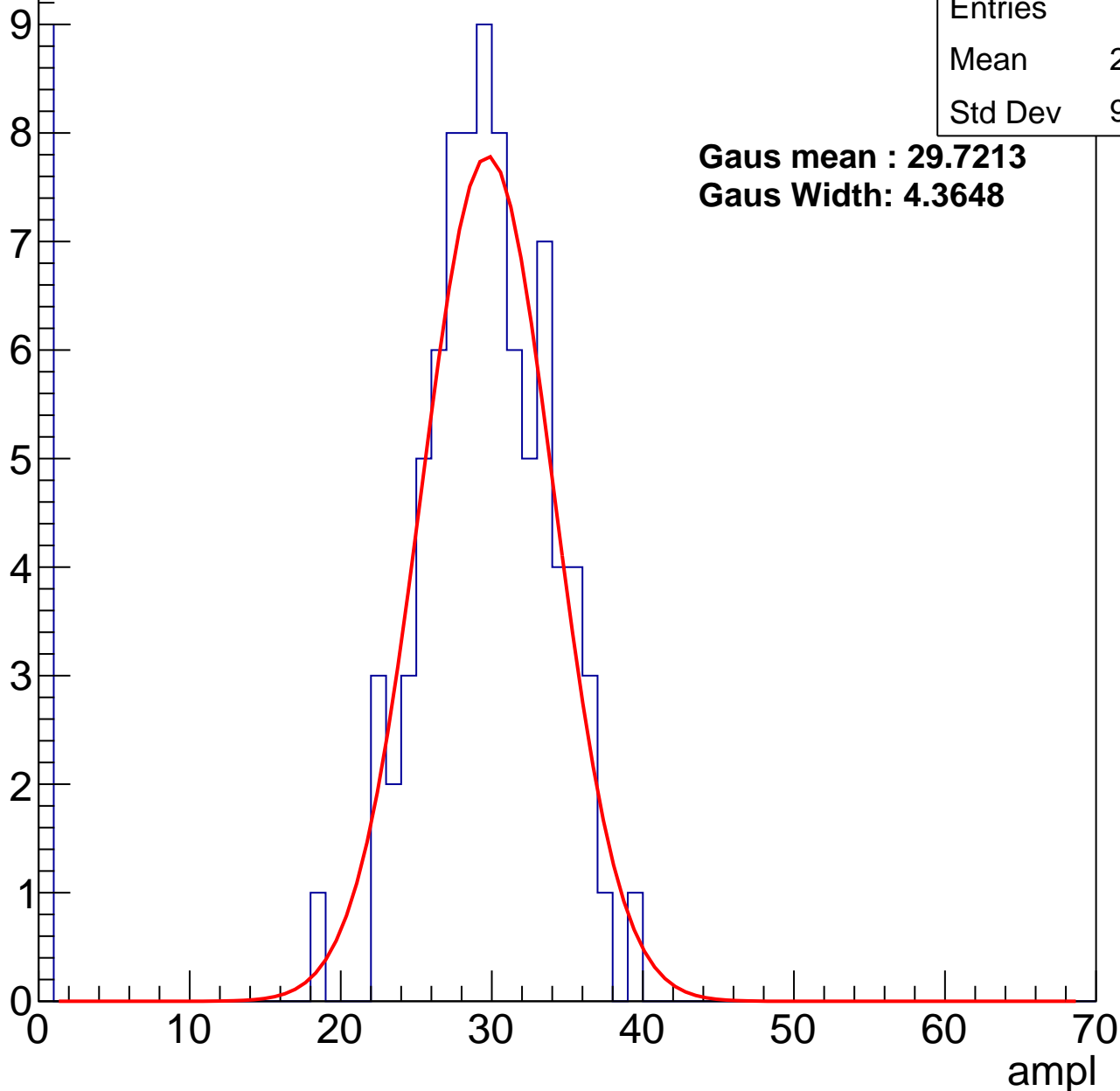
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	93
Mean	26.46
Std Dev	9.449

Gaus mean : 29.7213

Gaus Width: 4.3648



B1L103S, U7-ch109, adc1

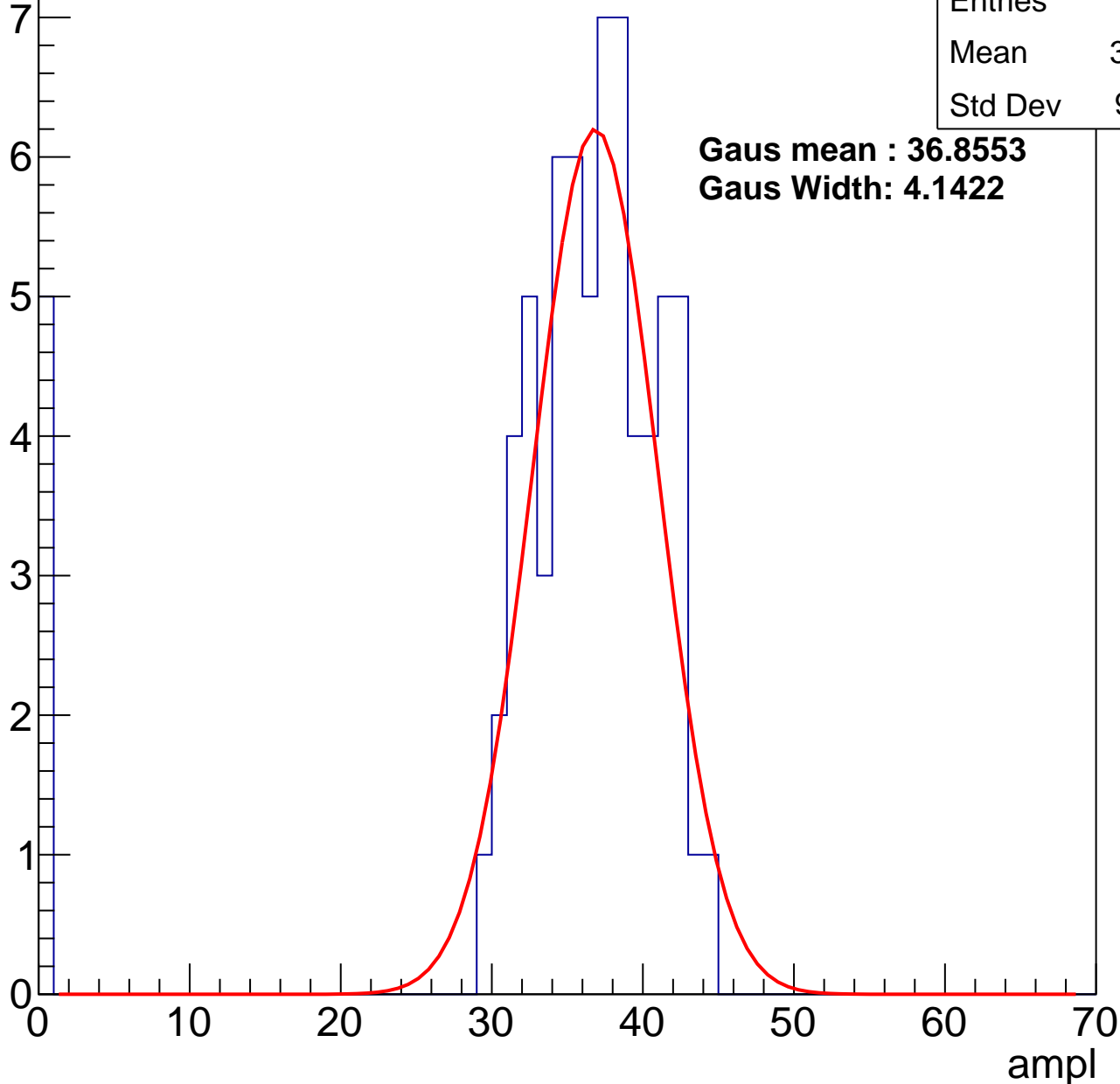
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	33.93
Std Dev	9.991

Gaus mean : 36.8553

Gaus Width: 4.1422



B1L103S, U7-ch109, adc2

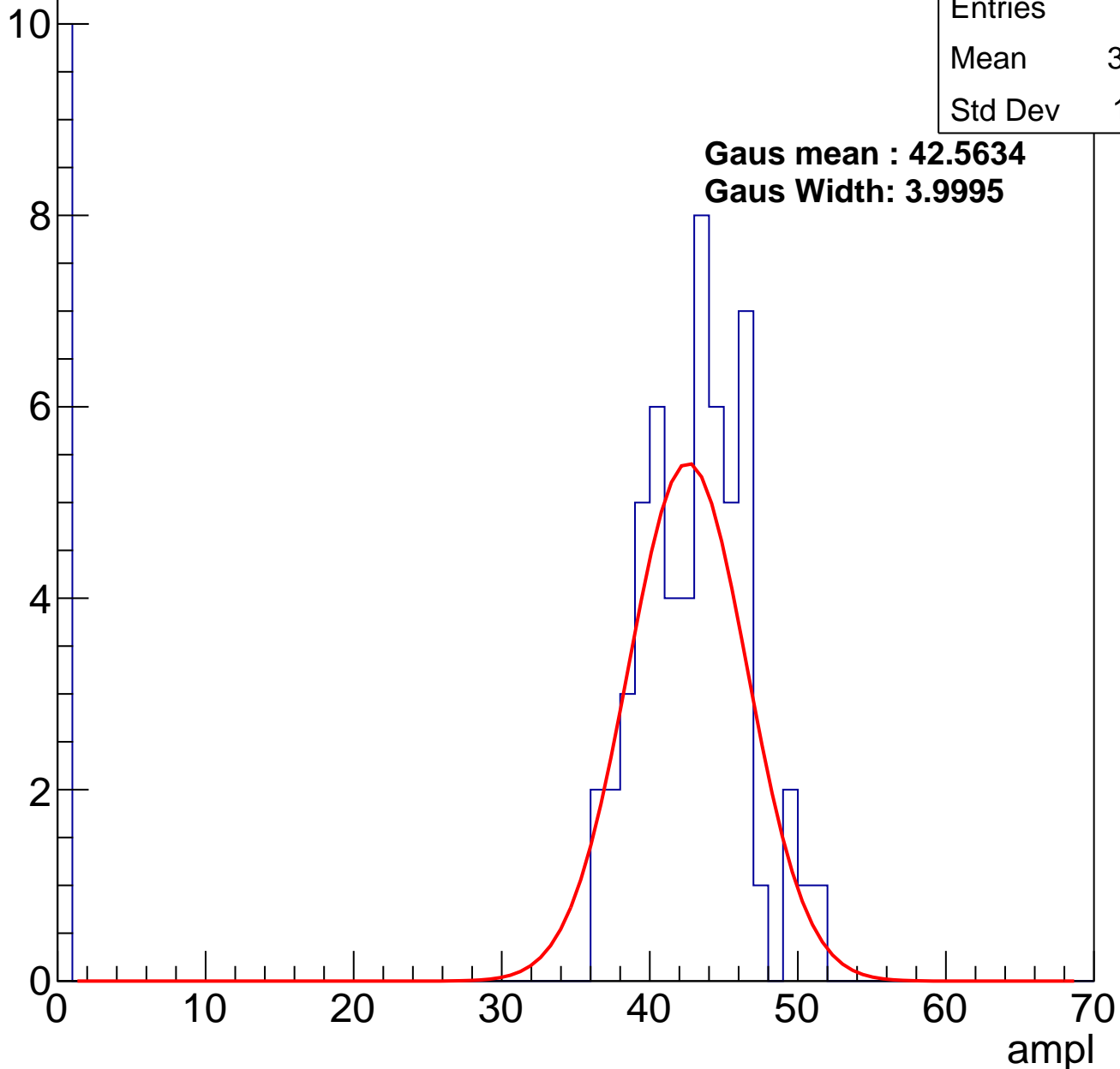
calib_packv5_041523_1651.root, FC#0, port C2

Entries	67
Mean	36.24
Std Dev	15.51

Gaus mean : 42.5634

Gaus Width: 3.9995

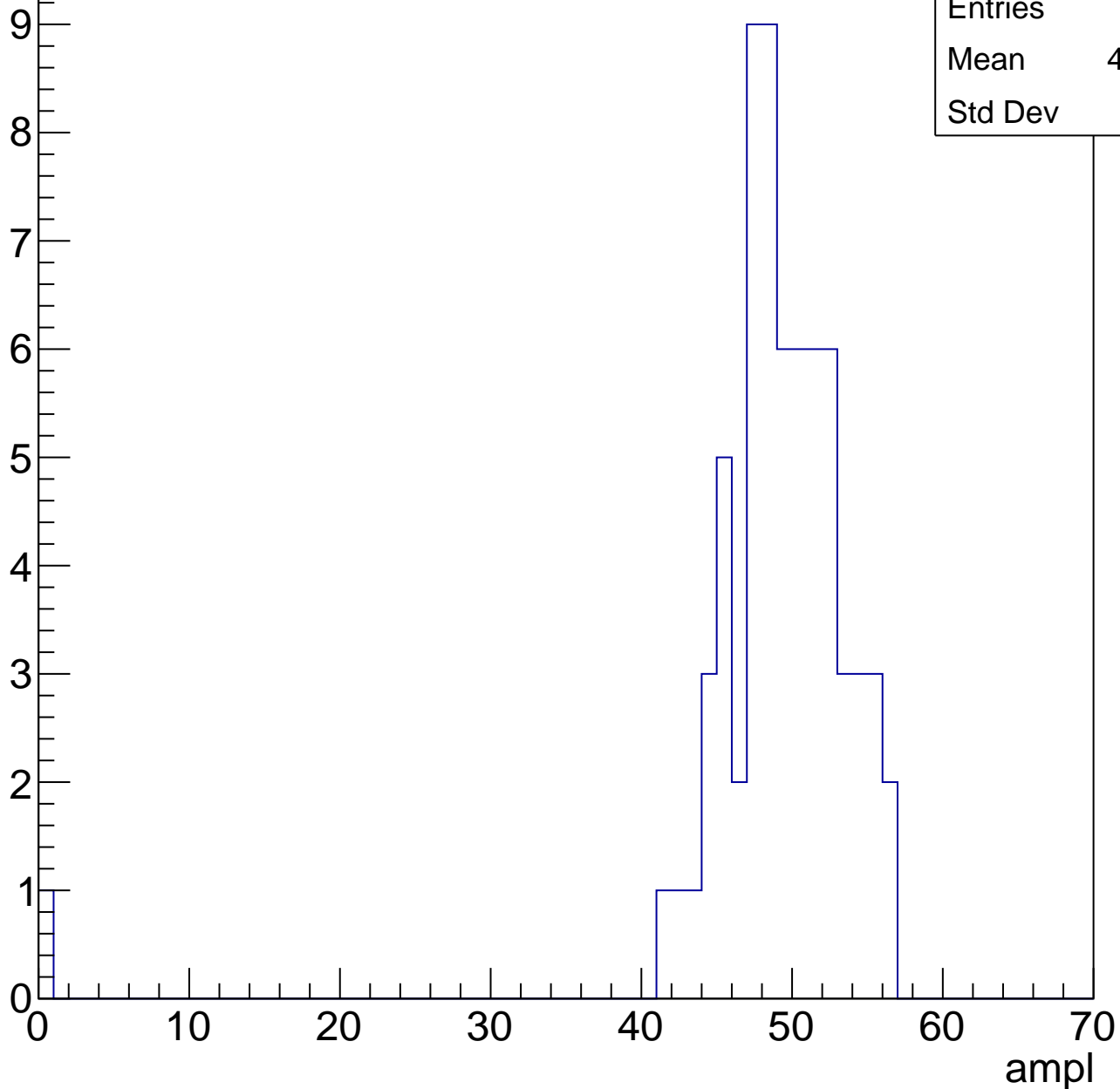
Entry



B1L103S, U7-ch109, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry



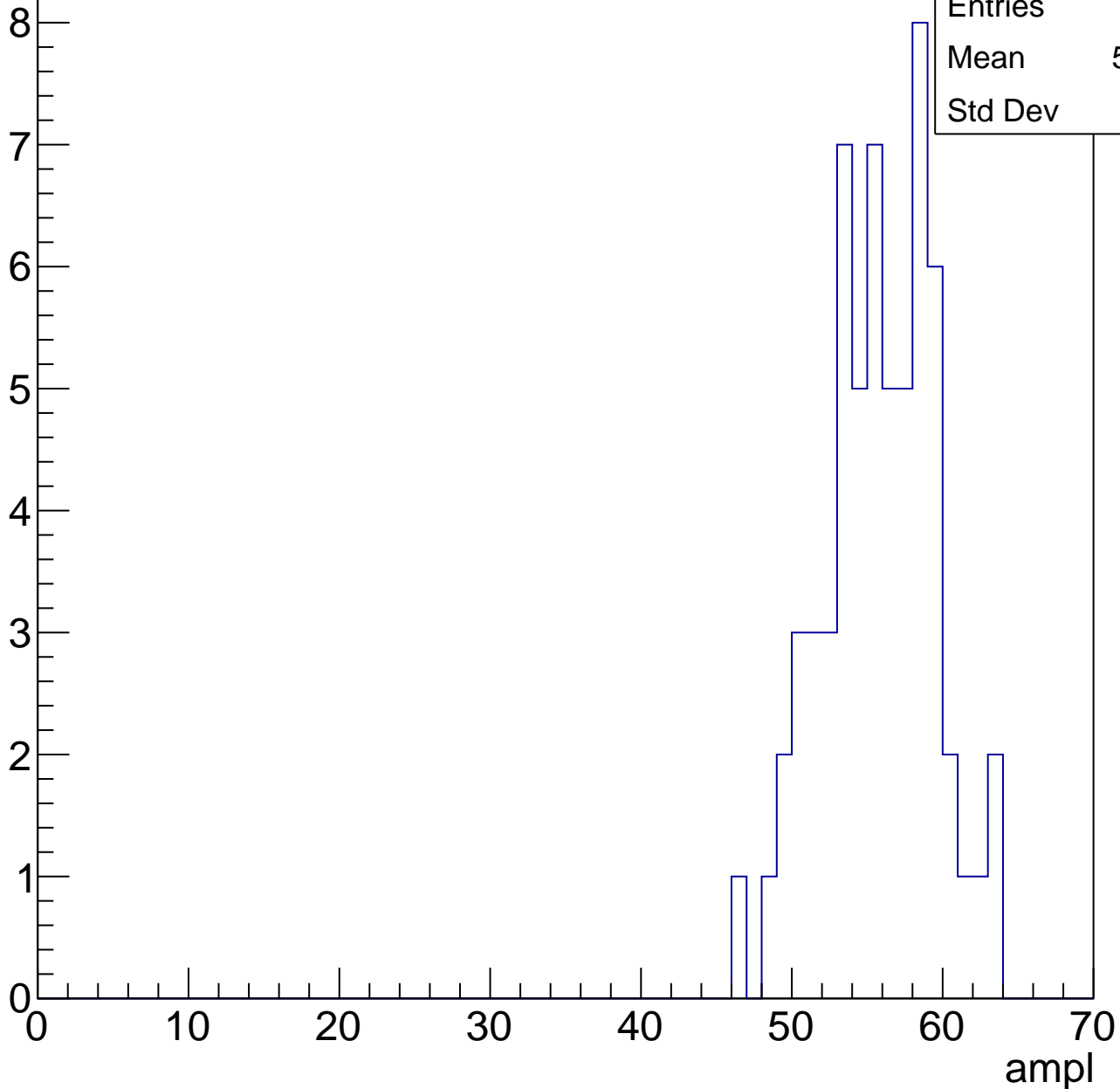
Entries	67
Mean	48.36
Std Dev	6.86

B1L103S, U7-ch109, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	55.31
Std Dev	3.67



B1L103S, U7-ch109, adc5

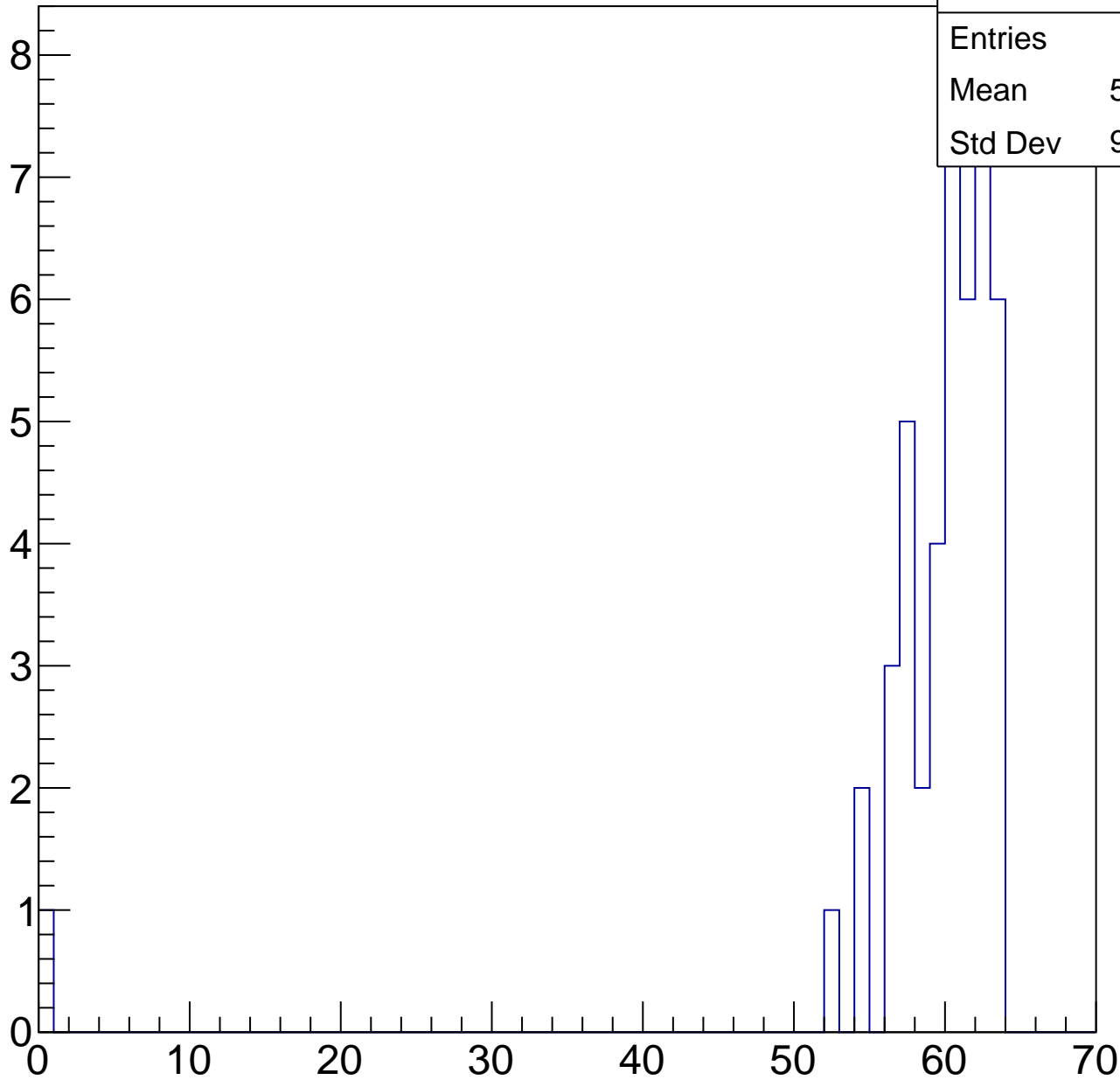
calib_packv5_041523_1651.root, FC#0, port C2

Entry

8
7
6
5
4
3
2
1
0

Entries	46
Mean	58.37
Std Dev	9.102

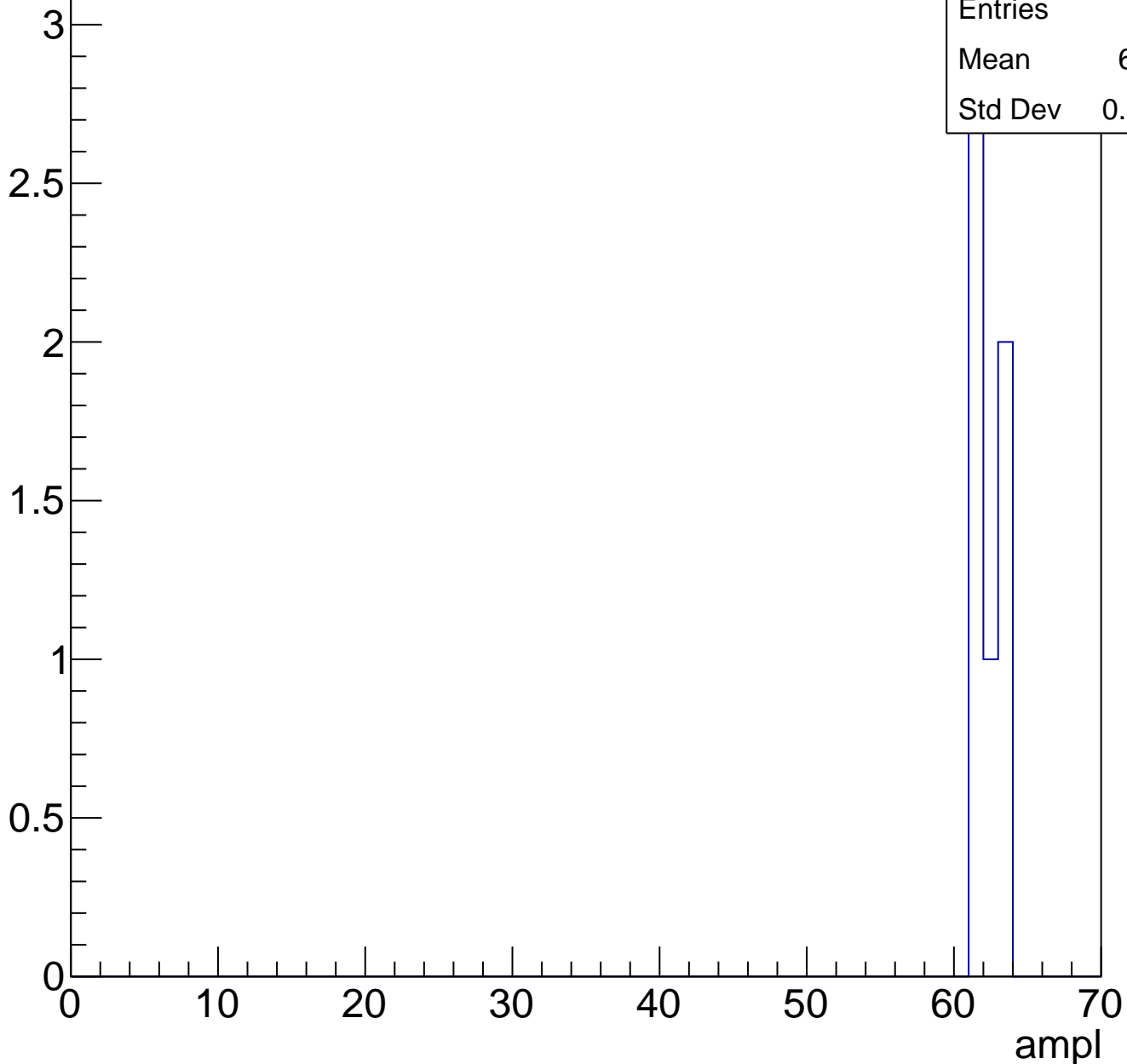
ampl



B1L103S, U7-ch109, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch109, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	18
Mean	0
Std Dev	0

B1L103S, U7-ch110, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	23.97
Std Dev	11.76

Gaus mean : 29.6933

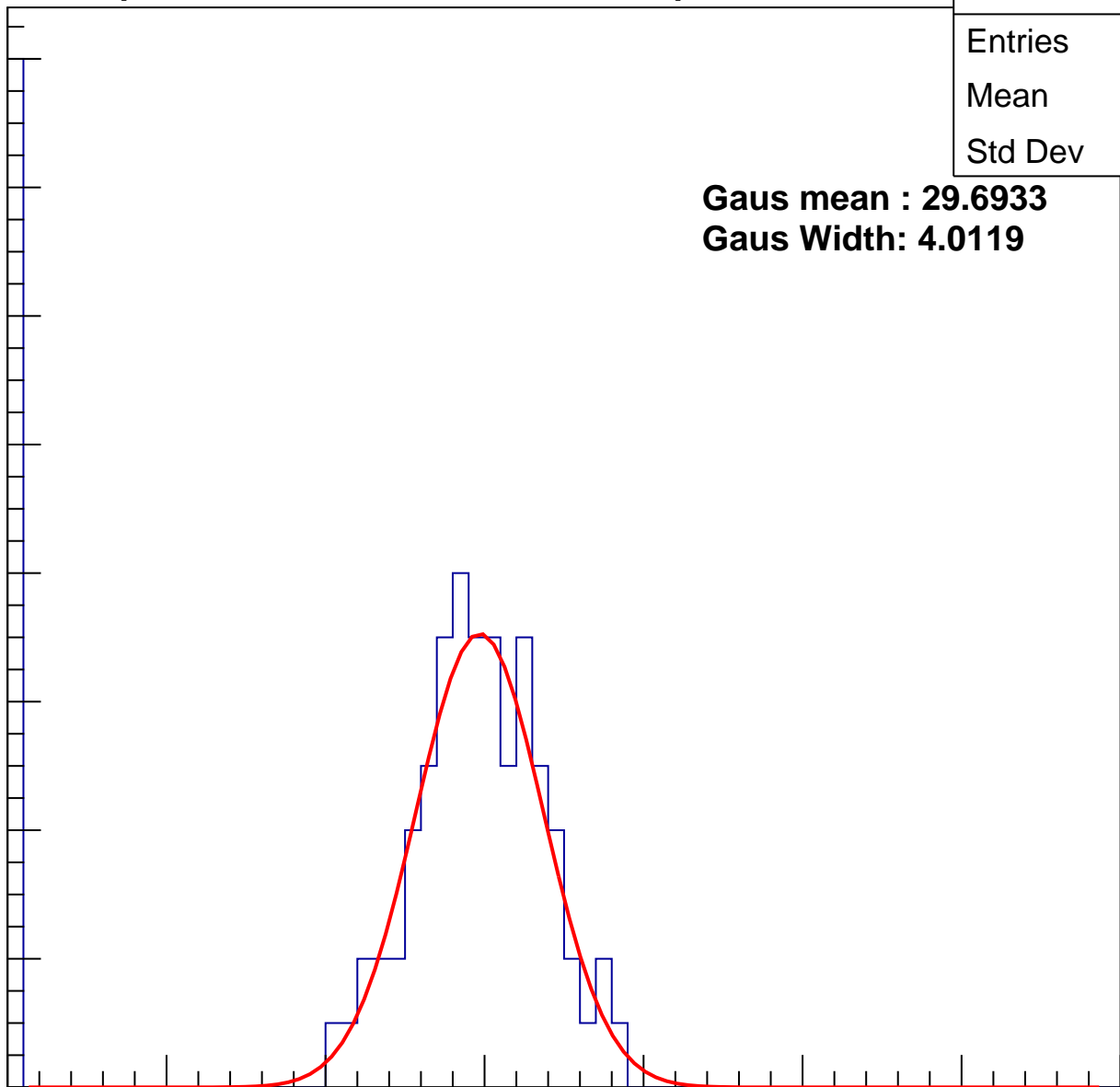
Gaus Width: 4.0119

Entry

16
14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U7-ch110, adc1

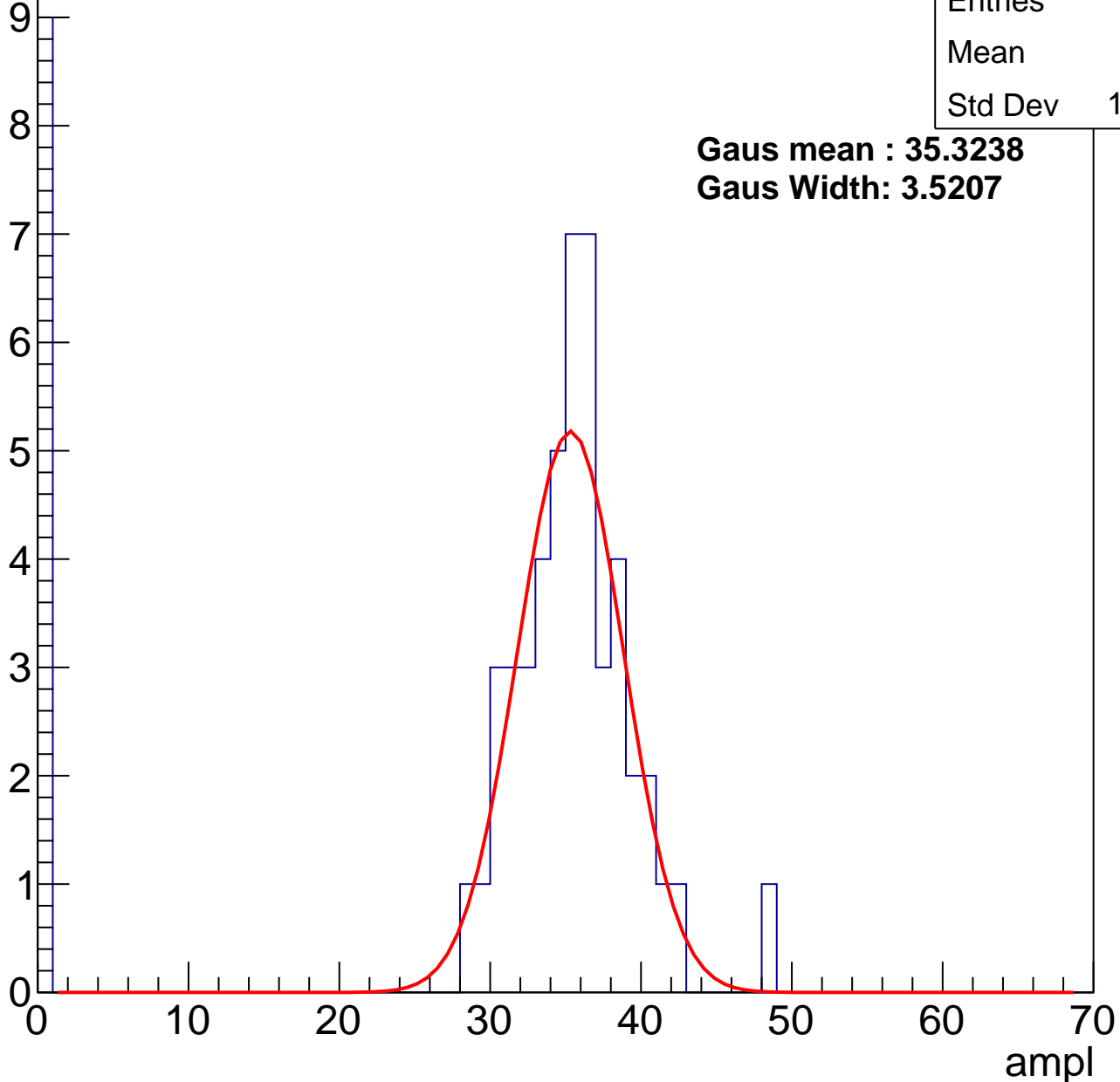
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	57
Mean	29.6
Std Dev	13.25

Gaus mean : 35.3238

Gaus Width: 3.5207



B1L103S, U7-ch110, adc2

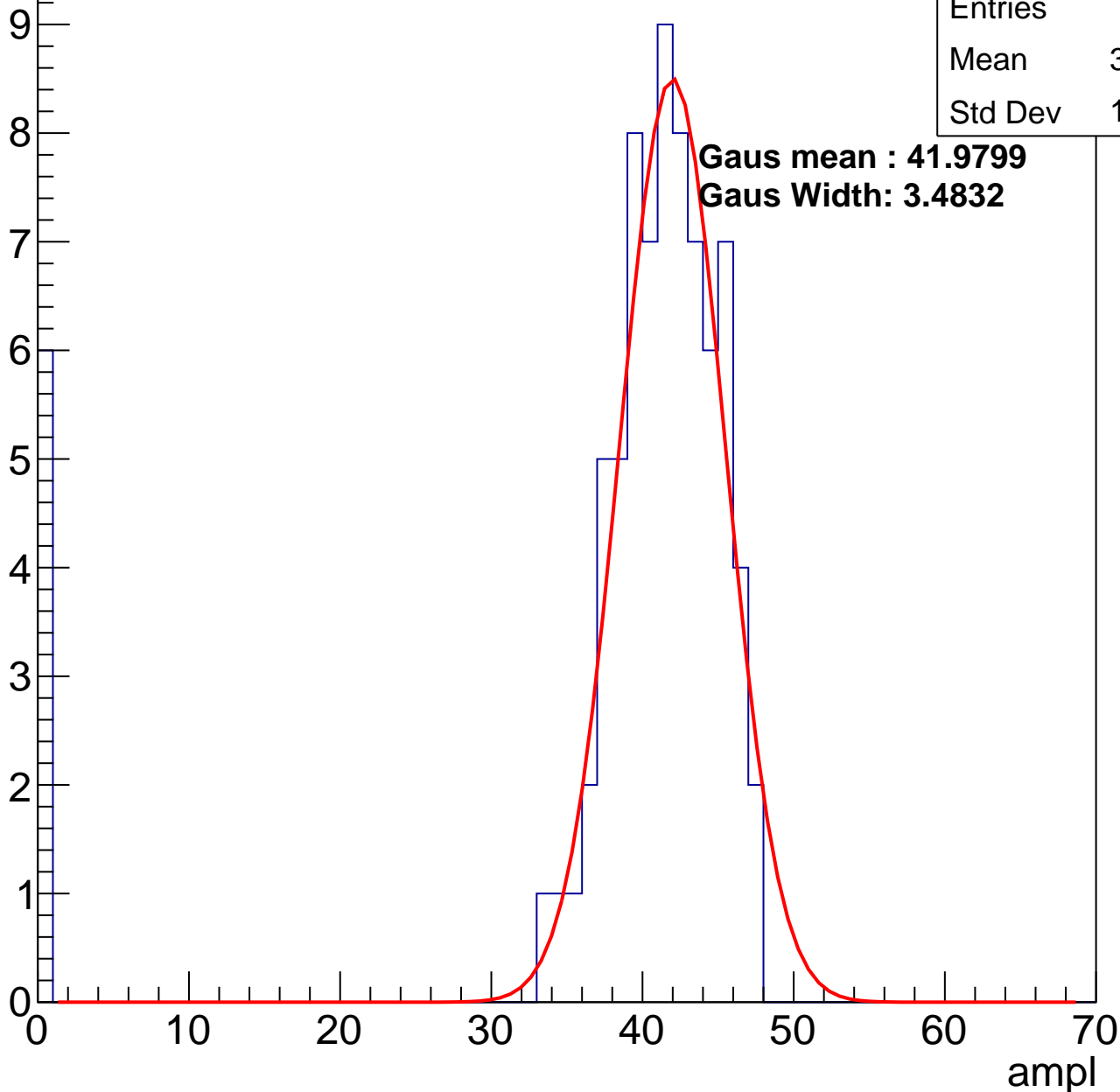
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	79
Mean	38.03
Std Dev	11.32

Gaus mean : 41.9799

Gaus Width: 3.4832

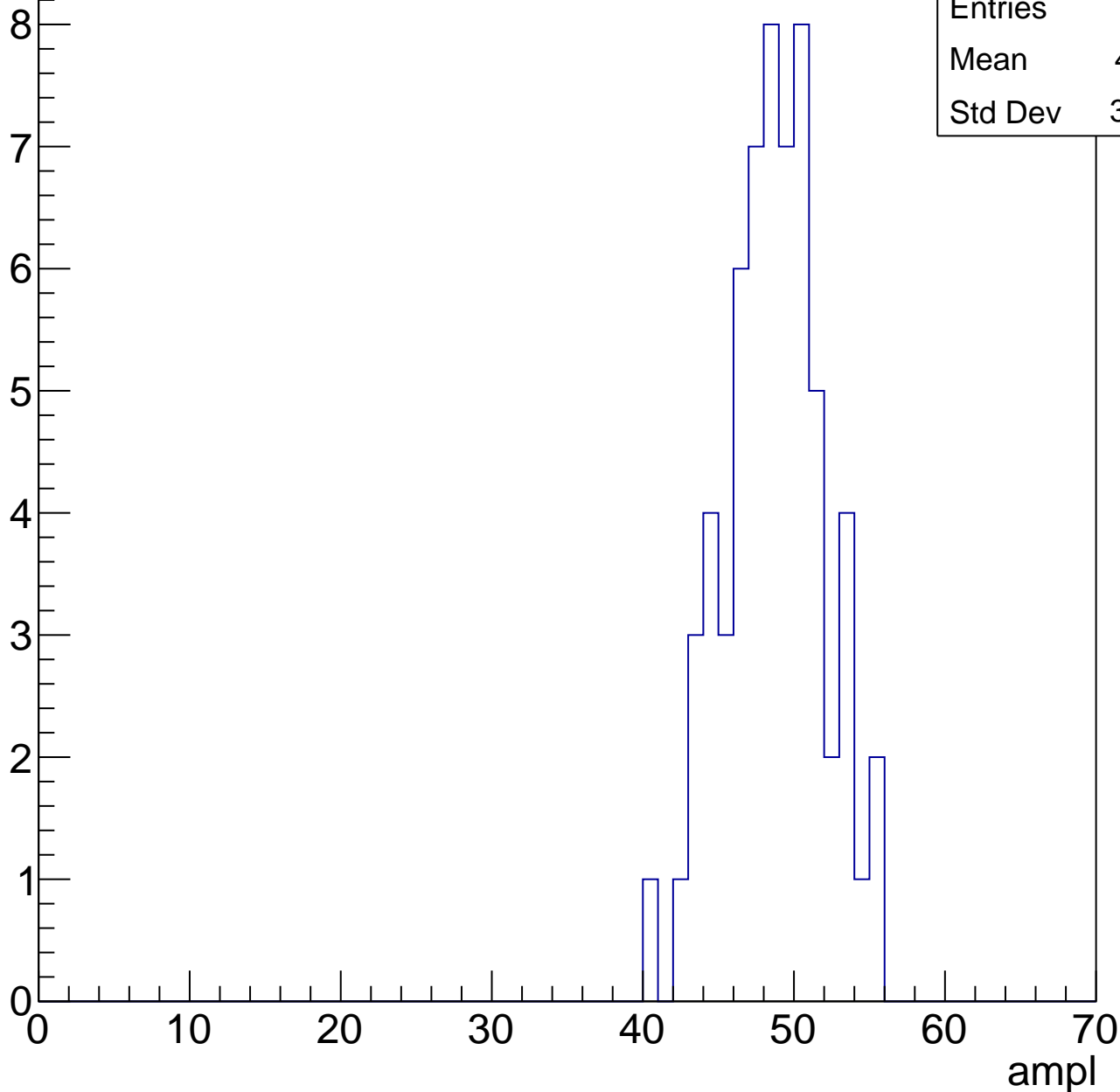


B1L103S, U7-ch110, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	48.21
Std Dev	3.224

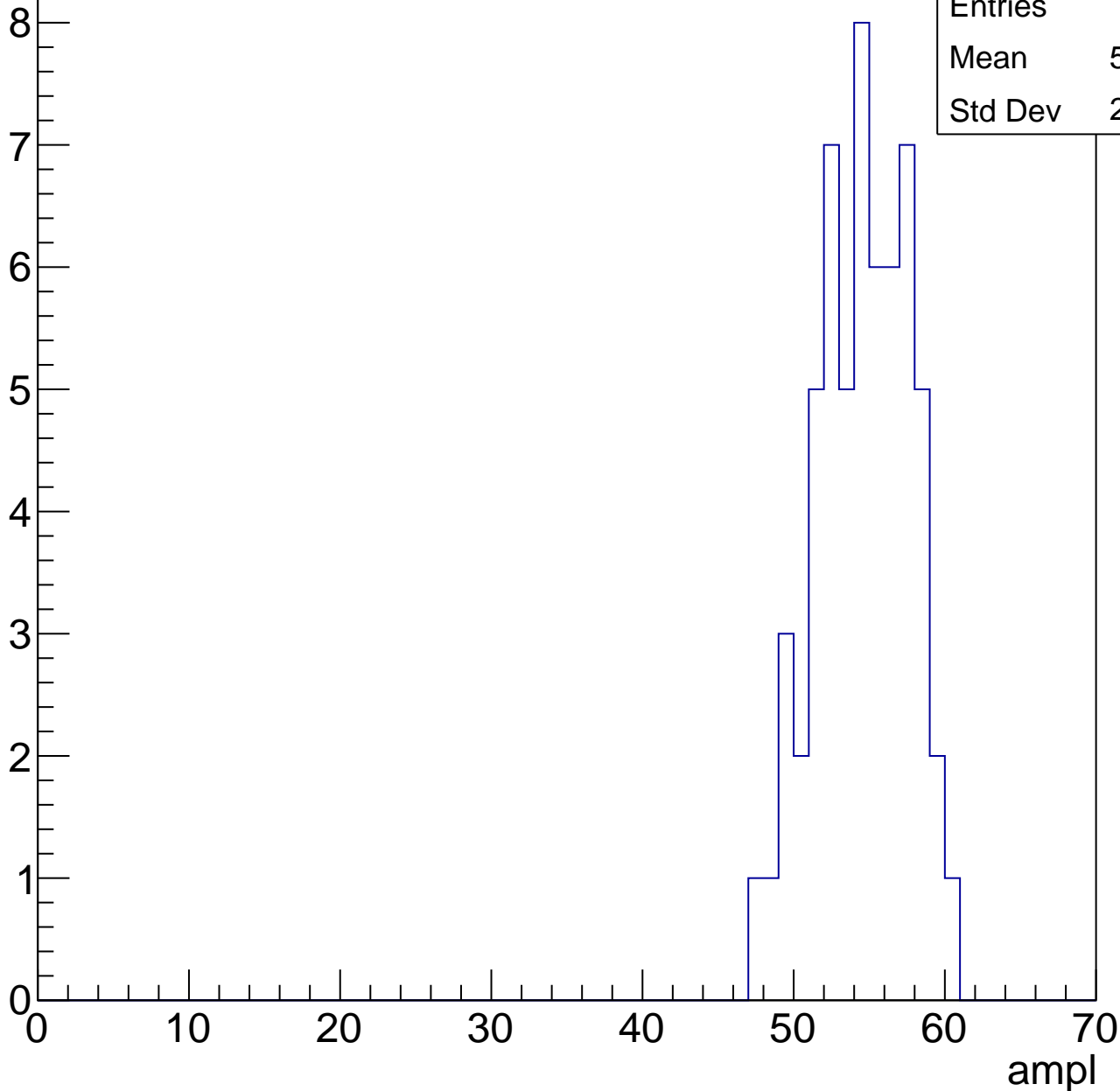


B1L103S, U7-ch110, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	54.08
Std Dev	2.993

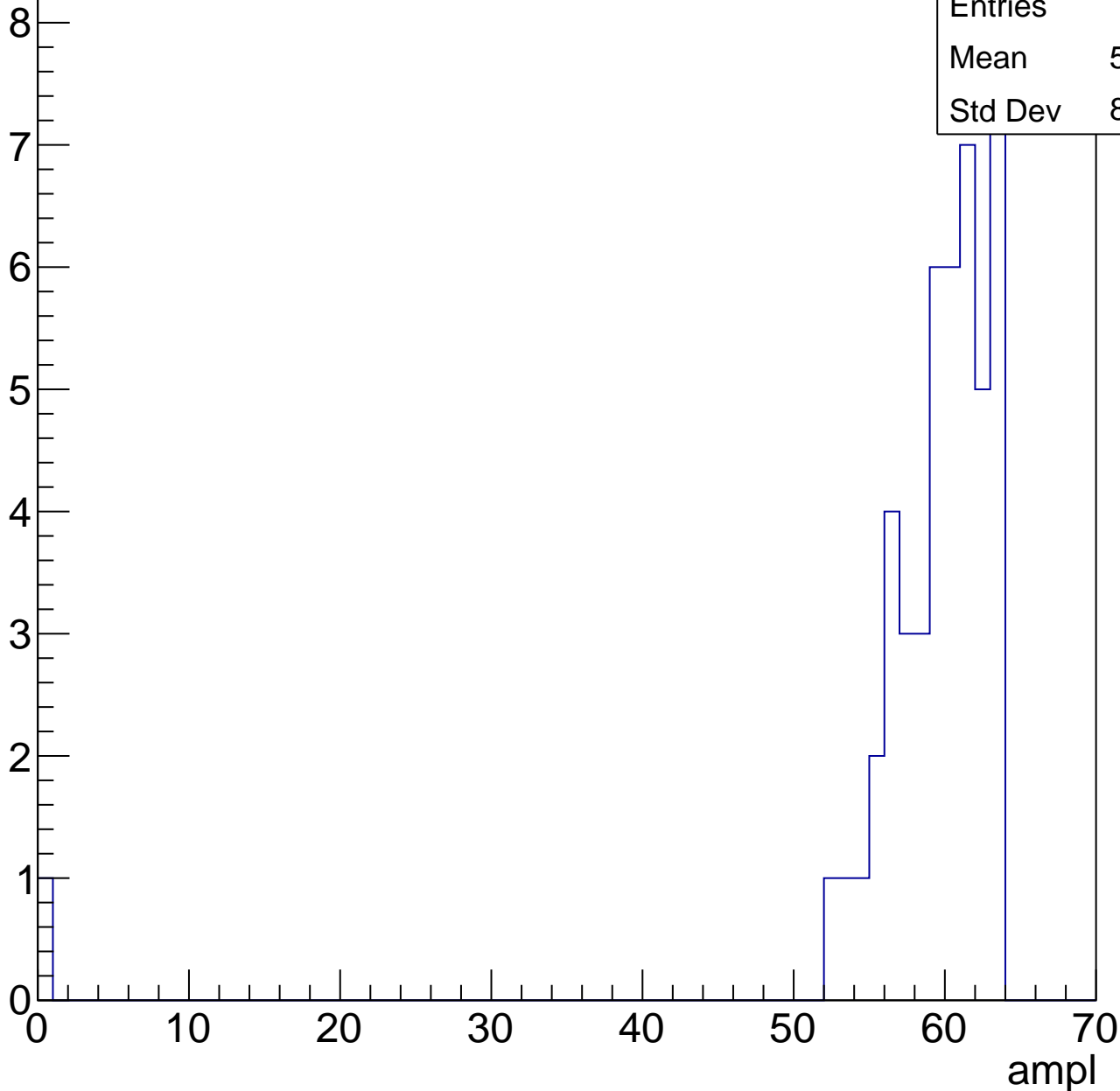


B1L103S, U7-ch110, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	48
Mean	58.19
Std Dev	8.955

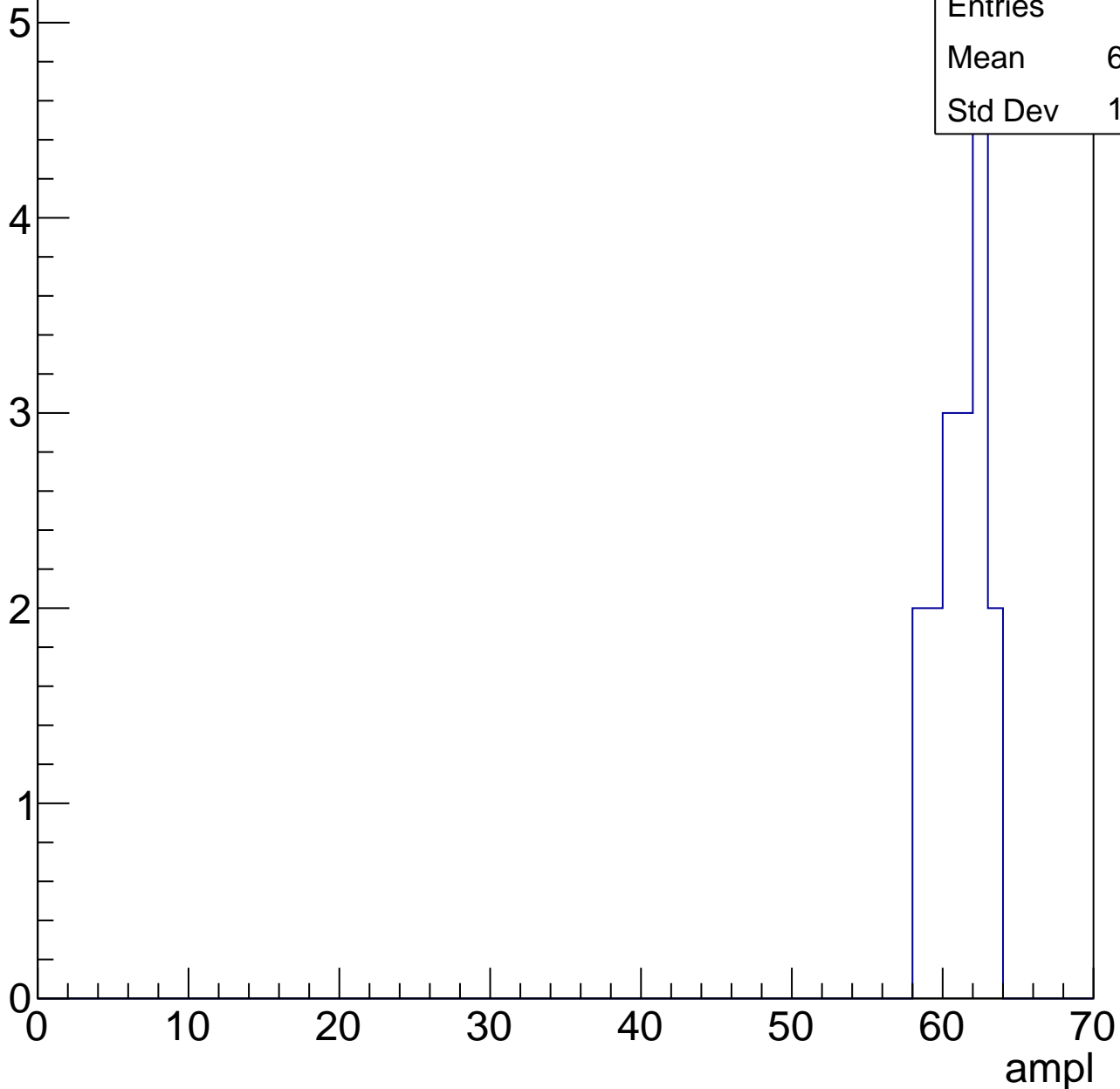


B1L103S, U7-ch110, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	17
Mean	60.76
Std Dev	1.554



B1L103S, U7-ch110, adc7

calib_packv5_041523_1651.root, FC#0, port C2

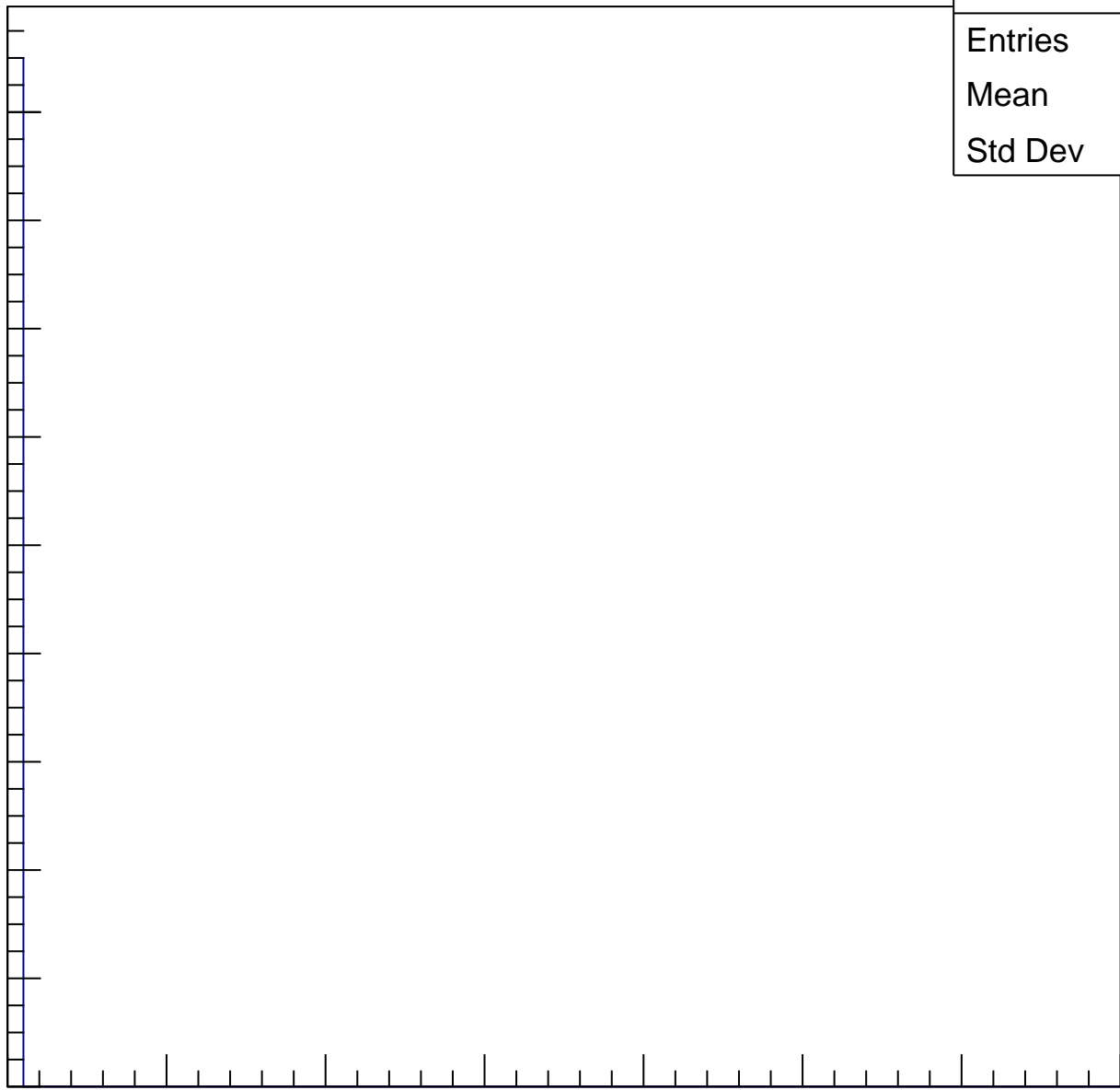
Entries	19
Mean	0
Std Dev	0

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl



B1L103S, U7-ch111, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	85
Mean	26.67
Std Dev	9.185

Gaus mean : 29.9797

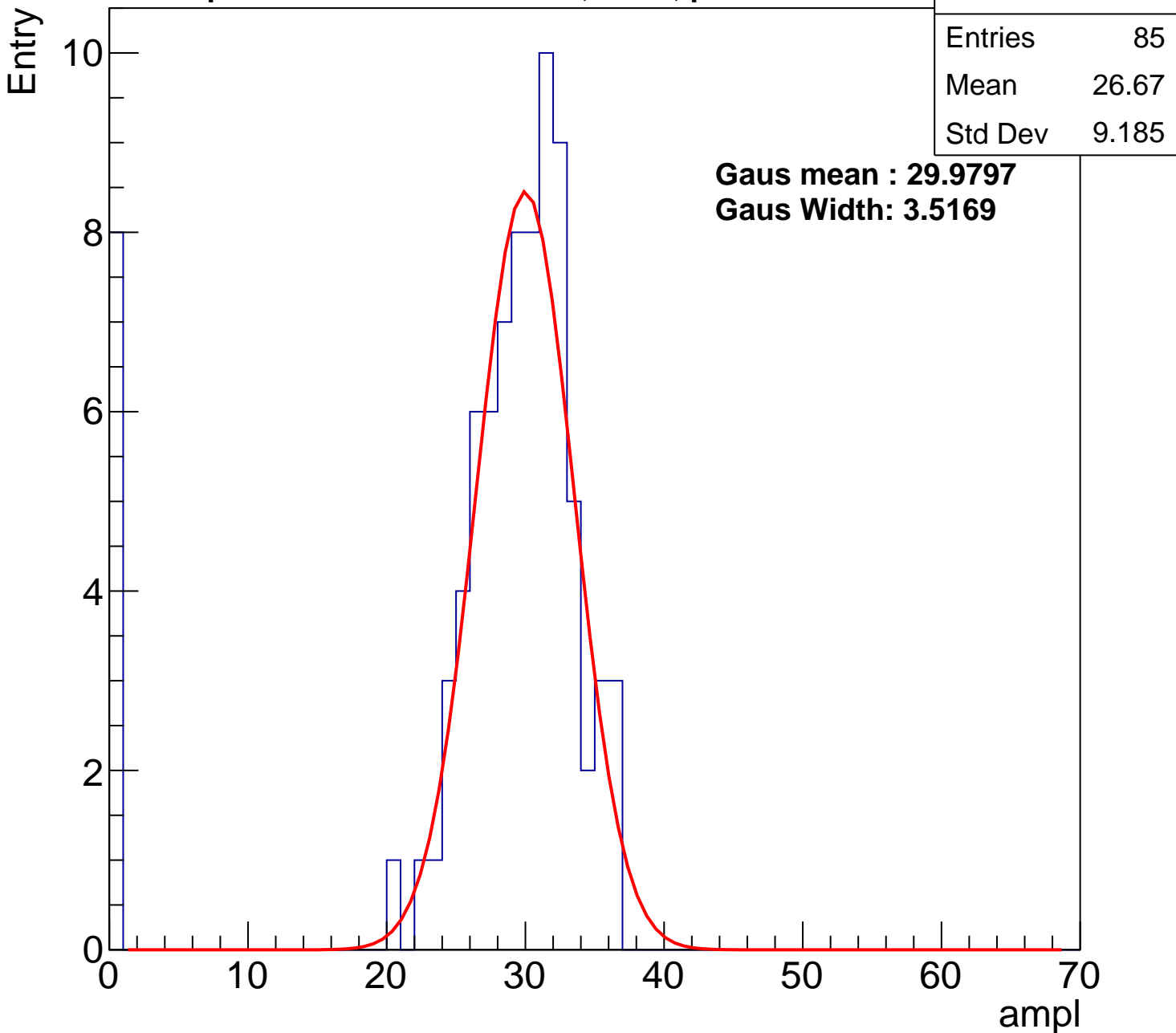
Gaus Width: 3.5169

Entry

10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U7-ch111, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	79
Mean	35.3
Std Dev	9.757

Gaus mean : 38.0996

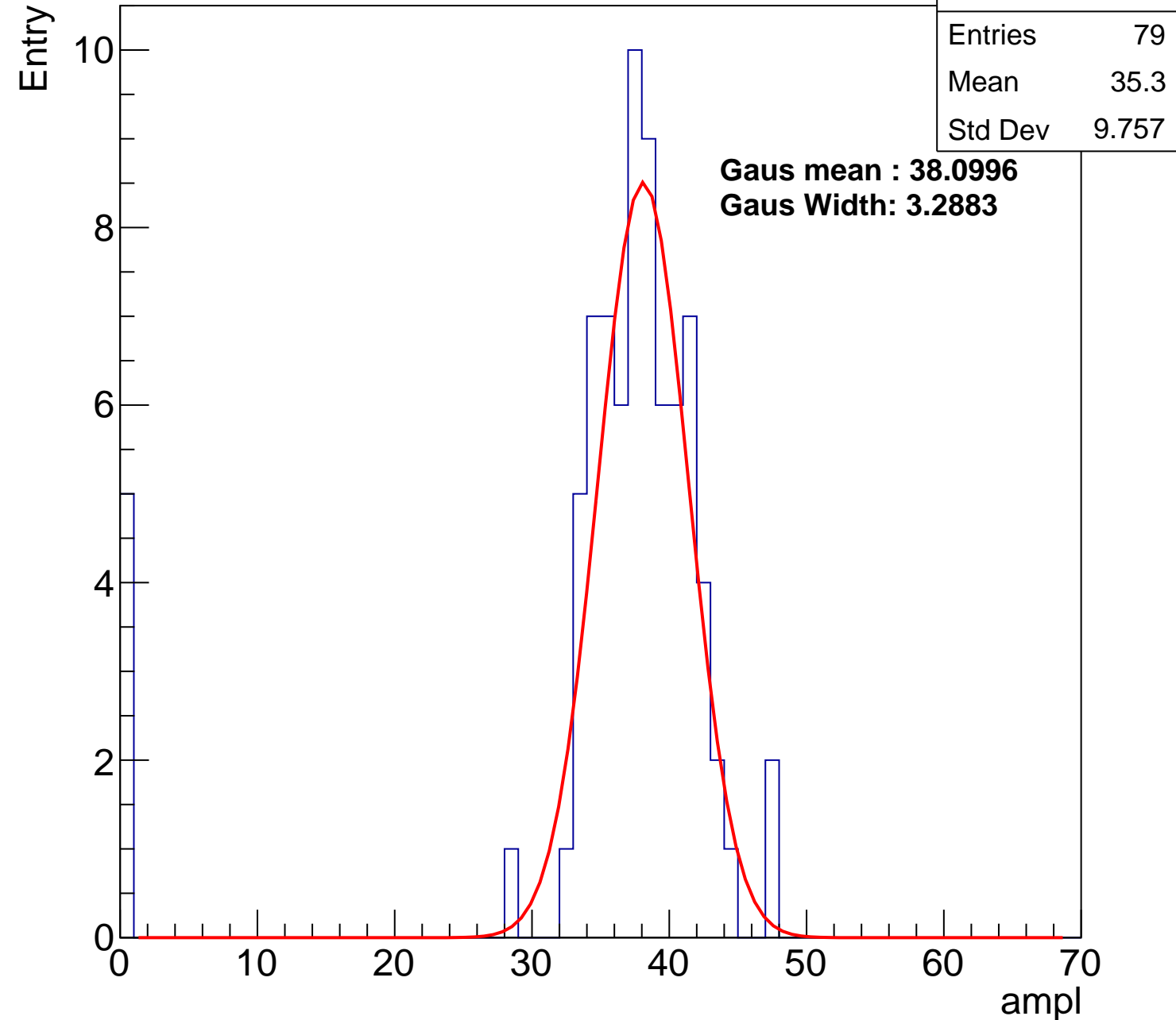
Gaus Width: 3.2883

Entry

10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U7-ch111, adc2

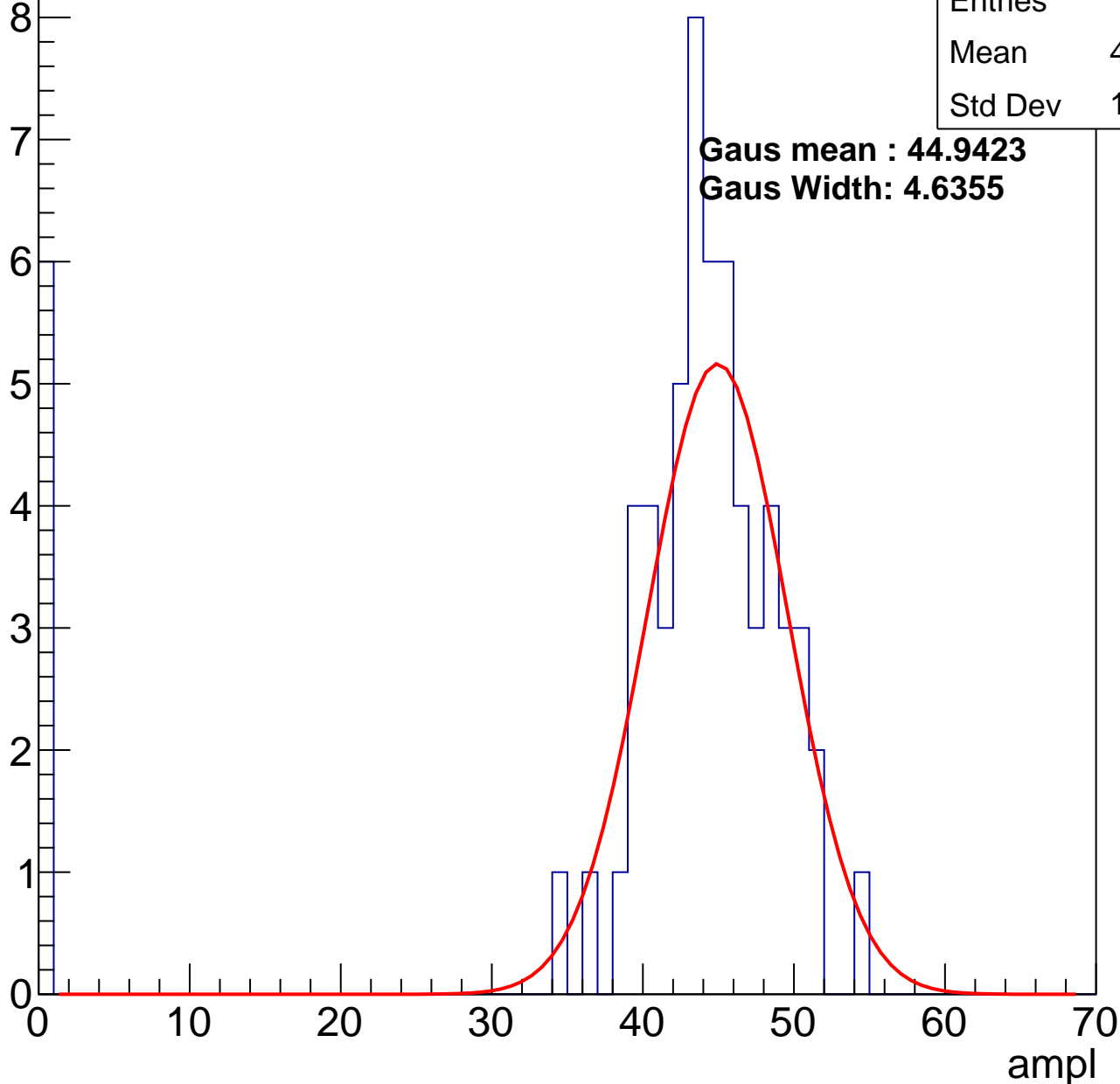
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	40.08
Std Dev	13.32

Gaus mean : 44.9423

Gaus Width: 4.6355

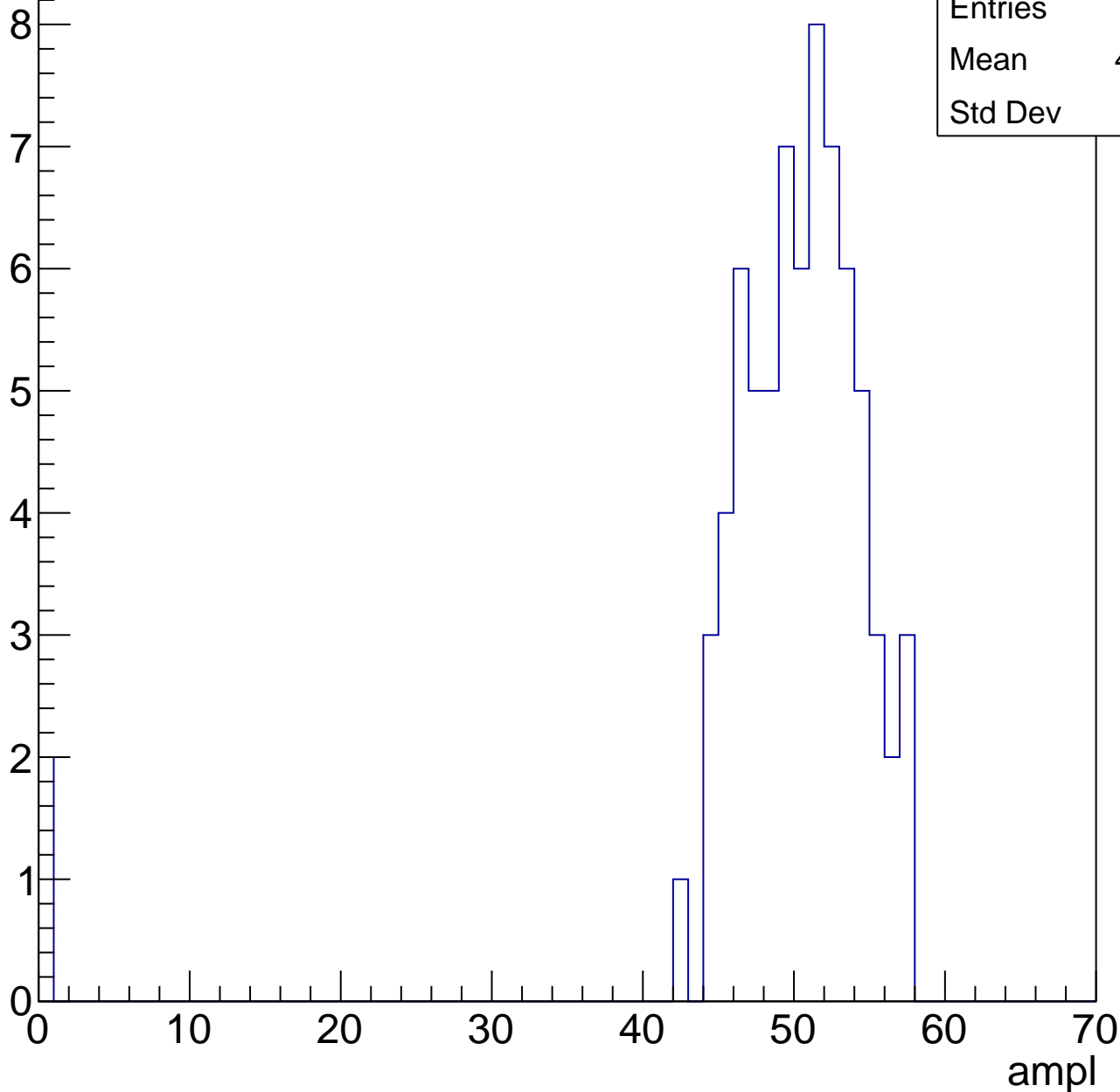


B1L103S, U7-ch111, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	73
Mean	48.71
Std Dev	8.9

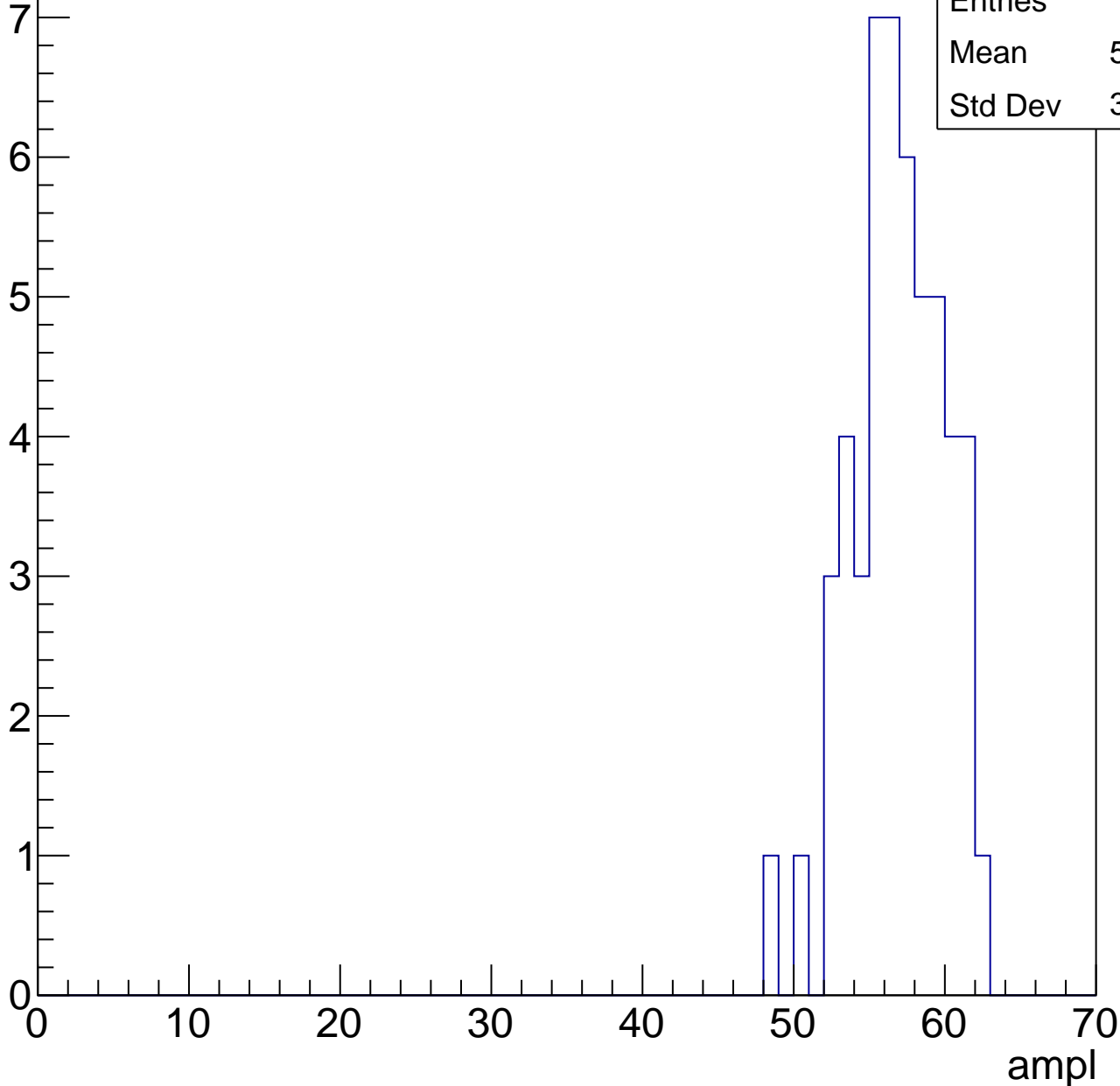


B1L103S, U7-ch111, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	51
Mean	56.43
Std Dev	3.018

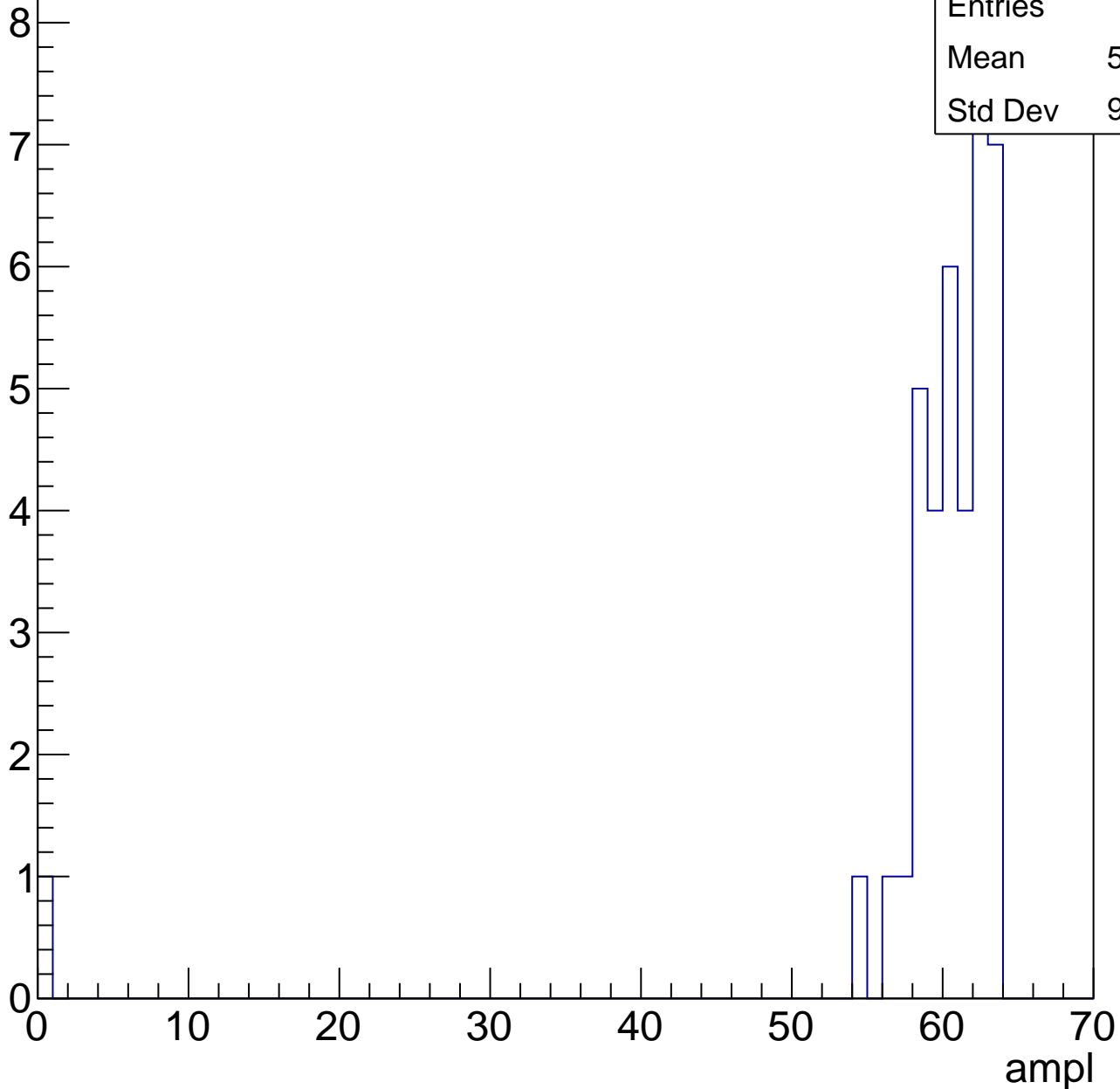


B1L103S, U7-ch111, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

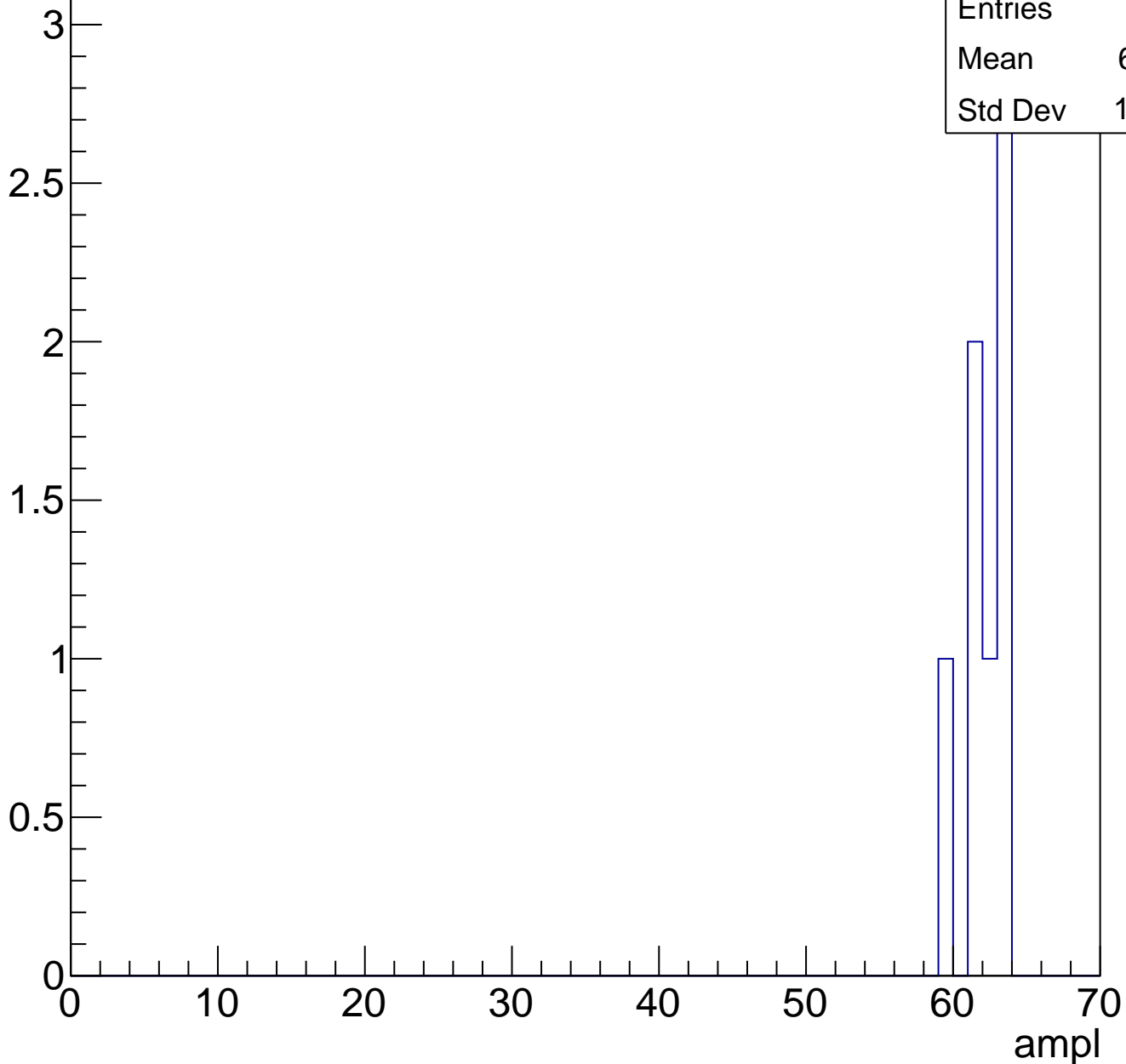
Entries	38
Mean	58.79
Std Dev	9.905



B1L103S, U7-ch111, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch111, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



Entries	18
Mean	0
Std Dev	0

B1L103S, U7-ch112, adc0

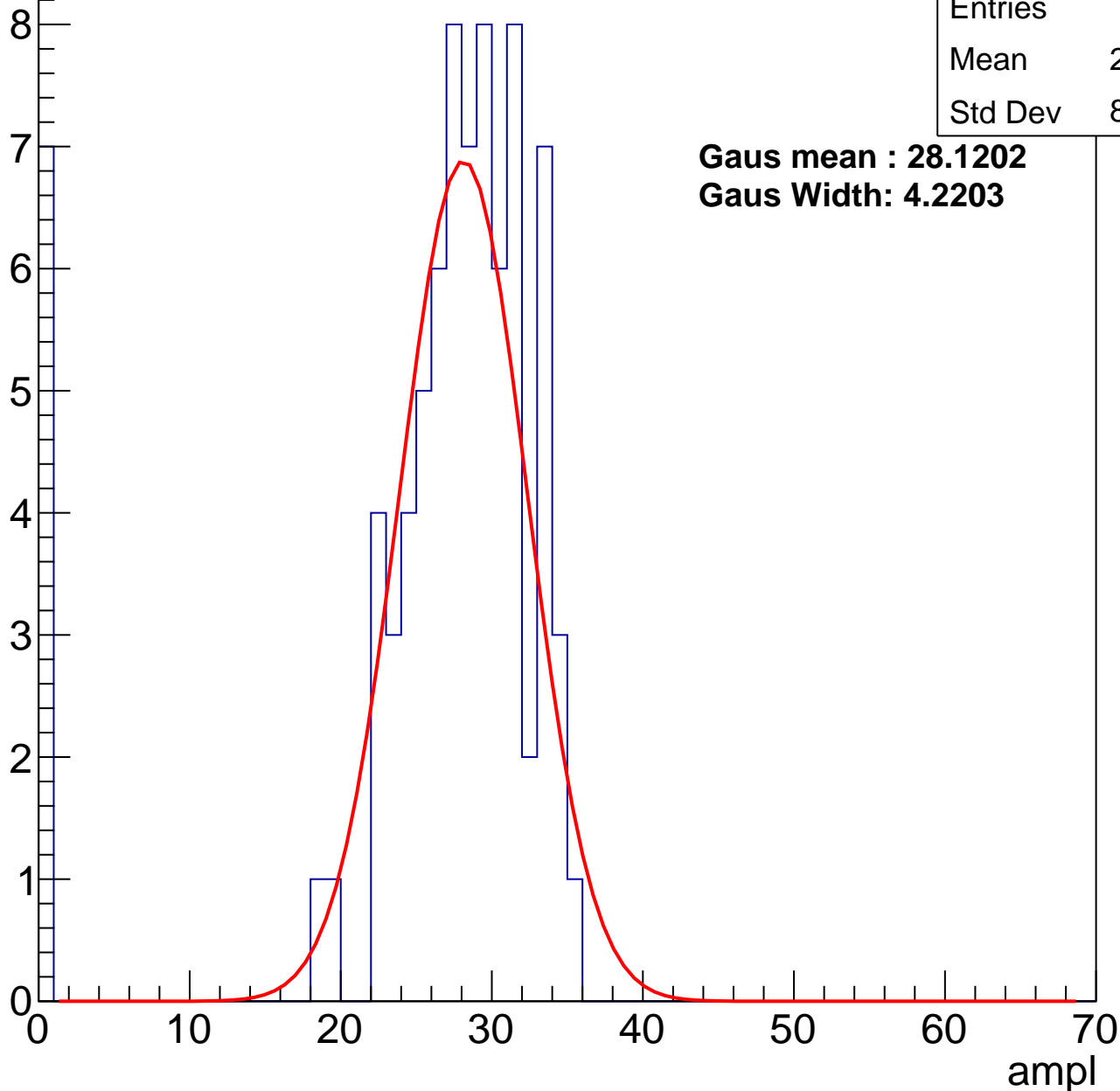
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	81
Mean	25.62
Std Dev	8.633

Gaus mean : 28.1202

Gaus Width: 4.2203



B1L103S, U7-ch112, adc1

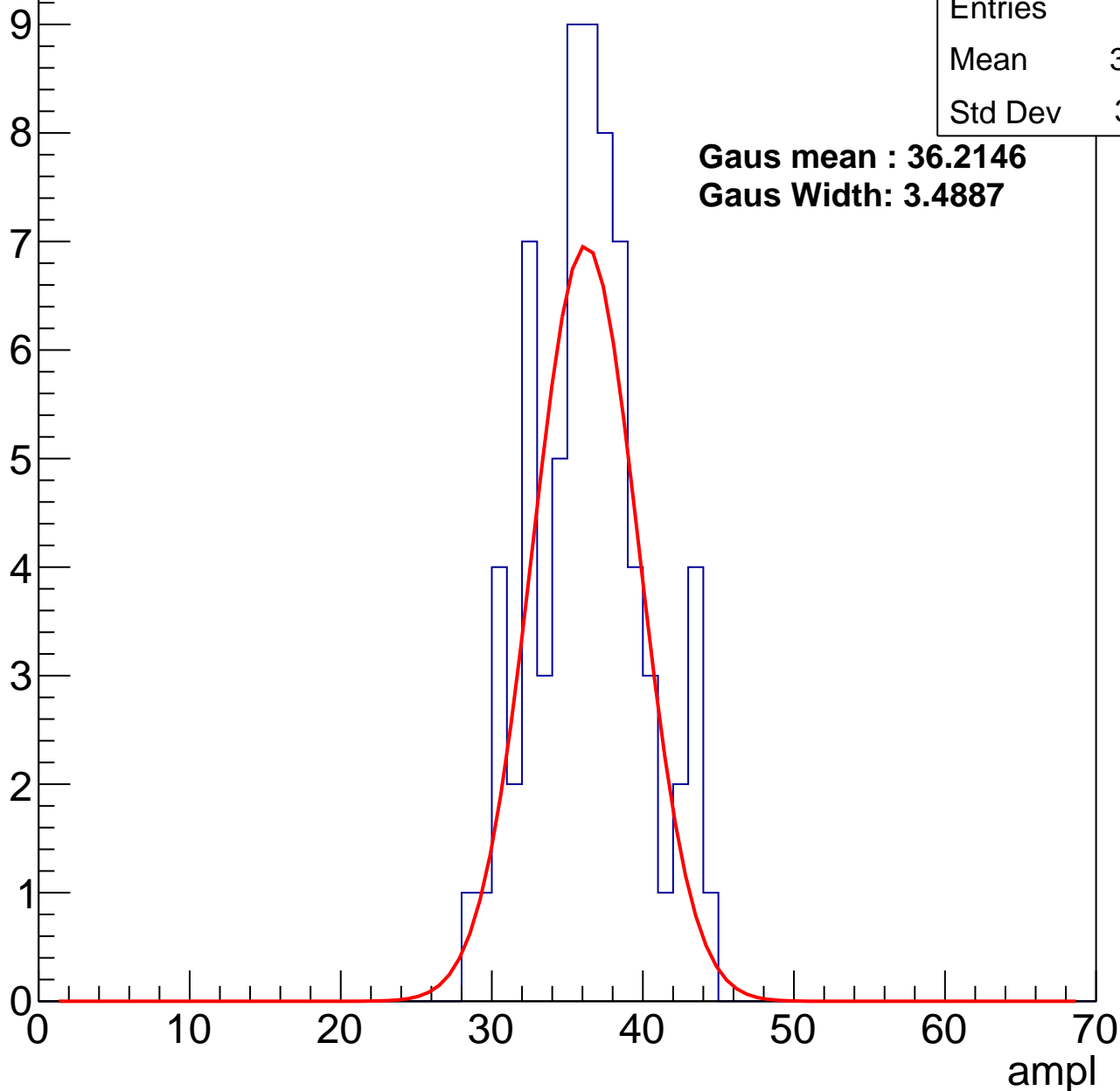
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	35.92
Std Dev	3.661

Gaus mean : 36.2146

Gaus Width: 3.4887



B1L103S, U7-ch112, adc2

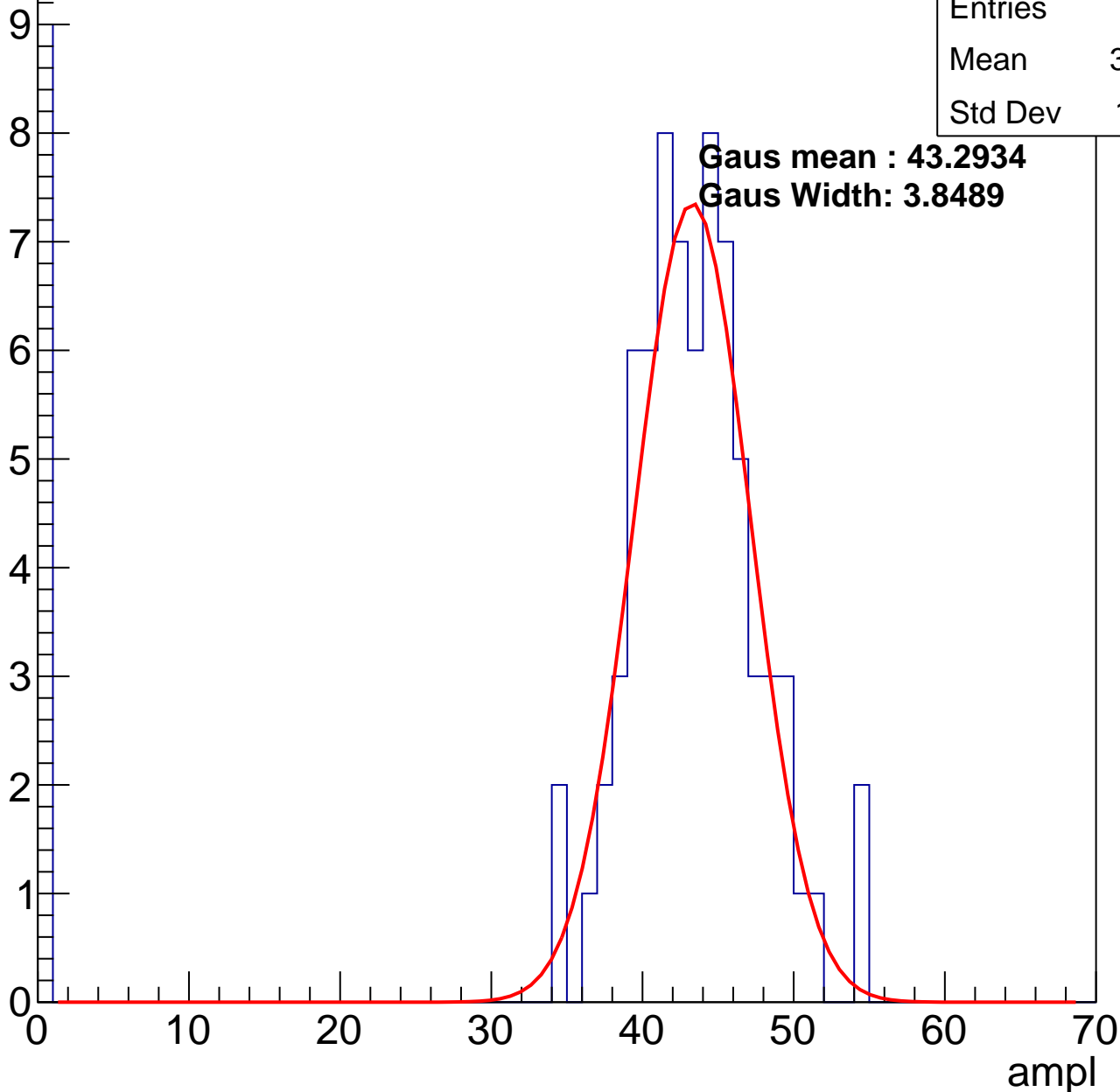
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	83
Mean	38.36
Std Dev	13.91

Gaus mean : 43.2934

Gaus Width: 3.8489

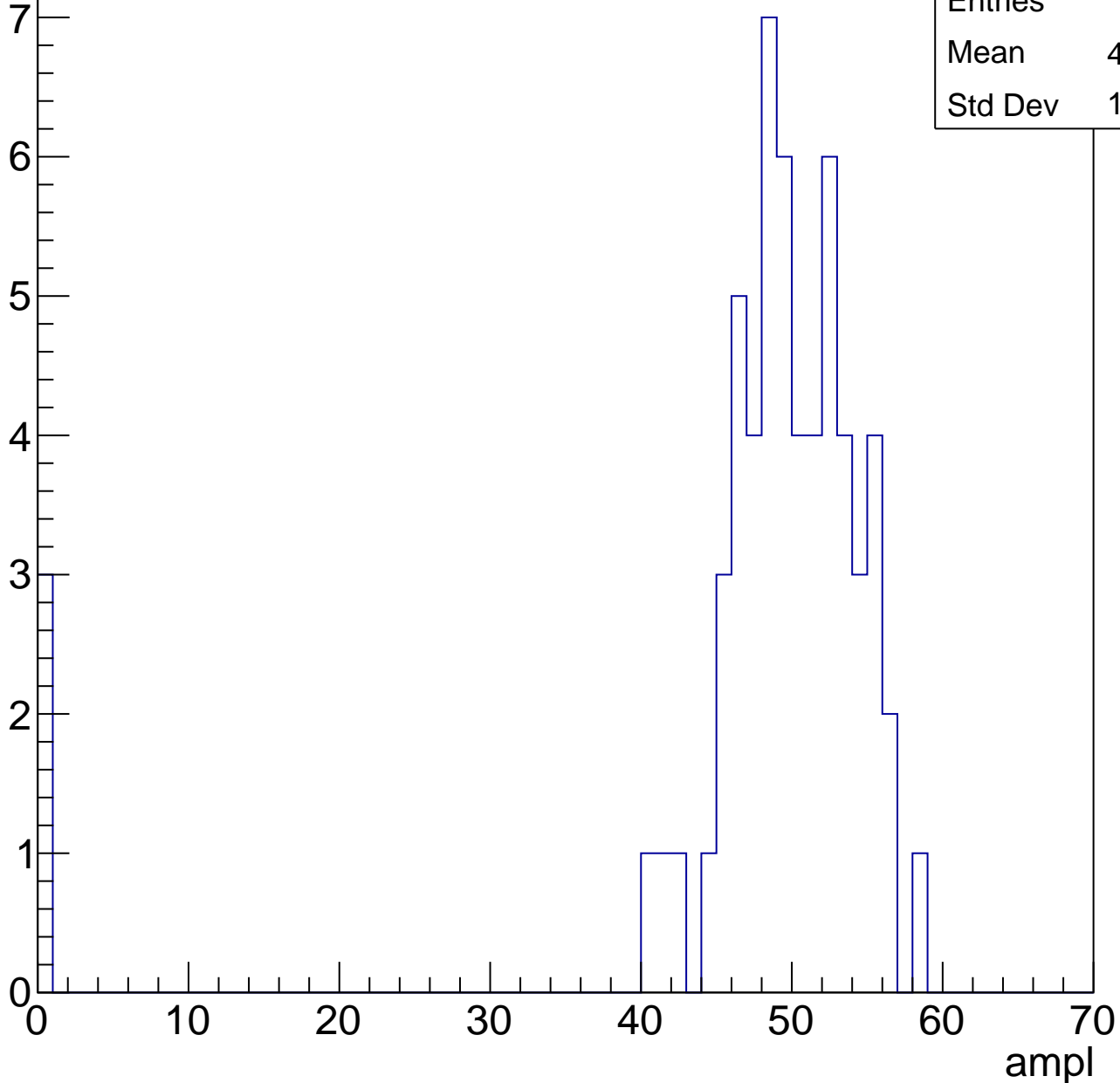


B1L103S, U7-ch112, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	47.17
Std Dev	11.45

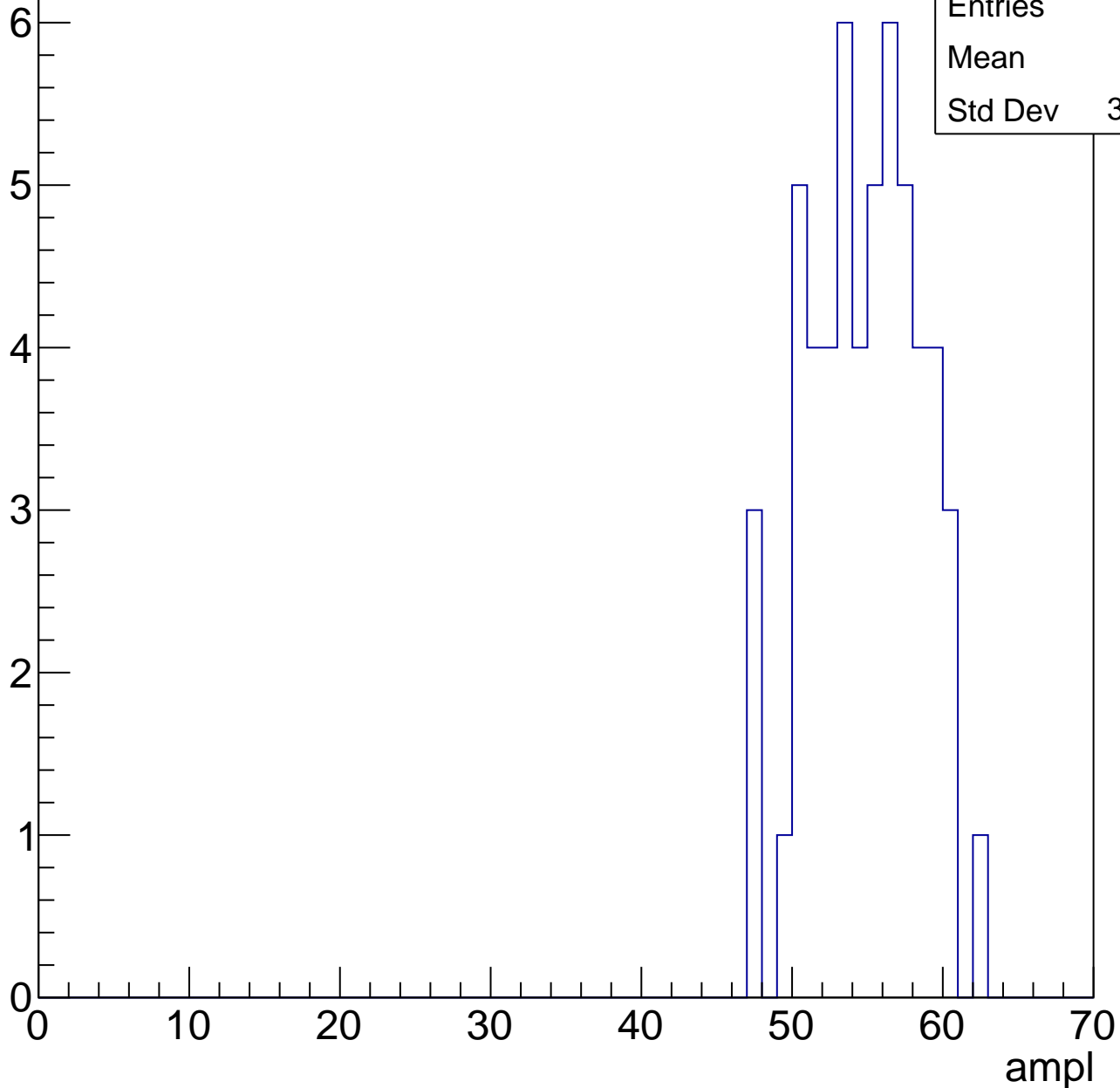


B1L103S, U7-ch112, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	54.4
Std Dev	3.596

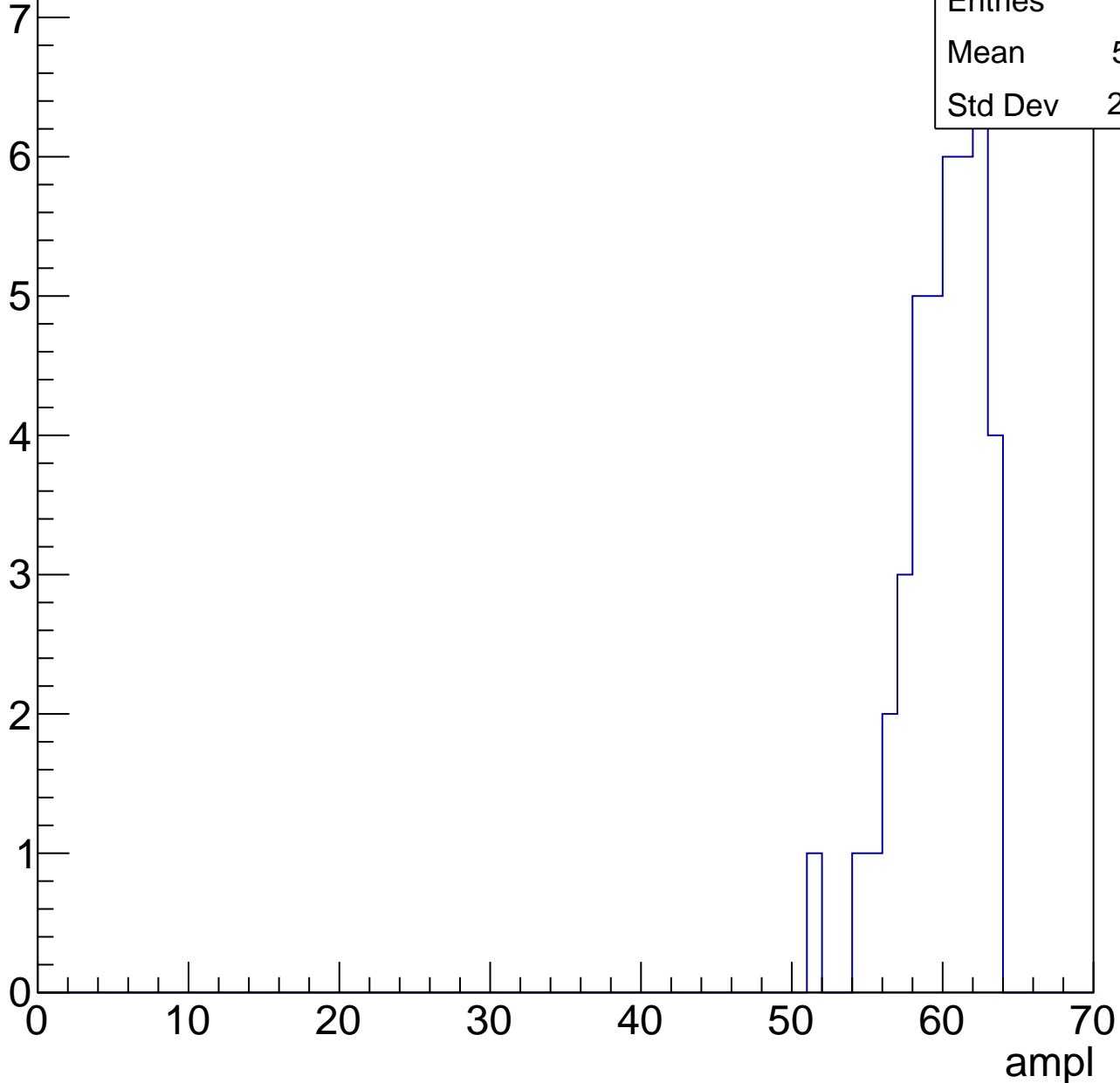


B1L103S, U7-ch112, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	41
Mean	59.51
Std Dev	2.642

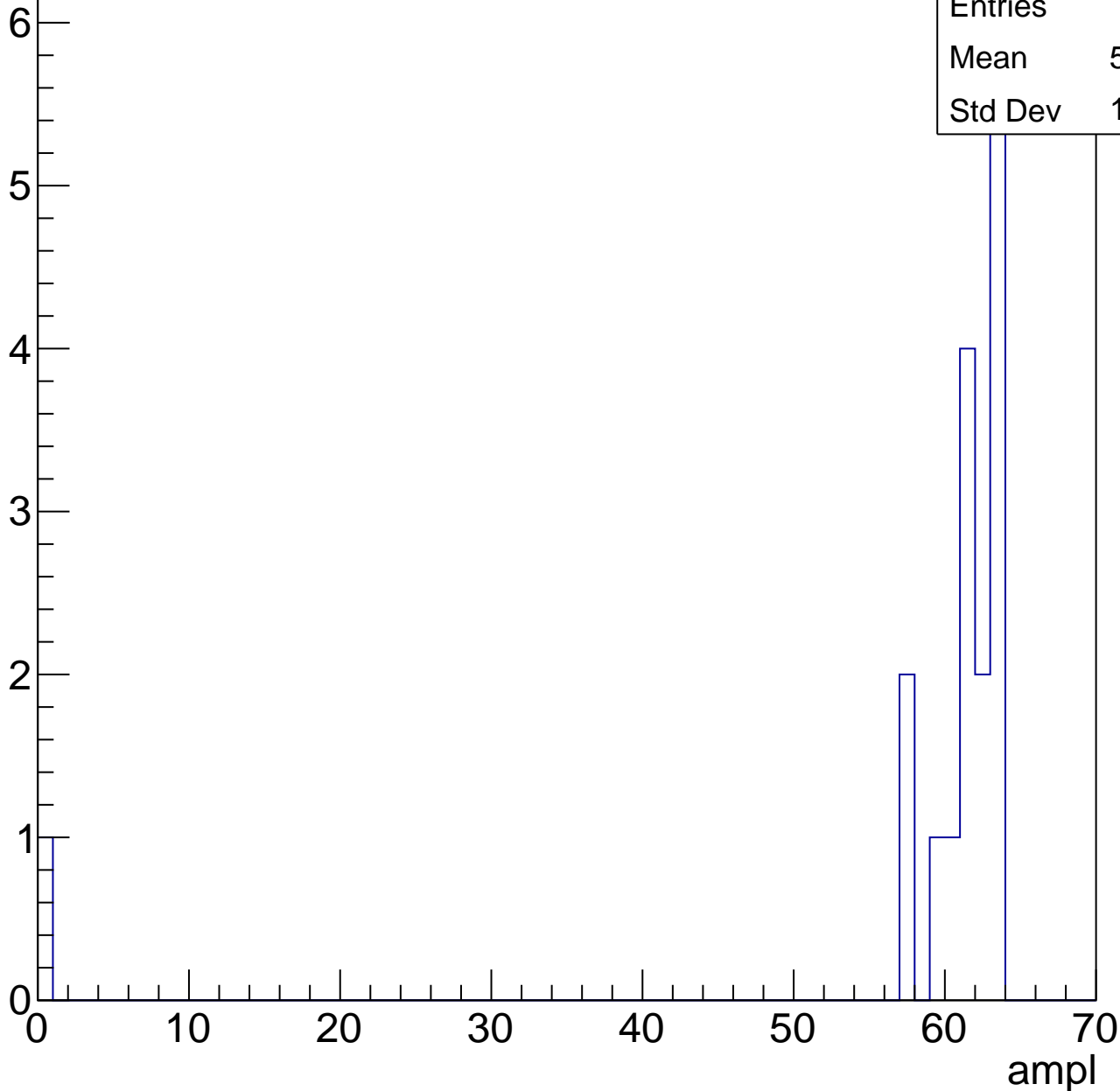


B1L103S, U7-ch112, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	17
Mean	57.59
Std Dev	14.52



B1L103S, U7-ch112, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U7-ch113, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	97
Mean	22.57
Std Dev	11.34

Gaus mean : 27.9936

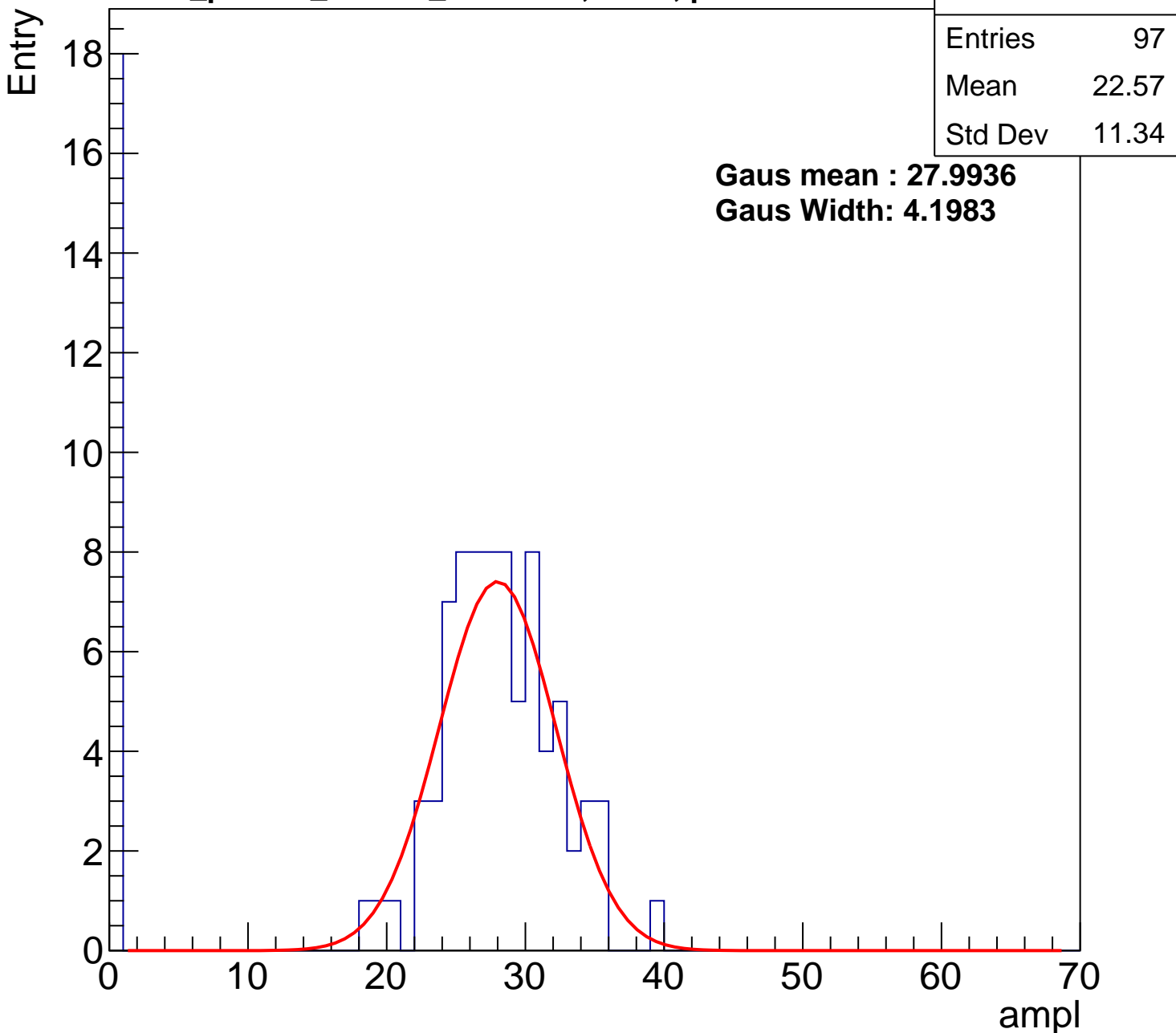
Gaus Width: 4.1983

Entry

18
16
14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U7-ch113, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	28.9
Std Dev	13.02

Gaus mean : 34.9997

Gaus Width: 3.6091

Entry

12

10

8

6

4

2

0

0

10

20

30

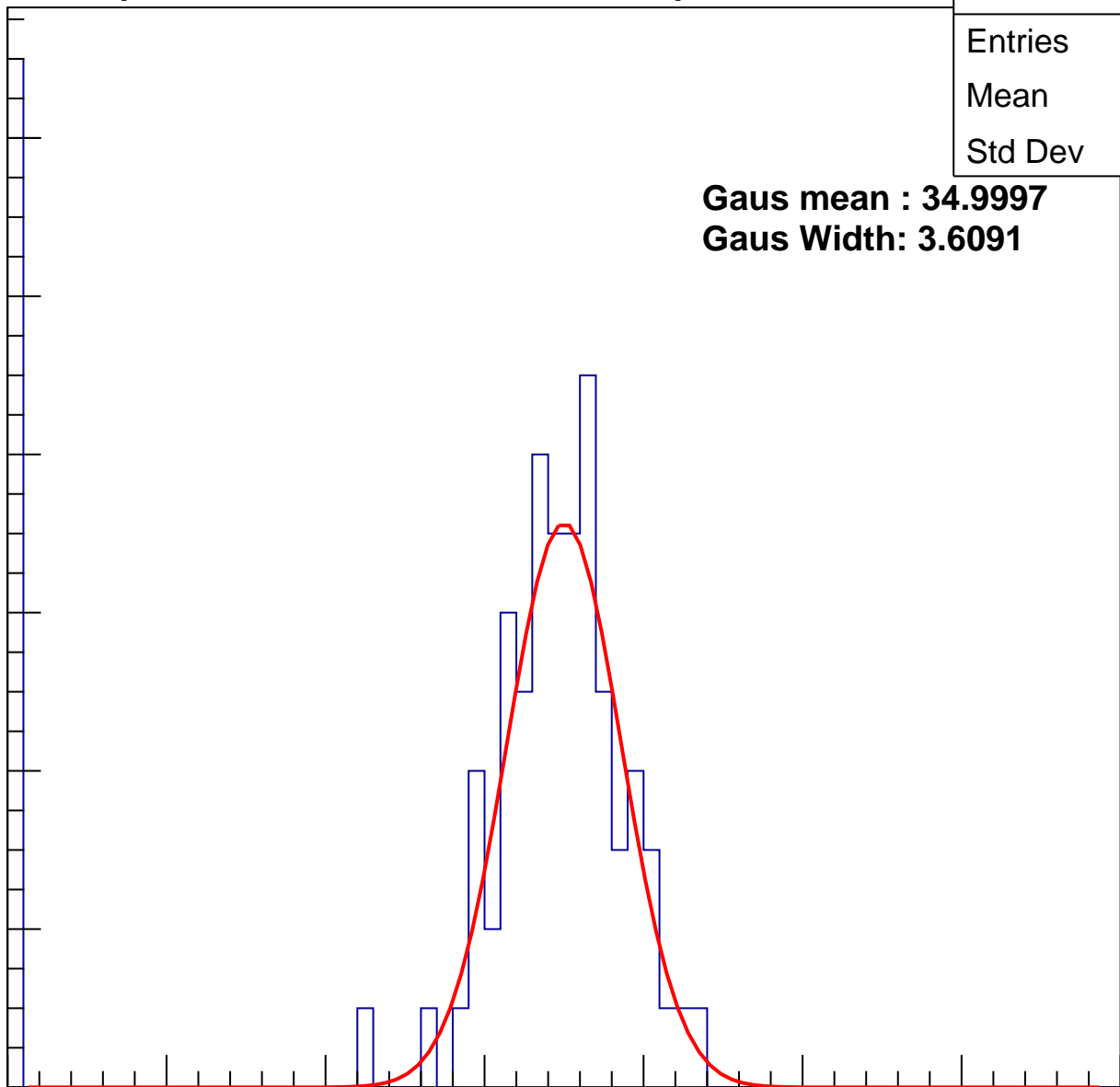
40

50

60

70

ampl



B1L103S, U7-ch113, adc2

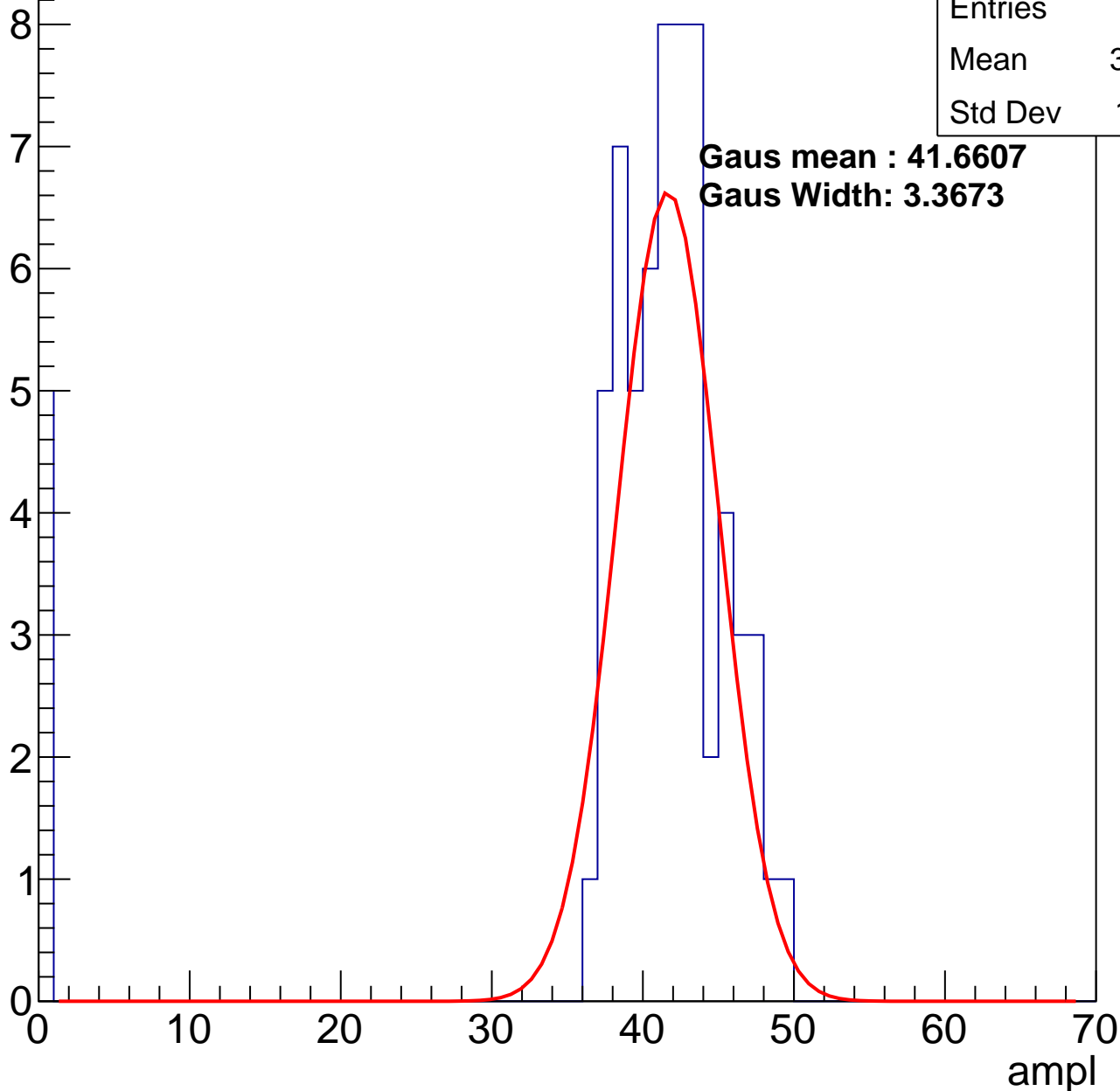
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	38.42
Std Dev	11.31

Gaus mean : 41.6607

Gaus Width: 3.3673

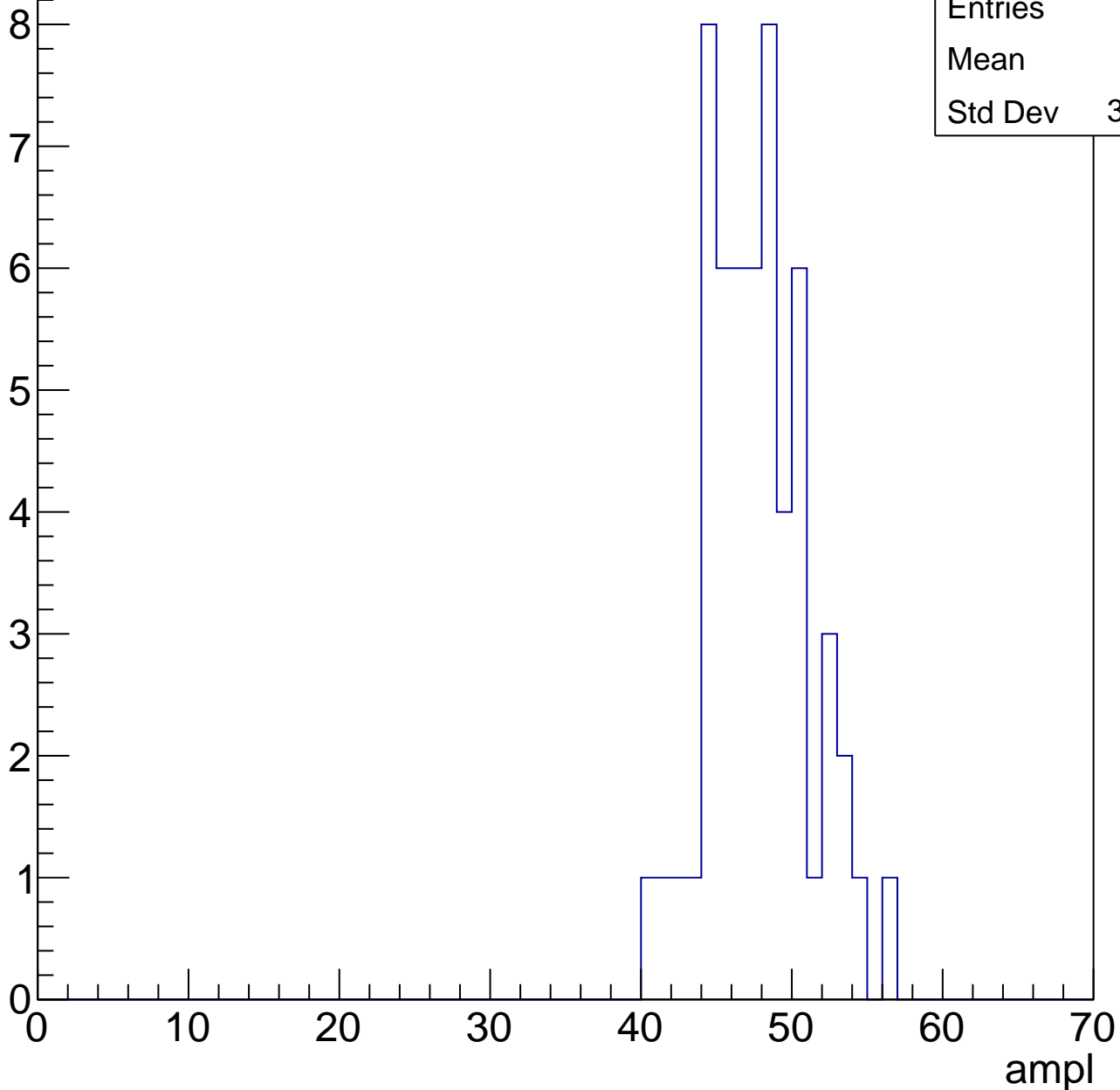


B1L103S, U7-ch113, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	47.3
Std Dev	3.256

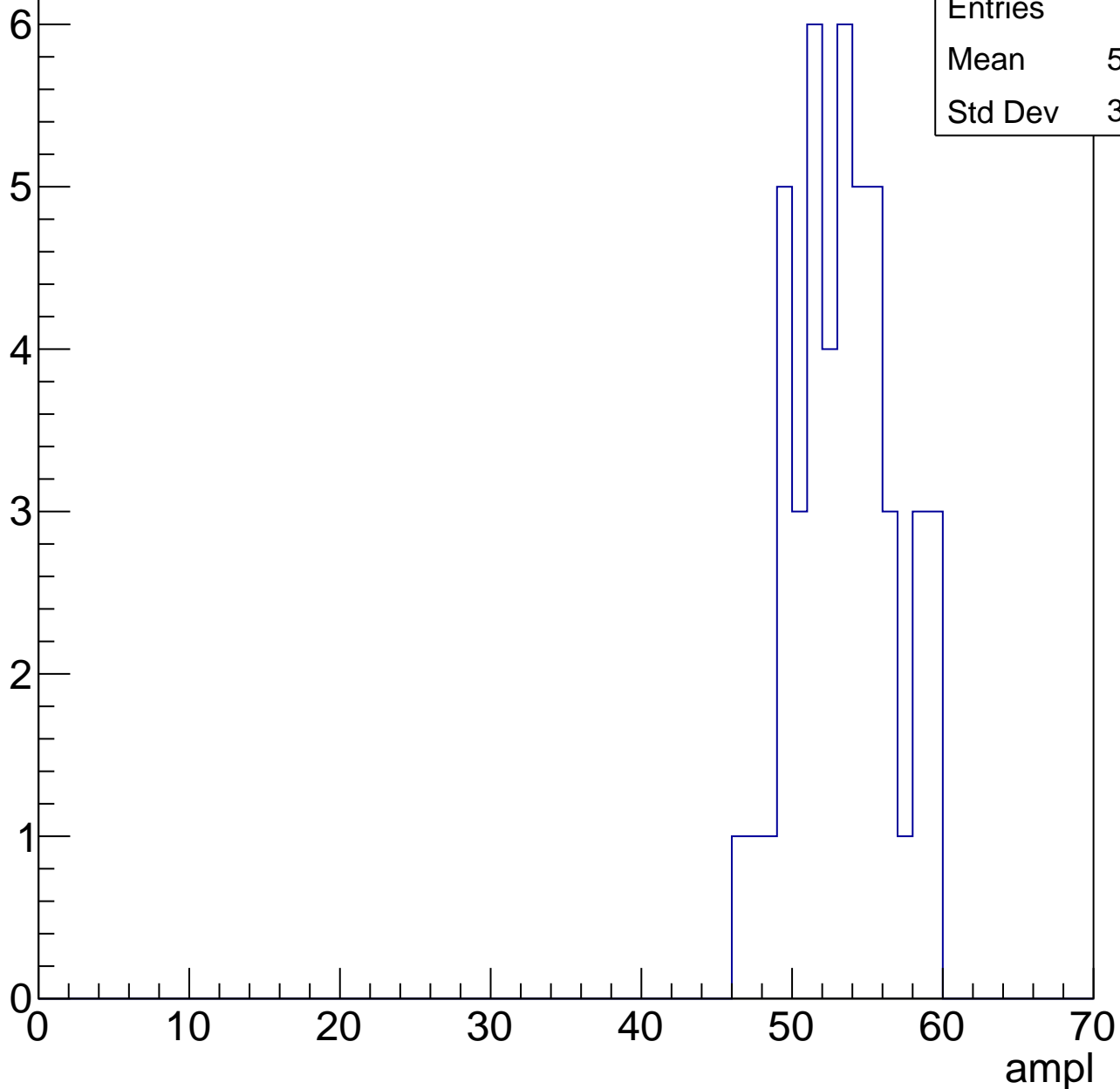


B1L103S, U7-ch113, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	47
Mean	52.96
Std Dev	3.248

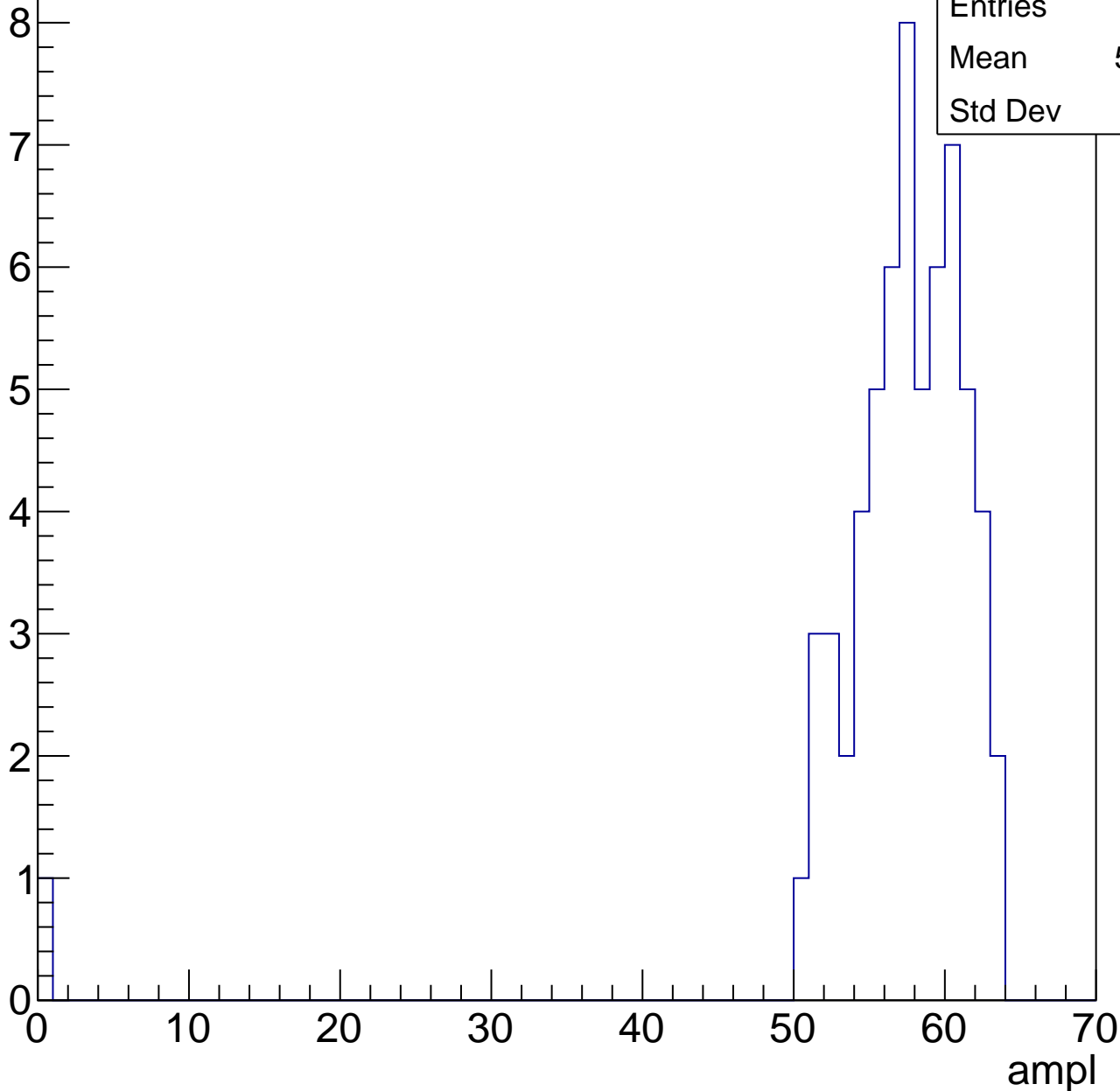


B1L103S, U7-ch113, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	56.31
Std Dev	7.92

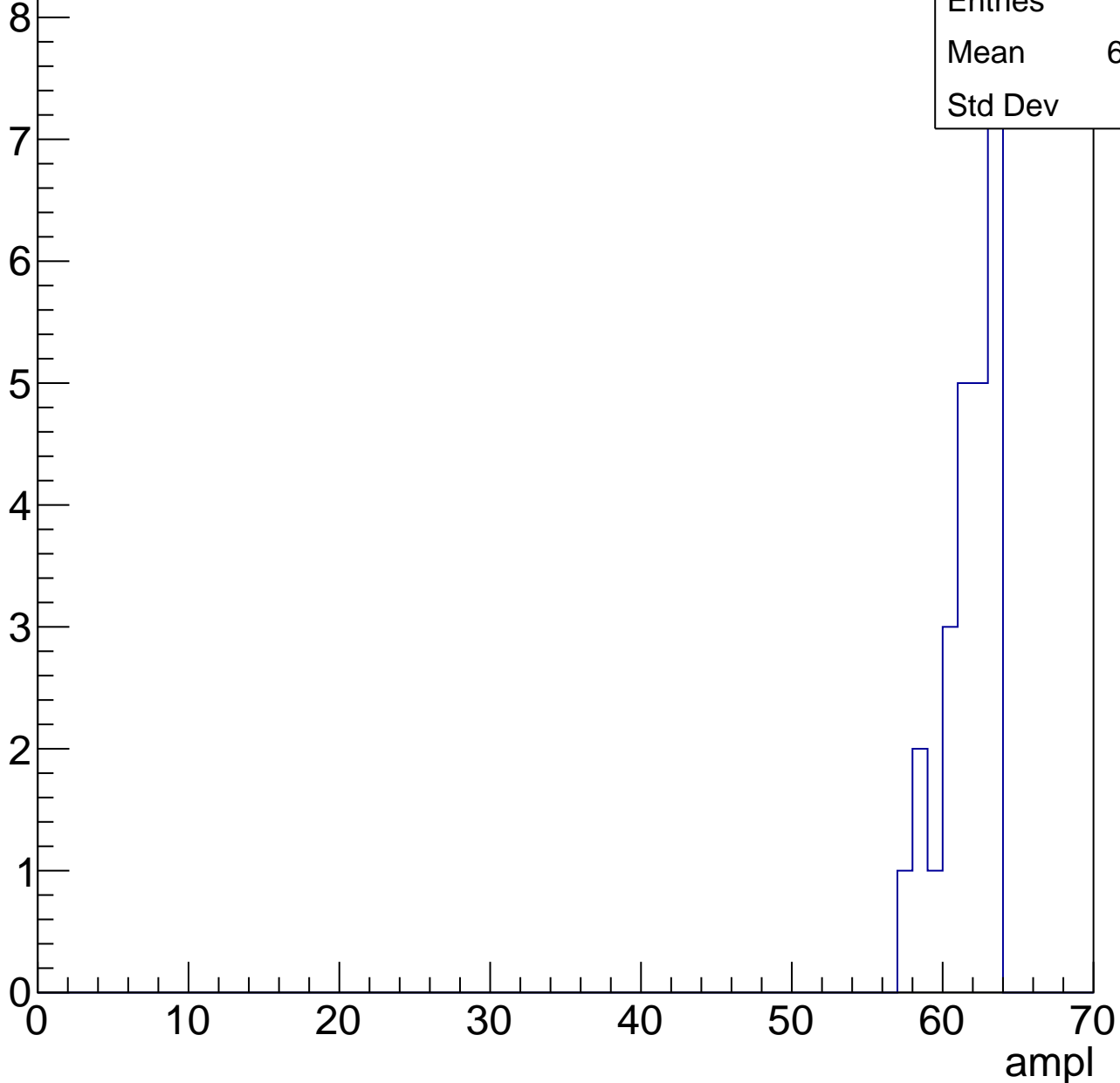


B1L103S, U7-ch113, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	25
Mean	61.24
Std Dev	1.75



B1L103S, U7-ch113, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.1
Std Dev	13.51

Entry



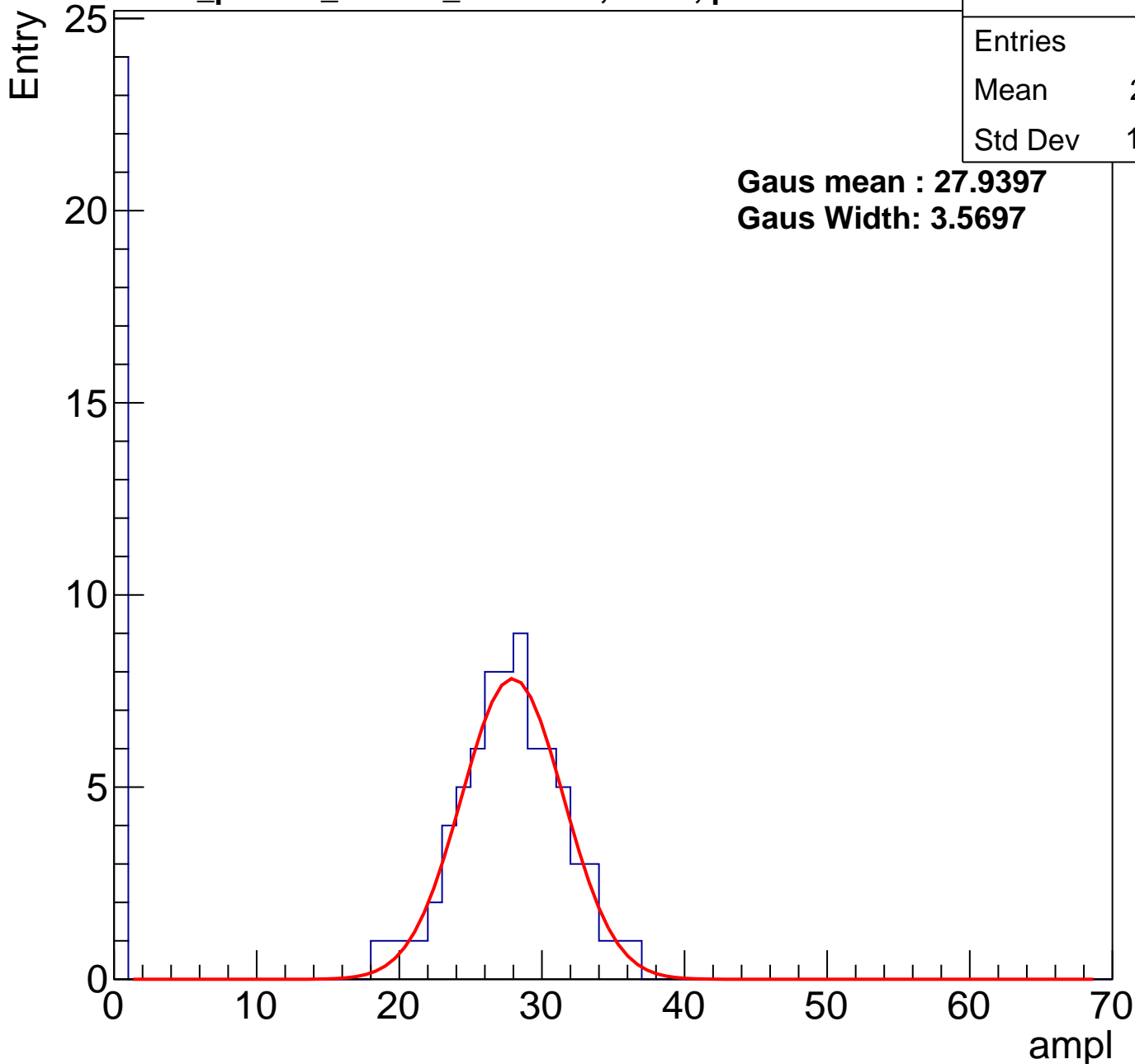
B1L103S, U7-ch114, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	96
Mean	20.51
Std Dev	12.26

Gaus mean : 27.9397

Gaus Width: 3.5697



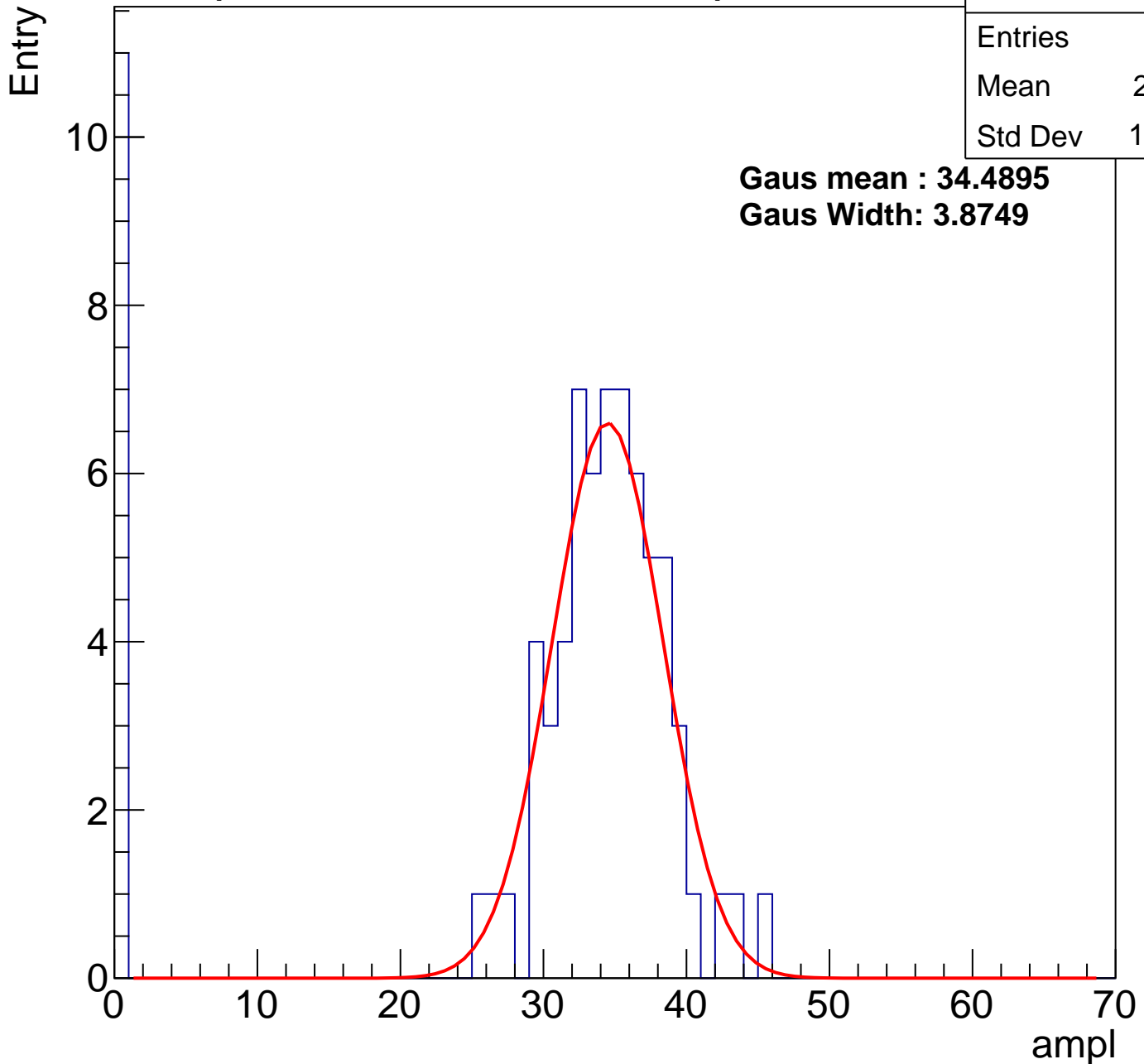
B1L103S, U7-ch114, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	29.21
Std Dev	12.62

Gaus mean : 34.4895

Gaus Width: 3.8749



B1L103S, U7-ch114, adc2

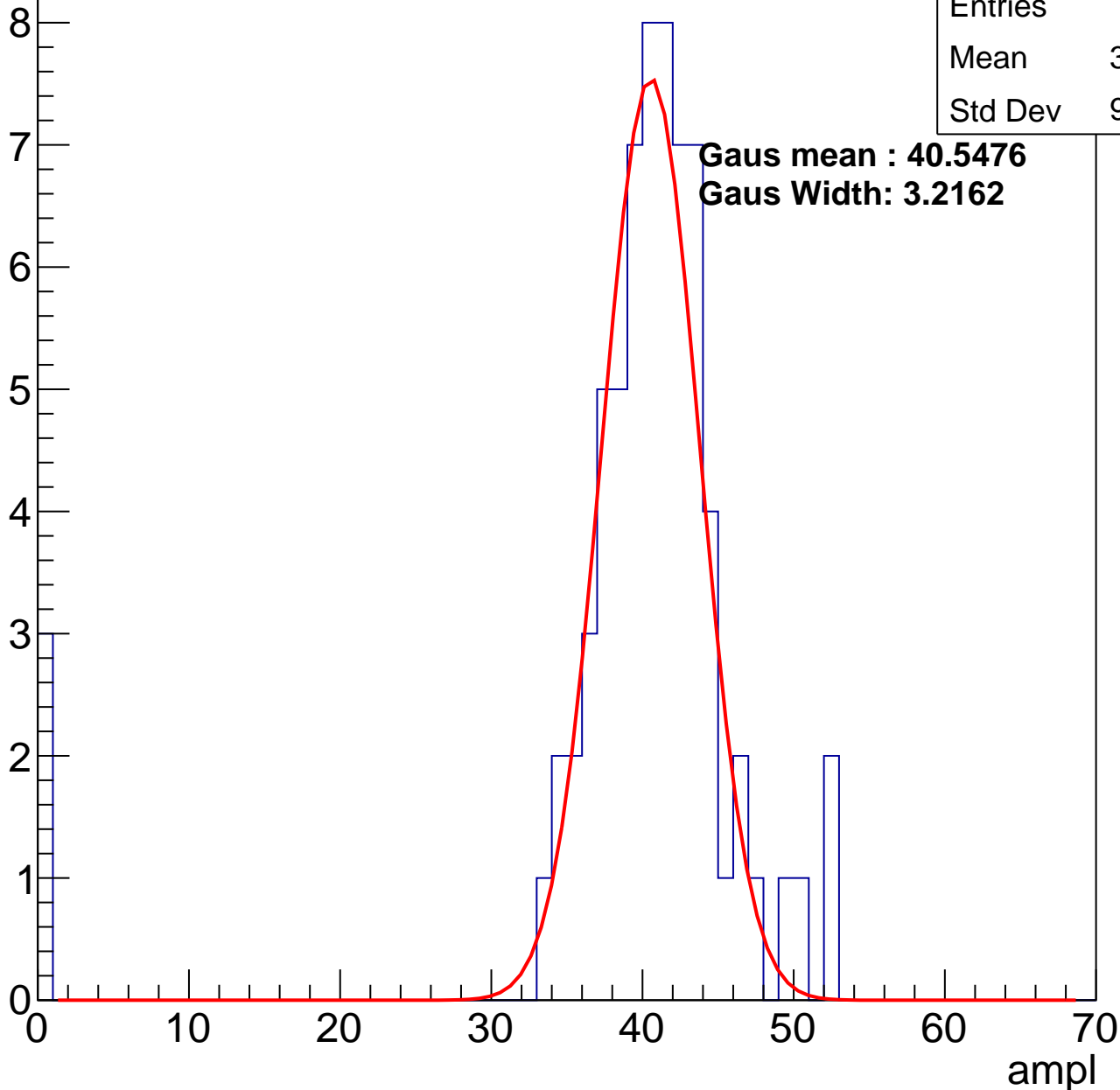
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	39.04
Std Dev	9.106

Gaus mean : 40.5476

Gaus Width: 3.2162

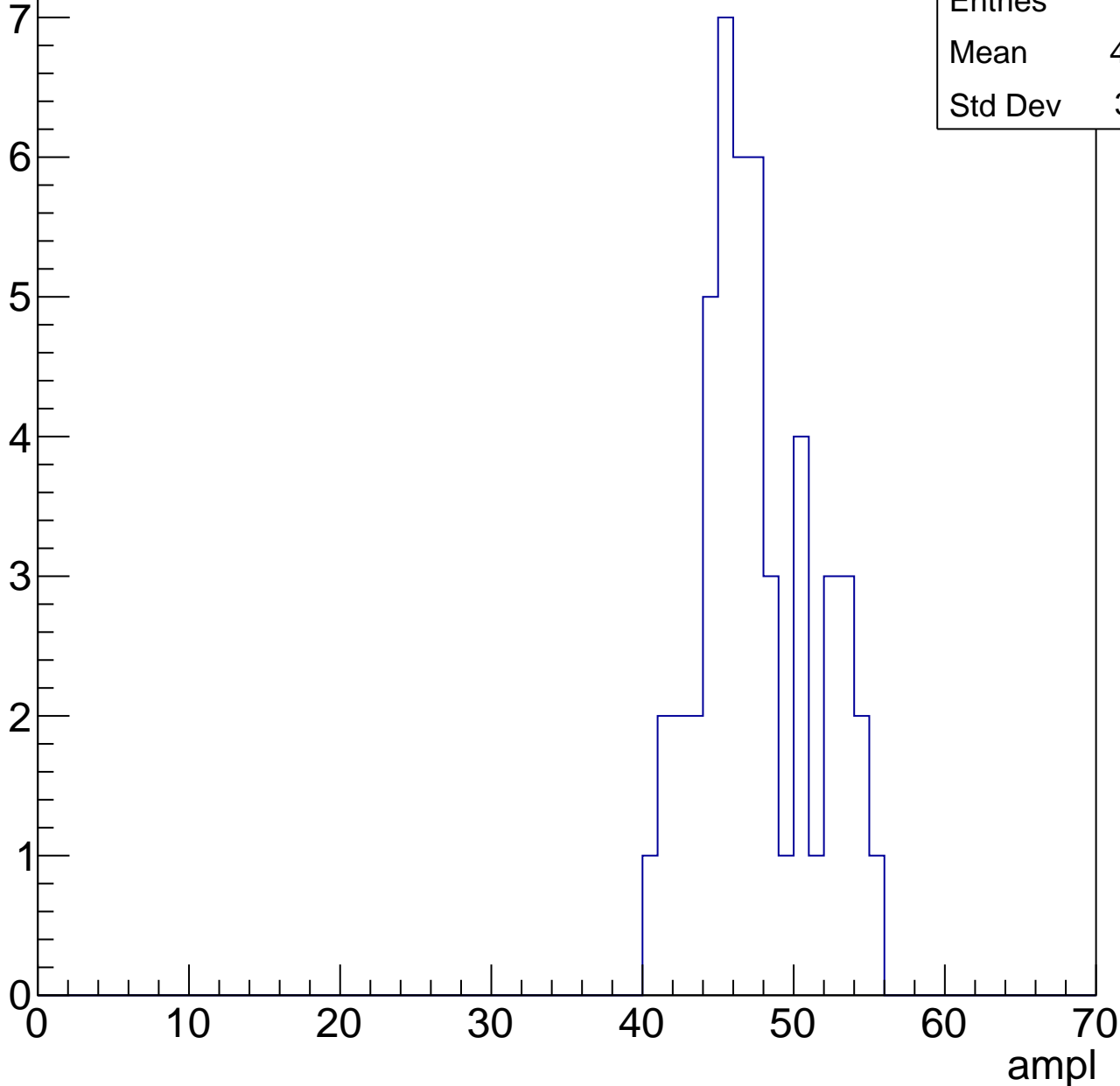


B1L103S, U7-ch114, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	49
Mean	47.08
Std Dev	3.741

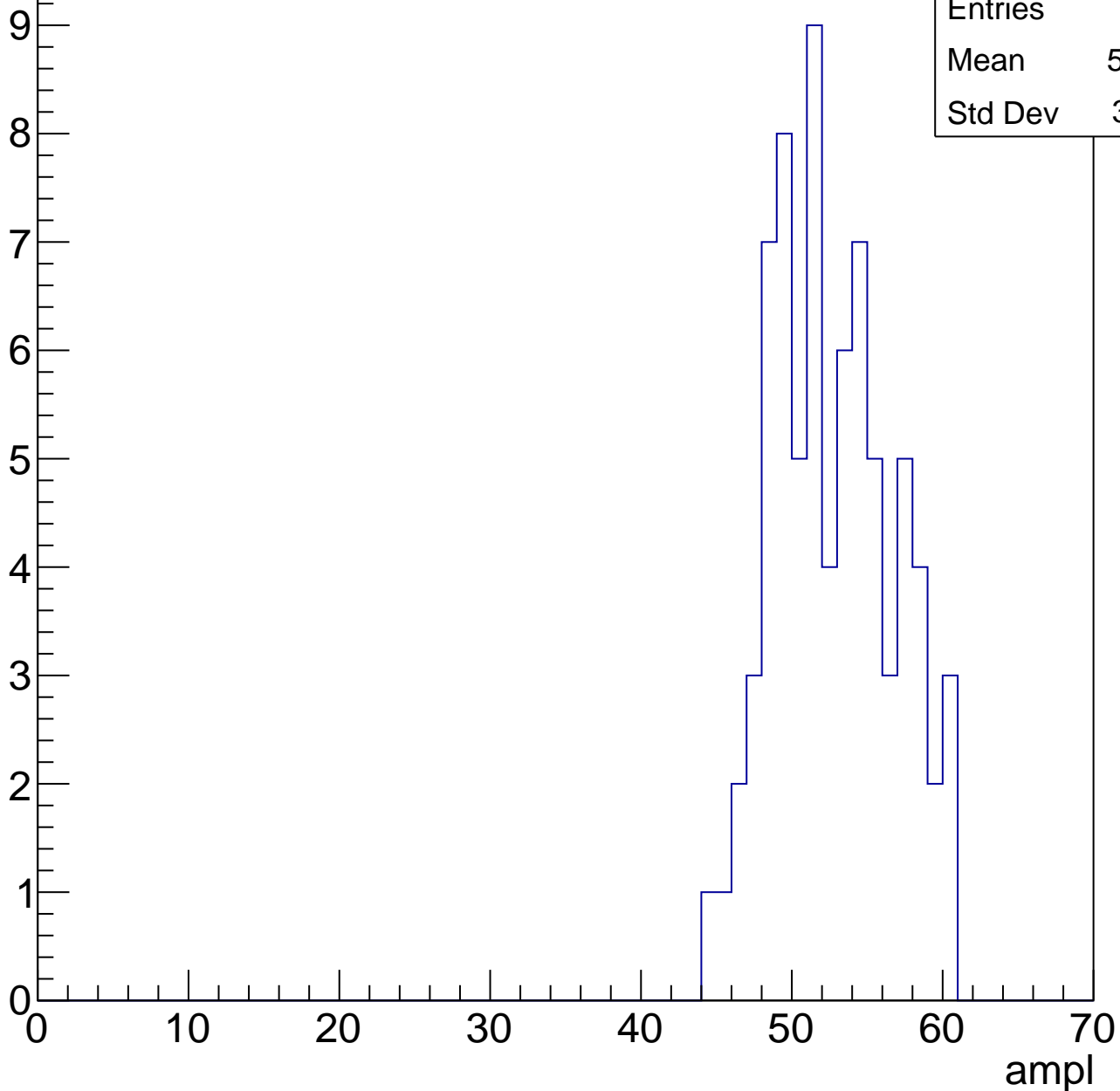


B1L103S, U7-ch114, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	75
Mean	52.28
Std Dev	3.921



B1L103S, U7-ch114, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

7

6

5

4

3

2

1

0

Entries

41

Mean

58.15

Std Dev

2.692

ampl

0

10

20

30

40

50

60

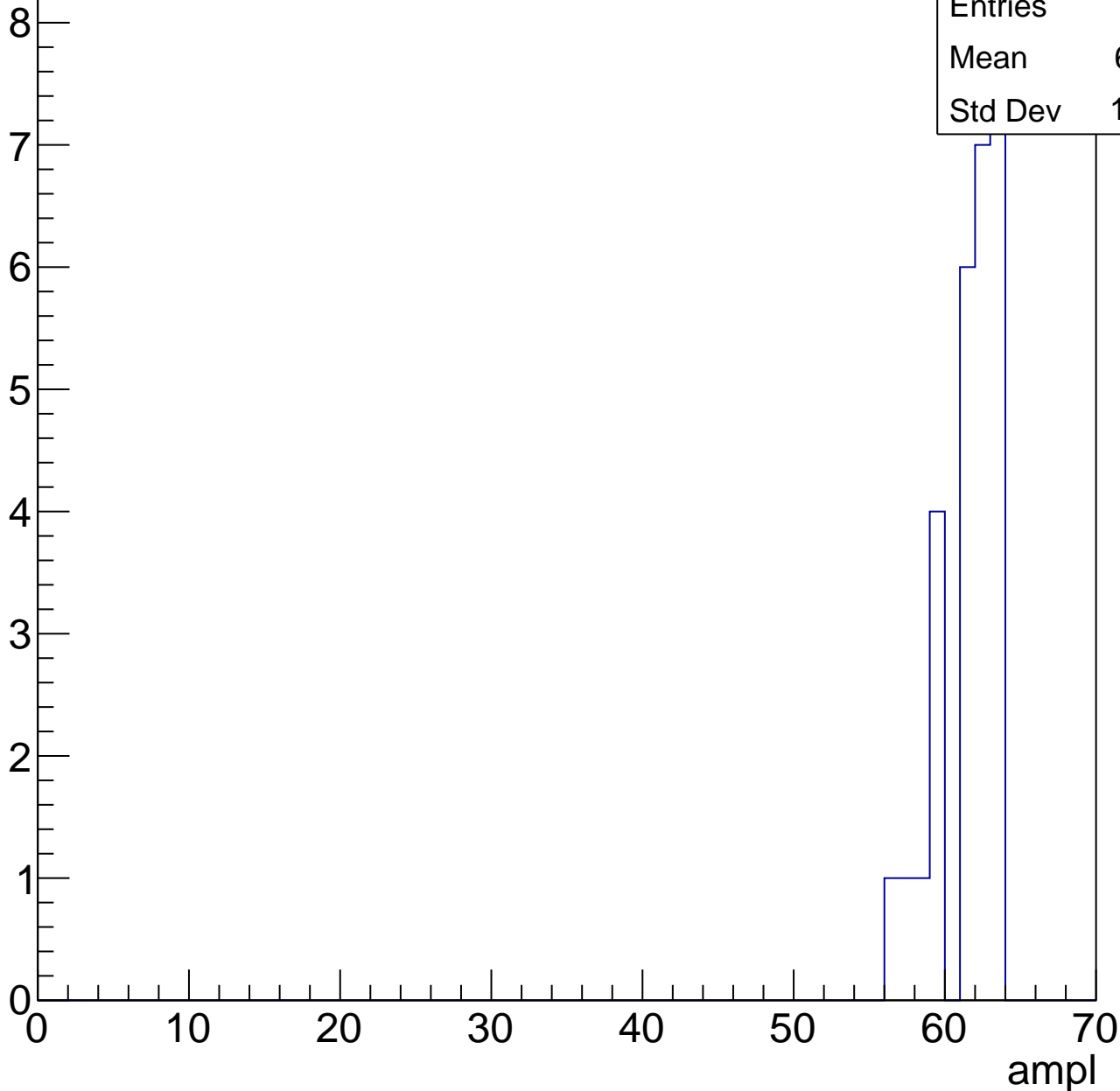
70

B1L103S, U7-ch114, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	28
Mean	61.11
Std Dev	1.934

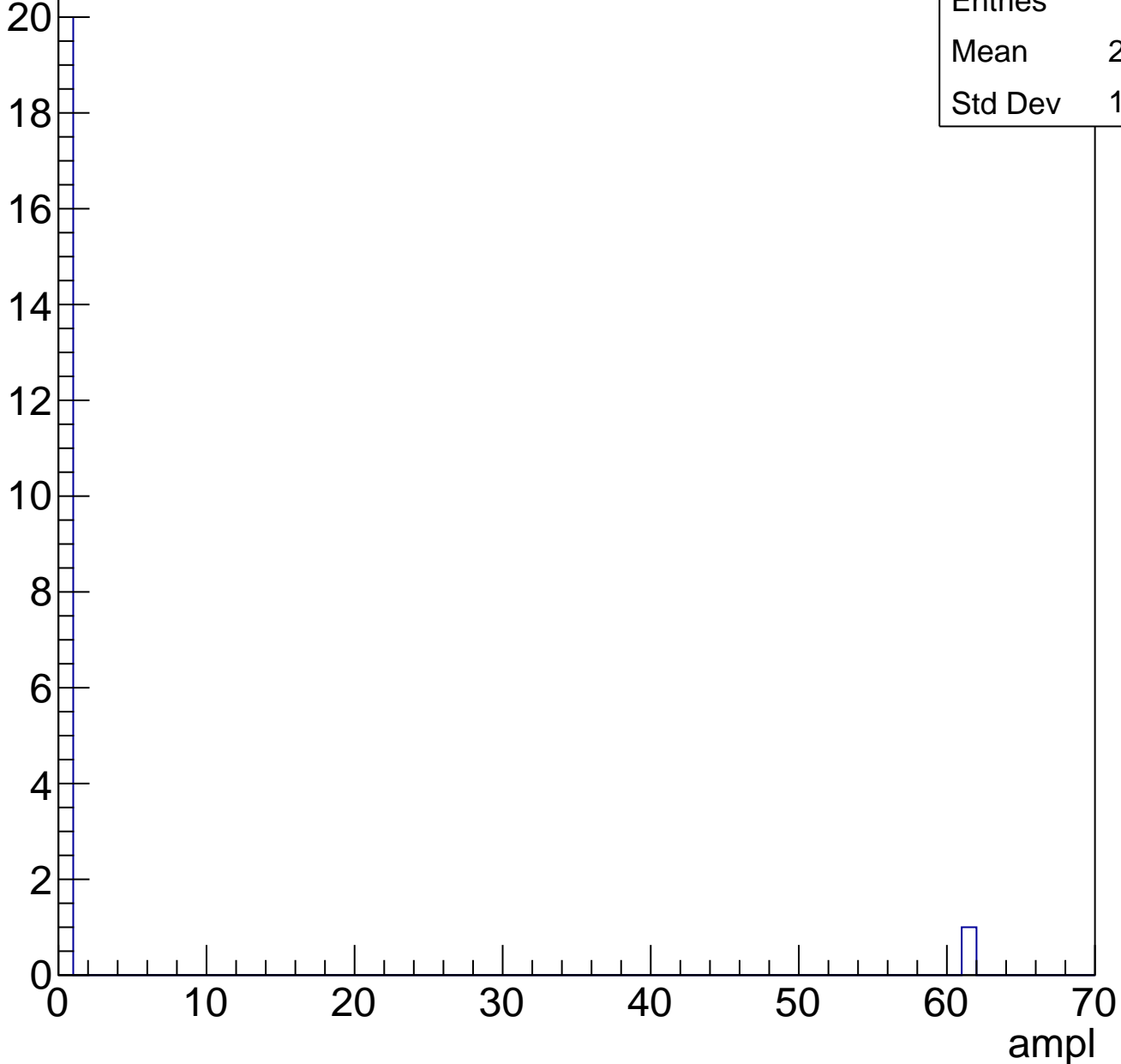


B1L103S, U7-ch114, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	2.905
Std Dev	12.99

Entry



B1L103S, U7-ch115, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	107
Mean	19.73
Std Dev	14.33

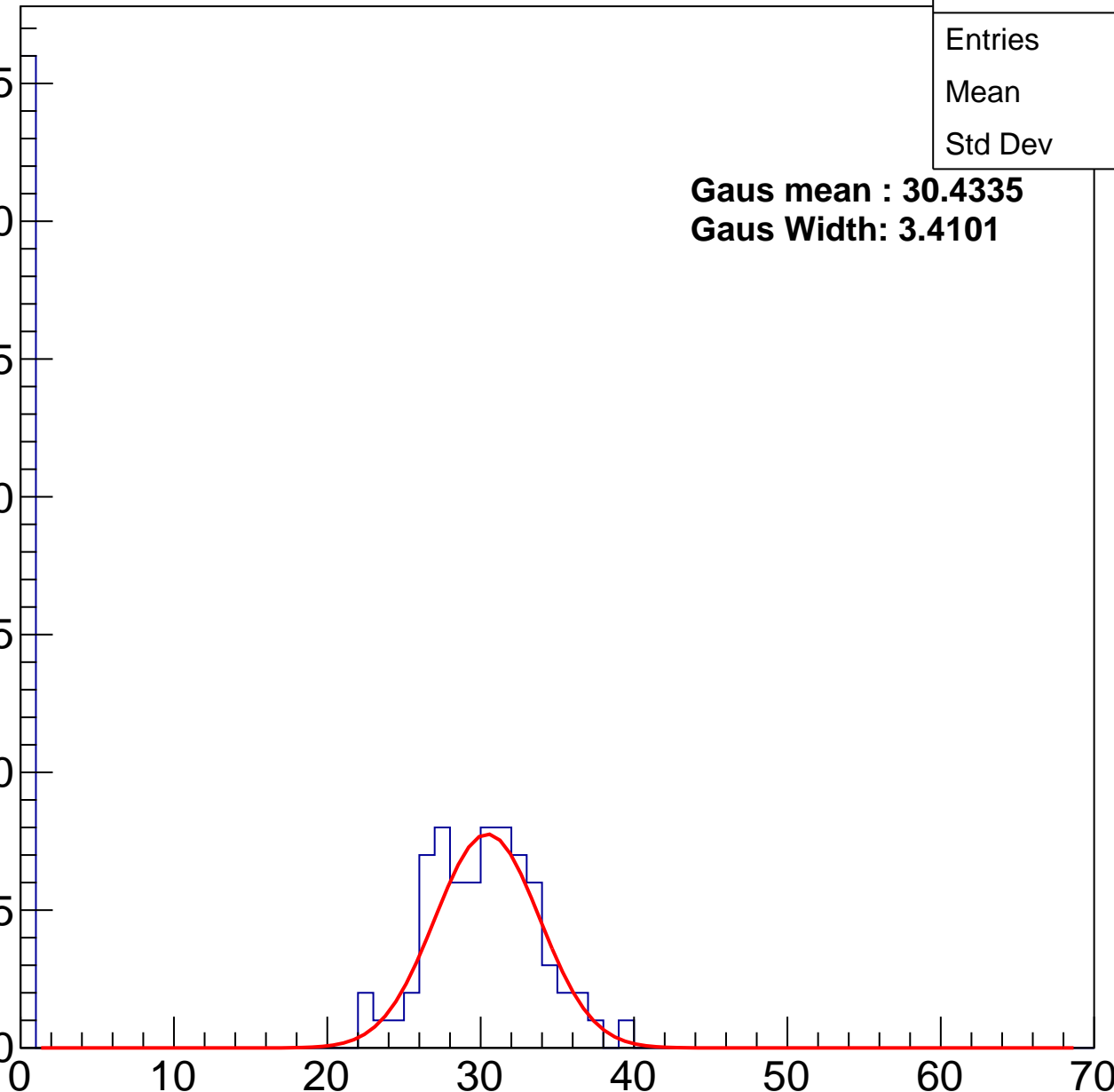
Gaus mean : 30.4335

Gaus Width: 3.4101

Entry

35
30
25
20
15
10
5
0

ampl

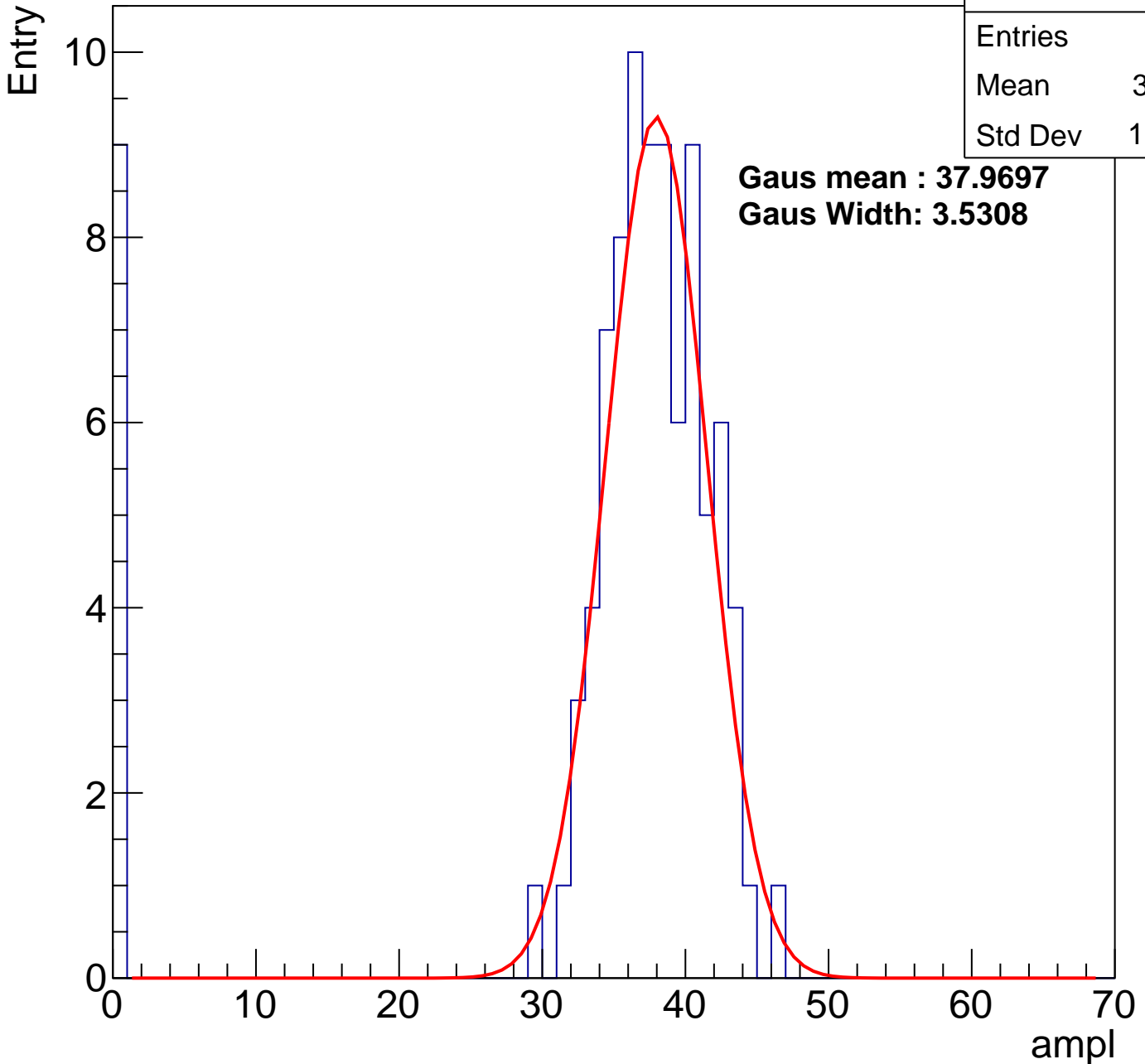


B1L103S, U7-ch115, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	93
Mean	33.91
Std Dev	11.55

Gaus mean : 37.9697
Gaus Width: 3.5308



B1L103S, U7-ch115, adc2

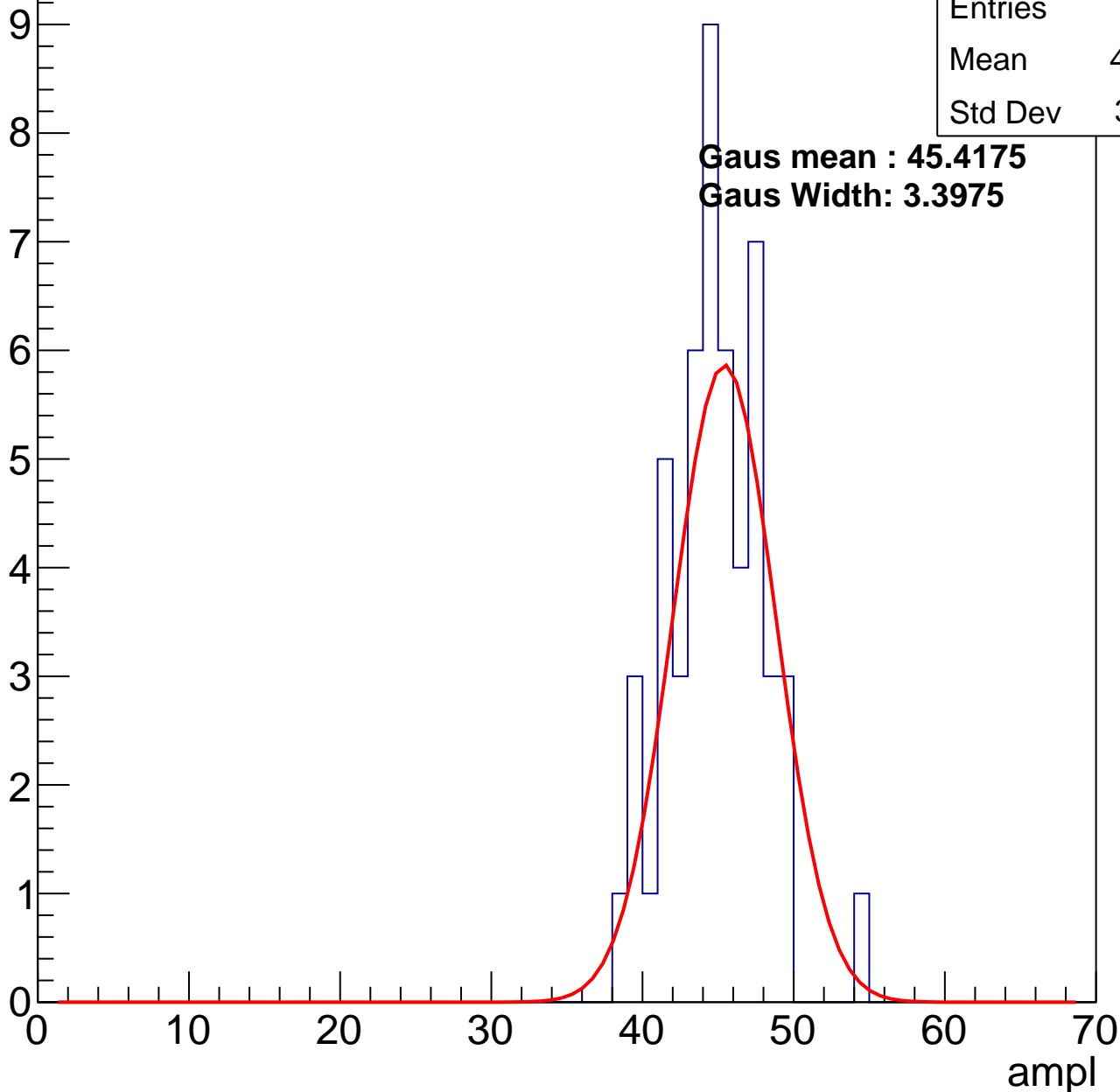
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	44.38
Std Dev	3.071

Gaus mean : 45.4175

Gaus Width: 3.3975

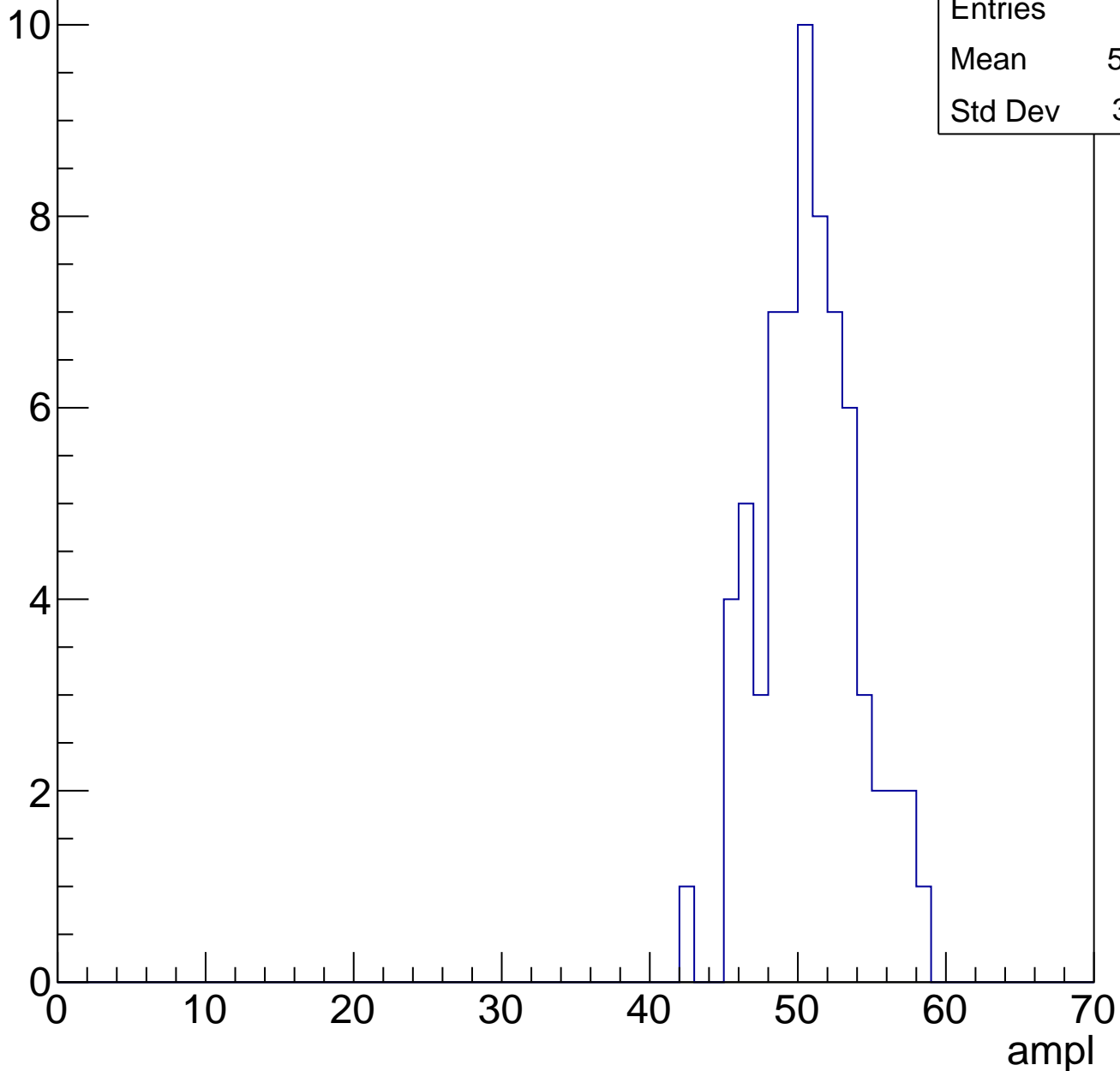


B1L103S, U7-ch115, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	50.26
Std Dev	3.261



B1L103S, U7-ch115, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

7

6

5

4

3

2

1

0

Entries	49
Mean	56.41
Std Dev	2.77

ampl

0

10

20

30

40

50

60

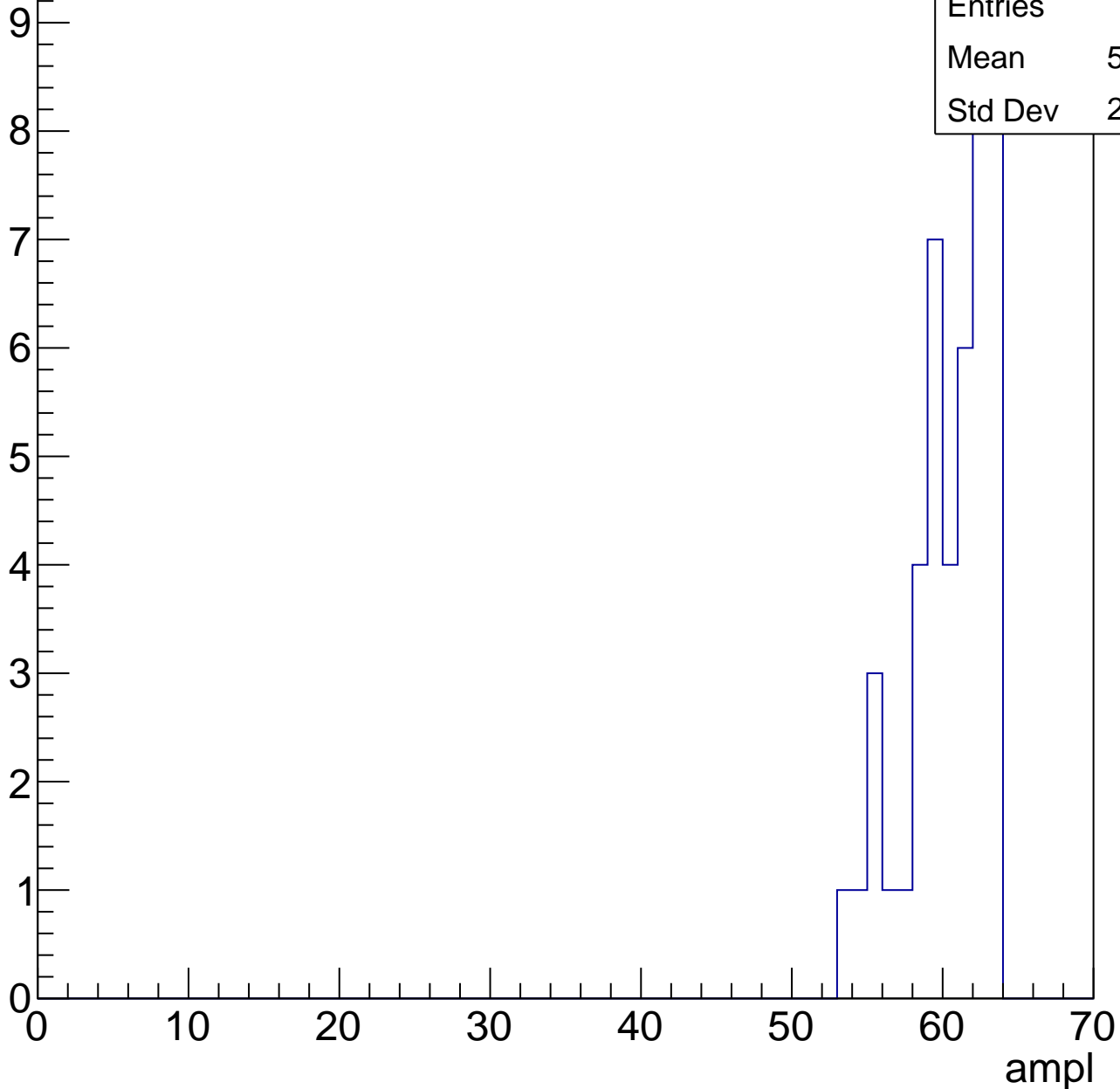
70

B1L103S, U7-ch115, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	45
Mean	59.96
Std Dev	2.675



B1L103S, U7-ch115, adc6

calib_packv5_041523_1651.root, FC#0, port C2

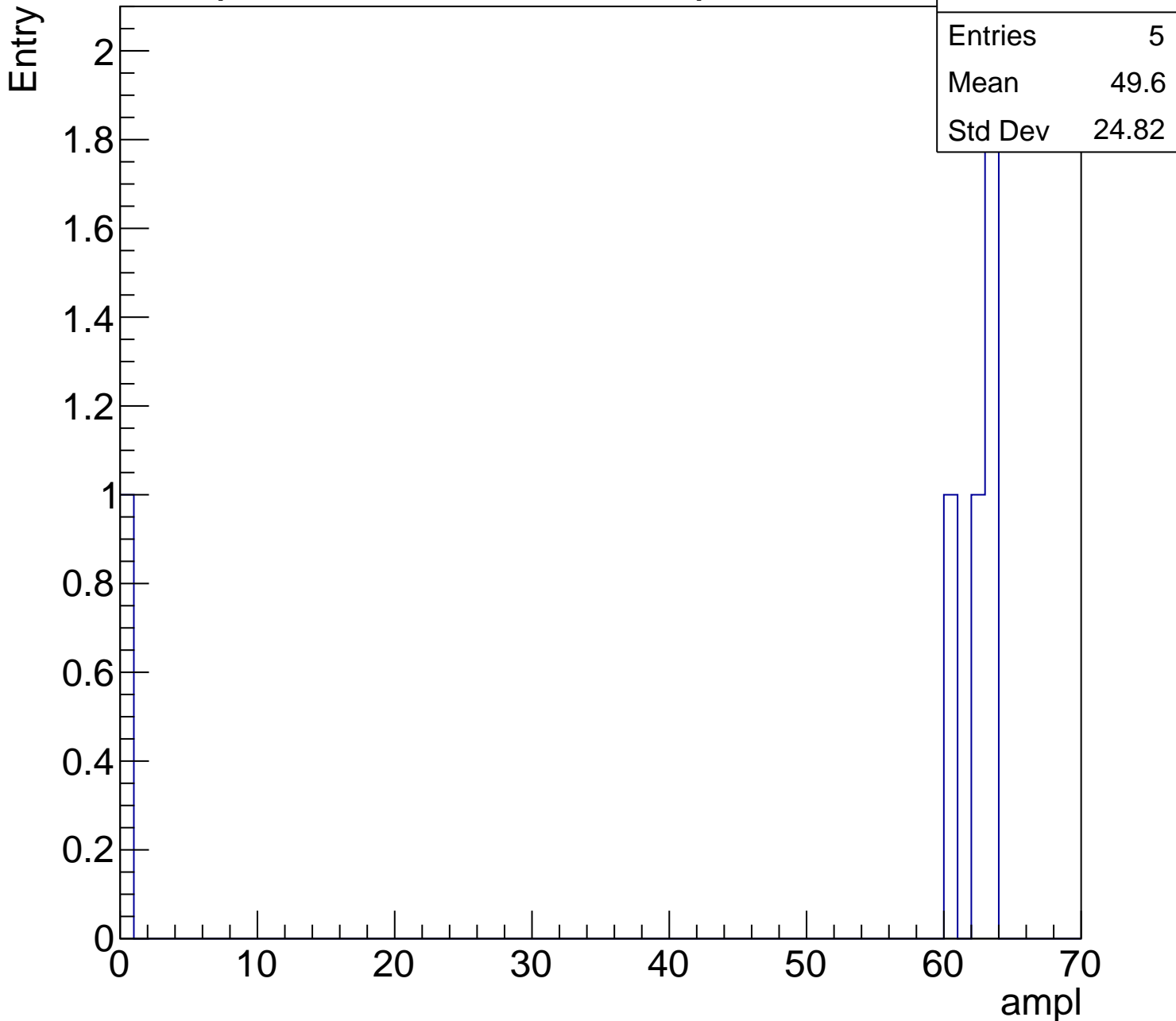
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	5
Mean	49.6
Std Dev	24.82

0 10 20 30 40 50 60 70

ampl



B1L103S, U7-ch115, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U7-ch116, adc0

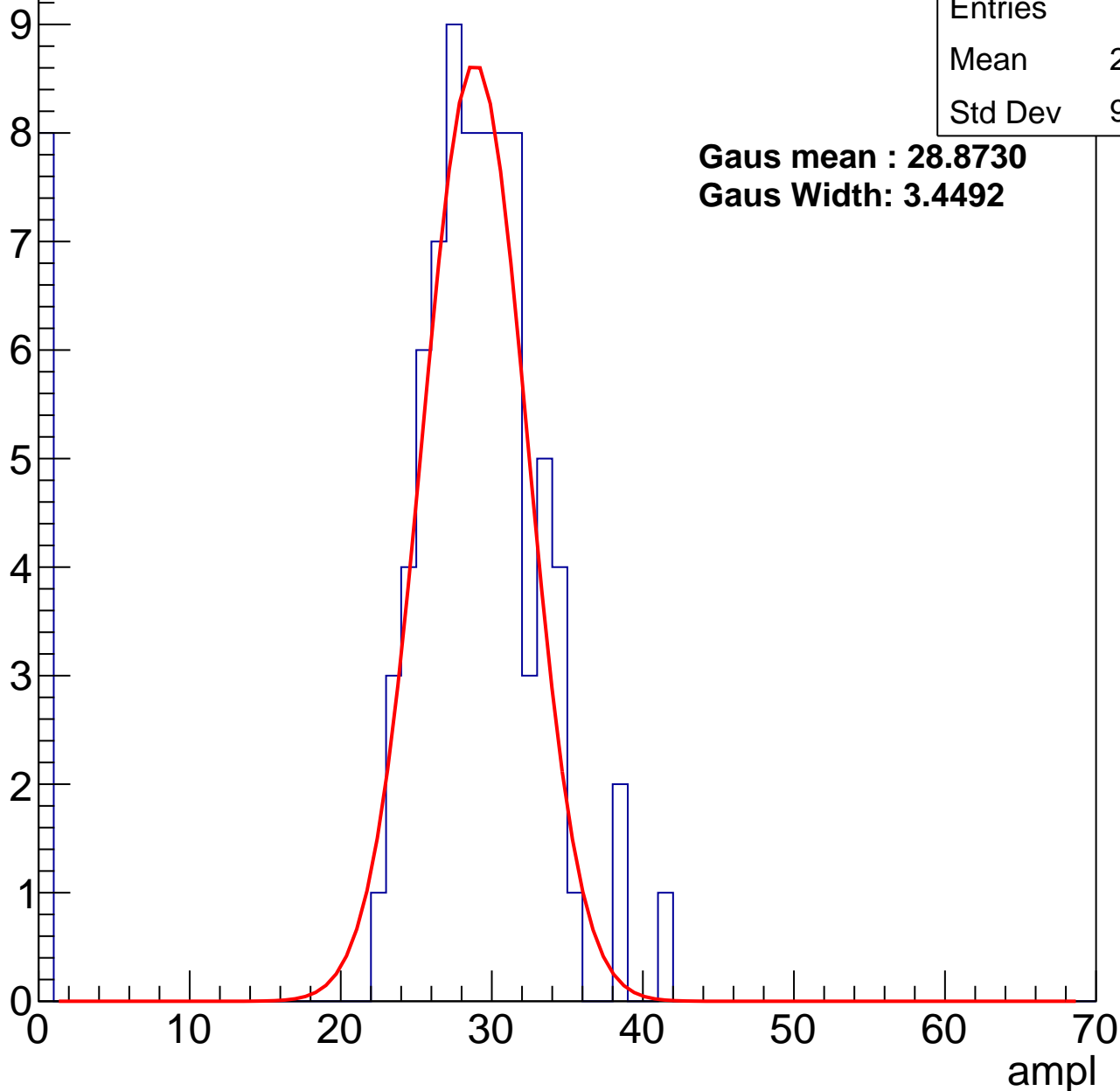
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	86
Mean	26.22
Std Dev	9.094

Gaus mean : 28.8730

Gaus Width: 3.4492



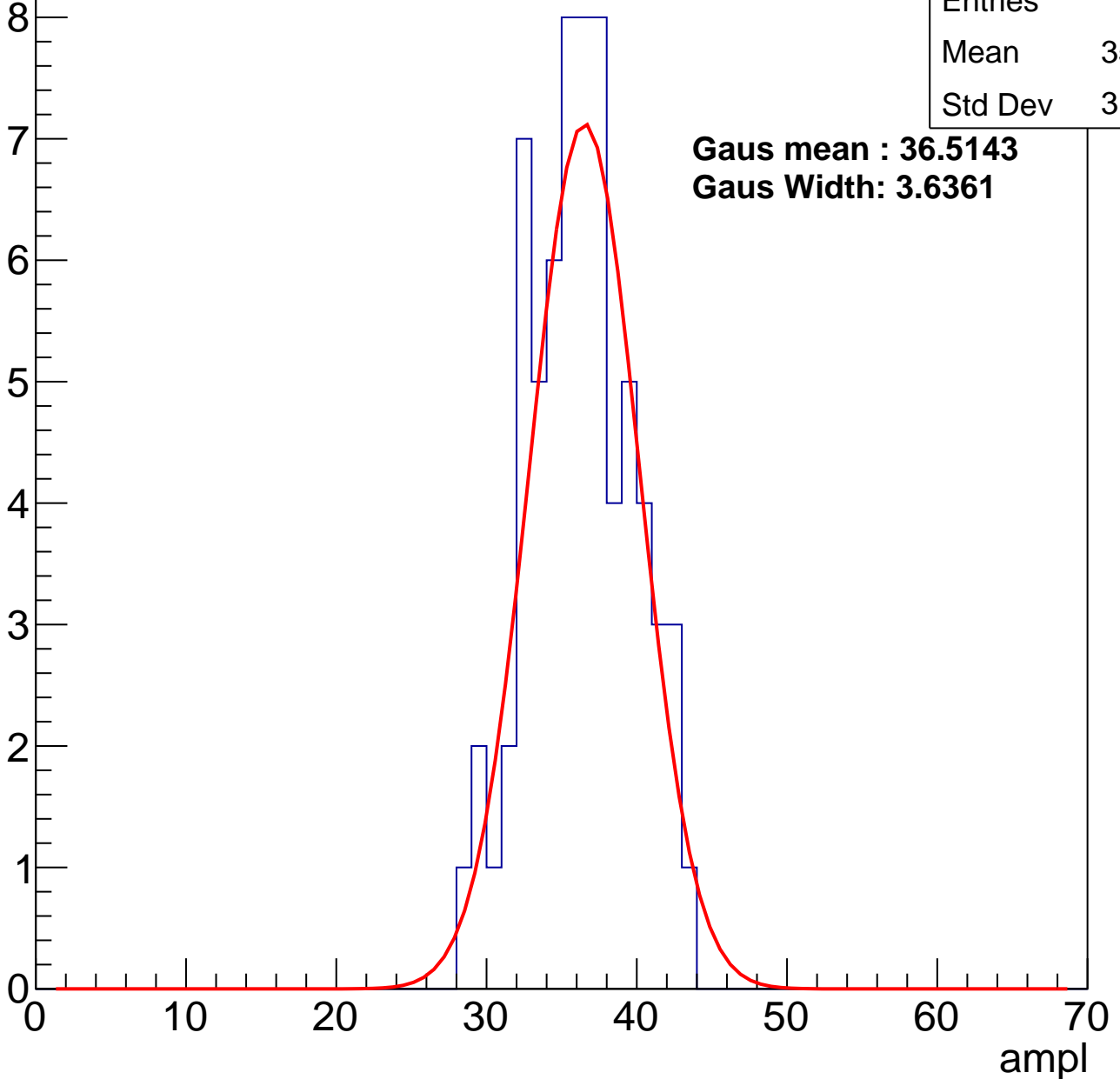
B1L103S, U7-ch116, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	68
Mean	35.79
Std Dev	3.428

Gaus mean : 36.5143
Gaus Width: 3.6361



B1L103S, U7-ch116, adc2

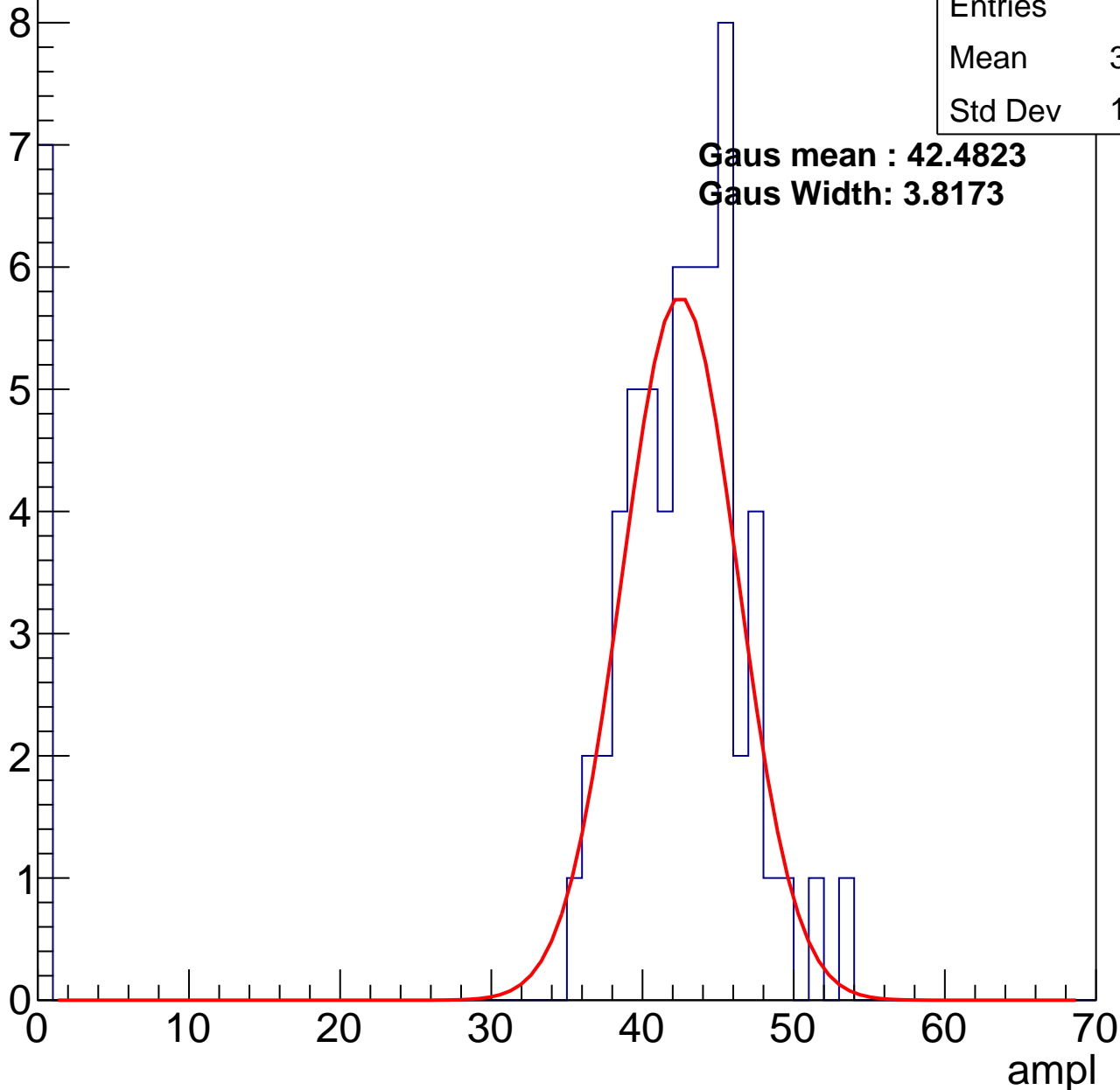
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	66
Mean	37.98
Std Dev	13.55

Gaus mean : 42.4823

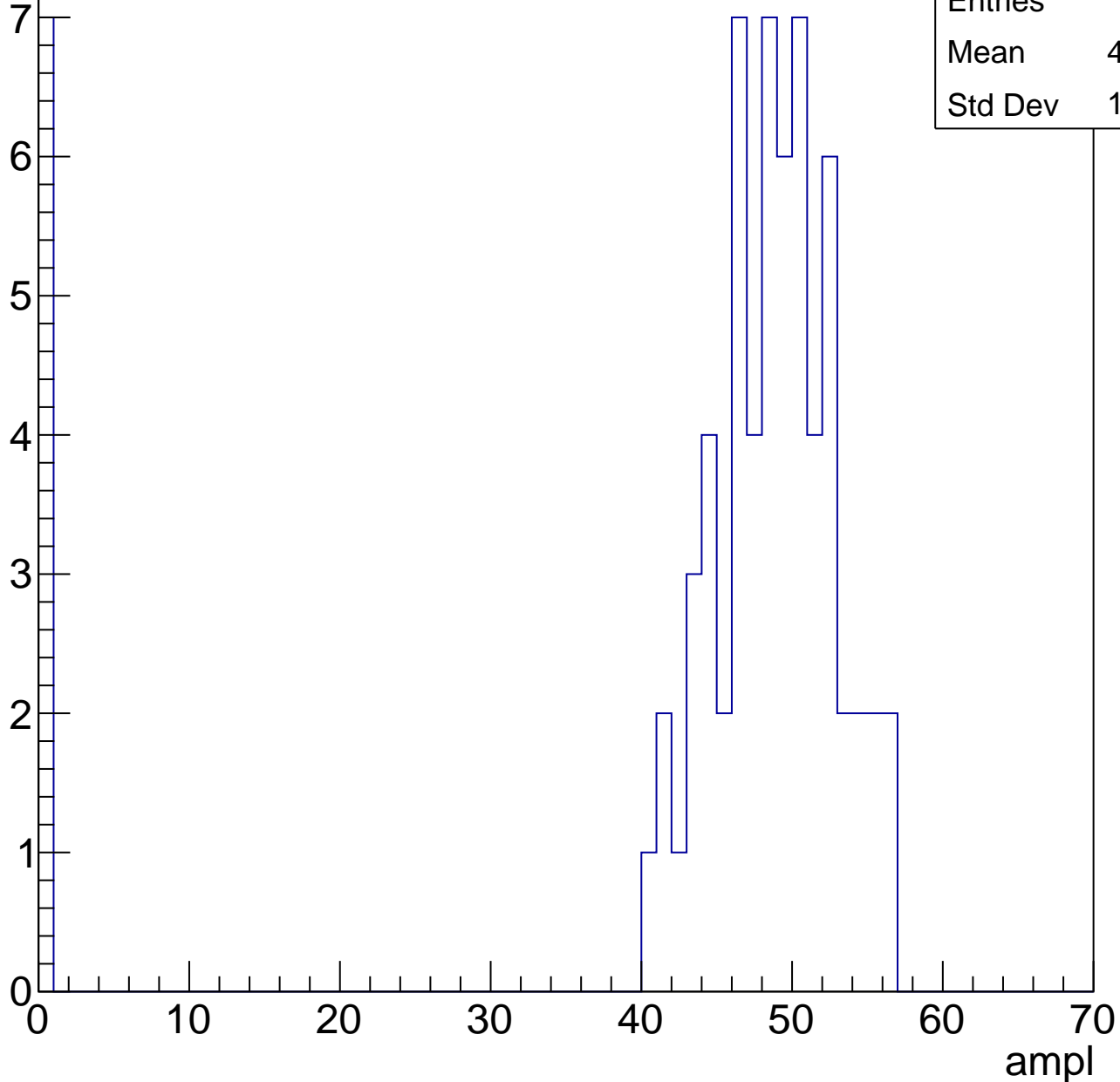
Gaus Width: 3.8173



B1L103S, U7-ch116, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry



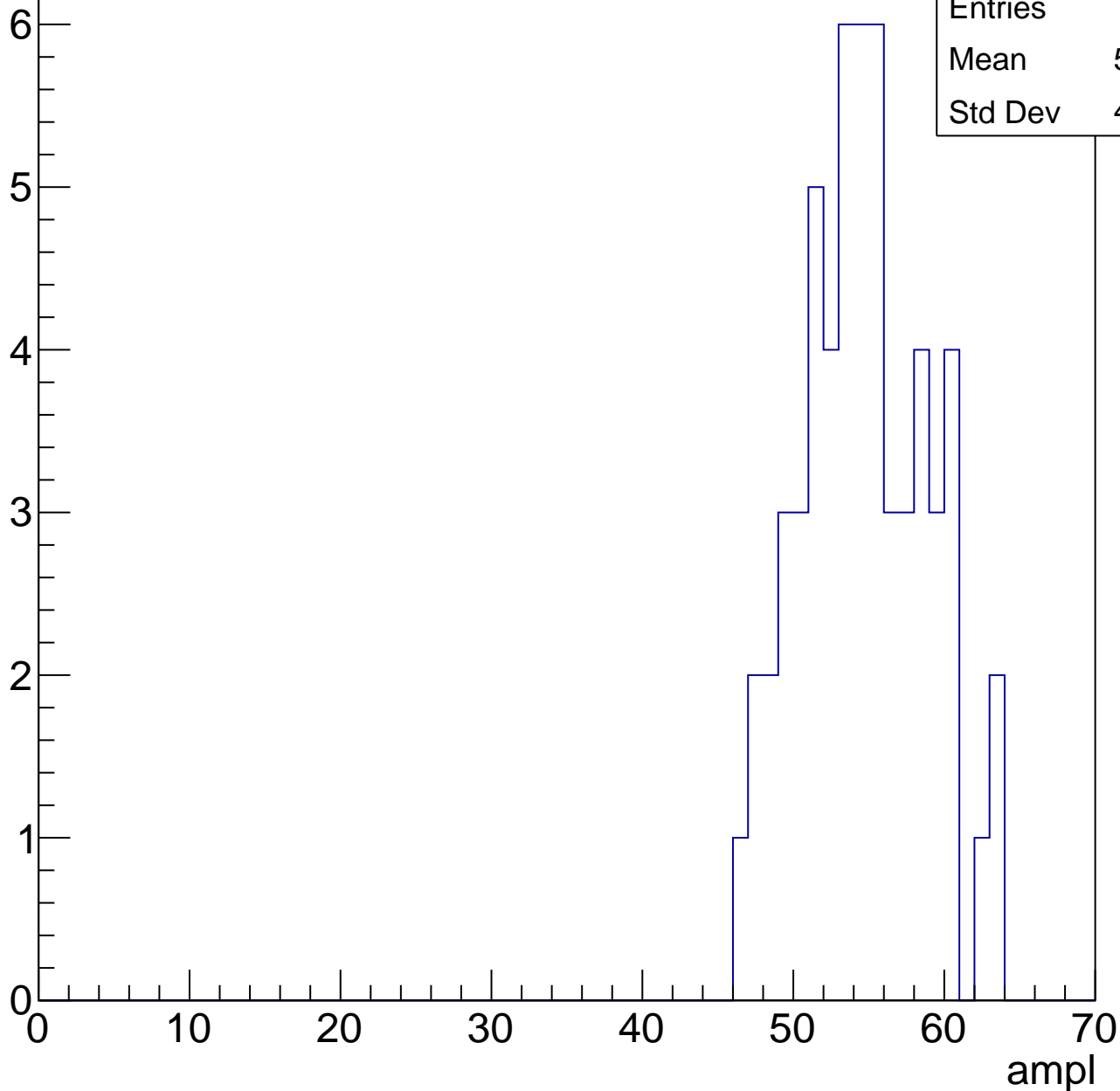
Entries	69
Mean	43.49
Std Dev	15.05

B1L103S, U7-ch116, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	54.21
Std Dev	4.101

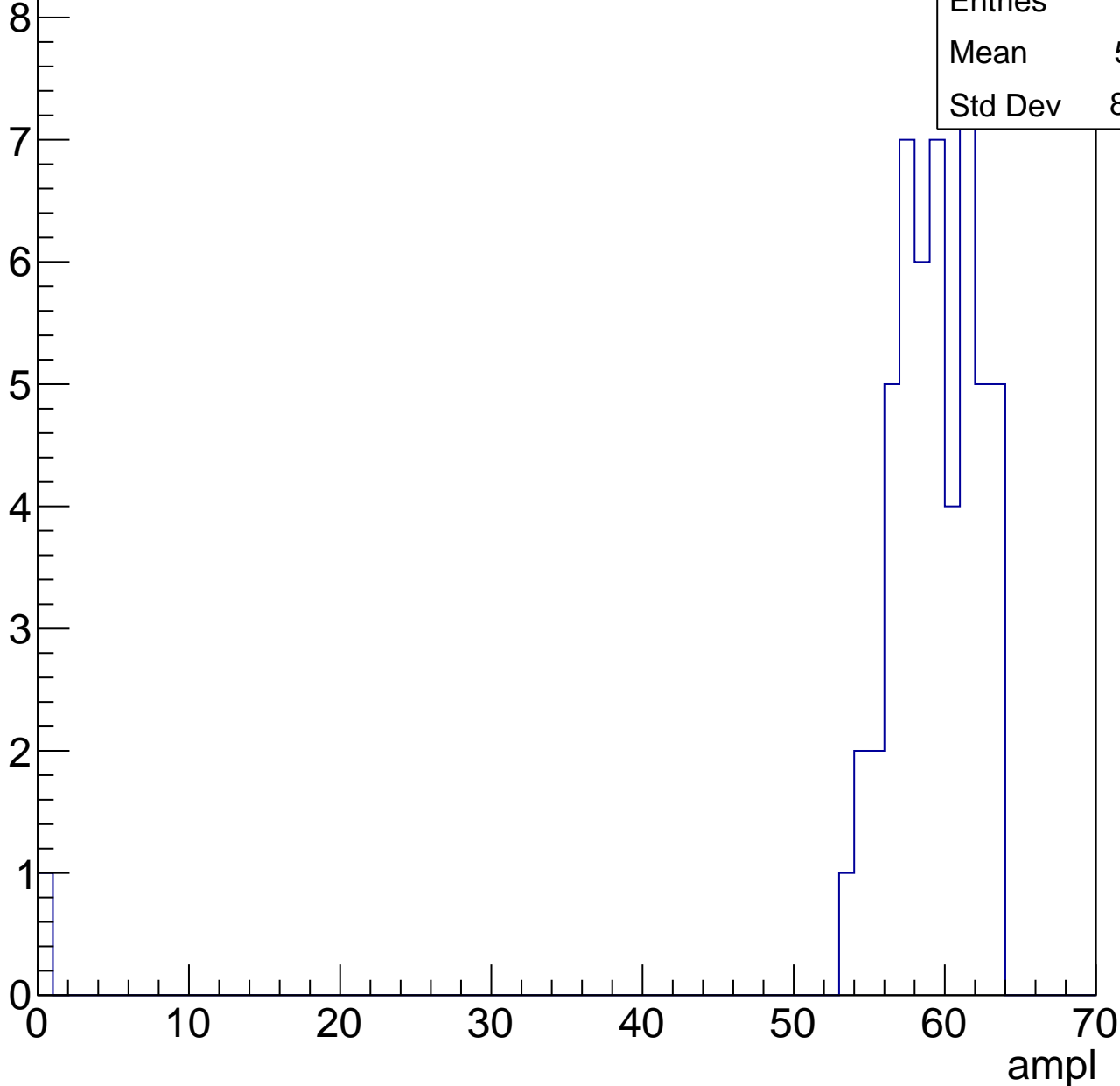


B1L103S, U7-ch116, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

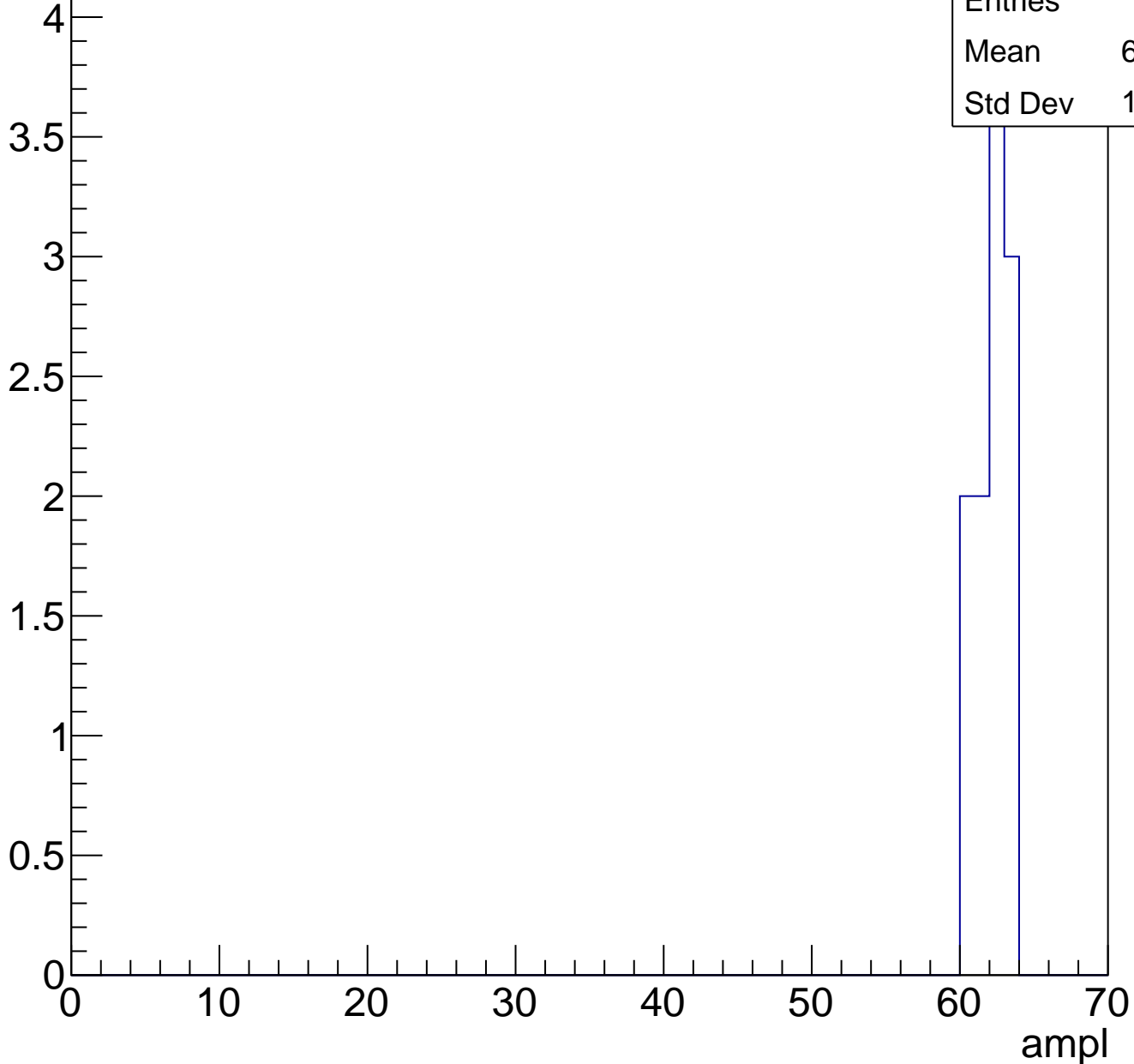
Entries	53
Mean	57.81
Std Dev	8.427



B1L103S, U7-ch116, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch116, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	18
Mean	1.056
Std Dev	4.352

Entry

16

14

12

10

8

6

4

2

0

0

10

20

30

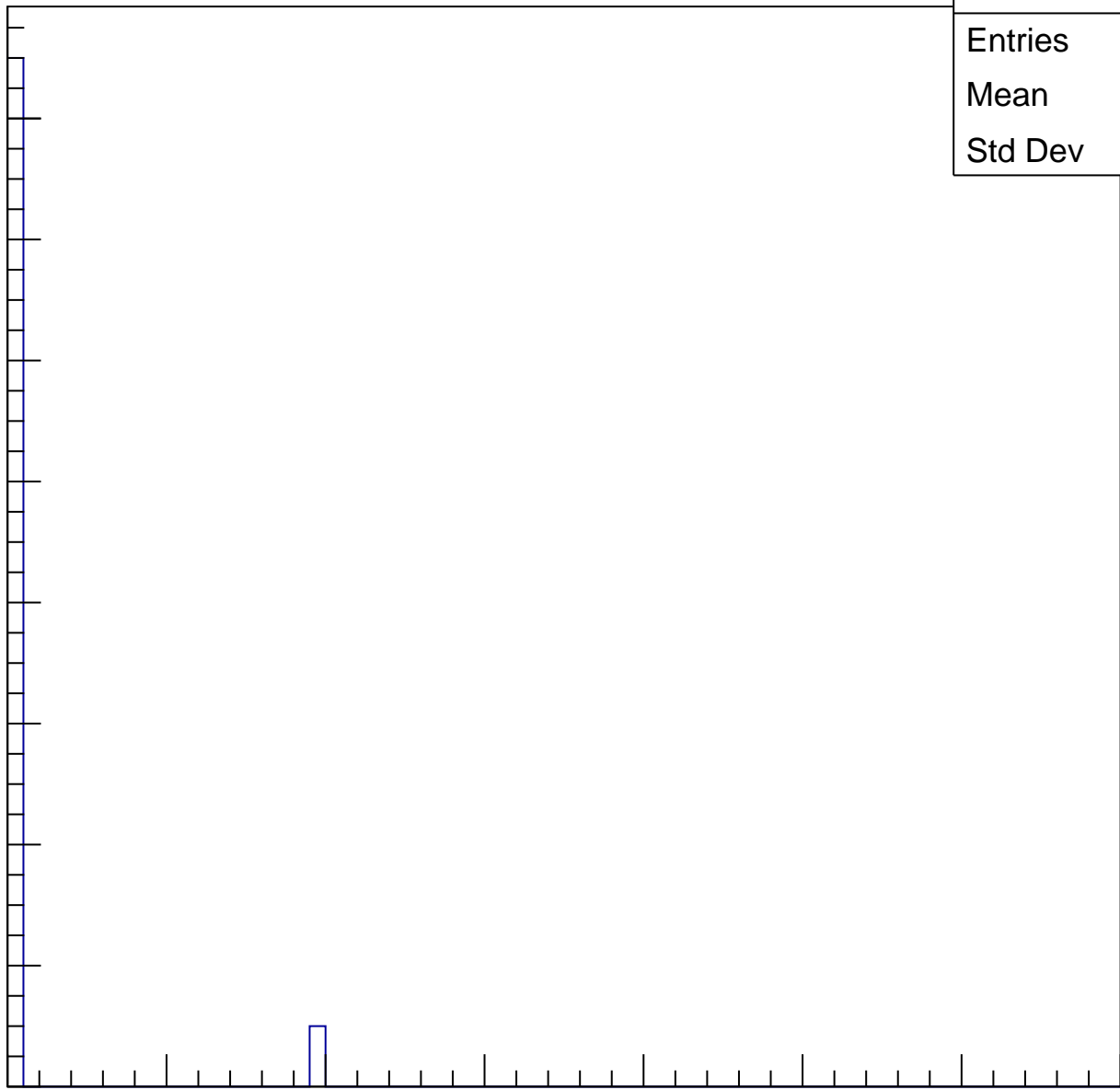
40

50

60

70

ampl



B1L103S, U7-ch117, adc0

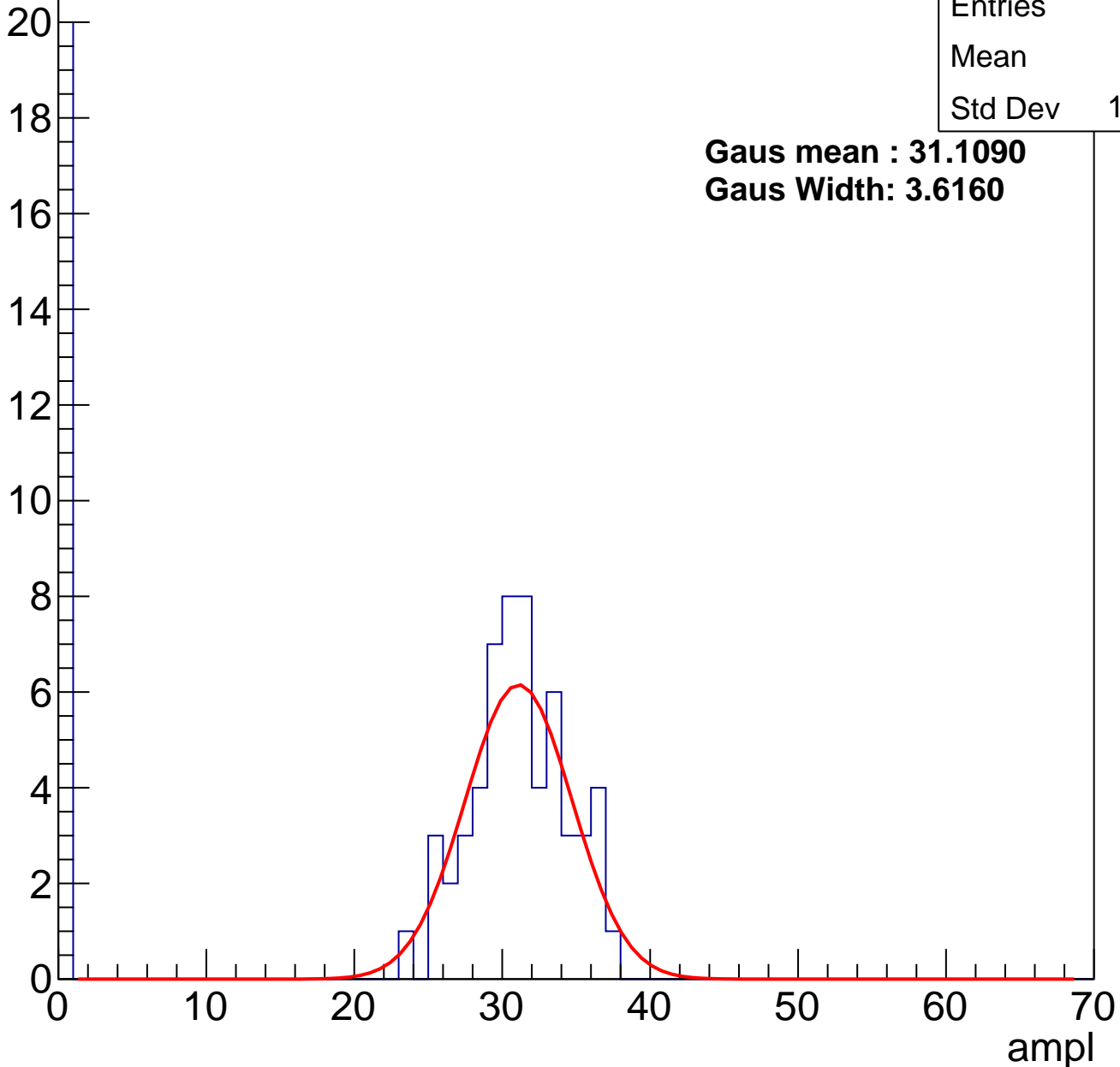
calib_packv5_041523_1651.root, FC#0, port C2

Entries	77
Mean	22.7
Std Dev	13.72

Gaus mean : 31.1090

Gaus Width: 3.6160

Entry



B1L103S, U7-ch117, adc1

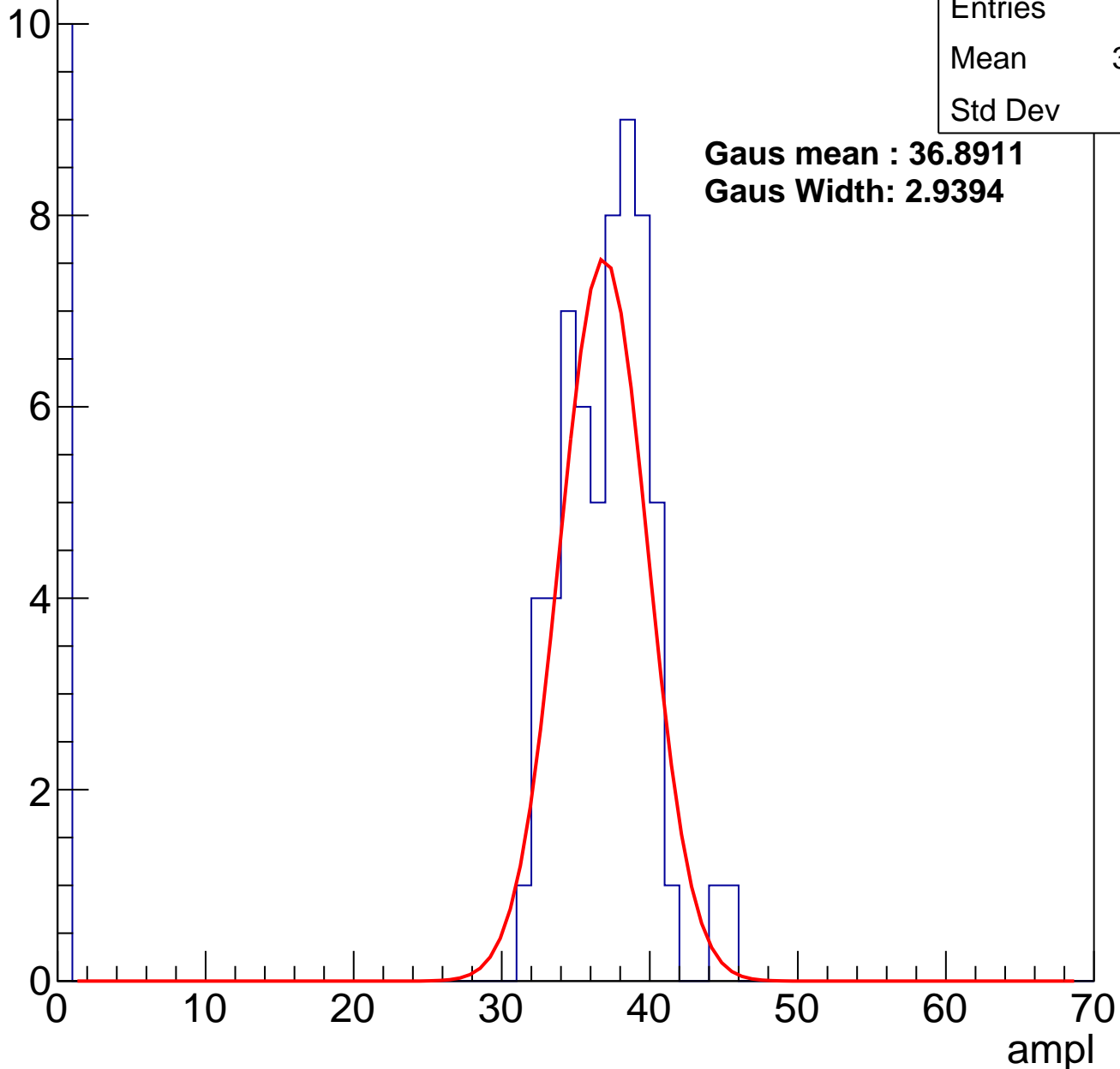
calib_packv5_041523_1651.root, FC#0, port C2

Entries	70
Mean	31.41
Std Dev	13.1

Gaus mean : 36.8911

Gaus Width: 2.9394

Entry



B1L103S, U7-ch117, adc2

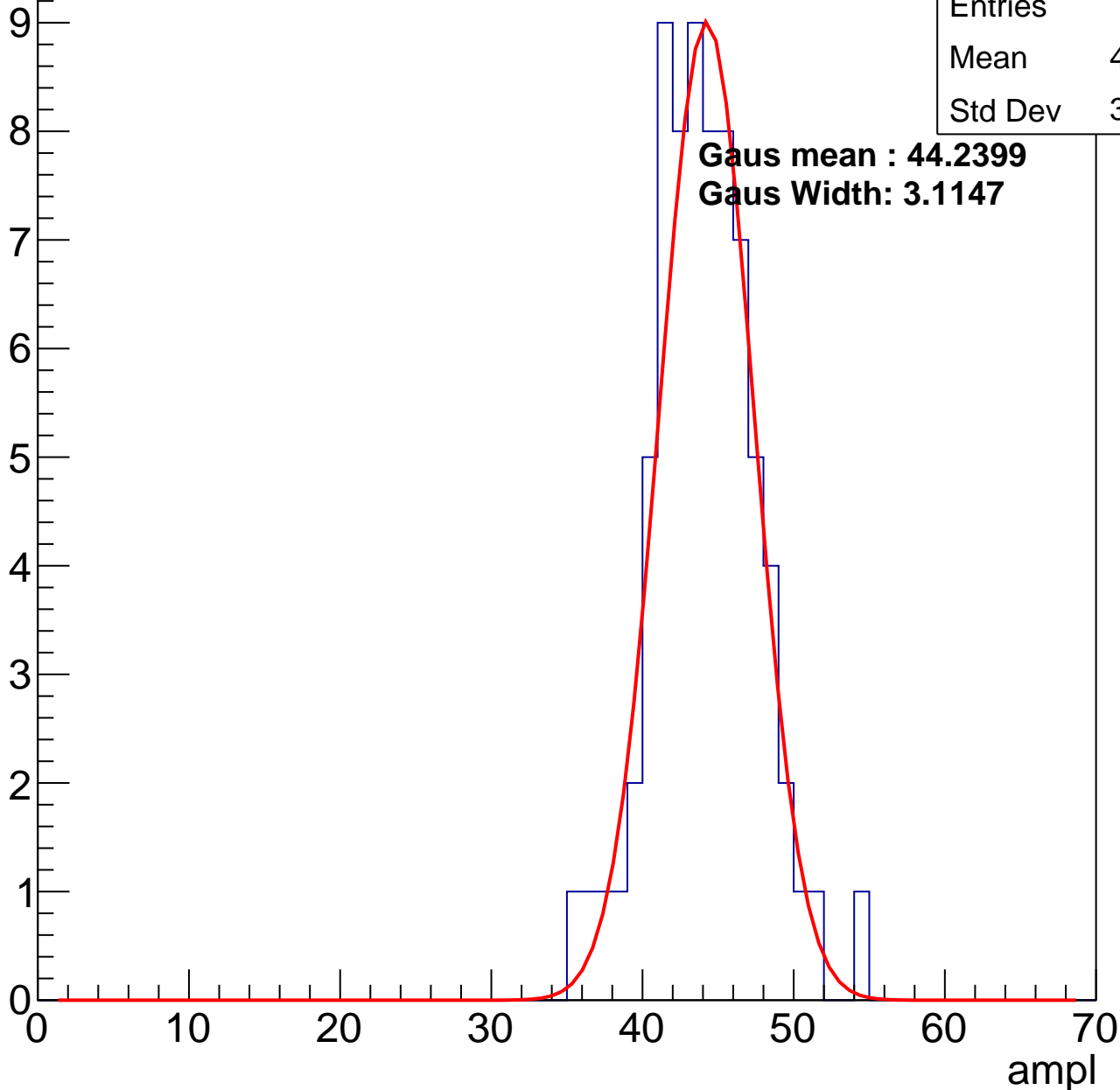
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	43.65
Std Dev	3.395

Gaus mean : 44.2399

Gaus Width: 3.1147

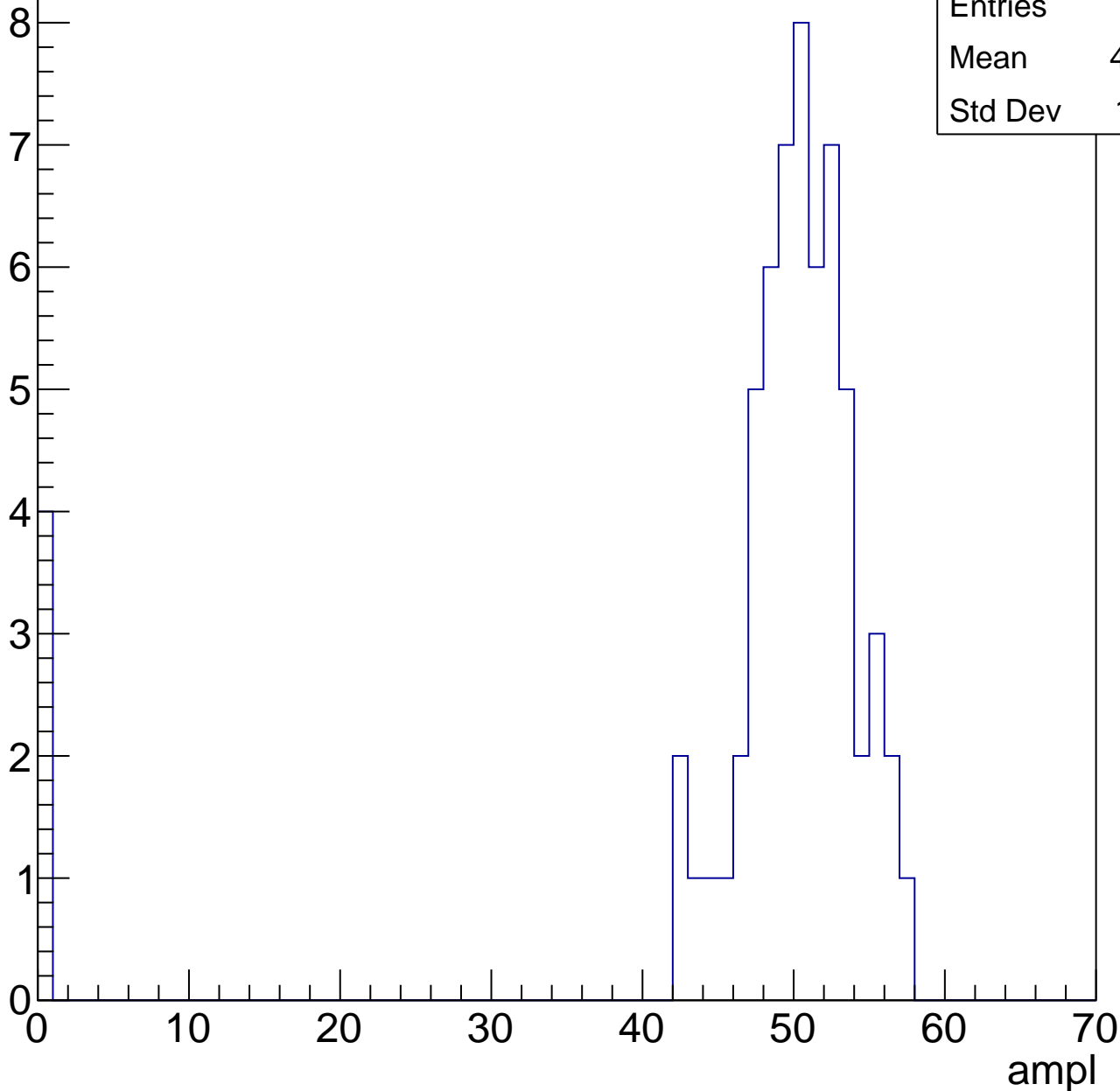


B1L103S, U7-ch117, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

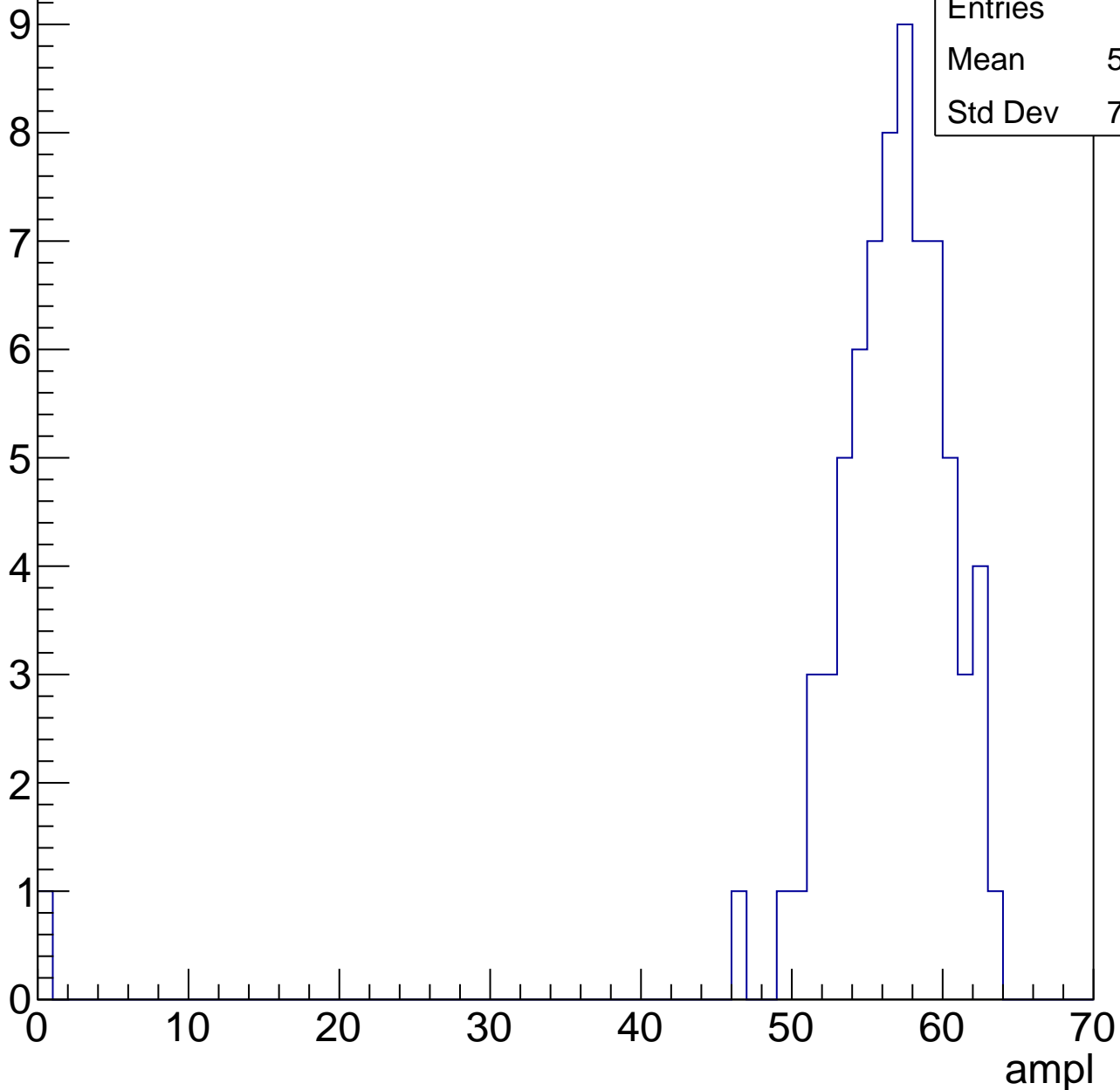
Entries	63
Mean	46.84
Std Dev	12.61



B1L103S, U7-ch117, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry



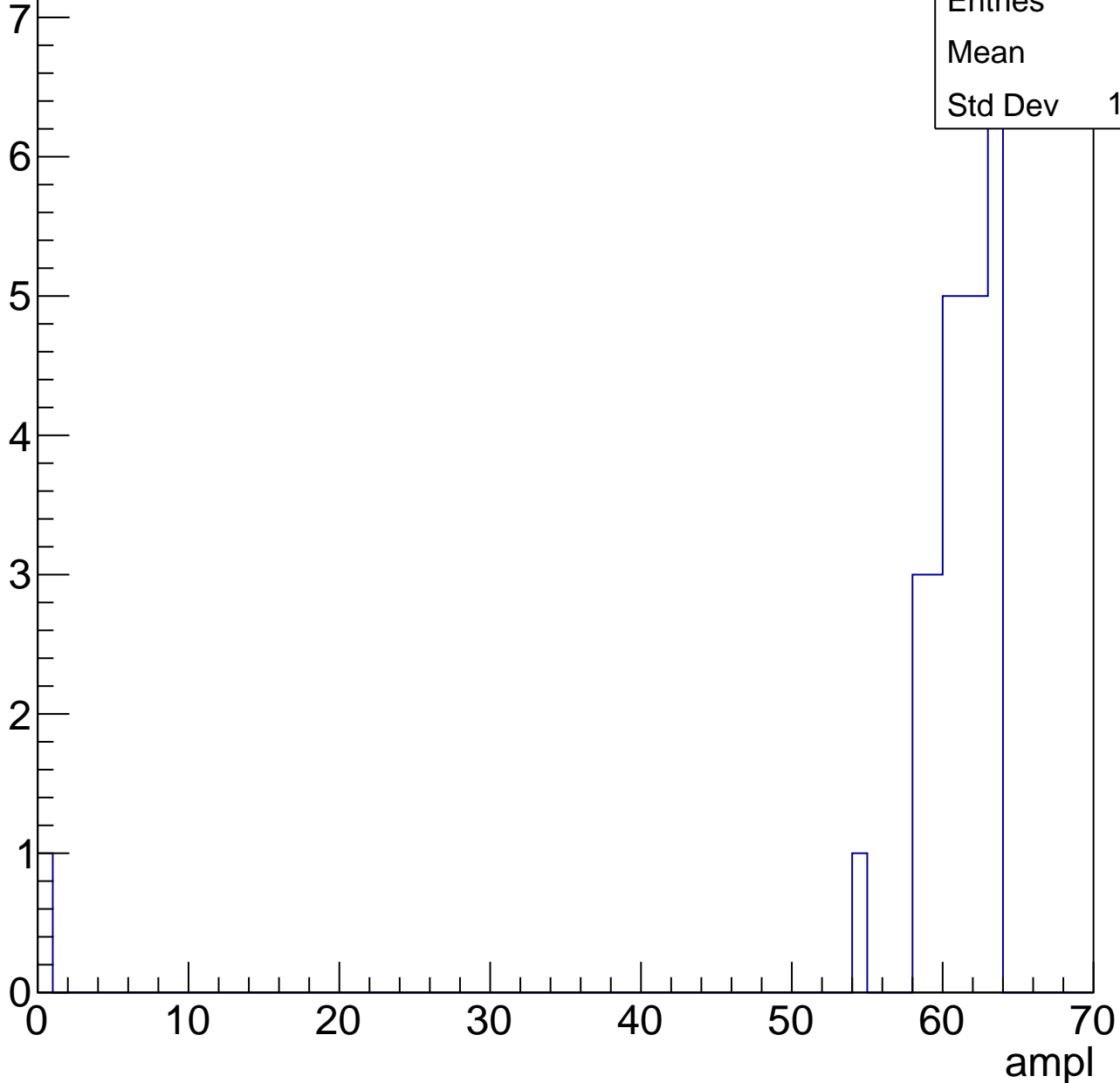
Entries	72
Mean	55.58
Std Dev	7.412

B1L103S, U7-ch117, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	30
Mean	58.7
Std Dev	11.09



B1L103S, U7-ch117, adc6

calib_packv5_041523_1651.root, FC#0, port C2

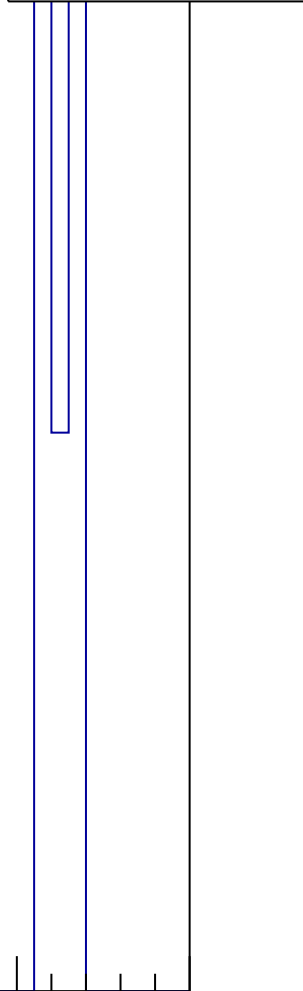
Entry

2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0

Entries	5
Mean	62
Std Dev	0.8944

0 10 20 30 40 50 60 70

ampl



B1L103S, U7-ch117, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch118, adc0

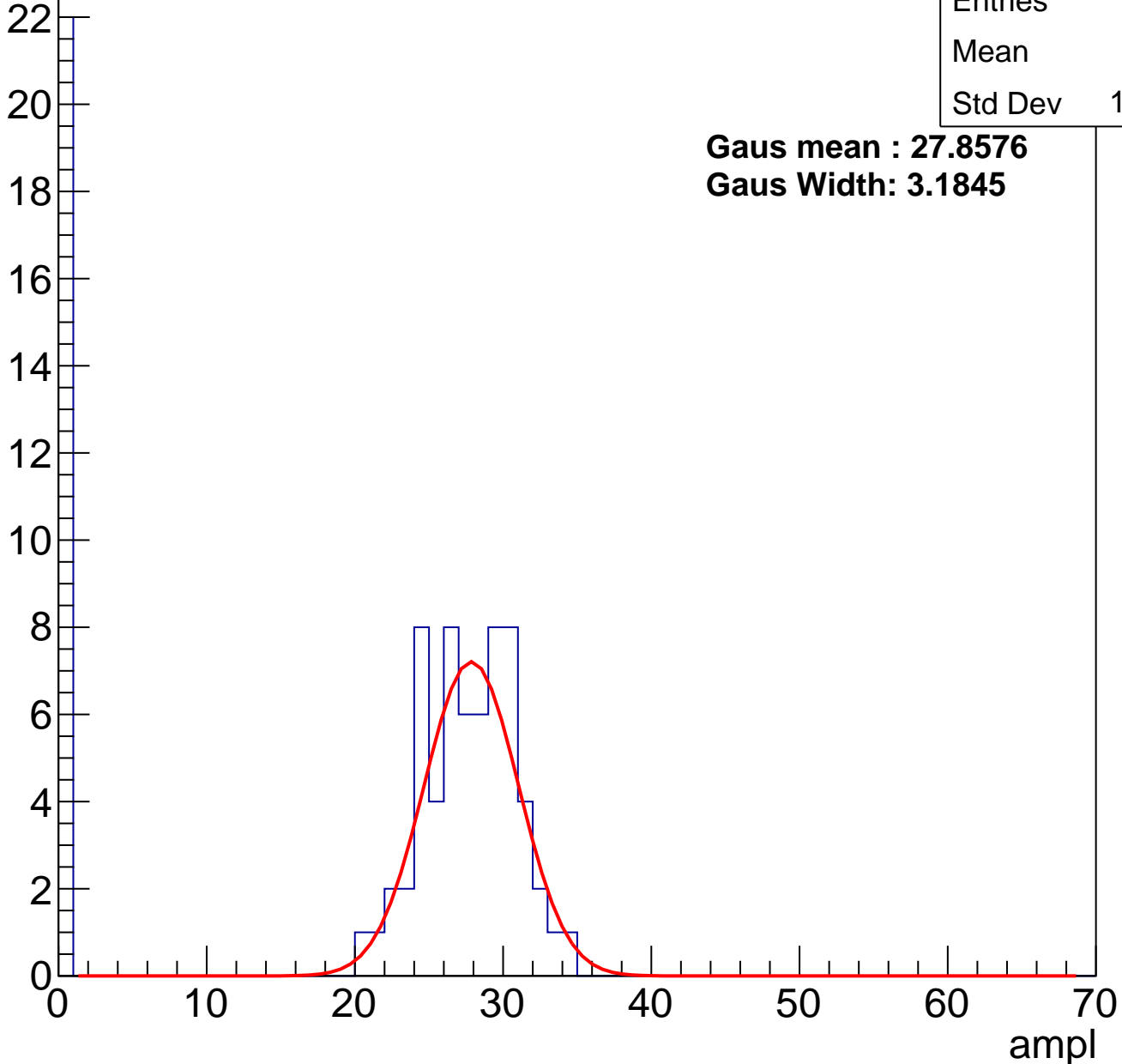
calib_packv5_041523_1651.root, FC#0, port C2

Entries	84
Mean	20.1
Std Dev	12.25

Gaus mean : 27.8576

Gaus Width: 3.1845

Entry



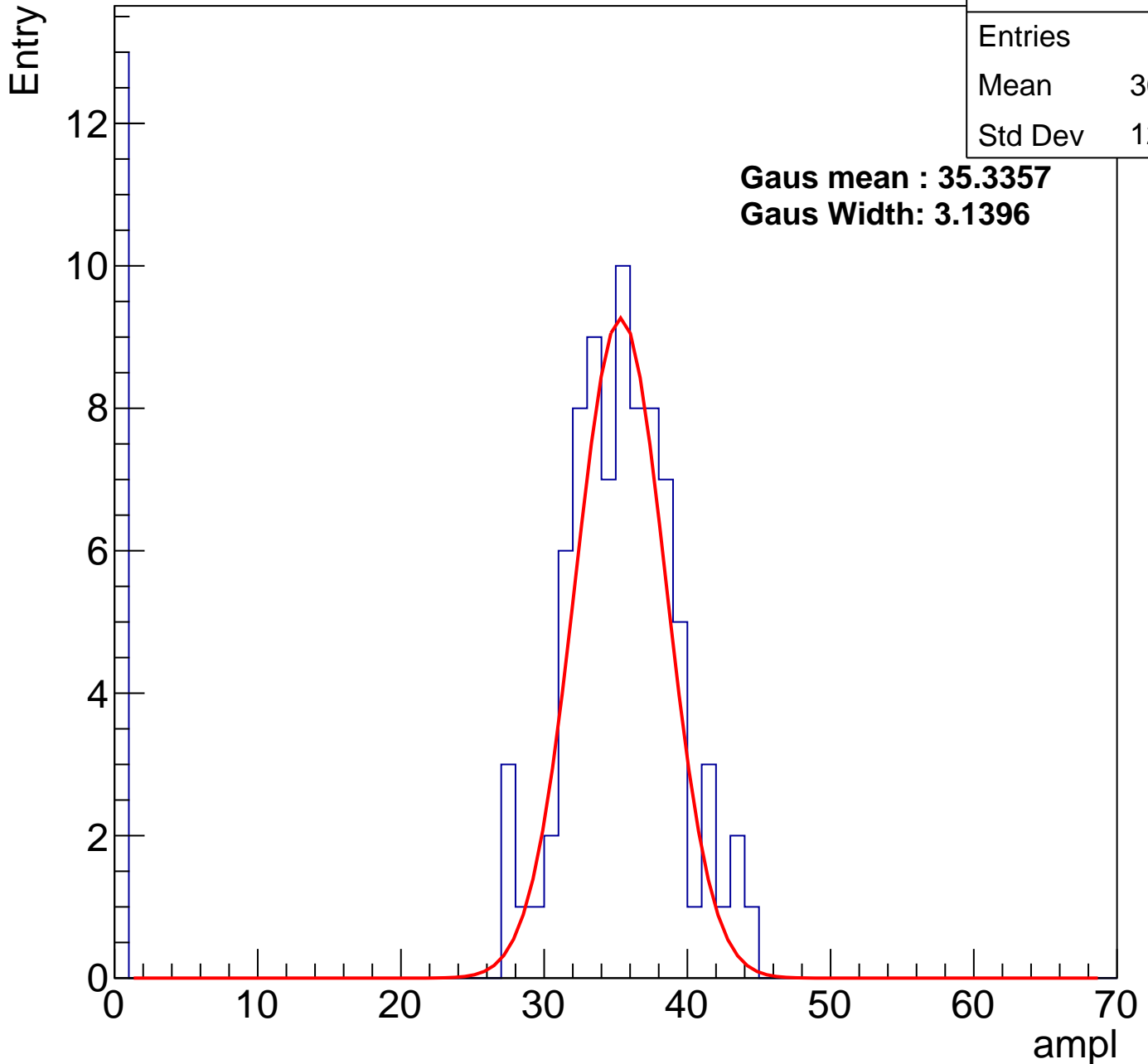
B1L103S, U7-ch118, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	96
Mean	30.26
Std Dev	12.45

Gaus mean : 35.3357

Gaus Width: 3.1396



B1L103S, U7-ch118, adc2

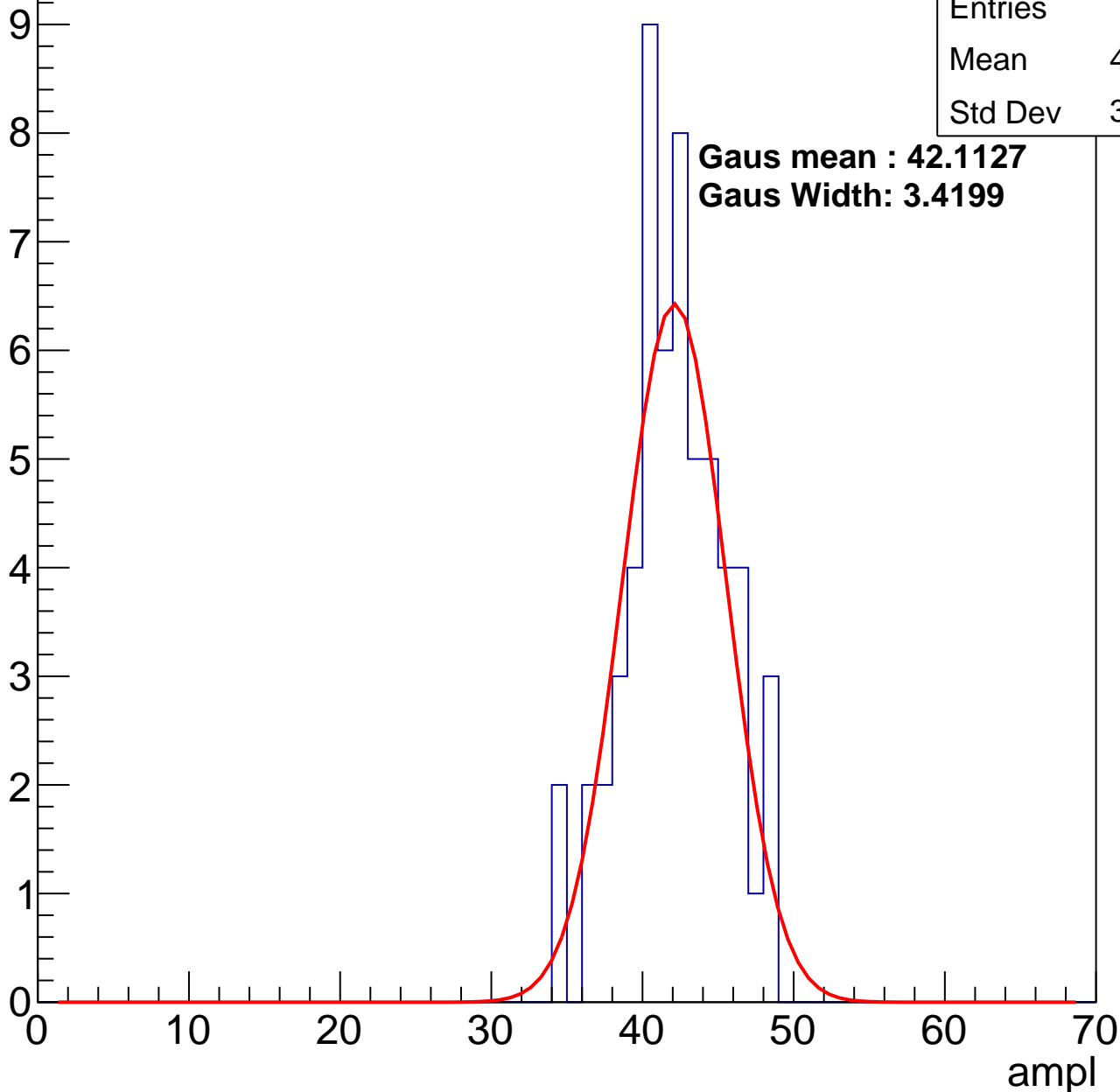
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	58
Mean	41.66
Std Dev	3.288

Gaus mean : 42.1127

Gaus Width: 3.4199

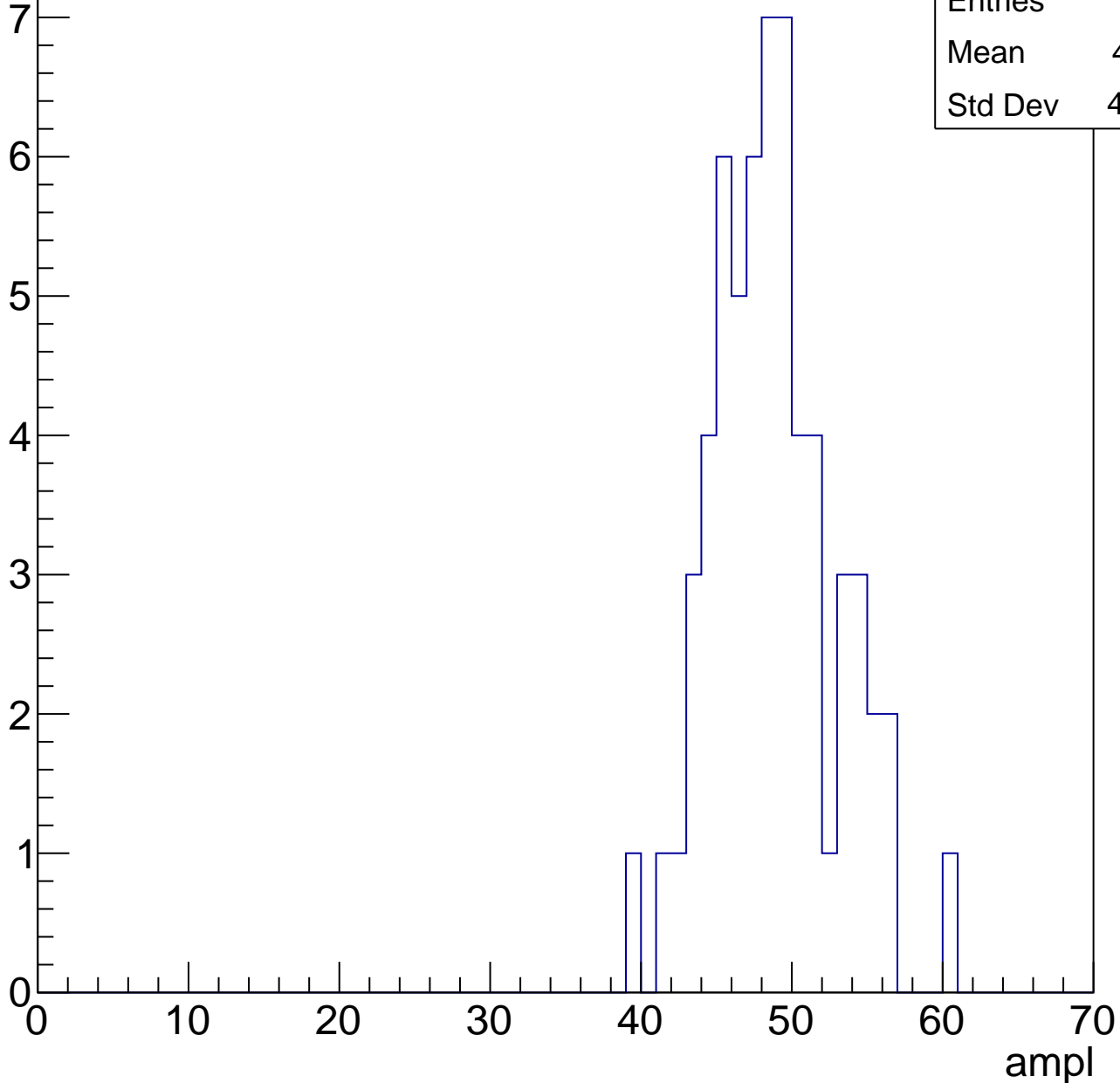


B1L103S, U7-ch118, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	48.31
Std Dev	4.063

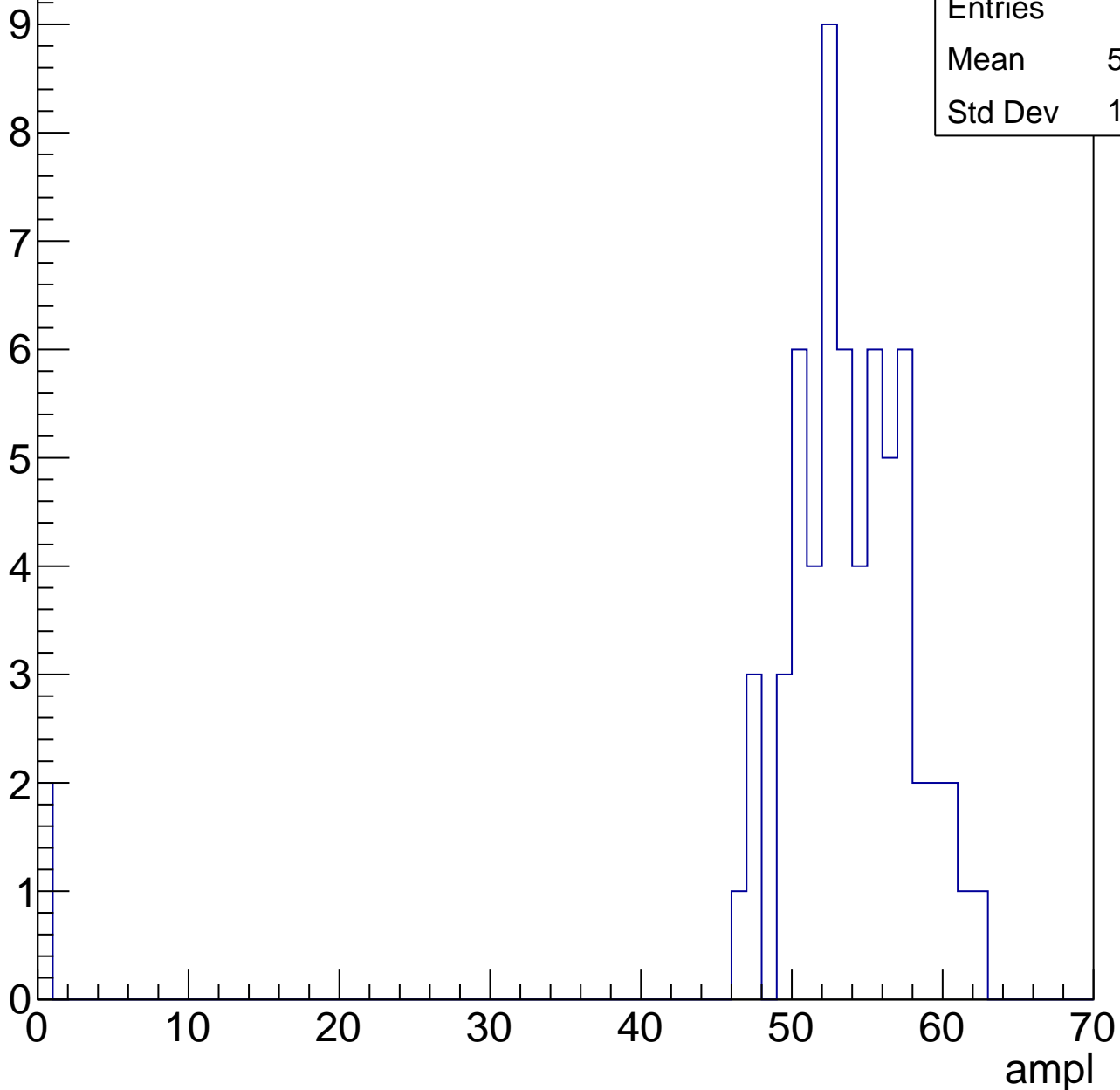


B1L103S, U7-ch118, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	51.89
Std Dev	10.05

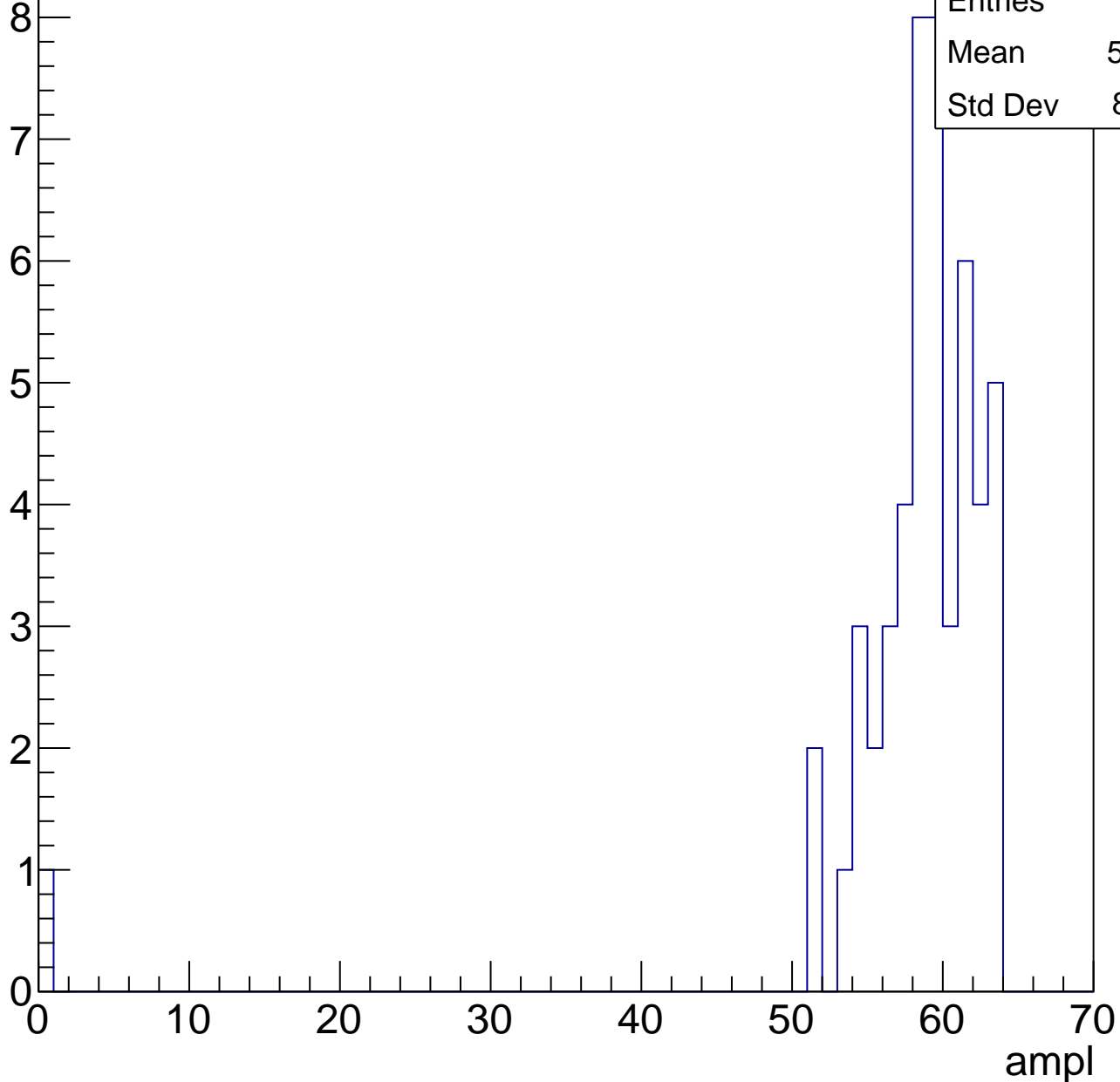


B1L103S, U7-ch118, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	50
Mean	57.36
Std Dev	8.731

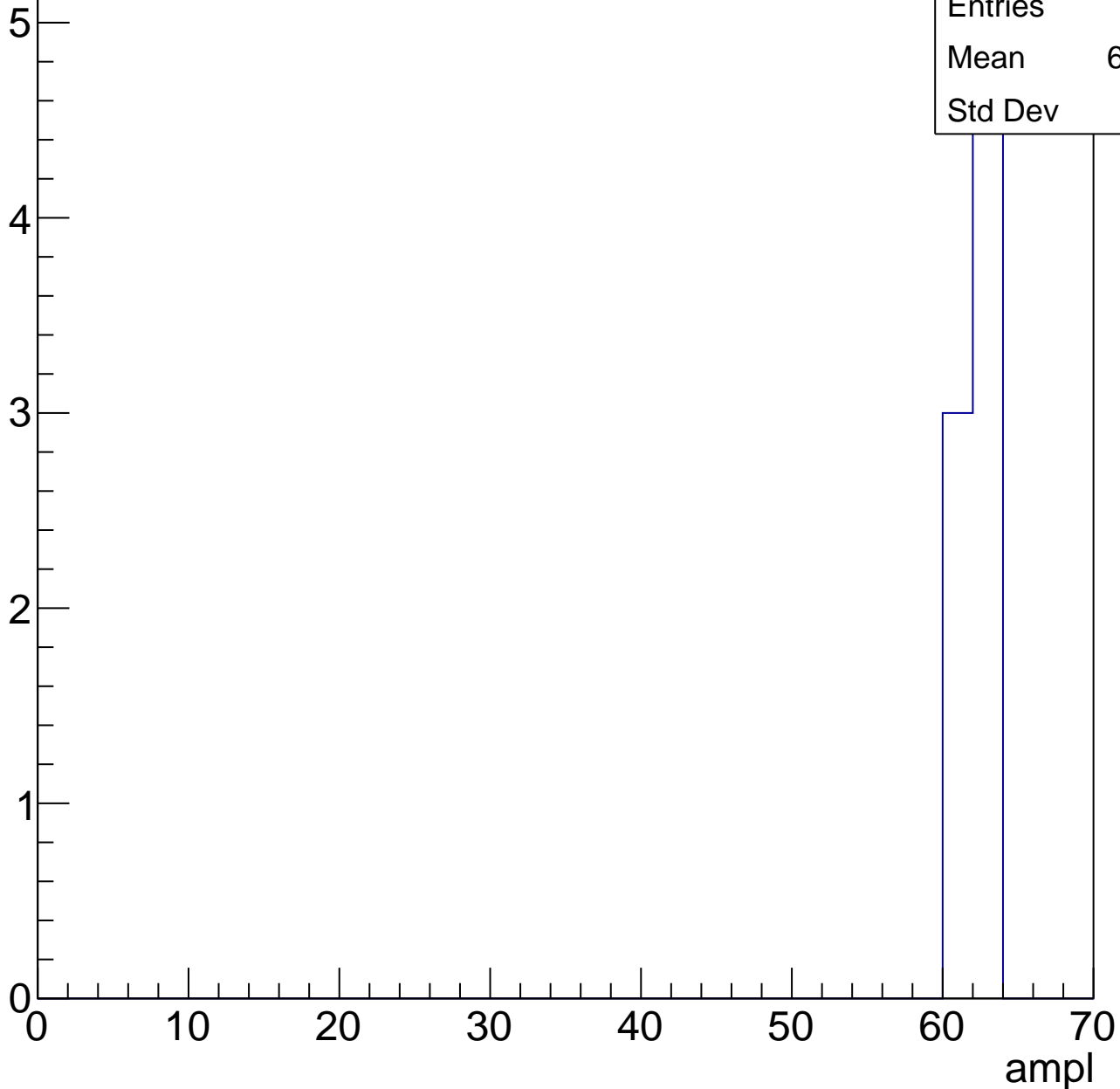


B1L103S, U7-ch118, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

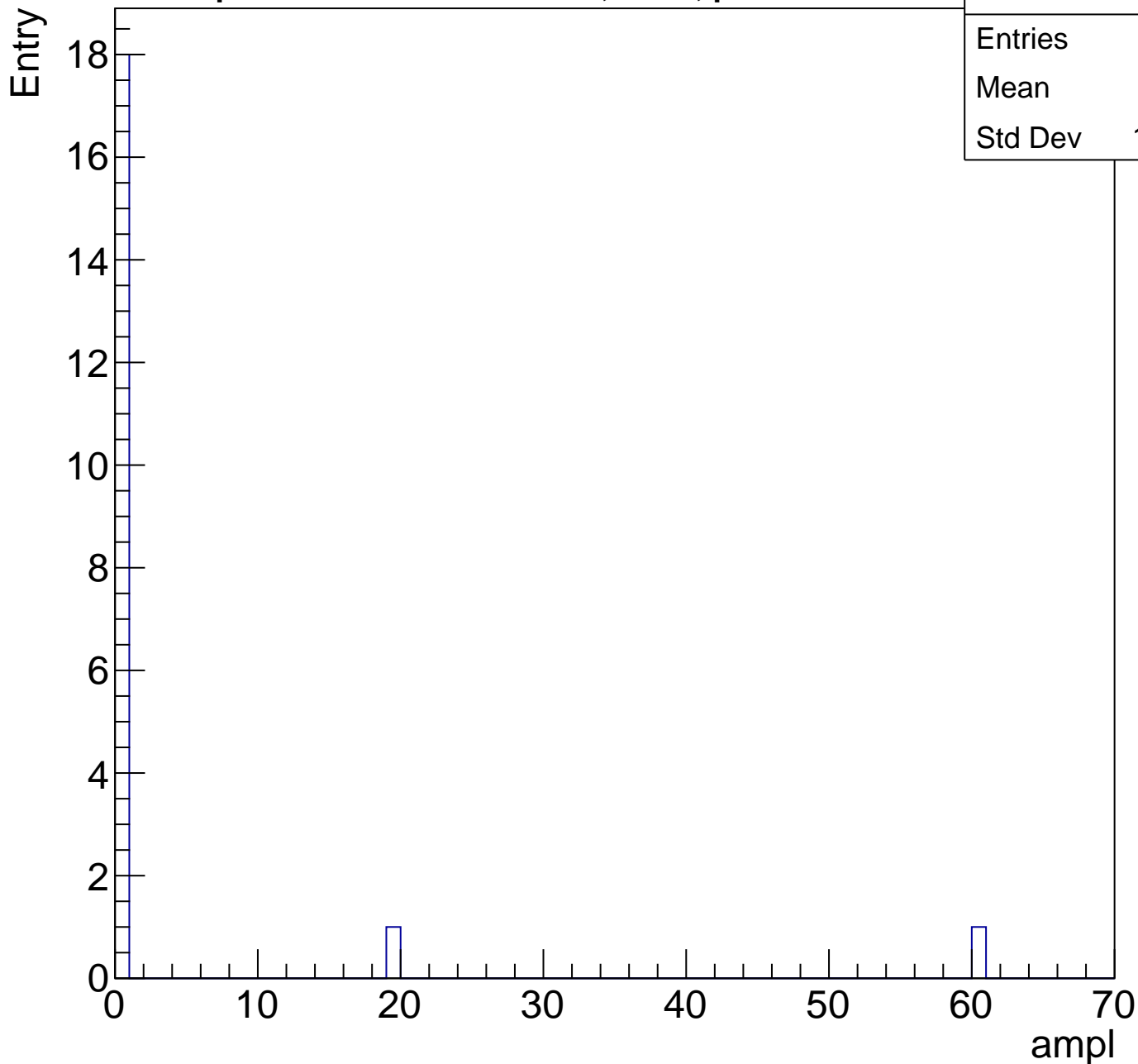
Entries	16
Mean	61.75
Std Dev	1.09



B1L103S, U7-ch118, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.95
Std Dev	13.51



B1L103S, U7-ch119, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	86
Mean	20.38
Std Dev	13.83

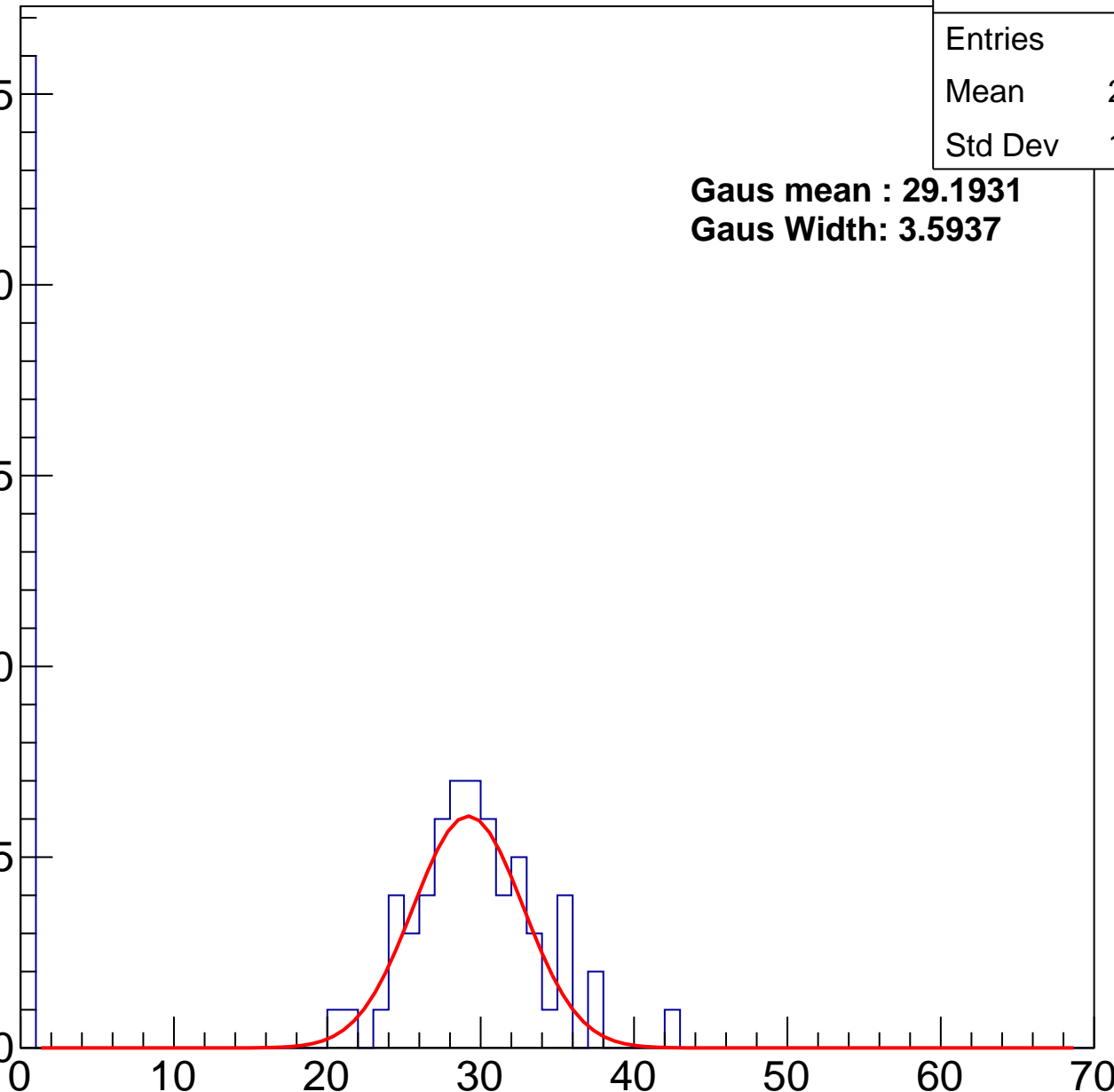
Gaus mean : 29.1931

Gaus Width: 3.5937

Entry

25
20
15
10
5
0

ampl



B1L103S, U7-ch119, adc1

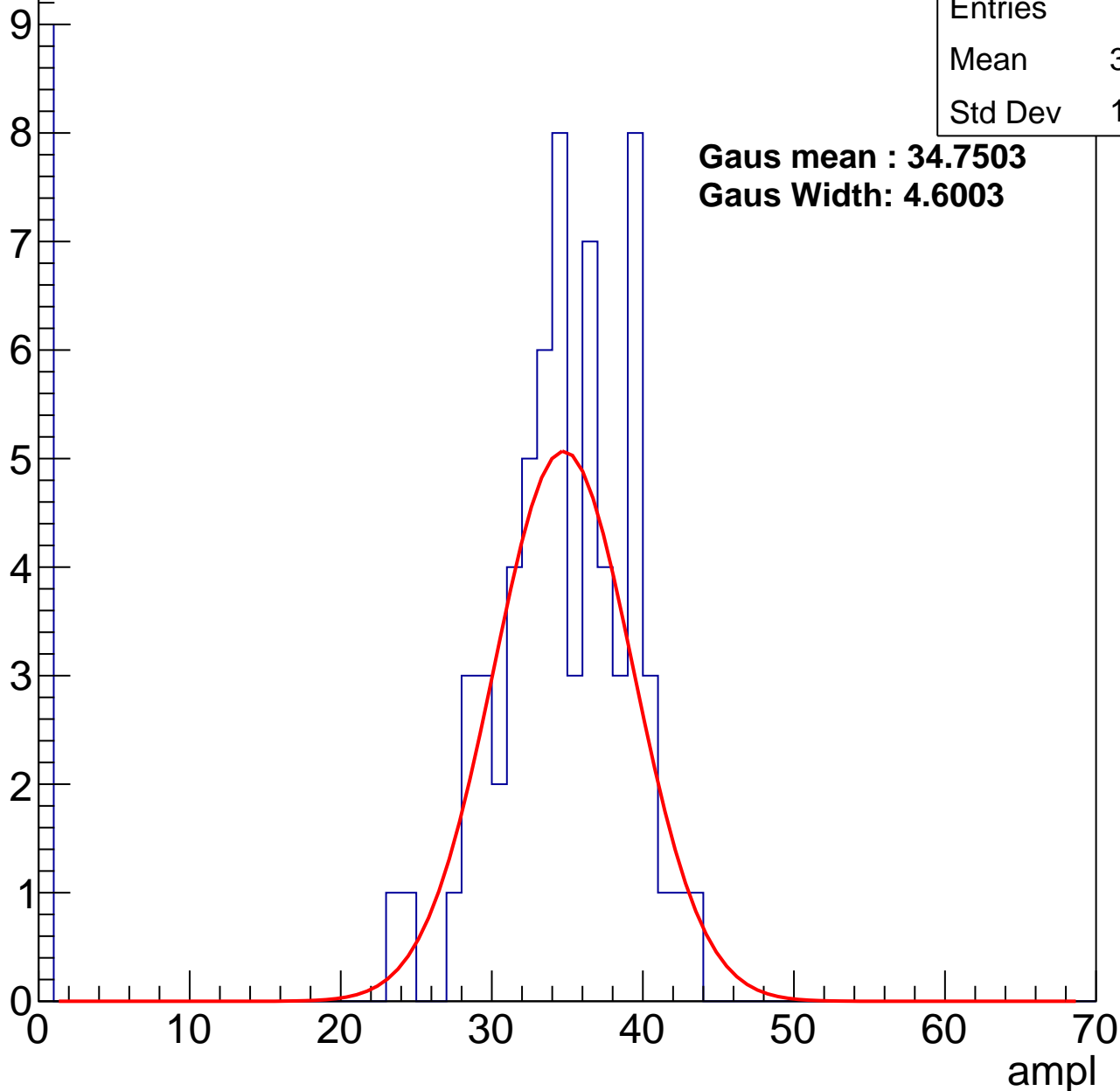
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	74
Mean	30.22
Std Dev	11.92

Gaus mean : 34.7503

Gaus Width: 4.6003



B1L103S, U7-ch119, adc2

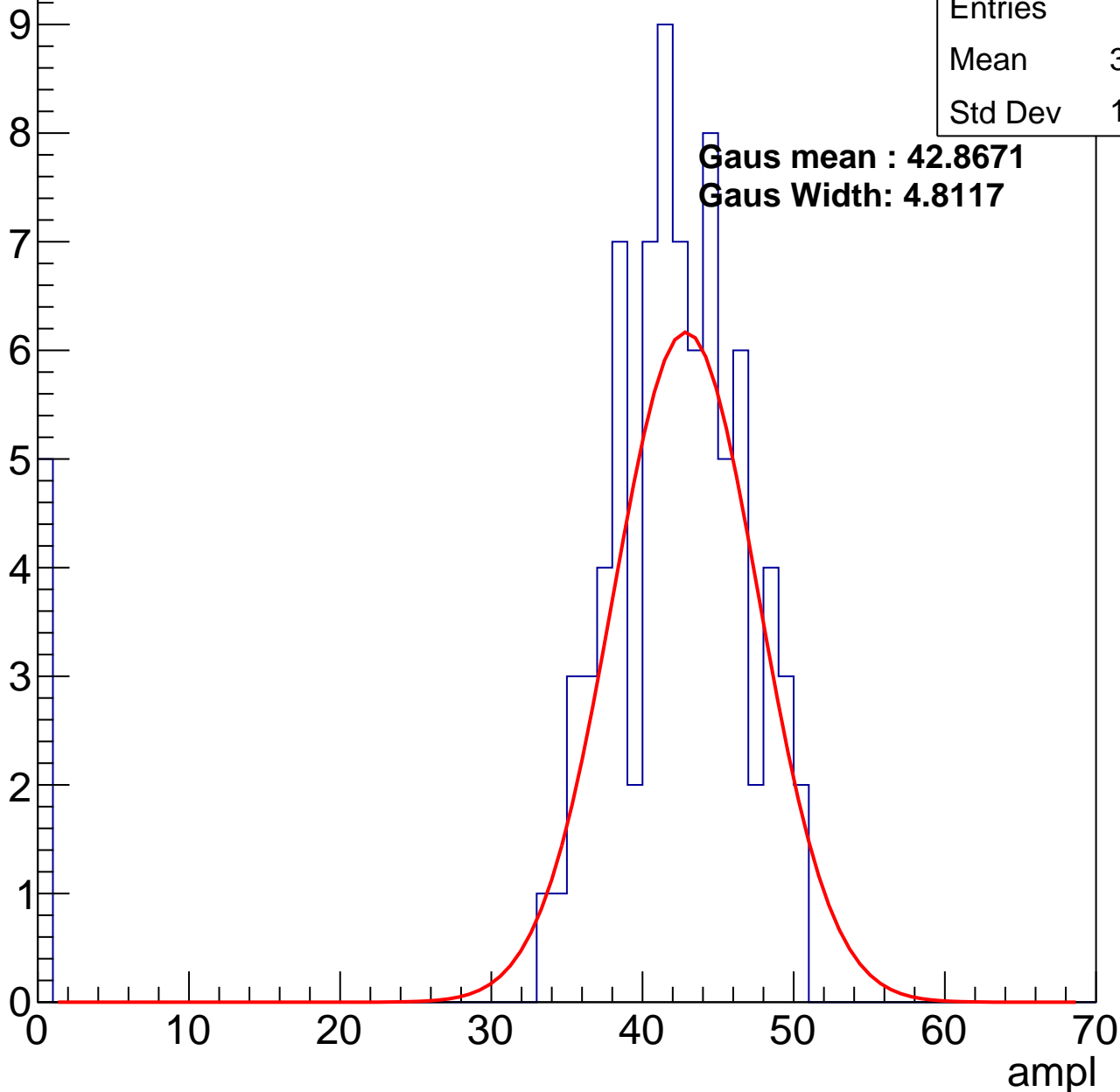
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	85
Mean	39.52
Std Dev	10.63

Gaus mean : 42.8671

Gaus Width: 4.8117

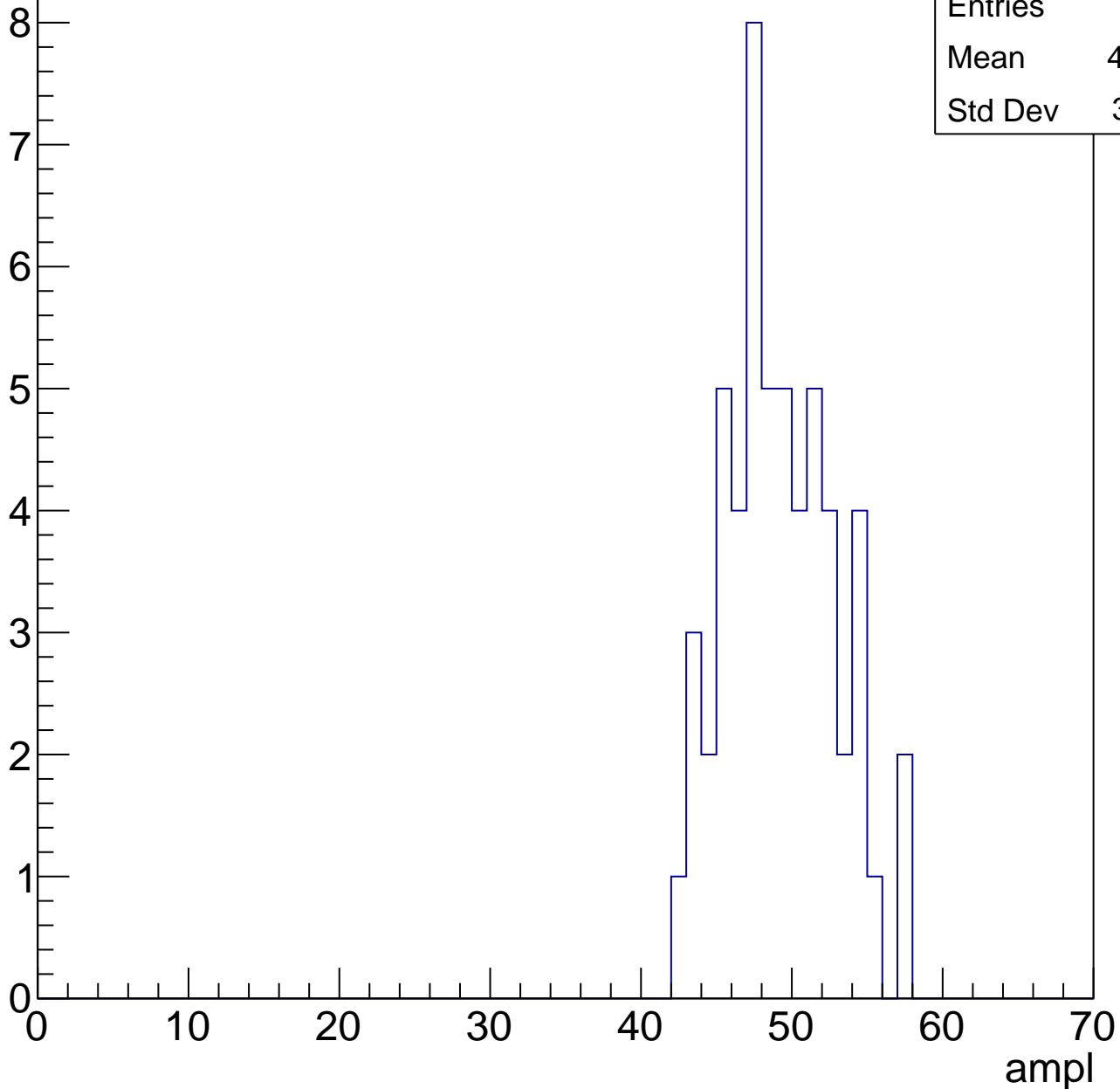


B1L103S, U7-ch119, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	55
Mean	48.78
Std Dev	3.601

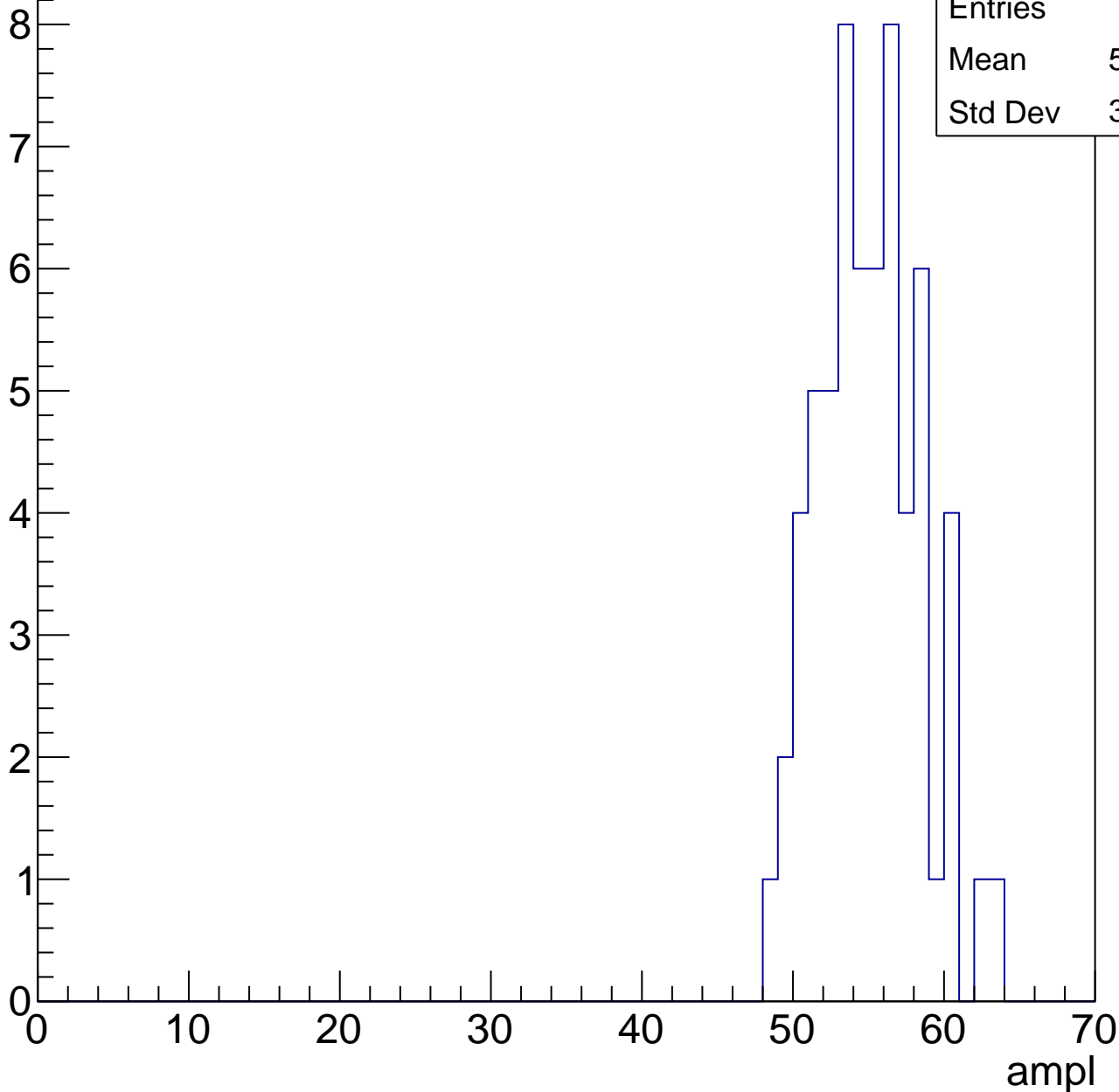


B1L103S, U7-ch119, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

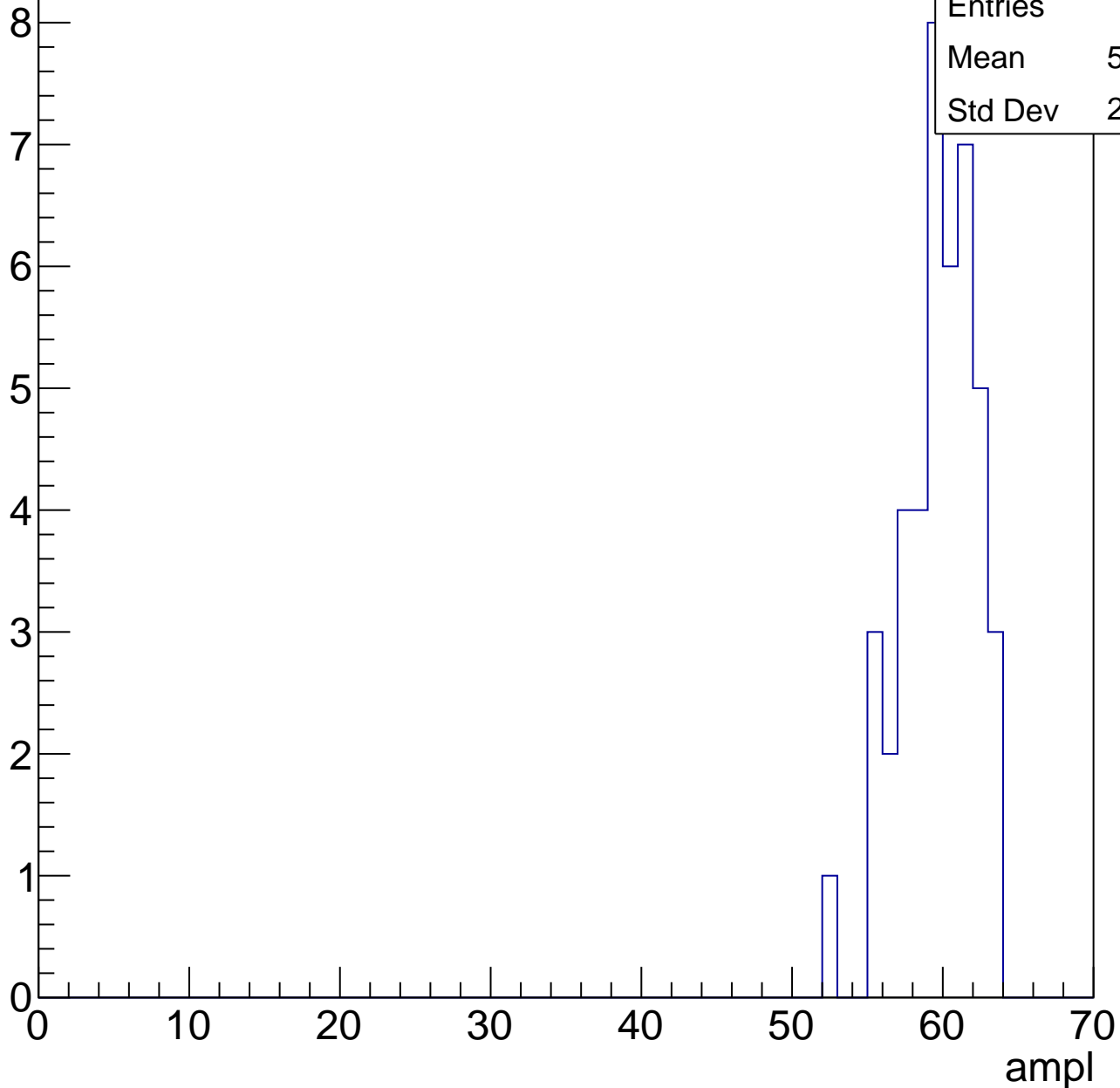
Entries	62
Mean	54.63
Std Dev	3.318



B1L103S, U7-ch119, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

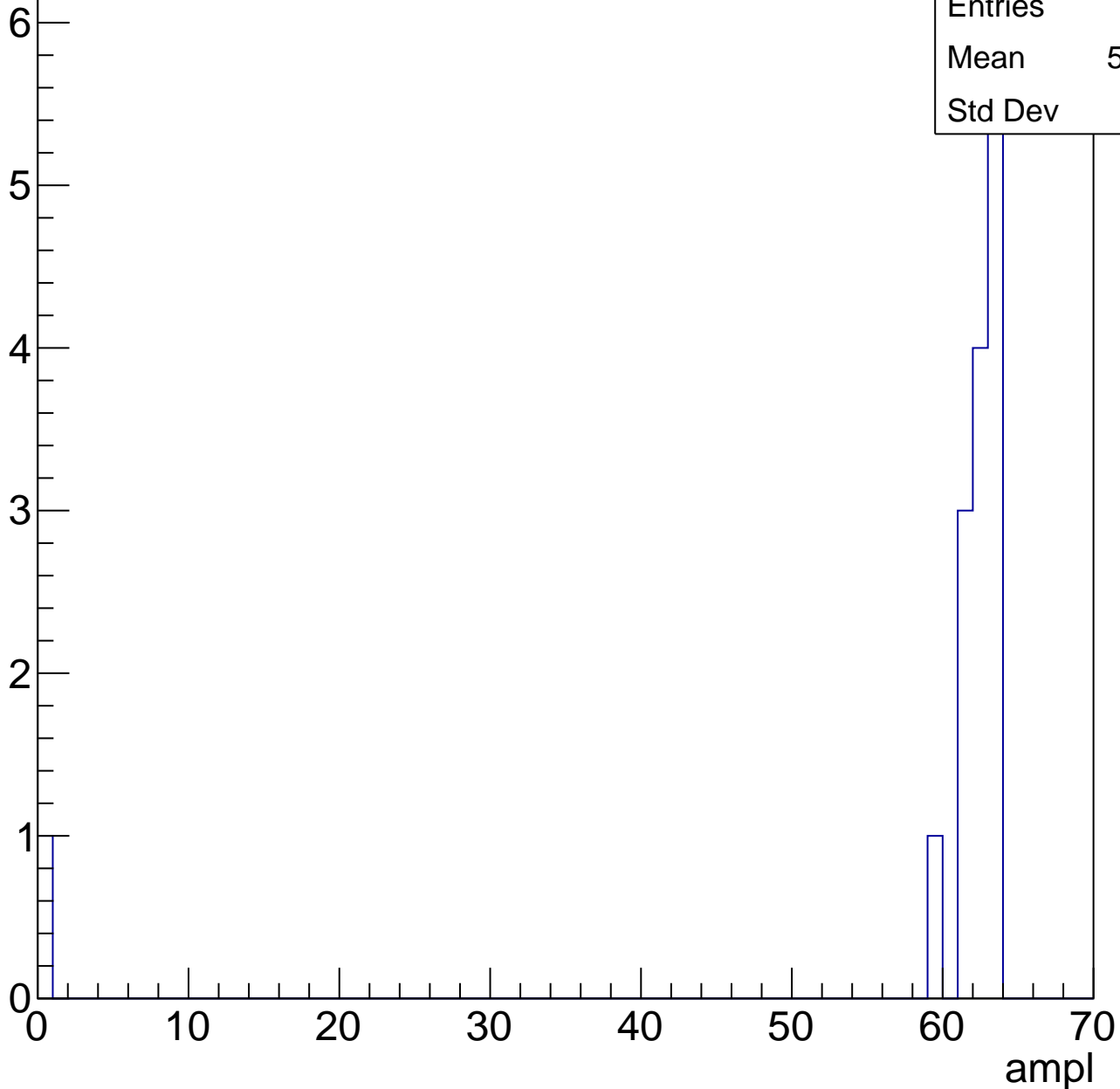


B1L103S, U7-ch119, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	15
Mean	57.87
Std Dev	15.5



B1L103S, U7-ch119, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U7-ch120, adc0

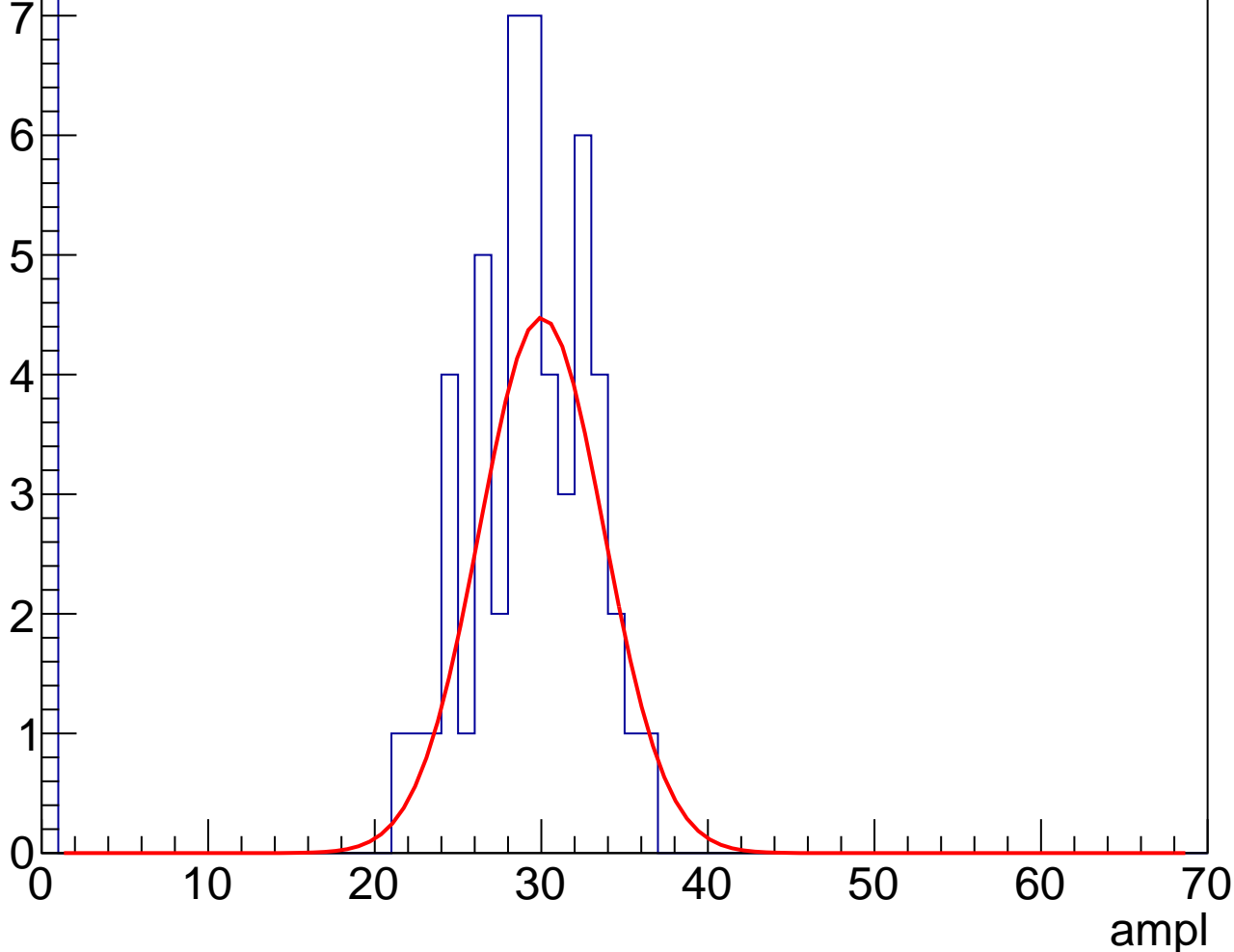
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	59
Mean	24.51
Std Dev	10.87

Gaus mean : 30.0218

Gaus Width: 3.7237



B1L103S, U7-ch120, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	33.44
Std Dev	8.972

Gaus mean : 36.3776

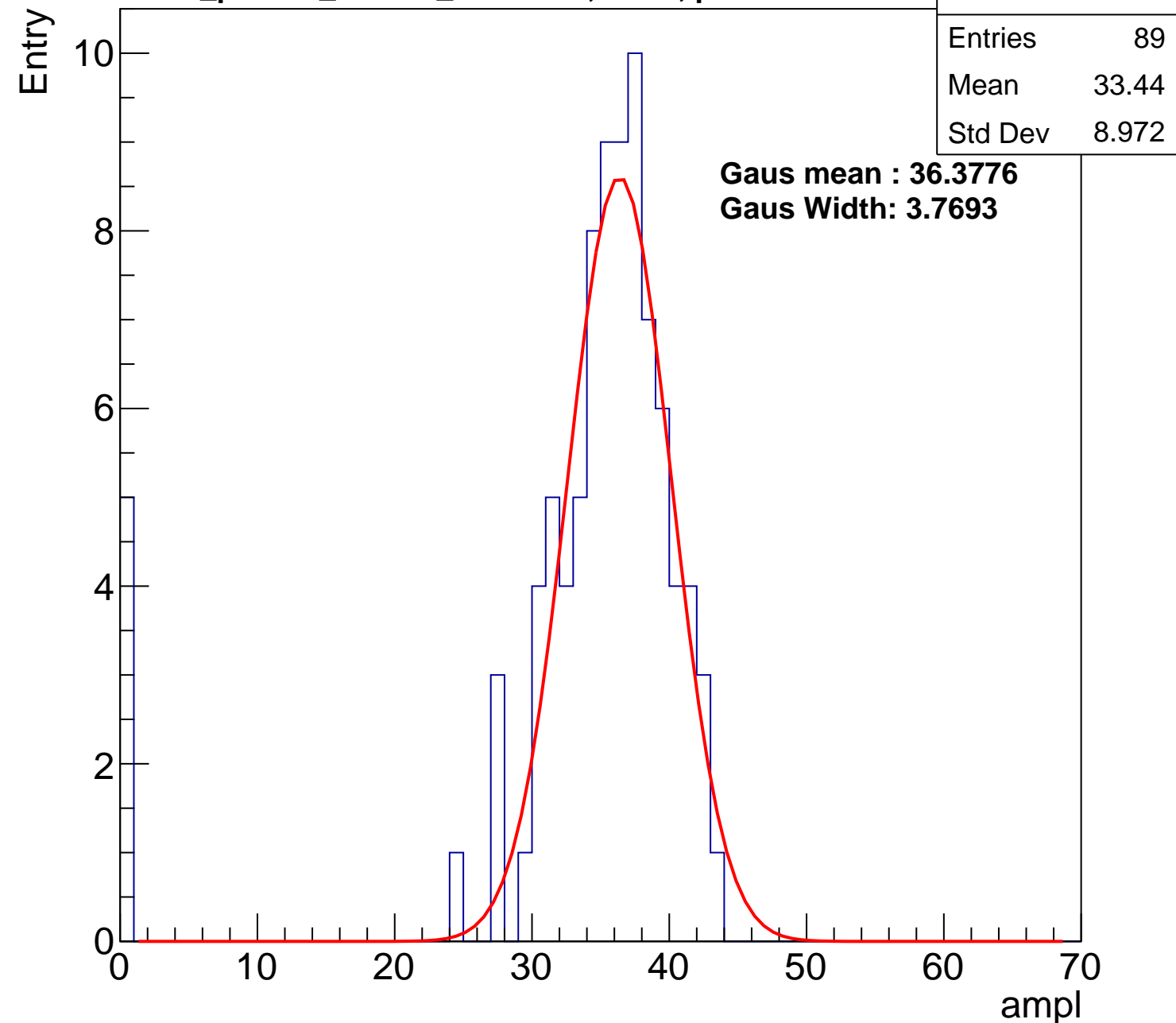
Gaus Width: 3.7693

Entry

10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U7-ch120, adc2

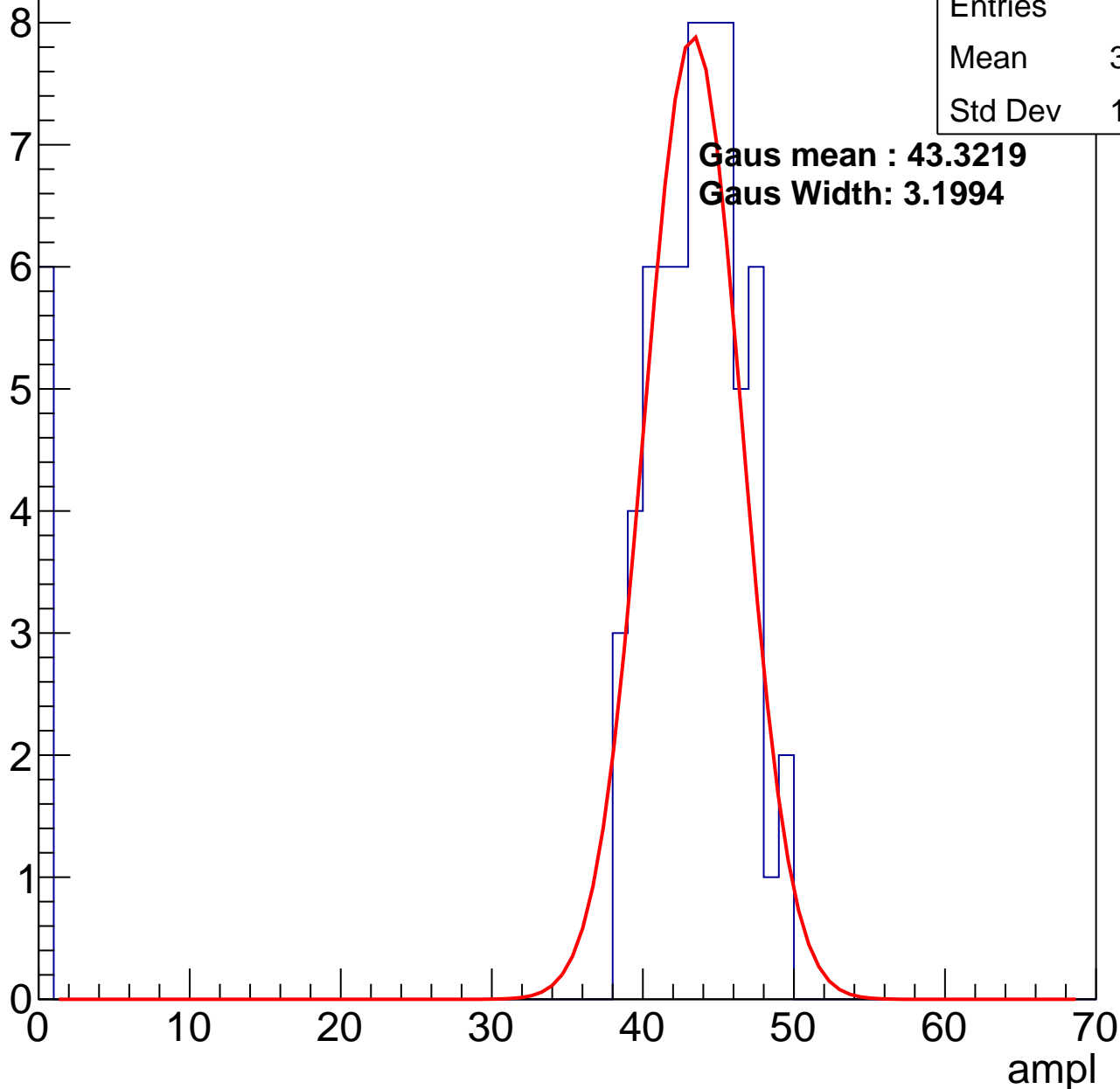
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	39.45
Std Dev	12.47

Gaus mean : 43.3219

Gaus Width: 3.1994

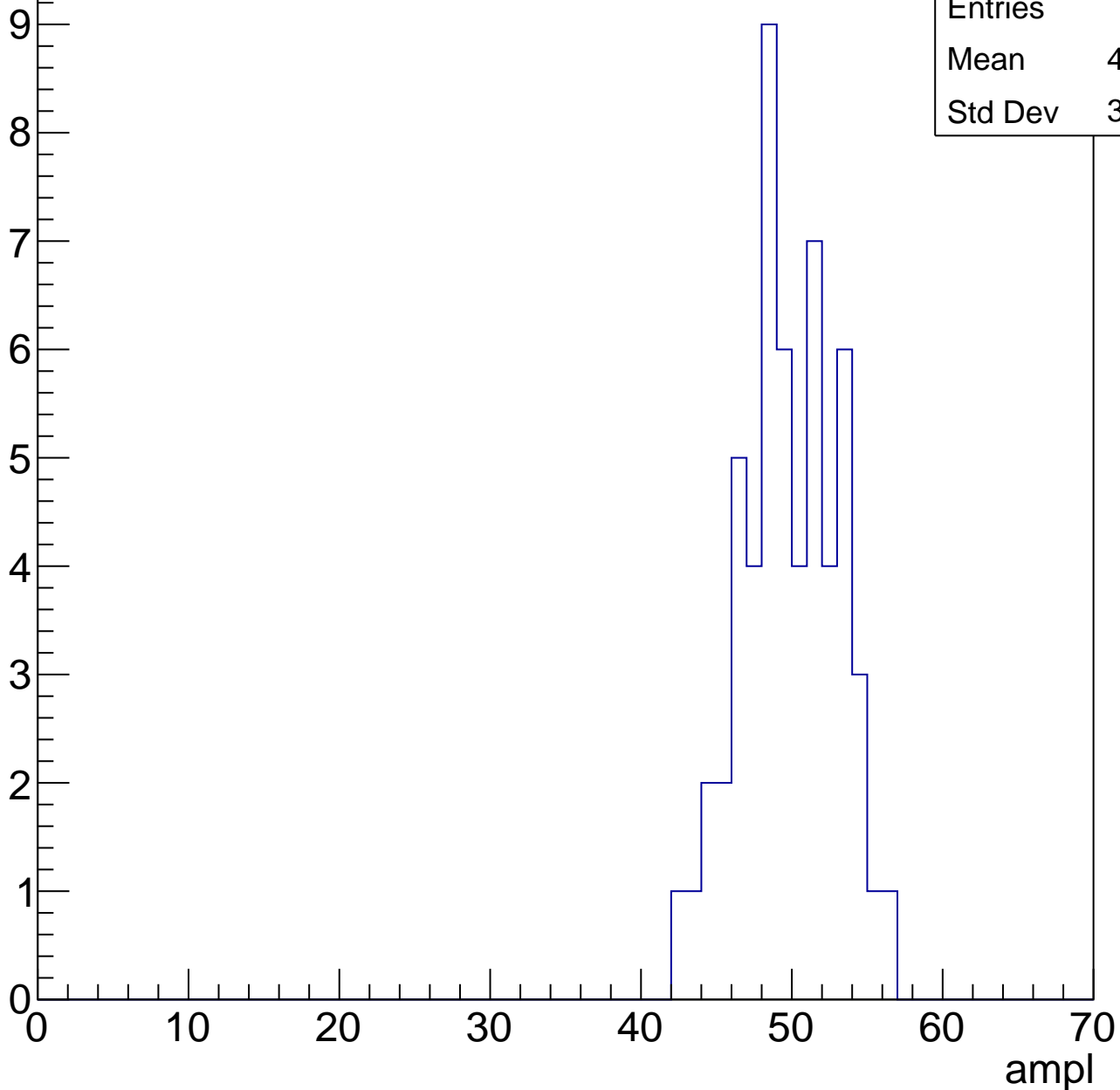


B1L103S, U7-ch120, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	49.34
Std Dev	3.147

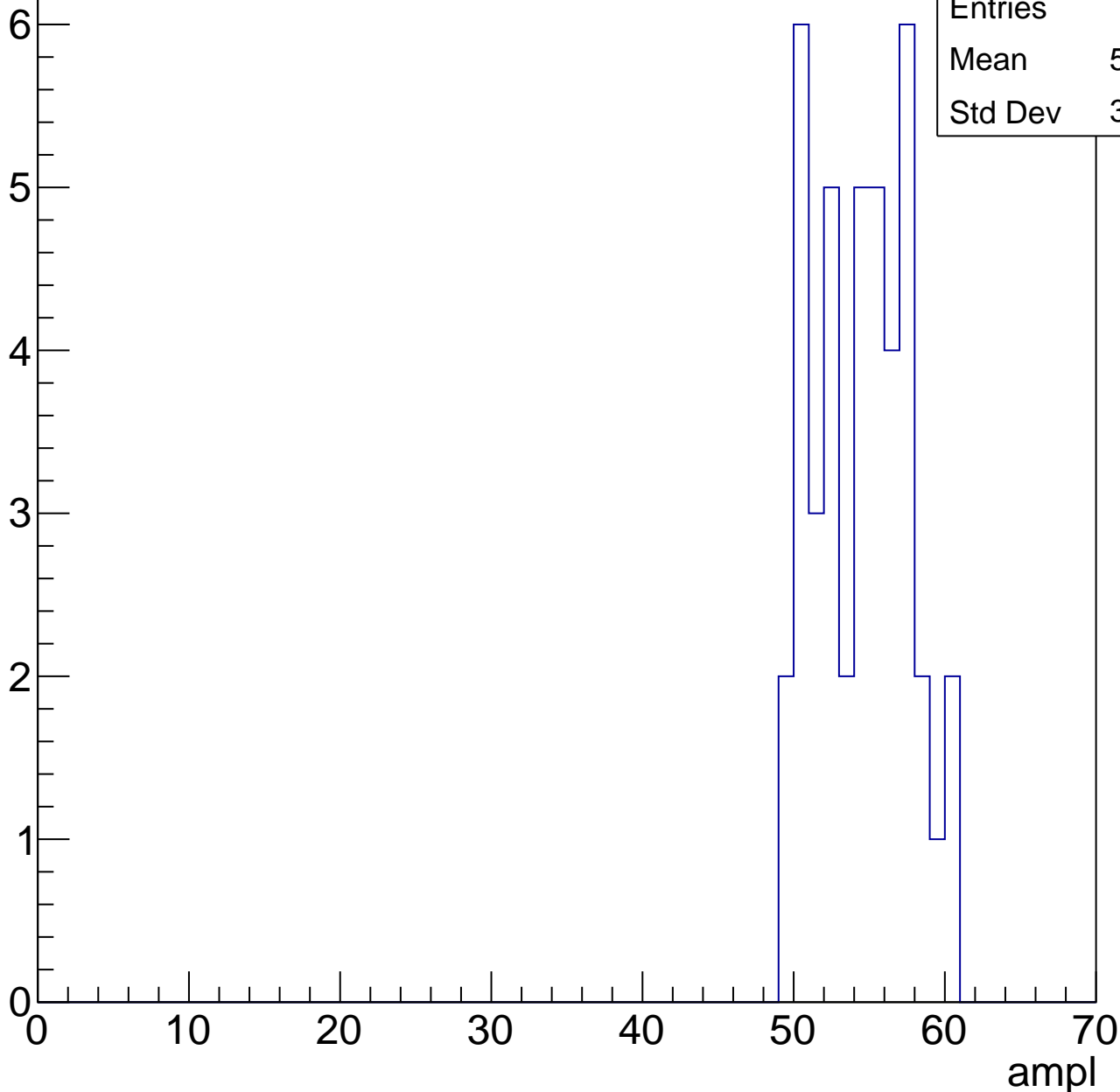


B1L103S, U7-ch120, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	43
Mean	54.02
Std Dev	3.046

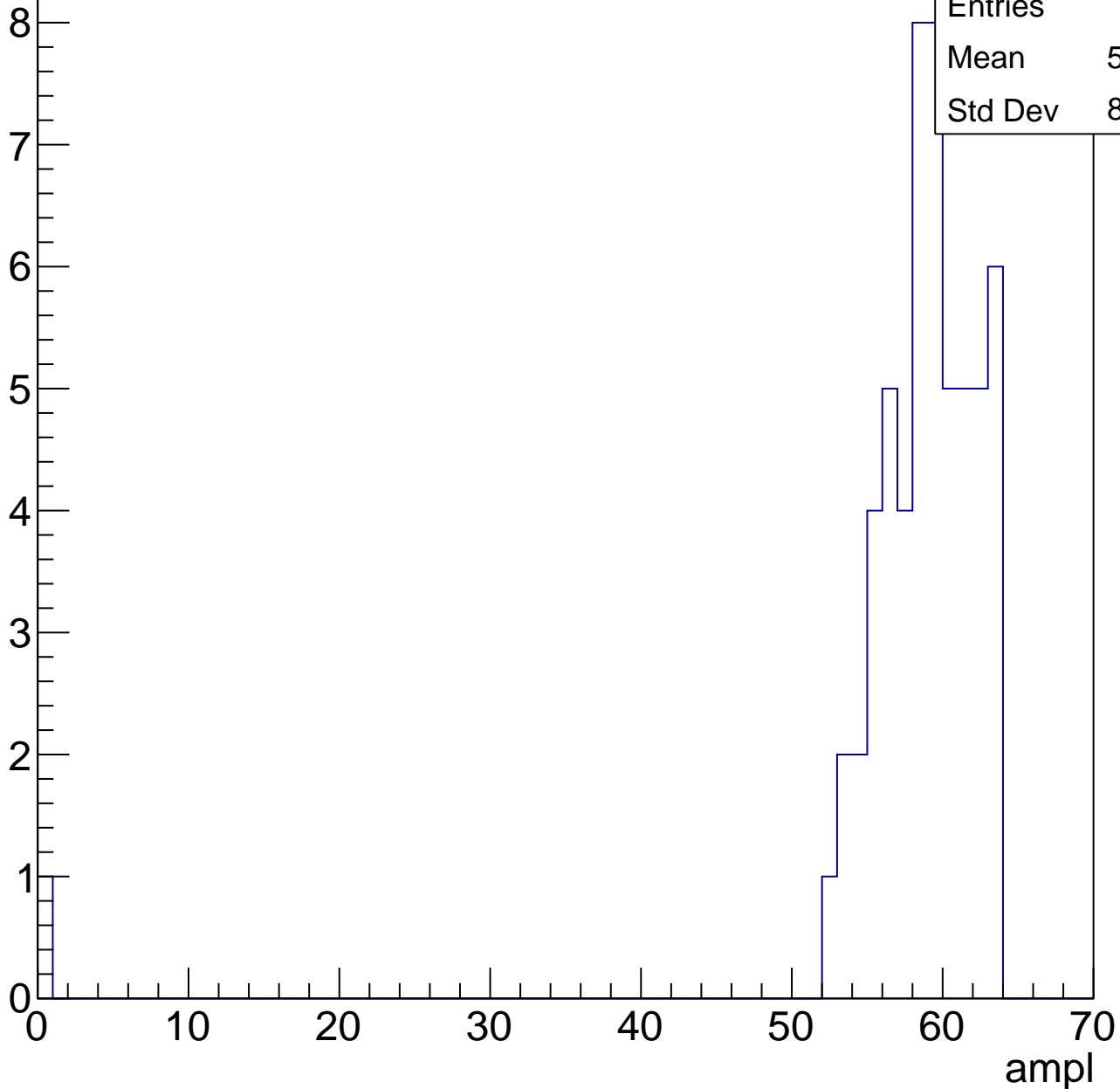


B1L103S, U7-ch120, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	56
Mean	57.55
Std Dev	8.274

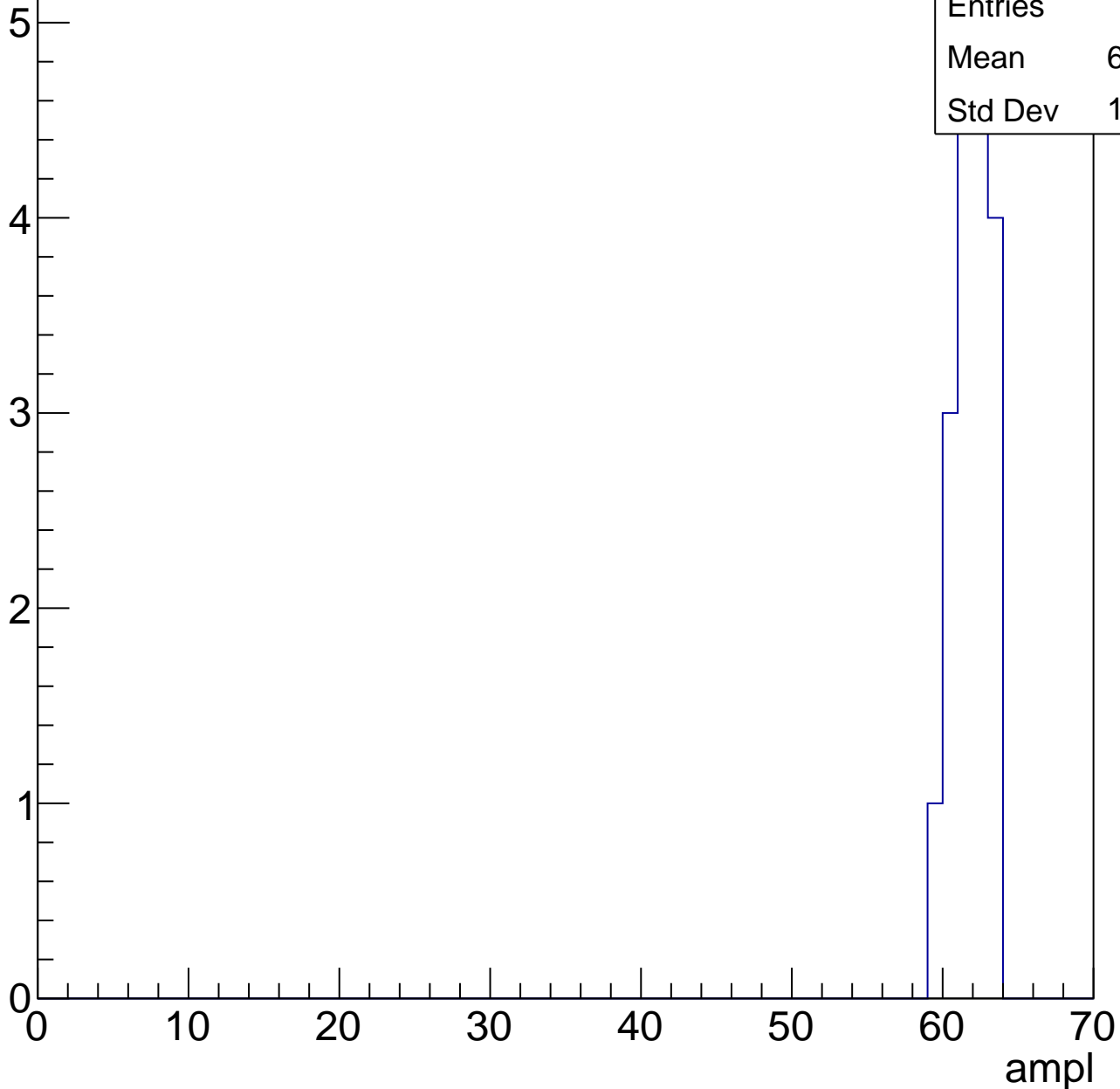


B1L103S, U7-ch120, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	18
Mean	61.44
Std Dev	1.165



B1L103S, U7-ch120, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entry

18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl

Entries	19
Mean	0
Std Dev	0

B1L103S, U7-ch121, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	85
Mean	25.67
Std Dev	8.914

Gaus mean : 28.7996

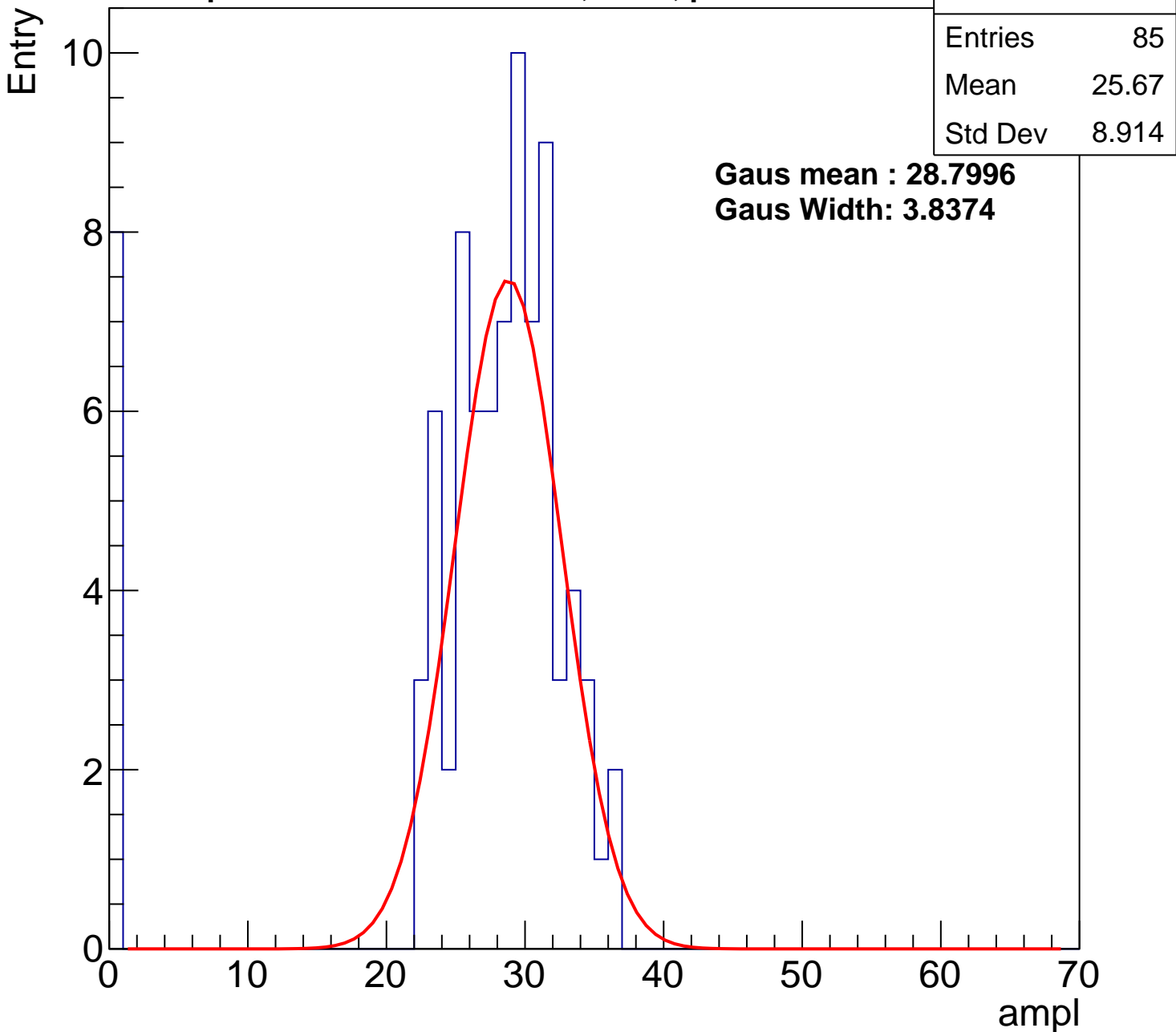
Gaus Width: 3.8374

Entry

10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U7-ch121, adc1

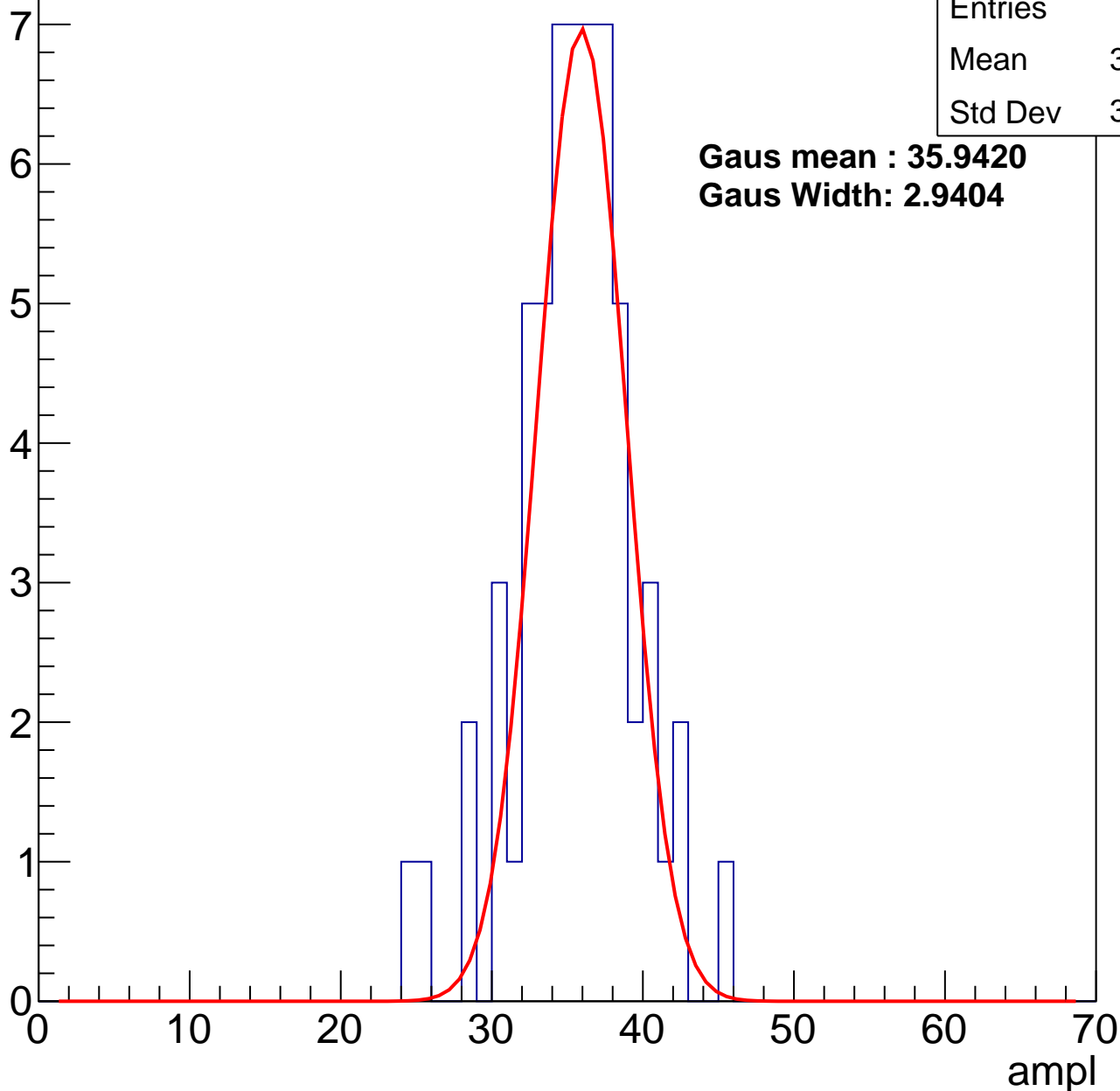
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	60
Mean	35.05
Std Dev	3.879

Gaus mean : 35.9420

Gaus Width: 2.9404



B1L103S, U7-ch121, adc2

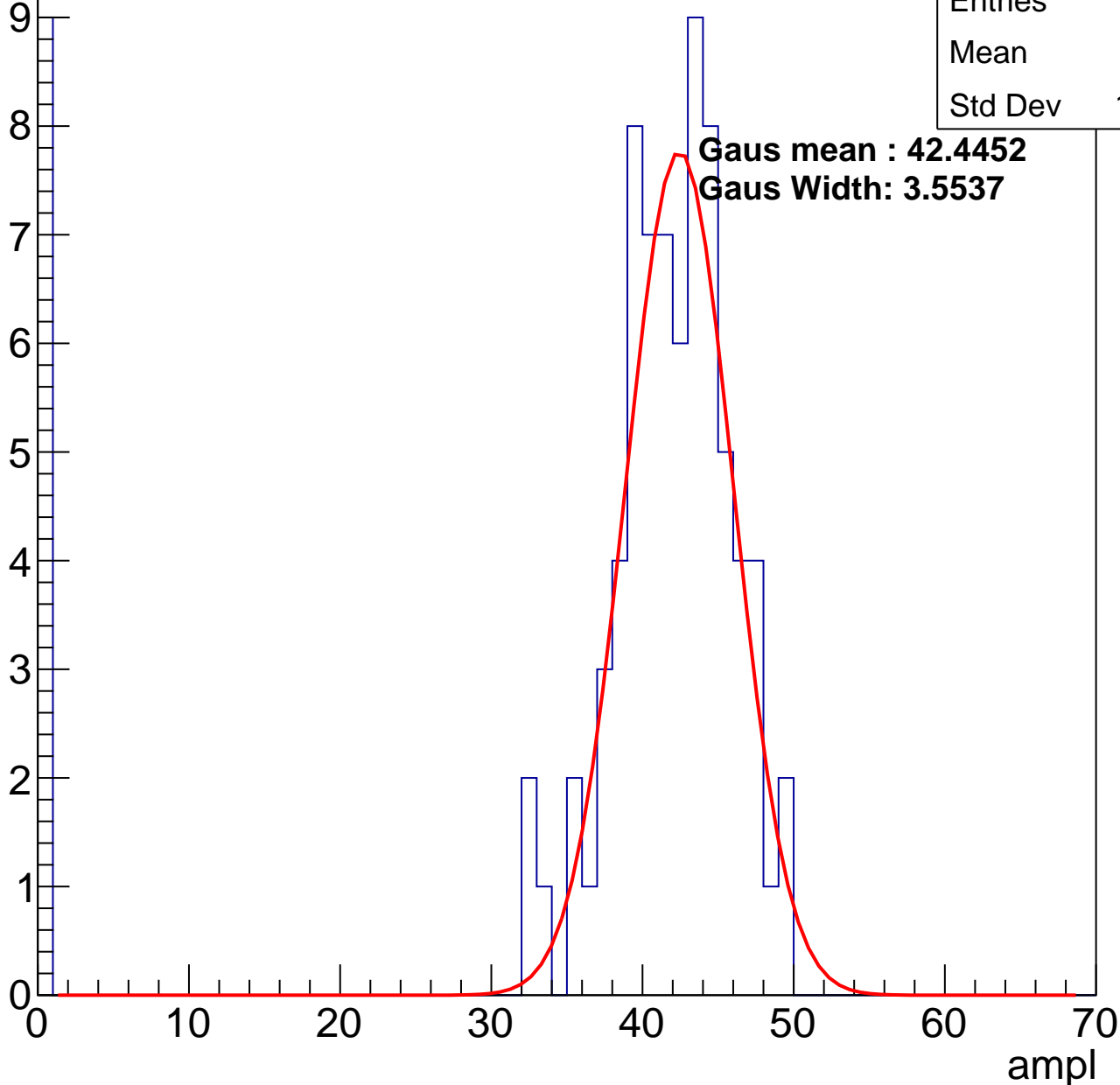
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	83
Mean	37.1
Std Dev	13.41

Gaus mean : 42.4452

Gaus Width: 3.5537

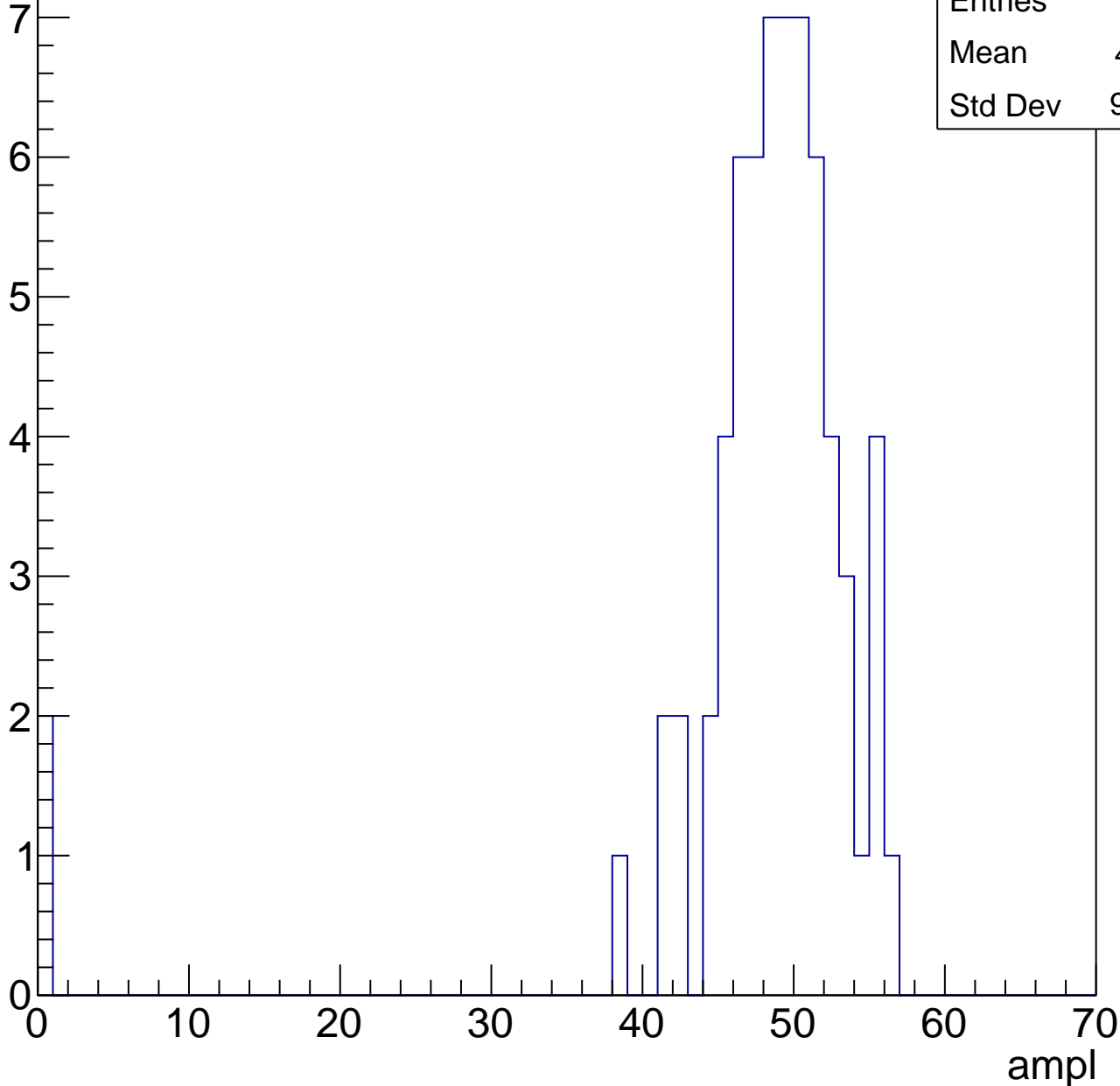


B1L103S, U7-ch121, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	65
Mean	47.11
Std Dev	9.155

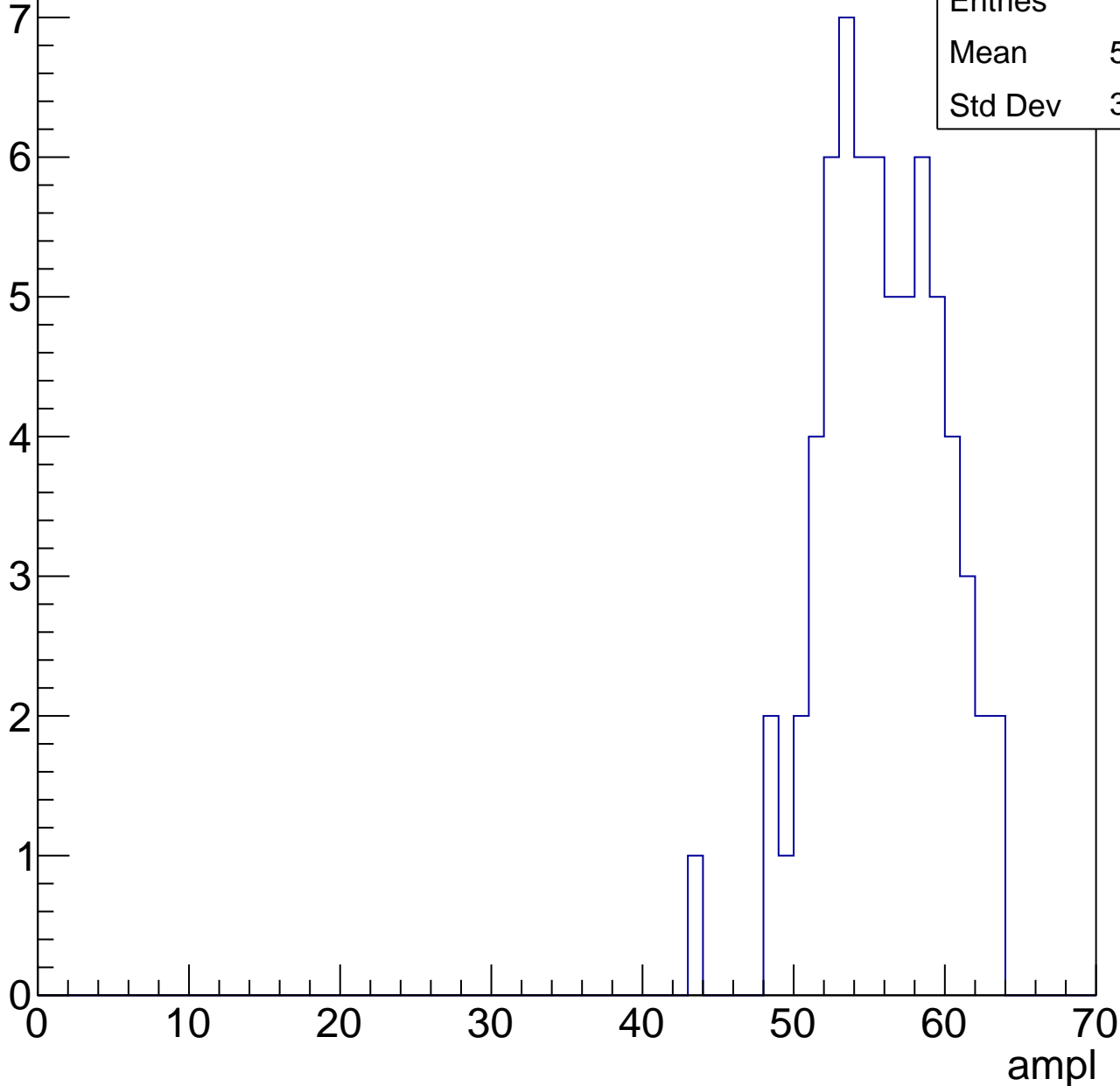


B1L103S, U7-ch121, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	67
Mean	55.37
Std Dev	3.984



B1L103S, U7-ch121, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

6

5

4

3

2

1

0

Entries

37

Mean

58.46

Std Dev

2.747

ampl

0

10

20

30

40

50

60

70

50

55

40

30

20

10

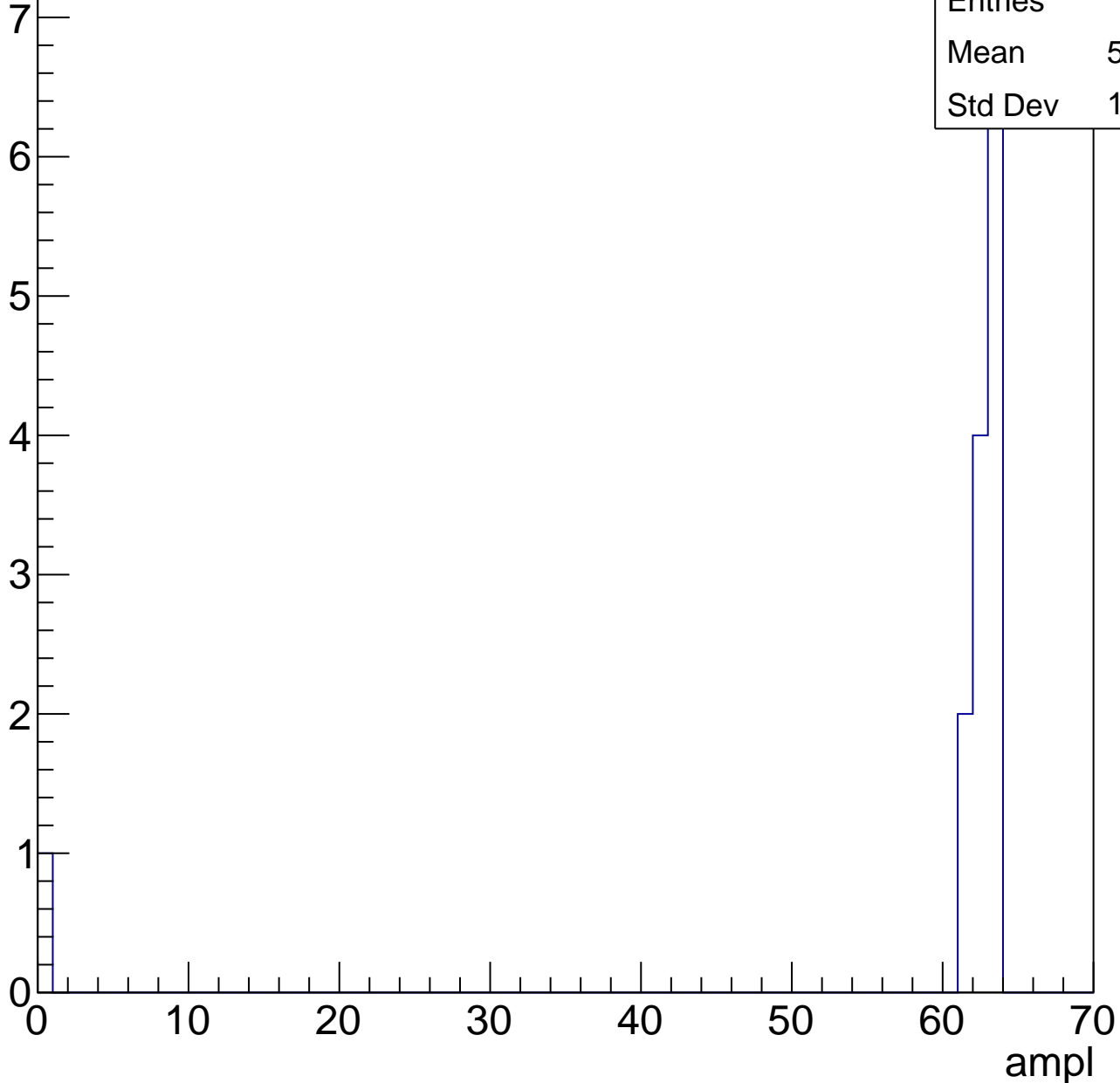
0

B1L103S, U7-ch121, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	14
Mean	57.93
Std Dev	16.08

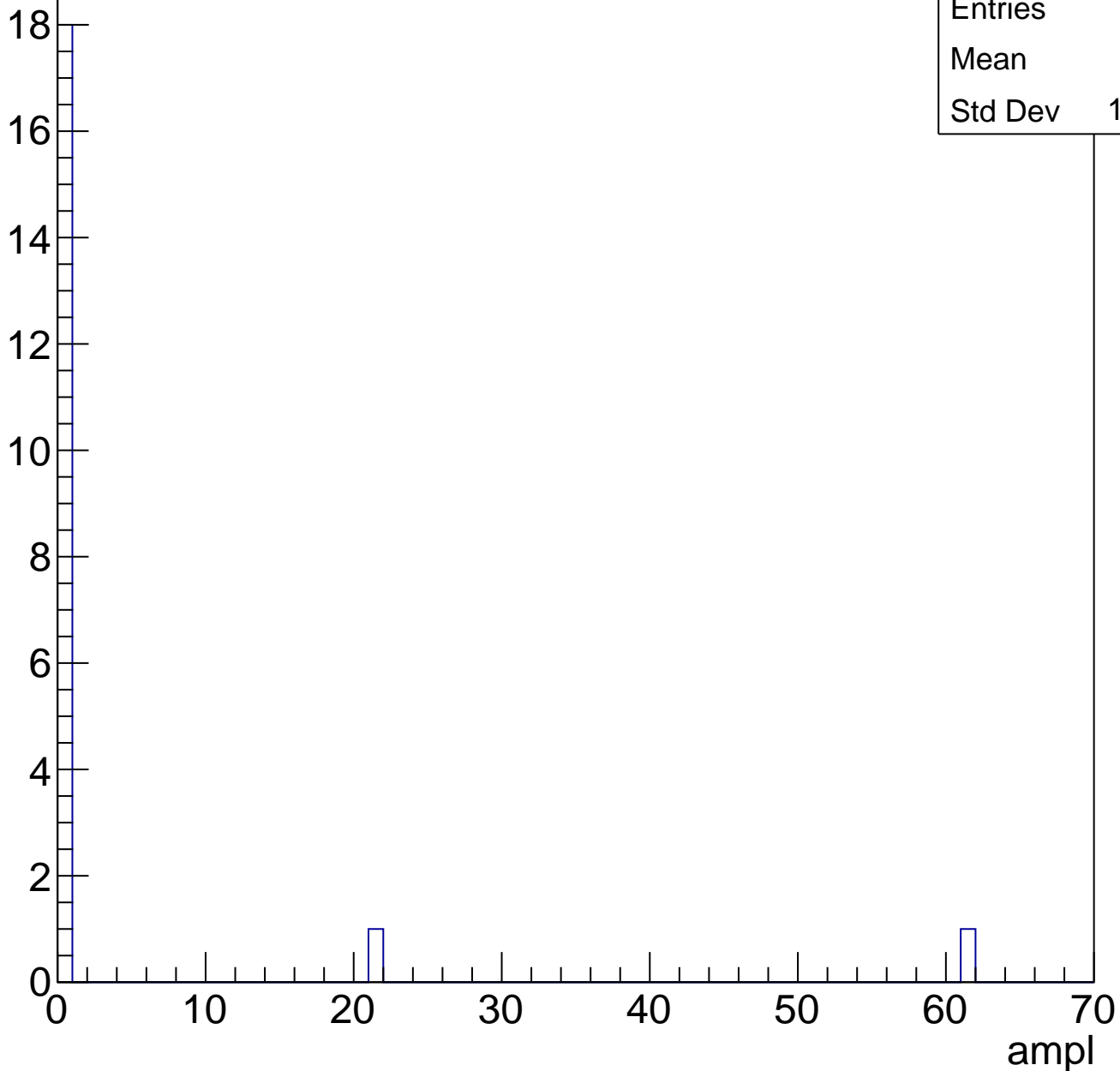


B1L103S, U7-ch121, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	4.1
Std Dev	13.83

Entry



B1L103S, U7-ch122, adc0

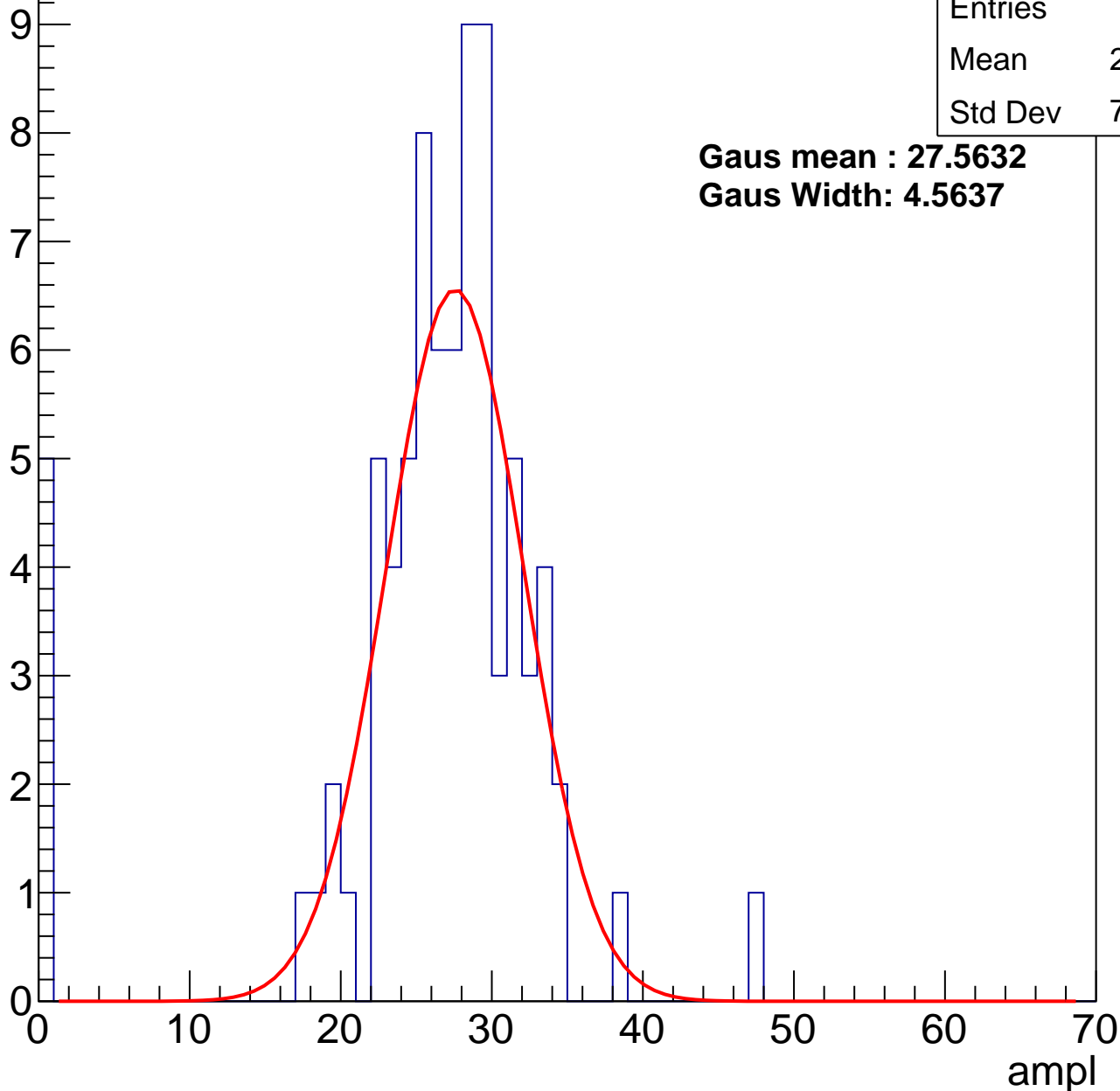
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	81
Mean	25.58
Std Dev	7.936

Gaus mean : 27.5632

Gaus Width: 4.5637



B1L103S, U7-ch122, adc1

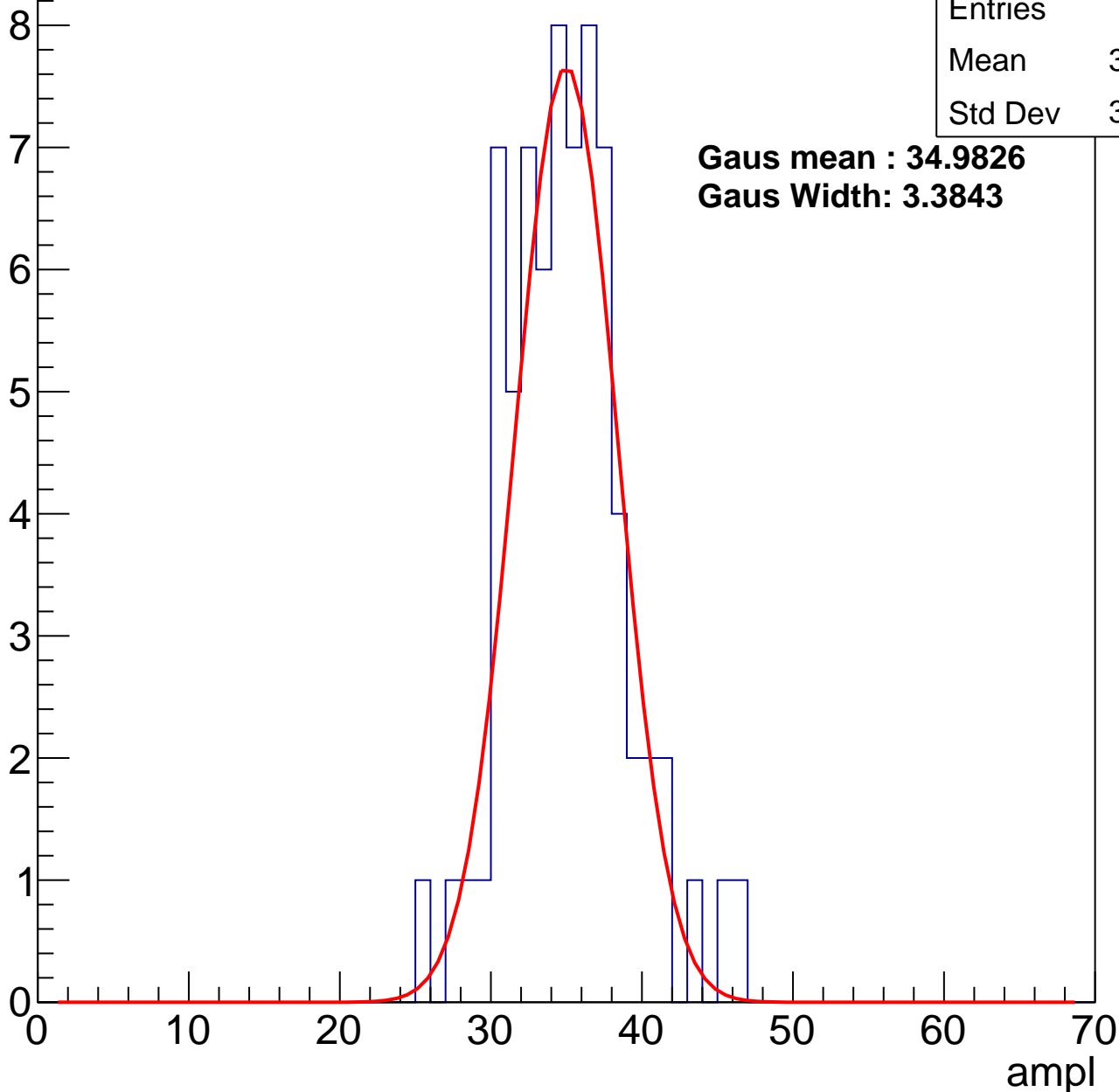
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	72
Mean	34.53
Std Dev	3.898

Gaus mean : 34.9826

Gaus Width: 3.3843



B1L103S, U7-ch122, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	75
Mean	35.67
Std Dev	14.31

Gaus mean : 42.1513

Gaus Width: 4.1592

Entry

10

8

6

4

2

0

0

10

20

30

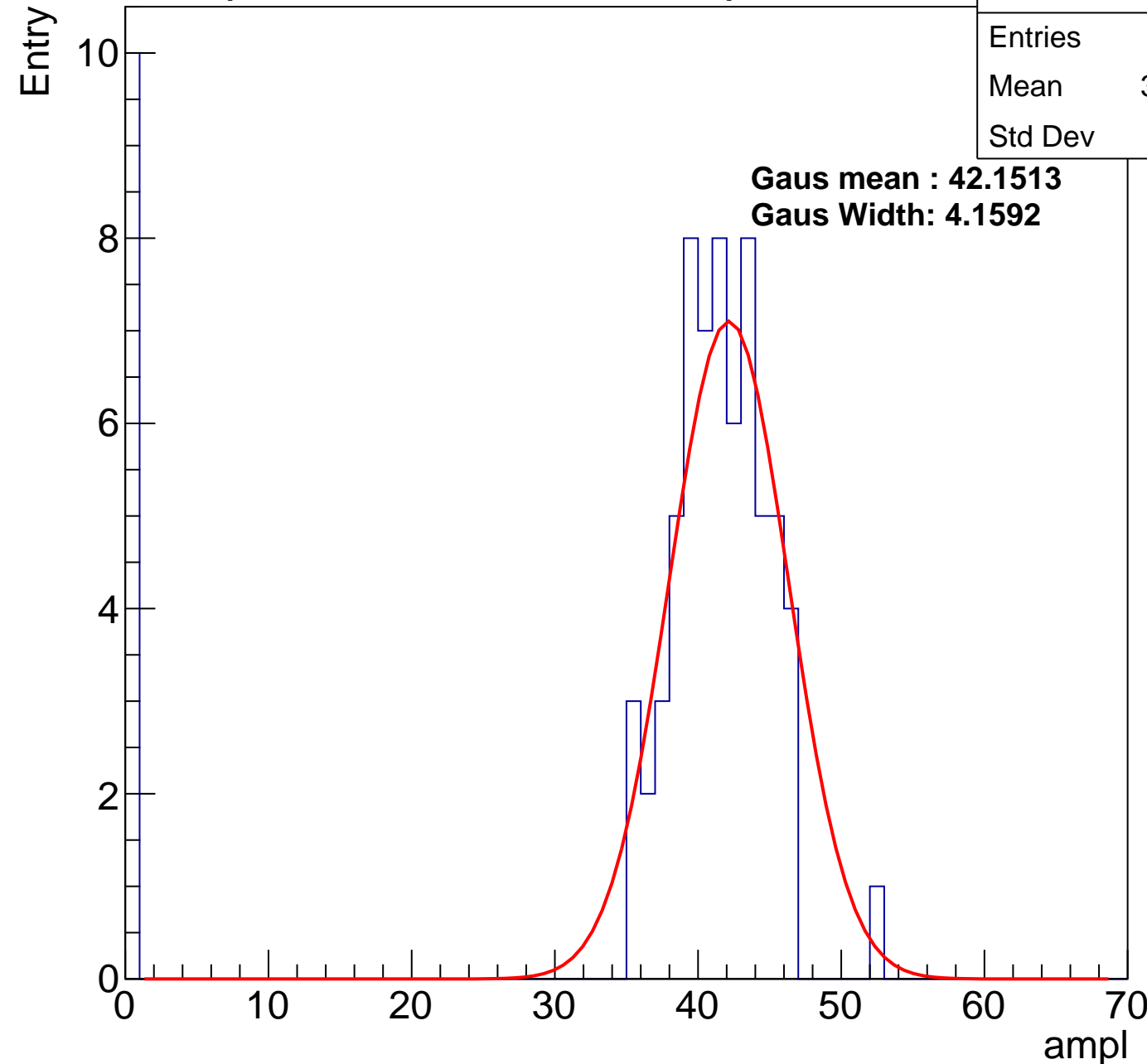
40

50

60

70

ampl

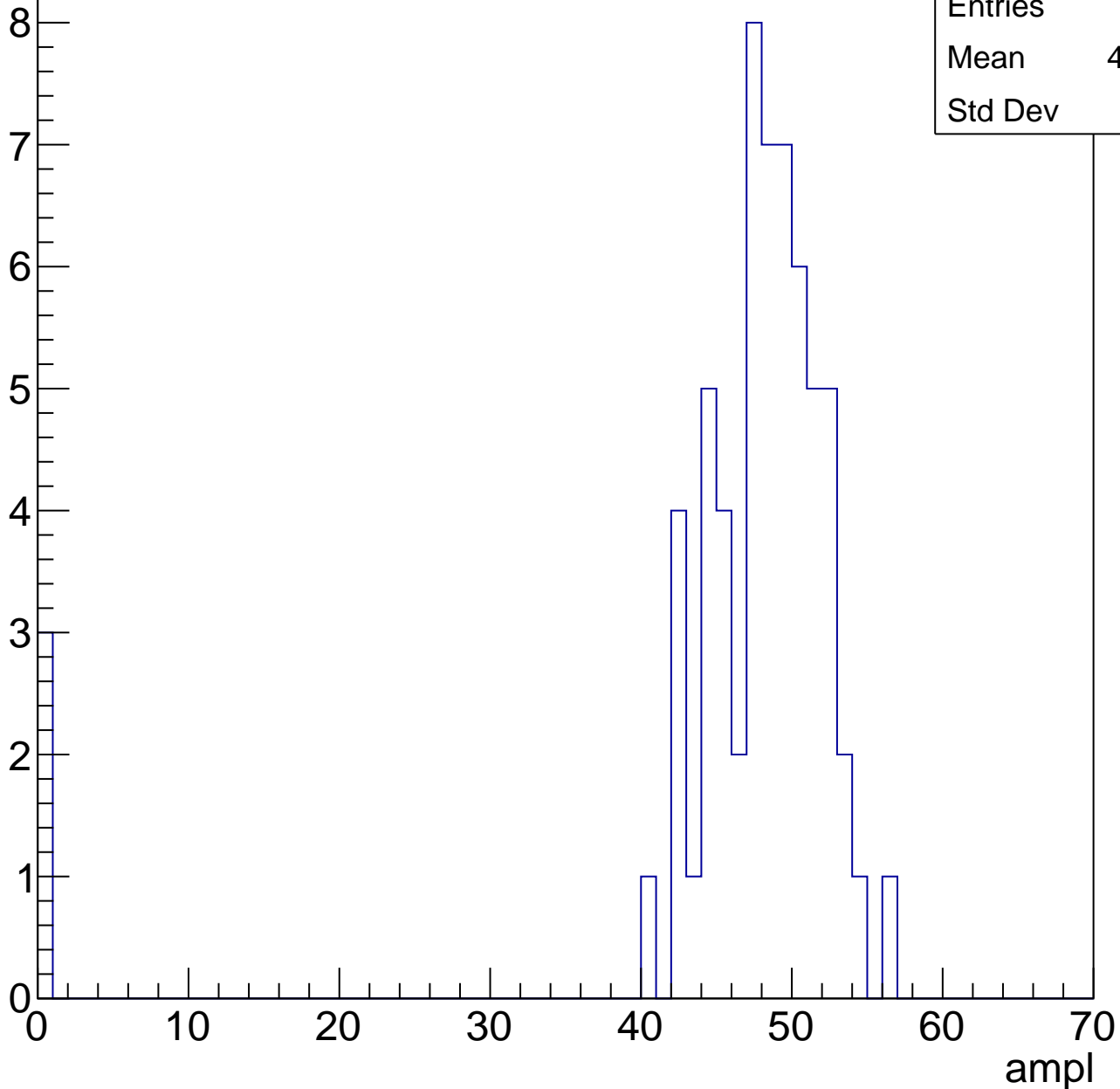


B1L103S, U7-ch122, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	62
Mean	45.63
Std Dev	10.8

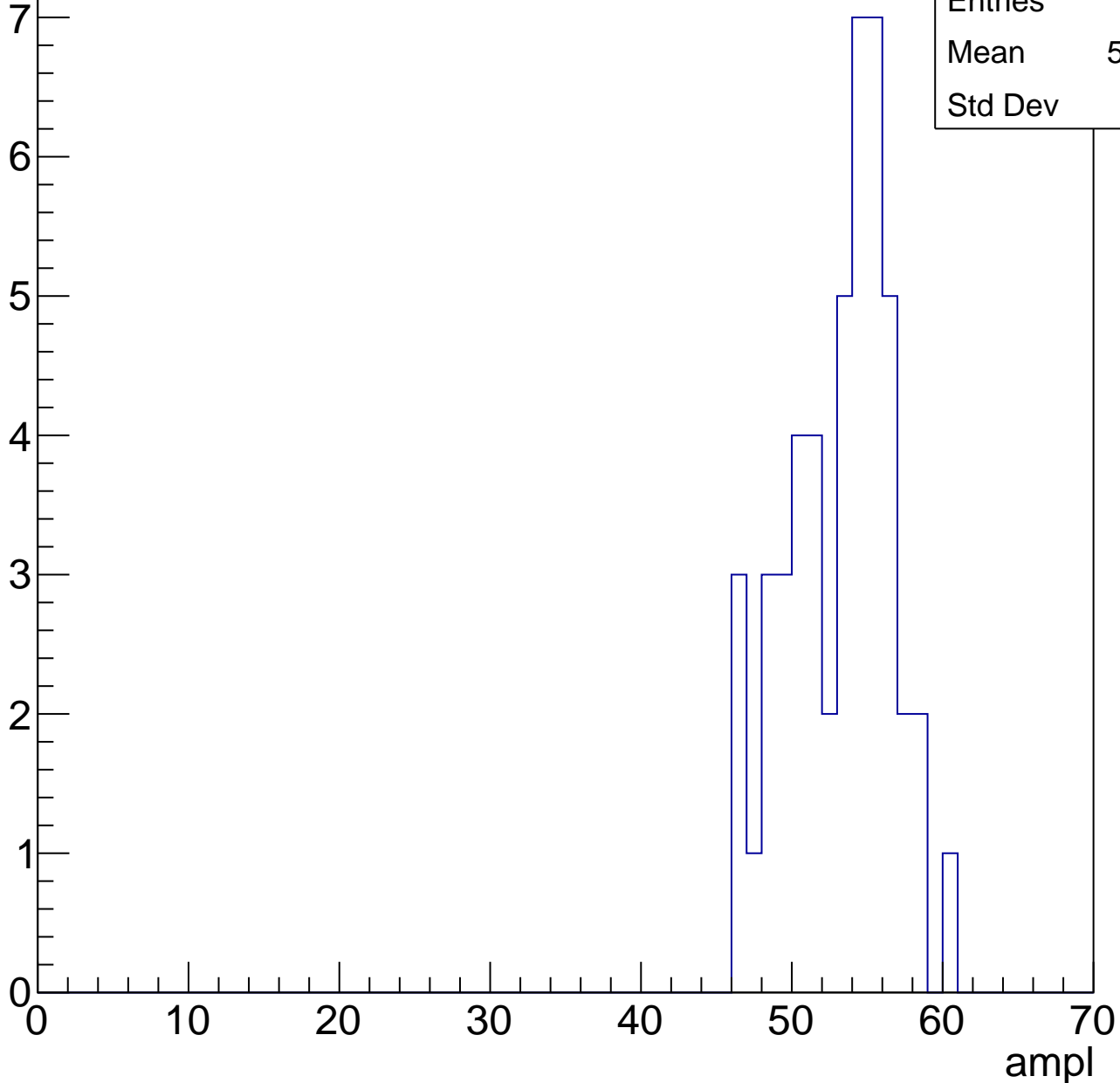


B1L103S, U7-ch122, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

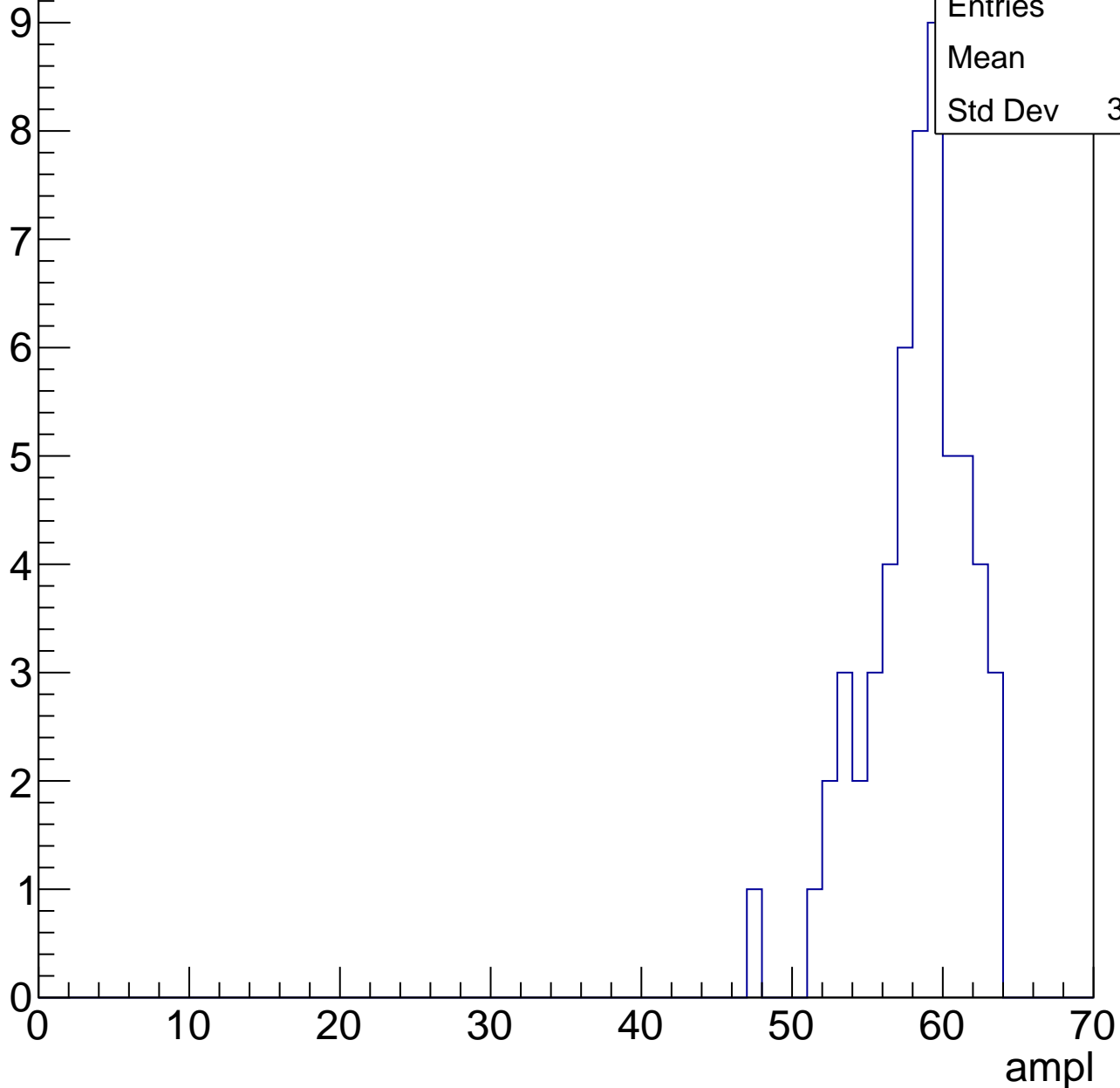
Entries	49
Mean	52.69
Std Dev	3.4



B1L103S, U7-ch122, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

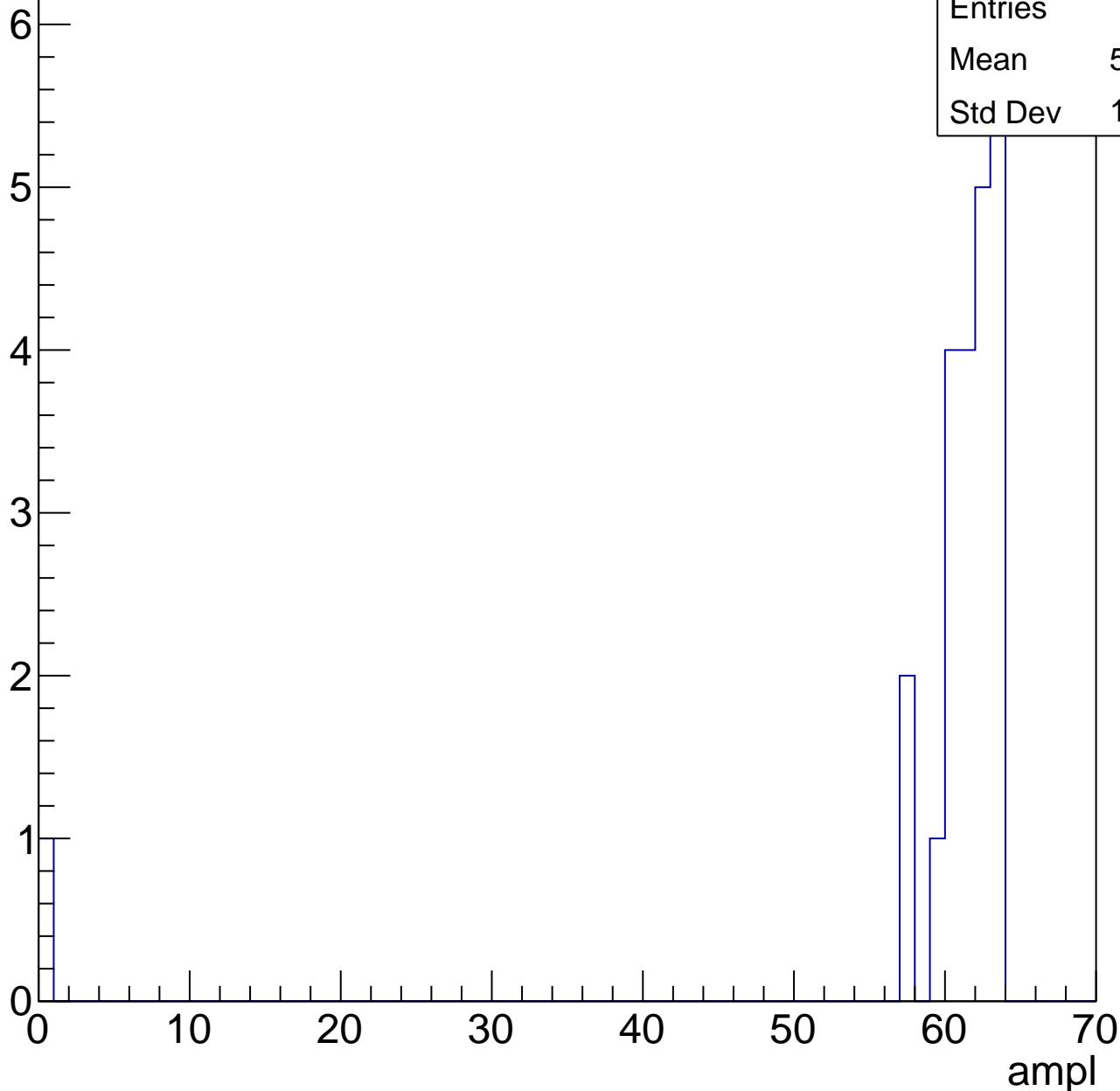


B1L103S, U7-ch122, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	23
Mean	58.48
Std Dev	12.59

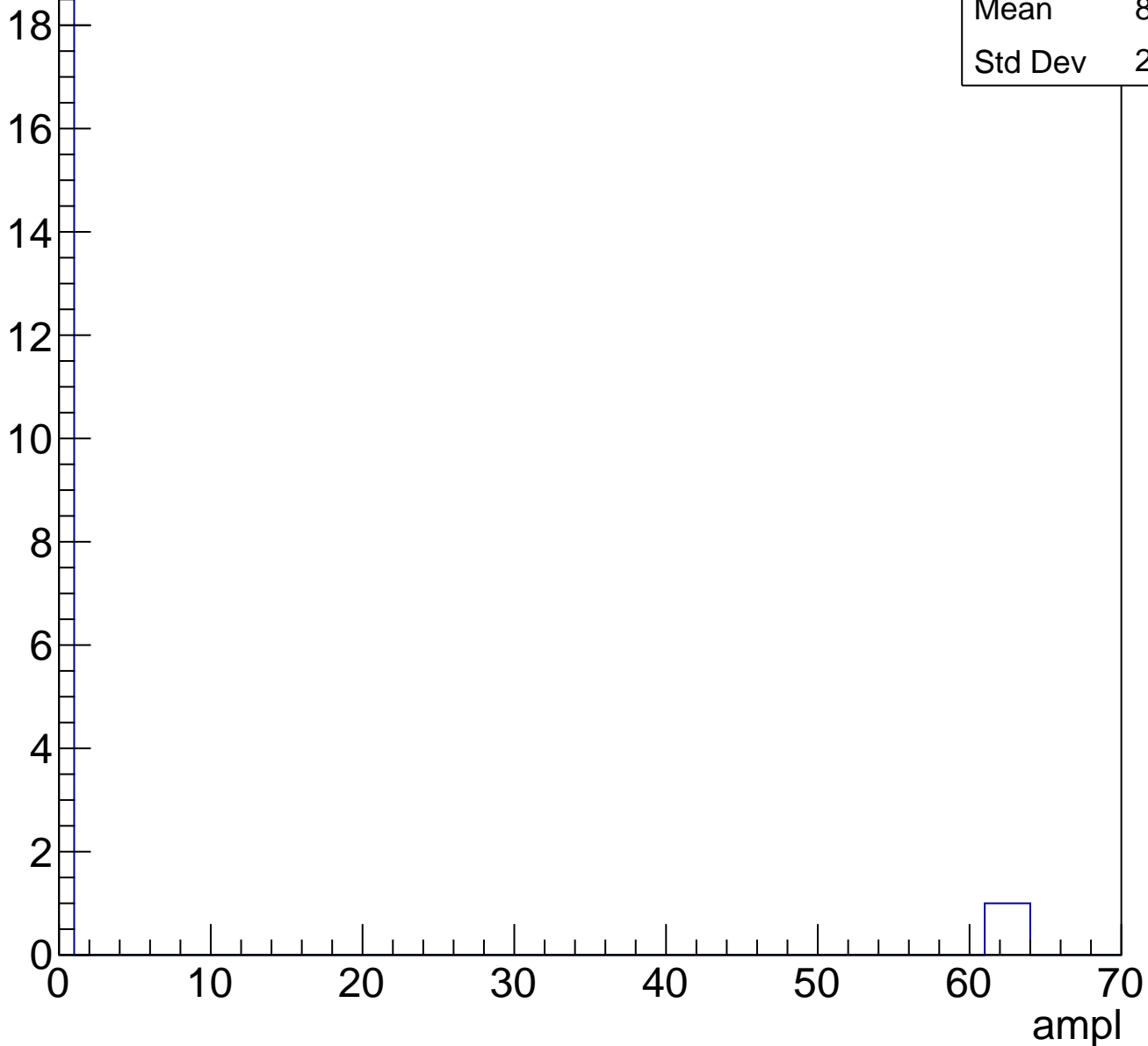


B1L103S, U7-ch122, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	22
Mean	8.455
Std Dev	21.28

Entry



B1L103S, U7-ch123, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	76
Mean	21.14
Std Dev	12.92

Gaus mean : 28.8005

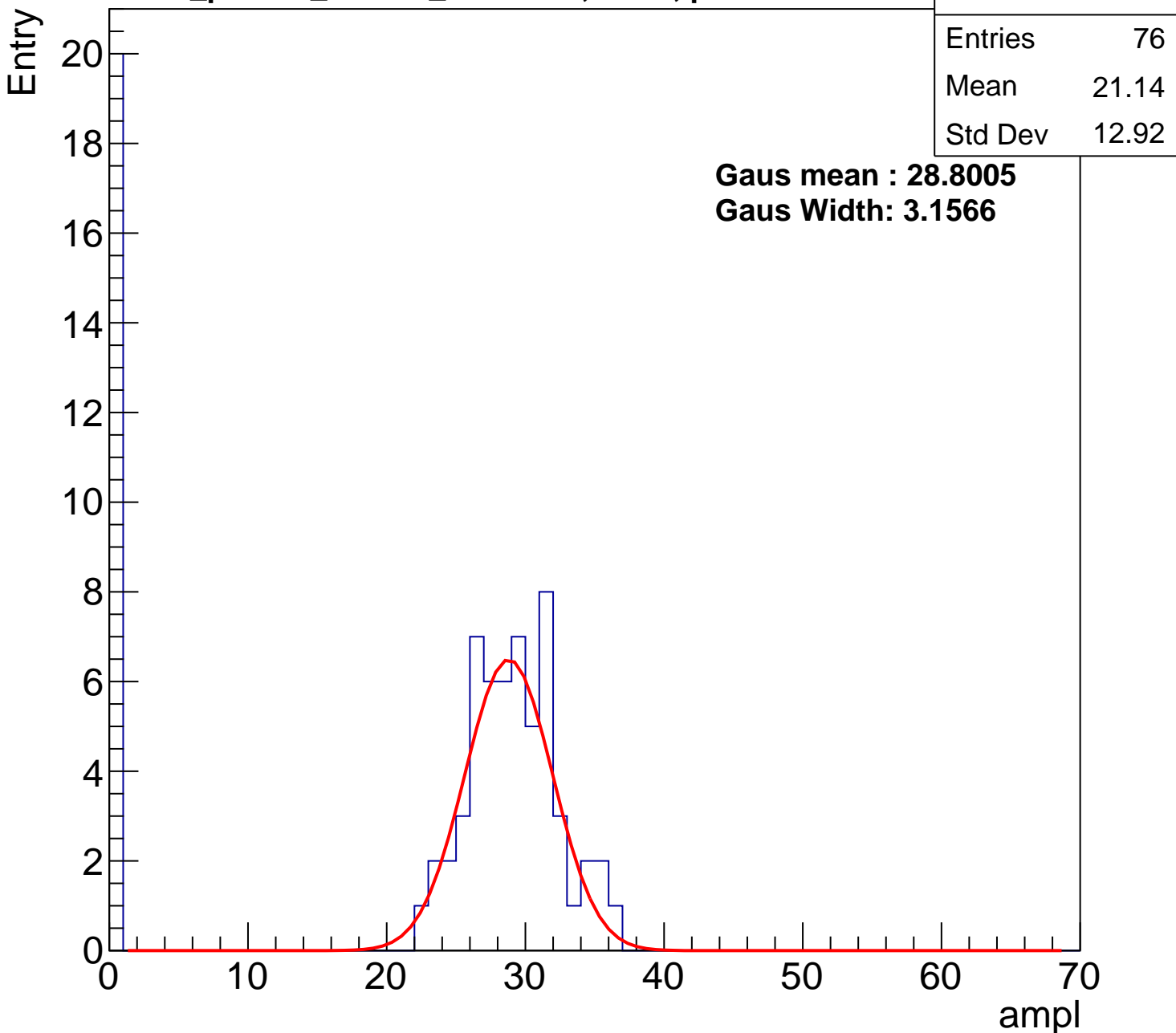
Gaus Width: 3.1566

Entry

20
18
16
14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U7-ch123, adc1

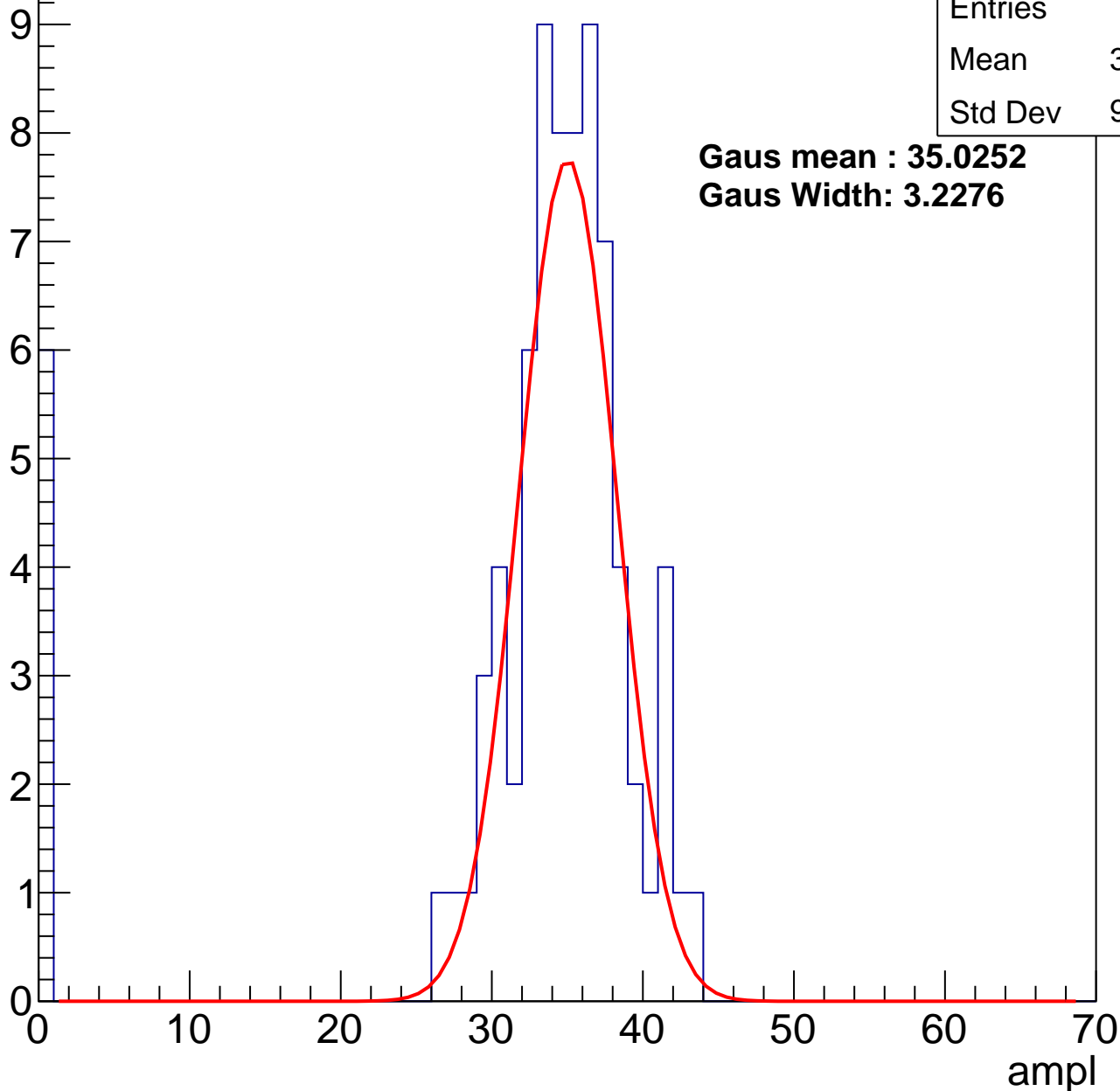
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	78
Mean	31.96
Std Dev	9.838

Gaus mean : 35.0252

Gaus Width: 3.2276



B1L103S, U7-ch123, adc2

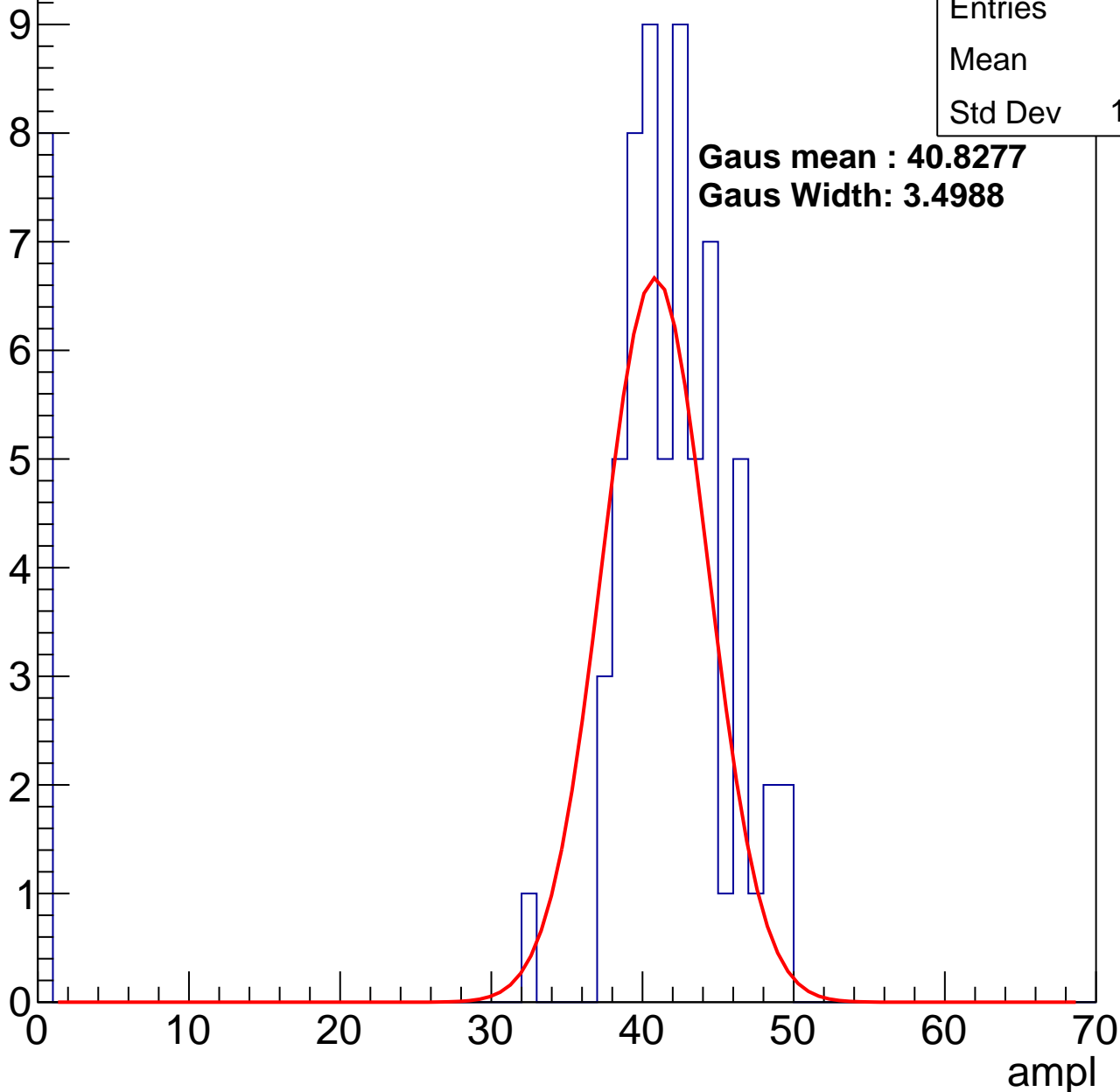
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	37
Std Dev	13.54

Gaus mean : 40.8277

Gaus Width: 3.4988

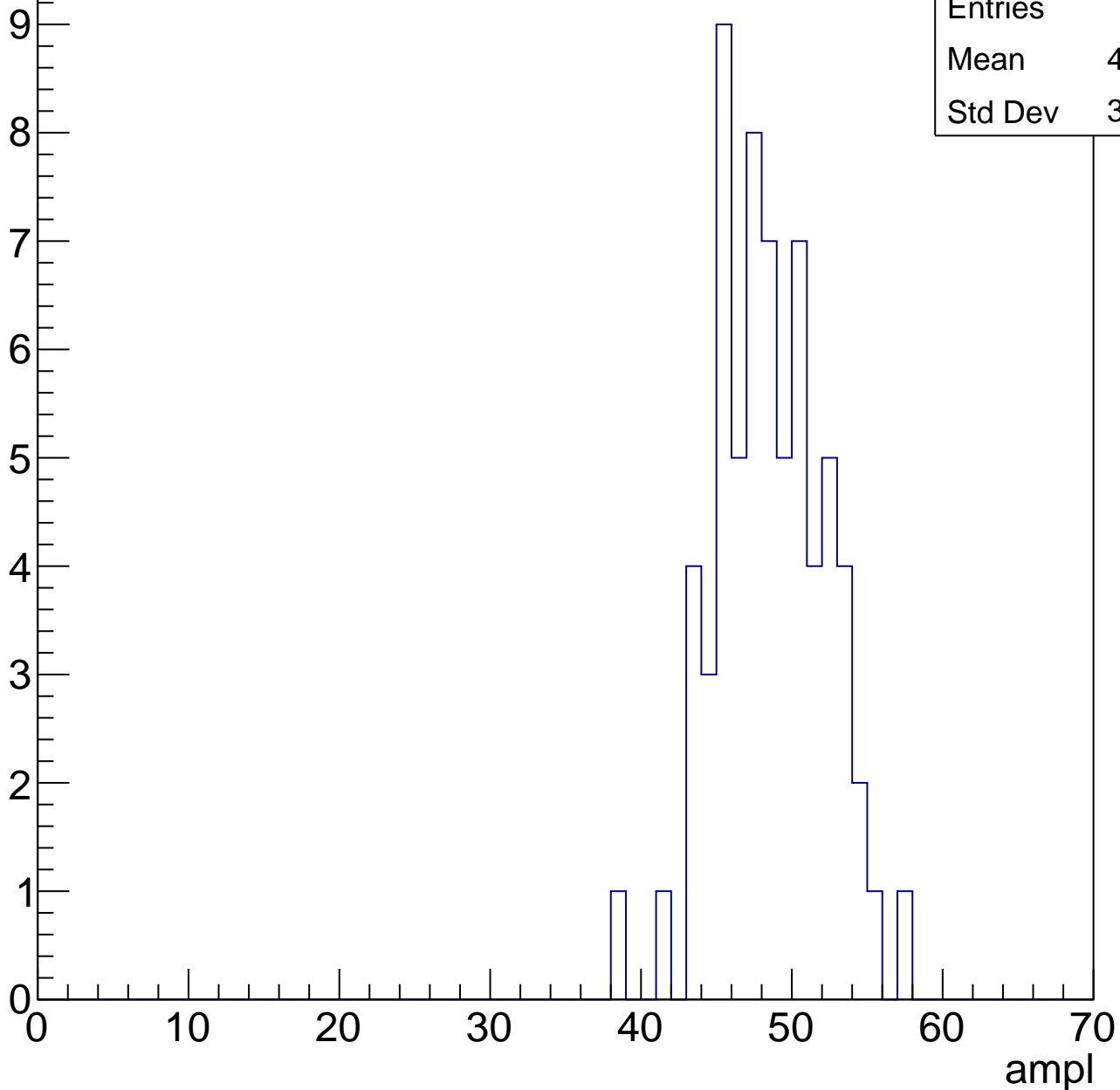


B1L103S, U7-ch123, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

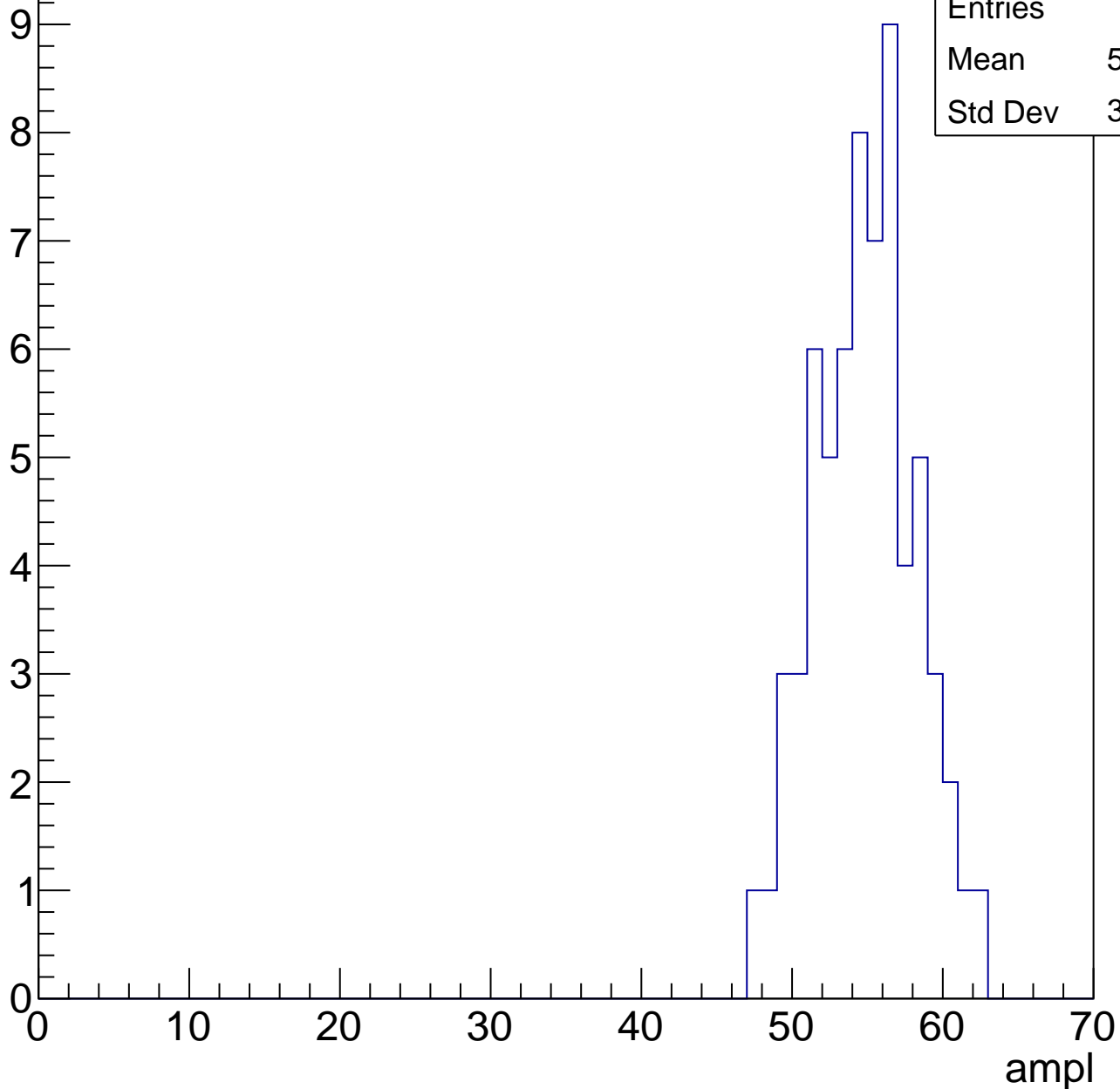
Entries	67
Mean	48.07
Std Dev	3.576



B1L103S, U7-ch123, adc4

calib_packv5_041523_1651.root, FC#0, port C2

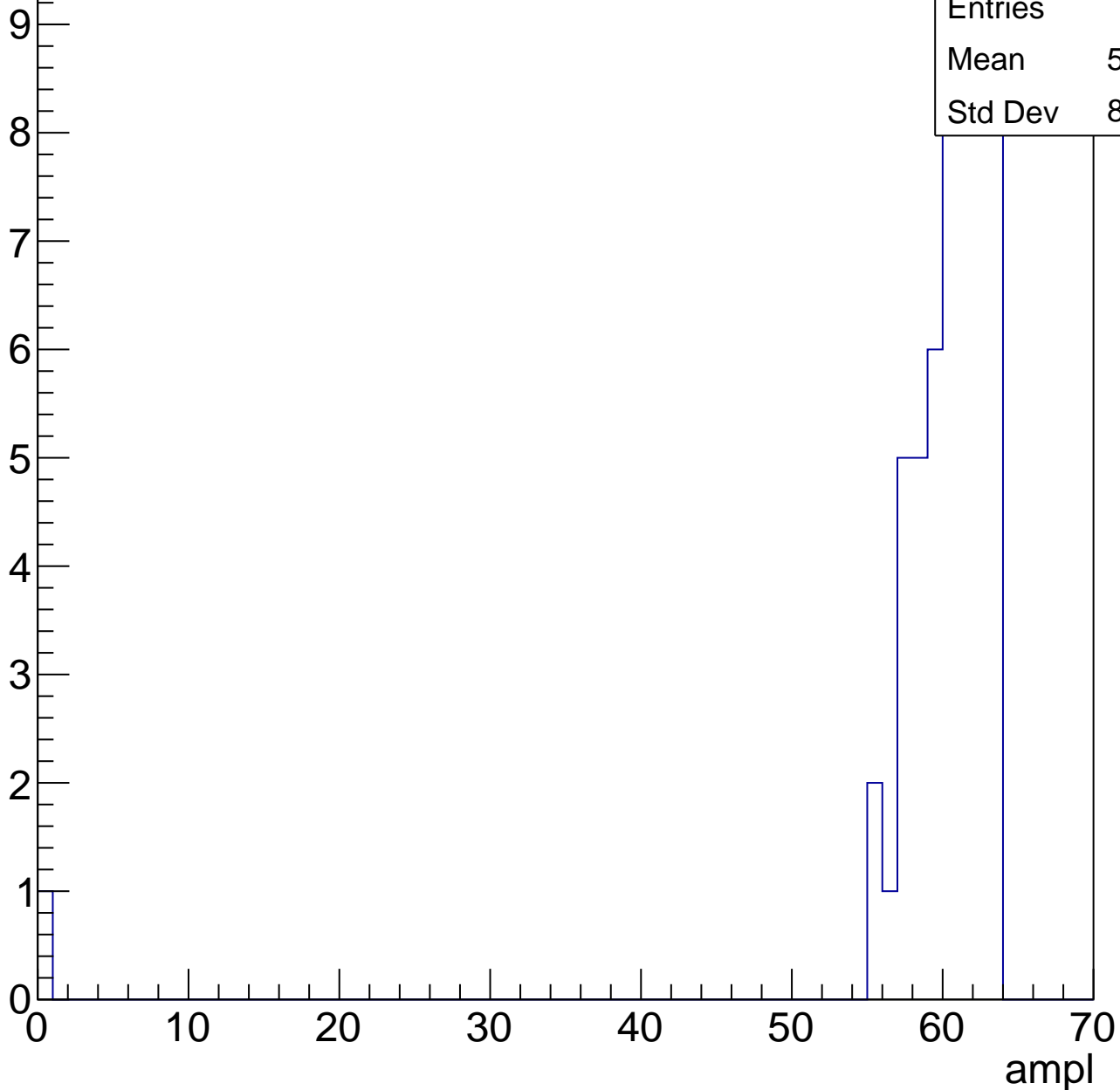
Entry



B1L103S, U7-ch123, adc5

calib_packv5_041523_1651.root, FC#0, port C2

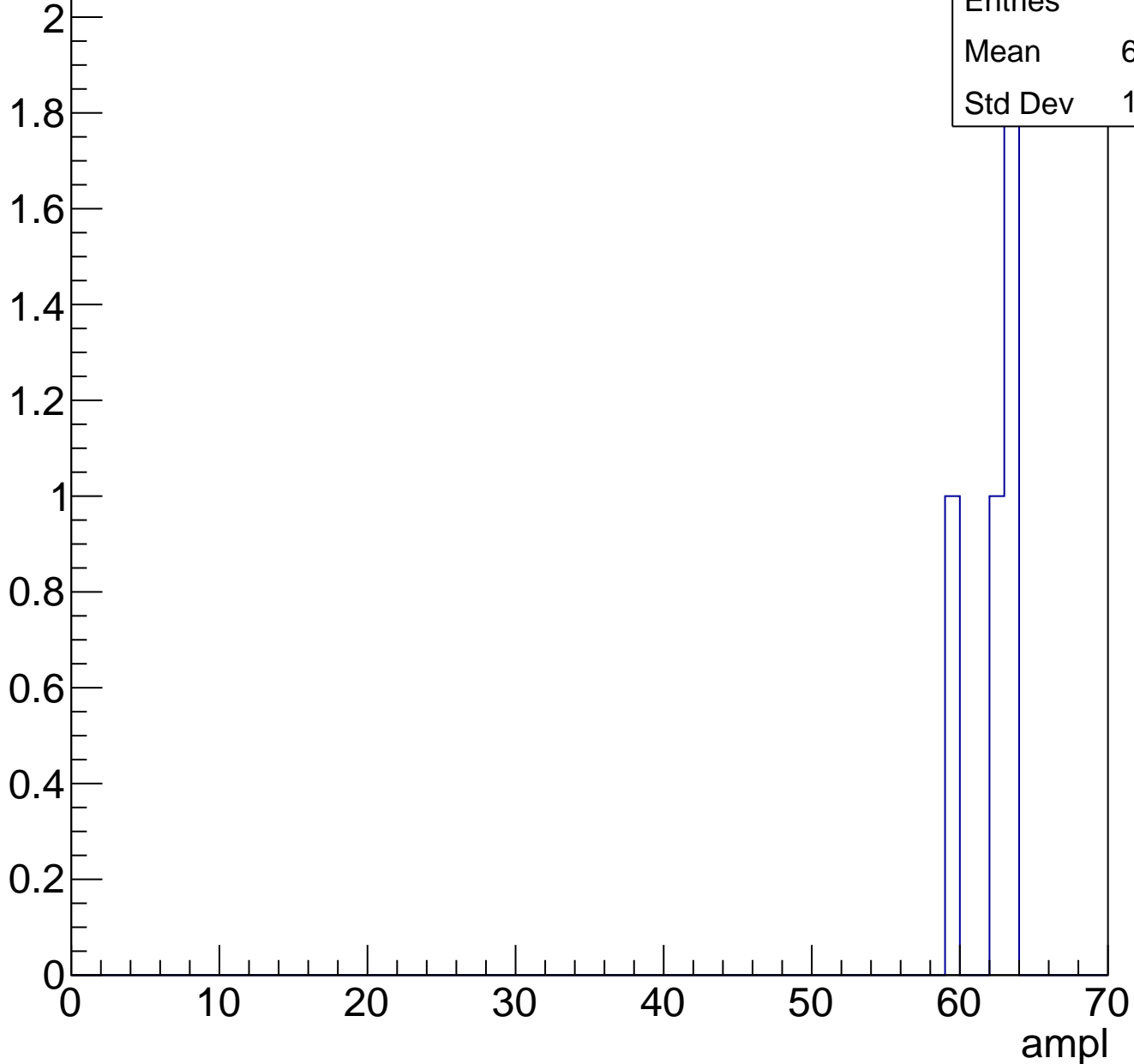
Entry



B1L103S, U7-ch123, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

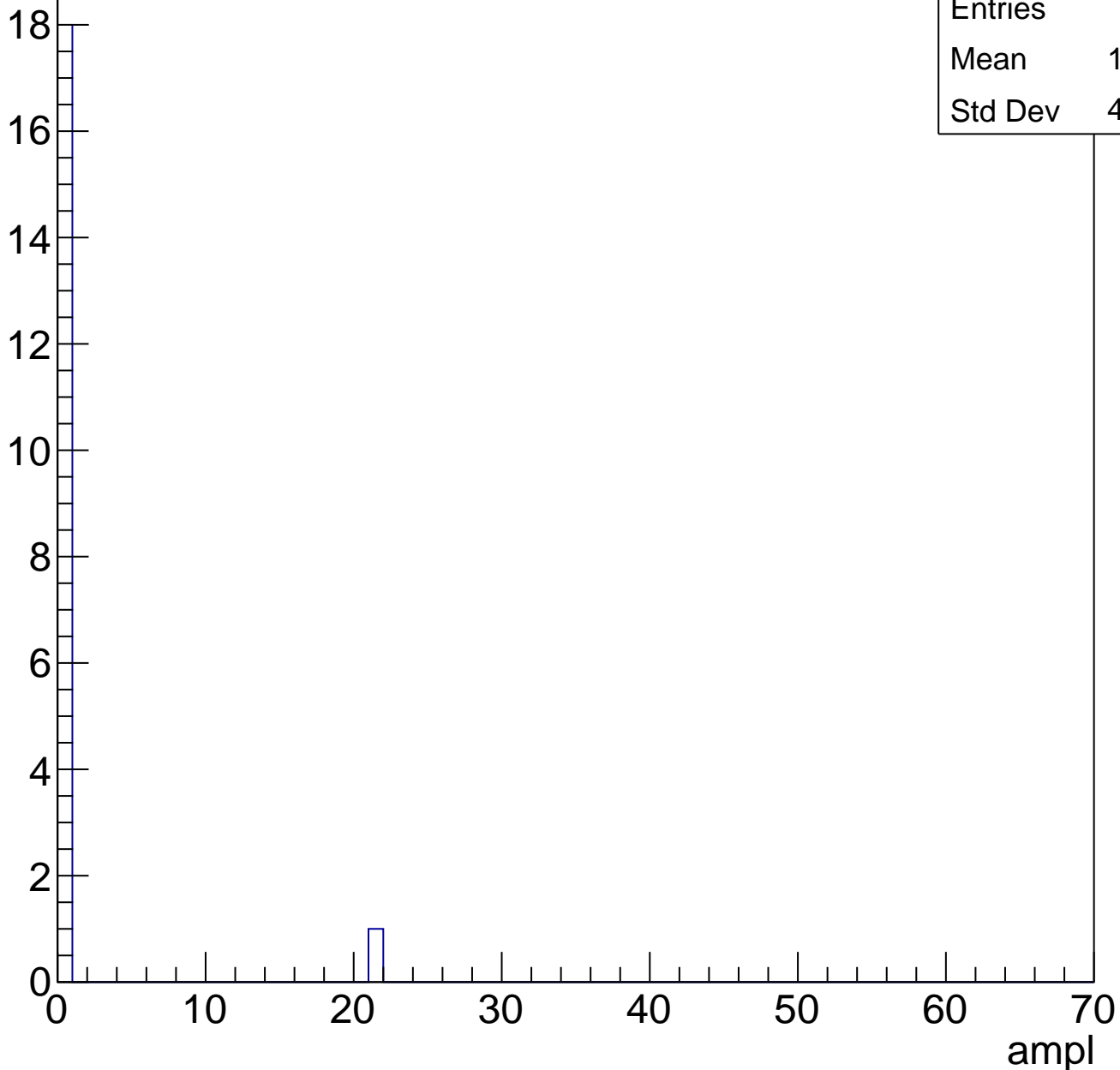


B1L103S, U7-ch123, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	19
Mean	1.105
Std Dev	4.689

Entry



B1L103S, U7-ch124, adc0

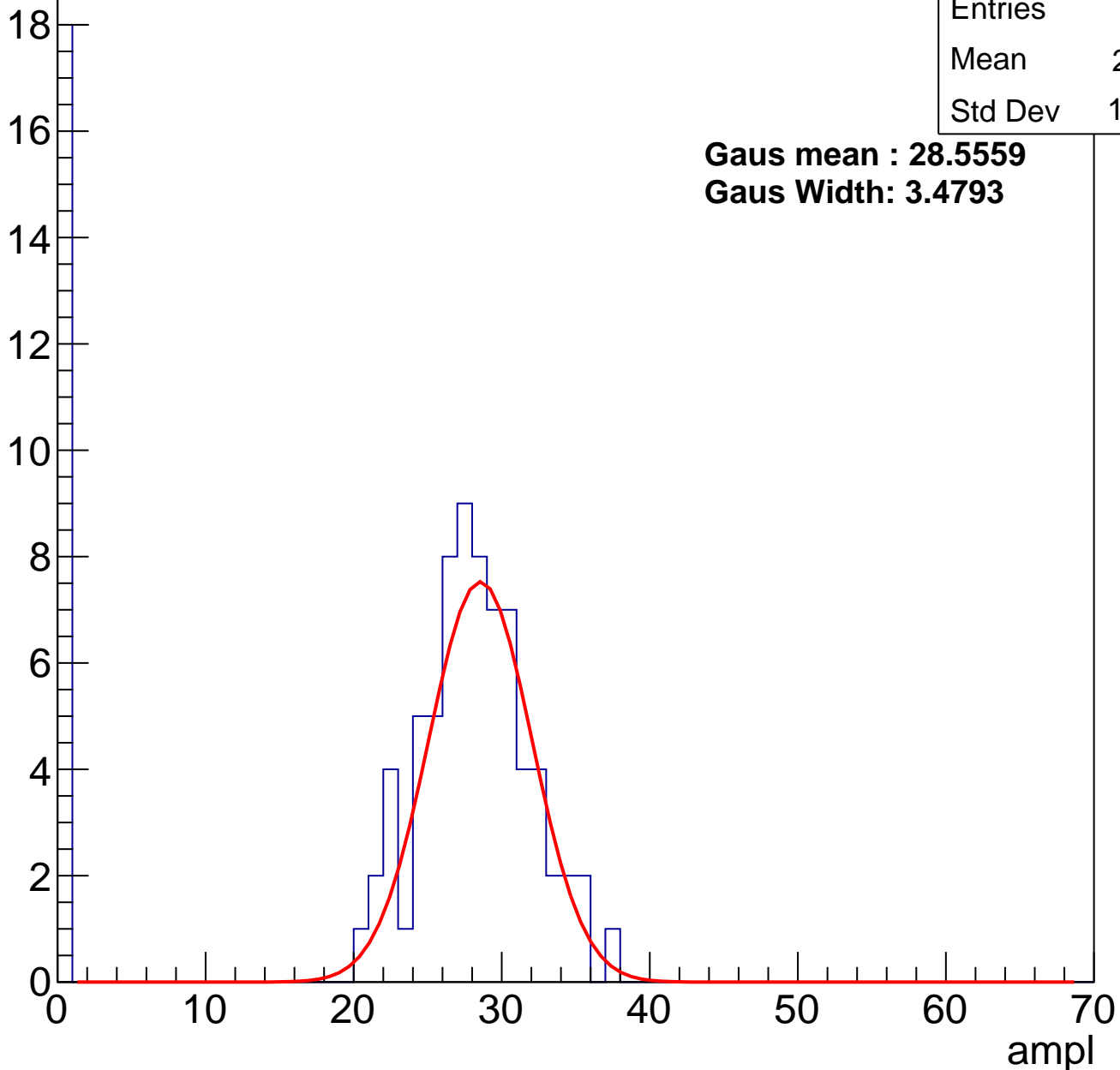
calib_packv5_041523_1651.root, FC#0, port C2

Entries	90
Mean	22.21
Std Dev	11.56

Gaus mean : 28.5559

Gaus Width: 3.4793

Entry



B1L103S, U7-ch124, adc1

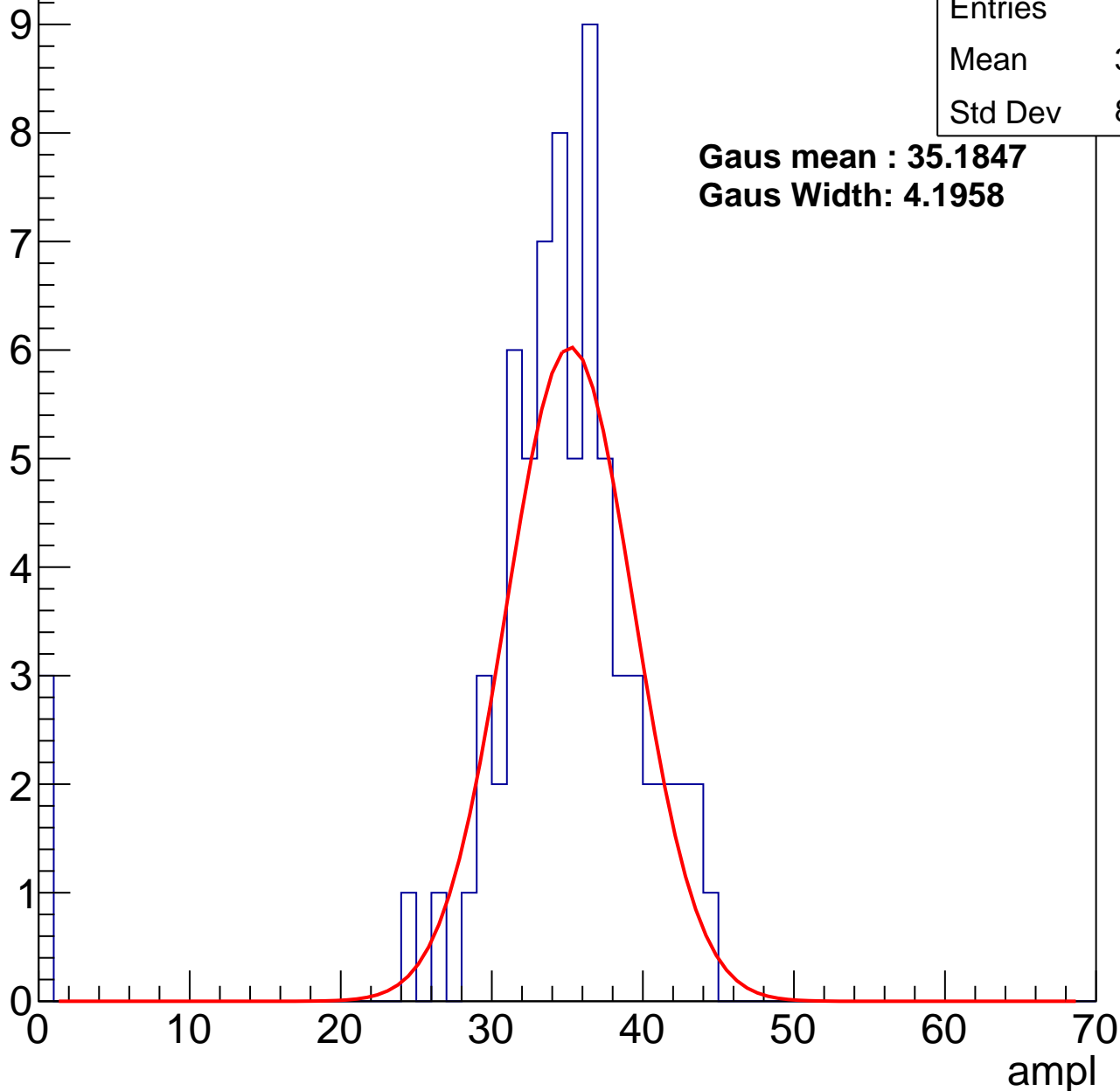
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	71
Mean	33.31
Std Dev	8.041

Gaus mean : 35.1847

Gaus Width: 4.1958



B1L103S, U7-ch124, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	73
Mean	34.47
Std Dev	14.84

Gaus mean : 41.3279

Gaus Width: 3.1943

Entry

10

8

6

4

2

0

0

10

20

30

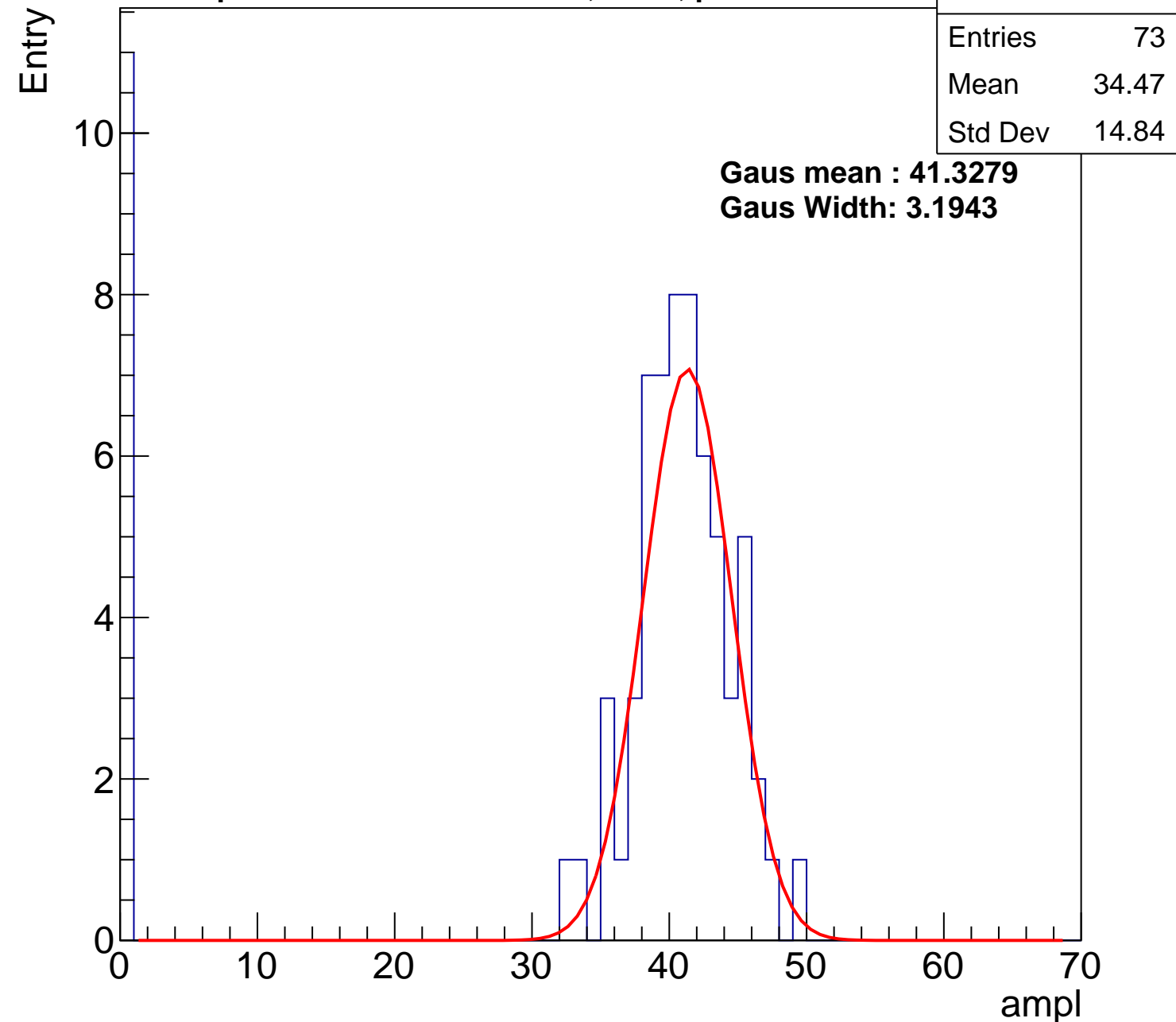
40

50

60

70

ampl

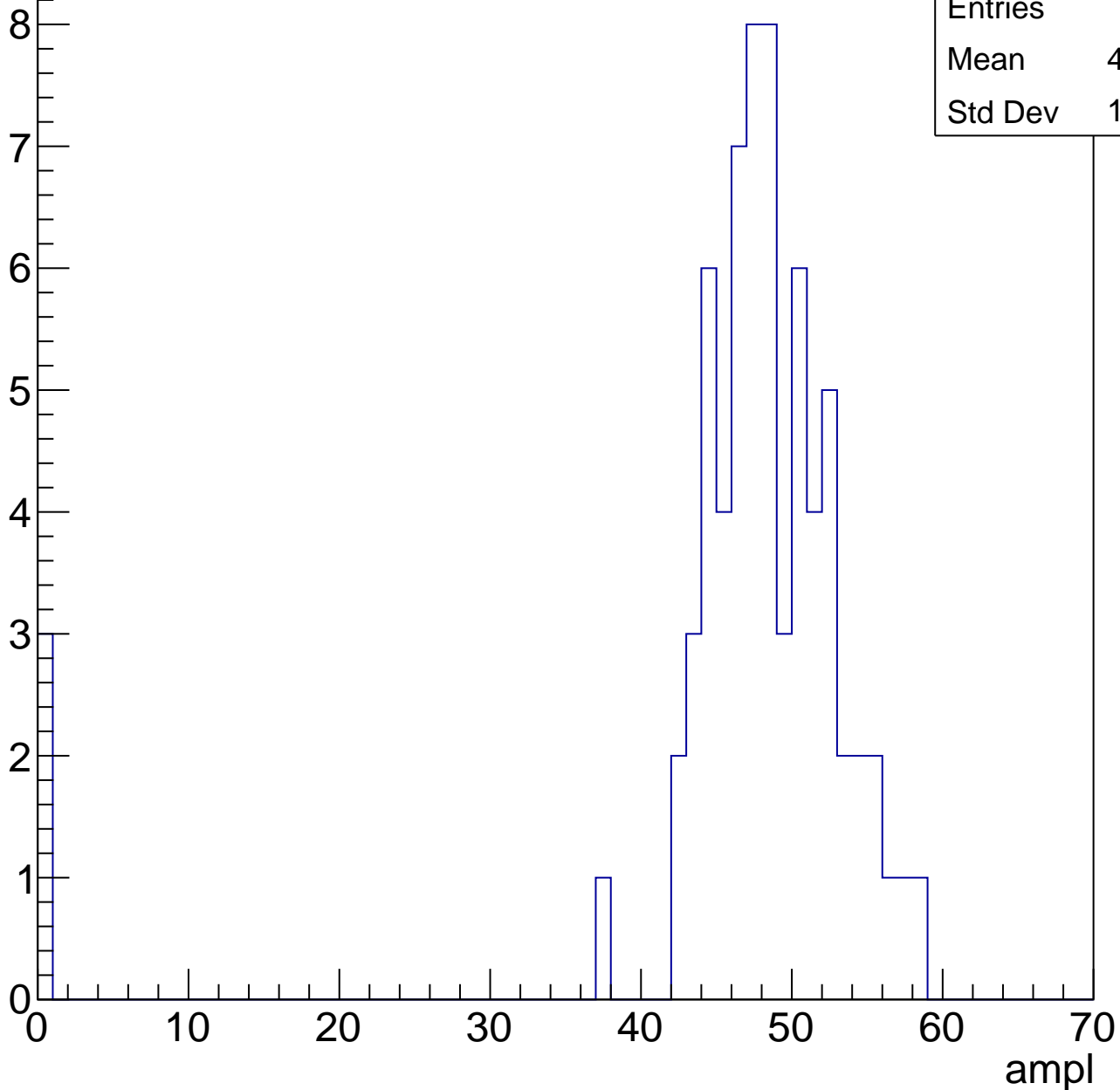


B1L103S, U7-ch124, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	46.12
Std Dev	10.57

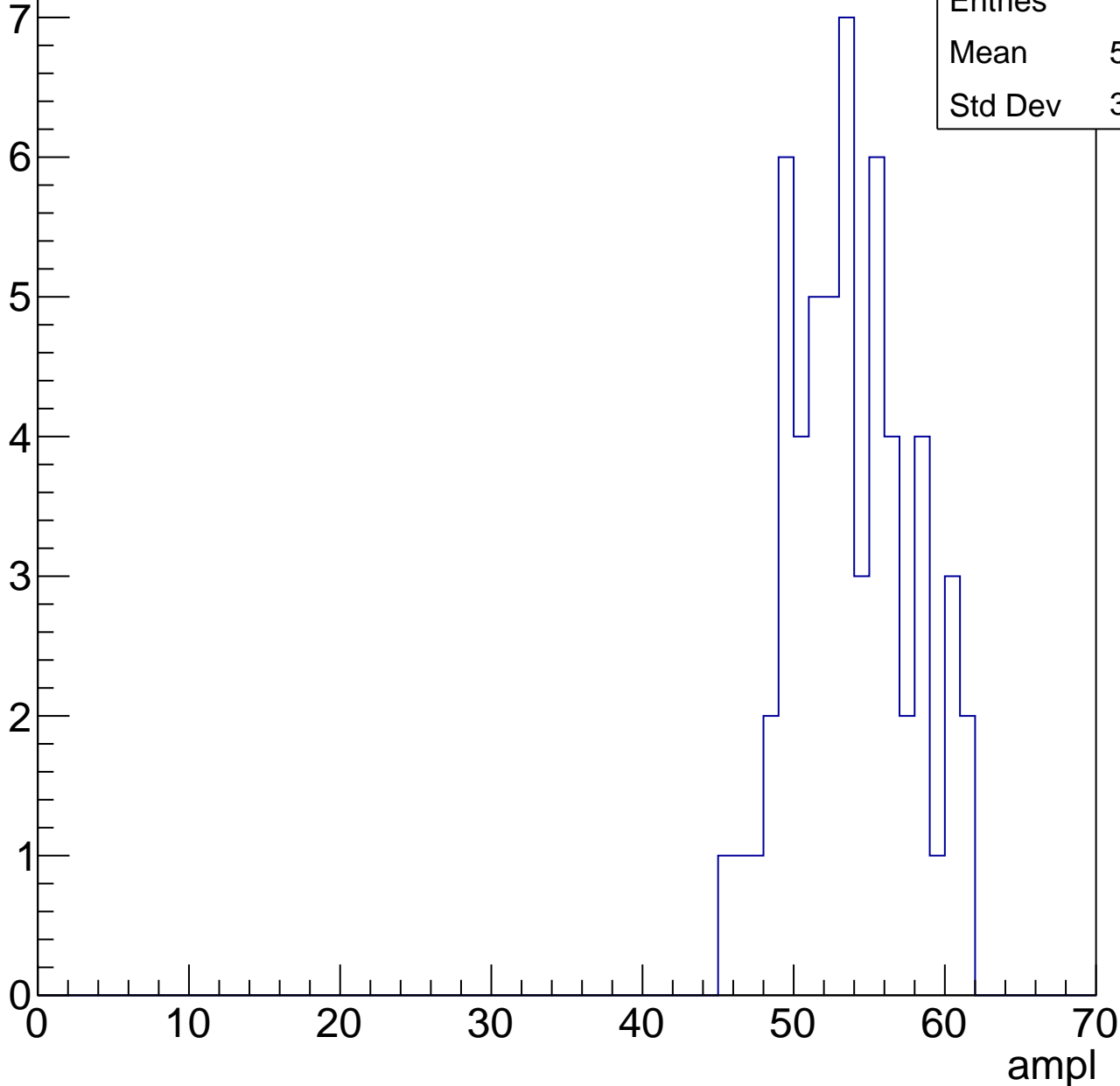


B1L103S, U7-ch124, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

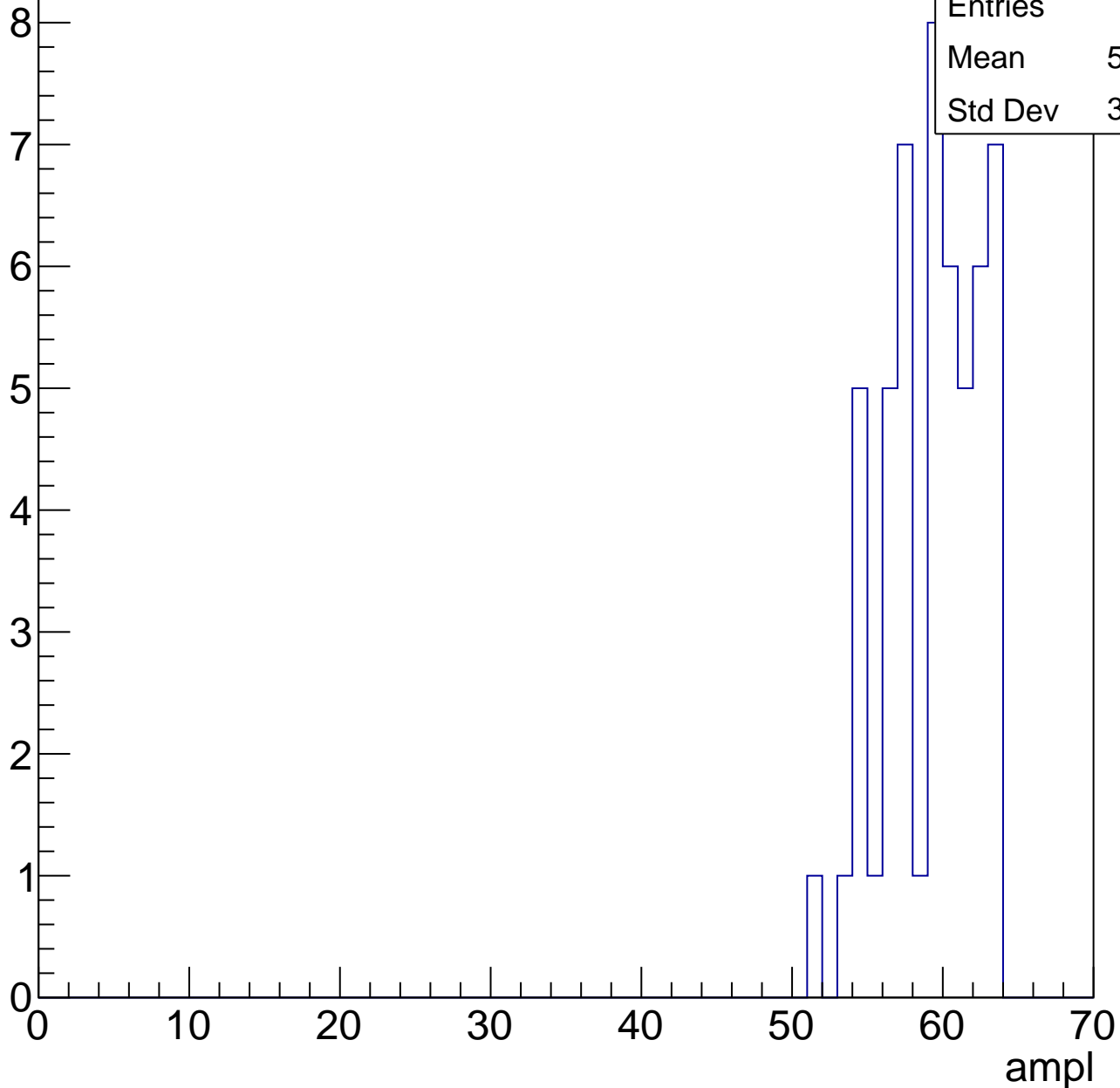
Entries	57
Mean	53.28
Std Dev	3.879



B1L103S, U7-ch124, adc5

calib_packv5_041523_1651.root, FC#0, port C2

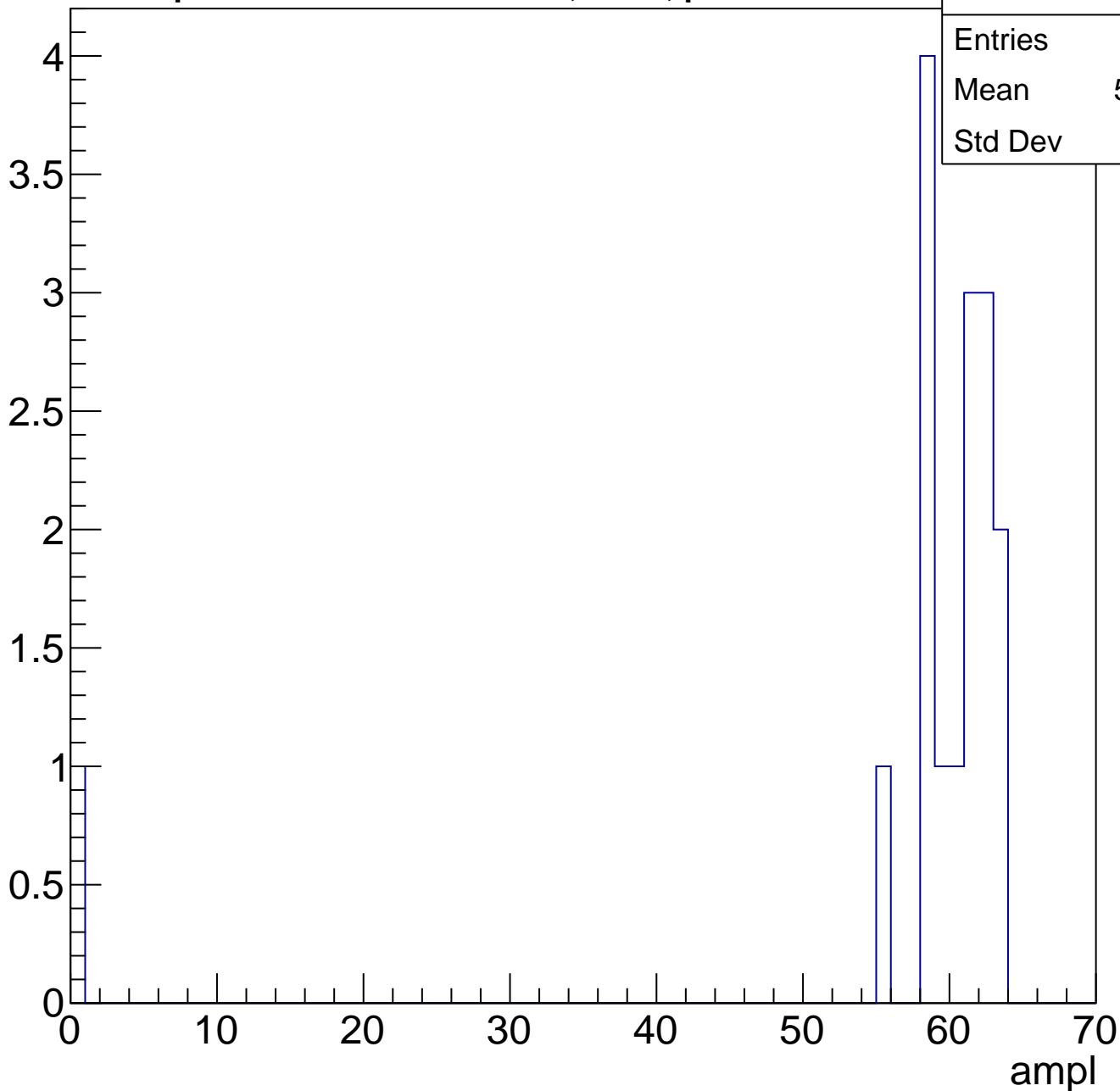
Entry



B1L103S, U7-ch124, adc6

calib_packv5_041523_1651.root, FC#0, port C2

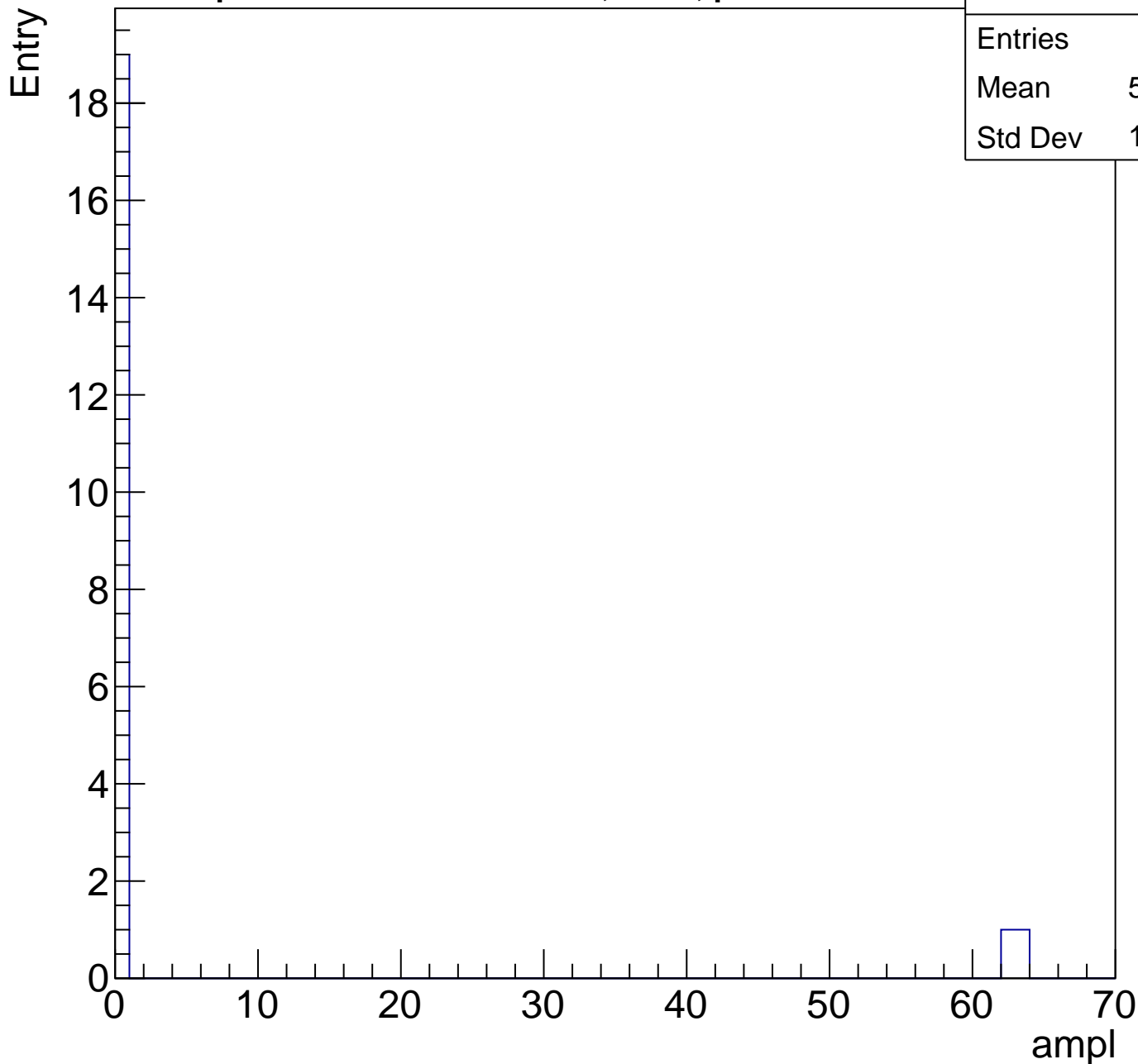
Entry



B1L103S, U7-ch124, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	21
Mean	5.952
Std Dev	18.35



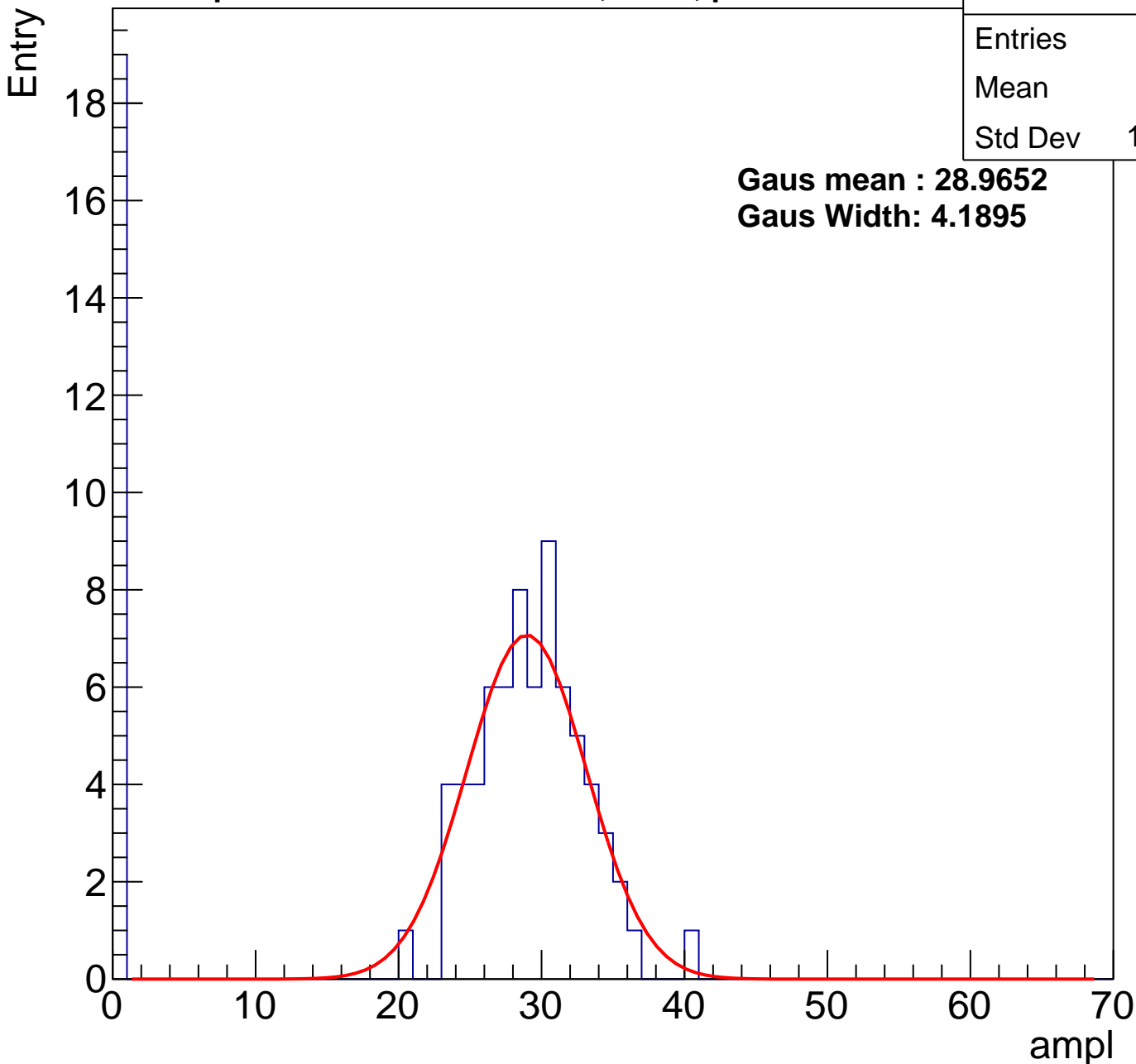
B1L103S, U7-ch125, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	89
Mean	22.7
Std Dev	12.26

Gaus mean : 28.9652

Gaus Width: 4.1895



B1L103S, U7-ch125, adc1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	80
Mean	30.71
Std Dev	12.71

Gaus mean : 36.4592

Gaus Width: 3.7497

Entry

10

8

6

4

2

0

0

10

20

30

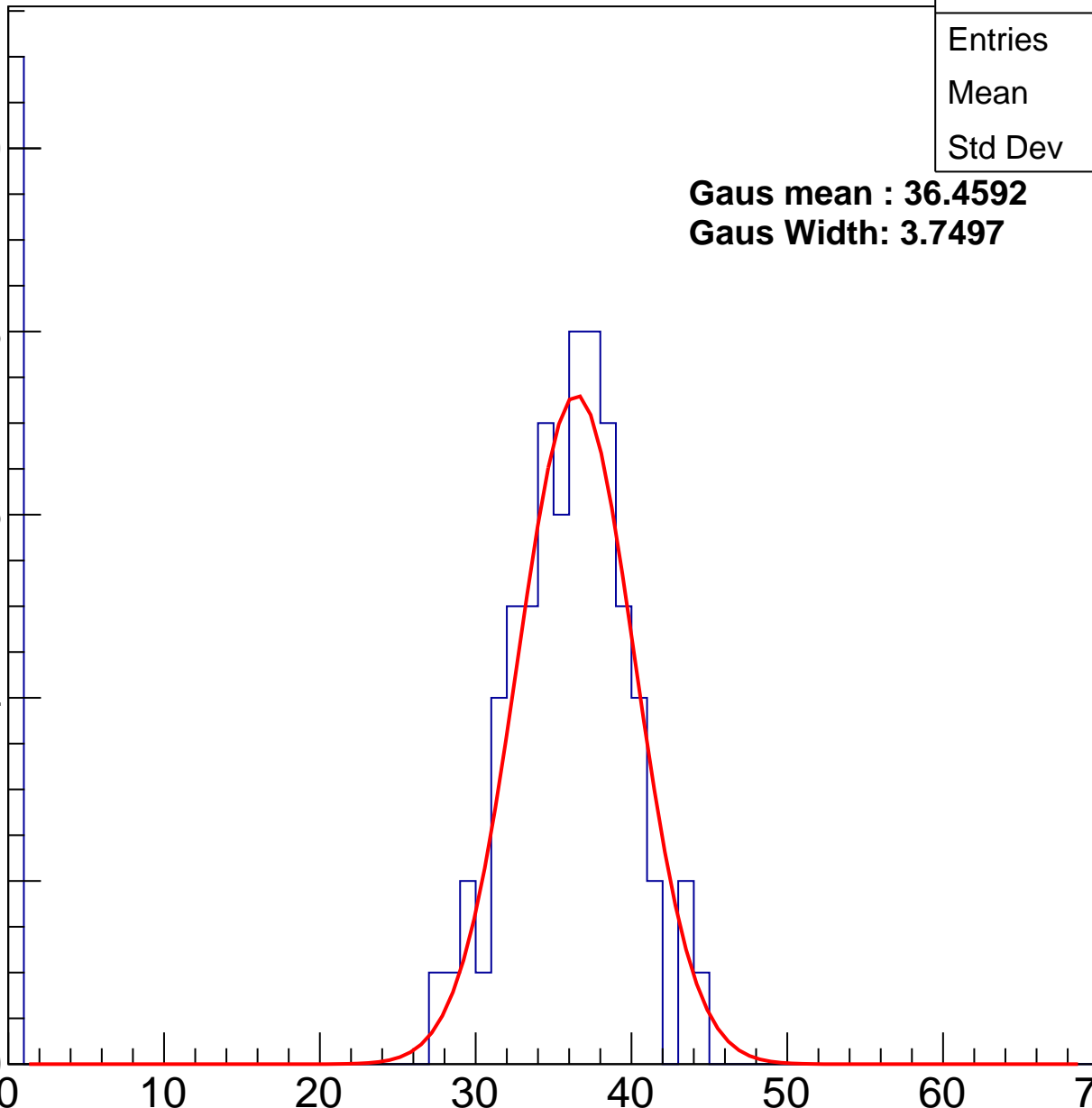
40

50

60

70

ampl



B1L103S, U7-ch125, adc2

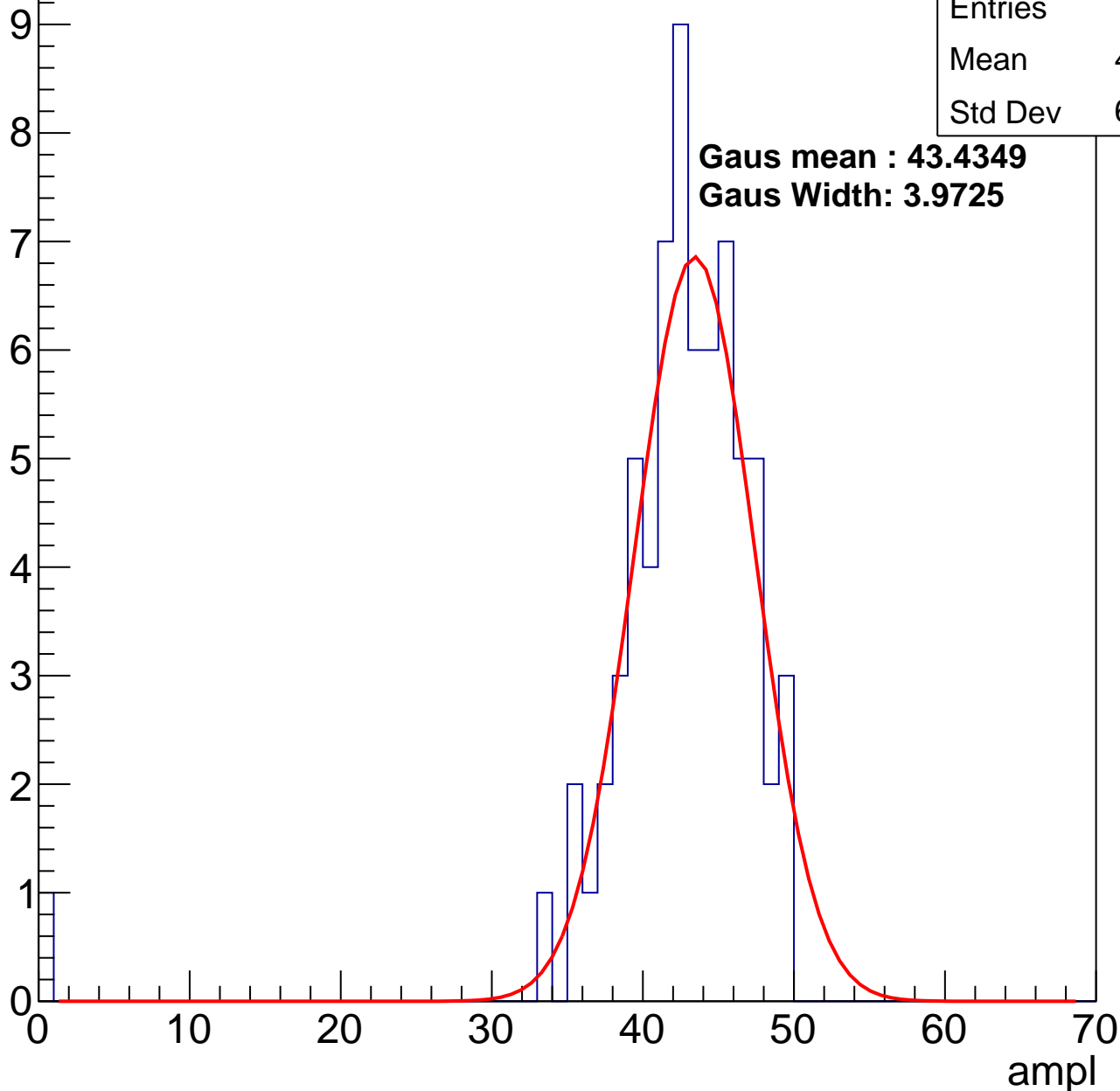
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	69
Mean	41.91
Std Dev	6.211

Gaus mean : 43.4349

Gaus Width: 3.9725

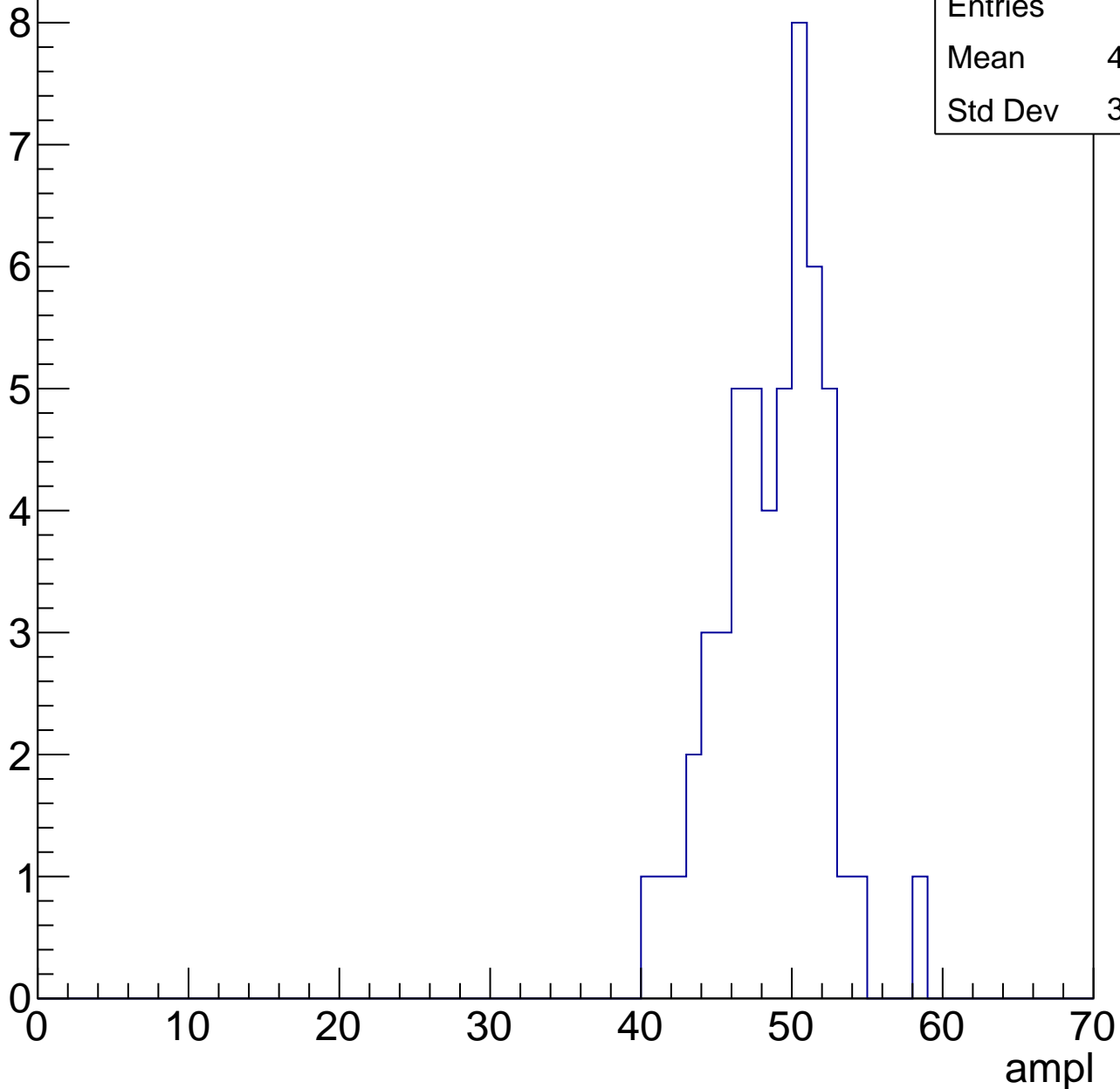


B1L103S, U7-ch125, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	52
Mean	48.25
Std Dev	3.474

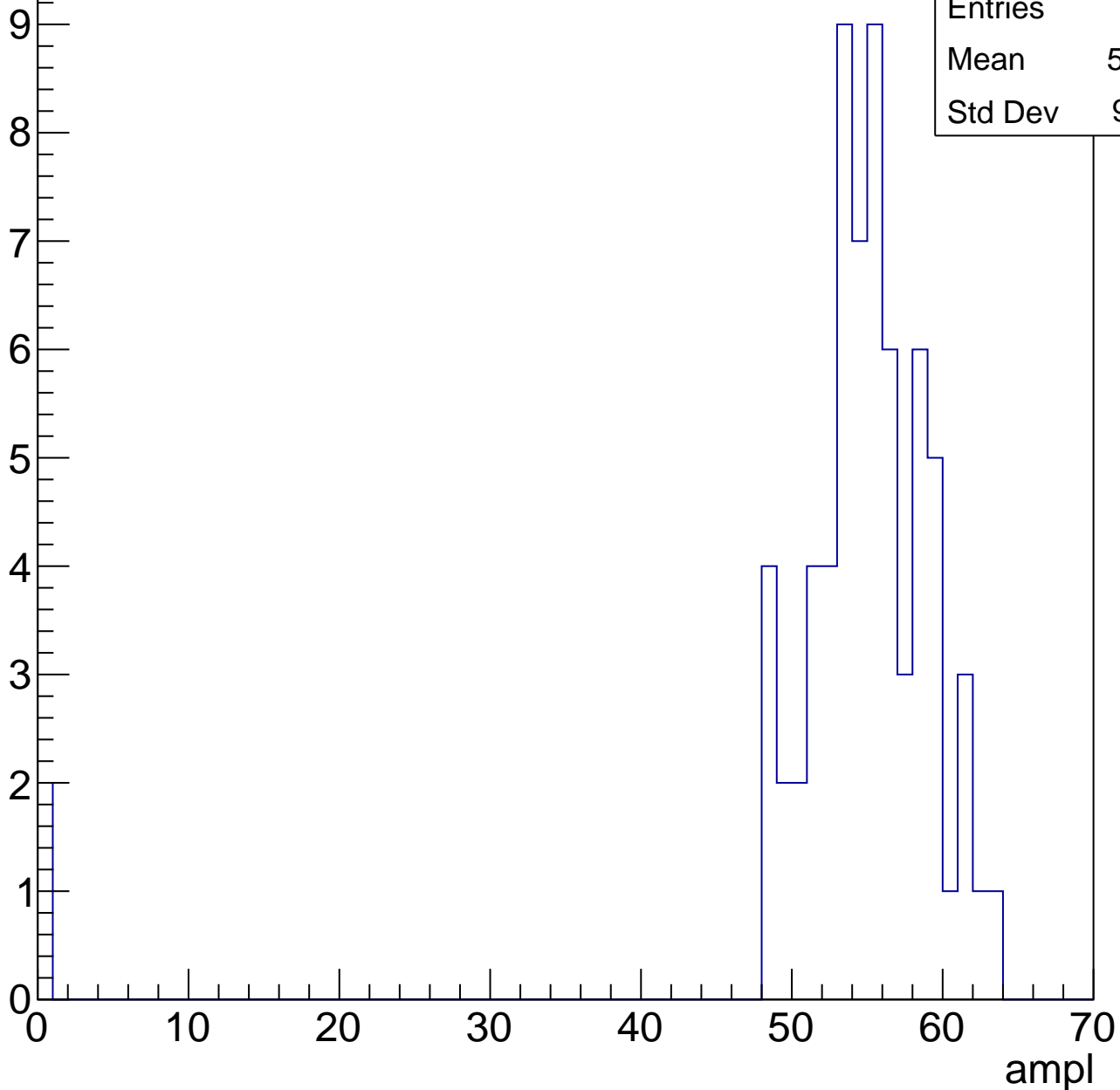


B1L103S, U7-ch125, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

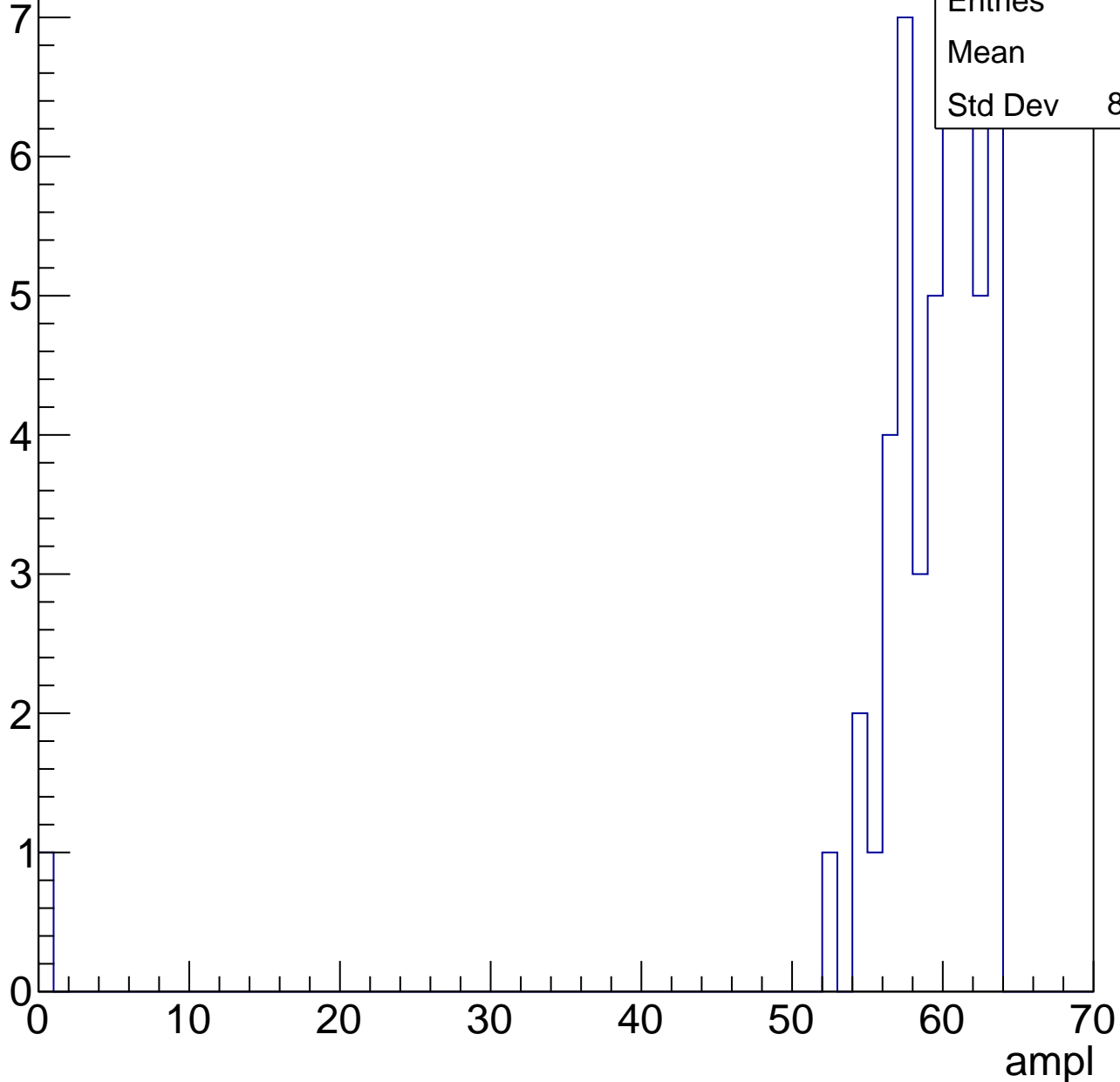
Entries	69
Mean	53.19
Std Dev	9.841



B1L103S, U7-ch125, adc5

calib_packv5_041523_1651.root, FC#0, port C2

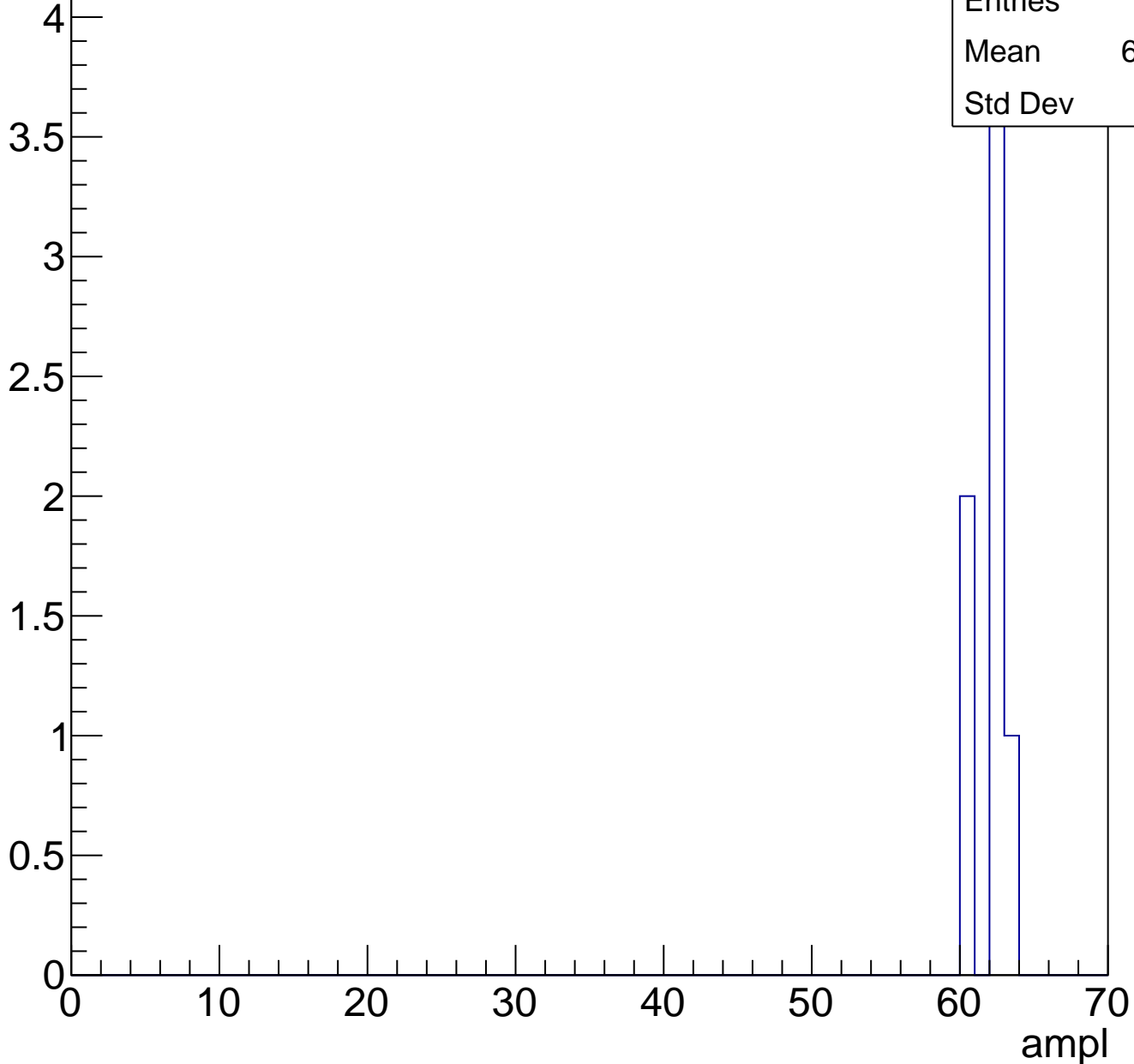
Entry



B1L103S, U7-ch125, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry



B1L103S, U7-ch125, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	20
Mean	3.15
Std Dev	13.73

Entry



B1L103S, U7-ch126, adc0

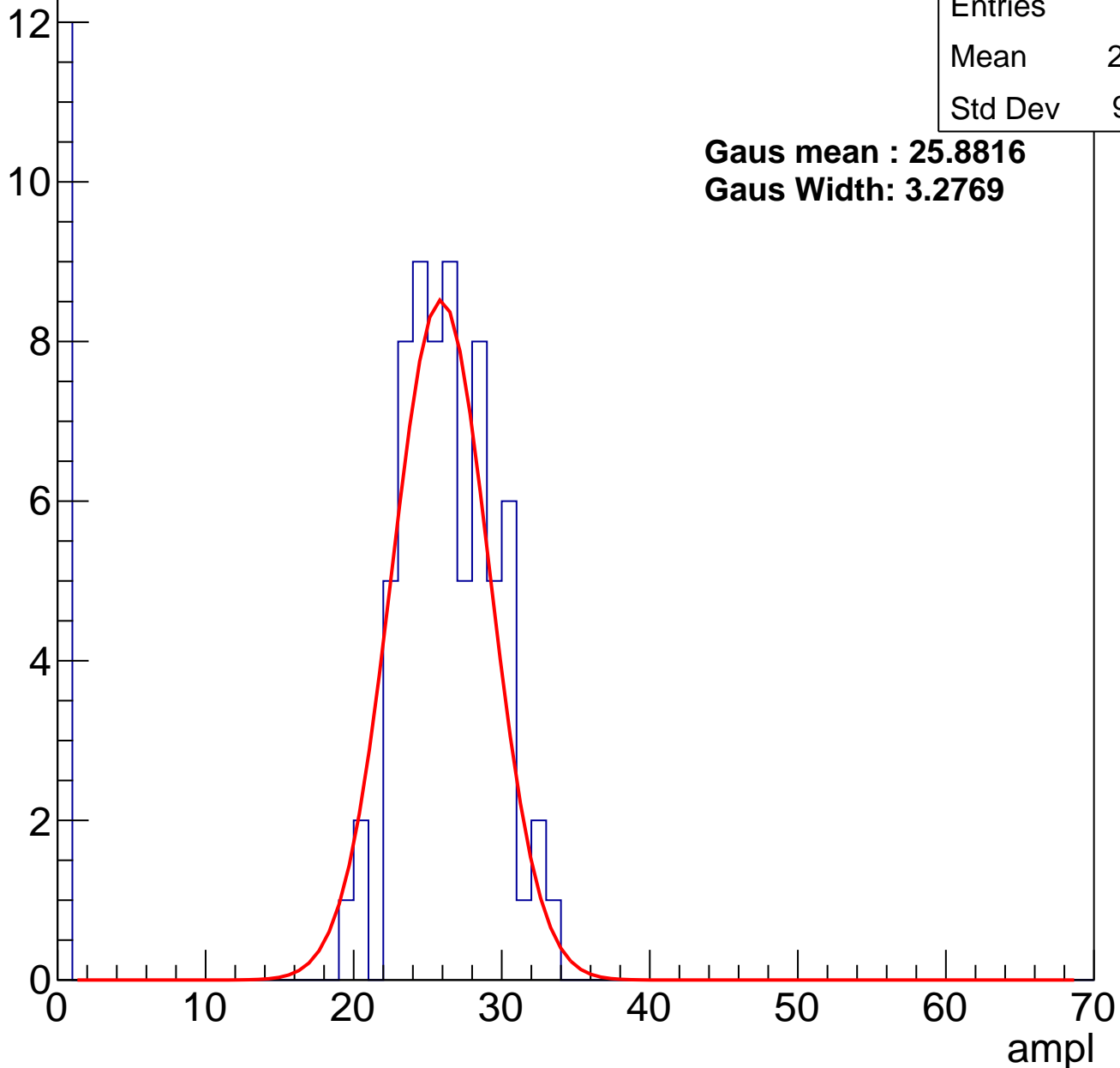
calib_packv5_041523_1651.root, FC#0, port C2

Entries	82
Mean	22.13
Std Dev	9.581

Gaus mean : 25.8816

Gaus Width: 3.2769

Entry



B1L103S, U7-ch126, adc1

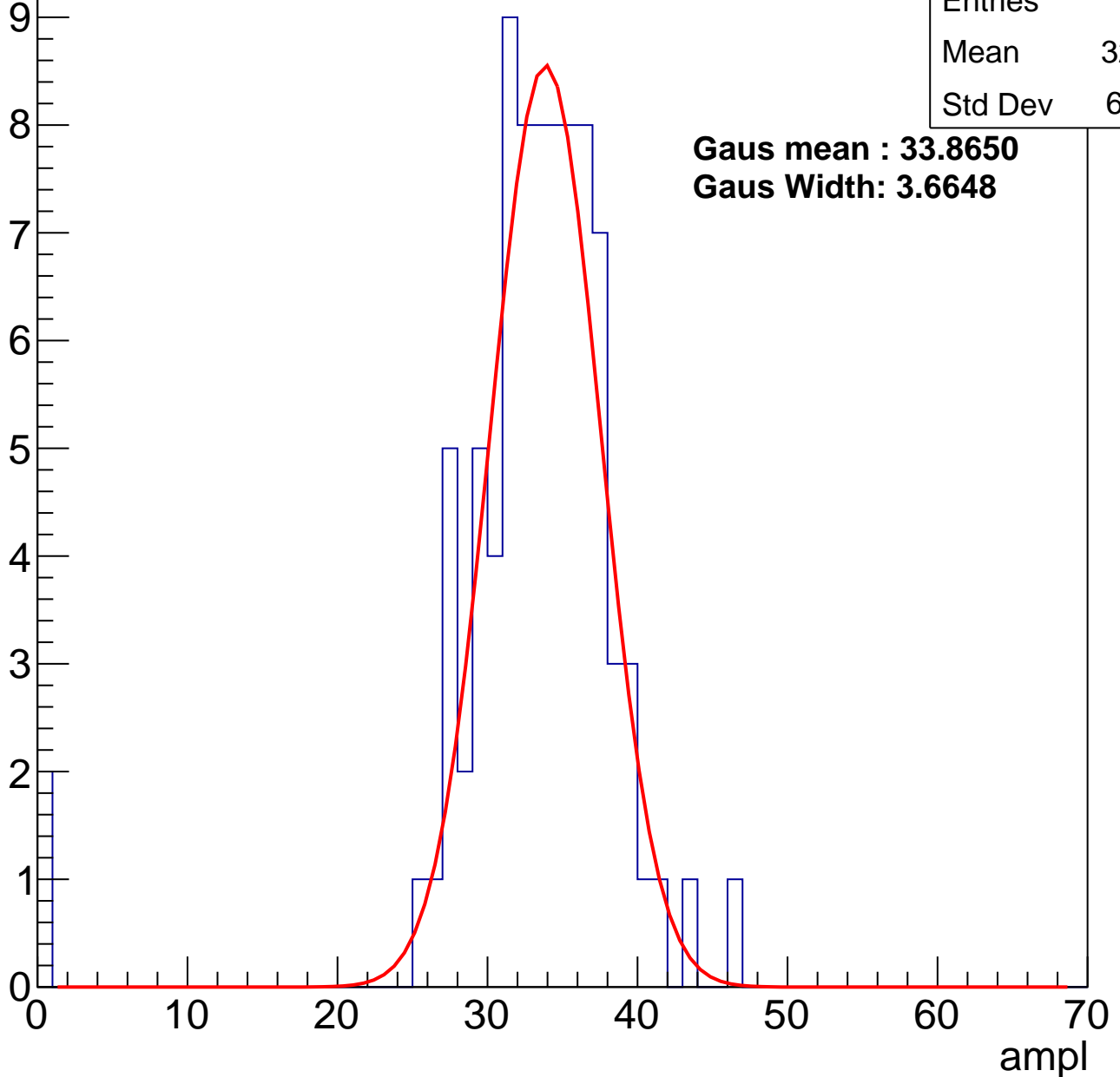
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	86
Mean	32.63
Std Dev	6.341

Gaus mean : 33.8650

Gaus Width: 3.6648



B1L103S, U7-ch126, adc2

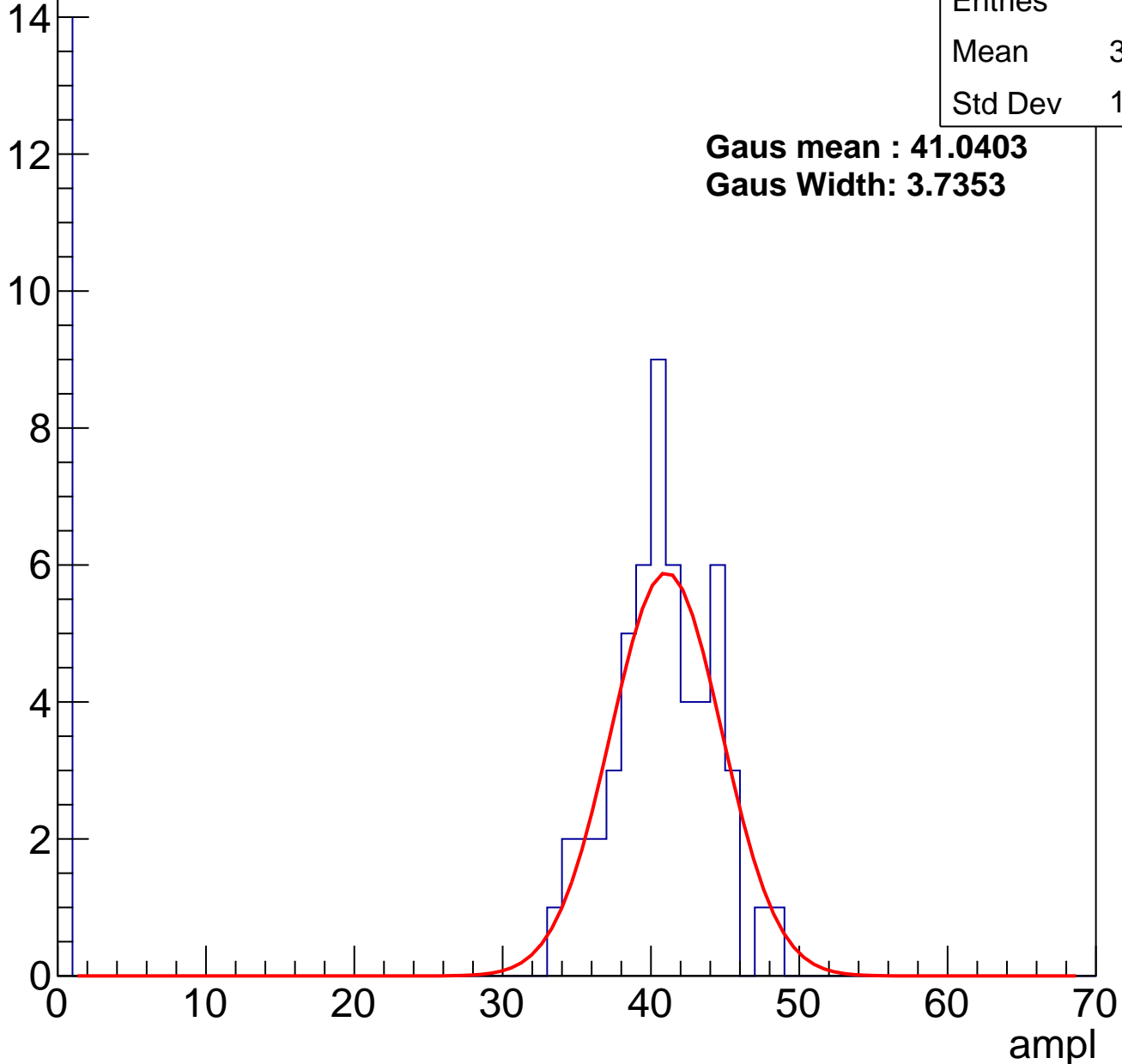
calib_packv5_041523_1651.root, FC#0, port C2

Entries	69
Mean	32.14
Std Dev	16.48

Gaus mean : 41.0403

Gaus Width: 3.7353

Entry

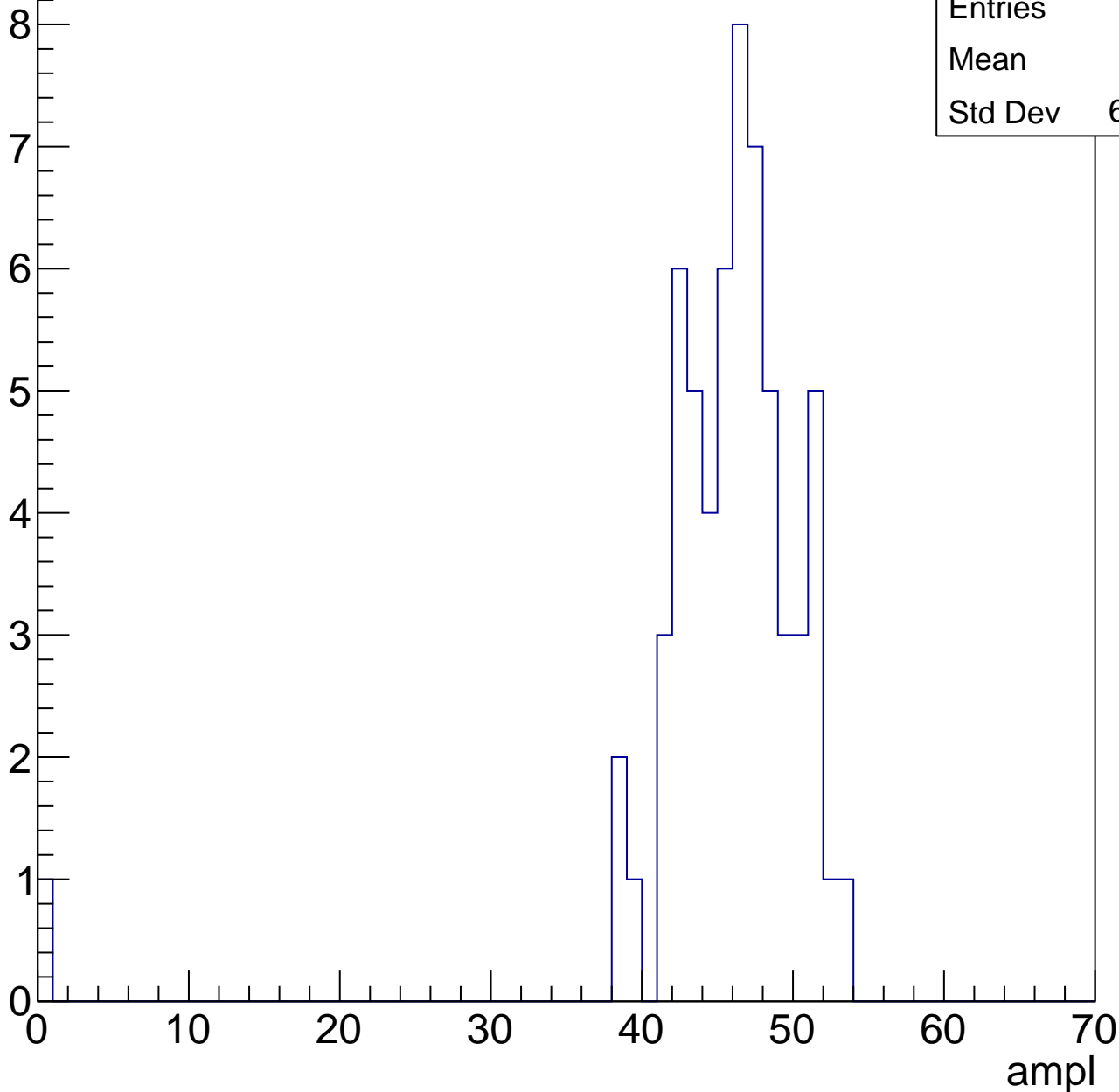


B1L103S, U7-ch126, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	61
Mean	45
Std Dev	6.753

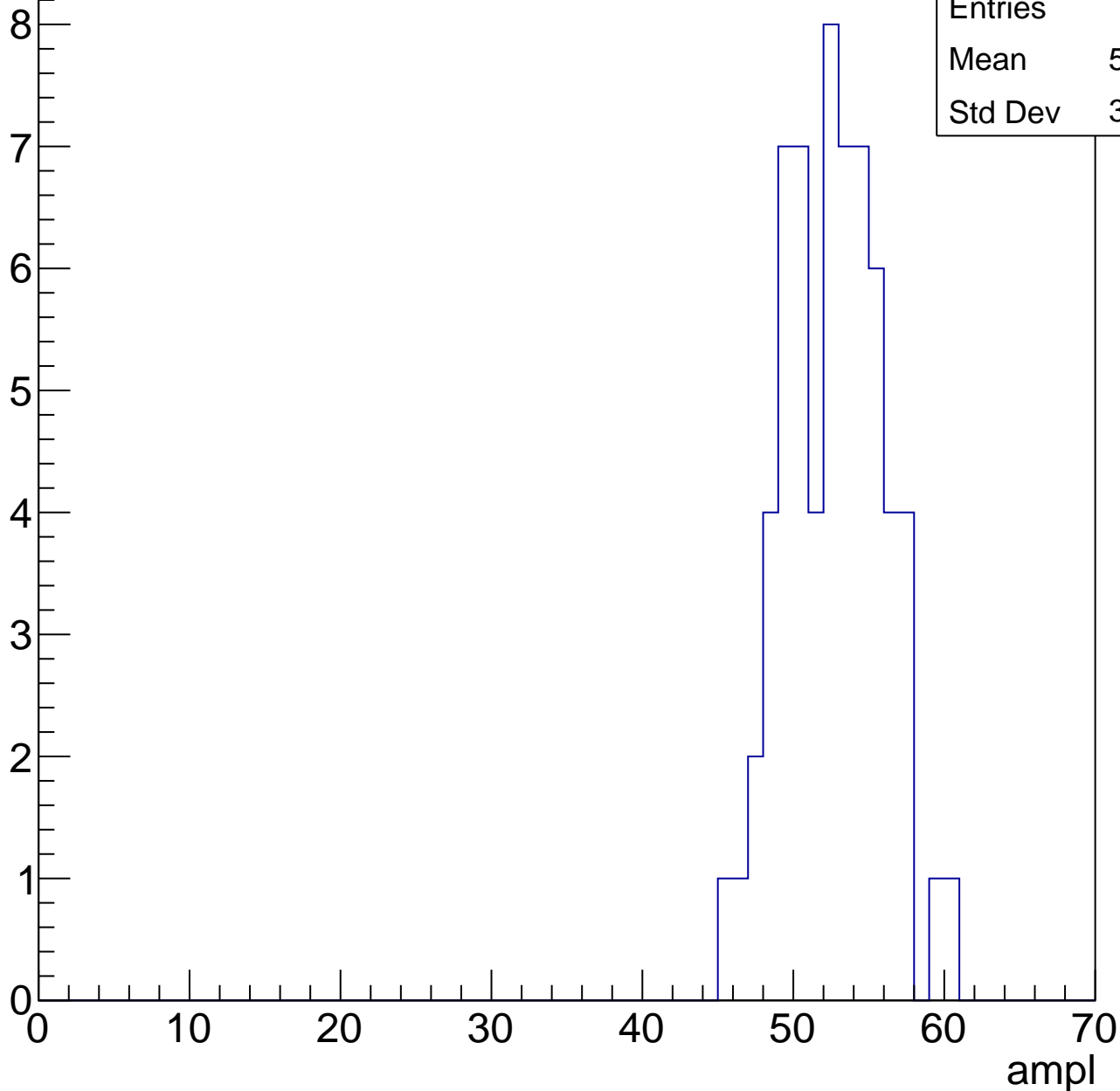


B1L103S, U7-ch126, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

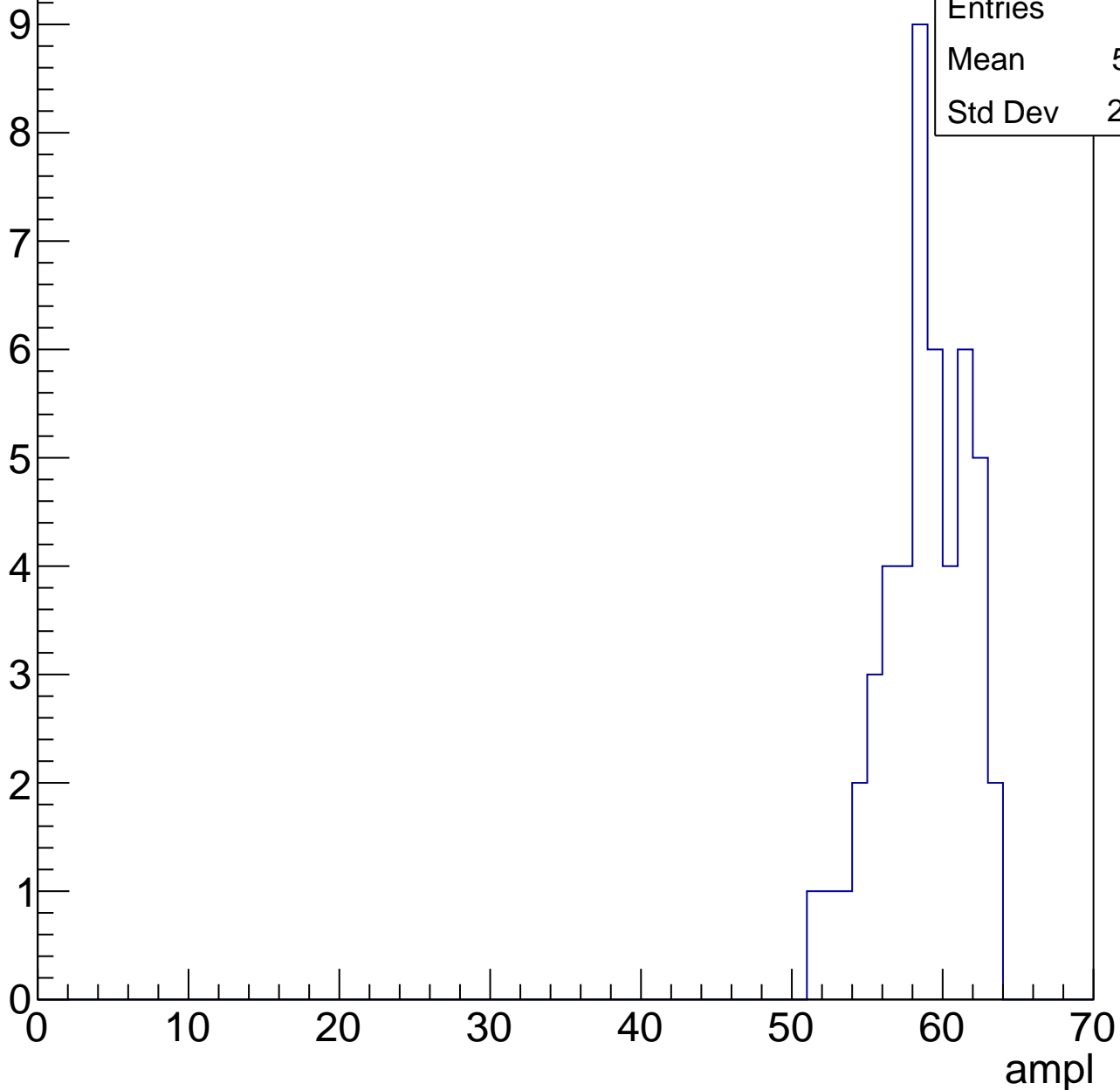
Entries	64
Mean	52.19
Std Dev	3.206



B1L103S, U7-ch126, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry



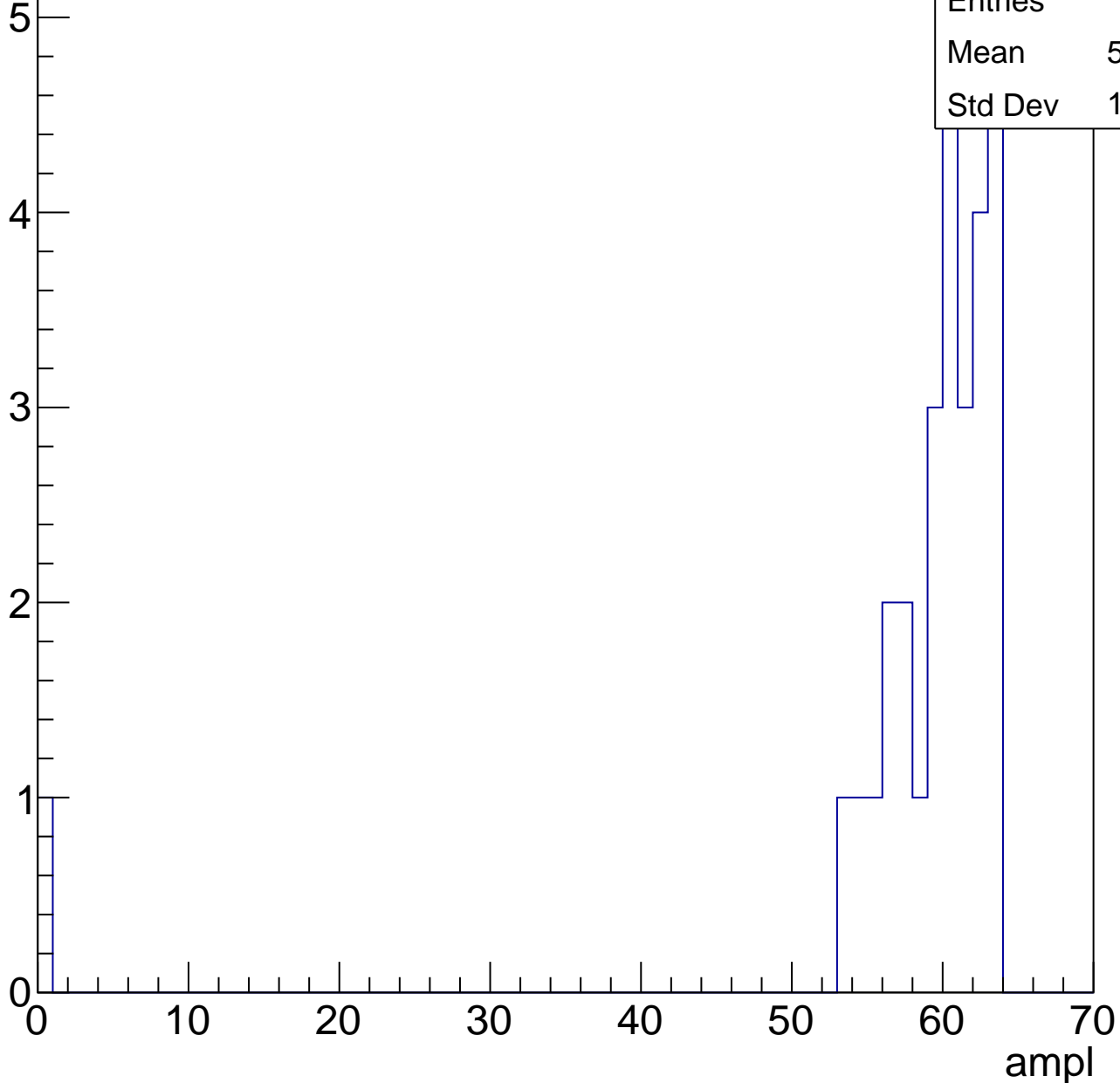
Entries	48
Mean	58.31
Std Dev	2.852

B1L103S, U7-ch126, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	29
Mean	57.55
Std Dev	11.23

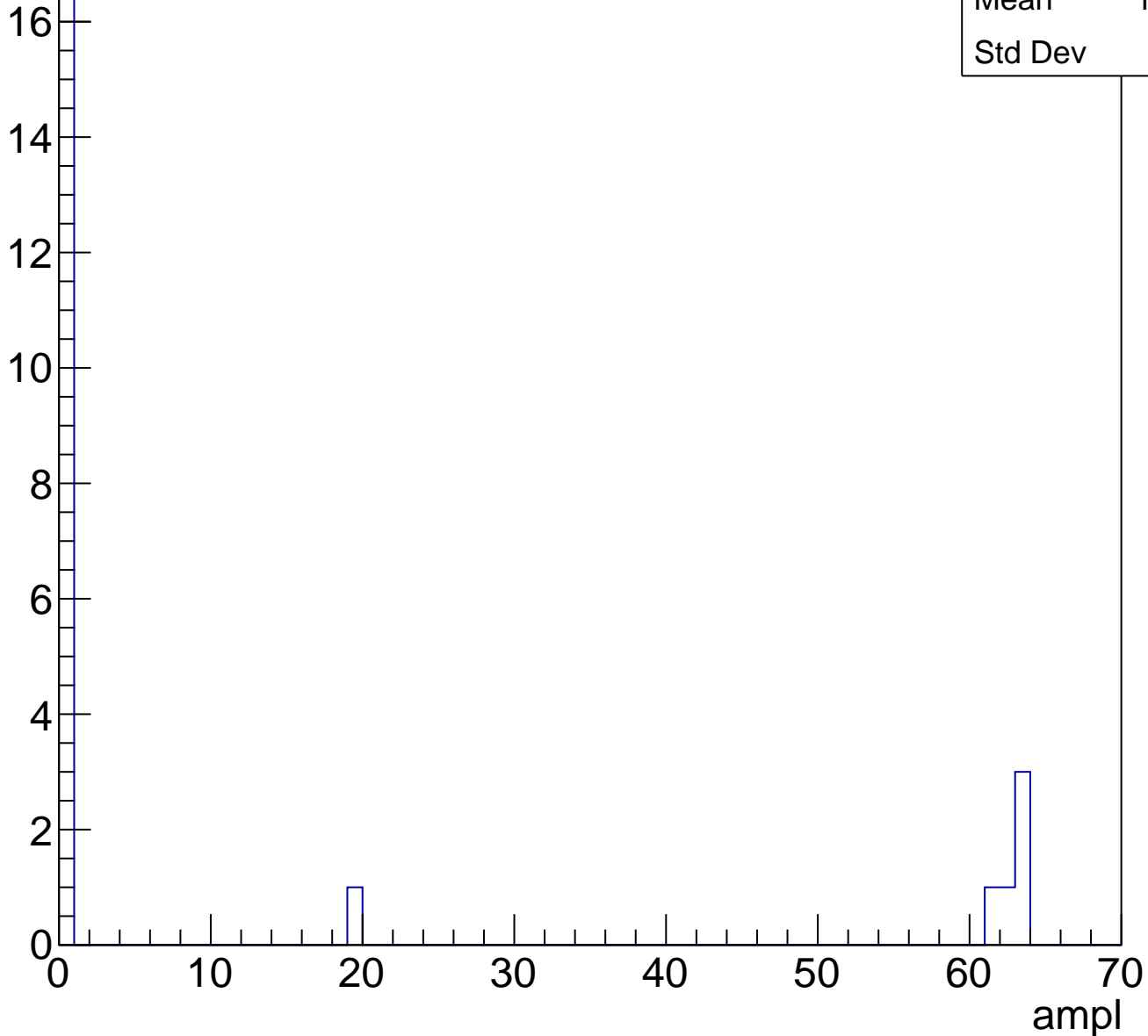


B1L103S, U7-ch126, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	23
Mean	14.39
Std Dev	25.6

Entry



B1L103S, U7-ch127, adc0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	92
Mean	23.36
Std Dev	10.23

Gaus mean : 27.3908

Gaus Width: 4.0695

Entry

12

10

8

6

4

2

0

0

10

20

30

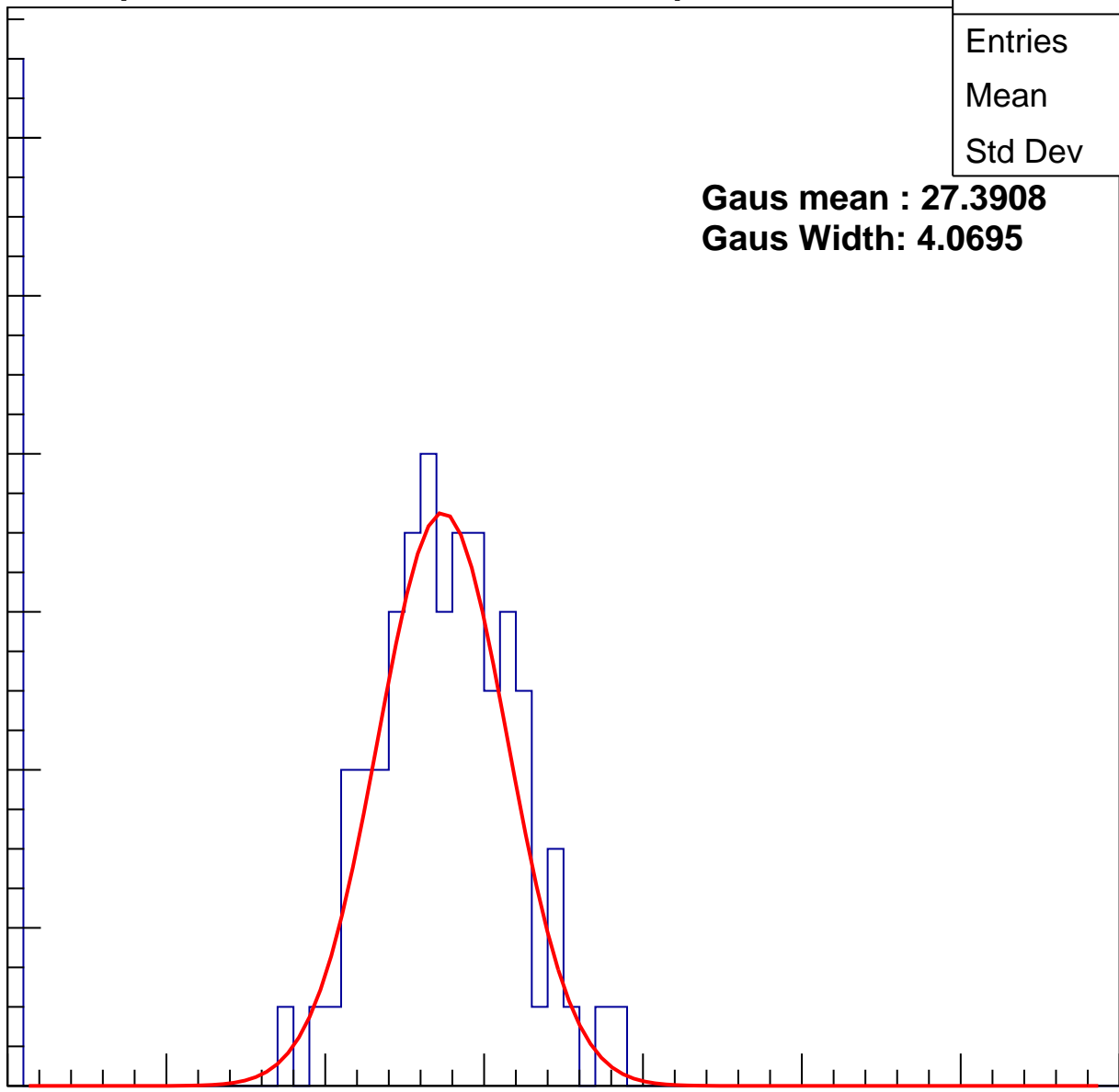
40

50

60

70

ampl



B1L103S, U7-ch127, adc1

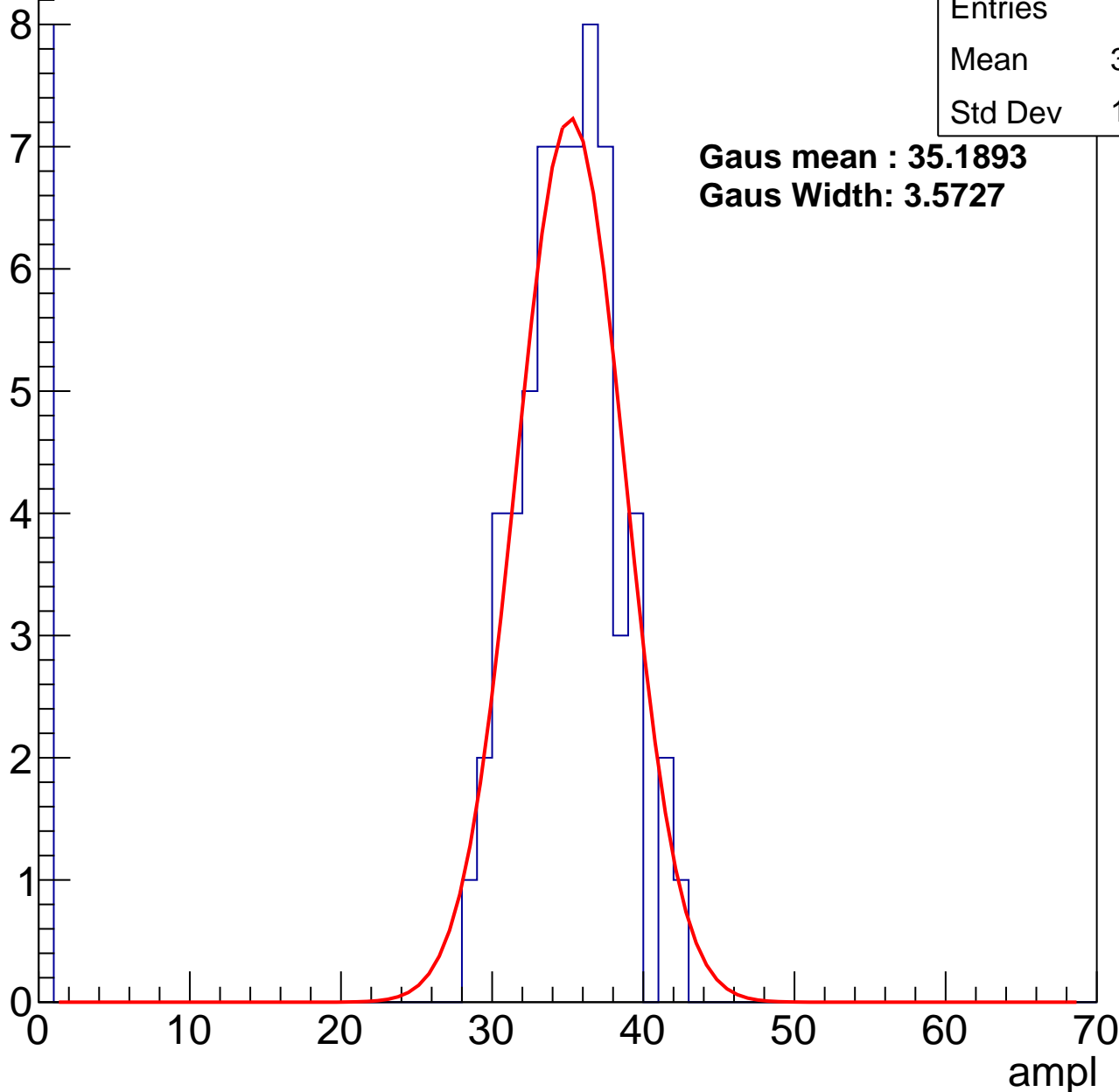
calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	70
Mean	30.64
Std Dev	11.39

Gaus mean : 35.1893

Gaus Width: 3.5727



B1L103S, U7-ch127, adc2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	81
Mean	36.96
Std Dev	13.5

Gaus mean : 42.2035

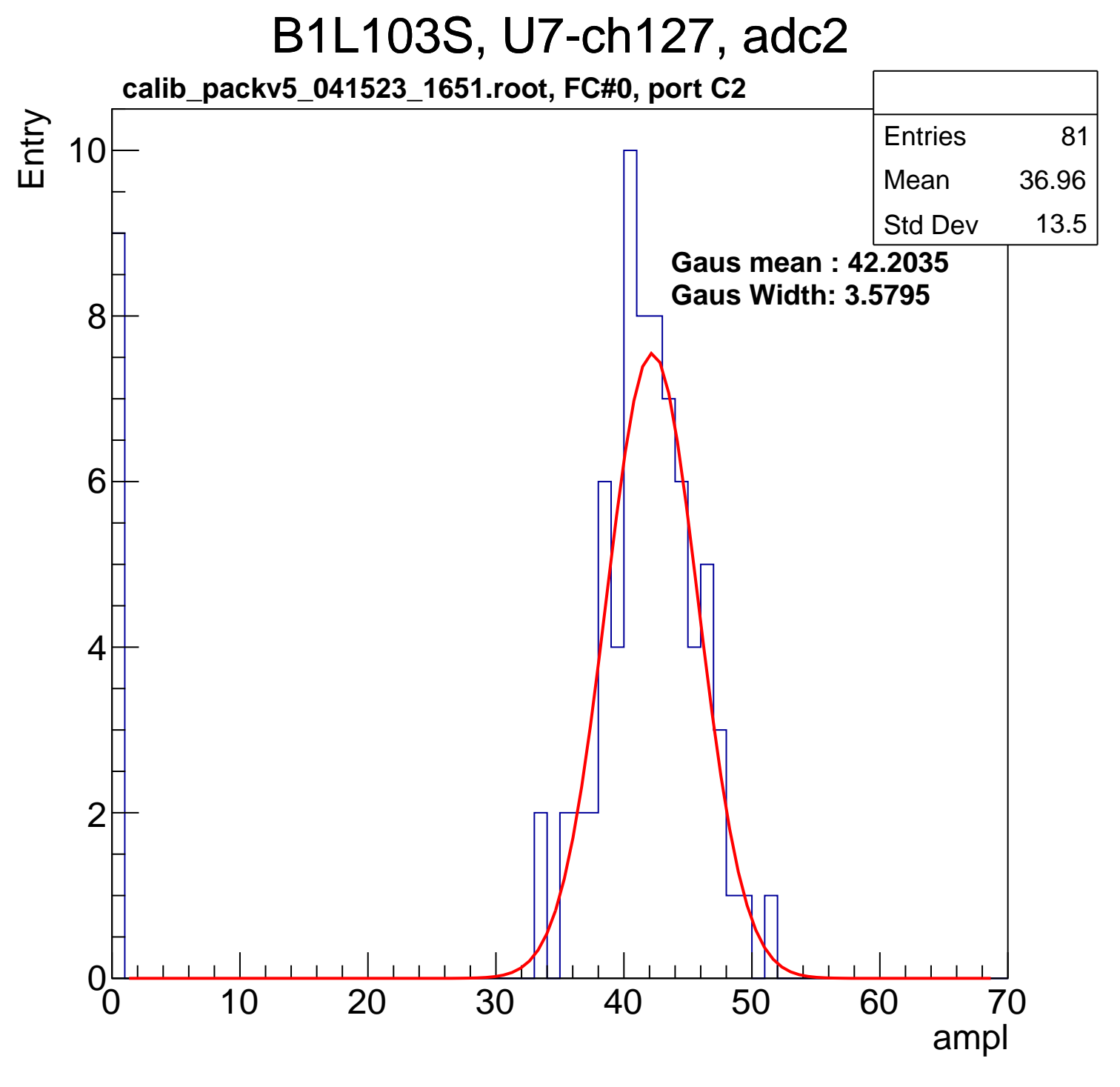
Gaus Width: 3.5795

Entry

10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70

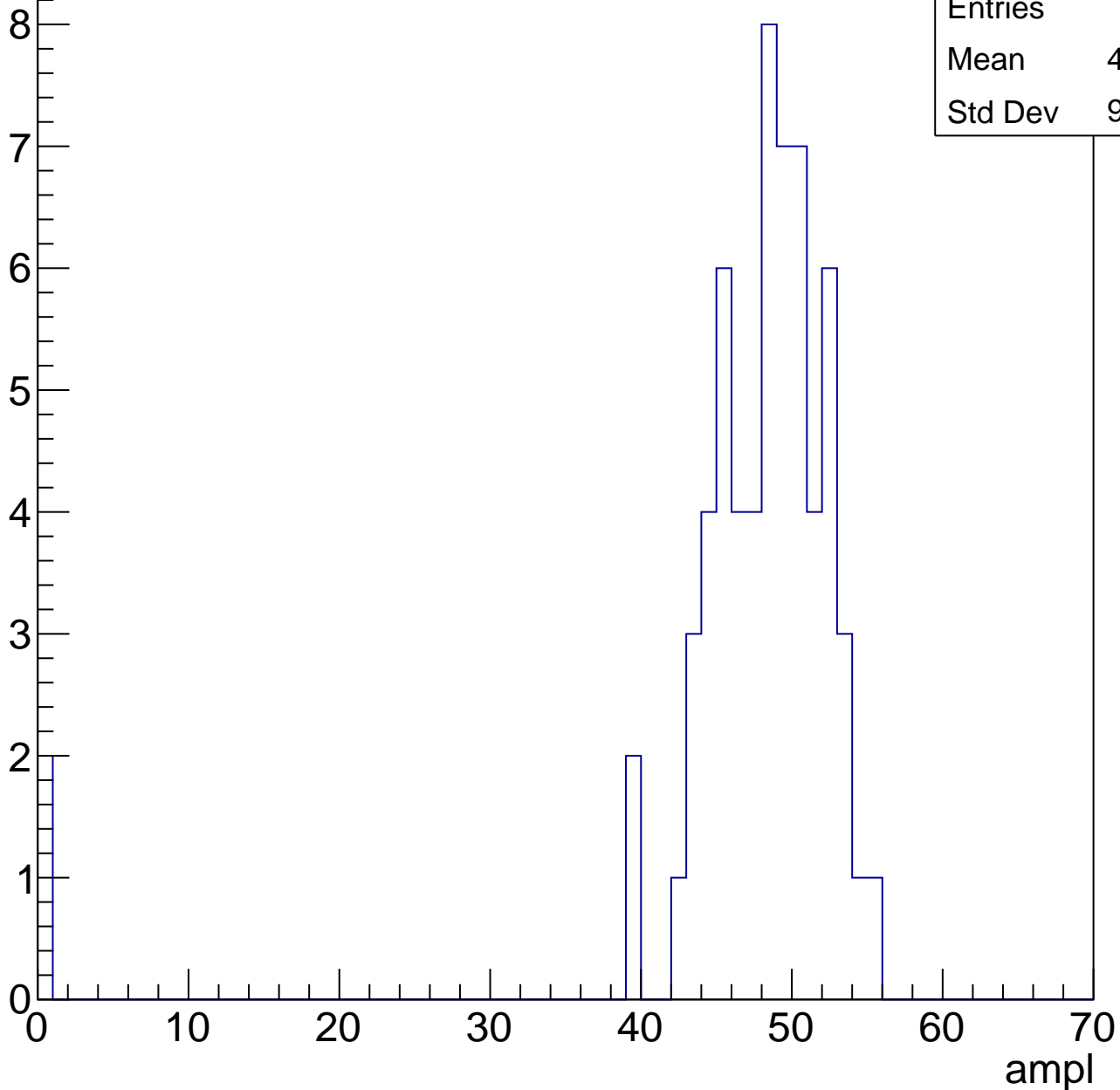


B1L103S, U7-ch127, adc3

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	63
Mean	46.48
Std Dev	9.085

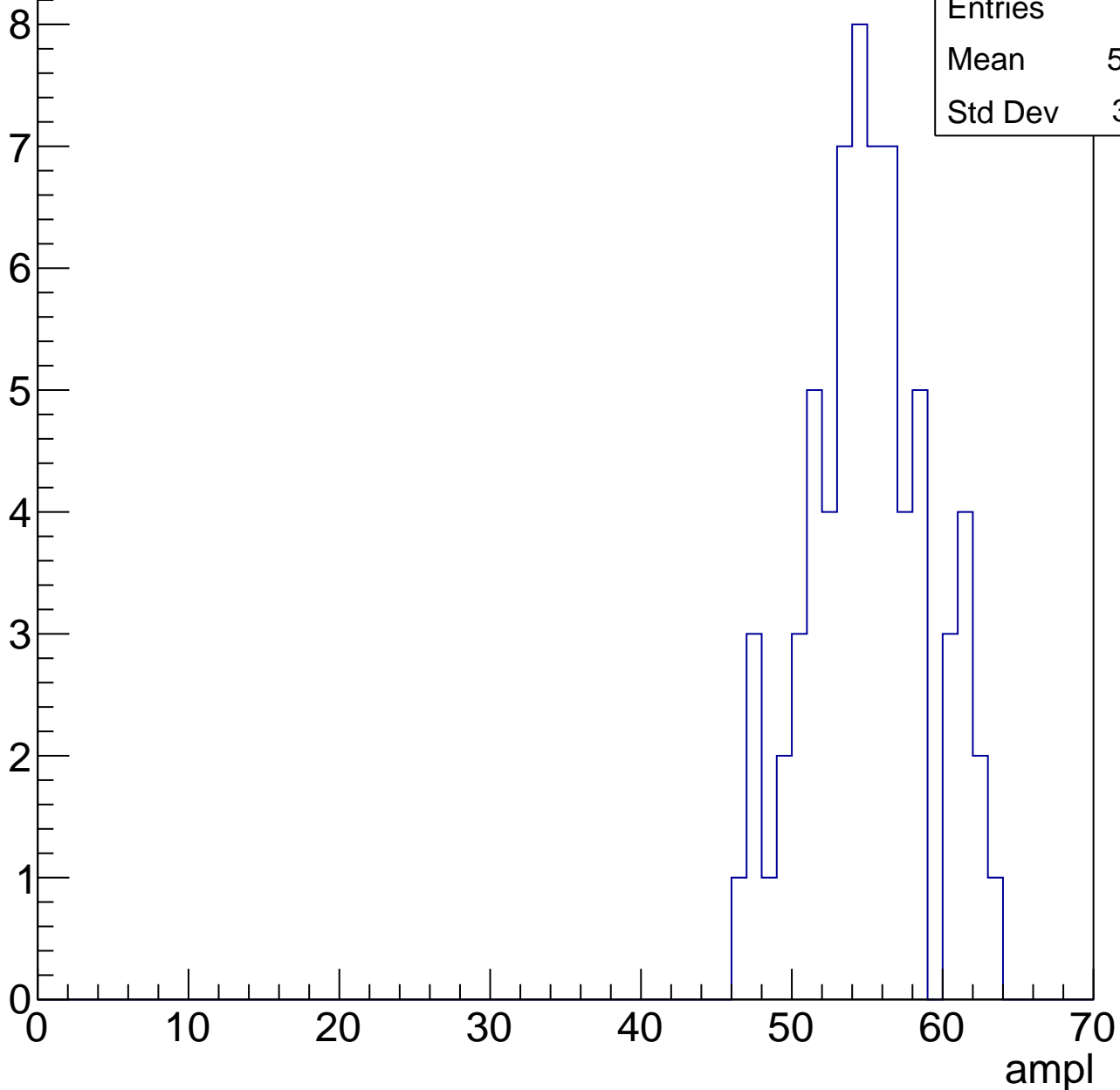


B1L103S, U7-ch127, adc4

calib_packv5_041523_1651.root, FC#0, port C2

Entry

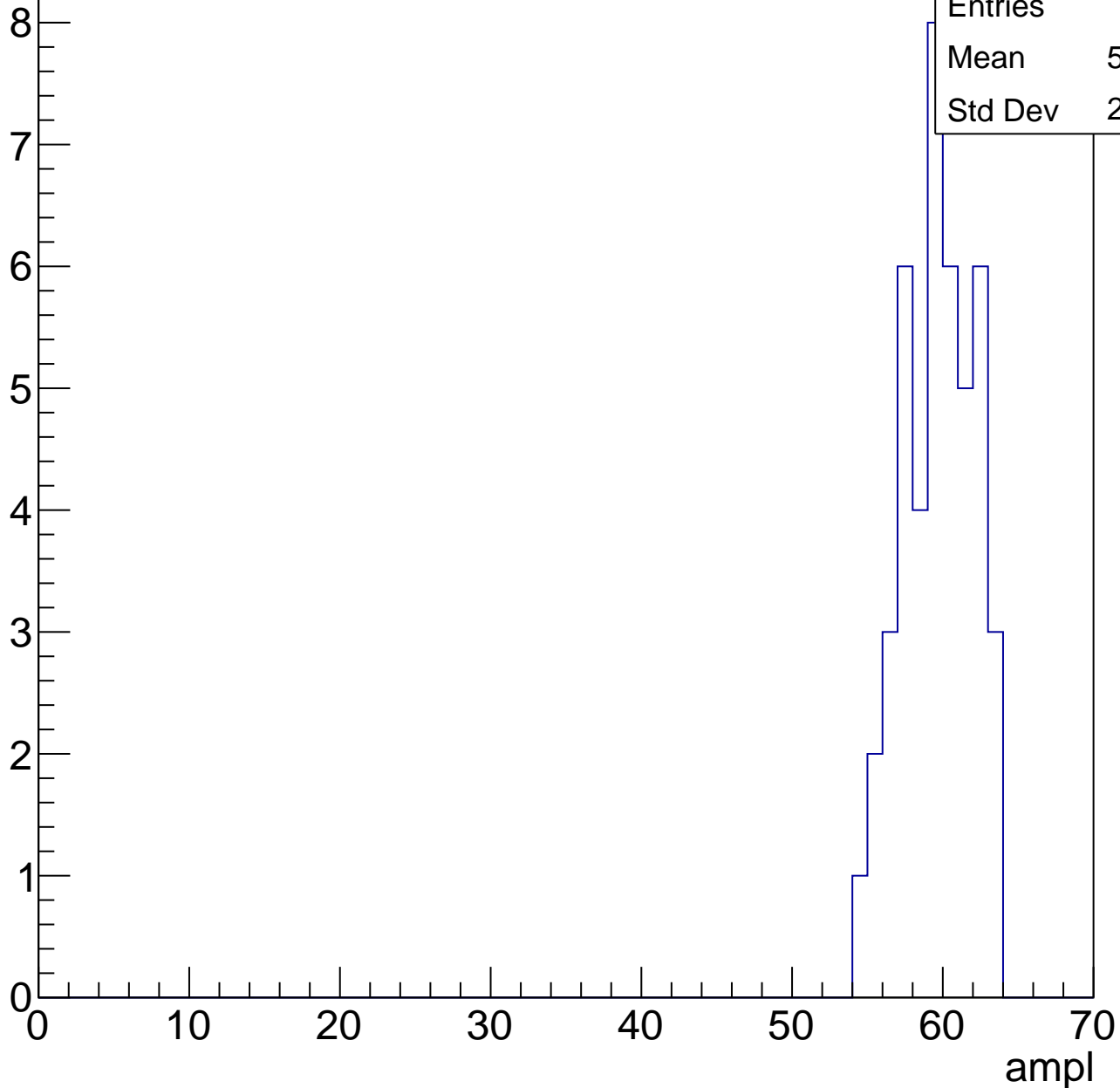
Entries	67
Mean	54.55
Std Dev	3.971



B1L103S, U7-ch127, adc5

calib_packv5_041523_1651.root, FC#0, port C2

Entry

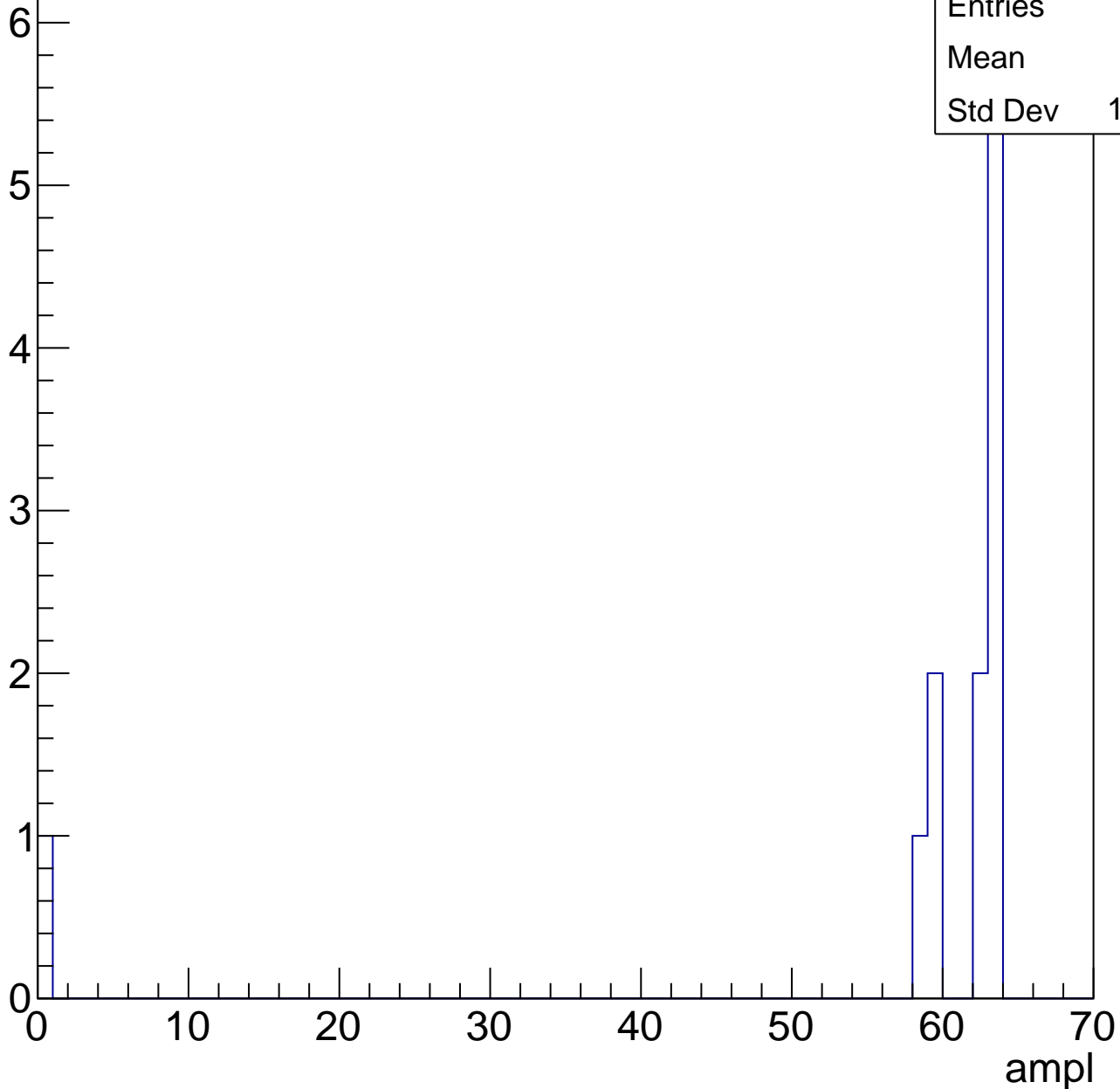


B1L103S, U7-ch127, adc6

calib_packv5_041523_1651.root, FC#0, port C2

Entry

Entries	12
Mean	56.5
Std Dev	17.13



B1L103S, U7-ch127, adc7

calib_packv5_041523_1651.root, FC#0, port C2

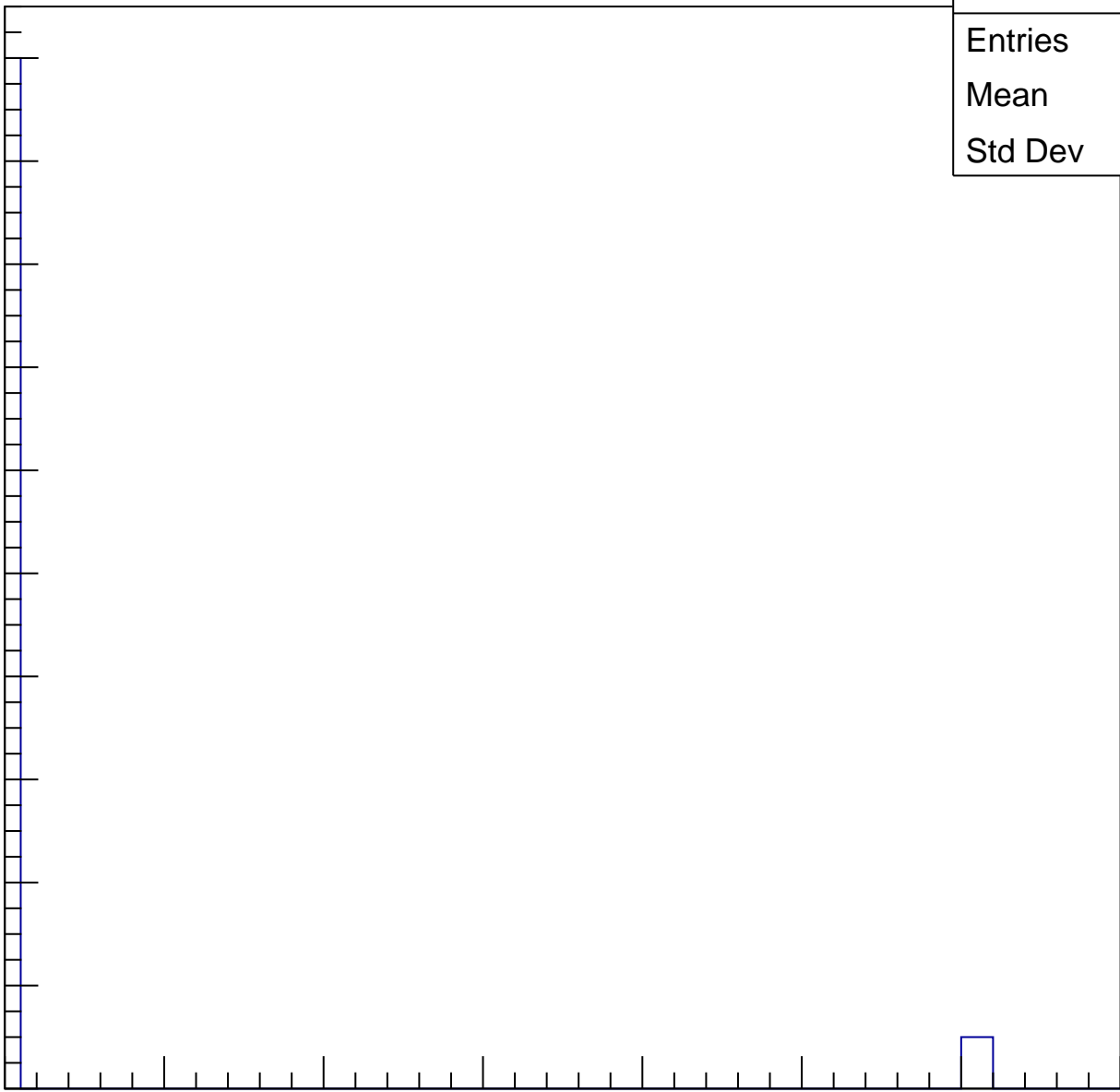
Entries	22
Mean	5.5
Std Dev	17.39

Entry

20
18
16
14
12
10
8
6
4
2
0

0 10 20 30 40 50 60 70

ampl



B1L103S, U7-ch127, adc7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	22
Mean	5.5
Std Dev	17.39

