

B1L100S, U8-ch0

calib_packv5_042523_0143.root, FC#4, port A2

Entries	397
Mean	43.36
Std Dev	12.12

Turn on : 24.5046

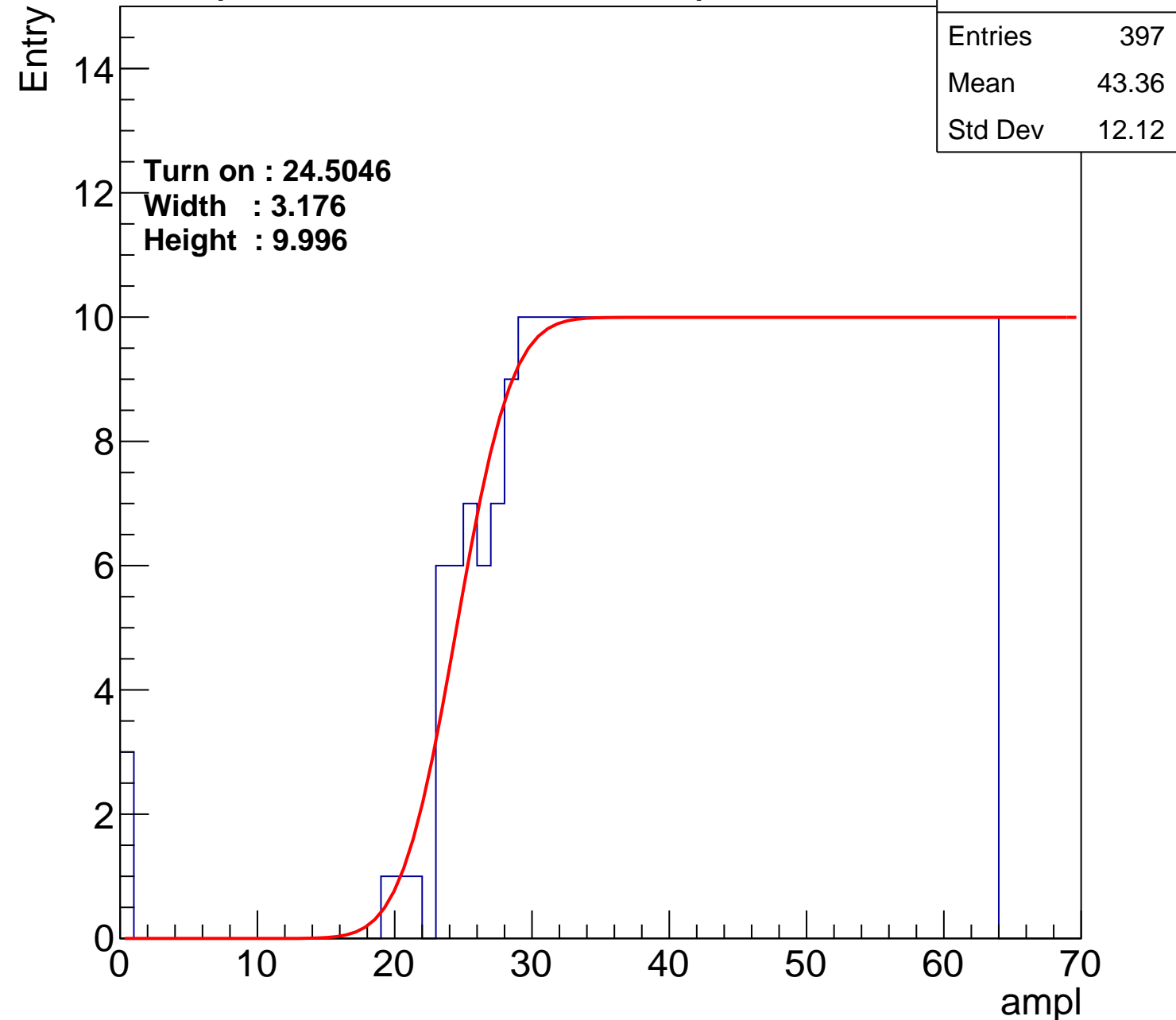
Width : 3.176

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch1

calib_packv5_042523_0143.root, FC#4, port A2

Entries	372
Mean	44.73
Std Dev	11.1

Turn on : 26.9720

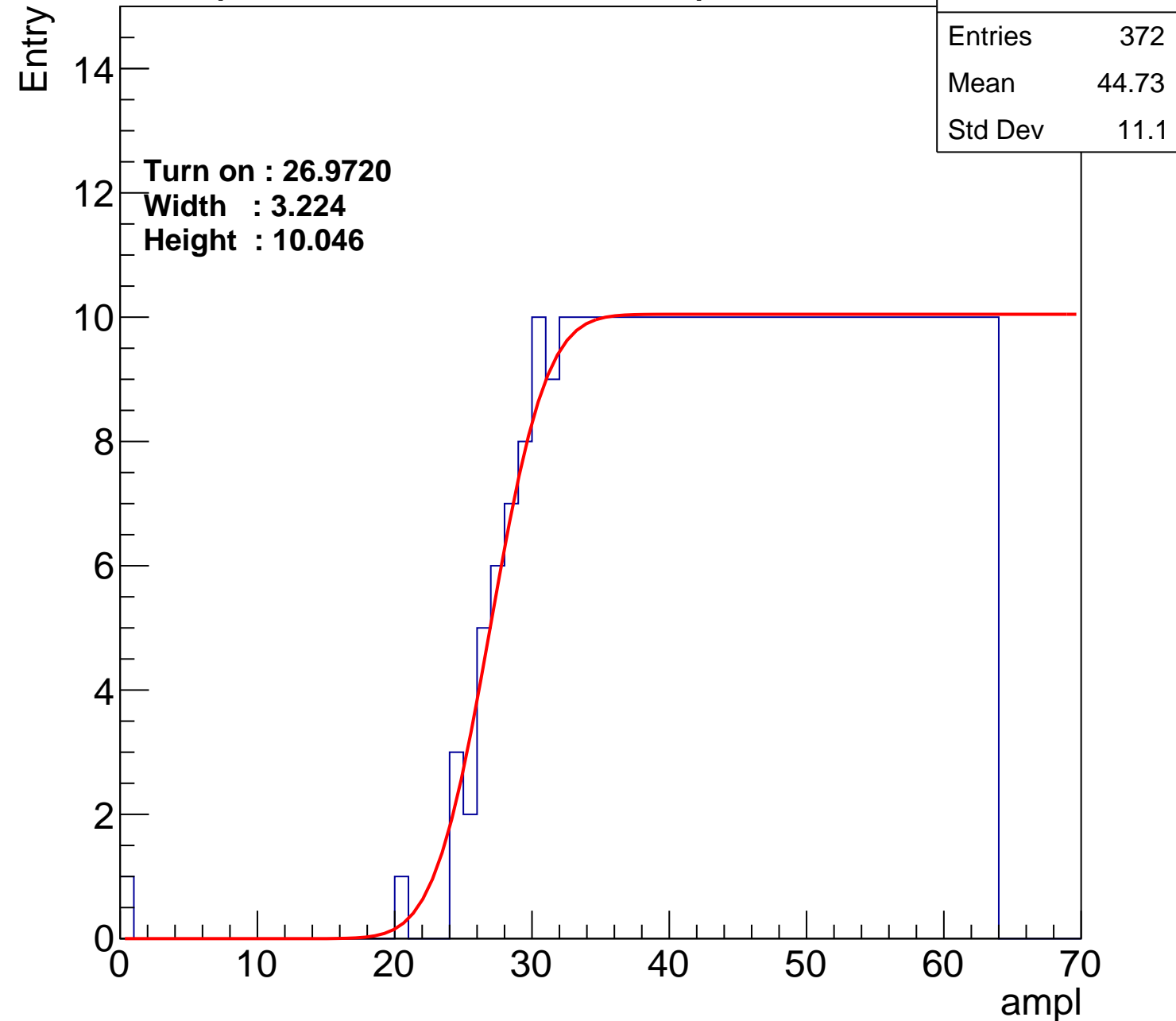
Width : 3.224

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch2

calib_packv5_042523_0143.root, FC#4, port A2

Entries	381
Mean	44.21
Std Dev	11.54

Turn on : 26.2332

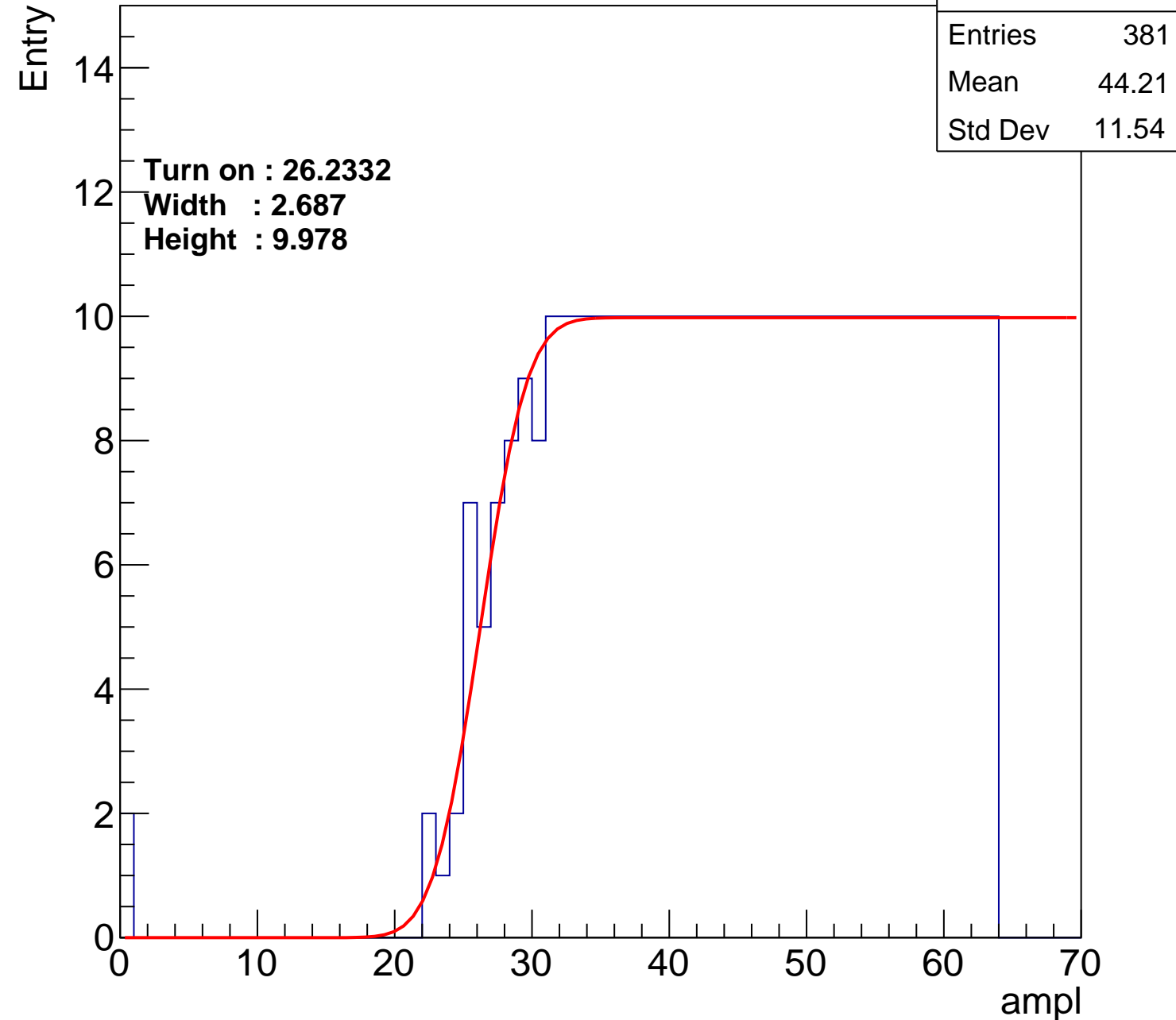
Width : 2.687

Height : 9.978

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch3

calib_packv5_042523_0143.root, FC#4, port A2

Entries	386
Mean	43.93
Std Dev	11.8

Turn on : 26.1442

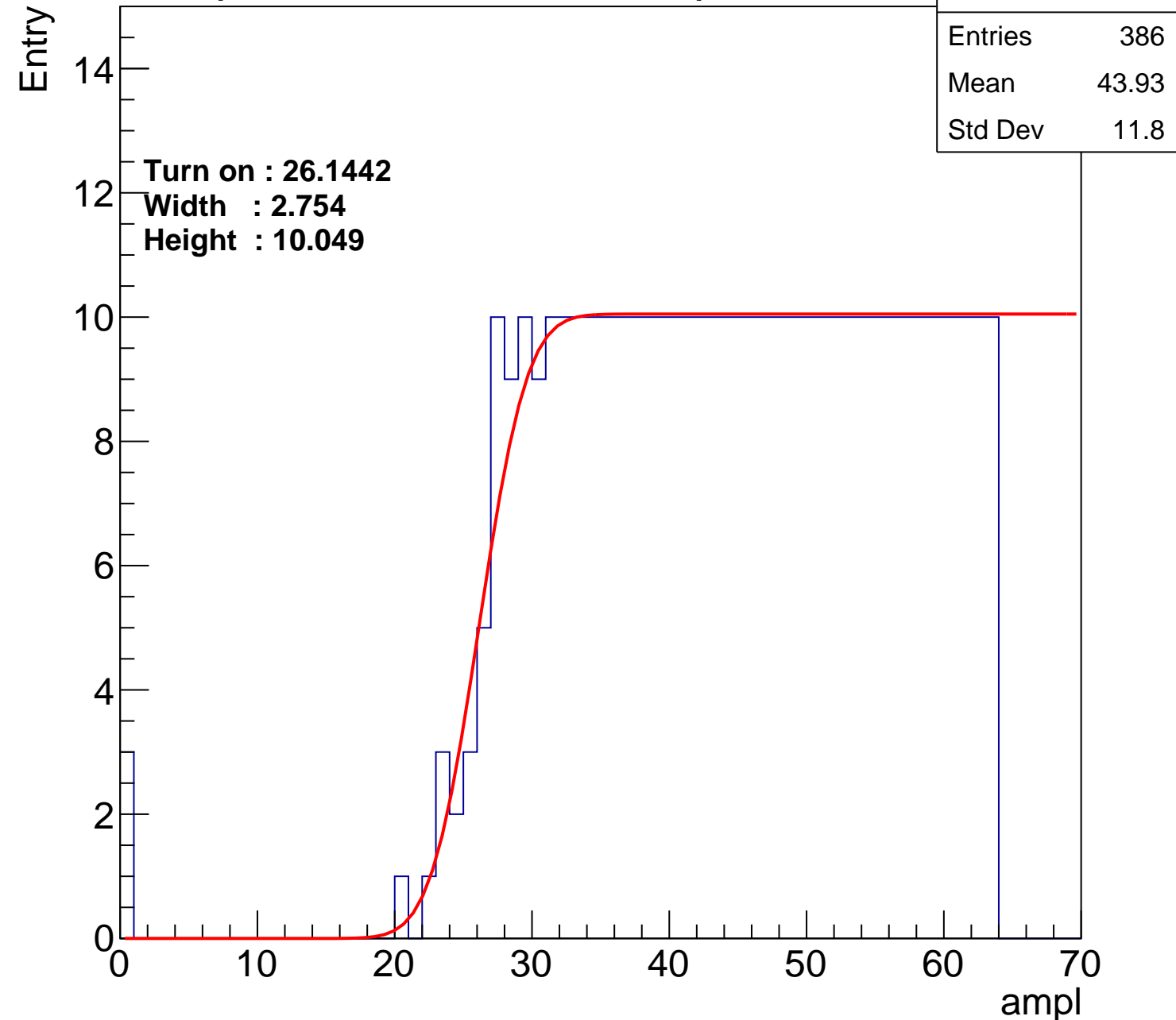
Width : 2.754

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch4

calib_packv5_042523_0143.root, FC#4, port A2

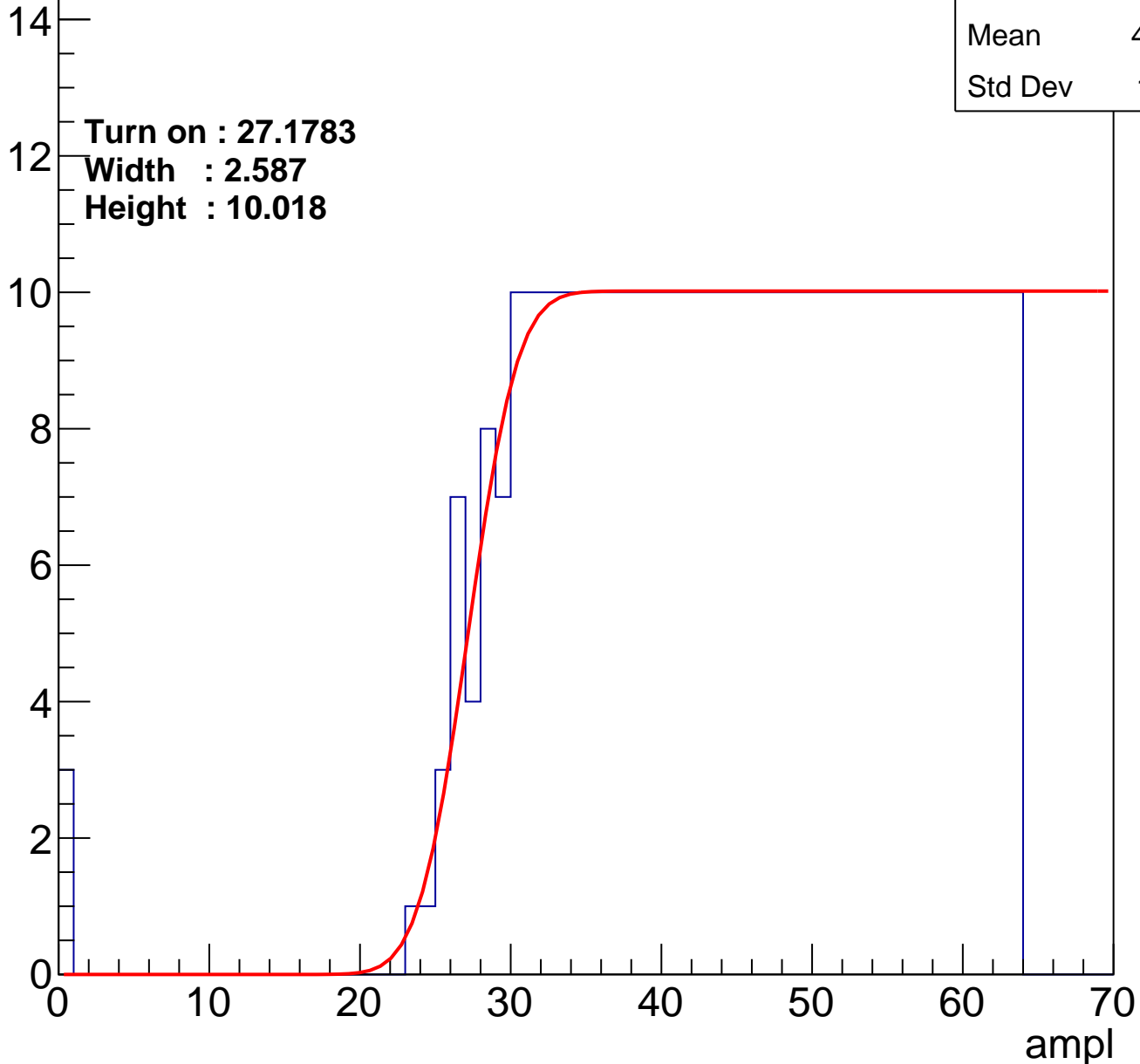
Entries	374
Mean	44.52
Std Dev	11.51

Turn on : 27.1783

Width : 2.587

Height : 10.018

Entry



B1L100S, U8-ch5

calib_packv5_042523_0143.root, FC#4, port A2

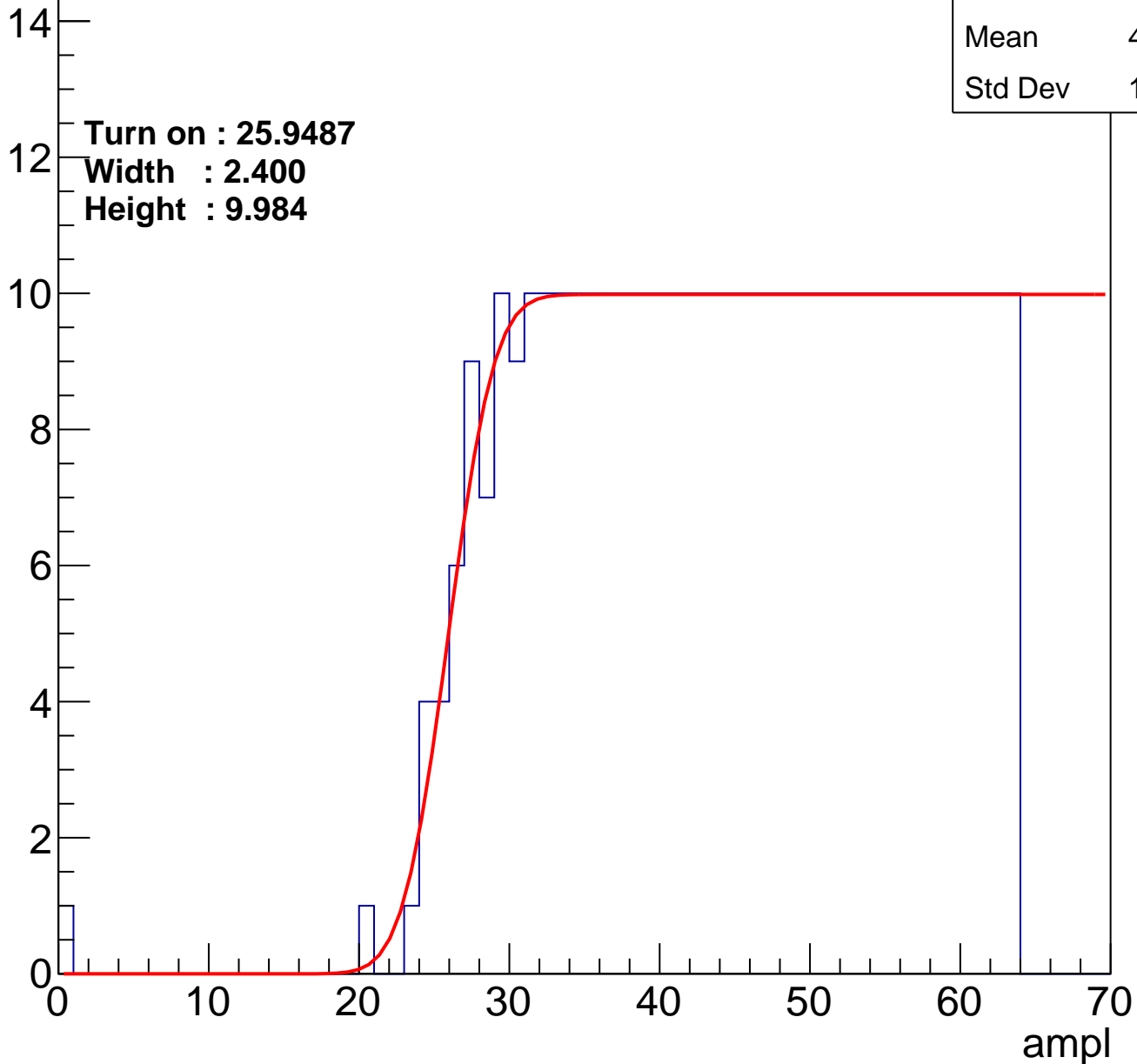
Entries	382
Mean	44.25
Std Dev	11.35

Turn on : 25.9487

Width : 2.400

Height : 9.984

Entry



B1L100S, U8-ch6

calib_packv5_042523_0143.root, FC#4, port A2

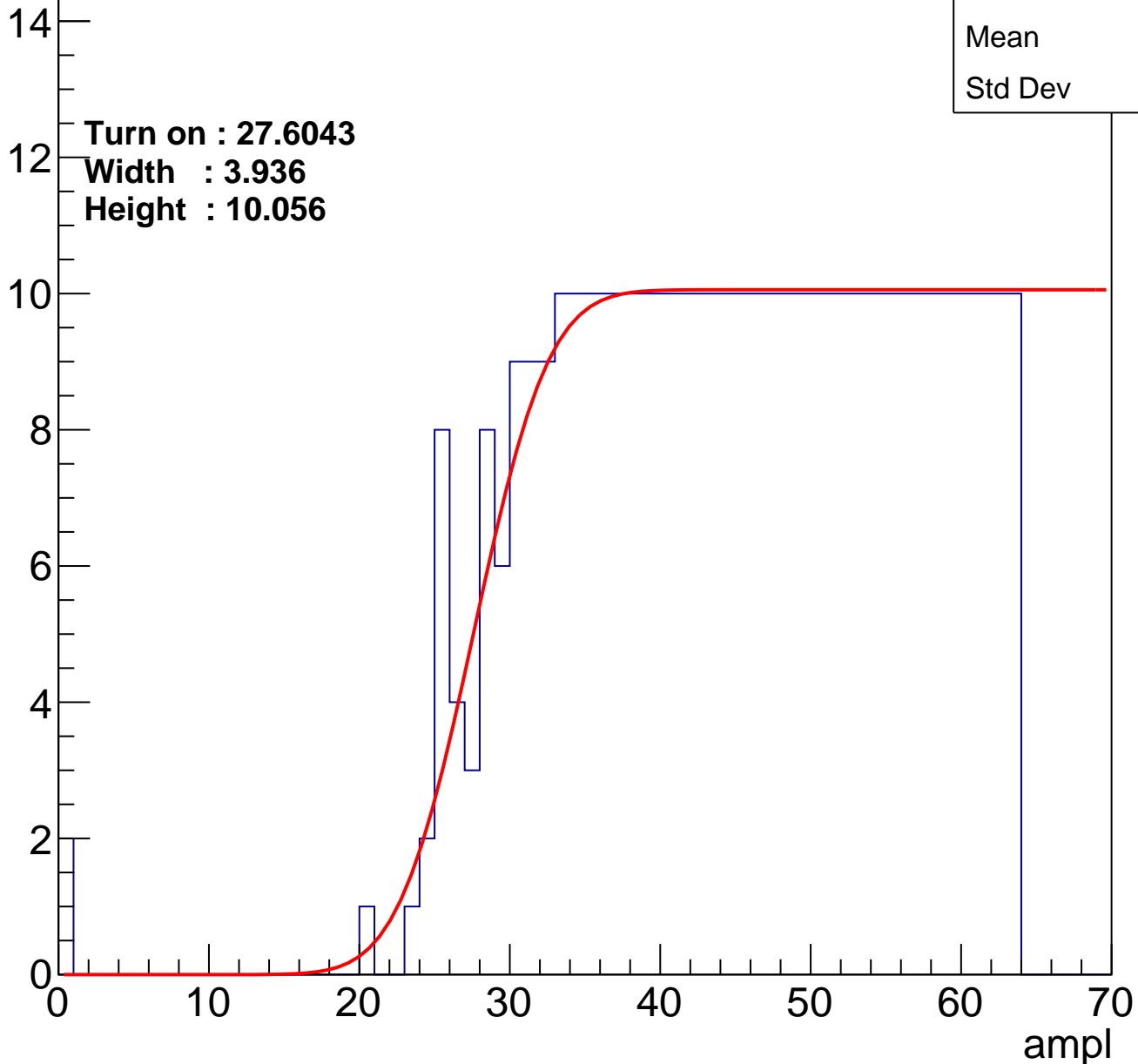
Entries	372
Mean	44.6
Std Dev	11.4

Turn on : 27.6043

Width : 3.936

Height : 10.056

Entry



B1L100S, U8-ch7

calib_packv5_042523_0143.root, FC#4, port A2

Entries	366
Mean	44.9
Std Dev	11.25

Turn on : 27.6687

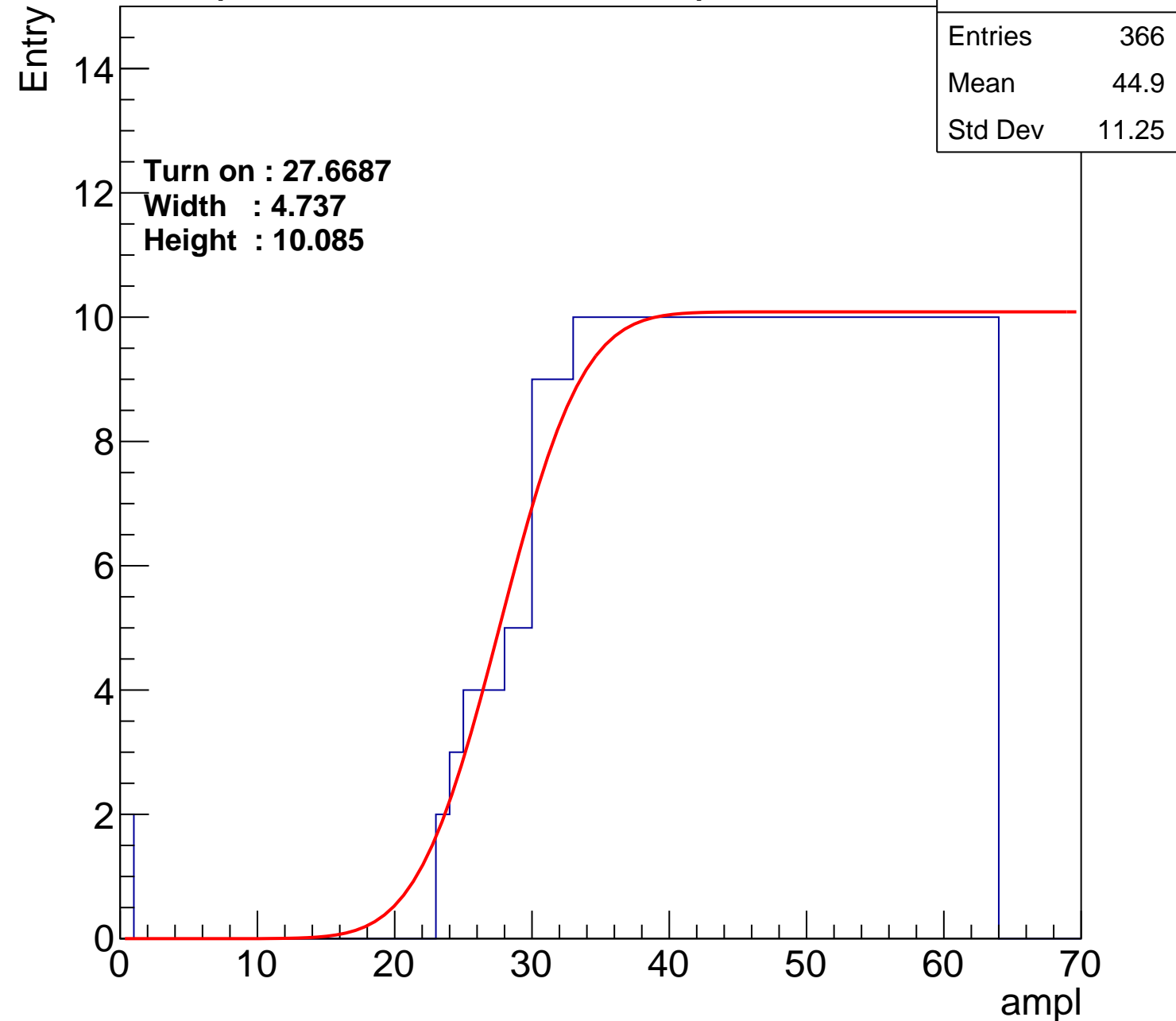
Width : 4.737

Height : 10.085

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch8

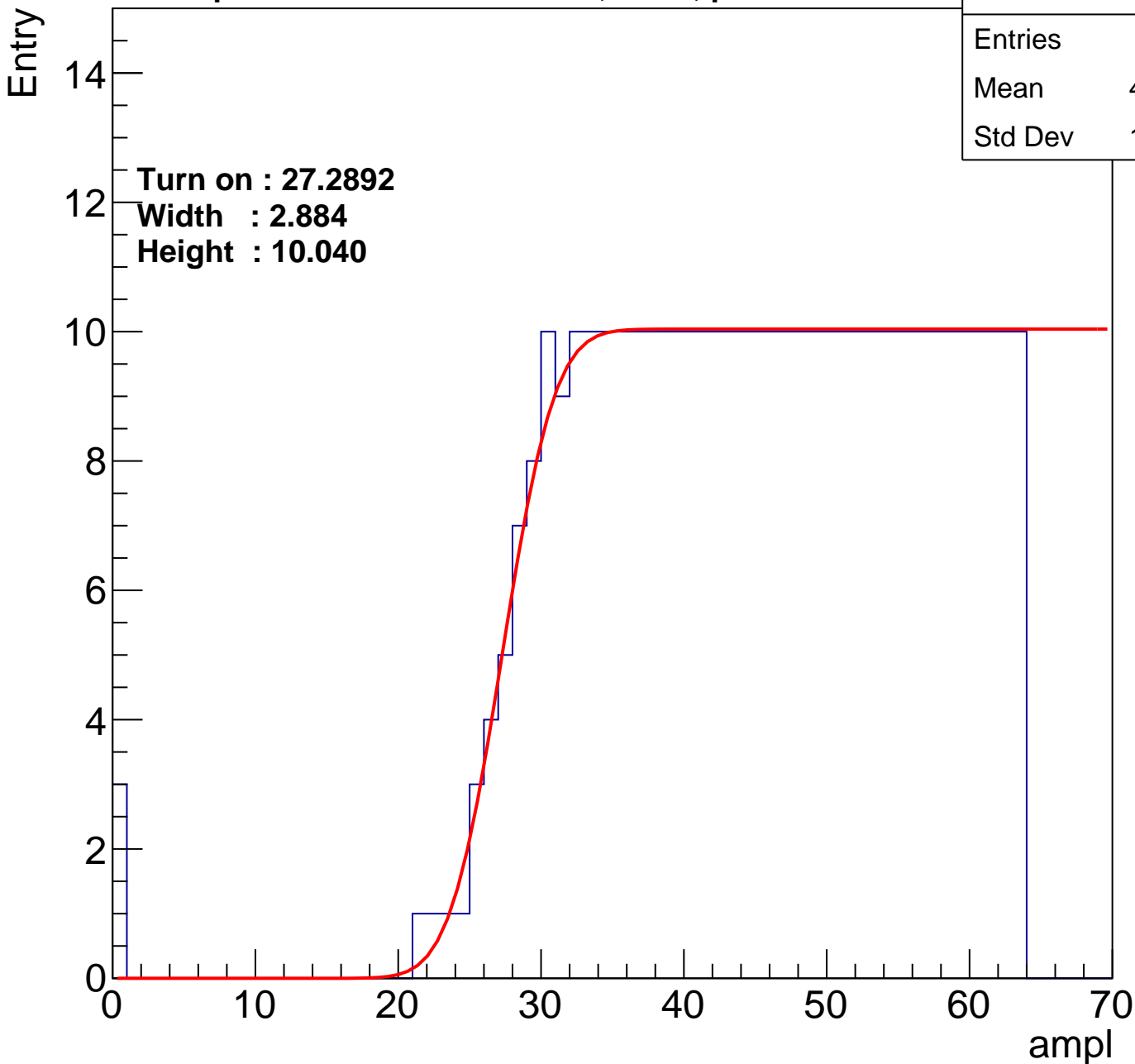
calib_packv5_042523_0143.root, FC#4, port A2

Entries	373
Mean	44.53
Std Dev	11.54

Turn on : 27.2892

Width : 2.884

Height : 10.040



B1L100S, U8-ch9

calib_packv5_042523_0143.root, FC#4, port A2

Entries	367
Mean	44.82
Std Dev	11.4

Turn on : 27.7155

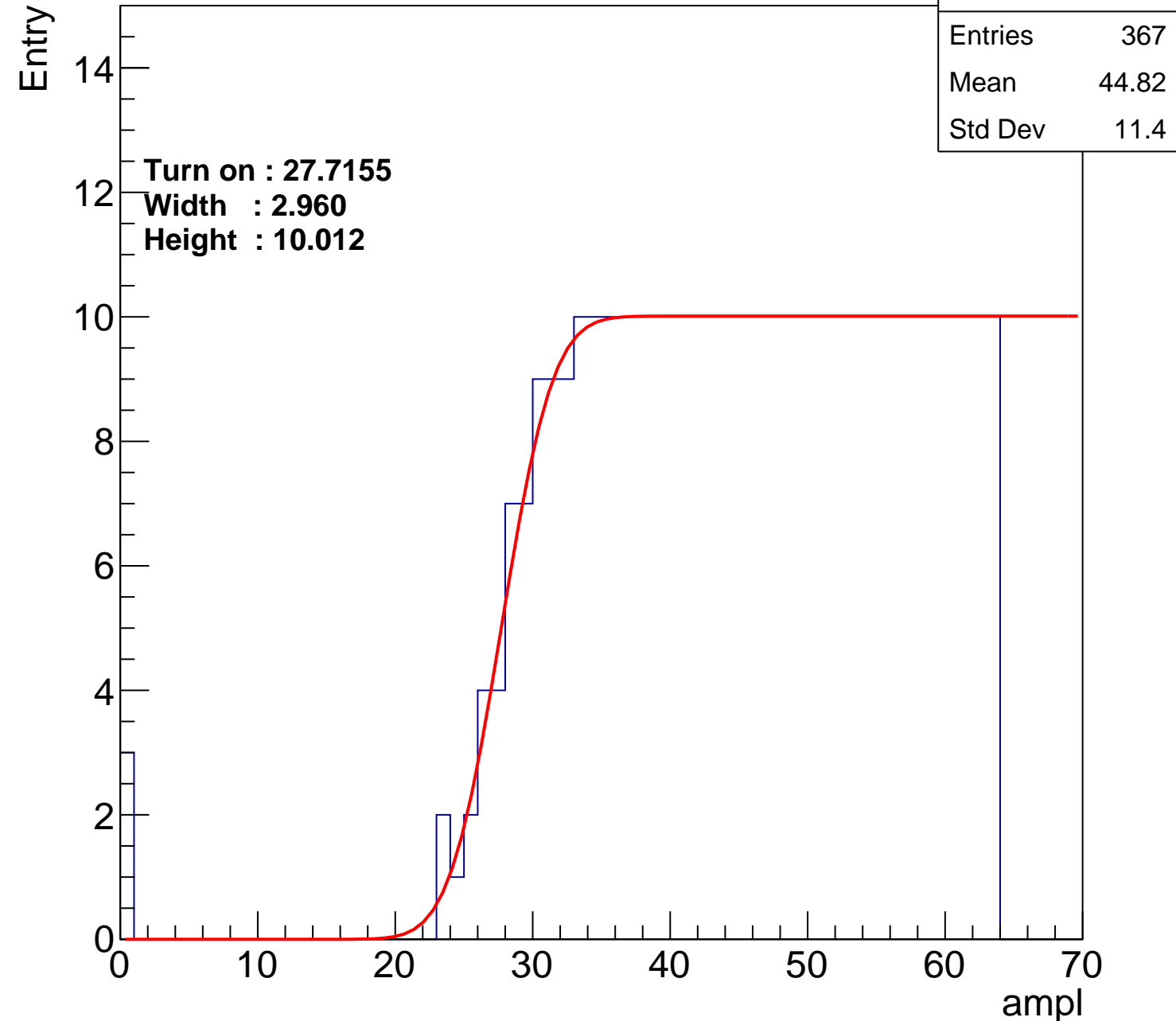
Width : 2.960

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch10

calib_packv5_042523_0143.root, FC#4, port A2

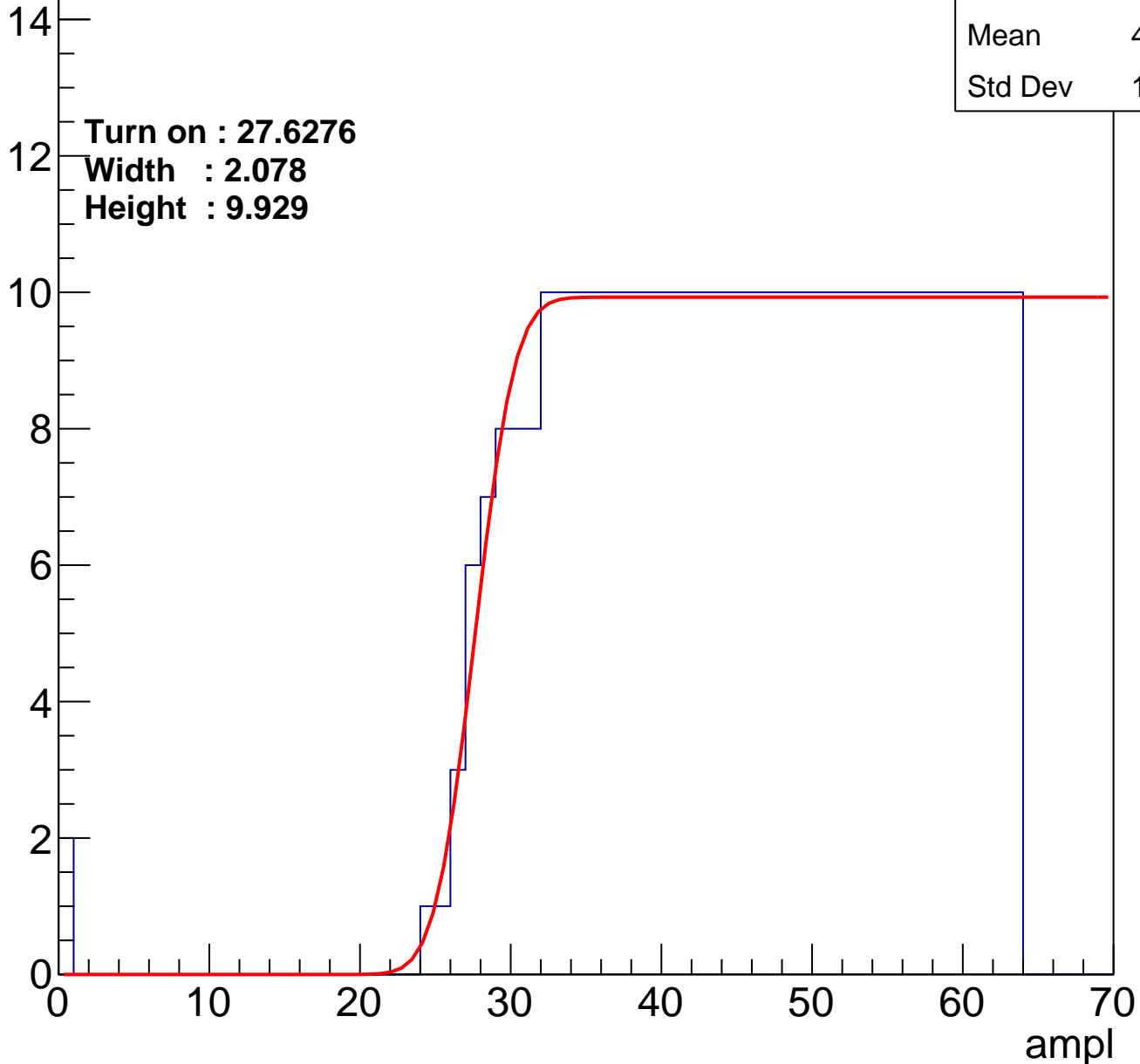
Entries	364
Mean	45.07
Std Dev	11.07

Turn on : 27.6276

Width : 2.078

Height : 9.929

Entry



B1L100S, U8-ch11

calib_packv5_042523_0143.root, FC#4, port A2

Entries	368
Mean	44.82
Std Dev	11.35

Turn on : 27.9809

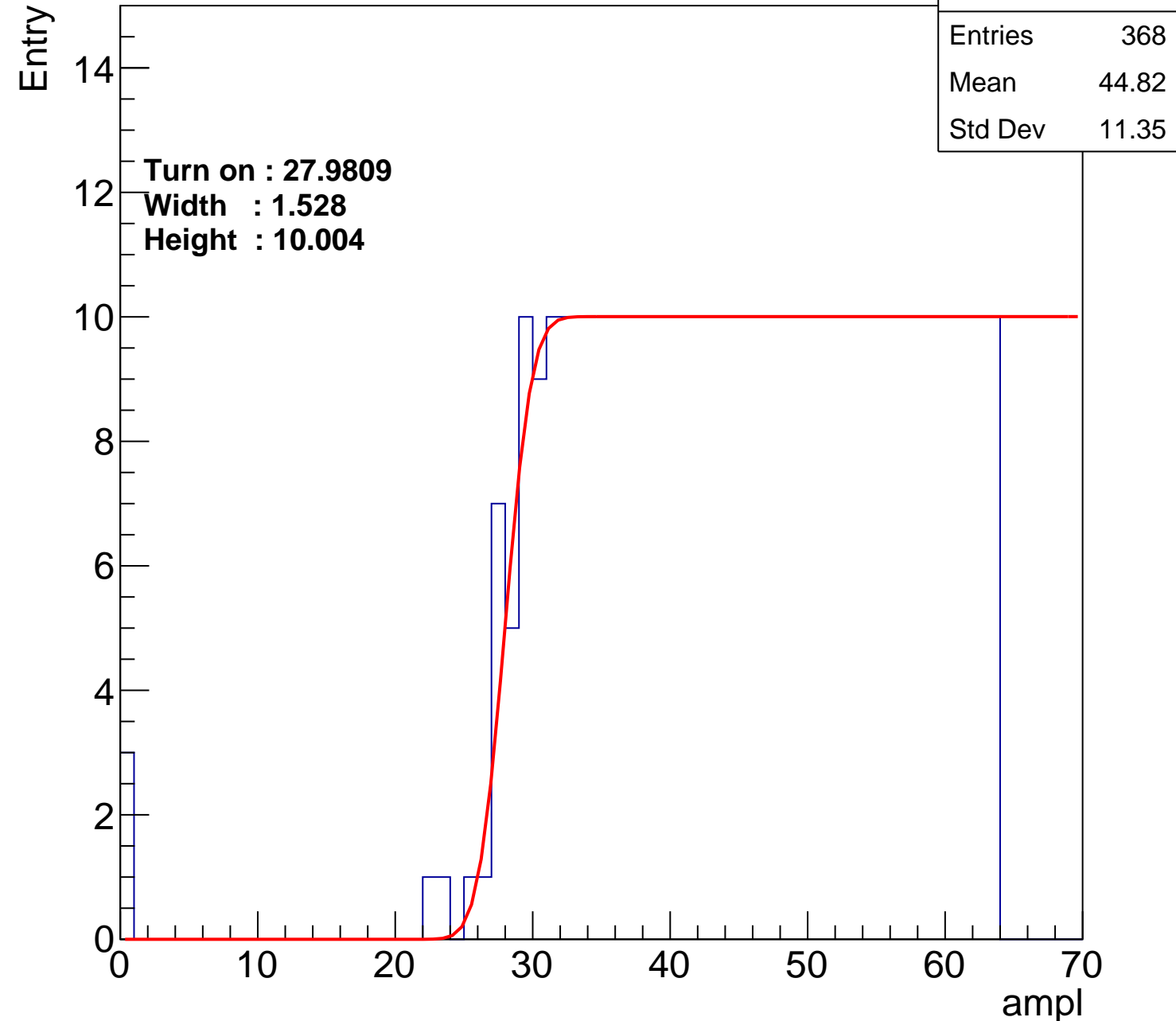
Width : 1.528

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch12

calib_packv5_042523_0143.root, FC#4, port A2

Entries	386
Mean	43.86
Std Dev	11.97

Turn on : 25.7104

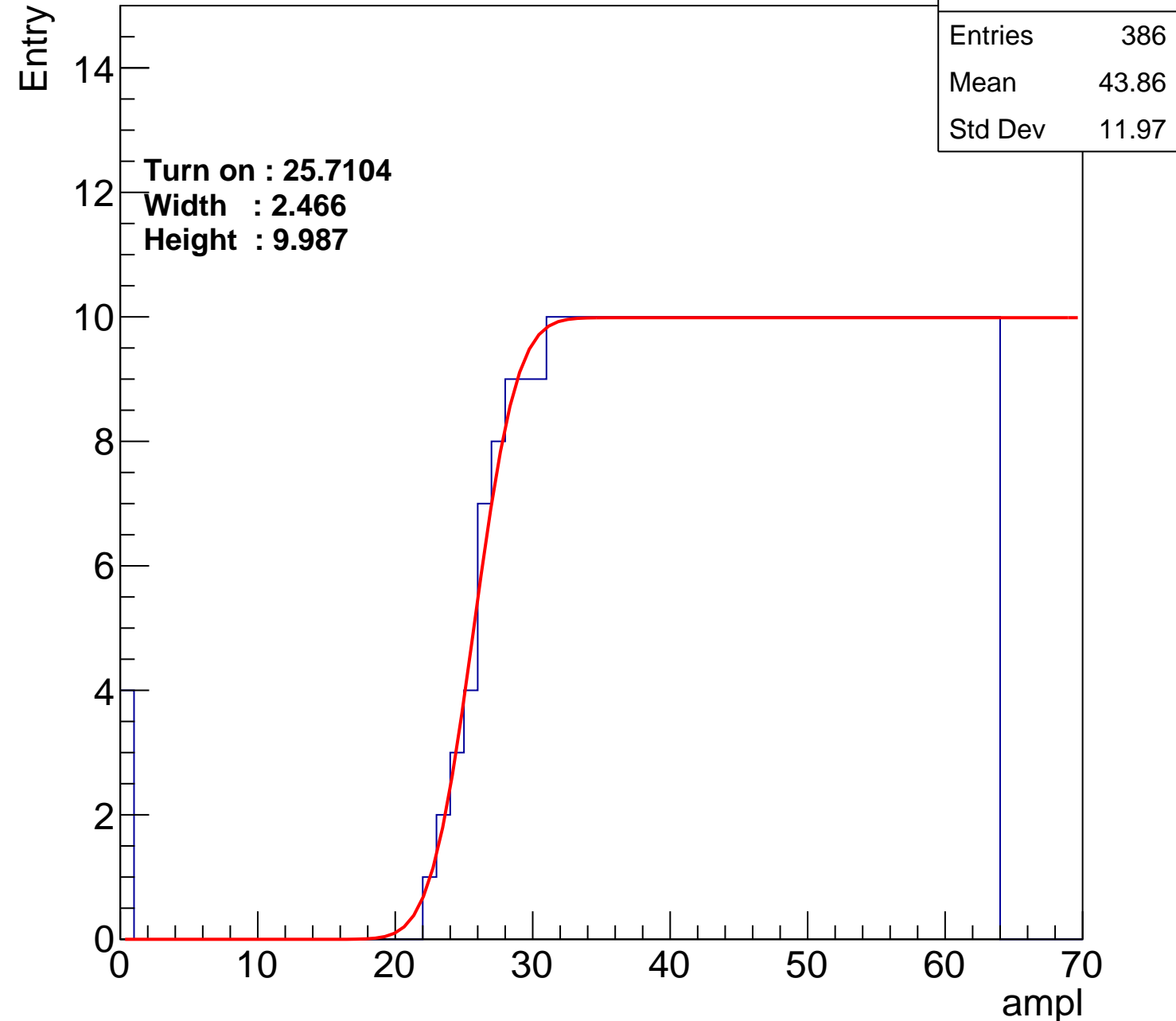
Width : 2.466

Height : 9.987

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch13

calib_packv5_042523_0143.root, FC#4, port A2

Entries	366
Mean	44.92
Std Dev	11.31

Turn on : 28.0093

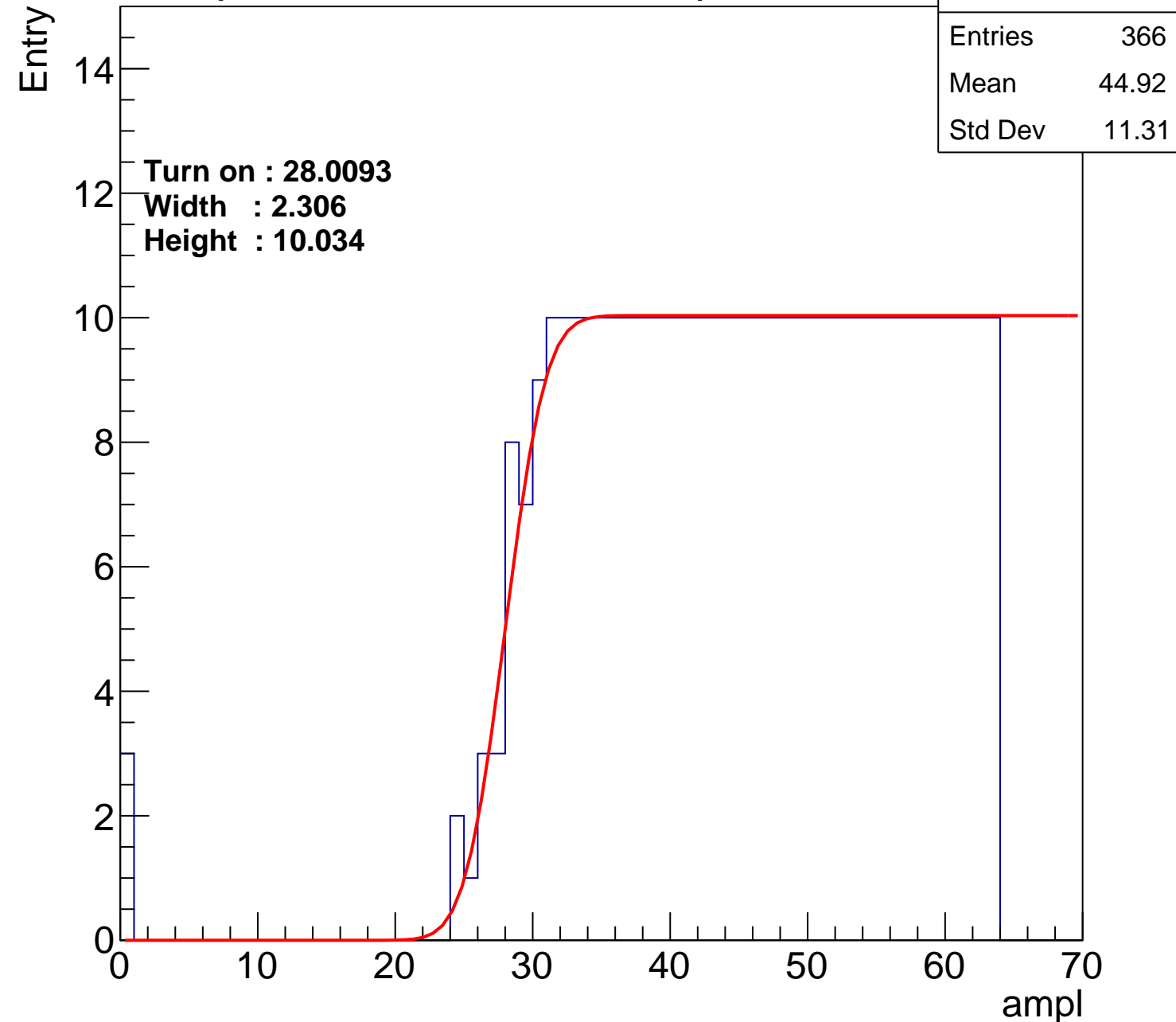
Width : 2.306

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch14

calib_packv5_042523_0143.root, FC#4, port A2

Entries	365
Mean	45.02
Std Dev	11.11

Turn on : 27.6730

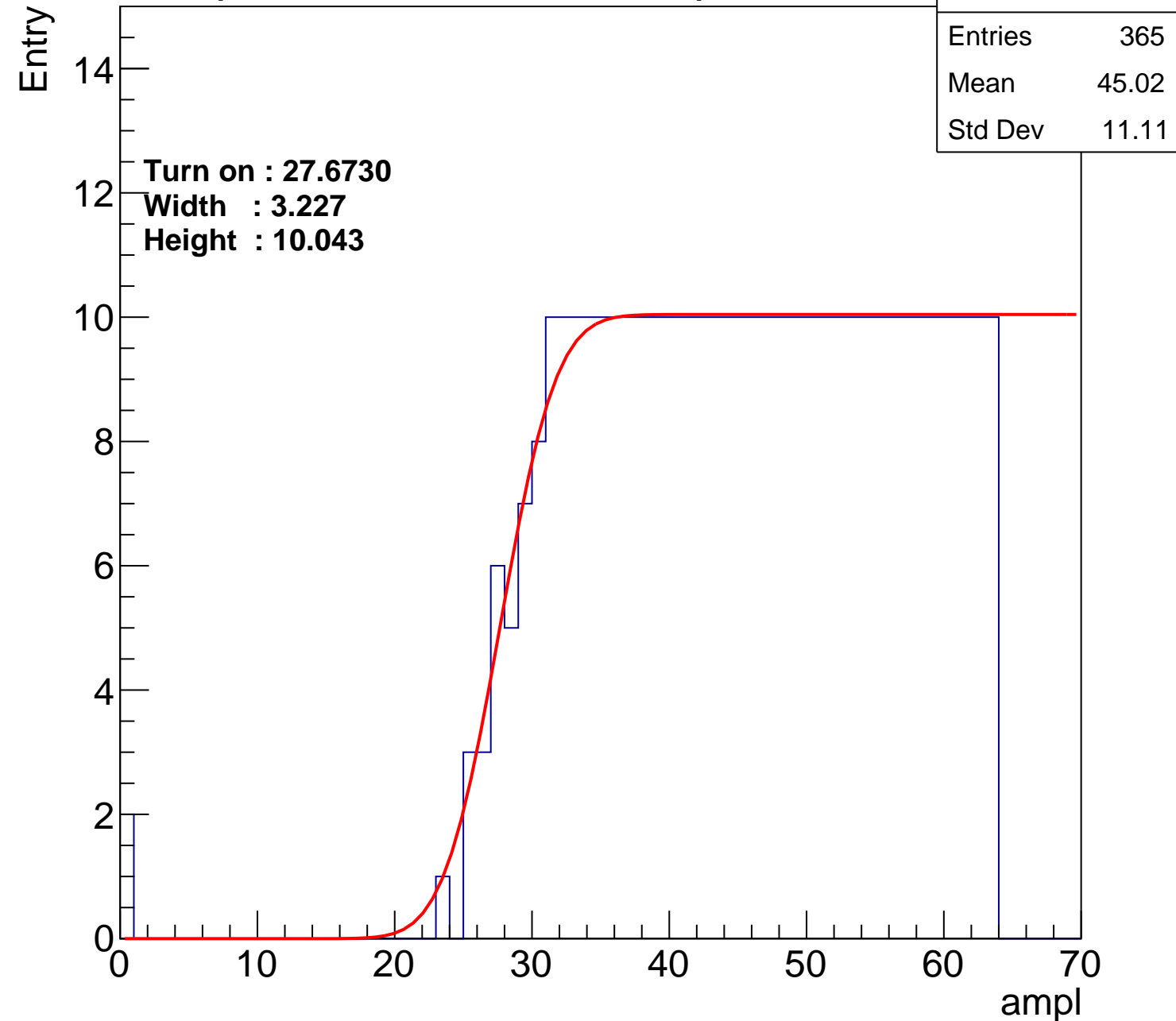
Width : 3.227

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch15

calib_packv5_042523_0143.root, FC#4, port A2

Entries	359
Mean	45.23
Std Dev	11.19

Turn on : 28.6311

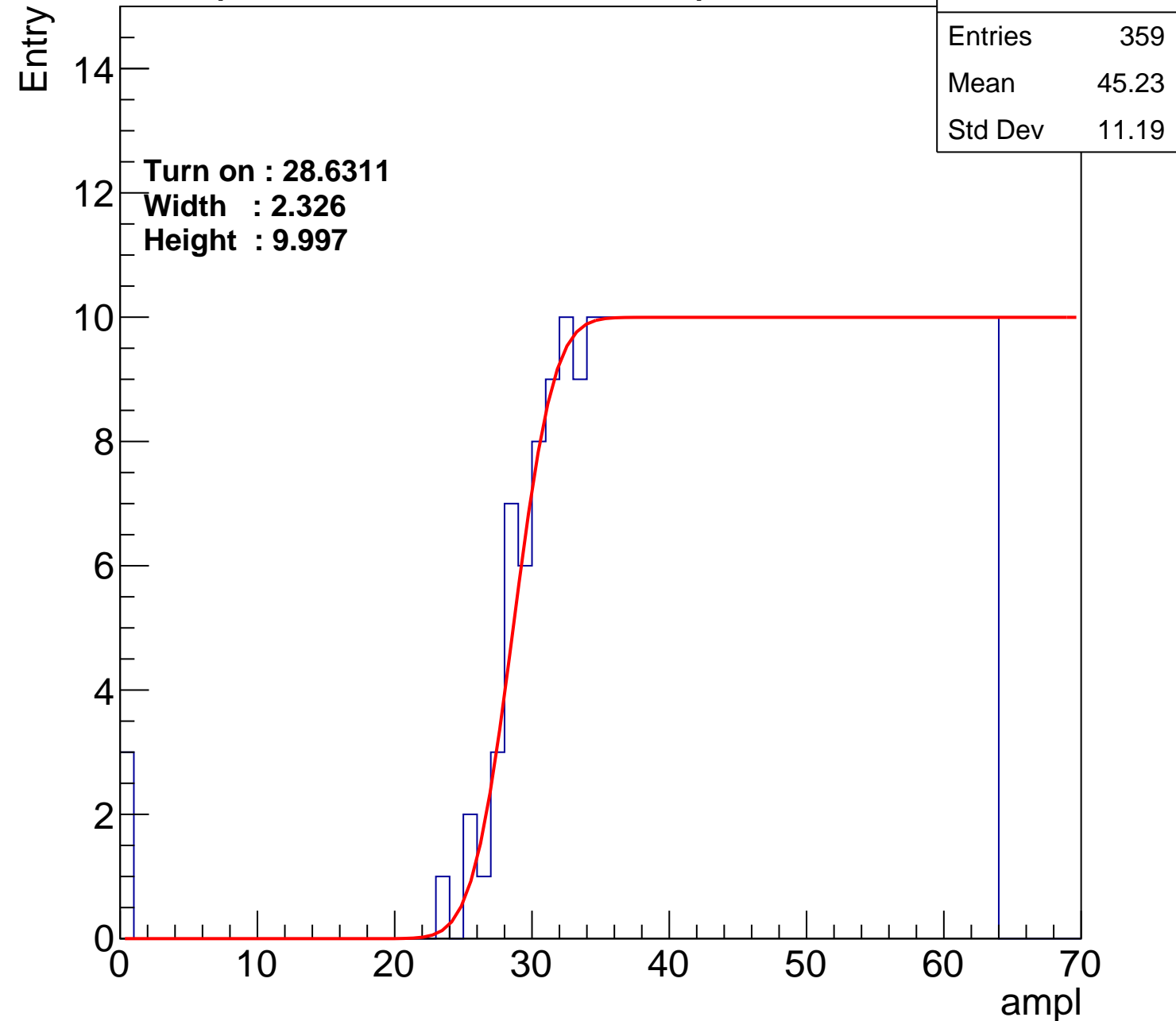
Width : 2.326

Height : 9.997

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch16

calib_packv5_042523_0143.root, FC#4, port A2

Entries	365
Mean	44.98
Std Dev	11.17

Turn on : 28.2290

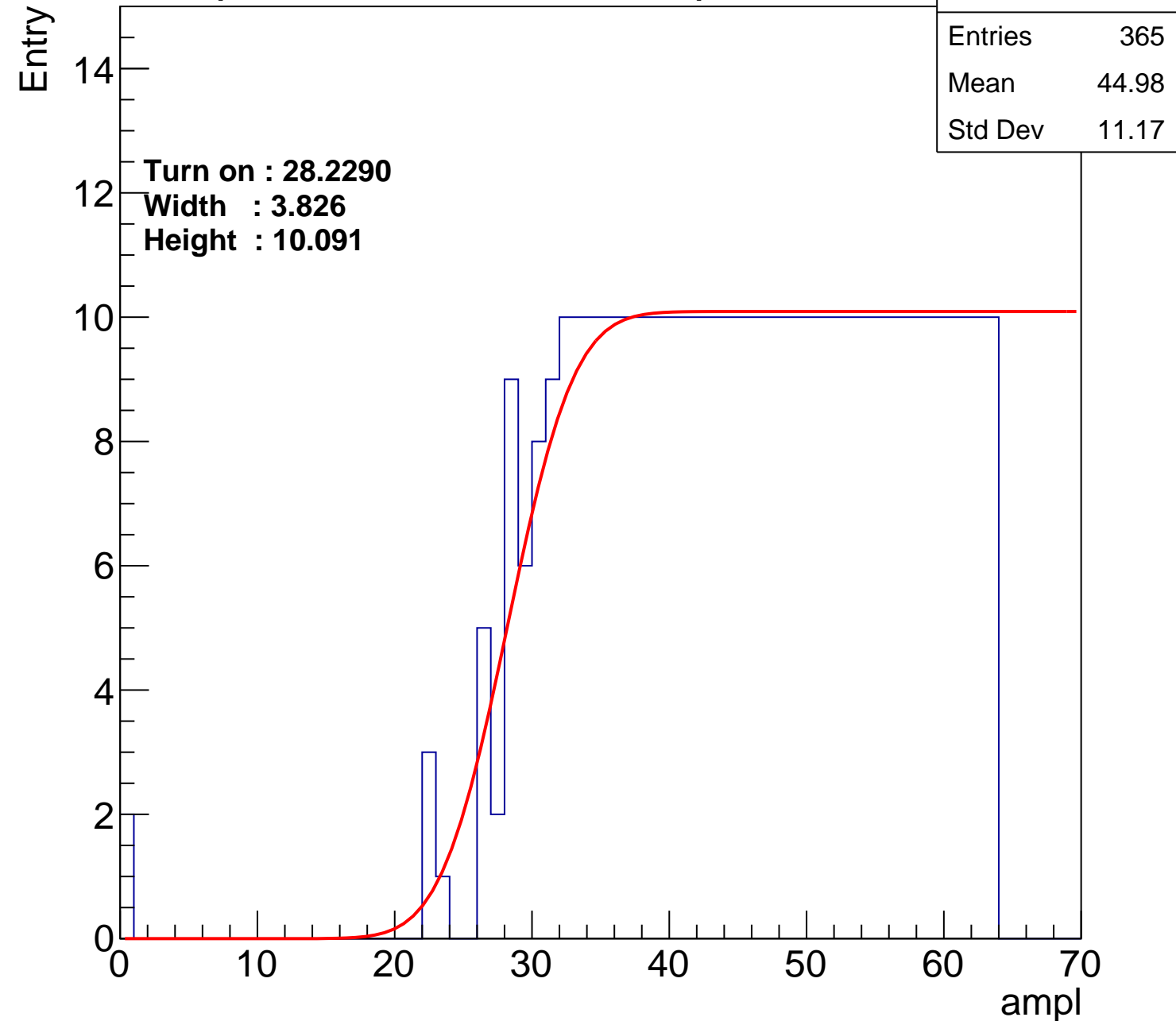
Width : 3.826

Height : 10.091

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch17

calib_packv5_042523_0143.root, FC#4, port A2

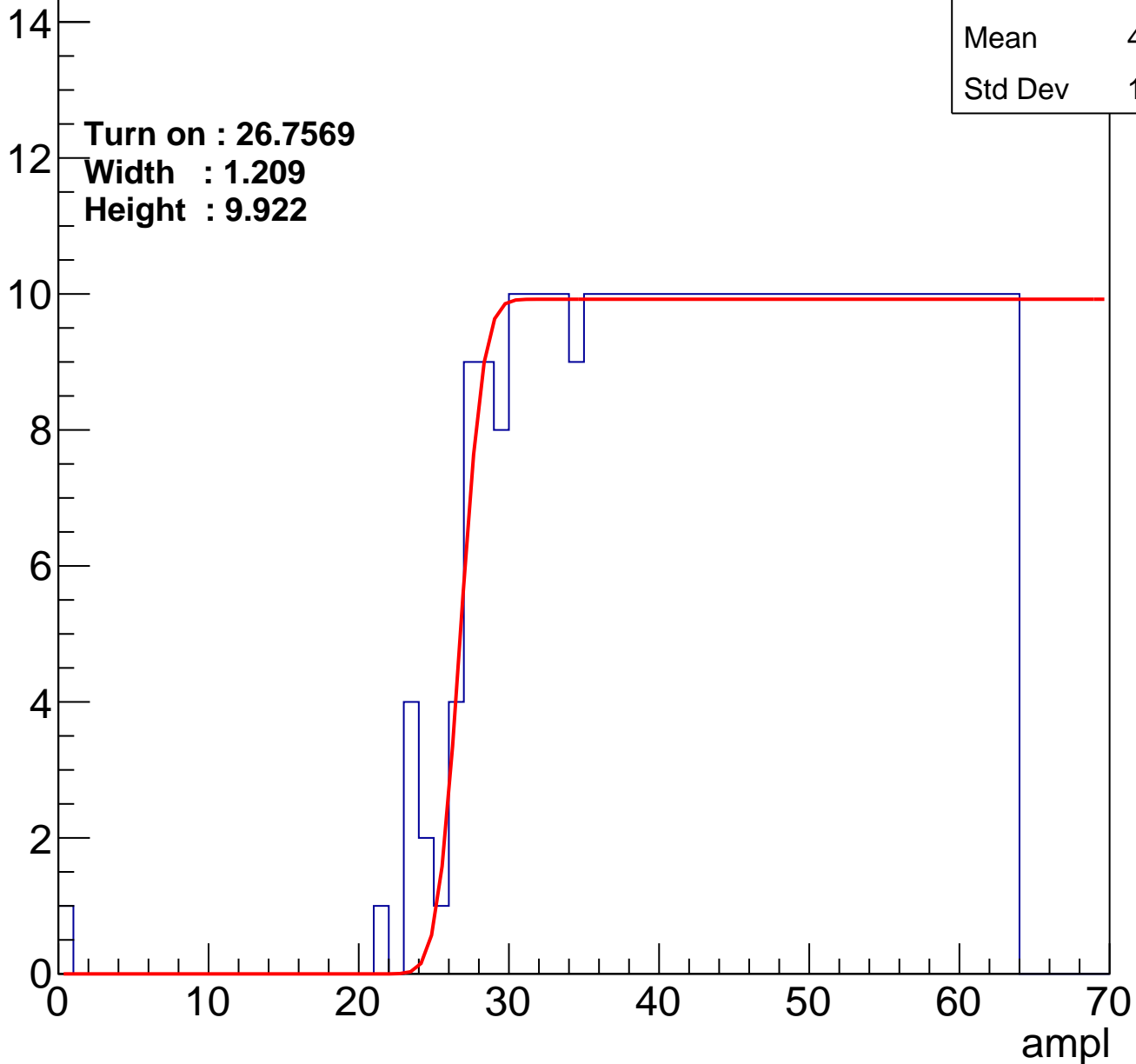
Entries	378
Mean	44.43
Std Dev	11.28

Turn on : 26.7569

Width : 1.209

Height : 9.922

Entry



B1L100S, U8-ch18

calib_packv5_042523_0143.root, FC#4, port A2

Entries	364
Mean	45.13
Std Dev	10.88

Turn on : 27.8127

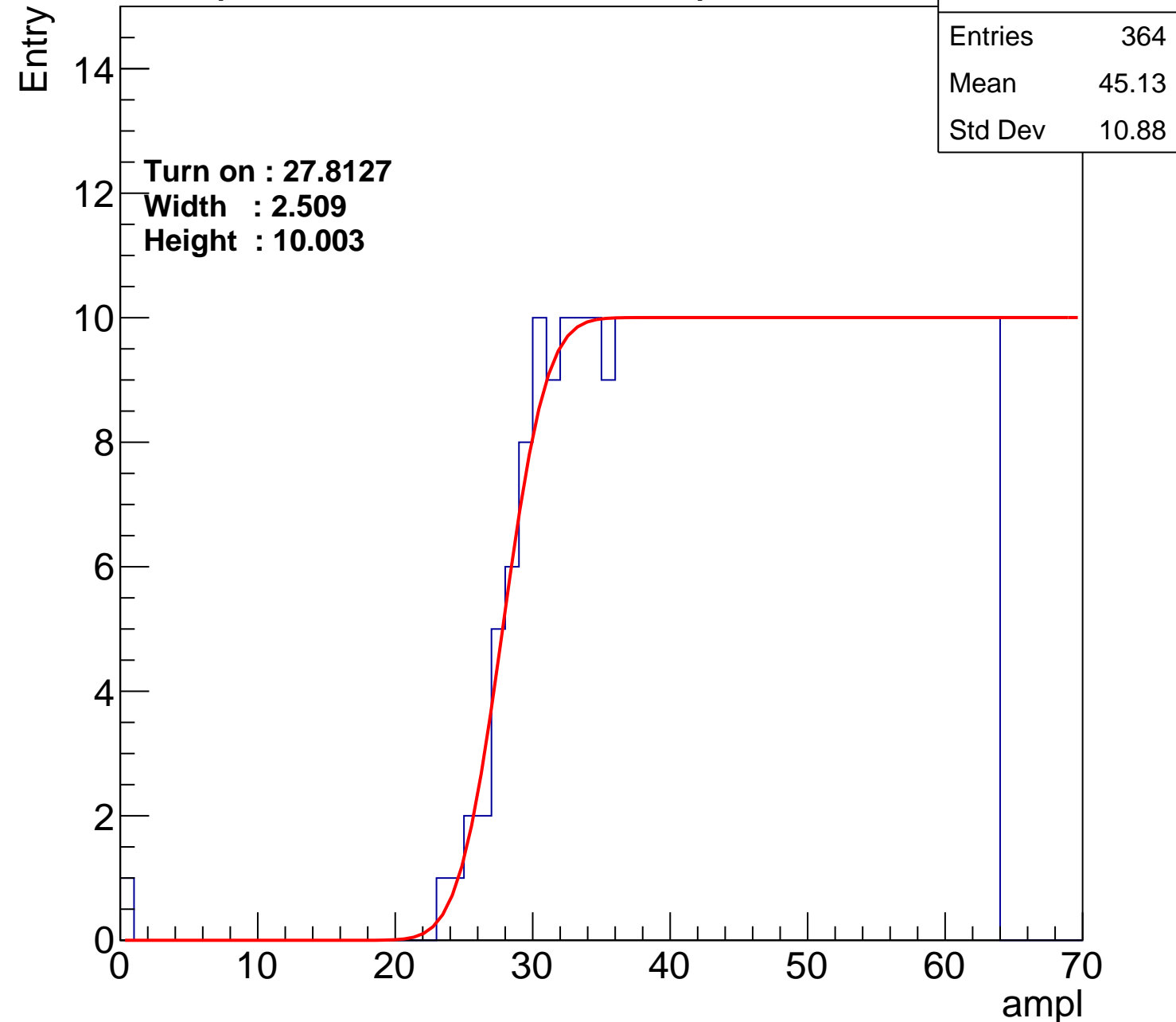
Width : 2.509

Height : 10.003

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch19

calib_packv5_042523_0143.root, FC#4, port A2

Entries	367
Mean	44.92
Std Dev	11.15

Turn on : 27.4740

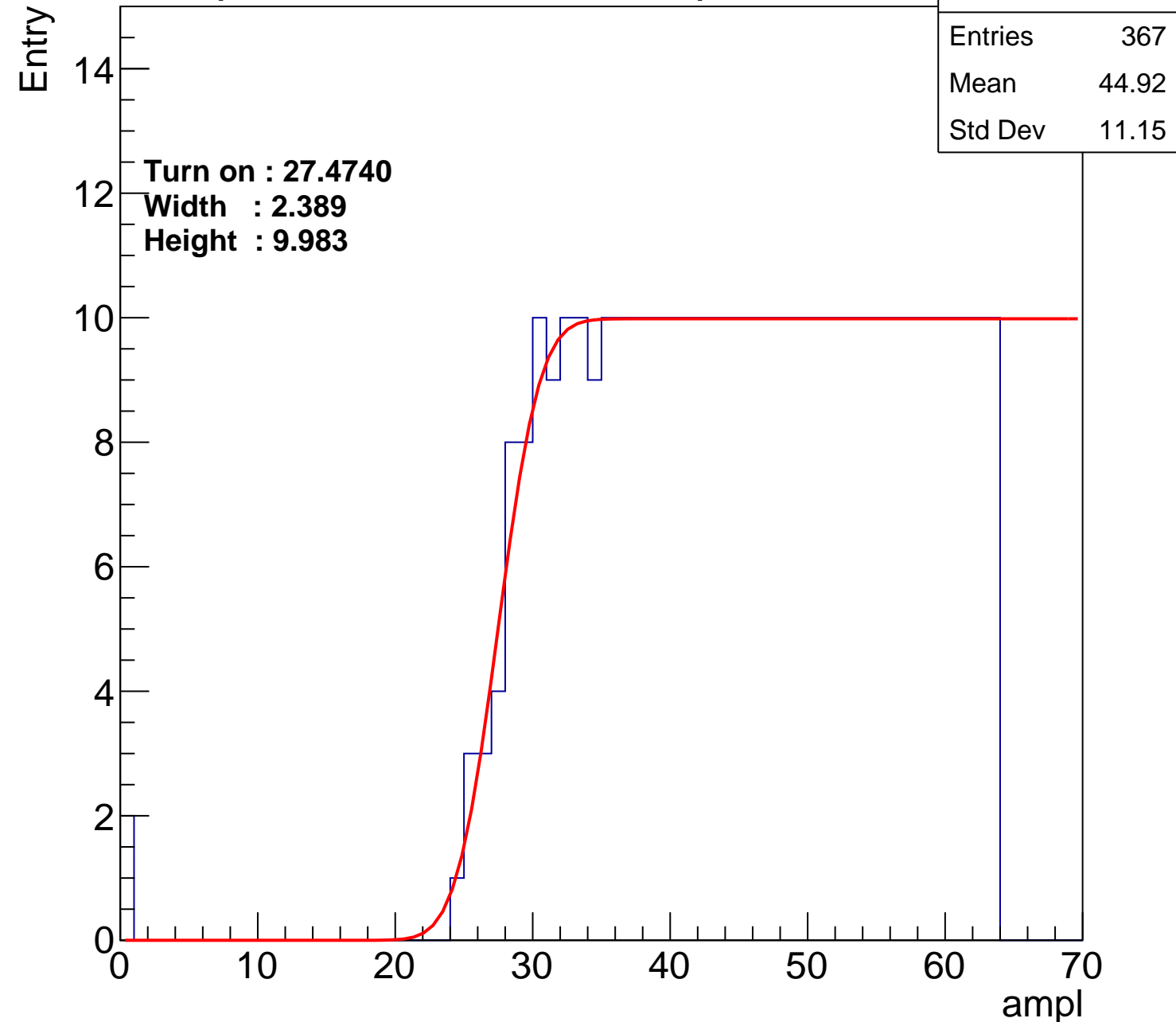
Width : 2.389

Height : 9.983

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch20

calib_packv5_042523_0143.root, FC#4, port A2

Entries	384
Mean	43.88
Std Dev	12.11

Turn on : 25.6866

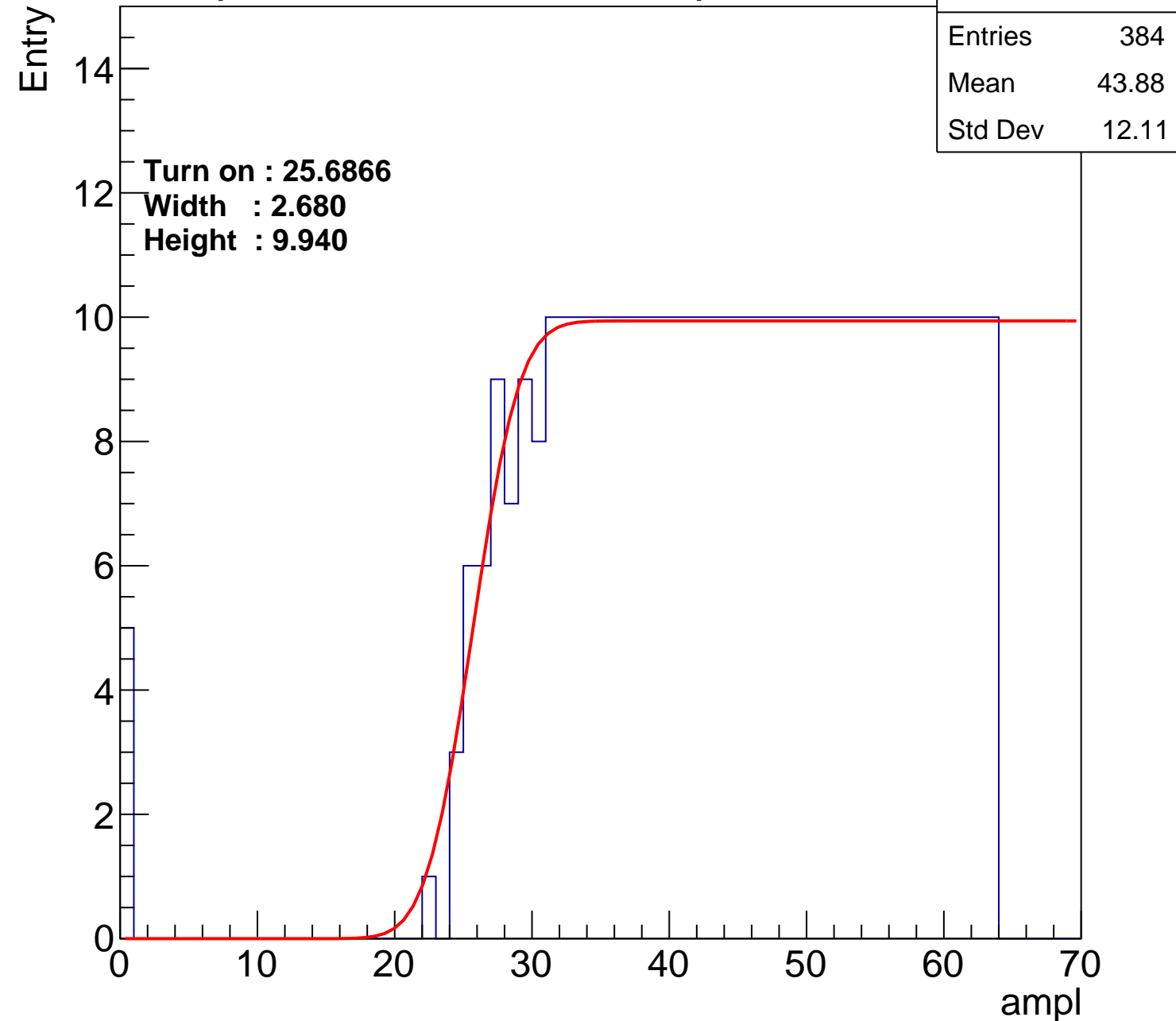
Width : 2.680

Height : 9.940

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch21

calib_packv5_042523_0143.root, FC#4, port A2

Entries	386
Mean	44.04
Std Dev	11.47

Turn on : 25.7075

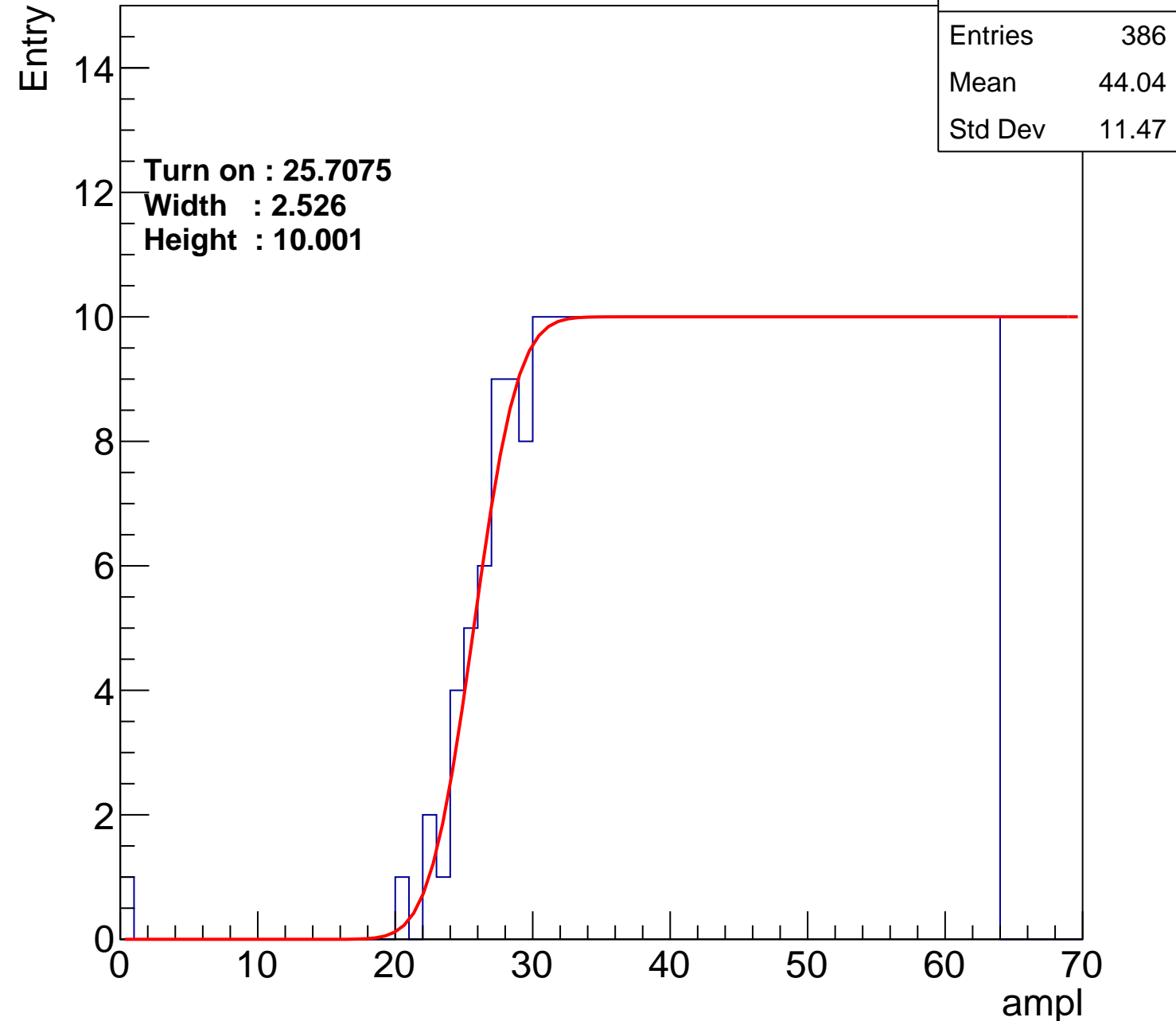
Width : 2.526

Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch22

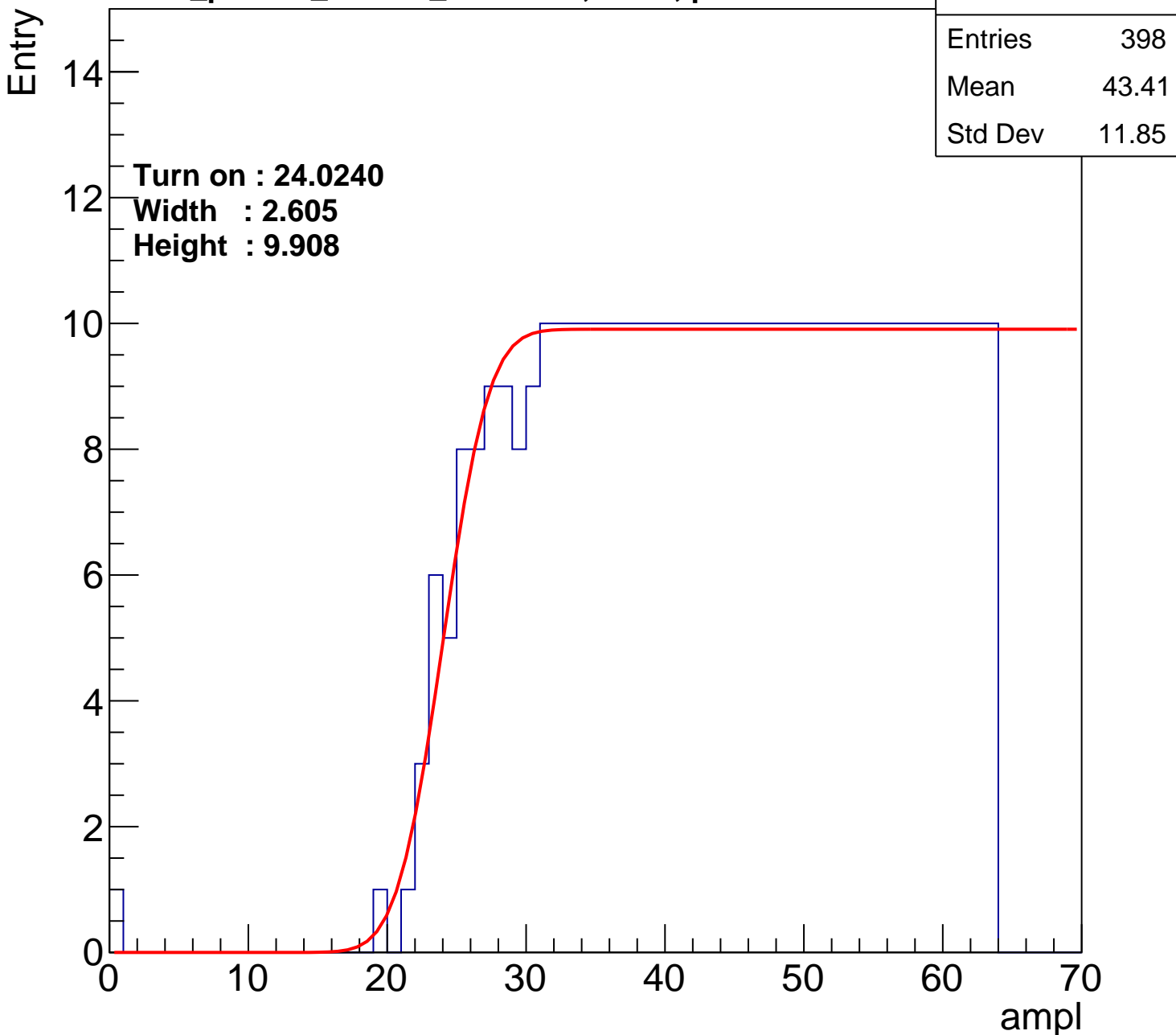
calib_packv5_042523_0143.root, FC#4, port A2

Turn on : 24.0240

Width : 2.605

Height : 9.908

Entries	398
Mean	43.41
Std Dev	11.85



B1L100S, U8-ch23

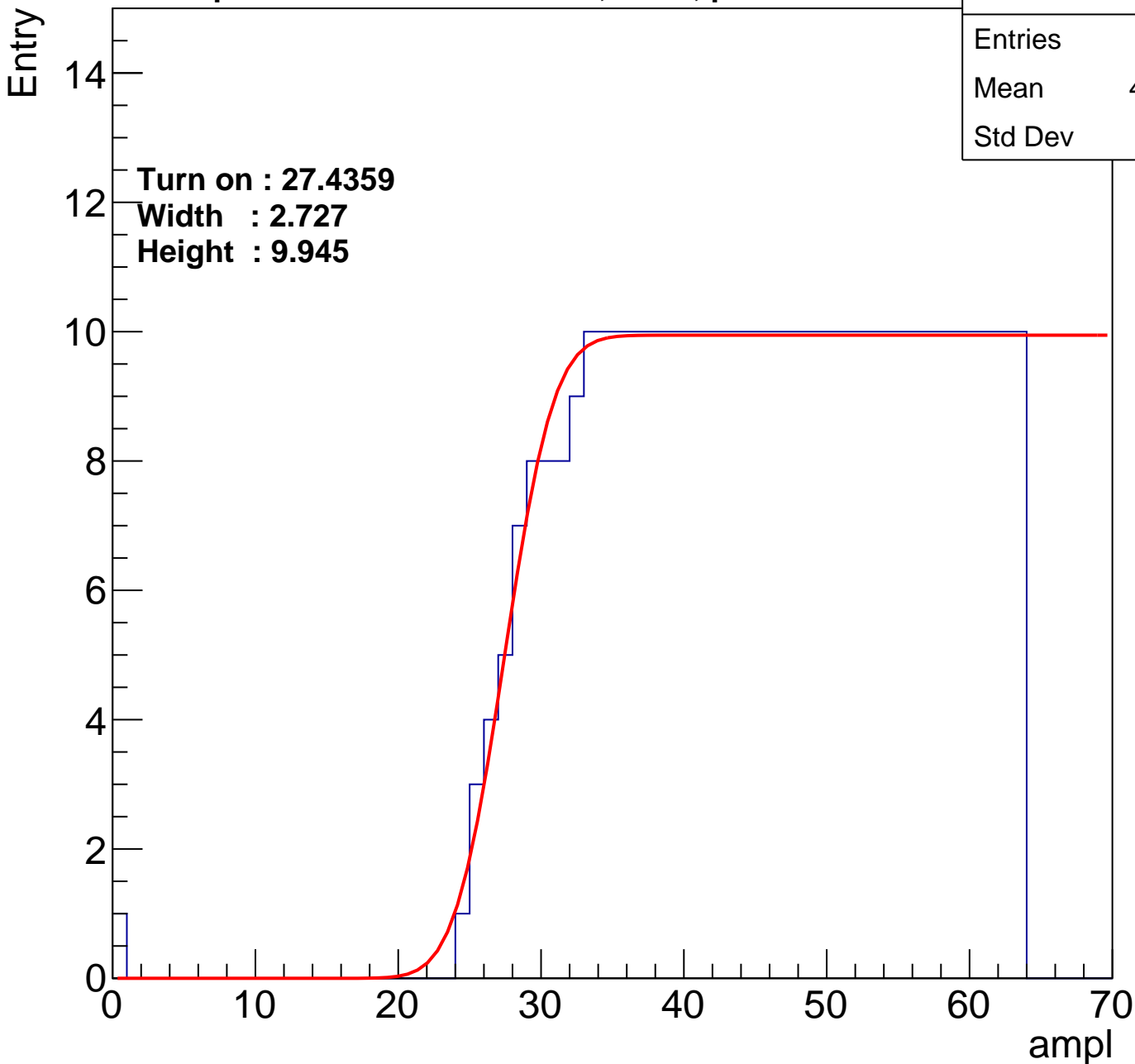
calib_packv5_042523_0143.root, FC#4, port A2

Entries	364
Mean	45.12
Std Dev	10.9

Turn on : 27.4359

Width : 2.727

Height : 9.945



B1L100S, U8-ch24

calib_packv5_042523_0143.root, FC#4, port A2

Entries	361
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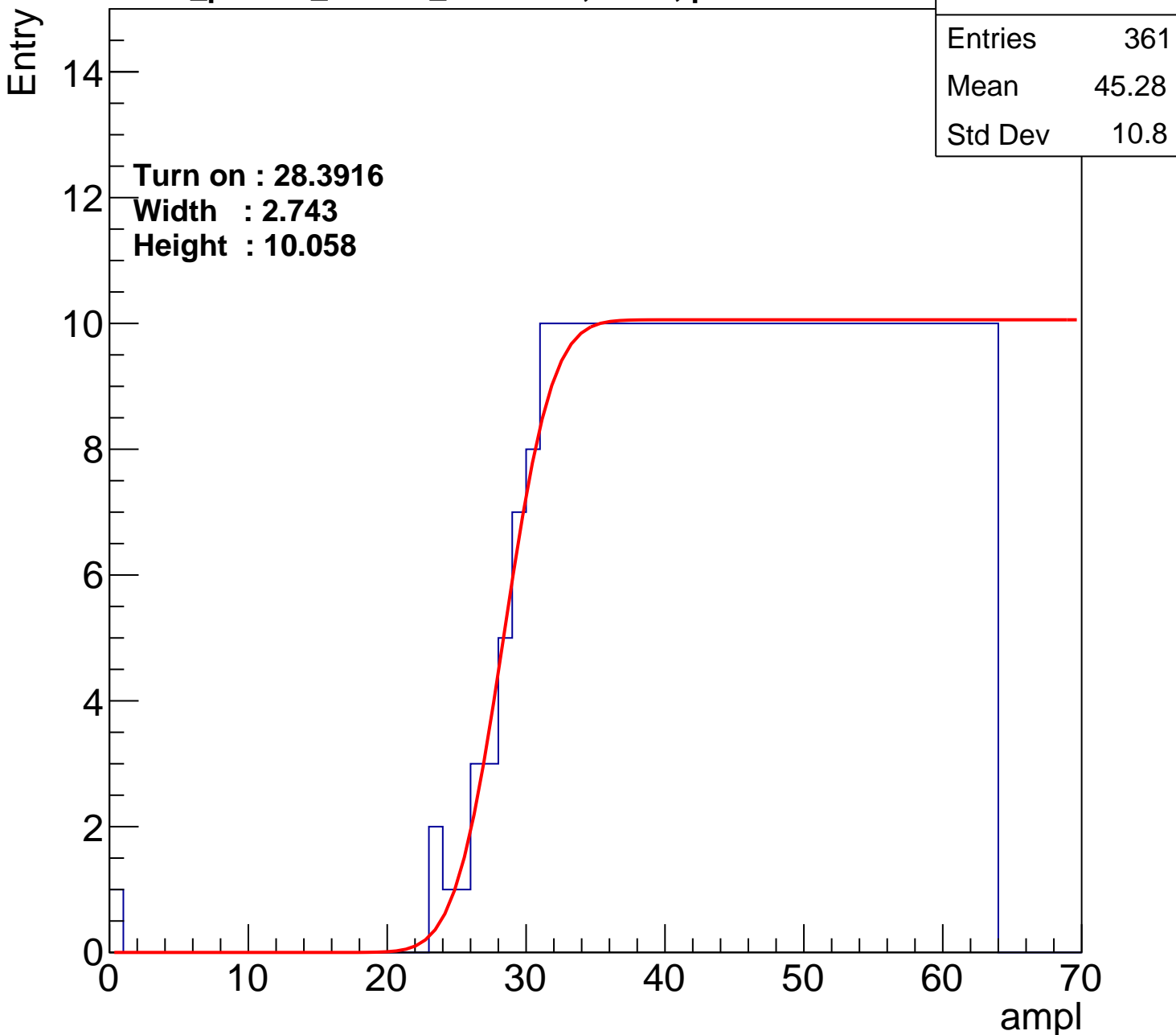
Mean	45.28
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Std Dev	10.8
---------	------

Turn on : 28.3916

Width : 2.743

Height : 10.058



B1L100S, U8-ch25

calib_packv5_042523_0143.root, FC#4, port A2

Entries	394
Mean	43.51
Std Dev	12.04

Turn on : 25.0457

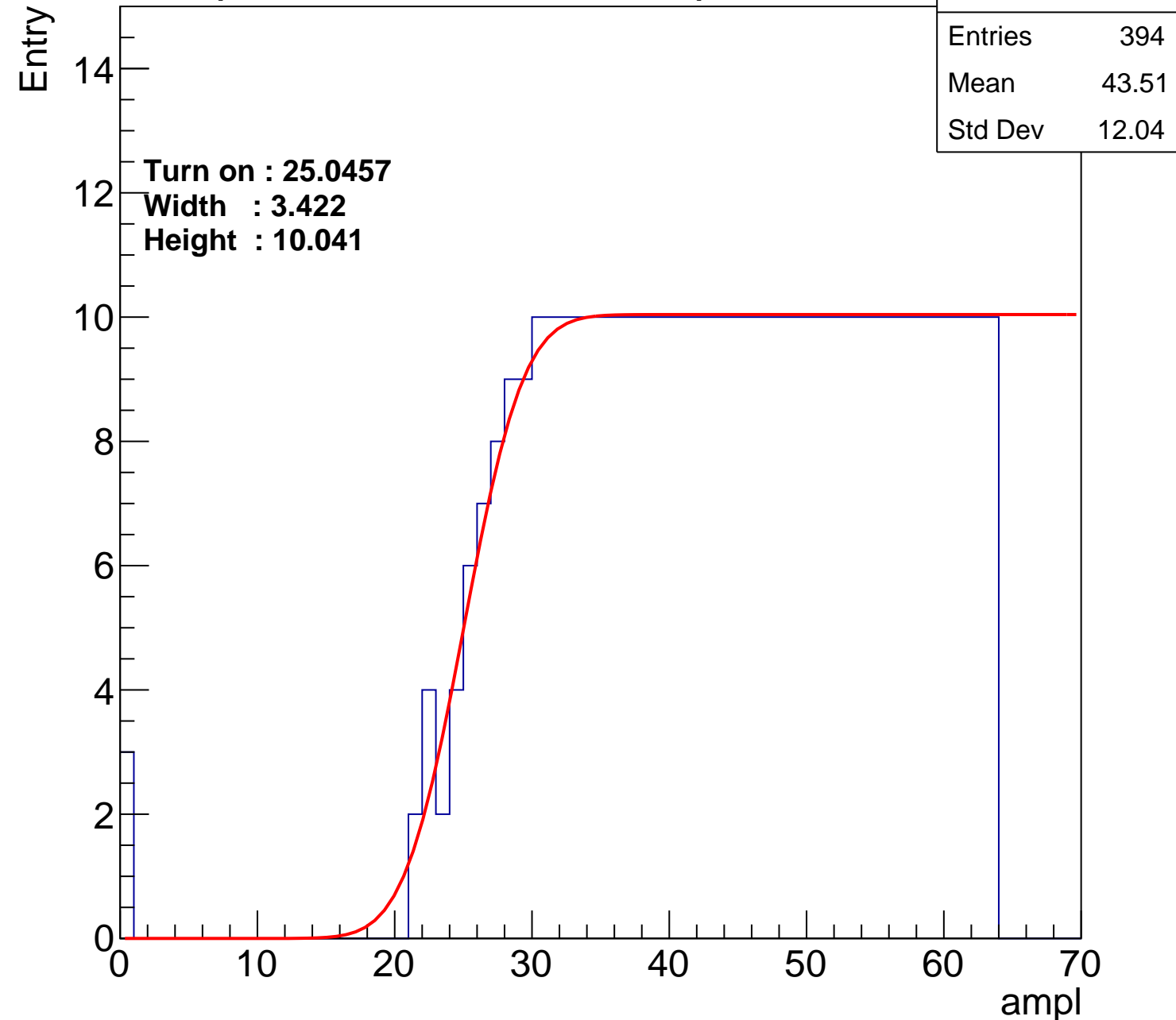
Width : 3.422

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch26

calib_packv5_042523_0143.root, FC#4, port A2

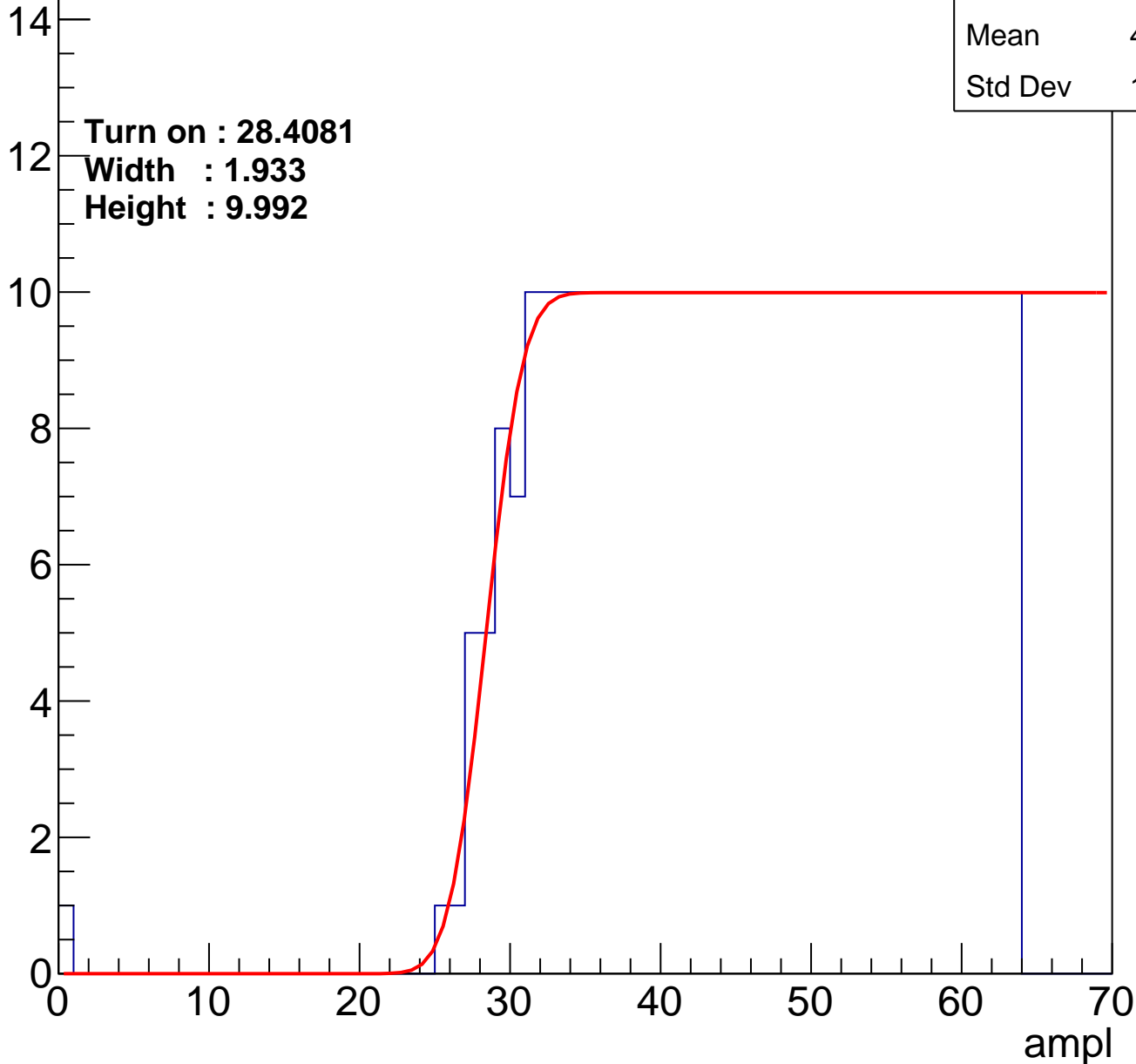
Entry

Entries	358
Mean	45.47
Std Dev	10.65

Turn on : 28.4081

Width : 1.933

Height : 9.992



B1L100S, U8-ch27

calib_packv5_042523_0143.root, FC#4, port A2

Entries	380
Mean	44.27
Std Dev	11.5

Turn on : 26.1499

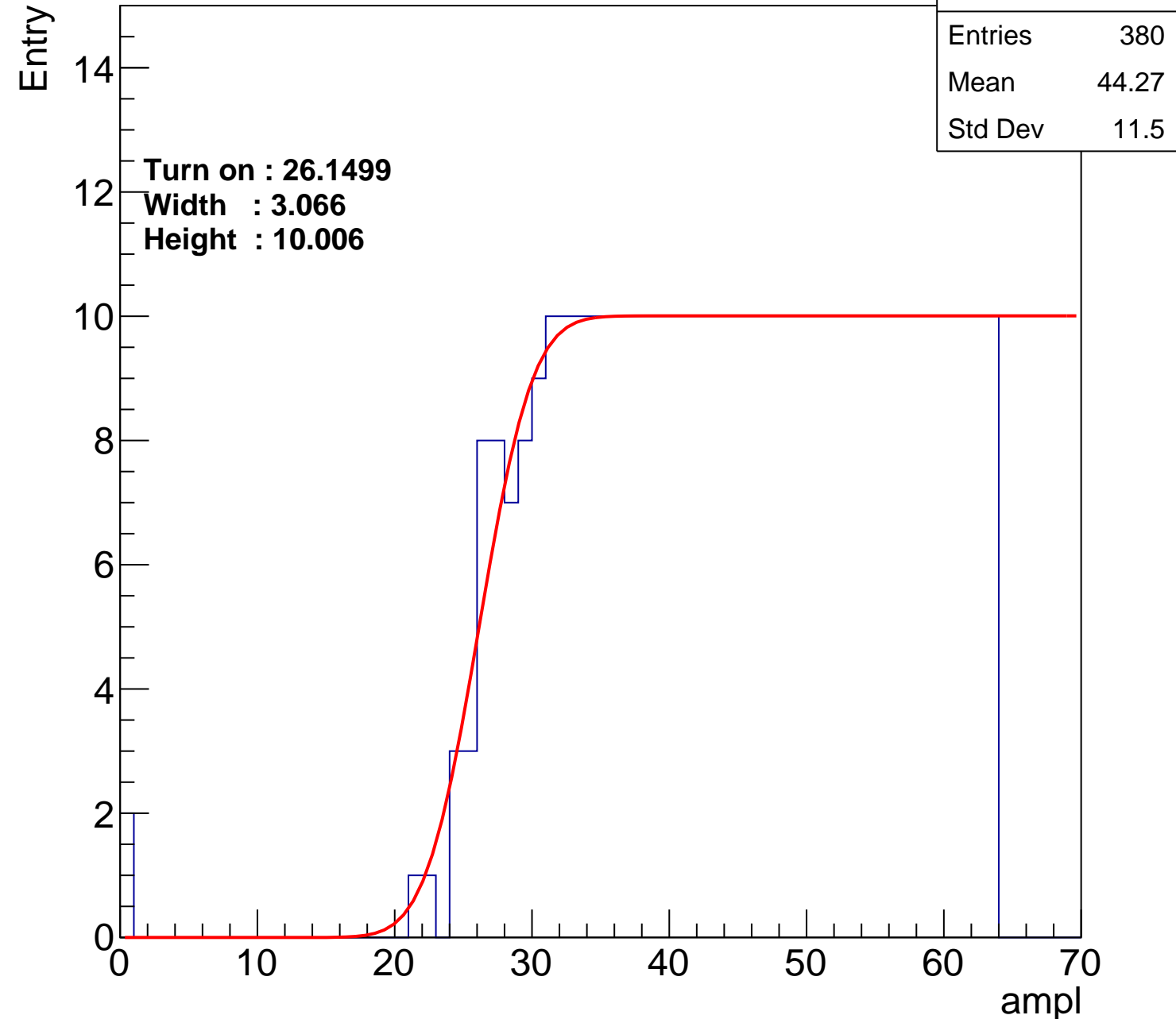
Width : 3.066

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch28

calib_packv5_042523_0143.root, FC#4, port A2

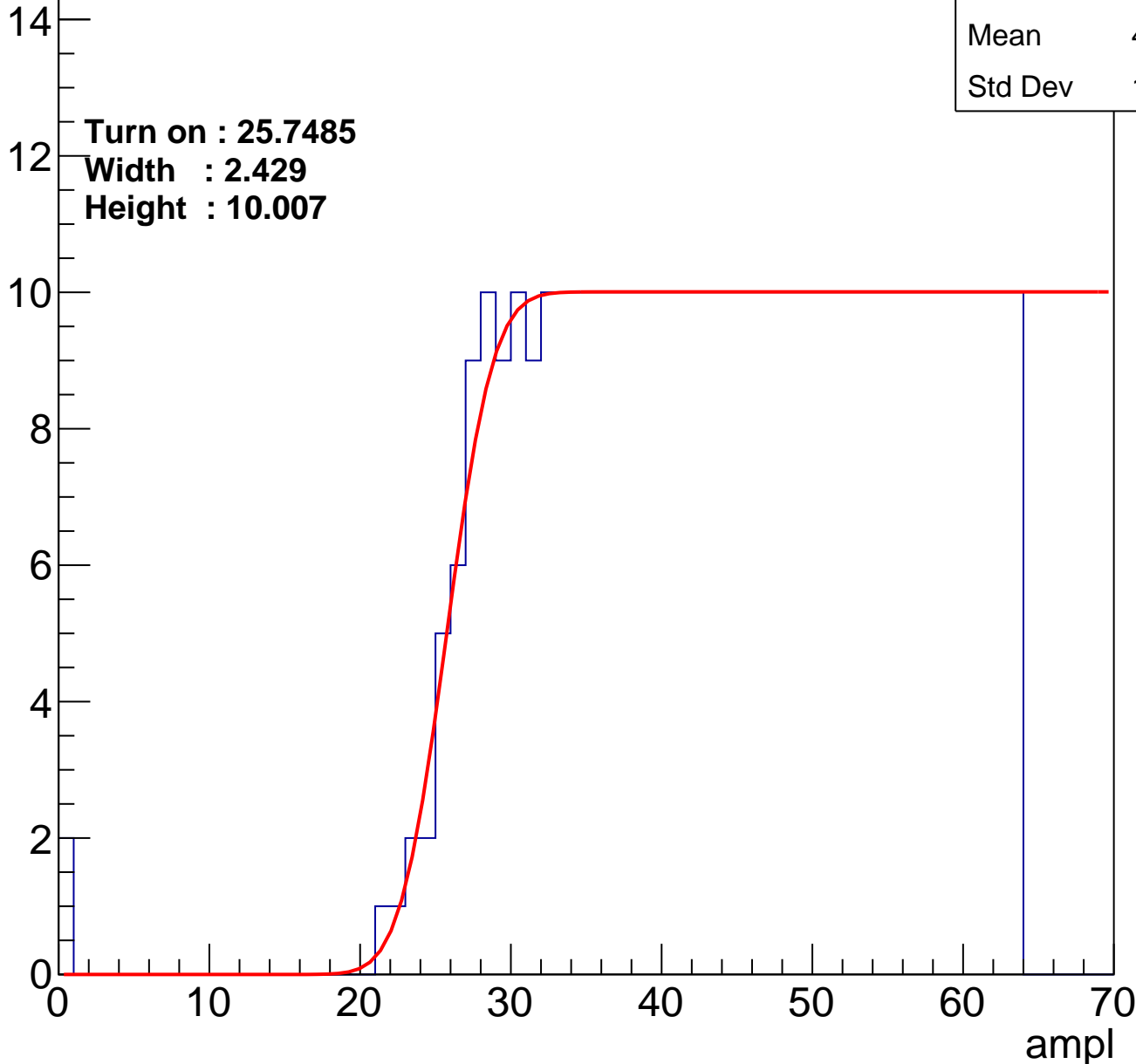
Entries	386
Mean	43.99
Std Dev	11.63

Turn on : 25.7485

Width : 2.429

Height : 10.007

Entry



B1L100S, U8-ch29

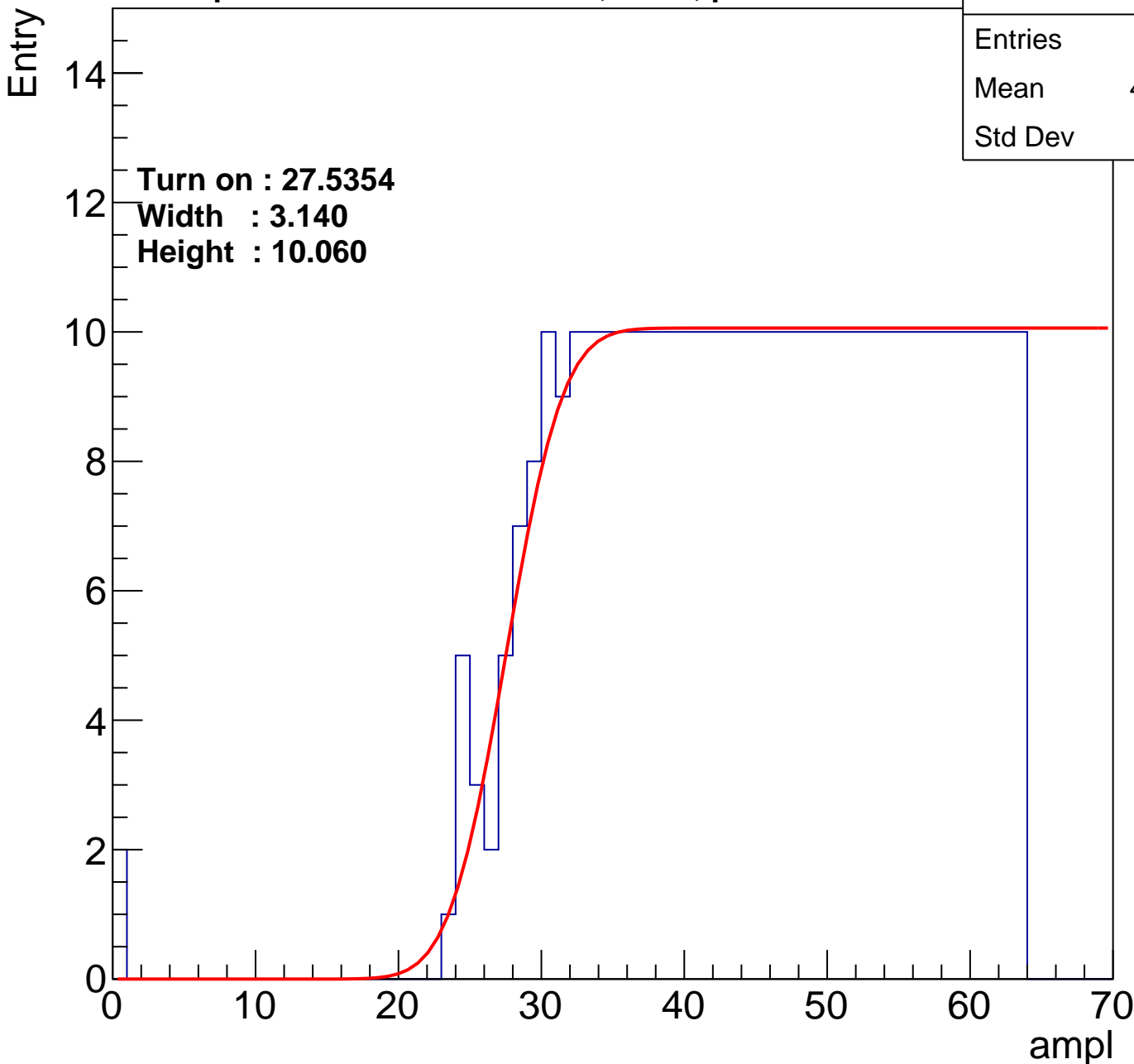
calib_packv5_042523_0143.root, FC#4, port A2

Entries	372
Mean	44.66
Std Dev	11.31

Turn on : 27.5354

Width : 3.140

Height : 10.060



B1L100S, U8-ch30

calib_packv5_042523_0143.root, FC#4, port A2

Entries	377
Mean	44.29
Std Dev	11.71

Turn on : 26.6449

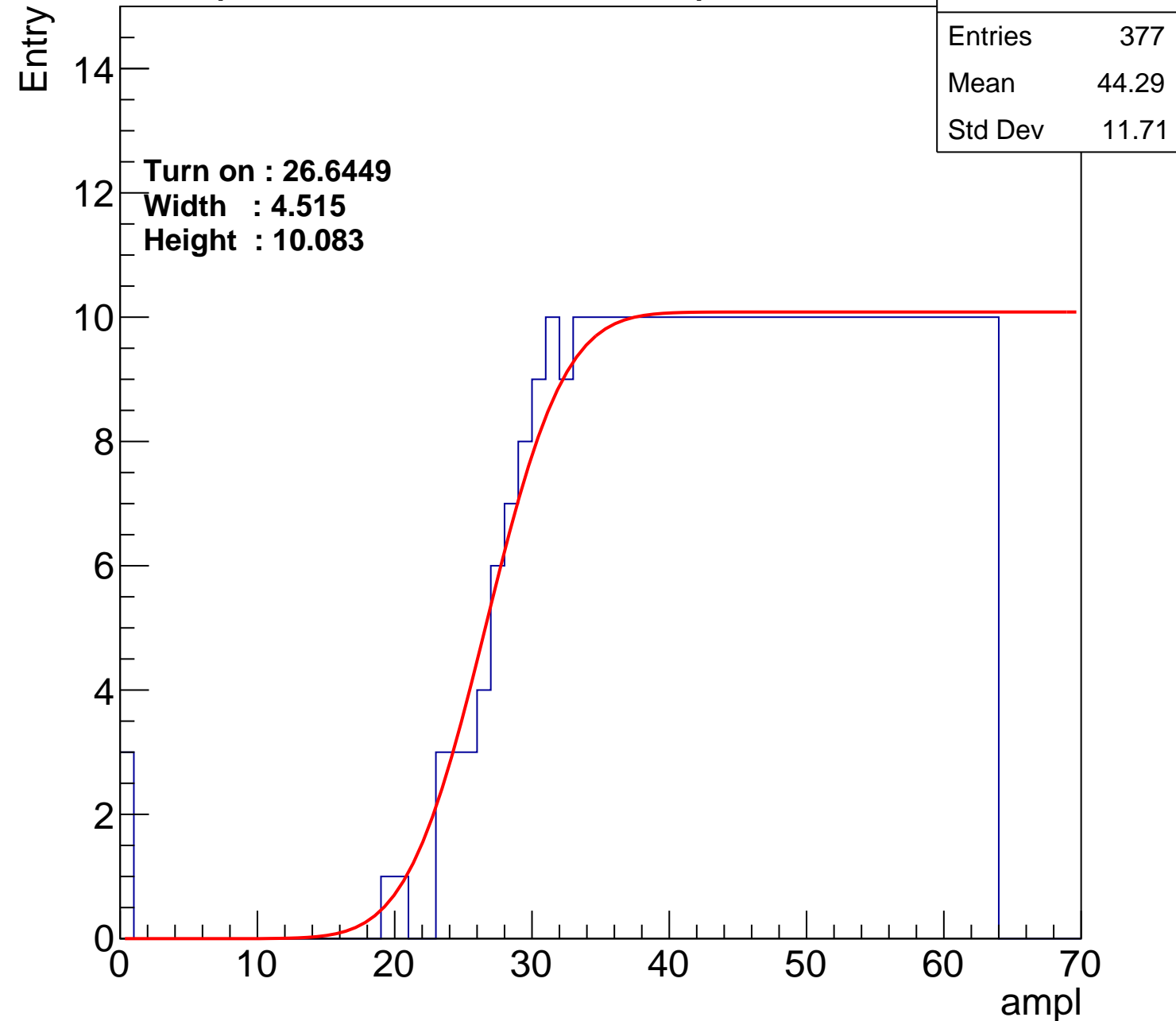
Width : 4.515

Height : 10.083

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch31

calib_packv5_042523_0143.root, FC#4, port A2

Entries	380
Mean	44.28
Std Dev	11.49

Turn on : 25.9716

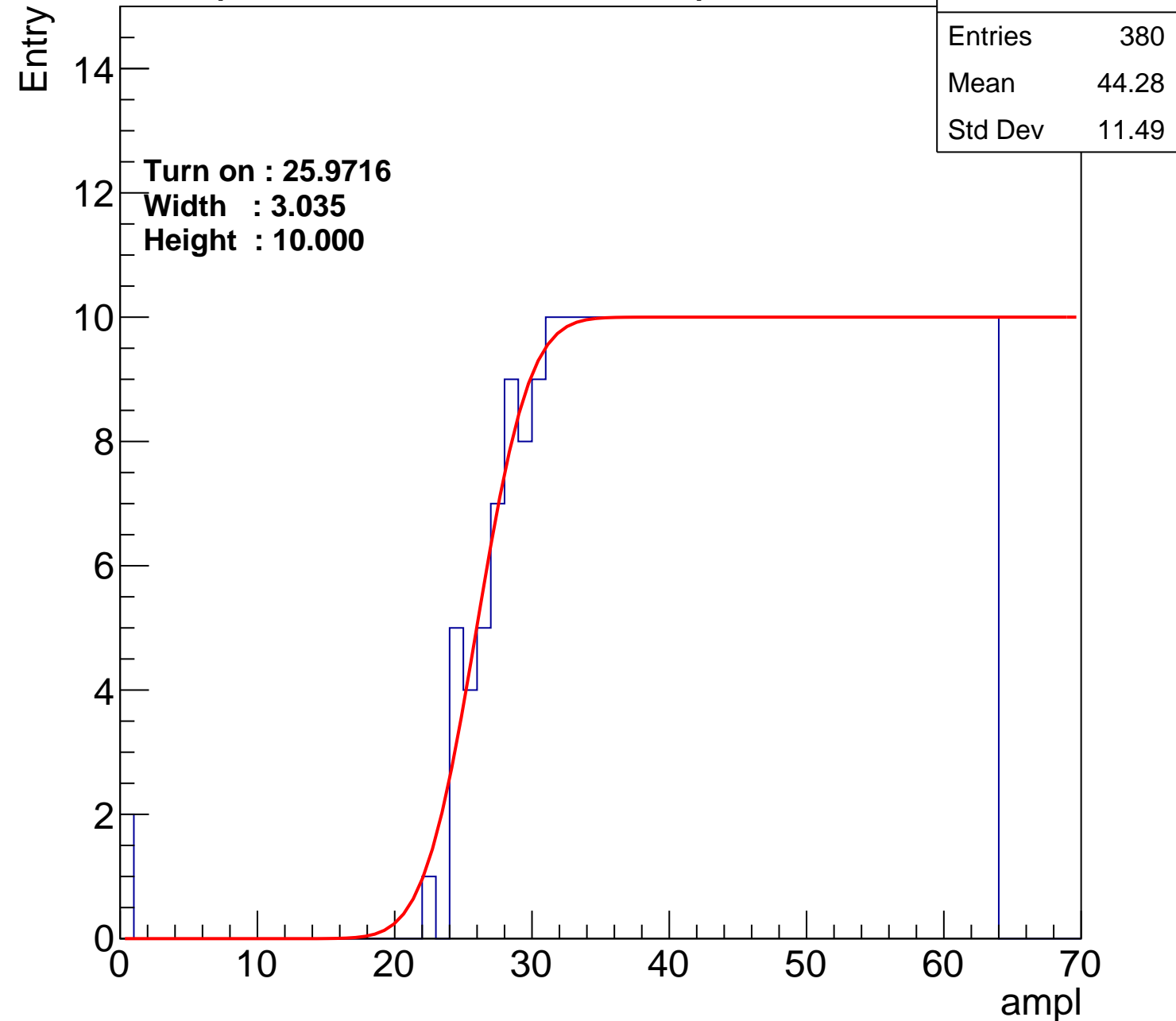
Width : 3.035

Height : 10.000

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch32

calib_packv5_042523_0143.root, FC#4, port A2

Entries	397
Mean	43.5
Std Dev	11.84

Turn on : 24.4858

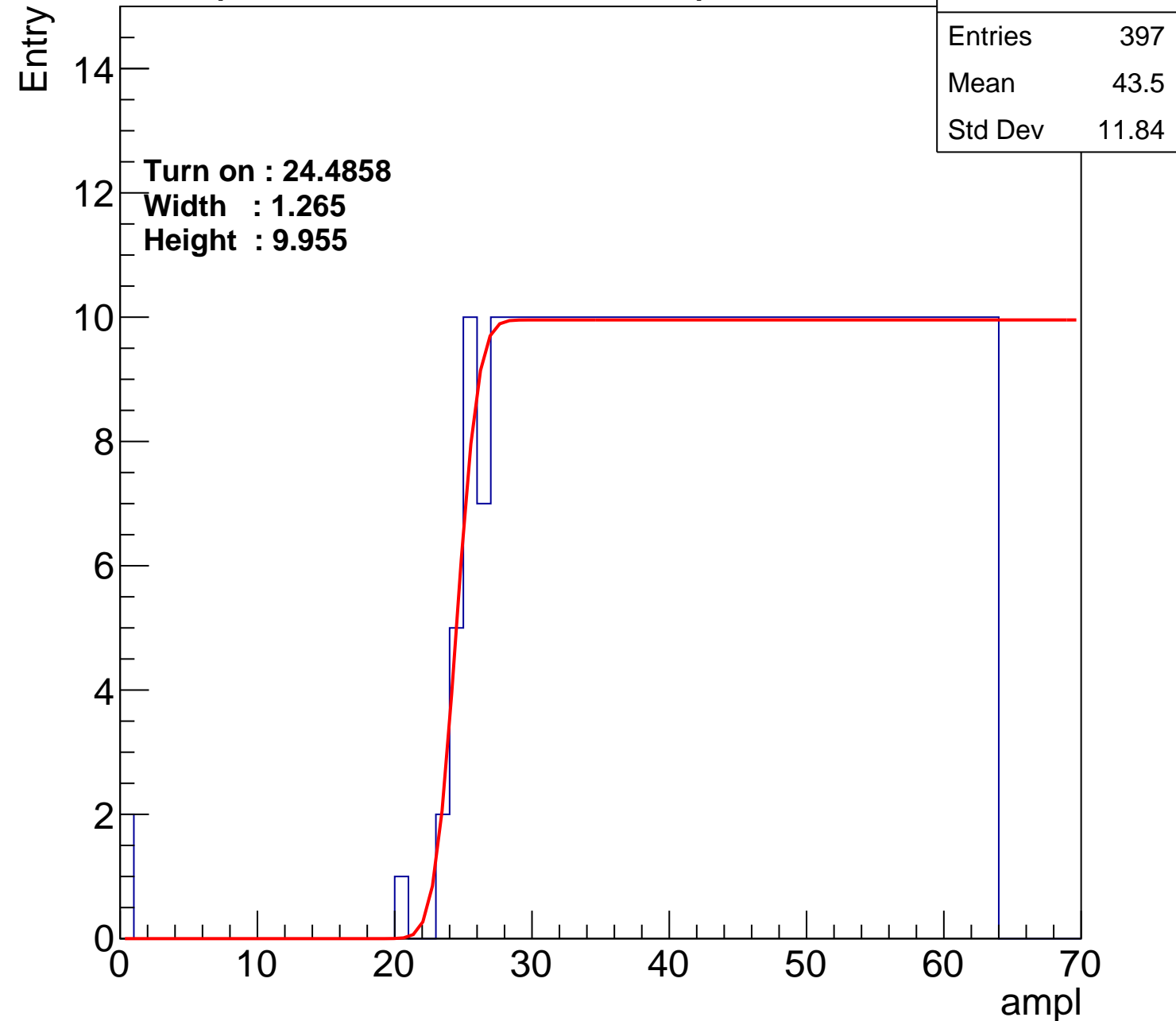
Width : 1.265

Height : 9.955

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch33

calib_packv5_042523_0143.root, FC#4, port A2

Entries	358
Mean	45.43
Std Dev	10.72

Turn on : 28.2272

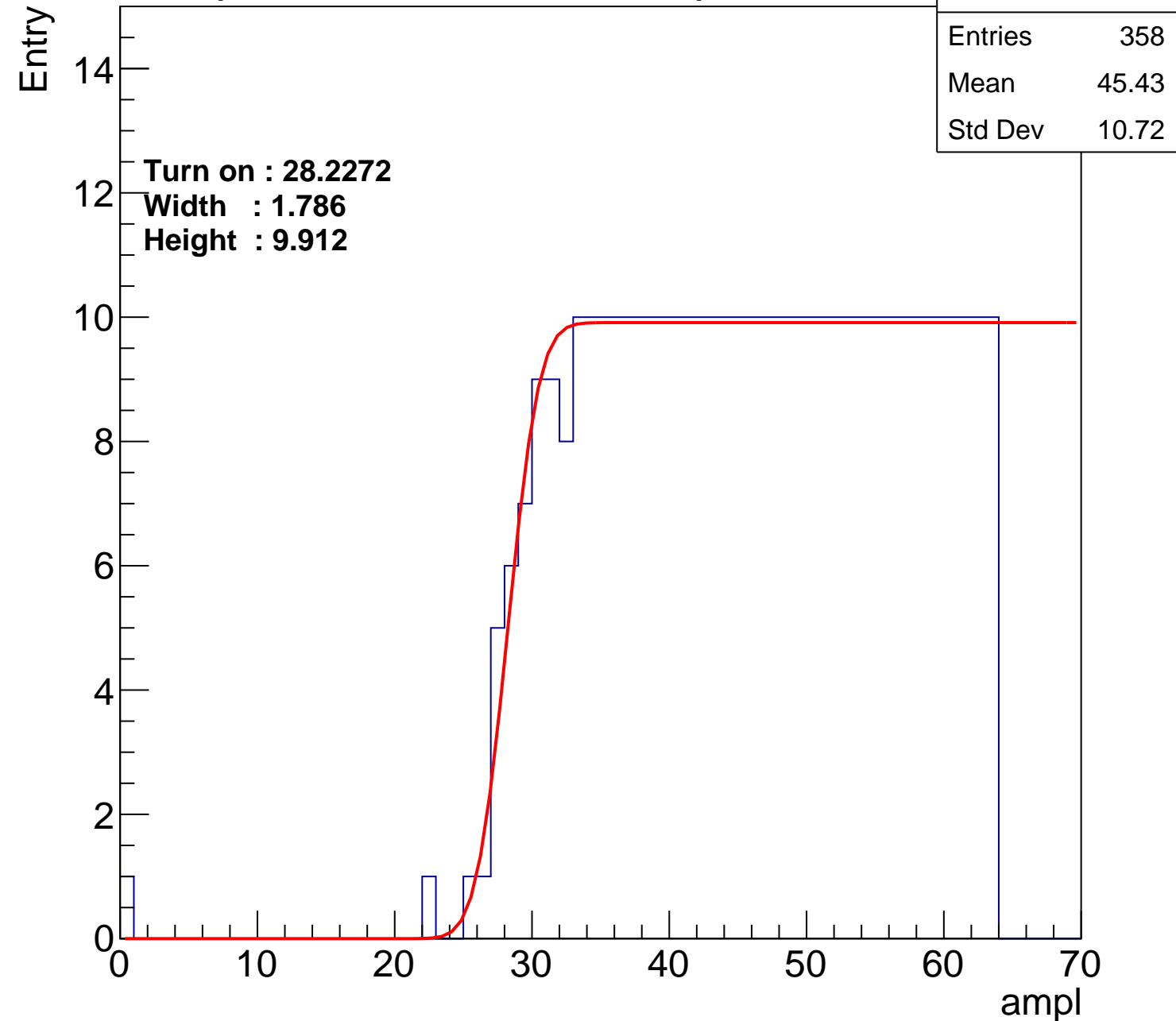
Width : 1.786

Height : 9.912

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch34

calib_packv5_042523_0143.root, FC#4, port A2

Entries	384
Mean	44.15
Std Dev	11.4

Turn on : 25.6790

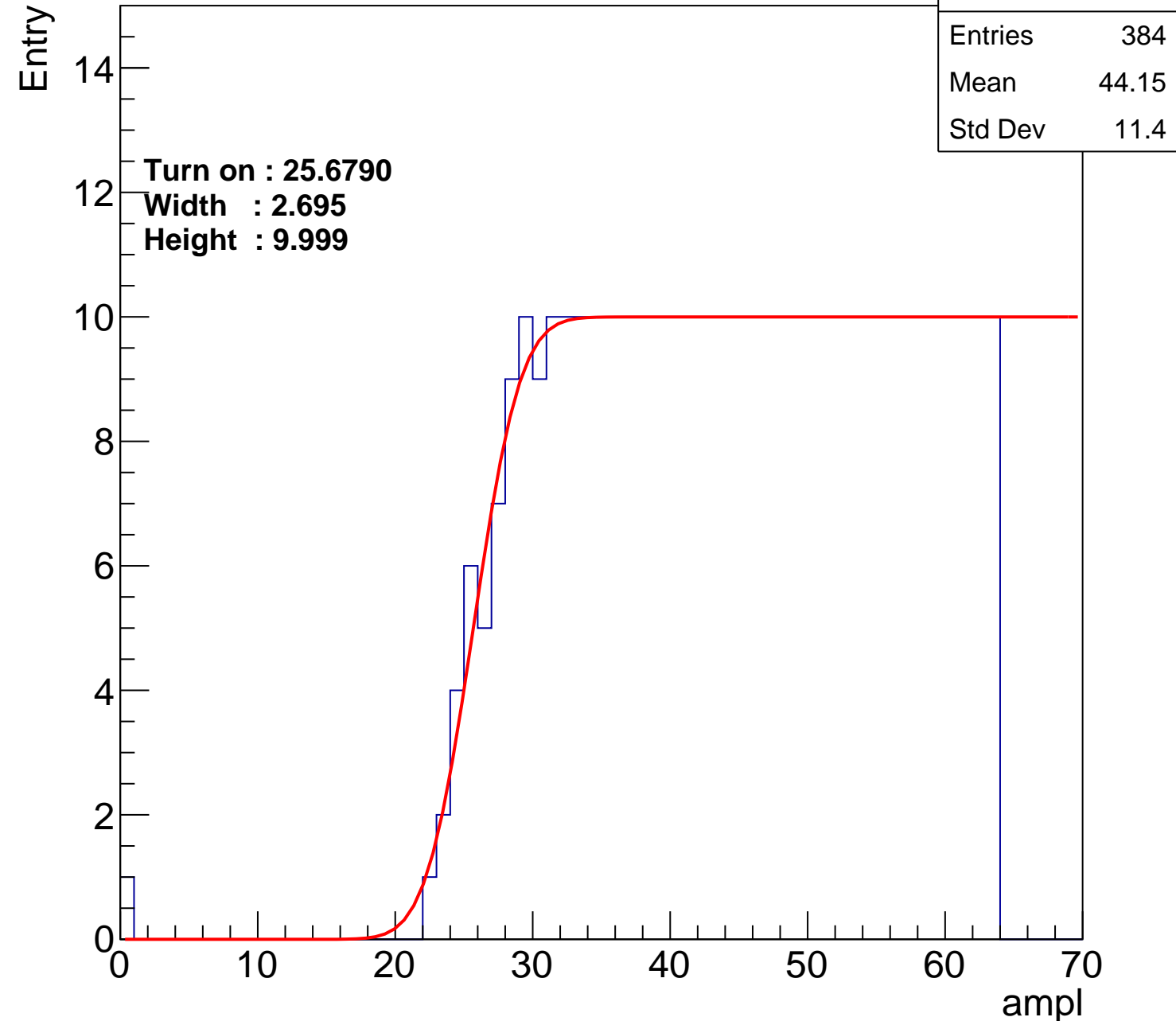
Width : 2.695

Height : 9.999

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch35

calib_packv5_042523_0143.root, FC#4, port A2

Entries	362
Mean	45.14
Std Dev	11.07

Turn on : 28.4148

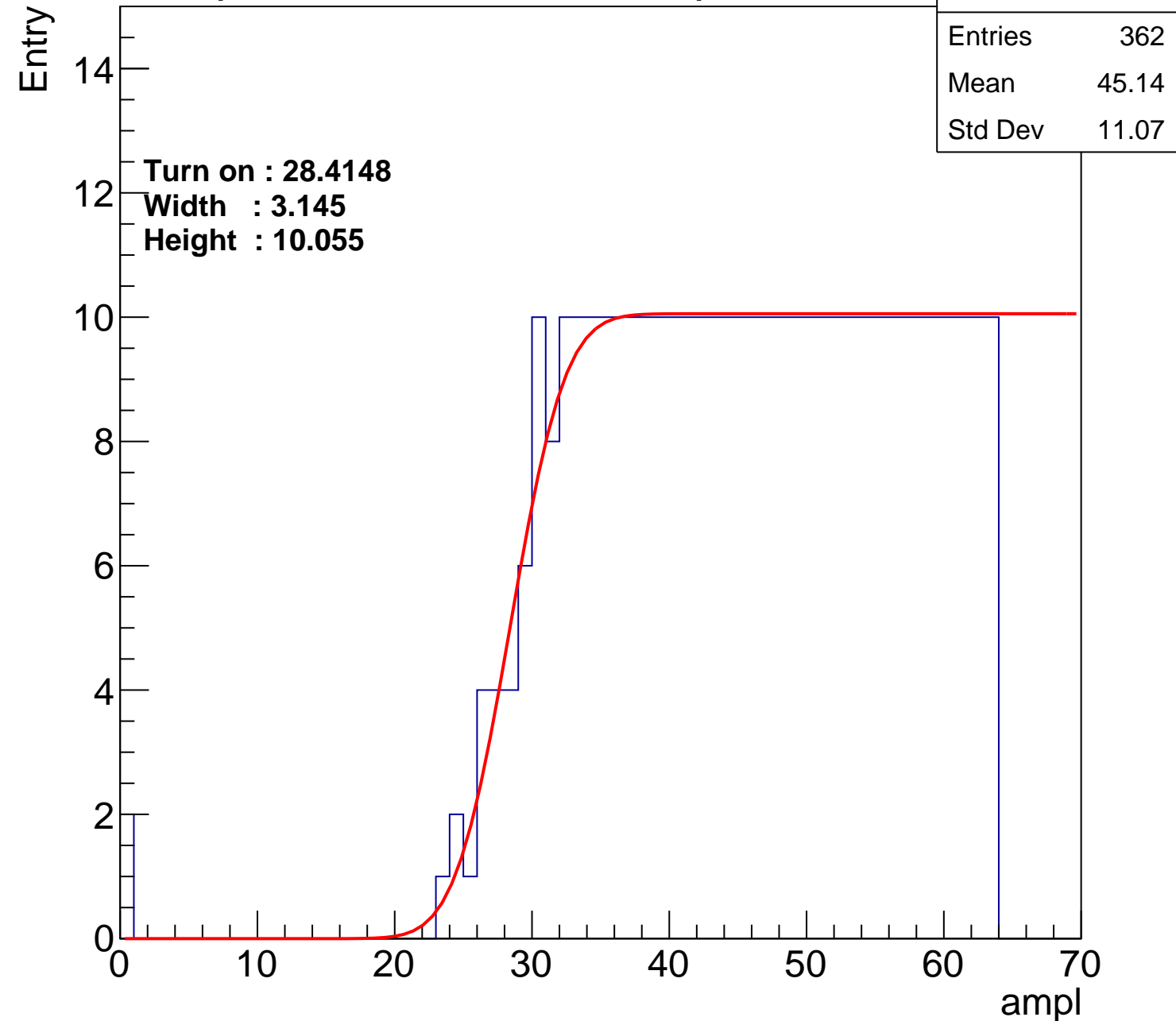
Width : 3.145

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch36

calib_packv5_042523_0143.root, FC#4, port A2

Entries	389
Mean	43.73
Std Dev	12.03

Turn on : 26.3258

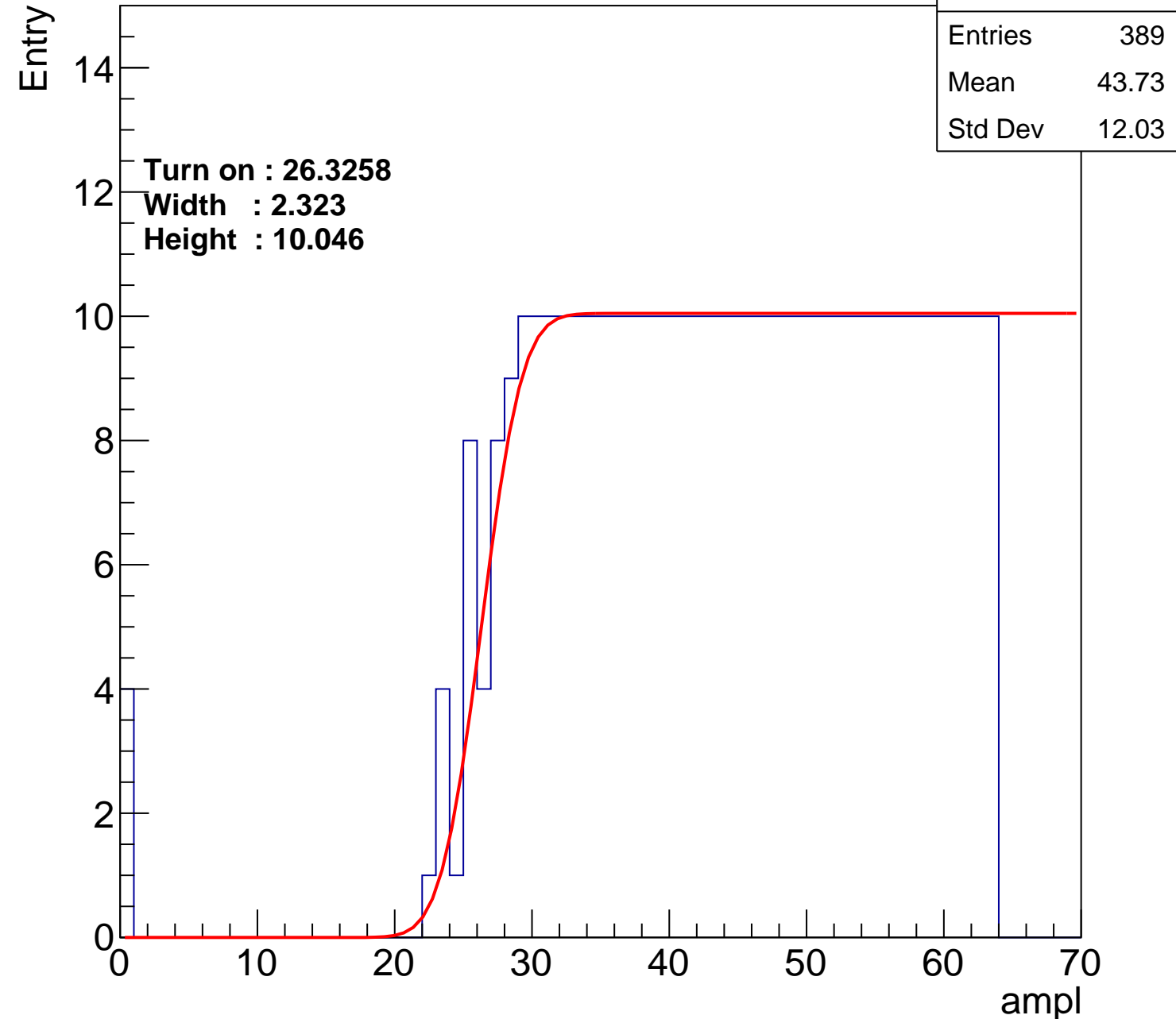
Width : 2.323

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch37

calib_packv5_042523_0143.root, FC#4, port A2

Entries	386
Mean	43.99
Std Dev	11.63

Turn on : 24.9656

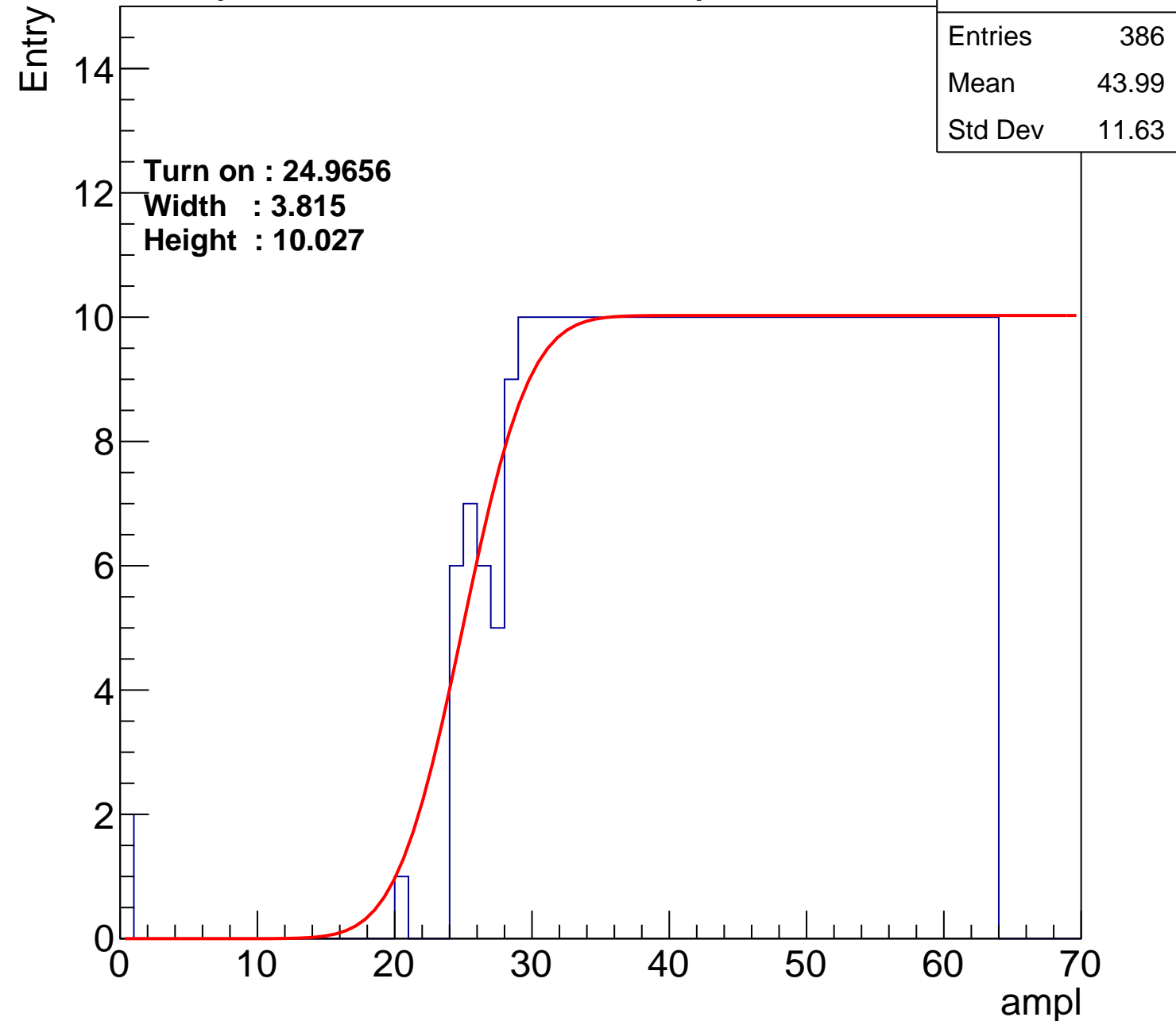
Width : 3.815

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch38

calib_packv5_042523_0143.root, FC#4, port A2

Entries	368
Mean	44.71
Std Dev	11.61

Turn on : 27.9439

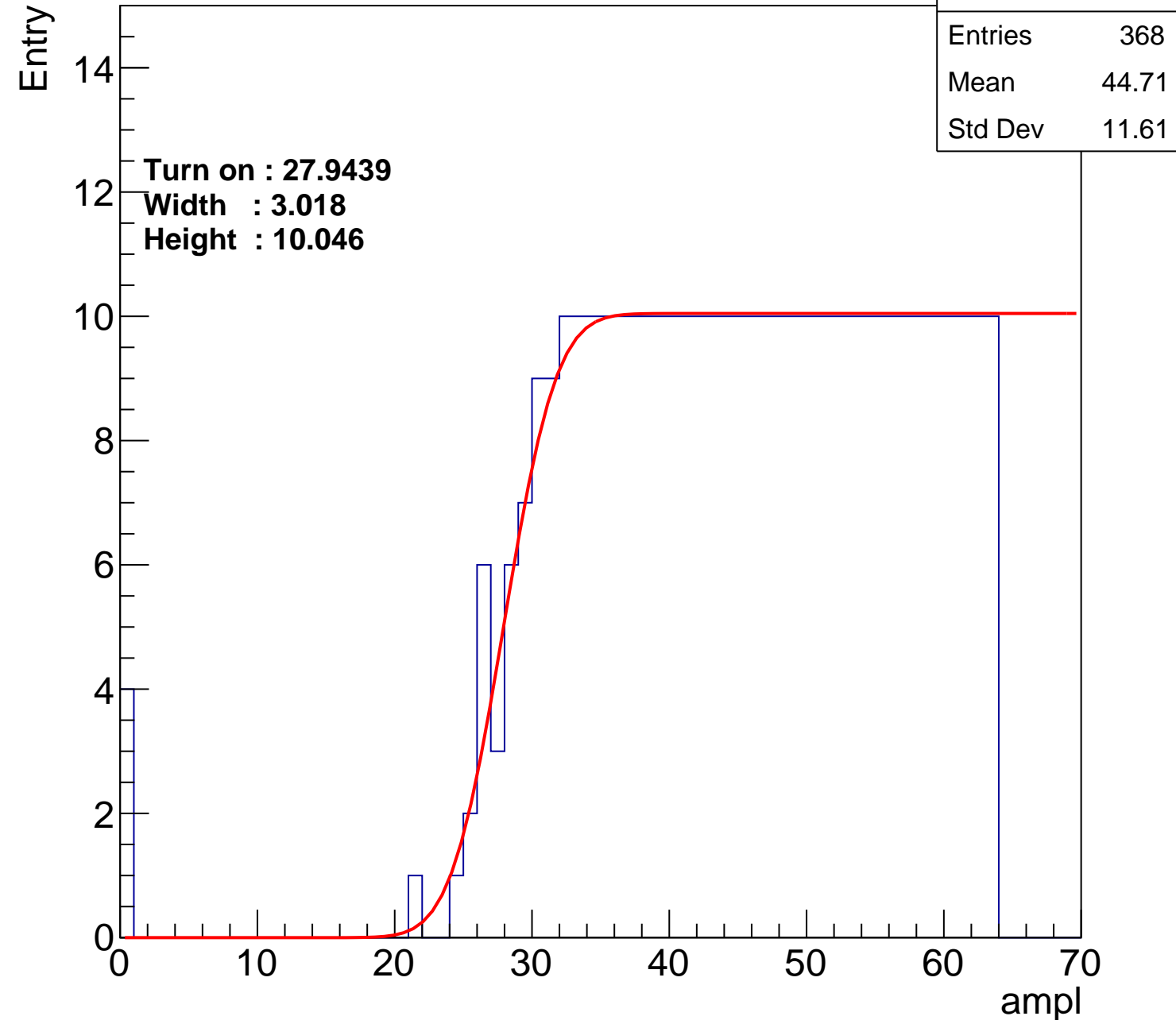
Width : 3.018

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch39

calib_packv5_042523_0143.root, FC#4, port A2

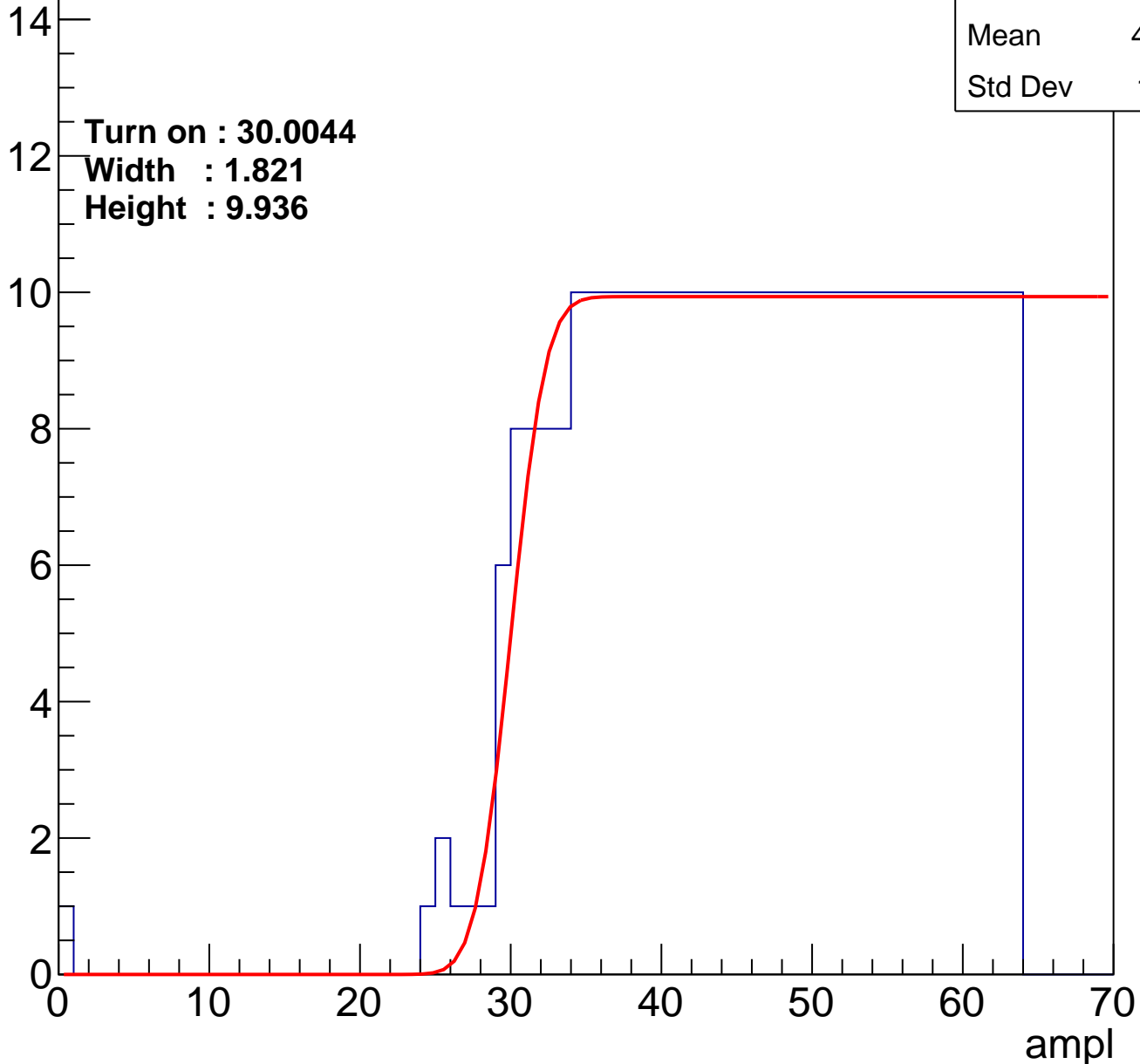
Entries	345
Mean	46.05
Std Dev	10.41

Turn on : 30.0044

Width : 1.821

Height : 9.936

Entry



B1L100S, U8-ch40

calib_packv5_042523_0143.root, FC#4, port A2

Entries	374
Mean	44.5
Std Dev	11.54

Turn on : 27.3394

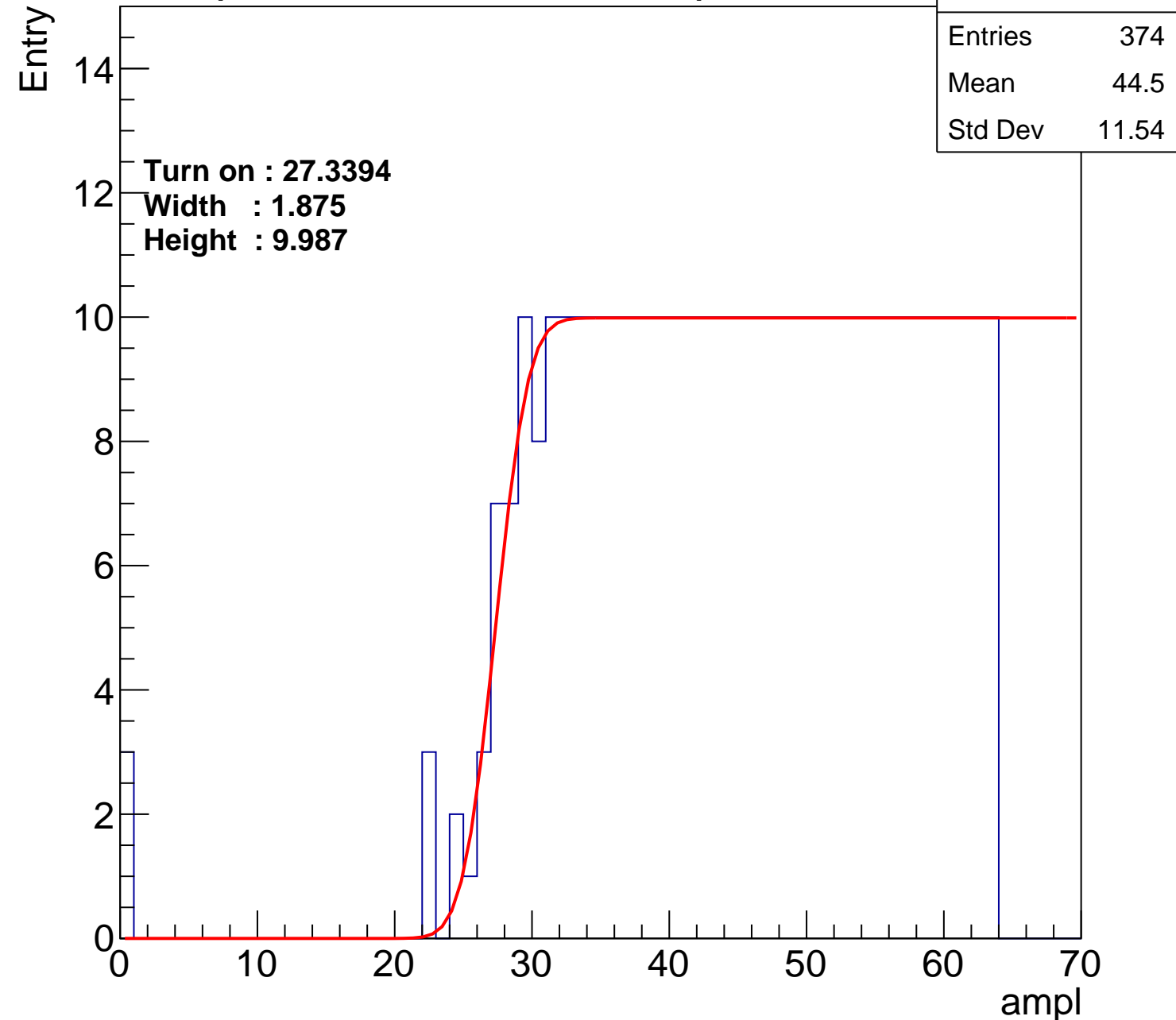
Width : 1.875

Height : 9.987

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch41

calib_packv5_042523_0143.root, FC#4, port A2

Entries	382
Mean	44.1
Std Dev	11.73

Turn on : 26.2423

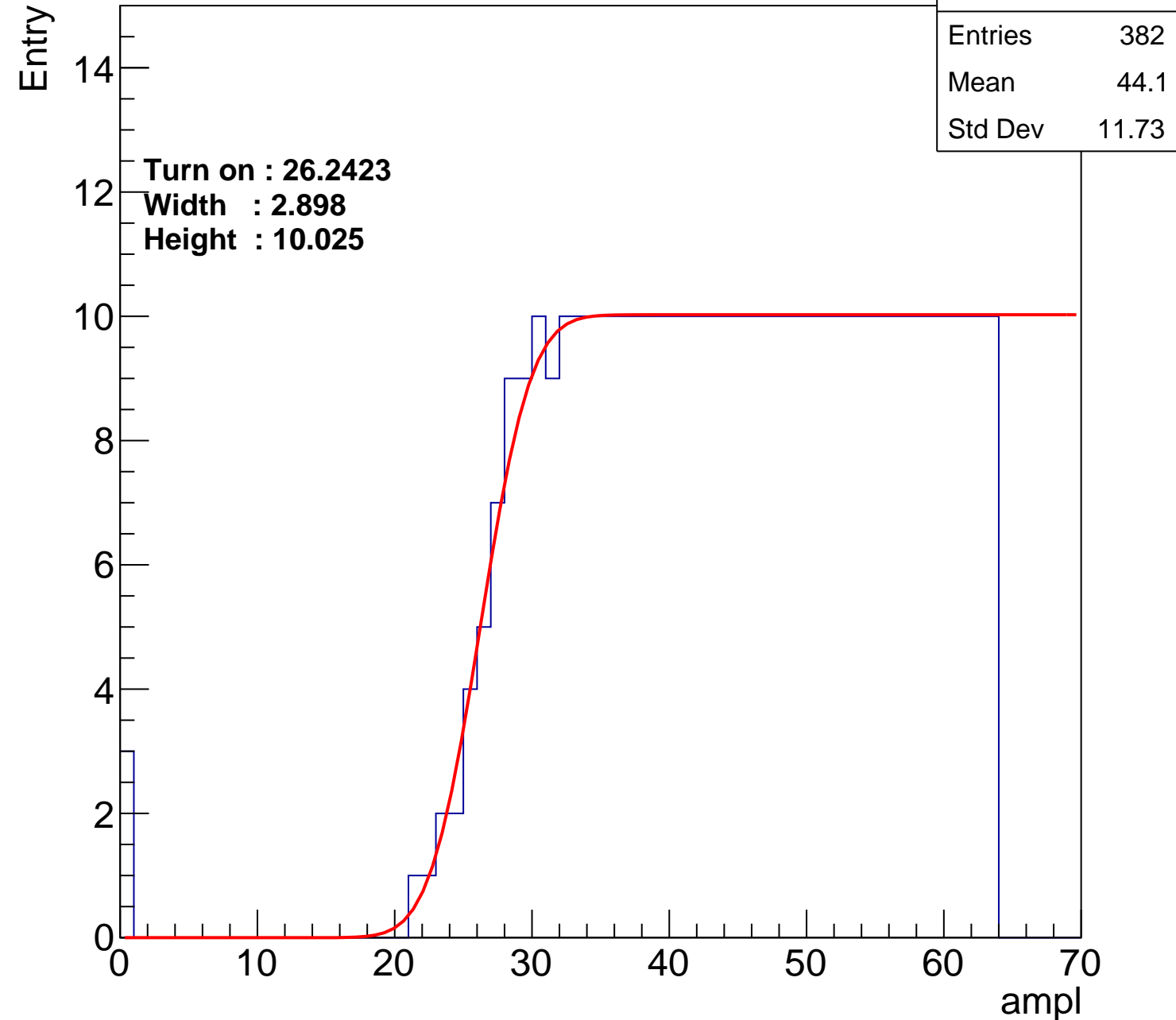
Width : 2.898

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch42

calib_packv5_042523_0143.root, FC#4, port A2

Entries	392
Mean	43.63
Std Dev	11.95

Turn on : 25.1374

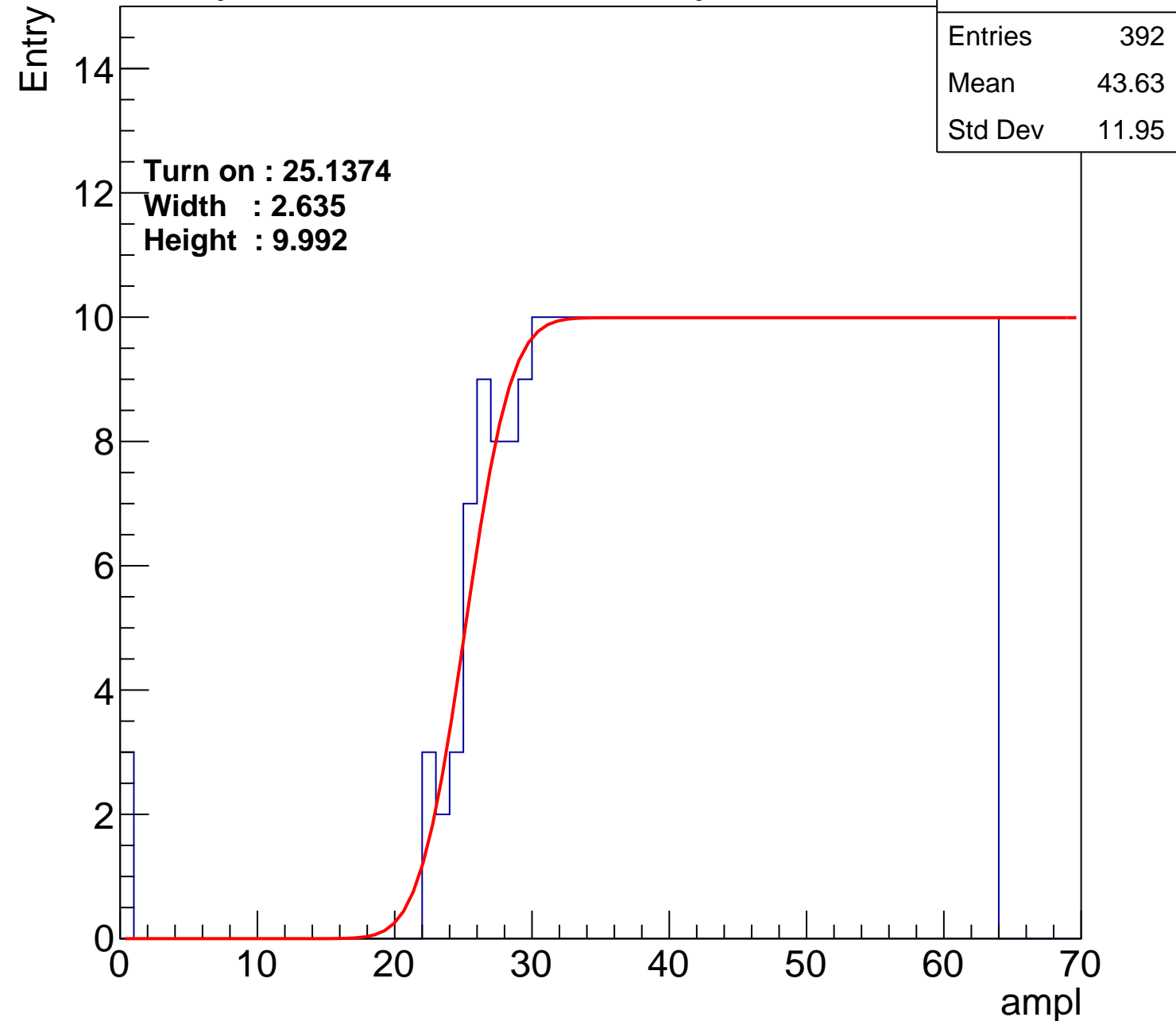
Width : 2.635

Height : 9.992

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch43

calib_packv5_042523_0143.root, FC#4, port A2

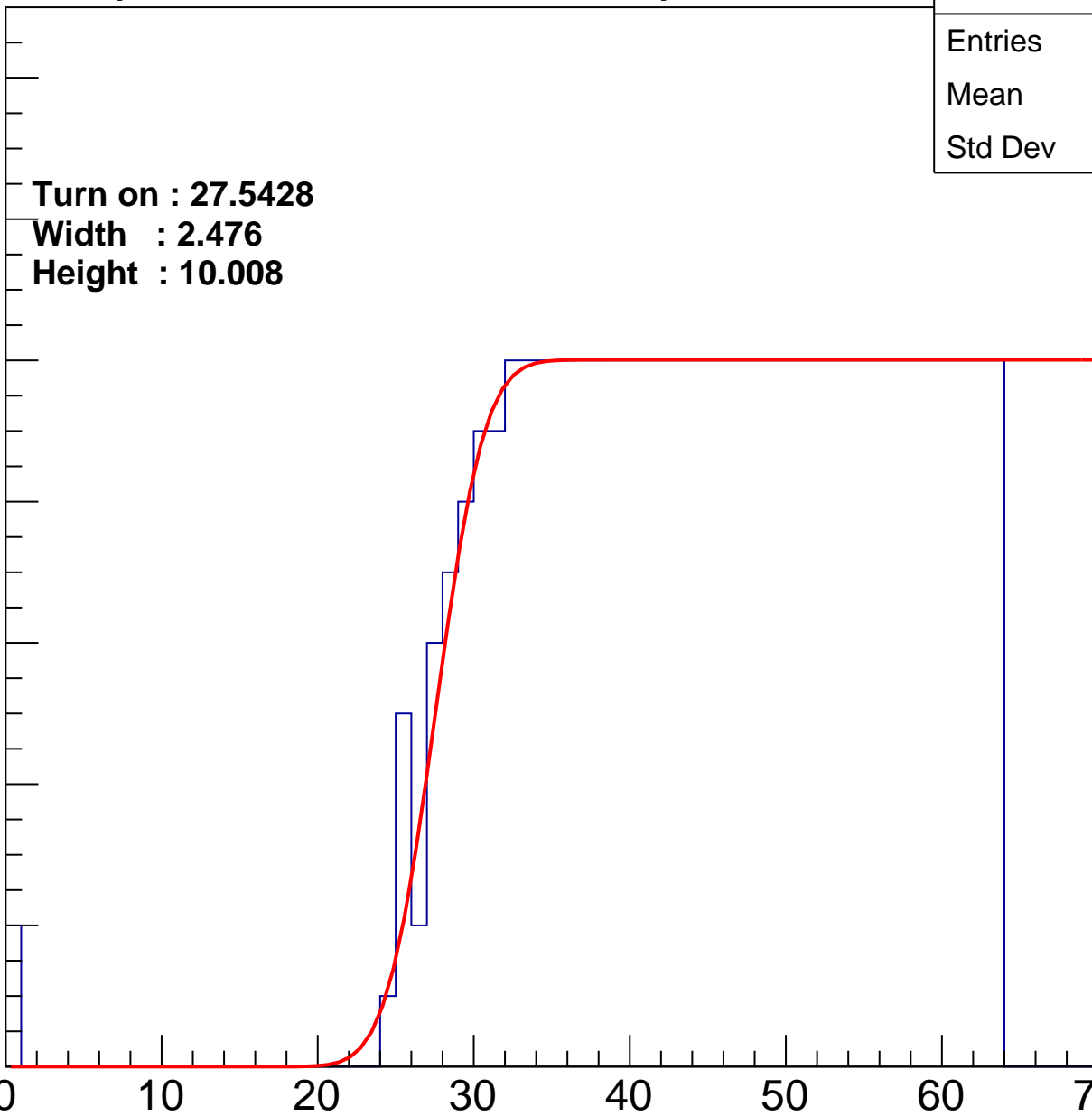
Entry

14
12
10
8
6
4
2
0

Turn on : 27.5428
Width : 2.476
Height : 10.008

Entries	369
Mean	44.82
Std Dev	11.2

ampl



B1L100S, U8-ch44

calib_packv5_042523_0143.root, FC#4, port A2

Entries	391
Mean	43.81
Std Dev	11.58

Turn on : 24.9966

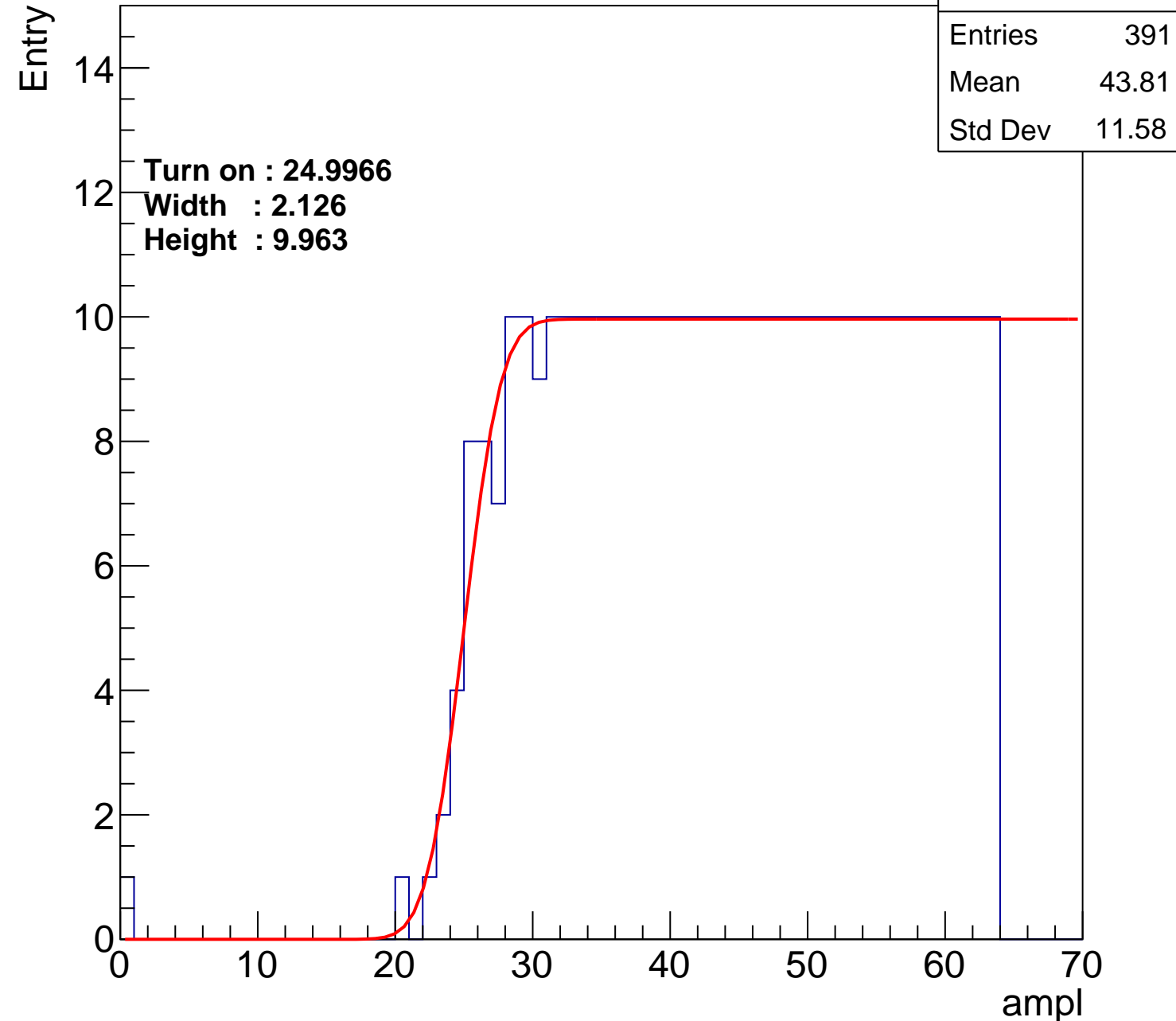
Width : 2.126

Height : 9.963

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch45

calib_packv5_042523_0143.root, FC#4, port A2

Entries	364
Mean	45.13
Std Dev	10.89

Turn on : 28.5123

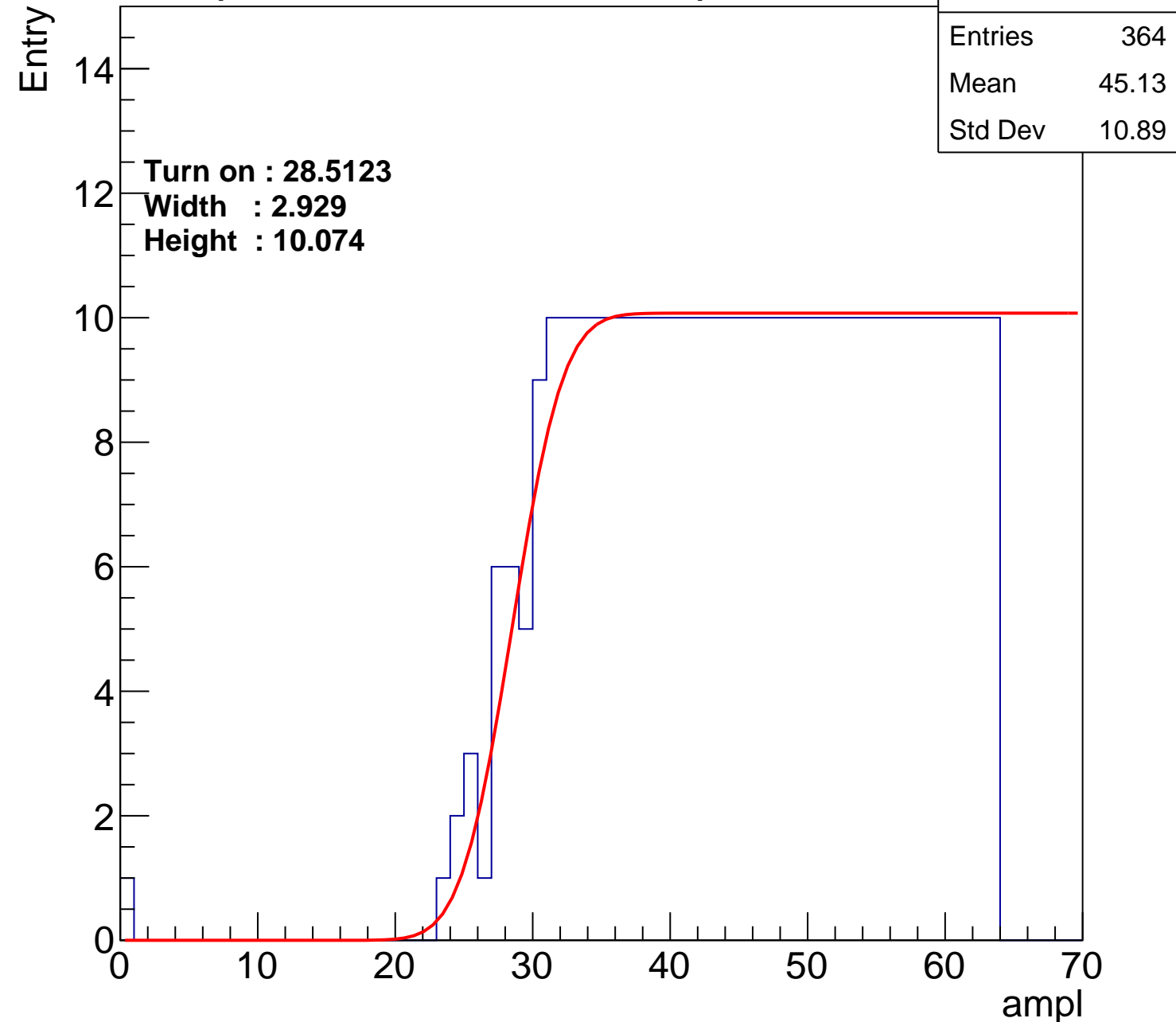
Width : 2.929

Height : 10.074

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch46

calib_packv5_042523_0143.root, FC#4, port A2

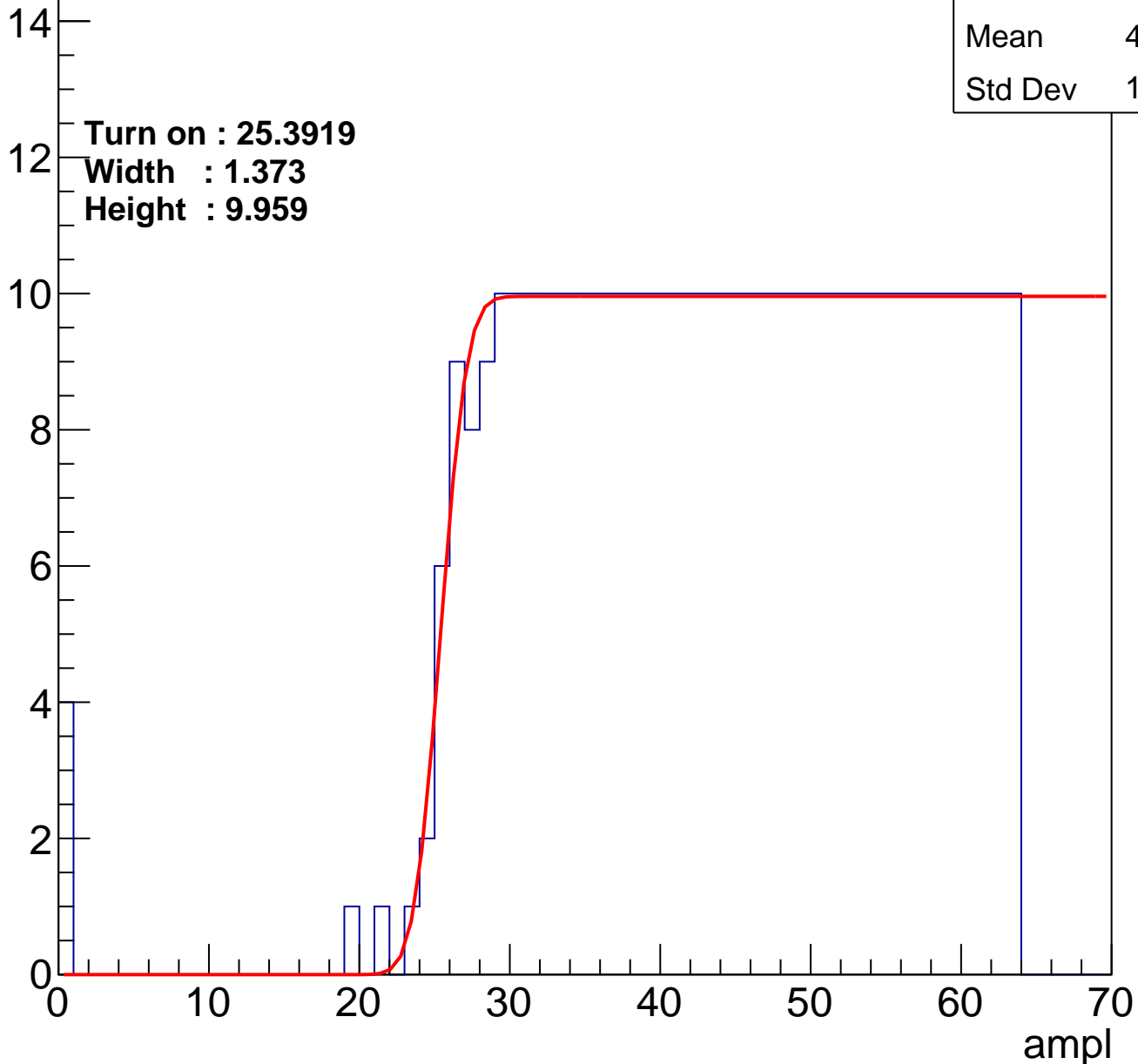
Entries	391
Mean	43.64
Std Dev	12.06

Turn on : 25.3919

Width : 1.373

Height : 9.959

Entry



B1L100S, U8-ch47

calib_packv5_042523_0143.root, FC#4, port A2

Entries	346
Mean	45.93
Std Dev	10.66

Turn on : 30.0086

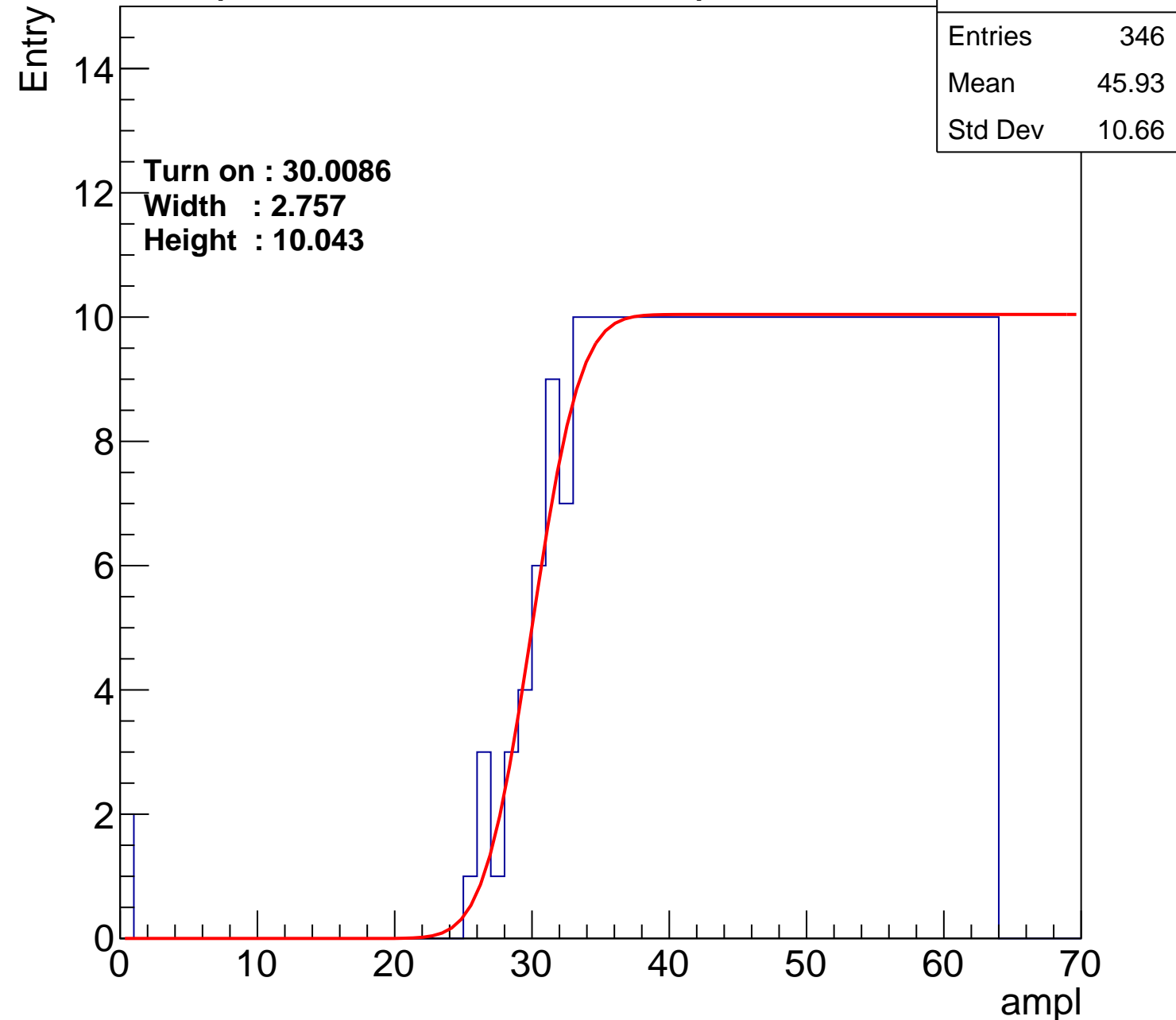
Width : 2.757

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch48

calib_packv5_042523_0143.root, FC#4, port A2

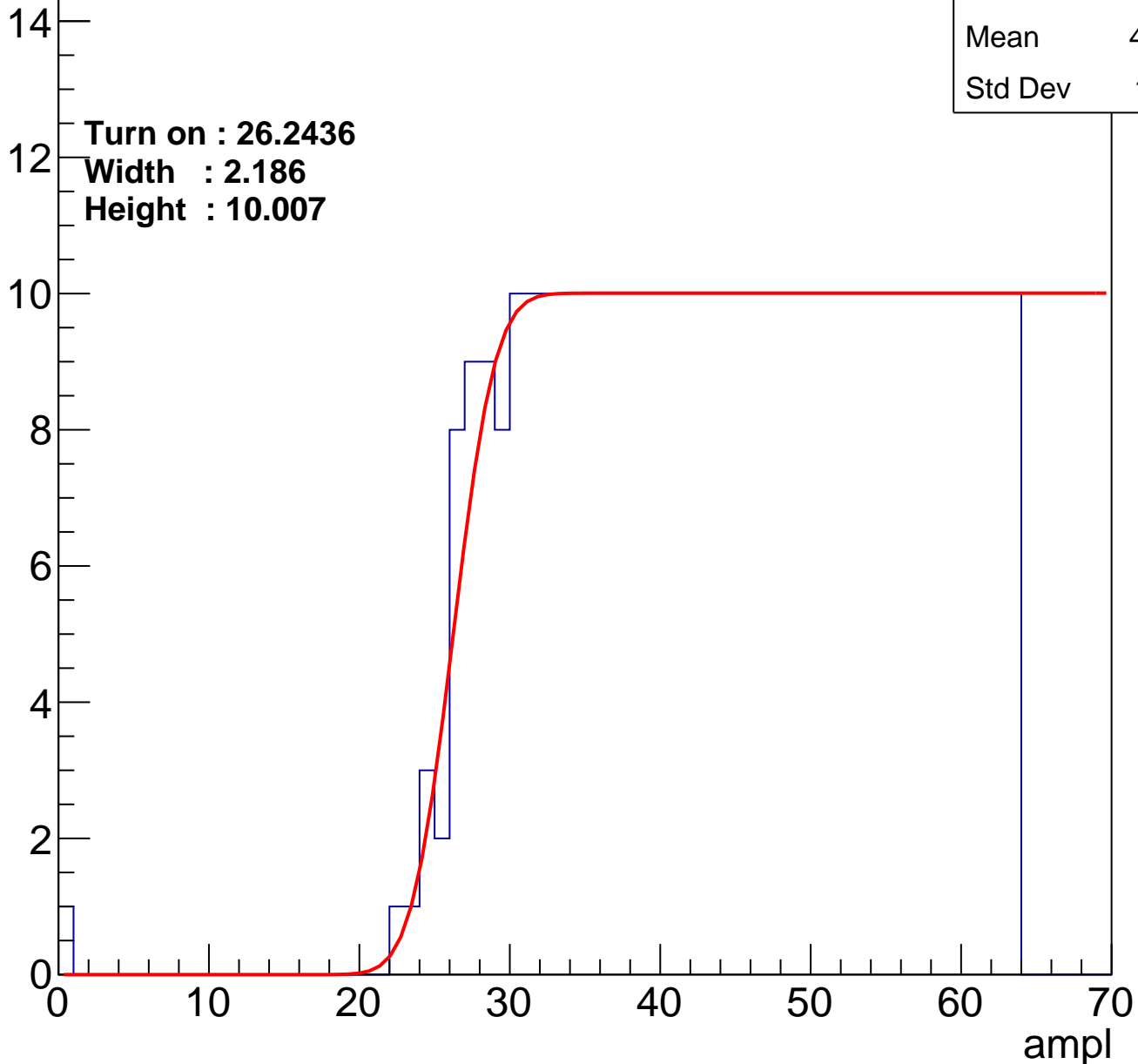
Entries	382
Mean	44.27
Std Dev	11.31

Turn on : 26.2436

Width : 2.186

Height : 10.007

Entry



B1L100S, U8-ch49

calib_packv5_042523_0143.root, FC#4, port A2

Entries	367
Mean	44.77
Std Dev	11.49

Turn on : 28.3763

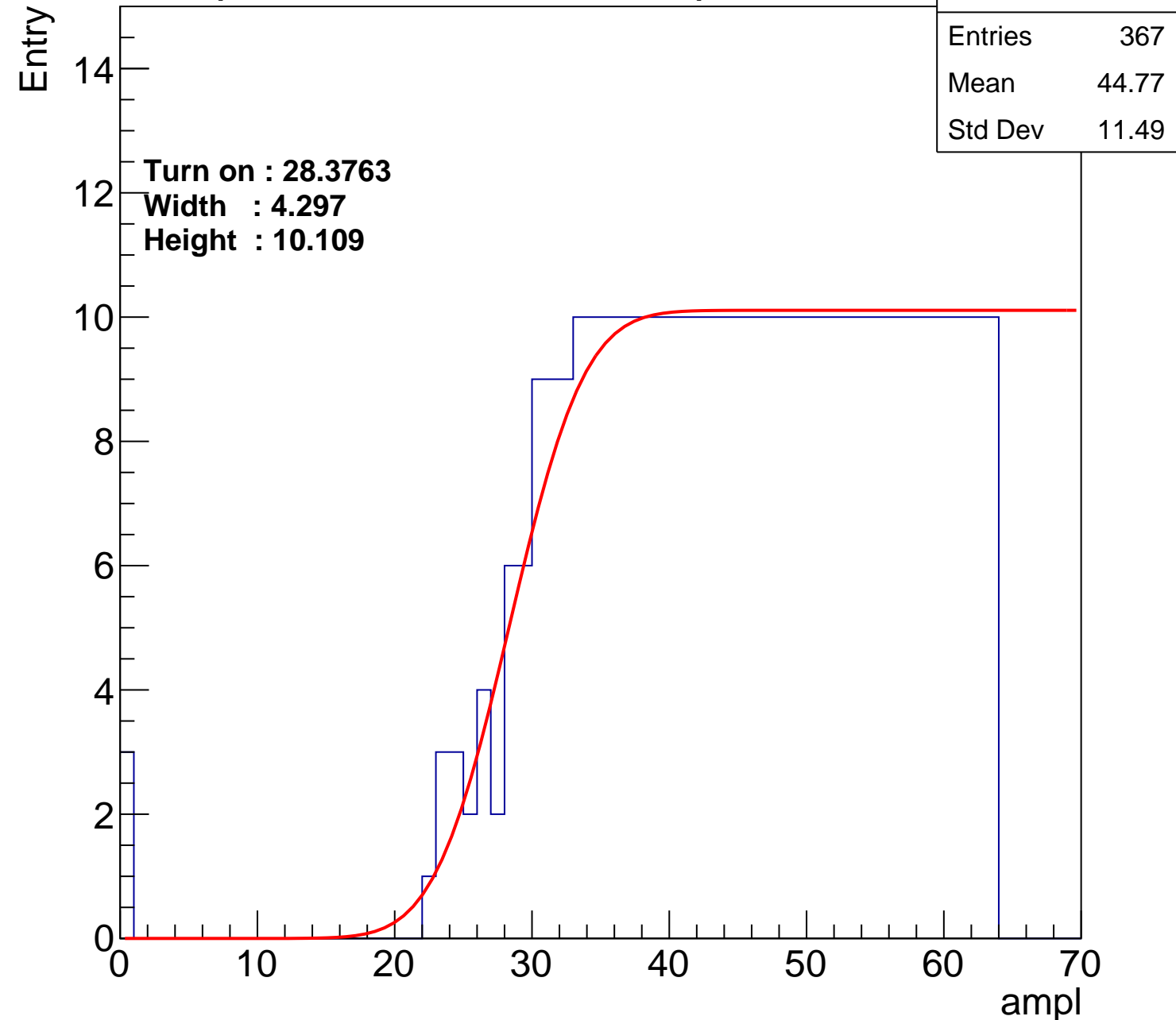
Width : 4.297

Height : 10.109

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch50

calib_packv5_042523_0143.root, FC#4, port A2

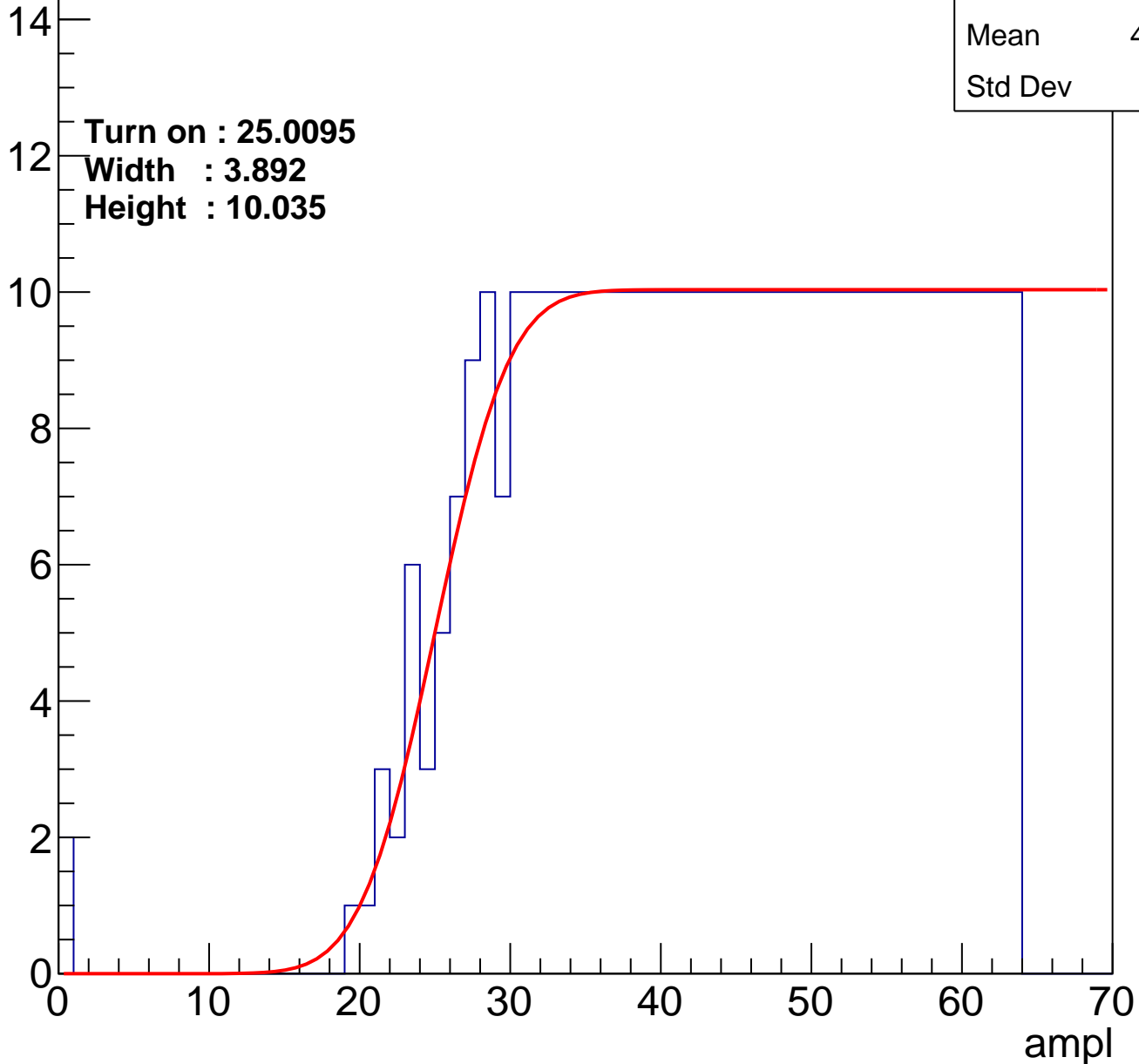
Entries	396
Mean	43.43
Std Dev	12

Turn on : 25.0095

Width : 3.892

Height : 10.035

Entry



B1L100S, U8-ch51

calib_packv5_042523_0143.root, FC#4, port A2

Entries	381
Mean	44.21
Std Dev	11.56

Turn on : 26.3661

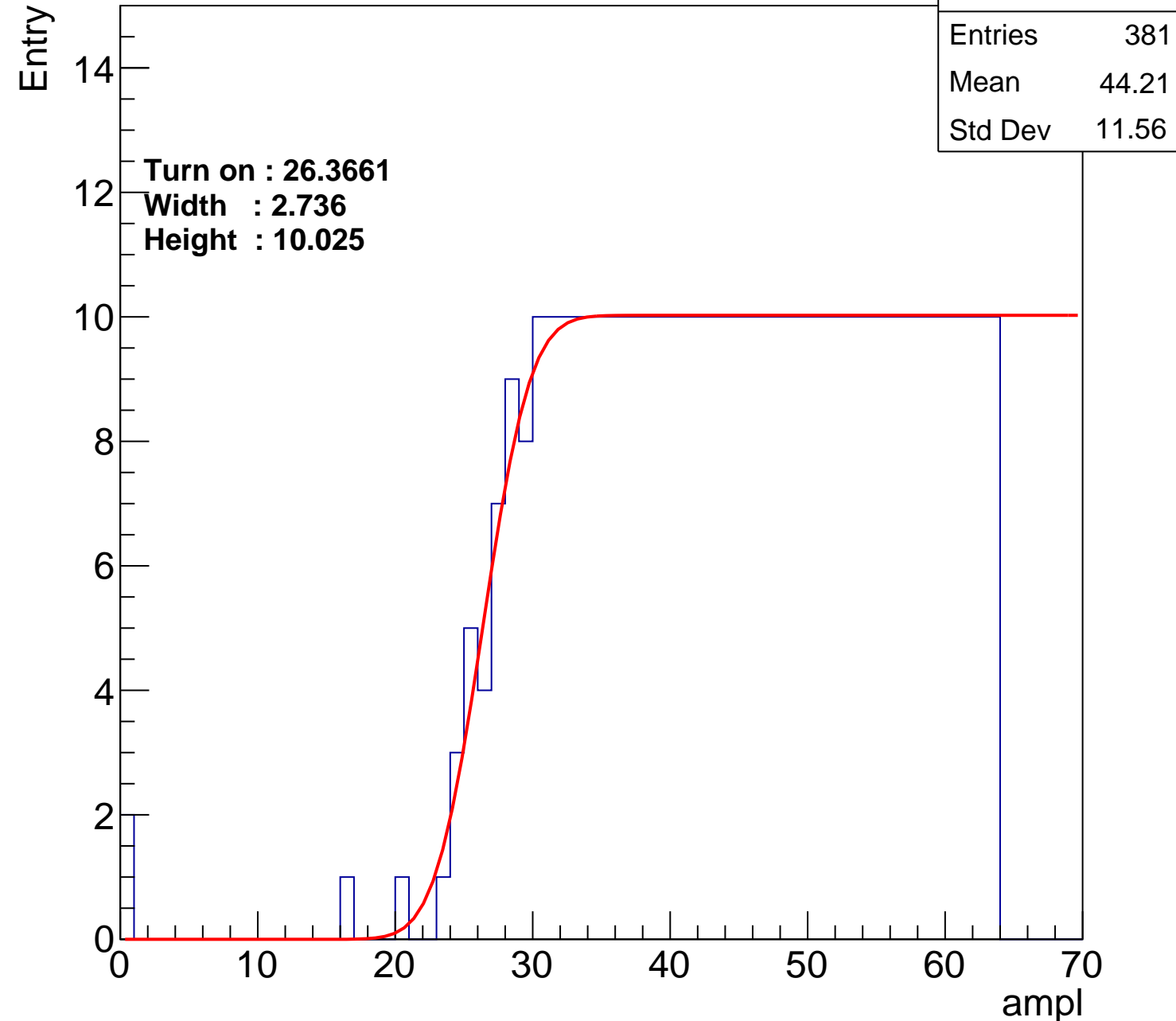
Width : 2.736

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch52

calib_packv5_042523_0143.root, FC#4, port A2

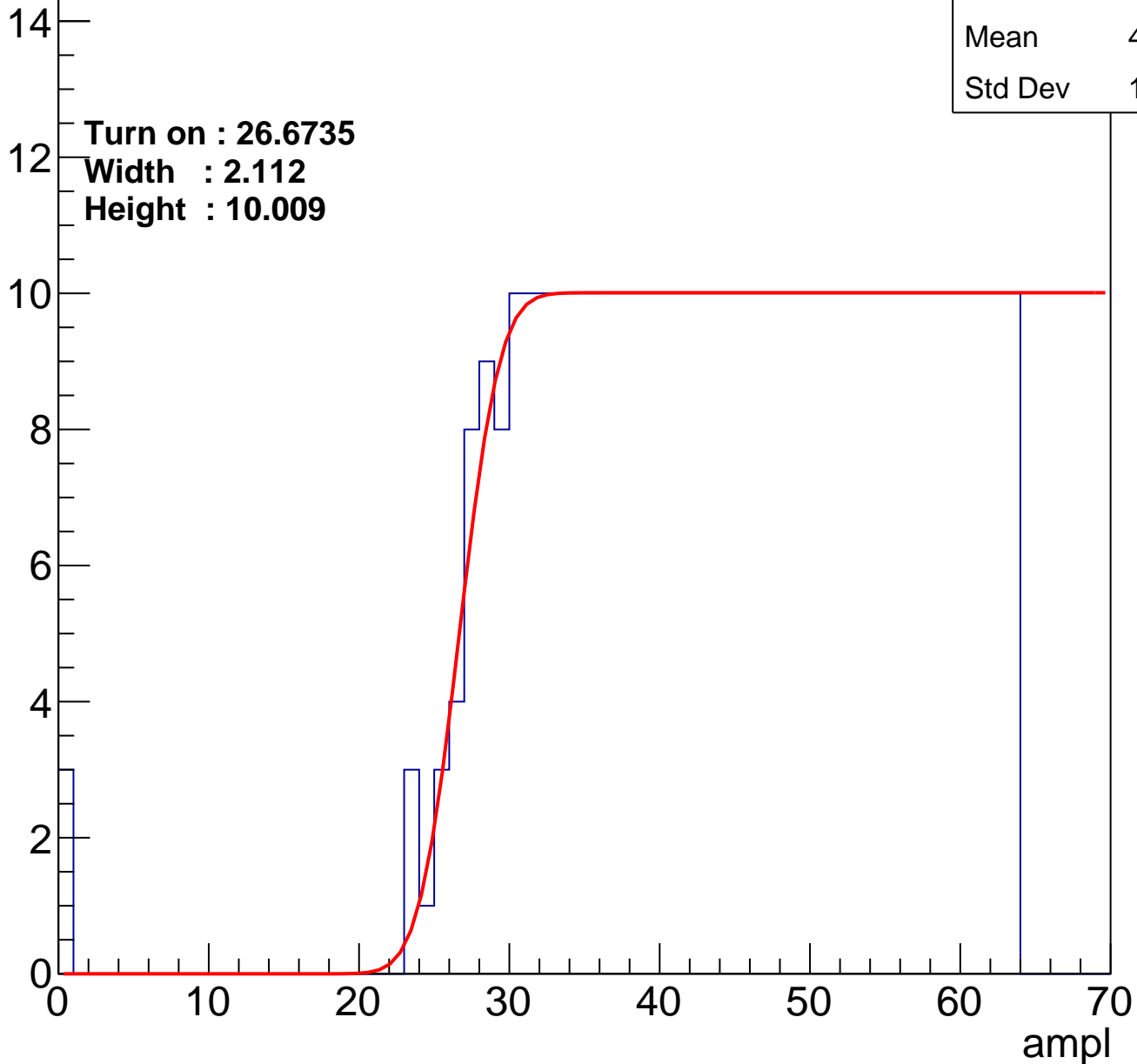
Entries	379
Mean	44.28
Std Dev	11.62

Turn on : 26.6735

Width : 2.112

Height : 10.009

Entry



B1L100S, U8-ch53

calib_packv5_042523_0143.root, FC#4, port A2

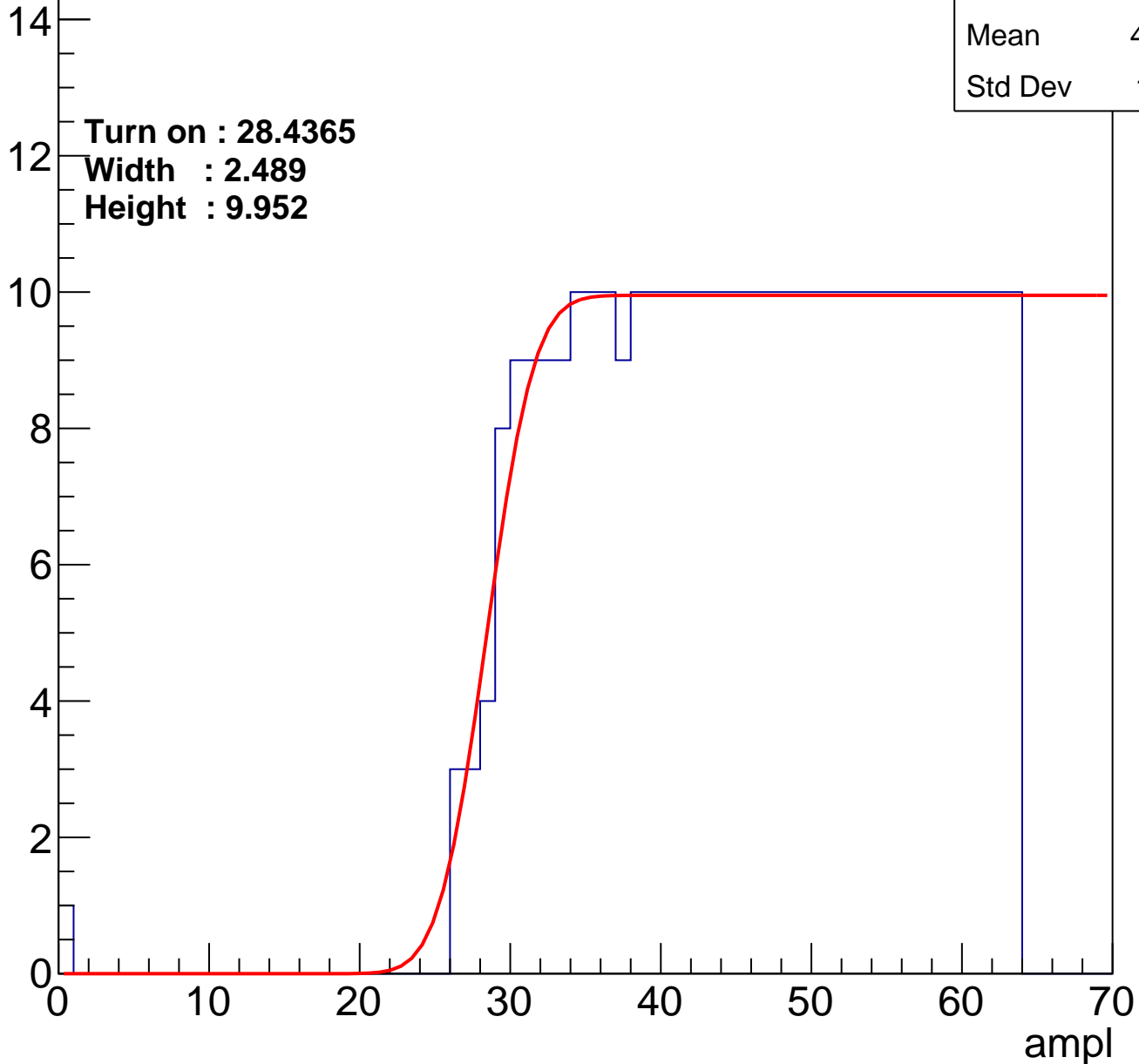
Entries	354
Mean	45.62
Std Dev	10.61

Turn on : 28.4365

Width : 2.489

Height : 9.952

Entry



B1L100S, U8-ch54

calib_packv5_042523_0143.root, FC#4, port A2

Entries	374
Mean	44.55
Std Dev	11.37

Turn on : 27.6964

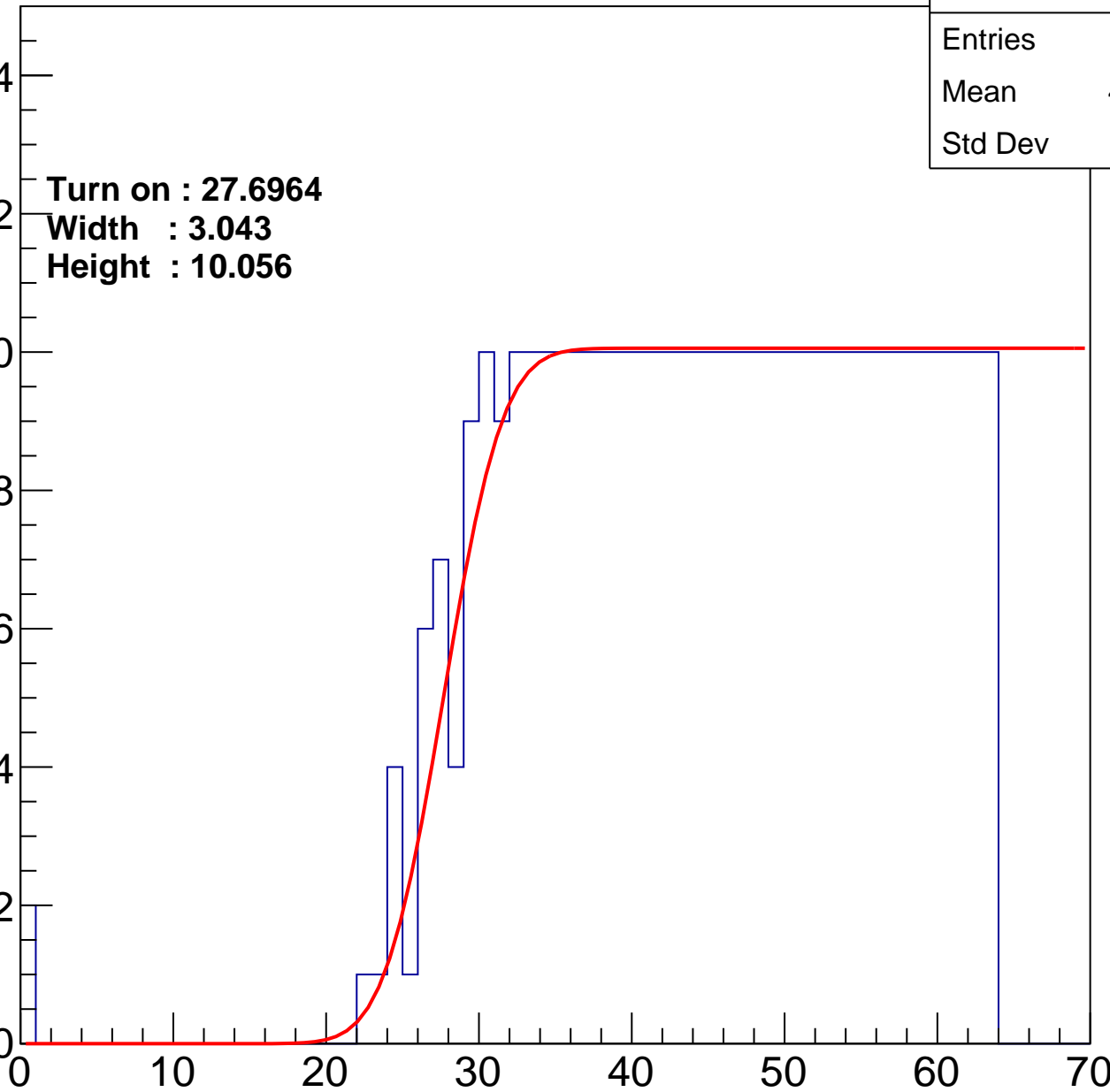
Width : 3.043

Height : 10.056

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch55

calib_packv5_042523_0143.root, FC#4, port A2

Entries	381
Mean	44.24
Std Dev	11.5

Turn on : 26.4675

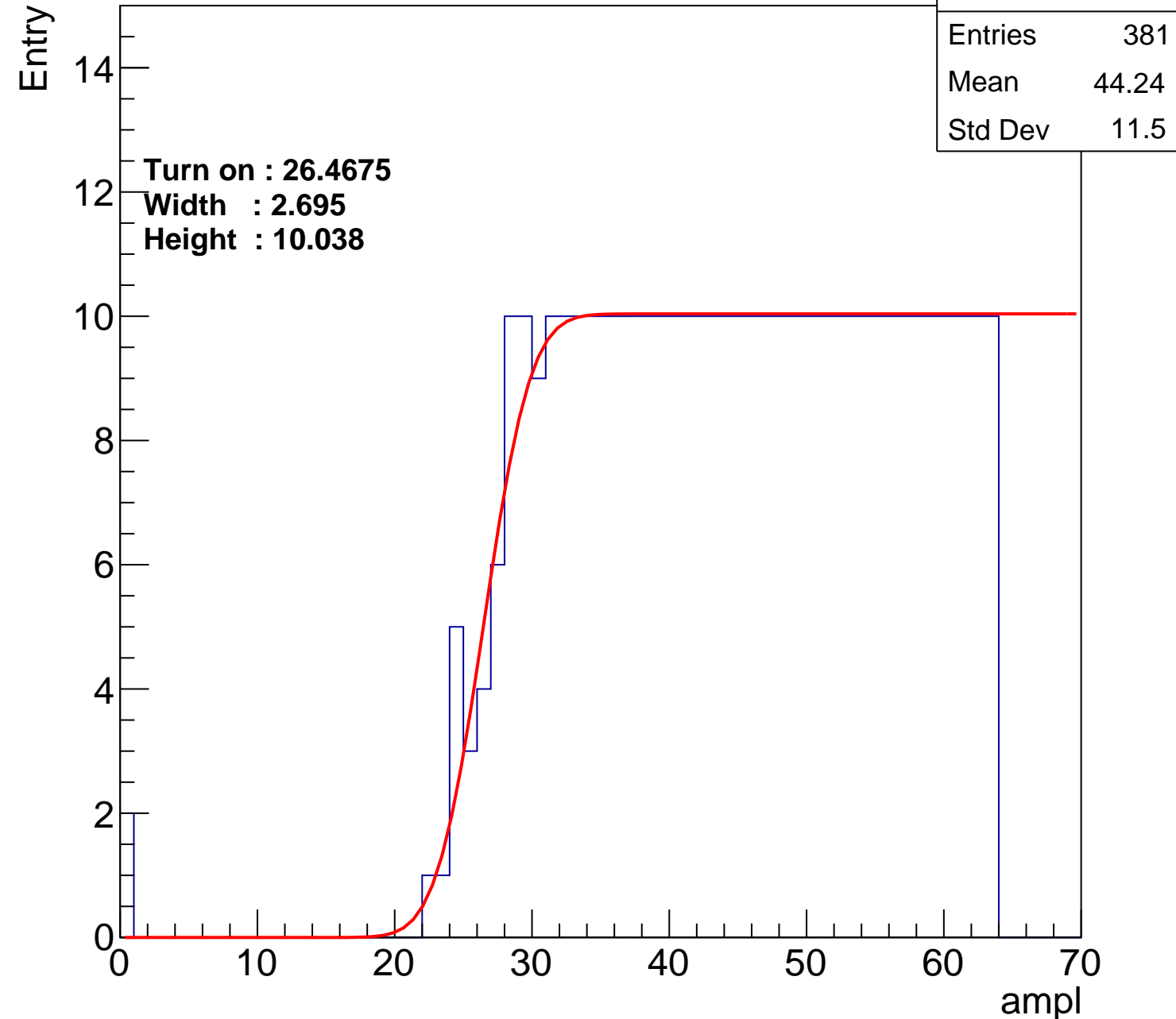
Width : 2.695

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch56

calib_packv5_042523_0143.root, FC#4, port A2

Entries	377
Mean	44.54
Std Dev	11.15

Turn on : 26.5543

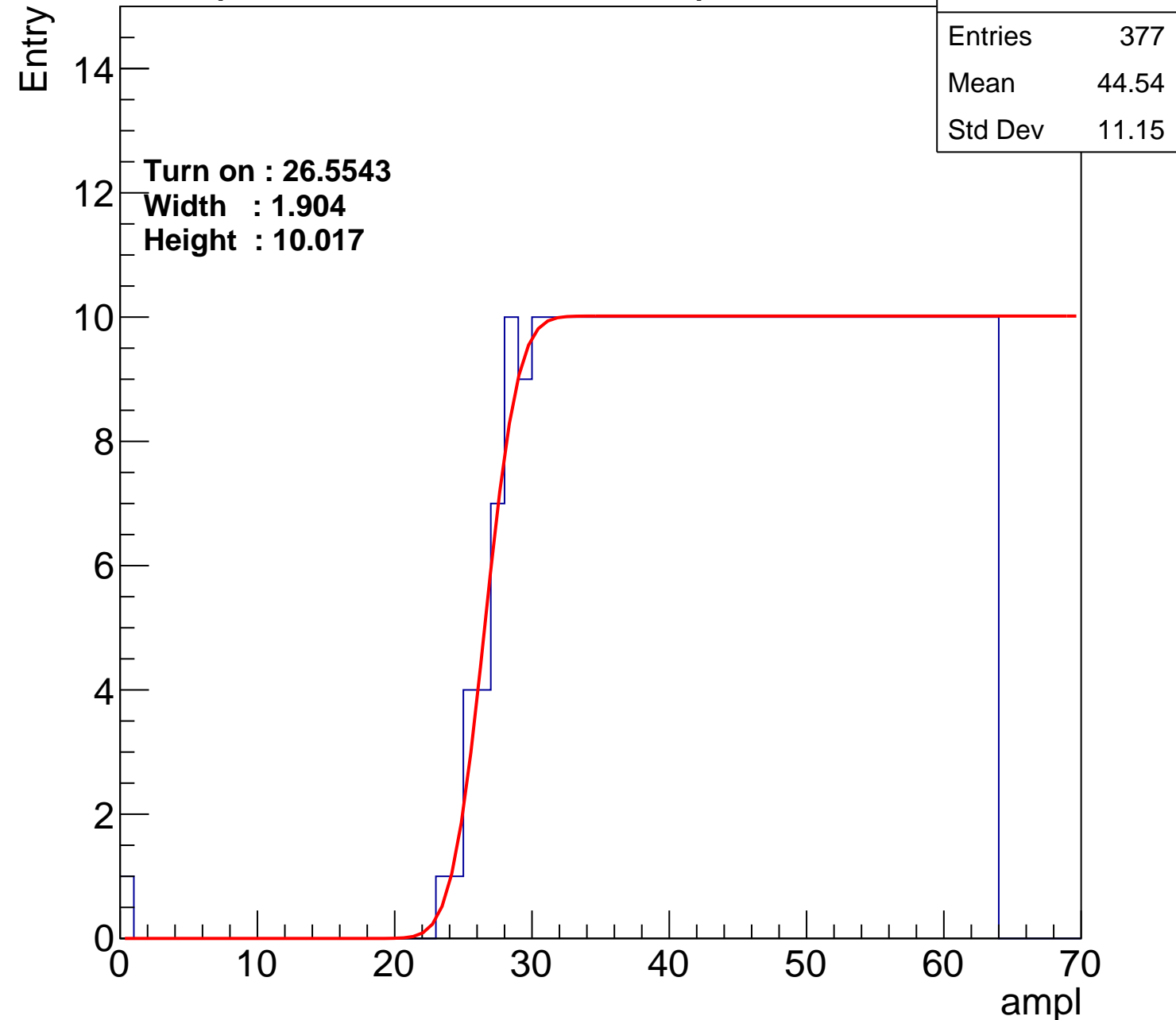
Width : 1.904

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch57

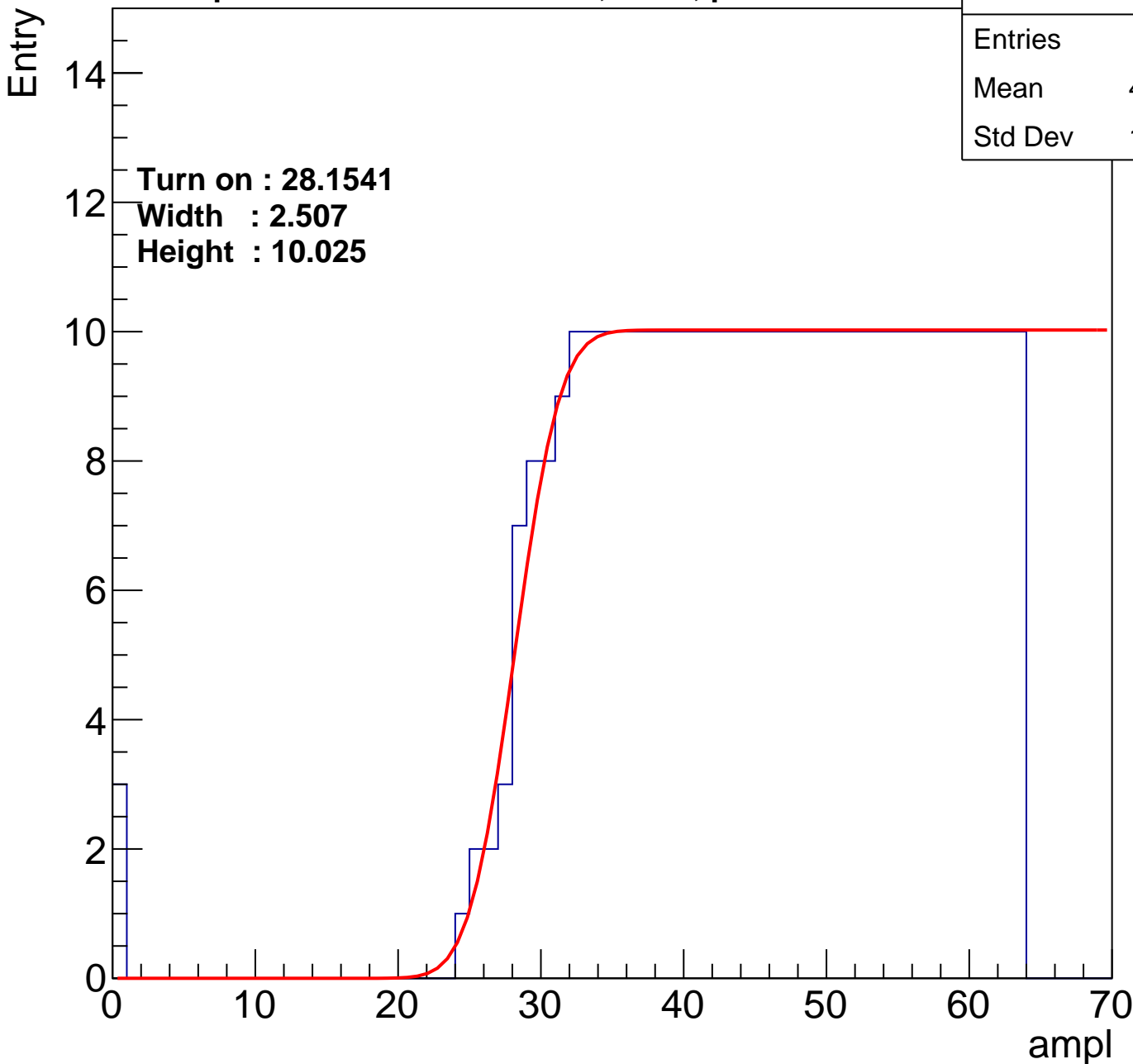
calib_packv5_042523_0143.root, FC#4, port A2

Entries	363
Mean	45.05
Std Dev	11.25

Turn on : 28.1541

Width : 2.507

Height : 10.025



B1L100S, U8-ch58

calib_packv5_042523_0143.root, FC#4, port A2

Entries	364
Mean	44.94
Std Dev	11.46

Turn on : 27.5326

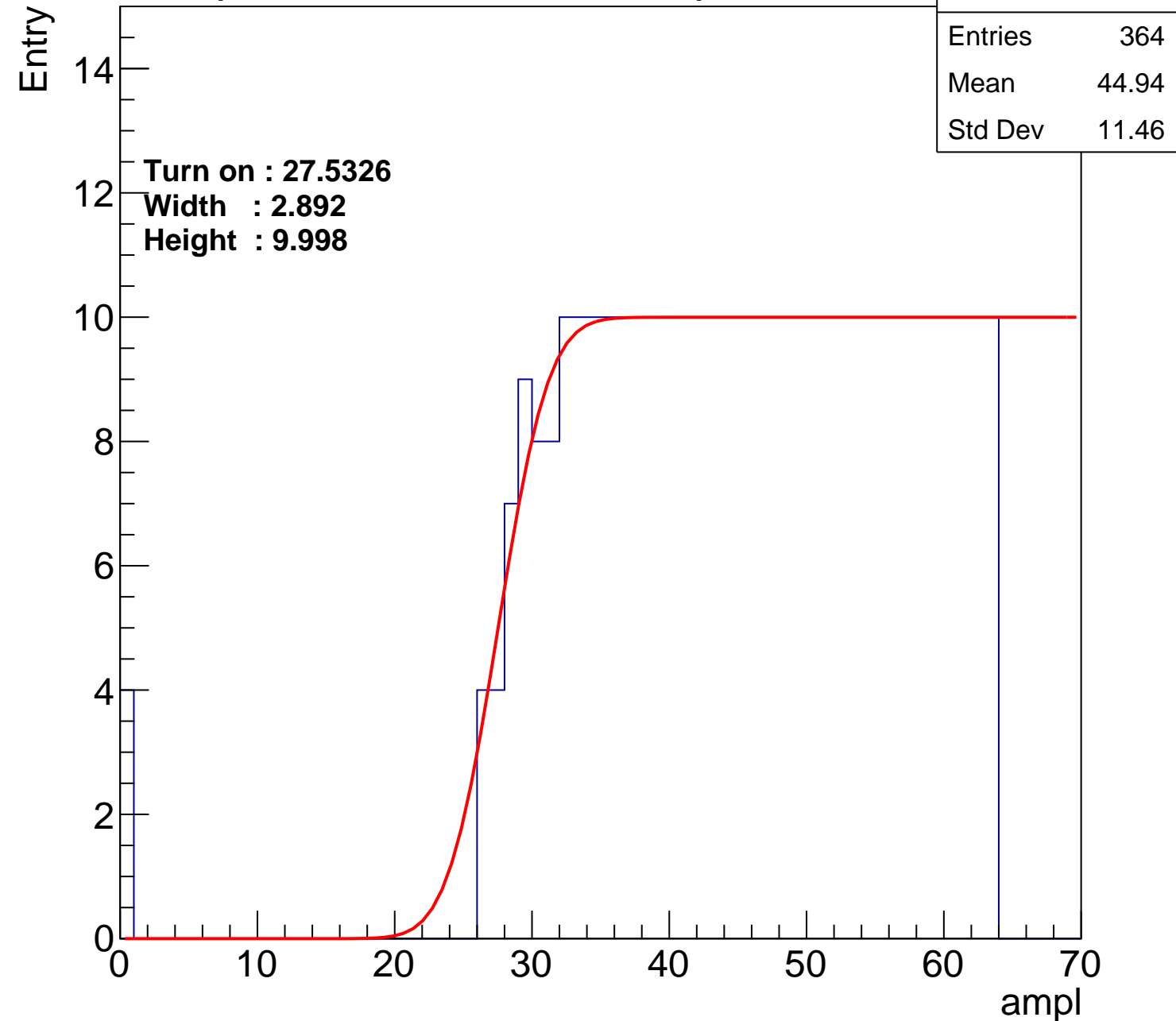
Width : 2.892

Height : 9.998

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch59

calib_packv5_042523_0143.root, FC#4, port A2

Entries	370
Mean	44.84
Std Dev	11.04

Turn on : 27.4033

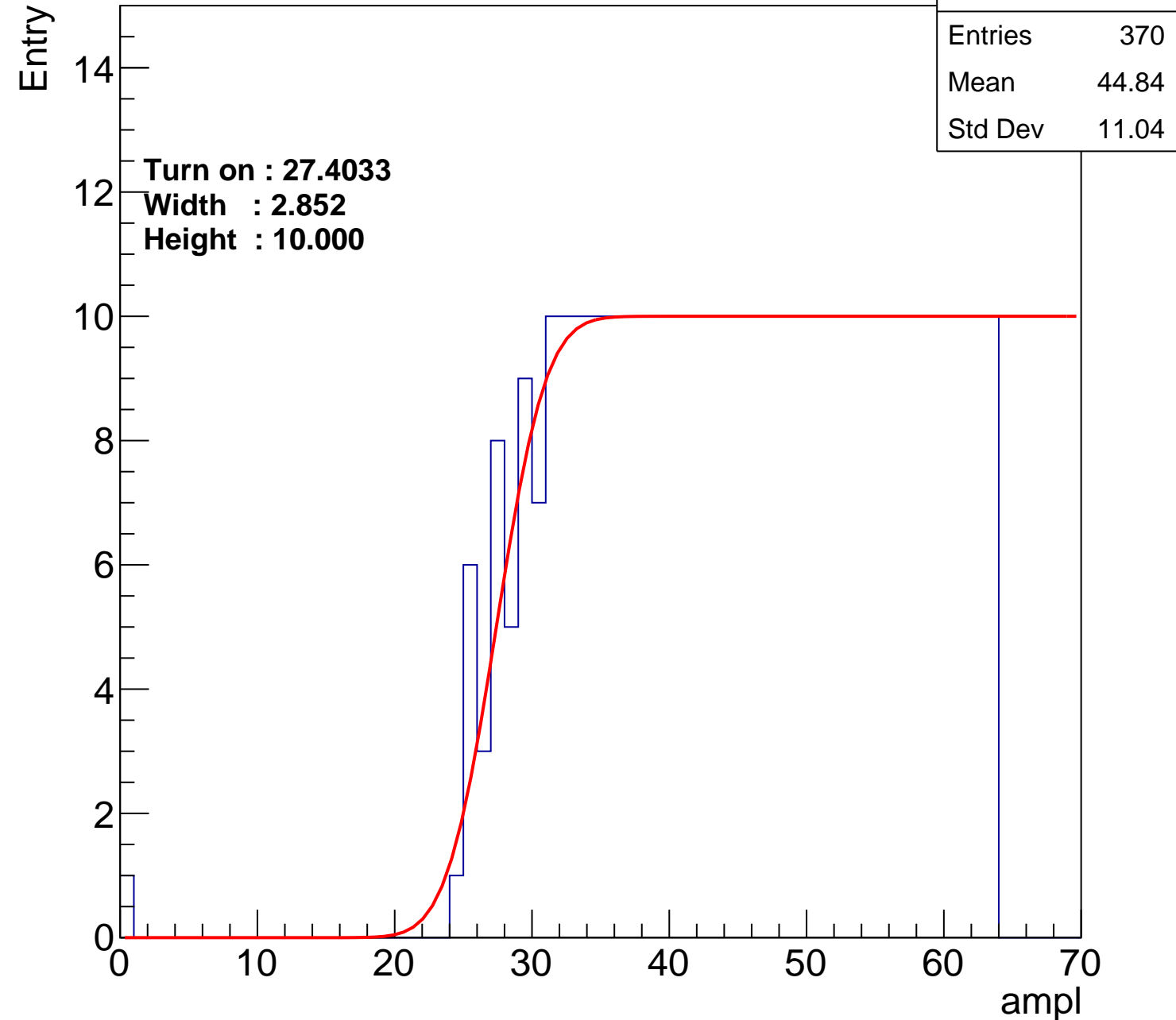
Width : 2.852

Height : 10.000

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch60

calib_packv5_042523_0143.root, FC#4, port A2

Entries	369
Mean	44.81
Std Dev	11.23

Turn on : 27.5948

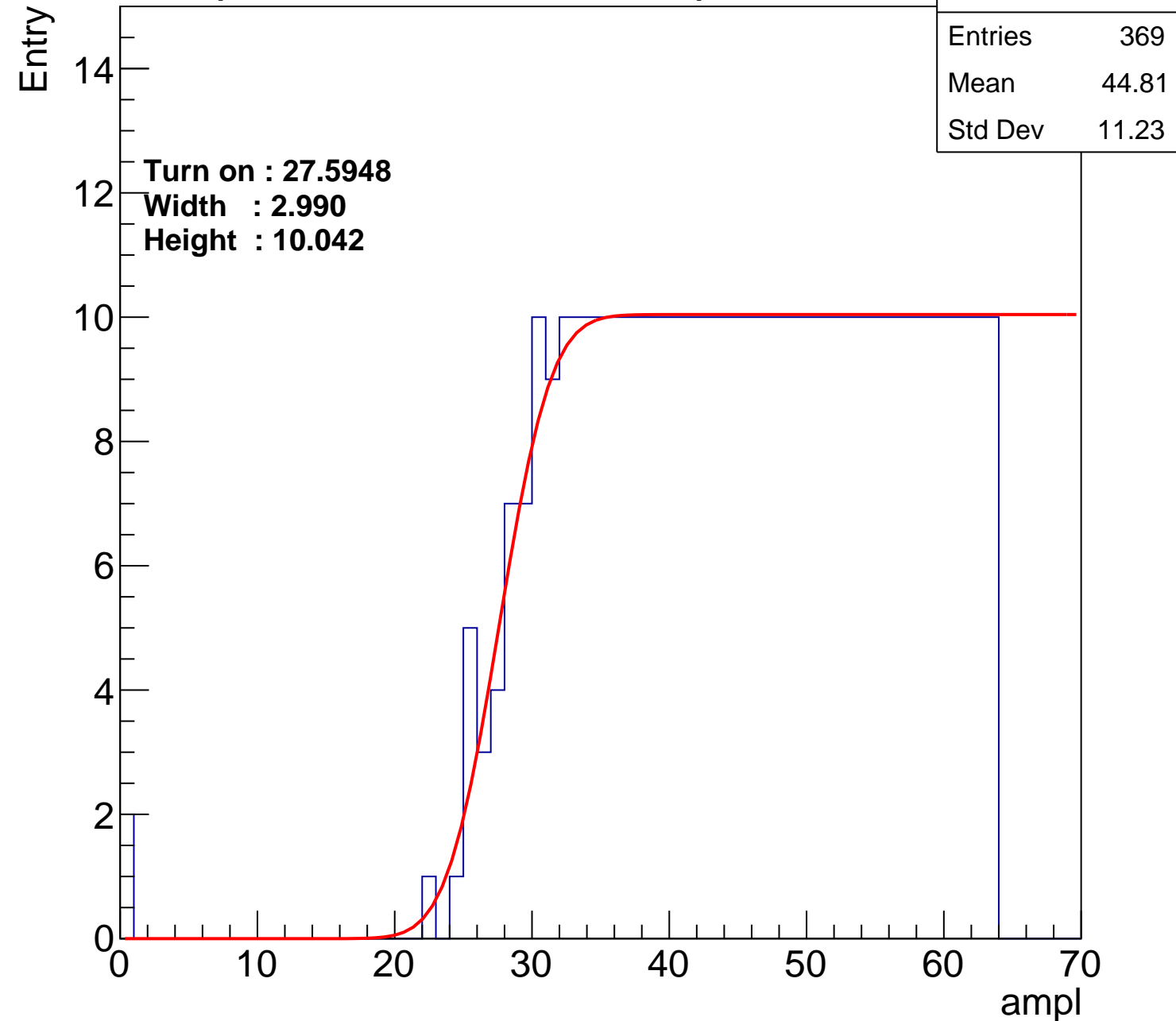
Width : 2.990

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch61

calib_packv5_042523_0143.root, FC#4, port A2

Entries	366
Mean	44.99
Std Dev	11.1

Turn on : 27.3853

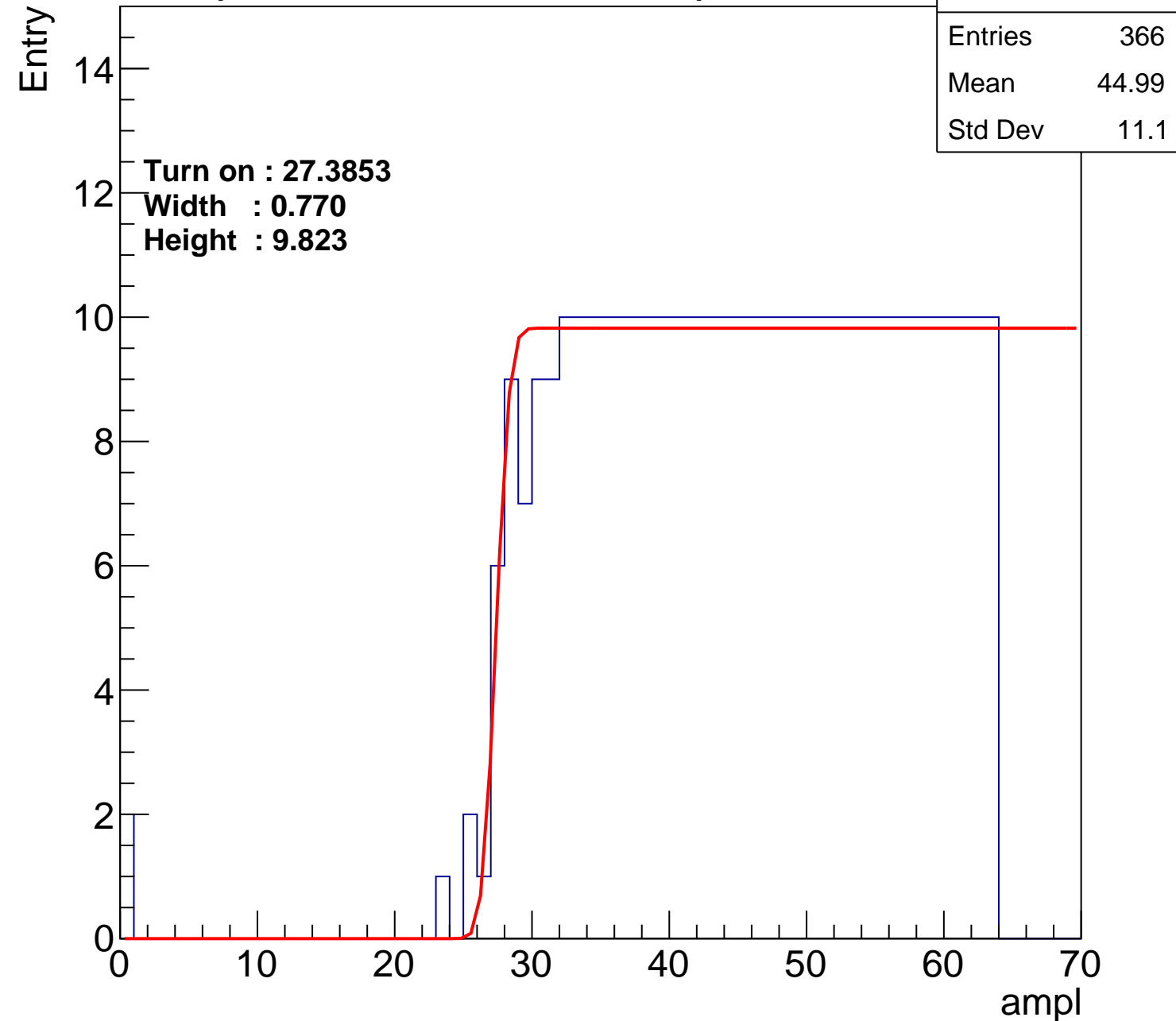
Width : 0.770

Height : 9.823

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch62

calib_packv5_042523_0143.root, FC#4, port A2

Entries	362
Mean	45.22
Std Dev	10.84

Turn on : 27.3077

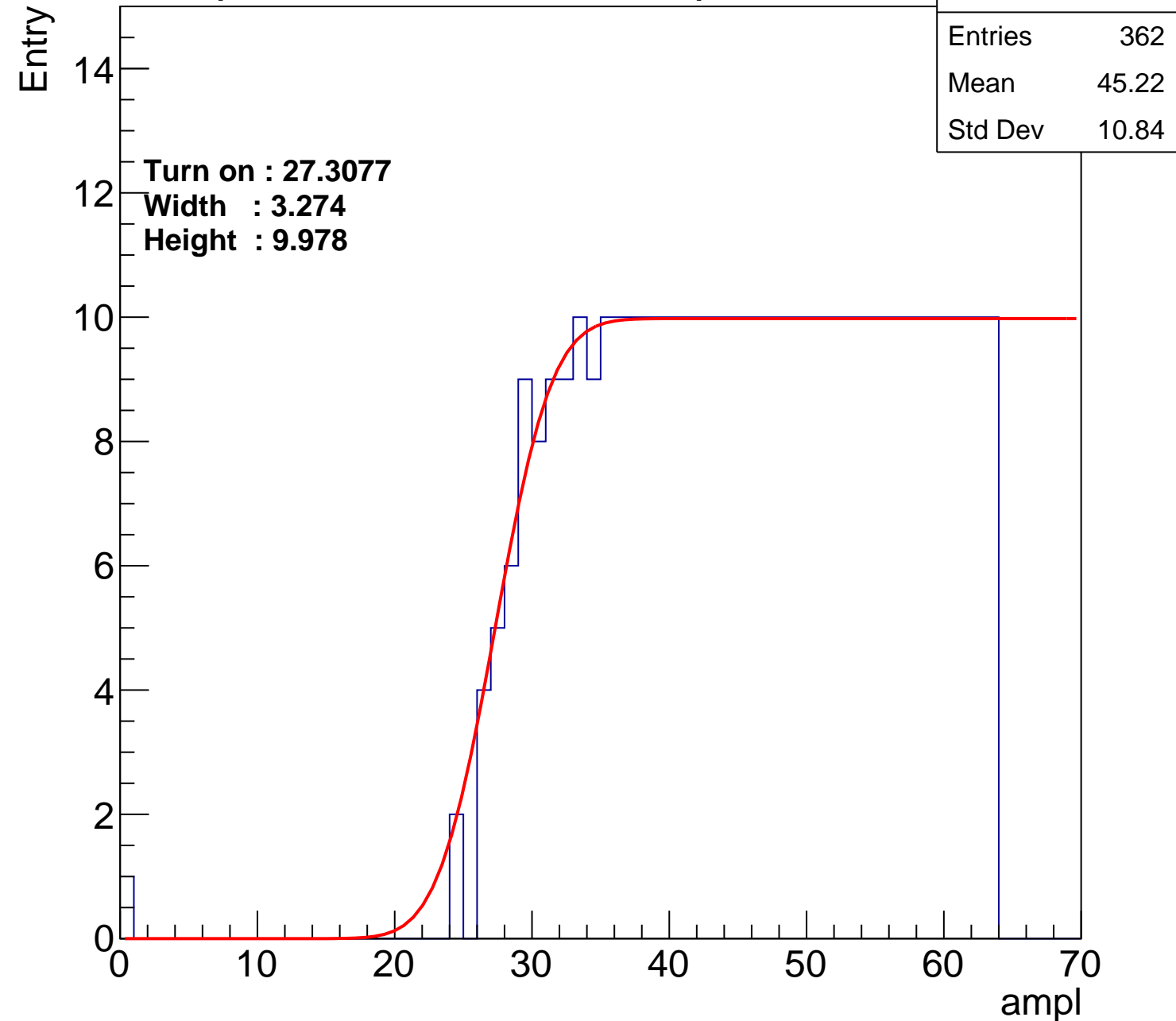
Width : 3.274

Height : 9.978

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch63

calib_packv5_042523_0143.root, FC#4, port A2

Entries	362
Mean	45.25
Std Dev	10.81

Turn on : 28.2429

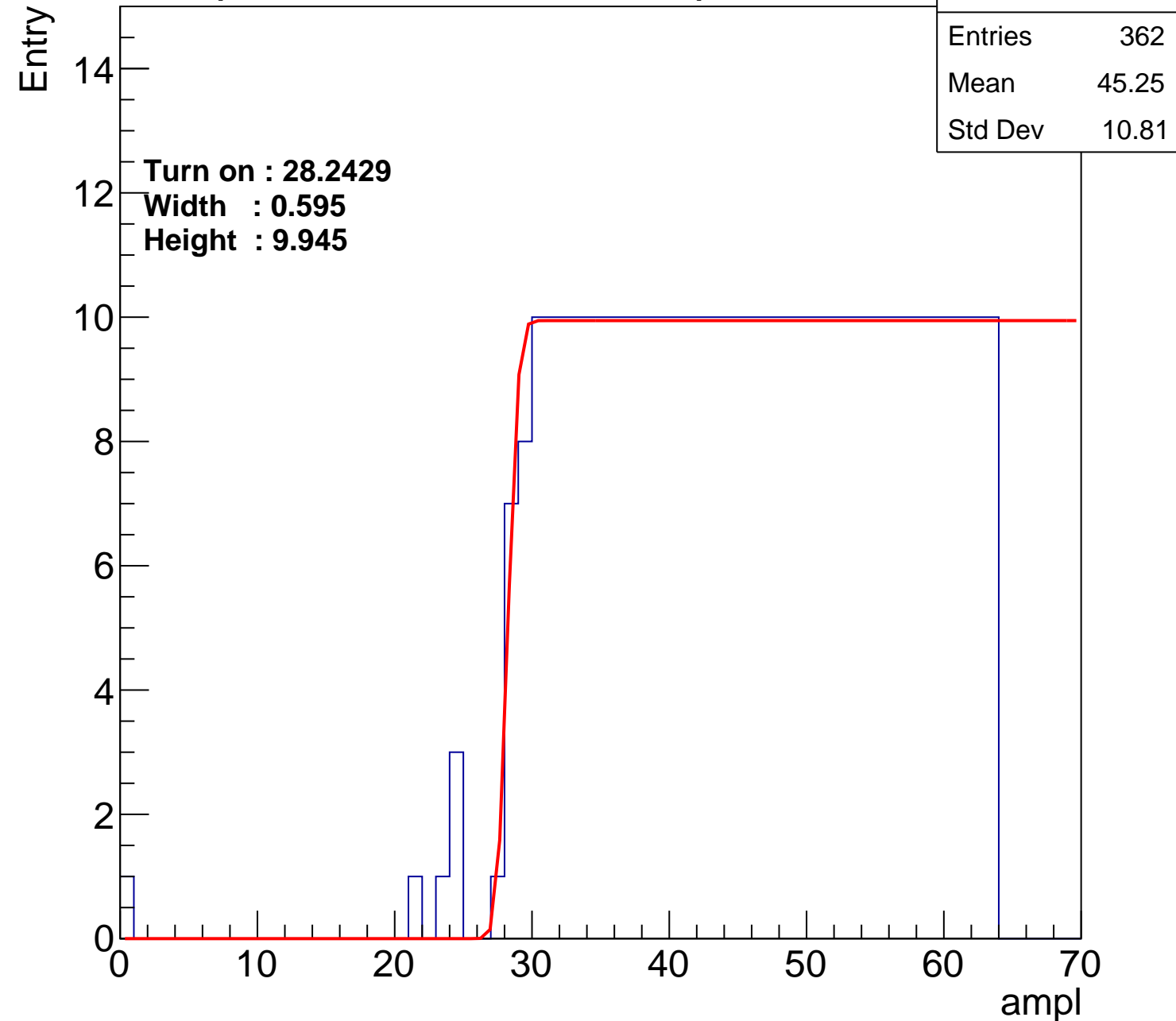
Width : 0.595

Height : 9.945

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch64

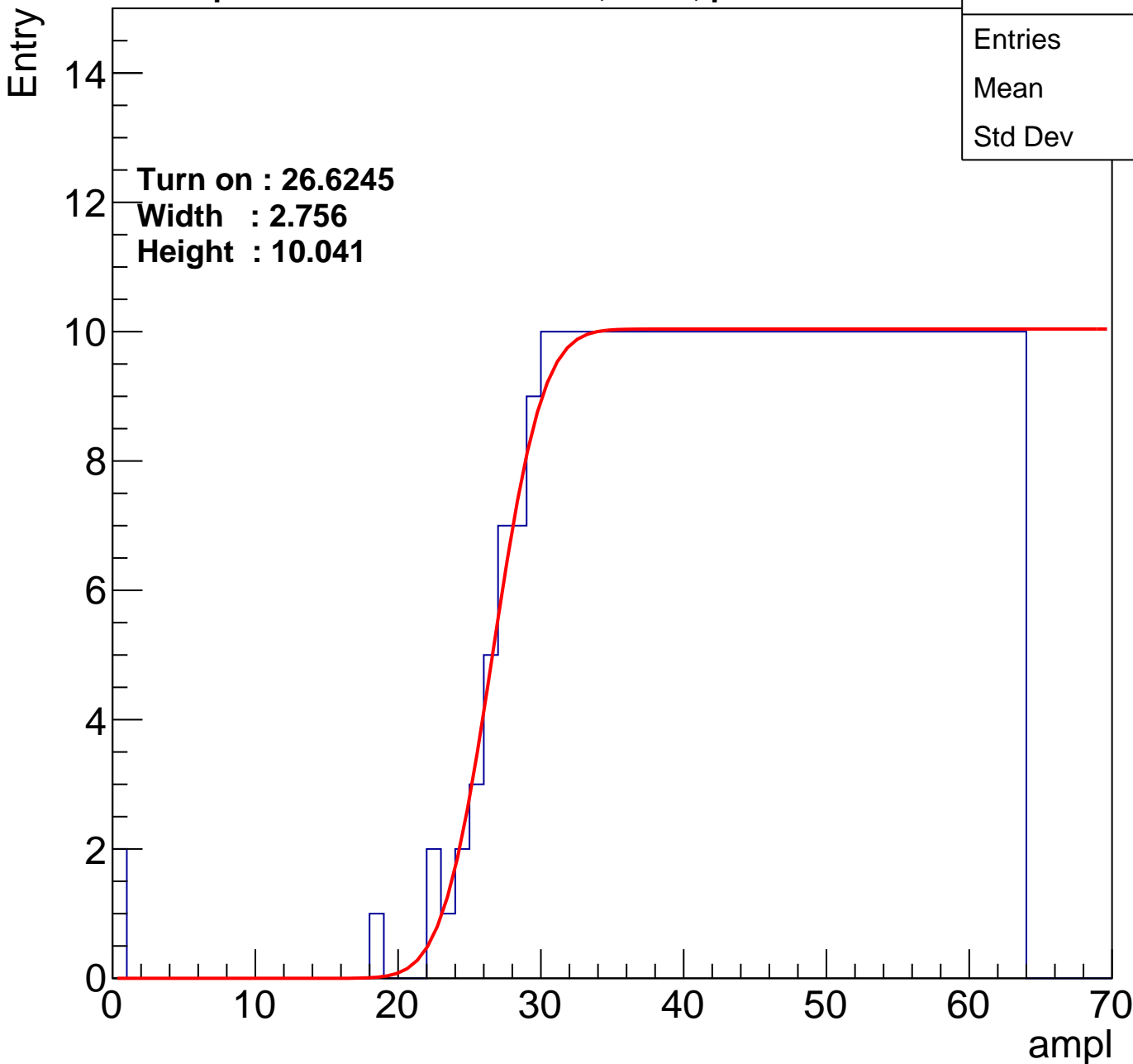
calib_packv5_042523_0143.root, FC#4, port A2

Entries	379
Mean	44.31
Std Dev	11.5

Turn on : 26.6245

Width : 2.756

Height : 10.041



B1L100S, U8-ch65

calib_packv5_042523_0143.root, FC#4, port A2

Entries	372
Mean	44.7
Std Dev	11.15

Turn on : 26.6240

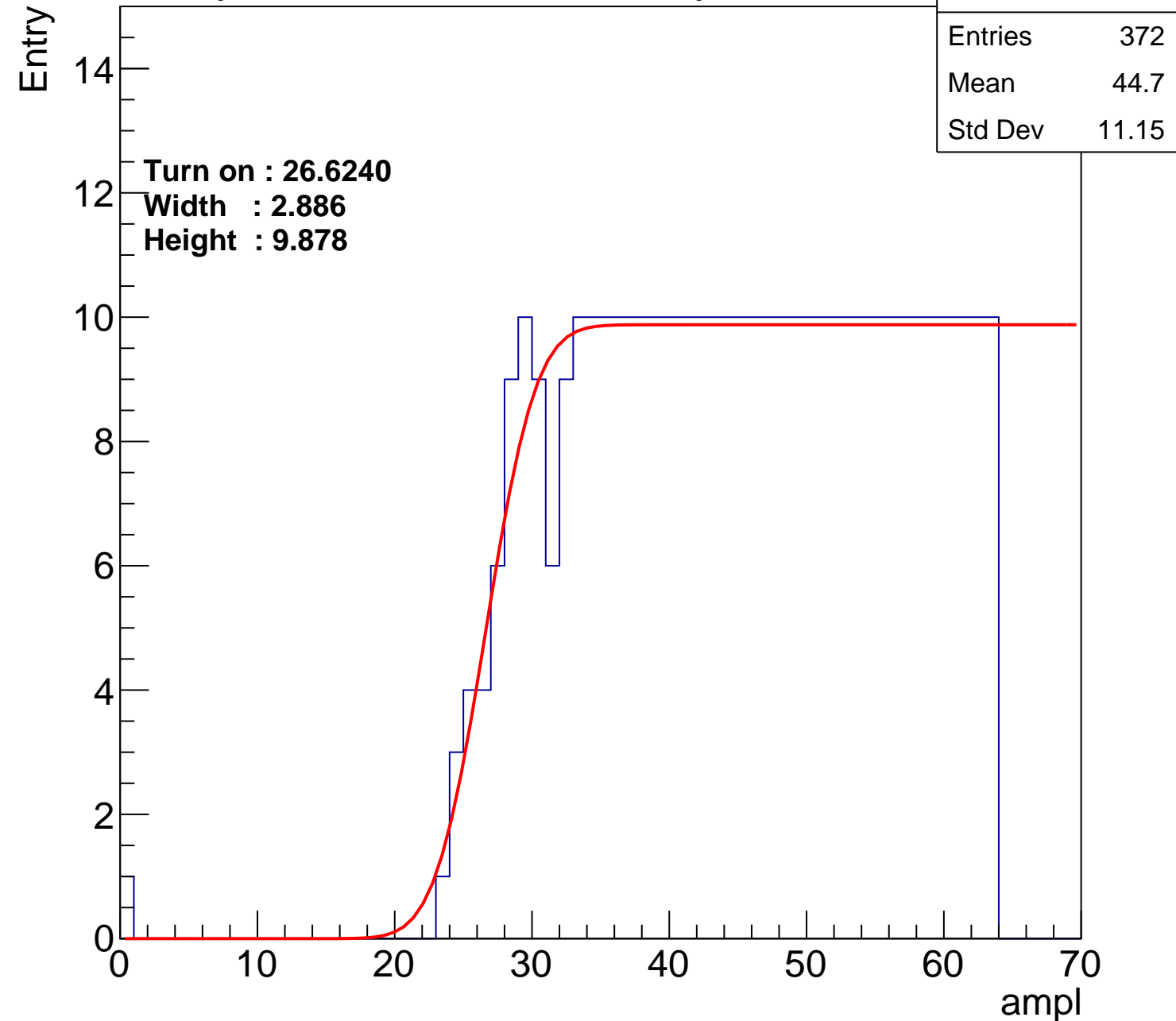
Width : 2.886

Height : 9.878

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch66

calib_packv5_042523_0143.root, FC#4, port A2

Entries	376
Mean	44.39
Std Dev	11.61

Turn on : 26.5900

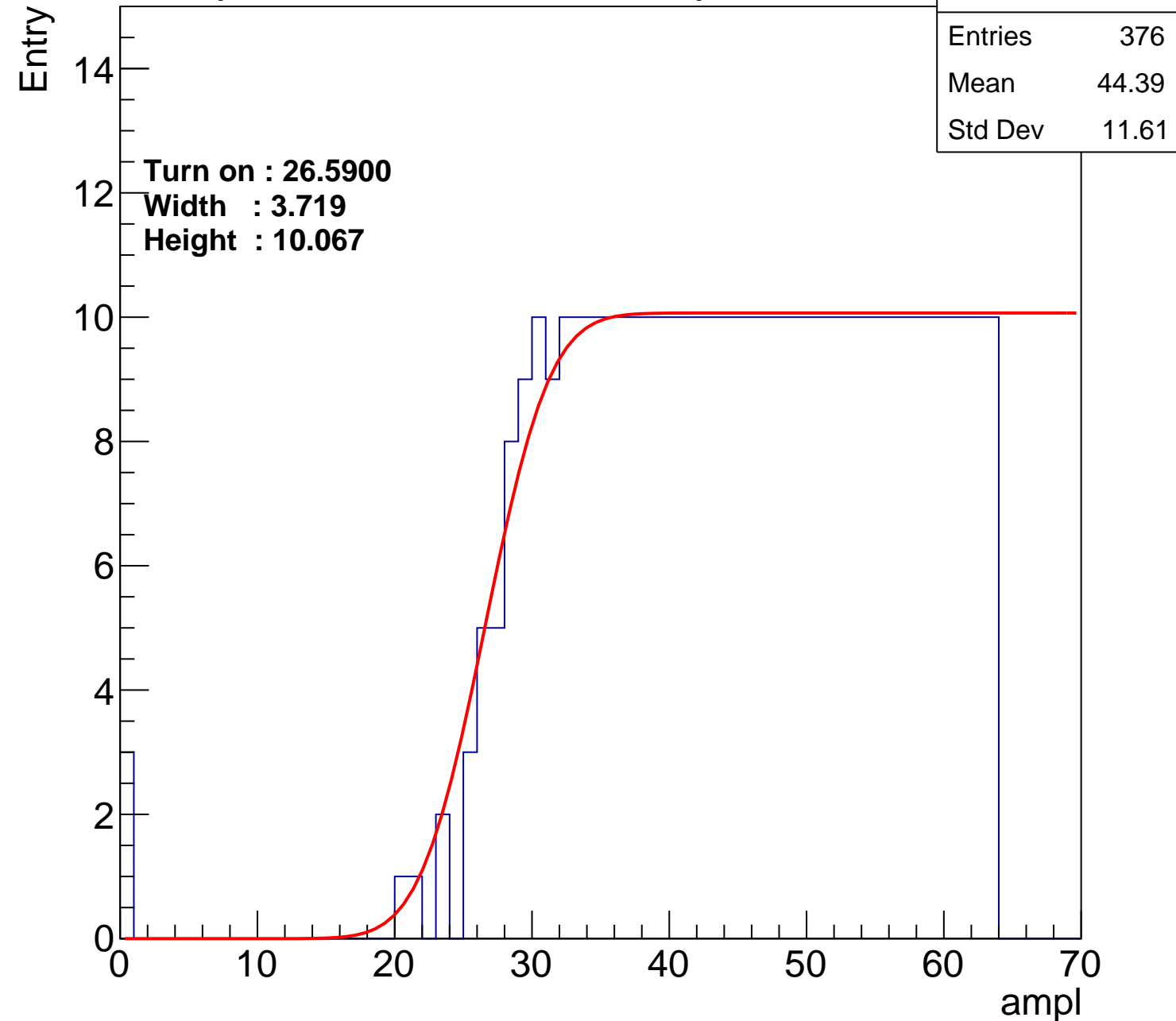
Width : 3.719

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch67

calib_packv5_042523_0143.root, FC#4, port A2

Entries	363
Mean	45.23
Std Dev	10.78

Turn on : 27.9045

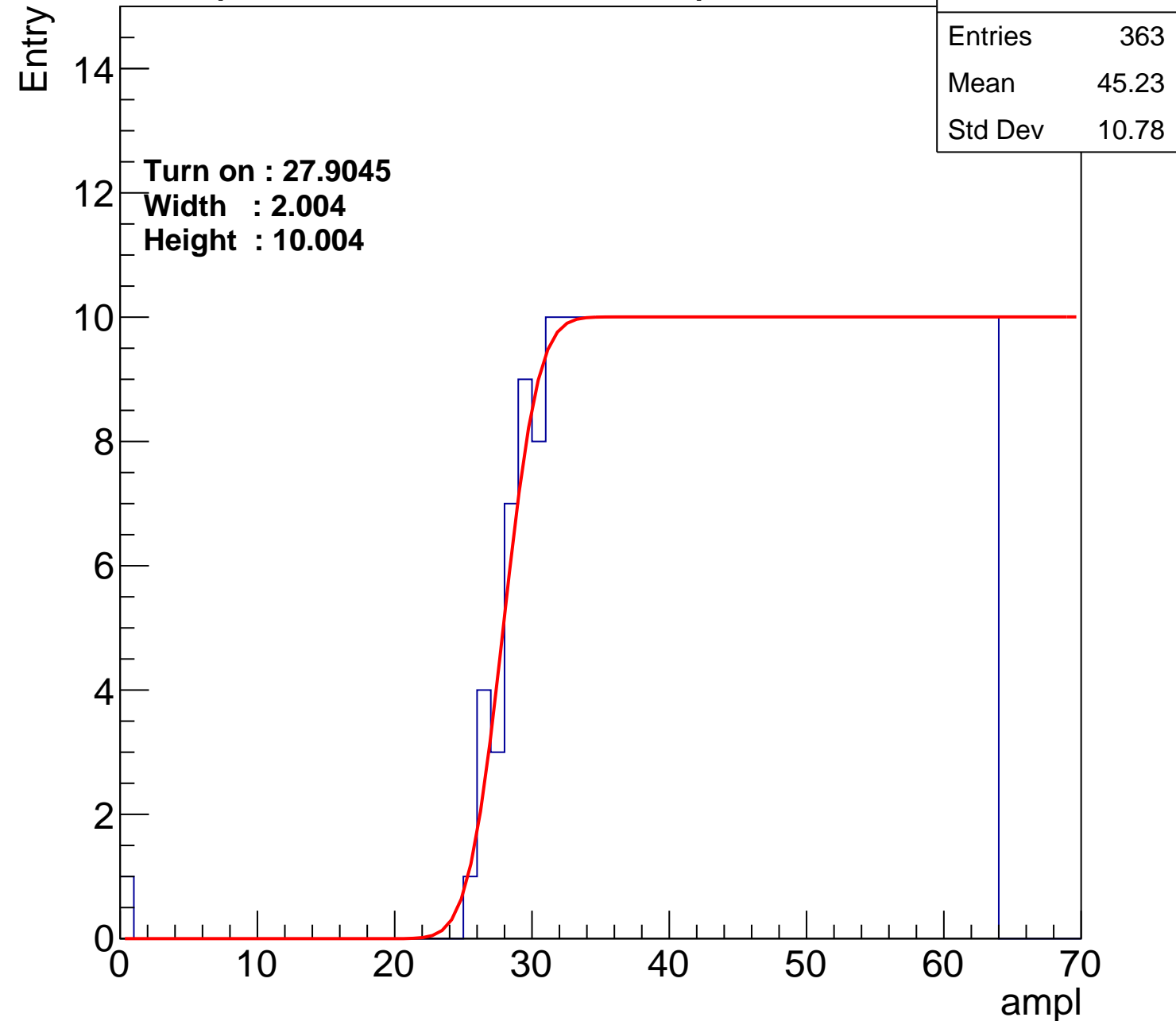
Width : 2.004

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch68

calib_packv5_042523_0143.root, FC#4, port A2

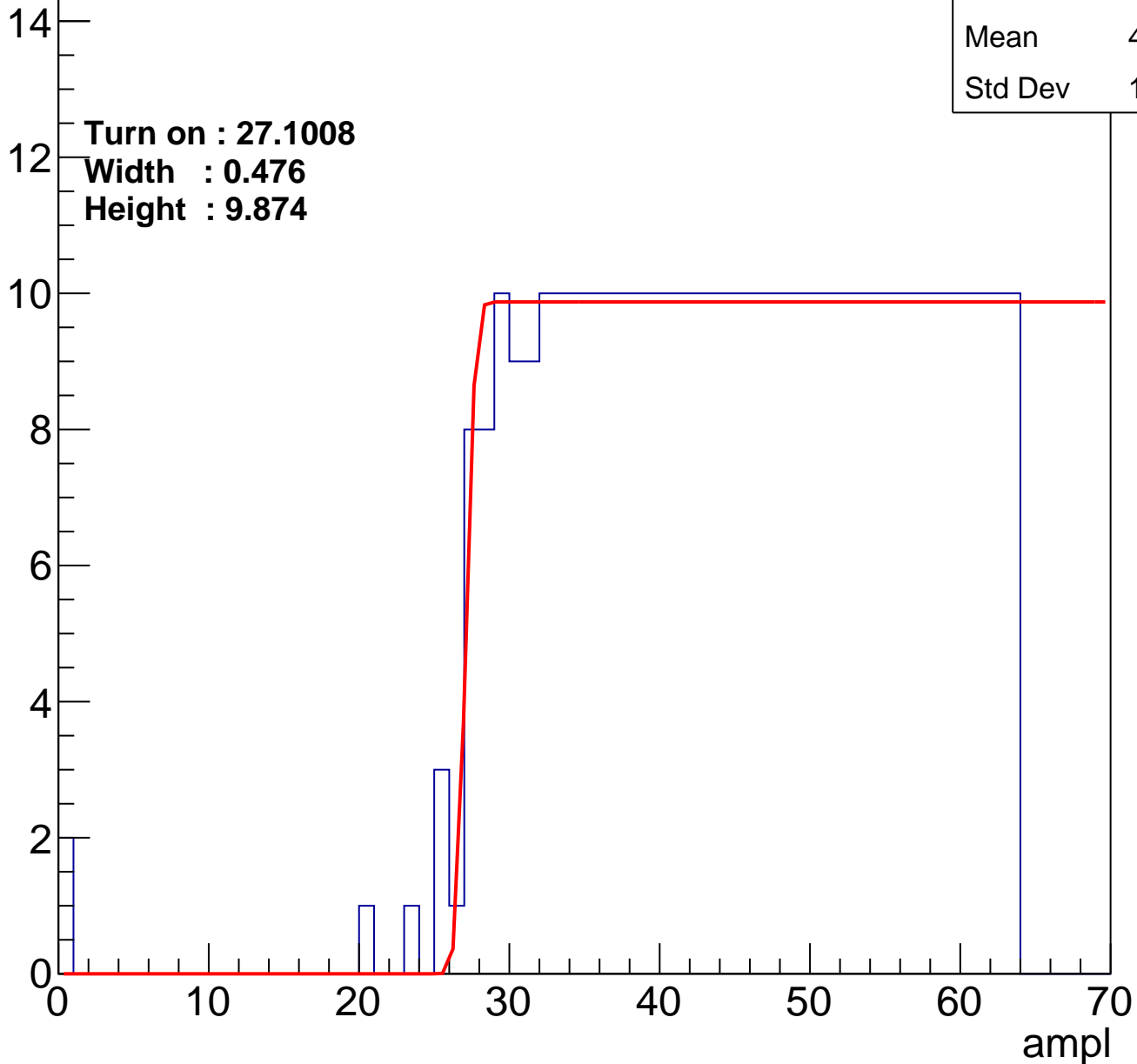
Entries	372
Mean	44.69
Std Dev	11.27

Turn on : 27.1008

Width : 0.476

Height : 9.874

Entry



B1L100S, U8-ch69

calib_packv5_042523_0143.root, FC#4, port A2

Entries	351
Mean	45.58
Std Dev	11.06

Turn on : 29.2745

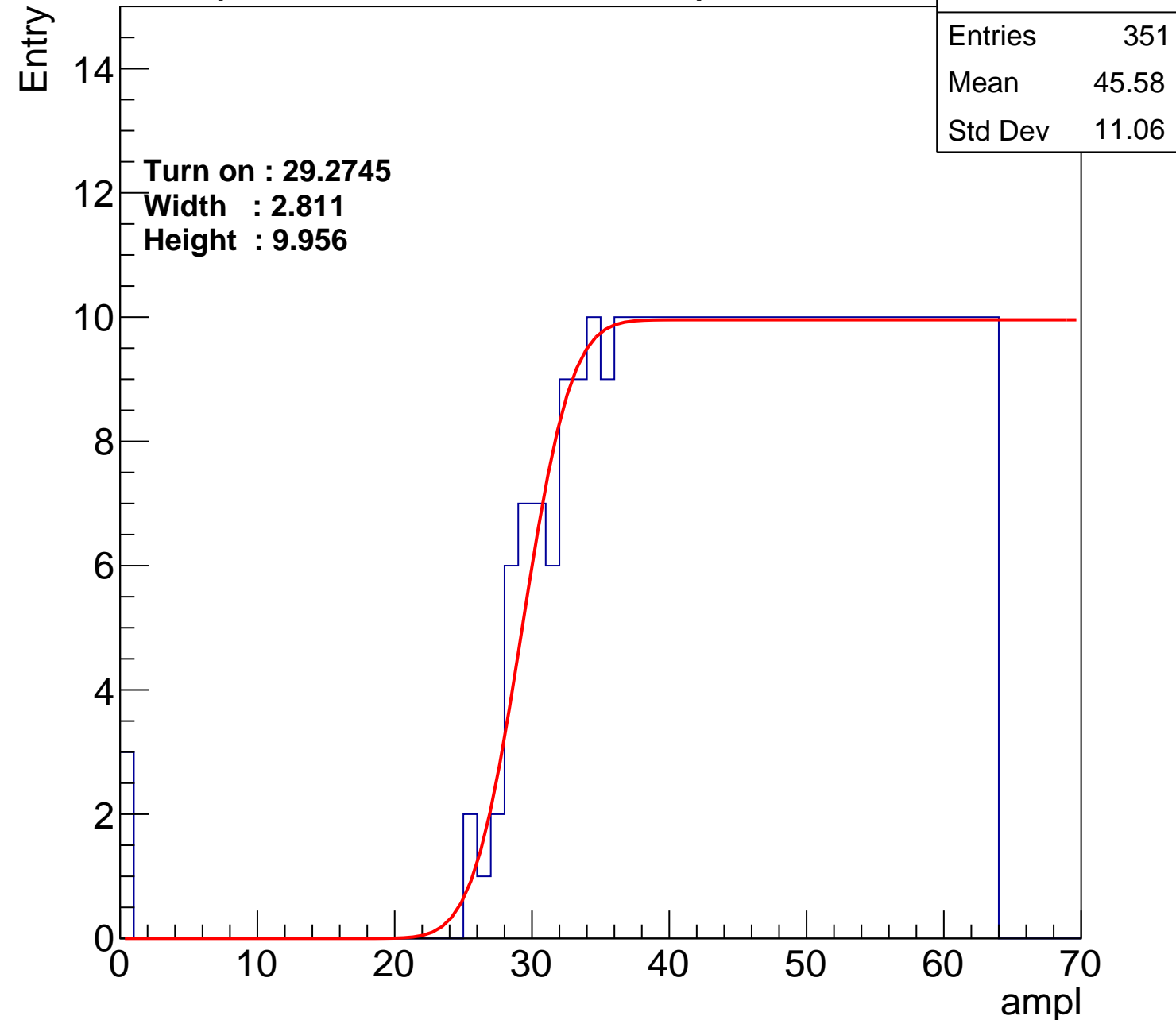
Width : 2.811

Height : 9.956

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch70

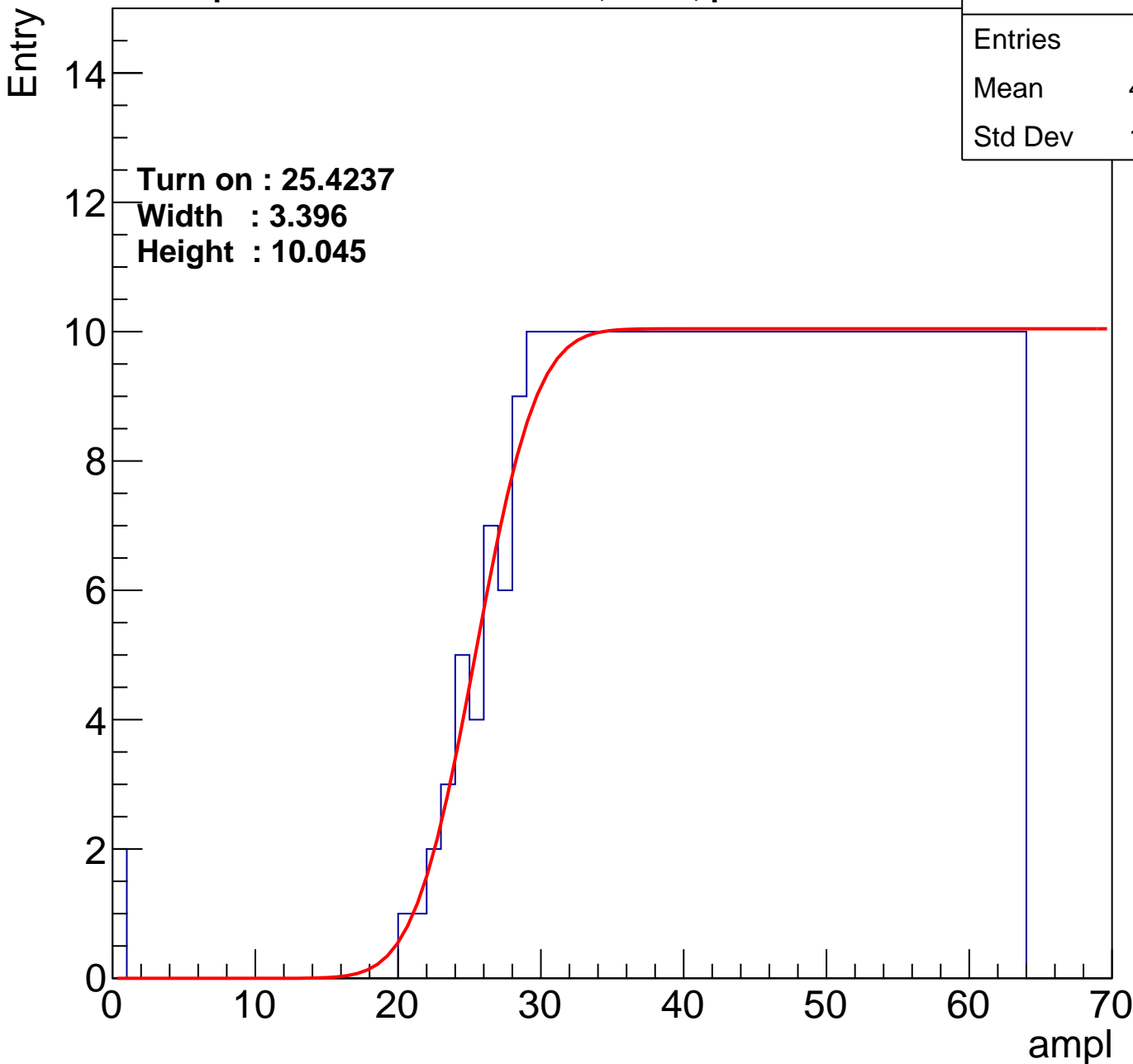
calib_packv5_042523_0143.root, FC#4, port A2

Entries	390
Mean	43.77
Std Dev	11.78

Turn on : 25.4237

Width : 3.396

Height : 10.045



B1L100S, U8-ch71

calib_packv5_042523_0143.root, FC#4, port A2

Entries	357
Mean	45.49
Std Dev	10.68

Turn on : 28.2511

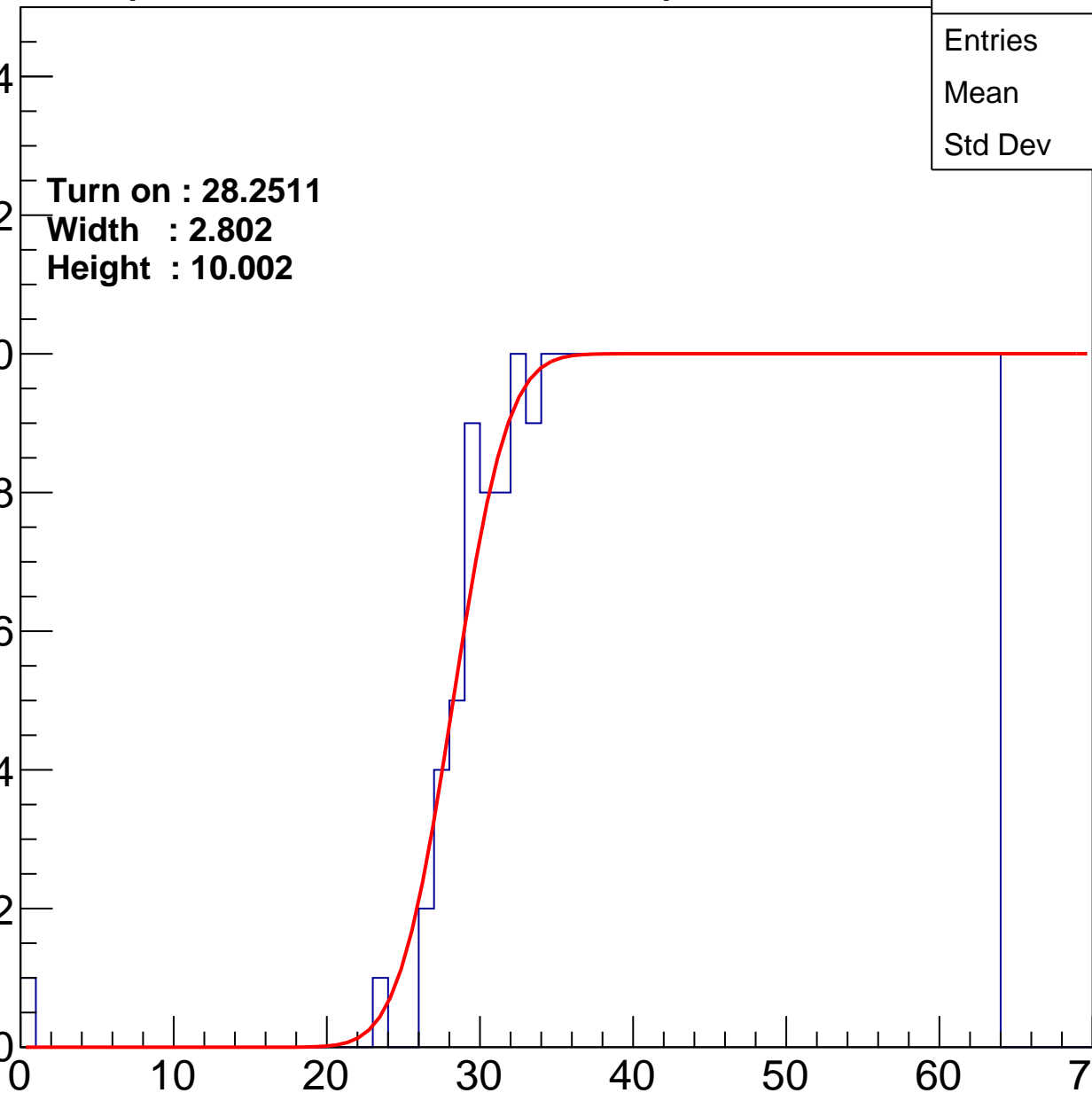
Width : 2.802

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch72

calib_packv5_042523_0143.root, FC#4, port A2

Entries	380
Mean	44.12
Std Dev	11.89

Turn on : 26.5557

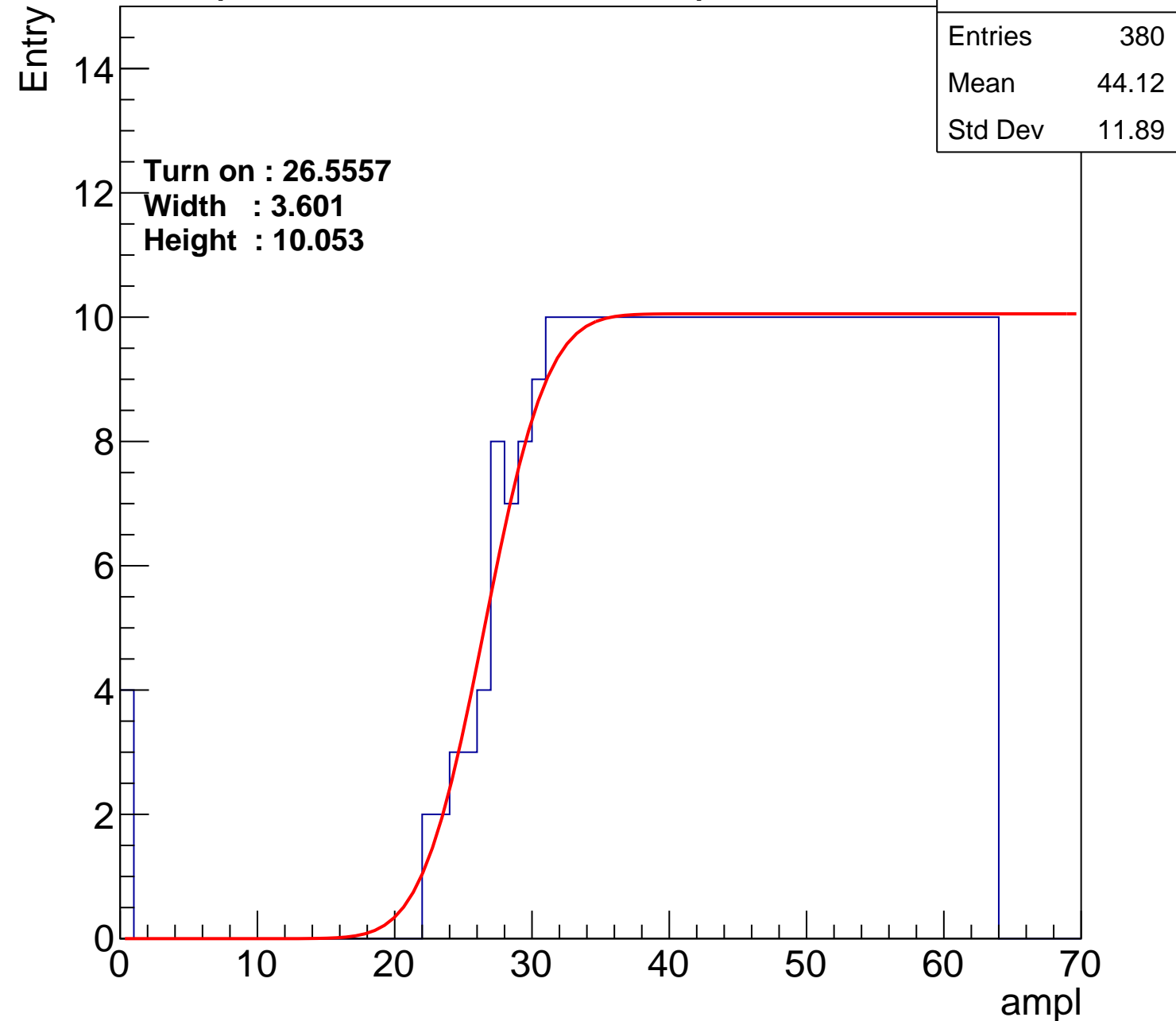
Width : 3.601

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch73

calib_packv5_042523_0143.root, FC#4, port A2

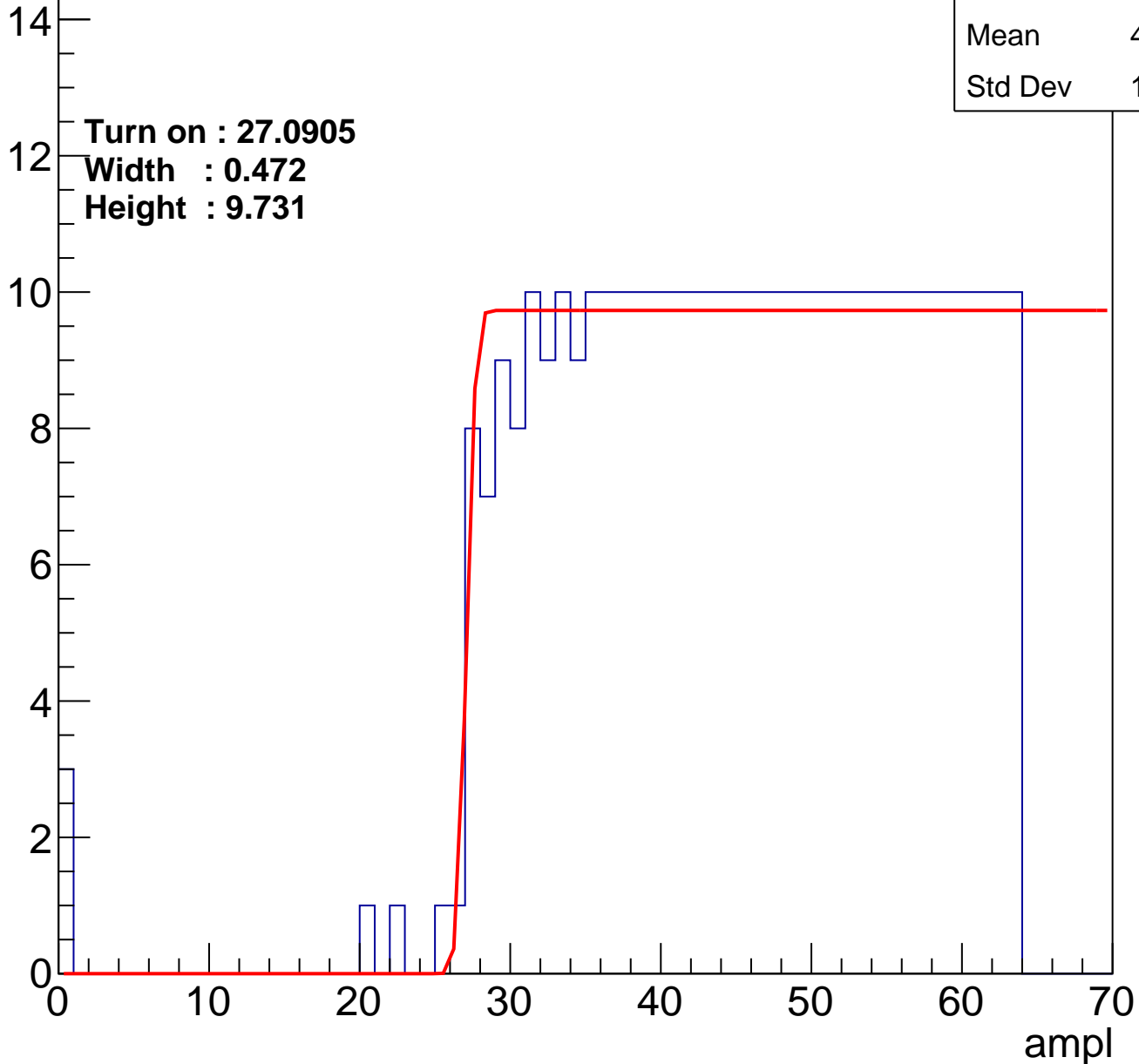
Entries	367
Mean	44.82
Std Dev	11.39

Turn on : 27.0905

Width : 0.472

Height : 9.731

Entry



B1L100S, U8-ch74

calib_packv5_042523_0143.root, FC#4, port A2

Entries	379
Mean	44.39
Std Dev	11.29

Turn on : 26.2442

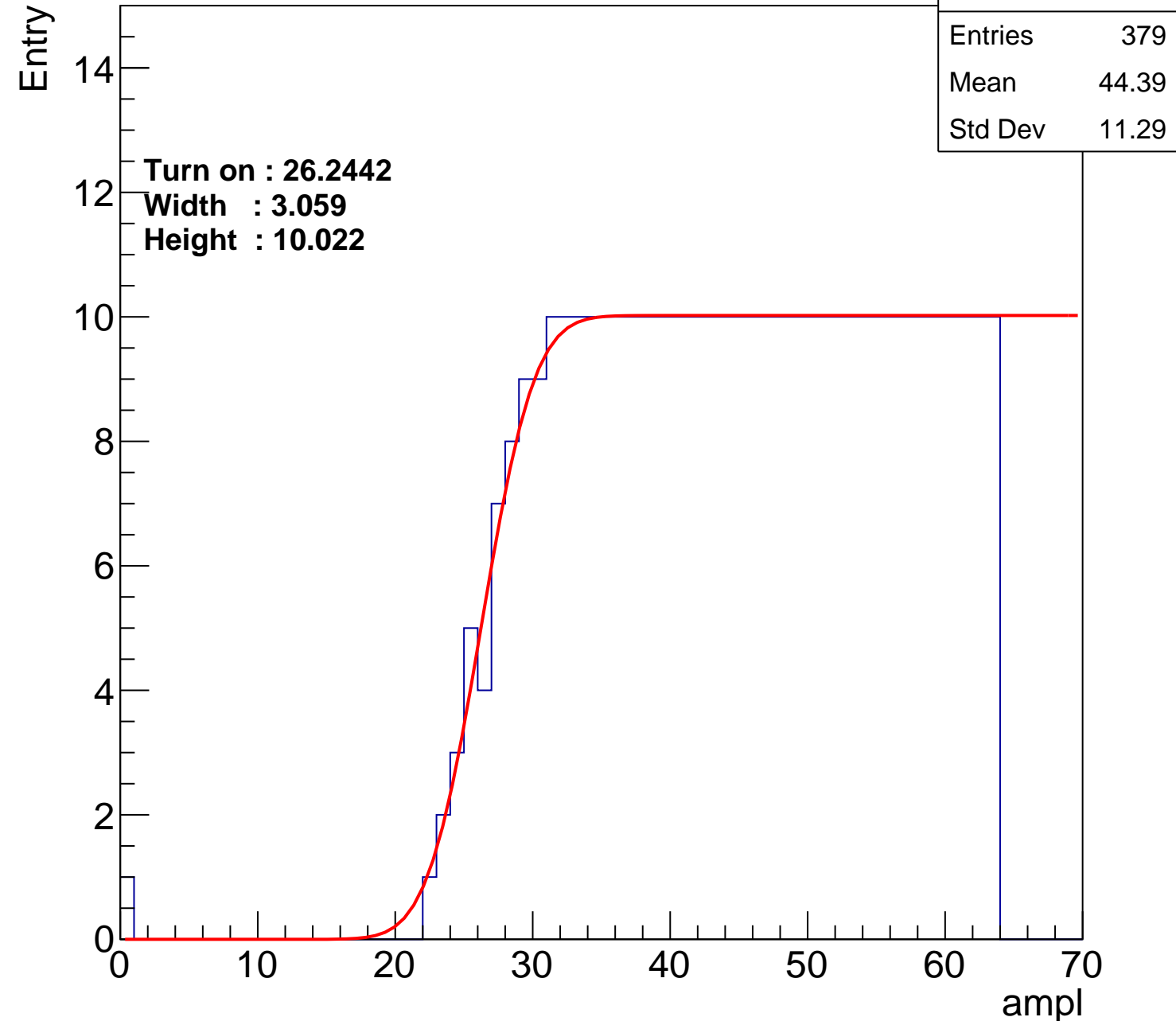
Width : 3.059

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch75

calib_packv5_042523_0143.root, FC#4, port A2

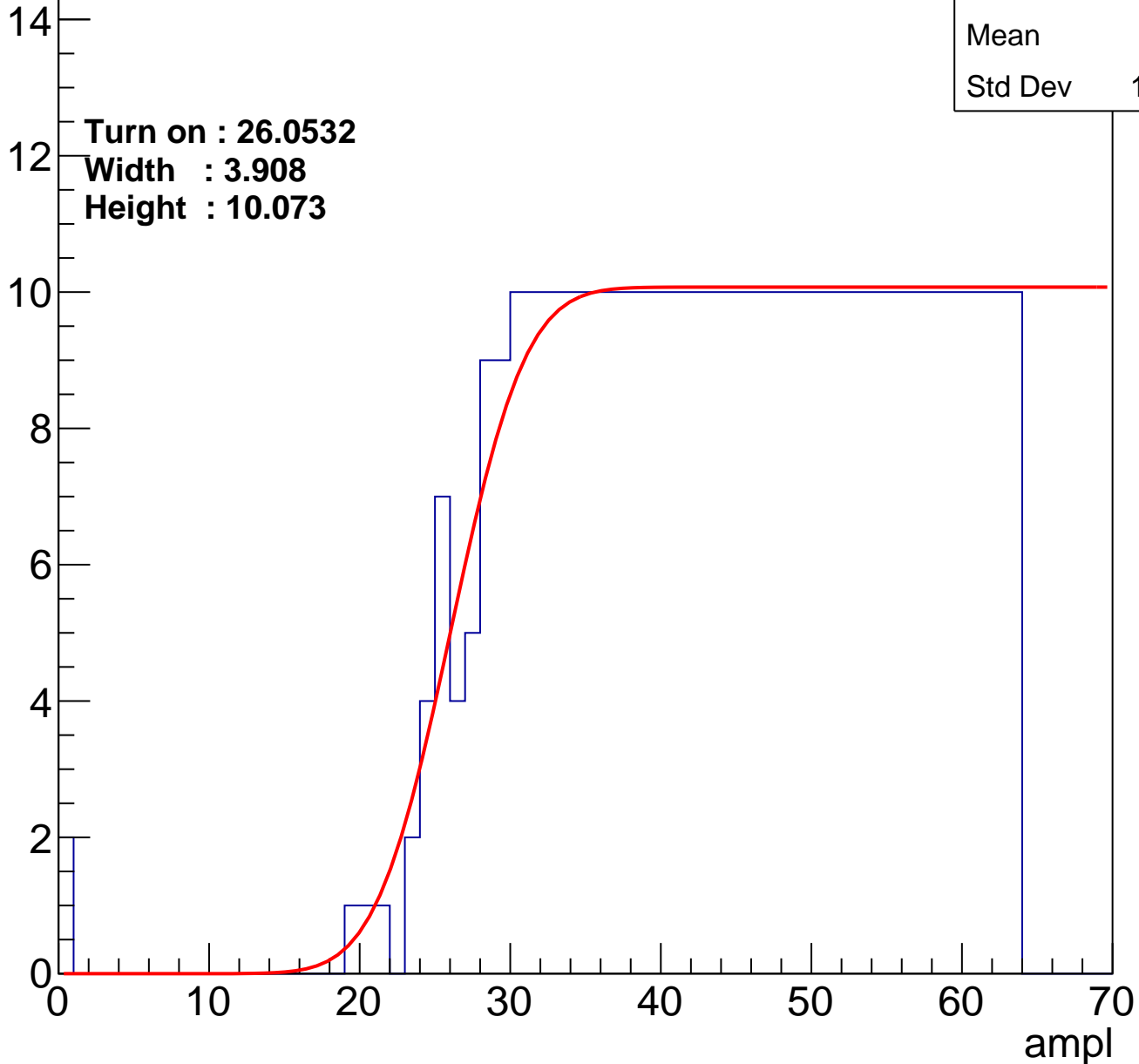
Entries	385
Mean	44
Std Dev	11.68

Turn on : 26.0532

Width : 3.908

Height : 10.073

Entry



B1L100S, U8-ch76

calib_packv5_042523_0143.root, FC#4, port A2

Entries	361
Mean	45.28
Std Dev	10.81

Turn on : 28.3004

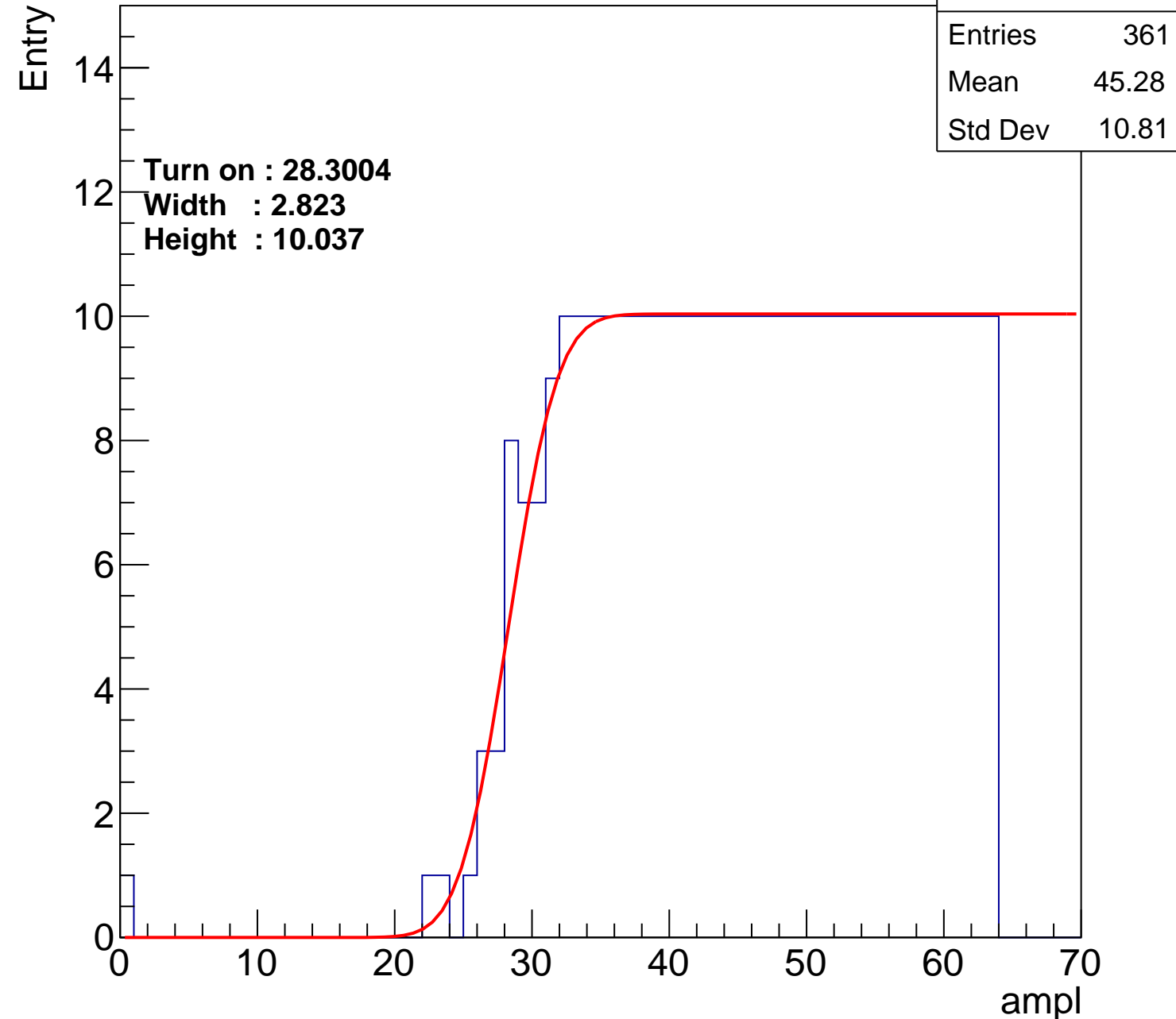
Width : 2.823

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch77

calib_packv5_042523_0143.root, FC#4, port A2

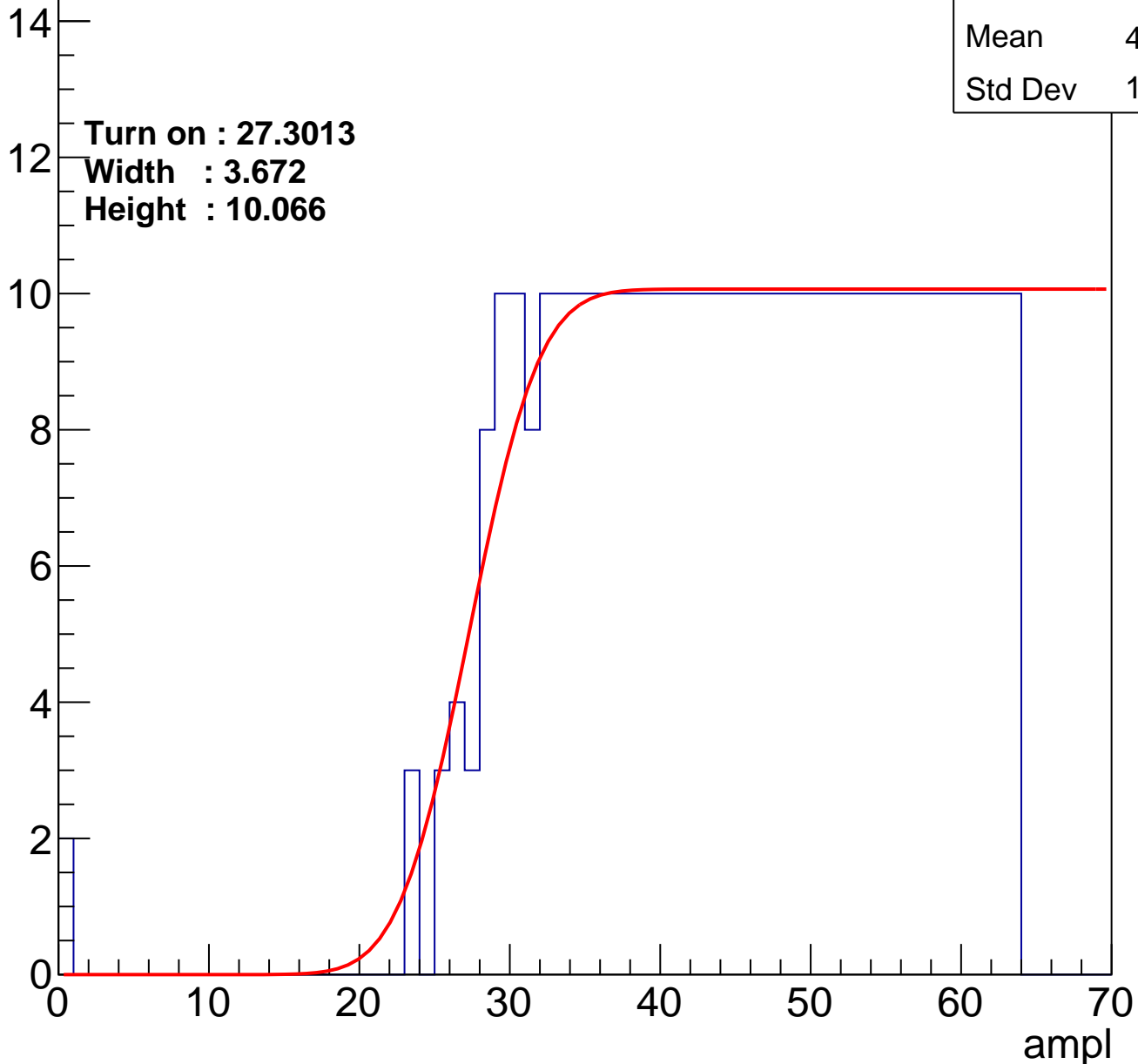
Entries	371
Mean	44.72
Std Dev	11.26

Turn on : 27.3013

Width : 3.672

Height : 10.066

Entry



B1L100S, U8-ch78

calib_packv5_042523_0143.root, FC#4, port A2

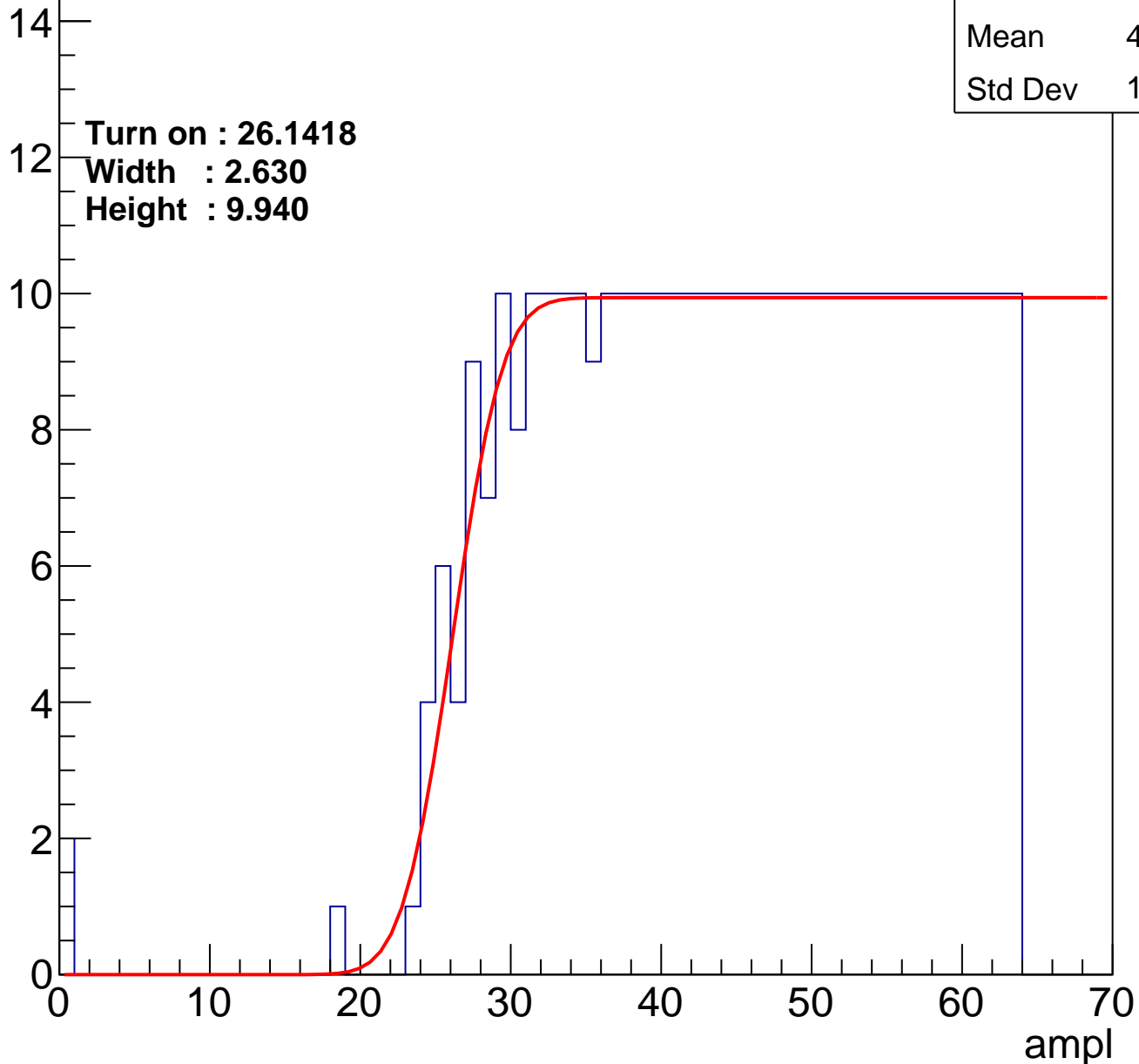
Entries	381
Mean	44.19
Std Dev	11.58

Turn on : 26.1418

Width : 2.630

Height : 9.940

Entry



B1L100S, U8-ch79

calib_packv5_042523_0143.root, FC#4, port A2

Entries	363
Mean	45.02
Std Dev	11.29

Turn on : 28.3642

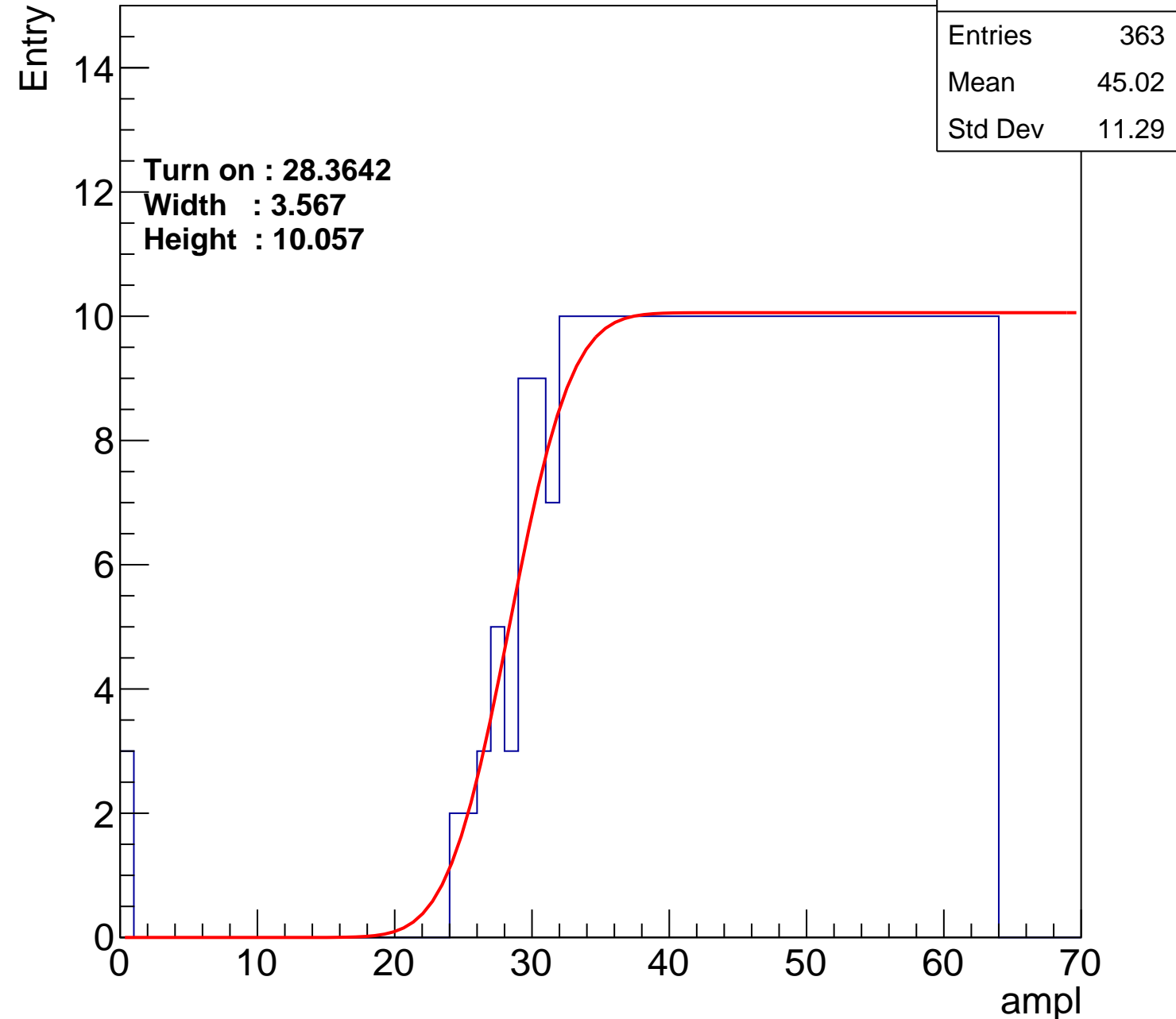
Width : 3.567

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch80

calib_packv5_042523_0143.root, FC#4, port A2

Entries	386
Mean	43.97
Std Dev	11.67

Turn on : 25.6172

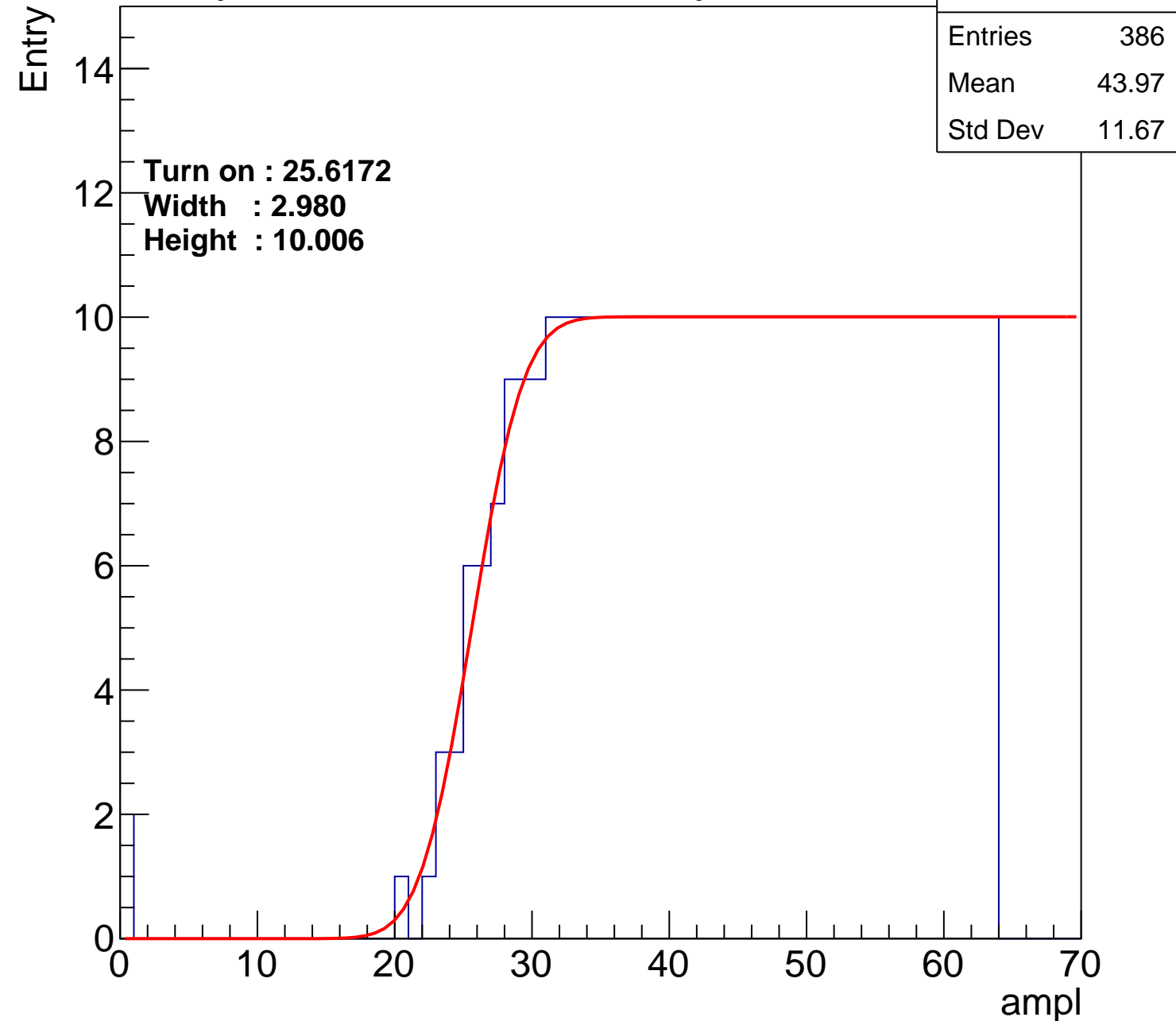
Width : 2.980

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch81

calib_packv5_042523_0143.root, FC#4, port A2

Entries	364
Mean	44.97
Std Dev	11.33

Turn on : 28.3266

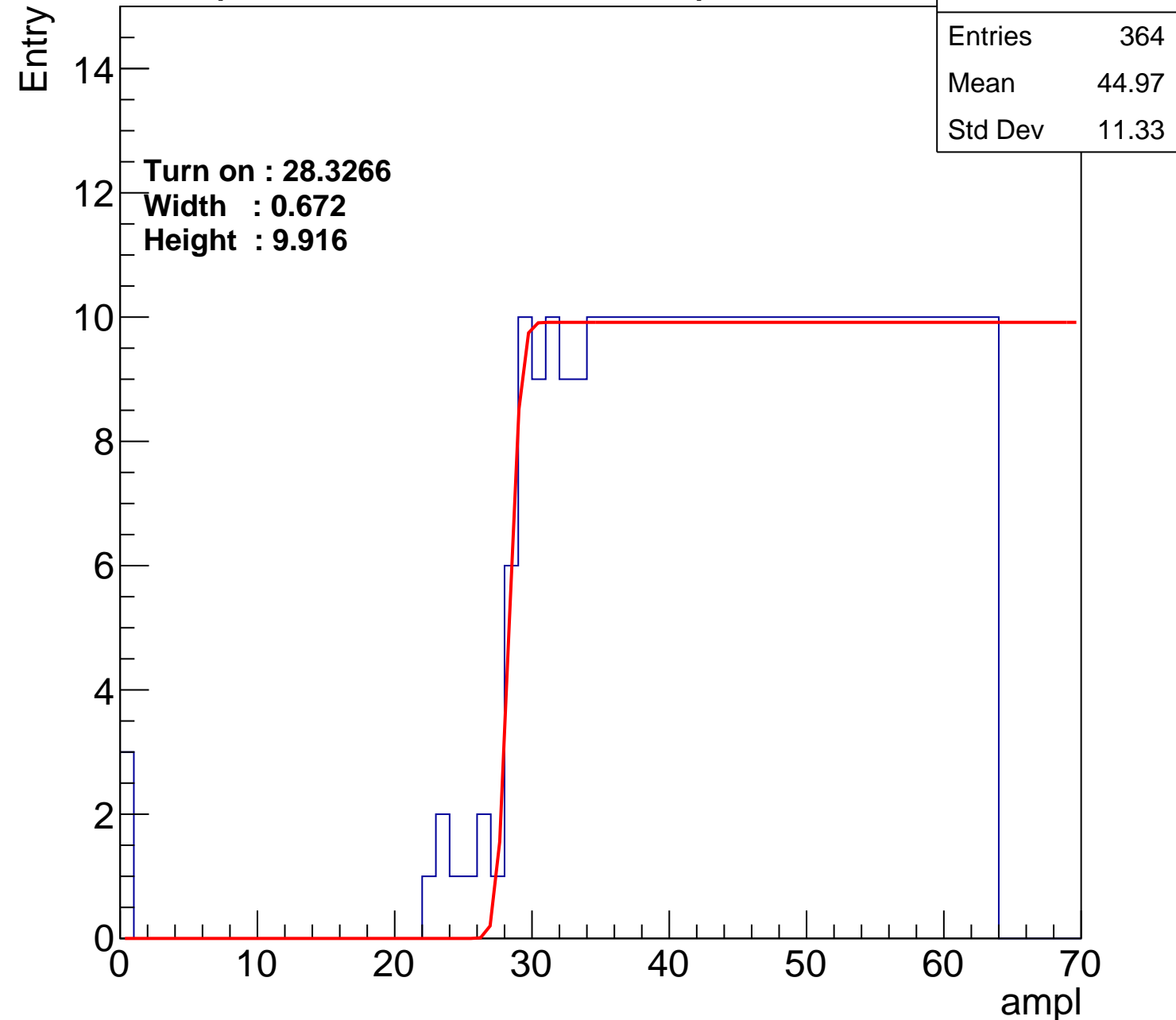
Width : 0.672

Height : 9.916

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch82

calib_packv5_042523_0143.root, FC#4, port A2

Entries	378
Mean	44.37
Std Dev	11.45

Turn on : 26.3725

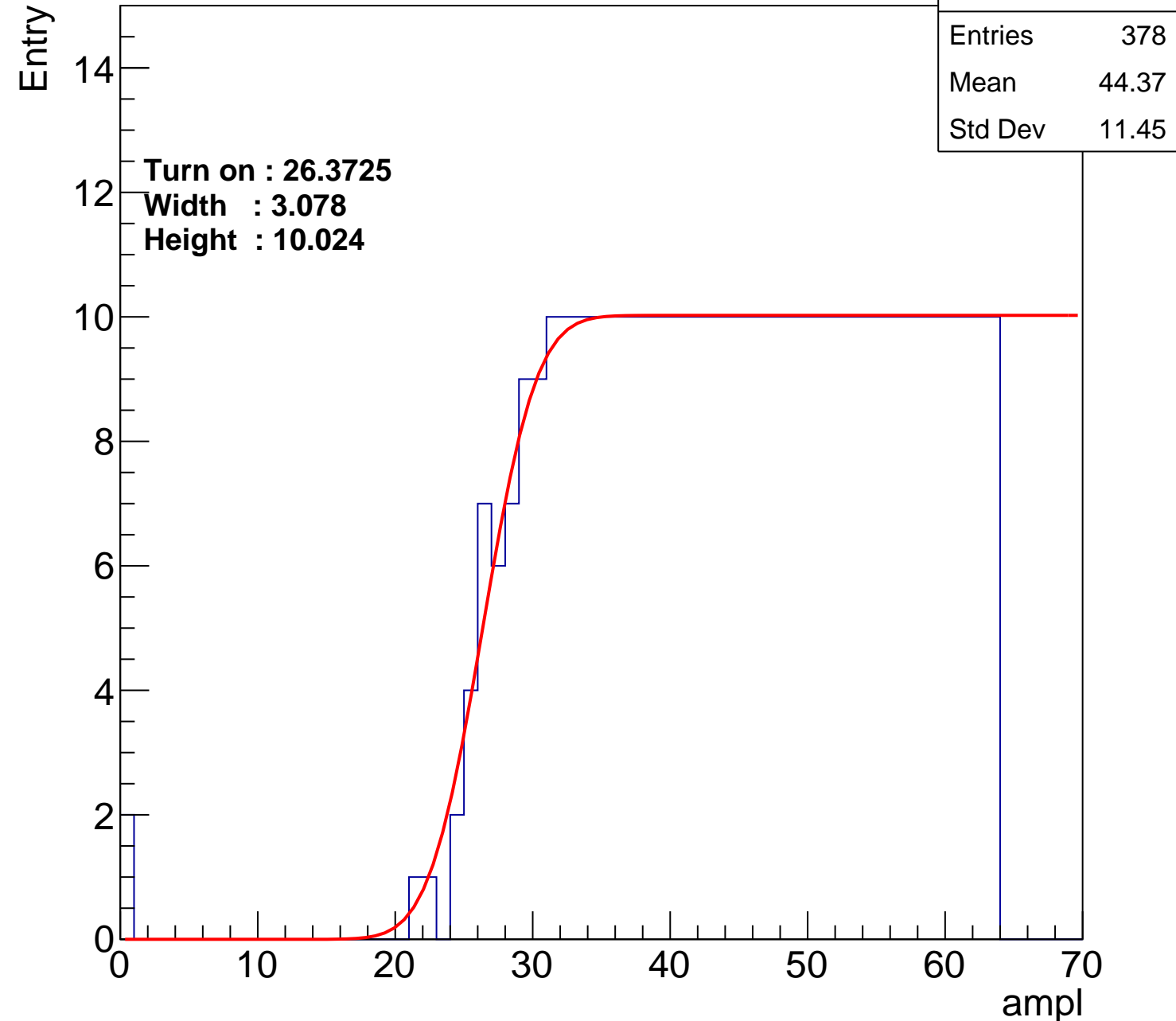
Width : 3.078

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch83

calib_packv5_042523_0143.root, FC#4, port A2

Entries	370
Mean	44.62
Std Dev	11.54

Turn on : 27.2775

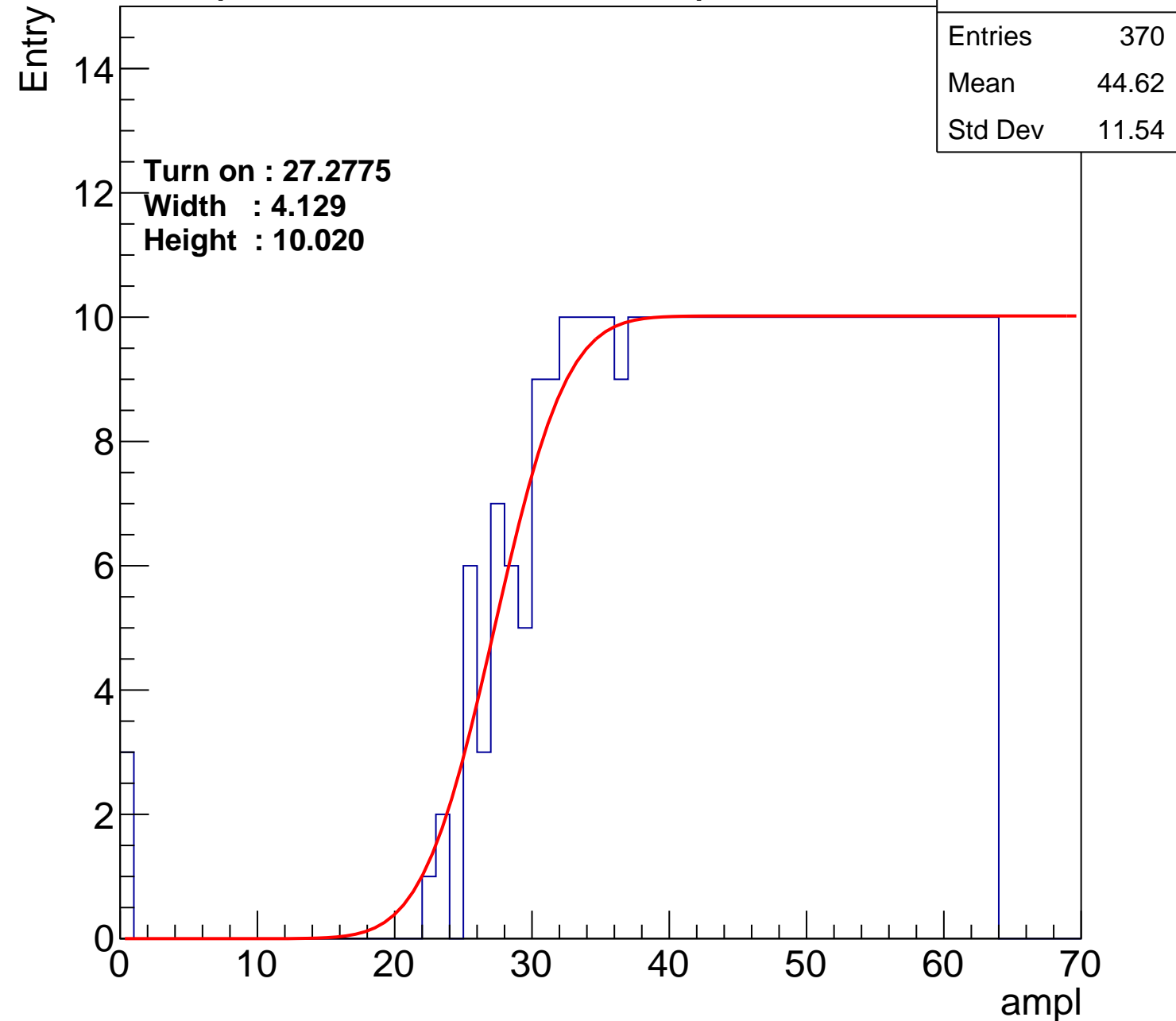
Width : 4.129

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch84

calib_packv5_042523_0143.root, FC#4, port A2

Entries	376
Mean	44.46
Std Dev	11.41

Turn on : 26.4873

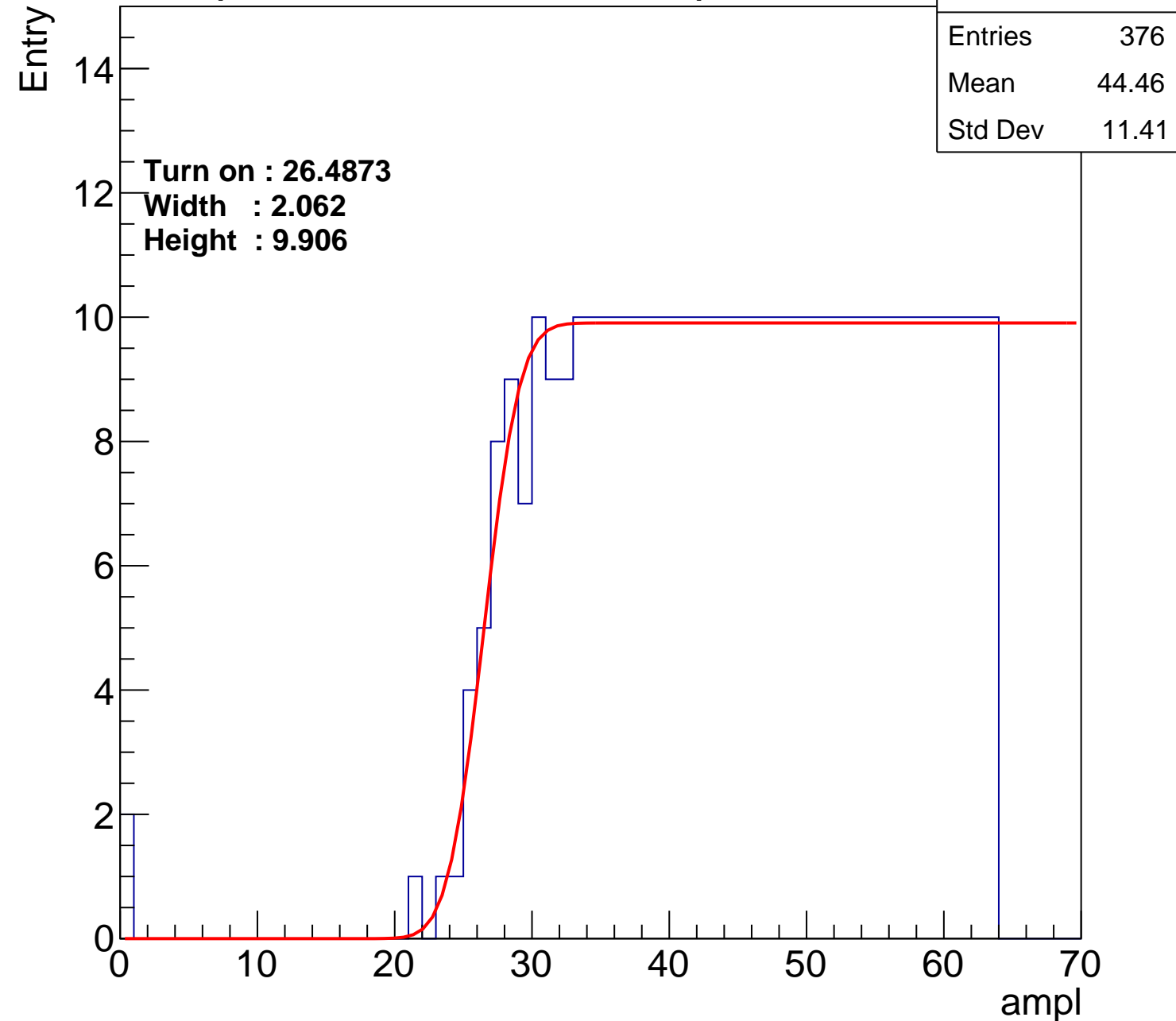
Width : 2.062

Height : 9.906

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch85

calib_packv5_042523_0143.root, FC#4, port A2

Entries	379
Mean	44.28
Std Dev	11.54

Turn on : 26.8322

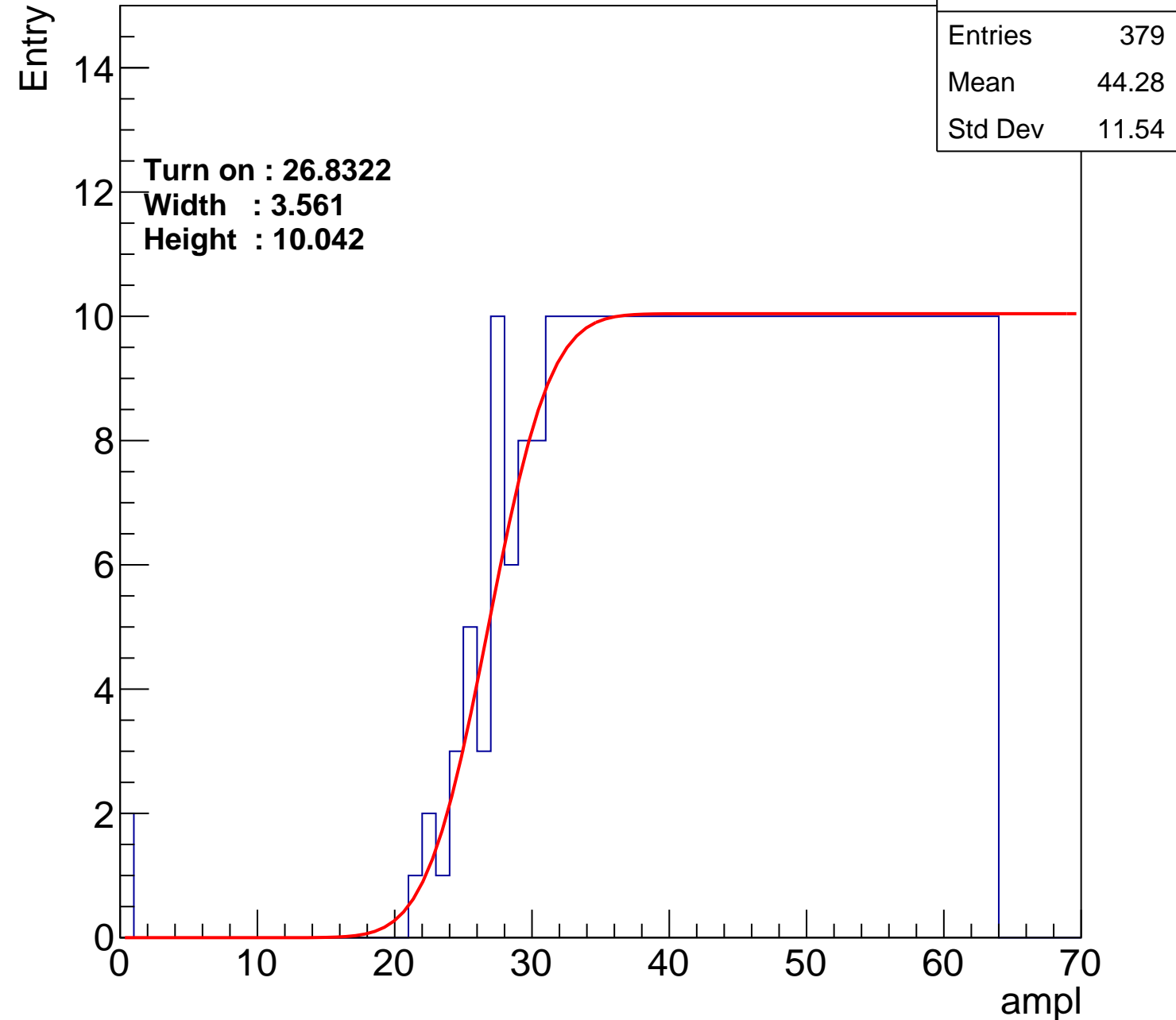
Width : 3.561

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch86

calib_packv5_042523_0143.root, FC#4, port A2

Entries	381
Mean	44.22
Std Dev	11.53

Turn on : 26.3836

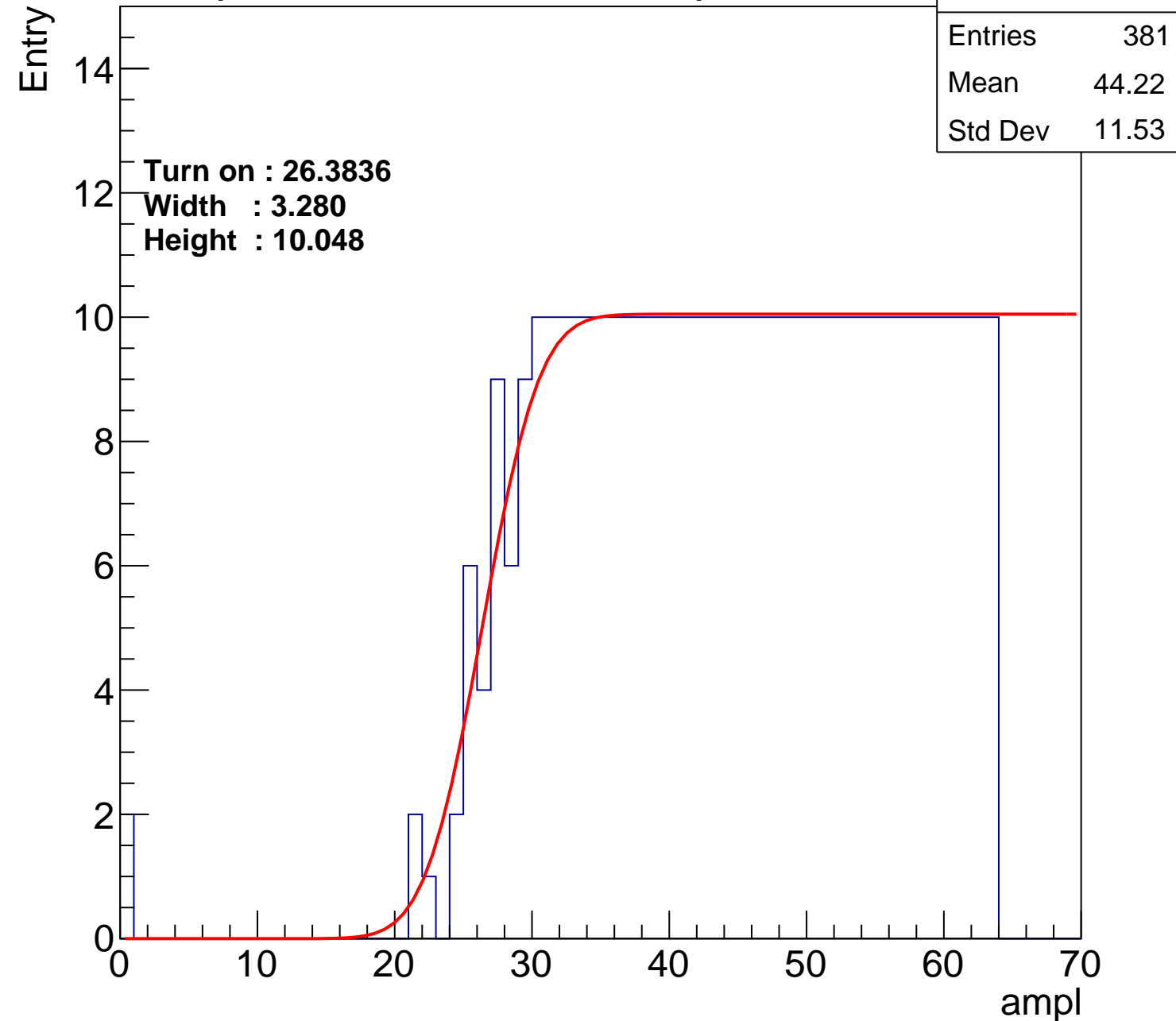
Width : 3.280

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch87

calib_packv5_042523_0143.root, FC#4, port A2

Entries	369
Mean	44.82
Std Dev	11.2

Turn on : 27.0675

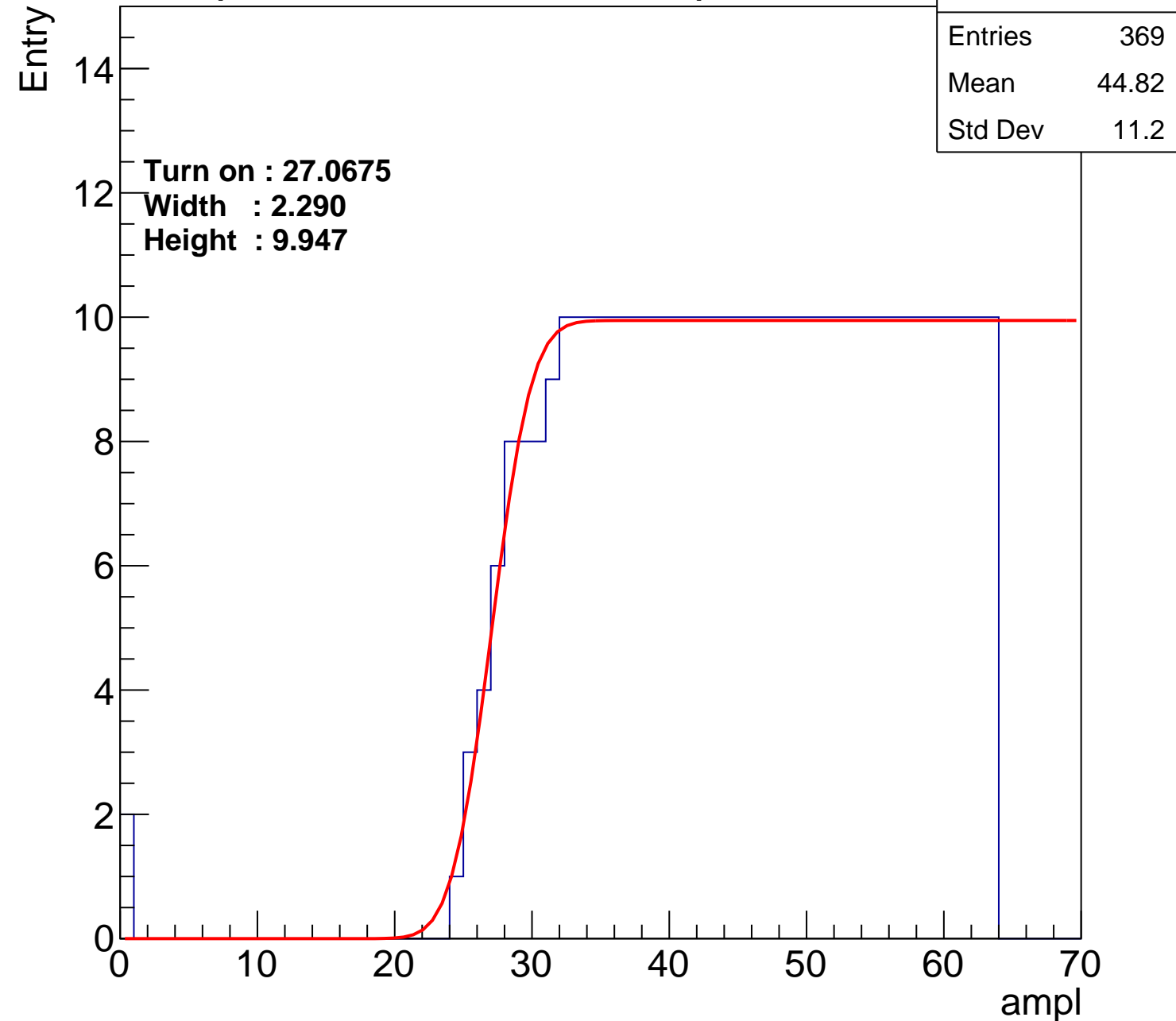
Width : 2.290

Height : 9.947

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch88

calib_packv5_042523_0143.root, FC#4, port A2

Entries	395
Mean	43.33
Std Dev	12.4

Turn on : 25.5205

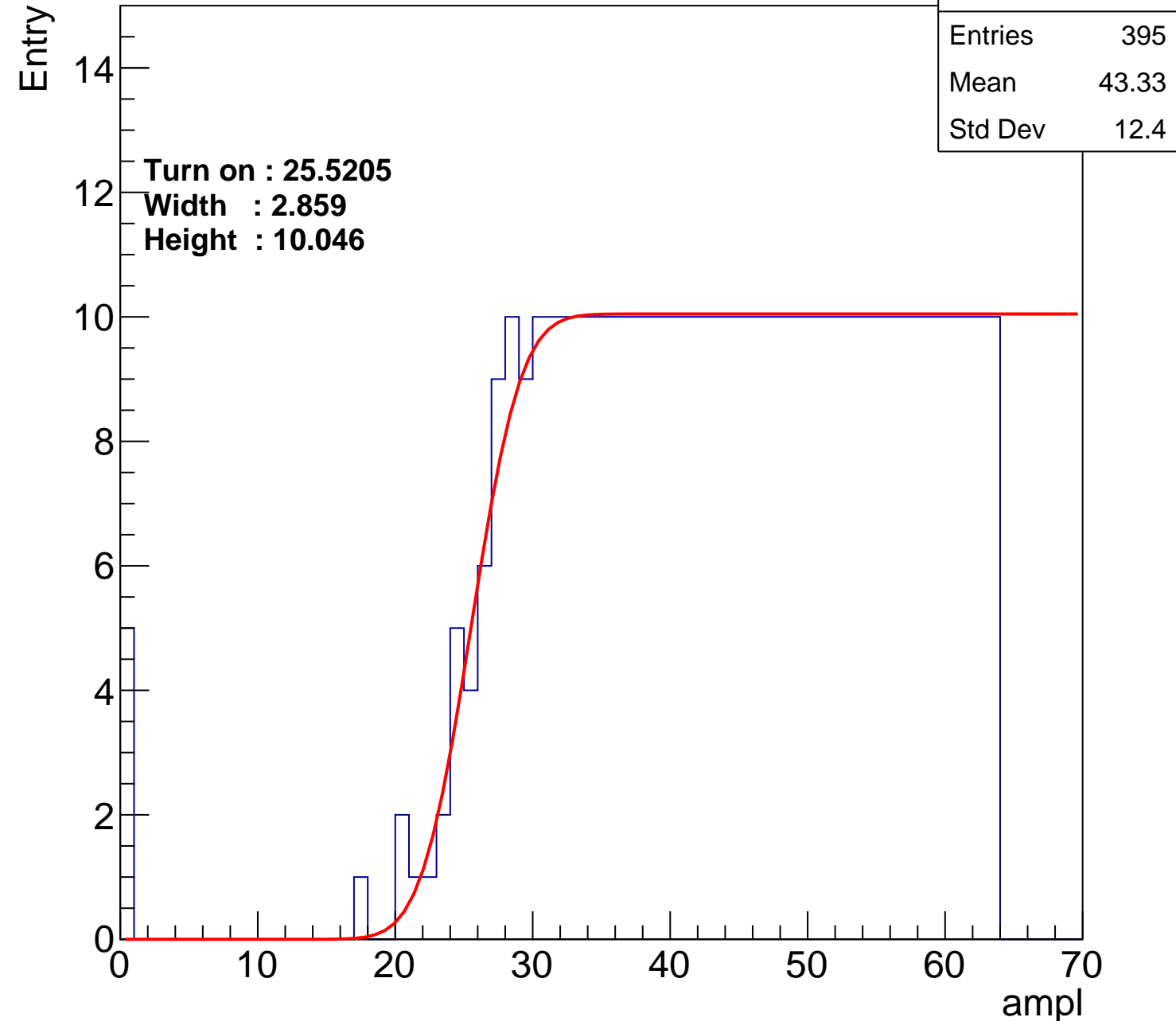
Width : 2.859

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch89

calib_packv5_042523_0143.root, FC#4, port A2

Entries	397
Mean	43.44
Std Dev	11.93

Turn on : 24.7476

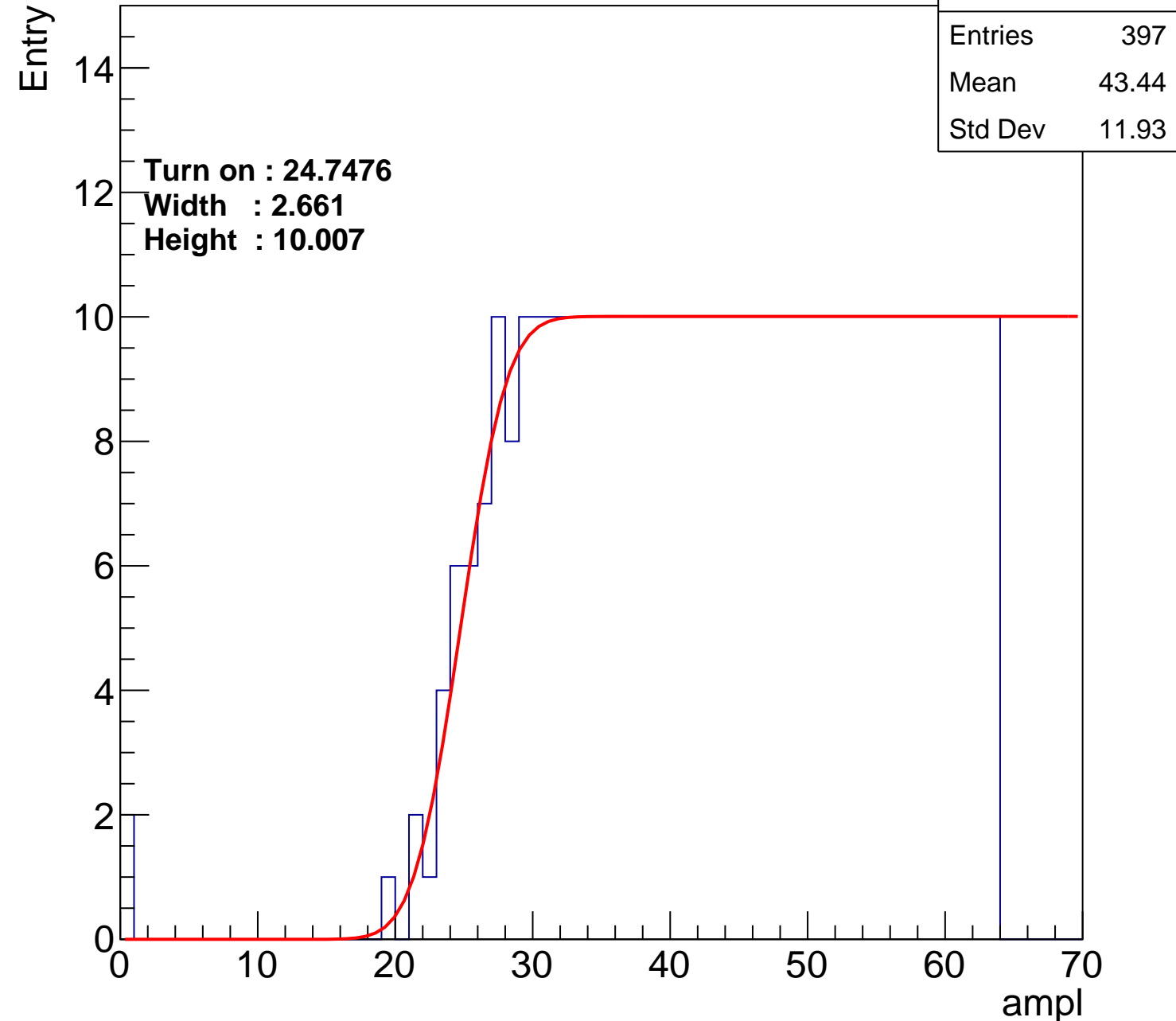
Width : 2.661

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch90

calib_packv5_042523_0143.root, FC#4, port A2

Entries	364
Mean	45.04
Std Dev	11.12

Turn on : 28.9949

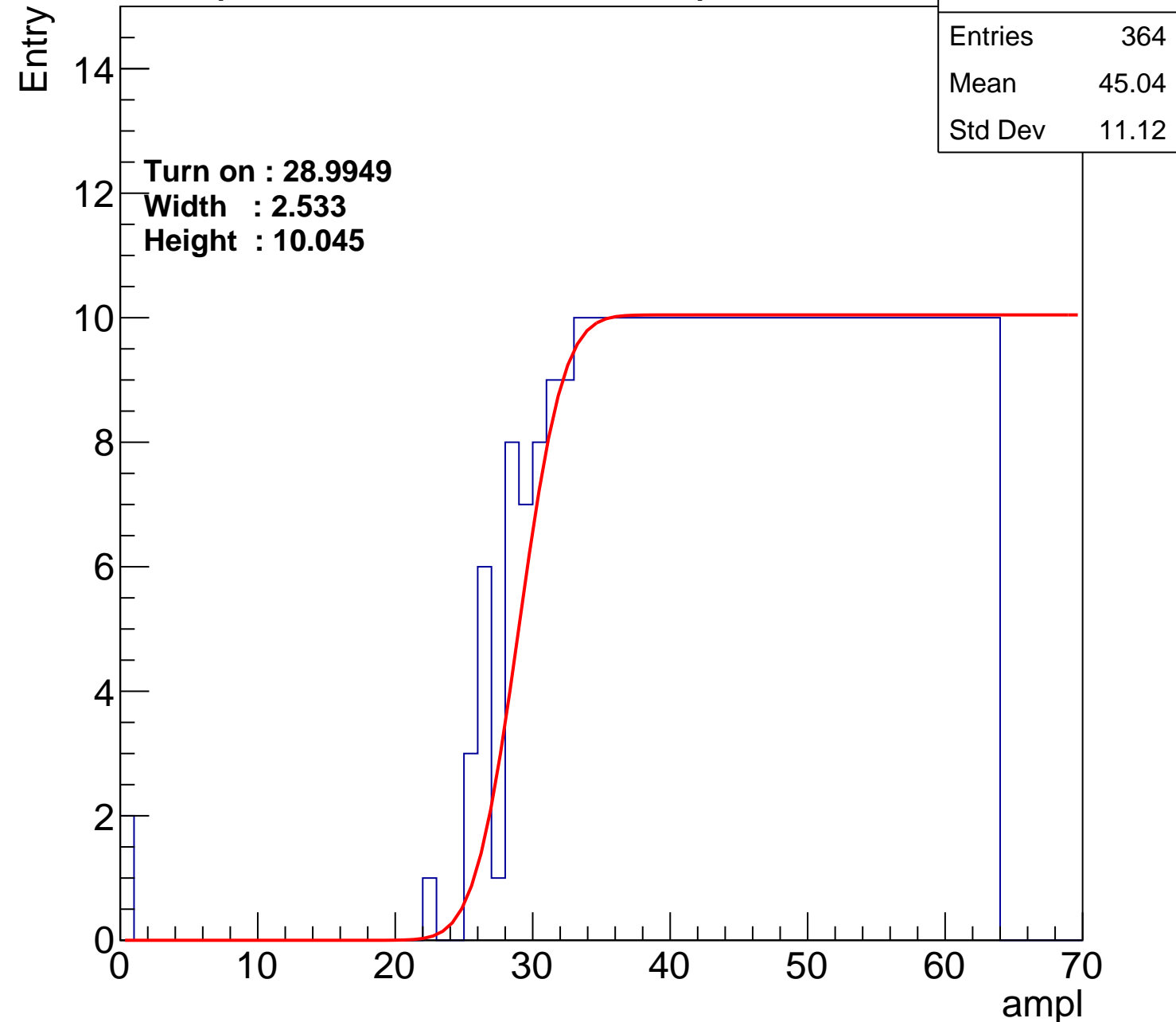
Width : 2.533

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch91

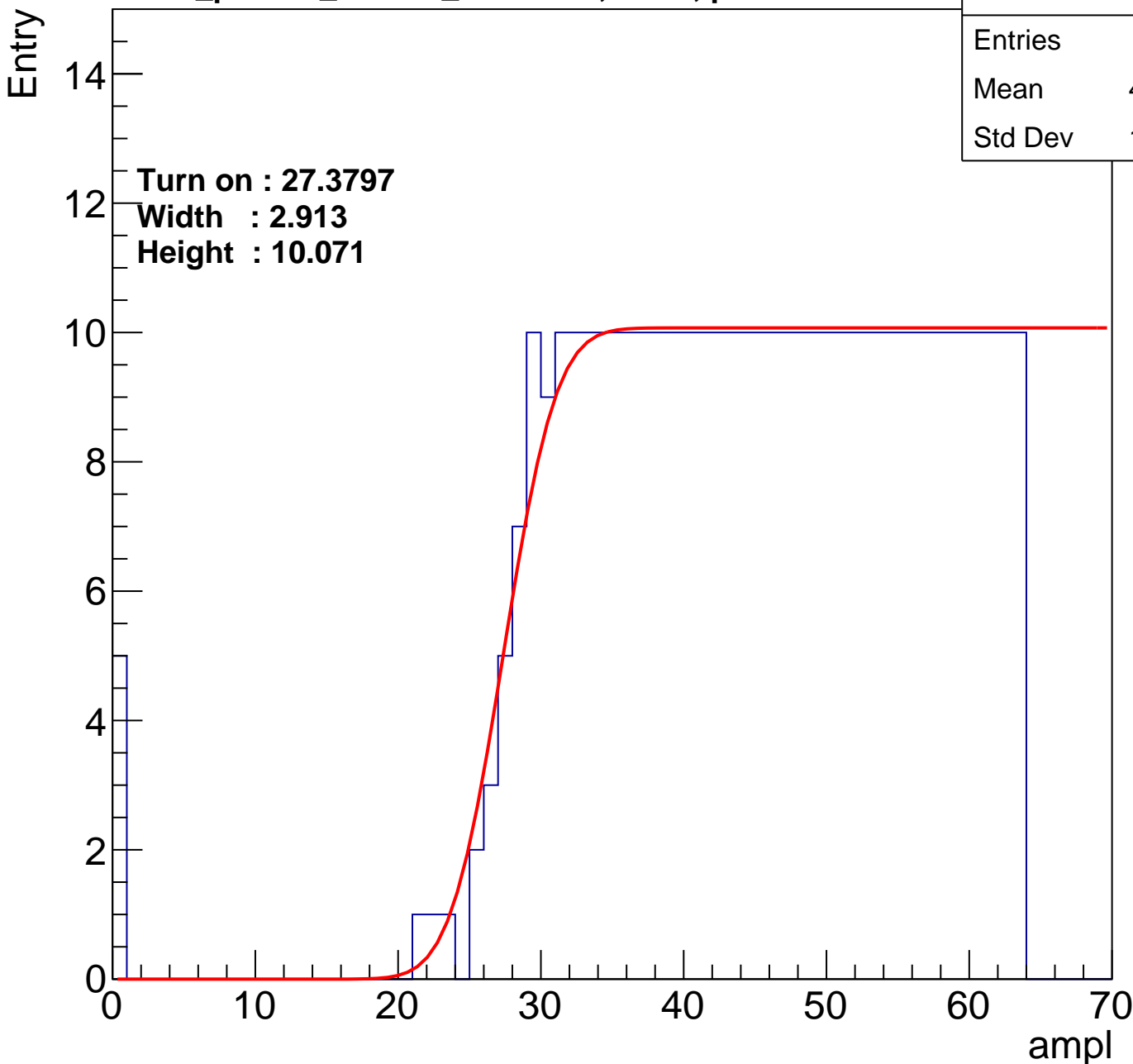
calib_packv5_042523_0143.root, FC#4, port A2

Entries	374
Mean	44.37
Std Dev	11.89

Turn on : 27.3797

Width : 2.913

Height : 10.071



B1L100S, U8-ch92

calib_packv5_042523_0143.root, FC#4, port A2

Entries	384
Mean	44.02
Std Dev	11.77

Turn on : 26.3223

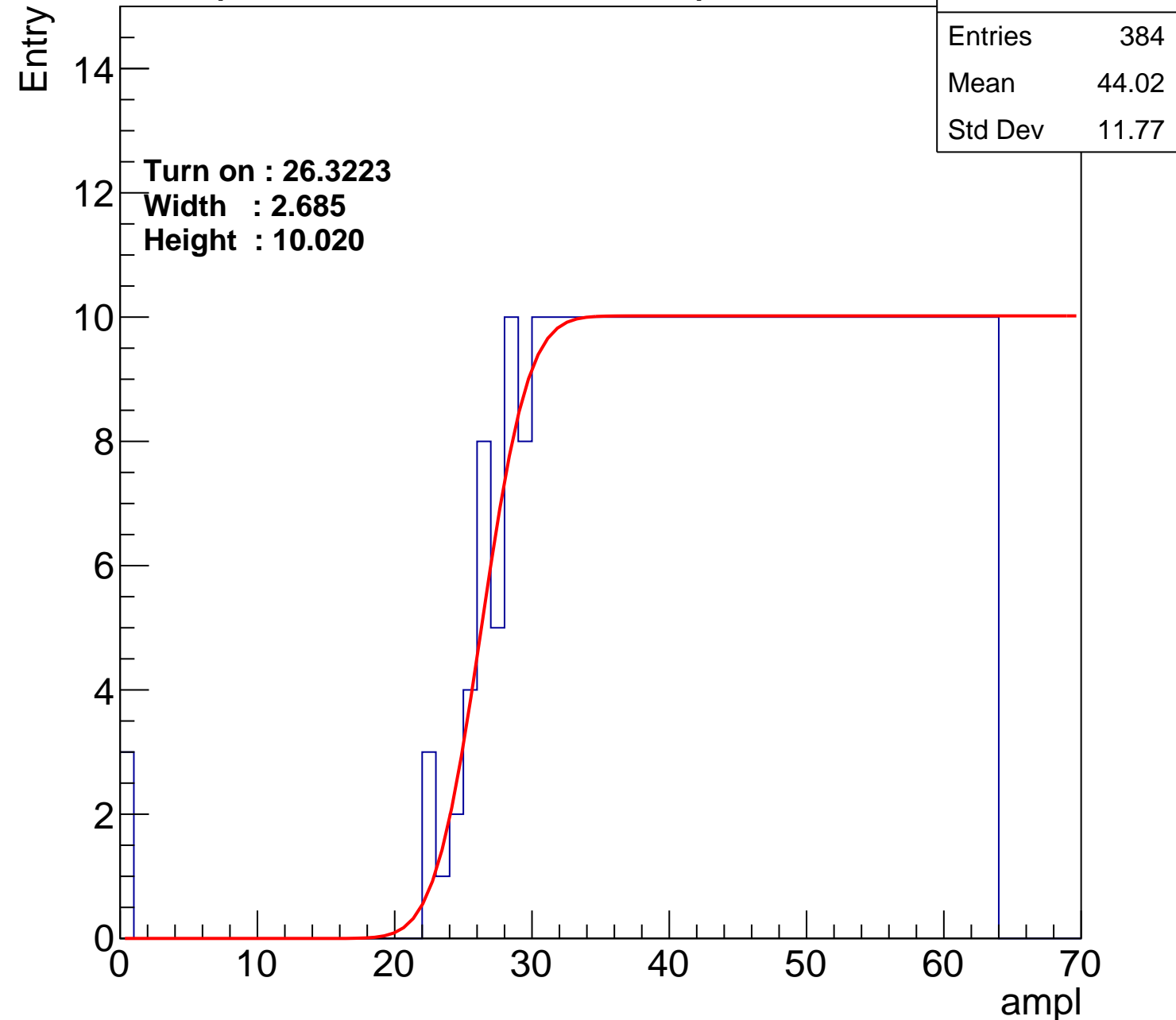
Width : 2.685

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch93

calib_packv5_042523_0143.root, FC#4, port A2

Entries	381
Mean	44.23
Std Dev	11.52

Turn on : 26.2303

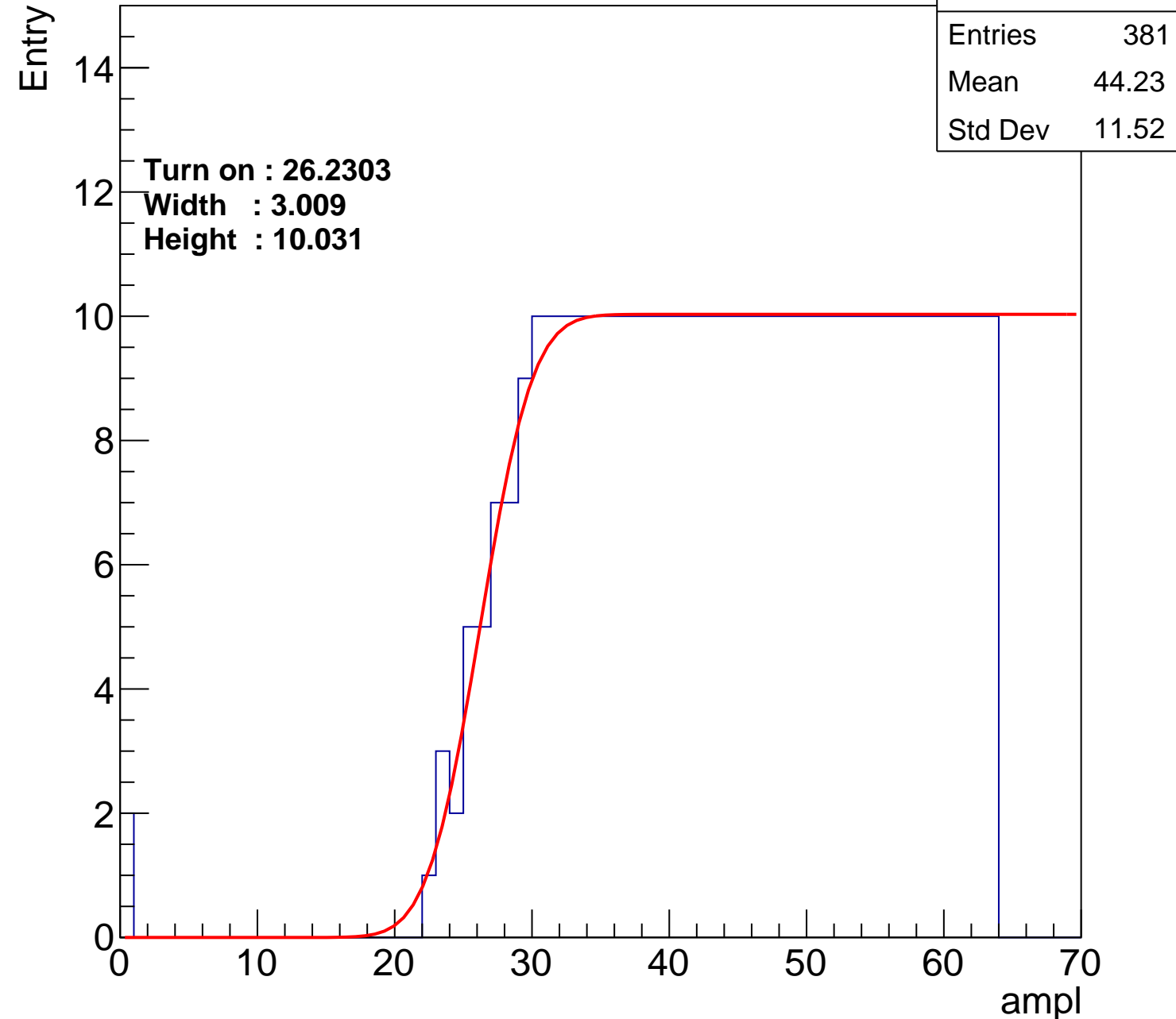
Width : 3.009

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch94

calib_packv5_042523_0143.root, FC#4, port A2

Entries	369
Mean	44.83
Std Dev	11.18

Turn on : 27.3869

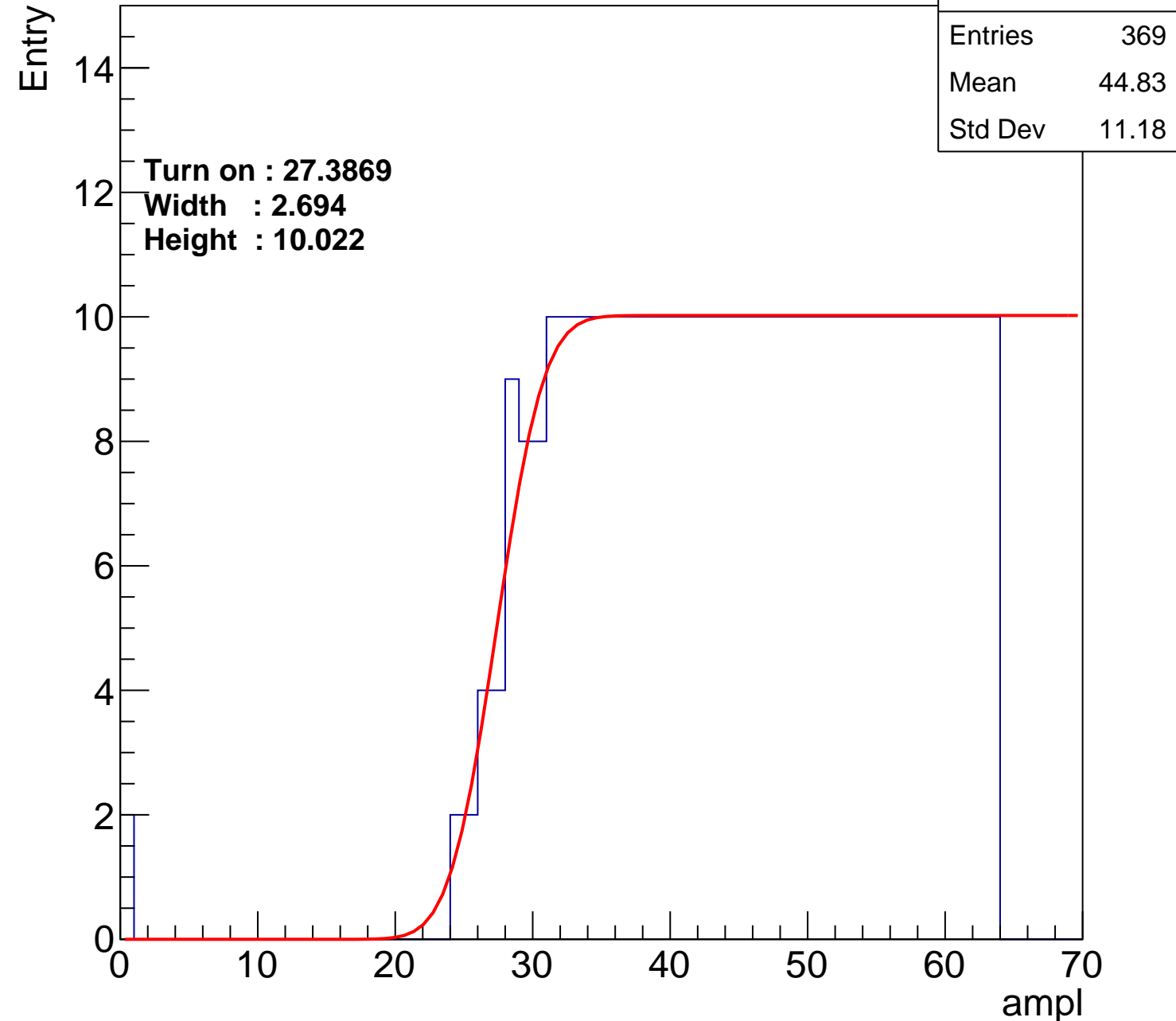
Width : 2.694

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch95

calib_packv5_042523_0143.root, FC#4, port A2

Entries	379
Mean	44.24
Std Dev	11.68

Turn on : 26.9189

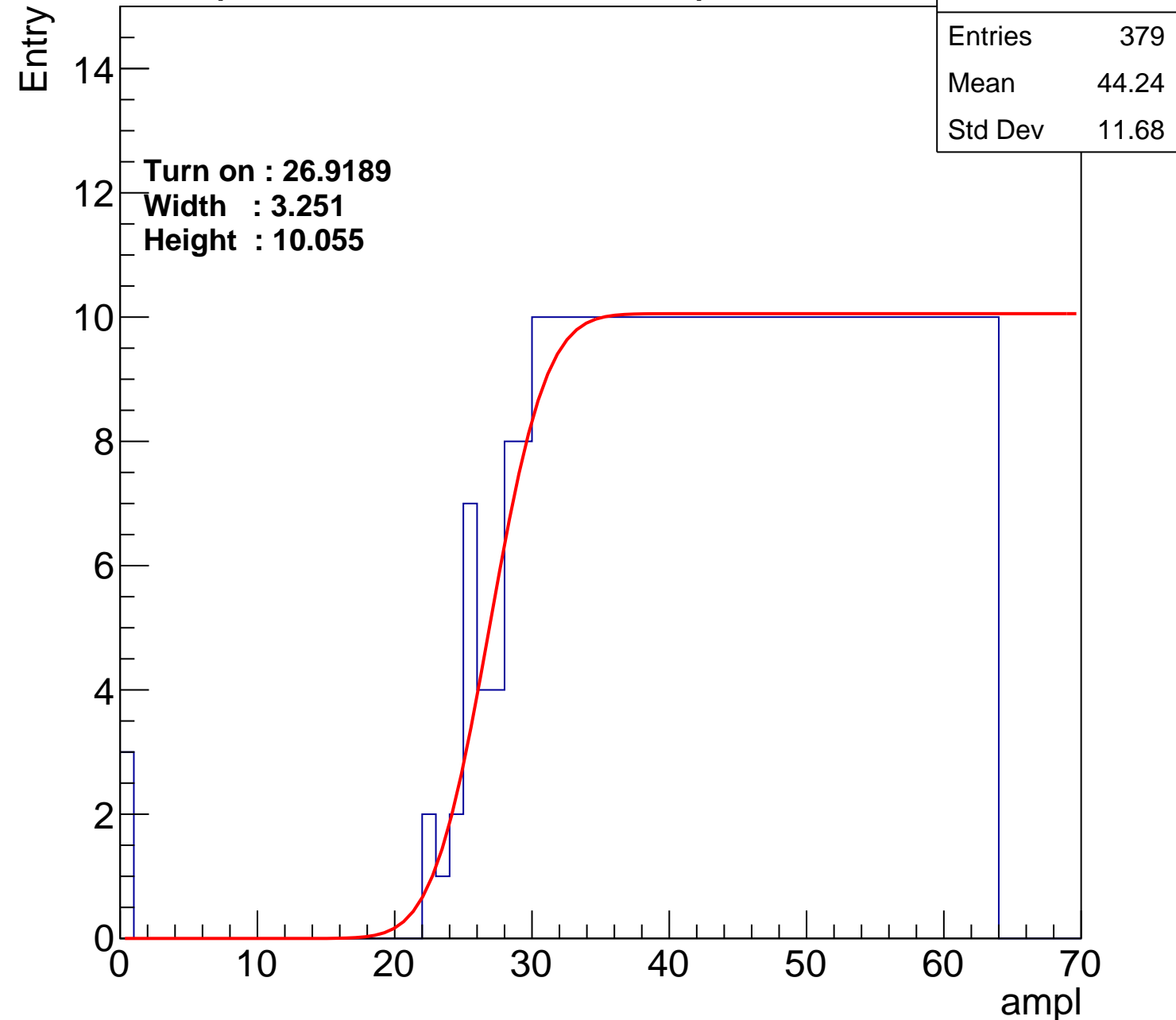
Width : 3.251

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch96

calib_packv5_042523_0143.root, FC#4, port A2

Entries	385
Mean	44.12
Std Dev	11.41

Turn on : 25.8139

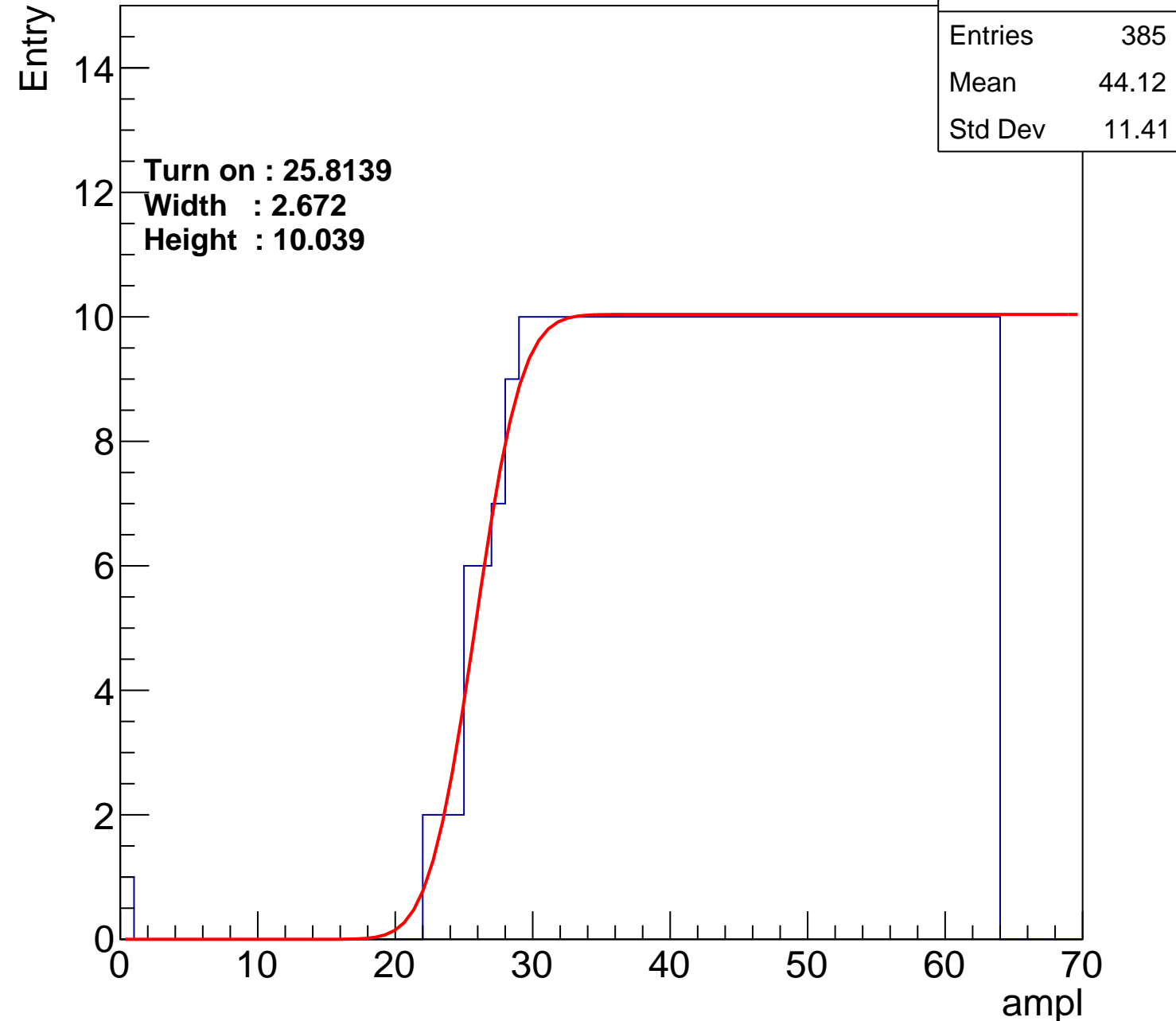
Width : 2.672

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch97

calib_packv5_042523_0143.root, FC#4, port A2

Entries	368
Mean	44.93
Std Dev	10.99

Turn on : 27.4210

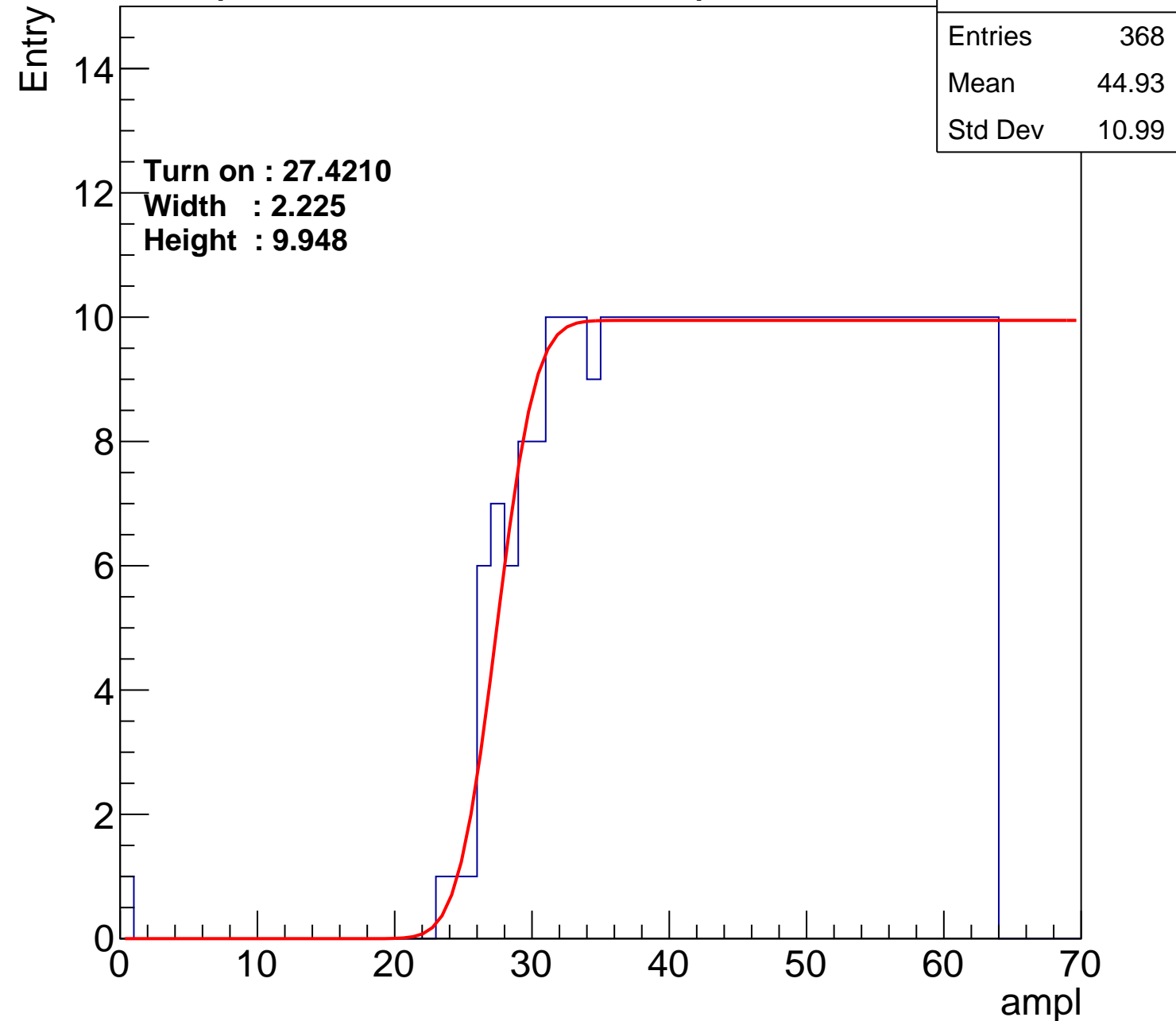
Width : 2.225

Height : 9.948

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch98

calib_packv5_042523_0143.root, FC#4, port A2

Entries	372
Mean	44.57
Std Dev	11.54

Turn on : 27.3573

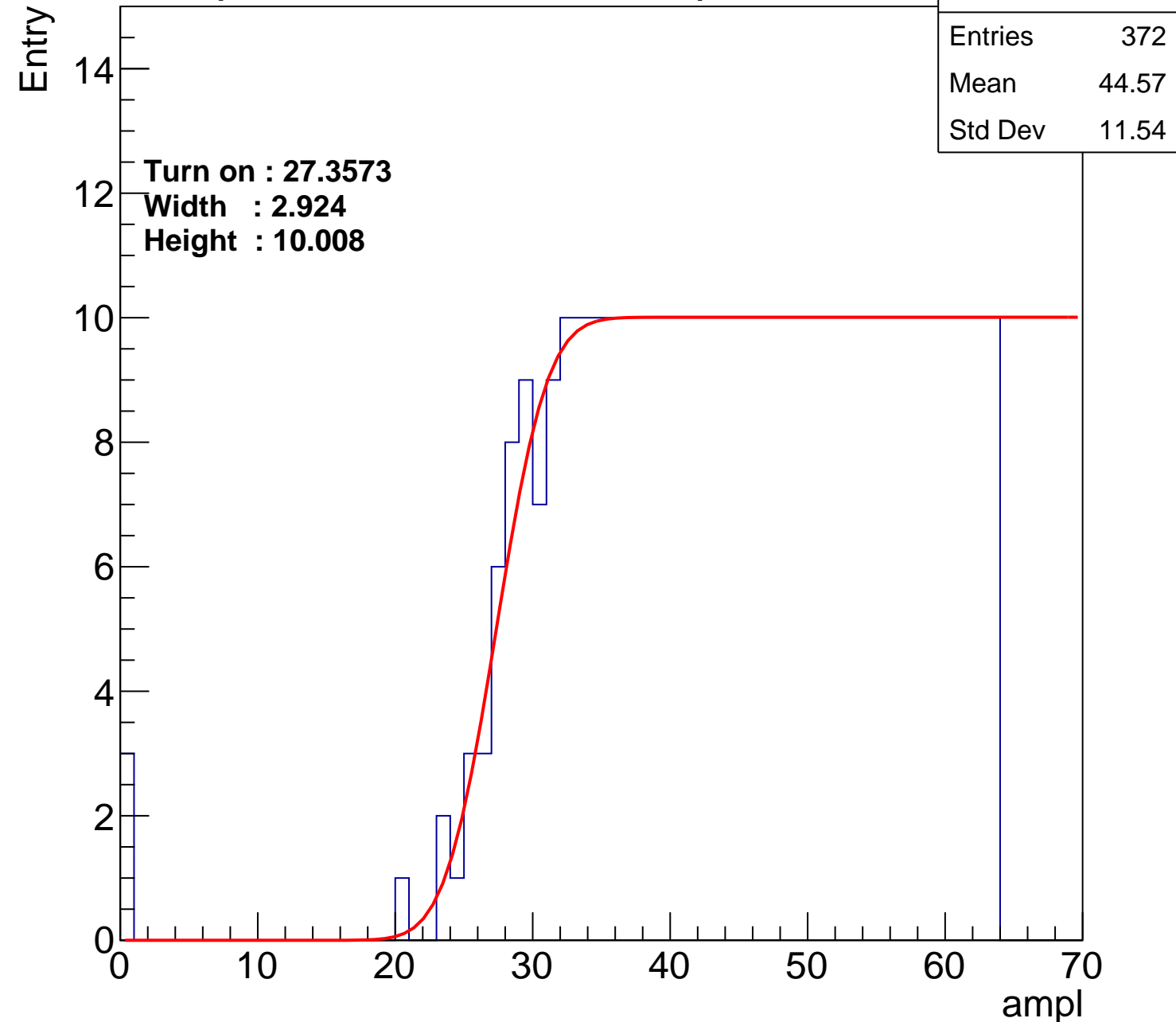
Width : 2.924

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch99

calib_packv5_042523_0143.root, FC#4, port A2

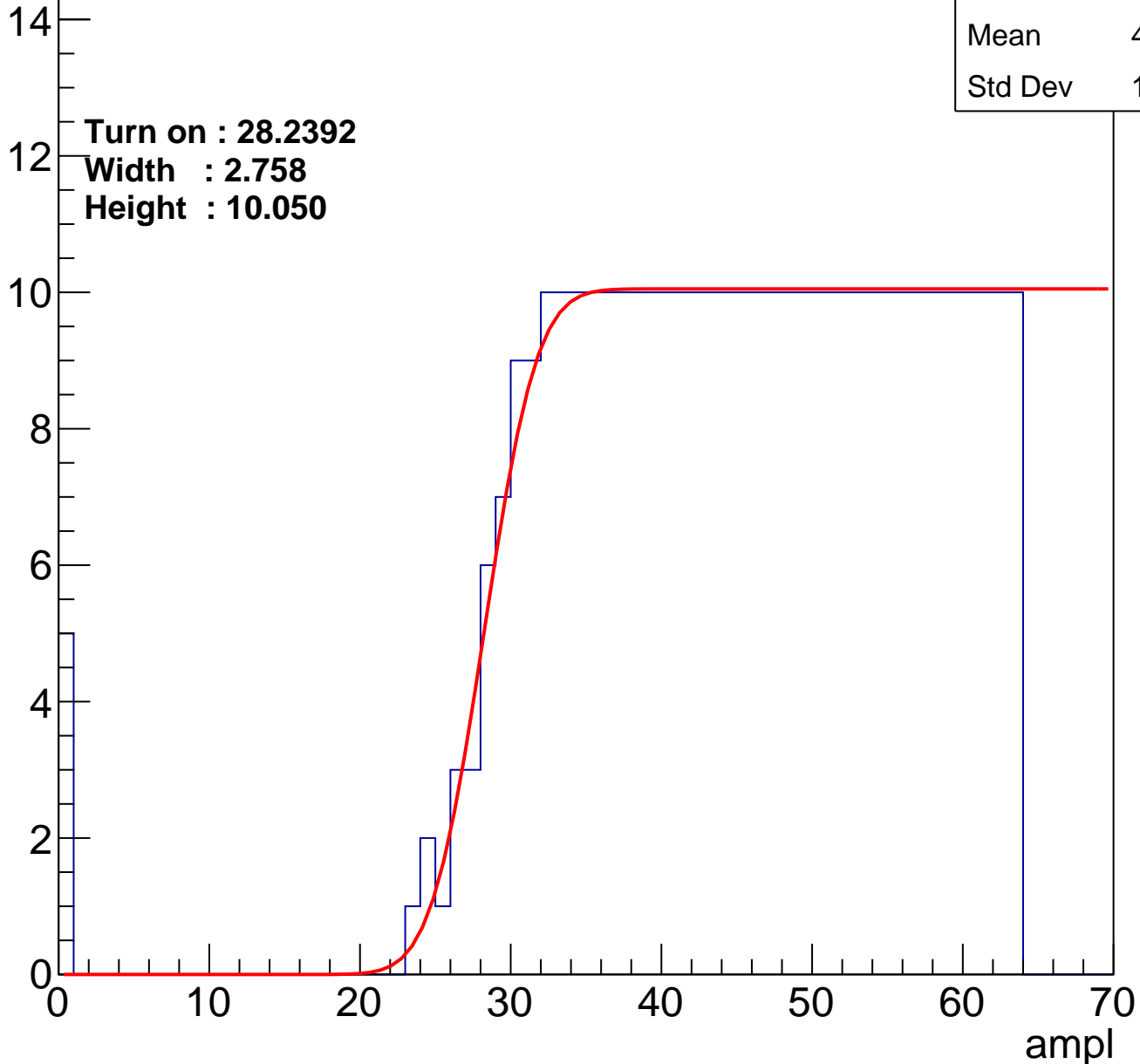
Entries	366
Mean	44.74
Std Dev	11.75

Turn on : 28.2392

Width : 2.758

Height : 10.050

Entry



B1L100S, U8-ch100

calib_packv5_042523_0143.root, FC#4, port A2

Entries	385
Mean	44.01
Std Dev	11.66

Turn on : 26.4403

Width : 2.880

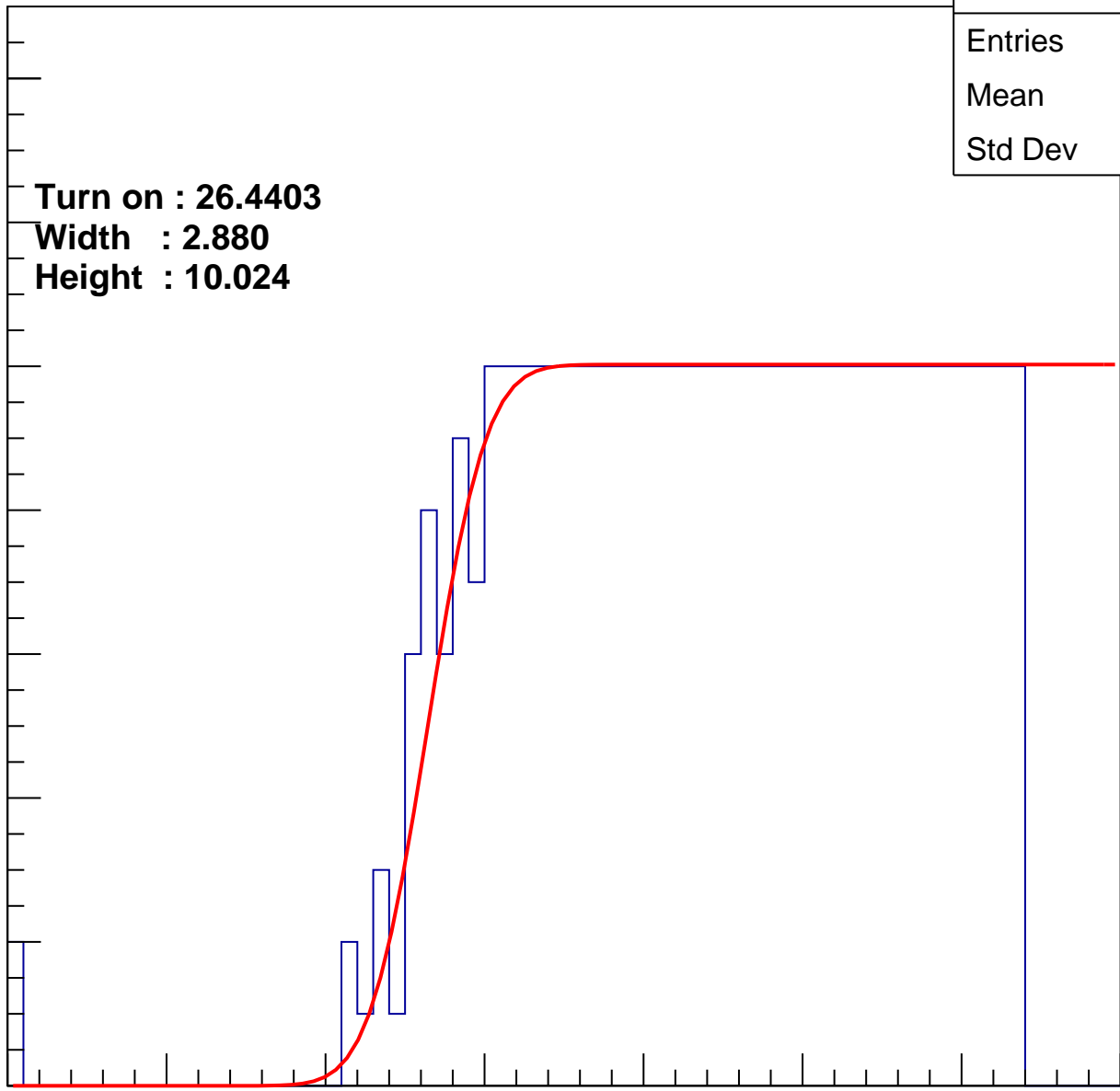
Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L100S, U8-ch101

calib_packv5_042523_0143.root, FC#4, port A2

Entries	373
Mean	44.57
Std Dev	11.39

Turn on : 26.7437

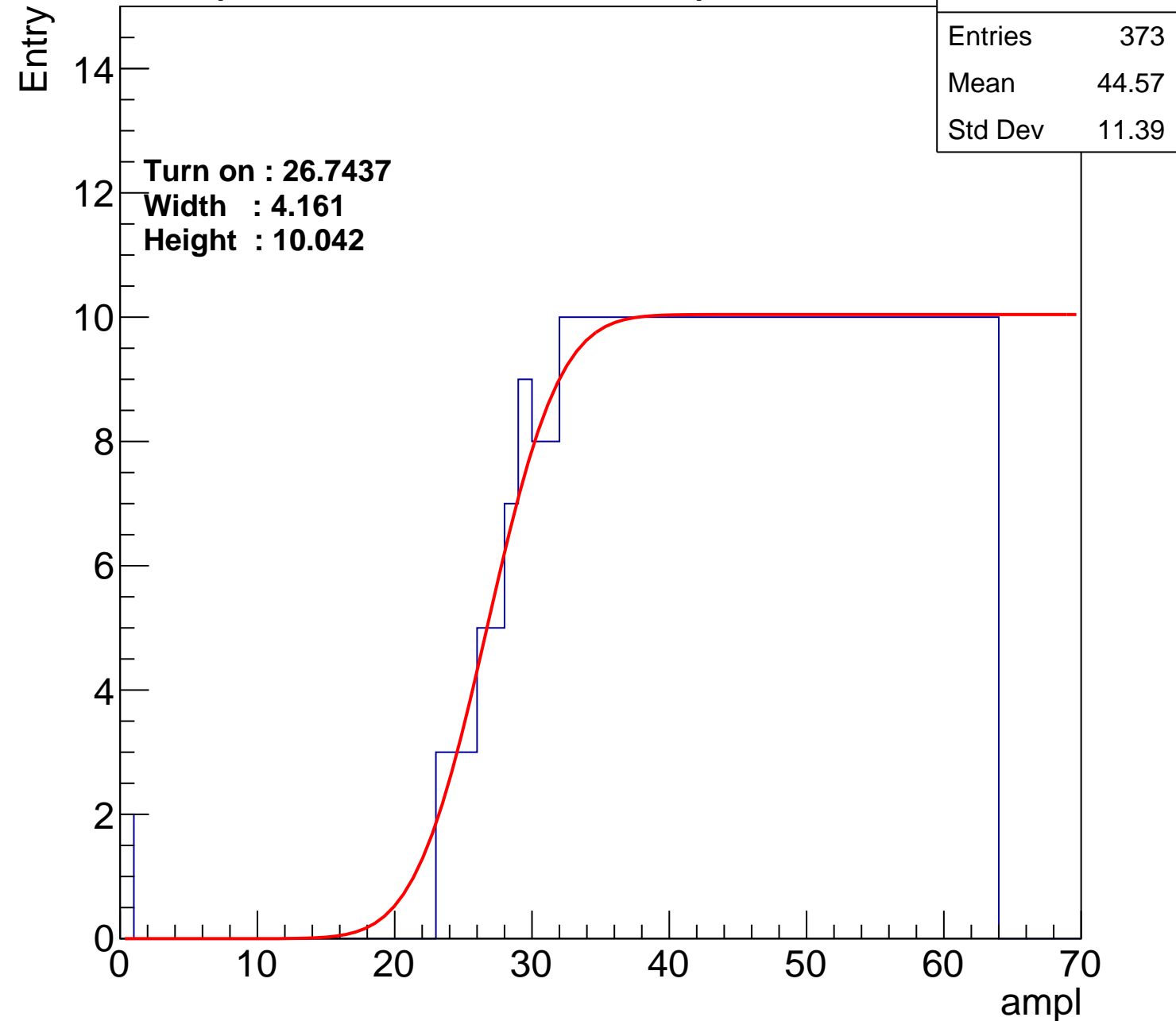
Width : 4.161

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch102

calib_packv5_042523_0143.root, FC#4, port A2

Entries	373
Mean	44.66
Std Dev	11.16

Turn on : 26.9586

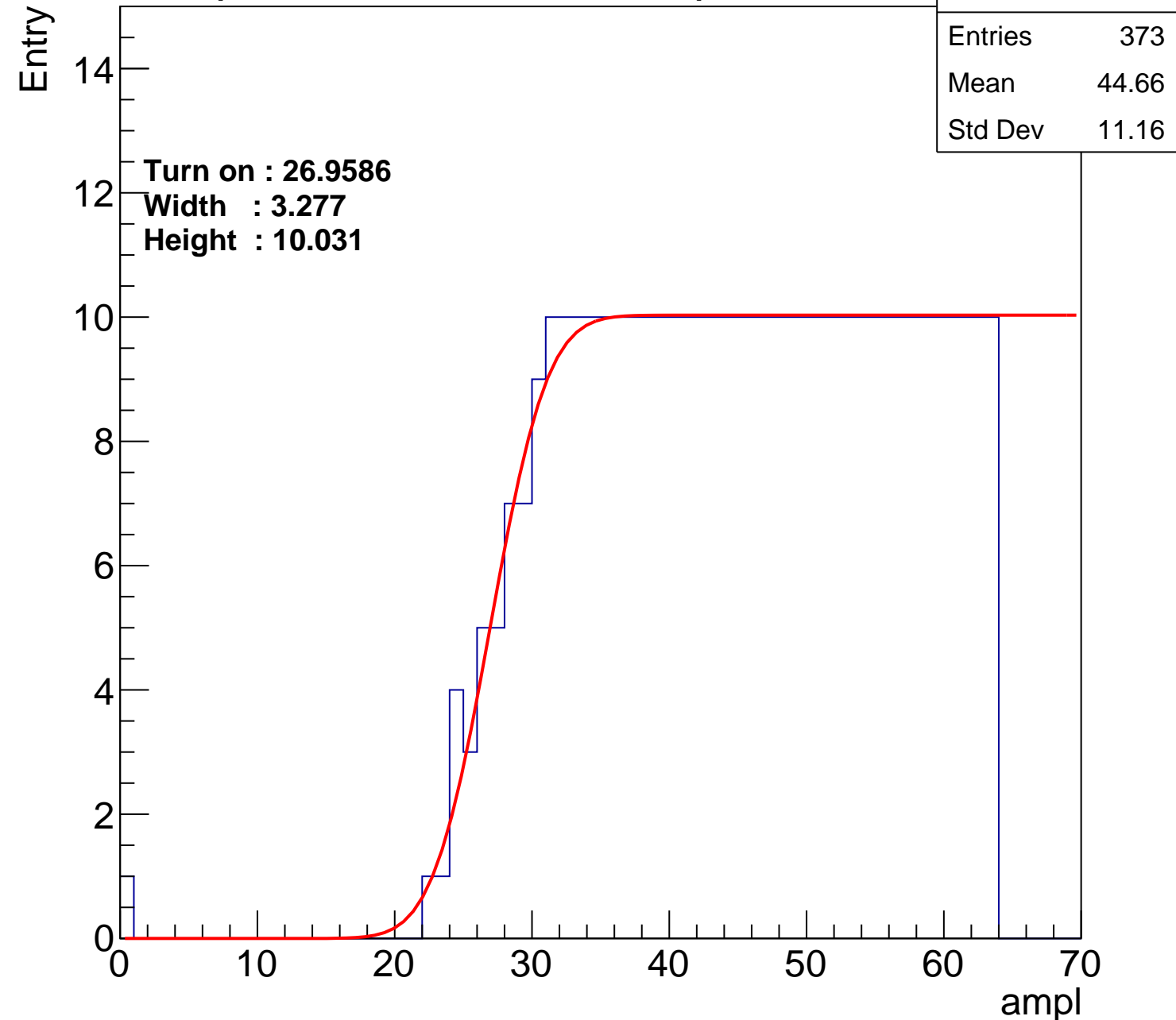
Width : 3.277

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch103

calib_packv5_042523_0143.root, FC#4, port A2

Entries	368
Mean	44.7
Std Dev	11.62

Turn on : 27.7042

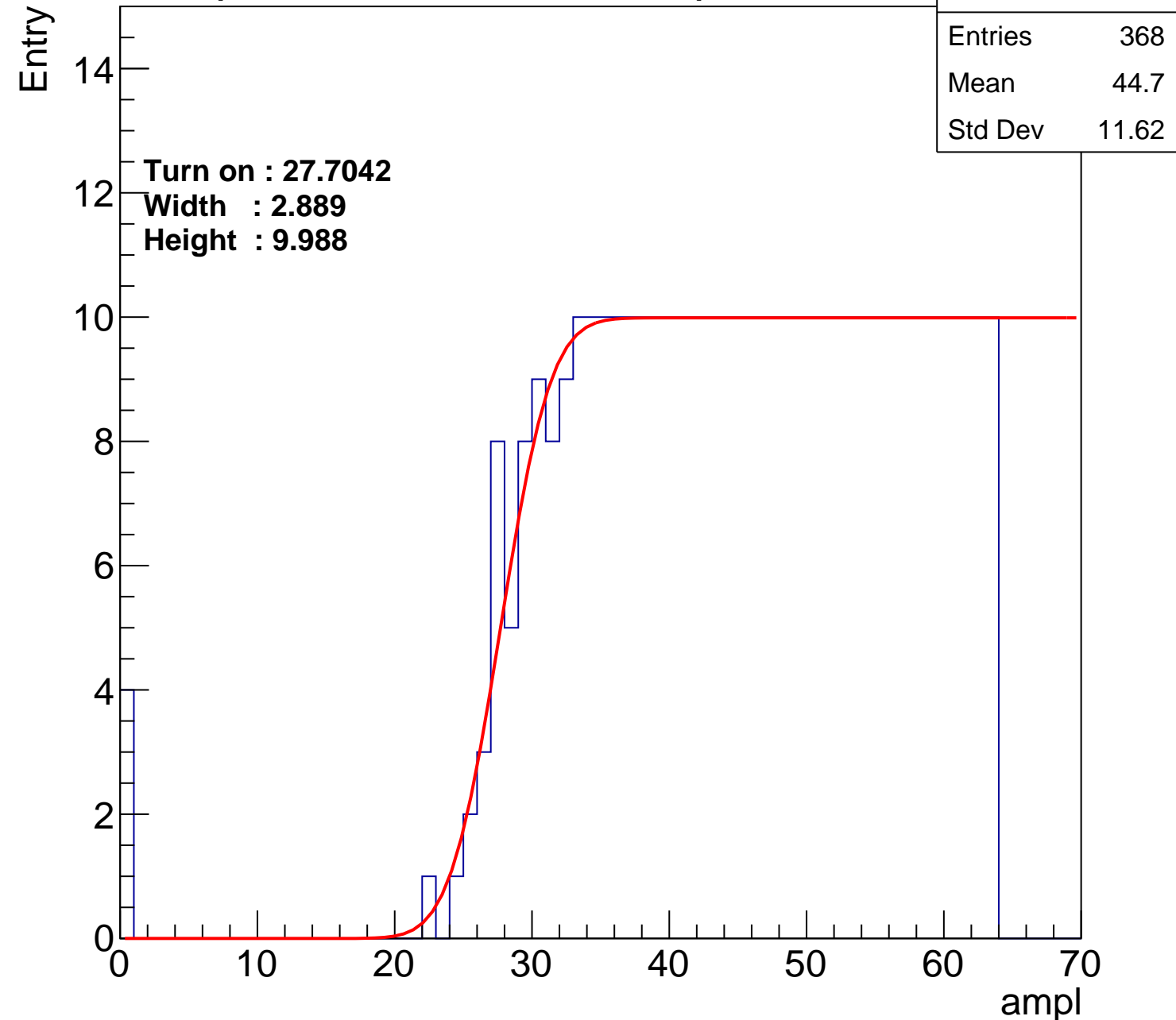
Width : 2.889

Height : 9.988

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch104

calib_packv5_042523_0143.root, FC#4, port A2

Entries	363
Mean	45.18
Std Dev	10.85

Turn on : 27.7912

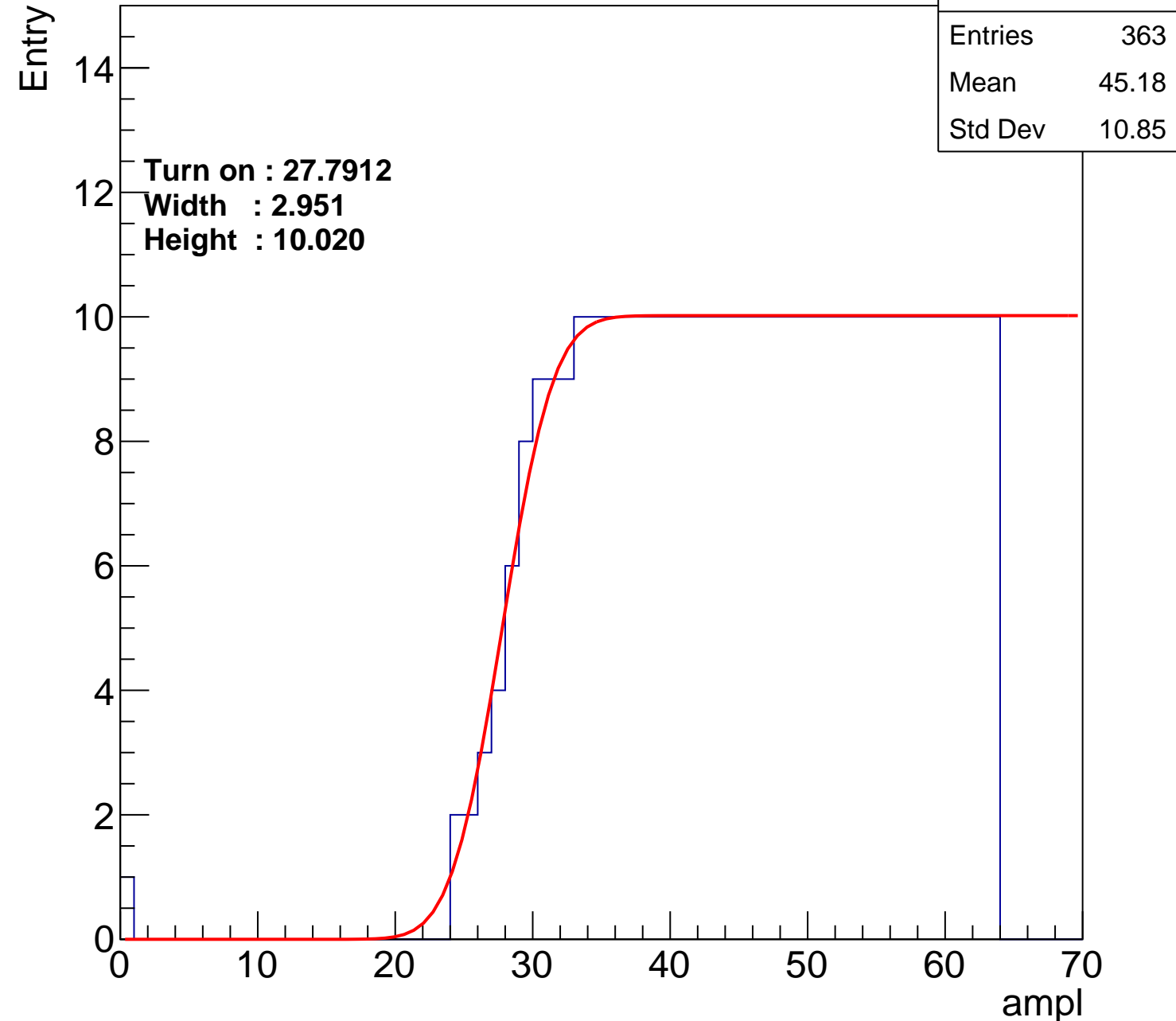
Width : 2.951

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch105

calib_packv5_042523_0143.root, FC#4, port A2

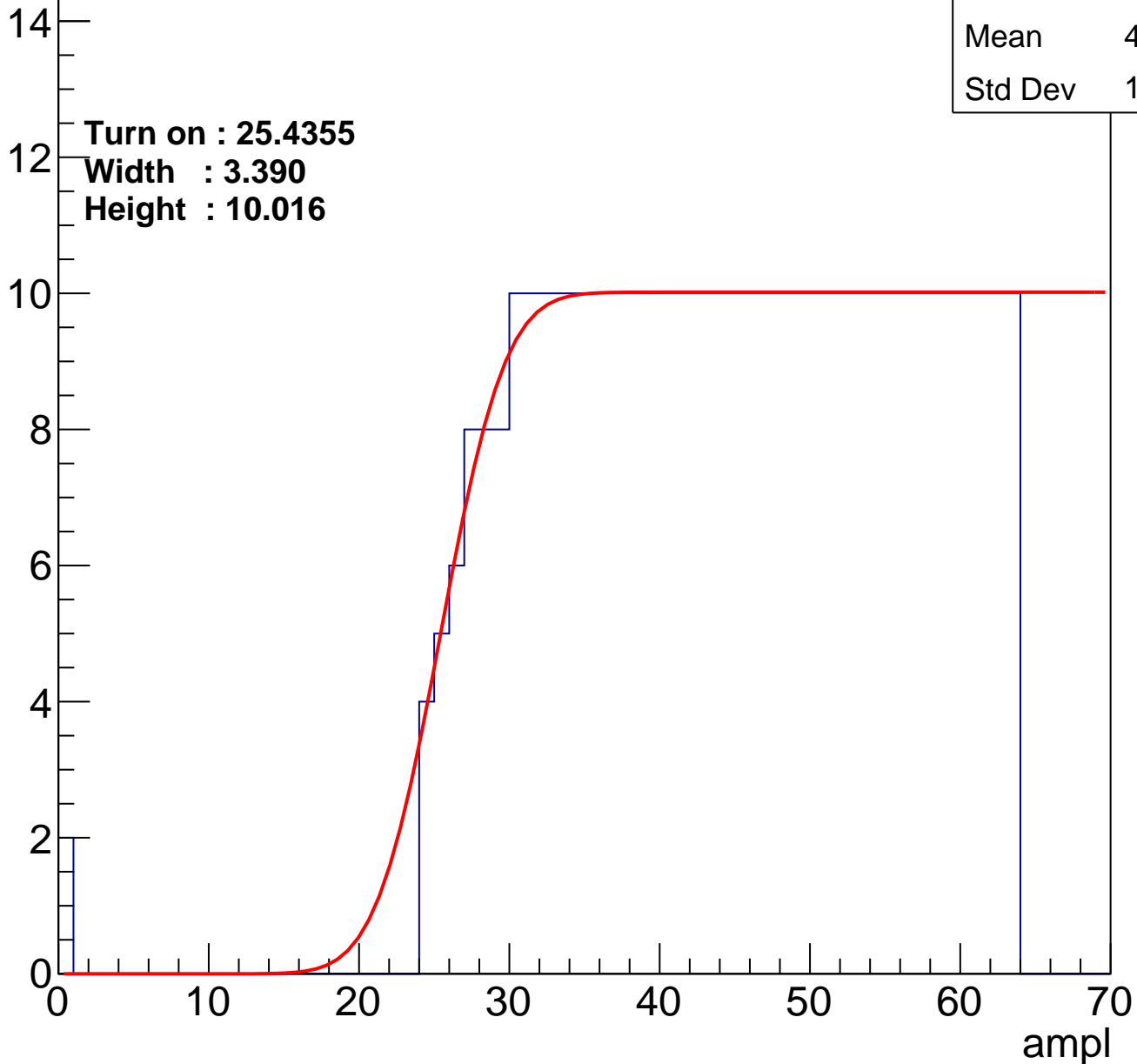
Entries	381
Mean	44.25
Std Dev	11.48

Turn on : 25.4355

Width : 3.390

Height : 10.016

Entry



B1L100S, U8-ch106

calib_packv5_042523_0143.root, FC#4, port A2

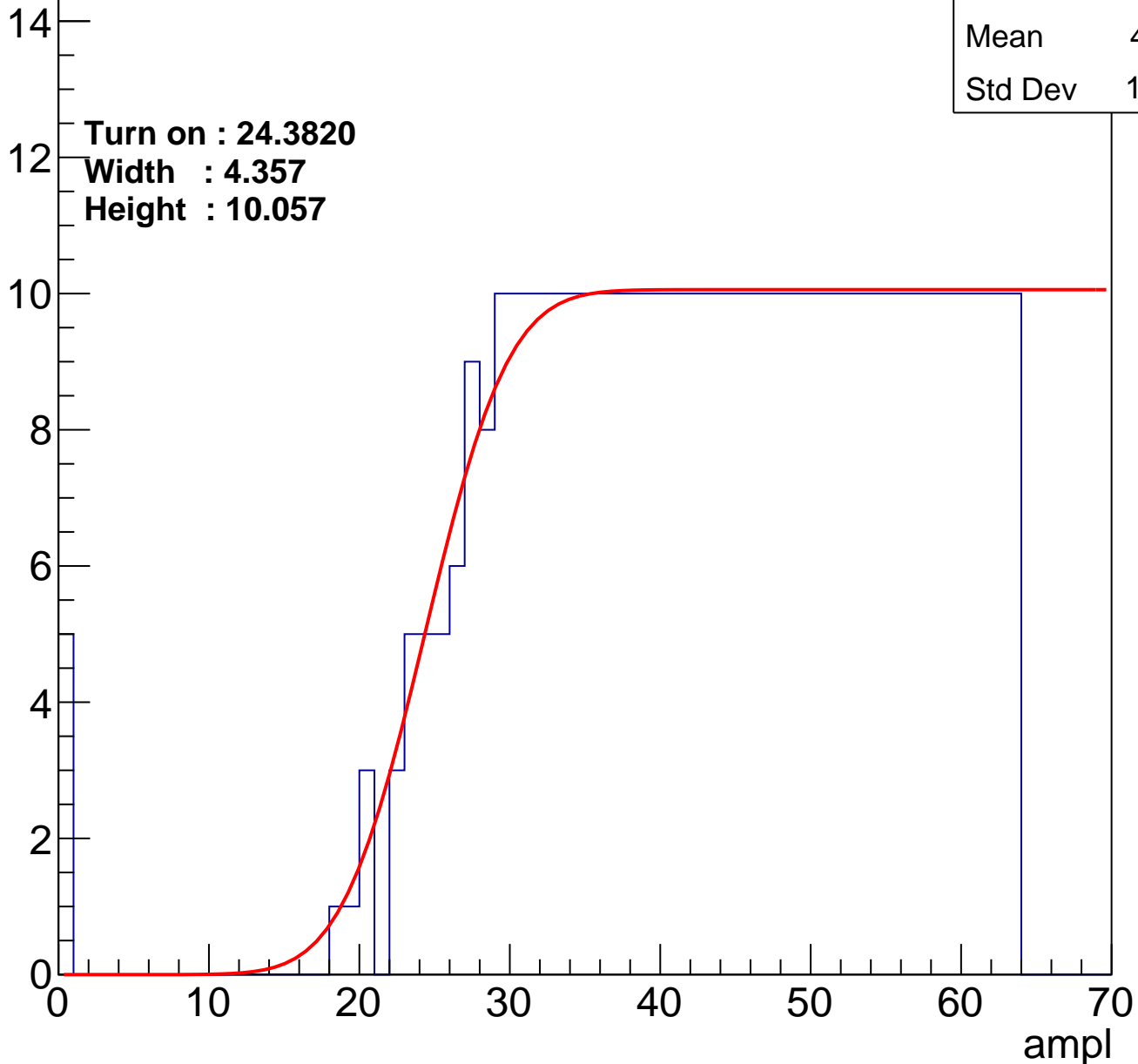
Entries	401
Mean	43.01
Std Dev	12.58

Turn on : 24.3820

Width : 4.357

Height : 10.057

Entry



B1L100S, U8-ch107

calib_packv5_042523_0143.root, FC#4, port A2

Entries	368
Mean	44.88
Std Dev	11.08

Turn on : 27.5319

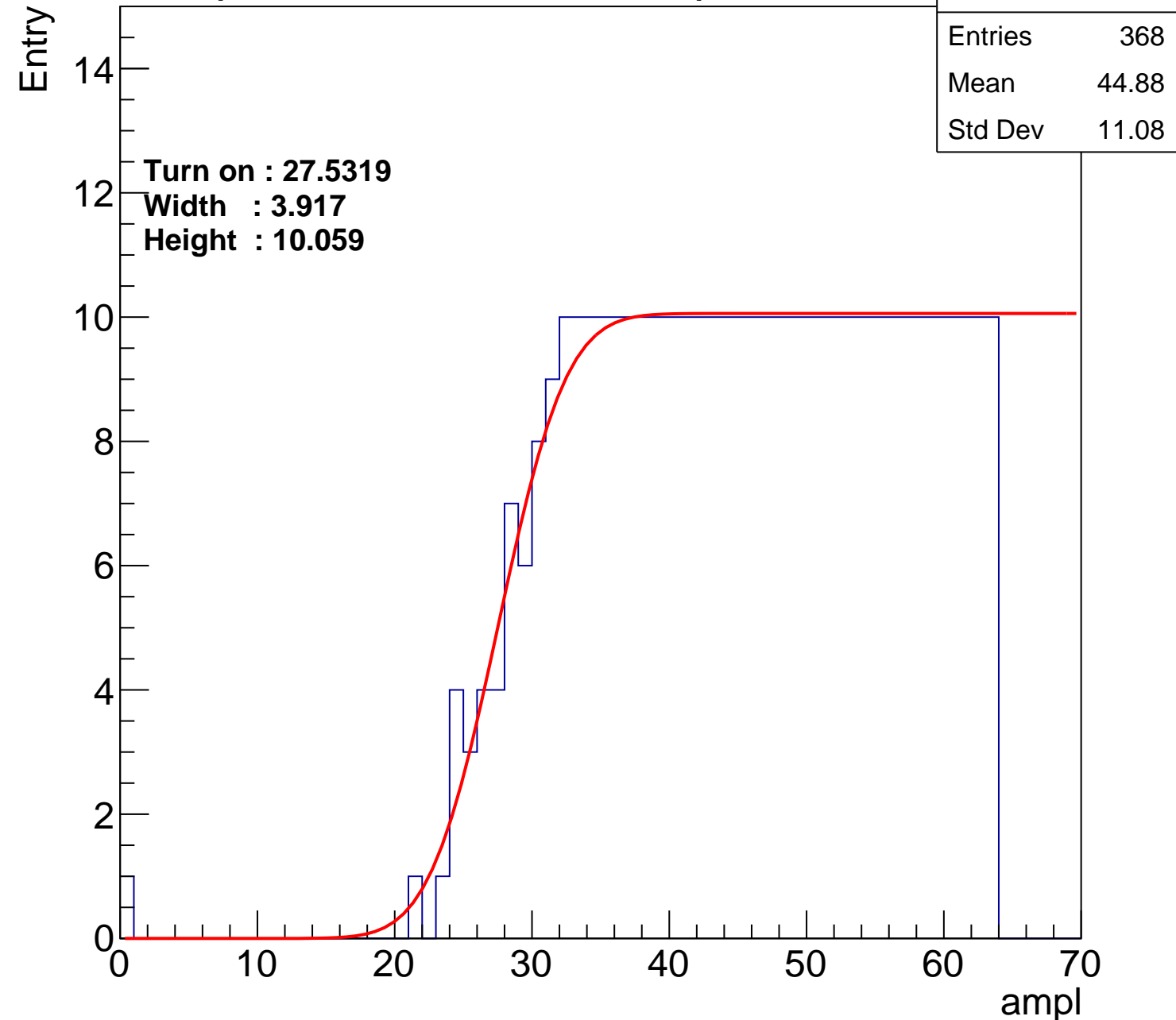
Width : 3.917

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch108

calib_packv5_042523_0143.root, FC#4, port A2

Entries	352
Mean	45.46
Std Dev	11.29

Turn on : 29.0144

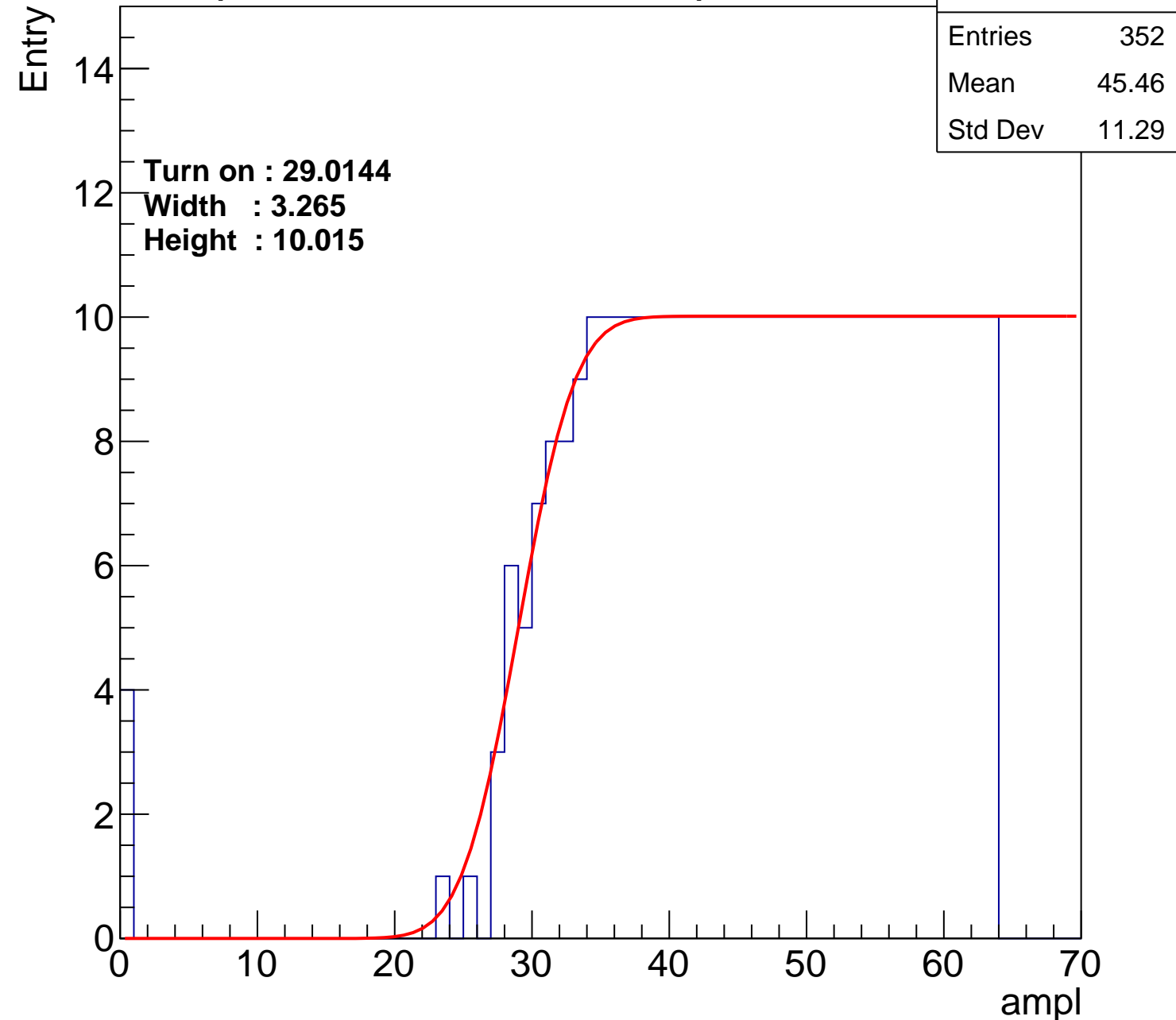
Width : 3.265

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch109

calib_packv5_042523_0143.root, FC#4, port A2

Entries	394
Mean	43.54
Std Dev	11.99

Turn on : 24.6408

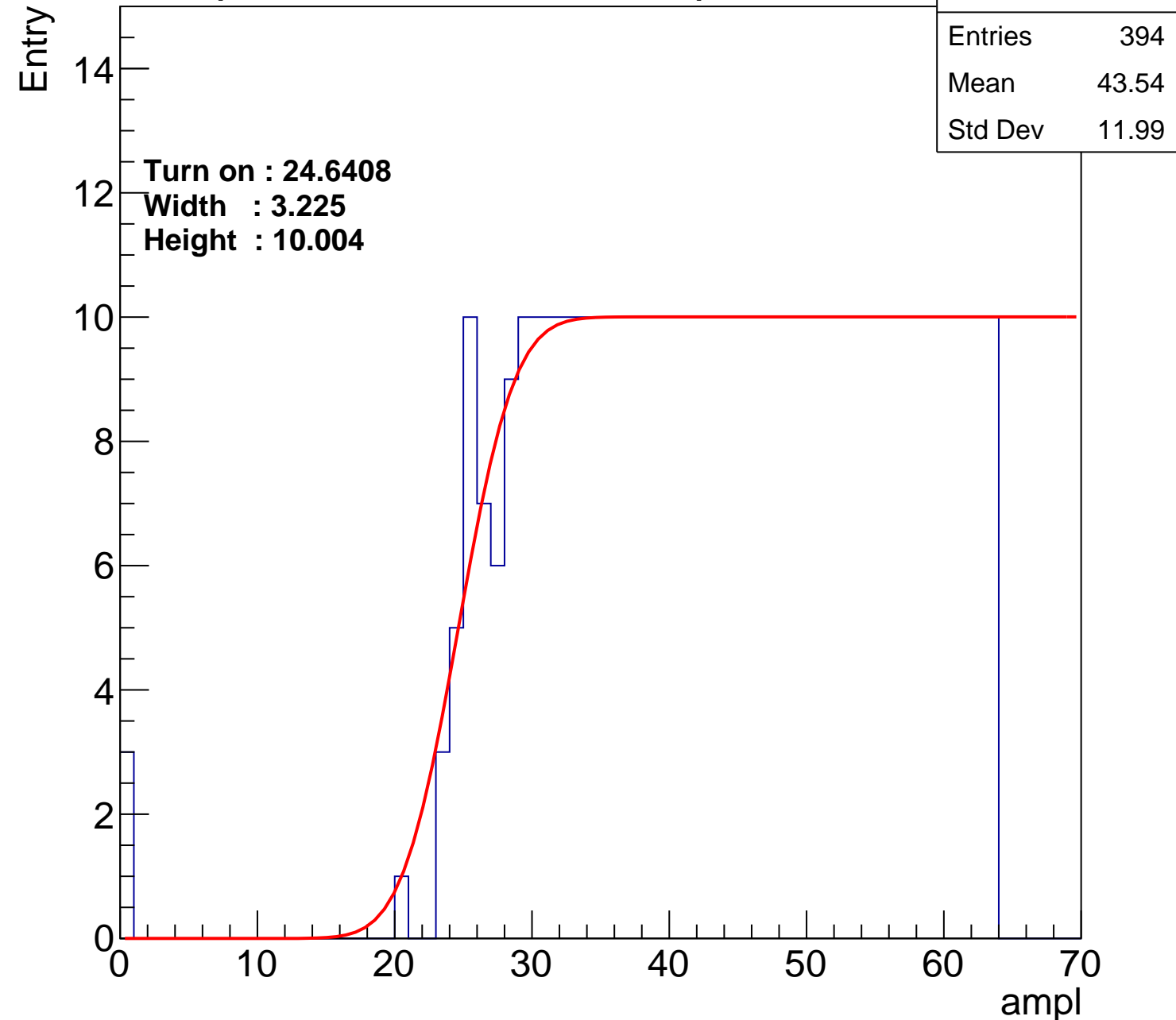
Width : 3.225

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch110

calib_packv5_042523_0143.root, FC#4, port A2

Entries	378
Mean	44.34
Std Dev	11.5

Turn on : 26.4528

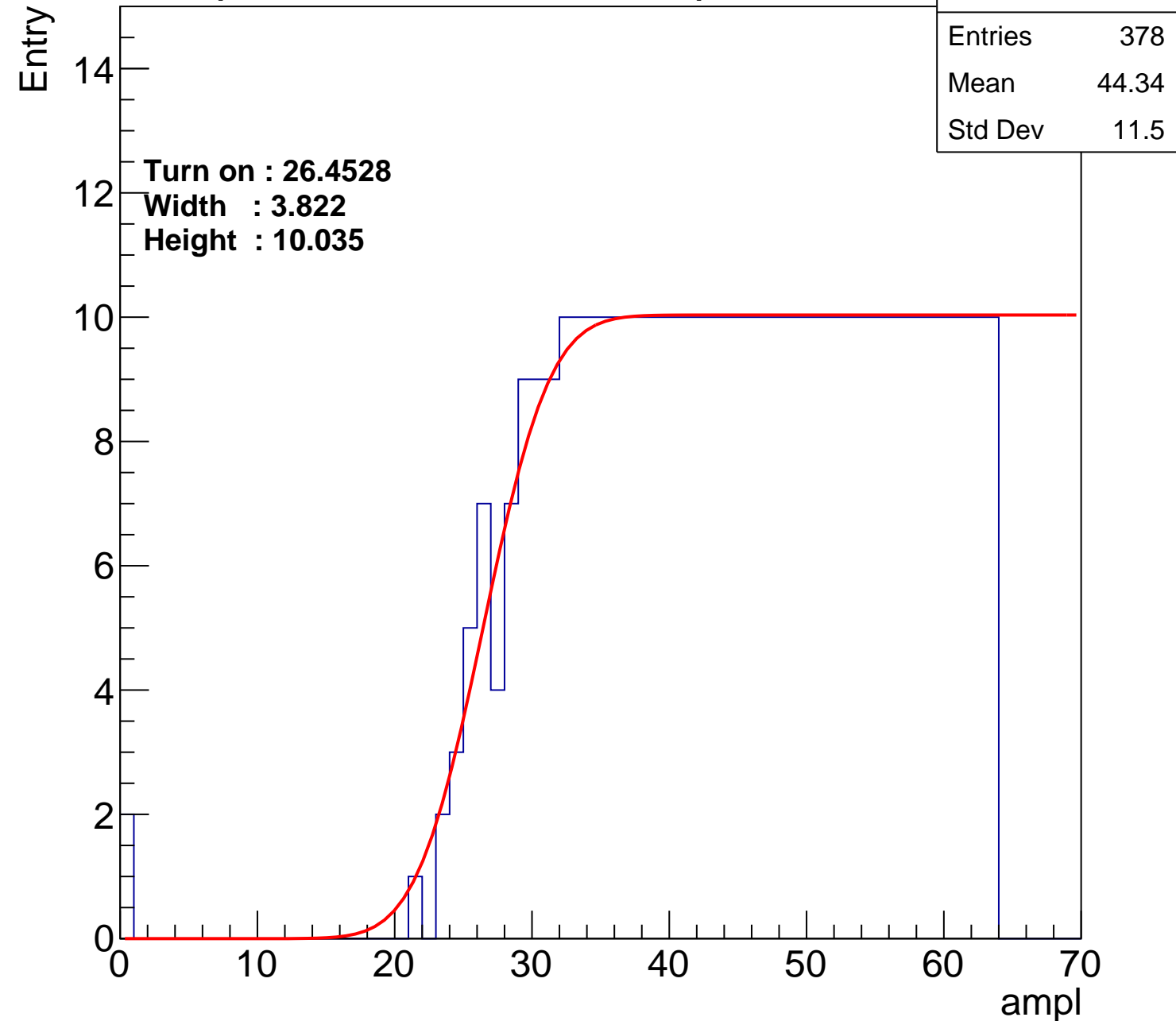
Width : 3.822

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch111

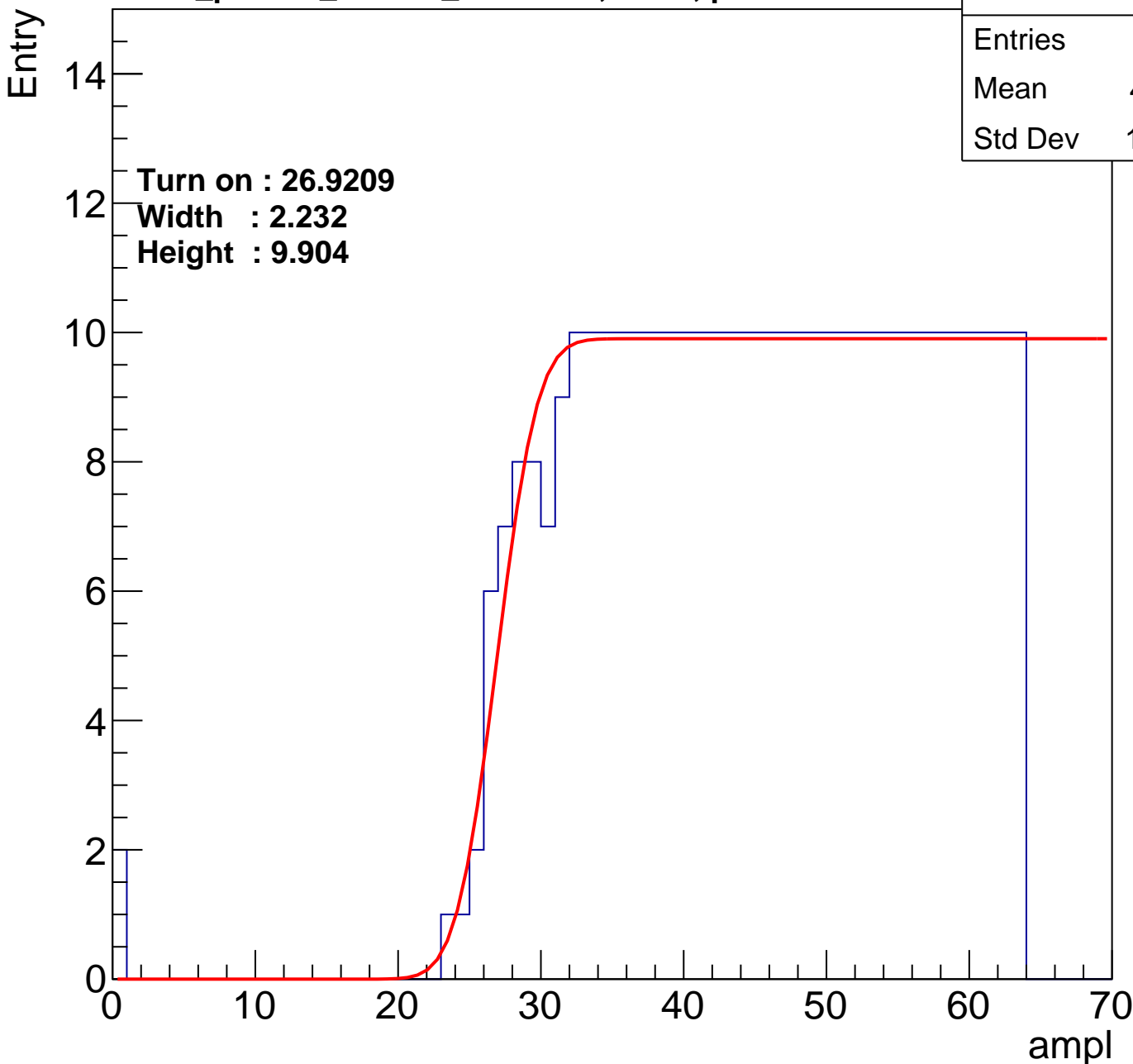
calib_packv5_042523_0143.root, FC#4, port A2

Entries	371
Mean	44.71
Std Dev	11.27

Turn on : 26.9209

Width : 2.232

Height : 9.904



B1L100S, U8-ch112

calib_packv5_042523_0143.root, FC#4, port A2

Entries	371
Mean	44.65
Std Dev	11.45

Turn on : 27.4967

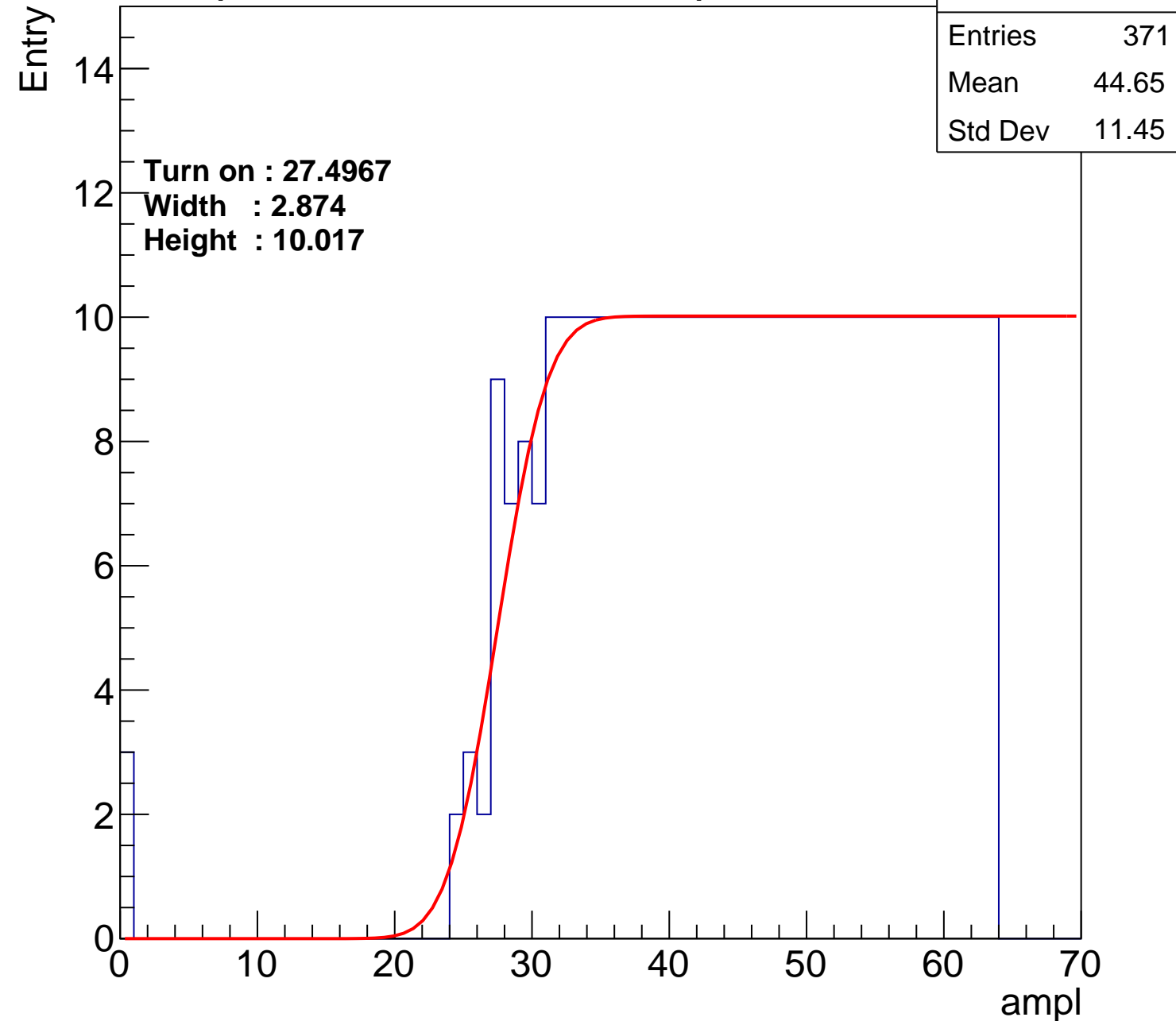
Width : 2.874

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch113

calib_packv5_042523_0143.root, FC#4, port A2

Entries	366
Mean	44.77
Std Dev	11.62

Turn on : 27.8166

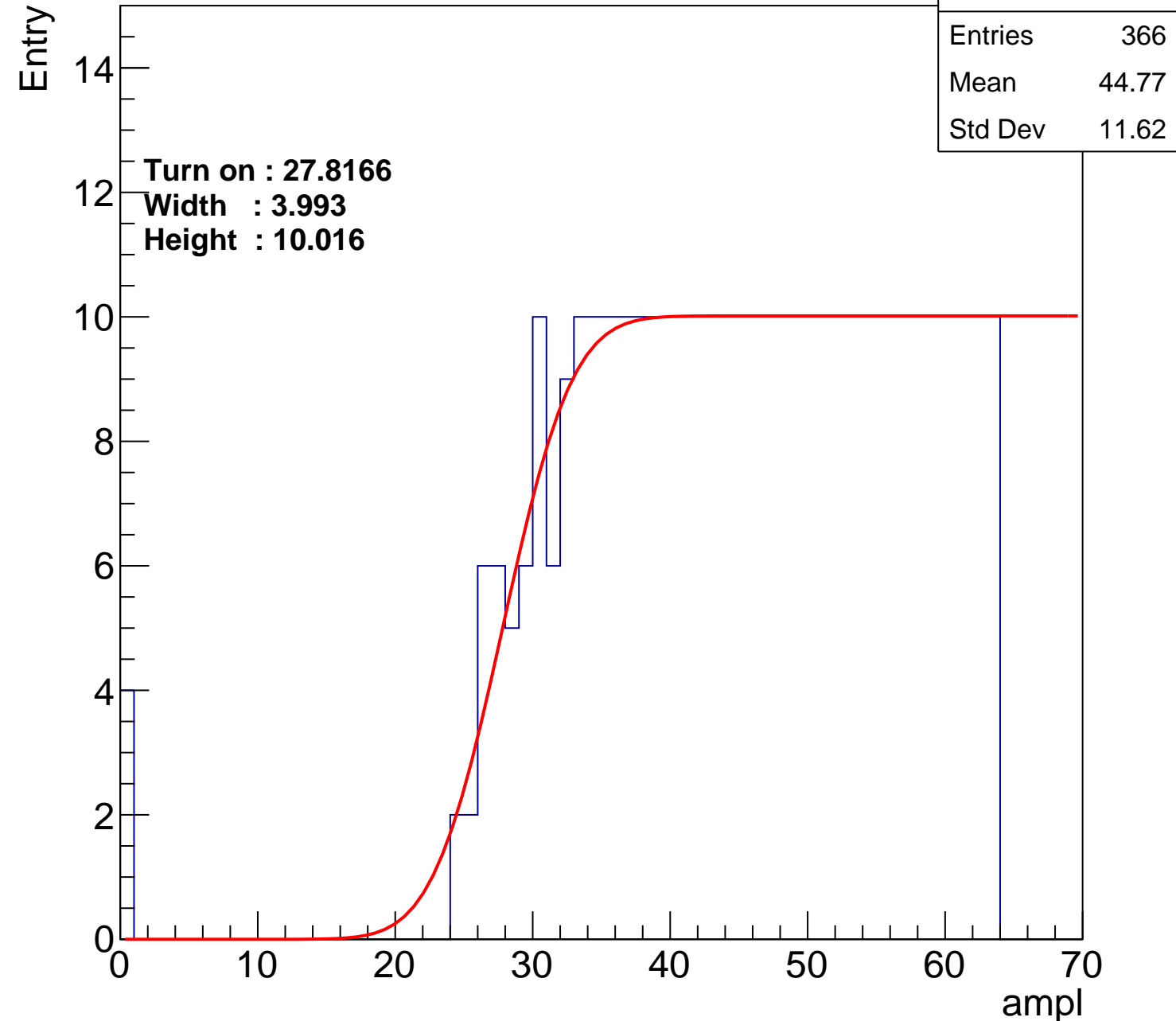
Width : 3.993

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch114

calib_packv5_042523_0143.root, FC#4, port A2

Entries	384
Mean	44.04
Std Dev	11.65

Turn on : 24.9579

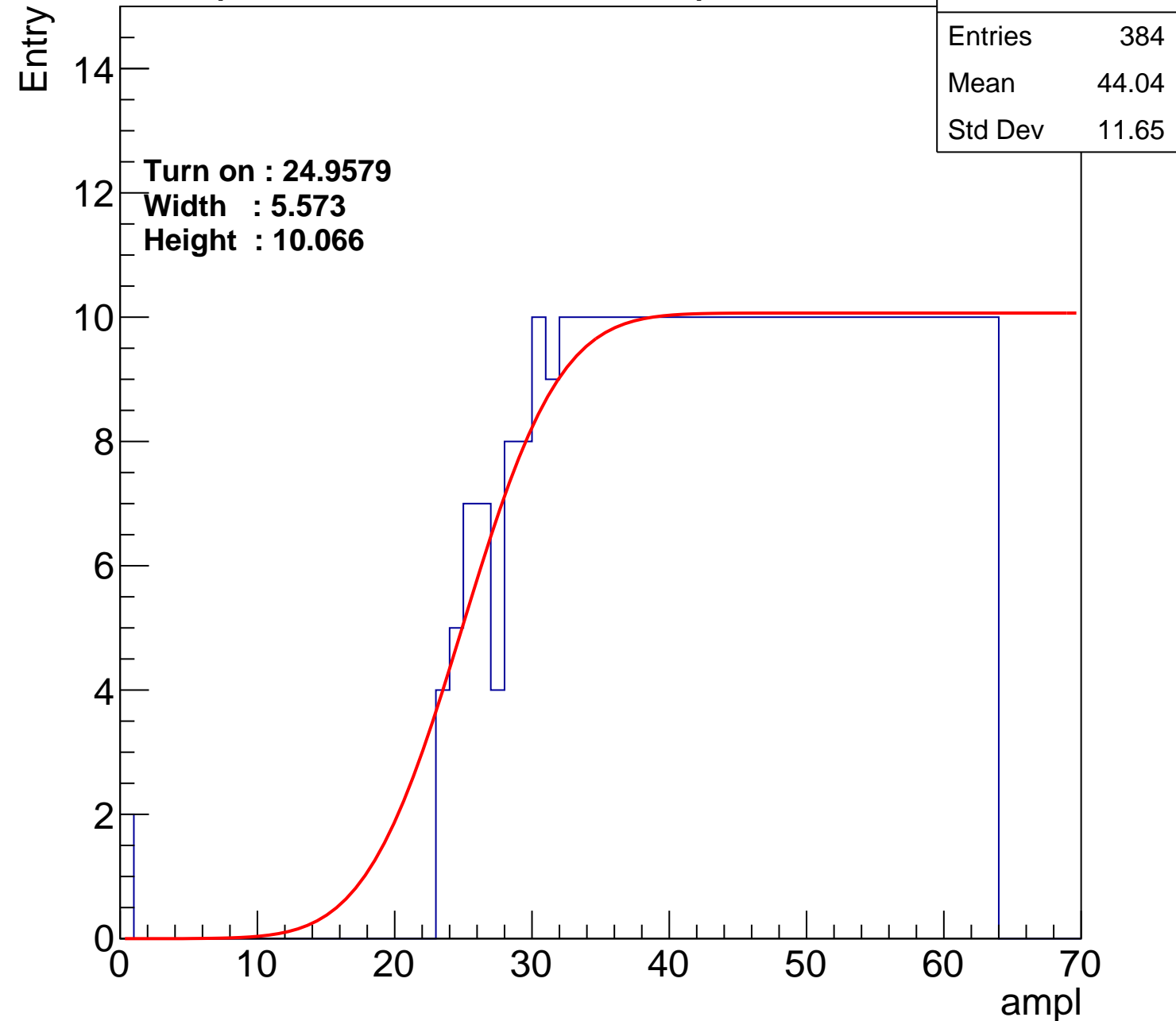
Width : 5.573

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch115

calib_packv5_042523_0143.root, FC#4, port A2

Entries	387
Mean	43.96
Std Dev	11.56

Turn on : 26.3402

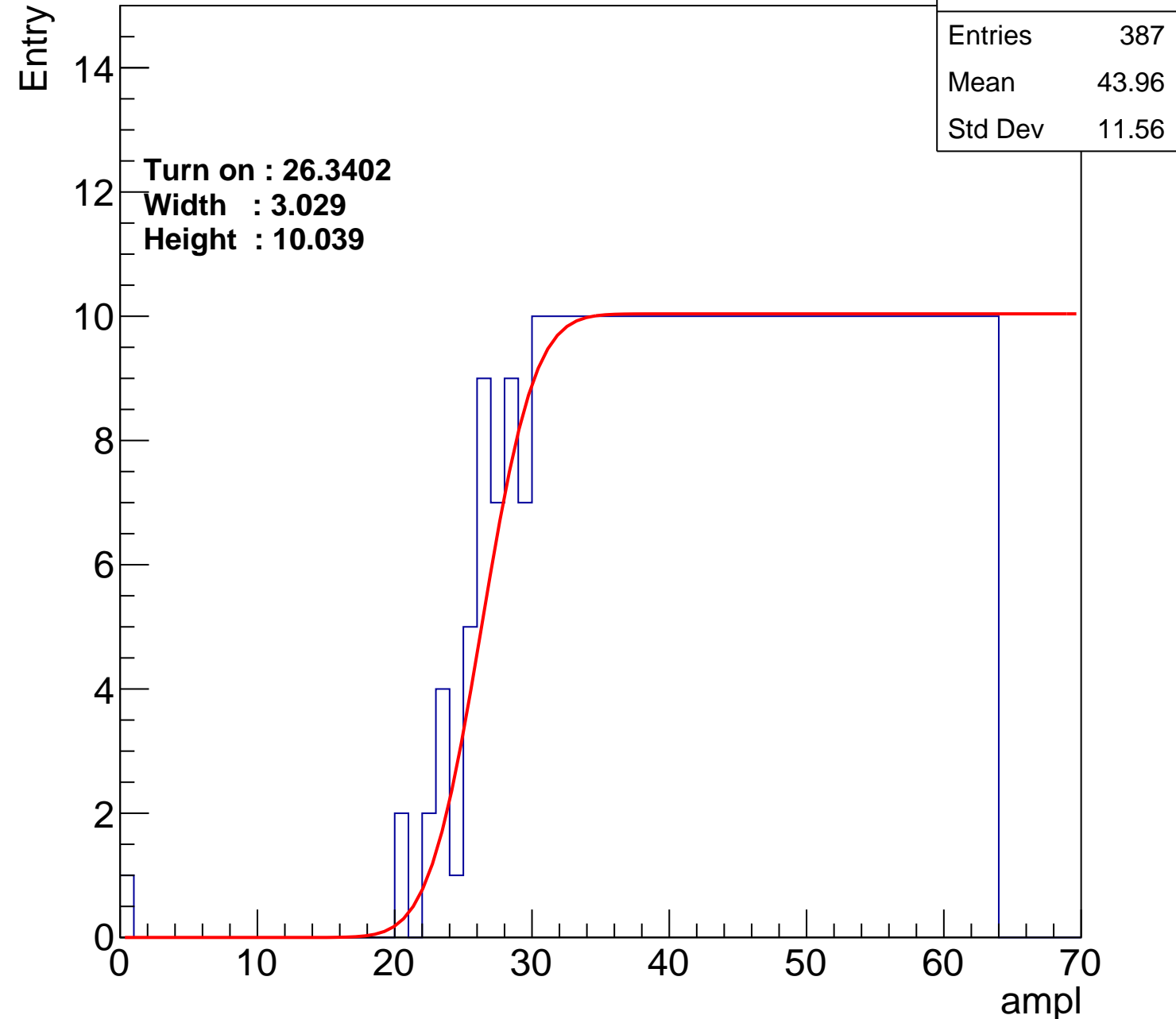
Width : 3.029

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch116

calib_packv5_042523_0143.root, FC#4, port A2

Entries	379
Mean	44.26
Std Dev	11.57

Turn on : 26.8947

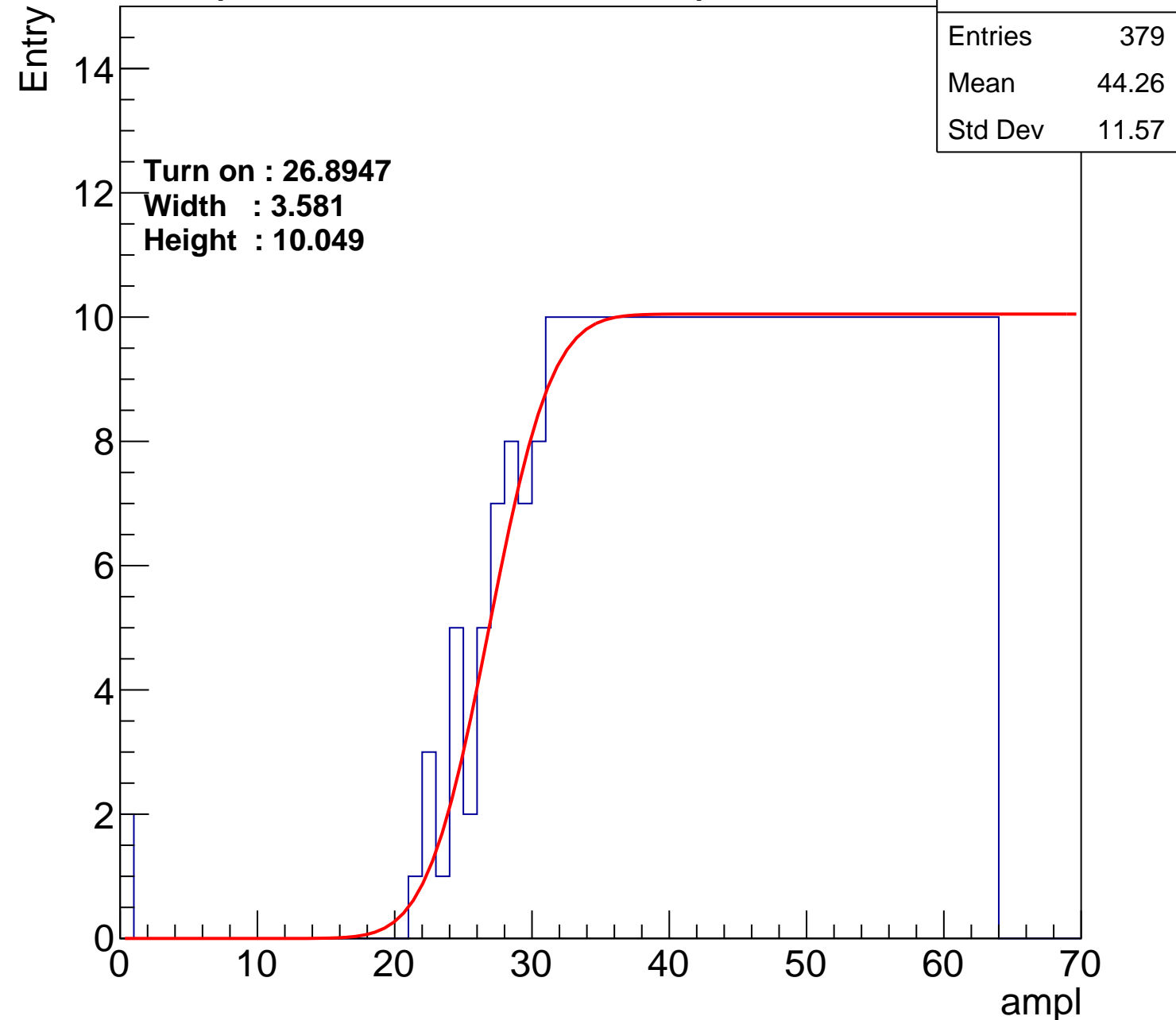
Width : 3.581

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch117

calib_packv5_042523_0143.root, FC#4, port A2

Entries	375
Mean	44.38
Std Dev	11.74

Turn on : 27.6215

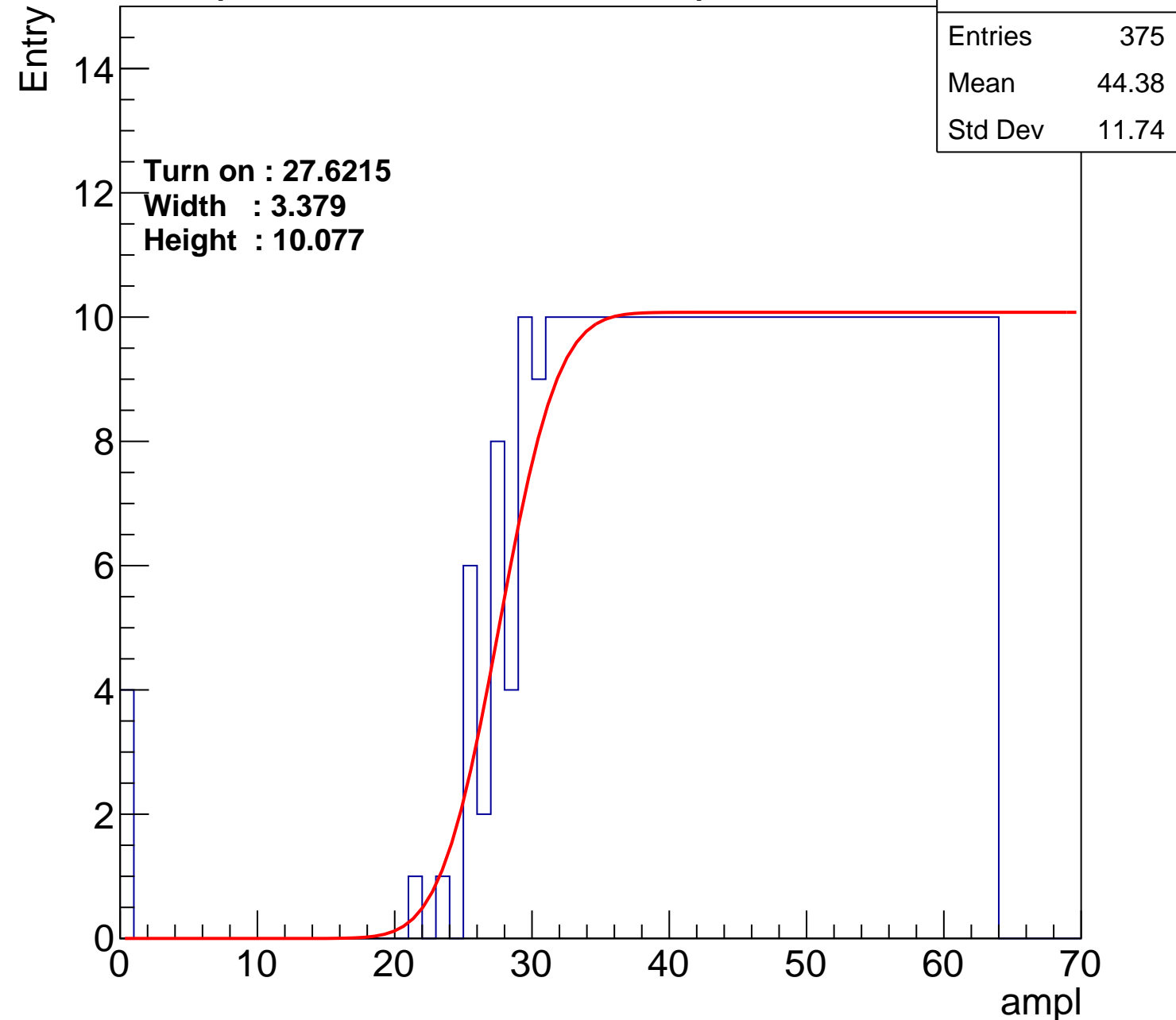
Width : 3.379

Height : 10.077

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch118

calib_packv5_042523_0143.root, FC#4, port A2

Entries	396
Mean	43.44
Std Dev	12.04

Turn on : 24.7531

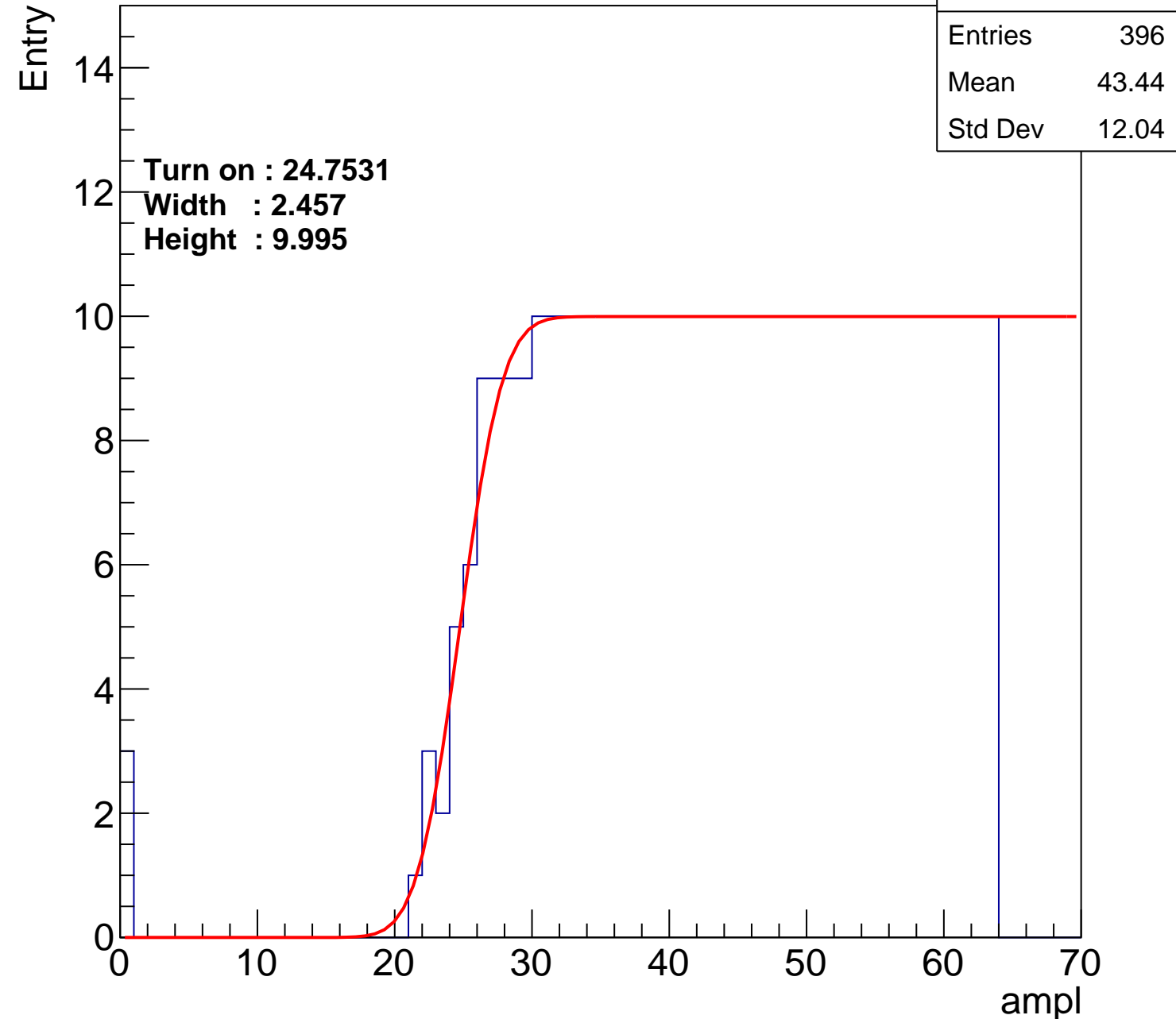
Width : 2.457

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch119

calib_packv5_042523_0143.root, FC#4, port A2

Entries	371
Mean	44.58
Std Dev	11.65

Turn on : 27.0513

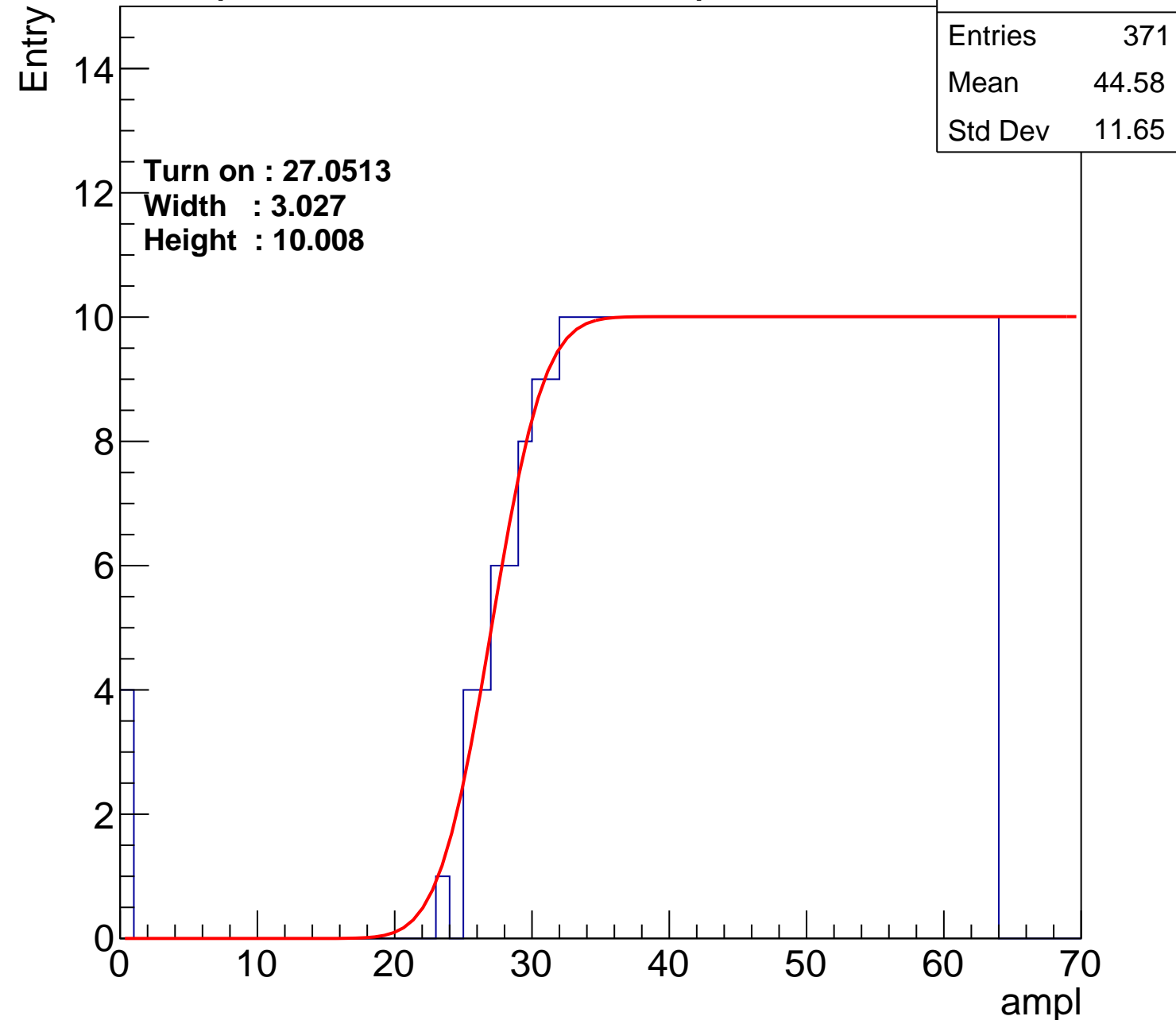
Width : 3.027

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch120

calib_packv5_042523_0143.root, FC#4, port A2

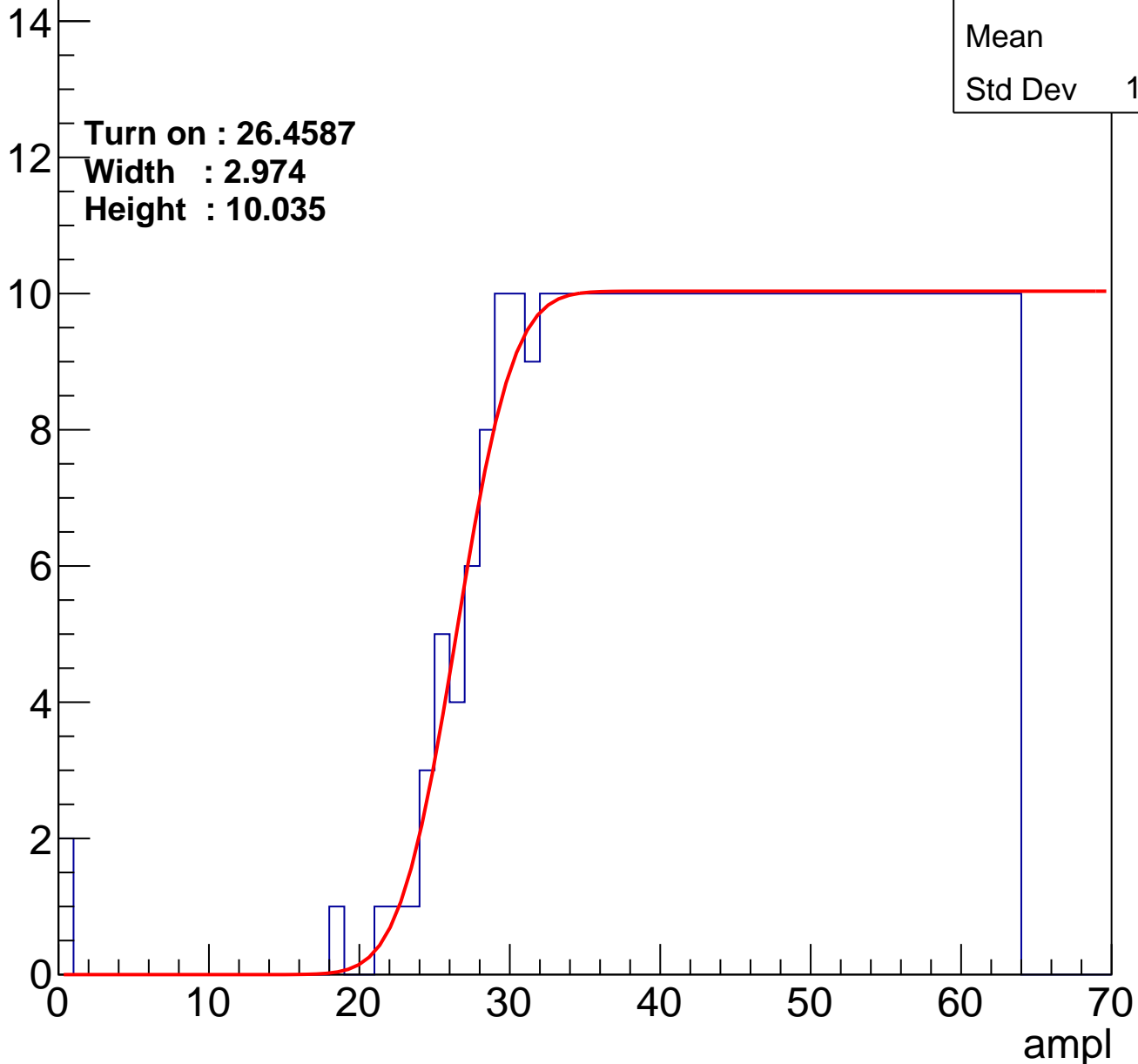
Entries	381
Mean	44.2
Std Dev	11.57

Turn on : 26.4587

Width : 2.974

Height : 10.035

Entry



B1L100S, U8-ch121

calib_packv5_042523_0143.root, FC#4, port A2

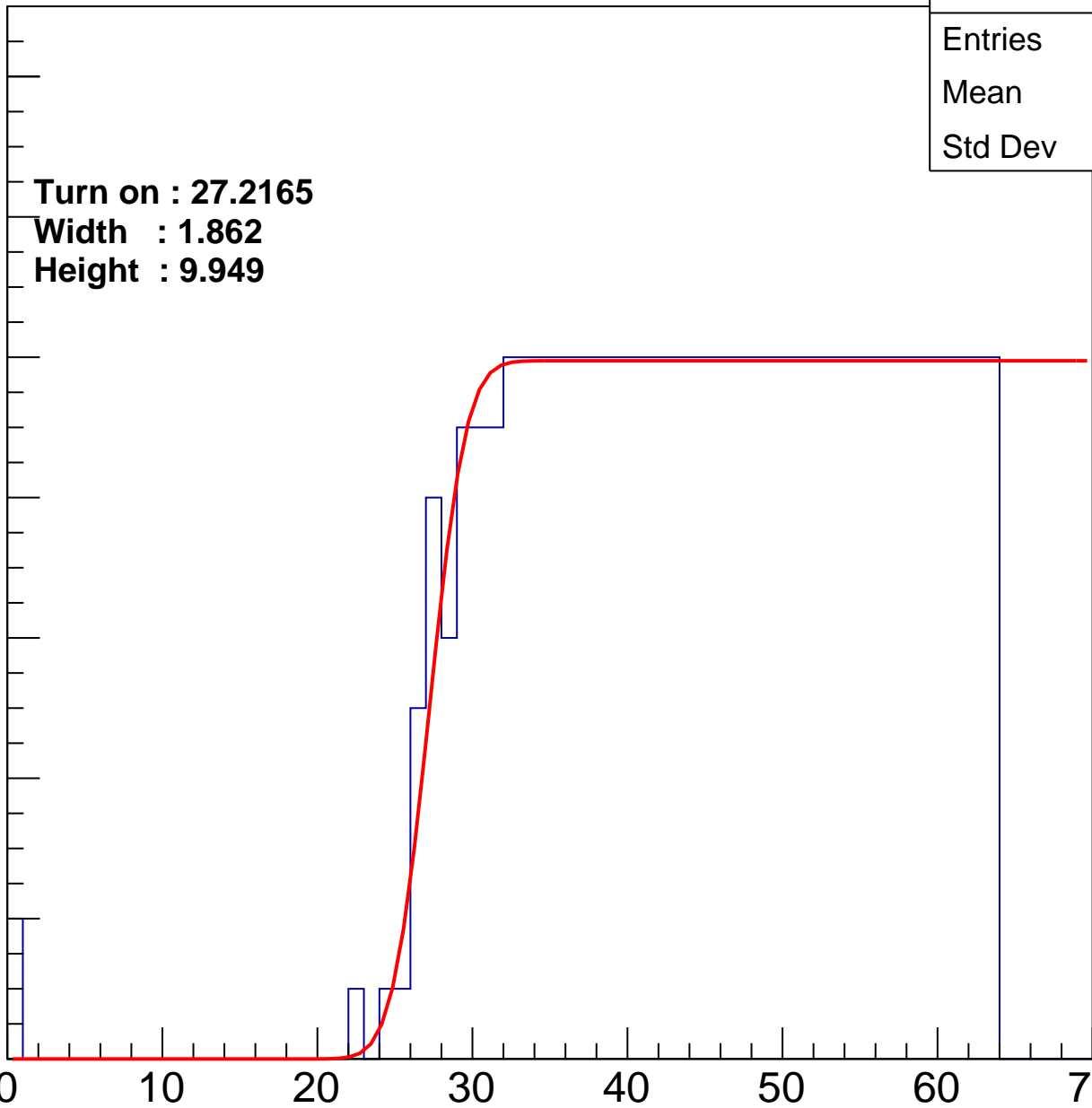
Entry

14
12
10
8
6
4
2
0

Turn on : 27.2165
Width : 1.862
Height : 9.949

Entries	371
Mean	44.73
Std Dev	11.24

ampl



B1L100S, U8-ch122

calib_packv5_042523_0143.root, FC#4, port A2

Entries	397
Mean	43.4
Std Dev	11.99

Turn on : 24.4791

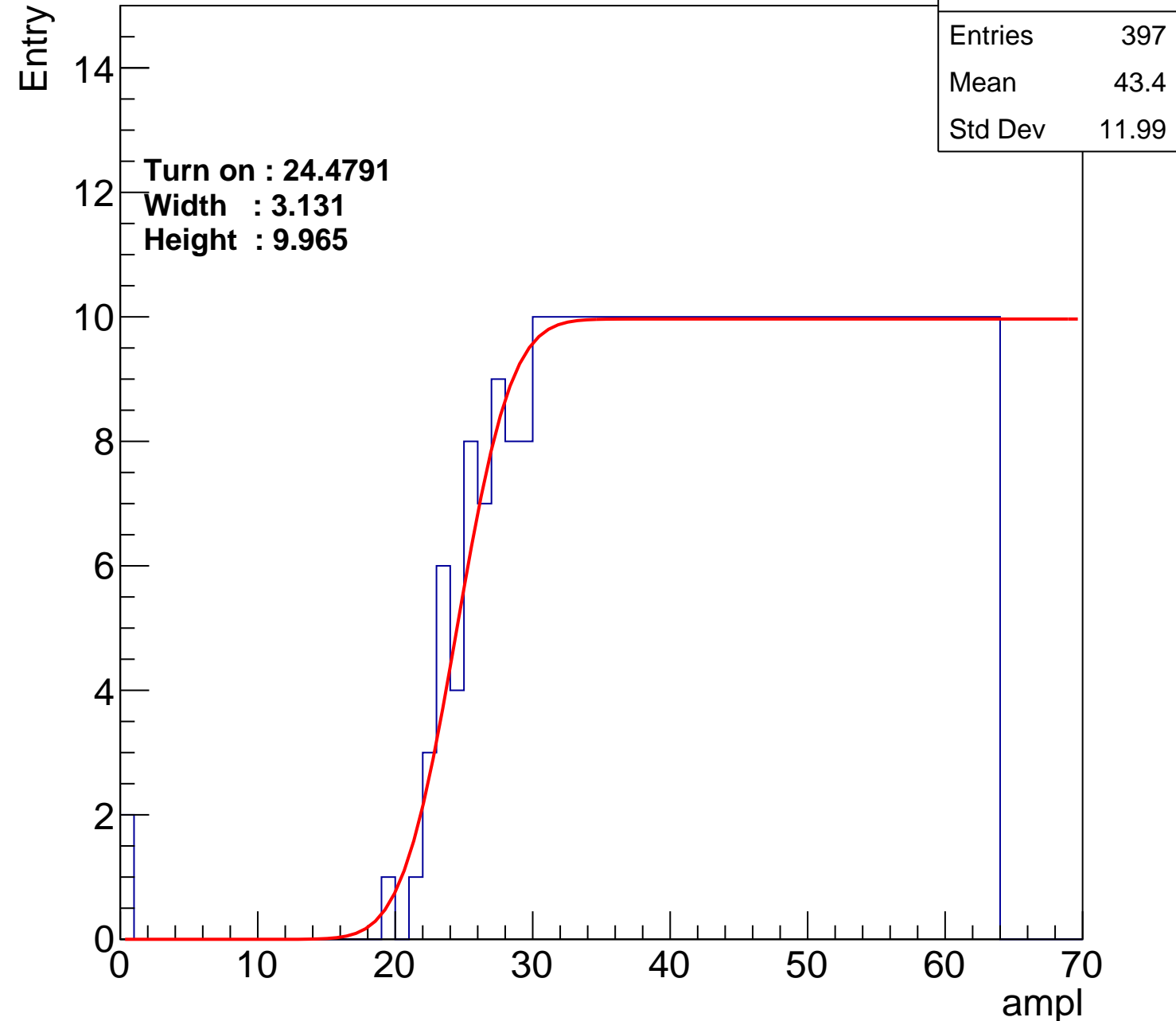
Width : 3.131

Height : 9.965

Entry

14
12
10
8
6
4
2
0

ampl

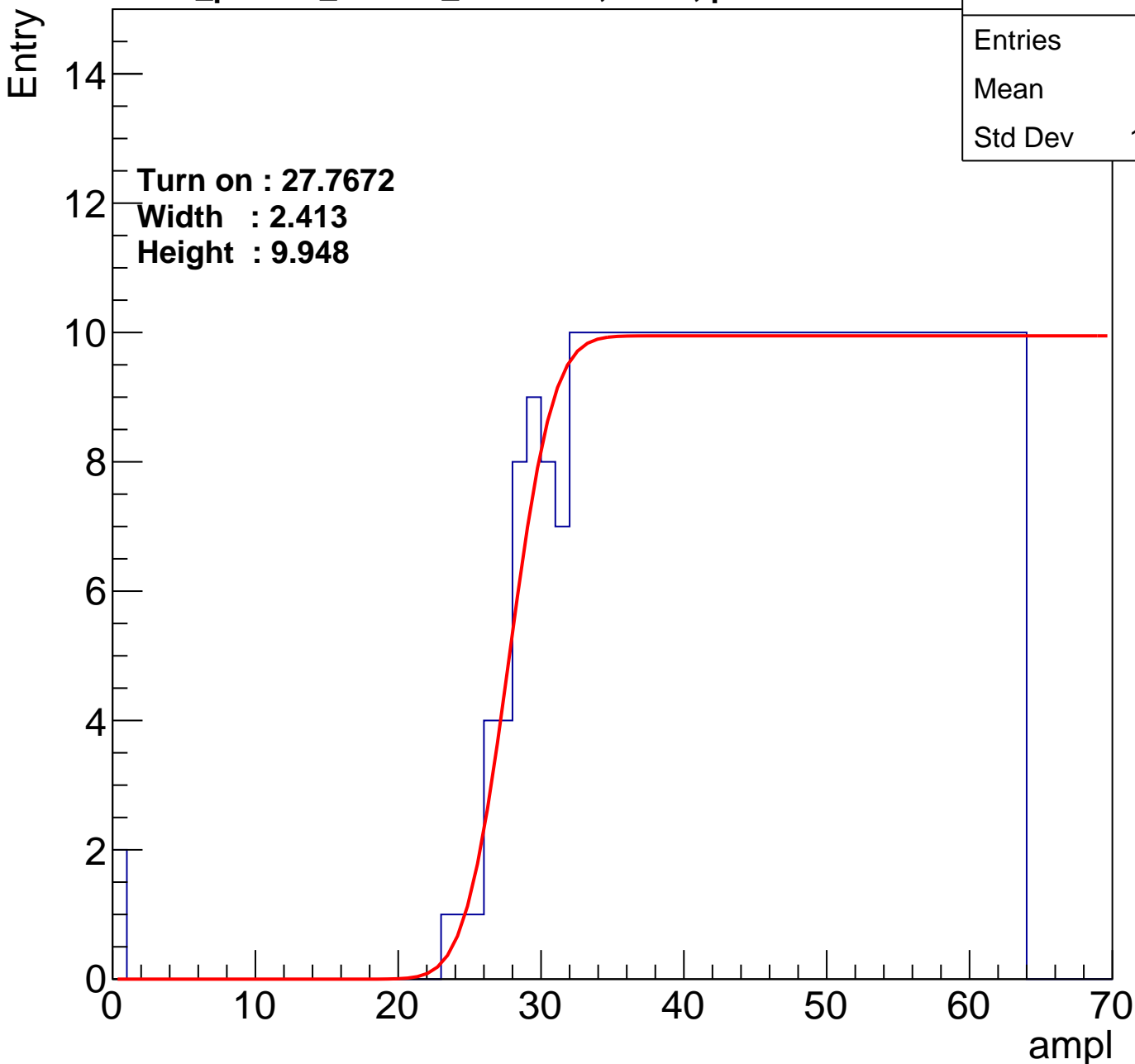


calib_packv5_042523_0143.root, FC#4, port A2

calib_packv5_042523_0143.root, FC#4, port A2

Entries	365
Mean	45
Std Dev	11.13

Height : 9.948



B1L100S, U8-ch124

calib_packv5_042523_0143.root, FC#4, port A2

Entries	372
Mean	44.59
Std Dev	11.51

Turn on : 27.2611

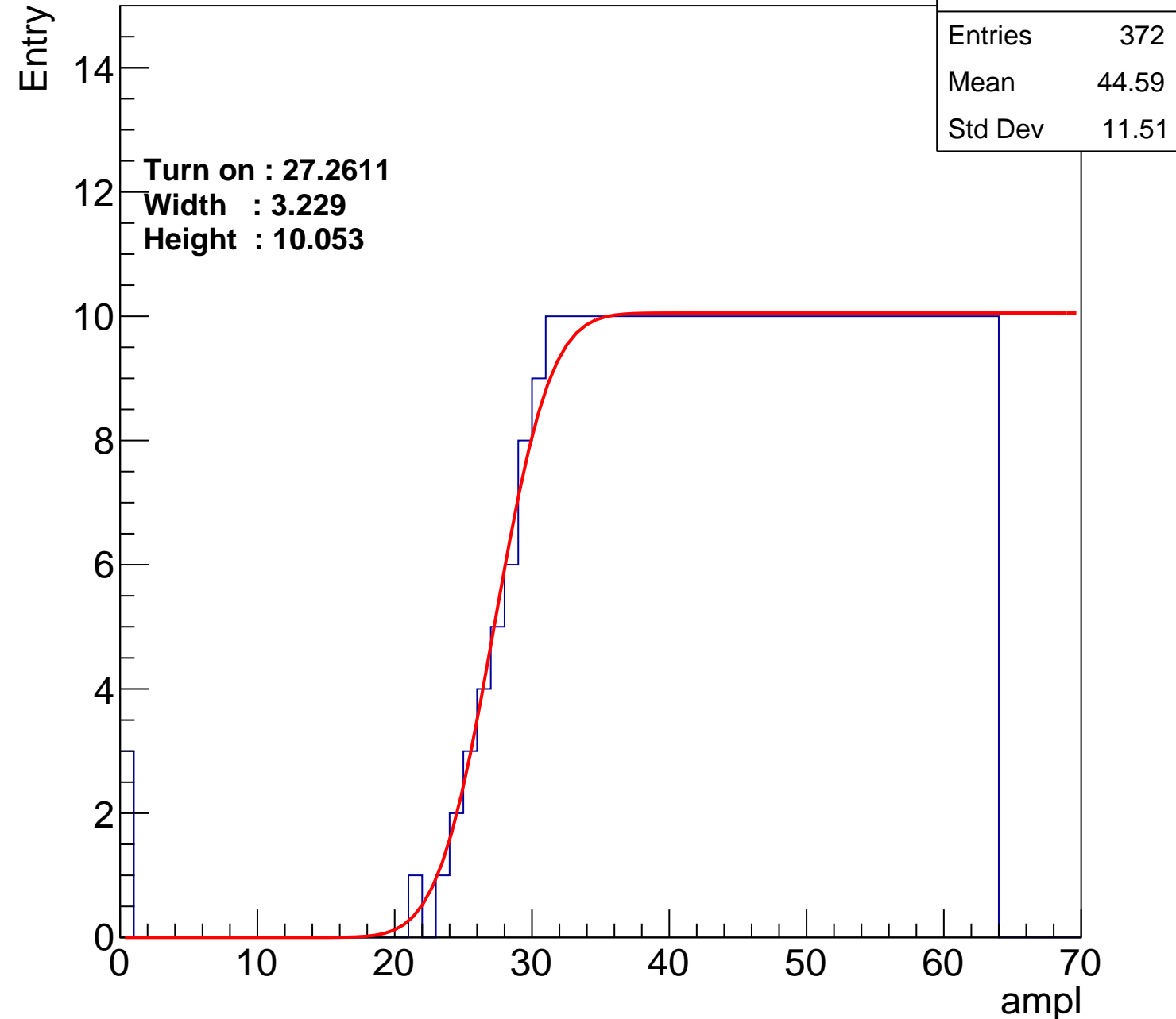
Width : 3.229

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch125

calib_packv5_042523_0143.root, FC#4, port A2

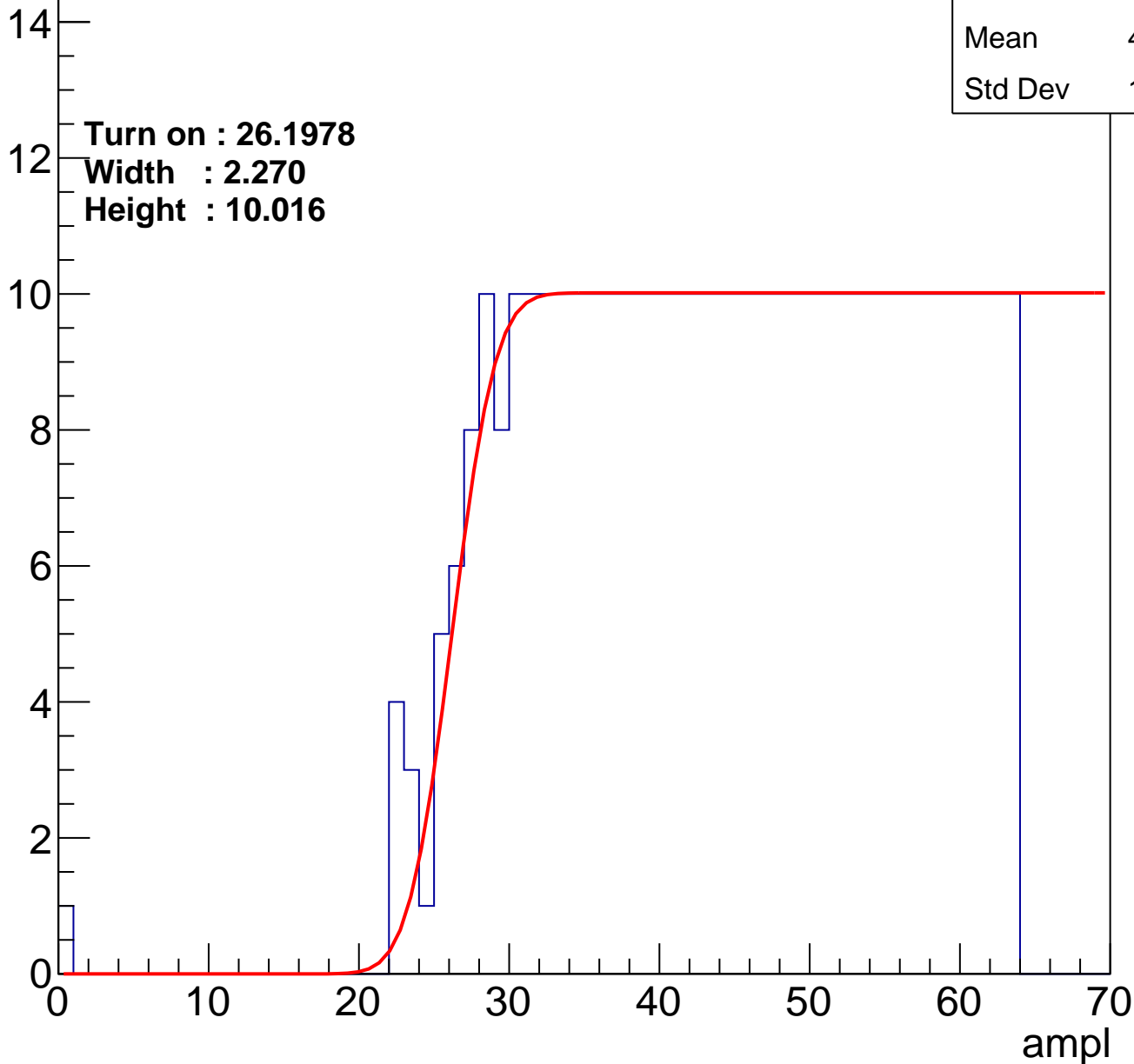
Entries	386
Mean	44.04
Std Dev	11.48

Turn on : 26.1978

Width : 2.270

Height : 10.016

Entry



B1L100S, U8-ch126

calib_packv5_042523_0143.root, FC#4, port A2

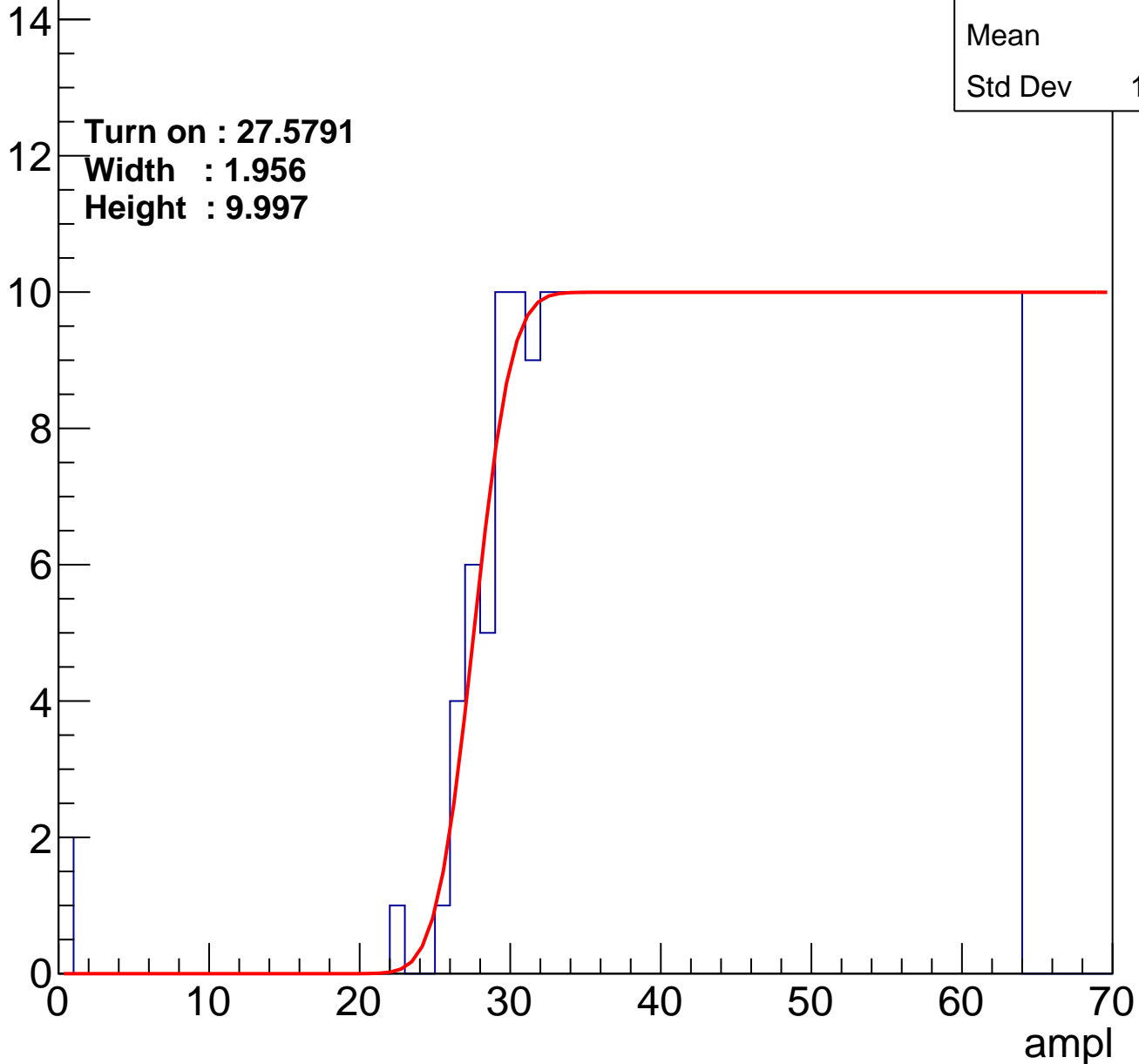
Entries	368
Mean	44.9
Std Dev	11.14

Turn on : 27.5791

Width : 1.956

Height : 9.997

Entry



B1L100S, U8-ch127

calib_packv5_042523_0143.root, FC#4, port A2

Entries	369
Mean	44.84
Std Dev	11.16

Turn on : 27.4106

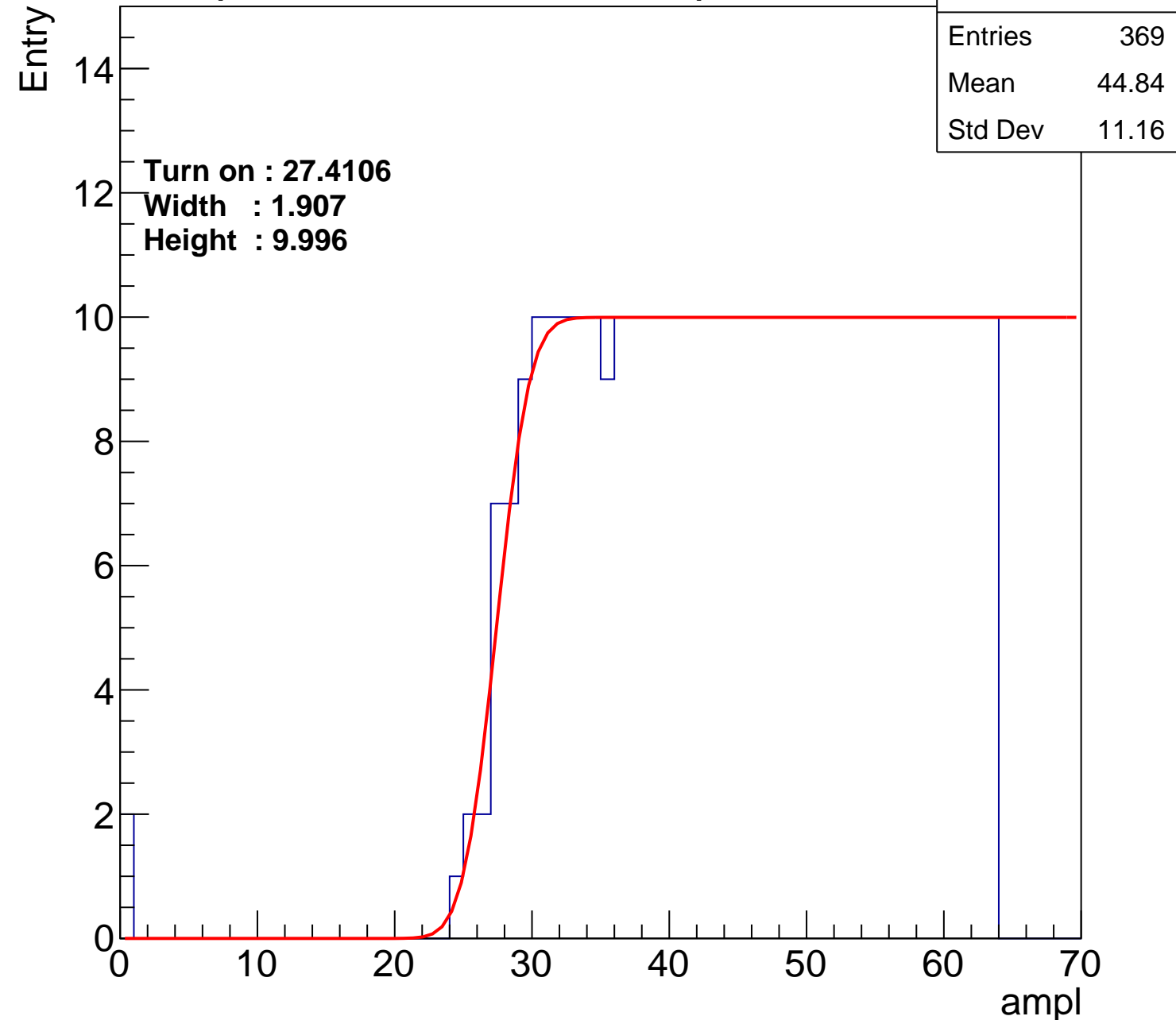
Width : 1.907

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl



B1L100S, U8-ch127

calib_packv5_042523_0143.root, FC#4, port A2

Entries	369
Mean	44.84
Std Dev	11.16

Turn on : 27.4106

Width : 1.907

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl

