



# B1L103S, U20-ch0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	470
Mean	37.28
Std Dev	18.31

Turn on : 23.0900

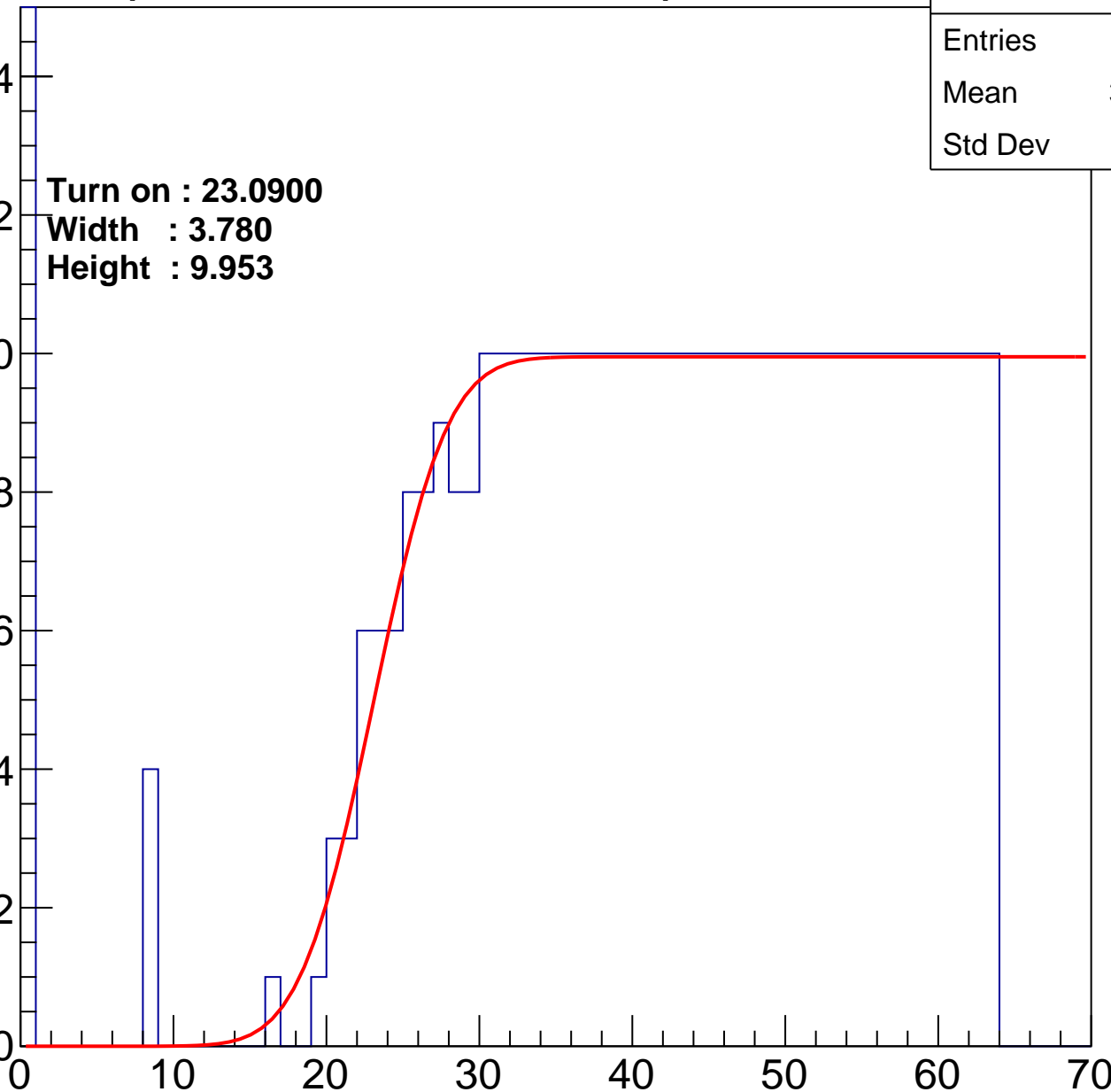
Width : 3.780

Height : 9.953

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	406
Mean	40.57
Std Dev	16.99

Turn on : 27.7403

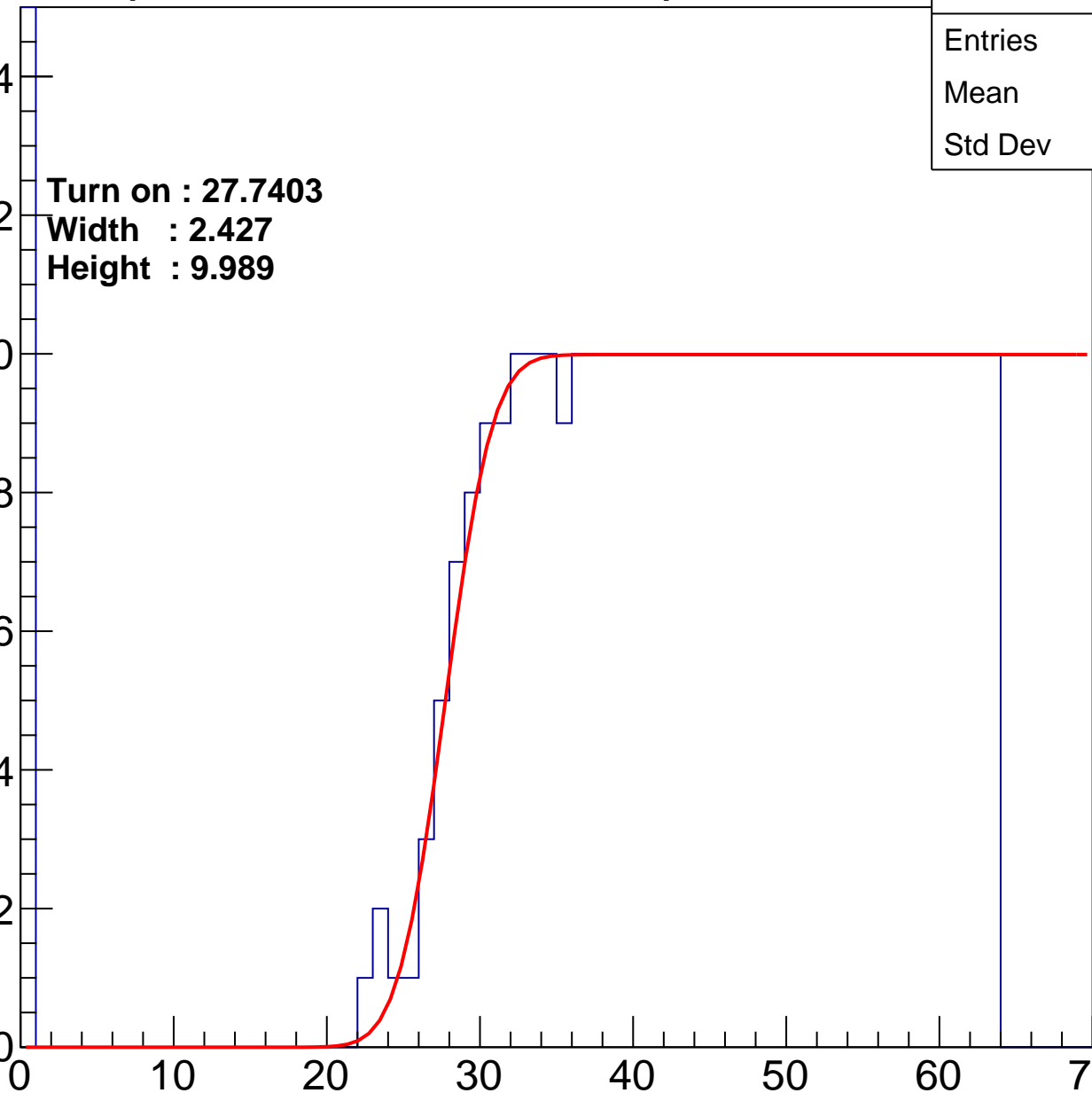
Width : 2.427

Height : 9.989

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	430
Mean	39.46
Std Dev	17.33

**Turn on : 25.9084**

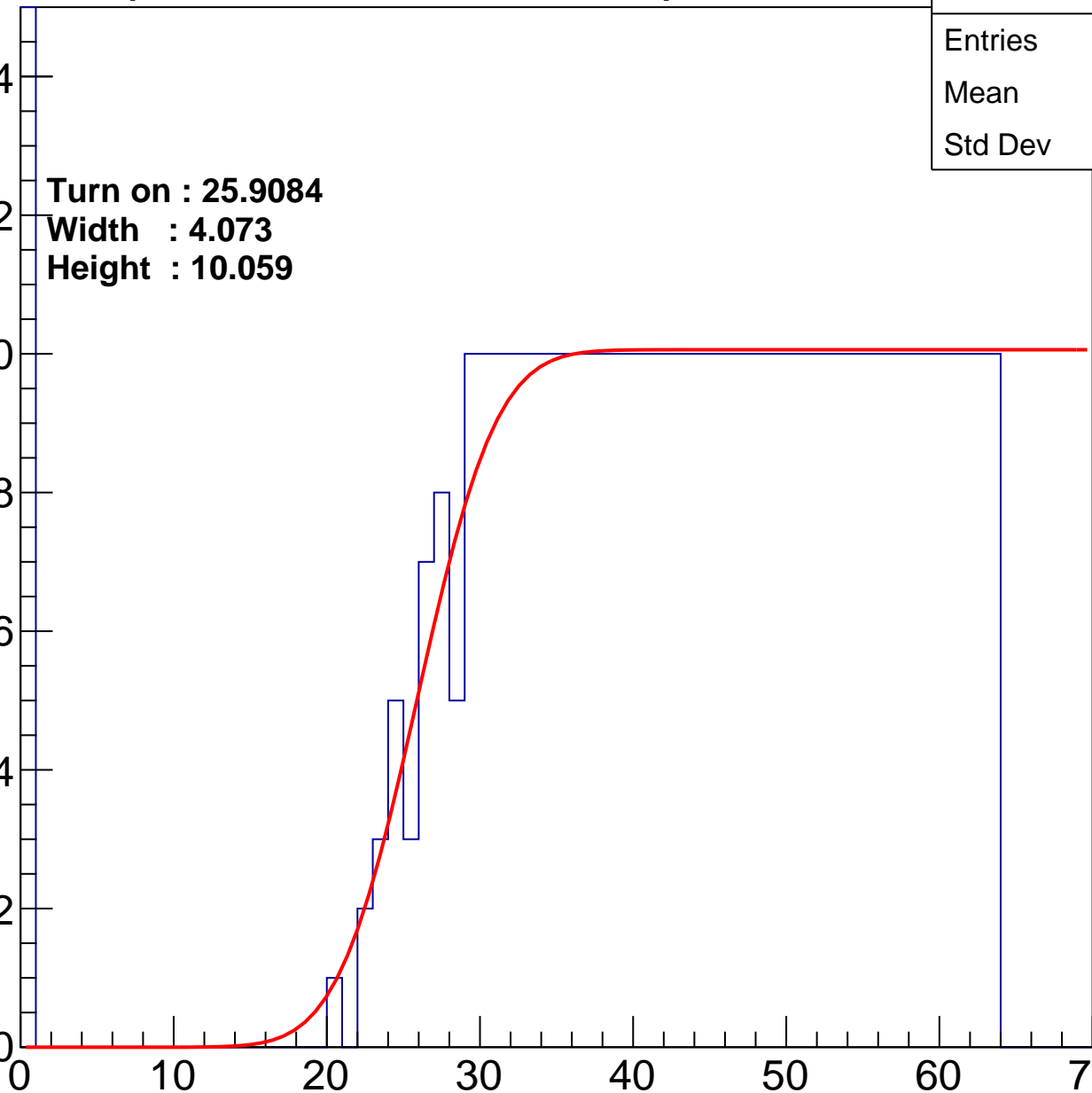
**Width : 4.073**

**Height : 10.059**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	403
Mean	40.56
Std Dev	17.2

Turn on : 27.7111

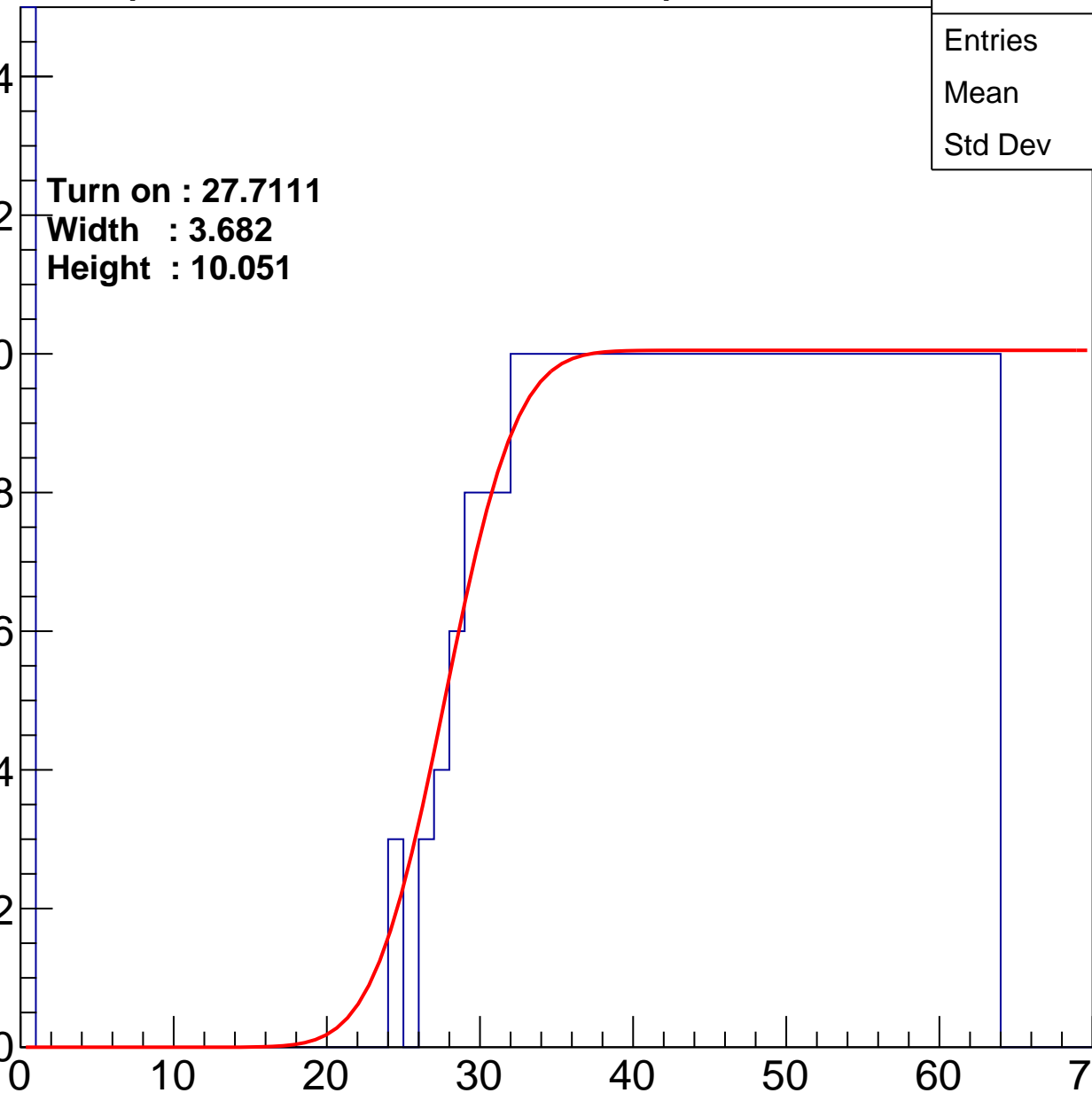
Width : 3.682

Height : 10.051

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	447
Mean	38.96
Std Dev	17.11

Turn on : 23.9463

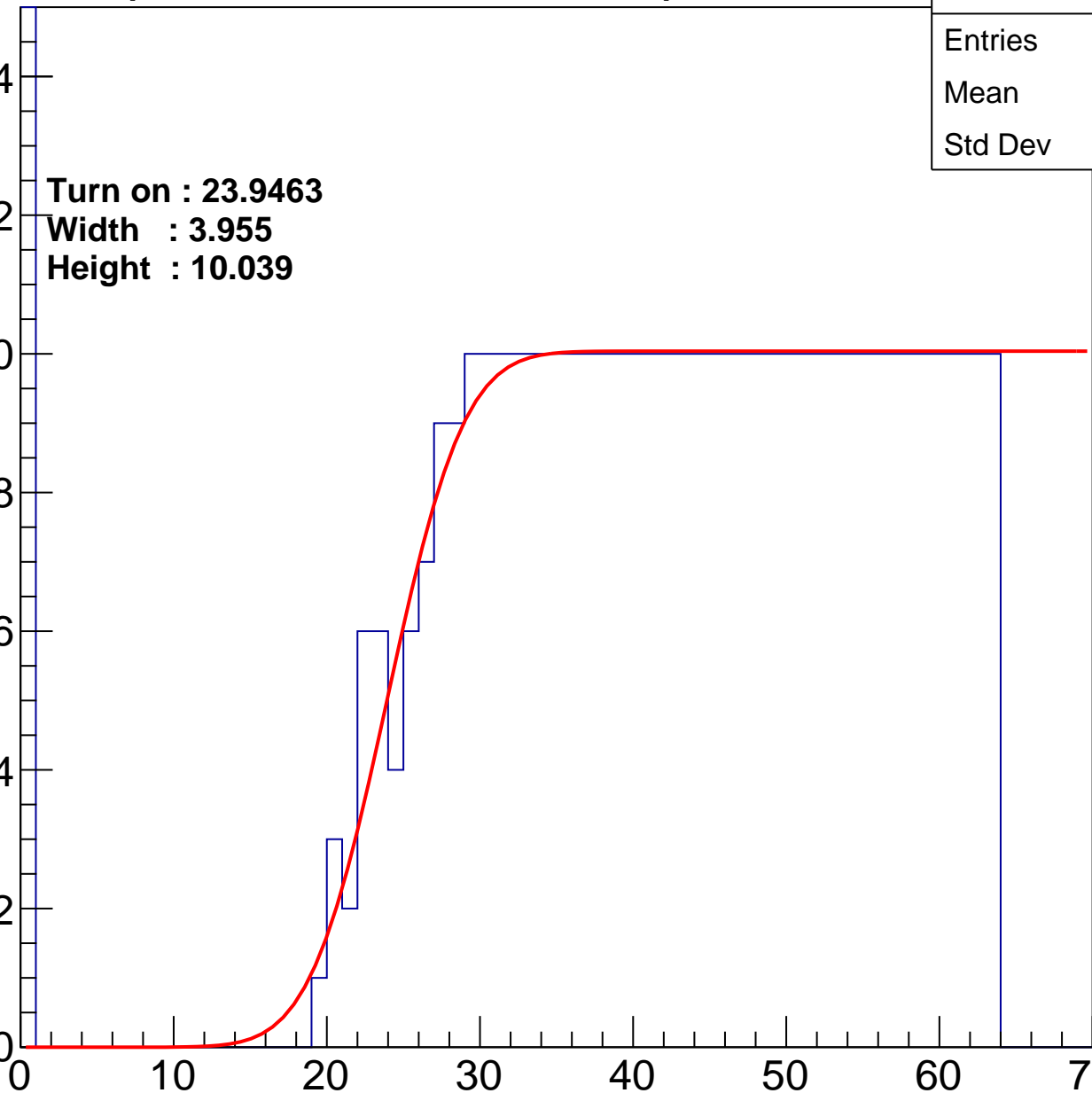
Width : 3.955

Height : 10.039

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	409
Mean	40.84
Std Dev	16.34

**Turn on : 26.4913**

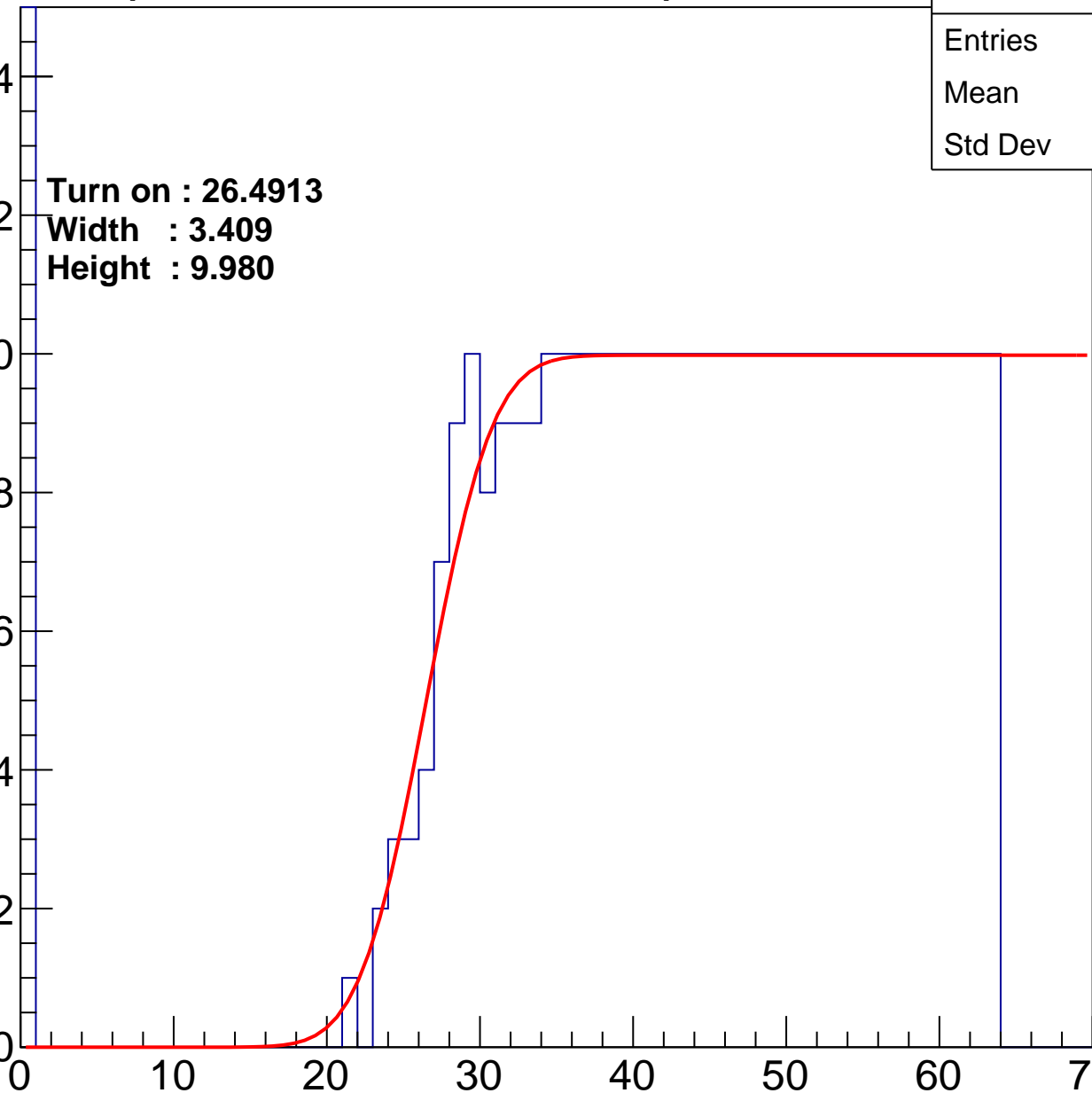
**Width : 3.409**

**Height : 9.980**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	420
Mean	40.45
Std Dev	16.32

**Turn on : 26.4193**

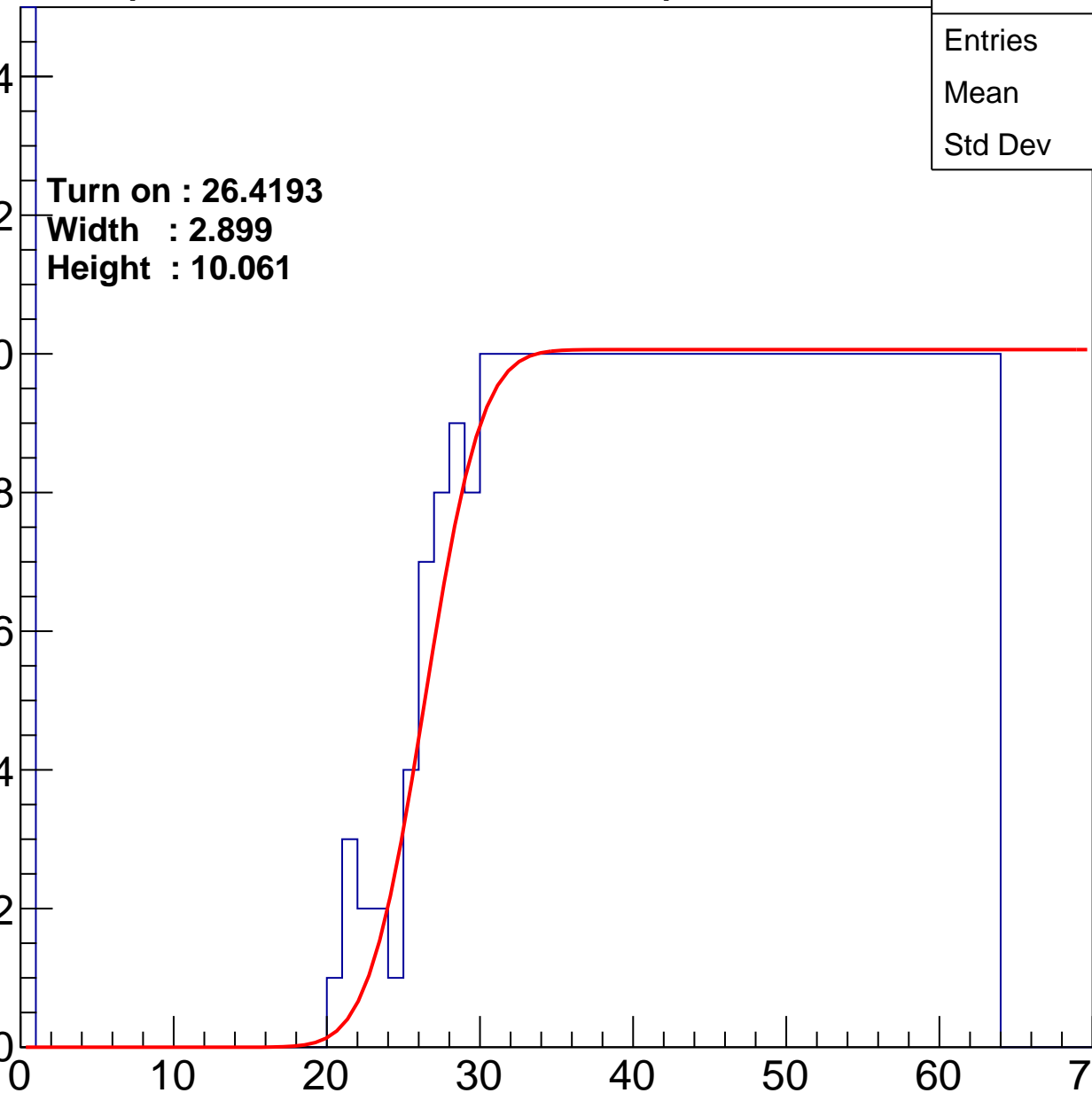
**Width : 2.899**

**Height : 10.061**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U20-ch7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	417
Mean	40.7
Std Dev	16.09

Turn on : 25.6013

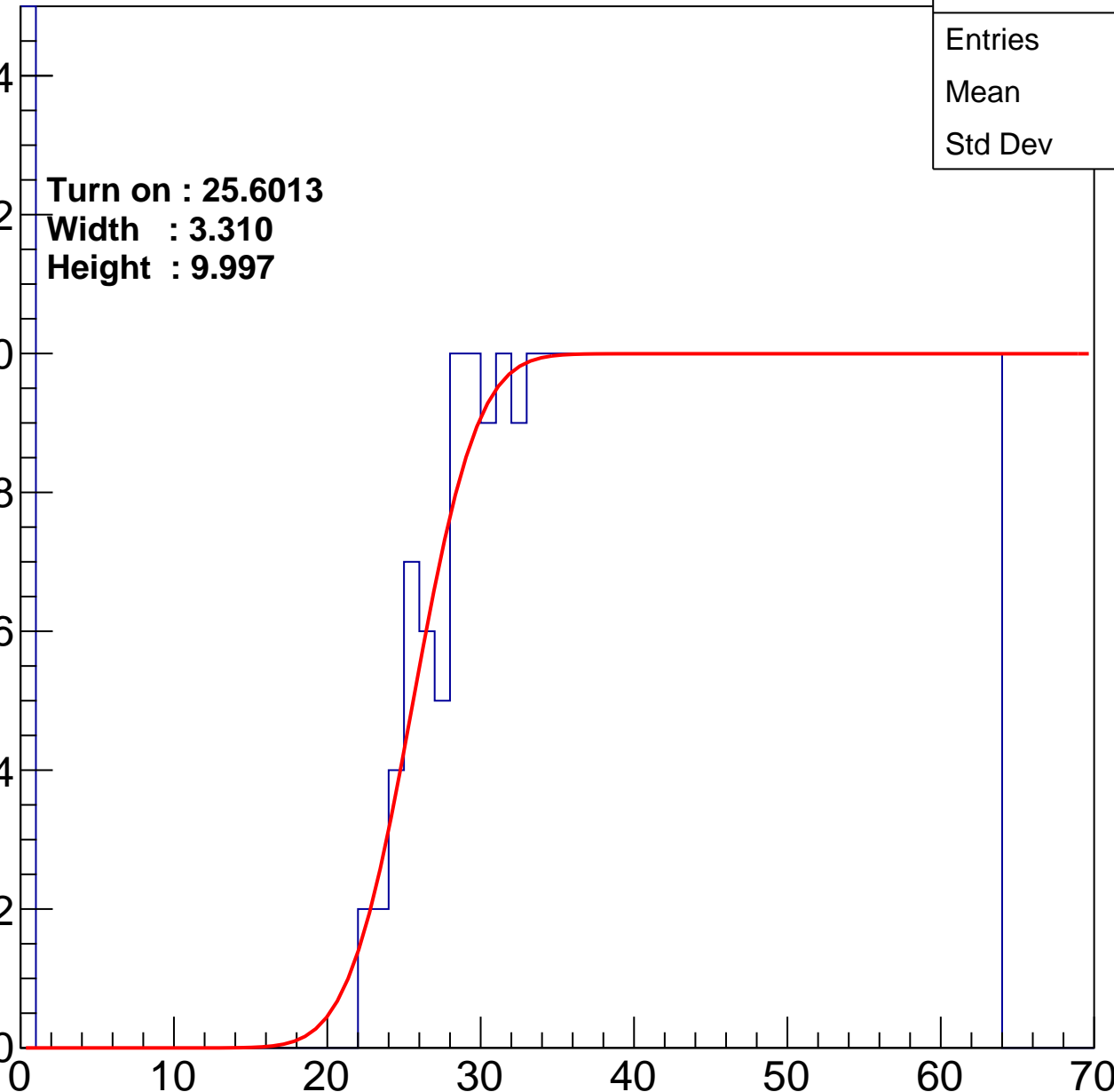
Width : 3.310

Height : 9.997

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch8

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	433
Mean	39.66
Std Dev	16.84

Turn on : 24.7204

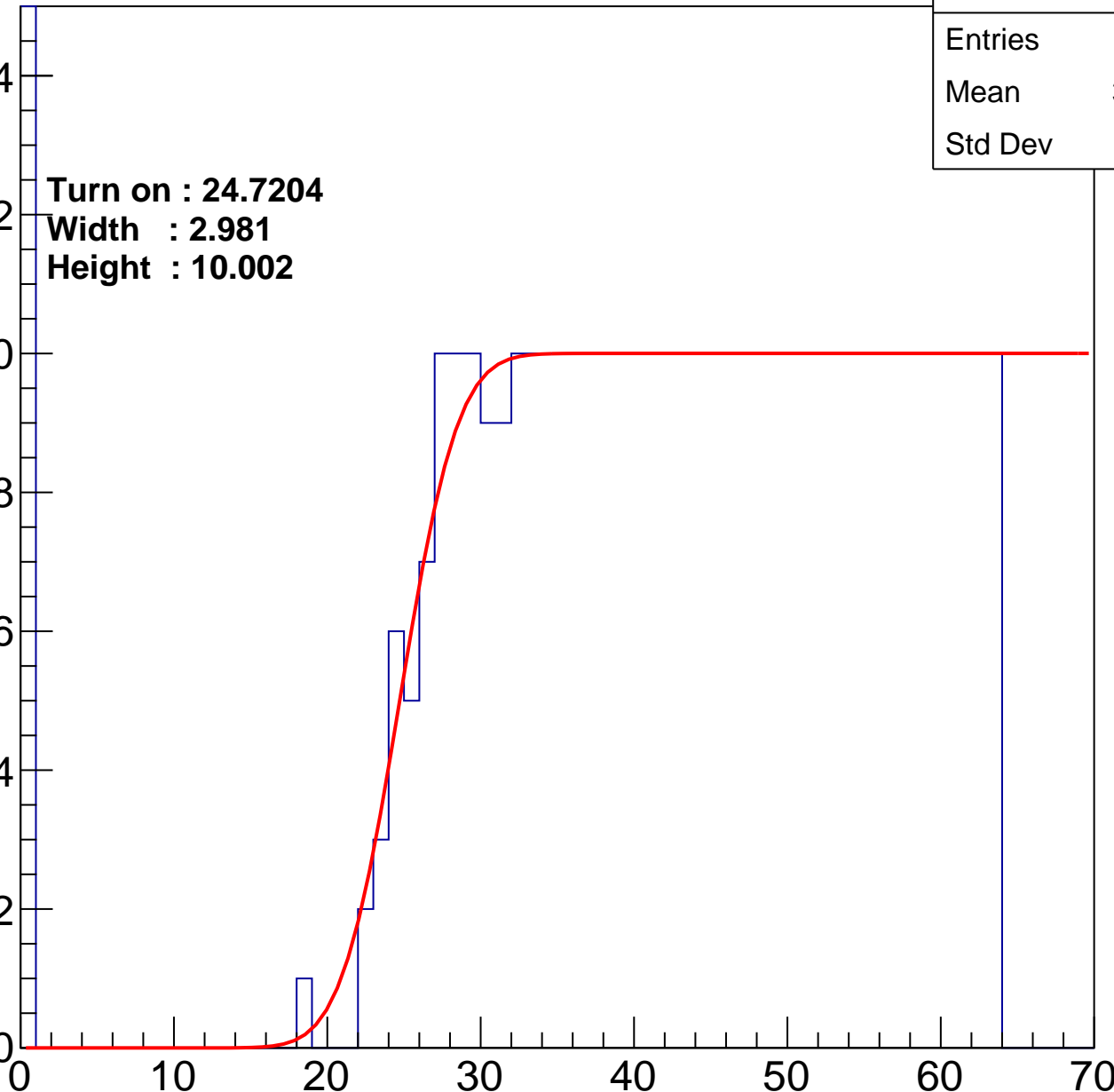
Width : 2.981

Height : 10.002

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch9

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	400
Mean	41.01
Std Dev	16.68

Turn on : 28.0705

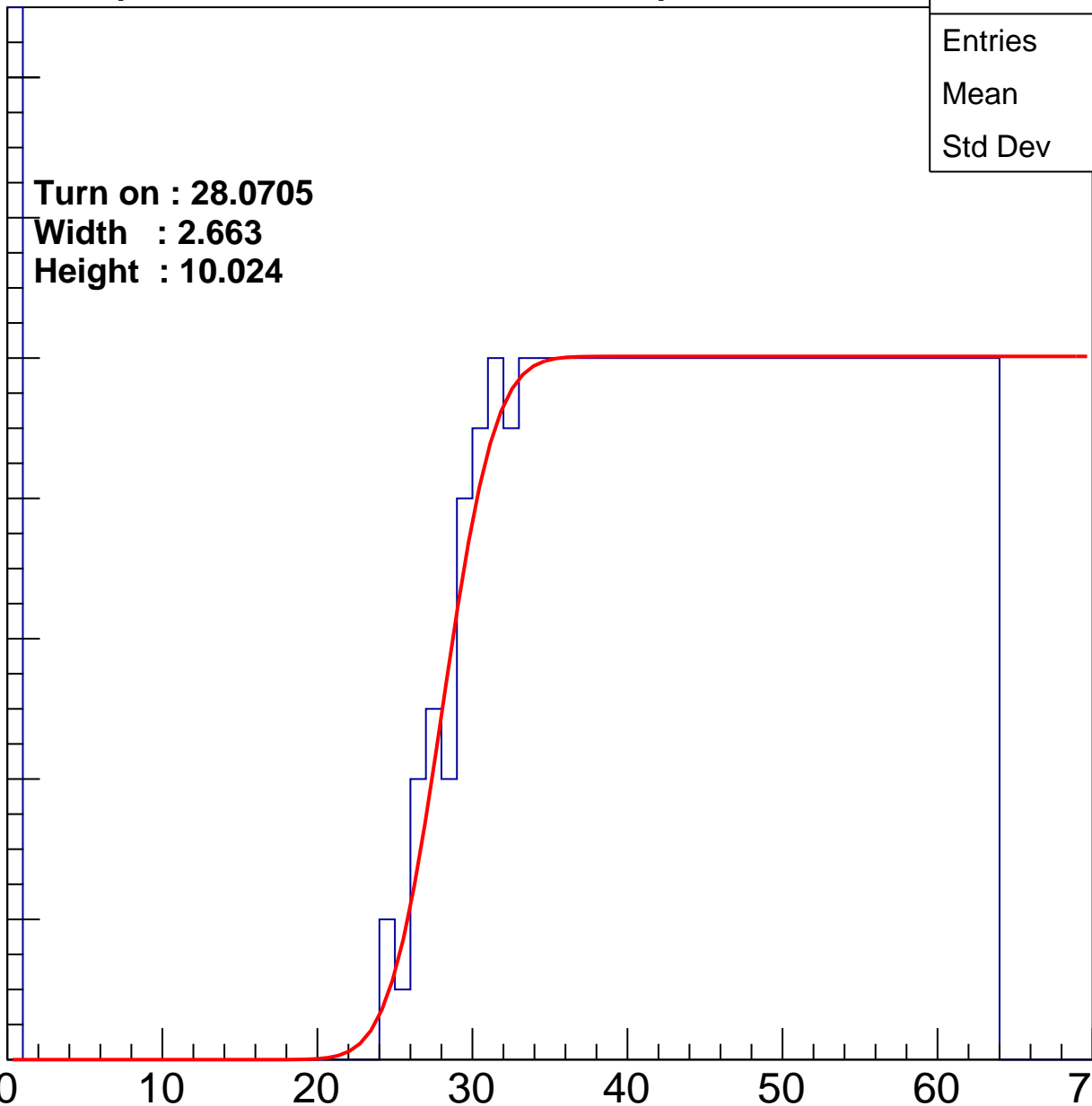
Width : 2.663

Height : 10.024

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch10

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	440
Mean	38.61
Std Dev	18.03

**Turn on : 25.5485**

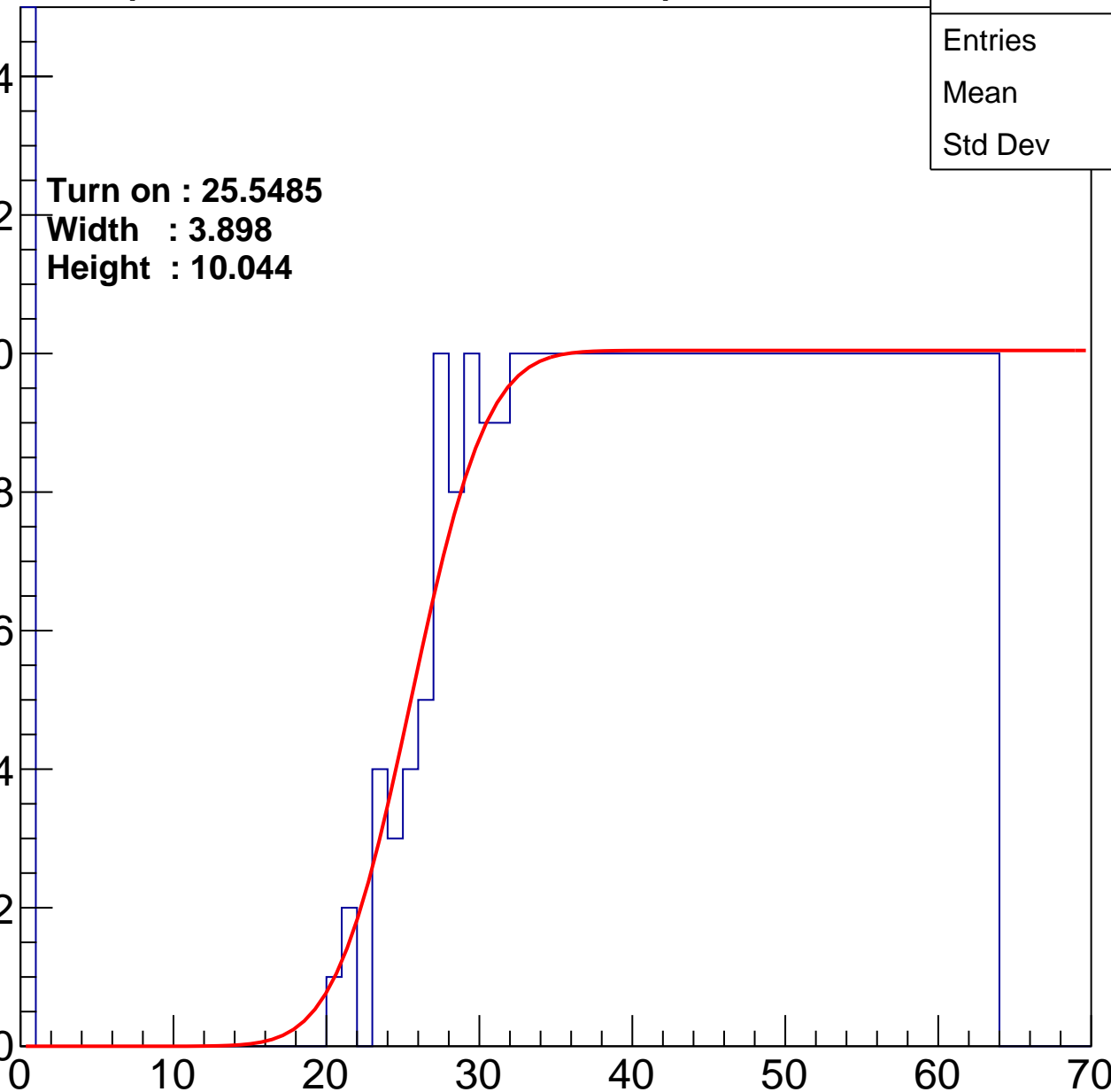
**Width : 3.898**

**Height : 10.044**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch11

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	406
Mean	40.59
Std Dev	16.98

**Turn on : 27.7147**

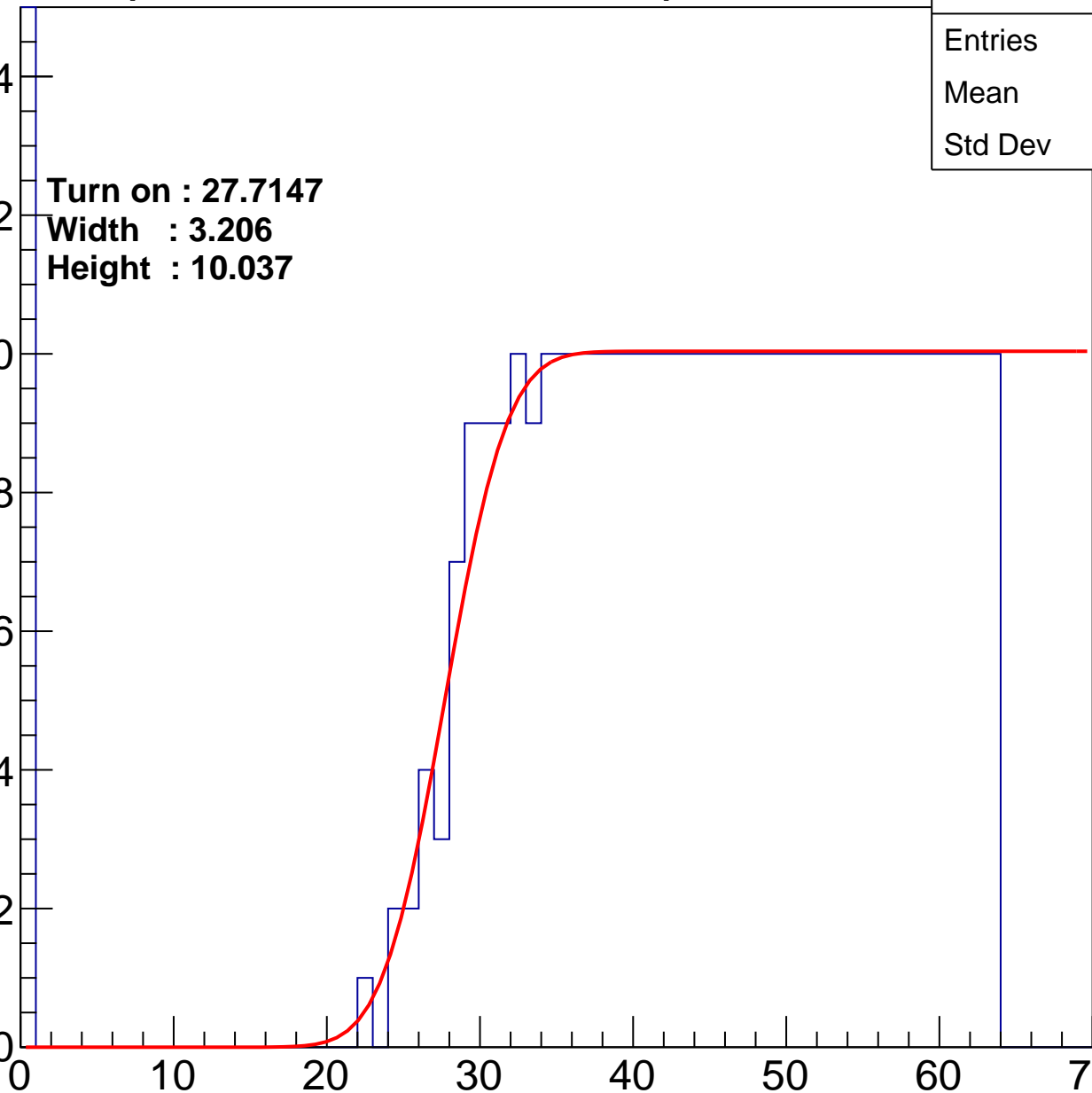
**Width : 3.206**

**Height : 10.037**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch12

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	433
Mean	38.74
Std Dev	18.23

Turn on : 26.5293

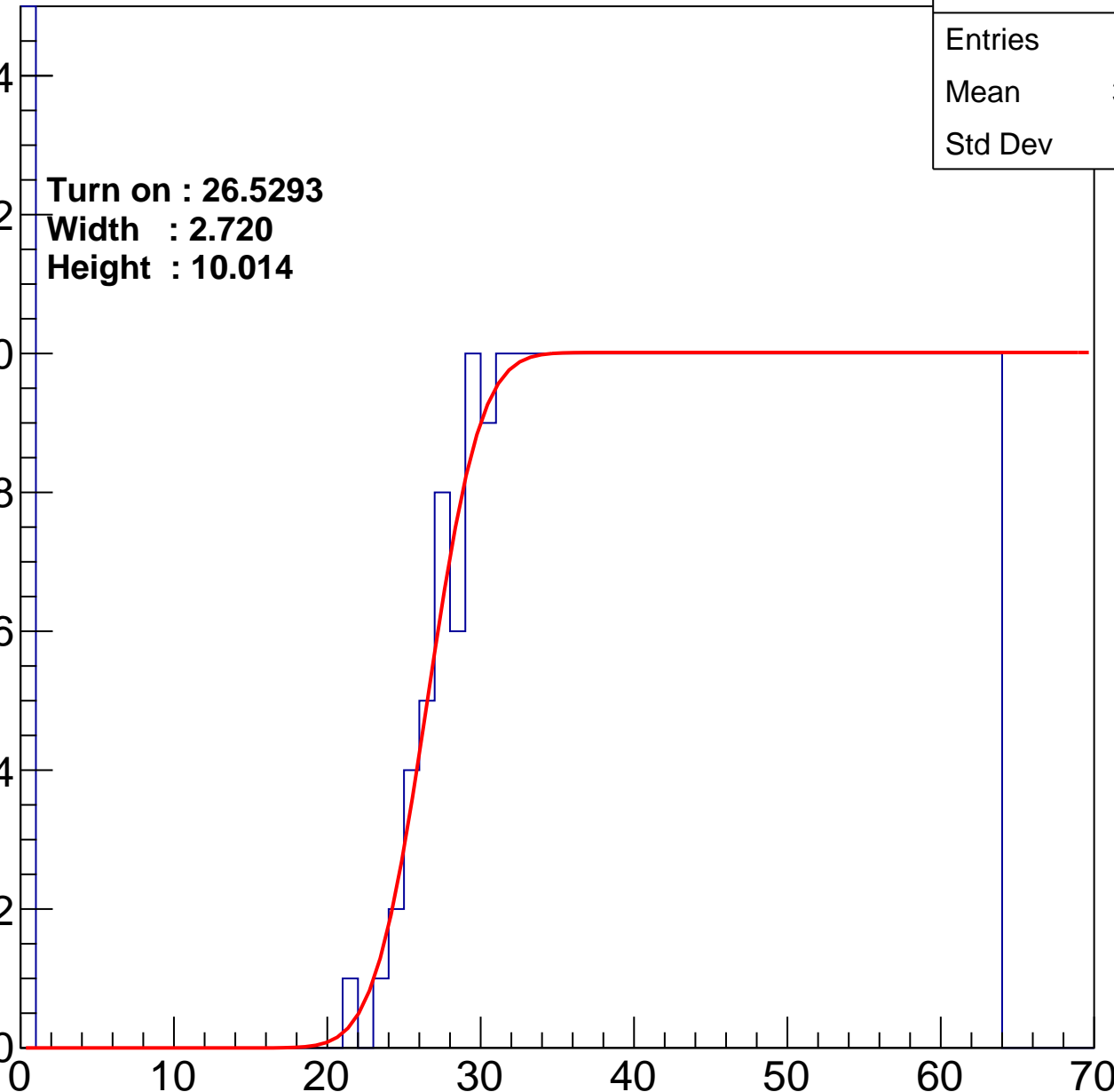
Width : 2.720

Height : 10.014

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch13

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	412
Mean	39.96
Std Dev	17.61

Turn on : 27.6733

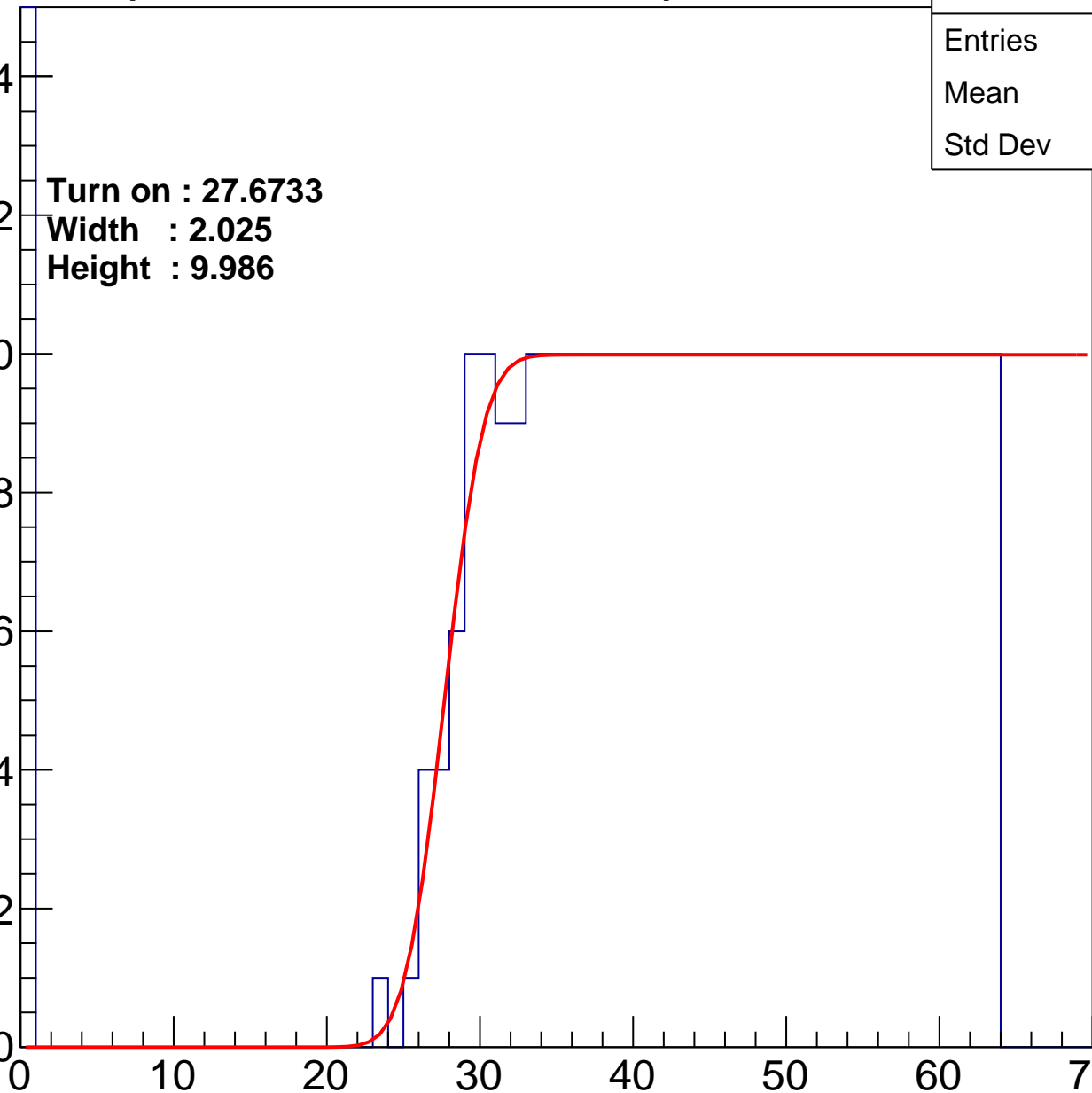
Width : 2.025

Height : 9.986

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch14

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	427
Mean	40.31
Std Dev	16.15

Turn on : 24.6190

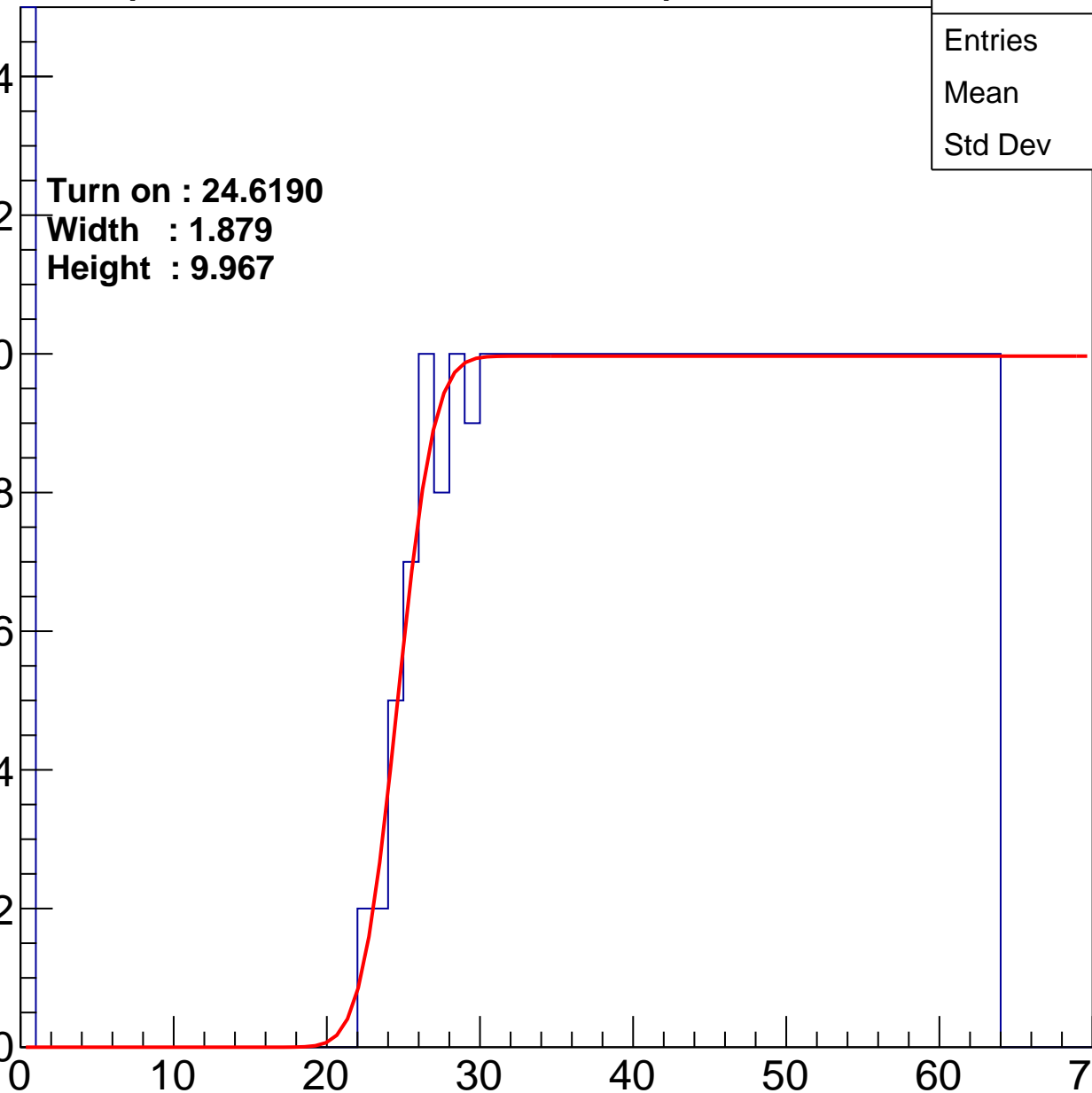
Width : 1.879

Height : 9.967

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U20-ch15

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	385
Mean	41.73
Std Dev	16.43

Turn on : 28.6913

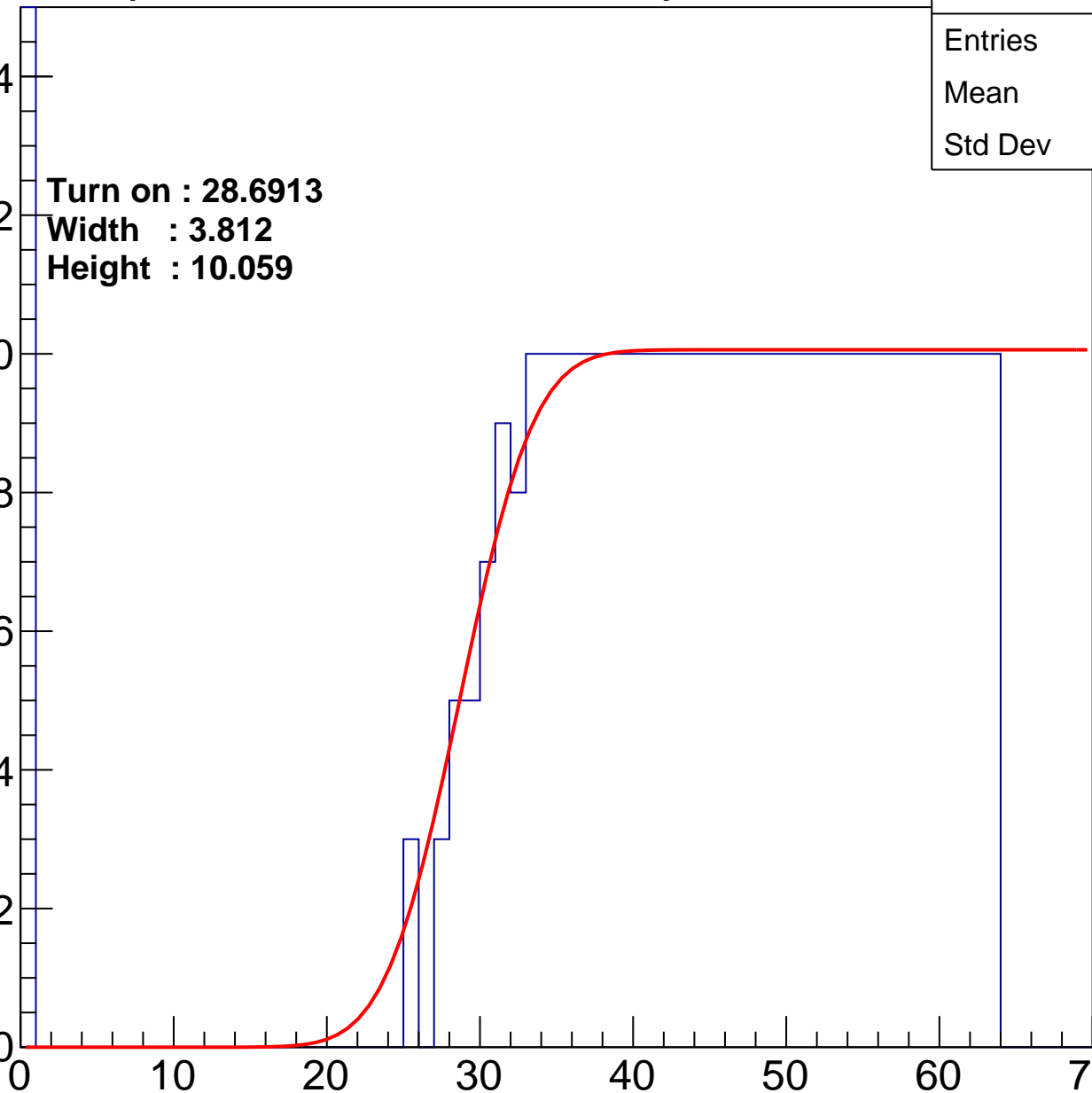
Width : 3.812

Height : 10.059

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch16

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	422
Mean	40.7
Std Dev	15.88

Turn on : 26.1648

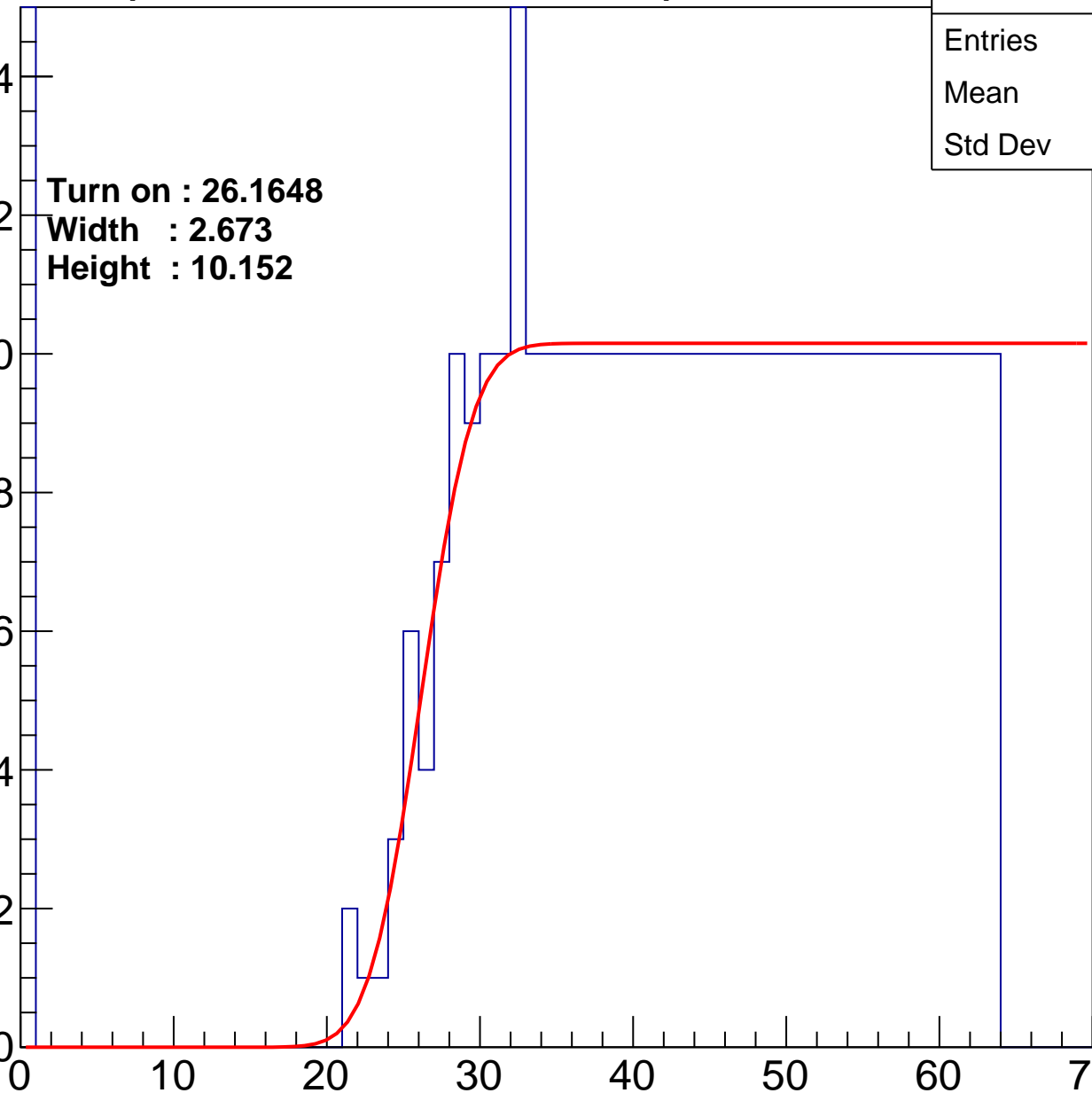
Width : 2.673

Height : 10.152

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch17

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	427
Mean	39.45
Std Dev	17.51

Turn on : 26.4817

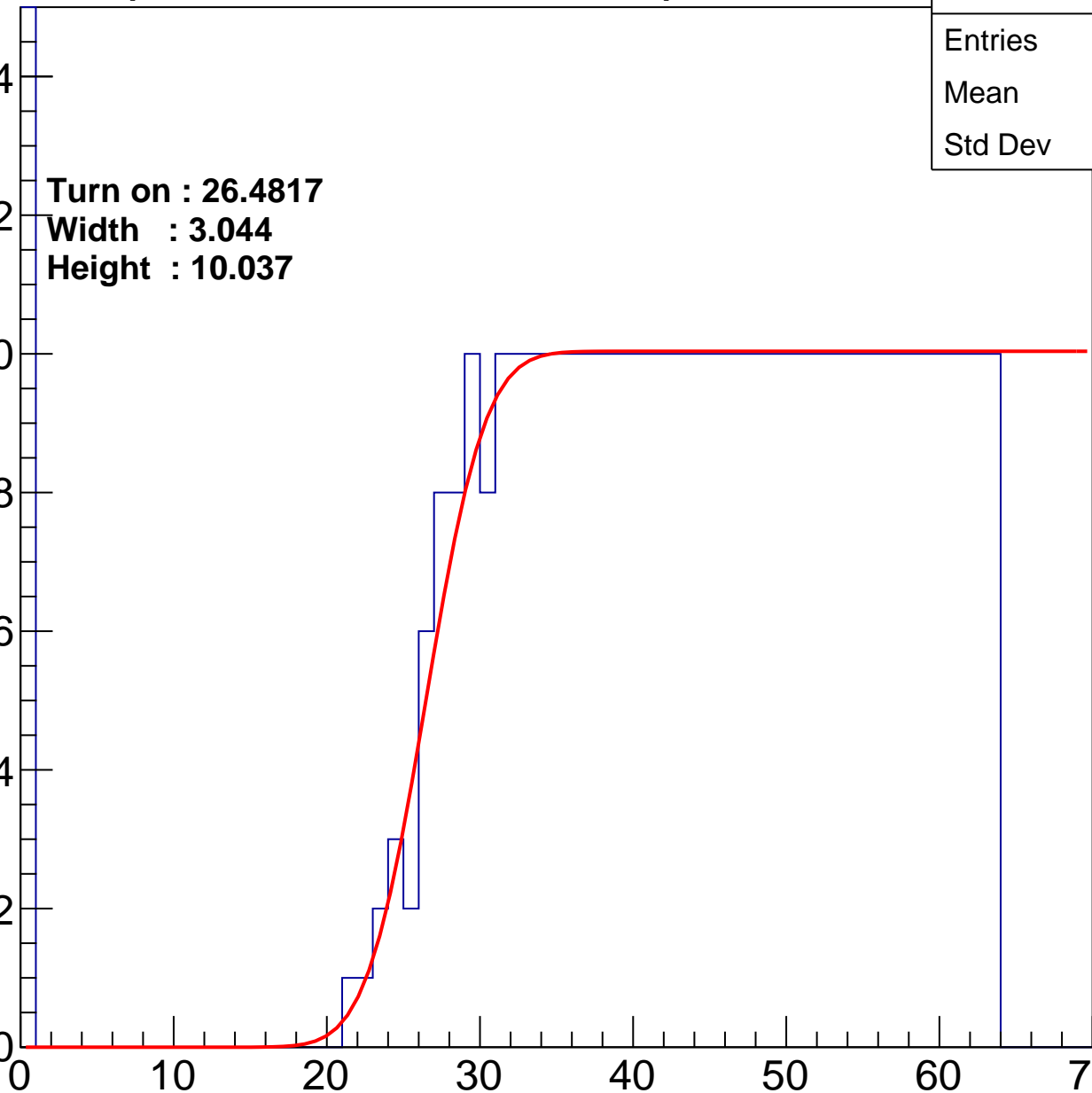
Width : 3.044

Height : 10.037

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch18

calib\_packv5\_041523\_1651.root, FC#0, port C2

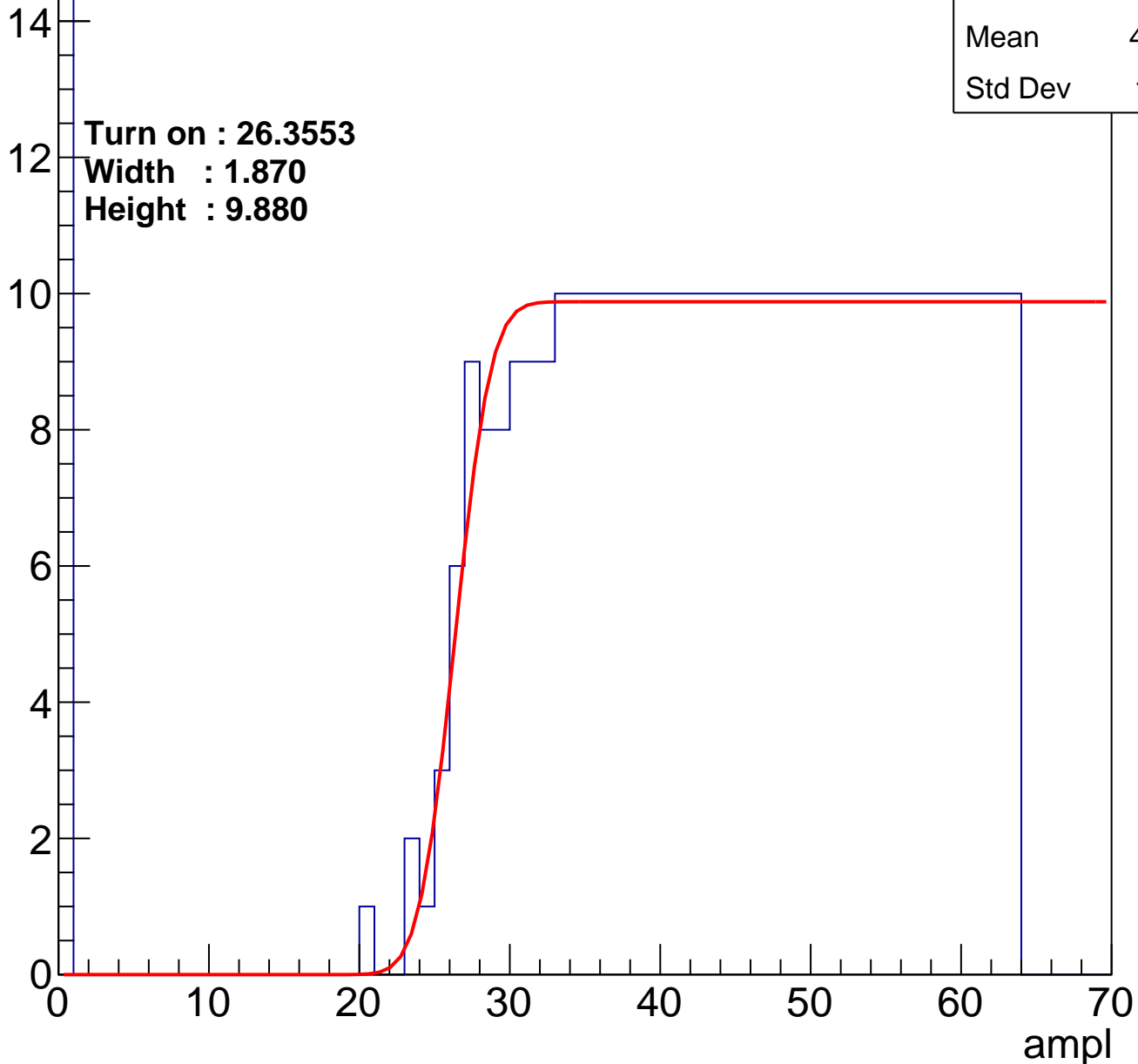
Entry

Entries	418
Mean	40.04
Std Dev	17.11

Turn on : 26.3553

Width : 1.870

Height : 9.880



# B1L103S, U20-ch19

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	428
Mean	39.9
Std Dev	16.76

Turn on : 25.7814

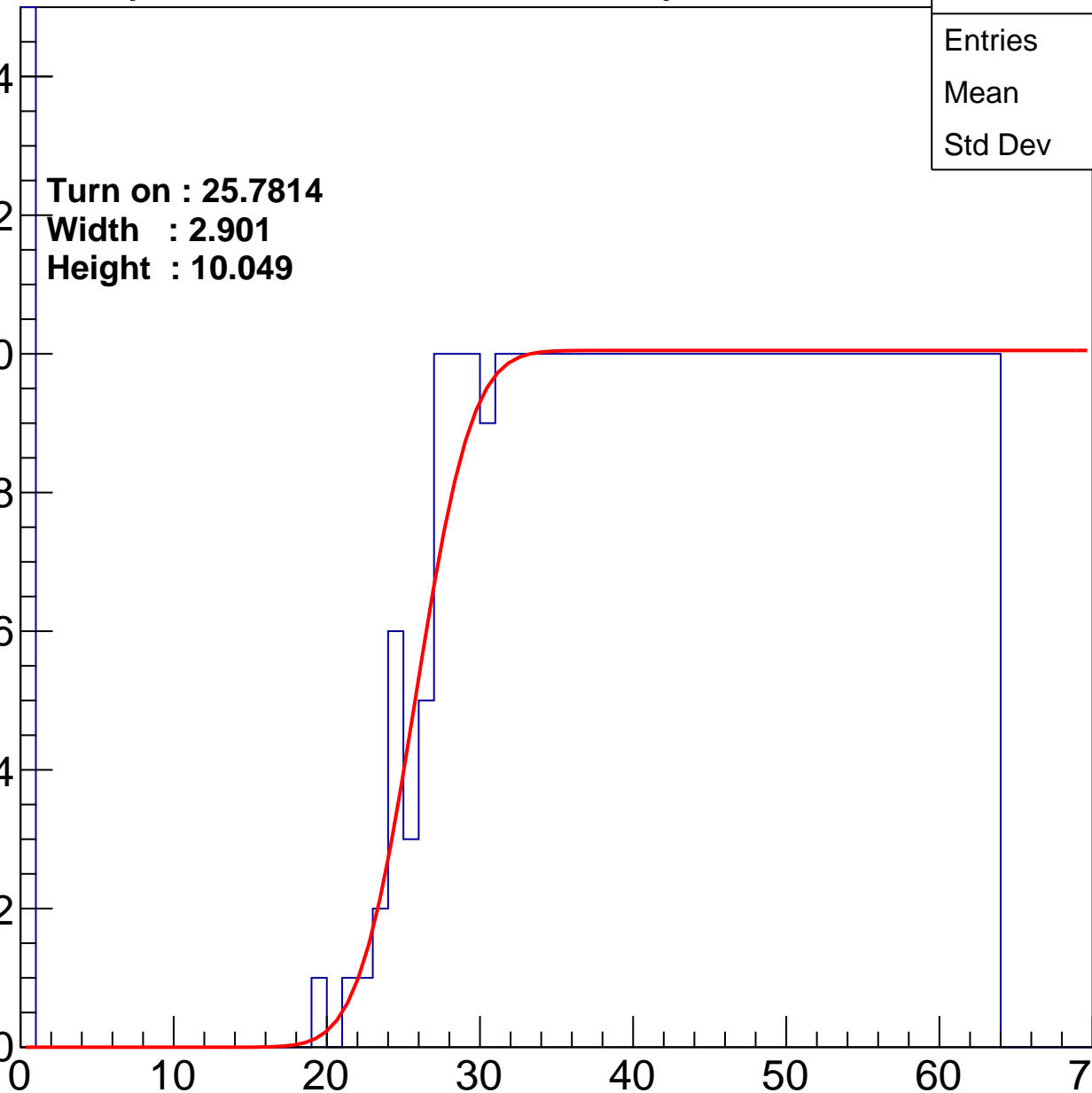
Width : 2.901

Height : 10.049

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch20

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	428
Mean	40
Std Dev	16.59

Turn on : 25.2415

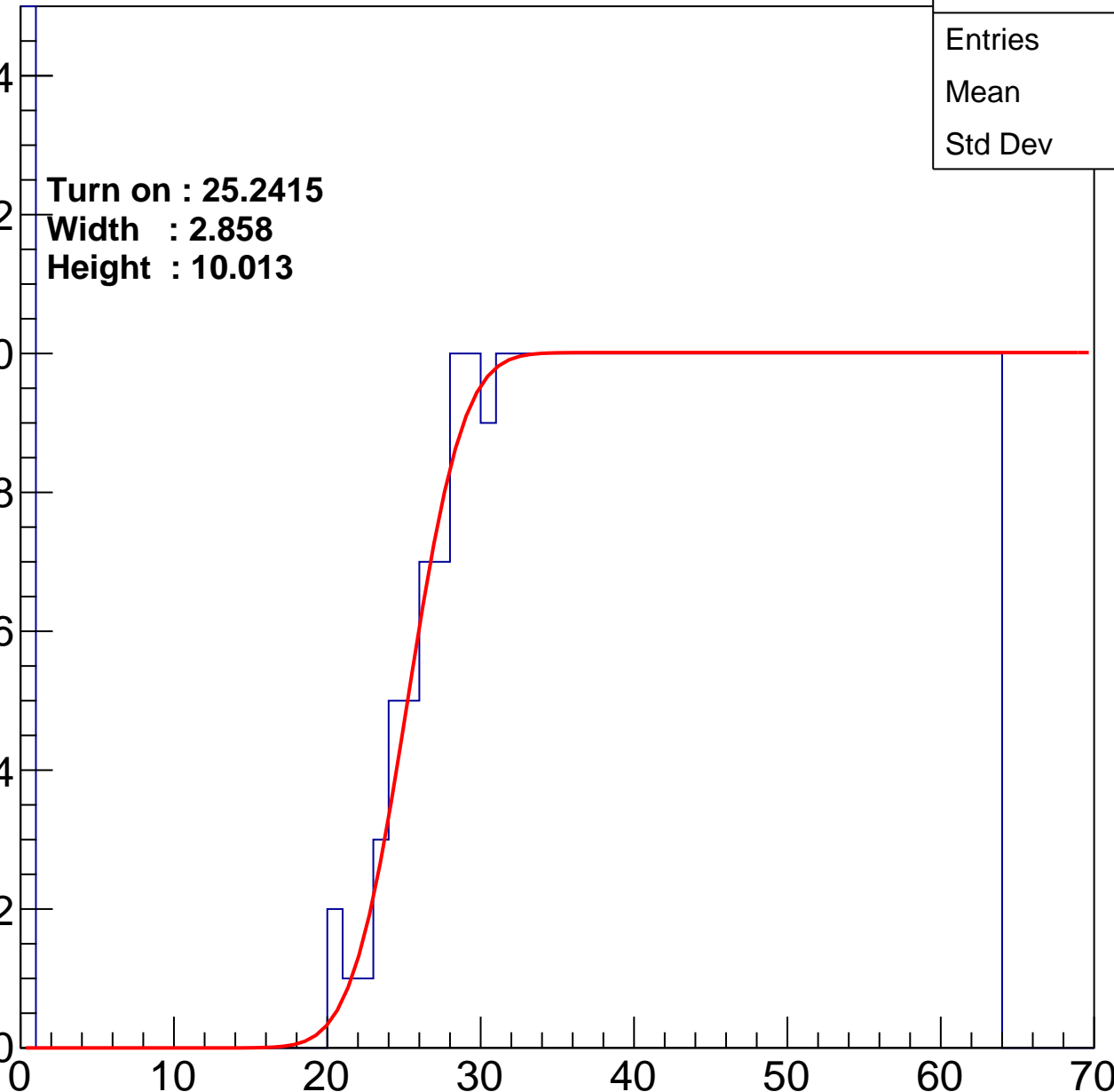
Width : 2.858

Height : 10.013

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch21

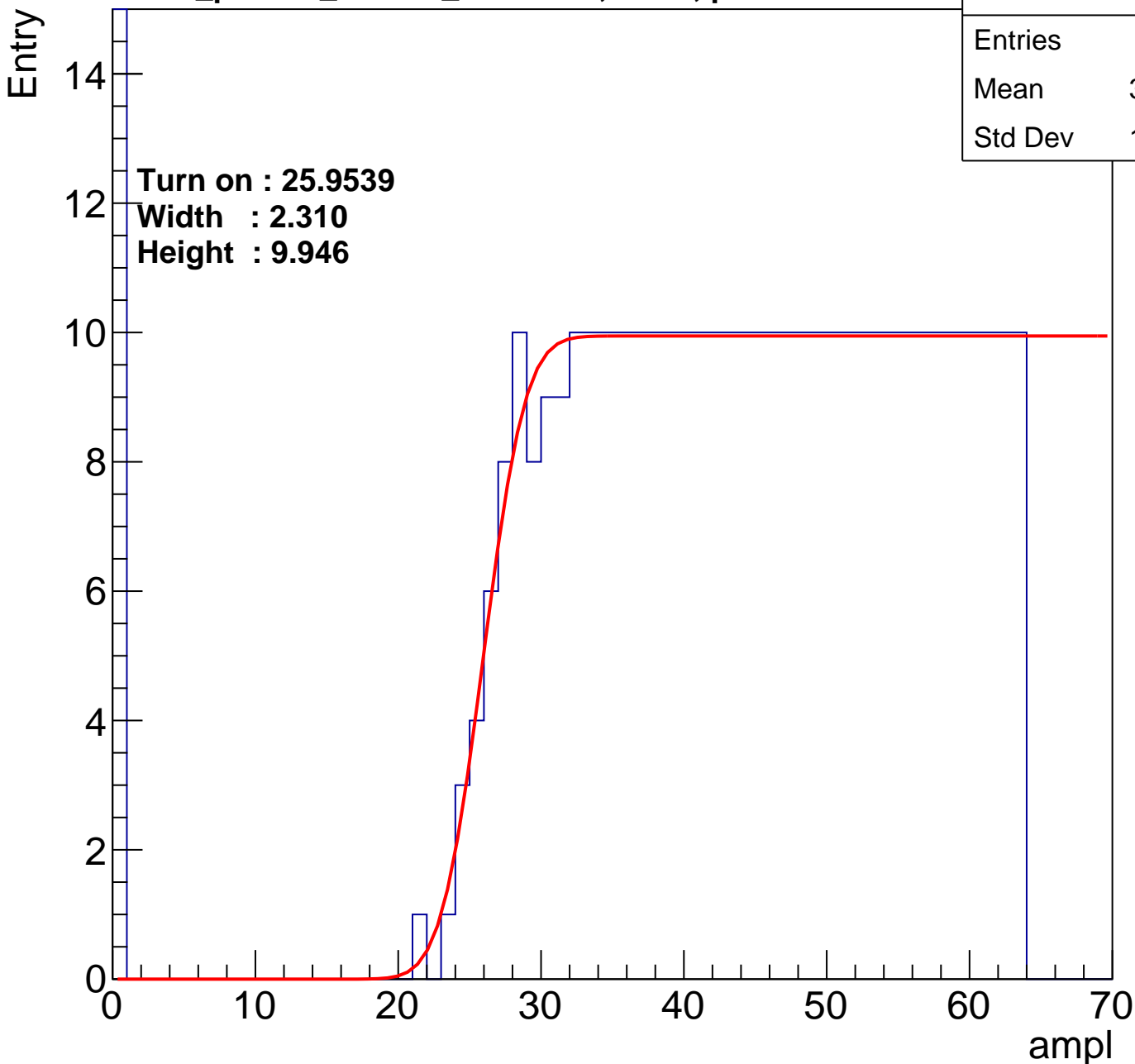
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	423
Mean	39.83
Std Dev	17.16

Turn on : 25.9539

Width : 2.310

Height : 9.946



# B1L103S, U20-ch22

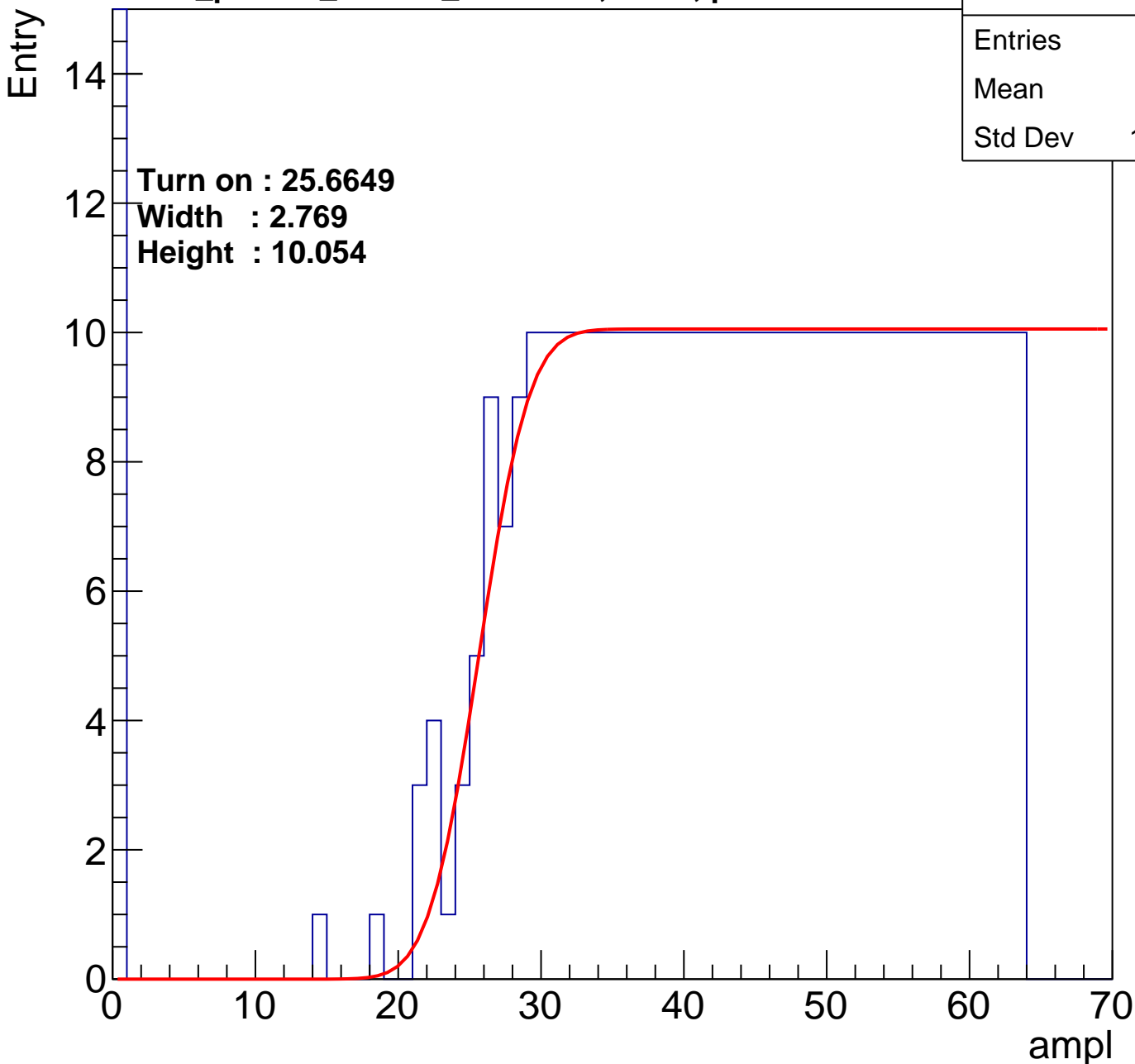
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	436
Mean	39.4
Std Dev	17.06

Turn on : 25.6649

Width : 2.769

Height : 10.054





# B1L103S, U20-ch23

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	406
Mean	40.63
Std Dev	16.94

**Turn on : 27.6346**

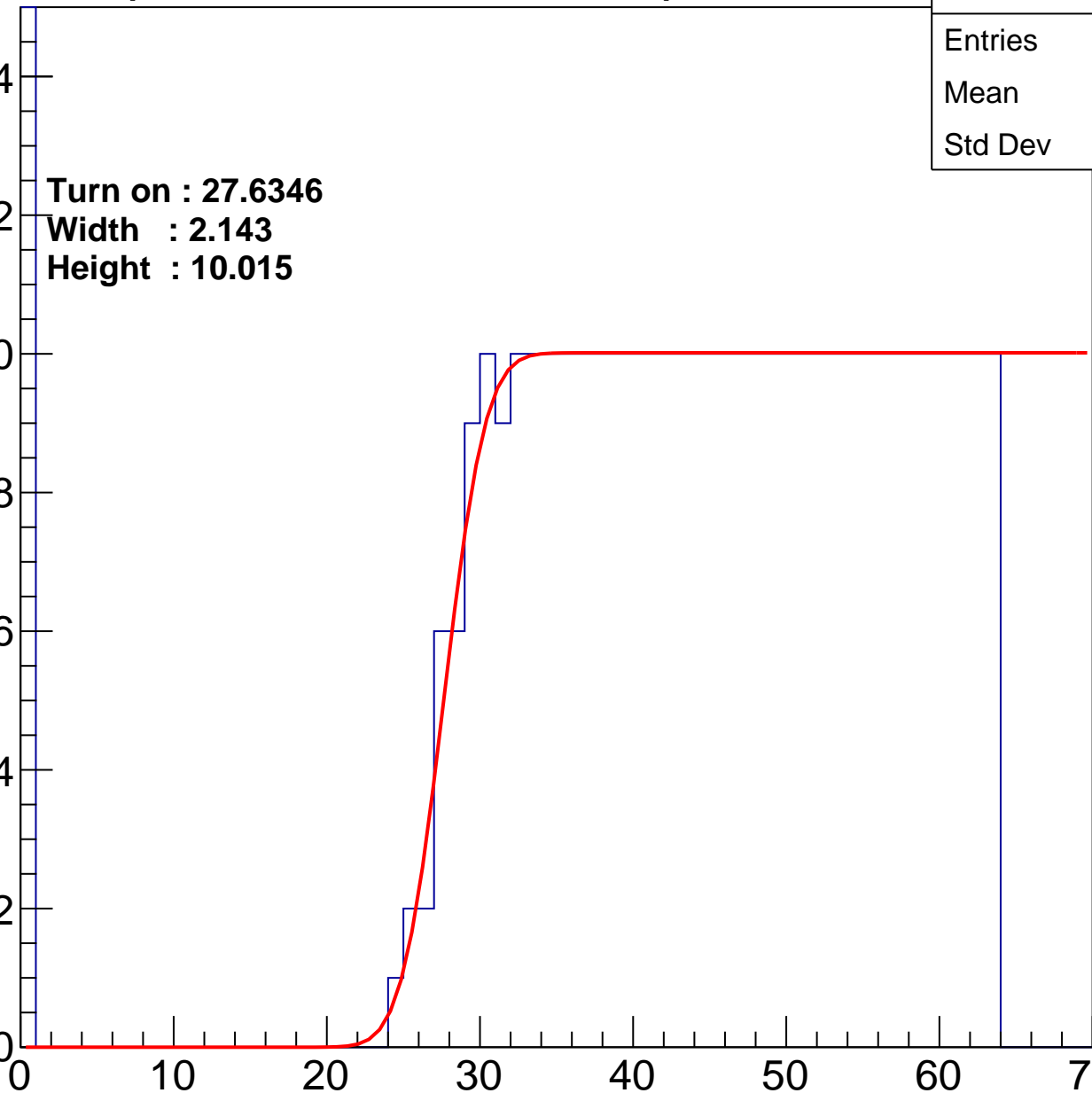
**Width : 2.143**

**Height : 10.015**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch24

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	449
Mean	38.35
Std Dev	17.95

Turn on : 24.7561

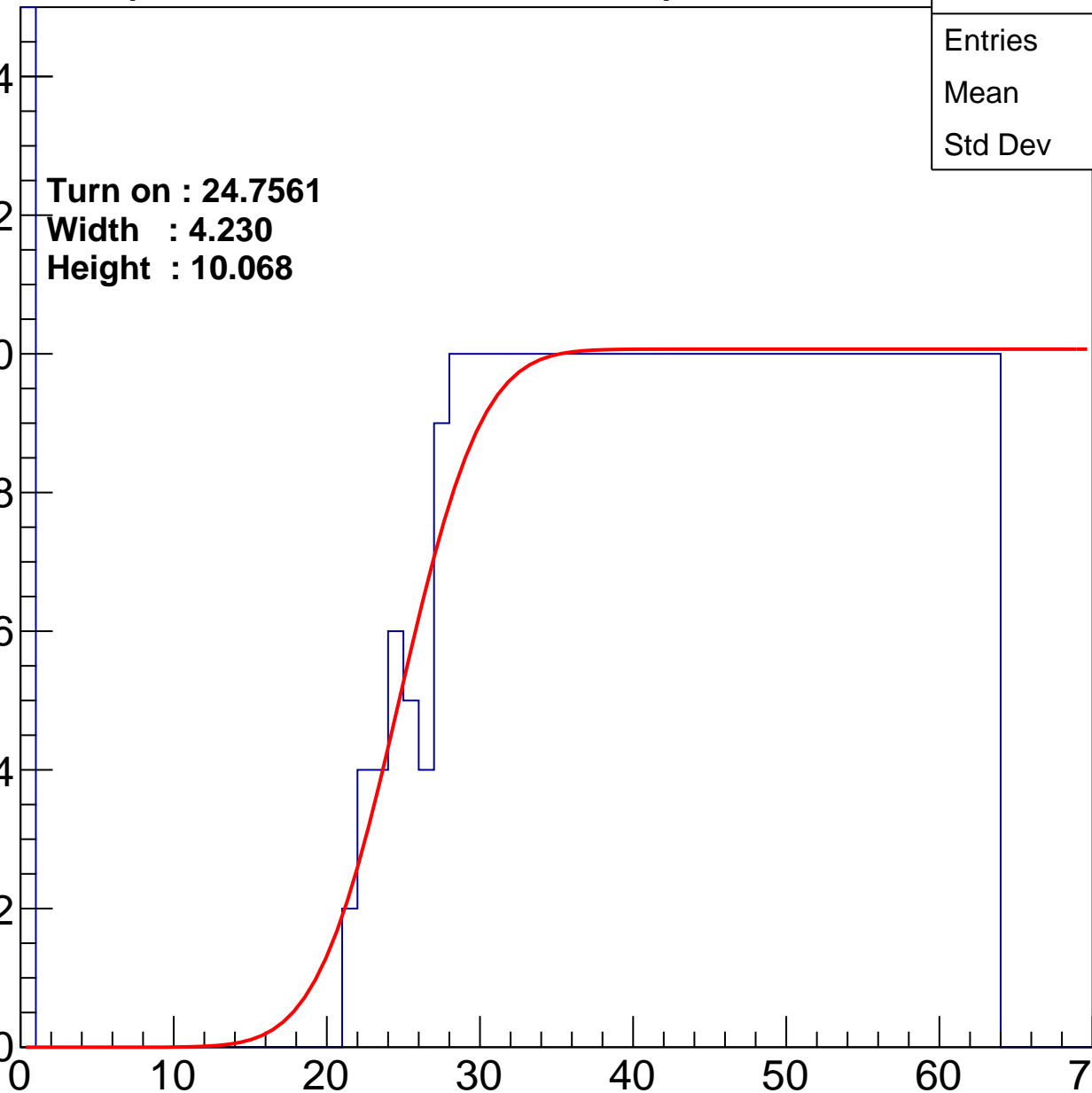
Width : 4.230

Height : 10.068

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch25

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	410
Mean	40.53
Std Dev	16.84

Turn on : 27.4118

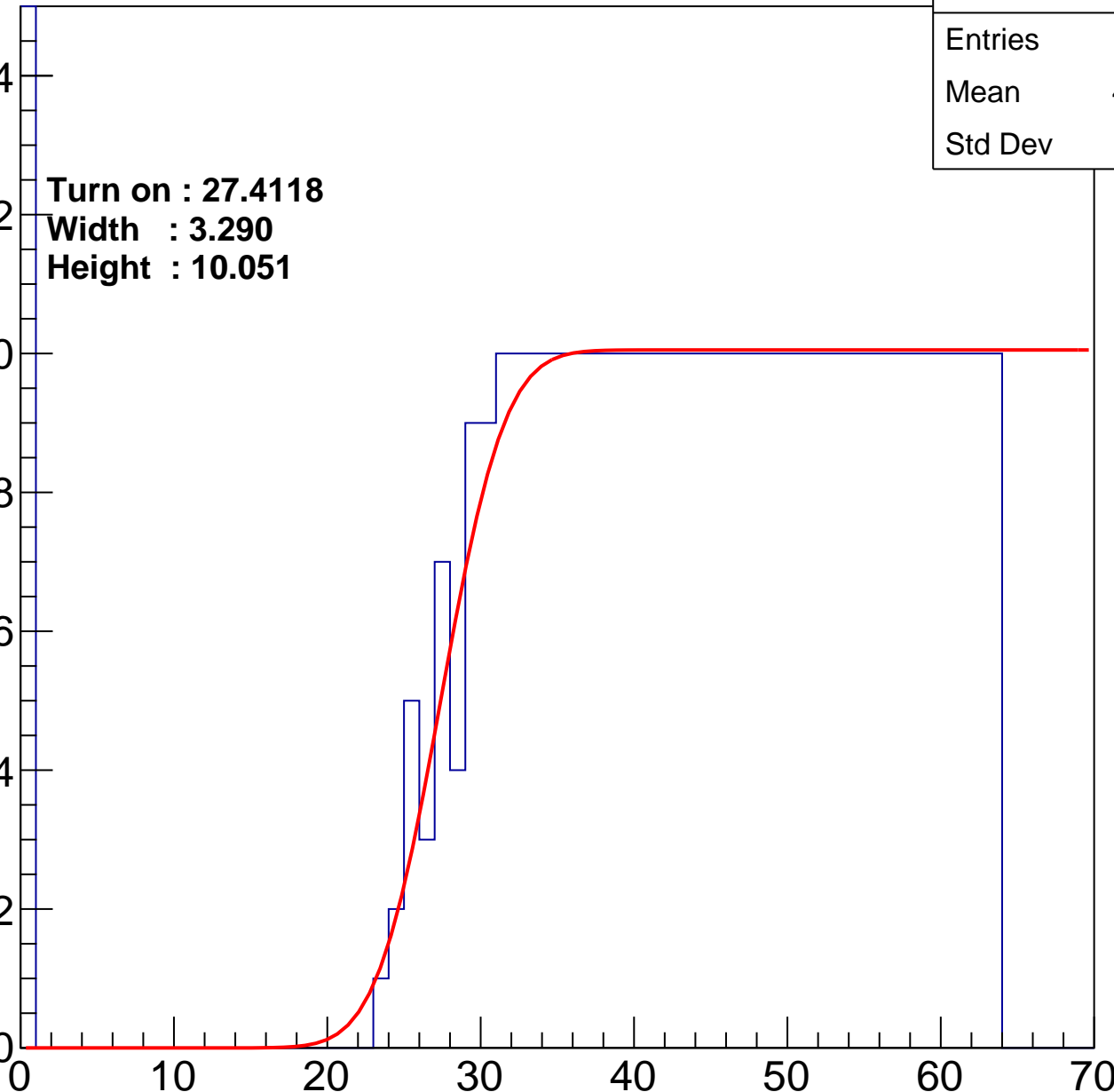
Width : 3.290

Height : 10.051

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch26

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	440
Mean	38.99
Std Dev	17.5

Turn on : 24.7367

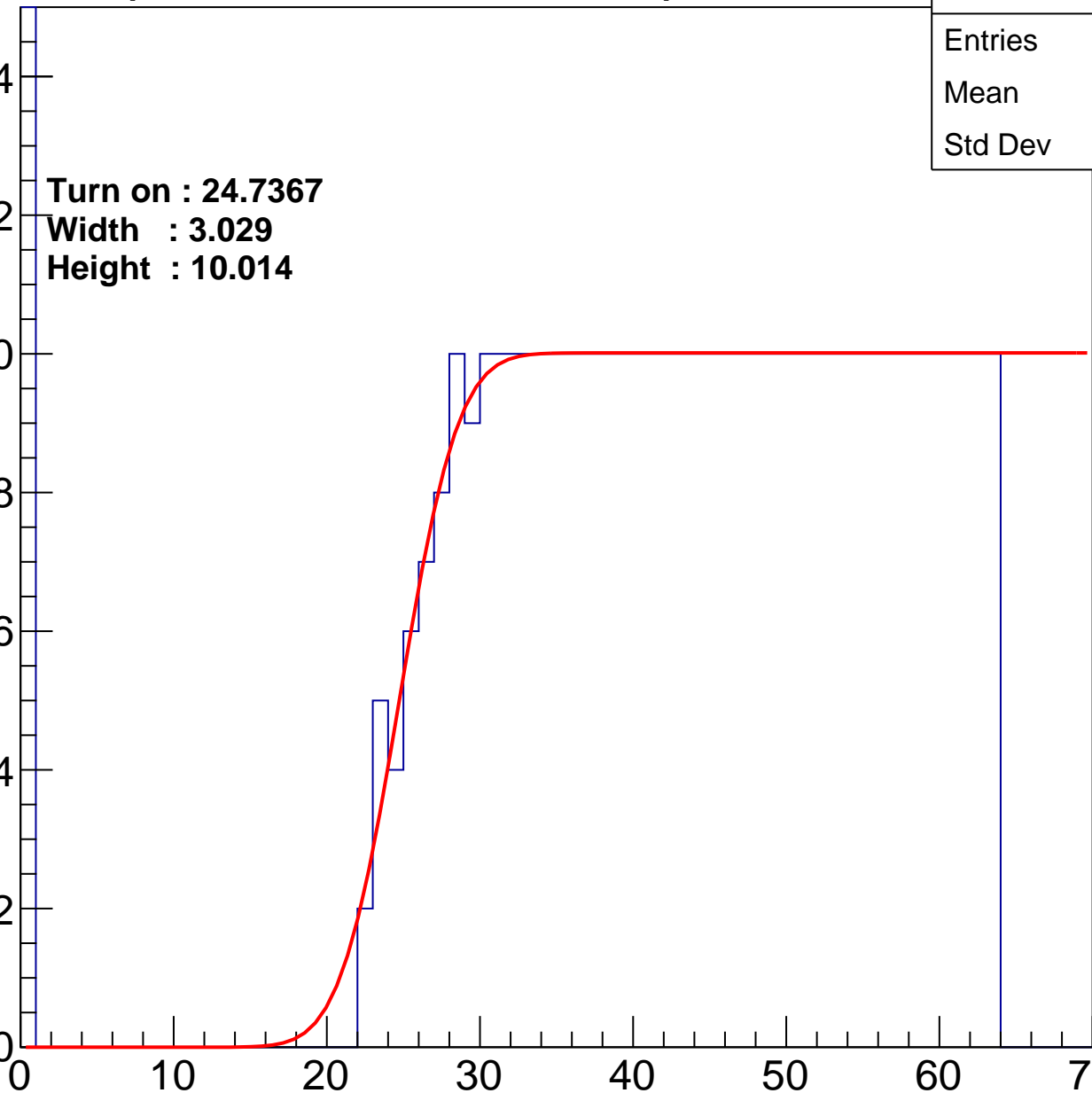
Width : 3.029

Height : 10.014

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch27

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	410
Mean	40.46
Std Dev	16.94

Turn on : 27.5196

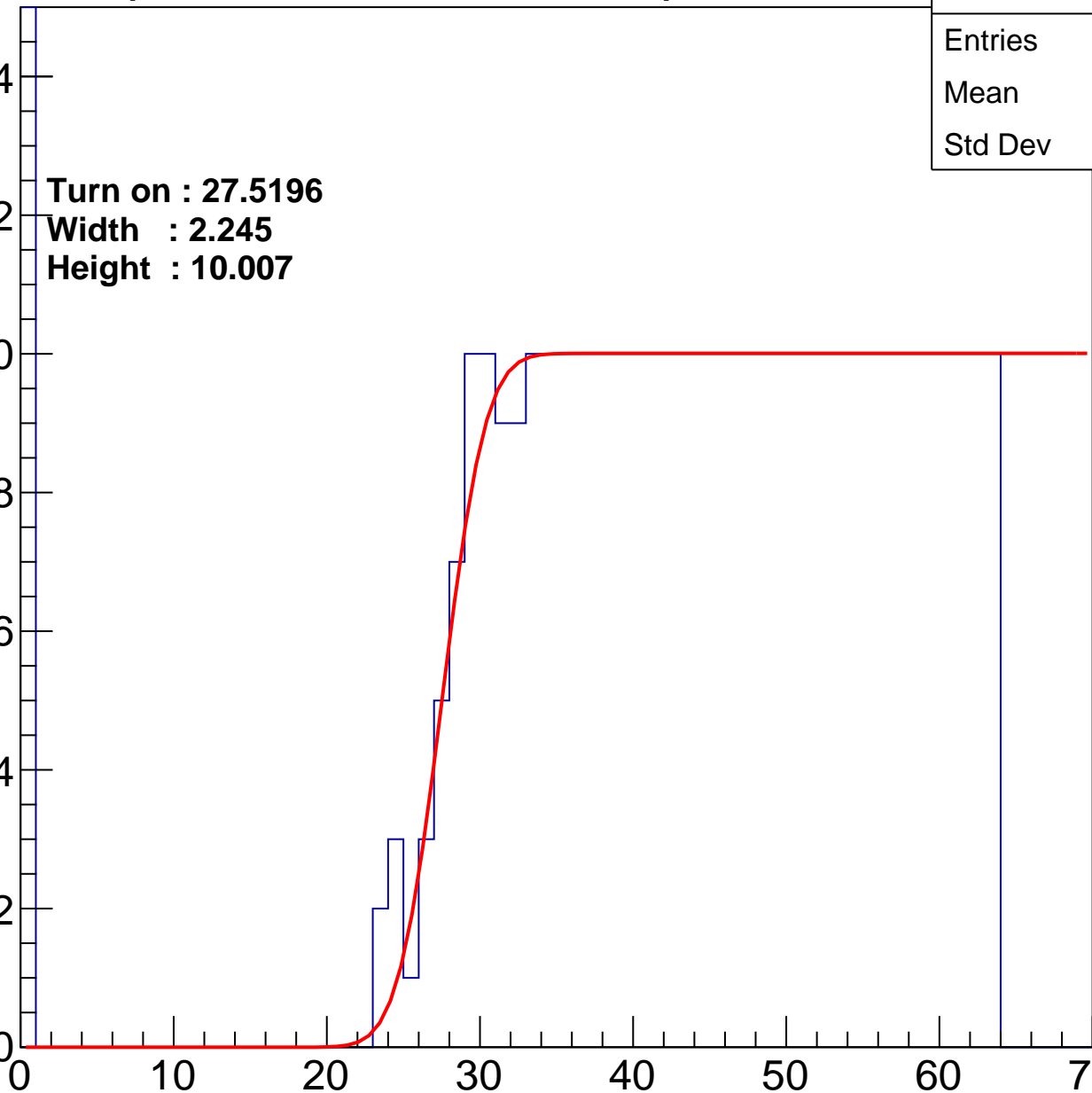
Width : 2.245

Height : 10.007

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch28

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	431
Mean	39.11
Std Dev	17.77

Turn on : 25.8298

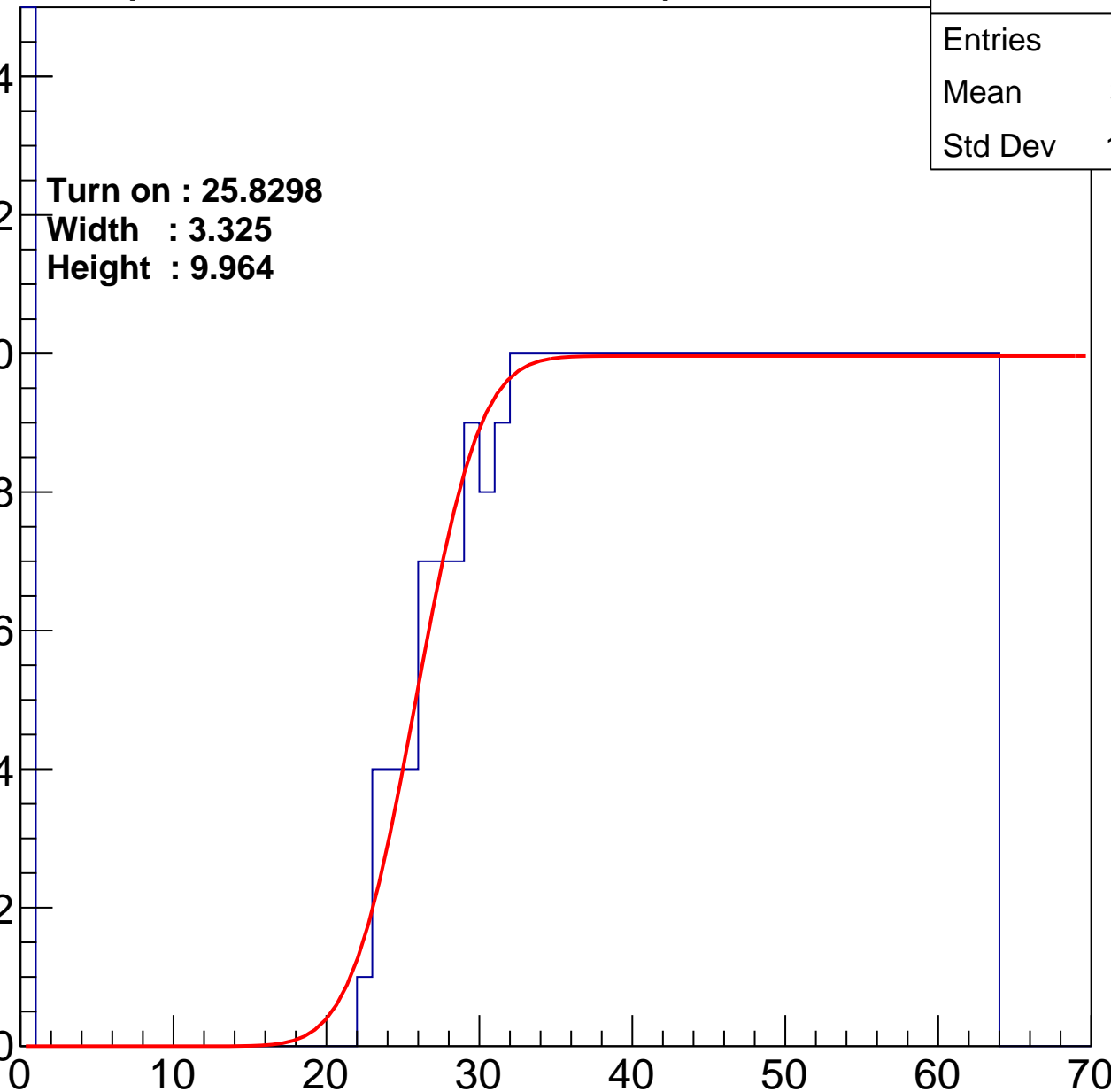
Width : 3.325

Height : 9.964

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch29

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	409
Mean	40.78
Std Dev	16.45

Turn on : 27.0799

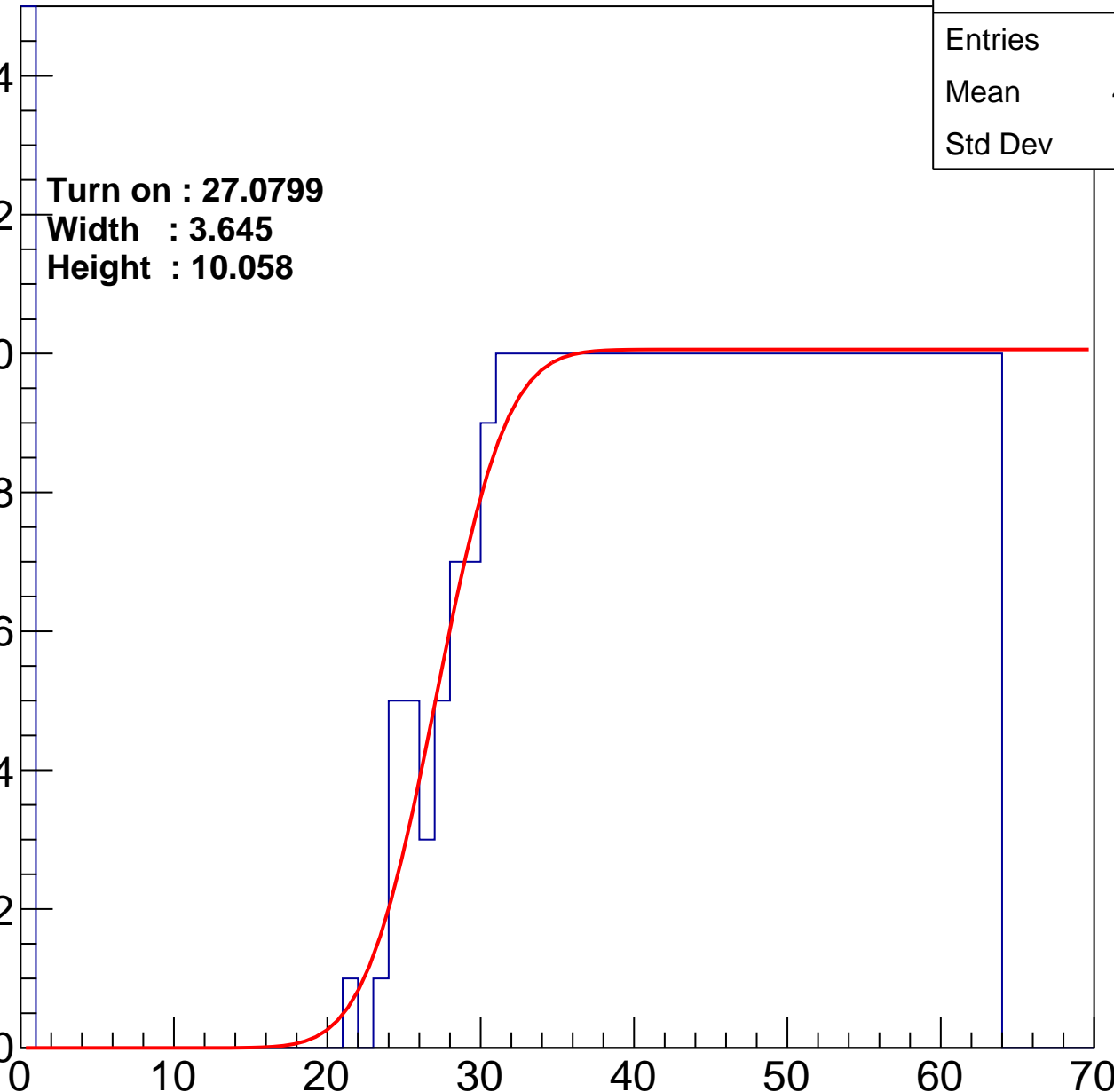
Width : 3.645

Height : 10.058

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch30

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	414
Mean	40.51
Std Dev	16.64

Turn on : 26.8067

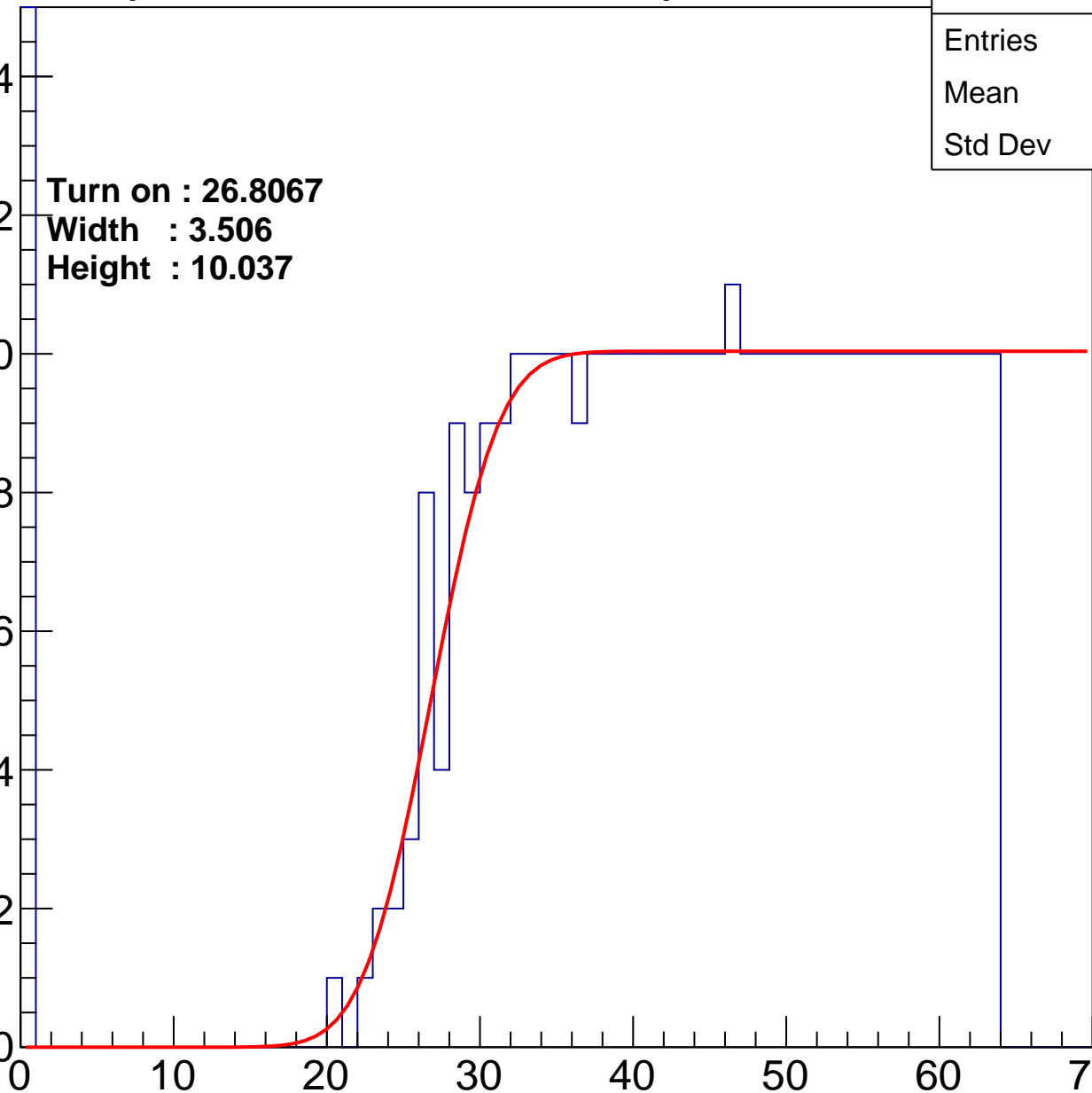
Width : 3.506

Height : 10.037

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U20-ch31

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	418
Mean	39.11
Std Dev	18.49

**Turn on : 27.9457**

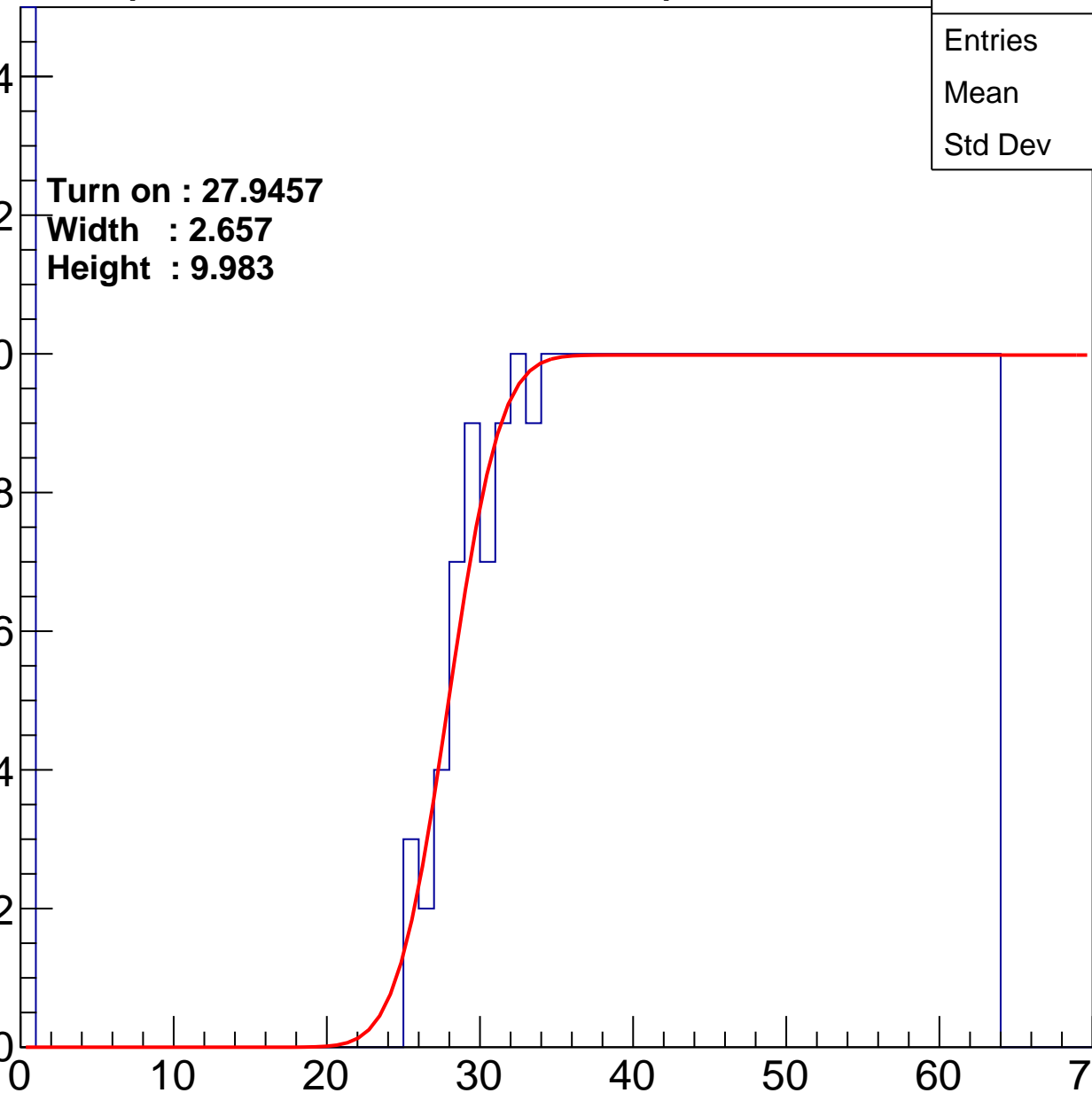
**Width : 2.657**

**Height : 9.983**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch32

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	423
Mean	40.05
Std Dev	16.8

**Turn on : 26.4457**

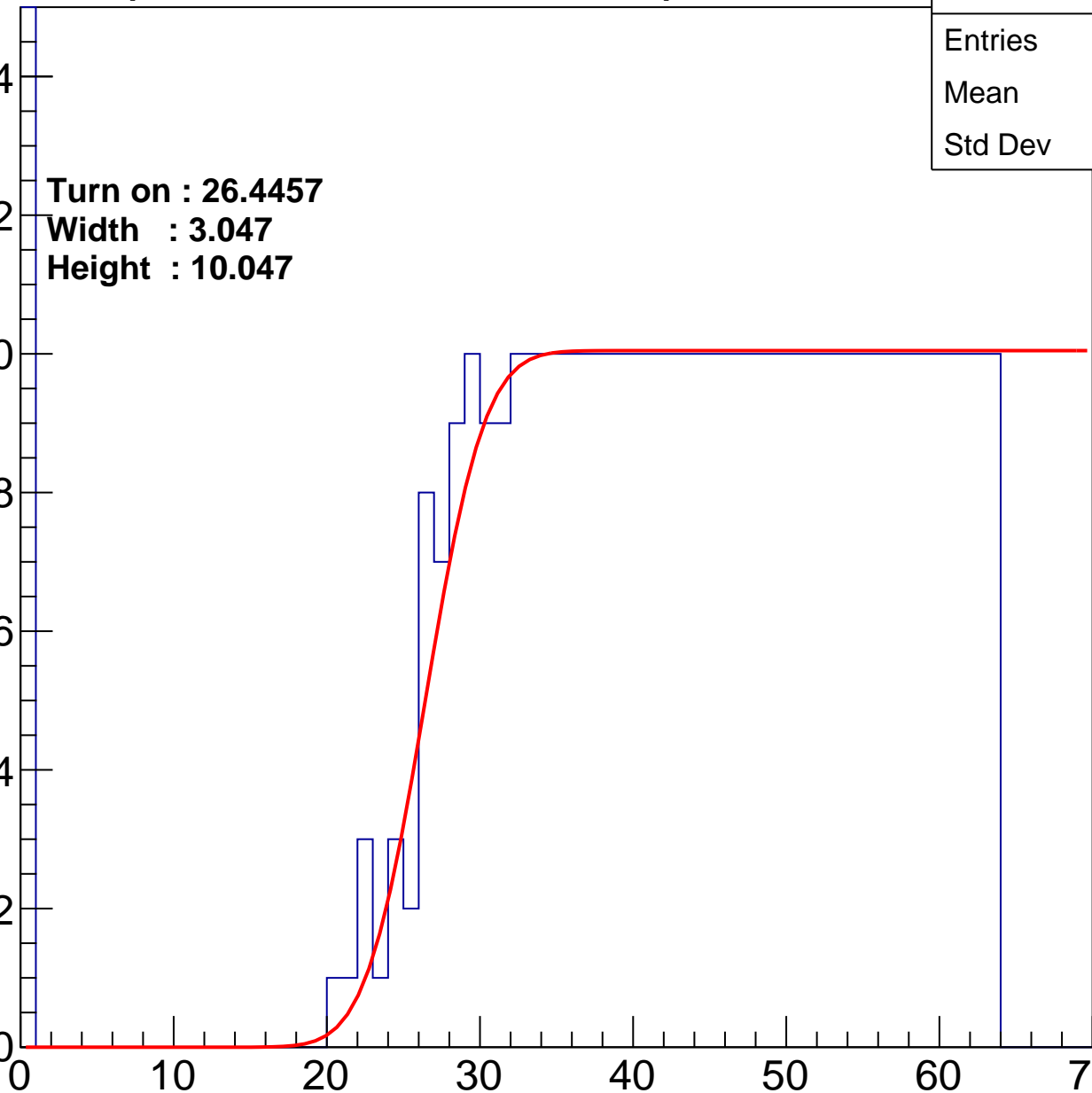
**Width : 3.047**

**Height : 10.047**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch33

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	404
Mean	40.47
Std Dev	17.29

Turn on : 27.7141

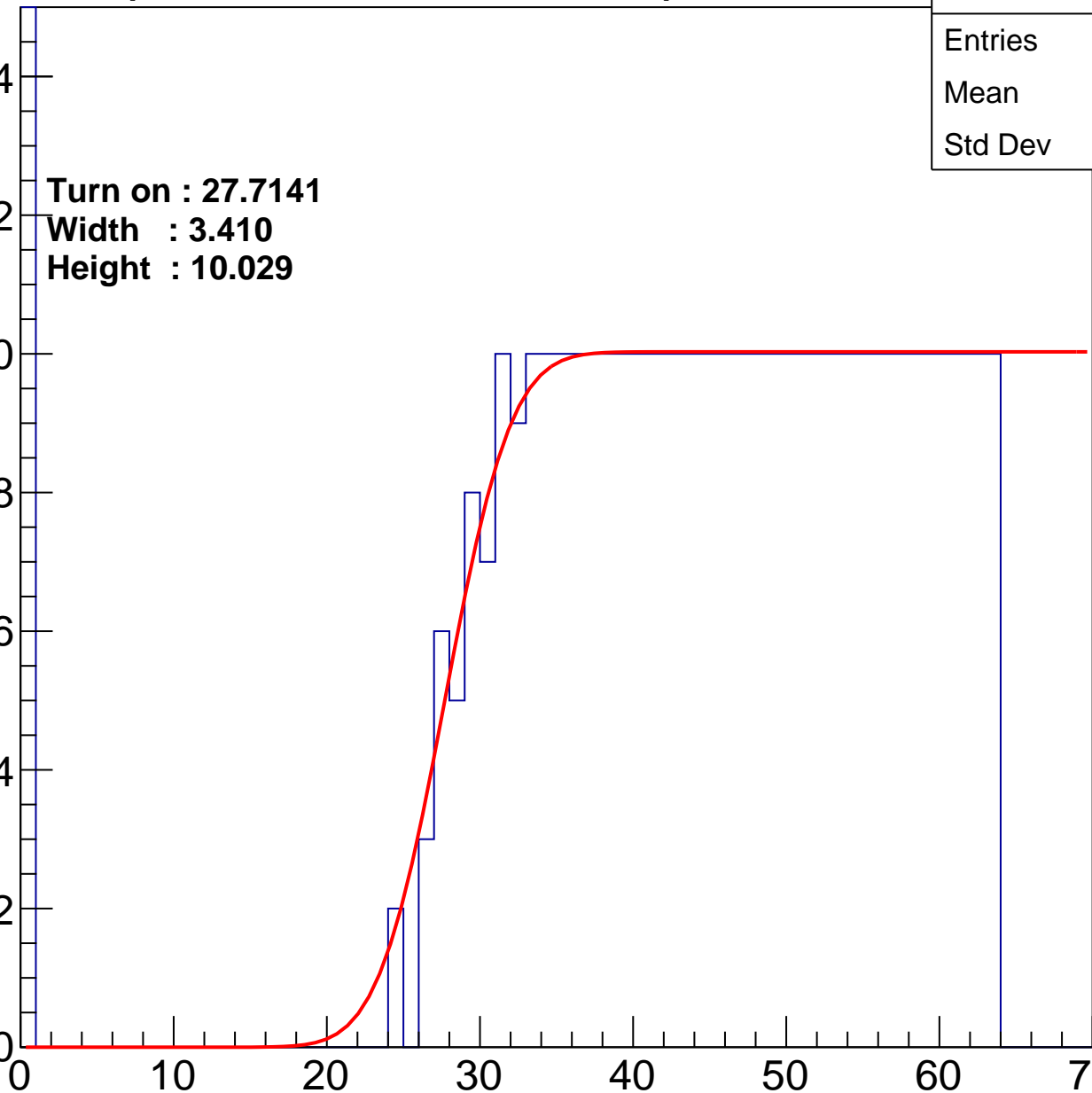
Width : 3.410

Height : 10.029

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch34

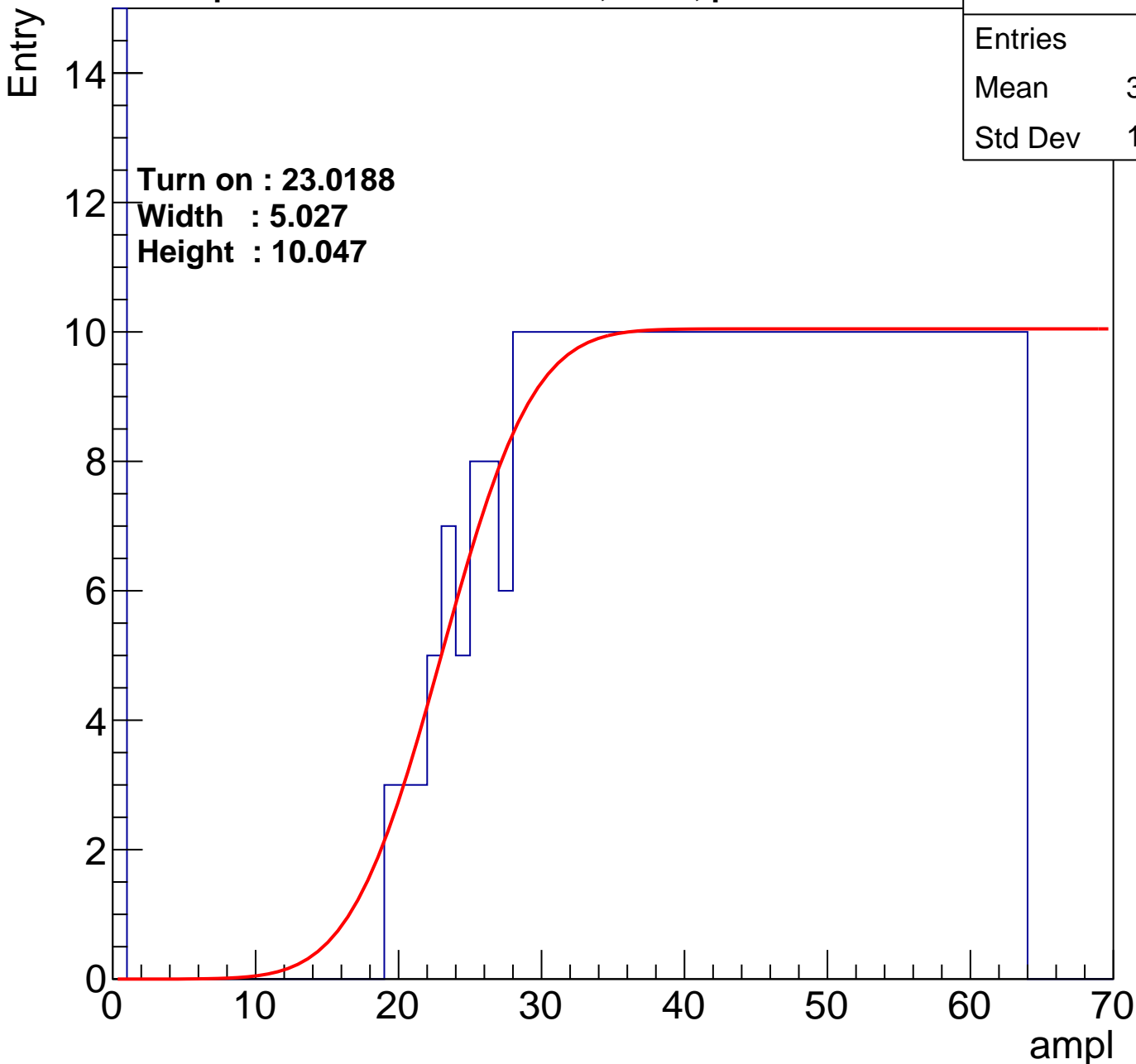
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	441
Mean	39.73
Std Dev	16.18

Turn on : 23.0188

Width : 5.027

Height : 10.047



# B1L103S, U20-ch35

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	406
Mean	40.91
Std Dev	16.49

Turn on : 27.1187

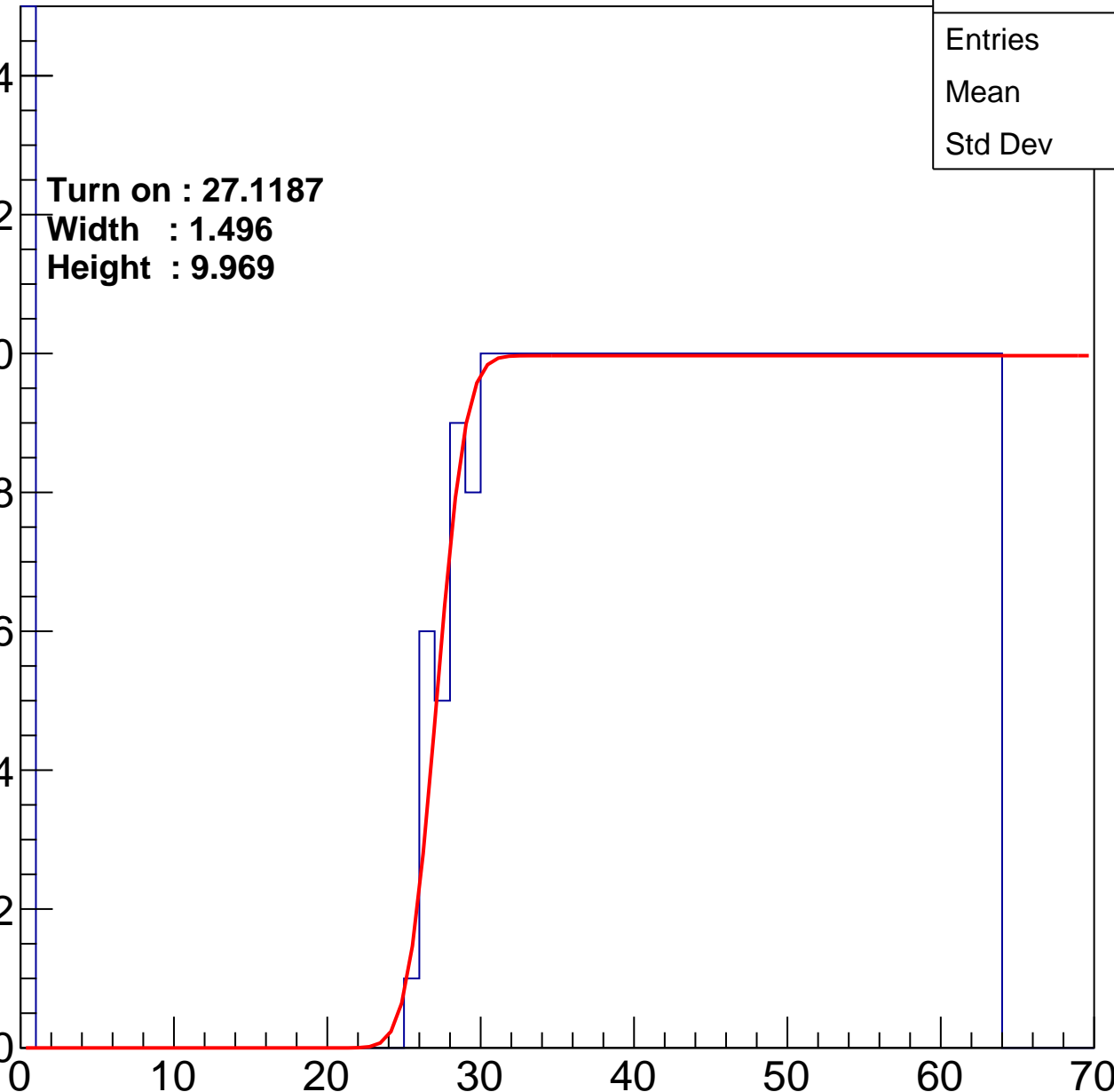
Width : 1.496

Height : 9.969

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch36

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	430
Mean	39.03
Std Dev	17.95

**Turn on : 26.5967**

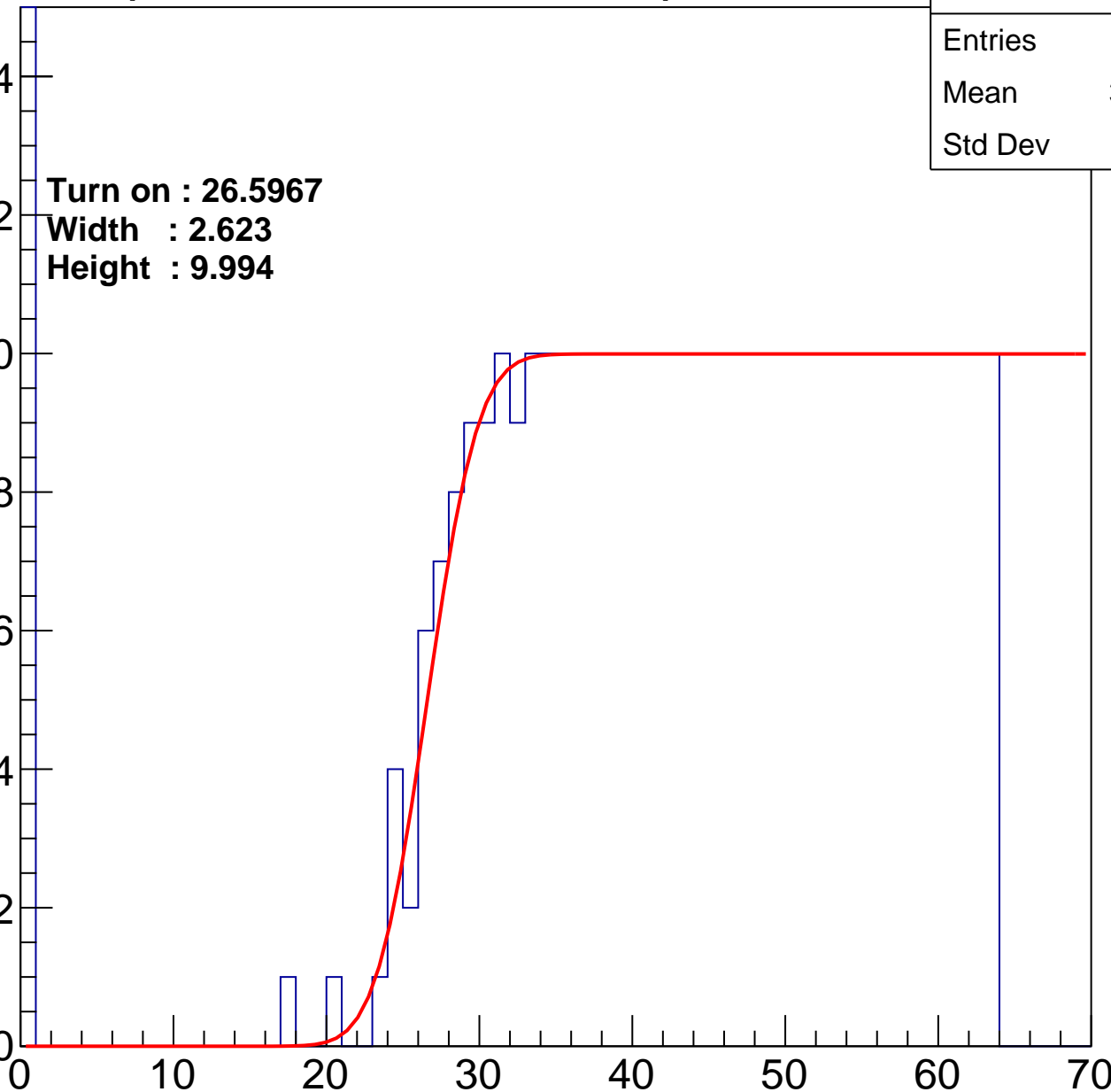
**Width : 2.623**

**Height : 9.994**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch37

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	432
Mean	39.25
Std Dev	17.51

Turn on : 25.7696

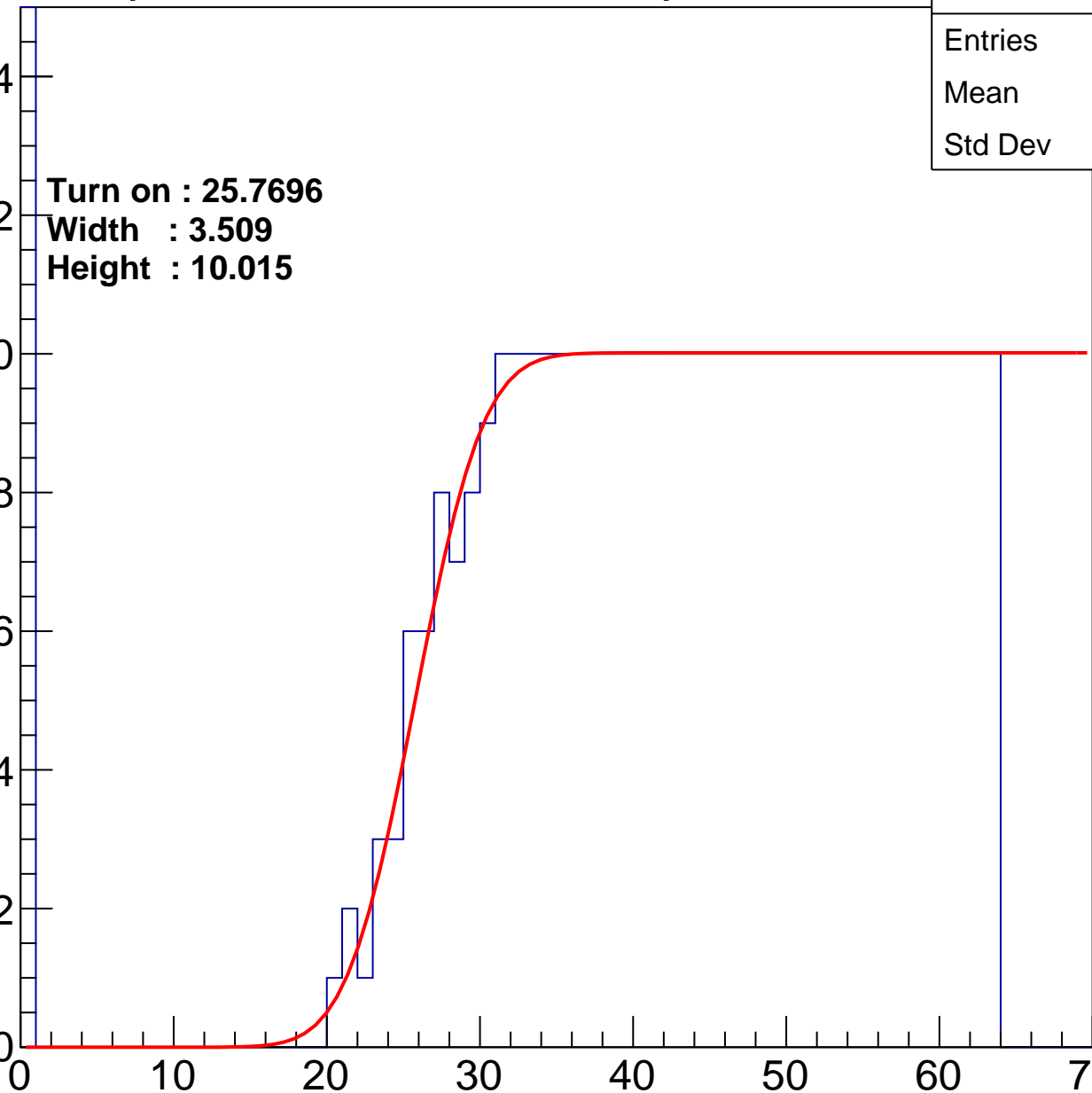
Width : 3.509

Height : 10.015

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch38

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	440
Mean	38.93
Std Dev	17.55

Turn on : 25.1495

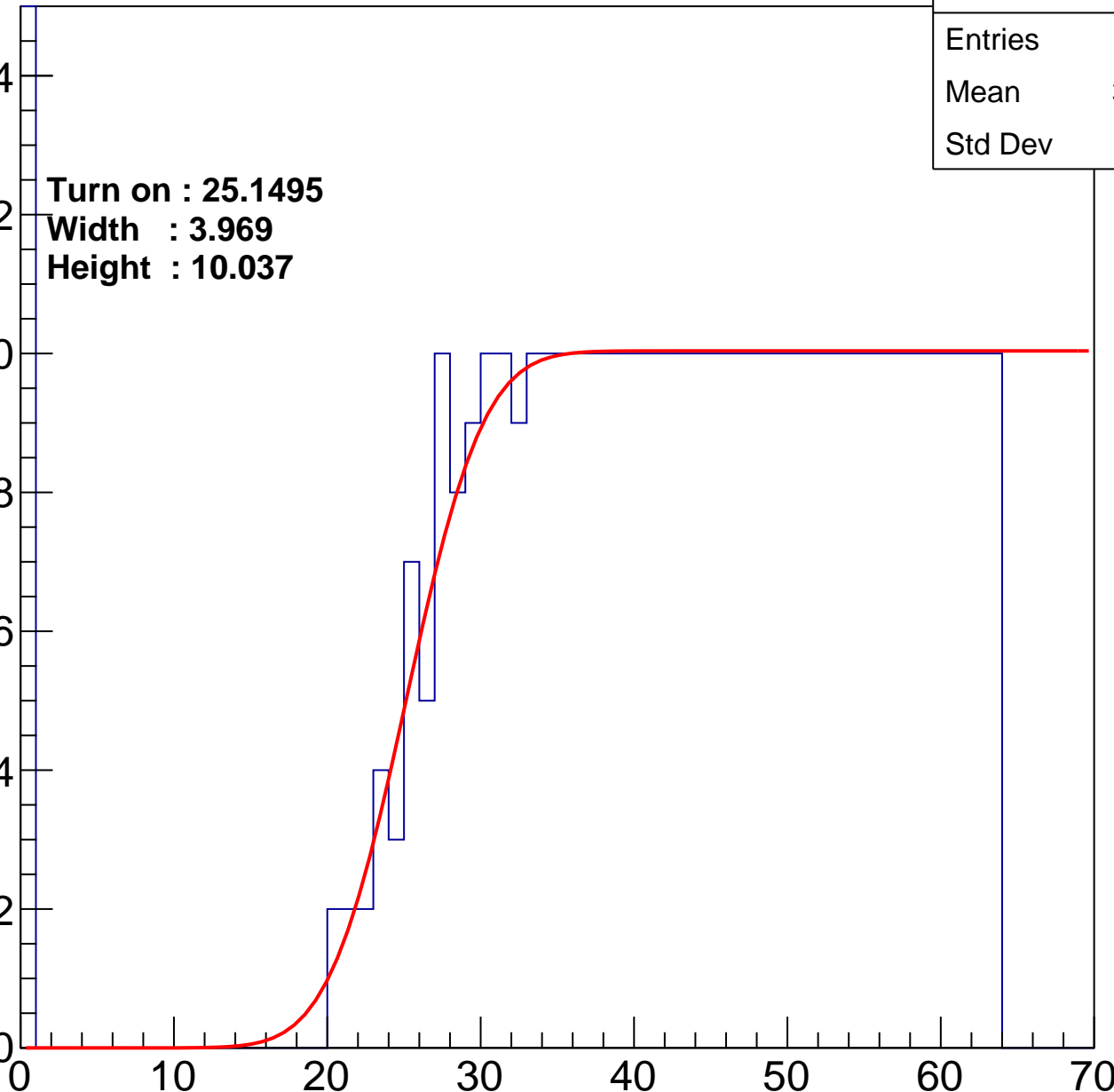
Width : 3.969

Height : 10.037

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U20-ch39

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	405
Mean	40.72
Std Dev	16.8

Turn on : 27.3532

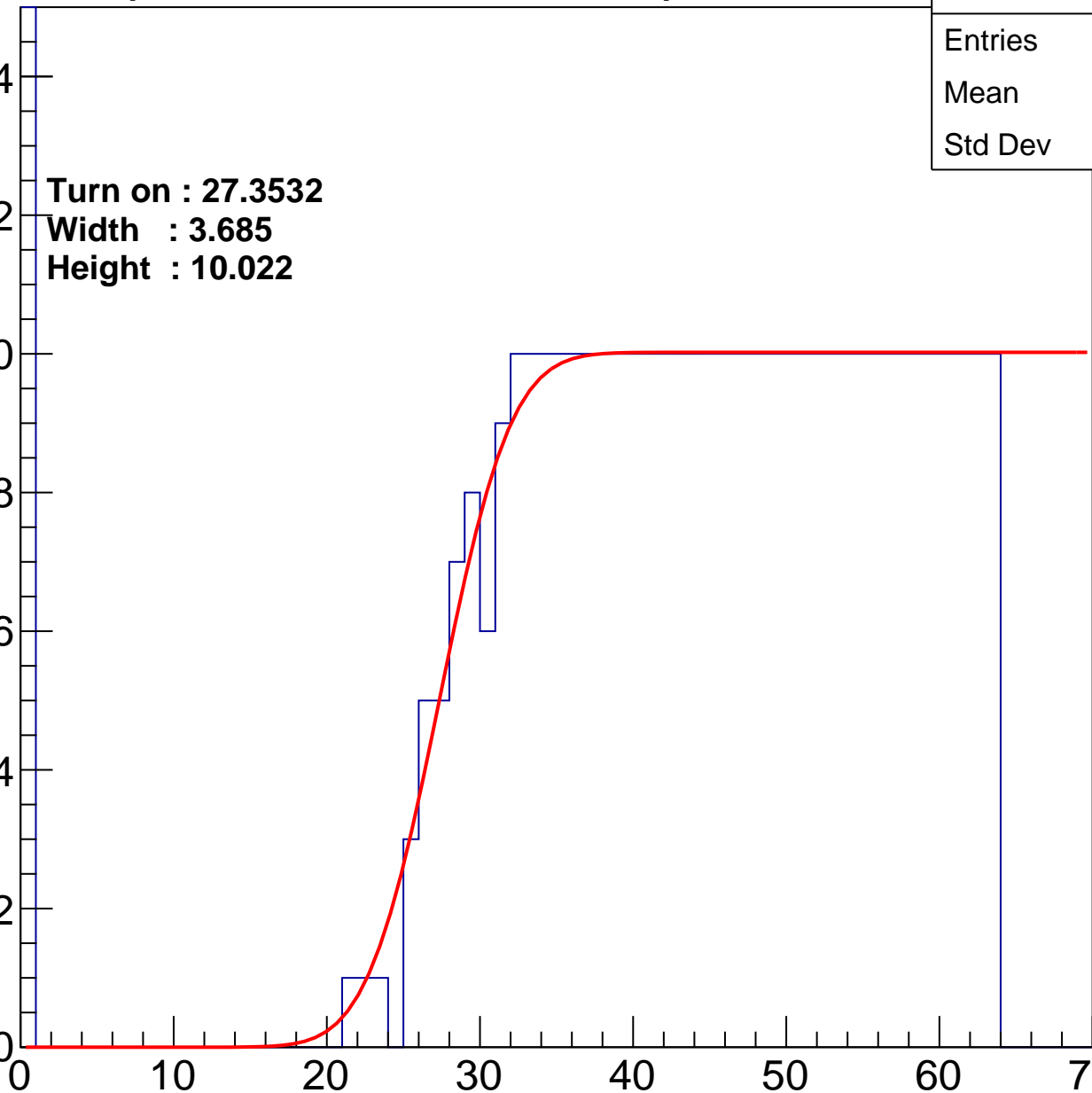
Width : 3.685

Height : 10.022

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch40

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	428
Mean	40.03
Std Dev	16.75

Turn on : 24.7293

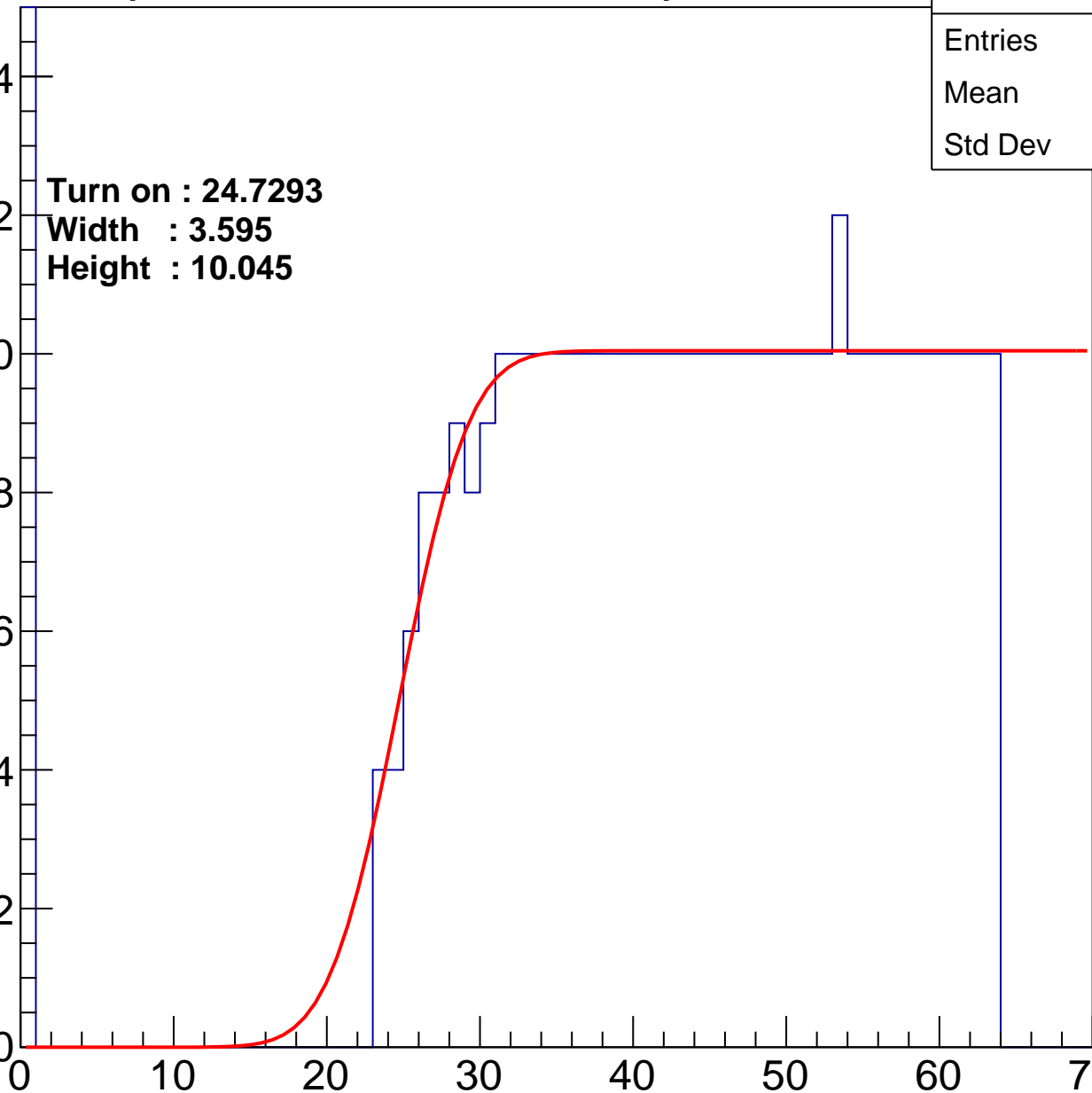
Width : 3.595

Height : 10.045

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch41

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	405
Mean	40.71
Std Dev	16.81

Turn on : 27.3011

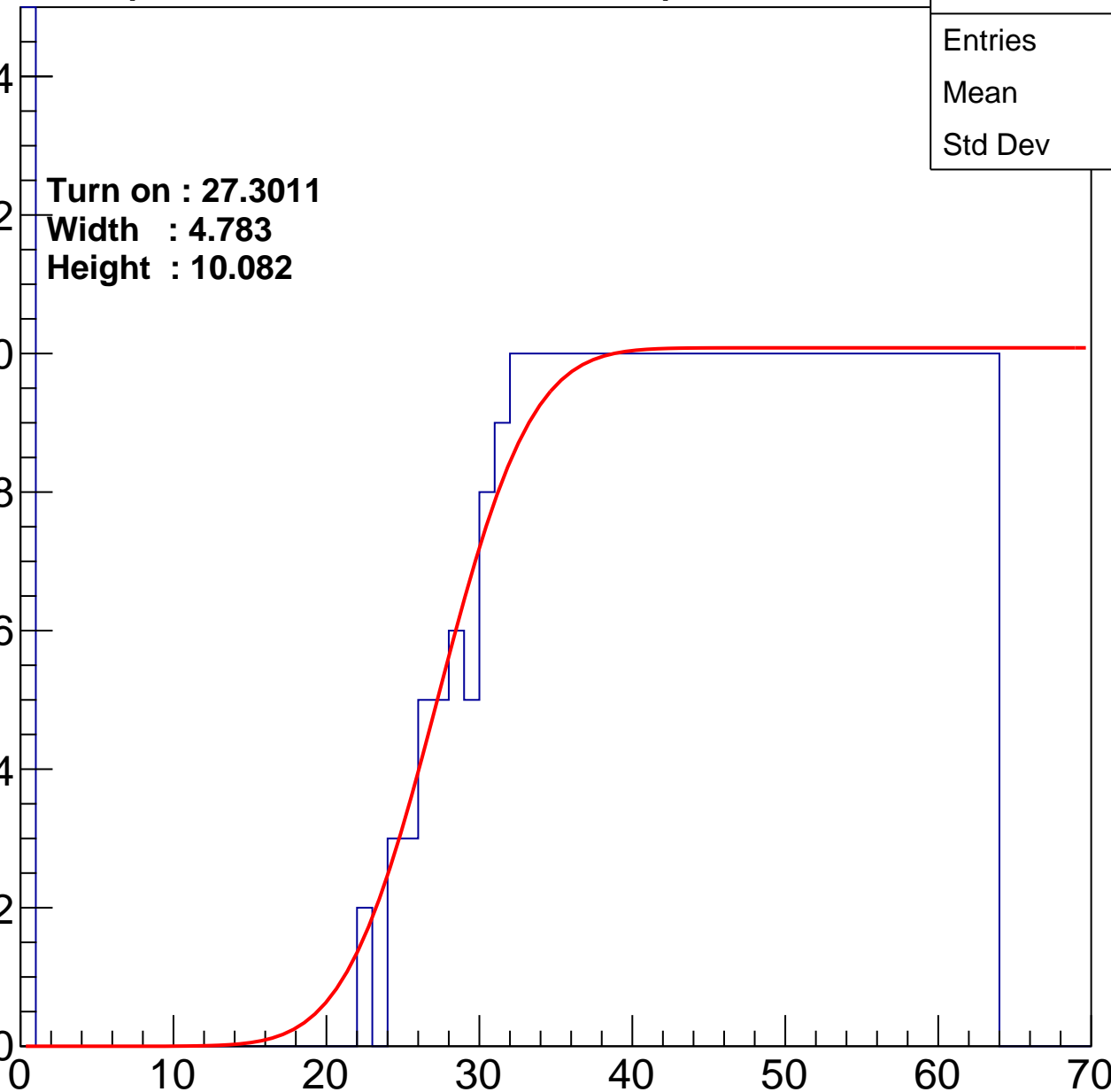
Width : 4.783

Height : 10.082

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch42

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	455
Mean	38.44
Std Dev	17.47

Turn on : 23.2950

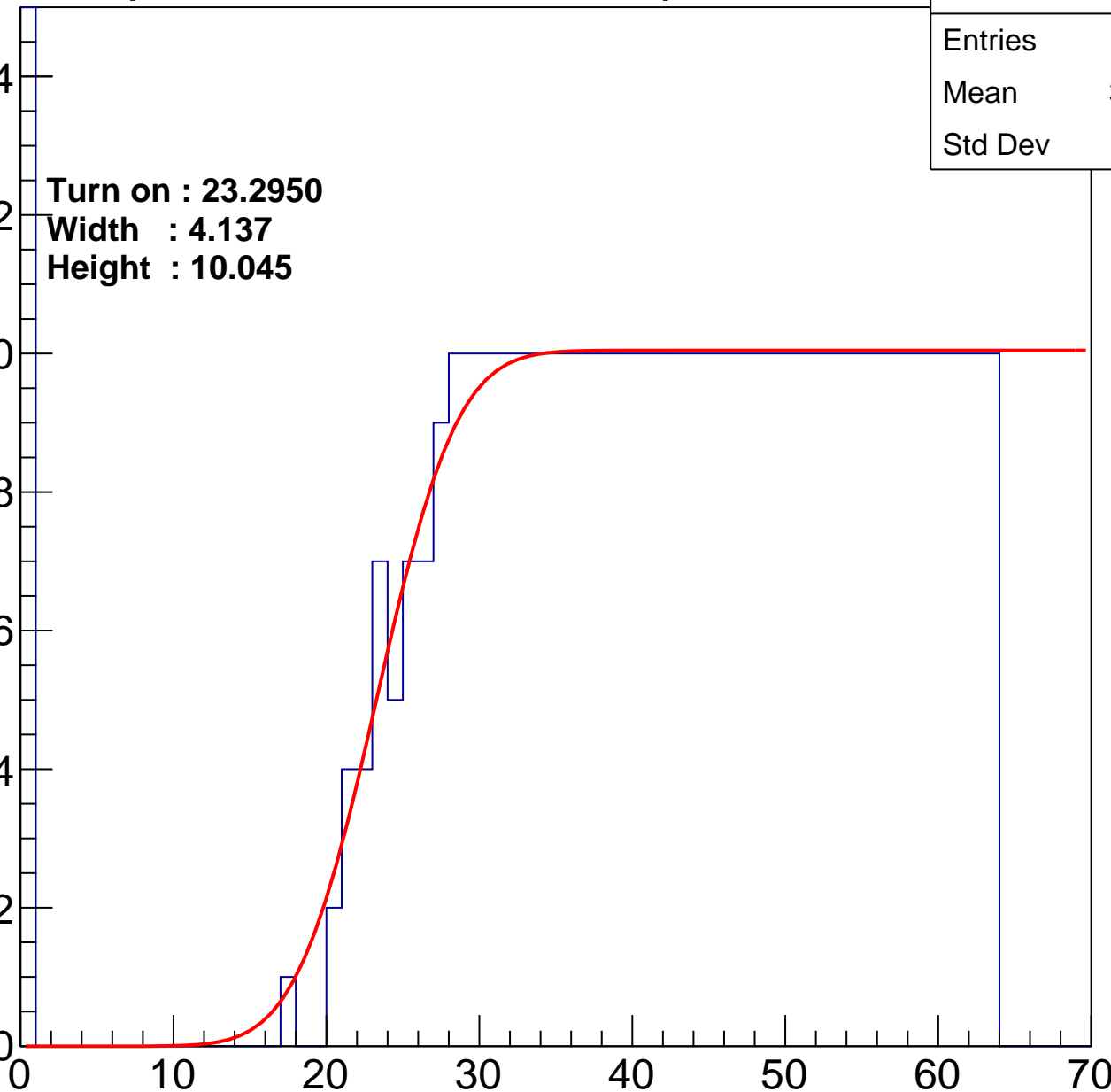
Width : 4.137

Height : 10.045

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch43

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	419
Mean	39.39
Std Dev	18.04

**Turn on : 27.4525**

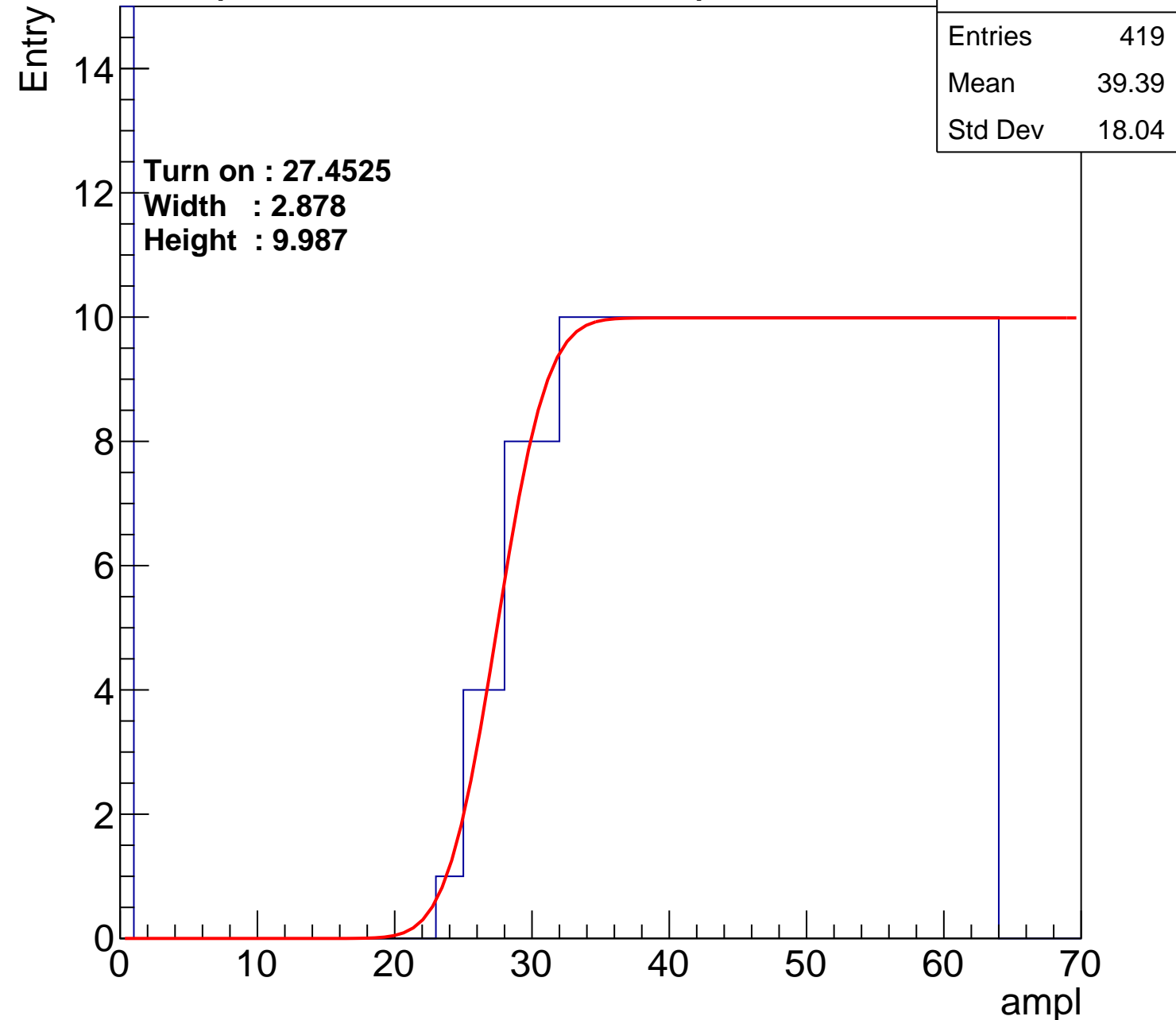
**Width : 2.878**

**Height : 9.987**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch44

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	449
Mean	38.24
Std Dev	18.07

Turn on : 25.1716

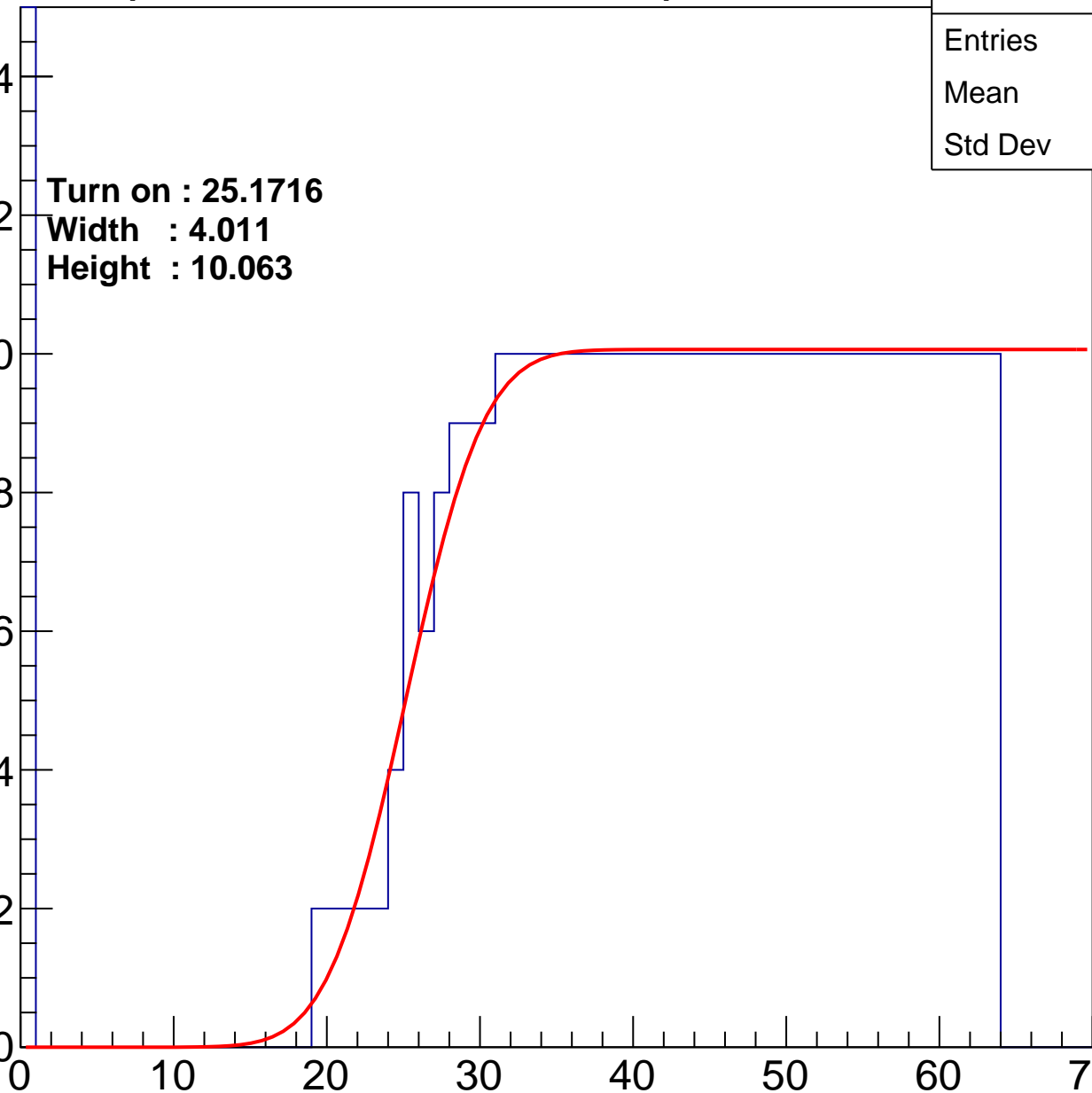
Width : 4.011

Height : 10.063

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch45

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	425
Mean	39.97
Std Dev	16.8

Turn on : 25.4828

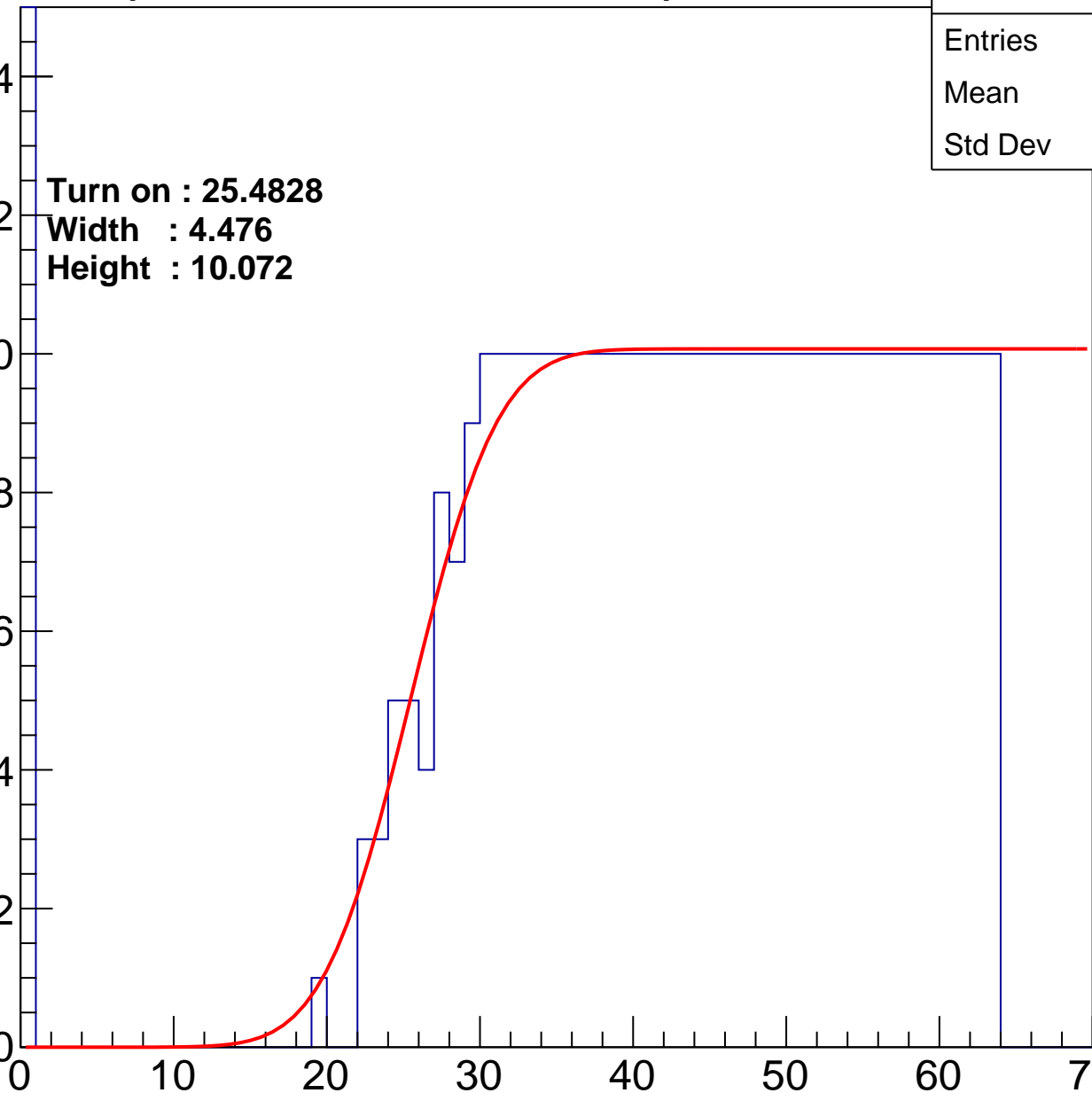
Width : 4.476

Height : 10.072

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch46

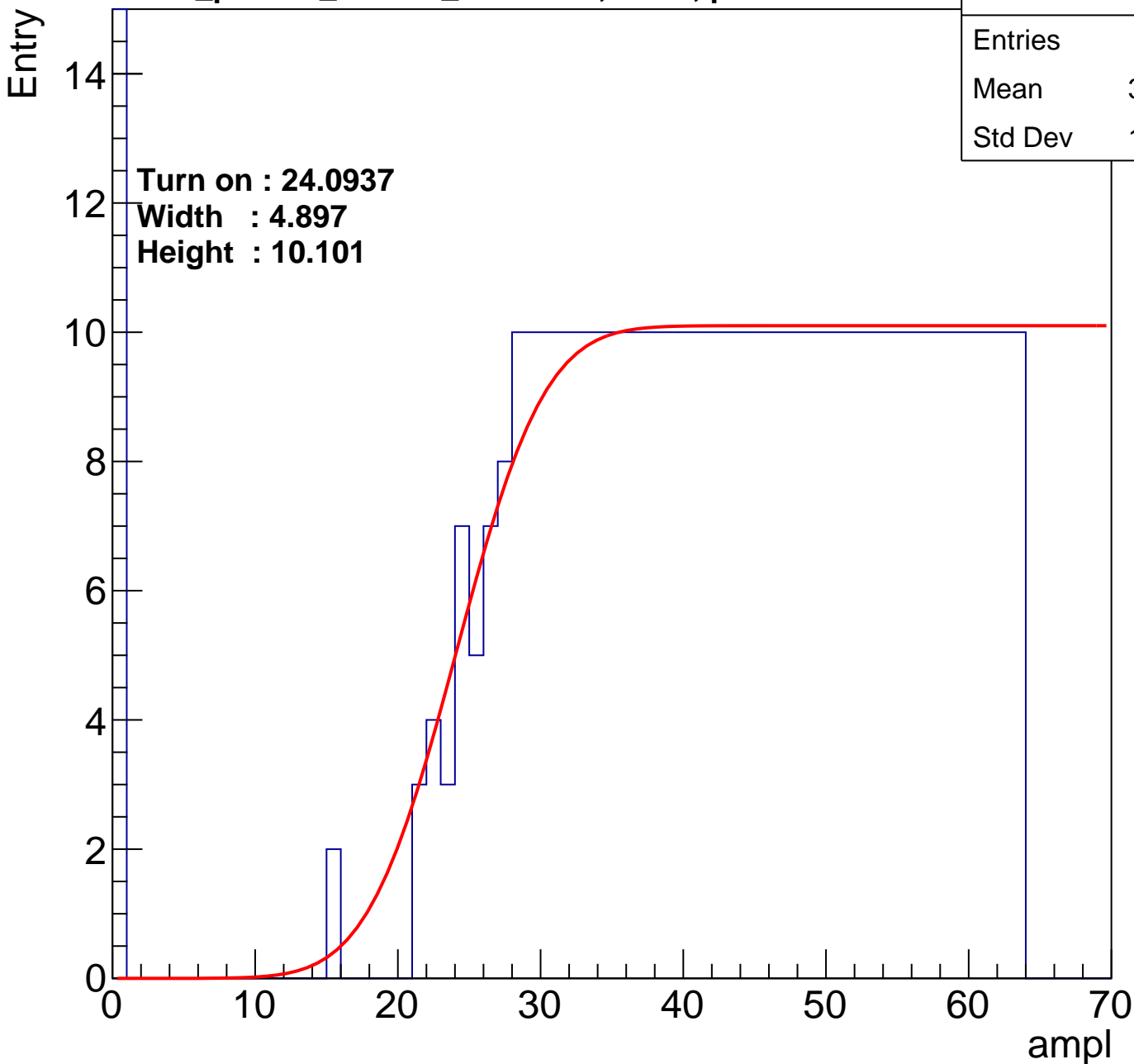
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	446
Mean	38.84
Std Dev	17.36

Turn on : 24.0937

Width : 4.897

Height : 10.101





# B1L103S, U20-ch47

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	432
Mean	39.43
Std Dev	17.24

Turn on : 25.4965

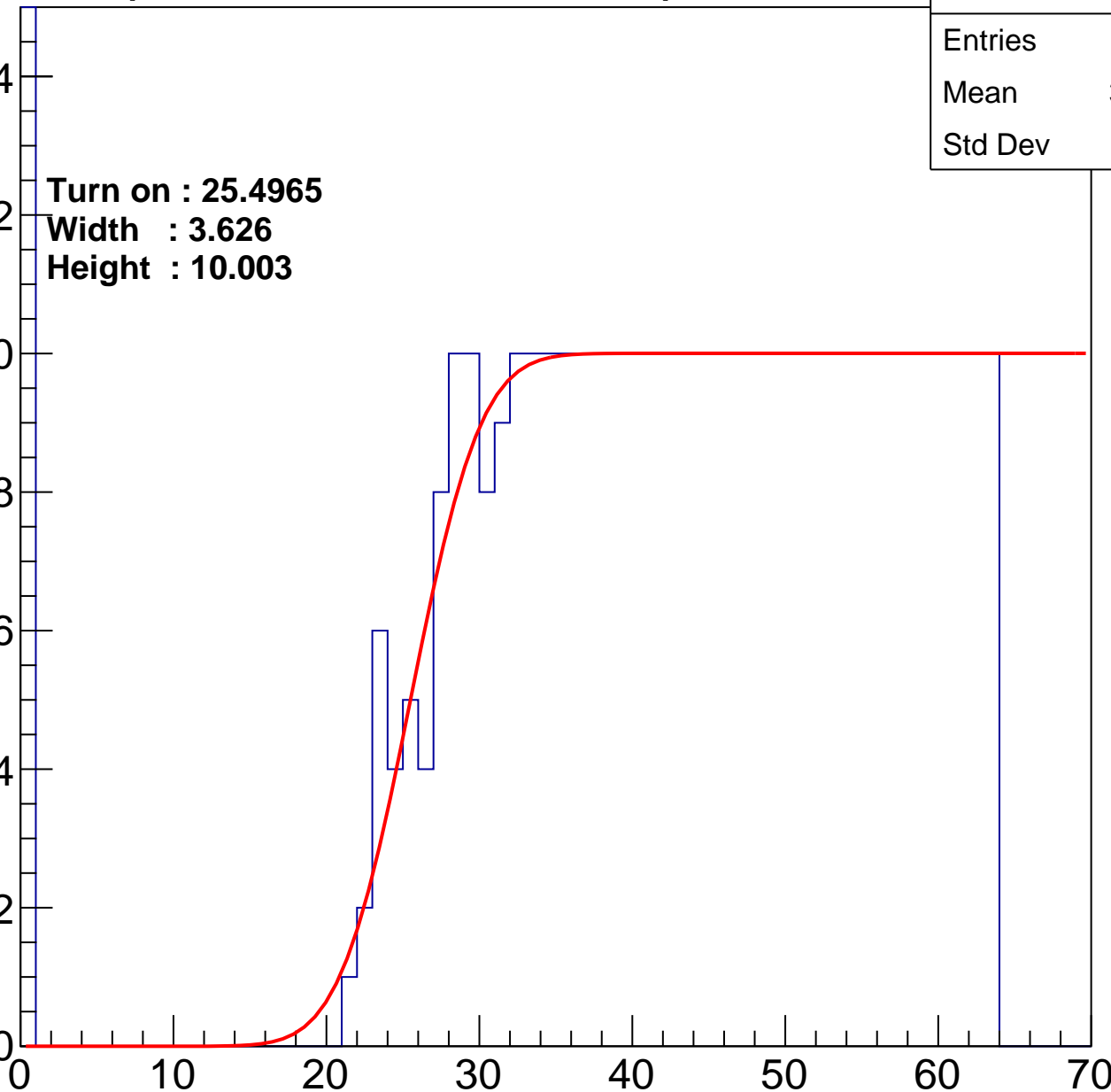
Width : 3.626

Height : 10.003

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch48

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	466
Mean	38.32
Std Dev	17.05

Turn on : 21.5373

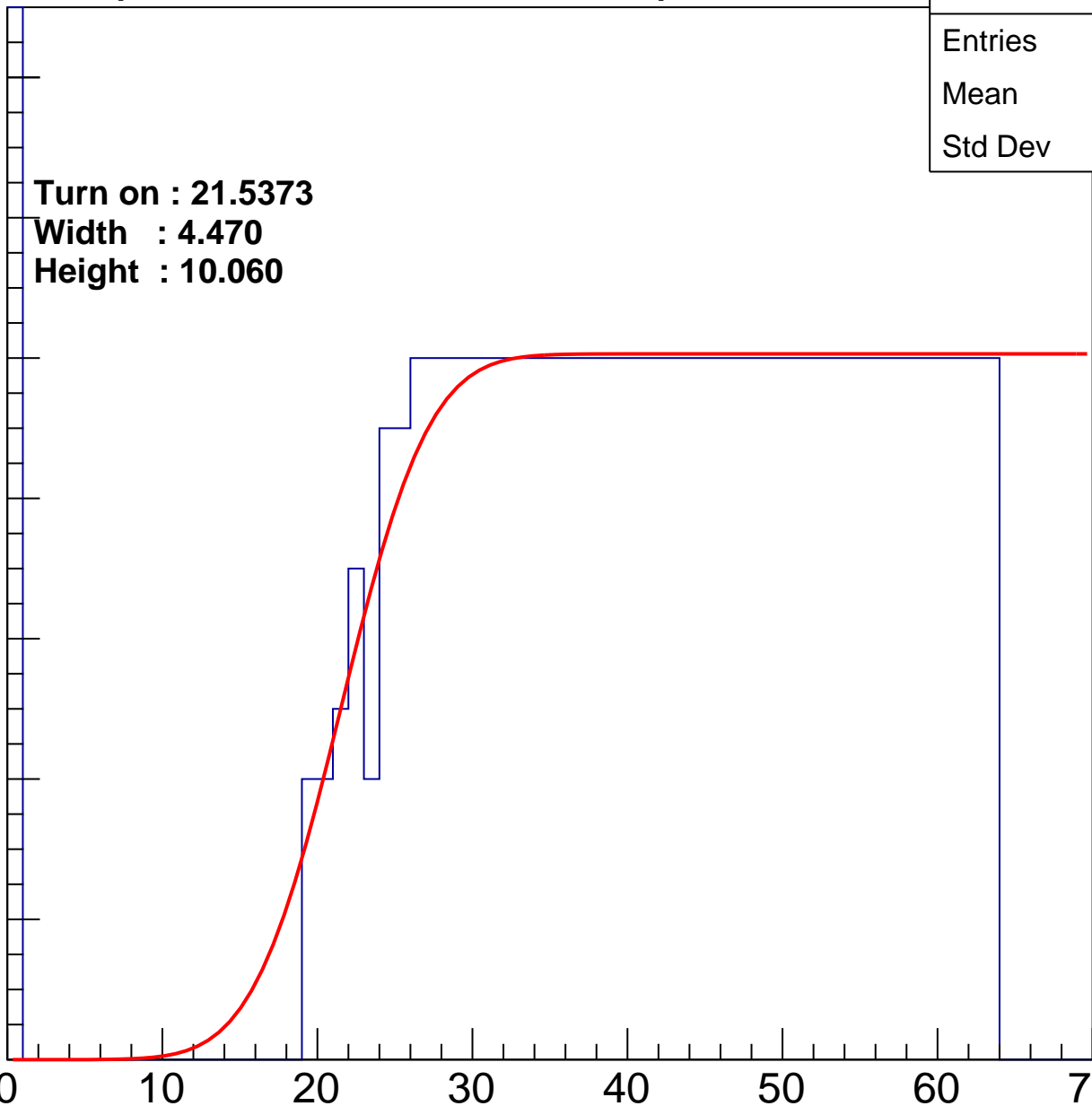
Width : 4.470

Height : 10.060

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch49

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	424
Mean	39.7
Std Dev	17.33

Turn on : 26.6192

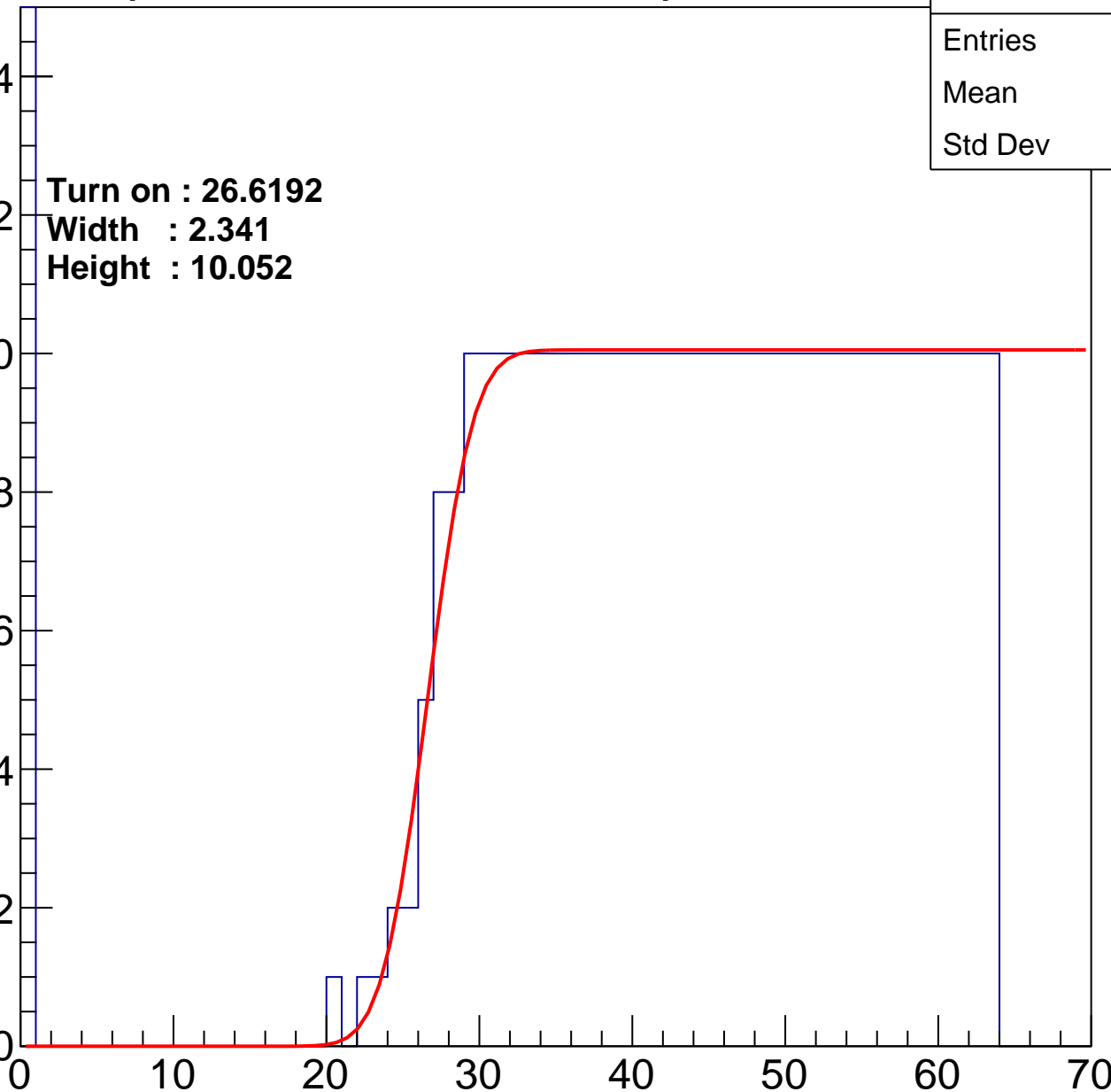
Width : 2.341

Height : 10.052

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch50

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	424
Mean	39.77
Std Dev	17.18

**Turn on : 26.3959**

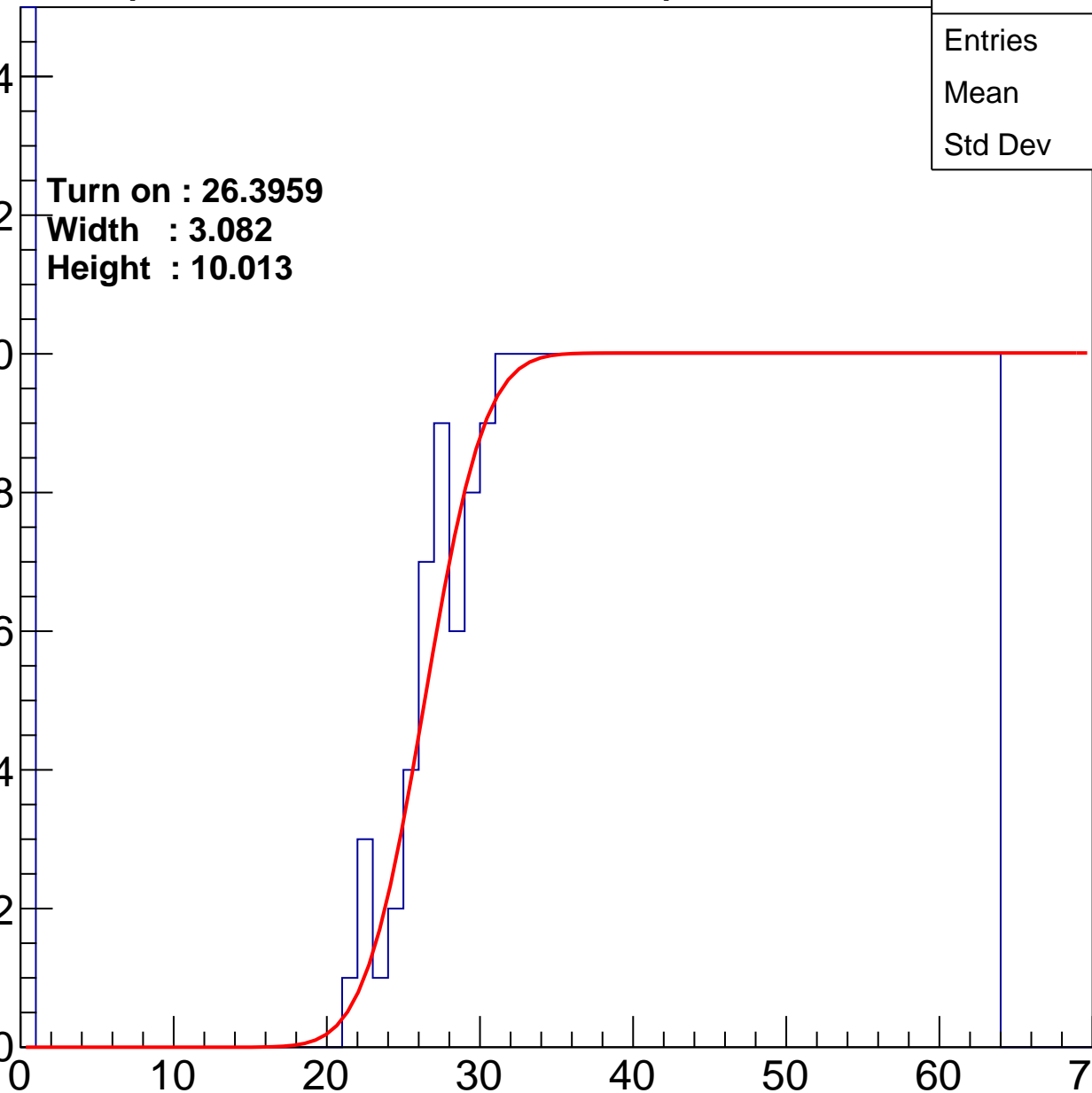
**Width : 3.082**

**Height : 10.013**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch51

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	435
Mean	39.18
Std Dev	17.47

Turn on : 25.7240

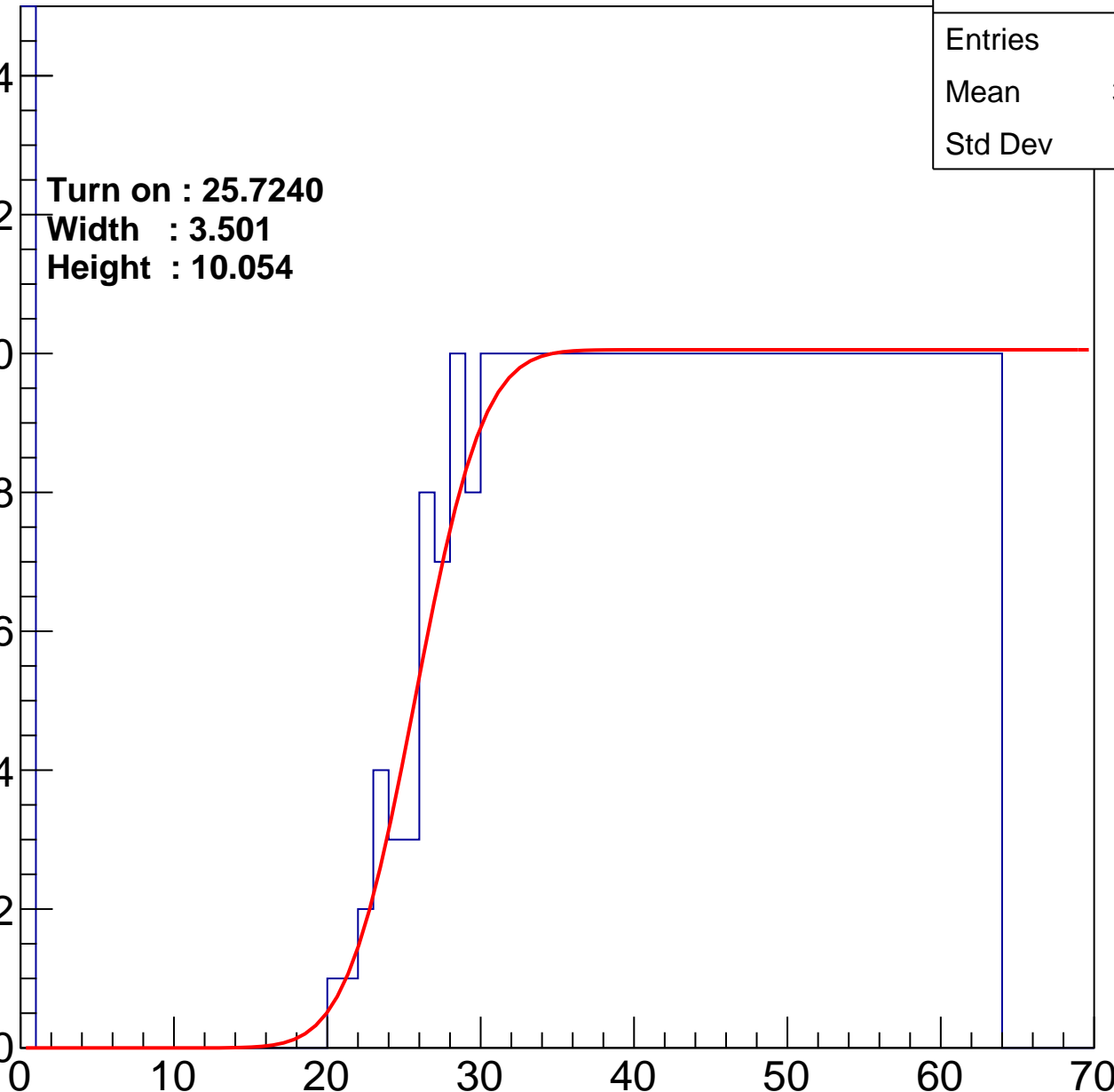
Width : 3.501

Height : 10.054

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch52

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	434
Mean	39.44
Std Dev	17.12

Turn on : 25.0050

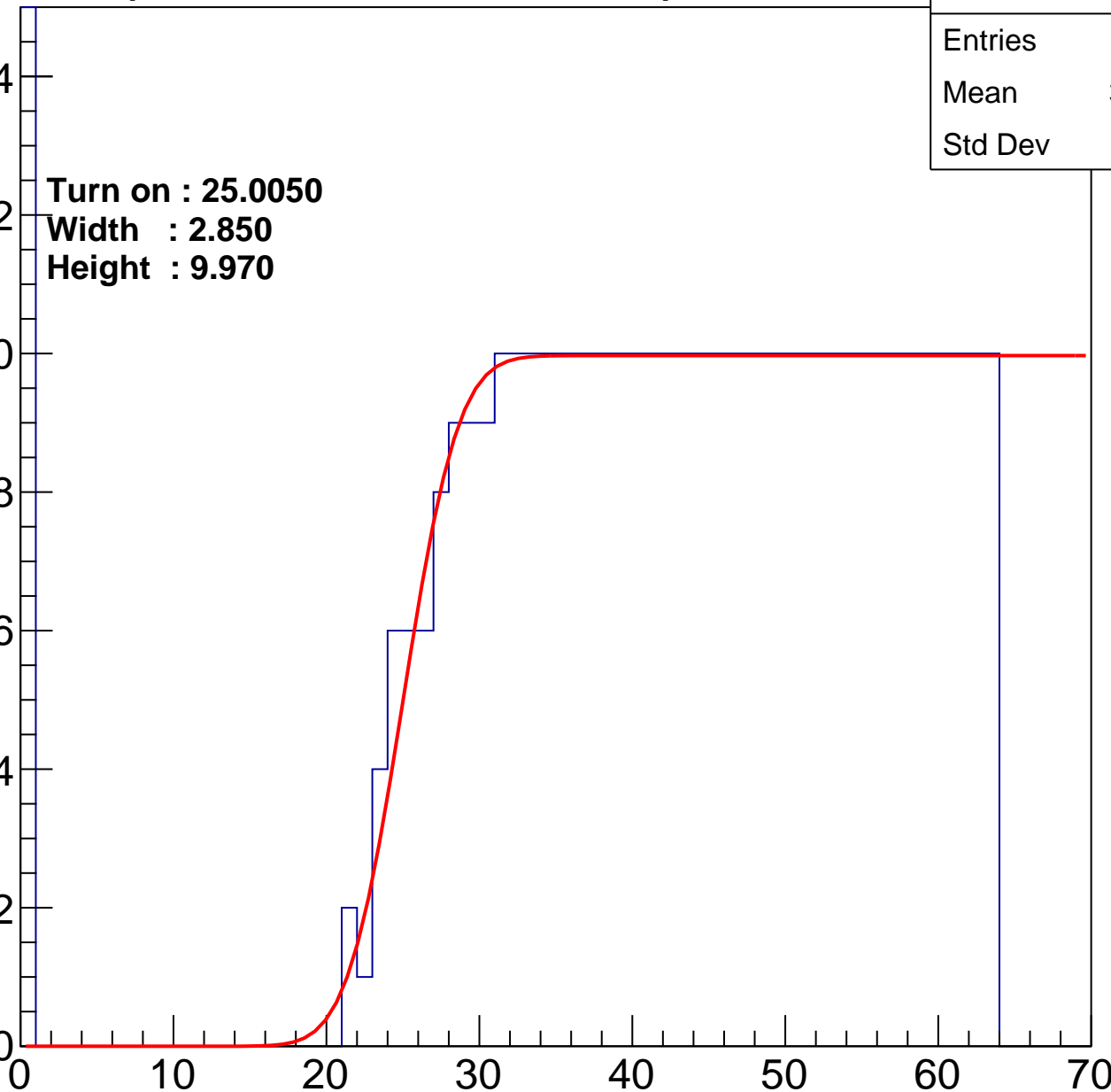
Width : 2.850

Height : 9.970

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch53

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	407
Mean	40.46
Std Dev	17.09

Turn on : 27.3820

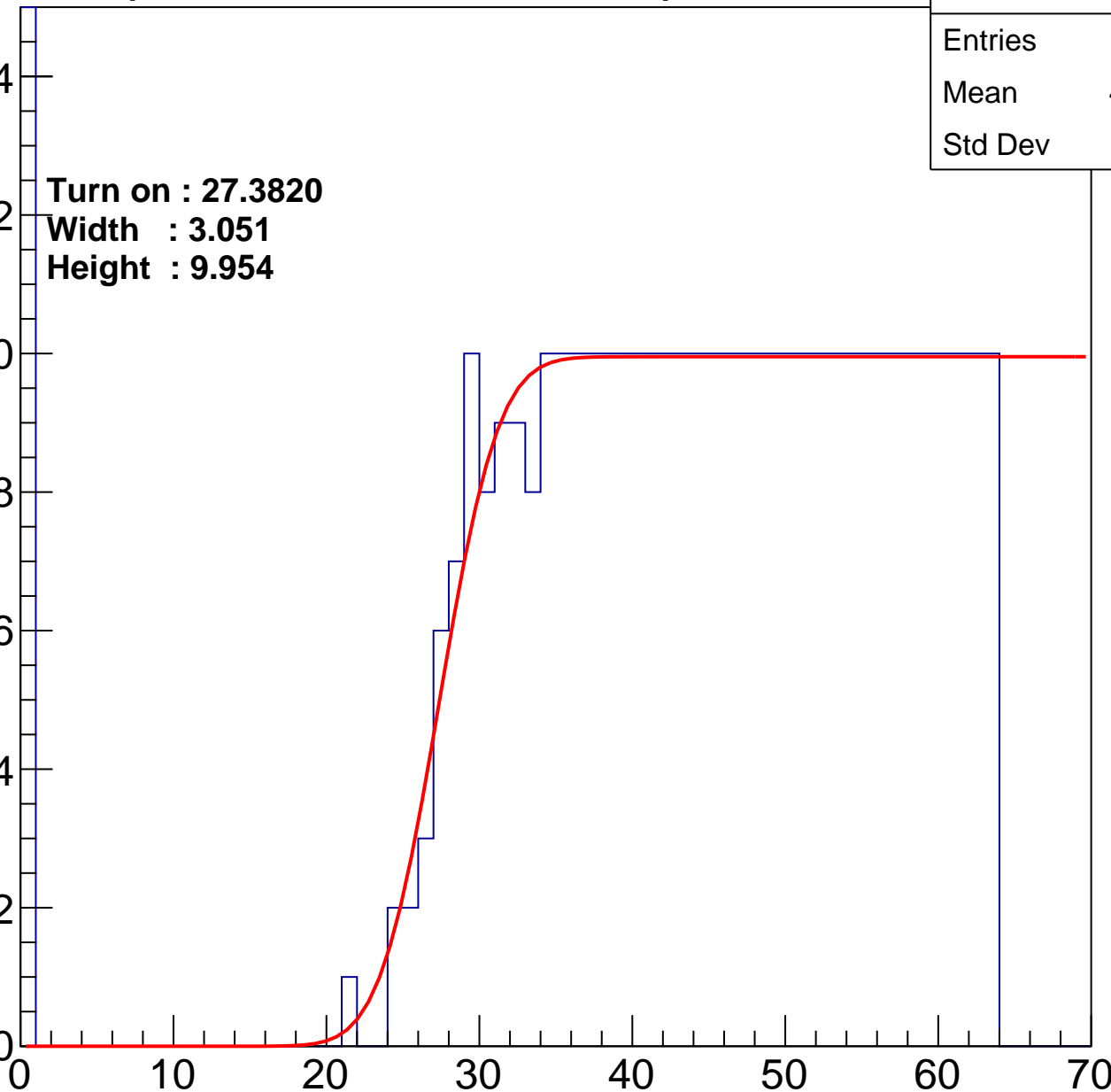
Width : 3.051

Height : 9.954

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch54

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	427
Mean	39.79
Std Dev	16.92

Turn on : 25.5678

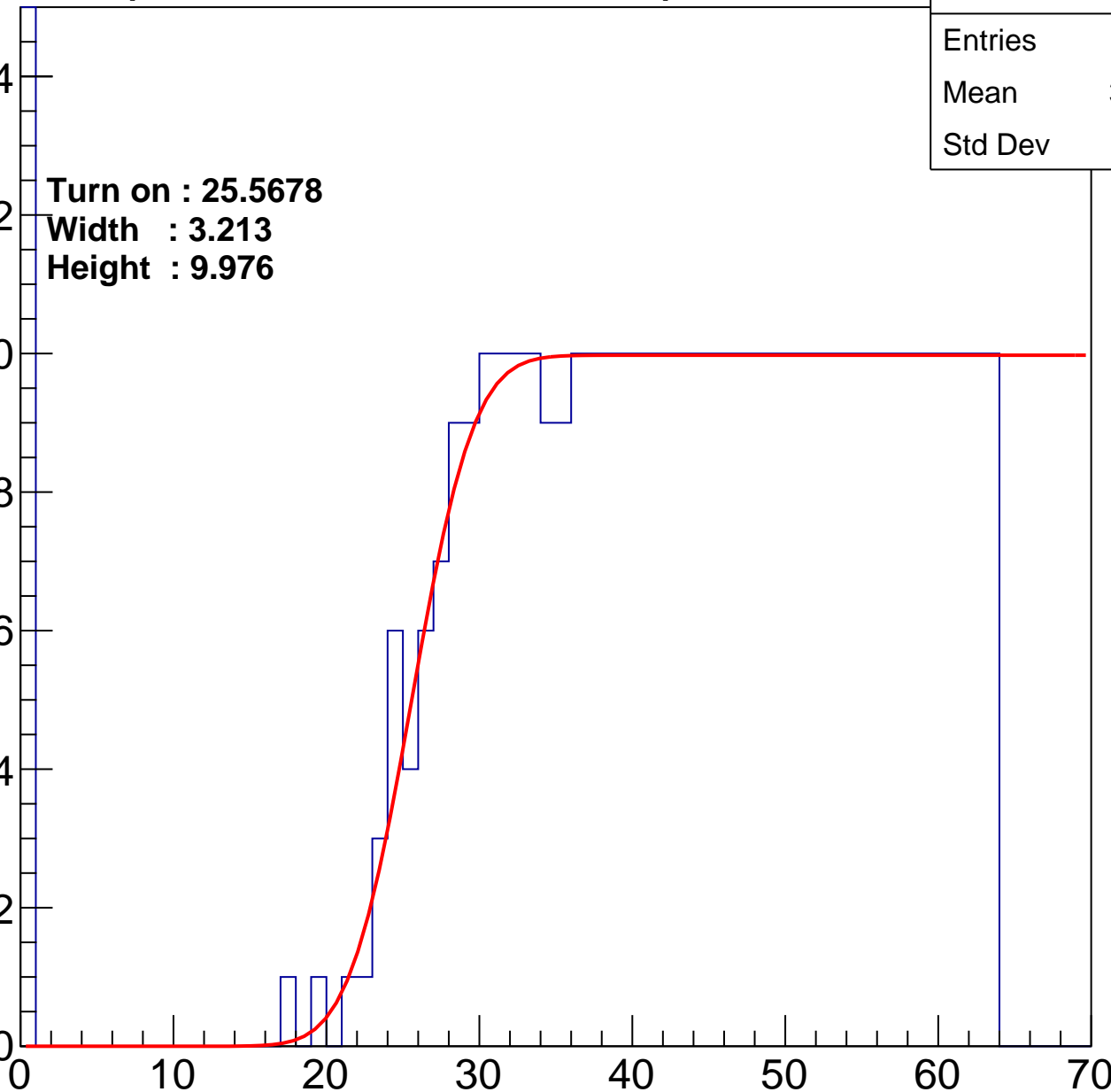
Width : 3.213

Height : 9.976

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U20-ch55

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	430
Mean	39.35
Std Dev	17.5

Turn on : 26.2605

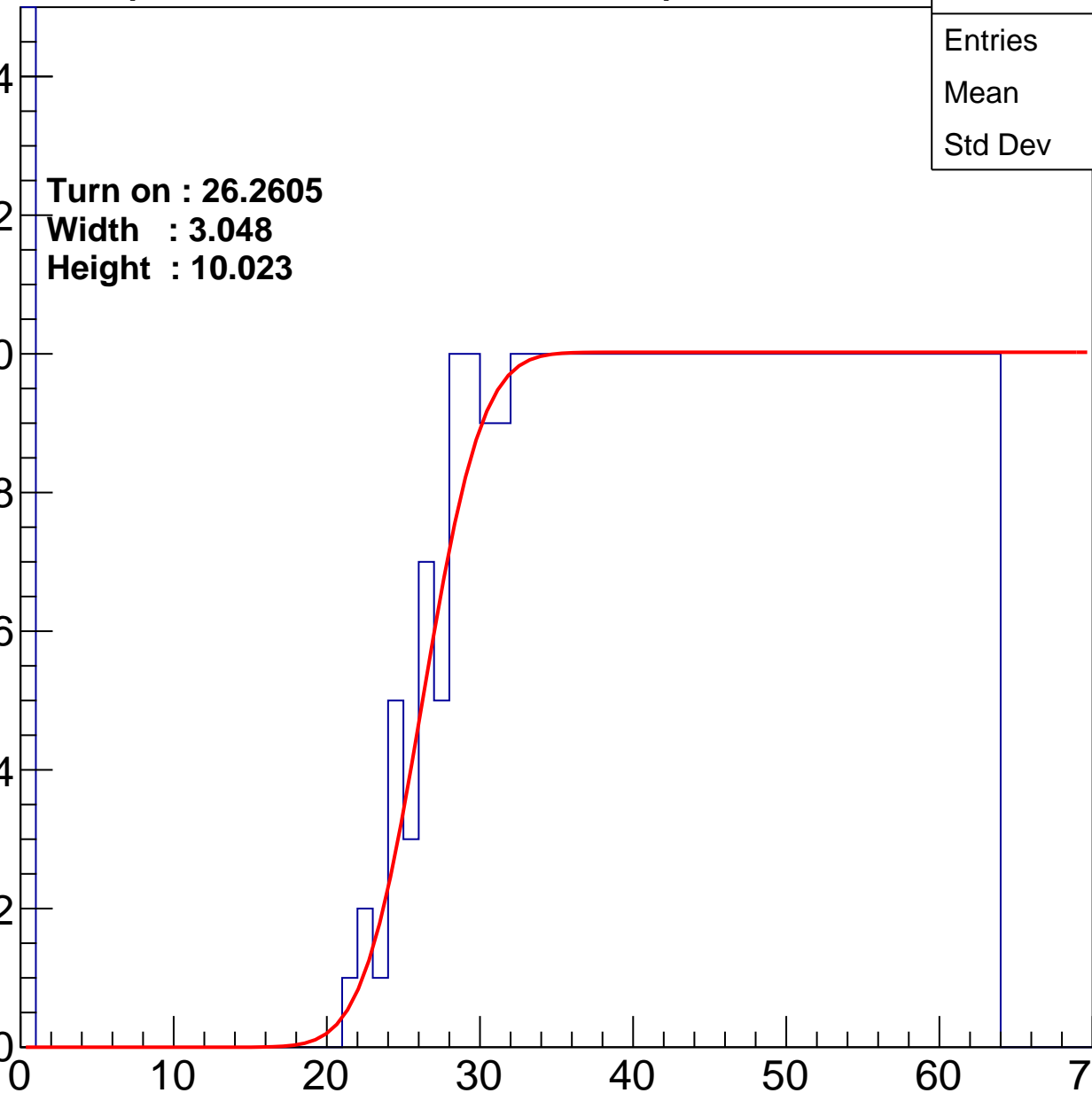
Width : 3.048

Height : 10.023

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch56

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	466
Mean	38.32
Std Dev	17.05

Turn on : 22.3241

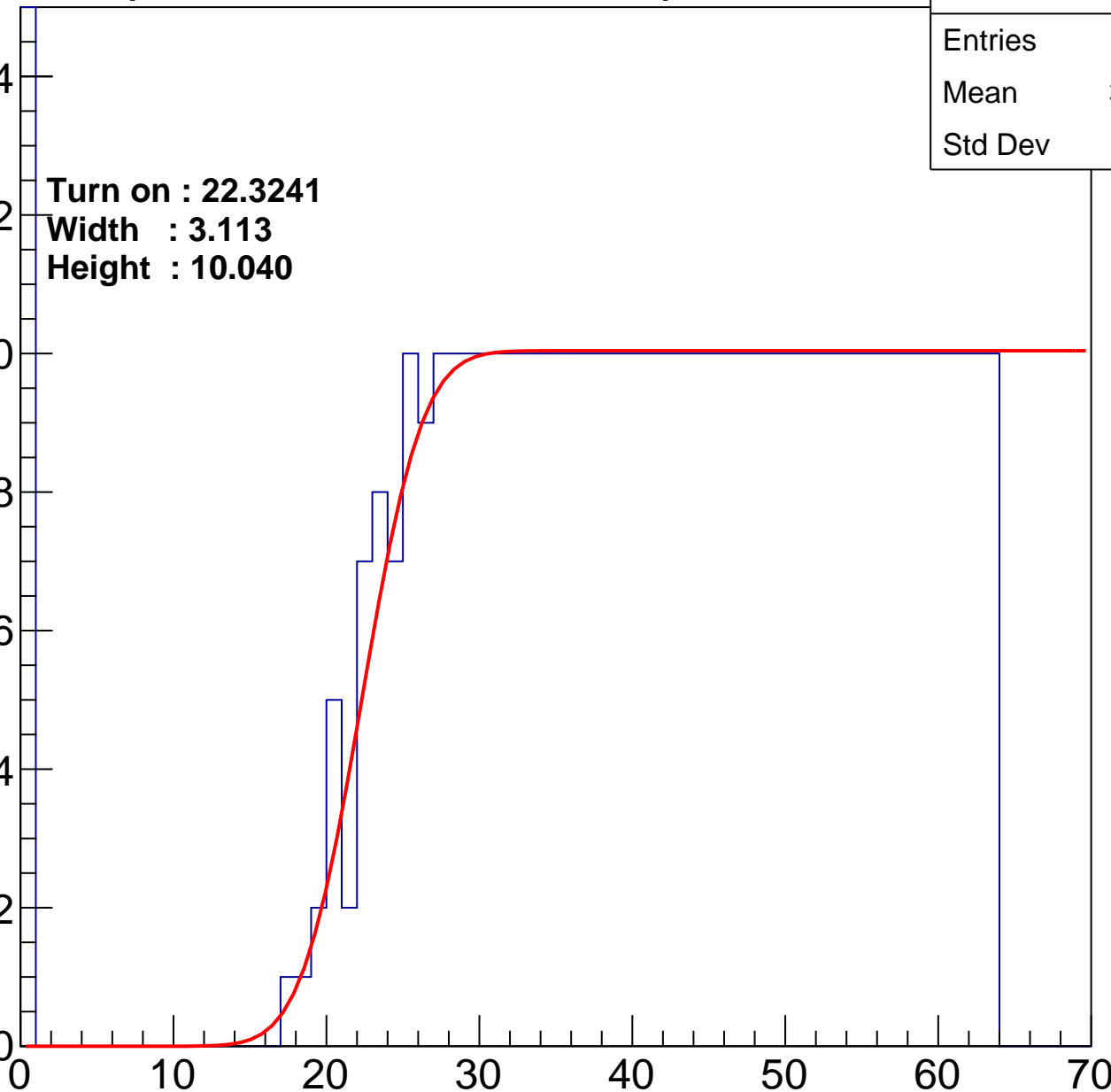
Width : 3.113

Height : 10.040

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch57

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	421
Mean	40.22
Std Dev	16.67

Turn on : 25.1303

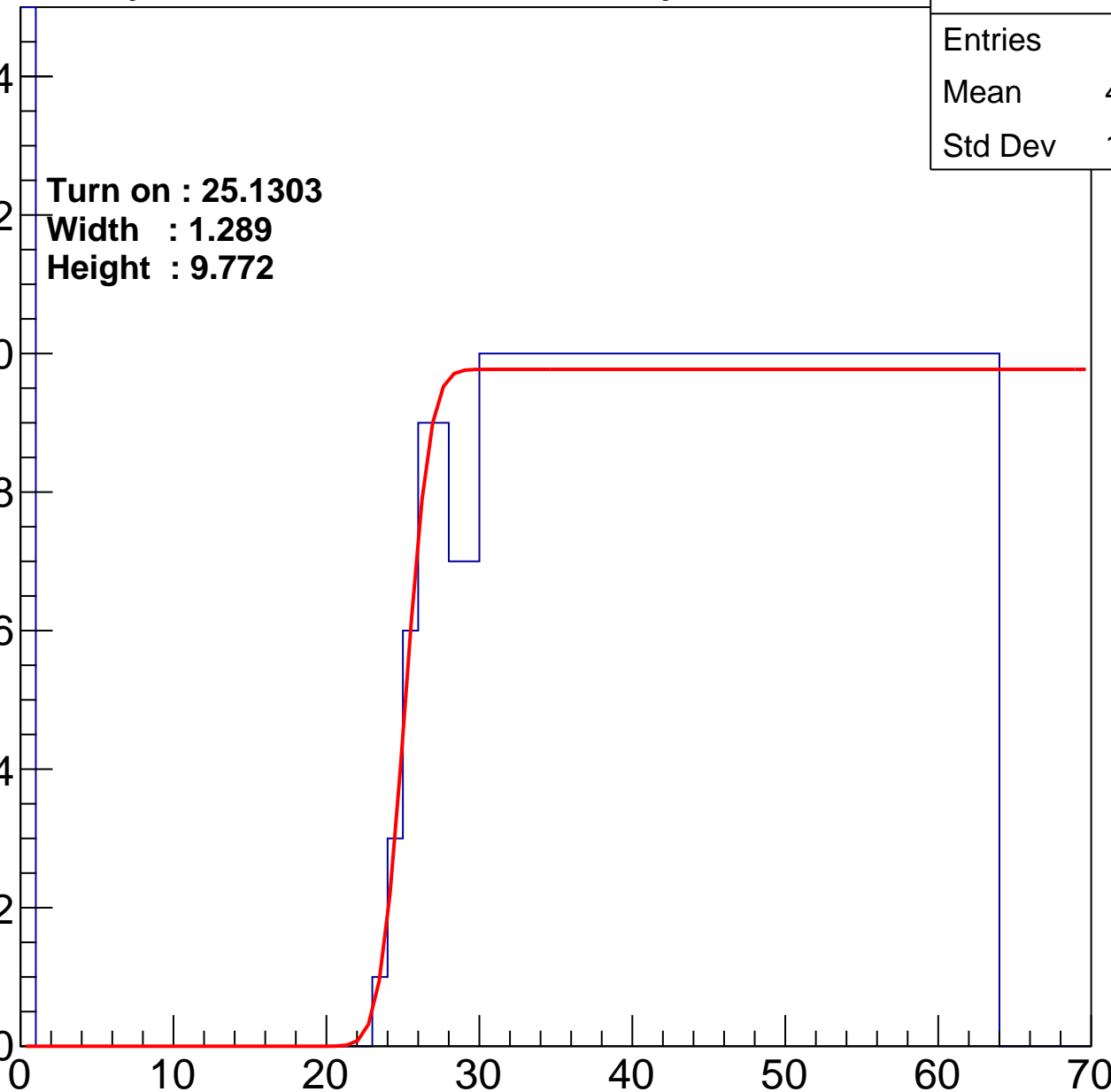
Width : 1.289

Height : 9.772

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch58

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	432
Mean	39.23
Std Dev	17.53

Turn on : 26.4848

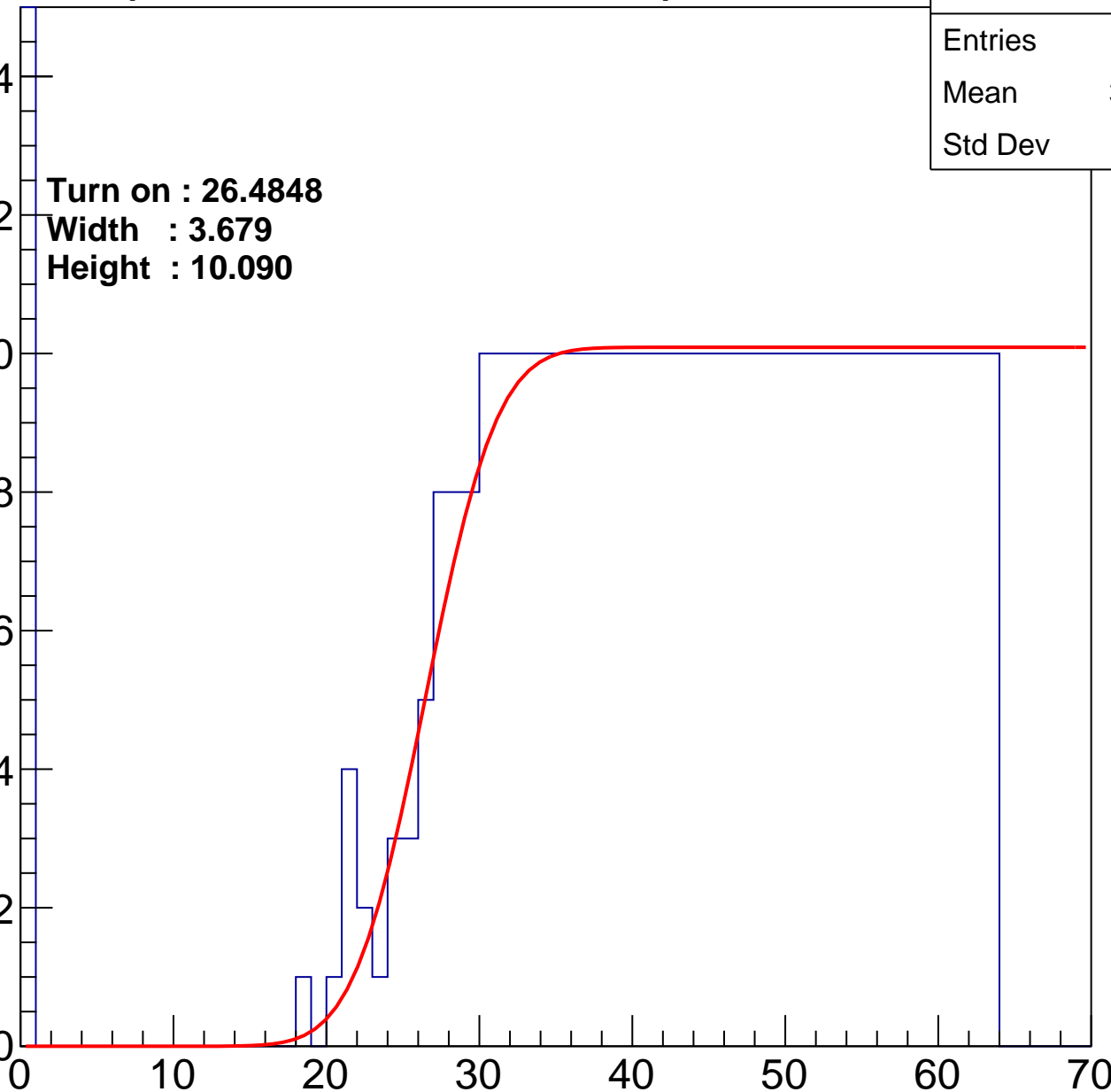
Width : 3.679

Height : 10.090

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch59

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	416
Mean	39.24
Std Dev	18.42

Turn on : 27.8506

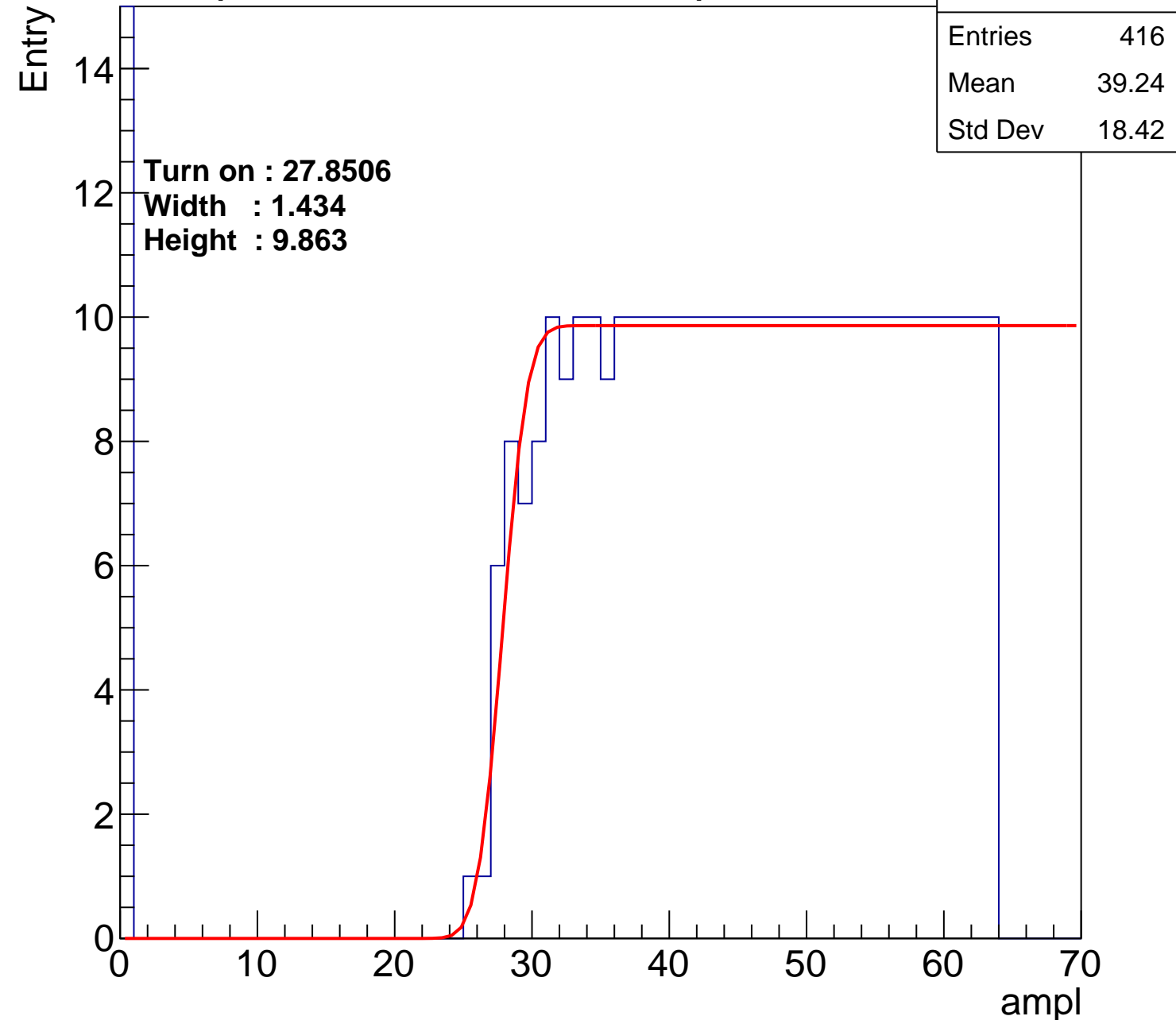
Width : 1.434

Height : 9.863

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch60

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	470
Mean	37.18
Std Dev	18.53

Turn on : 23.5561

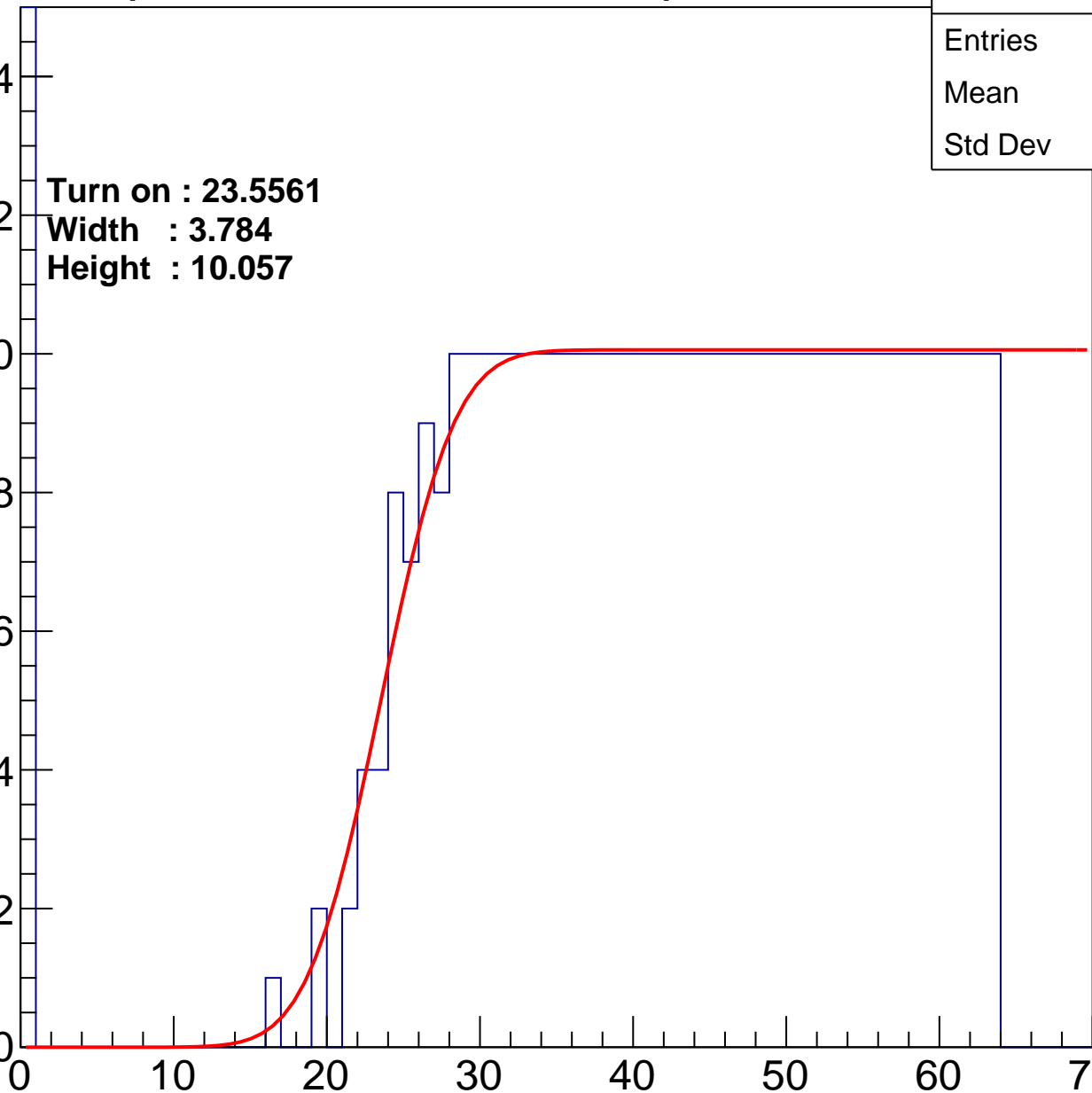
Width : 3.784

Height : 10.057

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch61

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	427
Mean	39.48
Std Dev	17.49

Turn on : 26.3311

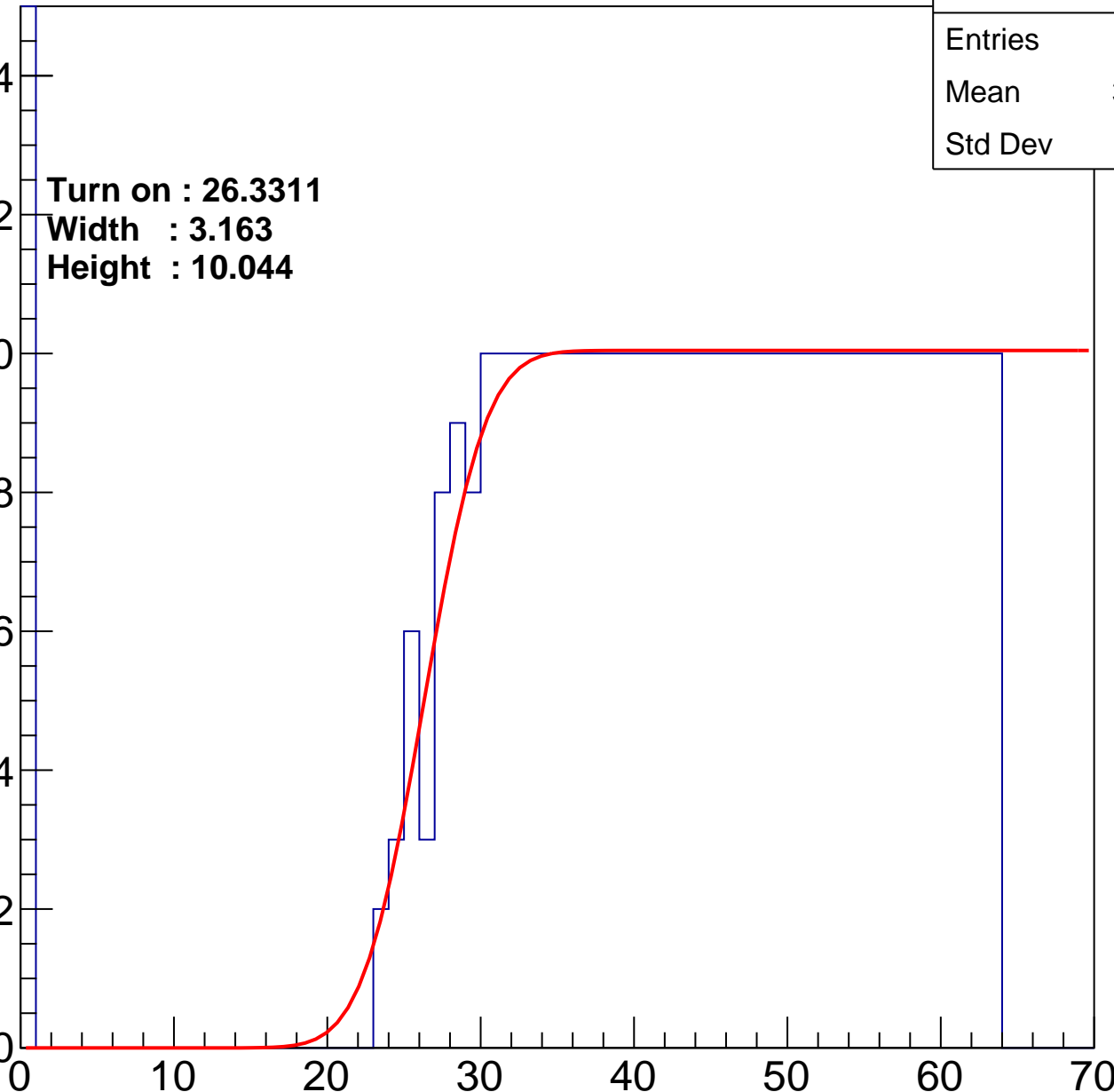
Width : 3.163

Height : 10.044

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch62

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	427
Mean	39.78
Std Dev	16.99

Turn on : 25.4356

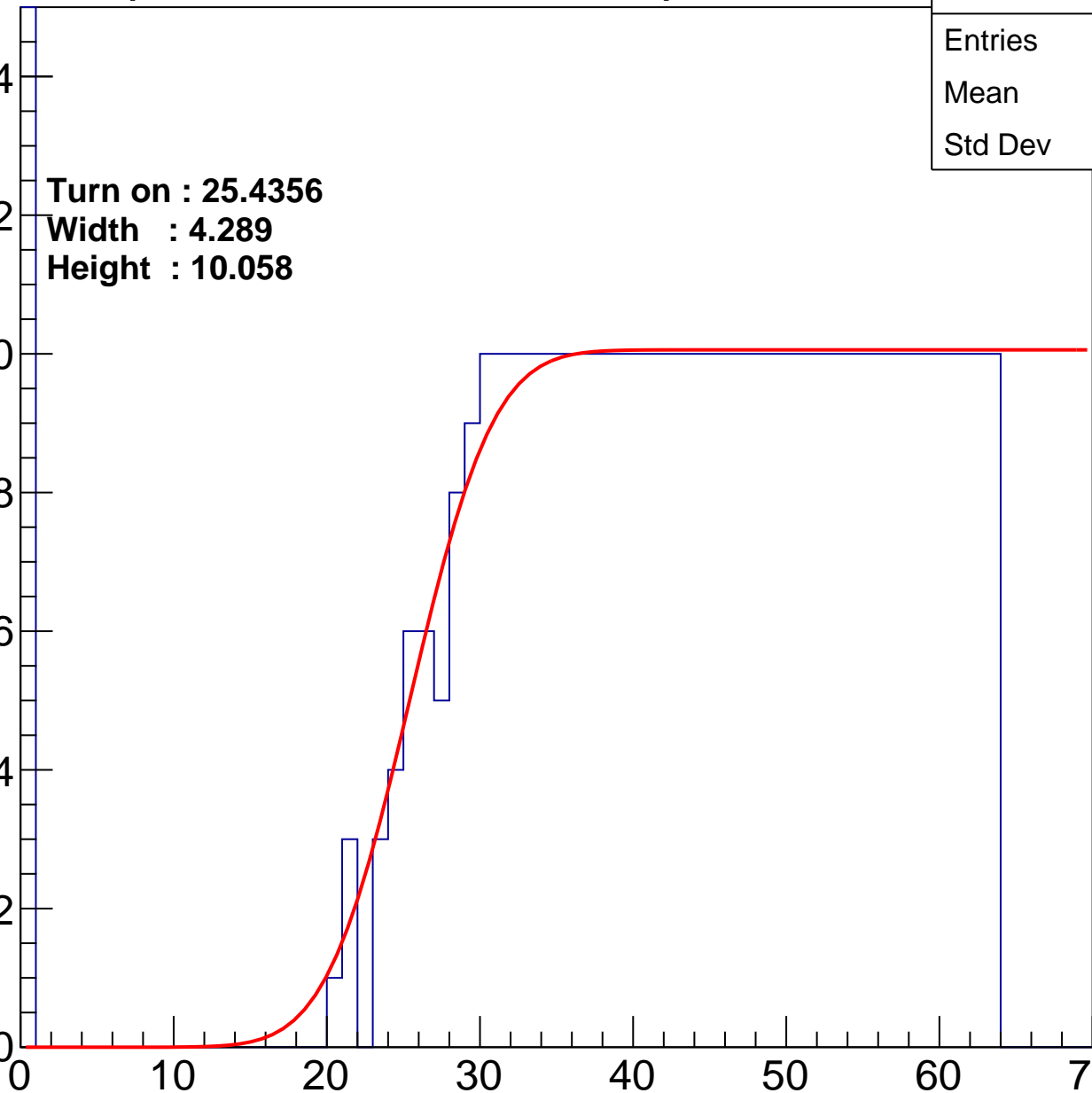
Width : 4.289

Height : 10.058

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U20-ch63

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	425
Mean	39.85
Std Dev	16.99

Turn on : 25.9403

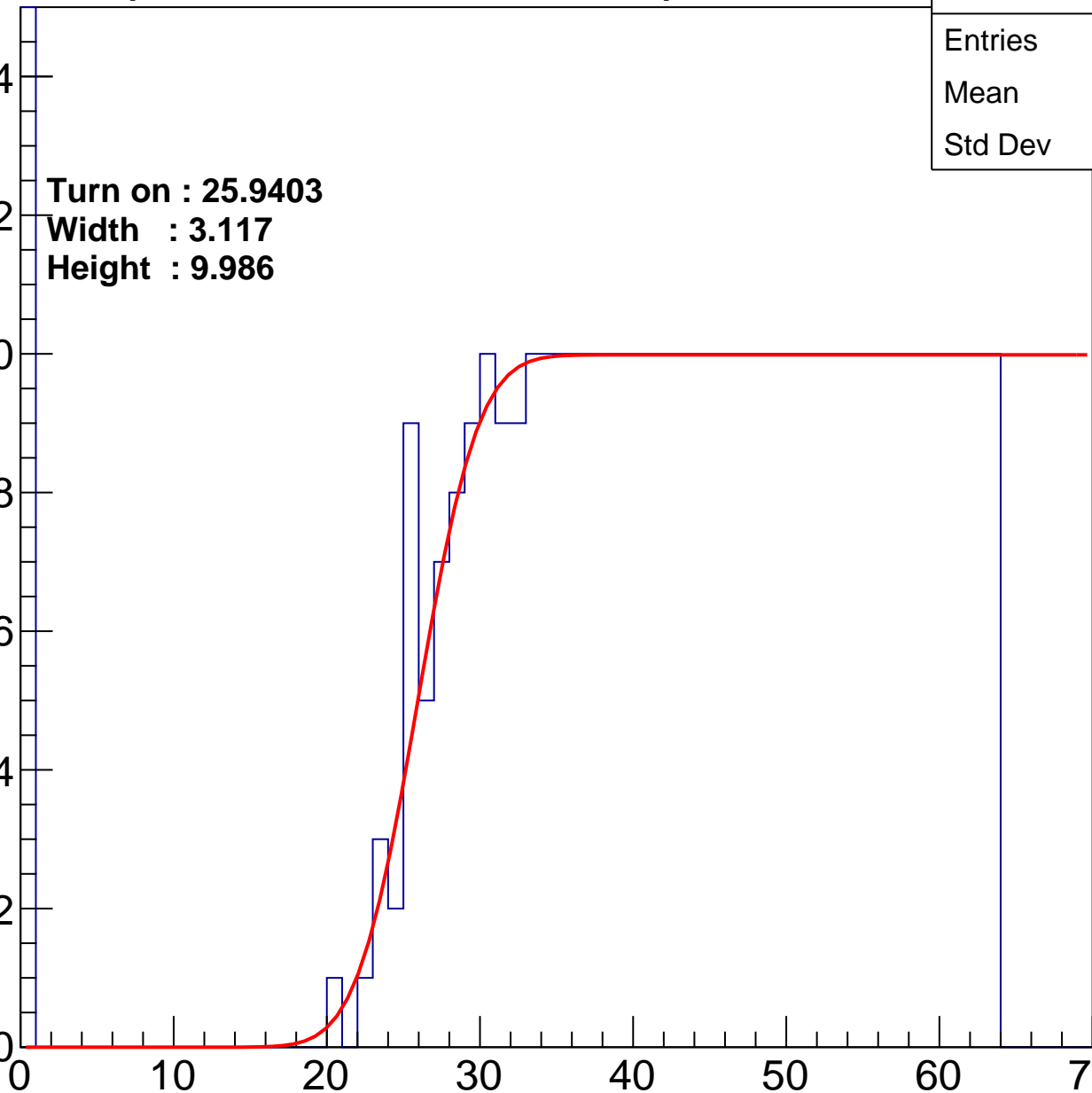
Width : 3.117

Height : 9.986

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch64

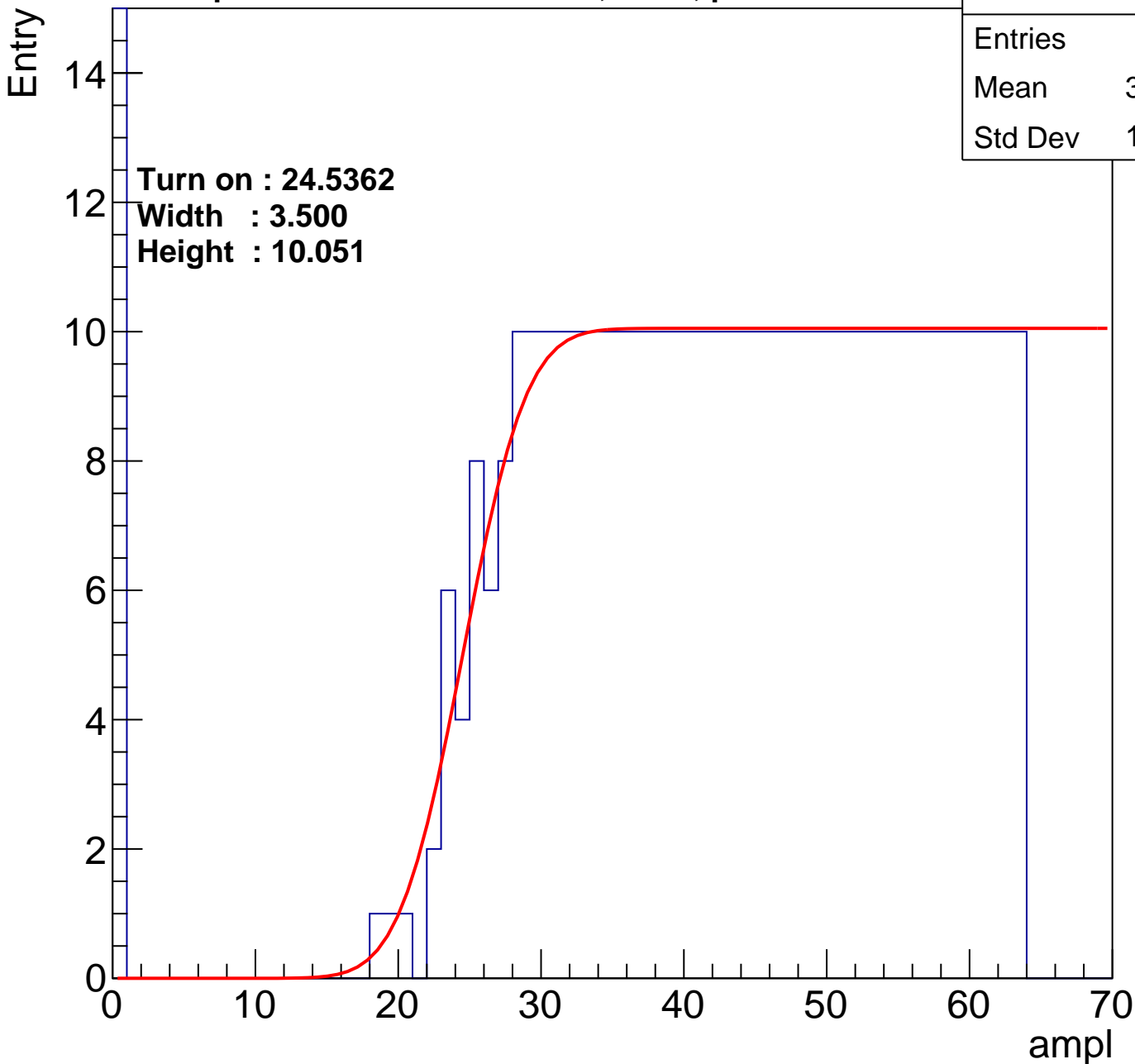
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	451
Mean	38.33
Std Dev	17.87

Turn on : 24.5362

Width : 3.500

Height : 10.051



# B1L103S, U20-ch65

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	414
Mean	39.75
Std Dev	17.8

Turn on : 27.5529

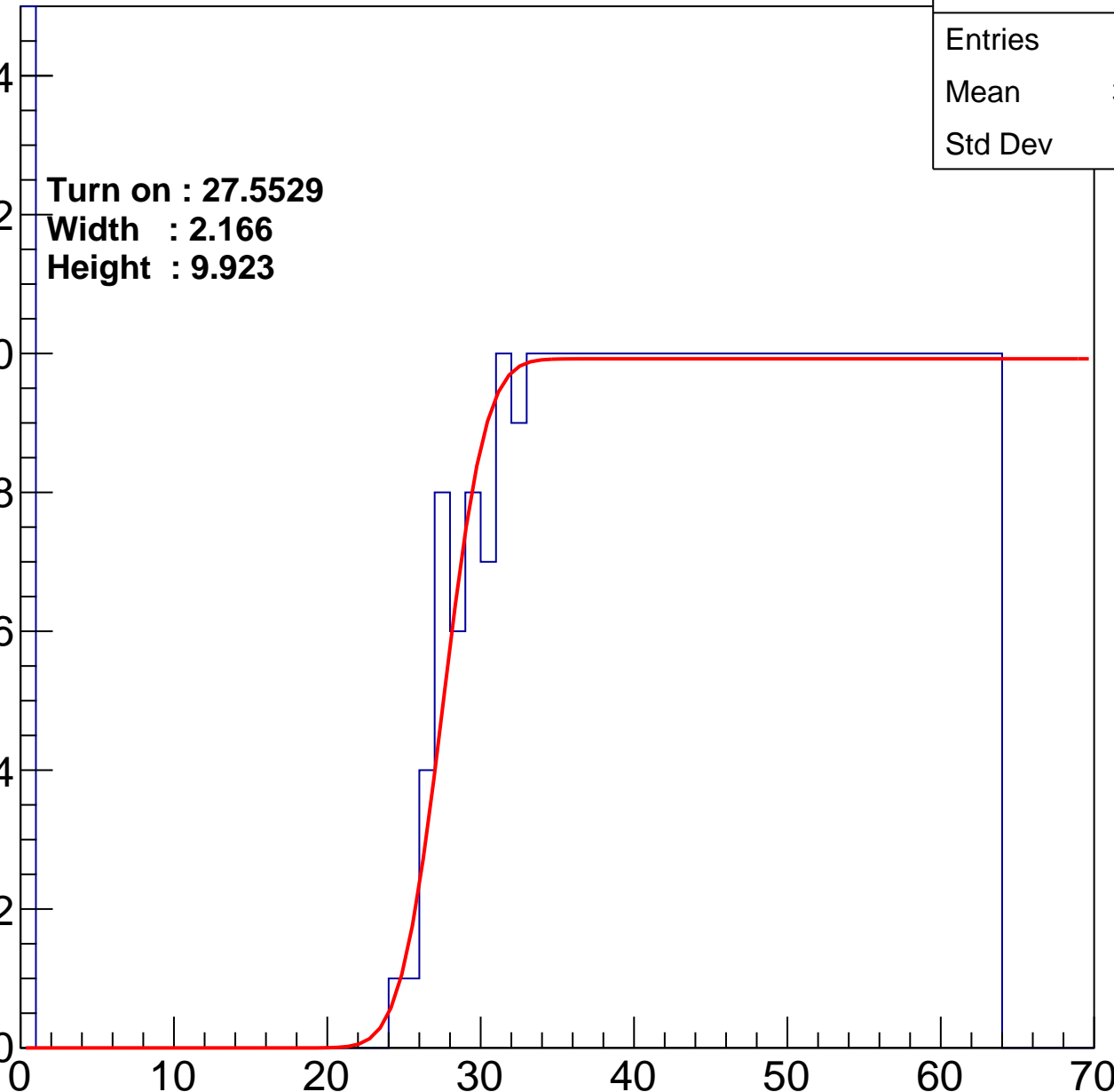
Width : 2.166

Height : 9.923

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch66

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	451
Mean	38.41
Std Dev	17.72

Turn on : 23.2301

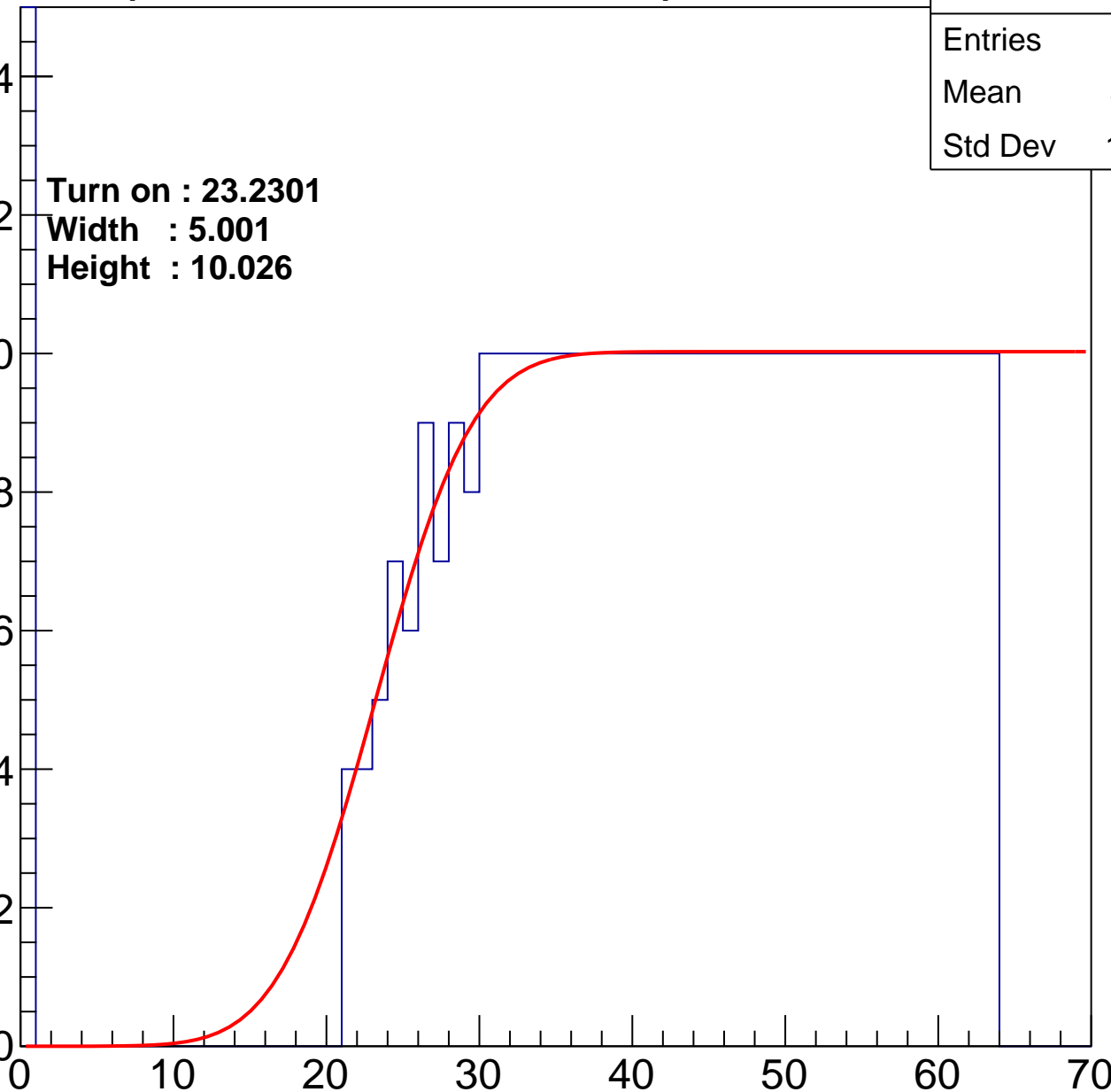
Width : 5.001

Height : 10.026

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch67

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	441
Mean	38.65
Std Dev	17.93

Turn on : 25.9066

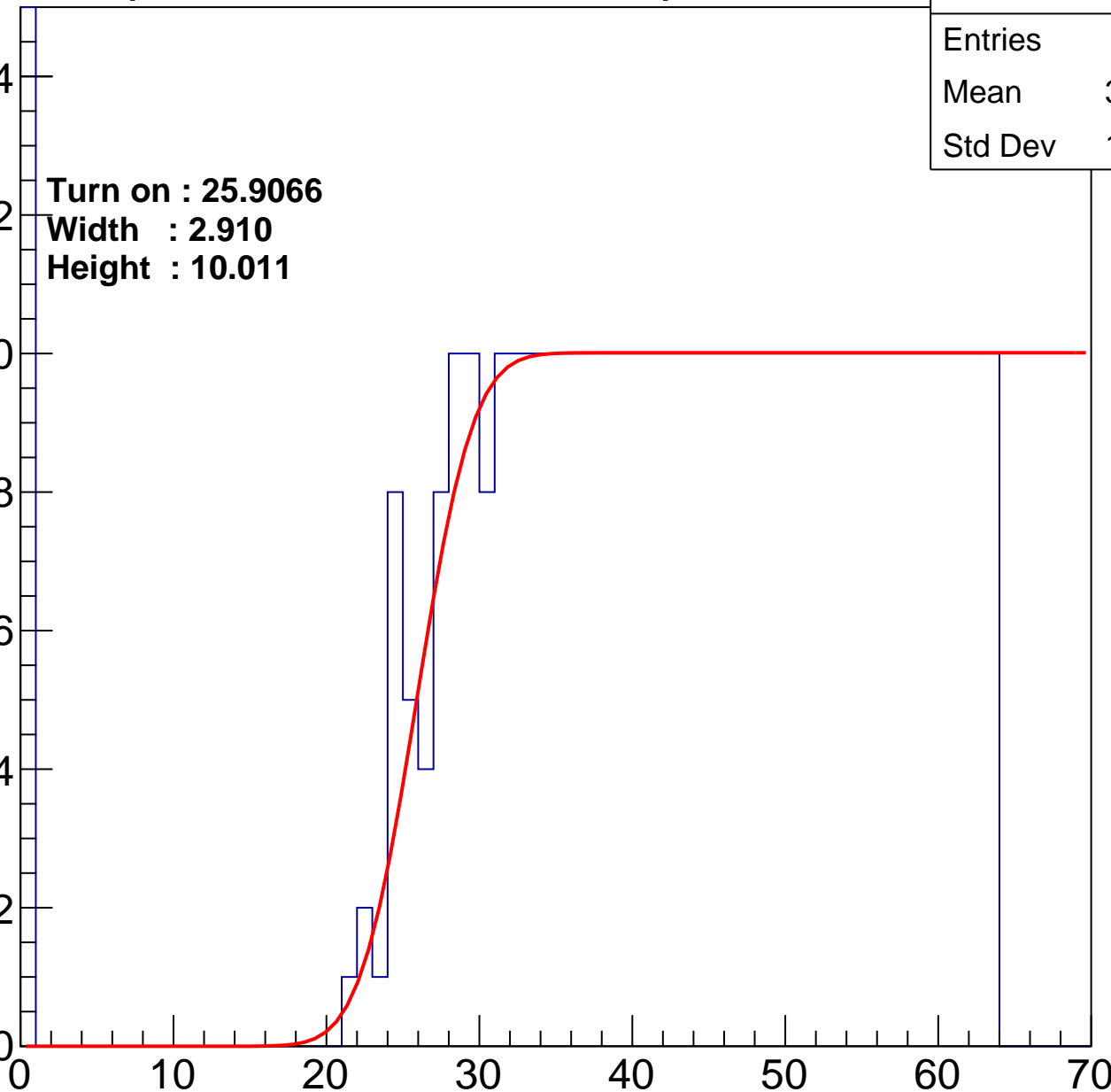
Width : 2.910

Height : 10.011

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch68

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	442
Mean	39.24
Std Dev	16.98

Turn on : 24.6011

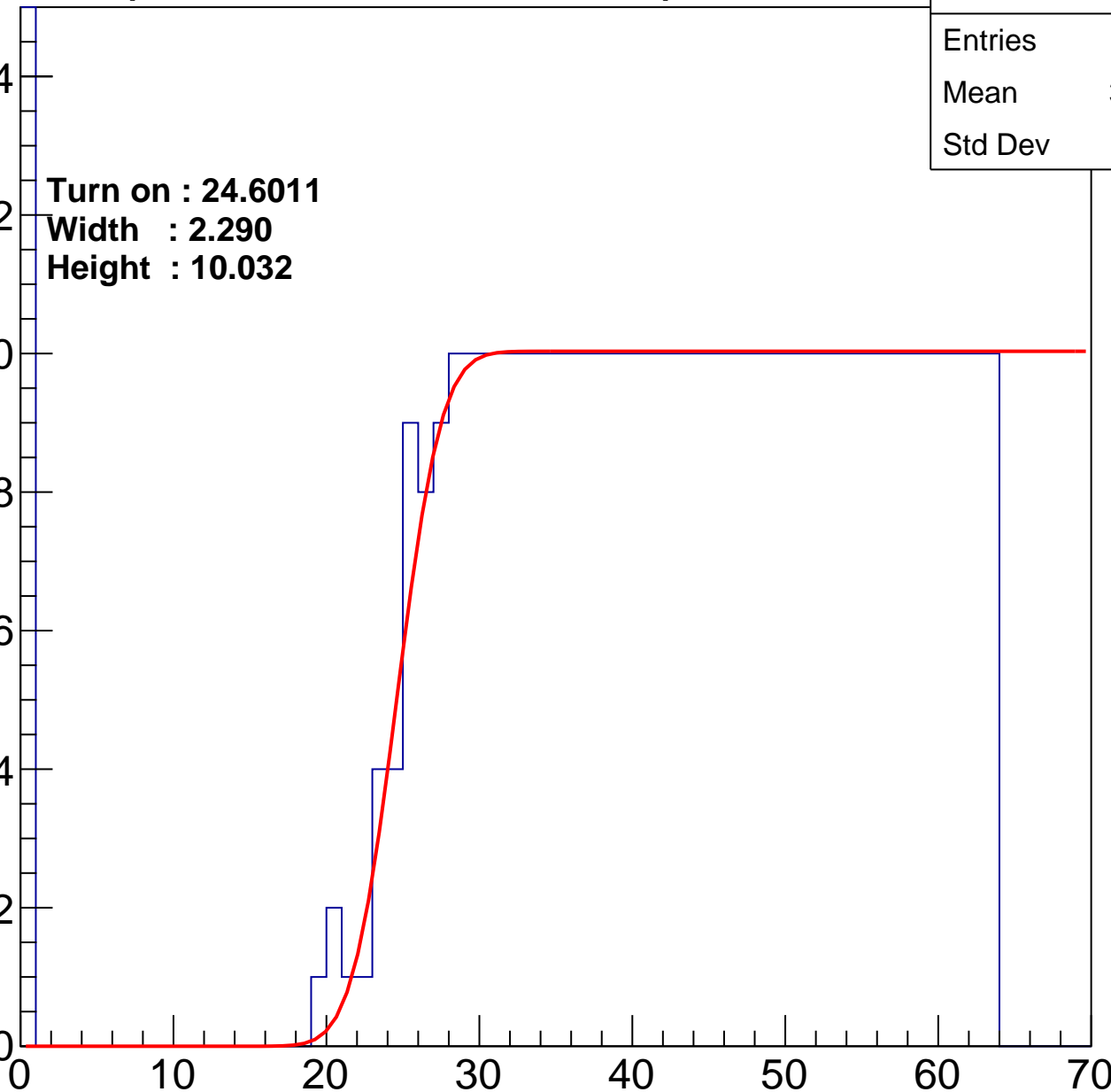
Width : 2.290

Height : 10.032

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch69

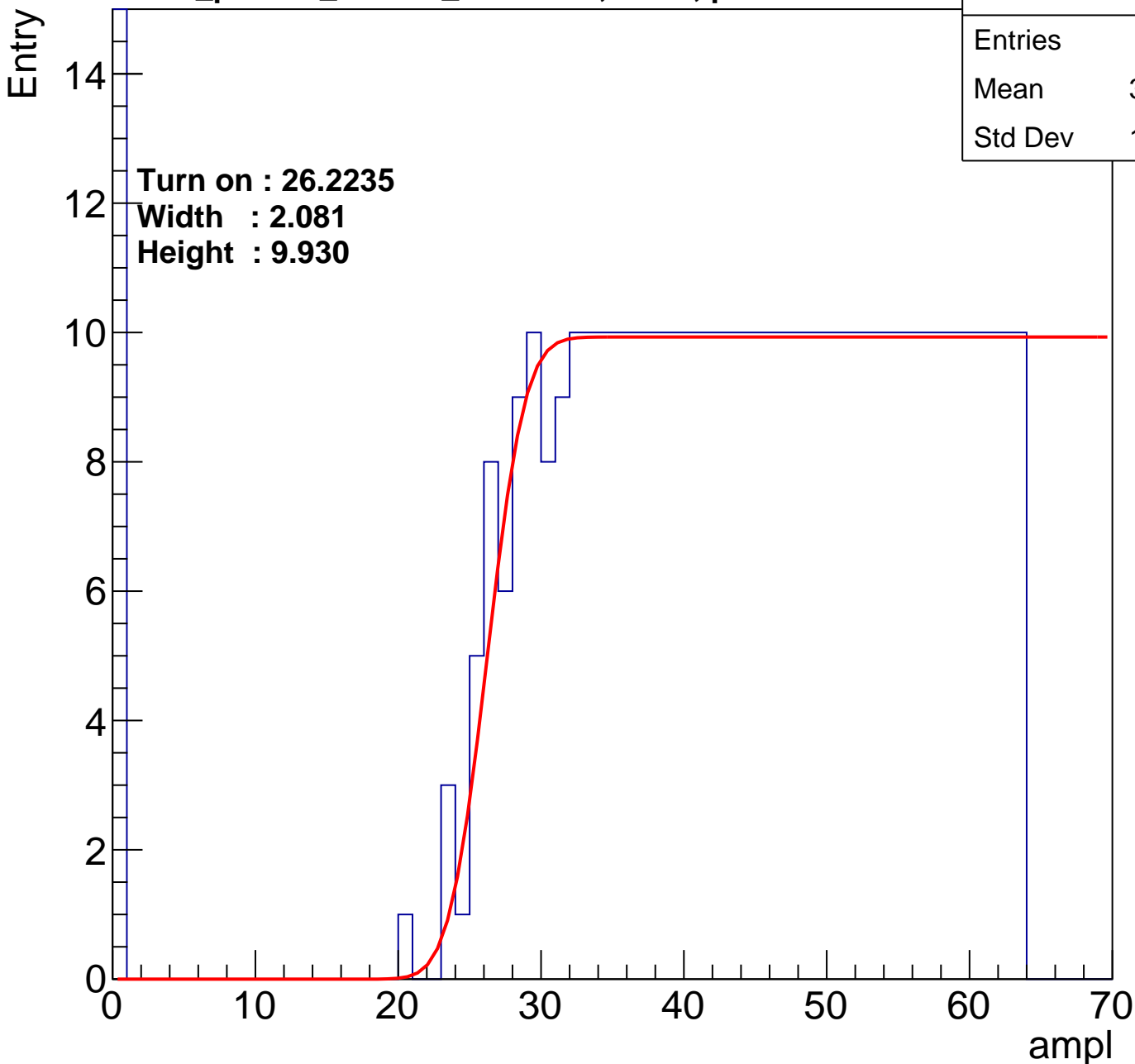
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	423
Mean	39.88
Std Dev	17.08

Turn on : 26.2235

Width : 2.081

Height : 9.930



# B1L103S, U20-ch70

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	426
Mean	39.62
Std Dev	17.33

Turn on : 26.3292

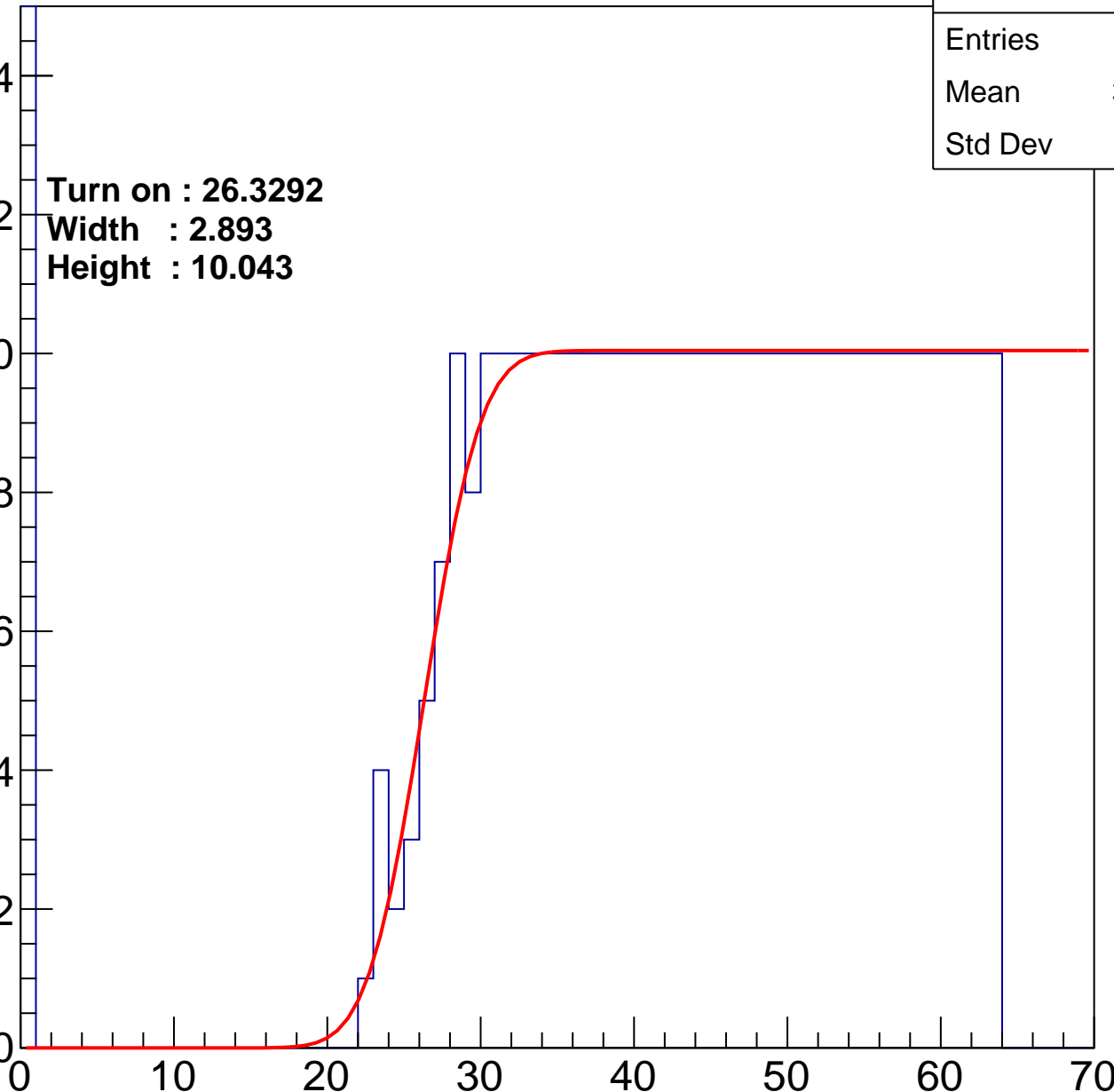
Width : 2.893

Height : 10.043

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U20-ch71

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	447
Mean	37.59
Std Dev	19.06

Turn on : 26.6020

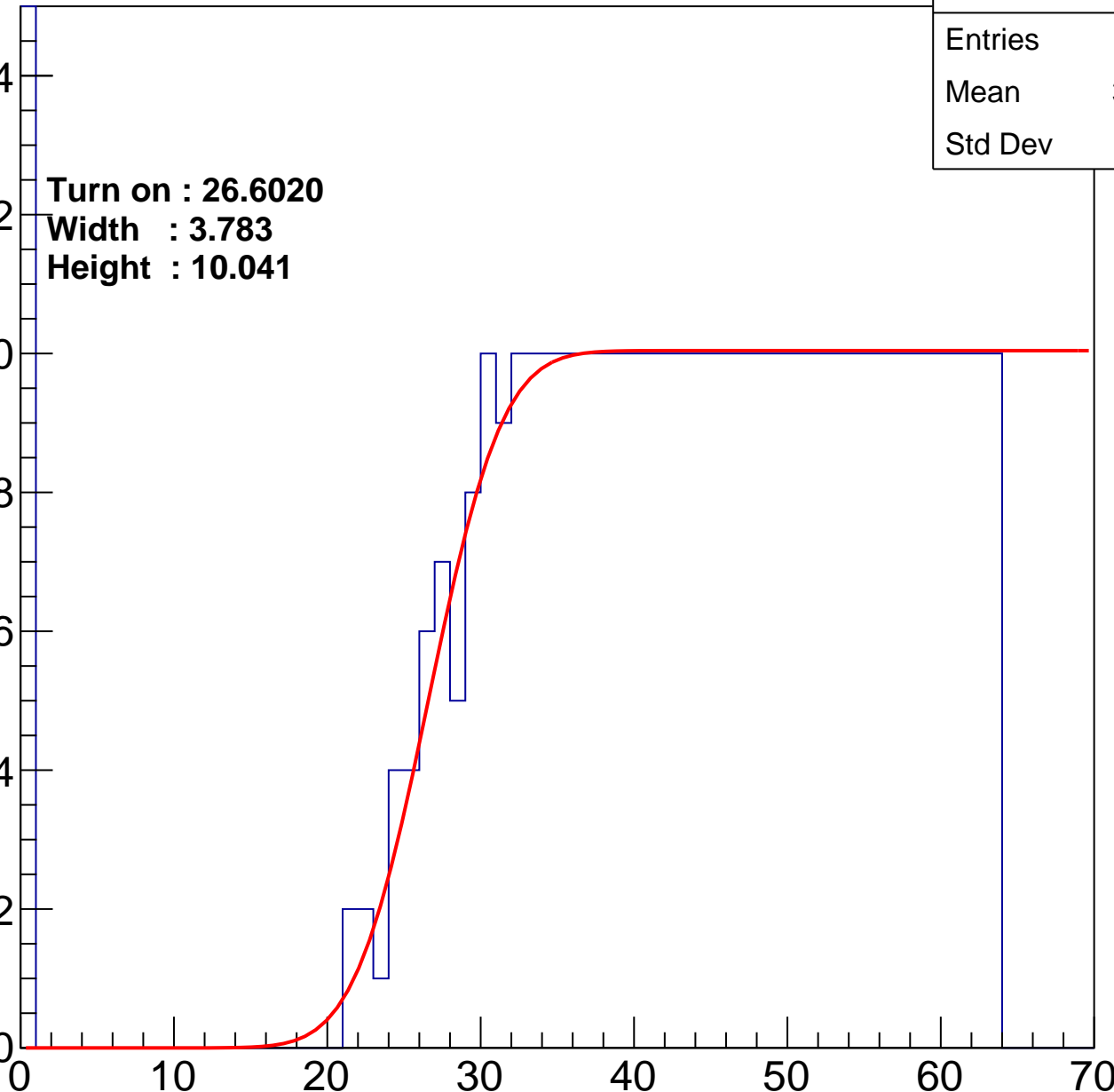
Width : 3.783

Height : 10.041

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch72

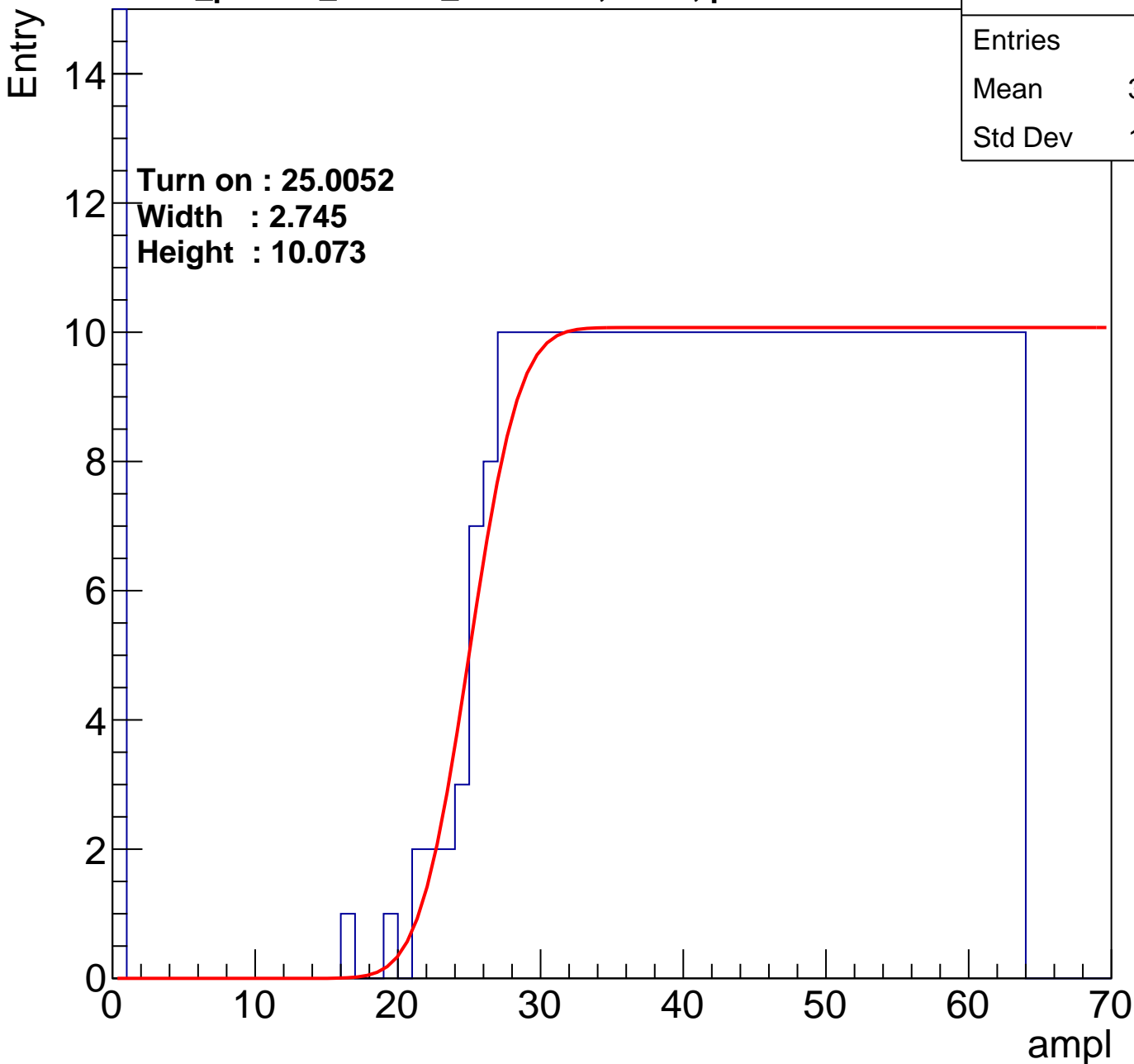
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	438
Mean	39.43
Std Dev	16.92

Turn on : 25.0052

Width : 2.745

Height : 10.073



# B1L103S, U20-ch73

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	403
Mean	40.78
Std Dev	16.82

Turn on : 28.0164

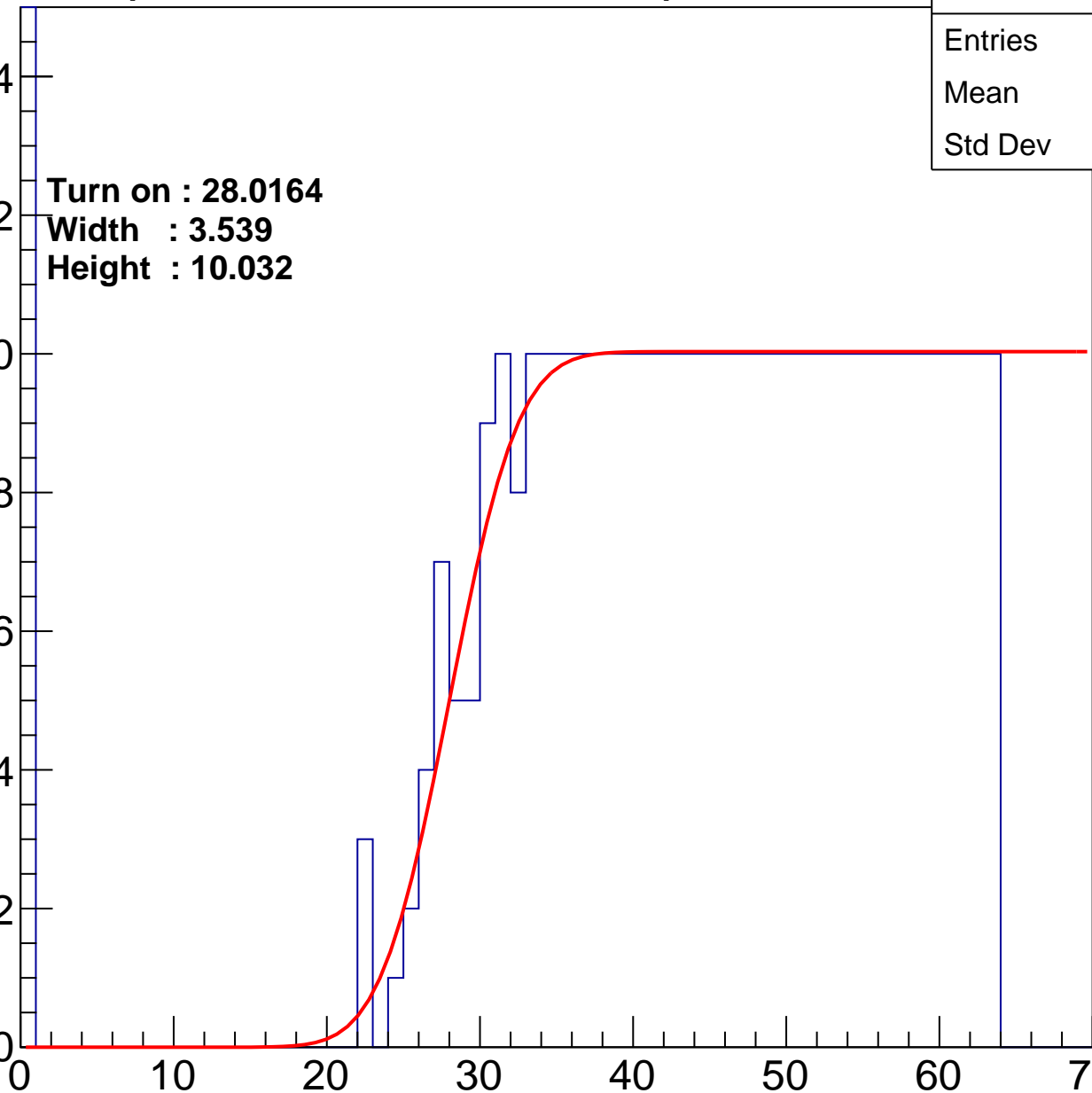
Width : 3.539

Height : 10.032

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch74

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	421
Mean	40.08
Std Dev	16.89

Turn on : 26.1349

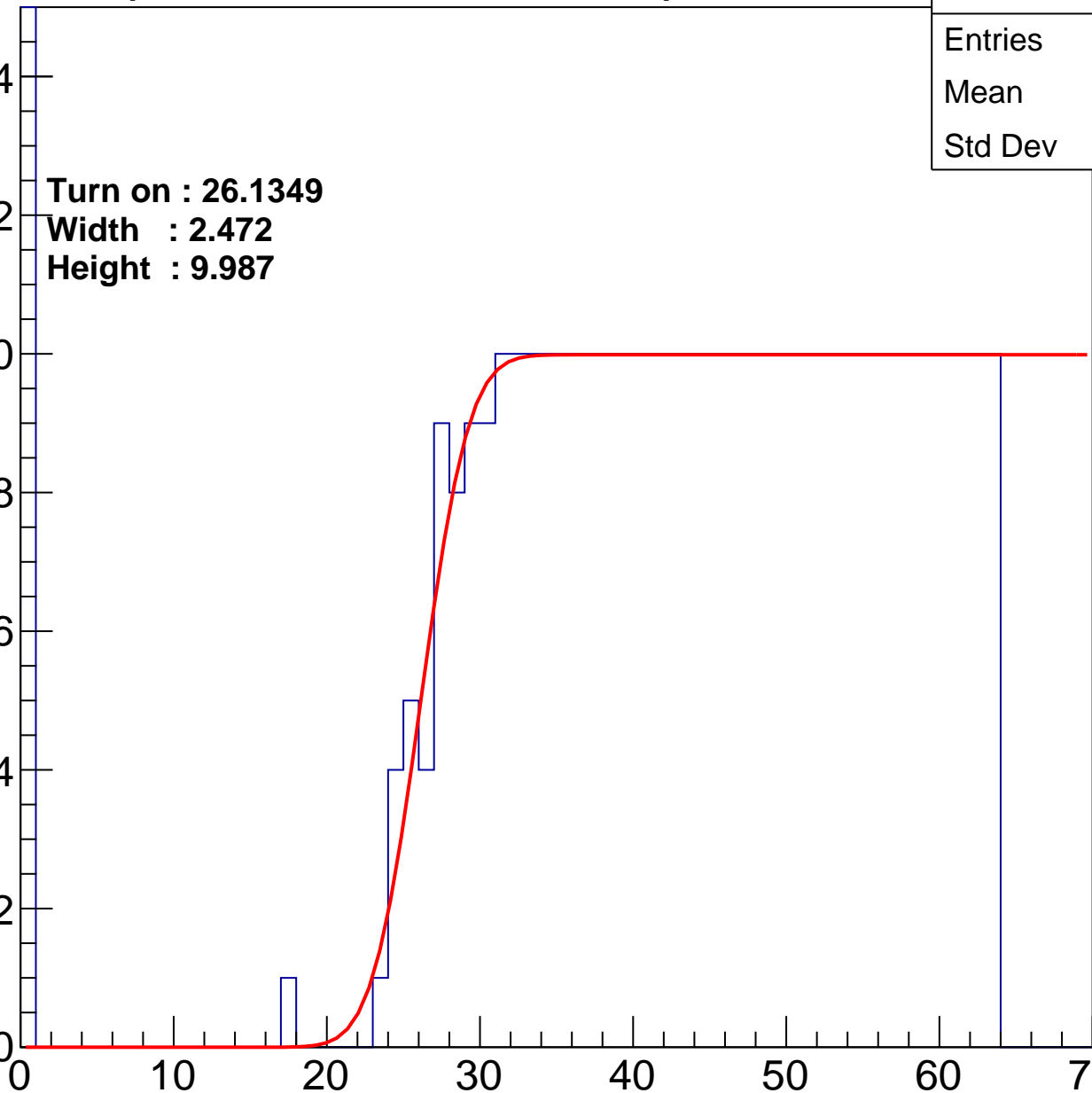
Width : 2.472

Height : 9.987

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch75

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	426
Mean	39.35
Std Dev	17.71

**Turn on : 27.0563**

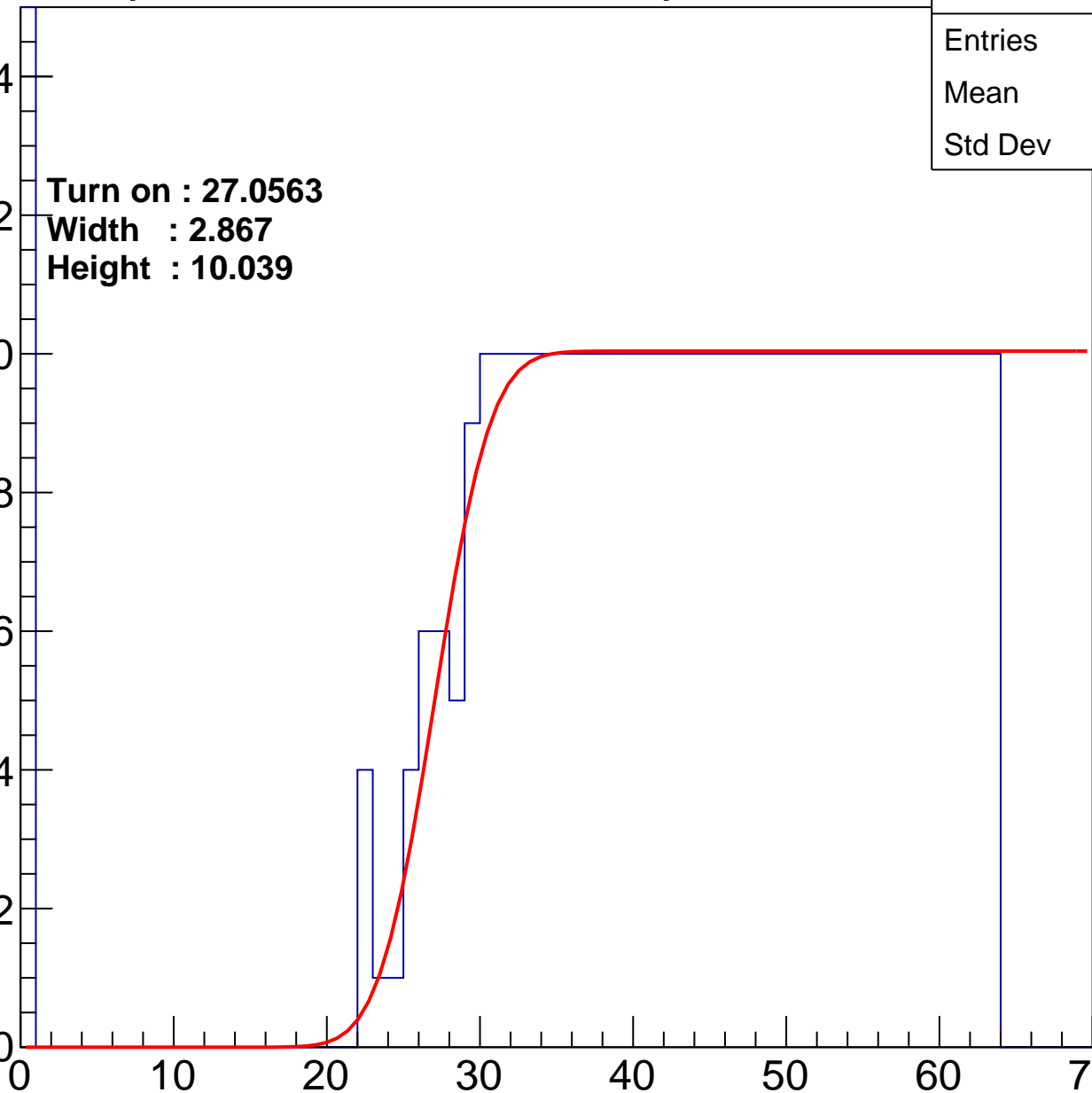
**Width : 2.867**

**Height : 10.039**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch76

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	459
Mean	38.24
Std Dev	17.55

Turn on : 23.4699

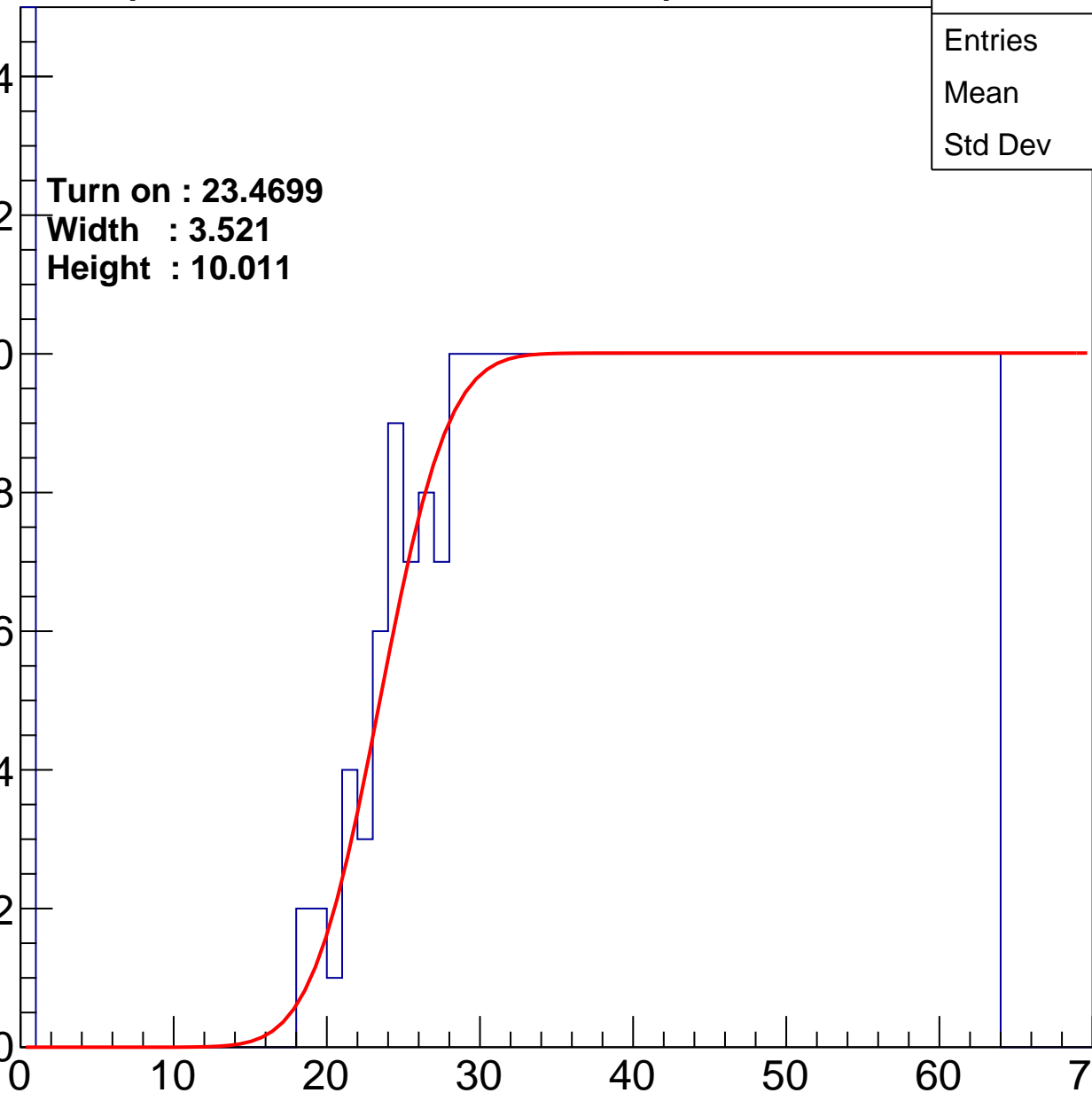
Width : 3.521

Height : 10.011

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch77

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	460
Mean	37.49
Std Dev	18.6

Turn on : 24.4991

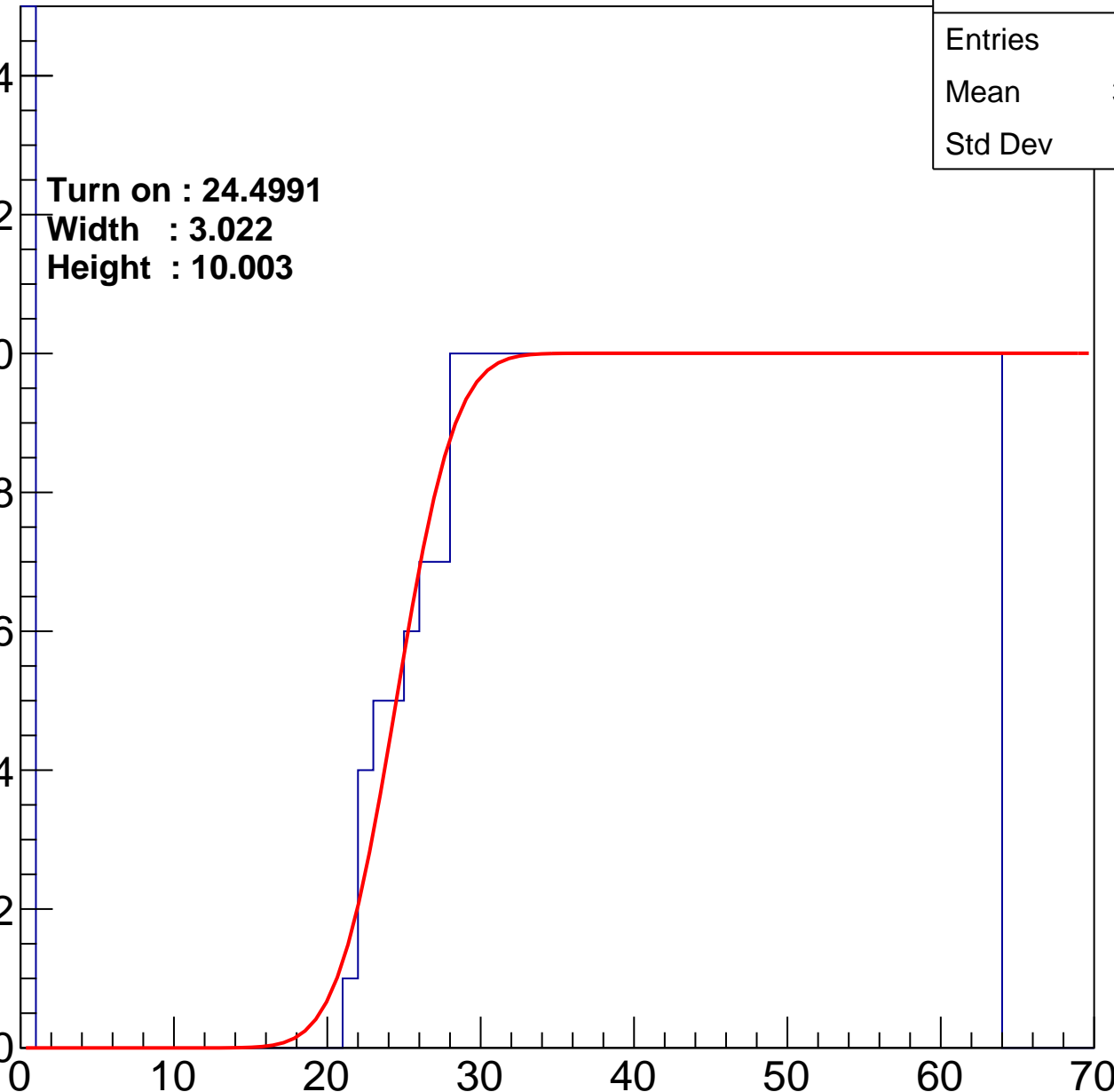
Width : 3.022

Height : 10.003

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch78

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	456
Mean	38.33
Std Dev	17.61

**Turn on : 24.2994**

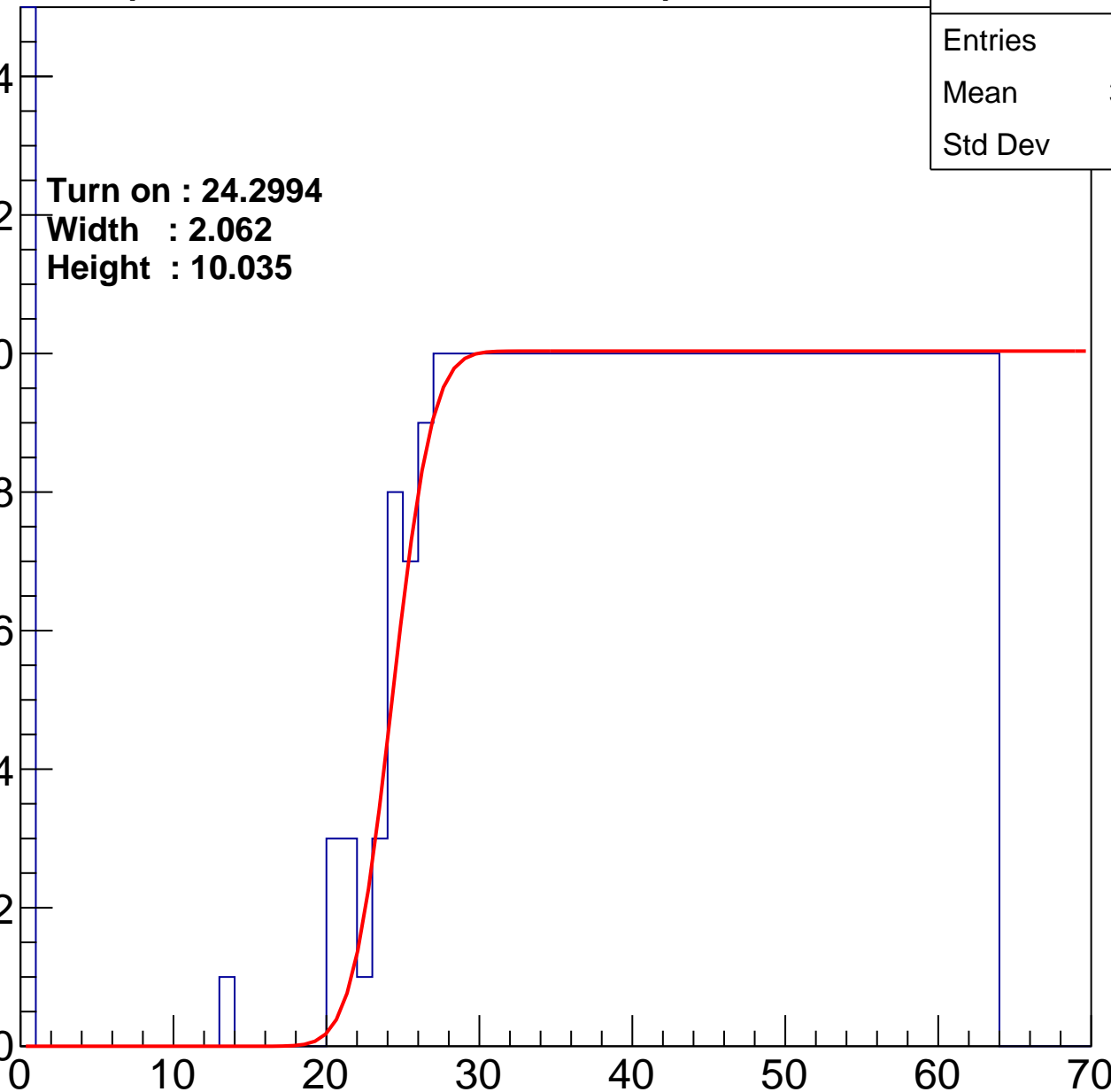
**Width : 2.062**

**Height : 10.035**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U20-ch79

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	425
Mean	39.83
Std Dev	17.06

Turn on : 25.6931

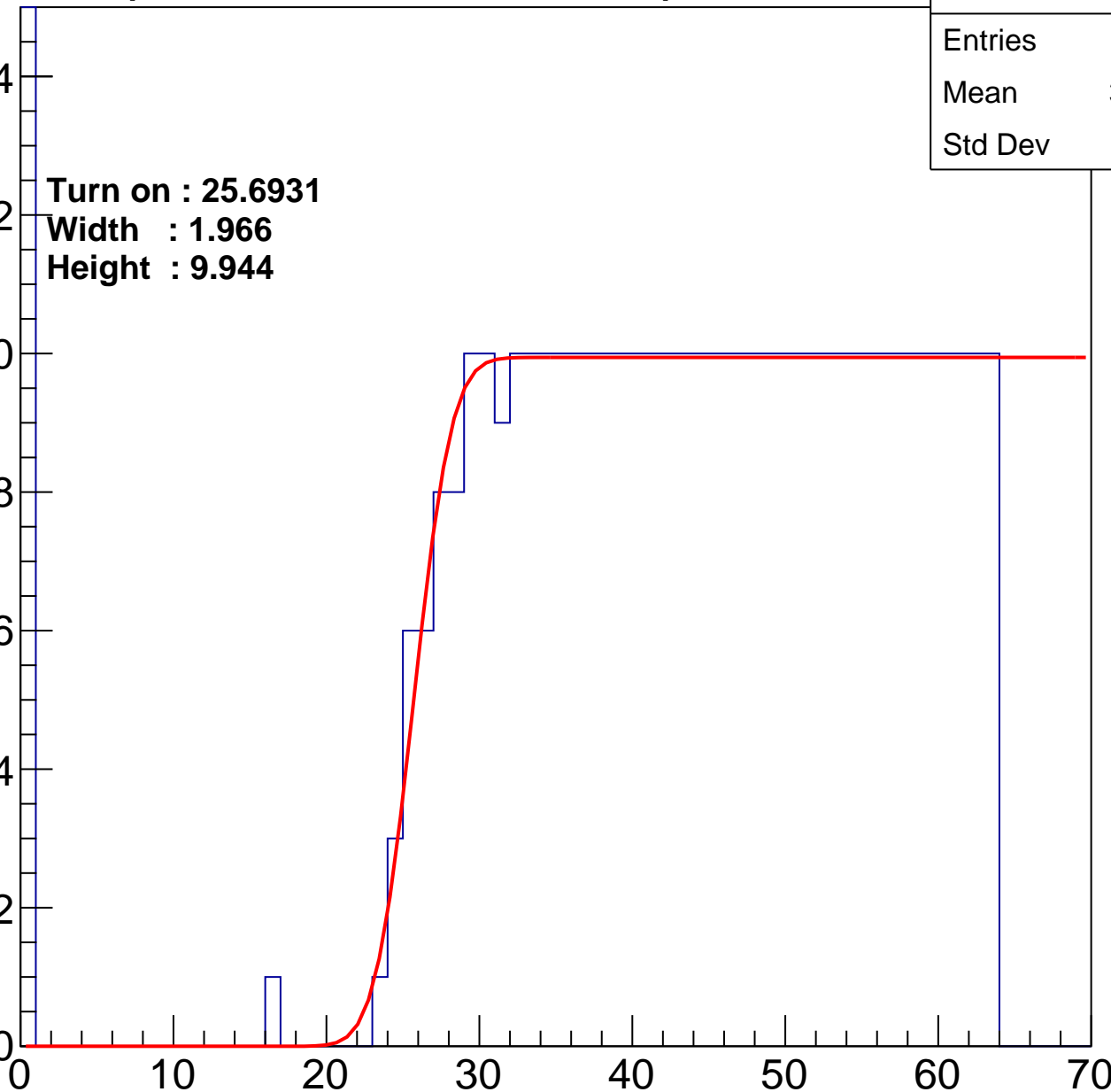
Width : 1.966

Height : 9.944

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch80

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	472
Mean	37.94
Std Dev	17.29

**Turn on : 21.9376**

**Width : 3.206**

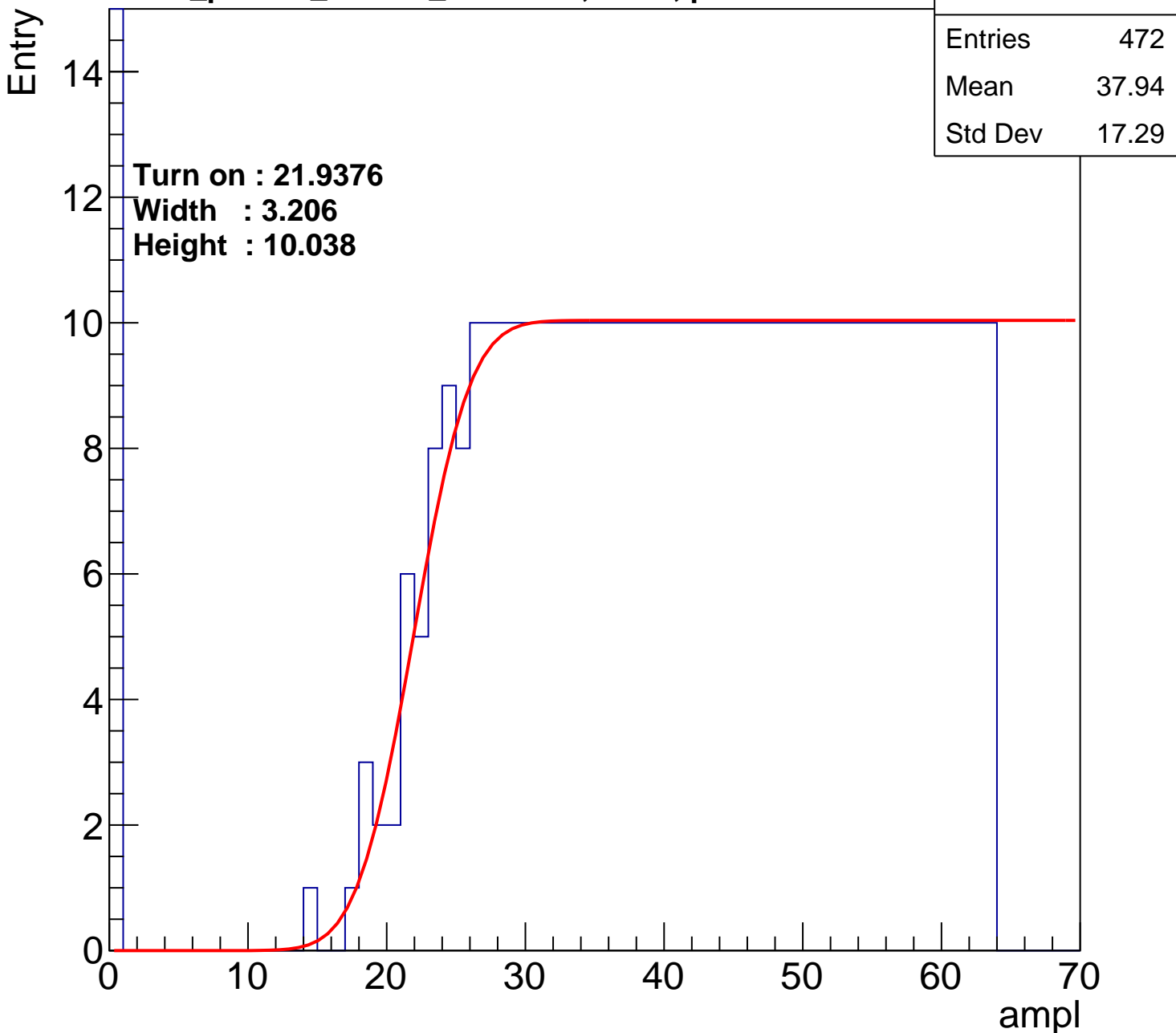
**Height : 10.038**

Entry

14  
12  
10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U20-ch81

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	436
Mean	38.42
Std Dev	18.49

**Turn on : 27.3787**

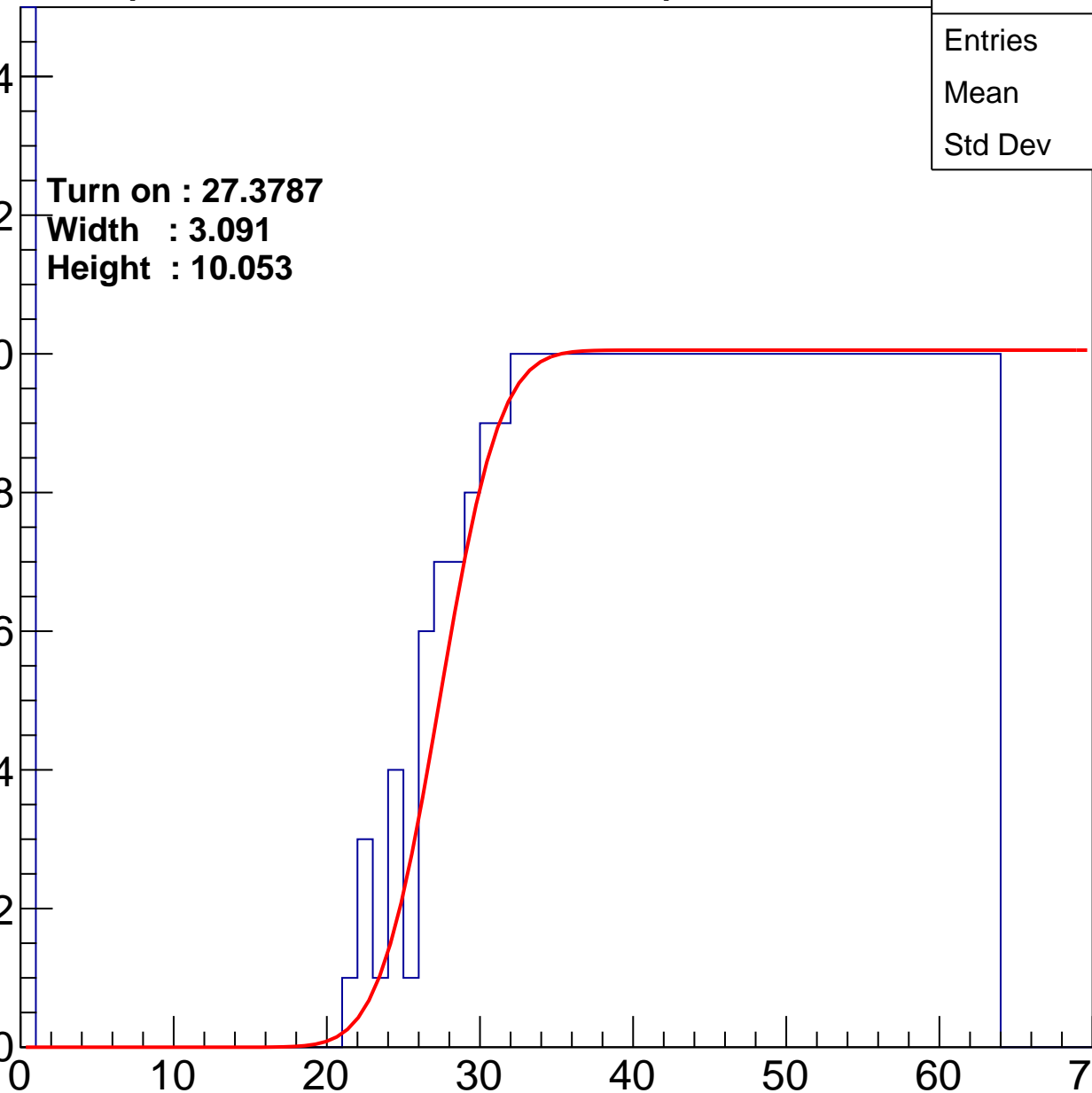
**Width : 3.091**

**Height : 10.053**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch82

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	484
Mean	35.62
Std Dev	19.73

Turn on : 25.5029

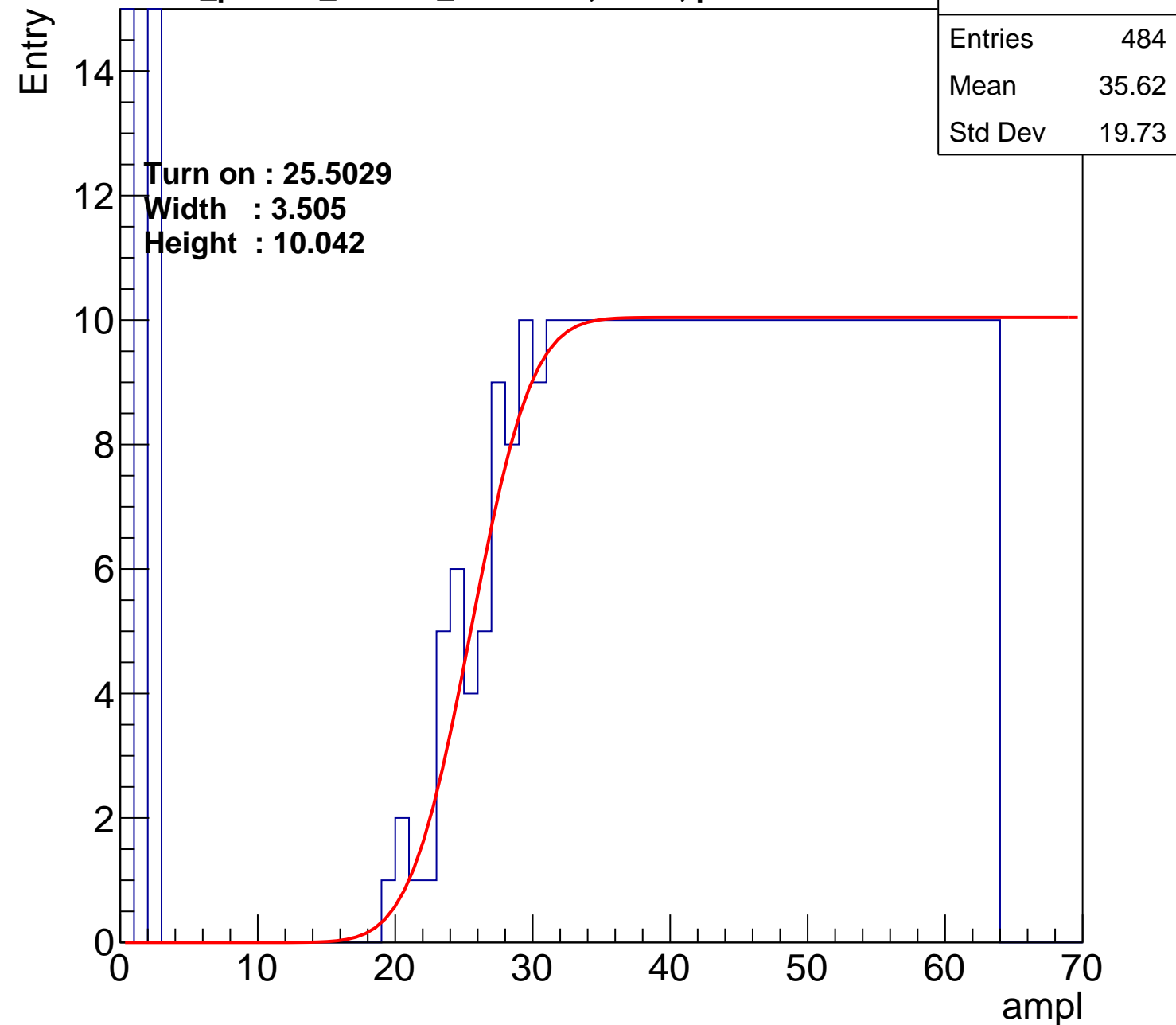
Width : 3.505

Height : 10.042

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch83

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	436
Mean	39.1
Std Dev	17.54

Turn on : 25.4231

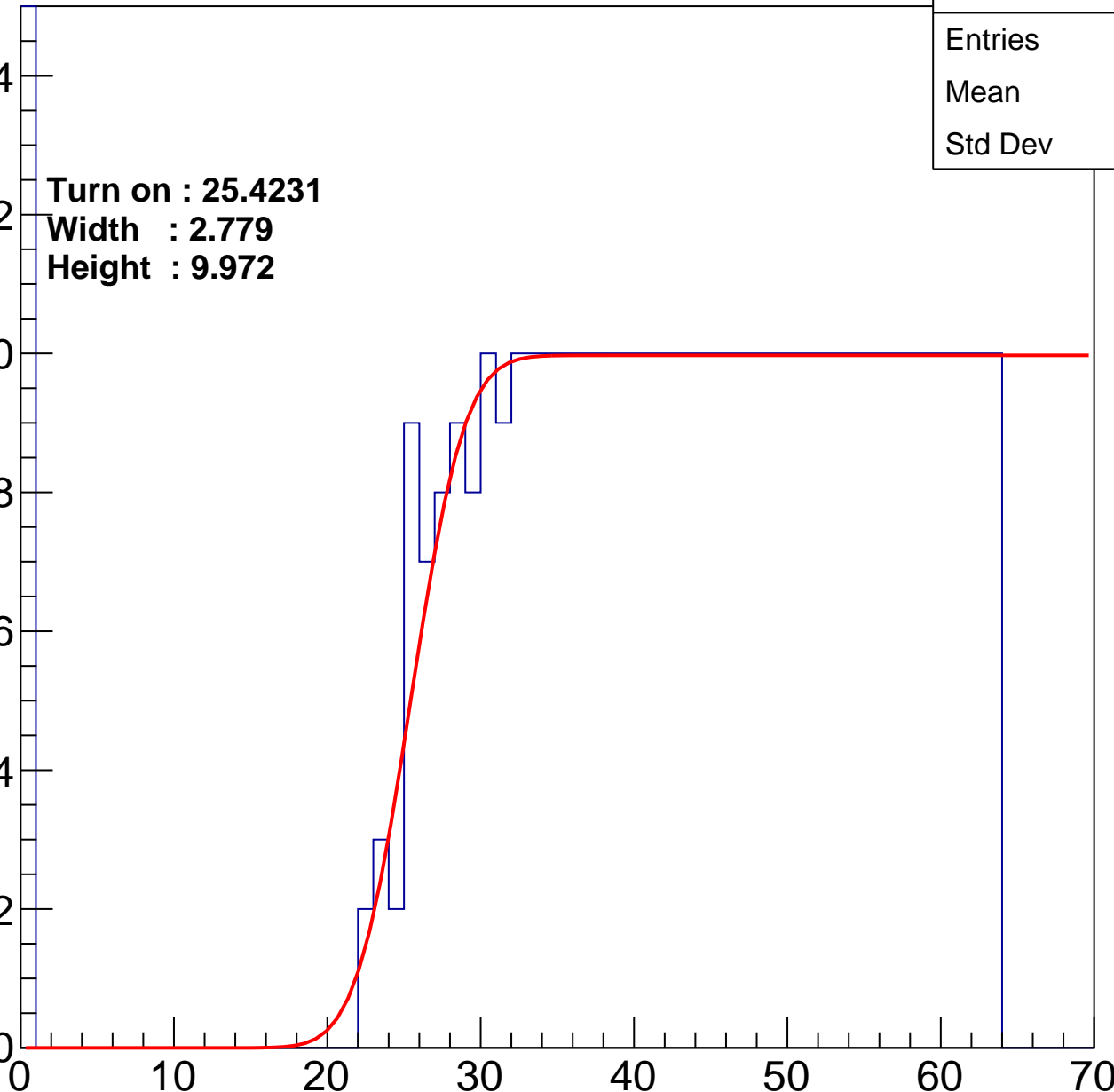
Width : 2.779

Height : 9.972

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch84

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	430
Mean	39.87
Std Dev	16.68

Turn on : 24.9188

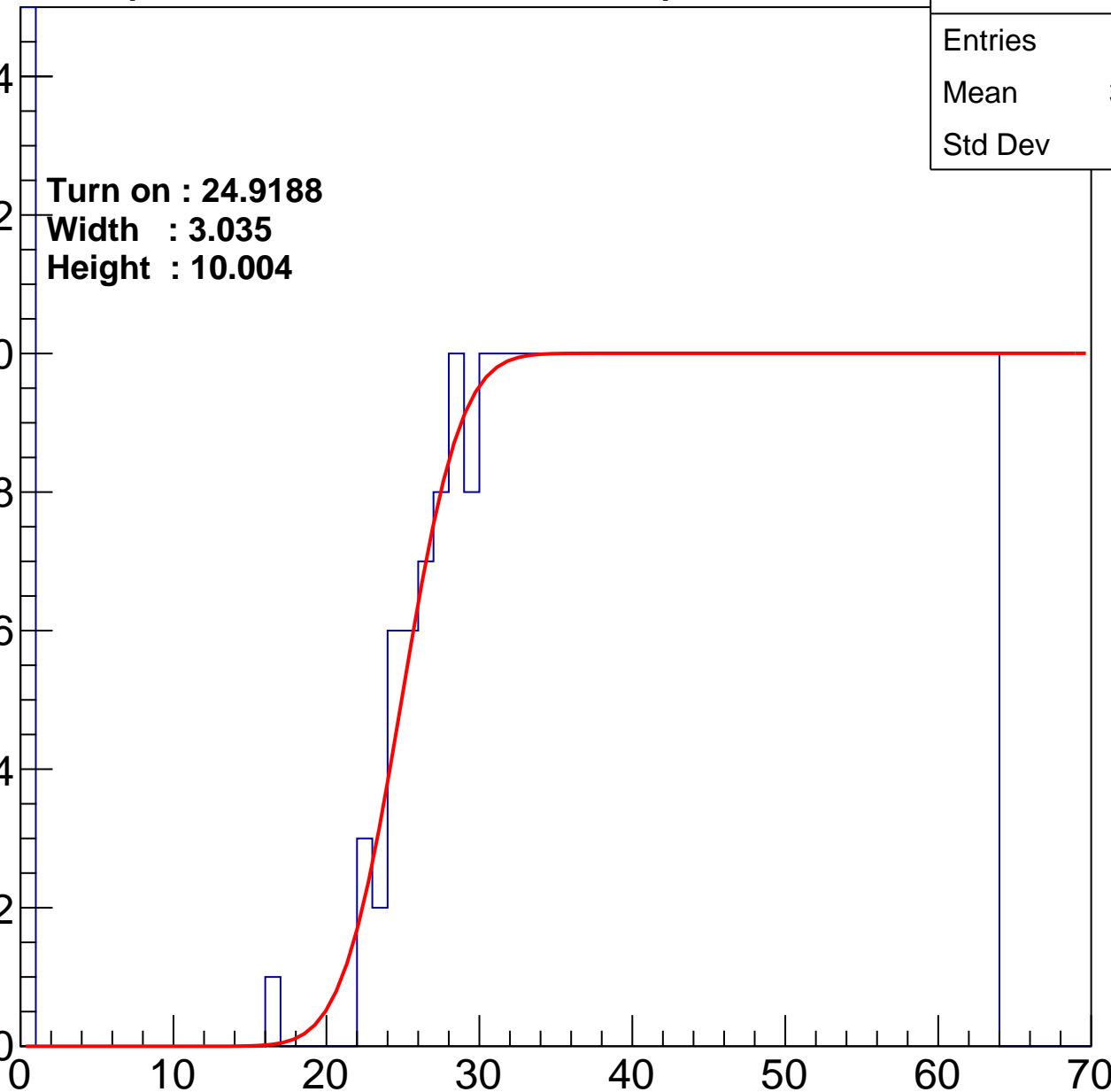
Width : 3.035

Height : 10.004

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch85

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	429
Mean	39.55
Std Dev	17.24

Turn on : 25.8736

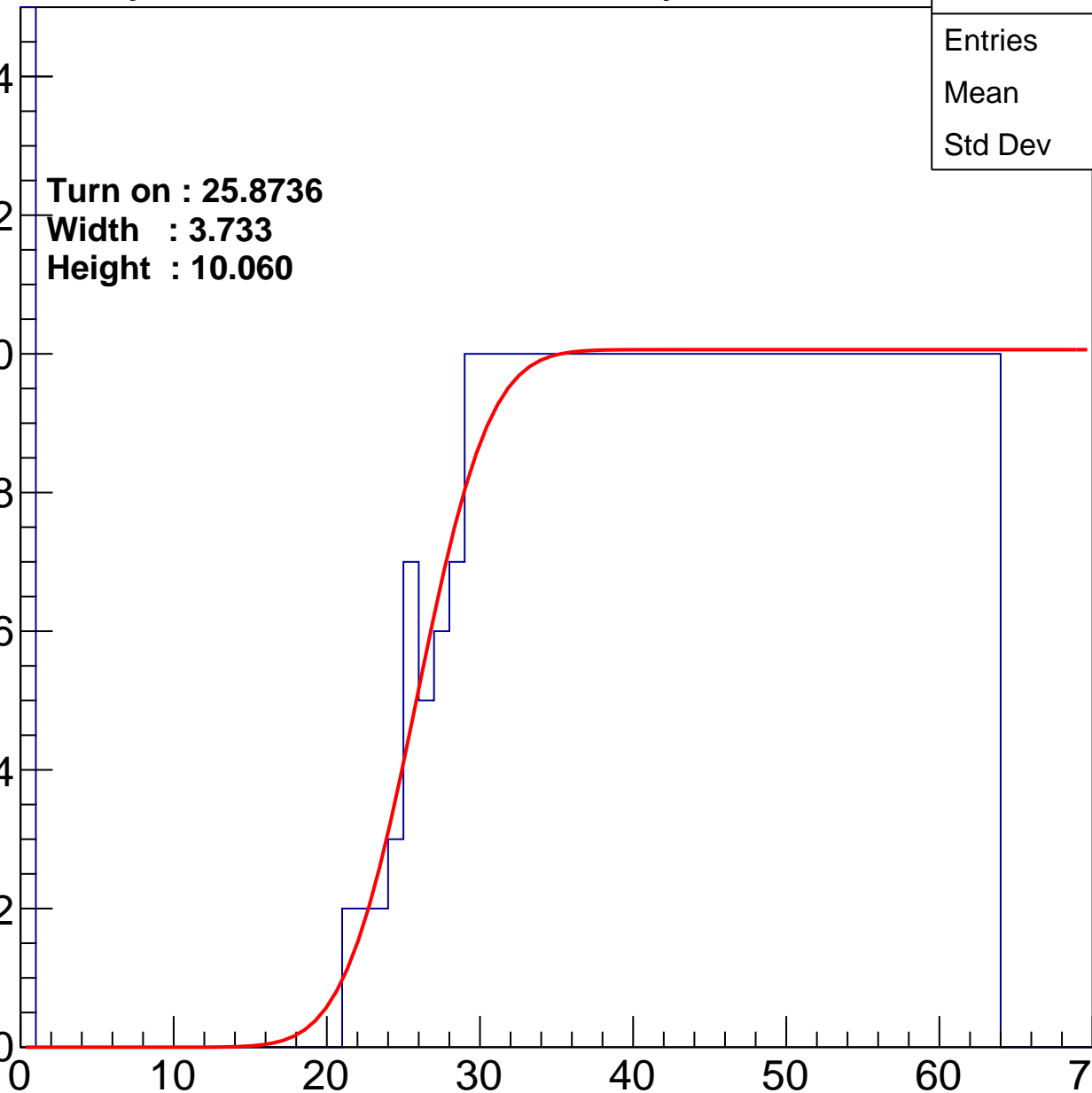
Width : 3.733

Height : 10.060

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch86

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	442
Mean	38.72
Std Dev	17.73

Turn on : 25.1048

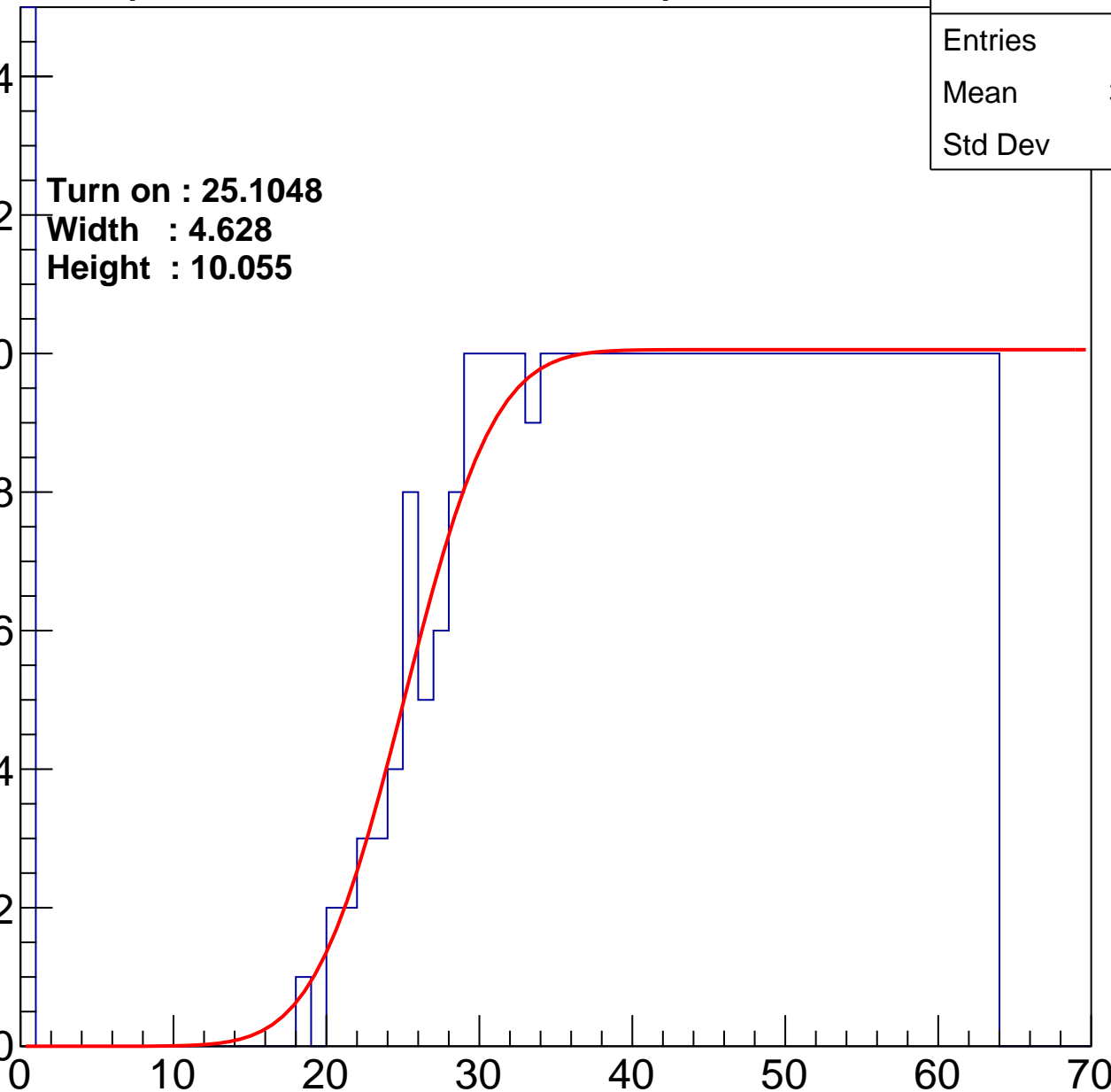
Width : 4.628

Height : 10.055

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U20-ch87

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	424
Mean	39.22
Std Dev	18.01

Turn on : 27.3308

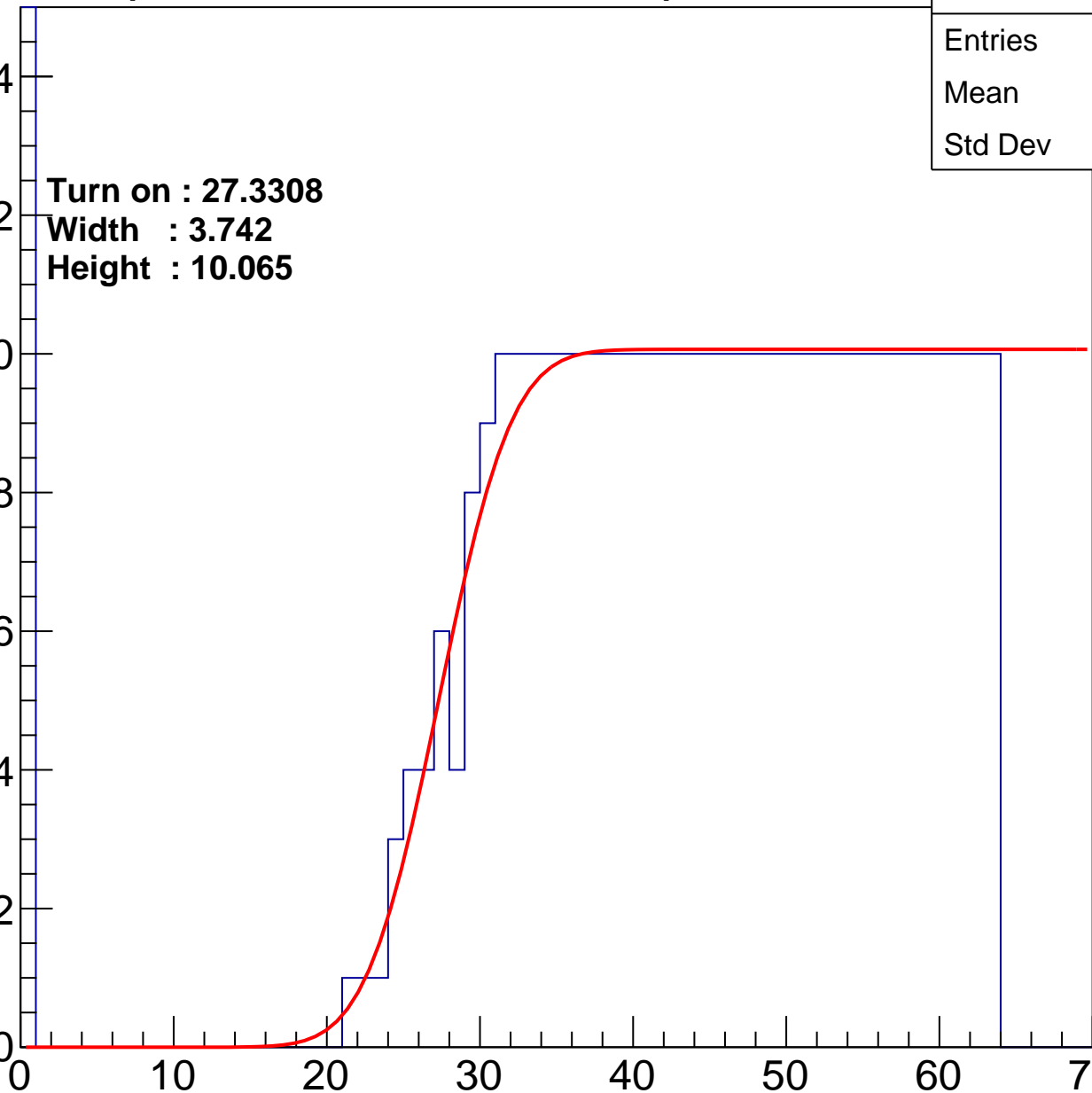
Width : 3.742

Height : 10.065

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch88

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	469
Mean	36.92
Std Dev	18.93

Turn on : 24.3856

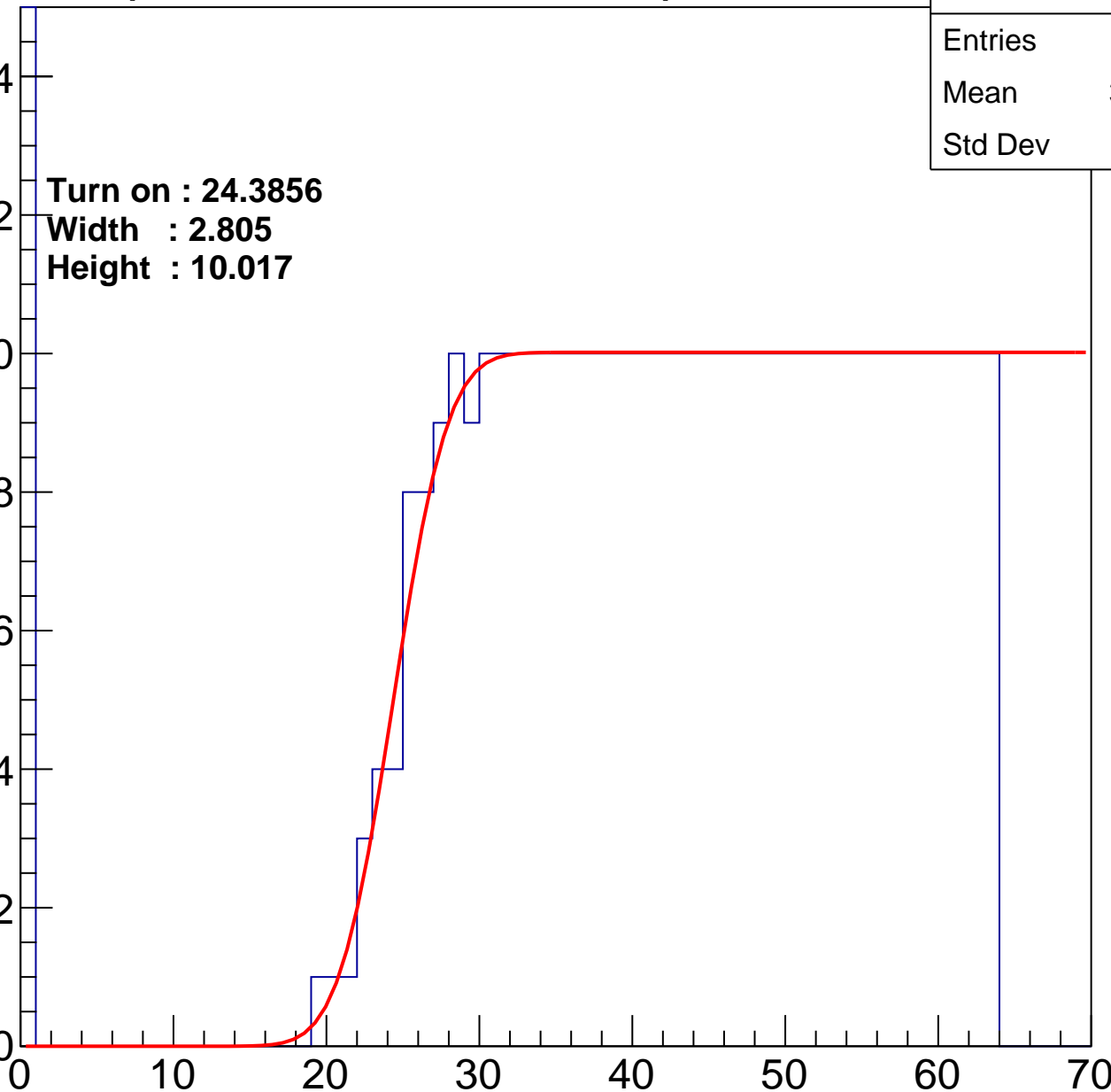
Width : 2.805

Height : 10.017

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch89

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	413
Mean	39.52
Std Dev	18.14

Turn on : 28.1719

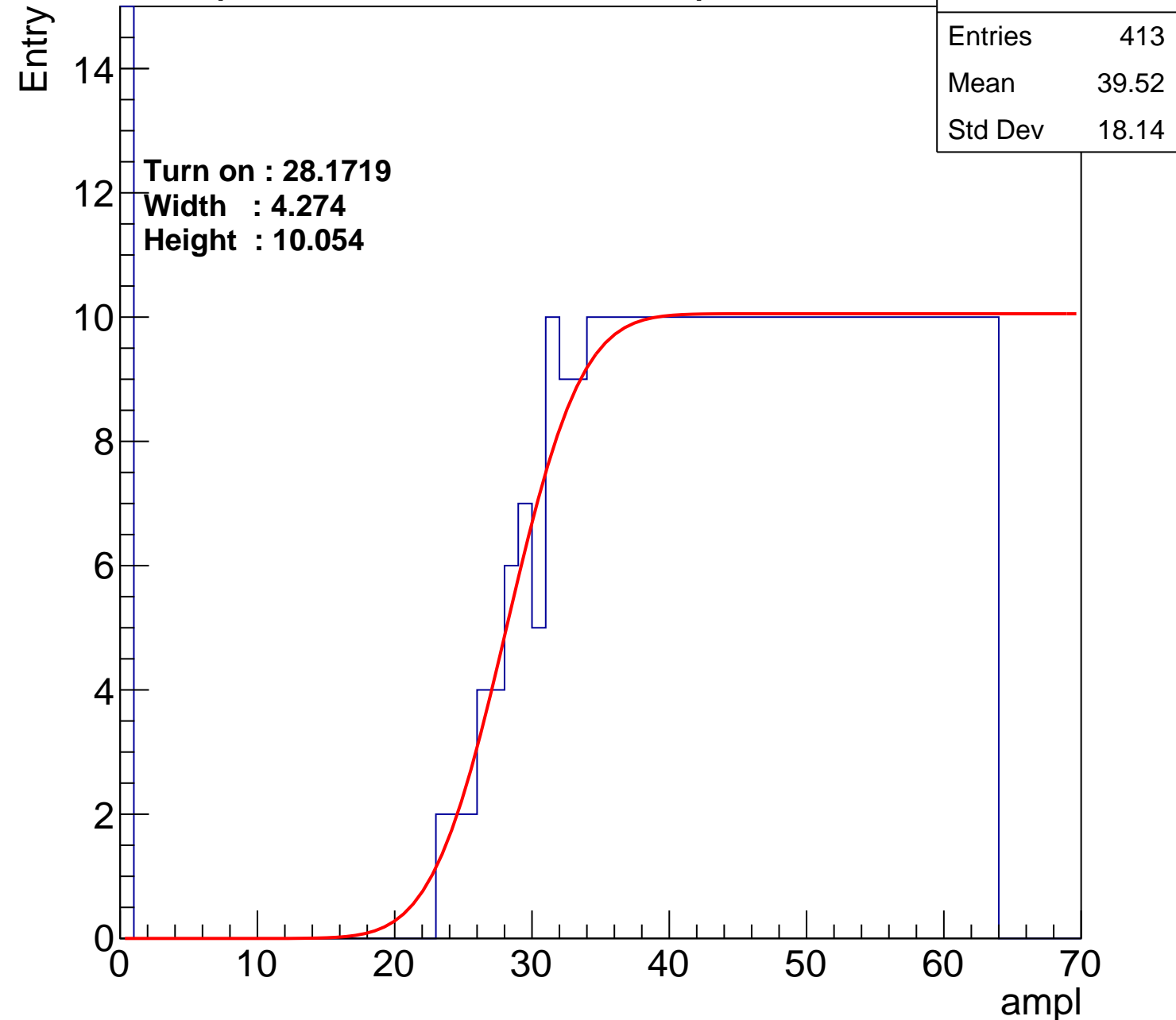
Width : 4.274

Height : 10.054

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch90

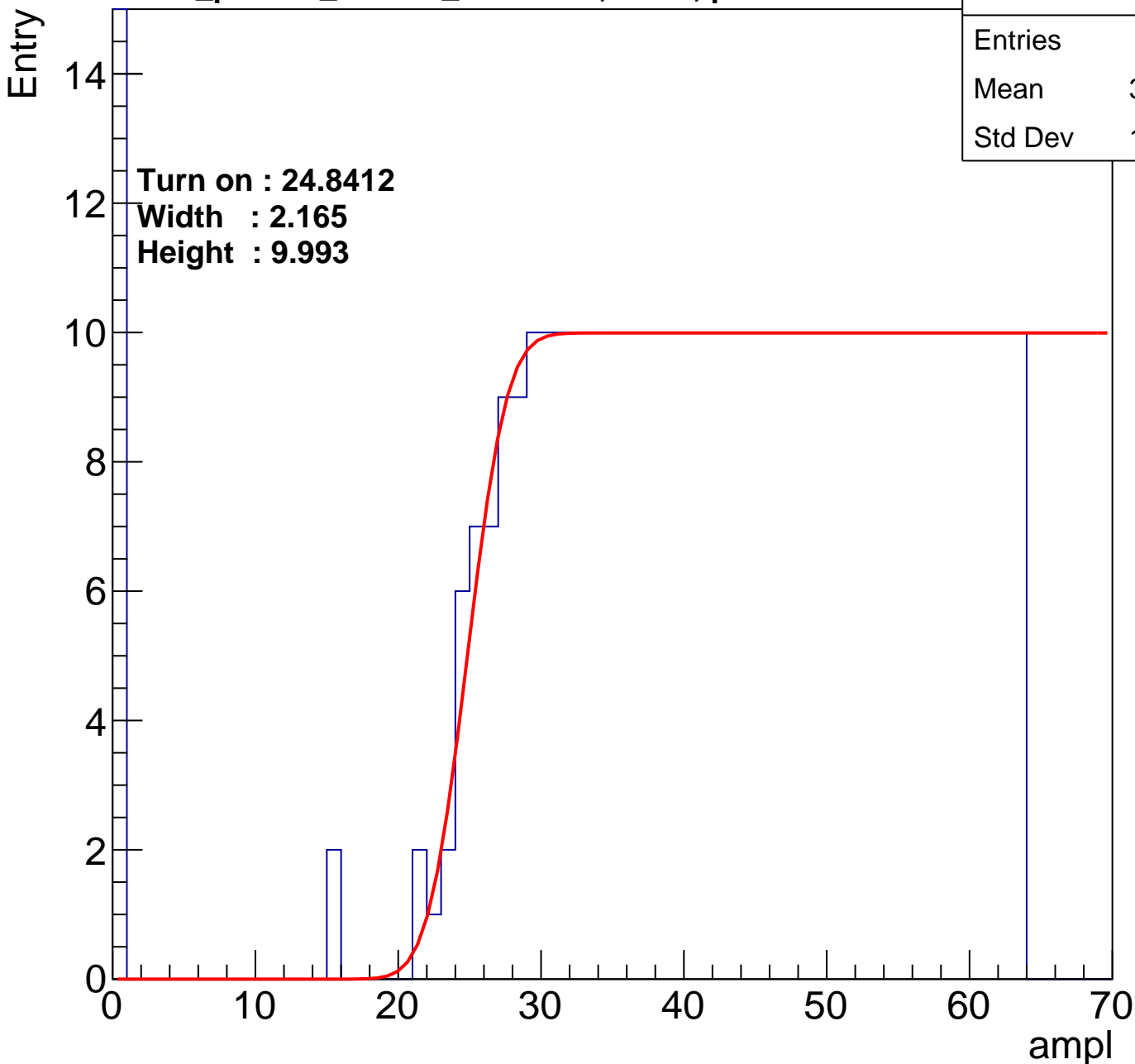
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	448
Mean	38.47
Std Dev	17.82

Turn on : 24.8412

Width : 2.165

Height : 9.993



# B1L103S, U20-ch91

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	417
Mean	40.44
Std Dev	16.53

**Turn on : 26.1786**

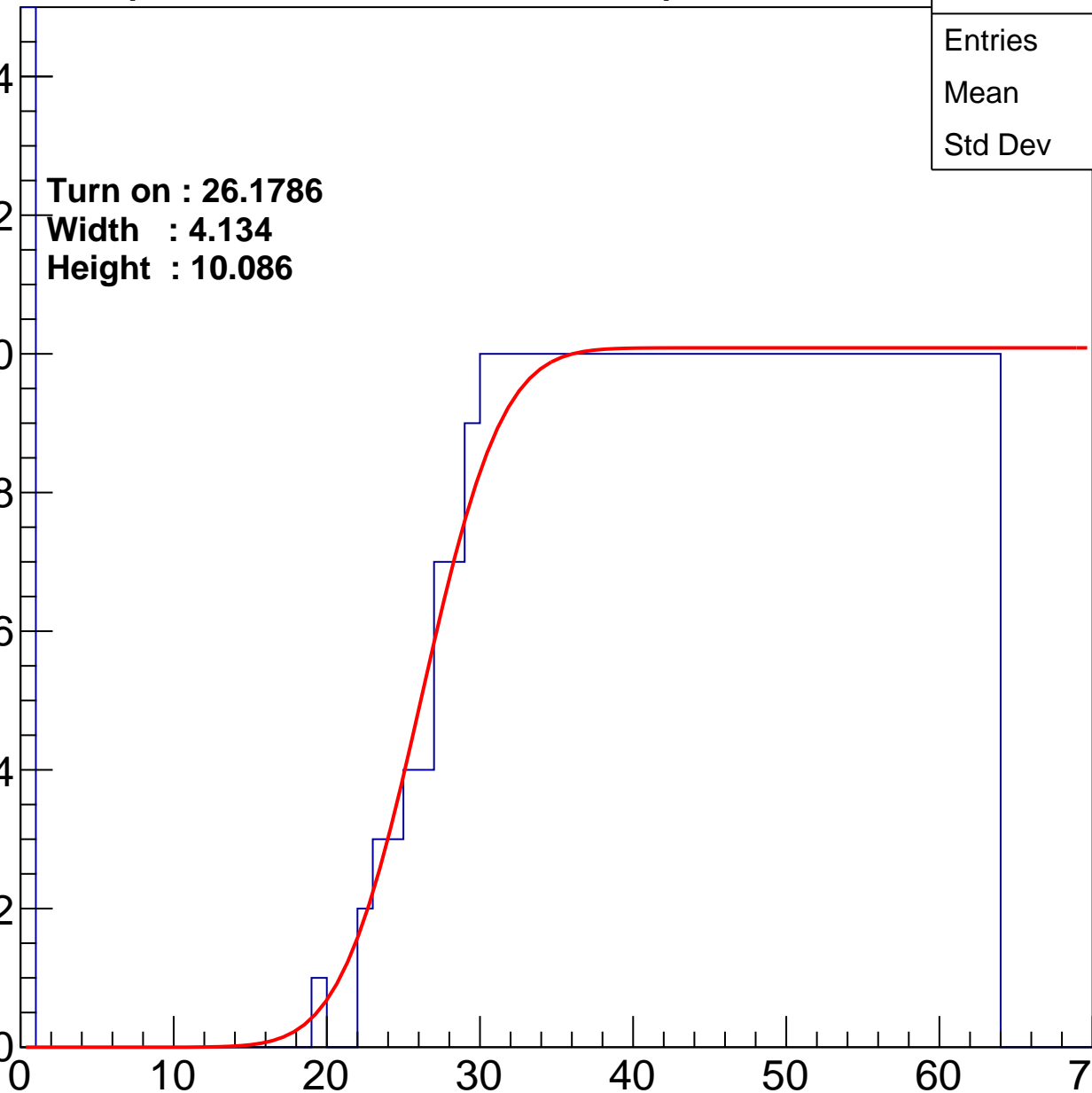
**Width : 4.134**

**Height : 10.086**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch92

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	437
Mean	39.23
Std Dev	17.28

Turn on : 24.8060

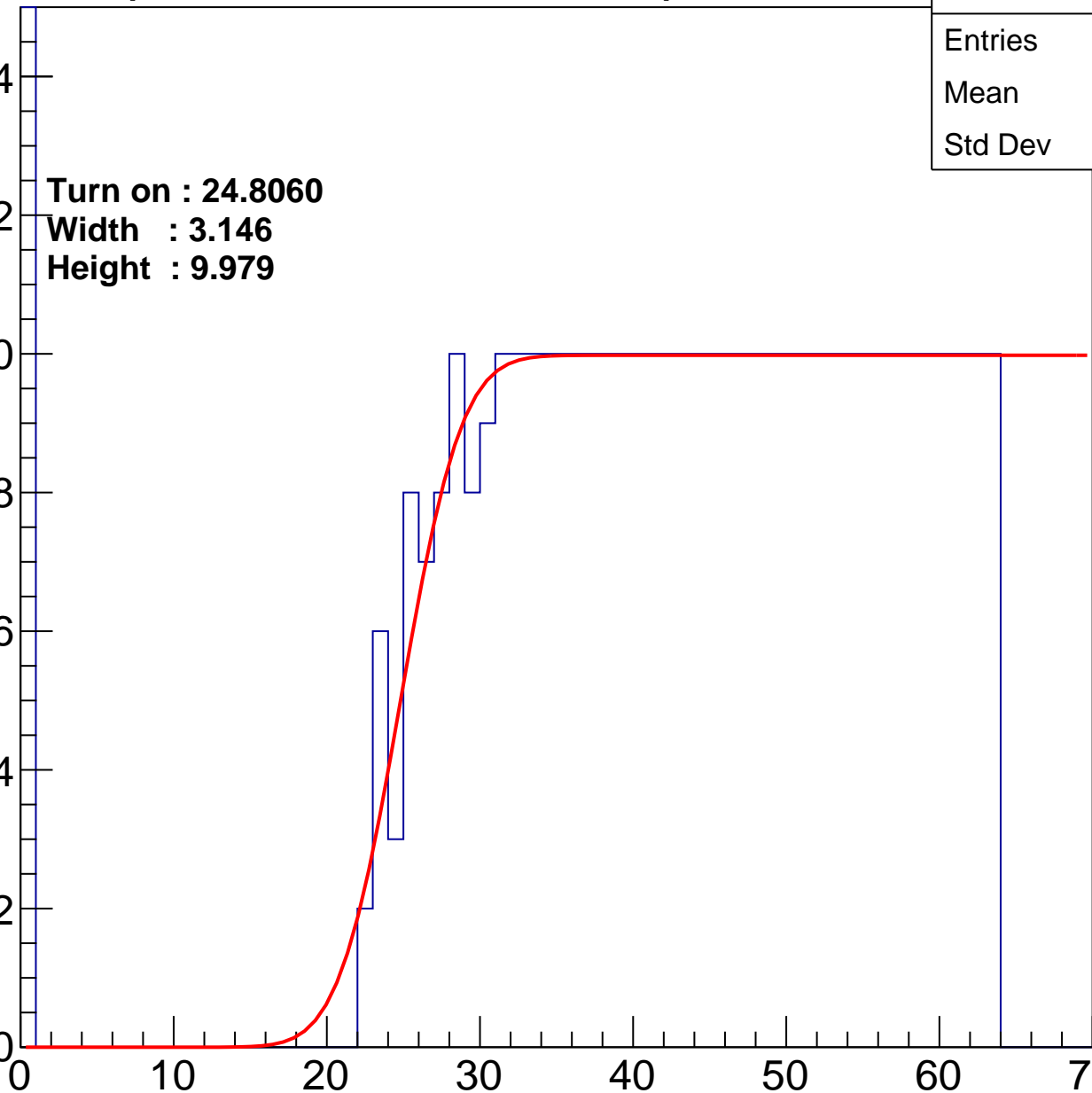
Width : 3.146

Height : 9.979

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch93

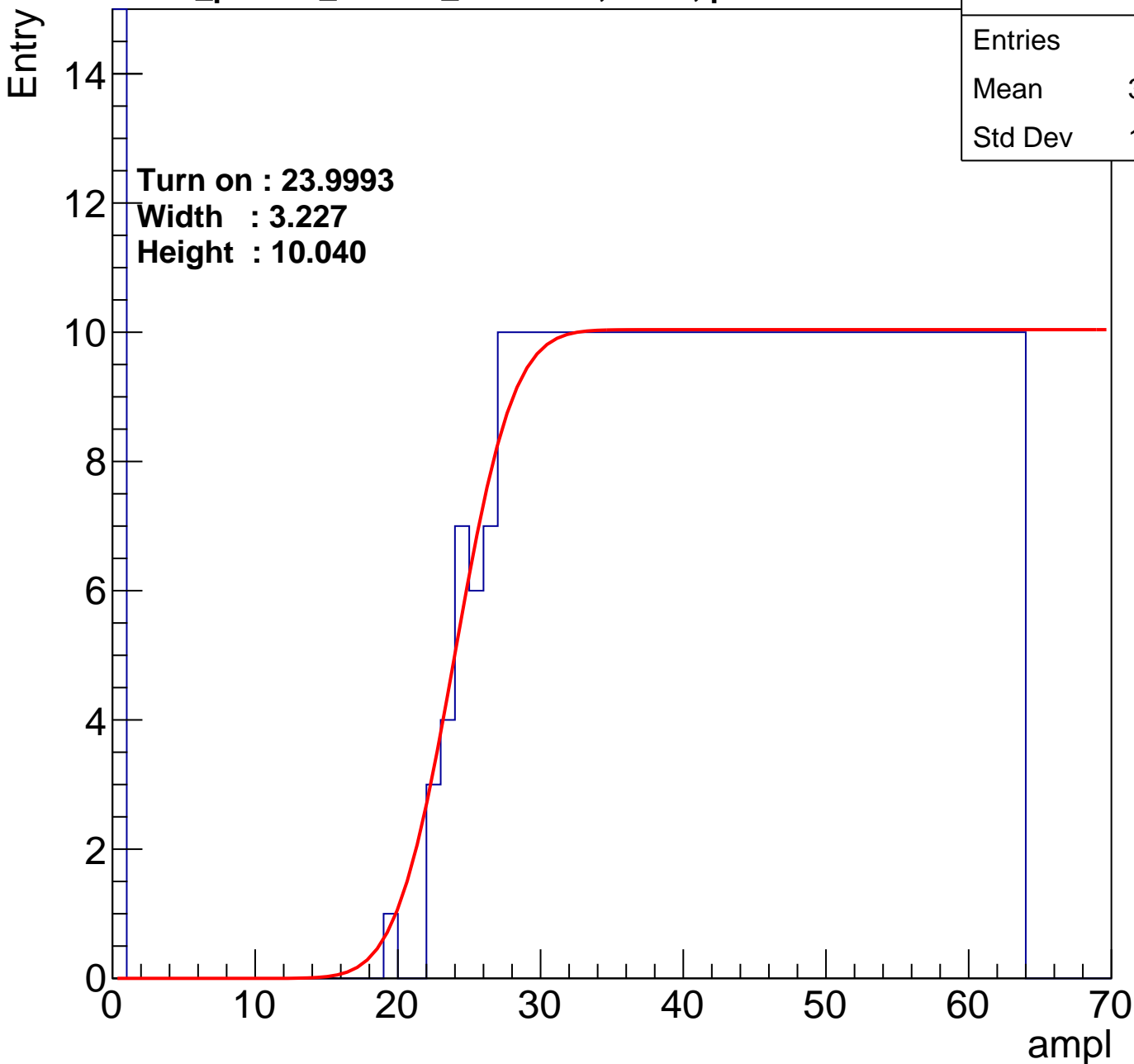
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	447
Mean	38.76
Std Dev	17.46

Turn on : 23.9993

Width : 3.227

Height : 10.040



# B1L103S, U20-ch94

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	457
Mean	38.24
Std Dev	17.64

Turn on : 23.7186

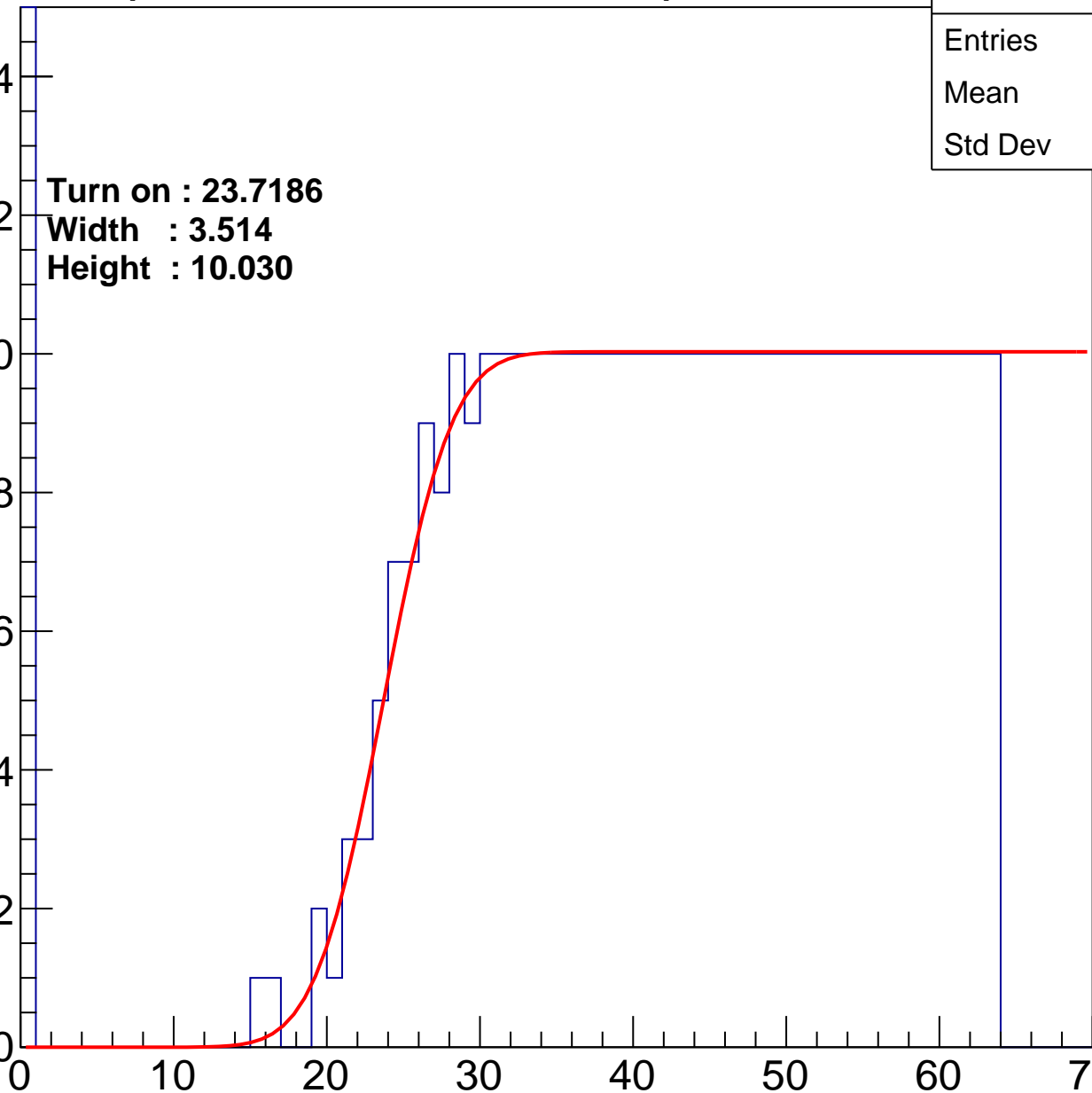
Width : 3.514

Height : 10.030

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U20-ch95

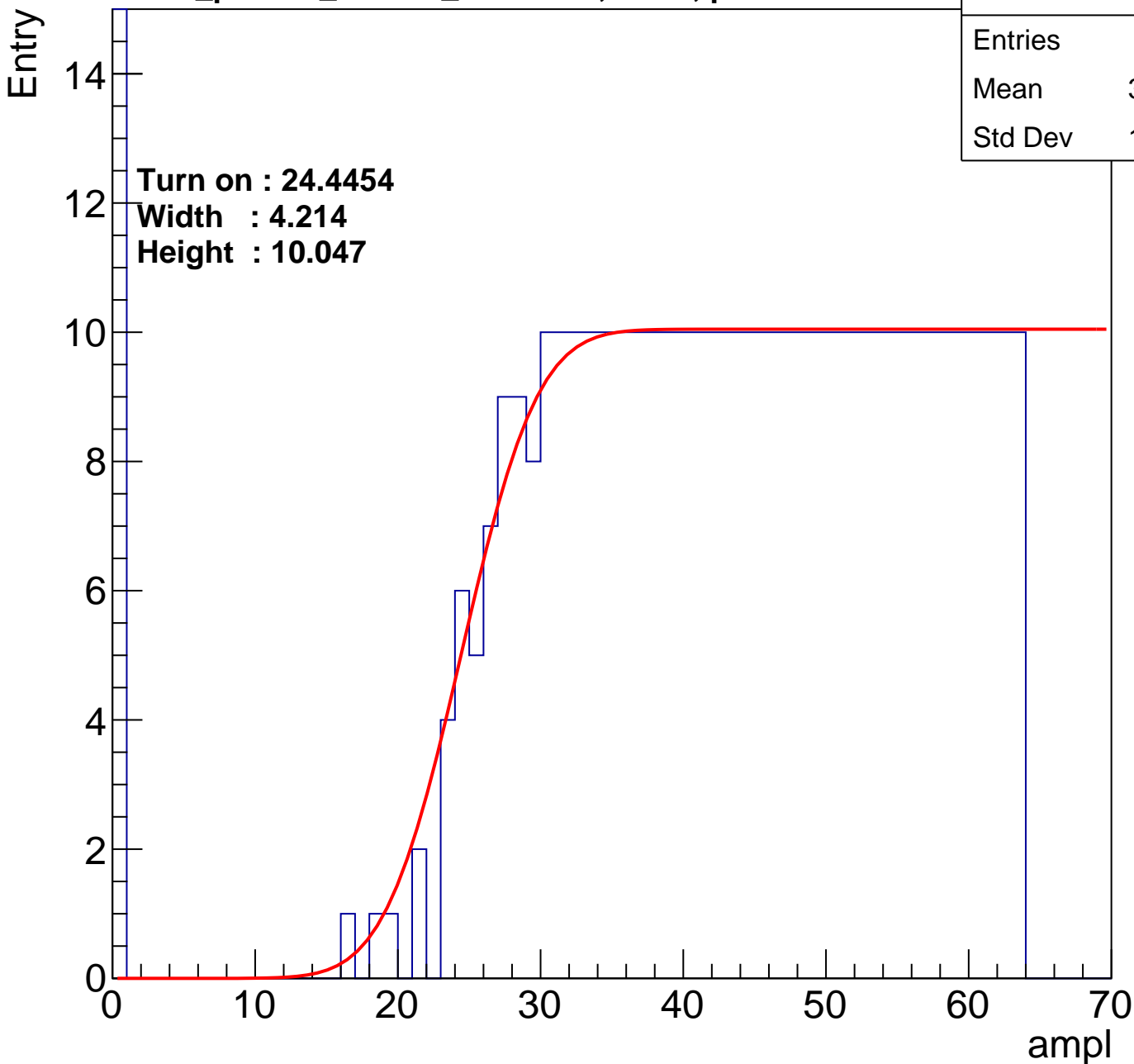
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	435
Mean	39.48
Std Dev	16.98

Turn on : 24.4454

Width : 4.214

Height : 10.047



# B1L103S, U20-ch96

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	475
Mean	37.21
Std Dev	18.32

Turn on : 24.2168

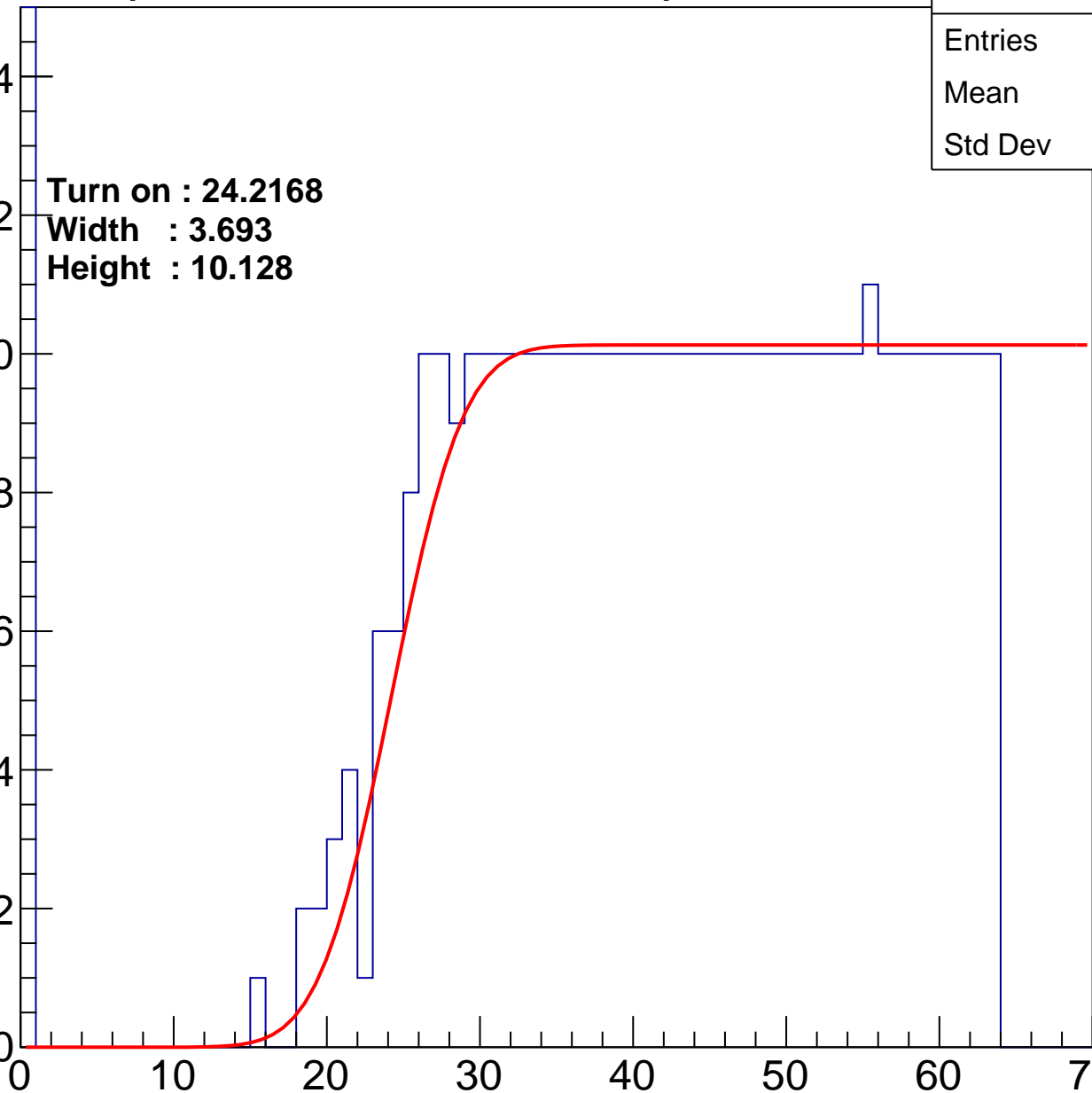
Width : 3.693

Height : 10.128

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch97

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	403
Mean	40.31
Std Dev	17.55

Turn on : 28.6164

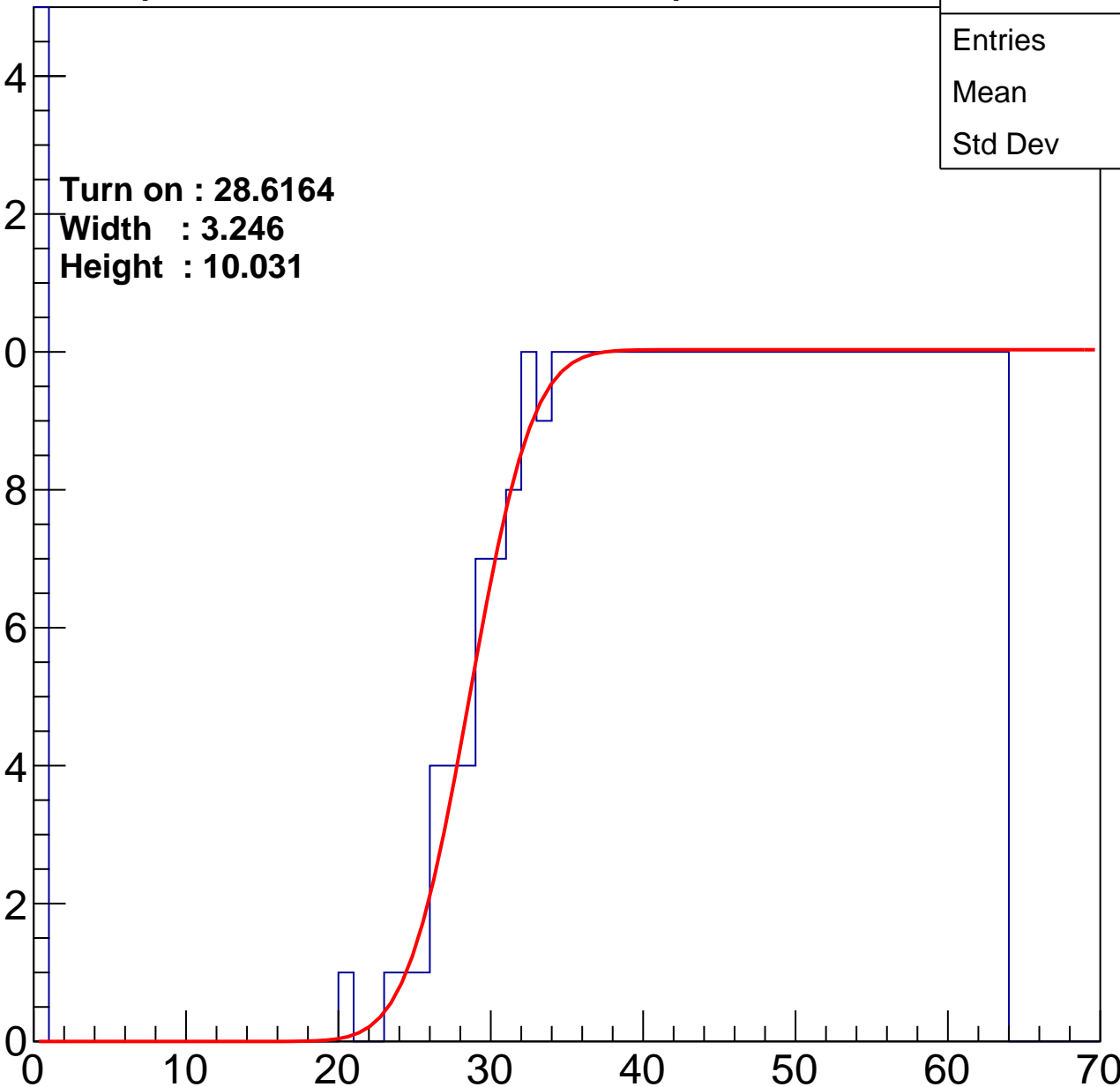
Width : 3.246

Height : 10.031

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch98

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	477
Mean	37.57
Std Dev	17.7

Turn on : 23.5784

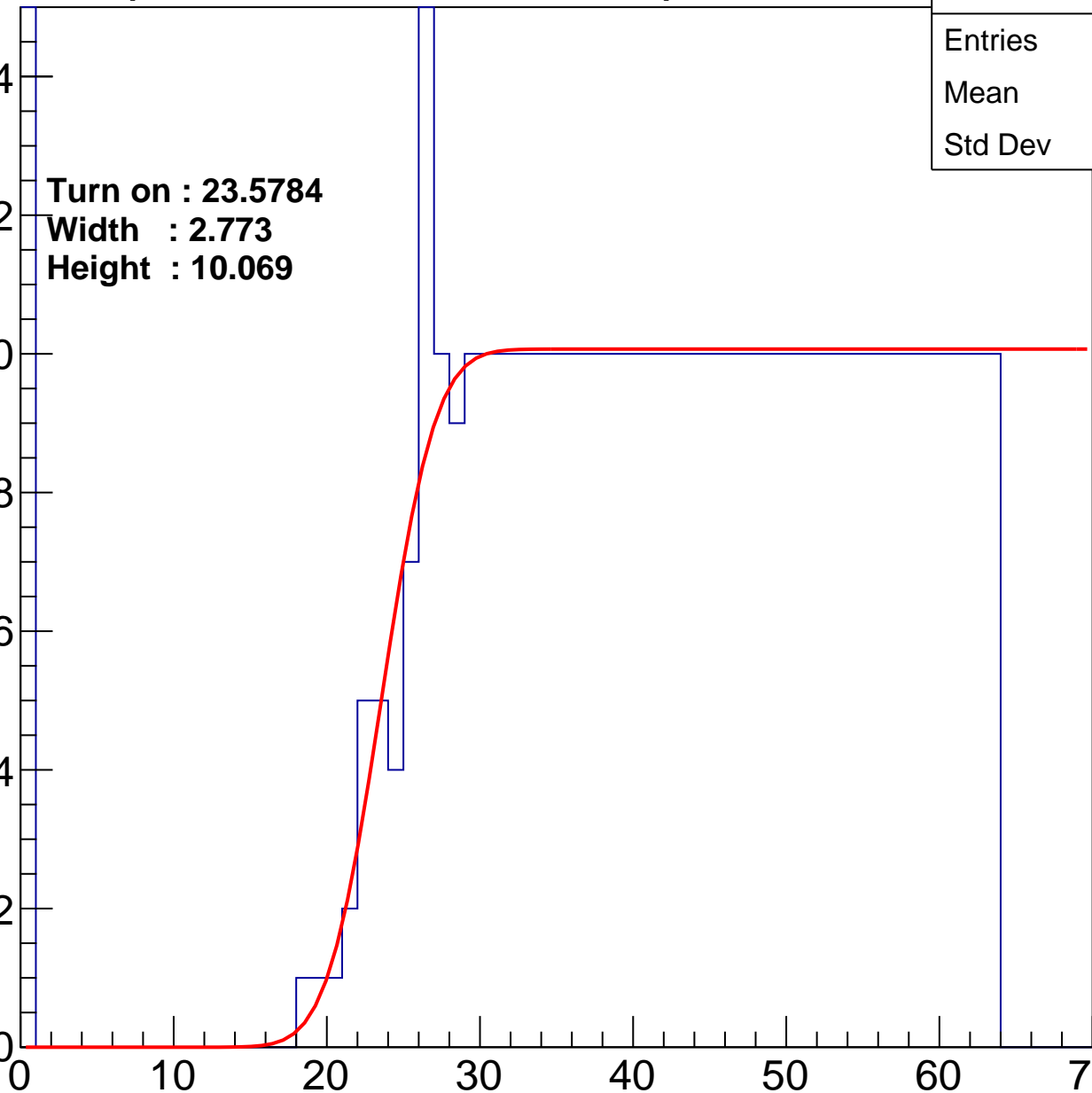
Width : 2.773

Height : 10.069

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch99

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	434
Mean	39.75
Std Dev	16.61

Turn on : 24.7689

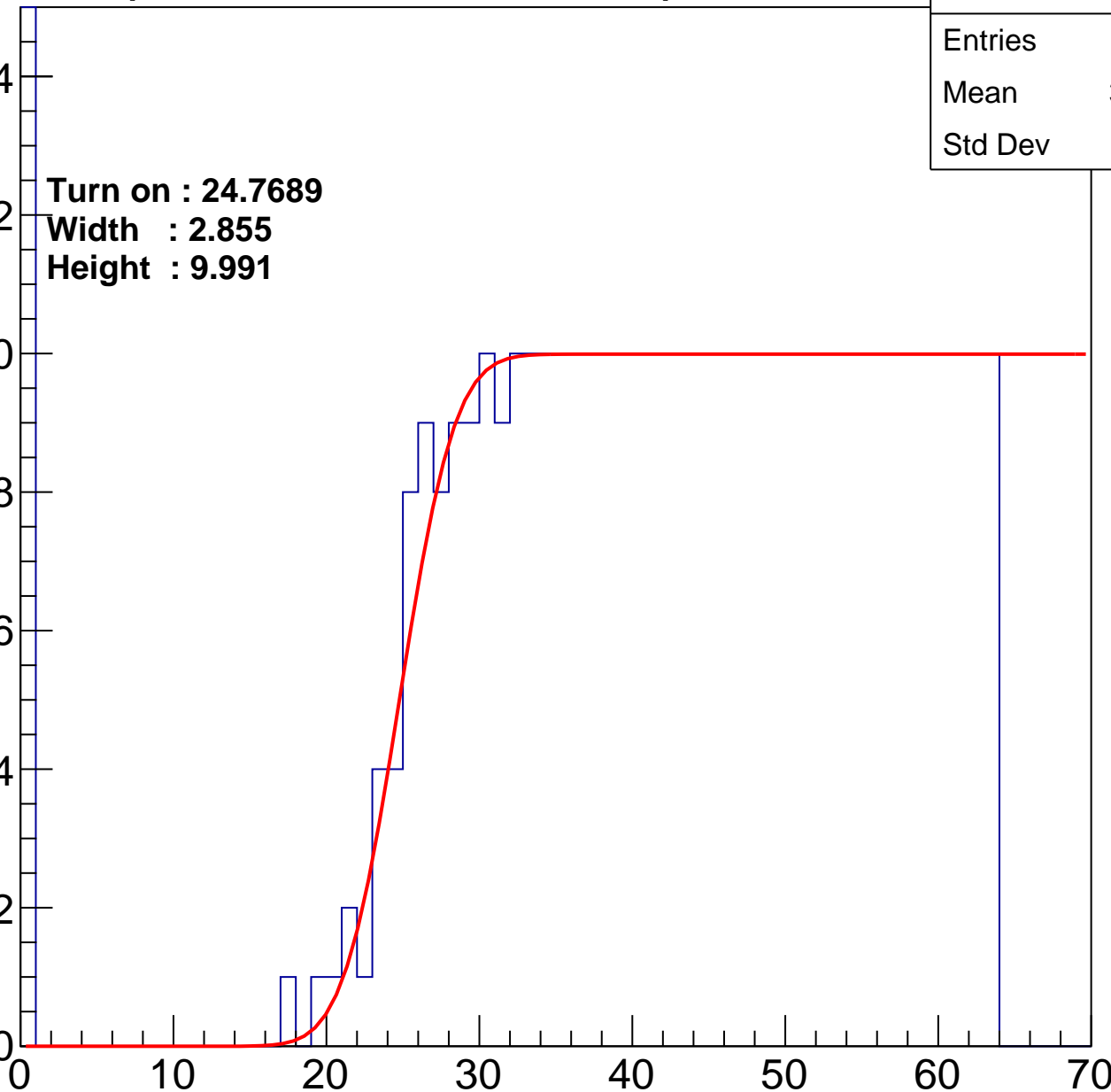
Width : 2.855

Height : 9.991

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch100

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	458
Mean	38.56
Std Dev	17.13

**Turn on : 23.0263**

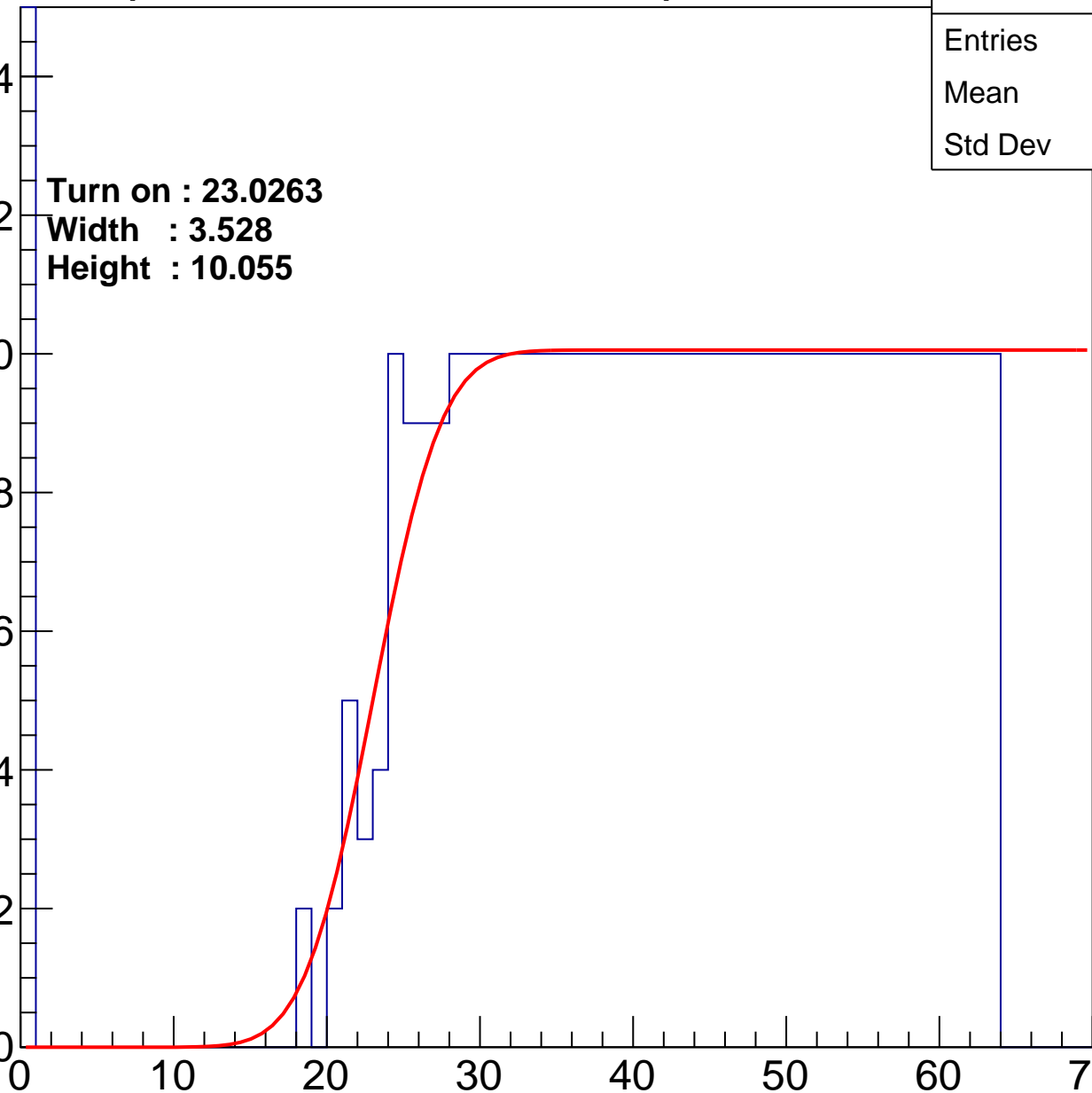
**Width : 3.528**

**Height : 10.055**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch101

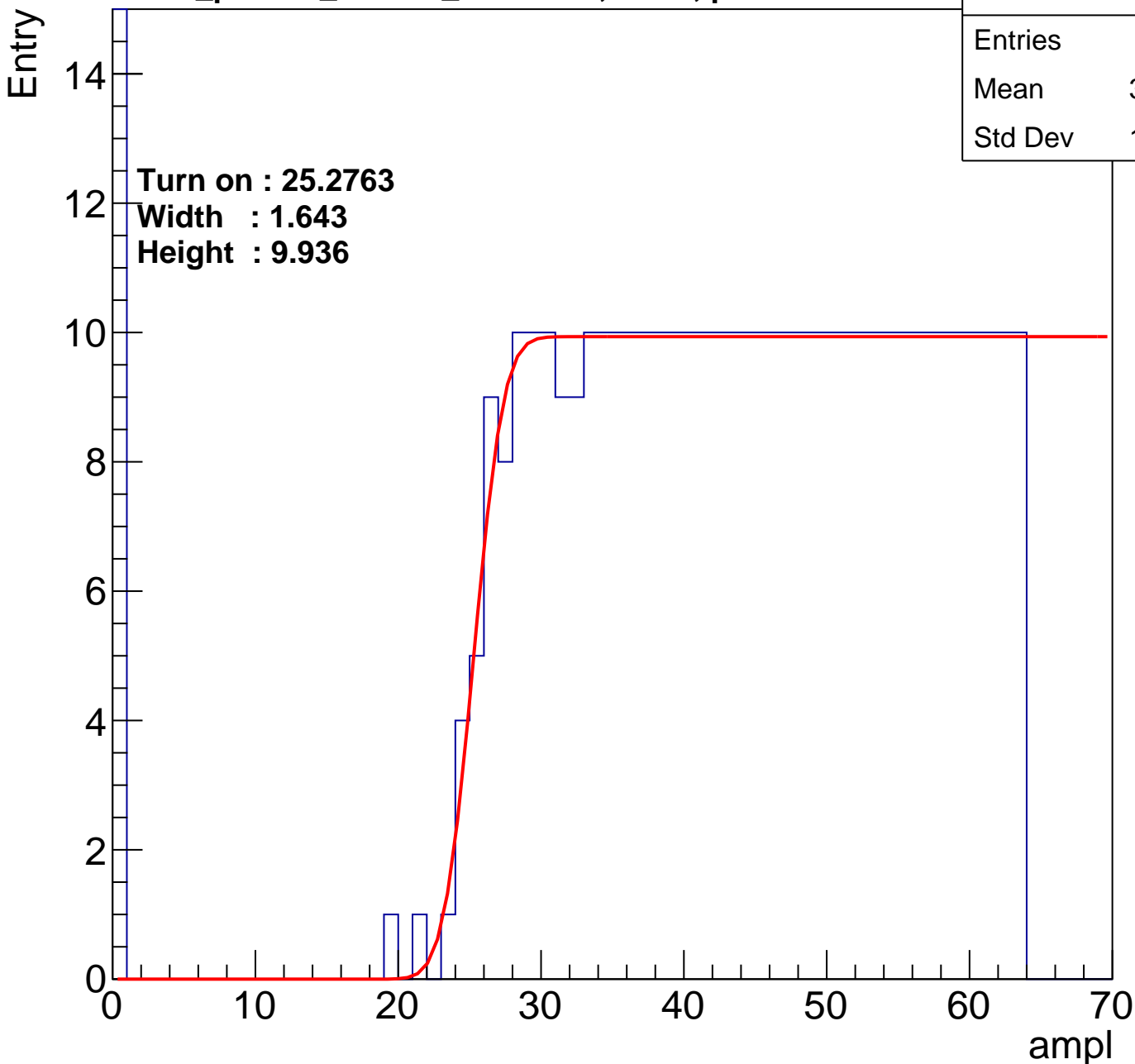
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	450
Mean	37.89
Std Dev	18.54

Turn on : 25.2763

Width : 1.643

Height : 9.936



# B1L103S, U20-ch102

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	460
Mean	38.1
Std Dev	17.7

Turn on : 23.3728

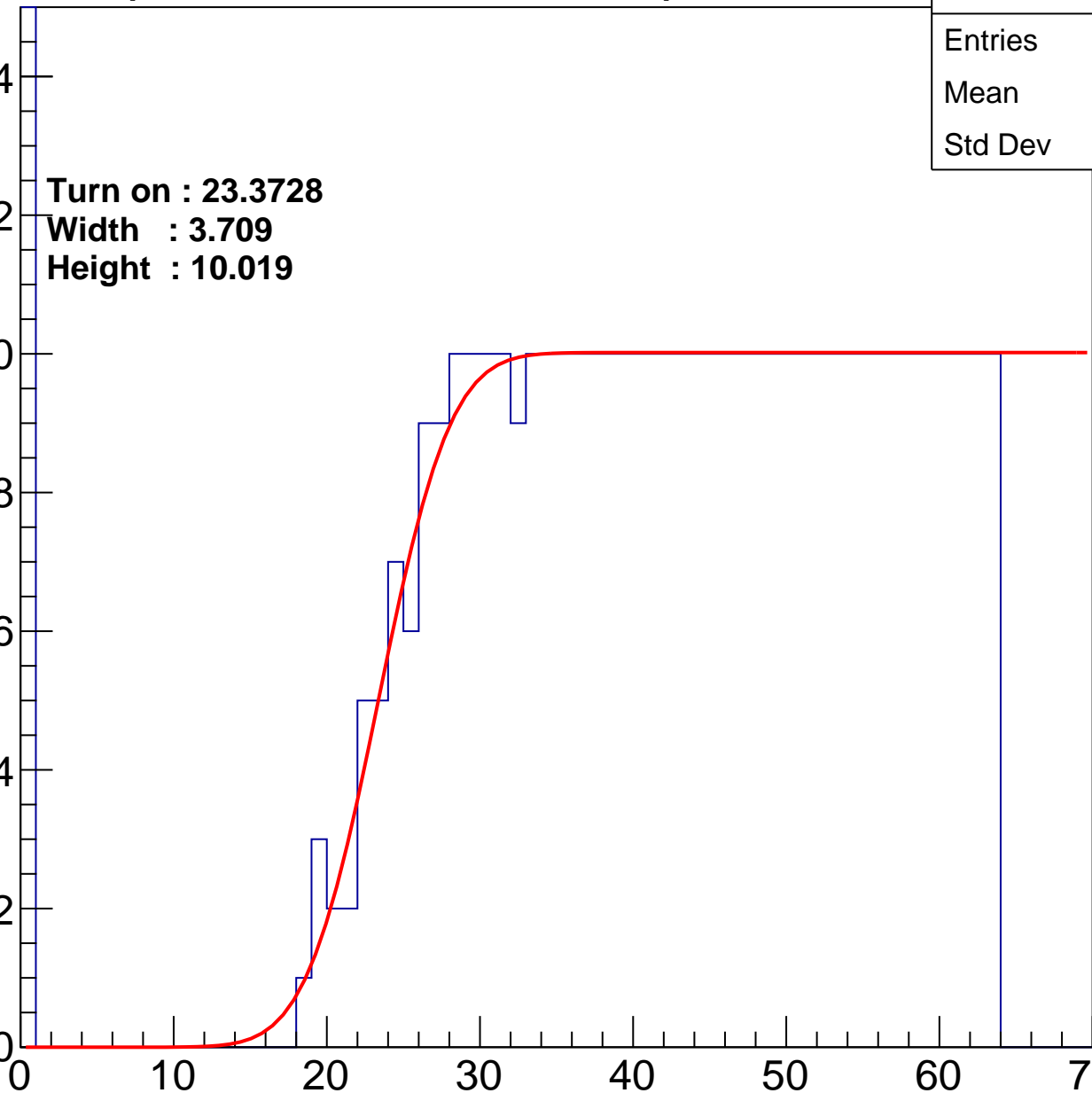
Width : 3.709

Height : 10.019

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U20-ch103

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	455
Mean	38.21
Std Dev	17.83

Turn on : 24.5226

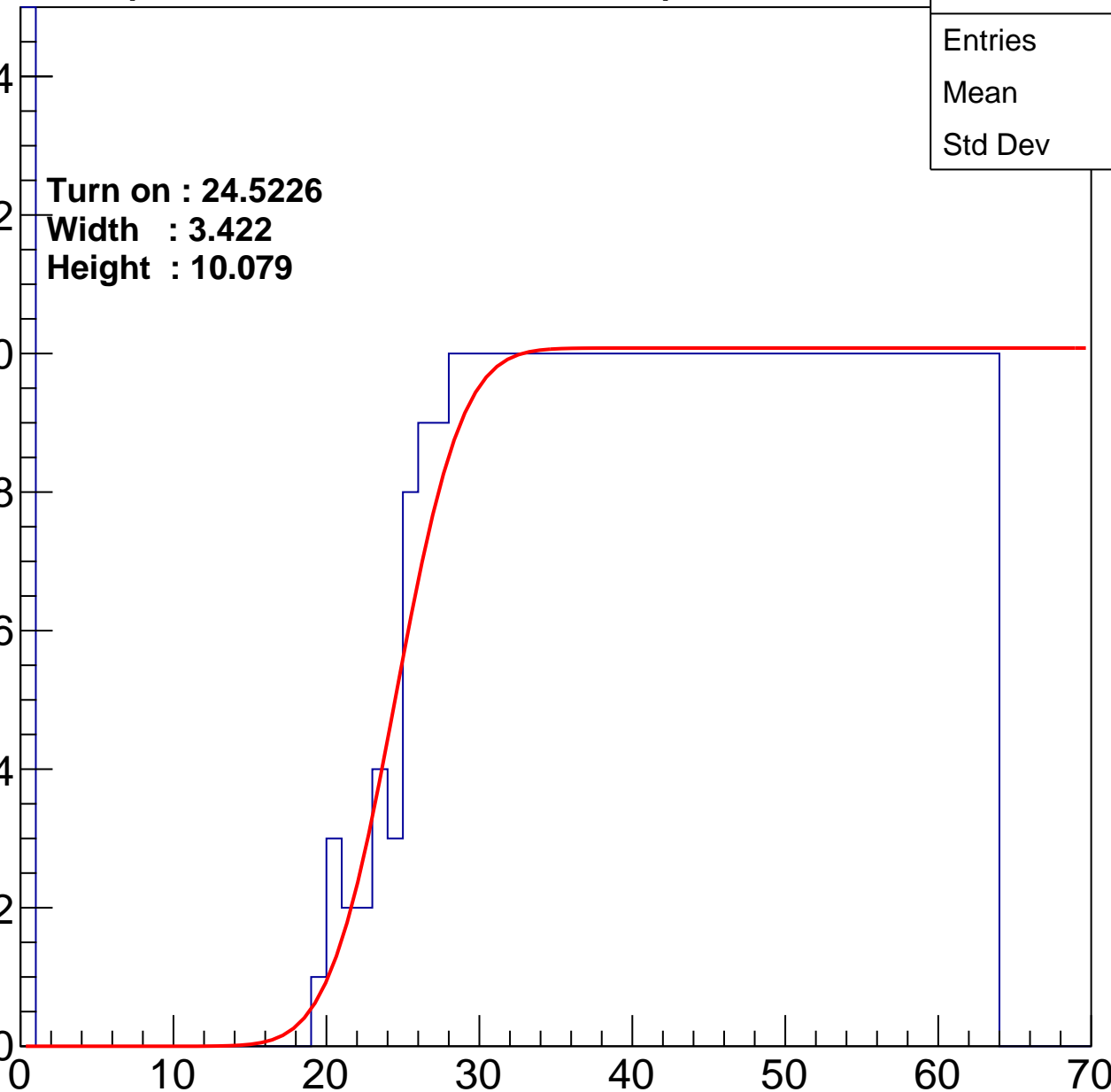
Width : 3.422

Height : 10.079

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch104

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	464
Mean	37.81
Std Dev	17.94

**Turn on : 23.5880**

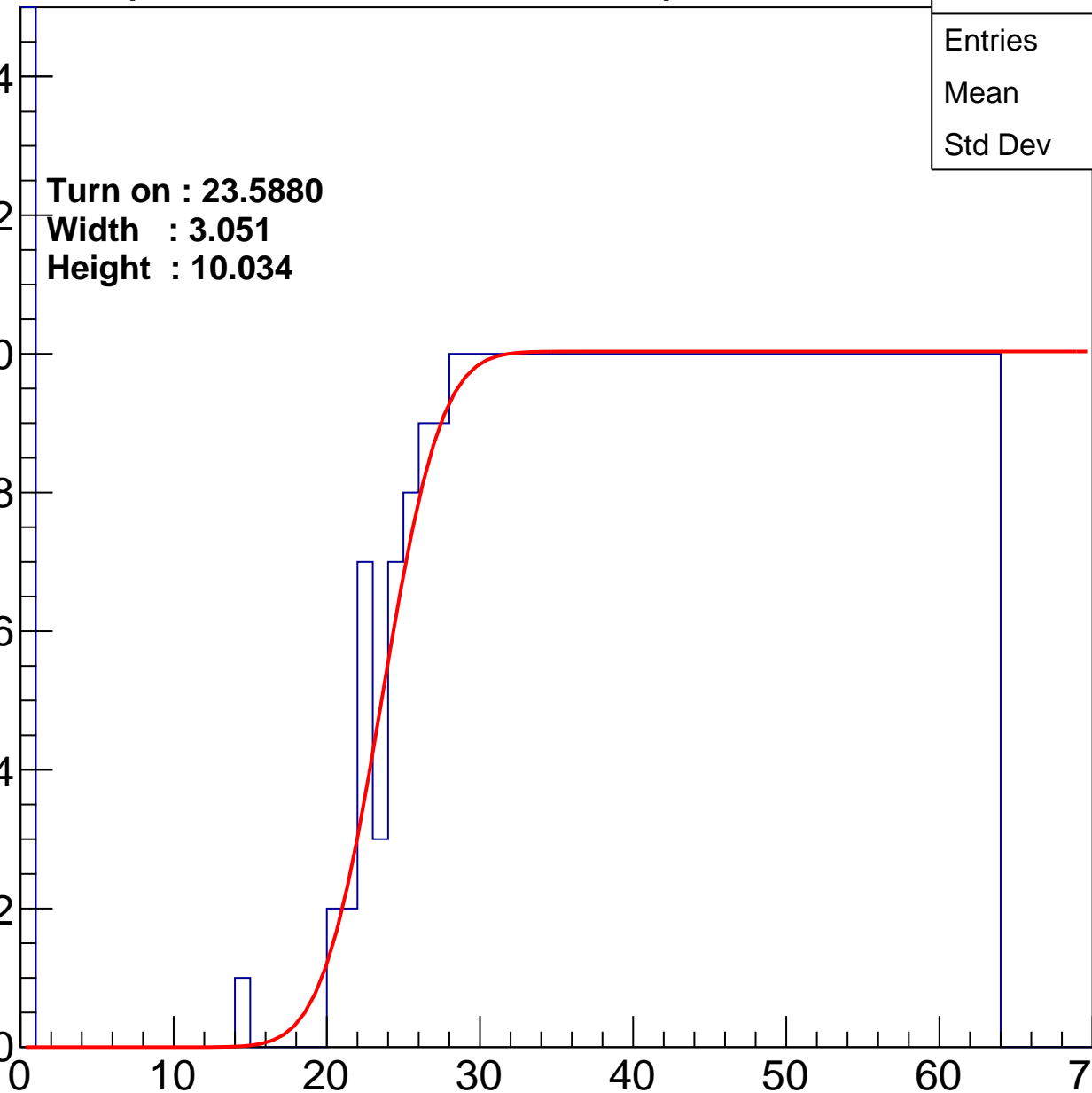
**Width : 3.051**

**Height : 10.034**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch105

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	434
Mean	39.44
Std Dev	17.13

**Turn on : 25.4635**

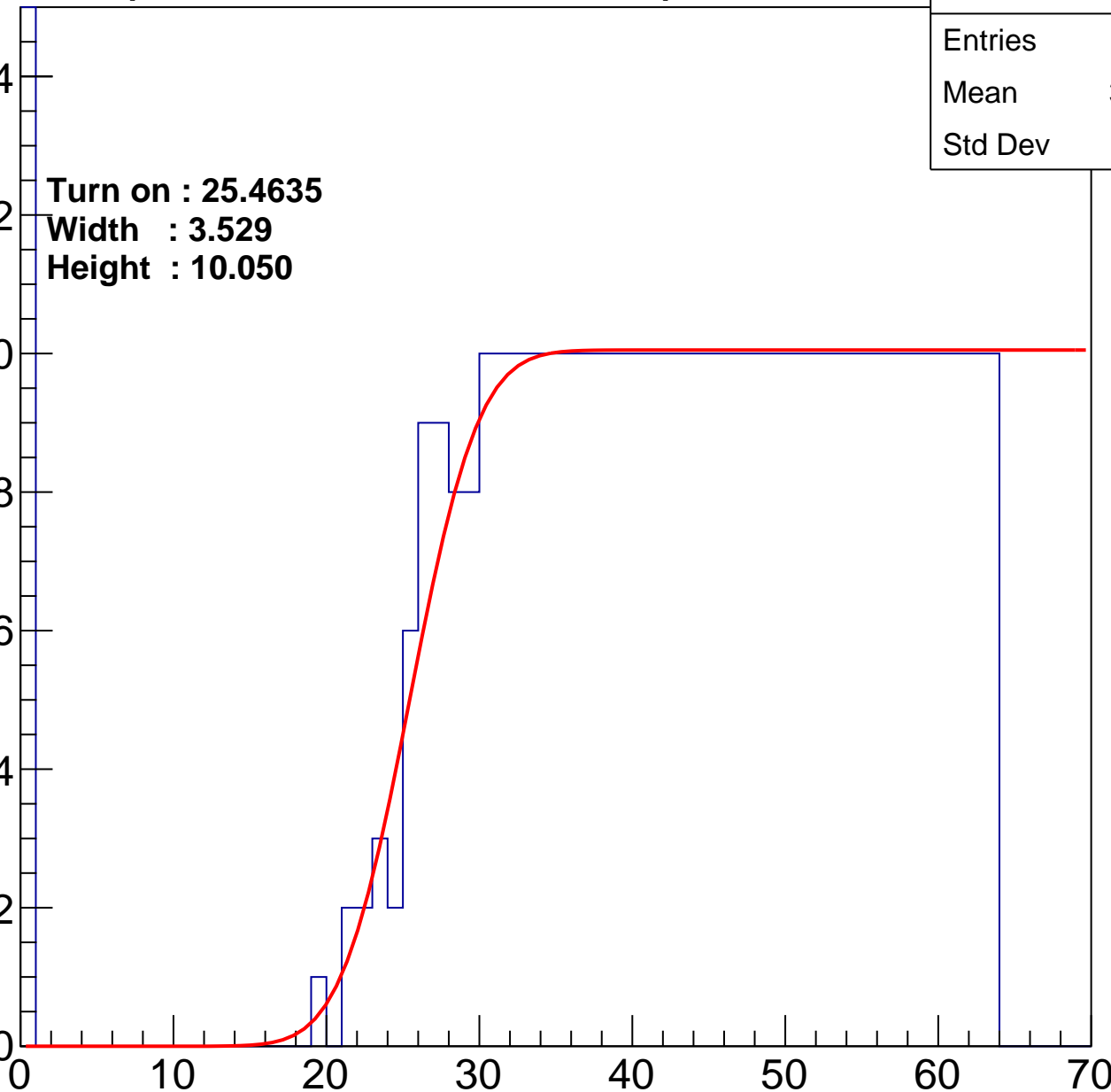
**Width : 3.529**

**Height : 10.050**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch106

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	458
Mean	38.2
Std Dev	17.68

Turn on : 23.8842

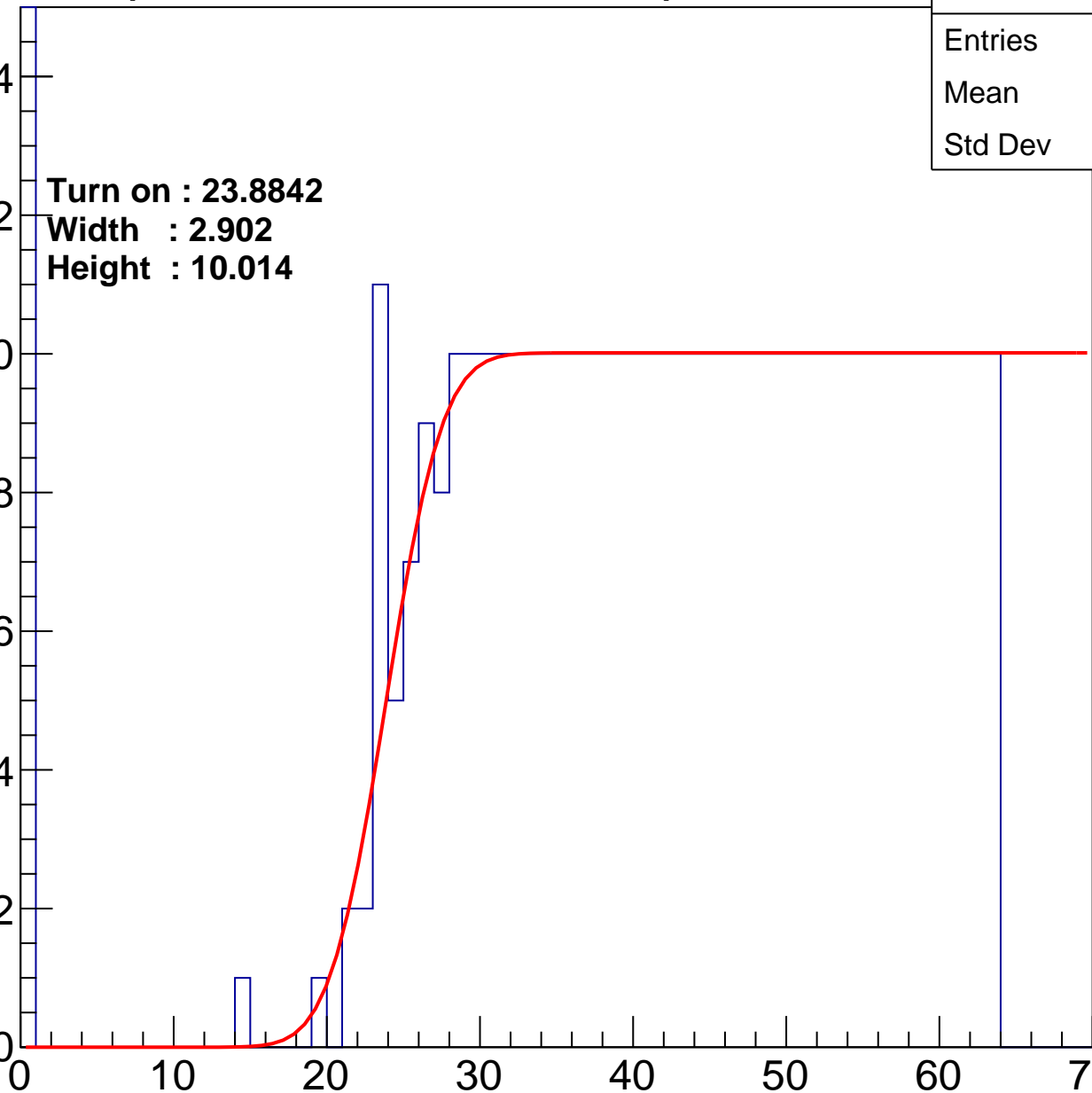
Width : 2.902

Height : 10.014

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch107

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	423
Mean	39.81
Std Dev	17.14

**Turn on : 26.5089**

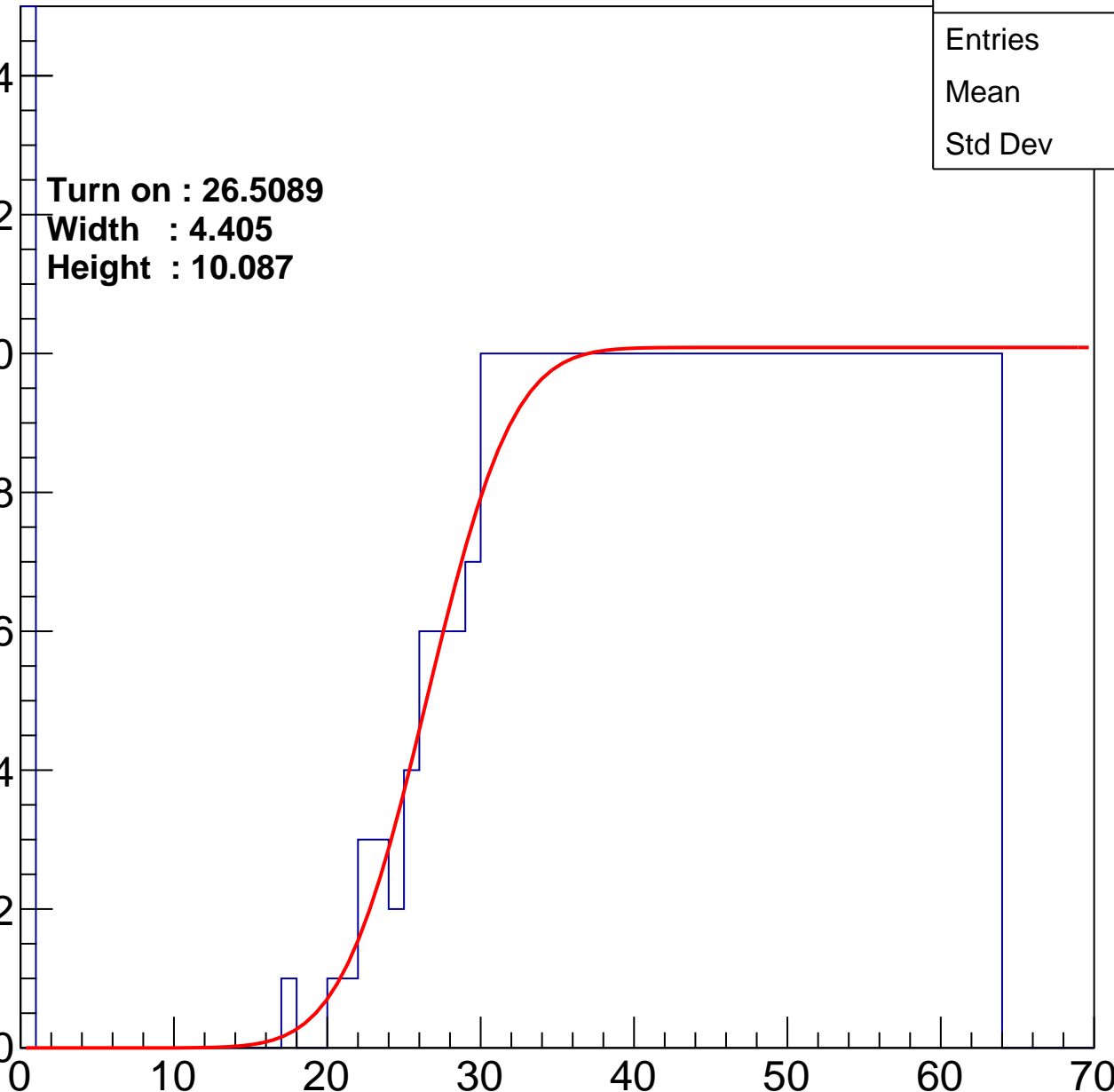
**Width : 4.405**

**Height : 10.087**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch108

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	455
Mean	38.09
Std Dev	17.95

Turn on : 24.2726

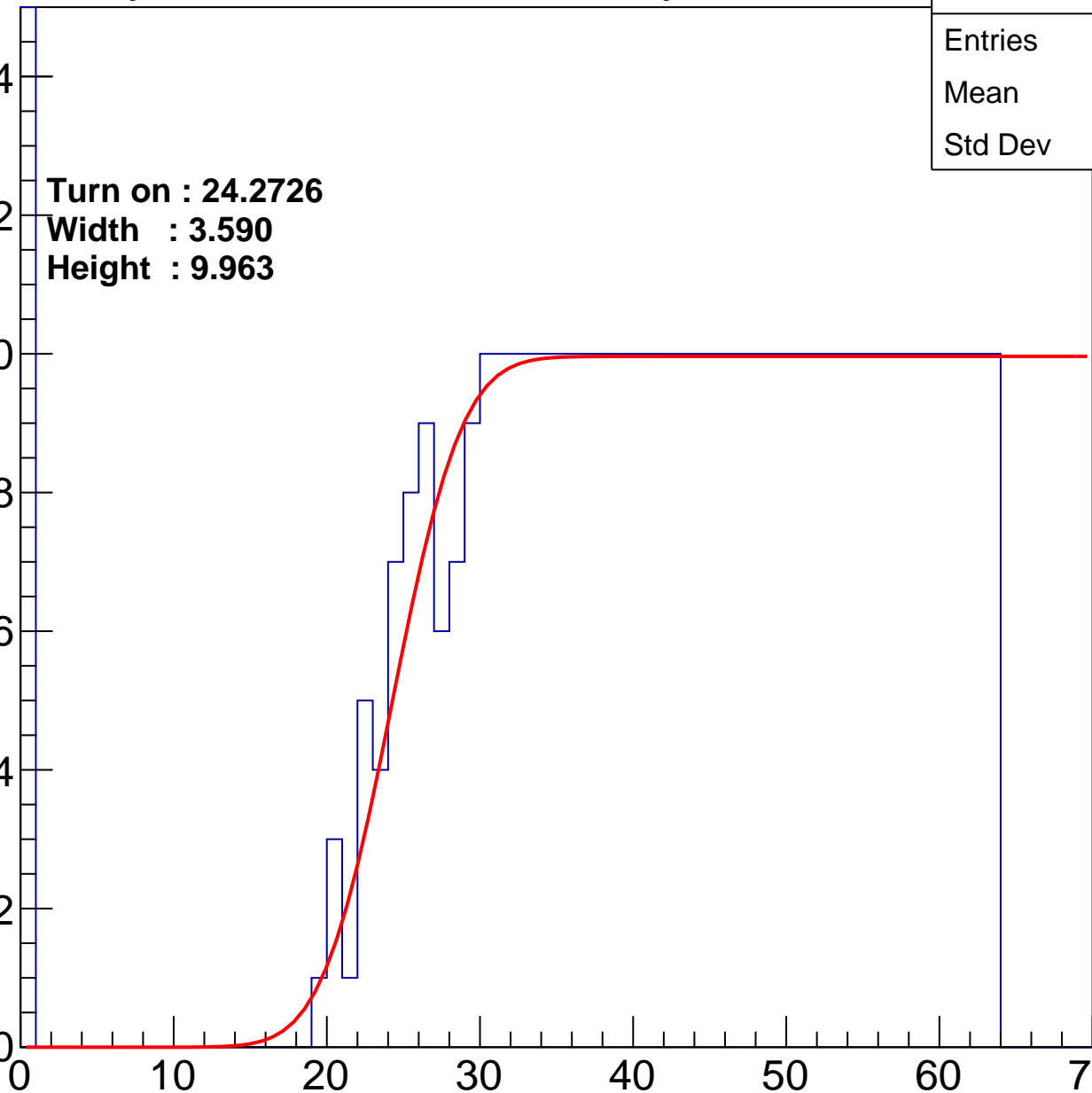
Width : 3.590

Height : 9.963

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch109

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	480
Mean	36.65
Std Dev	18.73

Turn on : 22.7885

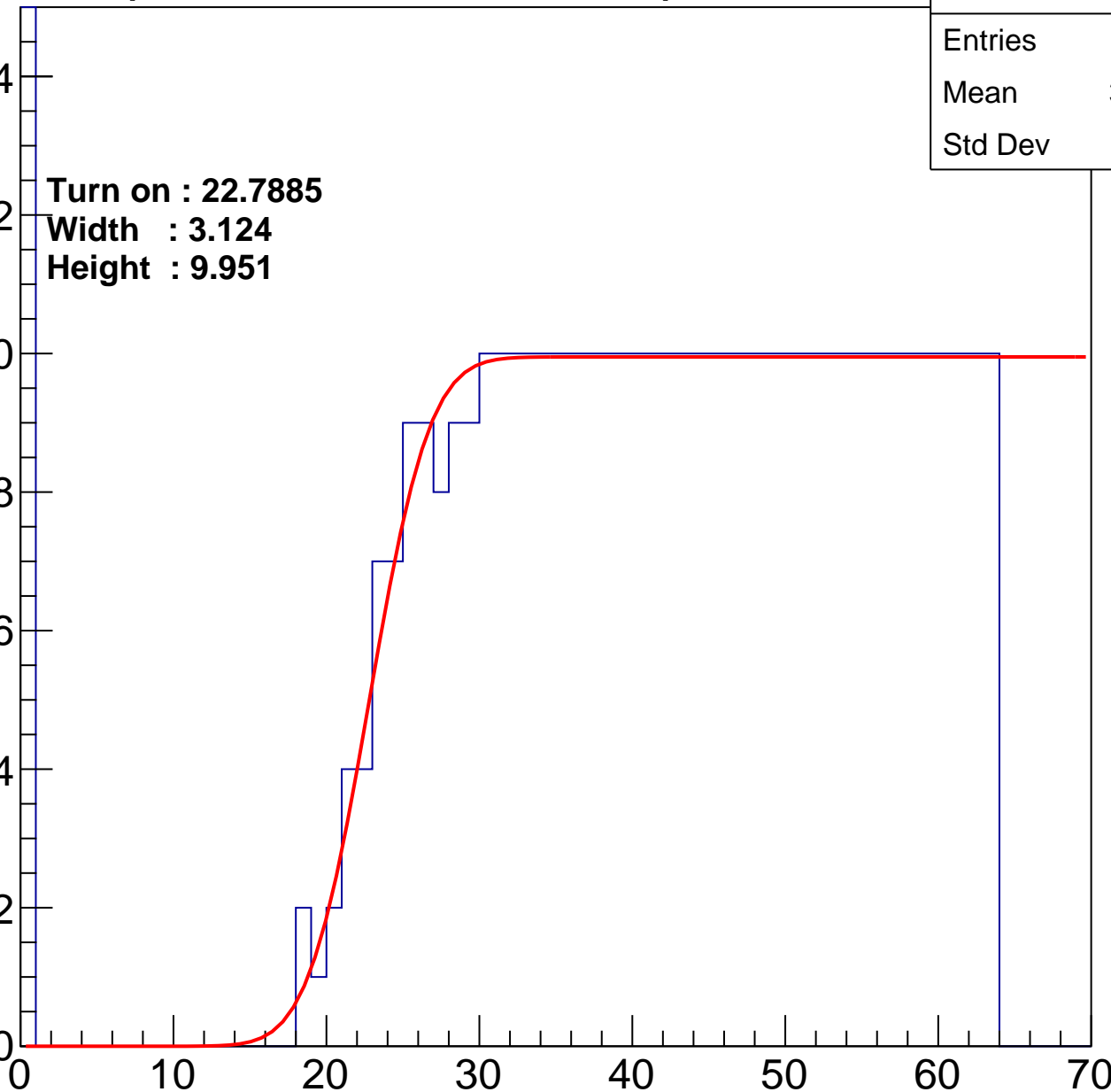
Width : 3.124

Height : 9.951

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch110

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	439
Mean	39.02
Std Dev	17.47

Turn on : 25.7592

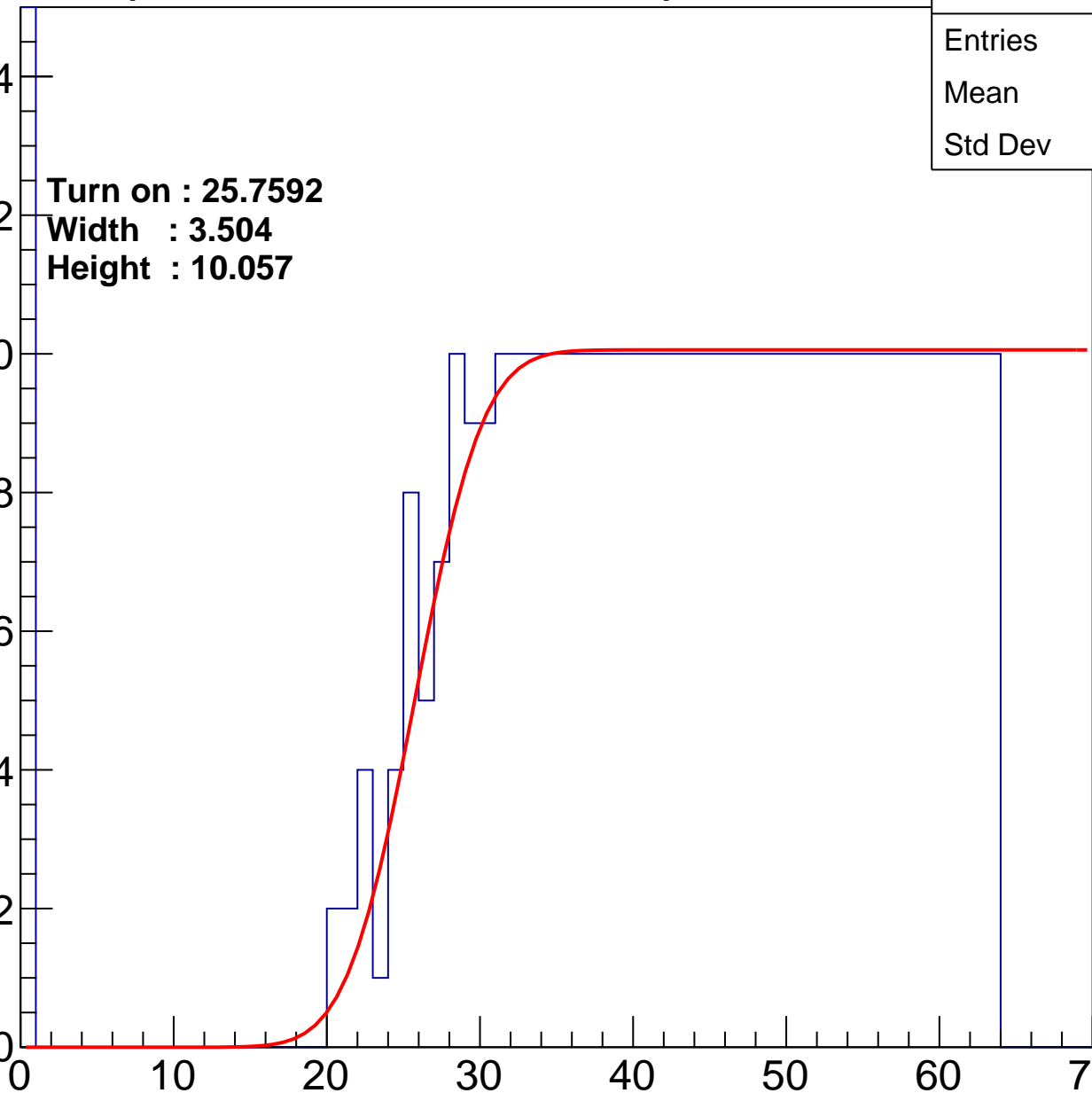
Width : 3.504

Height : 10.057

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U20-ch111

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	432
Mean	39.57
Std Dev	17.04

Turn on : 25.3735

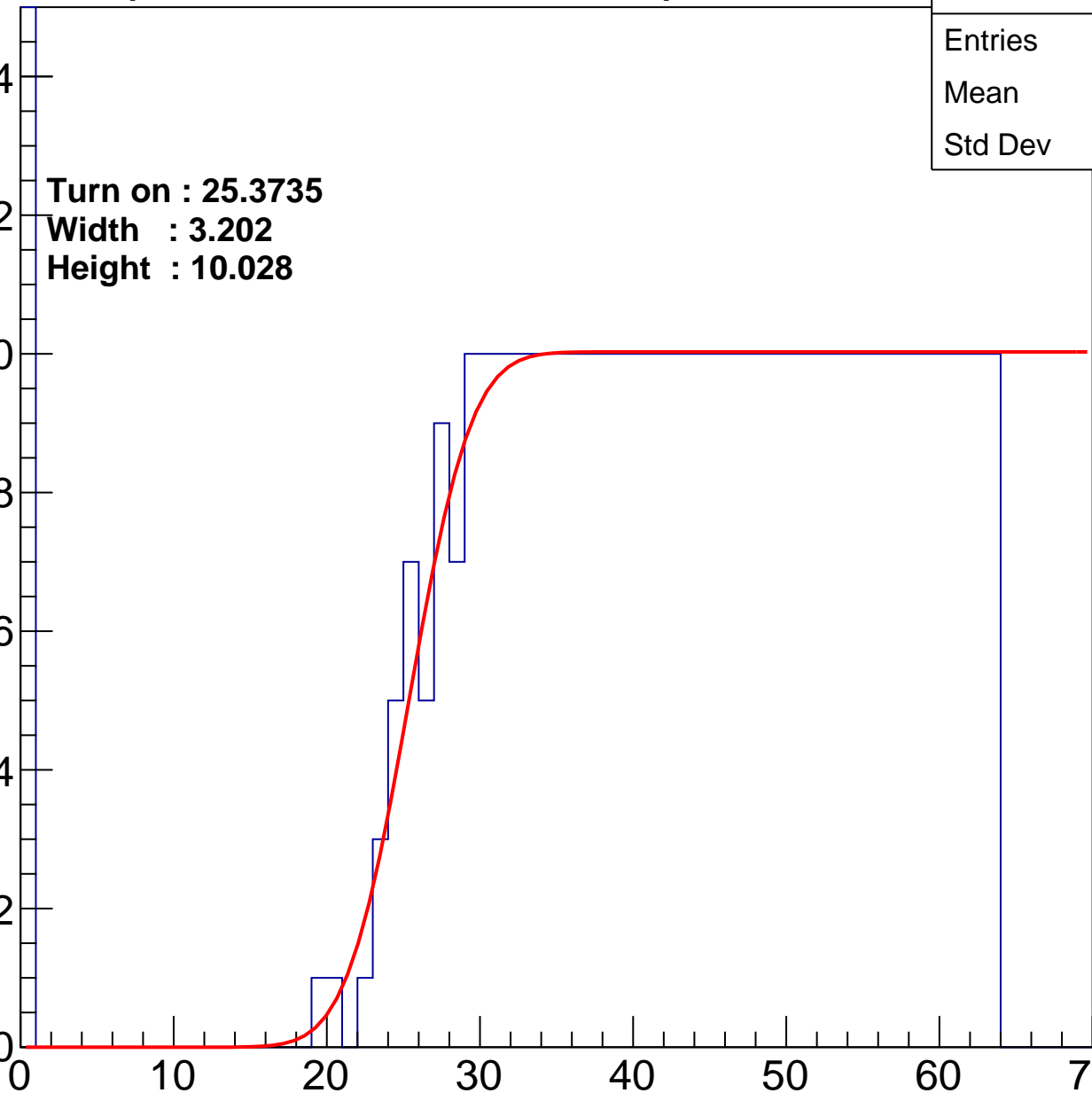
Width : 3.202

Height : 10.028

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch112

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	475
Mean	37.82
Std Dev	17.7

Turn on : 22.6882

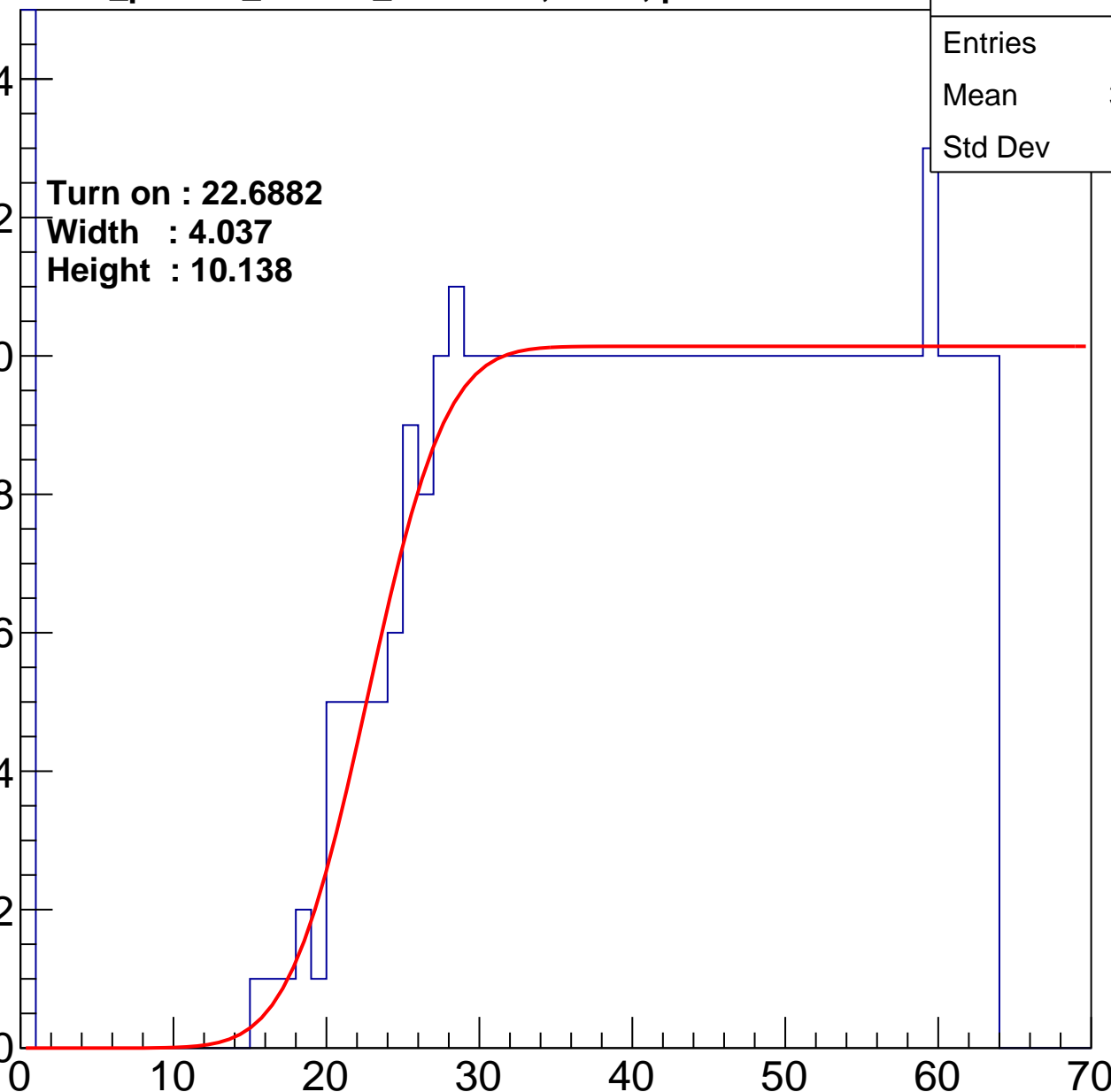
Width : 4.037

Height : 10.138

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch113

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	464
Mean	37.66
Std Dev	18.12

**Turn on : 23.5099**

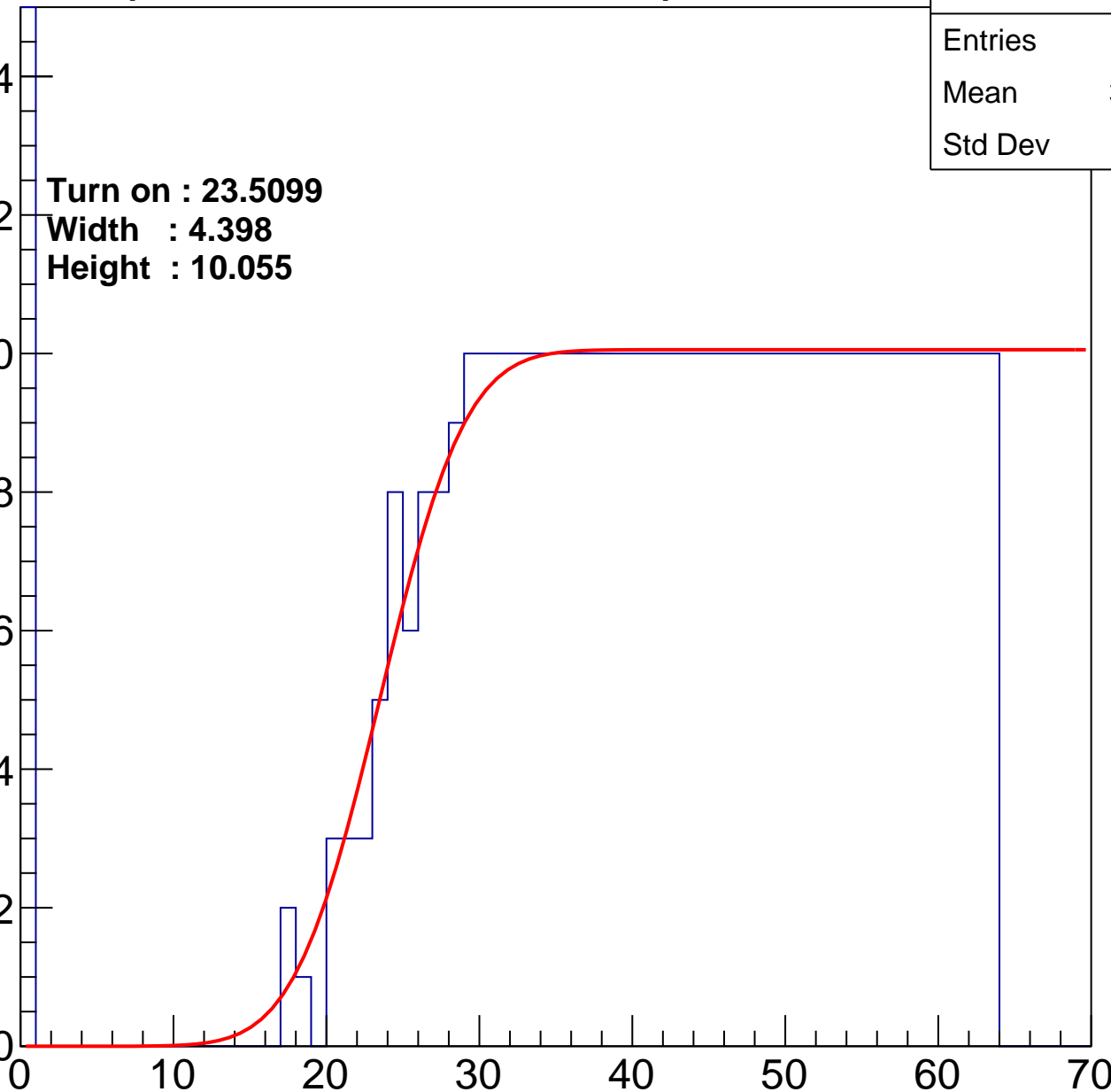
**Width : 4.398**

**Height : 10.055**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch114

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	472
Mean	37.5
Std Dev	17.97

**Turn on : 22.5260**

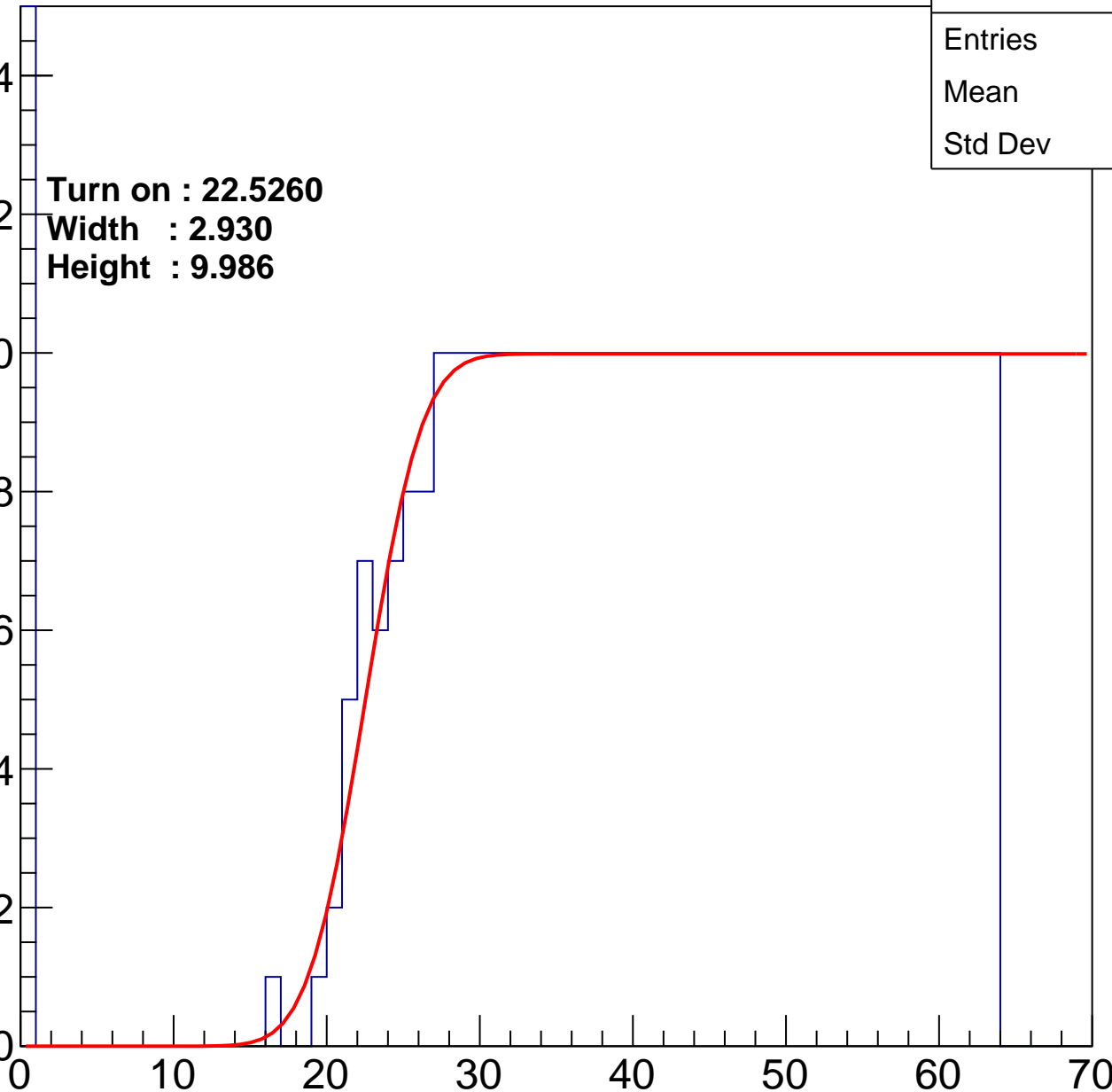
**Width : 2.930**

**Height : 9.986**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch115

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	462
Mean	37.18
Std Dev	18.93

Turn on : 24.9443

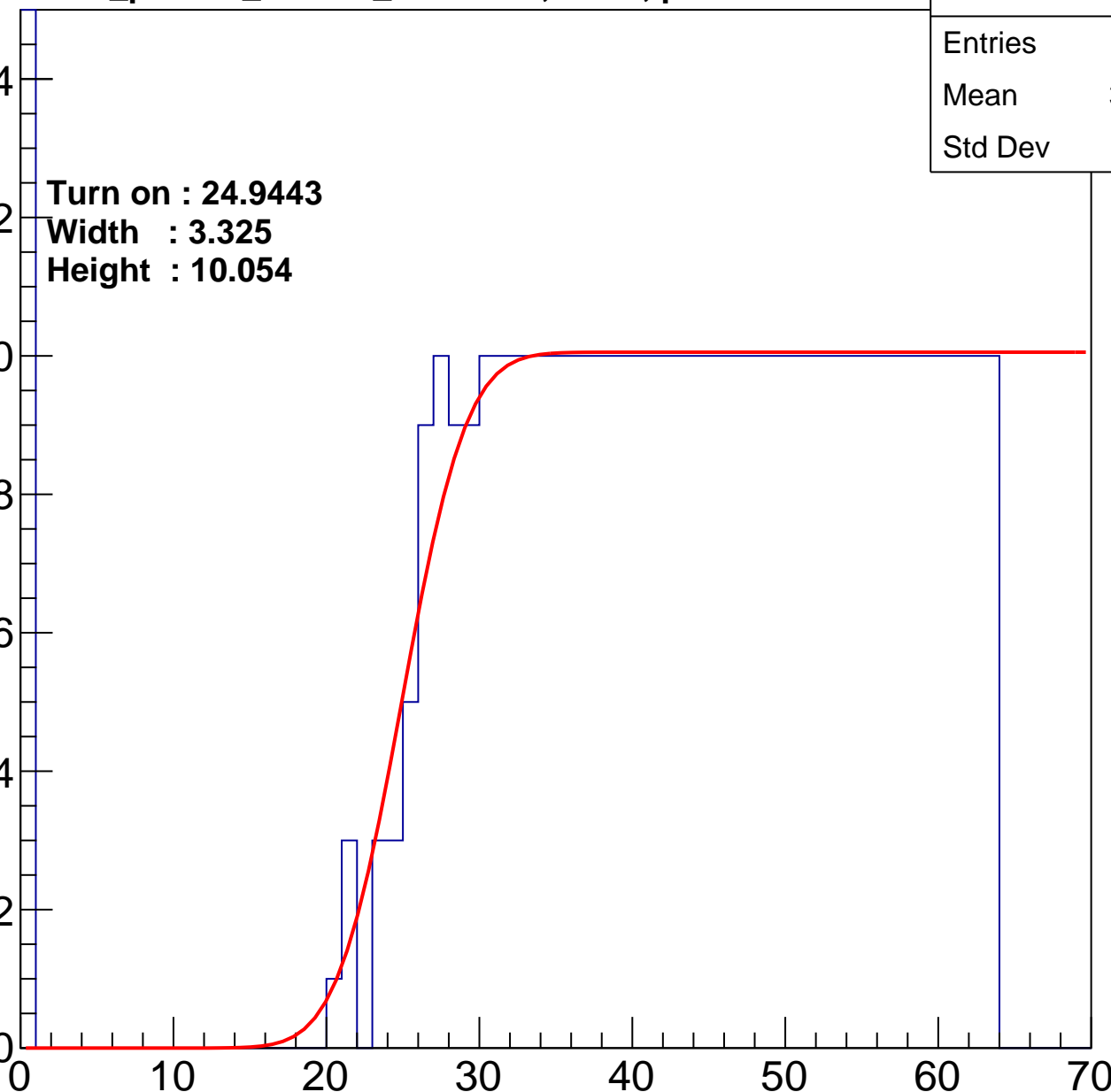
Width : 3.325

Height : 10.054

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch116

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	437
Mean	39.73
Std Dev	16.45

Turn on : 24.6868

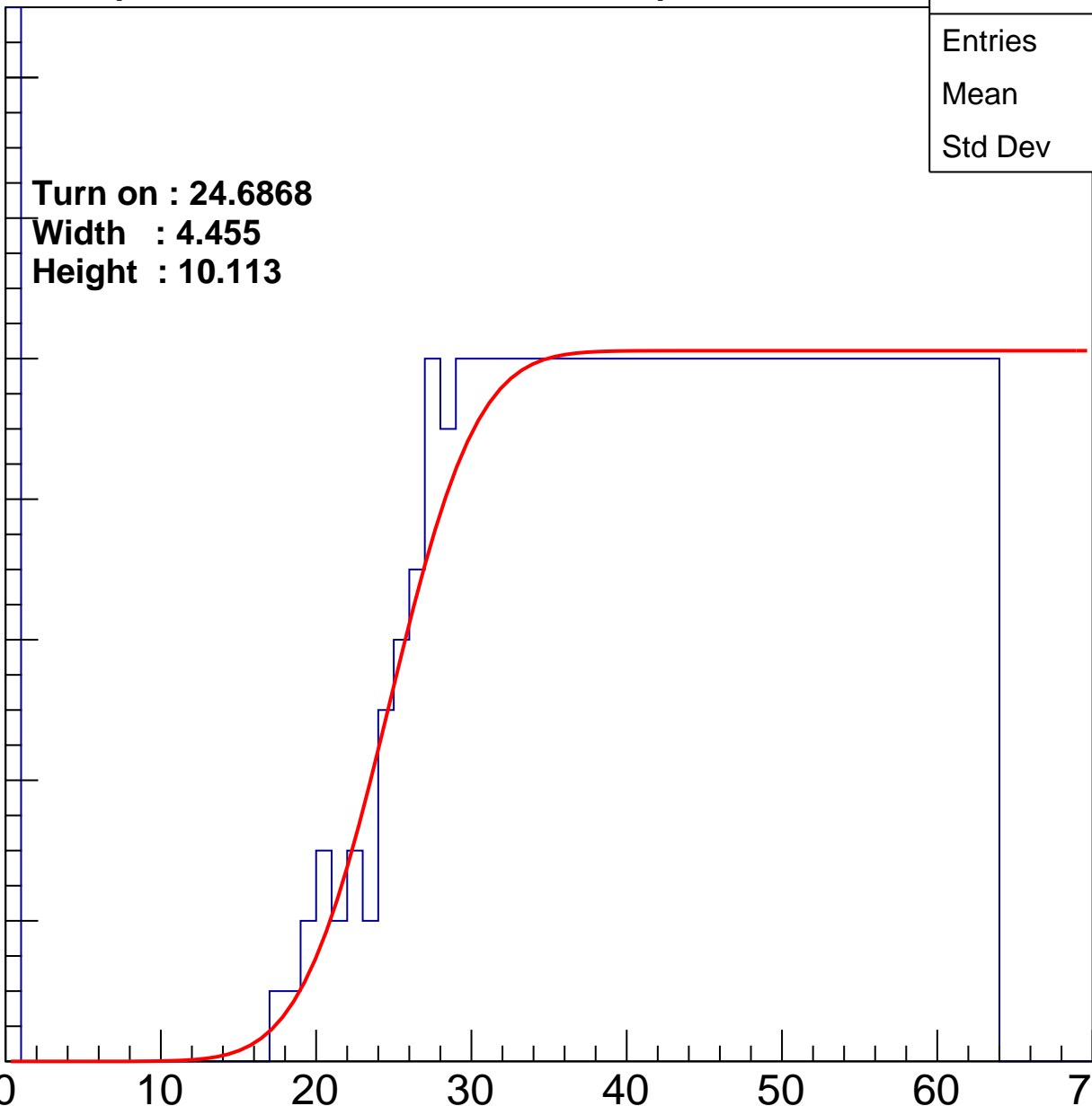
Width : 4.455

Height : 10.113

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch117

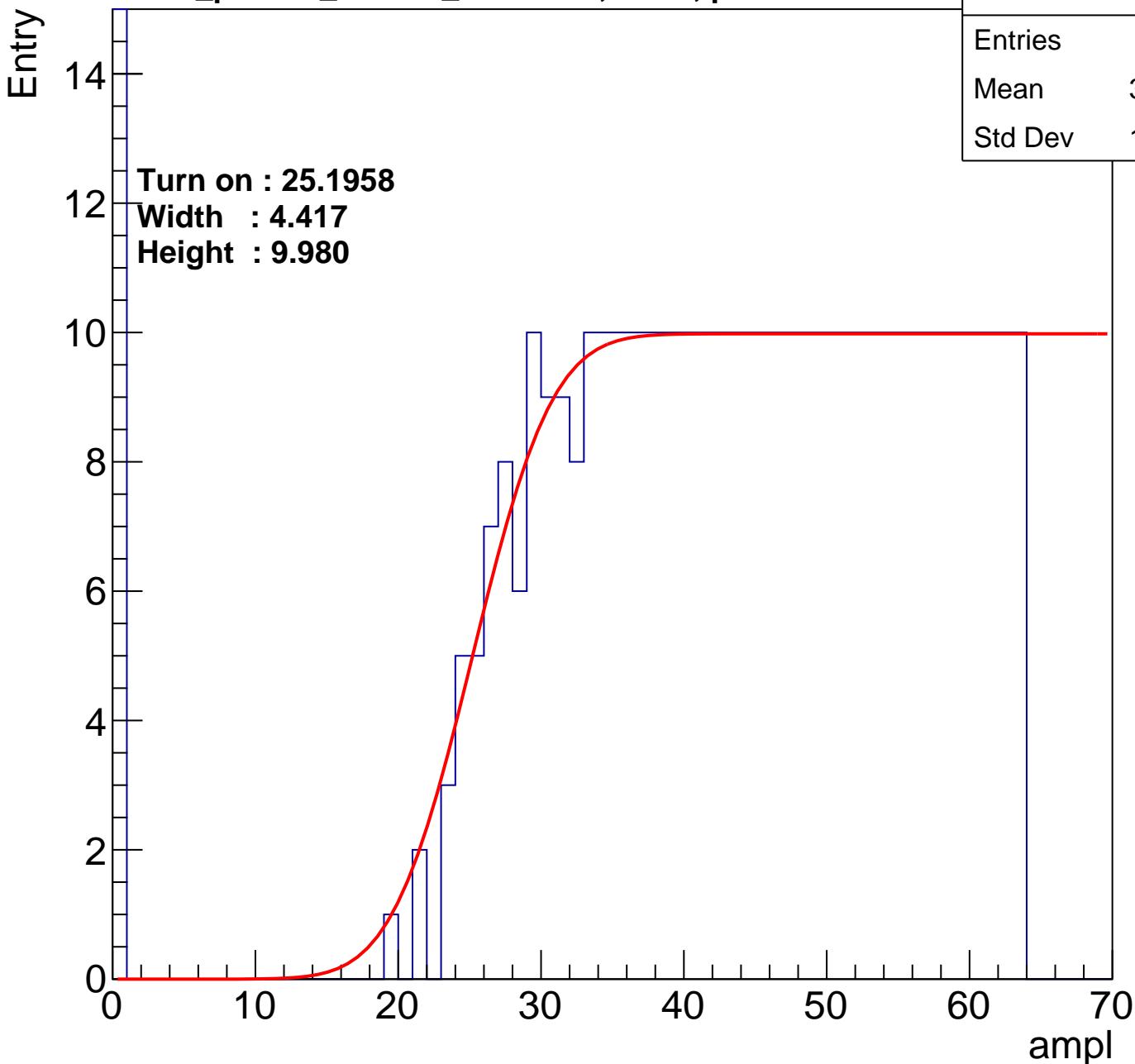
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	438
Mean	38.62
Std Dev	18.08

Turn on : 25.1958

Width : 4.417

Height : 9.980



# B1L103S, U20-ch118

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	437
Mean	39.37
Std Dev	17.04

Turn on : 24.9209

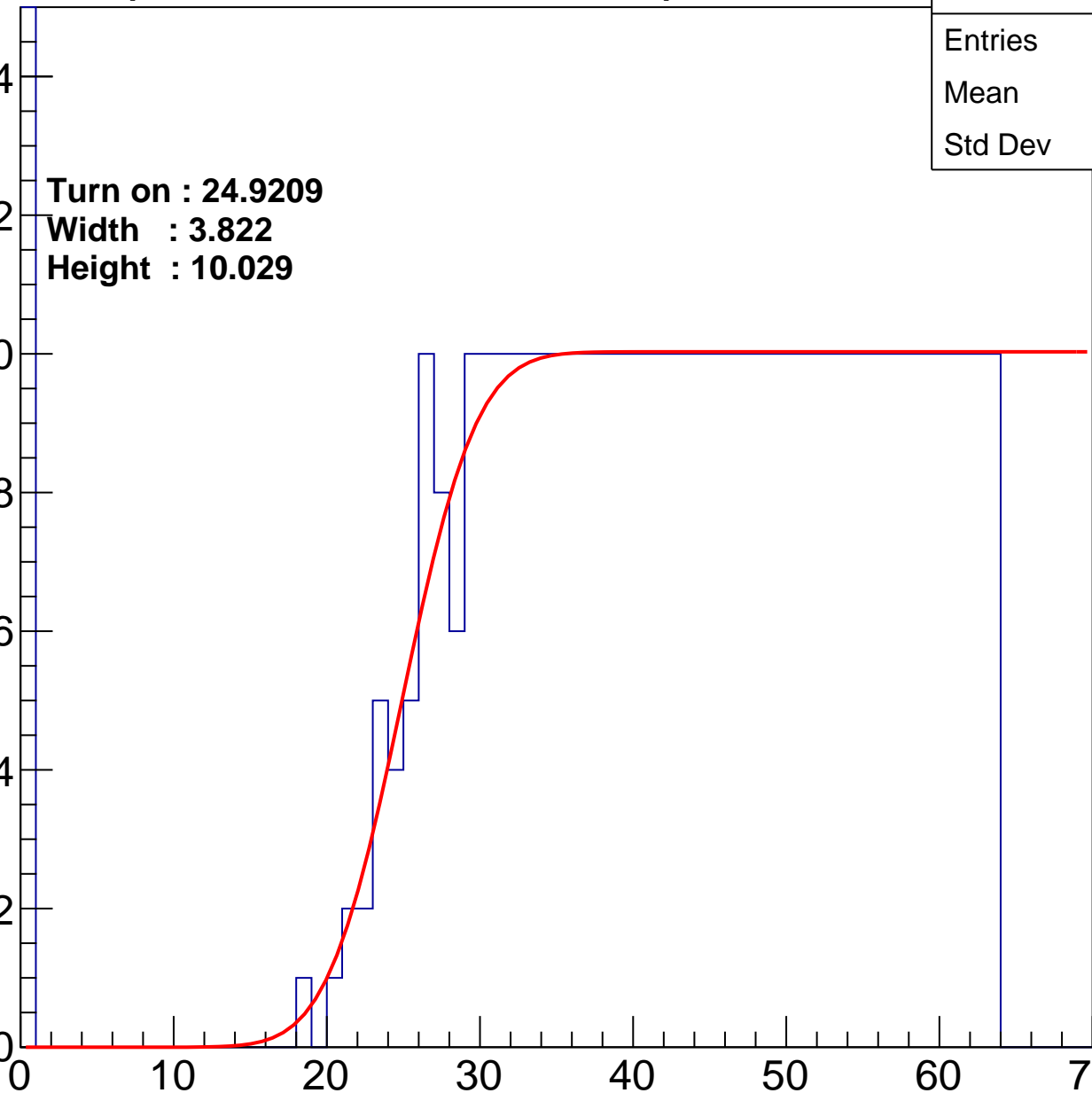
Width : 3.822

Height : 10.029

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U20-ch119

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	449
Mean	37.72
Std Dev	18.84

Turn on : 26.0488

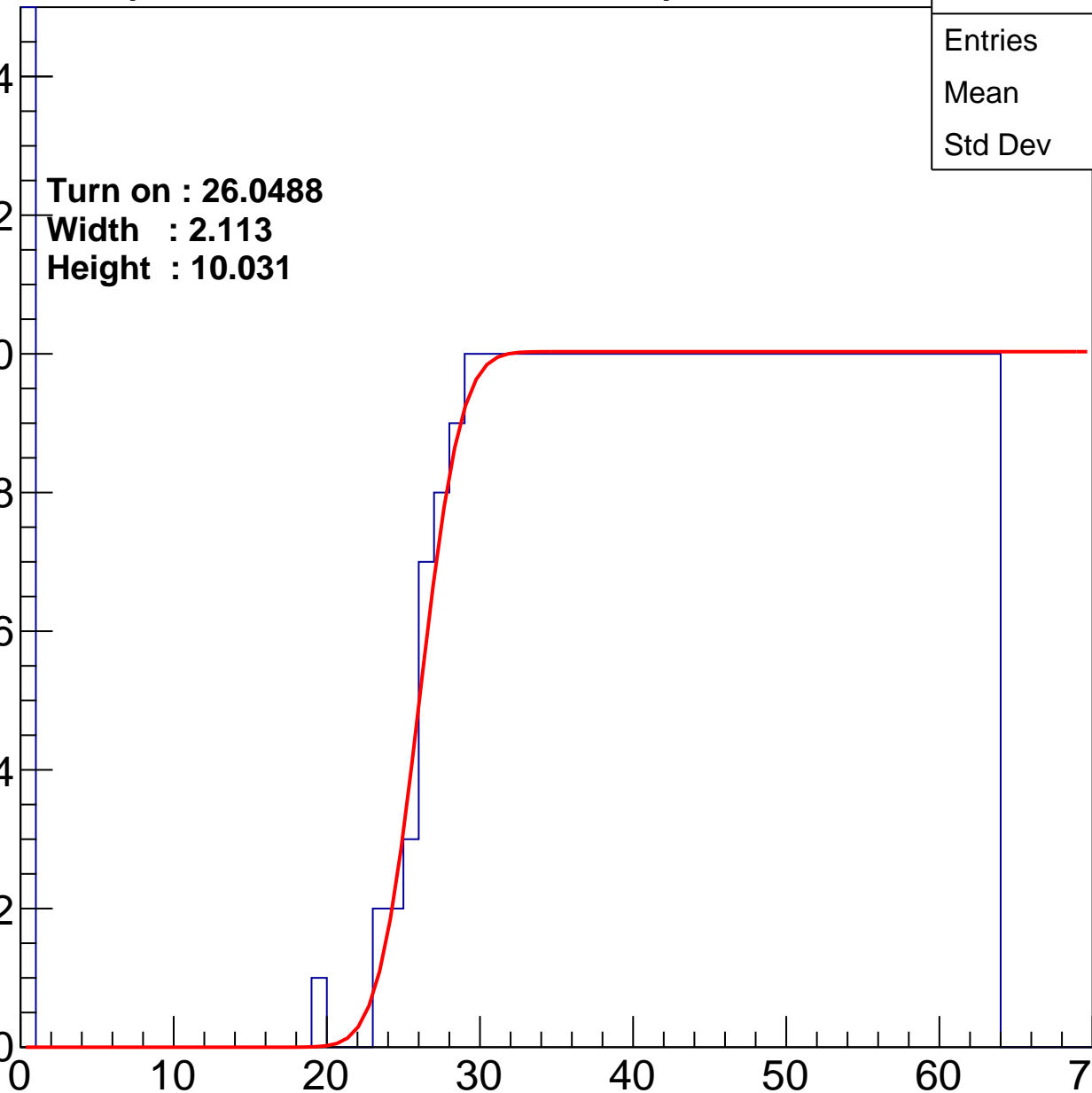
Width : 2.113

Height : 10.031

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch120

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	438
Mean	39.02
Std Dev	17.55

Turn on : 25.3717

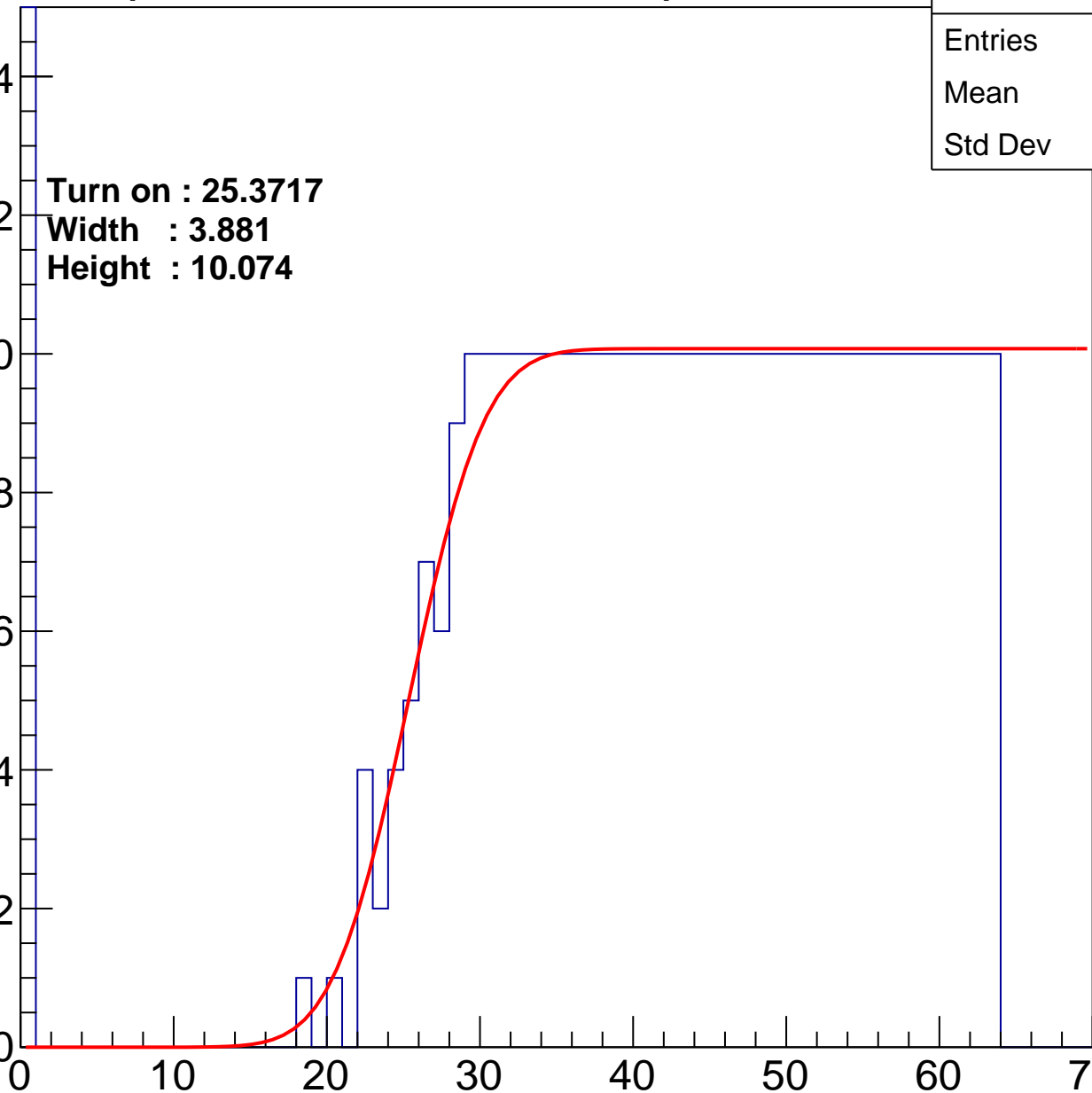
Width : 3.881

Height : 10.074

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch121

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	425
Mean	40.13
Std Dev	16.52

Turn on : 25.6111

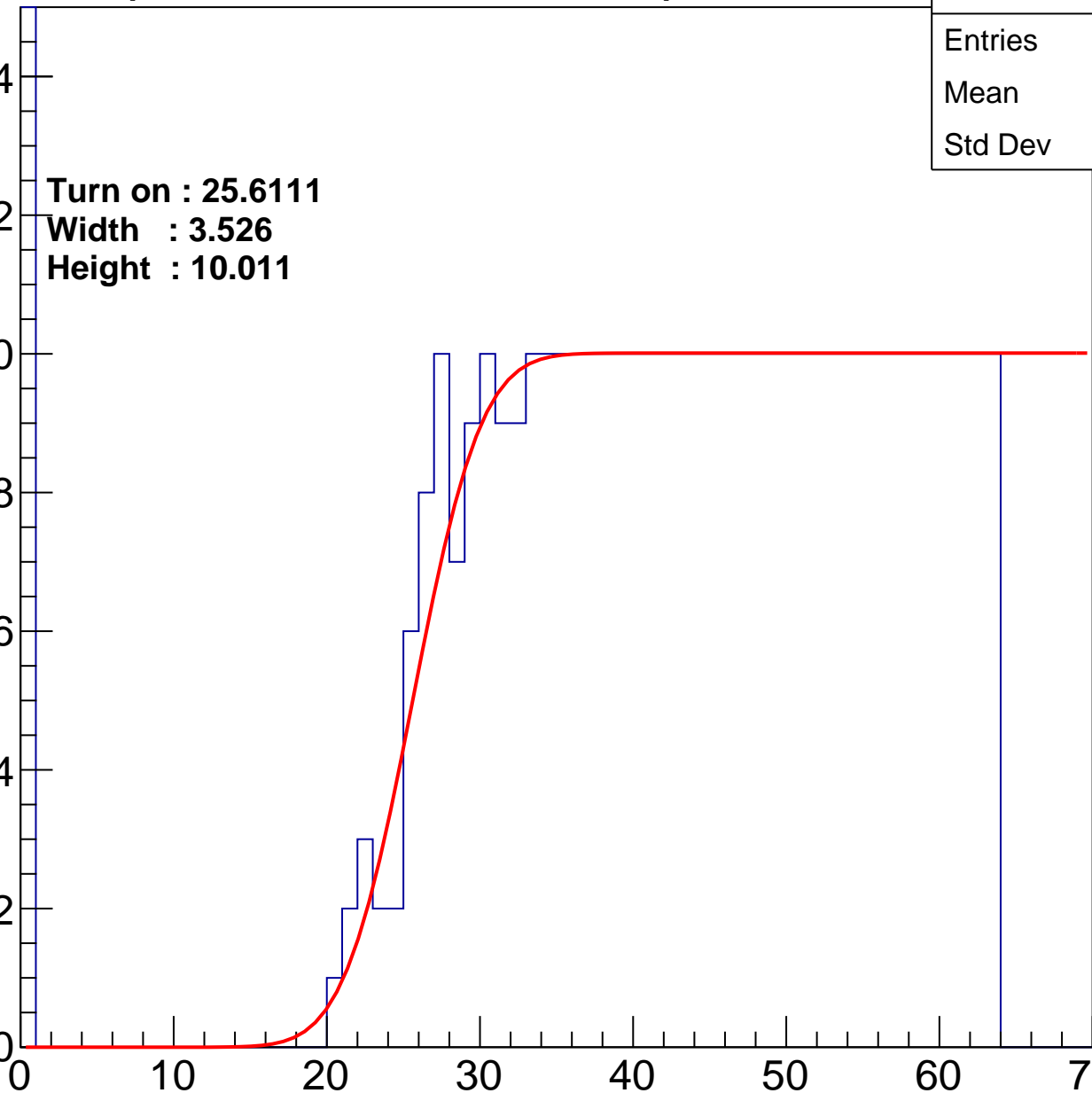
Width : 3.526

Height : 10.011

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch122

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	435
Mean	39.12
Std Dev	17.59

Turn on : 25.7855

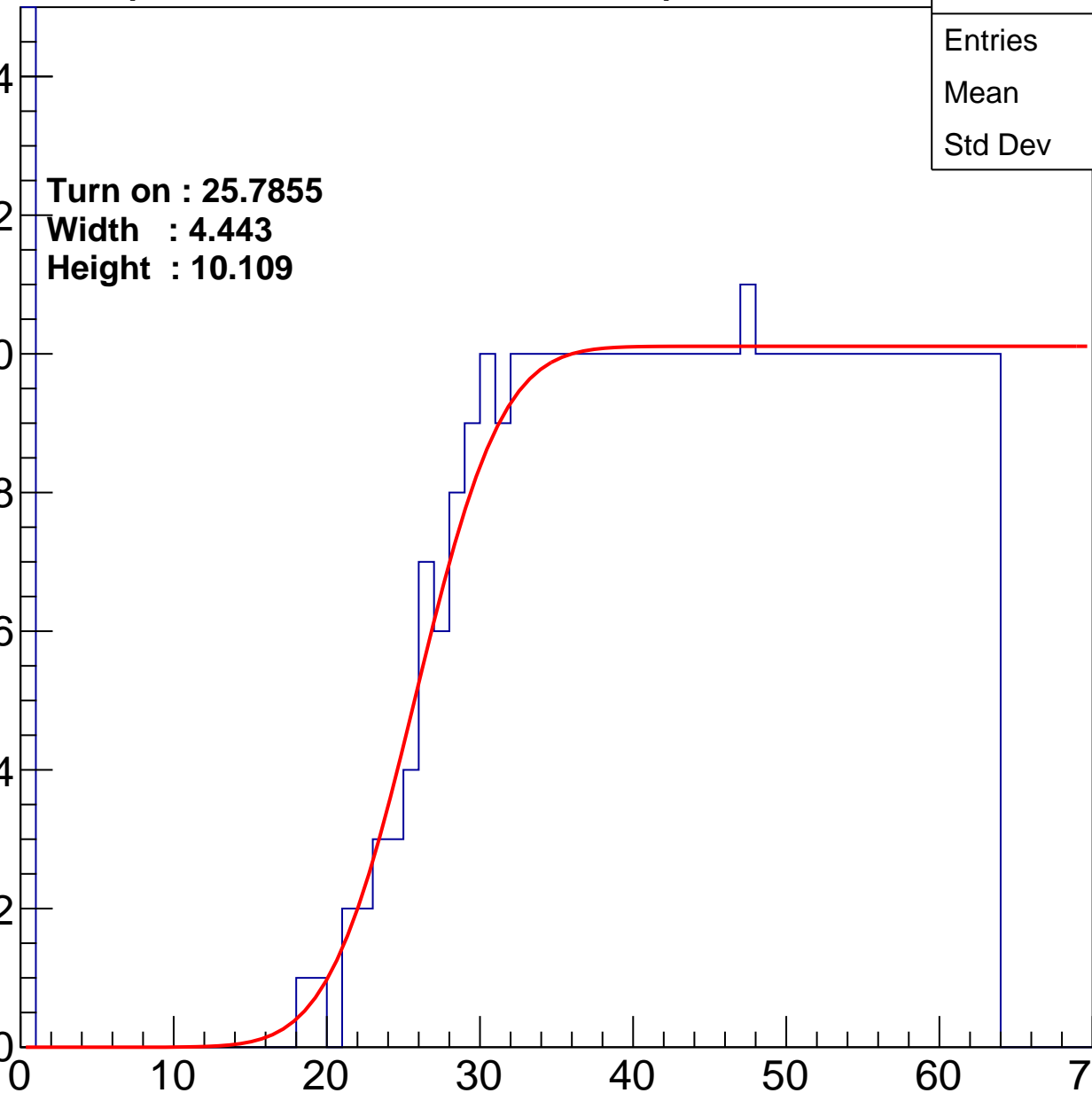
Width : 4.443

Height : 10.109

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch123

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	438
Mean	38.85
Std Dev	17.79

Turn on : 25.8753

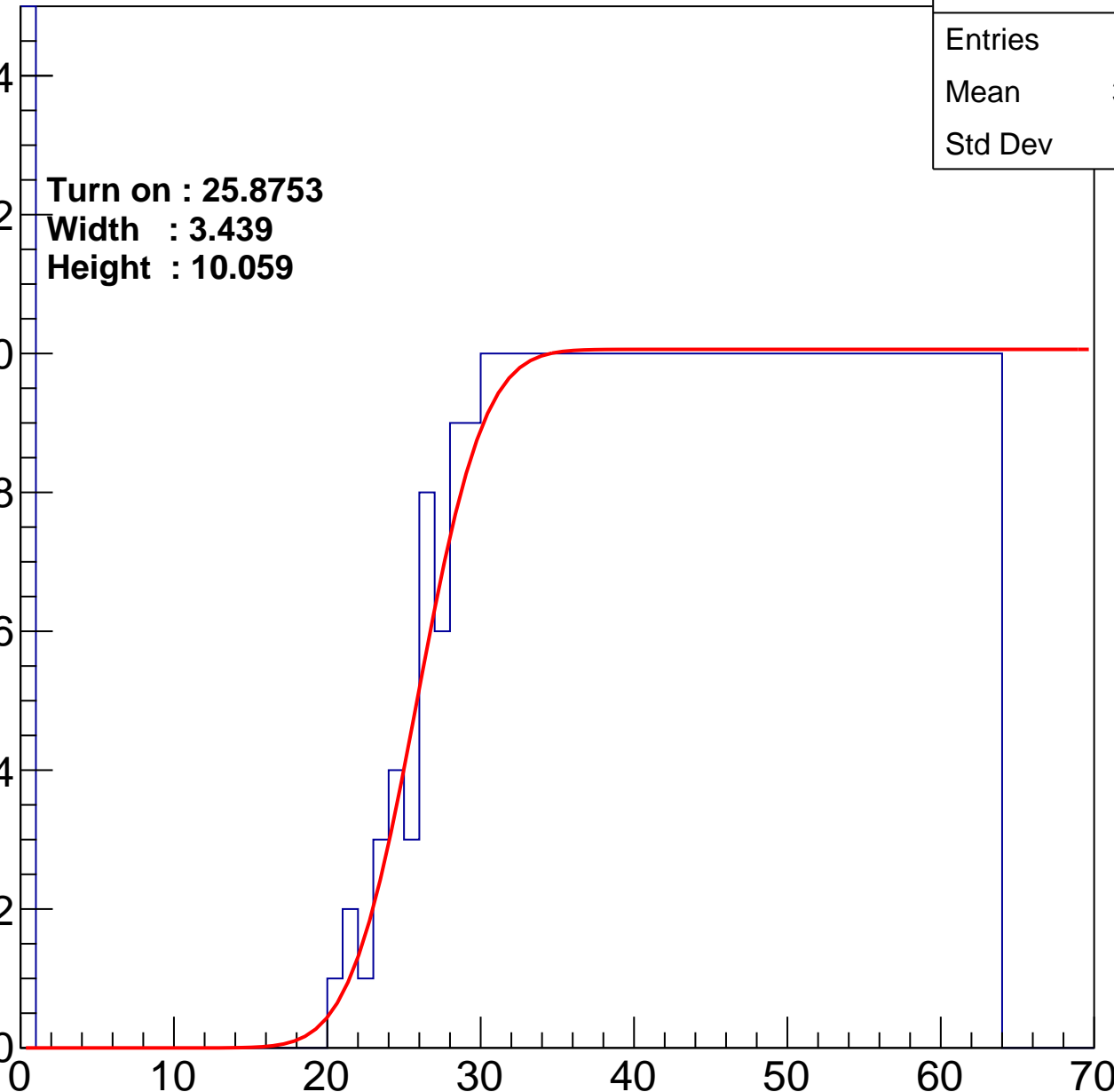
Width : 3.439

Height : 10.059

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch124

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	475
Mean	37.12
Std Dev	18.36

Turn on : 22.9575

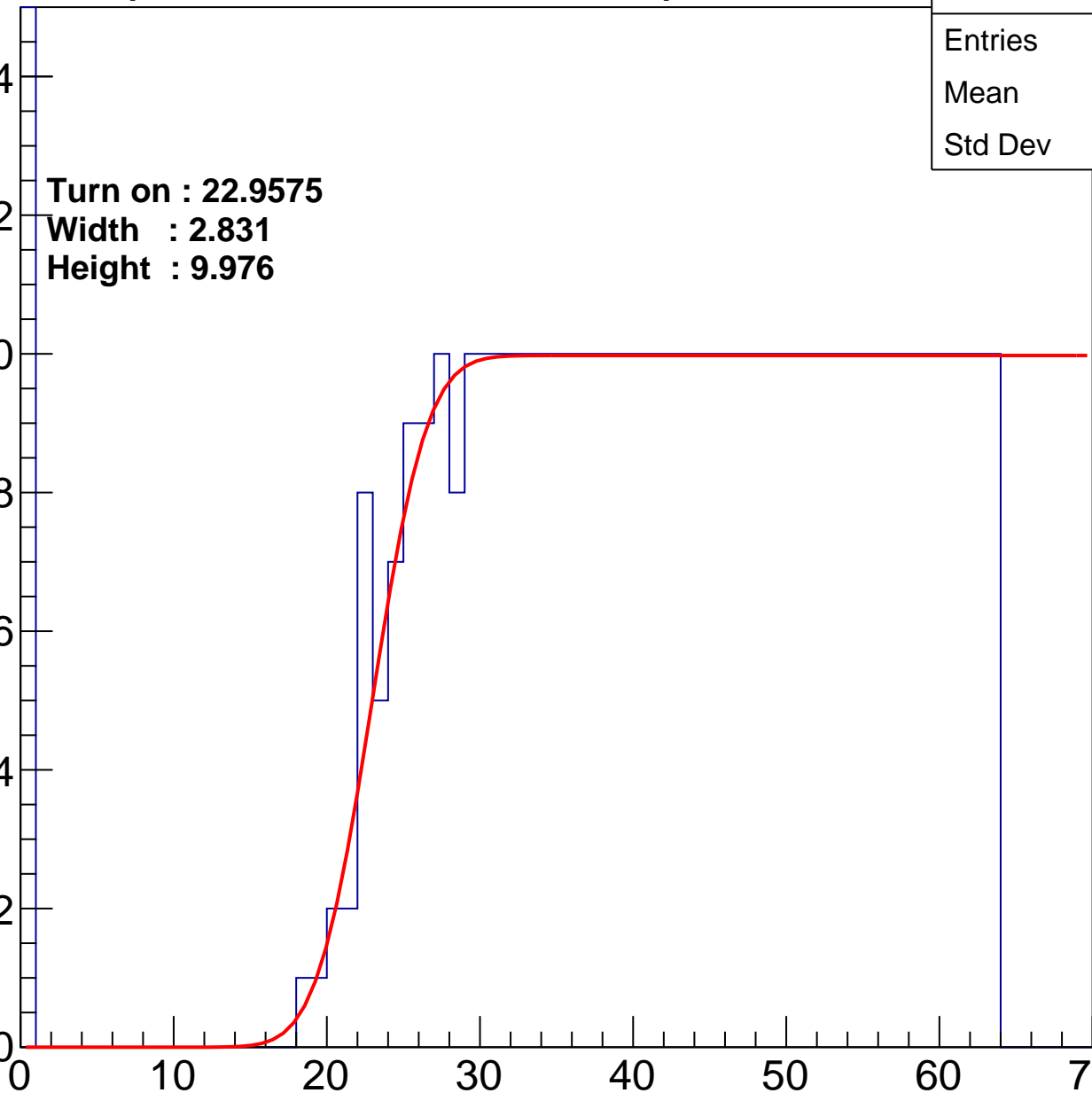
Width : 2.831

Height : 9.976

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch125

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	438
Mean	39.44
Std Dev	16.91

Turn on : 24.2451

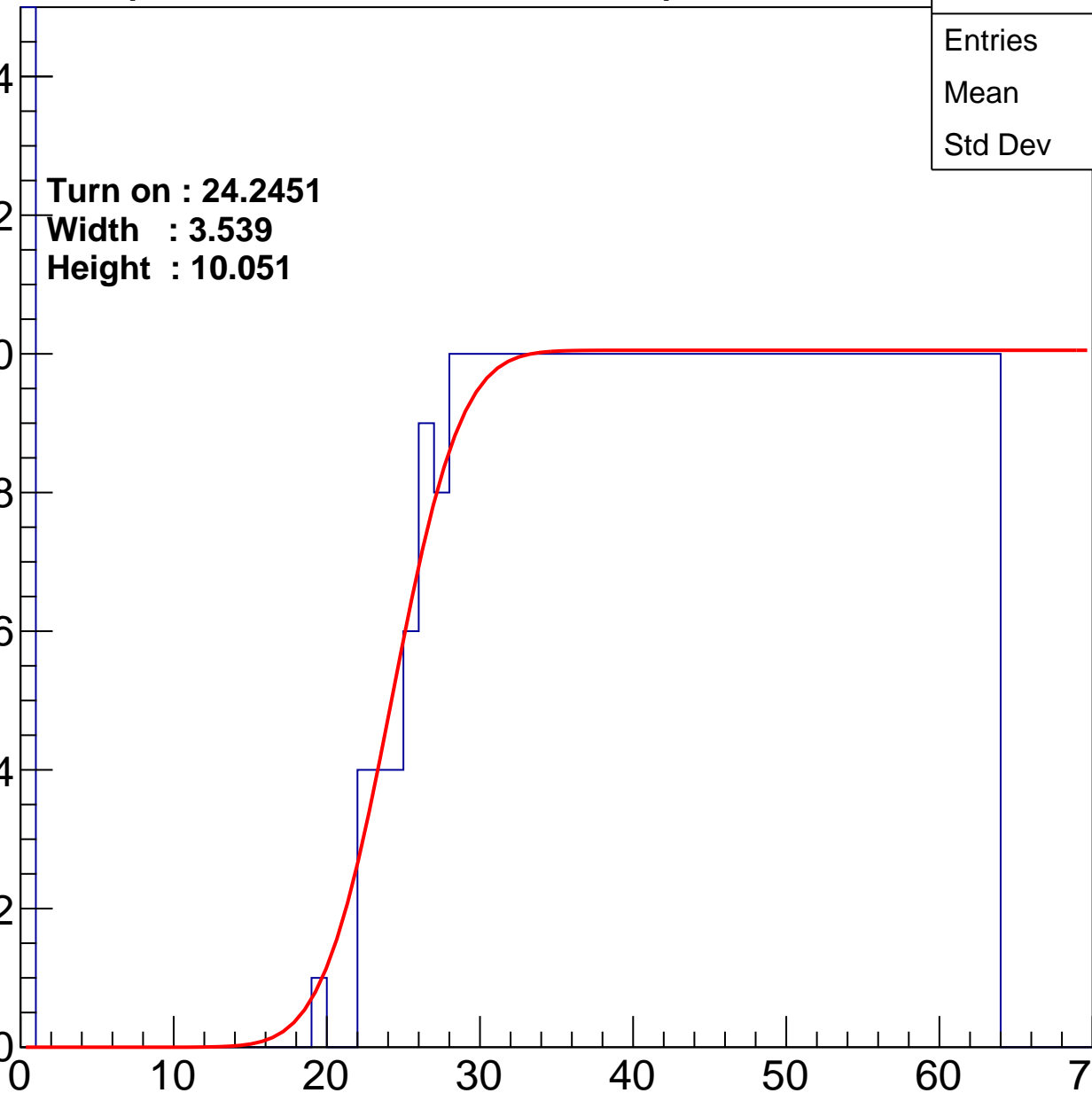
Width : 3.539

Height : 10.051

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch126

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	475
Mean	37.53
Std Dev	17.74

Turn on : 22.5872

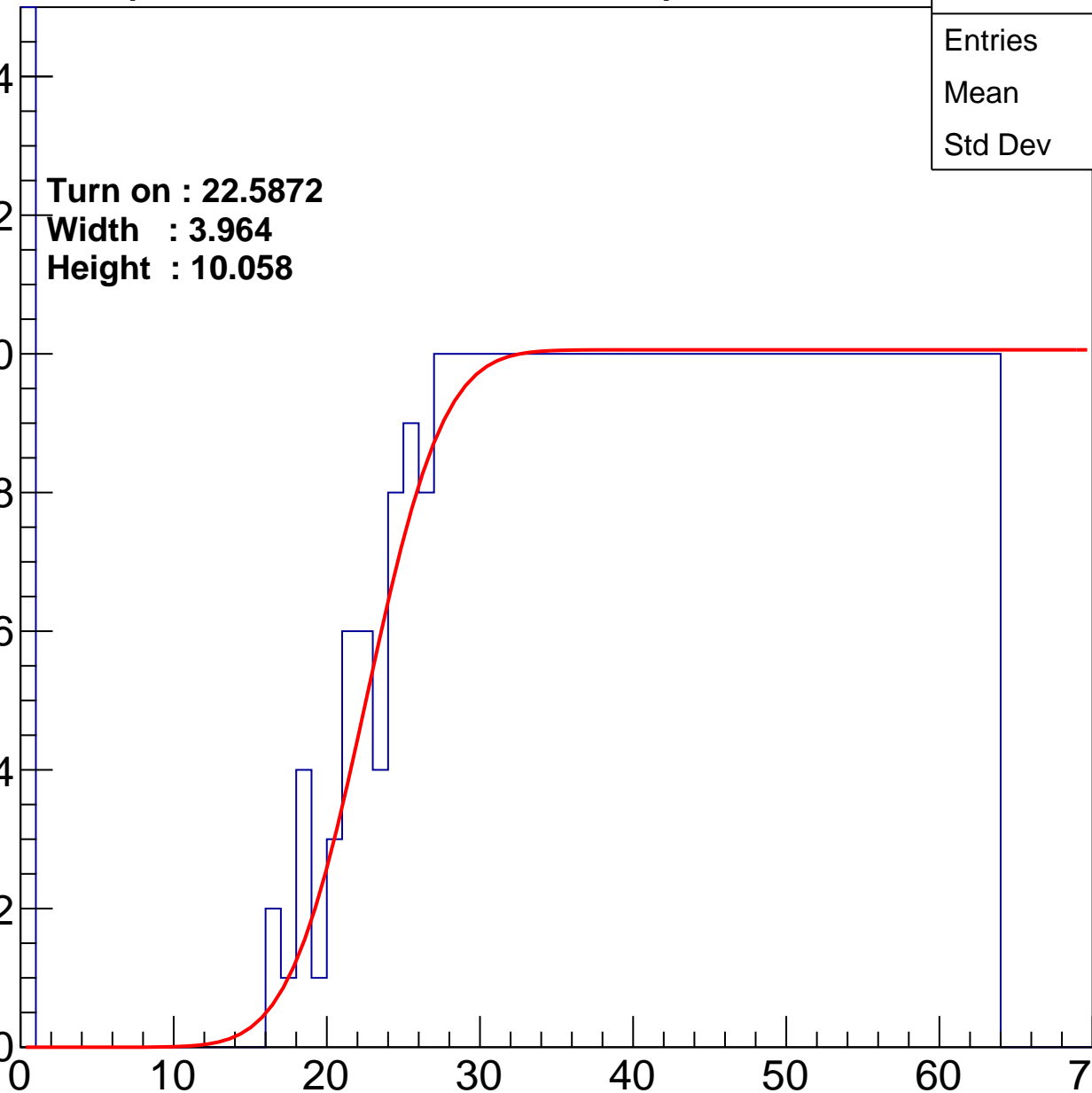
Width : 3.964

Height : 10.058

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U20-ch127

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	479
Mean	36.45
Std Dev	19.05

**Turn on : 23.7290**

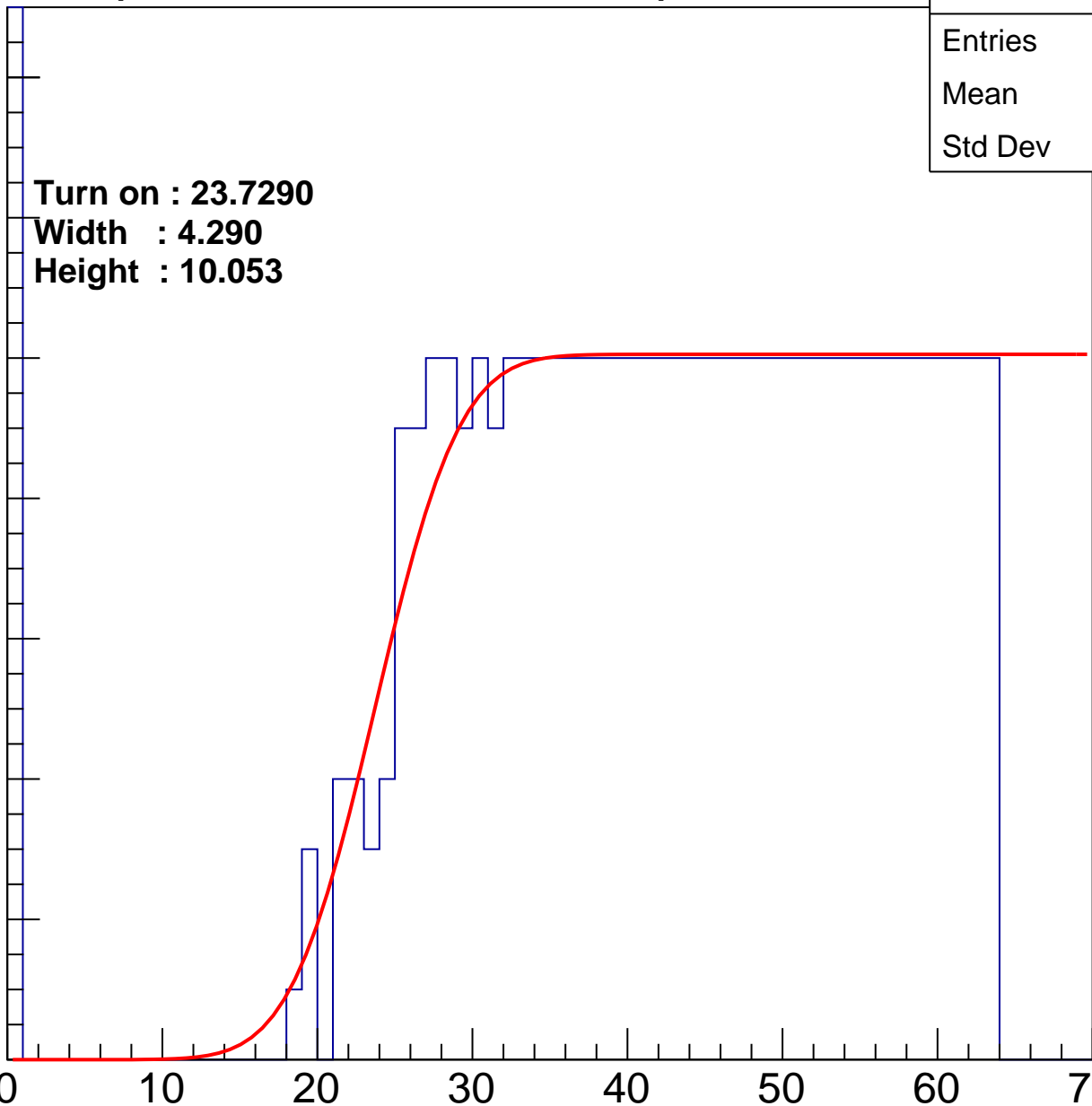
**Width : 4.290**

**Height : 10.053**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U20-ch127

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	479
Mean	36.45
Std Dev	19.05

**Turn on : 23.7290**

**Width : 4.290**

**Height : 10.053**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

