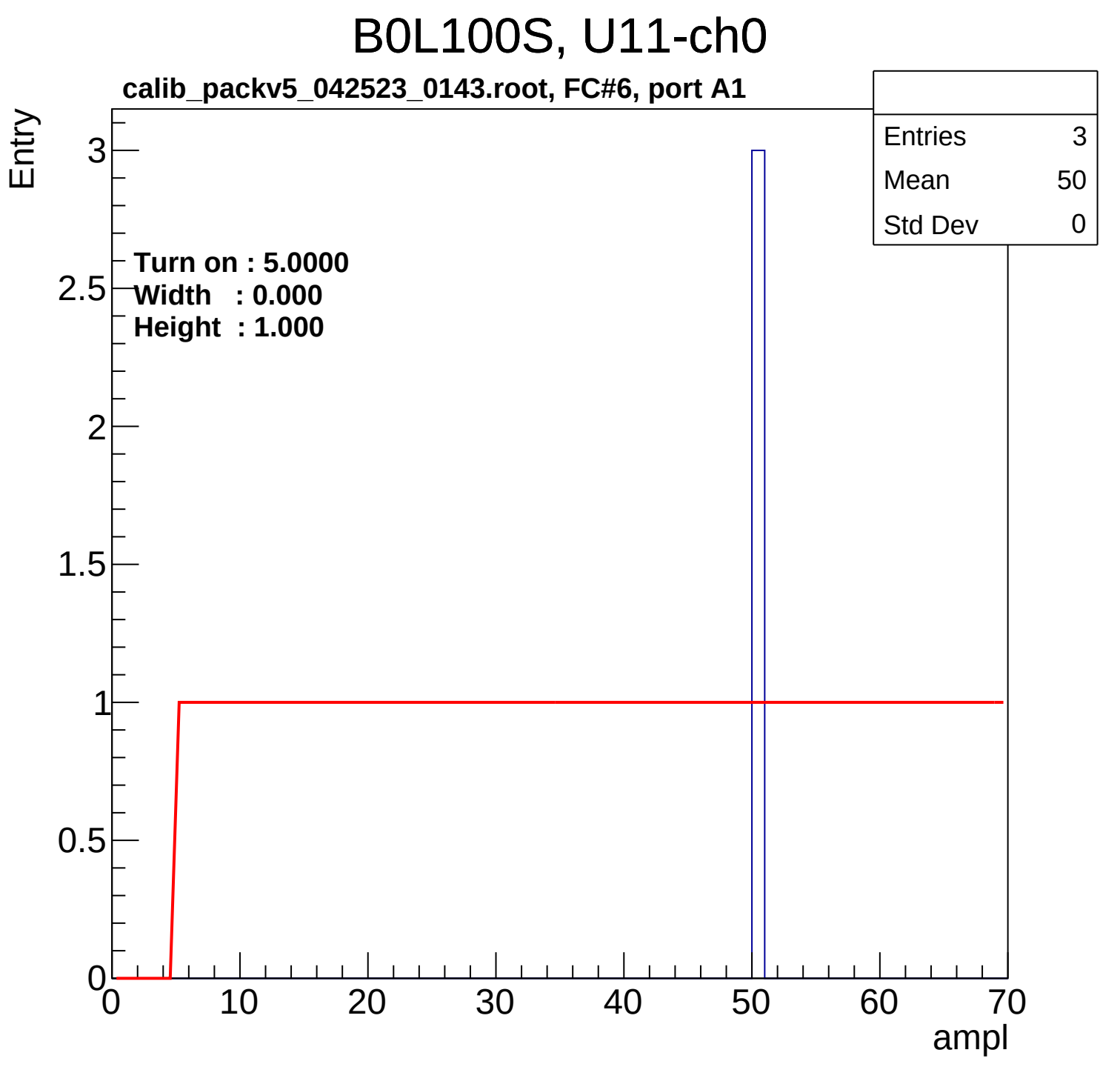
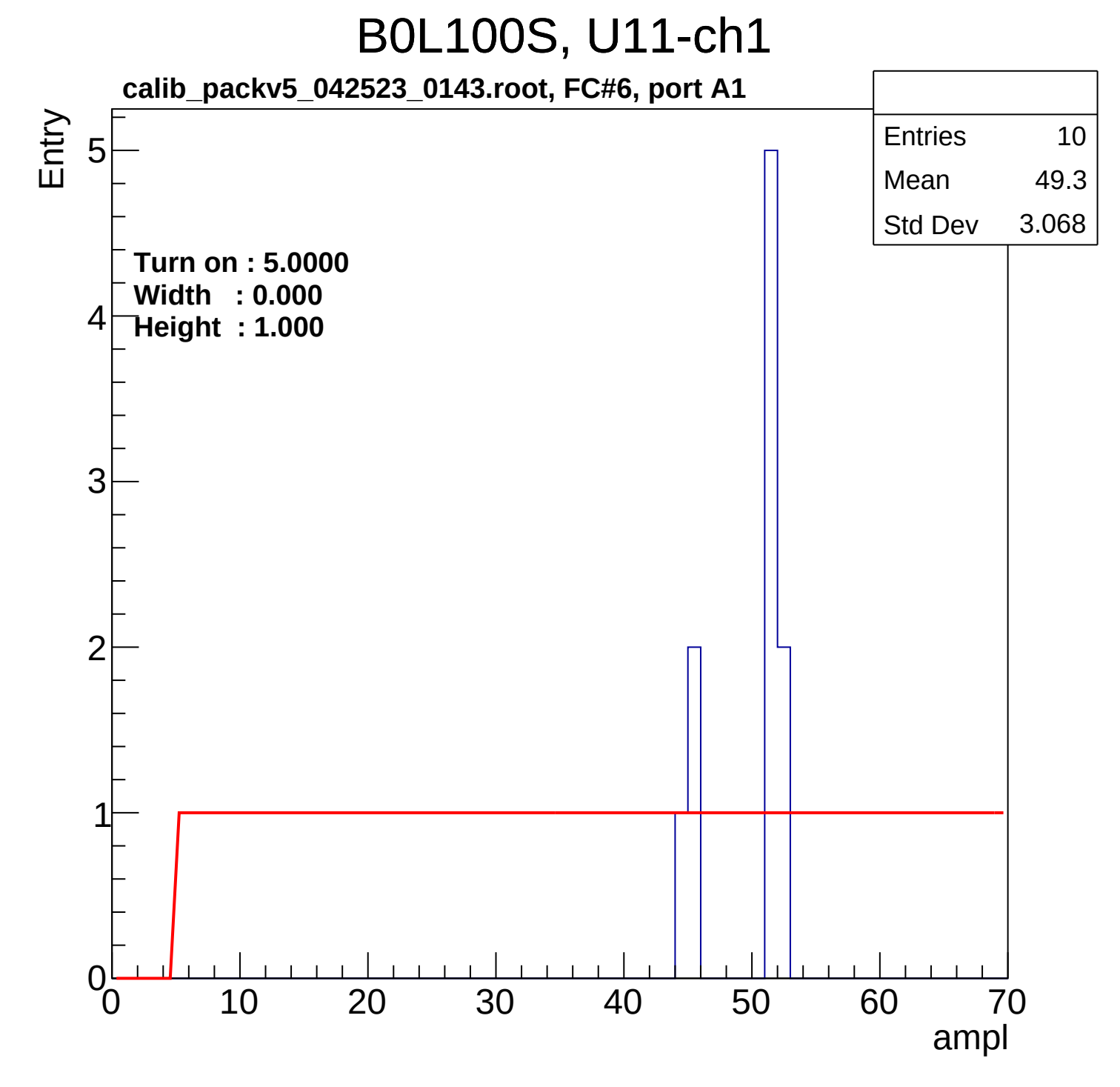

B0L100S, U11-ch0
calib_packv5_042523_0143.root, FC#6, port A1
Entries 3
Mean 50
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B0L100S, U11-ch1
calib_packv5_042523_0143.root, FC#6, port A1
Entries 10
Mean 49.3
Std Dev 3.068
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
10
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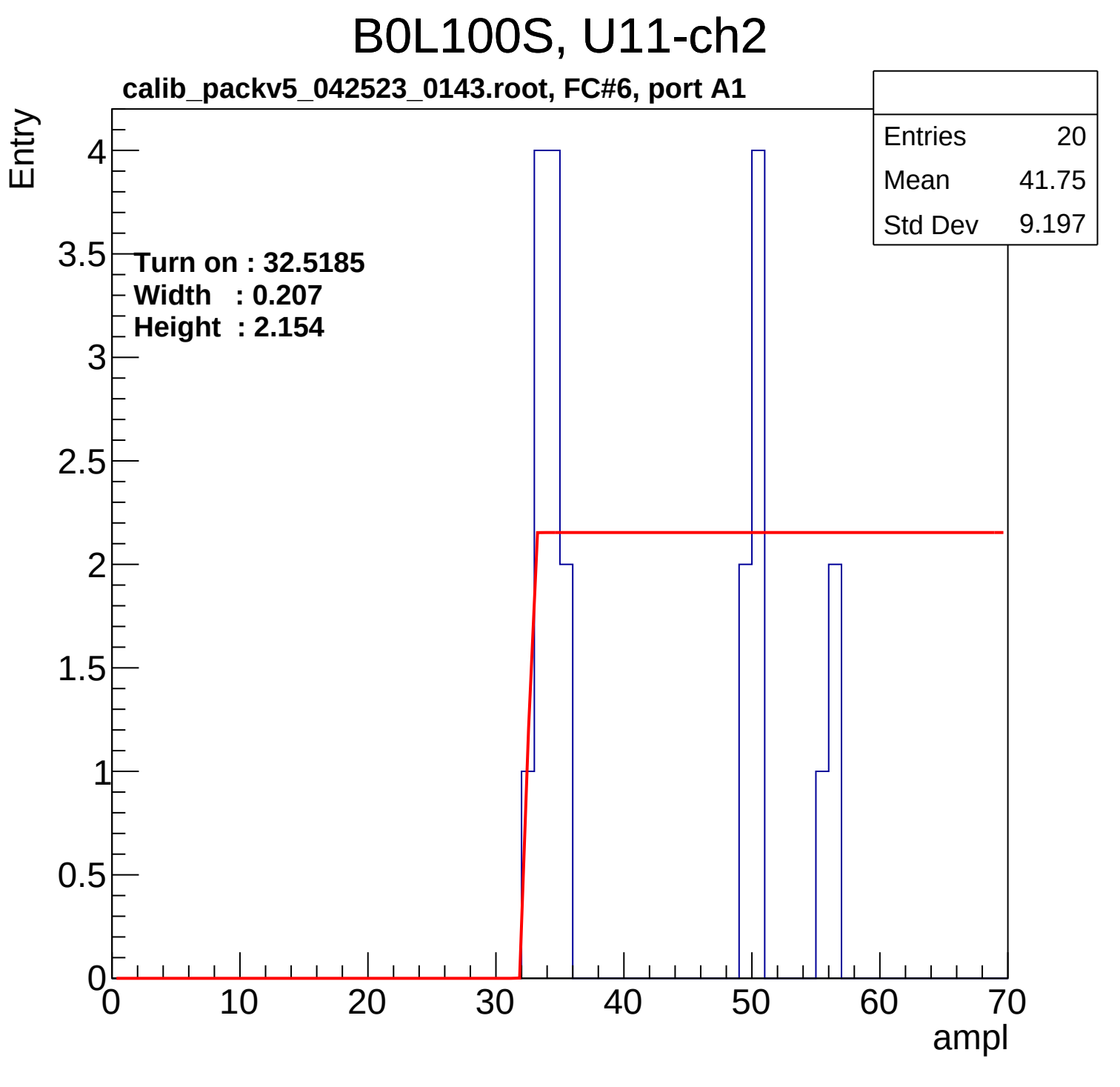
30
40
50
60
70


B0L100S, U11-ch2
calib_packv5_042523_0143.root, FC#6, port A1
Entries 20
Mean 41.75
Std Dev 9.197
Turn on : 32.5185
Width : 0.207
Height : 2.154
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
50
60
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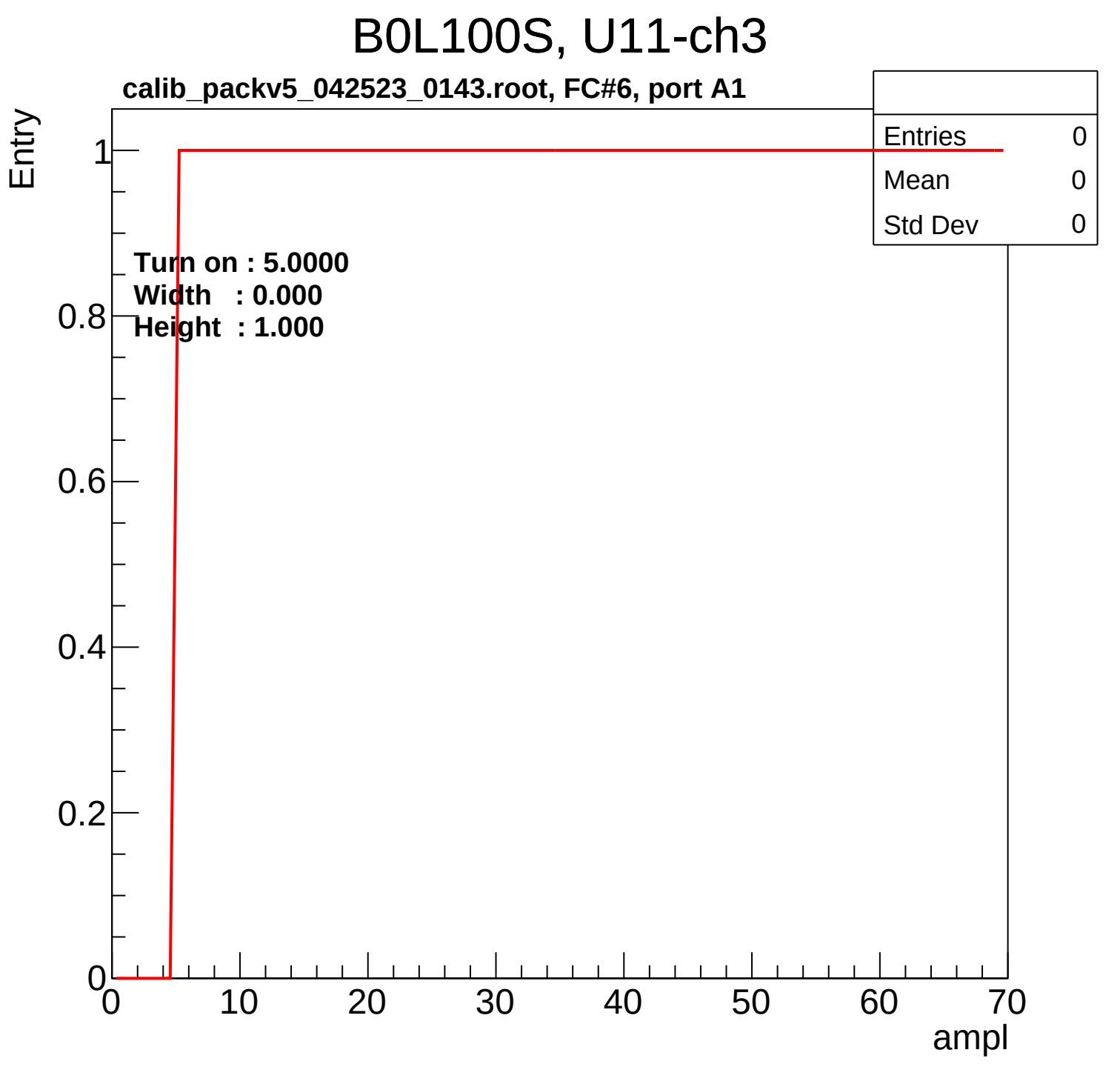
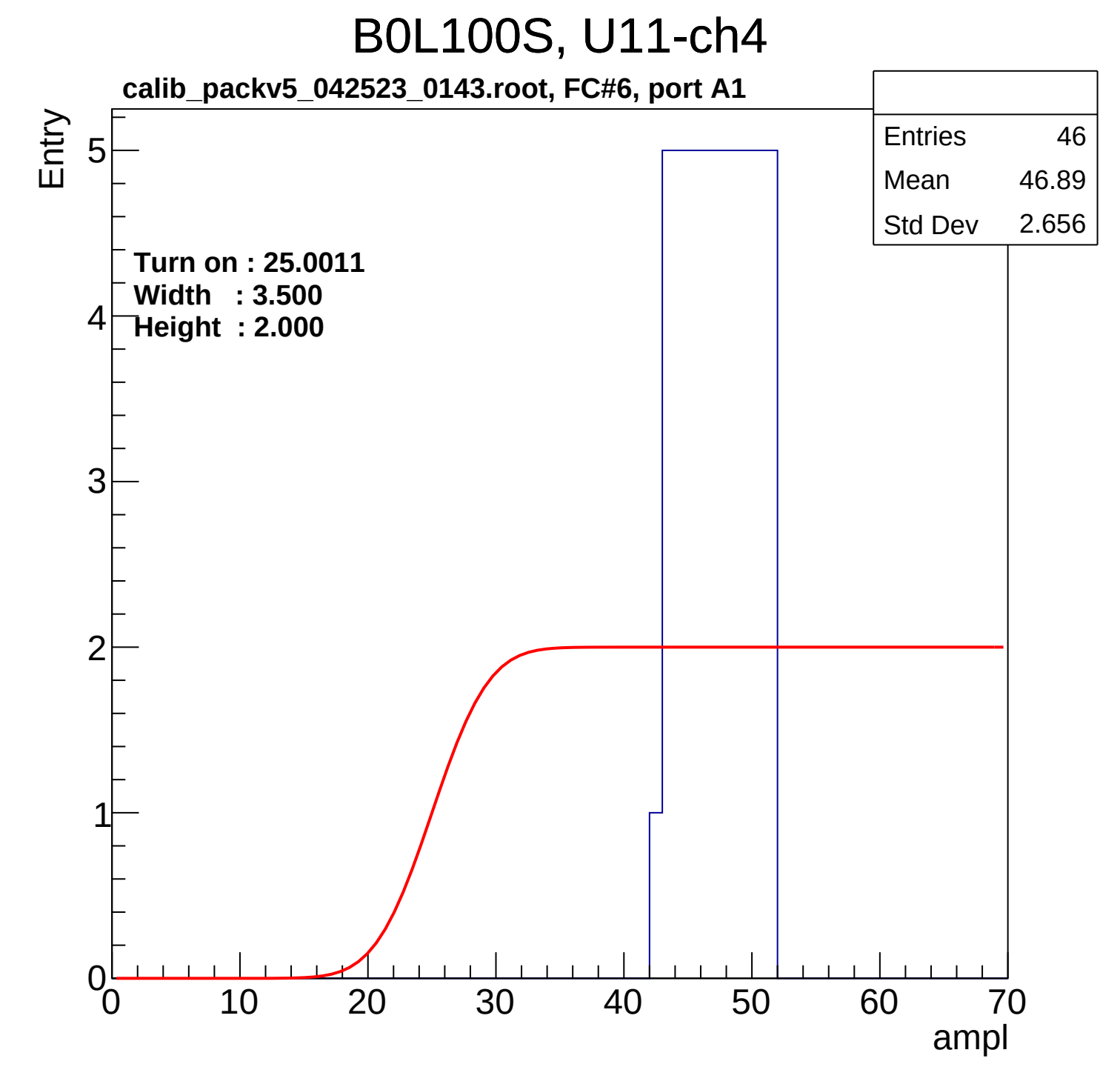
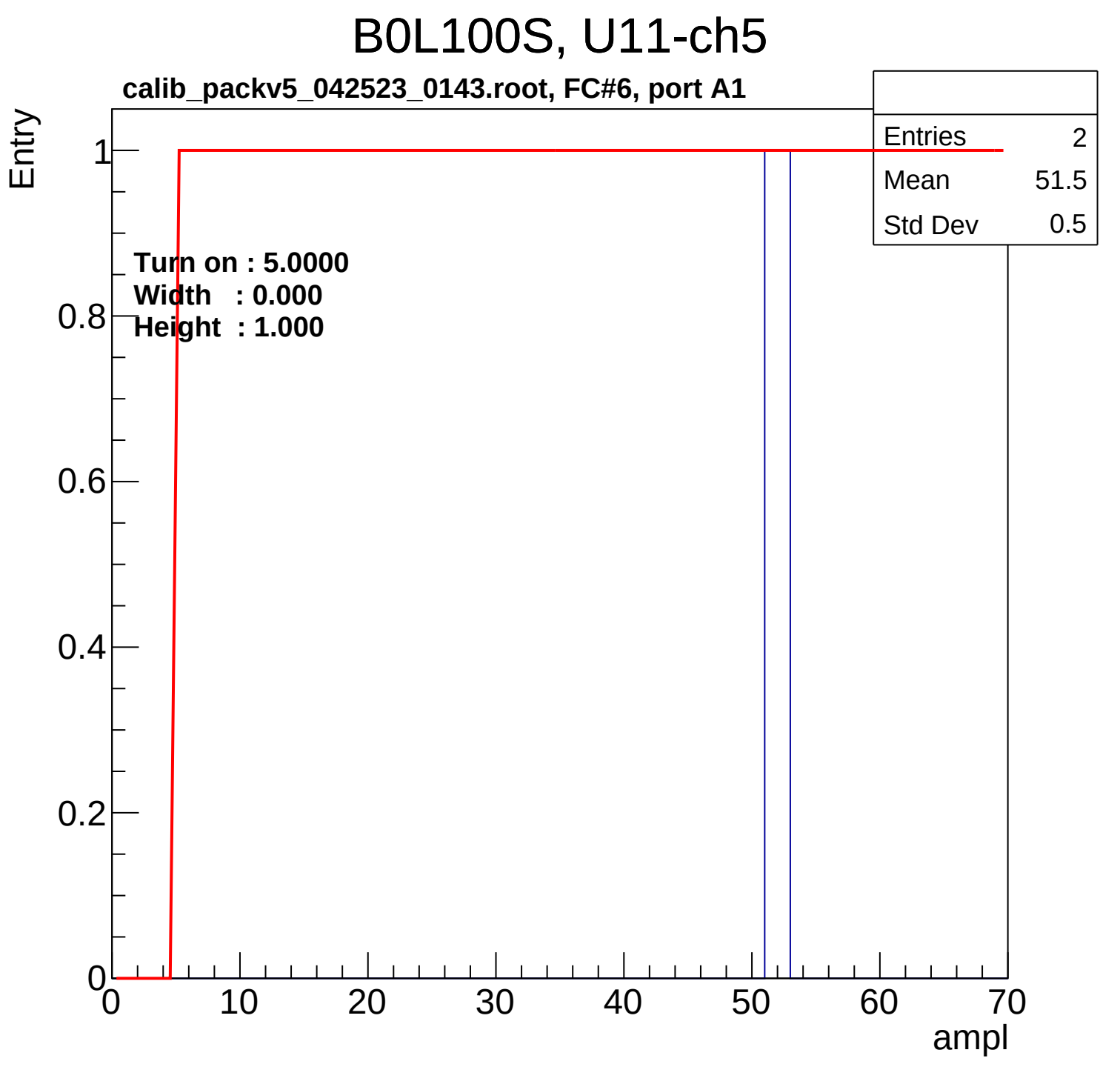
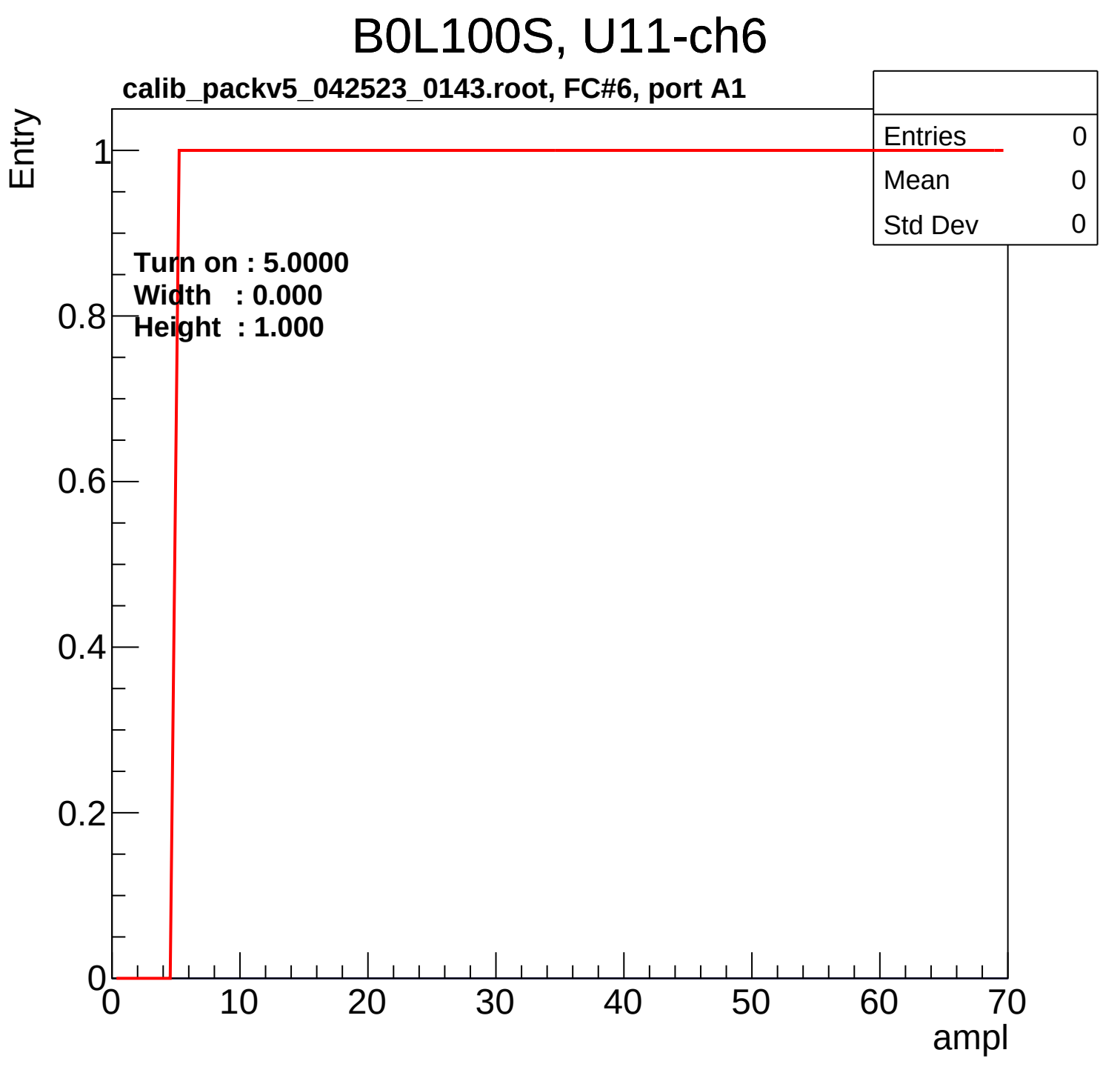
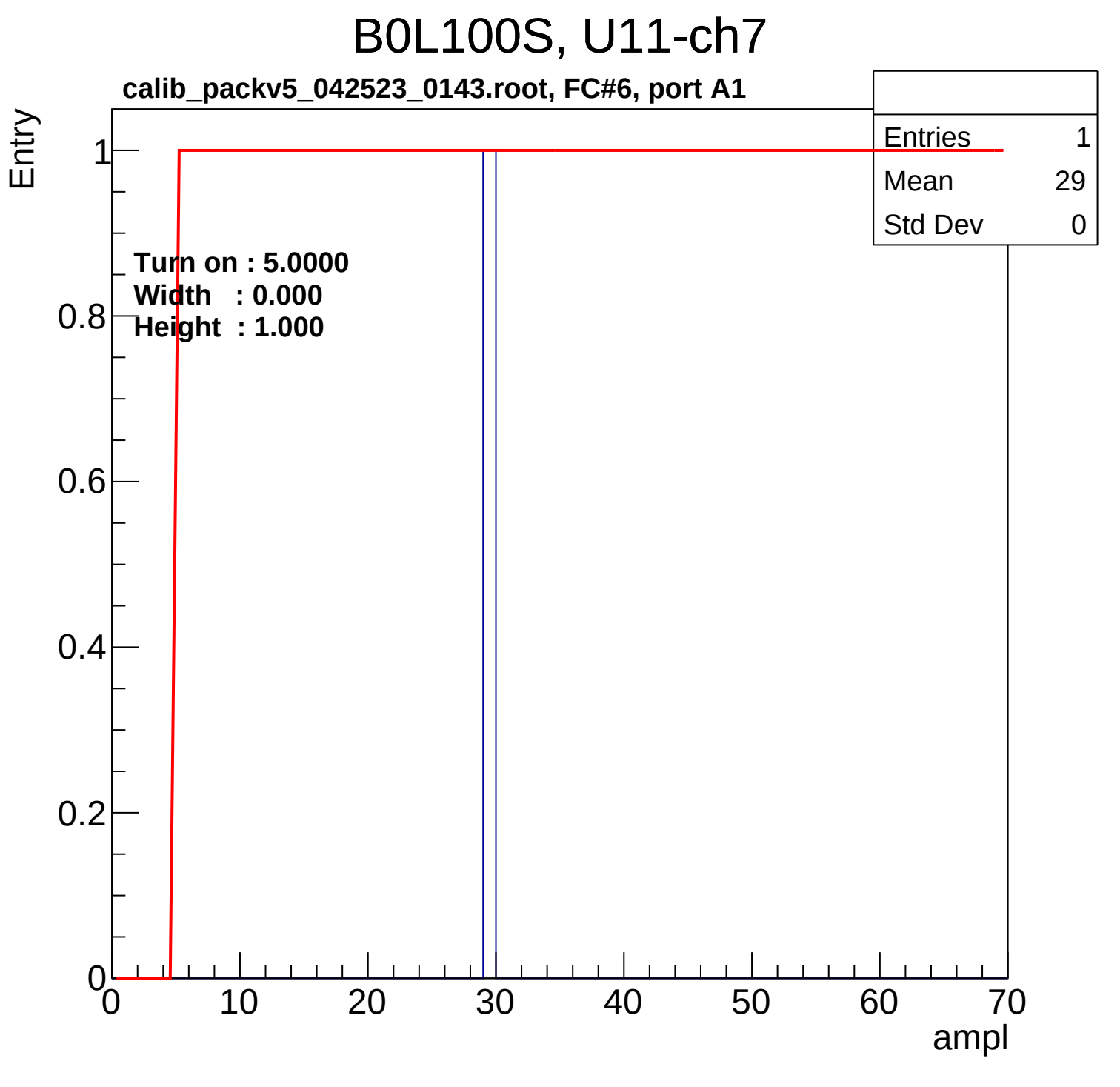
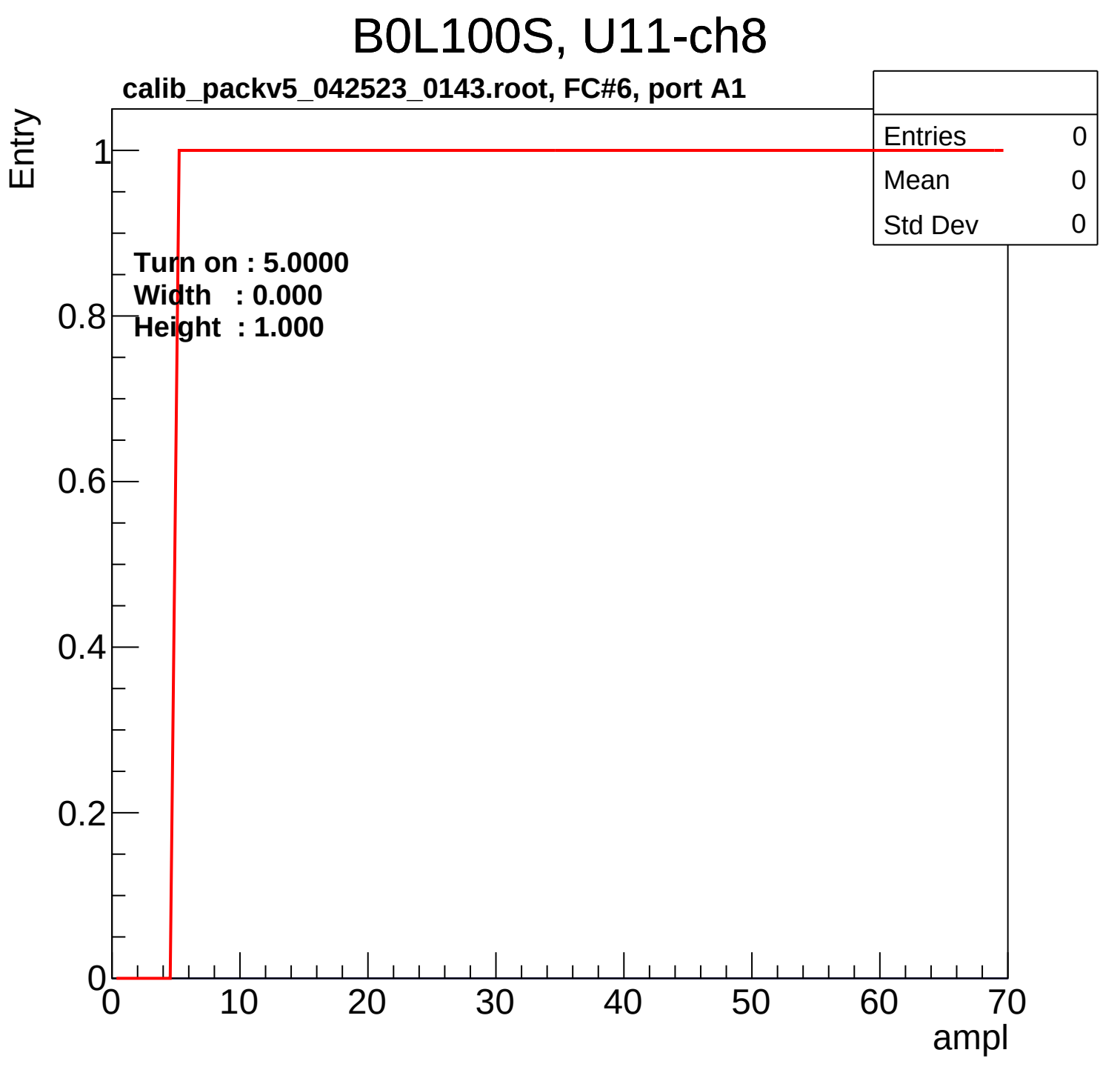

B0L100S, U11-ch3
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

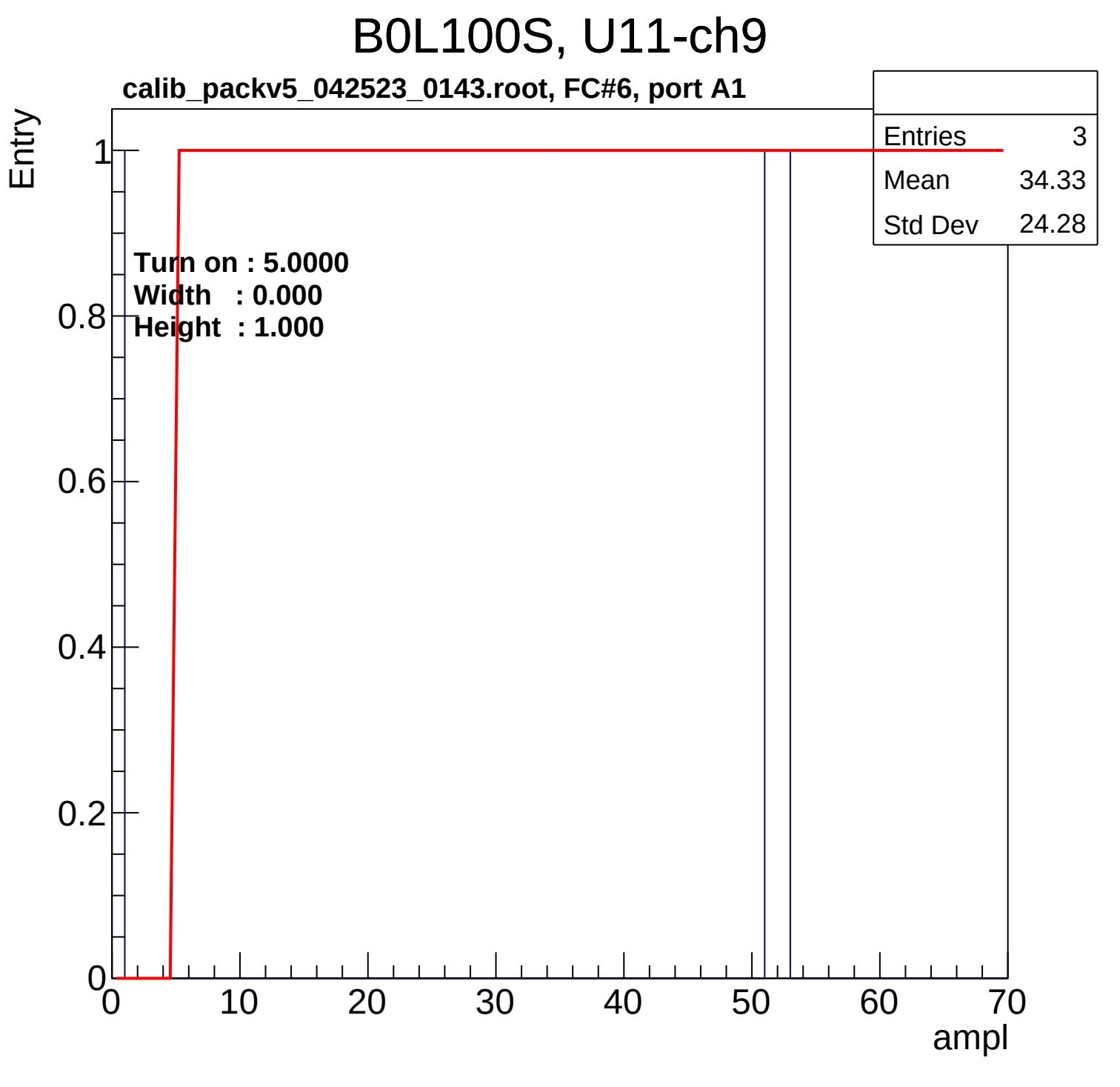

B0L100S, U11-ch4
calib_packv5_042523_0143.root, FC#6, port A1
Entries 46
Mean 46.89
Std Dev 2.656
Turn on : 25.0011
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

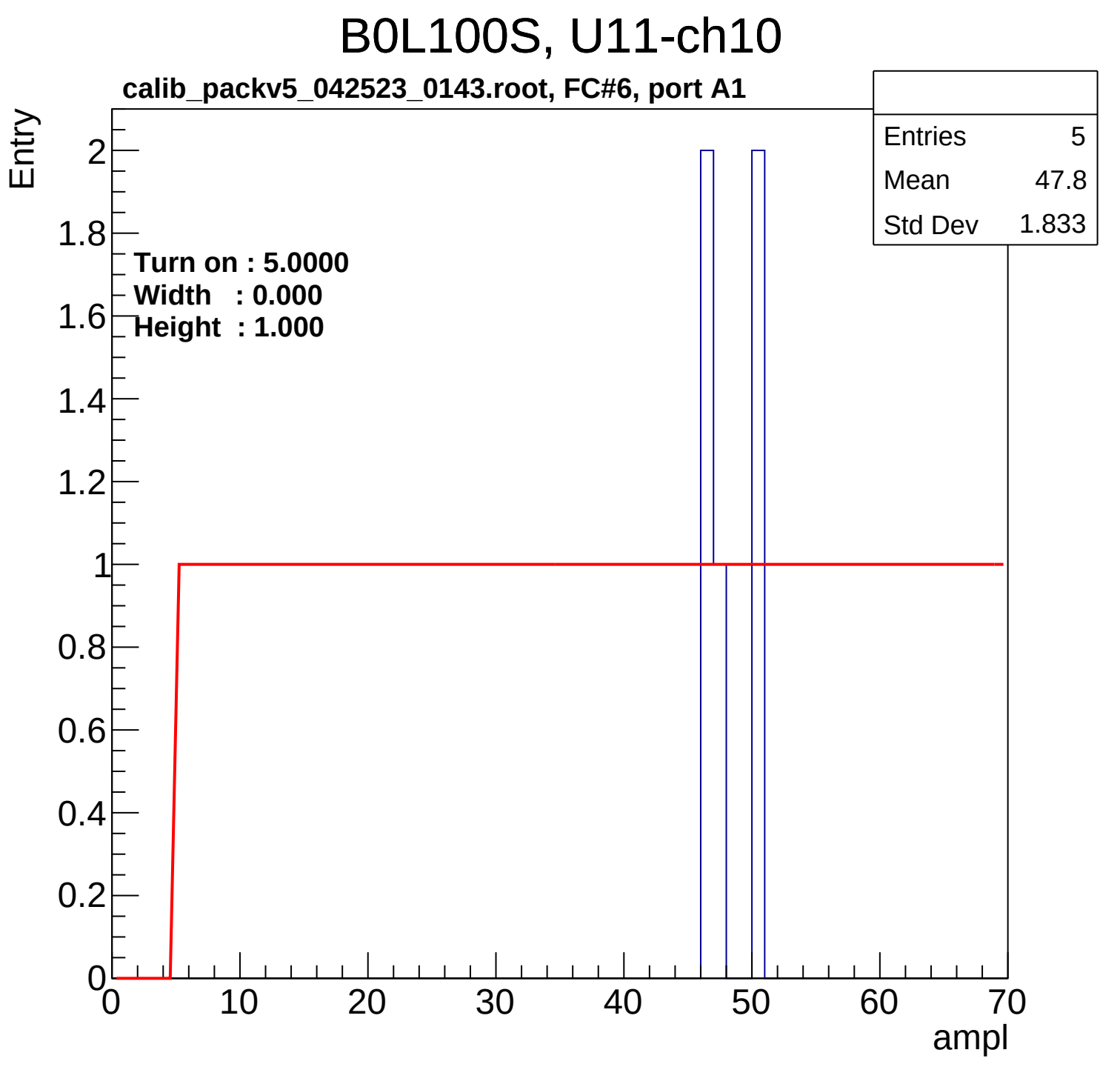

B0L100S, U11-ch5
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 51.5
Std Dev 0.5
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

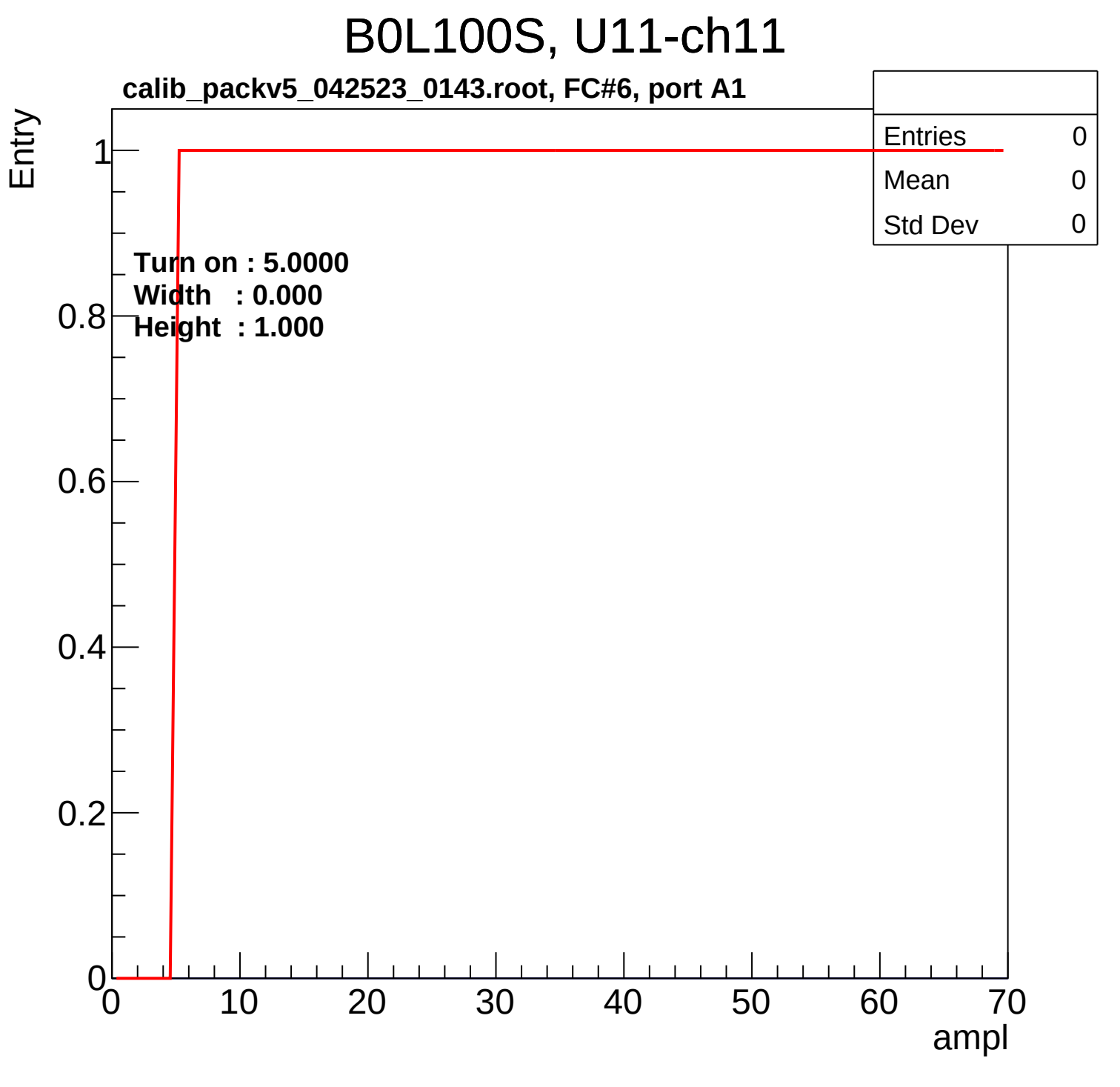

B0L100S, U11-ch6
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

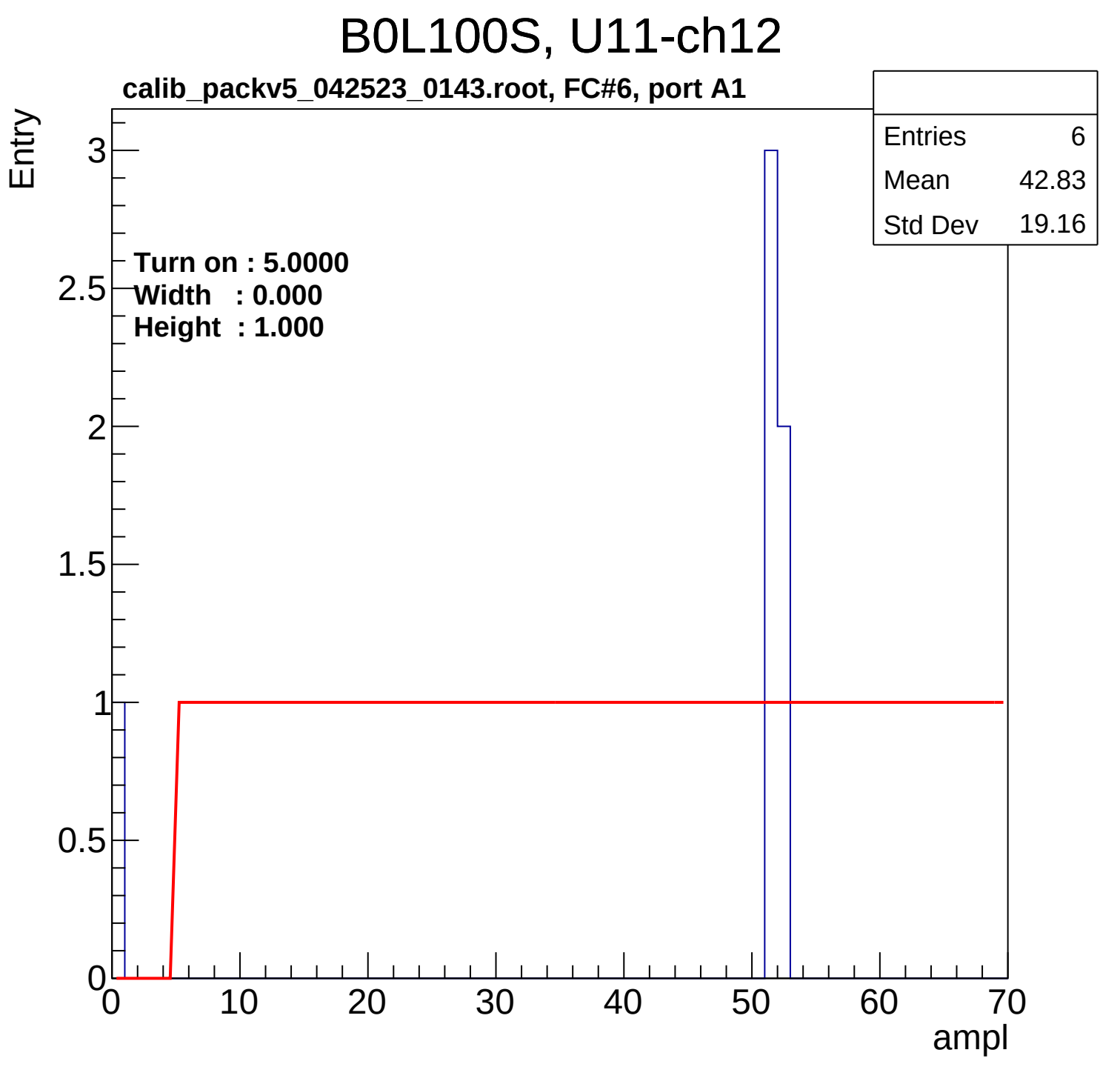

B0L100S, U11-ch7
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 29
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

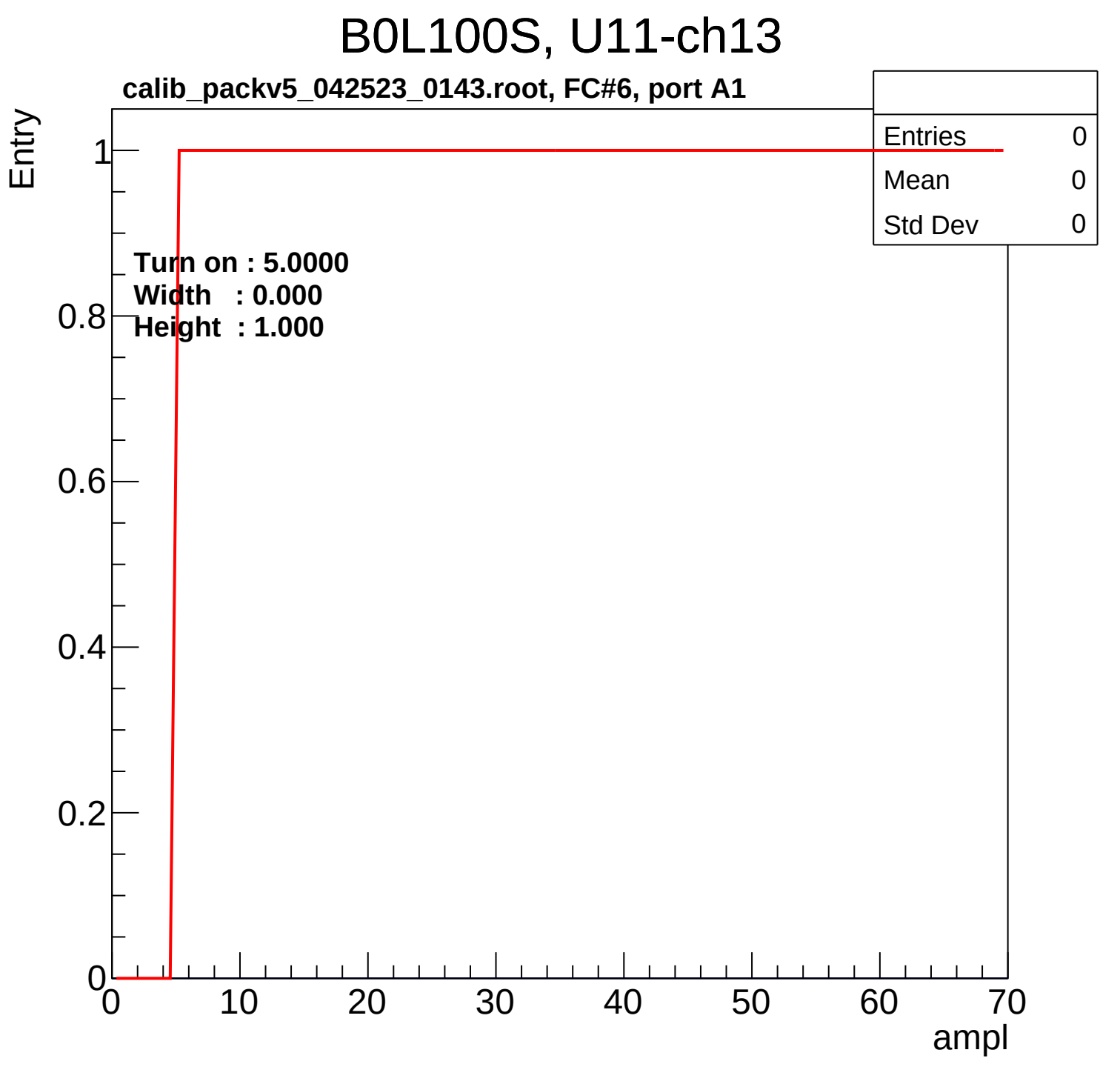

B0L100S, U11-ch8
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

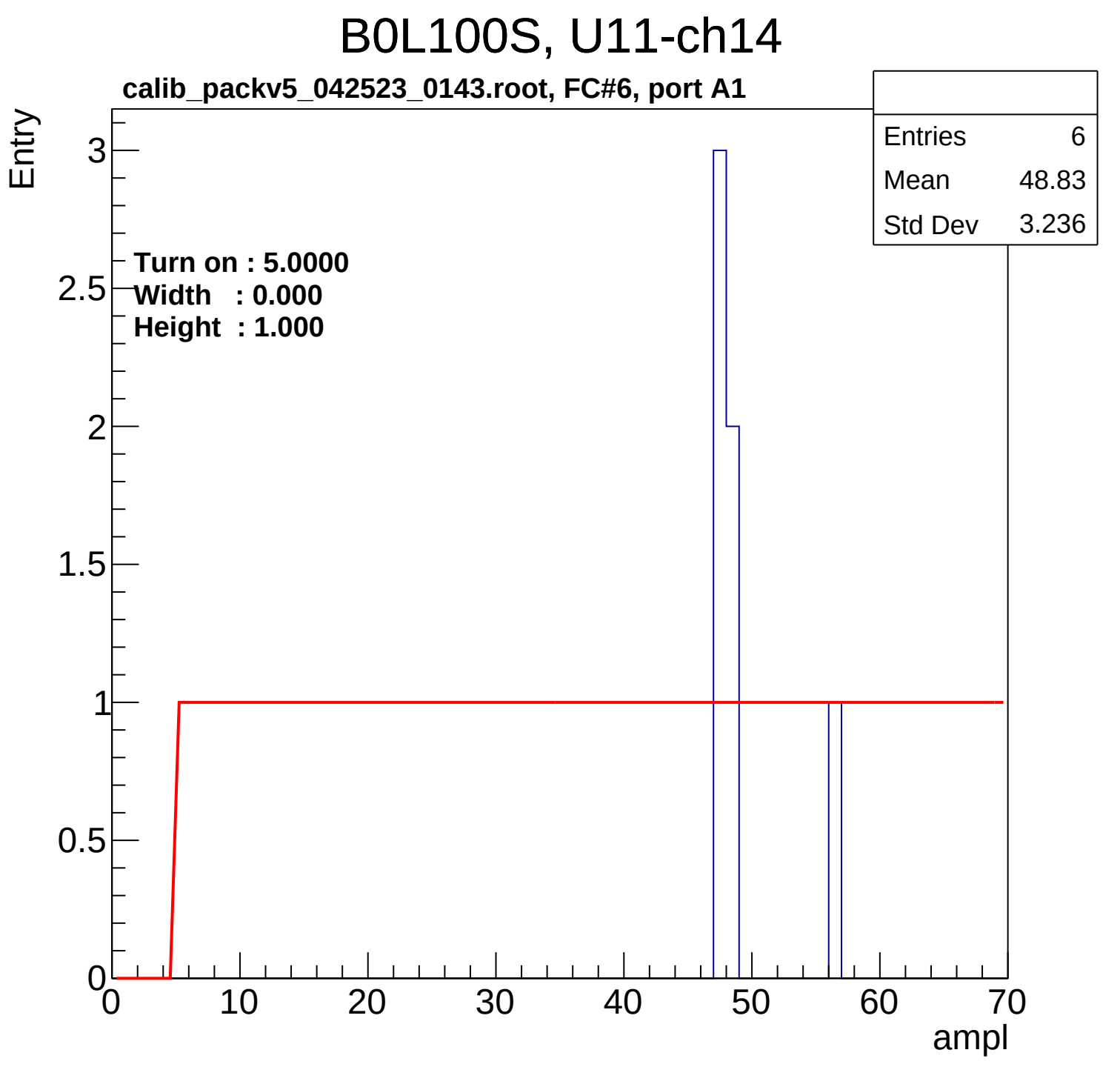

B0L100S, U11-ch9
calib_packv5_042523_0143.root, FC#6, port A1
Entries 3
Mean 34.33
Std Dev 24.28
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U11-ch10
calib_packv5_042523_0143.root, FC#6, port A1
Entries 5
Mean 47.8
Std Dev 1.833
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L100S, U11-ch11
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U11-ch12
calib_packv5_042523_0143.root, FC#6, port A1
Entries 6
Mean 42.83
Std Dev 19.16
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B0L100S, U11-ch13
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U11-ch14
calib_packv5_042523_0143.root, FC#6, port A1
Entries 6
Mean 48.83
Std Dev 3.236
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
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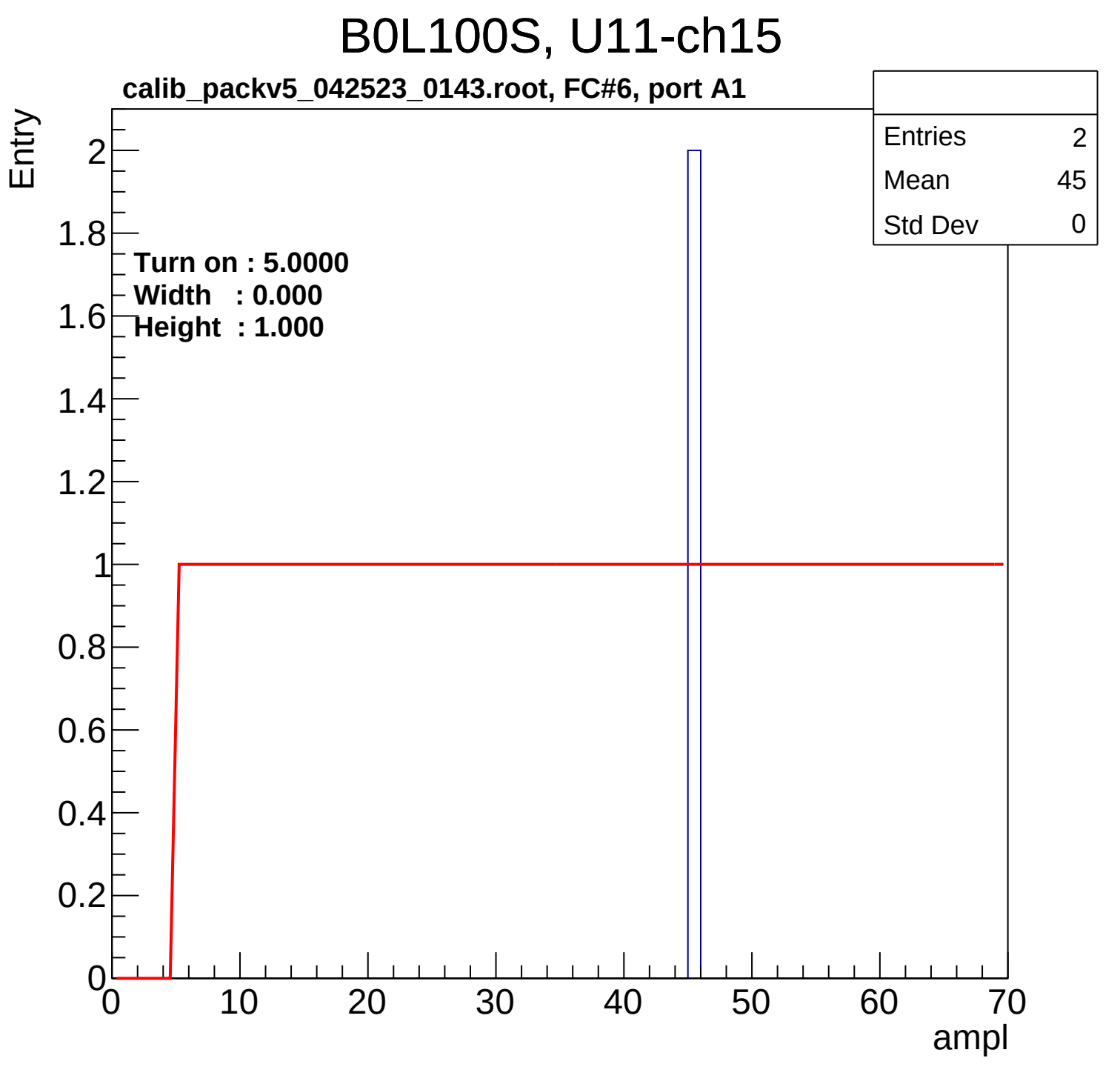
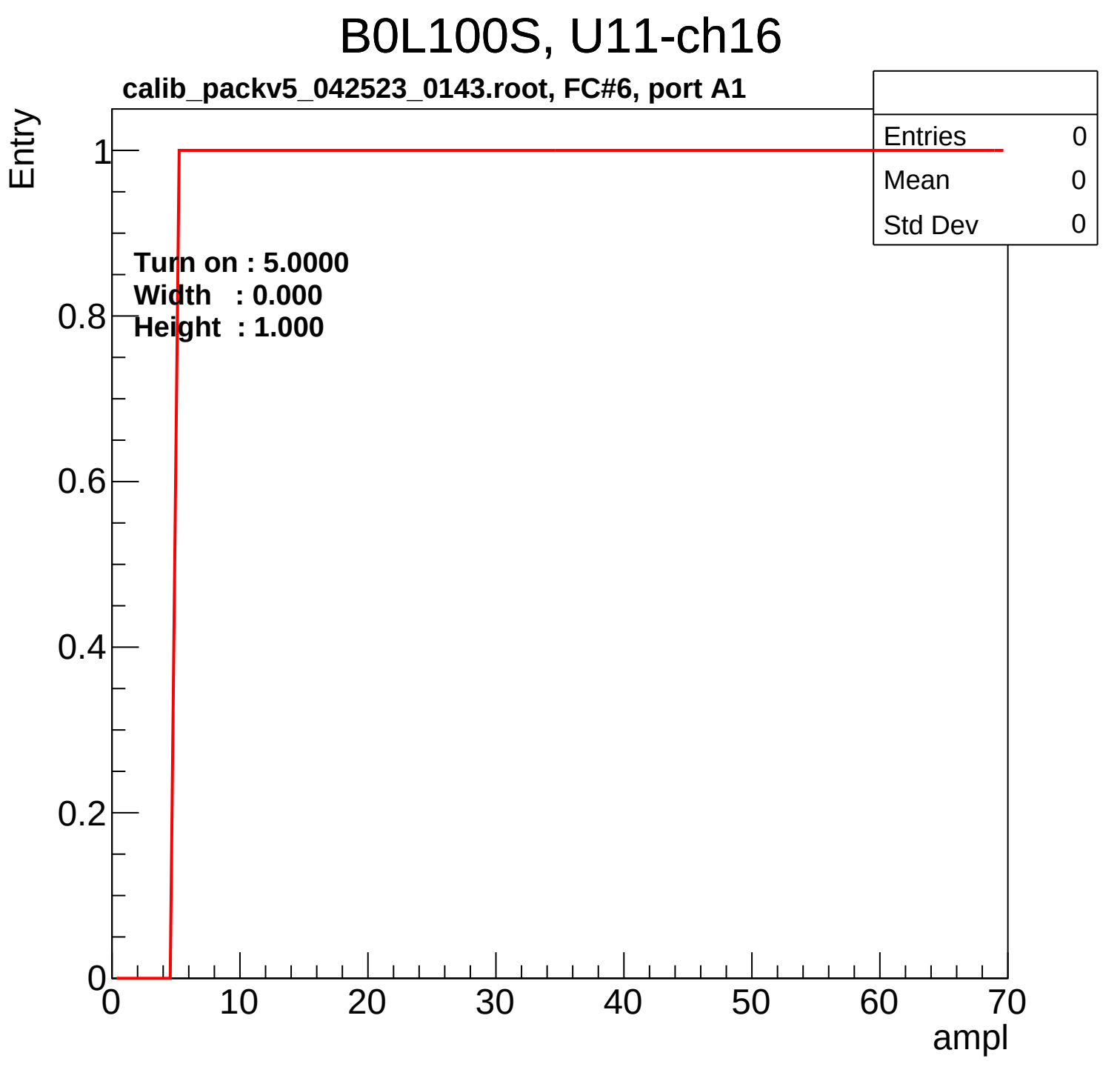
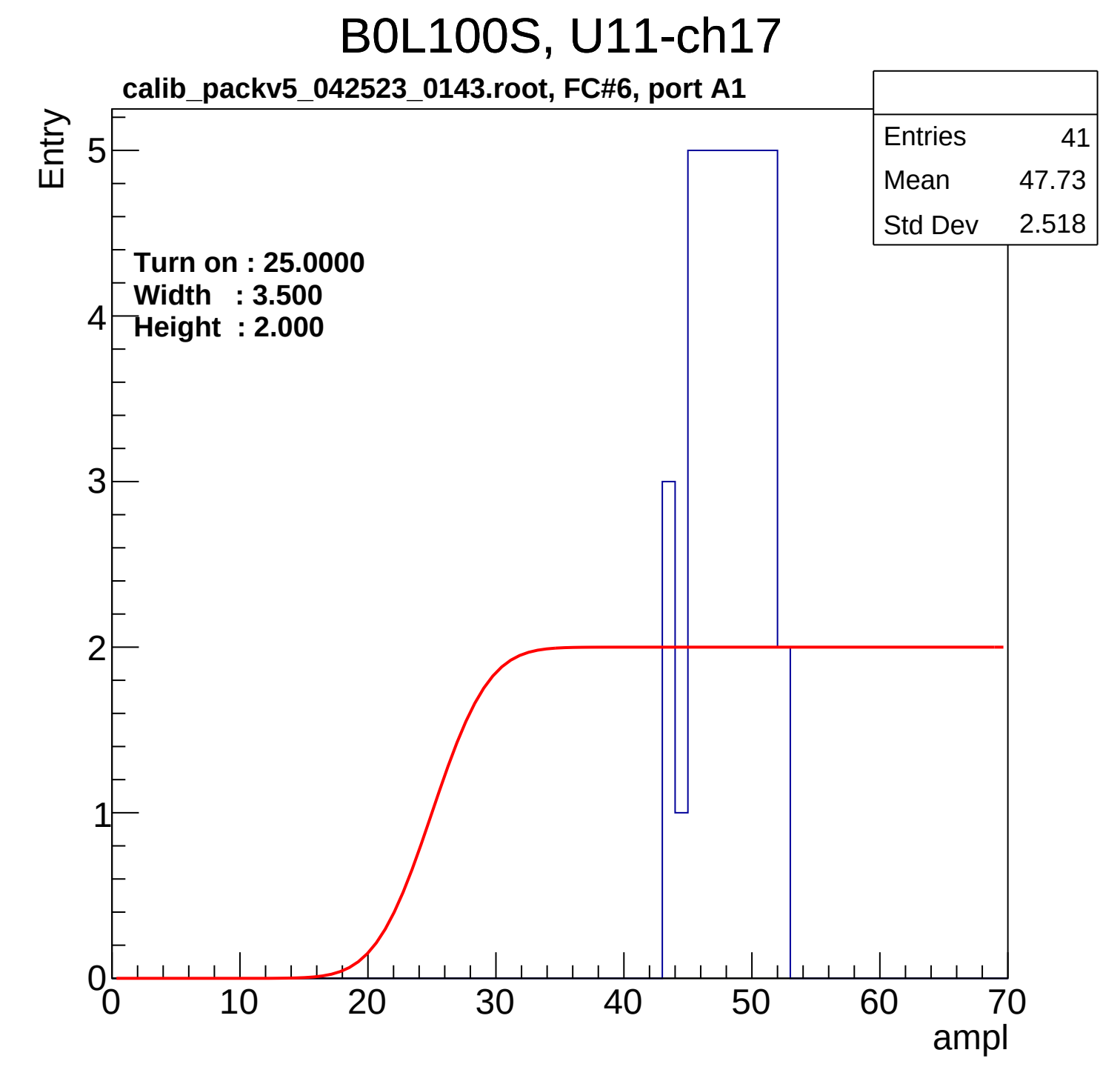
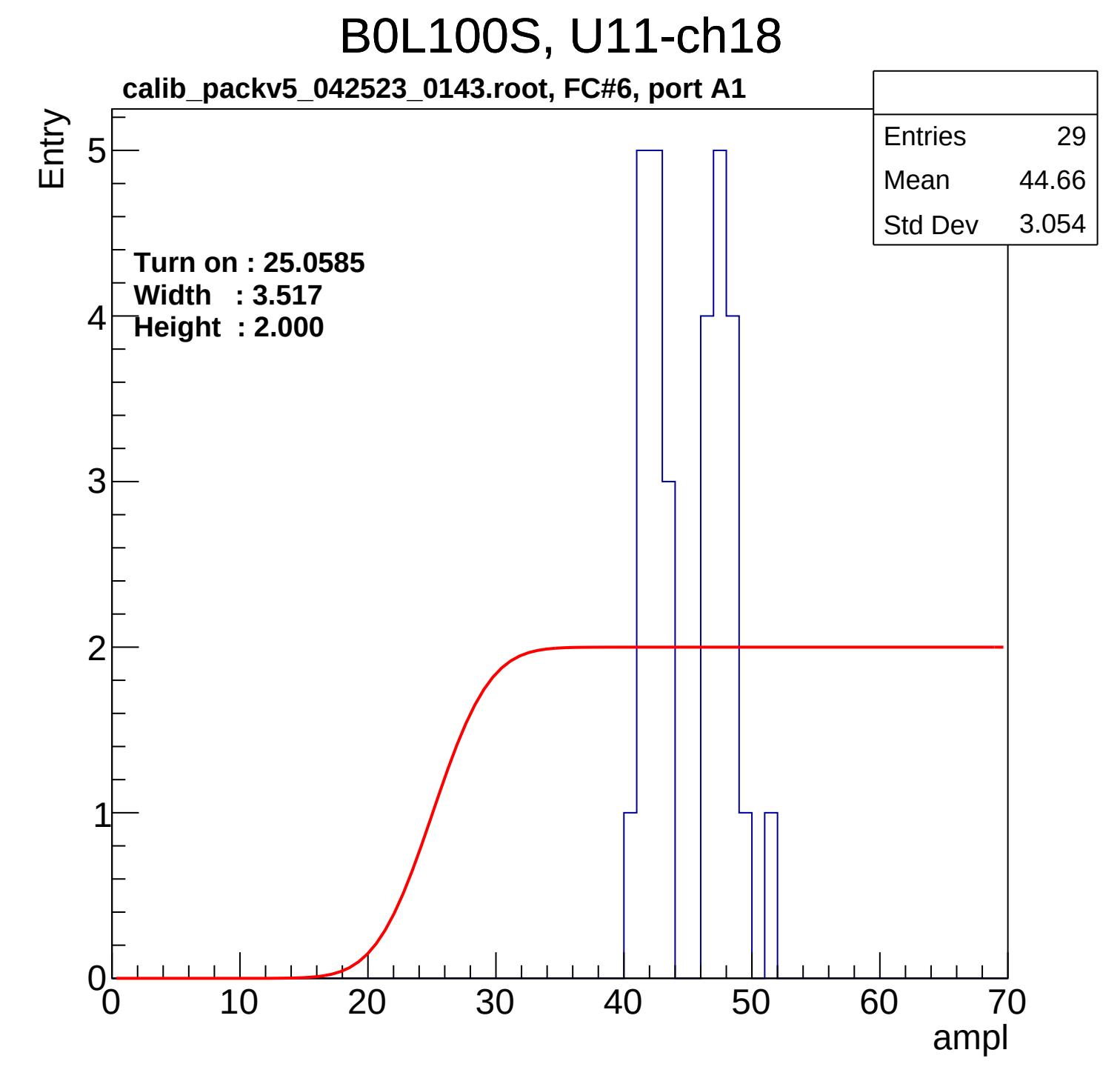
20
30
40
50
60
70


B0L100S, U11-ch15
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 45
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L100S, U11-ch16
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U11-ch17
calib_packv5_042523_0143.root, FC#6, port A1
Entries 41
Mean 47.73
Std Dev 2.518
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U11-ch18
calib_packv5_042523_0143.root, FC#6, port A1
Entries 29
Mean 44.66
Std Dev 3.054
Turn on : 25.0585
Width : 3.517
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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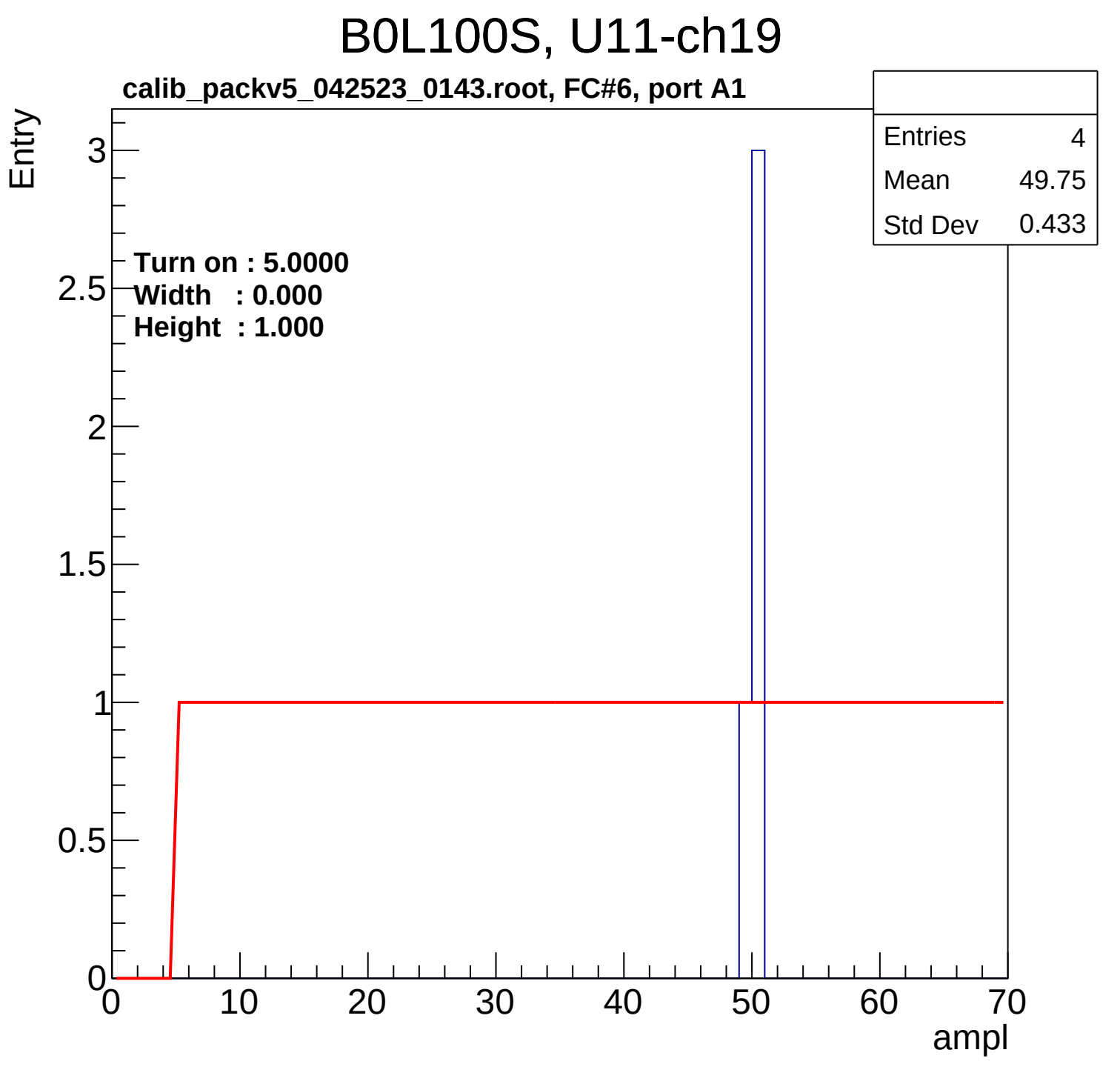
B0L100S, U11-ch19
calib_packv5_042523_0143.root, FC#6, port A1
Entries 4
Mean 49.75
Std Dev 0.433
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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40
50
60
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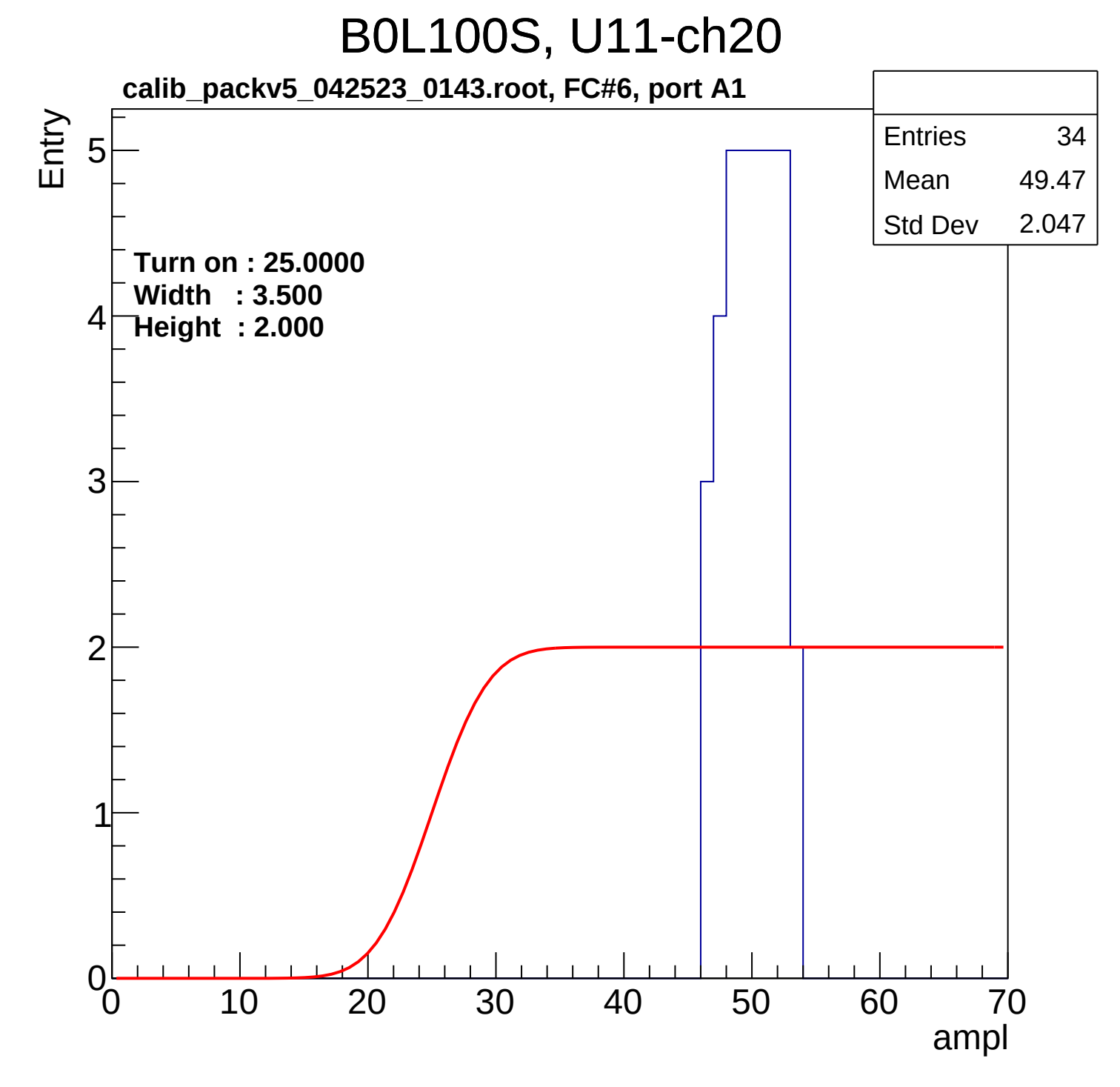
B0L100S, U11-ch20
calib_packv5_042523_0143.root, FC#6, port A1
Entries 34
Mean 49.47
Std Dev 2.047
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
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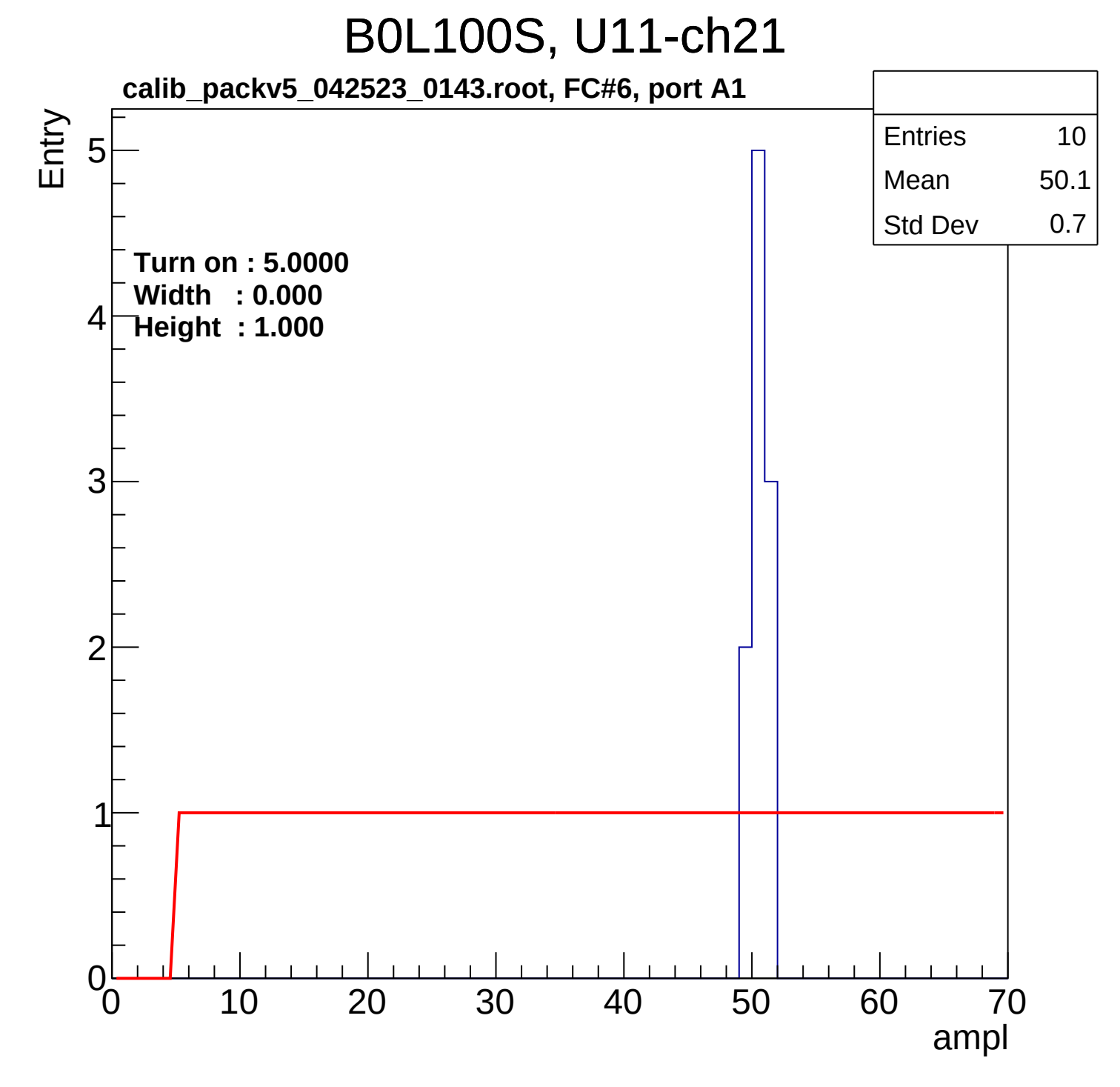
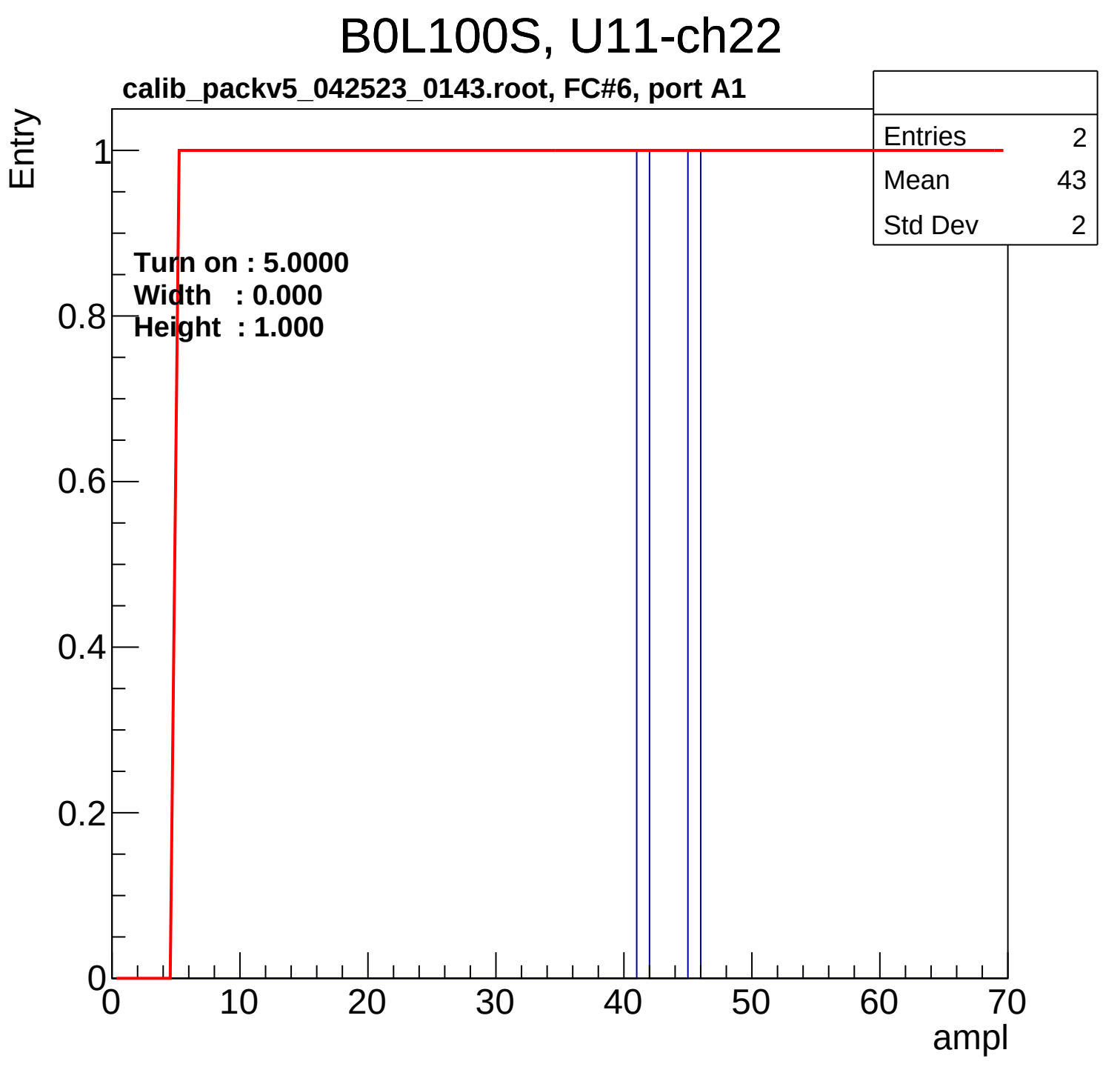
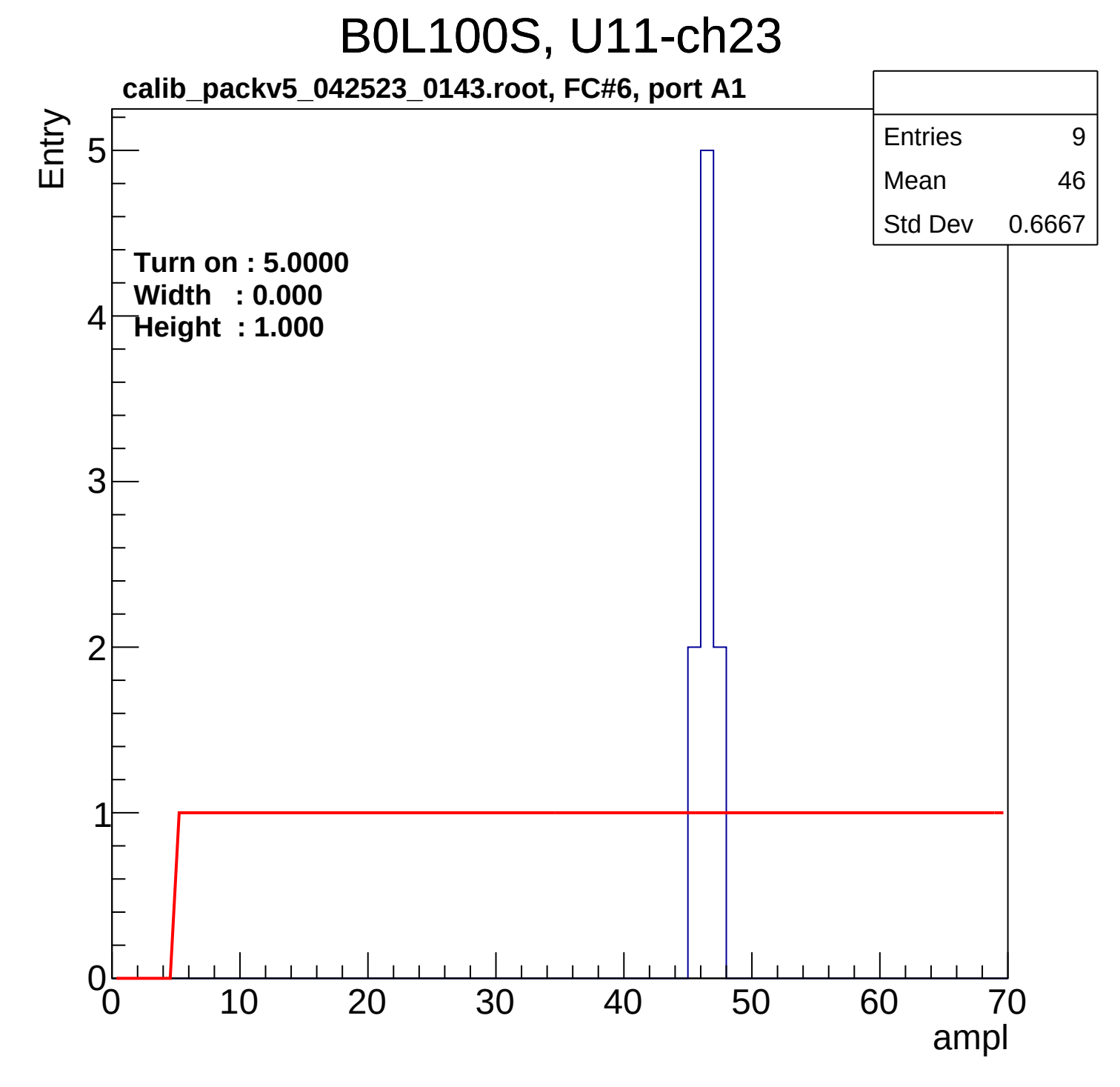
20
30
40
50
60
70


B0L100S, U11-ch21
calib_packv5_042523_0143.root, FC#6, port A1
Entries 10
Mean 50.1
Std Dev 0.7
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U11-ch22
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 43
Std Dev 2
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U11-ch23
calib_packv5_042523_0143.root, FC#6, port A1
Entries 9
Mean 46
Std Dev 0.6667
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
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60
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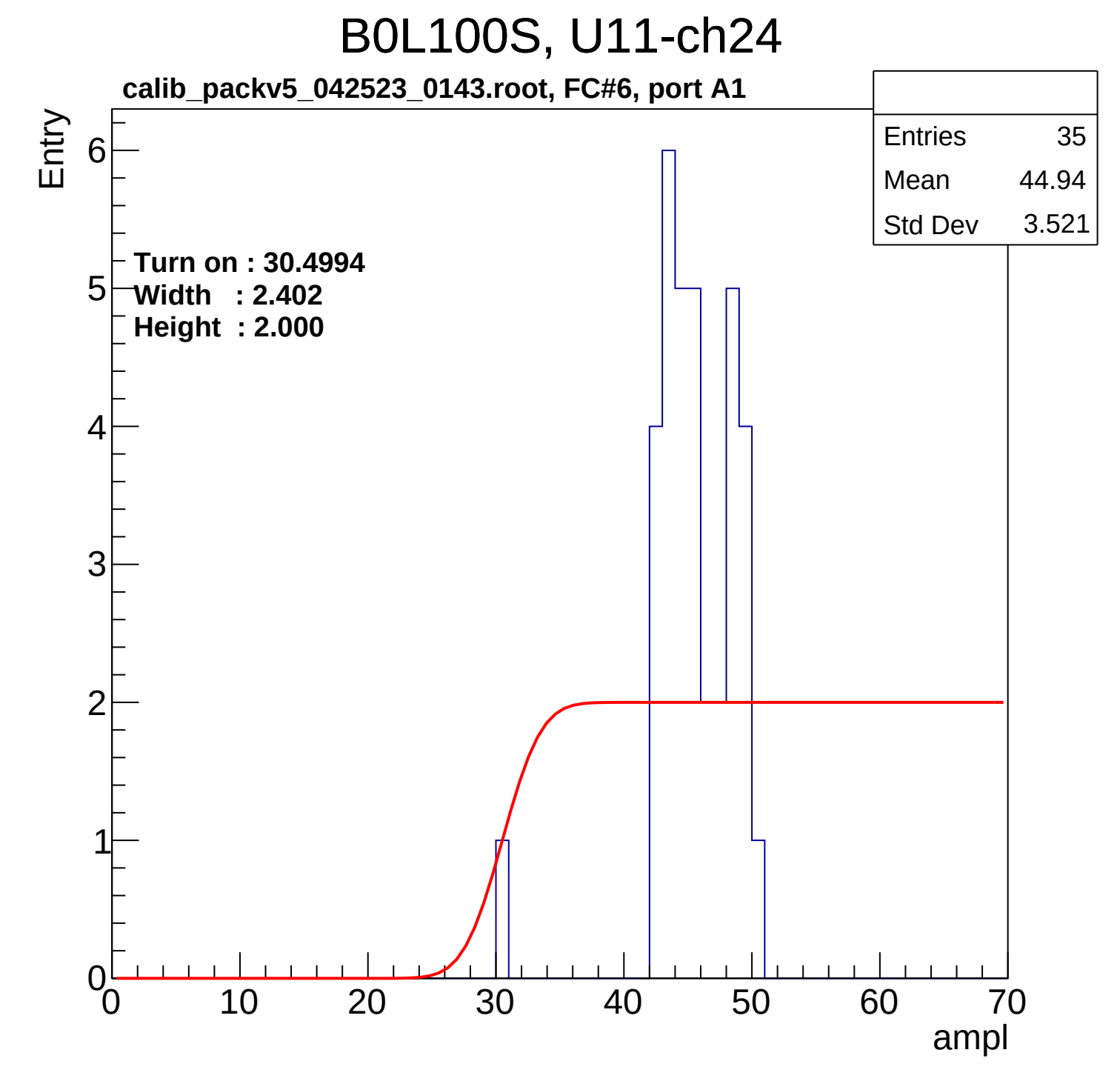
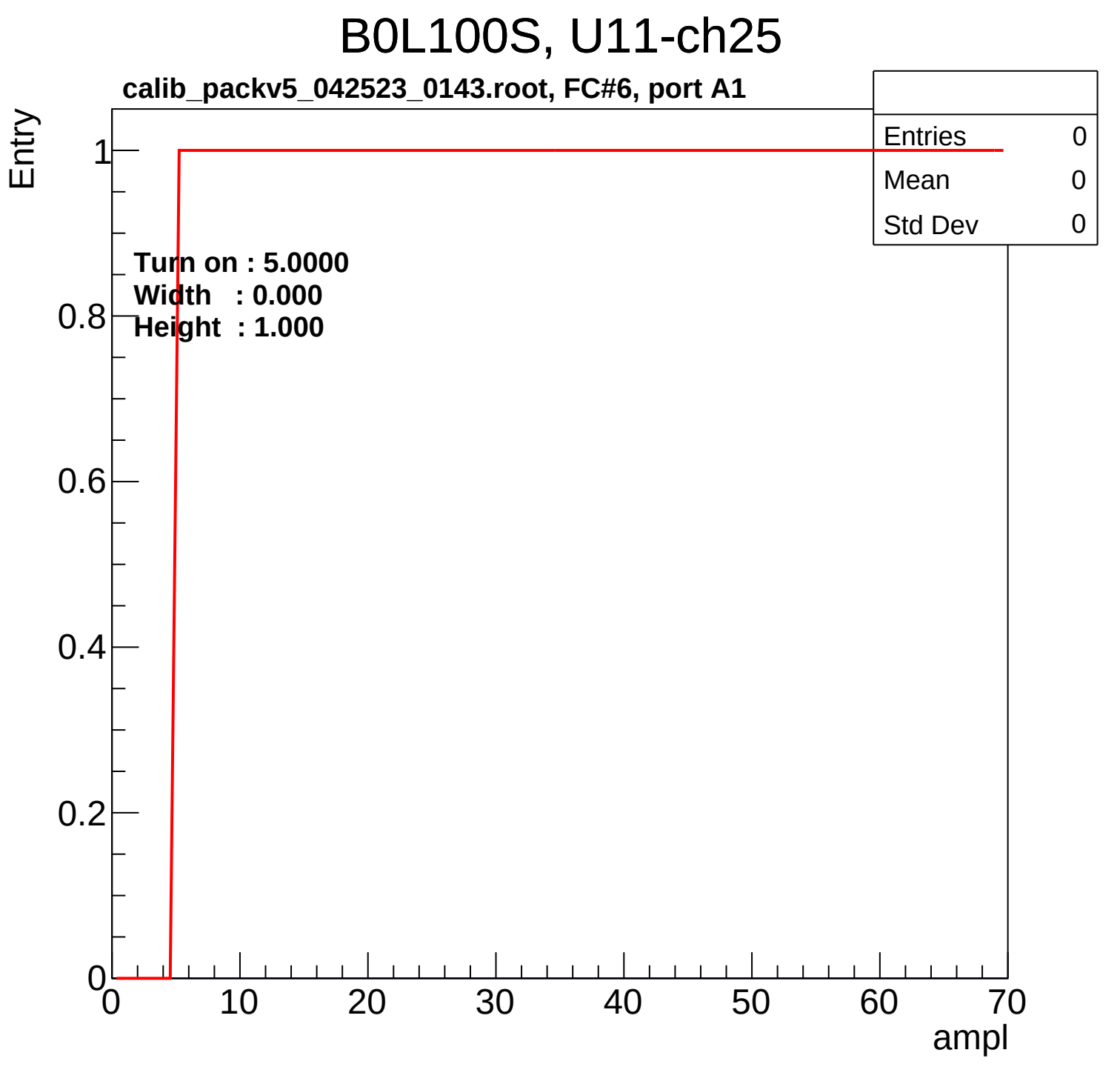

B0L100S, U11-ch24
calib_packv5_042523_0143.root, FC#6, port A1
Entries 35
Mean 44.94
Std Dev 3.521
Turn on : 30.4994
Width : 2.402
Height : 2.000
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B0L100S, U11-ch25
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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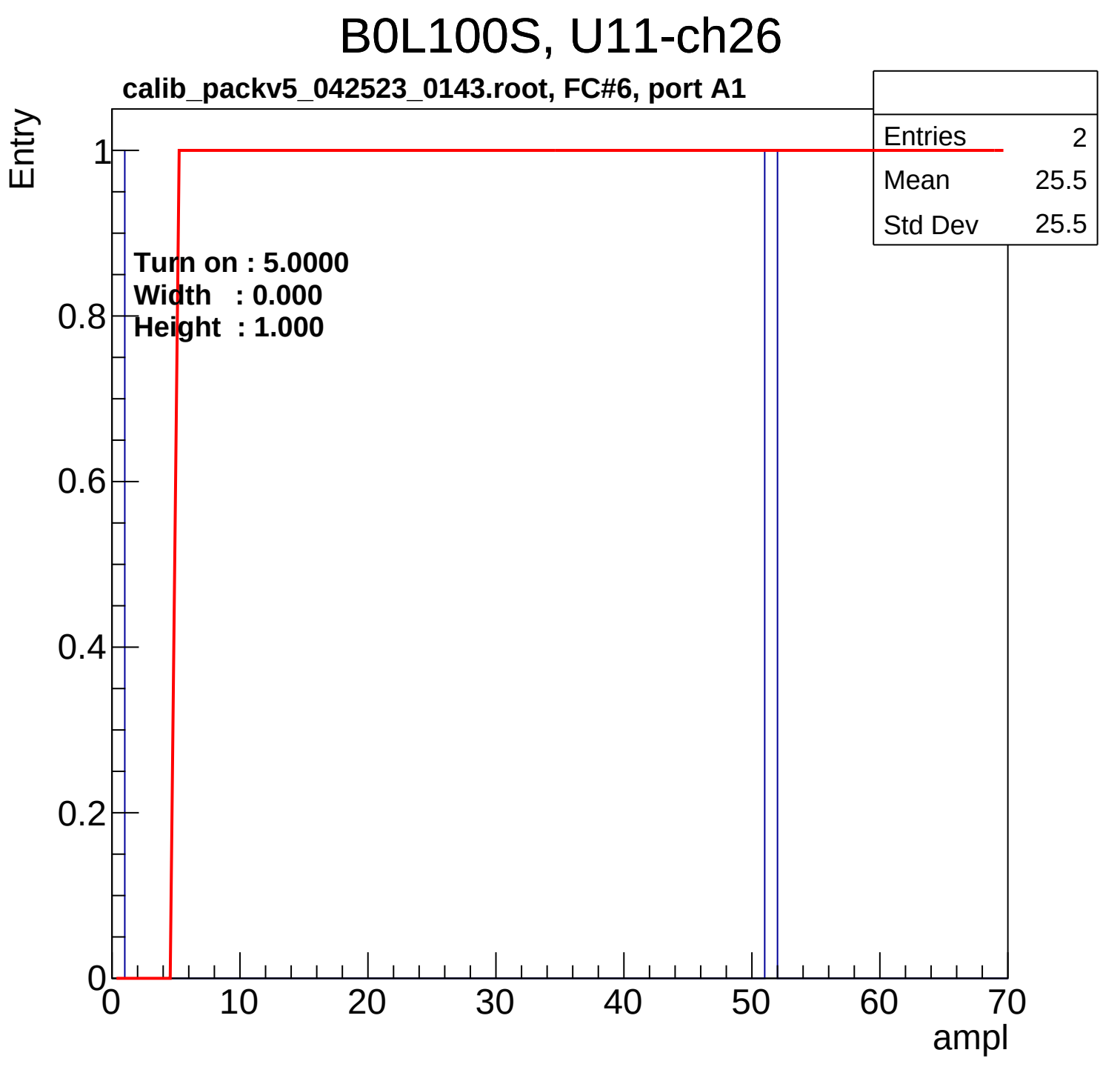
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U11-ch26
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 25.5
Std Dev 25.5
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
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50
60
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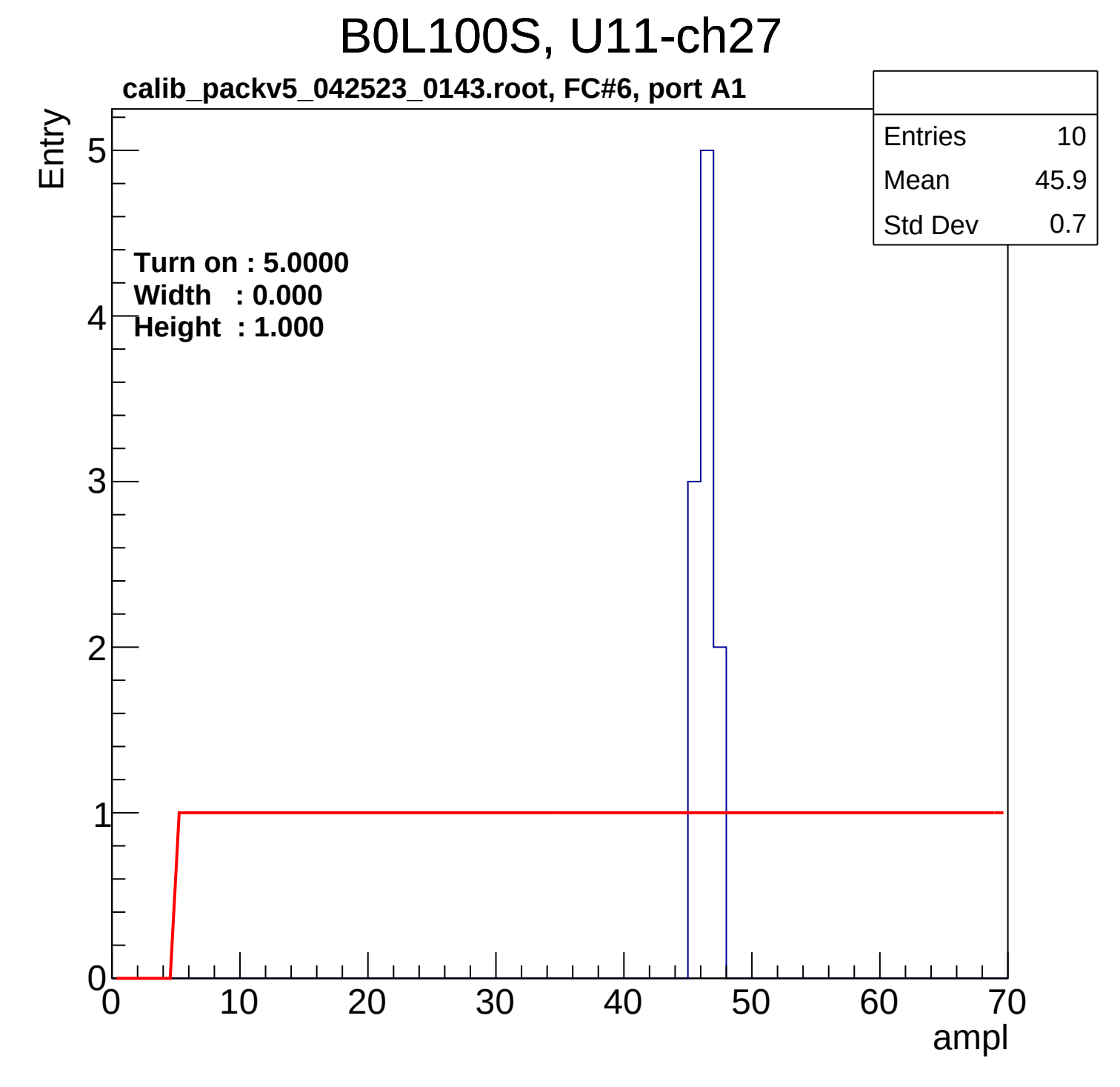
B0L100S, U11-ch27
calib_packv5_042523_0143.root, FC#6, port A1
Entries 10
Mean 45.9
Std Dev 0.7
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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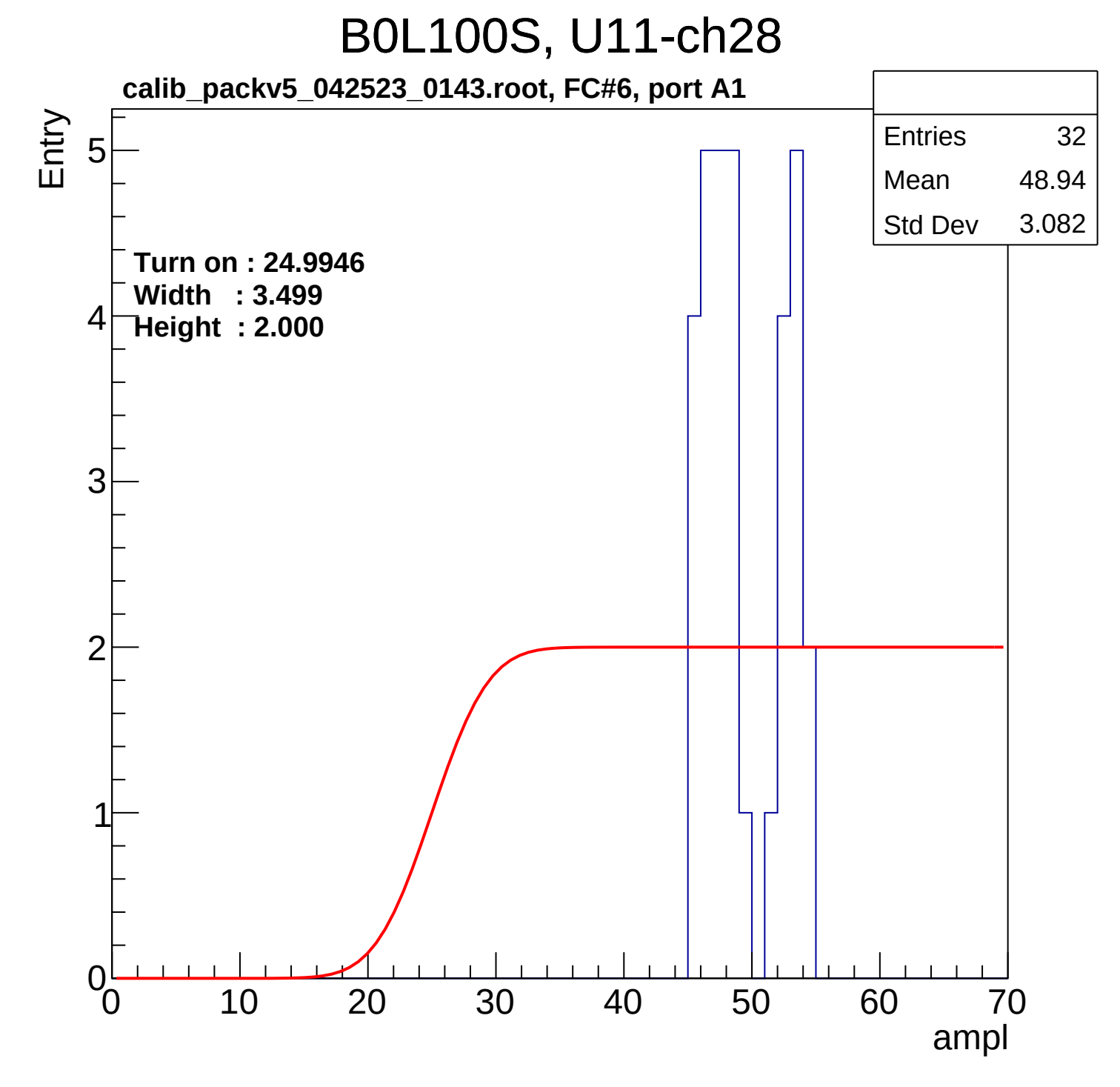
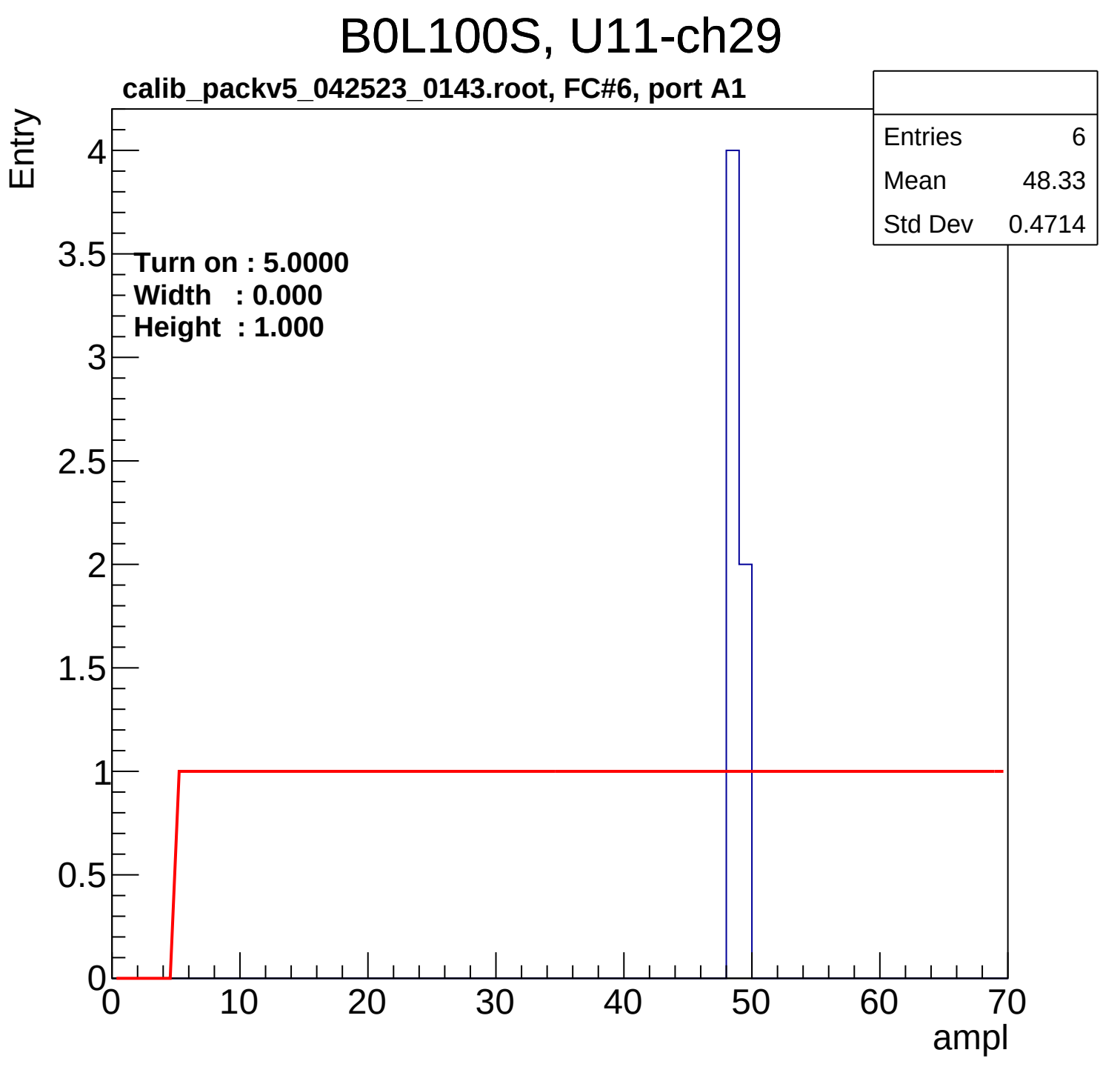

B0L100S, U11-ch28
calib_packv5_042523_0143.root, FC#6, port A1
Entries 32
Mean 48.94
Std Dev 3.082
Turn on : 24.9946
Width : 3.499
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U11-ch29
calib_packv5_042523_0143.root, FC#6, port A1
Entries 6
Mean 48.33
Std Dev 0.4714
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
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0
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60
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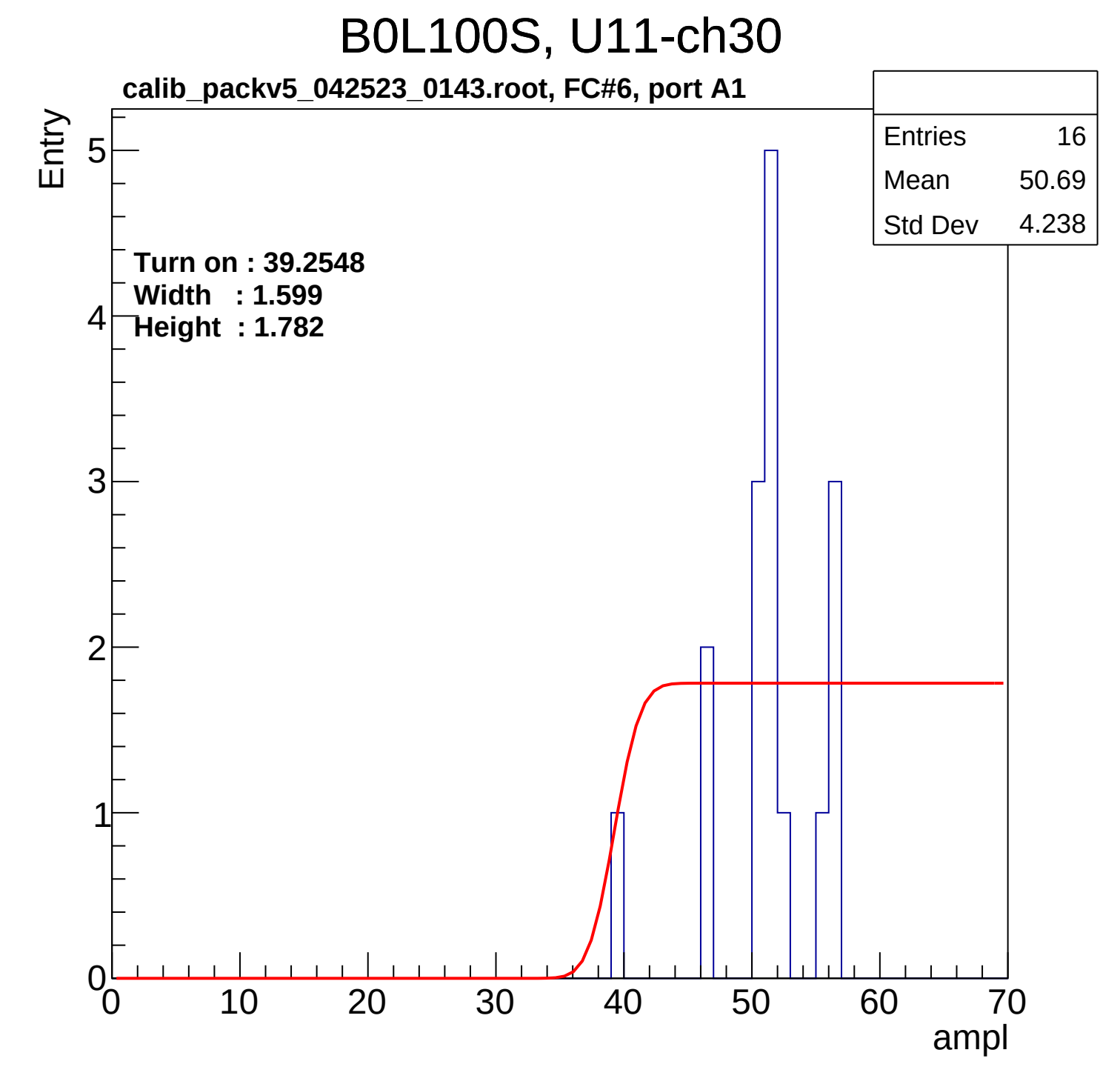
B0L100S, U11-ch30
calib_packv5_042523_0143.root, FC#6, port A1
Entries 16
Mean 50.69
Std Dev 4.238
Turn on : 39.2548
Width : 1.599
Height : 1.782
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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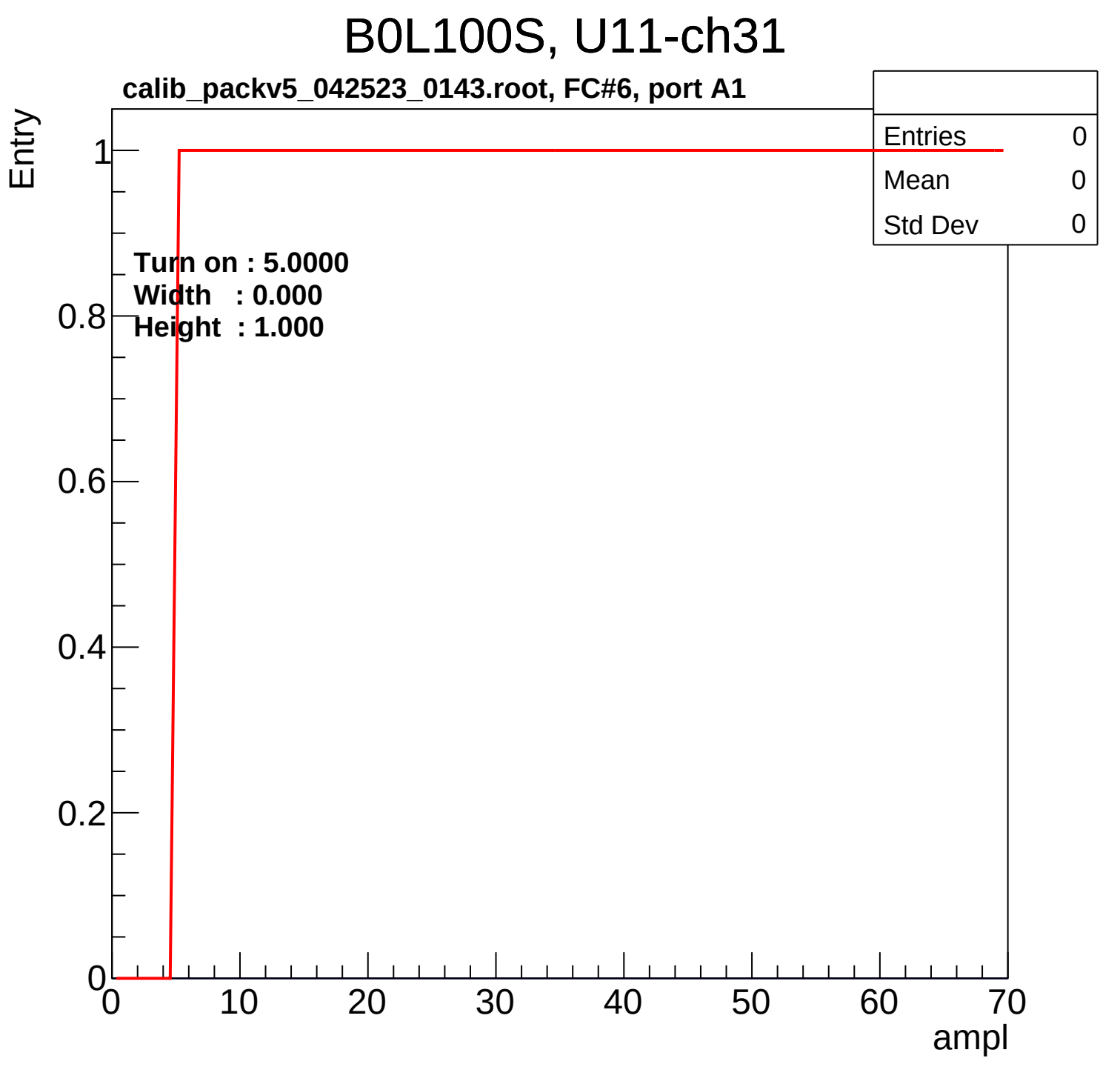
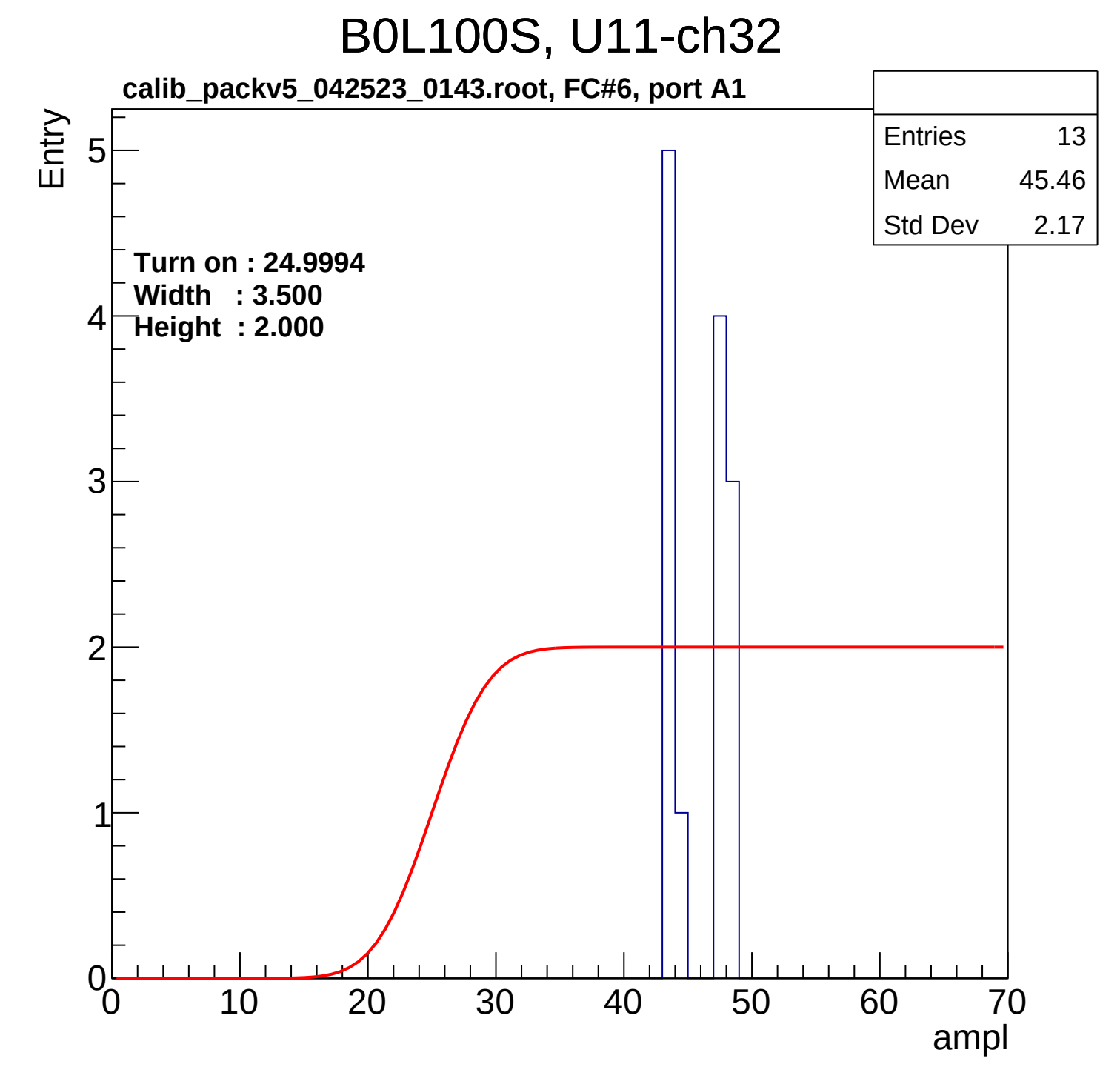
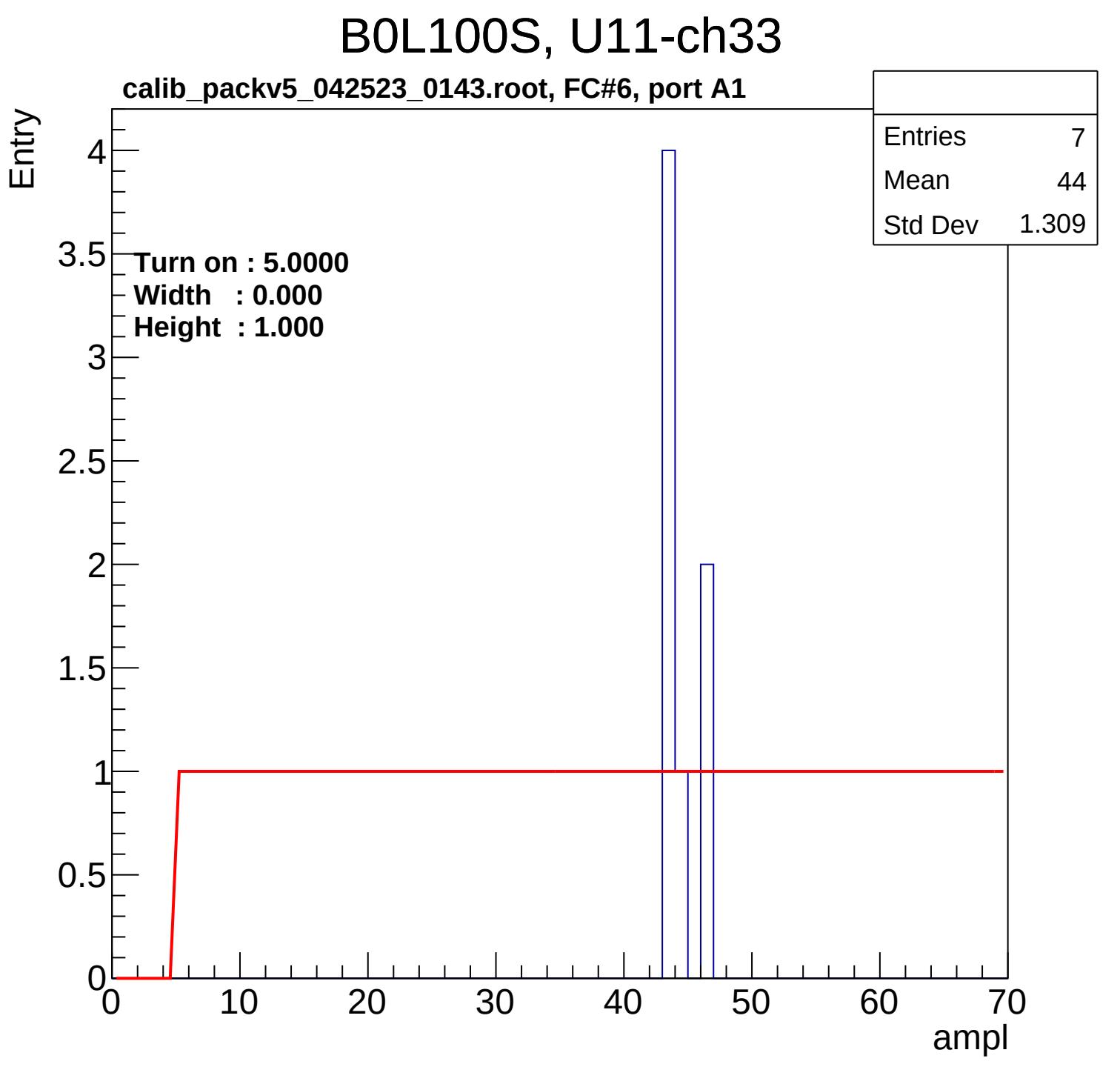

B0L100S, U11-ch31
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U11-ch32
calib_packv5_042523_0143.root, FC#6, port A1
Entries 13
Mean 45.46
Std Dev 2.17
Turn on : 24.9994
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U11-ch33
calib_packv5_042523_0143.root, FC#6, port A1
Entries 7
Mean 44
Std Dev 1.309
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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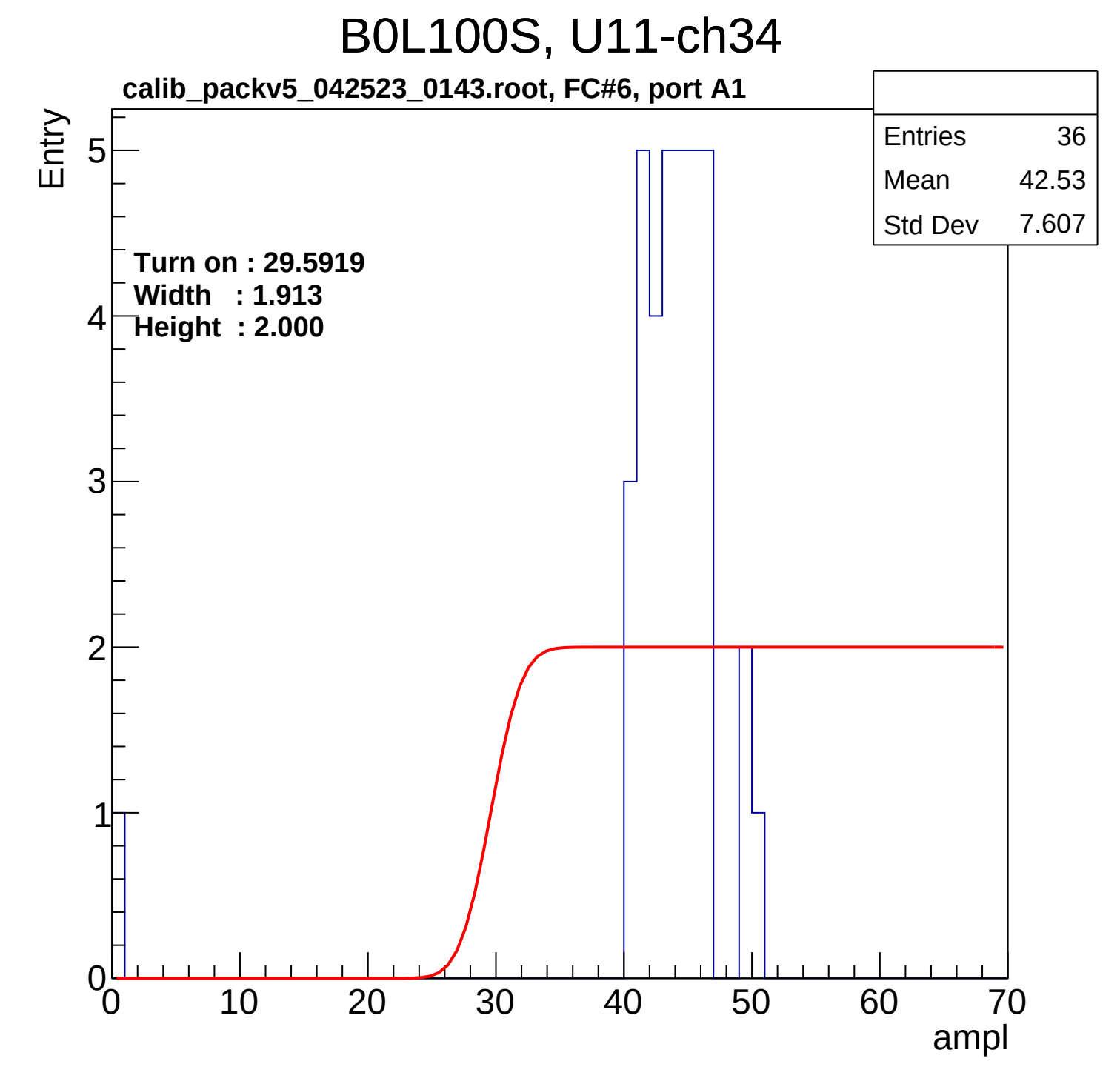
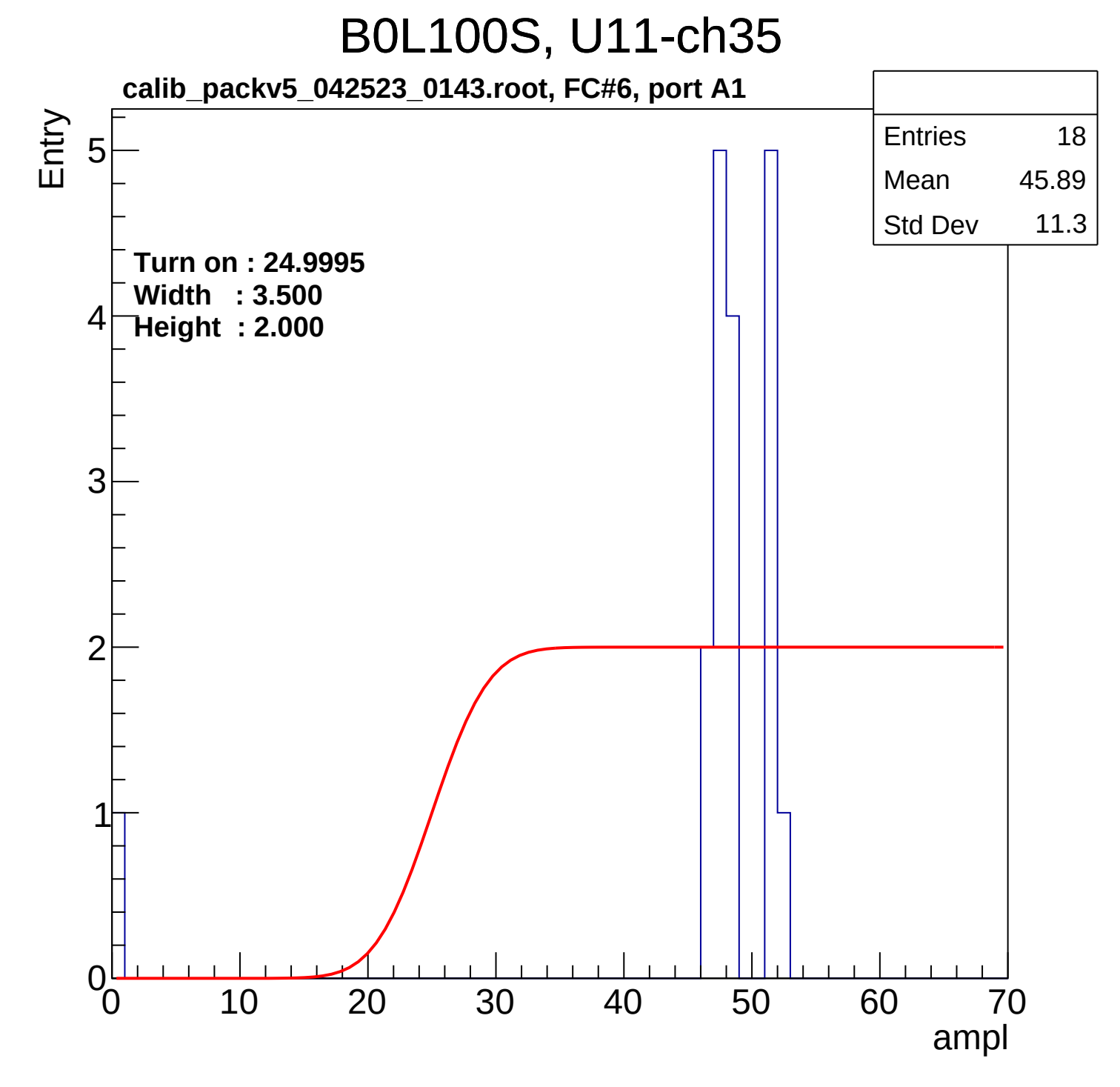

B0L100S, U11-ch34
calib_packv5_042523_0143.root, FC#6, port A1
Entries 36
Mean 42.53
Std Dev 7.607
Turn on : 29.5919
Width : 1.913
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U11-ch35
calib_packv5_042523_0143.root, FC#6, port A1
Entries 18
Mean 45.89
Std Dev 11.3
Turn on : 24.9995
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
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20
30
40
50
60
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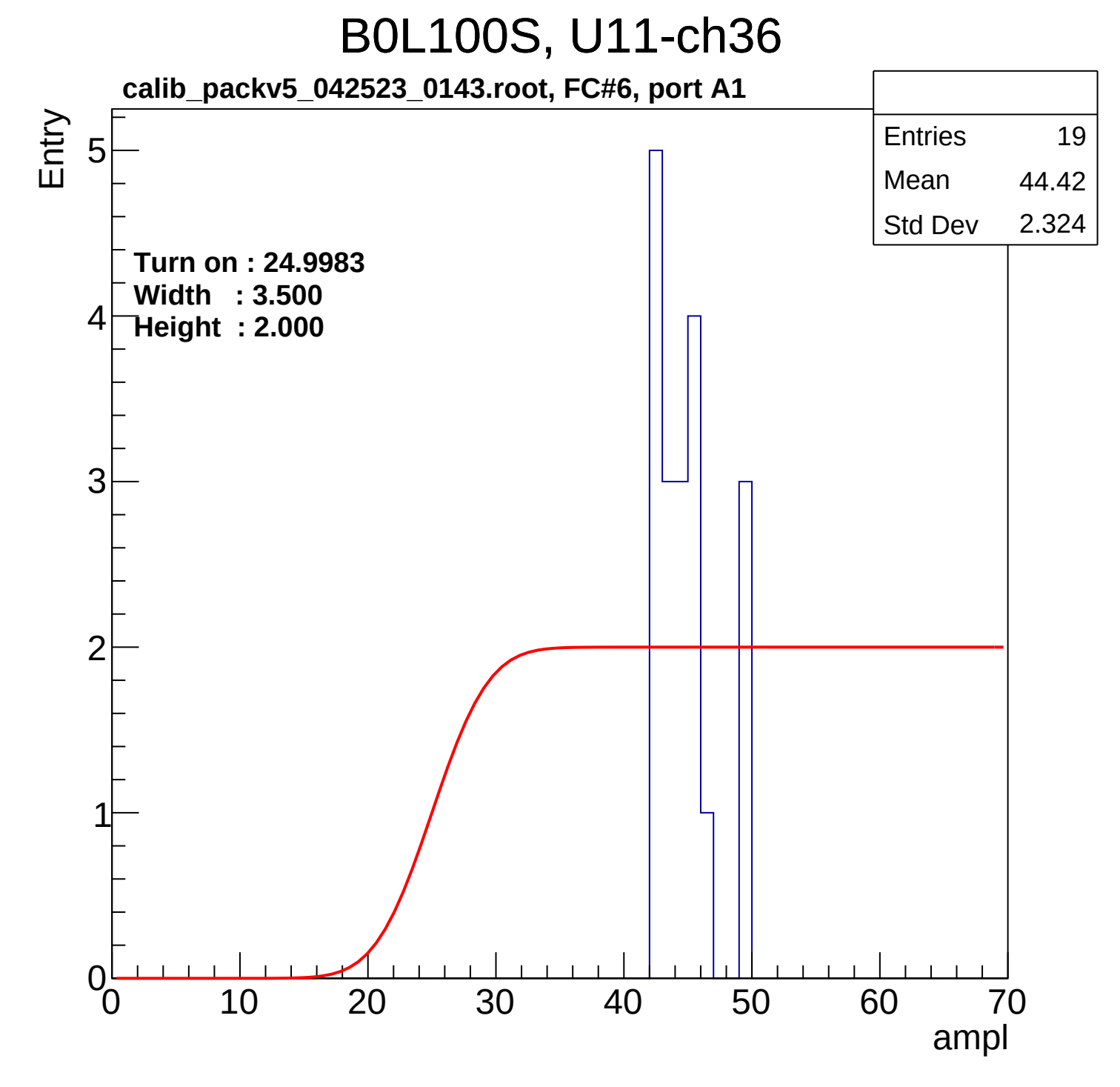
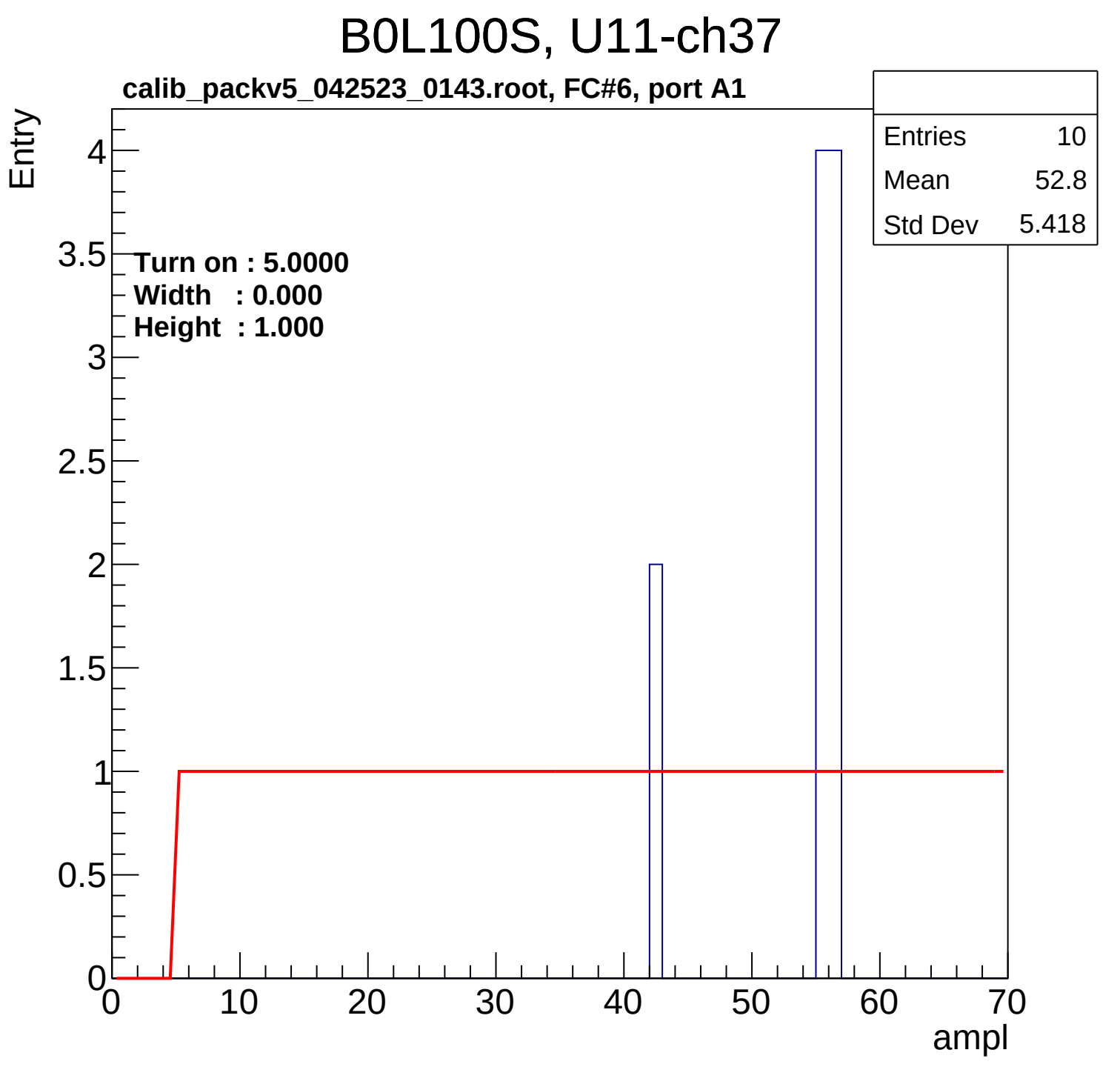
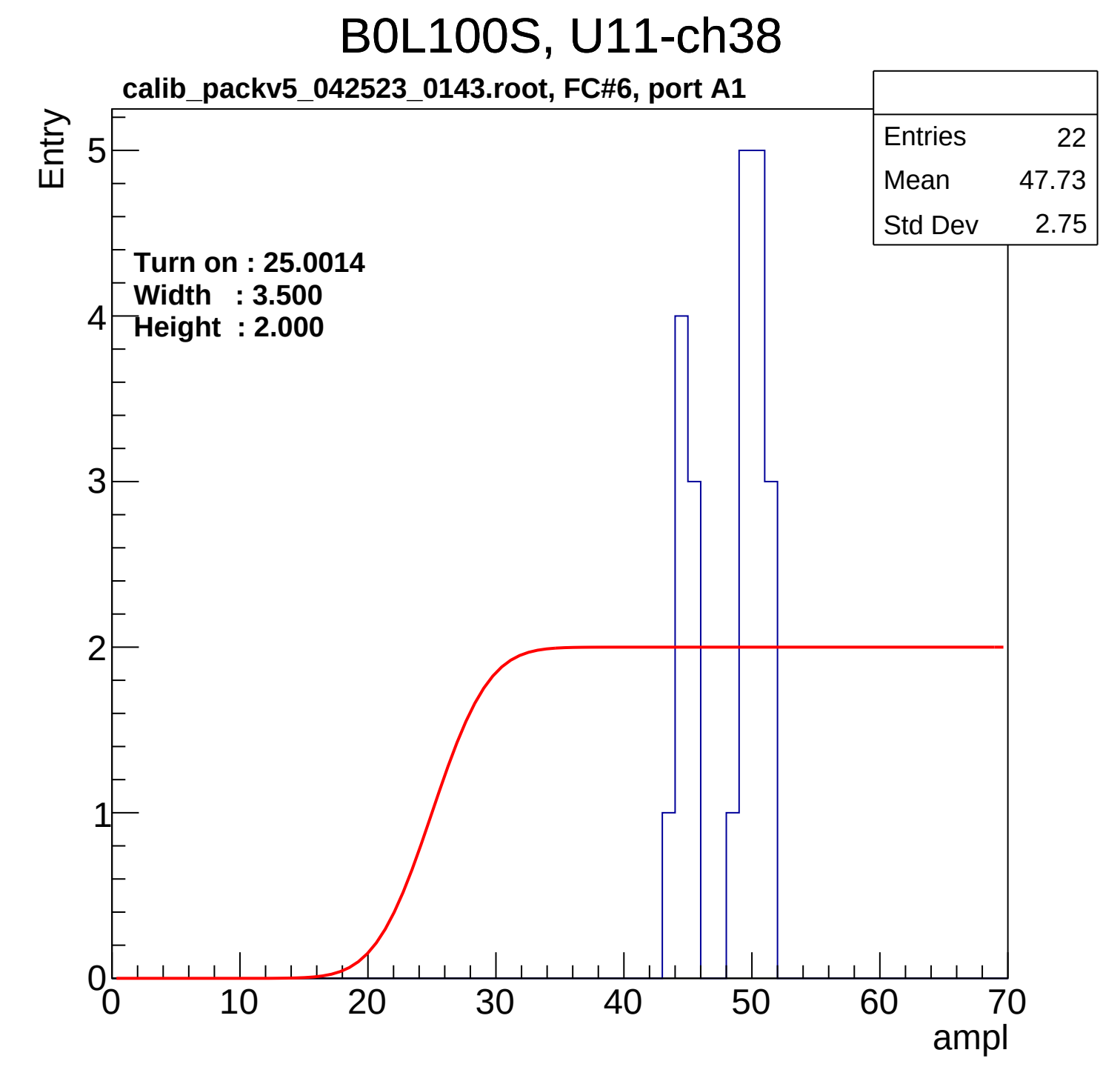

B0L100S, U11-ch36
calib_packv5_042523_0143.root, FC#6, port A1
Entries 19
Mean 44.42
Std Dev 2.324
Turn on : 24.9983
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U11-ch37
calib_packv5_042523_0143.root, FC#6, port A1
Entries 10
Mean 52.8
Std Dev 5.418
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B0L100S, U11-ch38
calib_packv5_042523_0143.root, FC#6, port A1
Entries 22
Mean 47.73
Std Dev 2.75
Turn on : 25.0014
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
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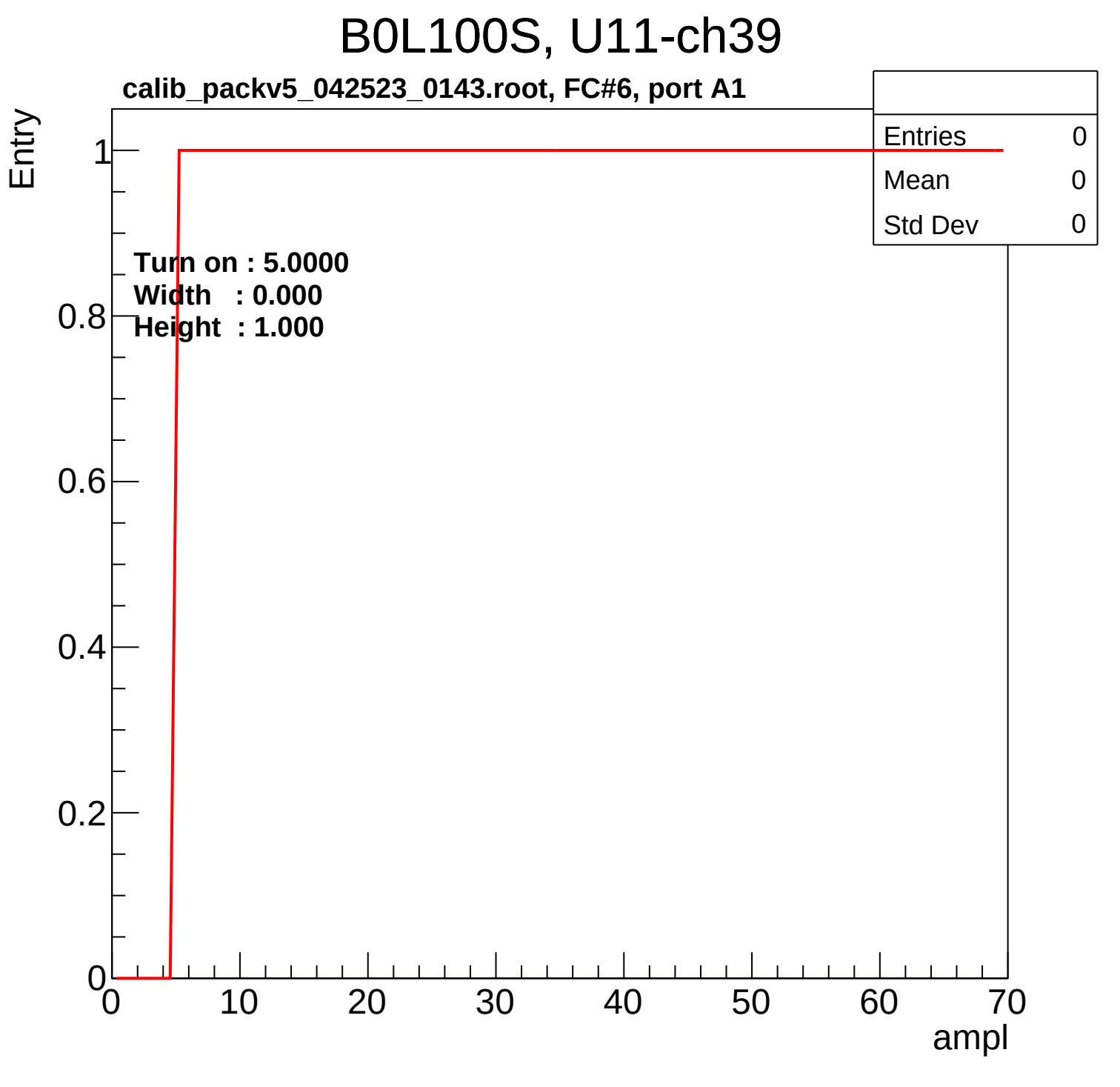
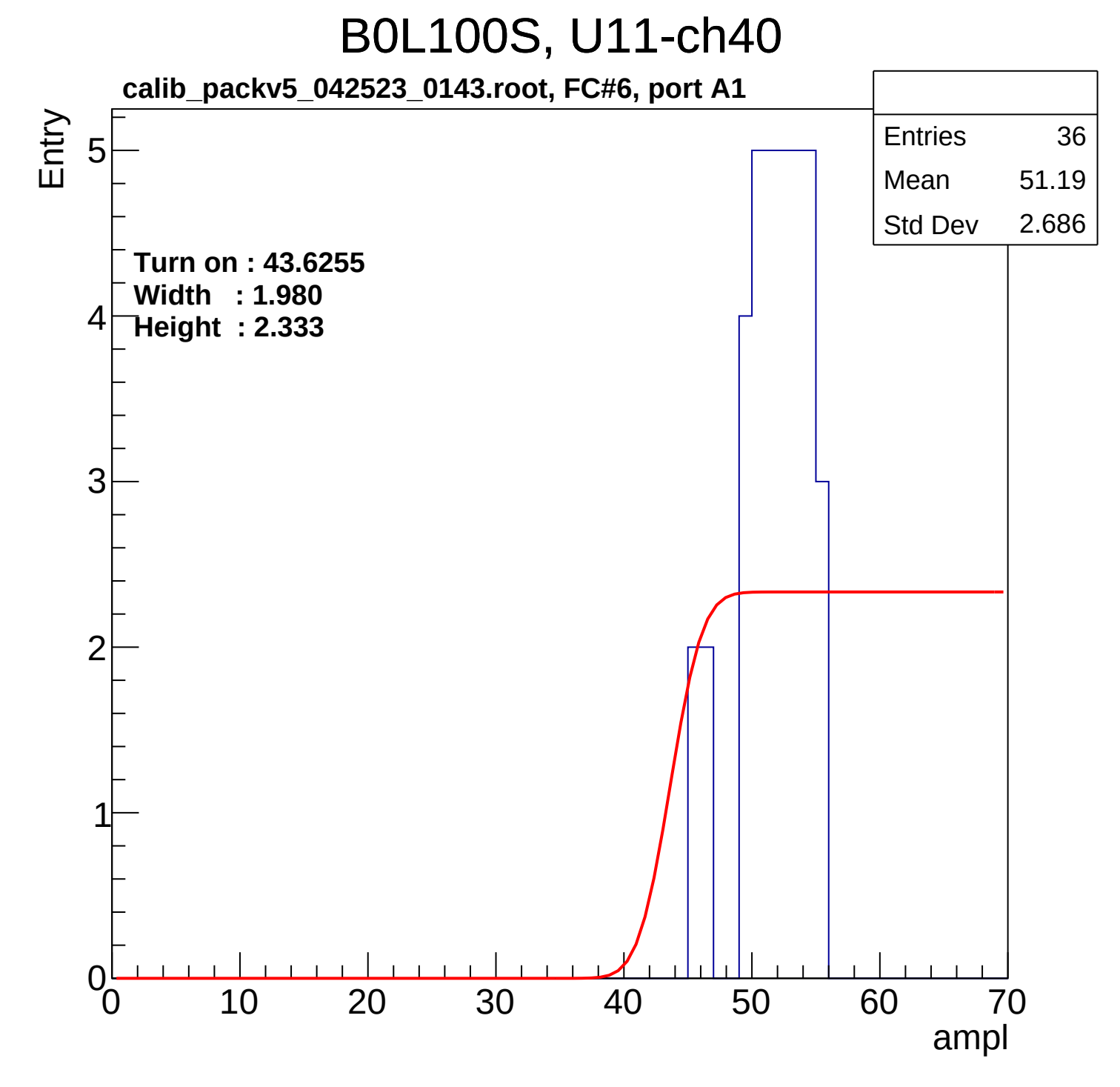
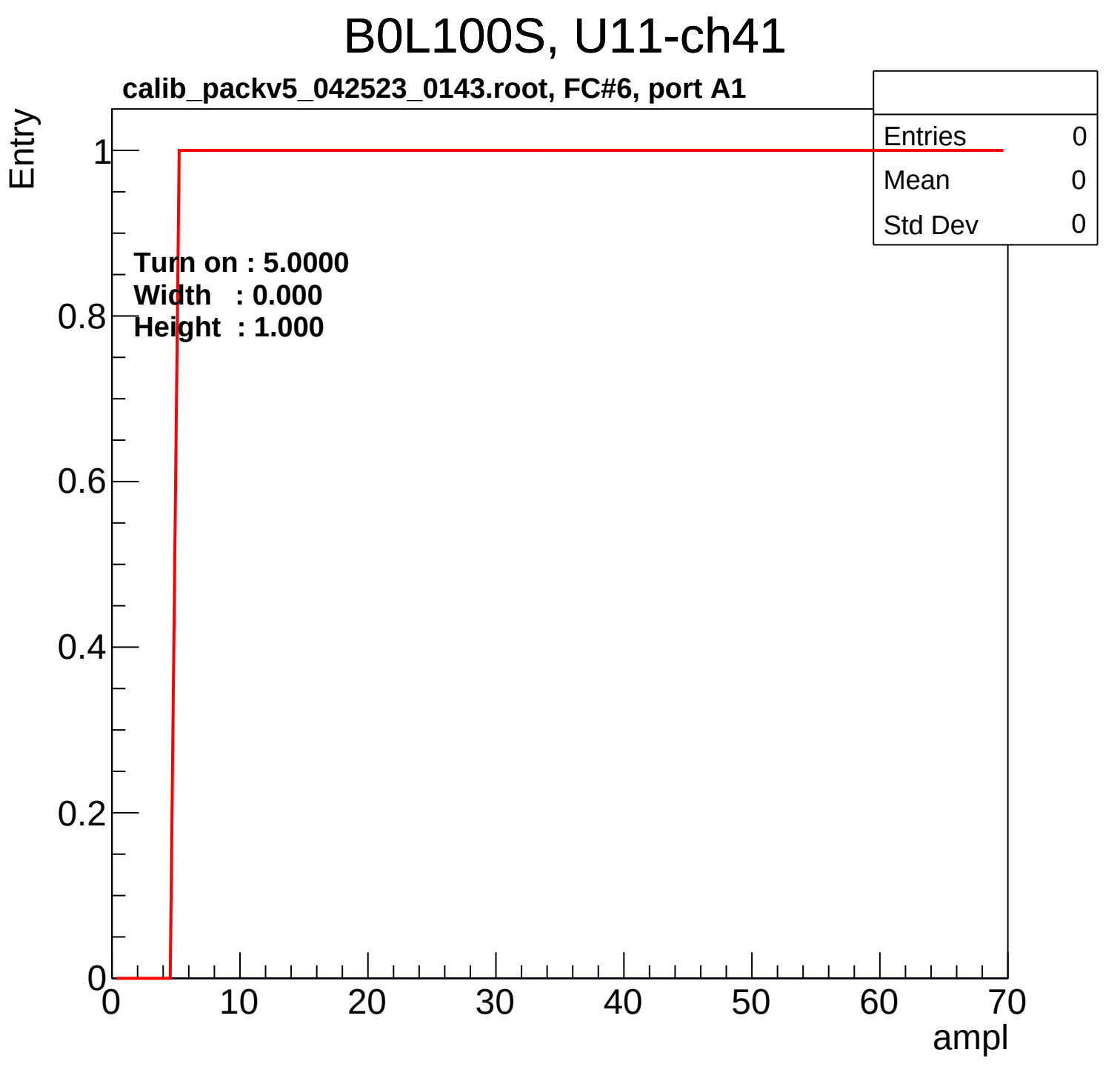
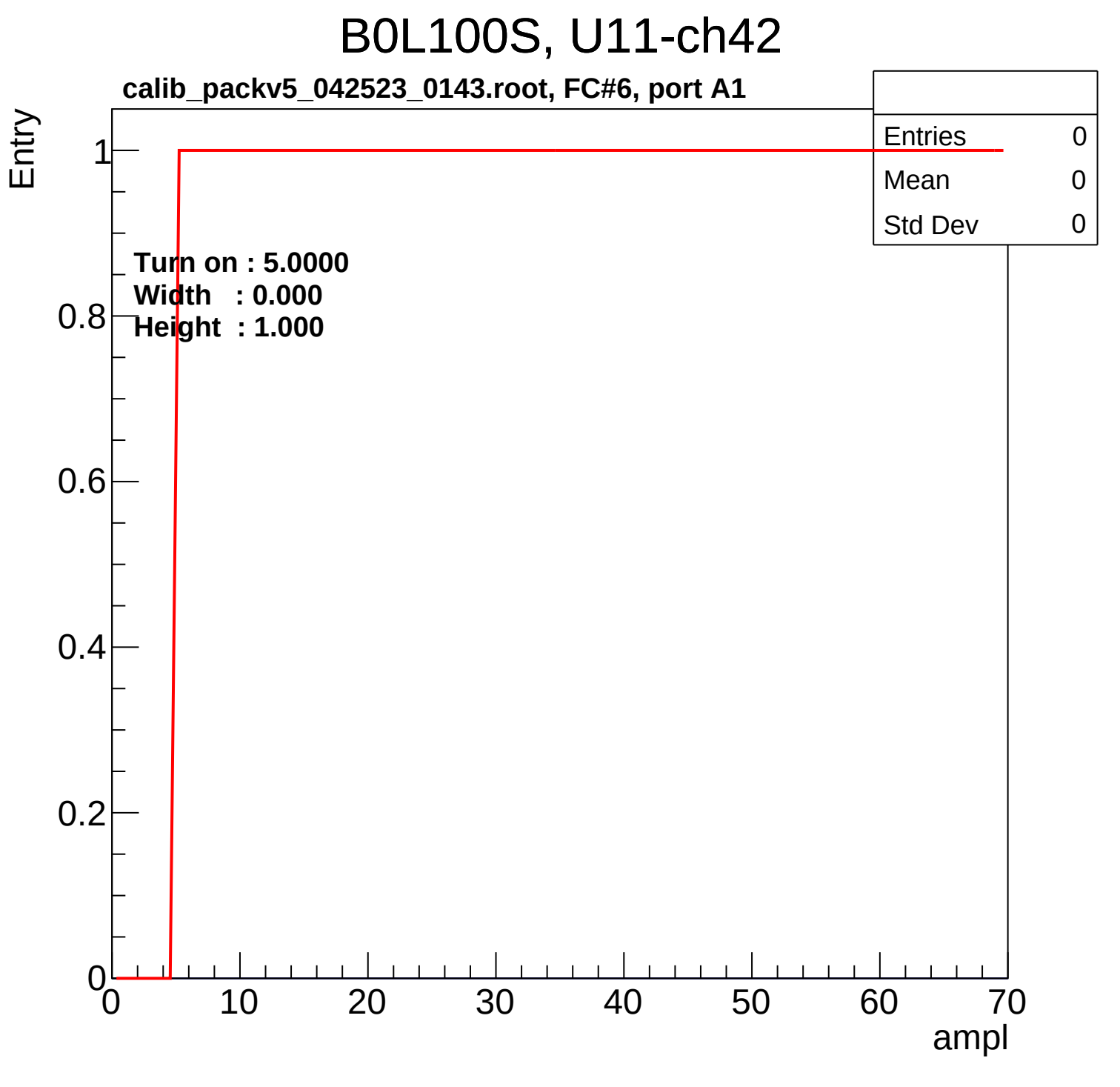
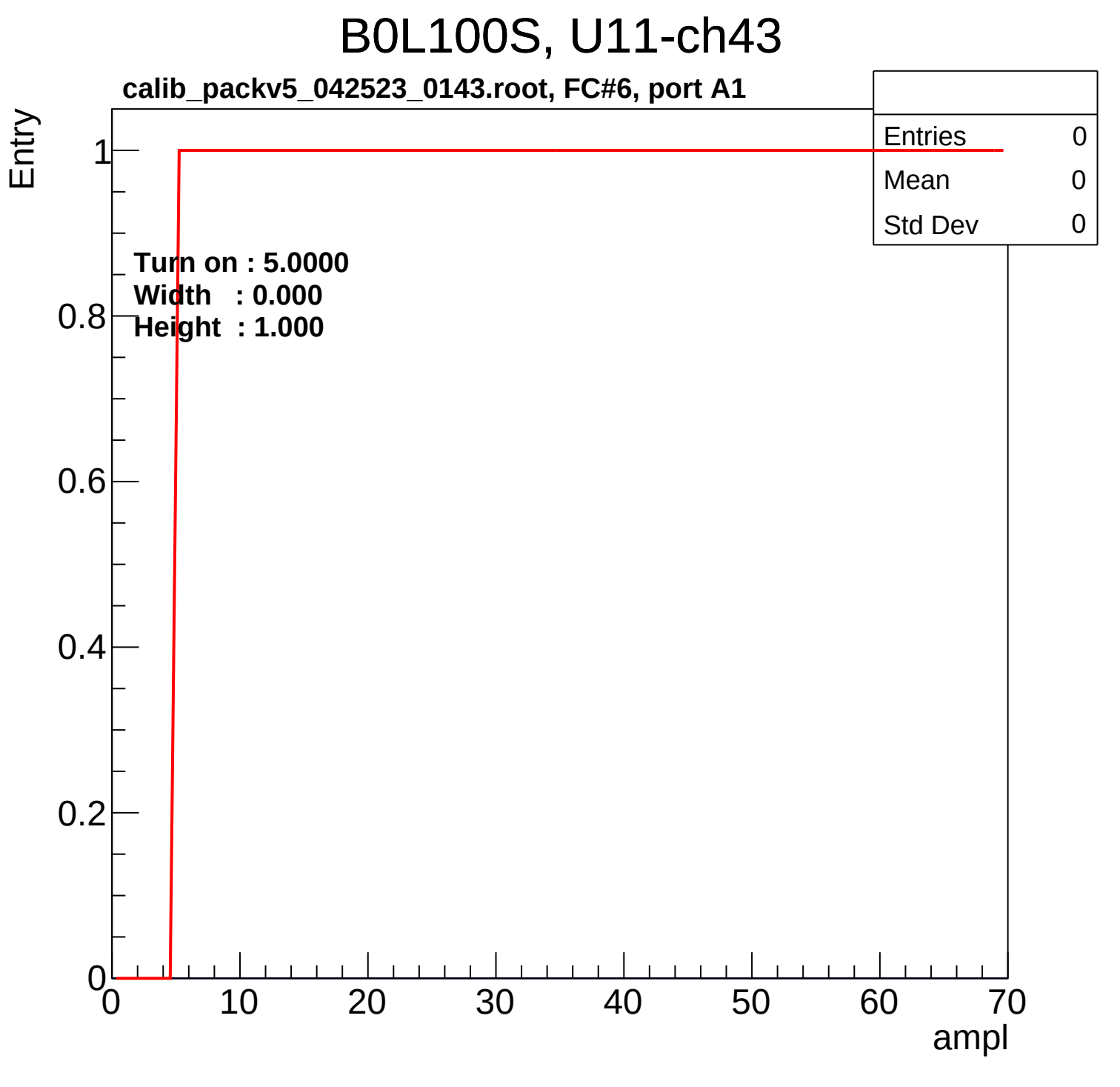
20
30
40
50
60
70

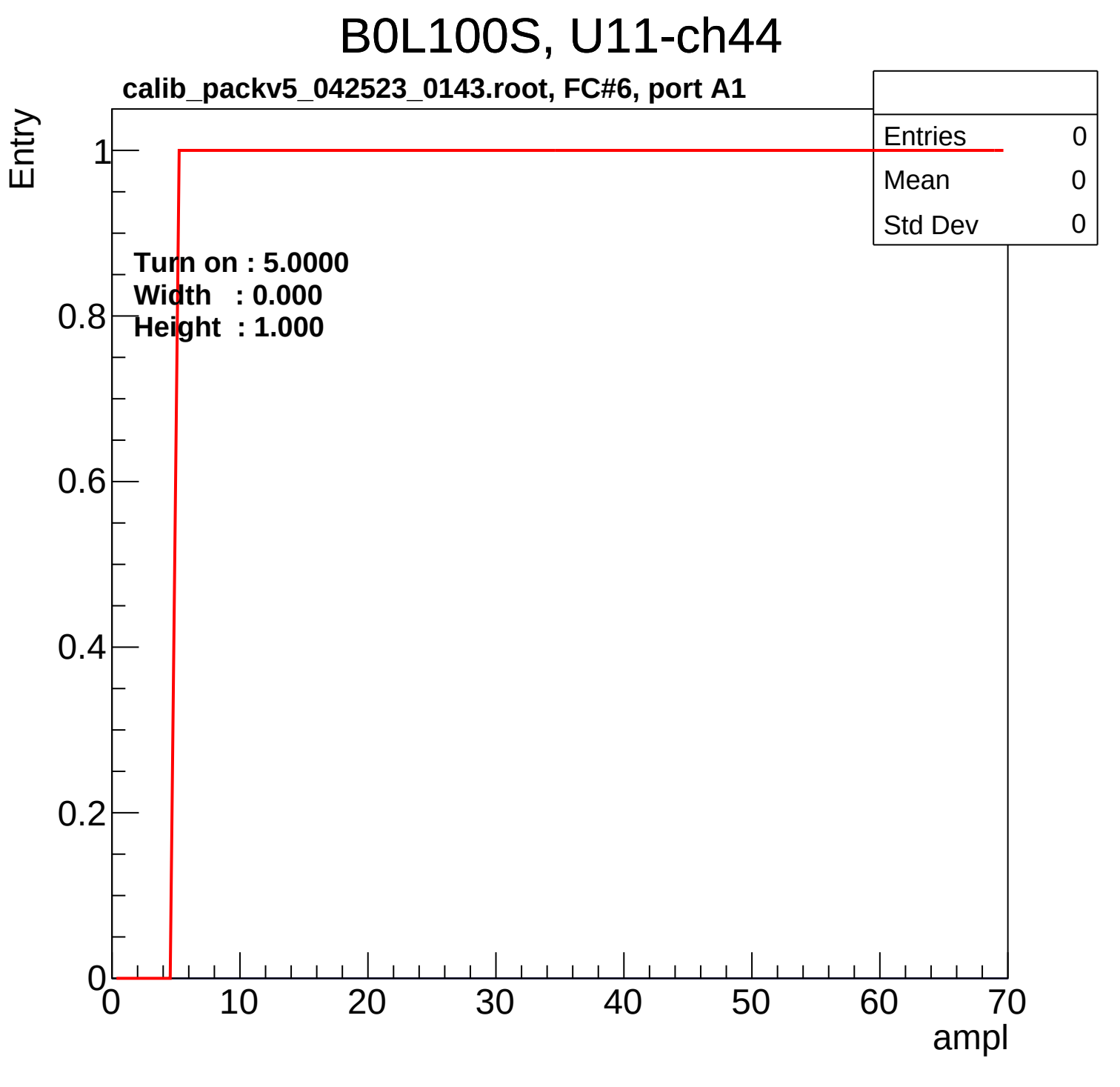

B0L100S, U11-ch39
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

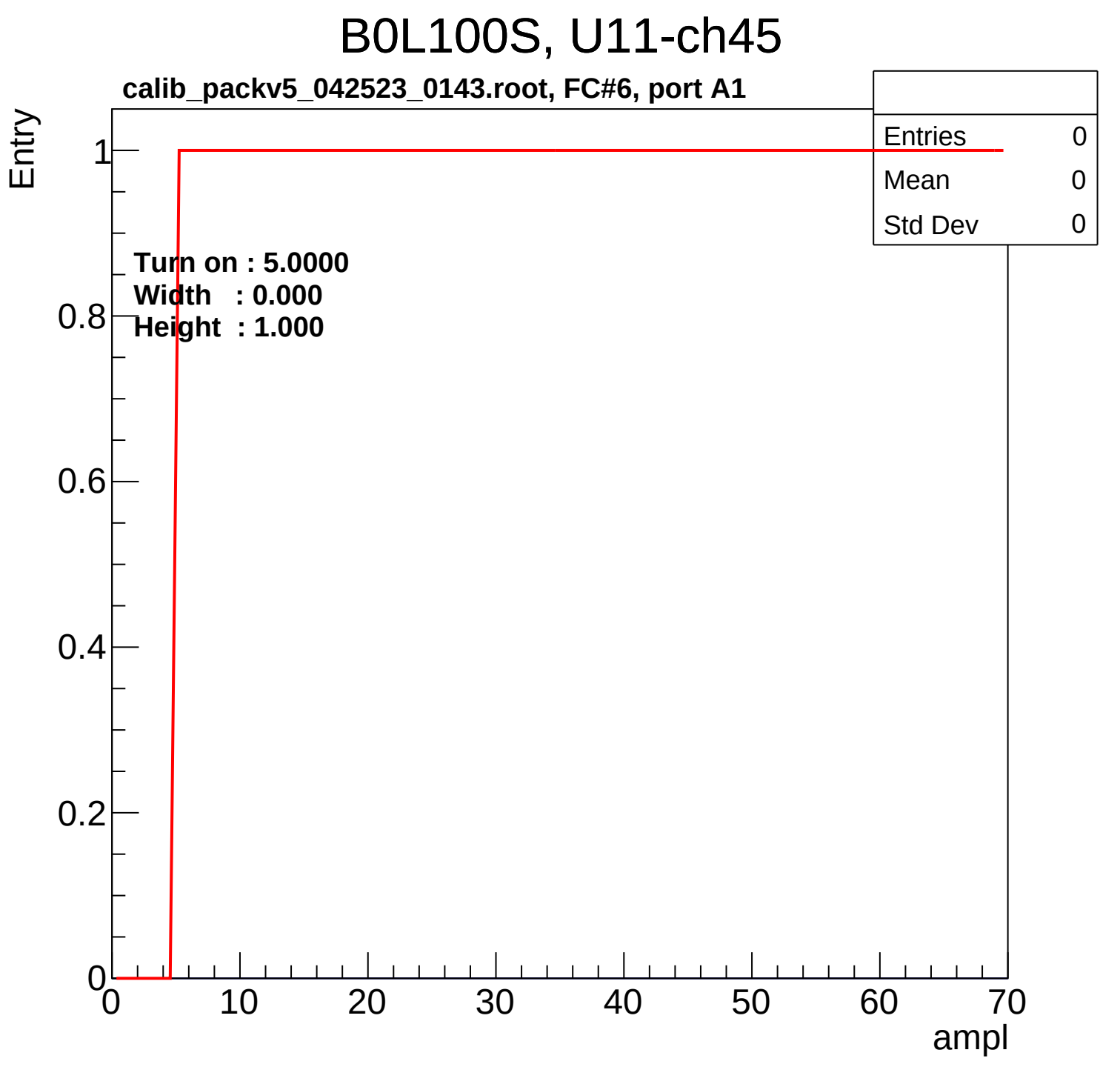

B0L100S, U11-ch40
calib_packv5_042523_0143.root, FC#6, port A1
Entries 36
Mean 51.19
Std Dev 2.686
Turn on : 43.6255
Width : 1.980
Height : 2.333
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

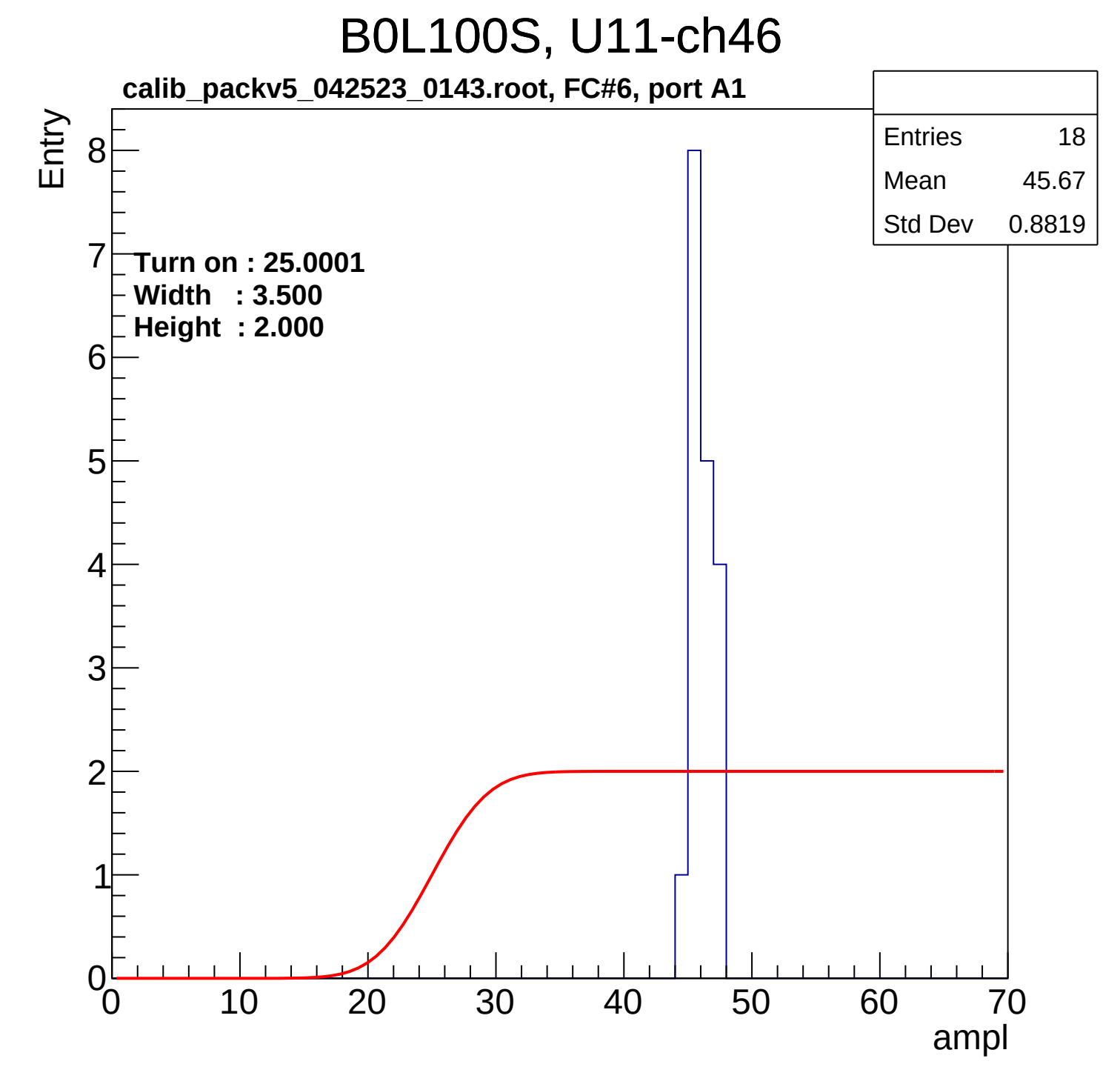

B0L100S, U11-ch41
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U11-ch42
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U11-ch43
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U11-ch44
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U11-ch45
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U11-ch46
calib_packv5_042523_0143.root, FC#6, port A1
Entries 18
Mean 45.67
Std Dev 0.8819
Turn on : 25.0001
Width : 3.500
Height : 2.000
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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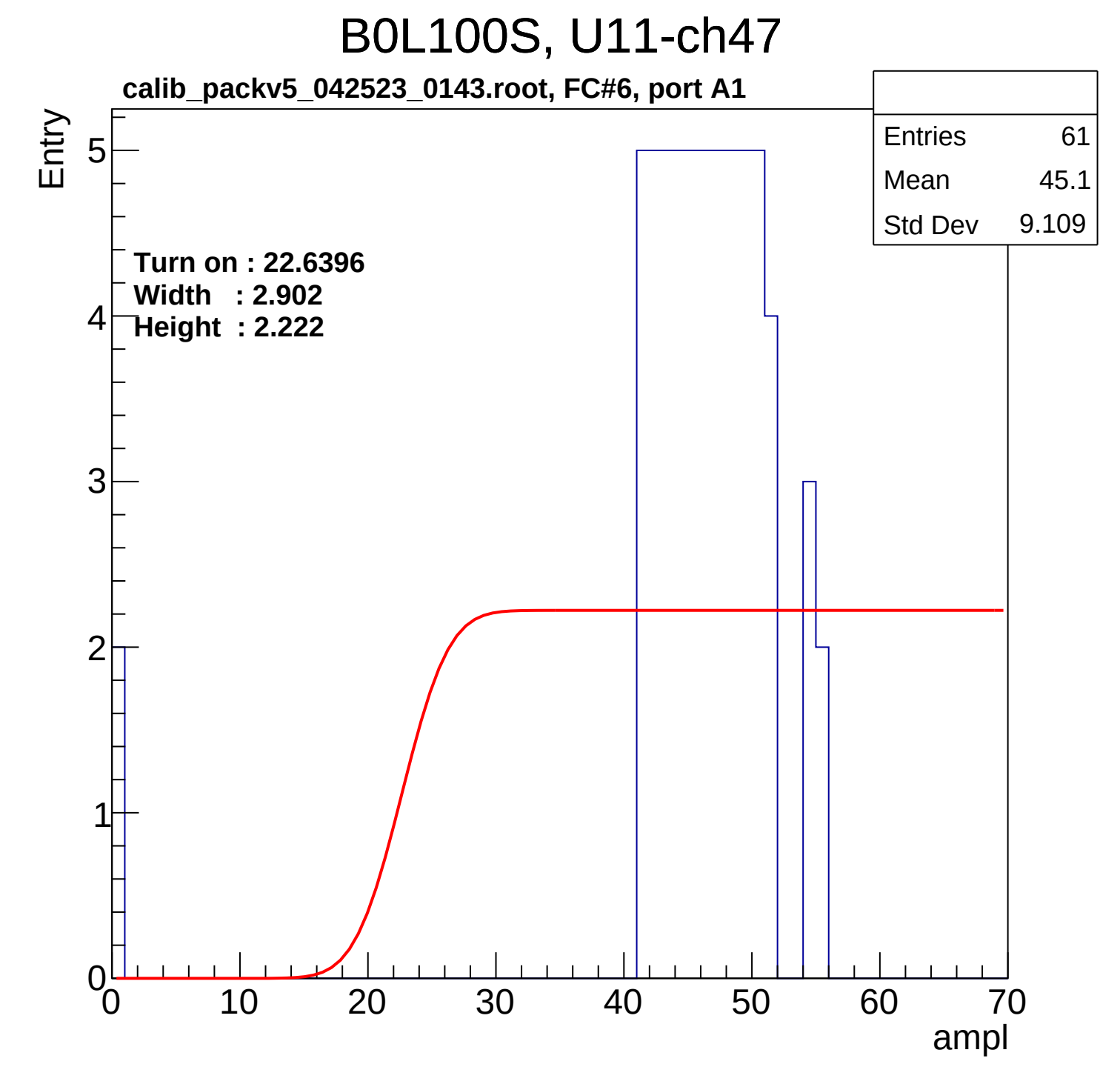
B0L100S, U11-ch47
calib_packv5_042523_0143.root, FC#6, port A1
Entries 61
Mean 45.1
Std Dev 9.109
Turn on : 22.6396
Width : 2.902
Height : 2.222
Entry
ampl
0
1
2
3
4
5
0
10
20
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40
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60
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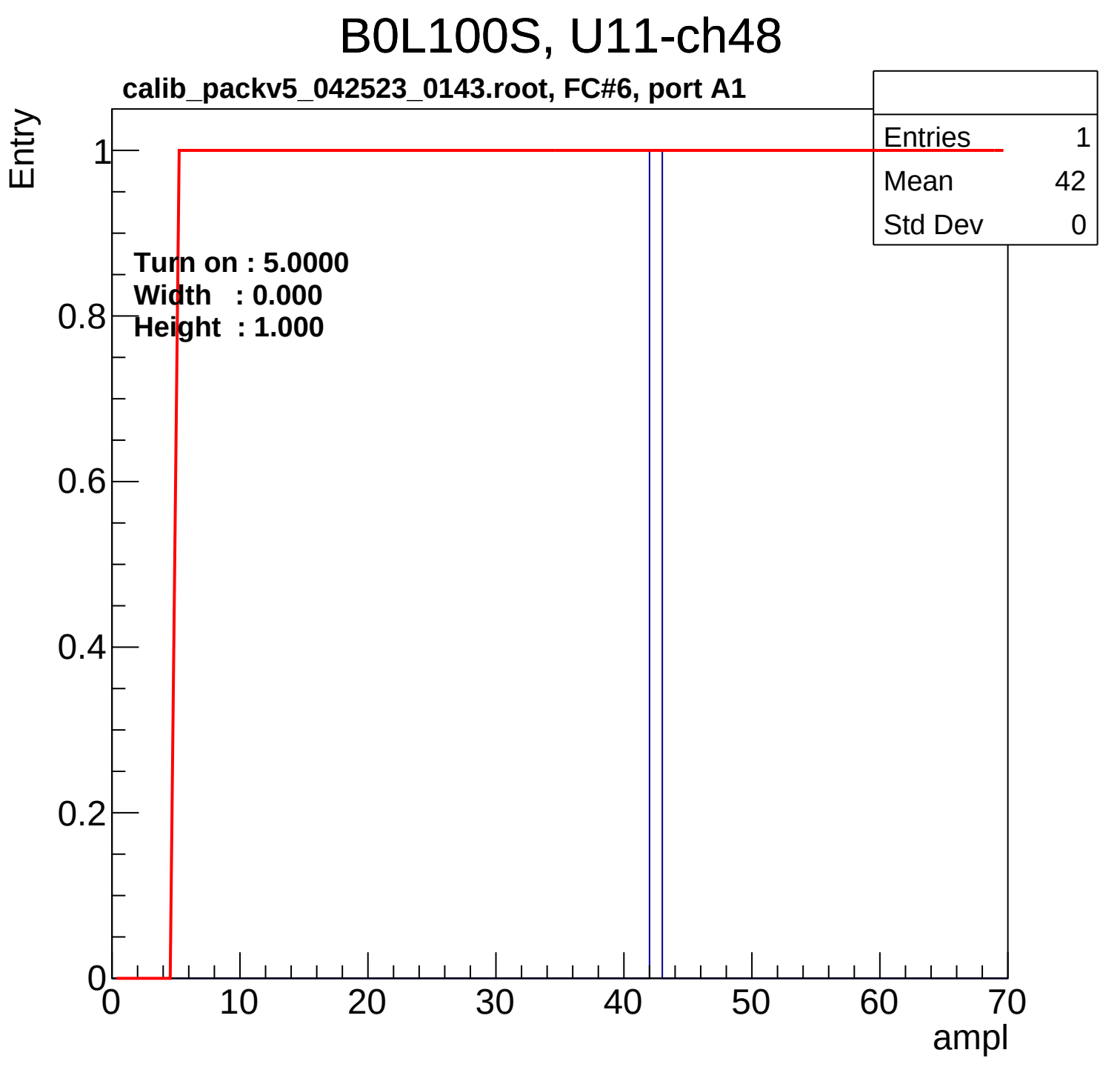
B0L100S, U11-ch48
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 42
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
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0
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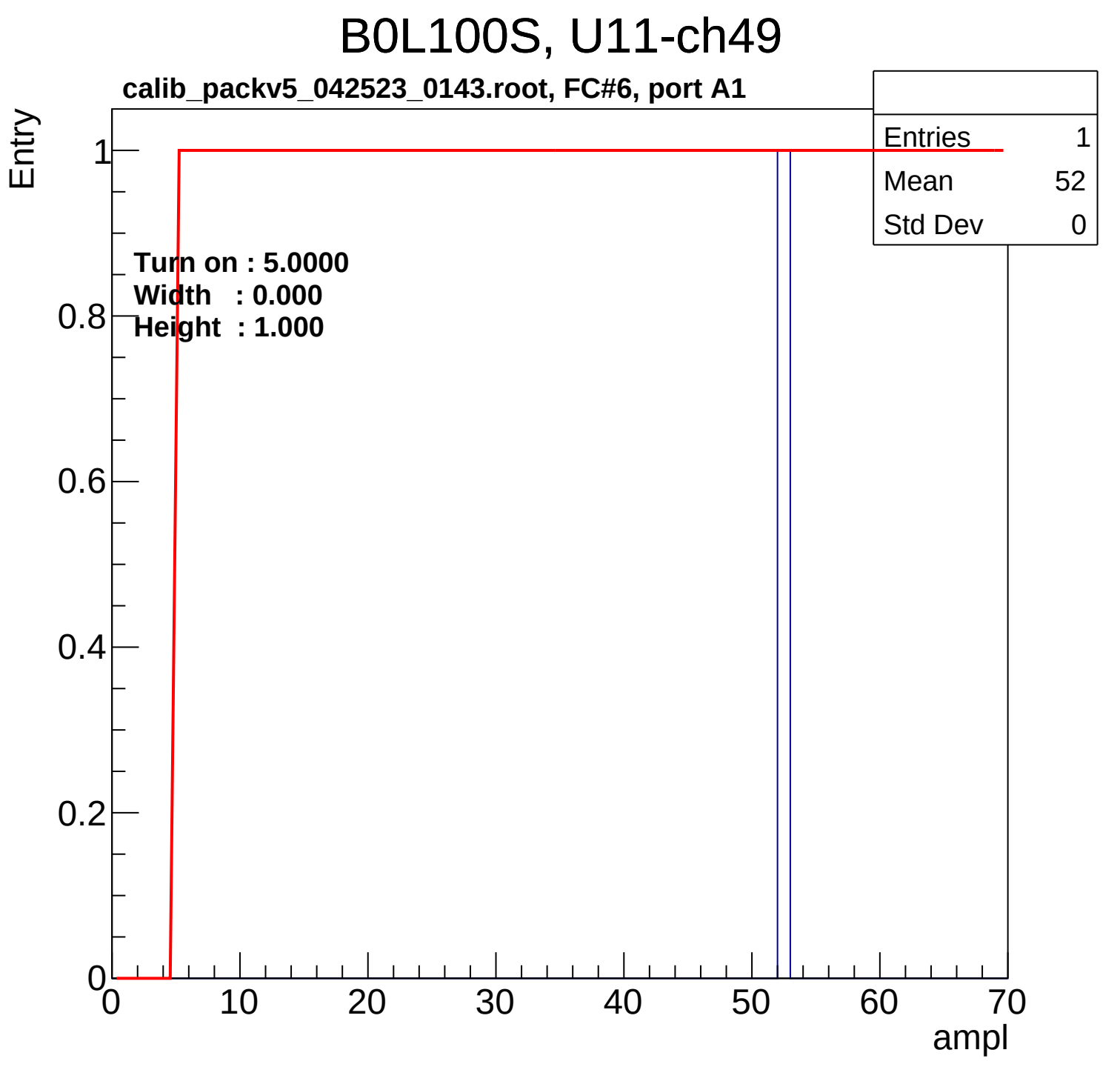
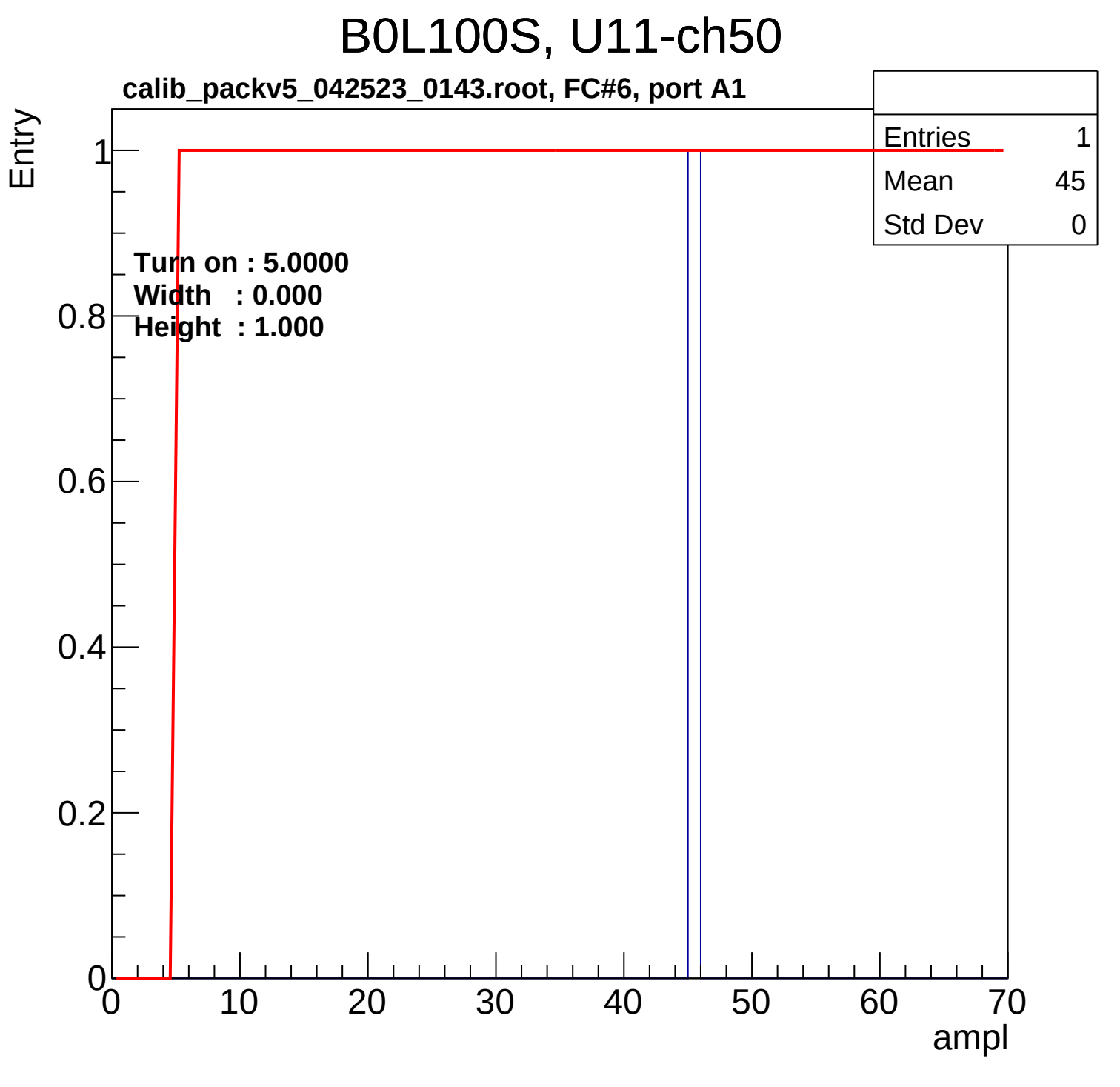
20
30
40
50
60
70


B0L100S, U11-ch49
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 52
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U11-ch50
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 45
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
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20
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60
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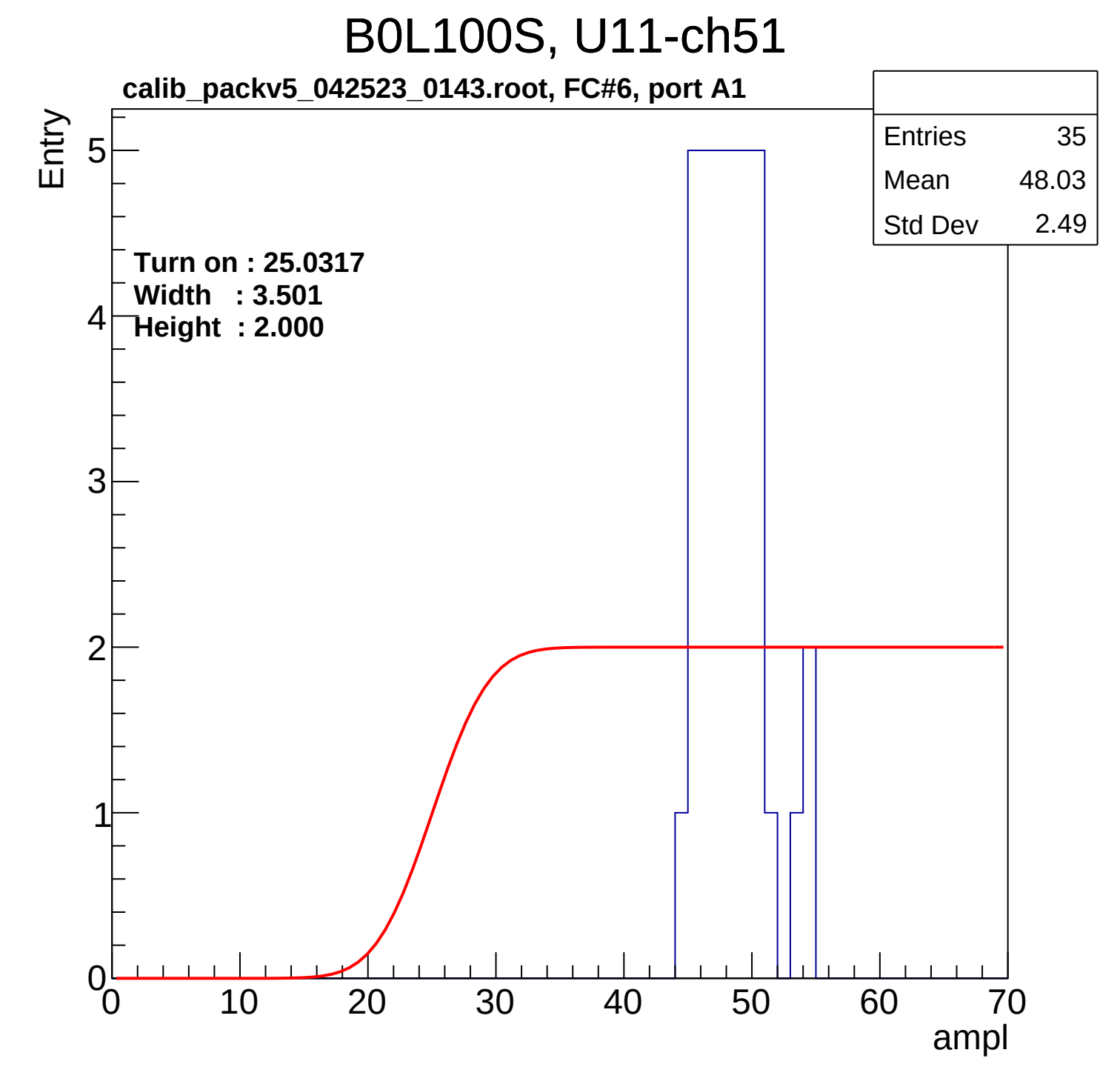
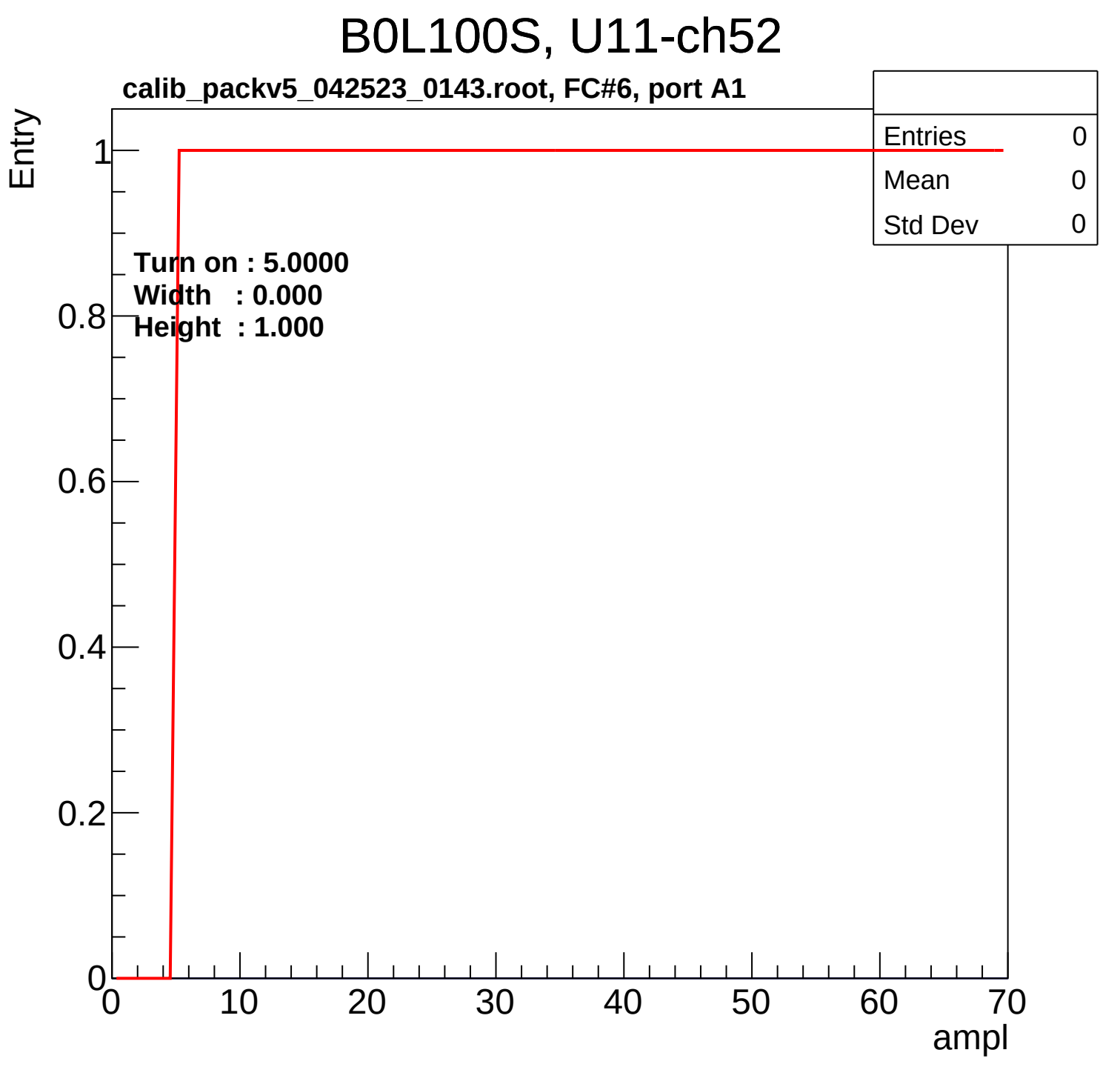
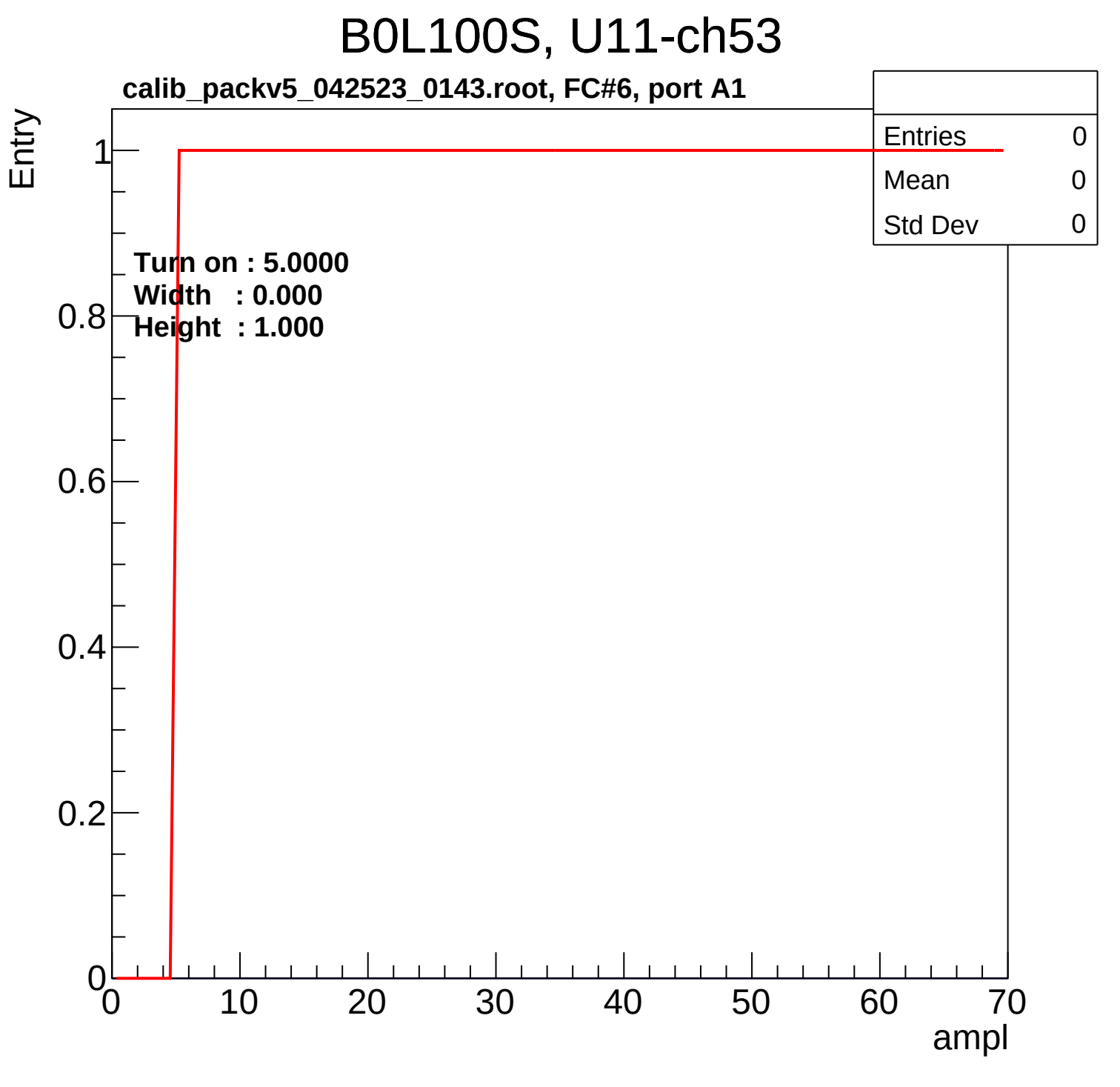

B0L100S, U11-ch51
calib_packv5_042523_0143.root, FC#6, port A1
Entries 35
Mean 48.03
Std Dev 2.49
Turn on : 25.0317
Width : 3.501
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U11-ch52
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U11-ch53
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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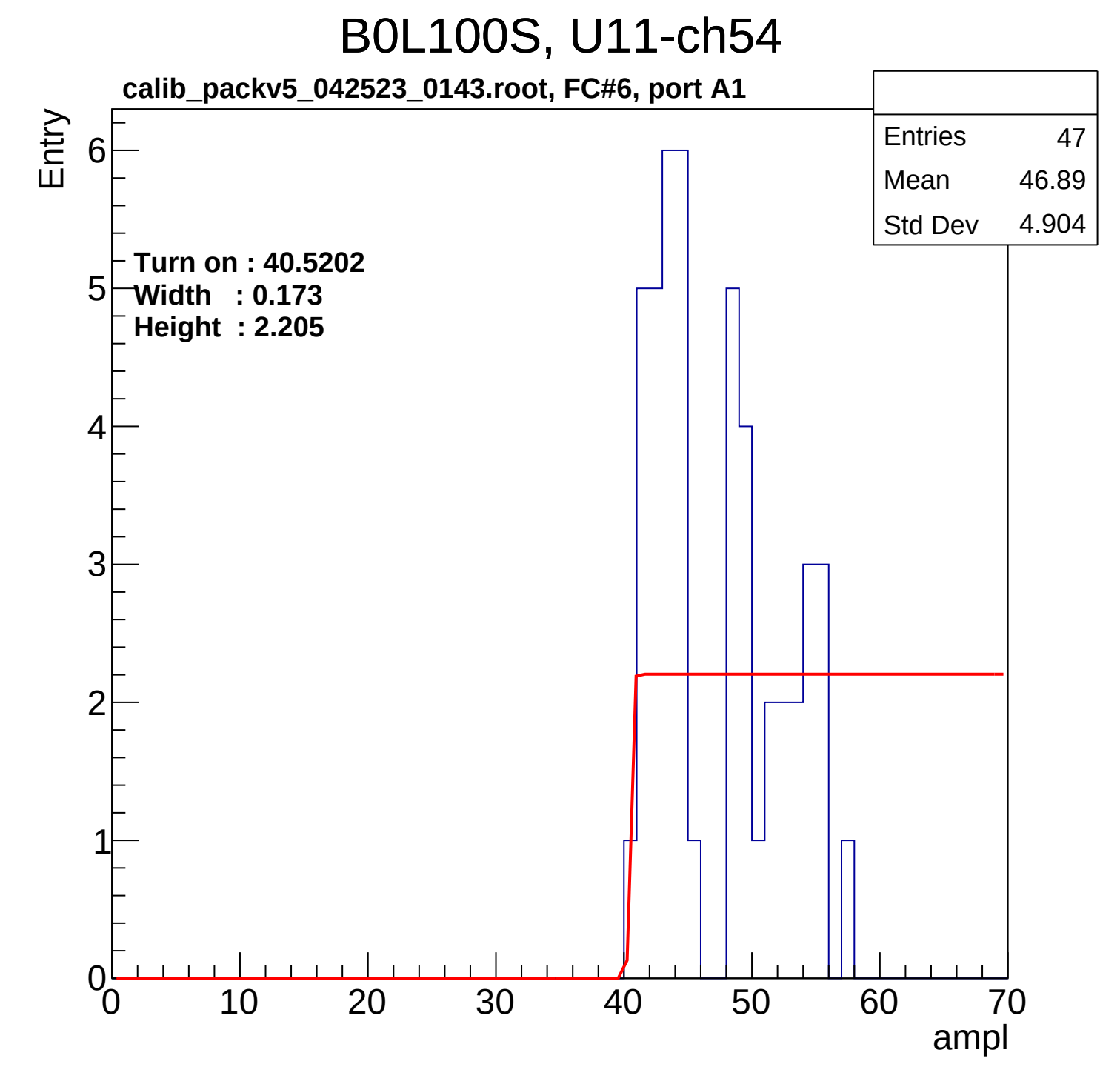
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U11-ch54
calib_packv5_042523_0143.root, FC#6, port A1
Entries 47
Mean 46.89
Std Dev 4.904
Turn on : 40.5202
Width : 0.173
Height : 2.205
Entry
ampl
0
1
2
3
4
5
6
0
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20
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40
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60
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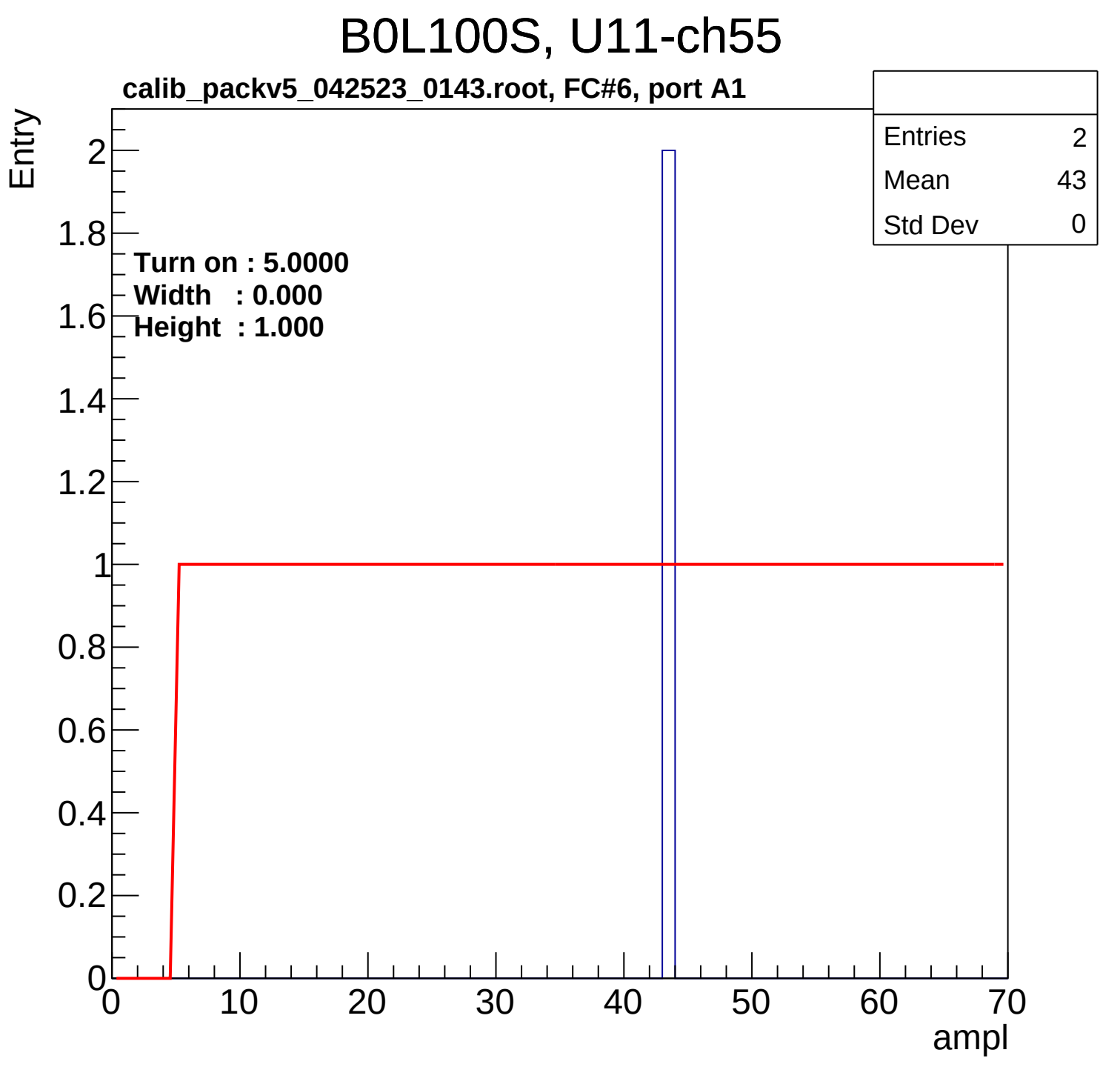
B0L100S, U11-ch55
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 43
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
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60
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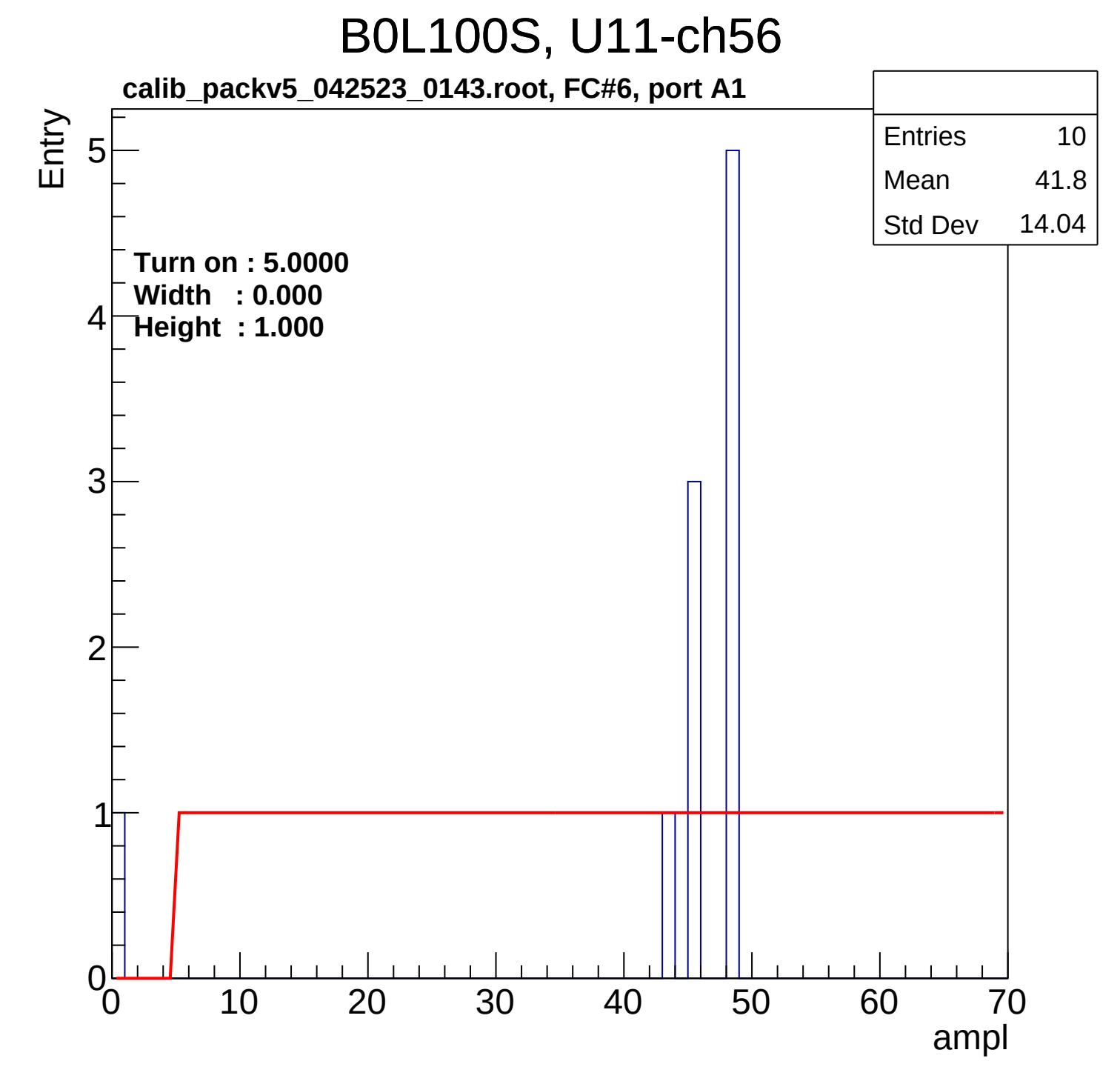
B0L100S, U11-ch56
calib_packv5_042523_0143.root, FC#6, port A1
Entries 10
Mean 41.8
Std Dev 14.04
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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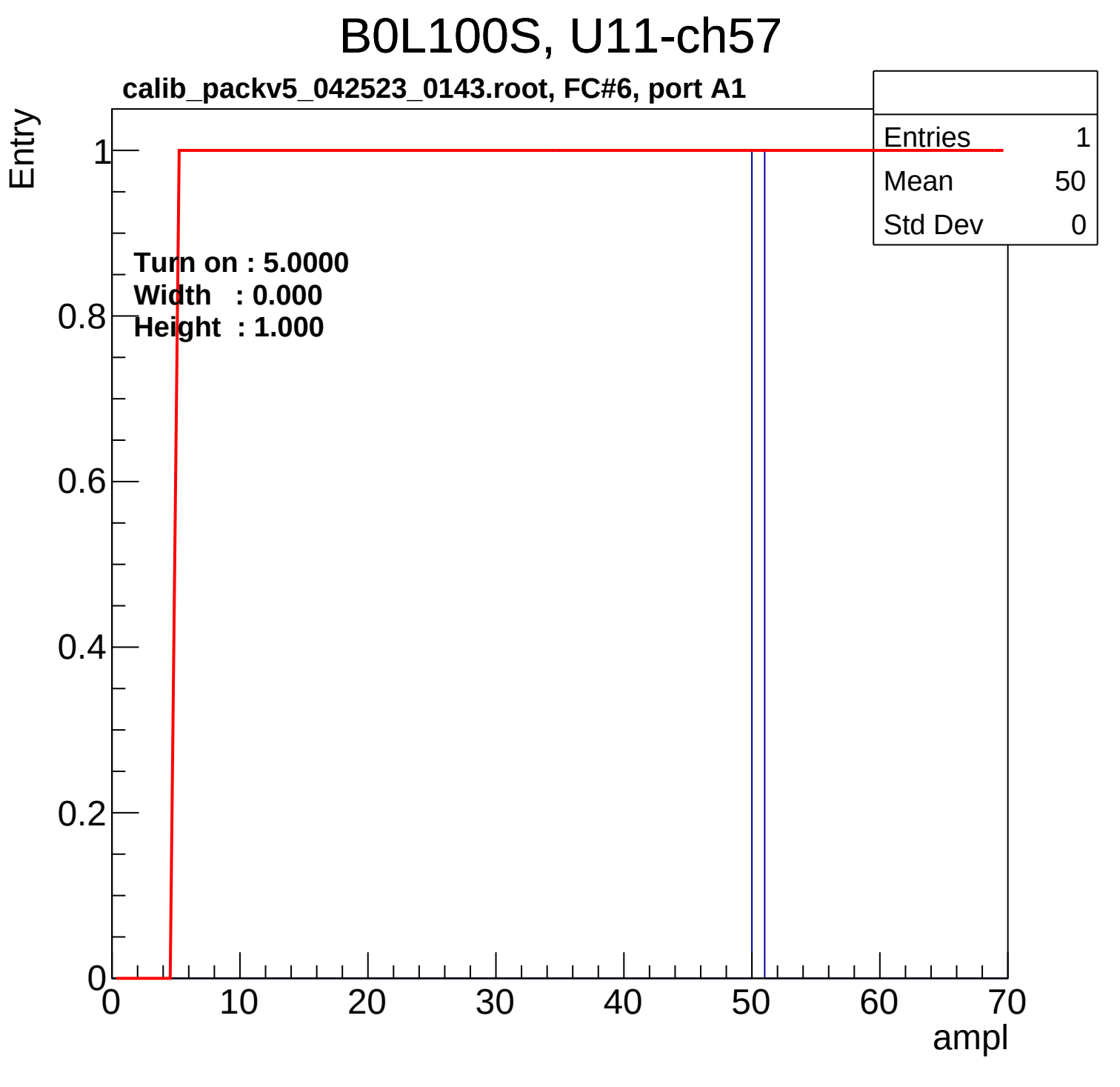
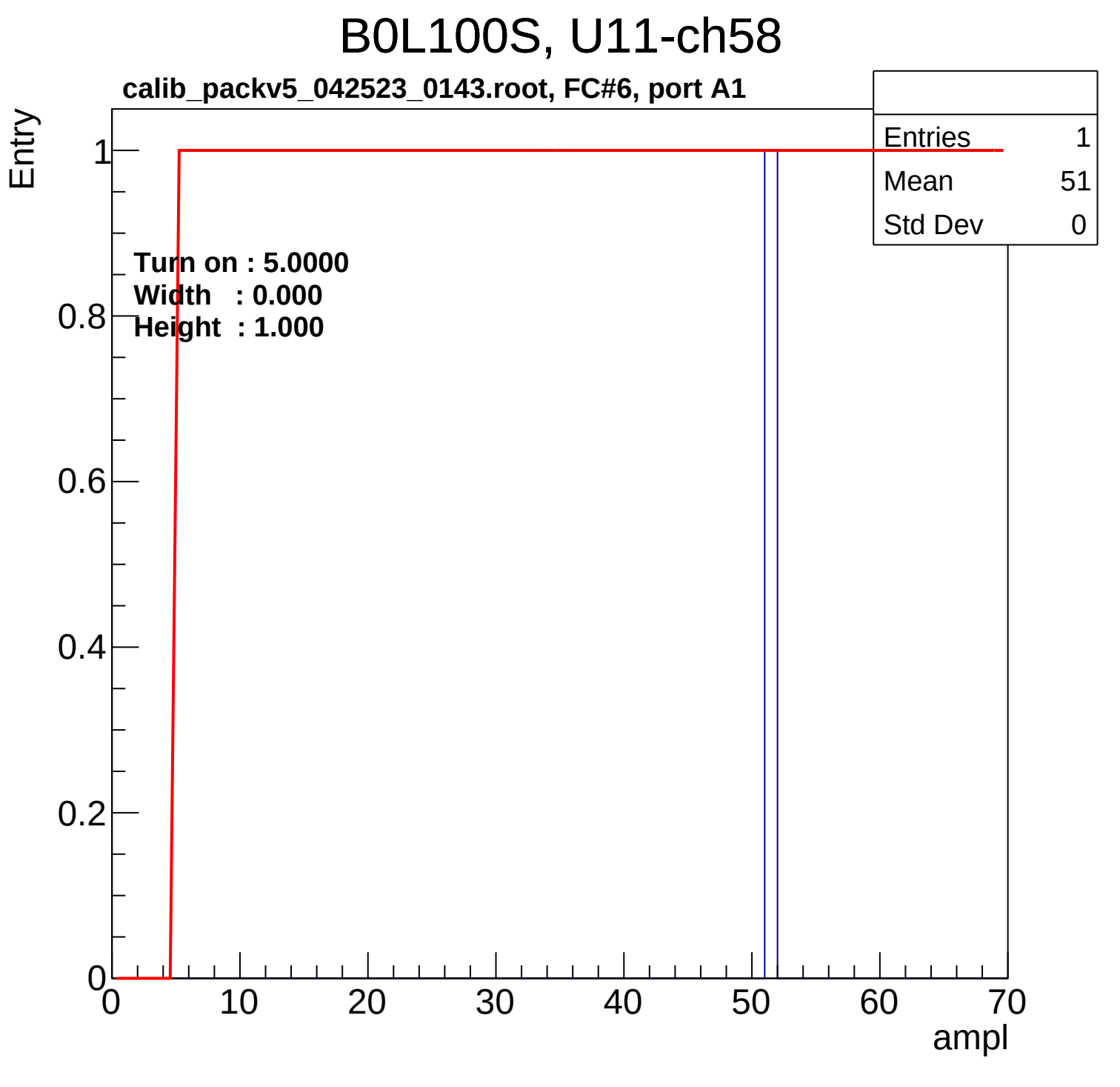

B0L100S, U11-ch57
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 50
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U11-ch58
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 51
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.2
0.4
0.6
0.8
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0
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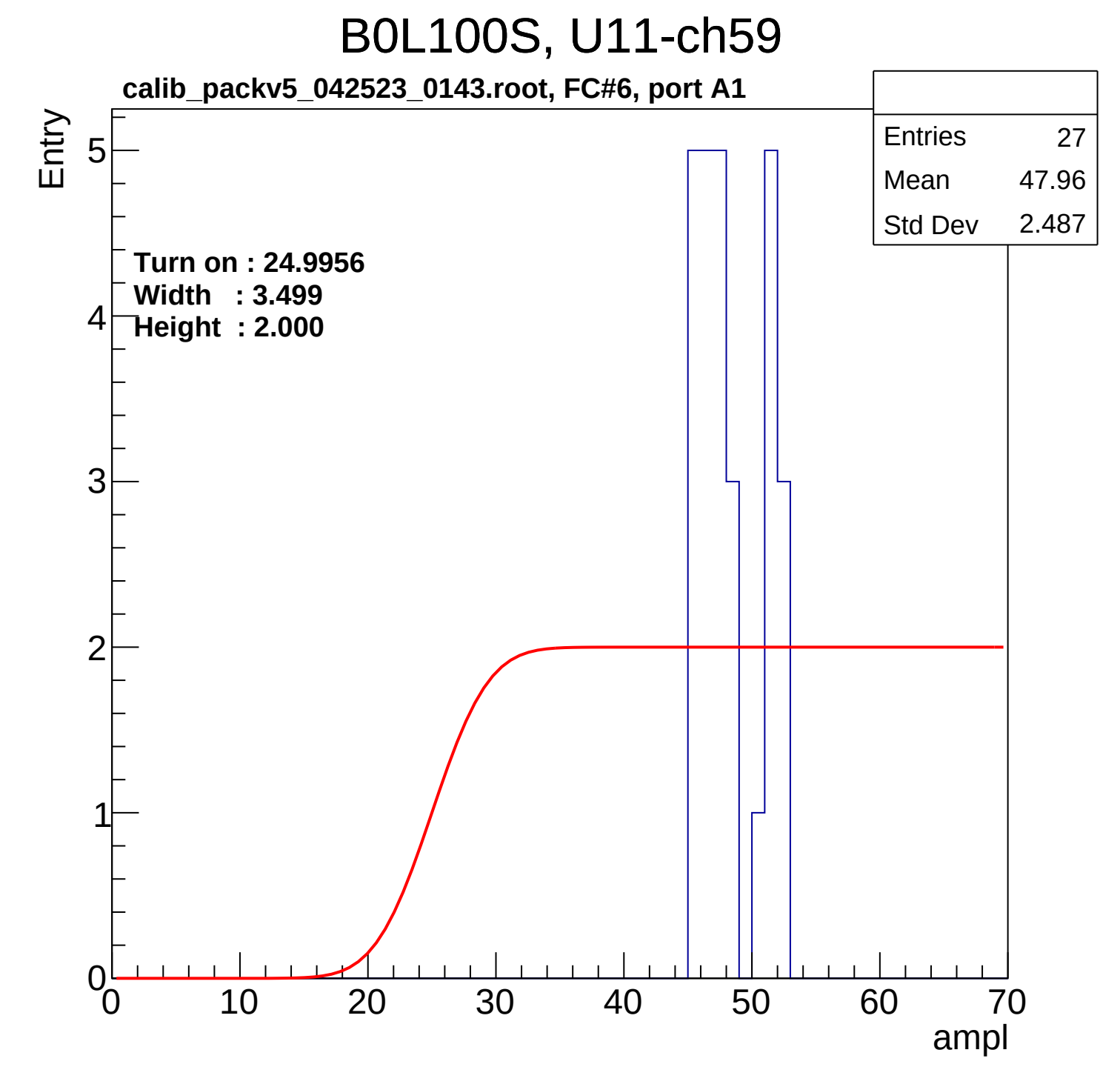
B0L100S, U11-ch59
calib_packv5_042523_0143.root, FC#6, port A1
Entries 27
Mean 47.96
Std Dev 2.487
Turn on : 24.9956
Width : 3.499
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
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40
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60
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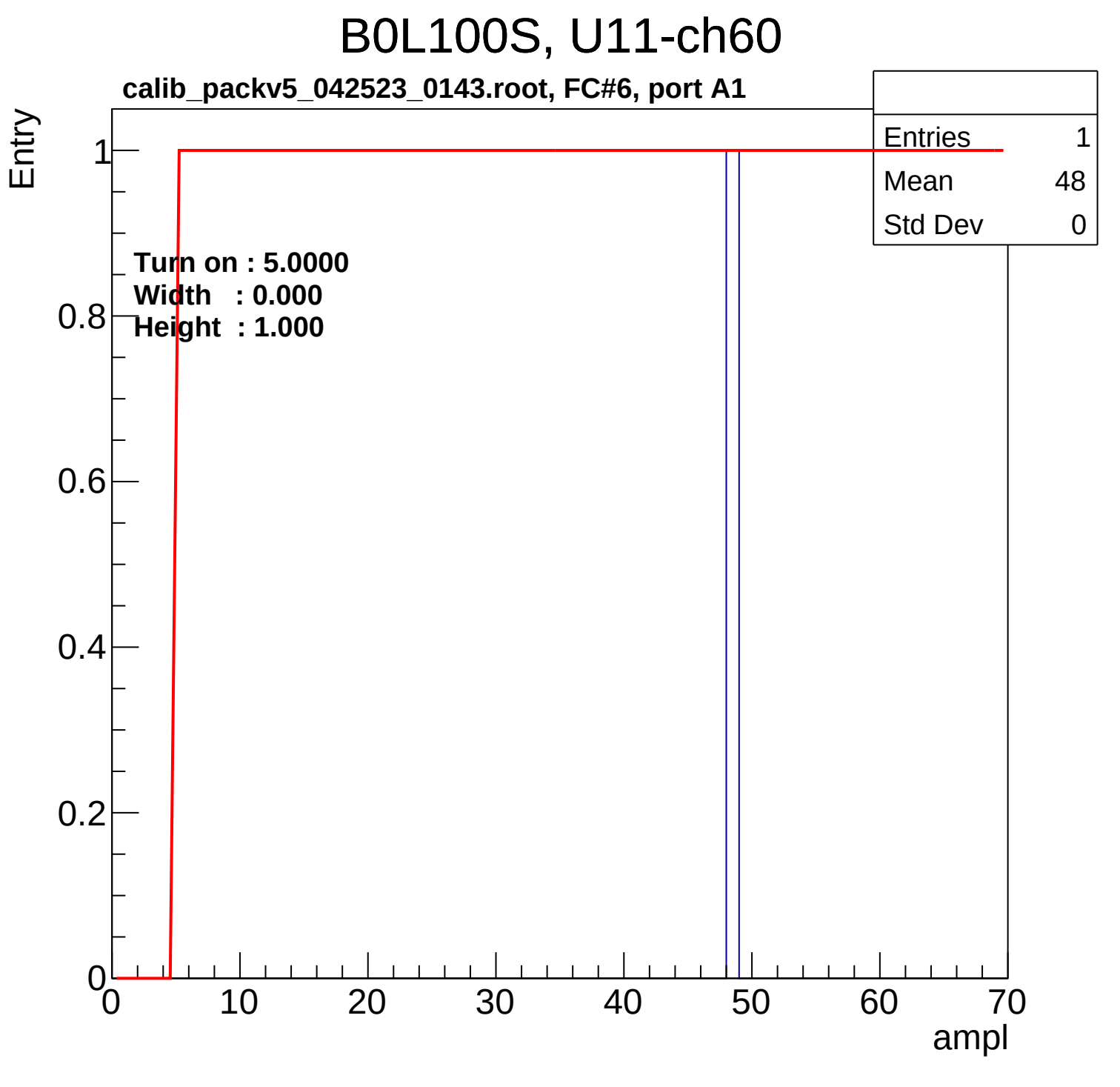
B0L100S, U11-ch60
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 48
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
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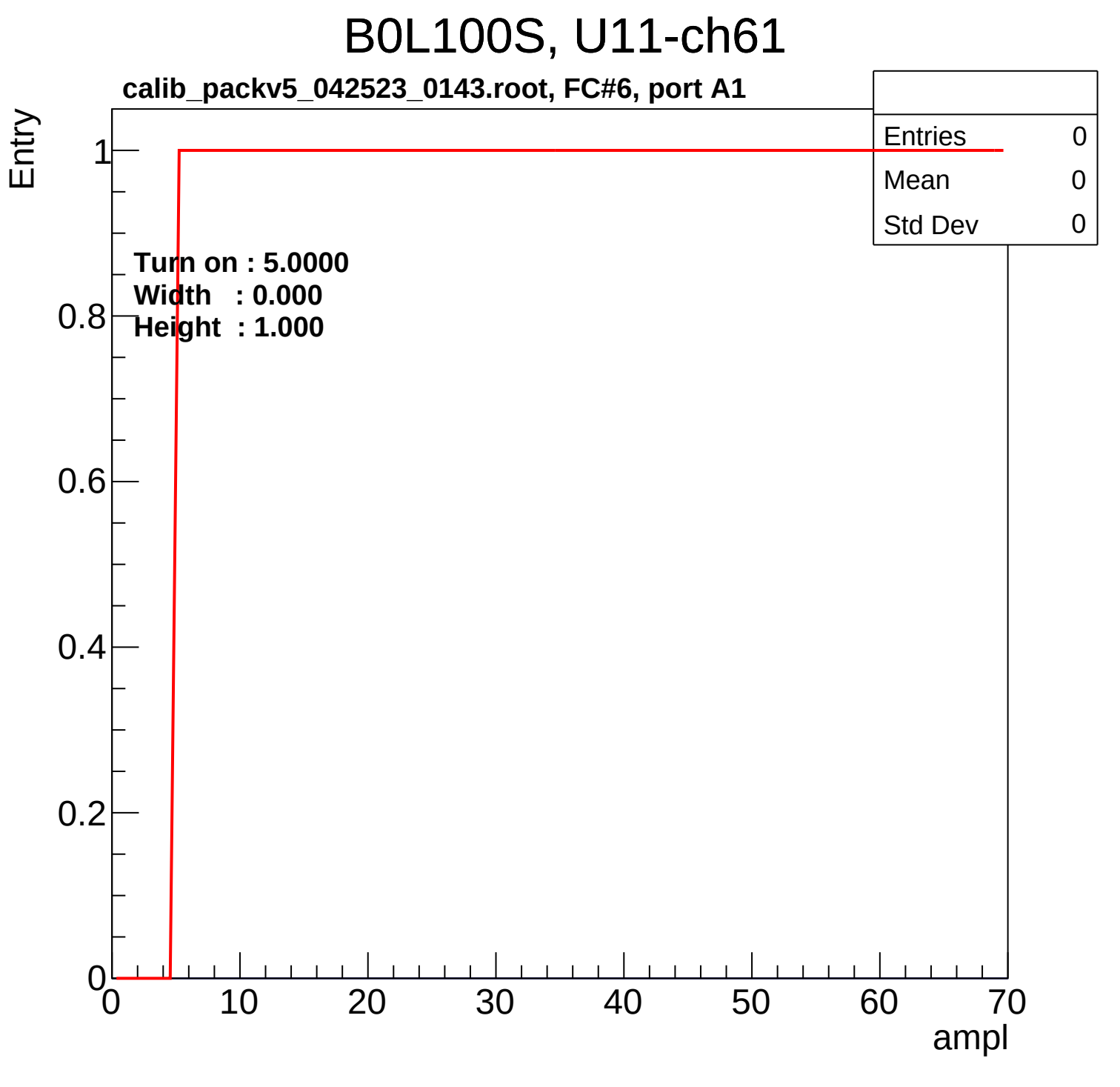
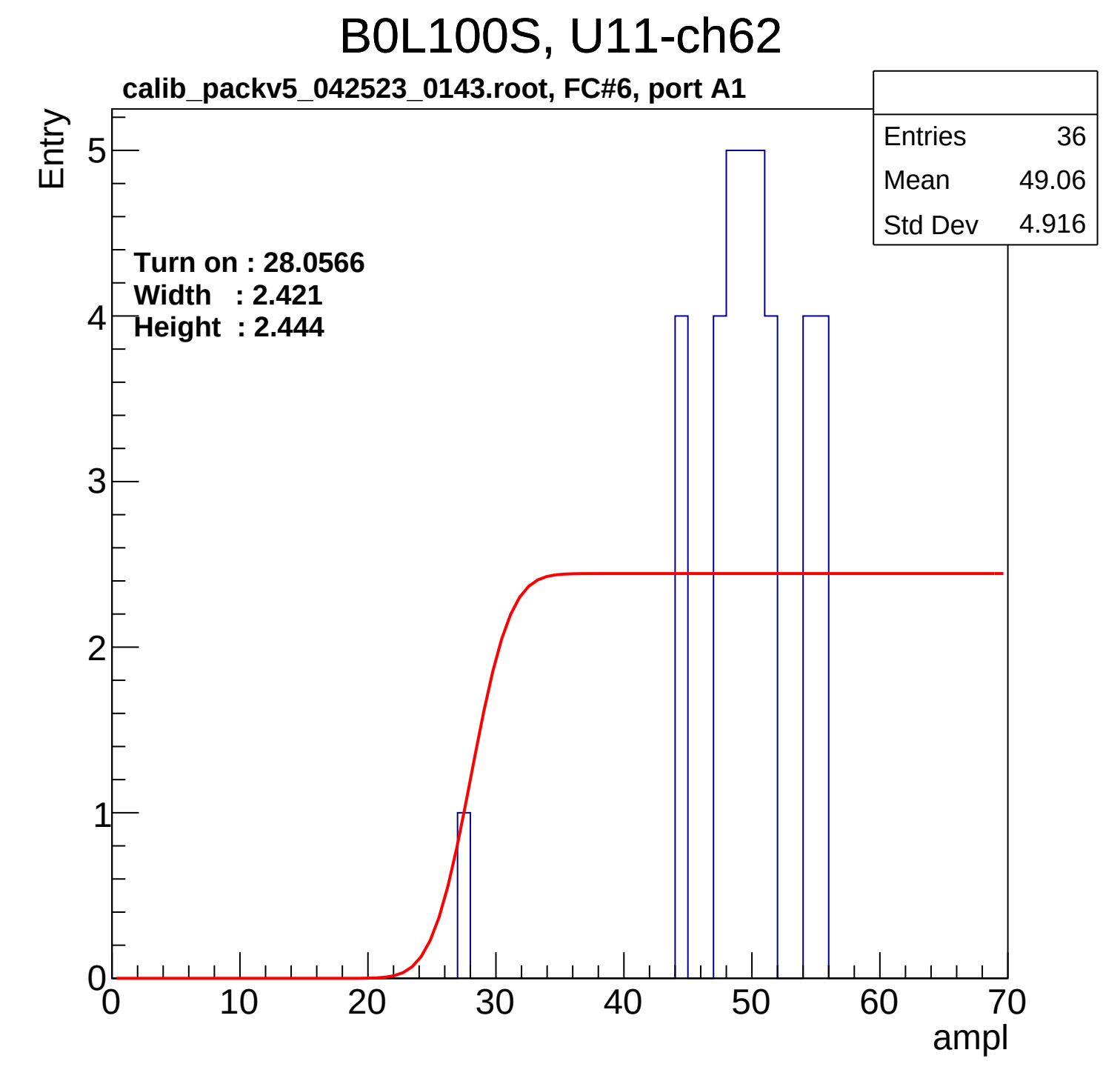

B0L100S, U11-ch61
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U11-ch62
calib_packv5_042523_0143.root, FC#6, port A1
Entries 36
Mean 49.06
Std Dev 4.916
Turn on : 28.0566
Width : 2.421
Height : 2.444
Entry
ampl
0
1
2
3
4
5
0
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20
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40
50
60
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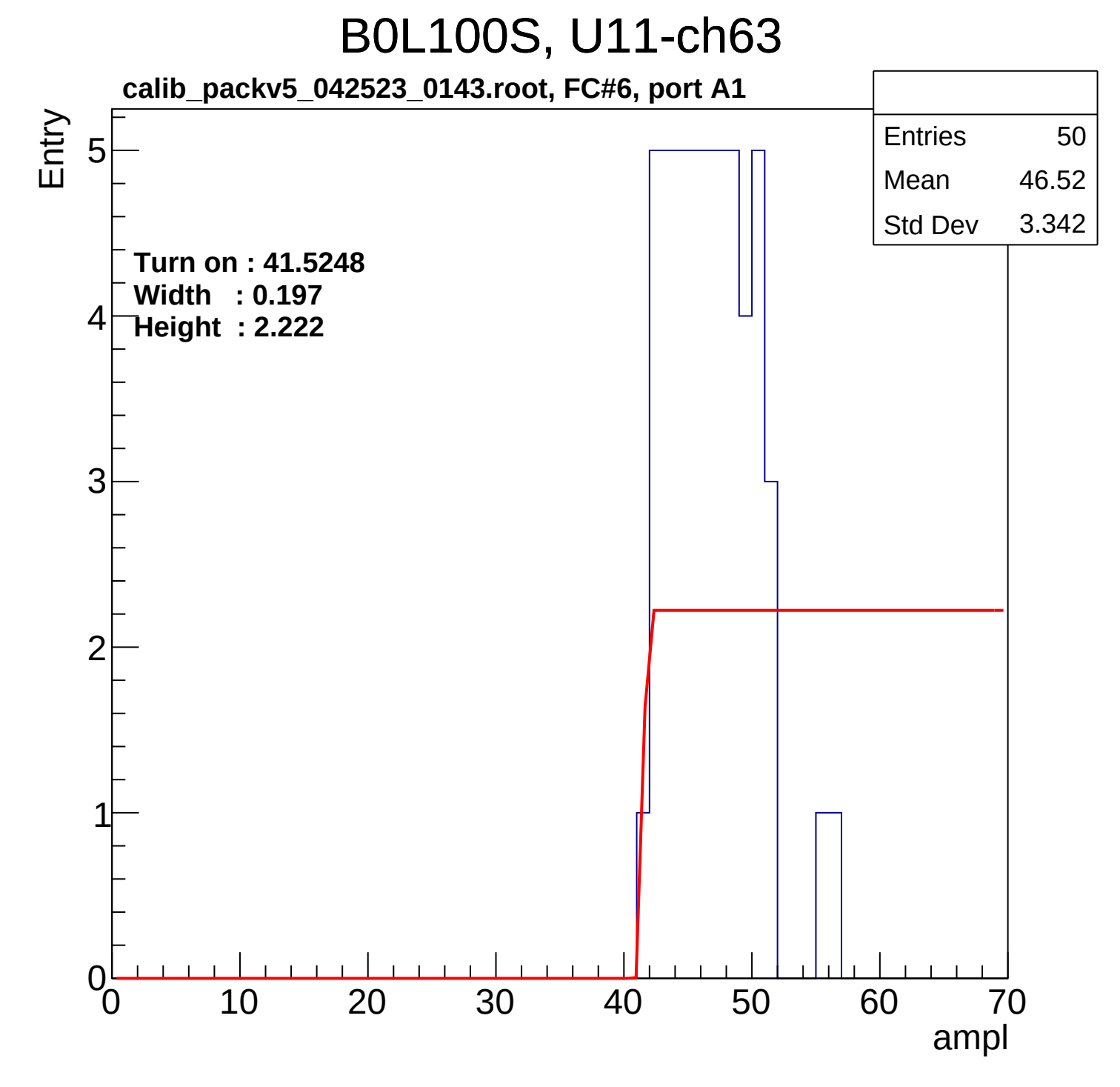
B0L100S, U11-ch63
calib_packv5_042523_0143.root, FC#6, port A1
Entries 50
Mean 46.52
Std Dev 3.342
Turn on : 41.5248
Width : 0.197
Height : 2.222
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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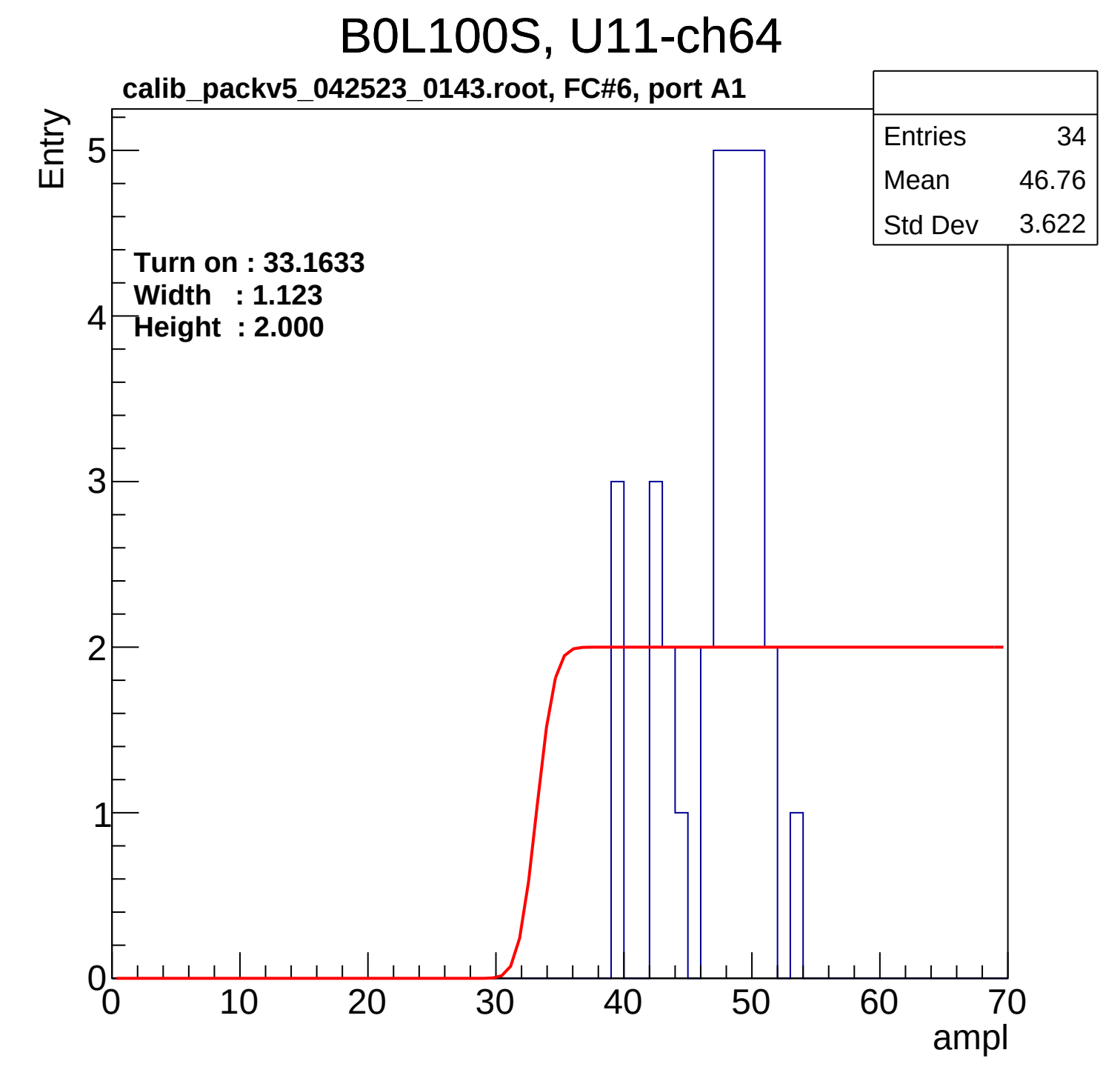
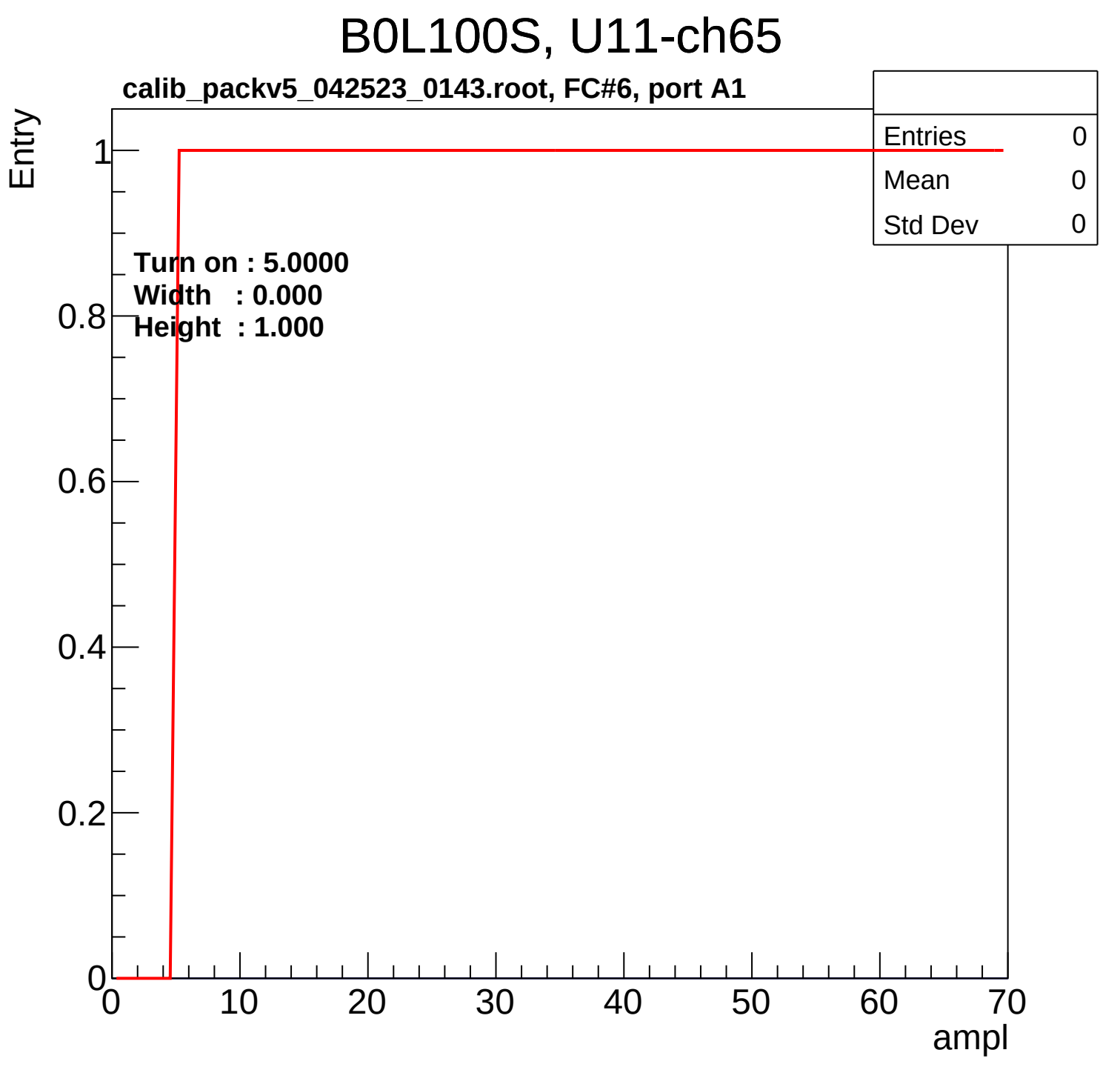
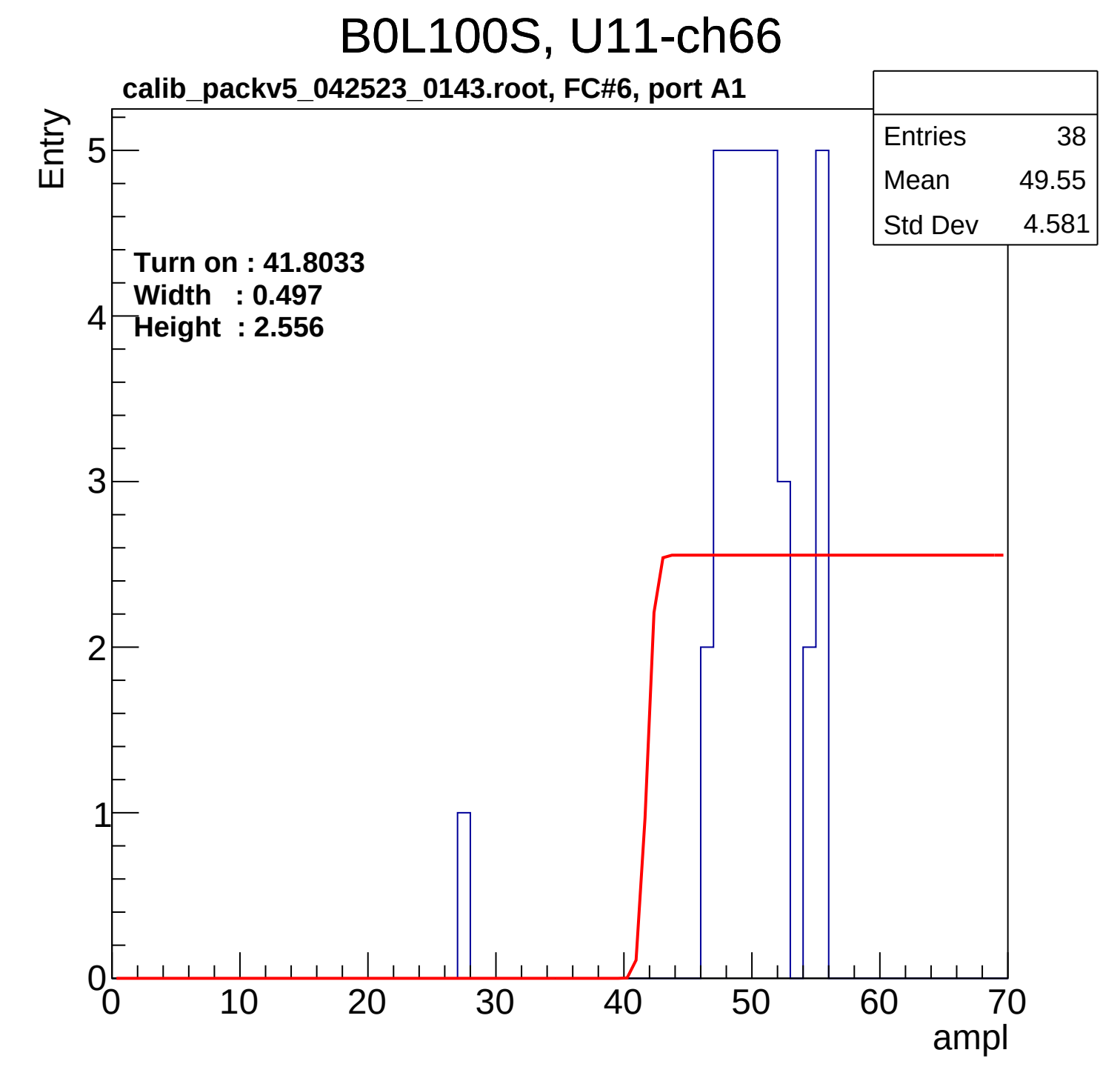
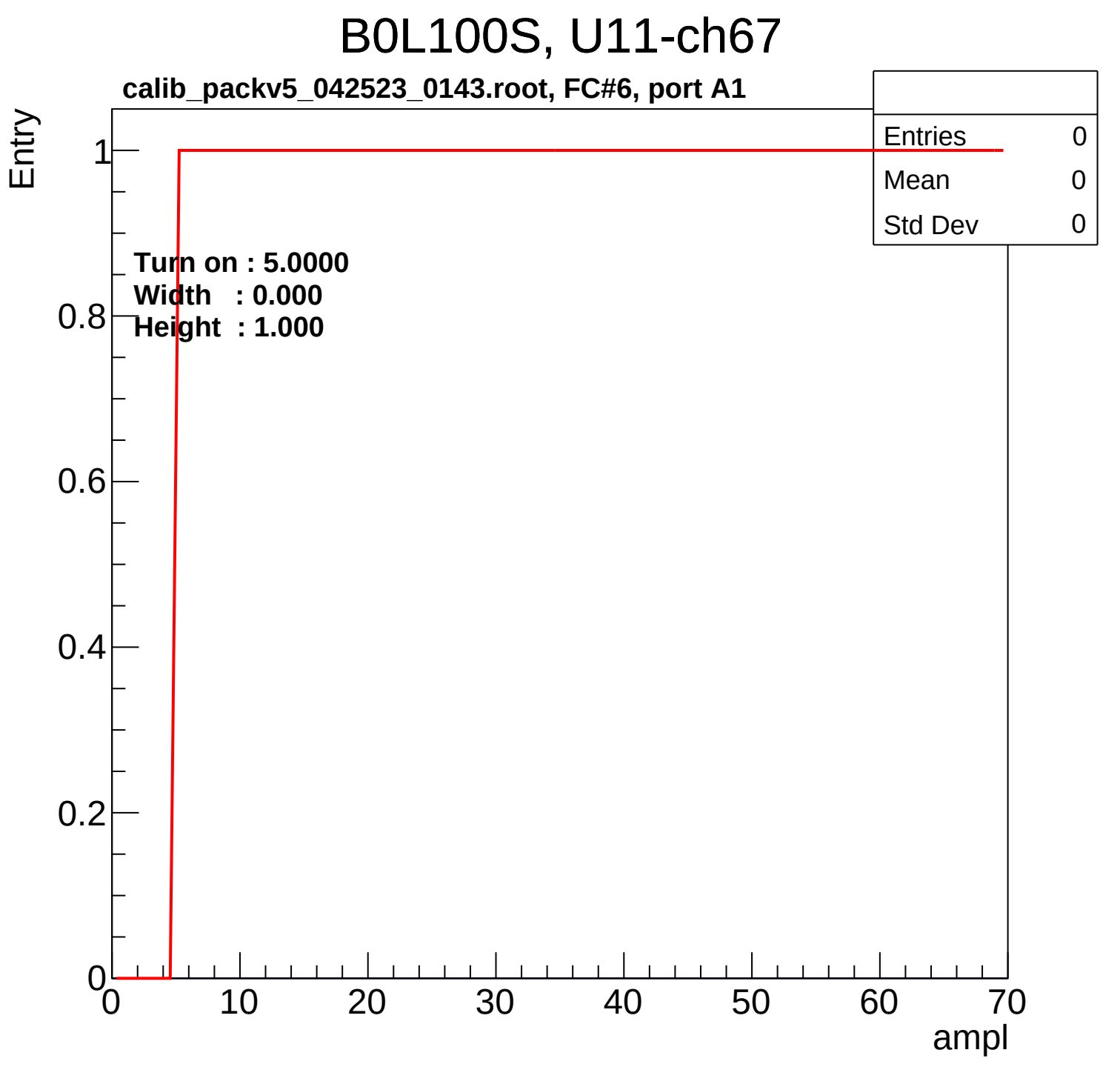
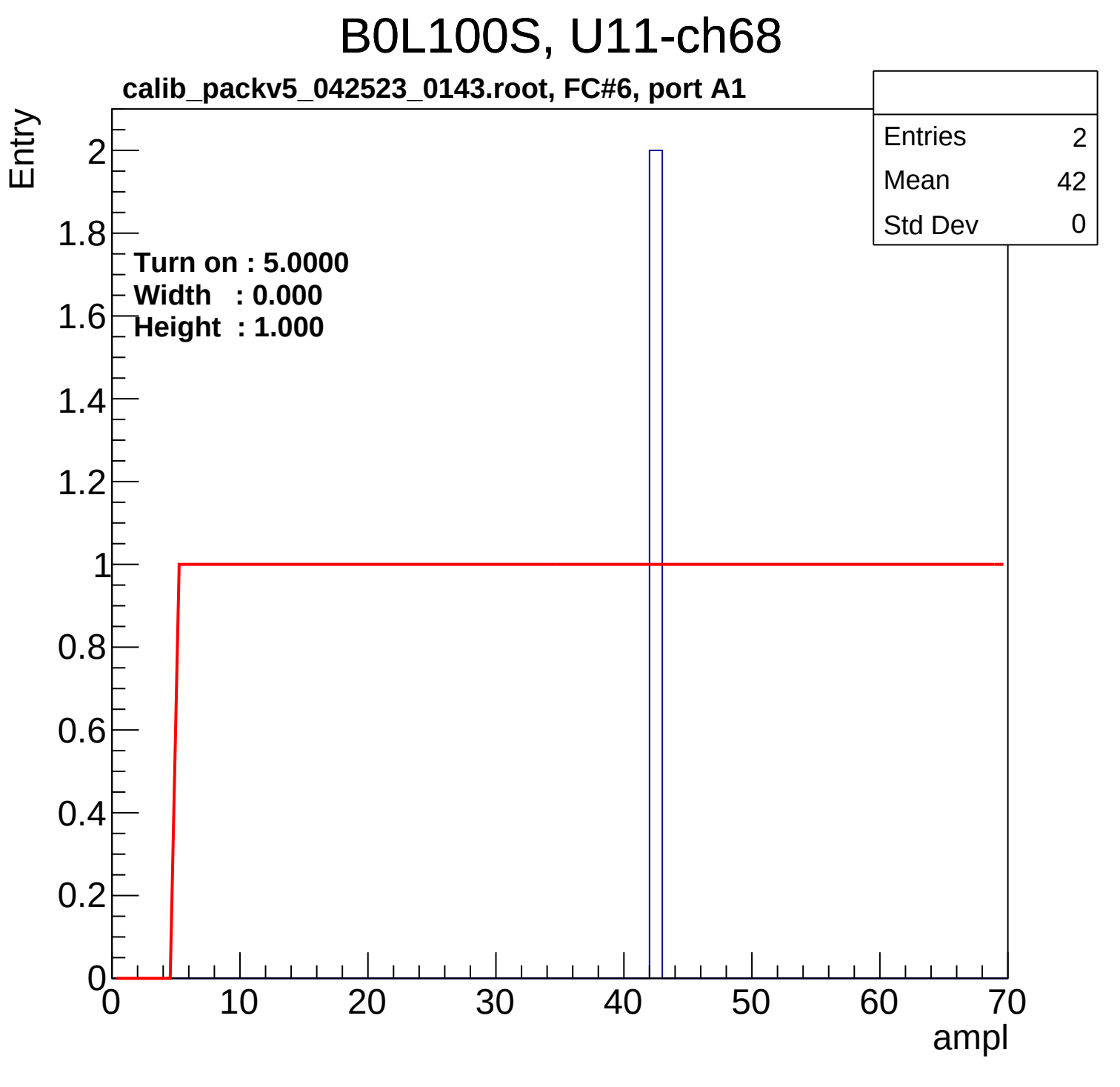
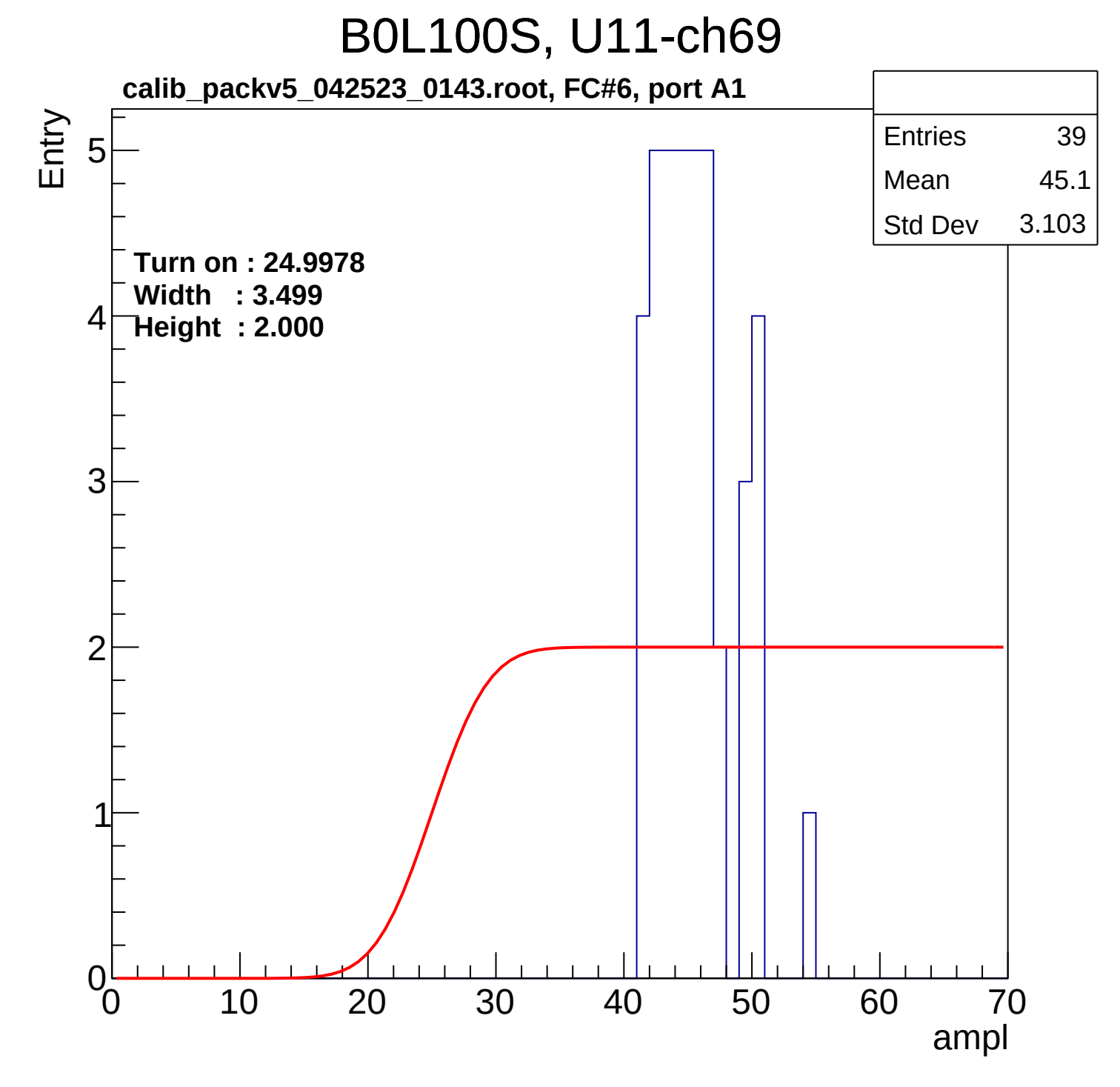

B0L100S, U11-ch64
calib_packv5_042523_0143.root, FC#6, port A1
Entries 34
Mean 46.76
Std Dev 3.622
Turn on : 33.1633
Width : 1.123
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

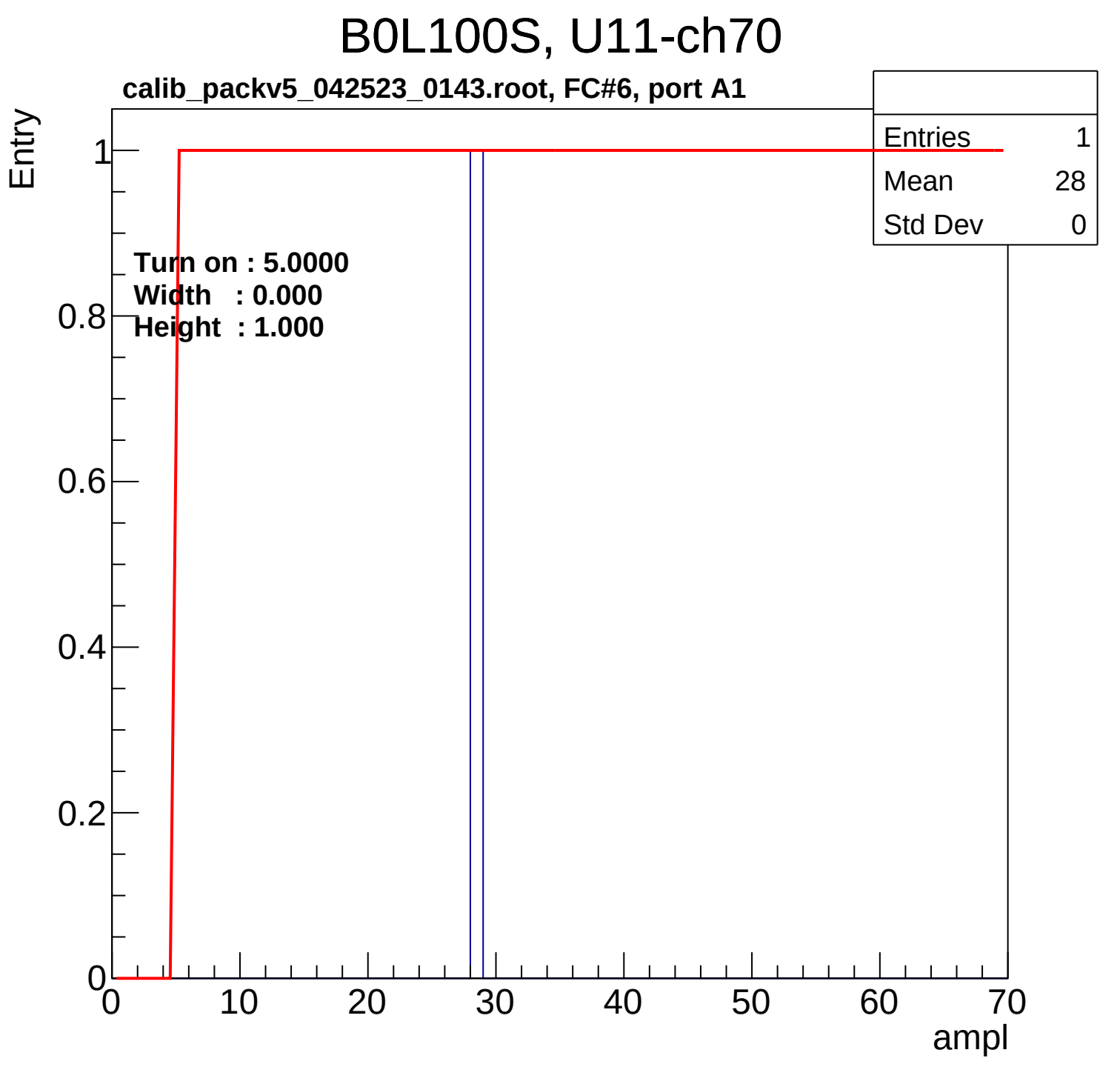

B0L100S, U11-ch65
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U11-ch66
calib_packv5_042523_0143.root, FC#6, port A1
Entries 38
Mean 49.55
Std Dev 4.581
Turn on : 41.8033
Width : 0.497
Height : 2.556
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U11-ch67
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U11-ch68
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 42
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L100S, U11-ch69
calib_packv5_042523_0143.root, FC#6, port A1
Entries 39
Mean 45.1
Std Dev 3.103
Turn on : 24.9978
Width : 3.499
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U11-ch70
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 28
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
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20
30
40
50
60
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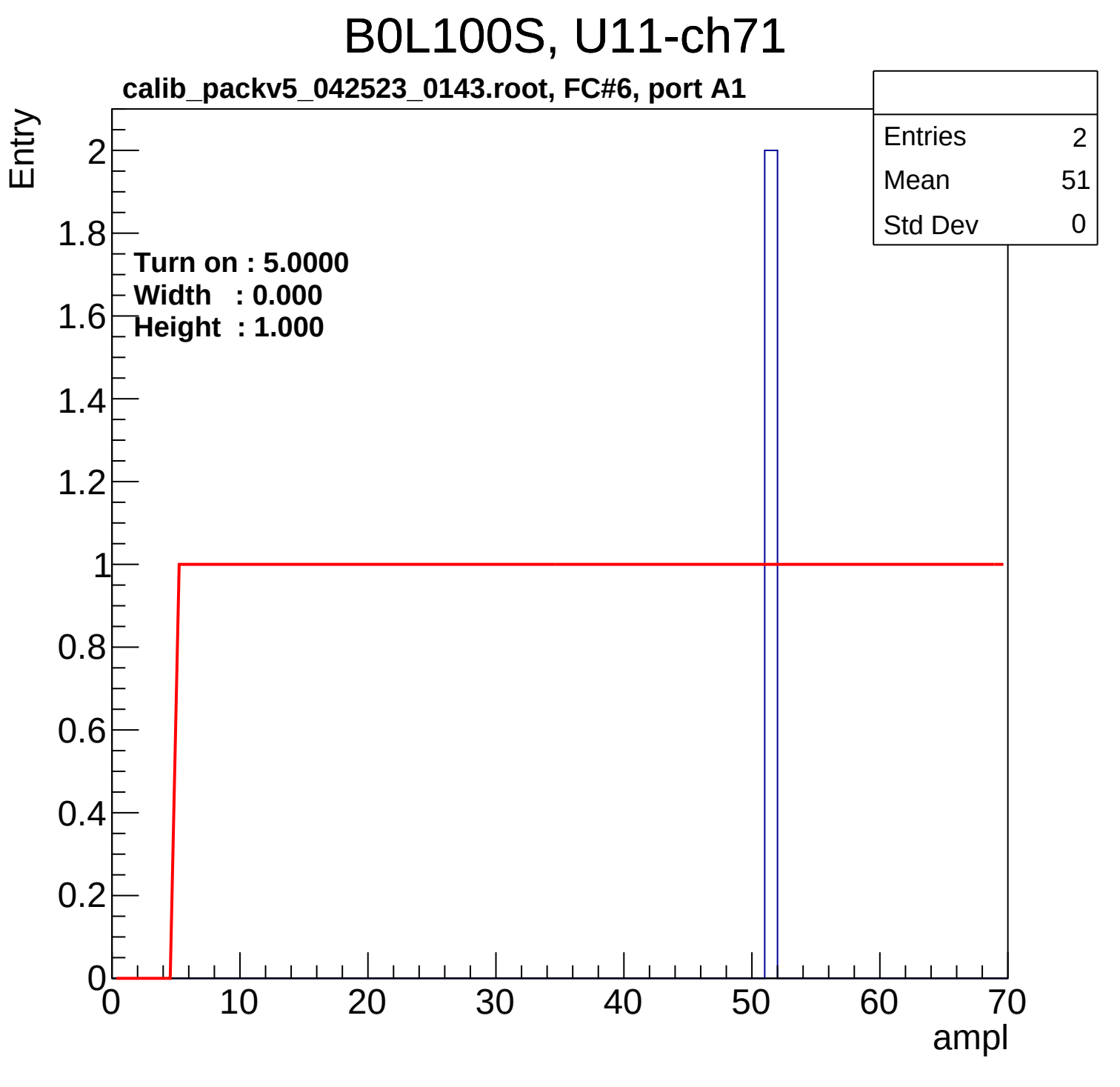
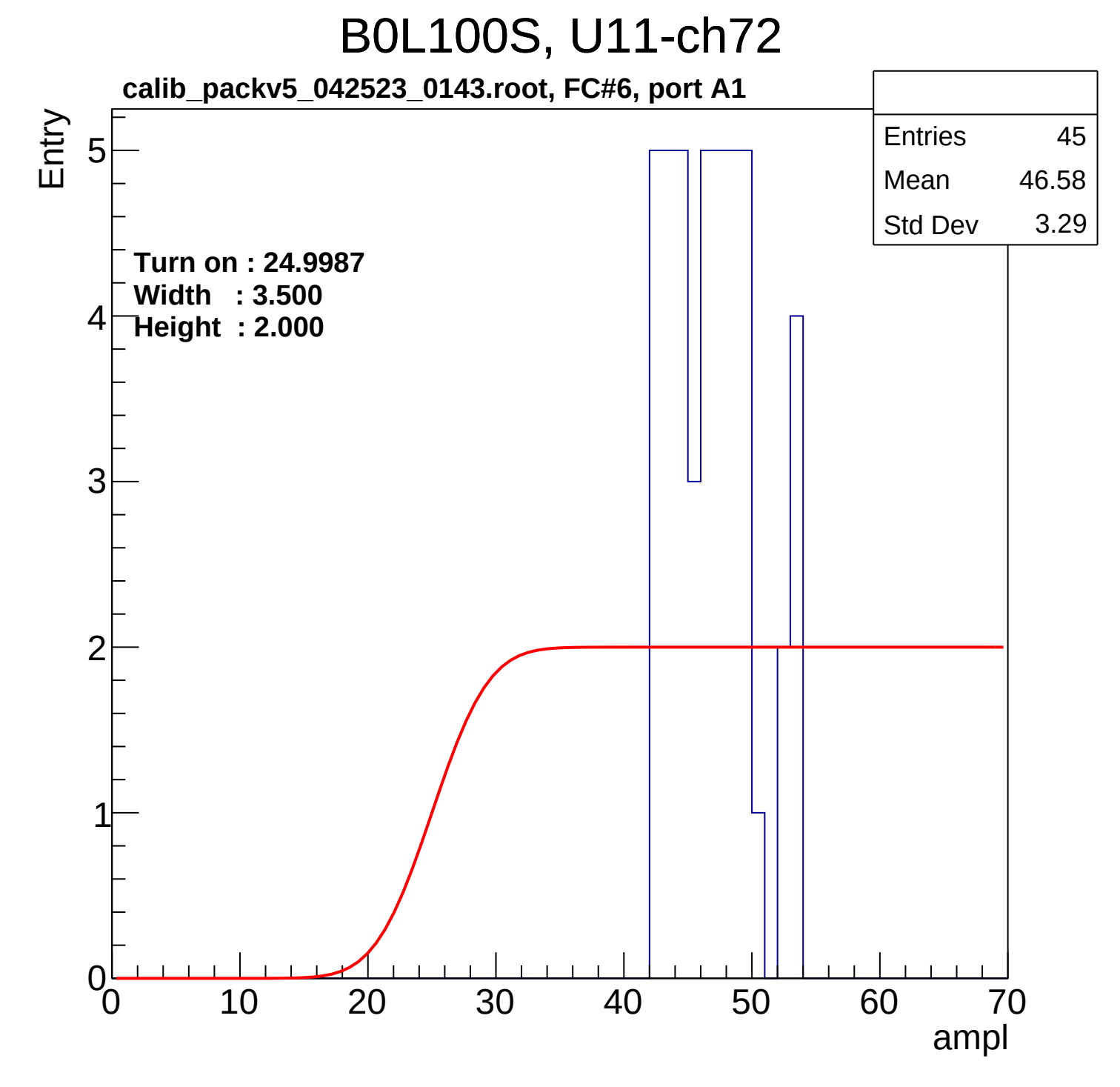

B0L100S, U11-ch71
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 51
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L100S, U11-ch72
calib_packv5_042523_0143.root, FC#6, port A1
Entries 45
Mean 46.58
Std Dev 3.29
Turn on : 24.9987
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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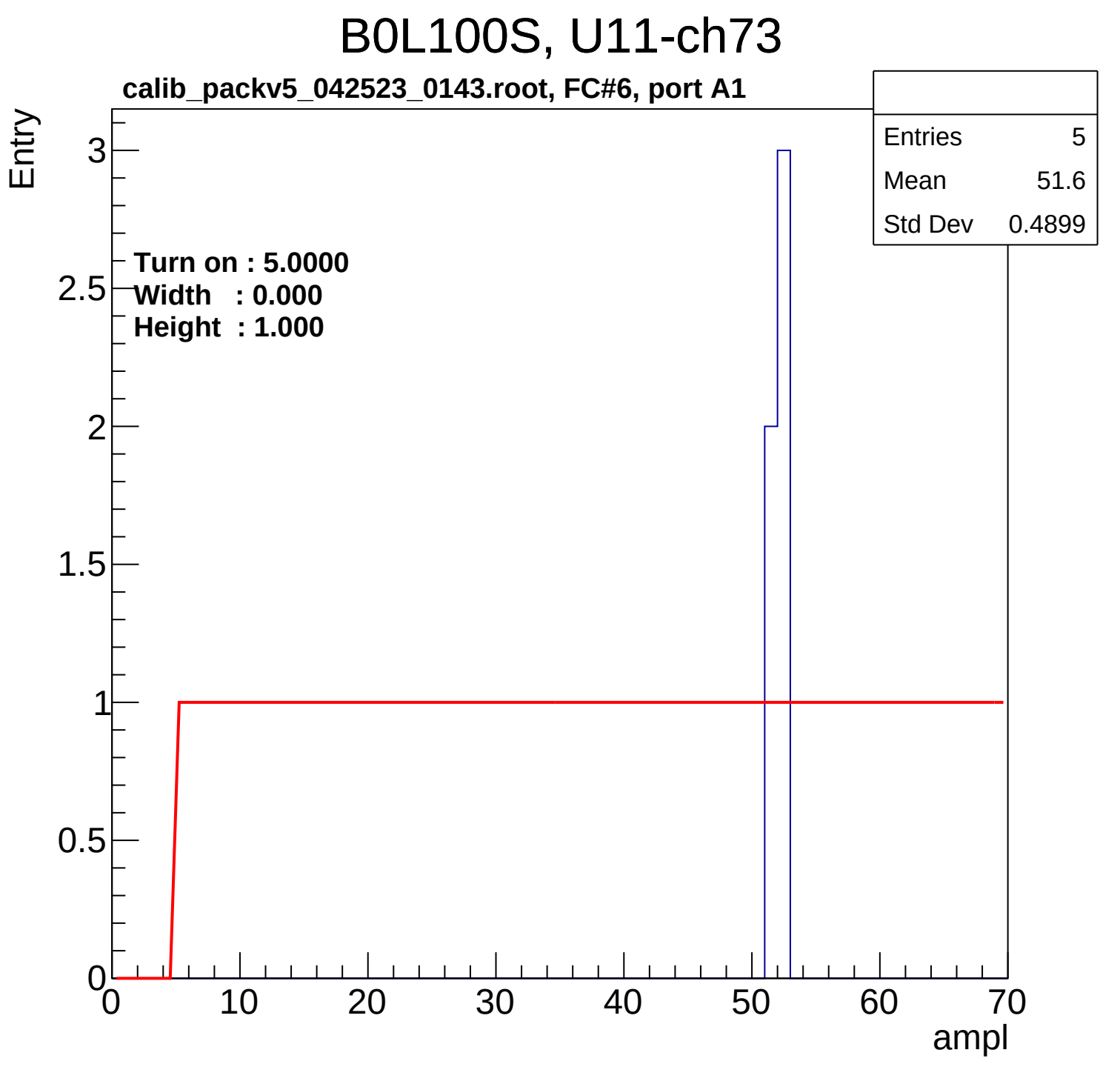
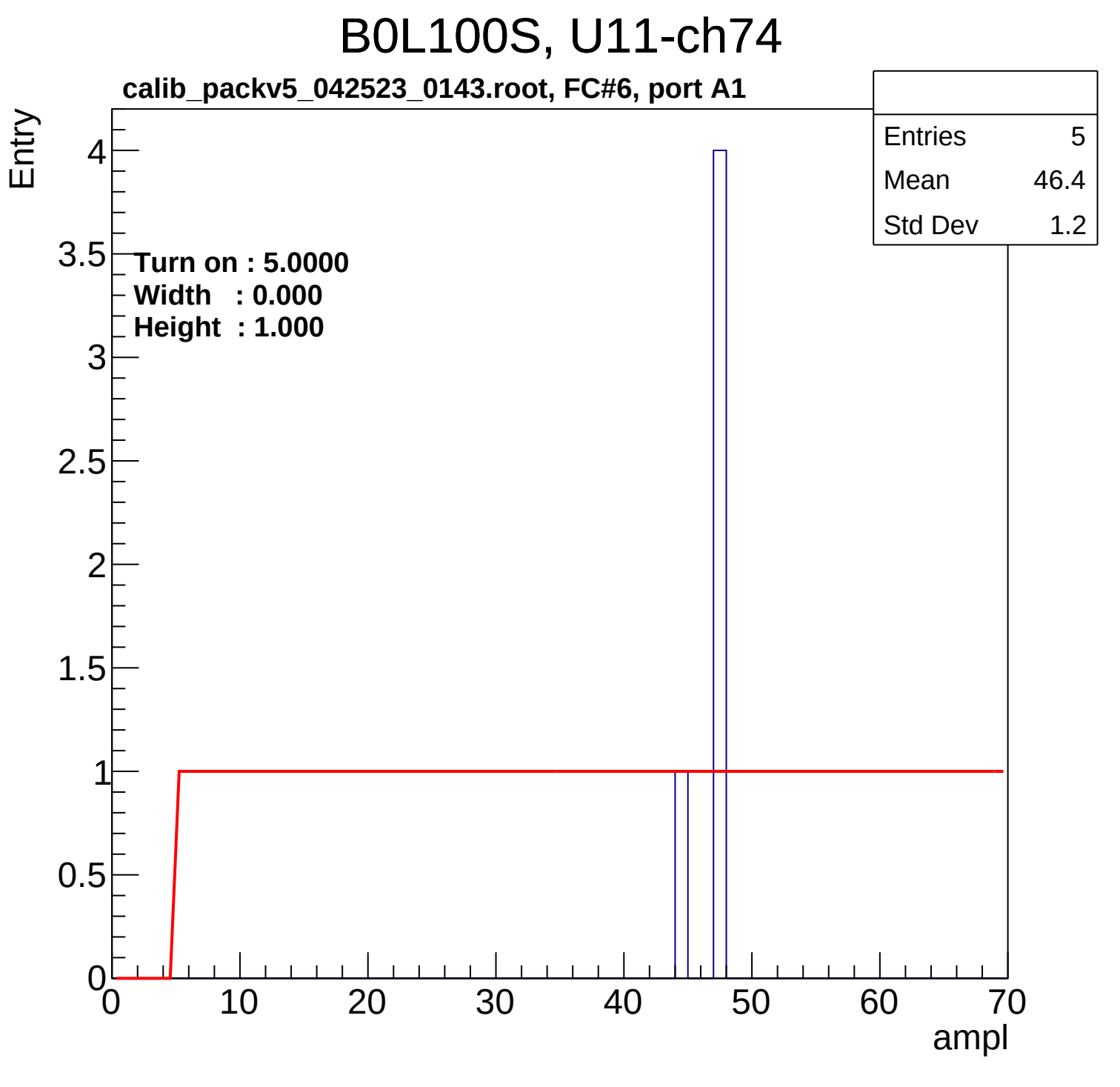
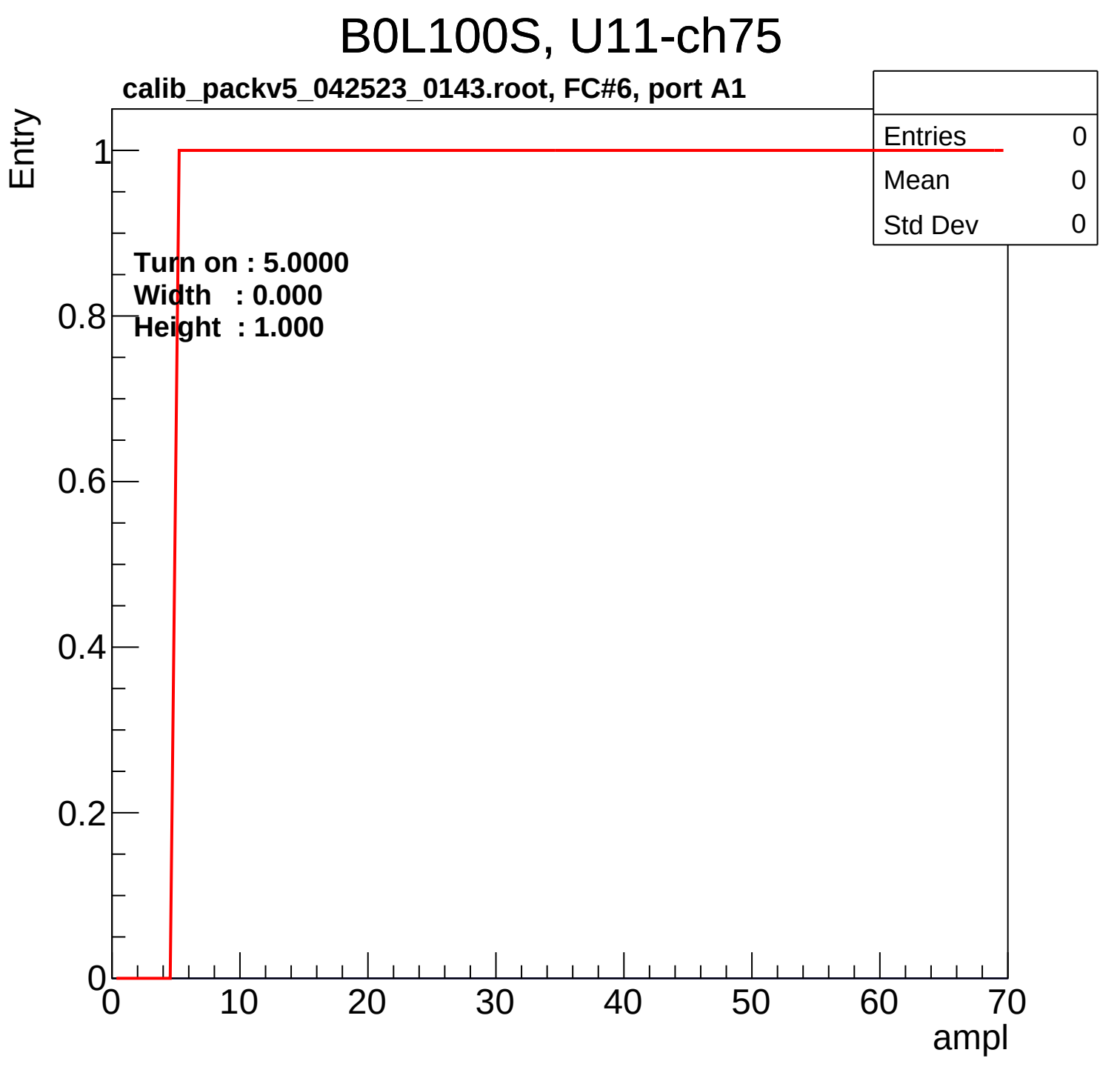

B0L100S, U11-ch73
calib_packv5_042523_0143.root, FC#6, port A1
Entries 5
Mean 51.6
Std Dev 0.4899
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B0L100S, U11-ch74
calib_packv5_042523_0143.root, FC#6, port A1
Entries 5
Mean 46.4
Std Dev 1.2
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B0L100S, U11-ch75
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
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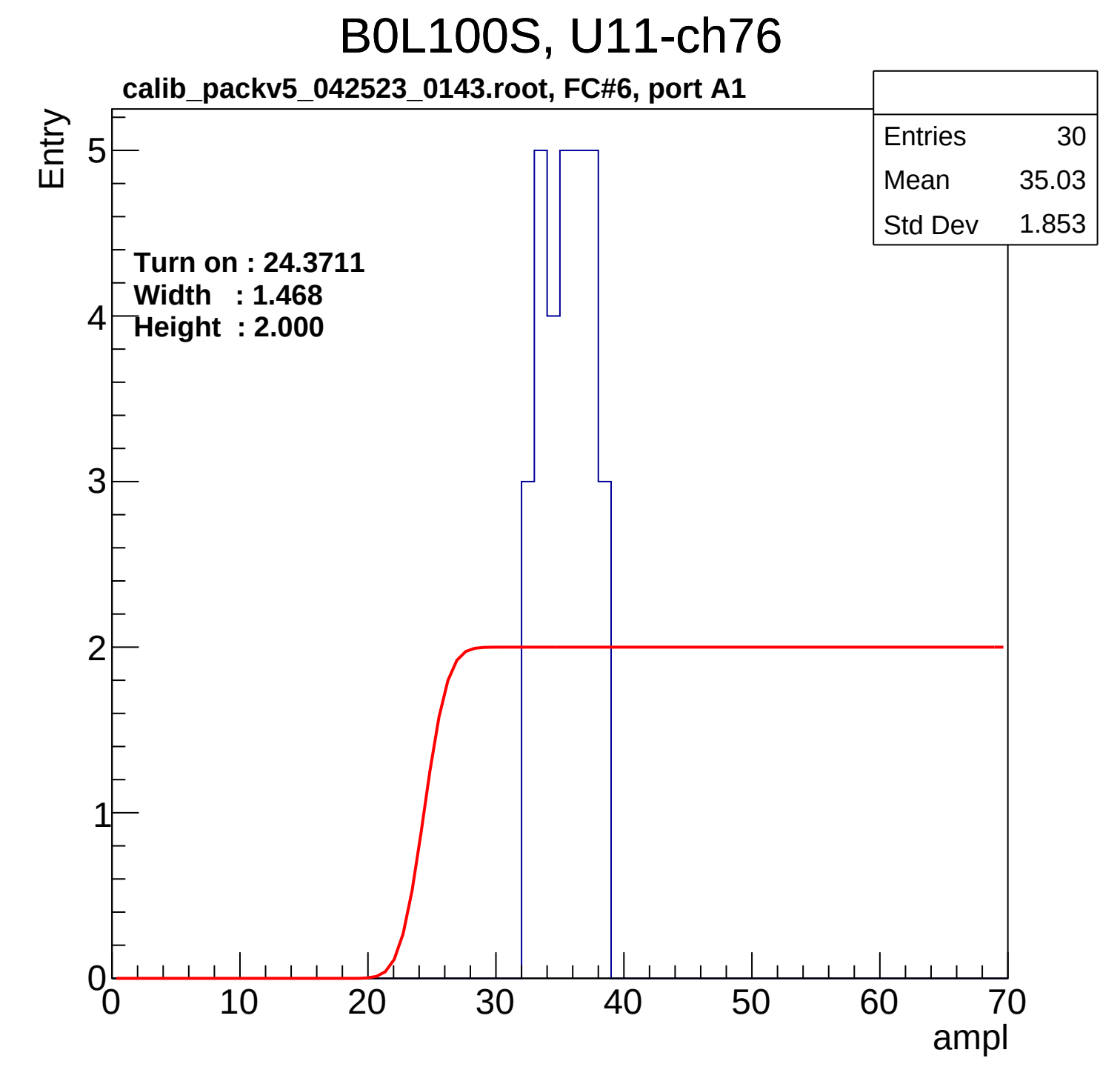
50
60
70
ampl


B0L100S, U11-ch76
calib_packv5_042523_0143.root, FC#6, port A1
Entries 30
Mean 35.03
Std Dev 1.853
Turn on : 24.3711
Width : 1.468
Height : 2.000
Entry
ampl
0
1
2
3
4
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0
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40
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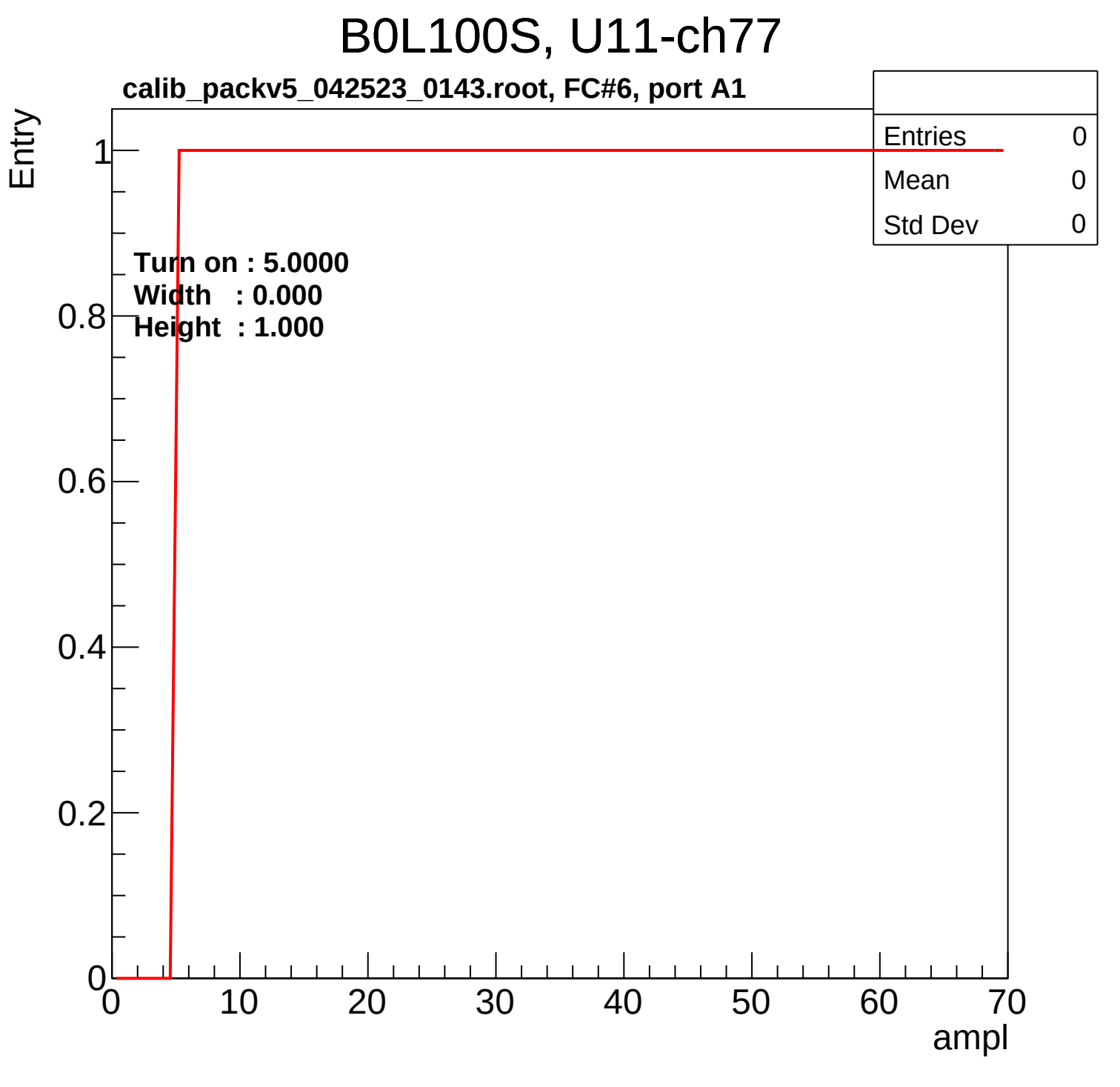
B0L100S, U11-ch77
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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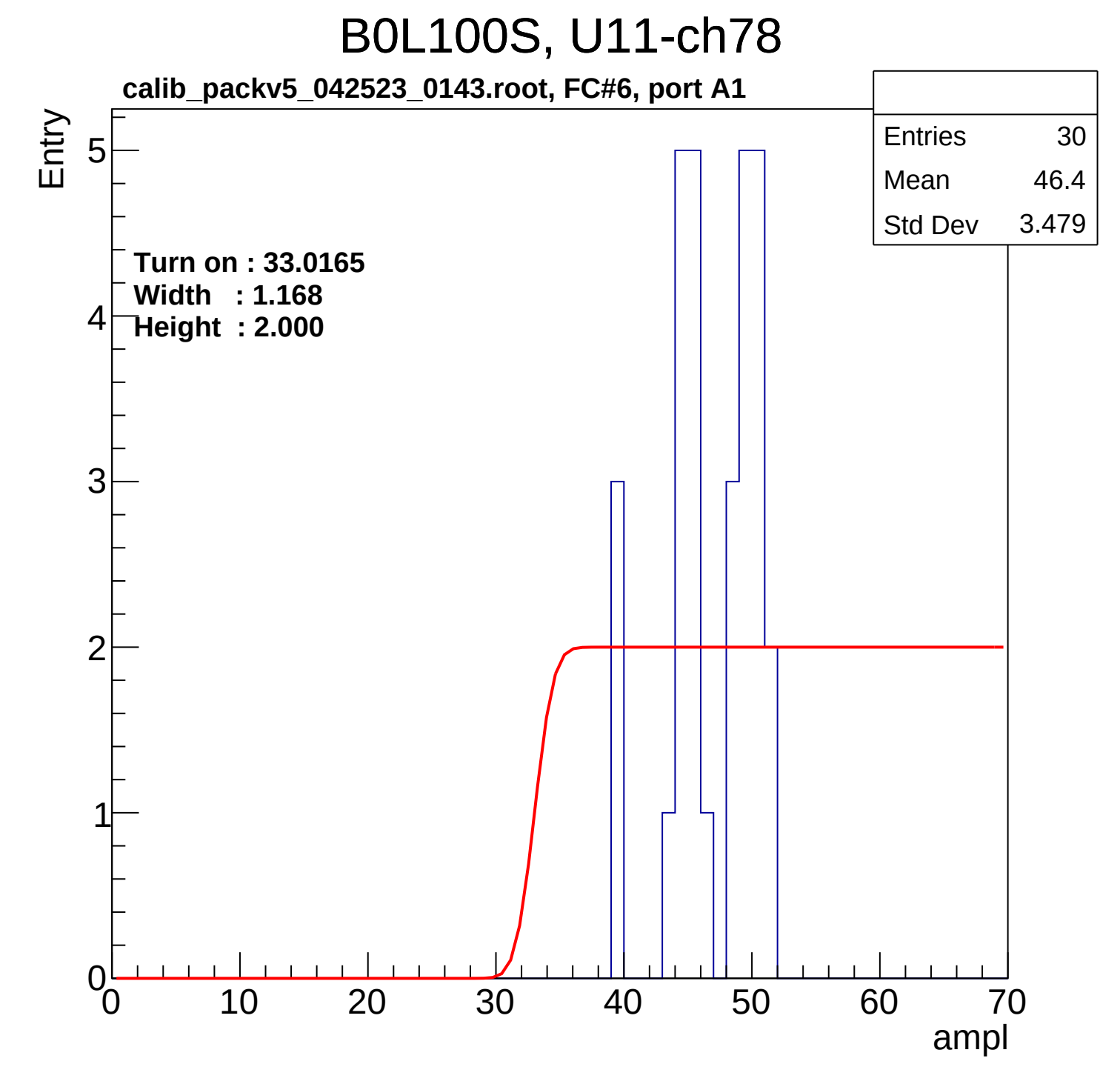
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U11-ch78
calib_packv5_042523_0143.root, FC#6, port A1
Entries 30
Mean 46.4
Std Dev 3.479
Turn on : 33.0165
Width : 1.168
Height : 2.000
Entry
ampl
0
1
2
3
4
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0
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20
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40
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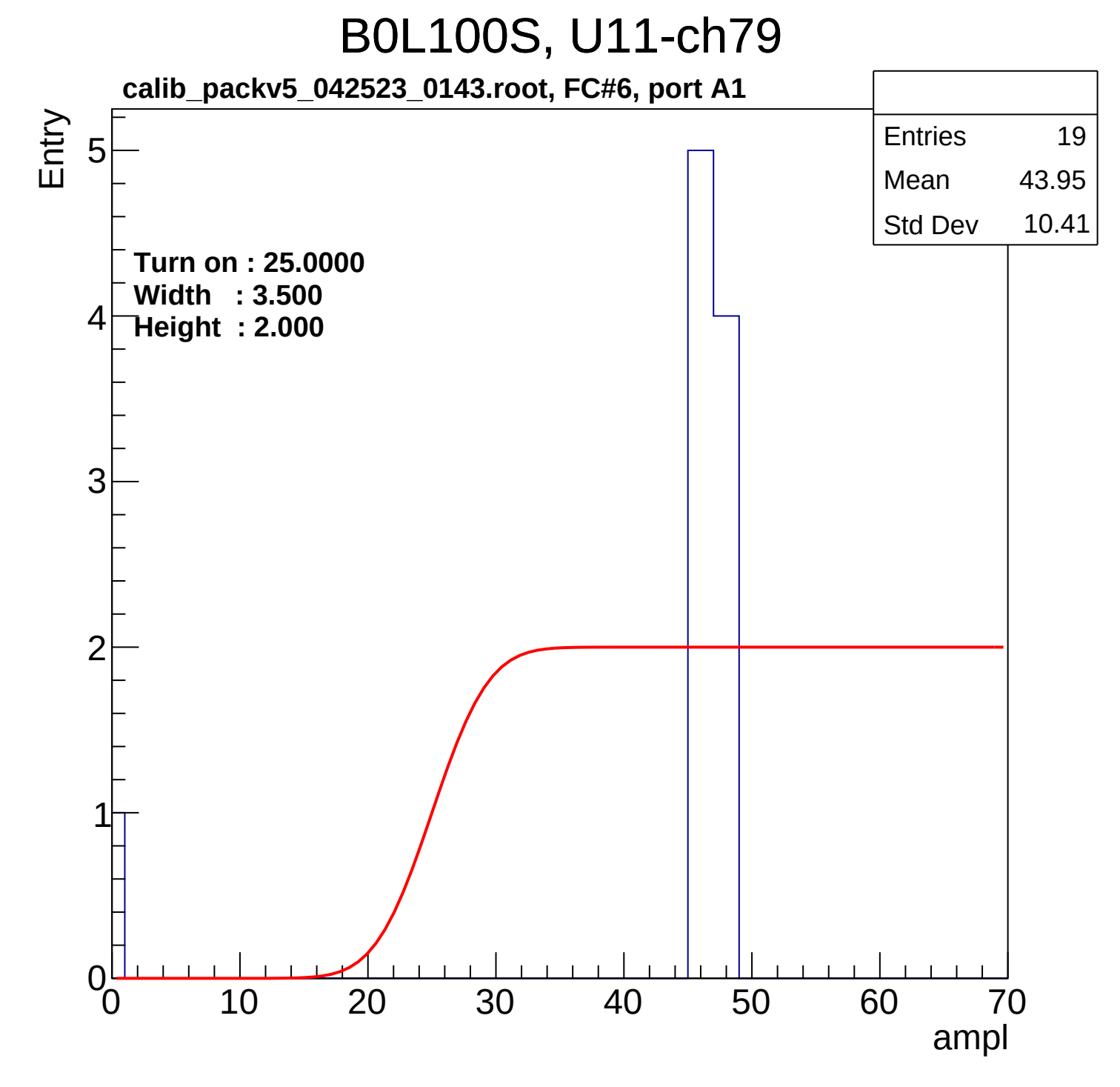
B0L100S, U11-ch79
calib_packv5_042523_0143.root, FC#6, port A1
Entries 19
Mean 43.95
Std Dev 10.41
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
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20
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40
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60
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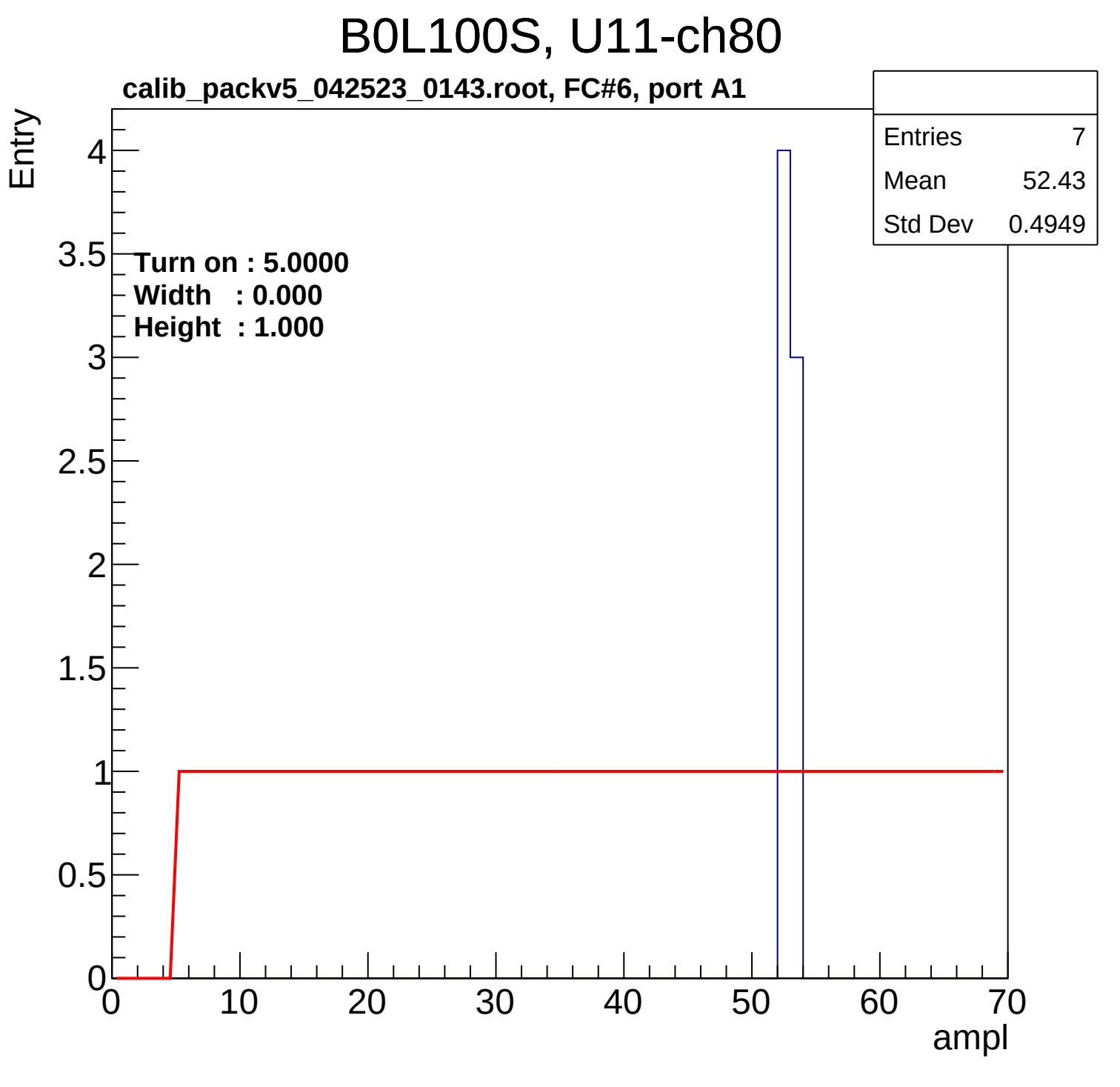
B0L100S, U11-ch80
calib_packv5_042523_0143.root, FC#6, port A1
Entries 7
Mean 52.43
Std Dev 0.4949
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
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20
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40
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60
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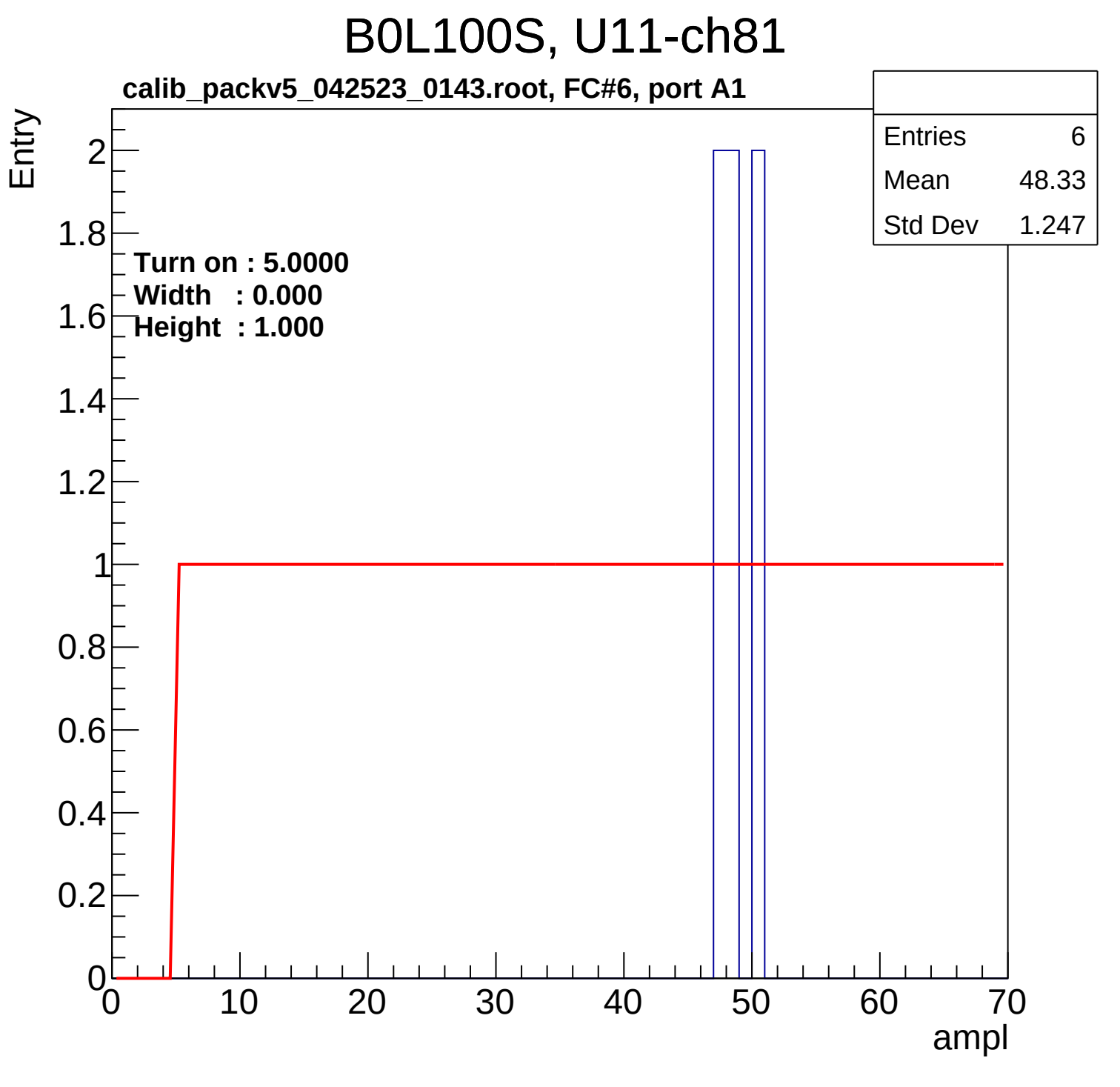
B0L100S, U11-ch81
calib_packv5_042523_0143.root, FC#6, port A1
Entries 6
Mean 48.33
Std Dev 1.247
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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20
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40
50
60
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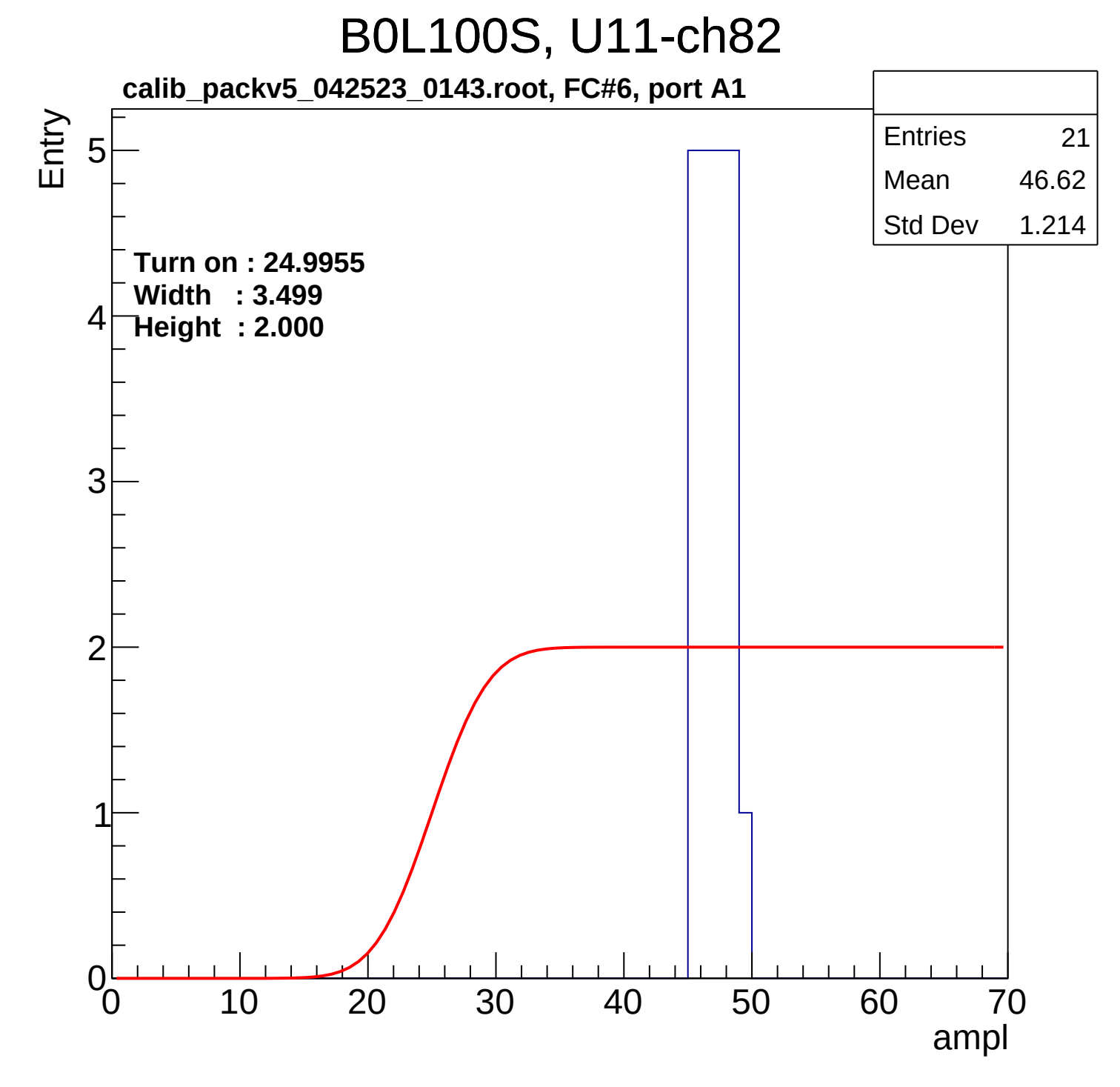
B0L100S, U11-ch82
calib_packv5_042523_0143.root, FC#6, port A1
Entries 21
Mean 46.62
Std Dev 1.214
Turn on : 24.9955
Width : 3.499
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
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20
30
40
50
60
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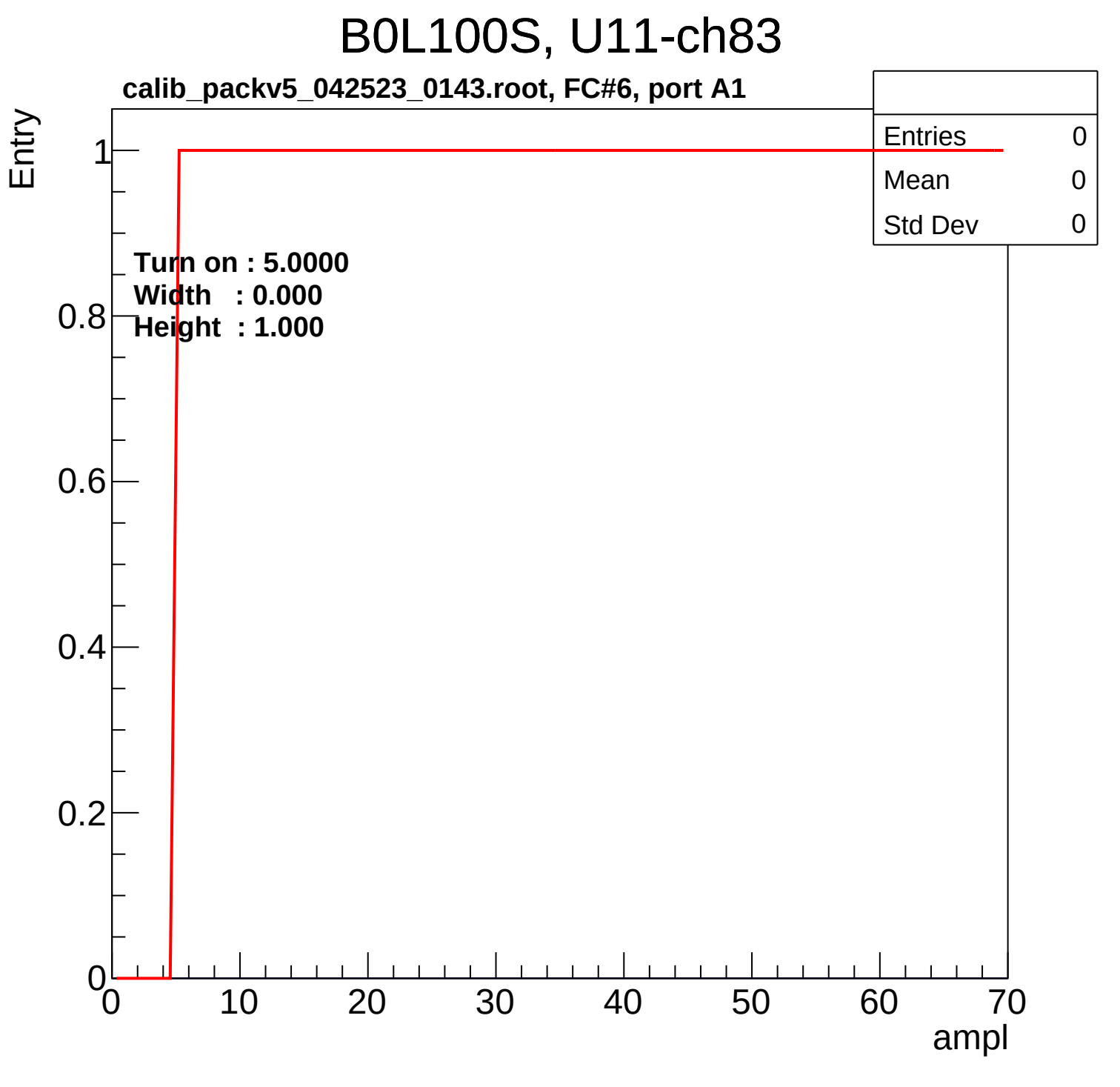
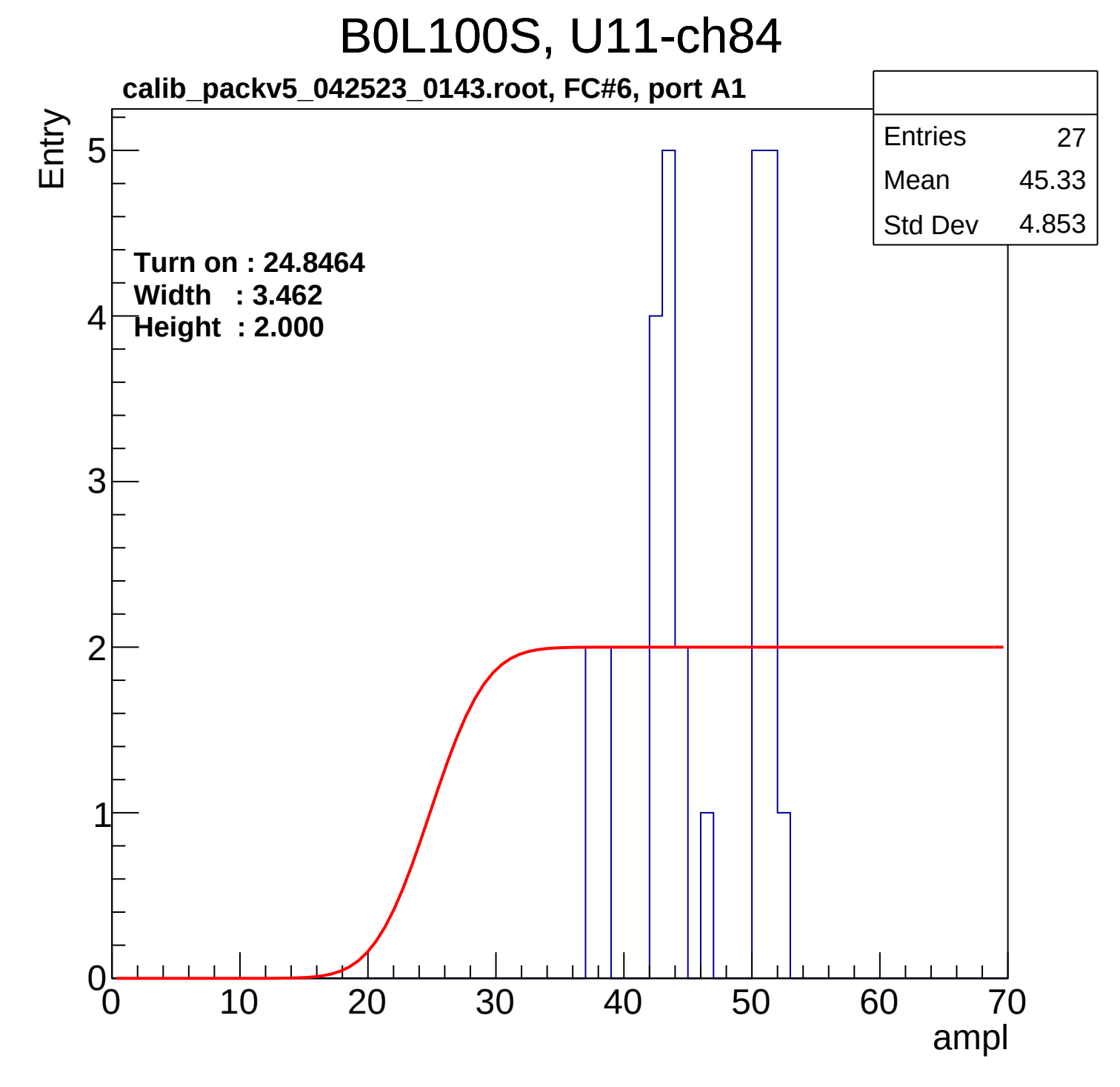

B0L100S, U11-ch83
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U11-ch84
calib_packv5_042523_0143.root, FC#6, port A1
Entries 27
Mean 45.33
Std Dev 4.853
Turn on : 24.8464
Width : 3.462
Height : 2.000
Entry
ampl
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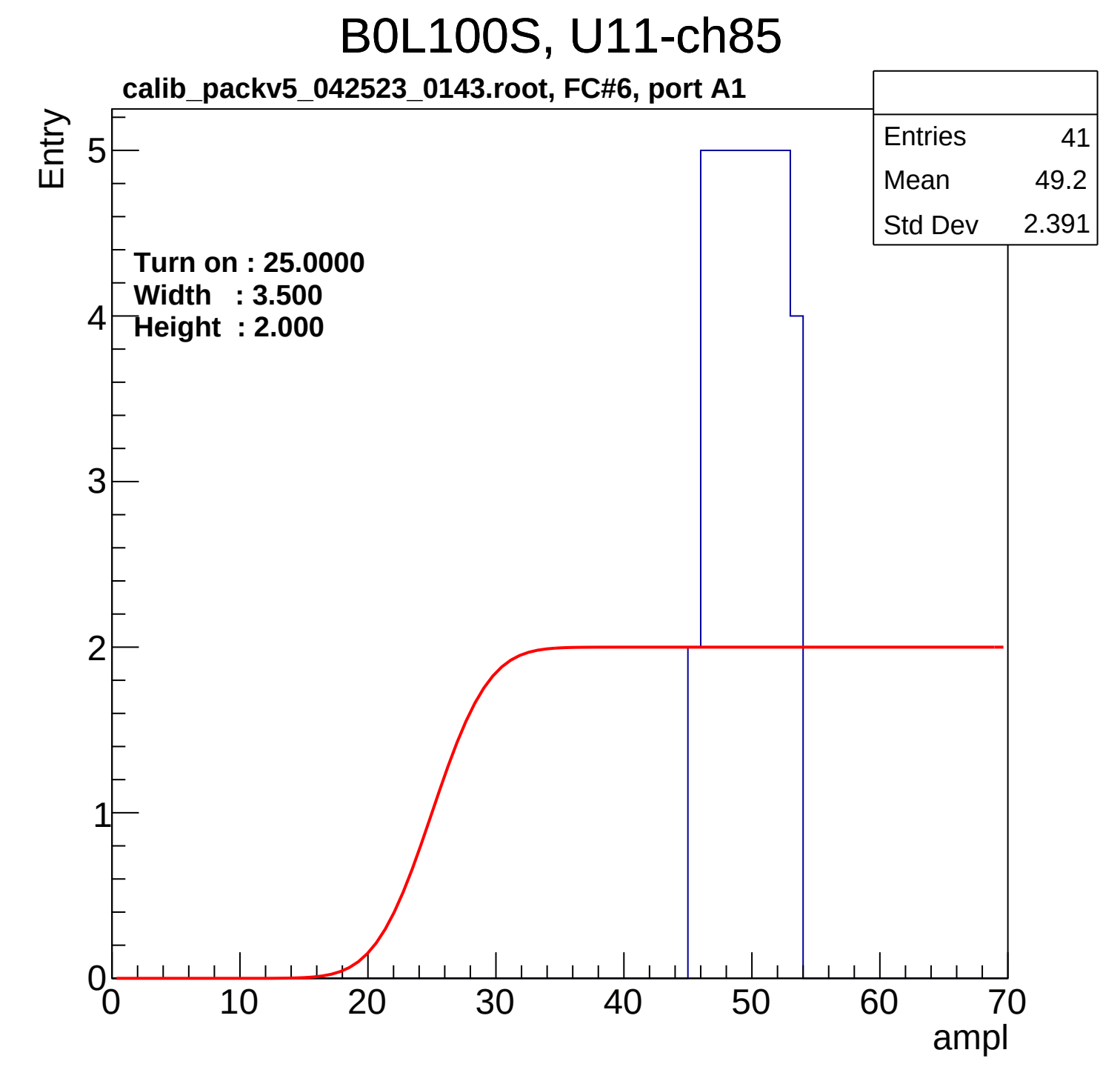
B0L100S, U11-ch85
calib_packv5_042523_0143.root, FC#6, port A1
Entries 41
Mean 49.2
Std Dev 2.391
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
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1
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3
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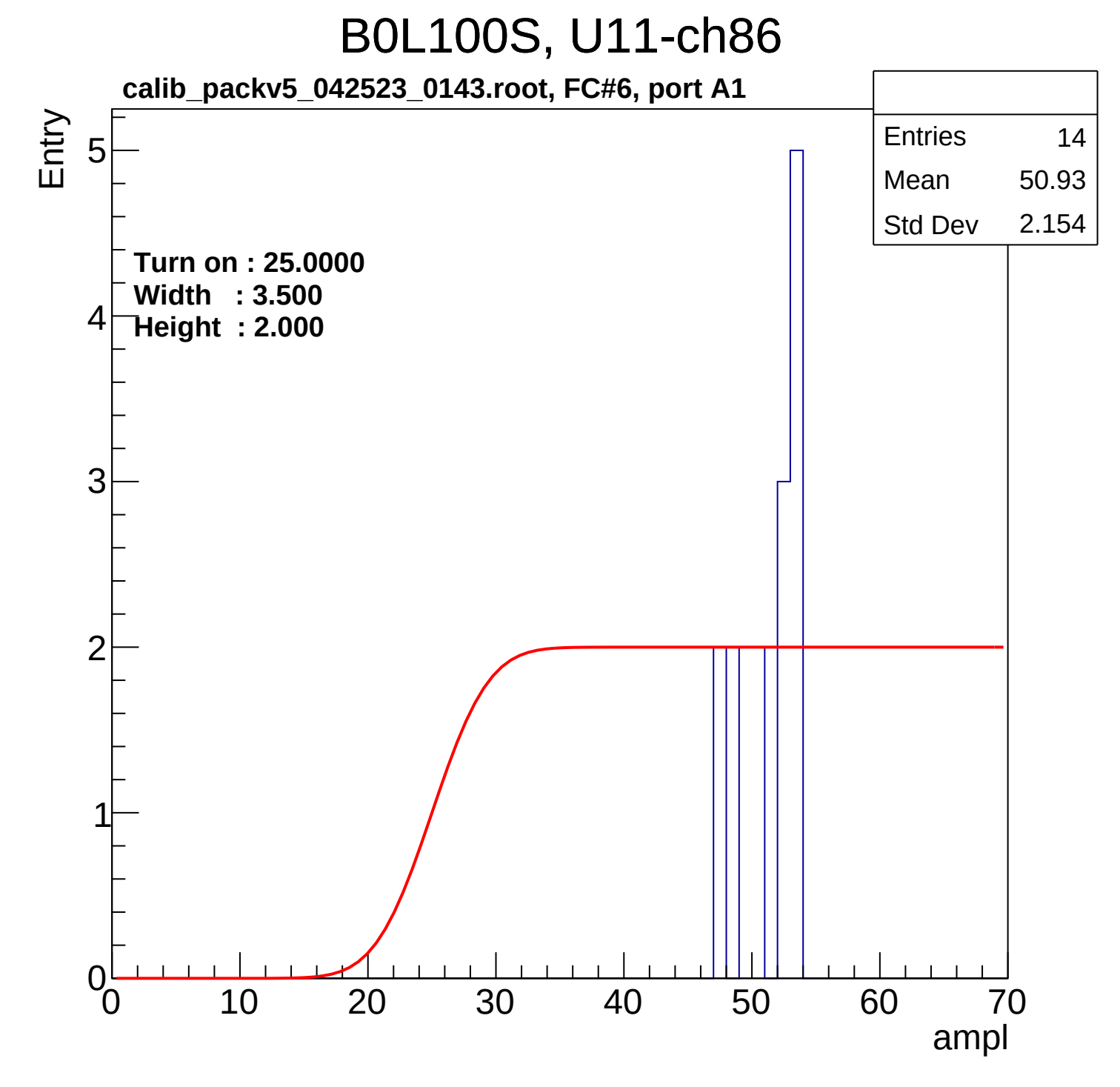
B0L100S, U11-ch86
calib_packv5_042523_0143.root, FC#6, port A1
Entries 14
Mean 50.93
Std Dev 2.154
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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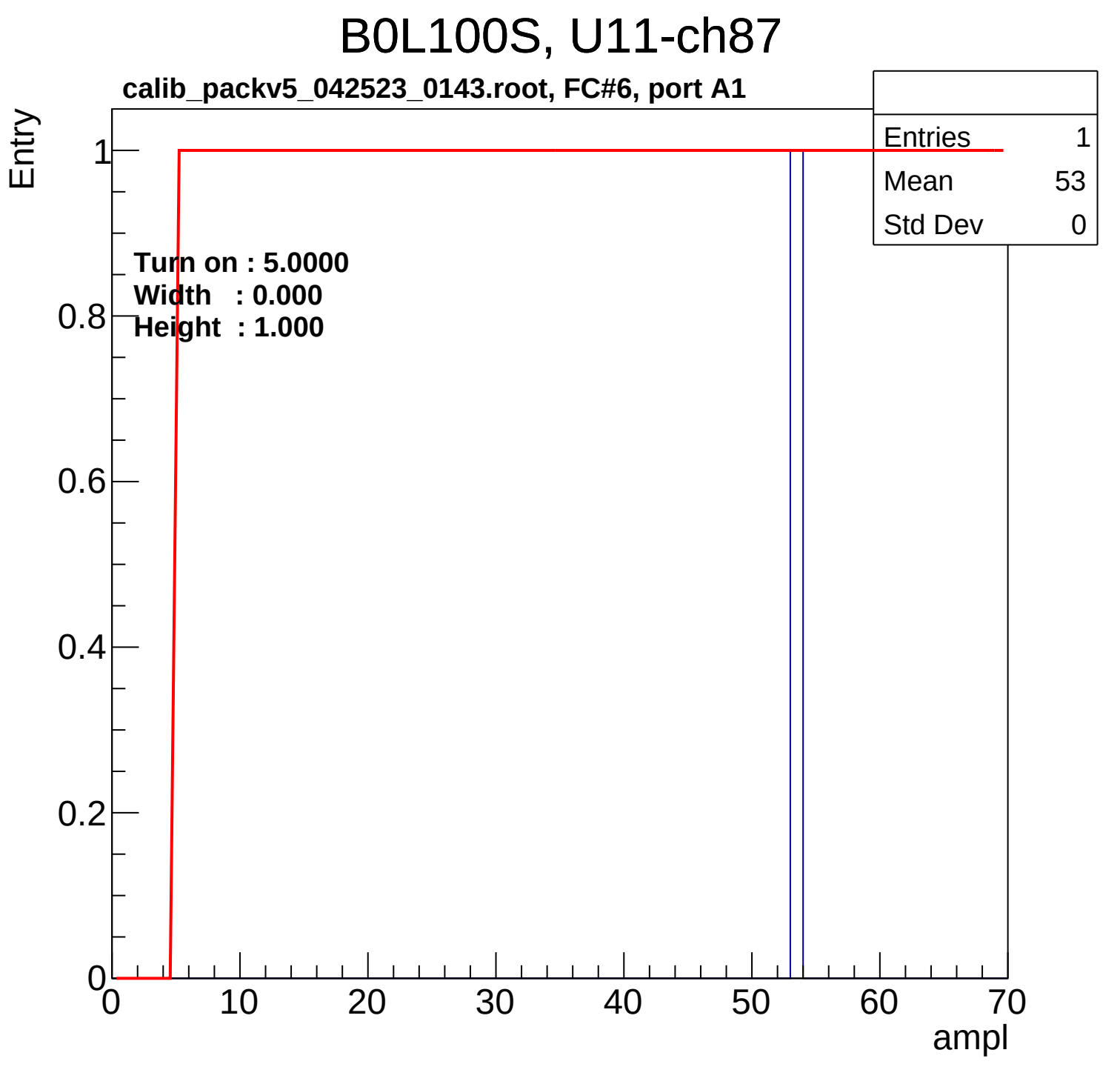
B0L100S, U11-ch87
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 53
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.2
0.4
0.6
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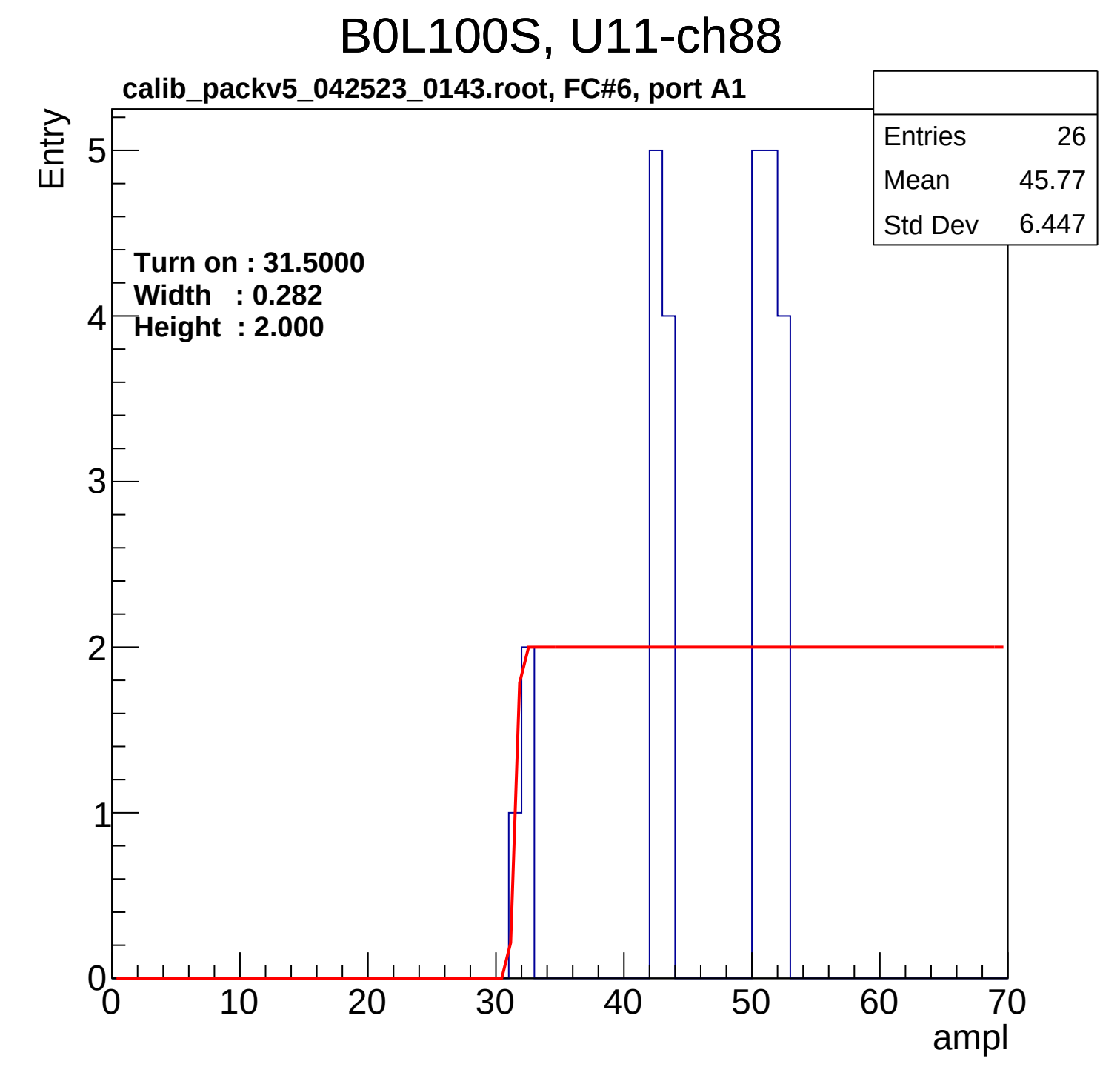
B0L100S, U11-ch88
calib_packv5_042523_0143.root, FC#6, port A1
Entries 26
Mean 45.77
Std Dev 6.447
Turn on : 31.5000
Width : 0.282
Height : 2.000
Entry
ampl
0
1
2
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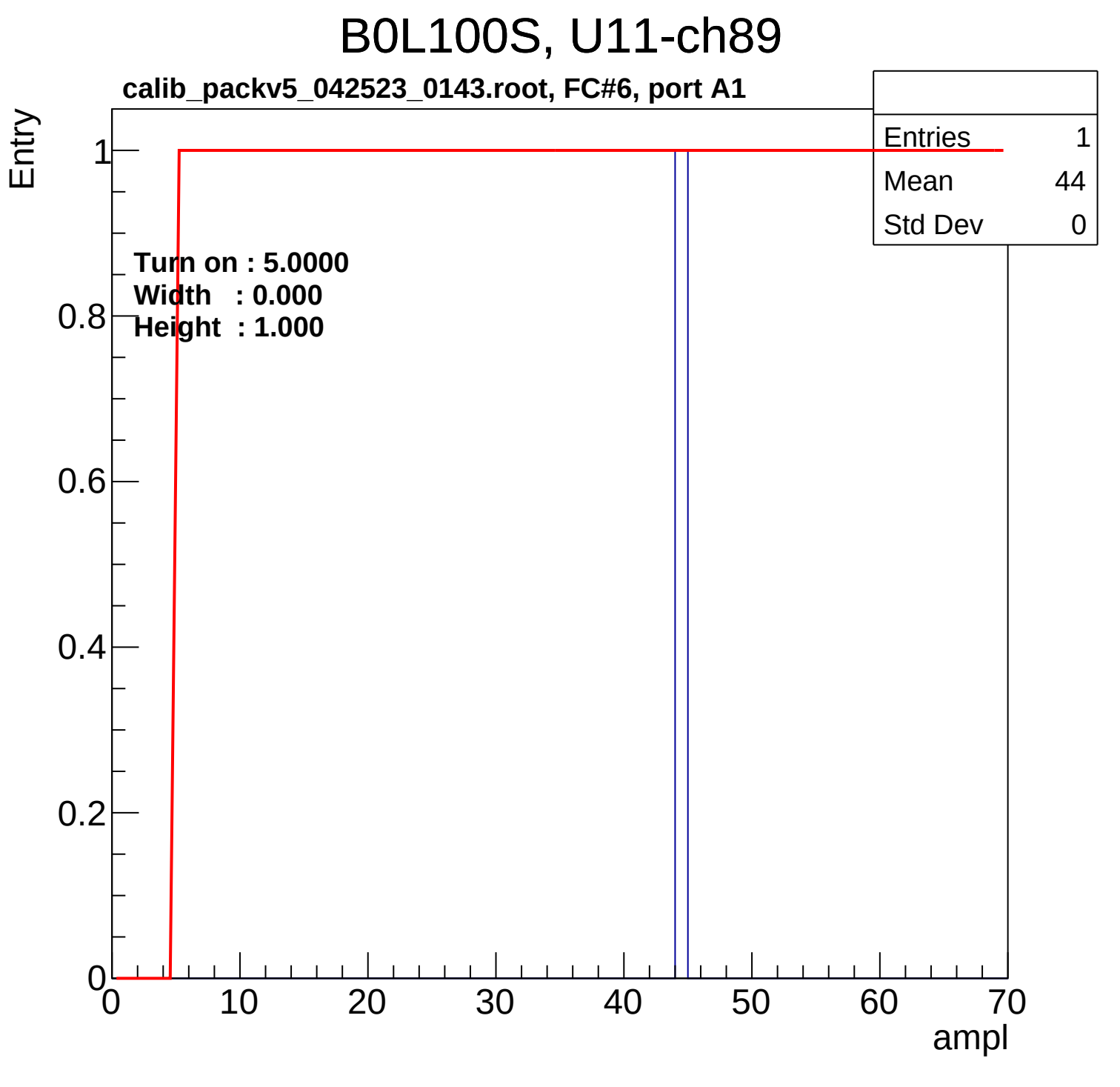
B0L100S, U11-ch89
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 44
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
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40
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60
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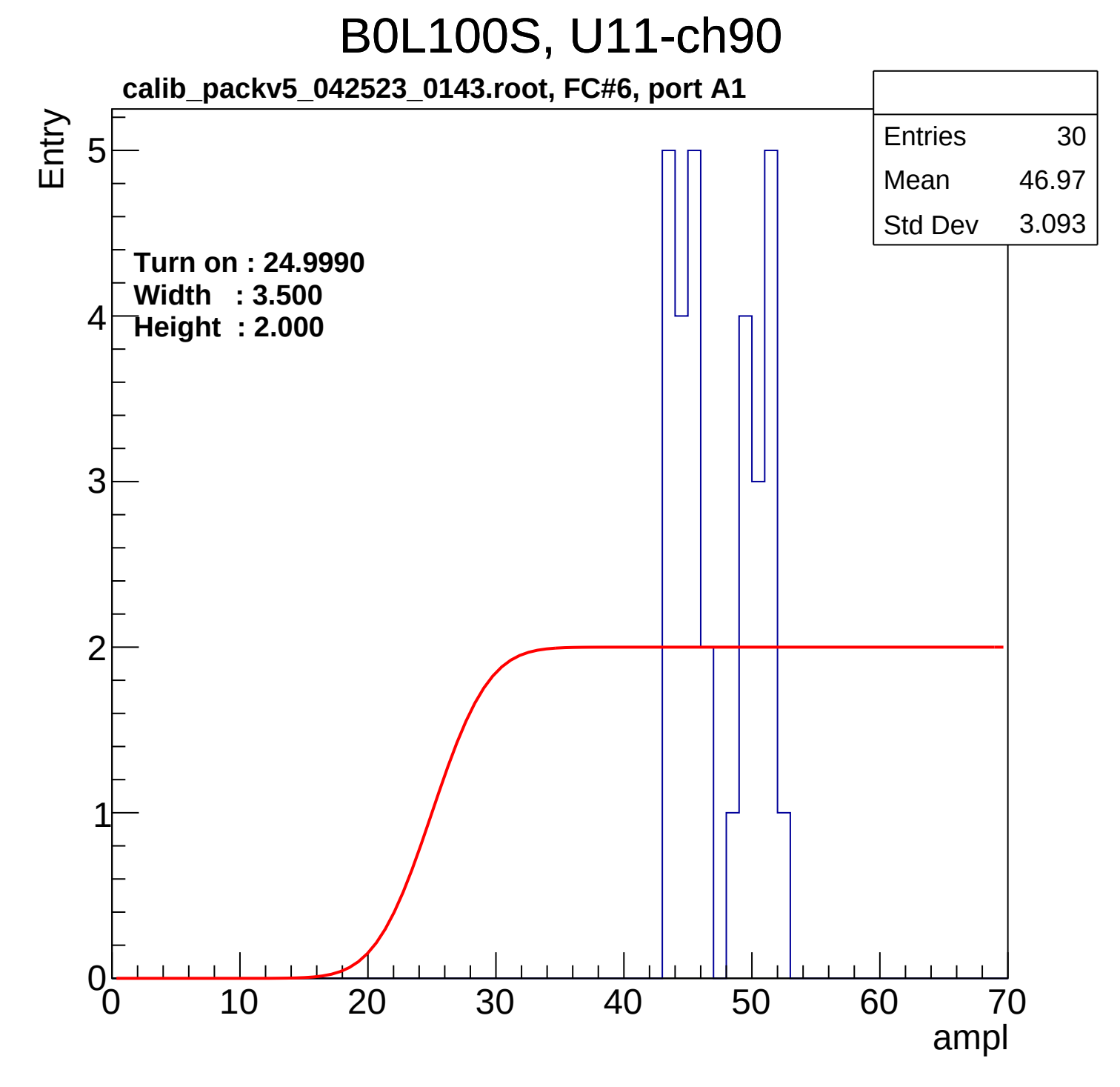
B0L100S, U11-ch90
calib_packv5_042523_0143.root, FC#6, port A1
Entries 30
Mean 46.97
Std Dev 3.093
Turn on : 24.9990
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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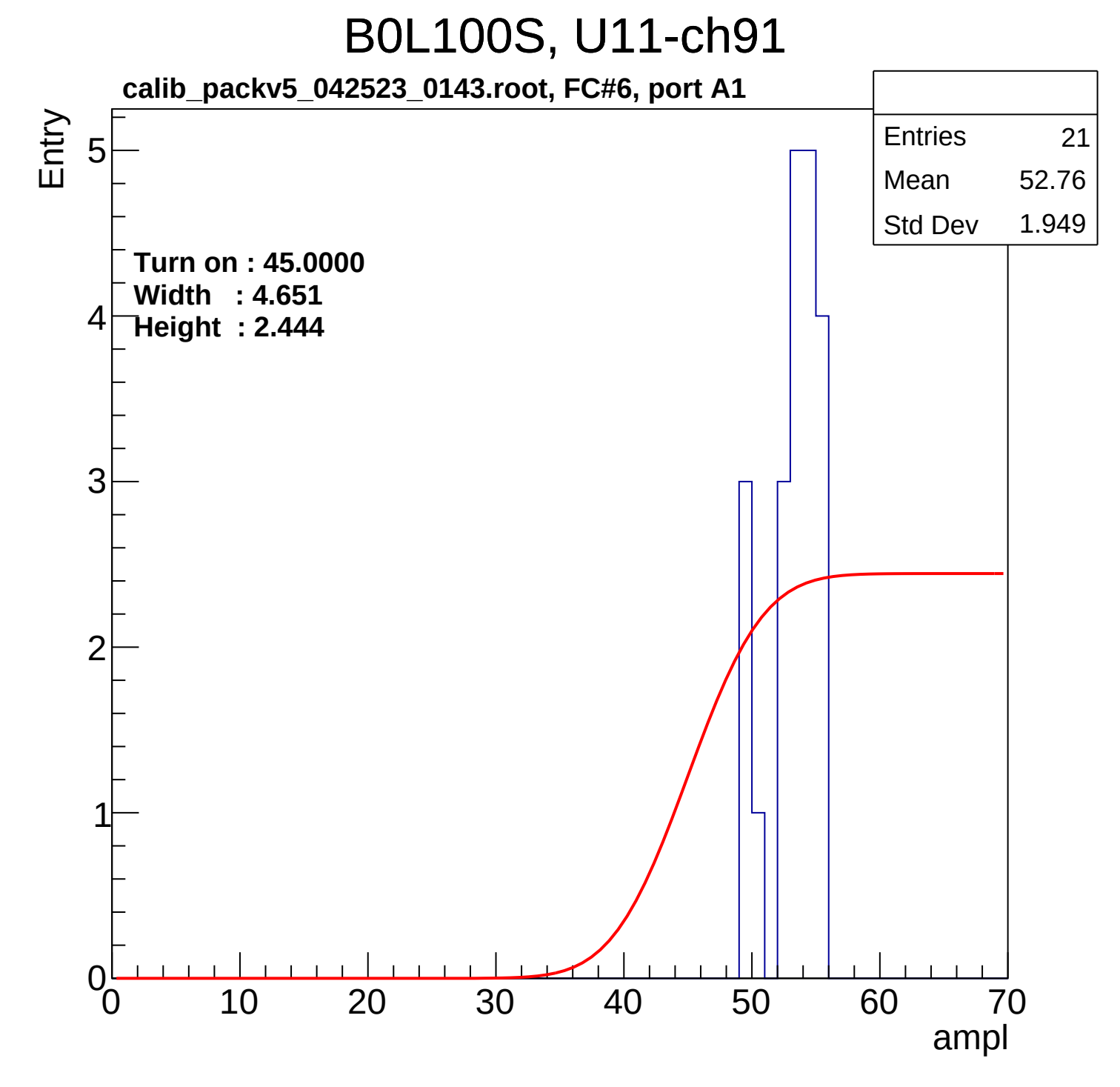
B0L100S, U11-ch91
calib_packv5_042523_0143.root, FC#6, port A1
Entries 21
Mean 52.76
Std Dev 1.949
Turn on : 45.0000
Width : 4.651
Height : 2.444
Entry
ampl
0
1
2
3
4
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0
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40
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60
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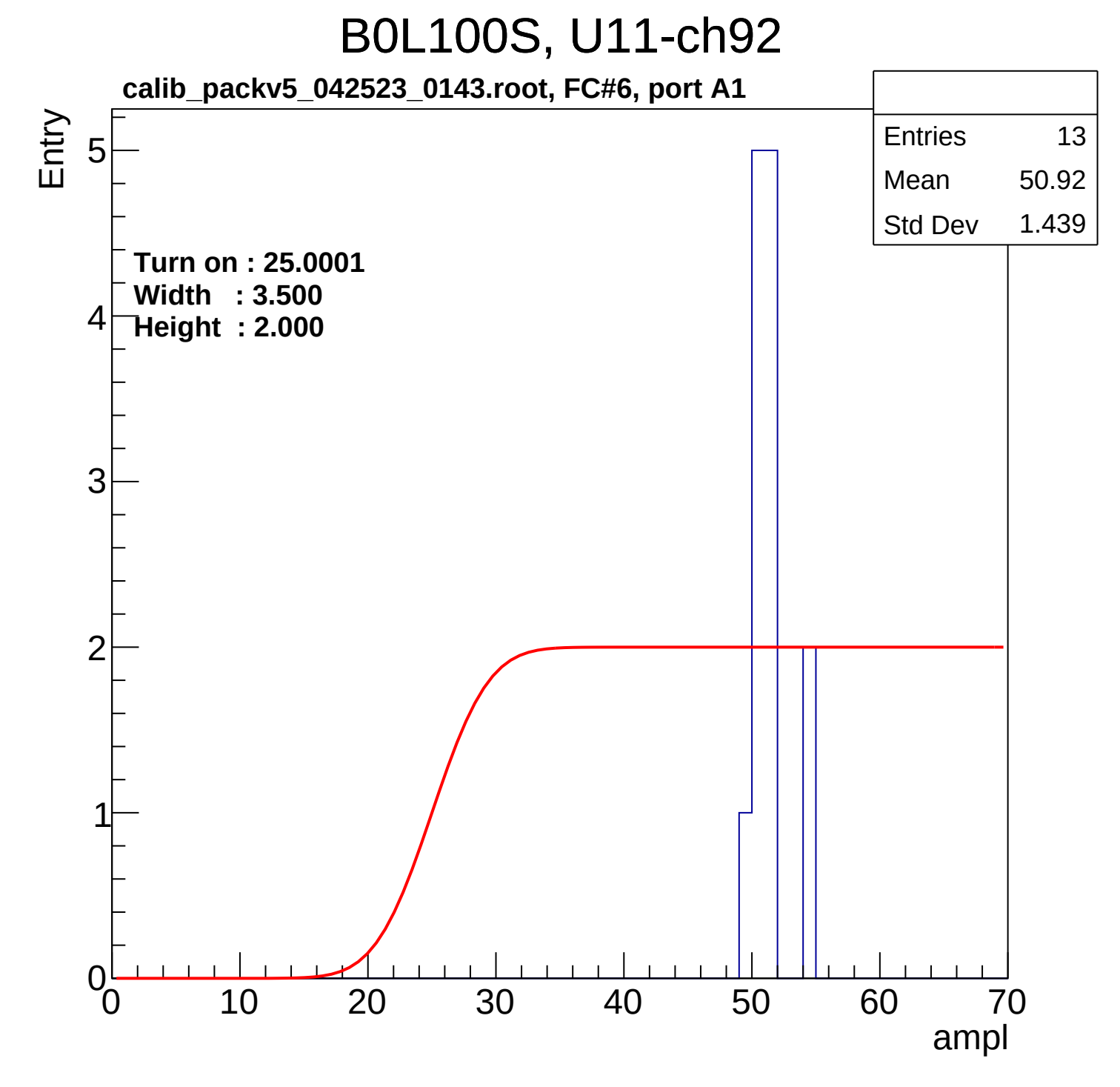
B0L100S, U11-ch92
calib_packv5_042523_0143.root, FC#6, port A1
Entries 13
Mean 50.92
Std Dev 1.439
Turn on : 25.0001
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
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40
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60
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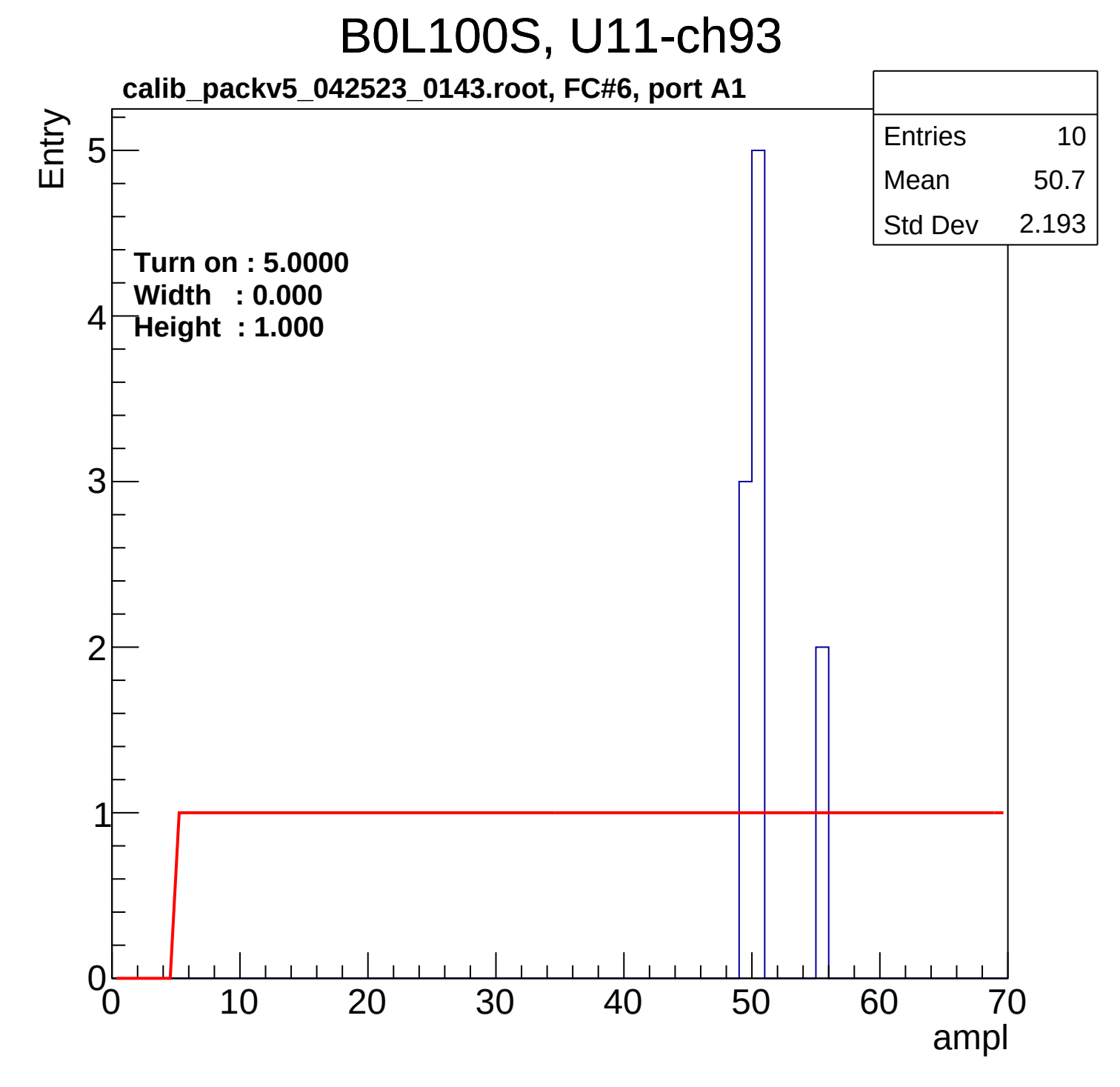
B0L100S, U11-ch93
calib_packv5_042523_0143.root, FC#6, port A1
Entries 10
Mean 50.7
Std Dev 2.193
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
10
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40
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60
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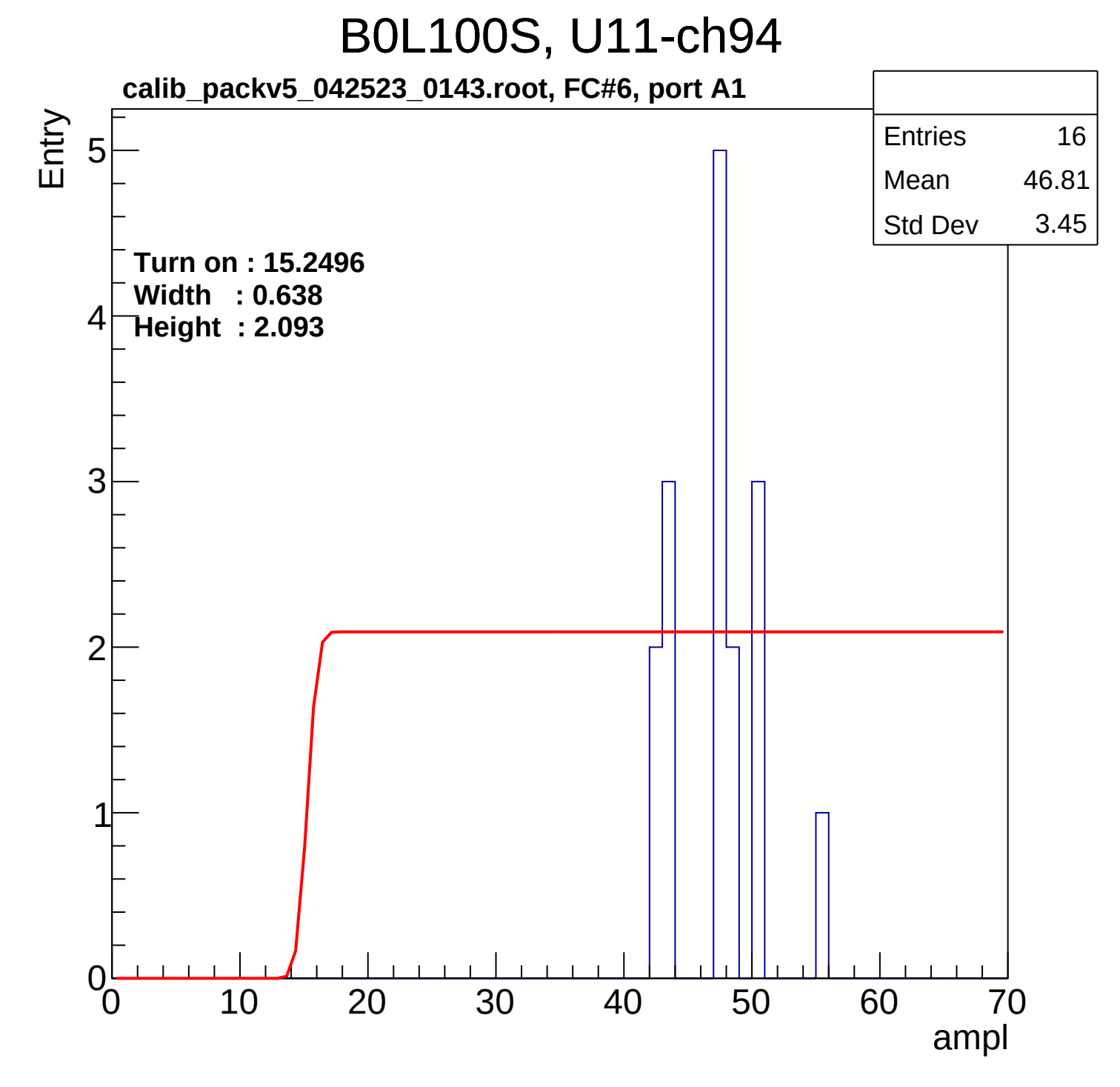
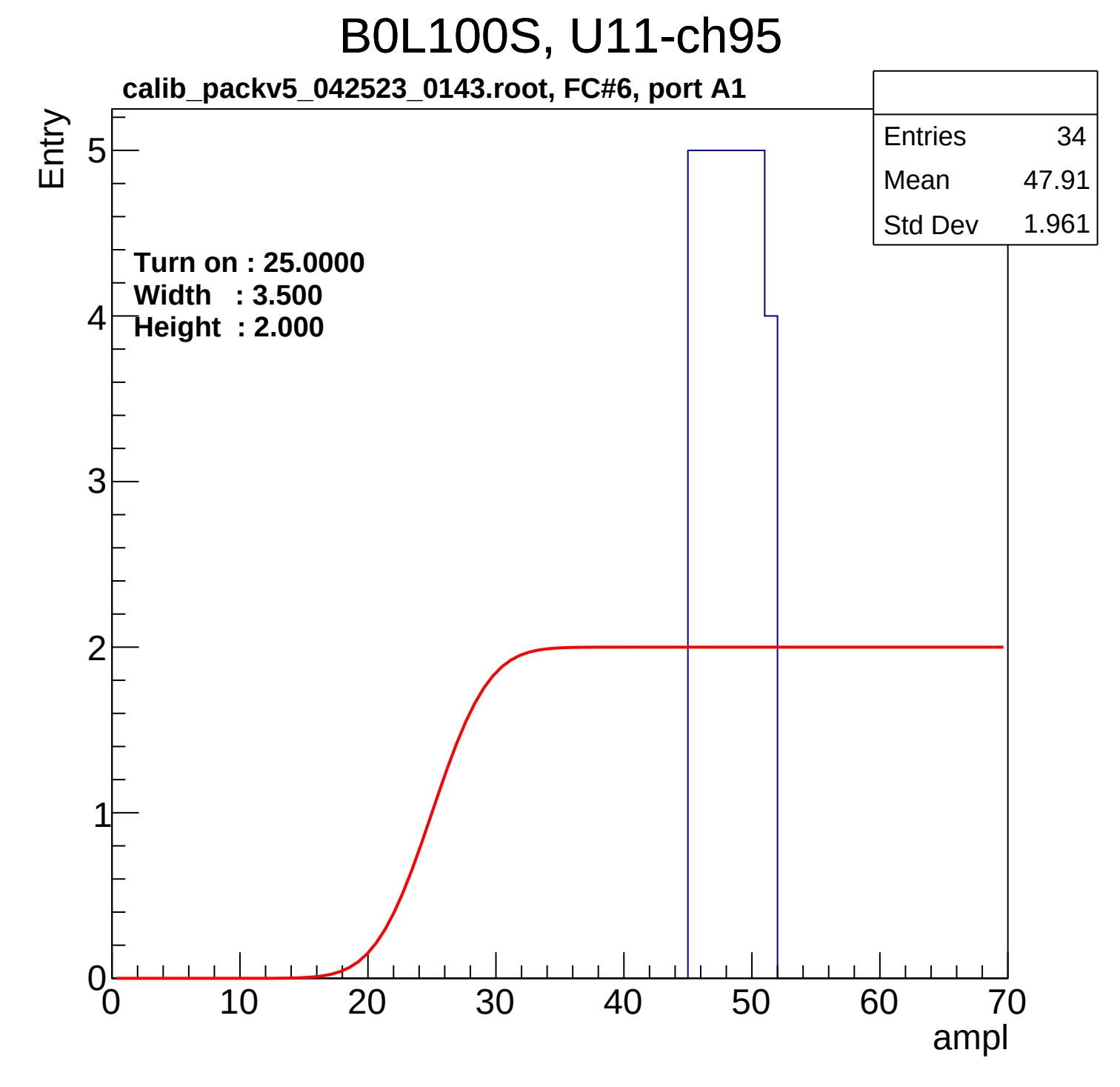
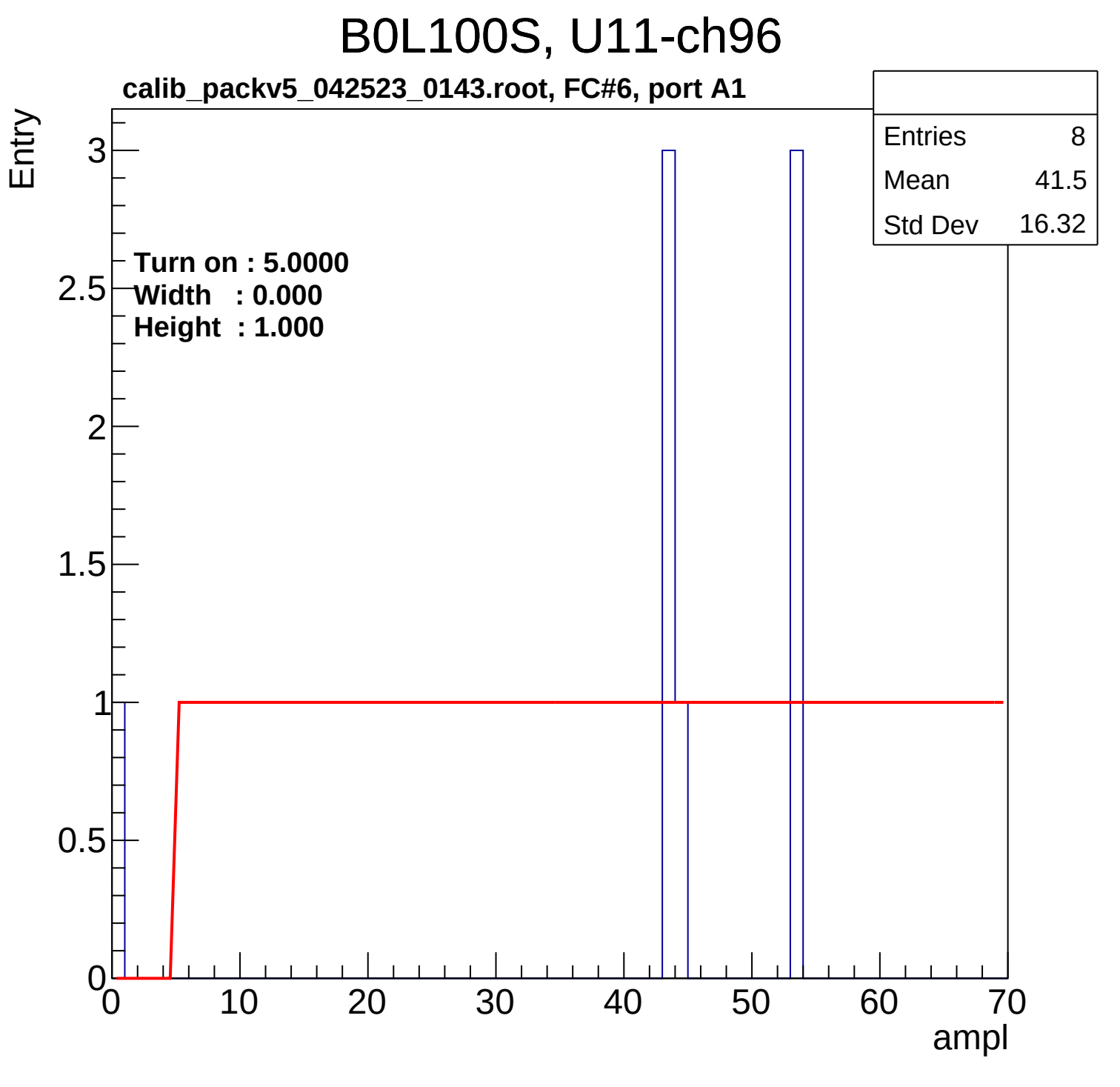

B0L100S, U11-ch94
calib_packv5_042523_0143.root, FC#6, port A1
Entries 16
Mean 46.81
Std Dev 3.45
Turn on : 15.2496
Width : 0.638
Height : 2.093
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U11-ch95
calib_packv5_042523_0143.root, FC#6, port A1
Entries 34
Mean 47.91
Std Dev 1.961
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U11-ch96
calib_packv5_042523_0143.root, FC#6, port A1
Entries 8
Mean 41.5
Std Dev 16.32
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
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20
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40
50
60
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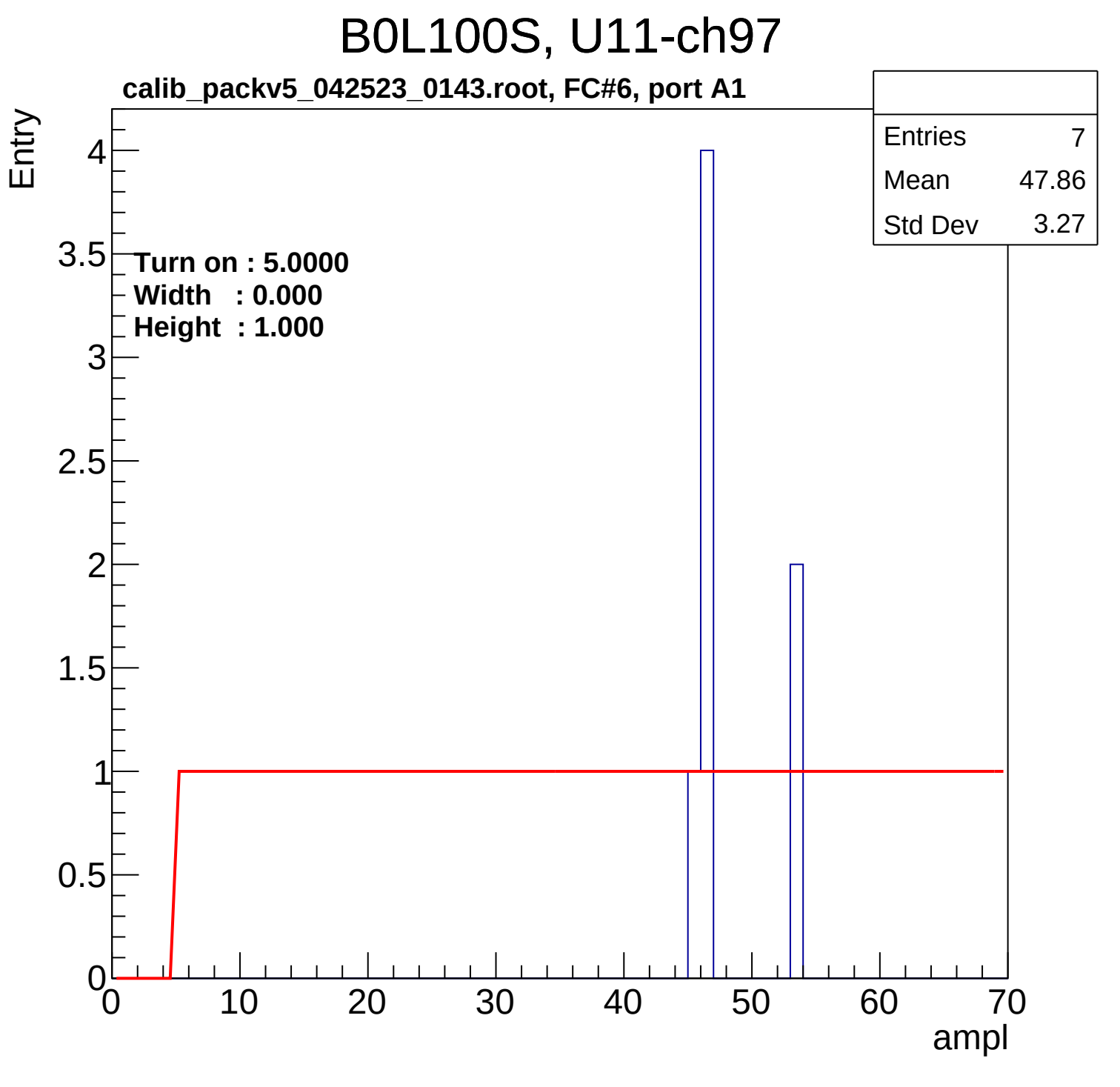
B0L100S, U11-ch97
calib_packv5_042523_0143.root, FC#6, port A1
Entries 7
Mean 47.86
Std Dev 3.27
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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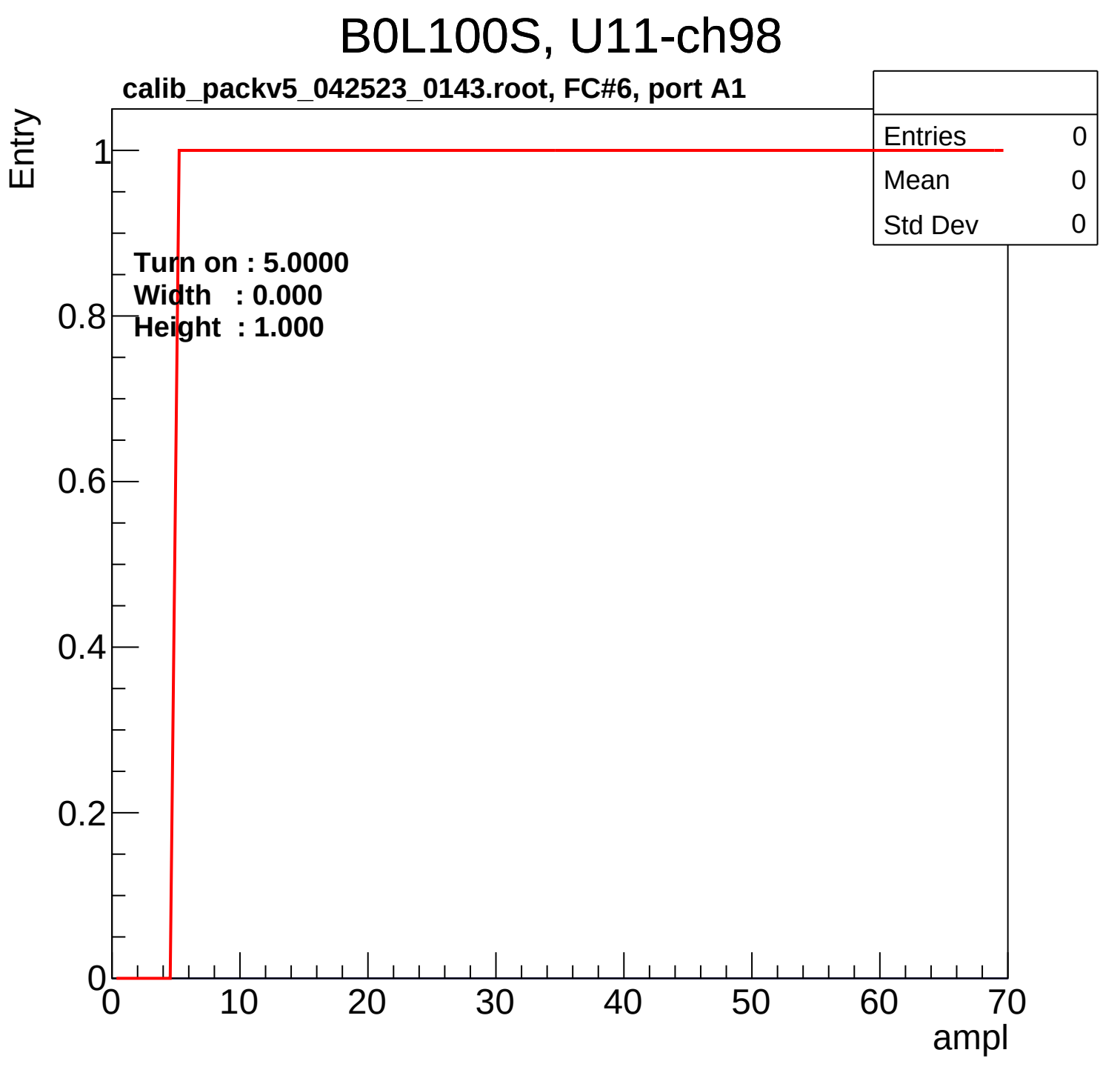
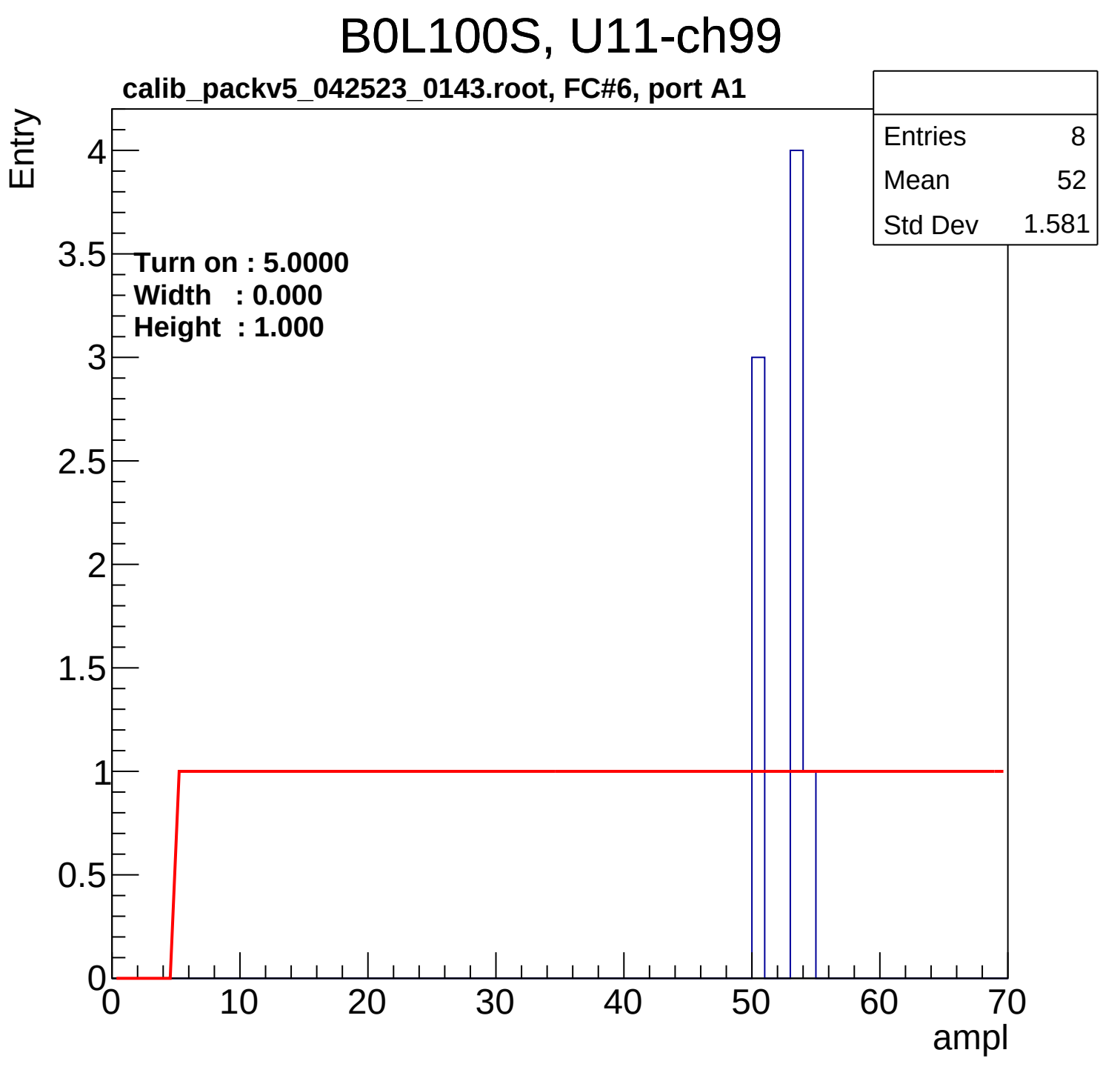
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B0L100S, U11-ch98
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U11-ch99
calib_packv5_042523_0143.root, FC#6, port A1
Entries 8
Mean 52
Std Dev 1.581
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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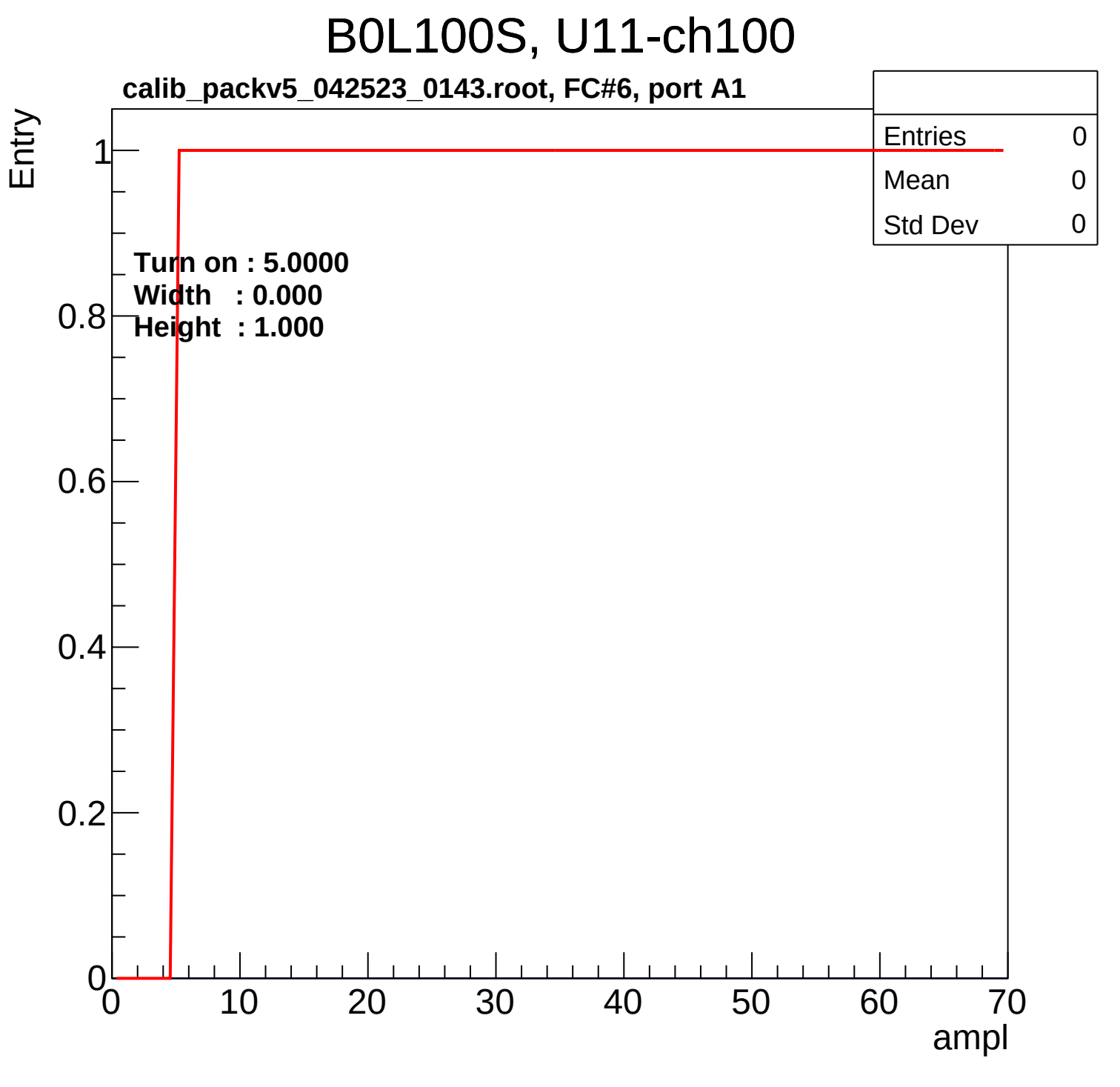
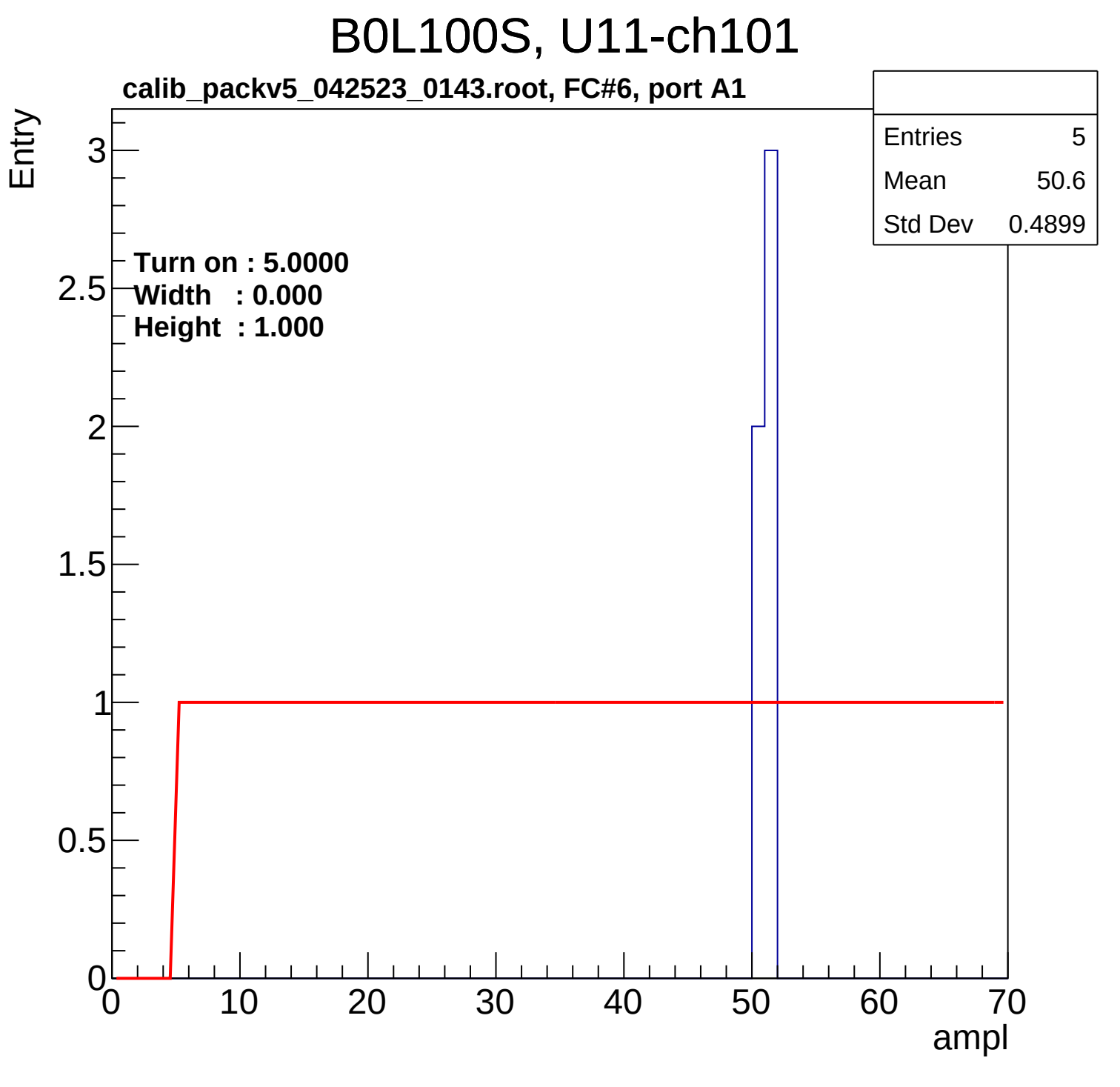
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B0L100S, U11-ch100
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U11-ch101
calib_packv5_042523_0143.root, FC#6, port A1
Entries 5
Mean 50.6
Std Dev 0.4899
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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40
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60
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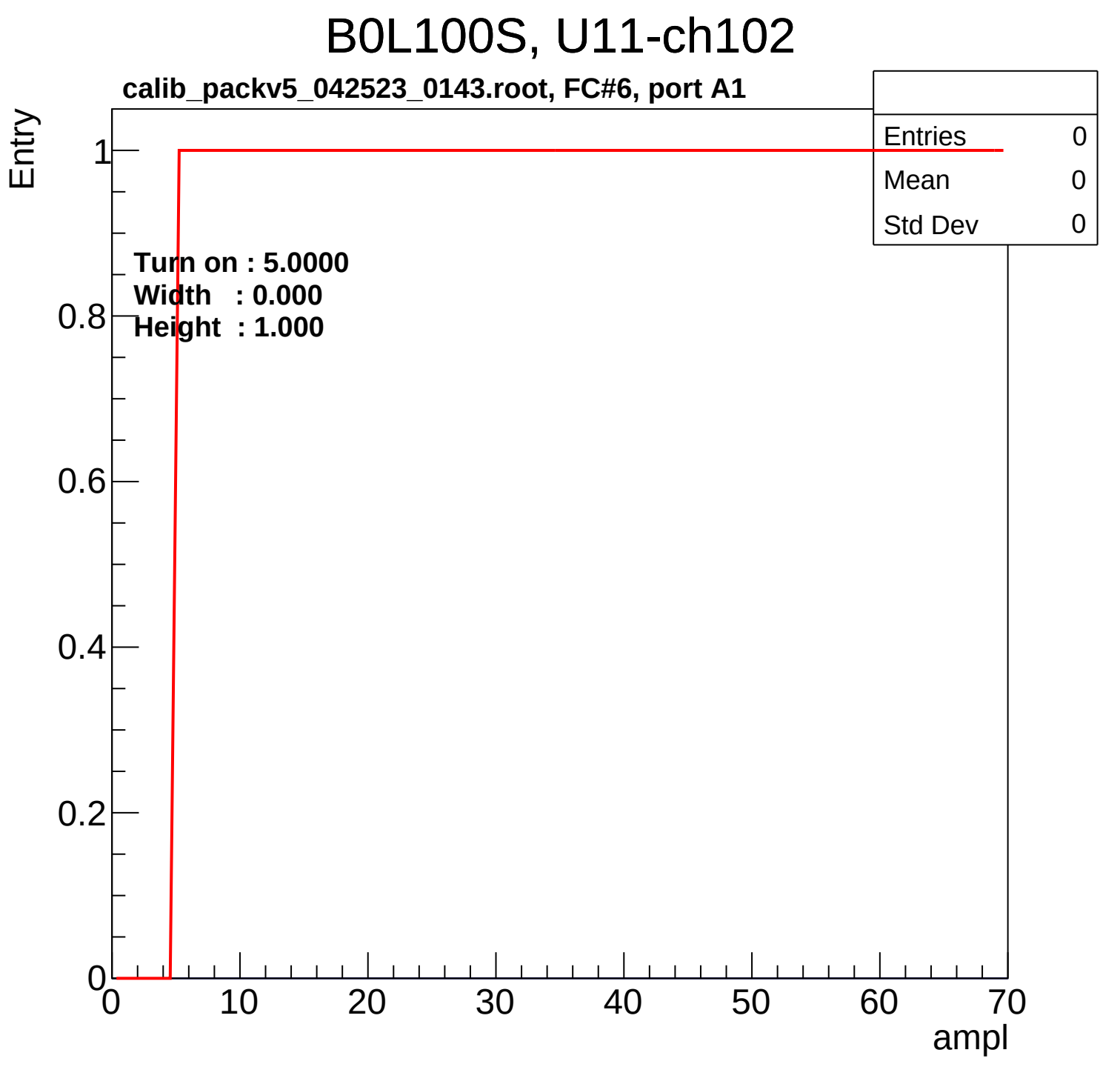
B0L100S, U11-ch102
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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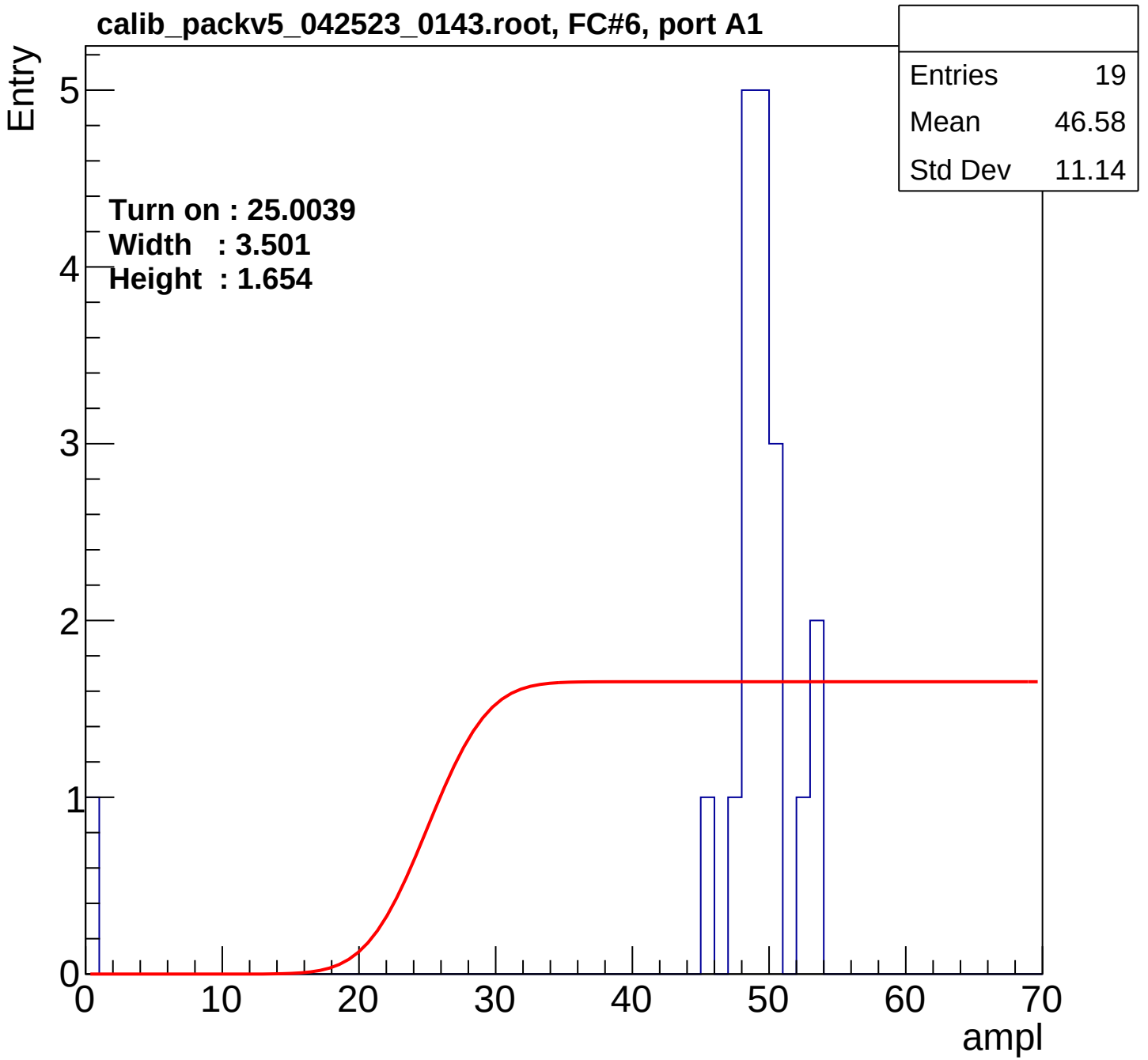
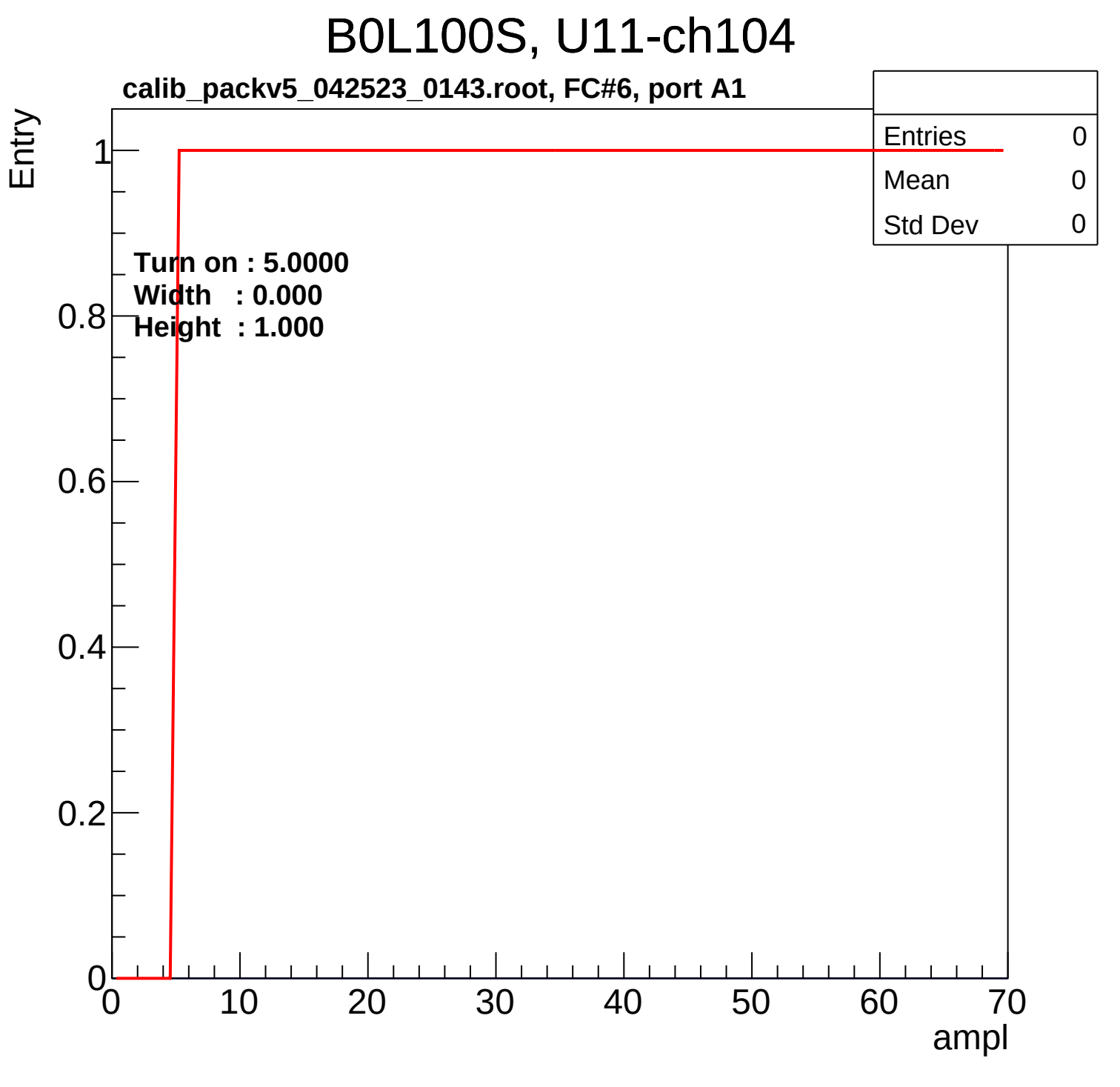
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U11-ch103
calib_packv5_042523_0143.root, FC#6, port A1
Entries 19
Mean 46.58
Std Dev 11.14
Turn on : 25.0039
Width : 3.501
Height : 1.654
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U11-ch104
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.8
0.6
0.4
0.2
0
0
10
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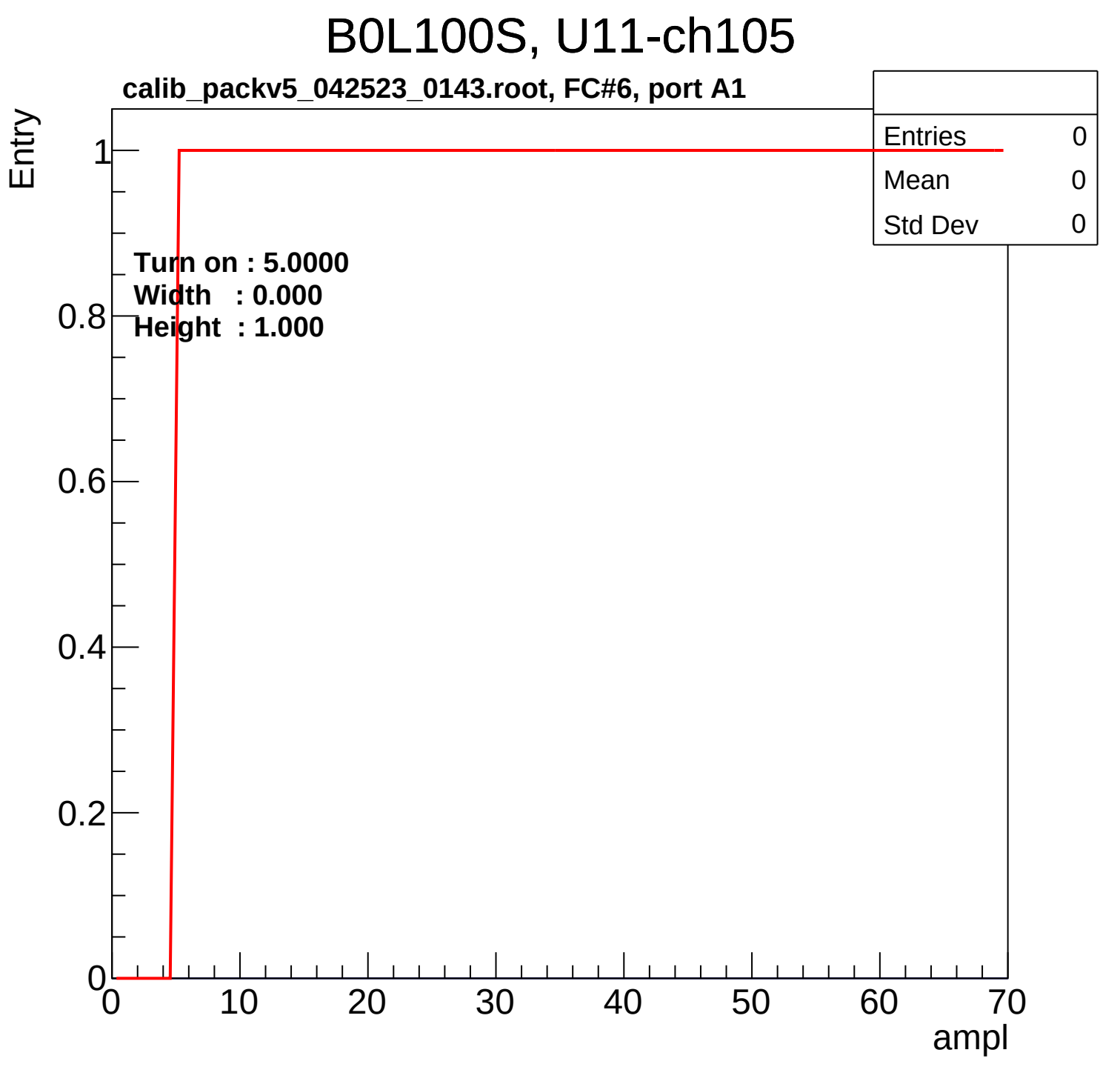
30
40
50
60
70
ampl


B0L100S, U11-ch105
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.8
0.6
0.4
0.2
0
0
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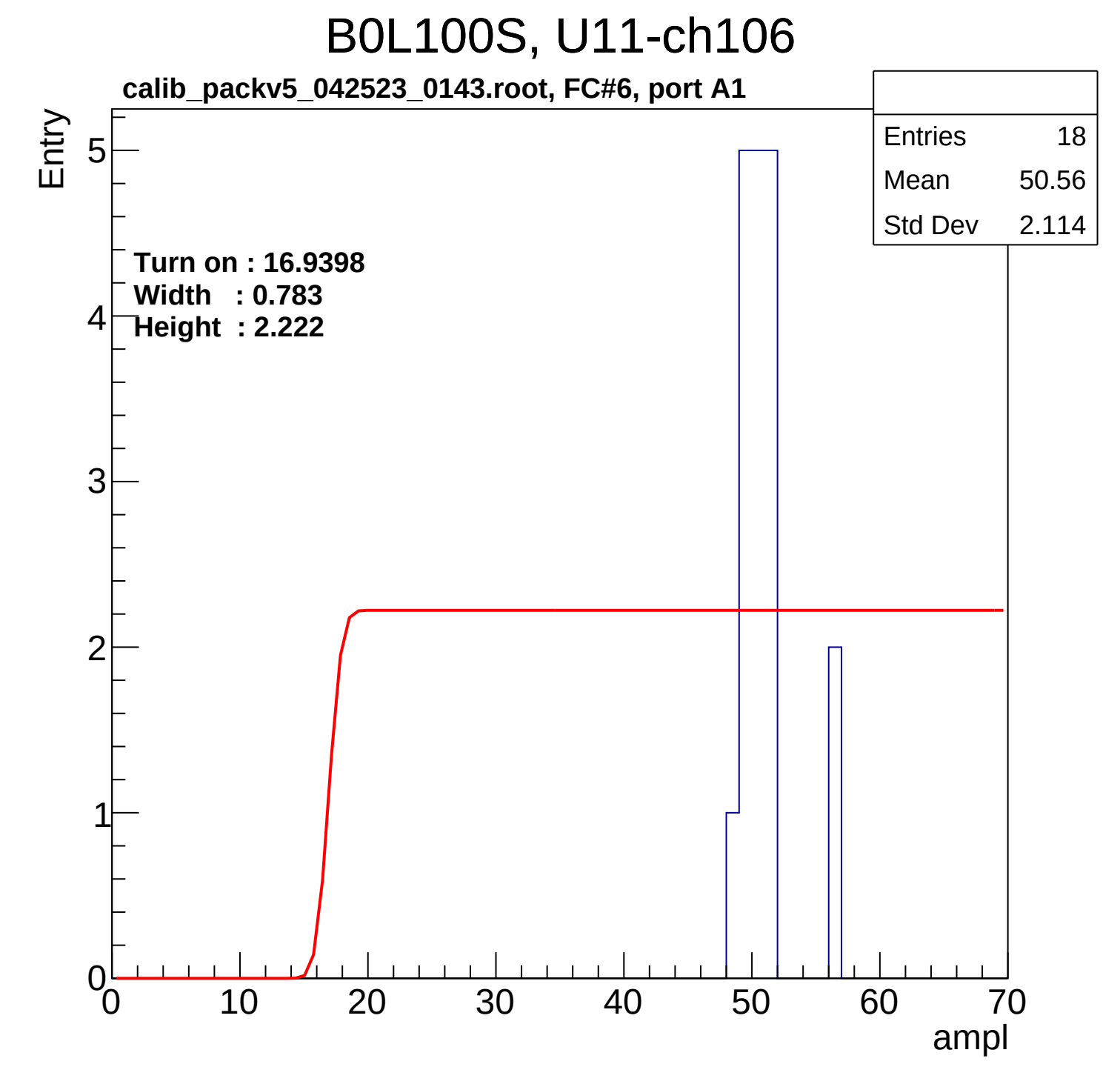
60
70
ampl


B0L100S, U11-ch106
calib_packv5_042523_0143.root, FC#6, port A1
Entries 18
Mean 50.56
Std Dev 2.114
Turn on : 16.9398
Width : 0.783
Height : 2.222
Entry
ampl
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4
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0
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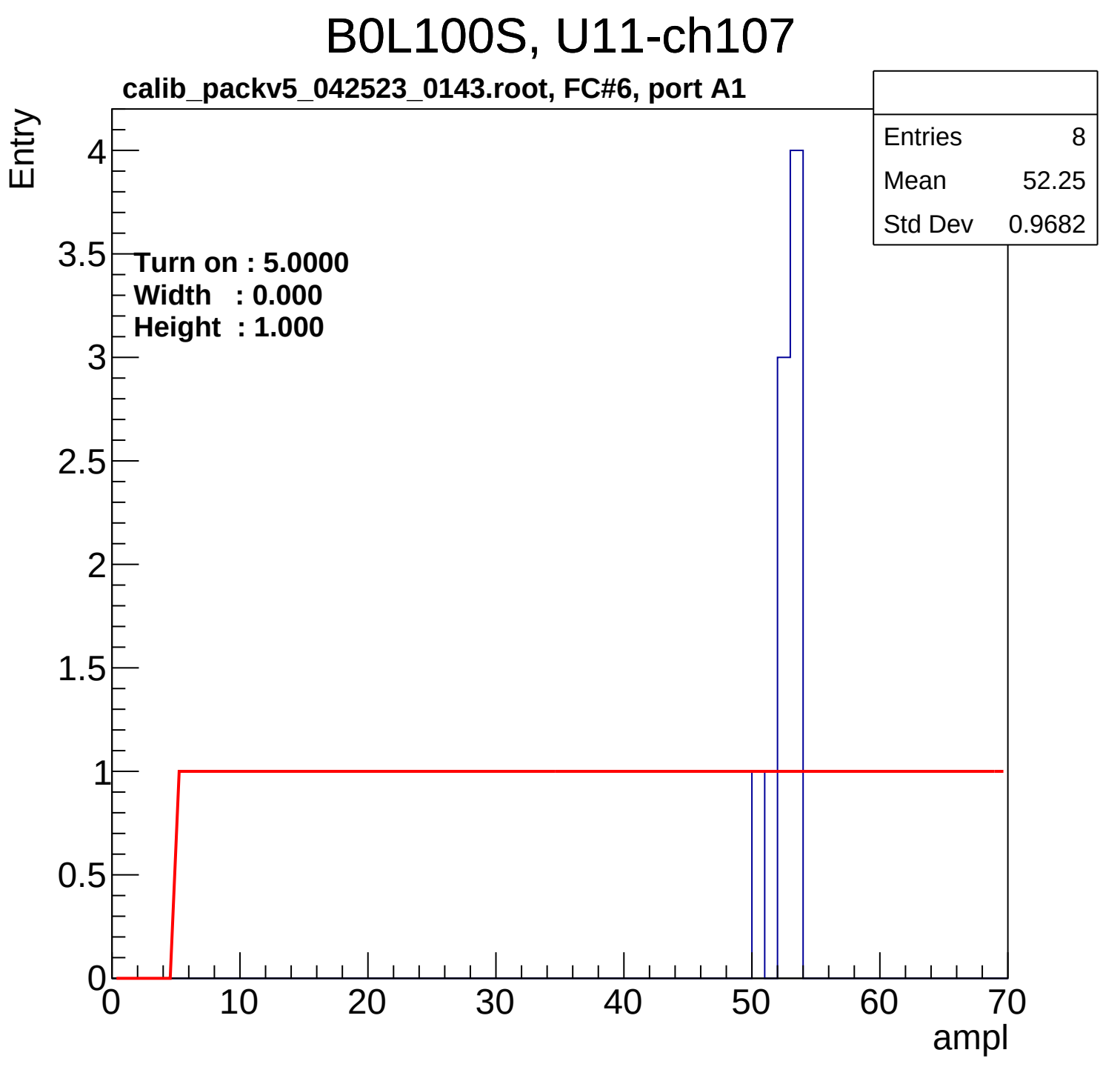
B0L100S, U11-ch107
calib_packv5_042523_0143.root, FC#6, port A1
Entries 8
Mean 52.25
Std Dev 0.9682
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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1.5
2
2.5
3
3.5
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0
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60
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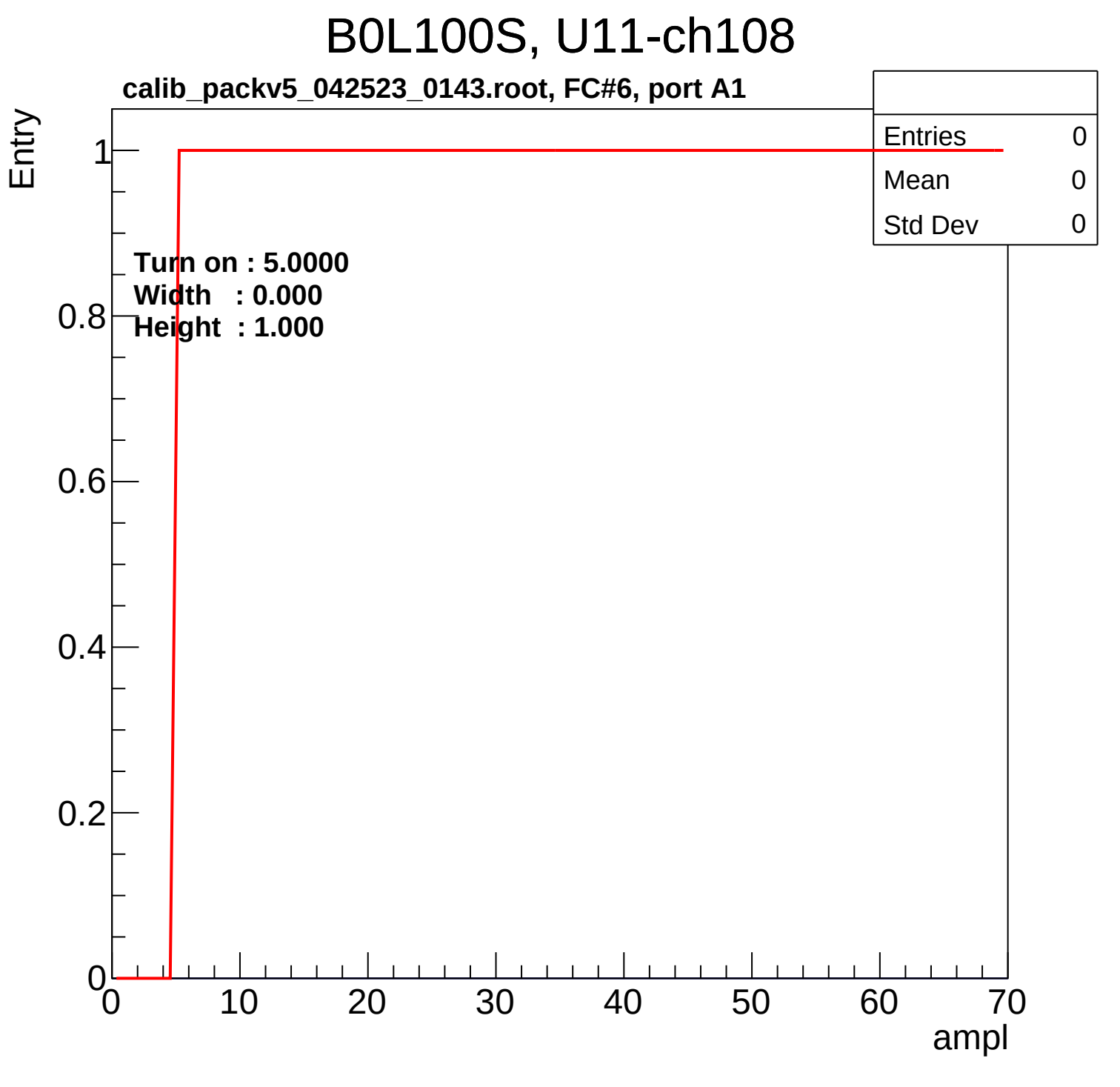
B0L100S, U11-ch108
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
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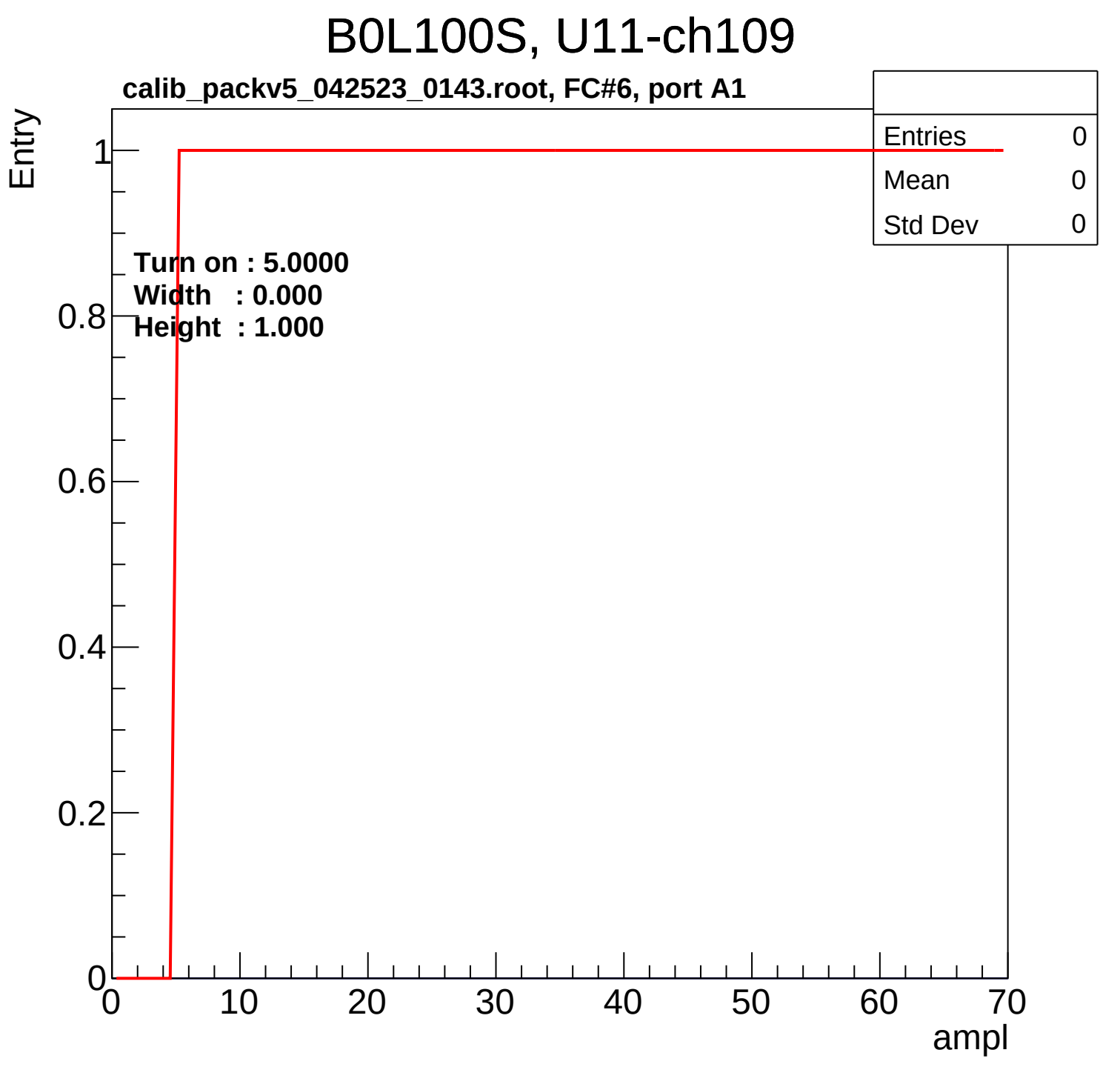
40
50
60
70


B0L100S, U11-ch109
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.8
0.6
0.4
0.2
0
0
10
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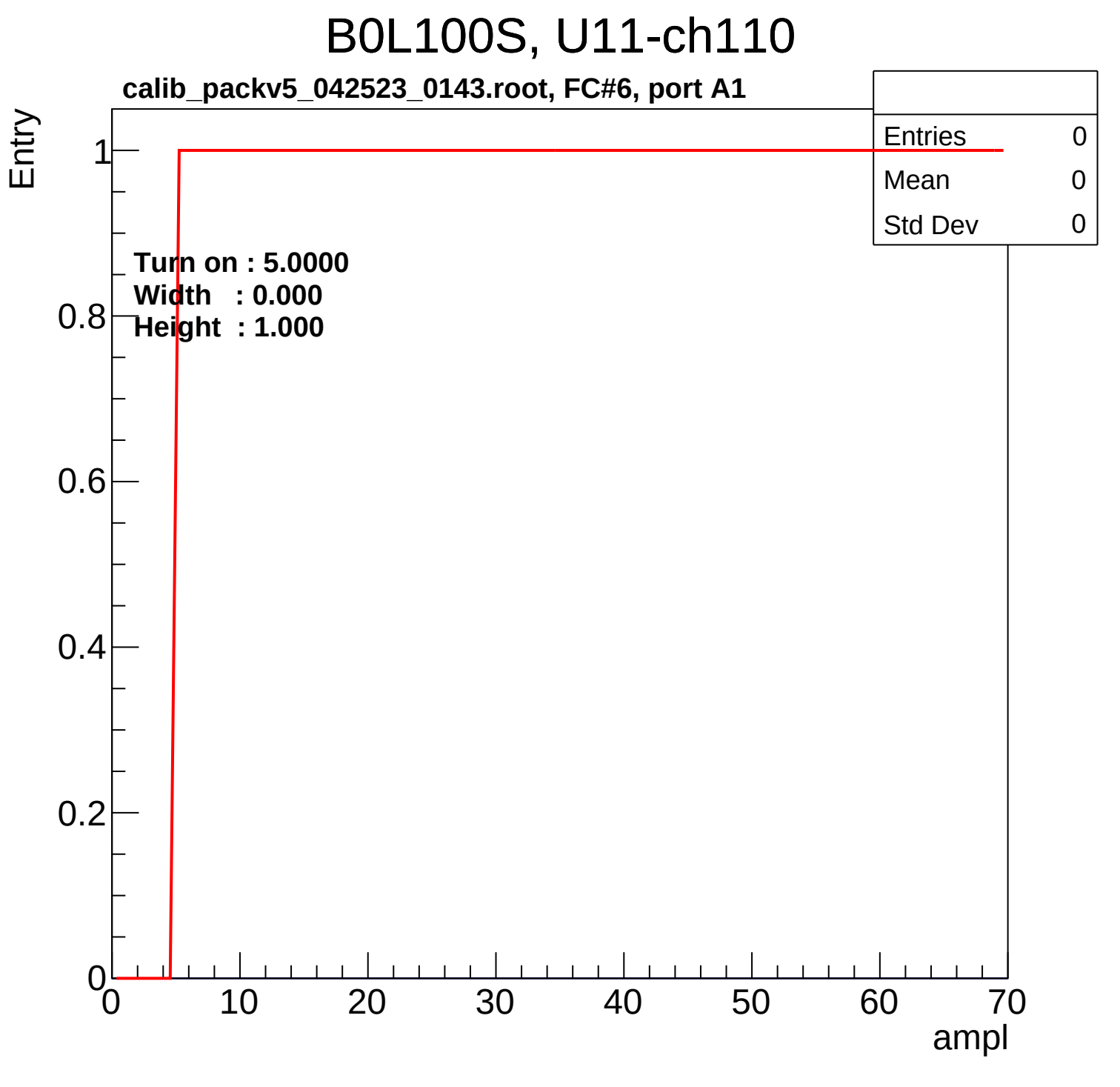
60
70
ampl


B0L100S, U11-ch110
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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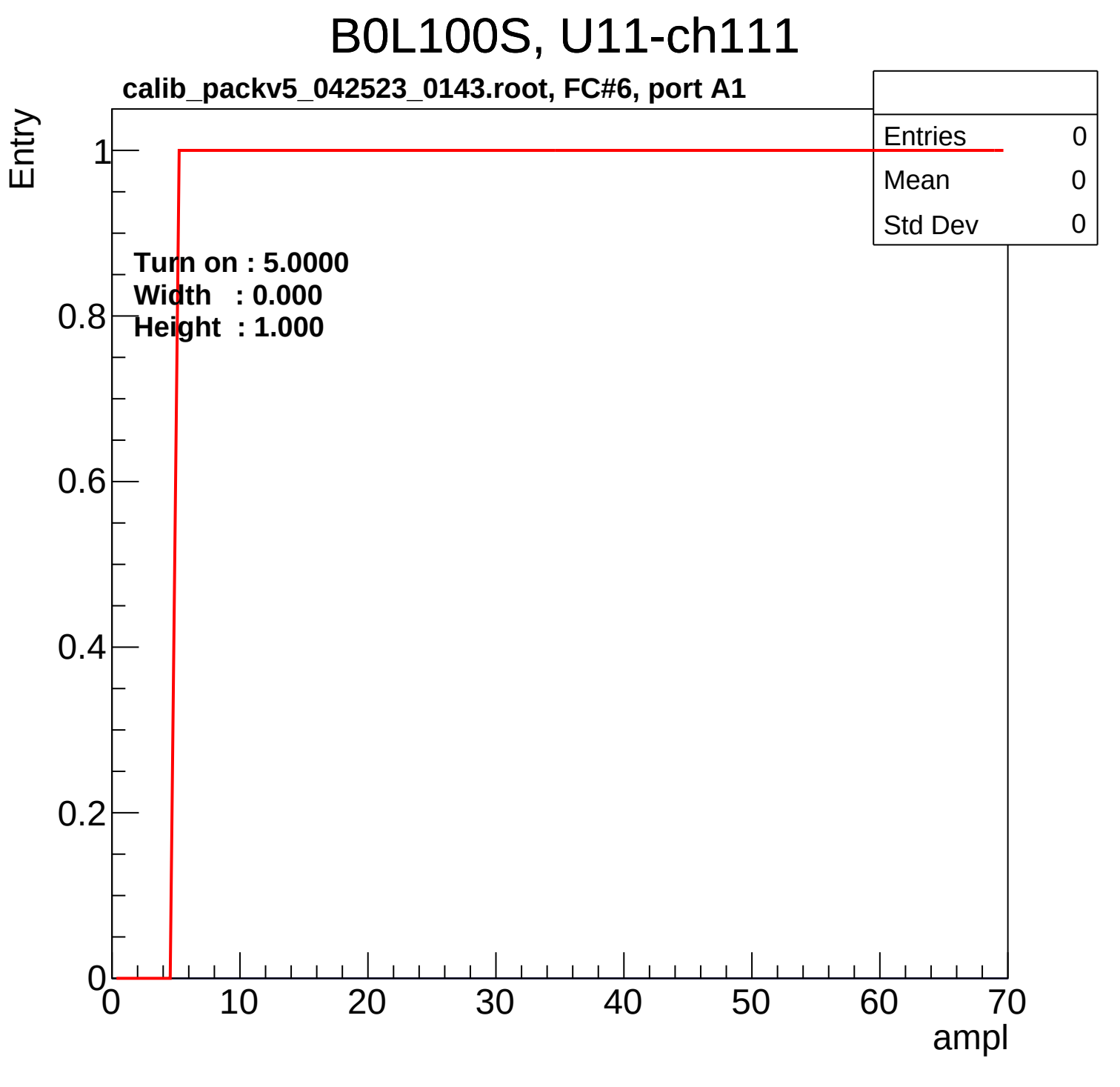
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U11-ch111
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.6
0.4
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10
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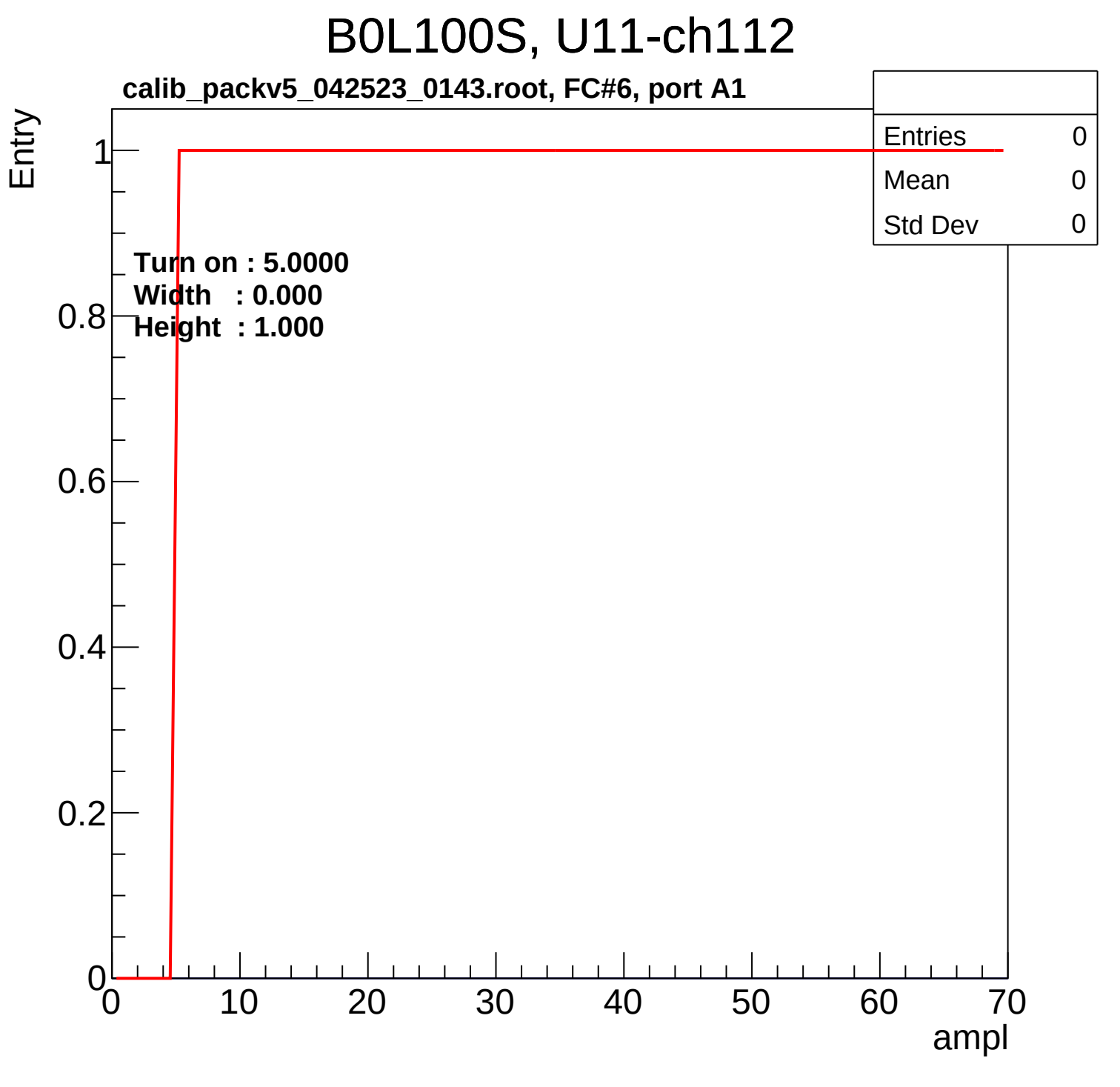
50
60
70
ampl


B0L100S, U11-ch112
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.2
0.4
0.6
0.8
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0
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20
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60
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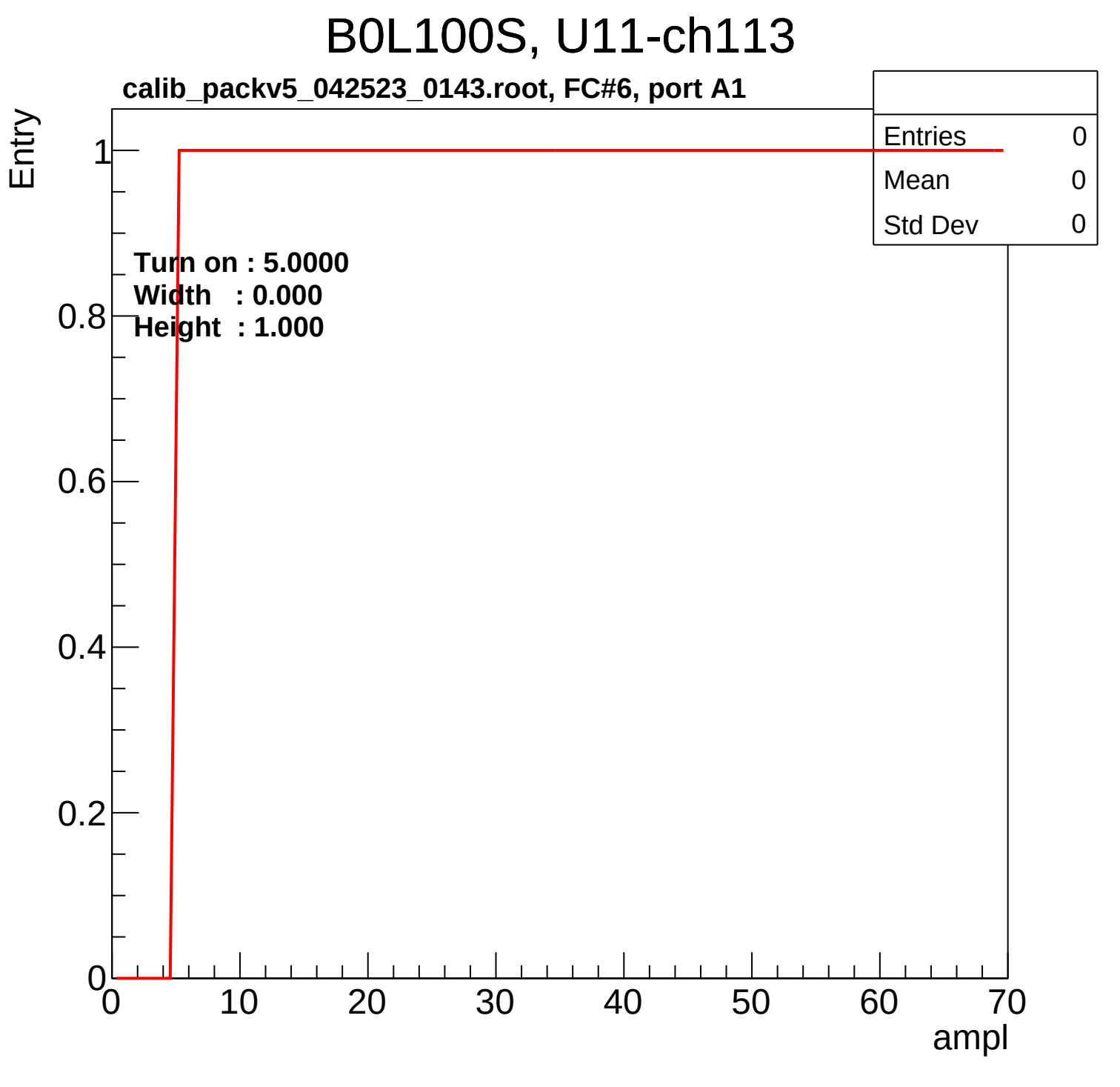
B0L100S, U11-ch113
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.6
0.4
0.2
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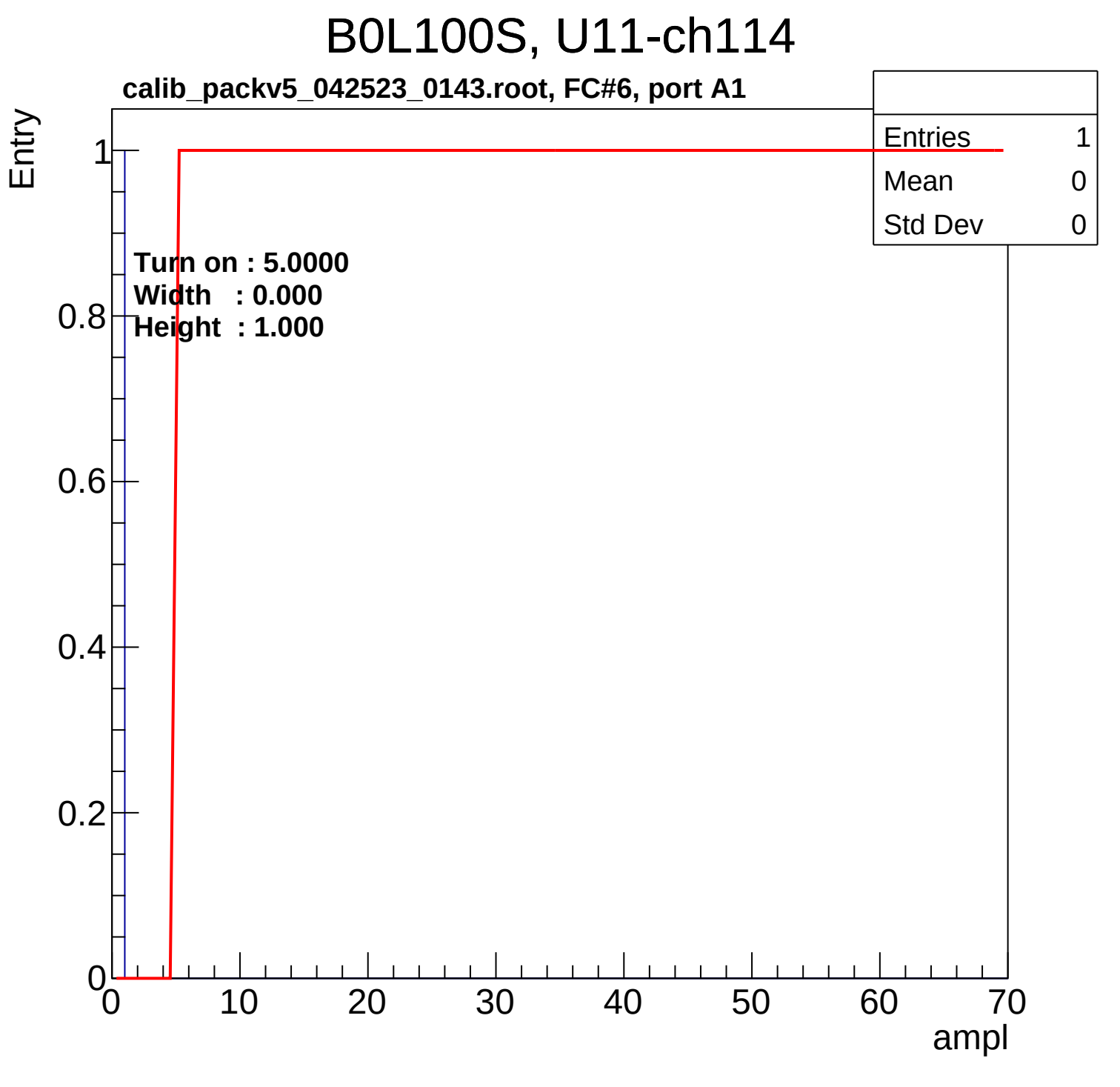
ampl


B0L100S, U11-ch114
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.6
0.4
0.2
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10
20
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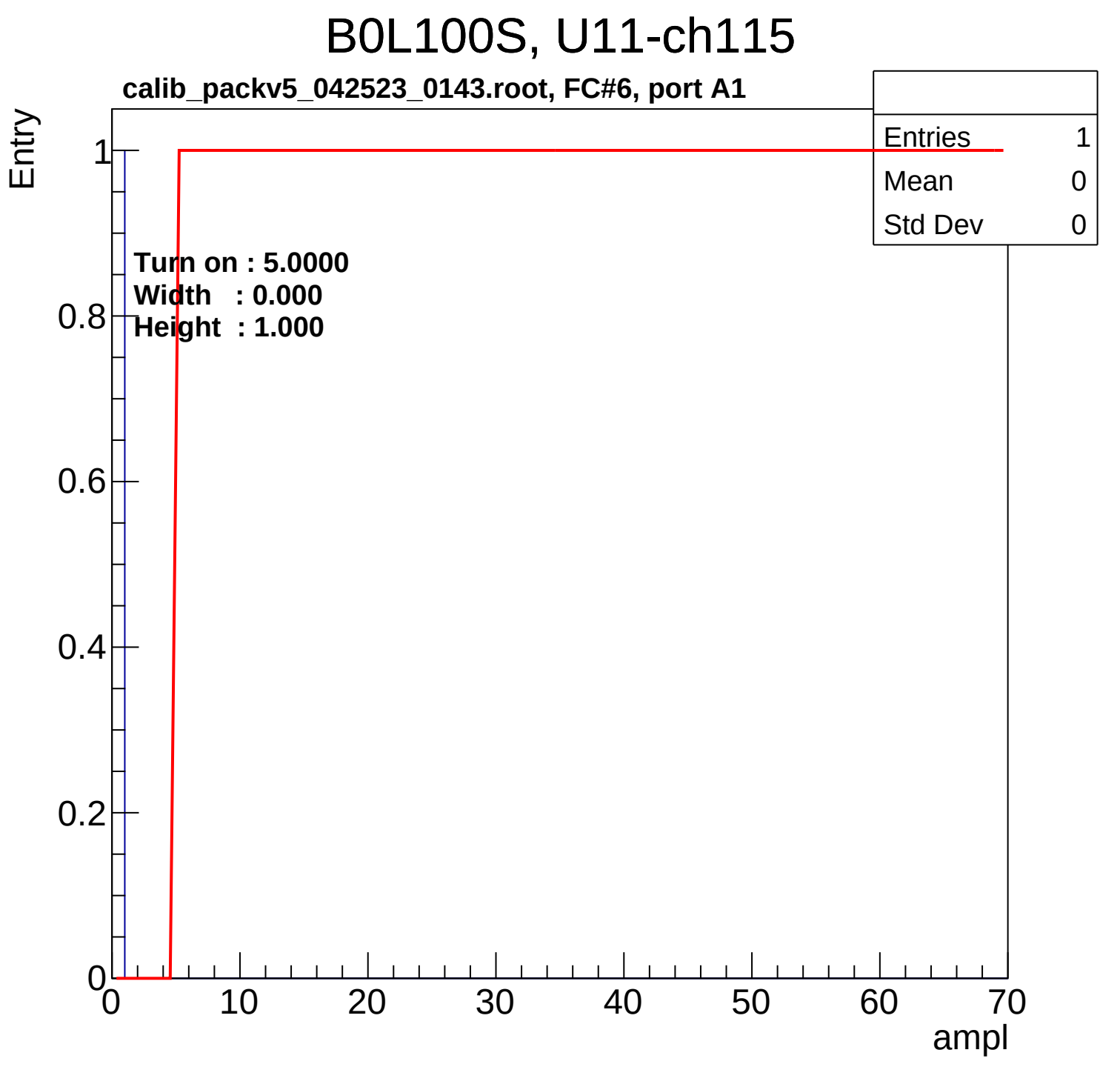
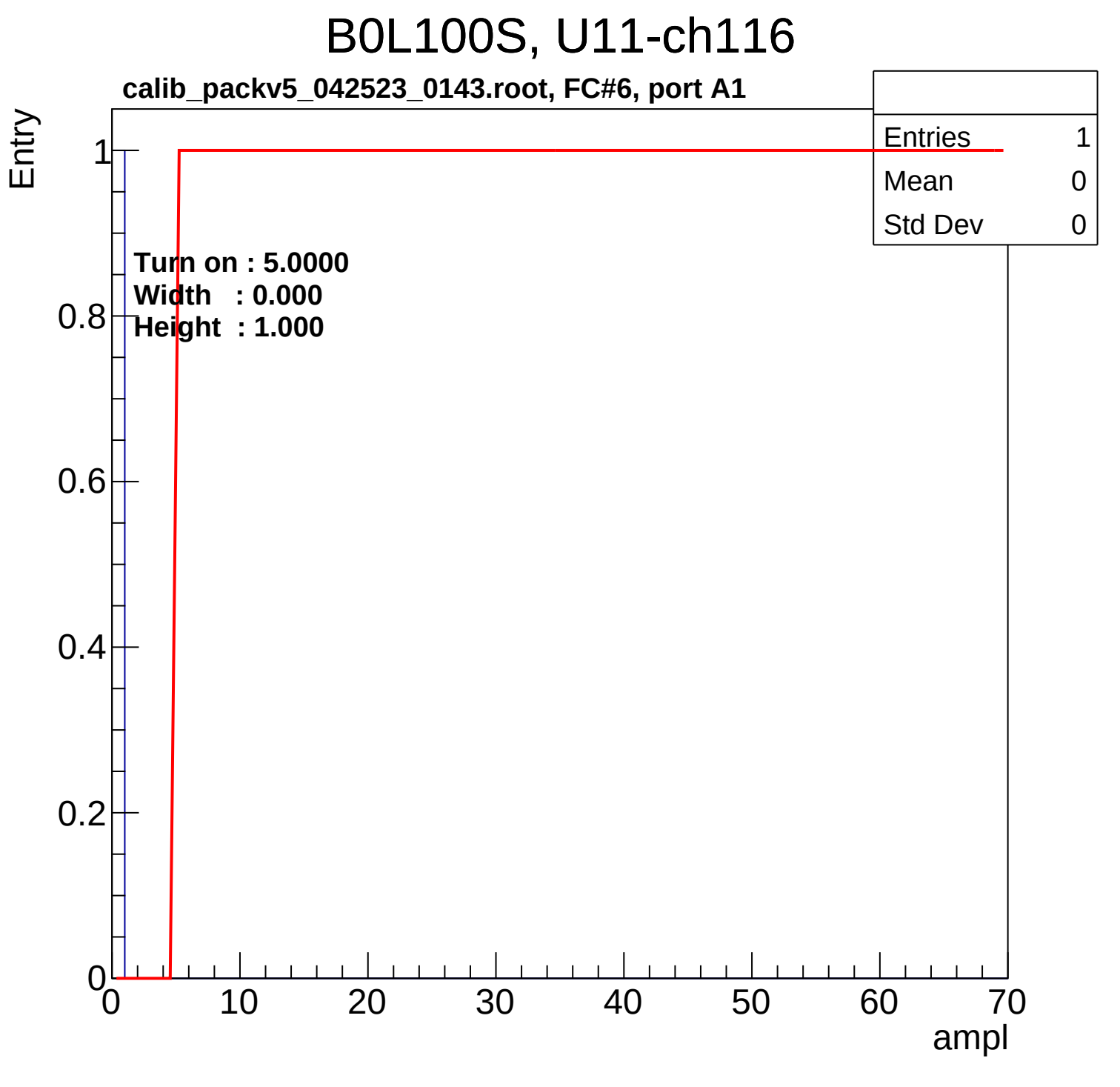
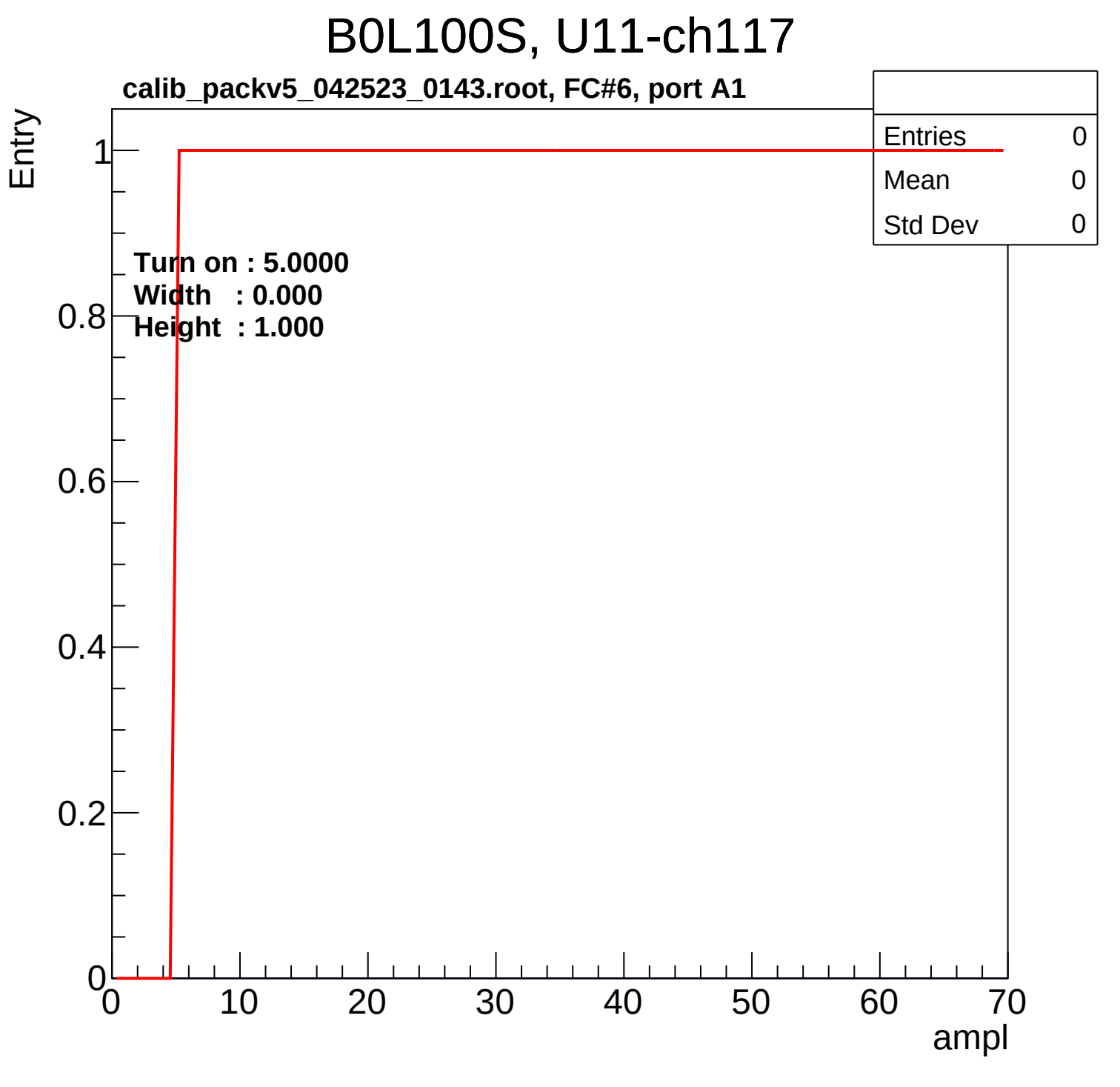
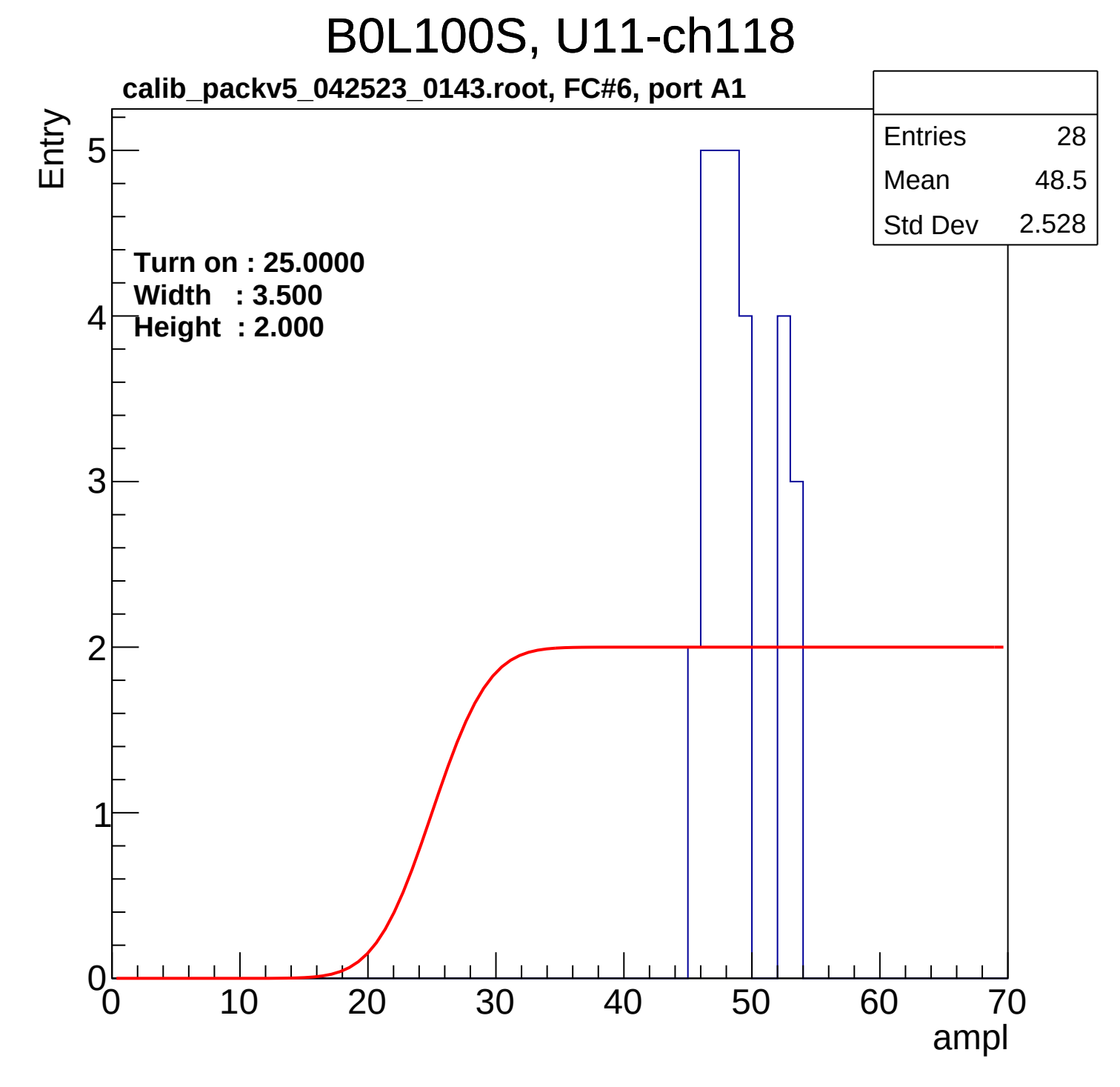
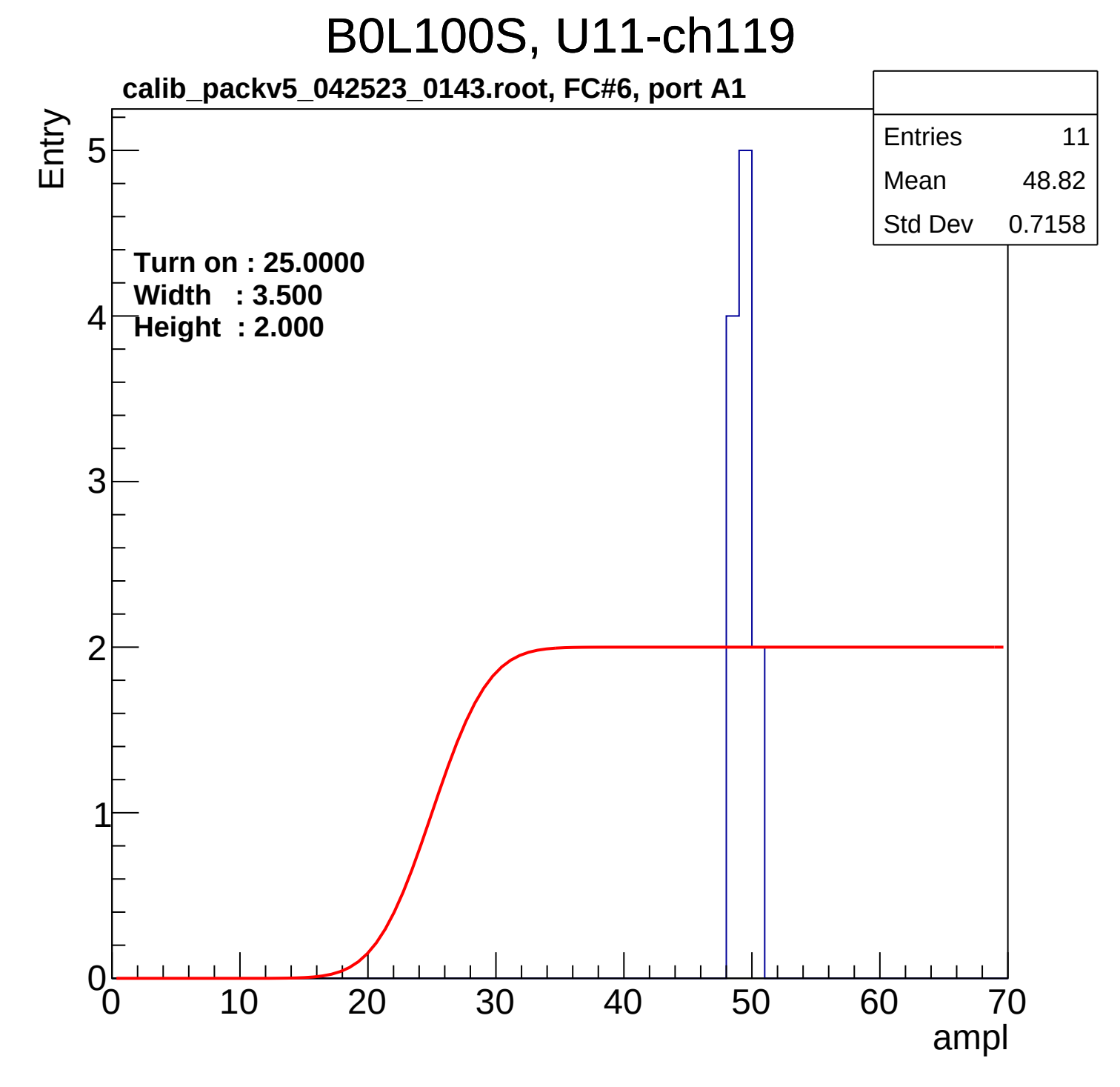
50
60
70
ampl

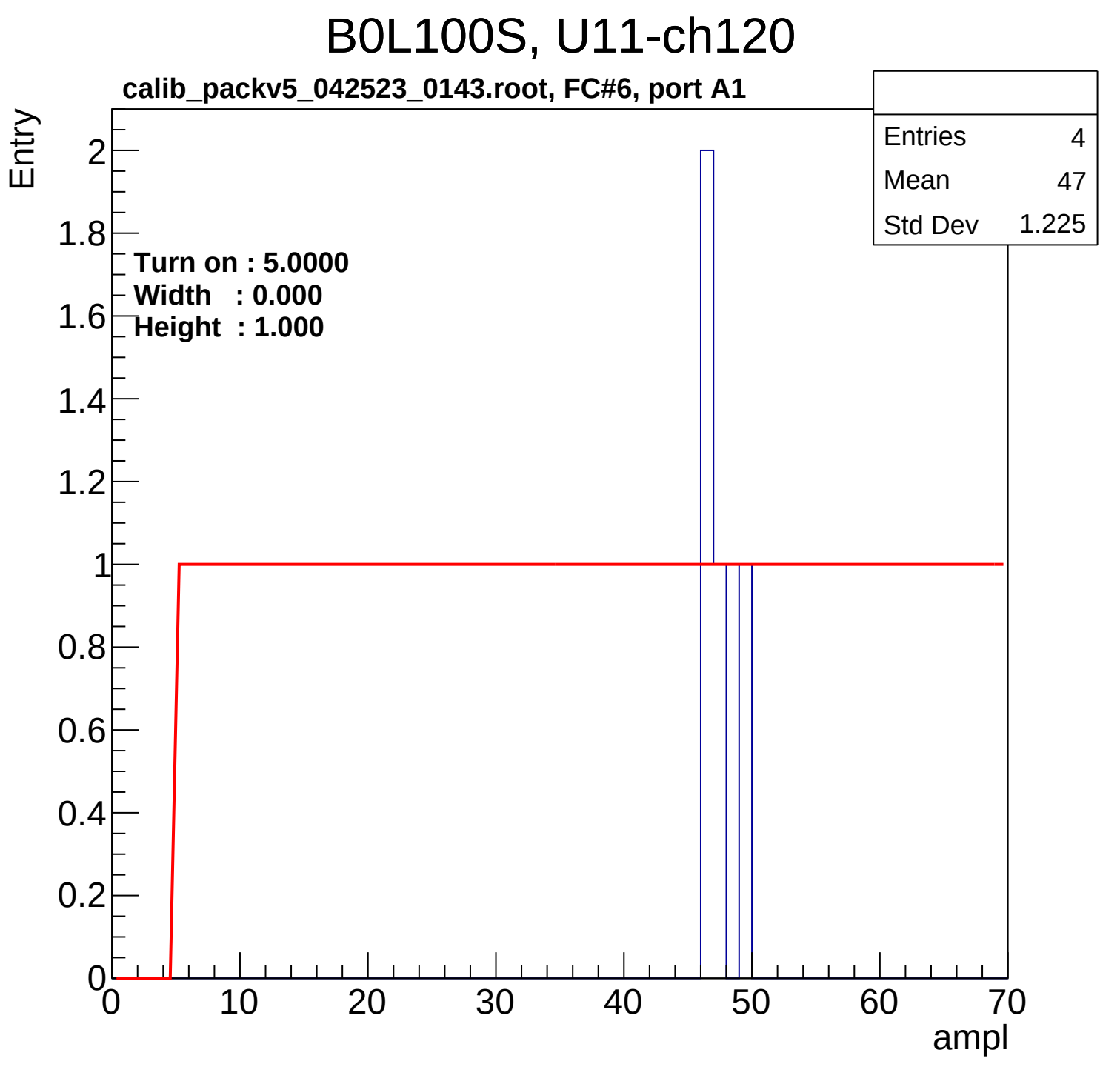

B0L100S, U11-ch115
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

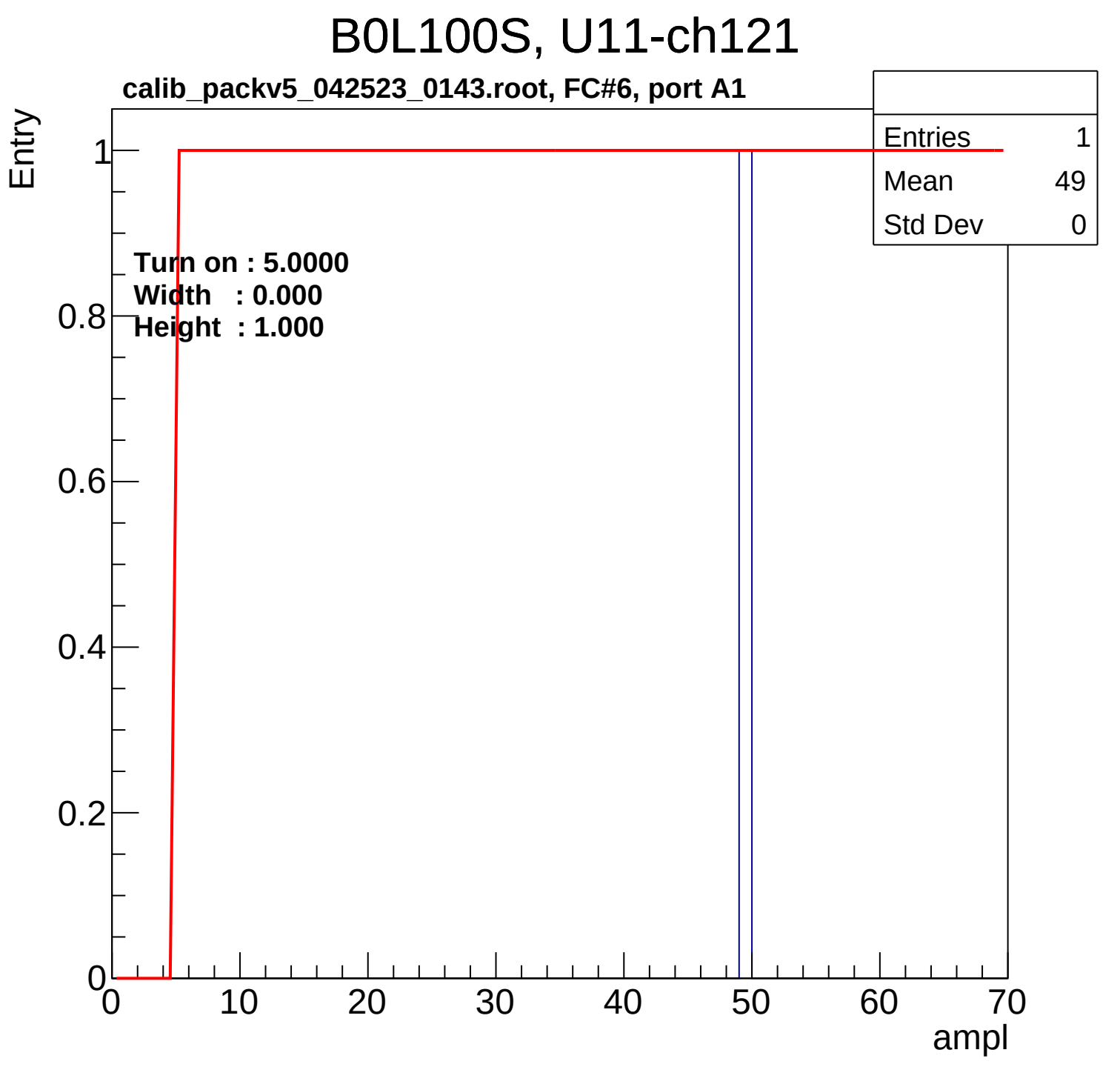

B0L100S, U11-ch116
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

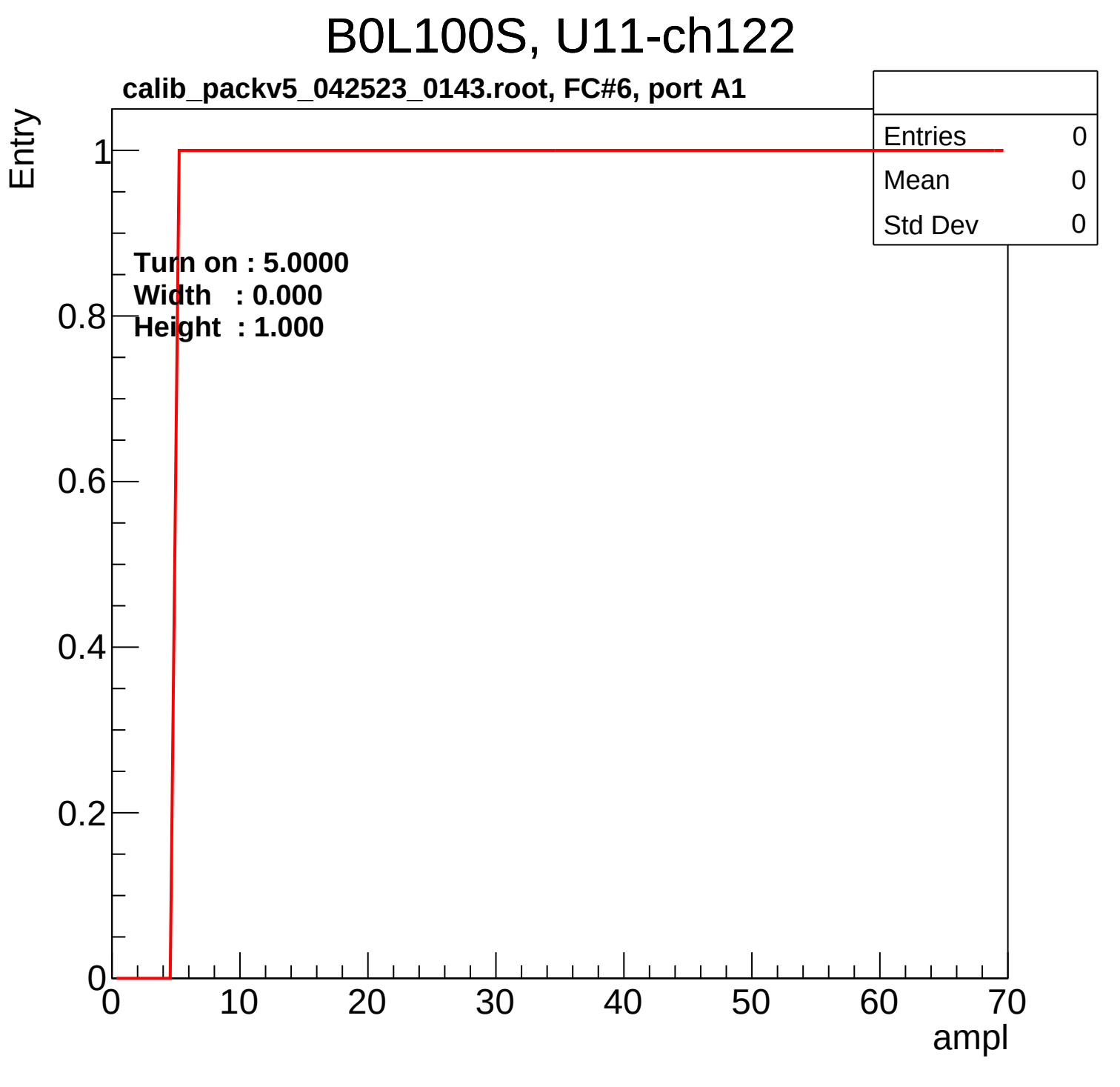

B0L100S, U11-ch117
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

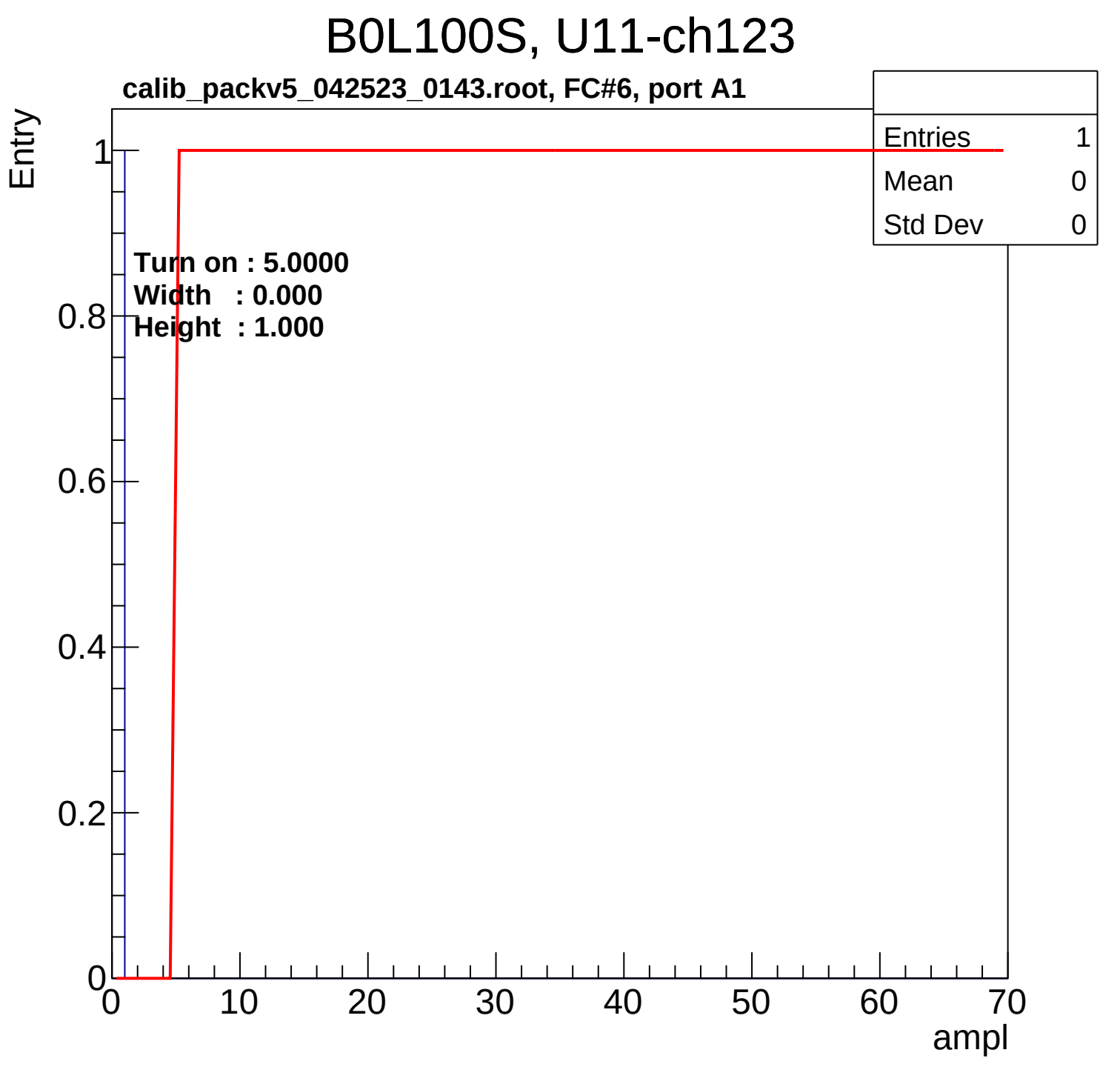

B0L100S, U11-ch118
calib_packv5_042523_0143.root, FC#6, port A1
Entries 28
Mean 48.5
Std Dev 2.528
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

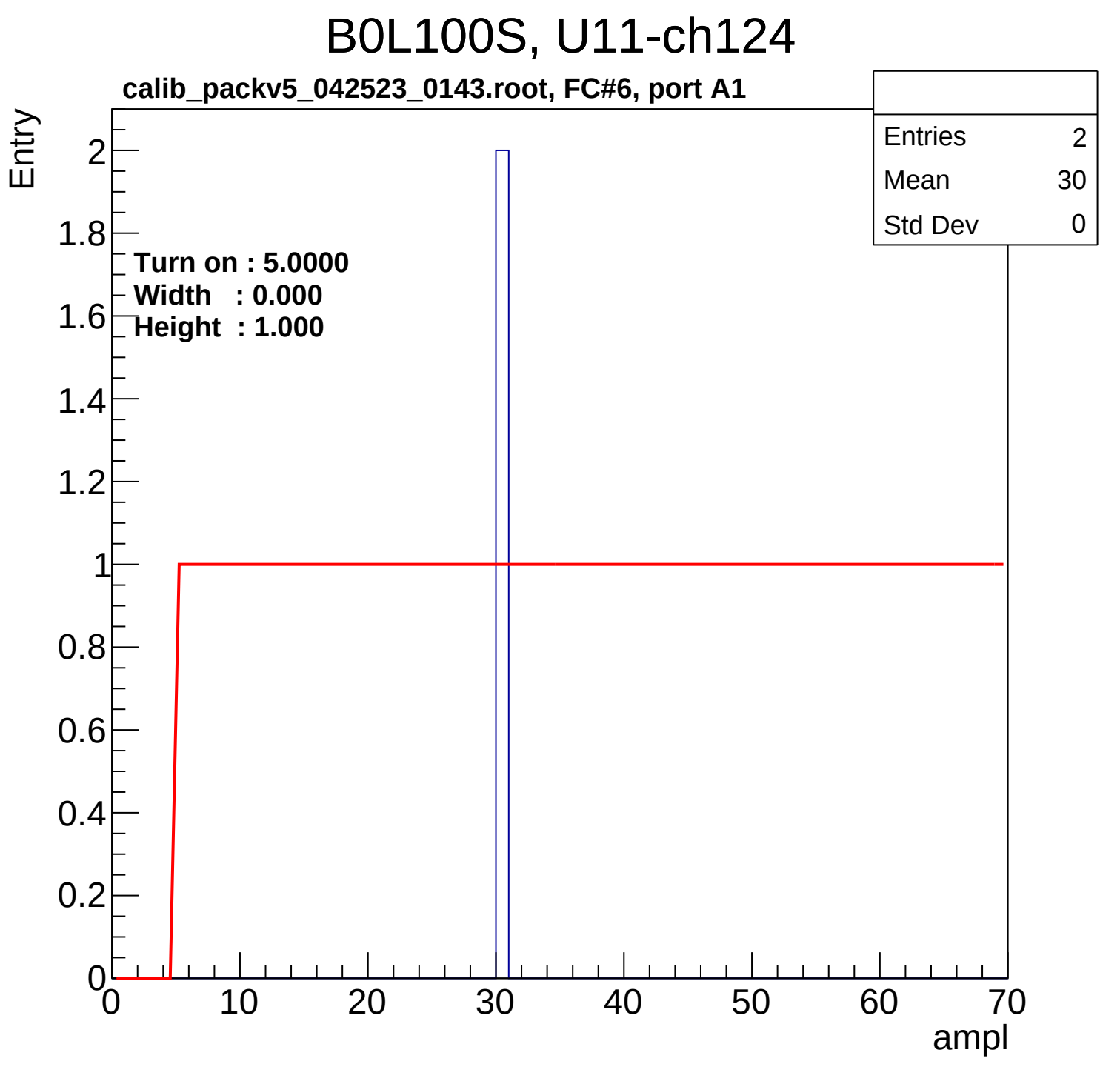

B0L100S, U11-ch119
calib_packv5_042523_0143.root, FC#6, port A1
Entries 11
Mean 48.82
Std Dev 0.7158
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

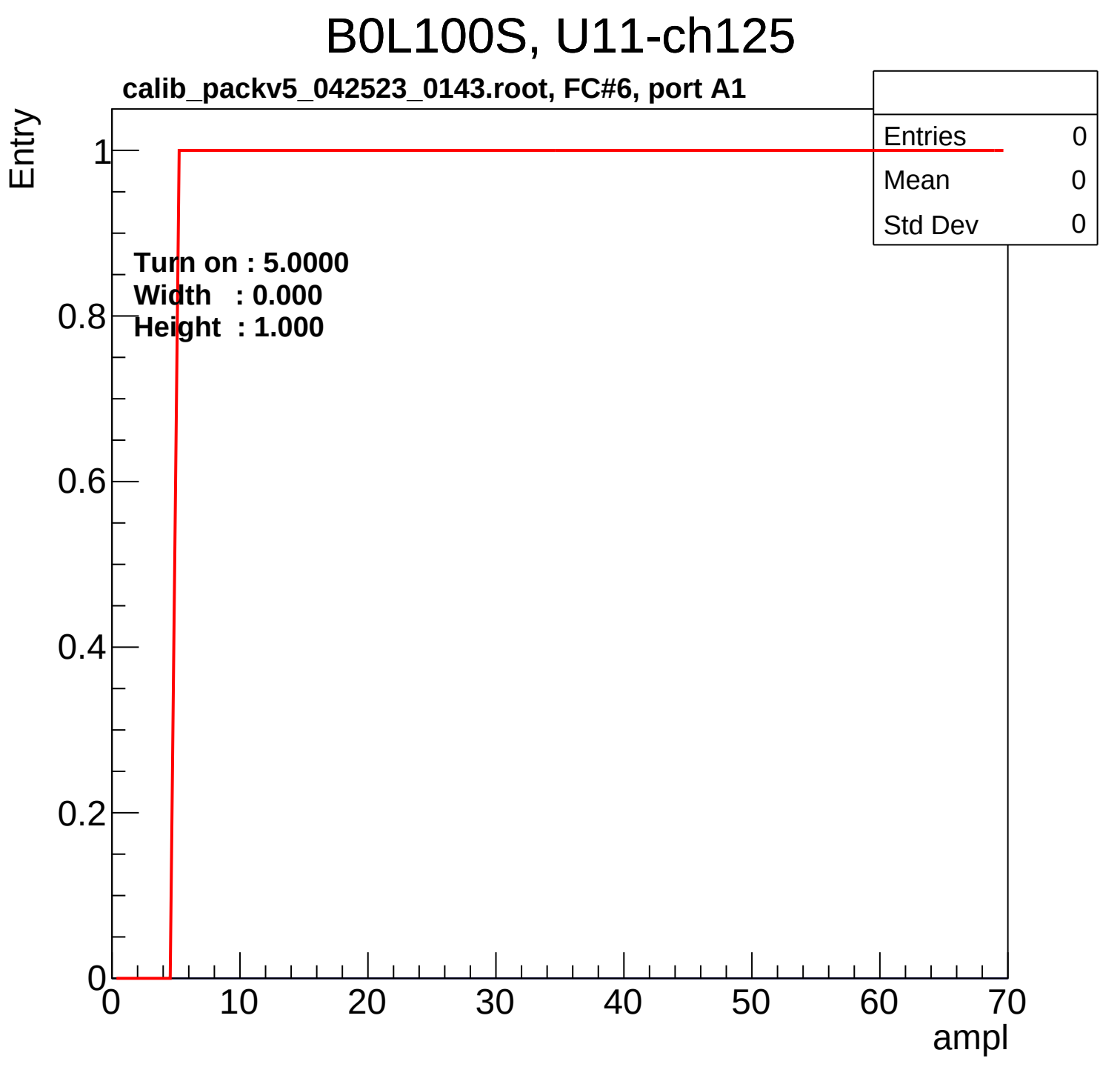

B0L100S, U11-ch120
calib_packv5_042523_0143.root, FC#6, port A1
Entries 4
Mean 47
Std Dev 1.225
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

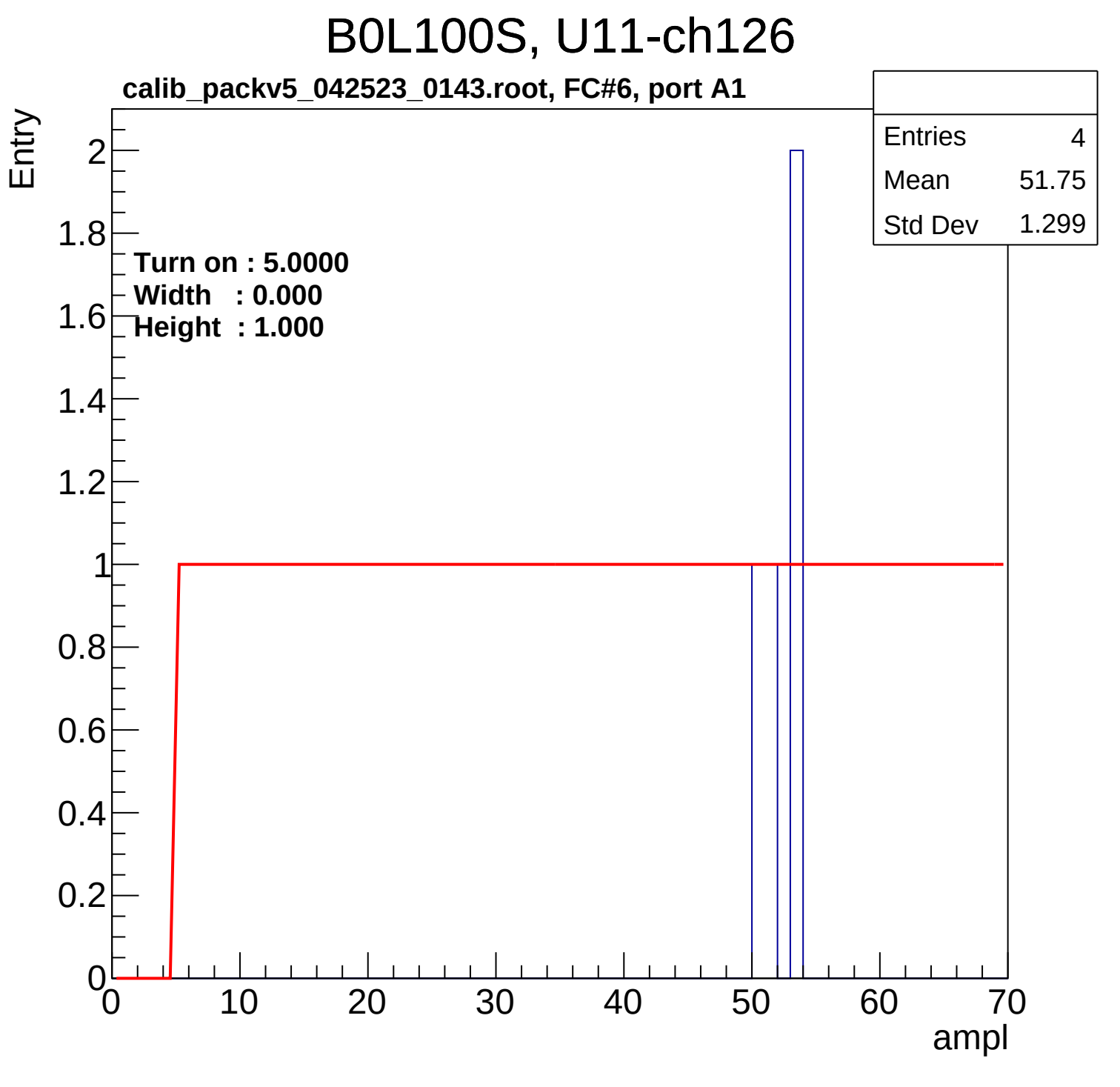

B0L100S, U11-ch121
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 49
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

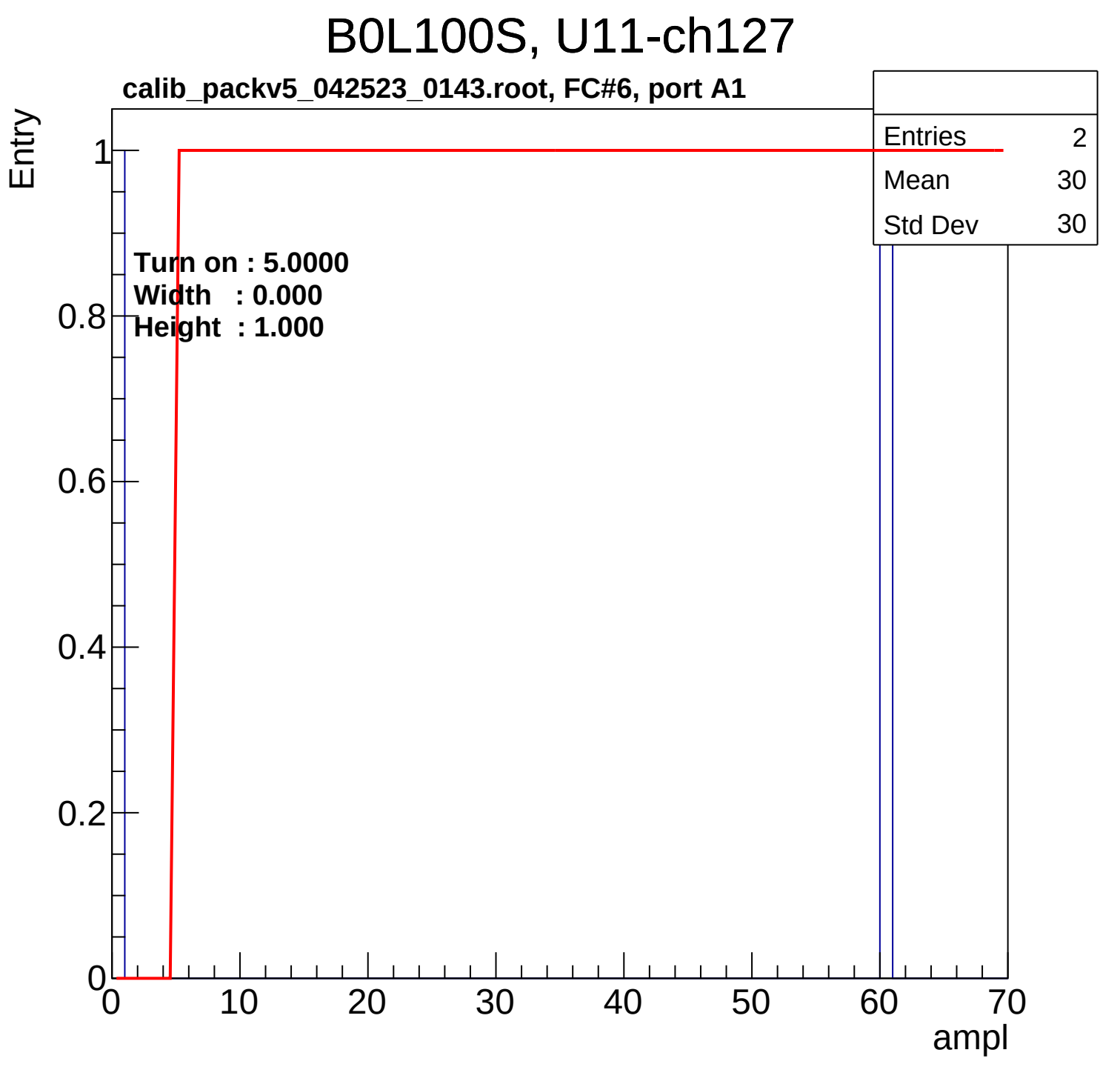

B0L100S, U11-ch122
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

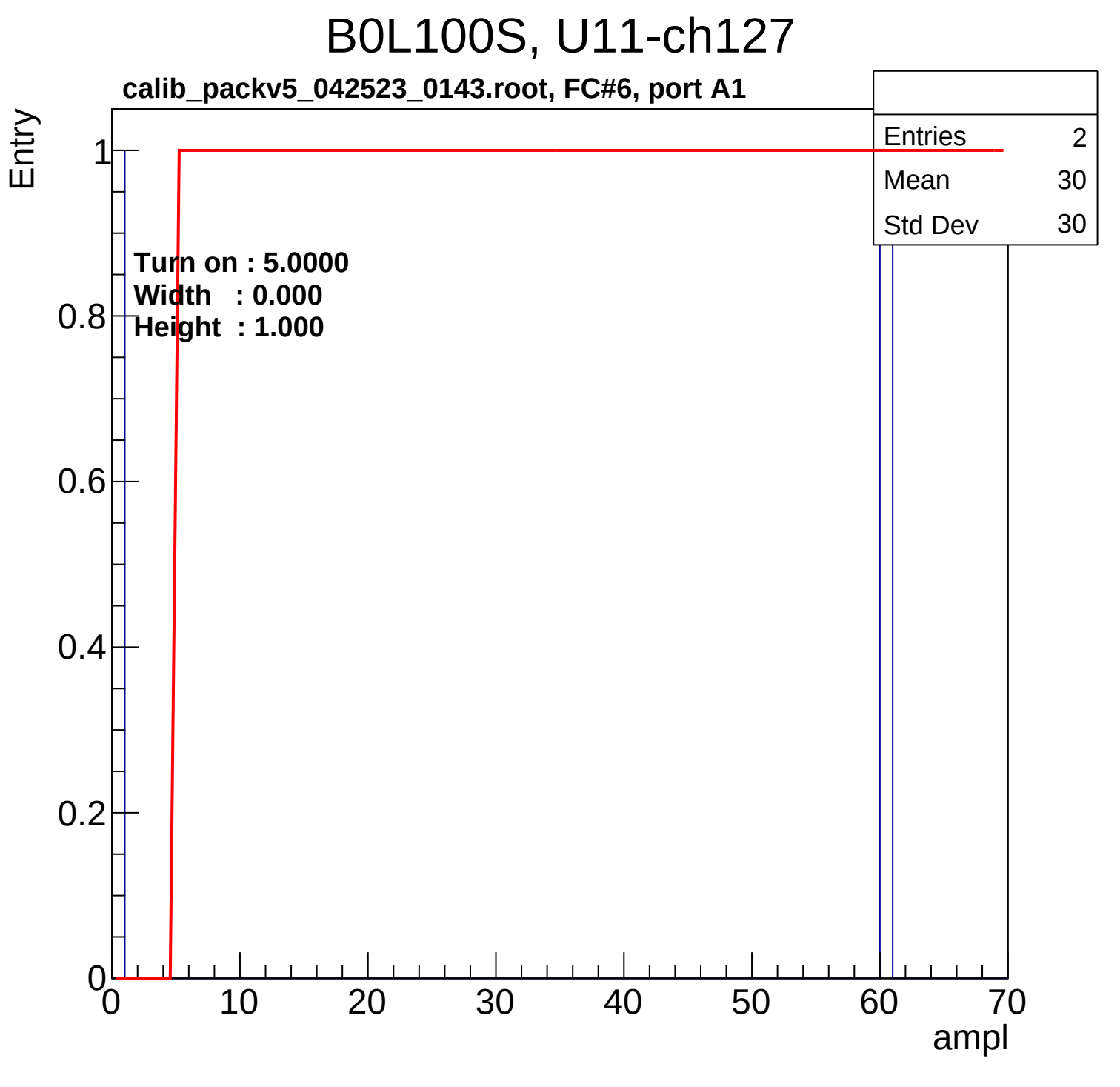

B0L100S, U11-ch123
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U11-ch124
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 30
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L100S, U11-ch125
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U11-ch126
calib_packv5_042523_0143.root, FC#6, port A1
Entries 4
Mean 51.75
Std Dev 1.299
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L100S, U11-ch127
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 30
Std Dev 30
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U11-ch127
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 30
Std Dev 30
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70