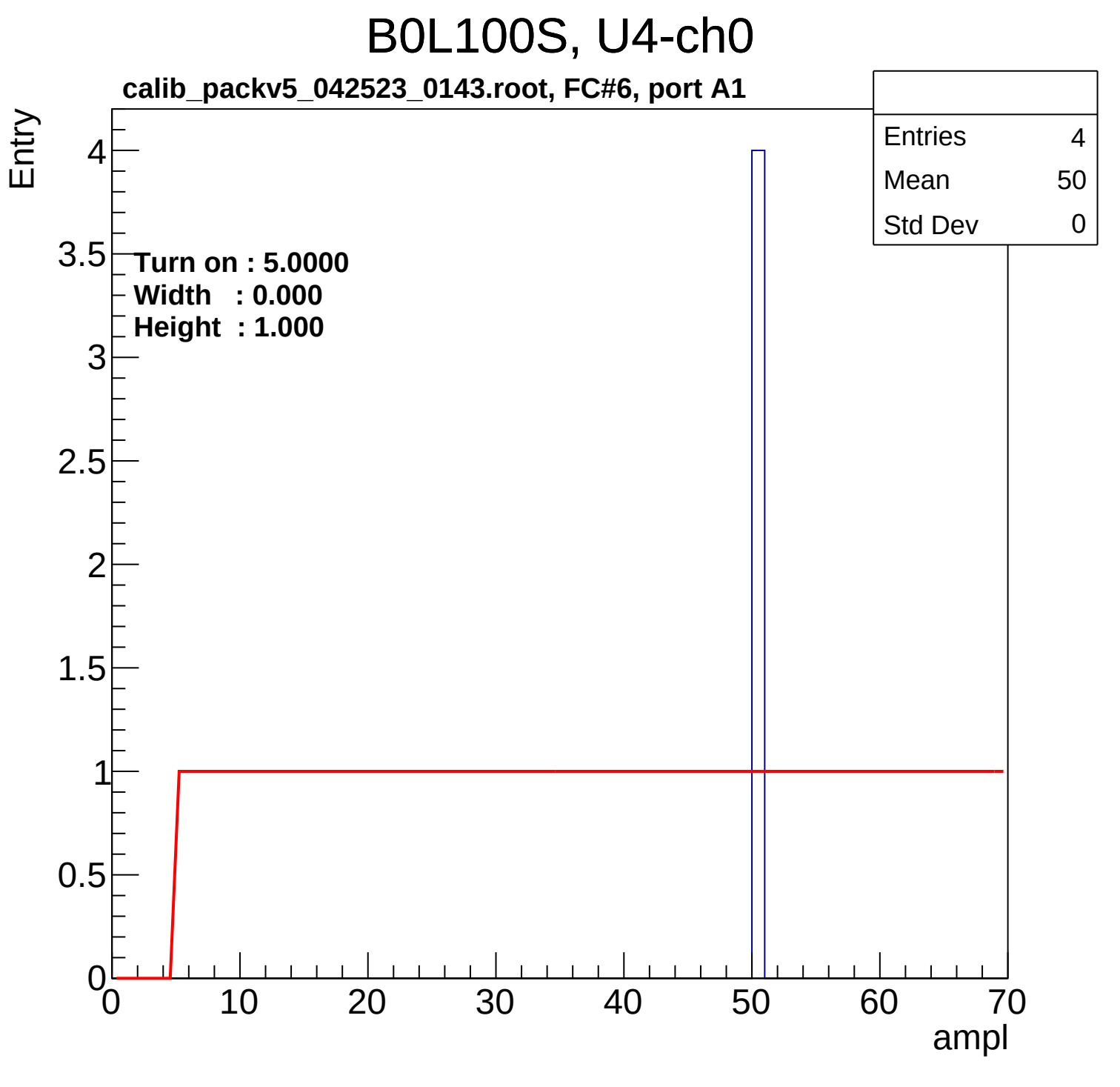
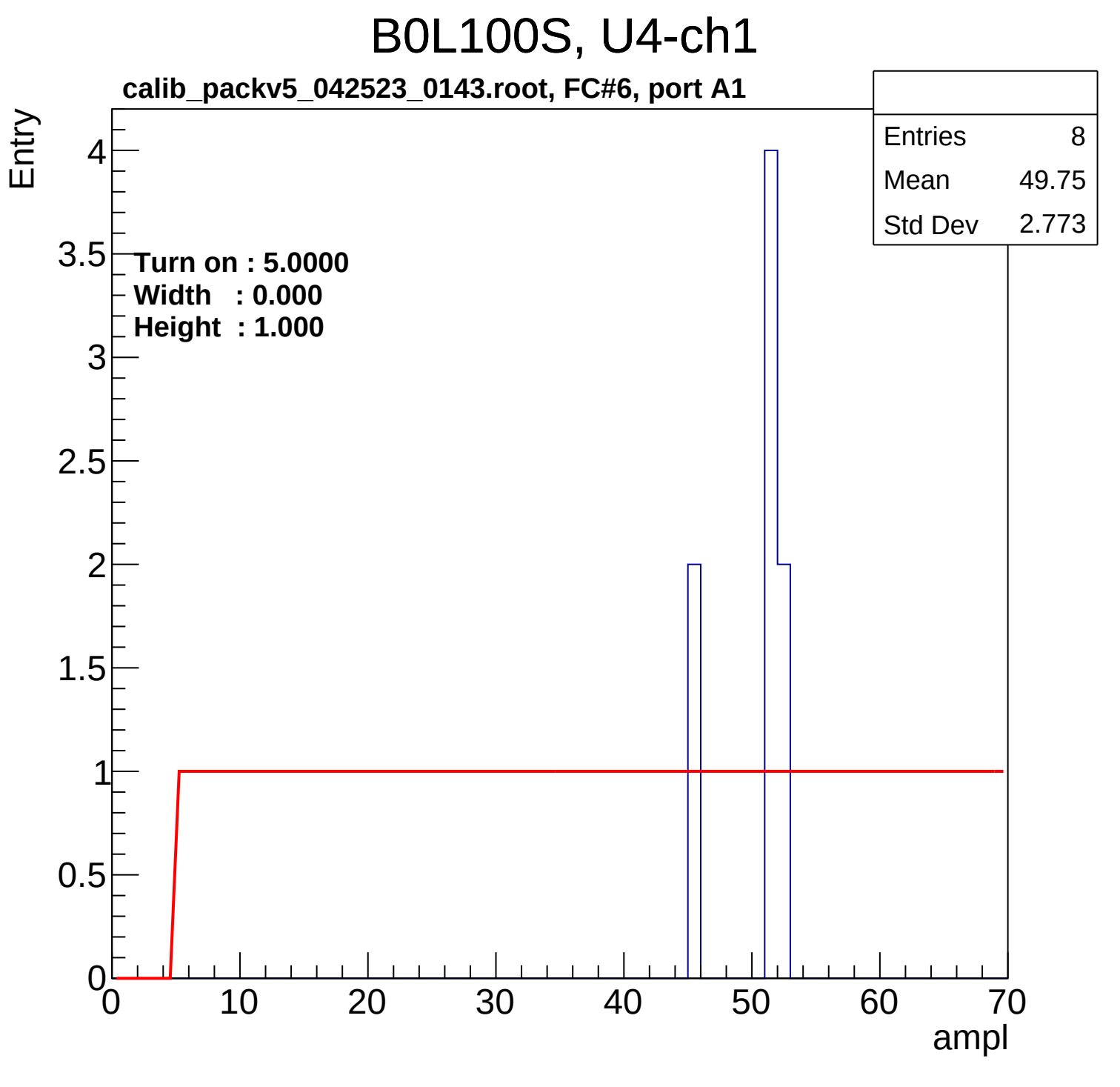
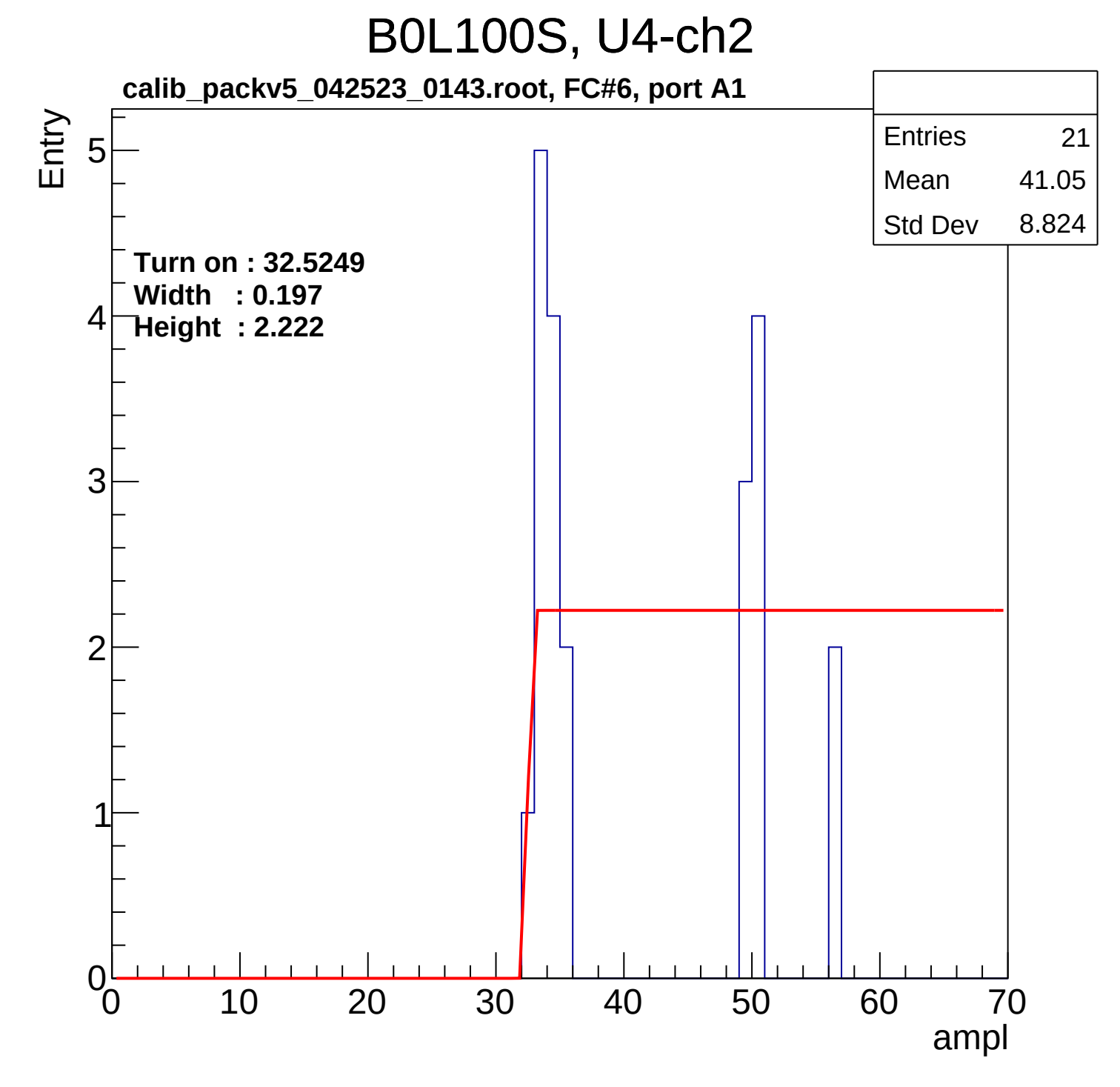
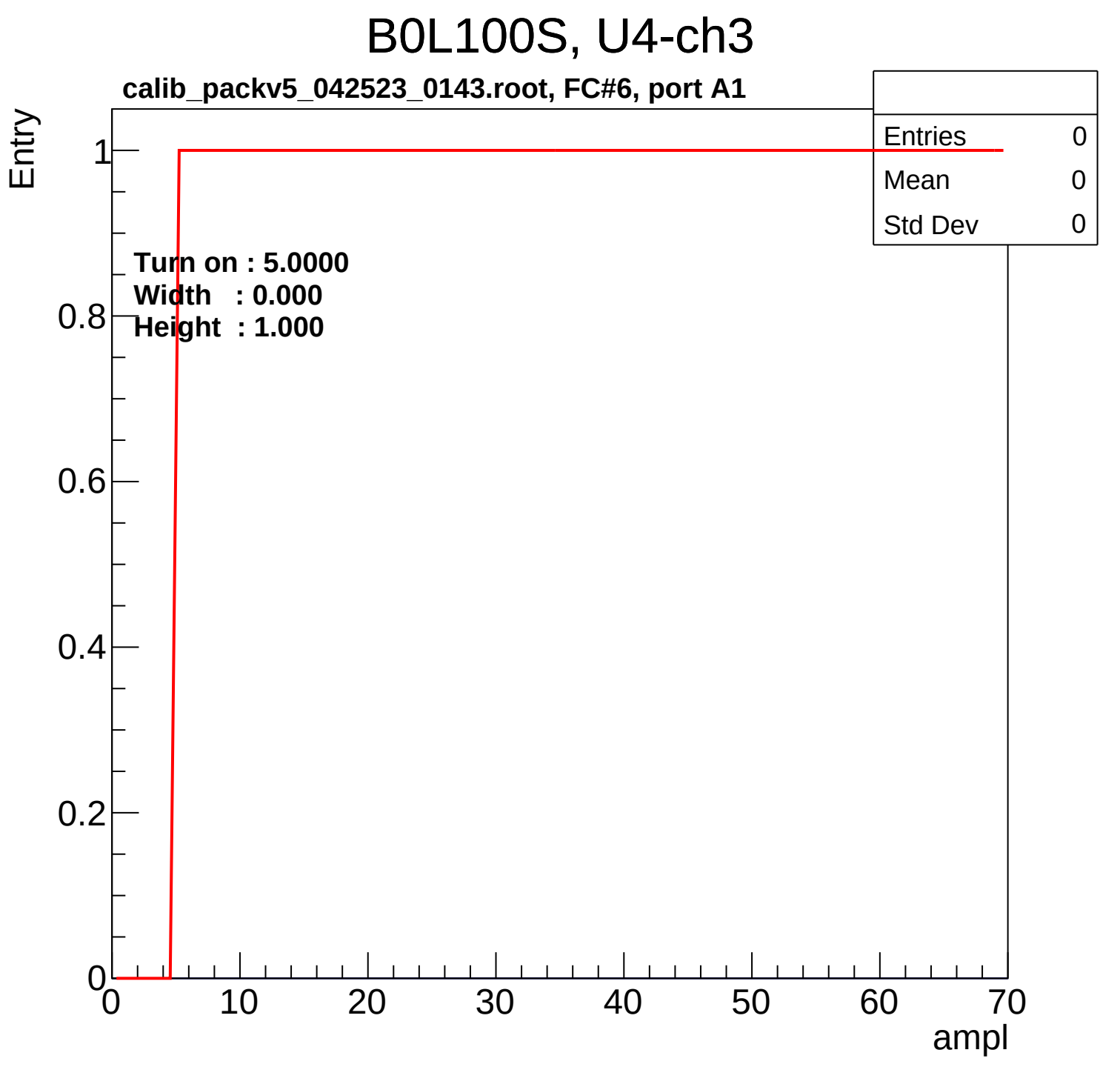
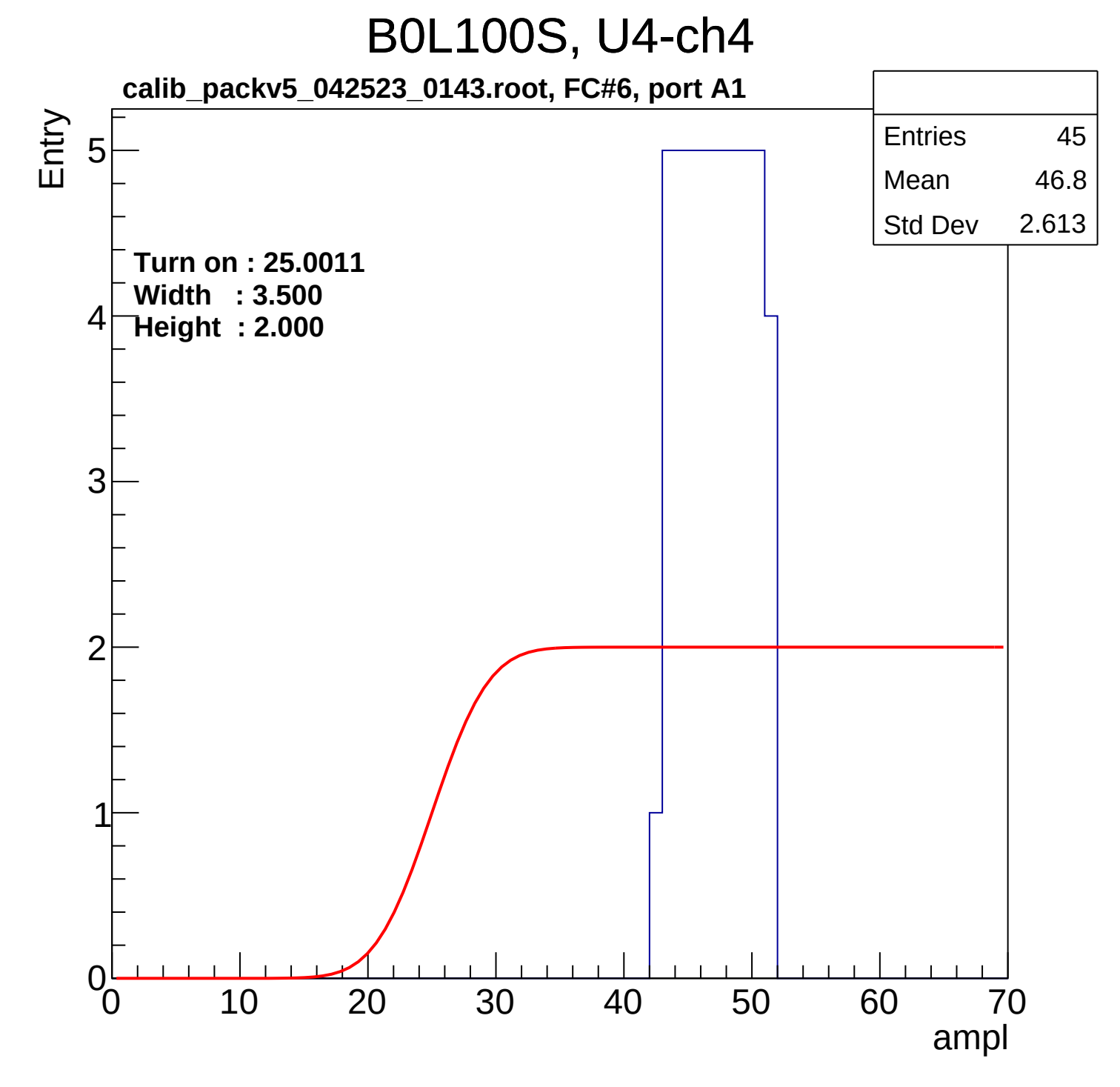
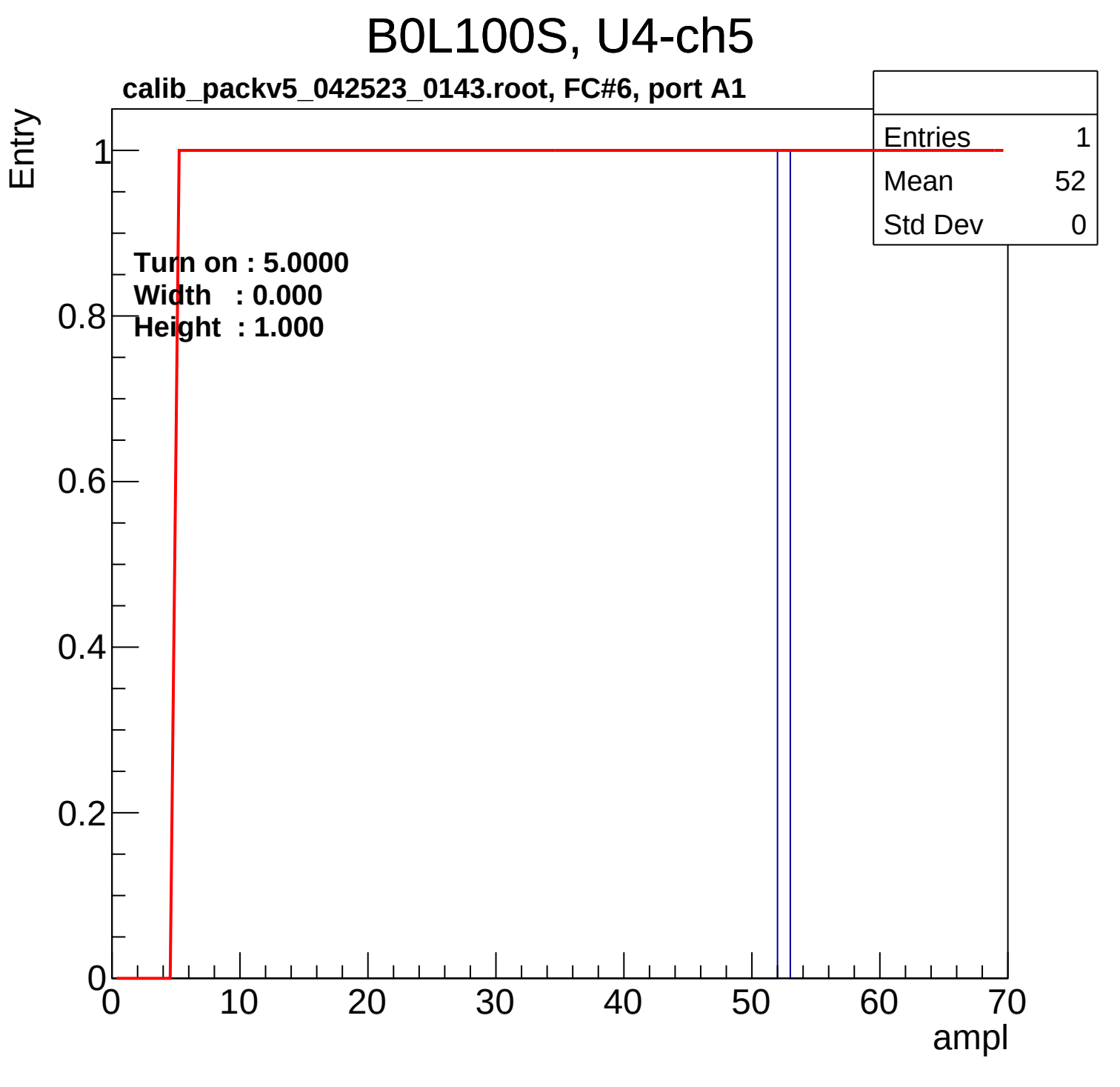

B0L100S, U4-ch0
calib_packv5_042523_0143.root, FC#6, port A1
Entries 4
Mean 50
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

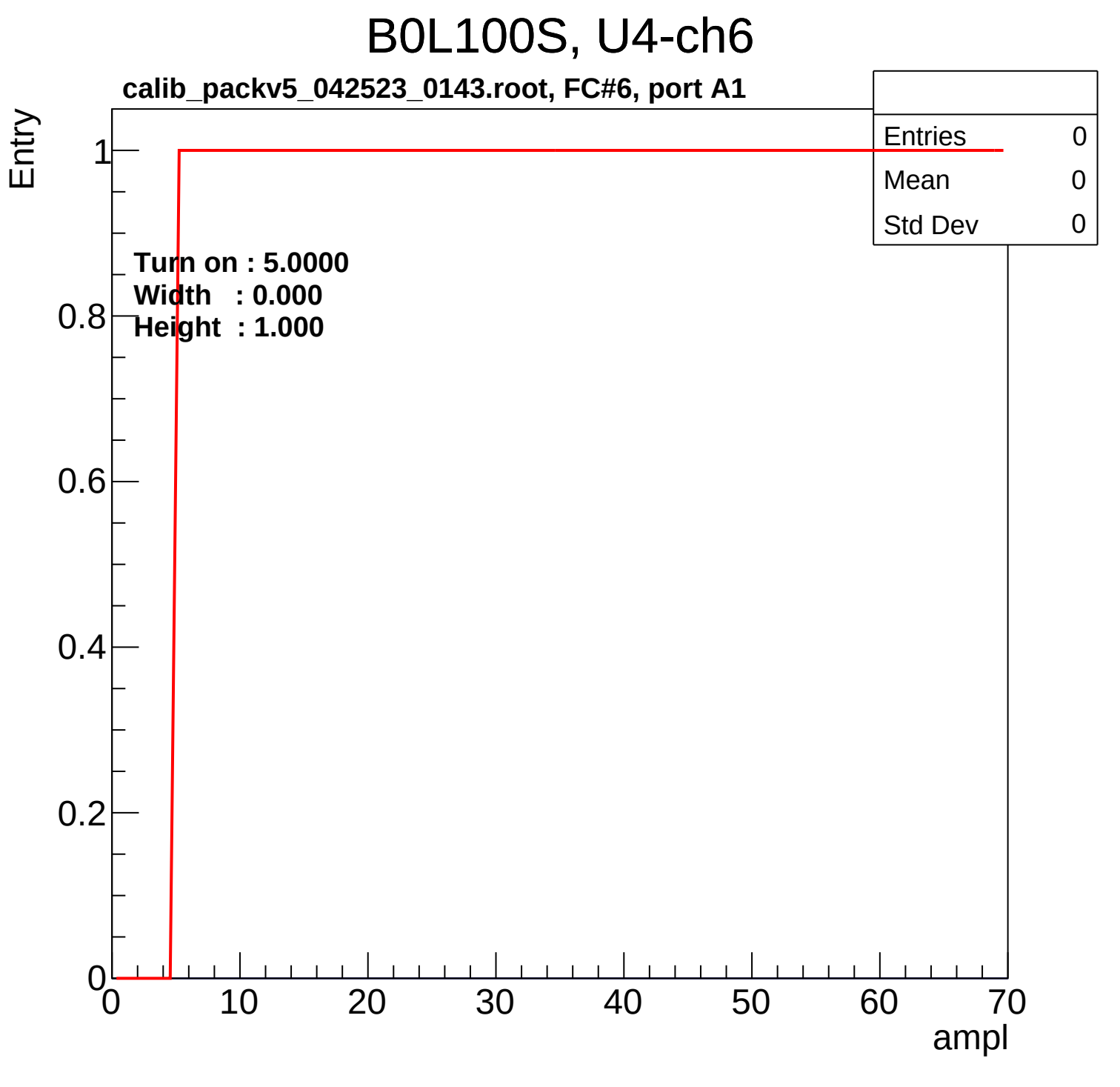

B0L100S, U4-ch1
calib_packv5_042523_0143.root, FC#6, port A1
Entries 8
Mean 49.75
Std Dev 2.773
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

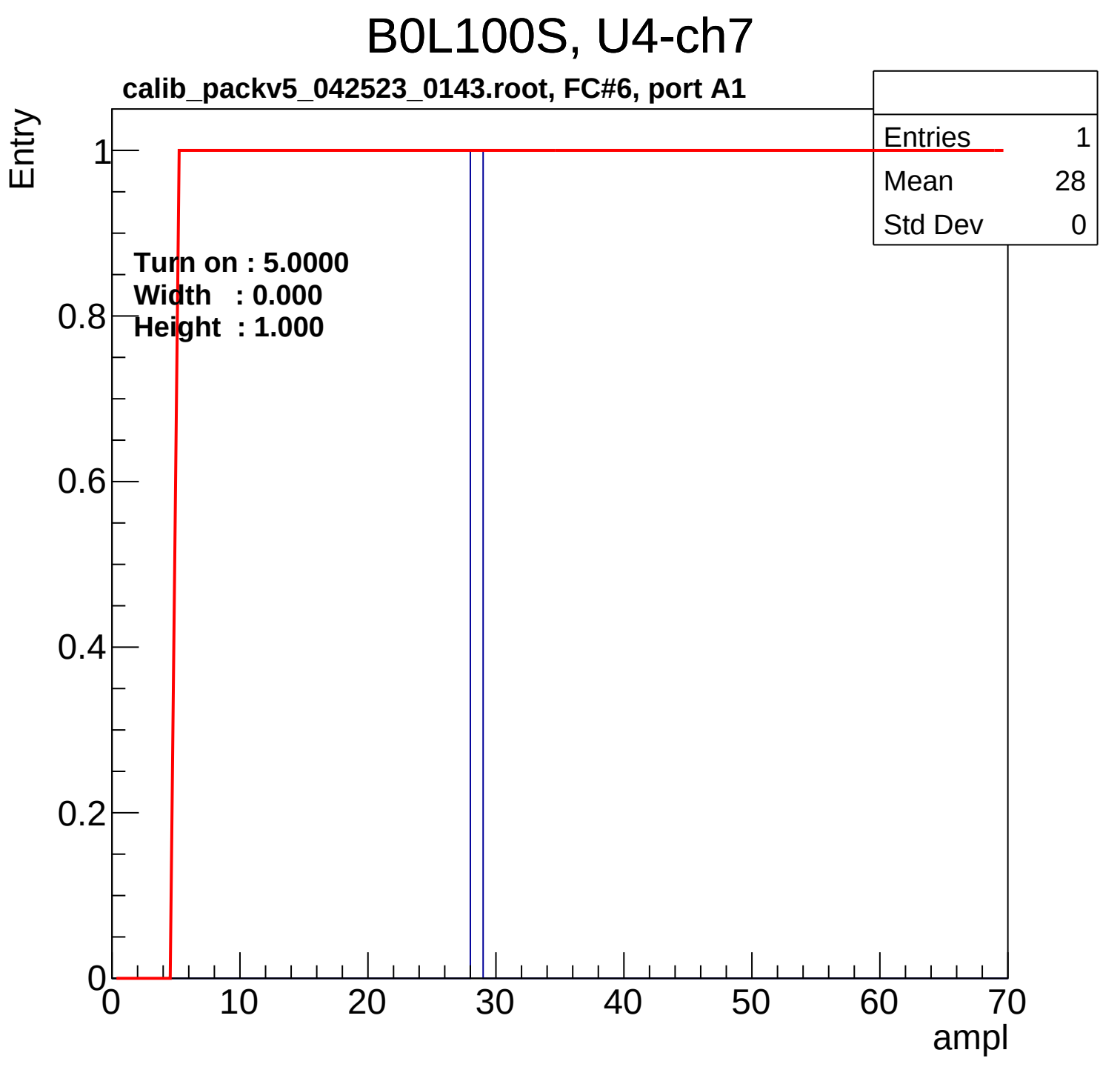

B0L100S, U4-ch2
calib_packv5_042523_0143.root, FC#6, port A1
Entries 21
Mean 41.05
Std Dev 8.824
Turn on : 32.5249
Width : 0.197
Height : 2.222
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

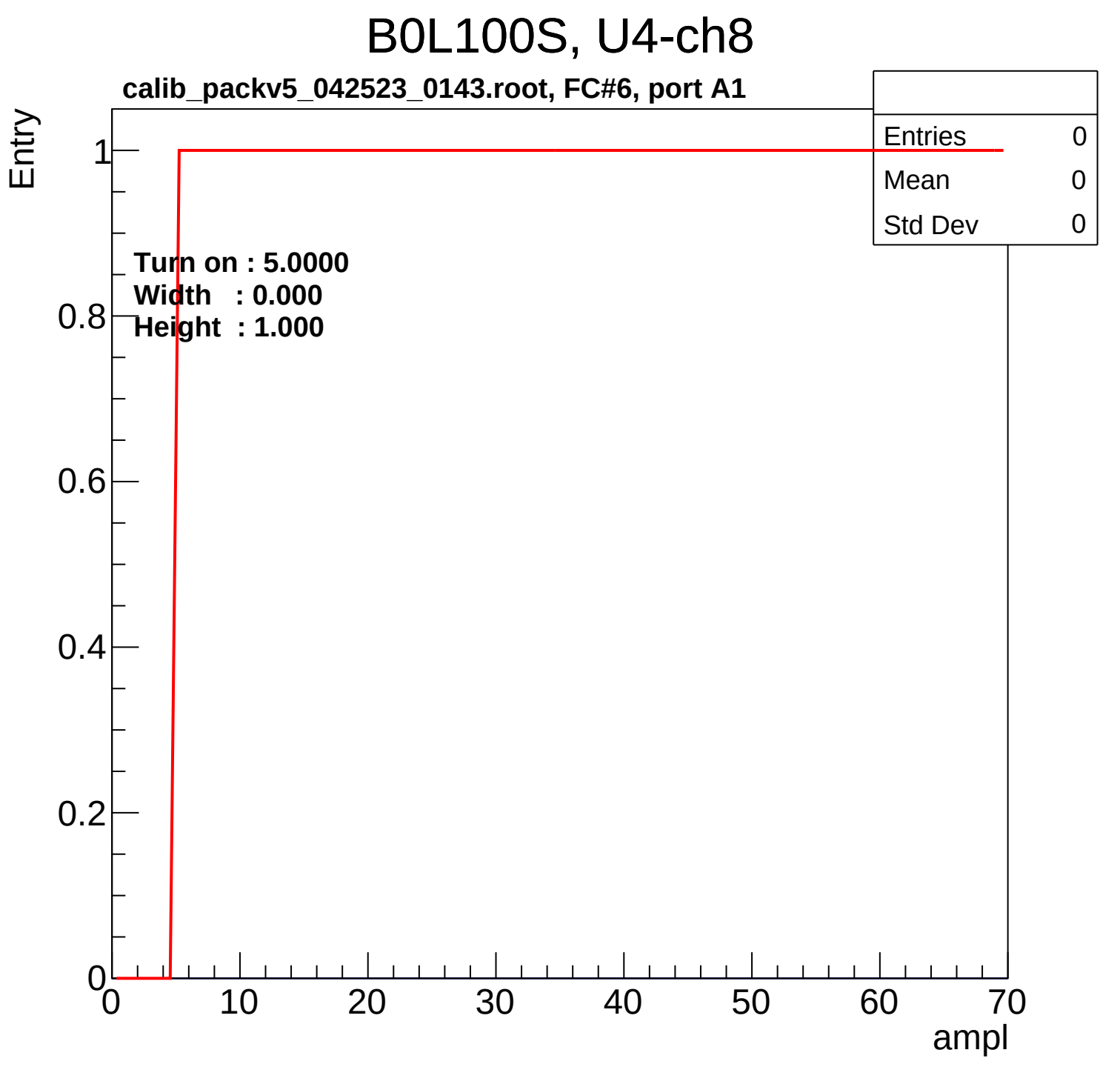

B0L100S, U4-ch3
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

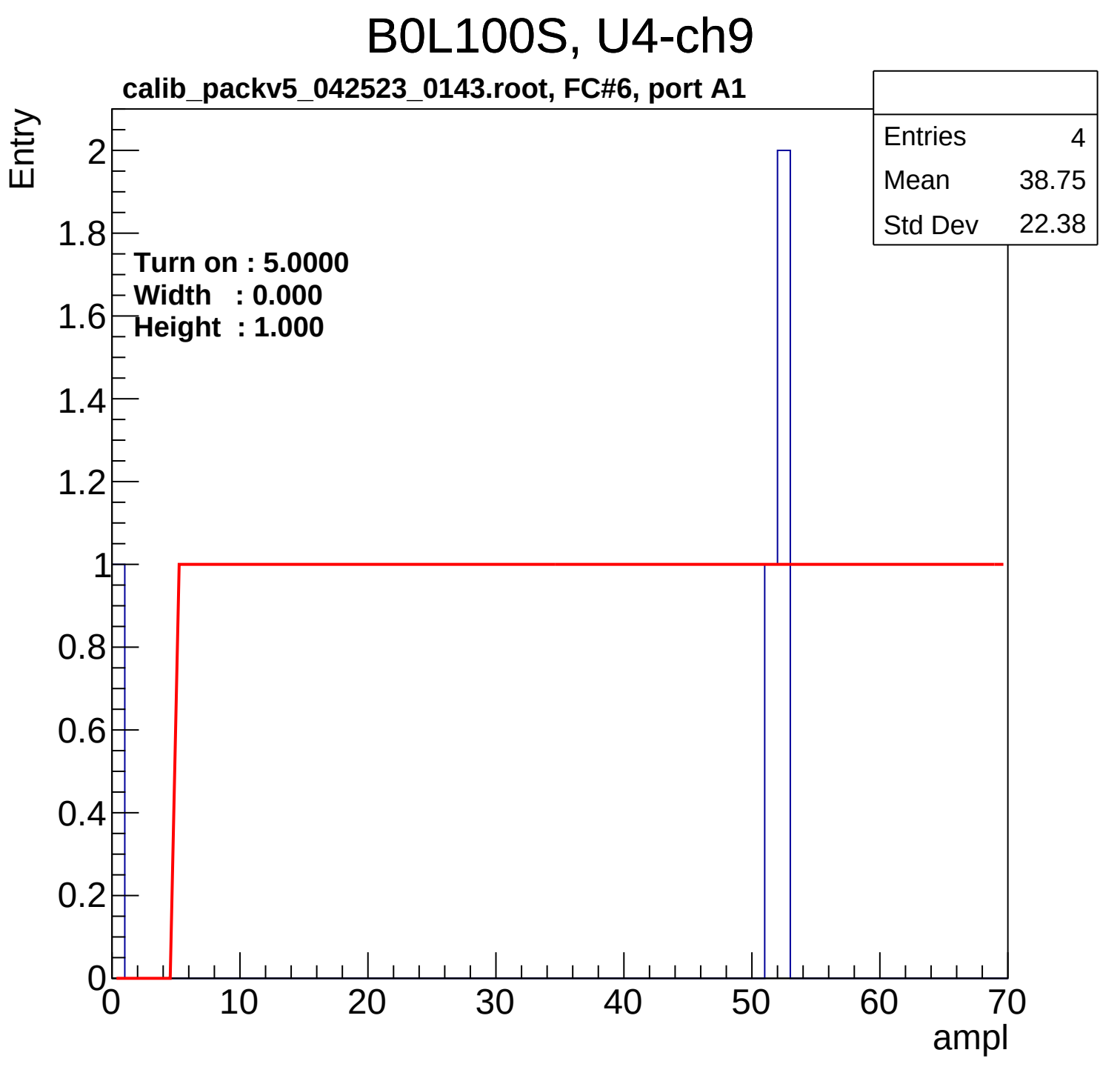

B0L100S, U4-ch4
calib_packv5_042523_0143.root, FC#6, port A1
Entries 45
Mean 46.8
Std Dev 2.613
Turn on : 25.0011
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

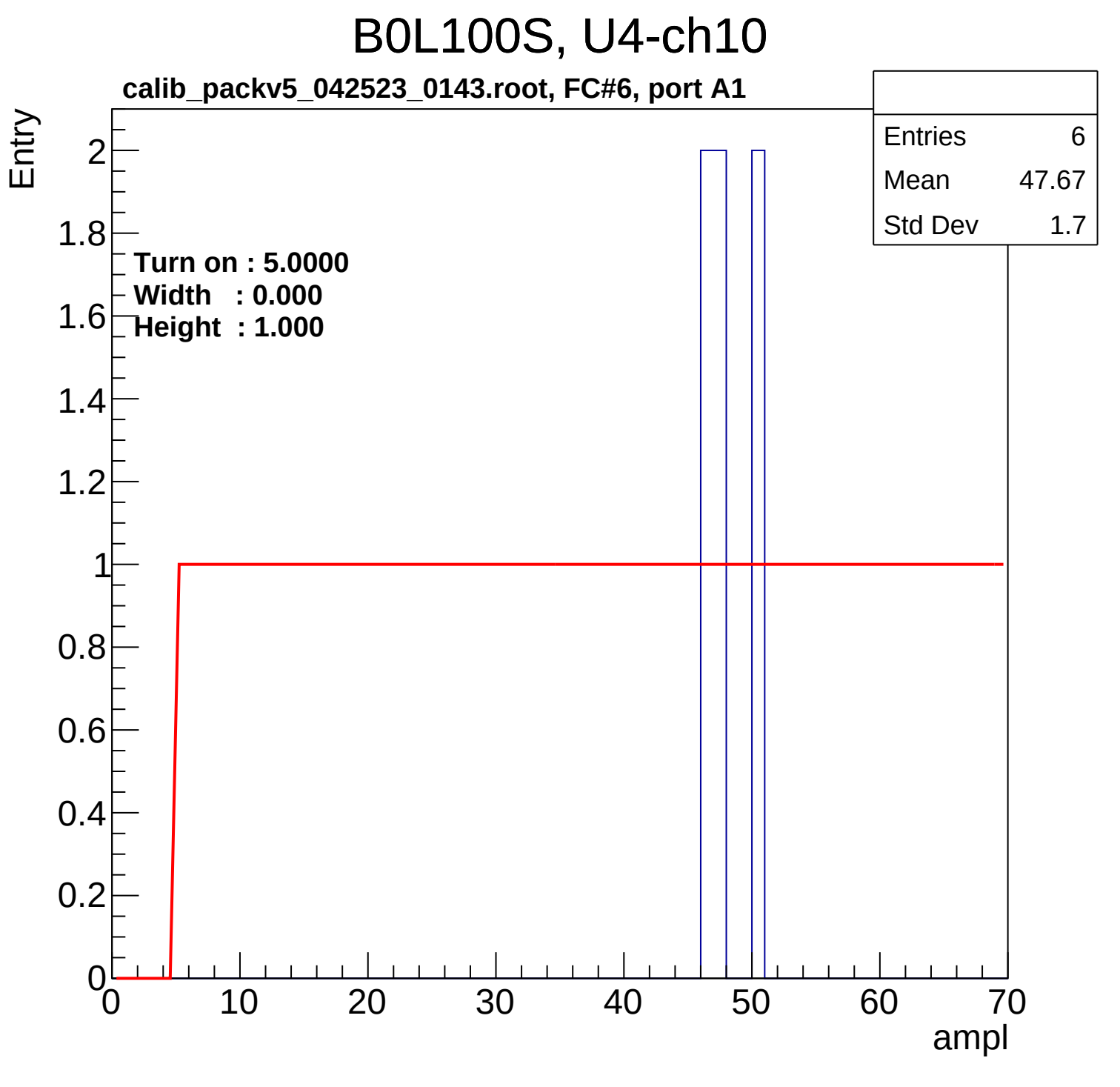

B0L100S, U4-ch5
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 52
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

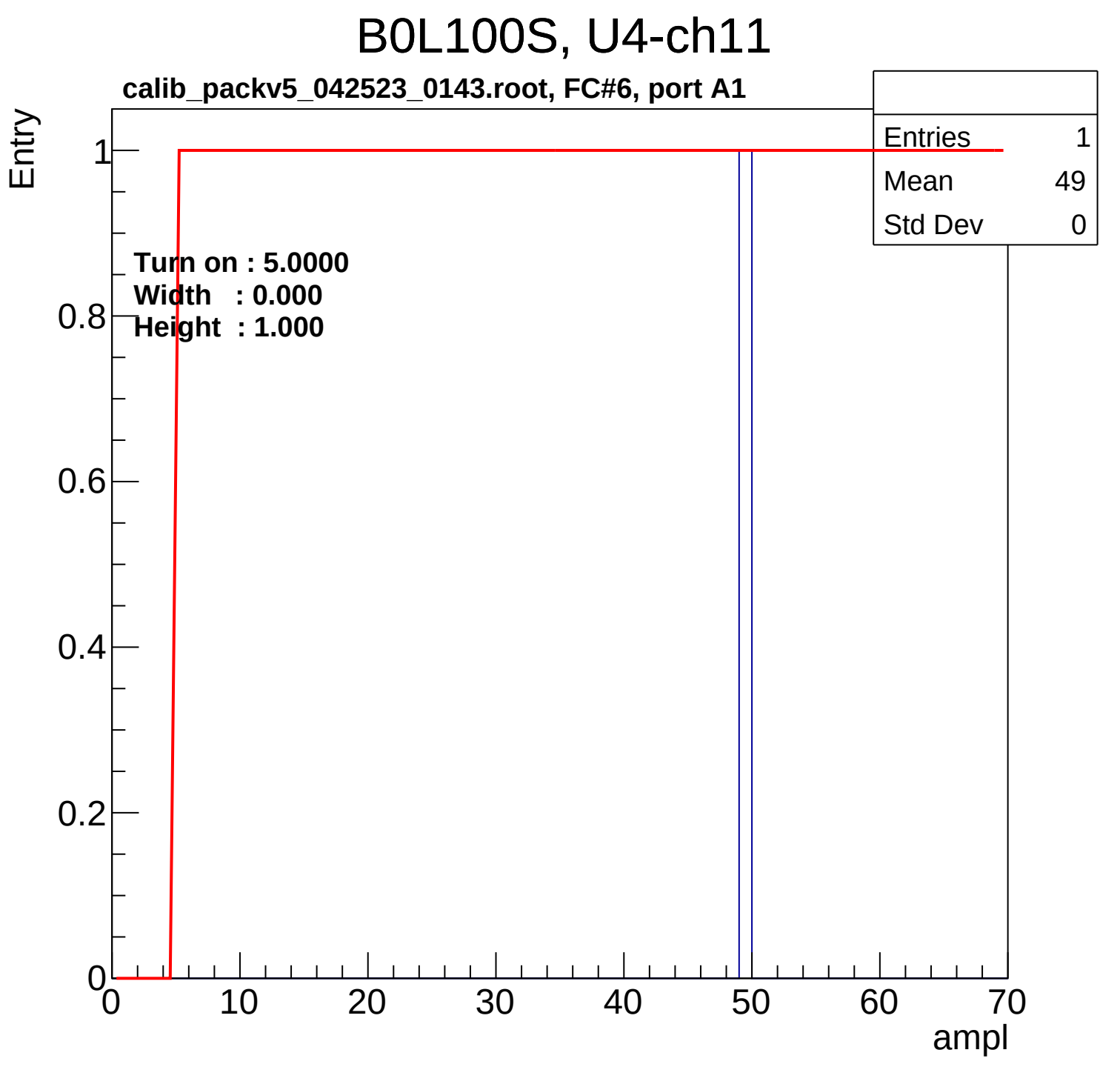

B0L100S, U4-ch6
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

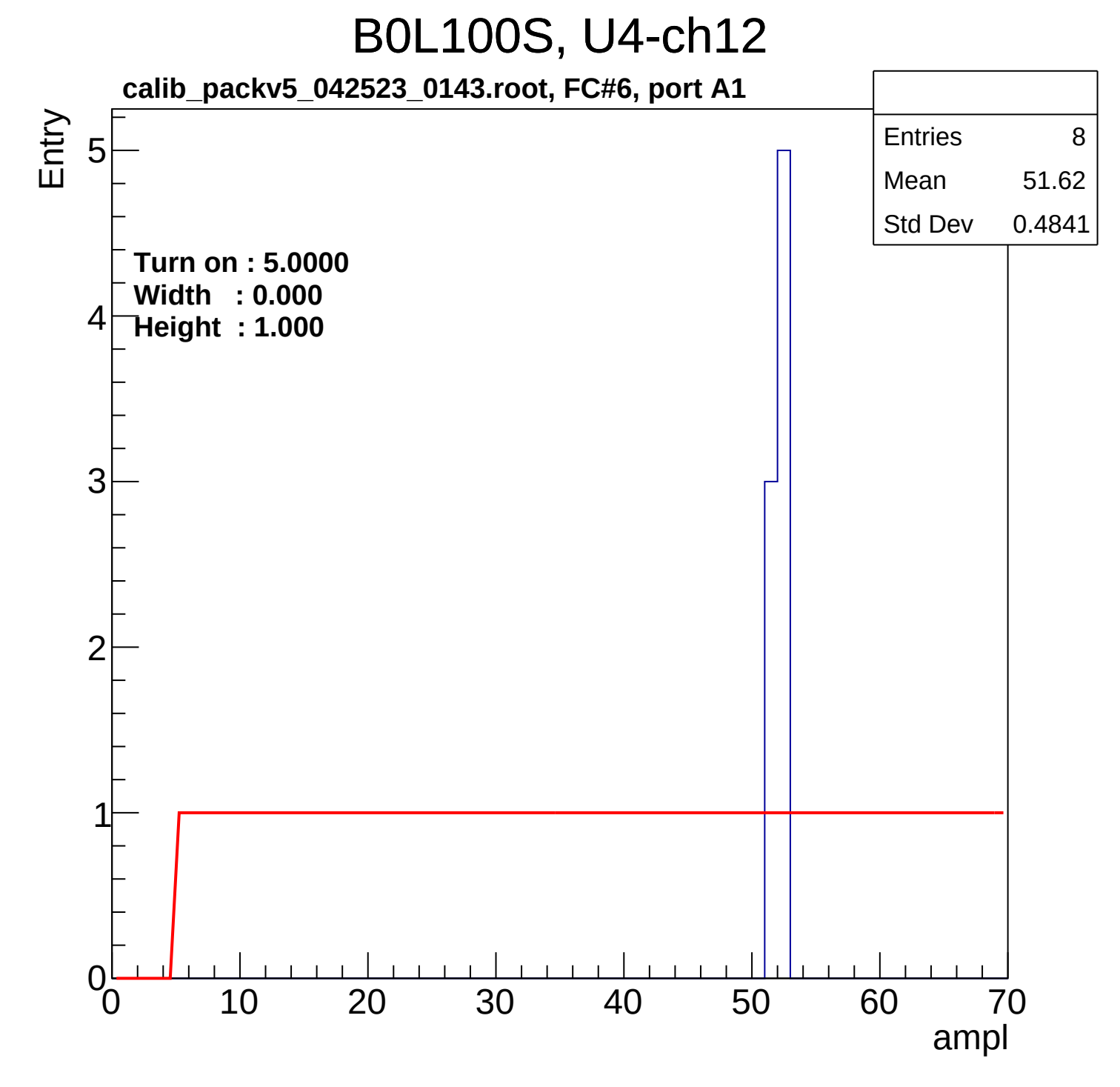

B0L100S, U4-ch7
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 28
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

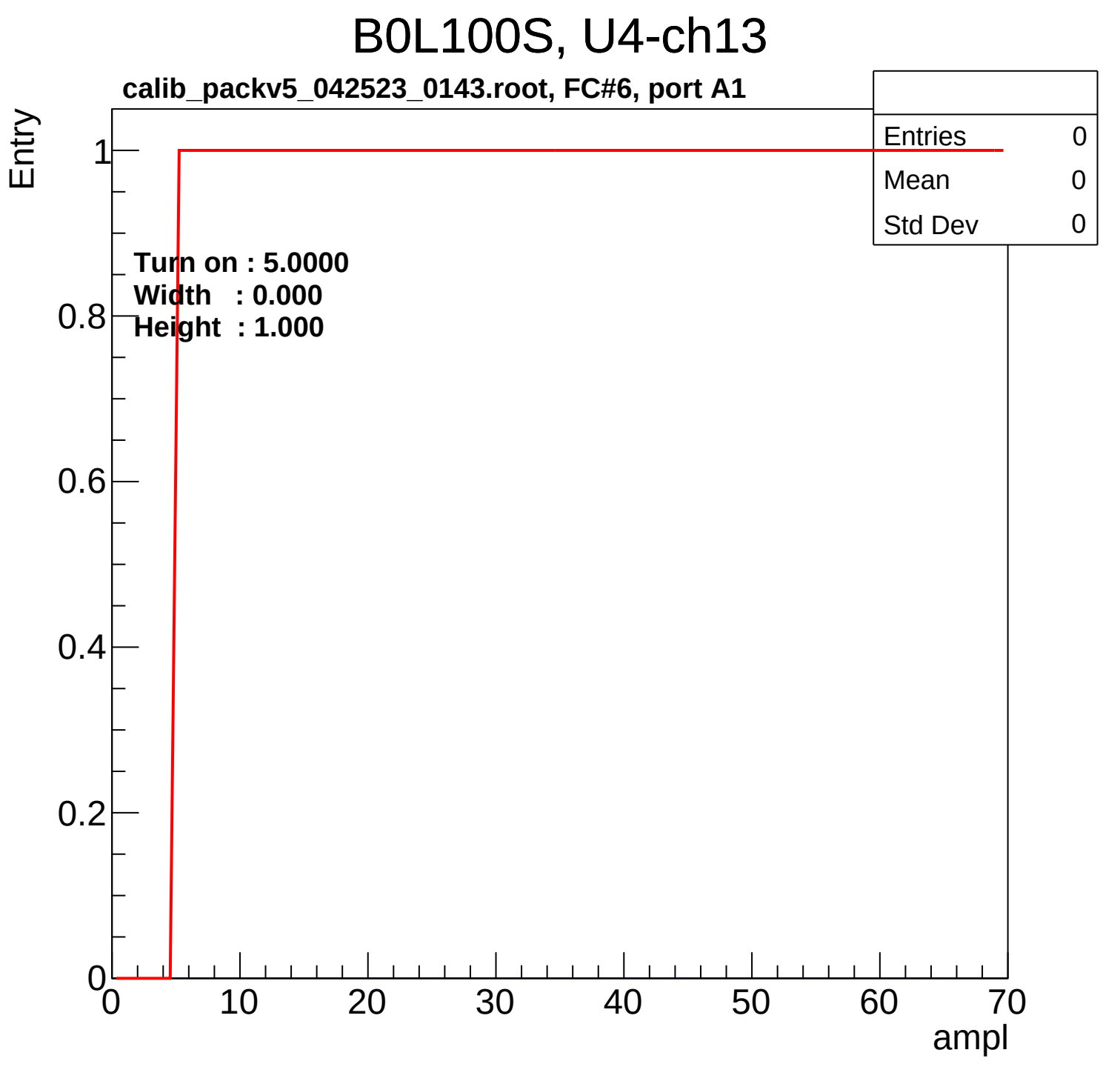

B0L100S, U4-ch8
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

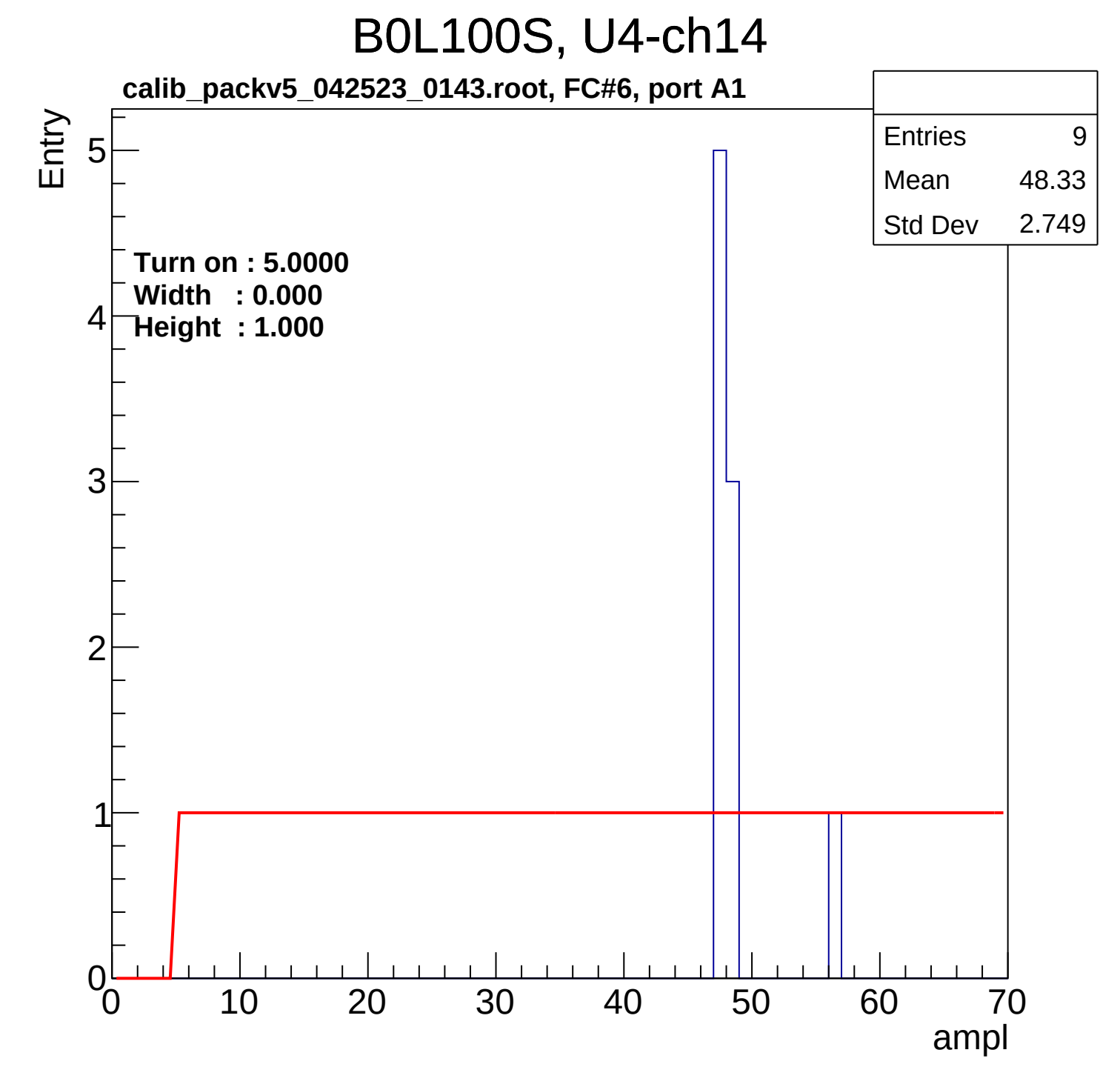

B0L100S, U4-ch9
calib_packv5_042523_0143.root, FC#6, port A1
Entries 4
Mean 38.75
Std Dev 22.38
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

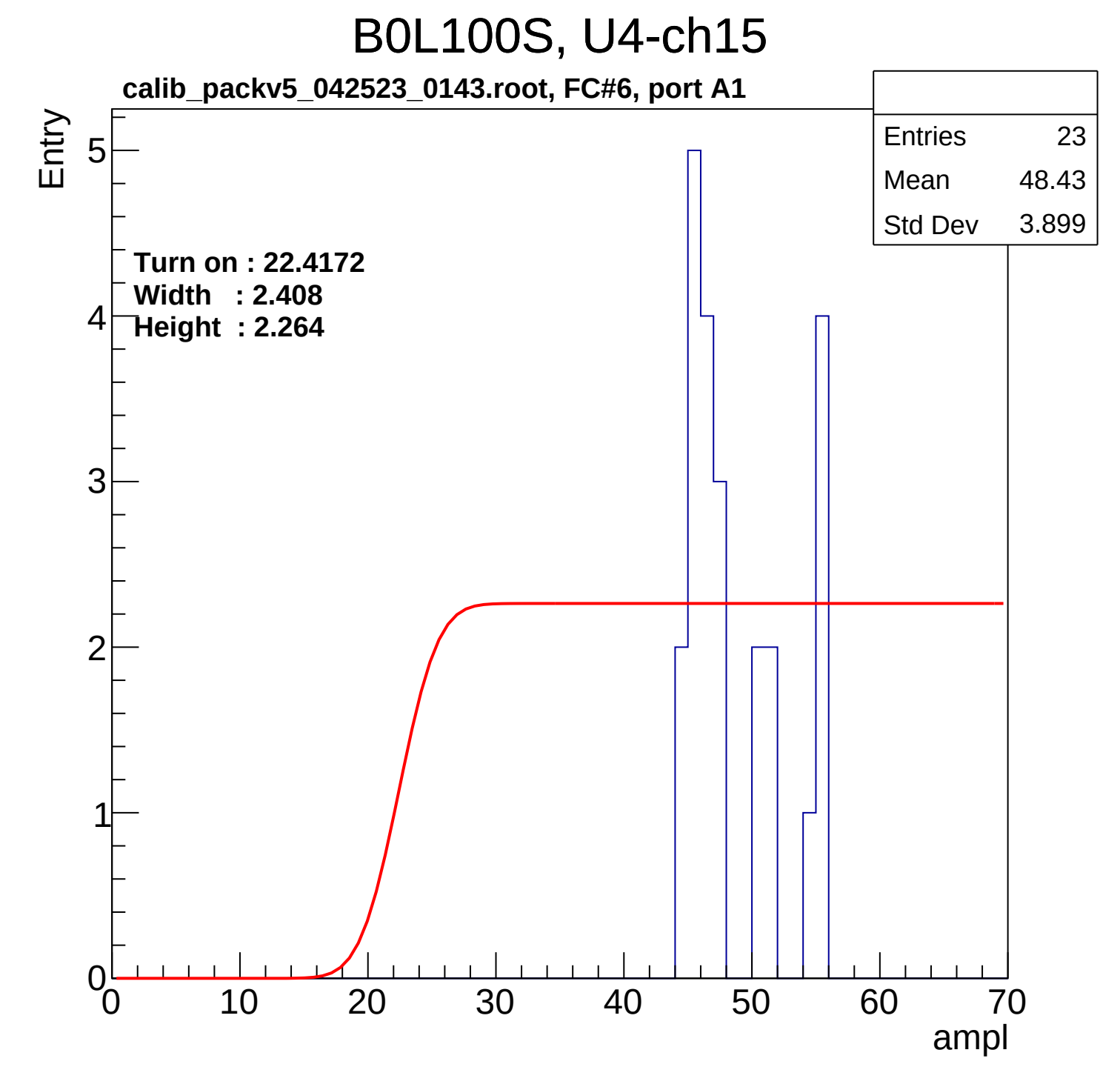

B0L100S, U4-ch10
calib_packv5_042523_0143.root, FC#6, port A1
Entries 6
Mean 47.67
Std Dev 1.7
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

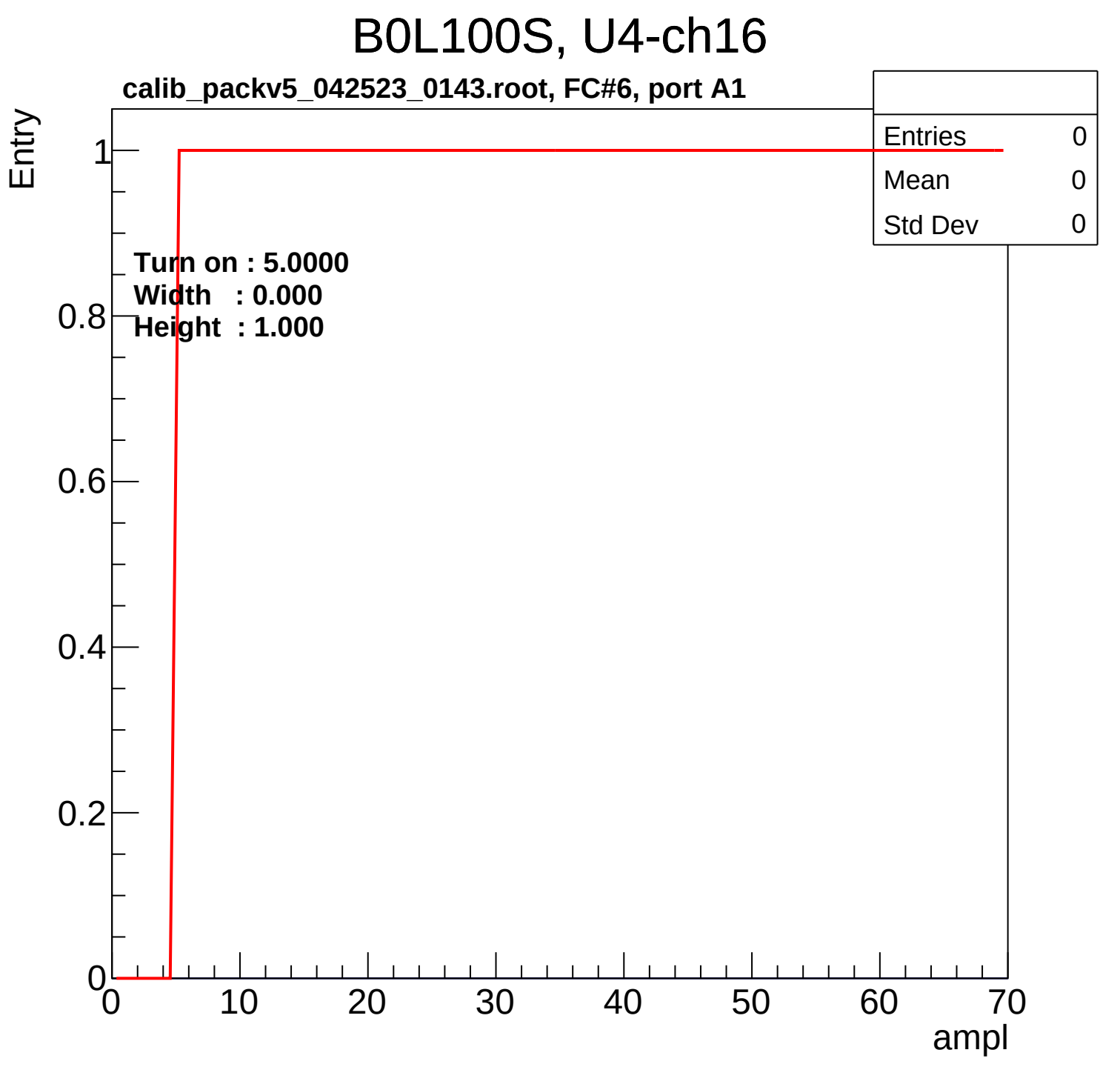

B0L100S, U4-ch11
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 49
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

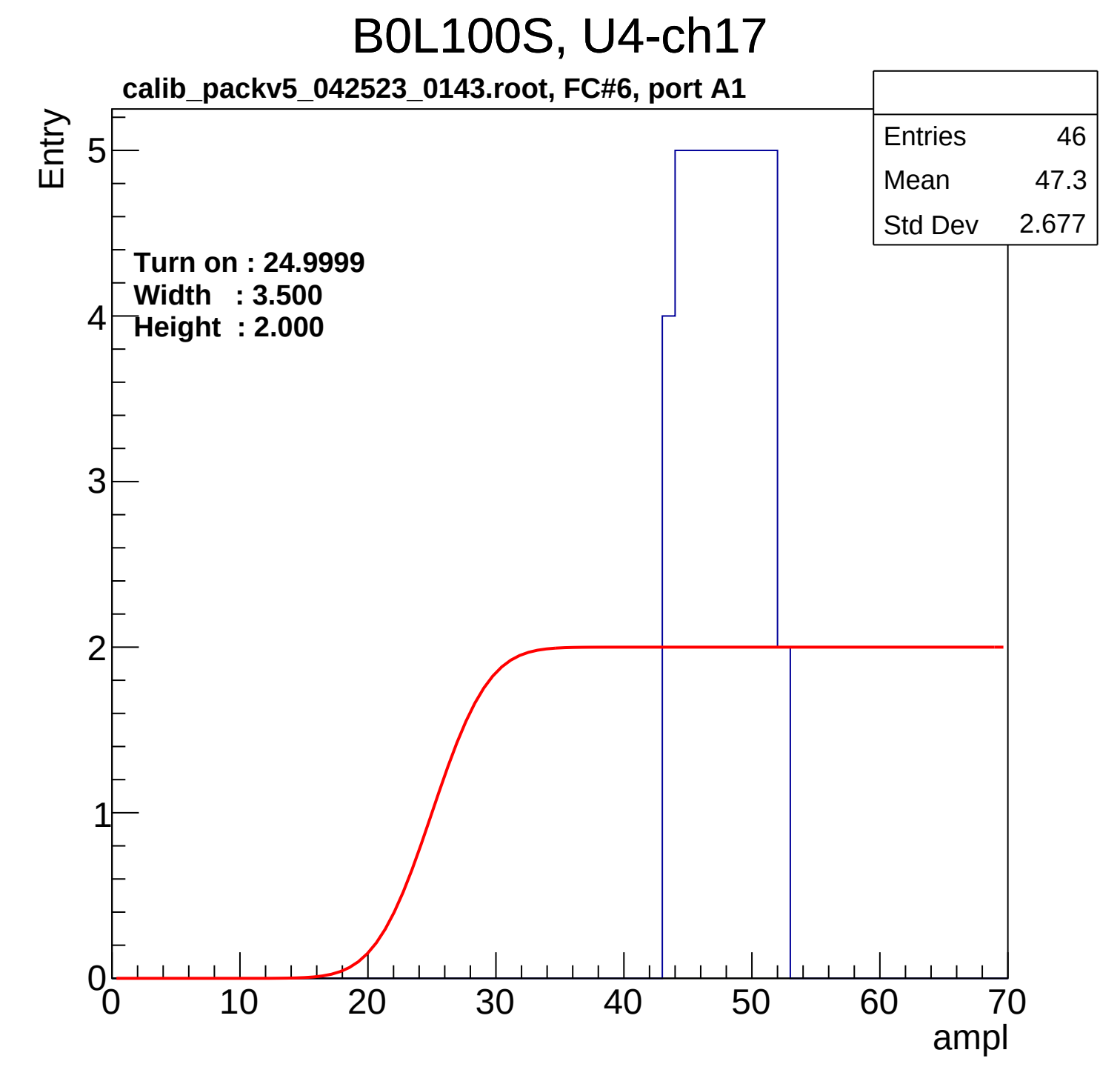

B0L100S, U4-ch12
calib_packv5_042523_0143.root, FC#6, port A1
Entries 8
Mean 51.62
Std Dev 0.4841
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

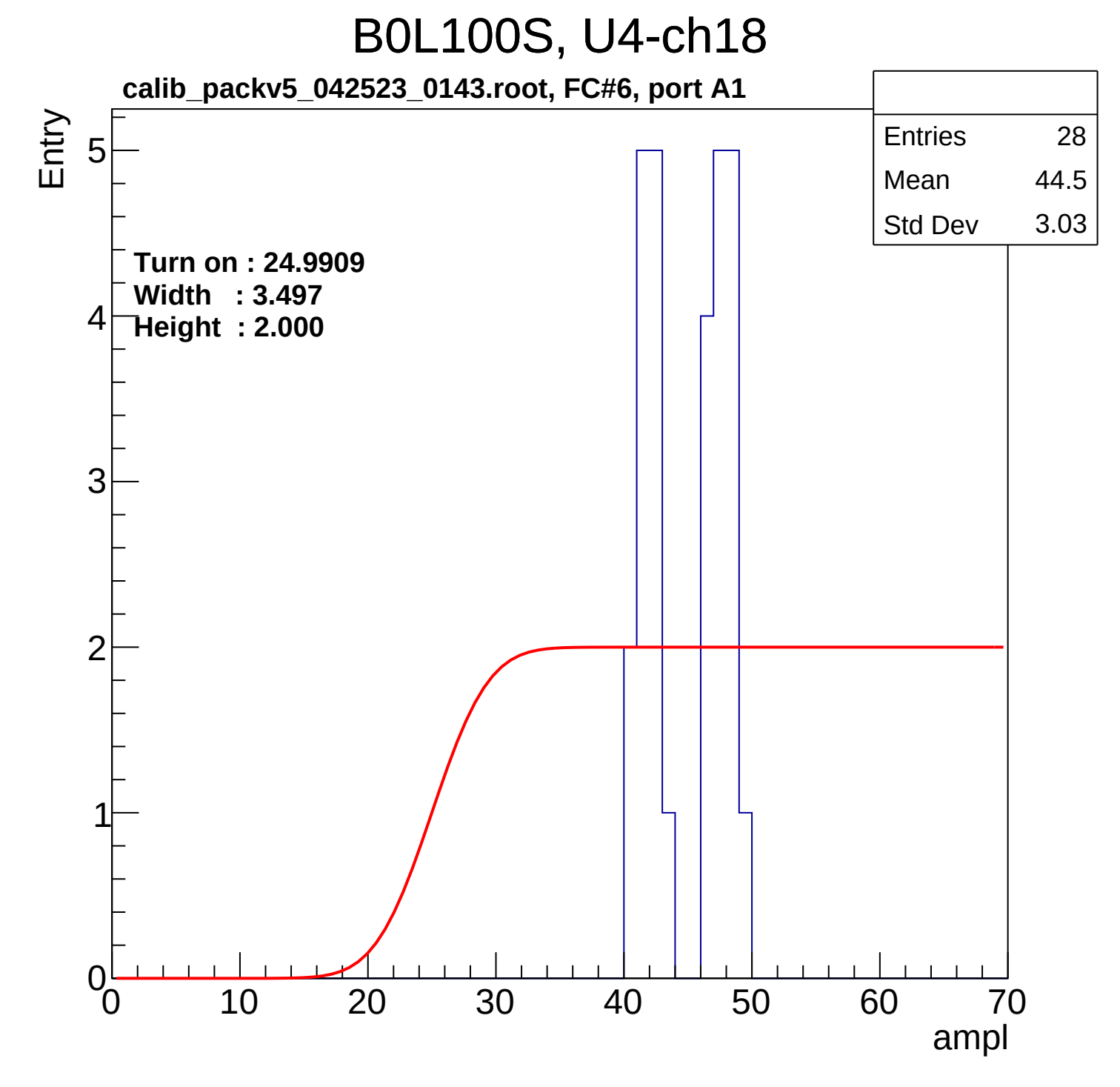

B0L100S, U4-ch13
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

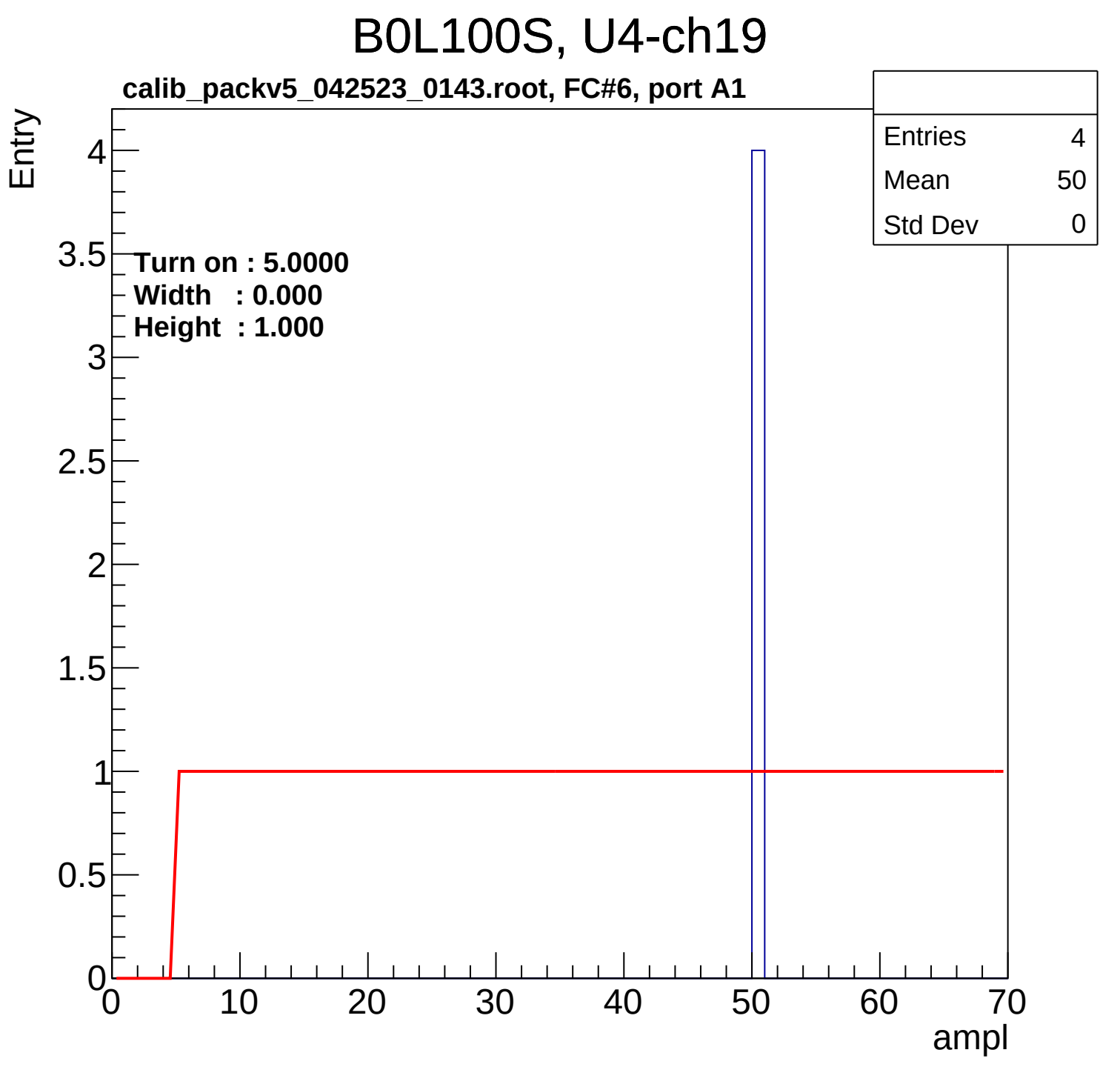

B0L100S, U4-ch14
calib_packv5_042523_0143.root, FC#6, port A1
Entries 9
Mean 48.33
Std Dev 2.749
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

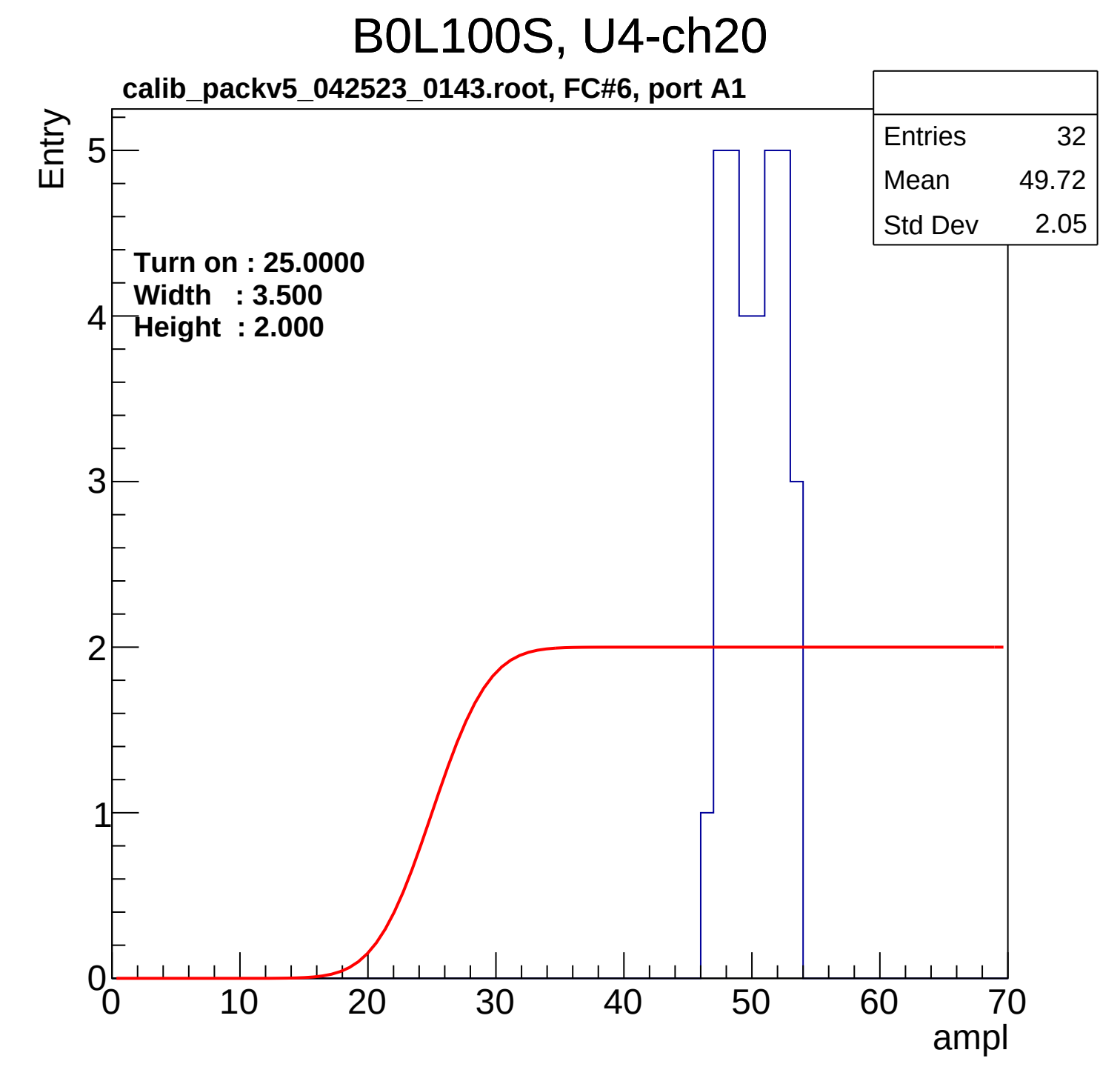

B0L100S, U4-ch15
calib_packv5_042523_0143.root, FC#6, port A1
Entries 23
Mean 48.43
Std Dev 3.899
Turn on : 22.4172
Width : 2.408
Height : 2.264
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

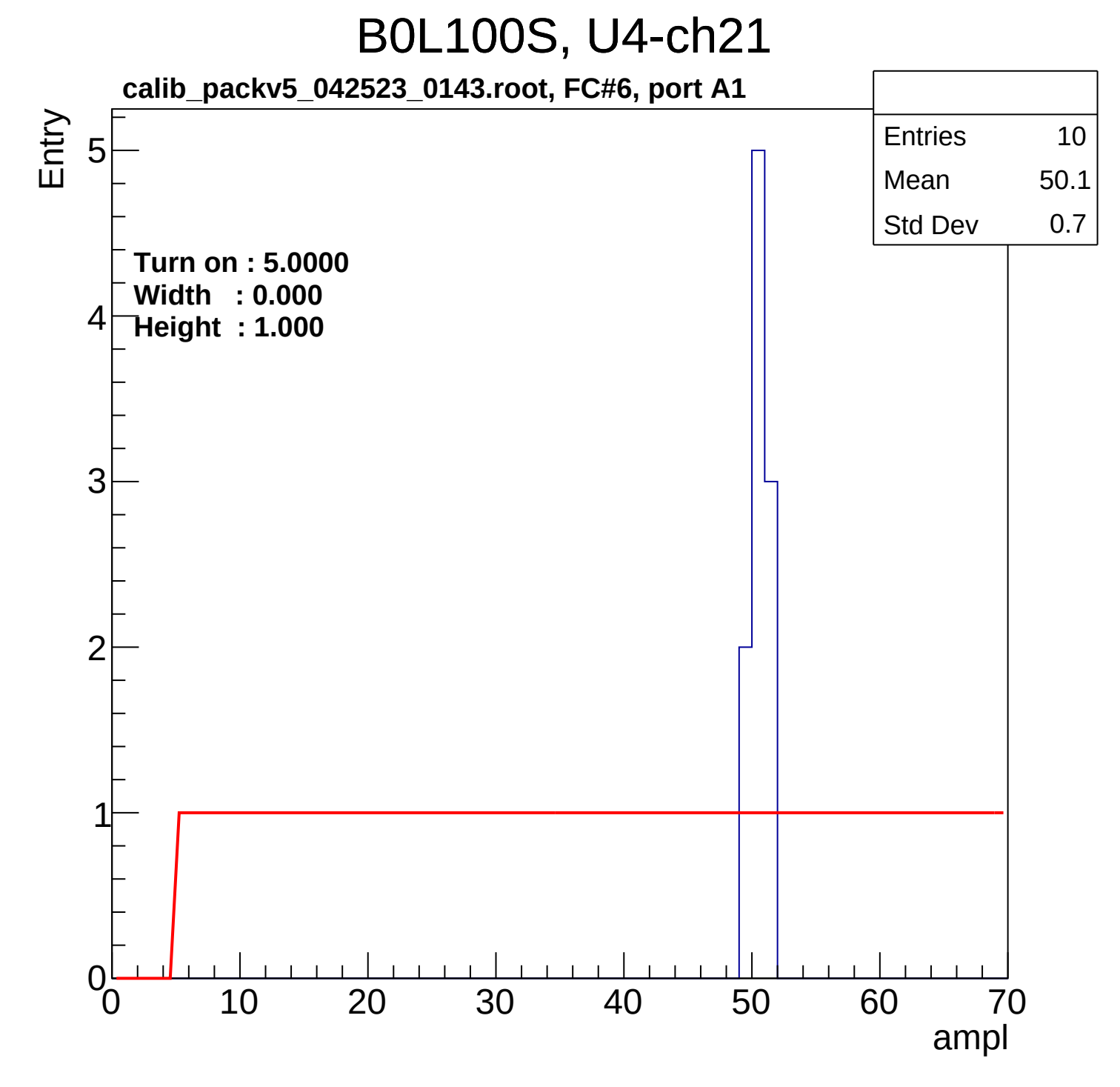

B0L100S, U4-ch16
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

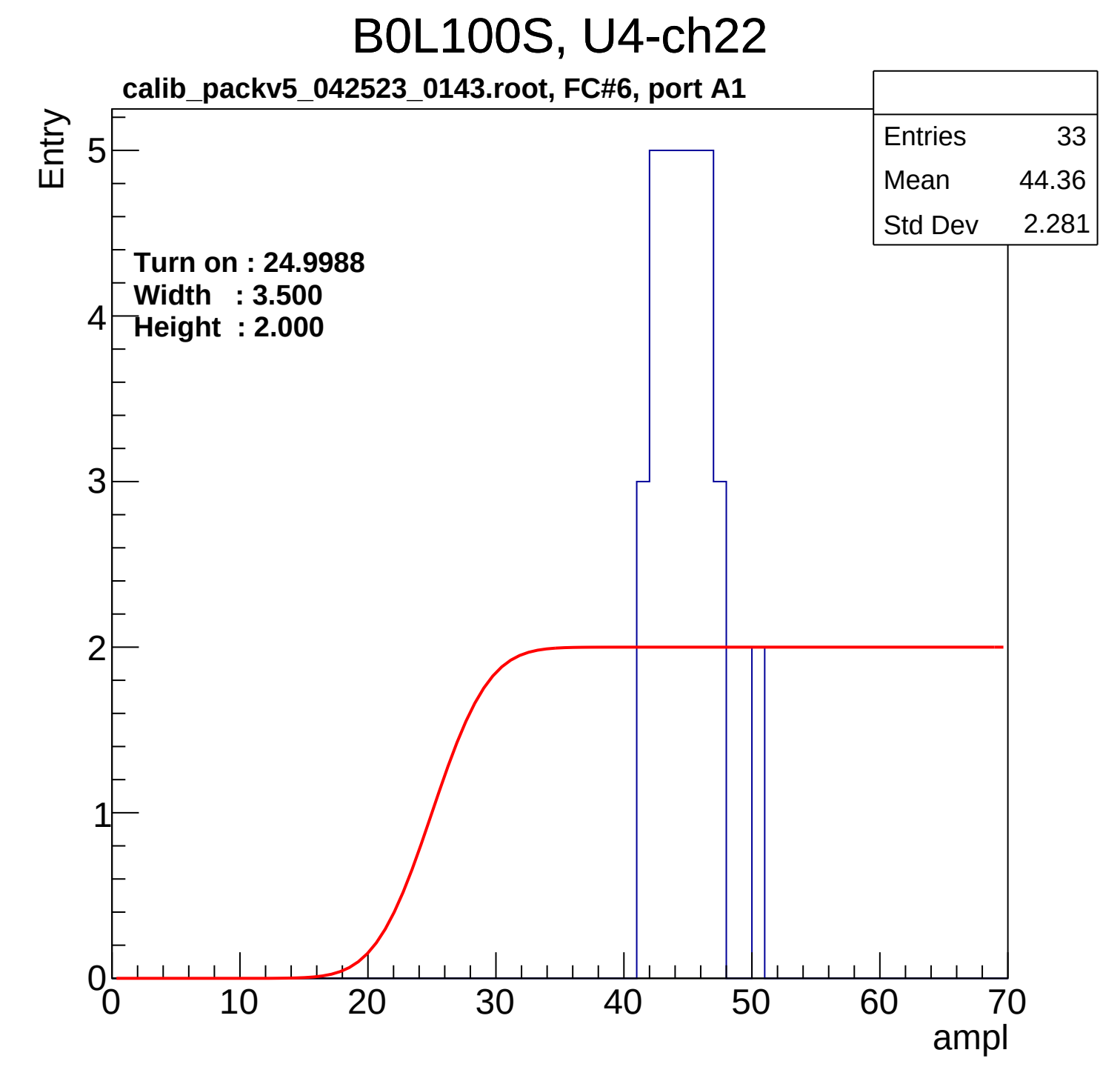

B0L100S, U4-ch17
calib_packv5_042523_0143.root, FC#6, port A1
Entries 46
Mean 47.3
Std Dev 2.677
Turn on : 24.9999
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

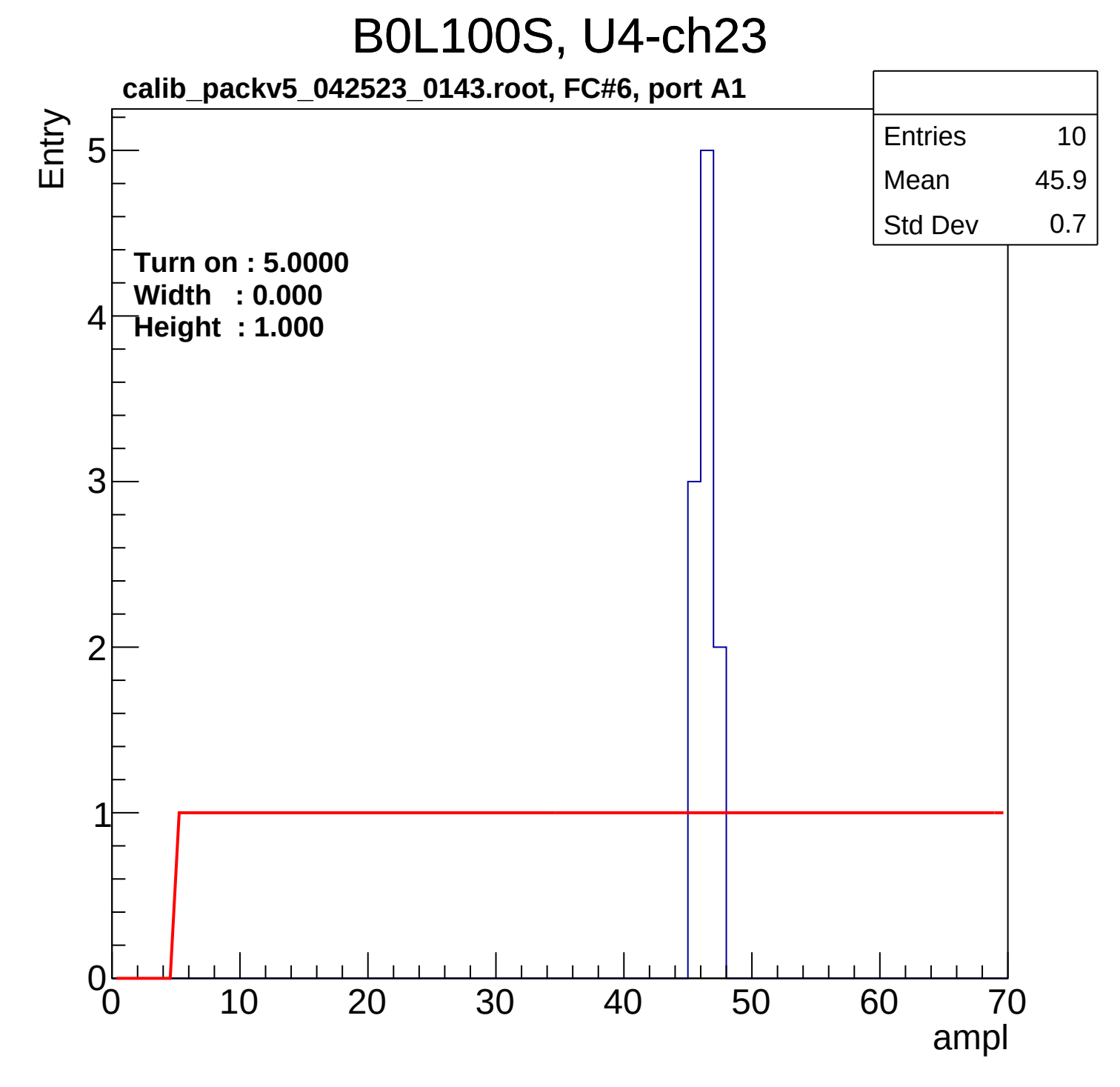

B0L100S, U4-ch18
calib_packv5_042523_0143.root, FC#6, port A1
Entries 28
Mean 44.5
Std Dev 3.03
Turn on : 24.9909
Width : 3.497
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

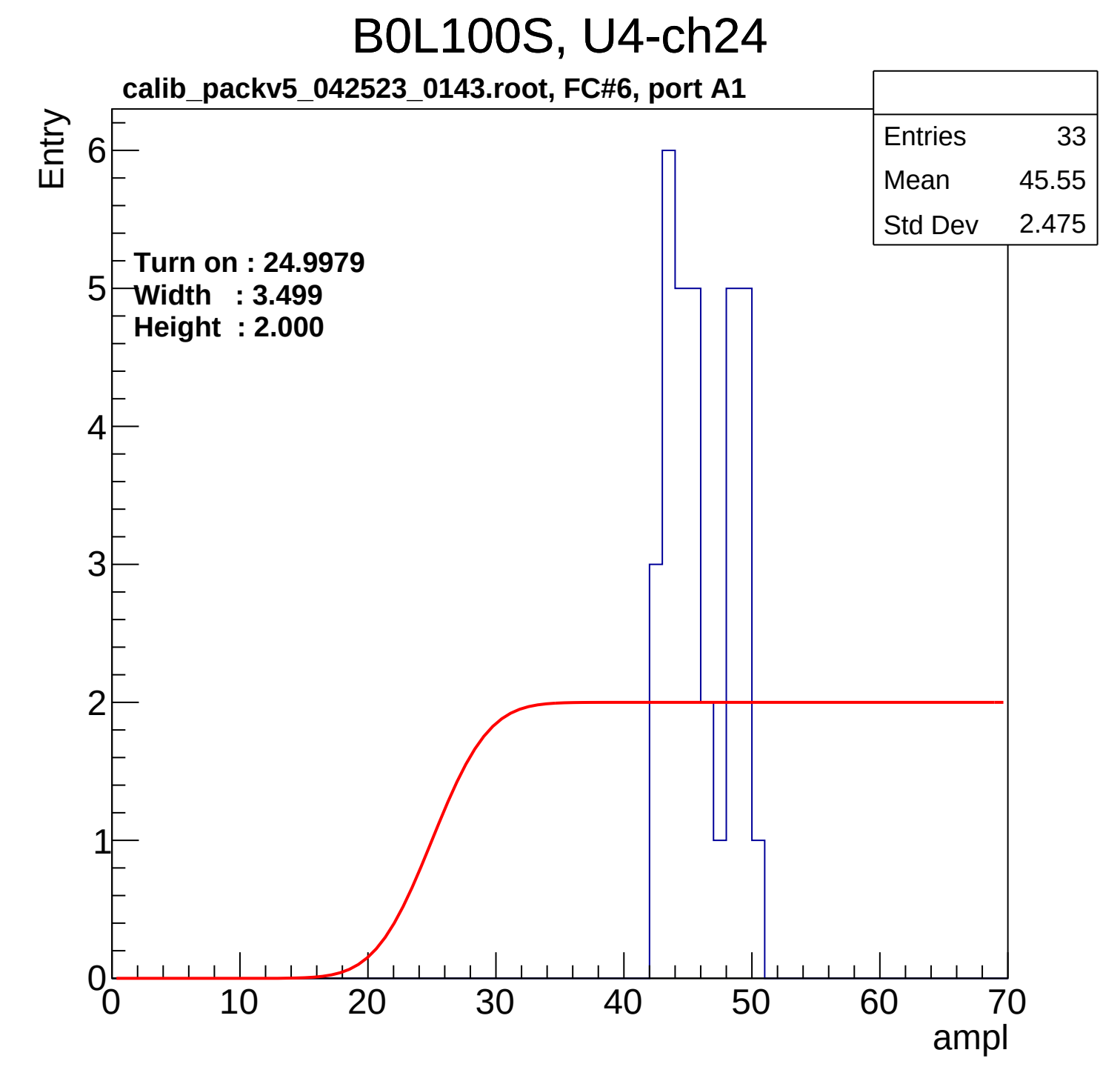

B0L100S, U4-ch19
calib_packv5_042523_0143.root, FC#6, port A1
Entries 4
Mean 50
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B0L100S, U4-ch20
calib_packv5_042523_0143.root, FC#6, port A1
Entries 32
Mean 49.72
Std Dev 2.05
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U4-ch21
calib_packv5_042523_0143.root, FC#6, port A1
Entries 10
Mean 50.1
Std Dev 0.7
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U4-ch22
calib_packv5_042523_0143.root, FC#6, port A1
Entries 33
Mean 44.36
Std Dev 2.281
Turn on : 24.9988
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U4-ch23
calib_packv5_042523_0143.root, FC#6, port A1
Entries 10
Mean 45.9
Std Dev 0.7
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B0L100S, U4-ch24
calib_packv5_042523_0143.root, FC#6, port A1
Entries 33
Mean 45.55
Std Dev 2.475
Turn on : 24.9979
Width : 3.499
Height : 2.000
Entry
ampl
0
1
2
3
4
5
6
0
10
20
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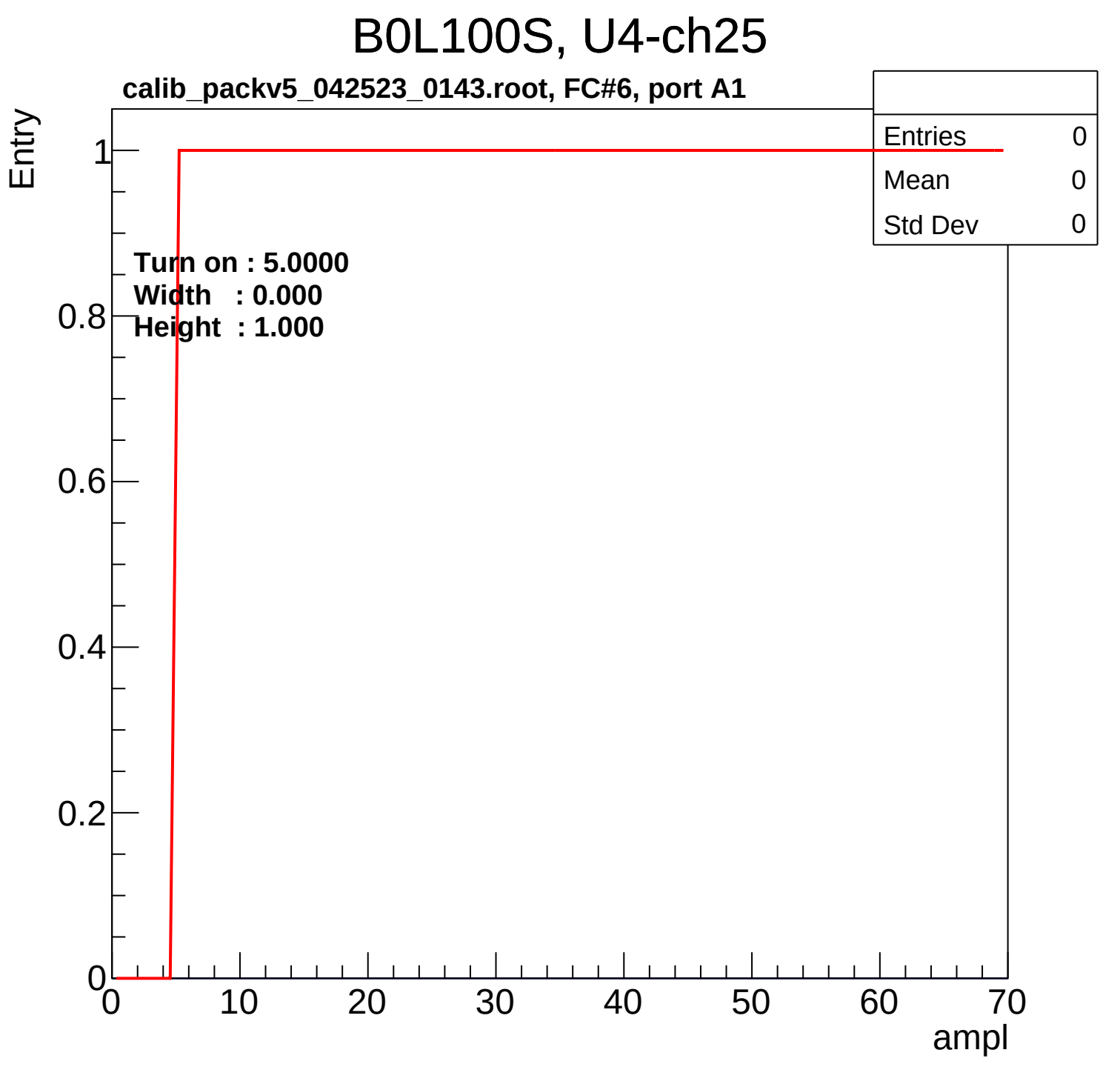
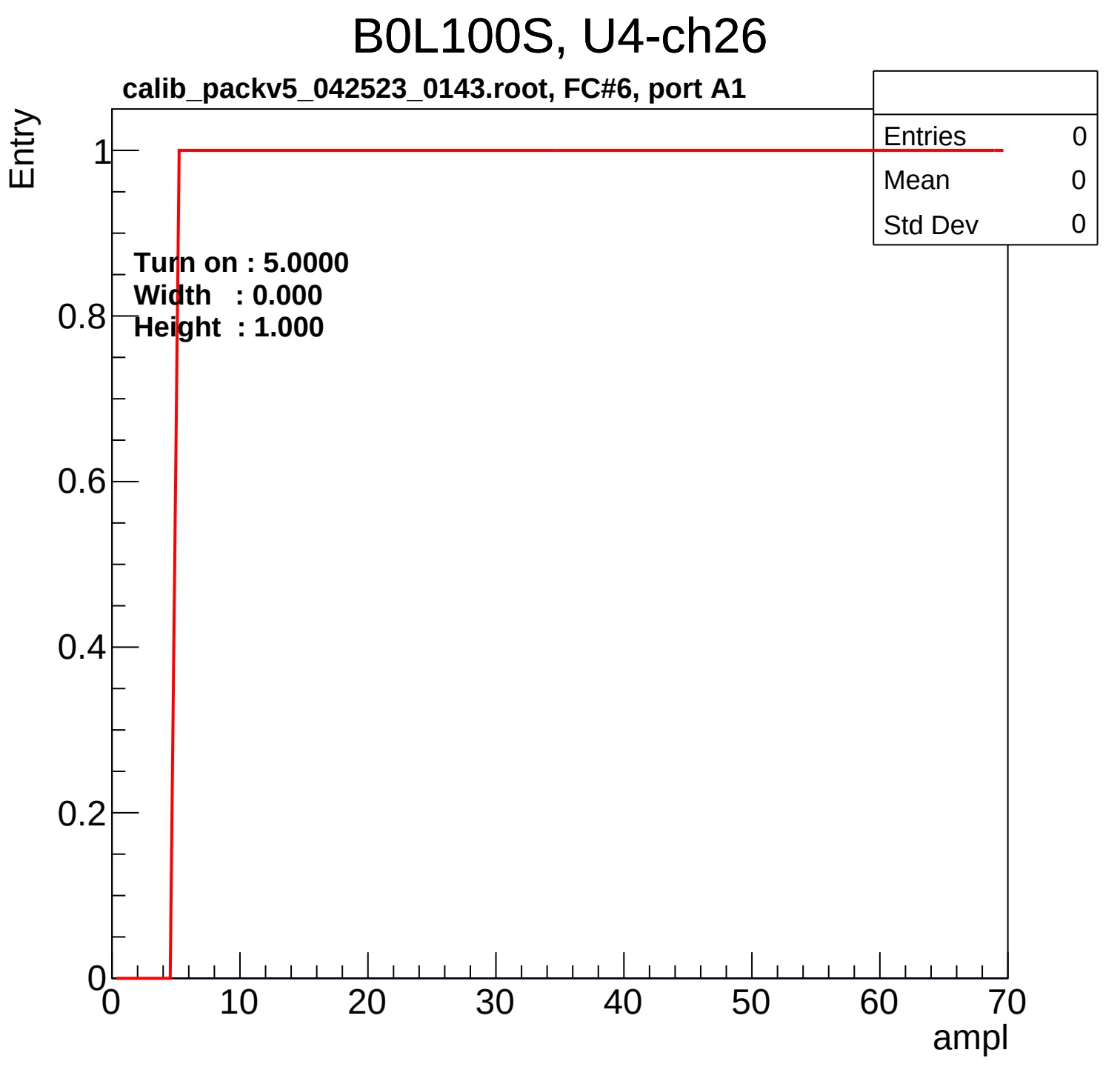
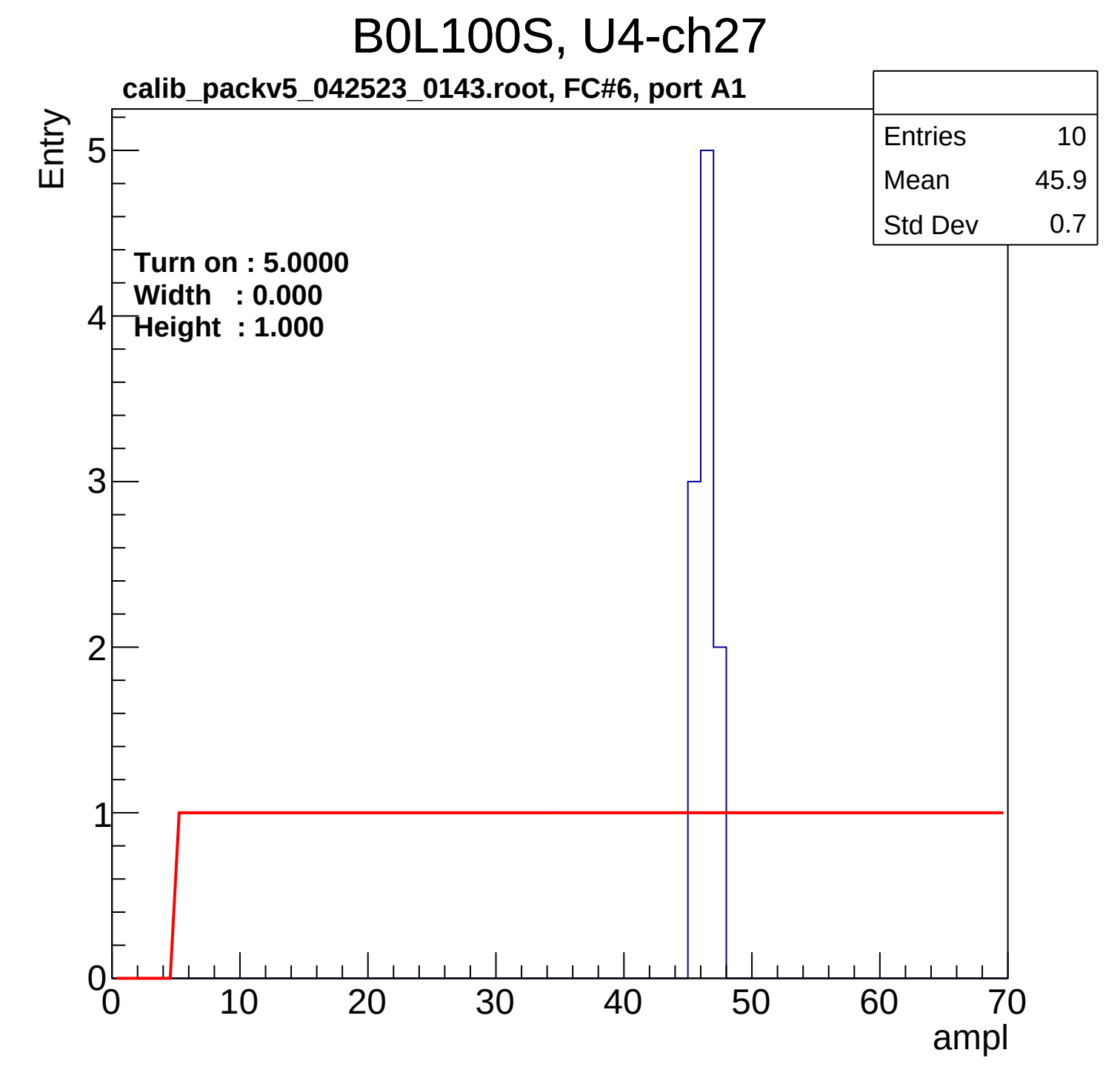
40
50
60
70


B0L100S, U4-ch25
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U4-ch26
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U4-ch27
calib_packv5_042523_0143.root, FC#6, port A1
Entries 10
Mean 45.9
Std Dev 0.7
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
10
20
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40
50
60
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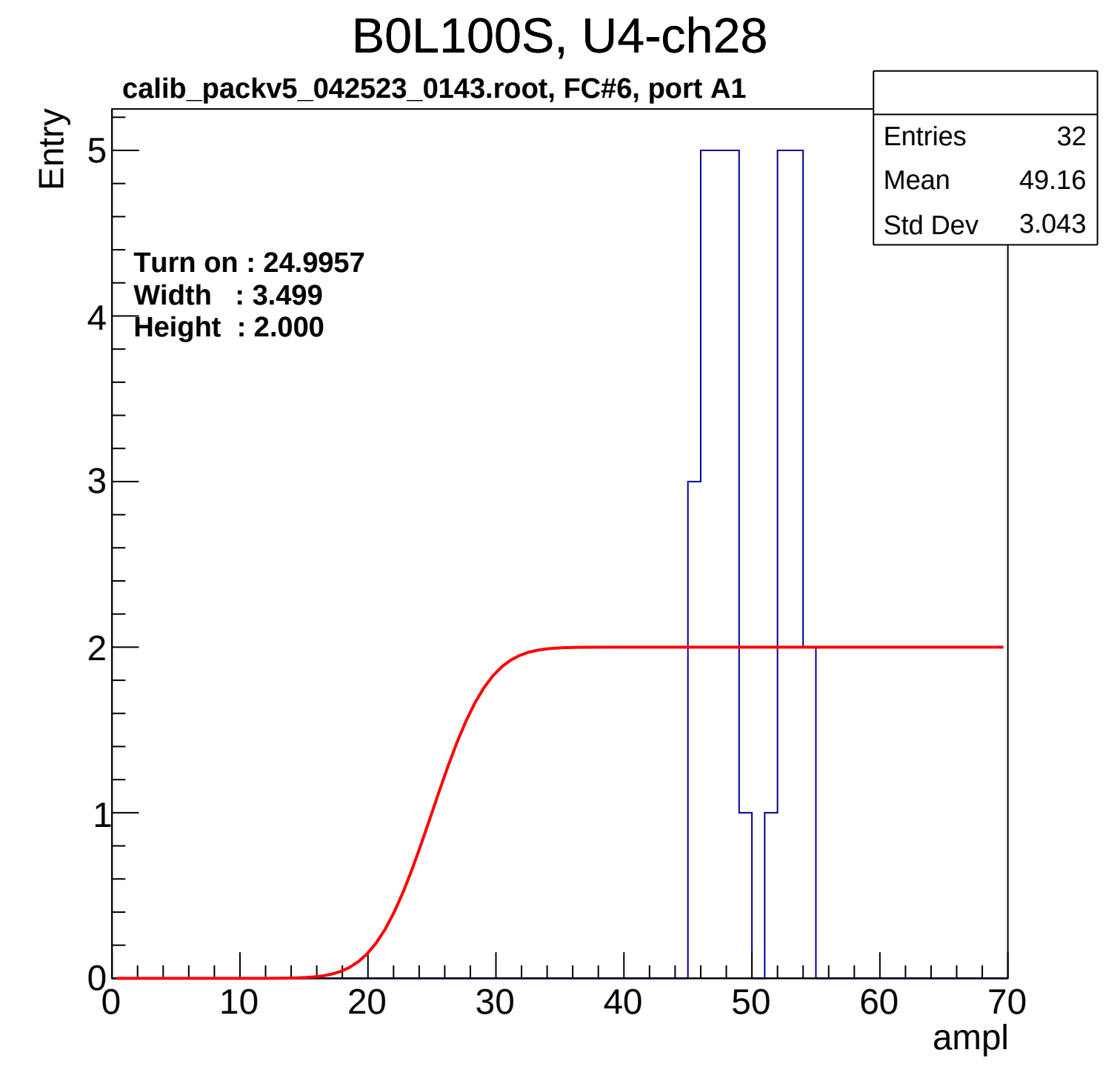
B0L100S, U4-ch28
calib_packv5_042523_0143.root, FC#6, port A1
Entries 32
Mean 49.16
Std Dev 3.043
Turn on : 24.9957
Width : 3.499
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
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20
30
40
50
60
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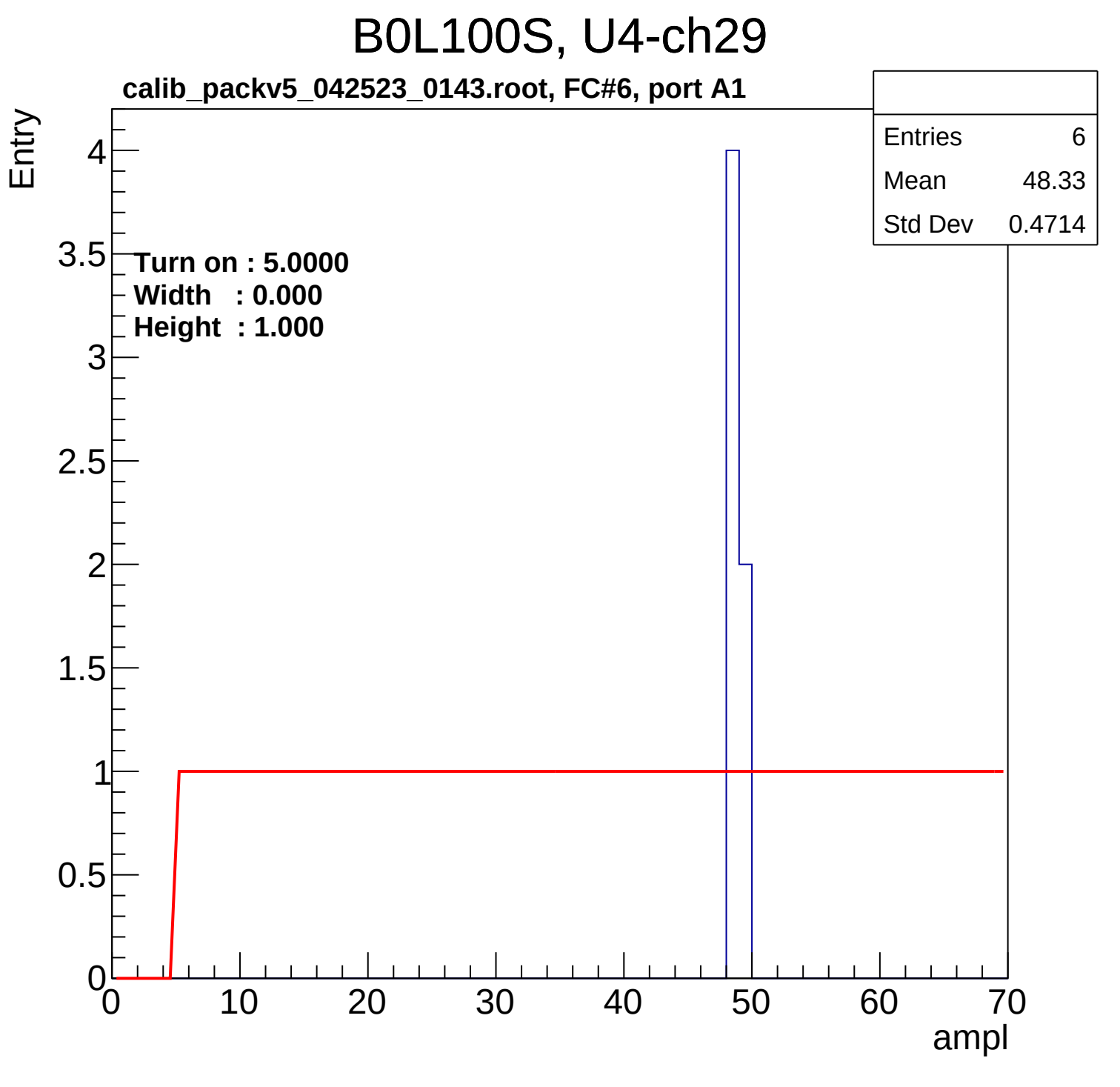
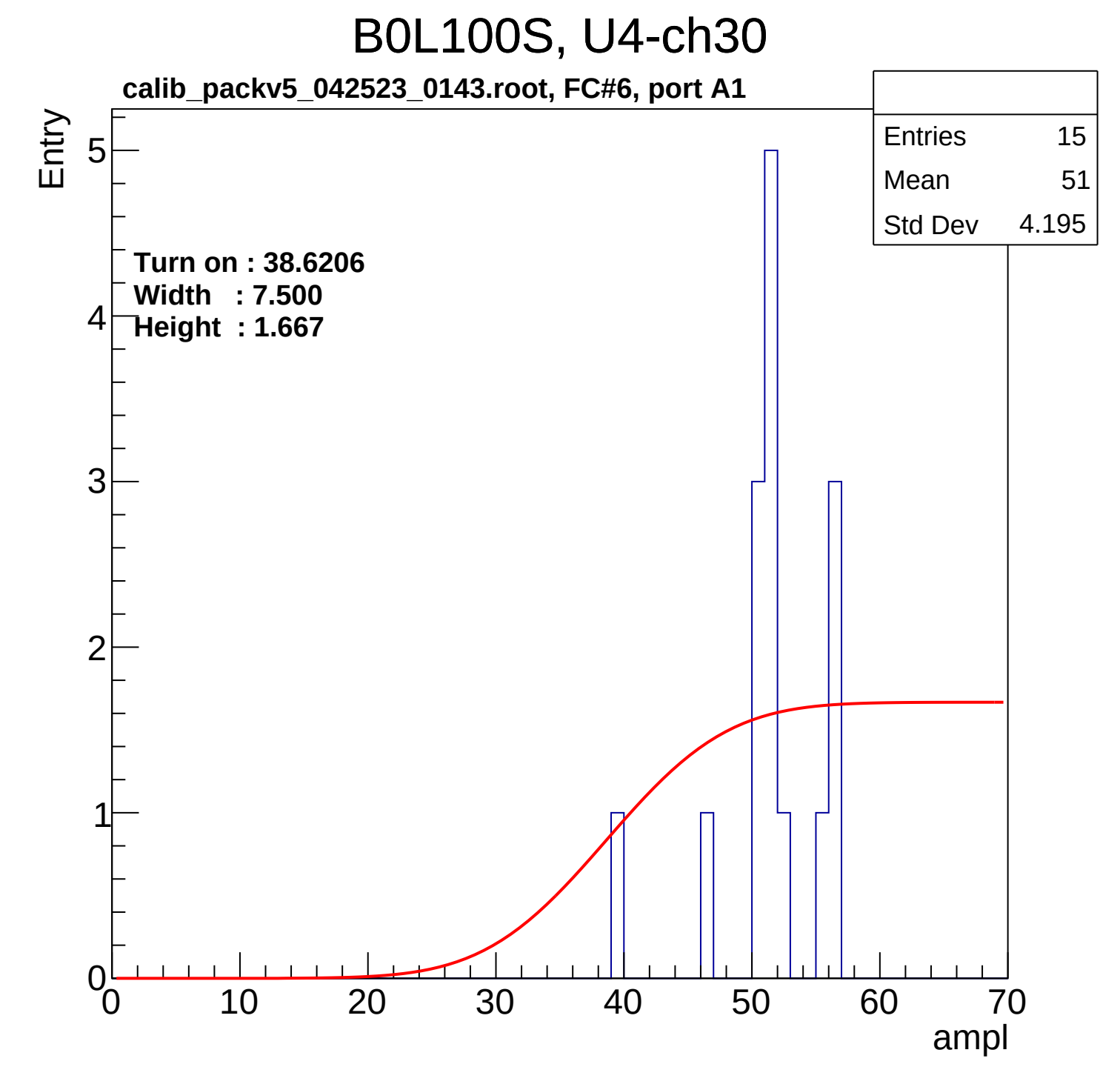
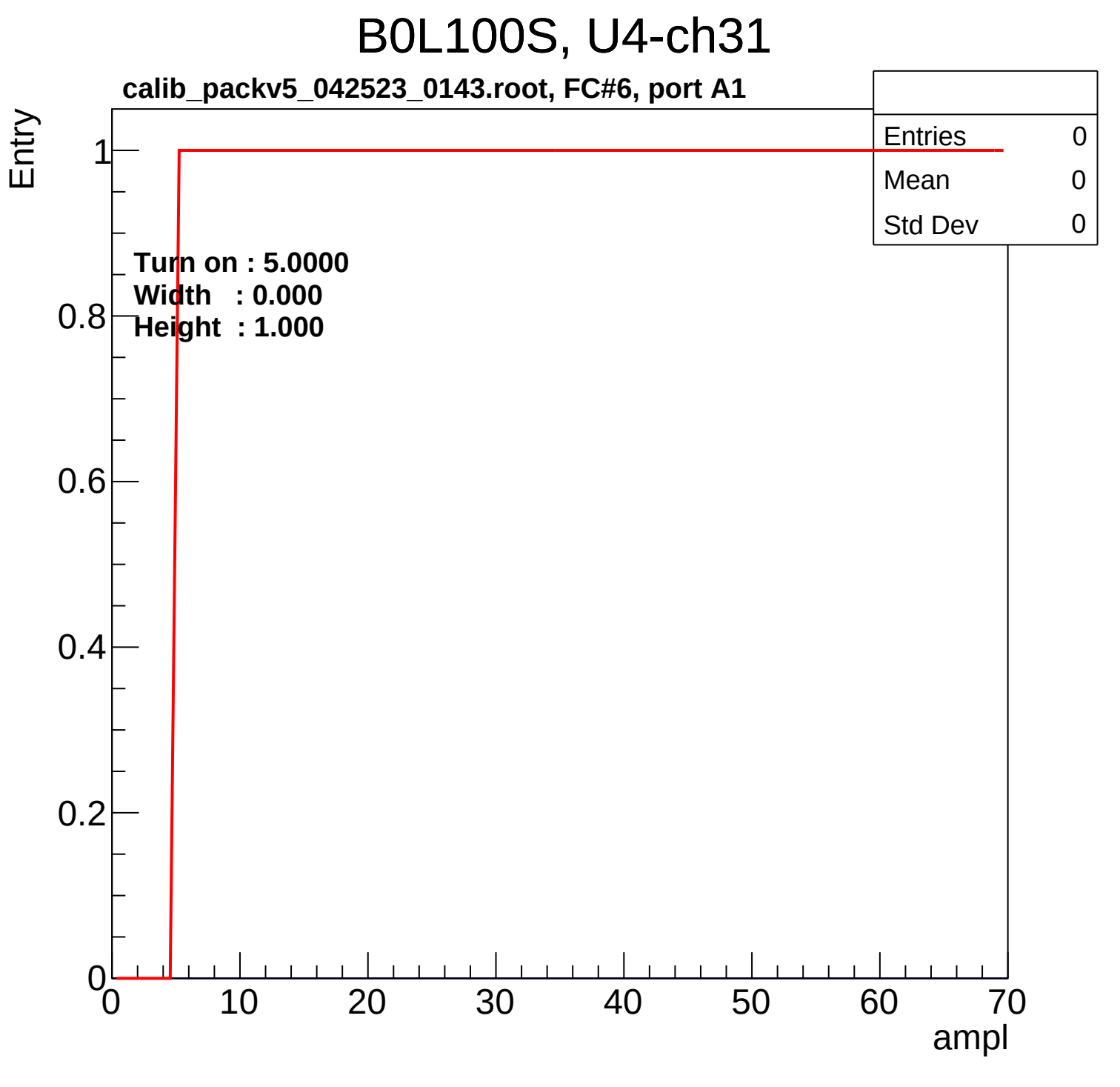
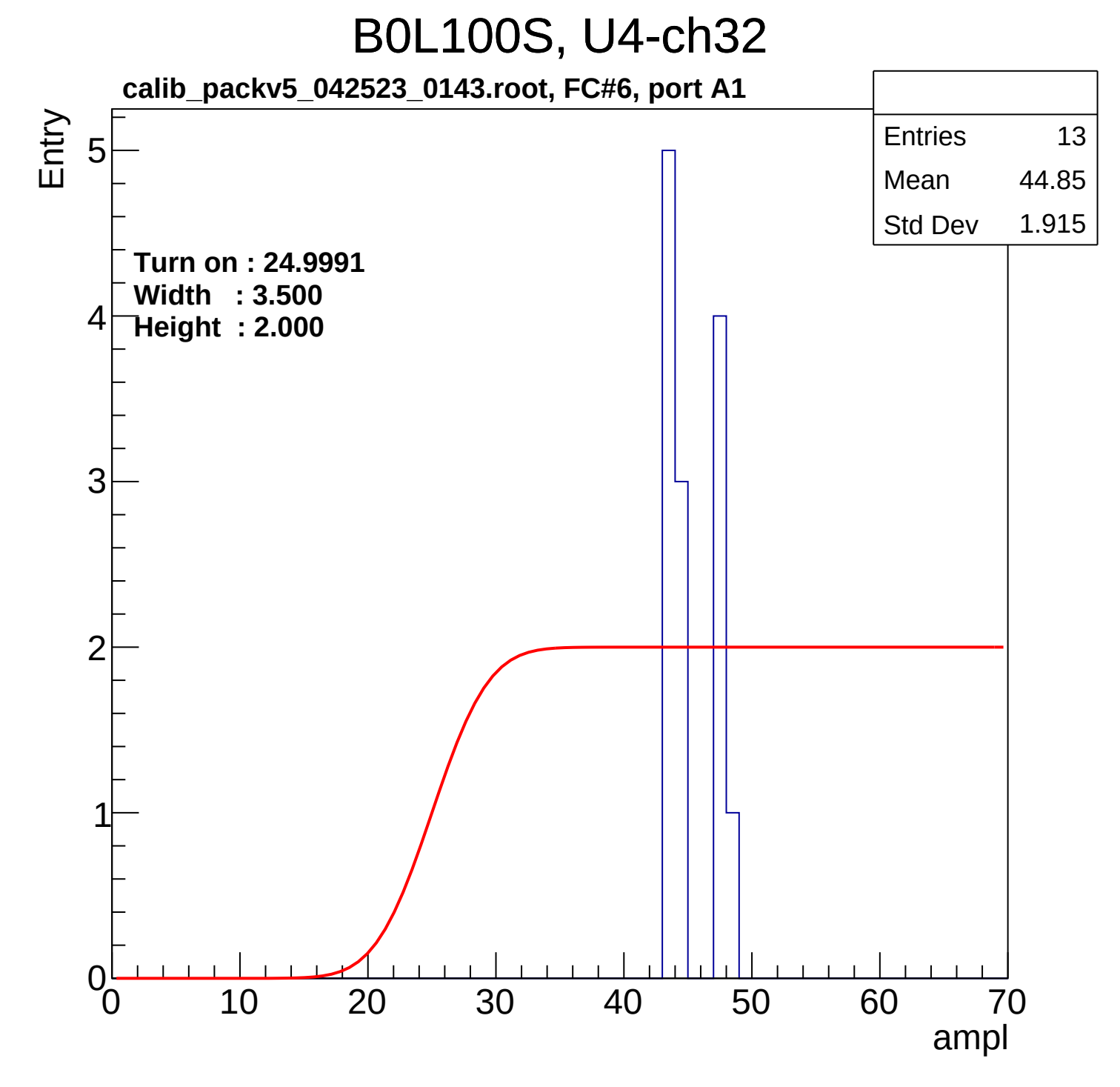
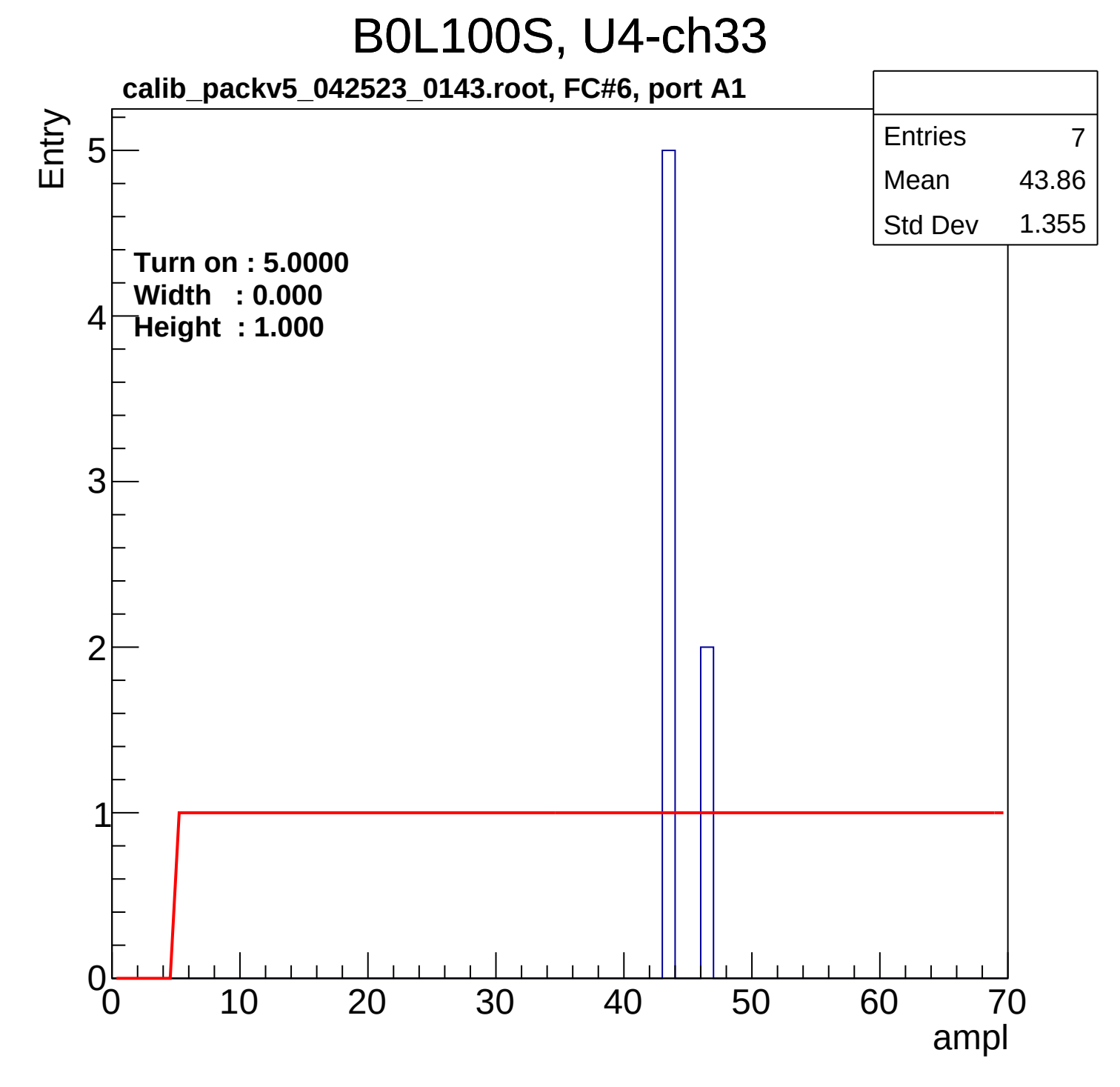
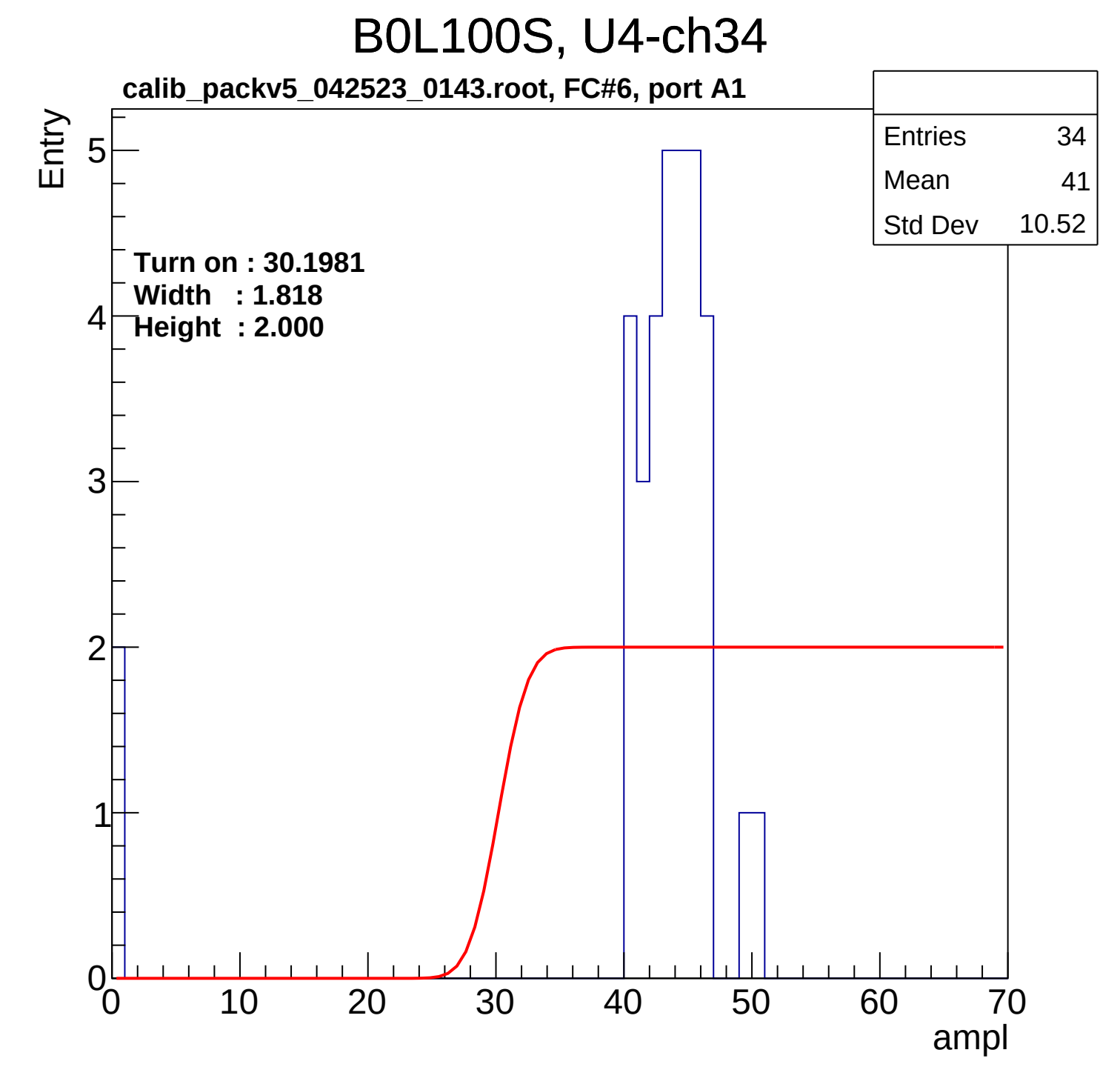

B0L100S, U4-ch29
calib_packv5_042523_0143.root, FC#6, port A1
Entries 6
Mean 48.33
Std Dev 0.4714
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

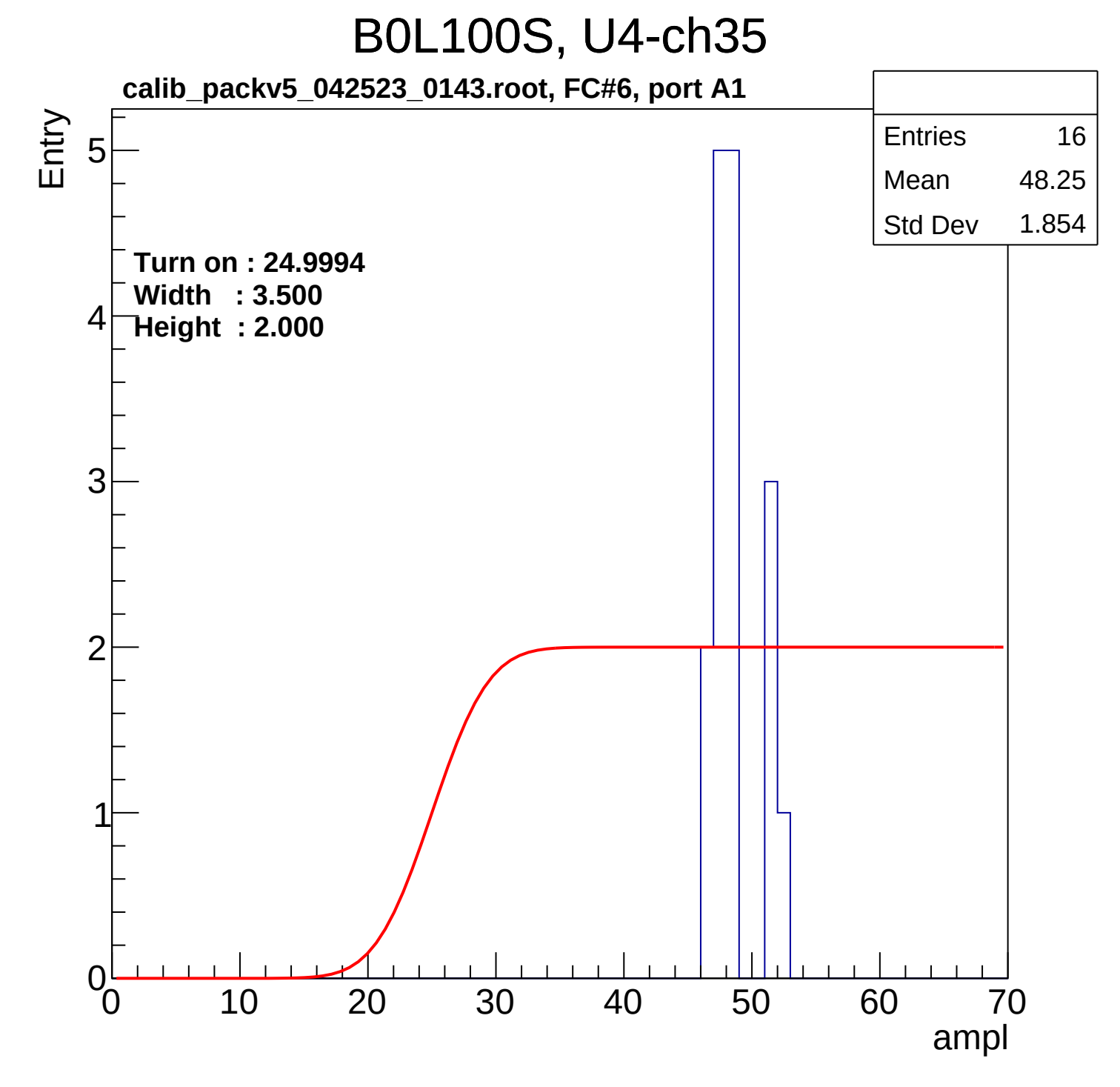

B0L100S, U4-ch30
calib_packv5_042523_0143.root, FC#6, port A1
Entries 15
Mean 51
Std Dev 4.195
Turn on : 38.6206
Width : 7.500
Height : 1.667
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

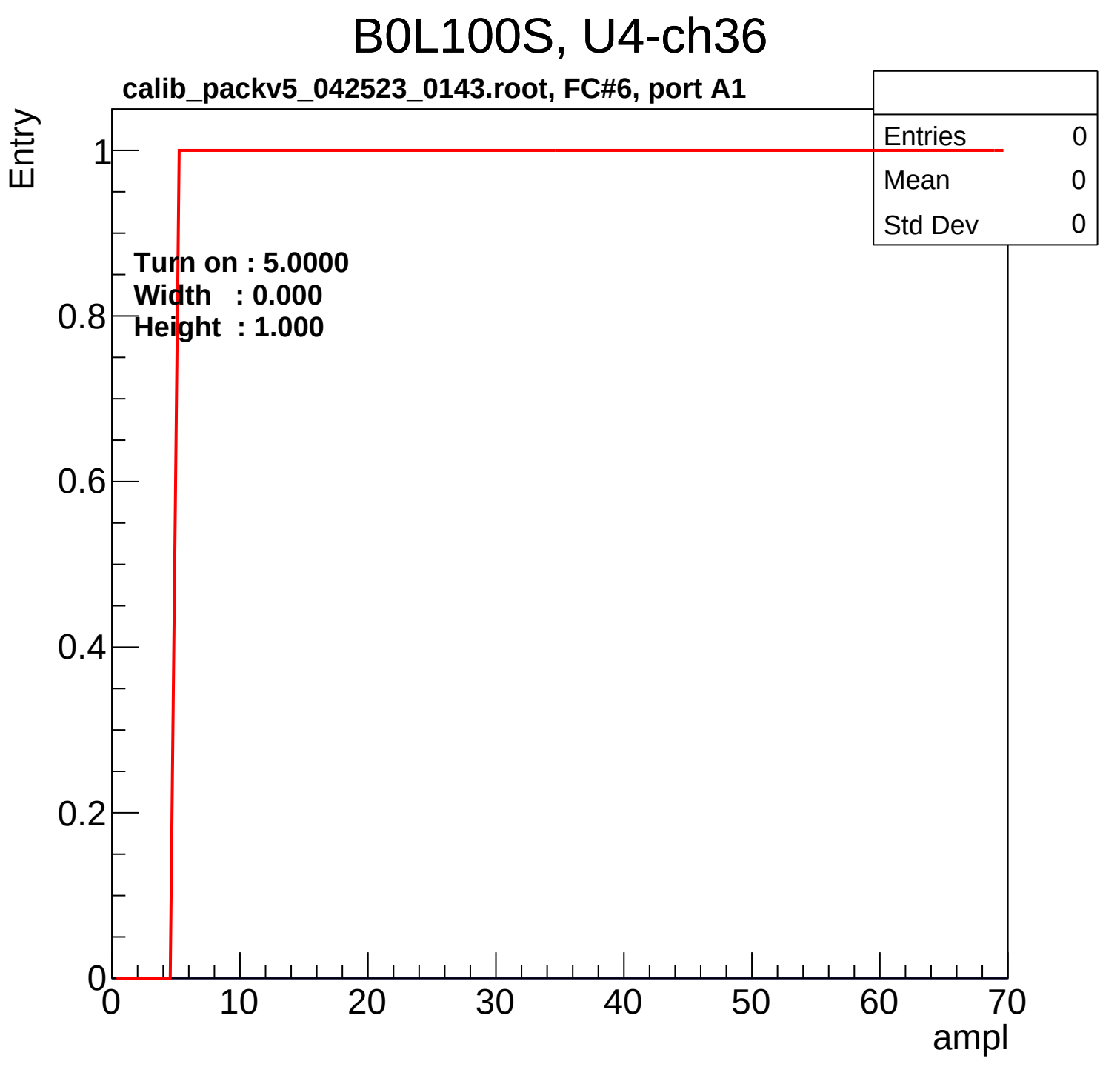

B0L100S, U4-ch31
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

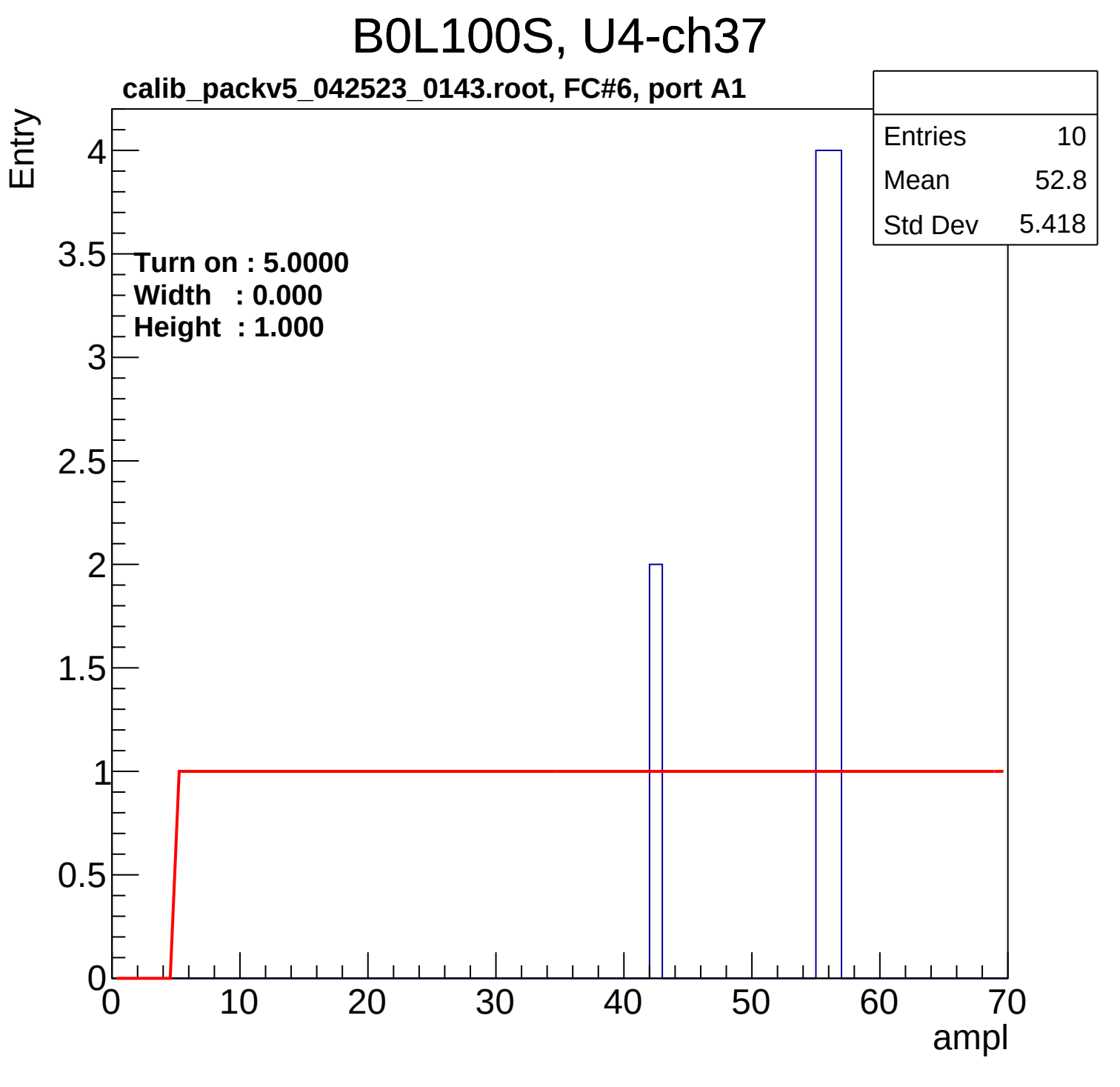

B0L100S, U4-ch32
calib_packv5_042523_0143.root, FC#6, port A1
Entries 13
Mean 44.85
Std Dev 1.915
Turn on : 24.9991
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

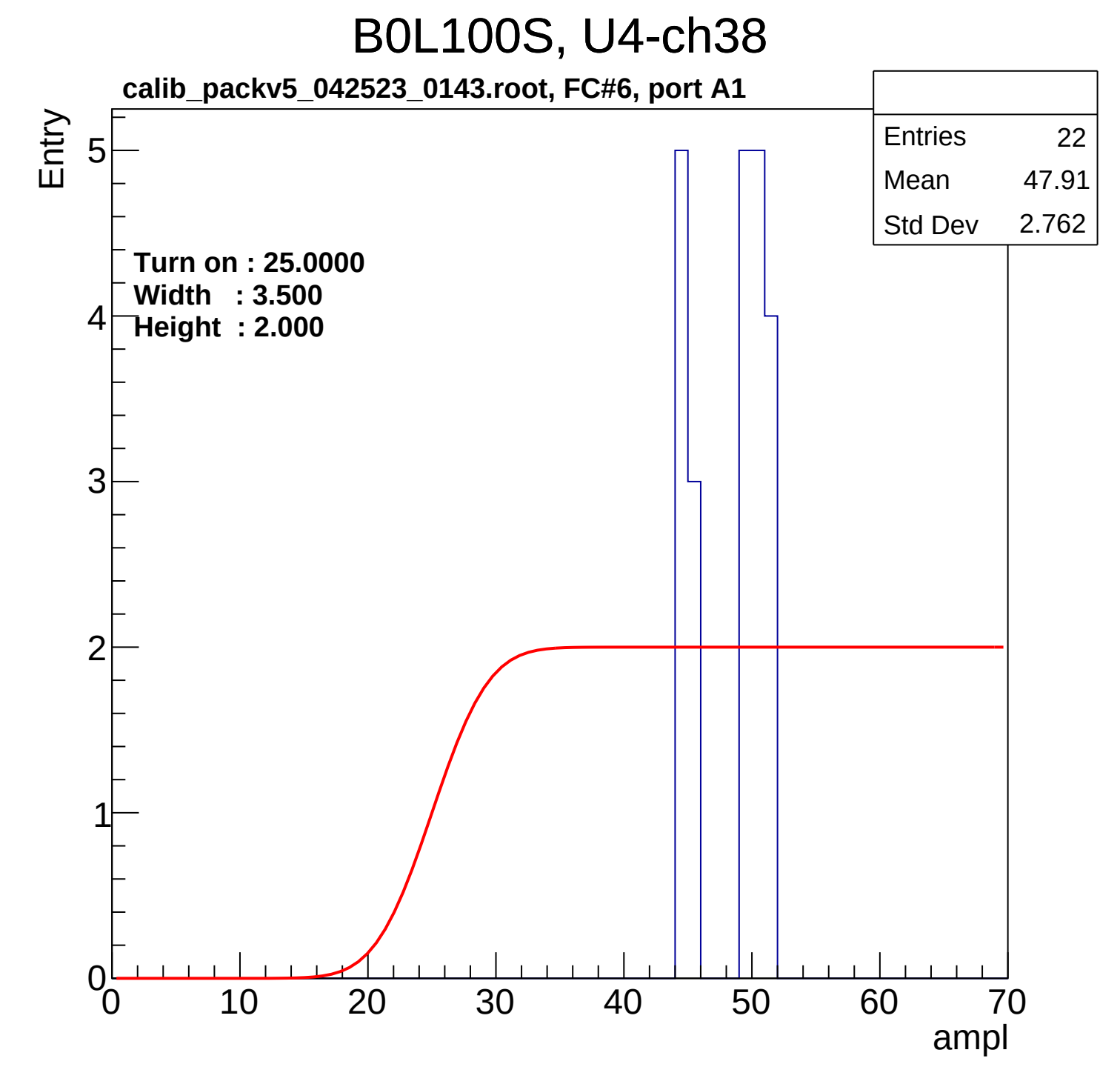

B0L100S, U4-ch33
calib_packv5_042523_0143.root, FC#6, port A1
Entries 7
Mean 43.86
Std Dev 1.355
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

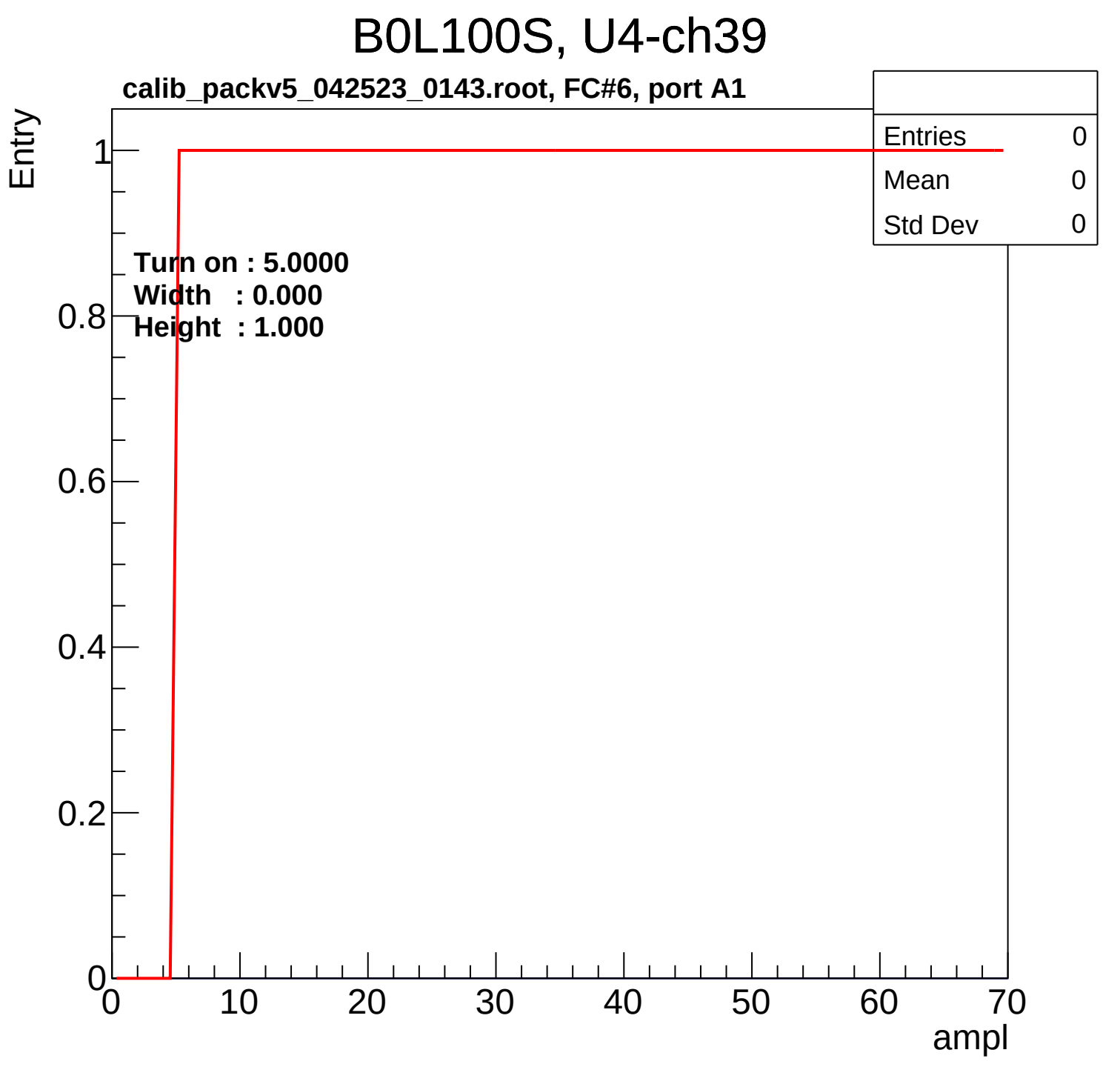

B0L100S, U4-ch34
calib_packv5_042523_0143.root, FC#6, port A1
Entries 34
Mean 41
Std Dev 10.52
Turn on : 30.1981
Width : 1.818
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

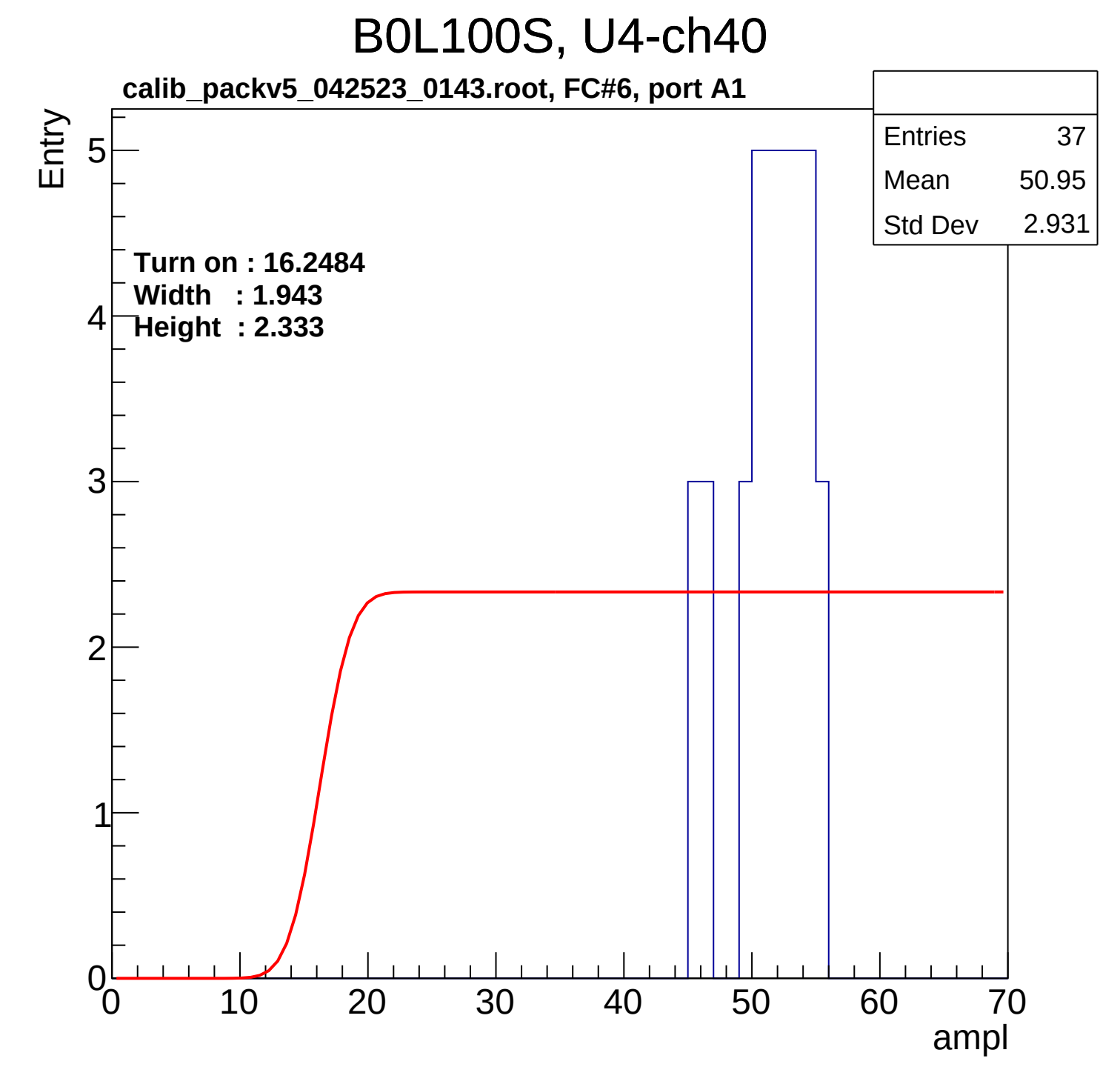

B0L100S, U4-ch35
calib_packv5_042523_0143.root, FC#6, port A1
Entries 16
Mean 48.25
Std Dev 1.854
Turn on : 24.9994
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

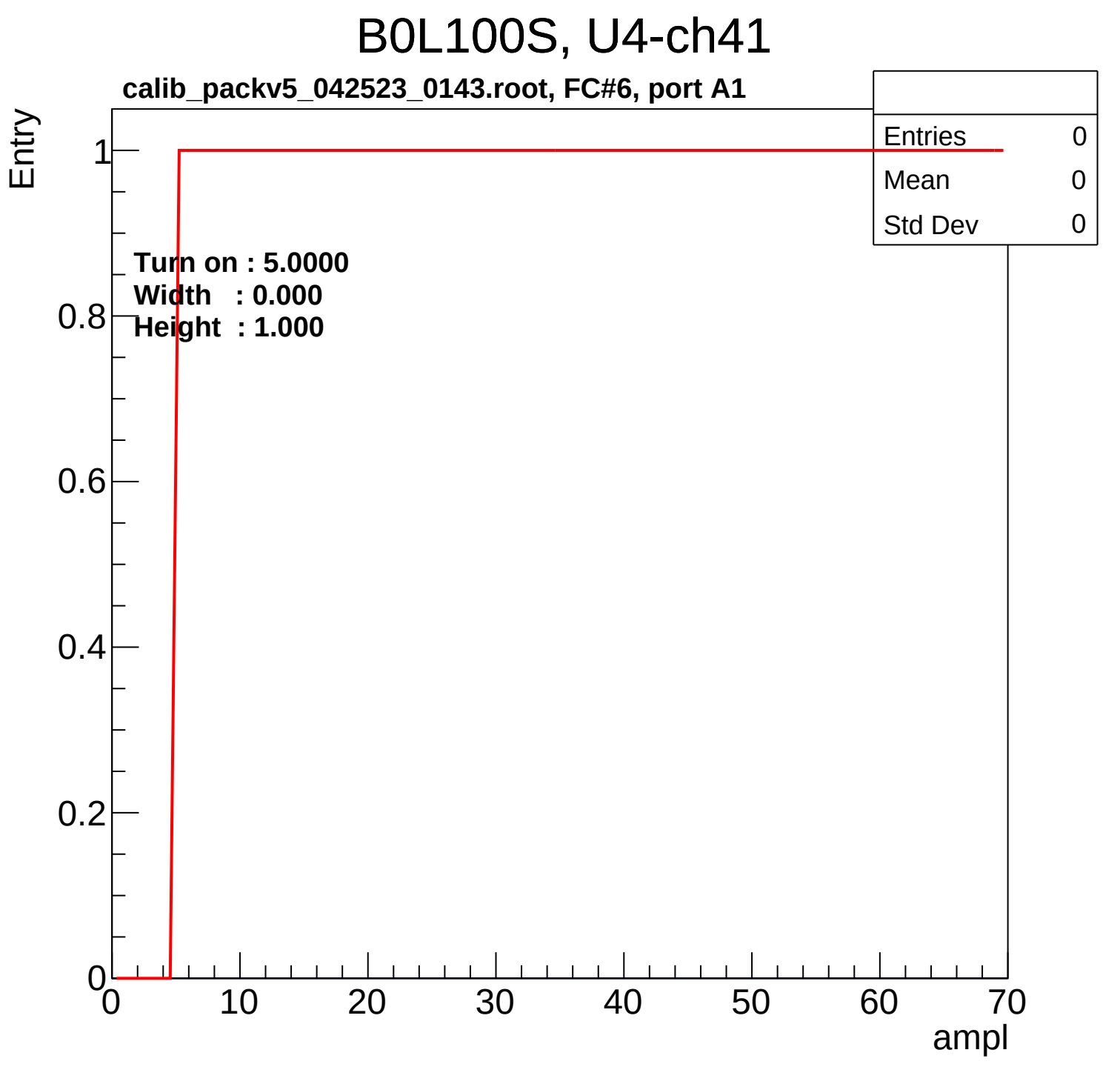

B0L100S, U4-ch36
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

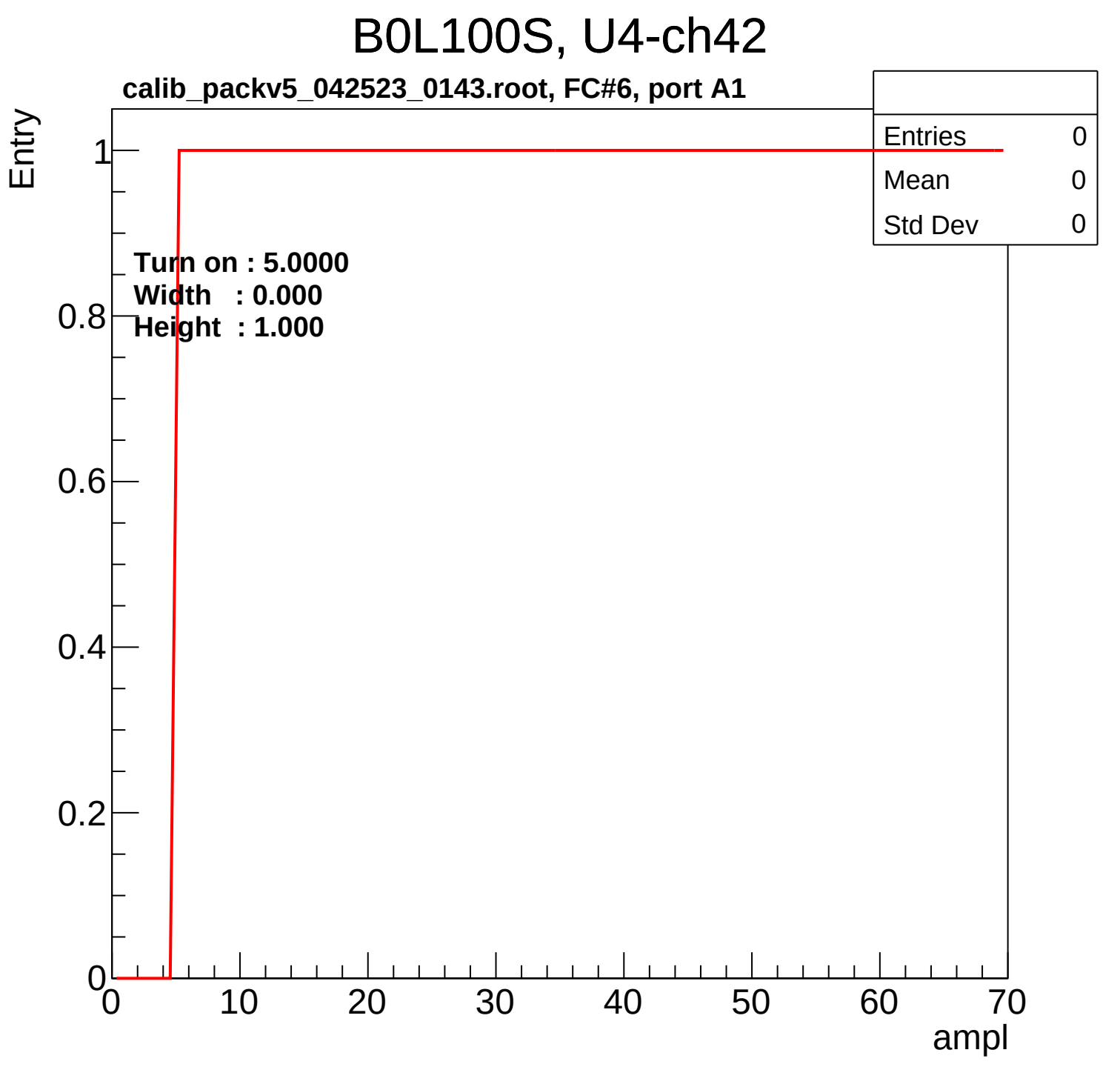

B0L100S, U4-ch37
calib_packv5_042523_0143.root, FC#6, port A1
Entries 10
Mean 52.8
Std Dev 5.418
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

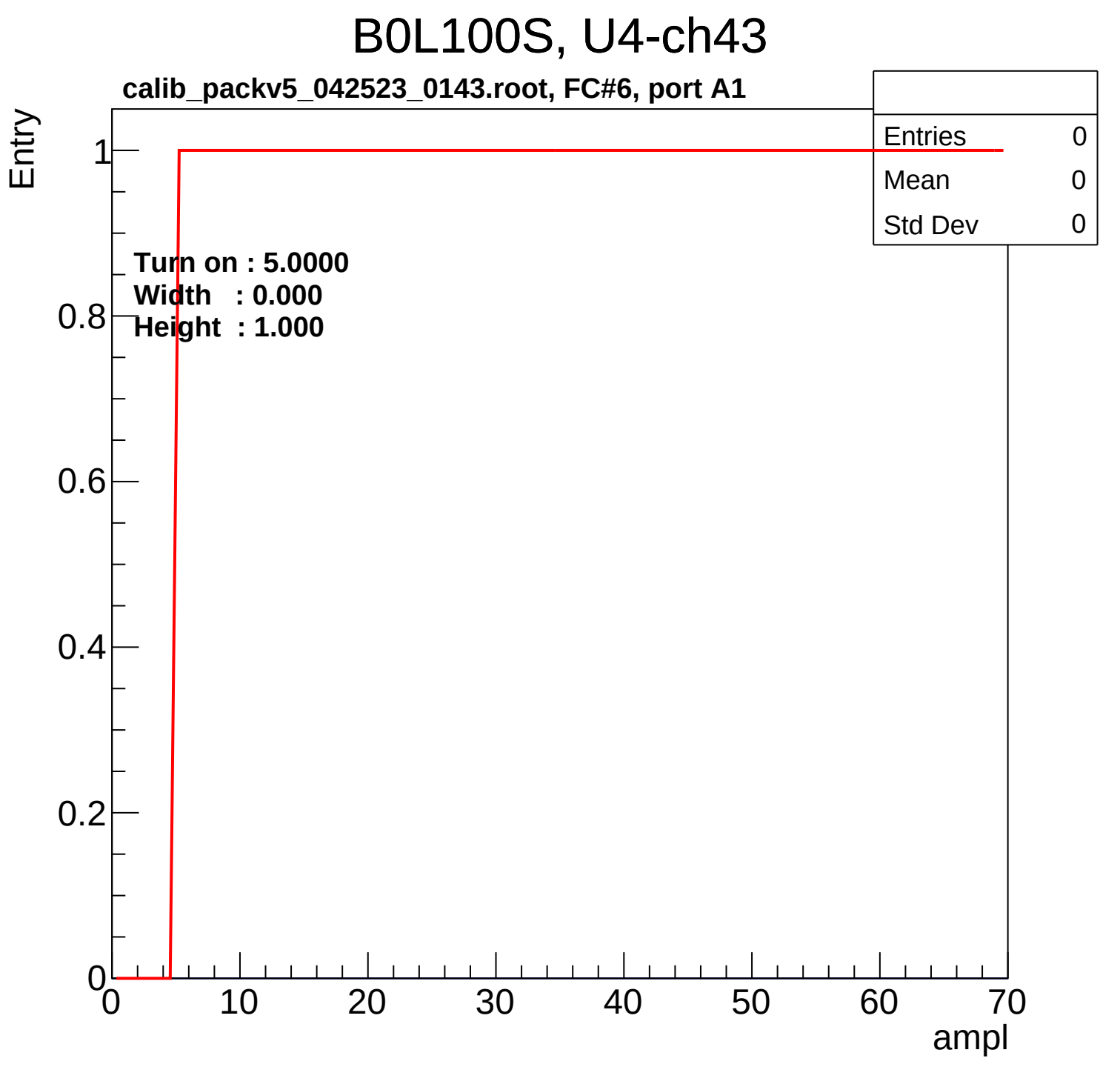

B0L100S, U4-ch38
calib_packv5_042523_0143.root, FC#6, port A1
Entries 22
Mean 47.91
Std Dev 2.762
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

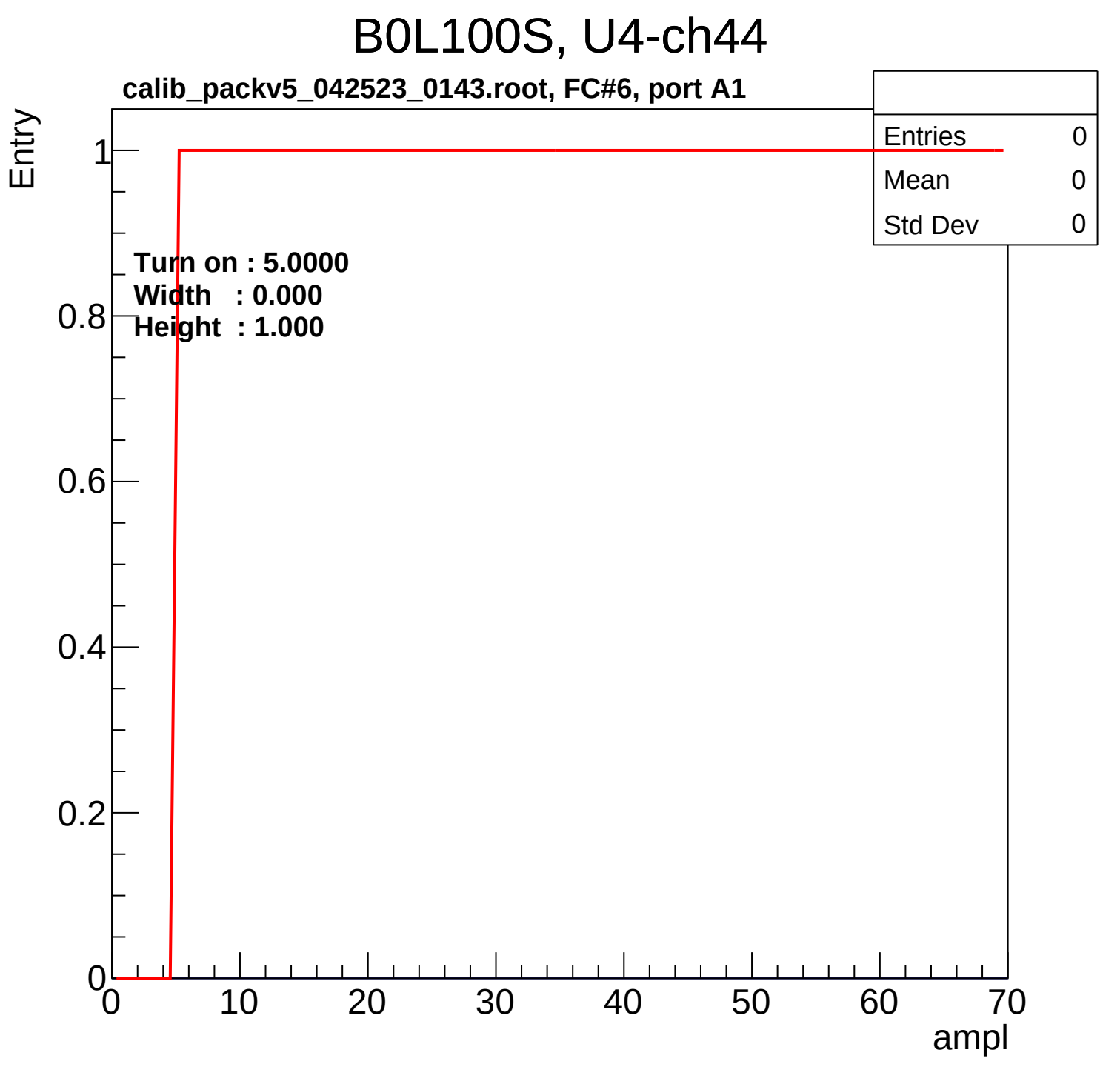

B0L100S, U4-ch39
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

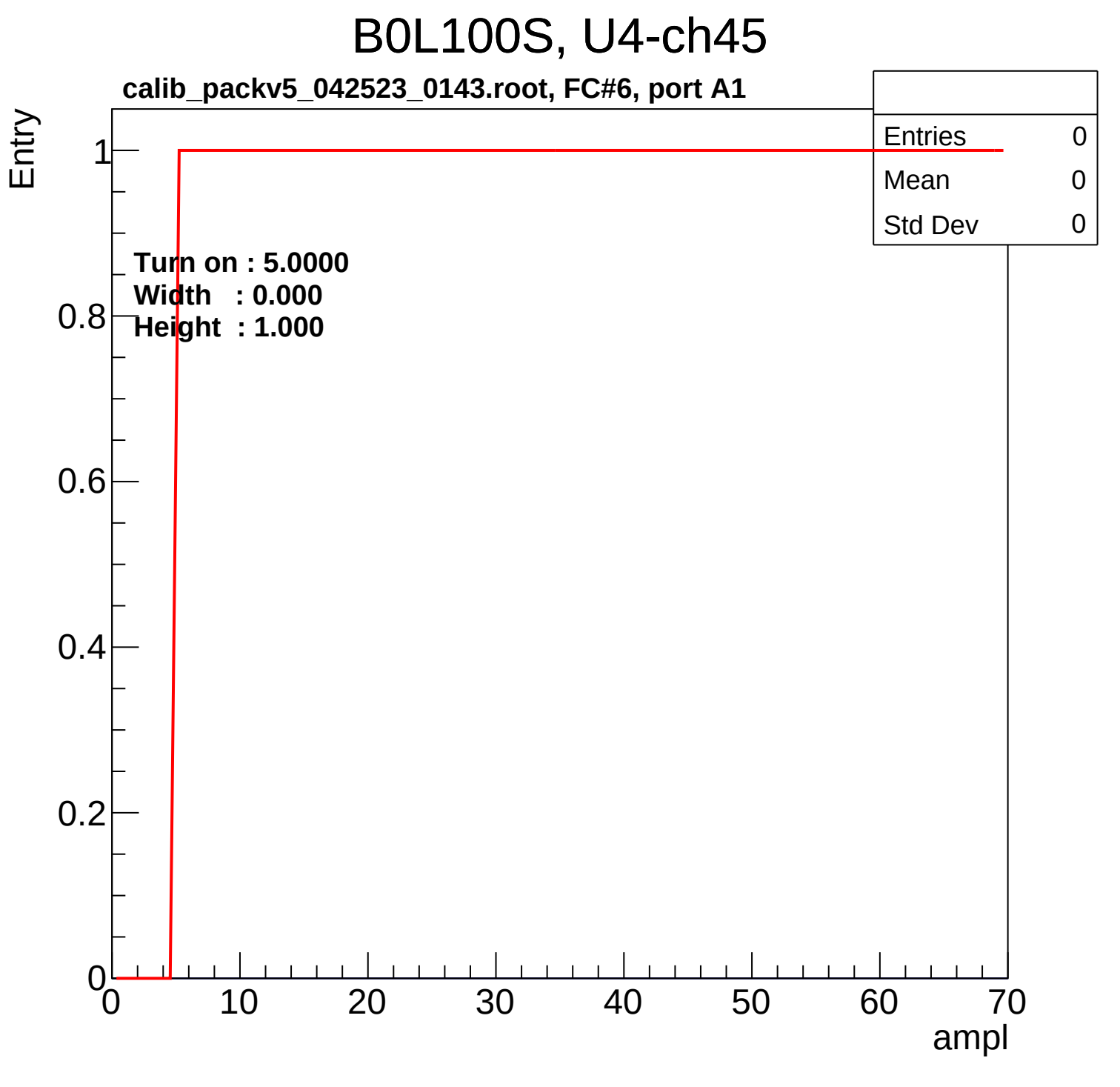

B0L100S, U4-ch40
calib_packv5_042523_0143.root, FC#6, port A1
Entries 37
Mean 50.95
Std Dev 2.931
Turn on : 16.2484
Width : 1.943
Height : 2.333
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

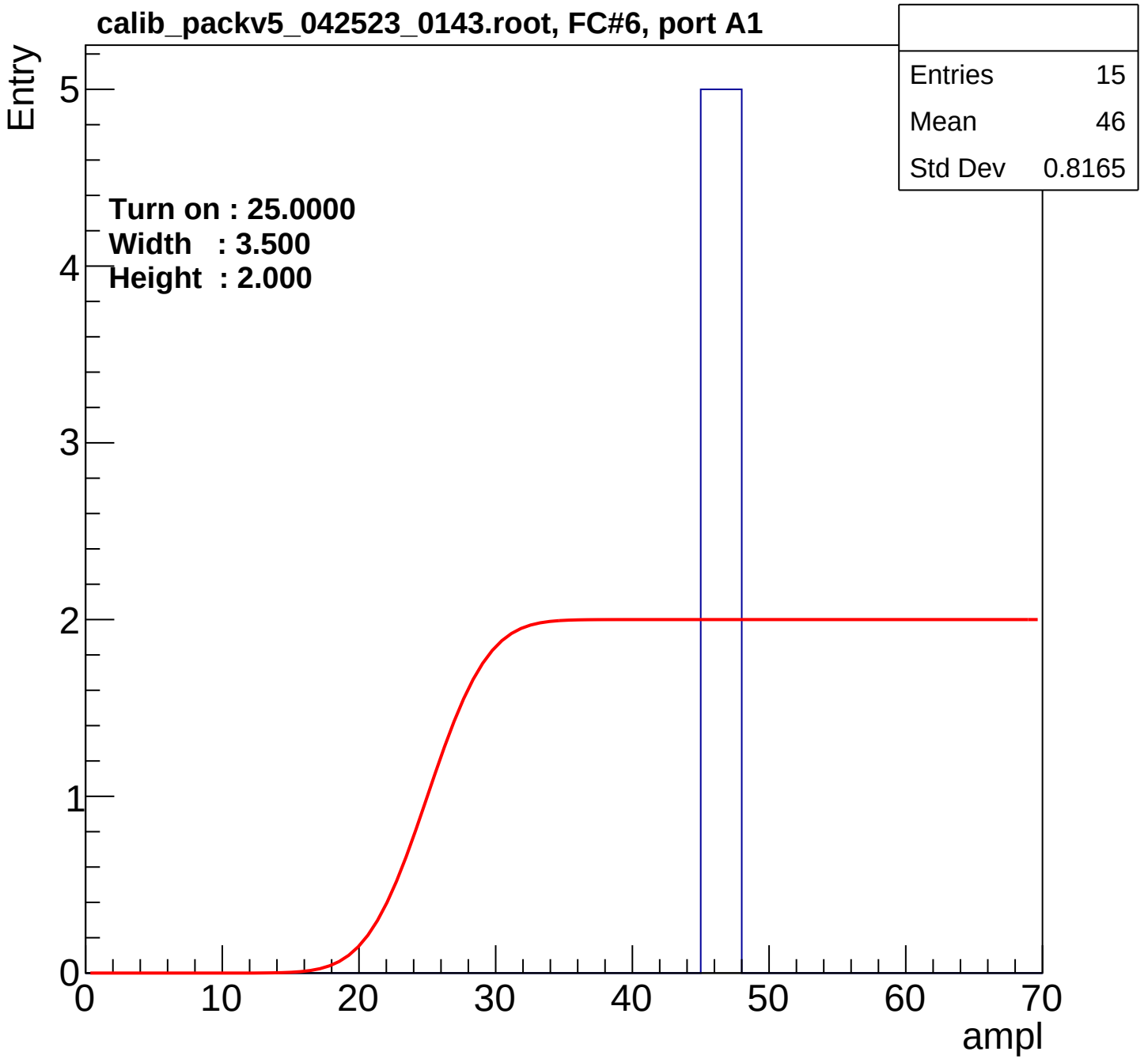

B0L100S, U4-ch41
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

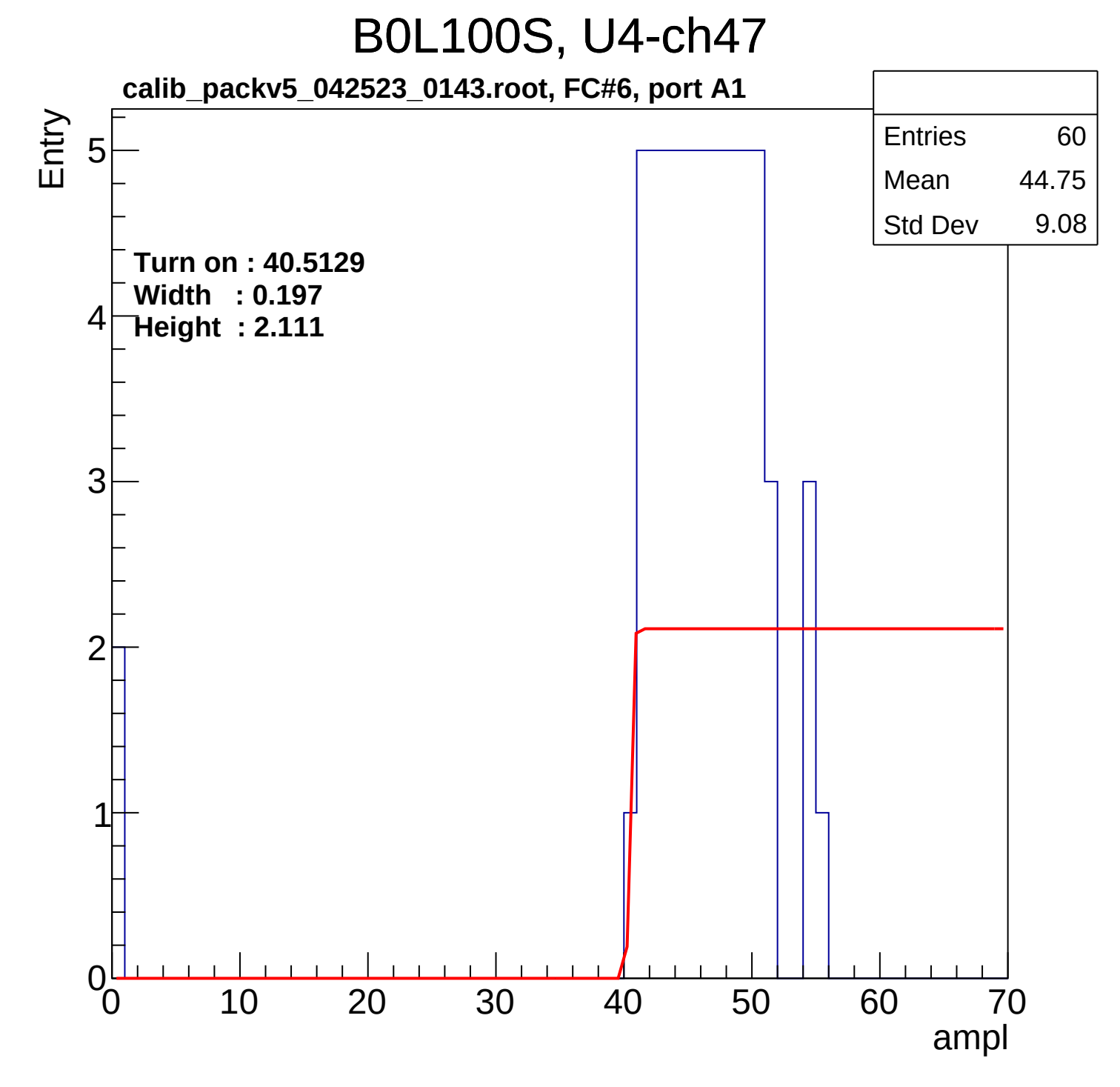

B0L100S, U4-ch42
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

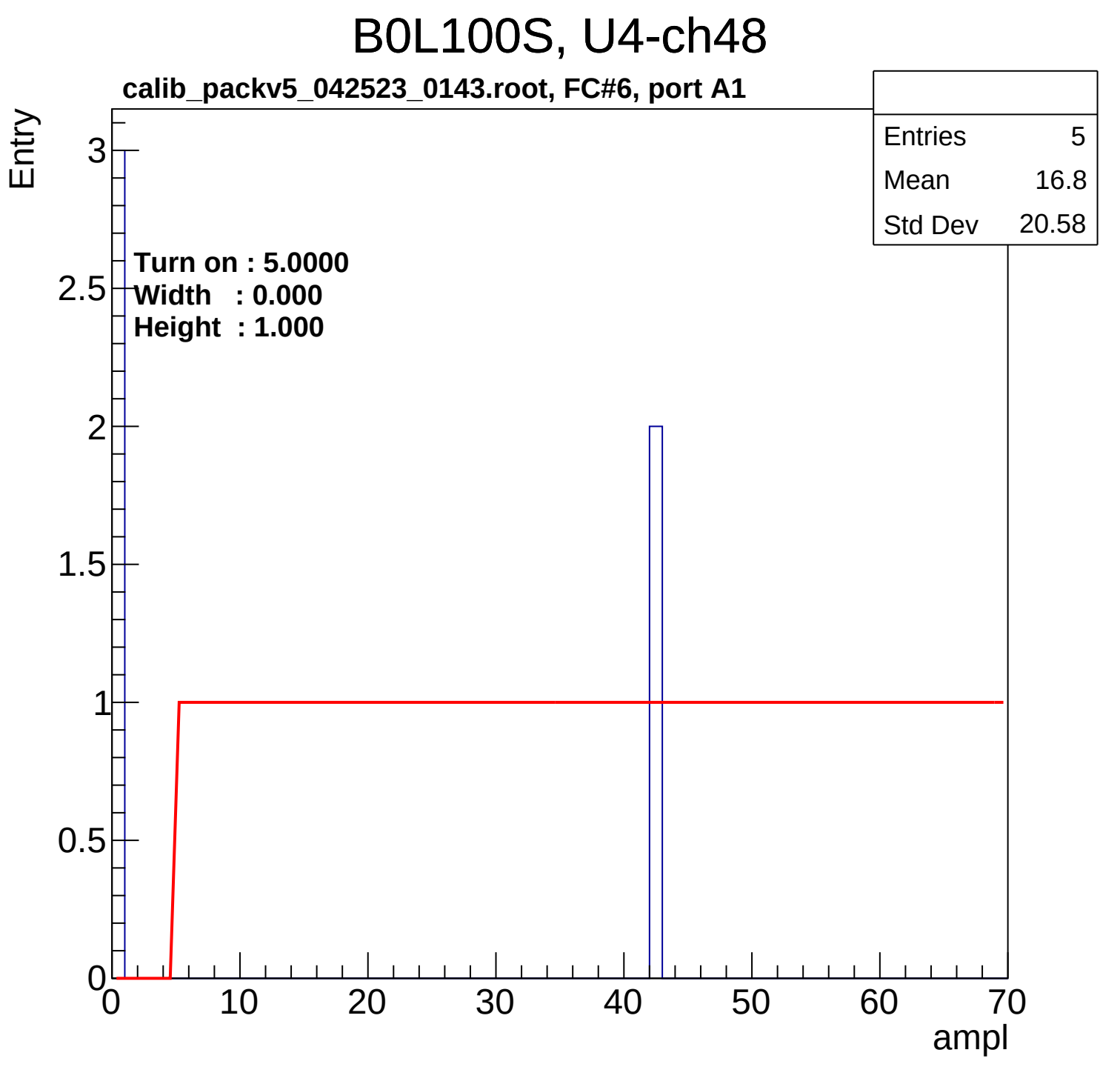

B0L100S, U4-ch43
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

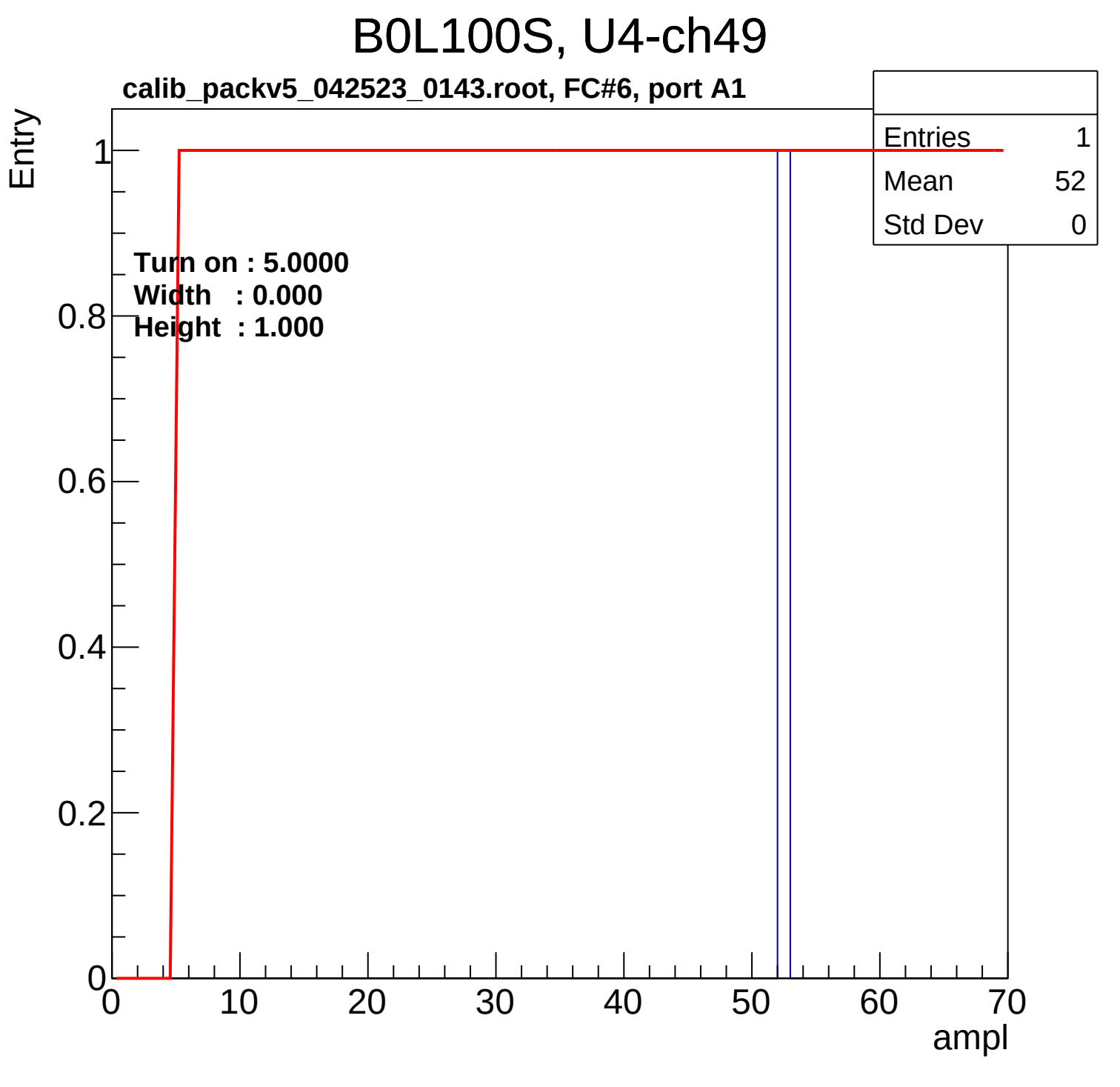

B0L100S, U4-ch44
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

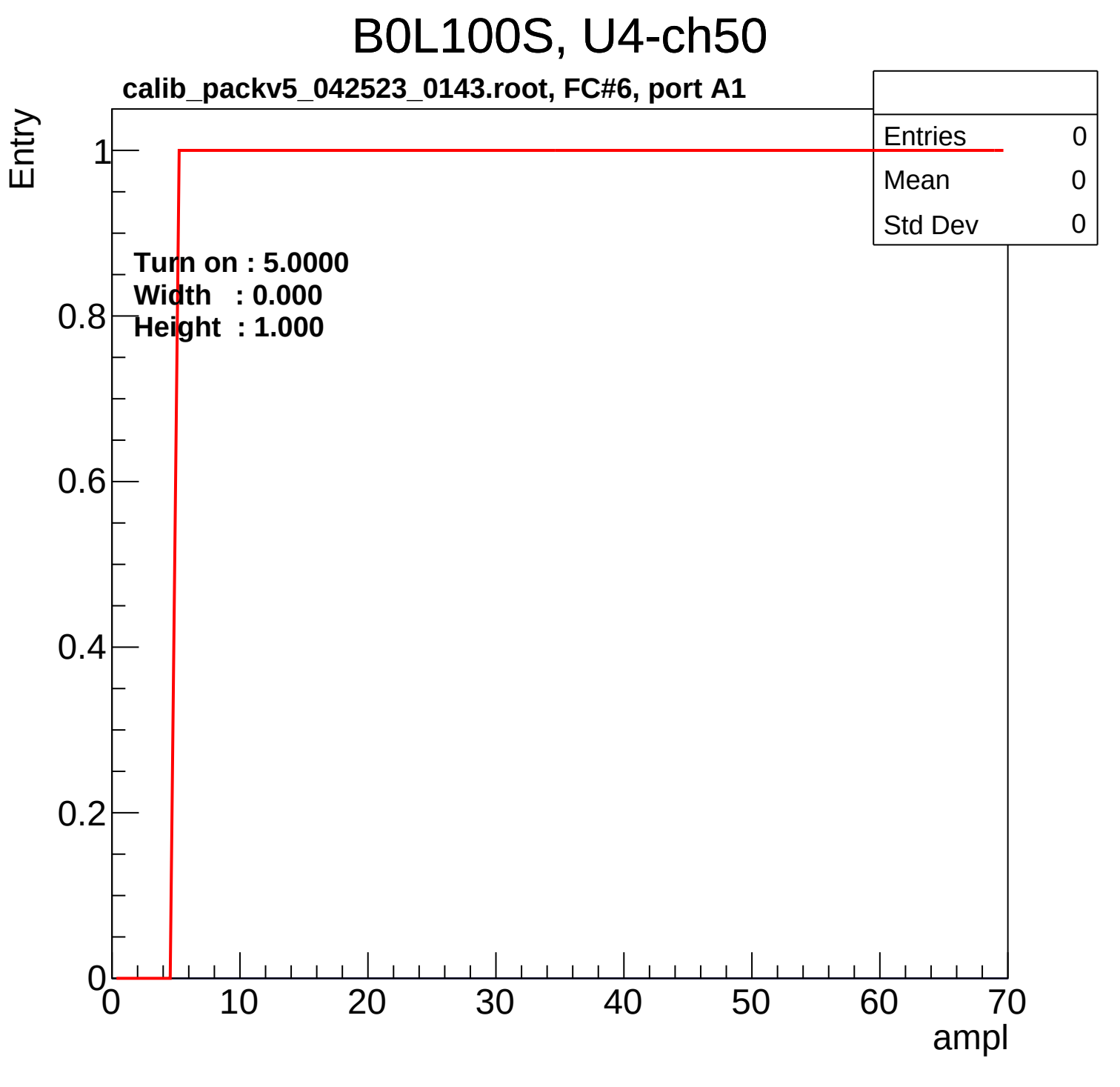

B0L100S, U4-ch45
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

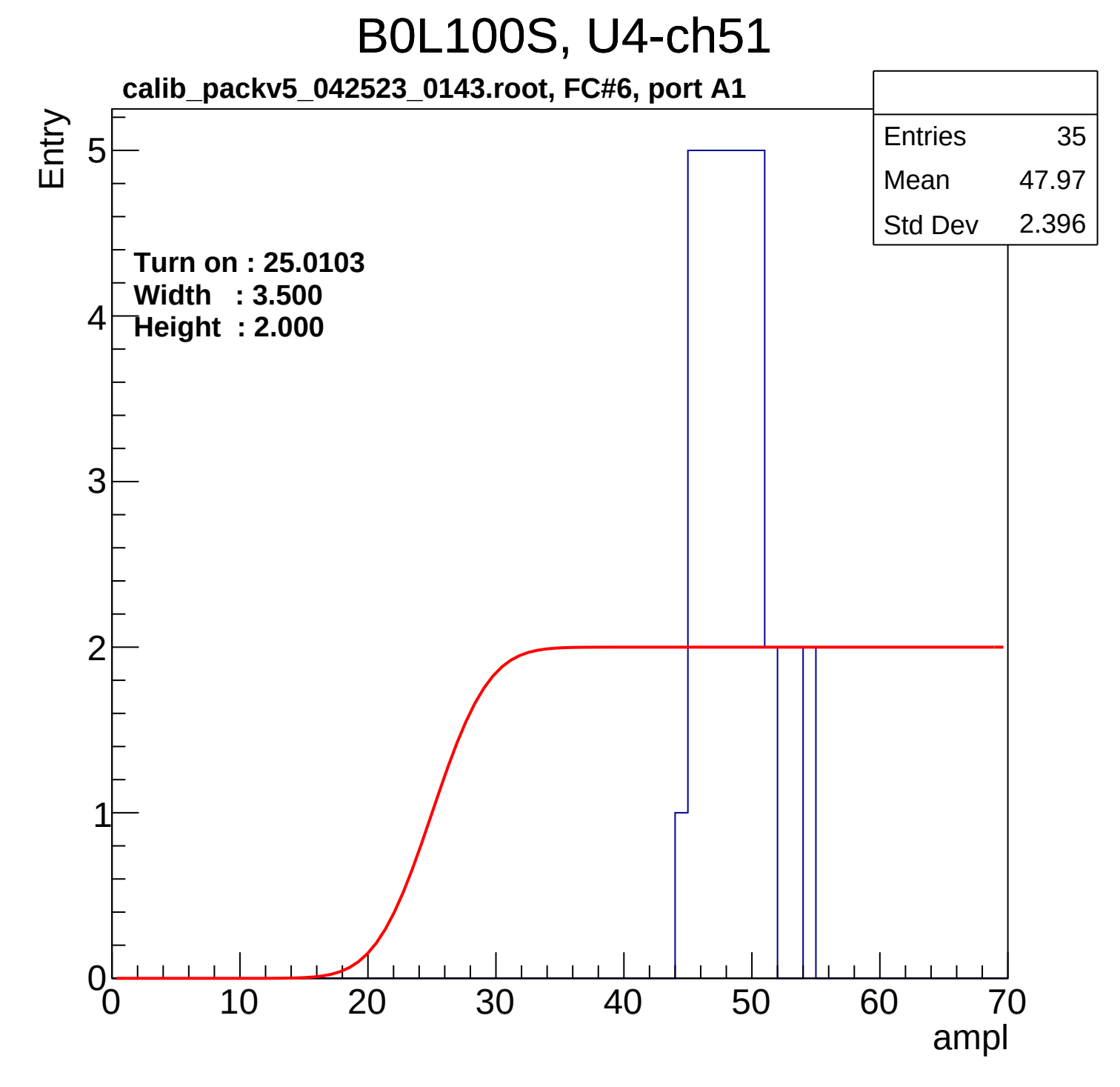

B0L100S, U4-ch46
calib_packv5_042523_0143.root, FC#6, port A1
Entries 15
Mean 46
Std Dev 0.8165
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

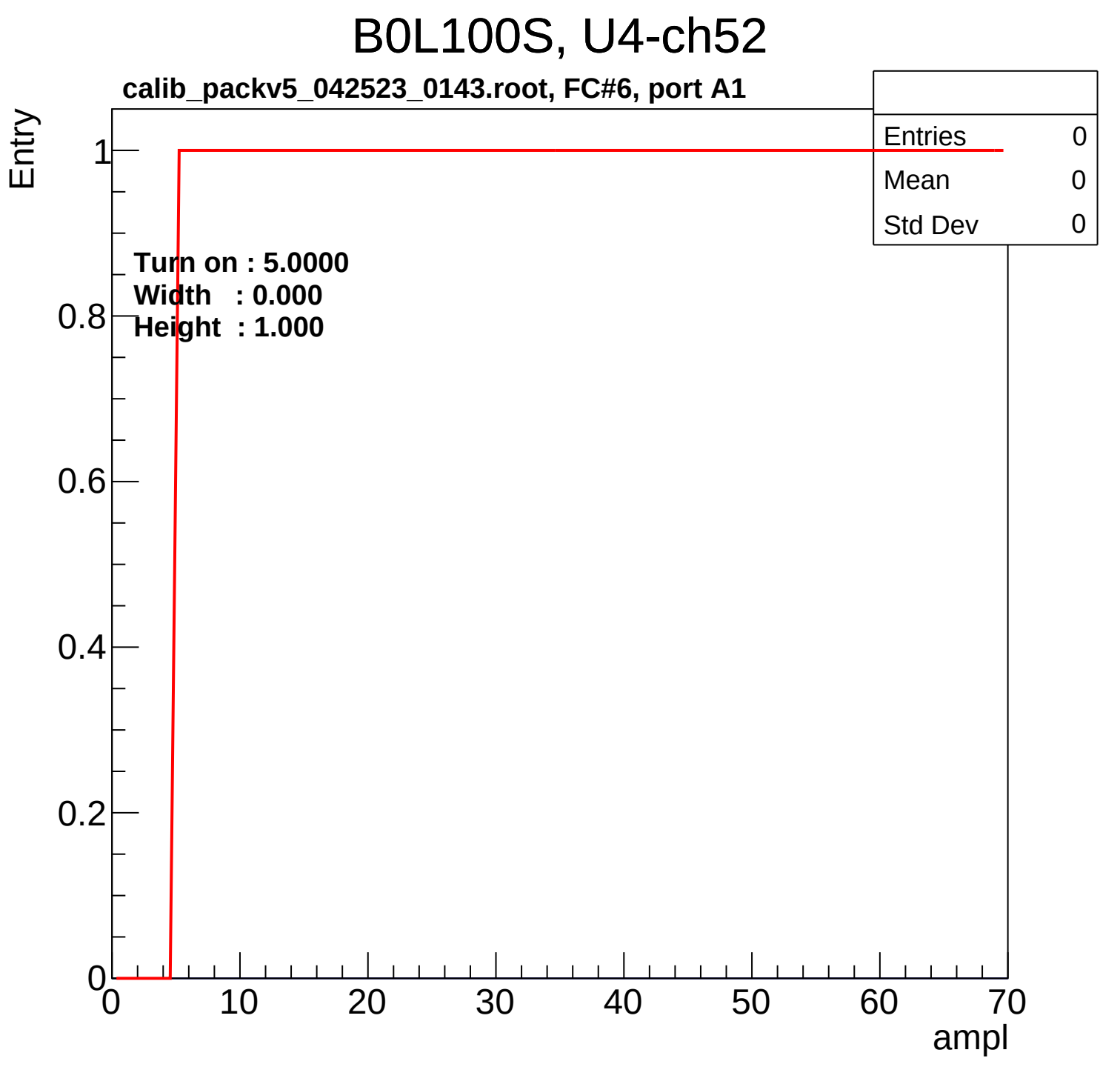

B0L100S, U4-ch47
calib_packv5_042523_0143.root, FC#6, port A1
Entries 60
Mean 44.75
Std Dev 9.08
Turn on : 40.5129
Width : 0.197
Height : 2.111
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

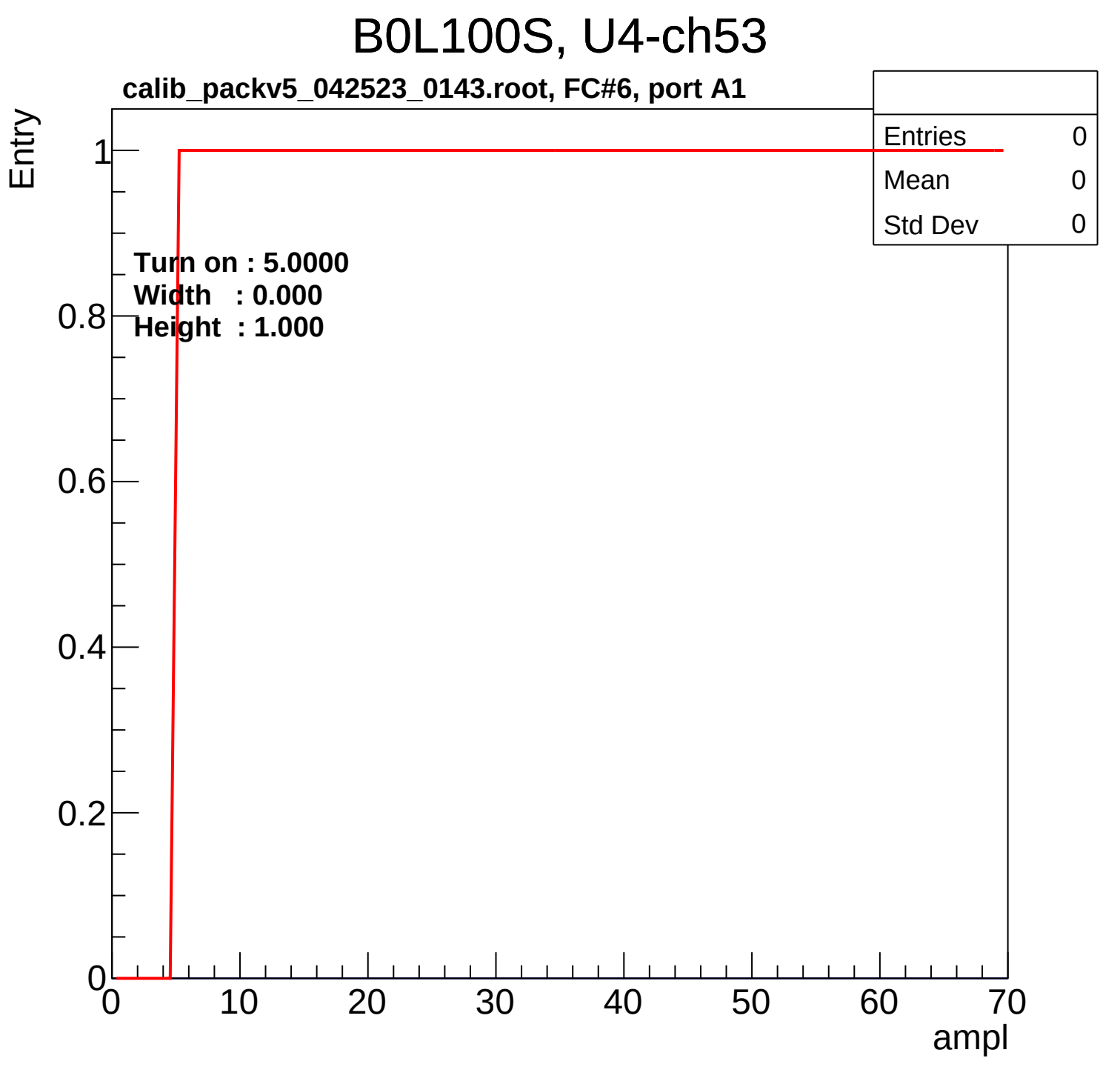

B0L100S, U4-ch48
calib_packv5_042523_0143.root, FC#6, port A1
Entries 5
Mean 16.8
Std Dev 20.58
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

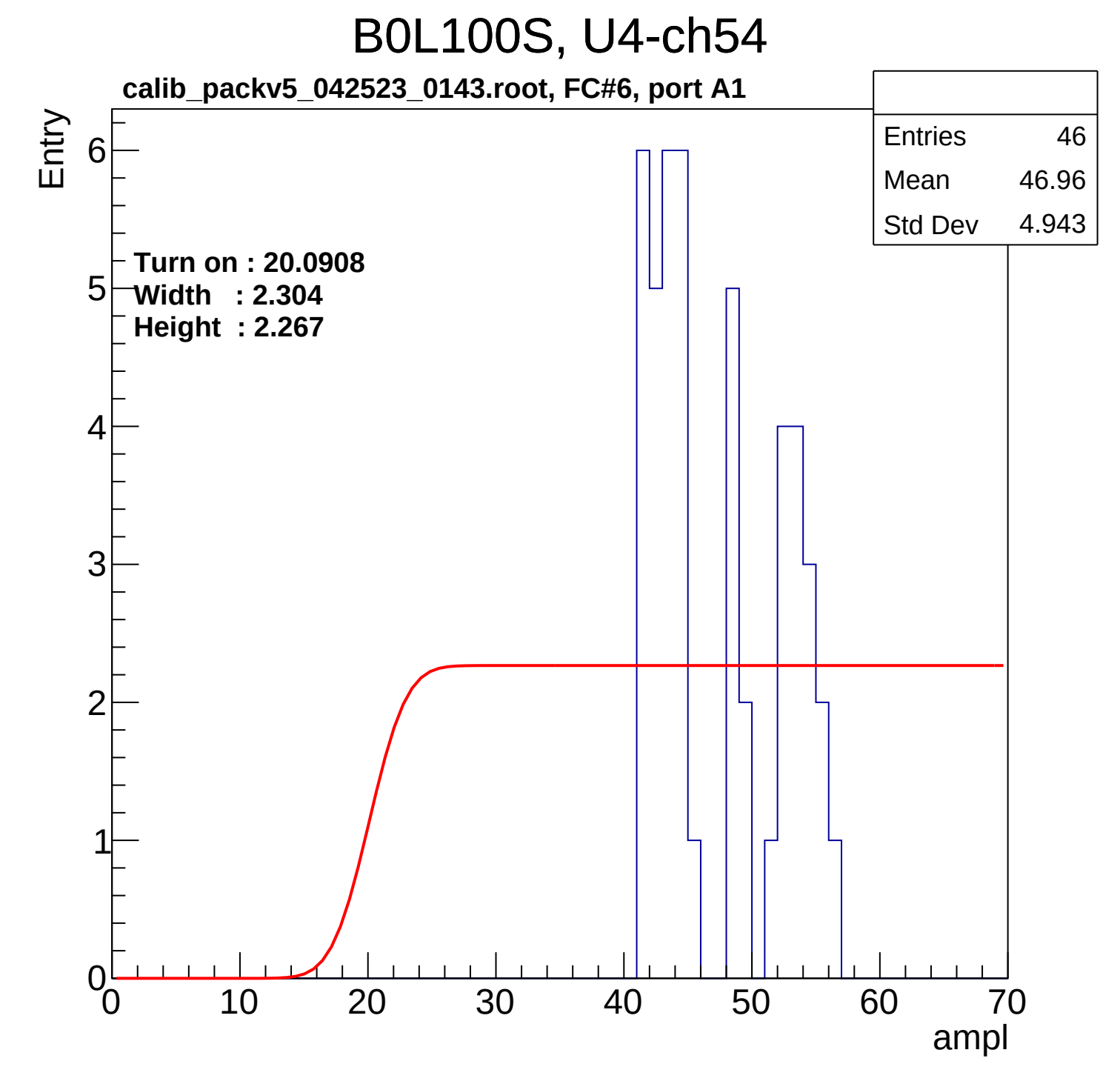

B0L100S, U4-ch49
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 52
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

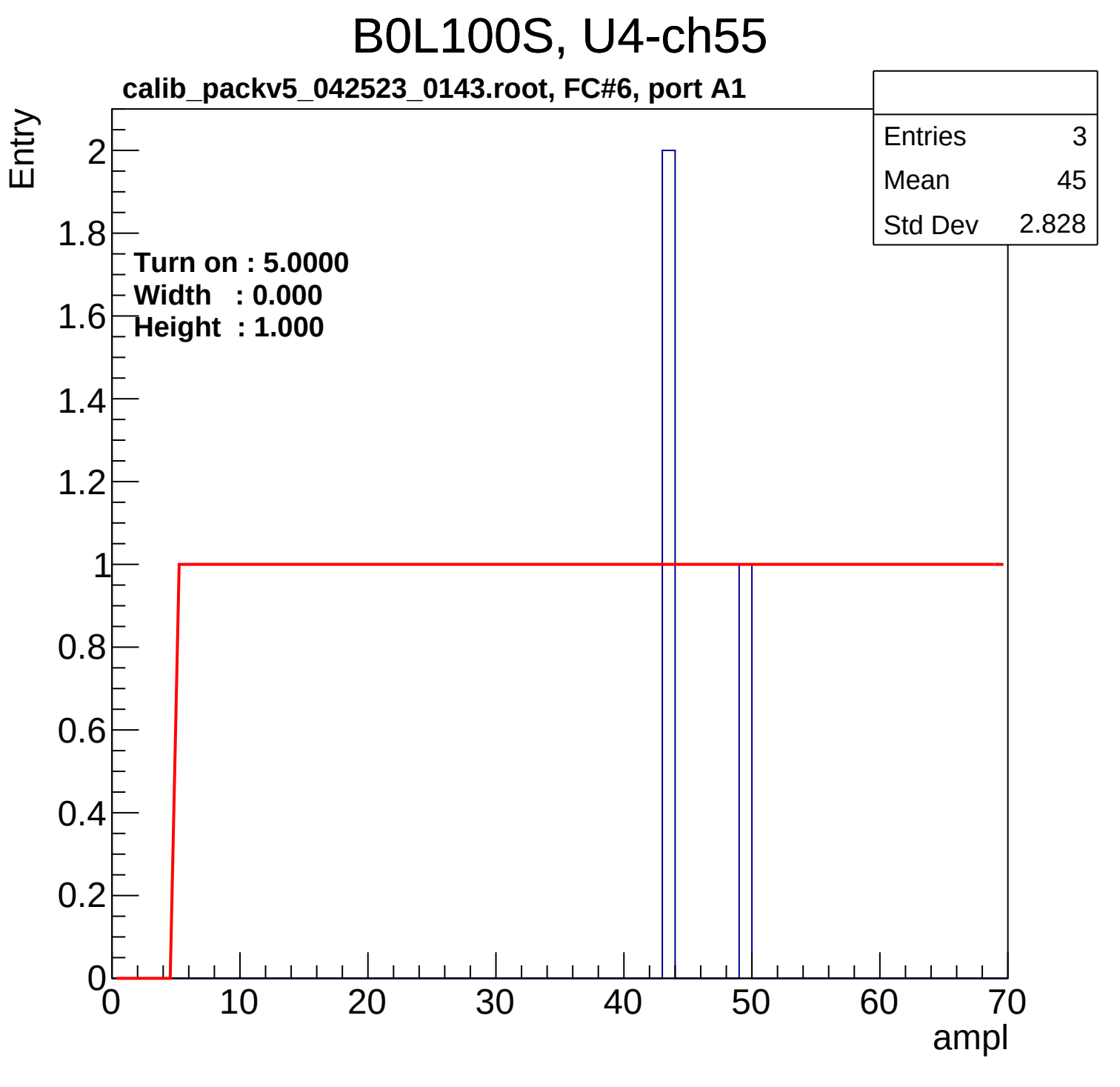

B0L100S, U4-ch50
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

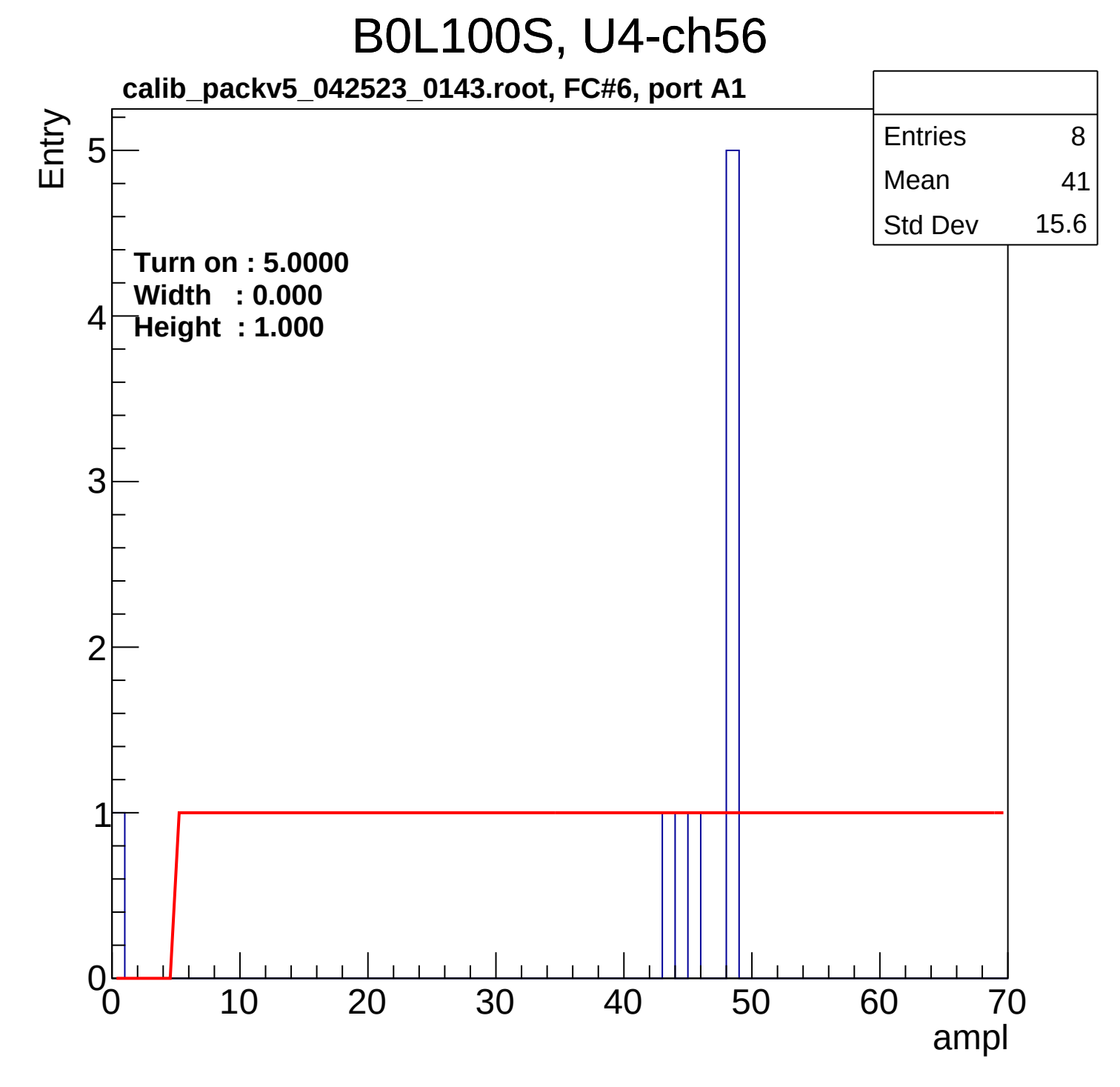

B0L100S, U4-ch51
calib_packv5_042523_0143.root, FC#6, port A1
Entries 35
Mean 47.97
Std Dev 2.396
Turn on : 25.0103
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

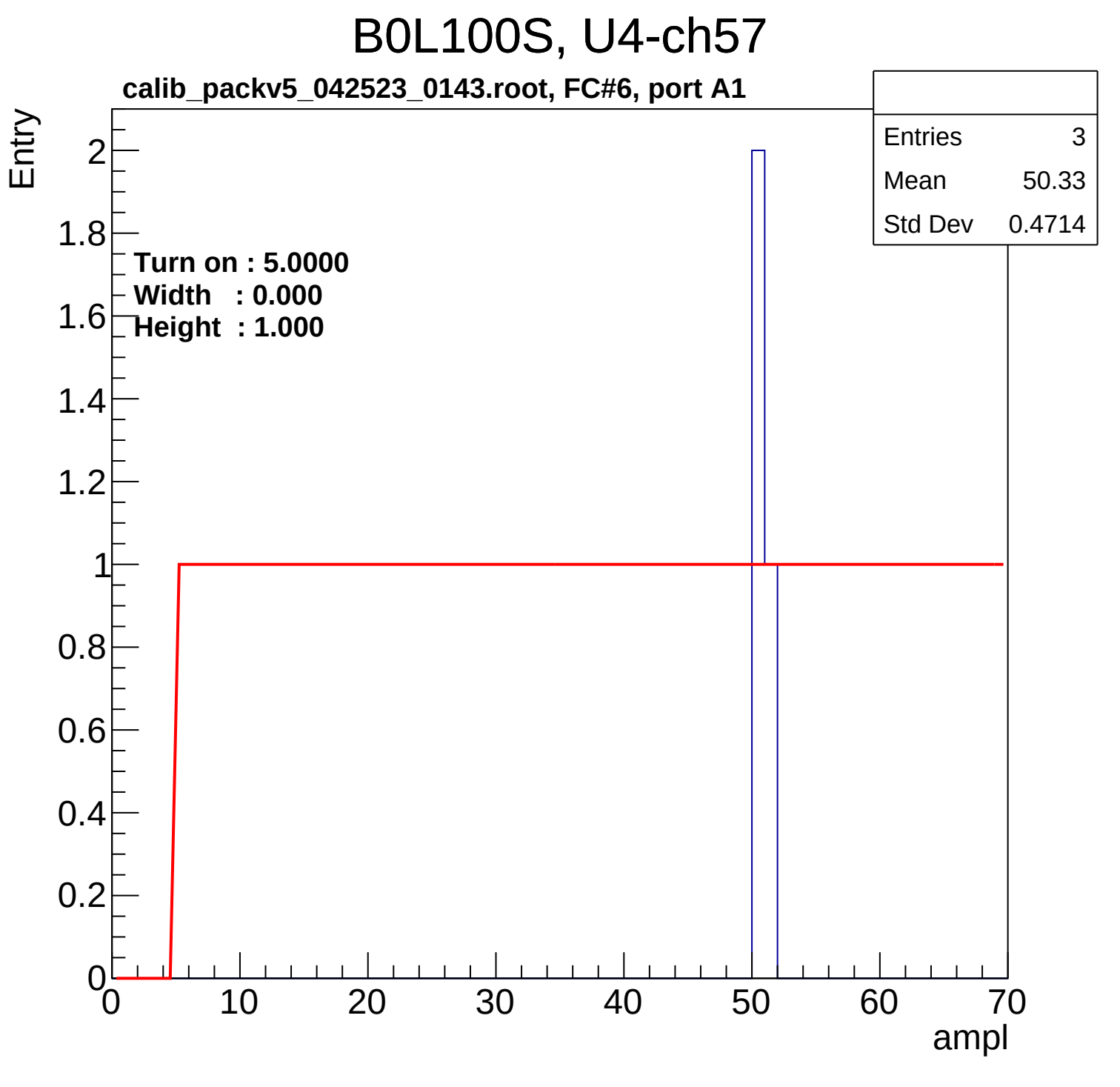

B0L100S, U4-ch52
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

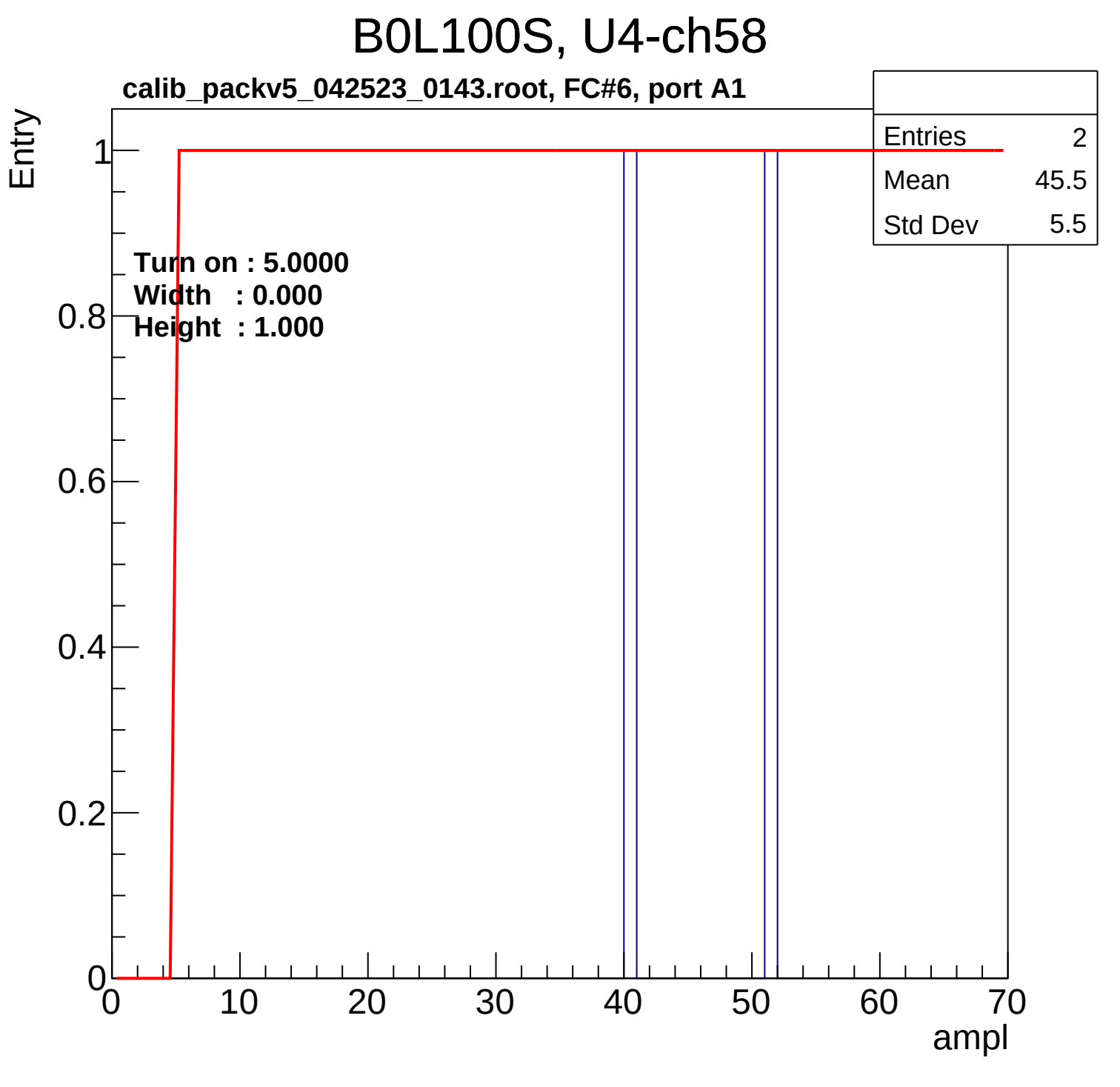

B0L100S, U4-ch53
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U4-ch54
calib_packv5_042523_0143.root, FC#6, port A1
Entries 46
Mean 46.96
Std Dev 4.943
Turn on : 20.0908
Width : 2.304
Height : 2.267
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B0L100S, U4-ch55
calib_packv5_042523_0143.root, FC#6, port A1
Entries 3
Mean 45
Std Dev 2.828
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L100S, U4-ch56
calib_packv5_042523_0143.root, FC#6, port A1
Entries 8
Mean 41
Std Dev 15.6
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U4-ch57
calib_packv5_042523_0143.root, FC#6, port A1
Entries 3
Mean 50.33
Std Dev 0.4714
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L100S, U4-ch58
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 45.5
Std Dev 5.5
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
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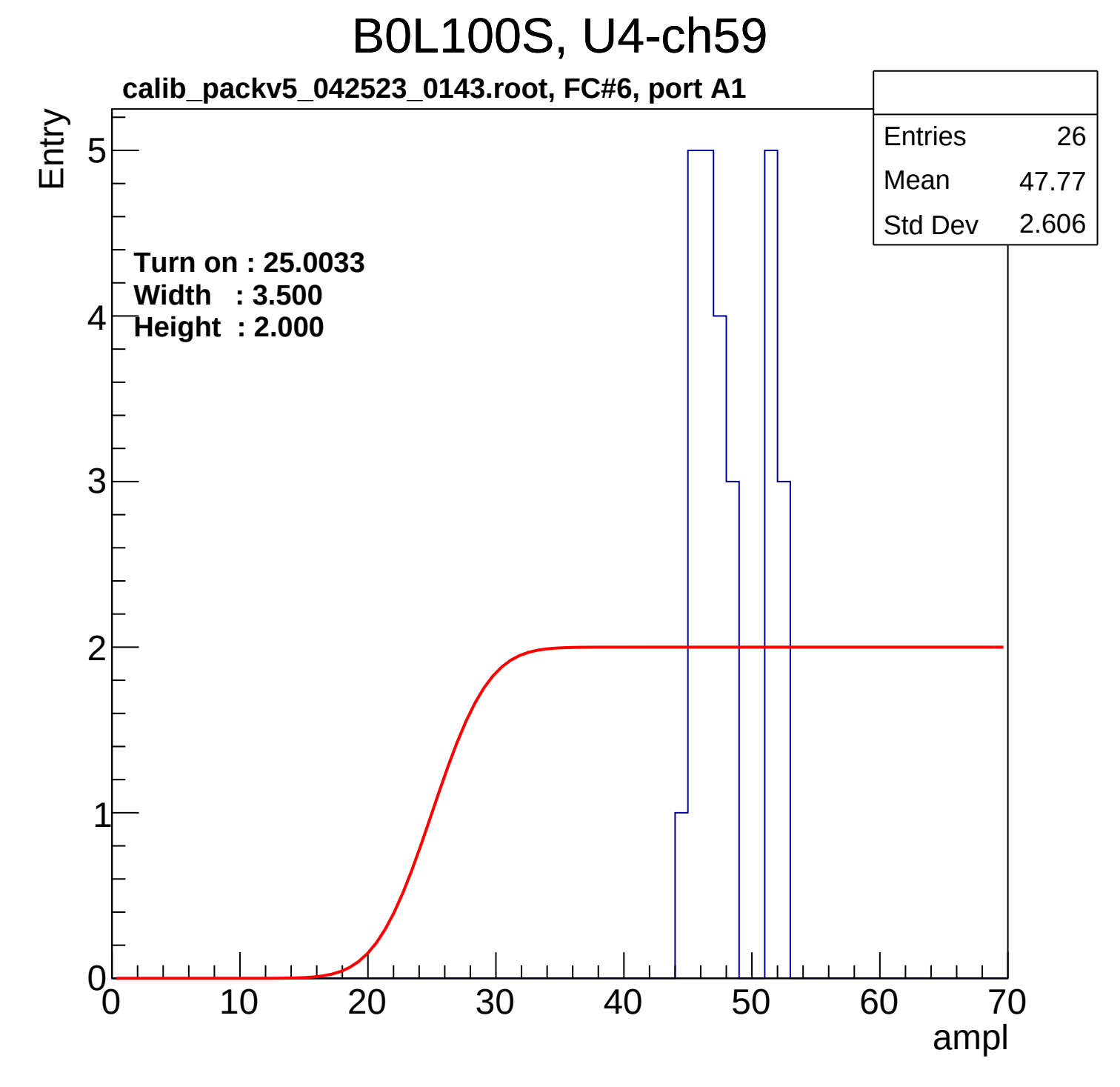
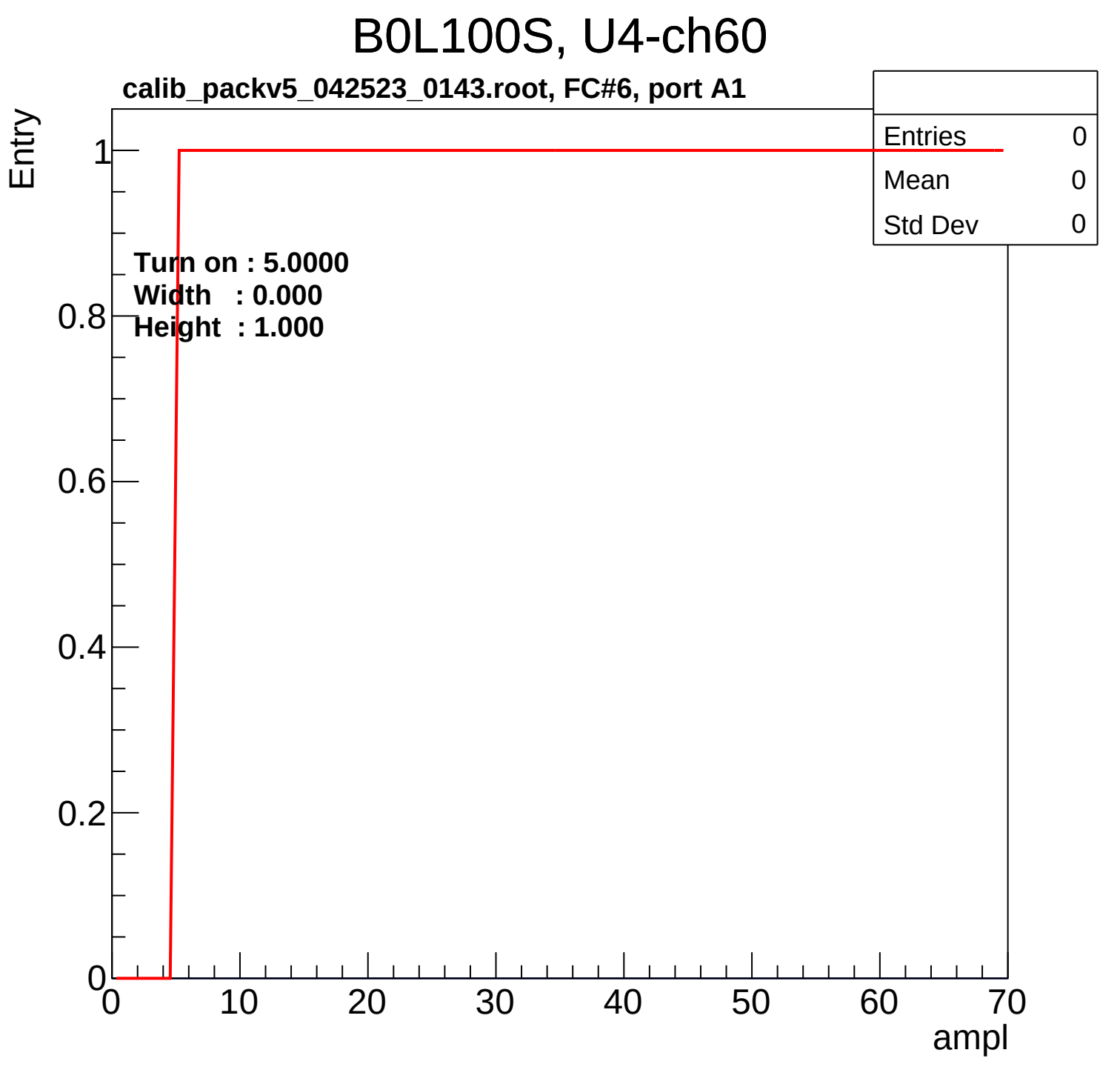
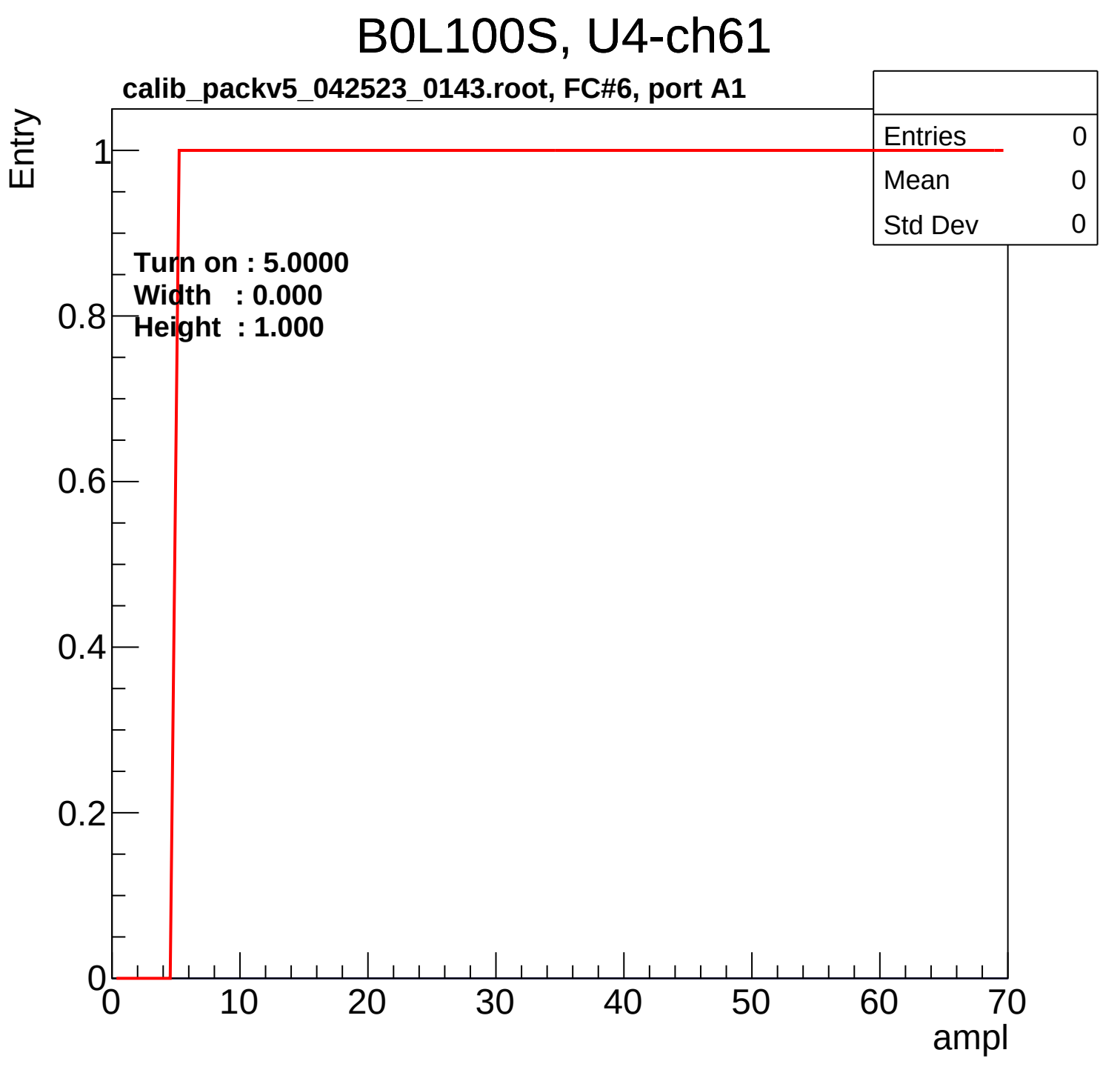
40
50
60
70


B0L100S, U4-ch59
calib_packv5_042523_0143.root, FC#6, port A1
Entries 26
Mean 47.77
Std Dev 2.606
Turn on : 25.0033
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U4-ch60
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U4-ch61
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
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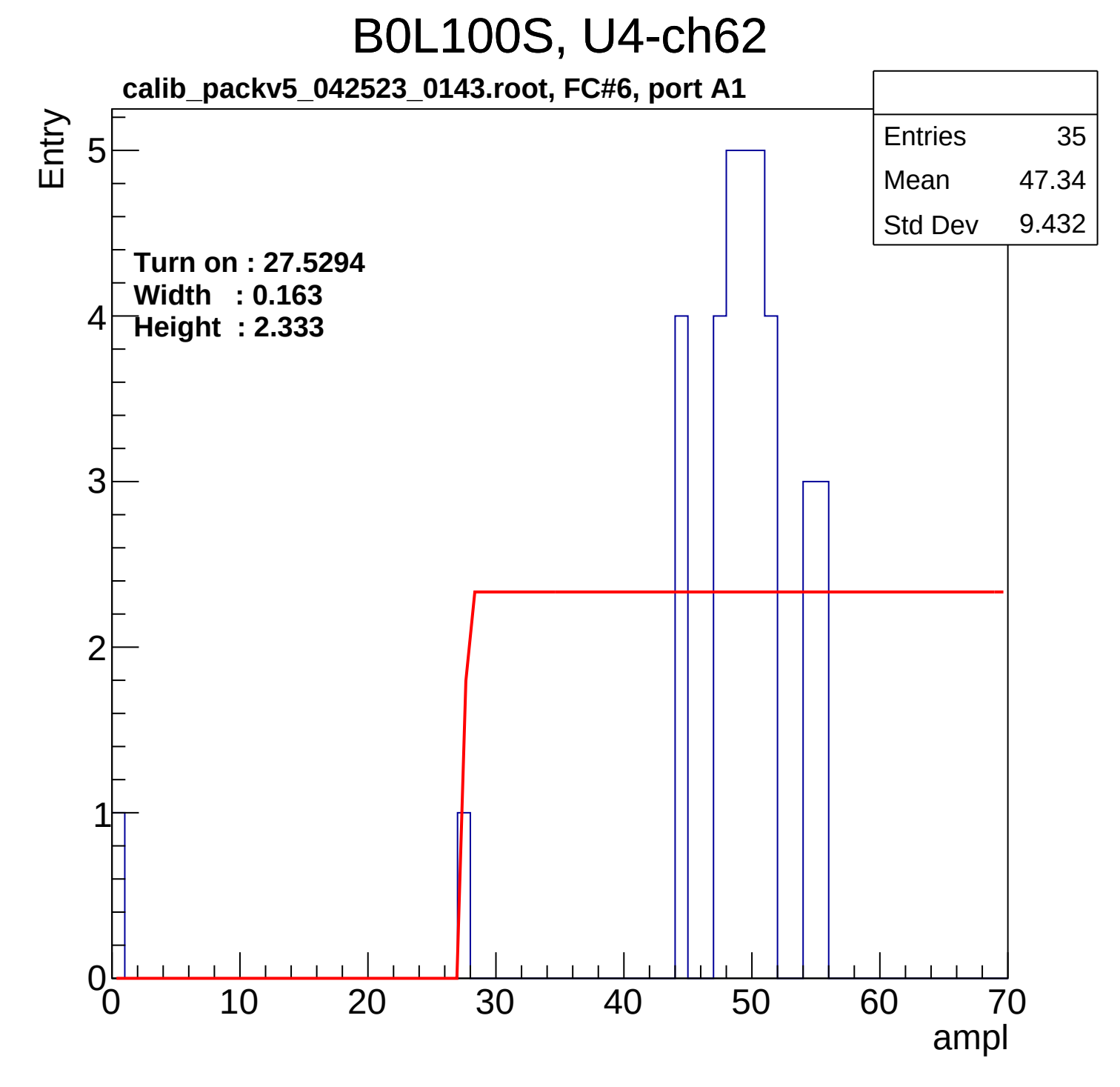
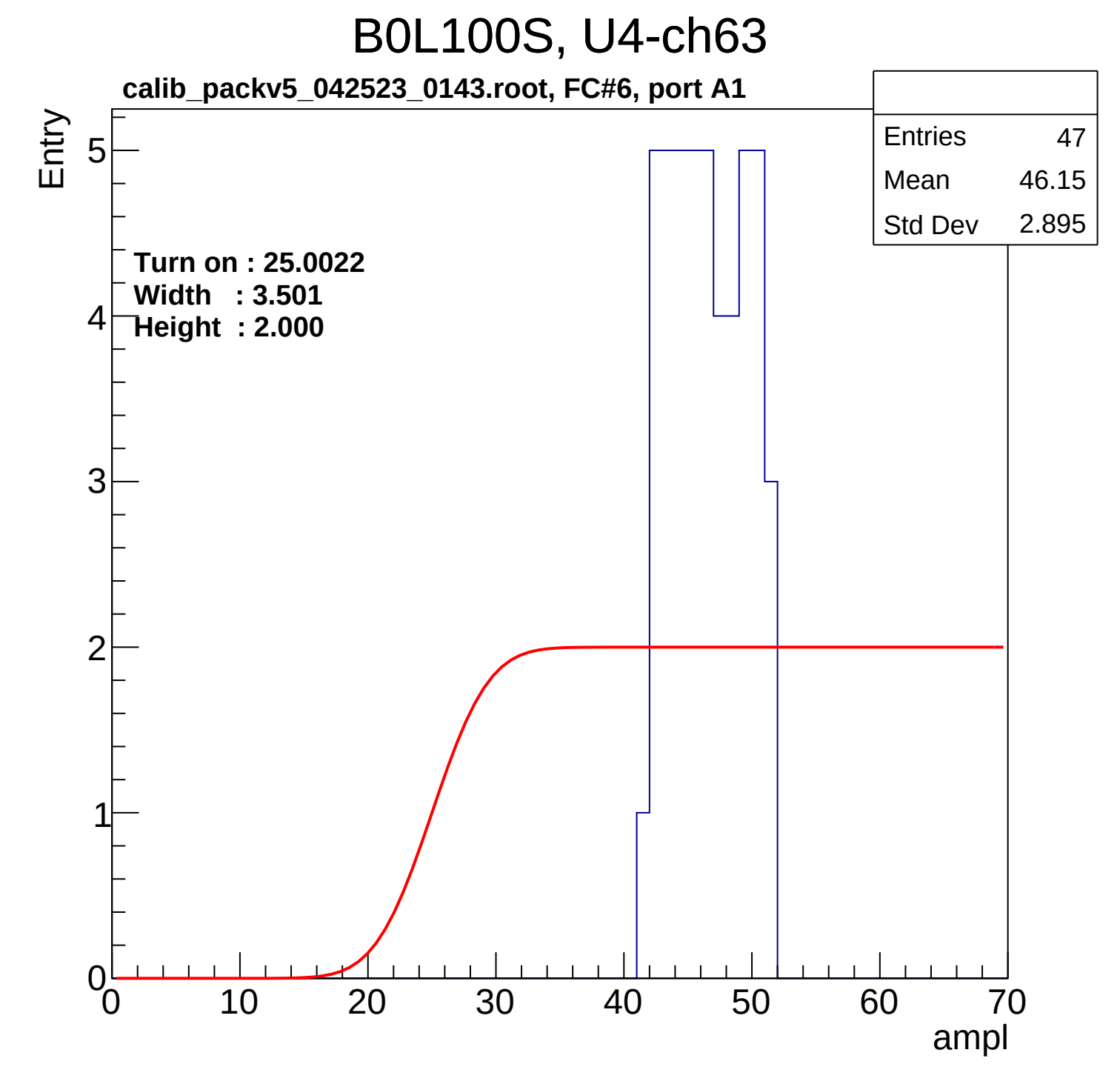
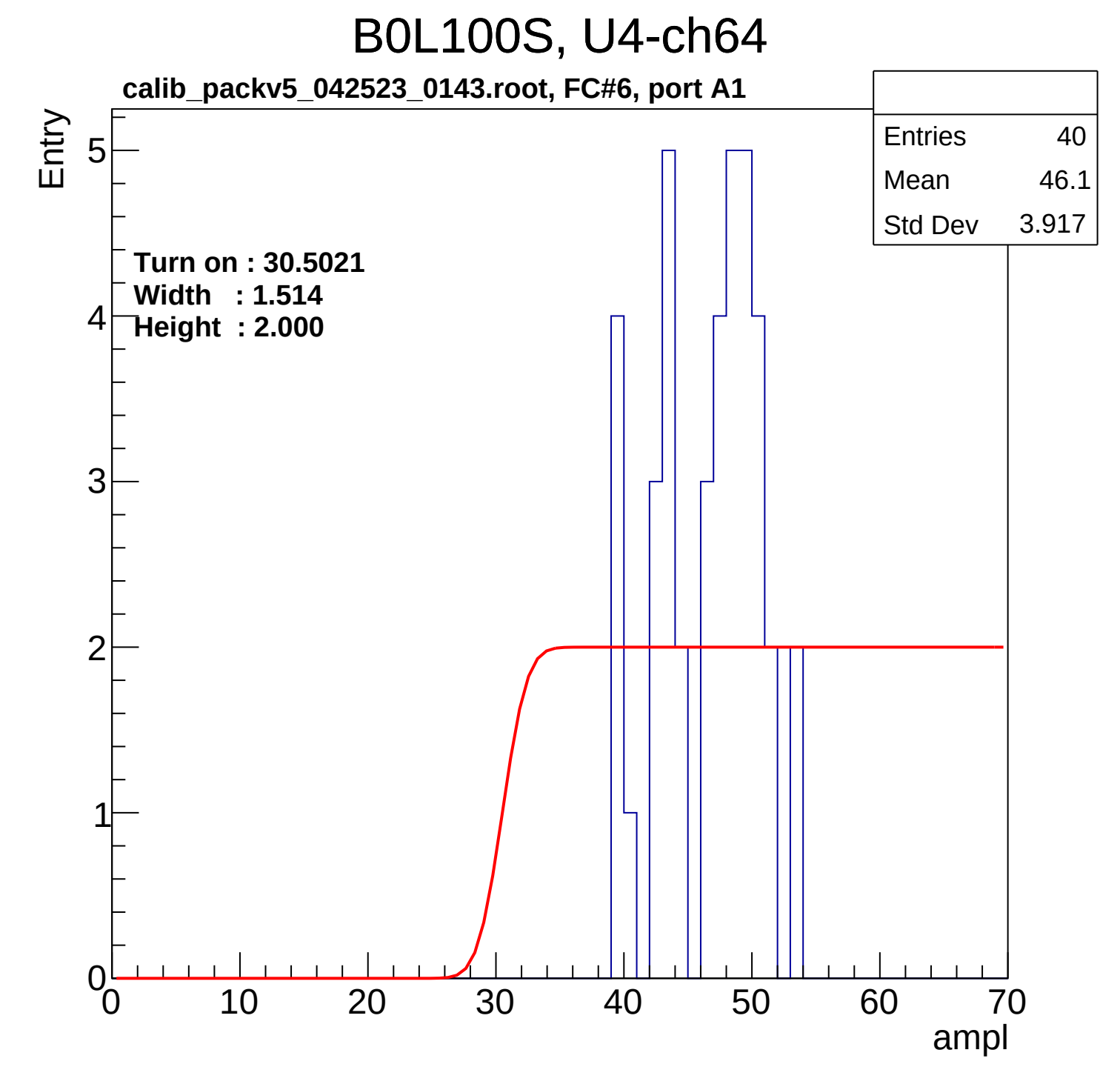
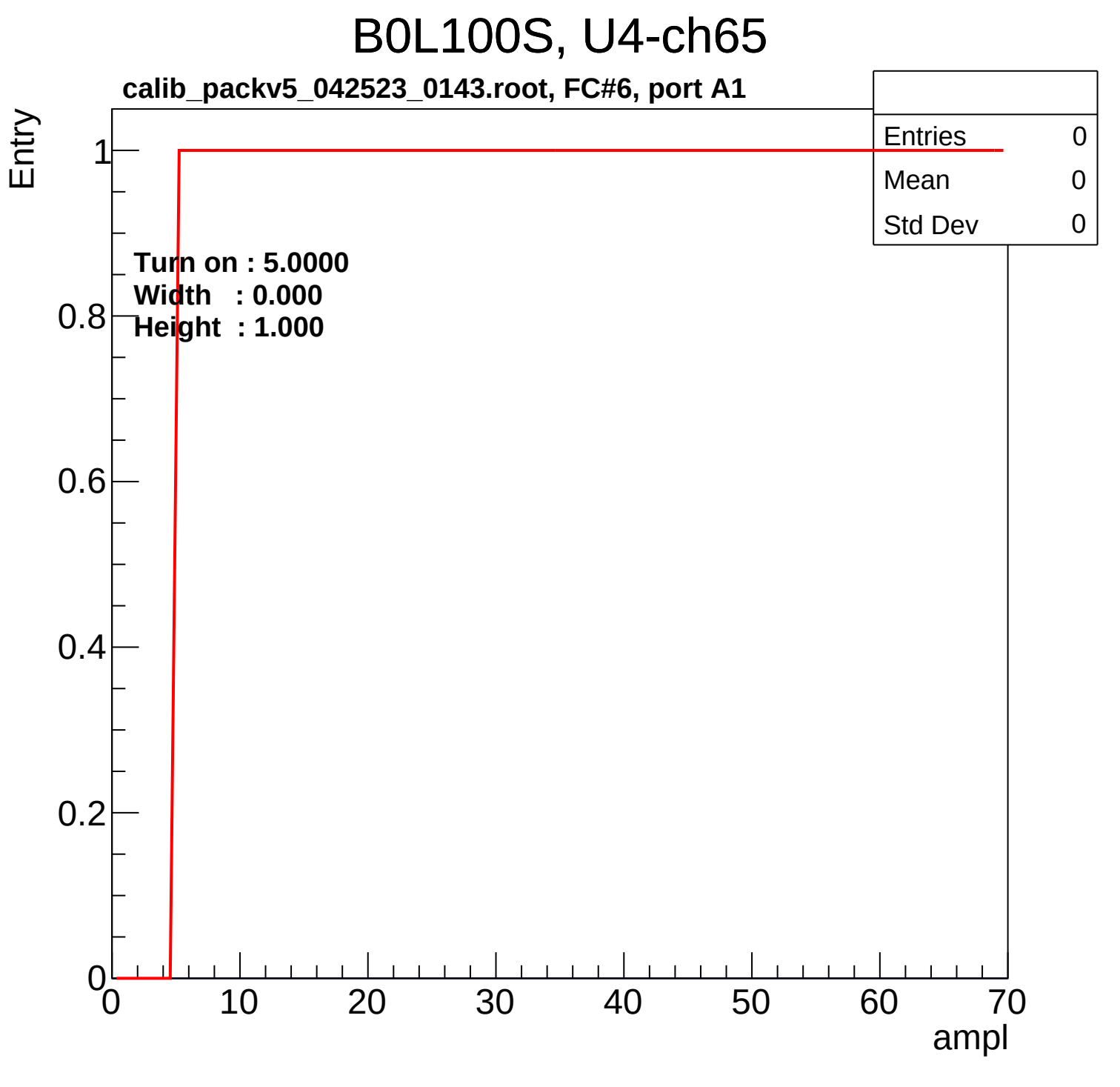
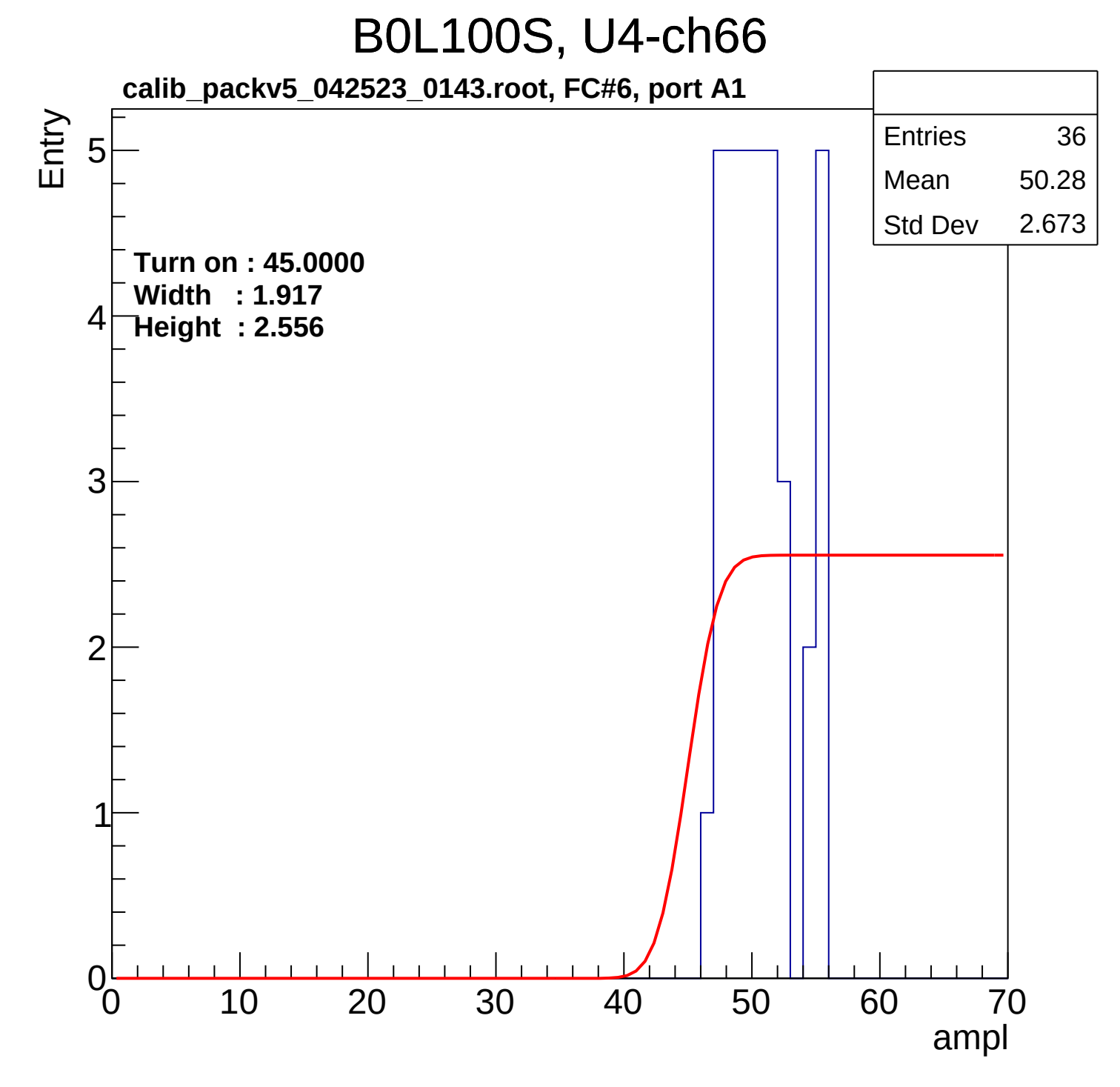
50
60
70
ampl

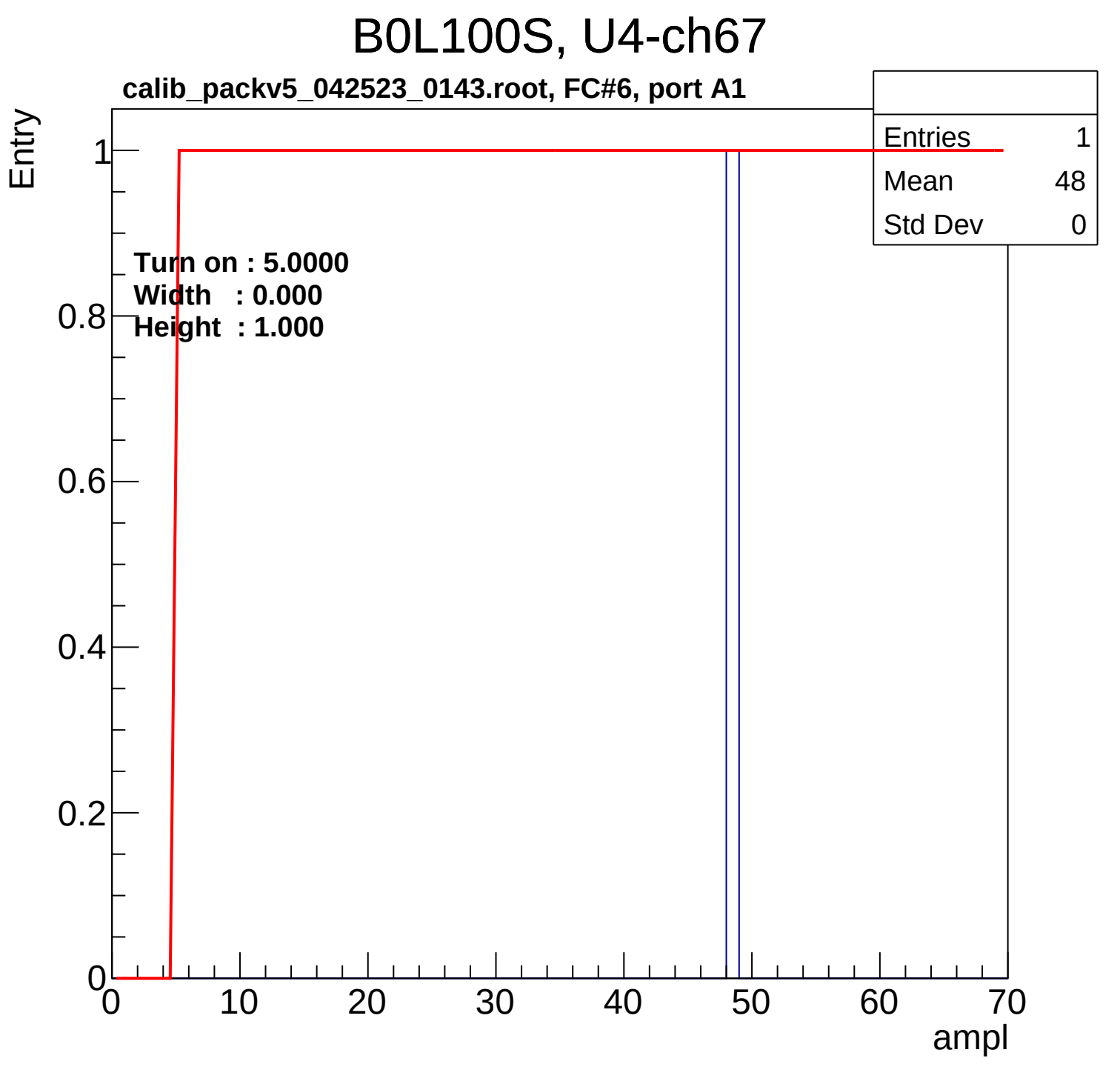

B0L100S, U4-ch62
calib_packv5_042523_0143.root, FC#6, port A1
Entries 35
Mean 47.34
Std Dev 9.432
Turn on : 27.5294
Width : 0.163
Height : 2.333
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

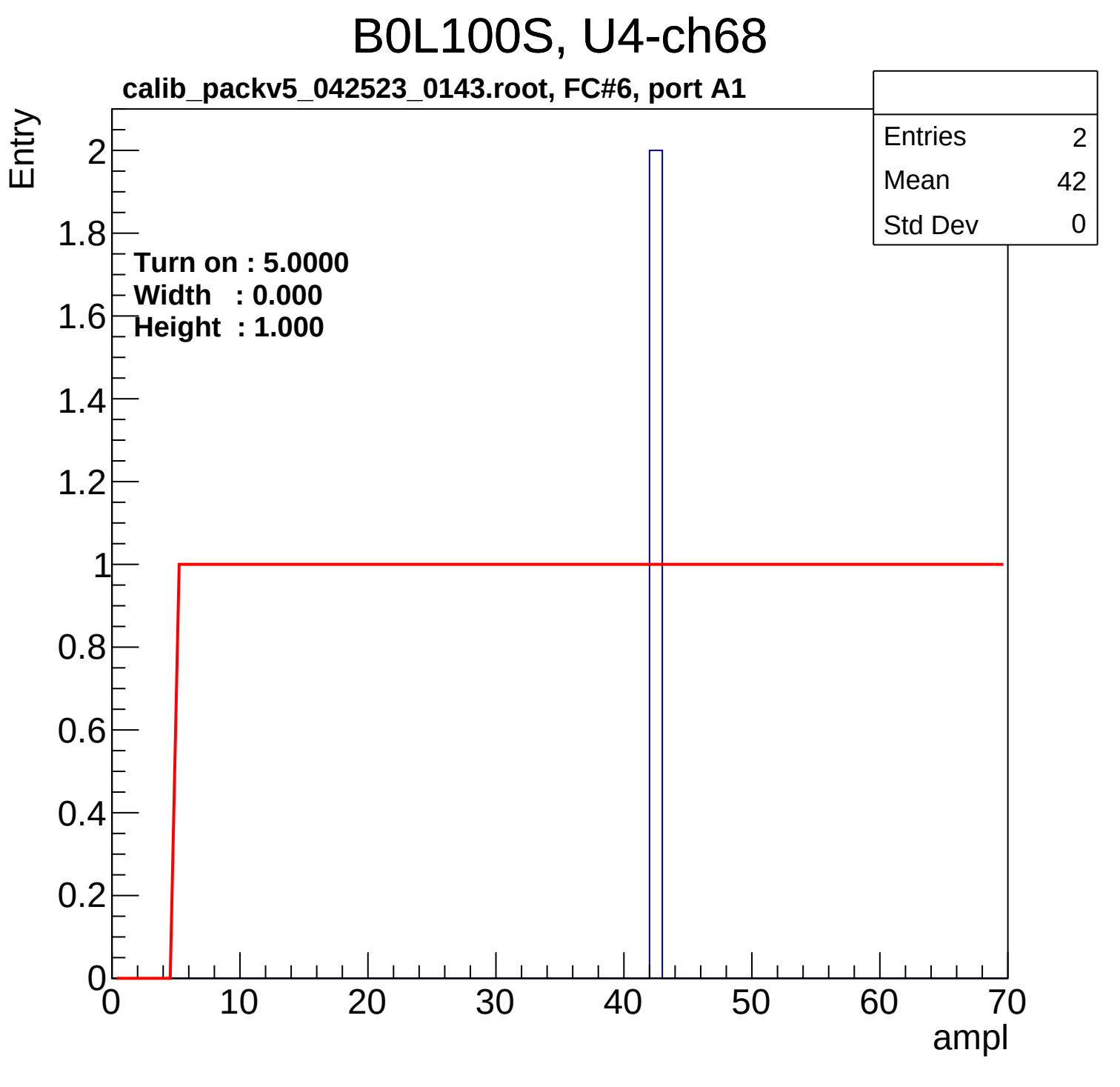

B0L100S, U4-ch63
calib_packv5_042523_0143.root, FC#6, port A1
Entries 47
Mean 46.15
Std Dev 2.895
Turn on : 25.0022
Width : 3.501
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

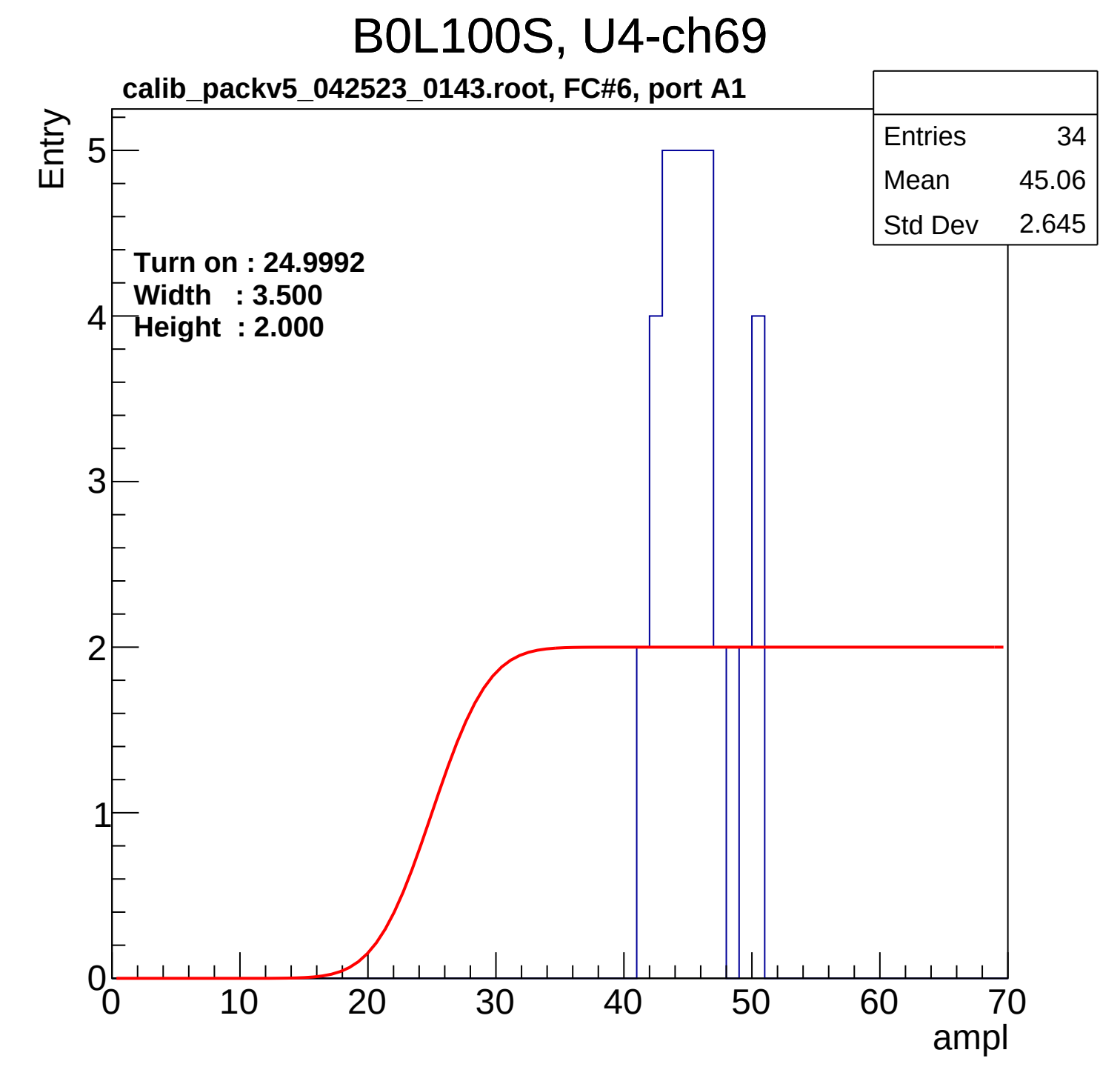

B0L100S, U4-ch64
calib_packv5_042523_0143.root, FC#6, port A1
Entries 40
Mean 46.1
Std Dev 3.917
Turn on : 30.5021
Width : 1.514
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

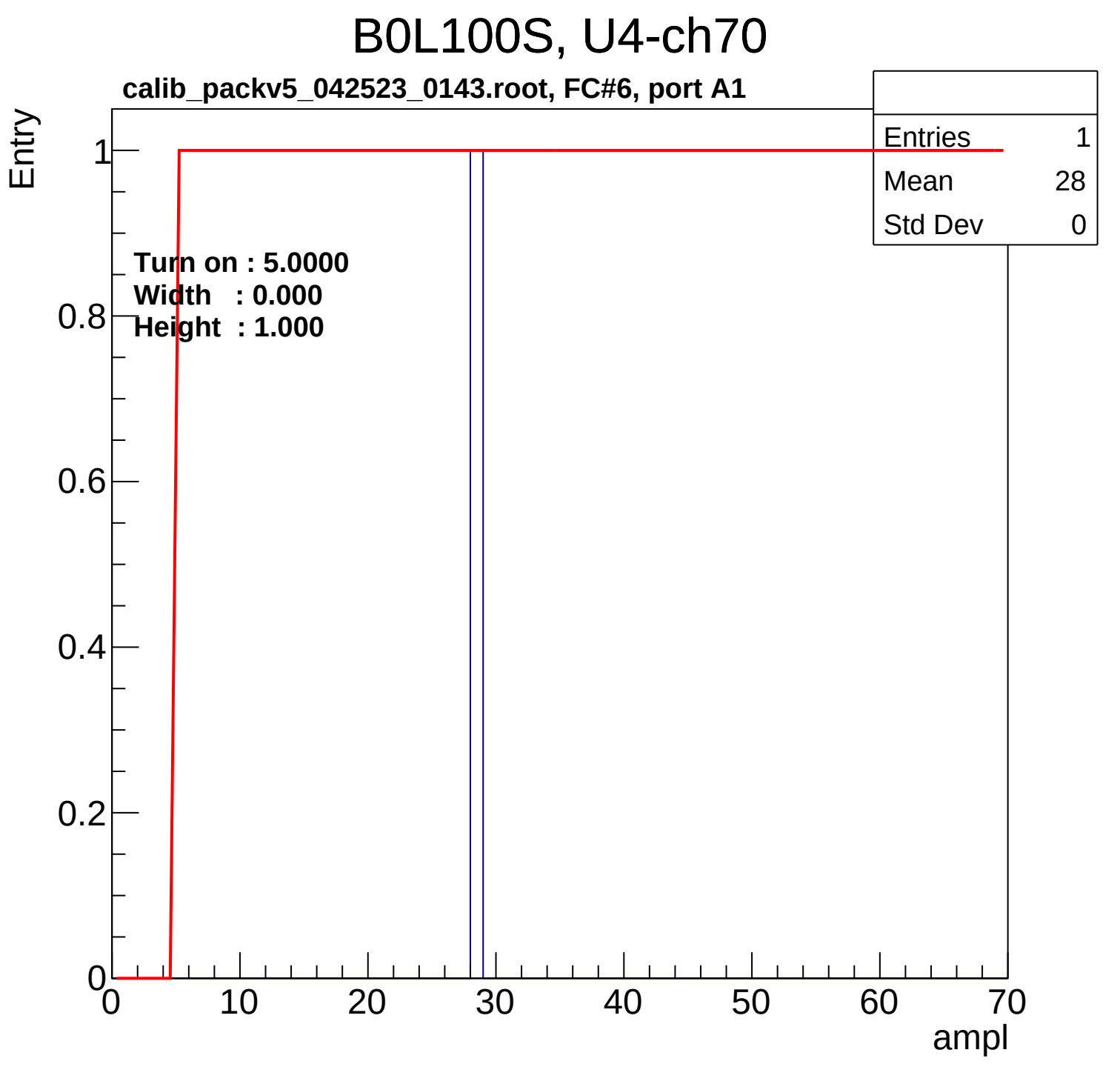

B0L100S, U4-ch65
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

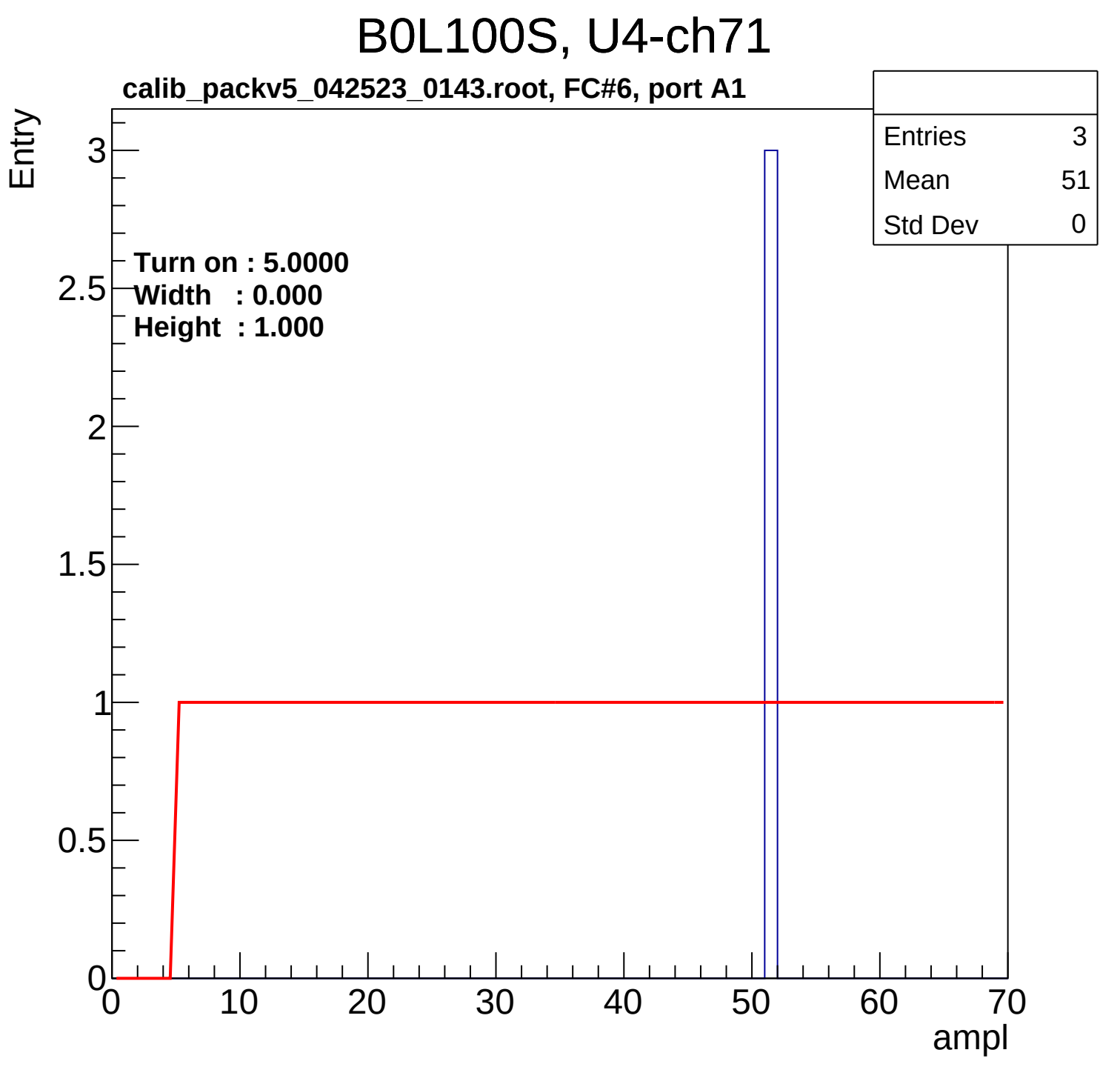

B0L100S, U4-ch66
calib_packv5_042523_0143.root, FC#6, port A1
Entries 36
Mean 50.28
Std Dev 2.673
Turn on : 45.0000
Width : 1.917
Height : 2.556
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

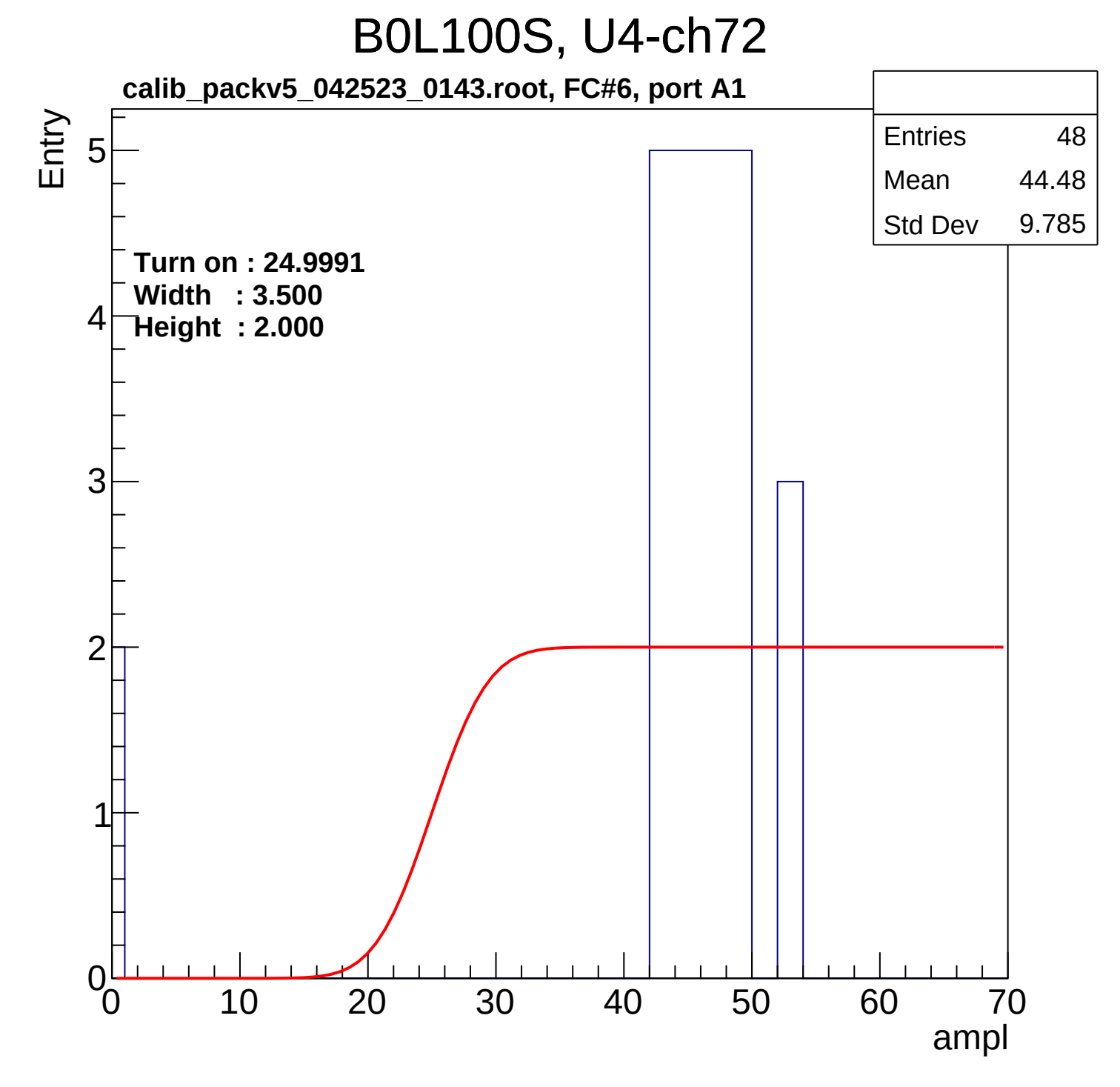

B0L100S, U4-ch67
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 48
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U4-ch68
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 42
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L100S, U4-ch69
calib_packv5_042523_0143.root, FC#6, port A1
Entries 34
Mean 45.06
Std Dev 2.645
Turn on : 24.9992
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U4-ch70
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 28
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U4-ch71
calib_packv5_042523_0143.root, FC#6, port A1
Entries 3
Mean 51
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B0L100S, U4-ch72
calib_packv5_042523_0143.root, FC#6, port A1
Entries 48
Mean 44.48
Std Dev 9.785
Turn on : 24.9991
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
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30
40
50
60
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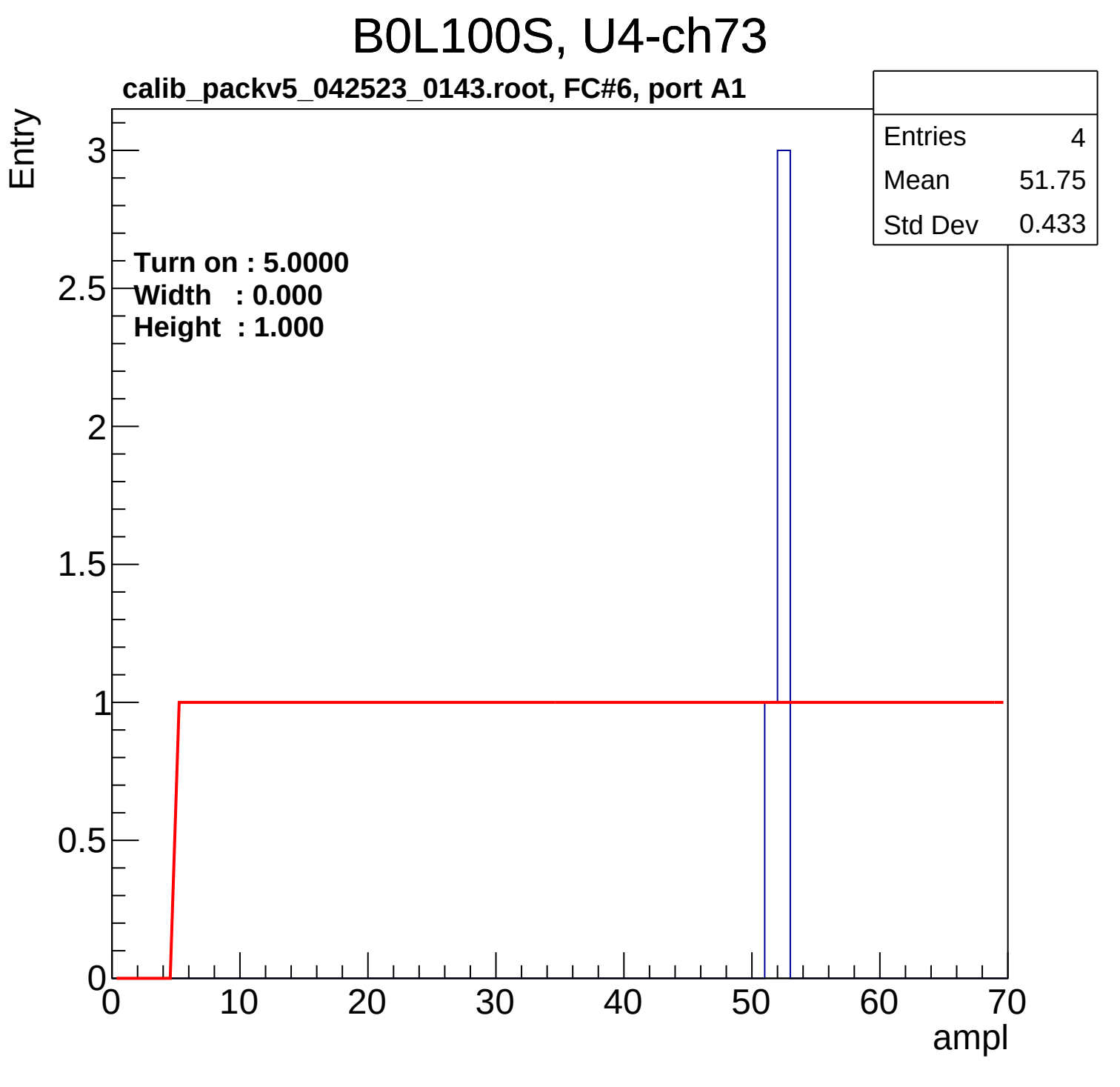
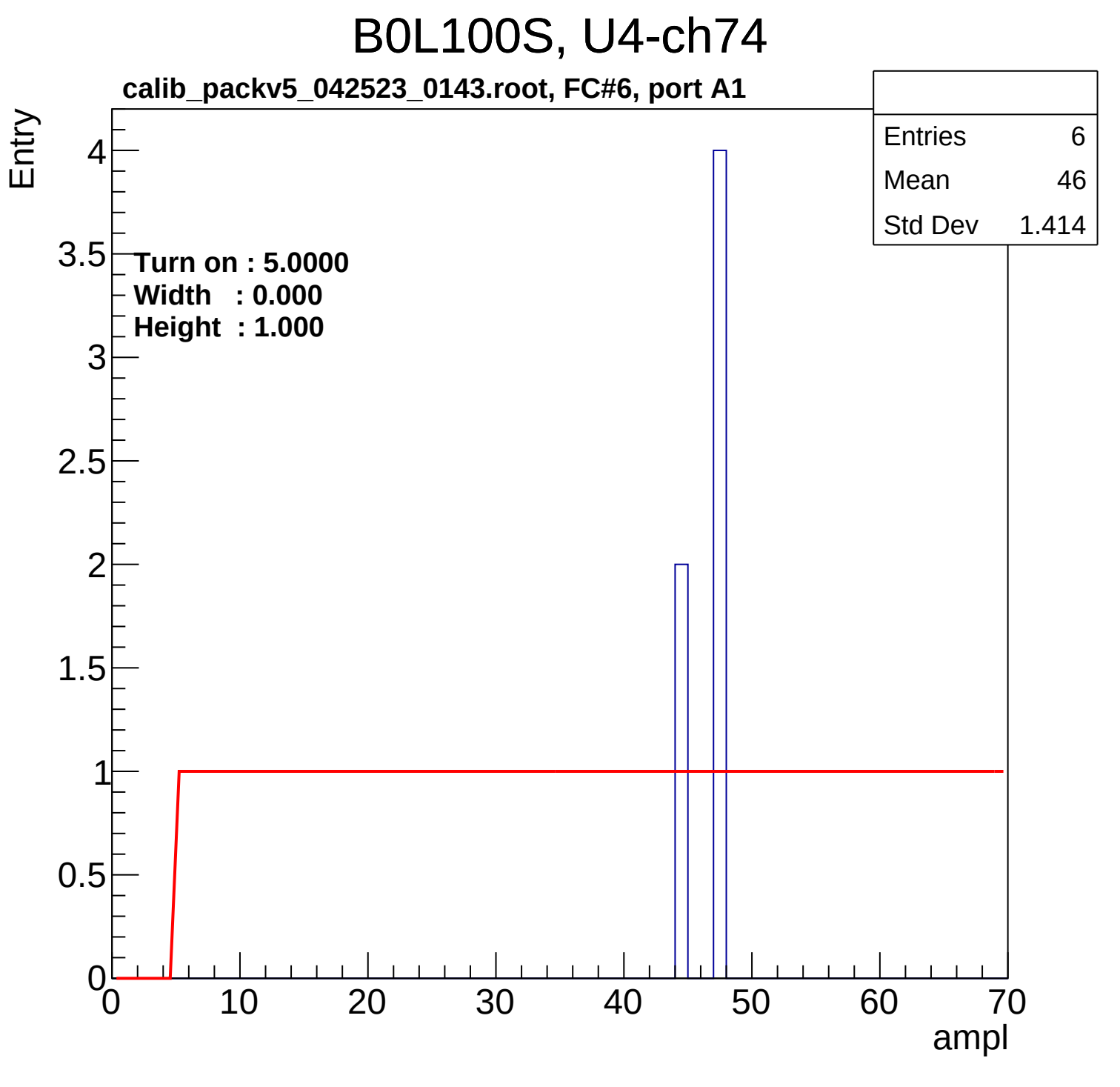
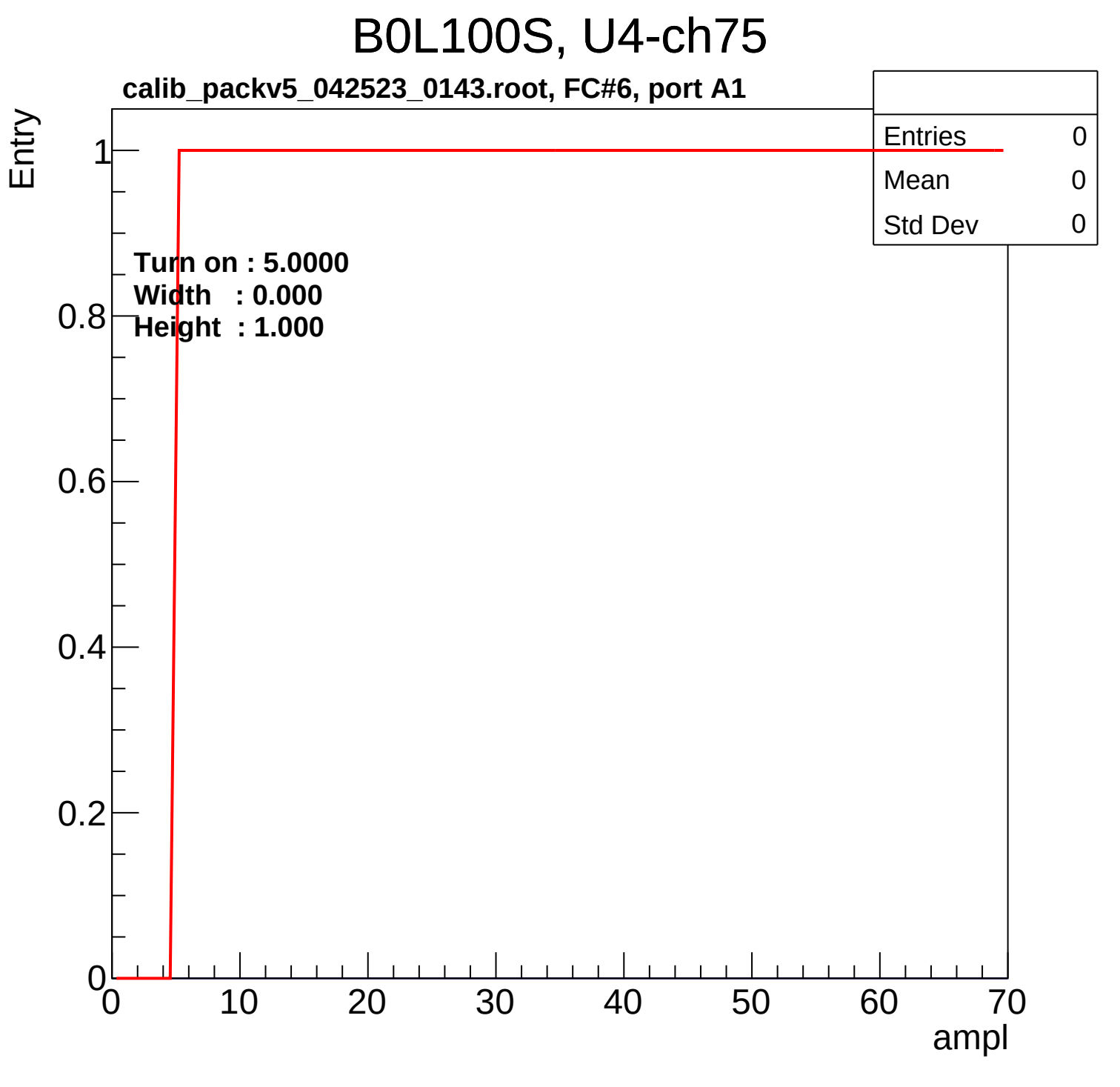
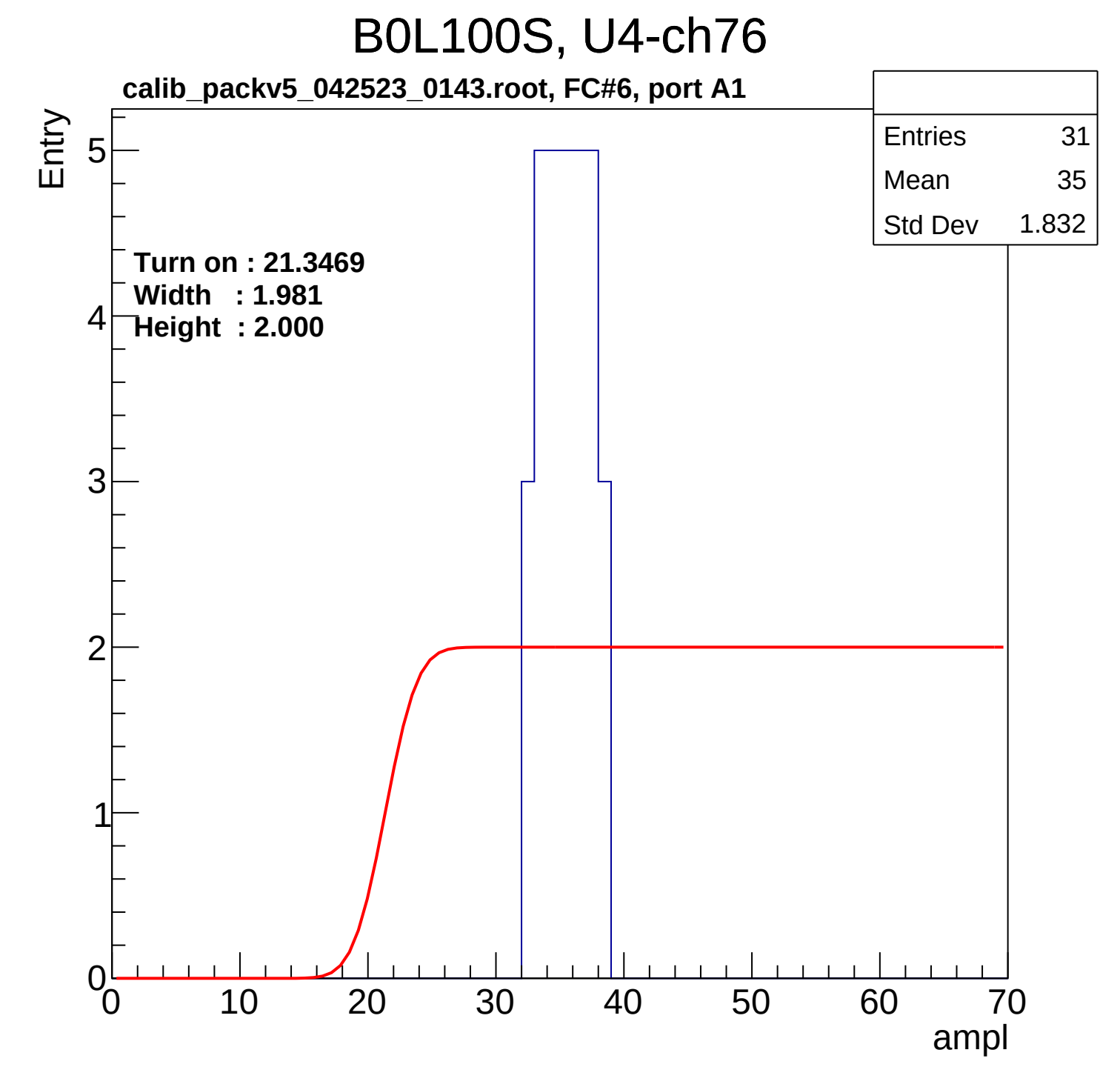

B0L100S, U4-ch73
calib_packv5_042523_0143.root, FC#6, port A1
Entries 4
Mean 51.75
Std Dev 0.433
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B0L100S, U4-ch74
calib_packv5_042523_0143.root, FC#6, port A1
Entries 6
Mean 46
Std Dev 1.414
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B0L100S, U4-ch75
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U4-ch76
calib_packv5_042523_0143.root, FC#6, port A1
Entries 31
Mean 35
Std Dev 1.832
Turn on : 21.3469
Width : 1.981
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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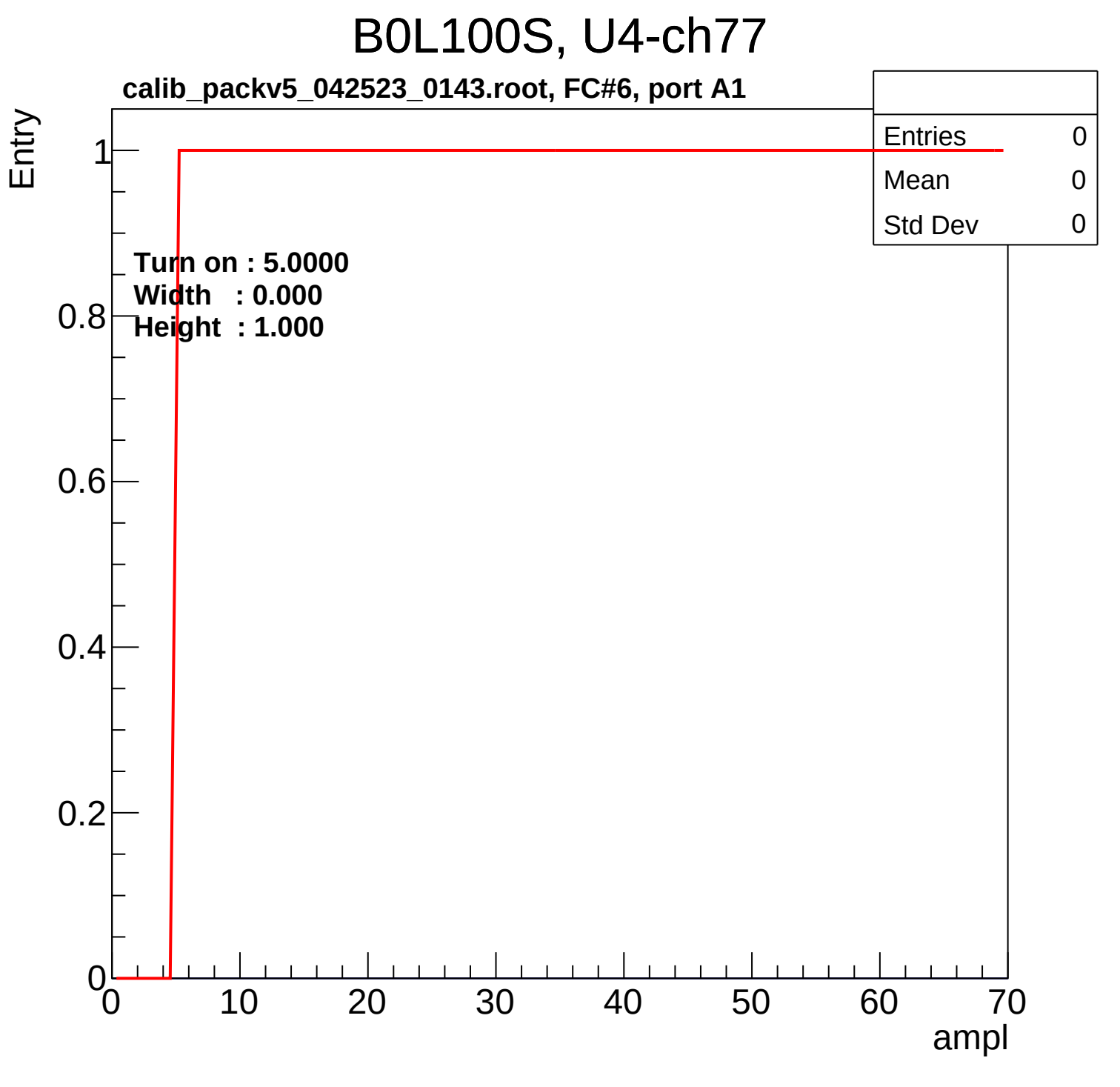
B0L100S, U4-ch77
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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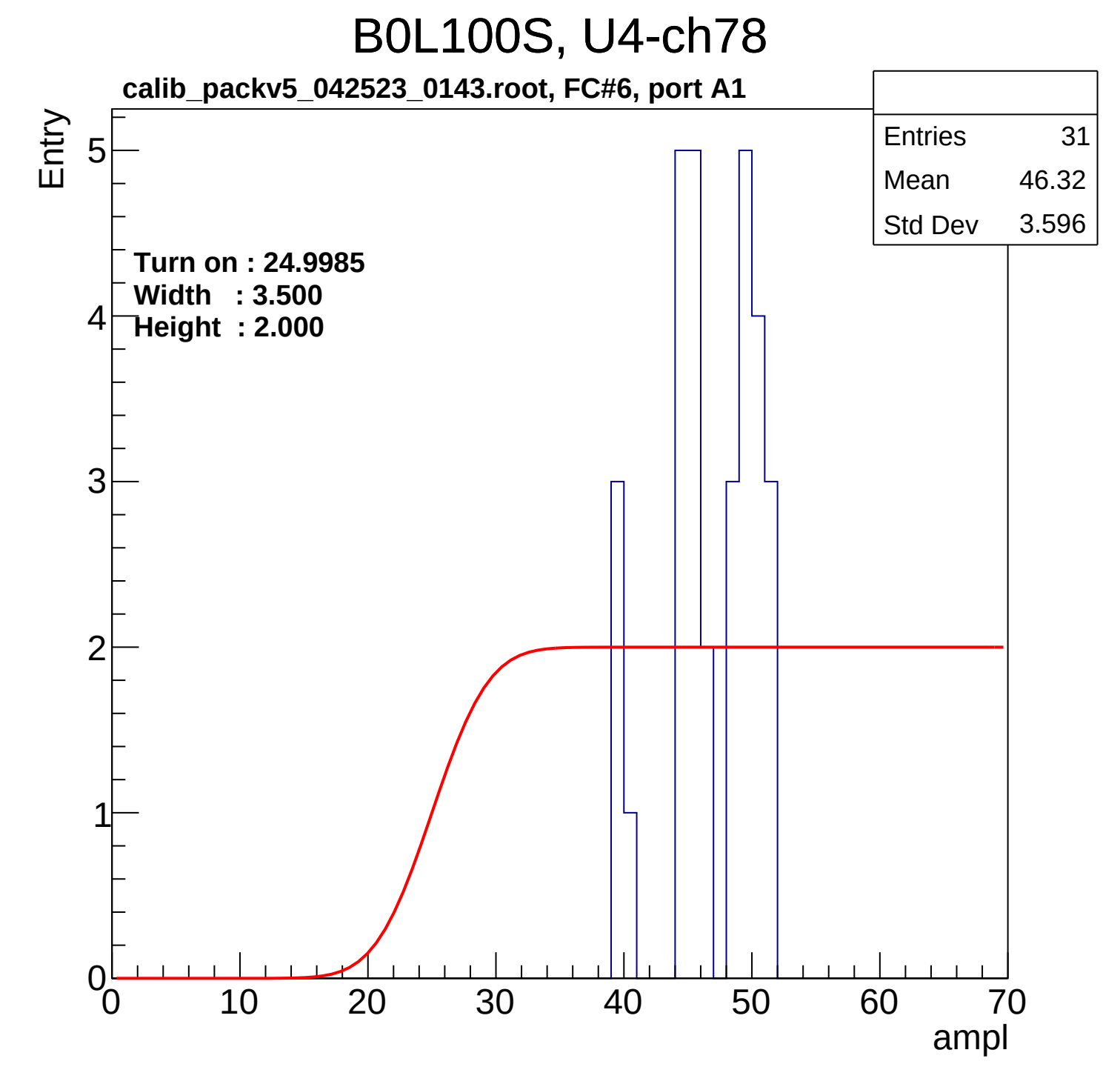
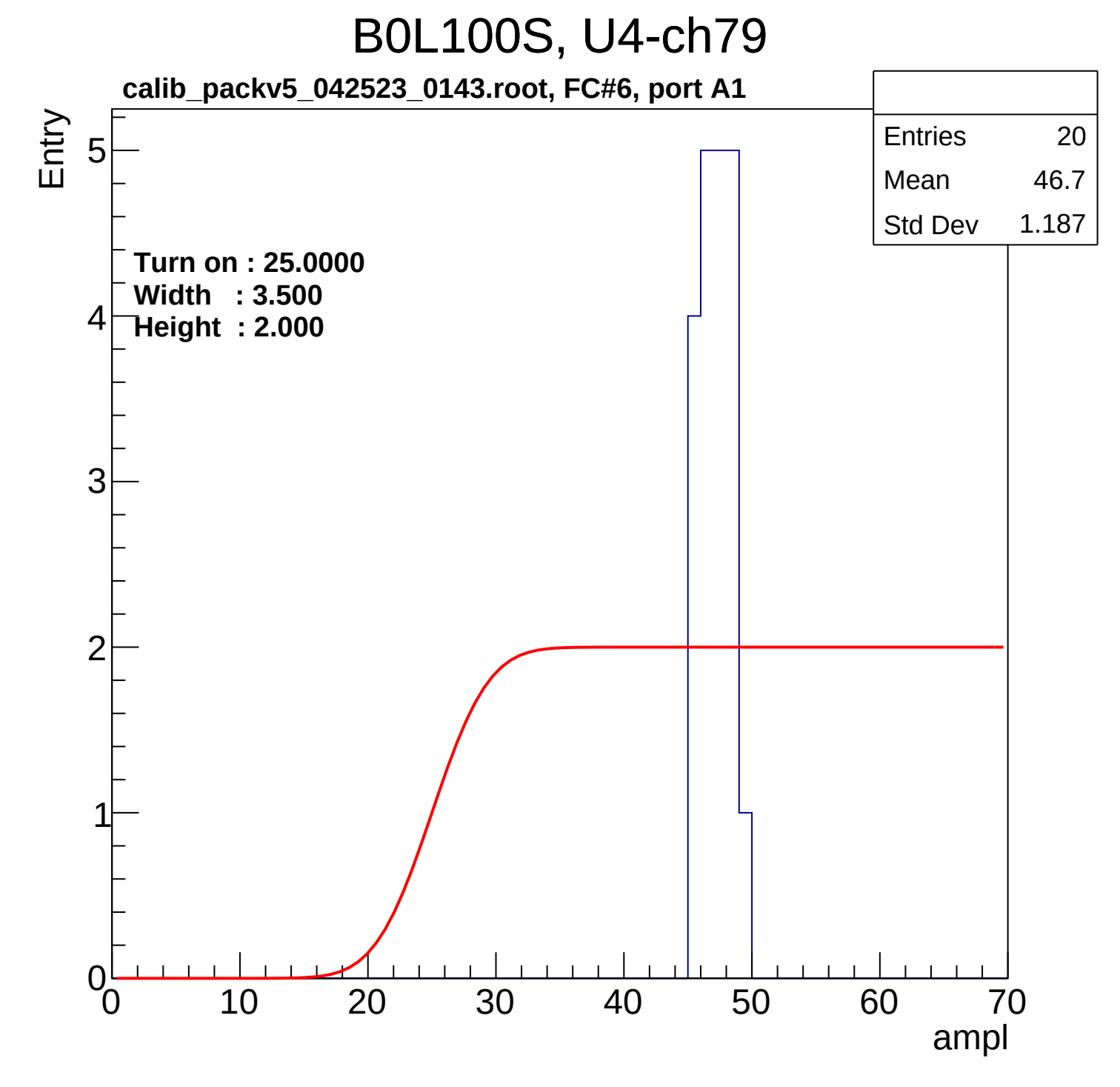
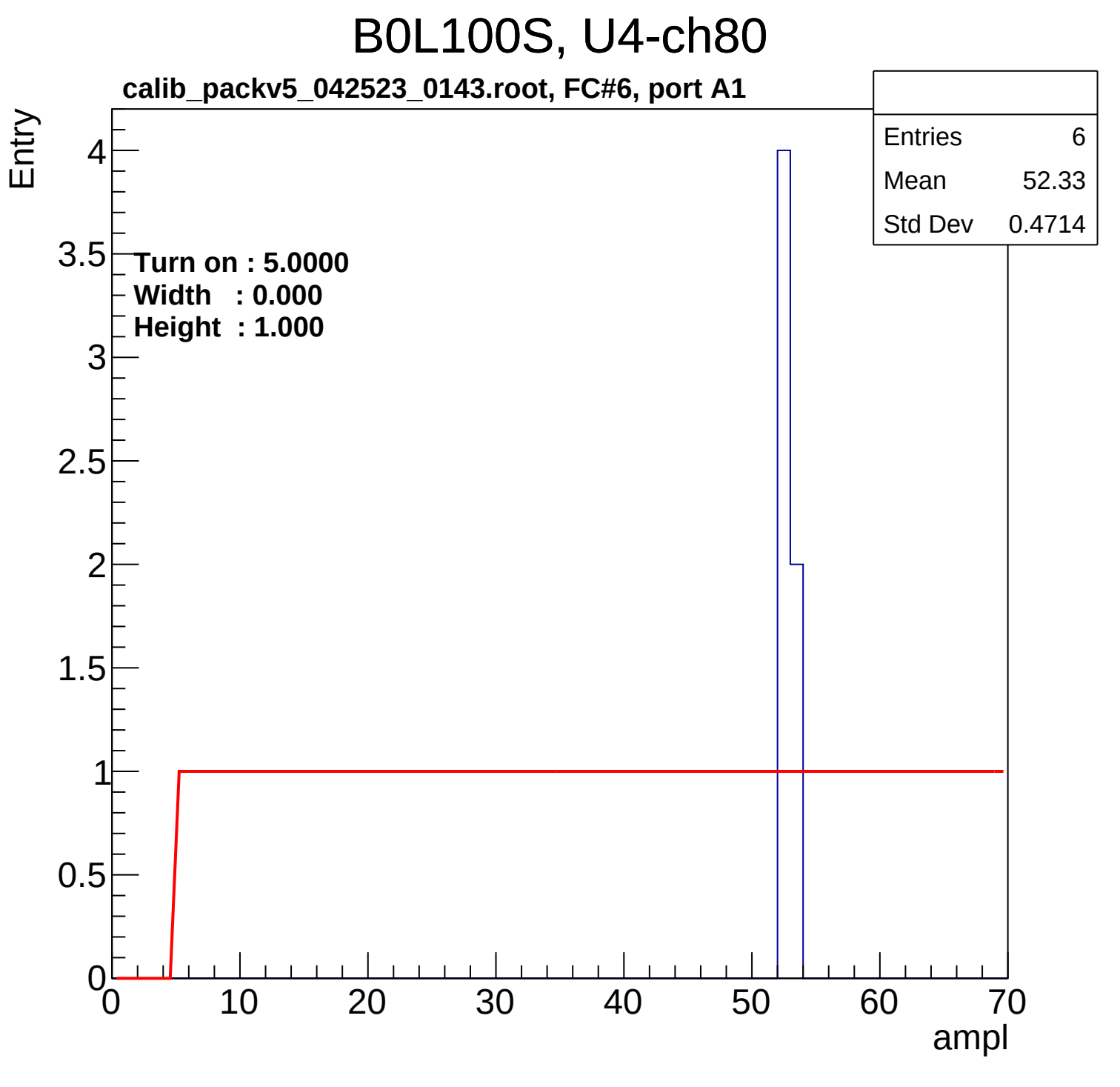
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U4-ch78
calib_packv5_042523_0143.root, FC#6, port A1
Entries 31
Mean 46.32
Std Dev 3.596
Turn on : 24.9985
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U4-ch79
calib_packv5_042523_0143.root, FC#6, port A1
Entries 20
Mean 46.7
Std Dev 1.187
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U4-ch80
calib_packv5_042523_0143.root, FC#6, port A1
Entries 6
Mean 52.33
Std Dev 0.4714
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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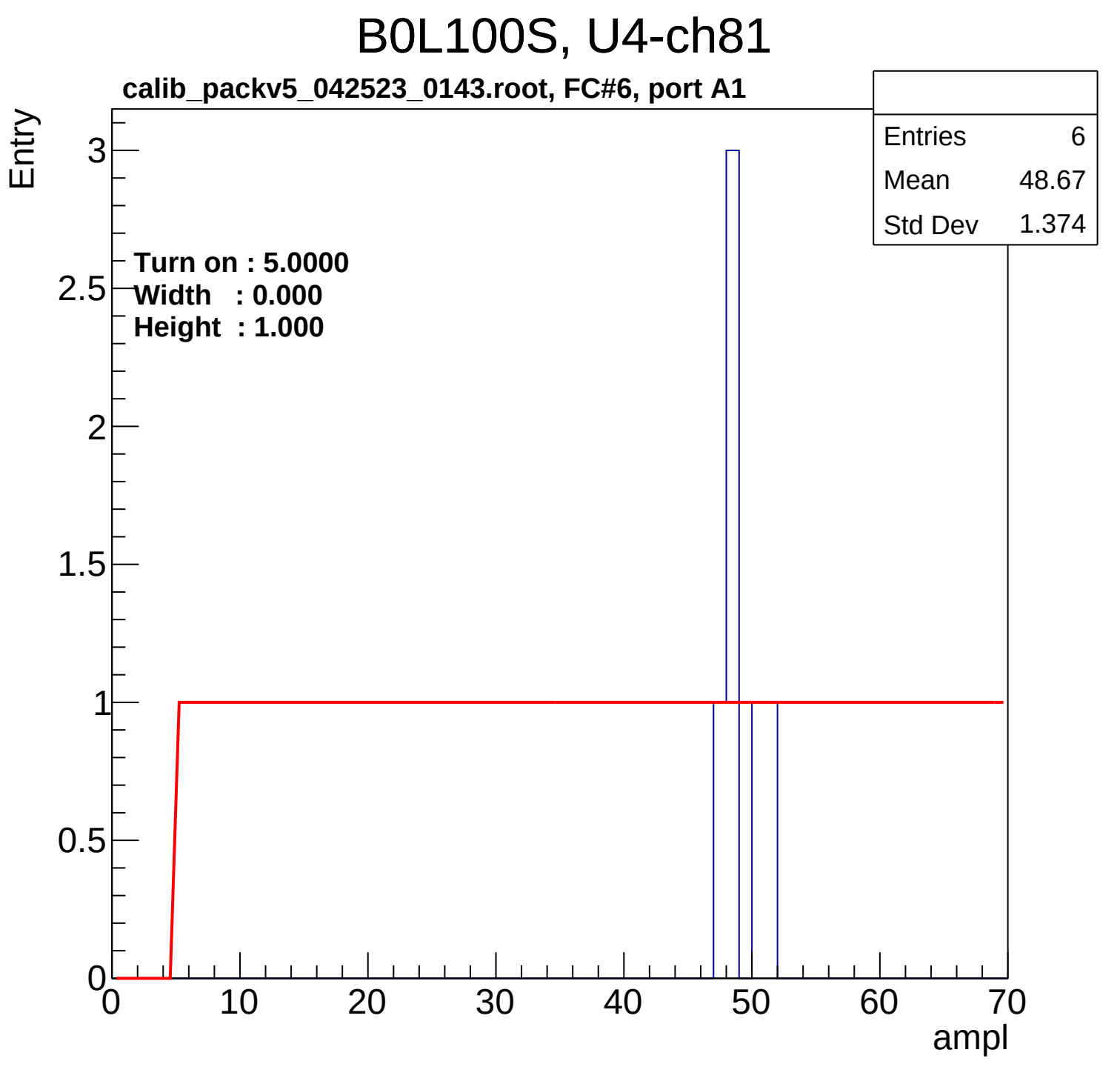
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B0L100S, U4-ch81
calib_packv5_042523_0143.root, FC#6, port A1
Entries 6
Mean 48.67
Std Dev 1.374
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
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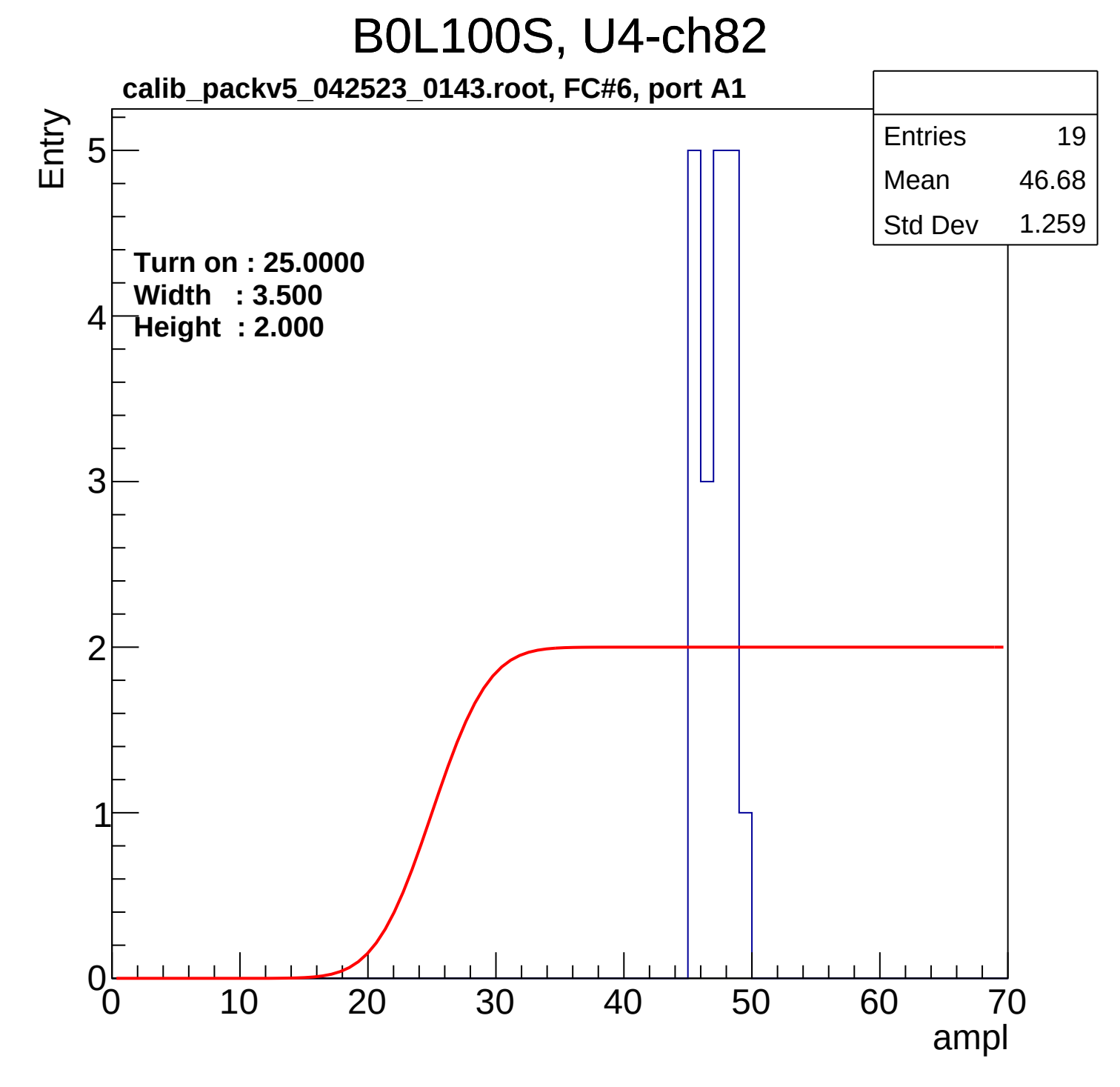
20
30
40
50
60
70


B0L100S, U4-ch82
calib_packv5_042523_0143.root, FC#6, port A1
Entries 19
Mean 46.68
Std Dev 1.259
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
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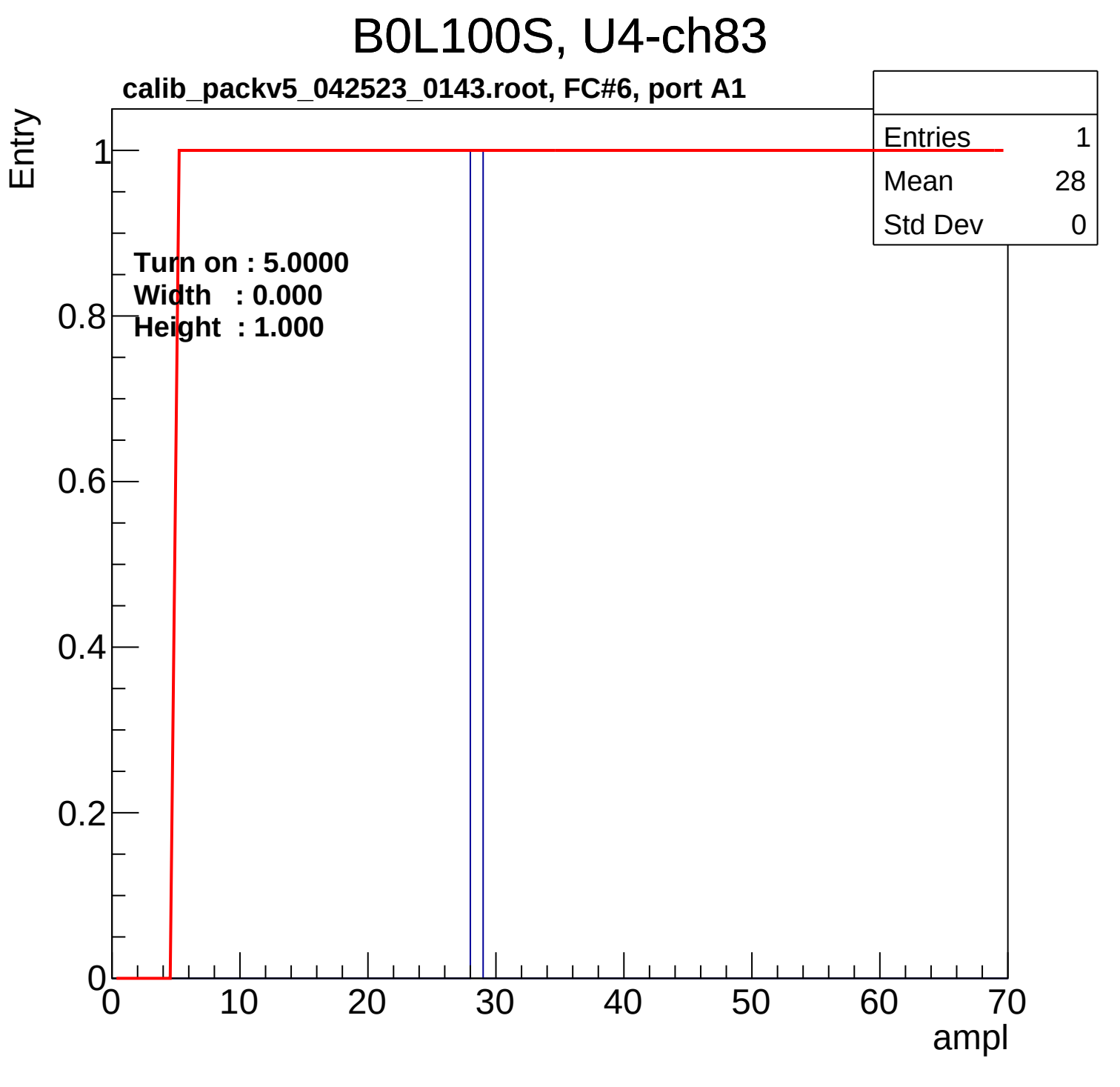
20
30
40
50
60
70


B0L100S, U4-ch83
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 28
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
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0.4
0.6
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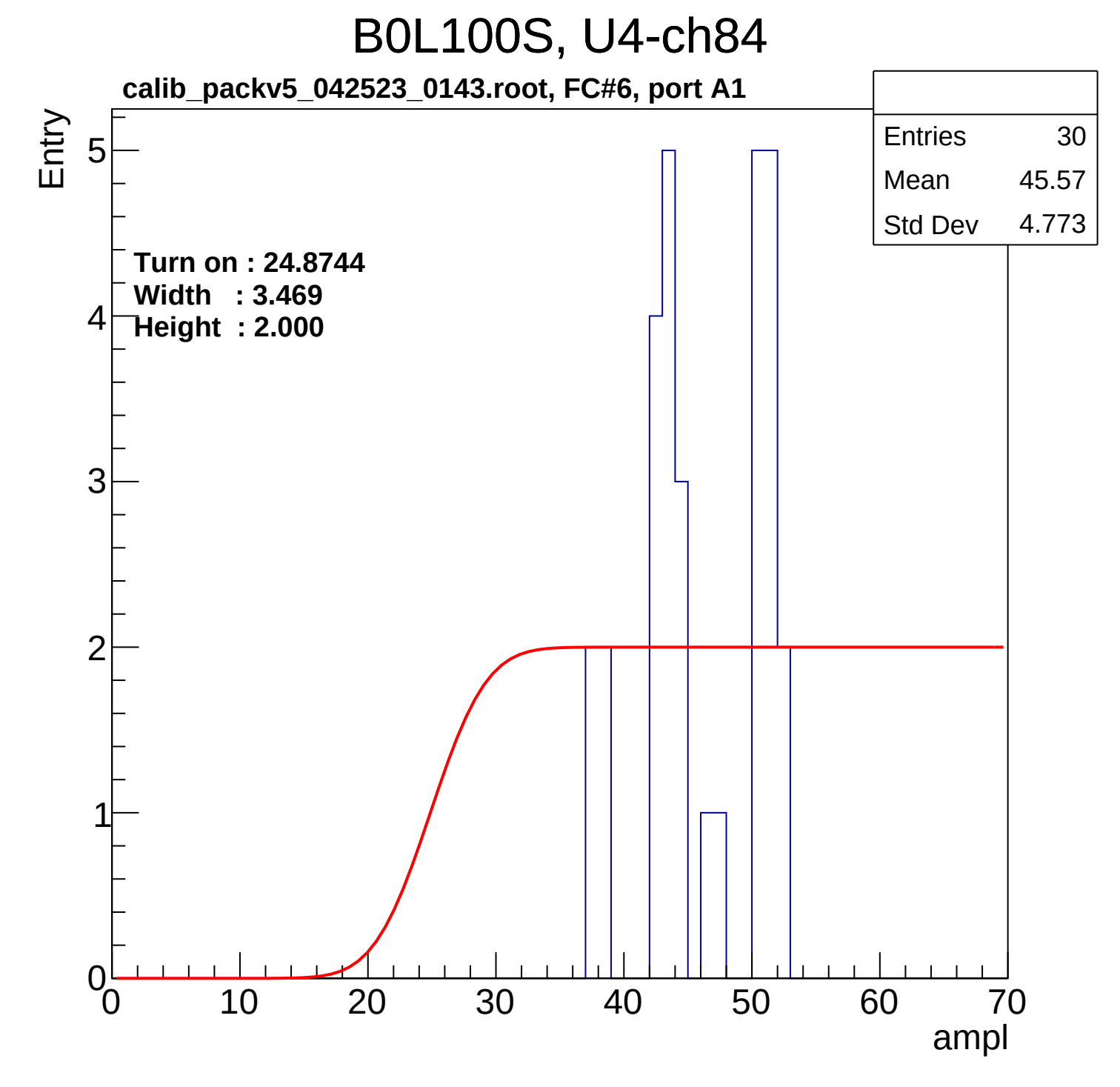
1
0
10
20
30
40
50
60
70


B0L100S, U4-ch84
calib_packv5_042523_0143.root, FC#6, port A1
Entries 30
Mean 45.57
Std Dev 4.773
Turn on : 24.8744
Width : 3.469
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
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40
50
60
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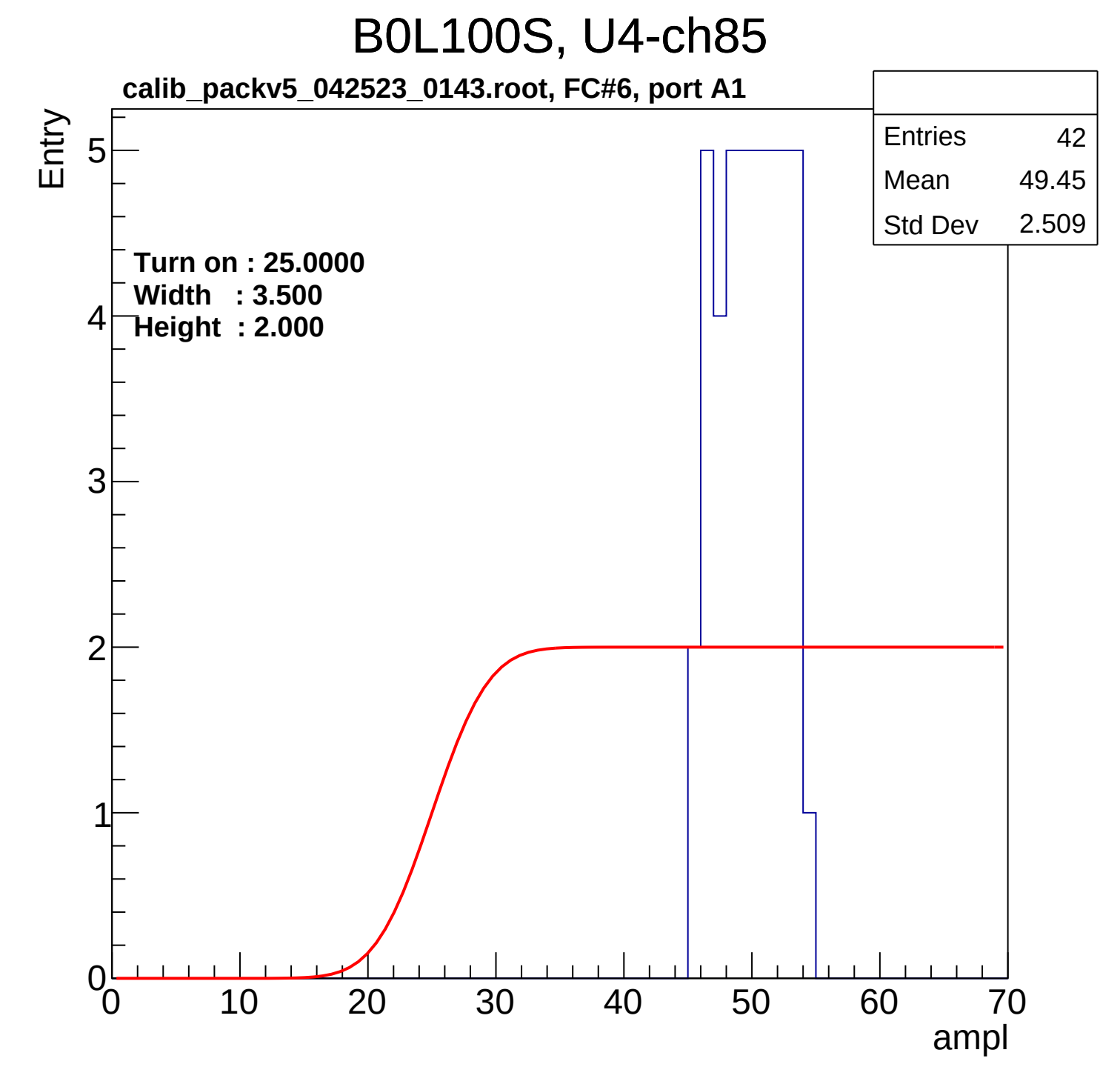
B0L100S, U4-ch85
calib_packv5_042523_0143.root, FC#6, port A1
Entries 42
Mean 49.45
Std Dev 2.509
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
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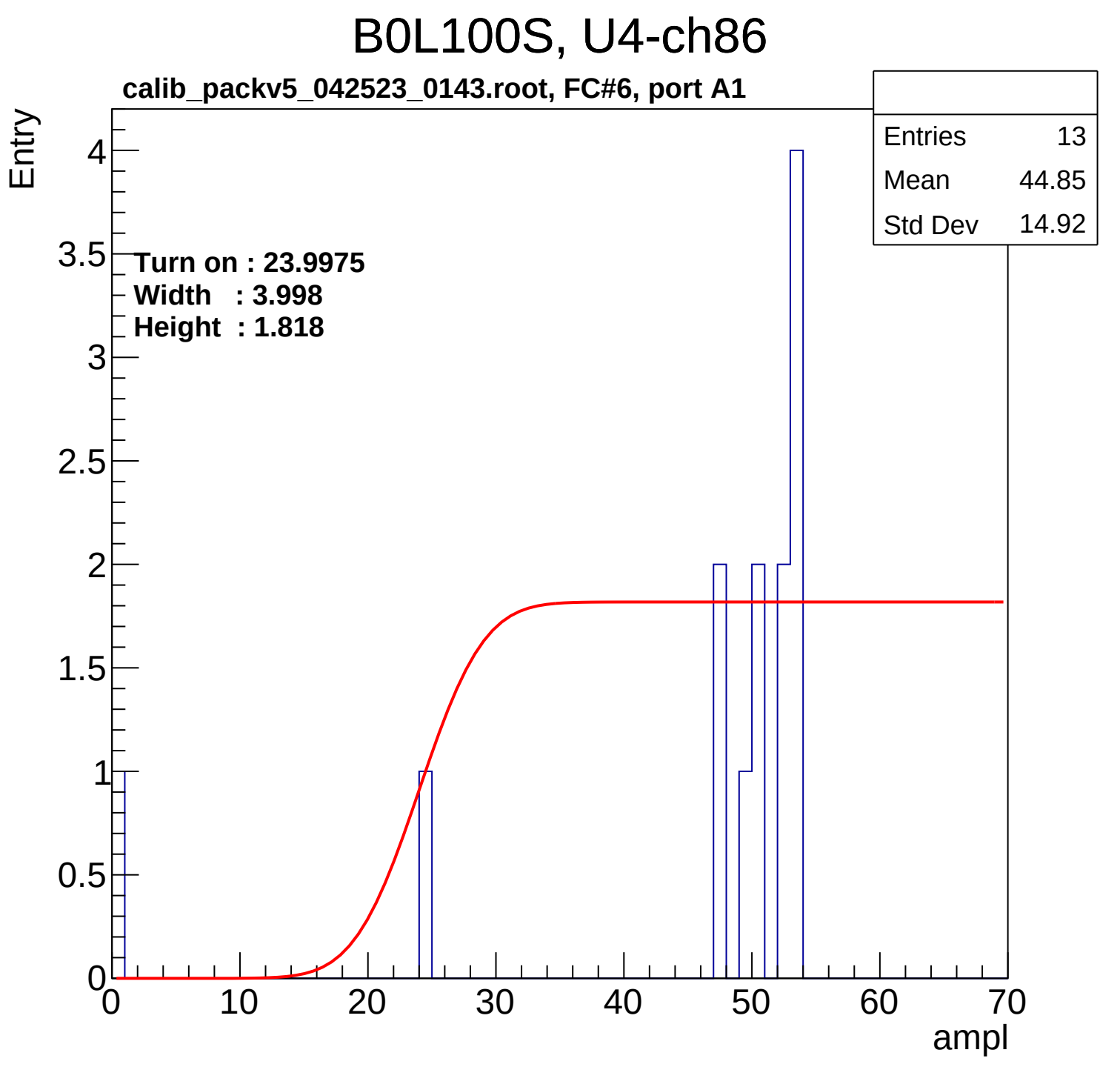
30
40
50
60
70


B0L100S, U4-ch86
calib_packv5_042523_0143.root, FC#6, port A1
Entries 13
Mean 44.85
Std Dev 14.92
Turn on : 23.9975
Width : 3.998
Height : 1.818
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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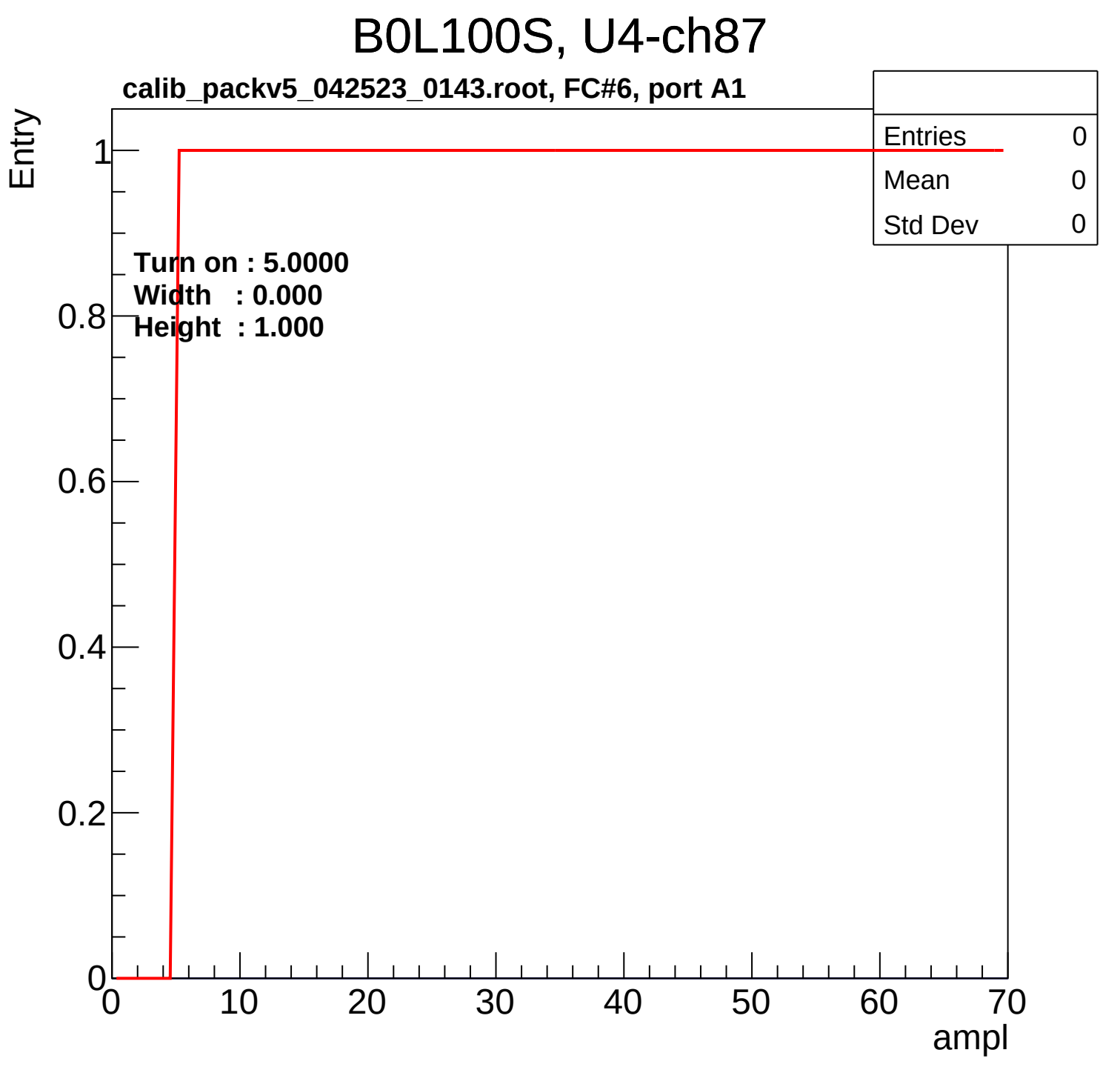
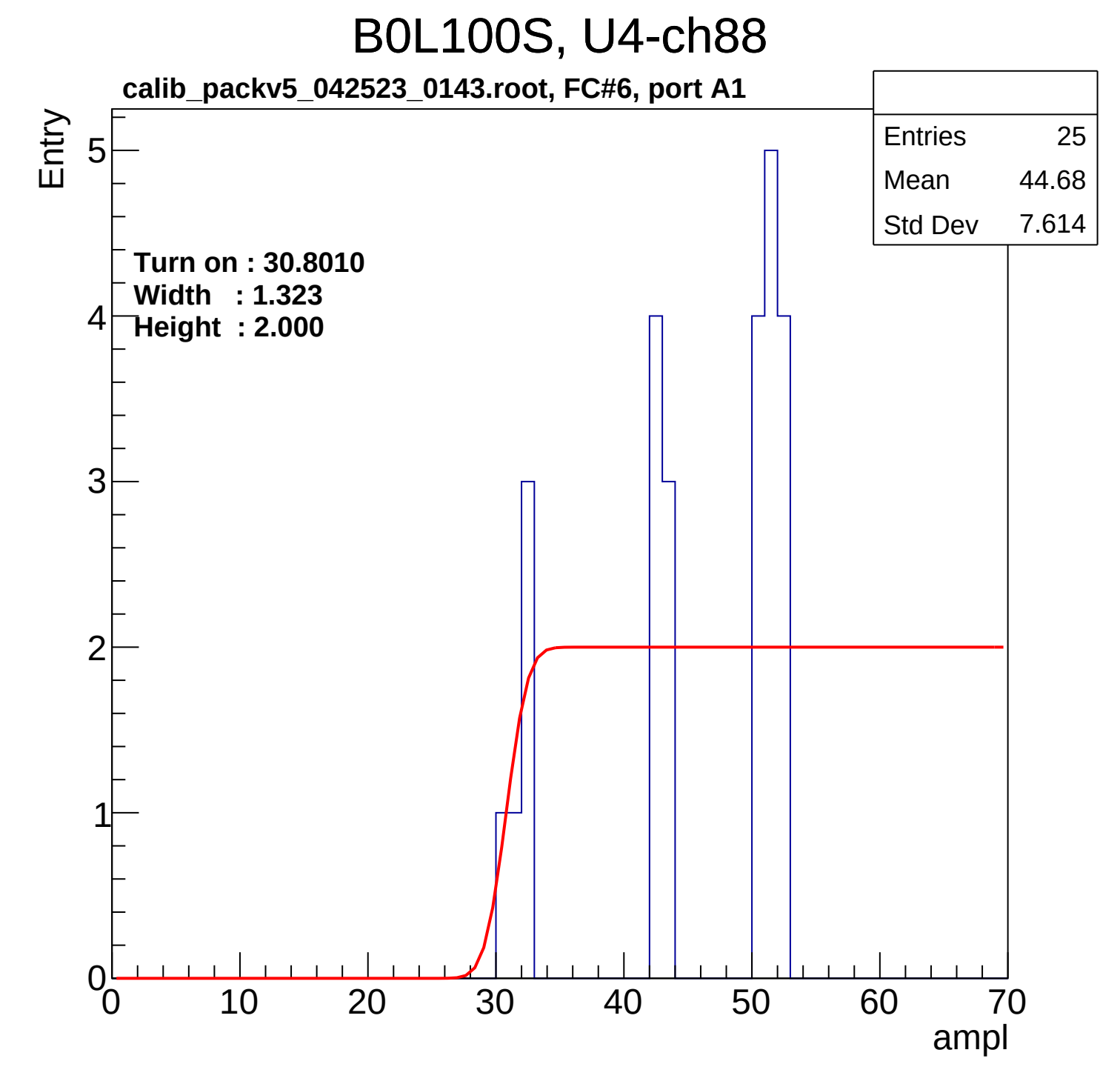
40
50
60
70


B0L100S, U4-ch87
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U4-ch88
calib_packv5_042523_0143.root, FC#6, port A1
Entries 25
Mean 44.68
Std Dev 7.614
Turn on : 30.8010
Width : 1.323
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
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40
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60
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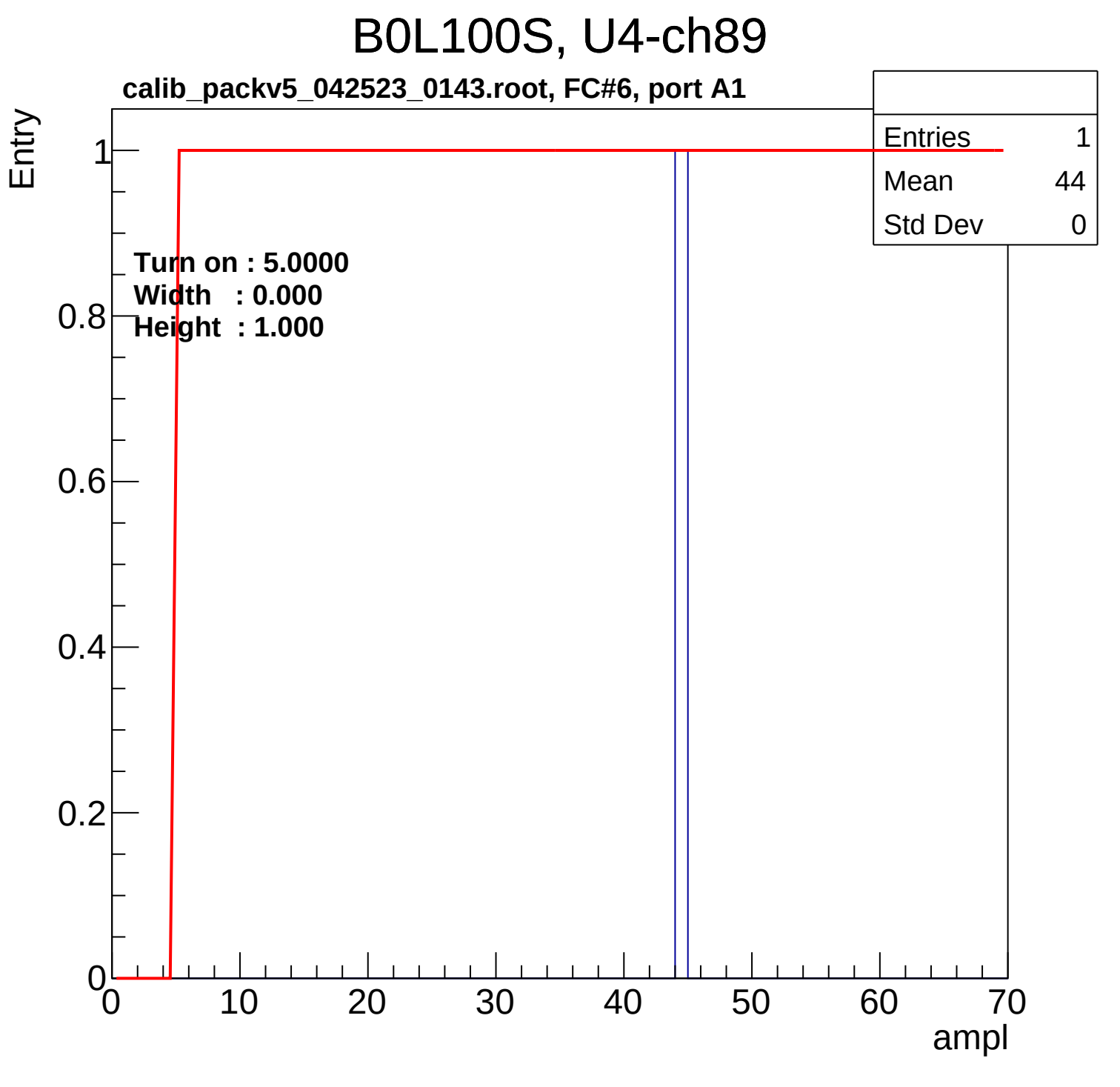
B0L100S, U4-ch89
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 44
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
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40
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60
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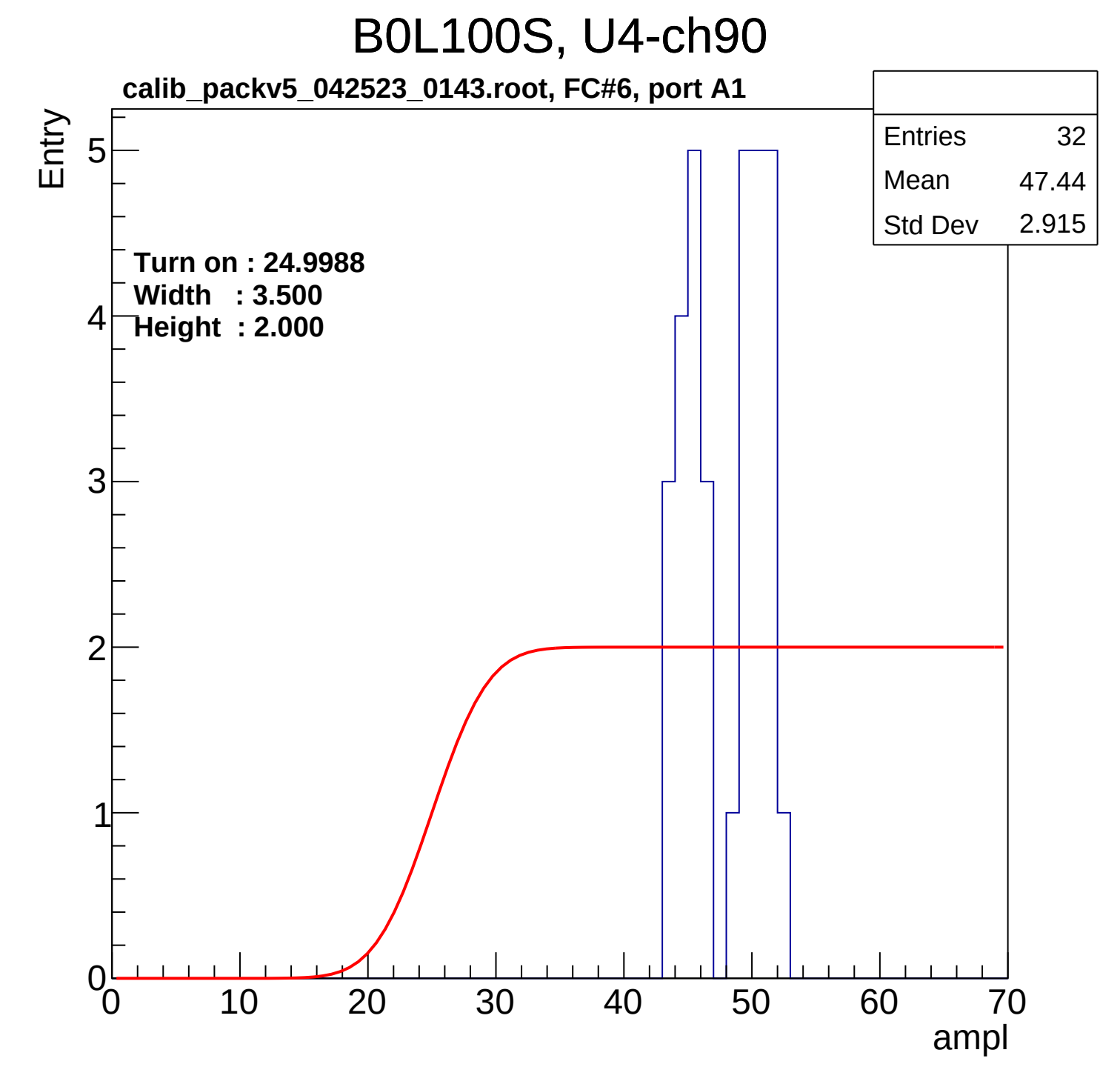
B0L100S, U4-ch90
calib_packv5_042523_0143.root, FC#6, port A1
Entries 32
Mean 47.44
Std Dev 2.915
Turn on : 24.9988
Width : 3.500
Height : 2.000
Entry
ampl
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2
3
4
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0
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40
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60
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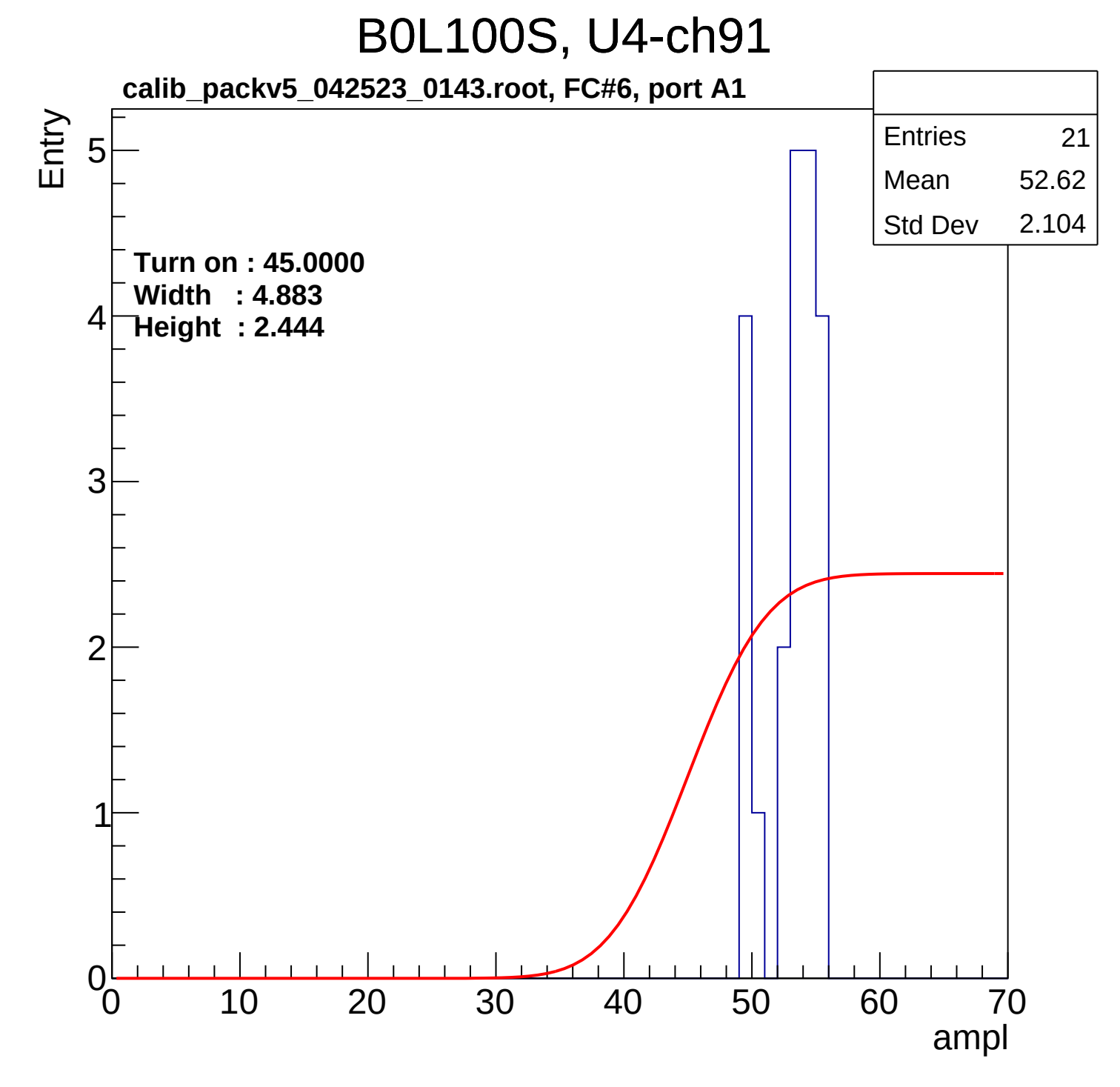
B0L100S, U4-ch91
calib_packv5_042523_0143.root, FC#6, port A1
Entries 21
Mean 52.62
Std Dev 2.104
Turn on : 45.0000
Width : 4.883
Height : 2.444
Entry
ampl
0
1
2
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4
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60
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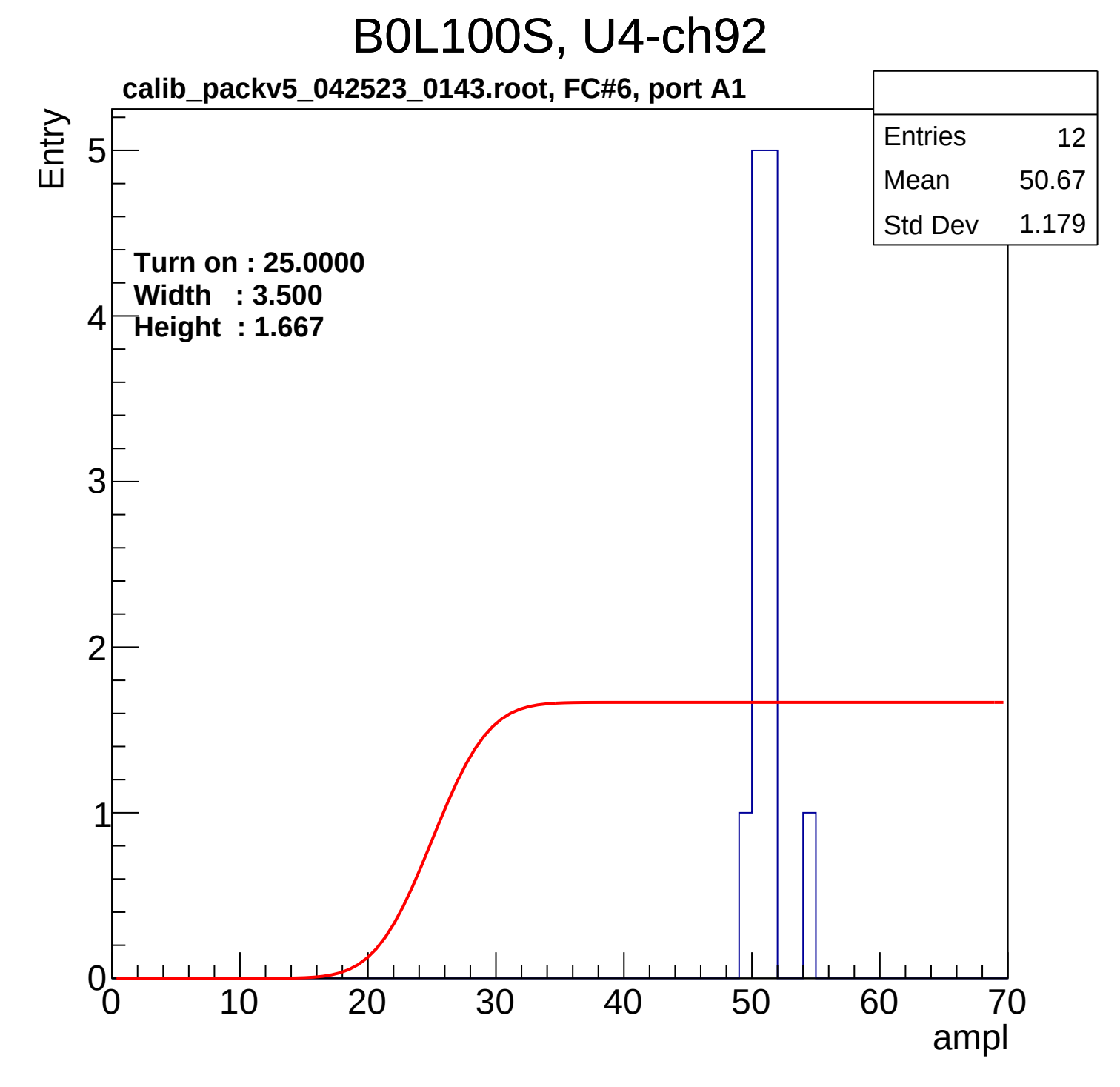
B0L100S, U4-ch92
calib_packv5_042523_0143.root, FC#6, port A1
Entries 12
Mean 50.67
Std Dev 1.179
Turn on : 25.0000
Width : 3.500
Height : 1.667
Entry
ampl
0
1
2
3
4
5
0
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40
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60
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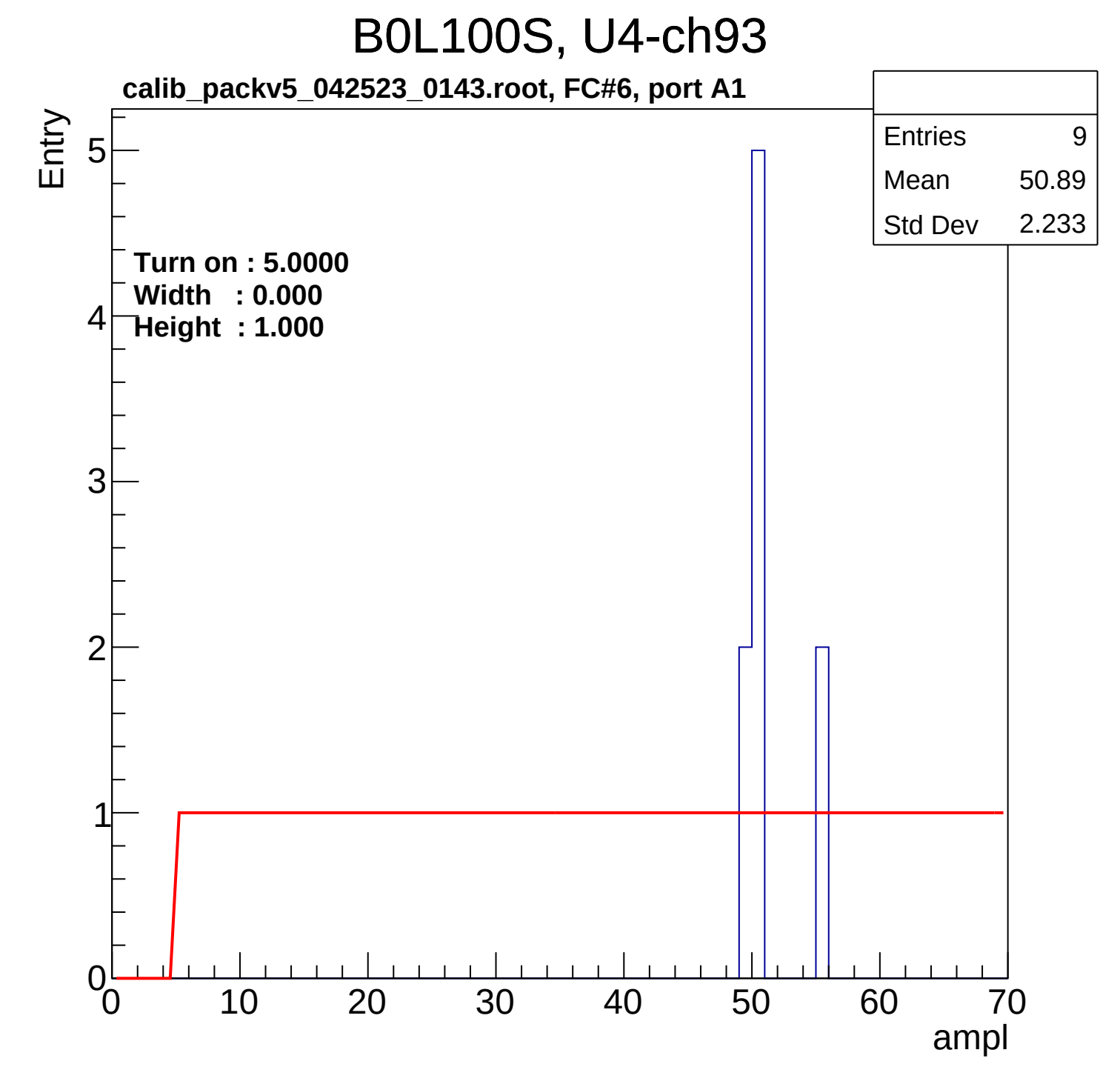
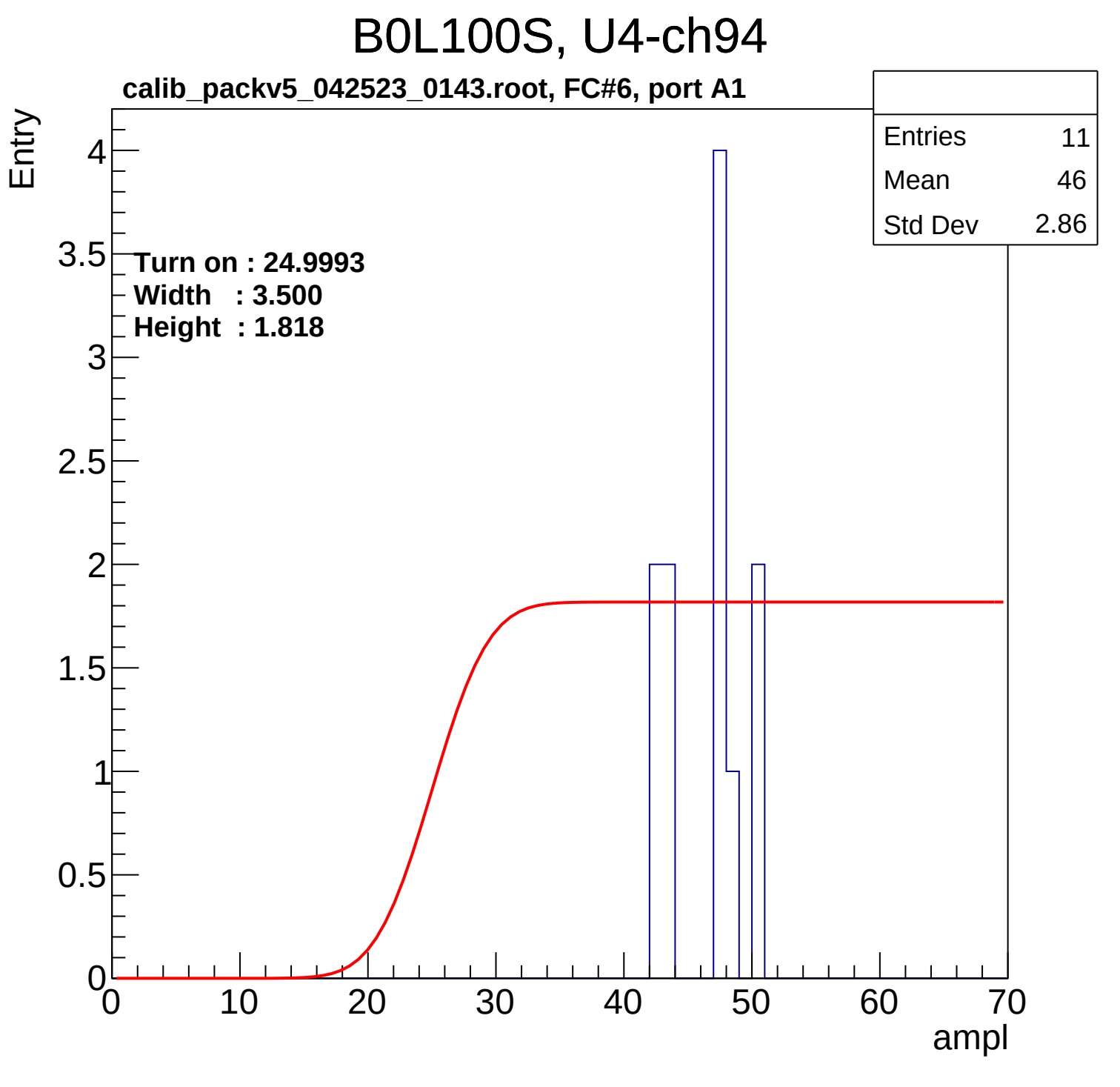

B0L100S, U4-ch93
calib_packv5_042523_0143.root, FC#6, port A1
Entries 9
Mean 50.89
Std Dev 2.233
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U4-ch94
calib_packv5_042523_0143.root, FC#6, port A1
Entries 11
Mean 46
Std Dev 2.86
Turn on : 24.9993
Width : 3.500
Height : 1.818
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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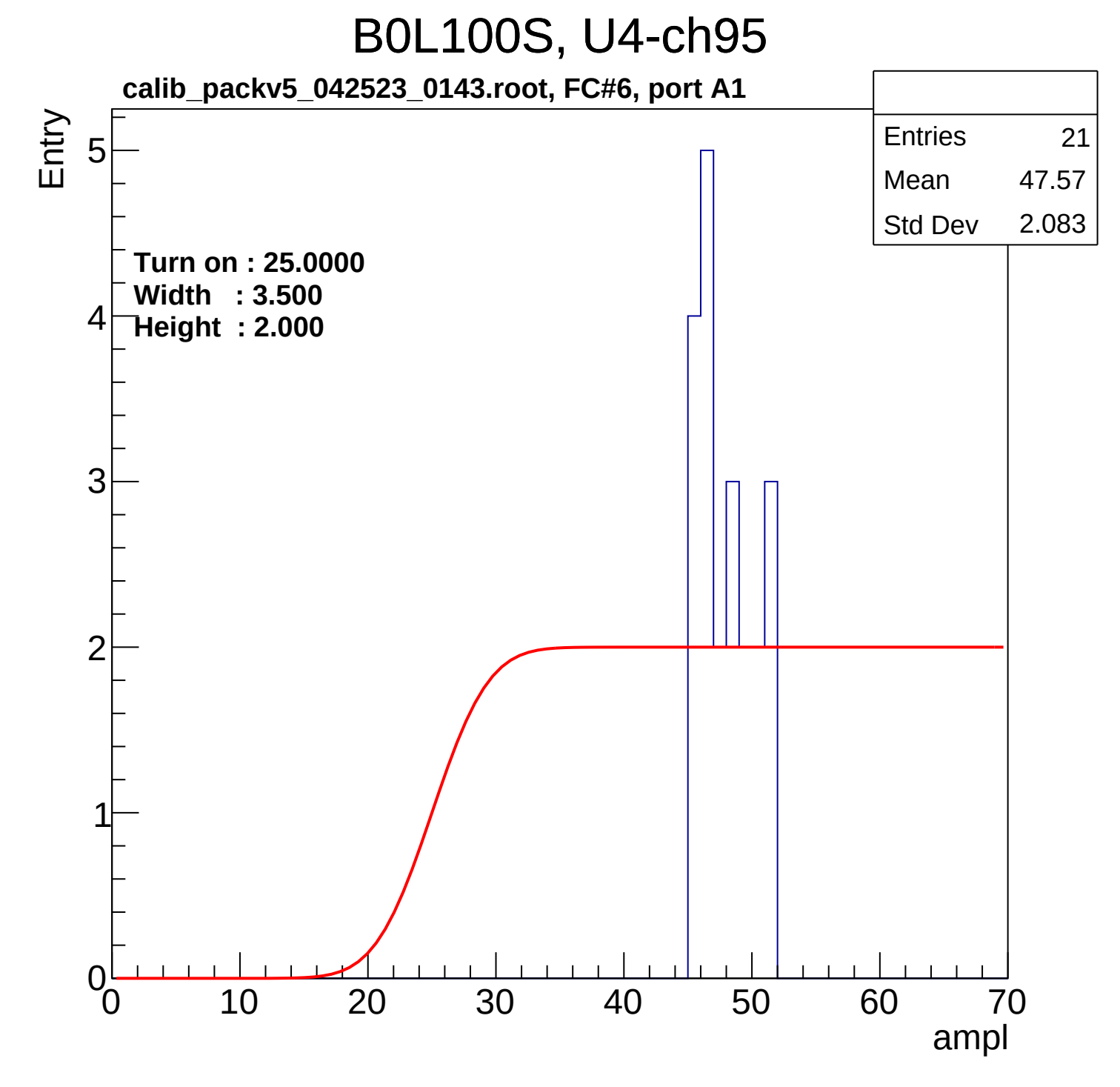
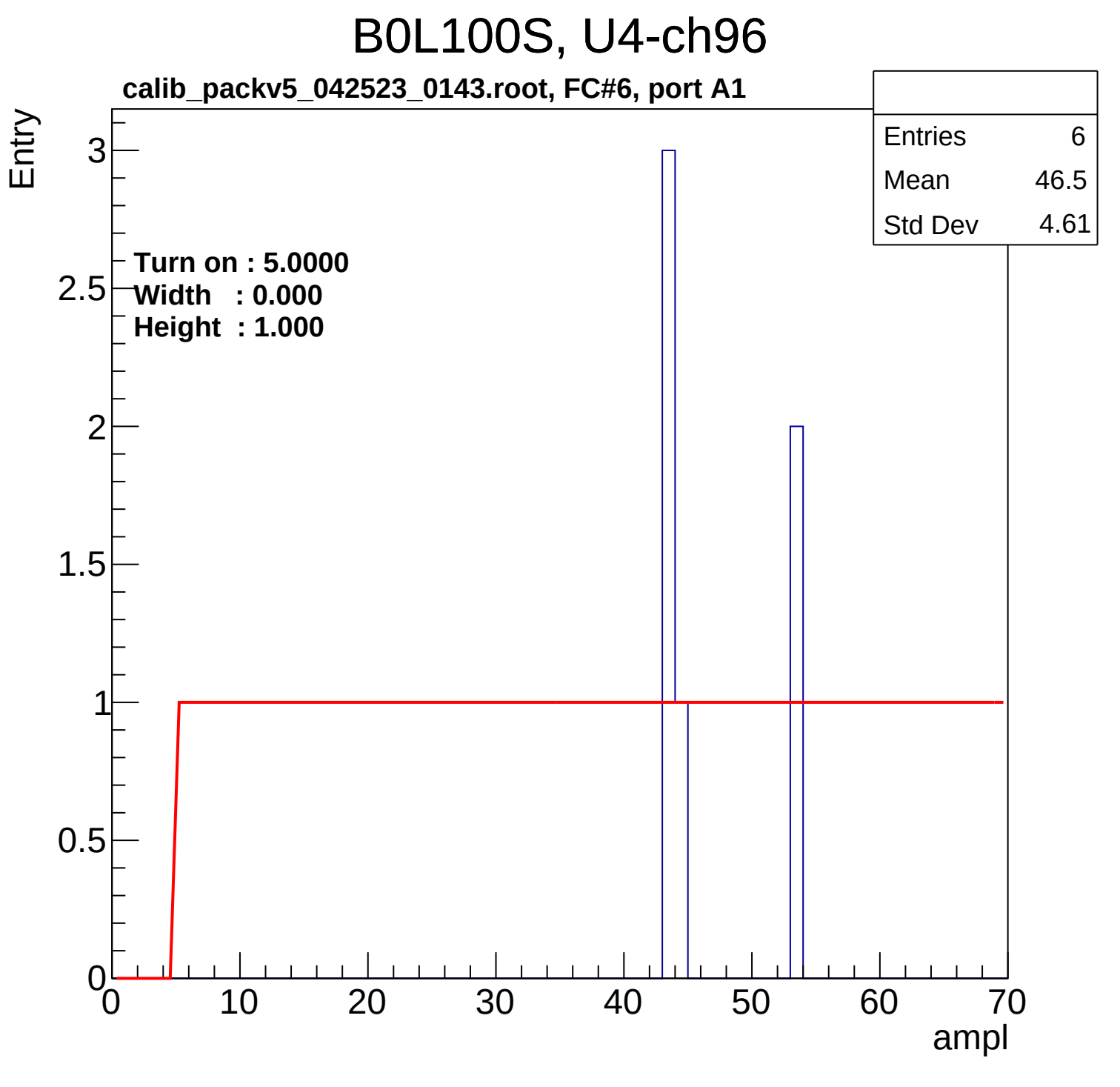
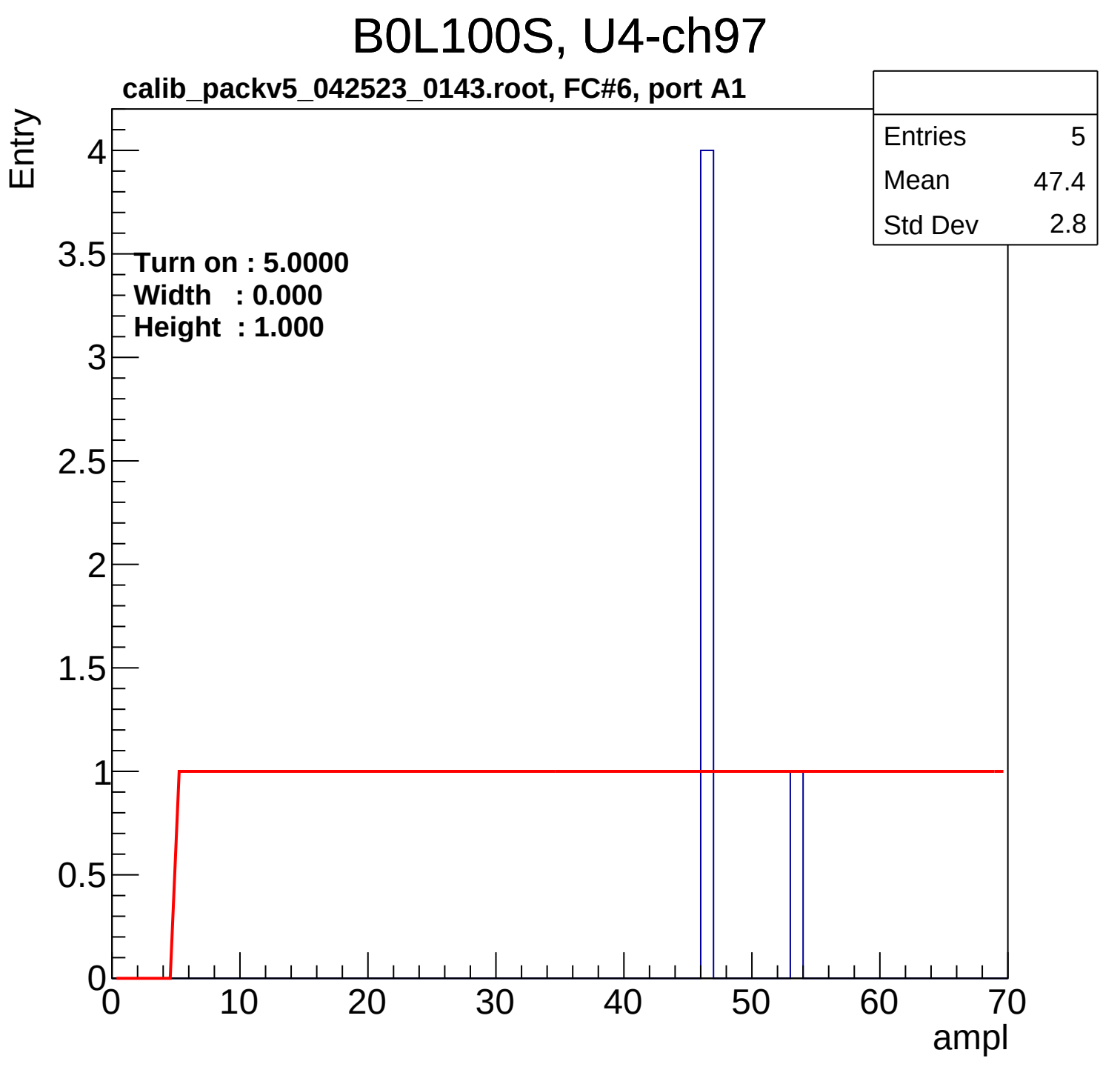
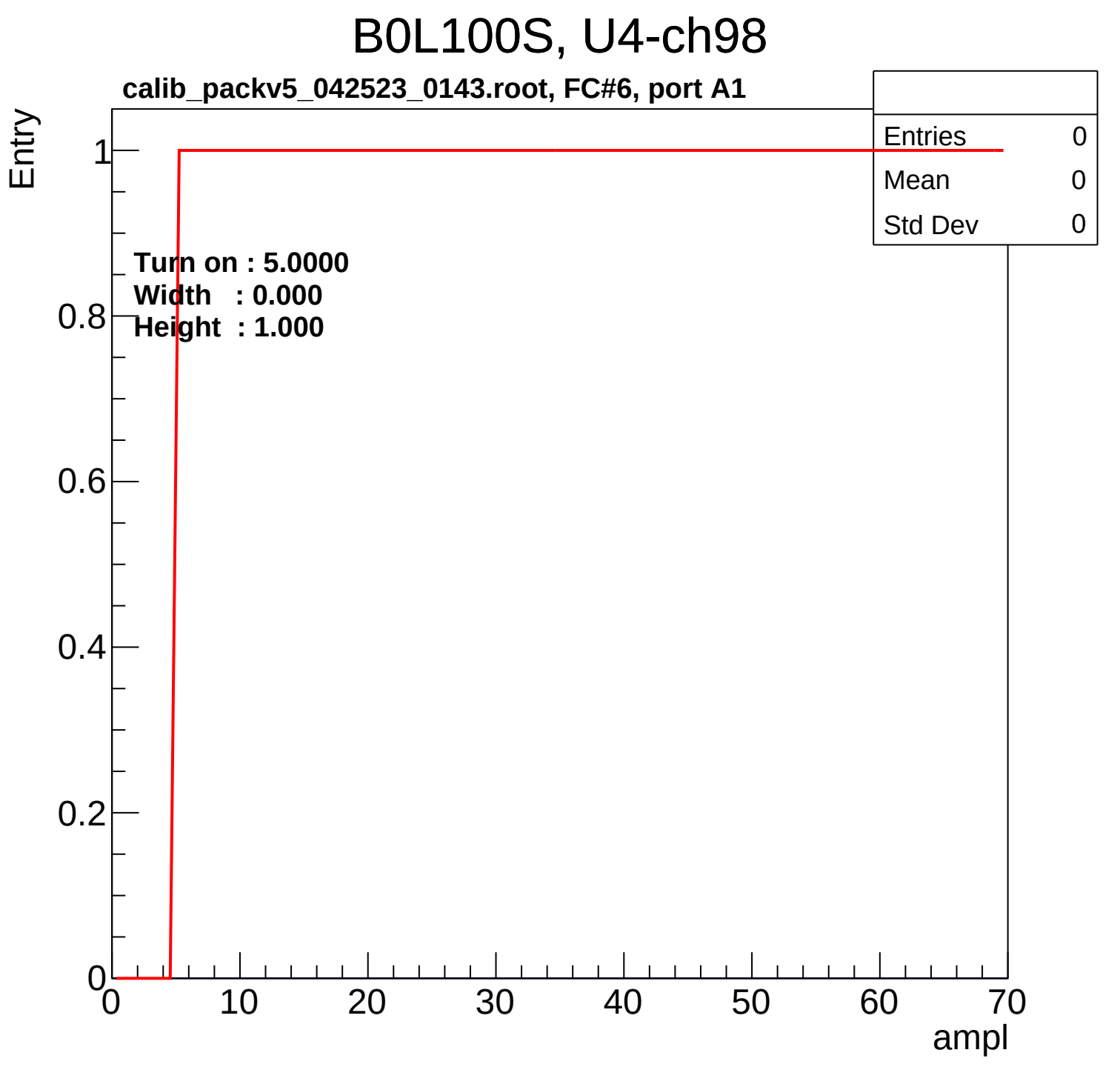
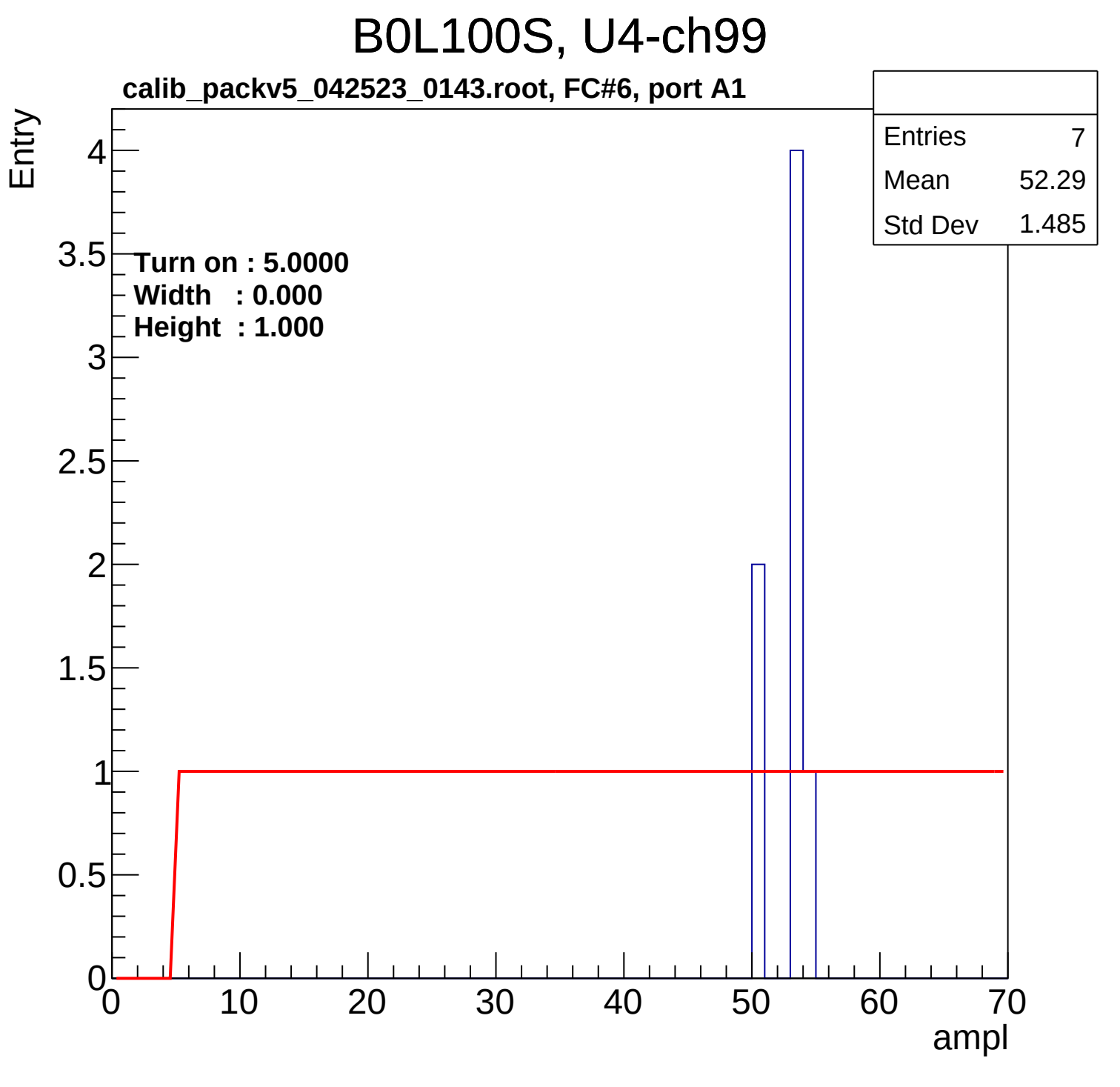
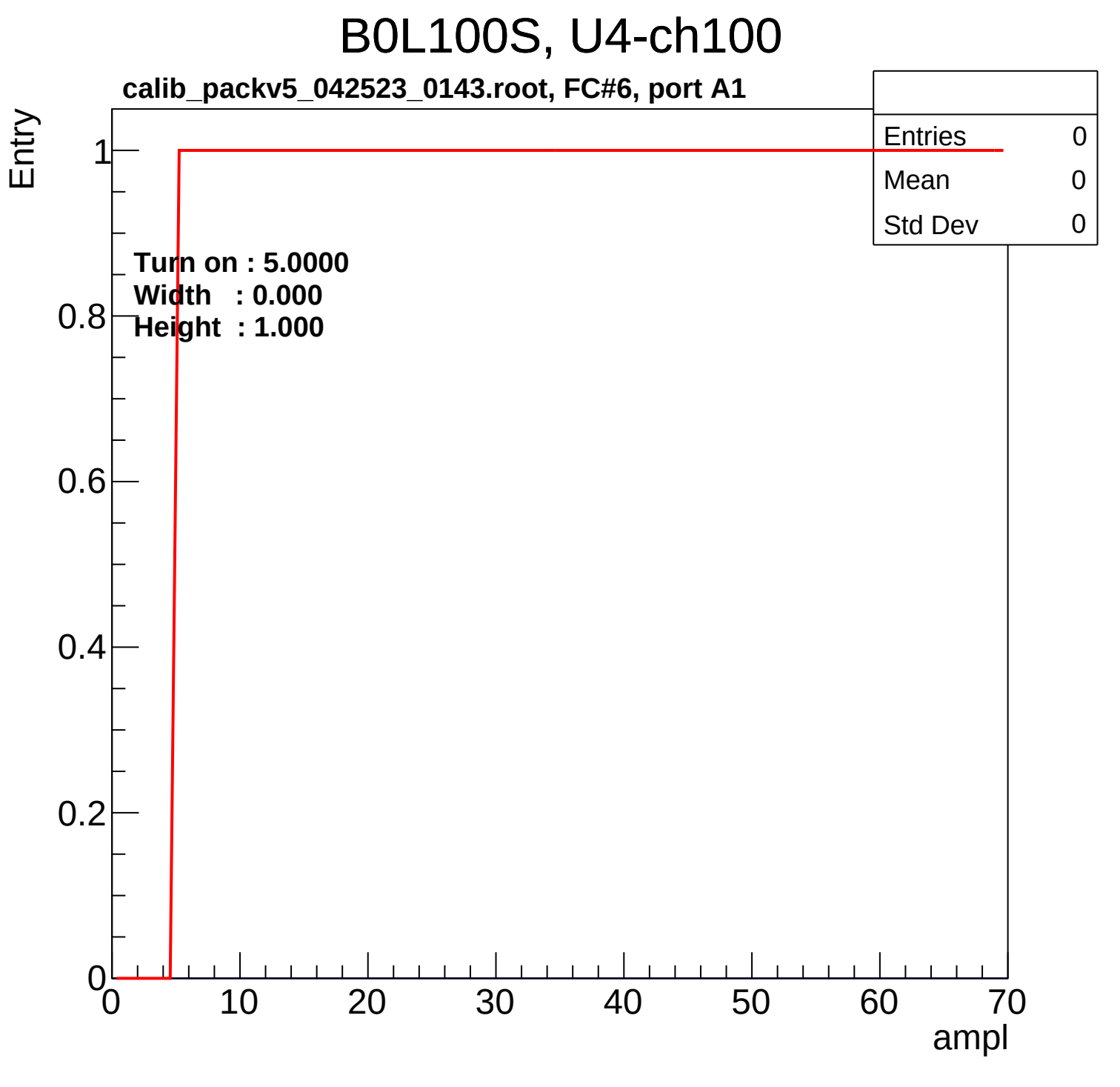

B0L100S, U4-ch95
calib_packv5_042523_0143.root, FC#6, port A1
Entries 21
Mean 47.57
Std Dev 2.083
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

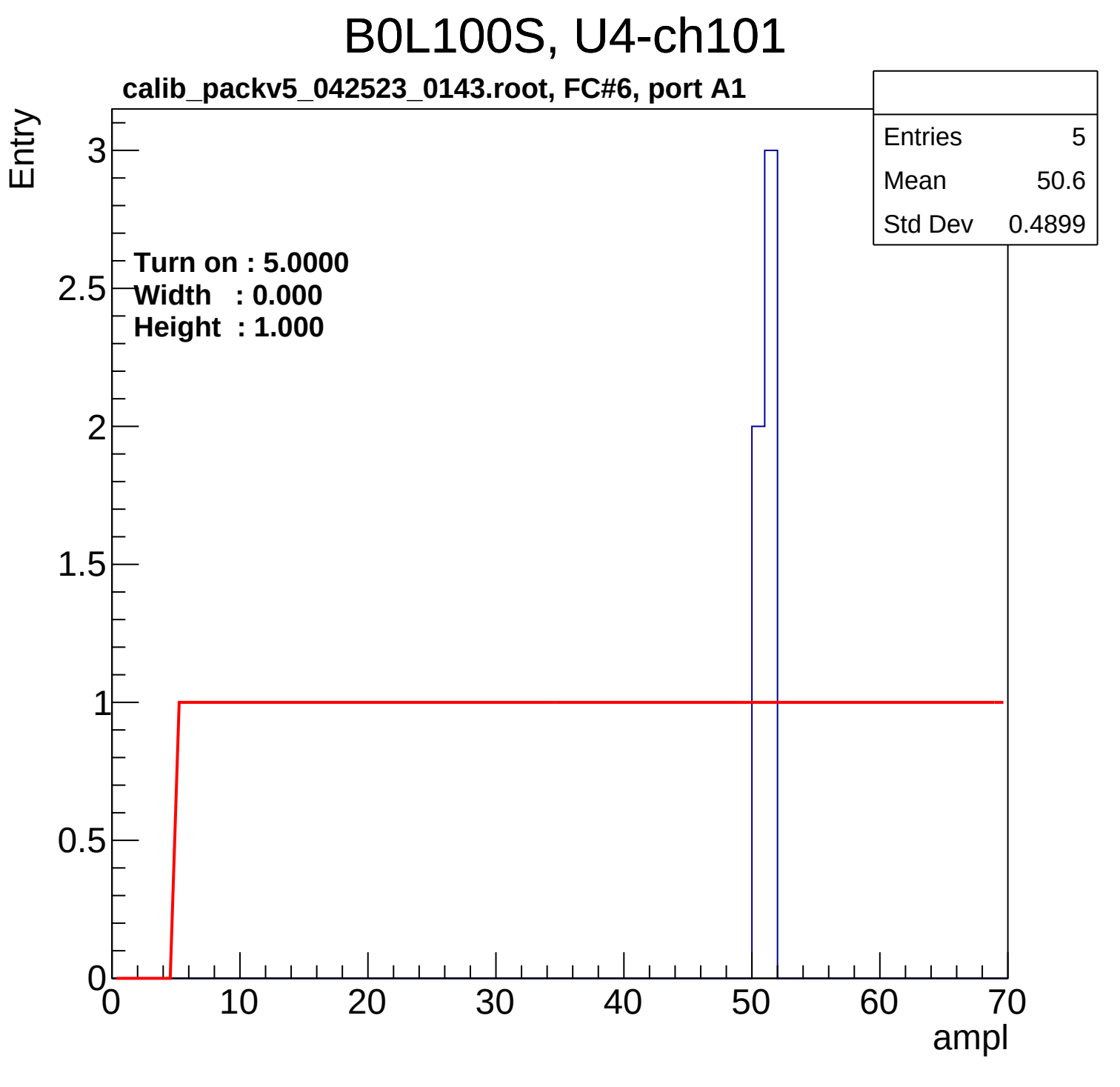

B0L100S, U4-ch96
calib_packv5_042523_0143.root, FC#6, port A1
Entries 6
Mean 46.5
Std Dev 4.61
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

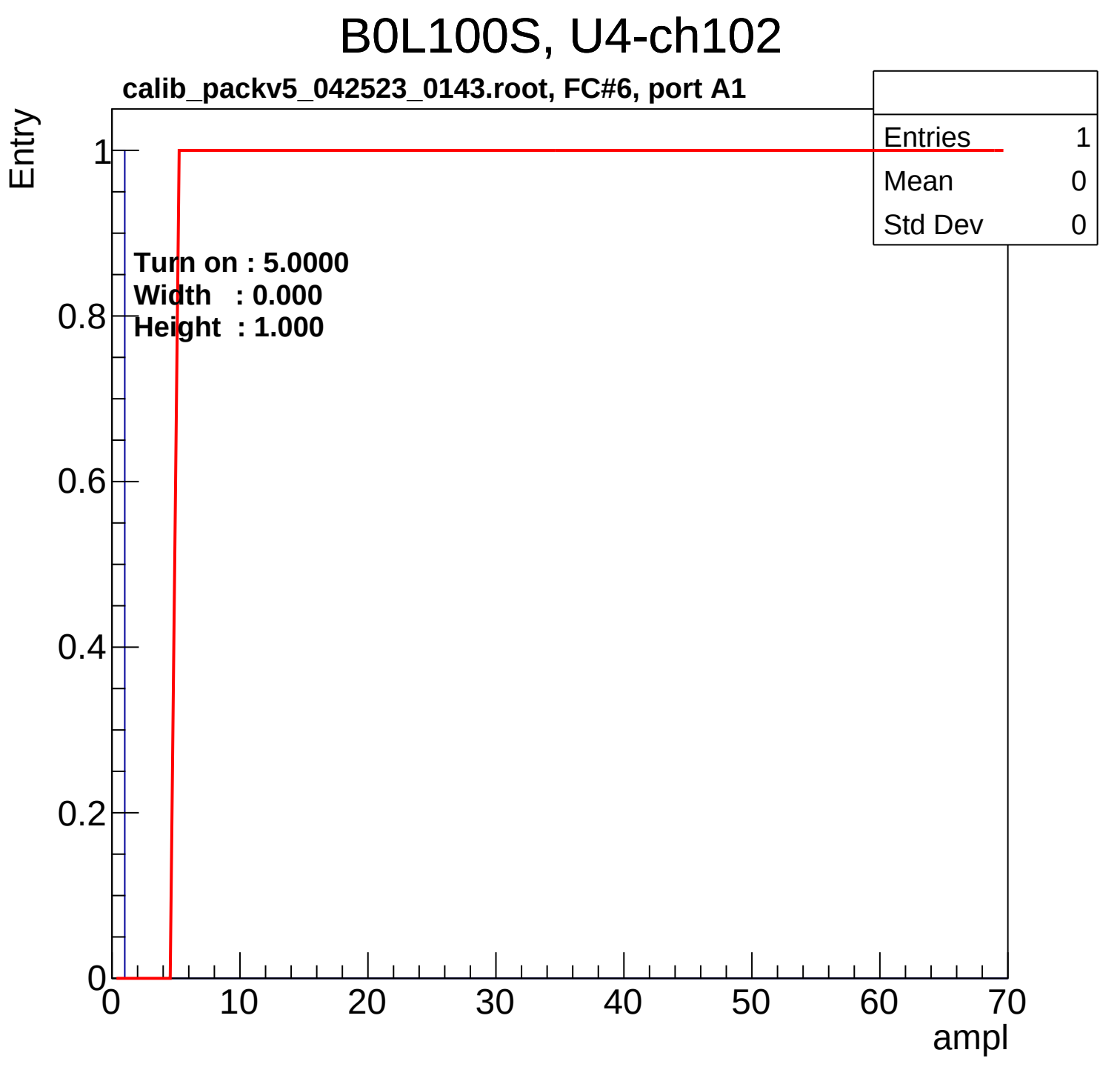

B0L100S, U4-ch97
calib_packv5_042523_0143.root, FC#6, port A1
Entries 5
Mean 47.4
Std Dev 2.8
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

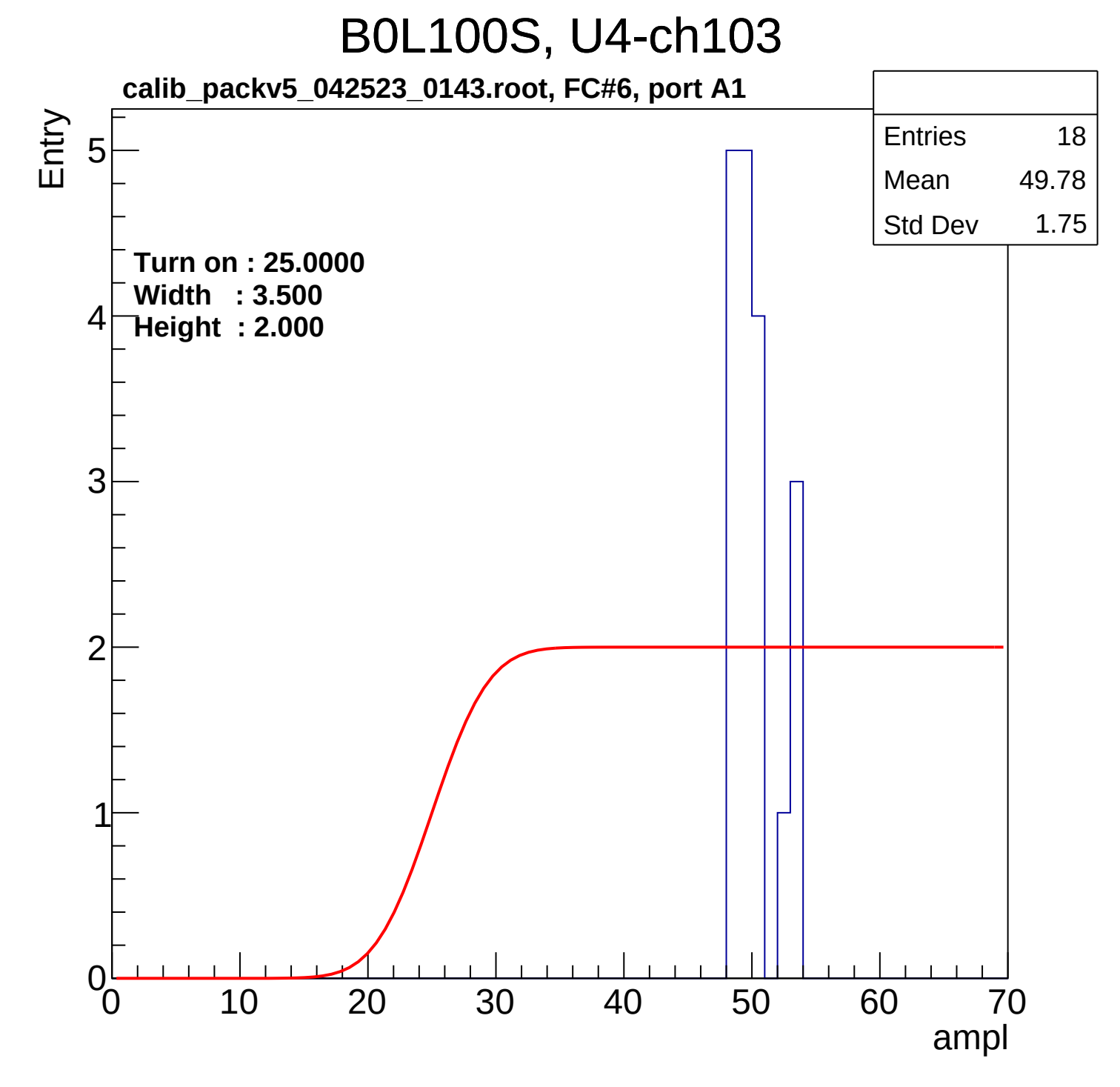

B0L100S, U4-ch98
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

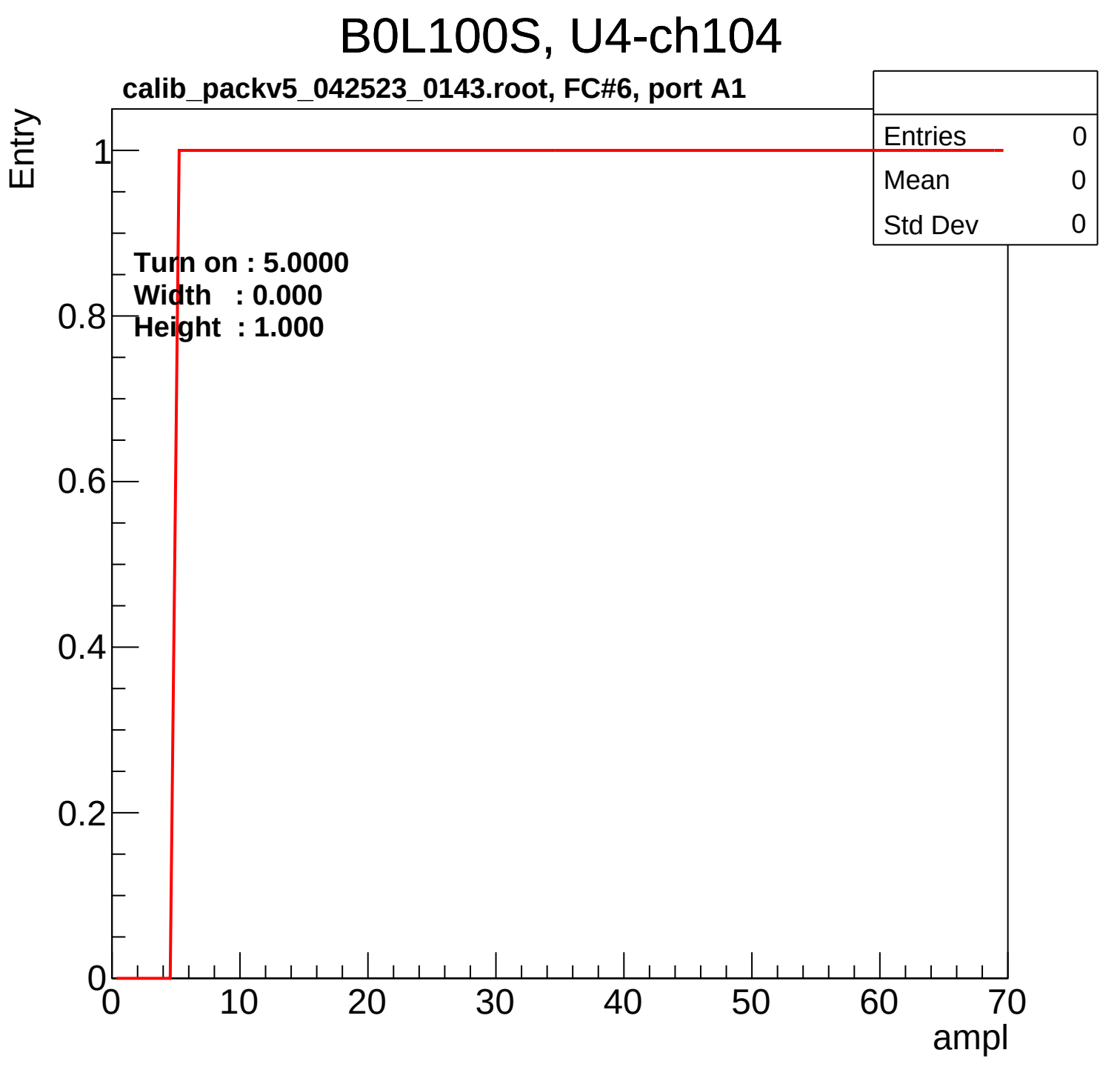

B0L100S, U4-ch99
calib_packv5_042523_0143.root, FC#6, port A1
Entries 7
Mean 52.29
Std Dev 1.485
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

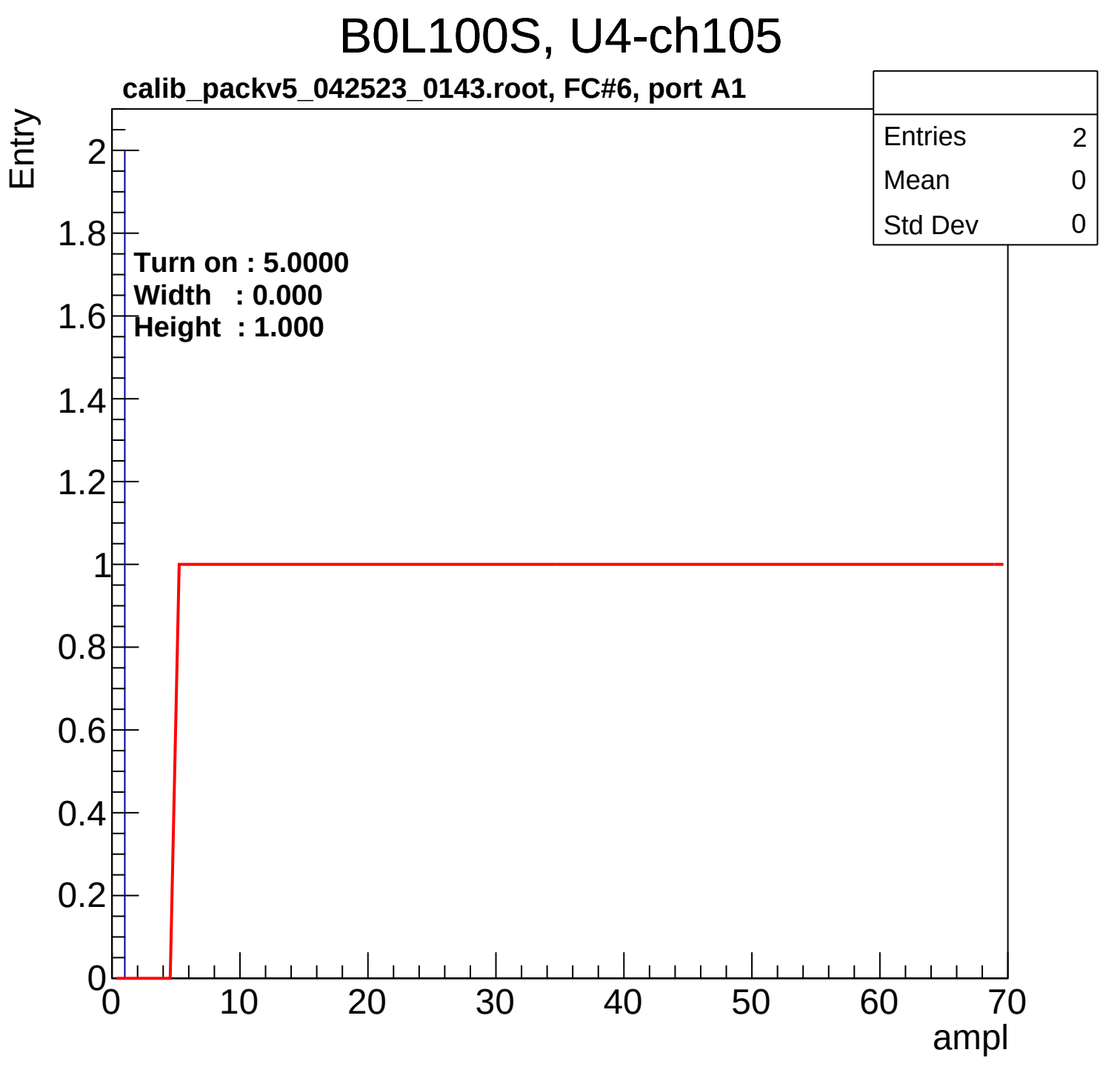

B0L100S, U4-ch100
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

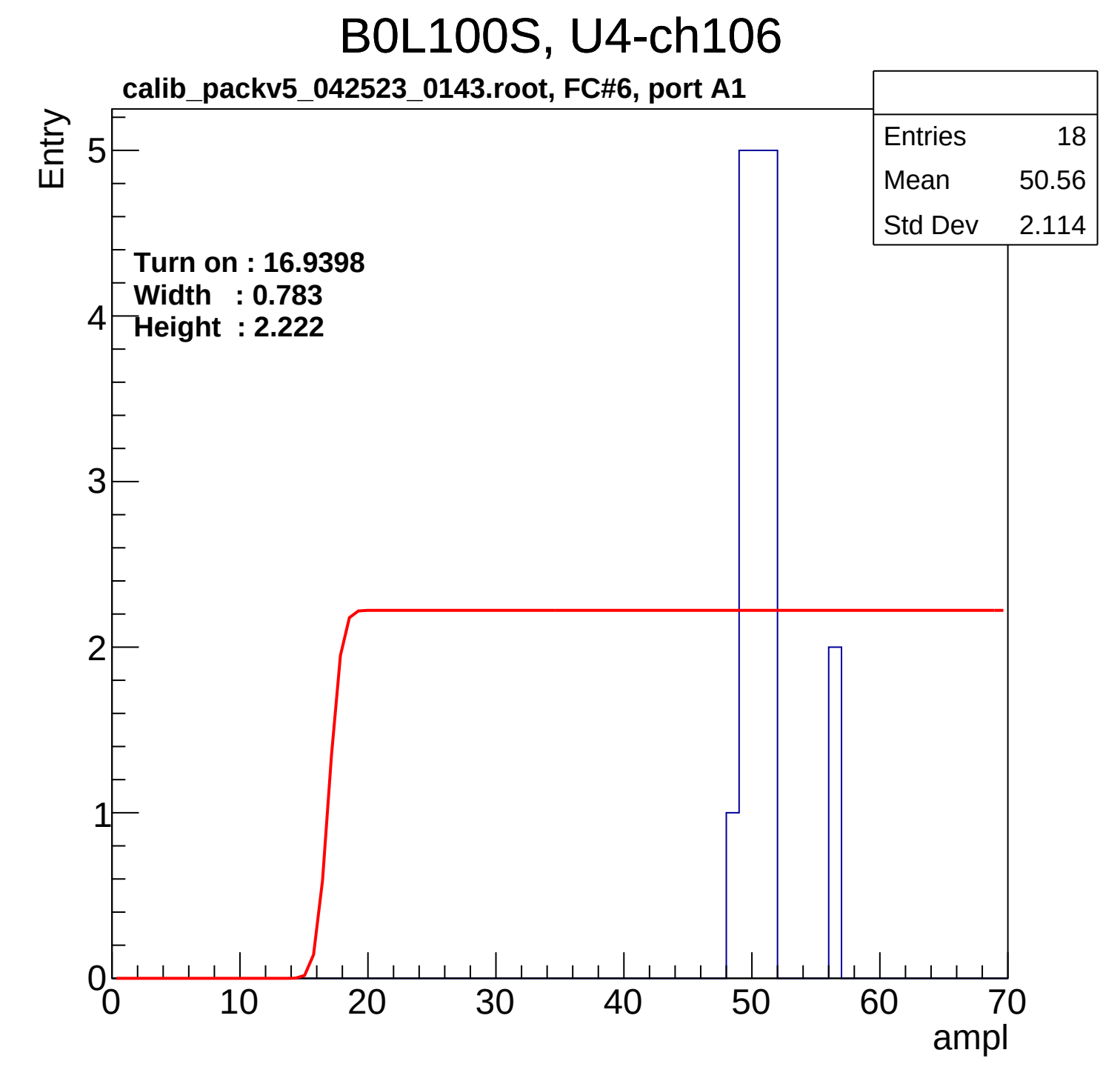

B0L100S, U4-ch101
calib_packv5_042523_0143.root, FC#6, port A1
Entries 5
Mean 50.6
Std Dev 0.4899
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

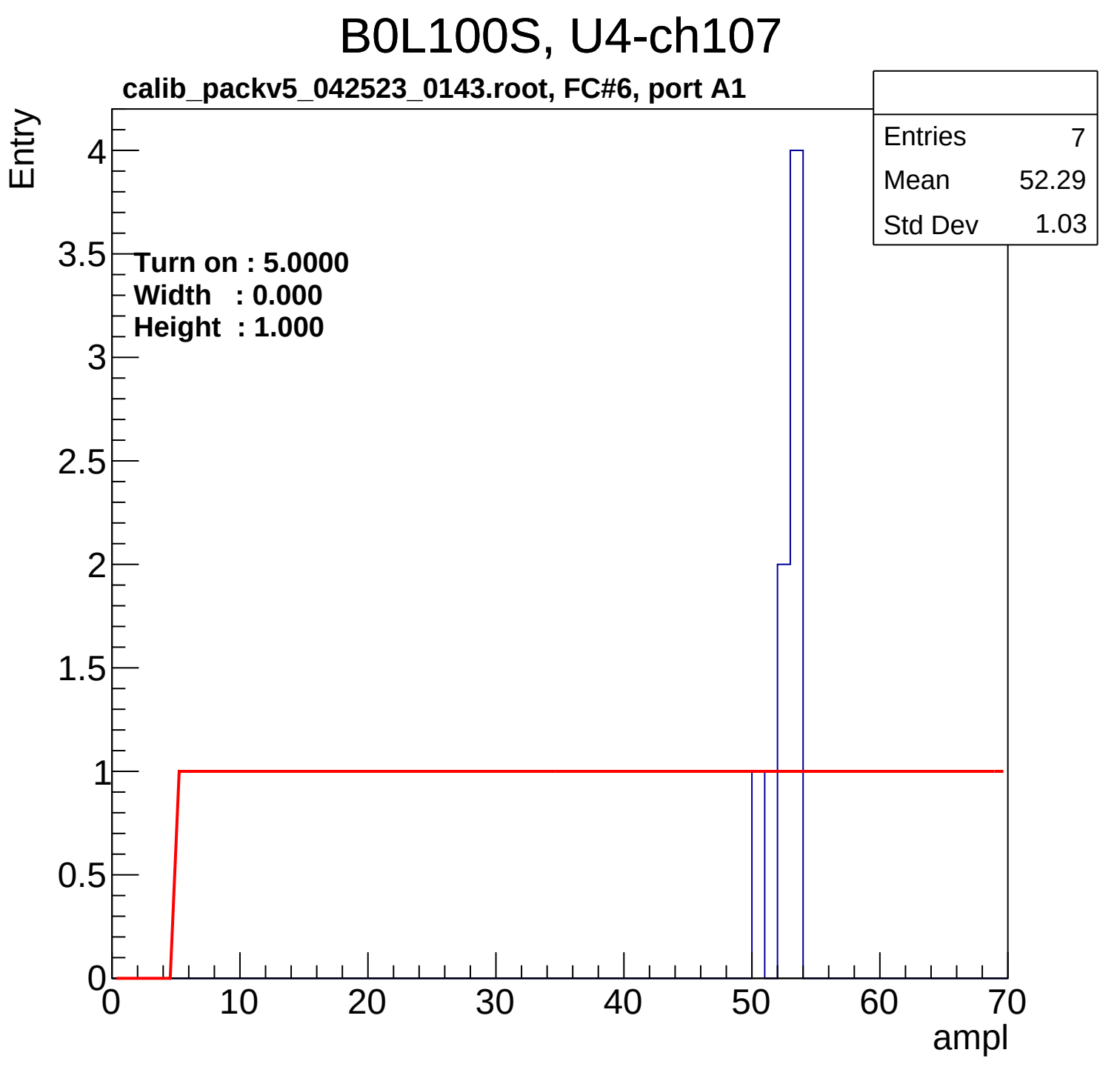

B0L100S, U4-ch102
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

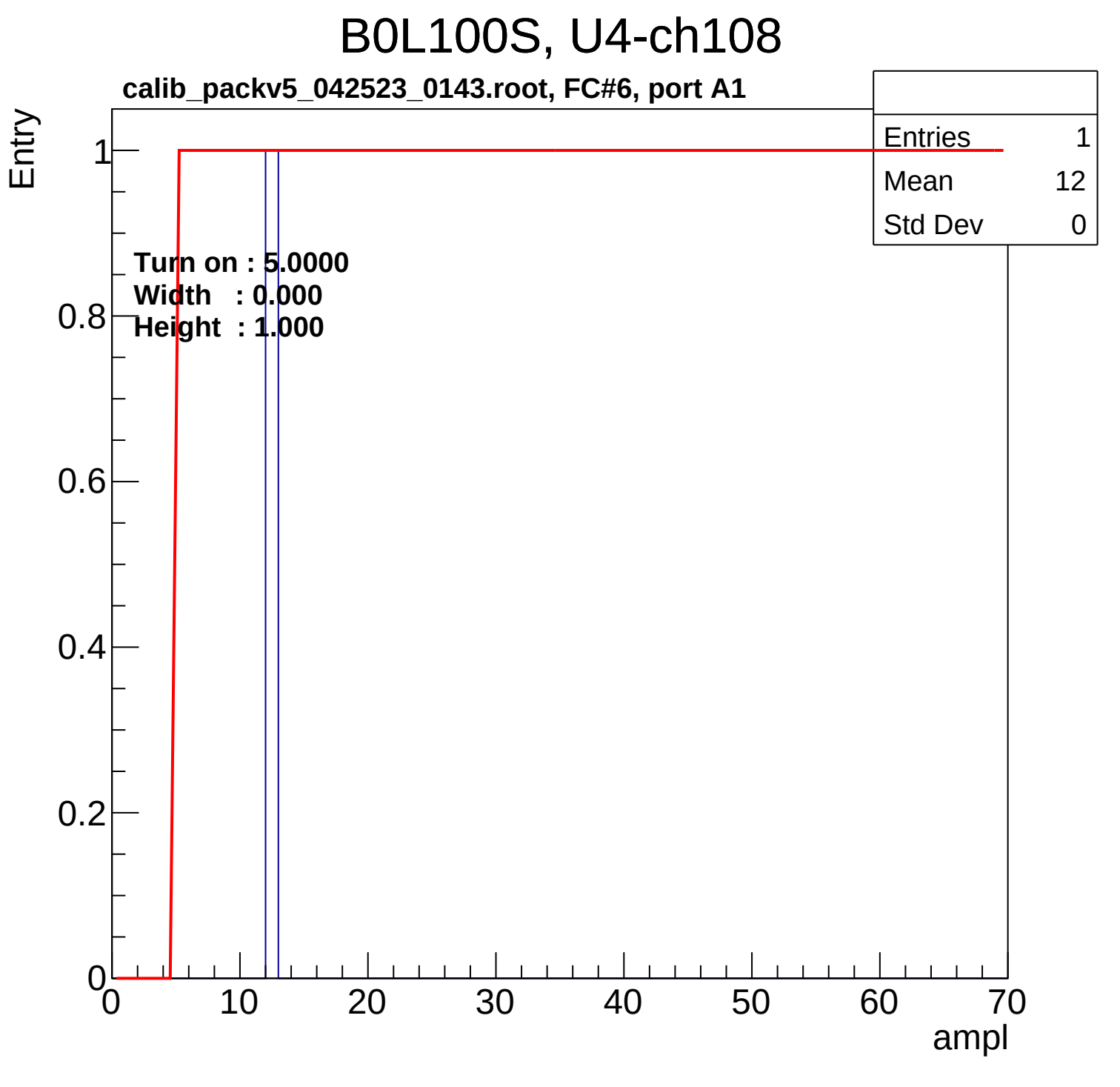

B0L100S, U4-ch103
calib_packv5_042523_0143.root, FC#6, port A1
Entries 18
Mean 49.78
Std Dev 1.75
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

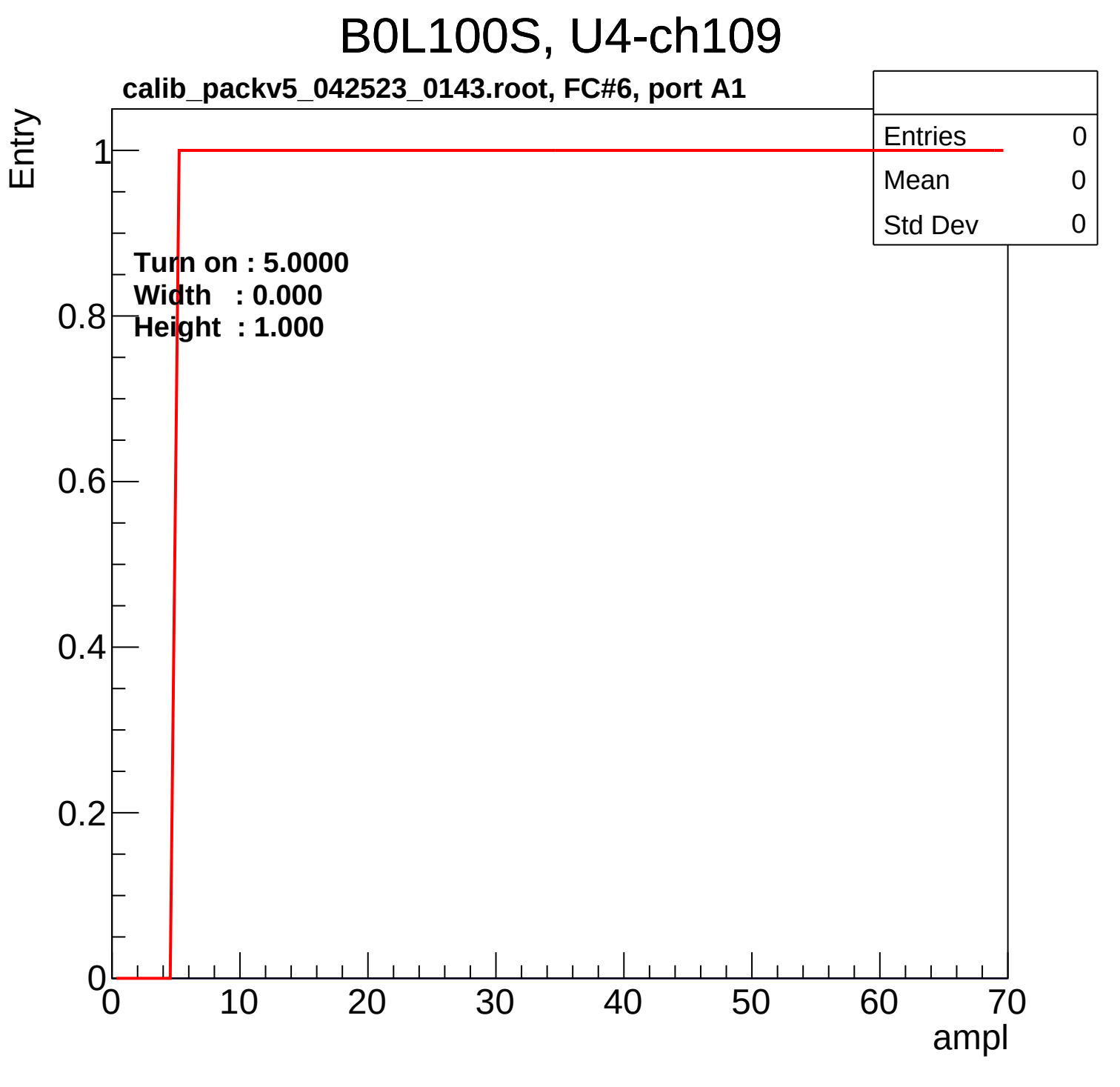

B0L100S, U4-ch104
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

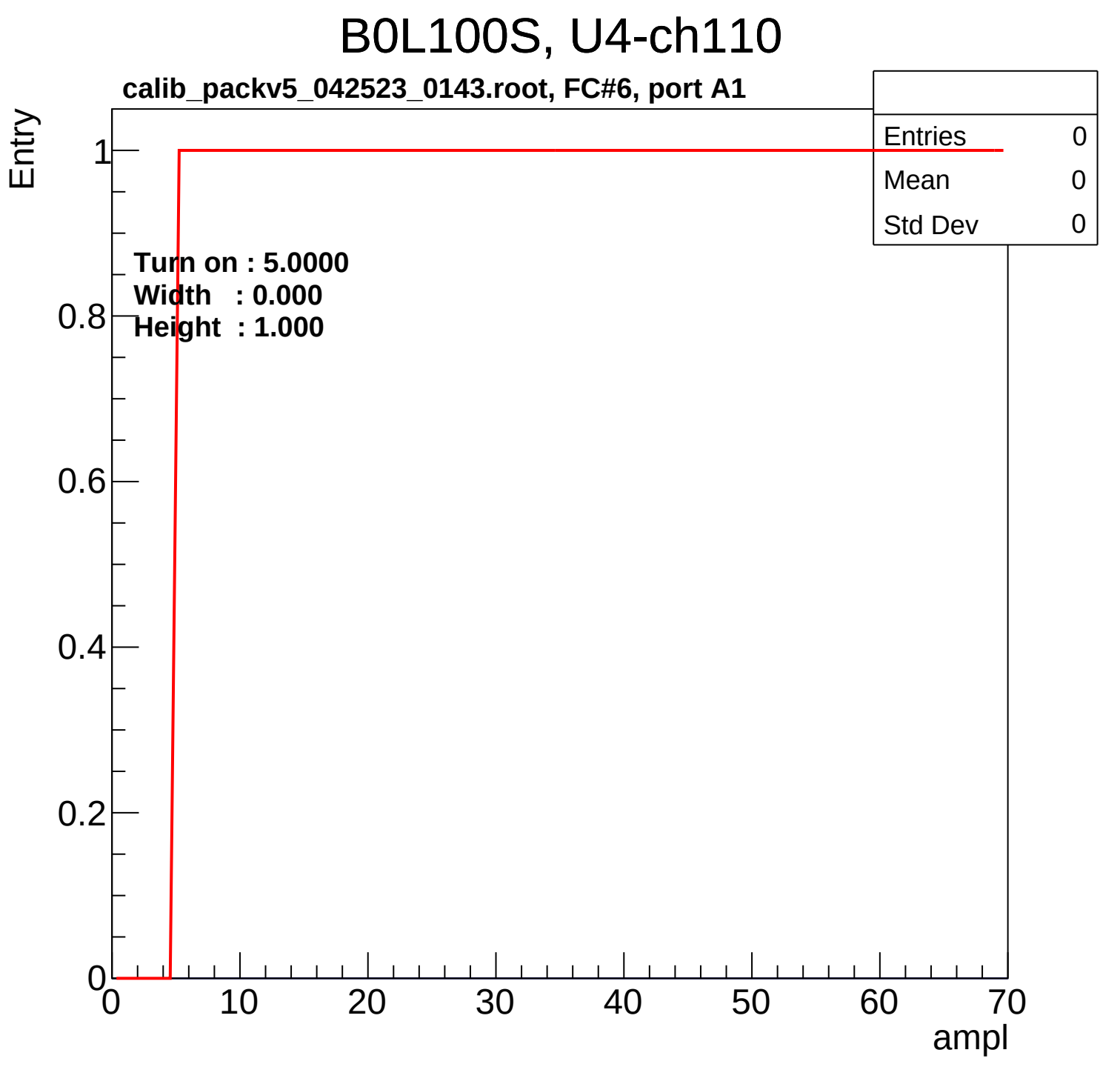

B0L100S, U4-ch105
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

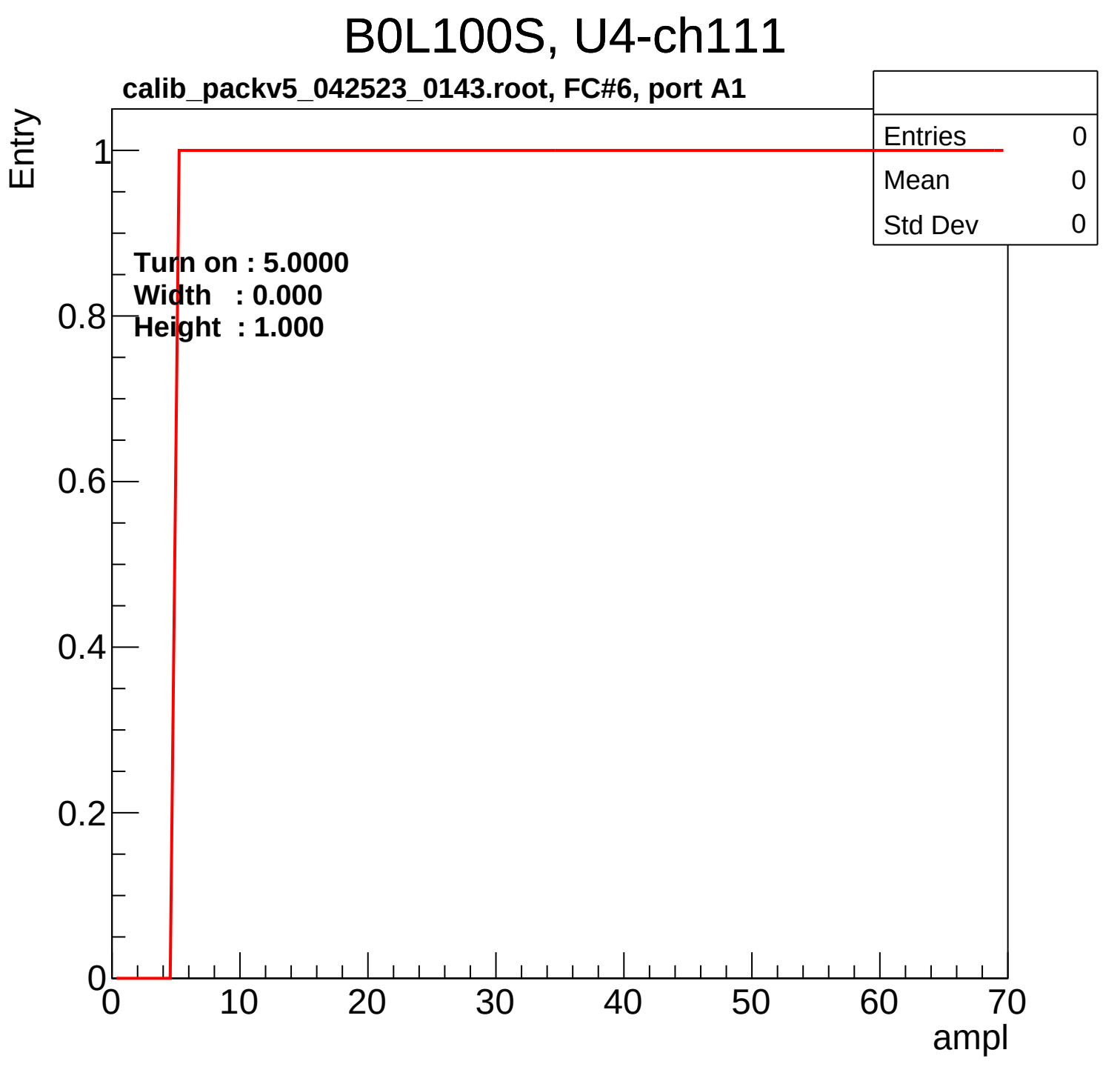

B0L100S, U4-ch106
calib_packv5_042523_0143.root, FC#6, port A1
Entries 18
Mean 50.56
Std Dev 2.114
Turn on : 16.9398
Width : 0.783
Height : 2.222
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

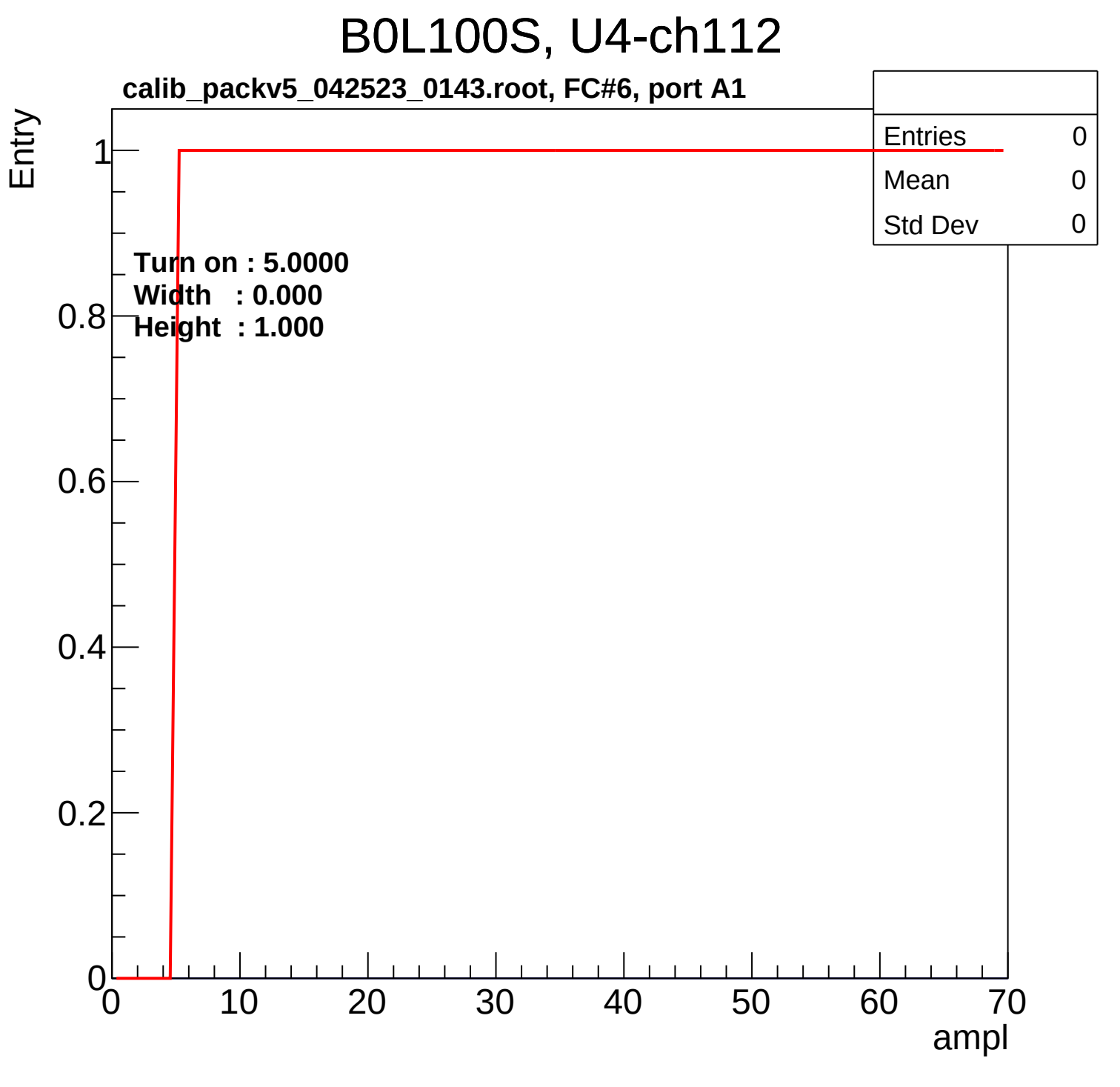

B0L100S, U4-ch107
calib_packv5_042523_0143.root, FC#6, port A1
Entries 7
Mean 52.29
Std Dev 1.03
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

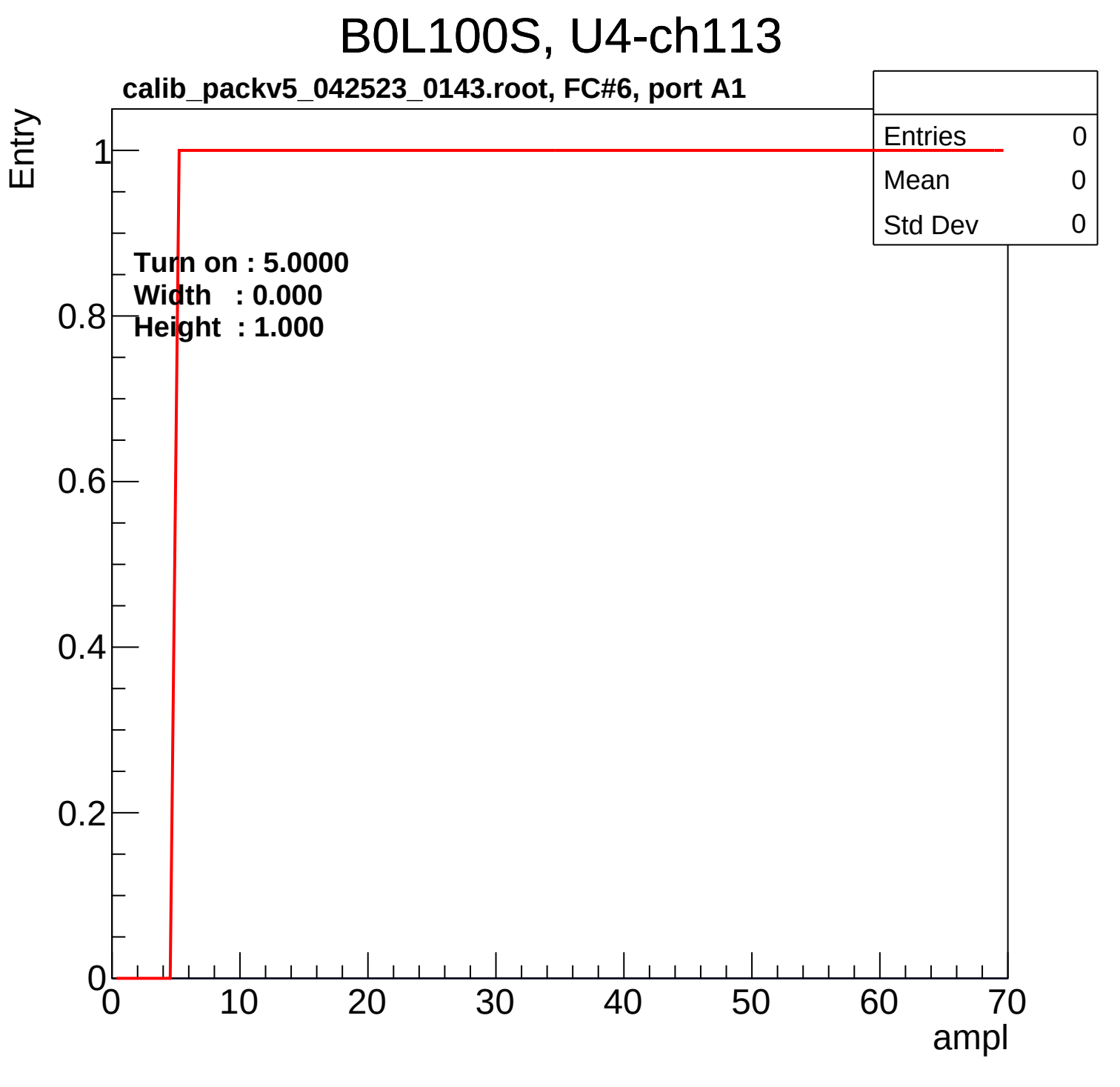

B0L100S, U4-ch108
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 12
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

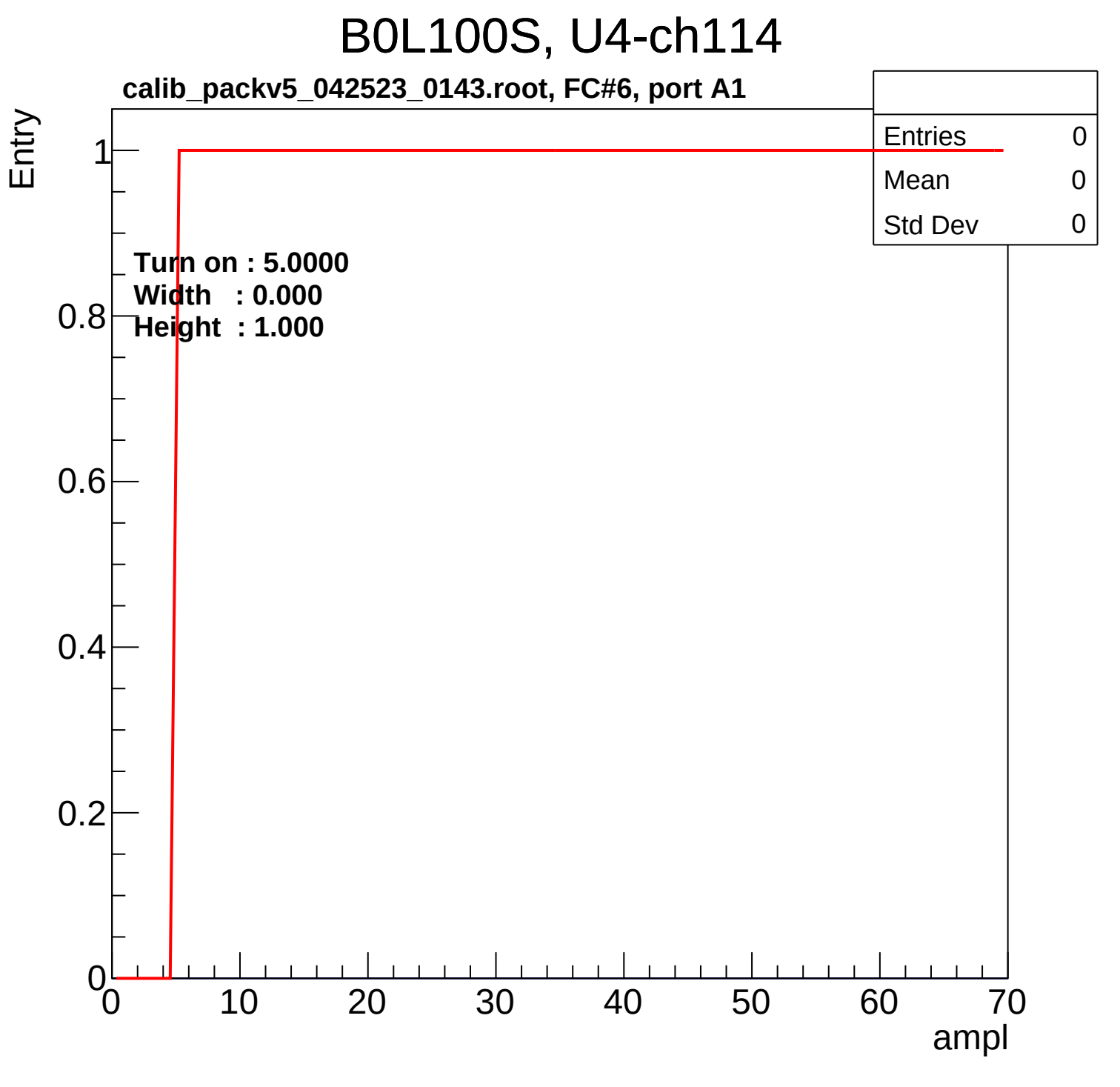

B0L100S, U4-ch109
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

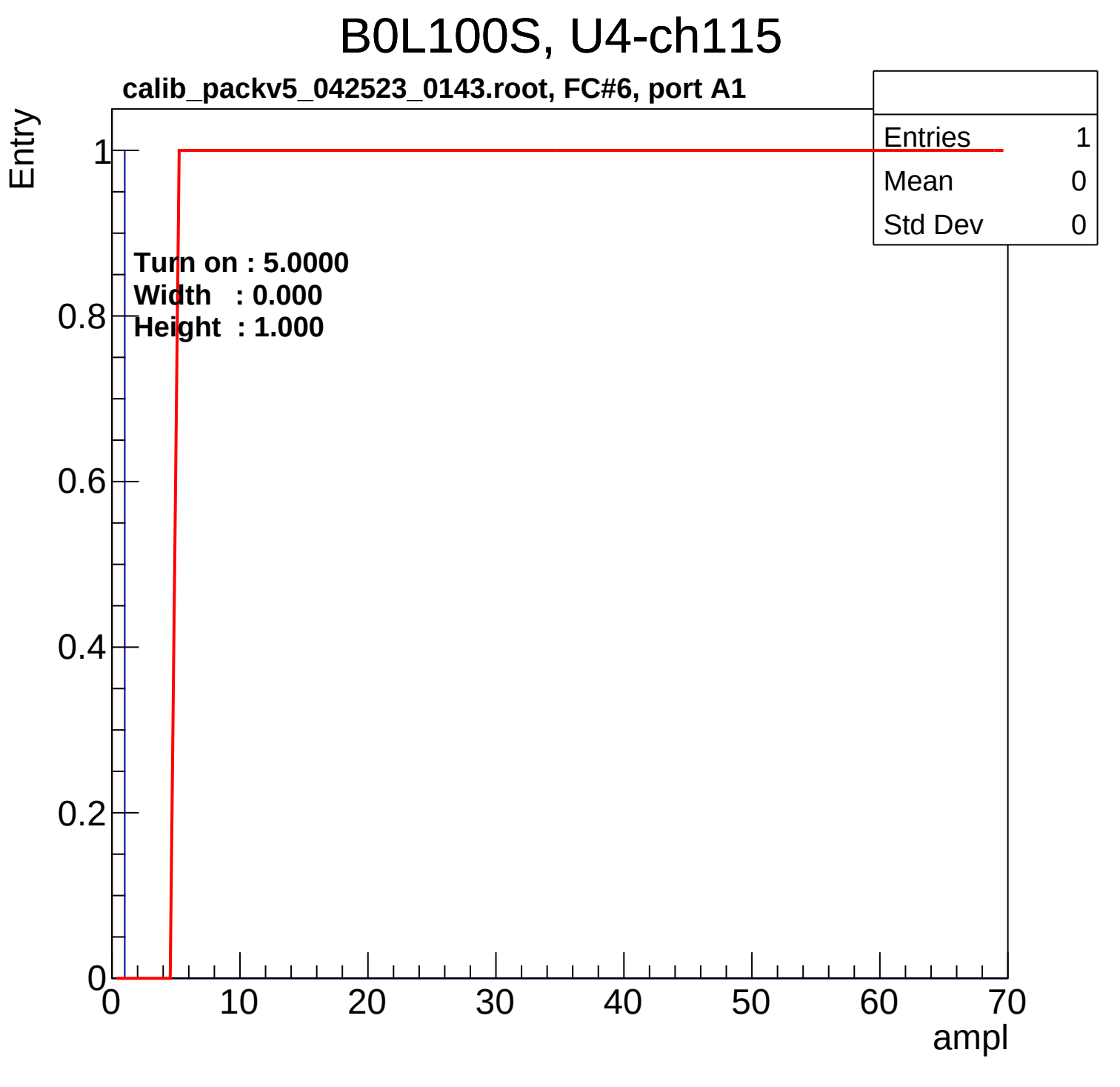

B0L100S, U4-ch110
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

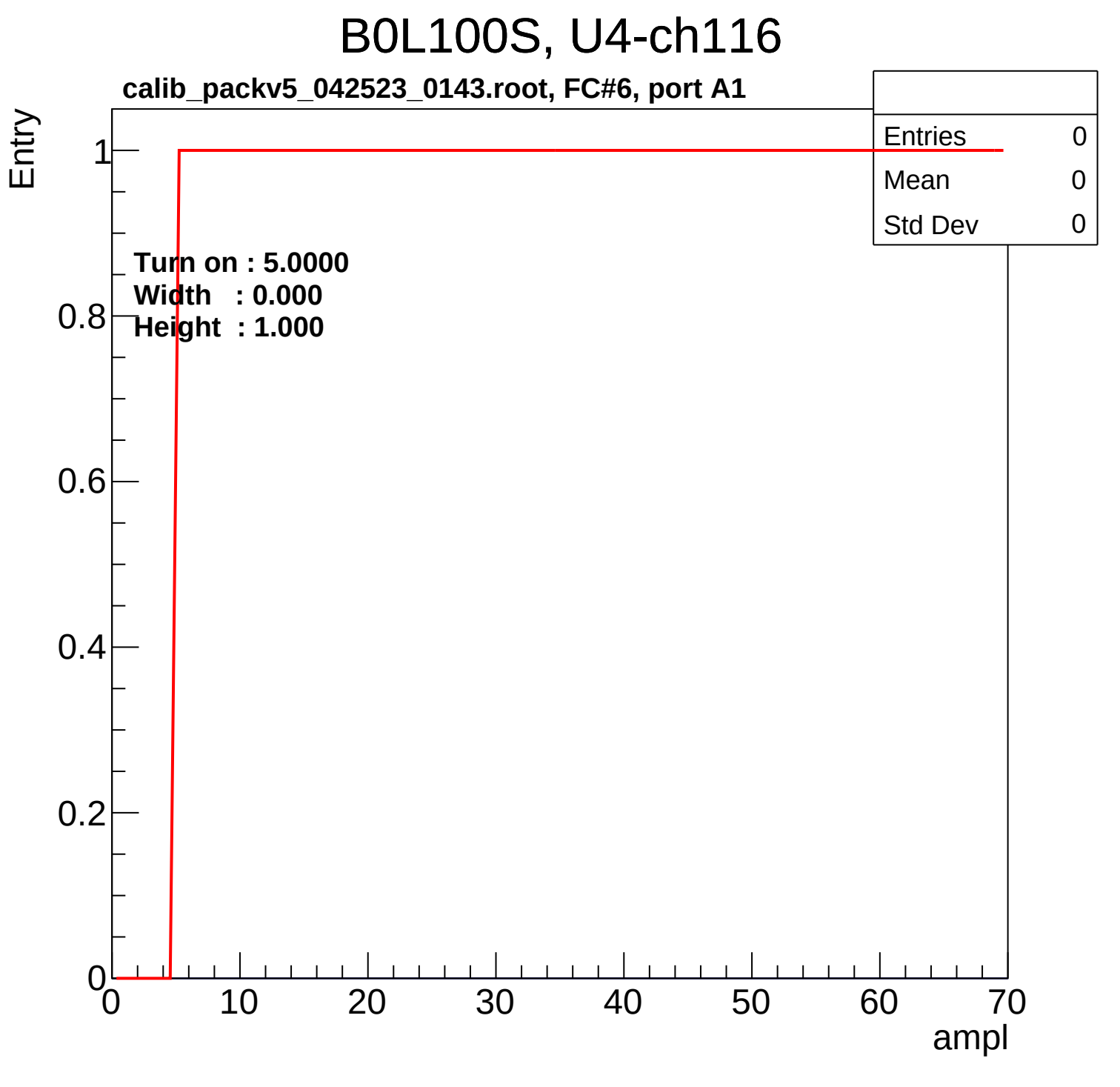

B0L100S, U4-ch111
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

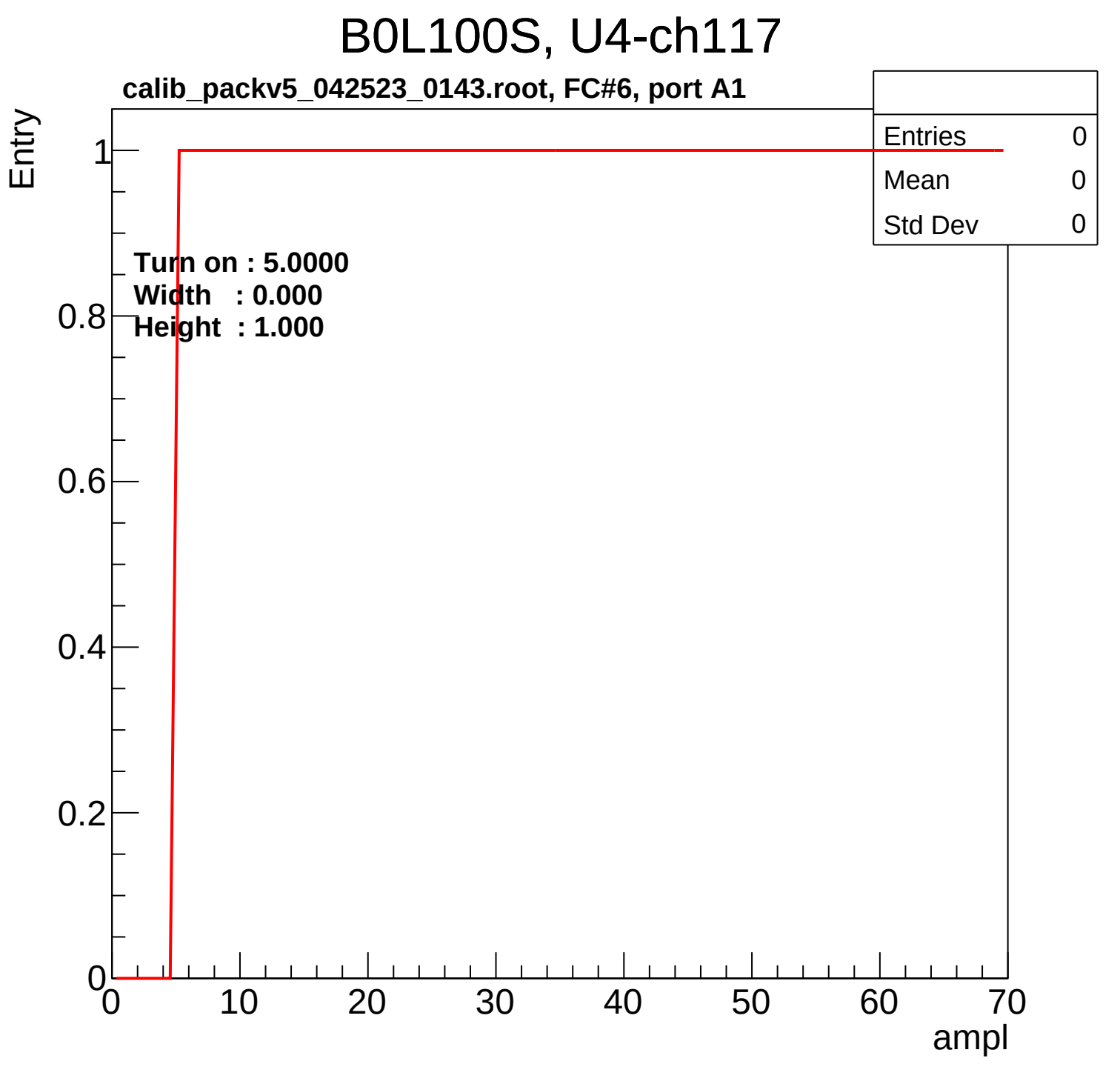

B0L100S, U4-ch112
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U4-ch113
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U4-ch114
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U4-ch115
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U4-ch116
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U4-ch117
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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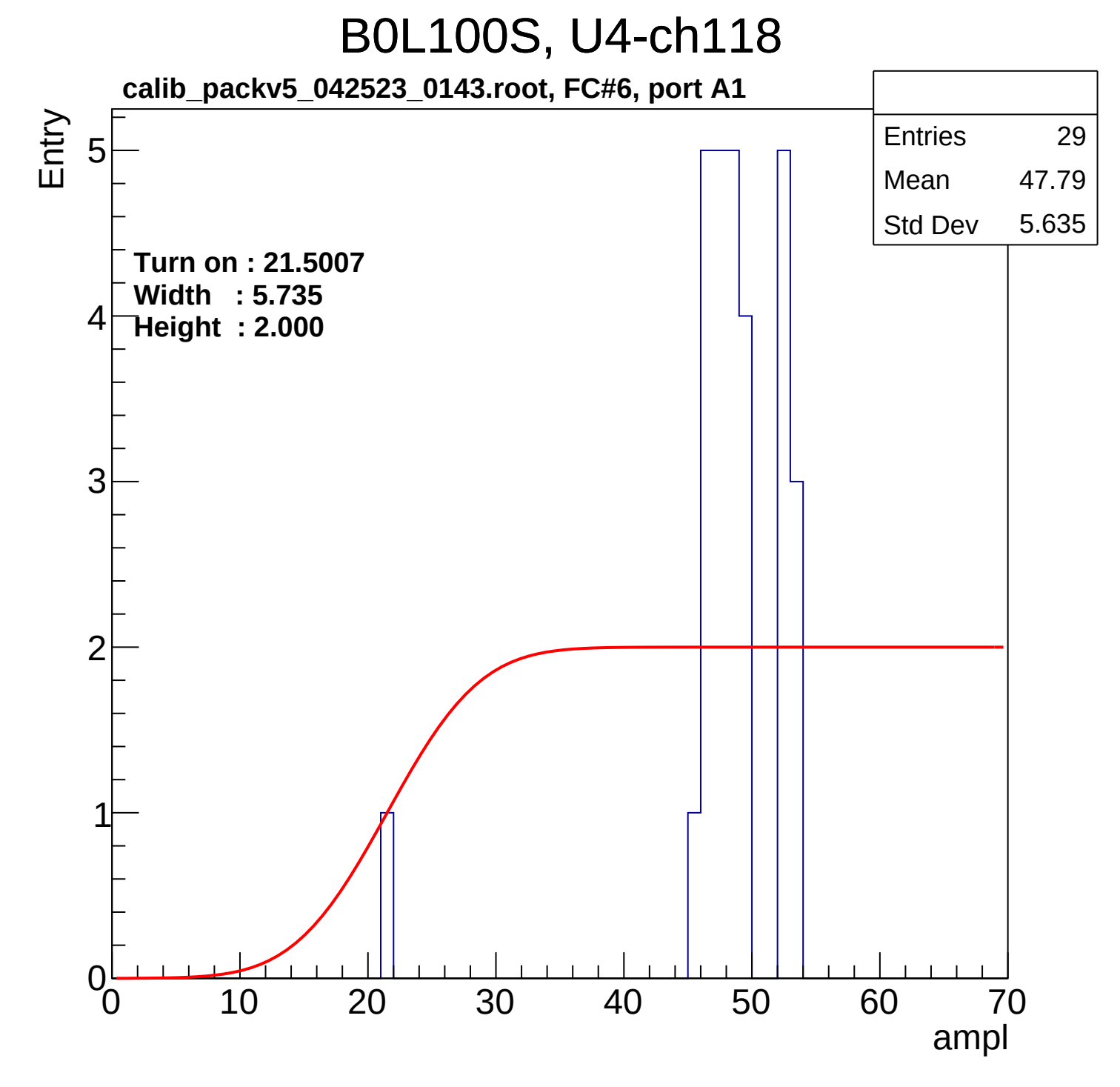
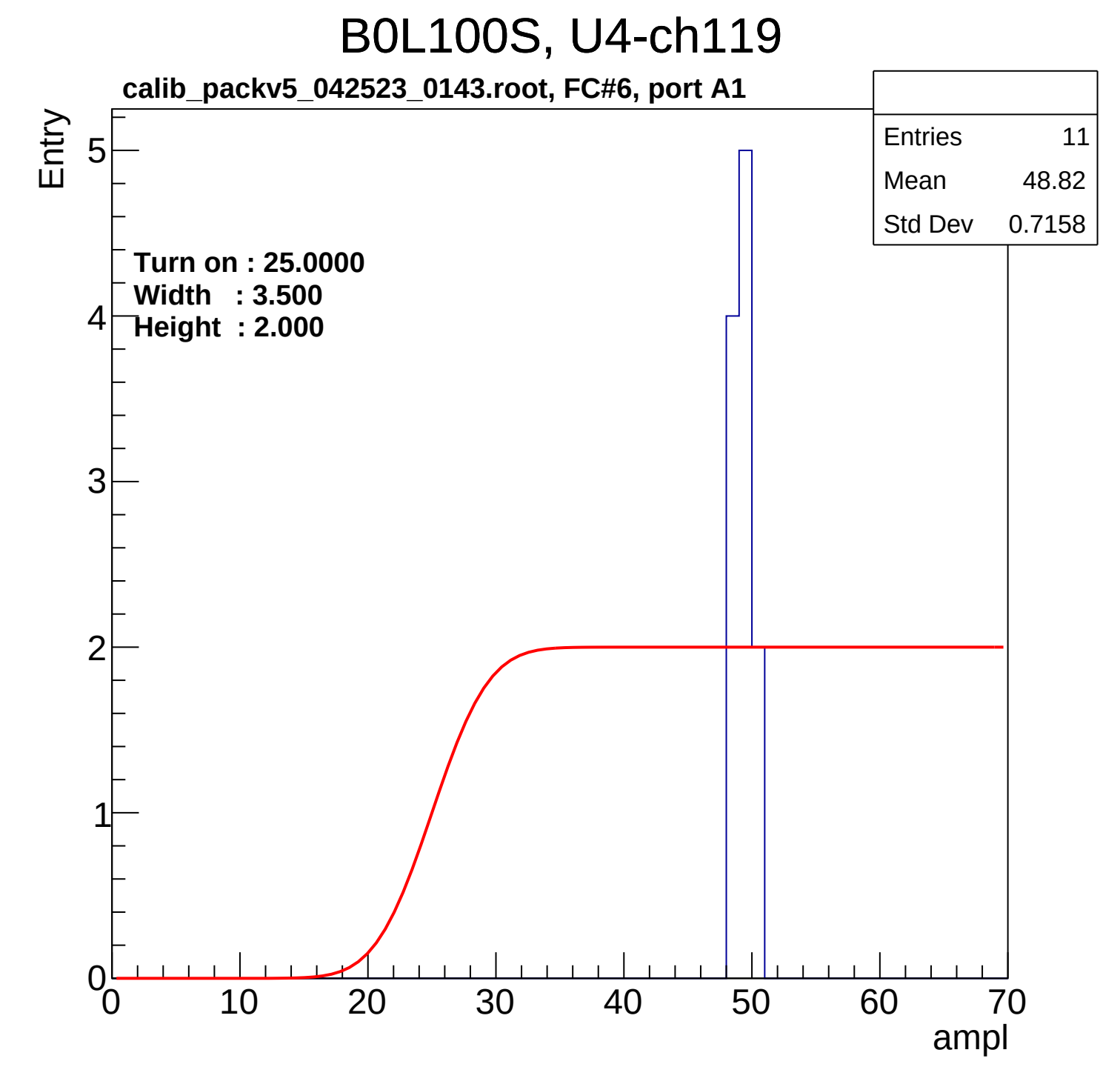
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U4-ch118
calib_packv5_042523_0143.root, FC#6, port A1
Entries 29
Mean 47.79
Std Dev 5.635
Turn on : 21.5007
Width : 5.735
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B0L100S, U4-ch119
calib_packv5_042523_0143.root, FC#6, port A1
Entries 11
Mean 48.82
Std Dev 0.7158
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
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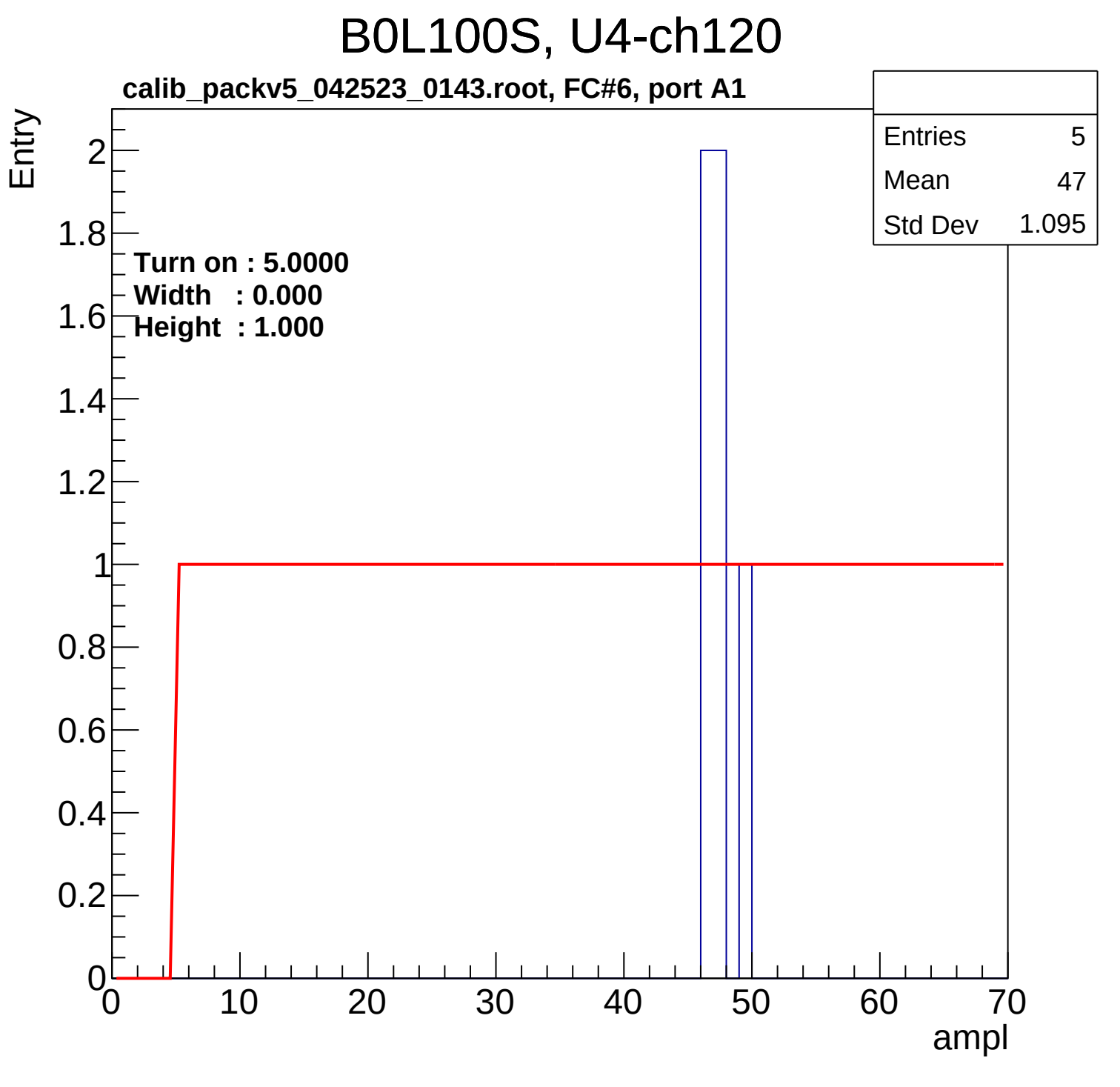
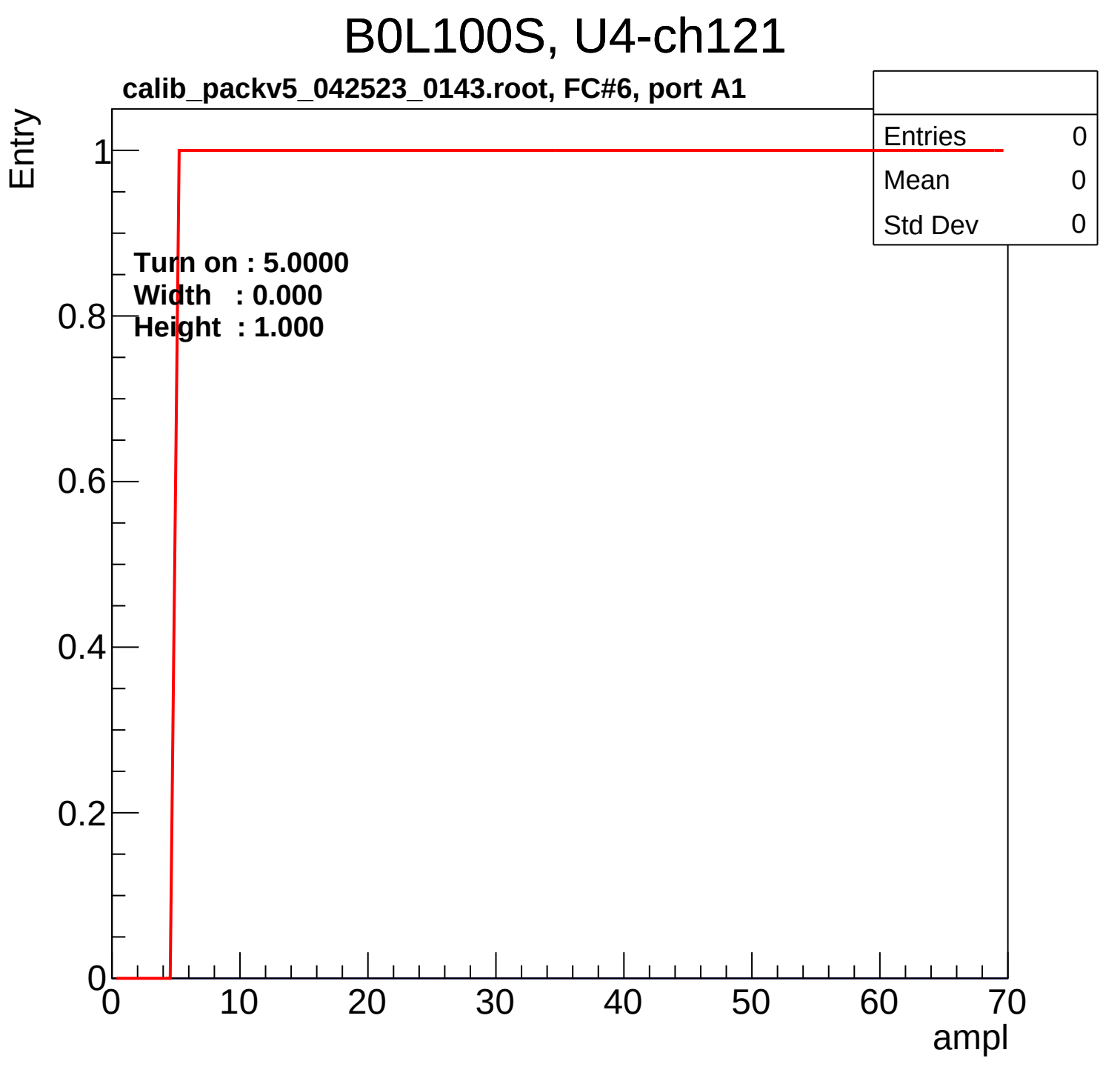
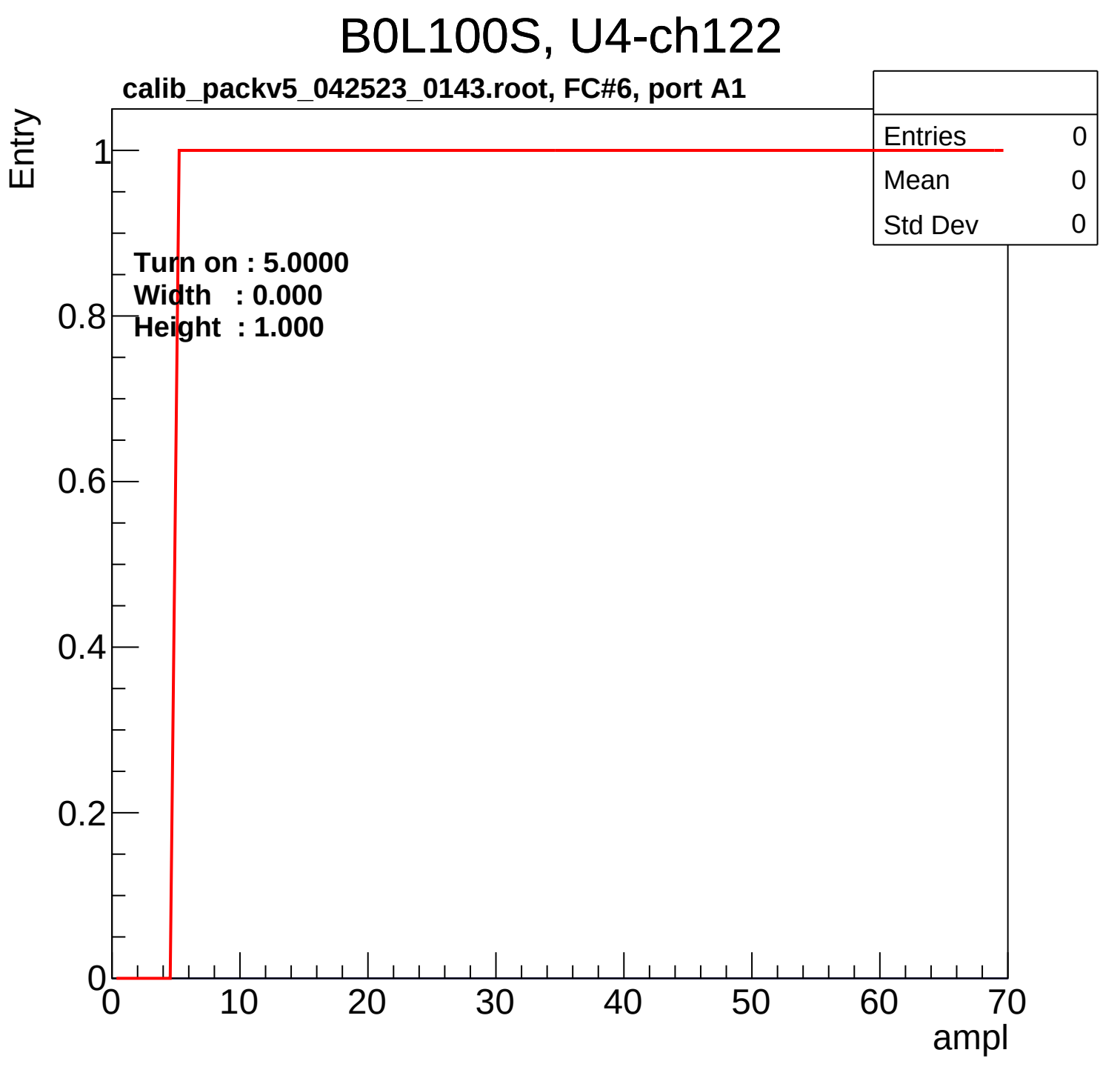
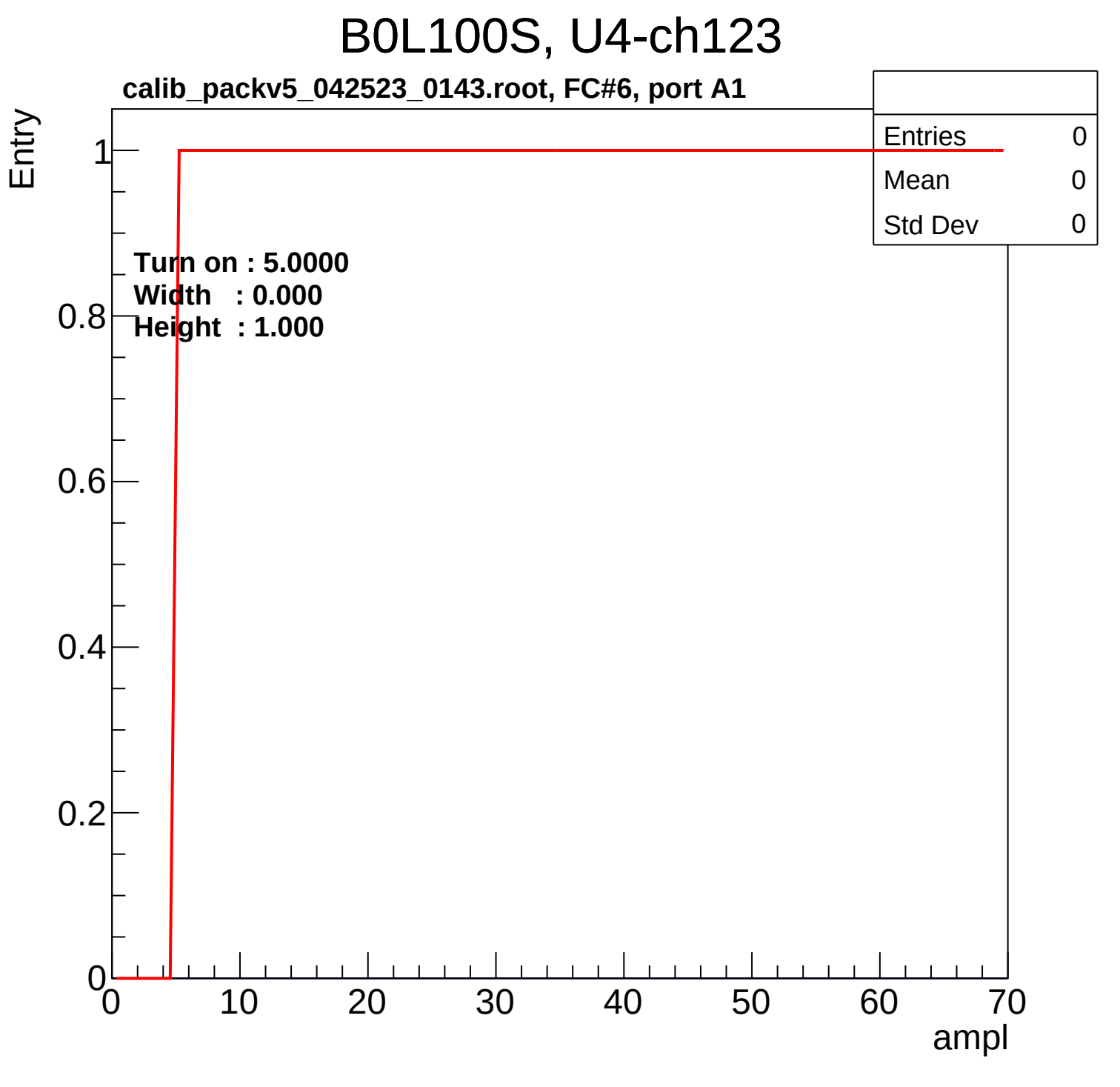
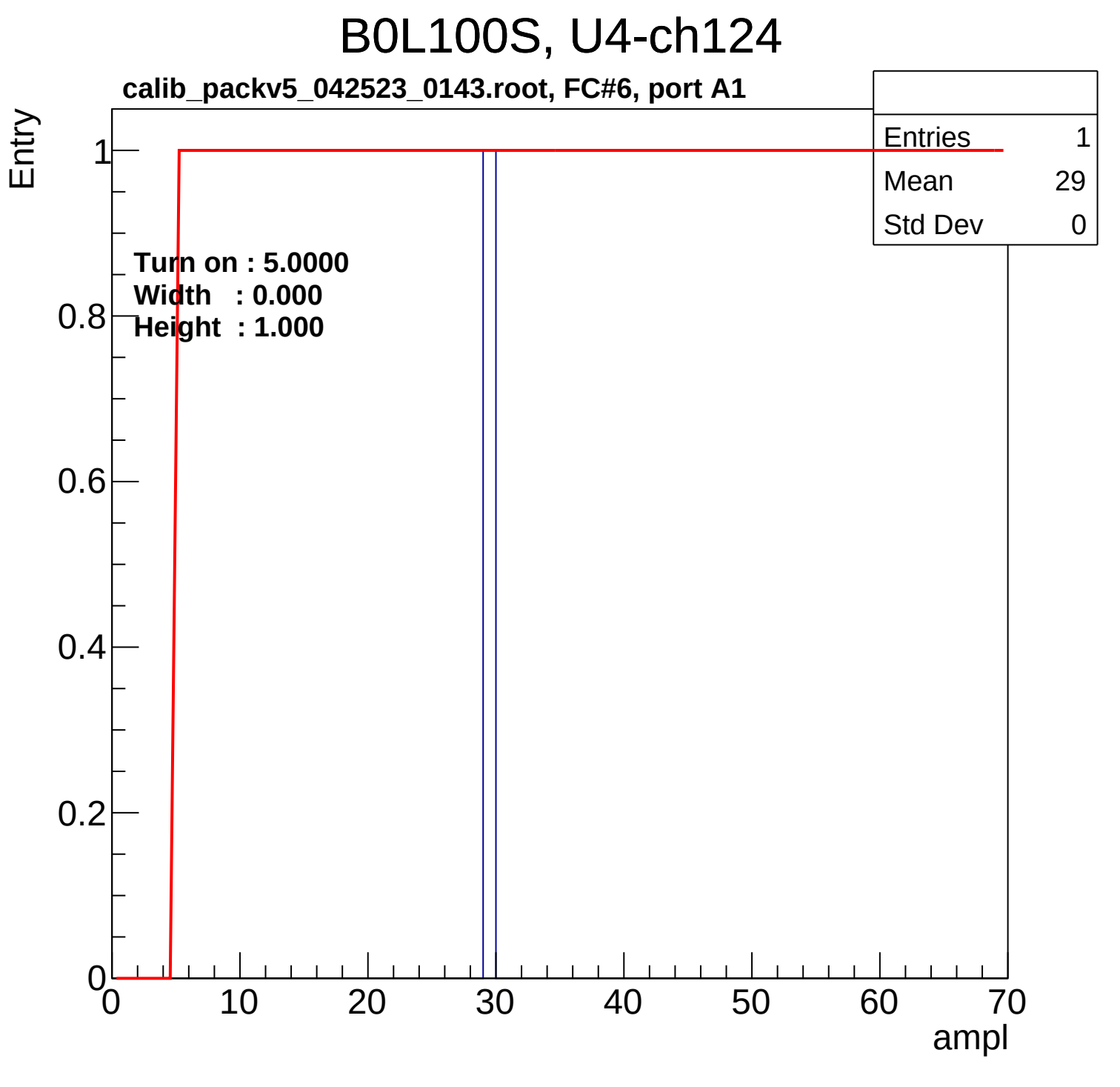
60
70

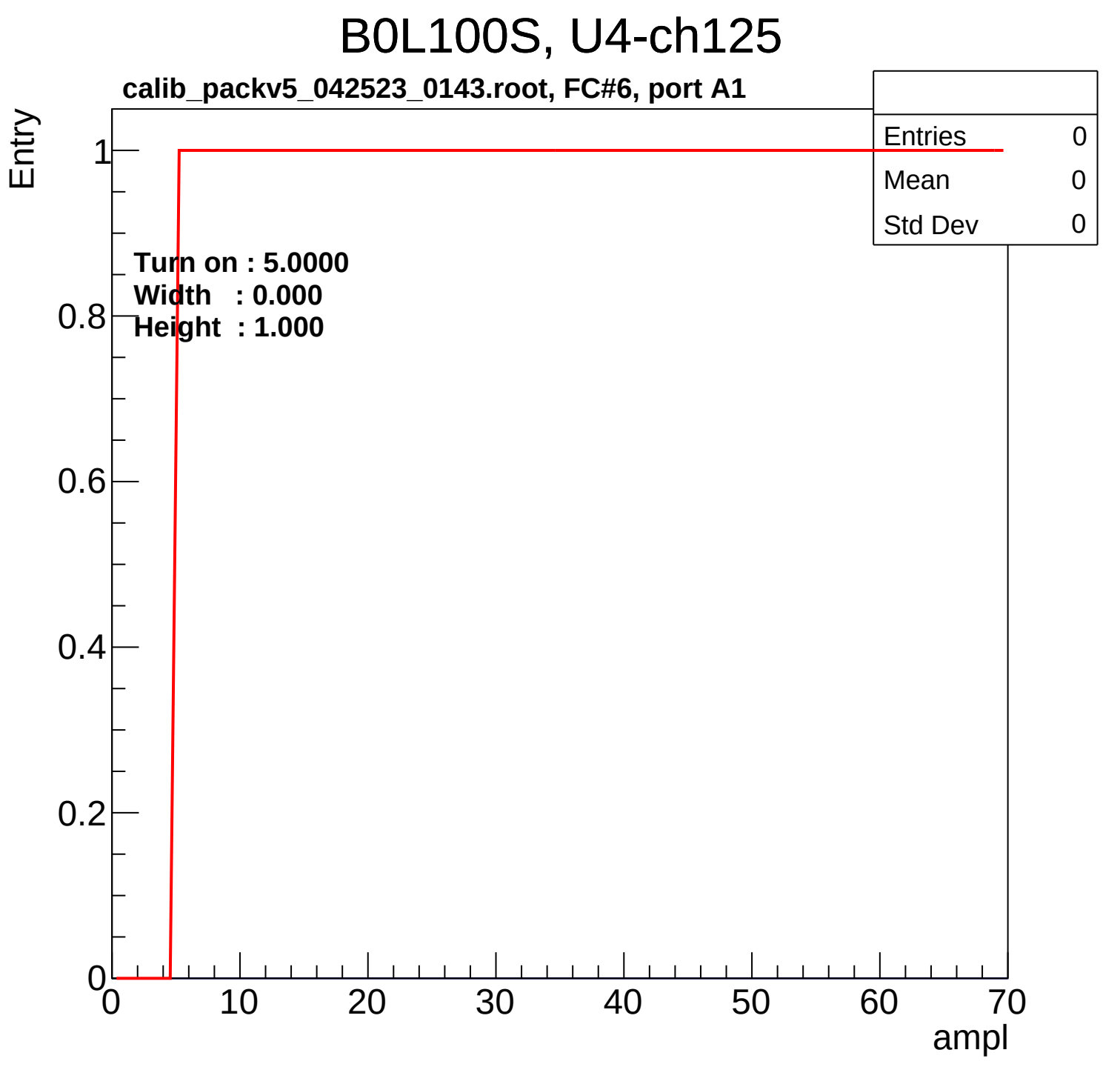

B0L100S, U4-ch120
calib_packv5_042523_0143.root, FC#6, port A1
Entries 5
Mean 47
Std Dev 1.095
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

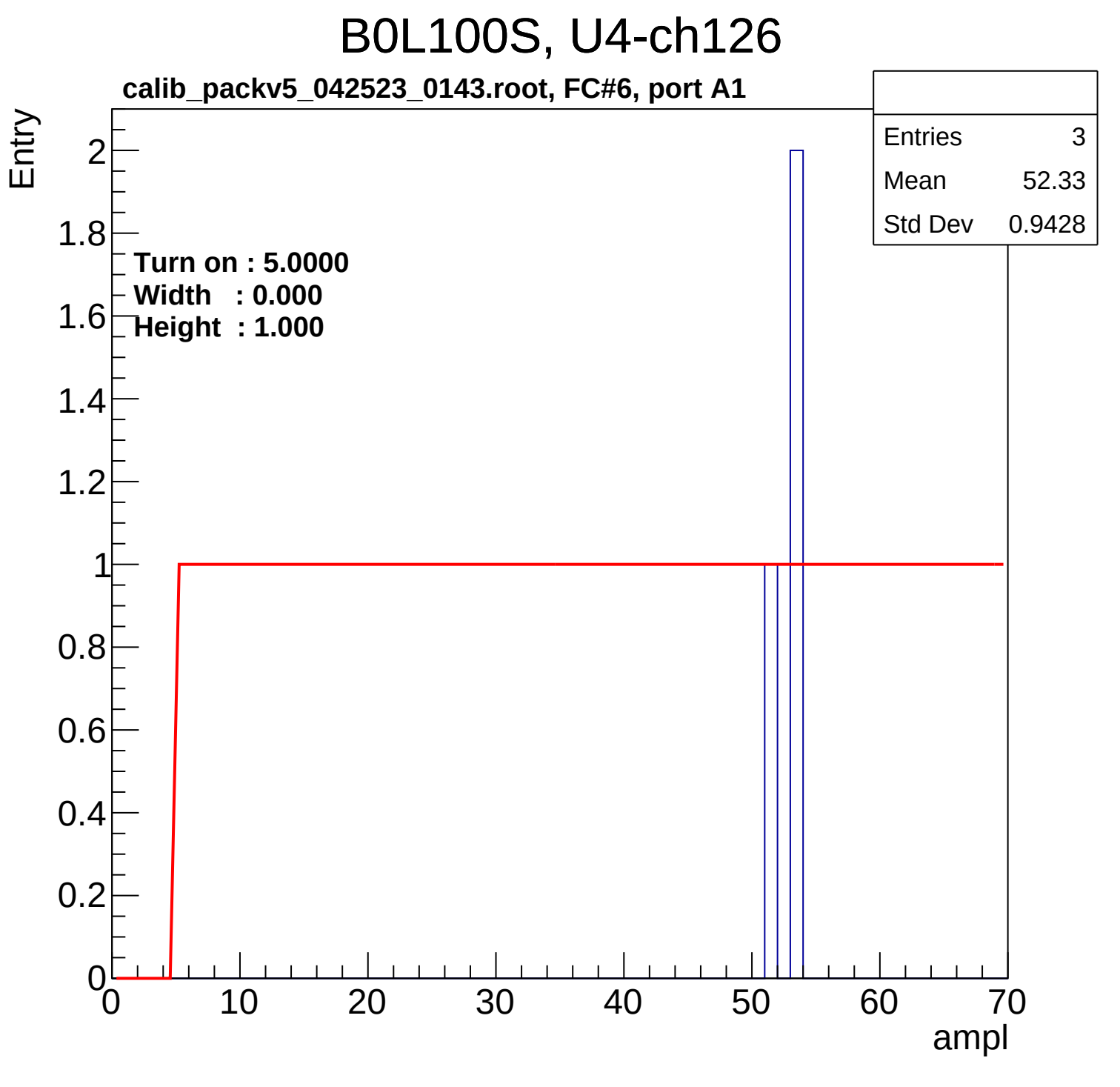

B0L100S, U4-ch121
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

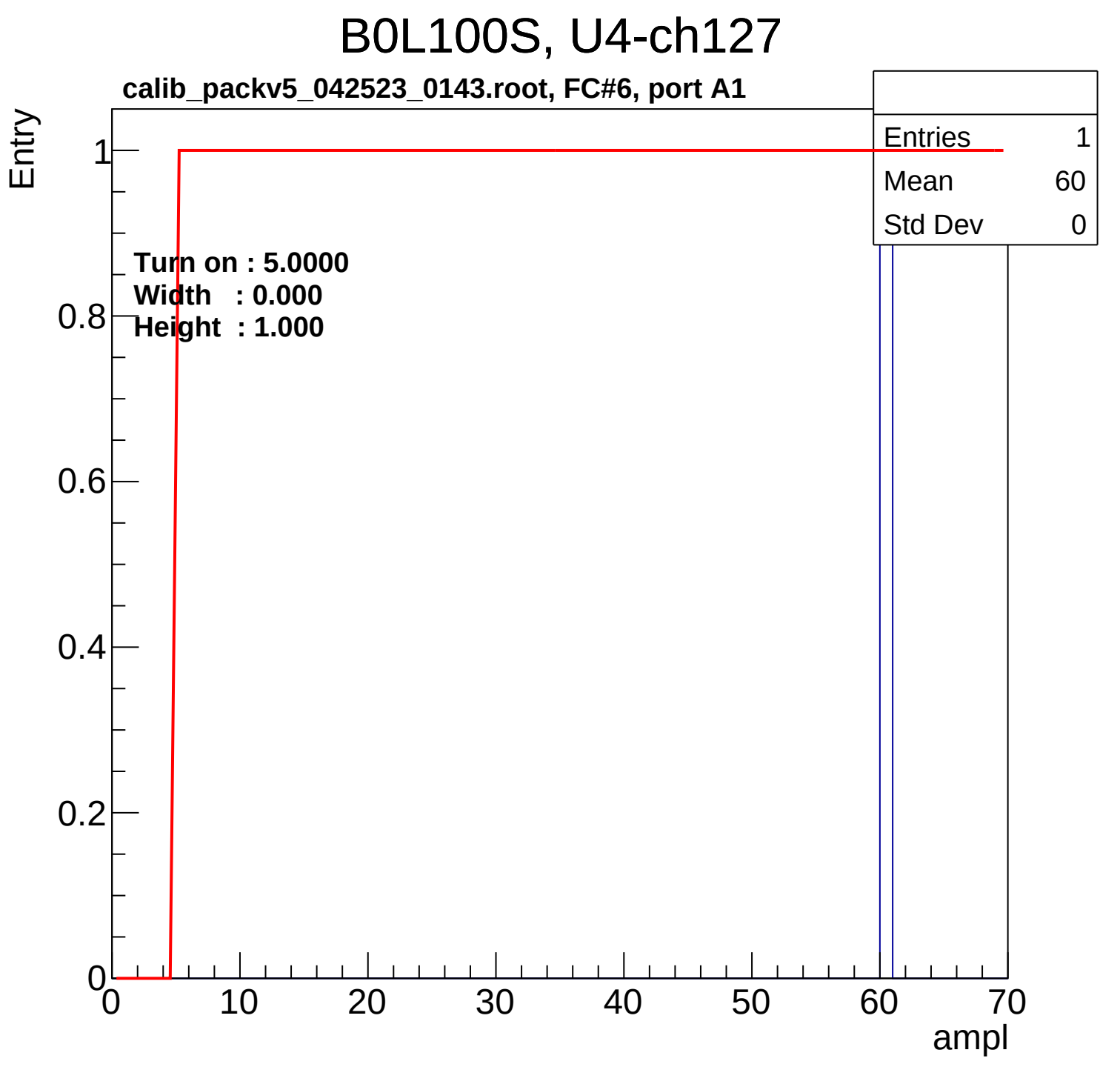

B0L100S, U4-ch122
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

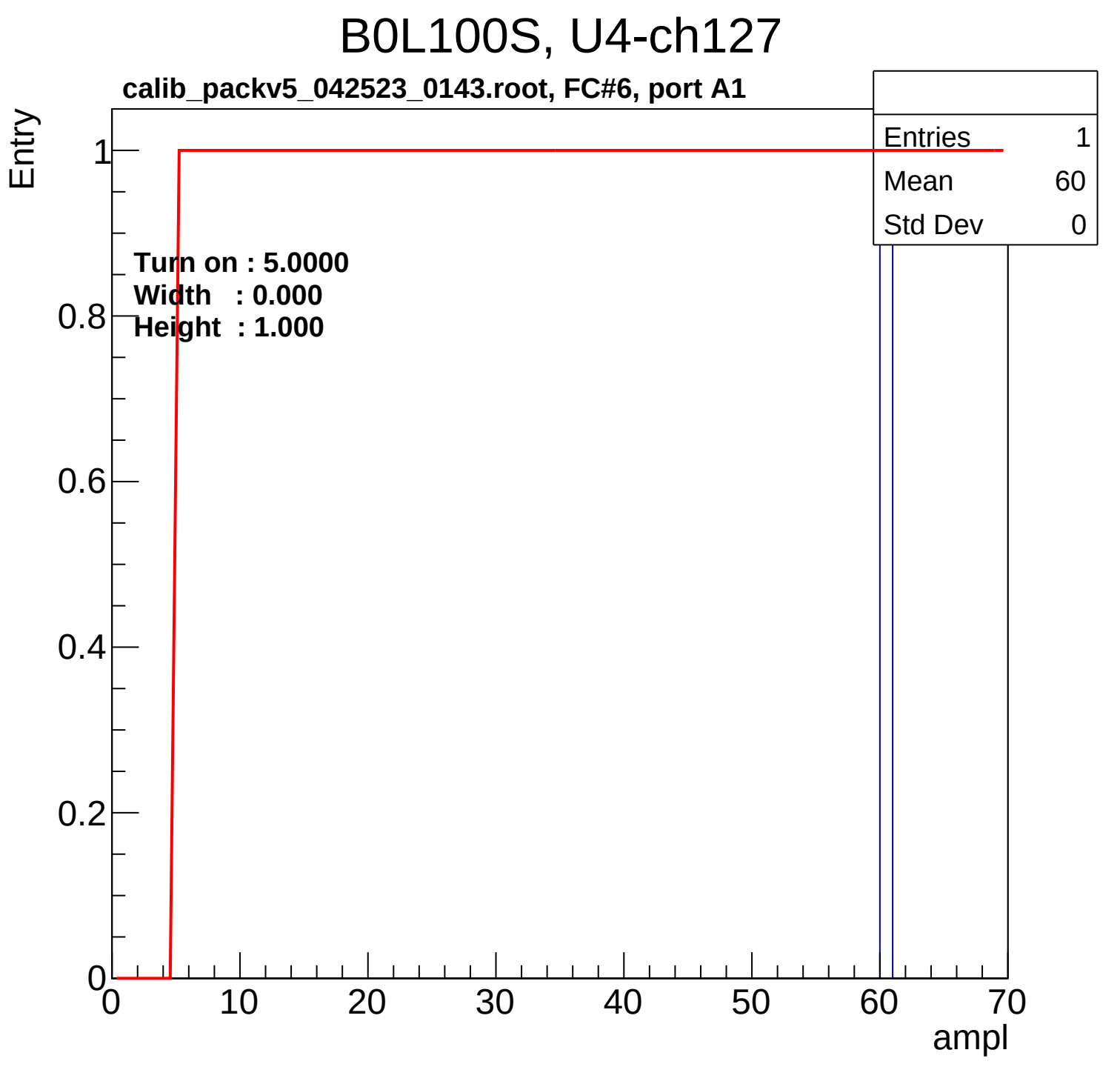

B0L100S, U4-ch123
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U4-ch124
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 29
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U4-ch125
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U4-ch126
calib_packv5_042523_0143.root, FC#6, port A1
Entries 3
Mean 52.33
Std Dev 0.9428
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L100S, U4-ch127
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 60
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U4-ch127
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 60
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70