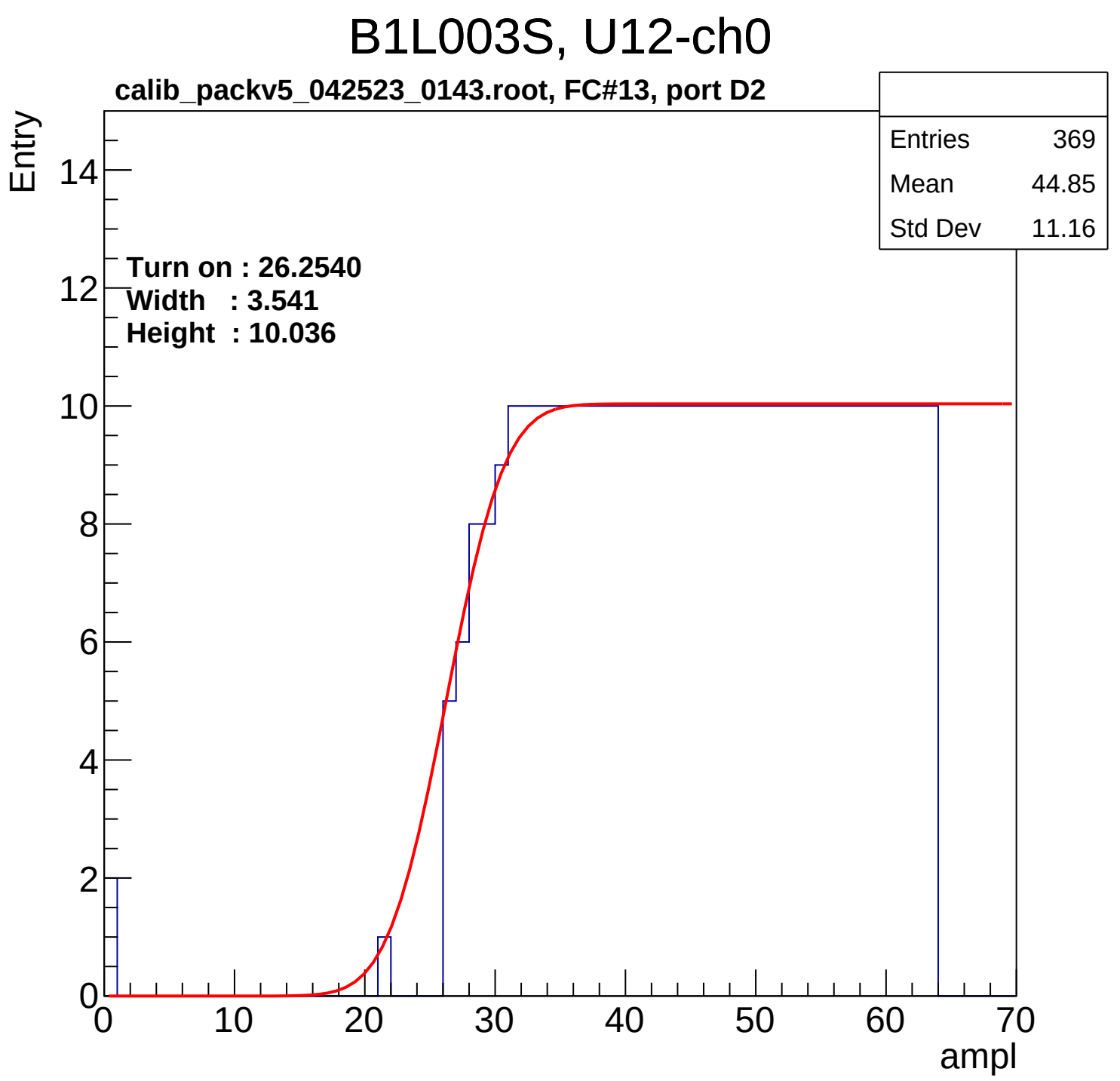
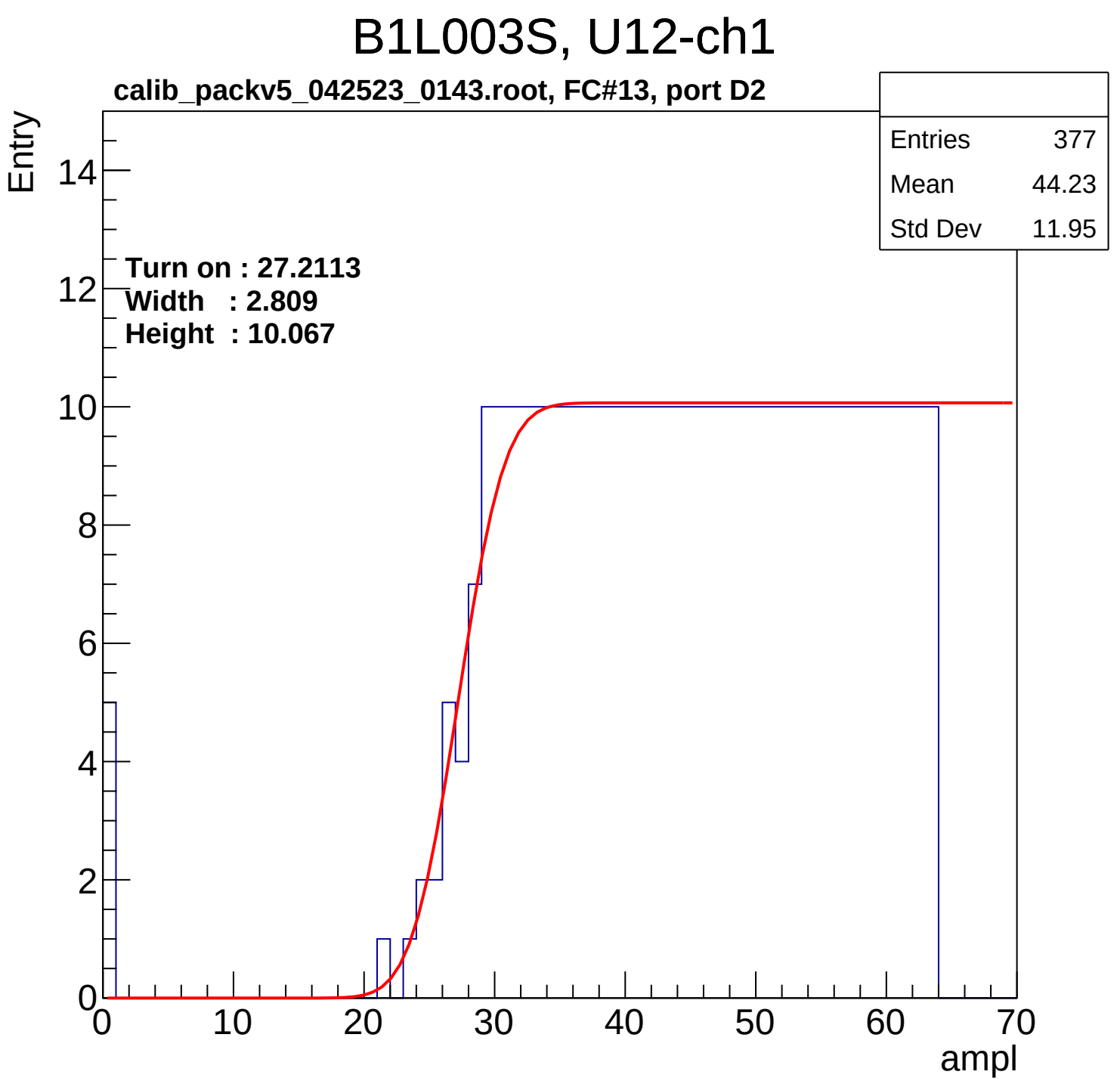
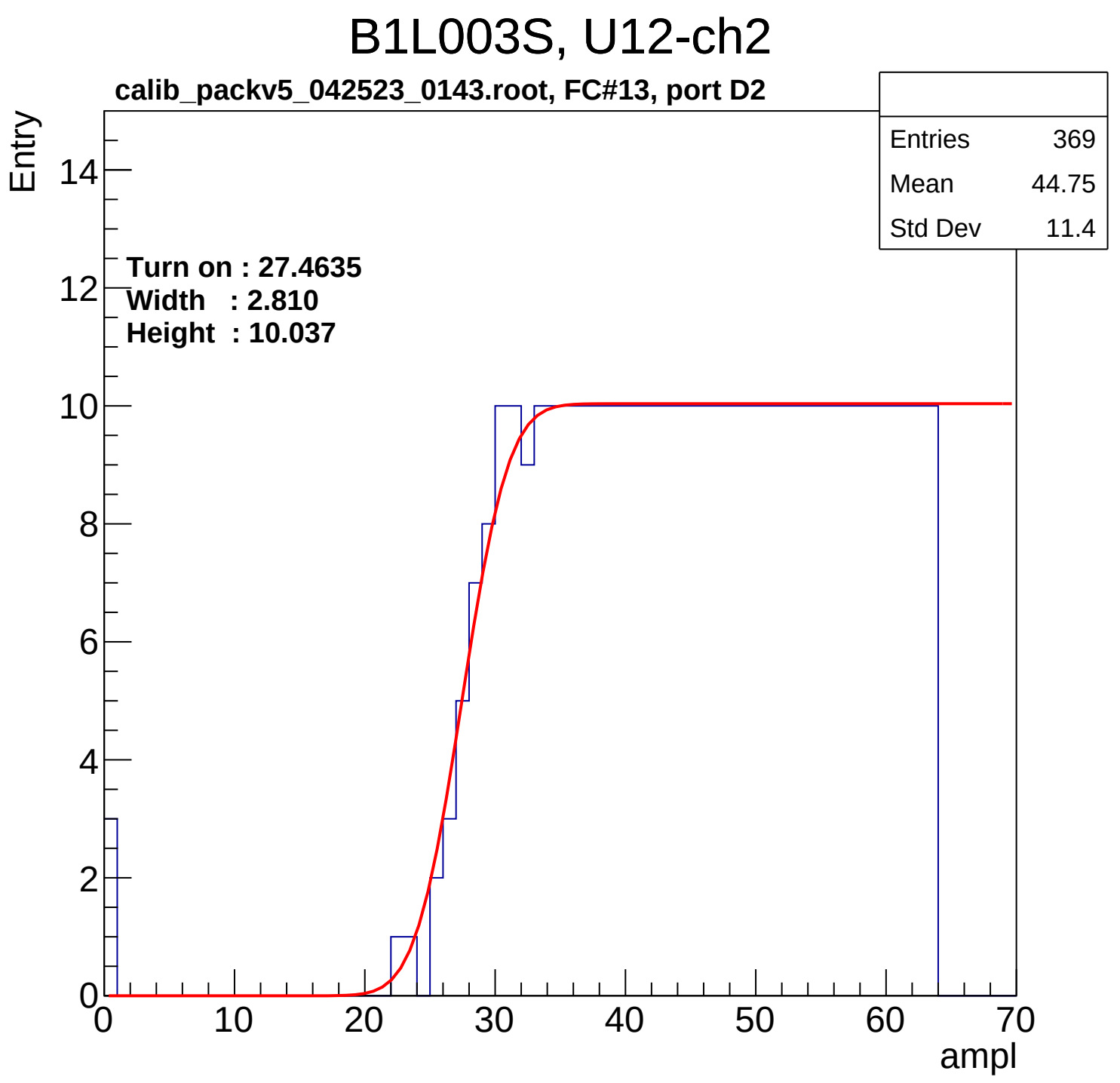
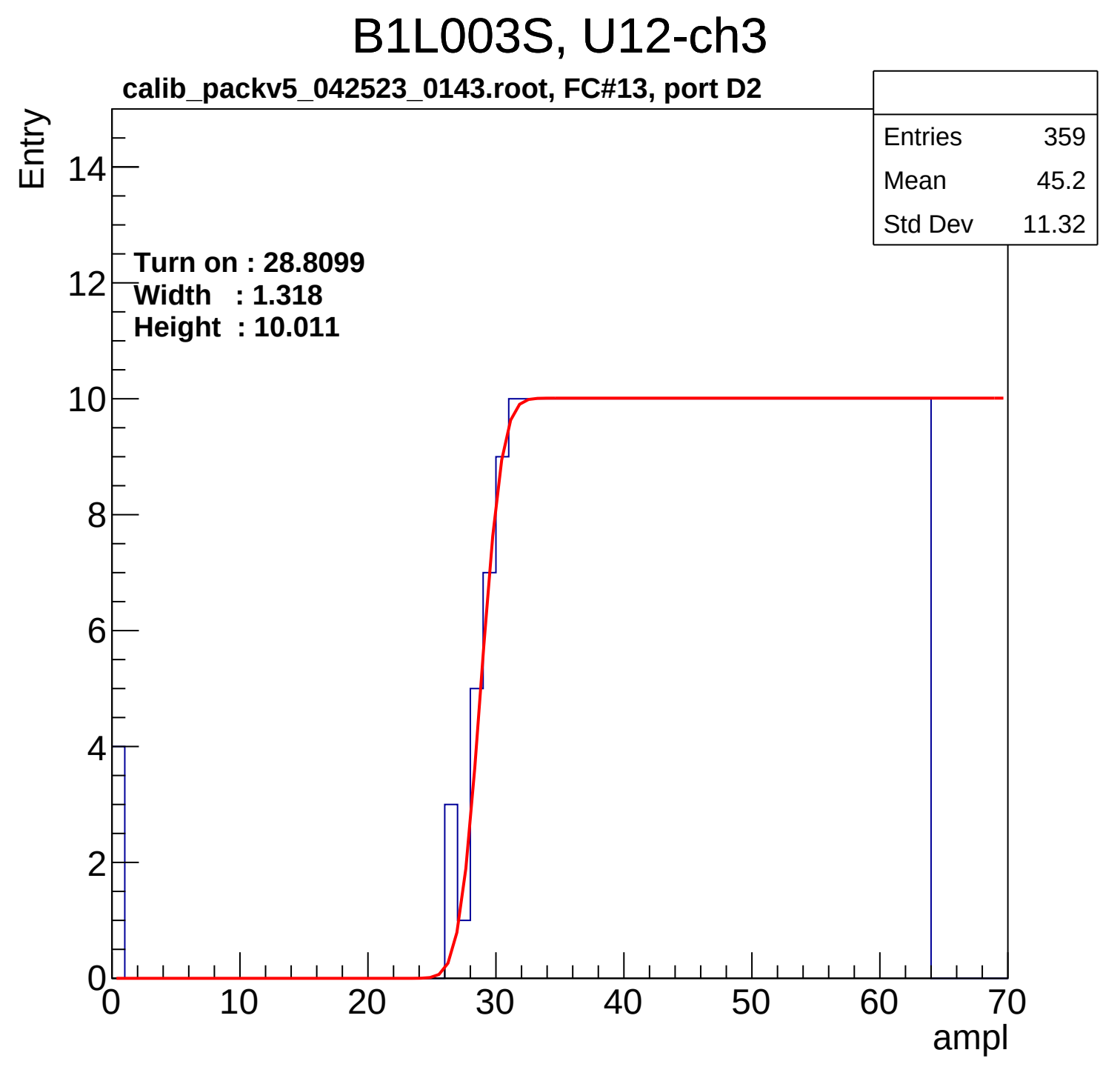
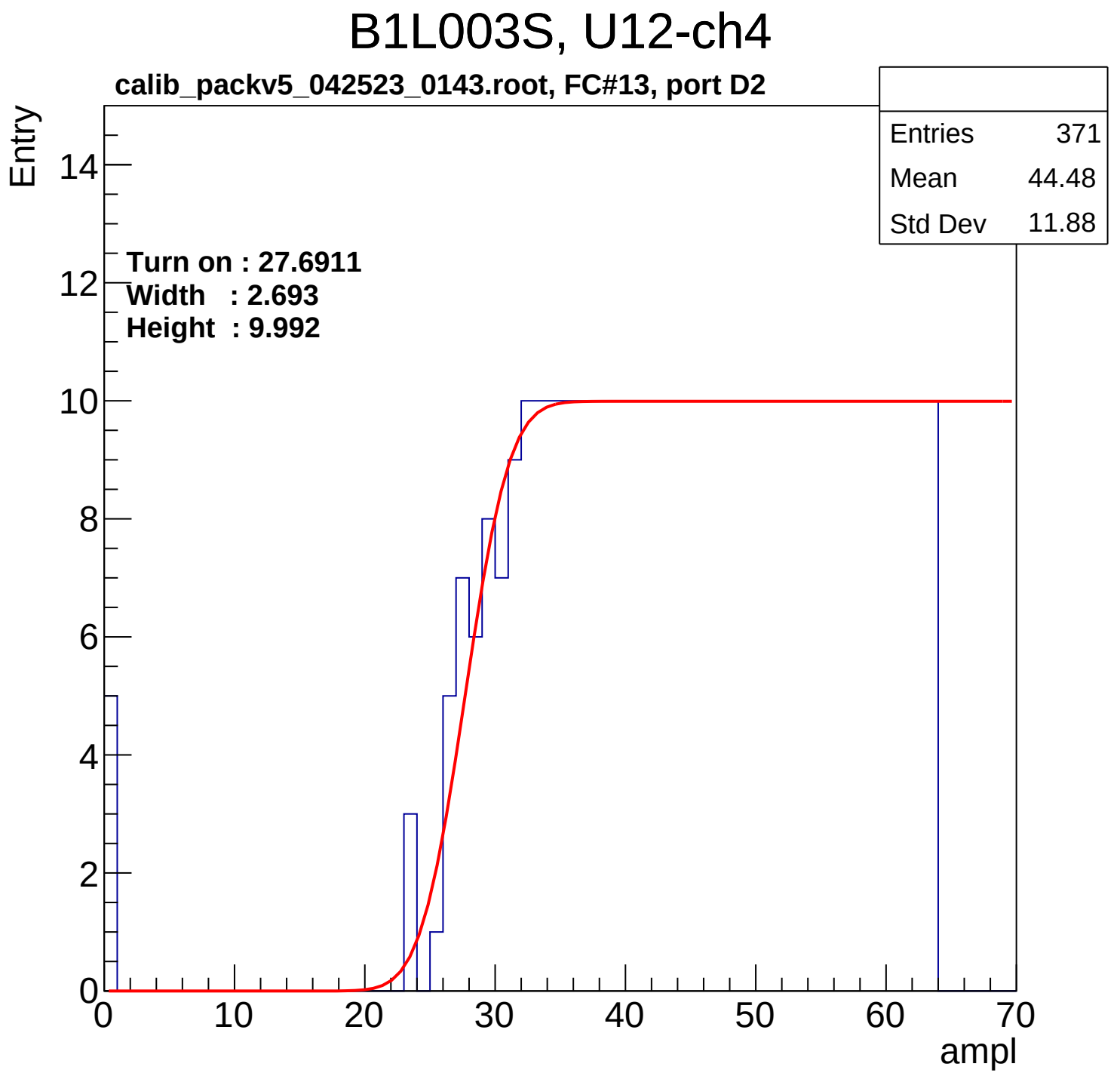
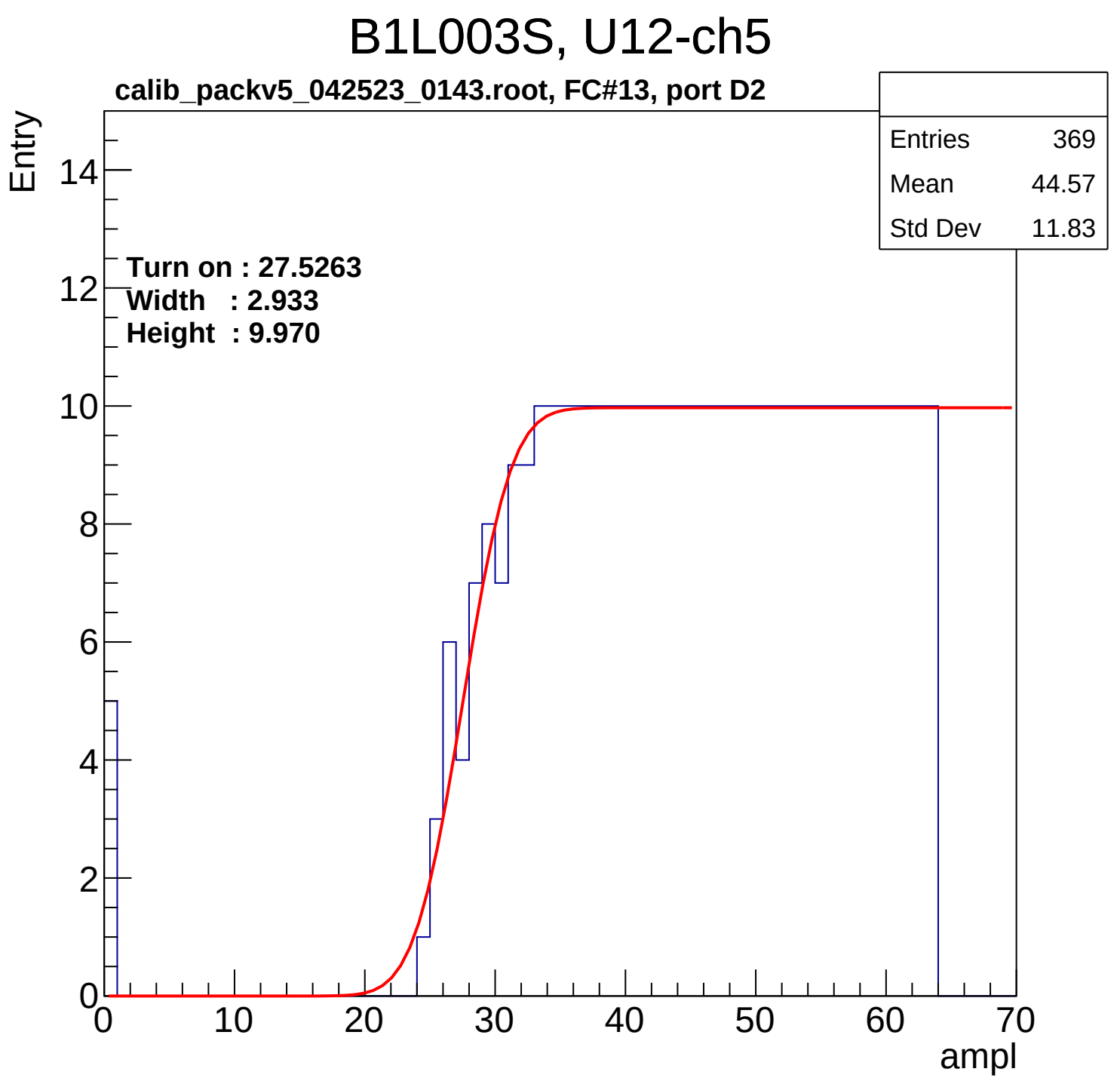

B1L003S, U12-ch0
calib_packv5_042523_0143.root, FC#13, port D2
Entries 369
Mean 44.85
Std Dev 11.16
Turn on : 26.2540
Width : 3.541
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

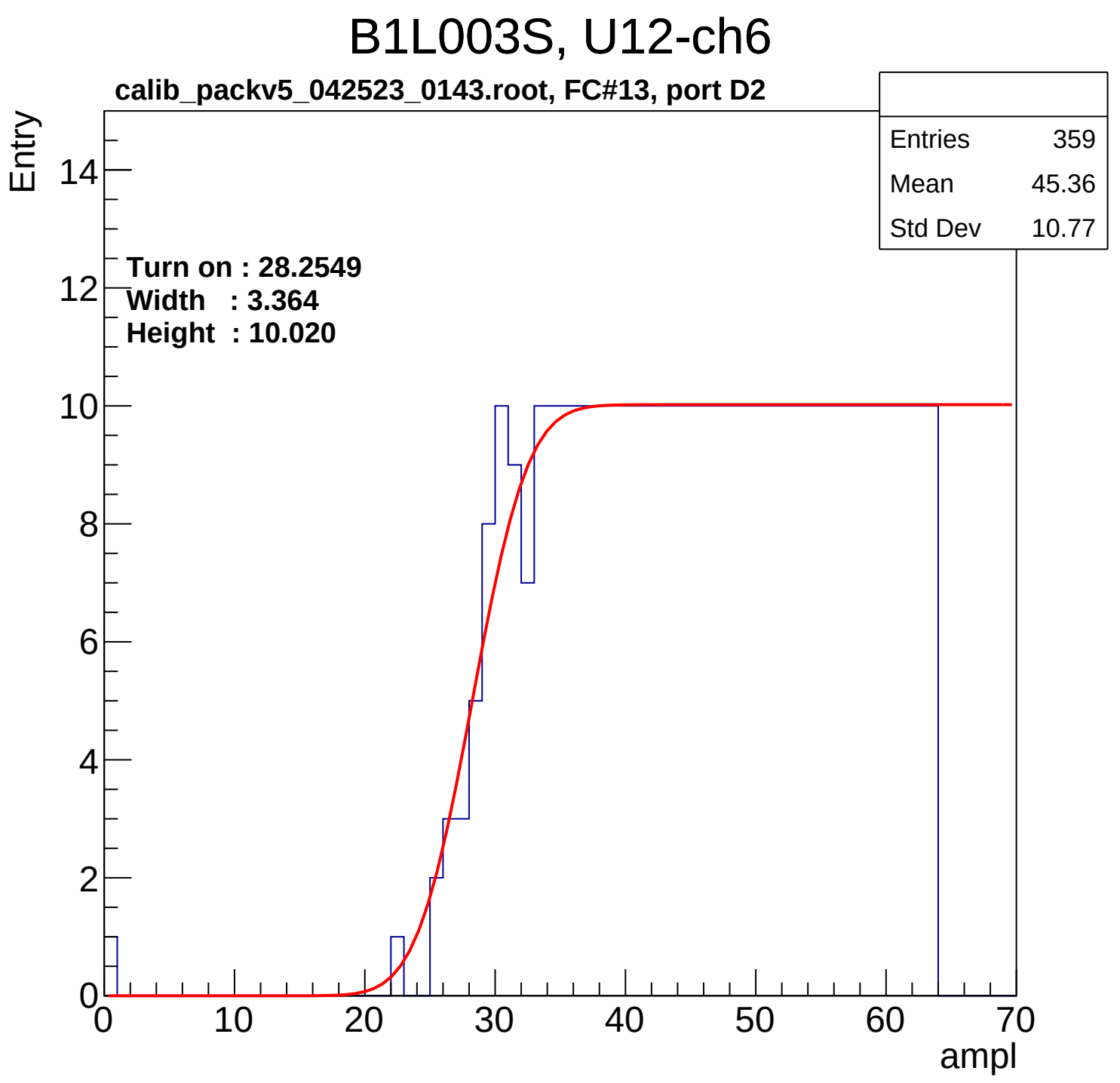

B1L003S, U12-ch1
calib_packv5_042523_0143.root, FC#13, port D2
Entries 377
Mean 44.23
Std Dev 11.95
Turn on : 27.2113
Width : 2.809
Height : 10.067
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

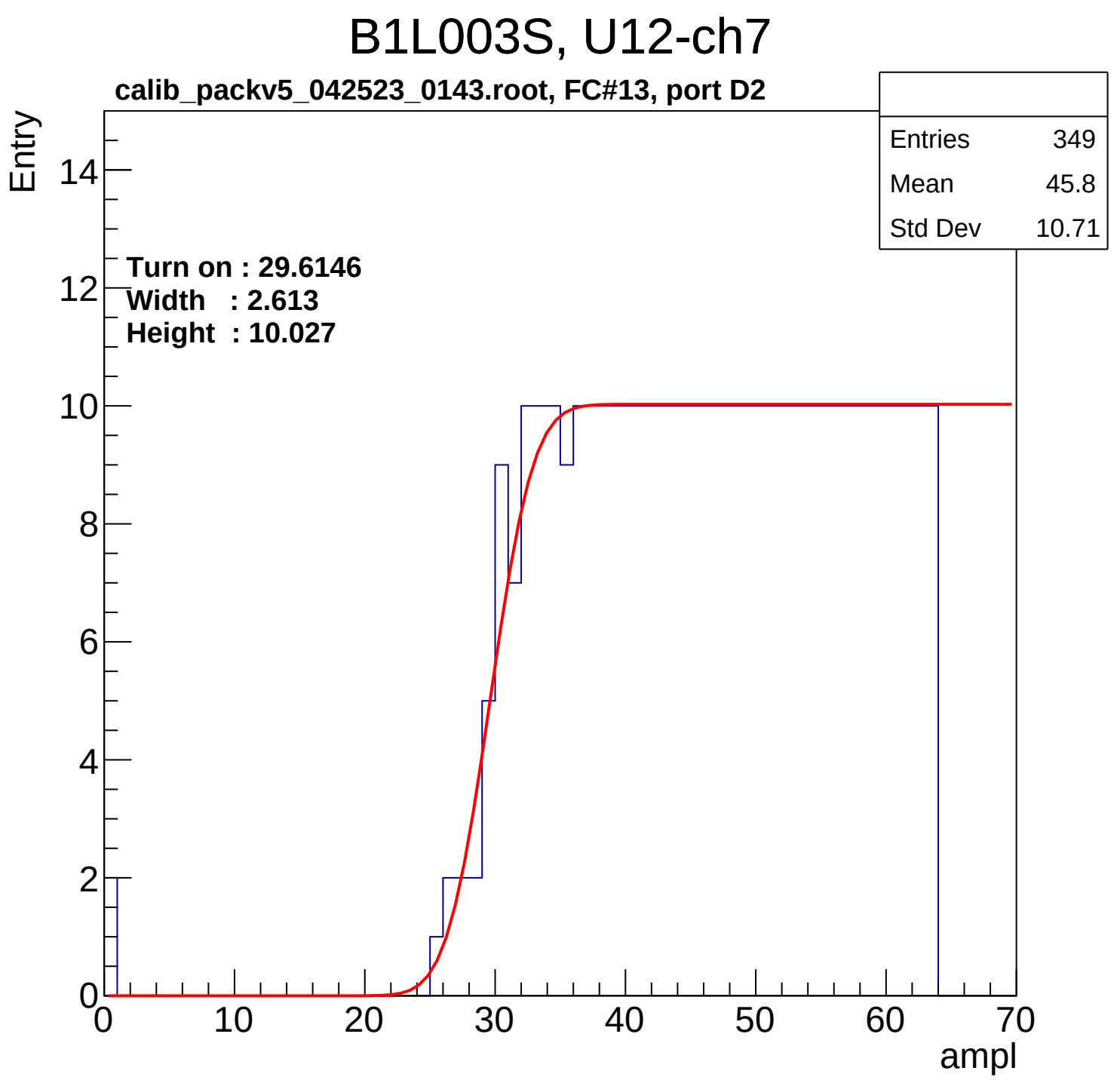

B1L003S, U12-ch2
calib_packv5_042523_0143.root, FC#13, port D2
Entries 369
Mean 44.75
Std Dev 11.4
Turn on : 27.4635
Width : 2.810
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

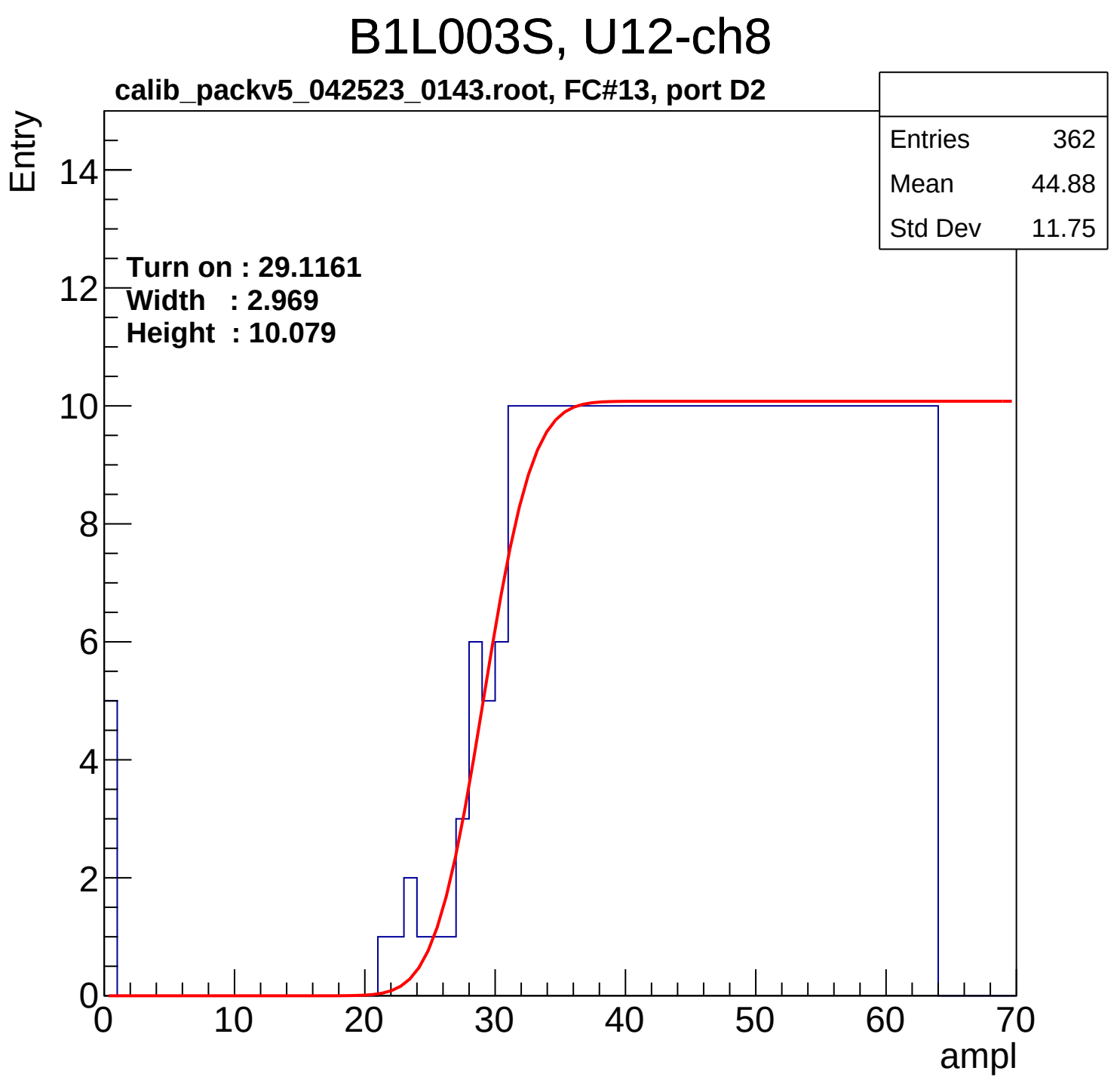

B1L003S, U12-ch3
calib_packv5_042523_0143.root, FC#13, port D2
Entries 359
Mean 45.2
Std Dev 11.32
Turn on : 28.8099
Width : 1.318
Height : 10.011
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

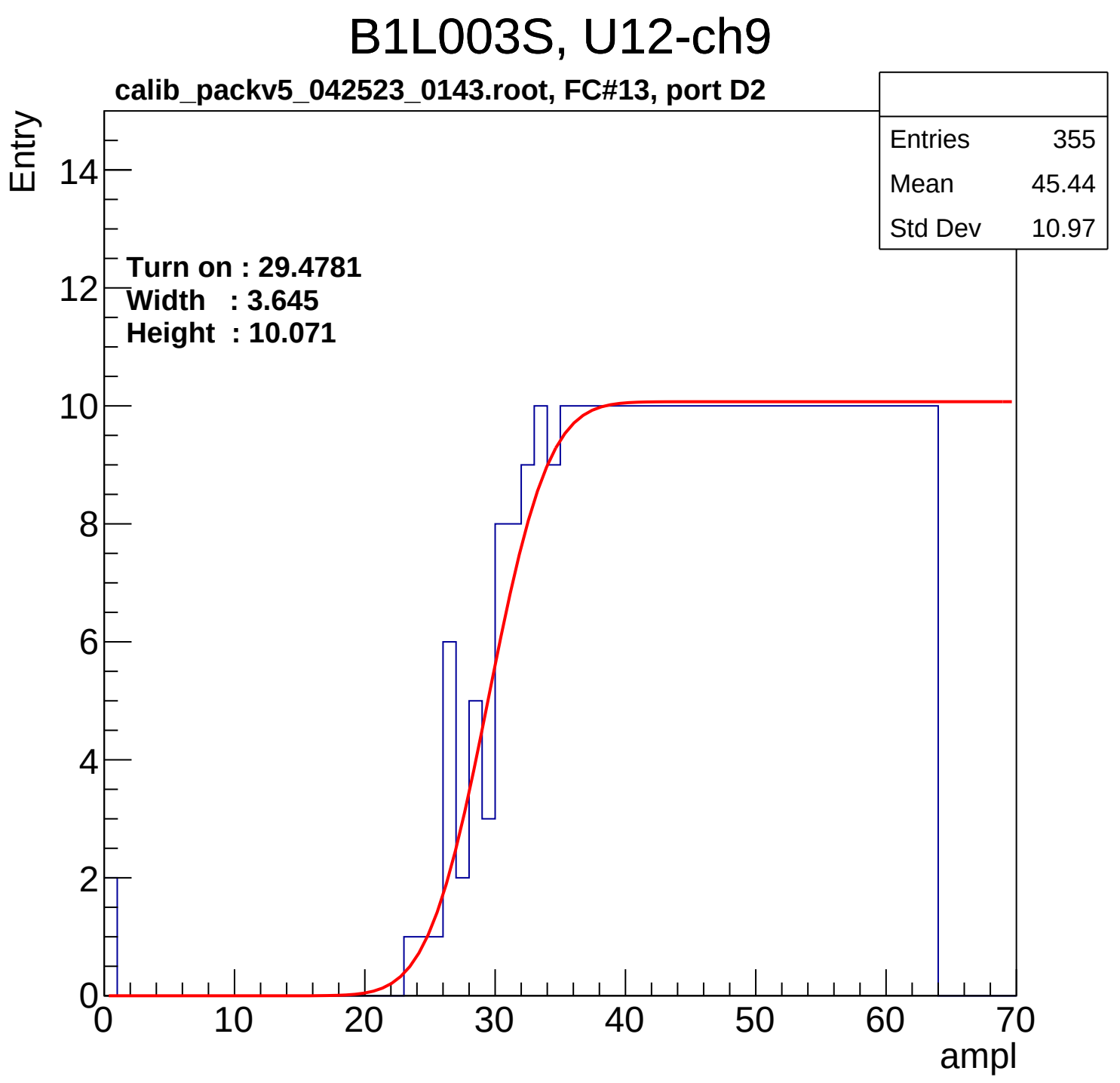

B1L003S, U12-ch4
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.48
Std Dev 11.88
Turn on : 27.6911
Width : 2.693
Height : 9.992
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

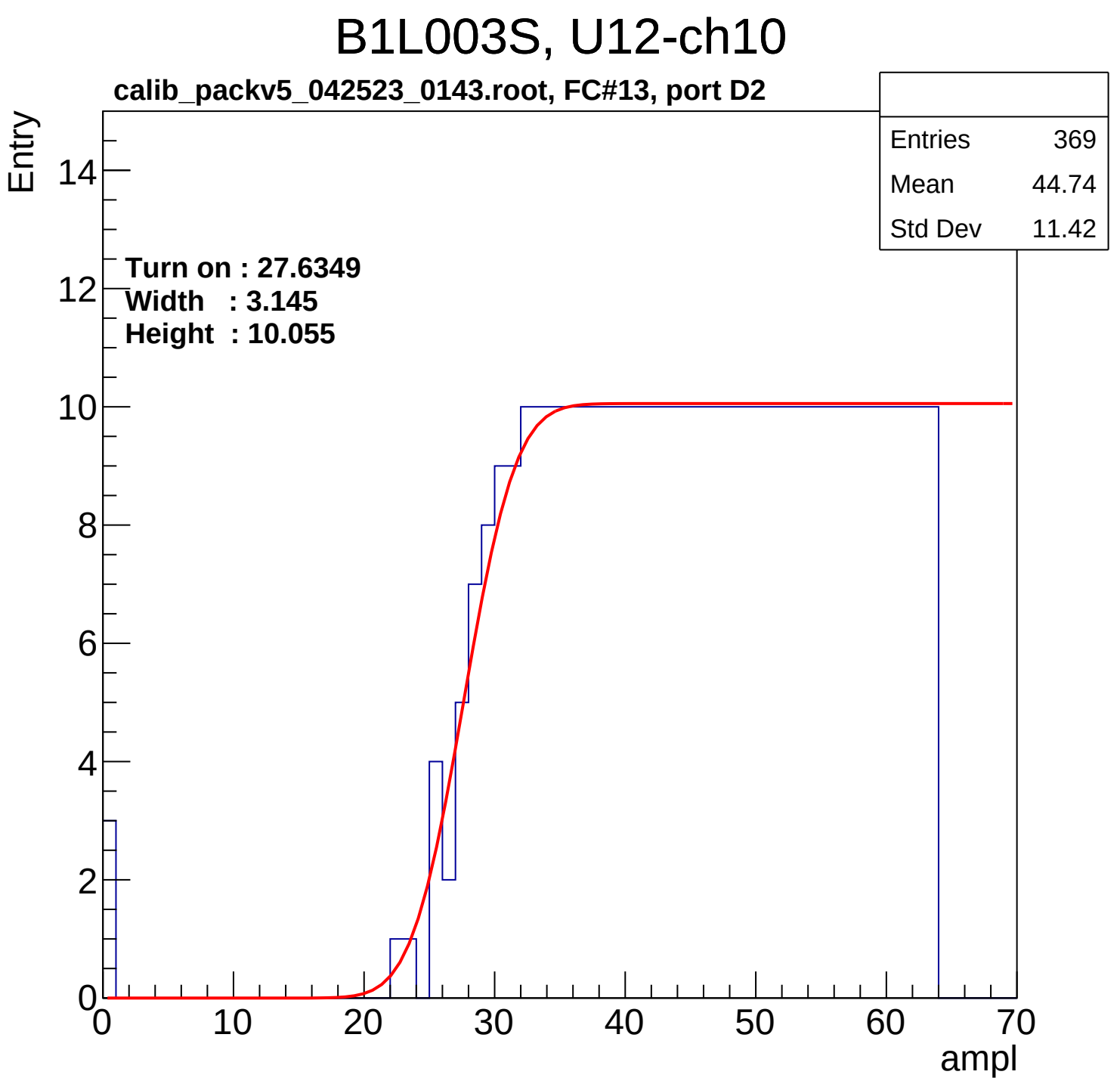

B1L003S, U12-ch5
calib_packv5_042523_0143.root, FC#13, port D2
Entries 369
Mean 44.57
Std Dev 11.83
Turn on : 27.5263
Width : 2.933
Height : 9.970
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

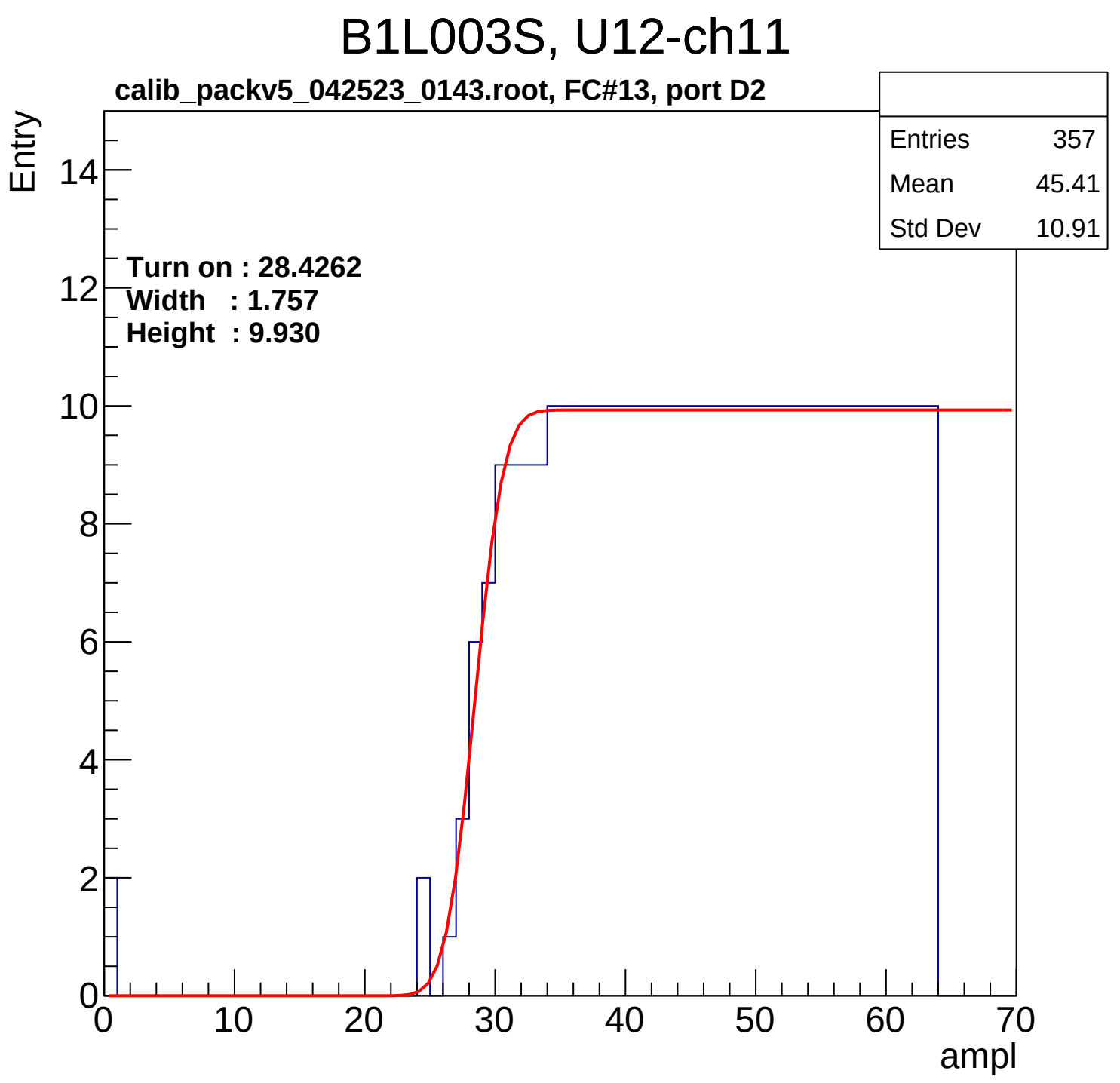

B1L003S, U12-ch6
calib_packv5_042523_0143.root, FC#13, port D2
Entries 359
Mean 45.36
Std Dev 10.77
Turn on : 28.2549
Width : 3.364
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

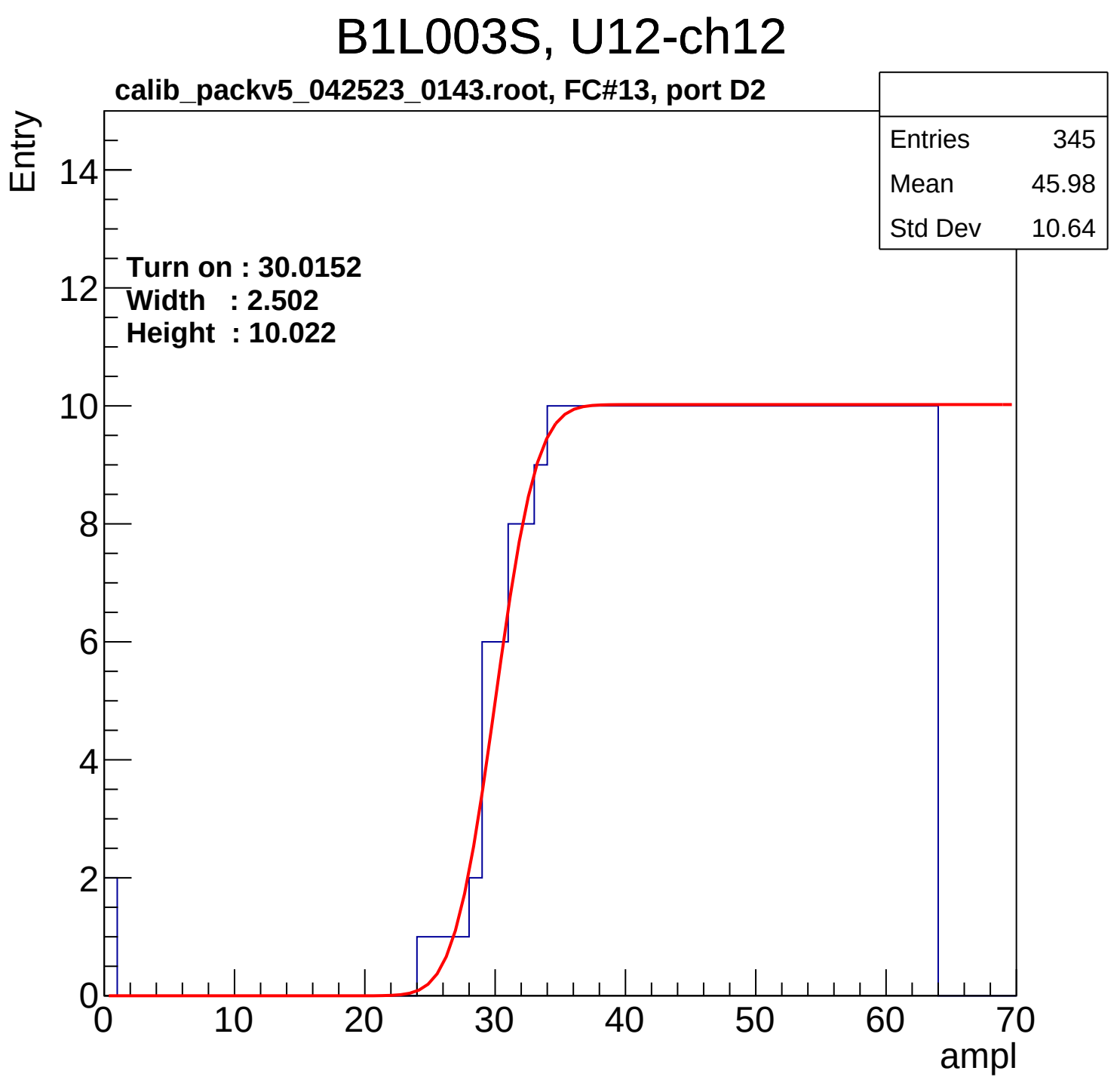

B1L003S, U12-ch7
calib_packv5_042523_0143.root, FC#13, port D2
Entries 349
Mean 45.8
Std Dev 10.71
Turn on : 29.6146
Width : 2.613
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

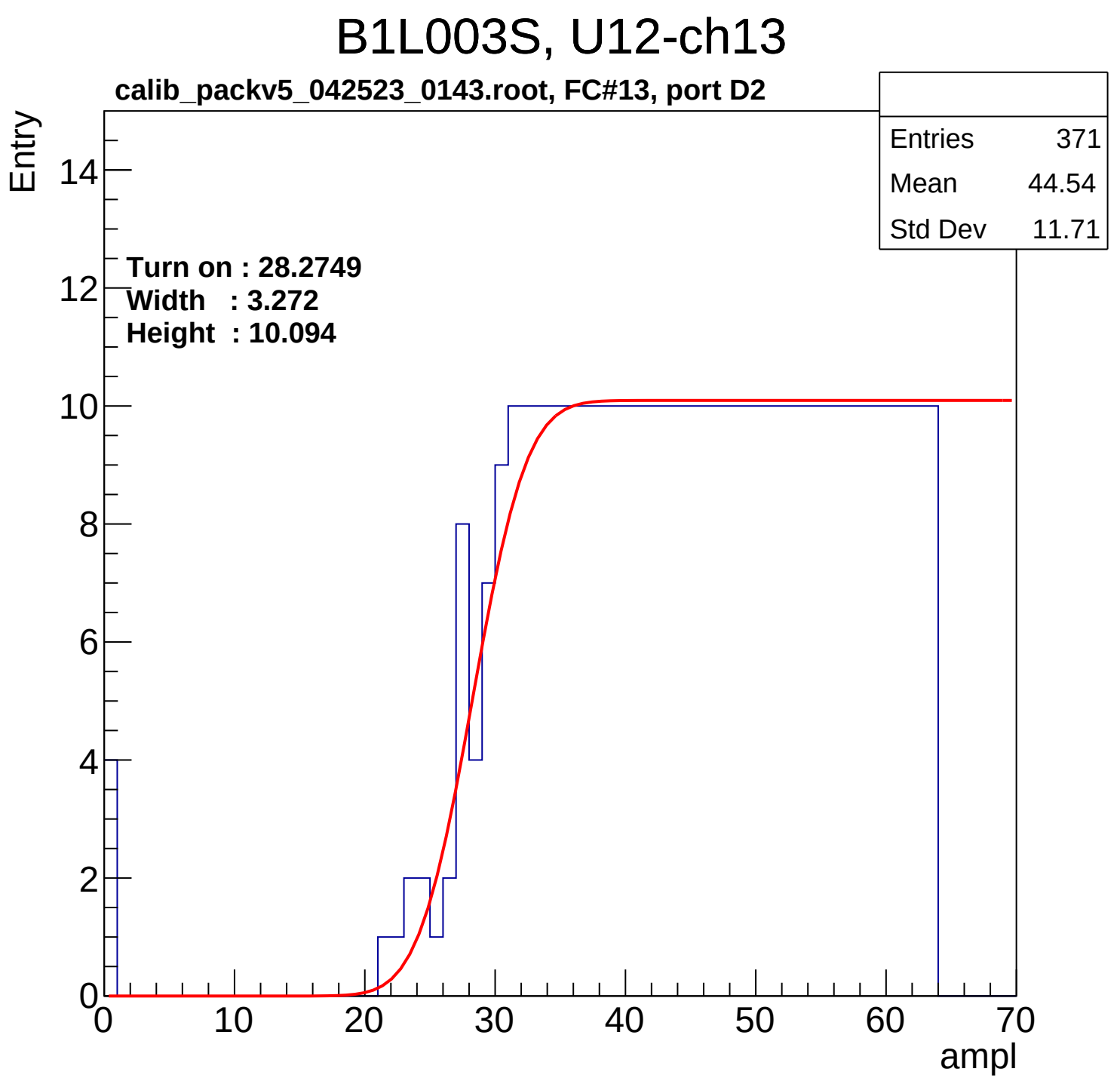

B1L003S, U12-ch8
calib_packv5_042523_0143.root, FC#13, port D2
Entries 362
Mean 44.88
Std Dev 11.75
Turn on : 29.1161
Width : 2.969
Height : 10.079
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

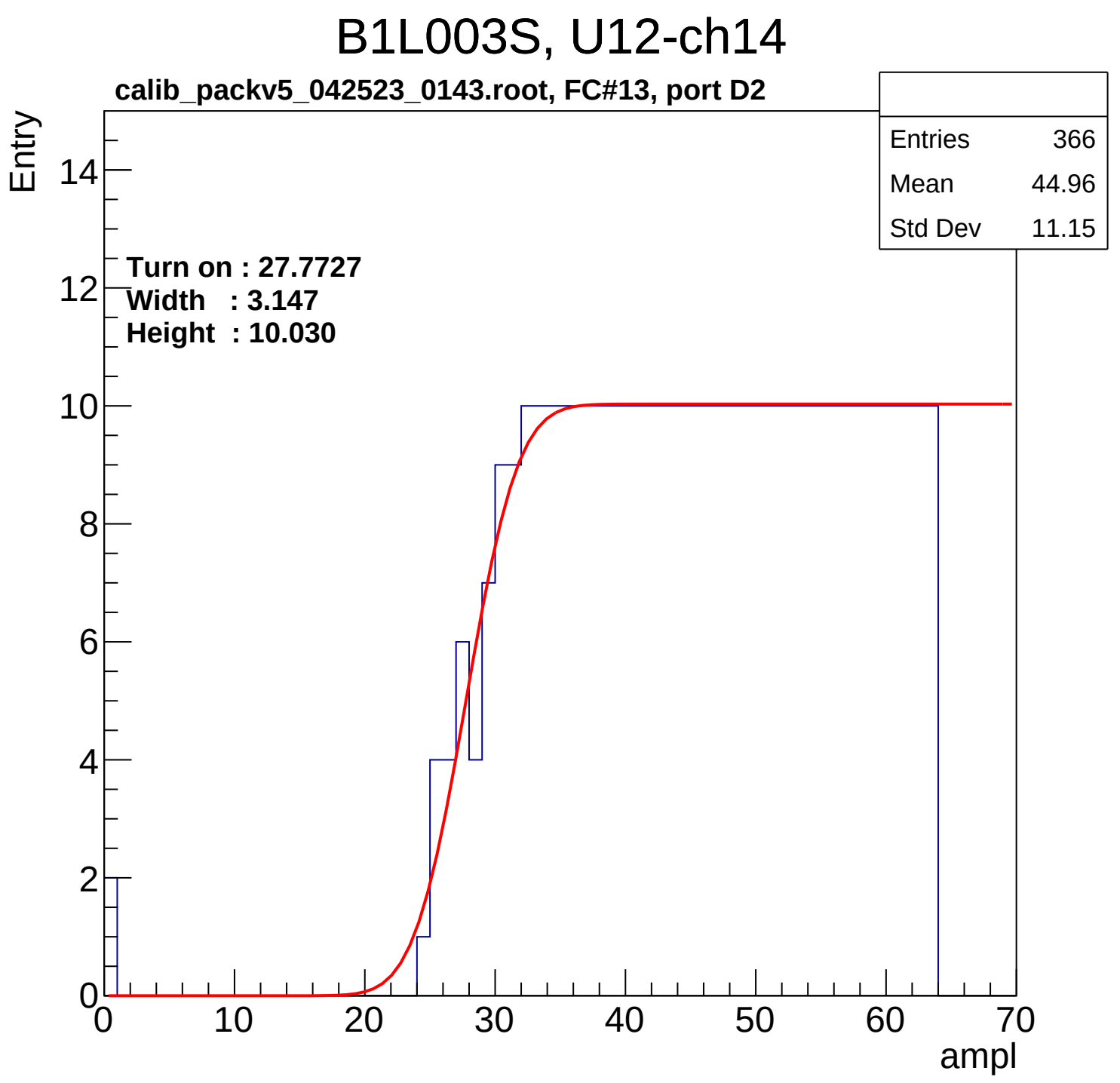

B1L003S, U12-ch9
calib_packv5_042523_0143.root, FC#13, port D2
Entries 355
Mean 45.44
Std Dev 10.97
Turn on : 29.4781
Width : 3.645
Height : 10.071
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

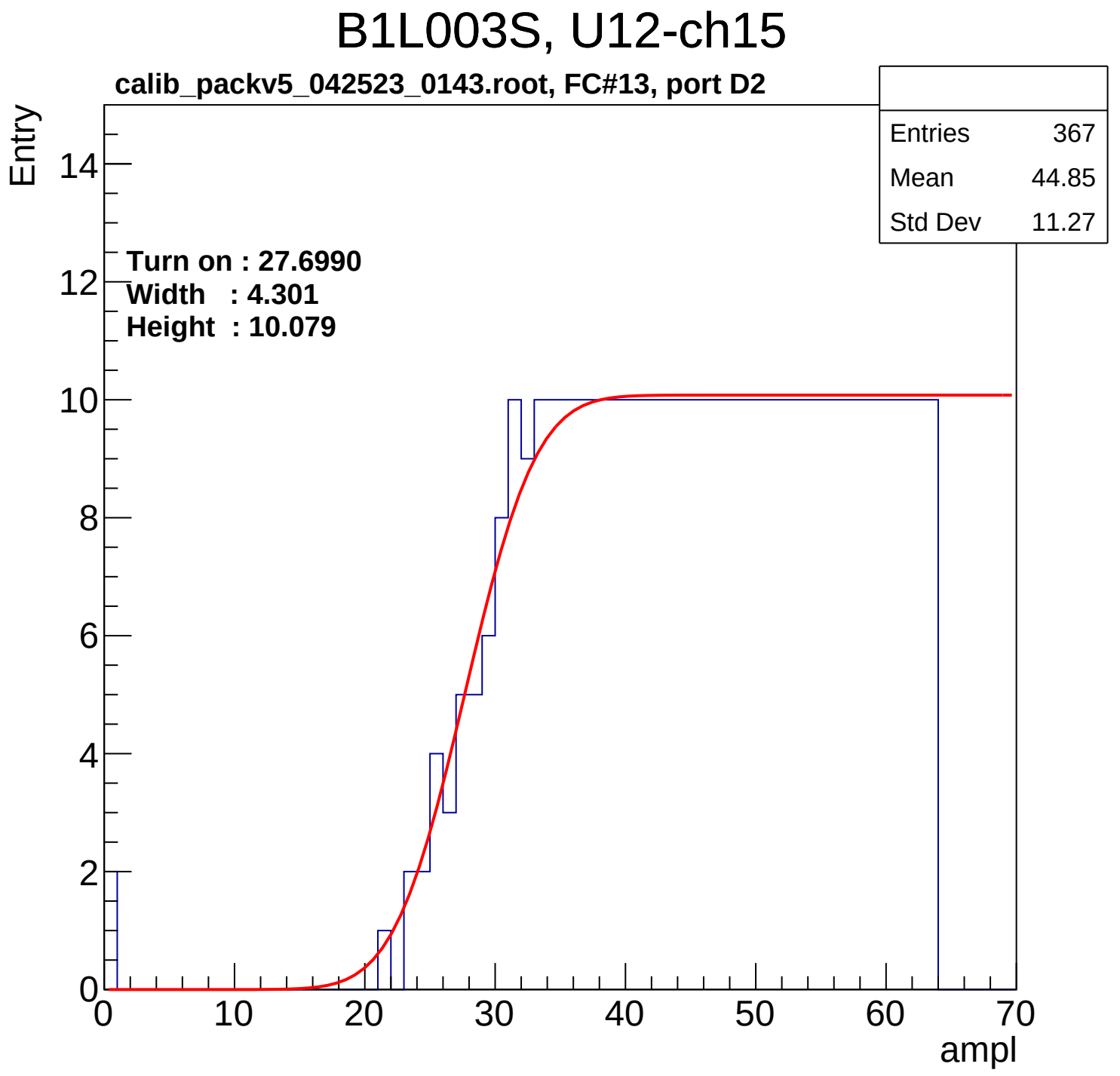

B1L003S, U12-ch10
calib_packv5_042523_0143.root, FC#13, port D2
Entries 369
Mean 44.74
Std Dev 11.42
Turn on : 27.6349
Width : 3.145
Height : 10.055
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

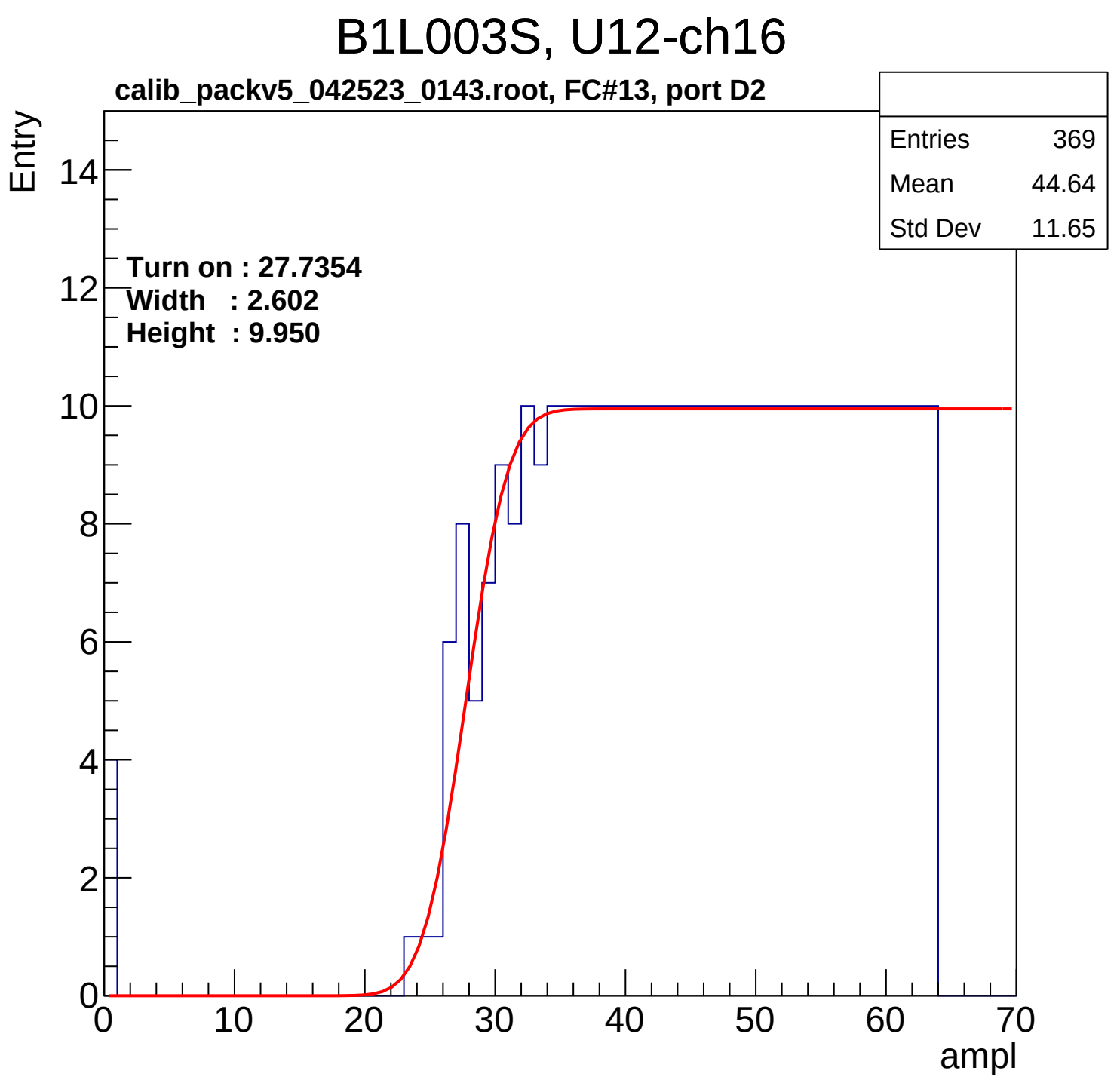

B1L003S, U12-ch11
calib_packv5_042523_0143.root, FC#13, port D2
Entries 357
Mean 45.41
Std Dev 10.91
Turn on : 28.4262
Width : 1.757
Height : 9.930
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

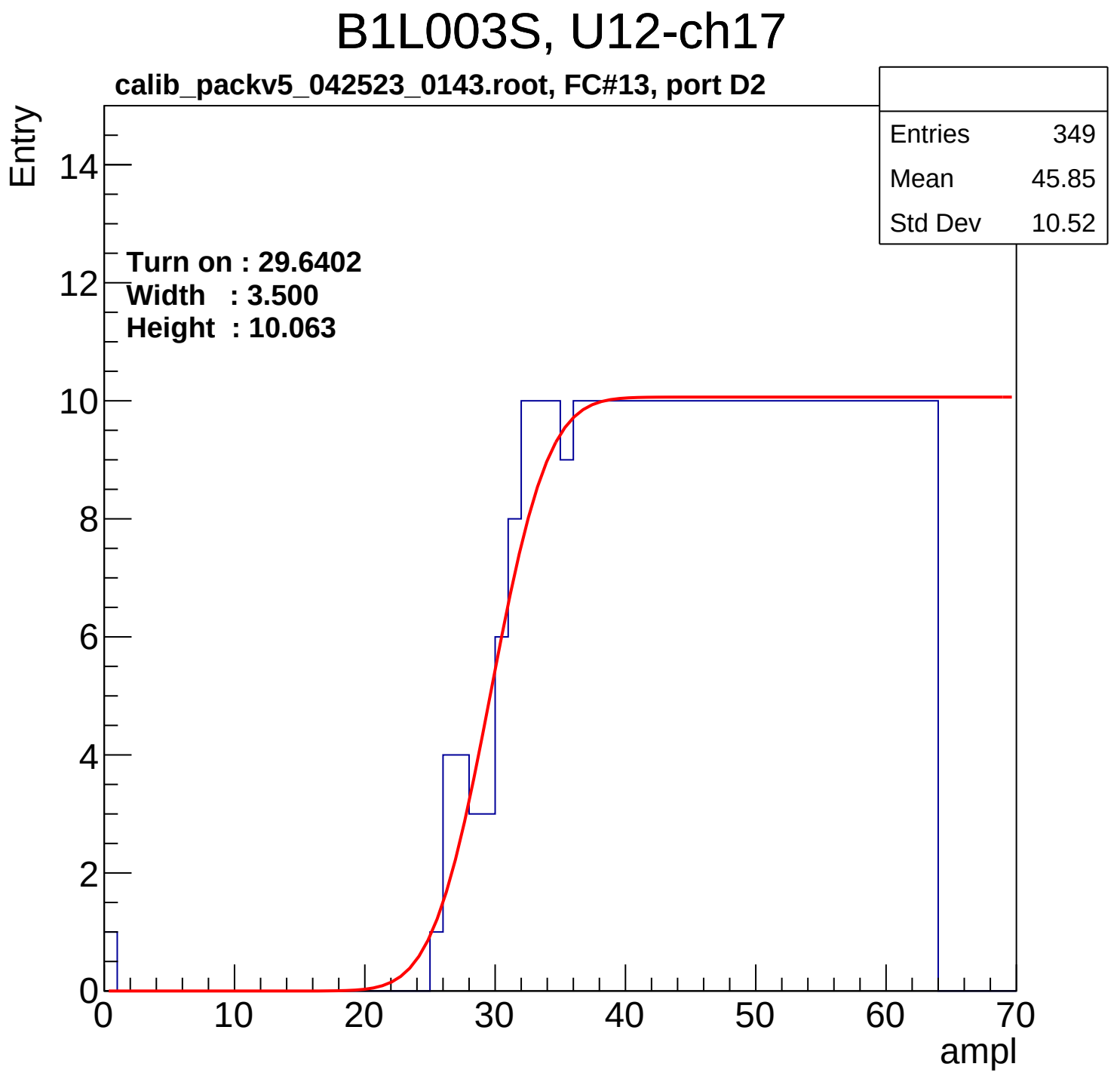

B1L003S, U12-ch12
calib_packv5_042523_0143.root, FC#13, port D2
Entries 345
Mean 45.98
Std Dev 10.64
Turn on : 30.0152
Width : 2.502
Height : 10.022
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

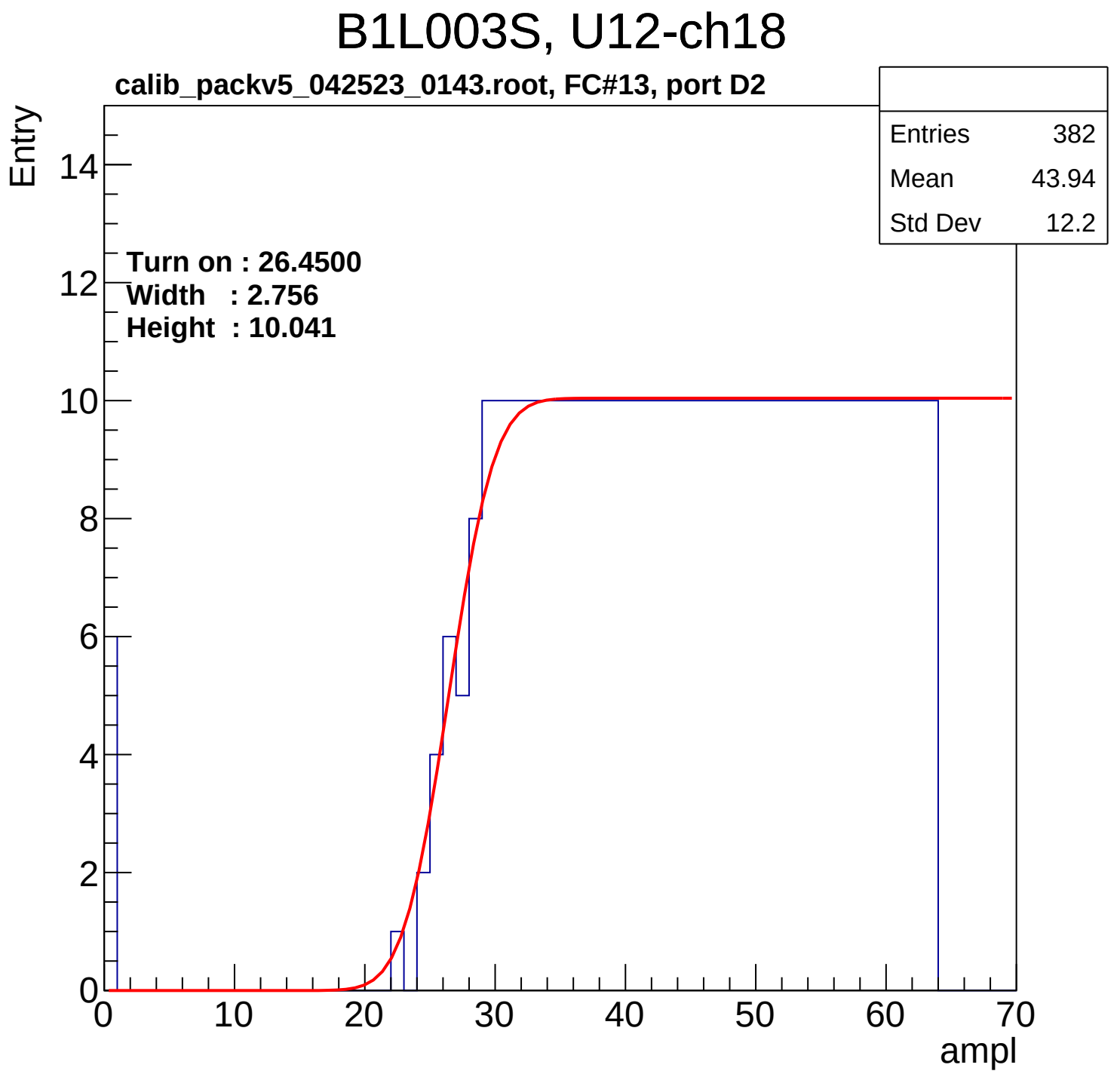

B1L003S, U12-ch13
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.54
Std Dev 11.71
Turn on : 28.2749
Width : 3.272
Height : 10.094
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

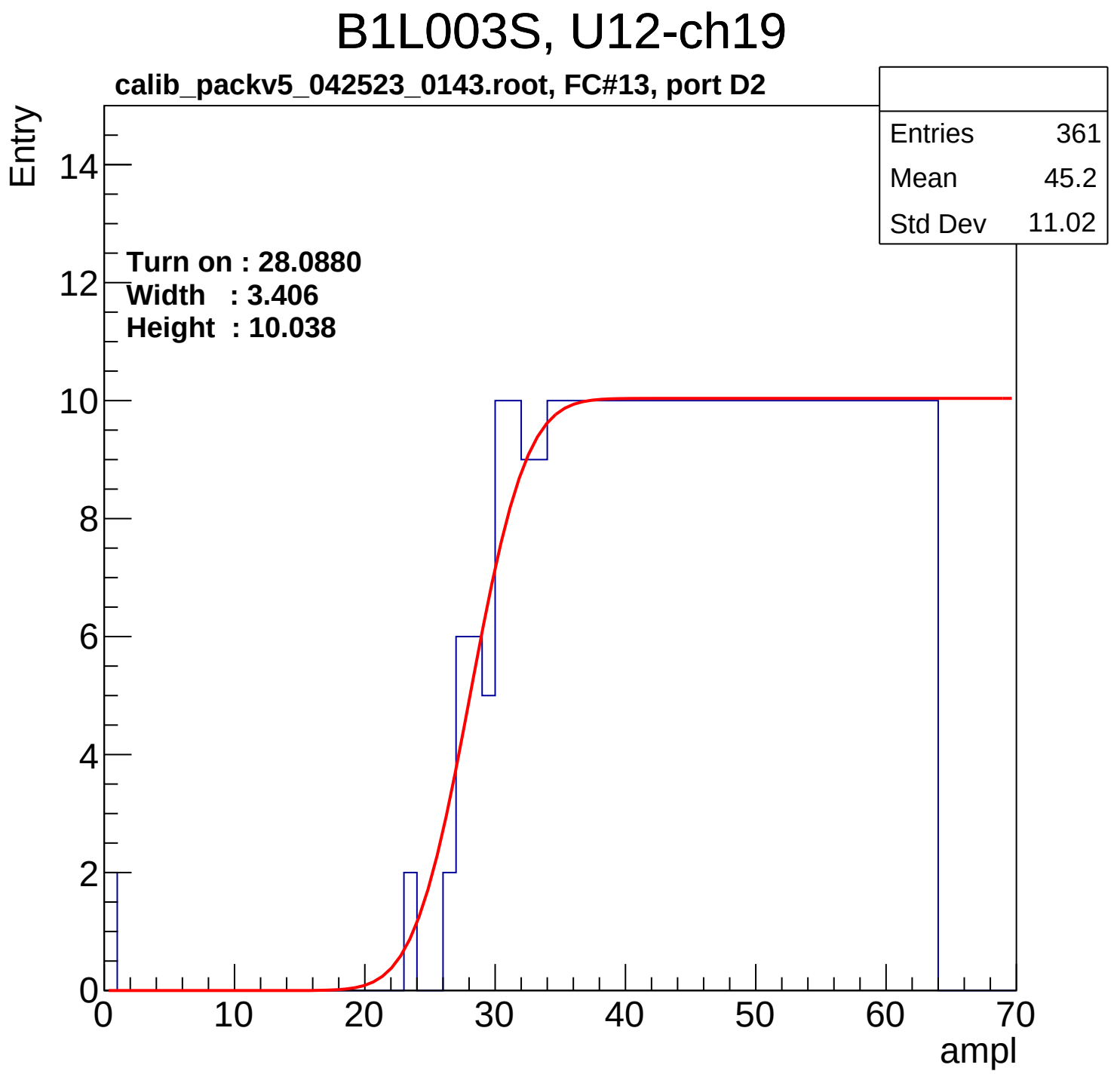

B1L003S, U12-ch14
calib_packv5_042523_0143.root, FC#13, port D2
Entries 366
Mean 44.96
Std Dev 11.15
Turn on : 27.7727
Width : 3.147
Height : 10.030
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

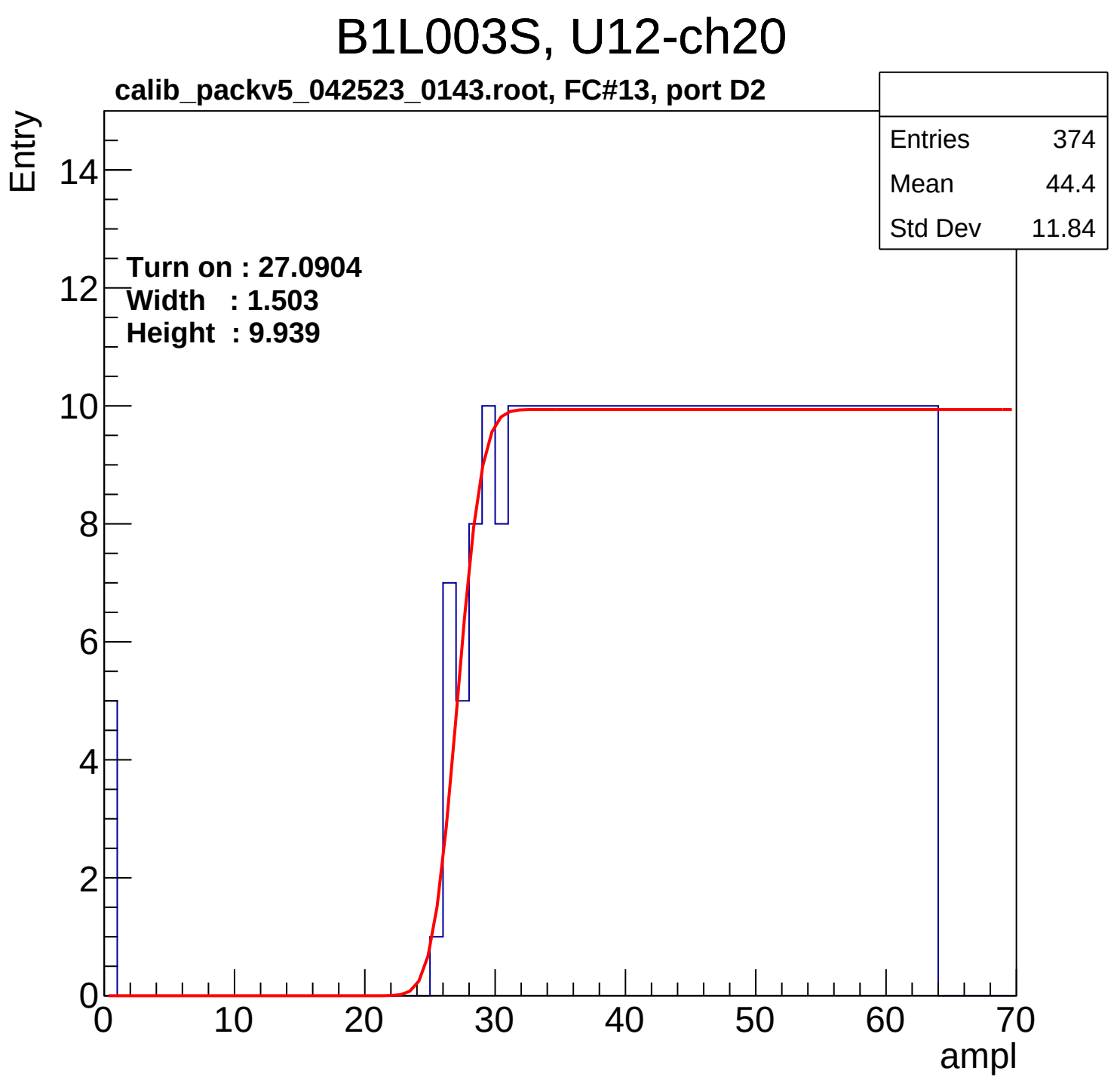

B1L003S, U12-ch15
calib_packv5_042523_0143.root, FC#13, port D2
Entries 367
Mean 44.85
Std Dev 11.27
Turn on : 27.6990
Width : 4.301
Height : 10.079
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

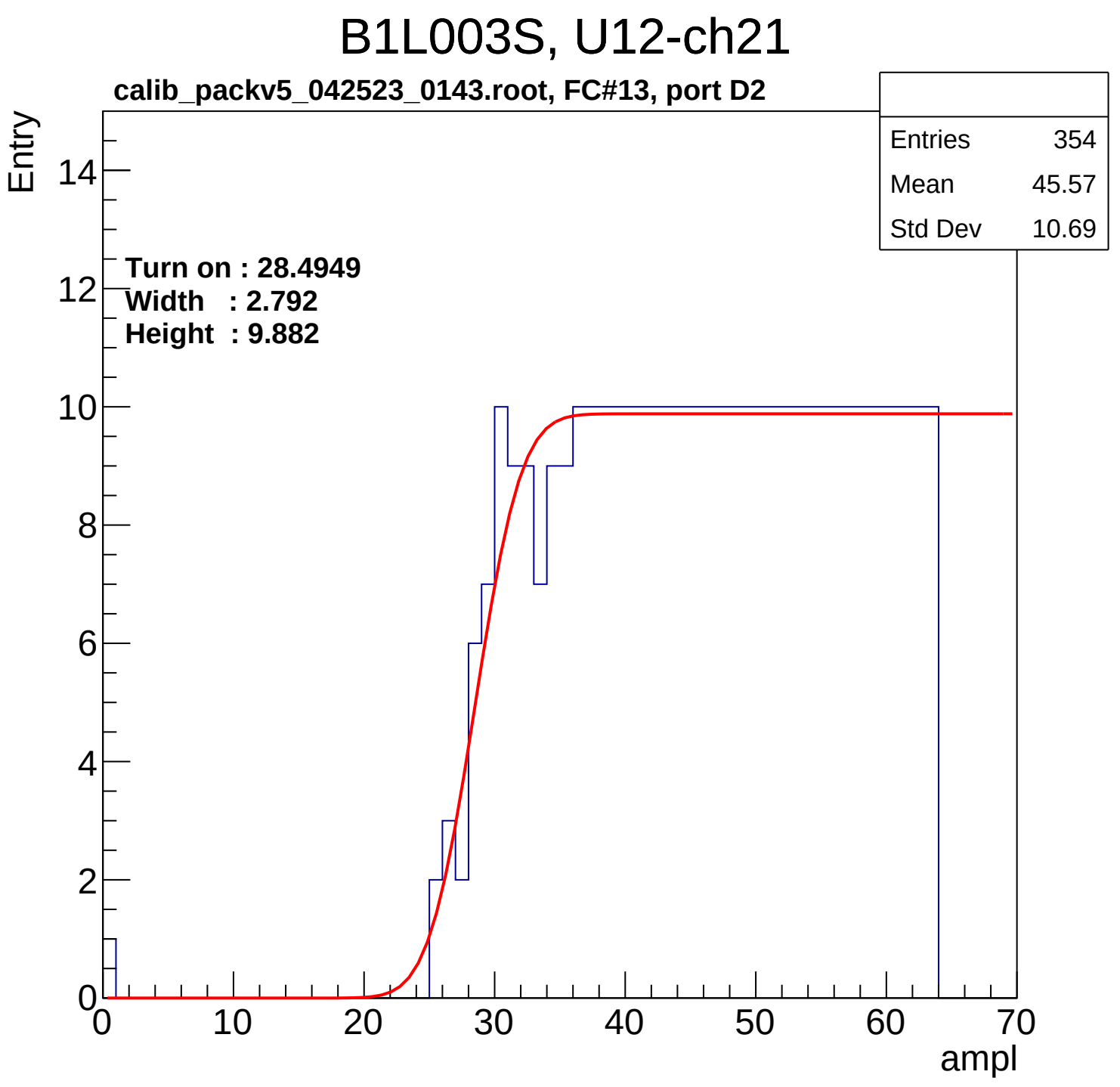

B1L003S, U12-ch16
calib_packv5_042523_0143.root, FC#13, port D2
Entries 369
Mean 44.64
Std Dev 11.65
Turn on : 27.7354
Width : 2.602
Height : 9.950
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

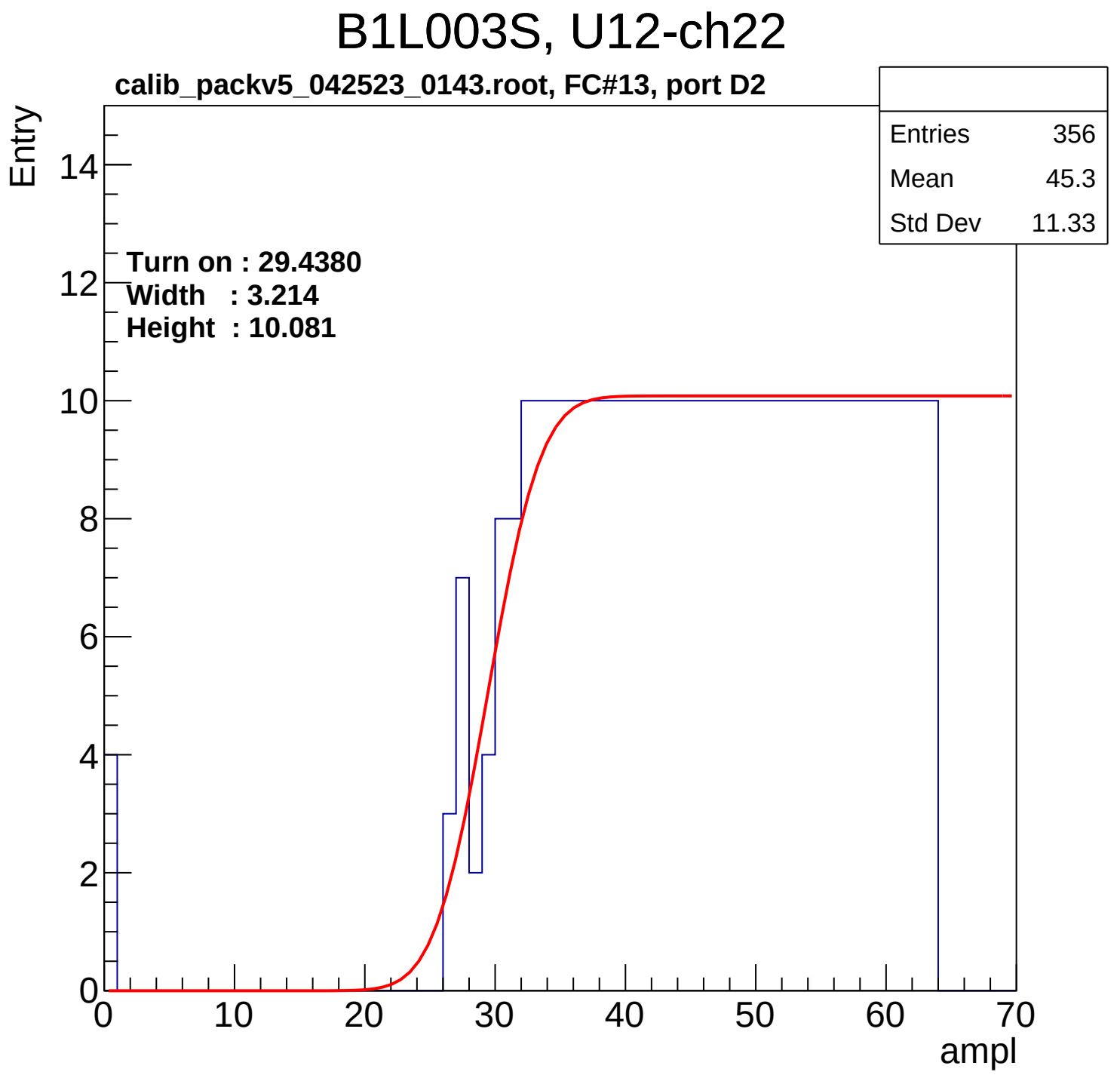

B1L003S, U12-ch17
calib_packv5_042523_0143.root, FC#13, port D2
Entries 349
Mean 45.85
Std Dev 10.52
Turn on : 29.6402
Width : 3.500
Height : 10.063
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

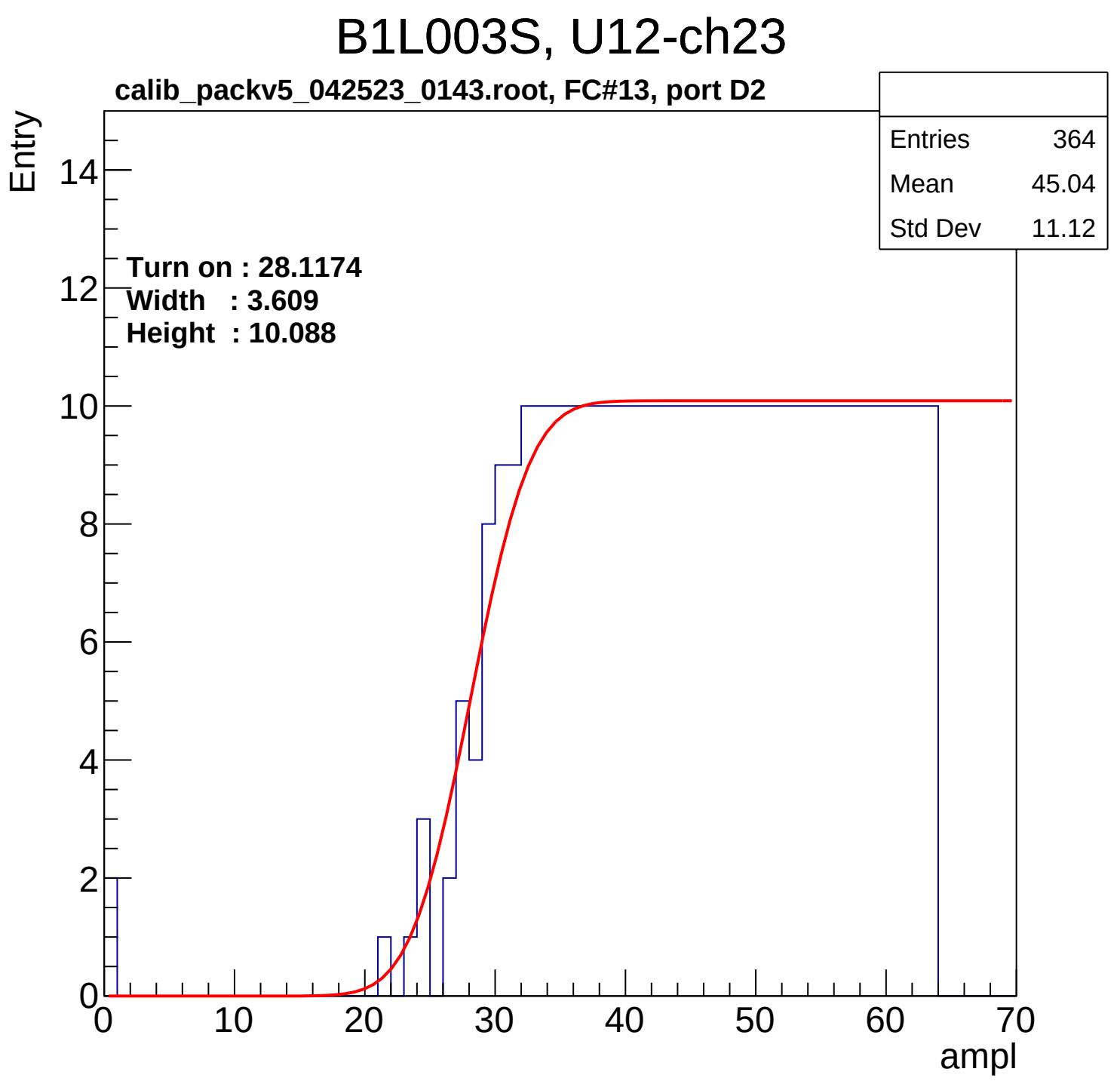

B1L003S, U12-ch18
calib_packv5_042523_0143.root, FC#13, port D2
Entries 382
Mean 43.94
Std Dev 12.2
Turn on : 26.4500
Width : 2.756
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

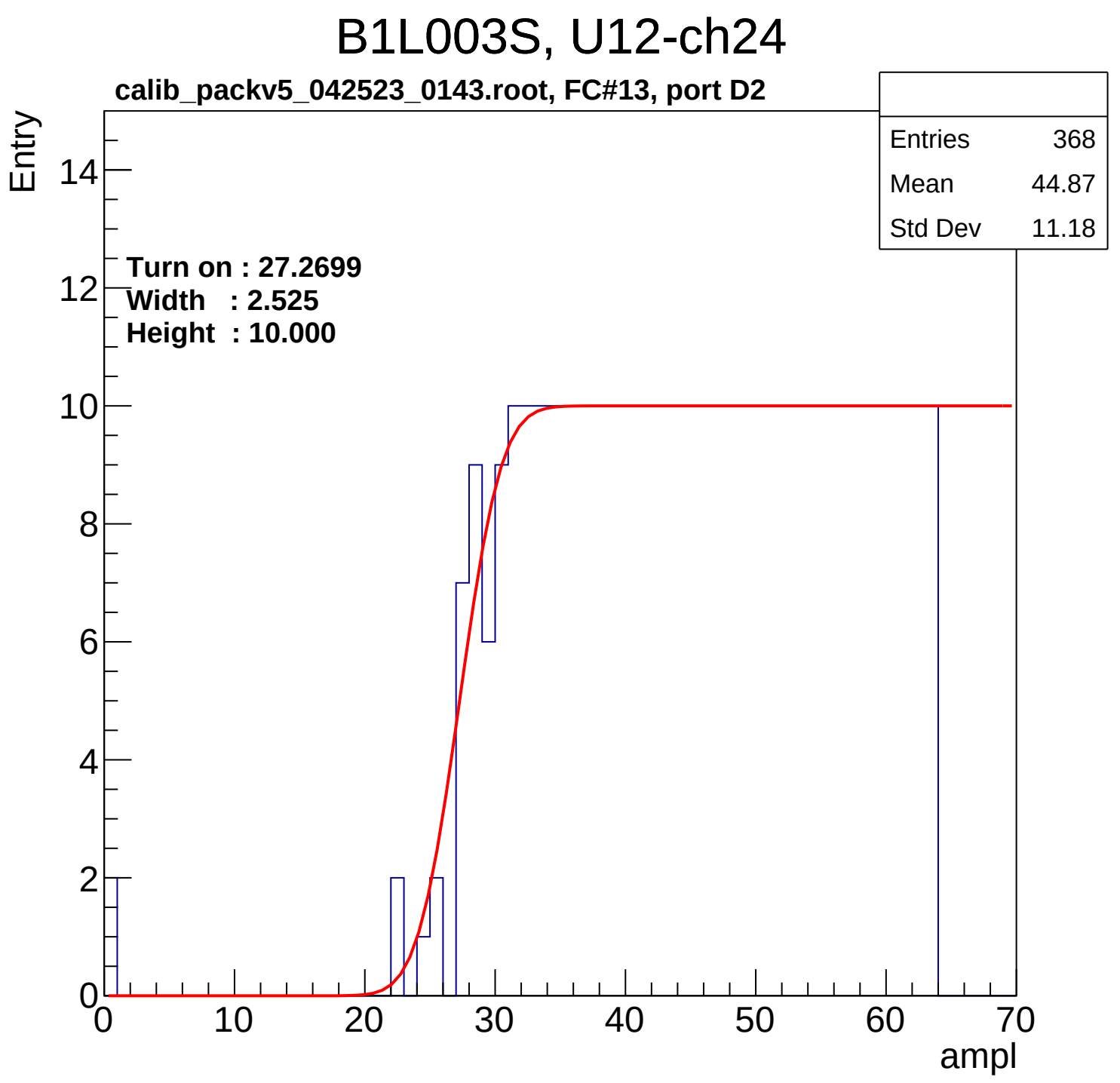

B1L003S, U12-ch19
calib_packv5_042523_0143.root, FC#13, port D2
Entries 361
Mean 45.2
Std Dev 11.02
Turn on : 28.0880
Width : 3.406
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

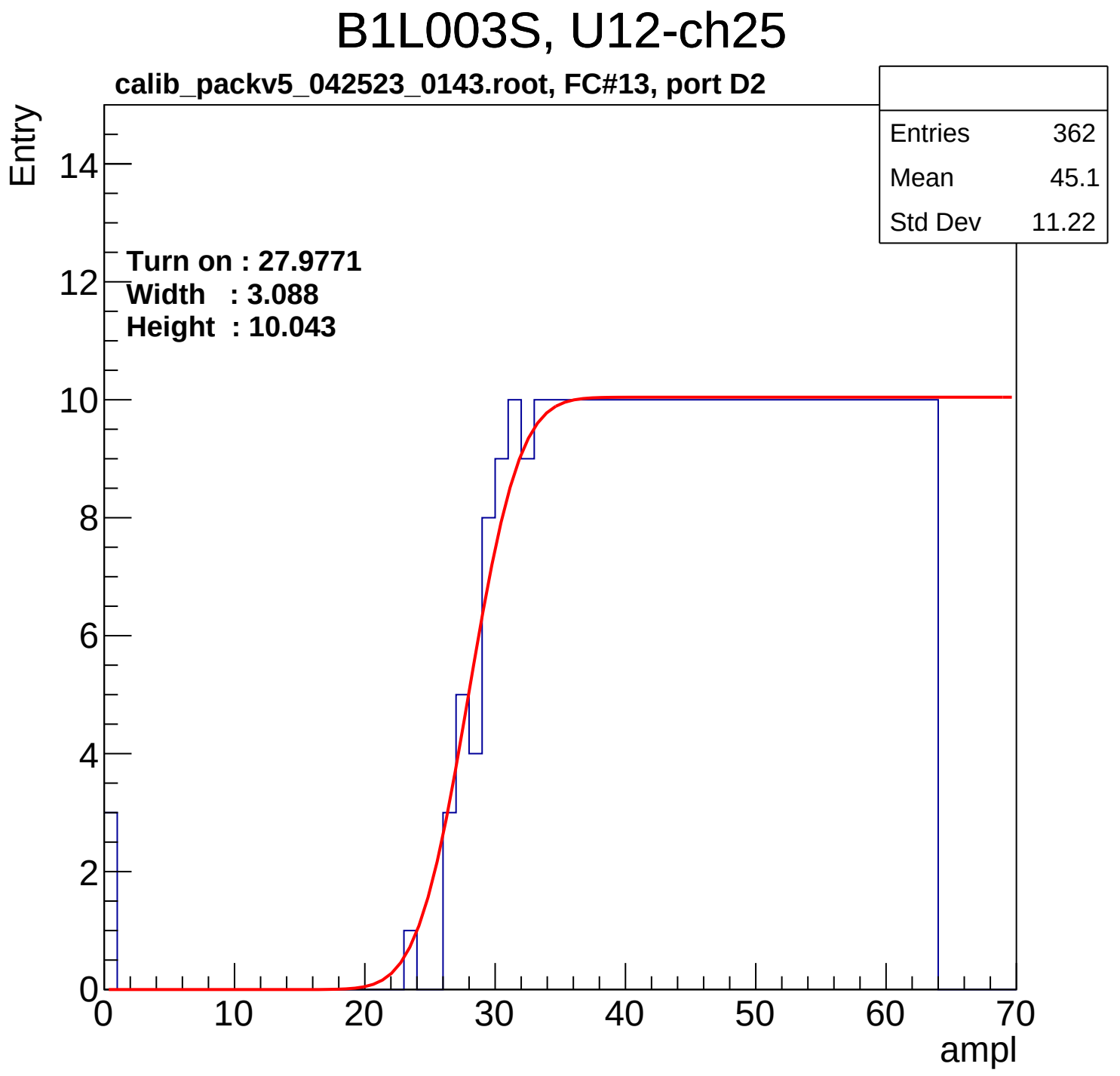

B1L003S, U12-ch20
calib_packv5_042523_0143.root, FC#13, port D2
Entries 374
Mean 44.4
Std Dev 11.84
Turn on : 27.0904
Width : 1.503
Height : 9.939
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

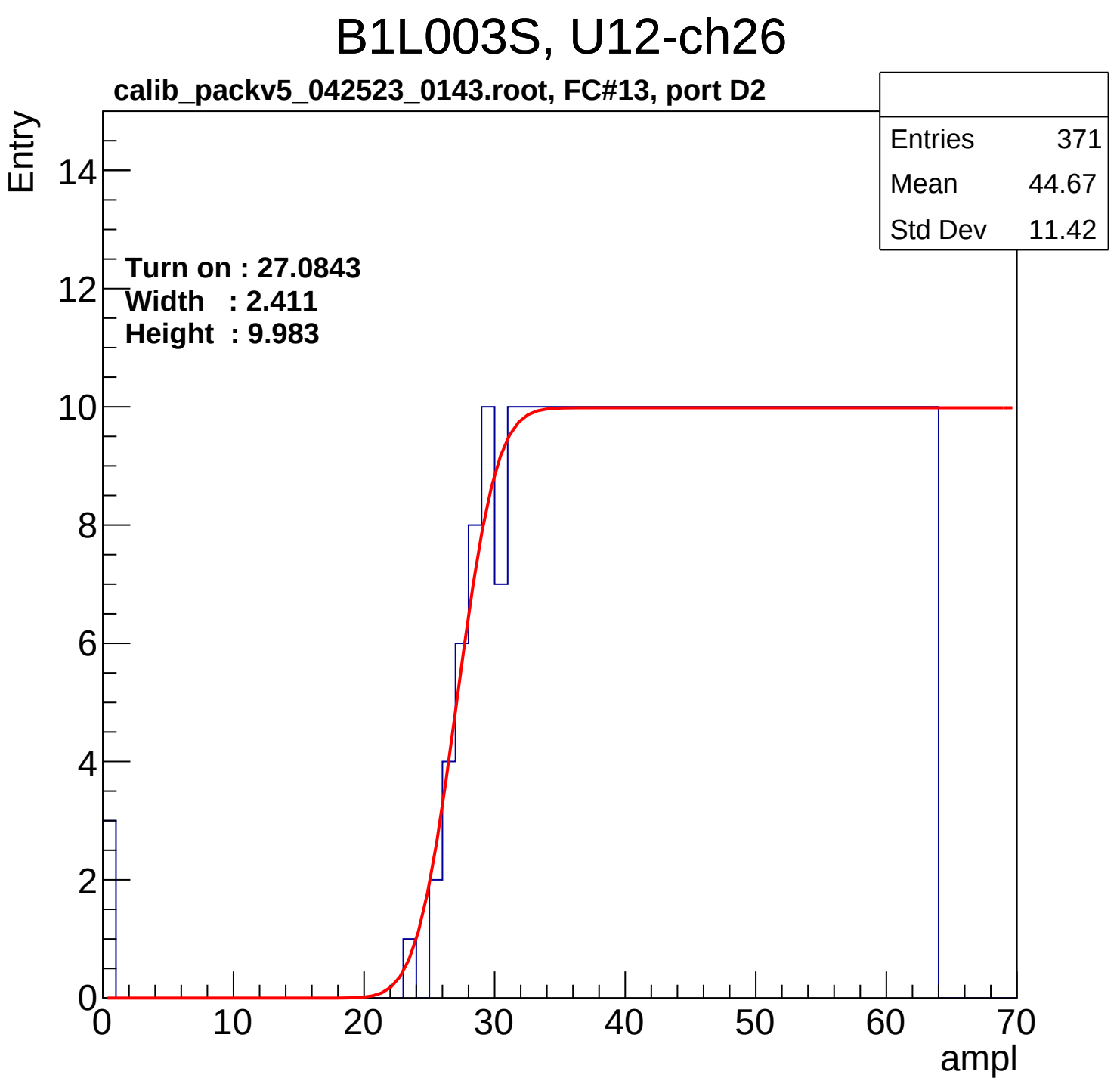

B1L003S, U12-ch21
calib_packv5_042523_0143.root, FC#13, port D2
Entries 354
Mean 45.57
Std Dev 10.69
Turn on : 28.4949
Width : 2.792
Height : 9.882
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

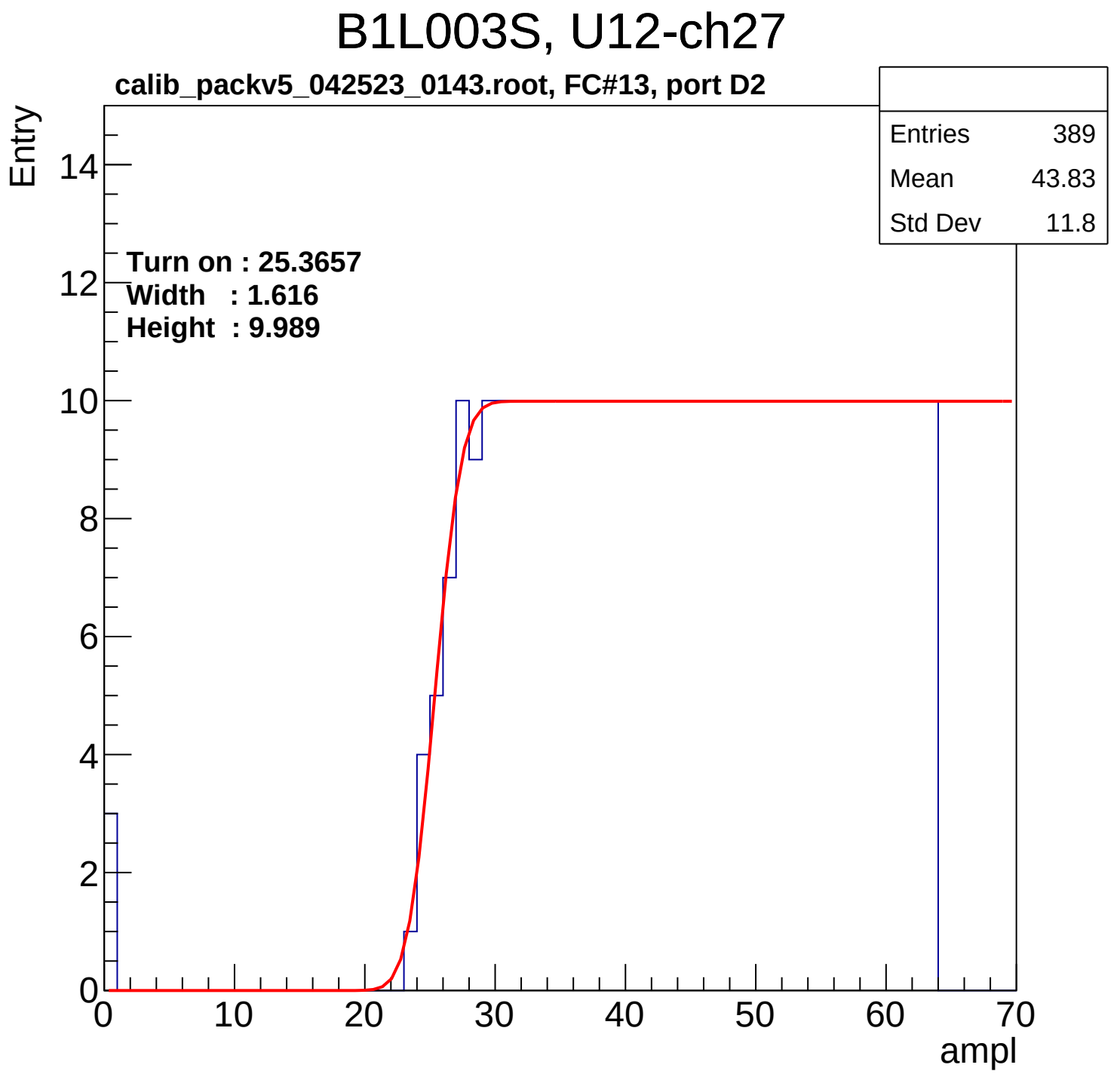

B1L003S, U12-ch22
calib_packv5_042523_0143.root, FC#13, port D2
Entries 356
Mean 45.3
Std Dev 11.33
Turn on : 29.4380
Width : 3.214
Height : 10.081
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

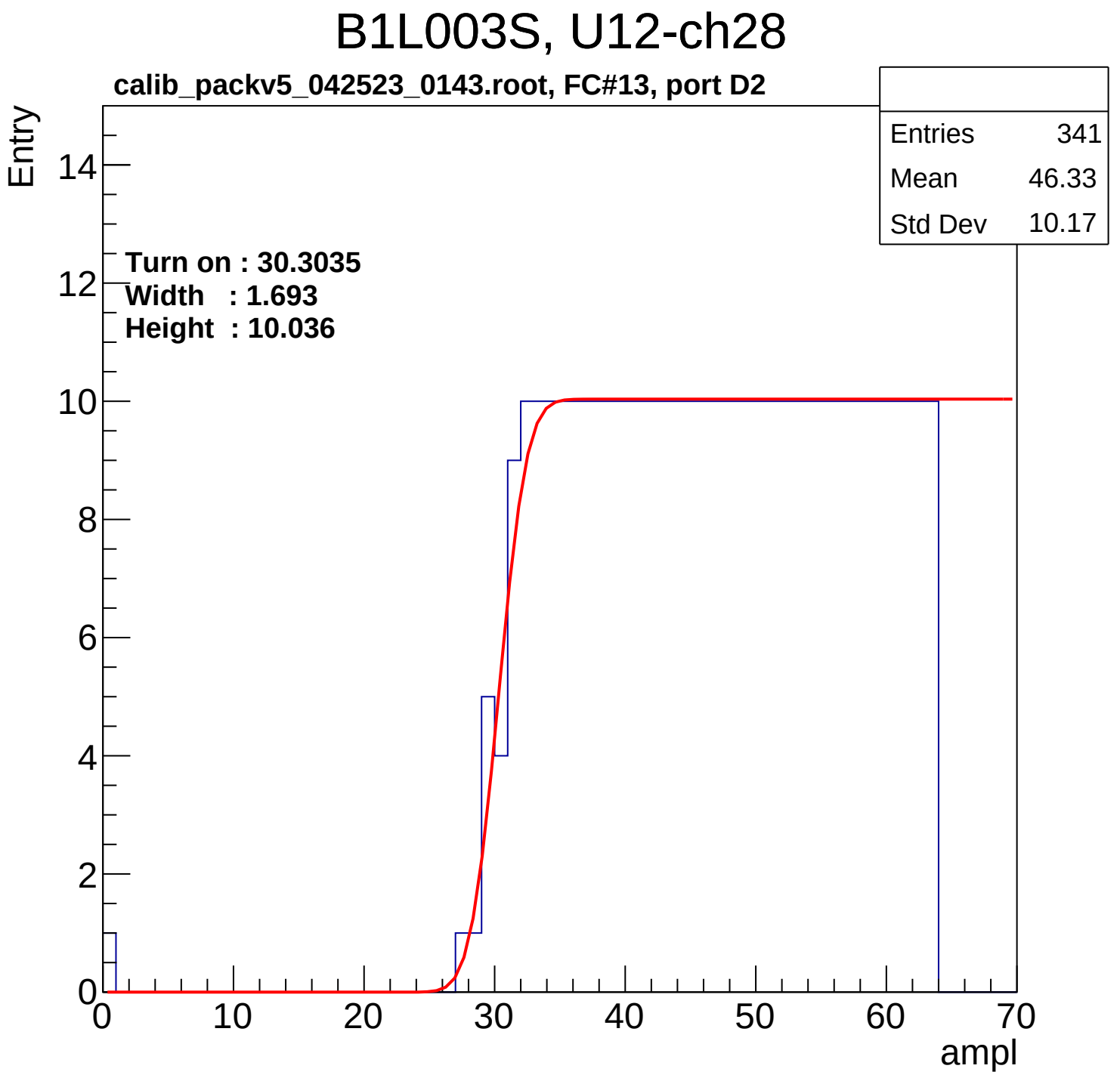

B1L003S, U12-ch23
calib_packv5_042523_0143.root, FC#13, port D2
Entries 364
Mean 45.04
Std Dev 11.12
Turn on : 28.1174
Width : 3.609
Height : 10.088
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

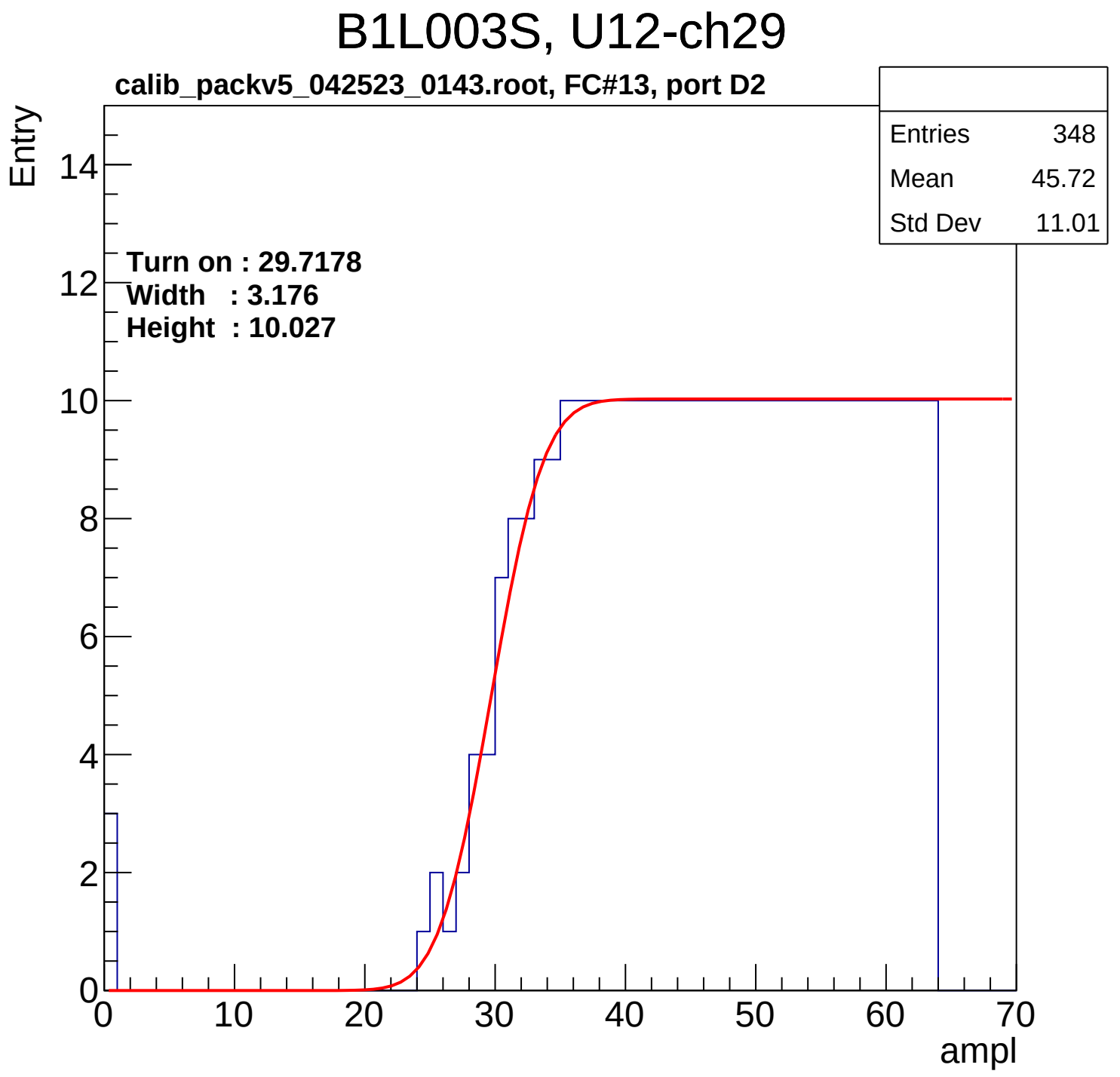

B1L003S, U12-ch24
calib_packv5_042523_0143.root, FC#13, port D2
Entries 368
Mean 44.87
Std Dev 11.18
Turn on : 27.2699
Width : 2.525
Height : 10.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

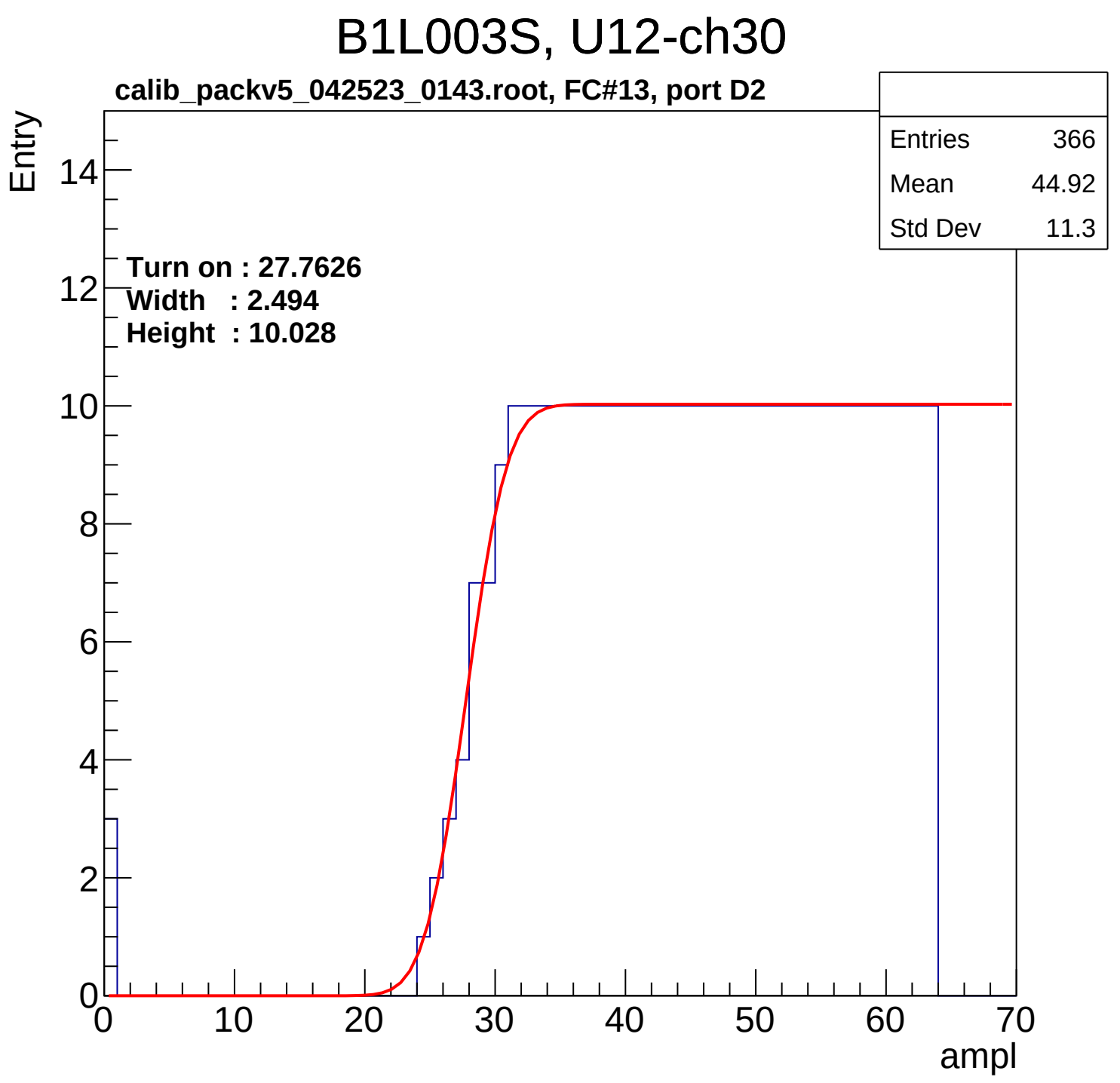

B1L003S, U12-ch25
calib_packv5_042523_0143.root, FC#13, port D2
Entries 362
Mean 45.1
Std Dev 11.22
Turn on : 27.9771
Width : 3.088
Height : 10.043
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

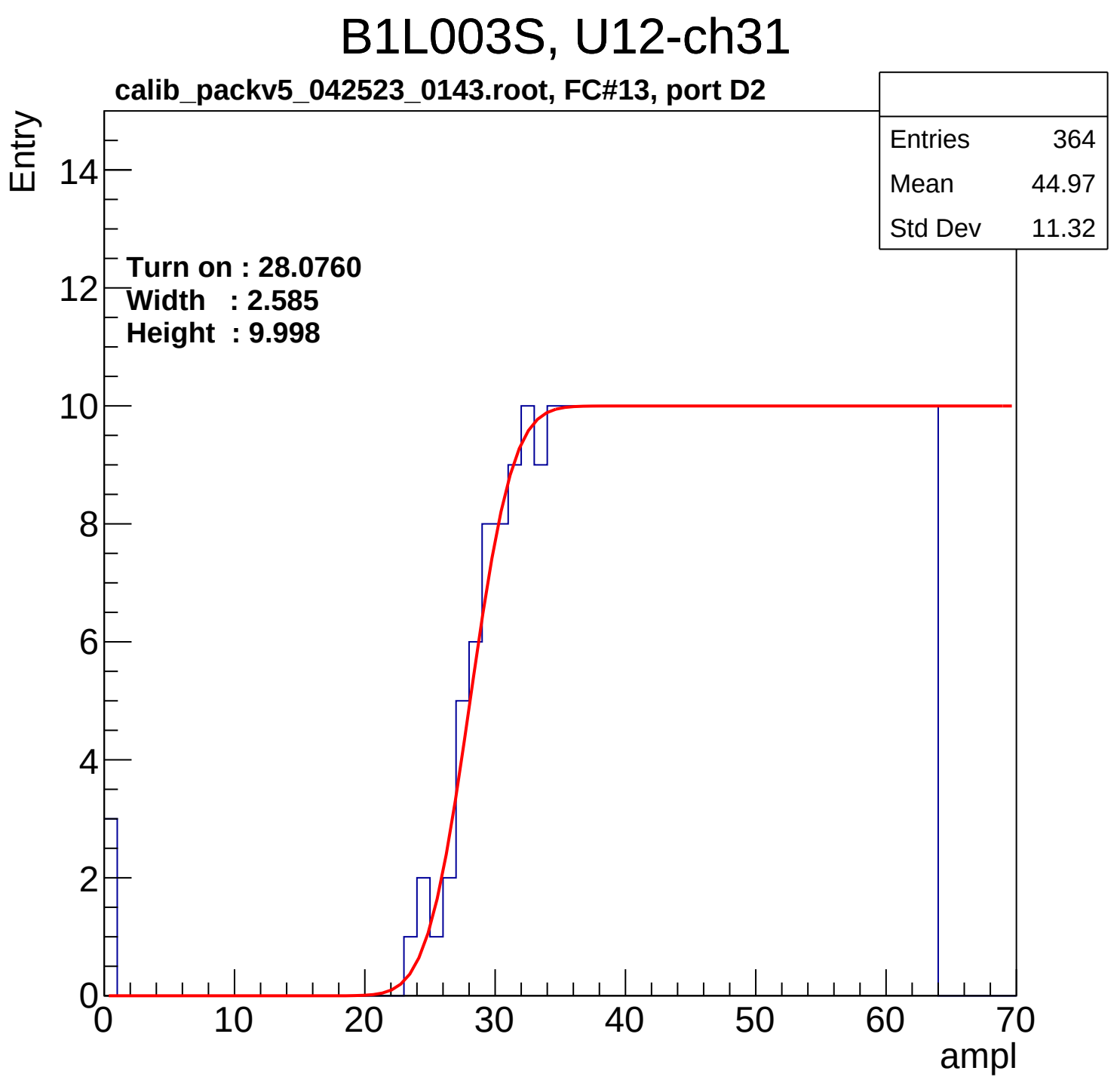

B1L003S, U12-ch26
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.67
Std Dev 11.42
Turn on : 27.0843
Width : 2.411
Height : 9.983
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

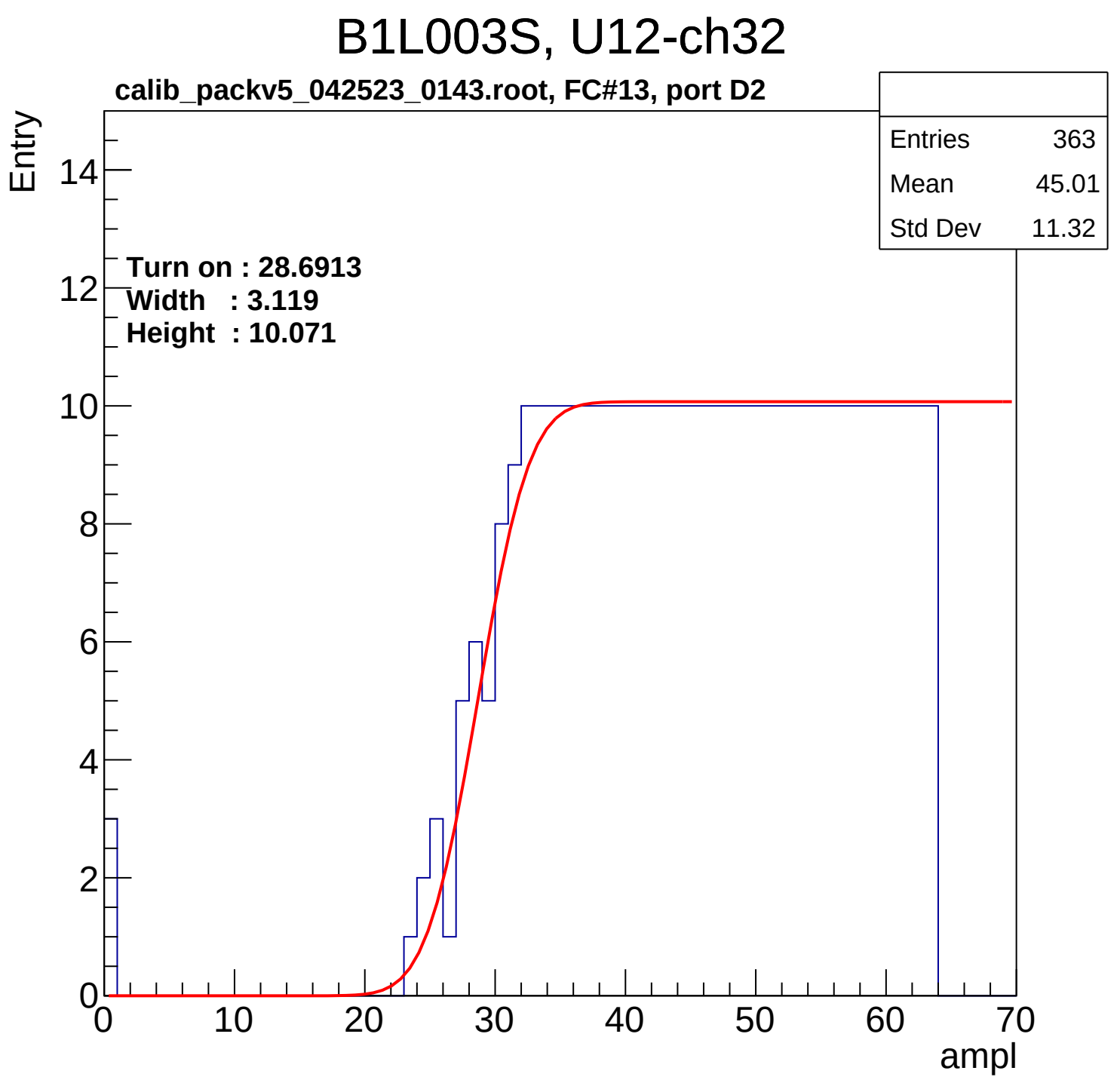

B1L003S, U12-ch27
calib_packv5_042523_0143.root, FC#13, port D2
Entries 389
Mean 43.83
Std Dev 11.8
Turn on : 25.3657
Width : 1.616
Height : 9.989
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

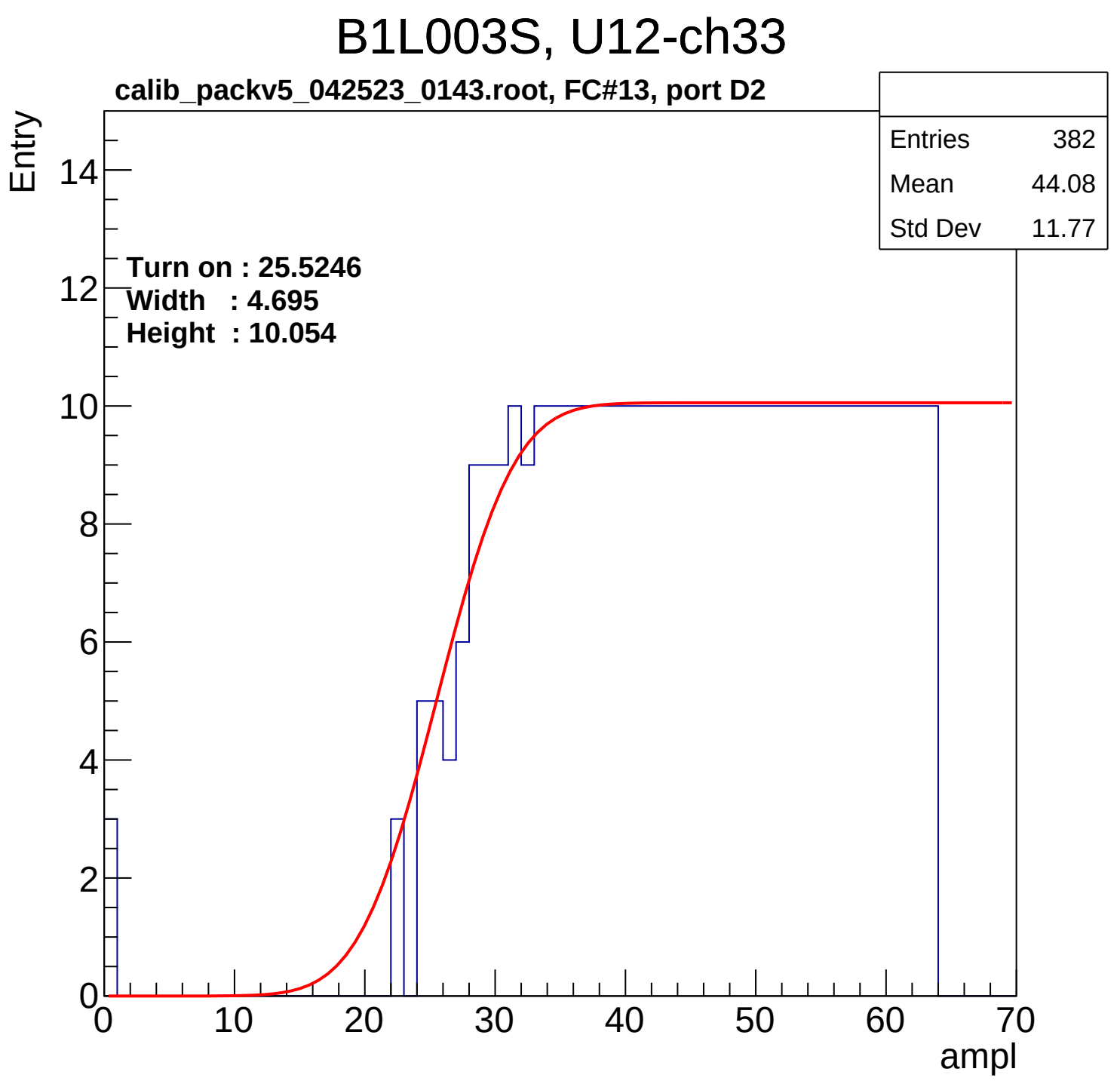

B1L003S, U12-ch28
calib_packv5_042523_0143.root, FC#13, port D2
Entries 341
Mean 46.33
Std Dev 10.17
Turn on : 30.3035
Width : 1.693
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

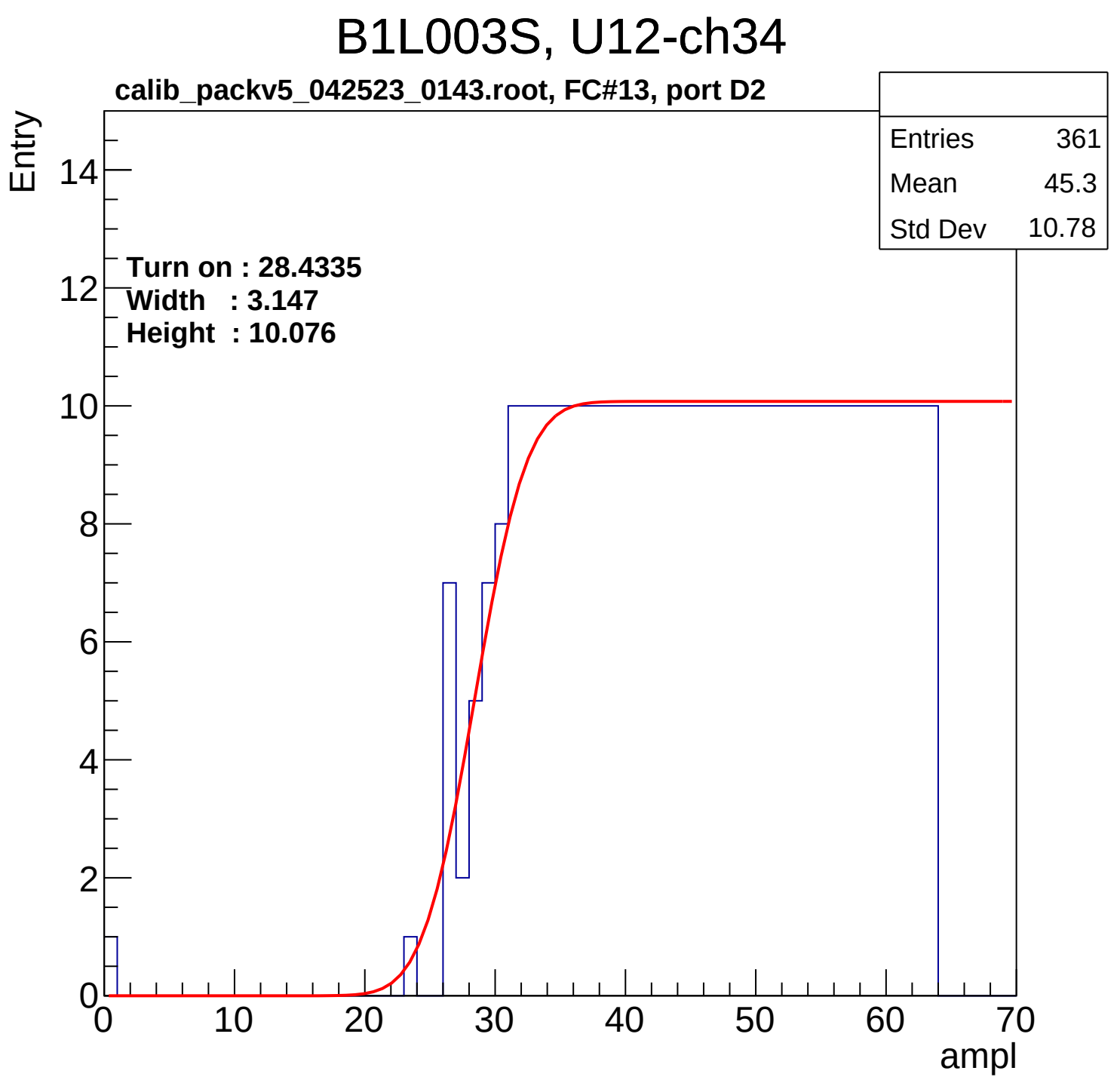

B1L003S, U12-ch29
calib_packv5_042523_0143.root, FC#13, port D2
Entries 348
Mean 45.72
Std Dev 11.01
Turn on : 29.7178
Width : 3.176
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

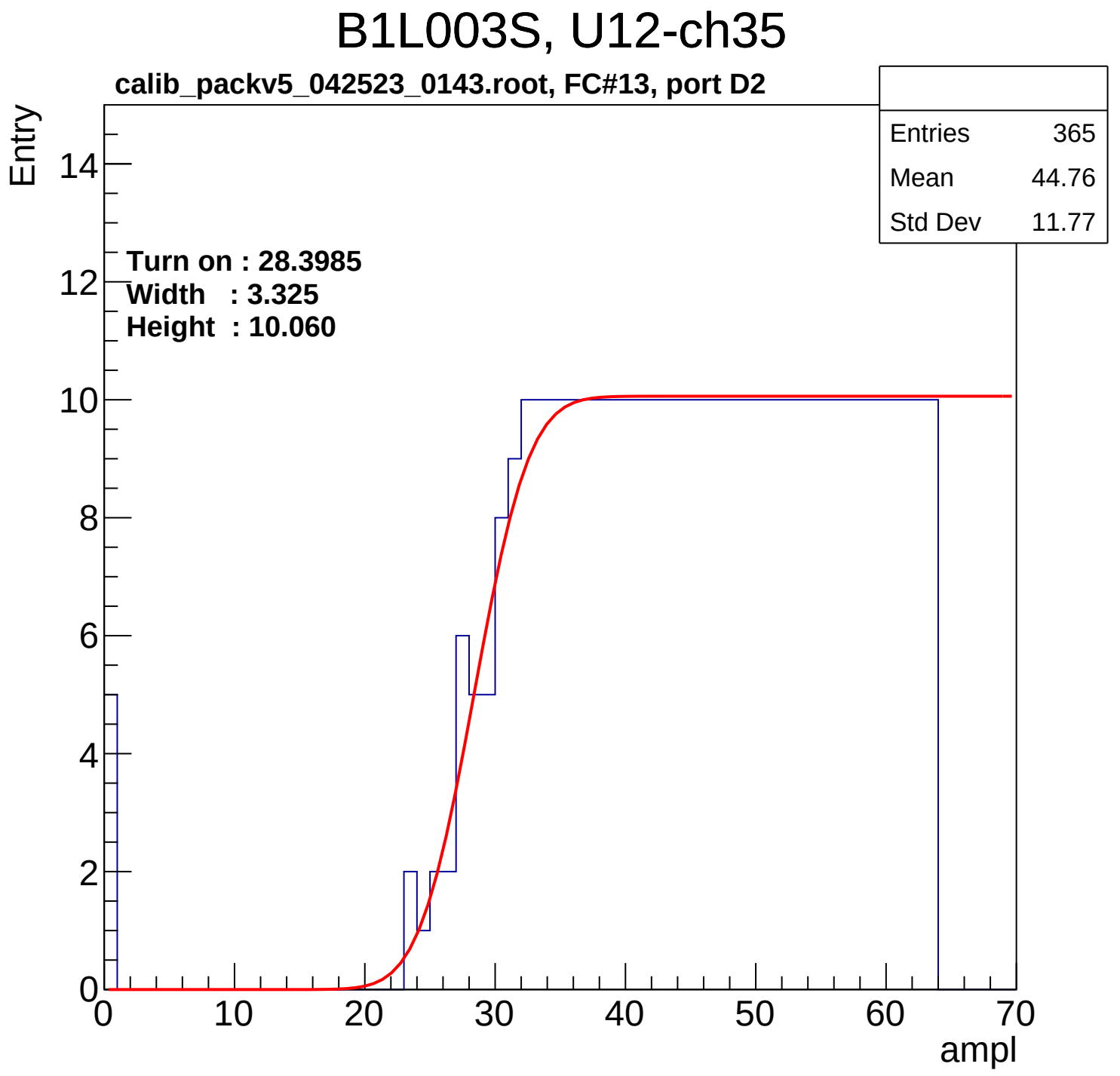

B1L003S, U12-ch30
calib_packv5_042523_0143.root, FC#13, port D2
Entries 366
Mean 44.92
Std Dev 11.3
Turn on : 27.7626
Width : 2.494
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

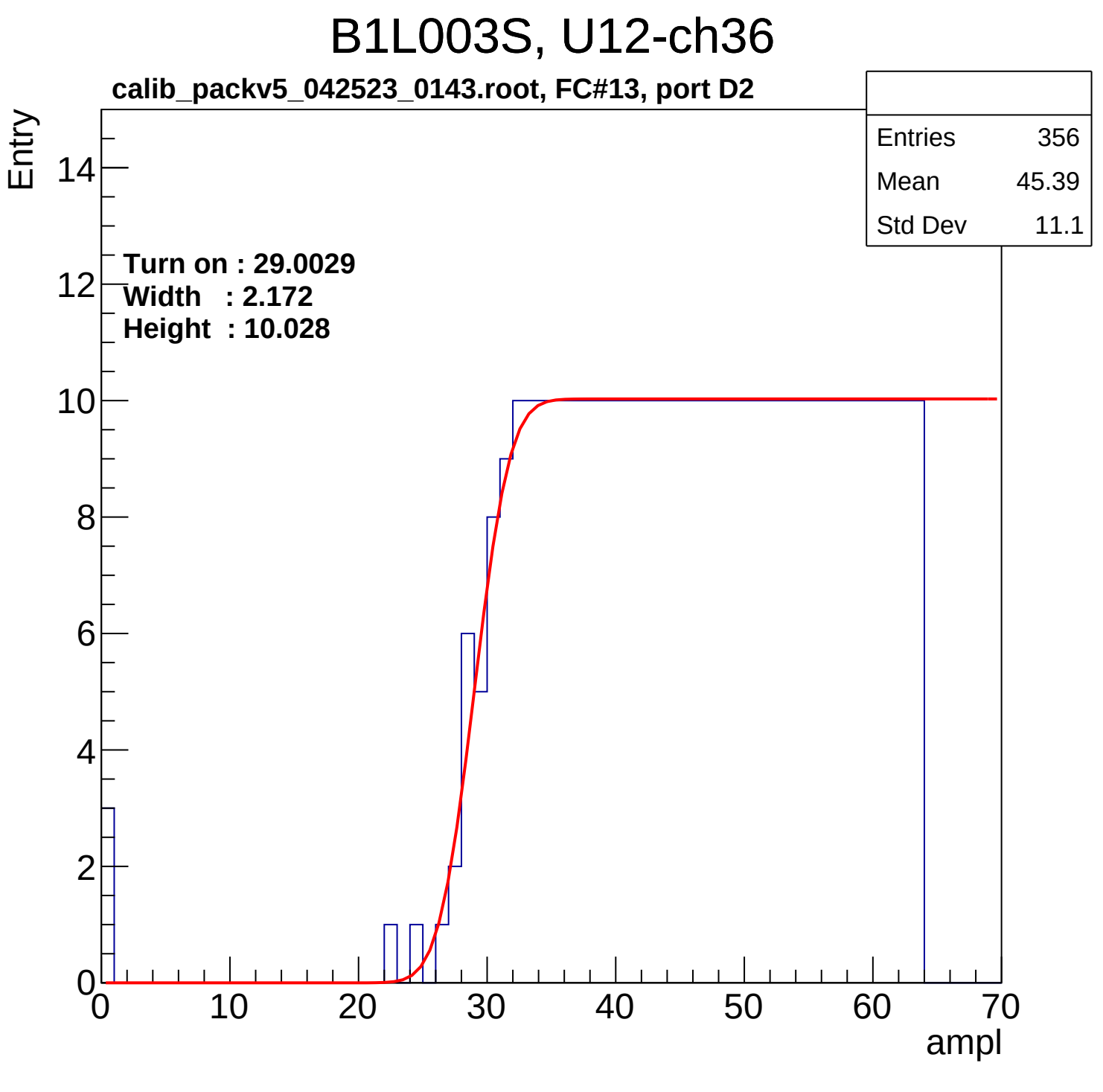

B1L003S, U12-ch31
calib_packv5_042523_0143.root, FC#13, port D2
Entries 364
Mean 44.97
Std Dev 11.32
Turn on : 28.0760
Width : 2.585
Height : 9.998
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

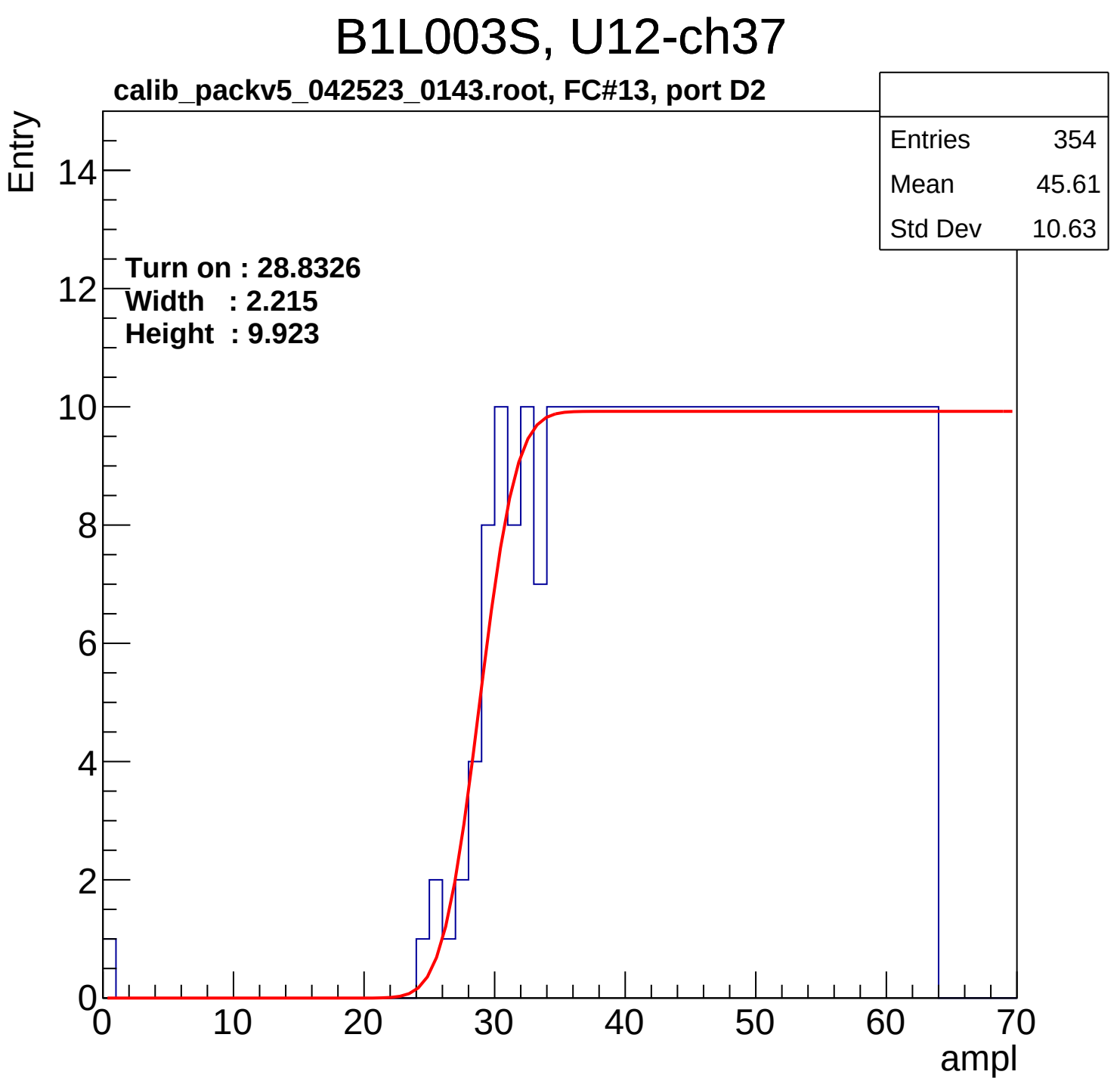

B1L003S, U12-ch32
calib_packv5_042523_0143.root, FC#13, port D2
Entries 363
Mean 45.01
Std Dev 11.32
Turn on : 28.6913
Width : 3.119
Height : 10.071
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

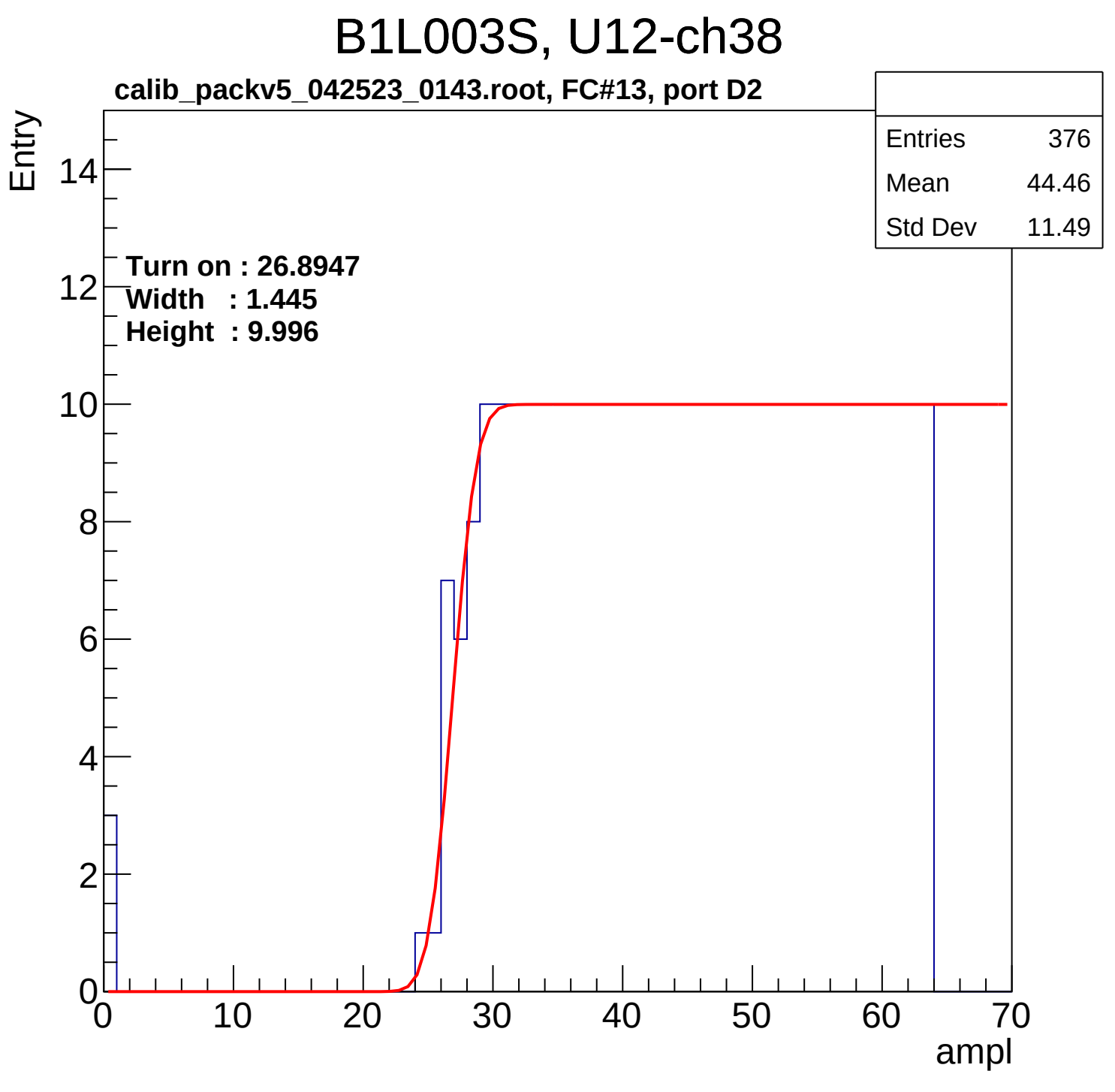

B1L003S, U12-ch33
calib_packv5_042523_0143.root, FC#13, port D2
Entries 382
Mean 44.08
Std Dev 11.77
Turn on : 25.5246
Width : 4.695
Height : 10.054
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

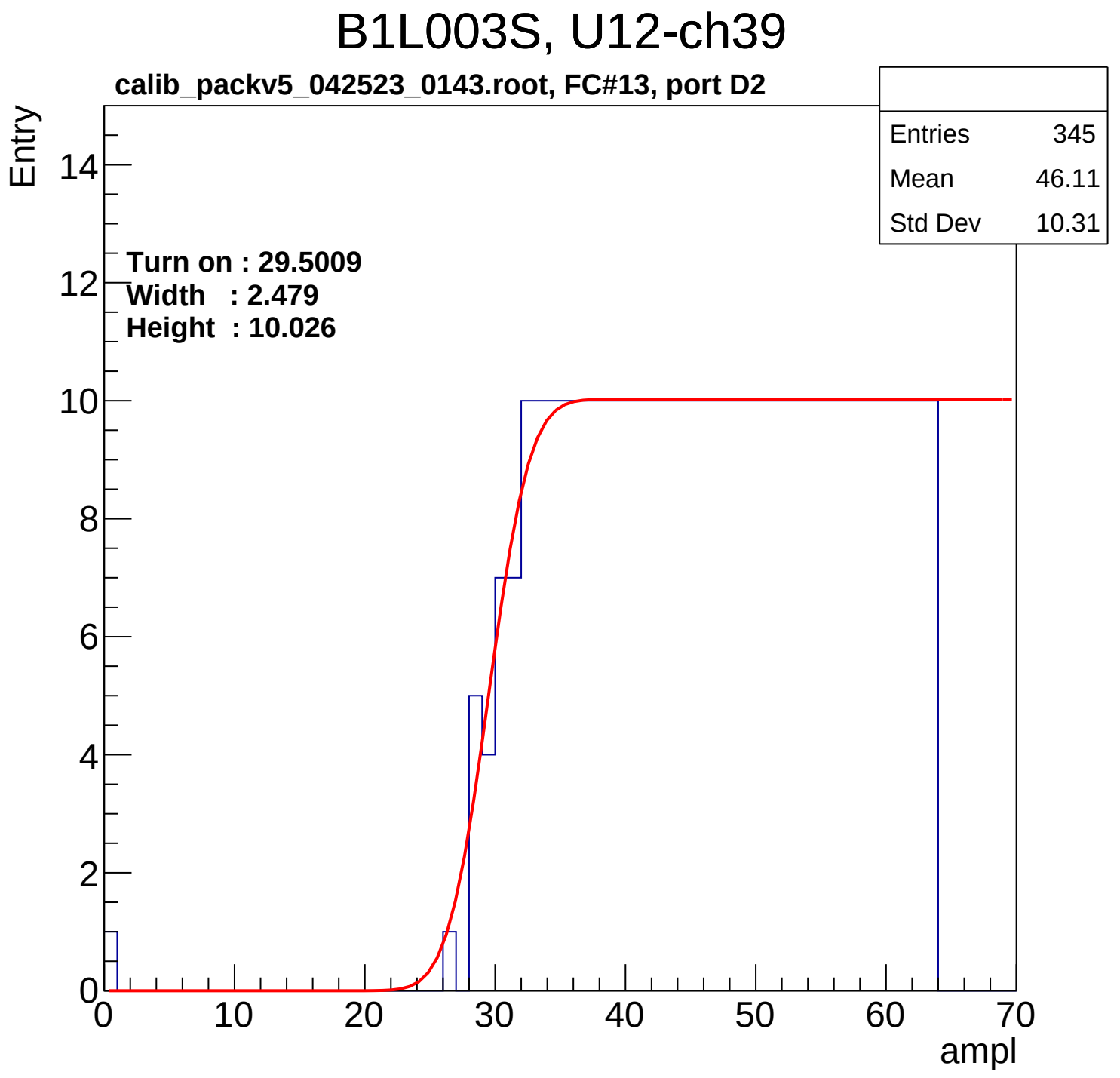

B1L003S, U12-ch34
calib_packv5_042523_0143.root, FC#13, port D2
Entries 361
Mean 45.3
Std Dev 10.78
Turn on : 28.4335
Width : 3.147
Height : 10.076
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

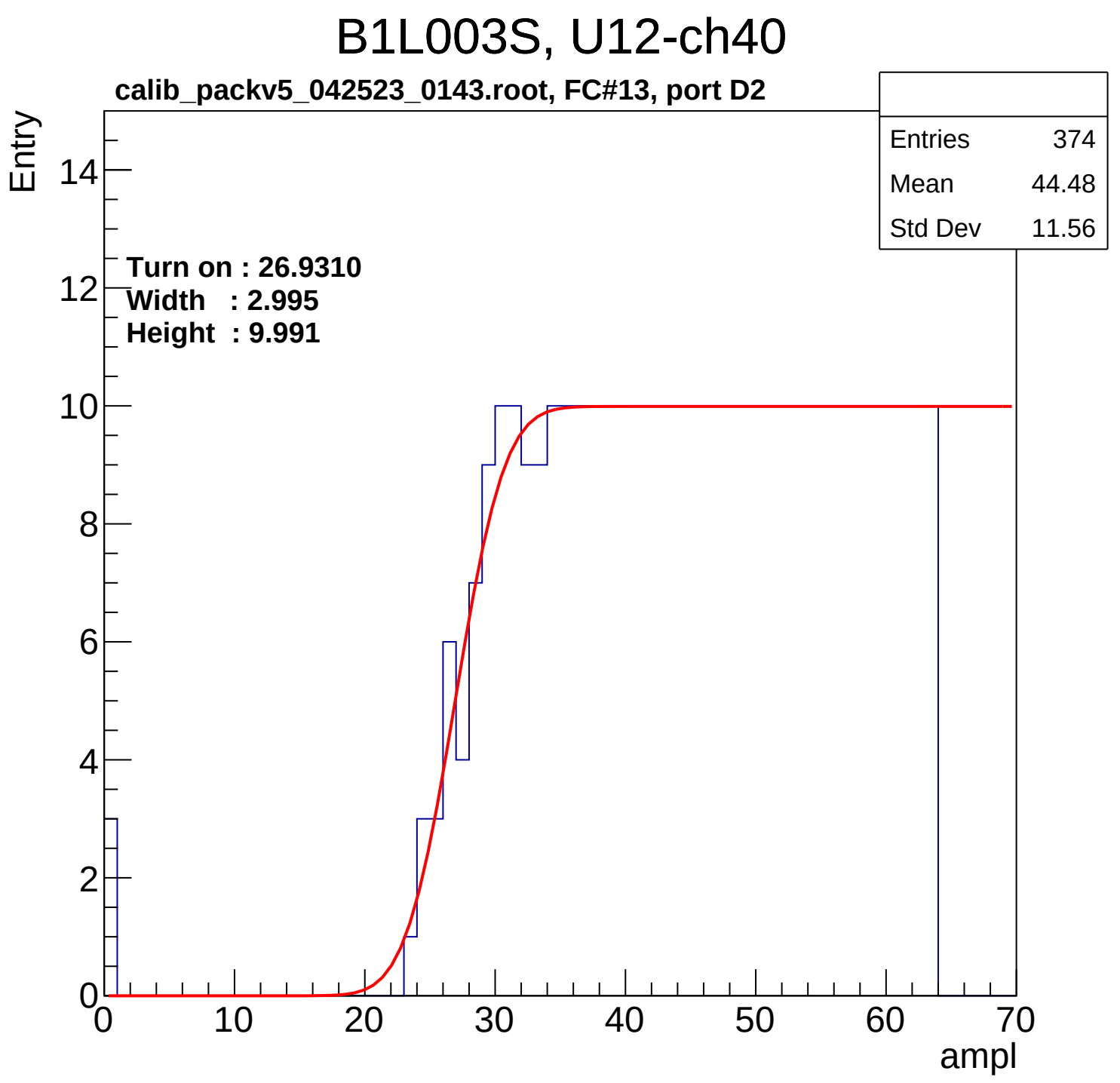

B1L003S, U12-ch35
calib_packv5_042523_0143.root, FC#13, port D2
Entries 365
Mean 44.76
Std Dev 11.77
Turn on : 28.3985
Width : 3.325
Height : 10.060
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

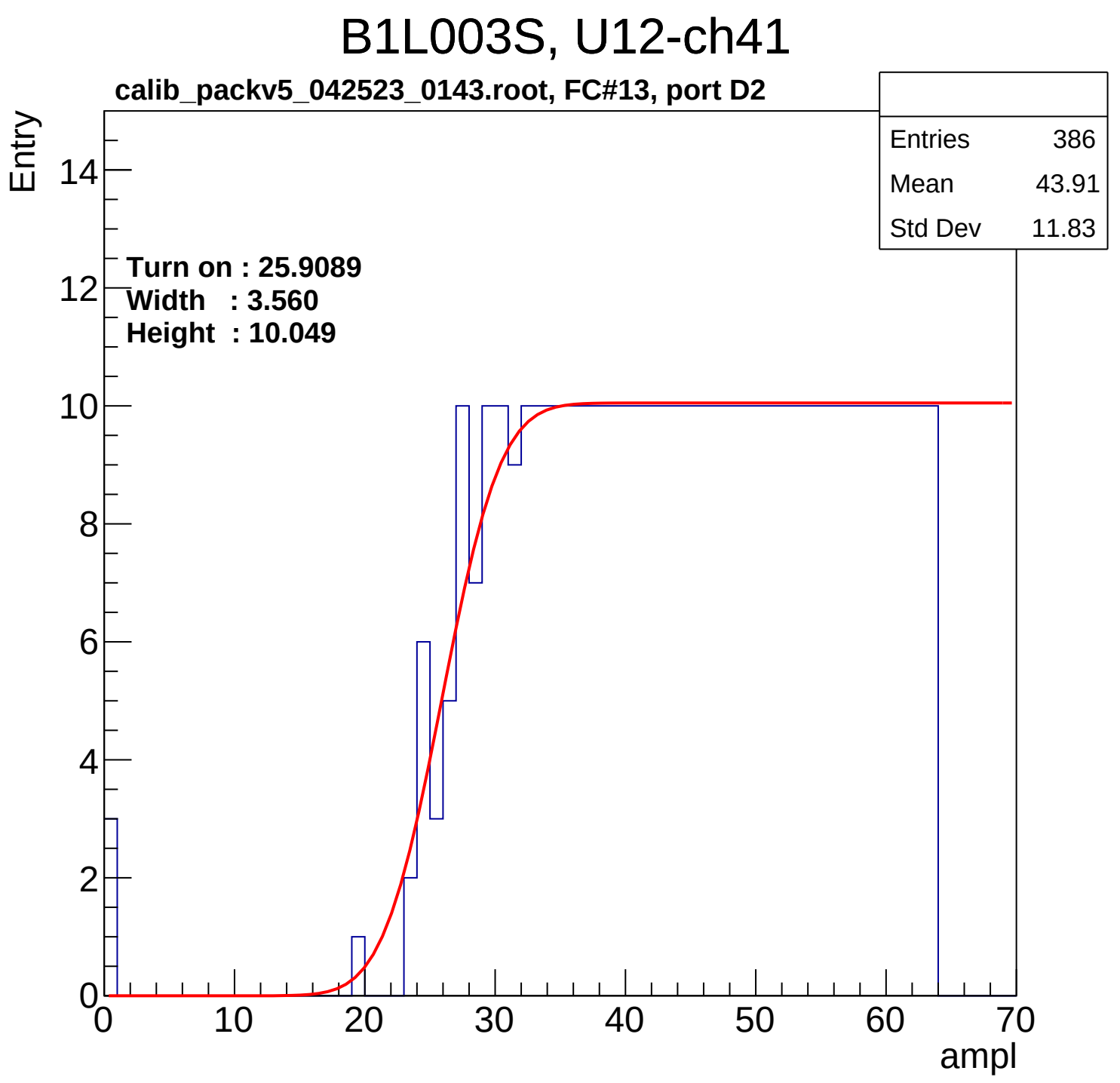

B1L003S, U12-ch36
calib_packv5_042523_0143.root, FC#13, port D2
Entries 356
Mean 45.39
Std Dev 11.1
Turn on : 29.0029
Width : 2.172
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

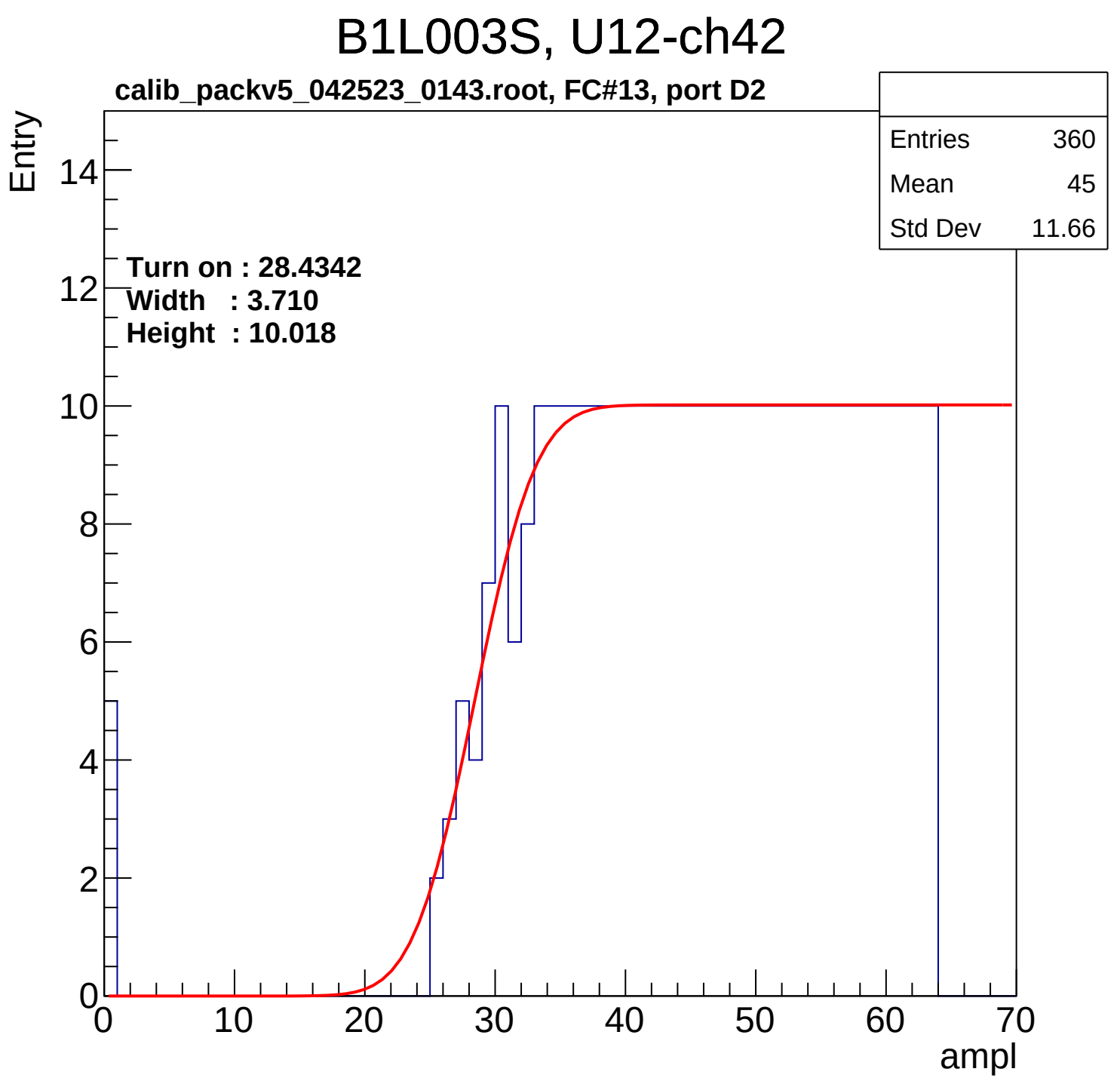

B1L003S, U12-ch37
calib_packv5_042523_0143.root, FC#13, port D2
Entries 354
Mean 45.61
Std Dev 10.63
Turn on : 28.8326
Width : 2.215
Height : 9.923
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

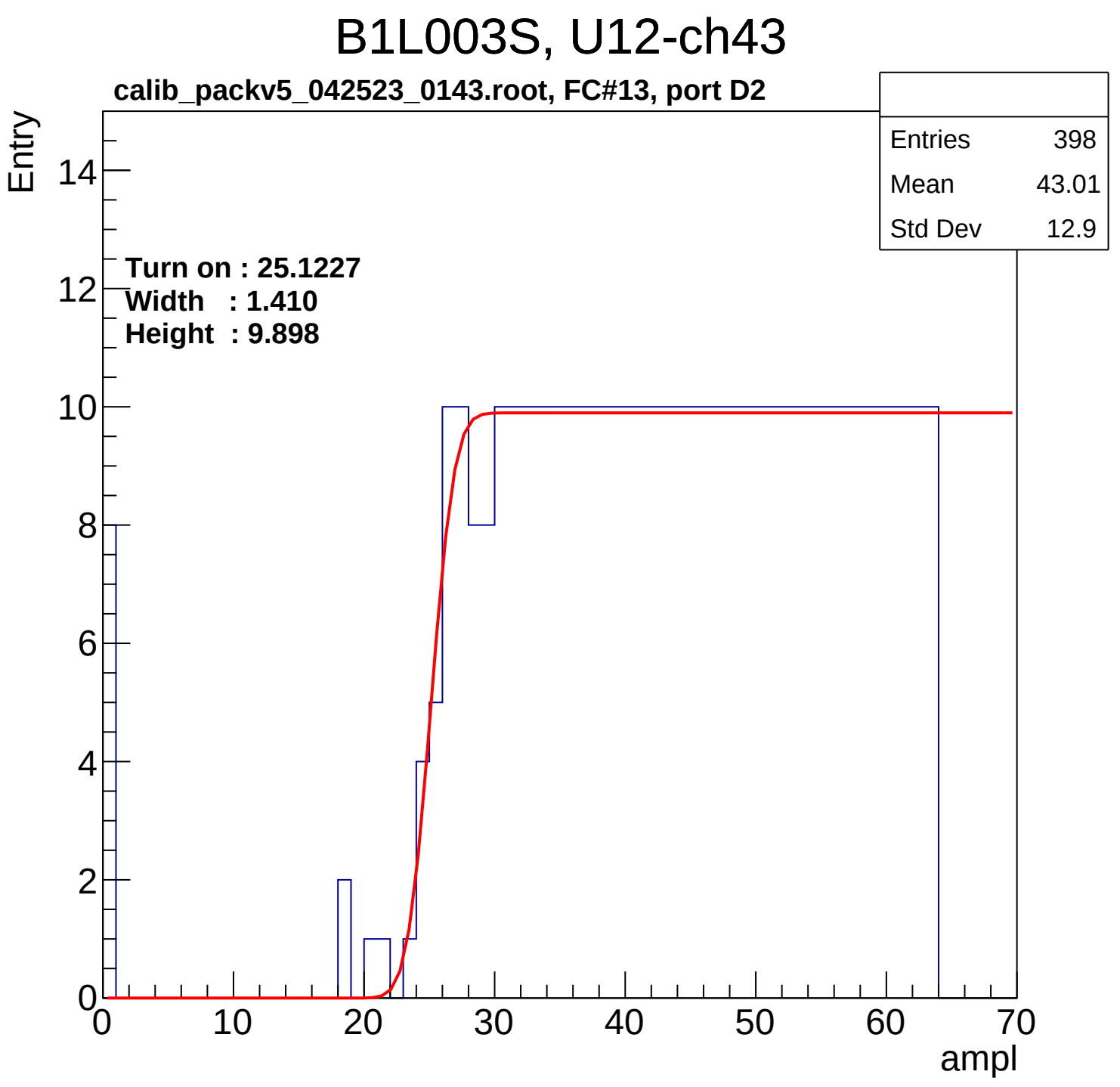

B1L003S, U12-ch38
calib_packv5_042523_0143.root, FC#13, port D2
Entries 376
Mean 44.46
Std Dev 11.49
Turn on : 26.8947
Width : 1.445
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

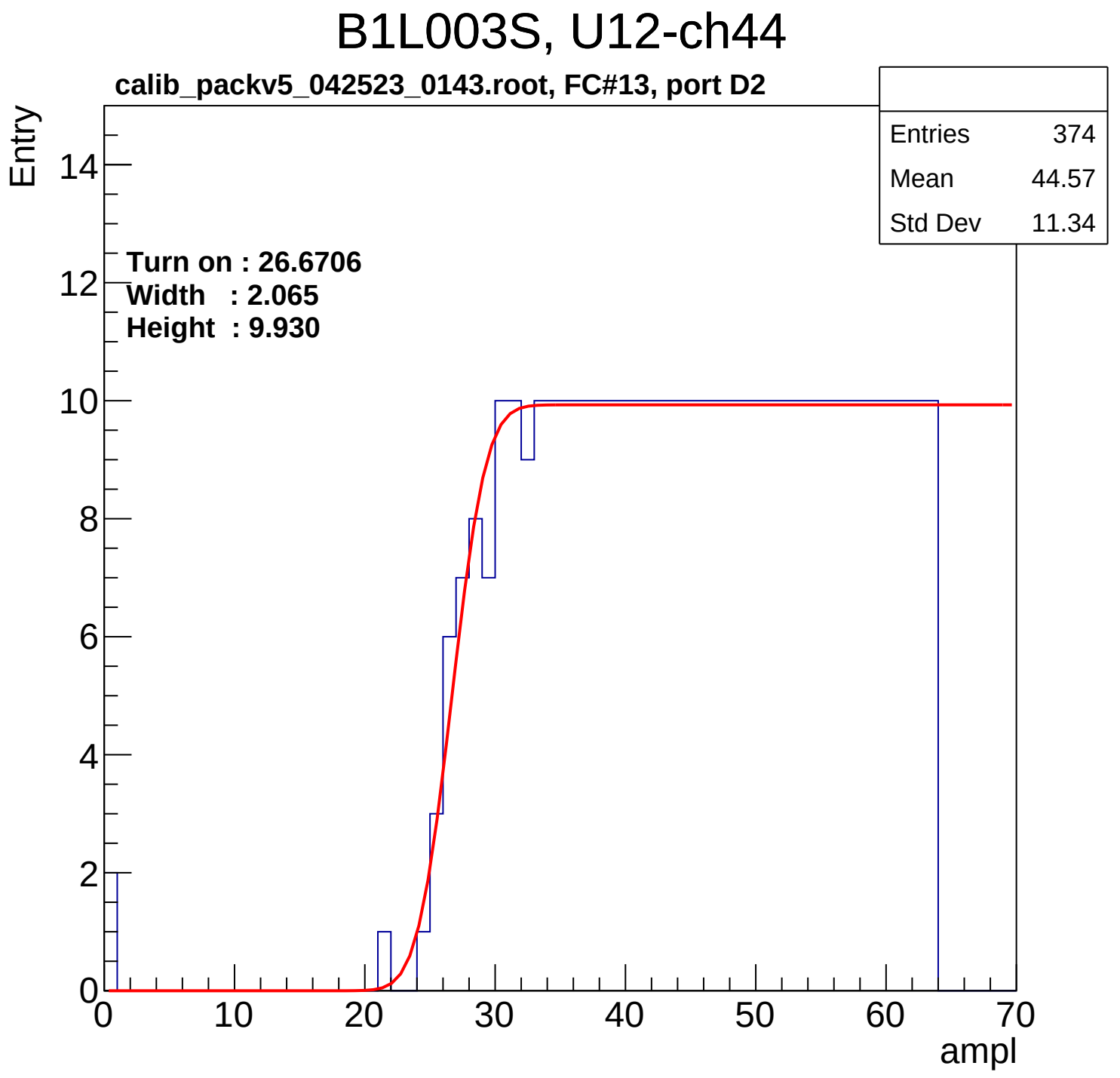

B1L003S, U12-ch39
calib_packv5_042523_0143.root, FC#13, port D2
Entries 345
Mean 46.11
Std Dev 10.31
Turn on : 29.5009
Width : 2.479
Height : 10.026
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

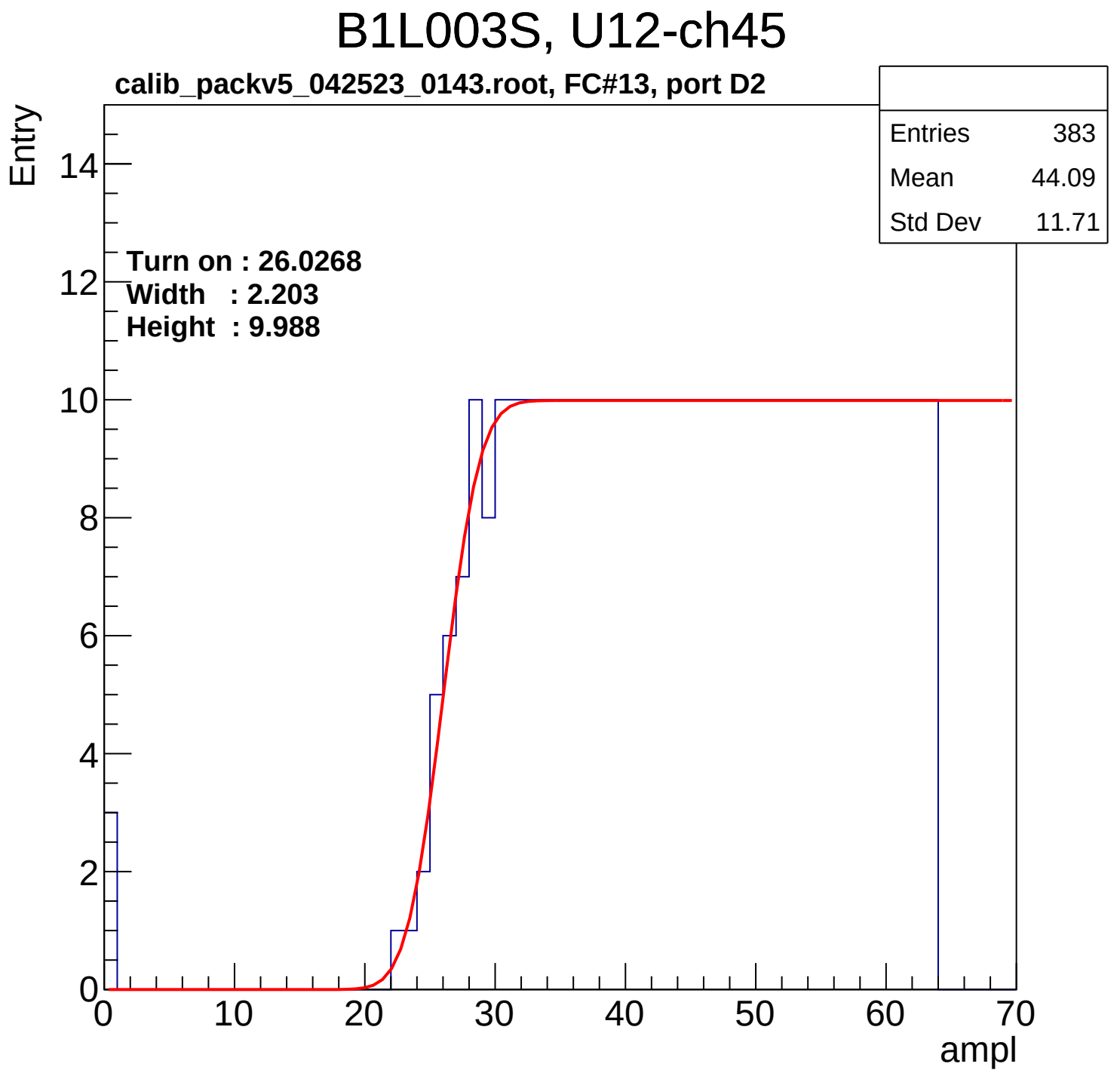

B1L003S, U12-ch40
calib_packv5_042523_0143.root, FC#13, port D2
Entries 374
Mean 44.48
Std Dev 11.56
Turn on : 26.9310
Width : 2.995
Height : 9.991
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

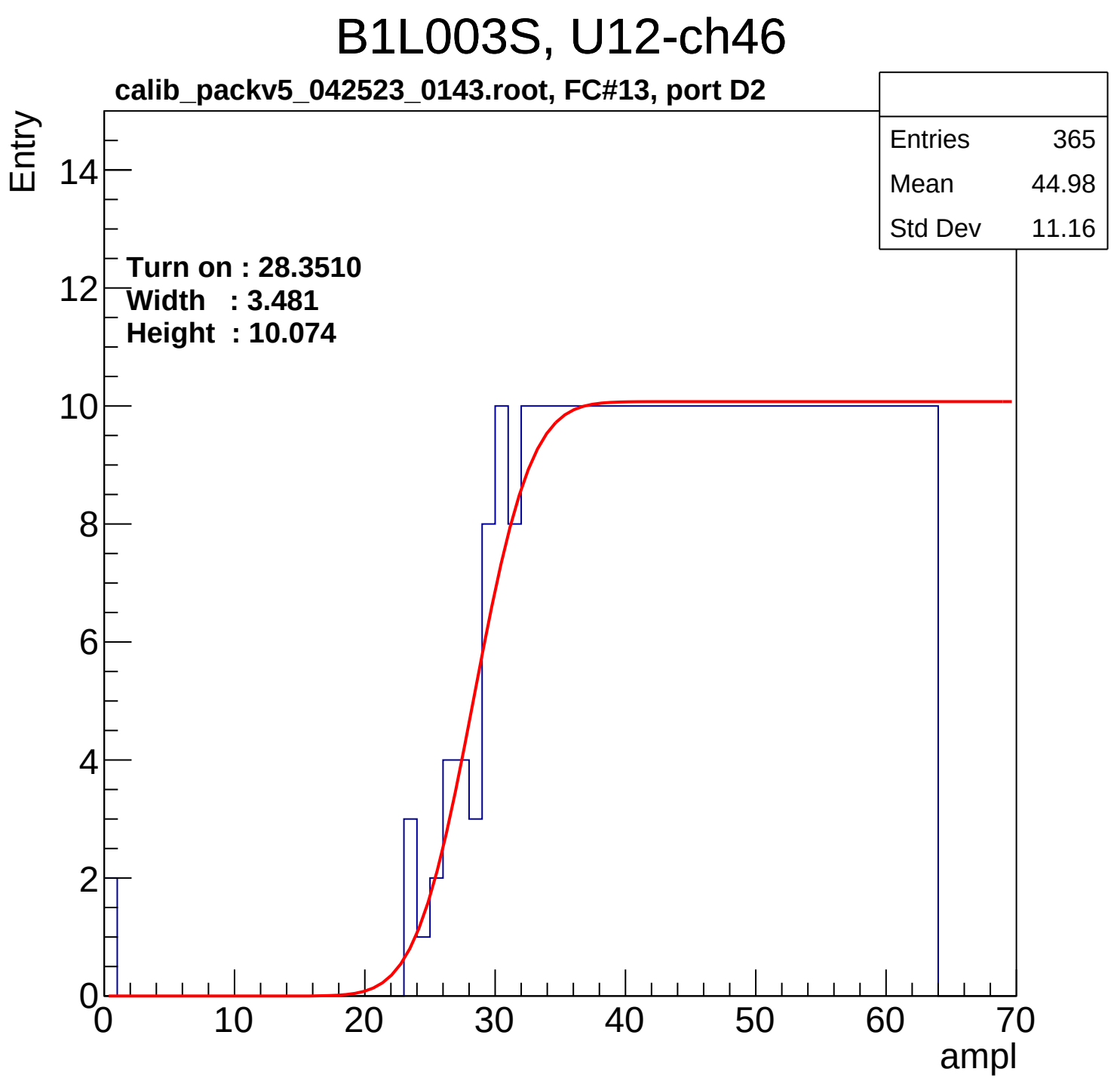

B1L003S, U12-ch41
calib_packv5_042523_0143.root, FC#13, port D2
Entries 386
Mean 43.91
Std Dev 11.83
Turn on : 25.9089
Width : 3.560
Height : 10.049
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

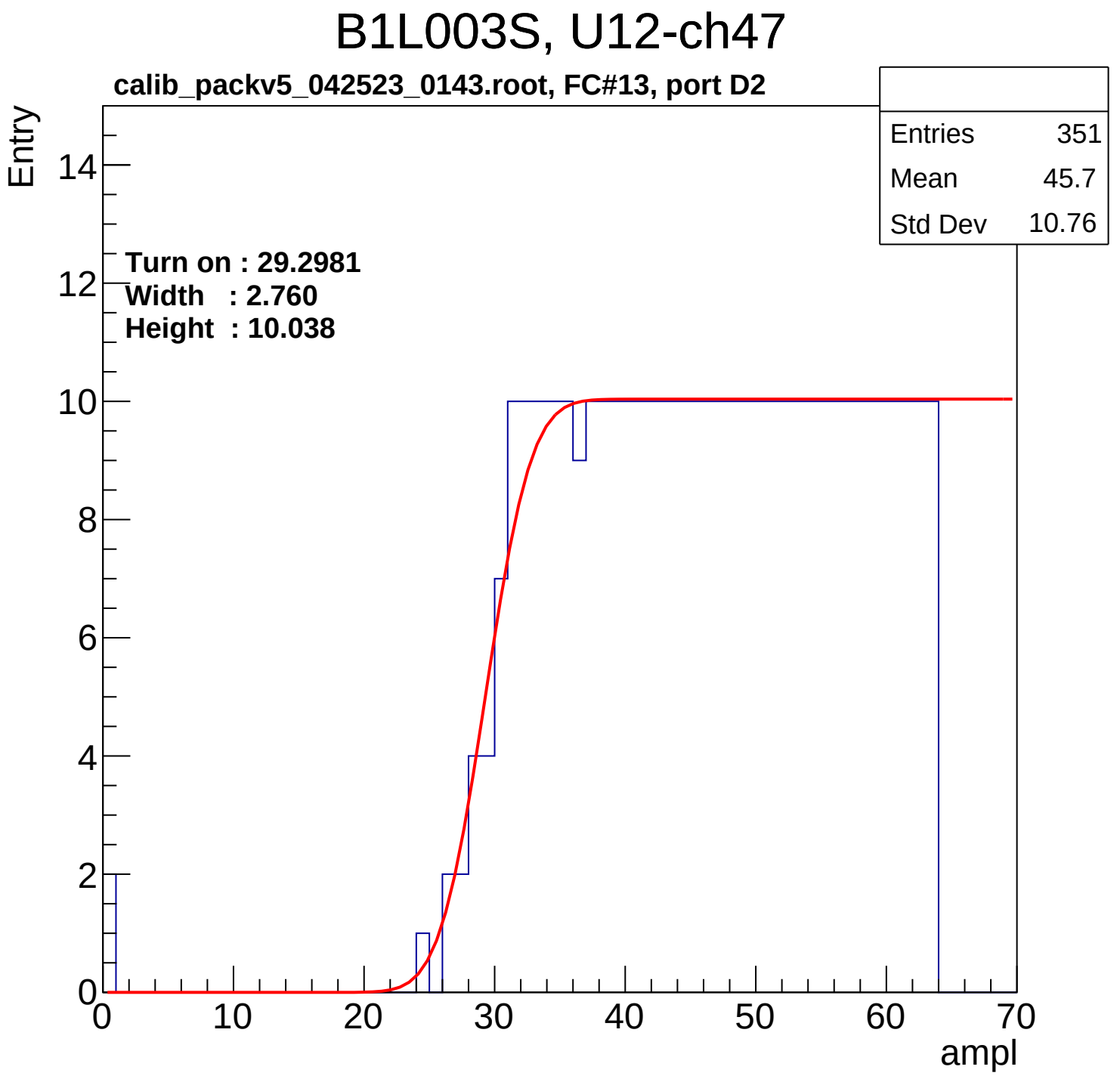

B1L003S, U12-ch42
calib_packv5_042523_0143.root, FC#13, port D2
Entries 360
Mean 45
Std Dev 11.66
Turn on : 28.4342
Width : 3.710
Height : 10.018
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

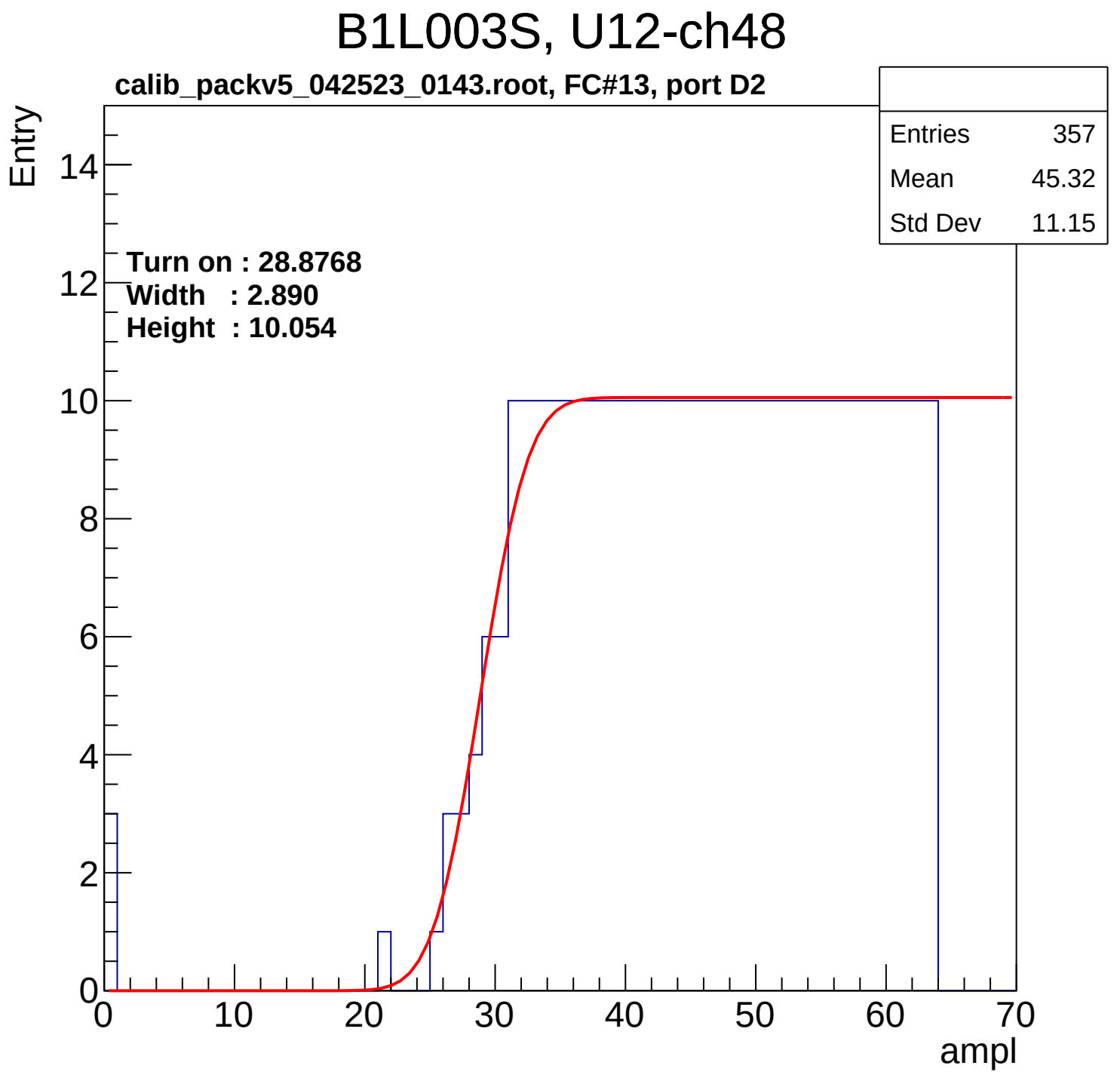

B1L003S, U12-ch43
calib_packv5_042523_0143.root, FC#13, port D2
Entries 398
Mean 43.01
Std Dev 12.9
Turn on : 25.1227
Width : 1.410
Height : 9.898
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

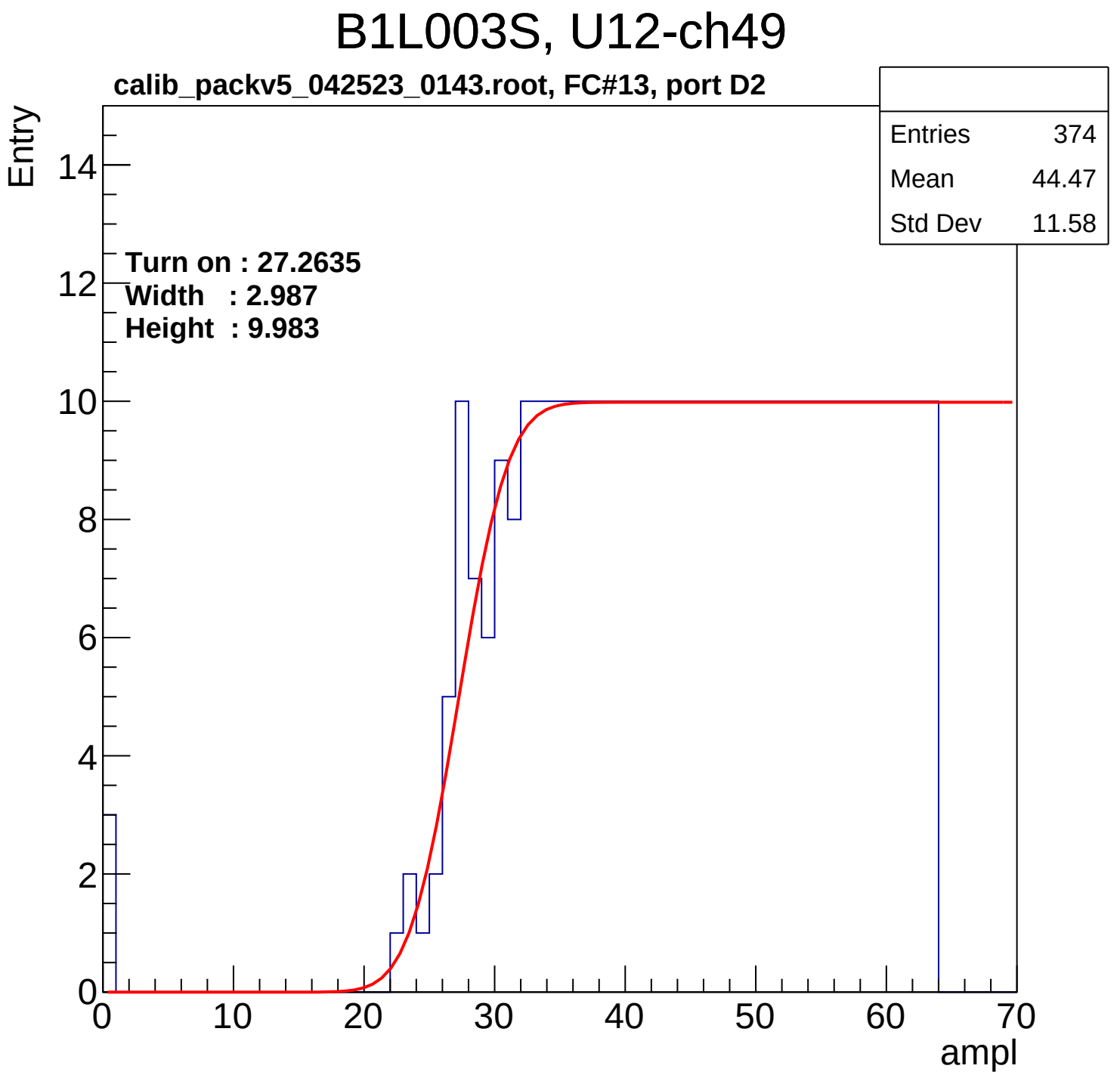

B1L003S, U12-ch44
calib_packv5_042523_0143.root, FC#13, port D2
Entries 374
Mean 44.57
Std Dev 11.34
Turn on : 26.6706
Width : 2.065
Height : 9.930
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

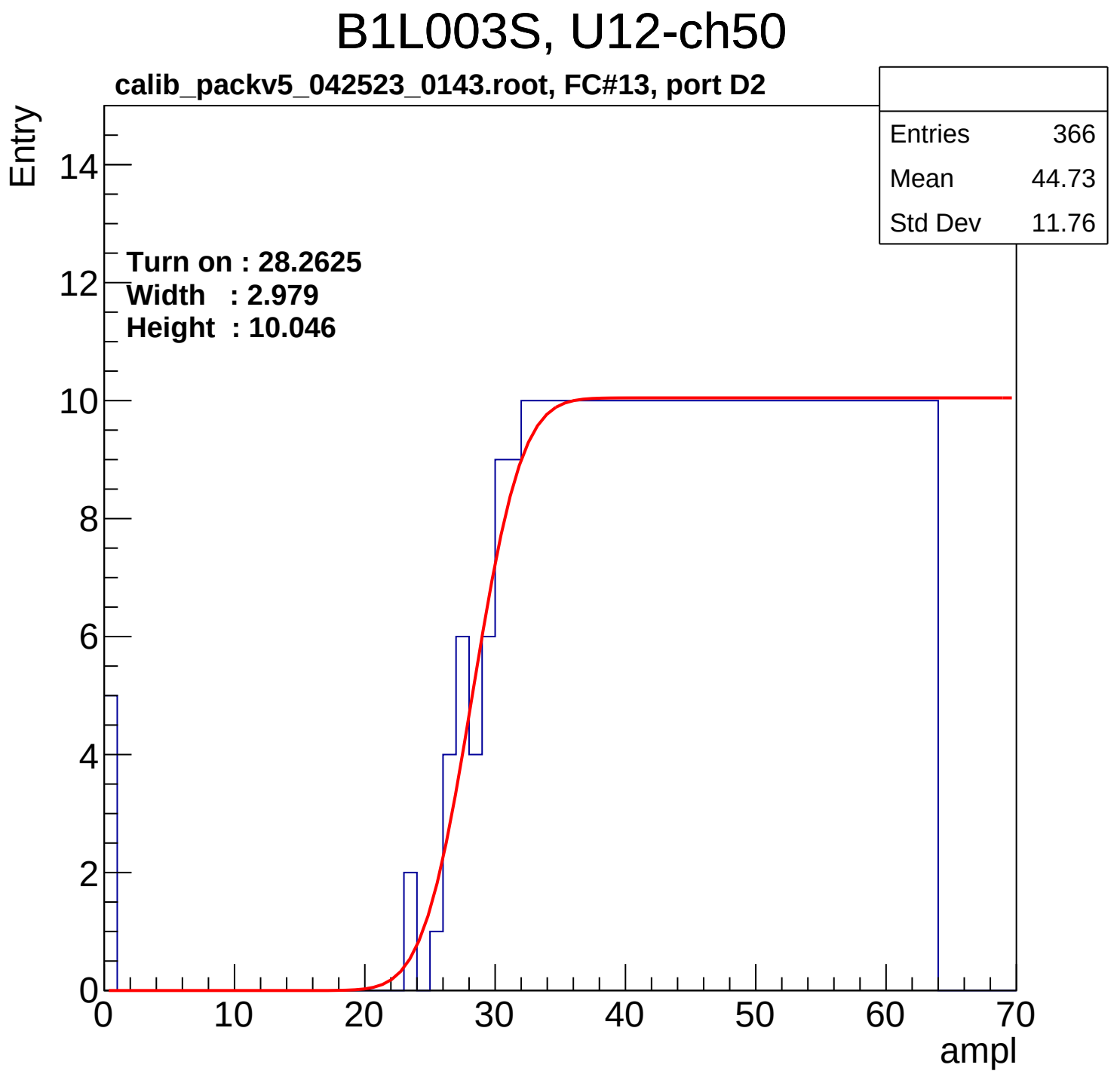

B1L003S, U12-ch45
calib_packv5_042523_0143.root, FC#13, port D2
Entries 383
Mean 44.09
Std Dev 11.71
Turn on : 26.0268
Width : 2.203
Height : 9.988
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

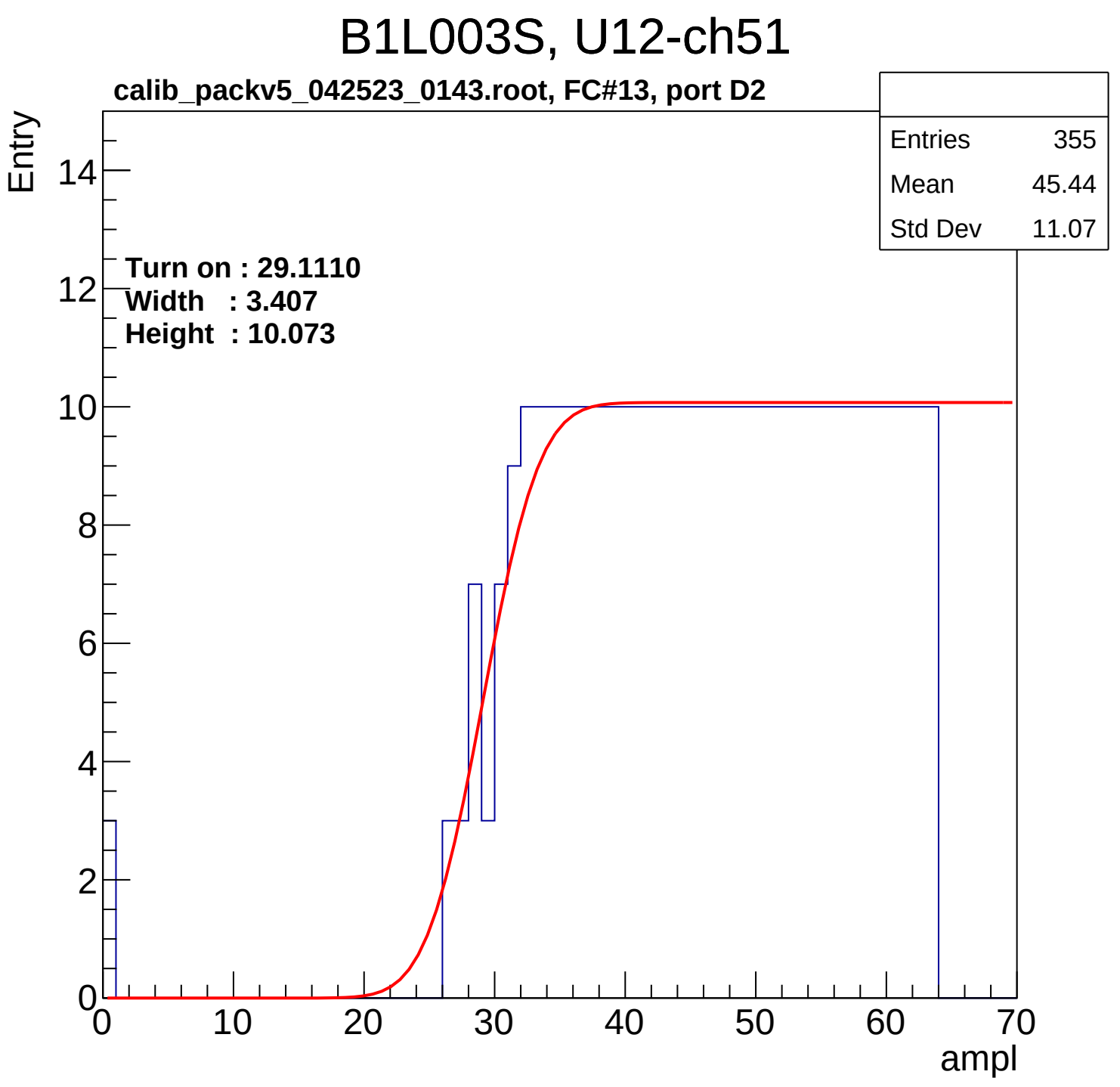

B1L003S, U12-ch46
calib_packv5_042523_0143.root, FC#13, port D2
Entries 365
Mean 44.98
Std Dev 11.16
Turn on : 28.3510
Width : 3.481
Height : 10.074
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

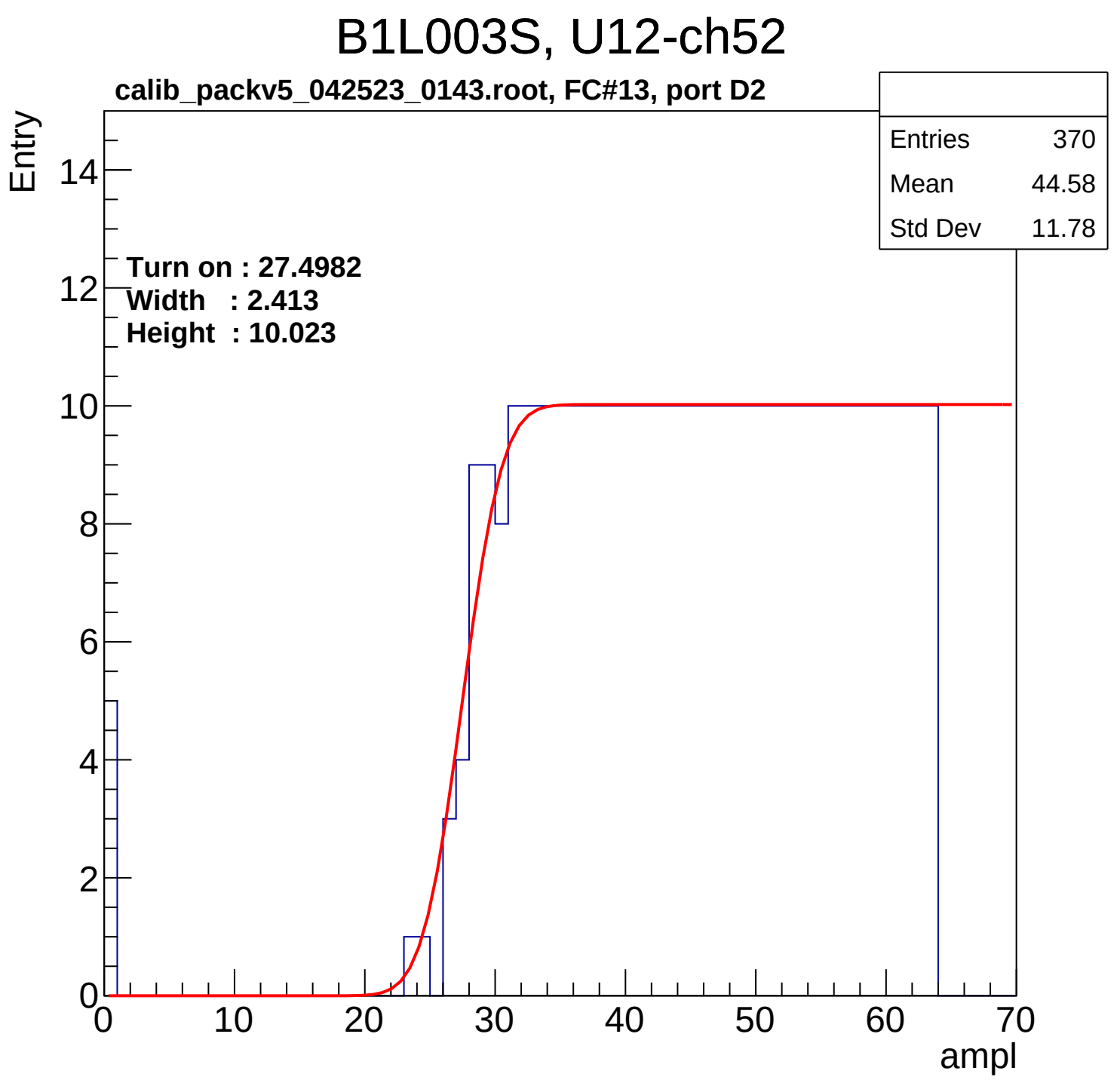

B1L003S, U12-ch47
calib_packv5_042523_0143.root, FC#13, port D2
Entries 351
Mean 45.7
Std Dev 10.76
Turn on : 29.2981
Width : 2.760
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

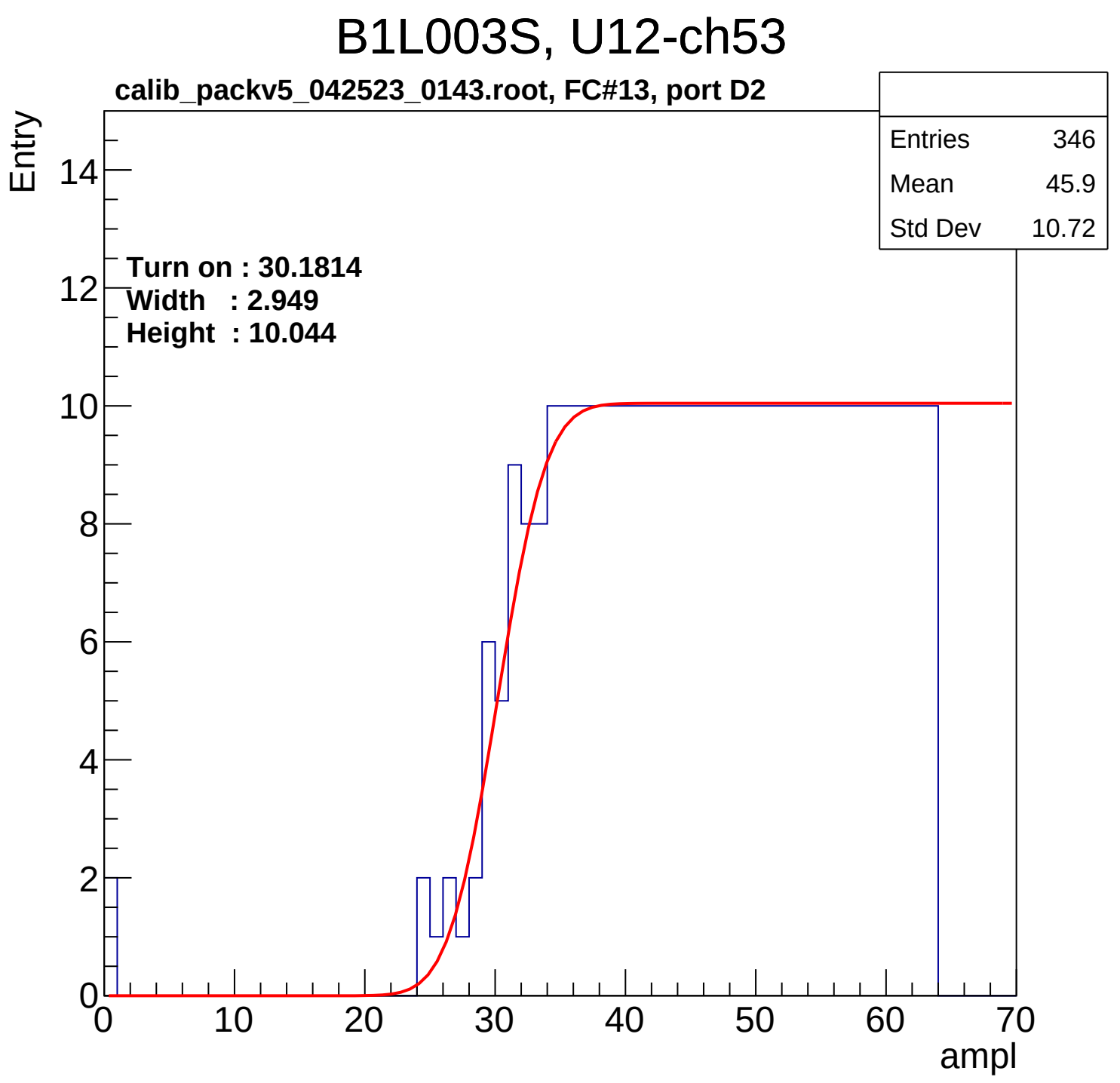

B1L003S, U12-ch48
calib_packv5_042523_0143.root, FC#13, port D2
Entries 357
Mean 45.32
Std Dev 11.15
Turn on : 28.8768
Width : 2.890
Height : 10.054
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

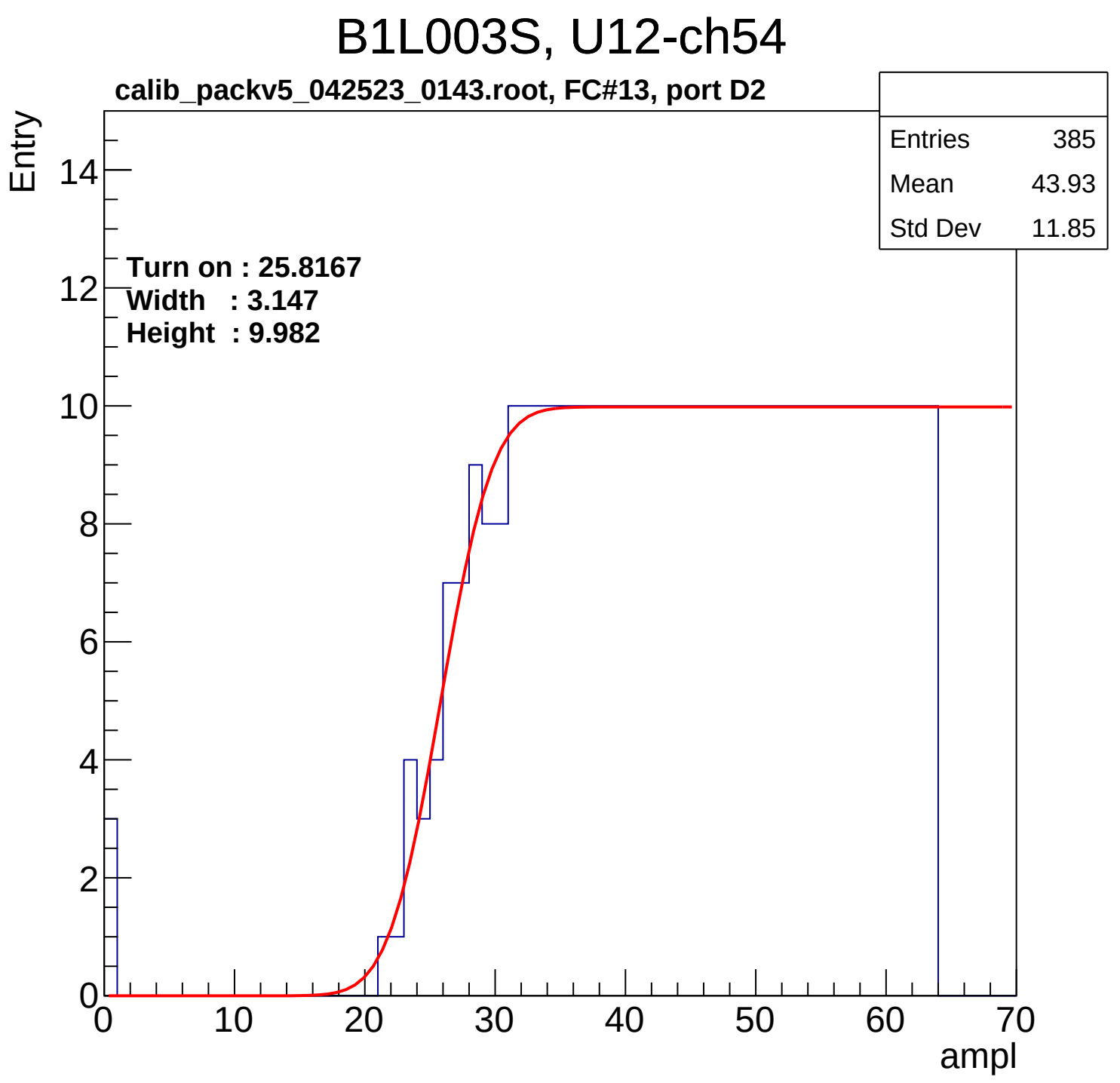

B1L003S, U12-ch49
calib_packv5_042523_0143.root, FC#13, port D2
Entries 374
Mean 44.47
Std Dev 11.58
Turn on : 27.2635
Width : 2.987
Height : 9.983
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

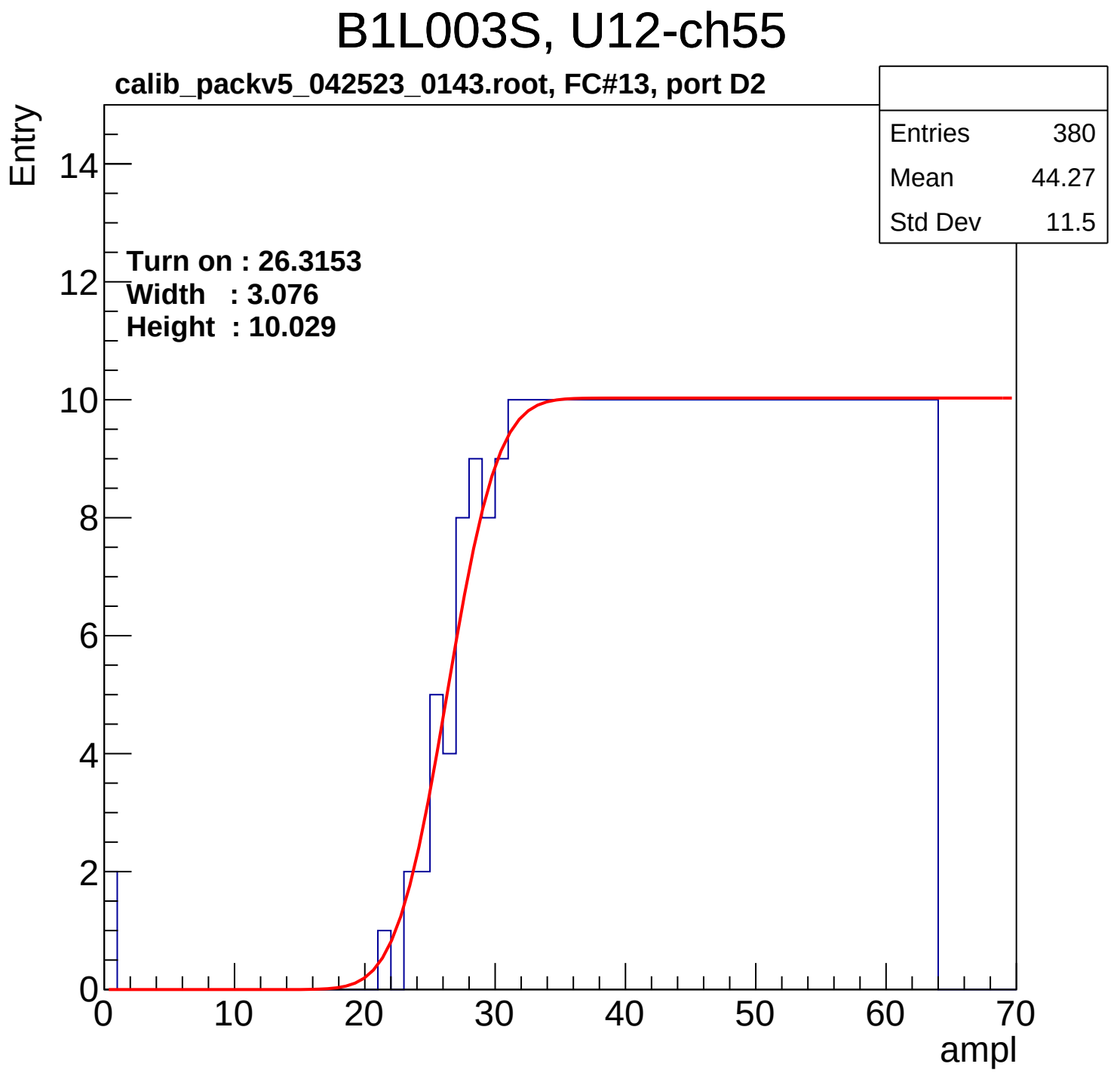

B1L003S, U12-ch50
calib_packv5_042523_0143.root, FC#13, port D2
Entries 366
Mean 44.73
Std Dev 11.76
Turn on : 28.2625
Width : 2.979
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

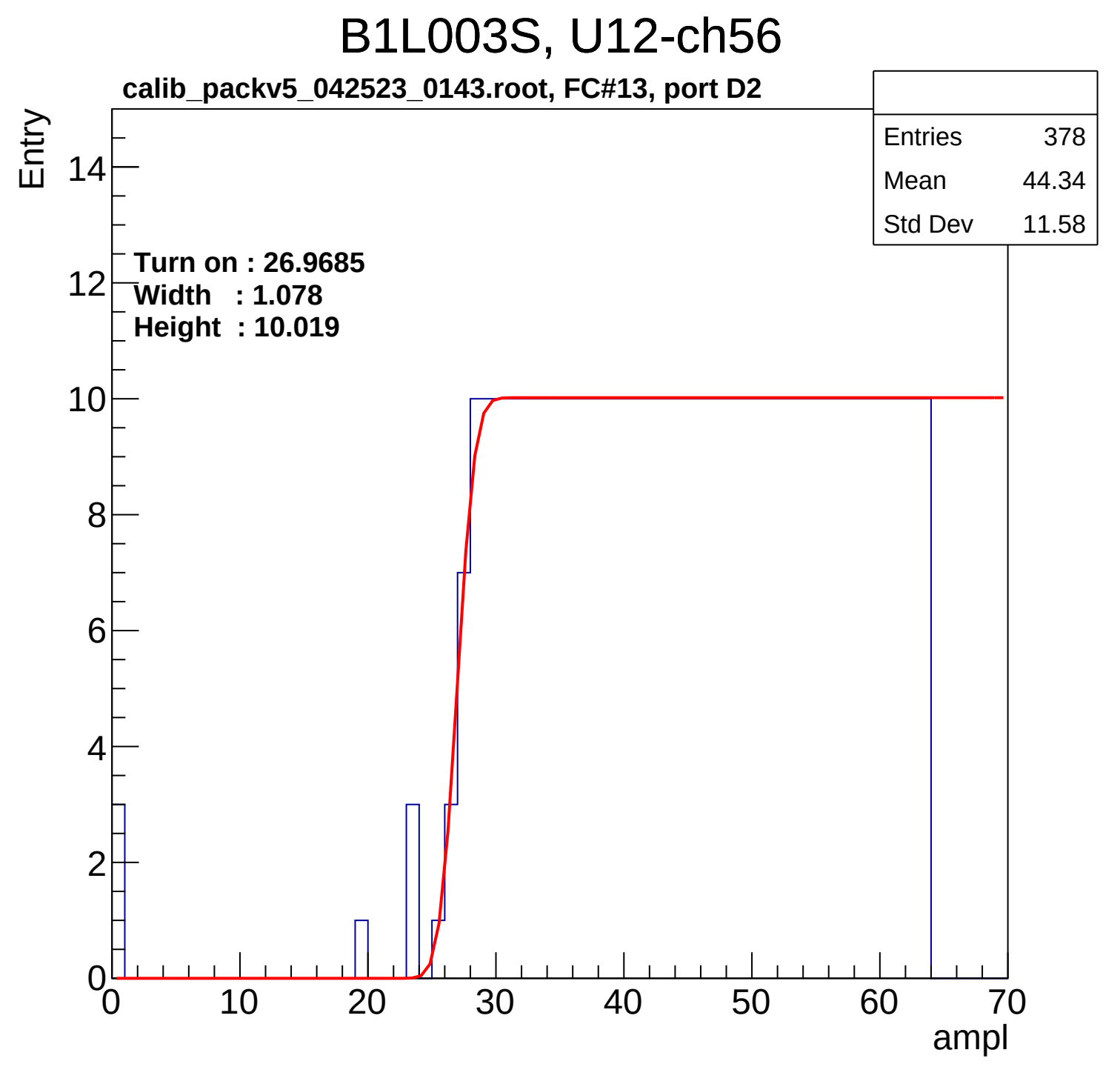

B1L003S, U12-ch51
calib_packv5_042523_0143.root, FC#13, port D2
Entries 355
Mean 45.44
Std Dev 11.07
Turn on : 29.1110
Width : 3.407
Height : 10.073
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

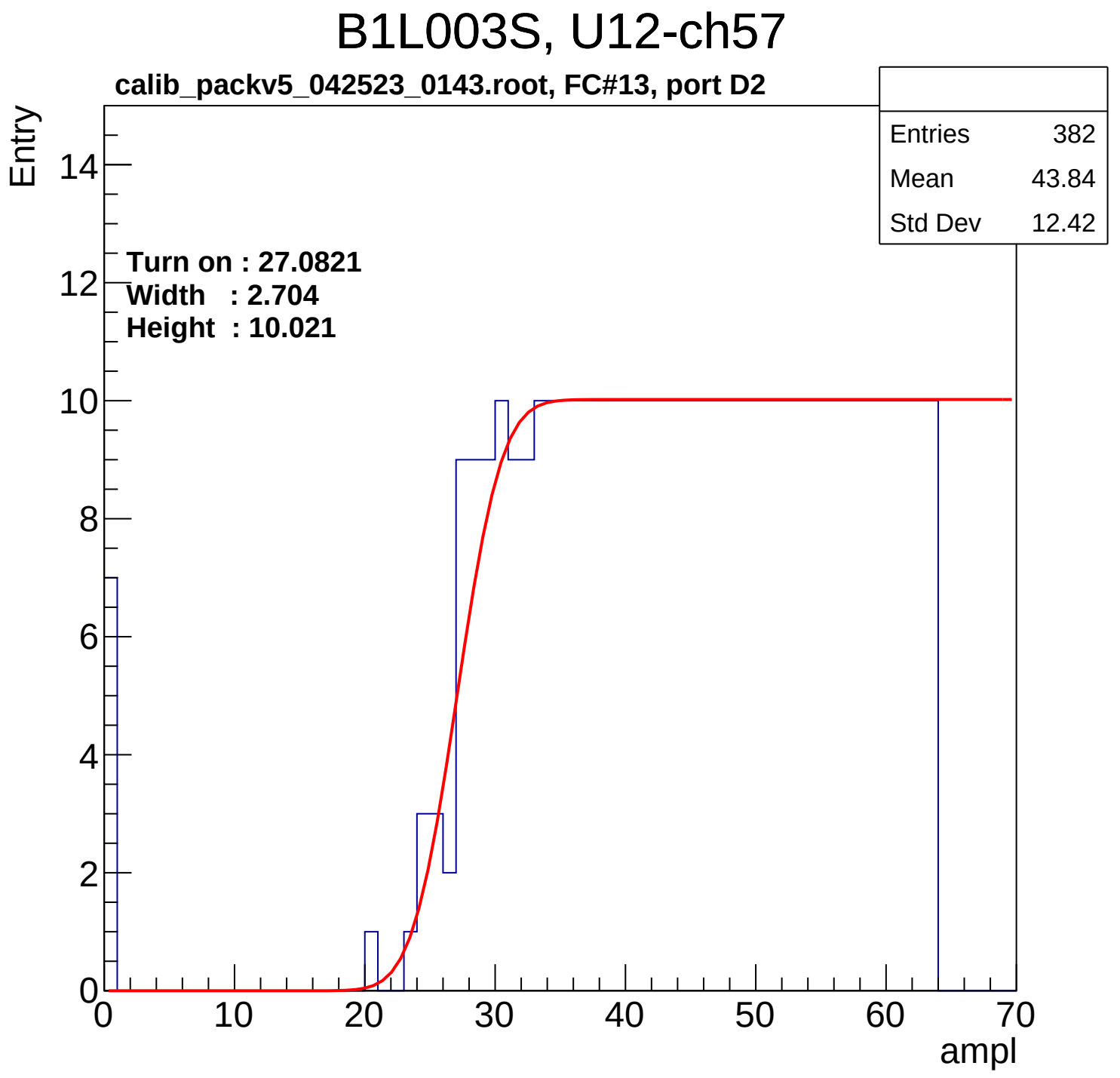

B1L003S, U12-ch52
calib_packv5_042523_0143.root, FC#13, port D2
Entries 370
Mean 44.58
Std Dev 11.78
Turn on : 27.4982
Width : 2.413
Height : 10.023
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

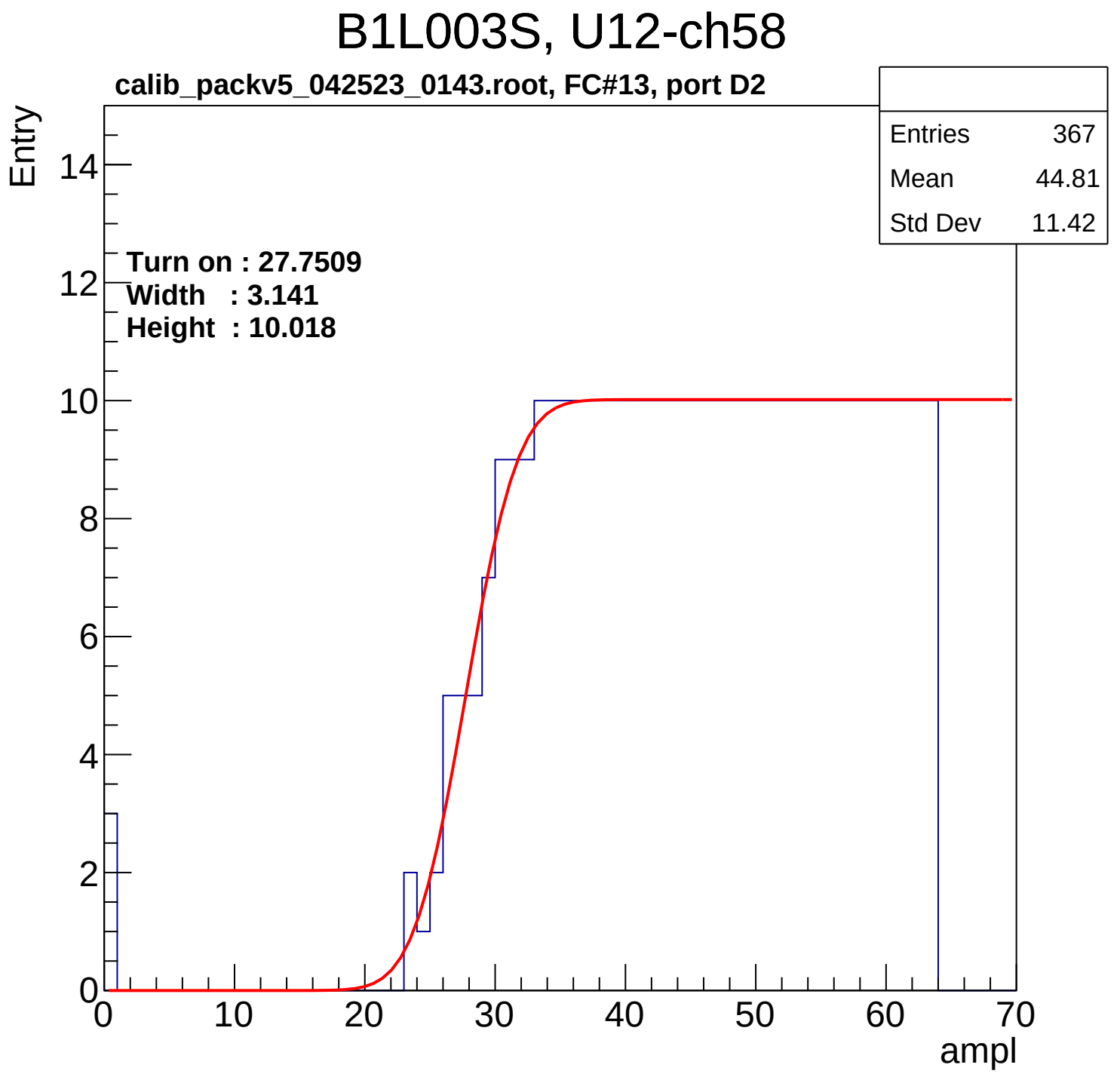

B1L003S, U12-ch53
calib_packv5_042523_0143.root, FC#13, port D2
Entries 346
Mean 45.9
Std Dev 10.72
Turn on : 30.1814
Width : 2.949
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

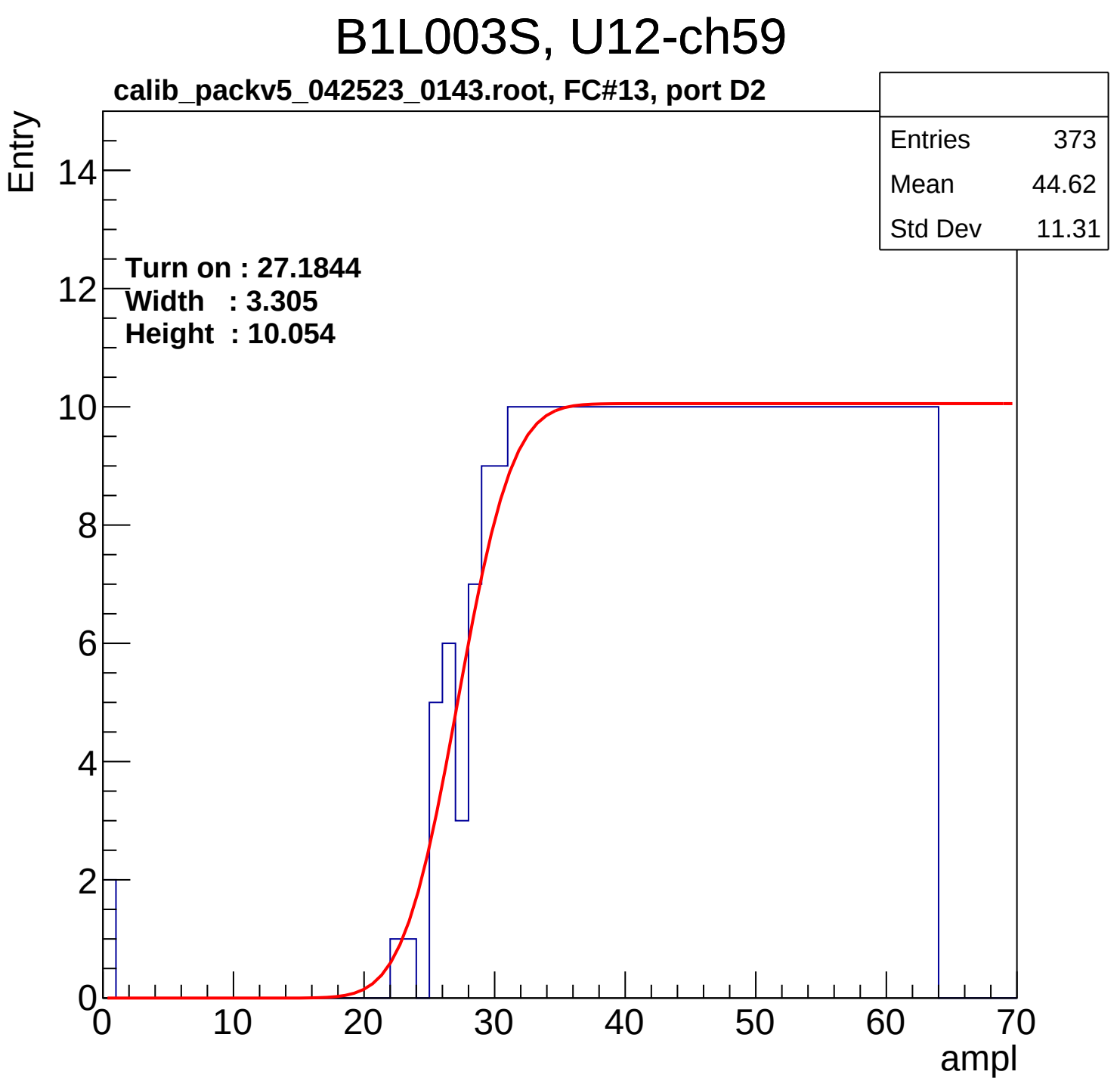

B1L003S, U12-ch54
calib_packv5_042523_0143.root, FC#13, port D2
Entries 385
Mean 43.93
Std Dev 11.85
Turn on : 25.8167
Width : 3.147
Height : 9.982
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

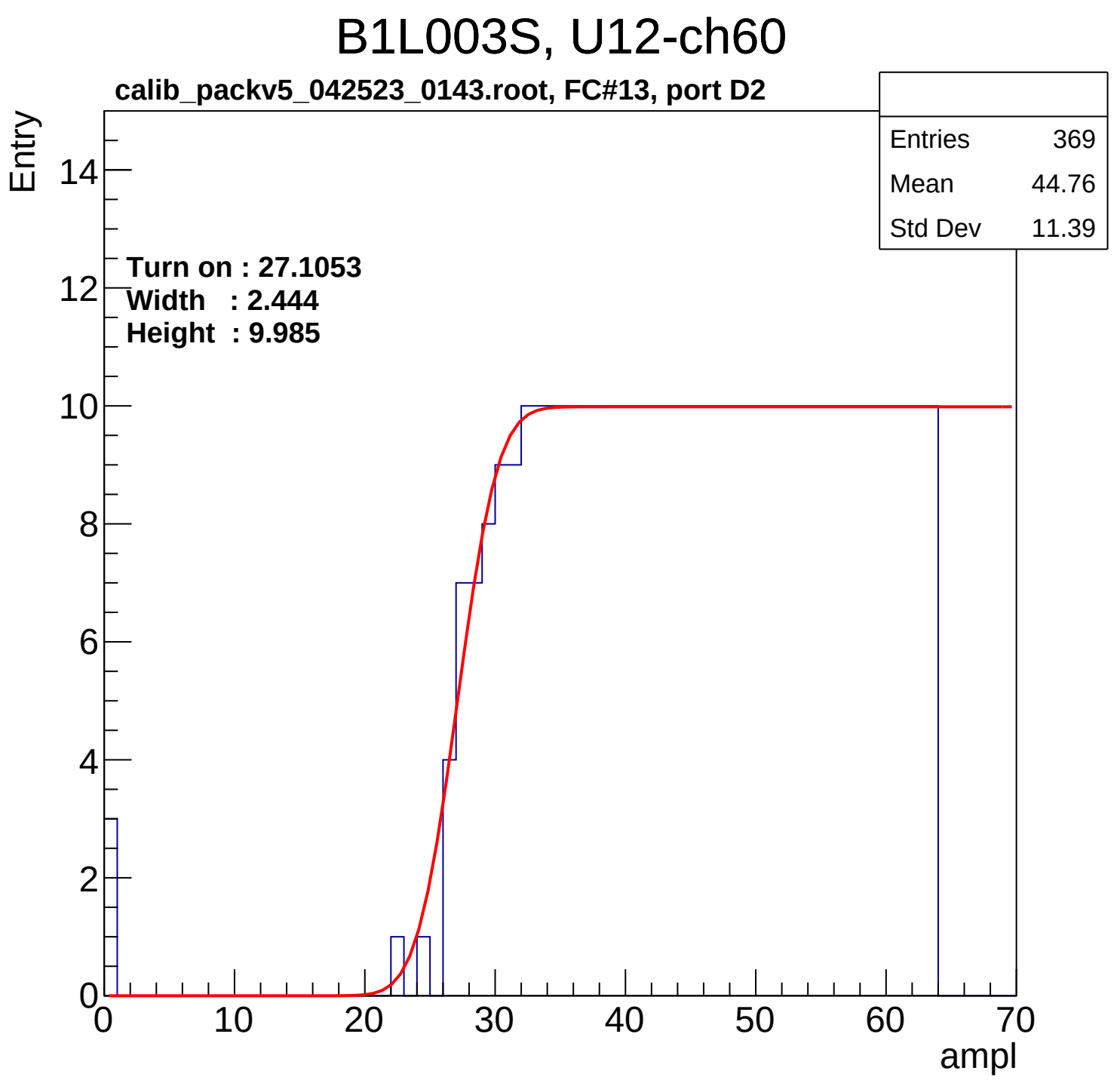

B1L003S, U12-ch55
calib_packv5_042523_0143.root, FC#13, port D2
Entries 380
Mean 44.27
Std Dev 11.5
Turn on : 26.3153
Width : 3.076
Height : 10.029
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

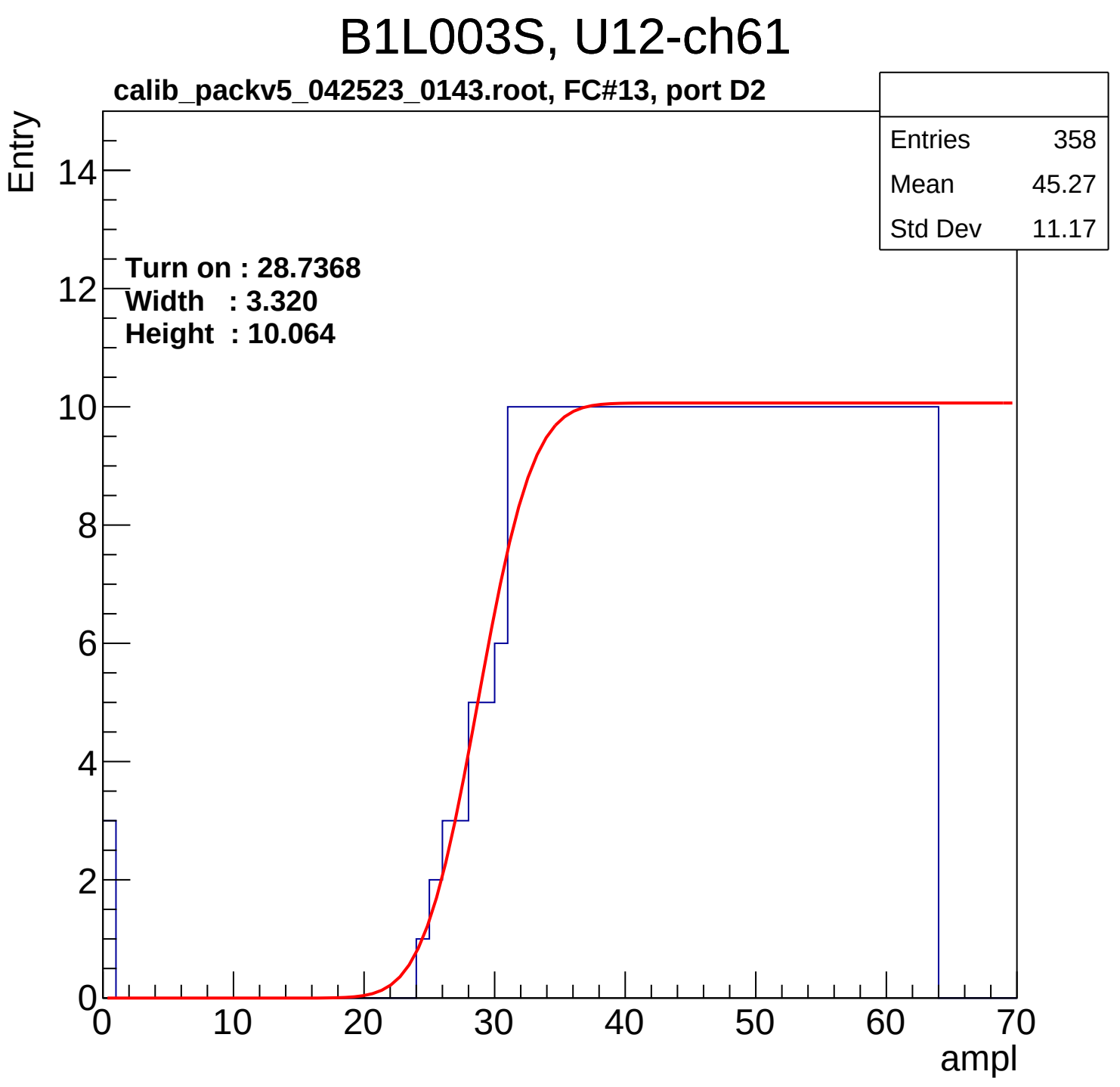

B1L003S, U12-ch56
calib_packv5_042523_0143.root, FC#13, port D2
Entries 378
Mean 44.34
Std Dev 11.58
Turn on : 26.9685
Width : 1.078
Height : 10.019
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

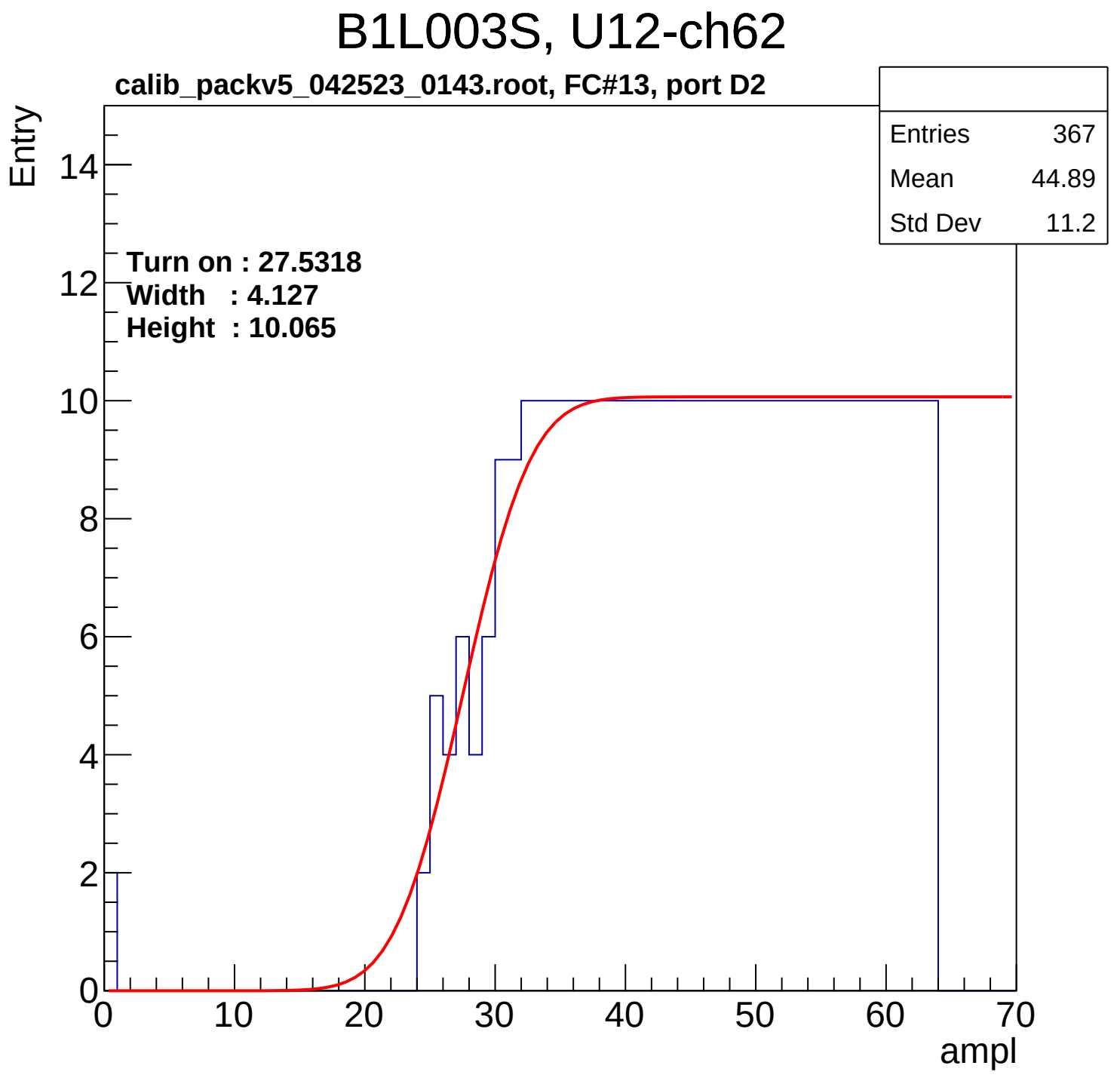

B1L003S, U12-ch57
calib_packv5_042523_0143.root, FC#13, port D2
Entries 382
Mean 43.84
Std Dev 12.42
Turn on : 27.0821
Width : 2.704
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

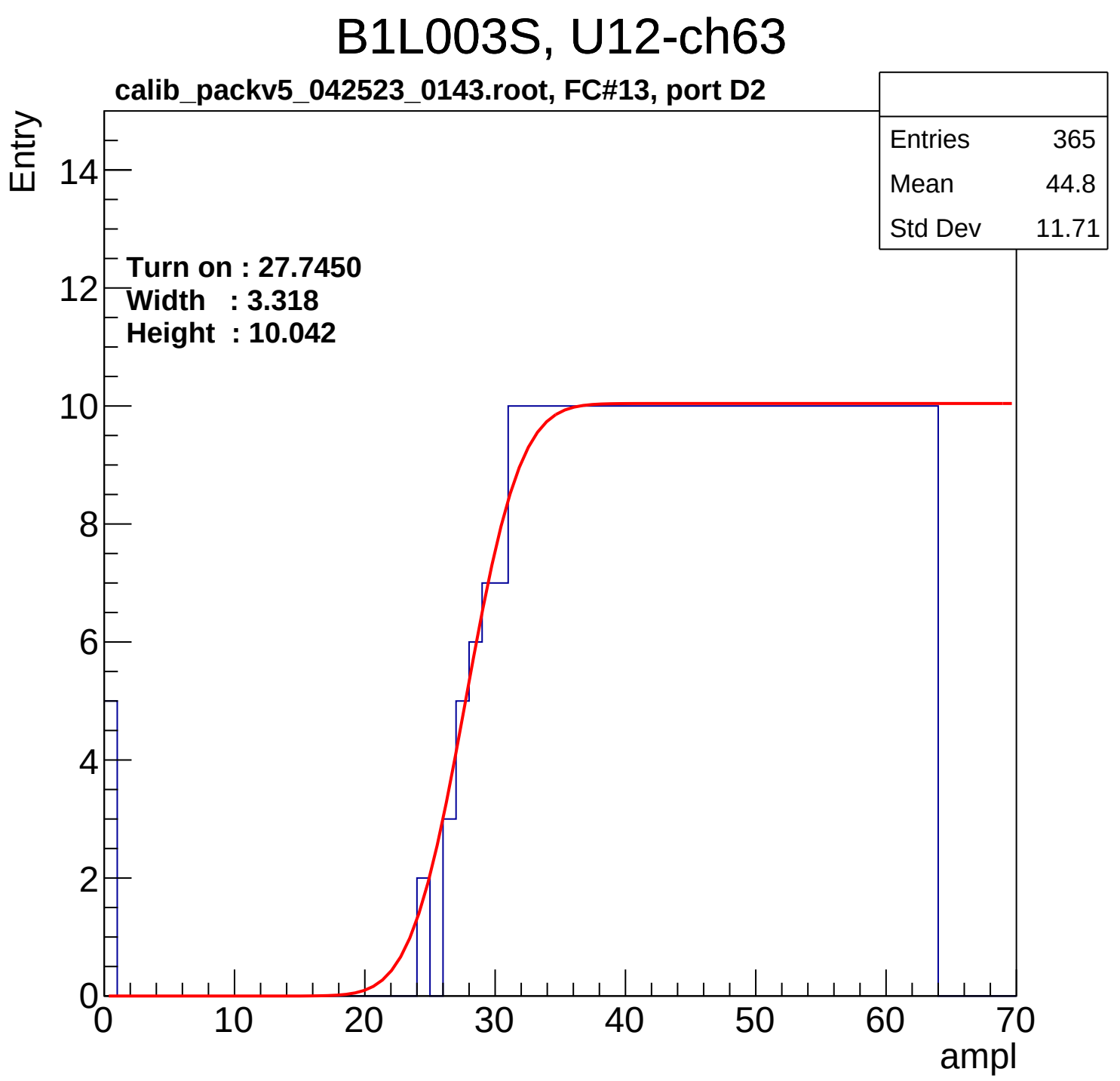

B1L003S, U12-ch58
calib_packv5_042523_0143.root, FC#13, port D2
Entries 367
Mean 44.81
Std Dev 11.42
Turn on : 27.7509
Width : 3.141
Height : 10.018
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

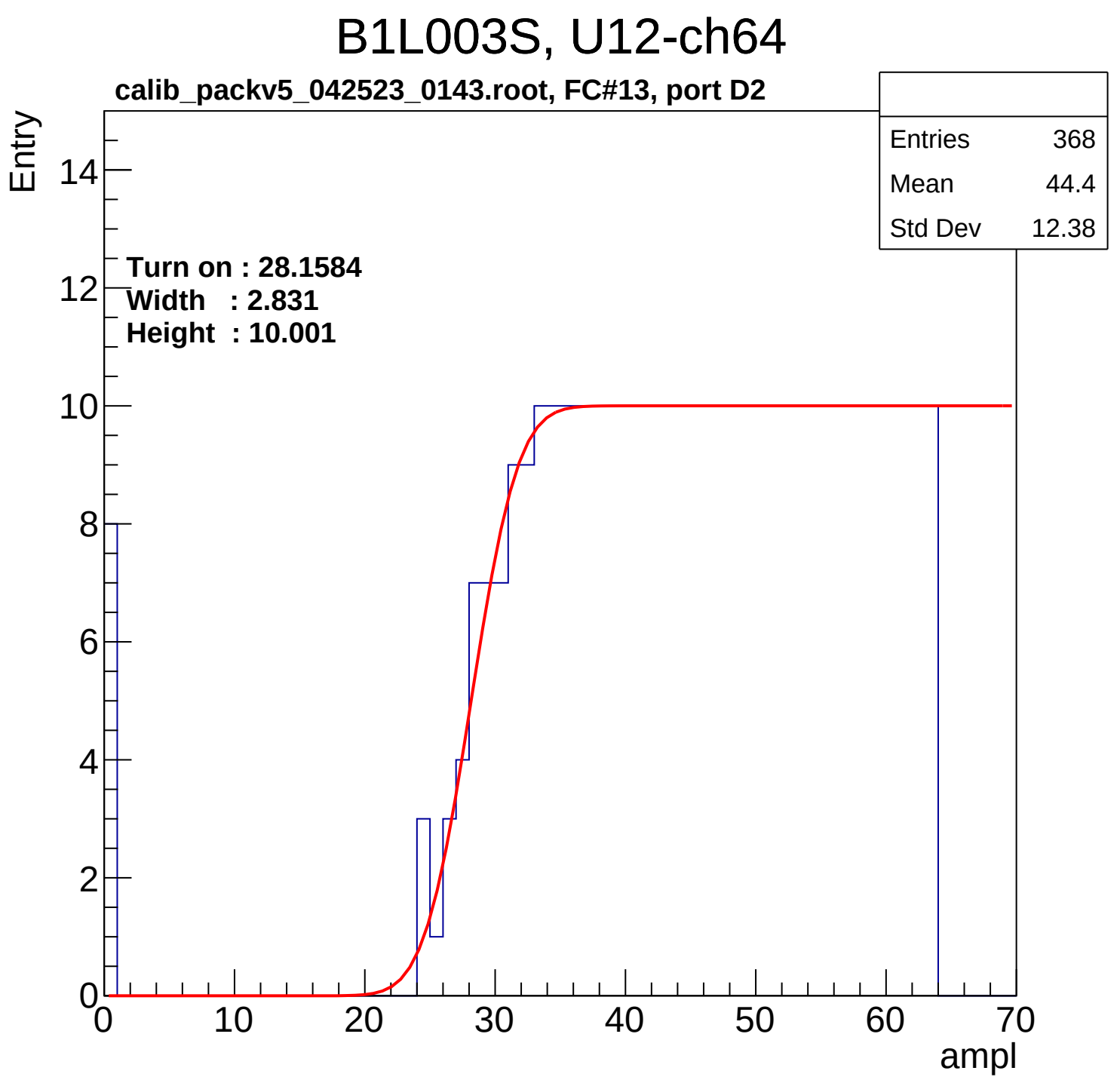

B1L003S, U12-ch59
calib_packv5_042523_0143.root, FC#13, port D2
Entries 373
Mean 44.62
Std Dev 11.31
Turn on : 27.1844
Width : 3.305
Height : 10.054
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

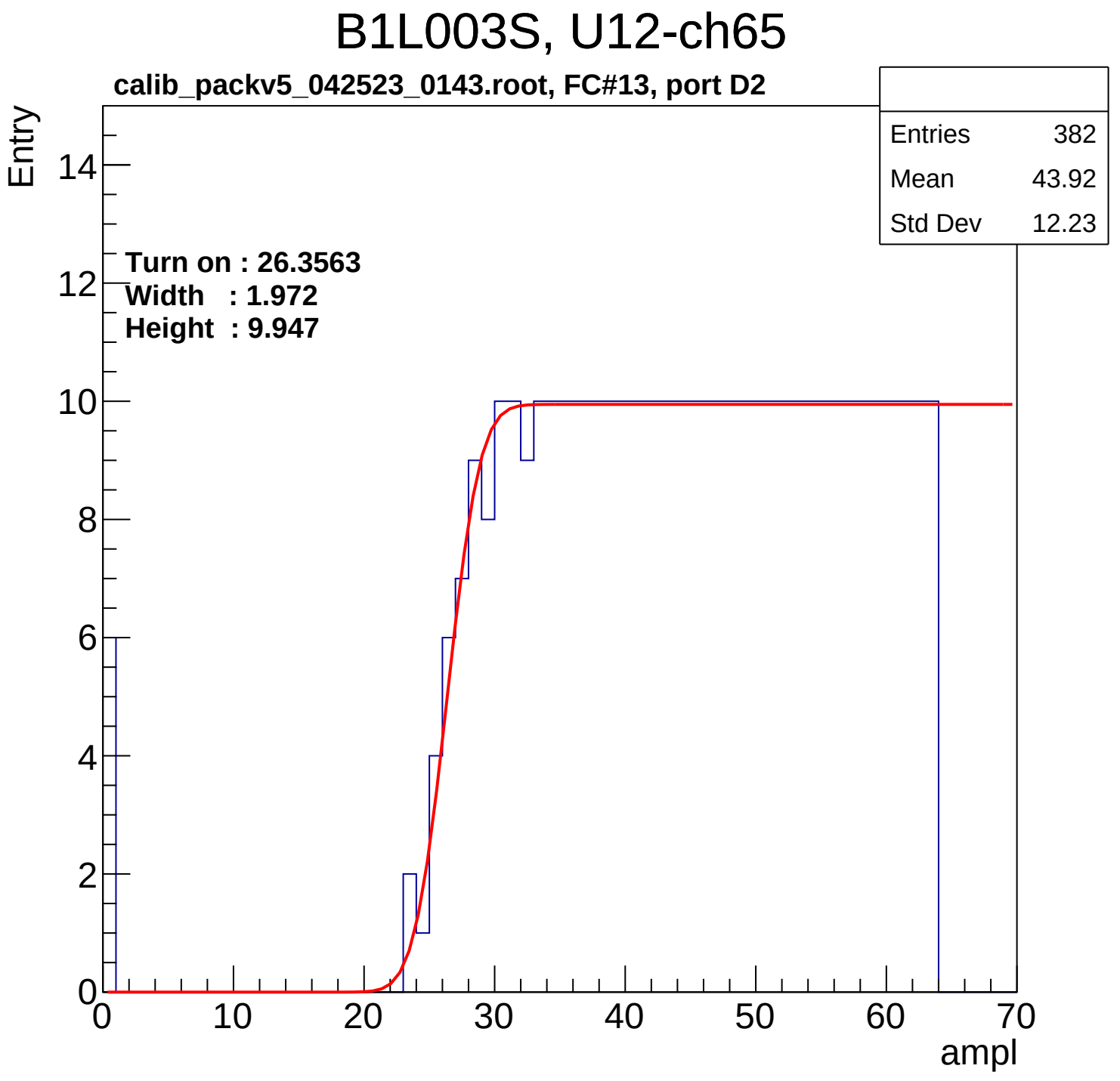

B1L003S, U12-ch60
calib_packv5_042523_0143.root, FC#13, port D2
Entries 369
Mean 44.76
Std Dev 11.39
Turn on : 27.1053
Width : 2.444
Height : 9.985
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

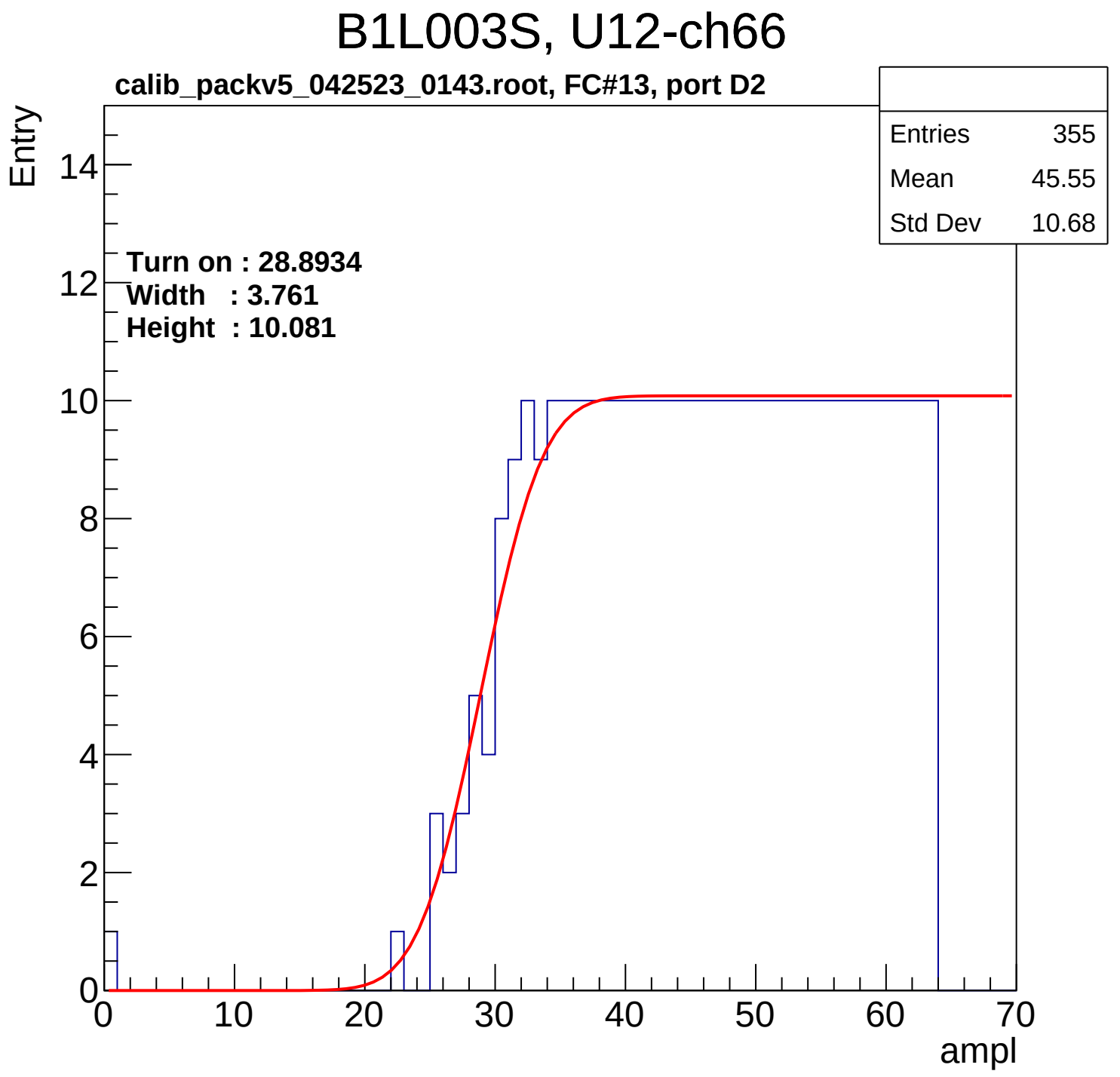

B1L003S, U12-ch61
calib_packv5_042523_0143.root, FC#13, port D2
Entries 358
Mean 45.27
Std Dev 11.17
Turn on : 28.7368
Width : 3.320
Height : 10.064
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

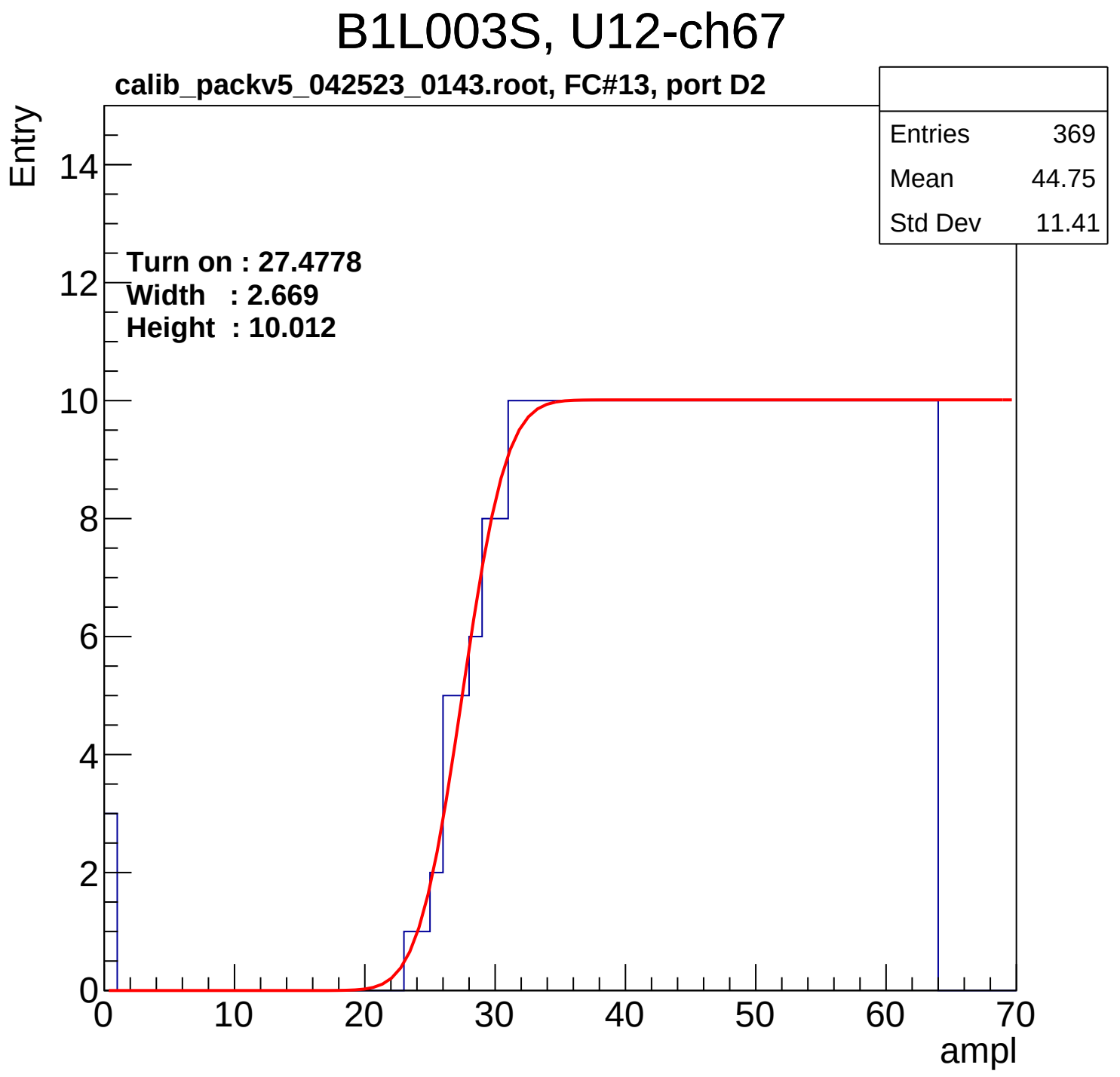

B1L003S, U12-ch62
calib_packv5_042523_0143.root, FC#13, port D2
Entries 367
Mean 44.89
Std Dev 11.2
Turn on : 27.5318
Width : 4.127
Height : 10.065
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

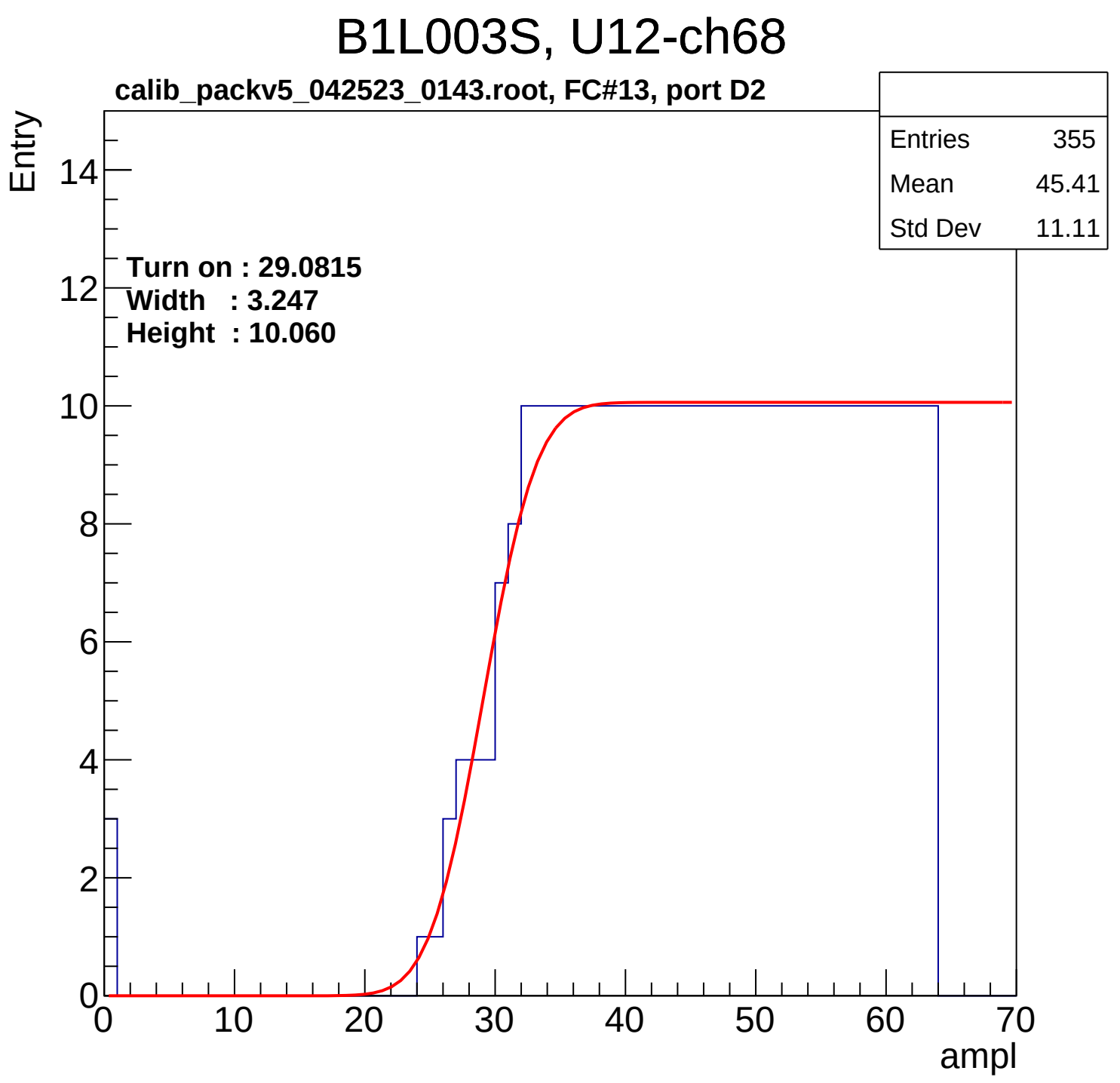

B1L003S, U12-ch63
calib_packv5_042523_0143.root, FC#13, port D2
Entries 365
Mean 44.8
Std Dev 11.71
Turn on : 27.7450
Width : 3.318
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

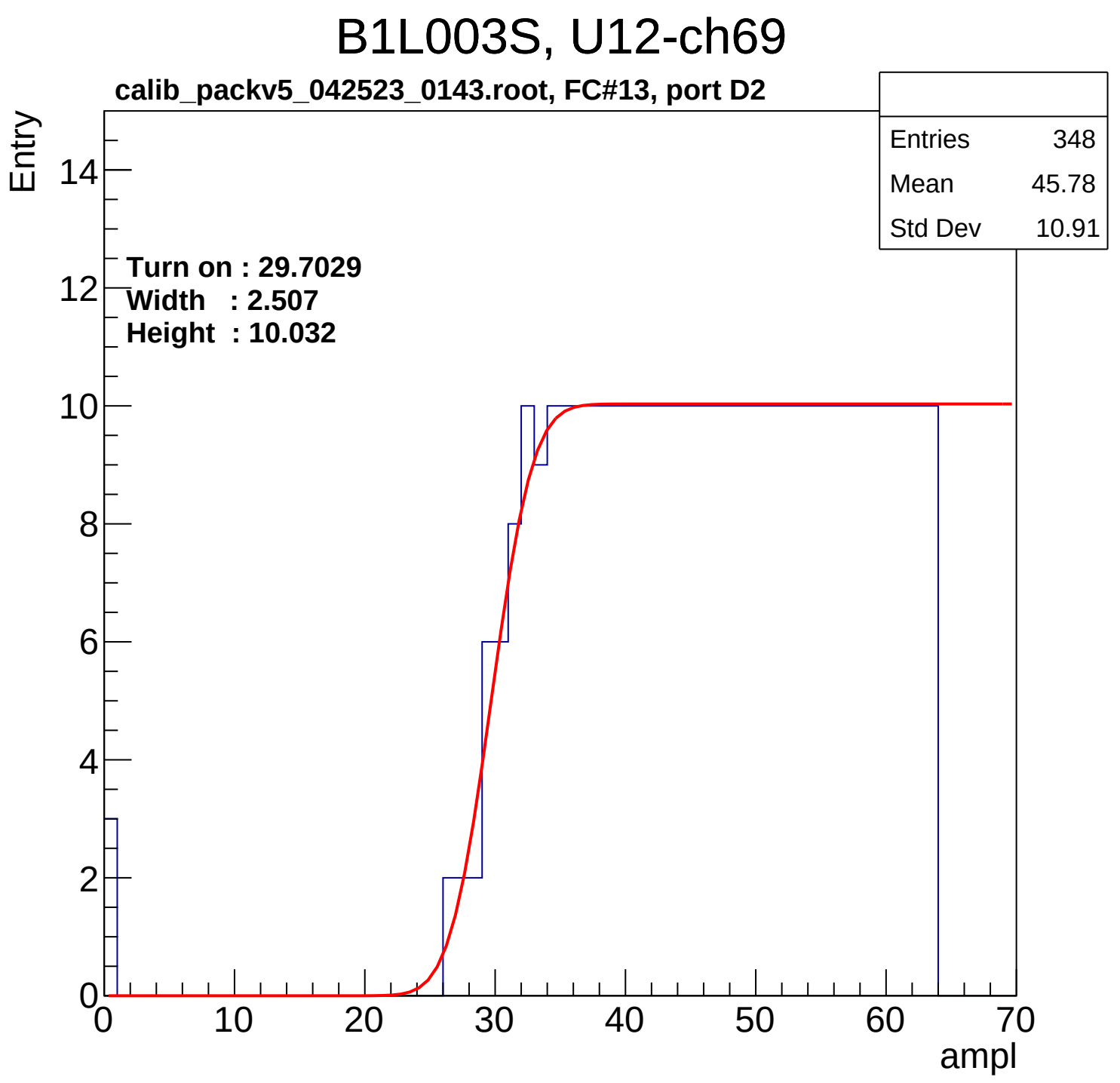

B1L003S, U12-ch64
calib_packv5_042523_0143.root, FC#13, port D2
Entries 368
Mean 44.4
Std Dev 12.38
Turn on : 28.1584
Width : 2.831
Height : 10.001
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

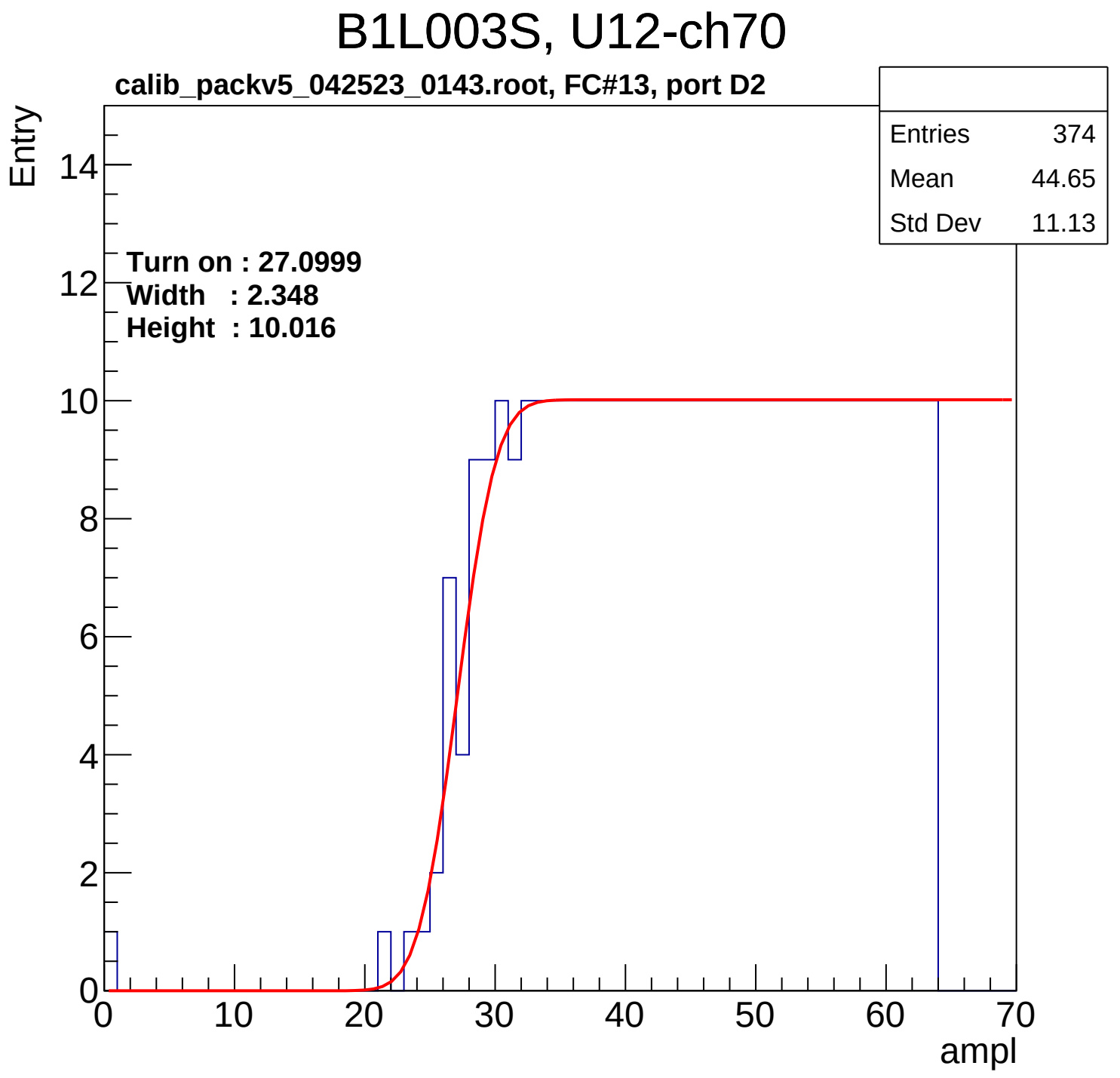

B1L003S, U12-ch65
calib_packv5_042523_0143.root, FC#13, port D2
Entries 382
Mean 43.92
Std Dev 12.23
Turn on : 26.3563
Width : 1.972
Height : 9.947
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

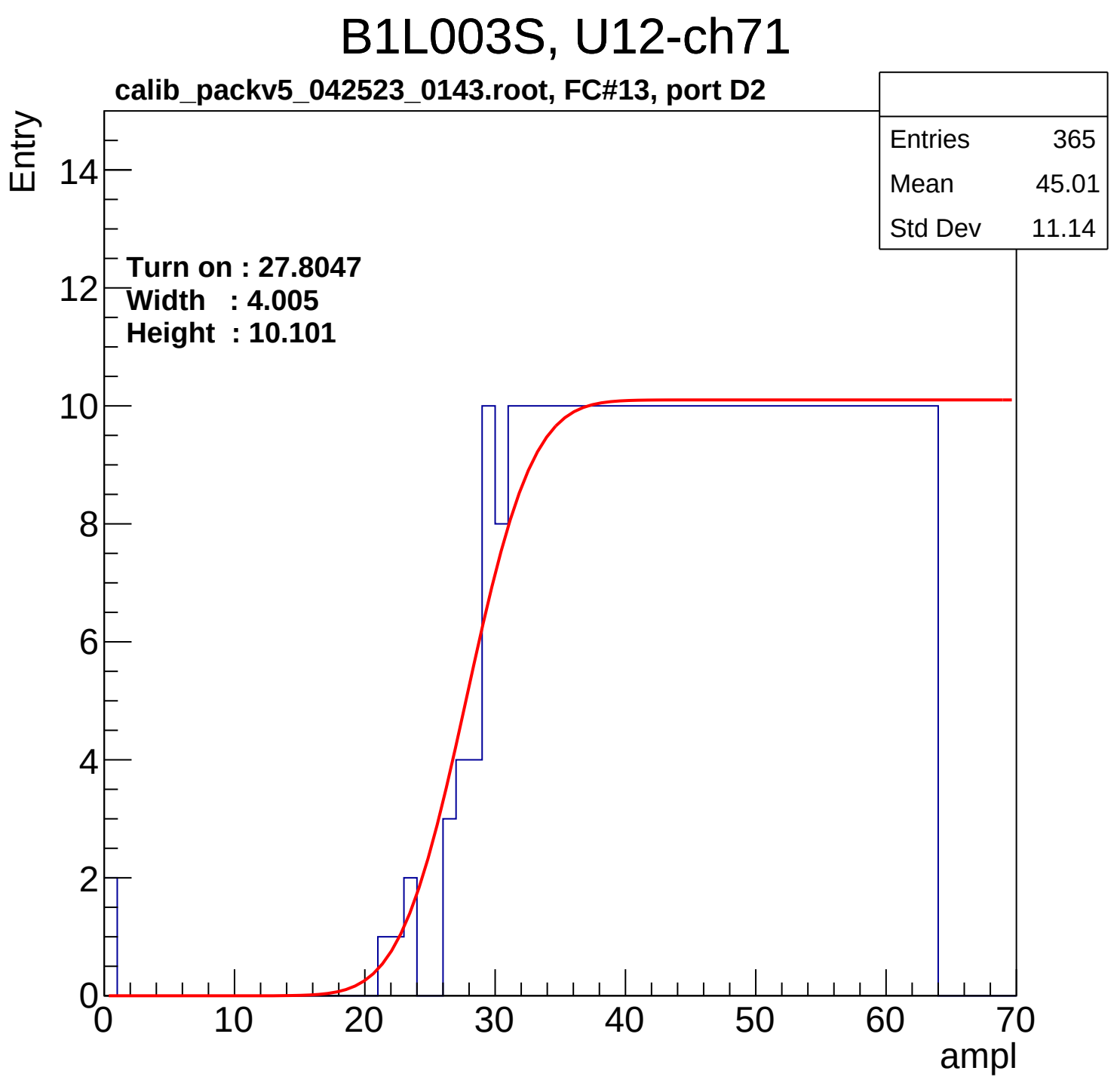

B1L003S, U12-ch66
calib_packv5_042523_0143.root, FC#13, port D2
Entries 355
Mean 45.55
Std Dev 10.68
Turn on : 28.8934
Width : 3.761
Height : 10.081
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

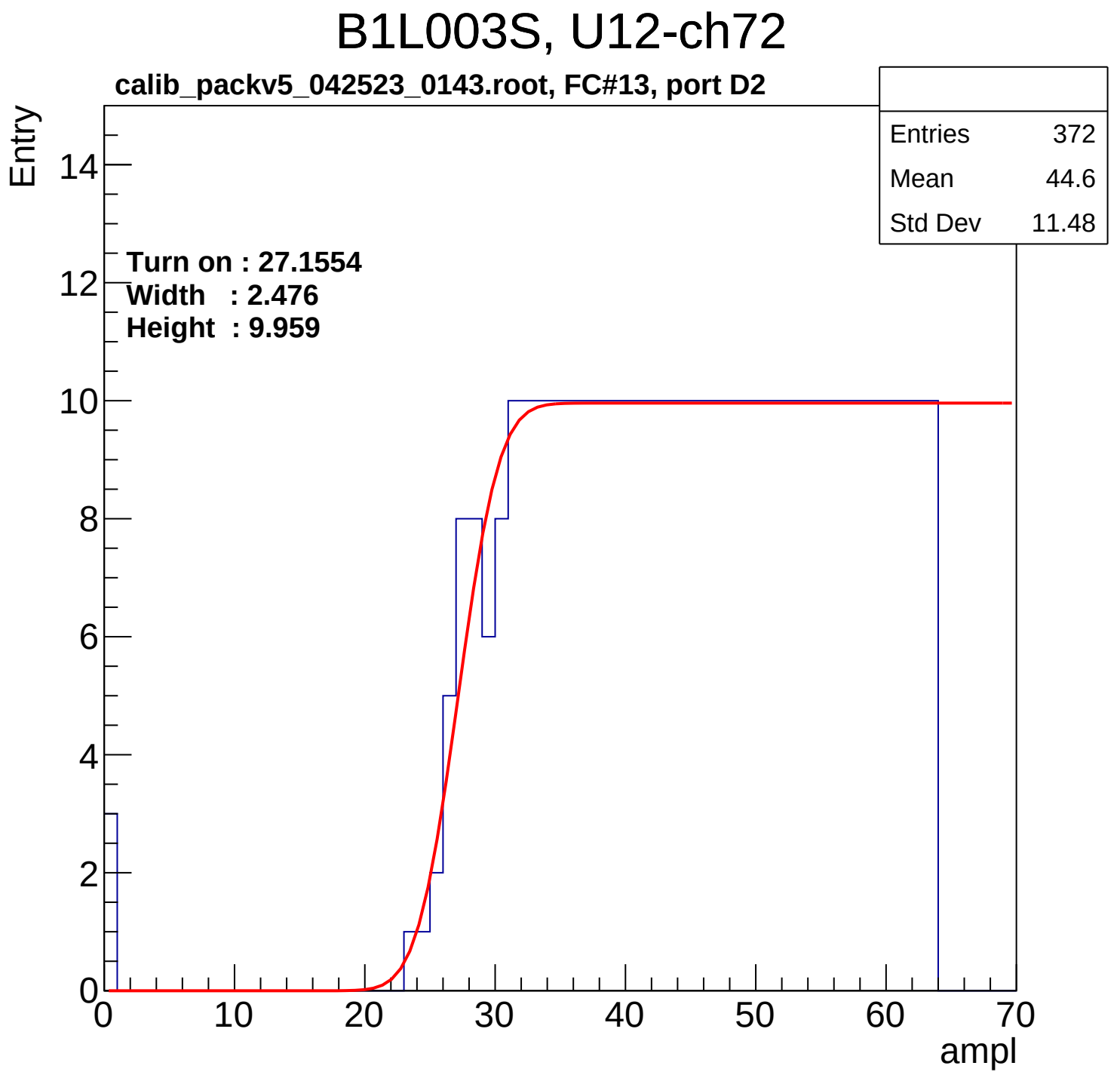

B1L003S, U12-ch67
calib_packv5_042523_0143.root, FC#13, port D2
Entries 369
Mean 44.75
Std Dev 11.41
Turn on : 27.4778
Width : 2.669
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

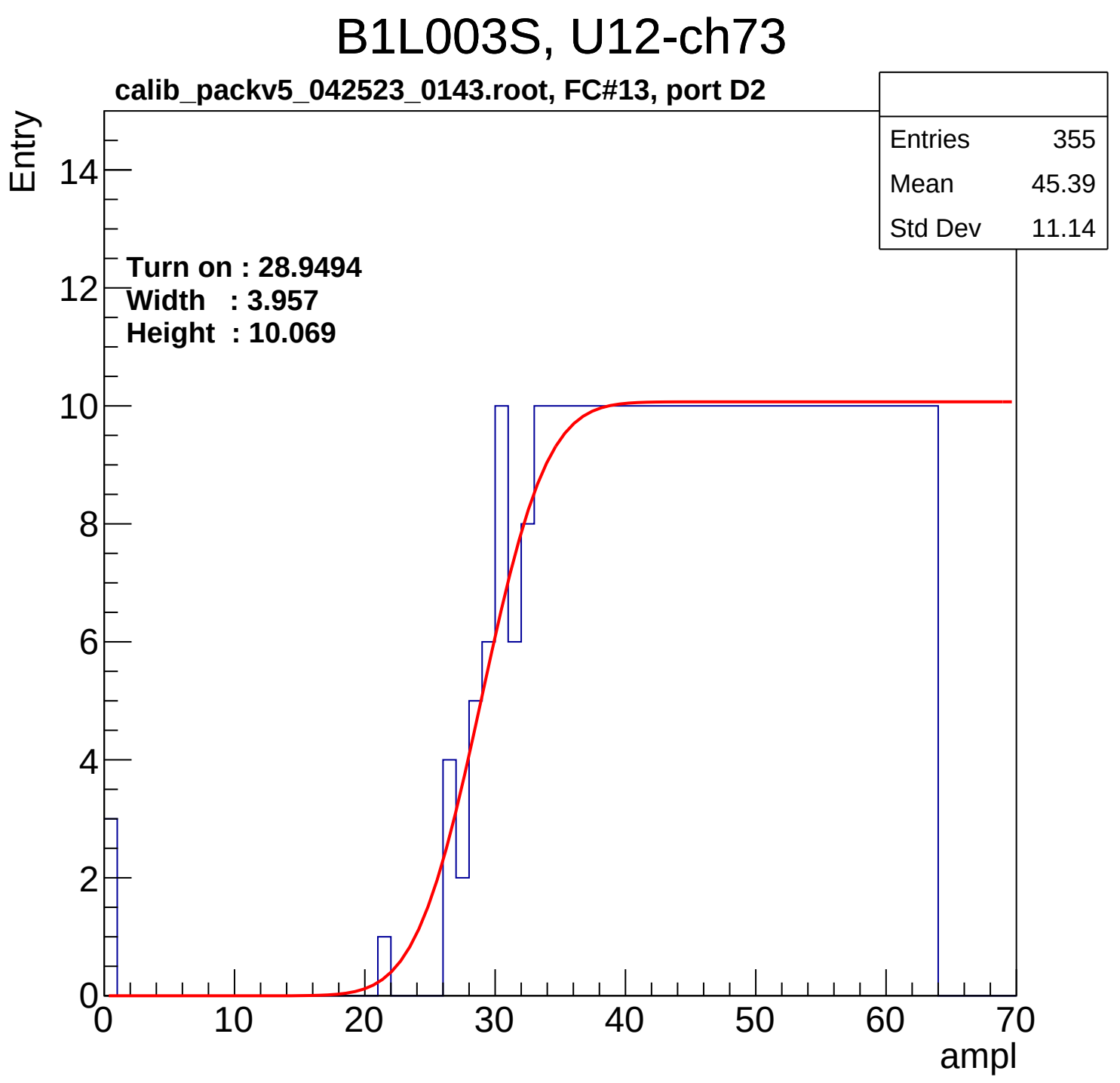

B1L003S, U12-ch68
calib_packv5_042523_0143.root, FC#13, port D2
Entries 355
Mean 45.41
Std Dev 11.11
Turn on : 29.0815
Width : 3.247
Height : 10.060
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

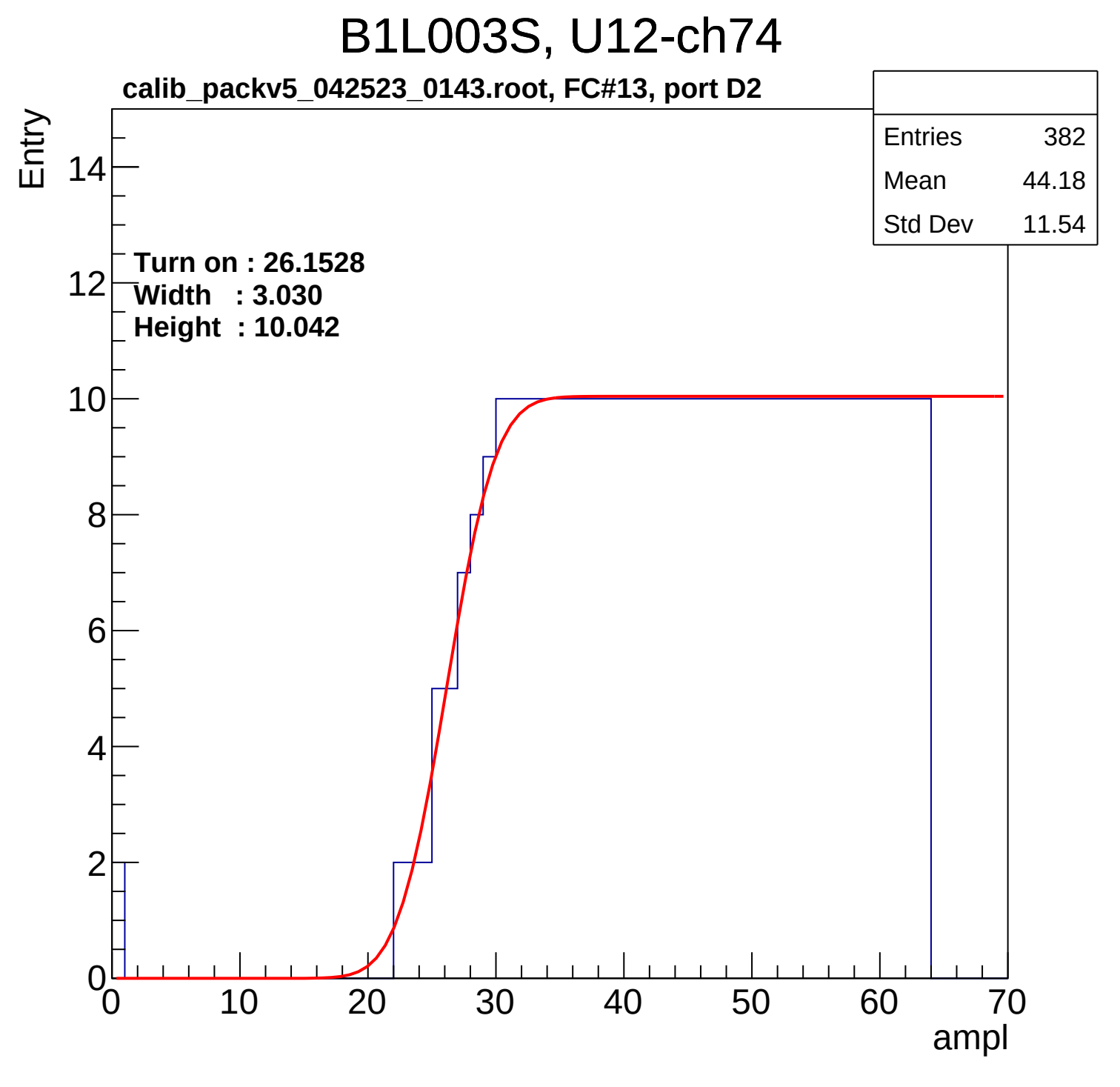

B1L003S, U12-ch69
calib_packv5_042523_0143.root, FC#13, port D2
Entries 348
Mean 45.78
Std Dev 10.91
Turn on : 29.7029
Width : 2.507
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

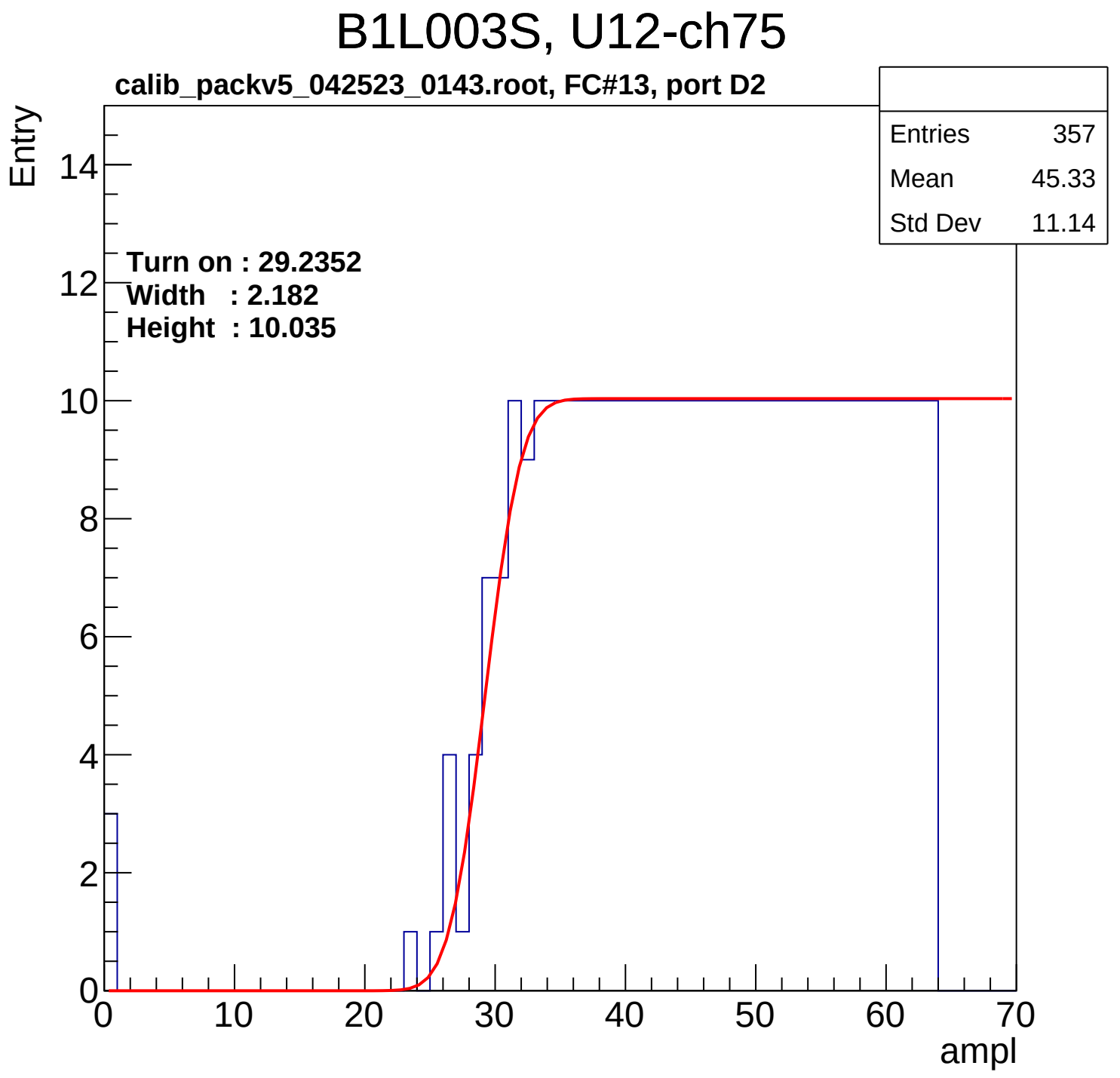

B1L003S, U12-ch70
calib_packv5_042523_0143.root, FC#13, port D2
Entries 374
Mean 44.65
Std Dev 11.13
Turn on : 27.0999
Width : 2.348
Height : 10.016
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

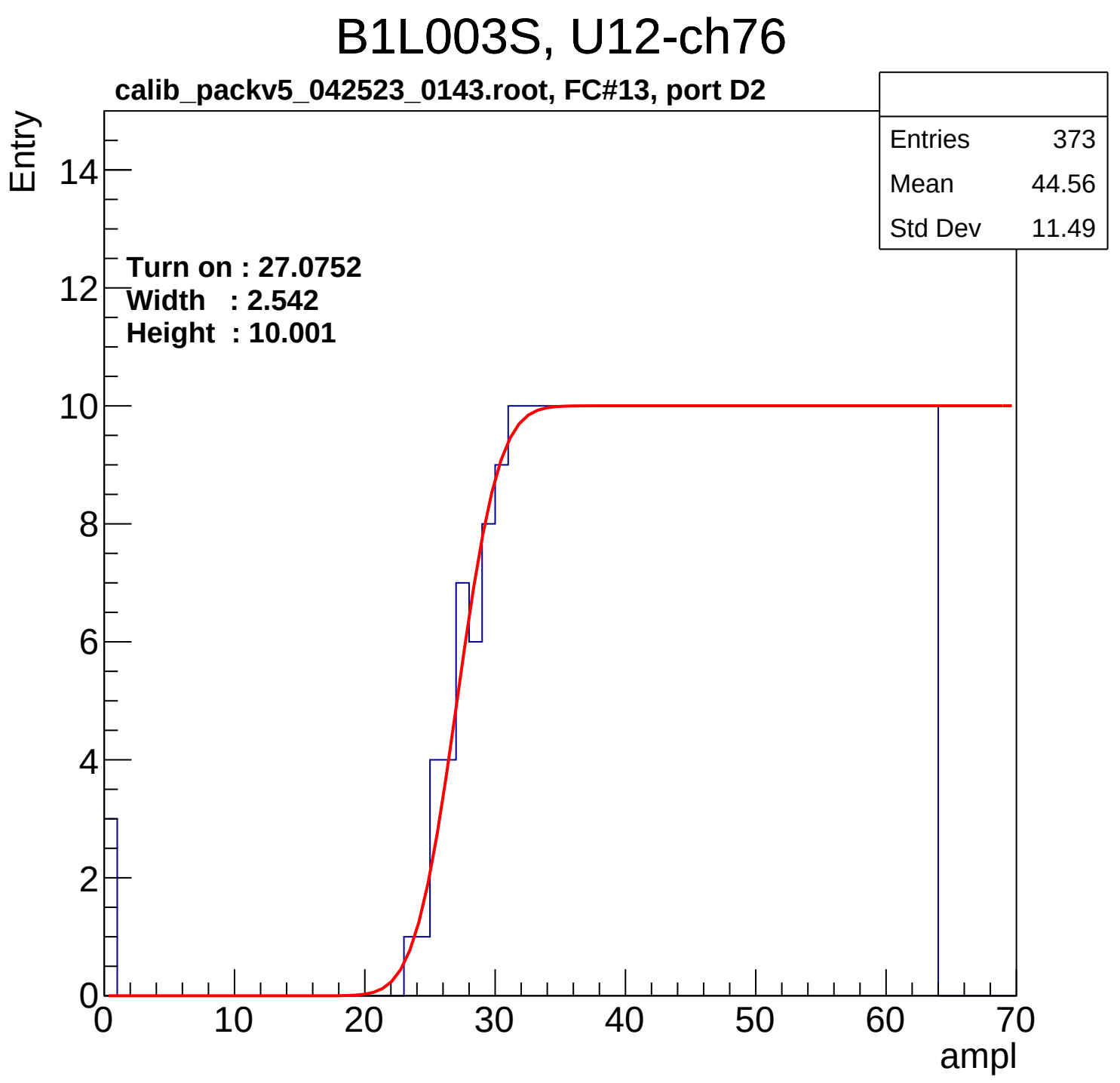

B1L003S, U12-ch71
calib_packv5_042523_0143.root, FC#13, port D2
Entries 365
Mean 45.01
Std Dev 11.14
Turn on : 27.8047
Width : 4.005
Height : 10.101
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

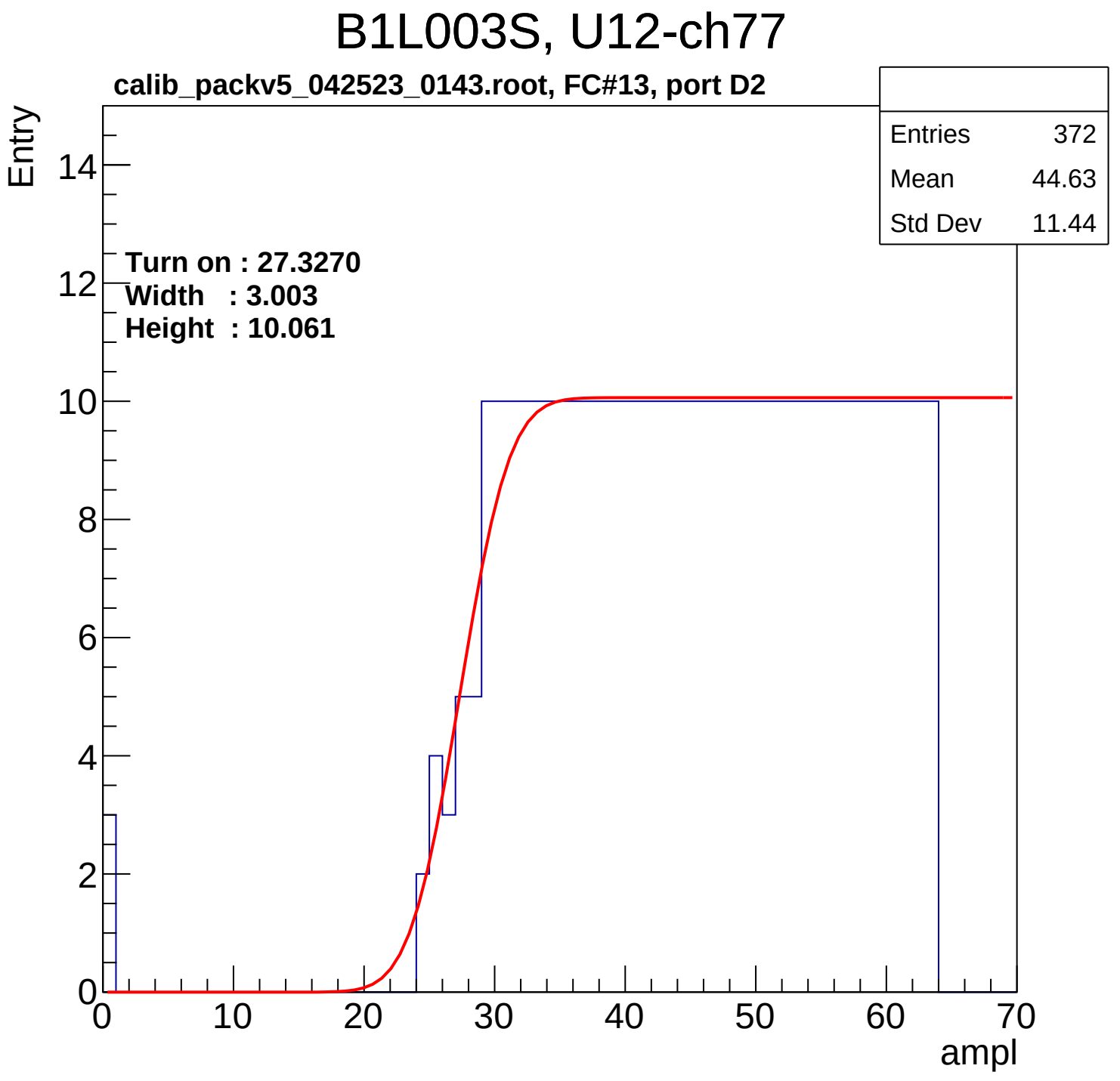

B1L003S, U12-ch72
calib_packv5_042523_0143.root, FC#13, port D2
Entries 372
Mean 44.6
Std Dev 11.48
Turn on : 27.1554
Width : 2.476
Height : 9.959
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

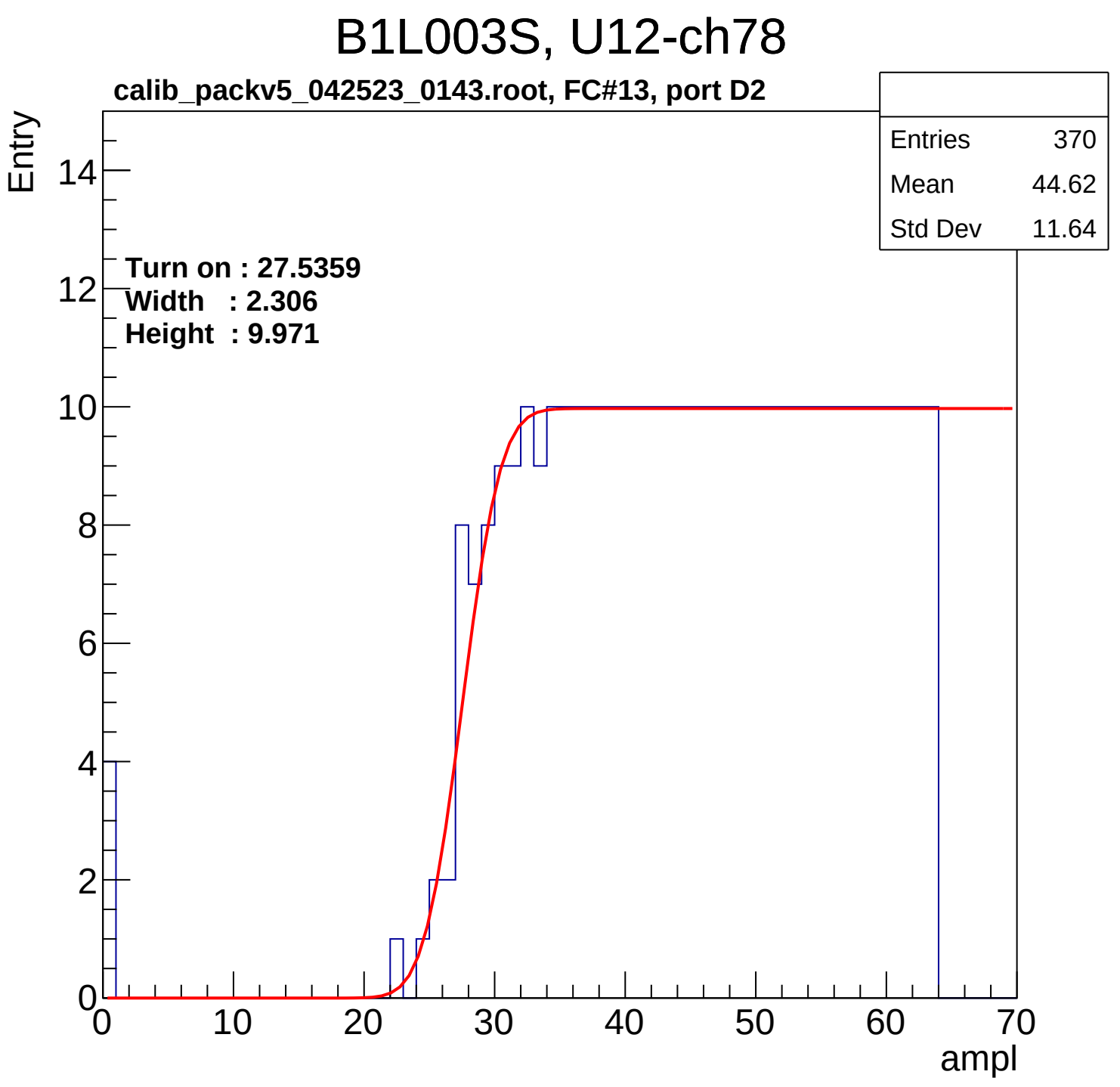

B1L003S, U12-ch73
calib_packv5_042523_0143.root, FC#13, port D2
Entries 355
Mean 45.39
Std Dev 11.14
Turn on : 28.9494
Width : 3.957
Height : 10.069
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

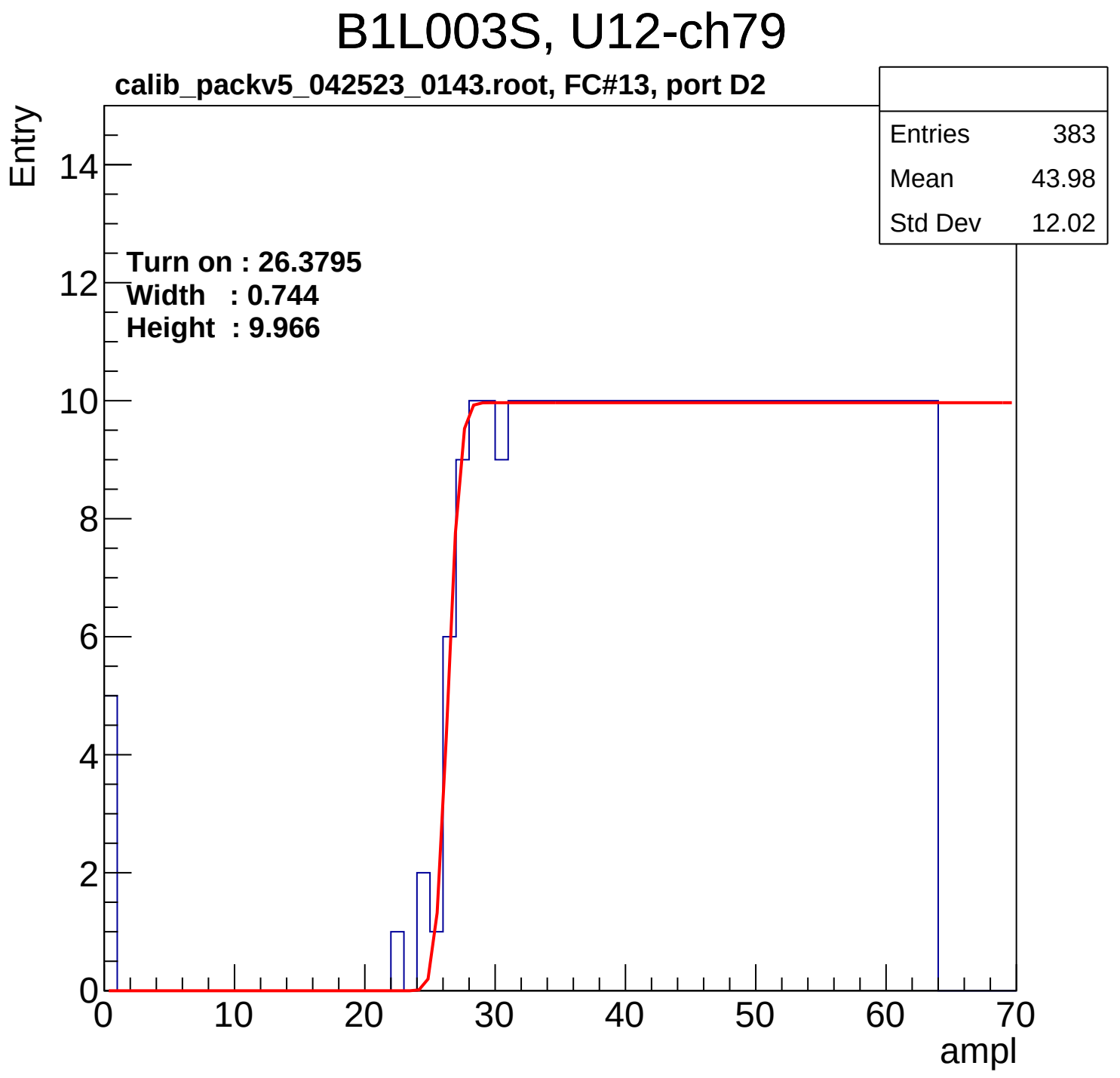

B1L003S, U12-ch74
calib_packv5_042523_0143.root, FC#13, port D2
Entries 382
Mean 44.18
Std Dev 11.54
Turn on : 26.1528
Width : 3.030
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

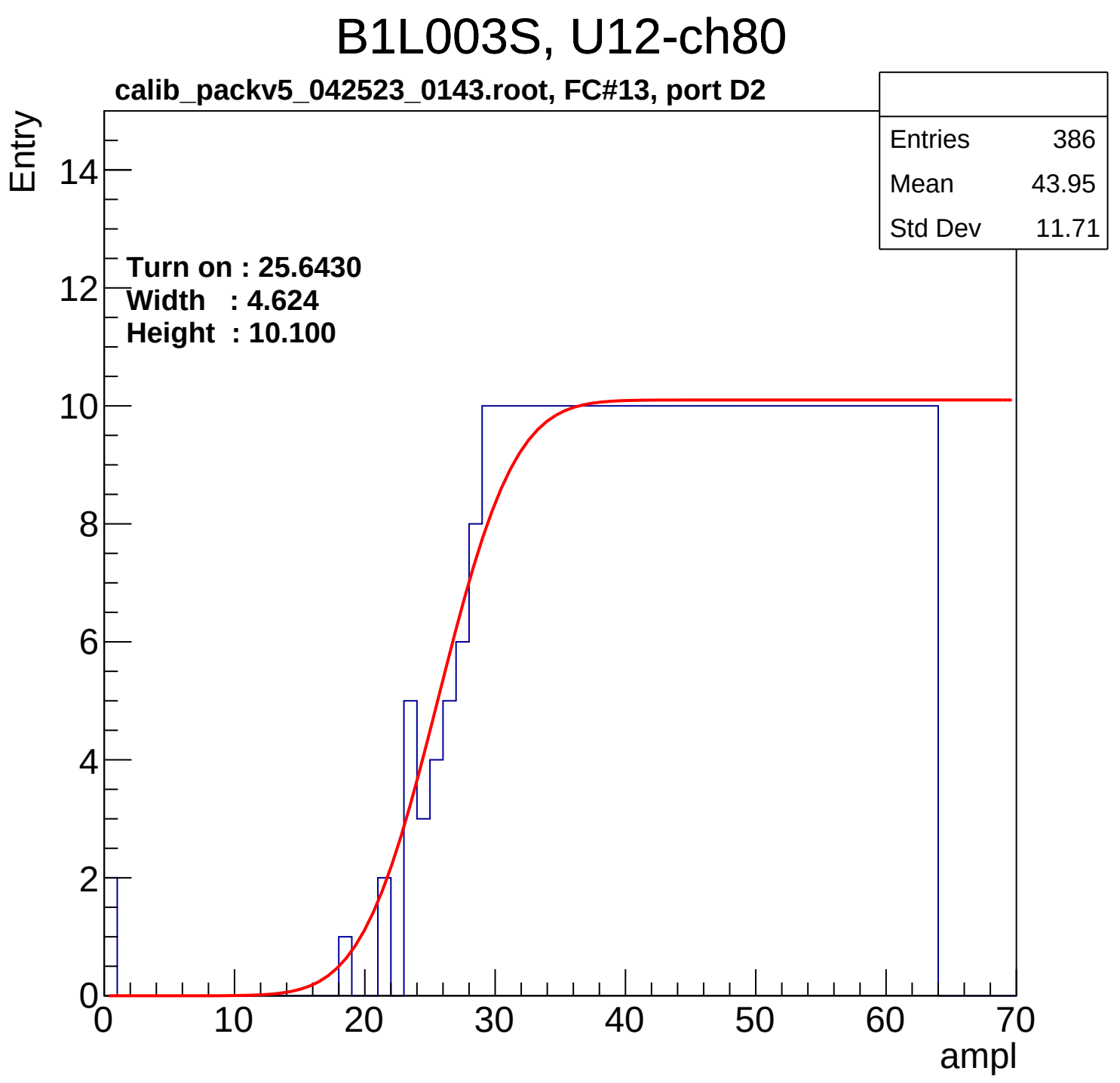

B1L003S, U12-ch75
calib_packv5_042523_0143.root, FC#13, port D2
Entries 357
Mean 45.33
Std Dev 11.14
Turn on : 29.2352
Width : 2.182
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

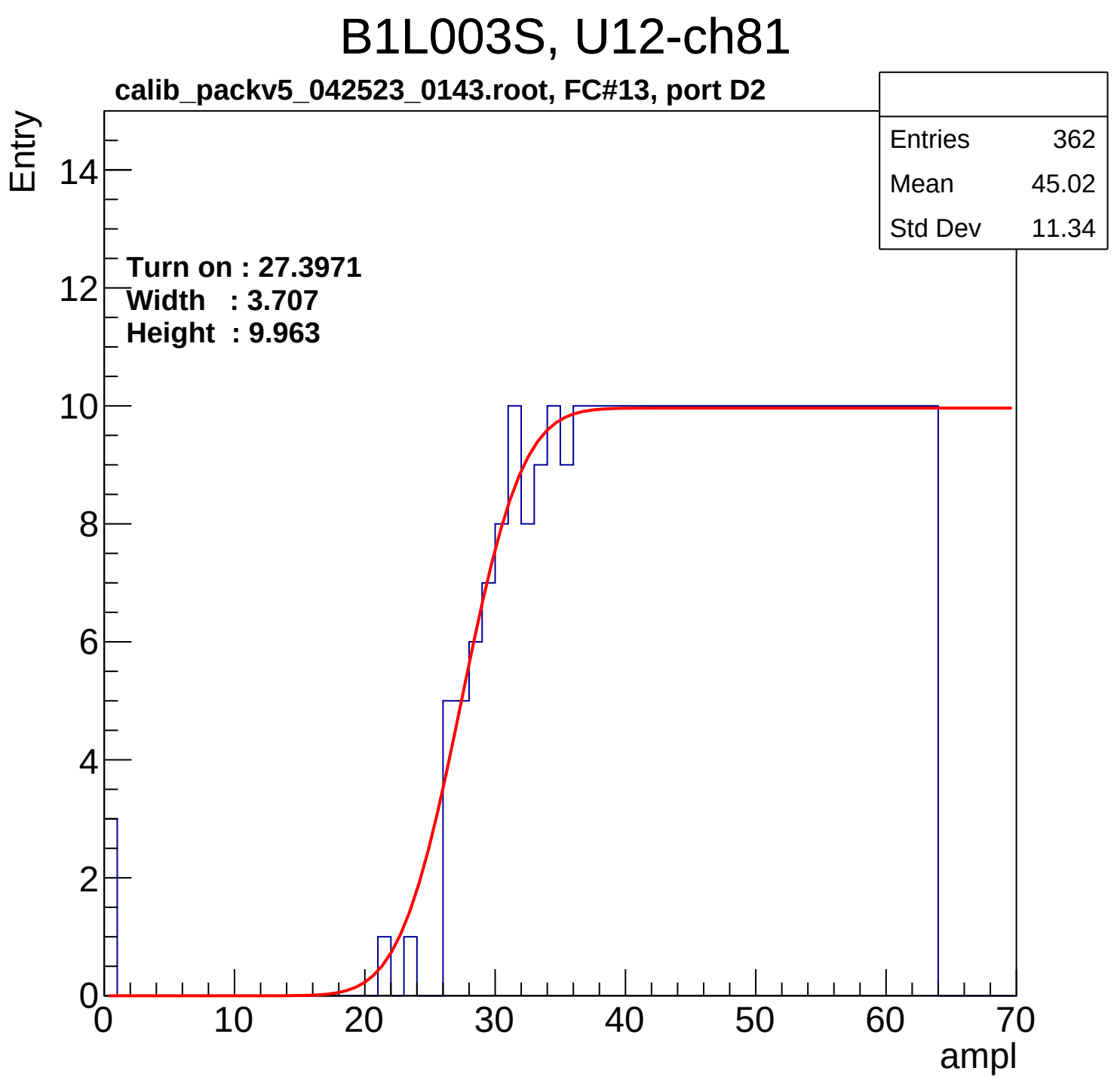

B1L003S, U12-ch76
calib_packv5_042523_0143.root, FC#13, port D2
Entries 373
Mean 44.56
Std Dev 11.49
Turn on : 27.0752
Width : 2.542
Height : 10.001
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

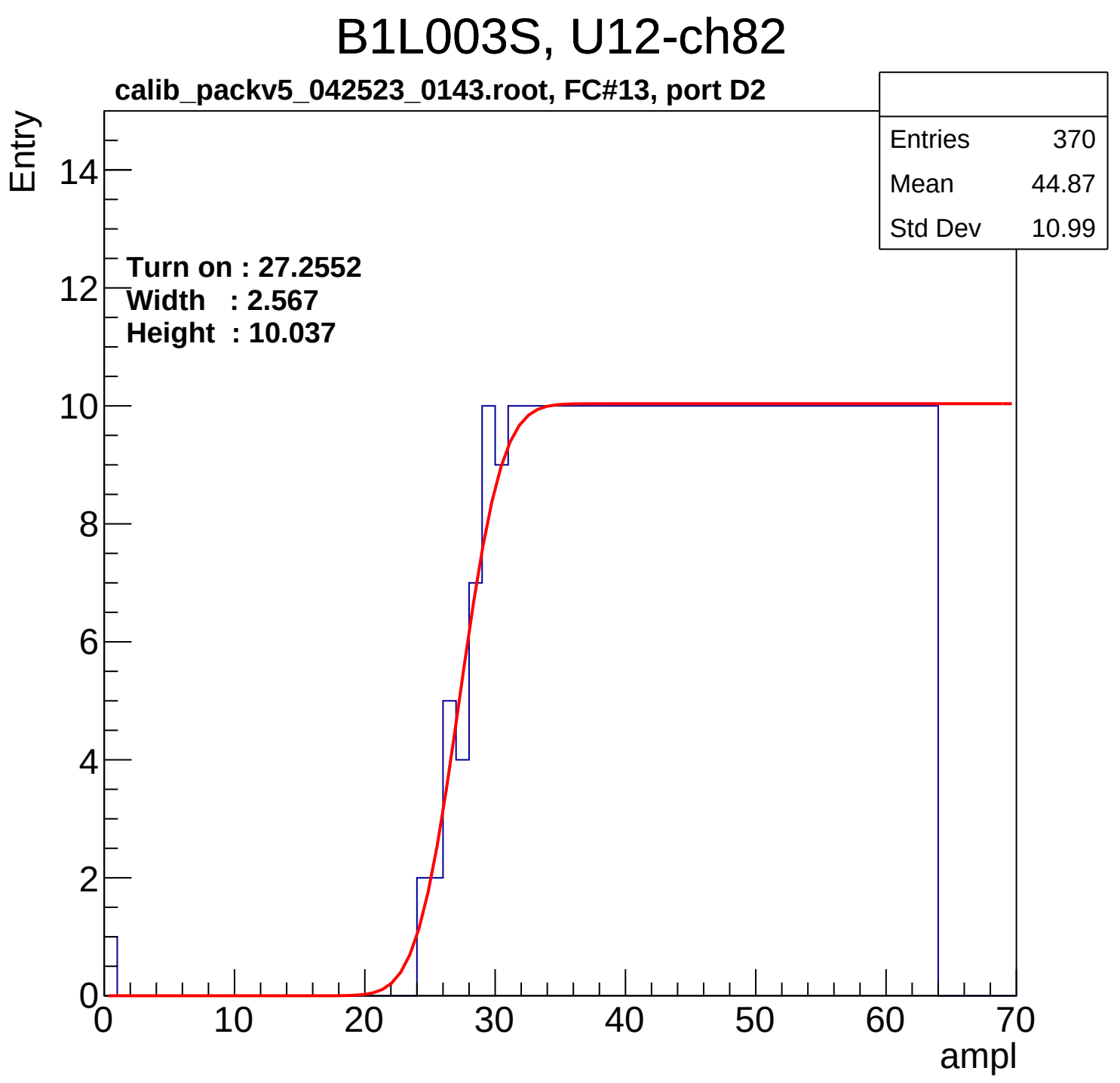

B1L003S, U12-ch77
calib_packv5_042523_0143.root, FC#13, port D2
Entries 372
Mean 44.63
Std Dev 11.44
Turn on : 27.3270
Width : 3.003
Height : 10.061
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

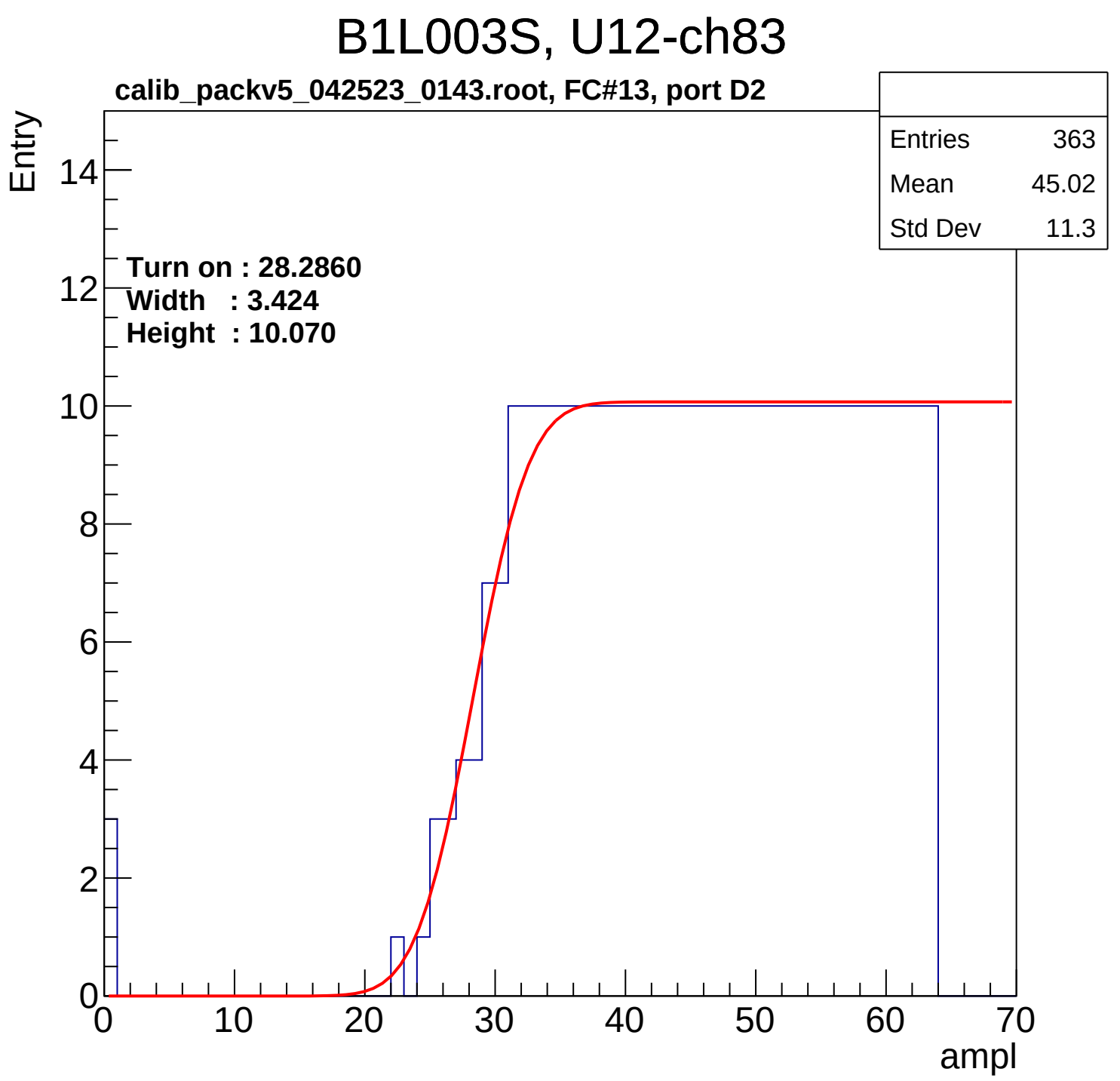

B1L003S, U12-ch78
calib_packv5_042523_0143.root, FC#13, port D2
Entries 370
Mean 44.62
Std Dev 11.64
Turn on : 27.5359
Width : 2.306
Height : 9.971
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

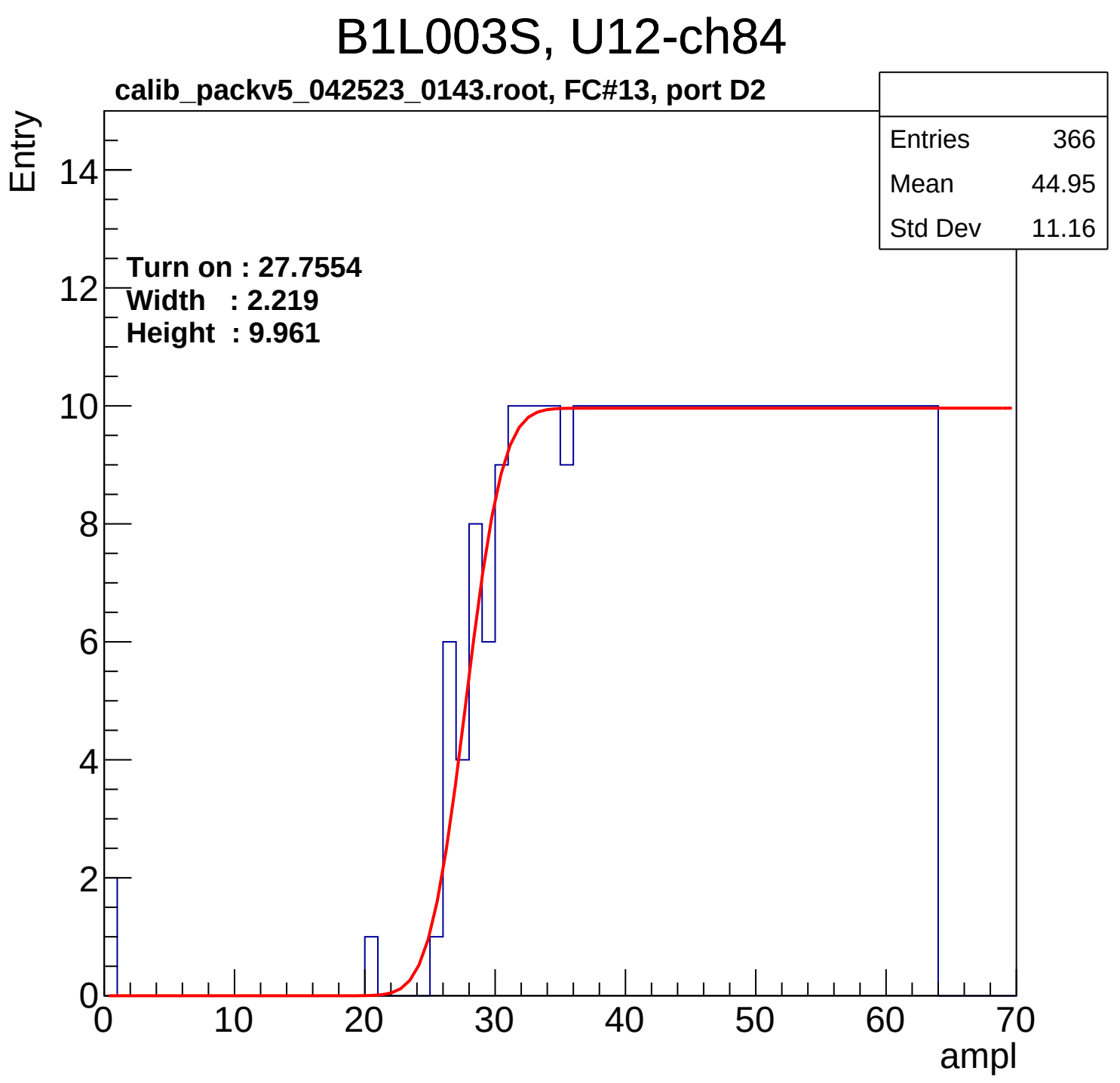

B1L003S, U12-ch79
calib_packv5_042523_0143.root, FC#13, port D2
Entries 383
Mean 43.98
Std Dev 12.02
Turn on : 26.3795
Width : 0.744
Height : 9.966
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

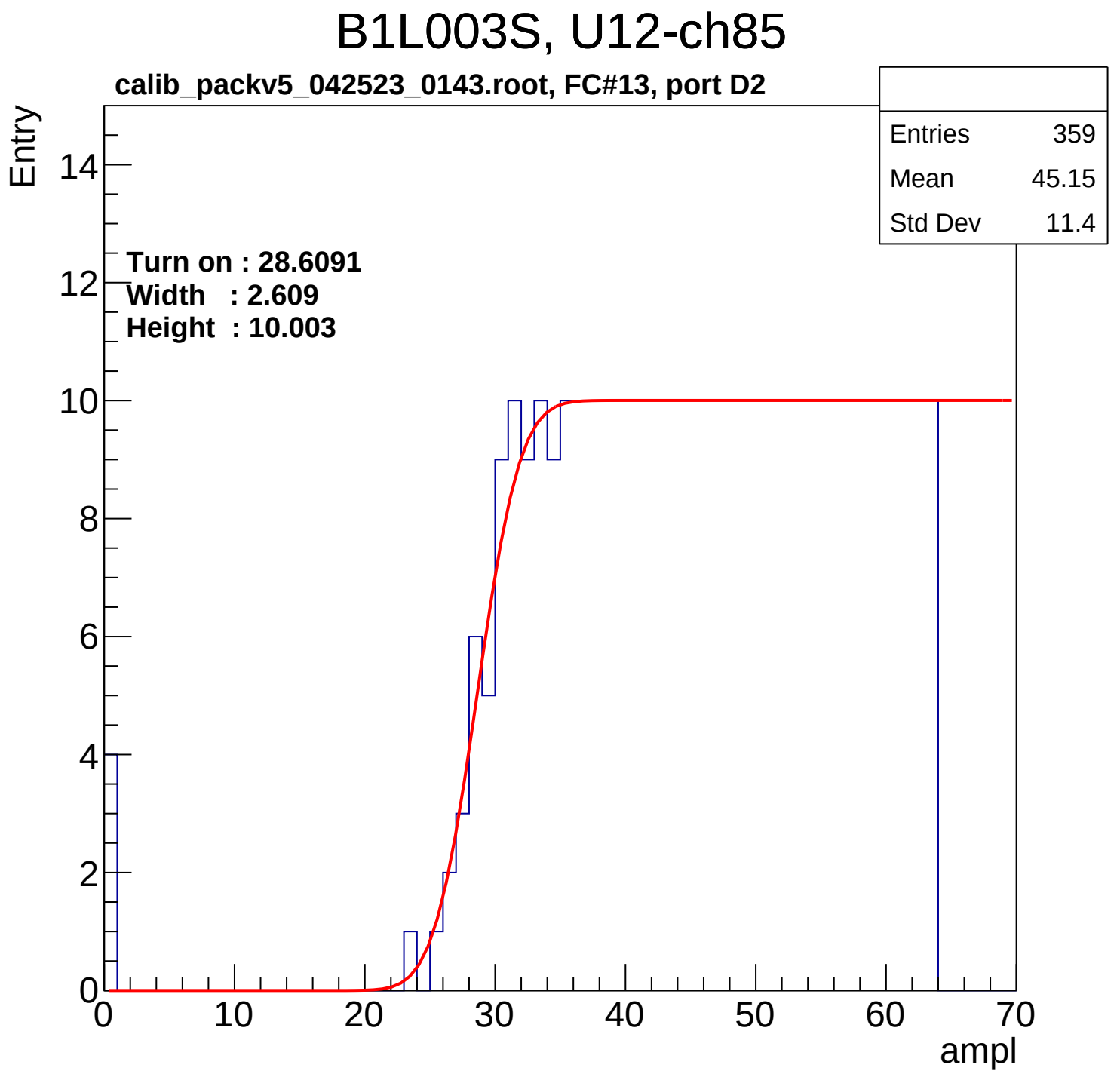

B1L003S, U12-ch80
calib_packv5_042523_0143.root, FC#13, port D2
Entries 386
Mean 43.95
Std Dev 11.71
Turn on : 25.6430
Width : 4.624
Height : 10.100
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

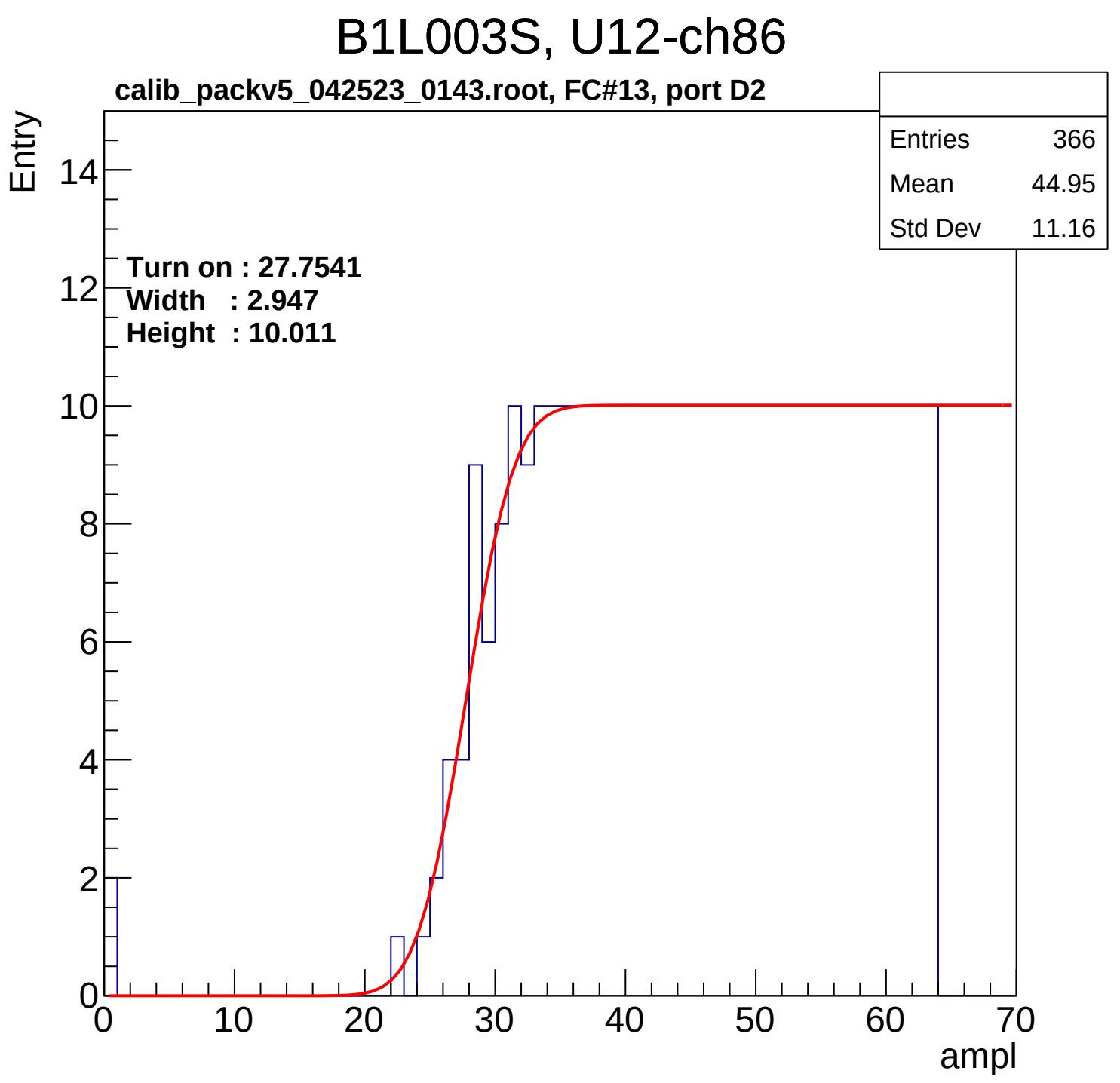

B1L003S, U12-ch81
calib_packv5_042523_0143.root, FC#13, port D2
Entries 362
Mean 45.02
Std Dev 11.34
Turn on : 27.3971
Width : 3.707
Height : 9.963
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

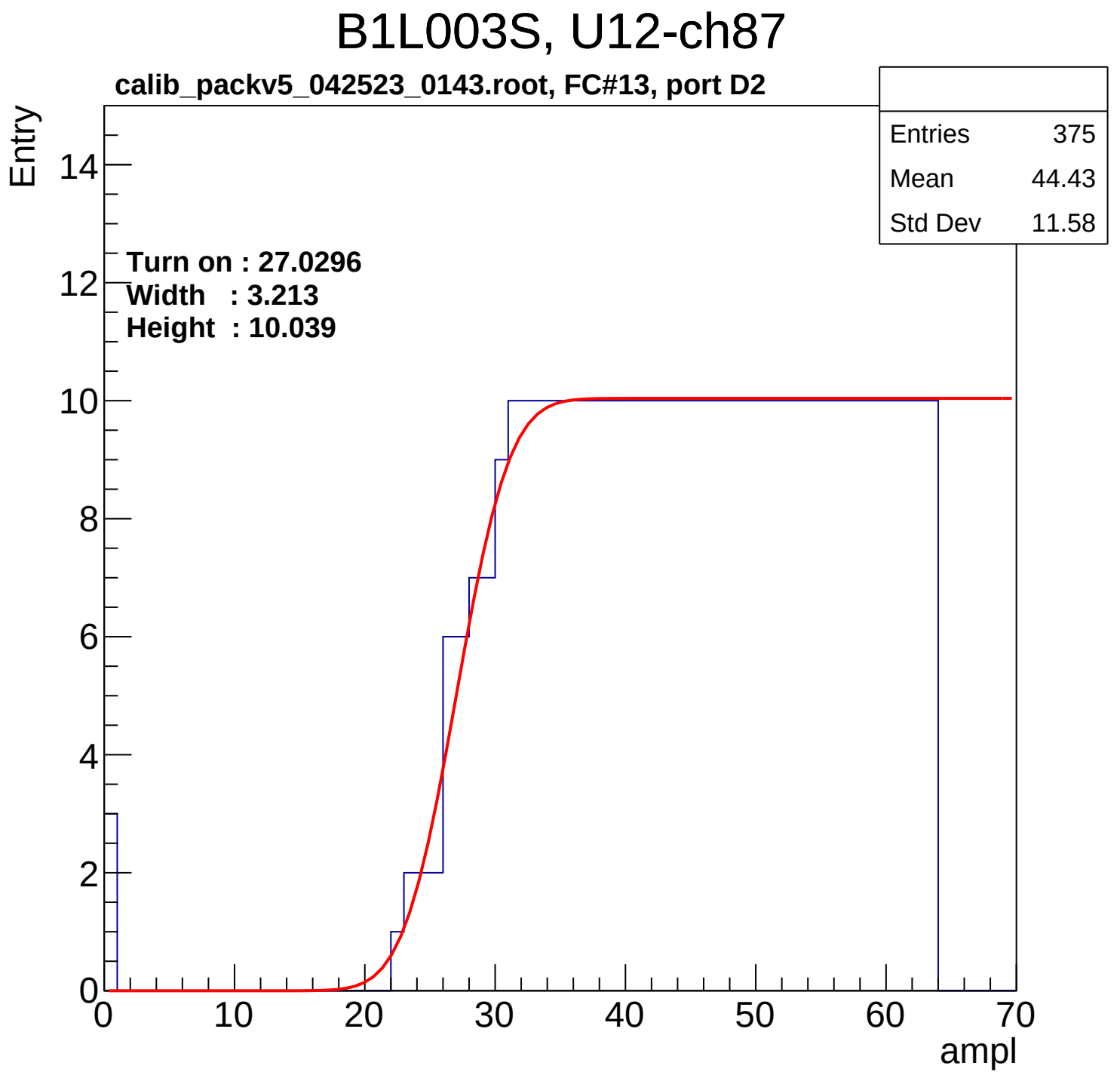

B1L003S, U12-ch82
calib_packv5_042523_0143.root, FC#13, port D2
Entries 370
Mean 44.87
Std Dev 10.99
Turn on : 27.2552
Width : 2.567
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

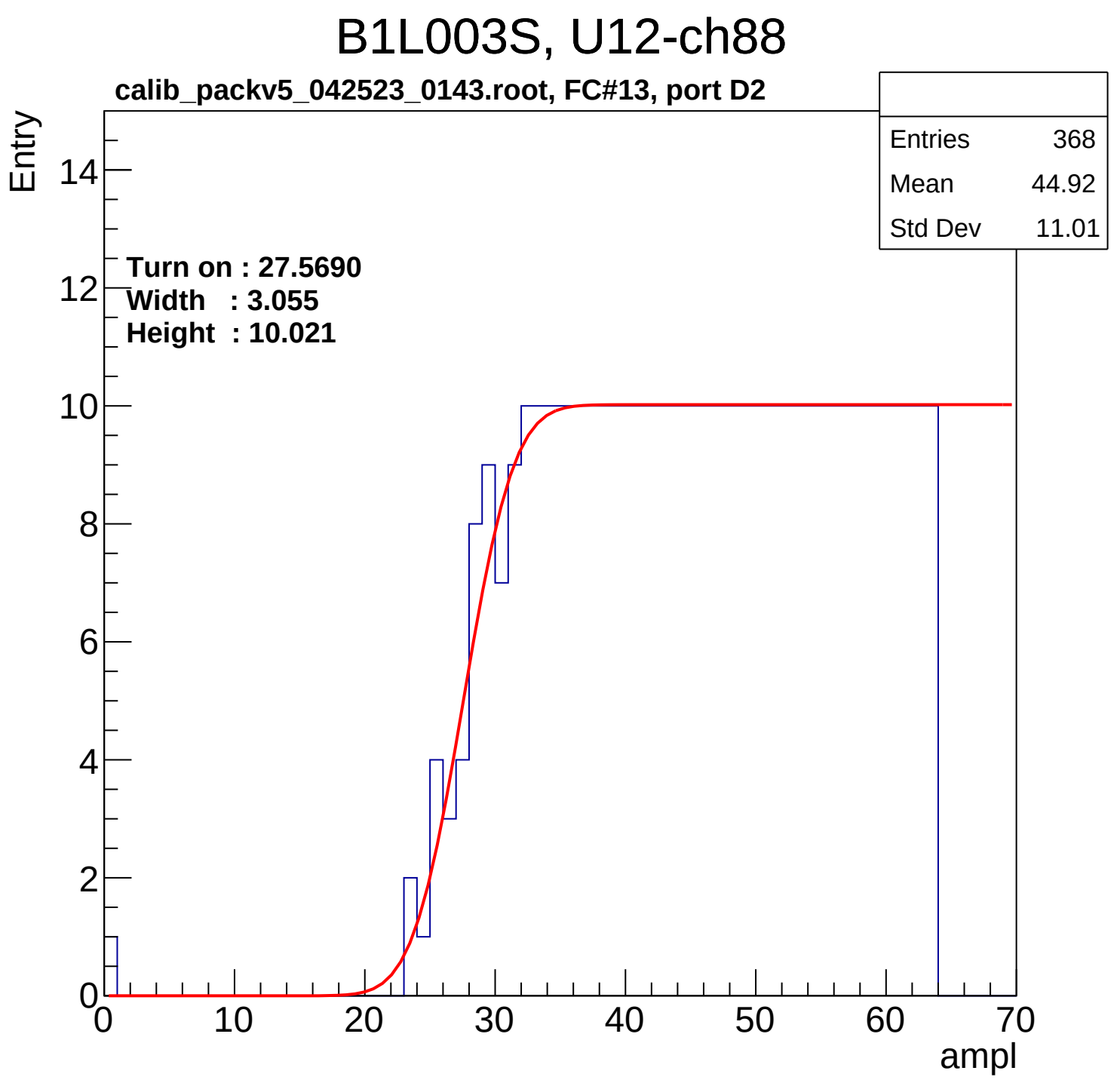

B1L003S, U12-ch83
calib_packv5_042523_0143.root, FC#13, port D2
Entries 363
Mean 45.02
Std Dev 11.3
Turn on : 28.2860
Width : 3.424
Height : 10.070
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

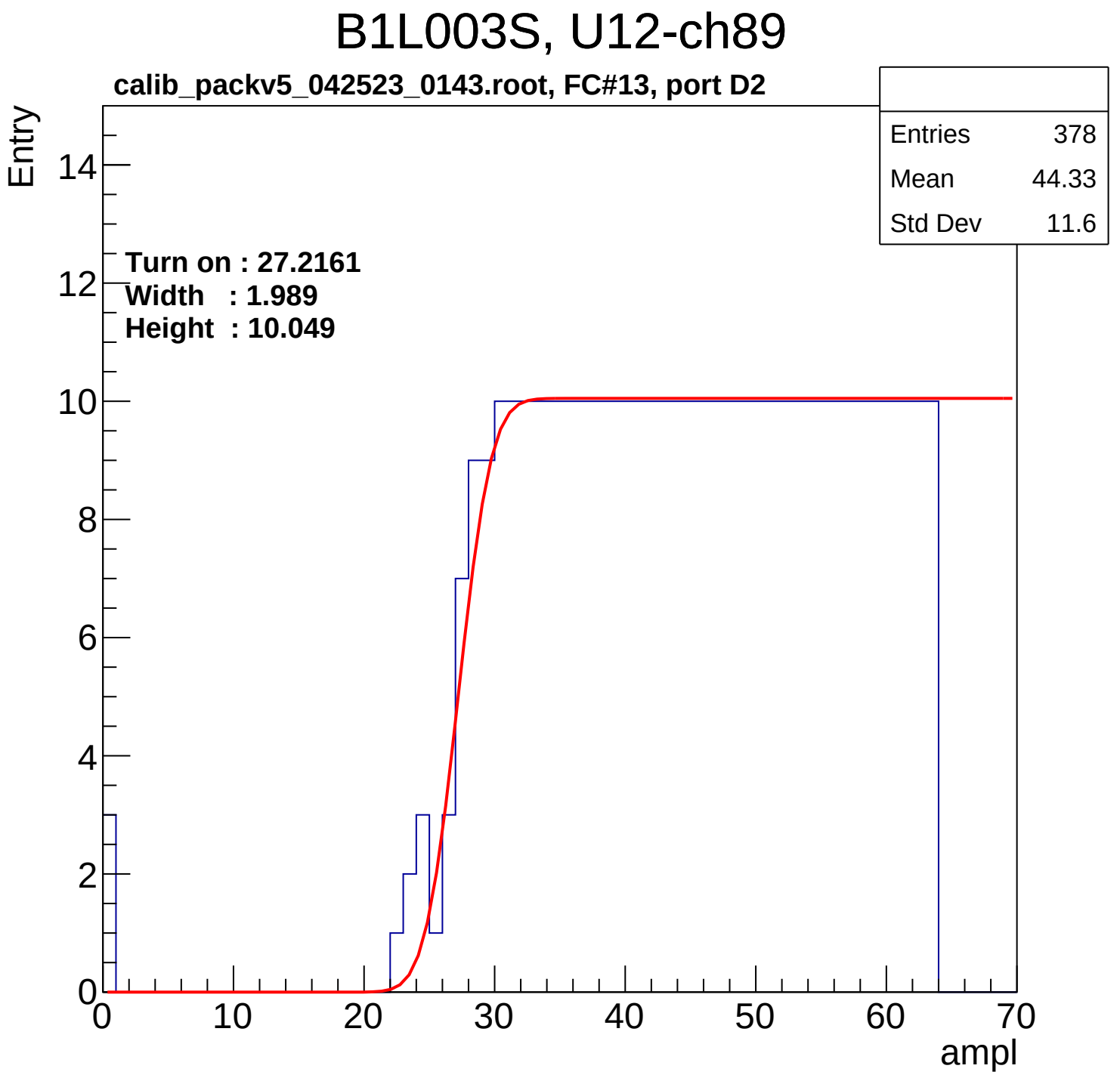

B1L003S, U12-ch84
calib_packv5_042523_0143.root, FC#13, port D2
Entries 366
Mean 44.95
Std Dev 11.16
Turn on : 27.7554
Width : 2.219
Height : 9.961
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

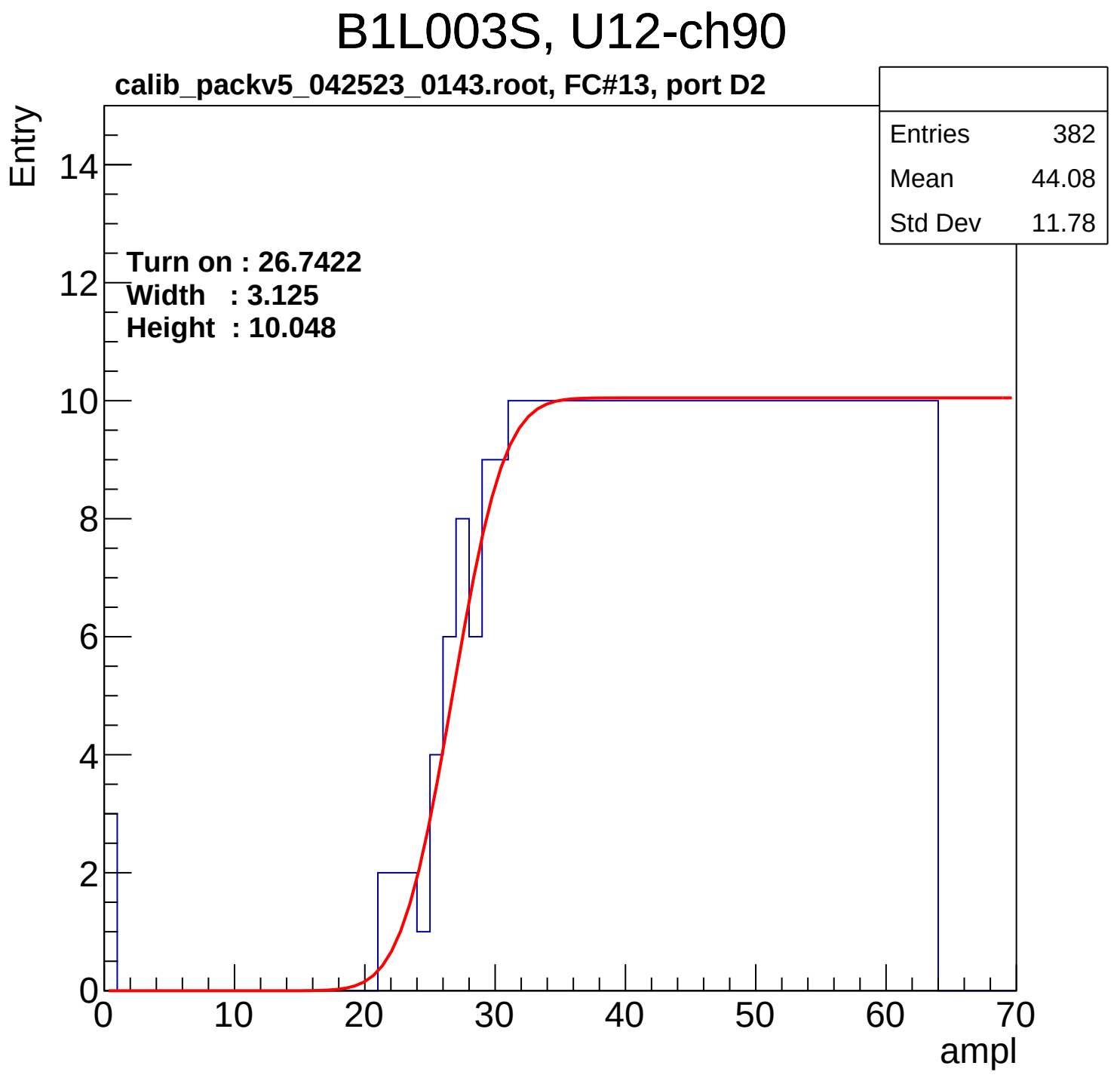

B1L003S, U12-ch85
calib_packv5_042523_0143.root, FC#13, port D2
Entries 359
Mean 45.15
Std Dev 11.4
Turn on : 28.6091
Width : 2.609
Height : 10.003
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

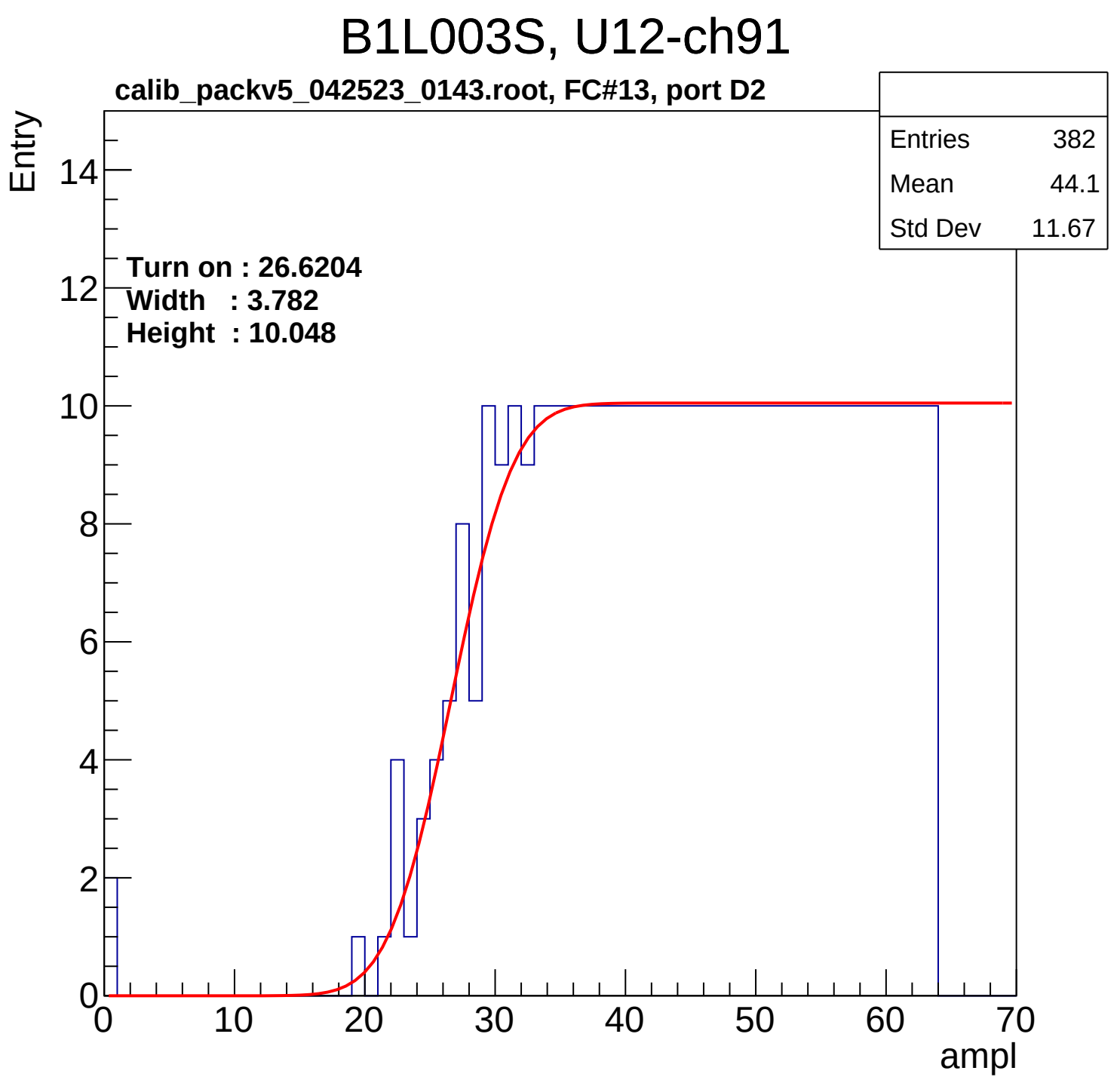

B1L003S, U12-ch86
calib_packv5_042523_0143.root, FC#13, port D2
Entries 366
Mean 44.95
Std Dev 11.16
Turn on : 27.7541
Width : 2.947
Height : 10.011
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

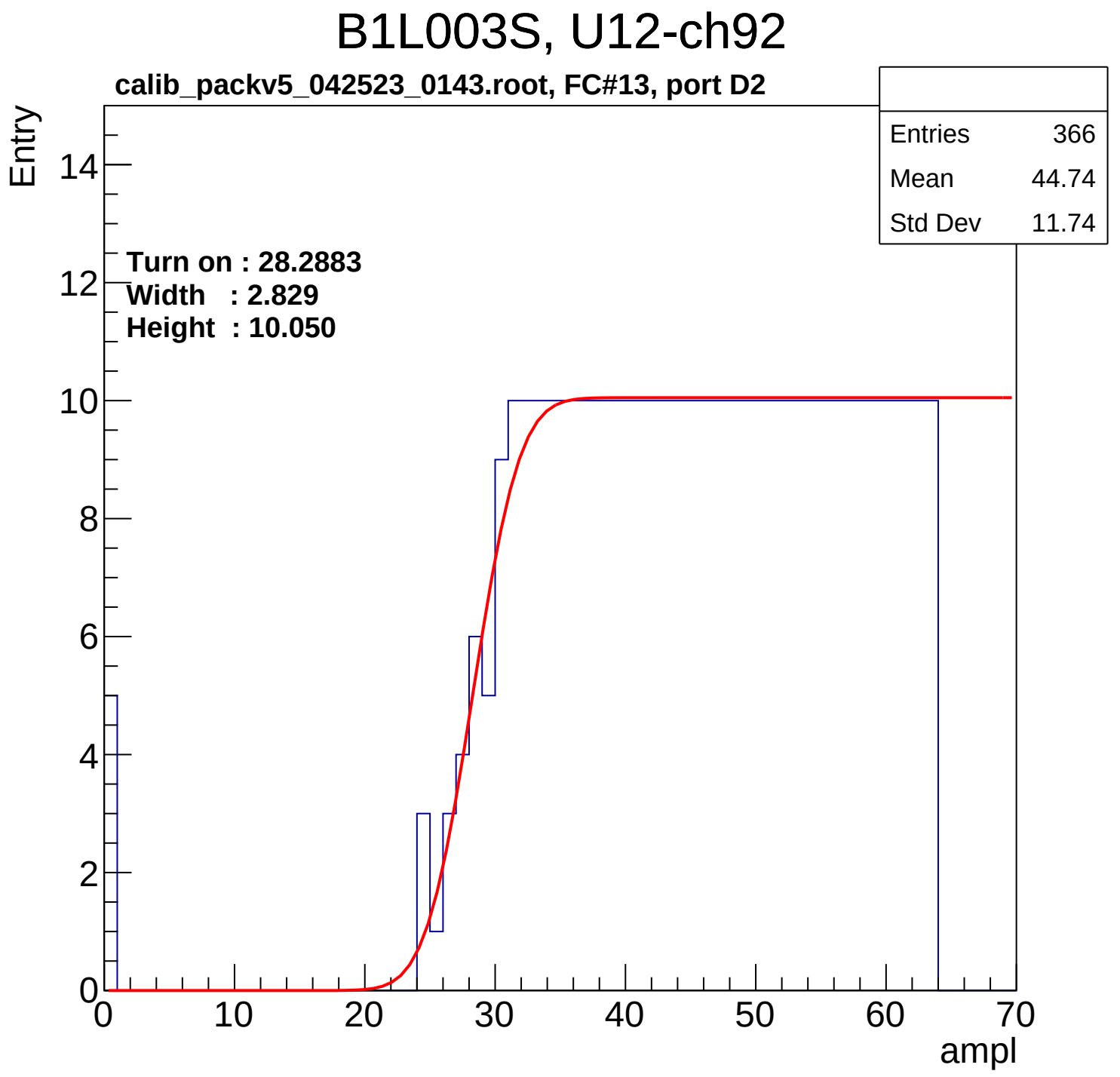

B1L003S, U12-ch87
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.43
Std Dev 11.58
Turn on : 27.0296
Width : 3.213
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

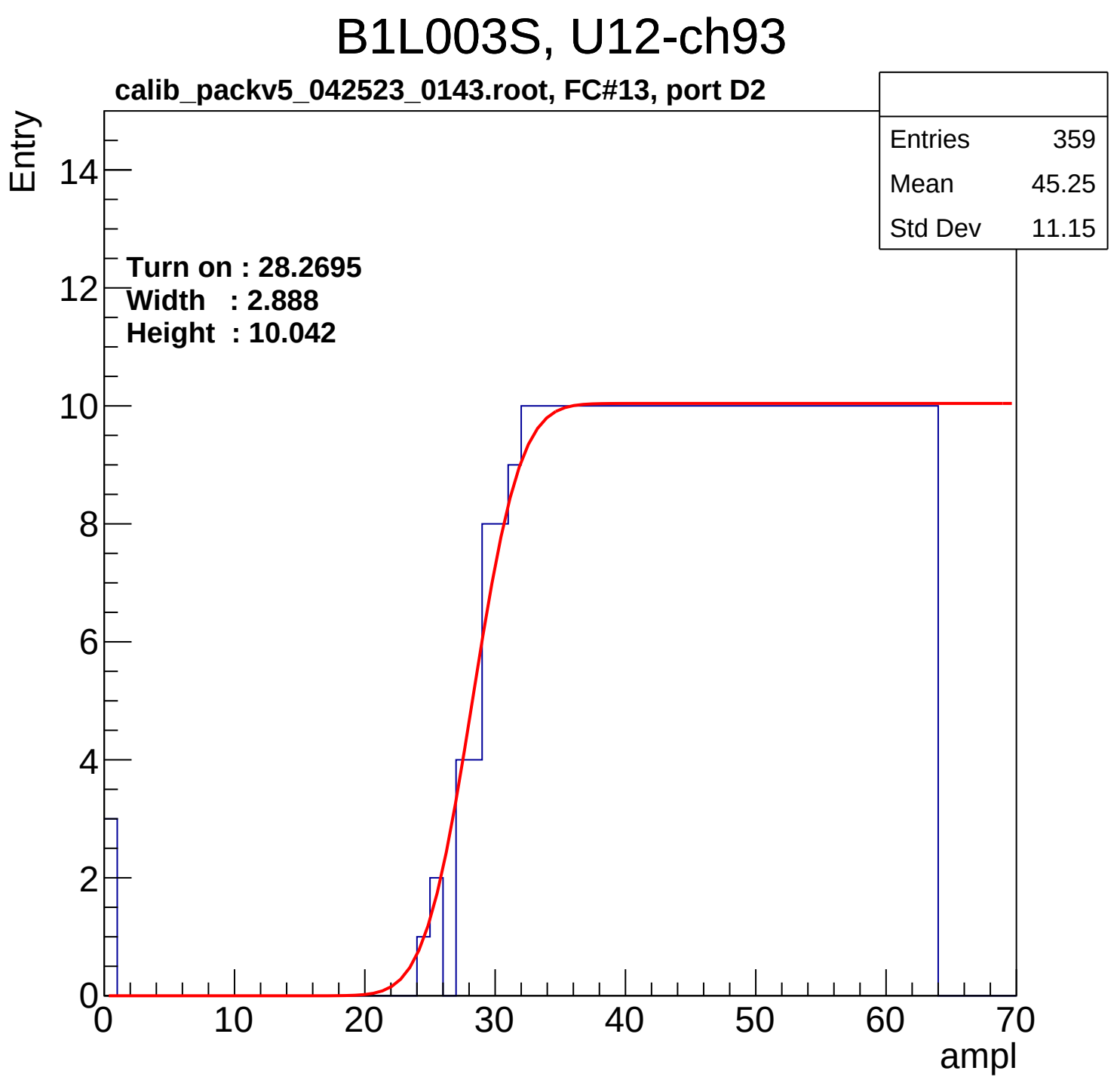

B1L003S, U12-ch88
calib_packv5_042523_0143.root, FC#13, port D2
Entries 368
Mean 44.92
Std Dev 11.01
Turn on : 27.5690
Width : 3.055
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

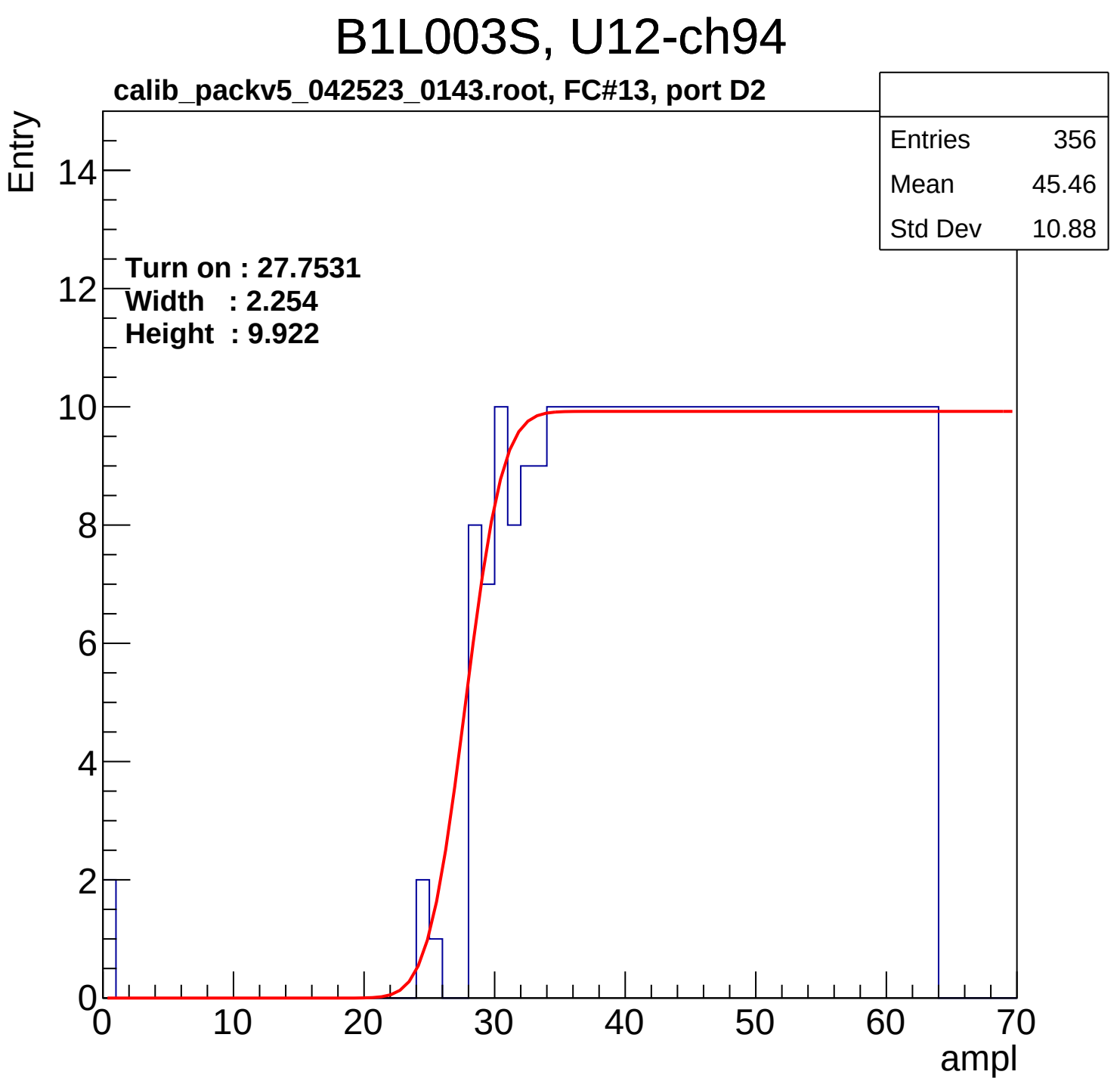

B1L003S, U12-ch89
calib_packv5_042523_0143.root, FC#13, port D2
Entries 378
Mean 44.33
Std Dev 11.6
Turn on : 27.2161
Width : 1.989
Height : 10.049
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

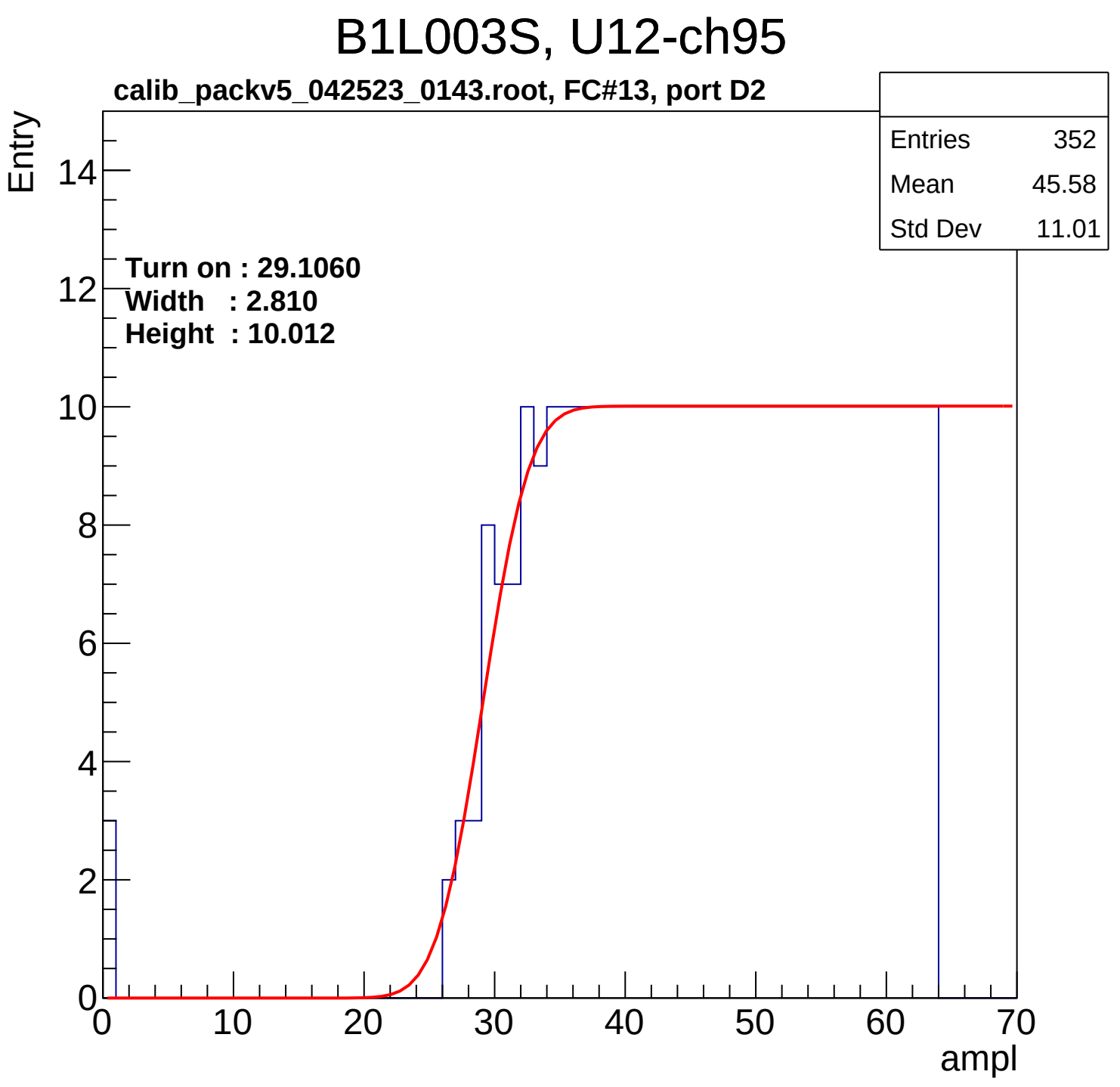

B1L003S, U12-ch90
calib_packv5_042523_0143.root, FC#13, port D2
Entries 382
Mean 44.08
Std Dev 11.78
Turn on : 26.7422
Width : 3.125
Height : 10.048
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

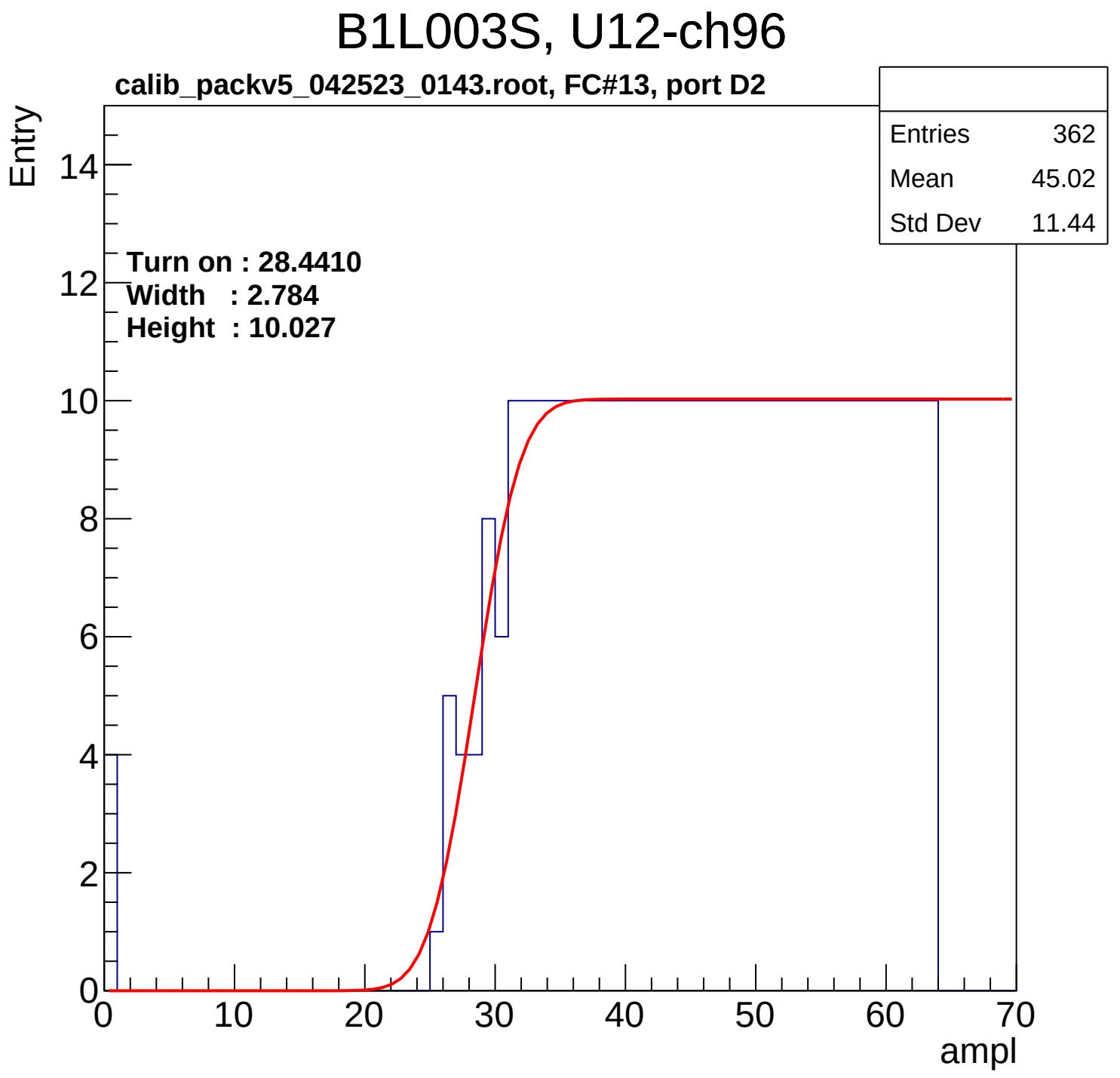

B1L003S, U12-ch91
calib_packv5_042523_0143.root, FC#13, port D2
Entries 382
Mean 44.1
Std Dev 11.67
Turn on : 26.6204
Width : 3.782
Height : 10.048
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

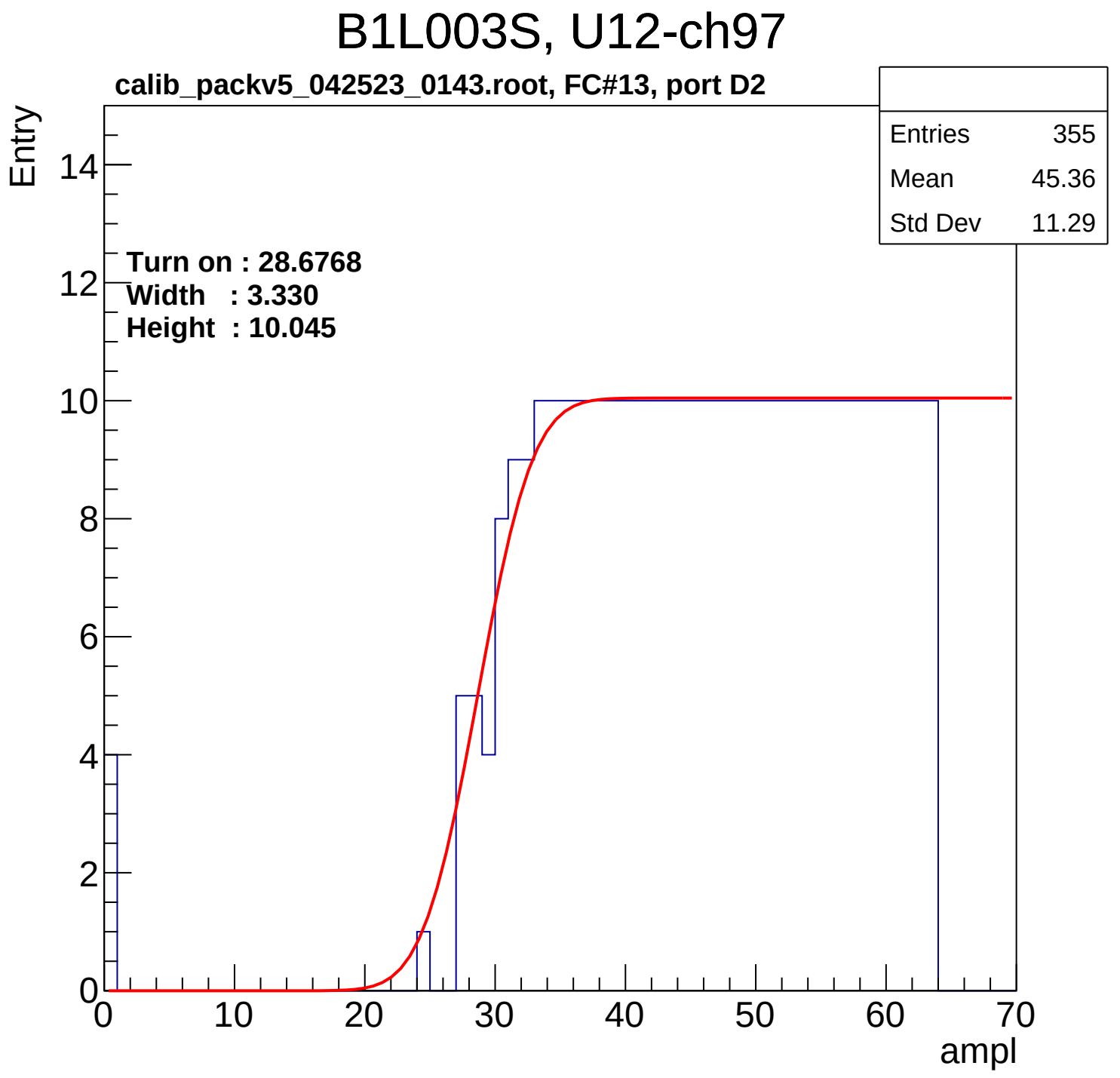

B1L003S, U12-ch92
calib_packv5_042523_0143.root, FC#13, port D2
Entries 366
Mean 44.74
Std Dev 11.74
Turn on : 28.2883
Width : 2.829
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

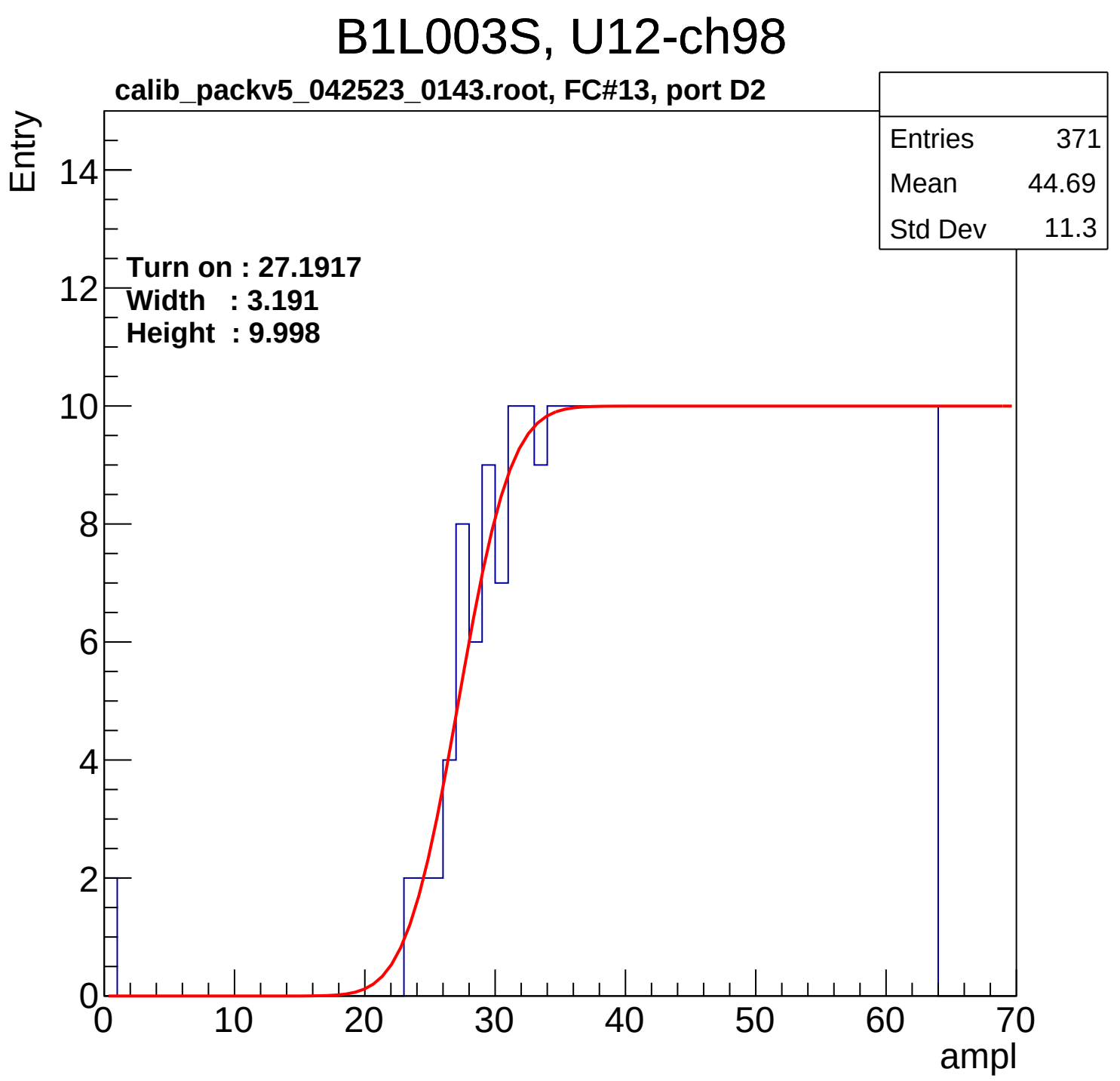

B1L003S, U12-ch93
calib_packv5_042523_0143.root, FC#13, port D2
Entries 359
Mean 45.25
Std Dev 11.15
Turn on : 28.2695
Width : 2.888
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

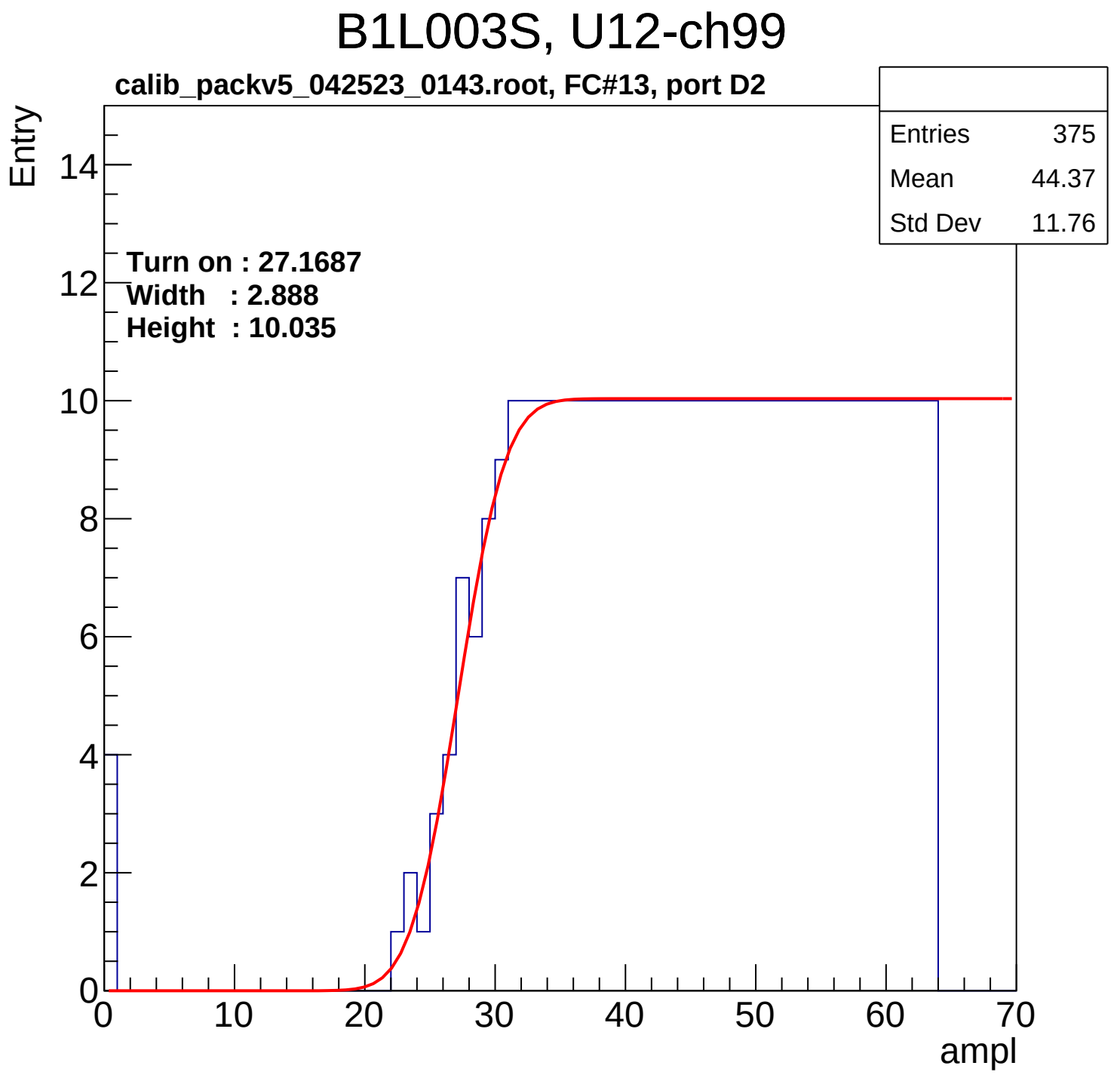

B1L003S, U12-ch94
calib_packv5_042523_0143.root, FC#13, port D2
Entries 356
Mean 45.46
Std Dev 10.88
Turn on : 27.7531
Width : 2.254
Height : 9.922
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

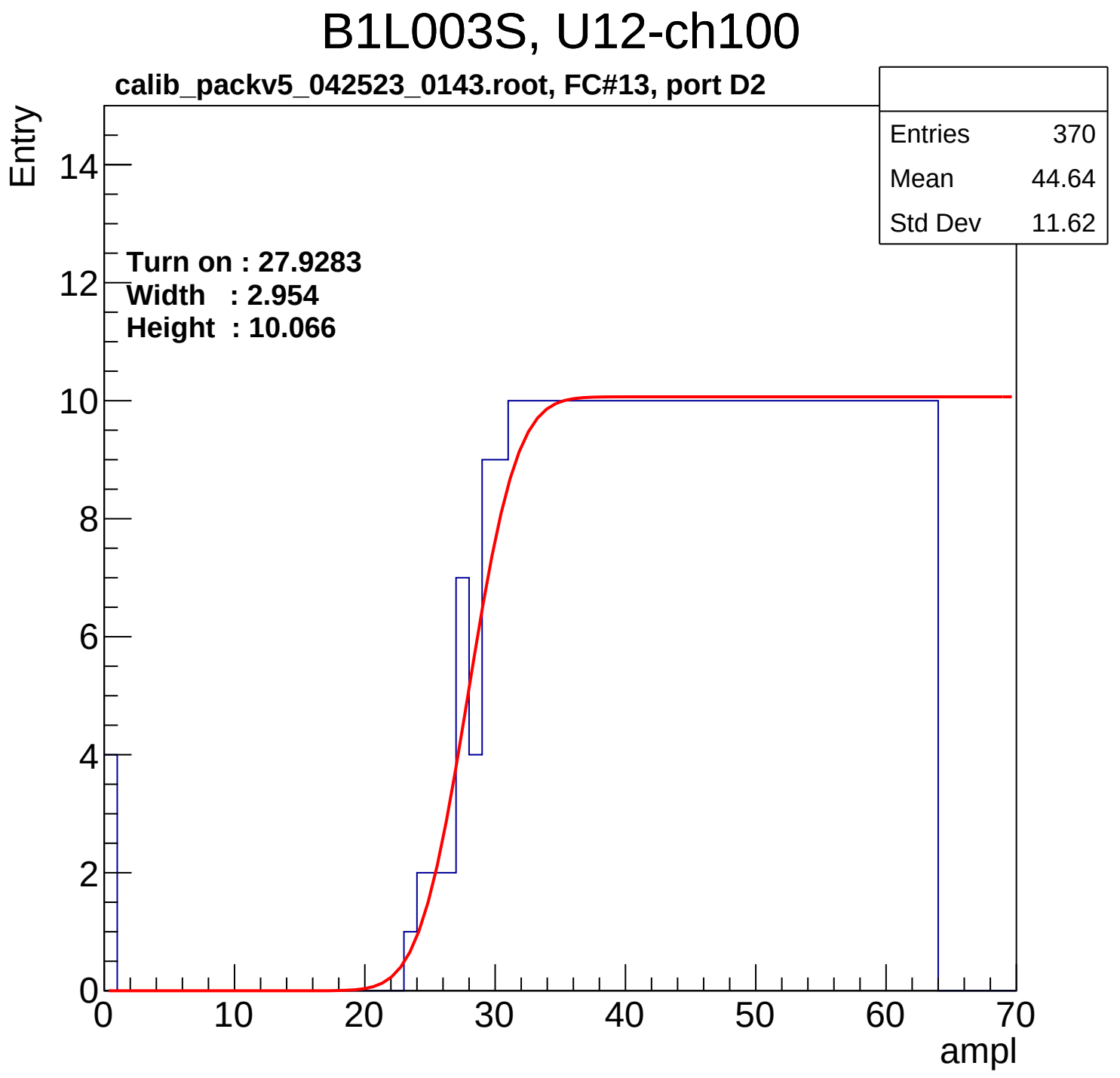

B1L003S, U12-ch95
calib_packv5_042523_0143.root, FC#13, port D2
Entries 352
Mean 45.58
Std Dev 11.01
Turn on : 29.1060
Width : 2.810
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

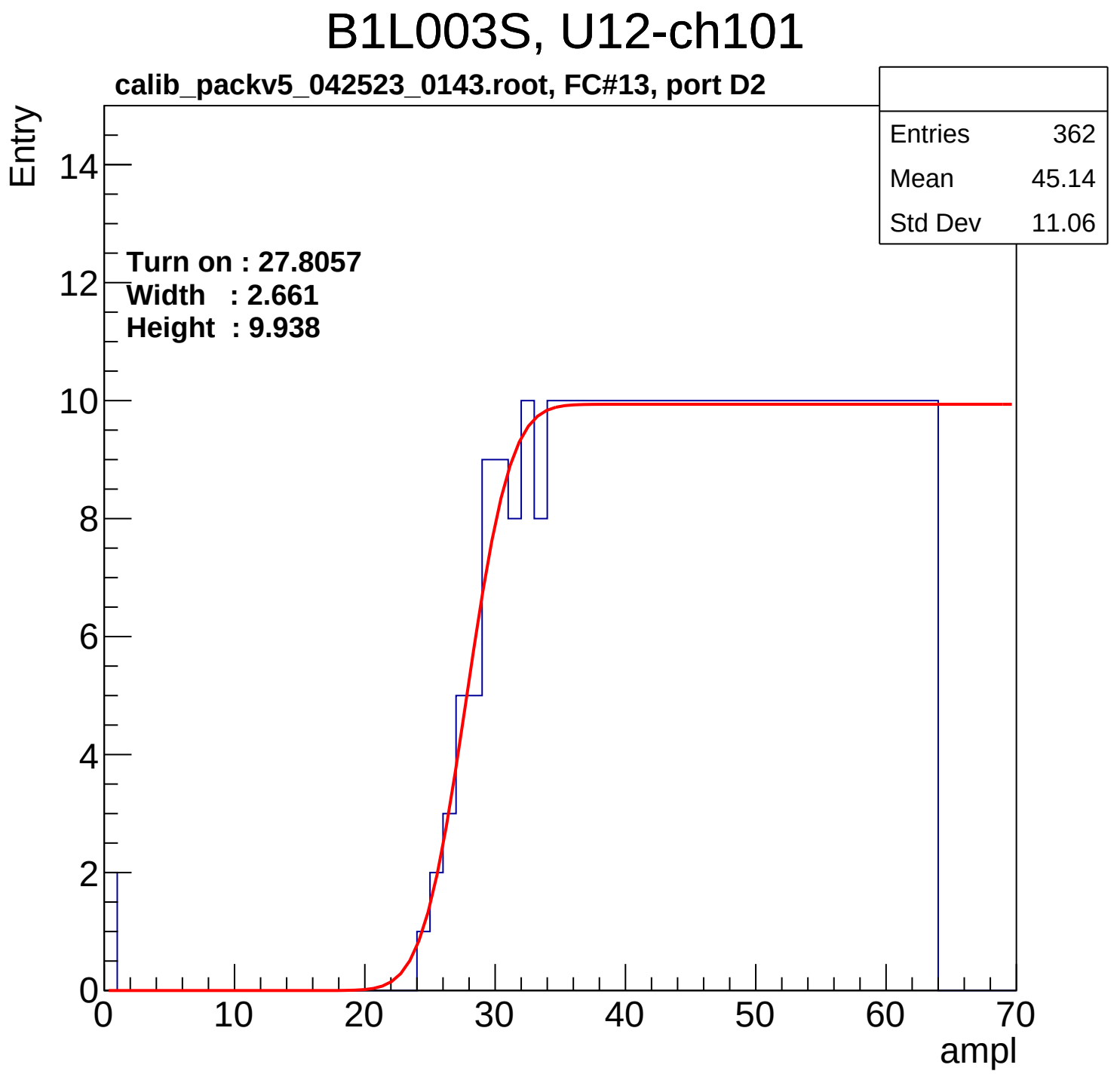

B1L003S, U12-ch96
calib_packv5_042523_0143.root, FC#13, port D2
Entries 362
Mean 45.02
Std Dev 11.44
Turn on : 28.4410
Width : 2.784
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

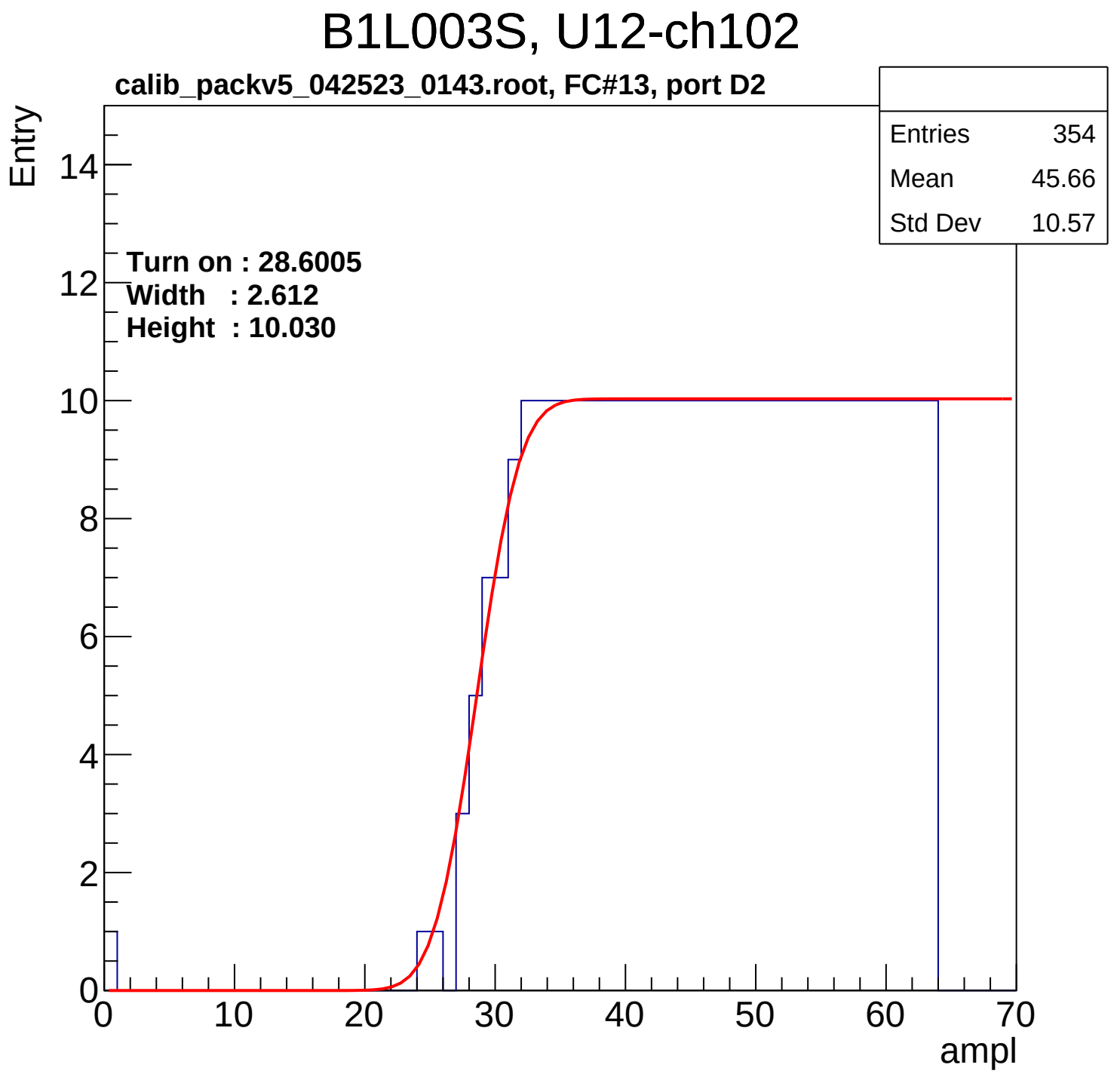

B1L003S, U12-ch97
calib_packv5_042523_0143.root, FC#13, port D2
Entries 355
Mean 45.36
Std Dev 11.29
Turn on : 28.6768
Width : 3.330
Height : 10.045
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

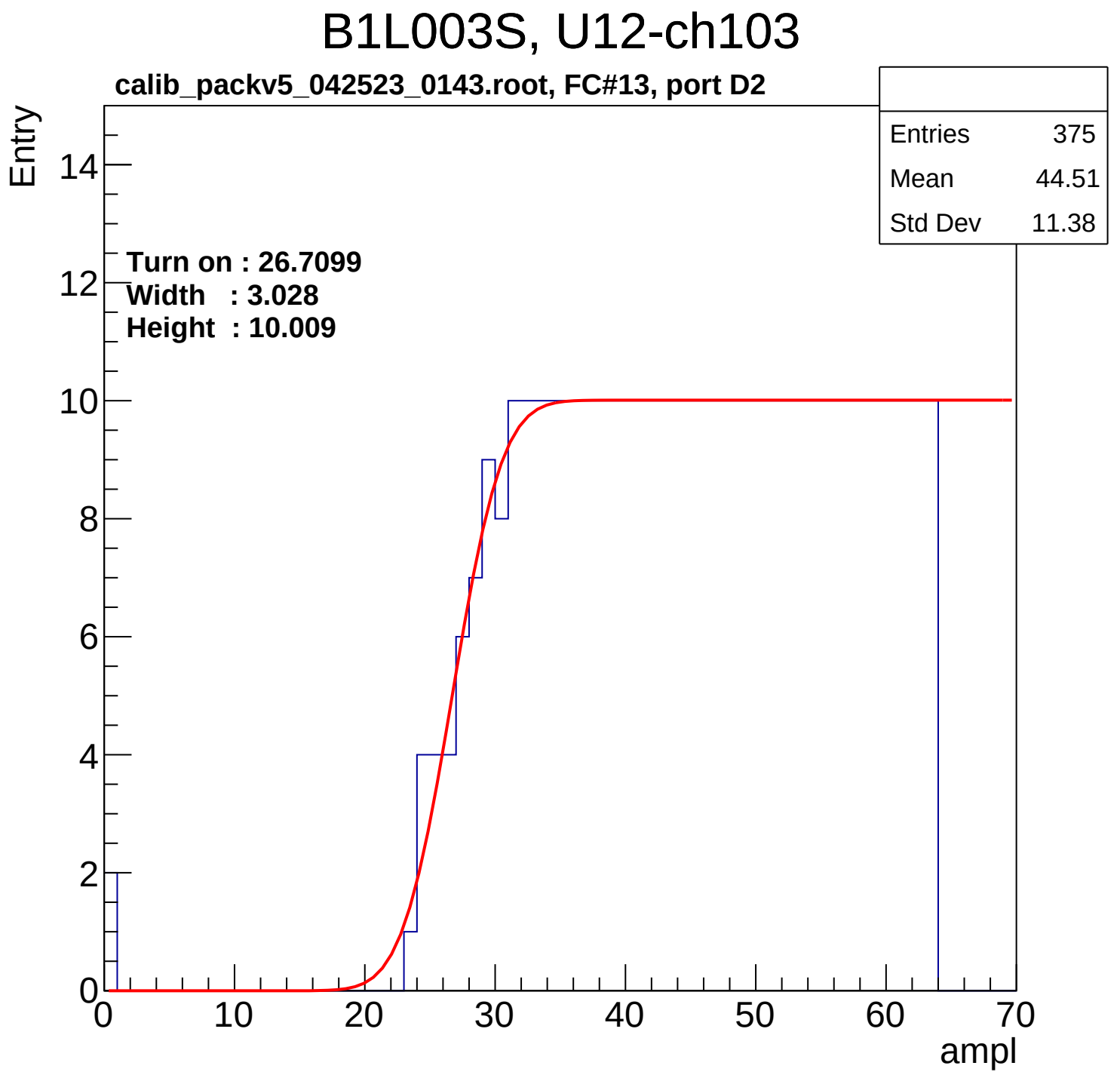

B1L003S, U12-ch98
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.69
Std Dev 11.3
Turn on : 27.1917
Width : 3.191
Height : 9.998
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

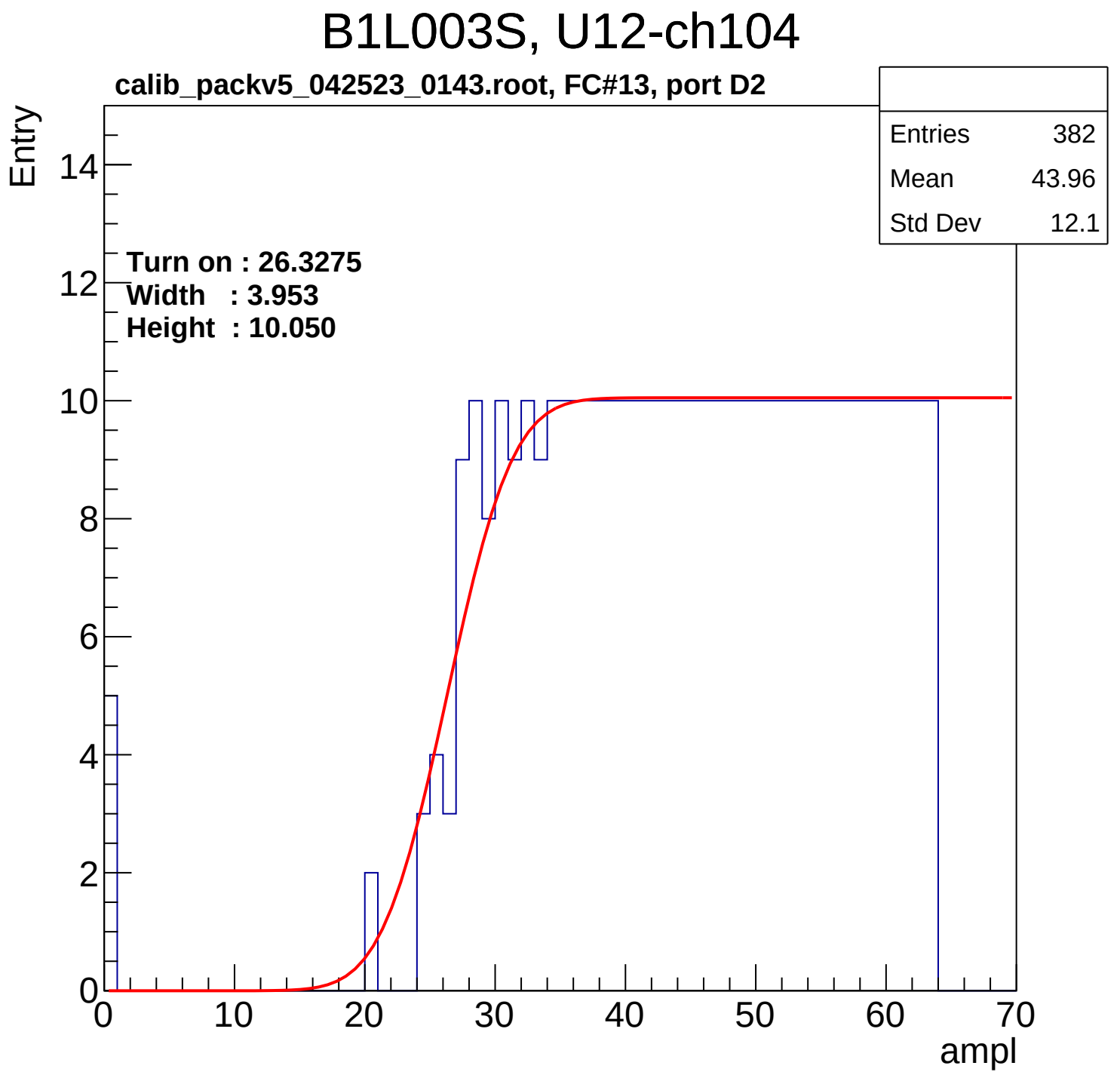

B1L003S, U12-ch99
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.37
Std Dev 11.76
Turn on : 27.1687
Width : 2.888
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

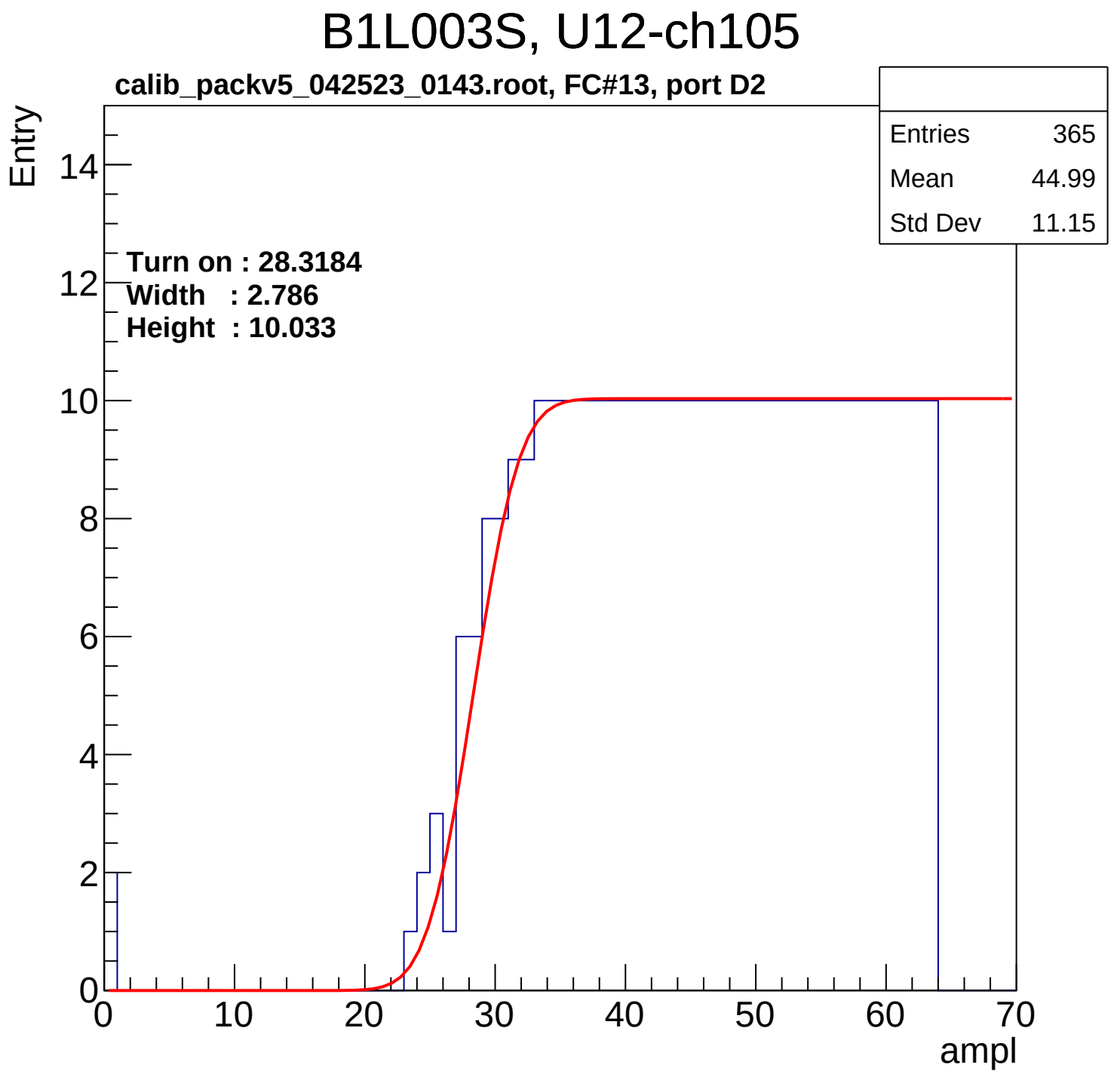

B1L003S, U12-ch100
calib_packv5_042523_0143.root, FC#13, port D2
Entries 370
Mean 44.64
Std Dev 11.62
Turn on : 27.9283
Width : 2.954
Height : 10.066
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

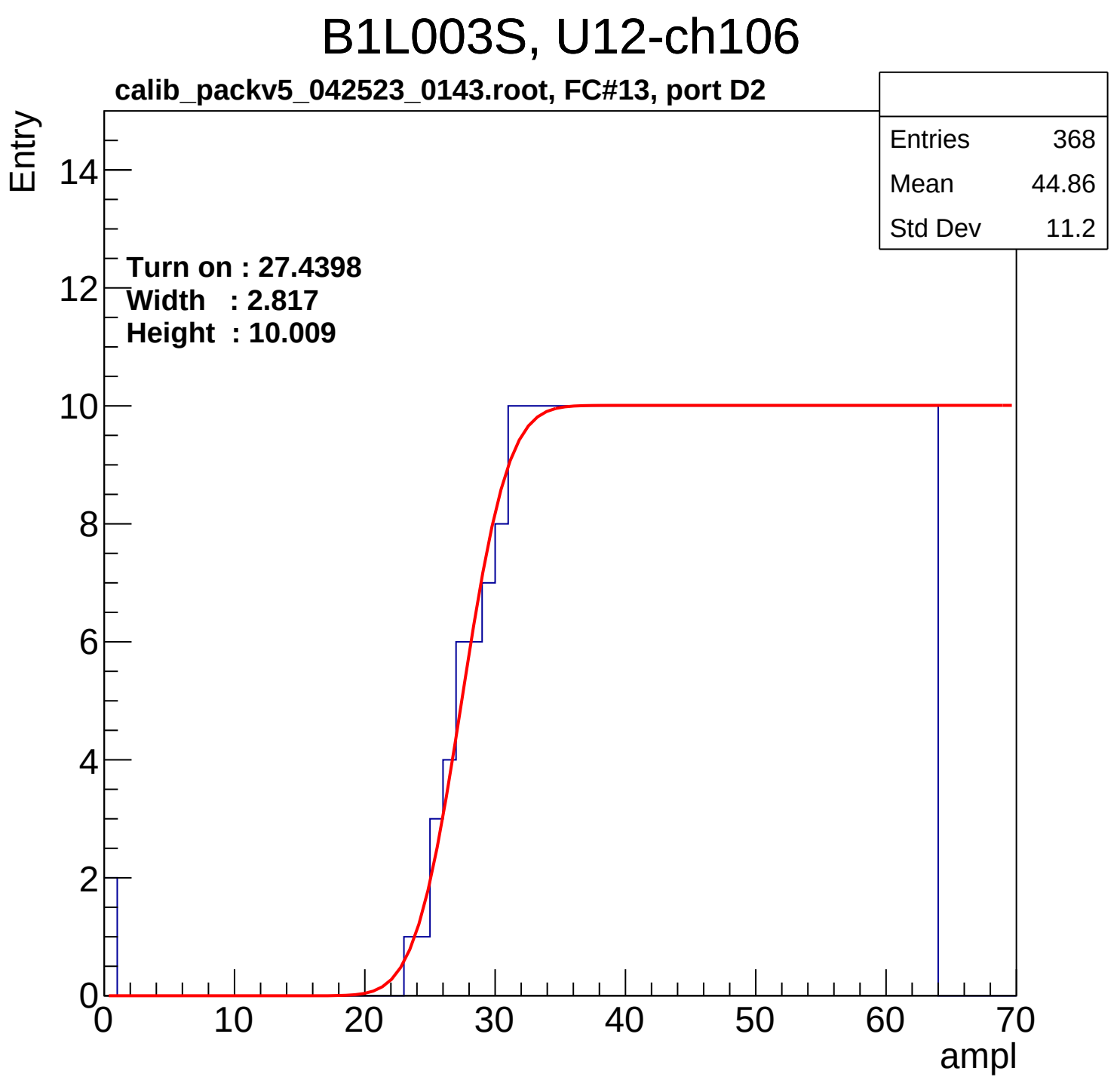

B1L003S, U12-ch101
calib_packv5_042523_0143.root, FC#13, port D2
Entries 362
Mean 45.14
Std Dev 11.06
Turn on : 27.8057
Width : 2.661
Height : 9.938
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

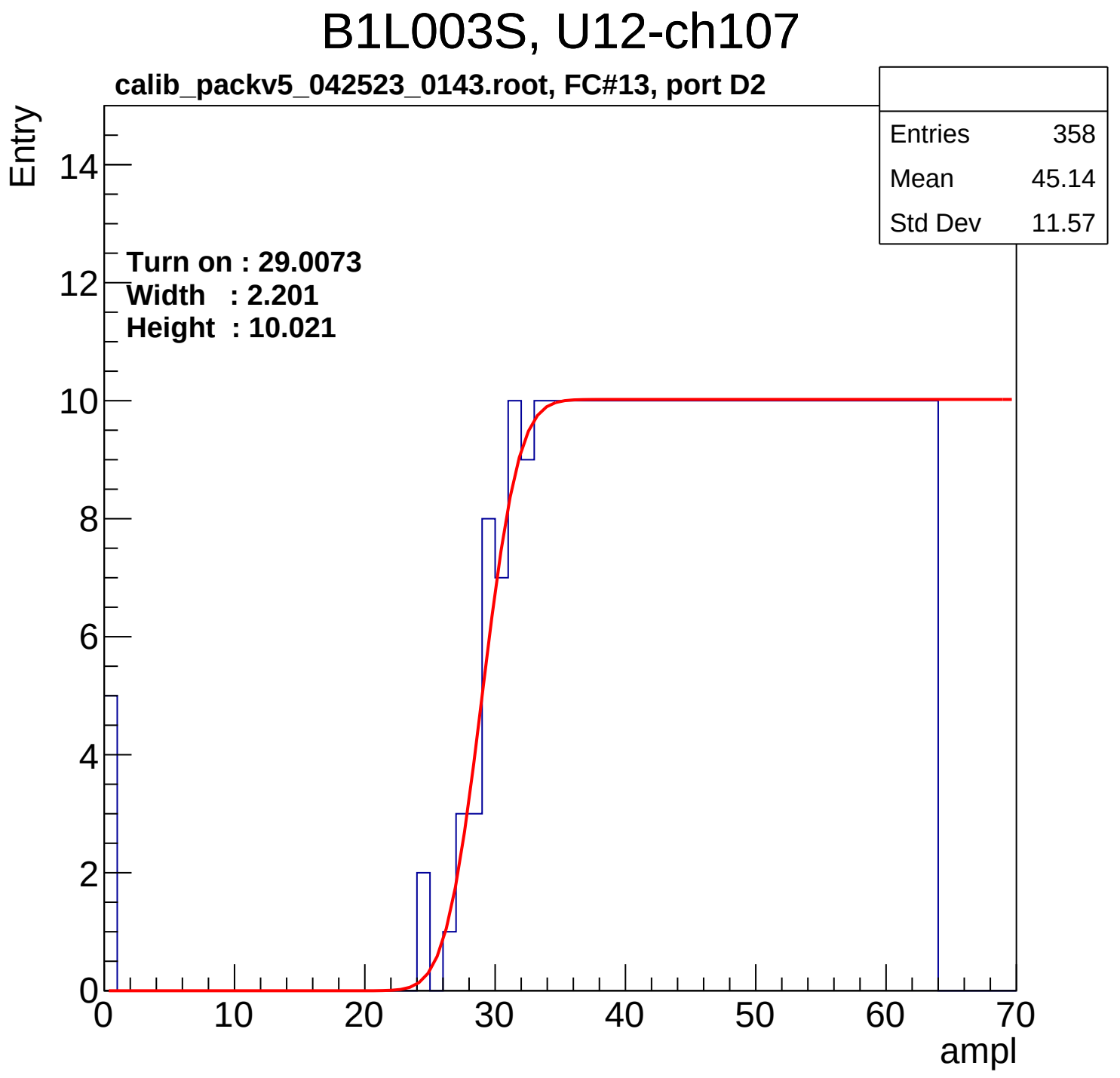

B1L003S, U12-ch102
calib_packv5_042523_0143.root, FC#13, port D2
Entries 354
Mean 45.66
Std Dev 10.57
Turn on : 28.6005
Width : 2.612
Height : 10.030
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

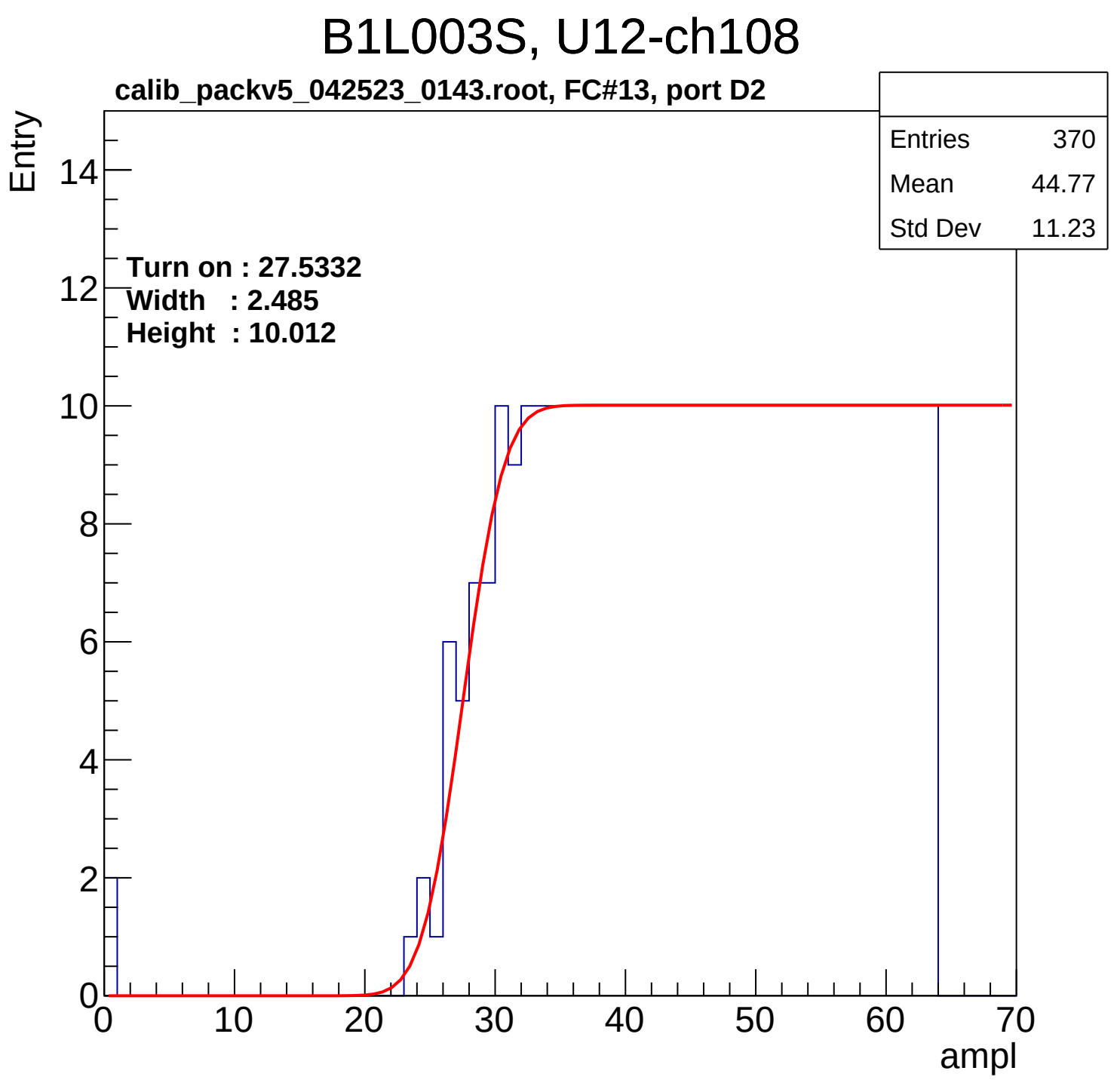

B1L003S, U12-ch103
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.51
Std Dev 11.38
Turn on : 26.7099
Width : 3.028
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

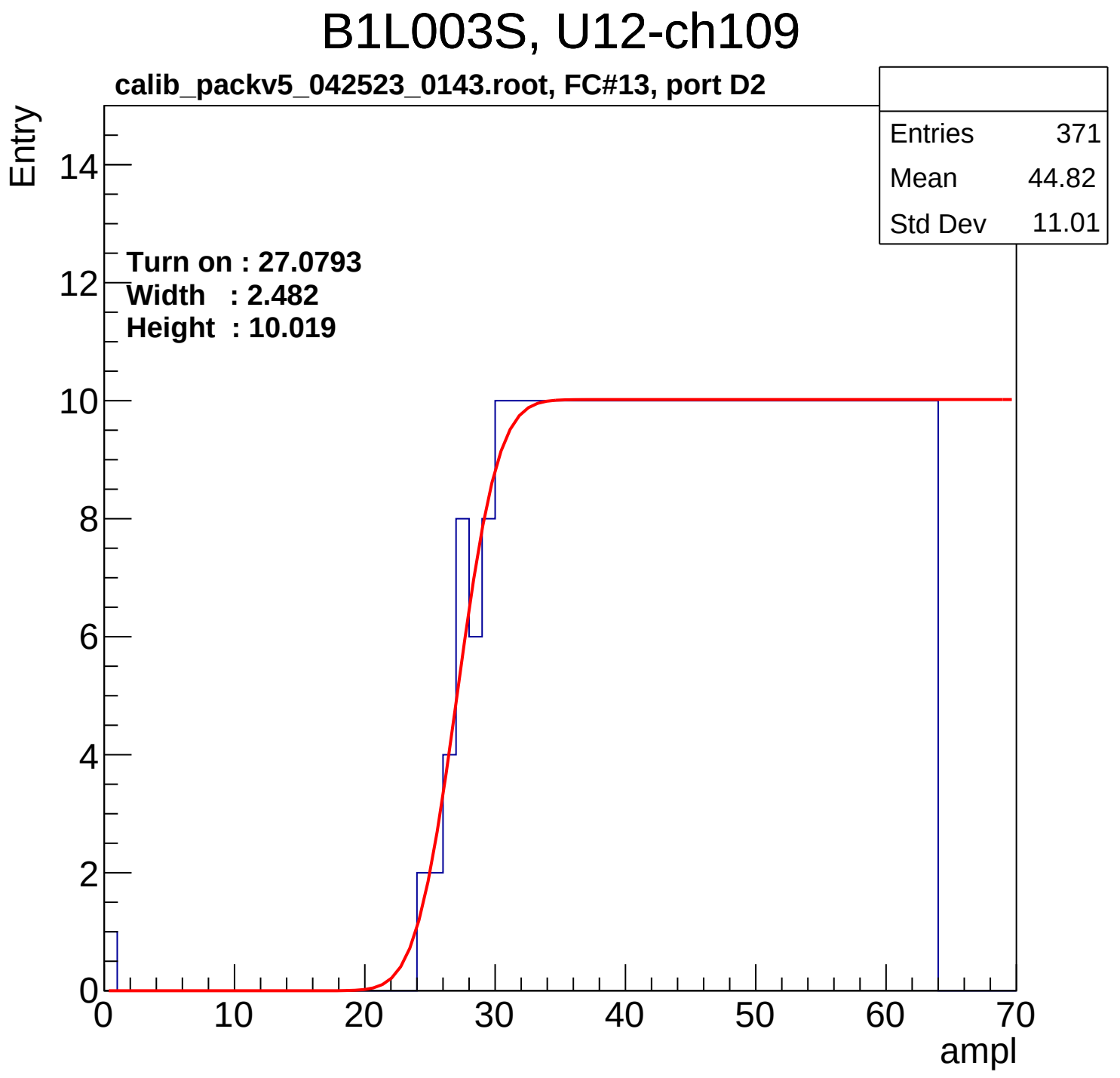

B1L003S, U12-ch104
calib_packv5_042523_0143.root, FC#13, port D2
Entries 382
Mean 43.96
Std Dev 12.1
Turn on : 26.3275
Width : 3.953
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

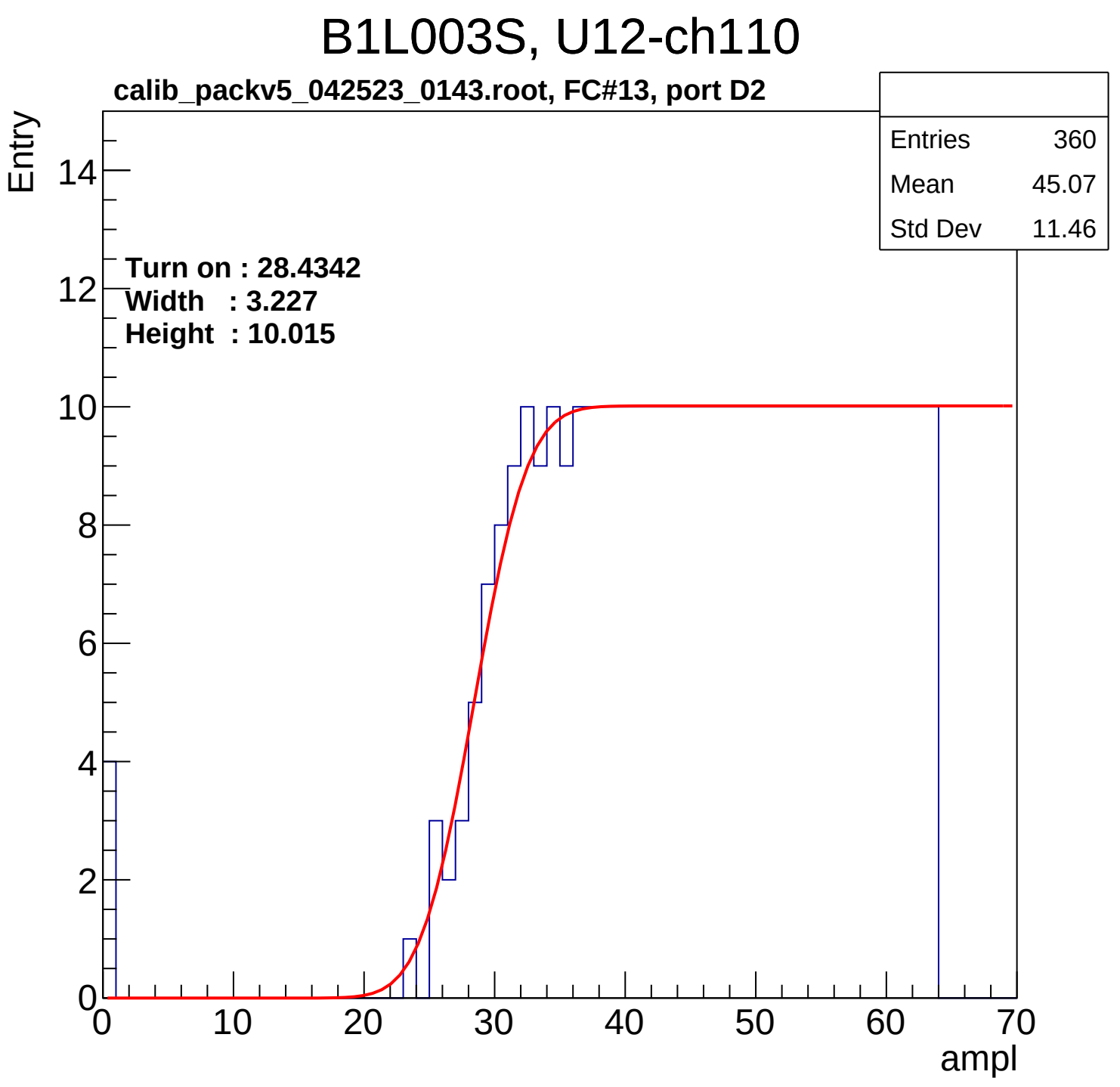

B1L003S, U12-ch105
calib_packv5_042523_0143.root, FC#13, port D2
Entries 365
Mean 44.99
Std Dev 11.15
Turn on : 28.3184
Width : 2.786
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

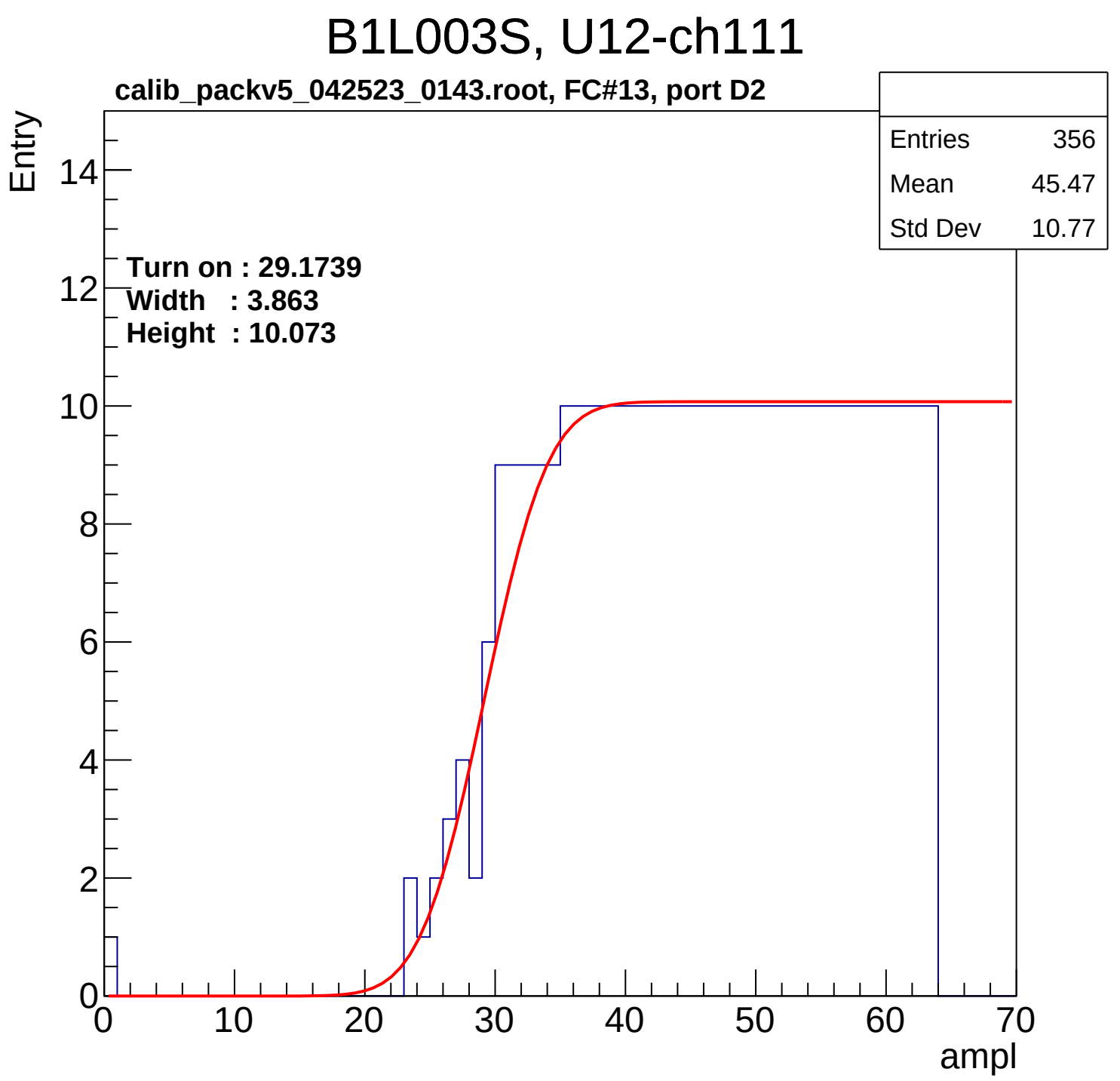

B1L003S, U12-ch106
calib_packv5_042523_0143.root, FC#13, port D2
Entries 368
Mean 44.86
Std Dev 11.2
Turn on : 27.4398
Width : 2.817
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

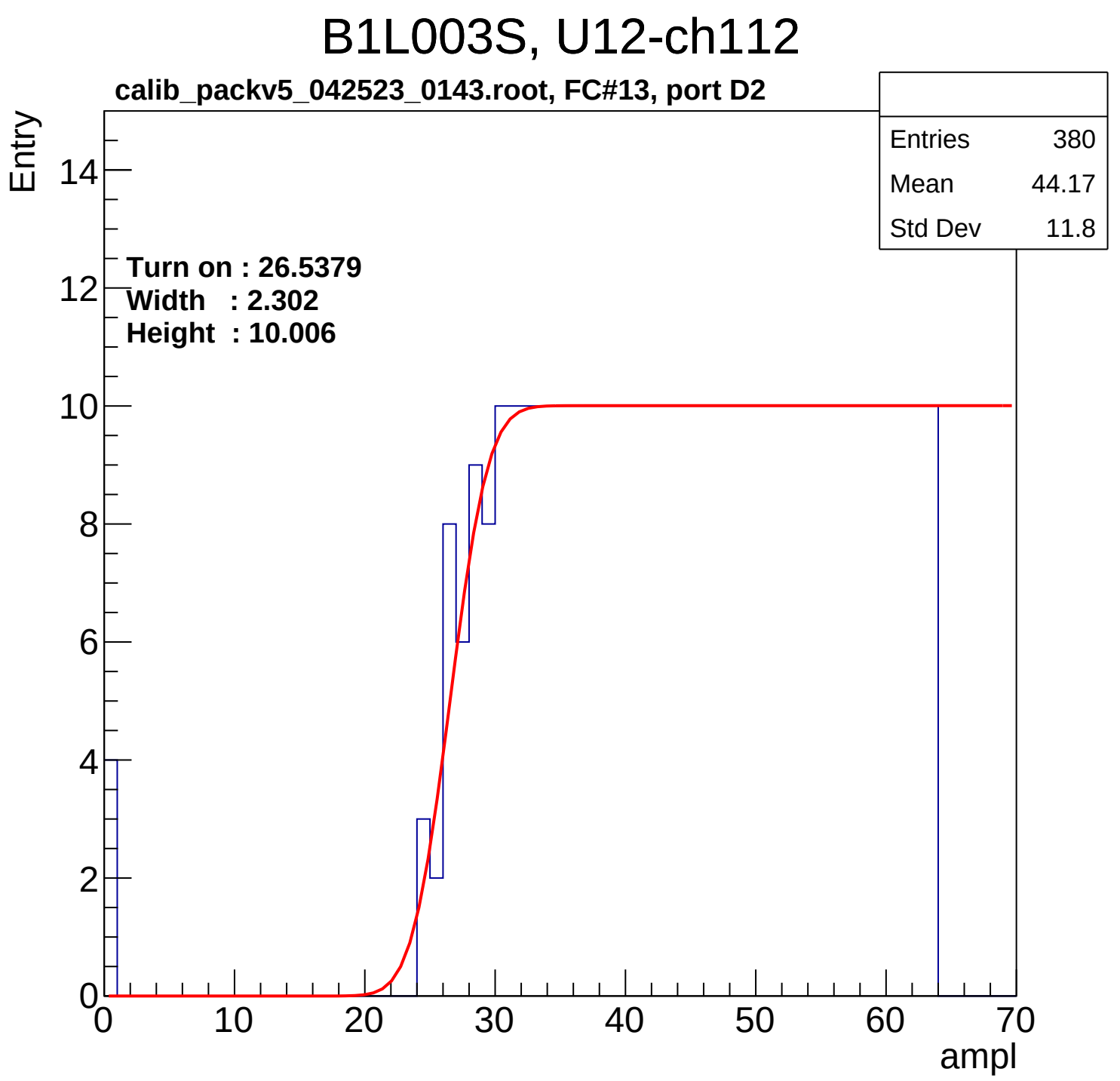

B1L003S, U12-ch107
calib_packv5_042523_0143.root, FC#13, port D2
Entries 358
Mean 45.14
Std Dev 11.57
Turn on : 29.0073
Width : 2.201
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

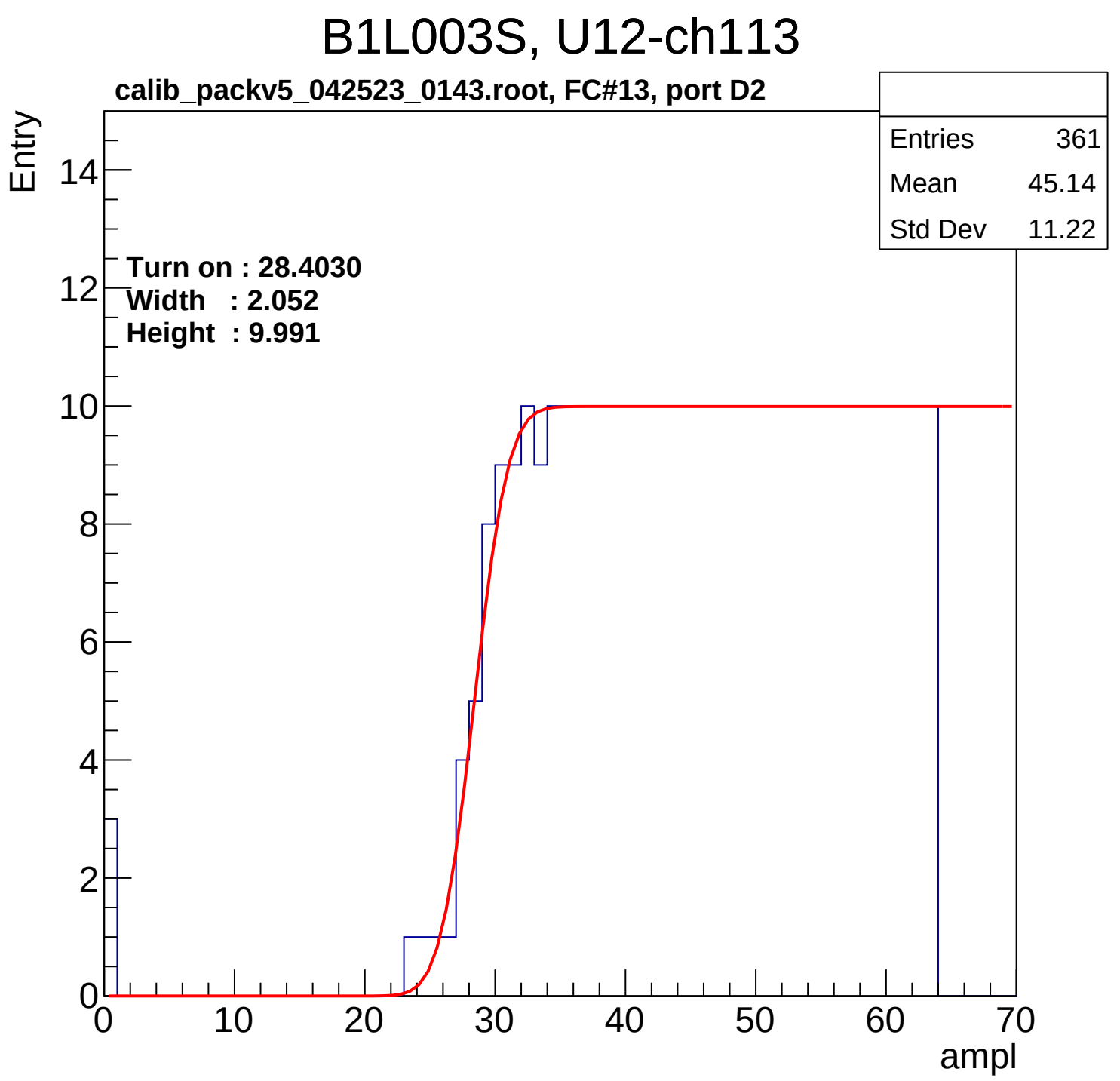

B1L003S, U12-ch108
calib_packv5_042523_0143.root, FC#13, port D2
Entries 370
Mean 44.77
Std Dev 11.23
Turn on : 27.5332
Width : 2.485
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

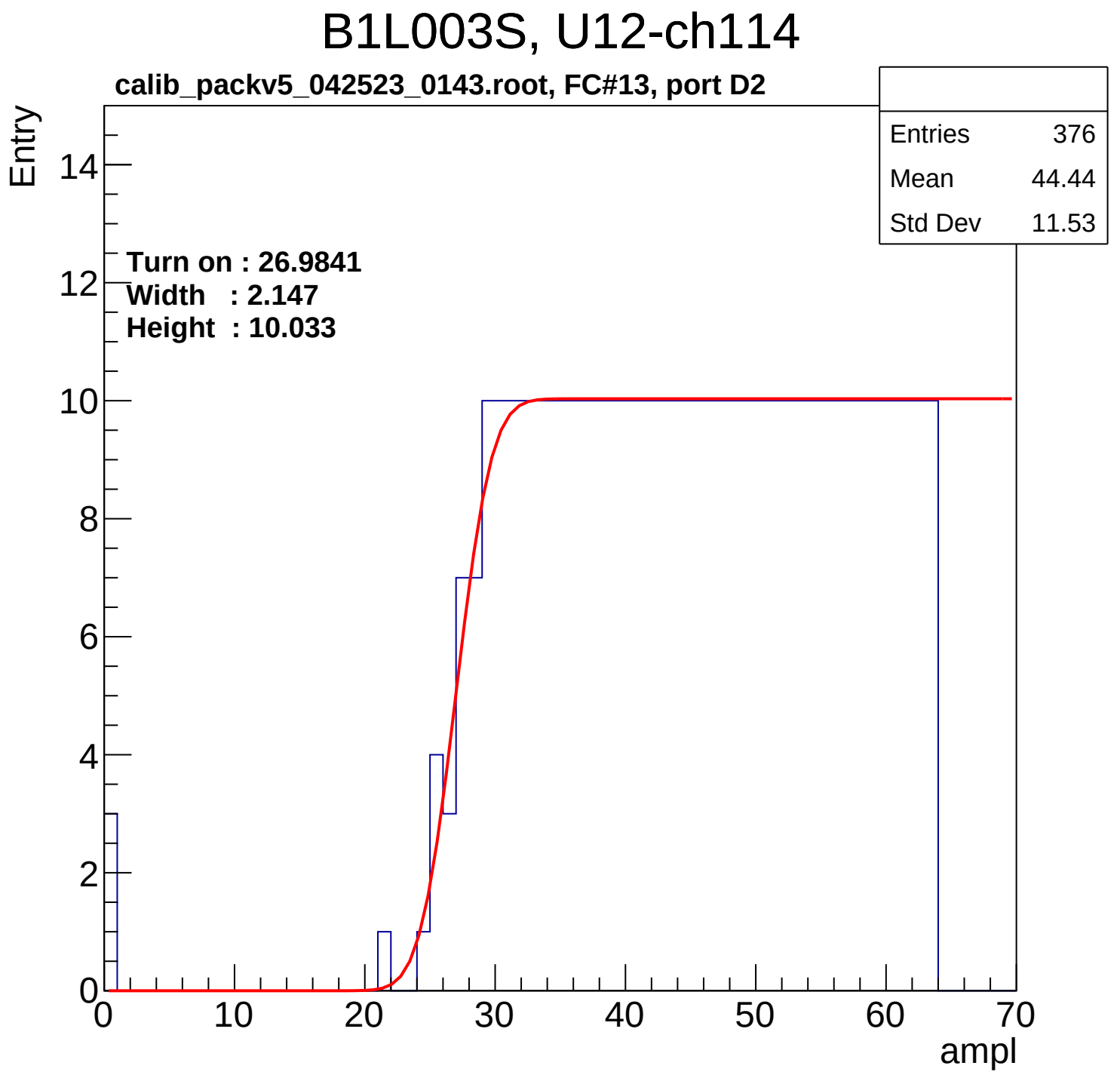

B1L003S, U12-ch109
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.82
Std Dev 11.01
Turn on : 27.0793
Width : 2.482
Height : 10.019
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

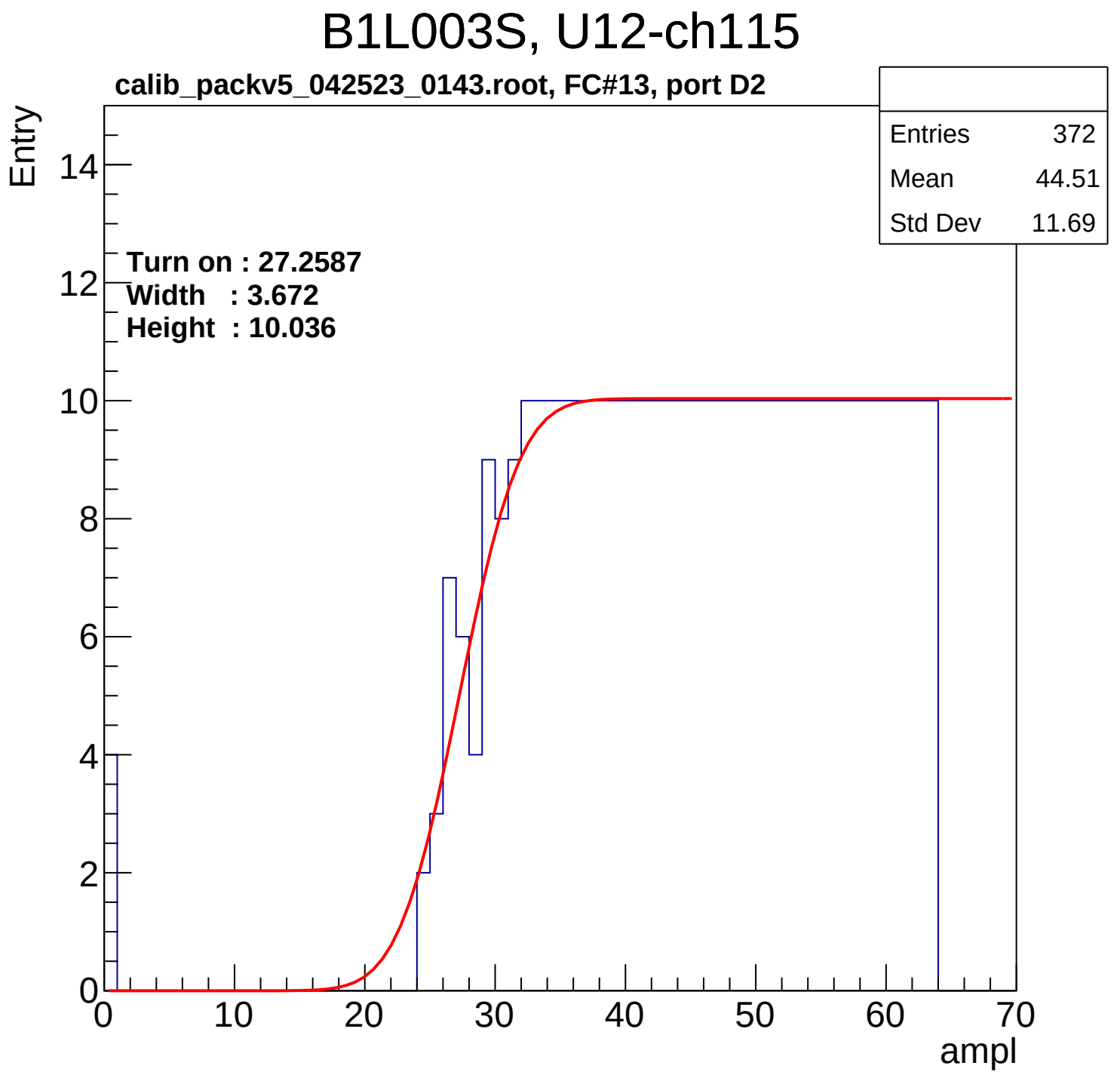

B1L003S, U12-ch110
calib_packv5_042523_0143.root, FC#13, port D2
Entries 360
Mean 45.07
Std Dev 11.46
Turn on : 28.4342
Width : 3.227
Height : 10.015
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

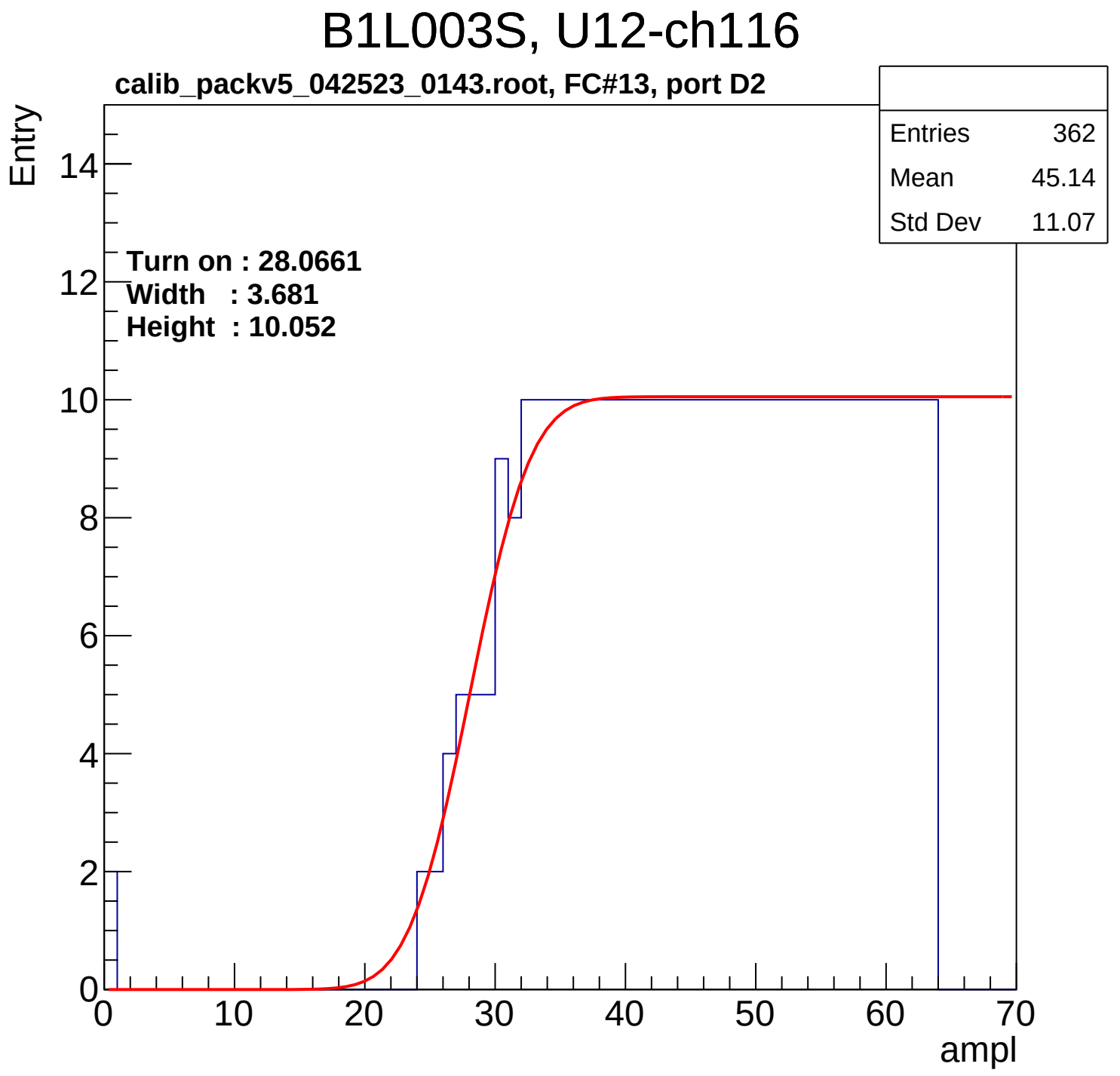

B1L003S, U12-ch111
calib_packv5_042523_0143.root, FC#13, port D2
Entries 356
Mean 45.47
Std Dev 10.77
Turn on : 29.1739
Width : 3.863
Height : 10.073
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

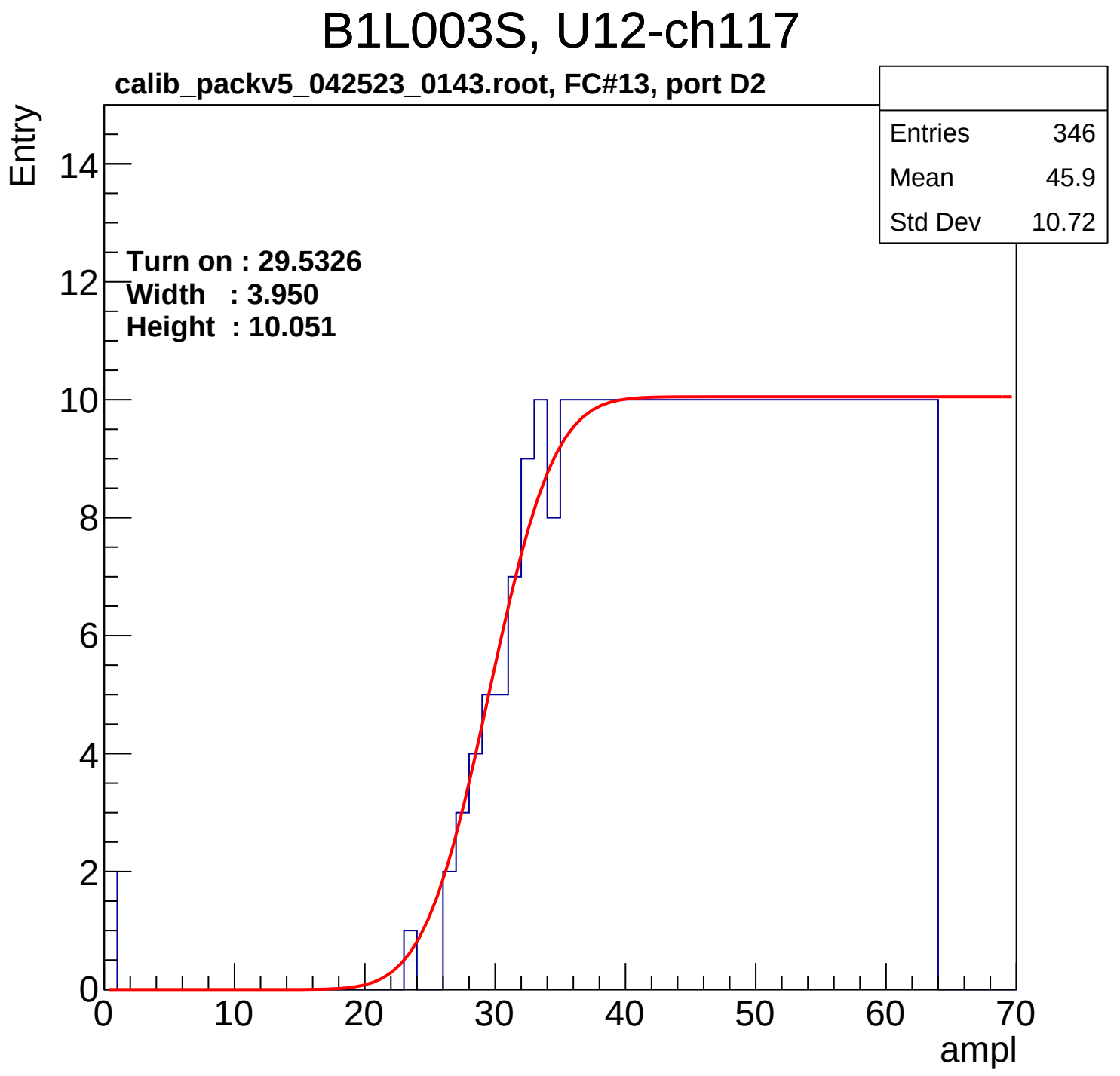

B1L003S, U12-ch112
calib_packv5_042523_0143.root, FC#13, port D2
Entries 380
Mean 44.17
Std Dev 11.8
Turn on : 26.5379
Width : 2.302
Height : 10.006
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

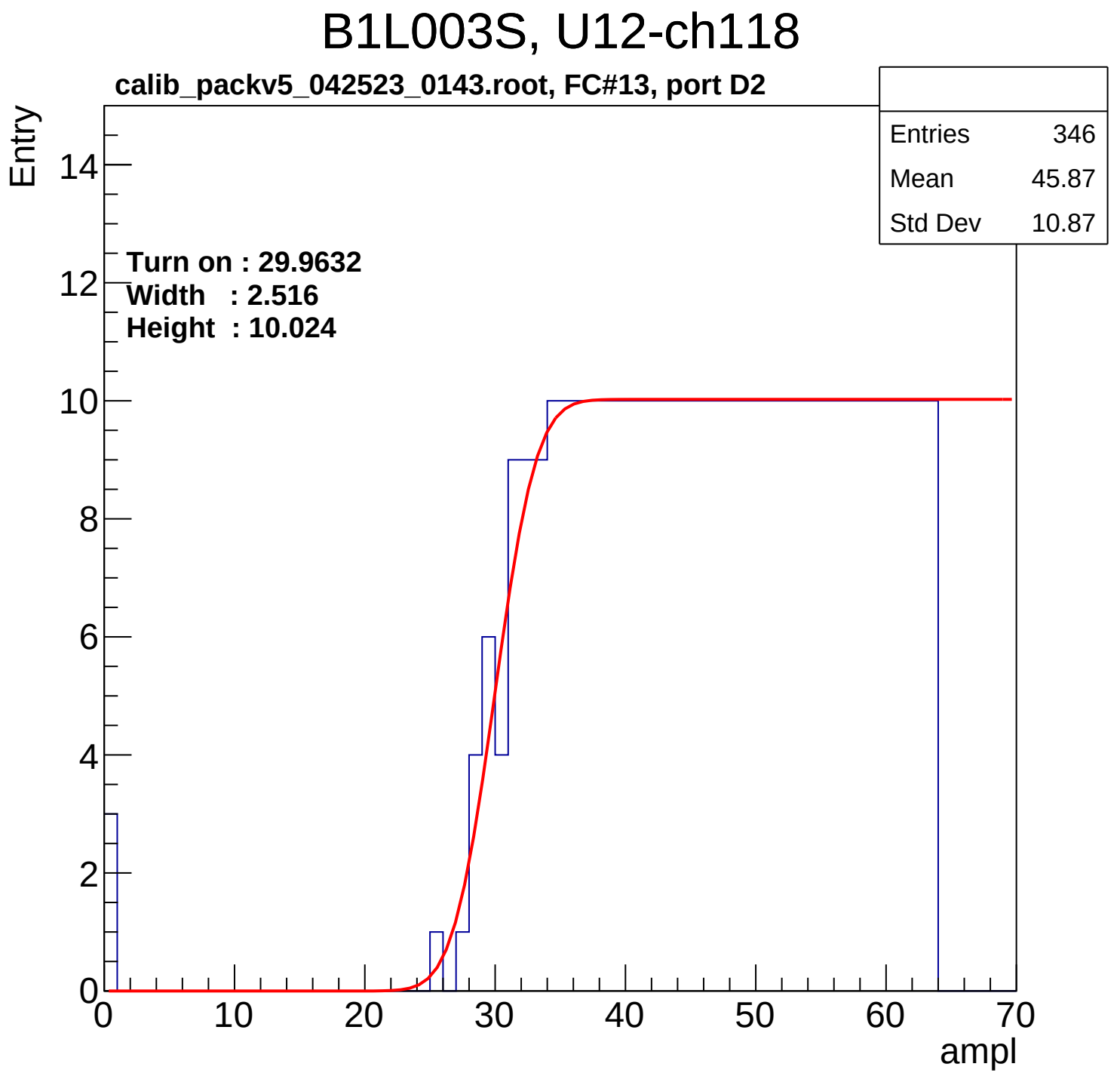

B1L003S, U12-ch113
calib_packv5_042523_0143.root, FC#13, port D2
Entries 361
Mean 45.14
Std Dev 11.22
Turn on : 28.4030
Width : 2.052
Height : 9.991
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

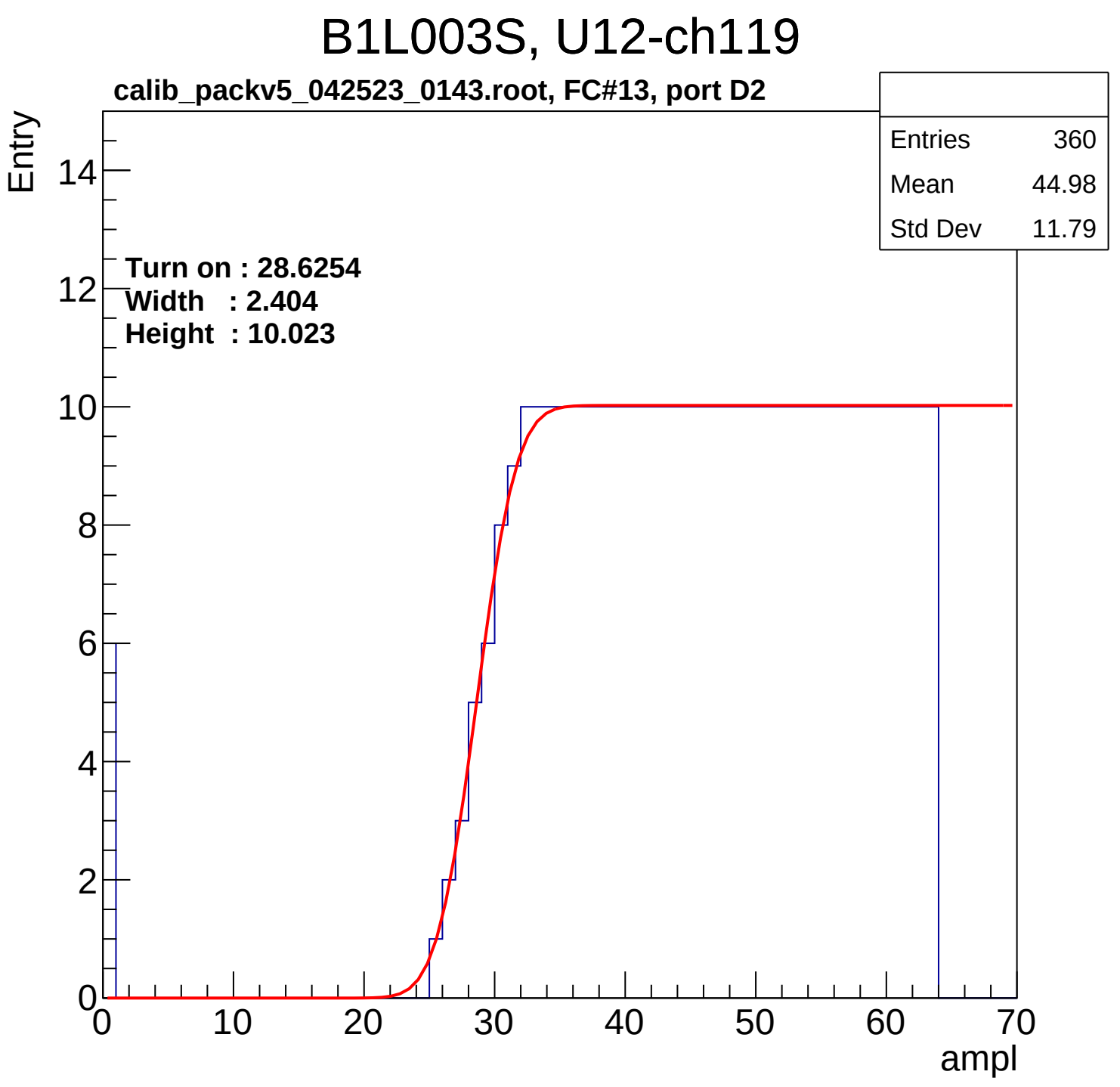

B1L003S, U12-ch114
calib_packv5_042523_0143.root, FC#13, port D2
Entries 376
Mean 44.44
Std Dev 11.53
Turn on : 26.9841
Width : 2.147
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

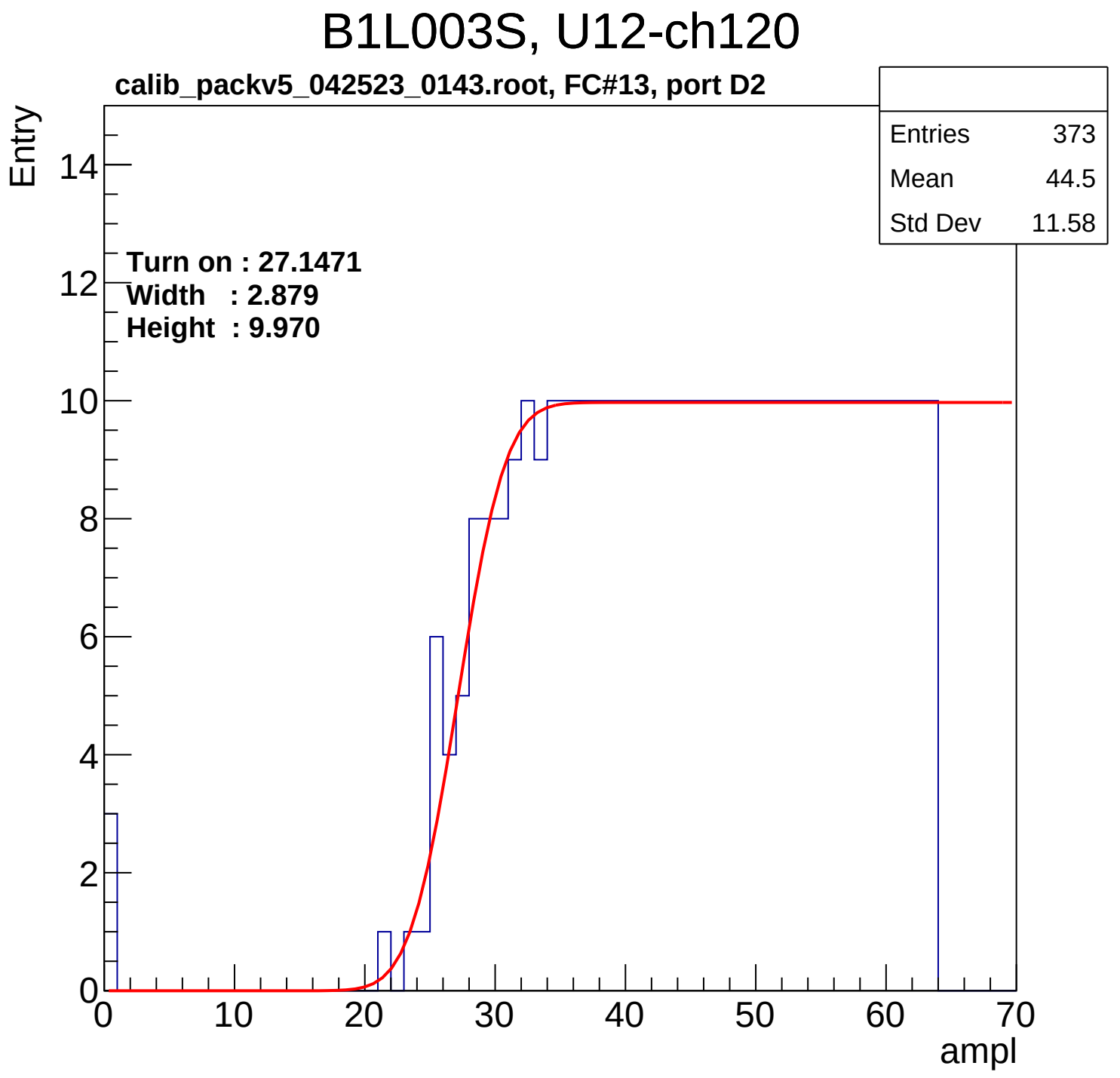

B1L003S, U12-ch115
calib_packv5_042523_0143.root, FC#13, port D2
Entries 372
Mean 44.51
Std Dev 11.69
Turn on : 27.2587
Width : 3.672
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

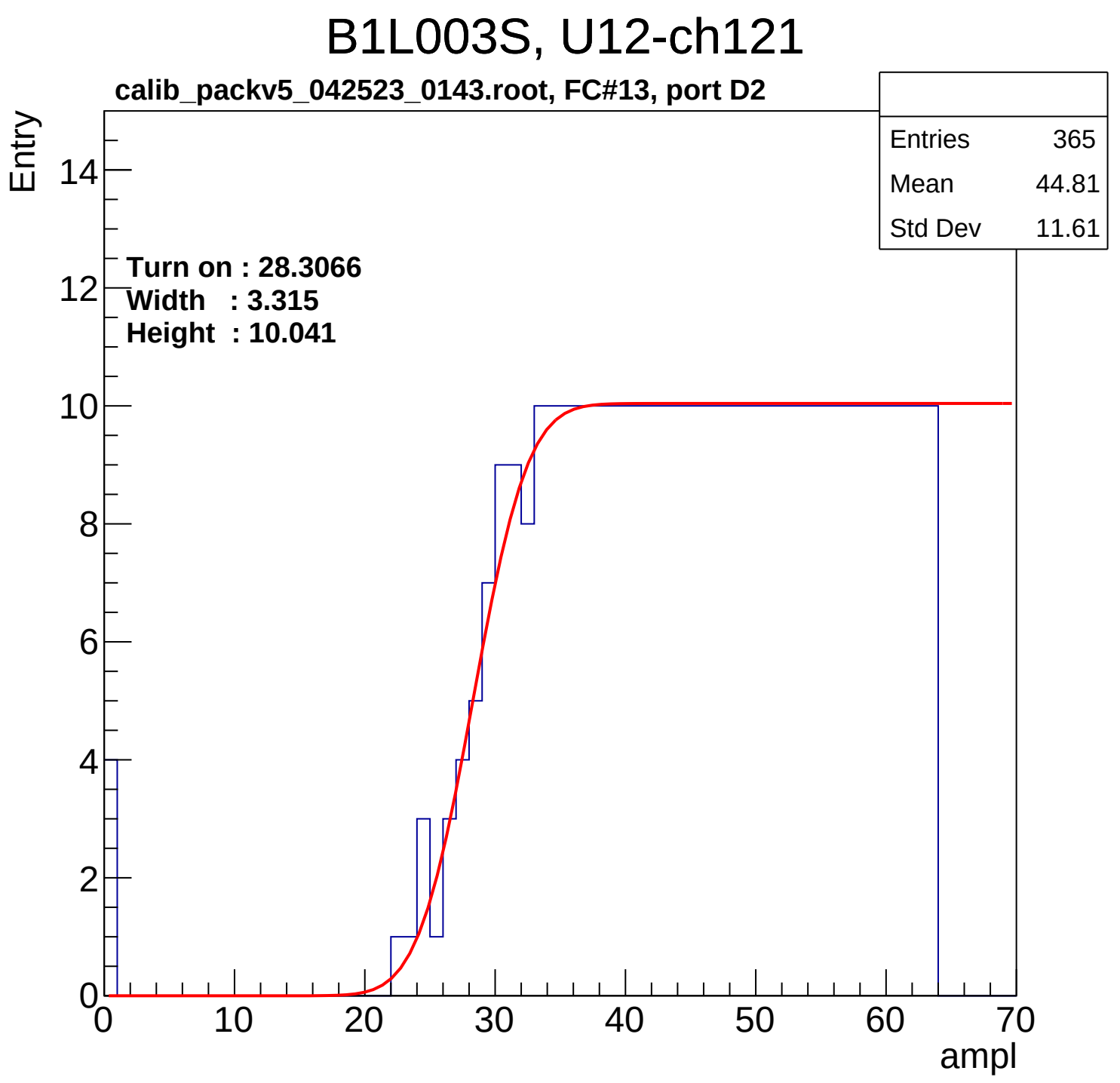

B1L003S, U12-ch116
calib_packv5_042523_0143.root, FC#13, port D2
Entries 362
Mean 45.14
Std Dev 11.07
Turn on : 28.0661
Width : 3.681
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

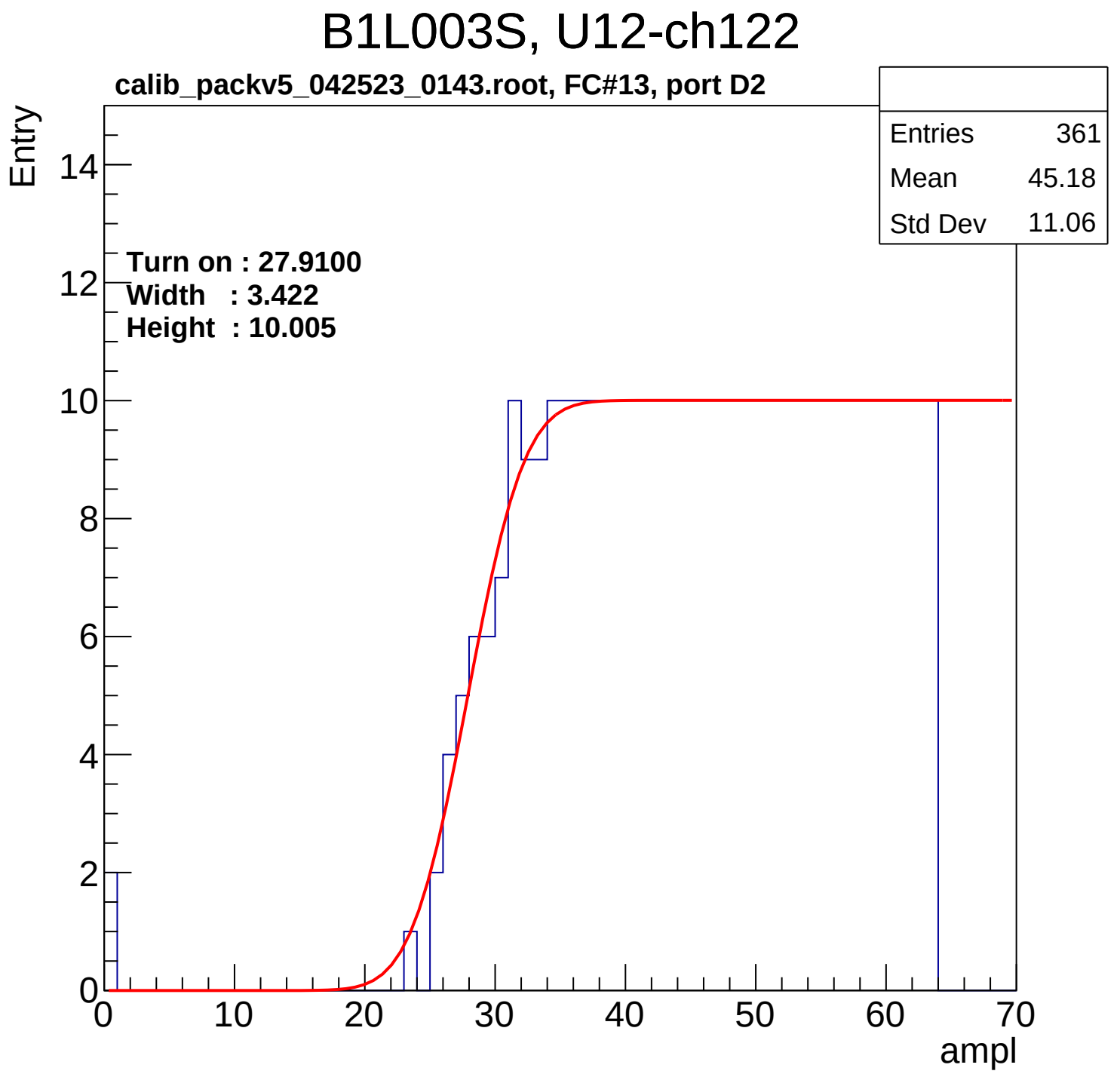

B1L003S, U12-ch117
calib_packv5_042523_0143.root, FC#13, port D2
Entries 346
Mean 45.9
Std Dev 10.72
Turn on : 29.5326
Width : 3.950
Height : 10.051
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

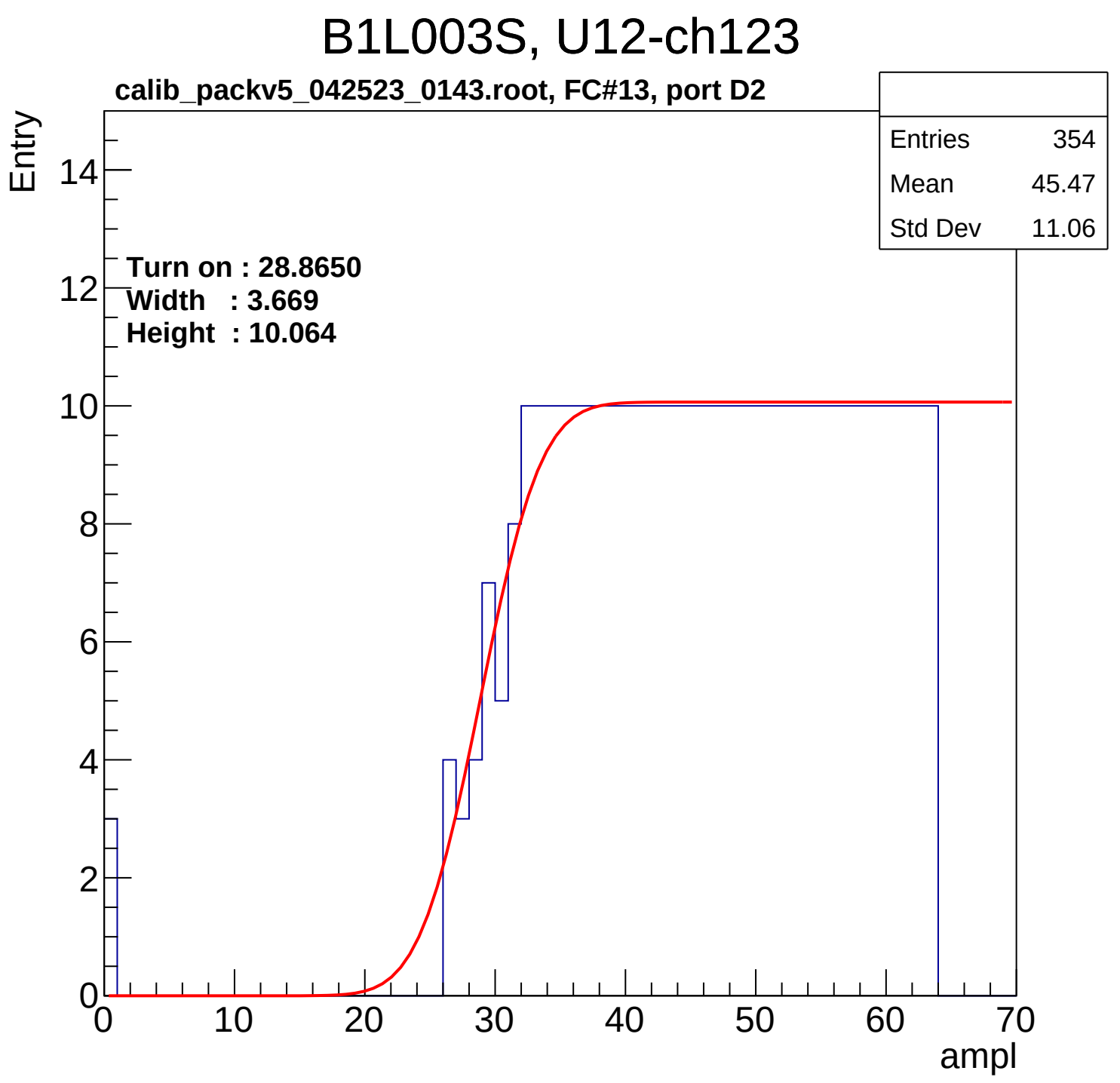

B1L003S, U12-ch118
calib_packv5_042523_0143.root, FC#13, port D2
Entries 346
Mean 45.87
Std Dev 10.87
Turn on : 29.9632
Width : 2.516
Height : 10.024
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

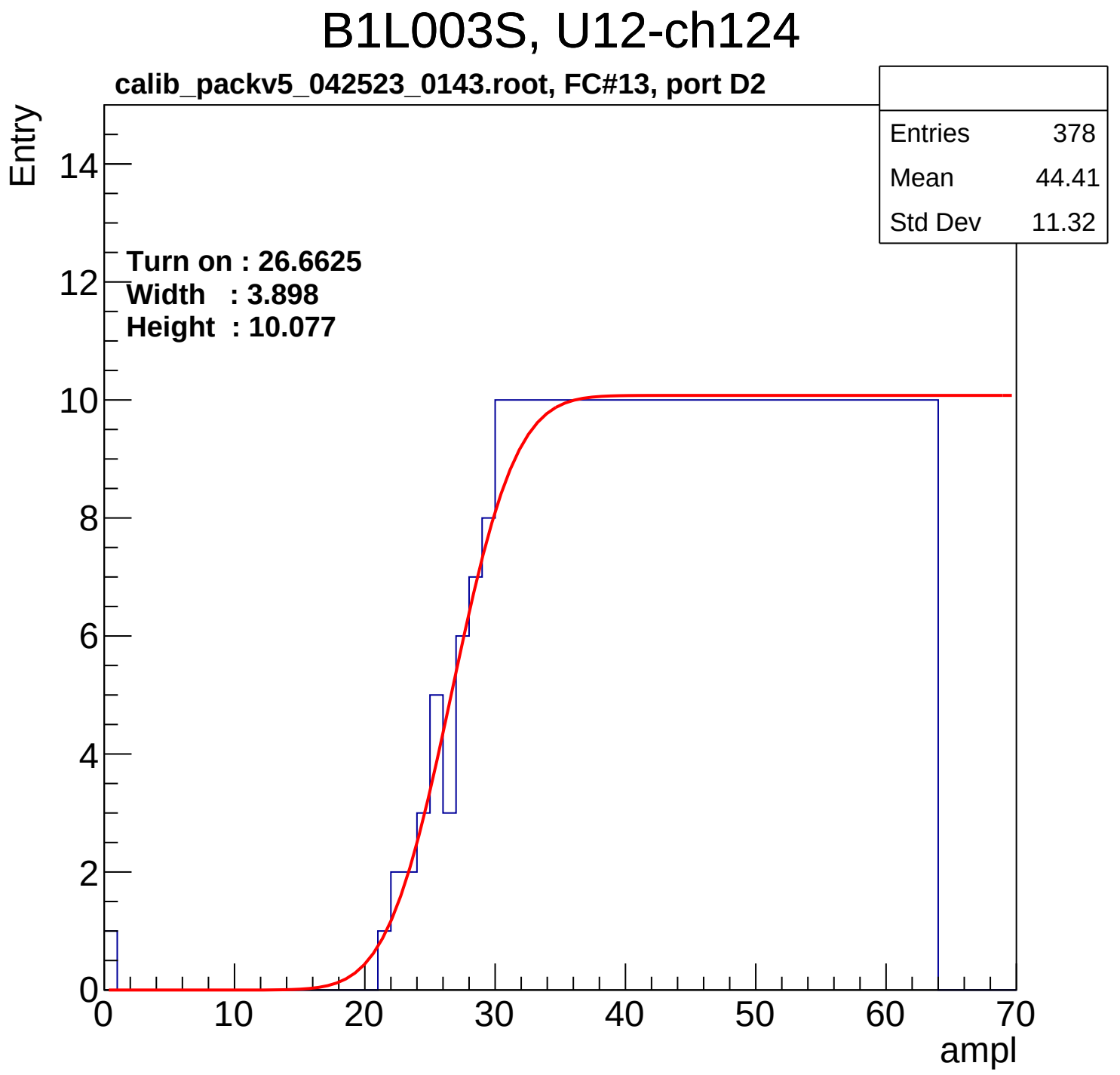

B1L003S, U12-ch119
calib_packv5_042523_0143.root, FC#13, port D2
Entries 360
Mean 44.98
Std Dev 11.79
Turn on : 28.6254
Width : 2.404
Height : 10.023
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

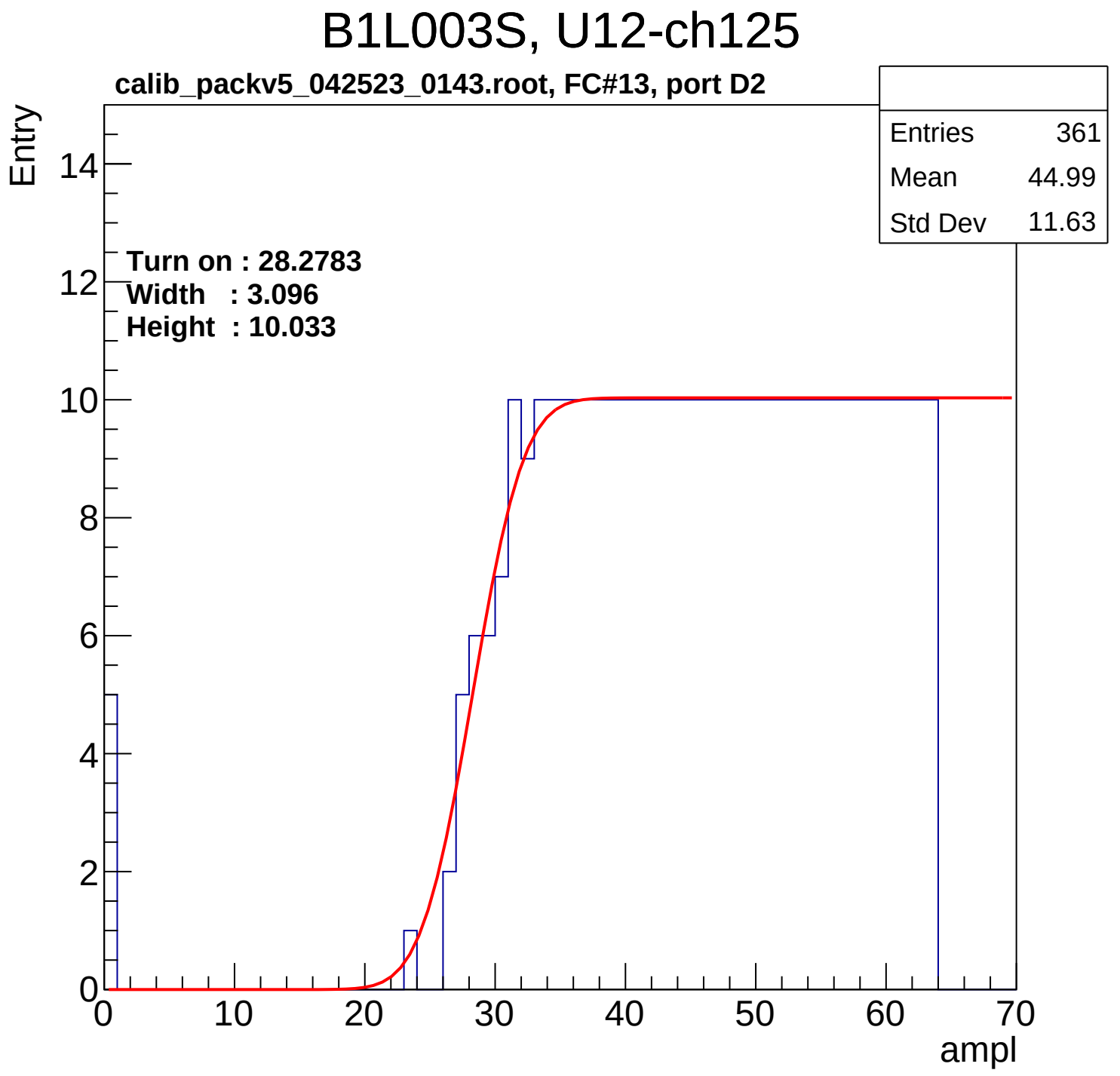

B1L003S, U12-ch120
calib_packv5_042523_0143.root, FC#13, port D2
Entries 373
Mean 44.5
Std Dev 11.58
Turn on : 27.1471
Width : 2.879
Height : 9.970
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

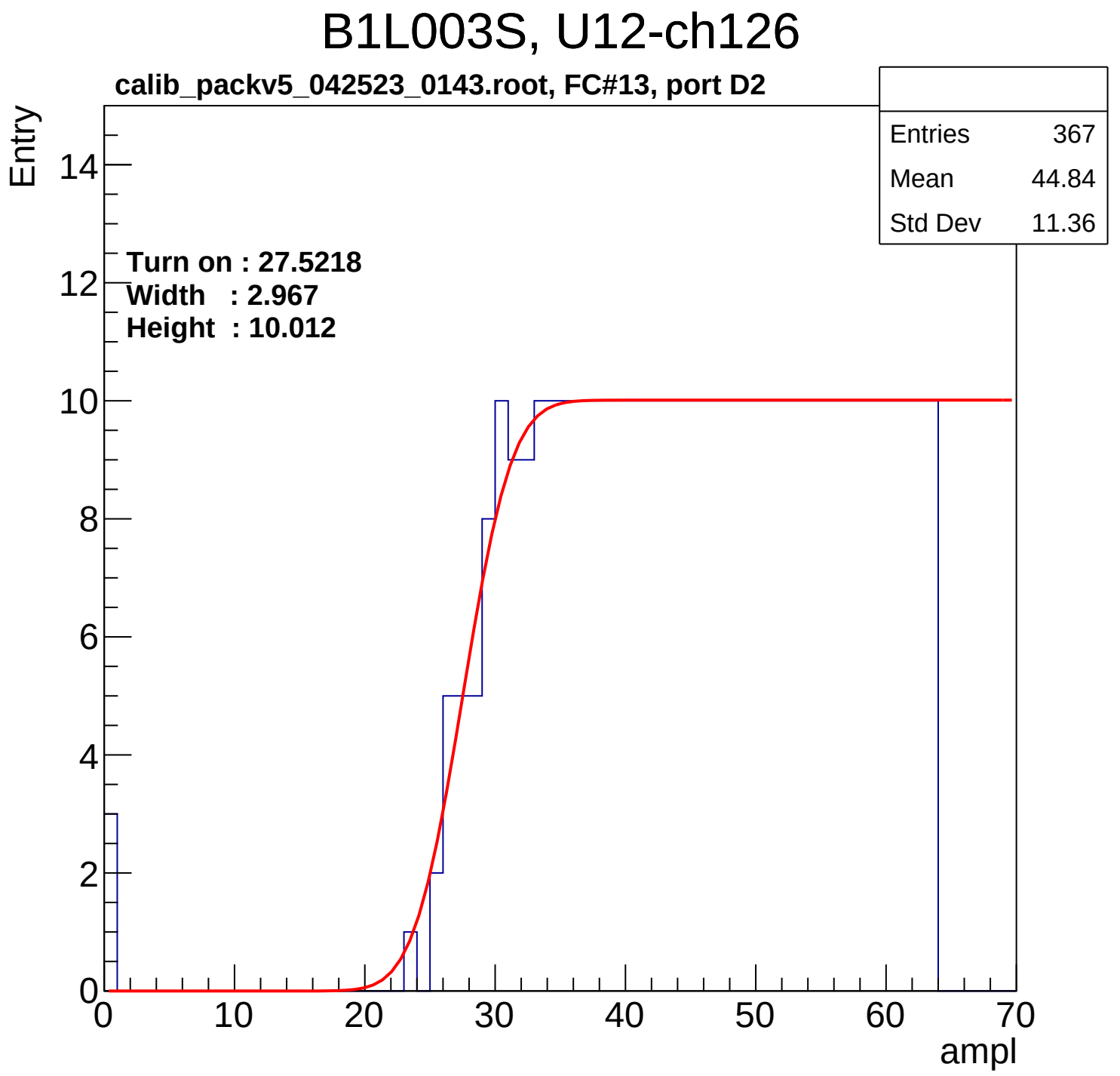

B1L003S, U12-ch121
calib_packv5_042523_0143.root, FC#13, port D2
Entries 365
Mean 44.81
Std Dev 11.61
Turn on : 28.3066
Width : 3.315
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

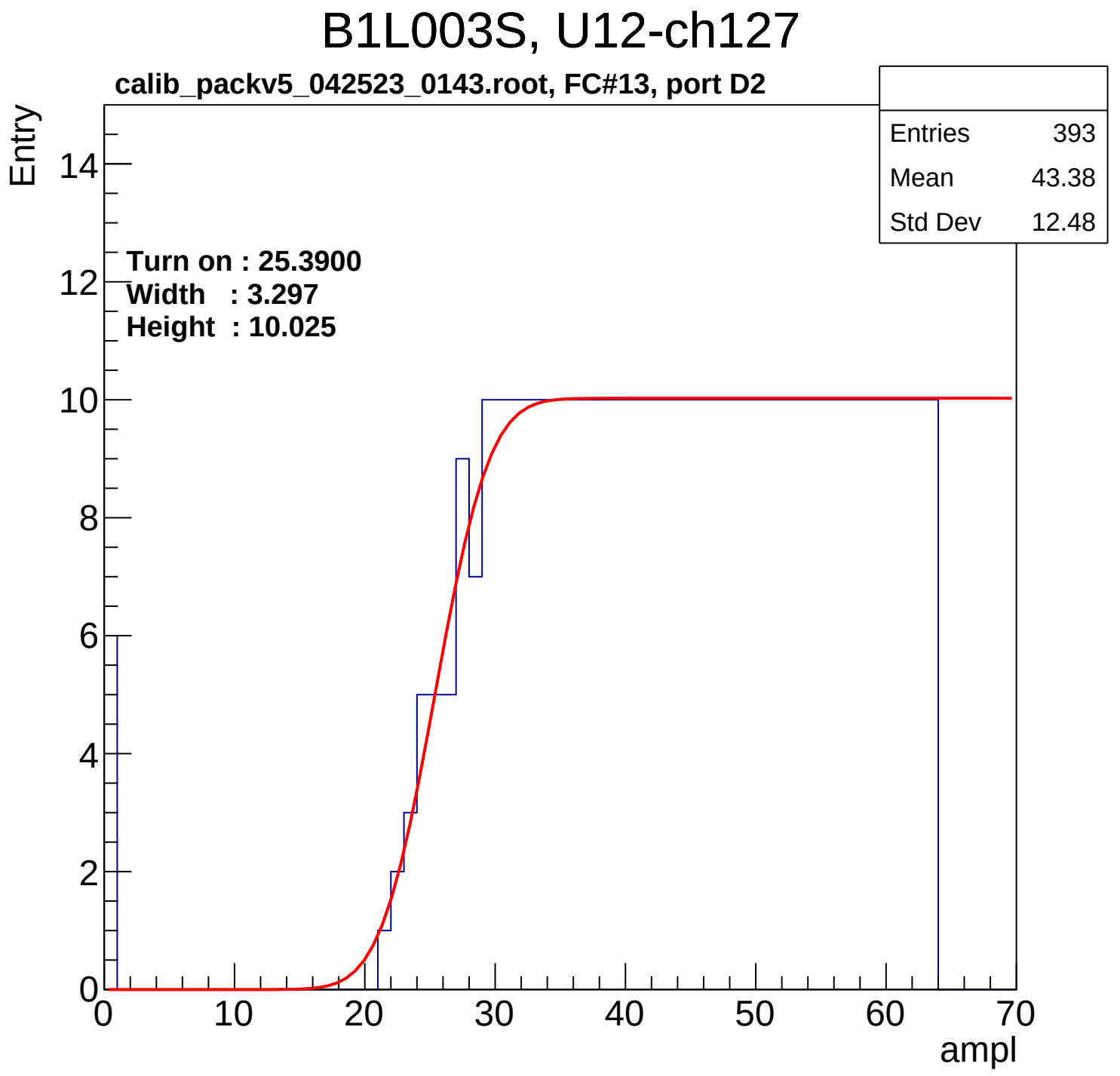

B1L003S, U12-ch122
calib_packv5_042523_0143.root, FC#13, port D2
Entries 361
Mean 45.18
Std Dev 11.06
Turn on : 27.9100
Width : 3.422
Height : 10.005
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

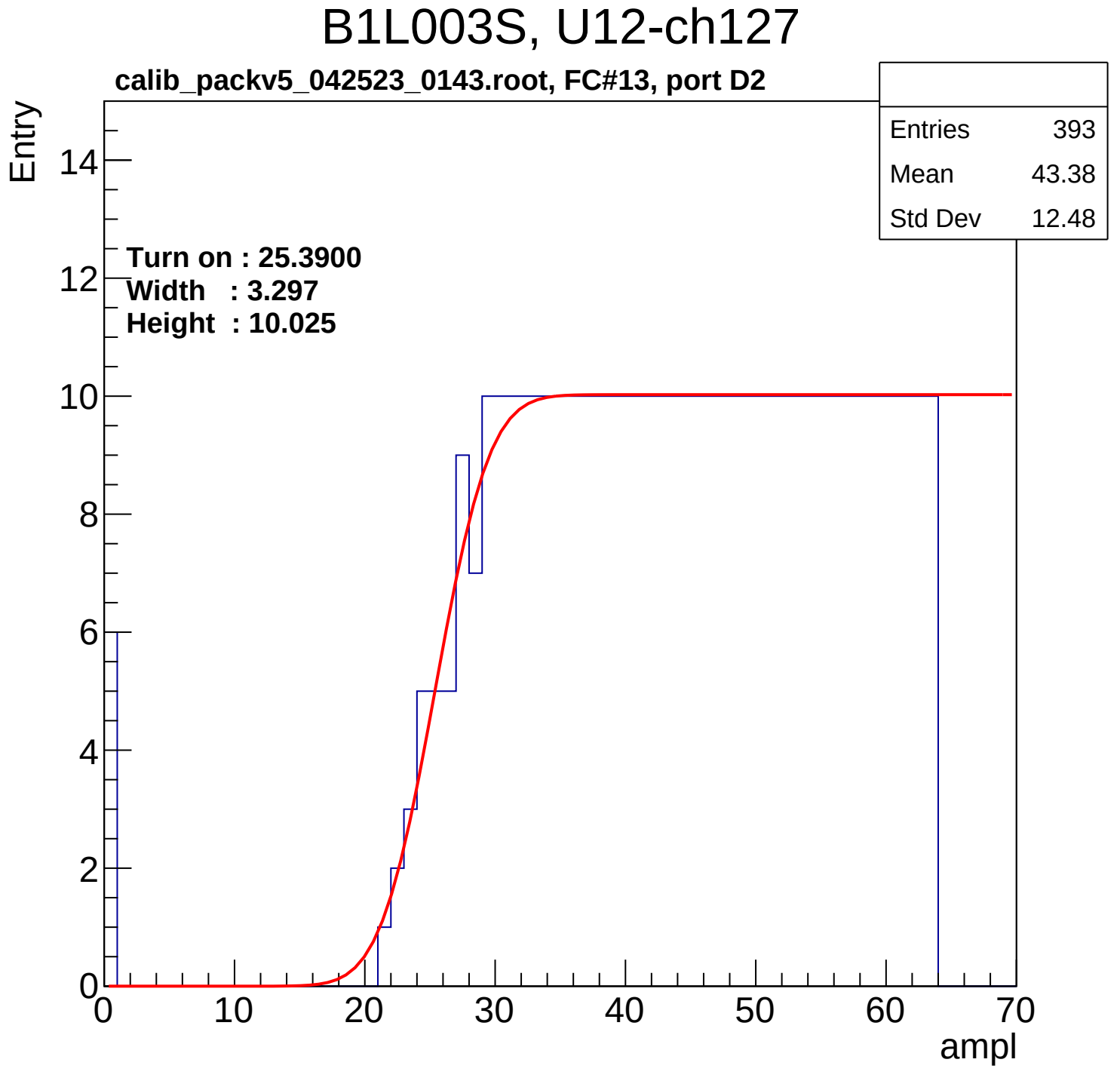

B1L003S, U12-ch123
calib_packv5_042523_0143.root, FC#13, port D2
Entries 354
Mean 45.47
Std Dev 11.06
Turn on : 28.8650
Width : 3.669
Height : 10.064
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U12-ch124
calib_packv5_042523_0143.root, FC#13, port D2
Entries 378
Mean 44.41
Std Dev 11.32
Turn on : 26.6625
Width : 3.898
Height : 10.077
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U12-ch125
calib_packv5_042523_0143.root, FC#13, port D2
Entries 361
Mean 44.99
Std Dev 11.63
Turn on : 28.2783
Width : 3.096
Height : 10.033
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U12-ch126
calib_packv5_042523_0143.root, FC#13, port D2
Entries 367
Mean 44.84
Std Dev 11.36
Turn on : 27.5218
Width : 2.967
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U12-ch127
calib_packv5_042523_0143.root, FC#13, port D2
Entries 393
Mean 43.38
Std Dev 12.48
Turn on : 25.3900
Width : 3.297
Height : 10.025
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U12-ch127
calib_packv5_042523_0143.root, FC#13, port D2
Entries 393
Mean 43.38
Std Dev 12.48
Turn on : 25.3900
Width : 3.297
Height : 10.025
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70