



# B0L001S, U21-ch0, adc0

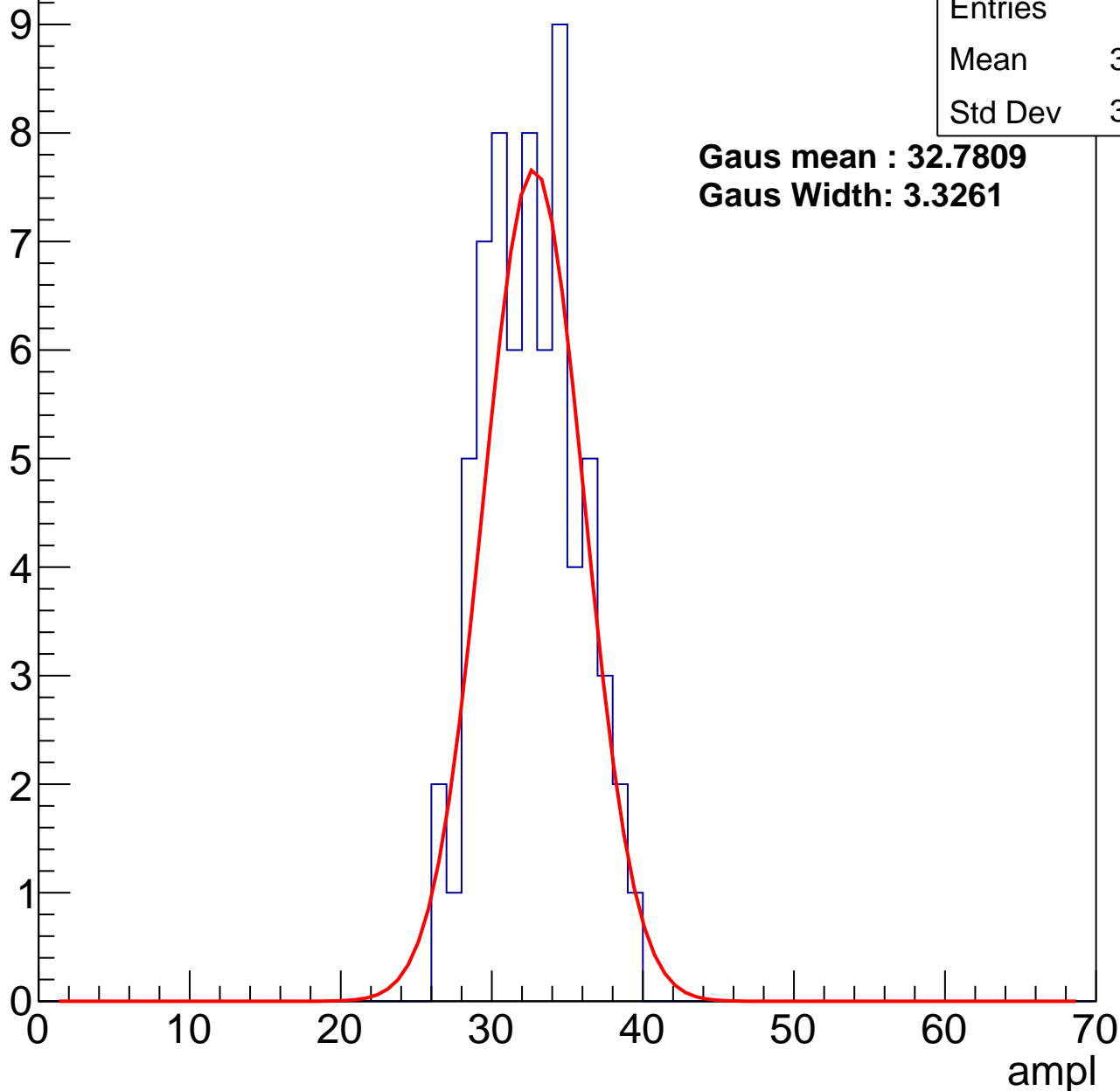
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	32.15
Std Dev	3.068

**Gaus mean : 32.7809**

**Gaus Width: 3.3261**



# B0L001S, U21-ch0, adc1

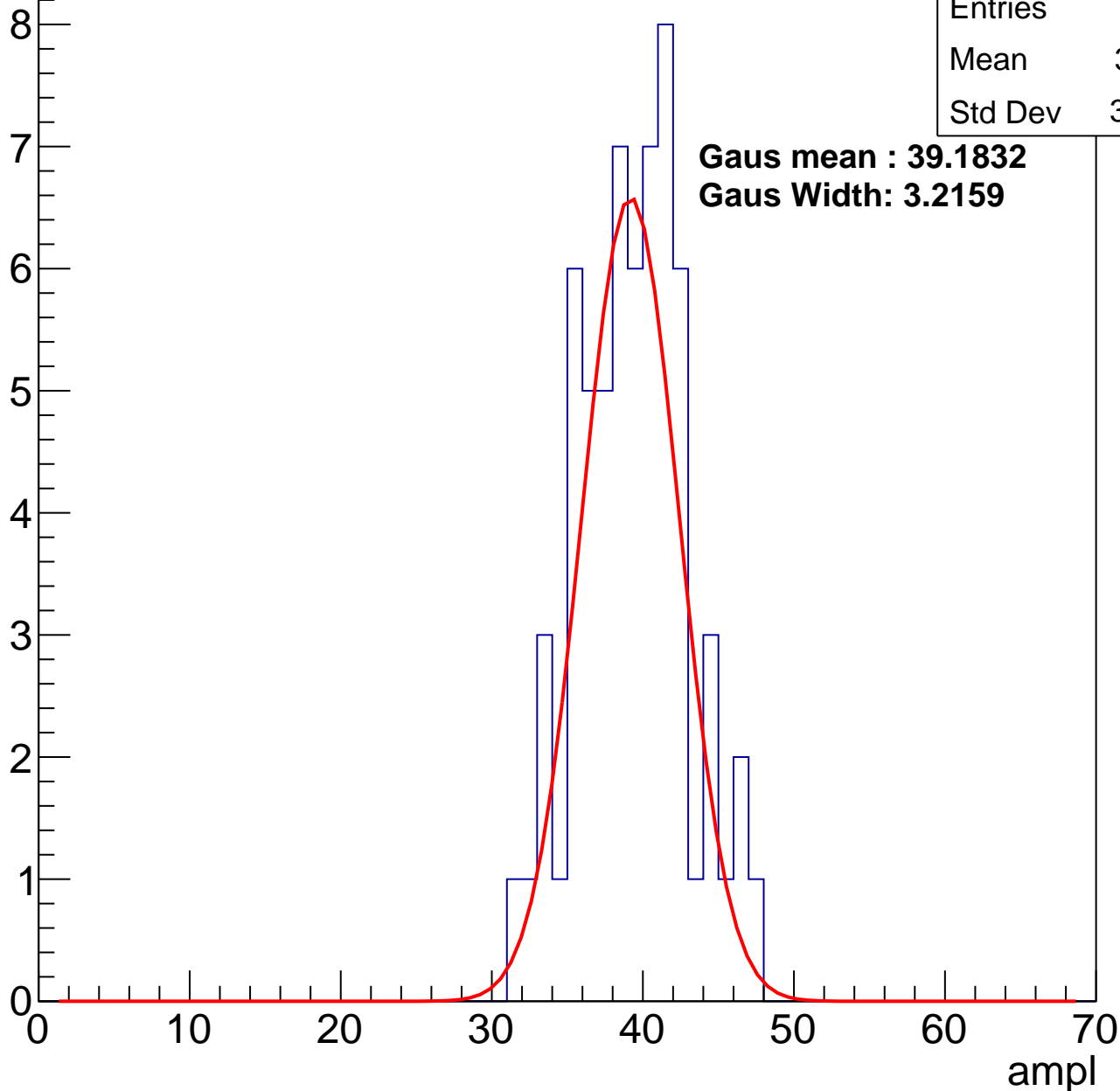
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	38.91
Std Dev	3.525

**Gaus mean : 39.1832**

**Gaus Width: 3.2159**



# B0L001S, U21-ch0, adc2

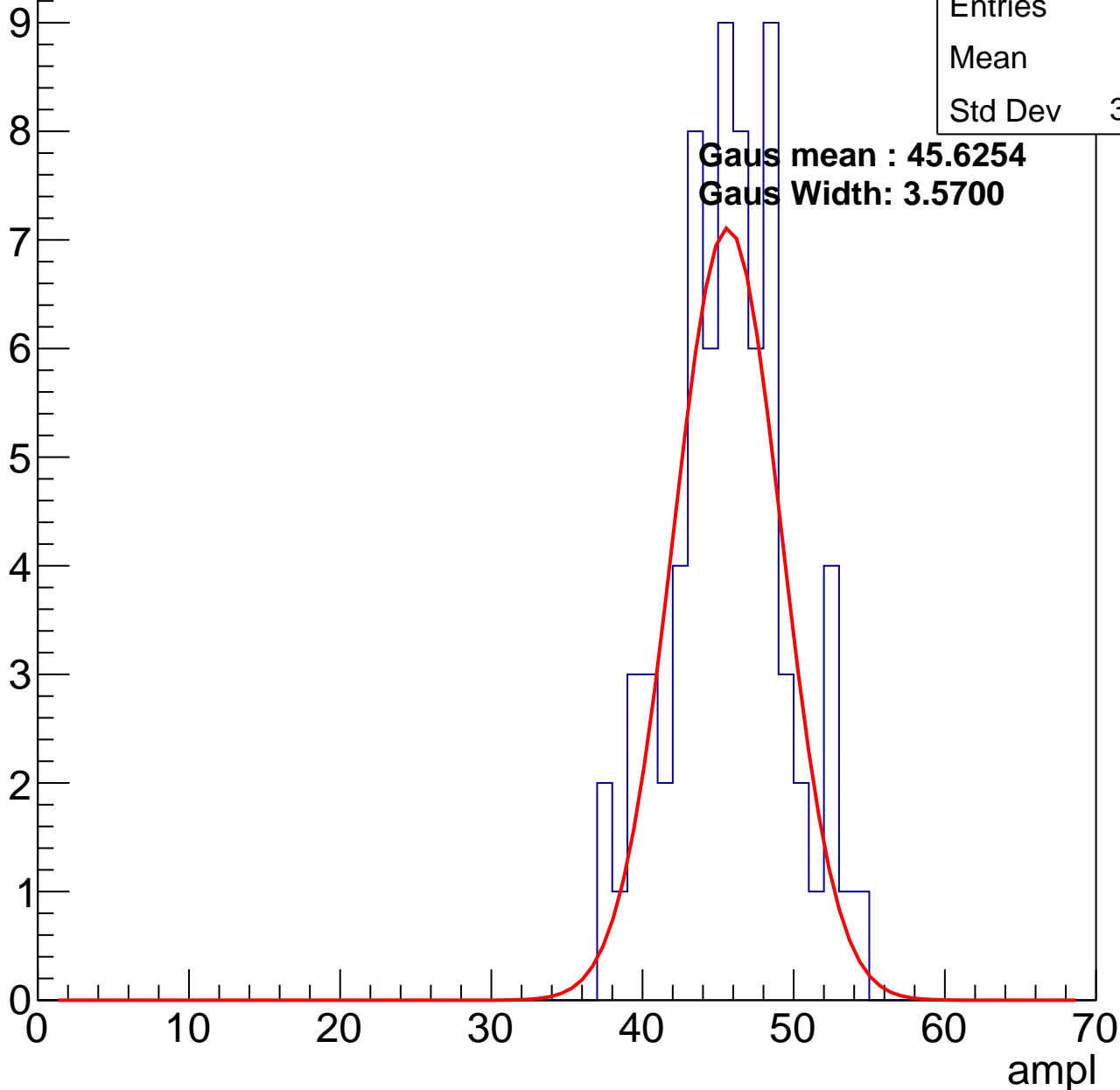
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	45.3
Std Dev	3.788

**Gaus mean : 45.6254**

**Gaus Width: 3.5700**

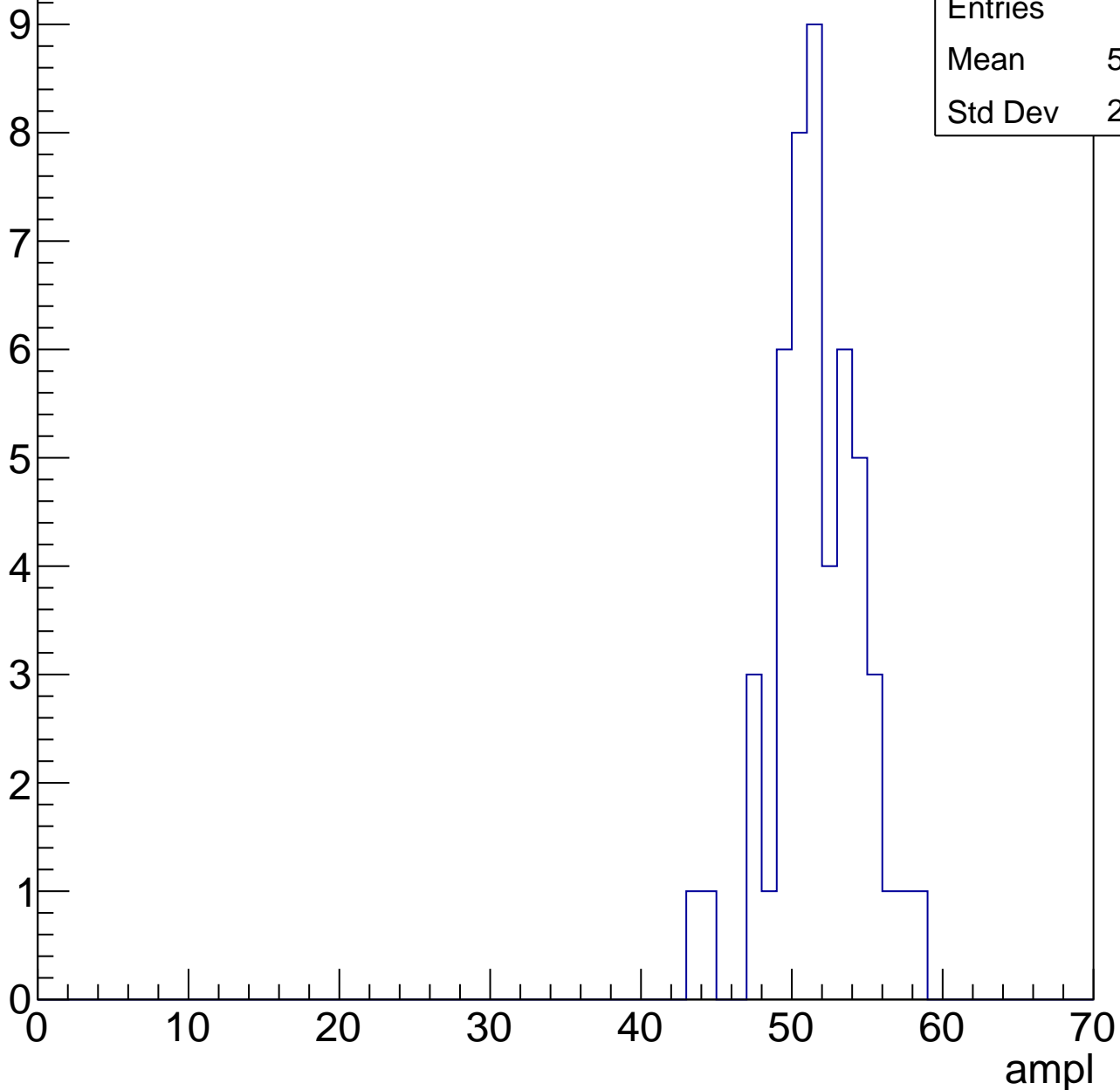


# B0L001S, U21-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	51.22
Std Dev	2.935

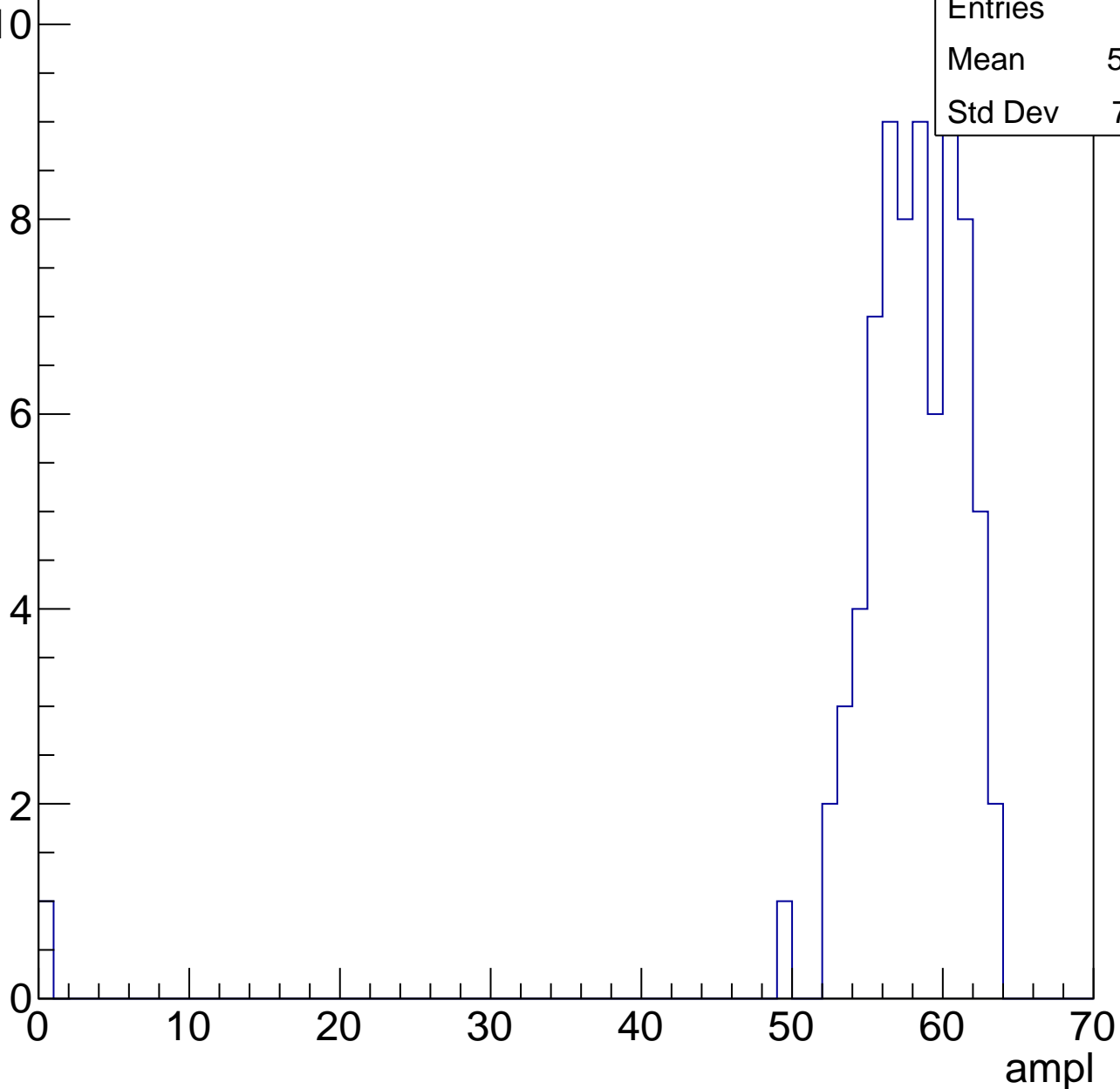


# B0L001S, U21-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	56.97
Std Dev	7.241

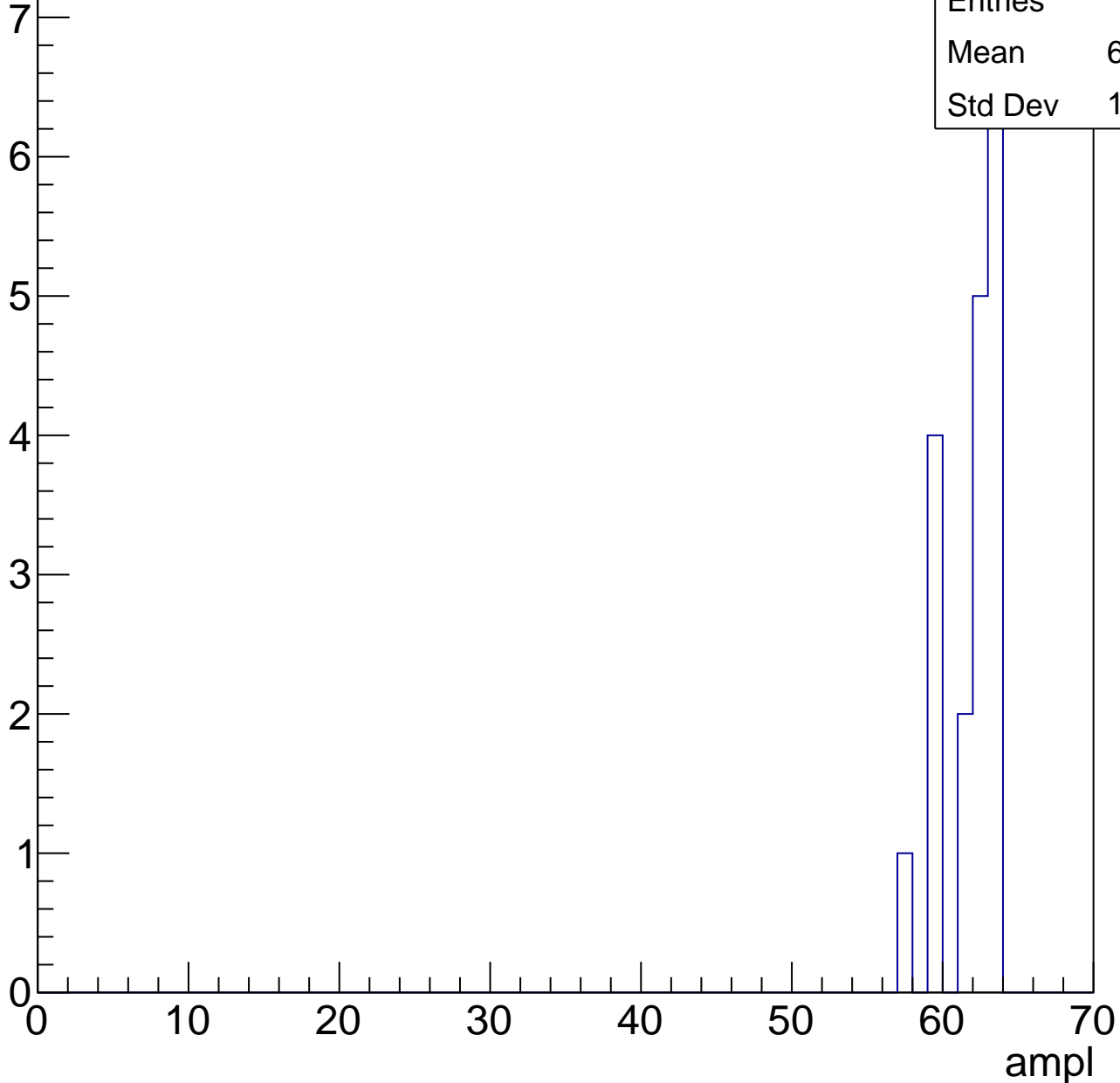


# B0L001S, U21-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	19
Mean	61.37
Std Dev	1.813



# B0L001S, U21-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U21-ch1, adc0

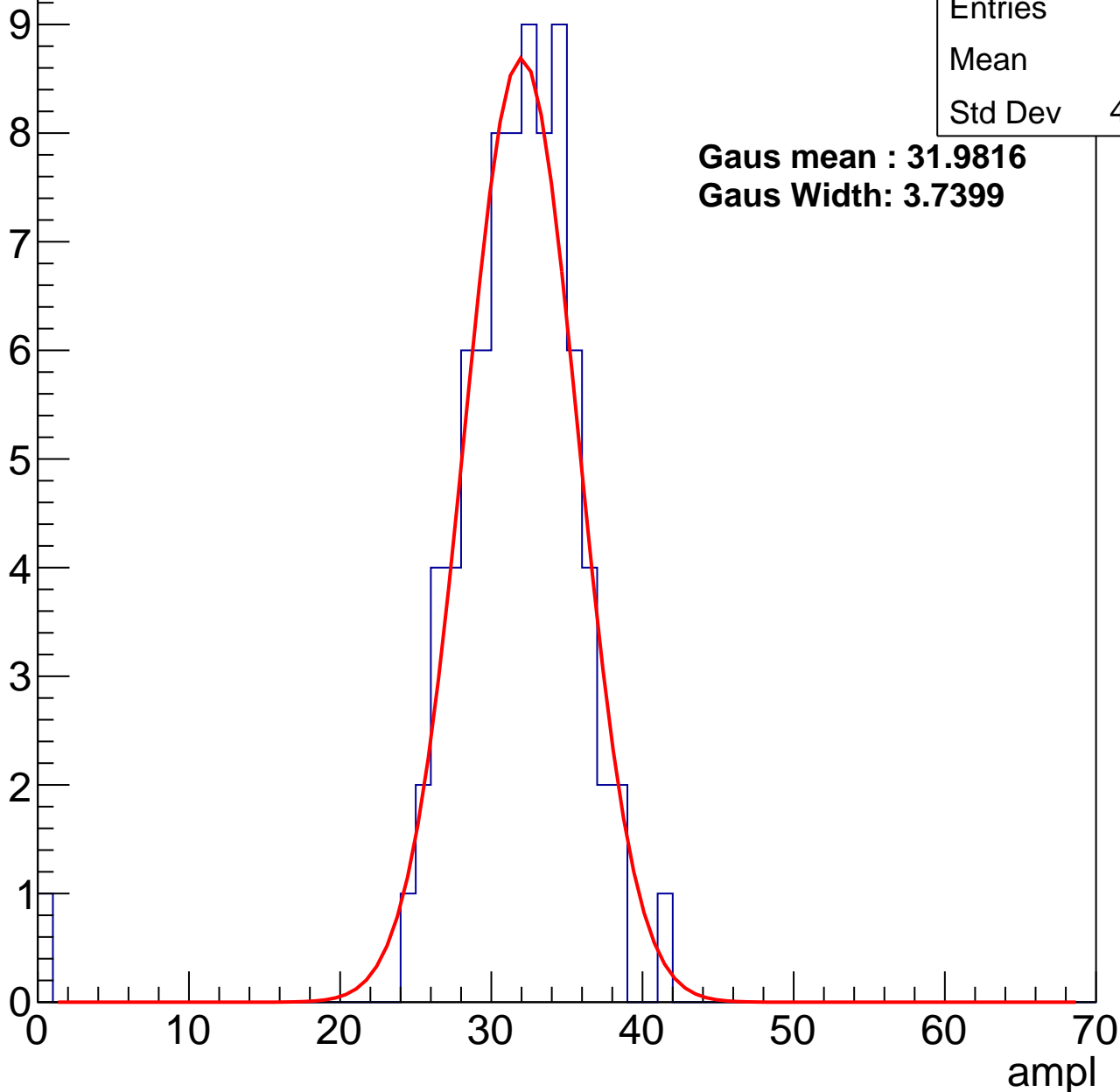
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	31.1
Std Dev	4.868

**Gaus mean : 31.9816**

**Gaus Width: 3.7399**



# B0L001S, U21-ch1, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	67
Mean	38.82
Std Dev	3.255

**Gaus mean : 38.8936**

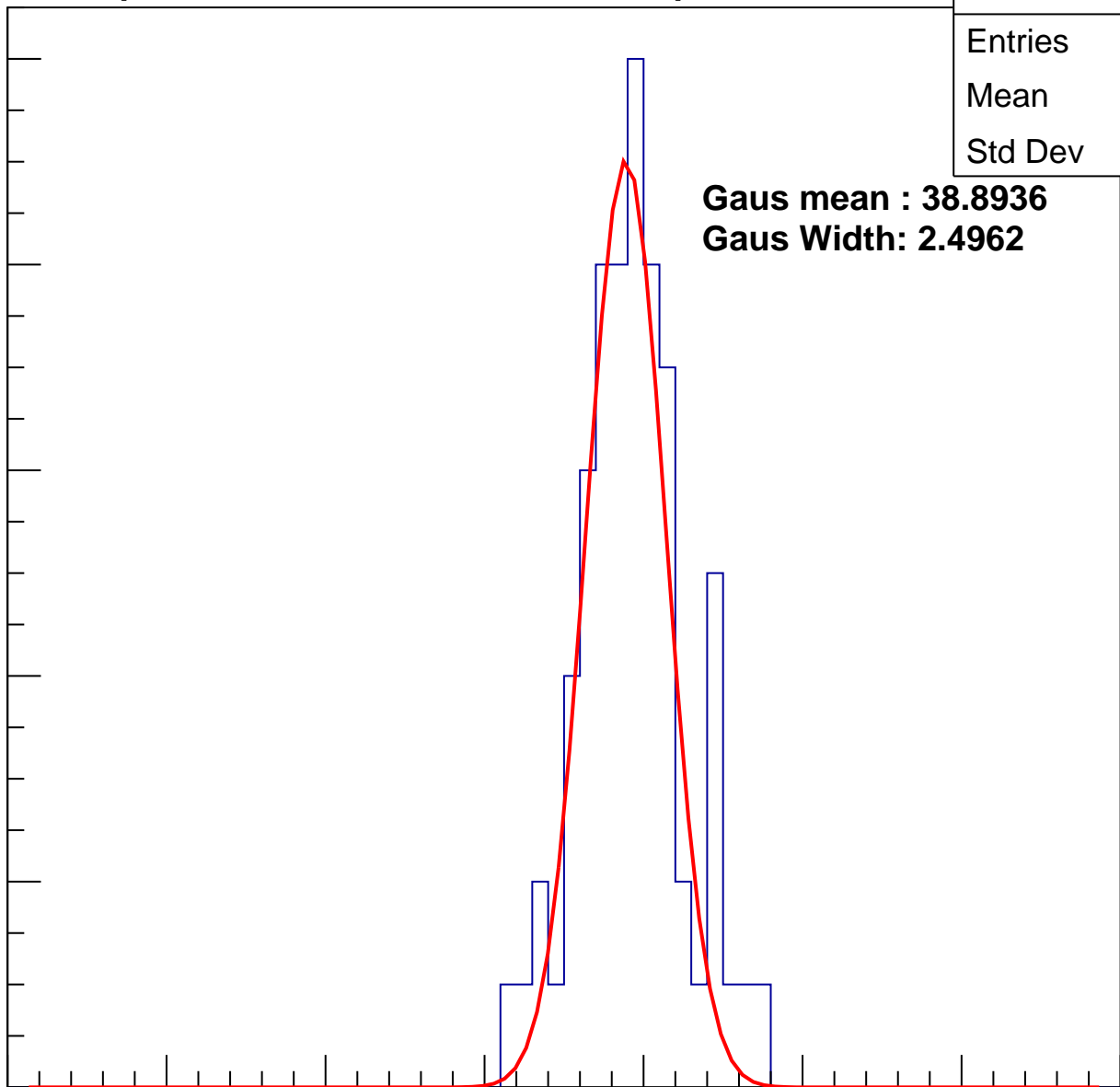
**Gaus Width: 2.4962**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U21-ch1, adc2

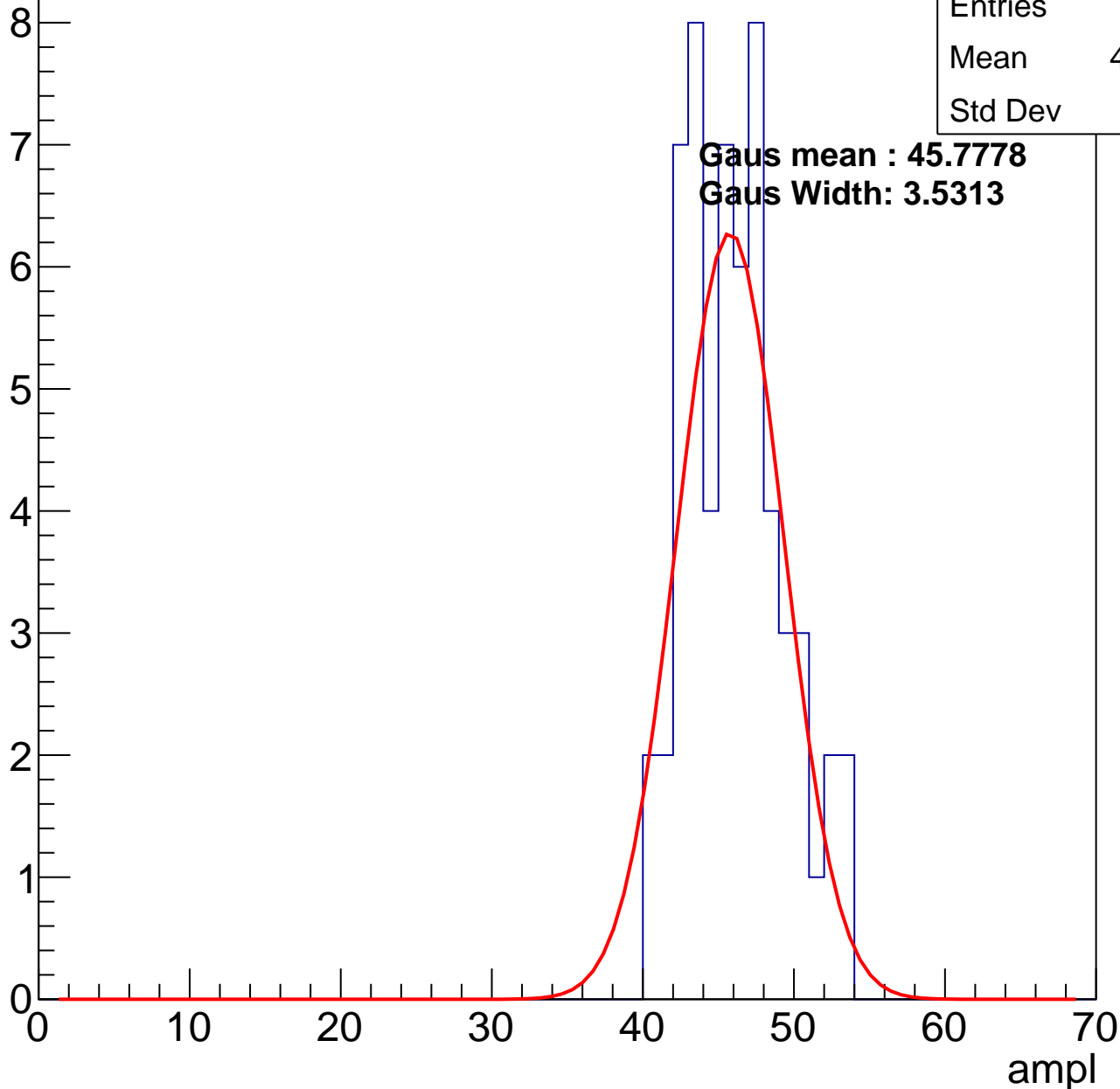
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	45.64
Std Dev	3.23

**Gaus mean : 45.7778**

**Gaus Width: 3.5313**

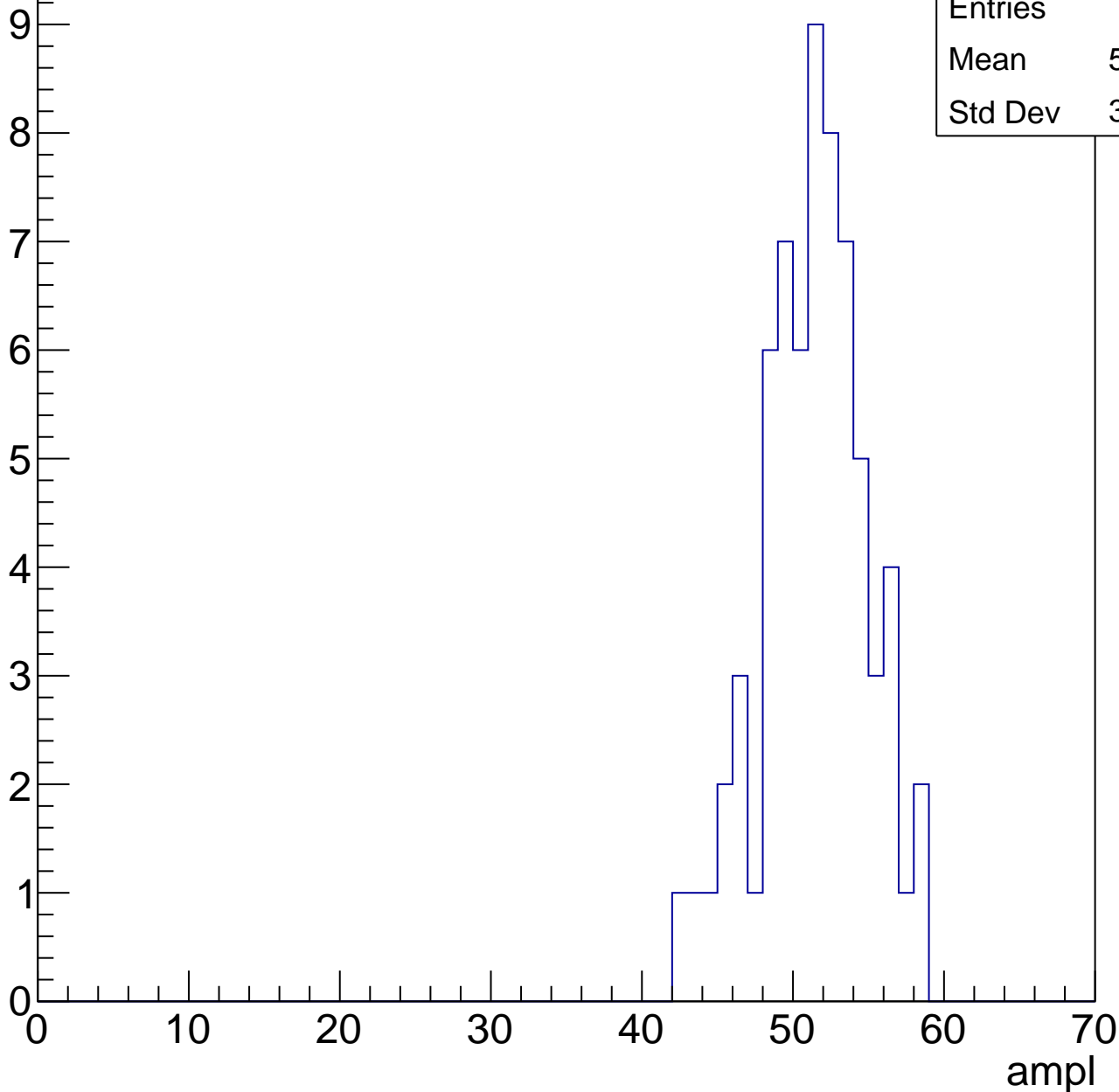


# B0L001S, U21-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

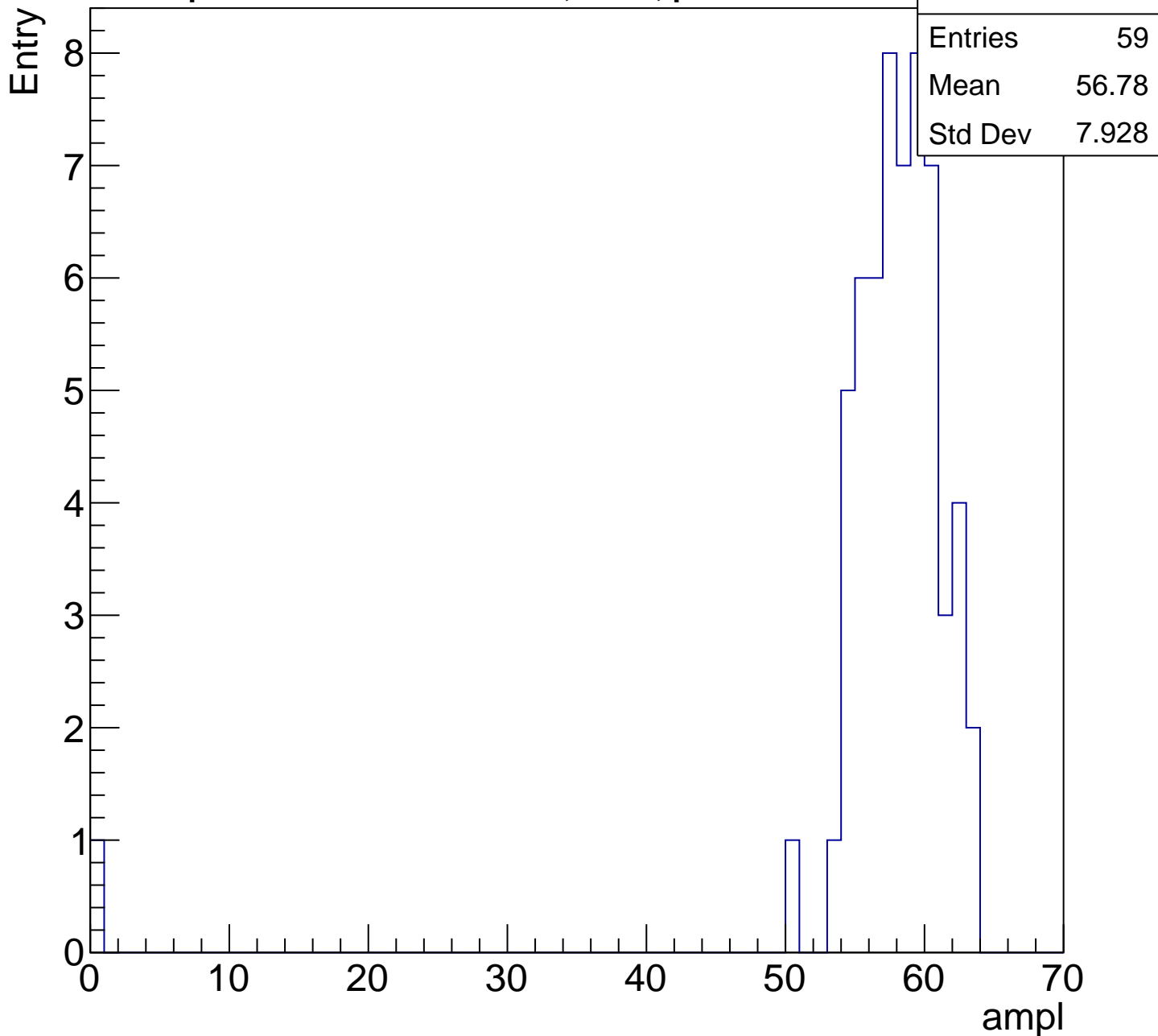
Entry

Entries	67
Mean	50.94
Std Dev	3.472



# B0L001S, U21-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

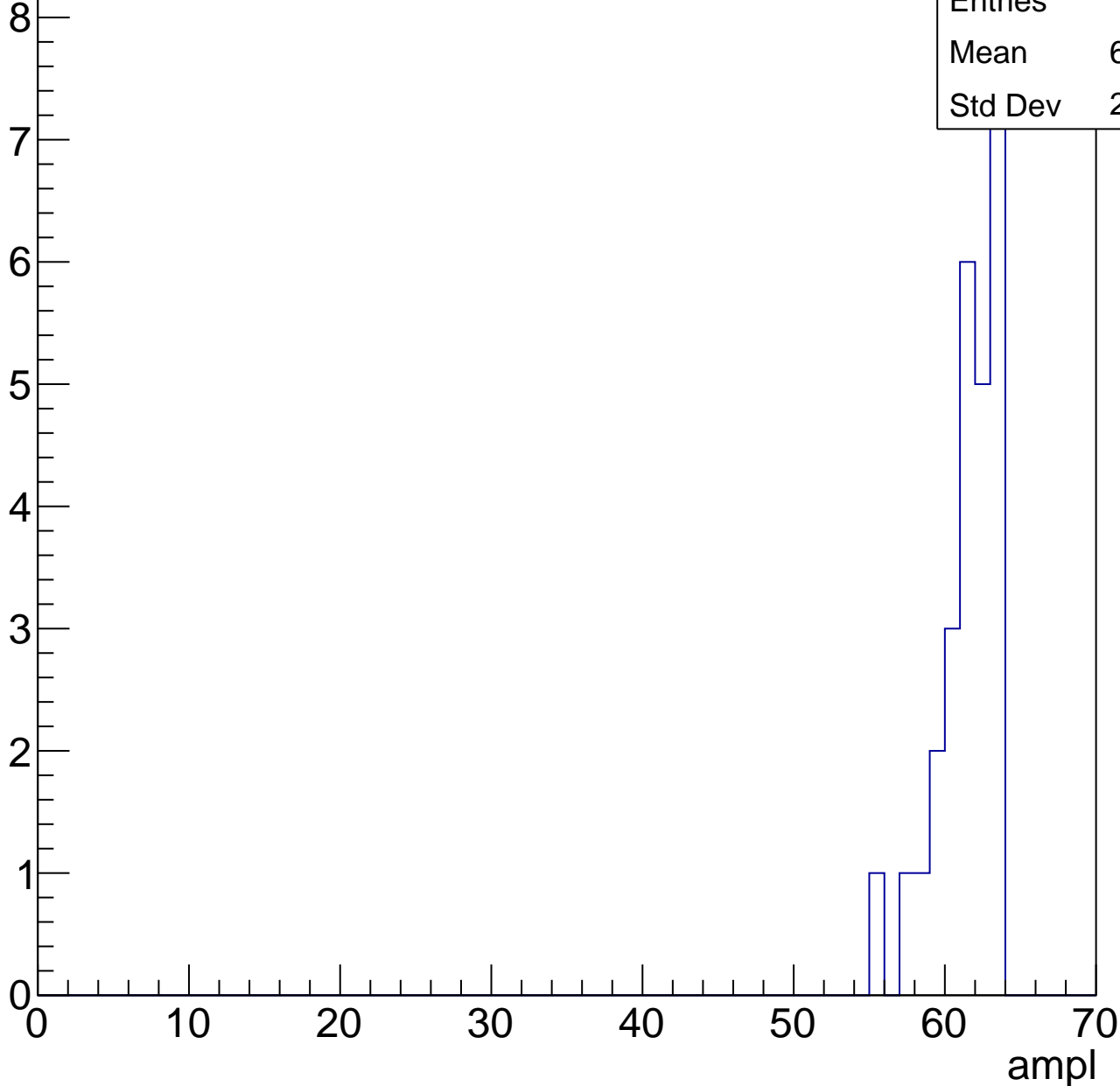


# B0L001S, U21-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

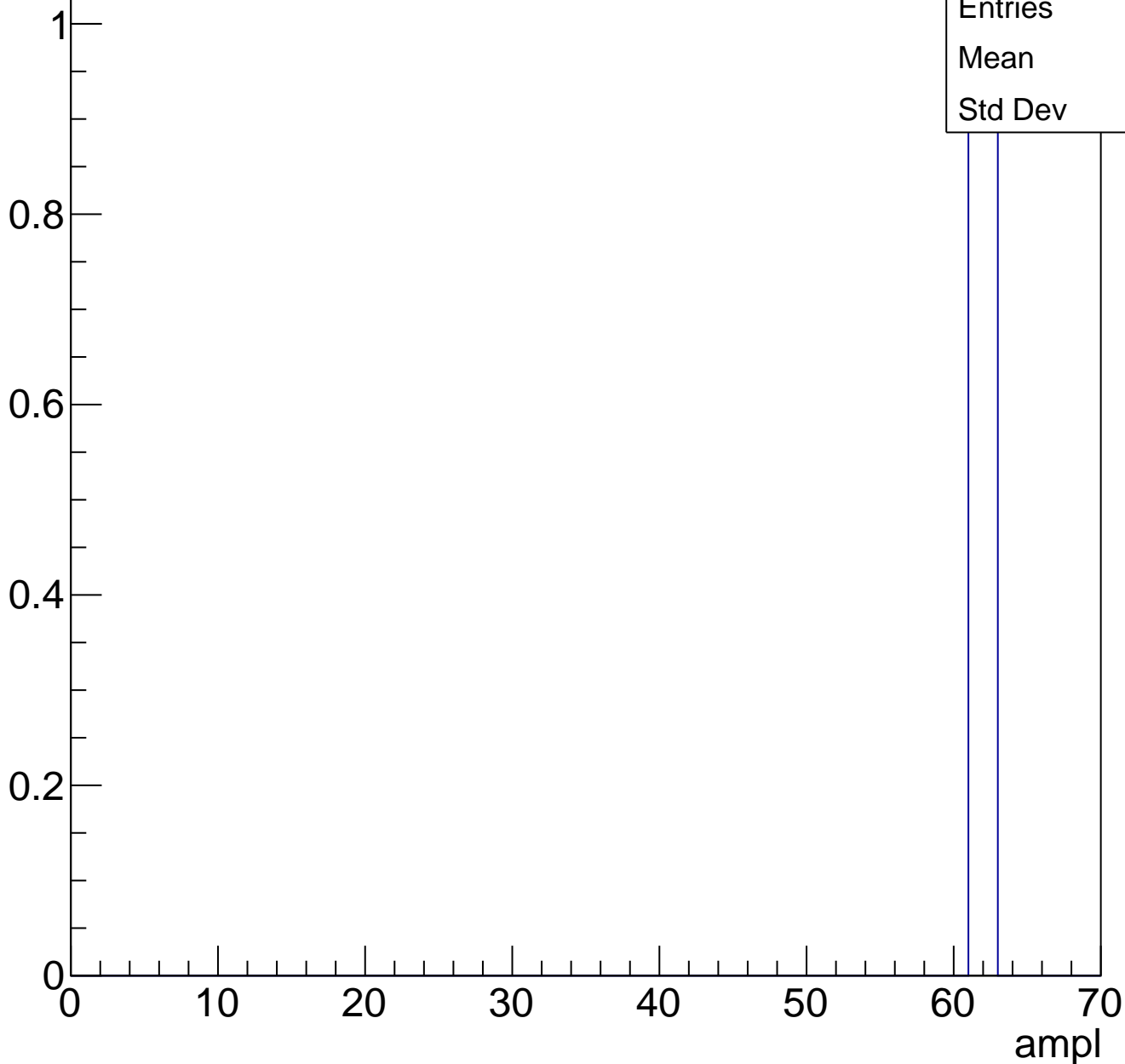
Entries	27
Mean	61.04
Std Dev	2.009



# B0L001S, U21-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch2, adc0

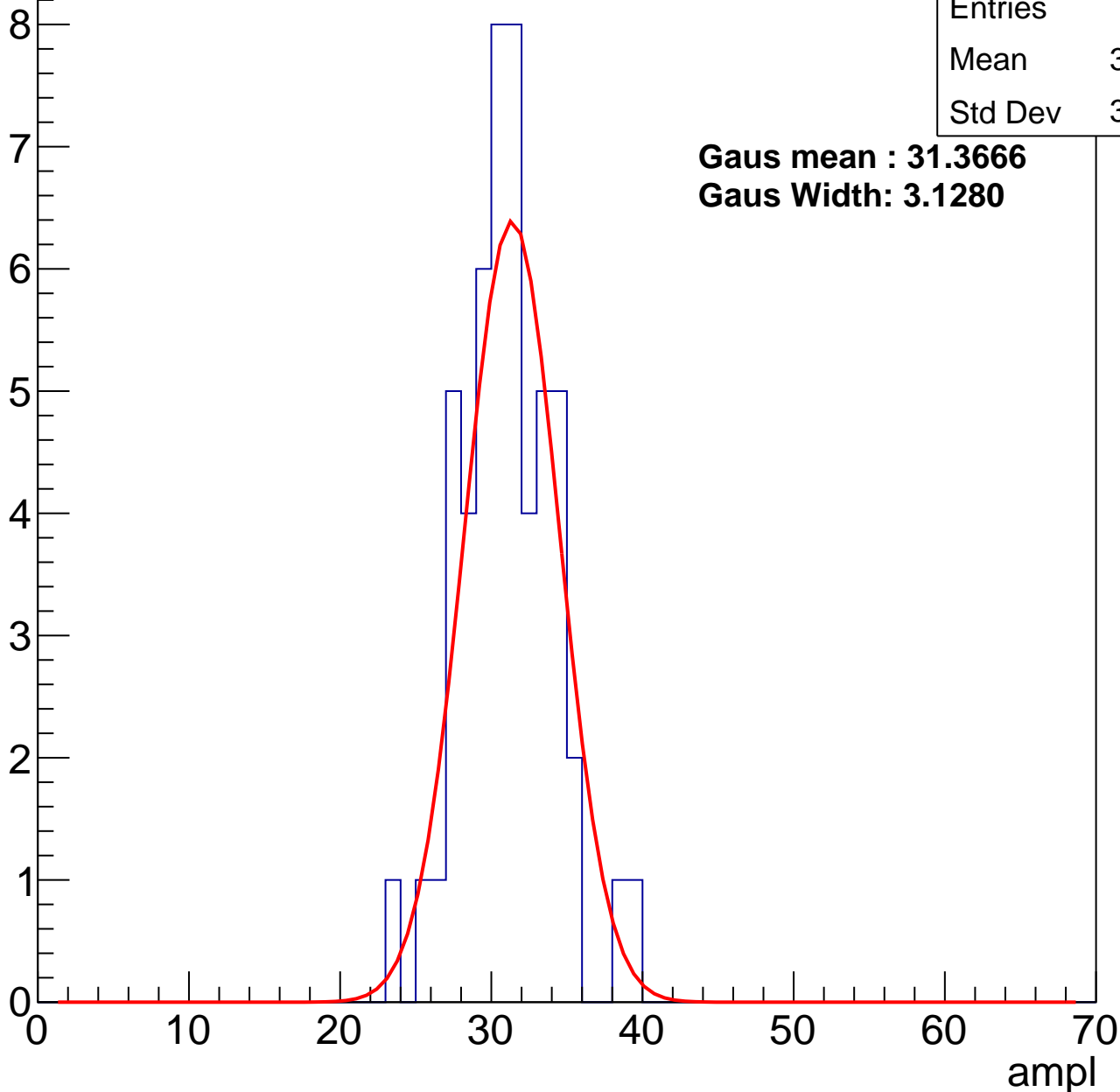
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	30.63
Std Dev	3.038

**Gaus mean : 31.3666**

**Gaus Width: 3.1280**



# B0L001S, U21-ch2, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

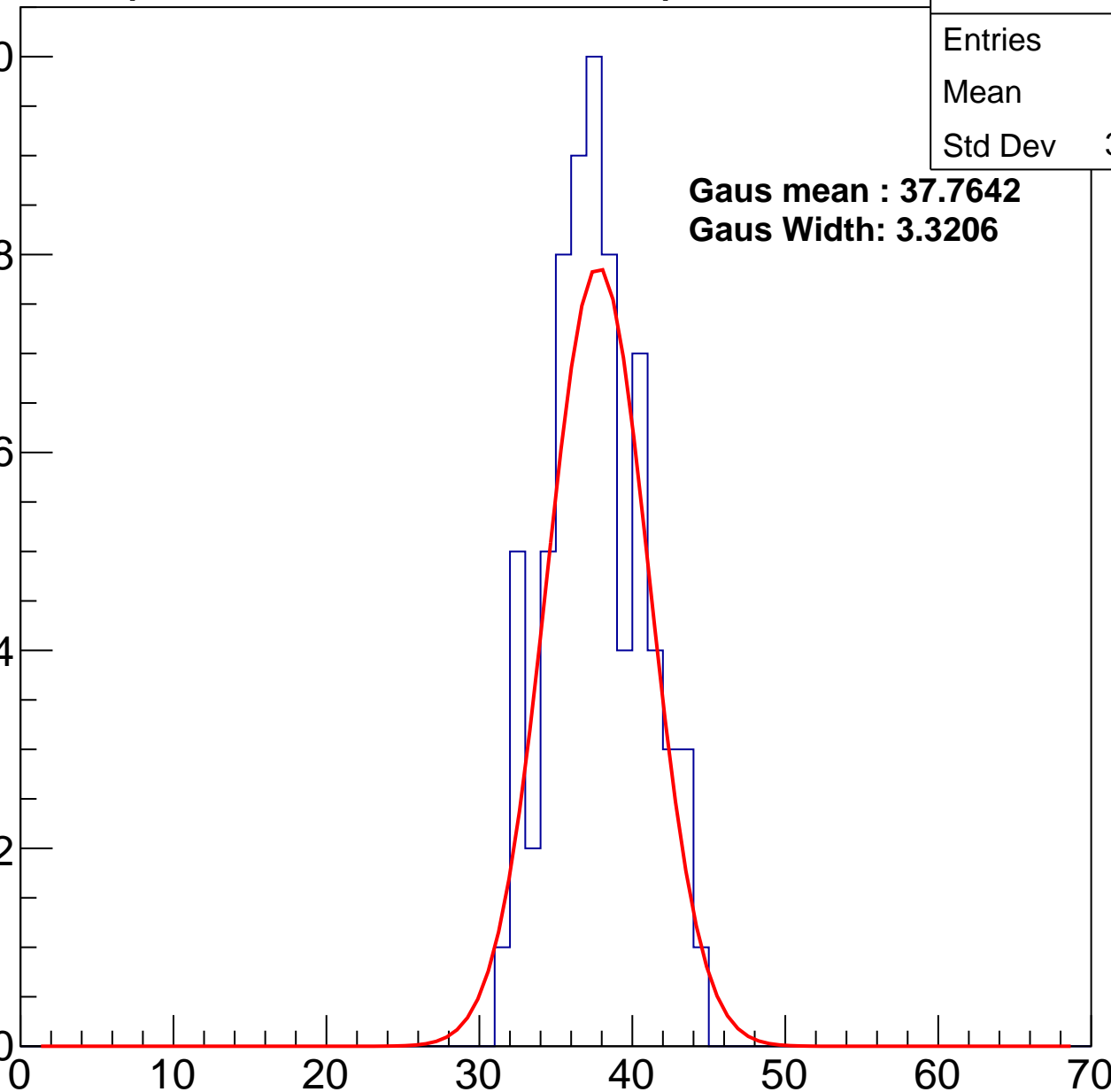
Entries	70
Mean	37.2
Std Dev	3.069

**Gaus mean : 37.7642**

**Gaus Width: 3.3206**

10  
8  
6  
4  
2  
0

ampl



# B0L001S, U21-ch2, adc2

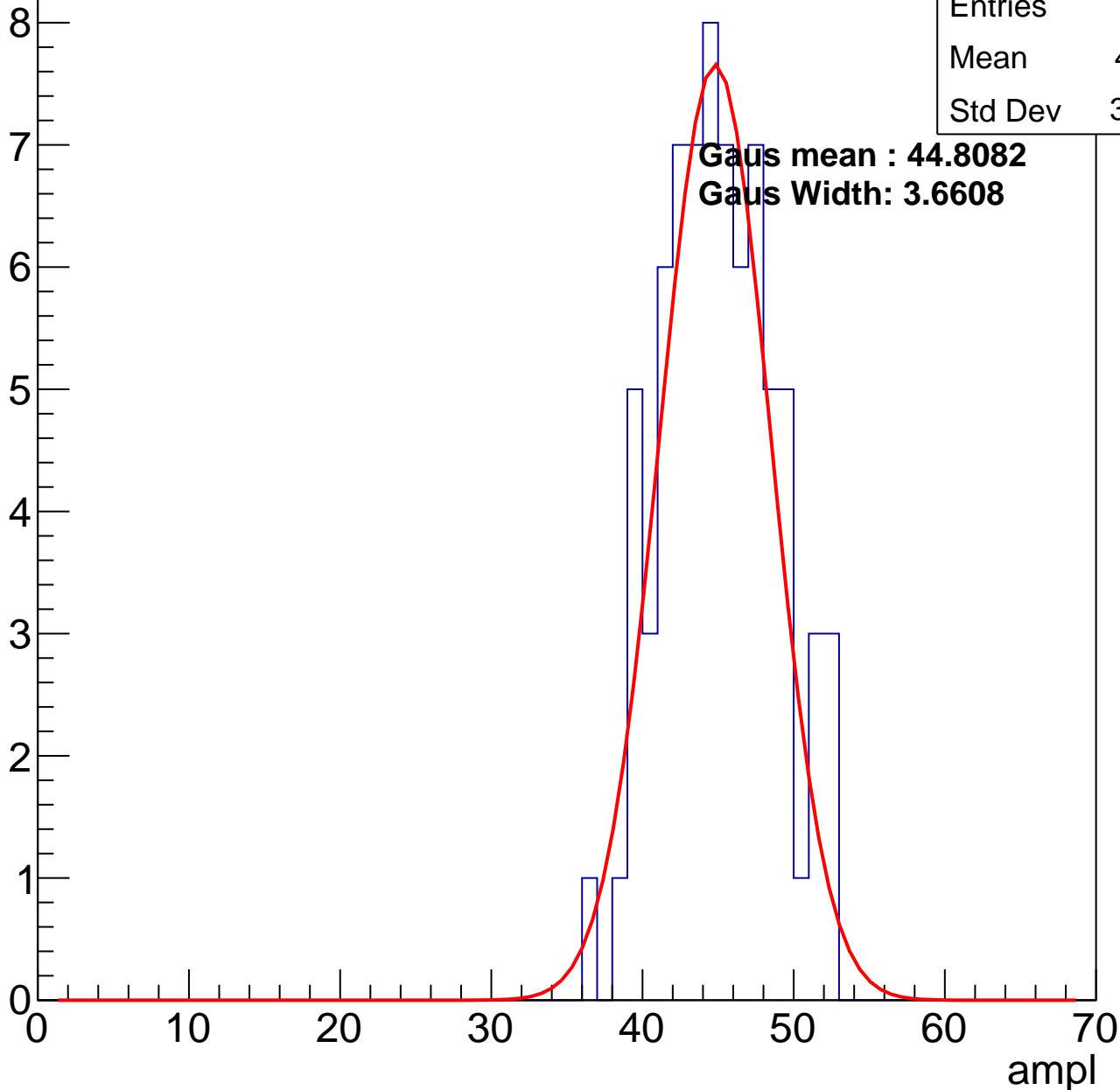
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	44.61
Std Dev	3.666

**Gaus mean : 44.8082**

**Gaus Width: 3.6608**

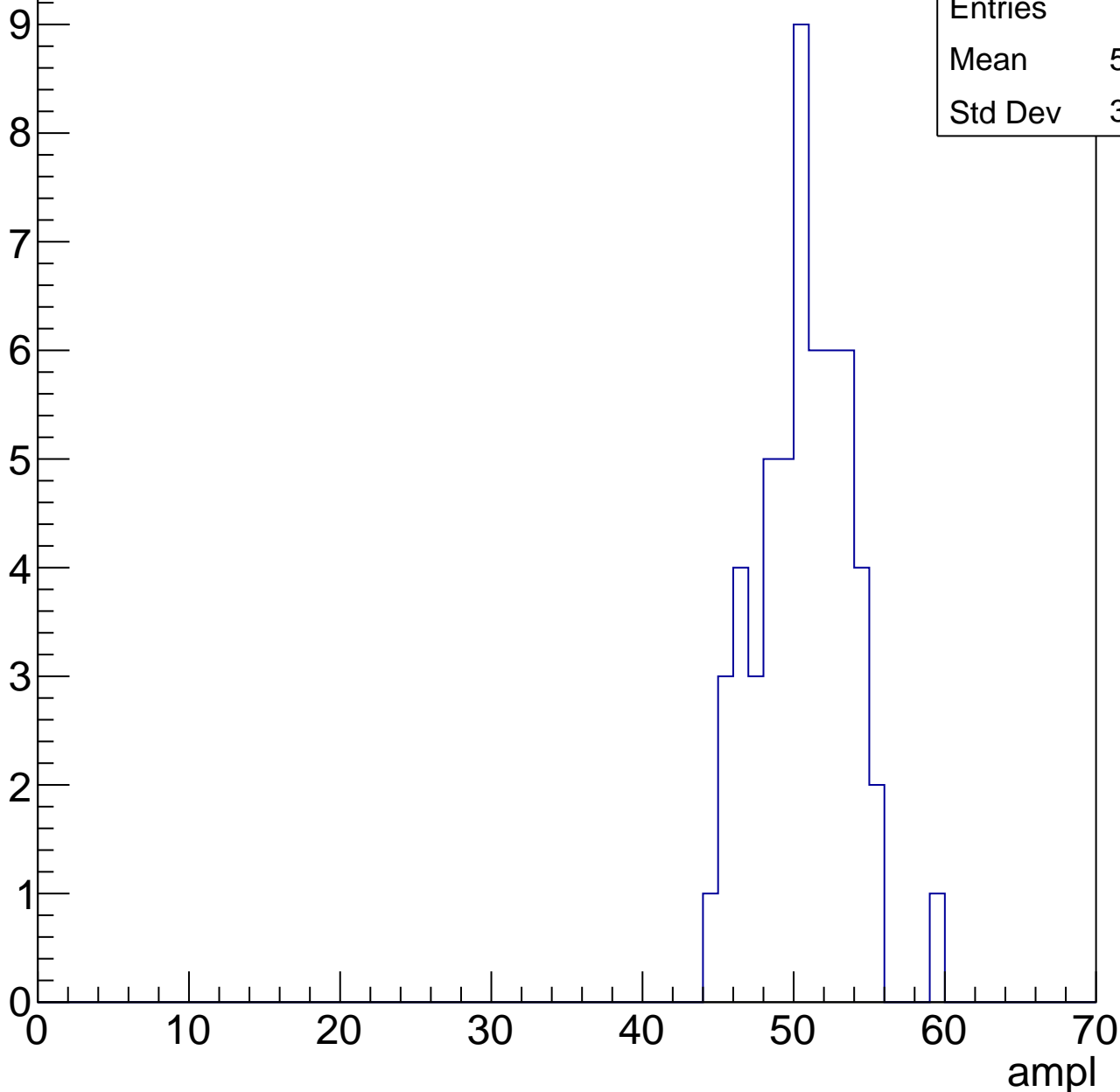


# B0L001S, U21-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

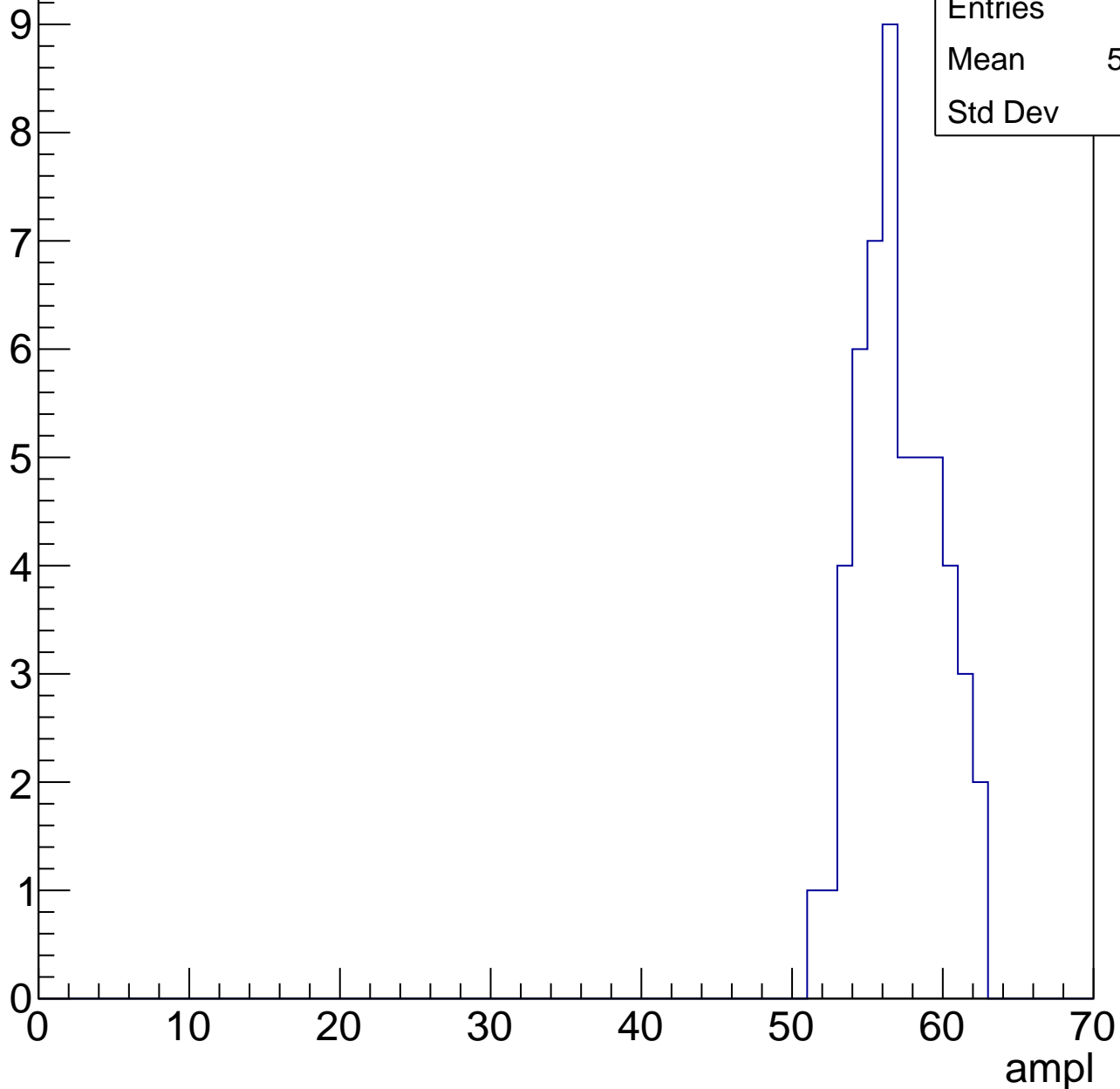
Entries	55
Mean	50.18
Std Dev	3.028



# B0L001S, U21-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



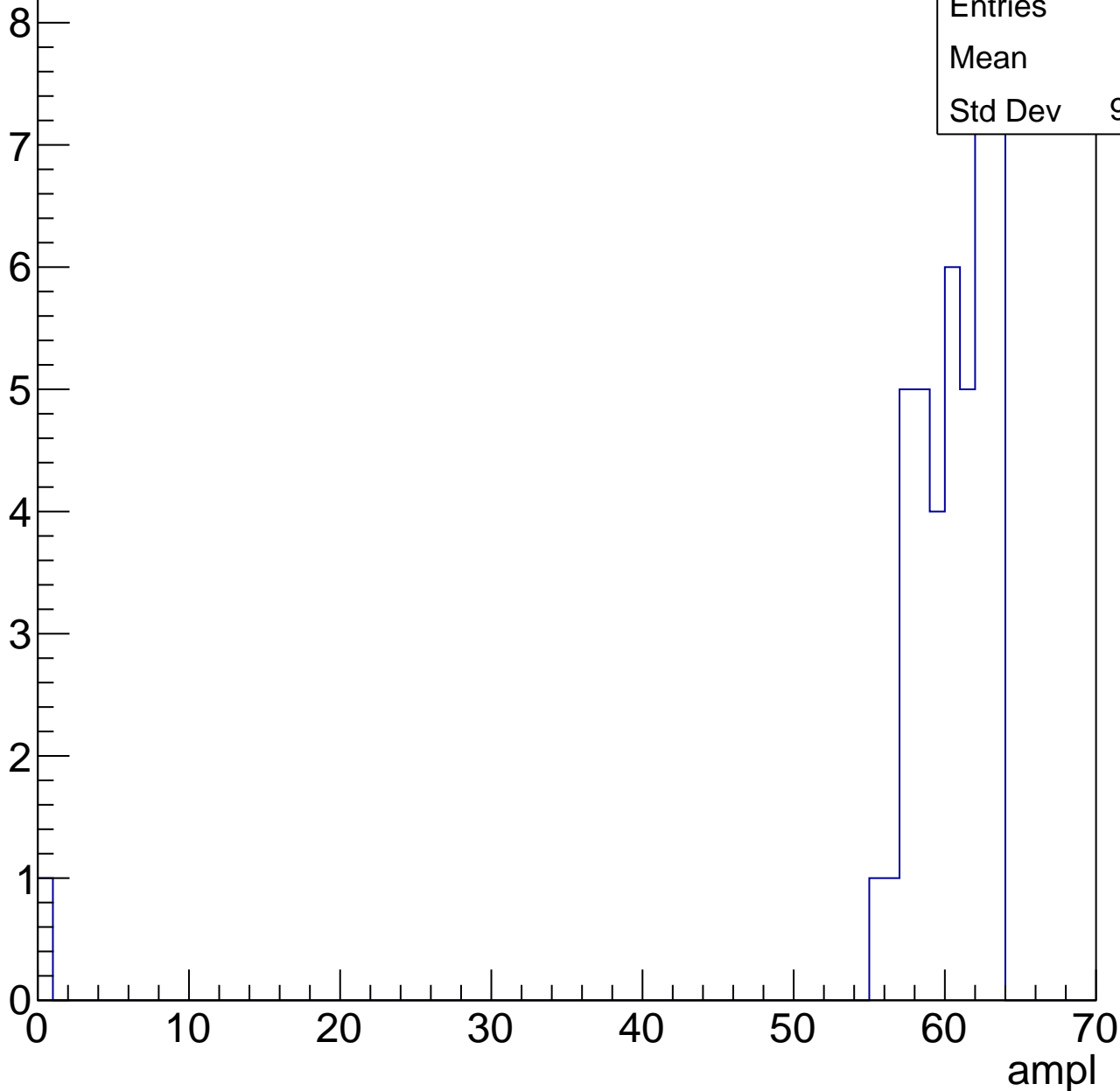
Entries	52
Mean	56.63
Std Dev	2.66

# B0L001S, U21-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	44
Mean	58.8
Std Dev	9.238



# B0L001S, U21-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U21-ch3, adc0

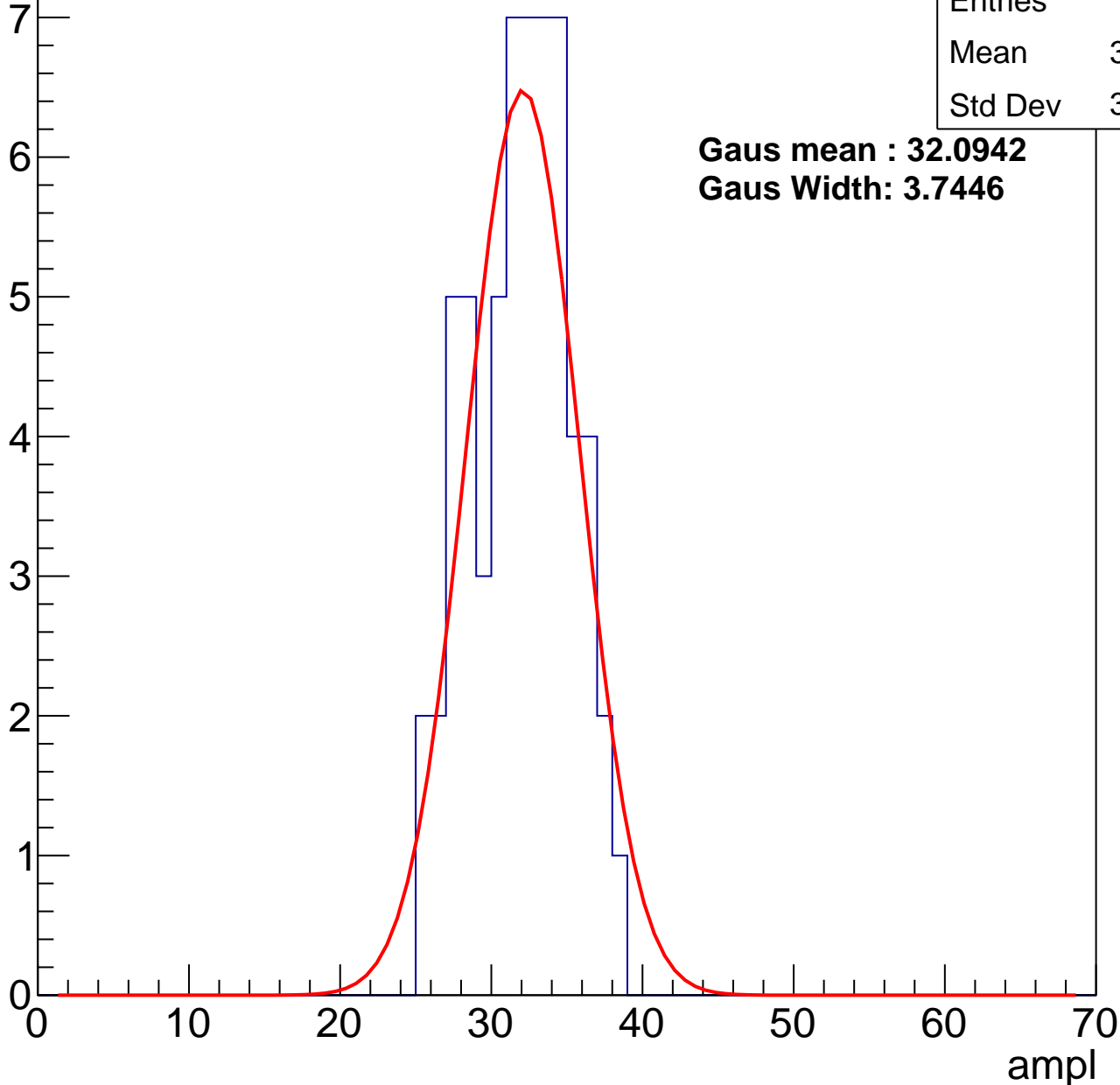
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	31.48
Std Dev	3.222

**Gaus mean : 32.0942**

**Gaus Width: 3.7446**



# B0L001S, U21-ch3, adc1

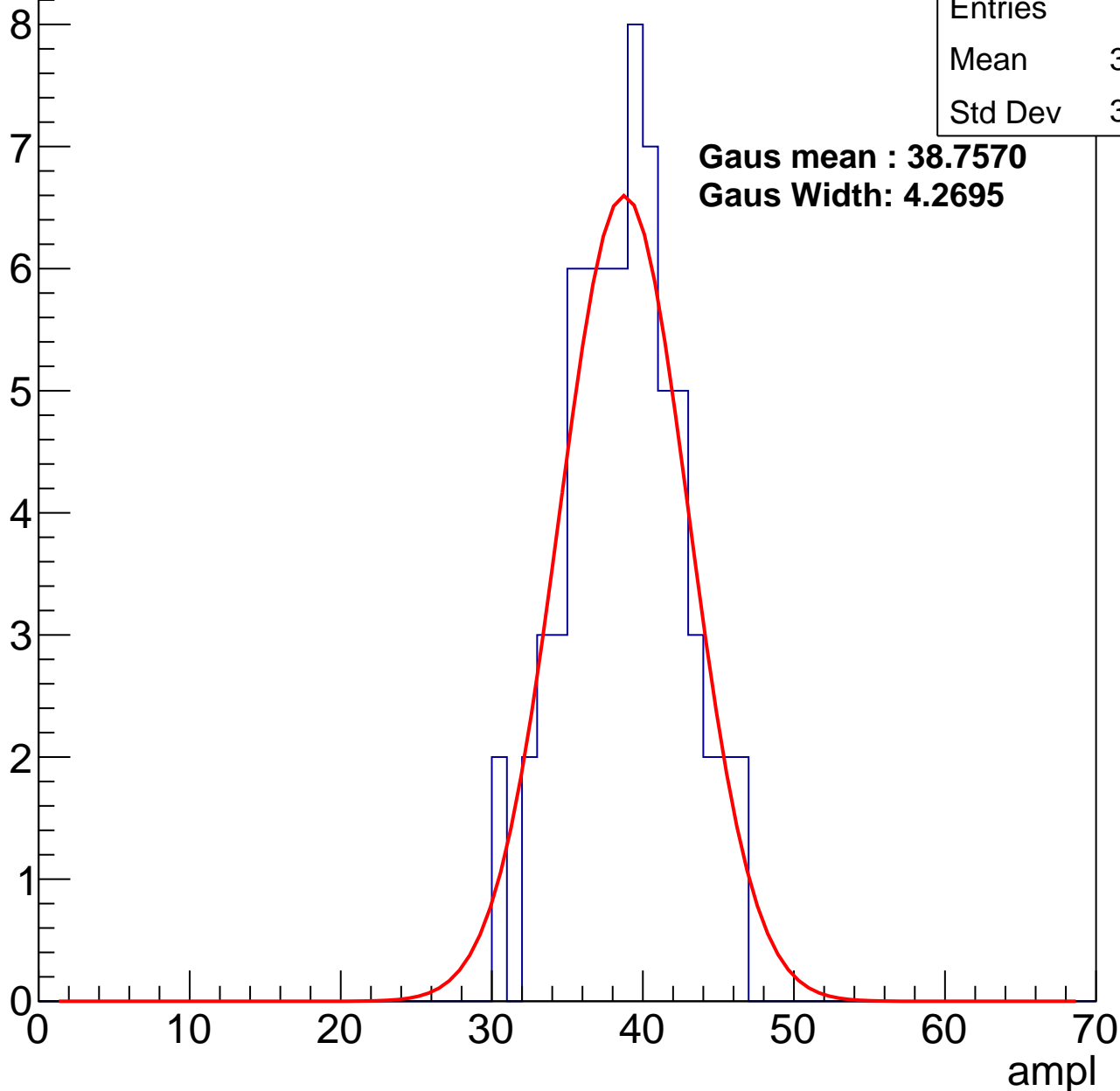
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	38.34
Std Dev	3.705

**Gaus mean : 38.7570**

**Gaus Width: 4.2695**



# B0L001S, U21-ch3, adc2

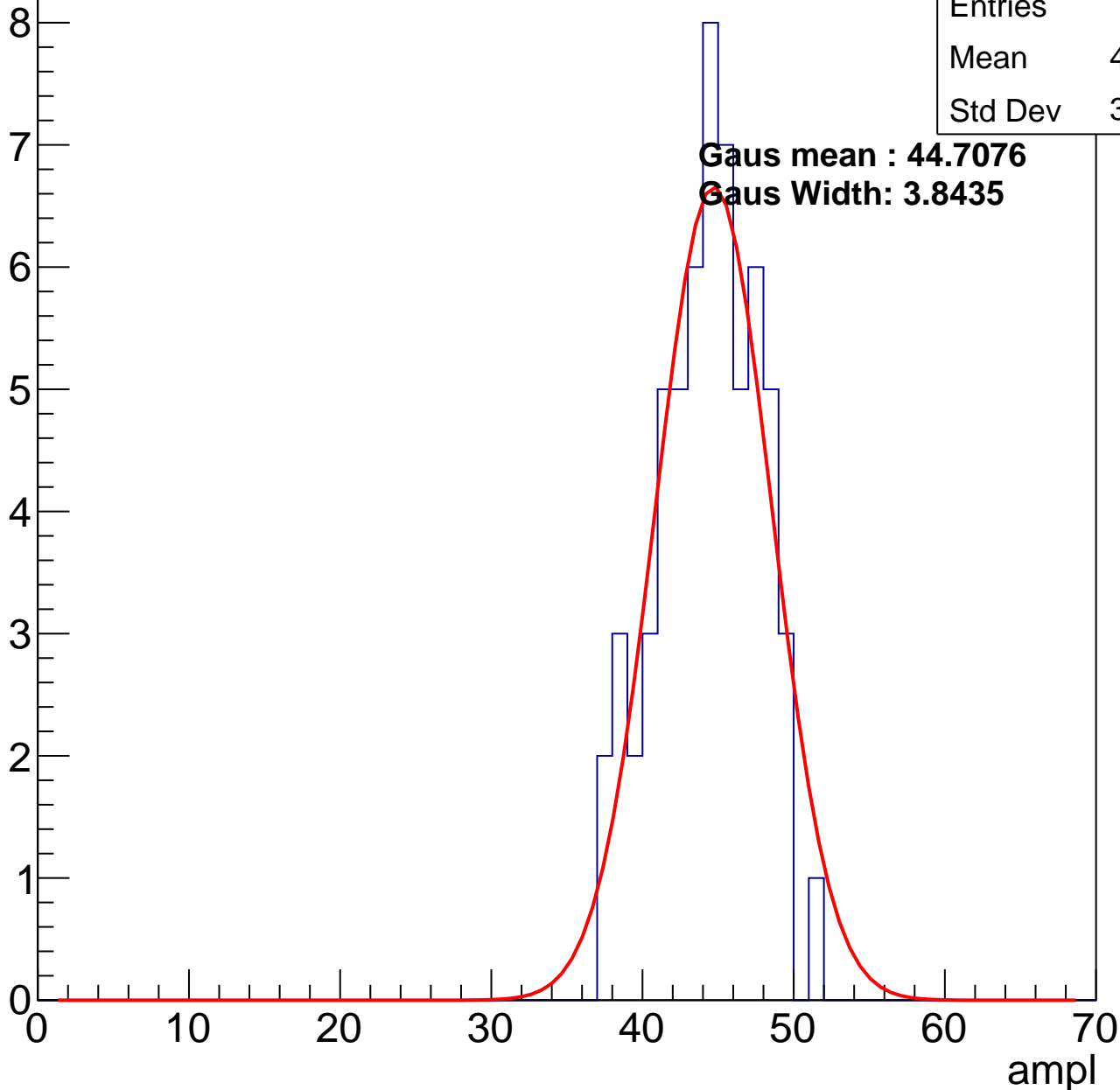
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	43.87
Std Dev	3.287

Gaus mean : 44.7076

Gaus Width: 3.8435

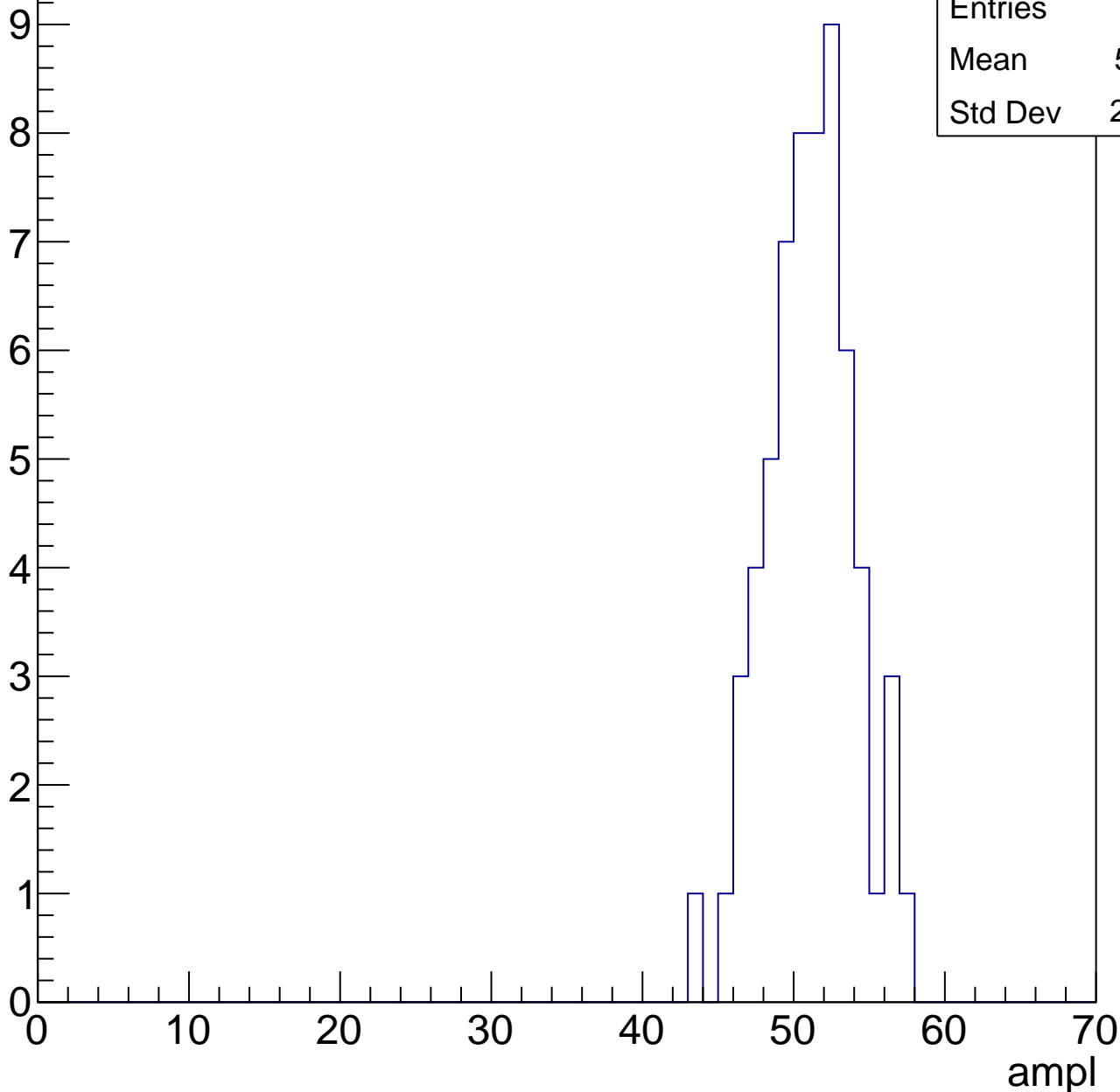


# B0L001S, U21-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

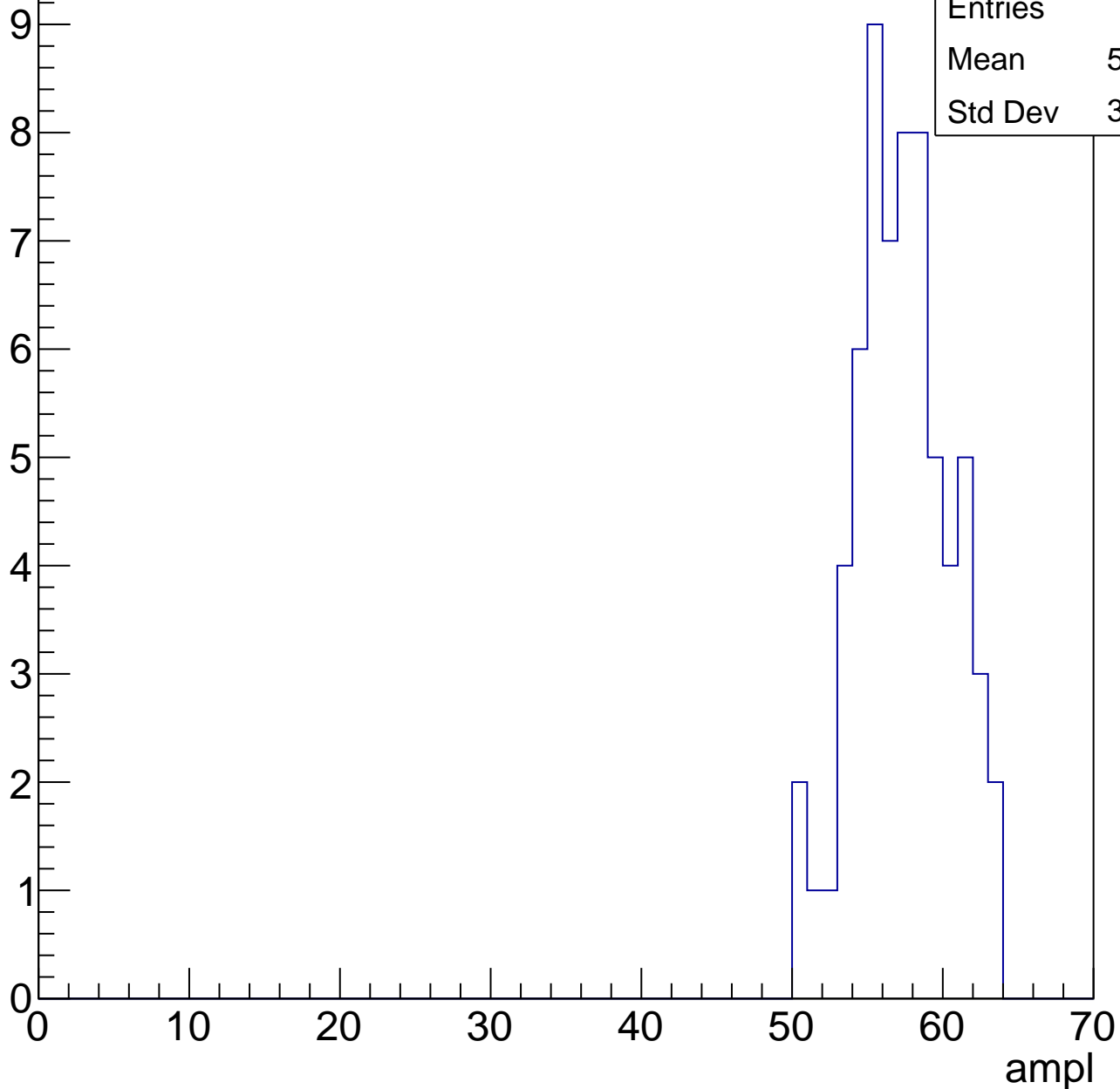
Entries	61
Mean	50.61
Std Dev	2.882



# B0L001S, U21-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



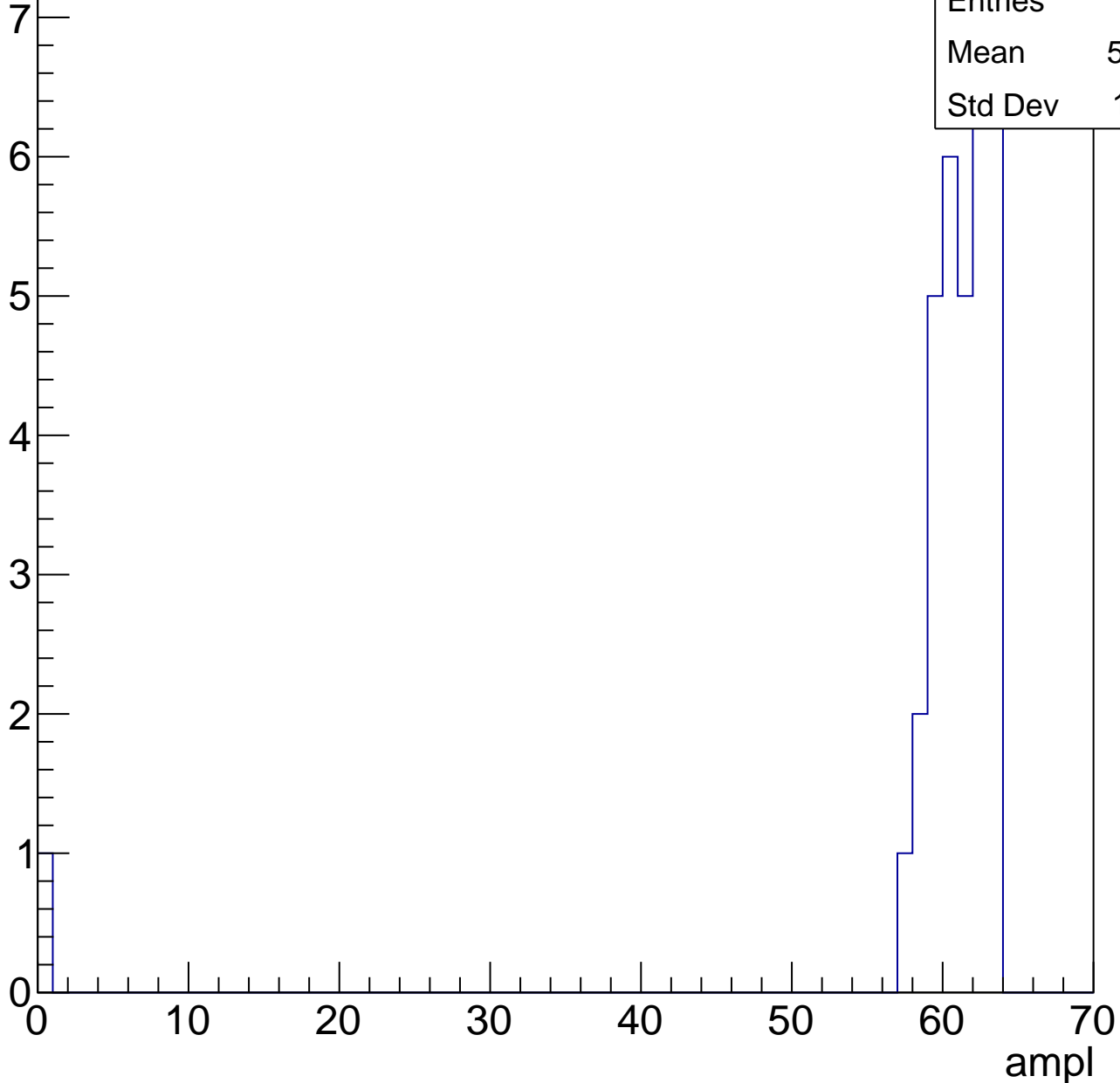
Entries	65
Mean	56.89
Std Dev	3.064

# B0L001S, U21-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

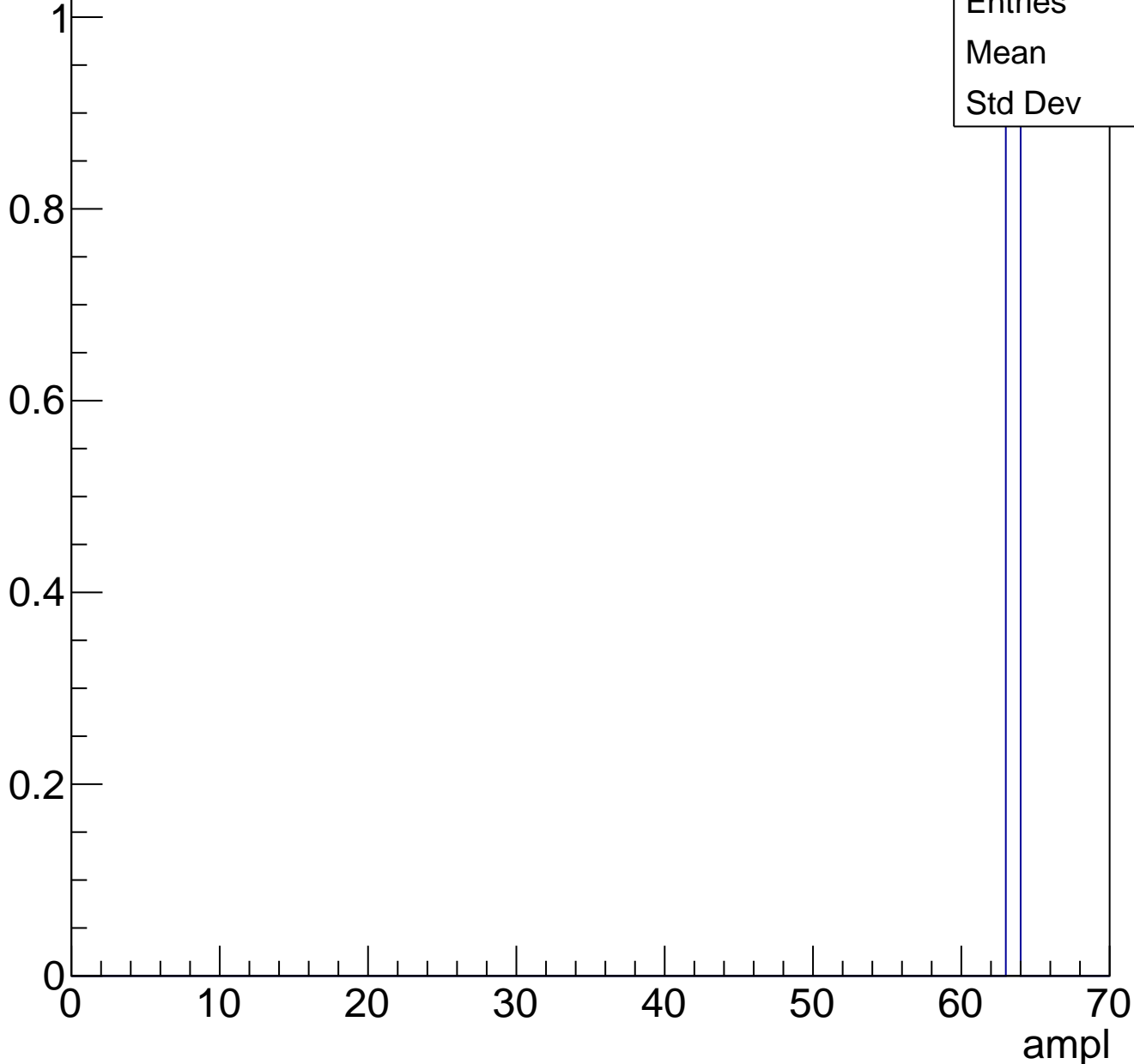
Entries	34
Mean	59.06
Std Dev	10.41



# B0L001S, U21-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U21-ch4, adc0

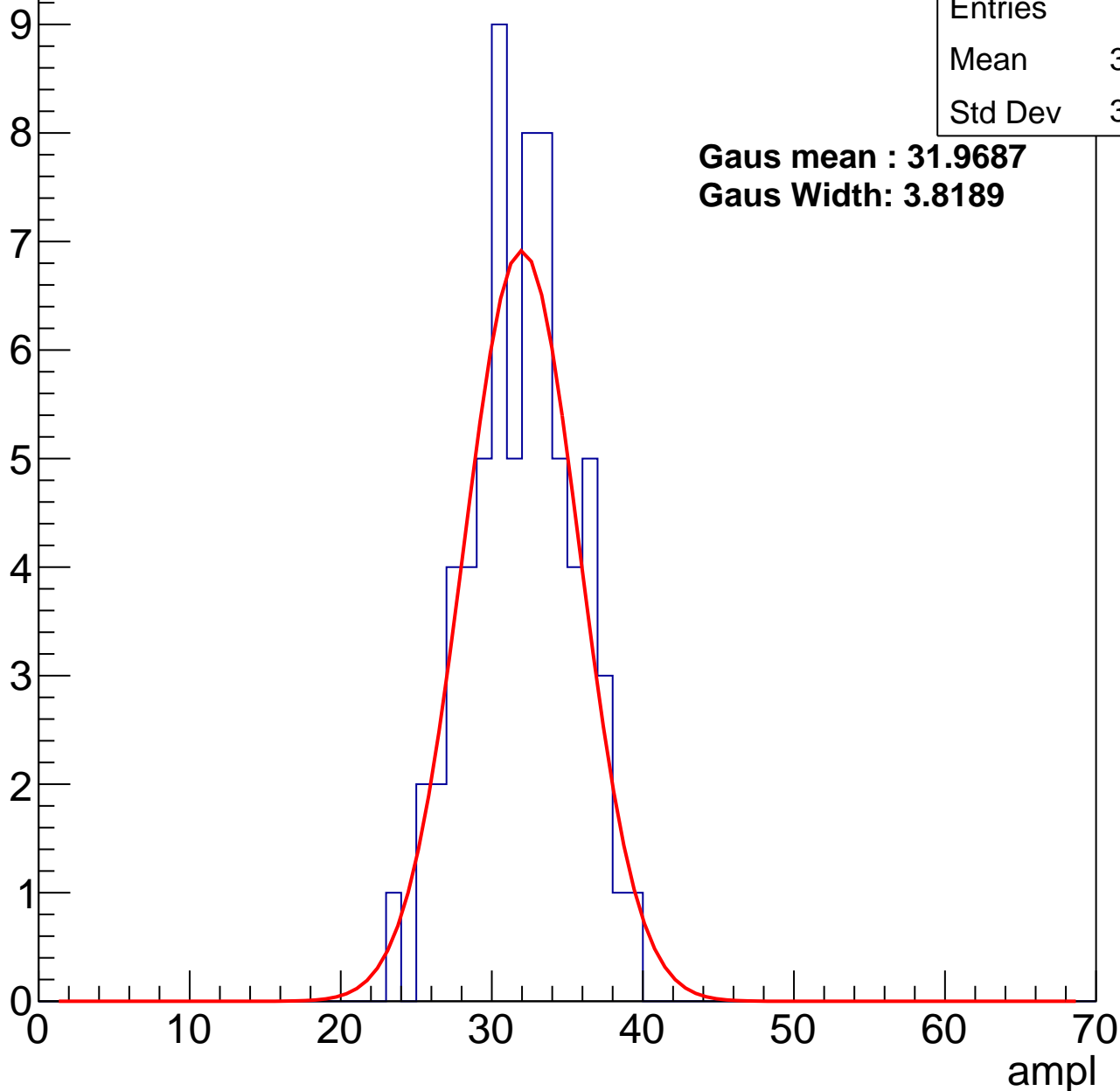
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	31.54
Std Dev	3.435

**Gaus mean : 31.9687**

**Gaus Width: 3.8189**



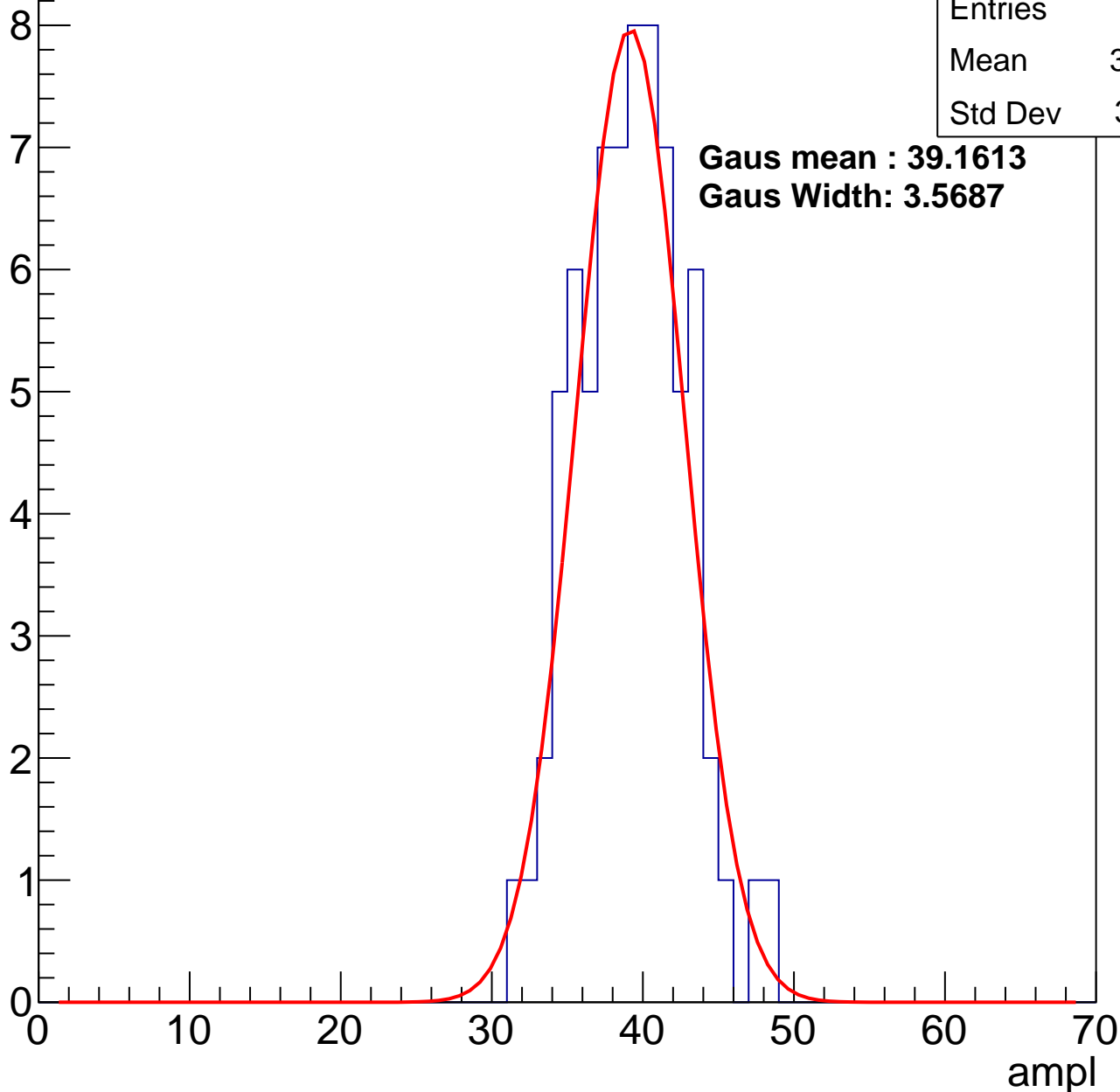
# B0L001S, U21-ch4, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	38.75
Std Dev	3.491

**Gaus mean : 39.1613**  
**Gaus Width: 3.5687**



# B0L001S, U21-ch4, adc2

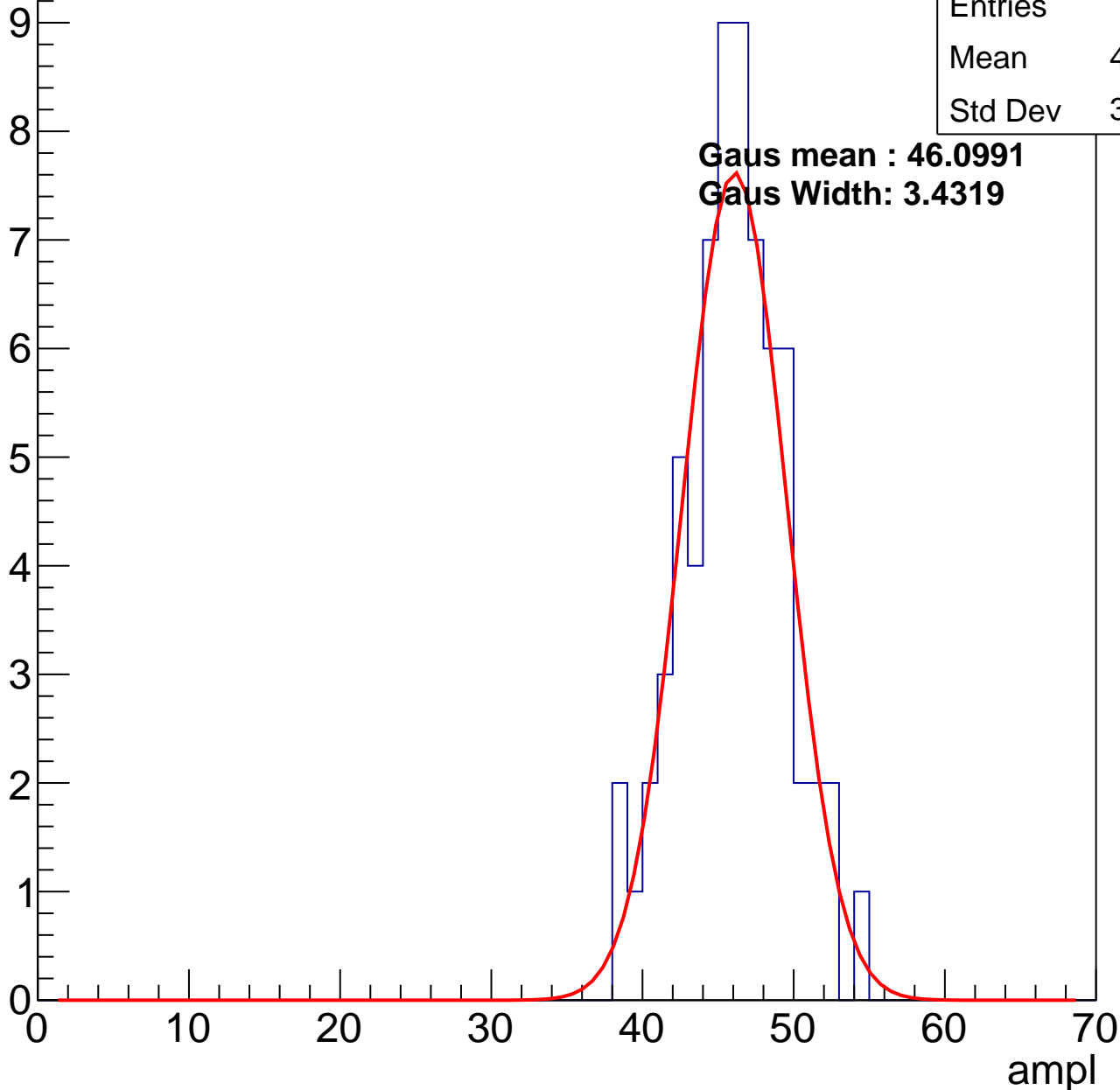
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	45.56
Std Dev	3.358

**Gaus mean : 46.0991**

**Gaus Width: 3.4319**

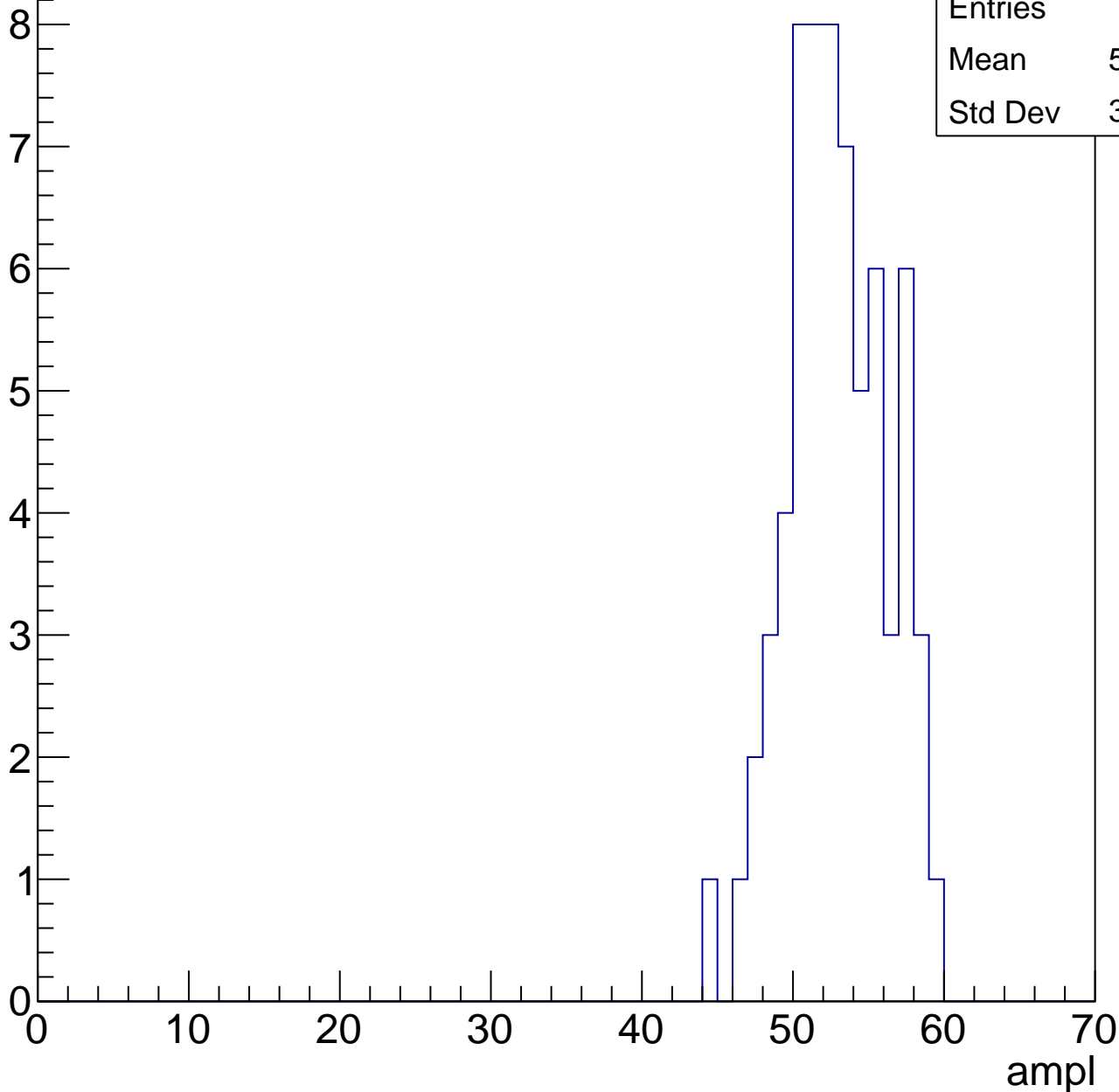


# B0L001S, U21-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	52.45
Std Dev	3.248



# B0L001S, U21-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

7

6

5

4

3

2

1

0

Entries	52
Mean	58.23
Std Dev	2.933

ampl

0

10

20

30

40

50

60

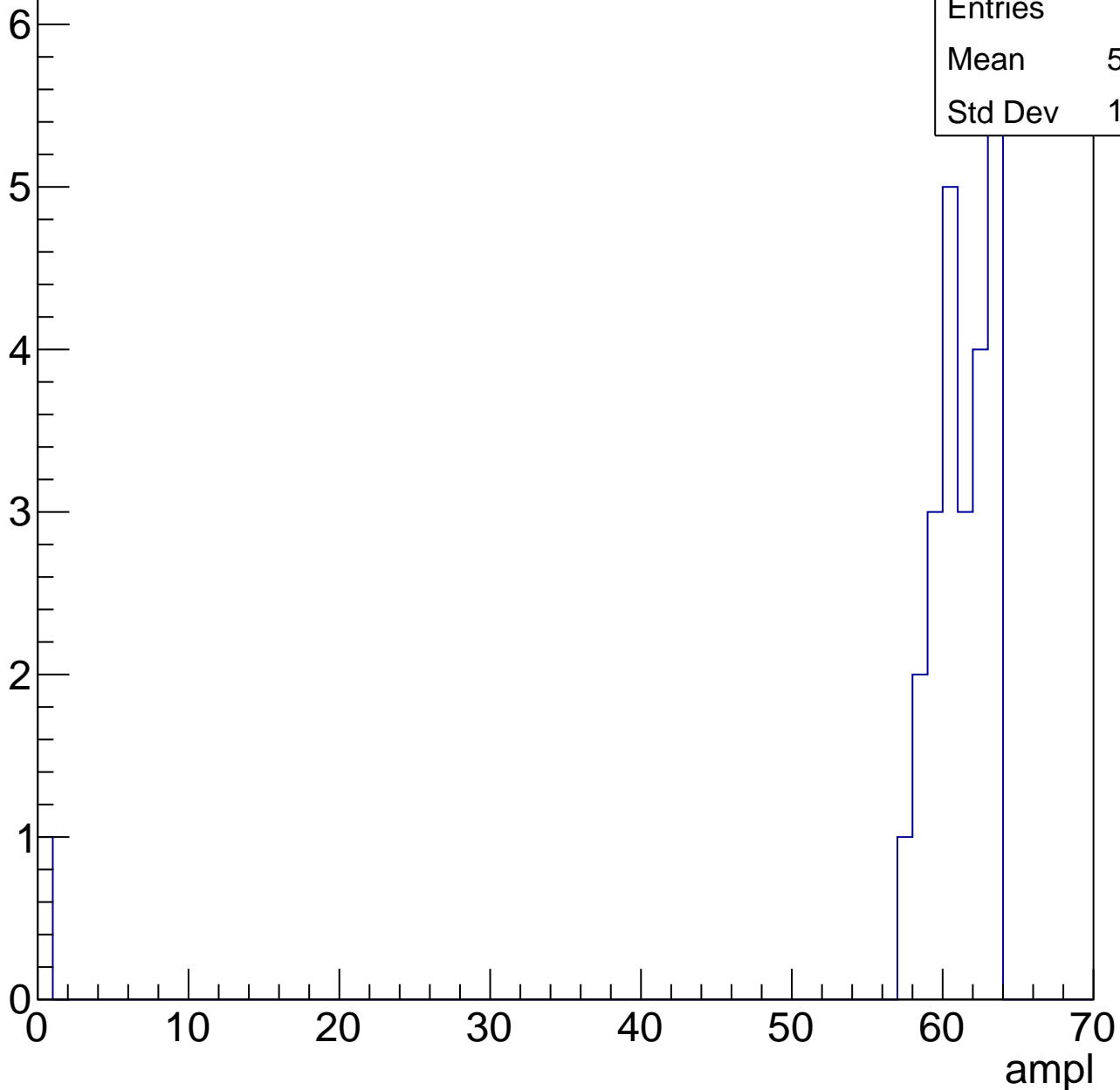
70

# B0L001S, U21-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	25
Mean	58.36
Std Dev	12.04



# B0L001S, U21-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch5, adc0

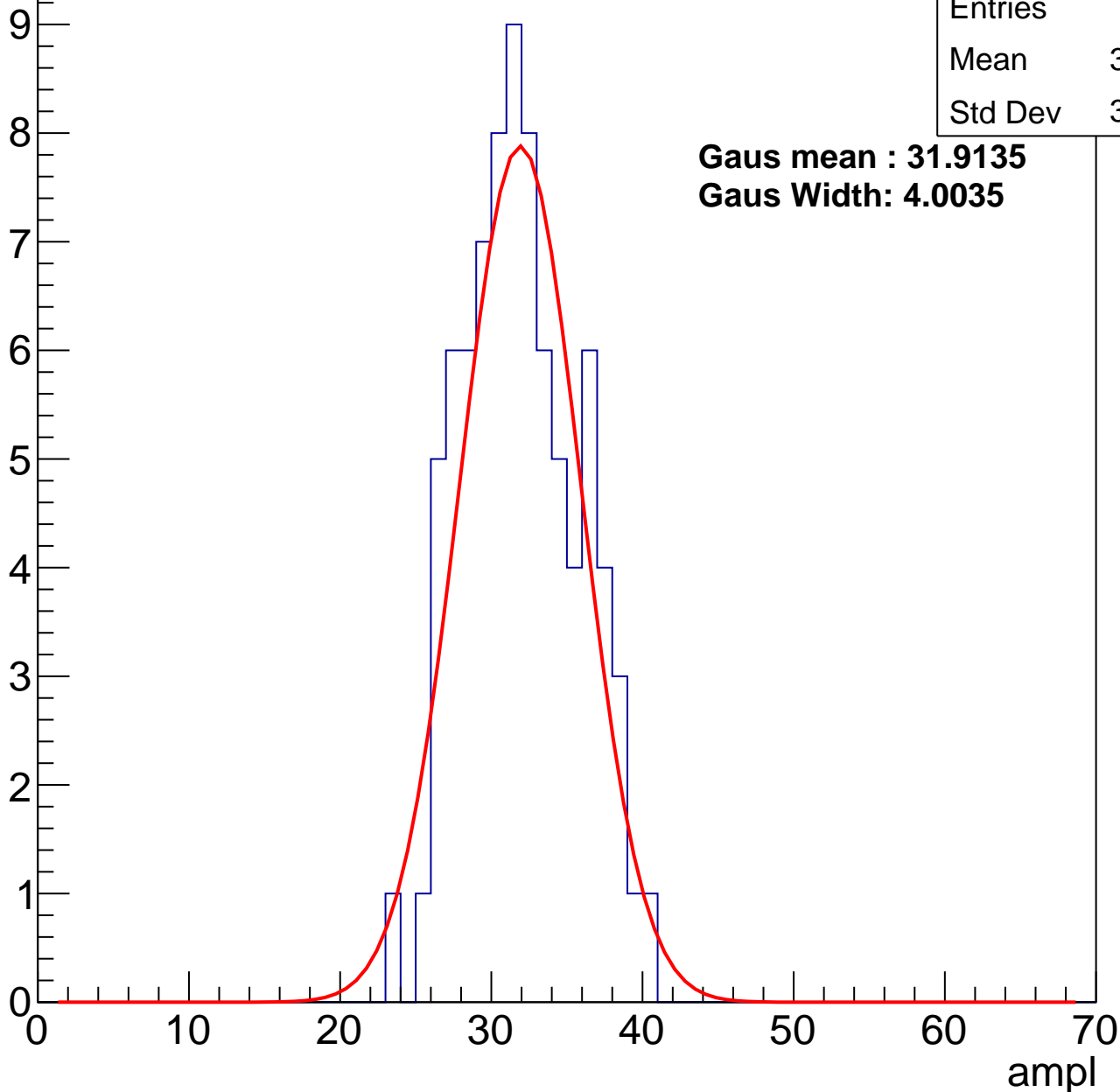
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	31.49
Std Dev	3.716

**Gaus mean : 31.9135**

**Gaus Width: 4.0035**



# B0L001S, U21-ch5, adc1

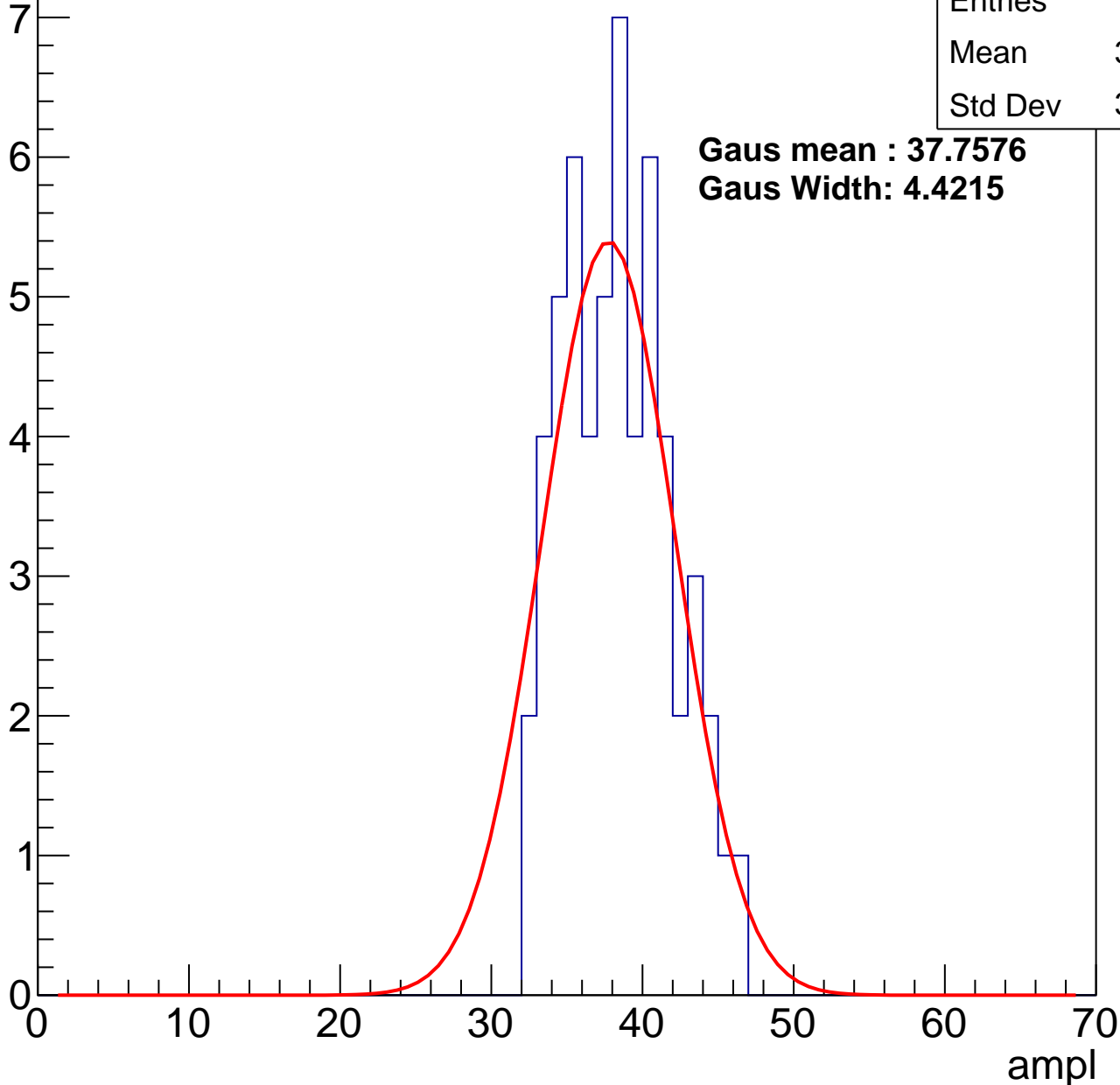
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	37.91
Std Dev	3.491

**Gaus mean : 37.7576**

**Gaus Width: 4.4215**



# B0L001S, U21-ch5, adc2

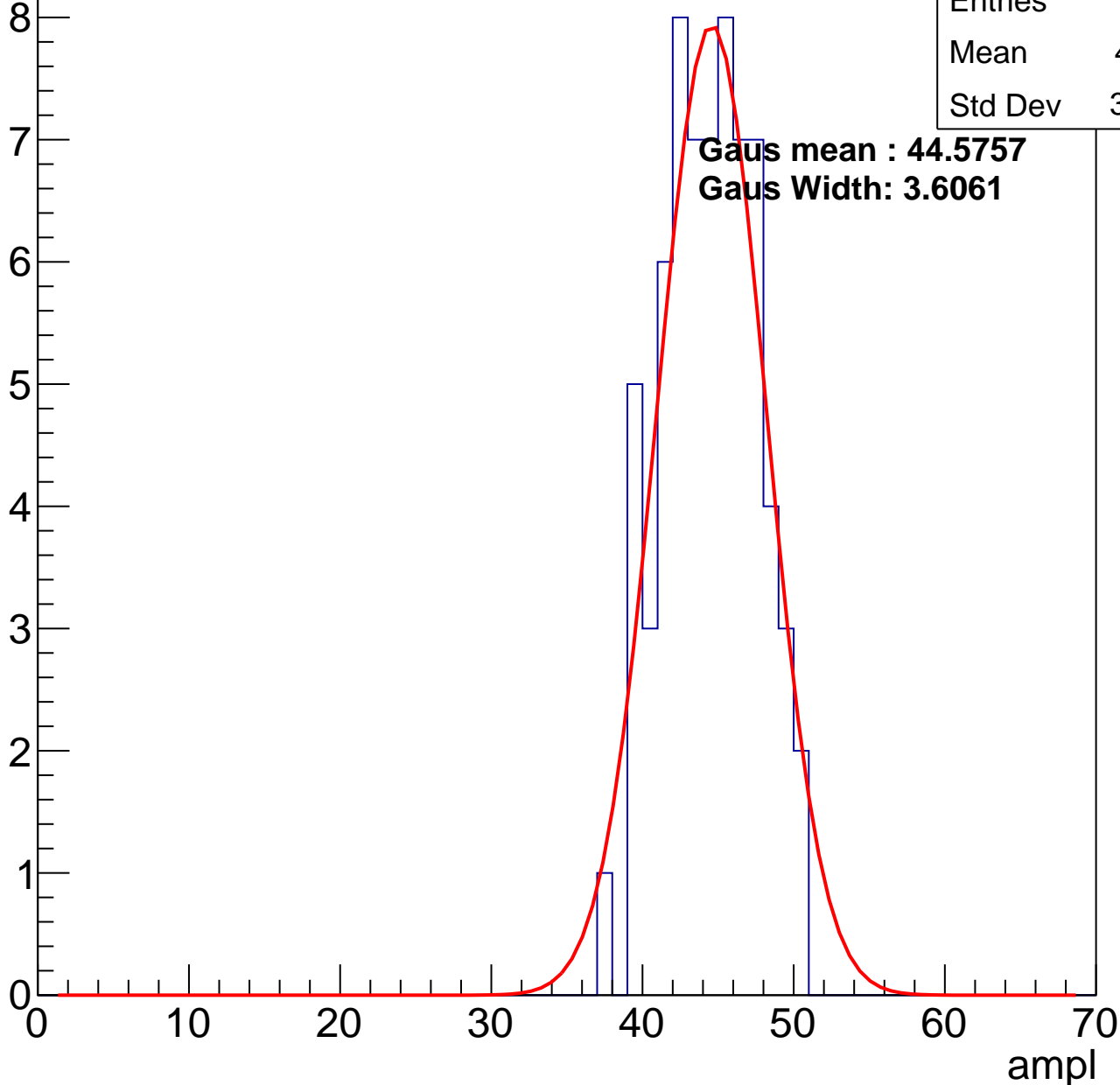
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	44.01
Std Dev	3.032

**Gaus mean : 44.5757**

**Gaus Width: 3.6061**

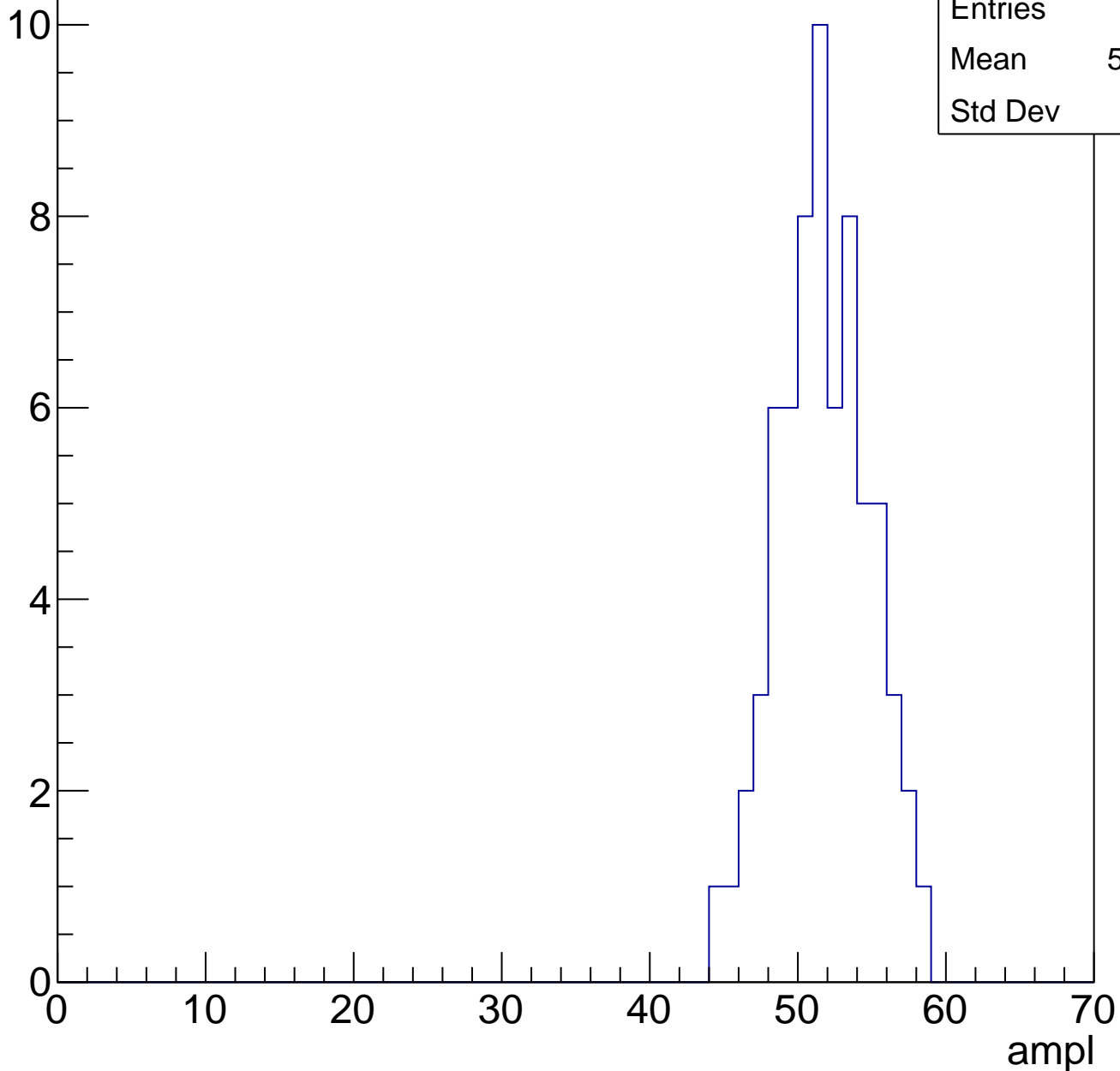


# B0L001S, U21-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	51.27
Std Dev	3.05

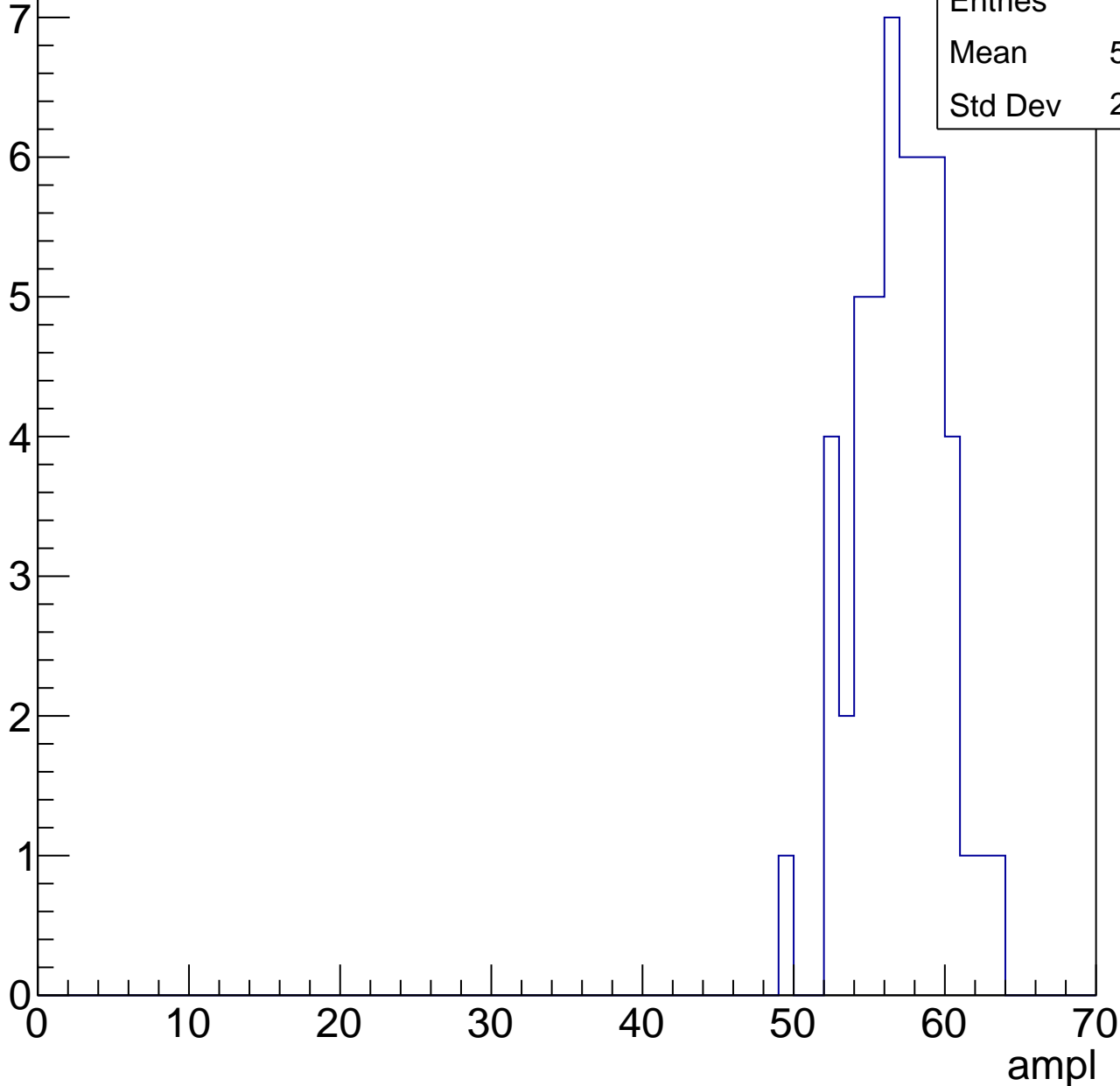


# B0L001S, U21-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

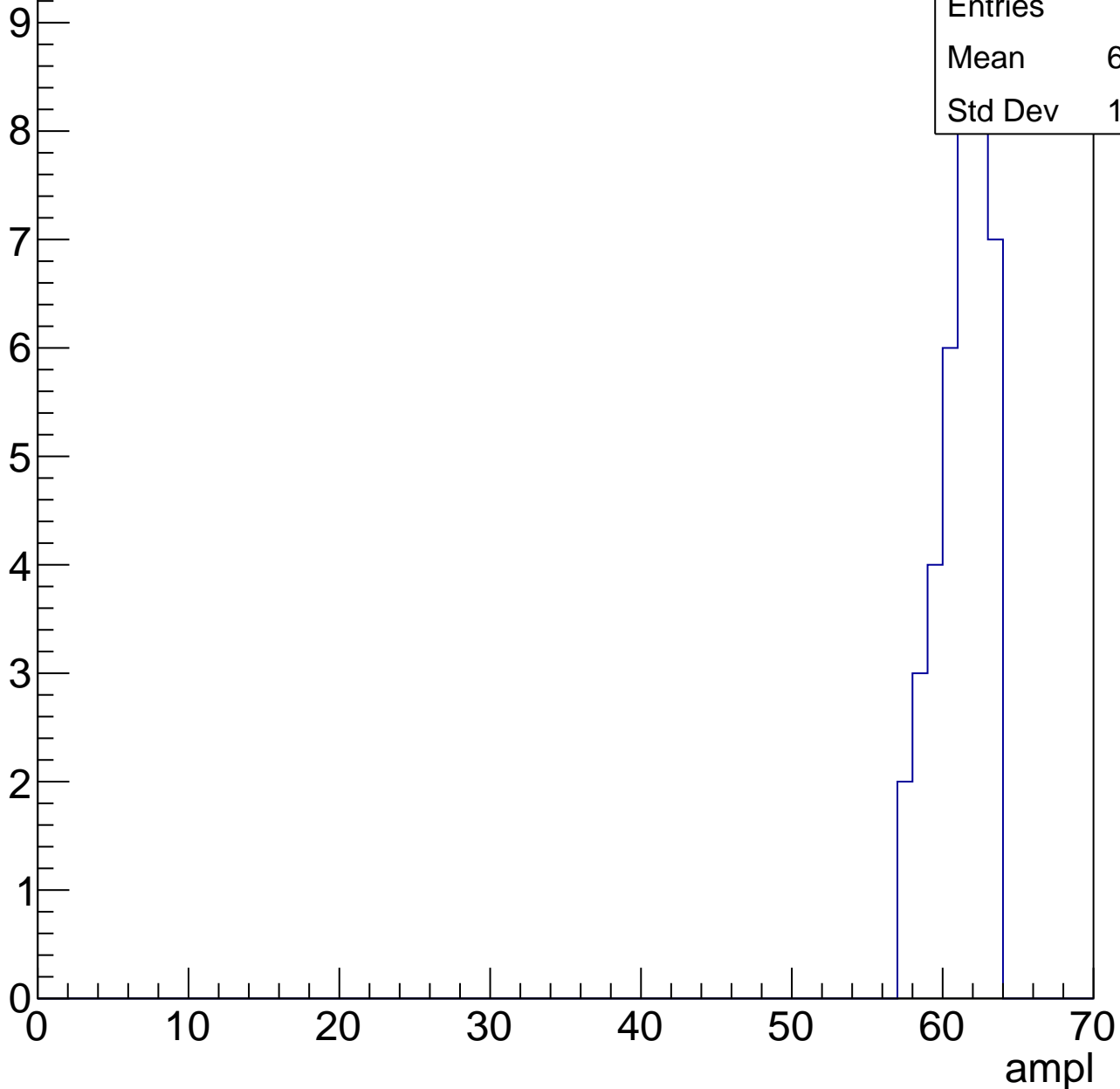
Entries	49
Mean	56.53
Std Dev	2.858



# B0L001S, U21-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U21-ch6, adc0

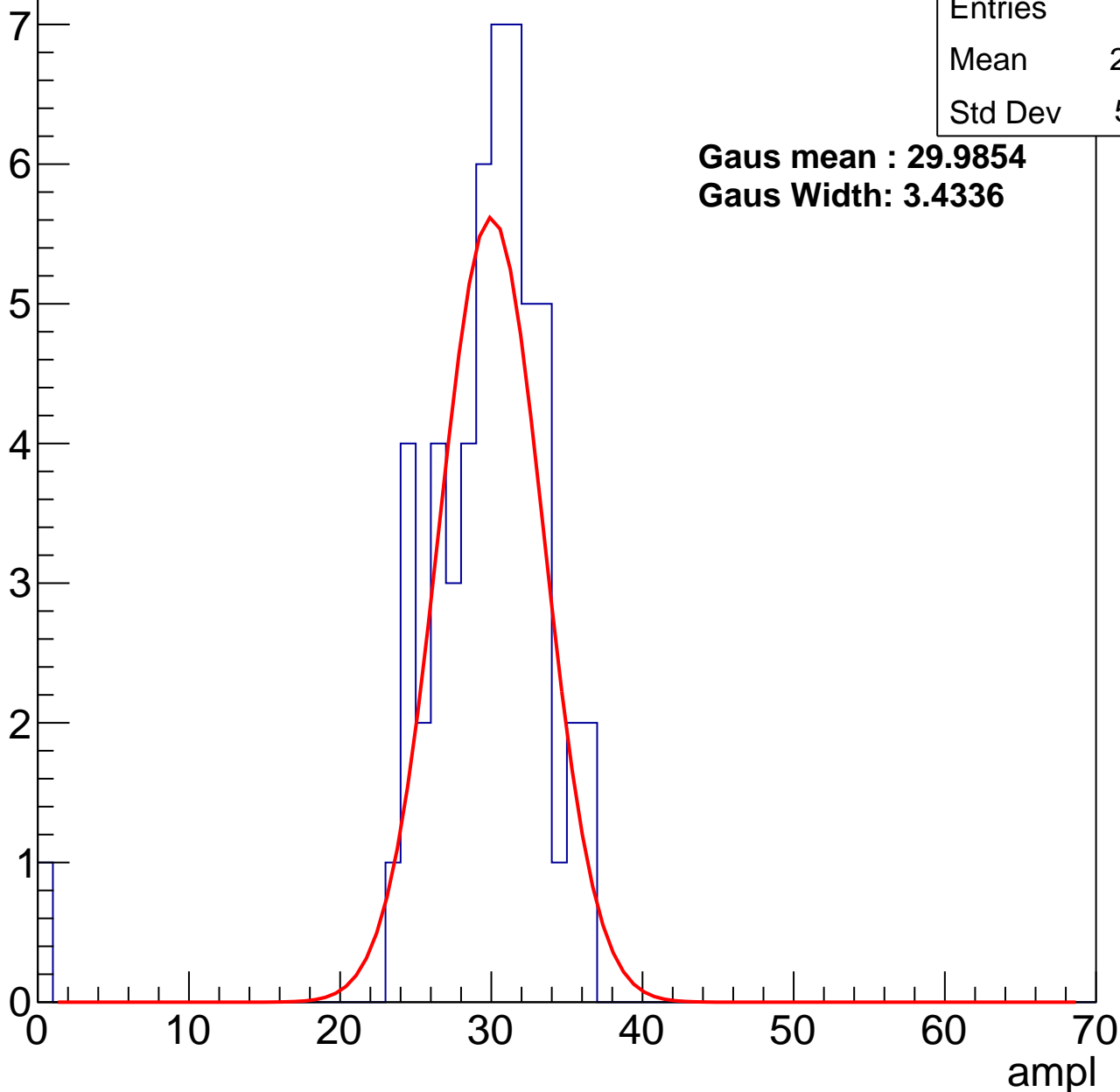
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	29.04
Std Dev	5.121

**Gaus mean : 29.9854**

**Gaus Width: 3.4336**



# B0L001S, U21-ch6, adc1

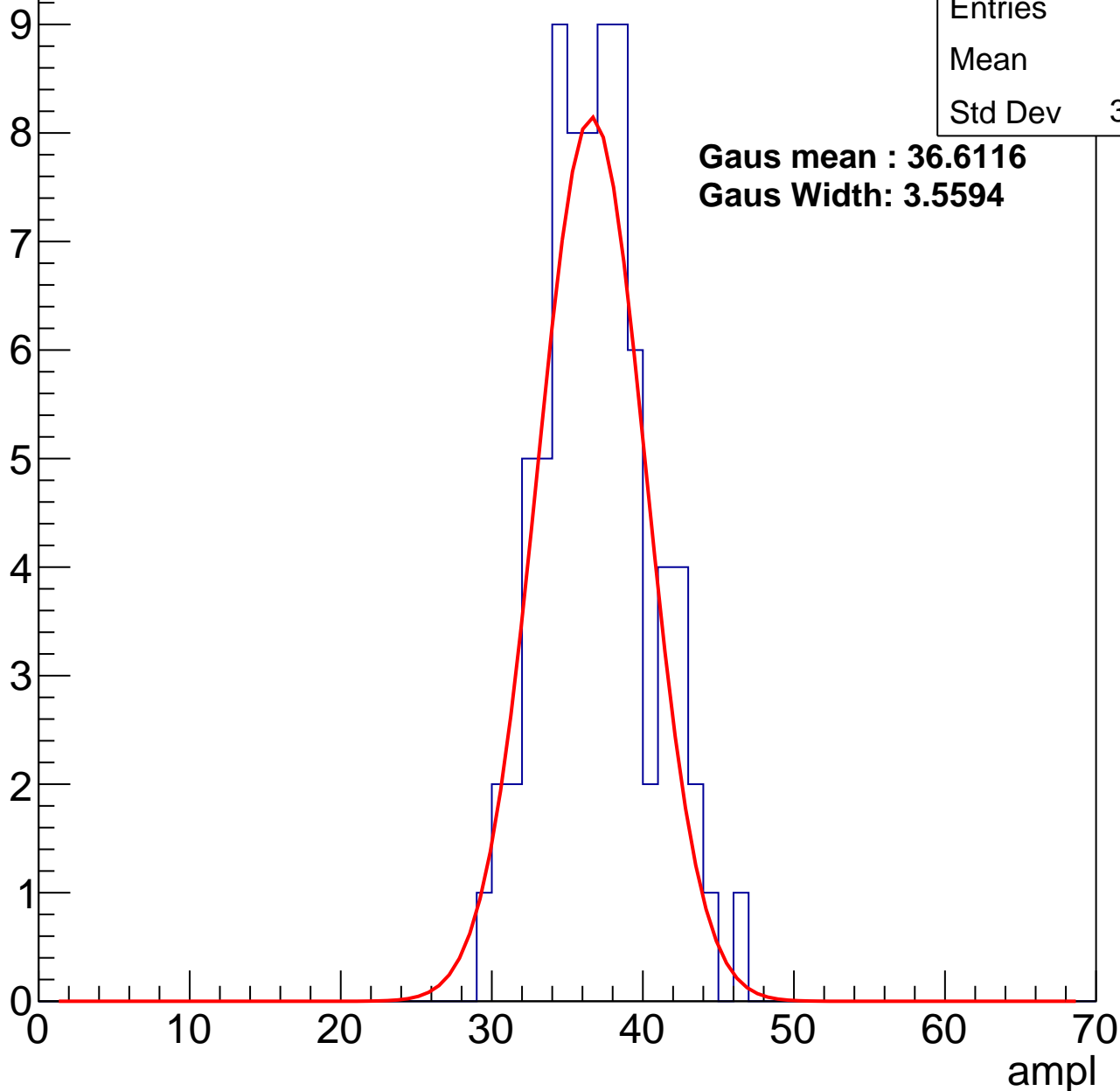
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	36.5
Std Dev	3.504

**Gaus mean : 36.6116**

**Gaus Width: 3.5594**



# B0L001S, U21-ch6, adc2

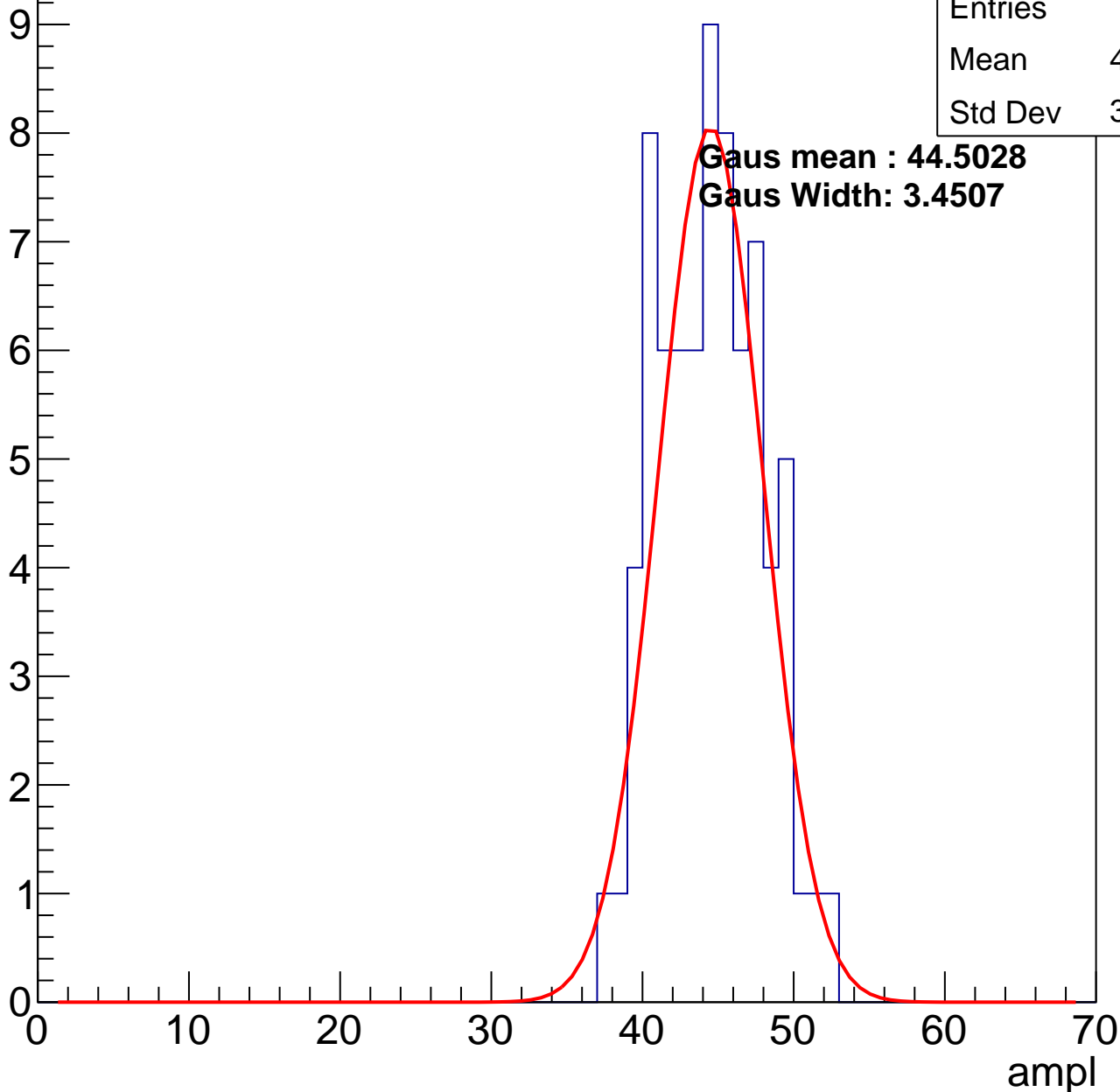
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	44.03
Std Dev	3.349

**Gaus mean : 44.5028**

**Gaus Width: 3.4507**

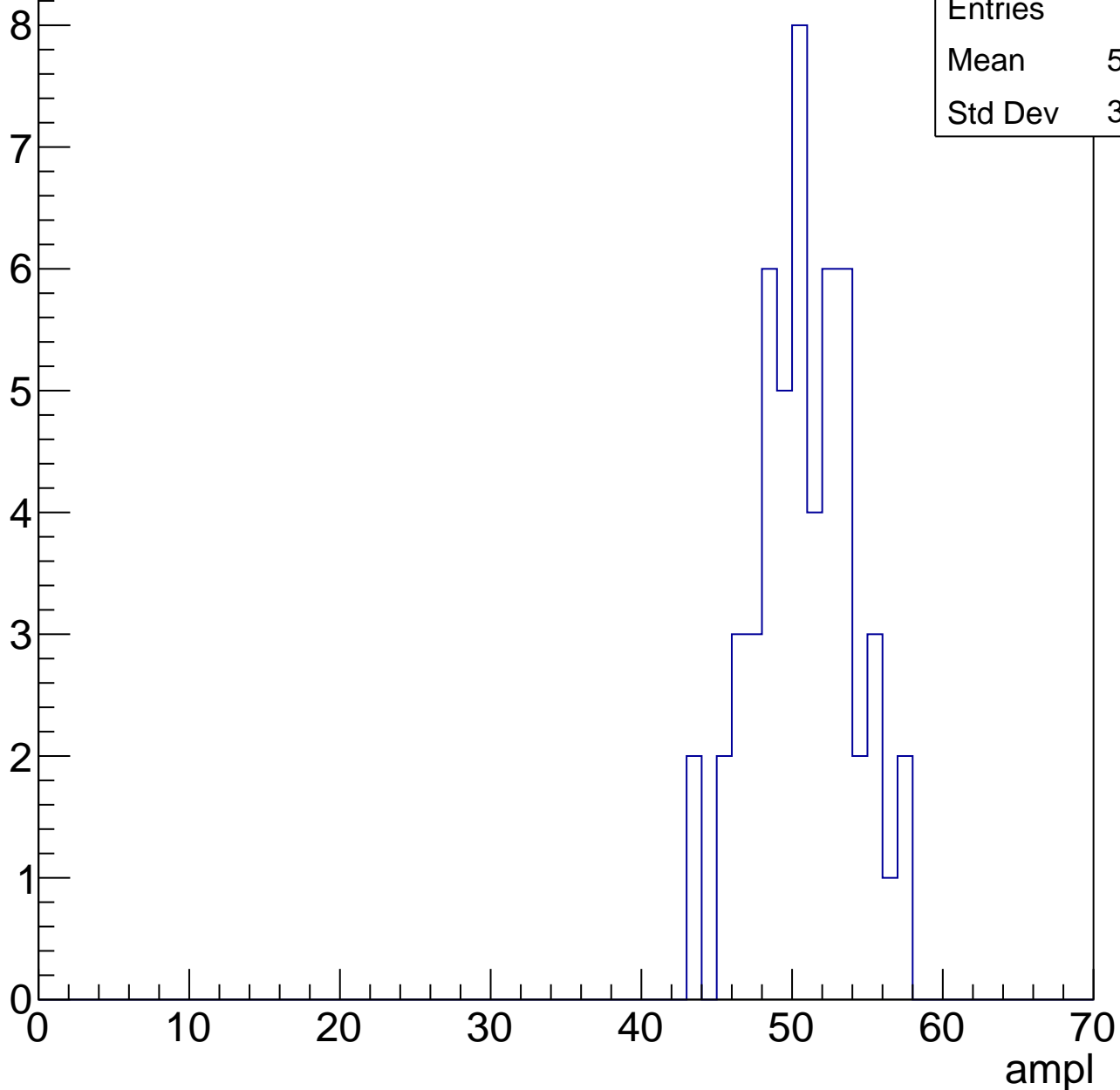


# B0L001S, U21-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

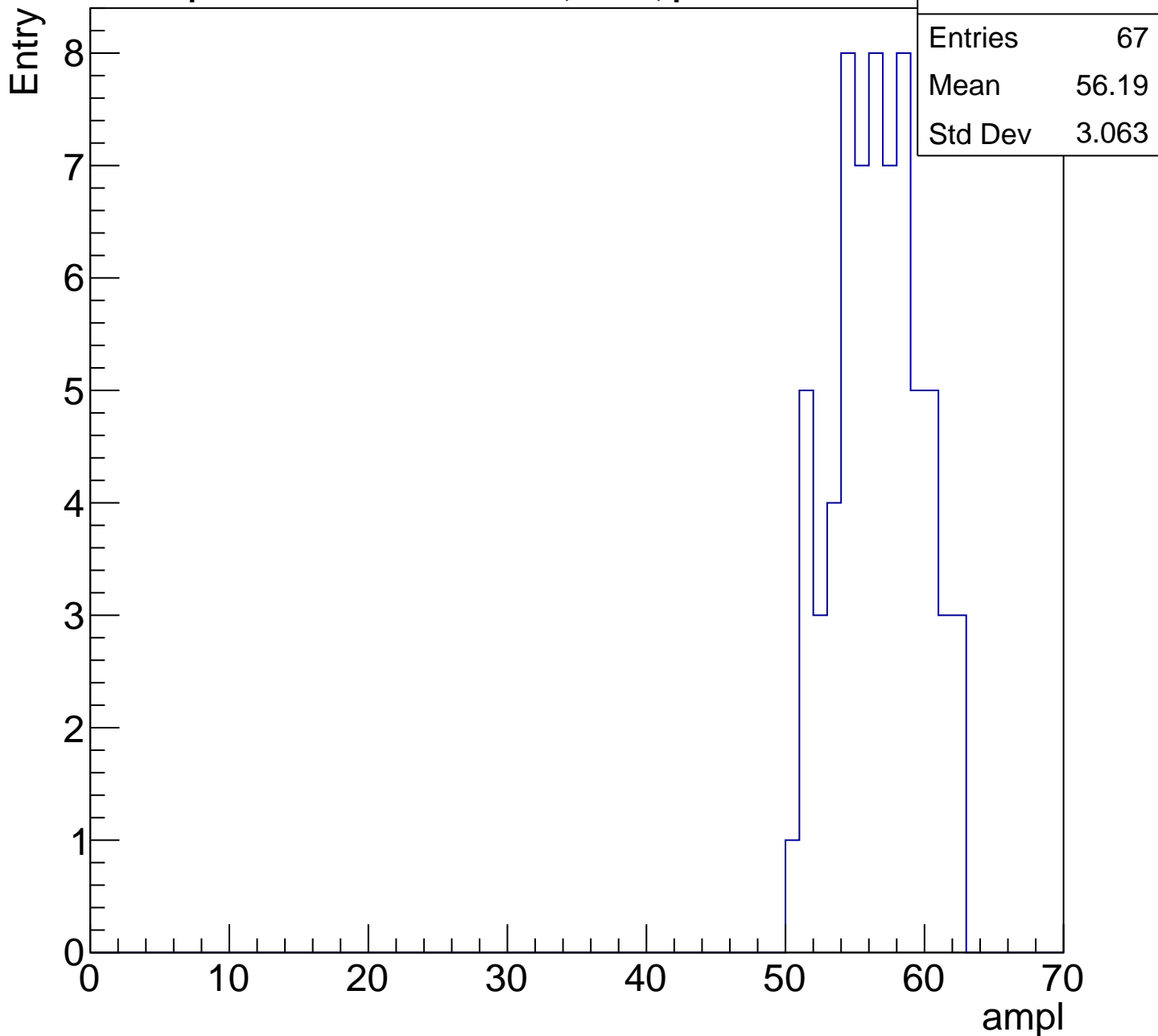
Entry

Entries	53
Mean	50.28
Std Dev	3.282



# B0L001S, U21-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

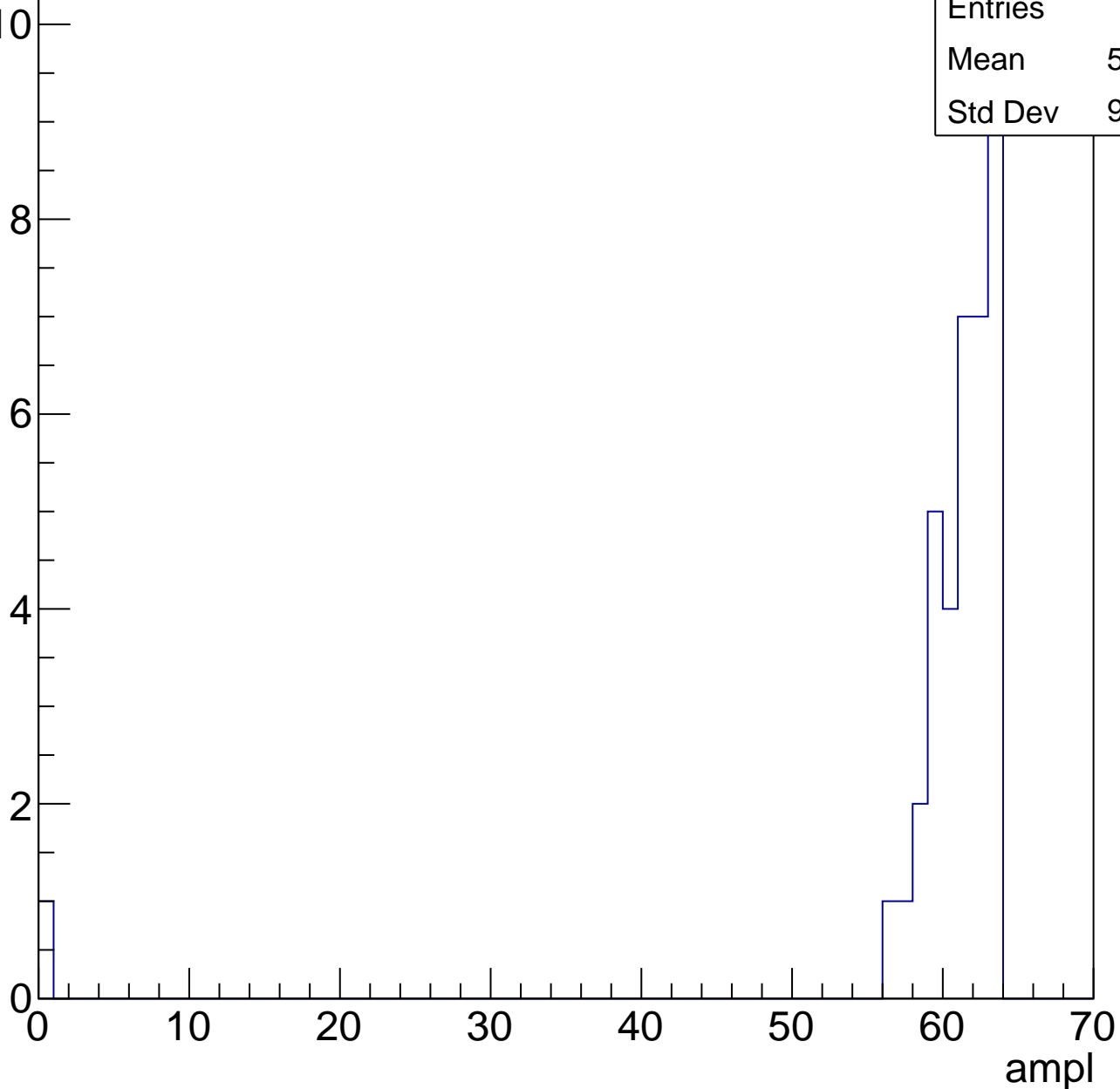


# B0L001S, U21-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	38
Mean	59.34
Std Dev	9.929



# B0L001S, U21-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	60
Std Dev	0



# B0L001S, U21-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	10.5
Std Dev	10.5

# B0L001S, U21-ch7, adc0

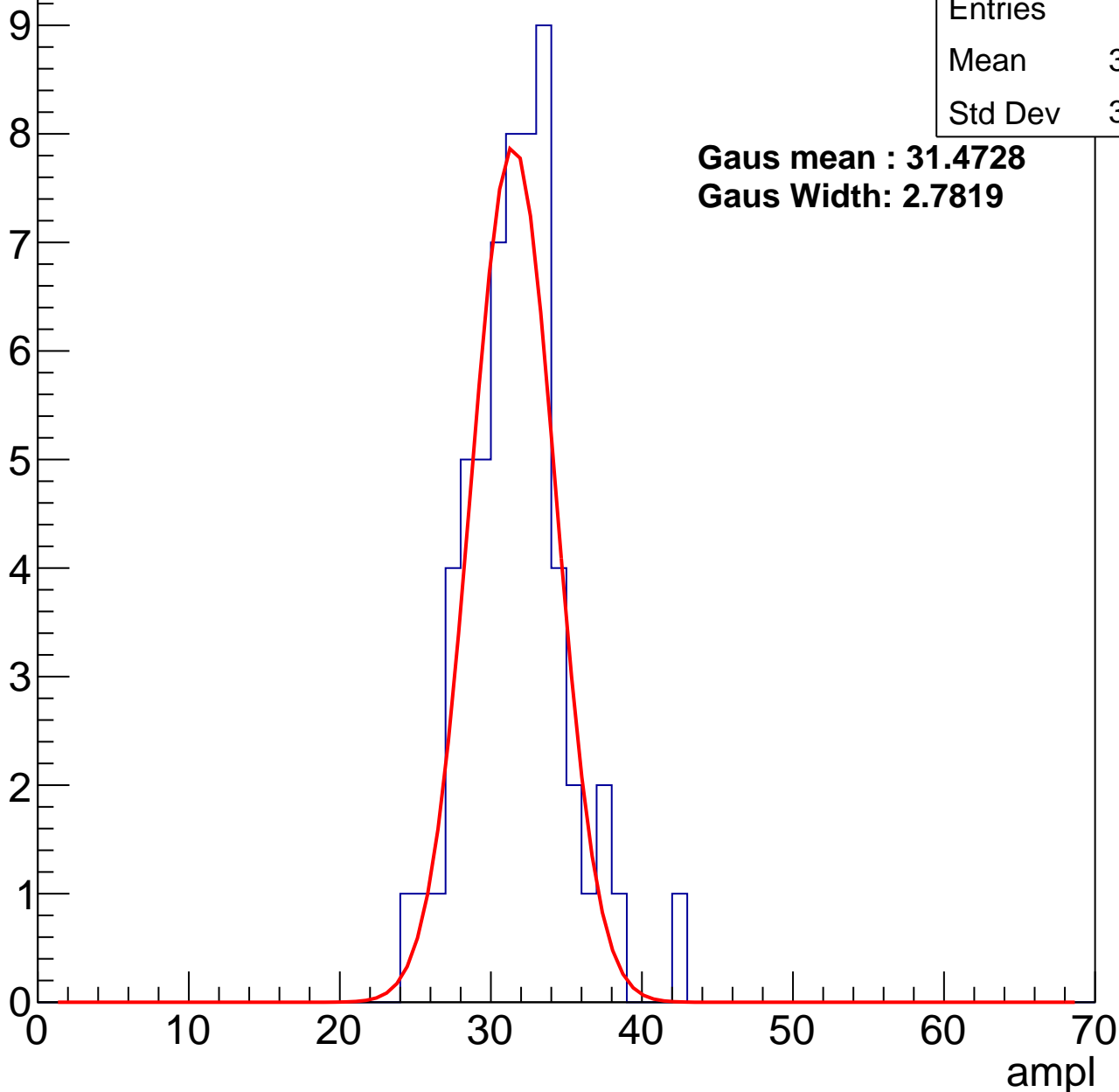
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	31.25
Std Dev	3.218

**Gaus mean : 31.4728**

**Gaus Width: 2.7819**



# B0L001S, U21-ch7, adc1

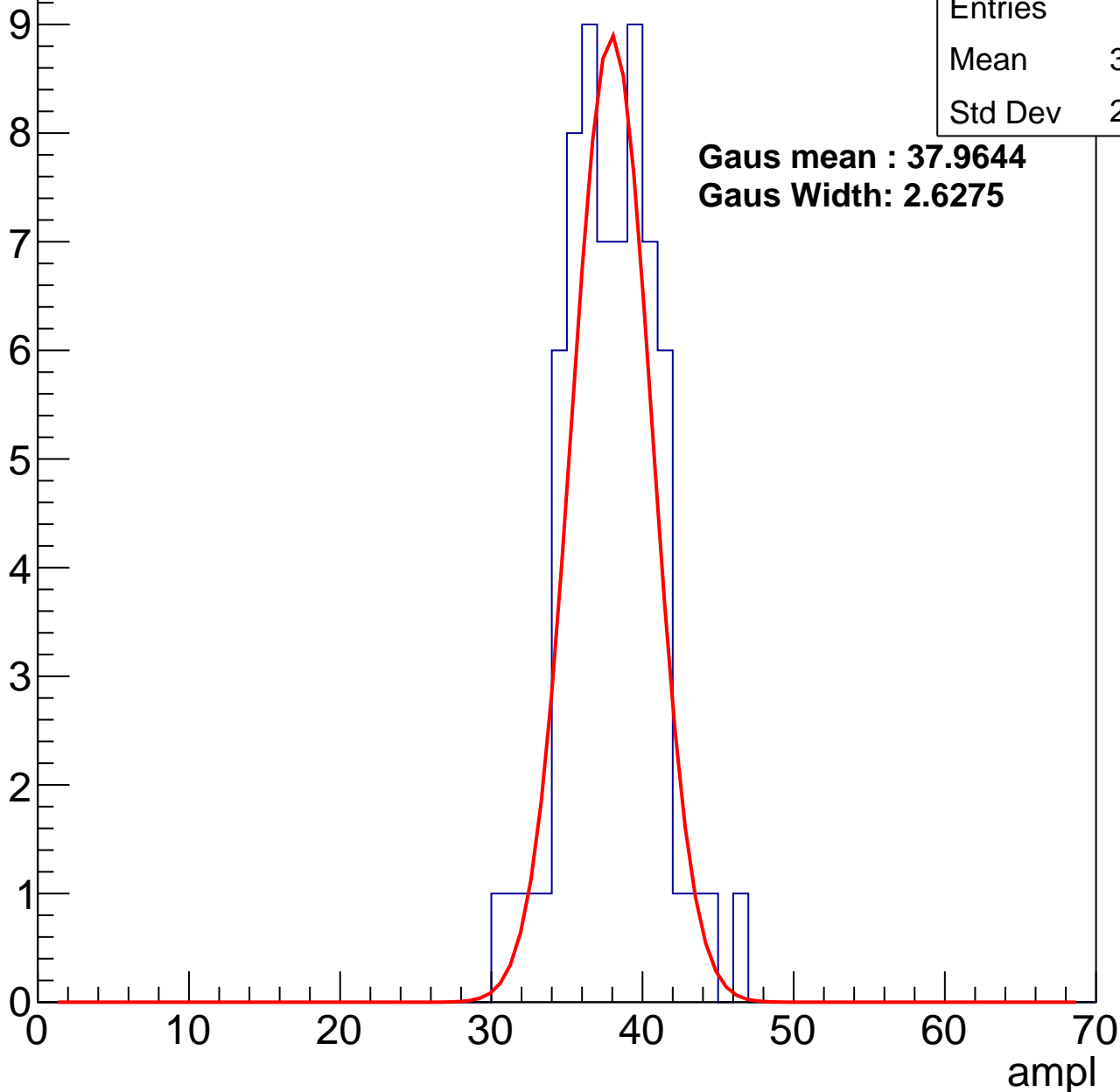
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	37.48
Std Dev	2.989

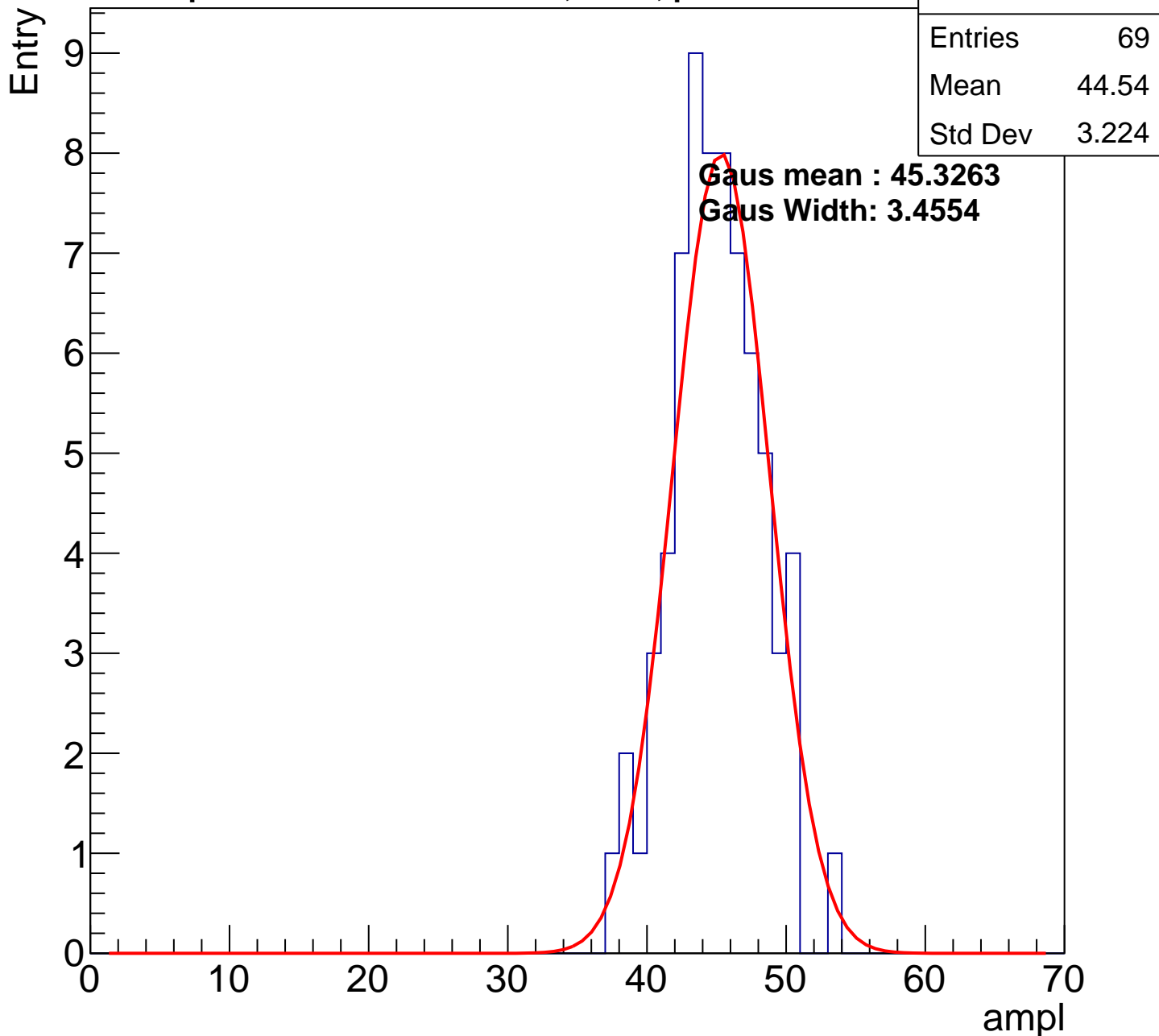
**Gaus mean : 37.9644**

**Gaus Width: 2.6275**



# B0L001S, U21-ch7, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

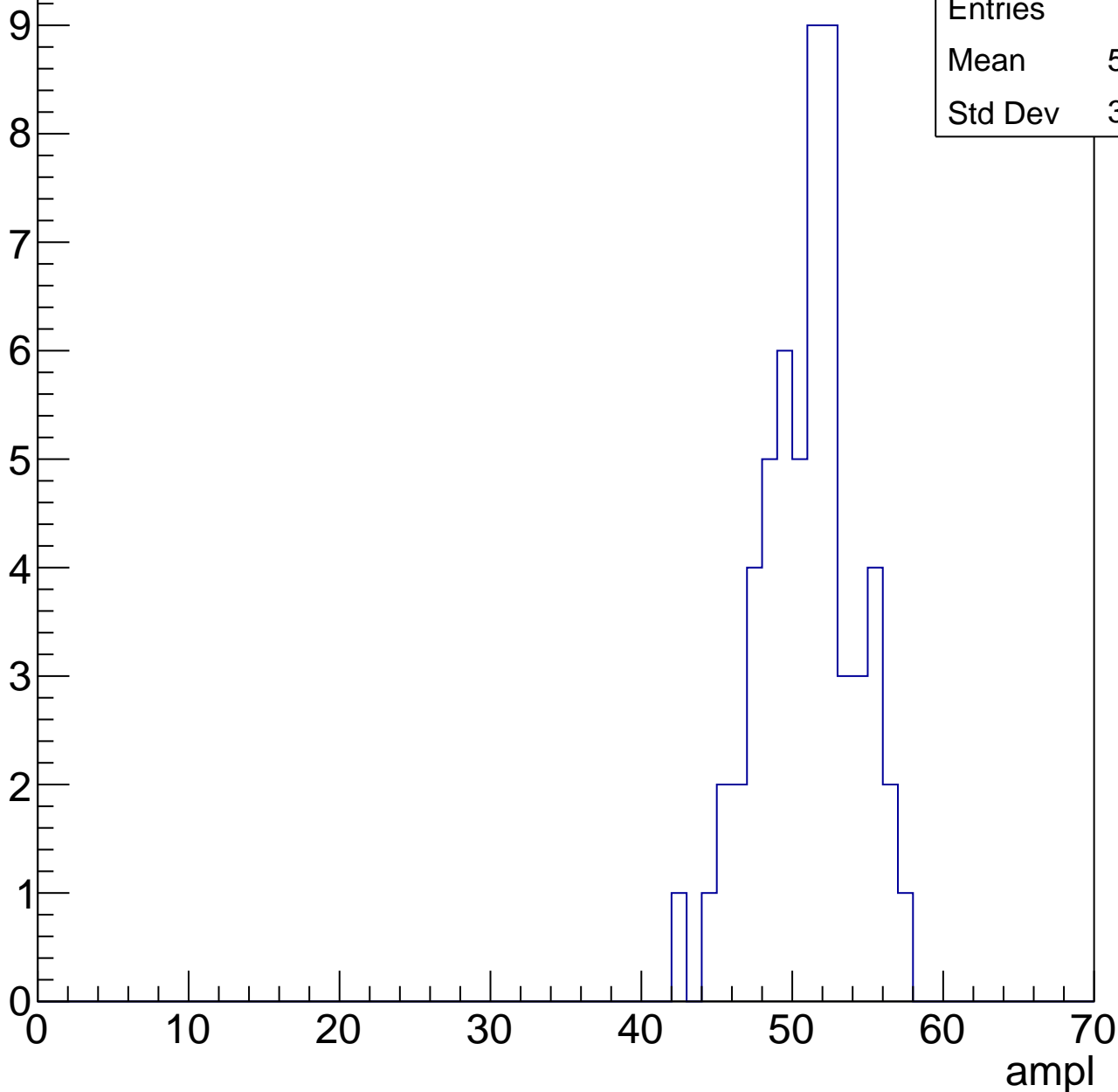


# B0L001S, U21-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	50.47
Std Dev	3.168

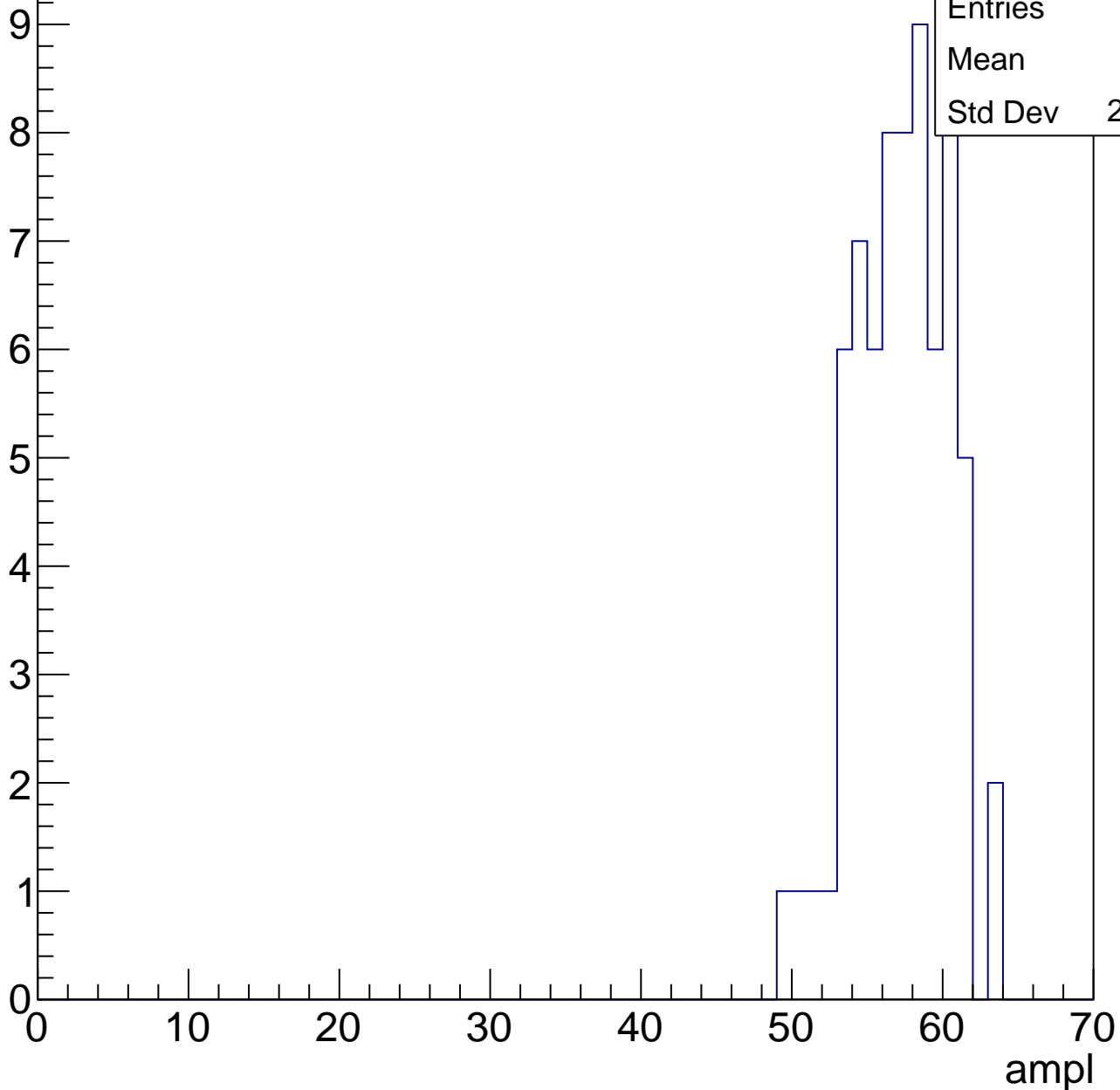


# B0L001S, U21-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	56.8
Std Dev	2.996

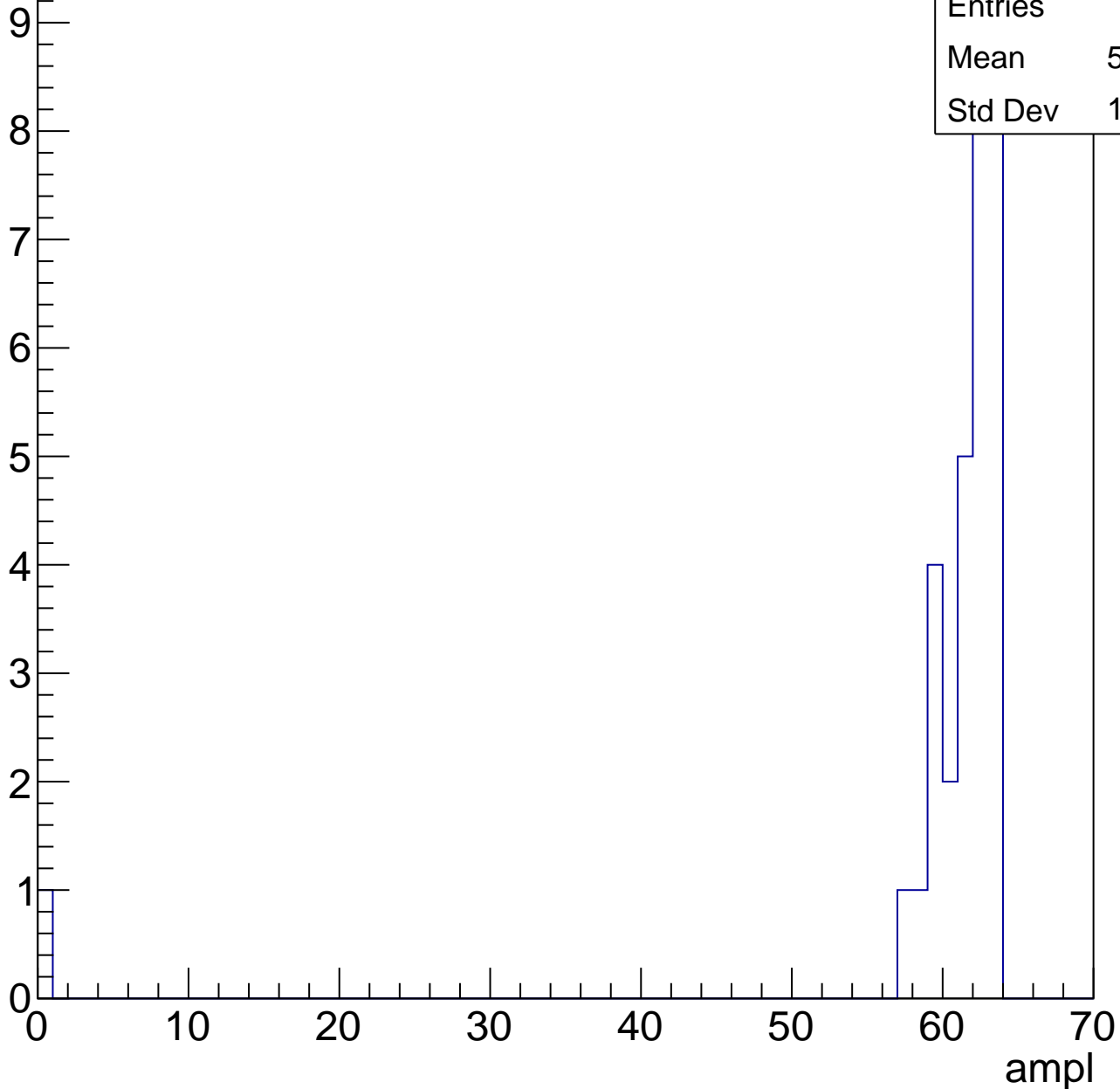


# B0L001S, U21-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	31
Mean	59.29
Std Dev	10.95



# B0L001S, U21-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U21-ch8, adc0

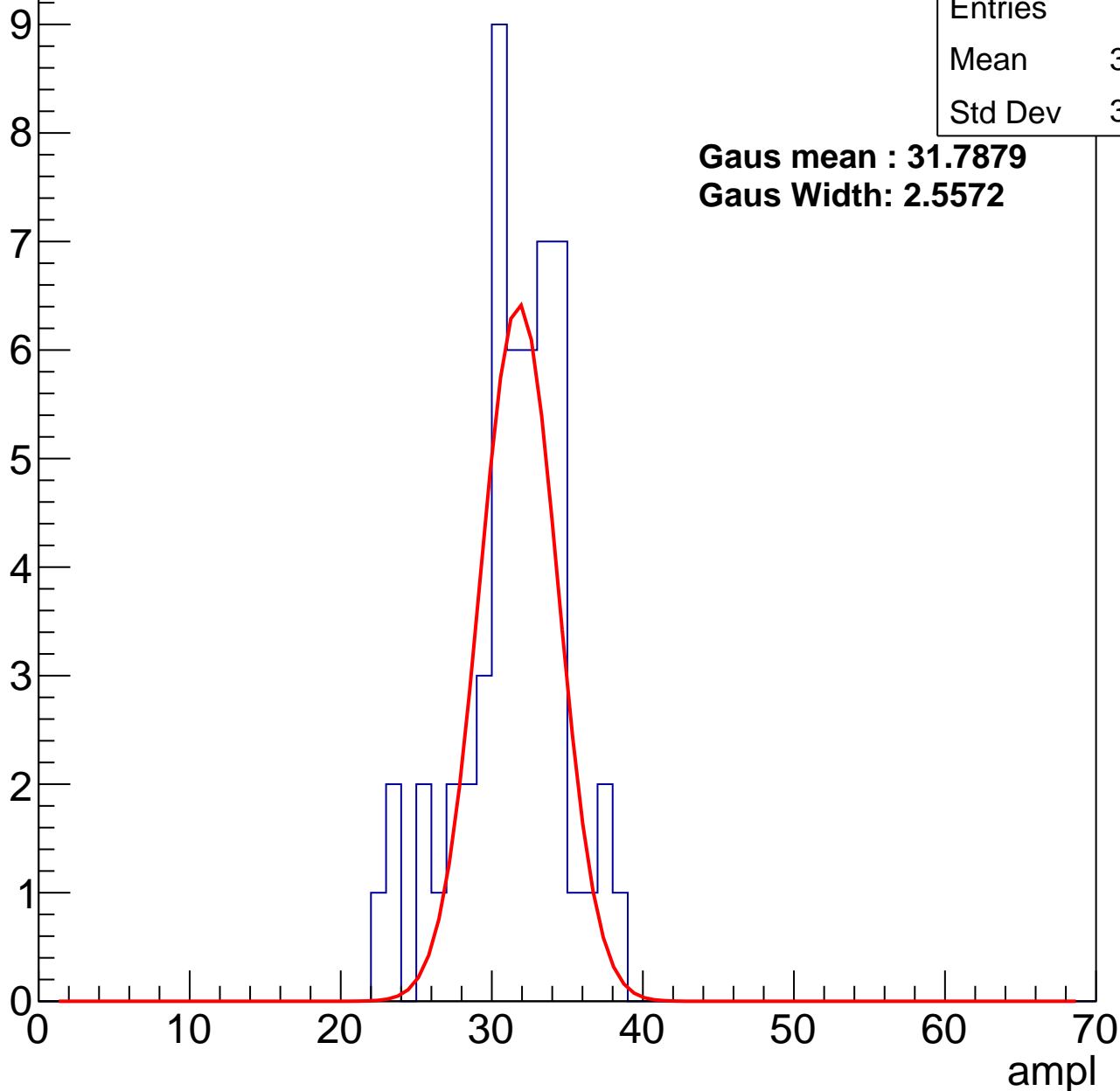
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	30.96
Std Dev	3.464

**Gaus mean : 31.7879**

**Gaus Width: 2.5572**



# B0L001S, U21-ch8, adc1

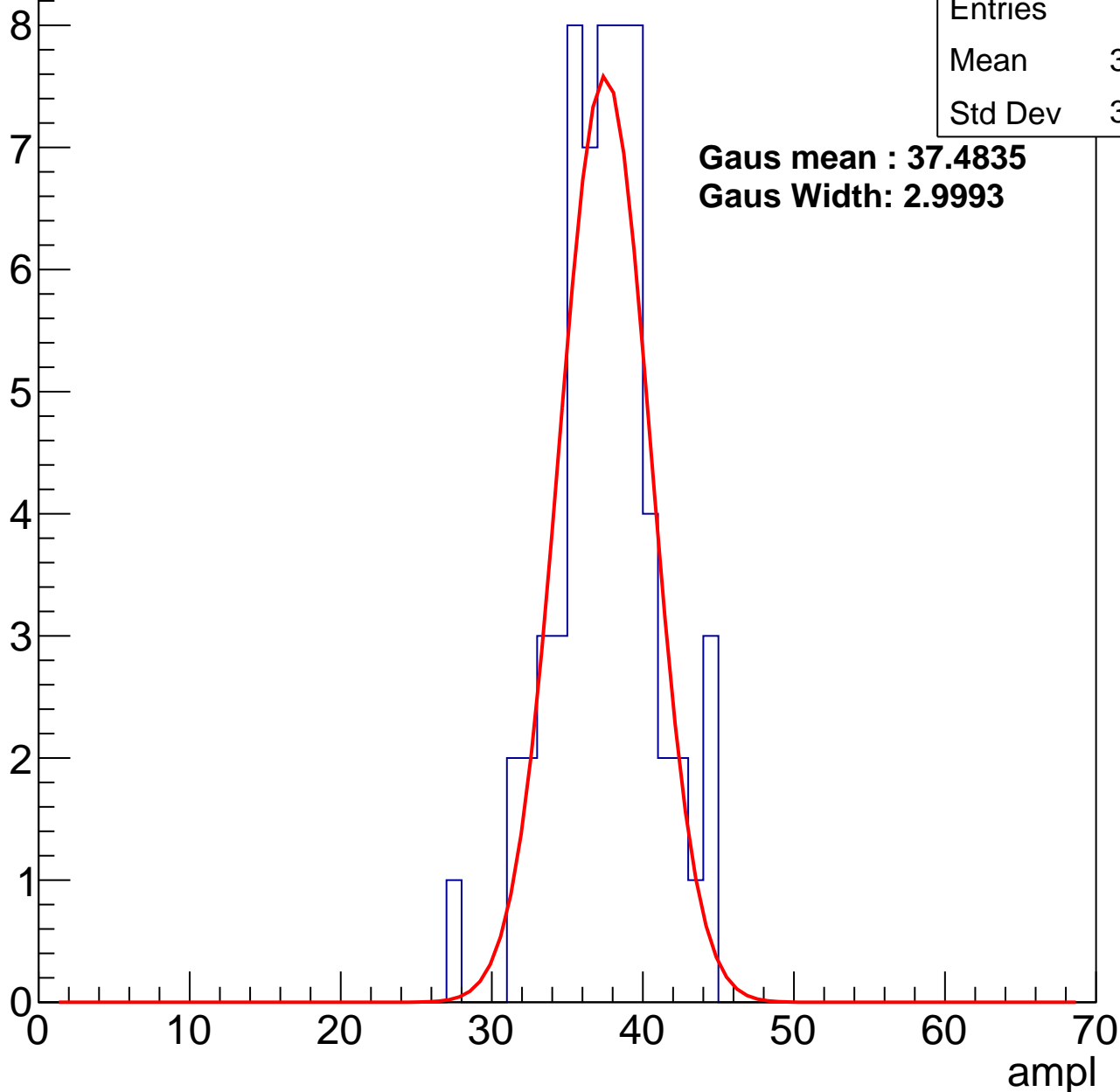
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	37.08
Std Dev	3.303

**Gaus mean : 37.4835**

**Gaus Width: 2.9993**



# B0L001S, U21-ch8, adc2

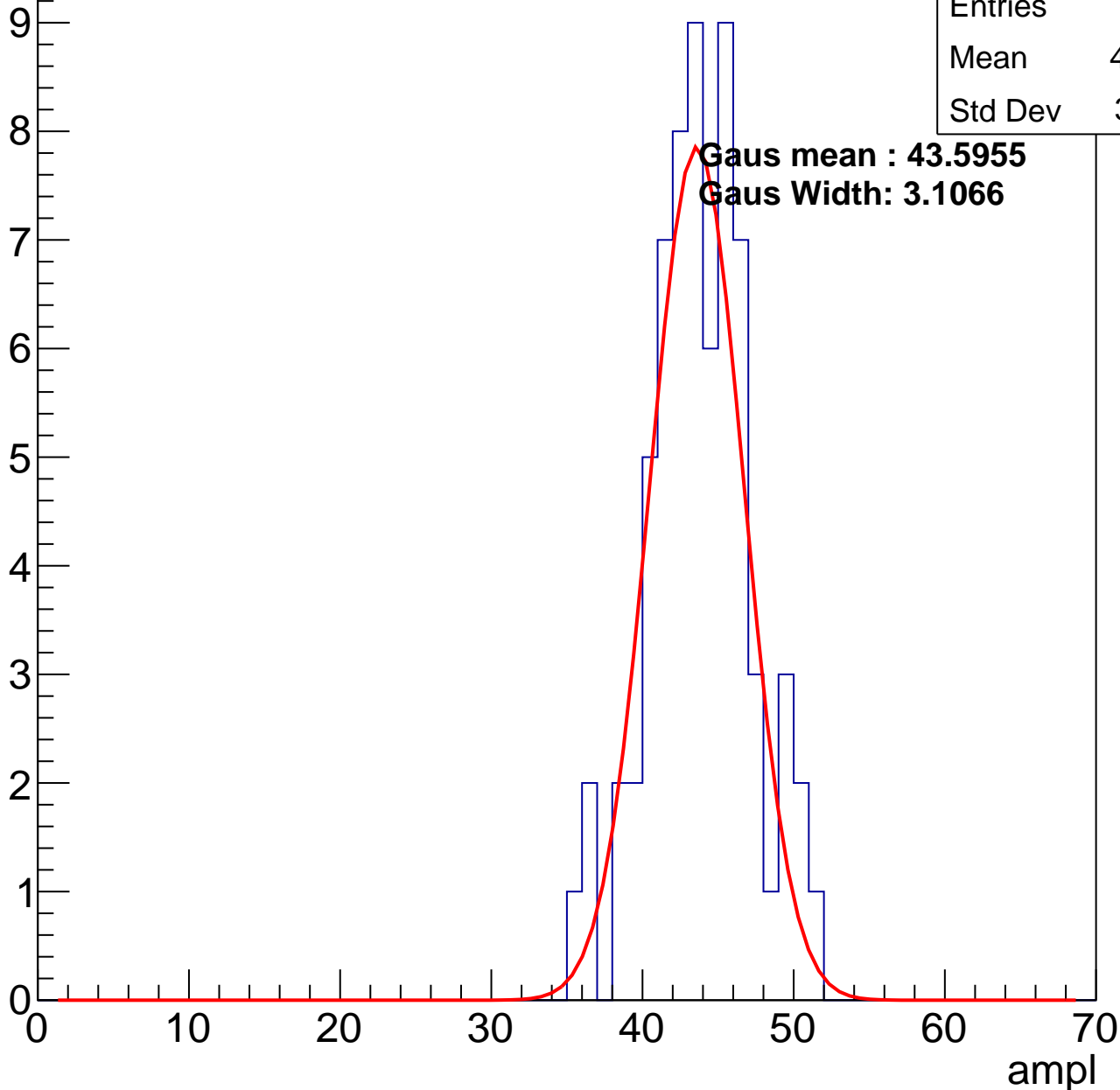
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	43.37
Std Dev	3.351

**Gaus mean : 43.5955**

**Gaus Width: 3.1066**

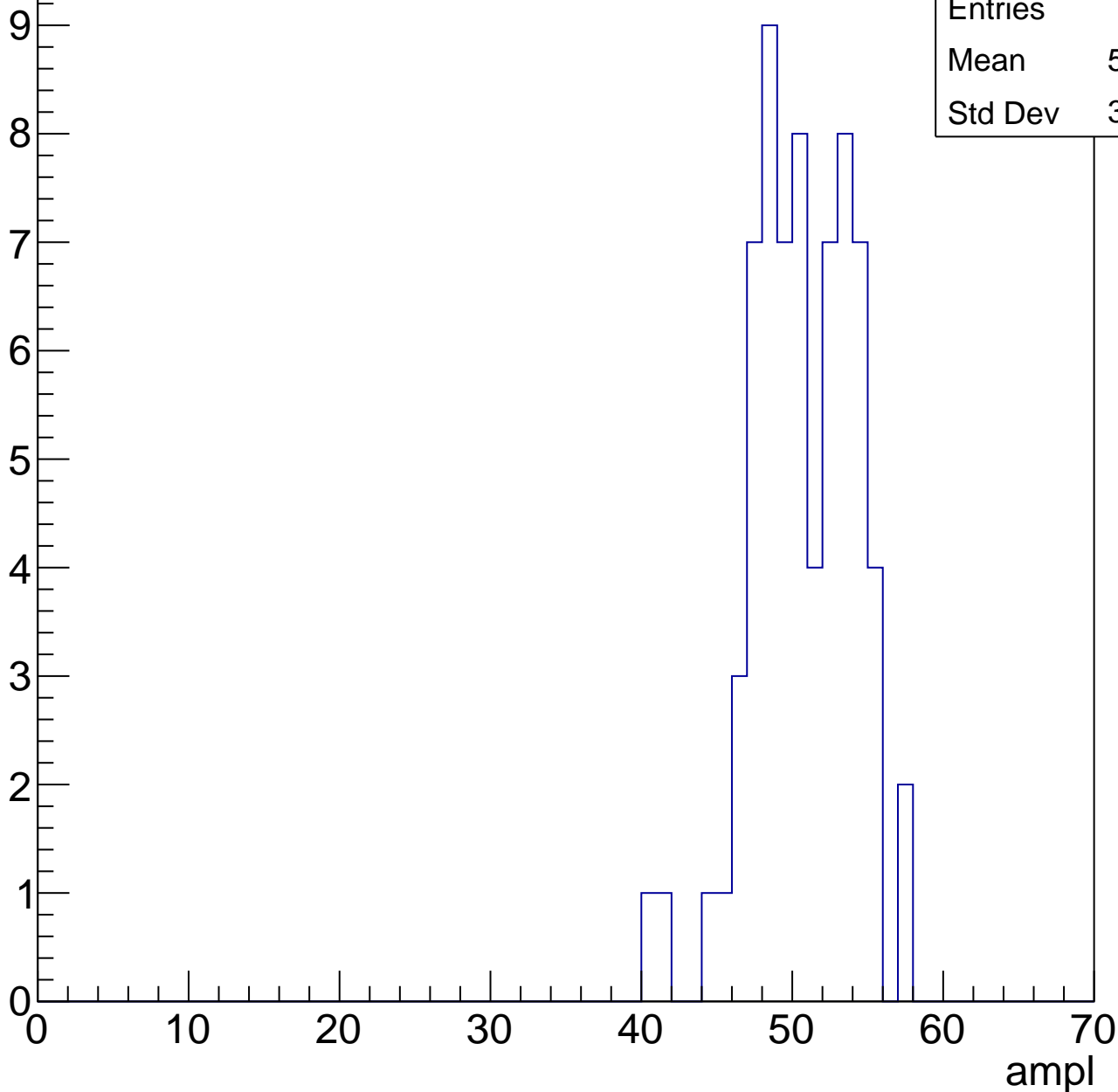


# B0L001S, U21-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

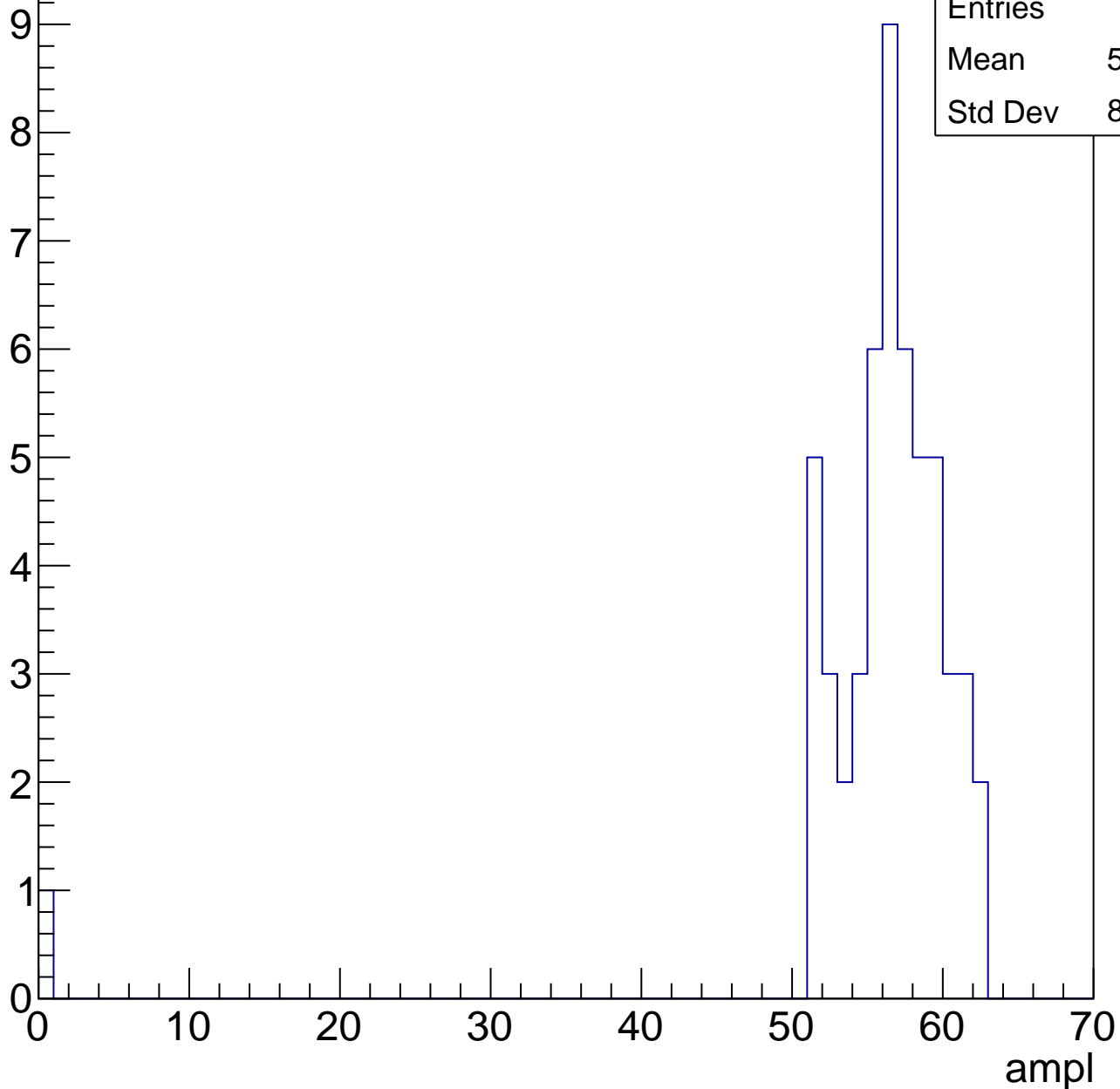
Entries	70
Mean	50.23
Std Dev	3.394



# B0L001S, U21-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	45
Mean	60.49
Std Dev	1.985

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

7

8

9

# B0L001S, U21-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U21-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch9, adc0

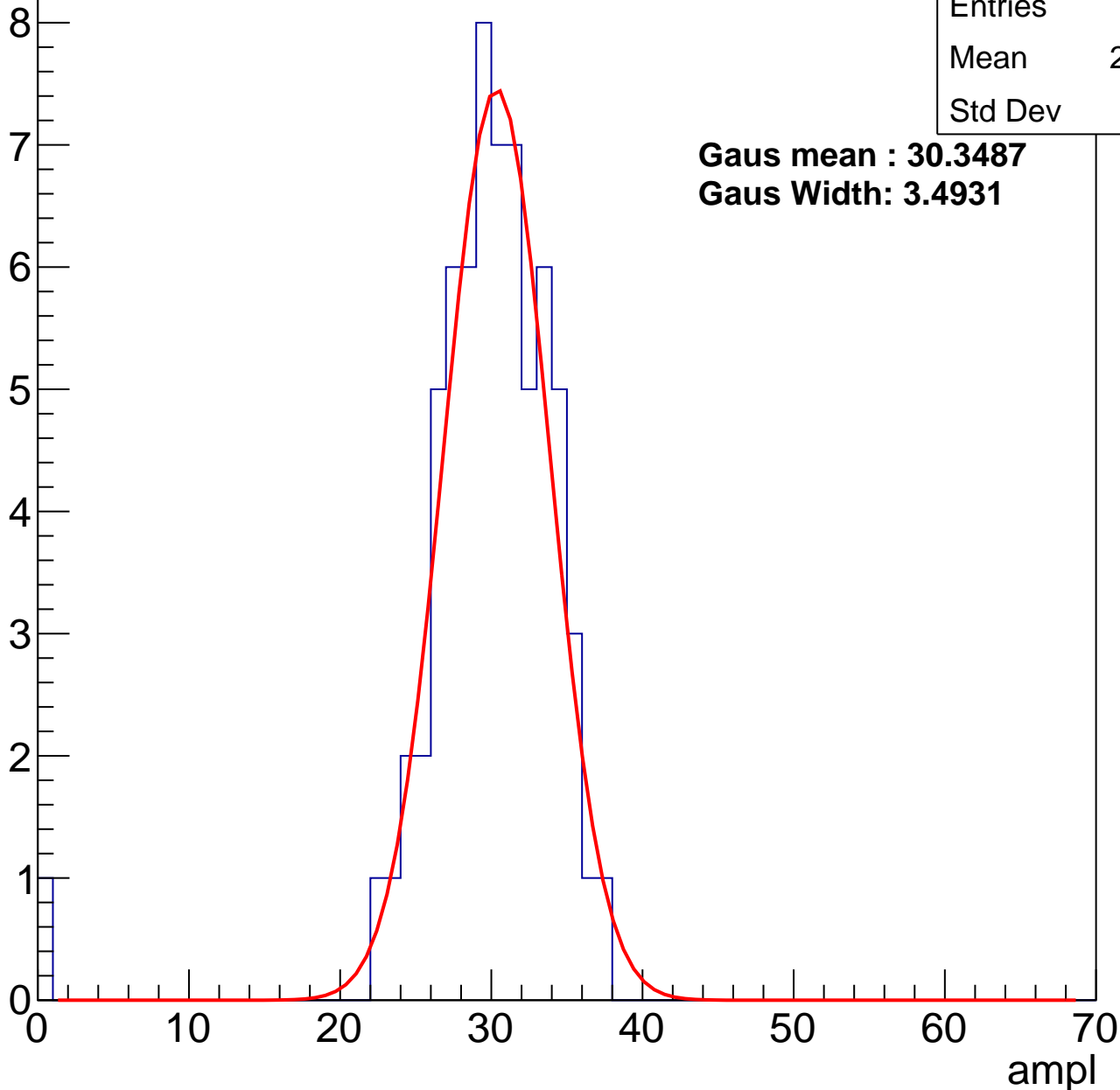
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	29.37
Std Dev	4.88

**Gaus mean : 30.3487**

**Gaus Width: 3.4931**



# B0L001S, U21-ch9, adc1

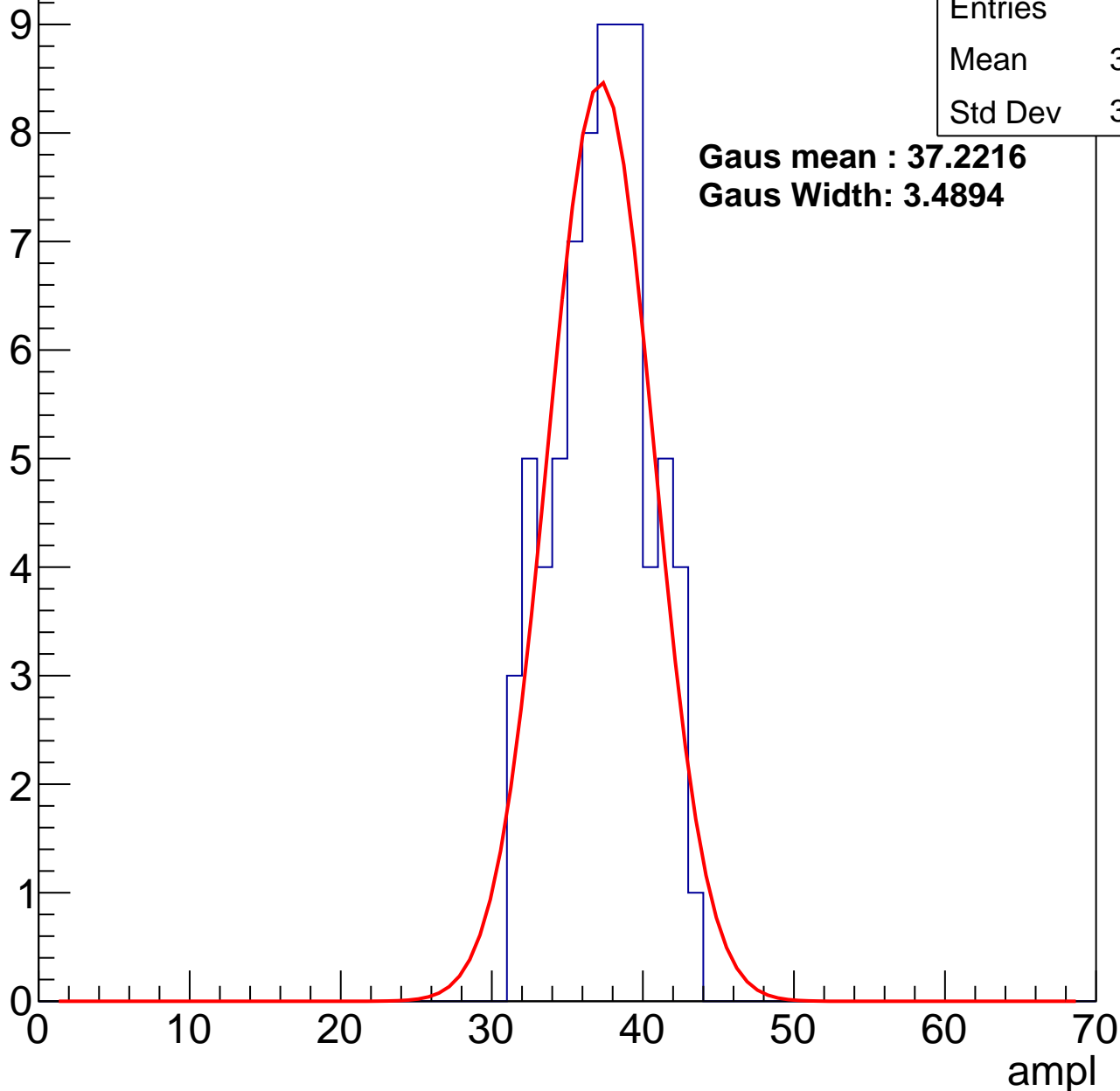
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	36.85
Std Dev	3.037

**Gaus mean : 37.2216**

**Gaus Width: 3.4894**



# B0L001S, U21-ch9, adc2

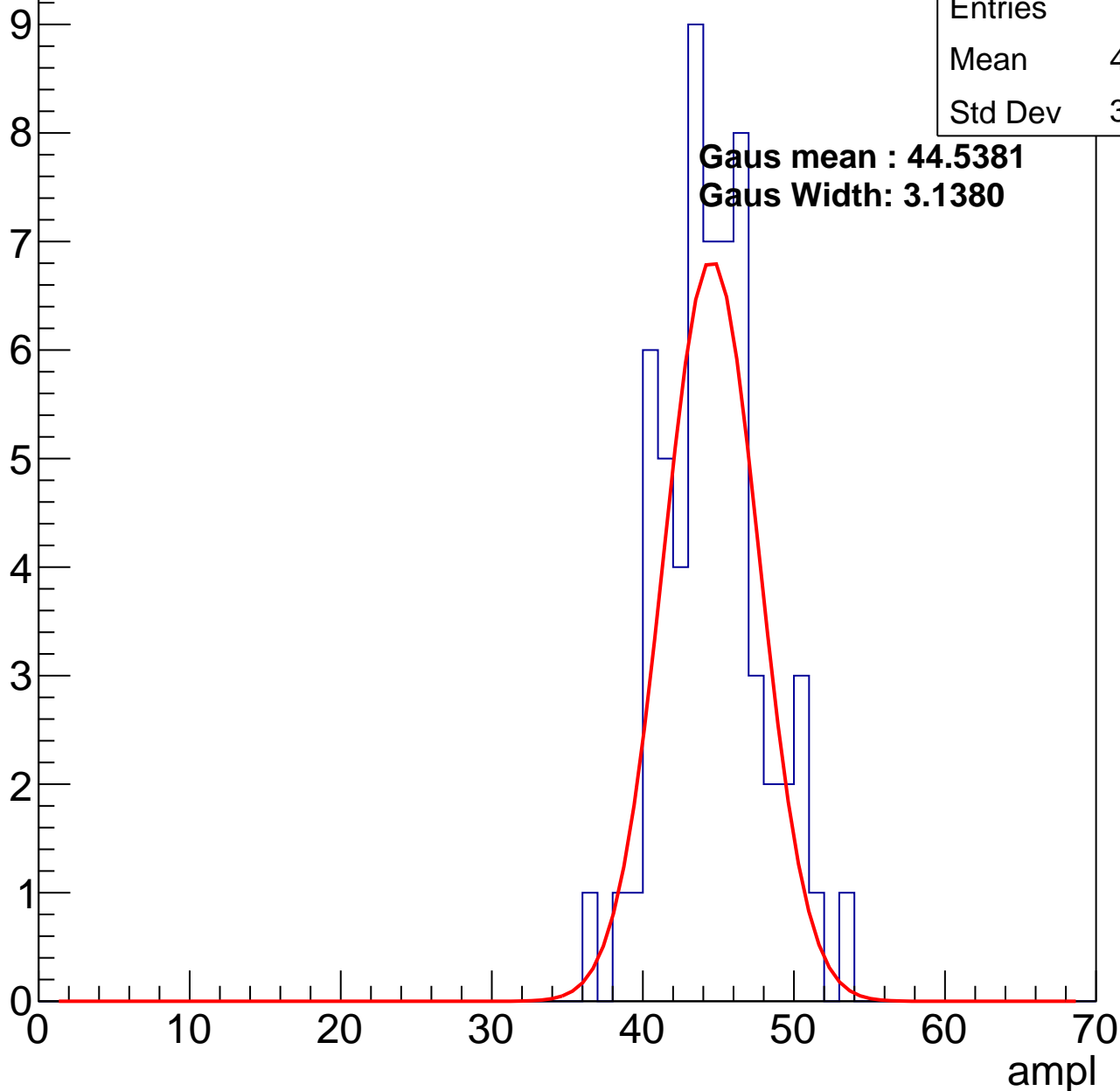
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	44.15
Std Dev	3.328

**Gaus mean : 44.5381**

**Gaus Width: 3.1380**

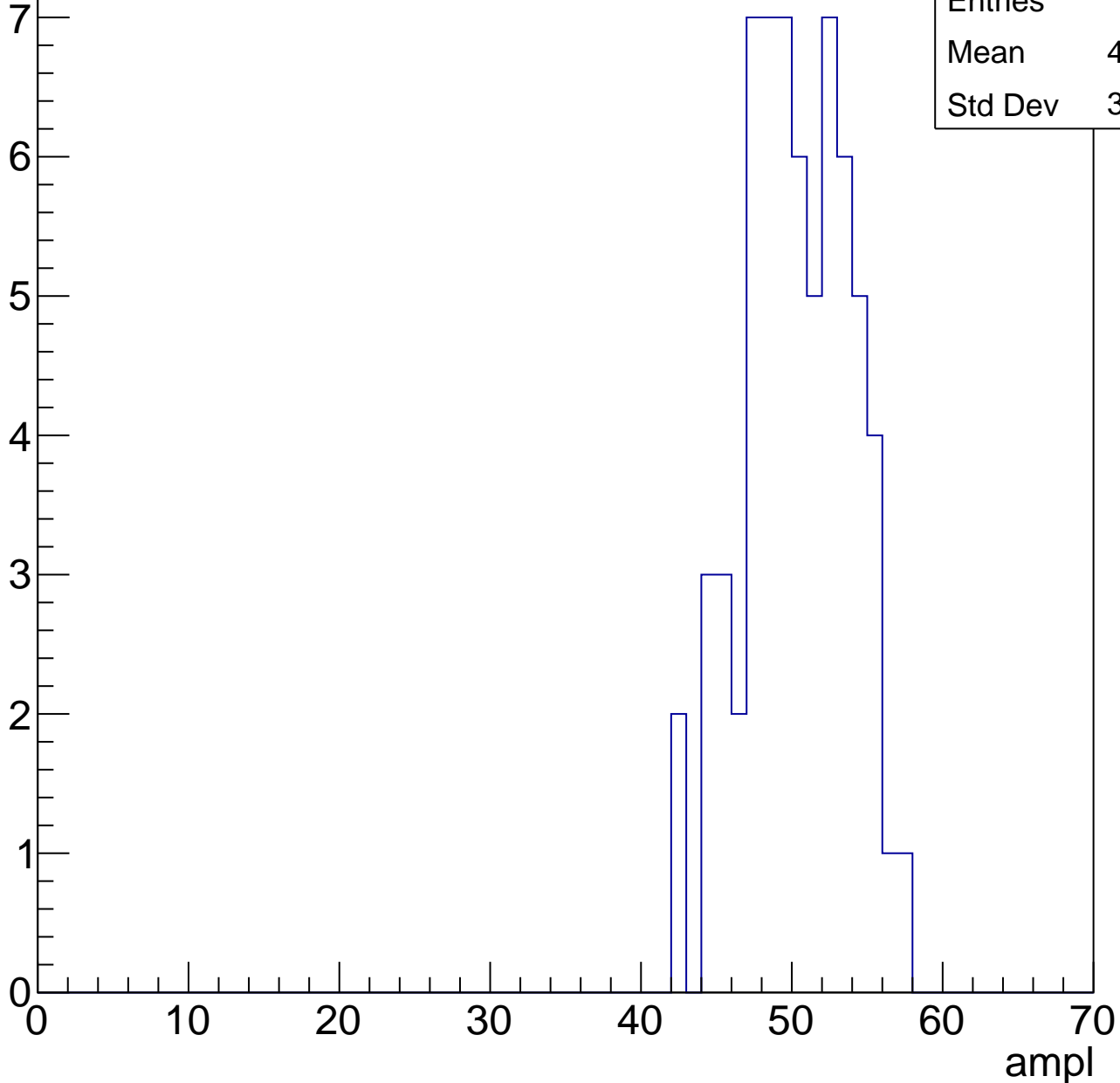


# B0L001S, U21-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	49.86
Std Dev	3.464

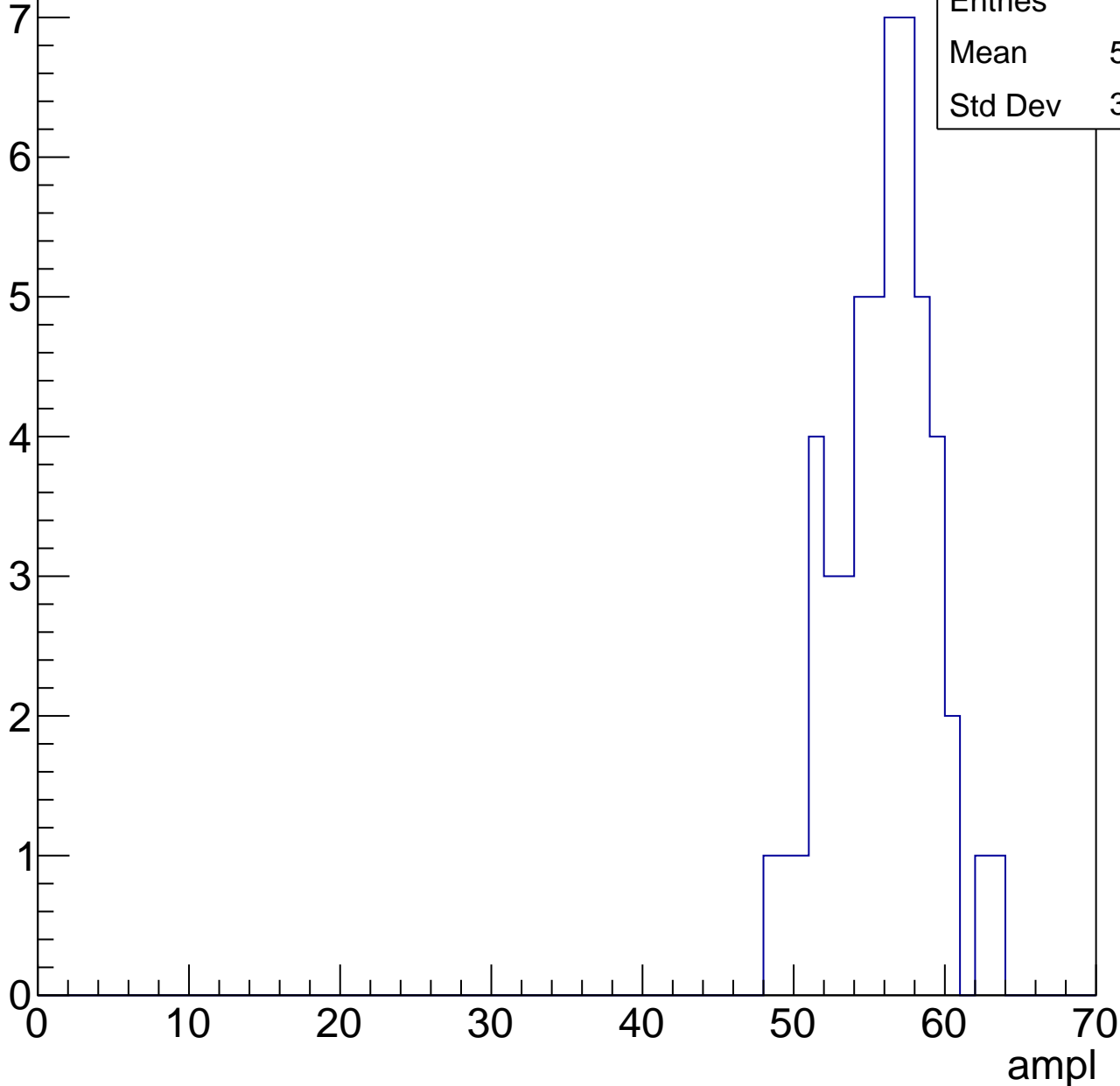


# B0L001S, U21-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	55.46
Std Dev	3.208

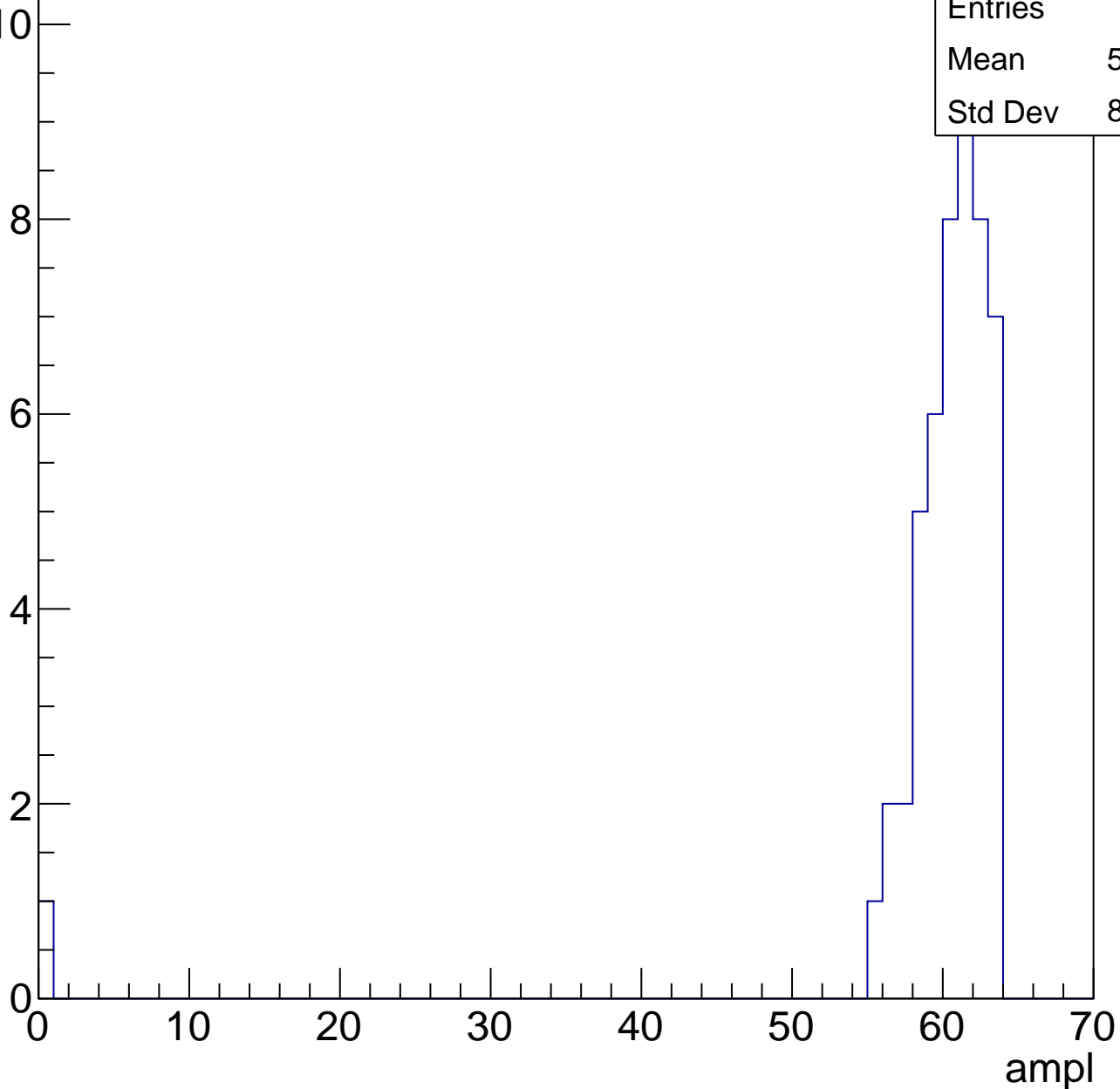


# B0L001S, U21-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	59.04
Std Dev	8.672



# B0L001S, U21-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U21-ch10, adc0

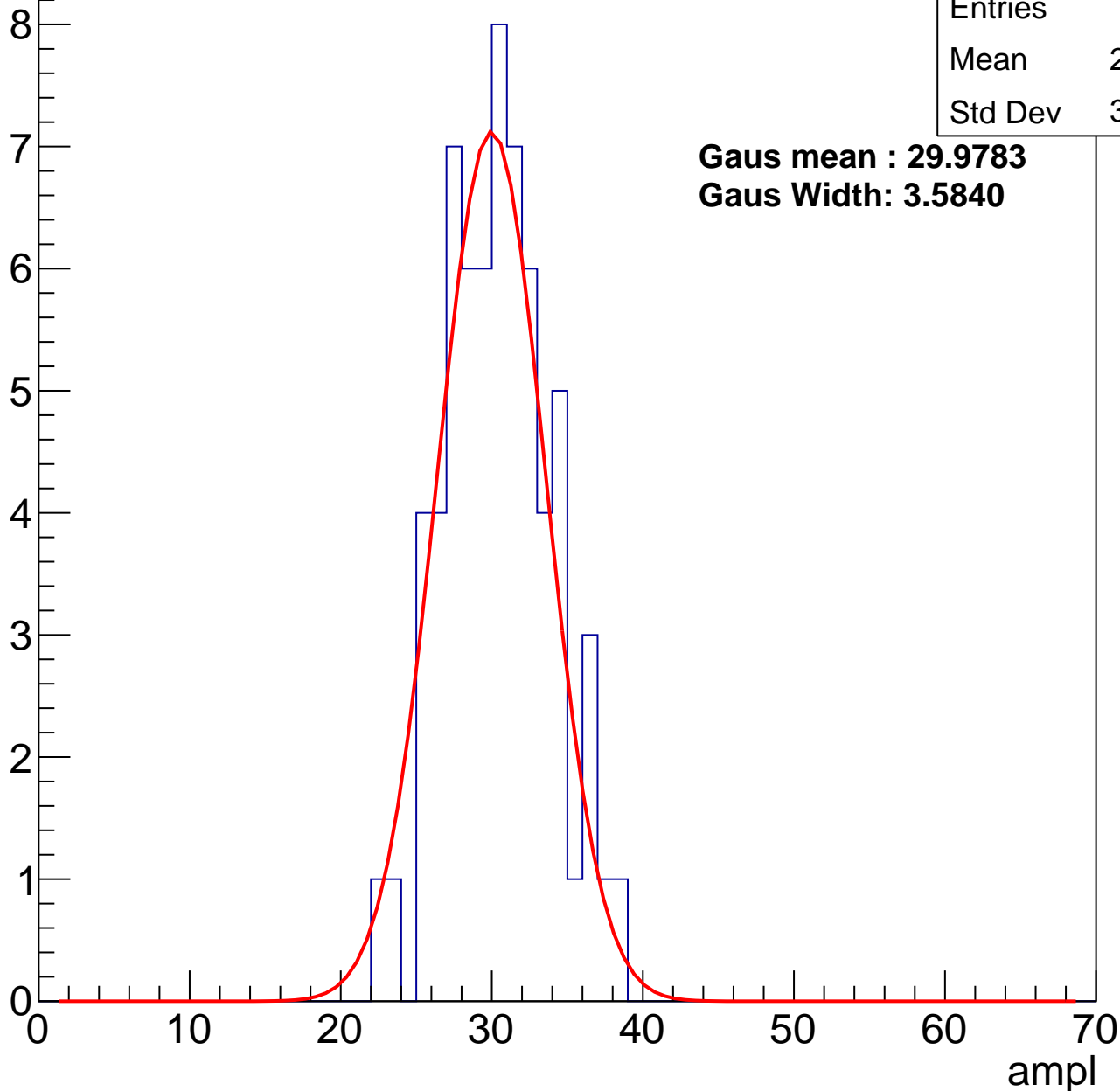
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	29.98
Std Dev	3.426

**Gaus mean : 29.9783**

**Gaus Width: 3.5840**



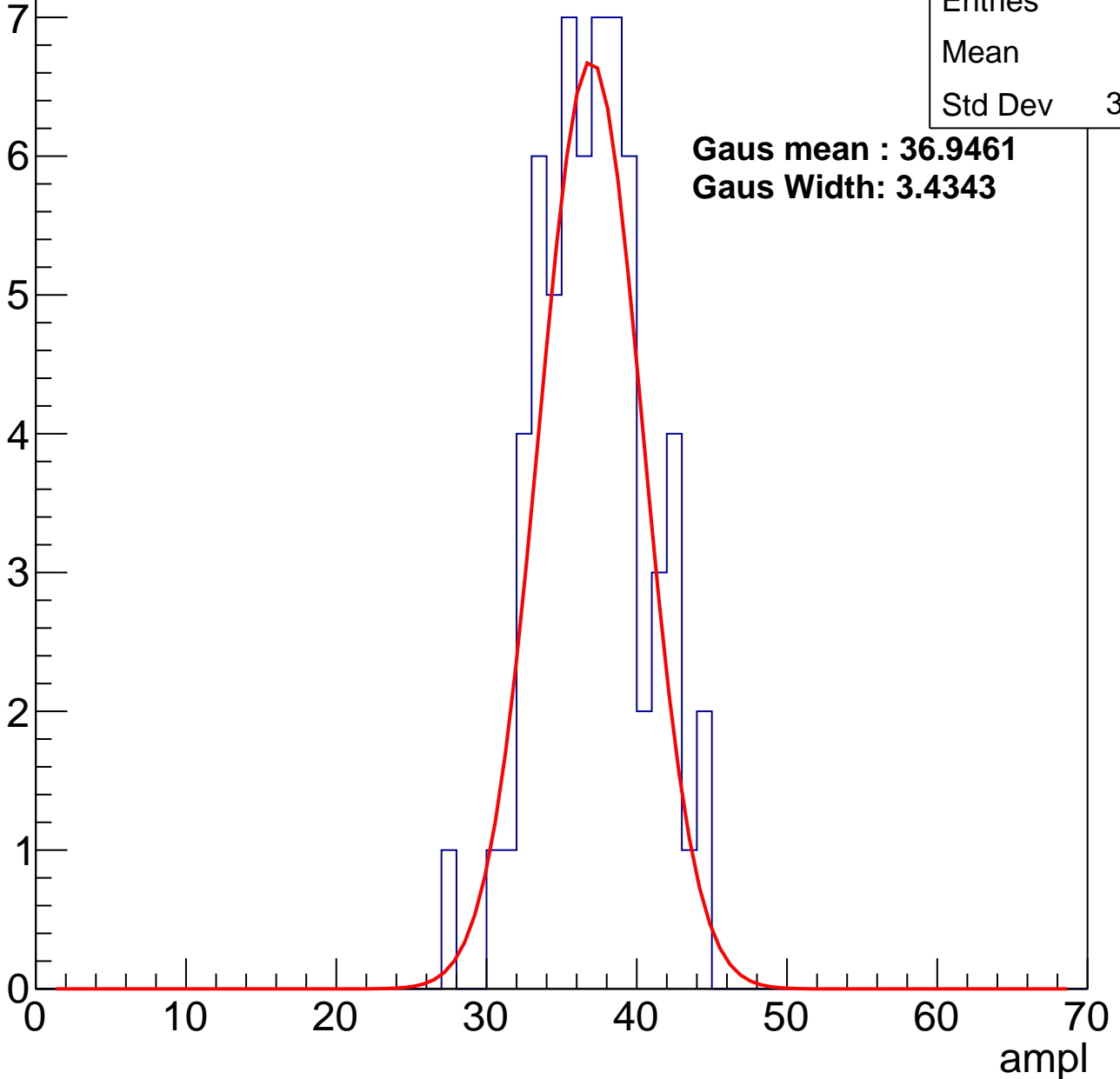
# B0L001S, U21-ch10, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	36.6
Std Dev	3.521

**Gaus mean : 36.9461**  
**Gaus Width: 3.4343**



# B0L001S, U21-ch10, adc2

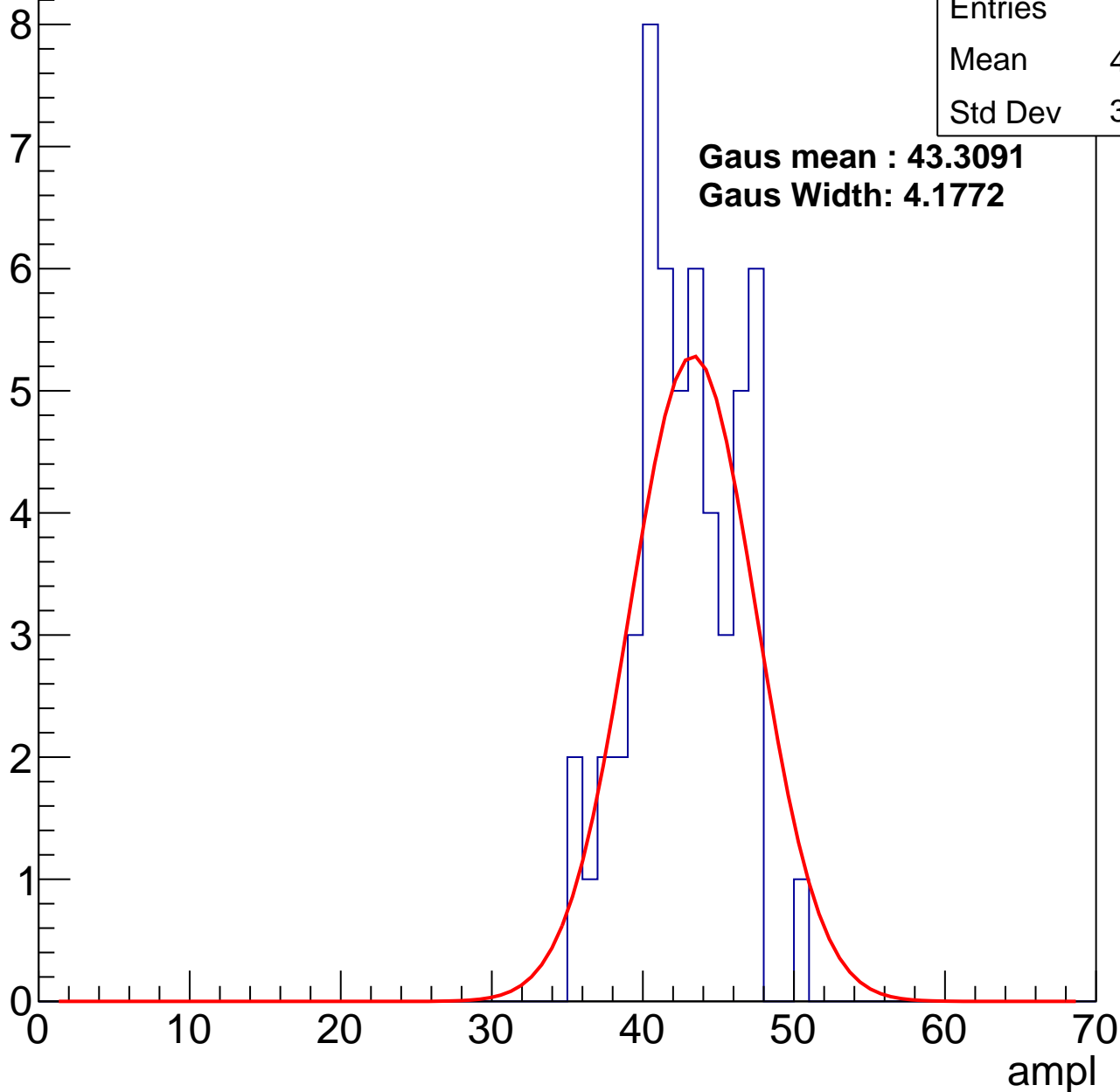
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	42.22
Std Dev	3.392

**Gaus mean : 43.3091**

**Gaus Width: 4.1772**

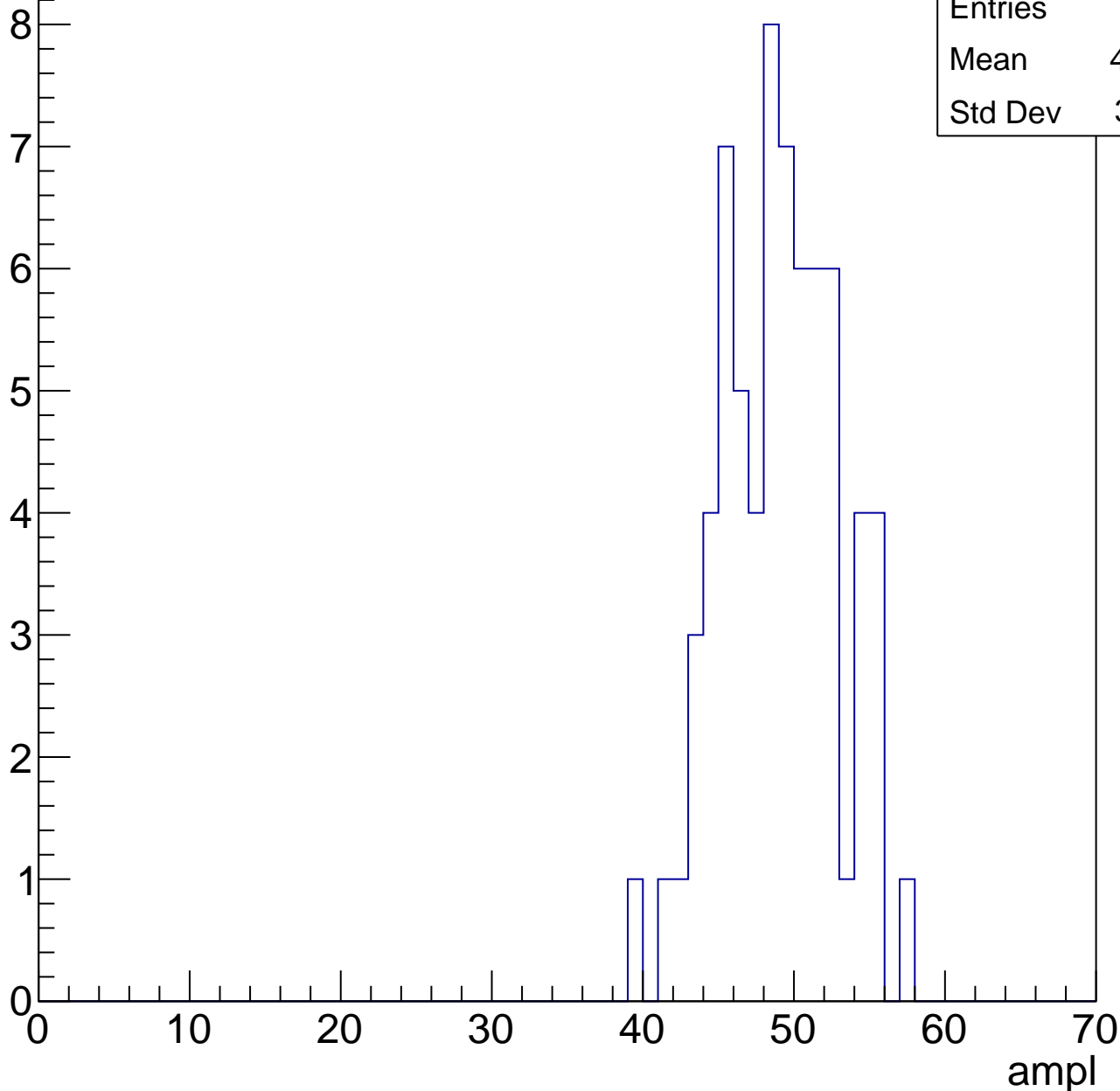


# B0L001S, U21-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	48.57
Std Dev	3.801



# B0L001S, U21-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	70
Mean	55.27
Std Dev	3.66

Entry

10

8

6

4

2

0

0

10

20

30

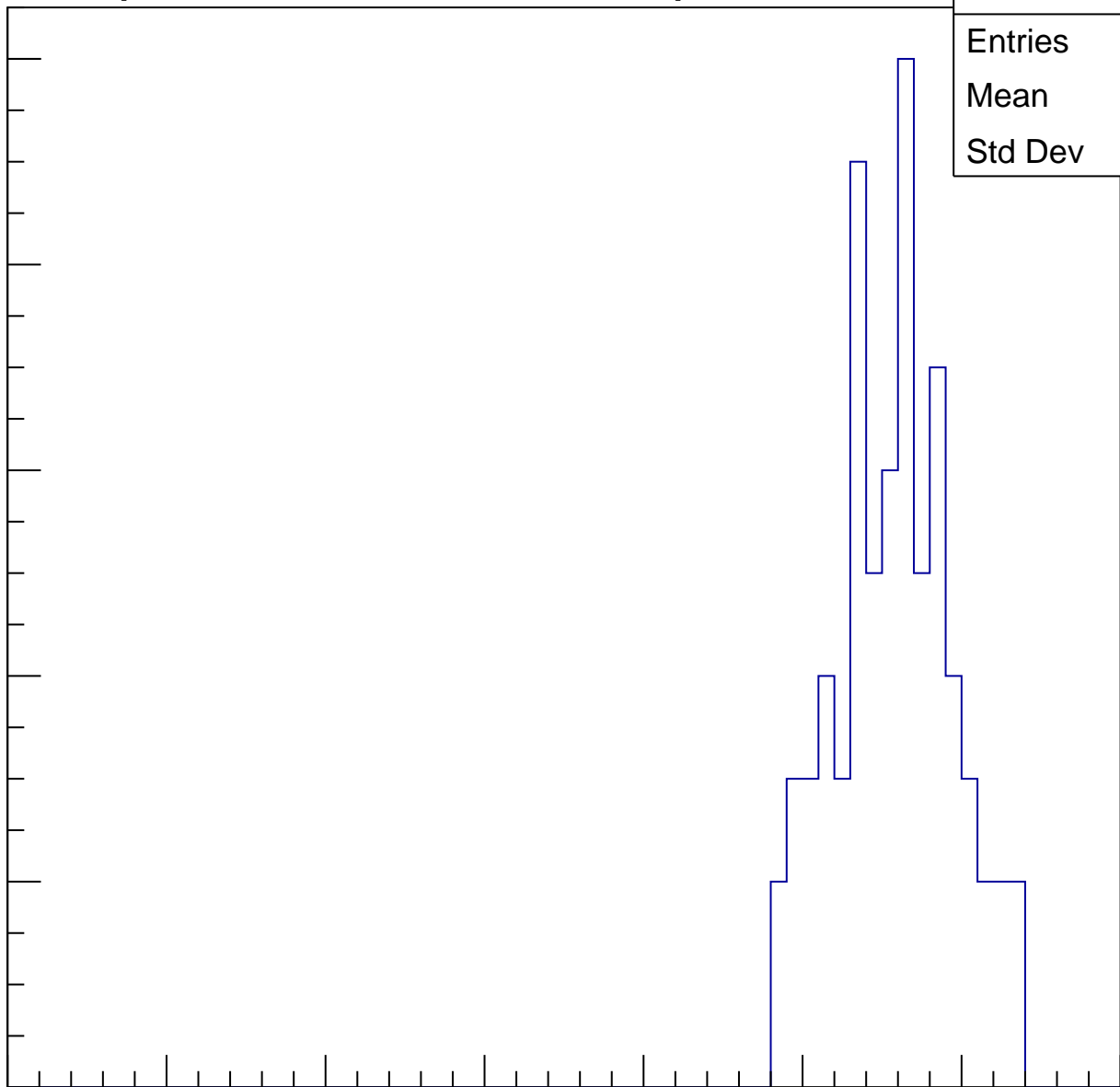
40

50

60

ampl

70

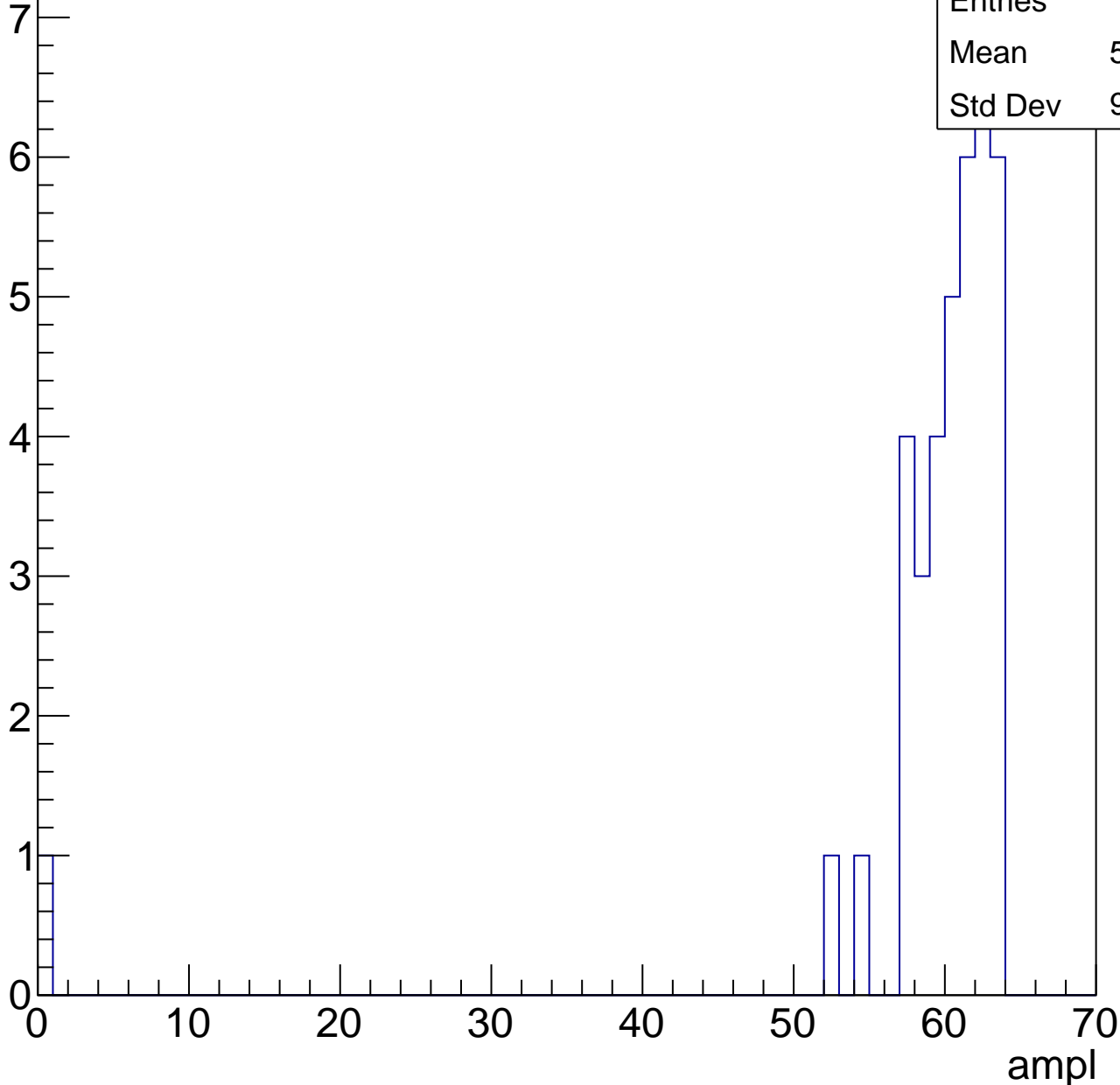


# B0L001S, U21-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	38
Mean	58.47
Std Dev	9.936



# B0L001S, U21-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

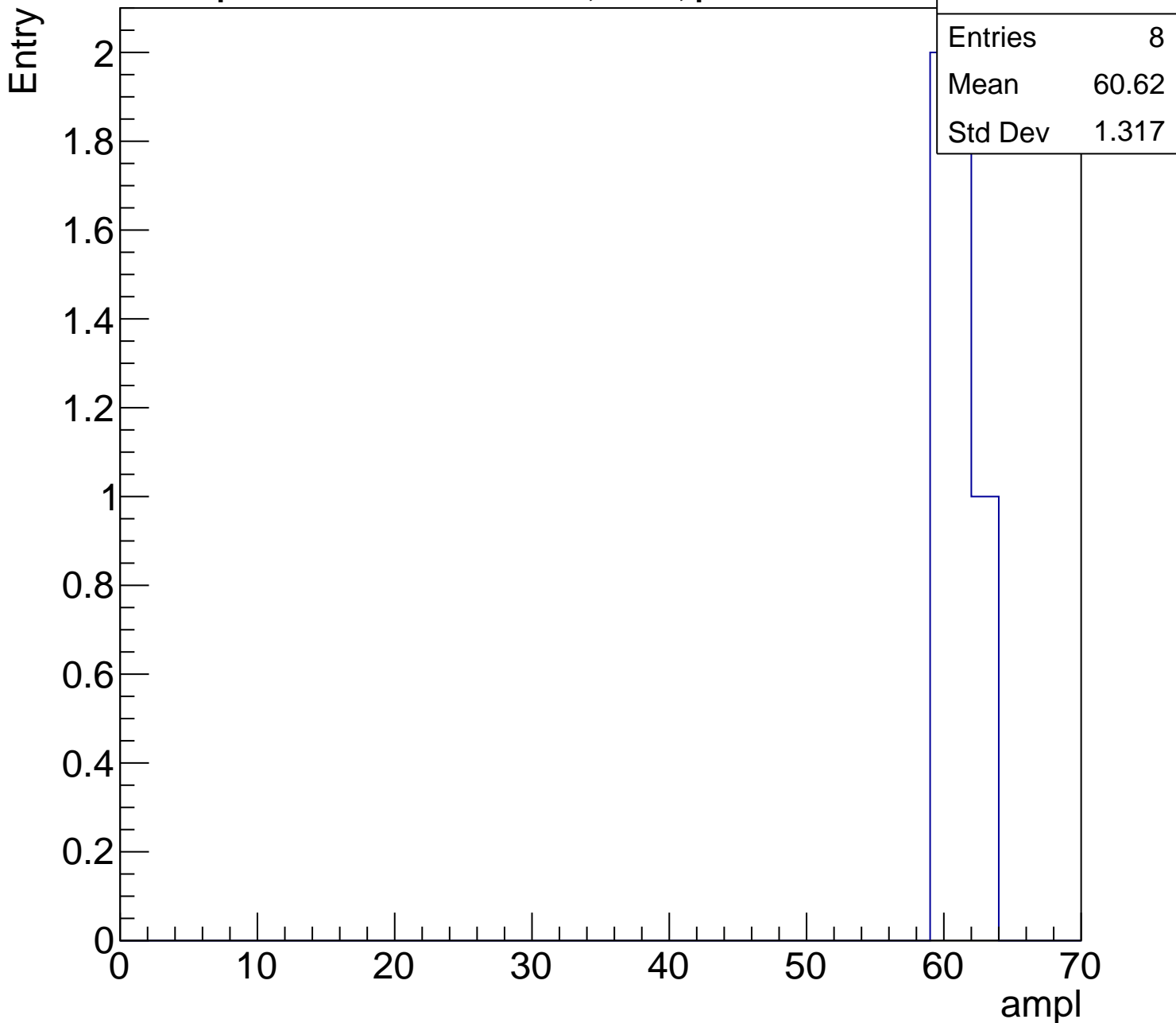
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	8
Mean	60.62
Std Dev	1.317

0 10 20 30 40 50 60 70

ampl





# B0L001S, U21-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch11, adc0

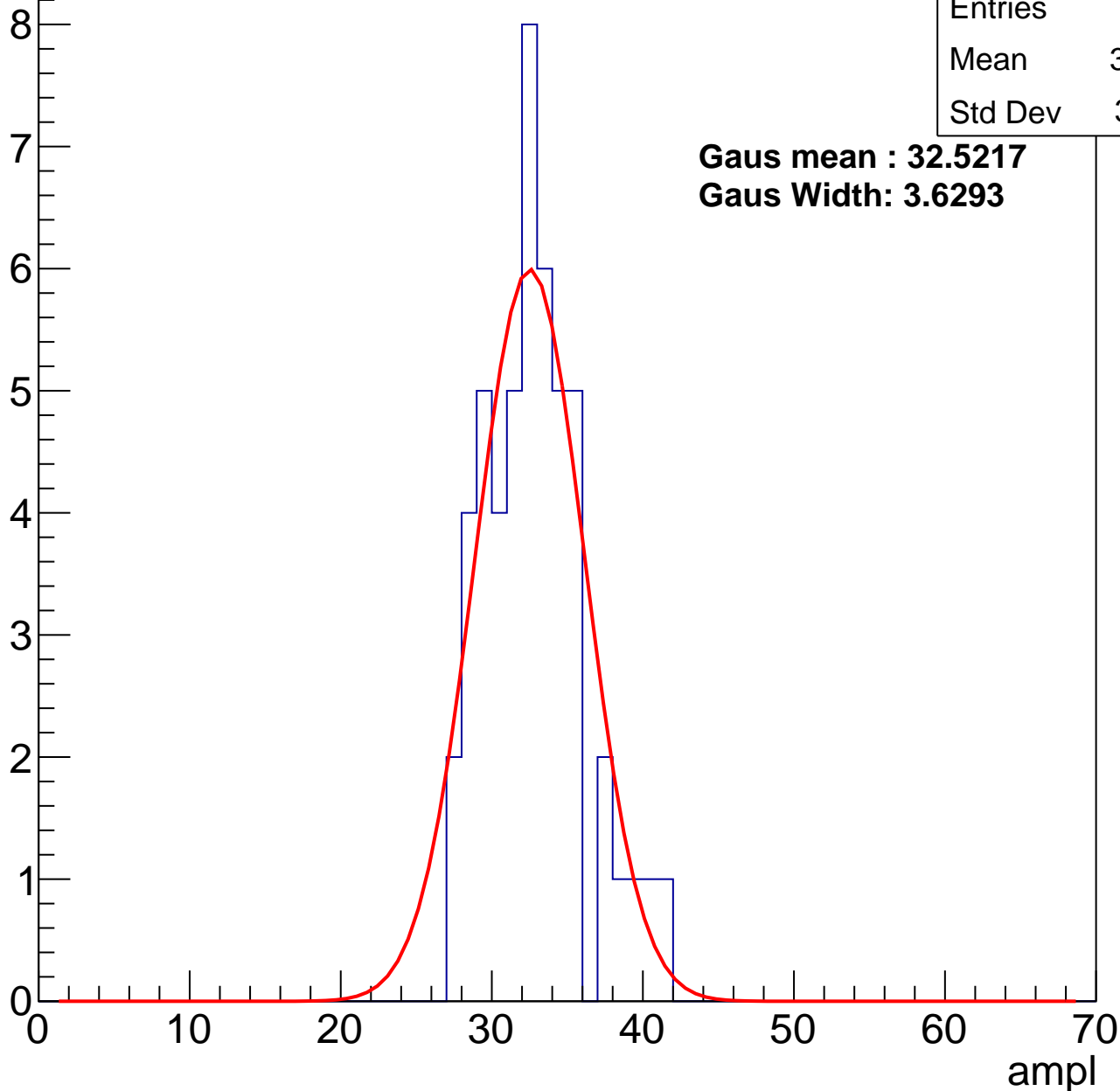
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	32.34
Std Dev	3.241

**Gaus mean : 32.5217**

**Gaus Width: 3.6293**



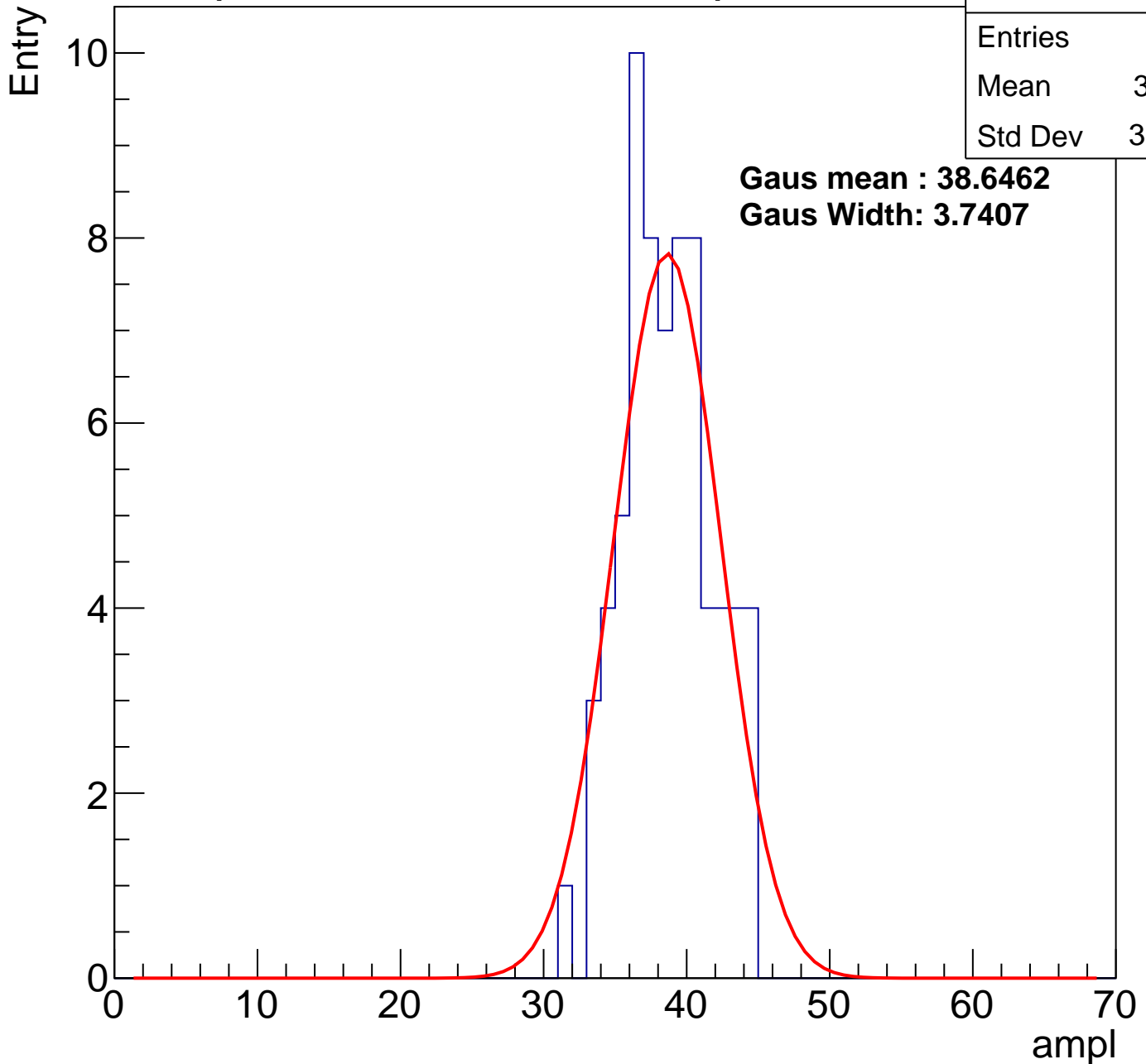
# B0L001S, U21-ch11, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	70
Mean	38.21
Std Dev	3.075

**Gaus mean : 38.6462**

**Gaus Width: 3.7407**



# B0L001S, U21-ch11, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	45.51
Std Dev	3.273

**Gaus mean : 46.3639**

**Gaus Width: 3.4492**

10

8

6

4

2

0

ampl

0

10

20

30

40

50

60

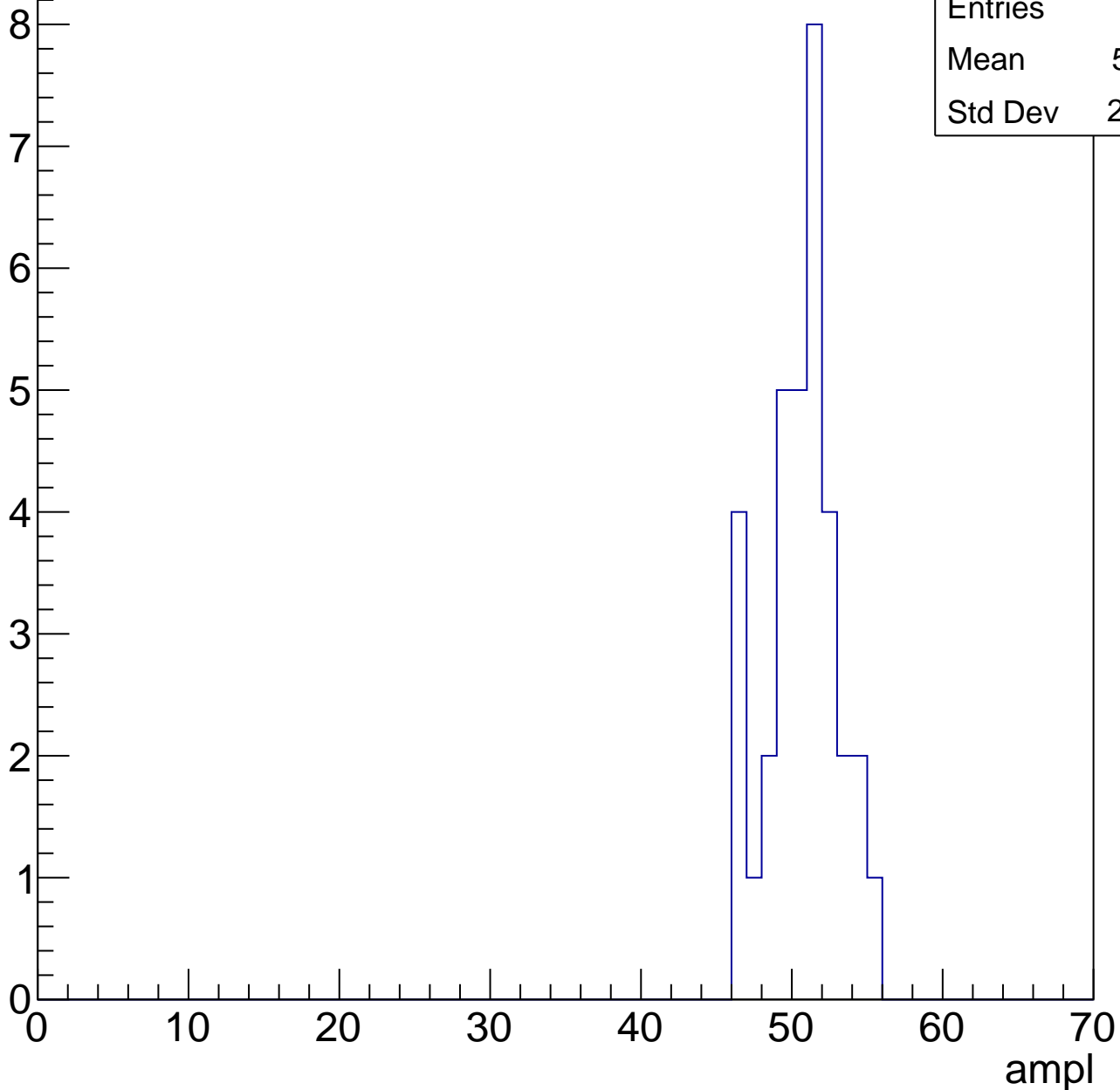
70

# B0L001S, U21-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	34
Mean	50.21
Std Dev	2.324



# B0L001S, U21-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

10

8

6

4

2

0

0

10

20

30

40

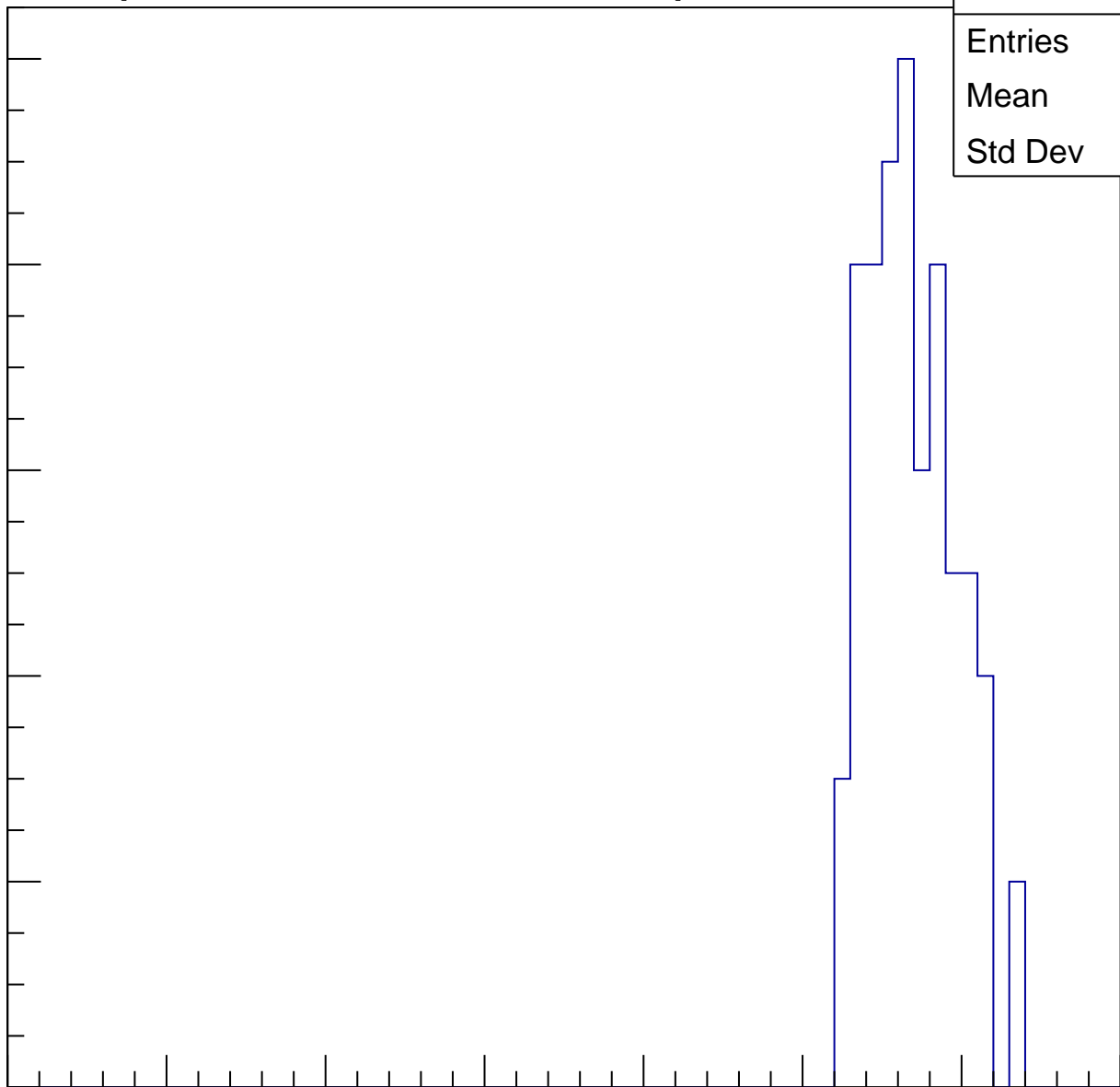
50

60

70

ampl

Entries	68
Mean	56.44
Std Dev	2.735

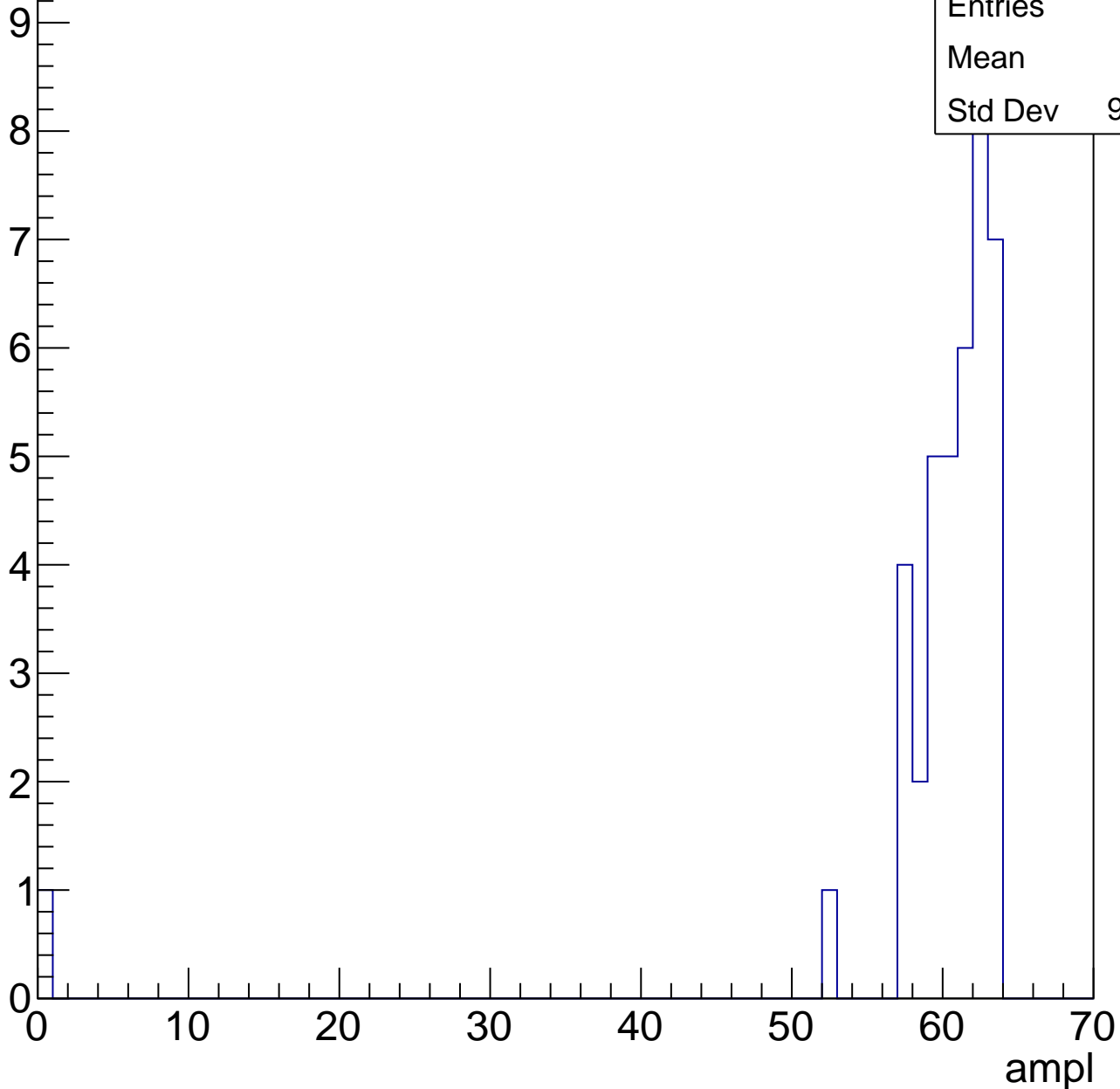


# B0L001S, U21-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	40
Mean	58.9
Std Dev	9.708



# B0L001S, U21-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch12, adc0

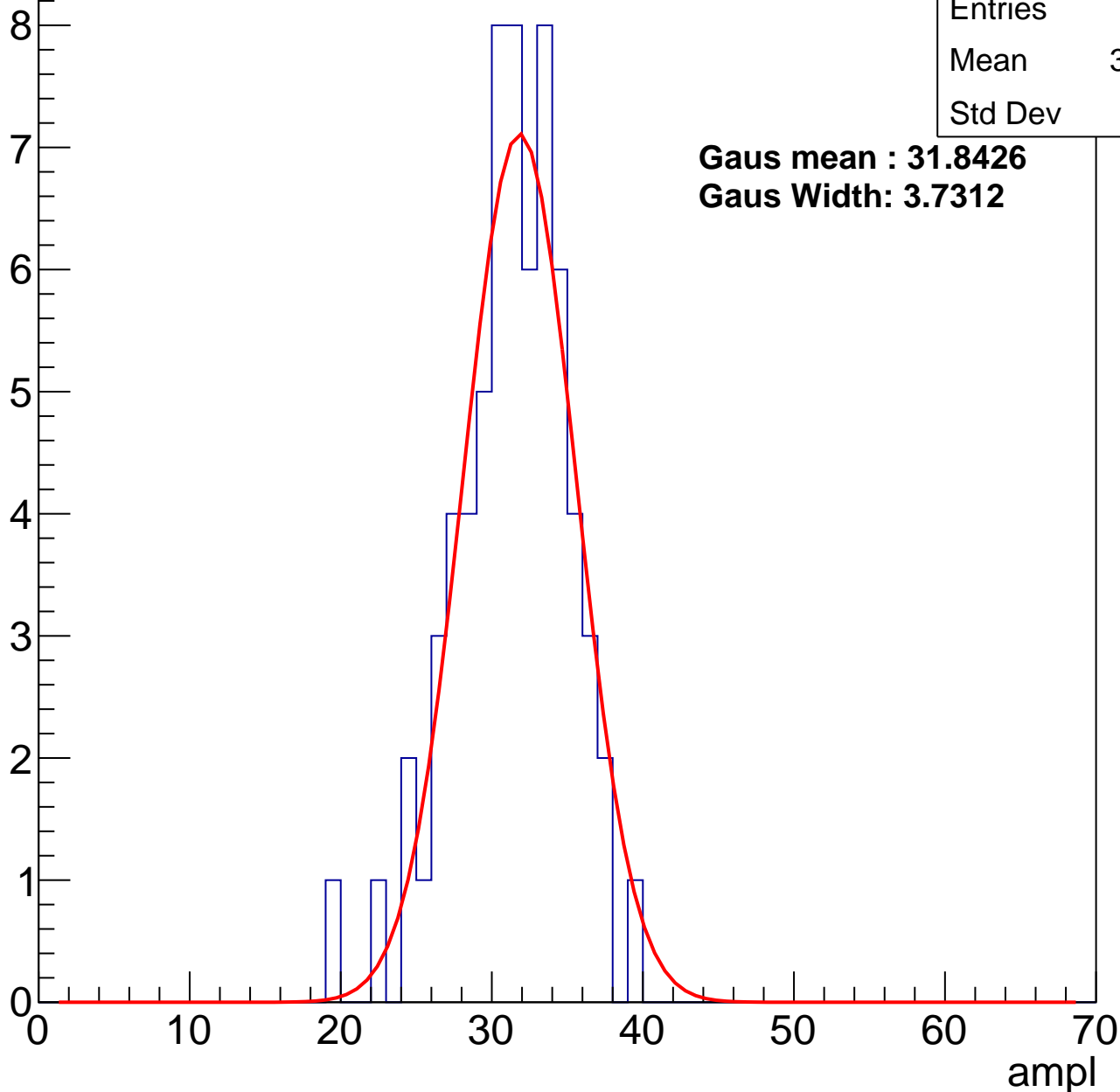
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	30.84
Std Dev	3.72

**Gaus mean : 31.8426**

**Gaus Width: 3.7312**



# B0L001S, U21-ch12, adc1

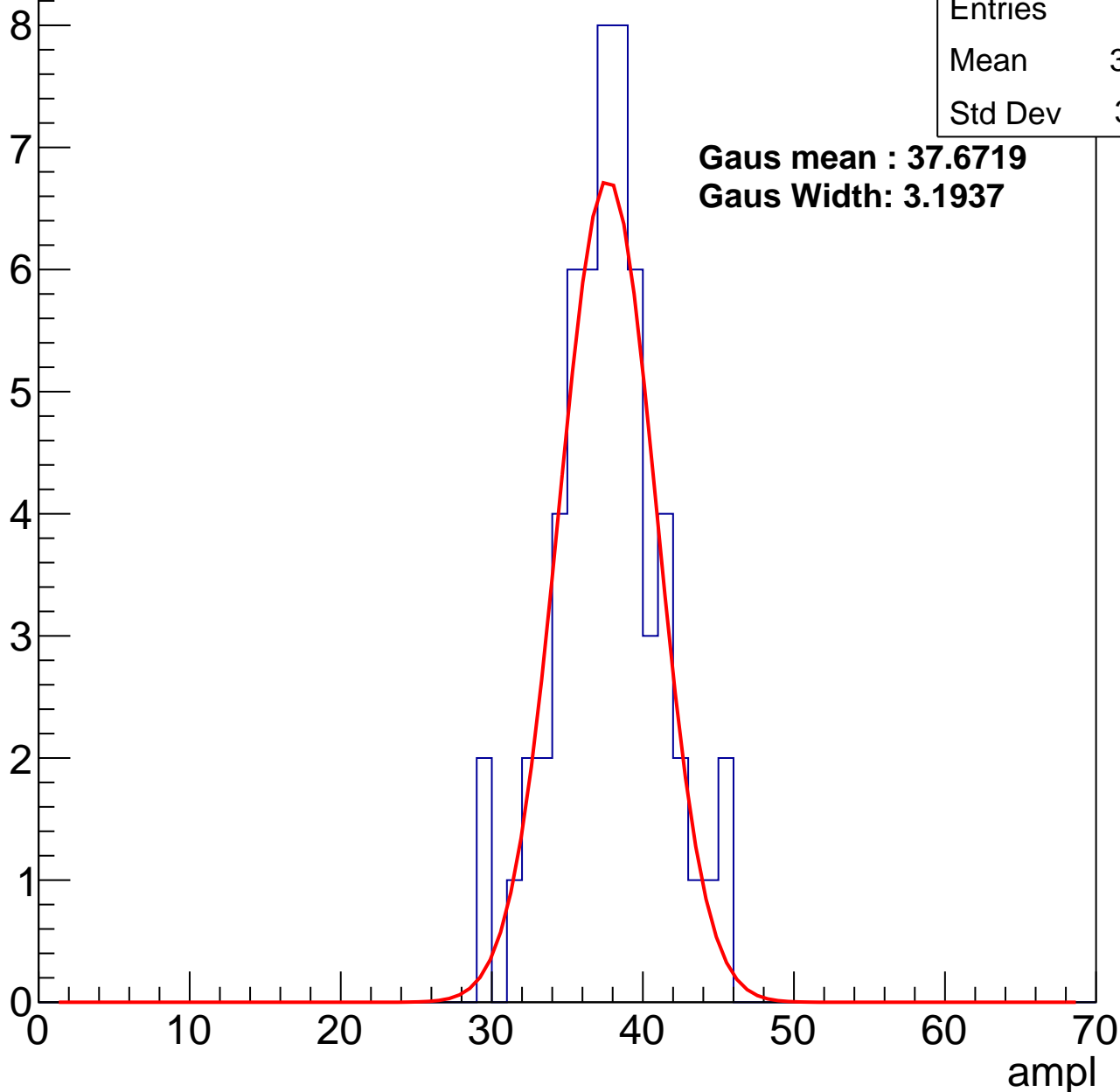
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	37.24
Std Dev	3.461

**Gaus mean : 37.6719**

**Gaus Width: 3.1937**



# B0L001S, U21-ch12, adc2

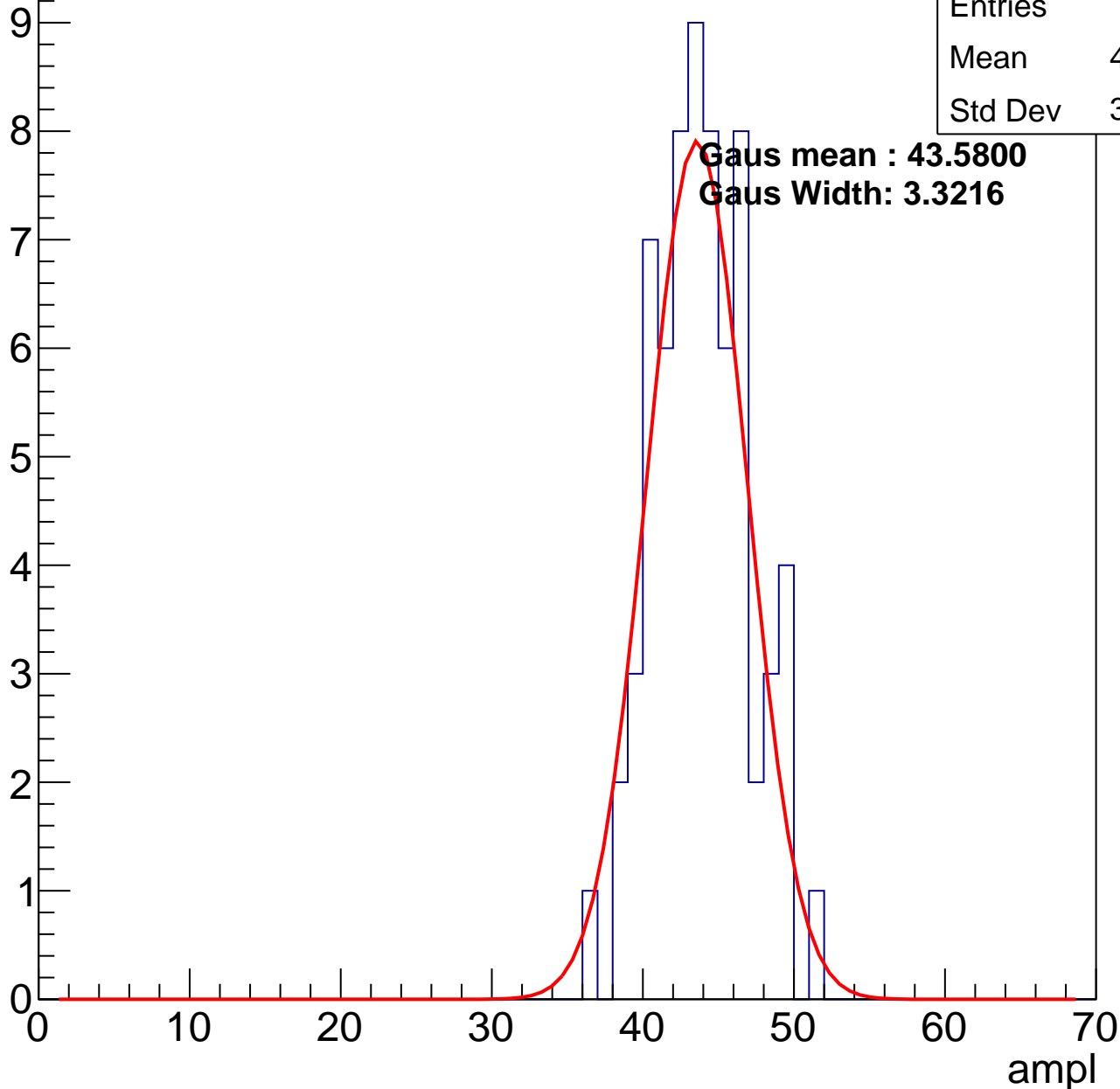
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	43.43
Std Dev	3.088

**Gaus mean : 43.5800**

**Gaus Width: 3.3216**



# B0L001S, U21-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

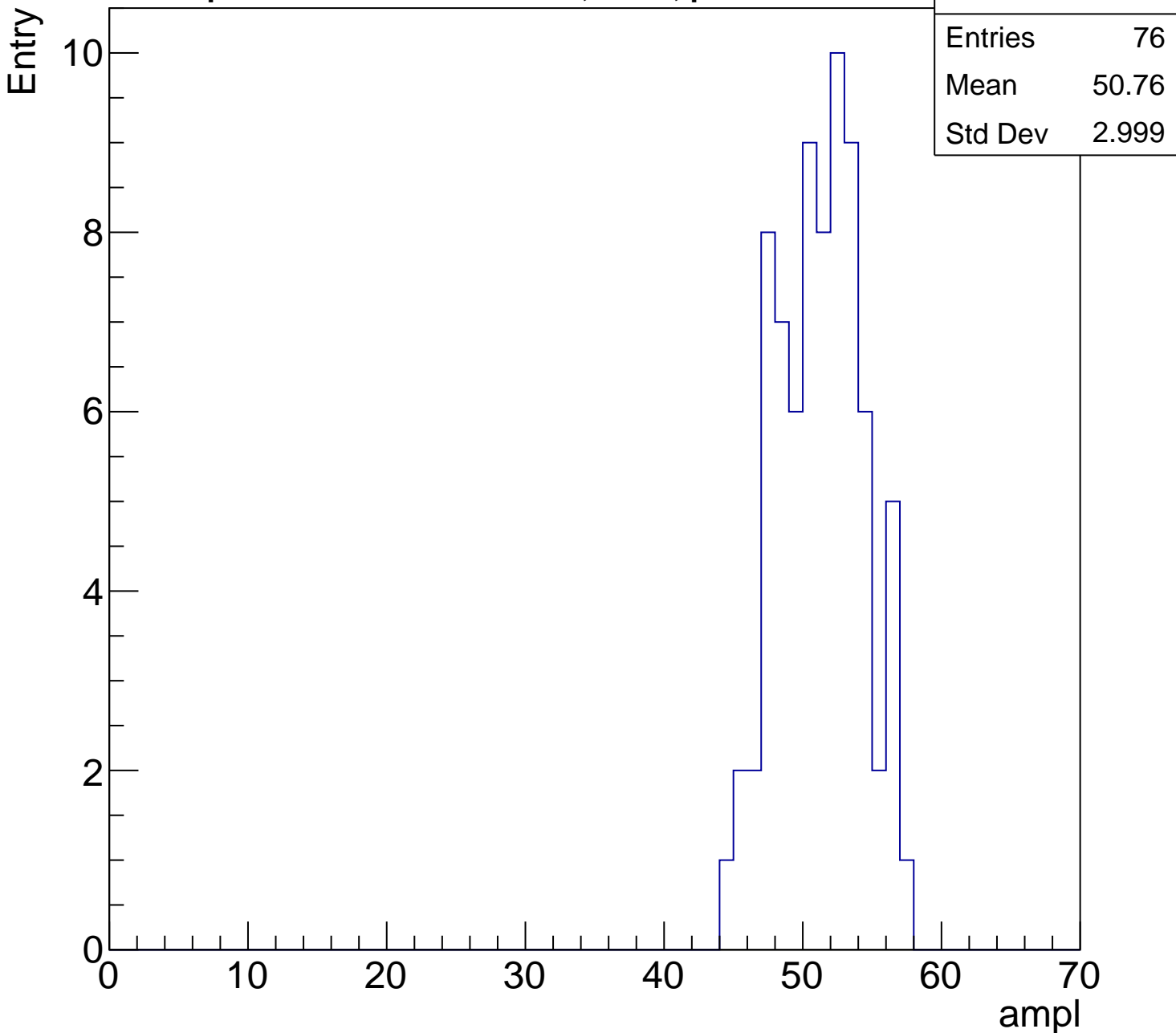
Entries	76
Mean	50.76
Std Dev	2.999

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

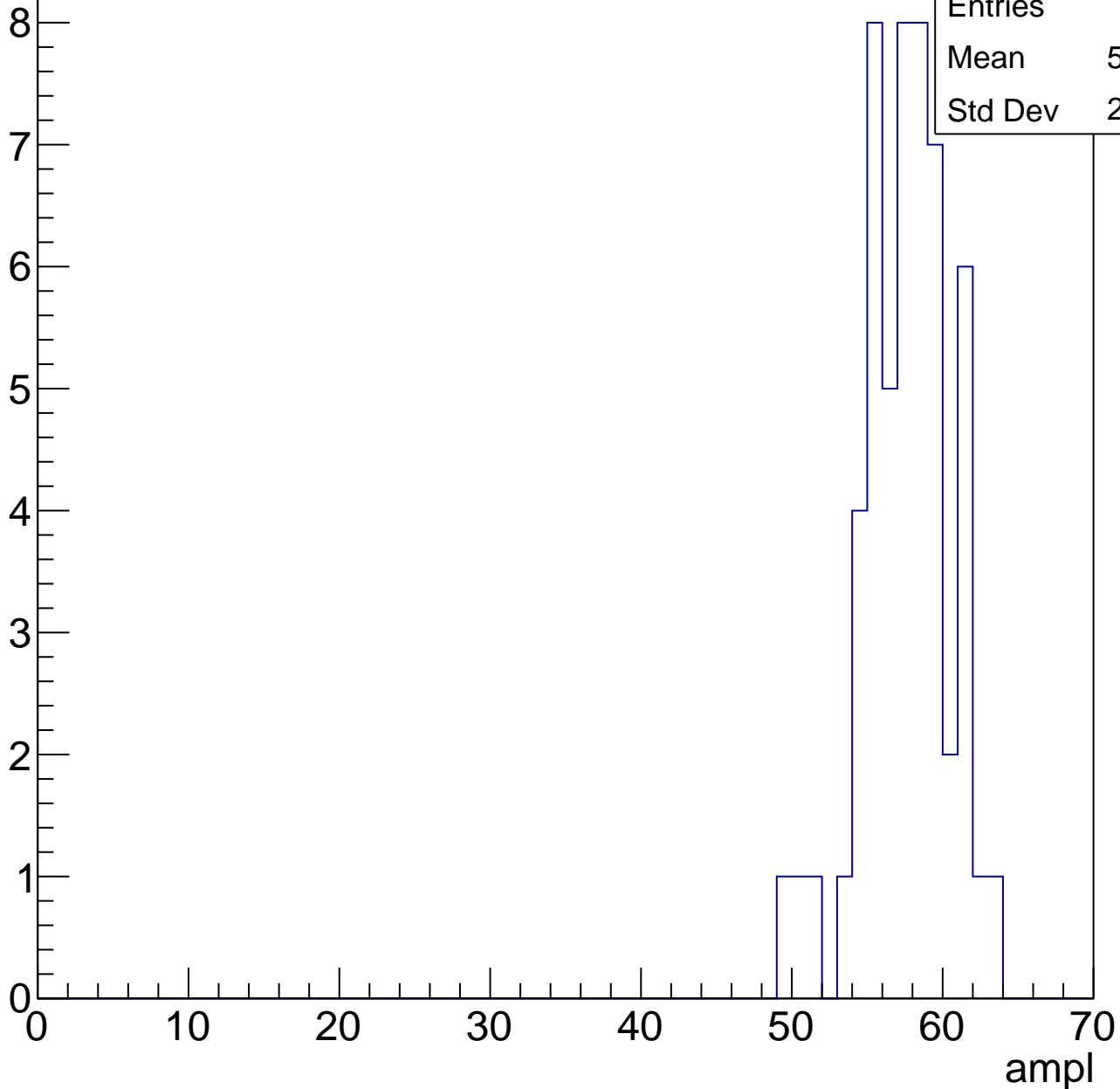


# B0L001S, U21-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	57.09
Std Dev	2.882

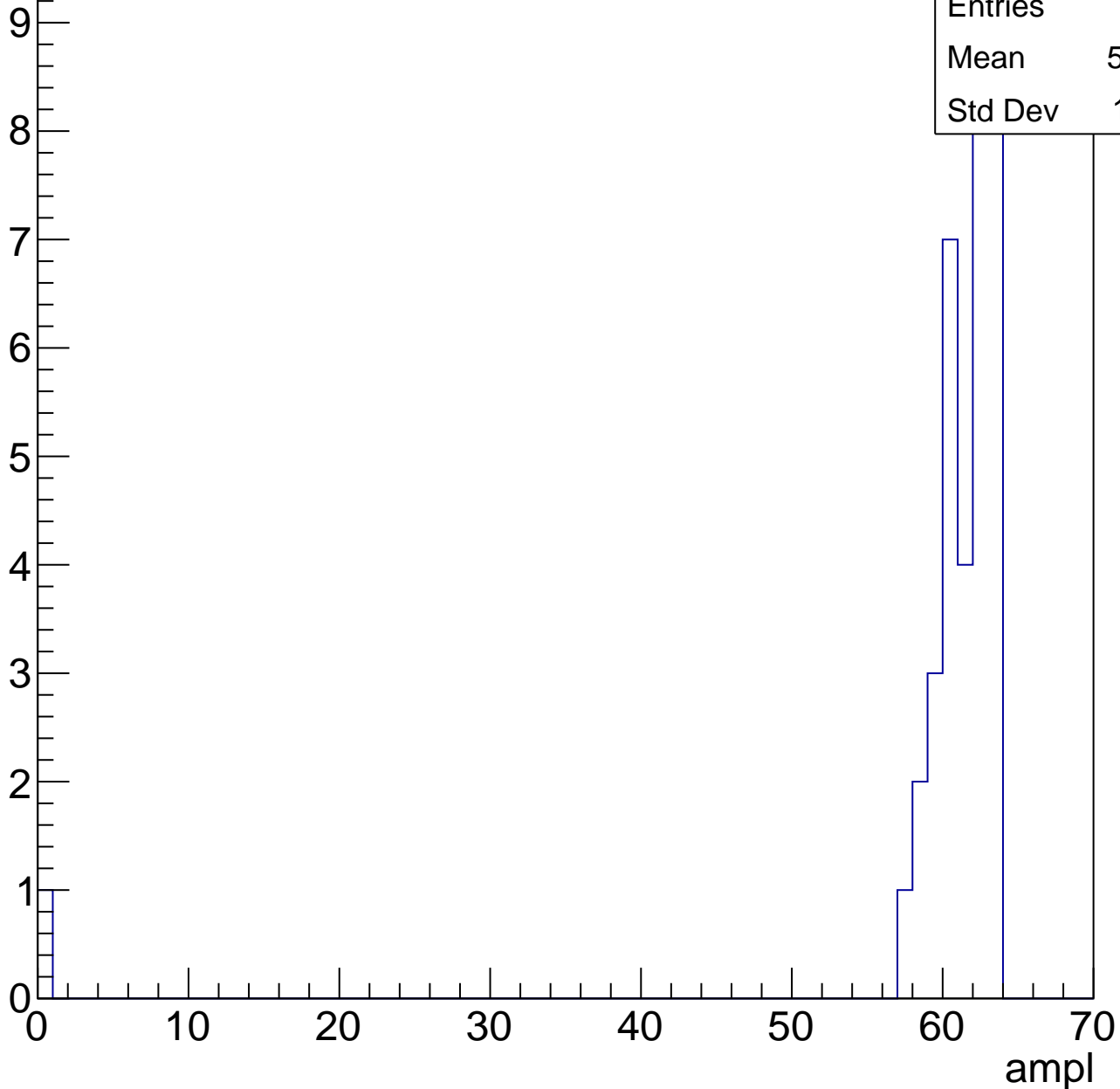


# B0L001S, U21-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	35
Mean	59.34
Std Dev	10.31



# B0L001S, U21-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U21-ch13, adc0

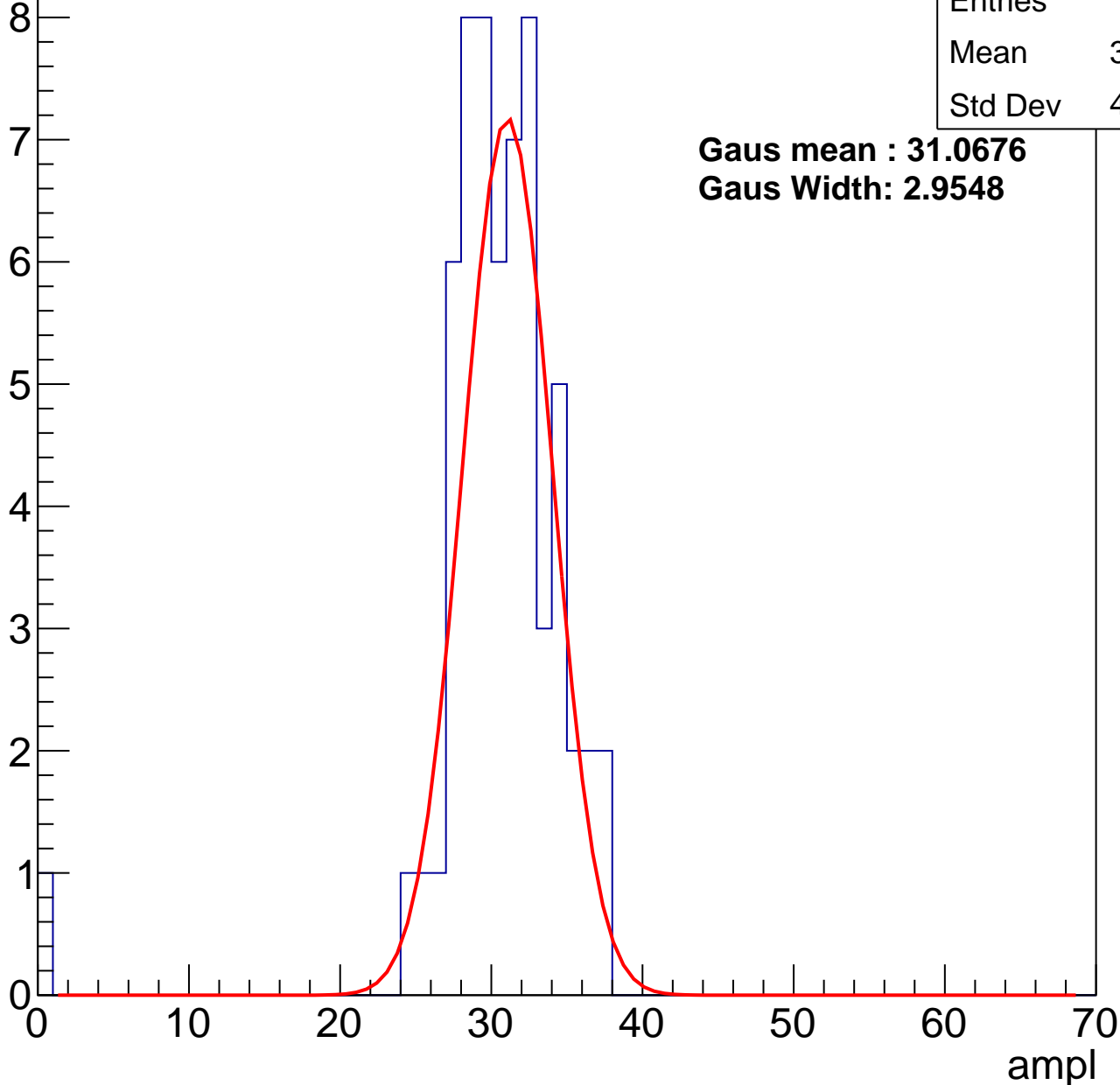
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	30.02
Std Dev	4.854

**Gaus mean : 31.0676**

**Gaus Width: 2.9548**



# B0L001S, U21-ch13, adc1

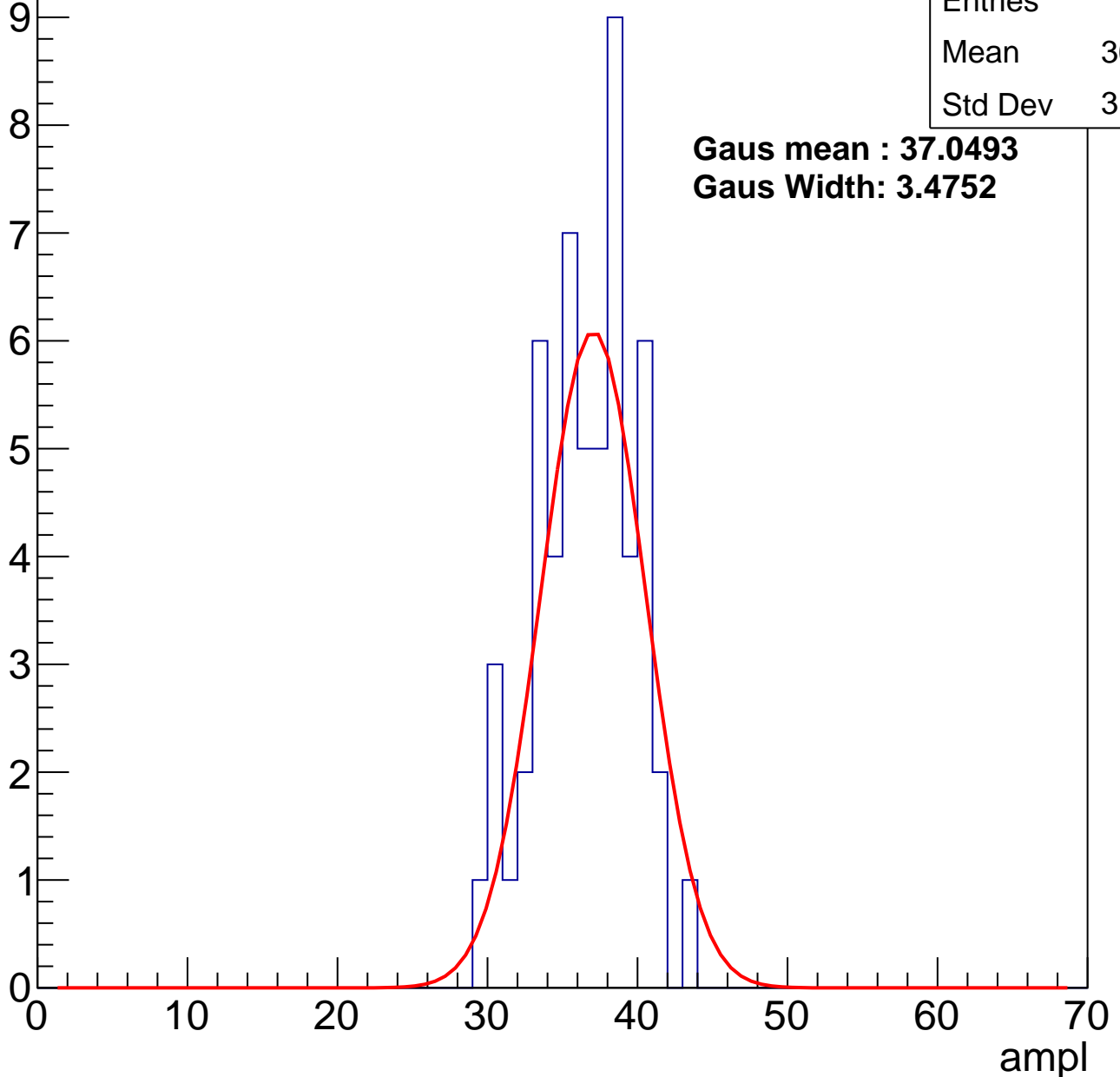
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	36.09
Std Dev	3.169

**Gaus mean : 37.0493**

**Gaus Width: 3.4752**



# B0L001S, U21-ch13, adc2

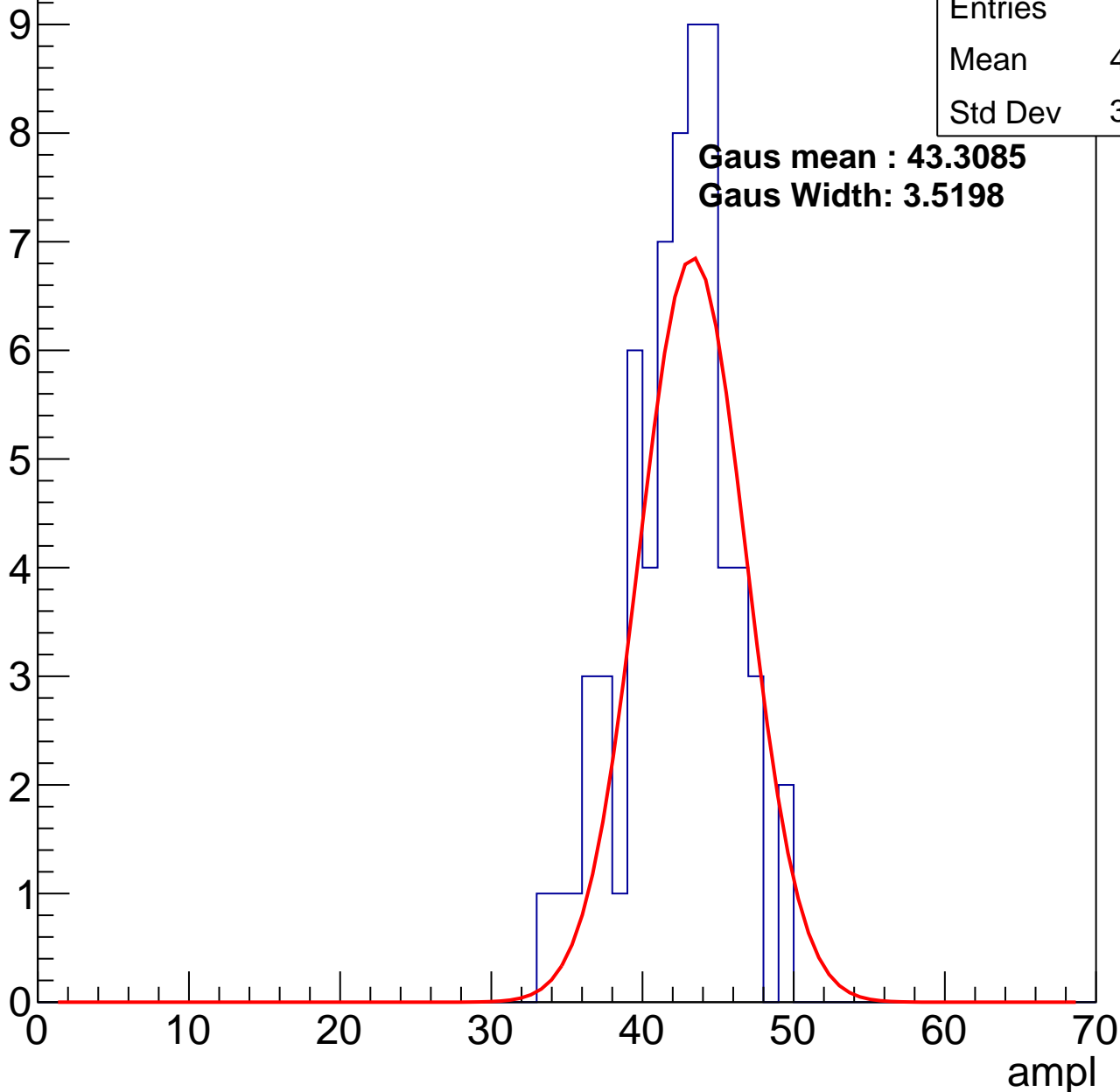
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	41.85
Std Dev	3.452

**Gaus mean : 43.3085**

**Gaus Width: 3.5198**



# B0L001S, U21-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

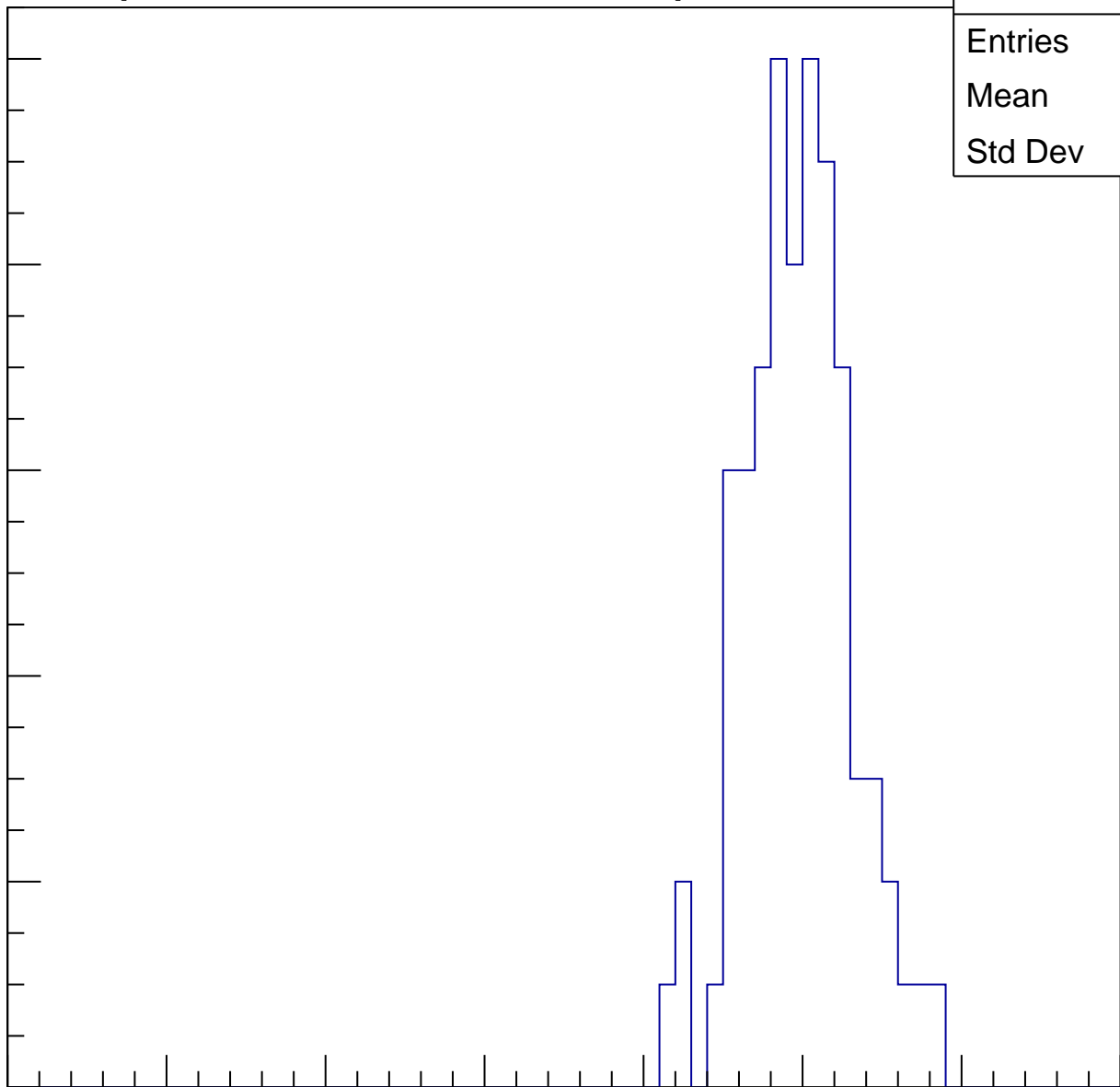
Entries	78
Mean	49.24
Std Dev	3.337

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

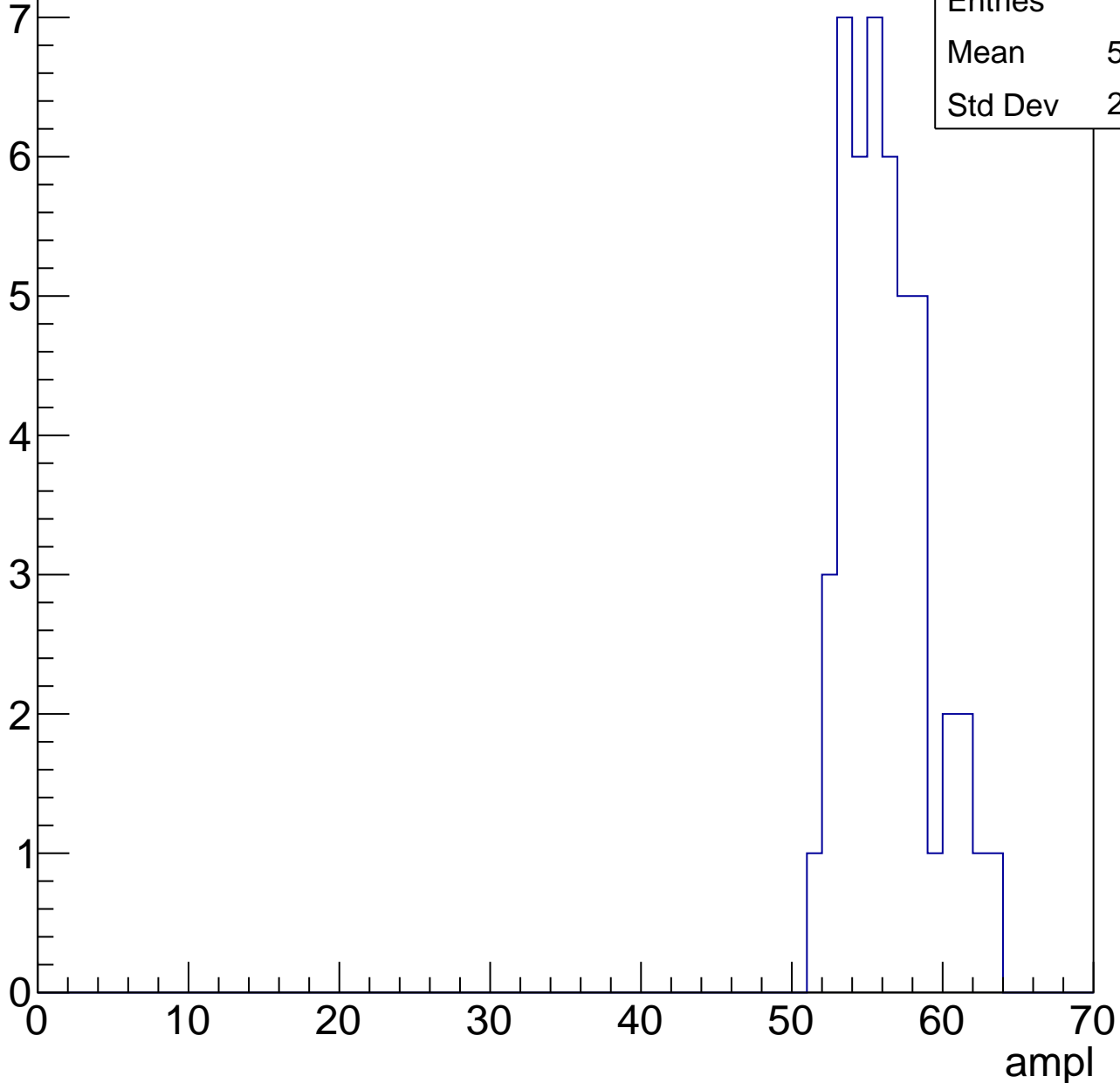


# B0L001S, U21-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

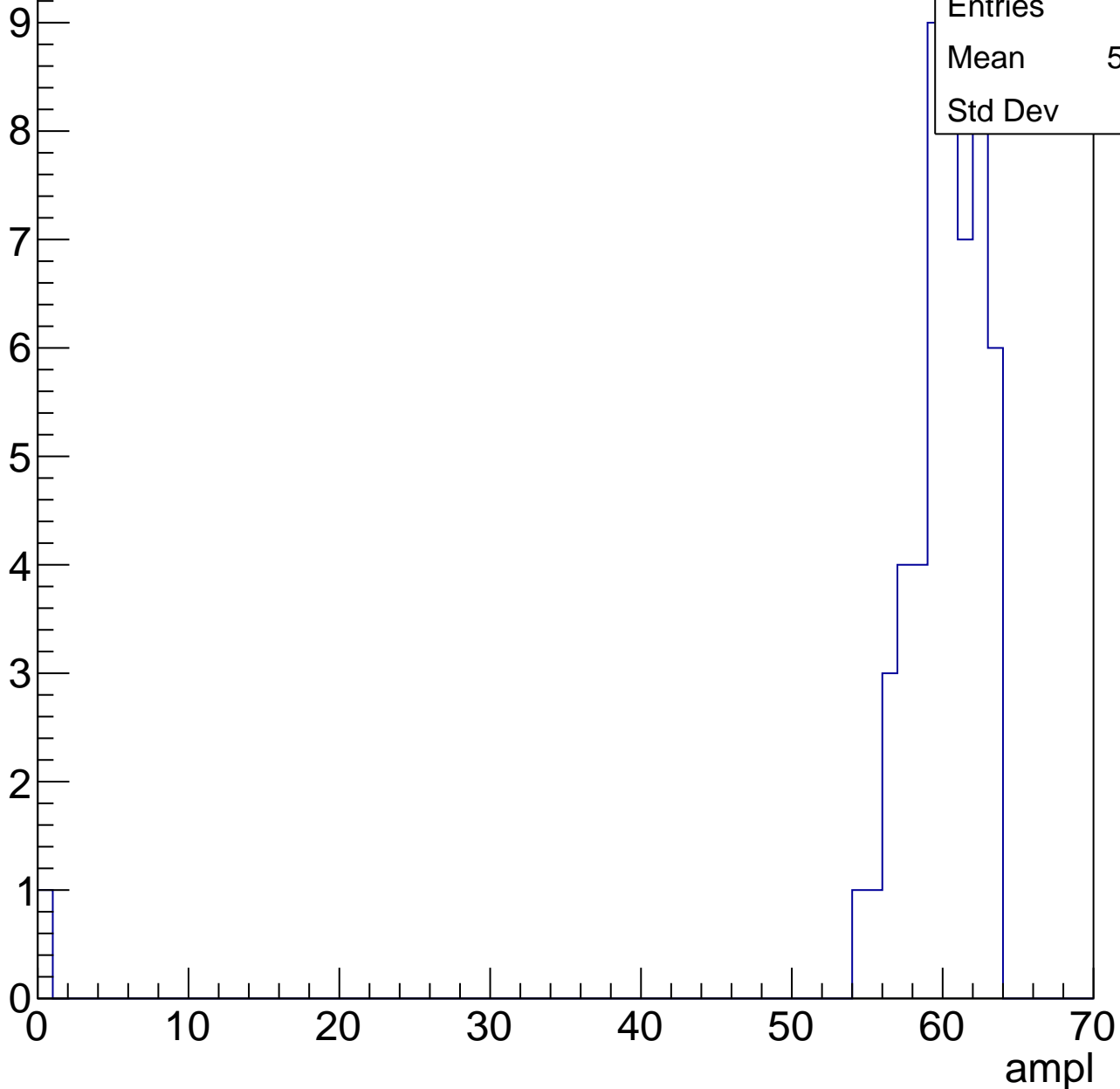
Entries	47
Mean	55.83
Std Dev	2.793



# B0L001S, U21-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U21-ch14, adc0

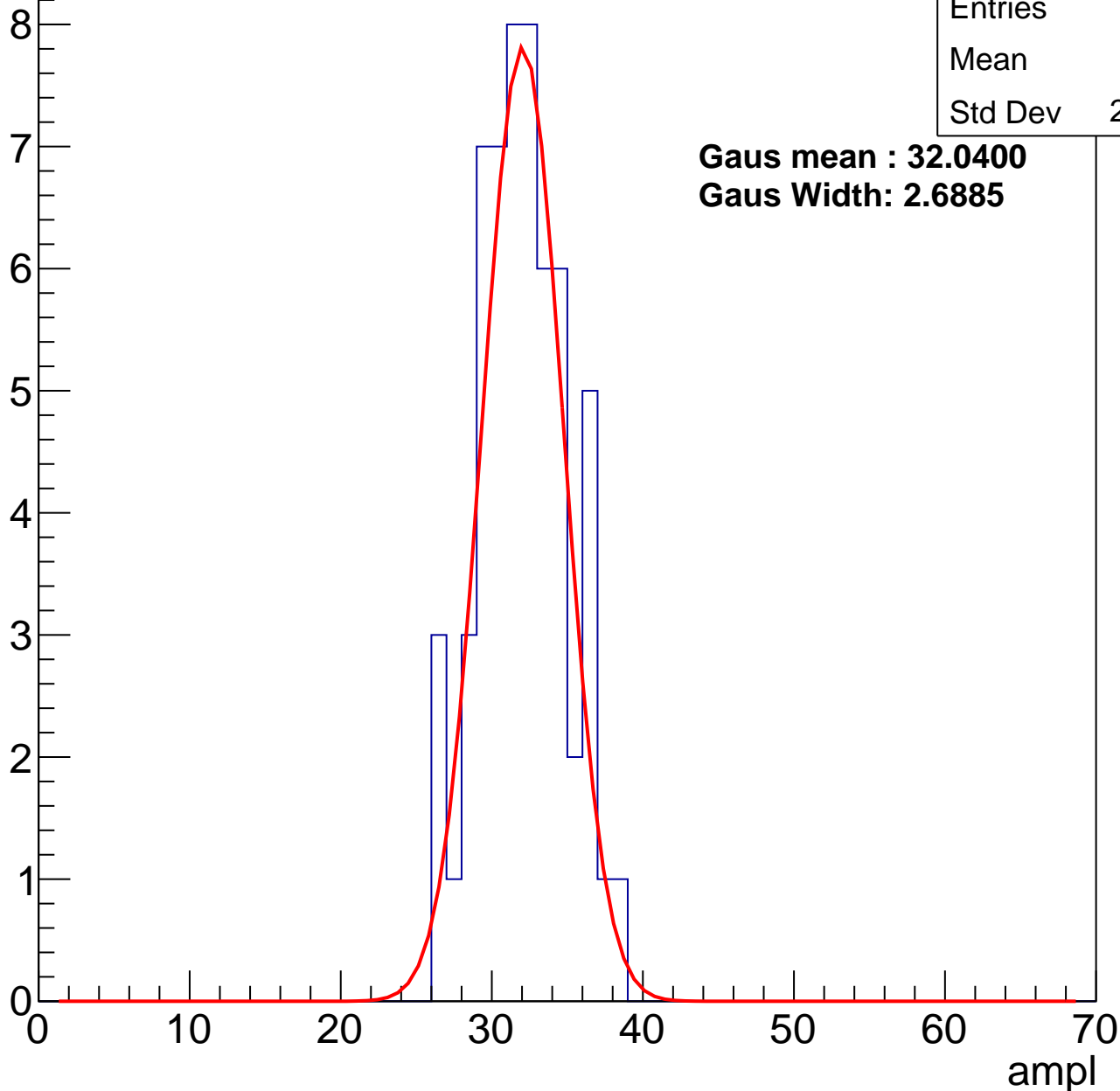
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	31.6
Std Dev	2.816

**Gaus mean : 32.0400**

**Gaus Width: 2.6885**



# B0L001S, U21-ch14, adc1

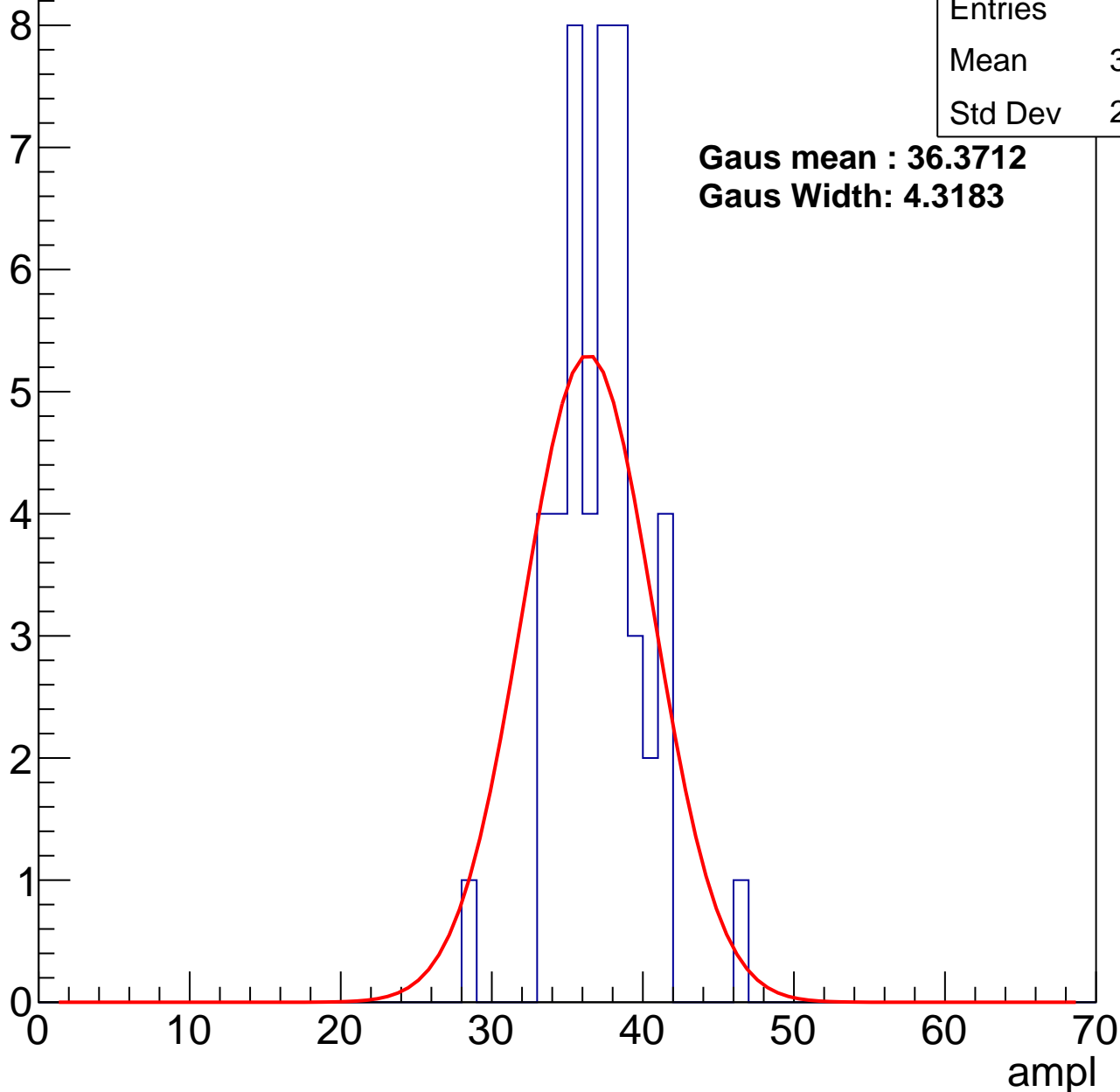
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	36.74
Std Dev	2.906

**Gaus mean : 36.3712**

**Gaus Width: 4.3183**



# B0L001S, U21-ch14, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	81
Mean	43.26
Std Dev	3.106

**Gaus mean : 43.9350**

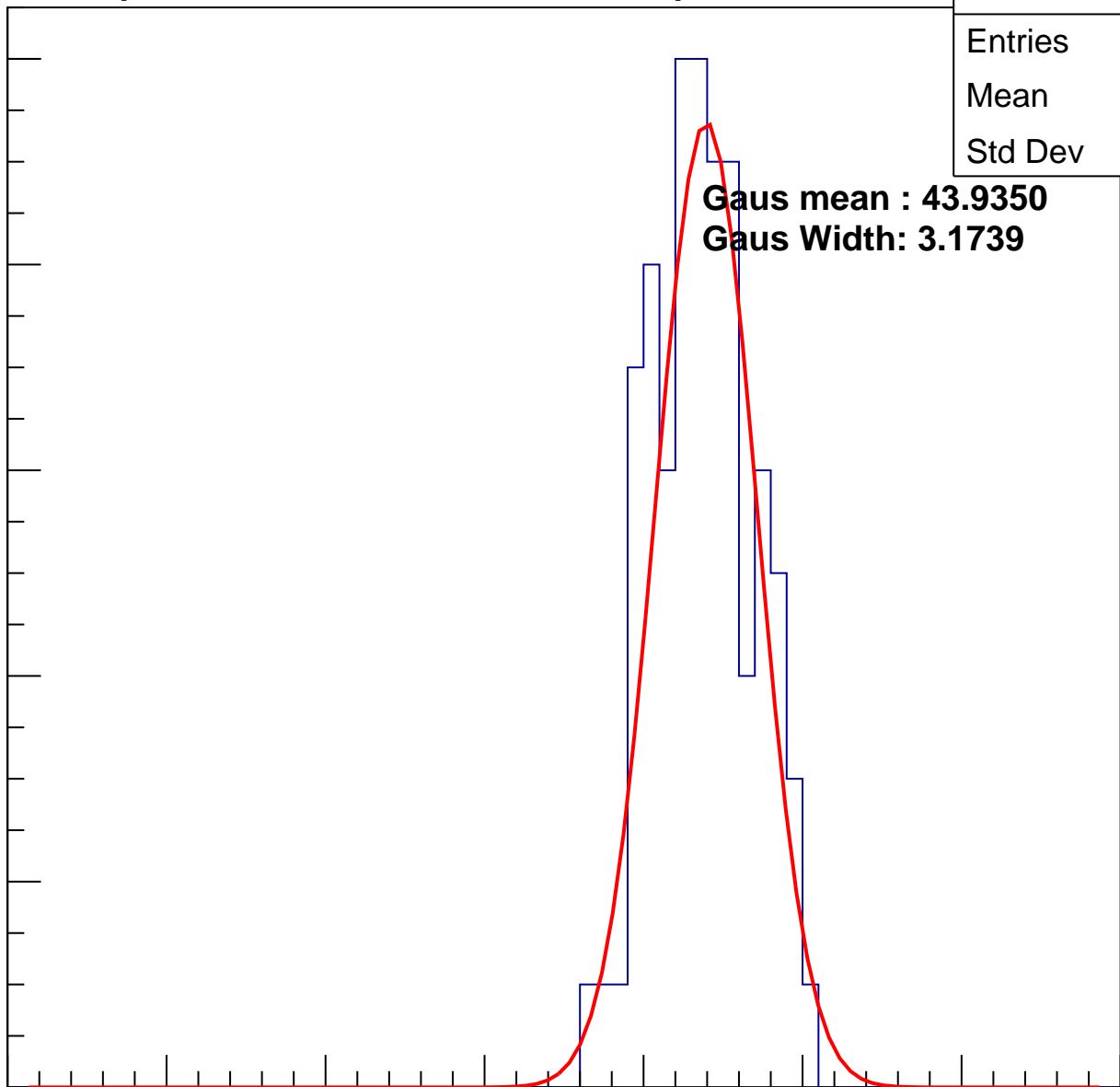
**Gaus Width: 3.1739**

Entry

10  
8  
6  
4  
2  
0

ampl

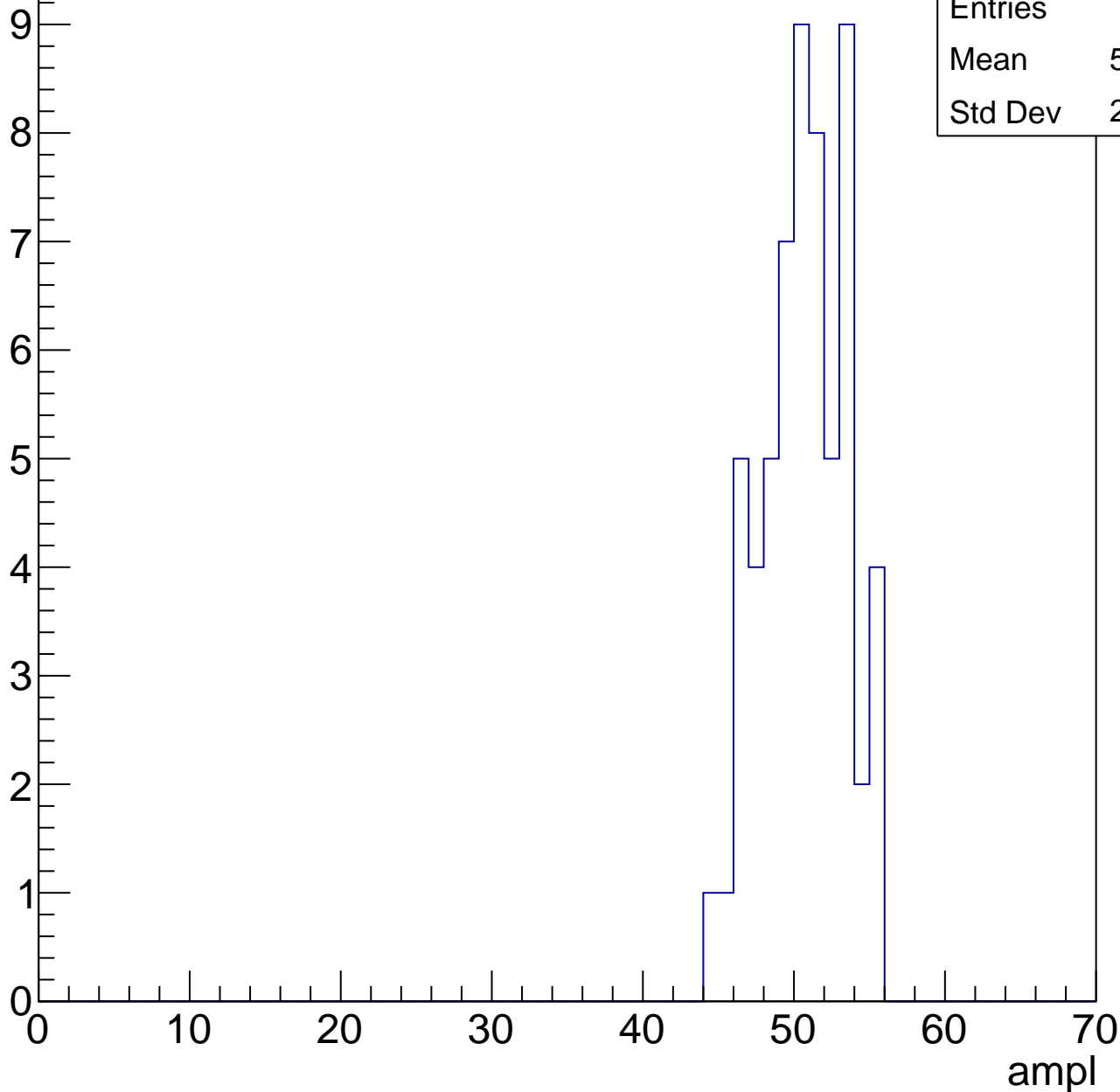
0 10 20 30 40 50 60 70



# B0L001S, U21-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



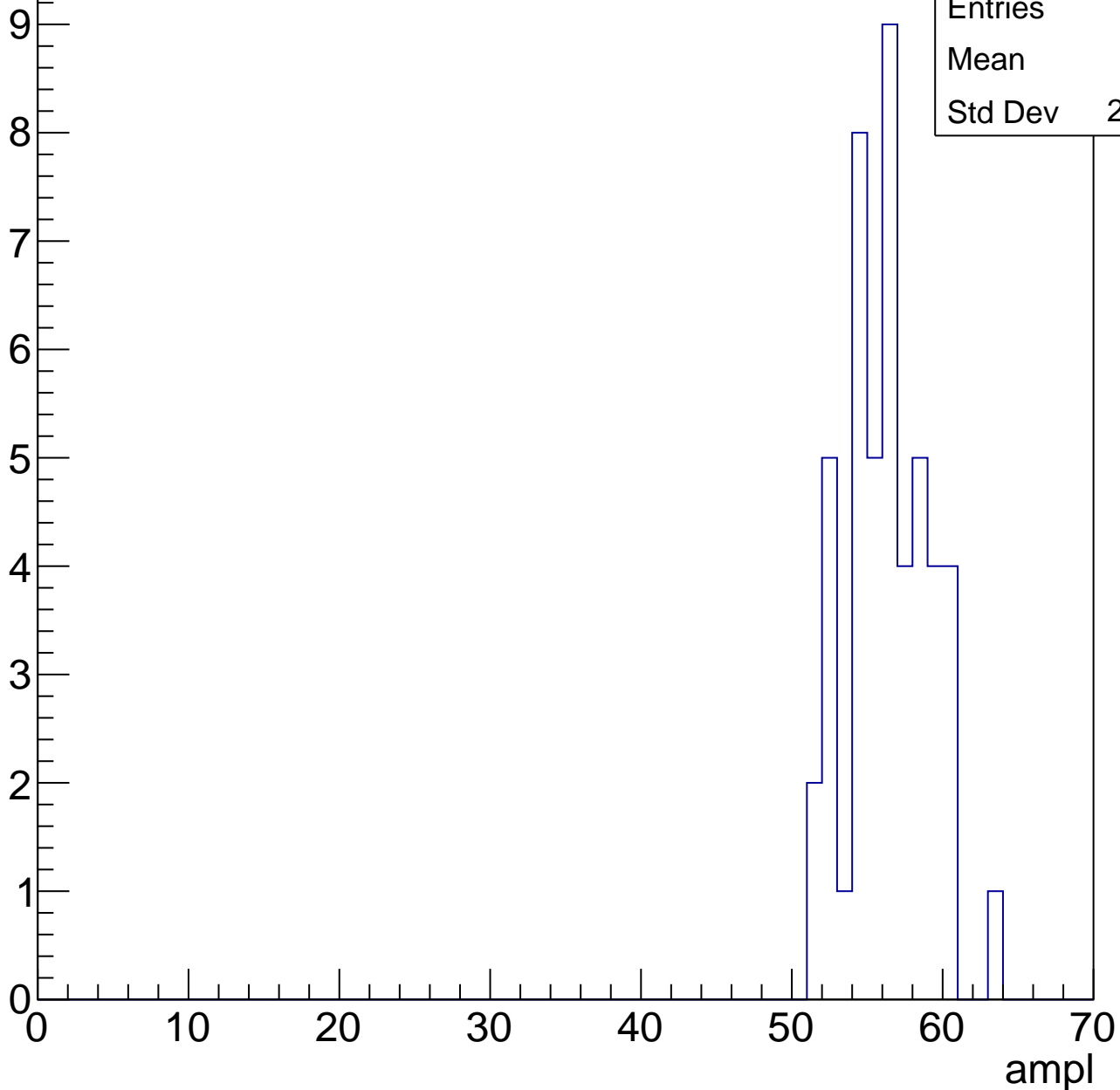
Entries	60
Mean	50.22
Std Dev	2.715

# B0L001S, U21-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	55.9
Std Dev	2.694

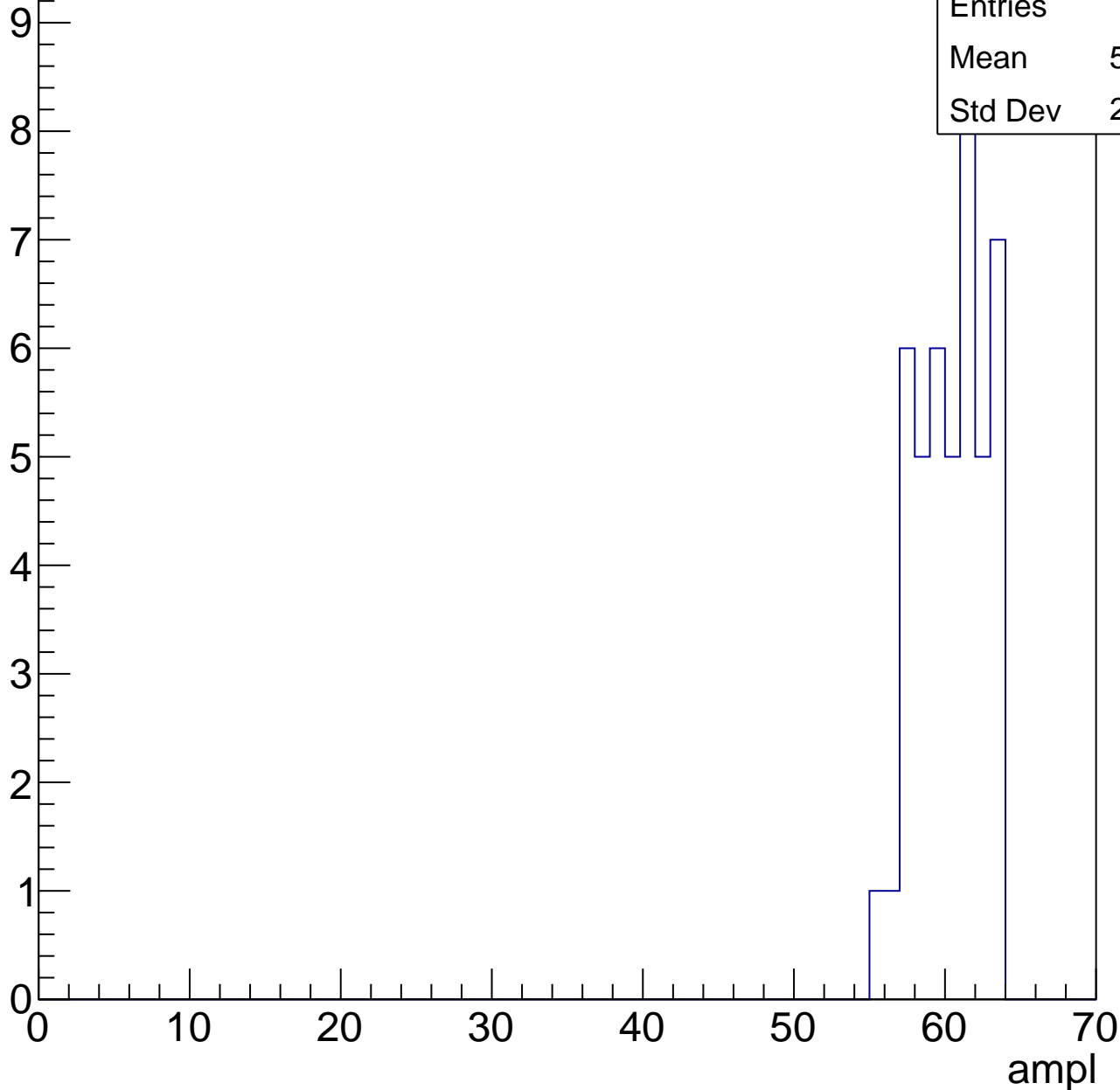


# B0L001S, U21-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	45
Mean	59.93
Std Dev	2.175

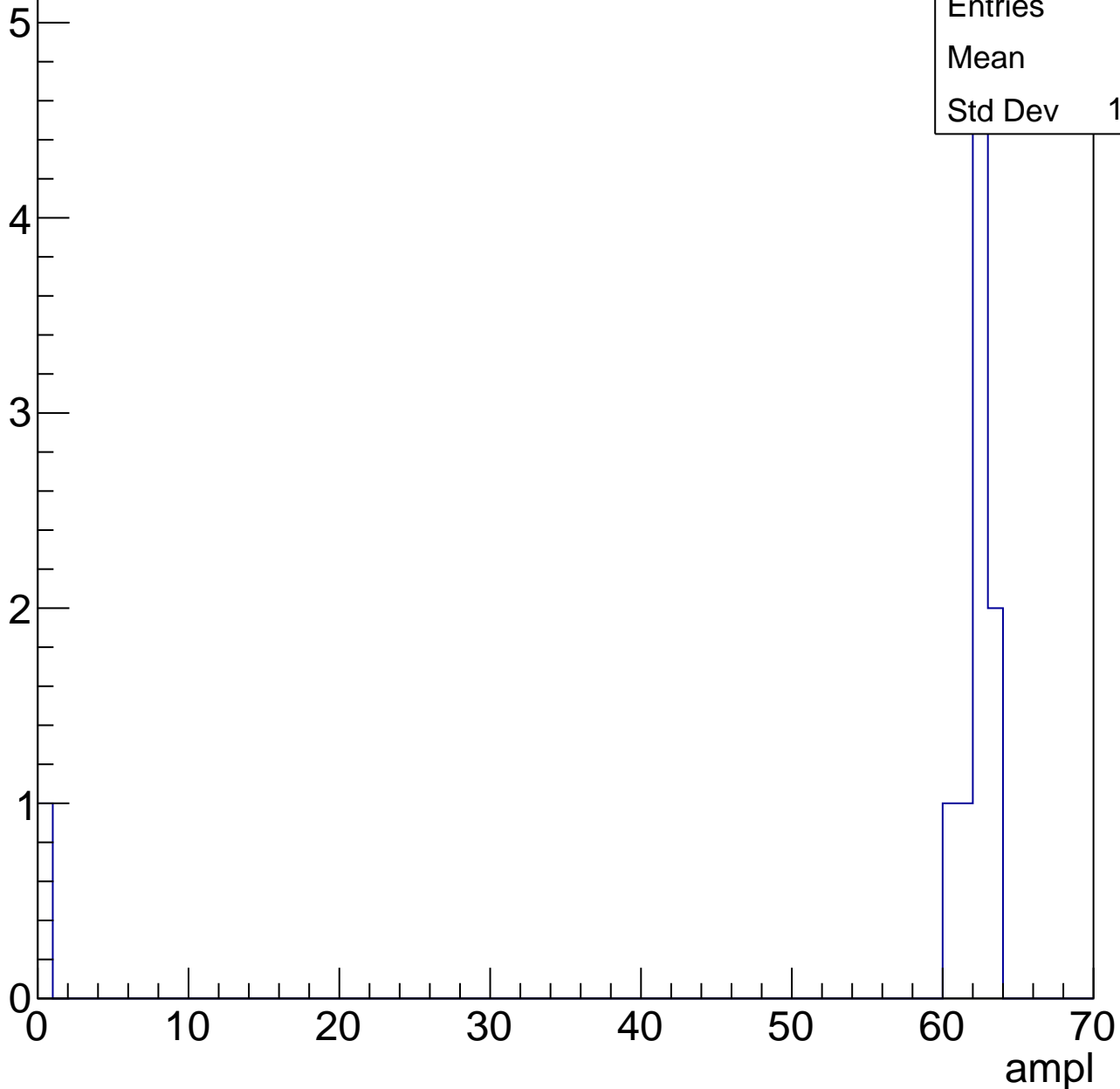


# B0L001S, U21-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	10
Mean	55.7
Std Dev	18.59





# B0L001S, U21-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch15, adc0

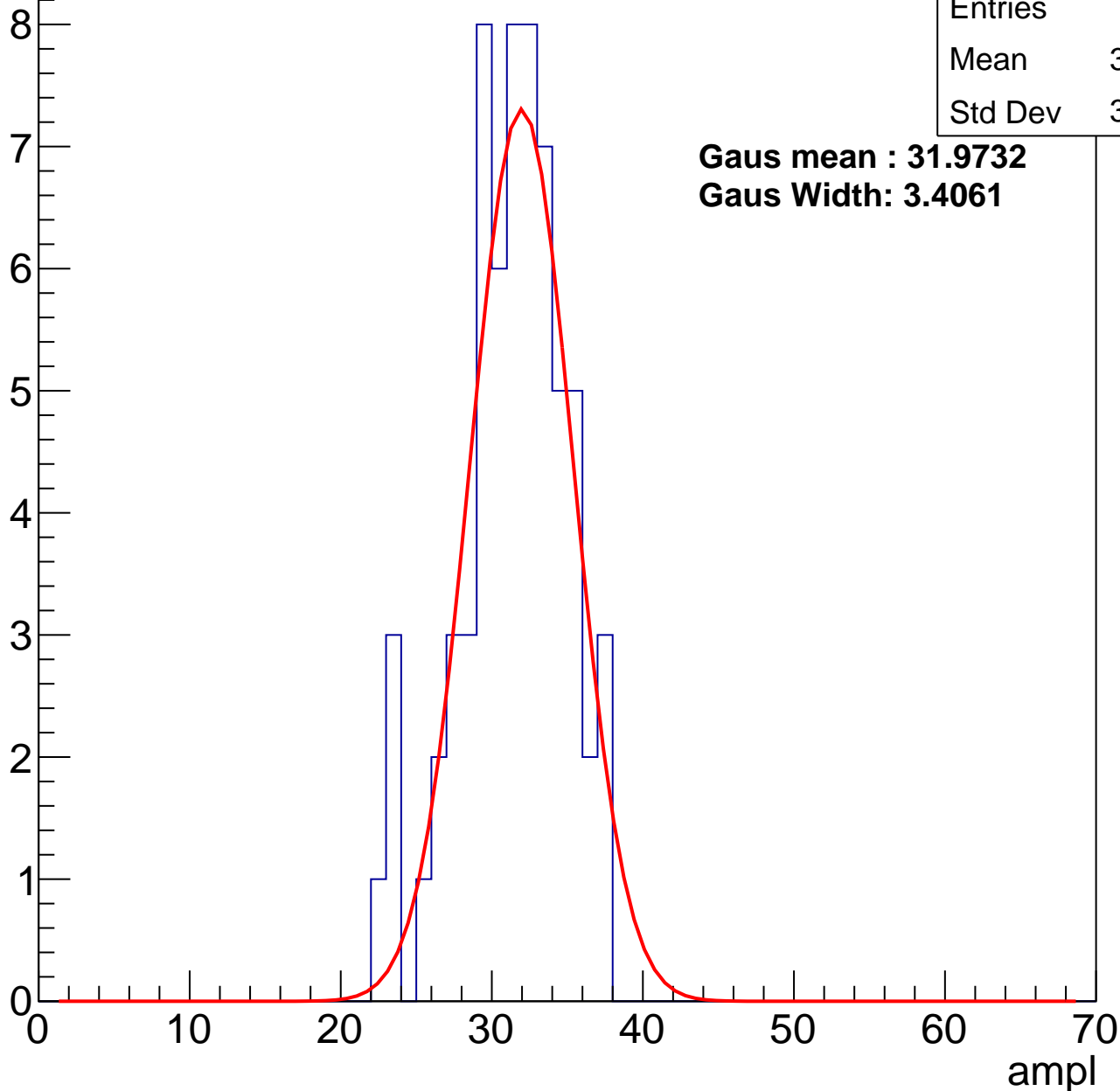
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	30.89
Std Dev	3.487

**Gaus mean : 31.9732**

**Gaus Width: 3.4061**



# B0L001S, U21-ch15, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	89
Mean	38.58
Std Dev	3.72

**Gaus mean : 39.5387**

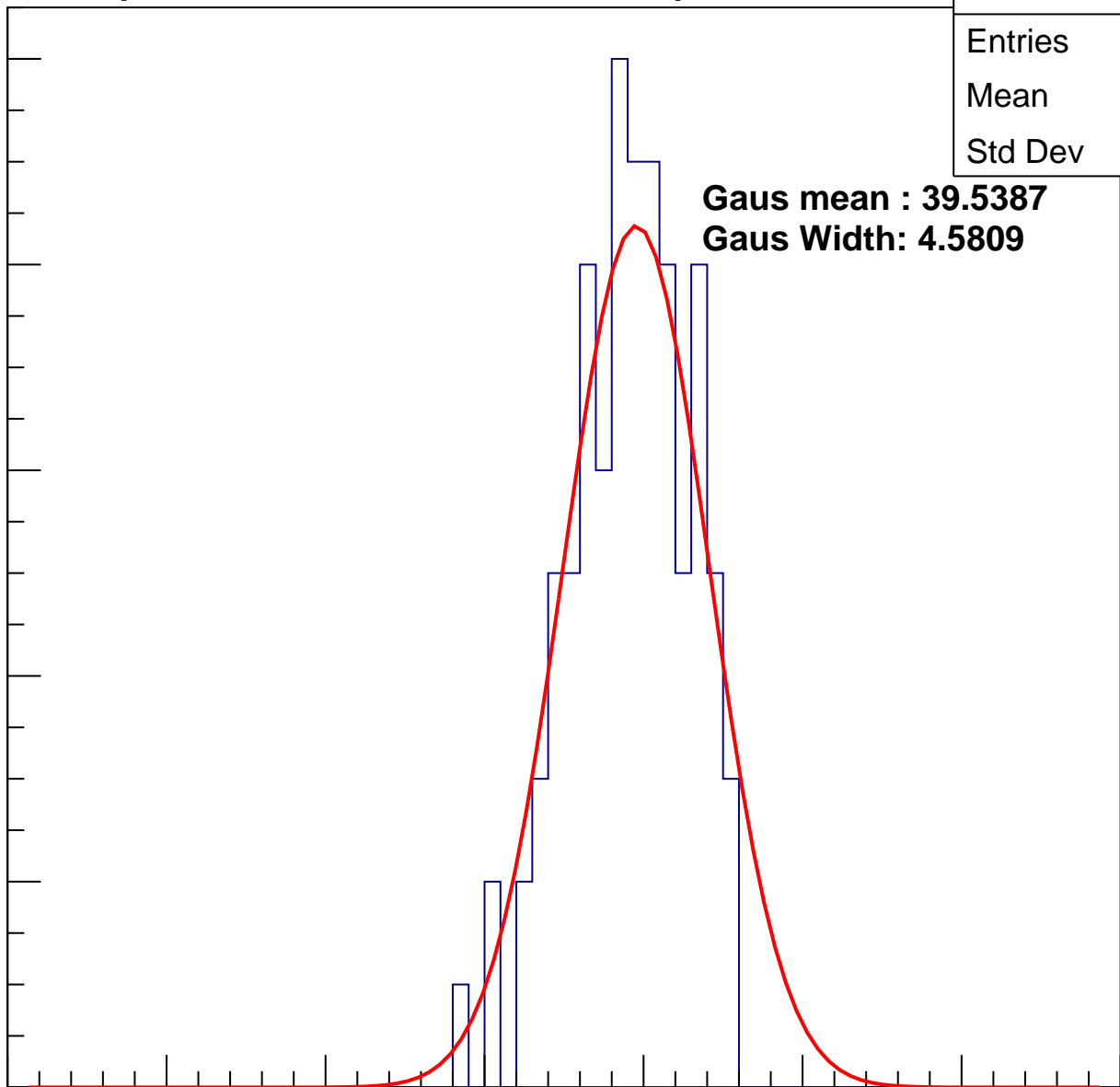
**Gaus Width: 4.5809**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U21-ch15, adc2

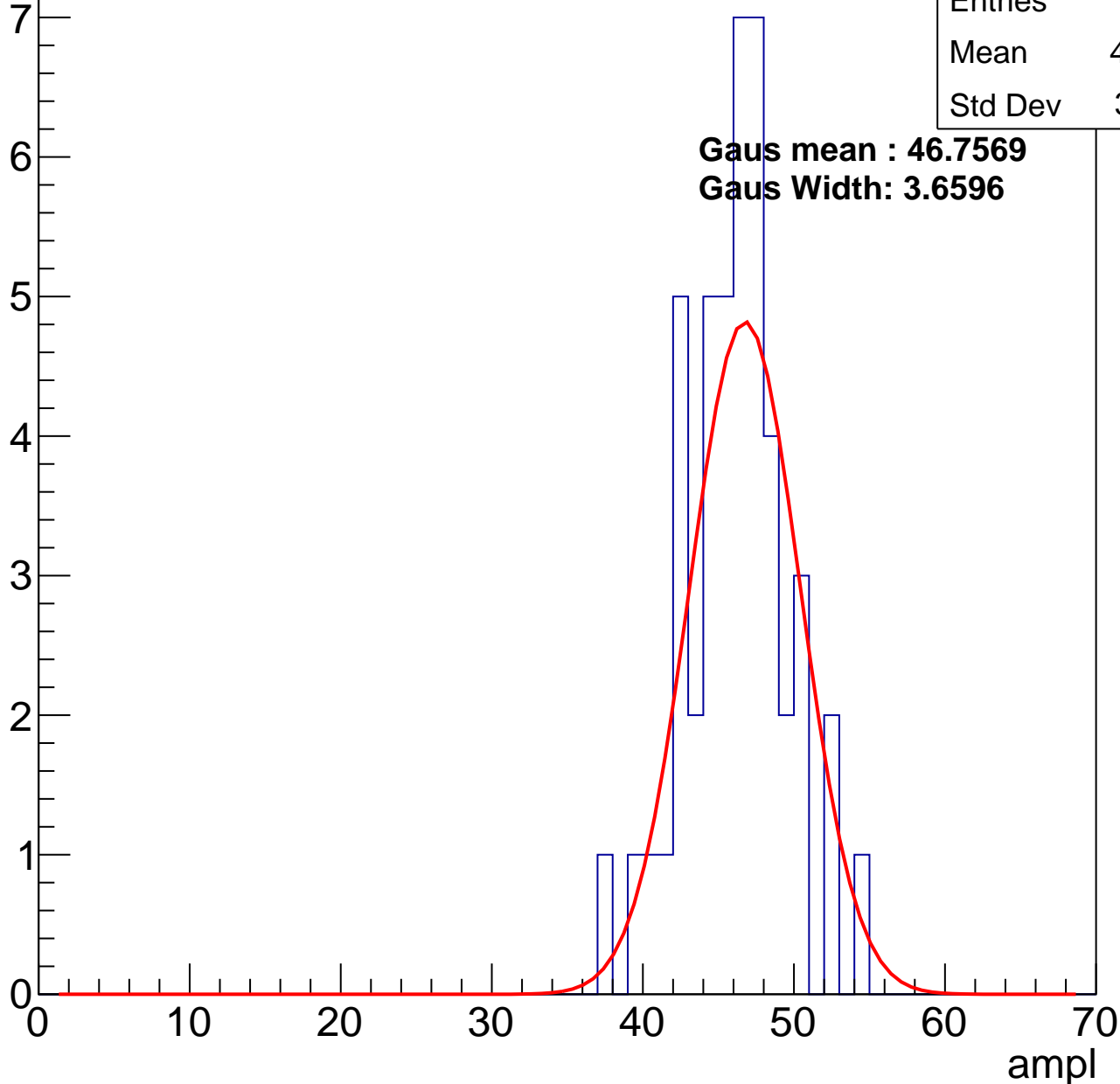
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	45.68
Std Dev	3.371

**Gaus mean : 46.7569**

**Gaus Width: 3.6596**

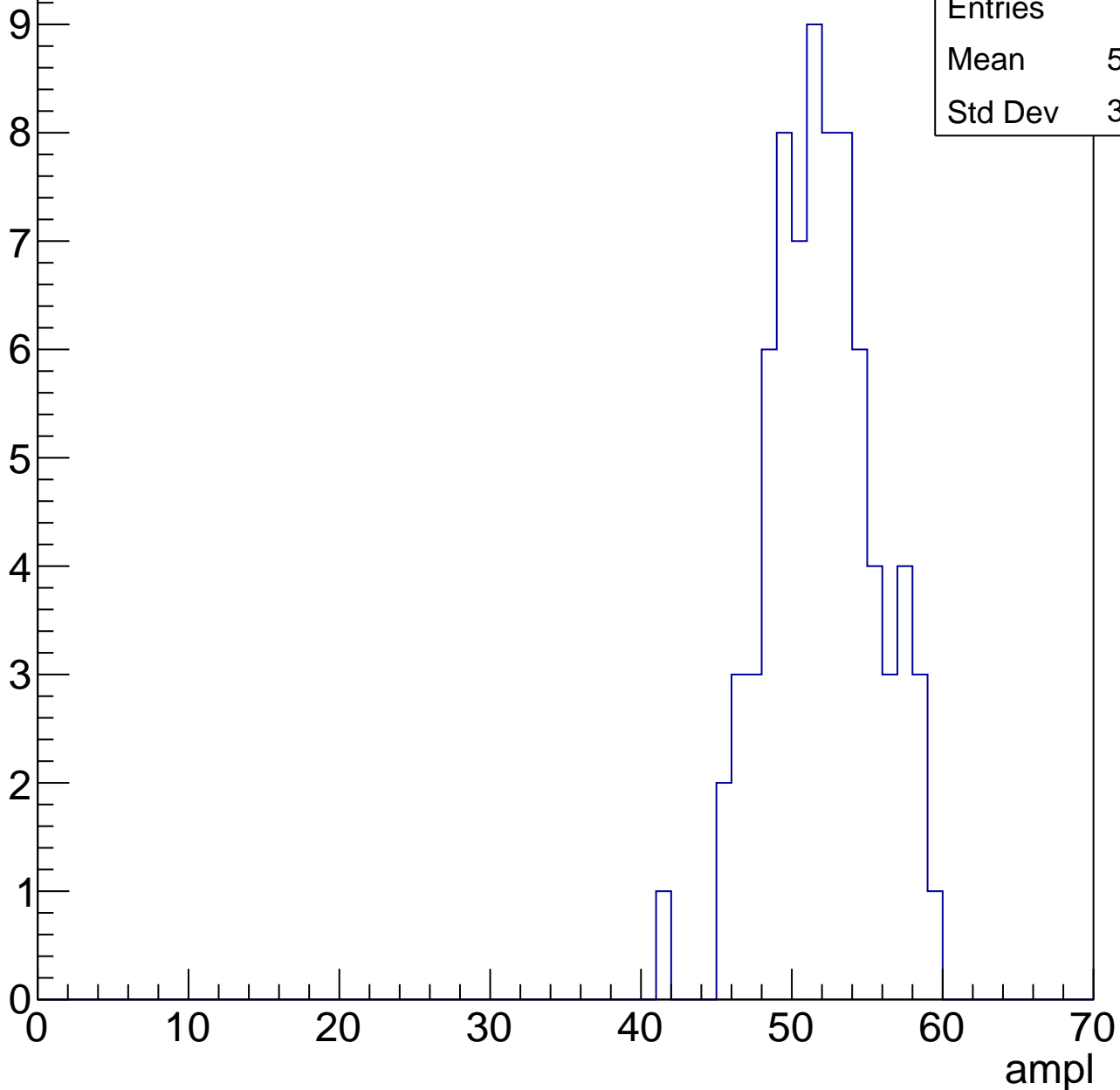


# B0L001S, U21-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

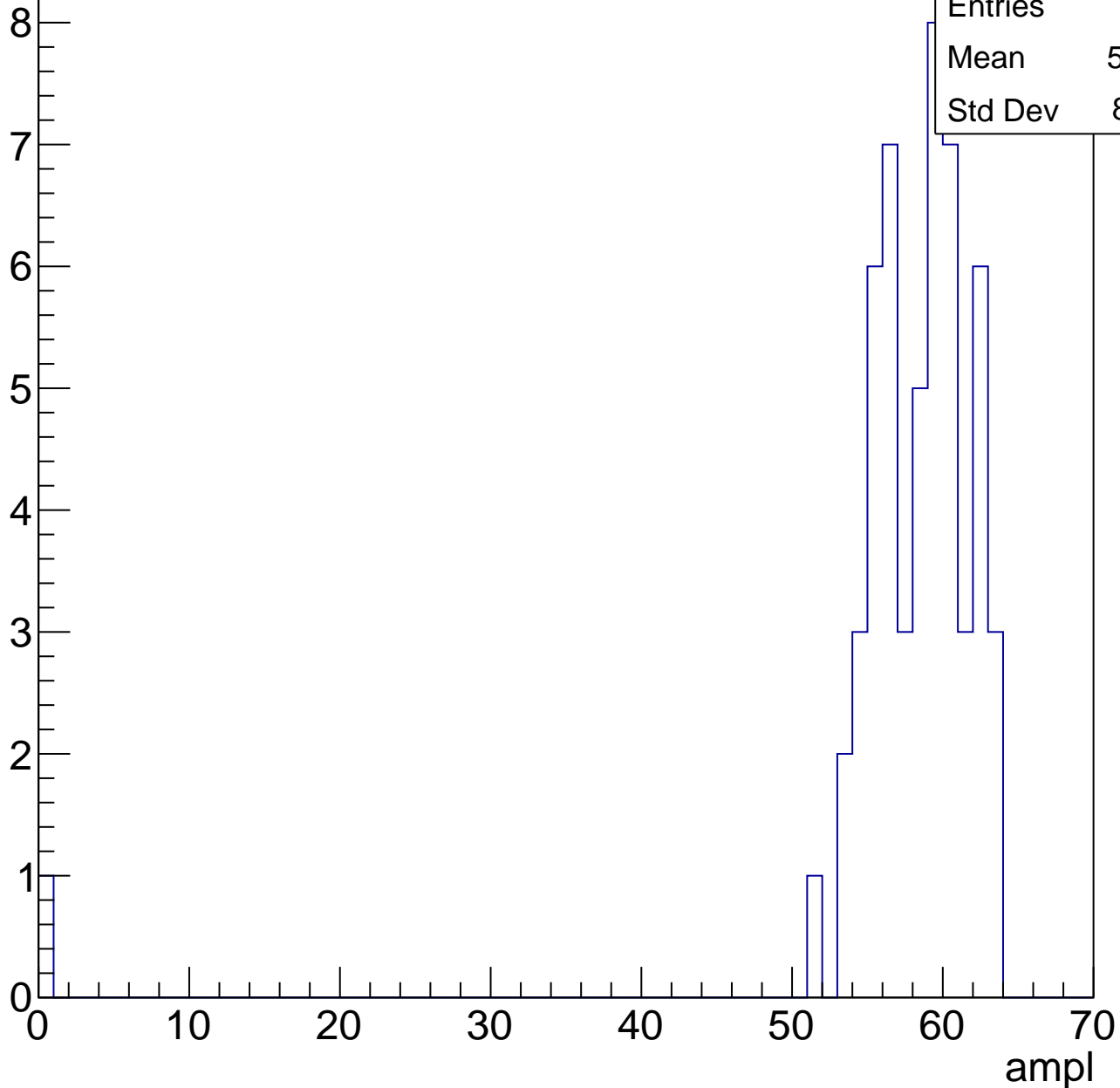
Entries	76
Mean	51.47
Std Dev	3.552



# B0L001S, U21-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

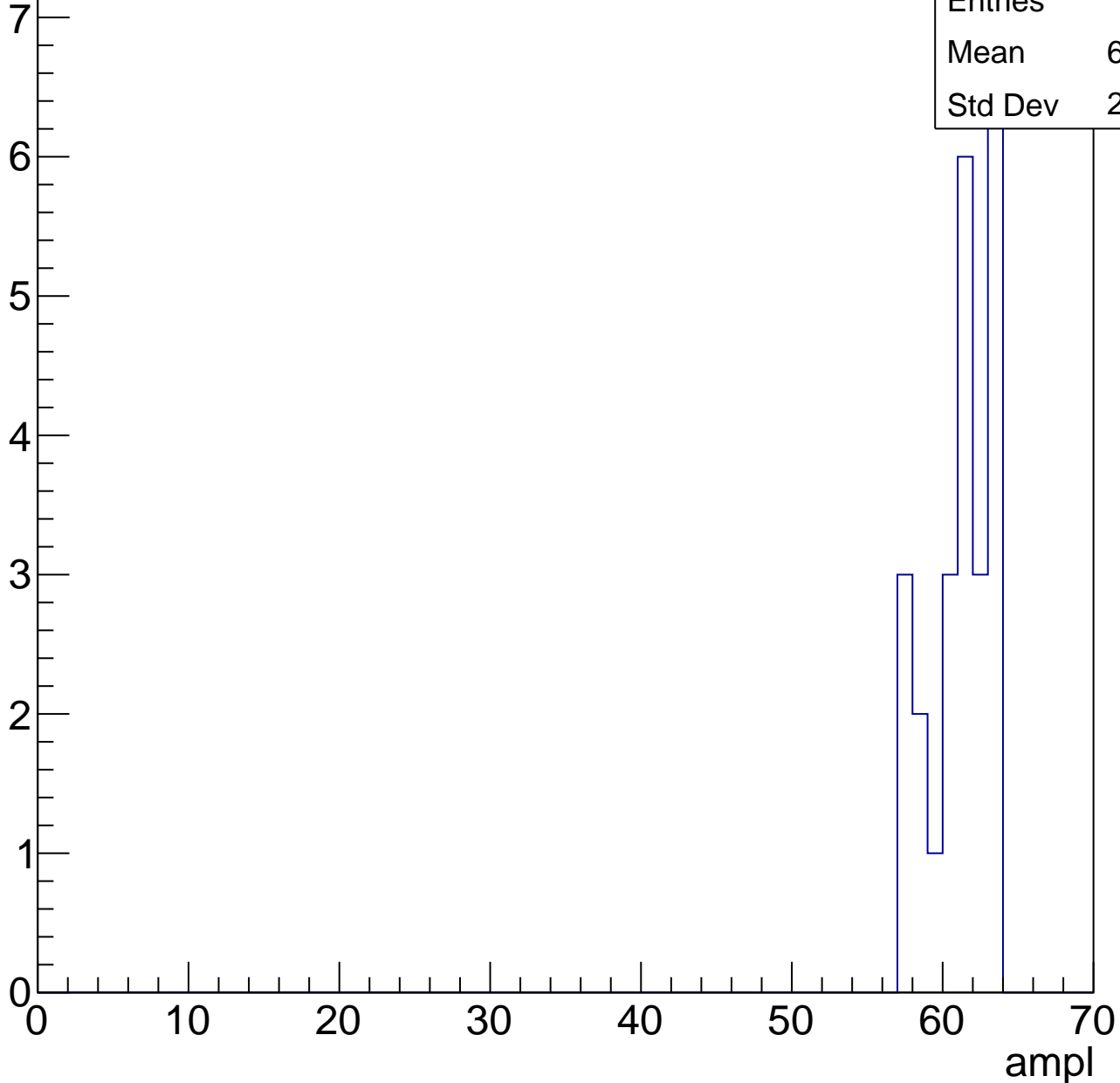


# B0L001S, U21-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	25
Mean	60.76
Std Dev	2.025



# B0L001S, U21-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch16, adc0

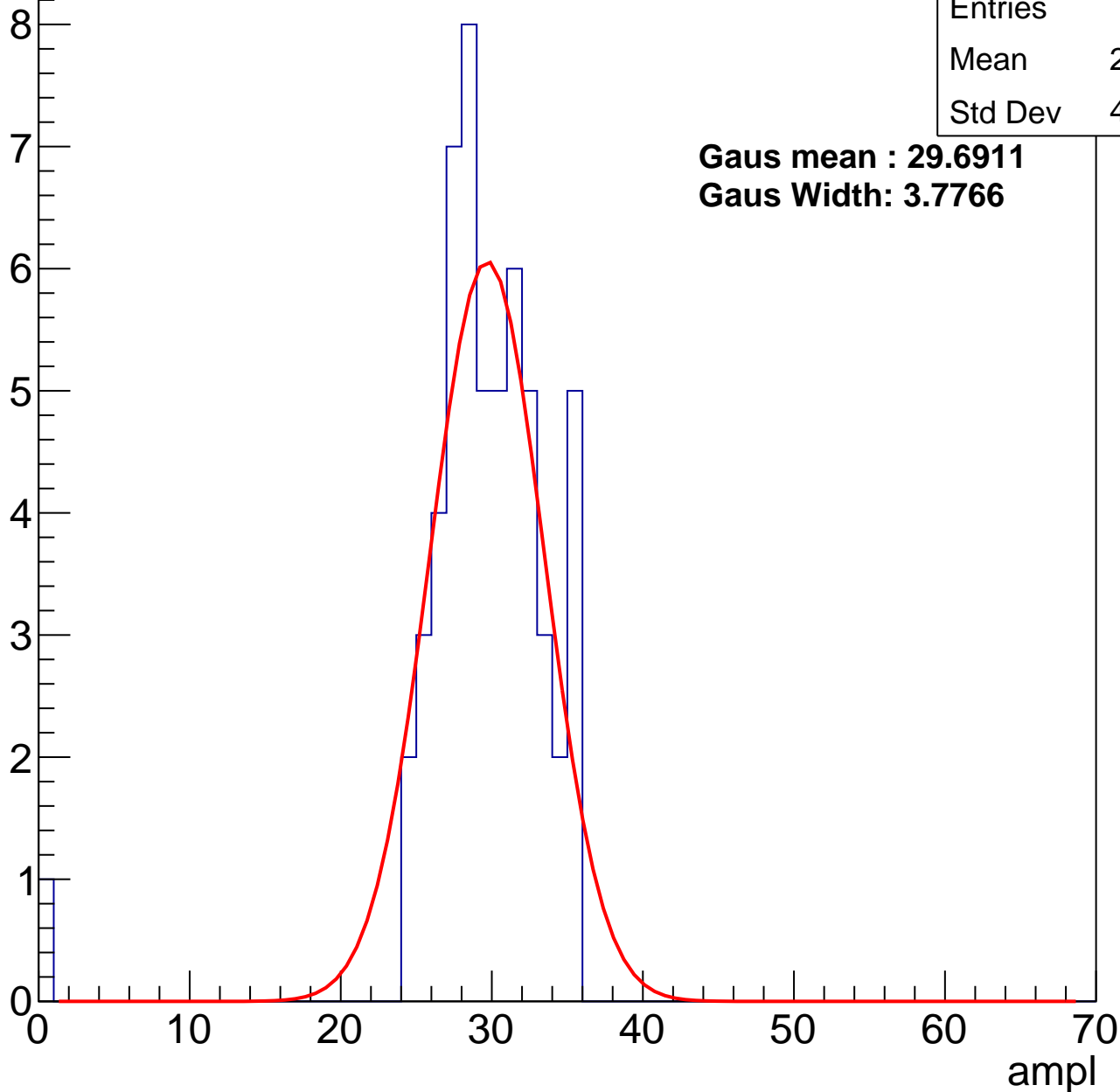
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	28.98
Std Dev	4.933

**Gaus mean : 29.6911**

**Gaus Width: 3.7766**

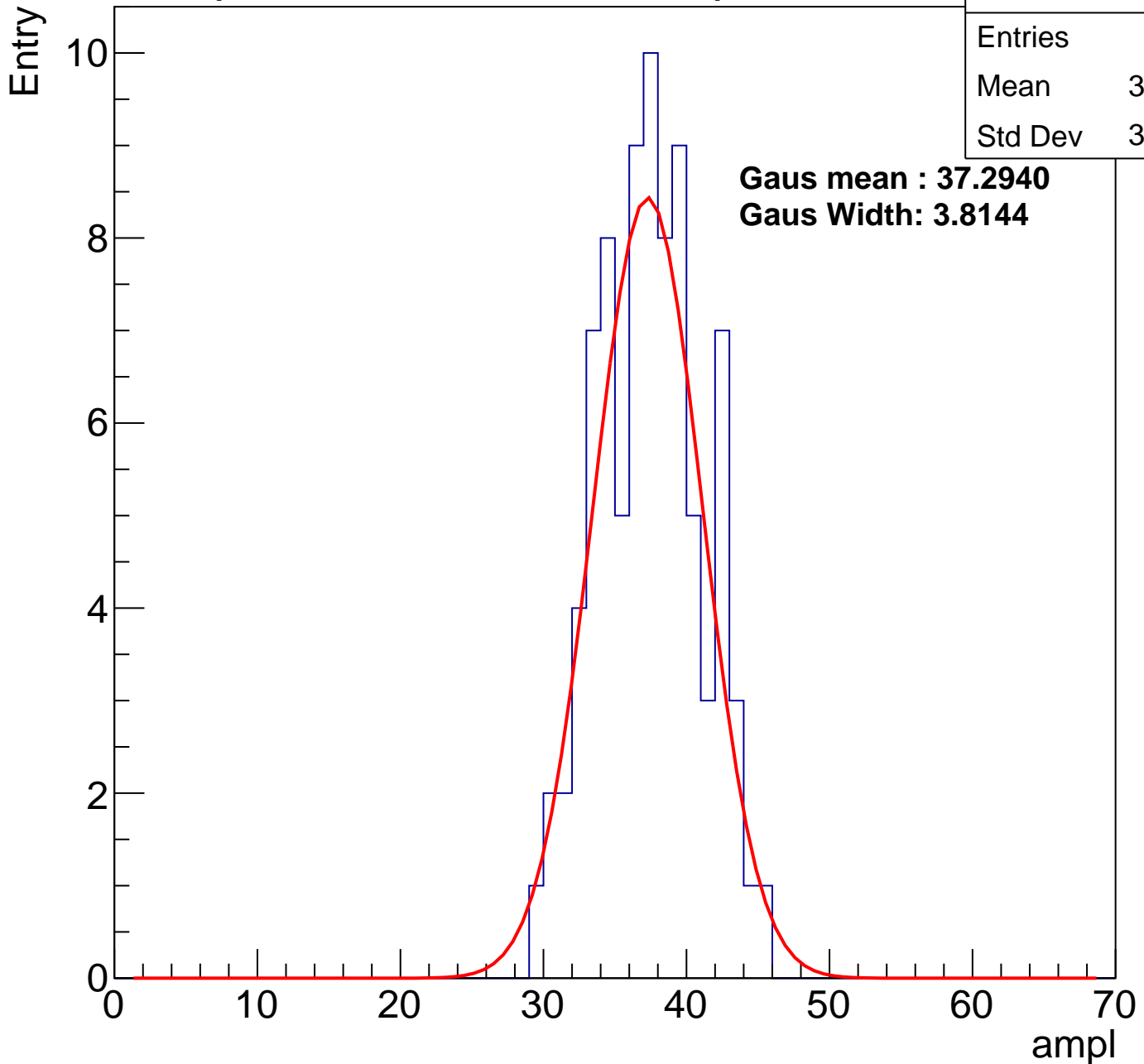


# B0L001S, U21-ch16, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	85
Mean	36.95
Std Dev	3.564

**Gaus mean : 37.2940**  
**Gaus Width: 3.8144**



# B0L001S, U21-ch16, adc2

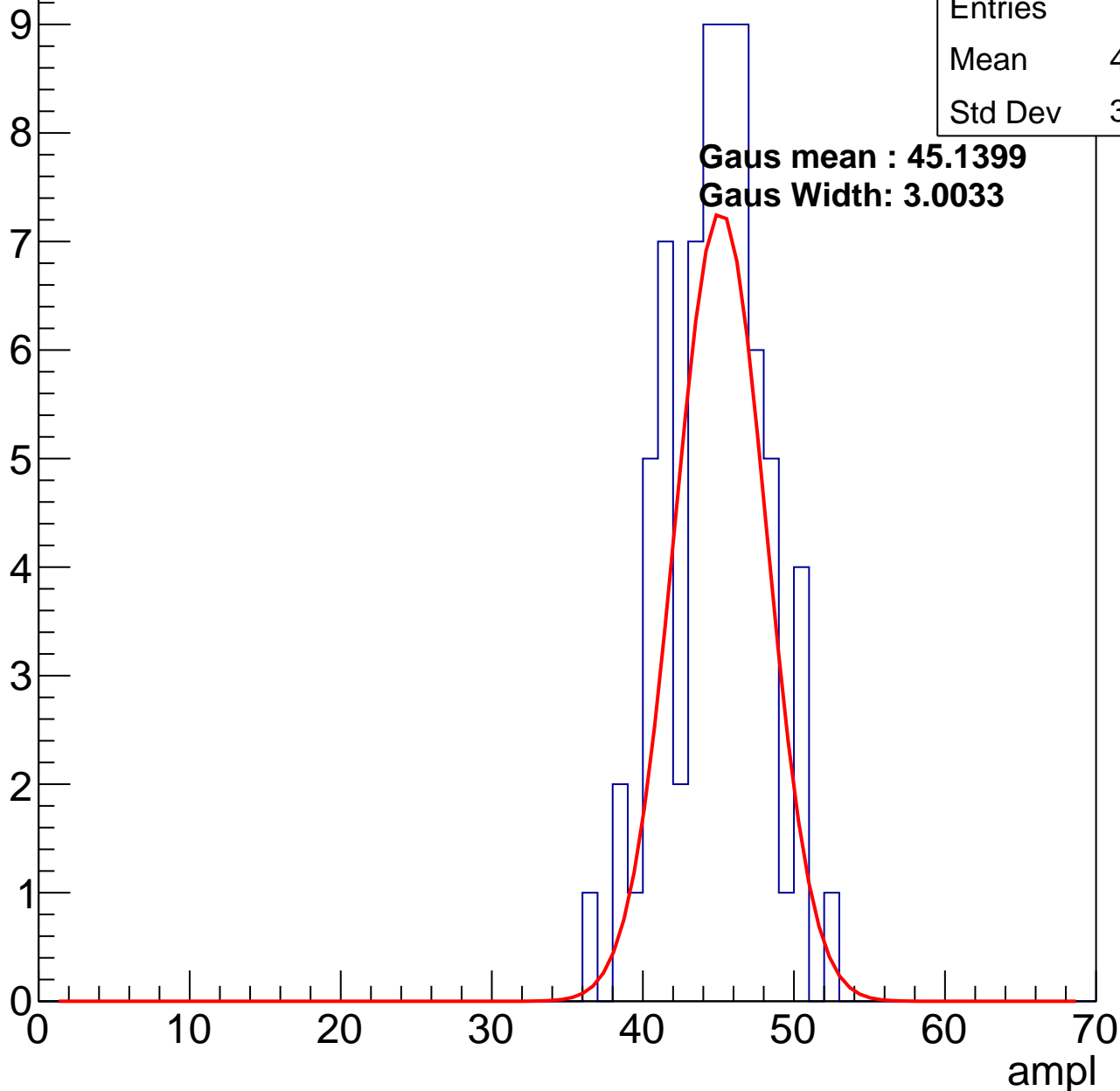
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	44.36
Std Dev	3.235

**Gaus mean : 45.1399**

**Gaus Width: 3.0033**

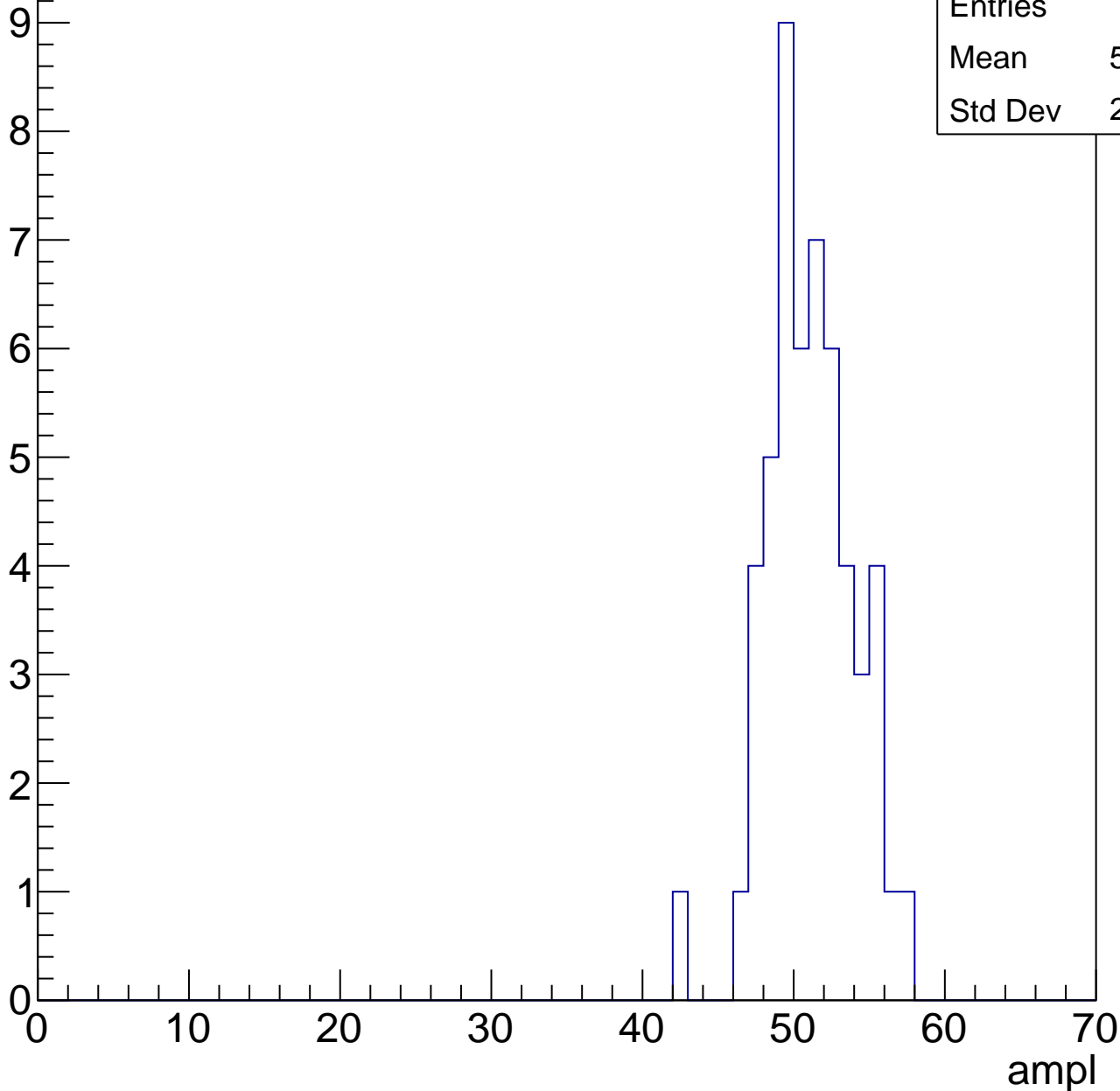


# B0L001S, U21-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	50.63
Std Dev	2.856

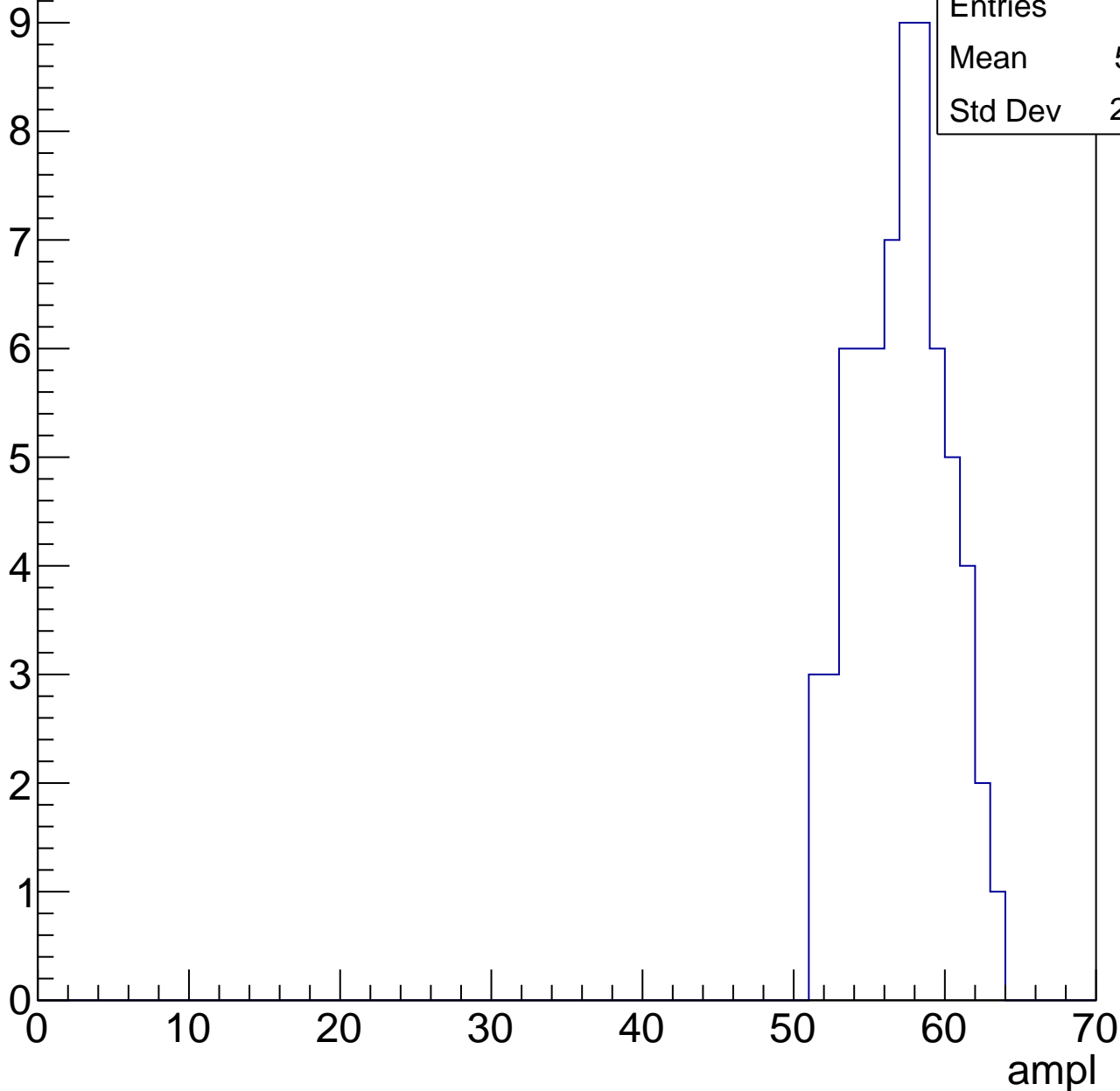


# B0L001S, U21-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

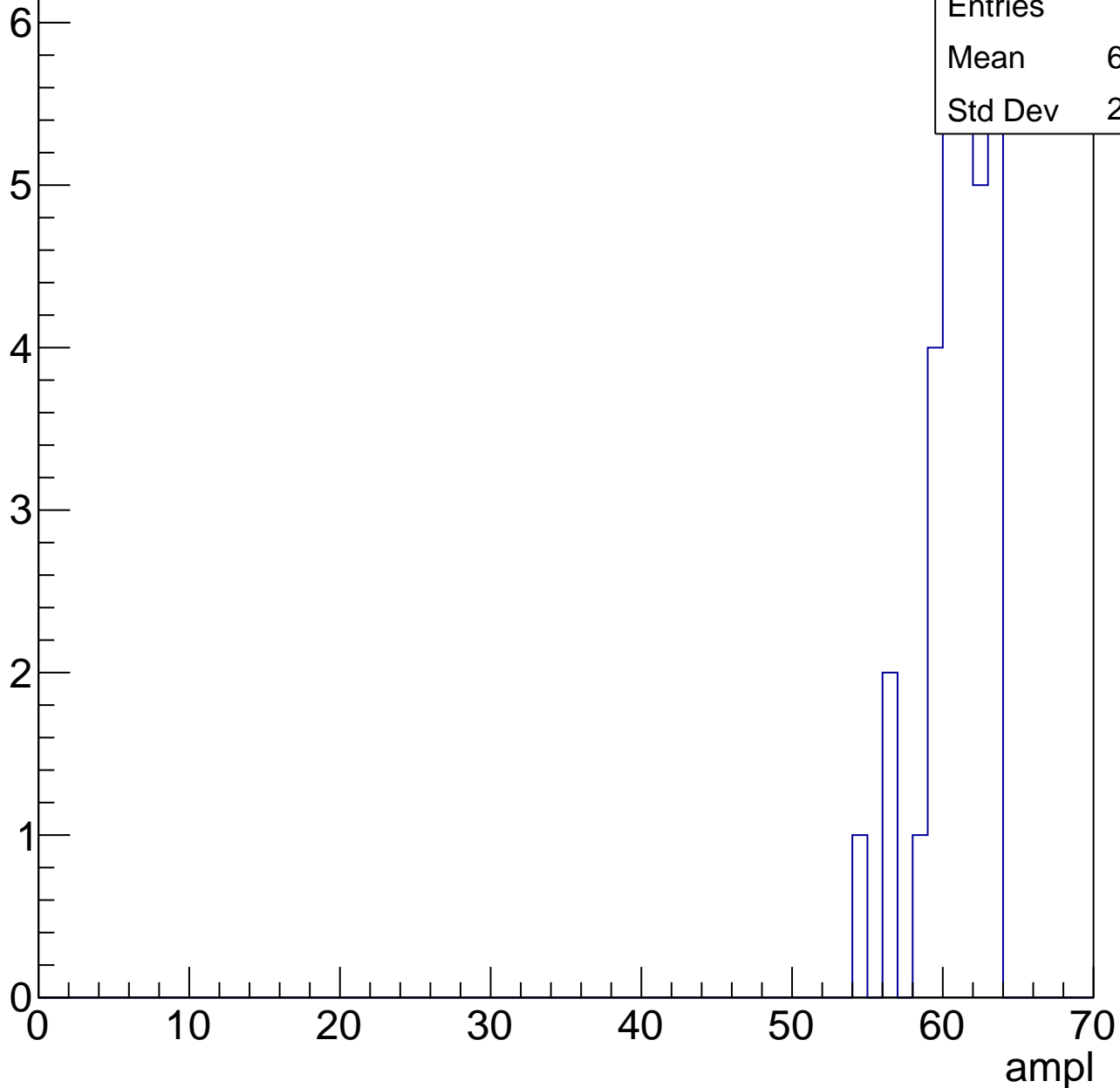
Entries	67
Mean	56.61
Std Dev	2.947



# B0L001S, U21-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

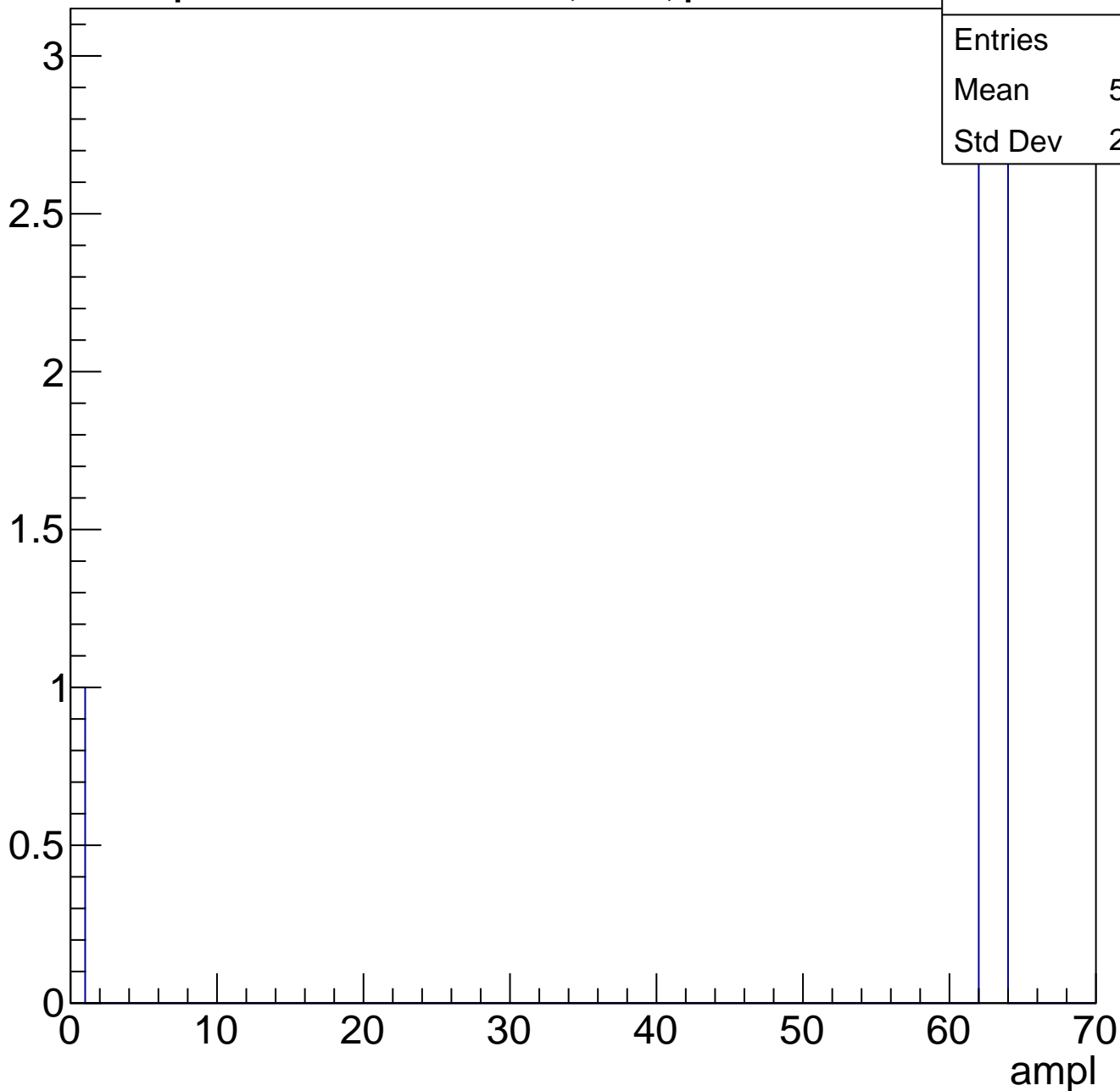
Entry



# B0L001S, U21-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	11.5
Std Dev	11.5

# B0L001S, U21-ch17, adc0

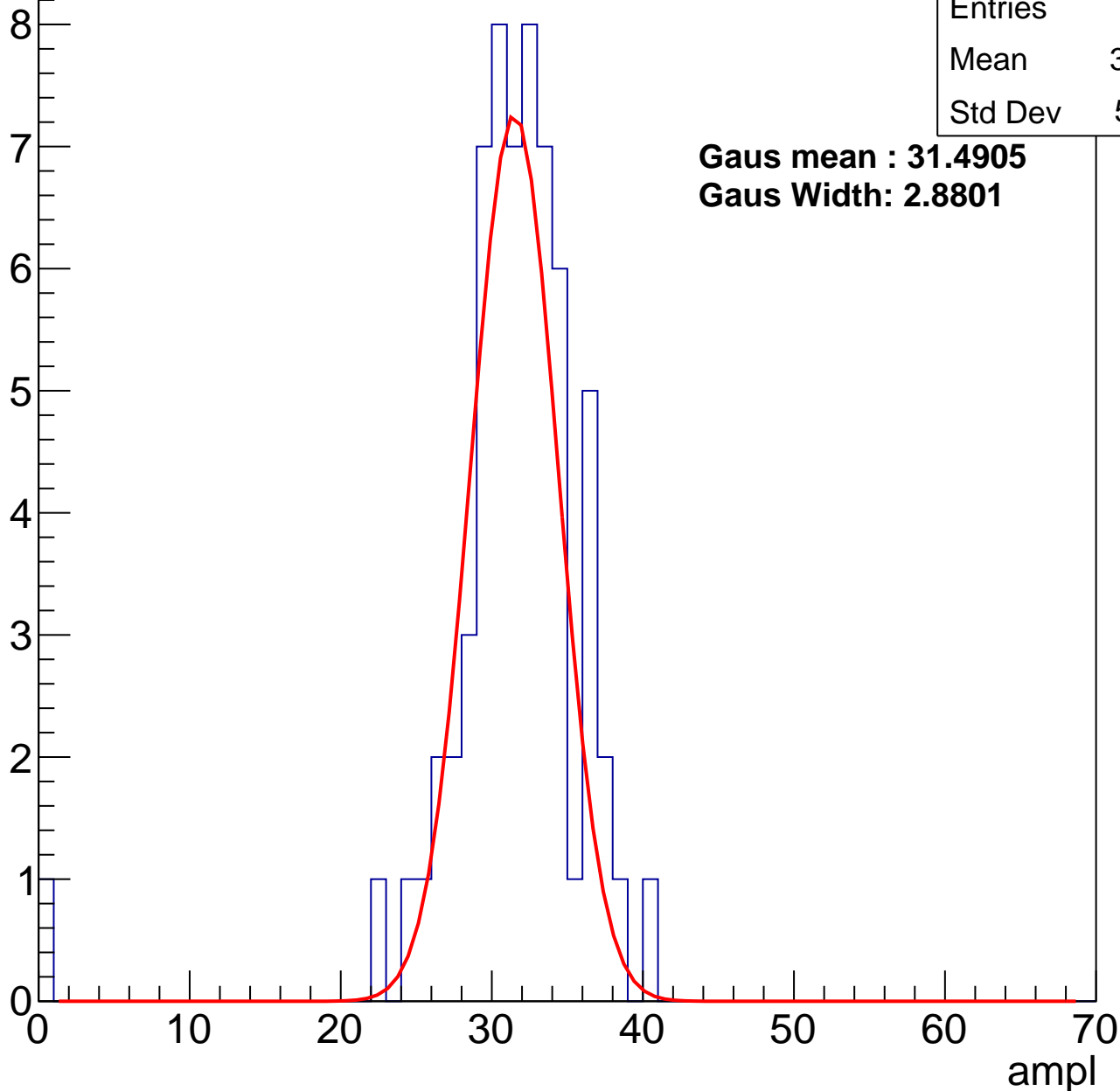
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	30.92
Std Dev	5.161

**Gaus mean : 31.4905**

**Gaus Width: 2.8801**



# B0L001S, U21-ch17, adc1

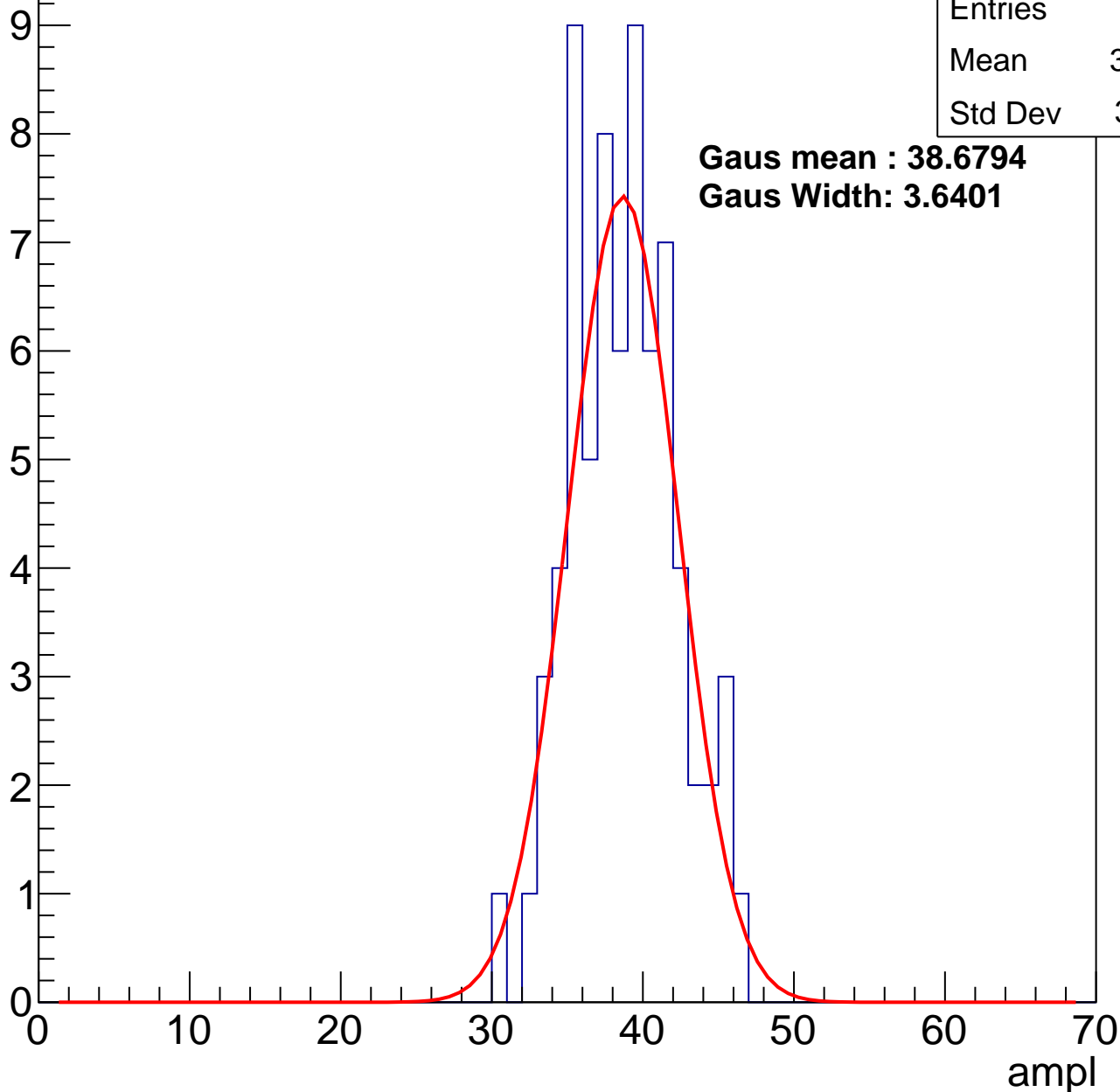
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	38.27
Std Dev	3.431

**Gaus mean : 38.6794**

**Gaus Width: 3.6401**



# B0L001S, U21-ch17, adc2

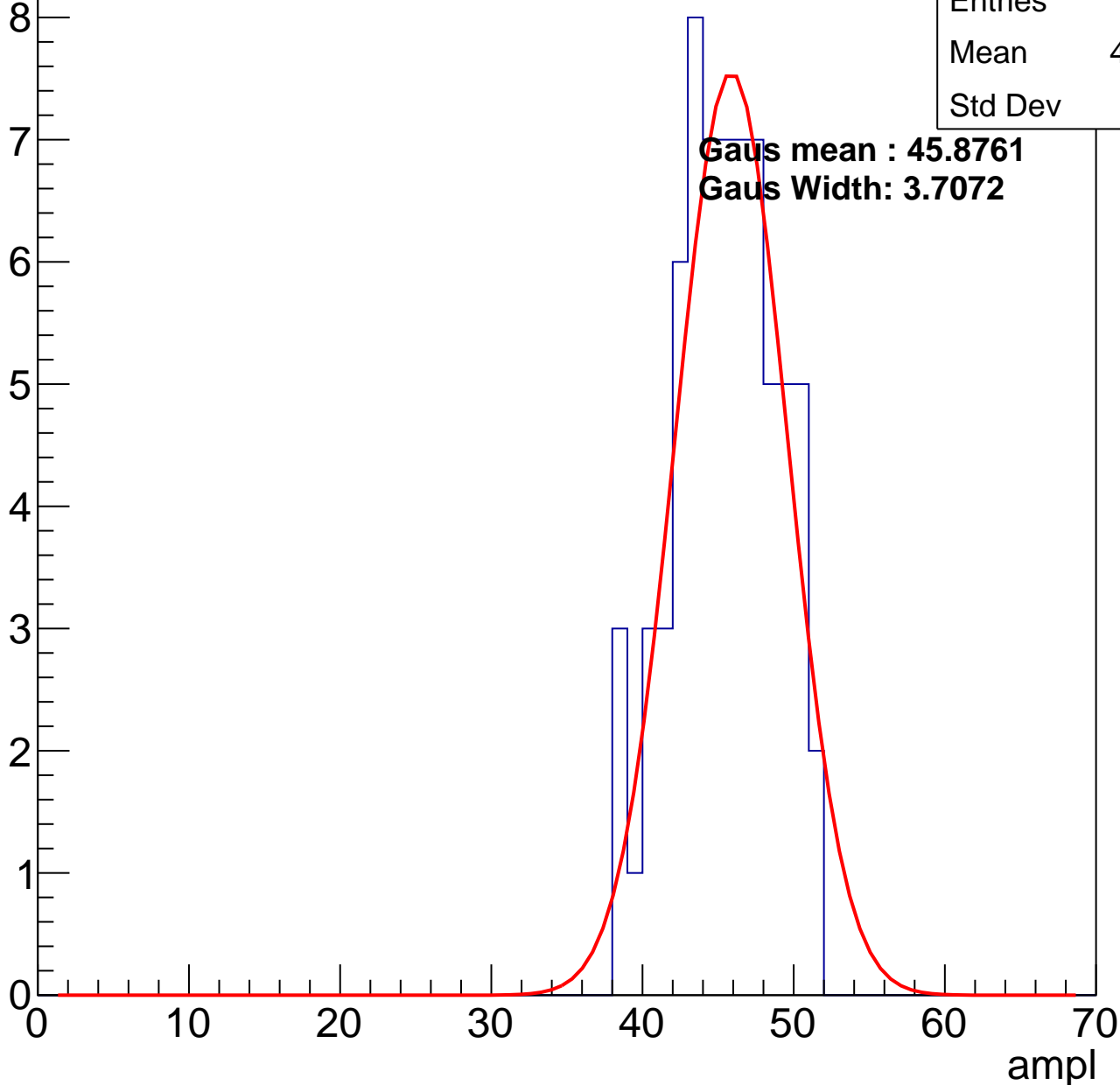
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	44.97
Std Dev	3.31

**Gaus mean : 45.8761**

**Gaus Width: 3.7072**

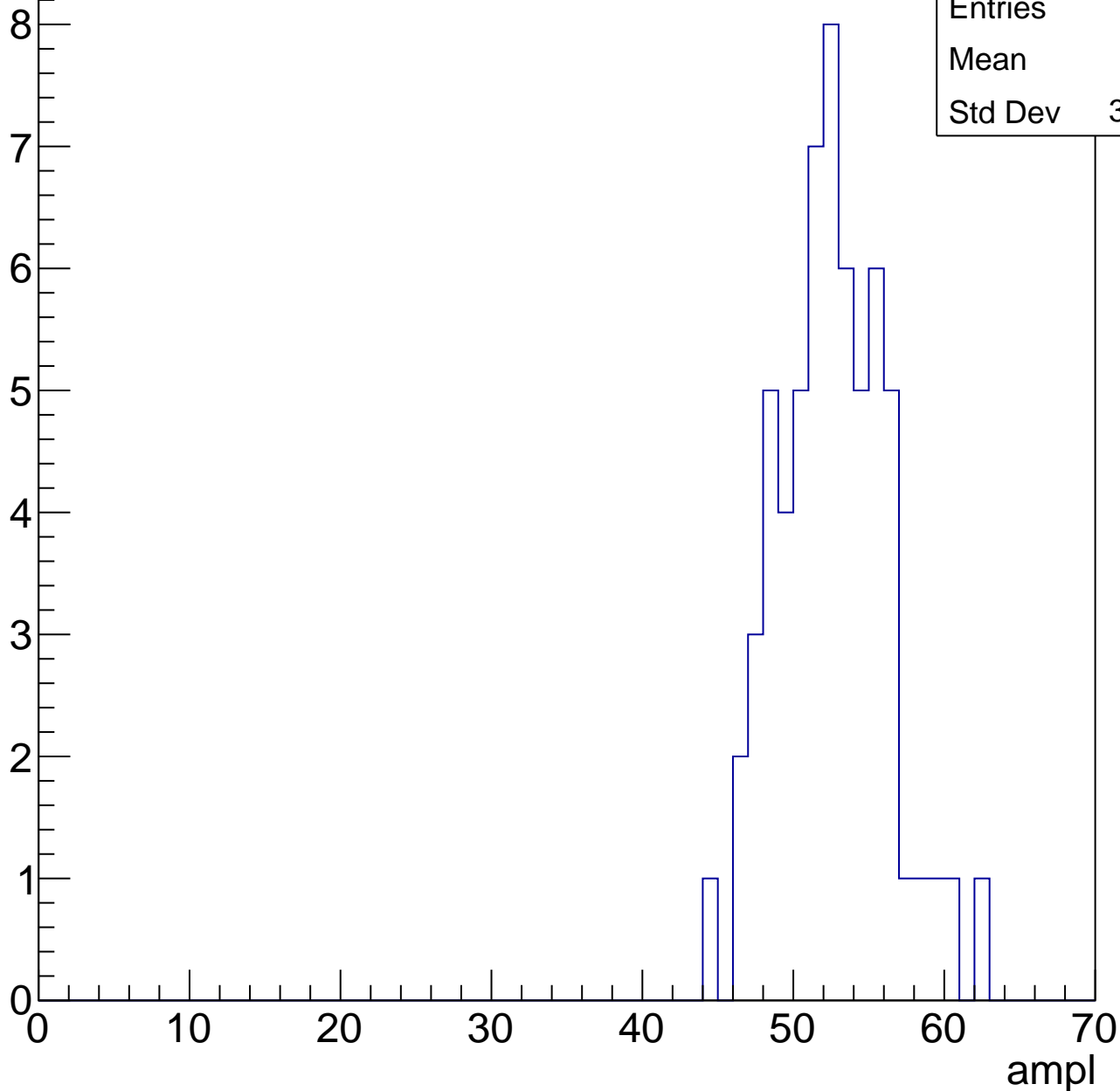


# B0L001S, U21-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	52.1
Std Dev	3.564

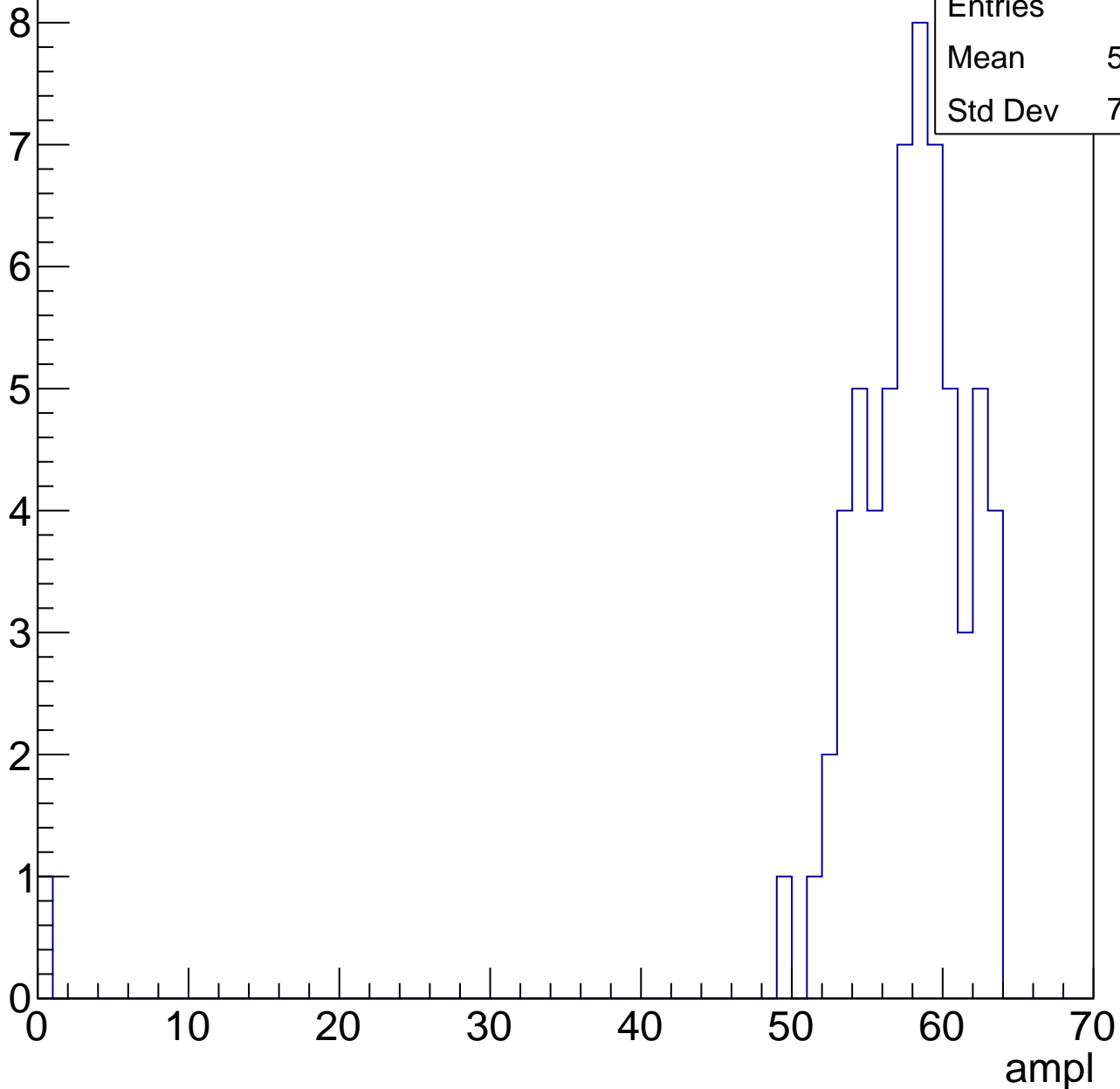


# B0L001S, U21-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

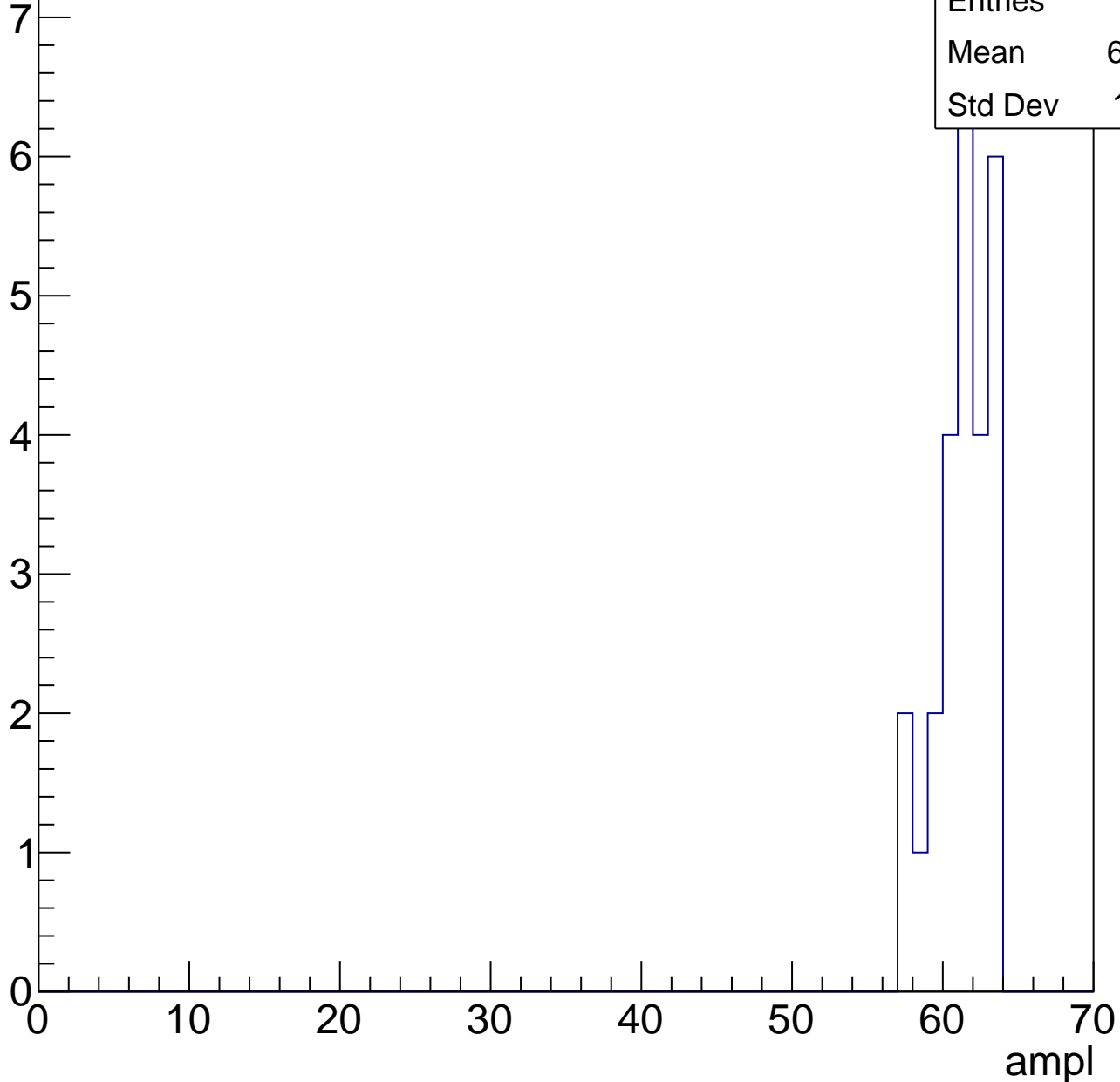
Entries	62
Mean	56.56
Std Dev	7.947



# B0L001S, U21-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	26
Mean	60.88
Std Dev	1.761

# B0L001S, U21-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U21-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U21-ch18, adc0

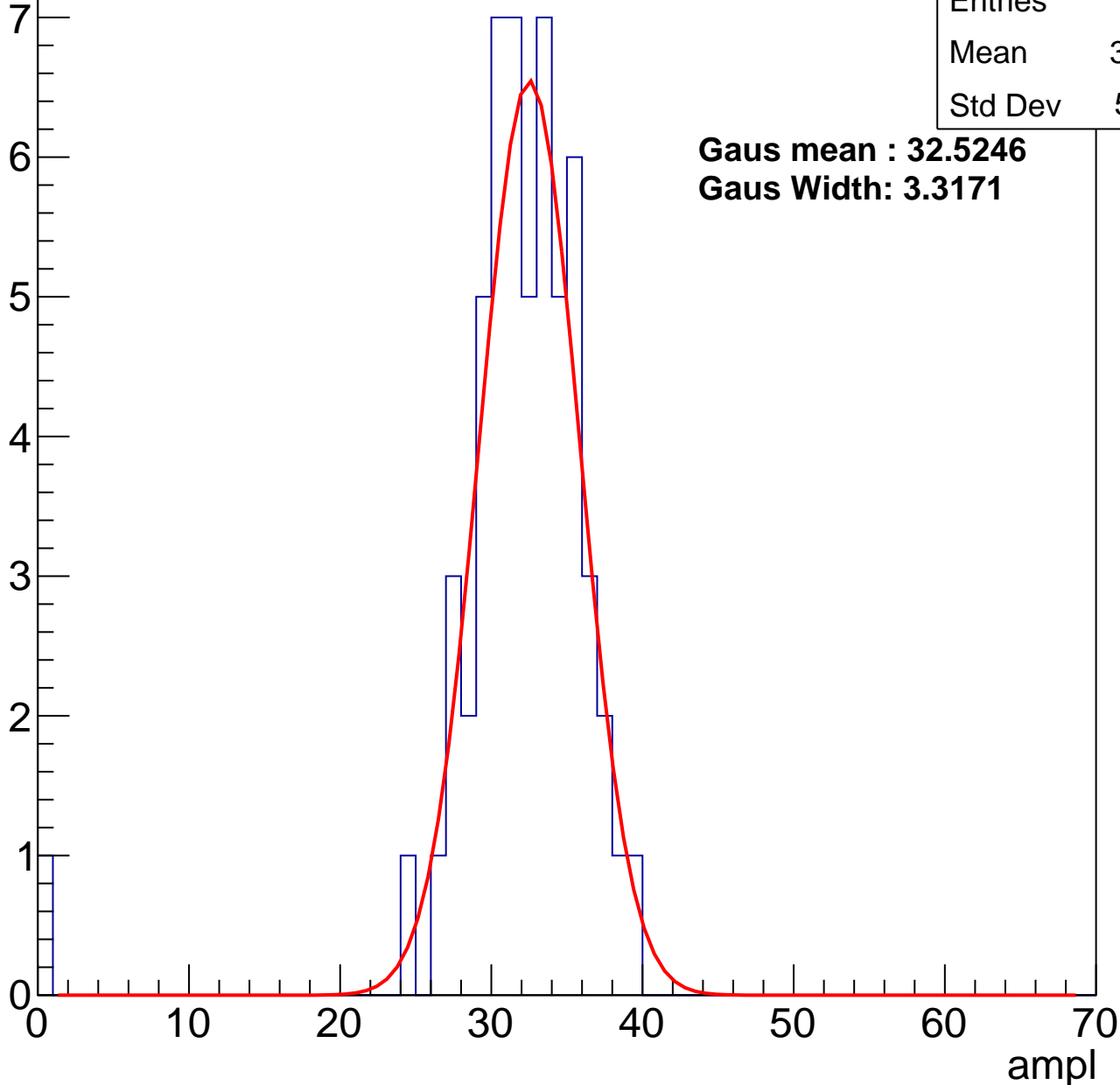
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	31.39
Std Dev	5.221

**Gaus mean : 32.5246**

**Gaus Width: 3.3171**



# B0L001S, U21-ch18, adc1

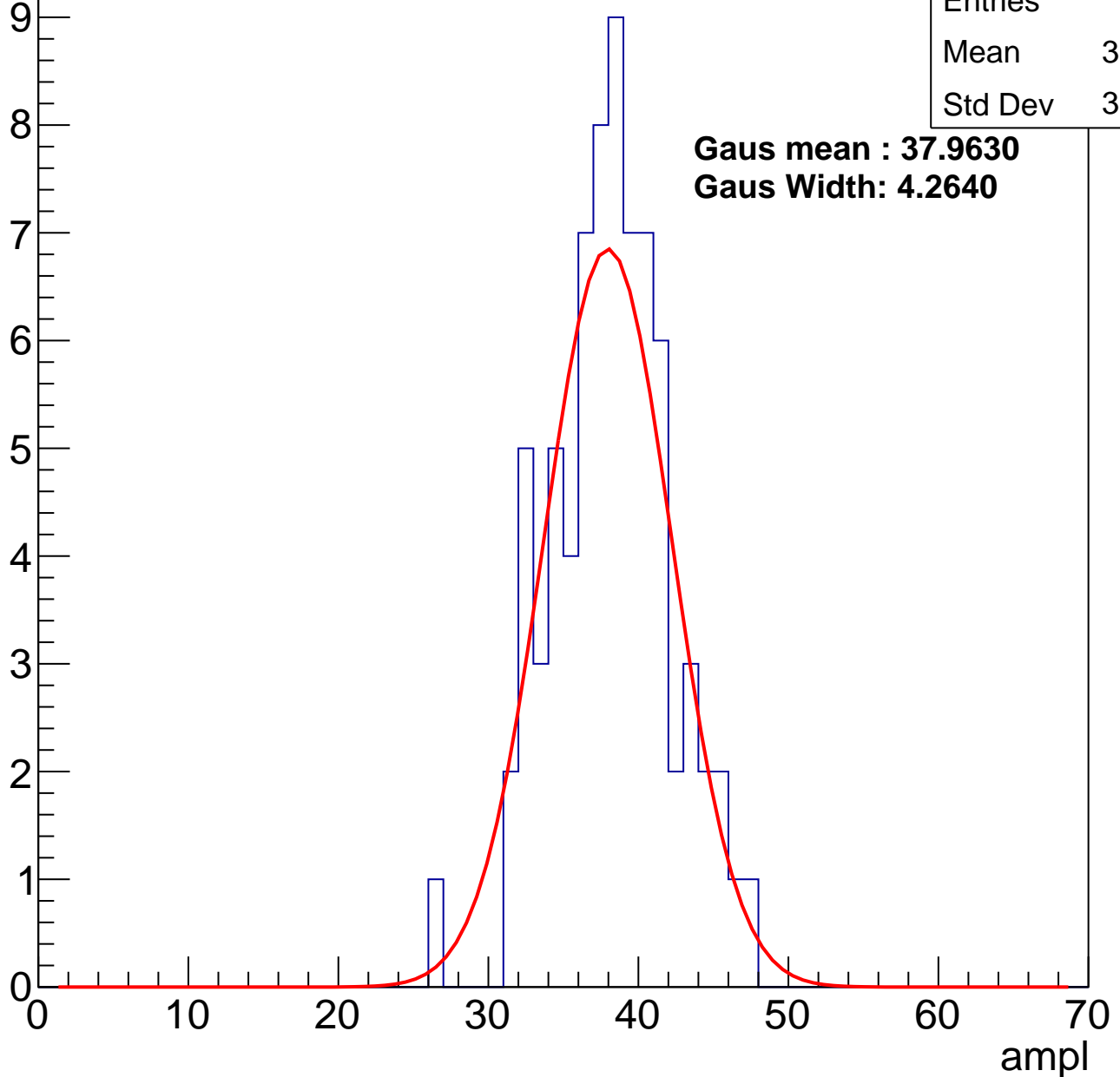
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	37.73
Std Dev	3.924

**Gaus mean : 37.9630**

**Gaus Width: 4.2640**



# B0L001S, U21-ch18, adc2

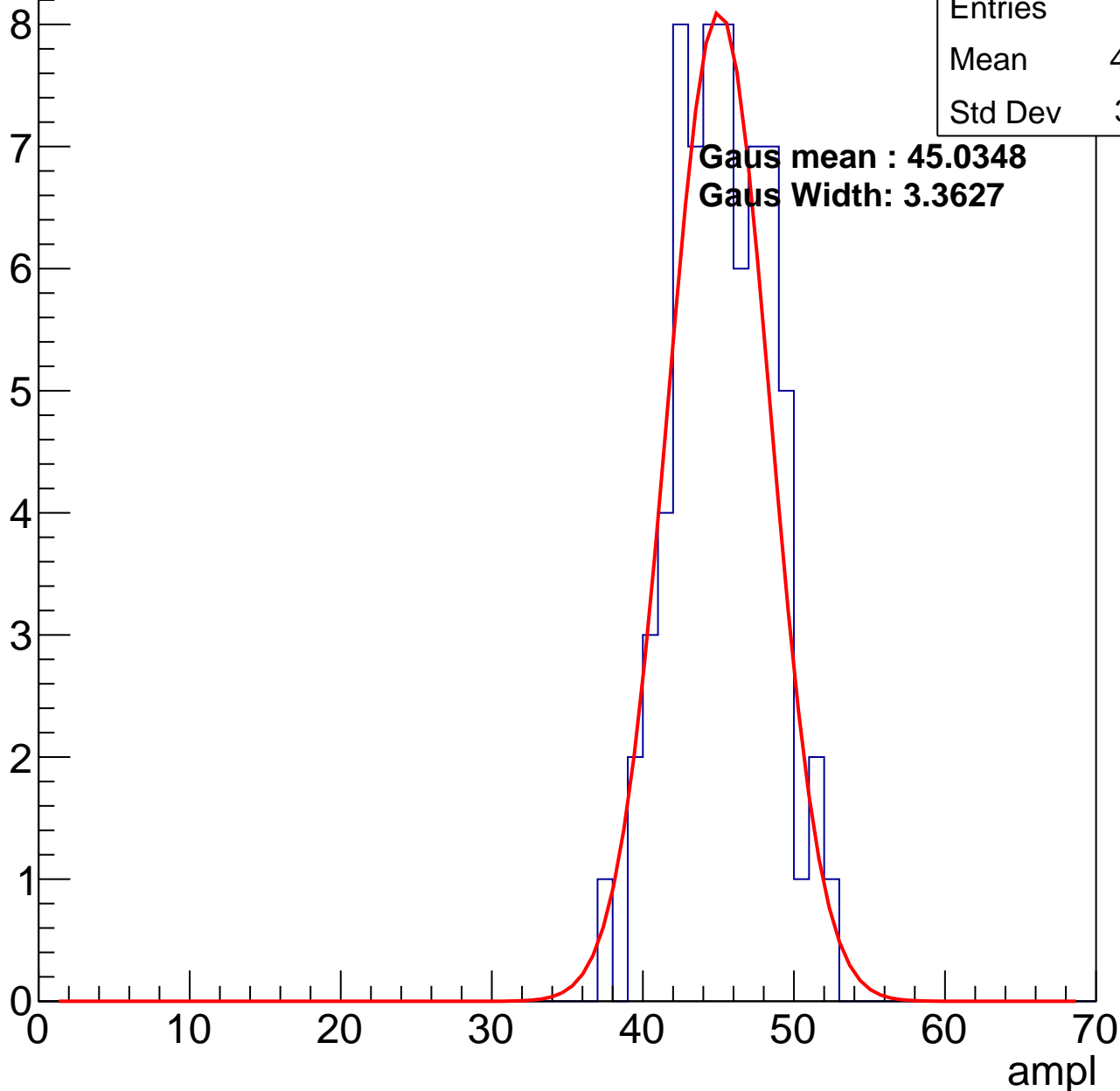
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	44.83
Std Dev	3.171

**Gaus mean : 45.0348**

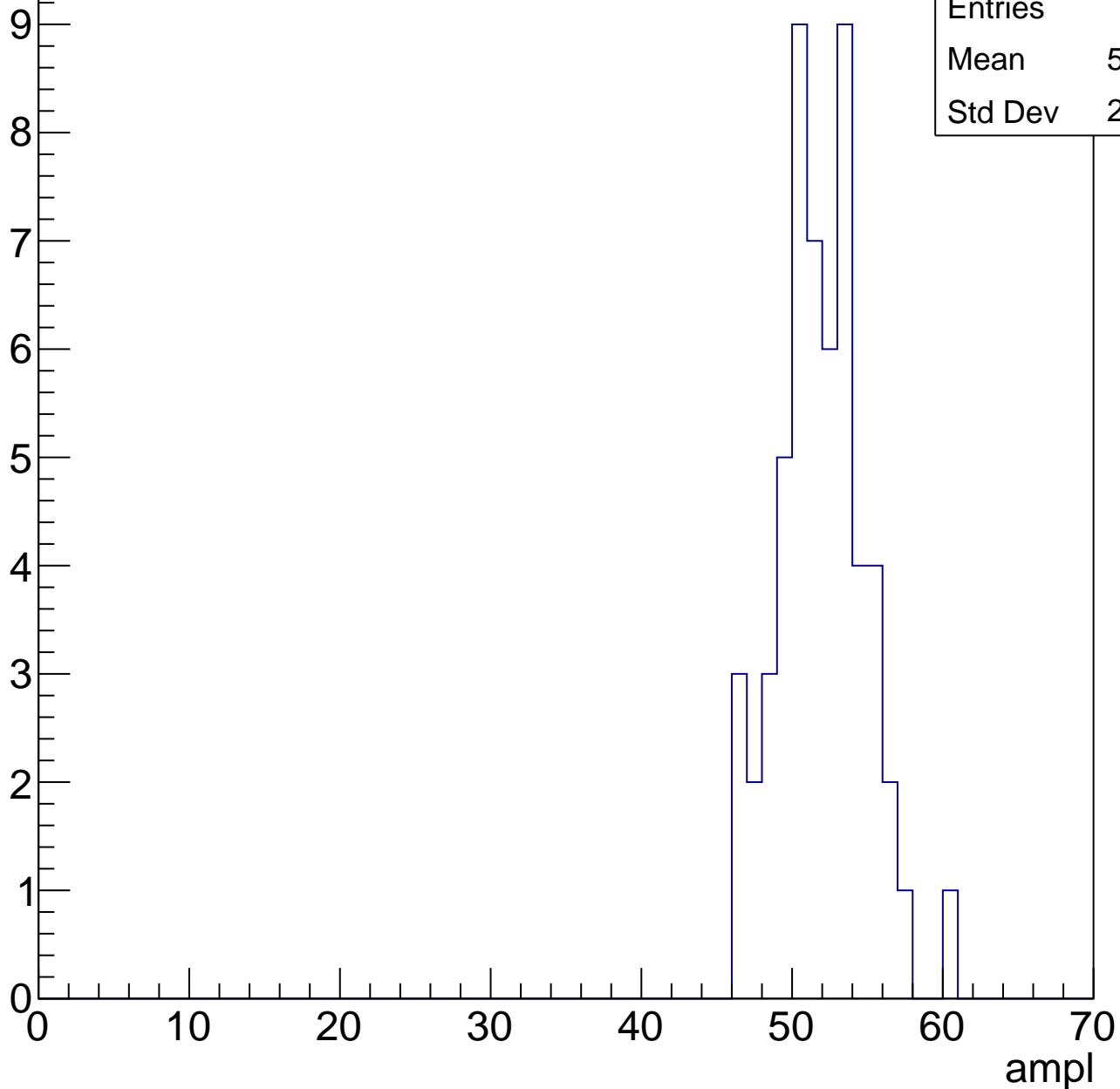
**Gaus Width: 3.3627**



# B0L001S, U21-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

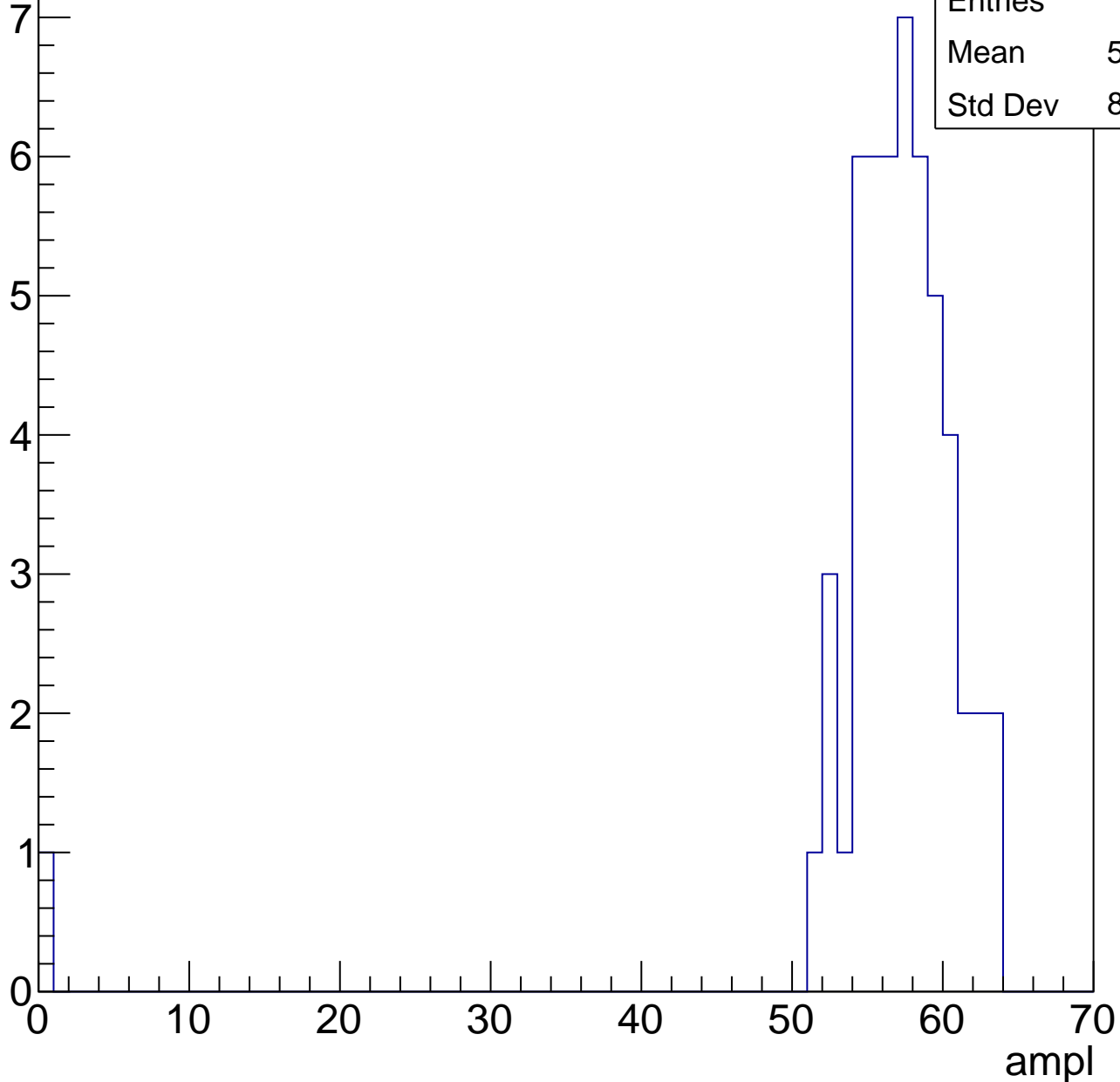
Entry



# B0L001S, U21-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



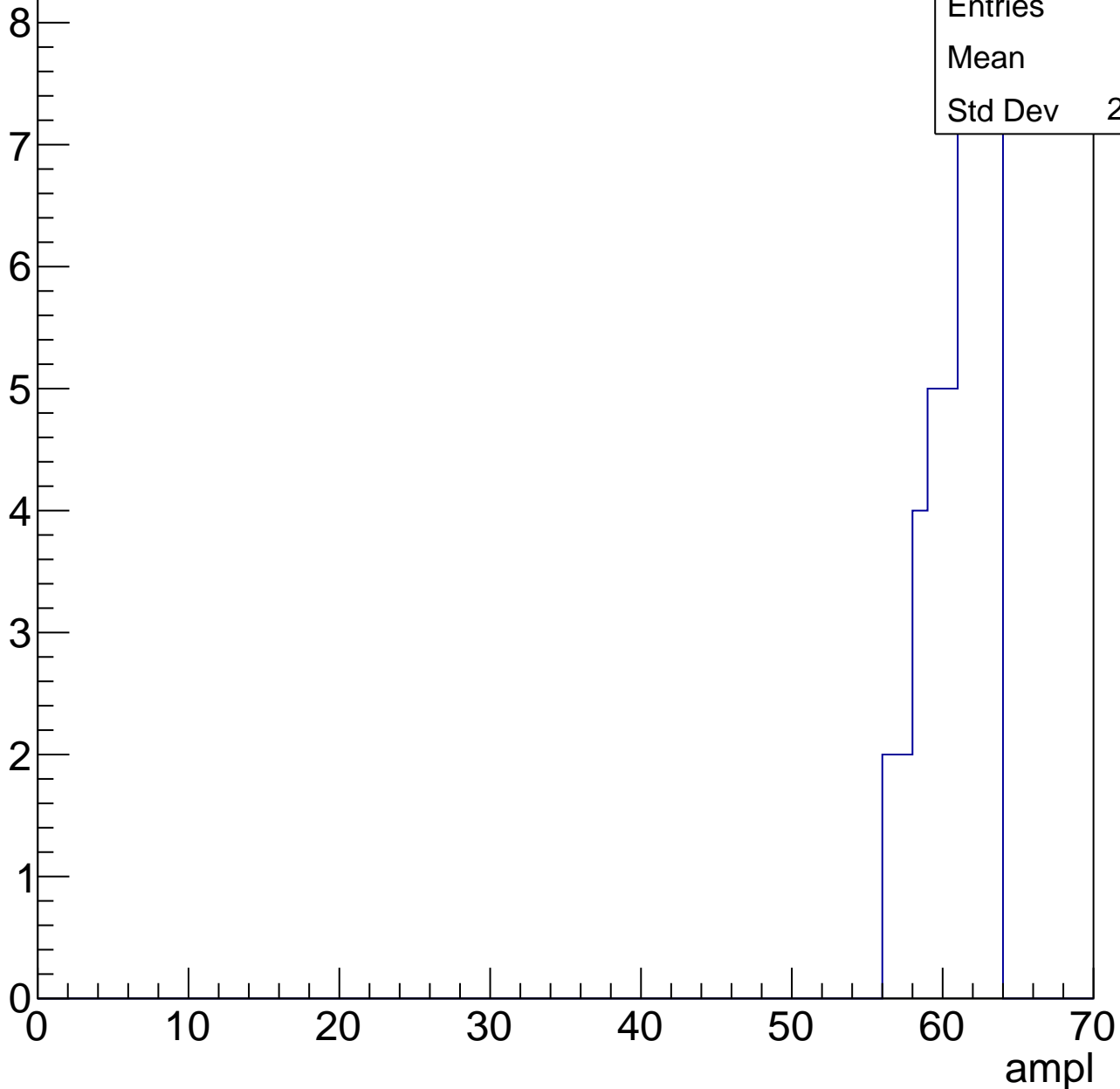
Entries	52
Mean	55.85
Std Dev	8.328

# B0L001S, U21-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	42
Mean	60.5
Std Dev	2.027



# B0L001S, U21-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U21-ch19, adc0

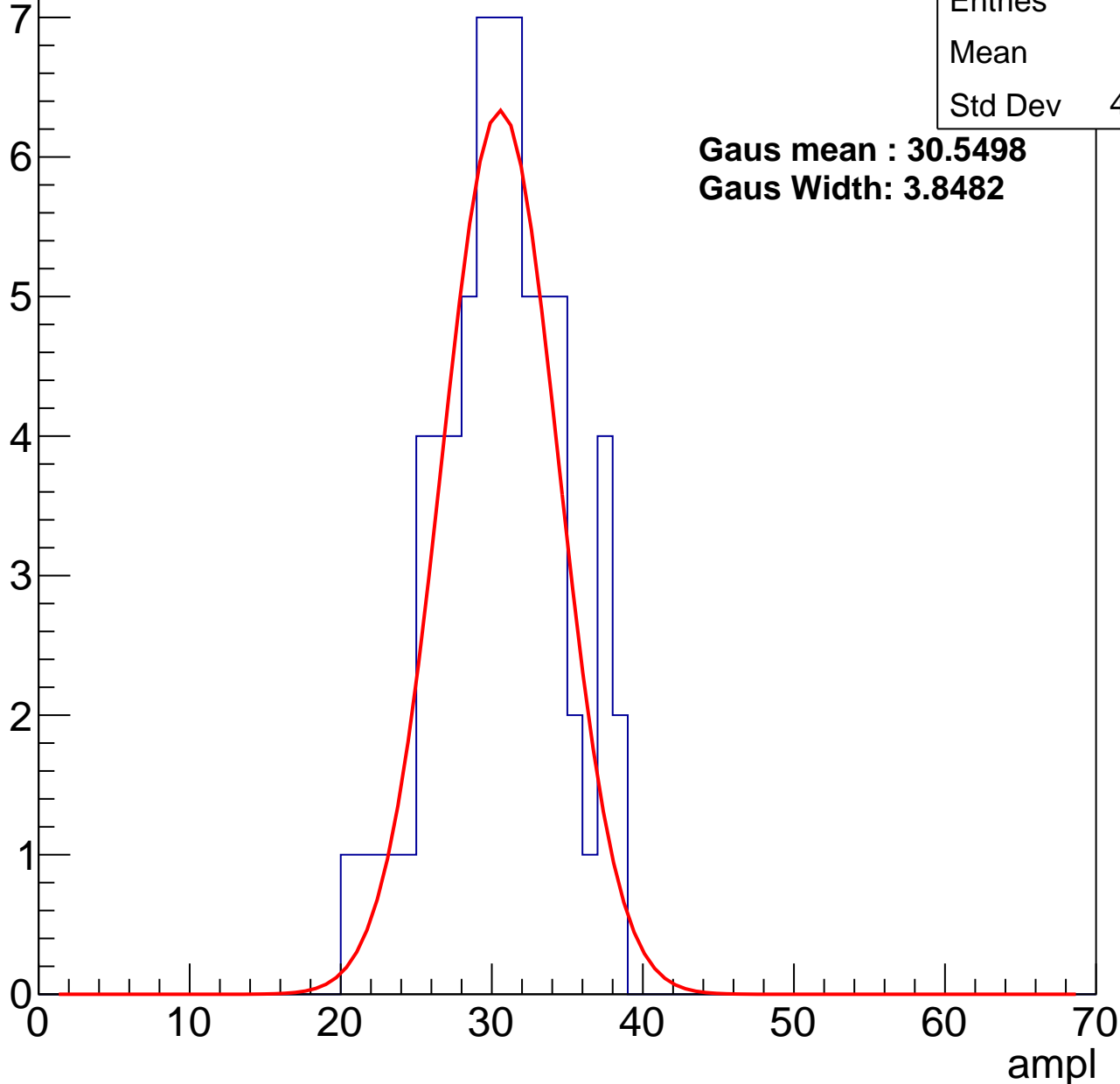
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	30.1
Std Dev	4.085

**Gaus mean : 30.5498**

**Gaus Width: 3.8482**



# B0L001S, U21-ch19, adc1

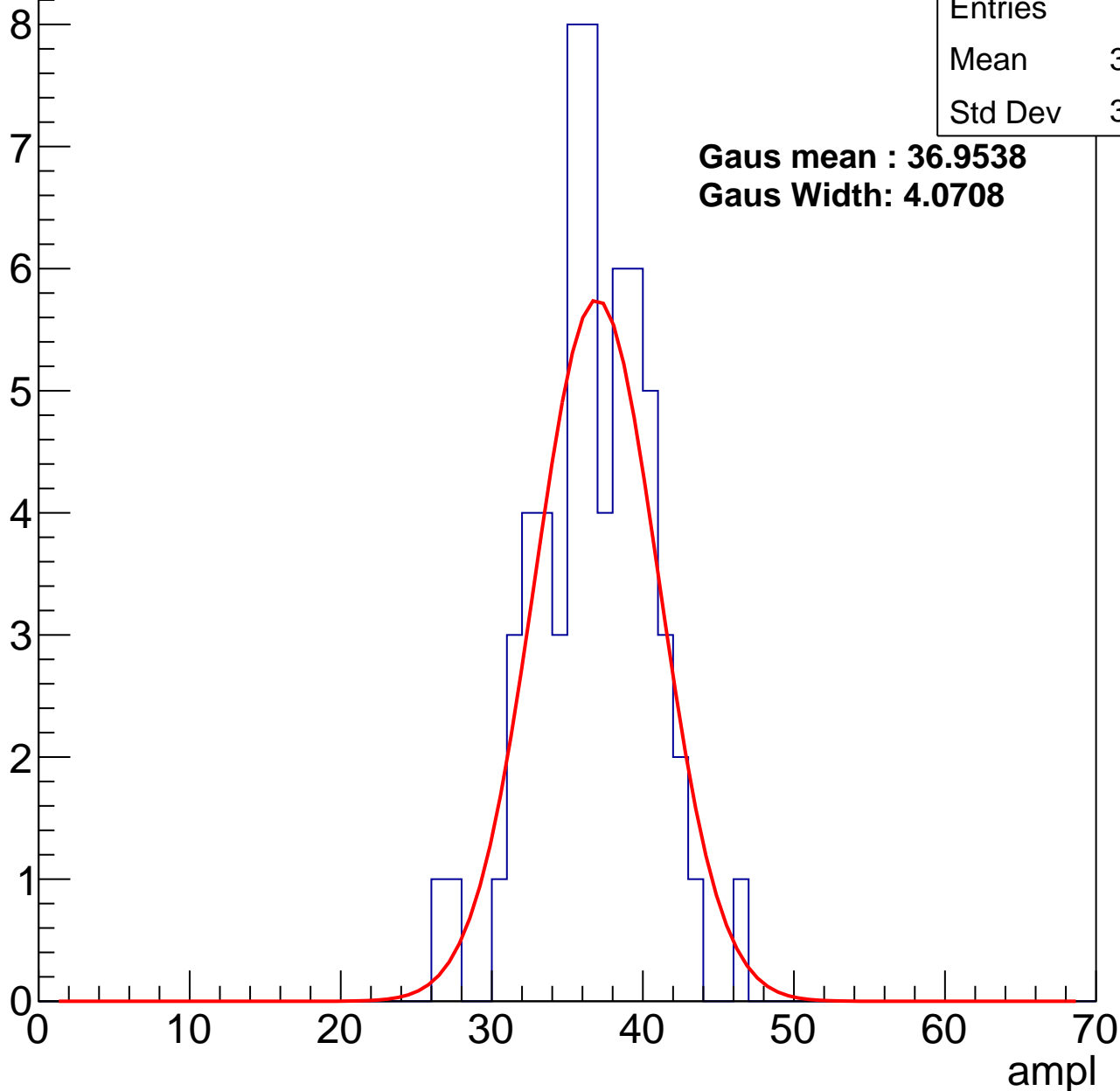
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	36.26
Std Dev	3.767

**Gaus mean : 36.9538**

**Gaus Width: 4.0708**



# B0L001S, U21-ch19, adc2

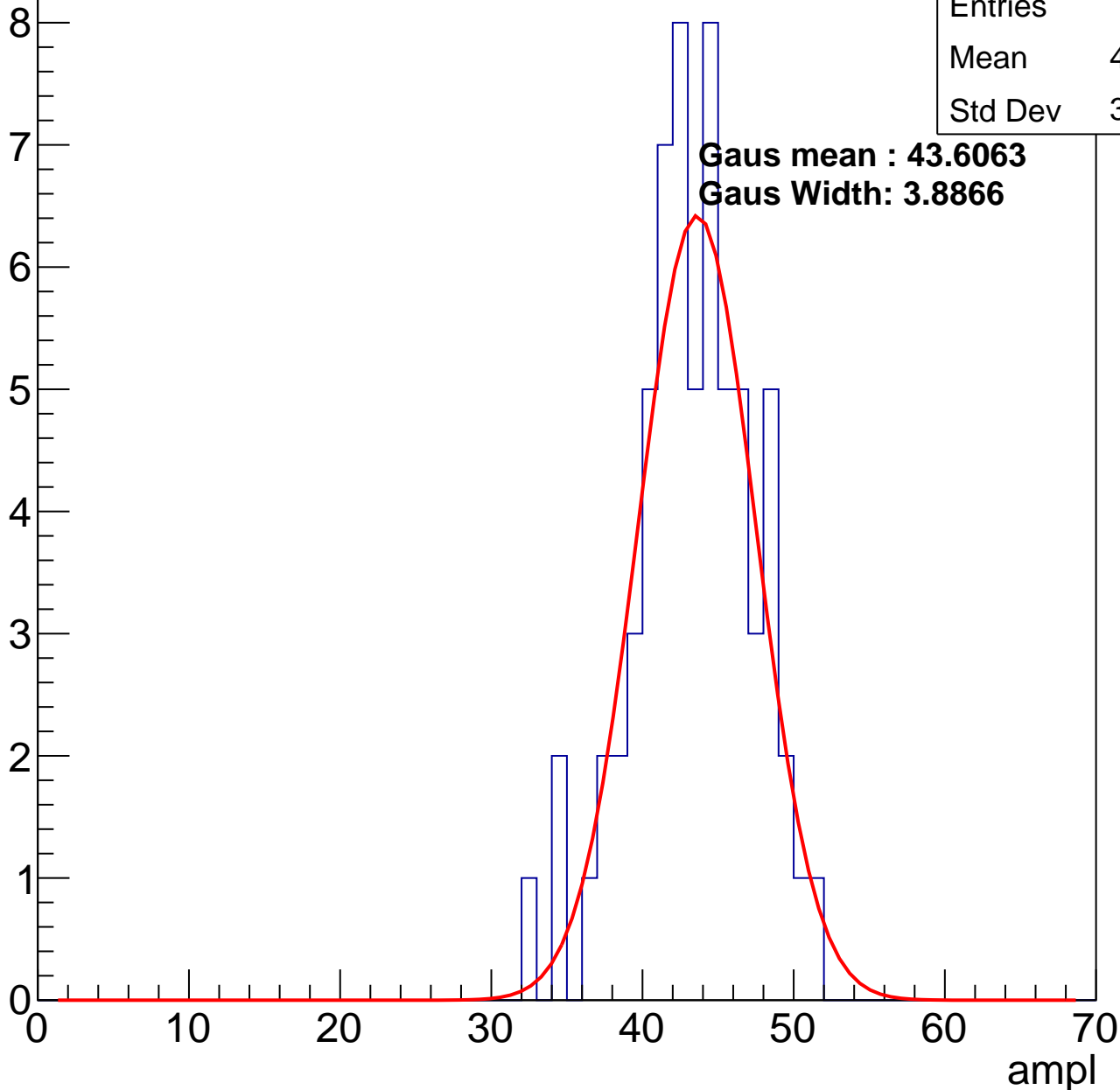
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	42.85
Std Dev	3.917

**Gaus mean : 43.6063**

**Gaus Width: 3.8866**

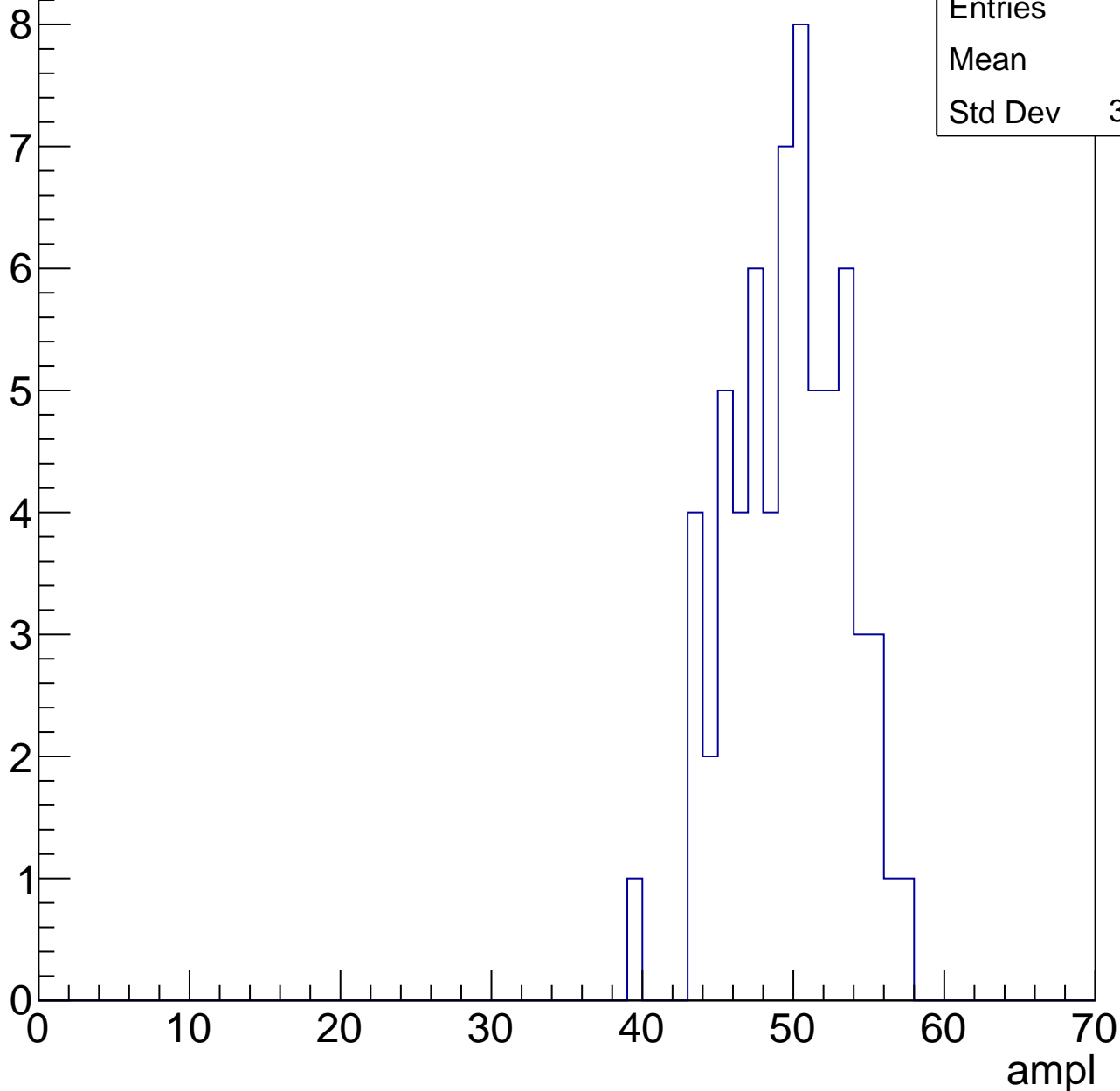


# B0L001S, U21-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	49.2
Std Dev	3.722

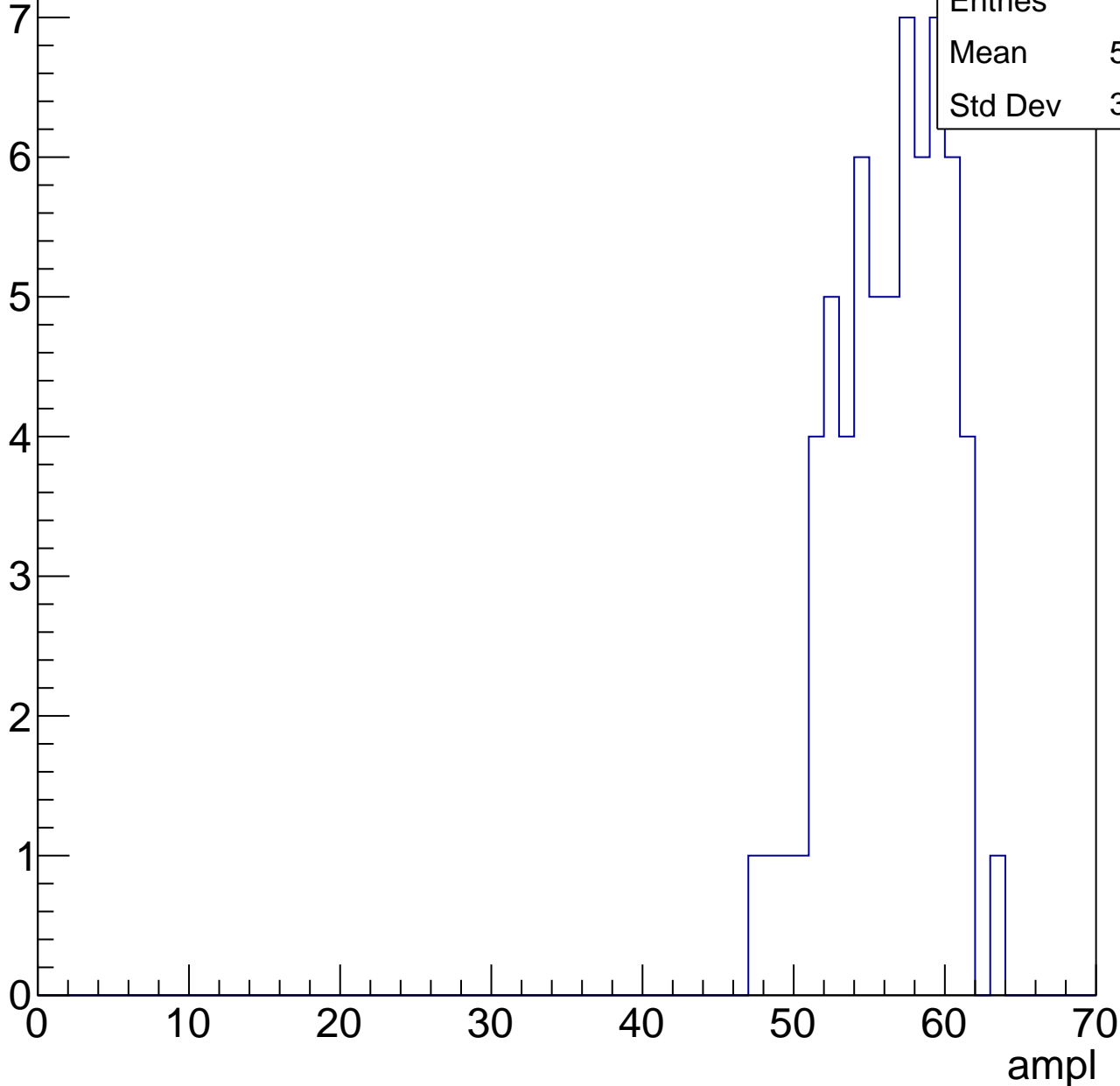


# B0L001S, U21-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	55.88
Std Dev	3.564

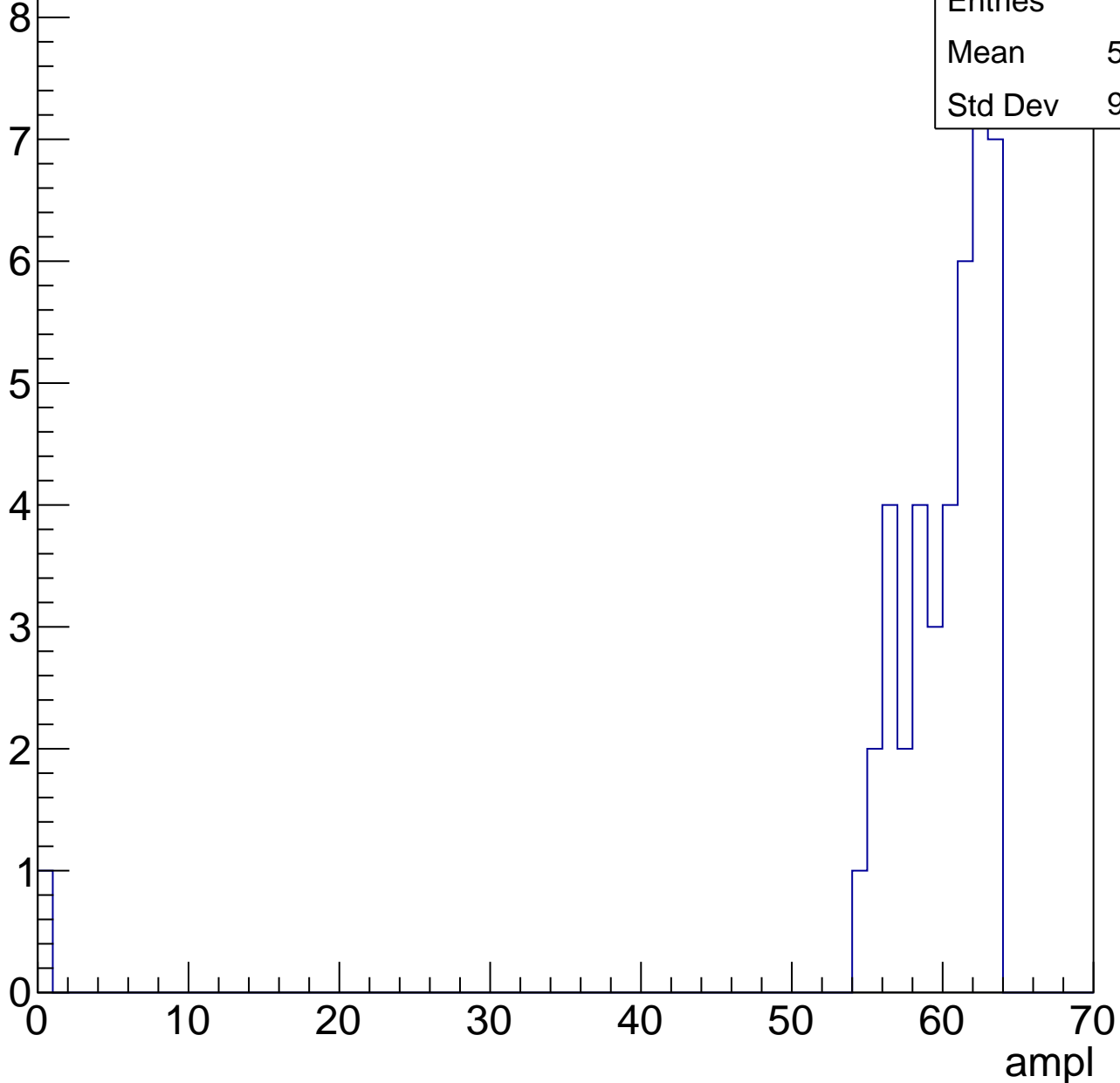


# B0L001S, U21-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	42
Mean	58.43
Std Dev	9.492



# B0L001S, U21-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U21-ch20, adc0

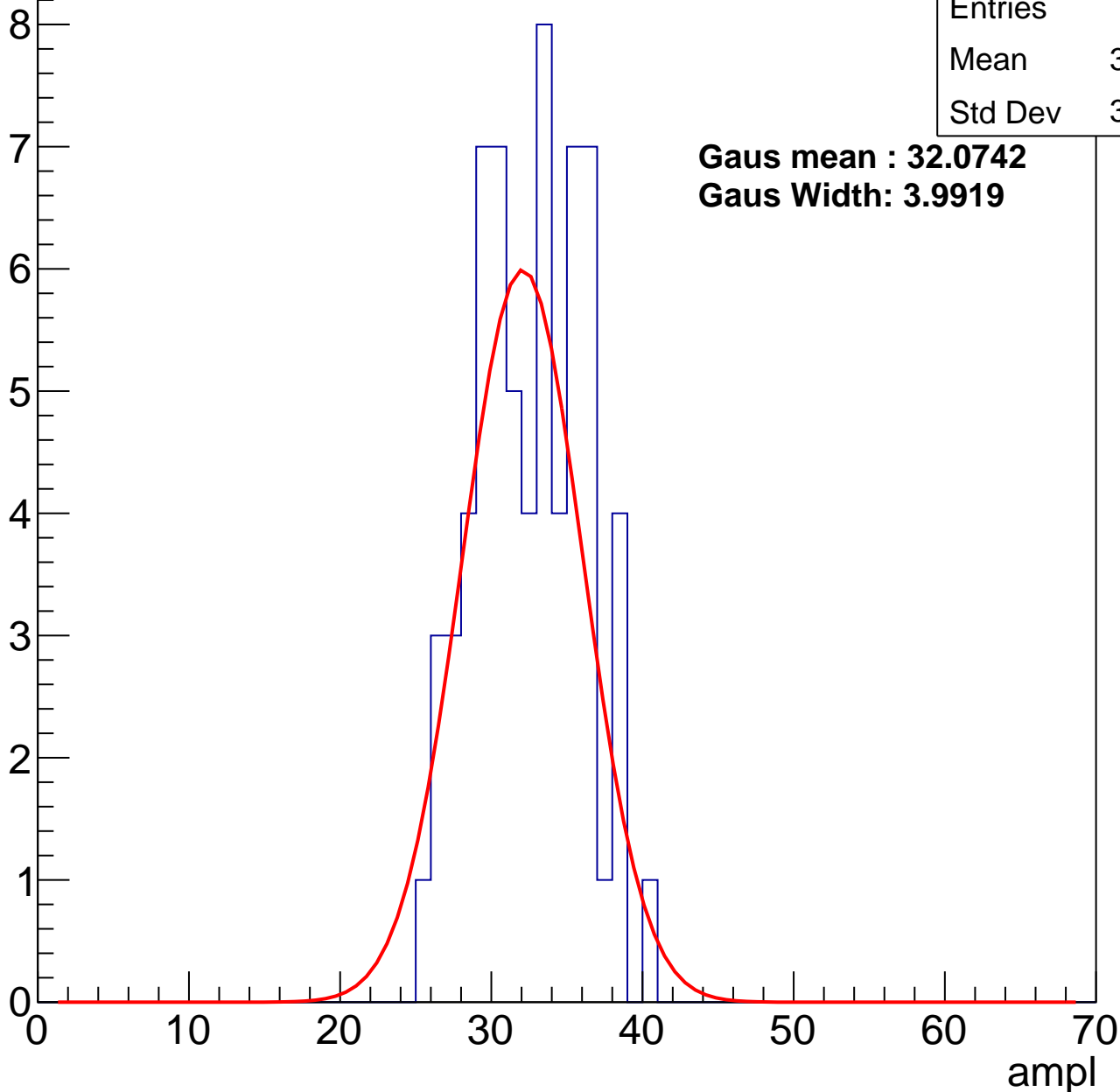
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	32.09
Std Dev	3.532

**Gaus mean : 32.0742**

**Gaus Width: 3.9919**



# B0L001S, U21-ch20, adc1

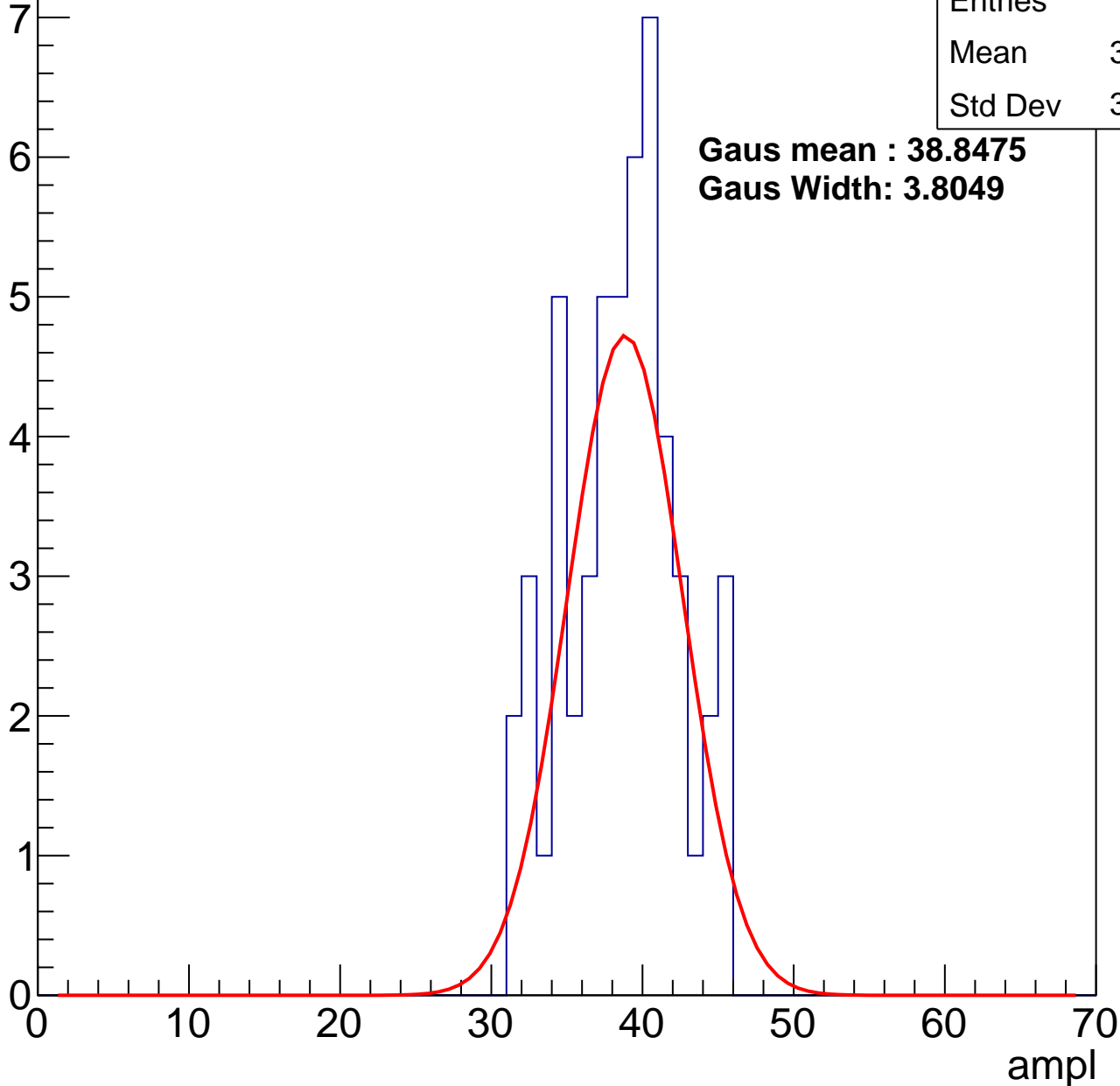
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	38.15
Std Dev	3.687

**Gaus mean : 38.8475**

**Gaus Width: 3.8049**



# B0L001S, U21-ch20, adc2

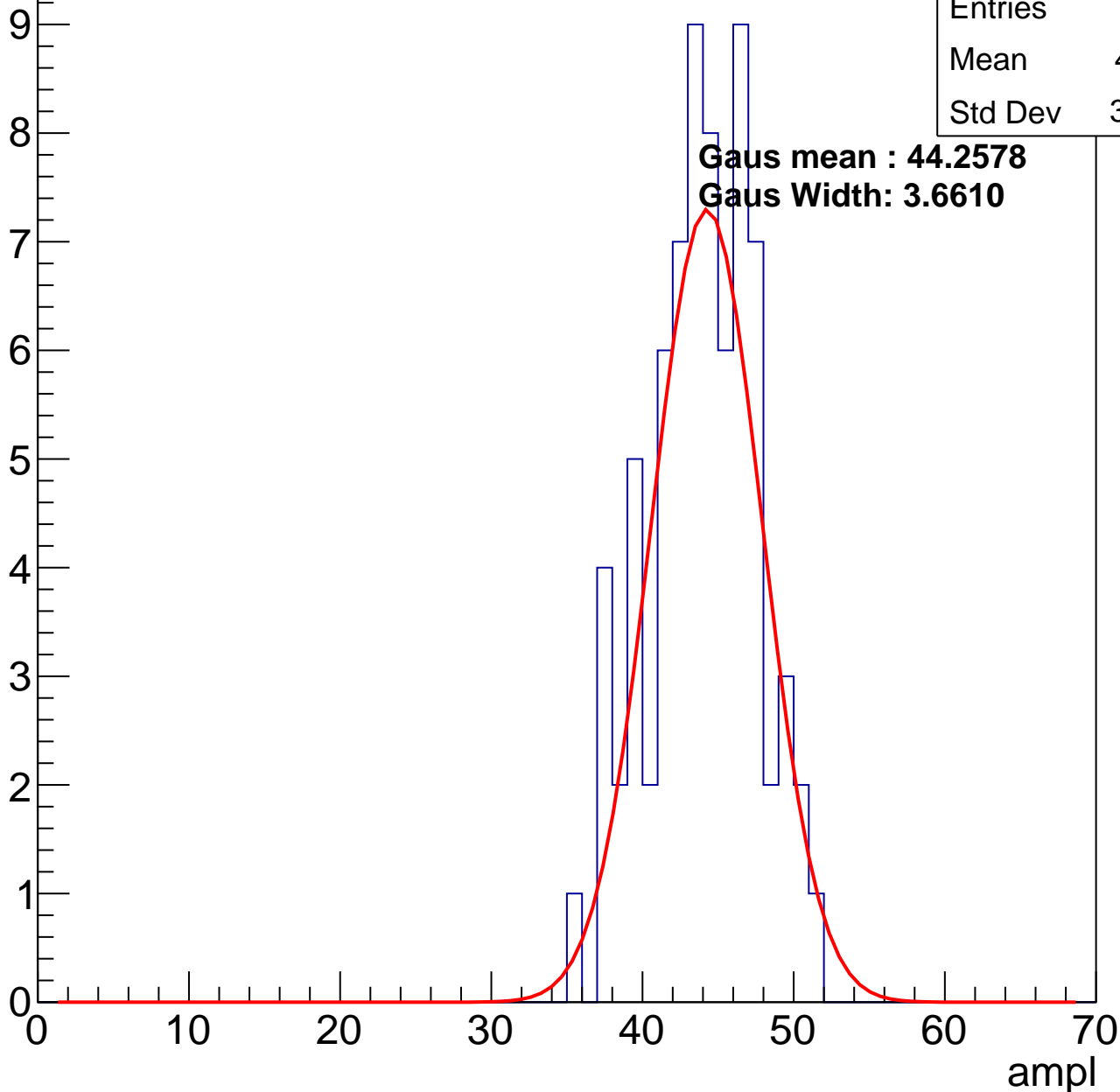
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	43.51
Std Dev	3.512

**Gaus mean : 44.2578**

**Gaus Width: 3.6610**

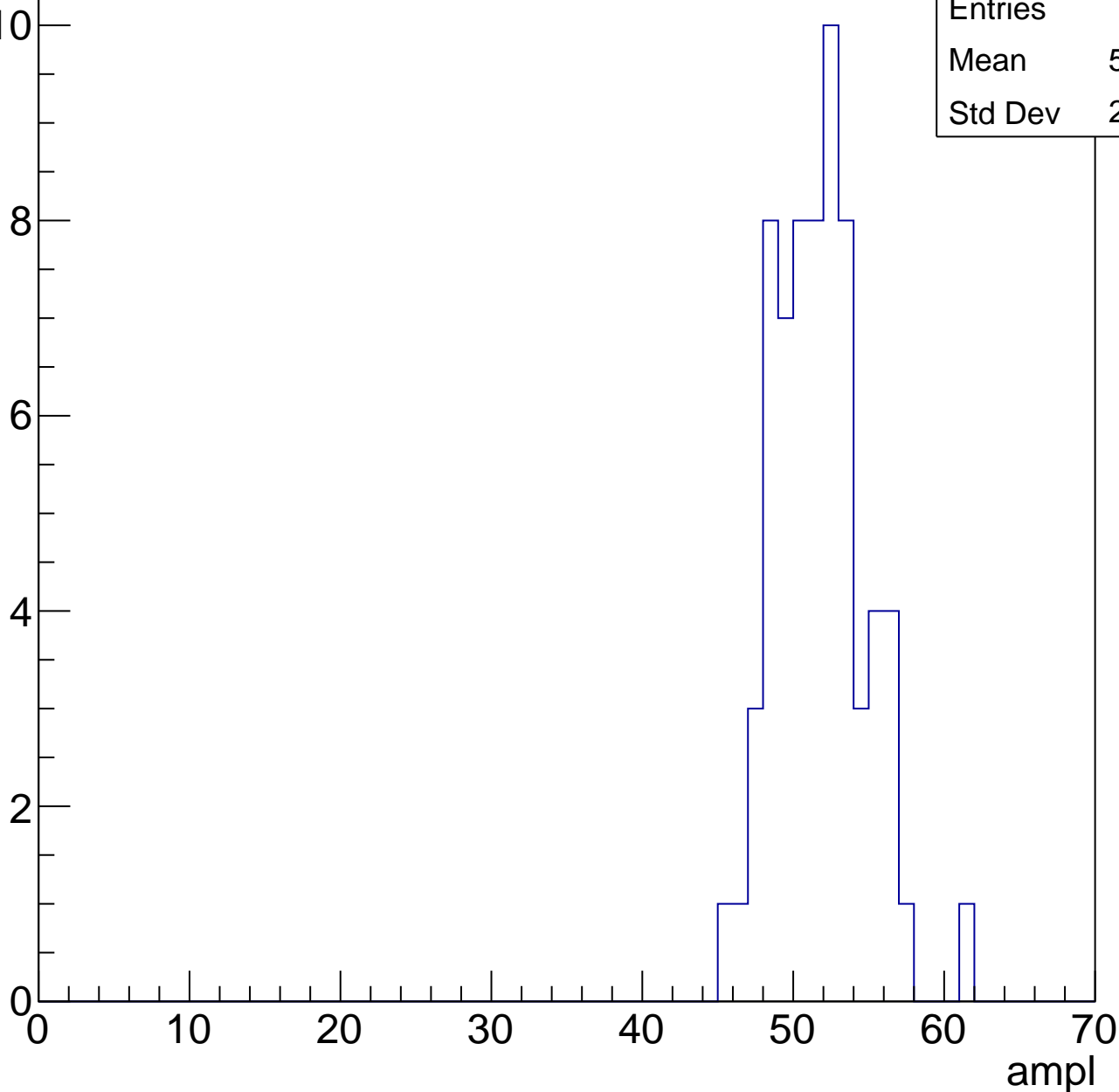


# B0L001S, U21-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	51.27
Std Dev	2.945

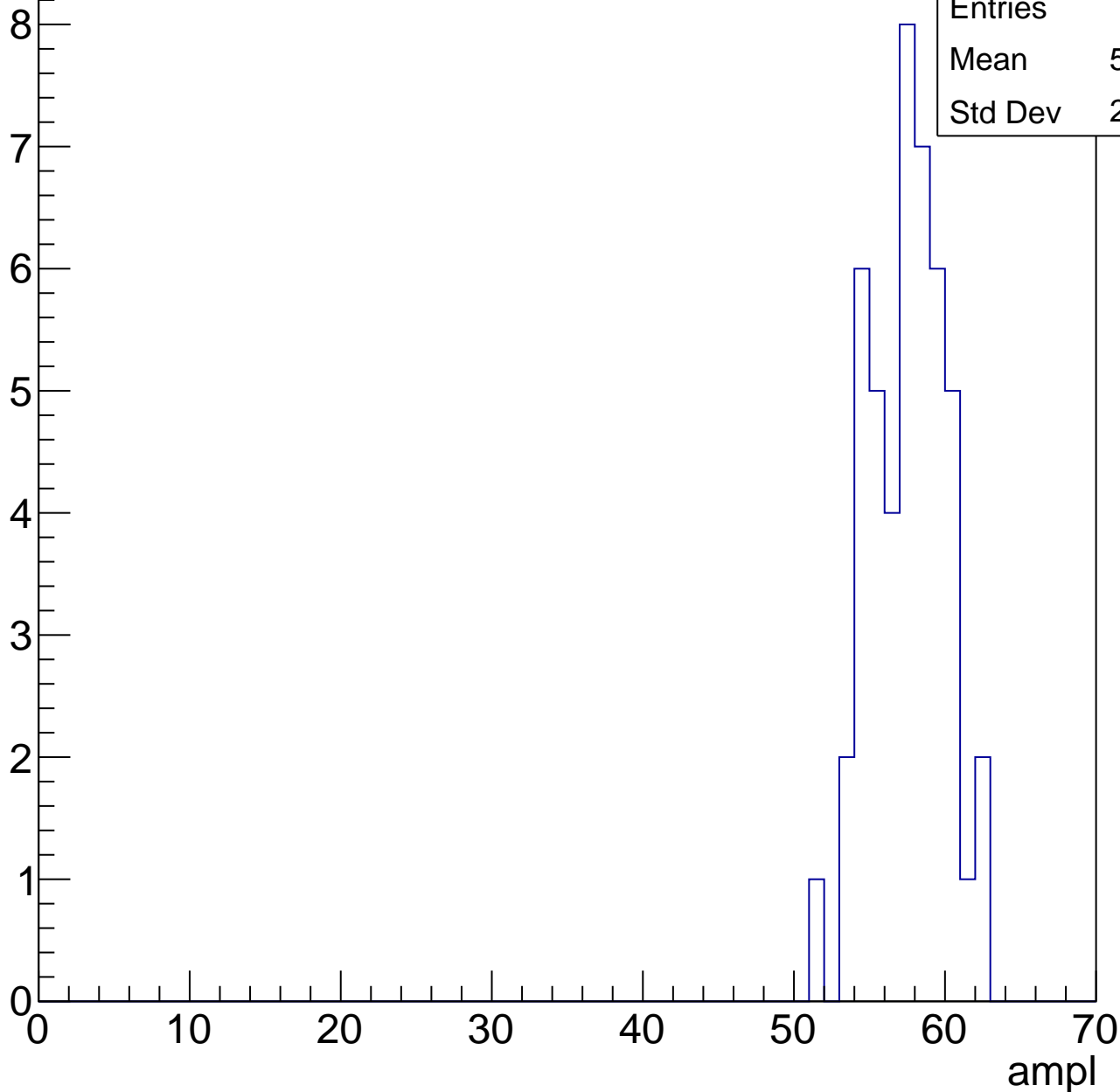


# B0L001S, U21-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	57.04
Std Dev	2.475

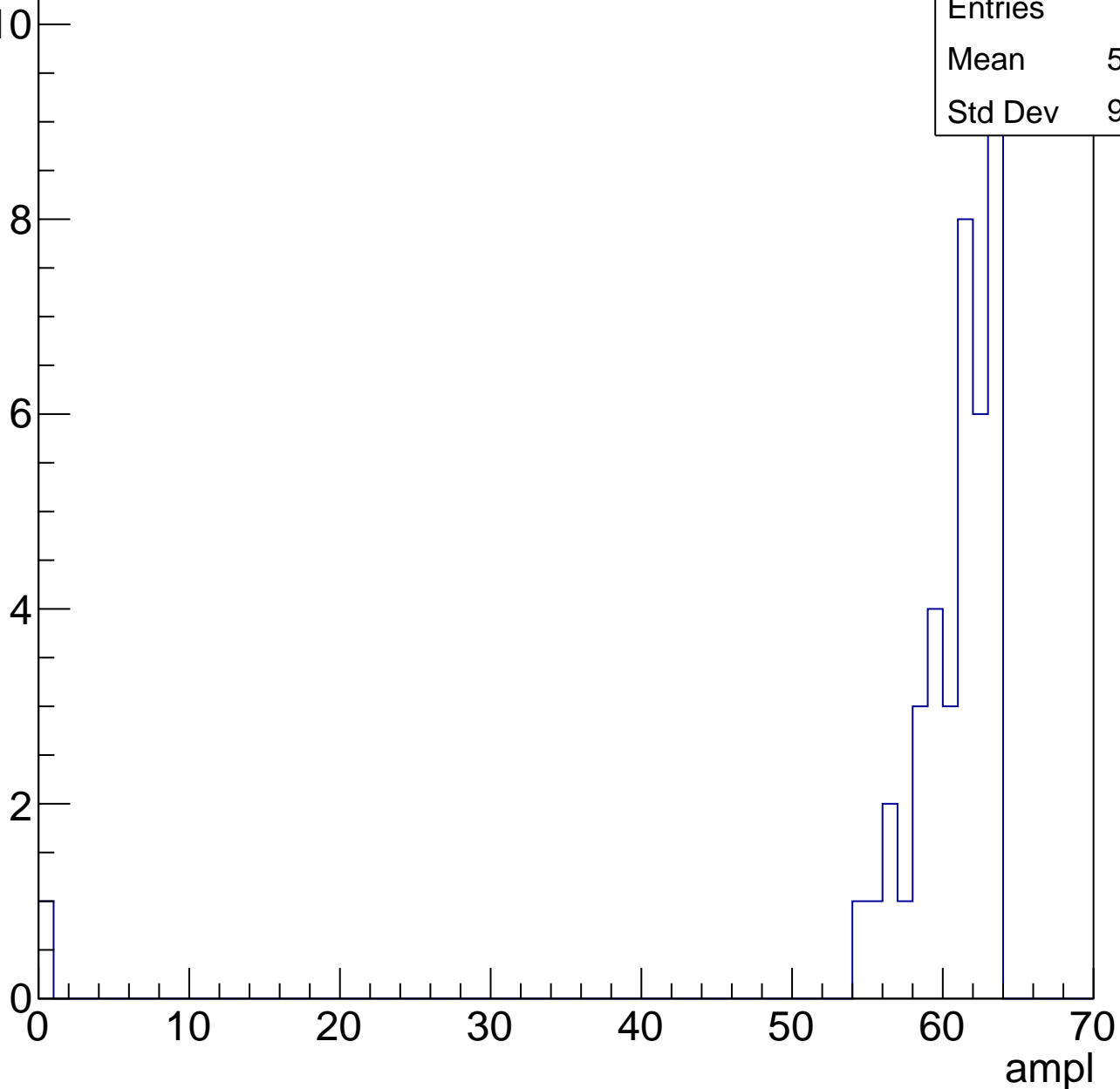


# B0L001S, U21-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	40
Mean	58.95
Std Dev	9.742



# B0L001S, U21-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	61
Std Dev	1

ampl



# B0L001S, U21-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



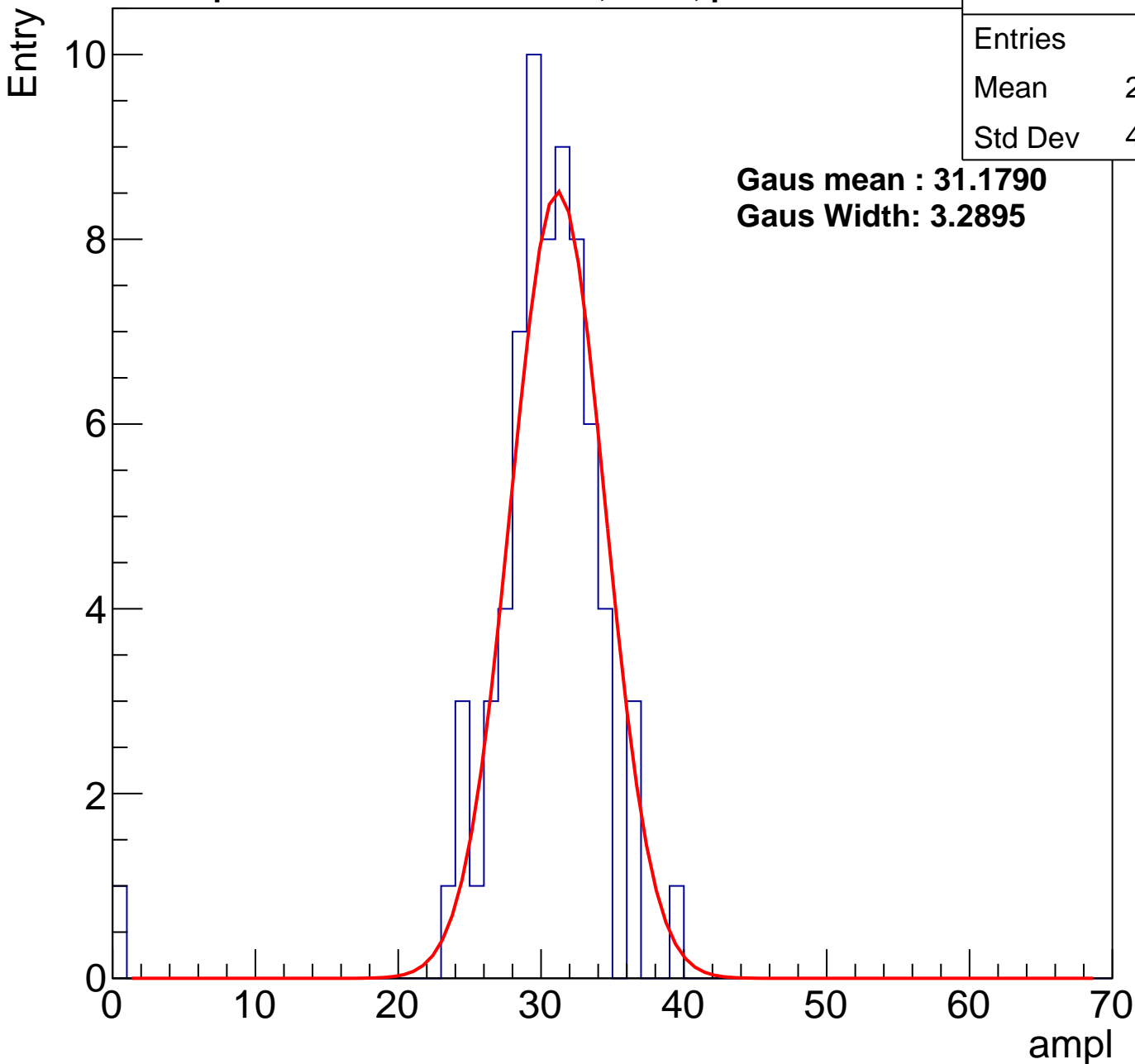
Entries	0
Mean	0
Std Dev	0

# B0L001S, U21-ch21, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	69
Mean	29.68
Std Dev	4.732

**Gaus mean : 31.1790**  
**Gaus Width: 3.2895**



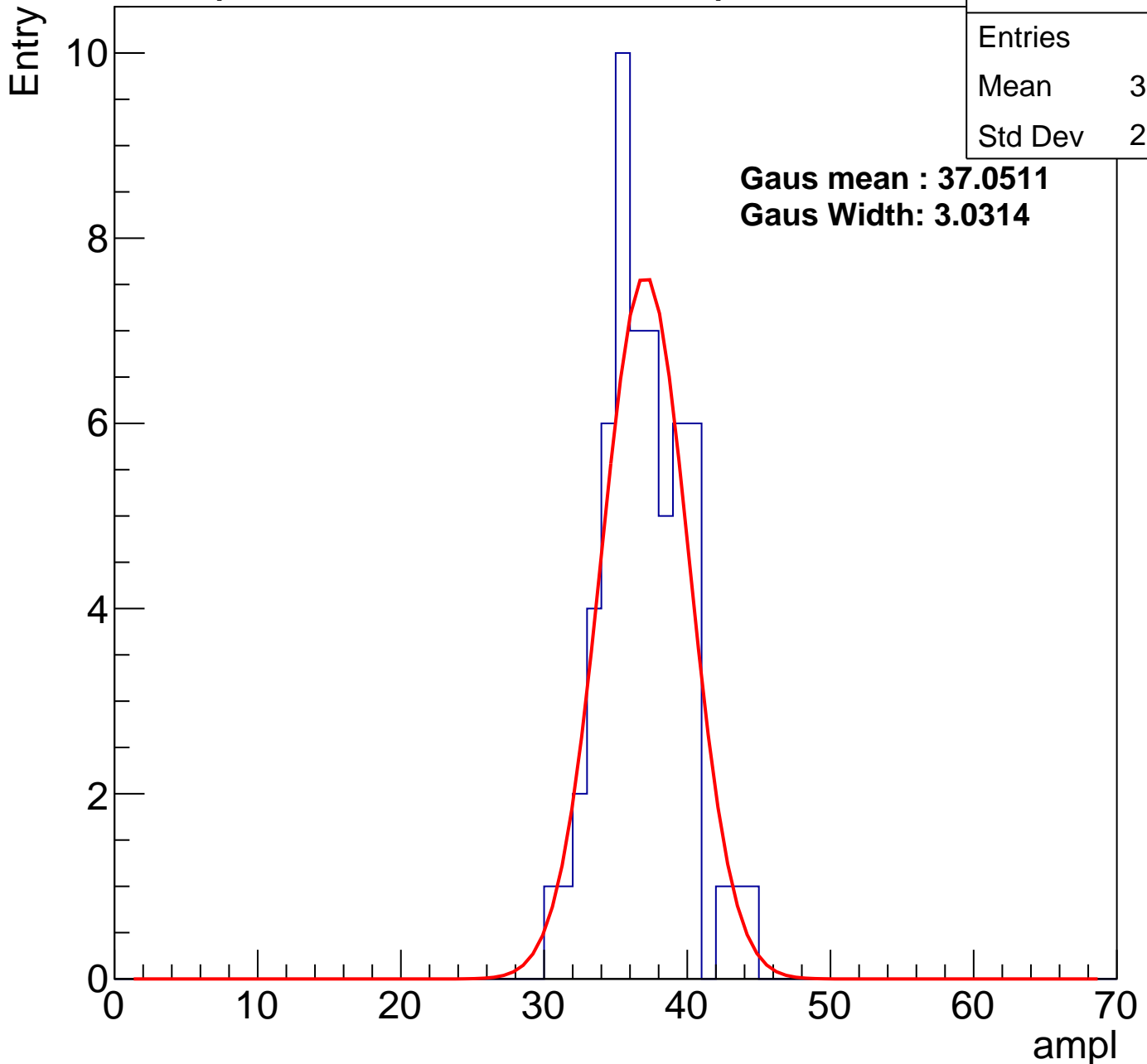
# B0L001S, U21-ch21, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	58
Mean	36.47
Std Dev	2.866

**Gaus mean : 37.0511**

**Gaus Width: 3.0314**



# B0L001S, U21-ch21, adc2

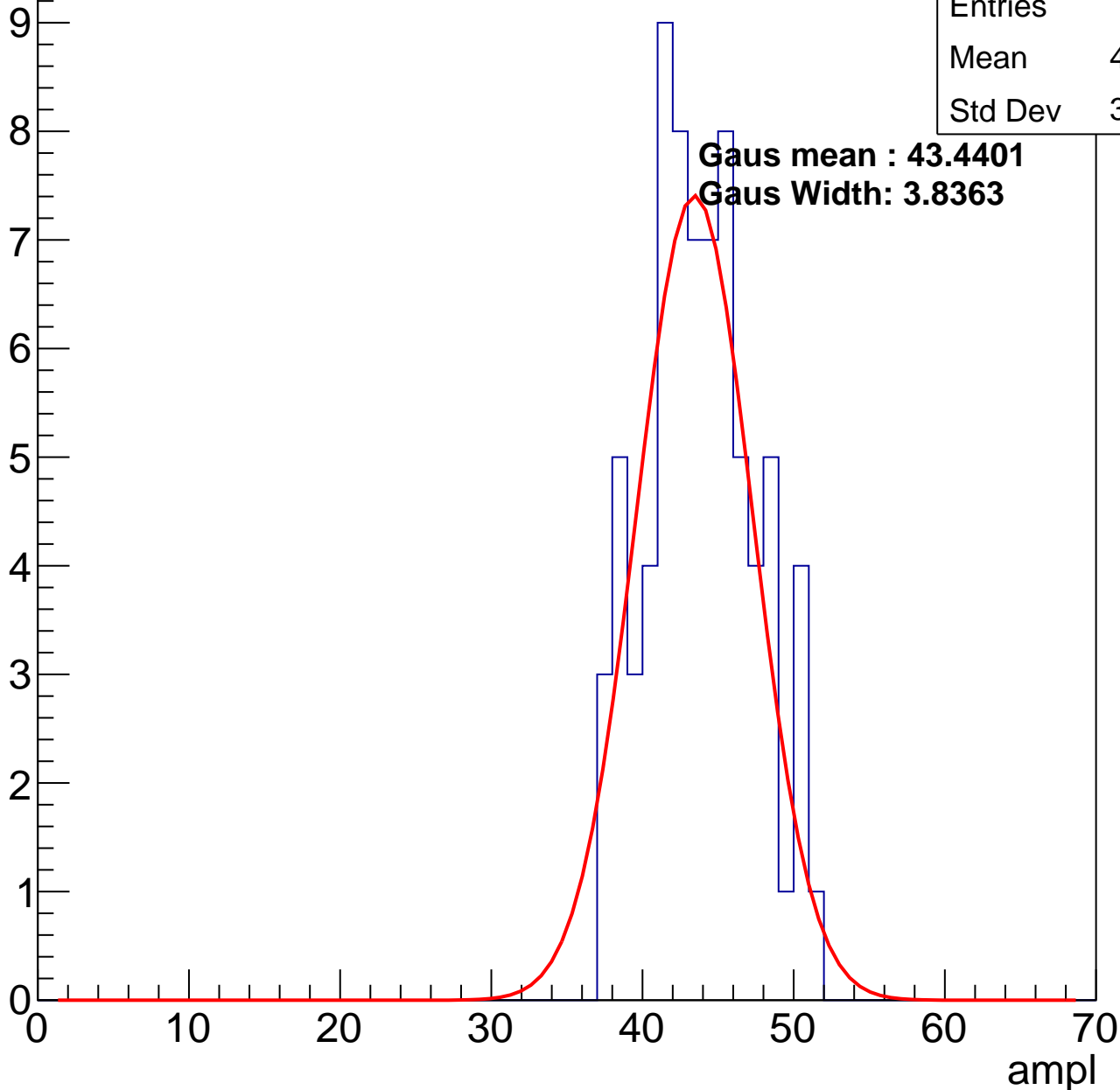
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	43.38
Std Dev	3.525

**Gaus mean : 43.4401**

**Gaus Width: 3.8363**

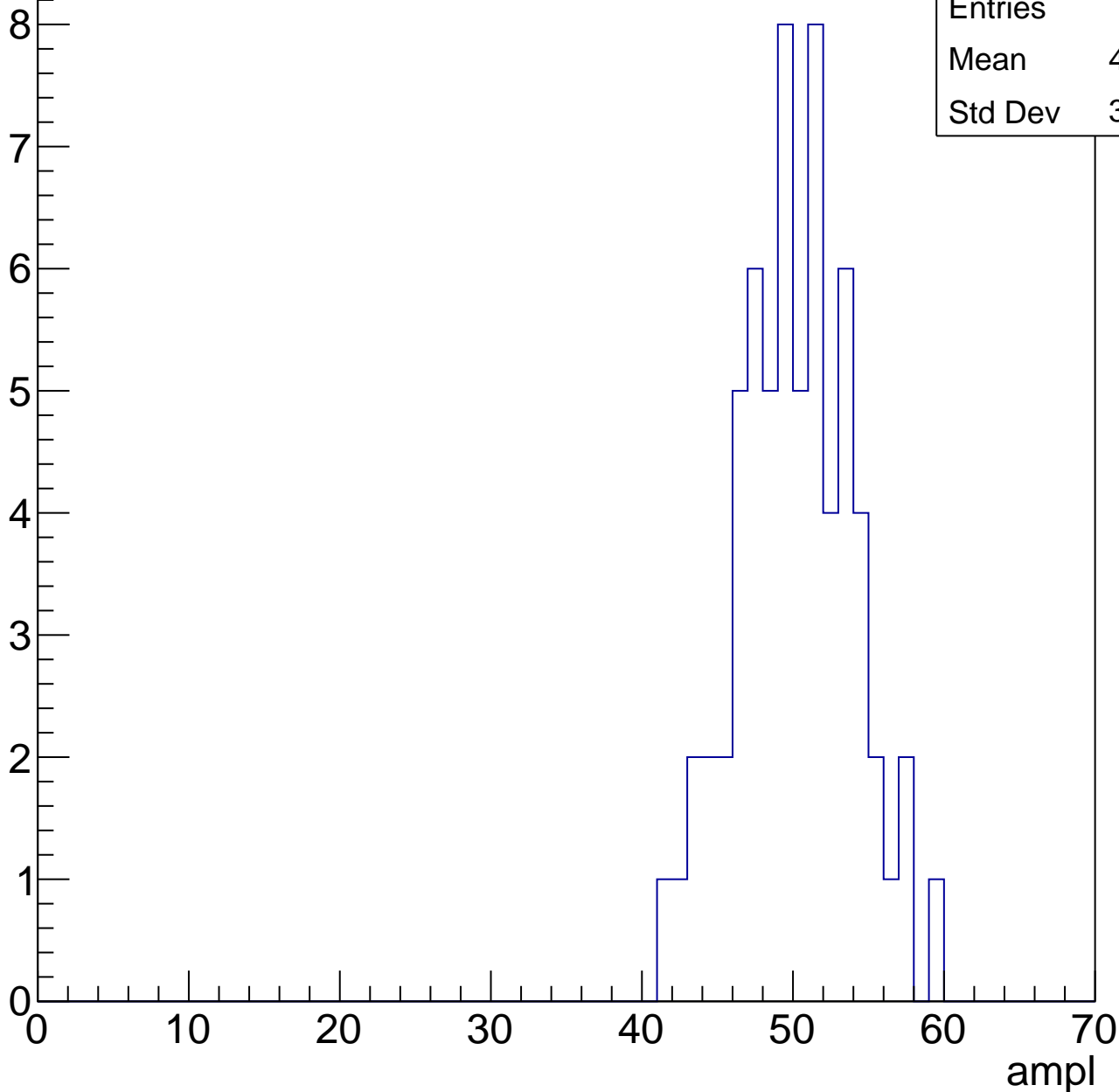


# B0L001S, U21-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	49.69
Std Dev	3.778

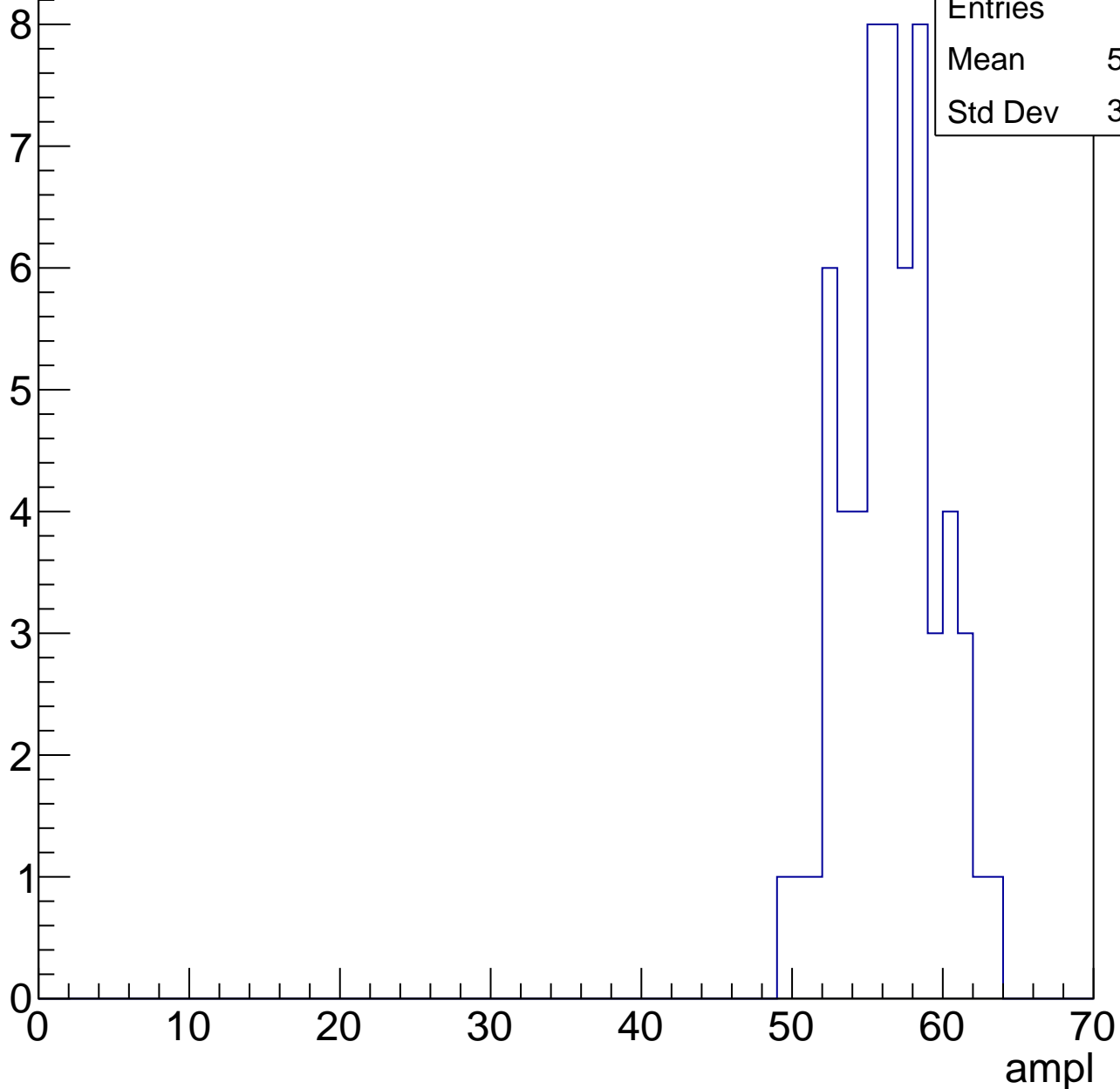


# B0L001S, U21-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	56.08
Std Dev	3.066

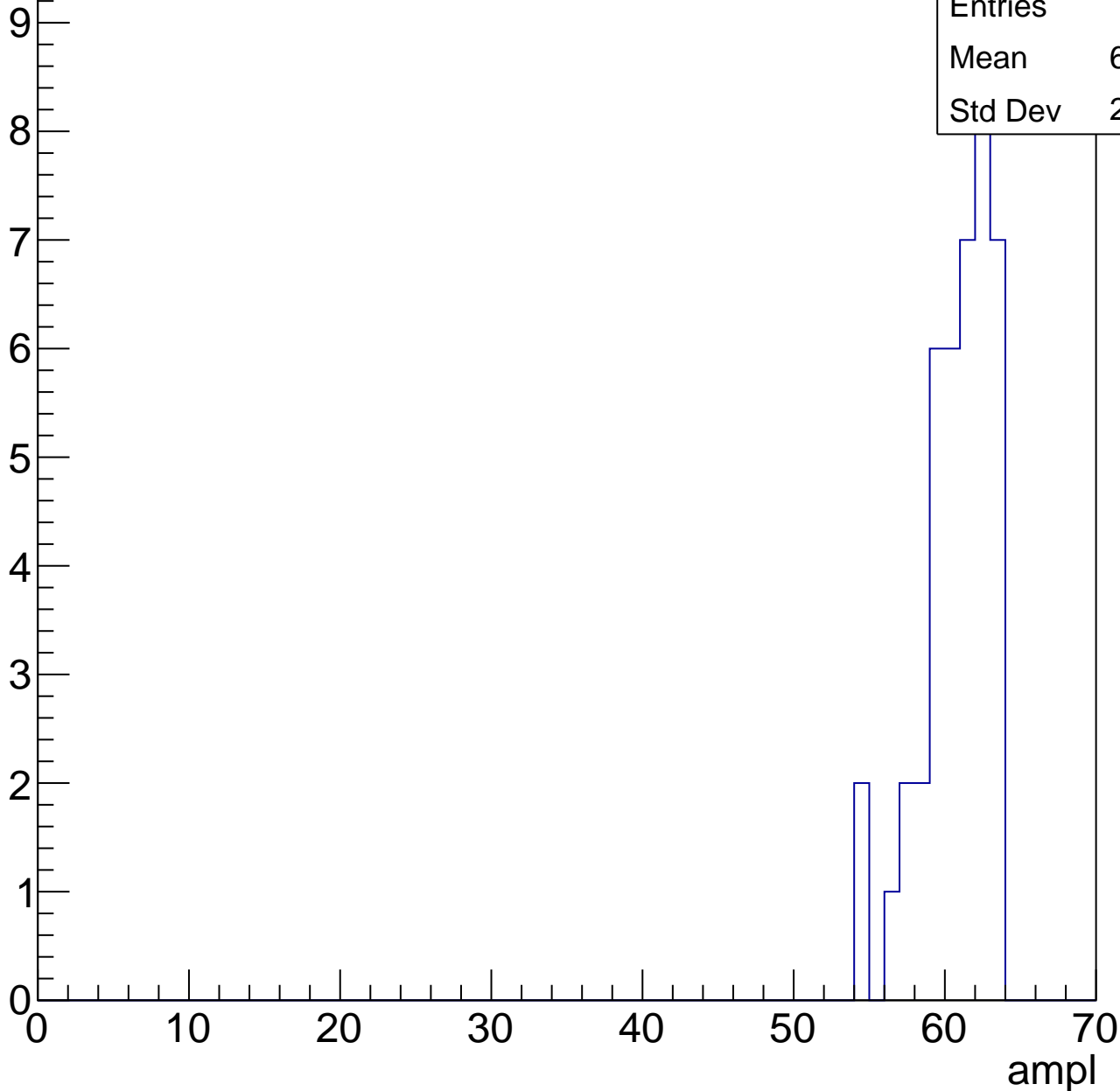


# B0L001S, U21-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	42
Mean	60.33
Std Dev	2.296



# B0L001S, U21-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	22
Std Dev	0

# B0L001S, U21-ch22, adc0

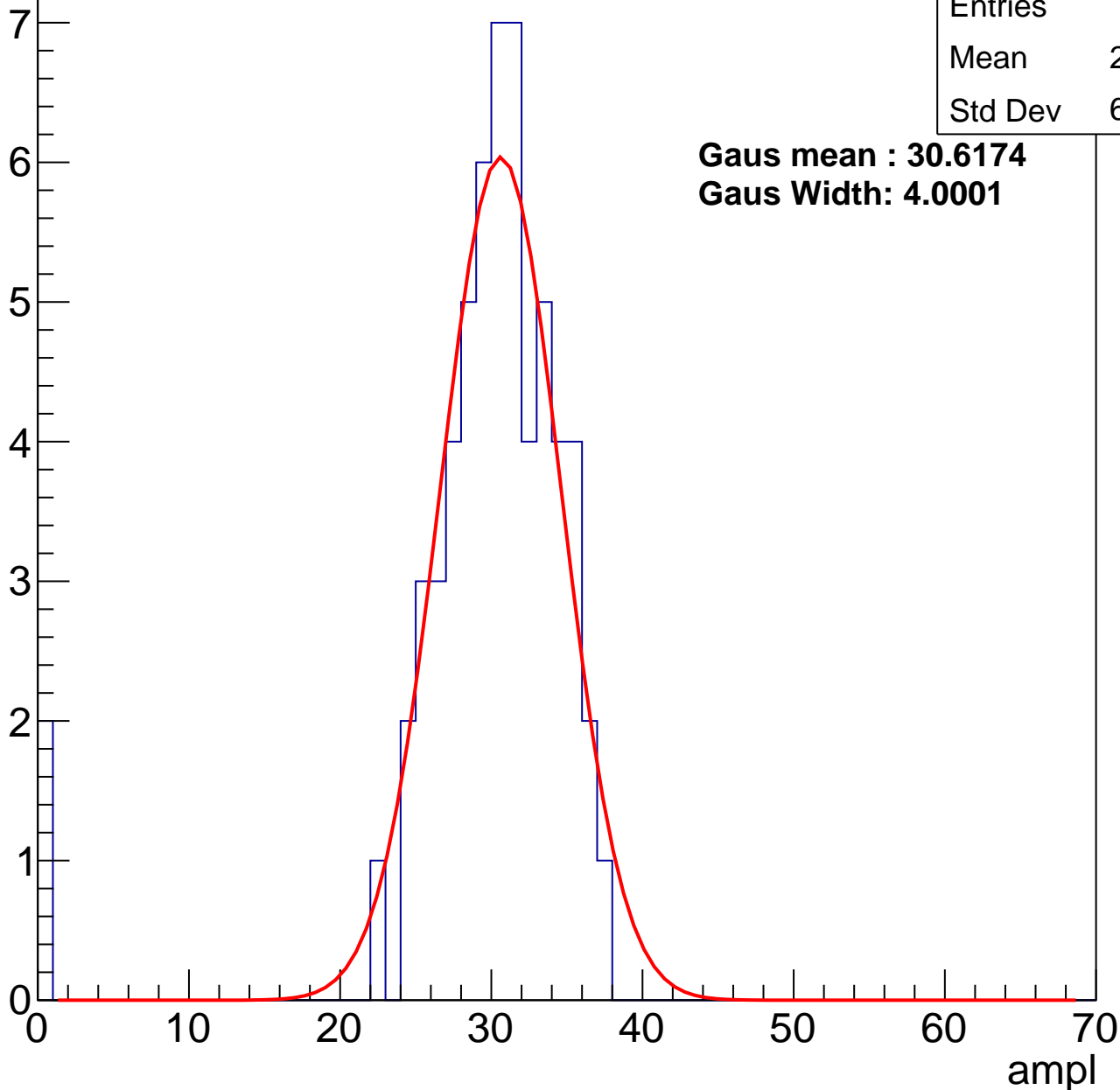
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	29.17
Std Dev	6.367

**Gaus mean : 30.6174**

**Gaus Width: 4.0001**



# B0L001S, U21-ch22, adc1

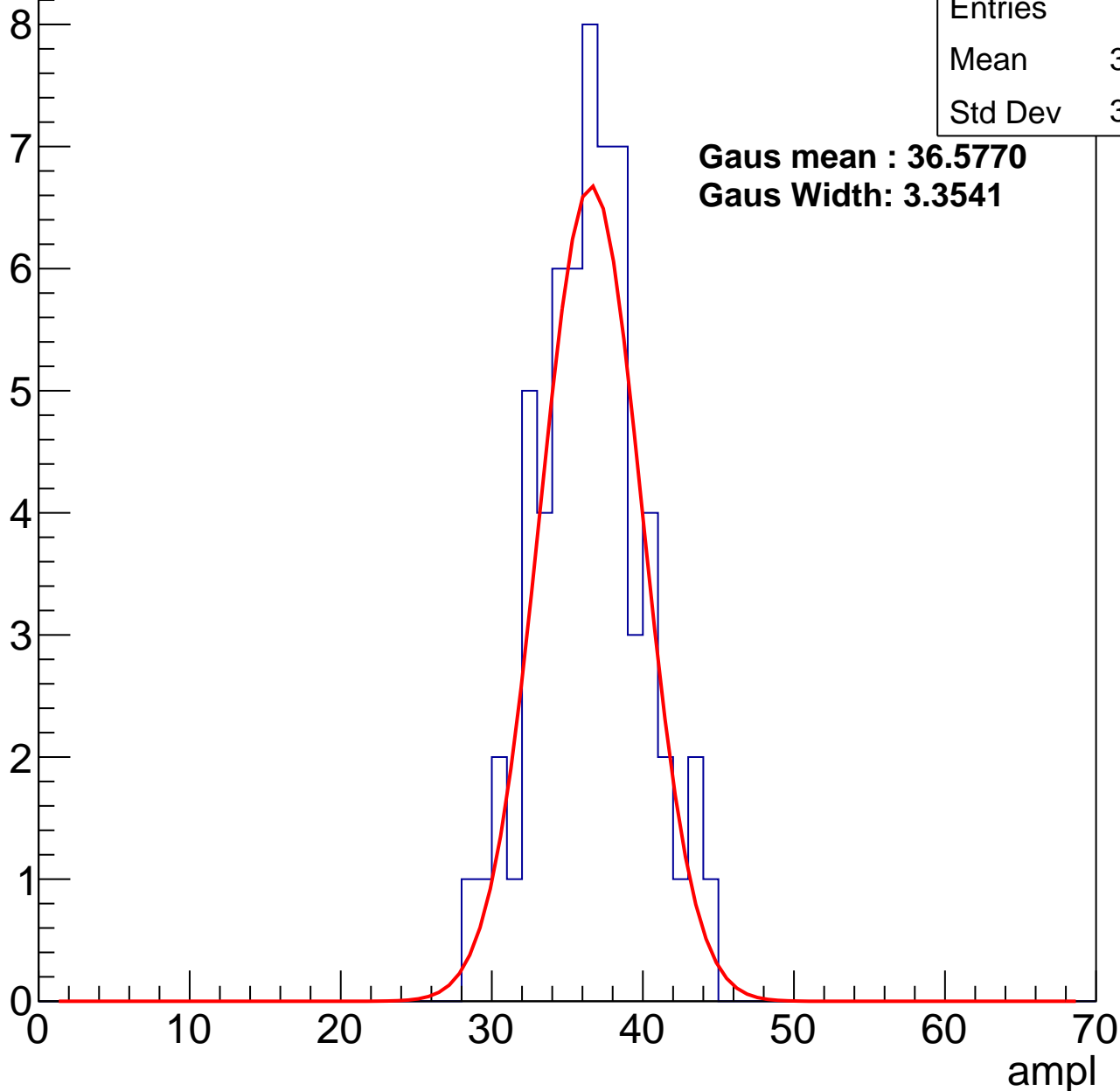
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	36.03
Std Dev	3.459

**Gaus mean : 36.5770**

**Gaus Width: 3.3541**



# B0L001S, U21-ch22, adc2

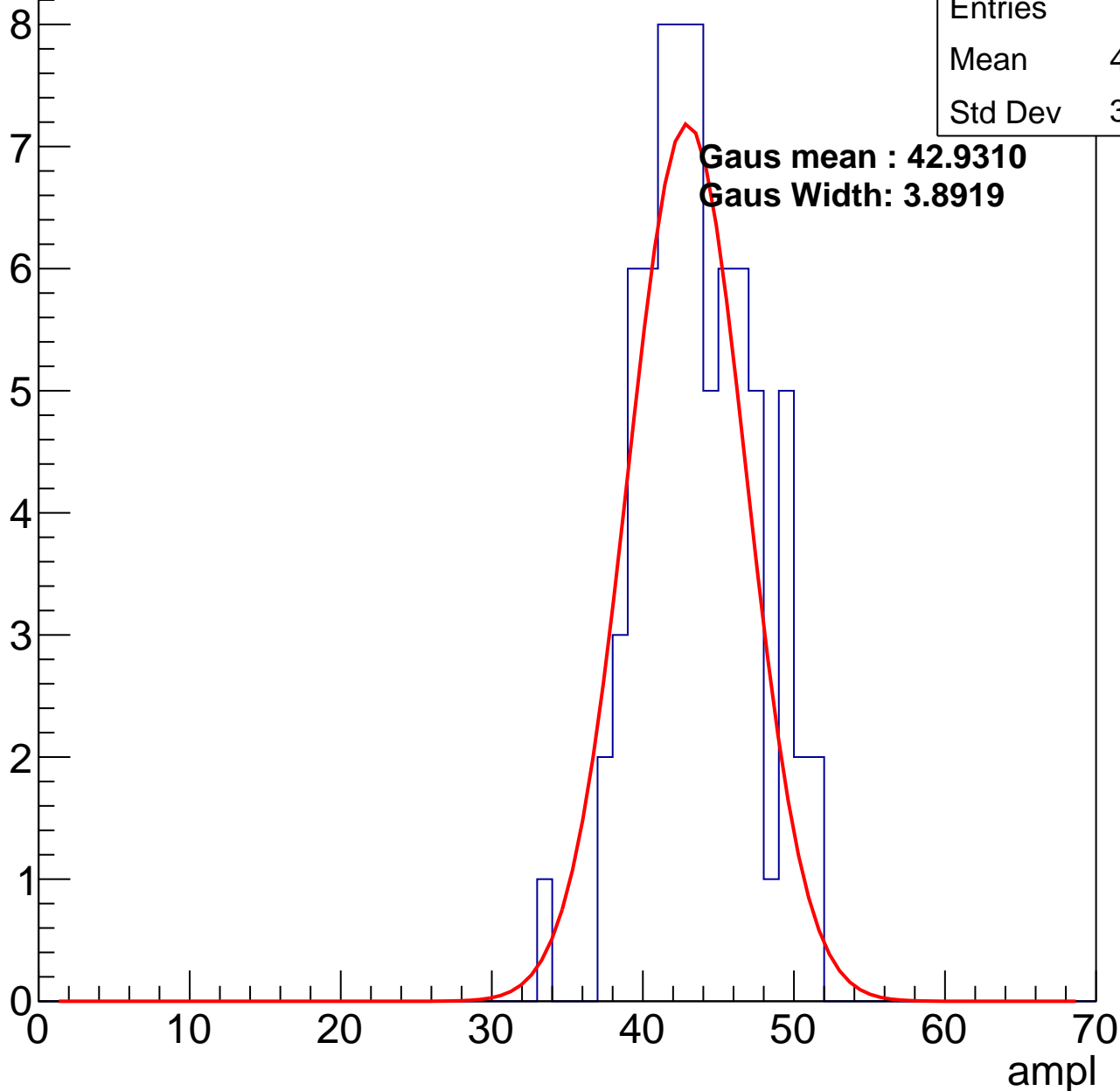
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	43.23
Std Dev	3.726

**Gaus mean : 42.9310**

**Gaus Width: 3.8919**

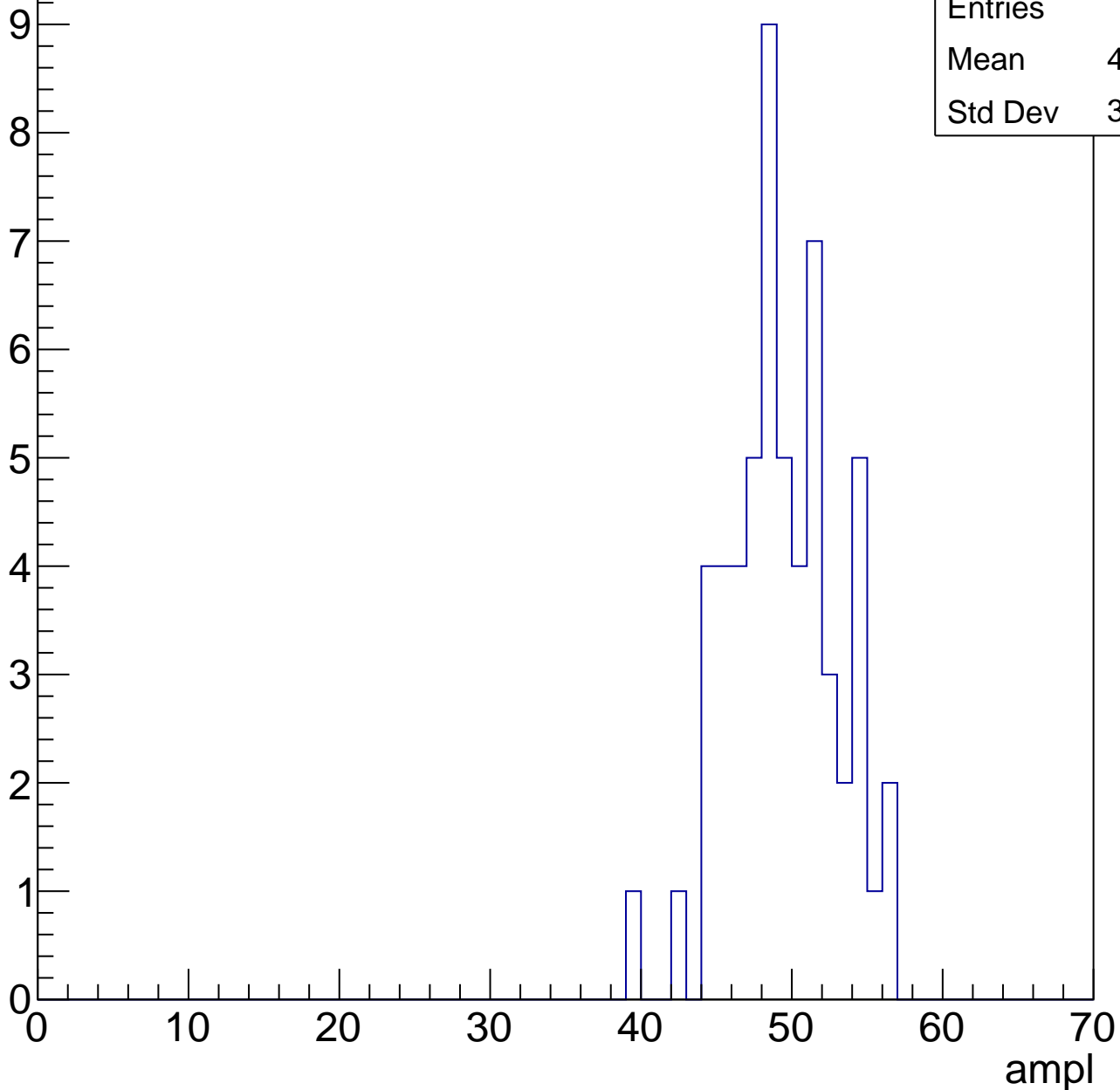


# B0L001S, U21-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	48.93
Std Dev	3.573

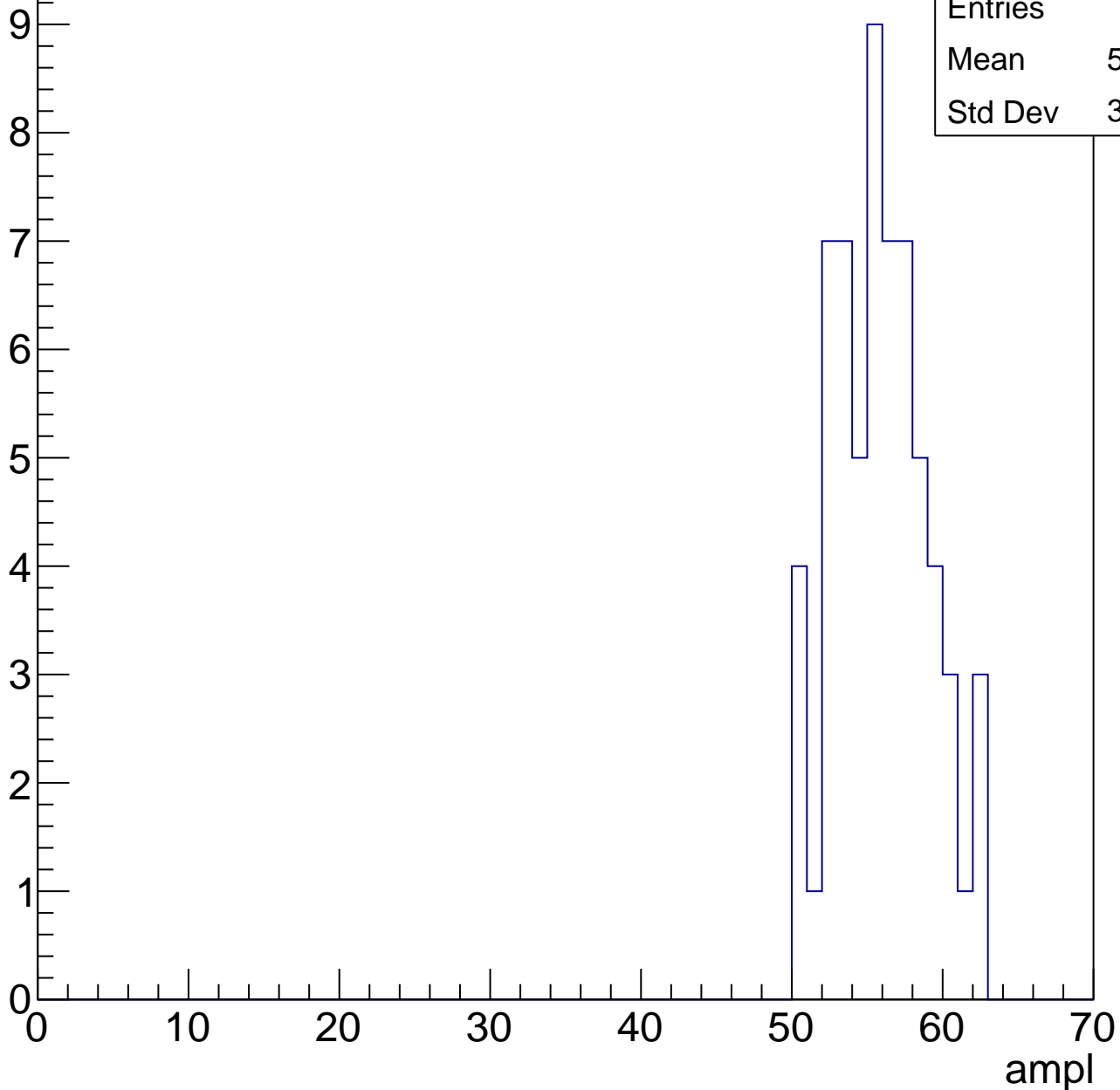


# B0L001S, U21-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	55.48
Std Dev	3.085

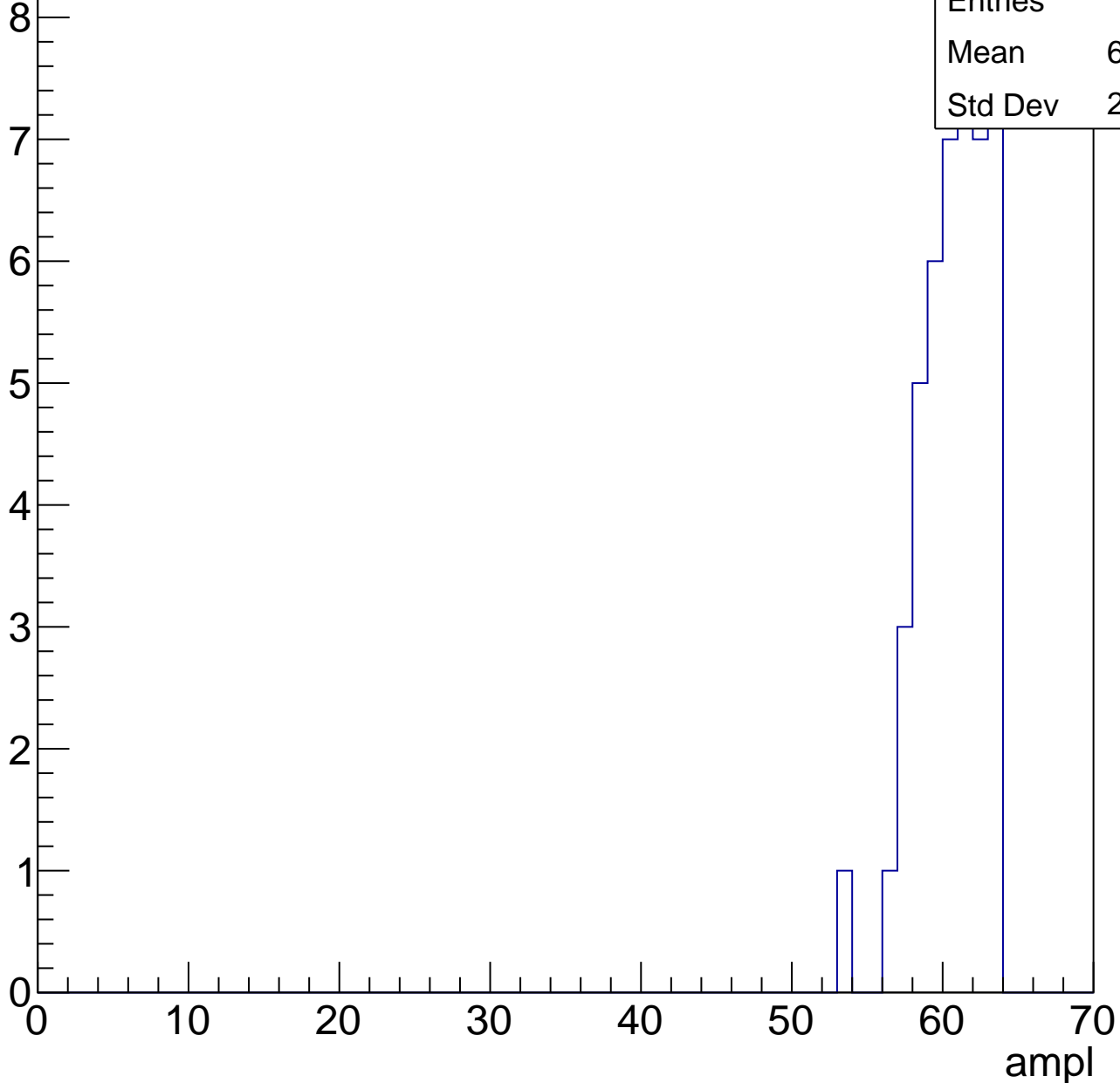


# B0L001S, U21-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

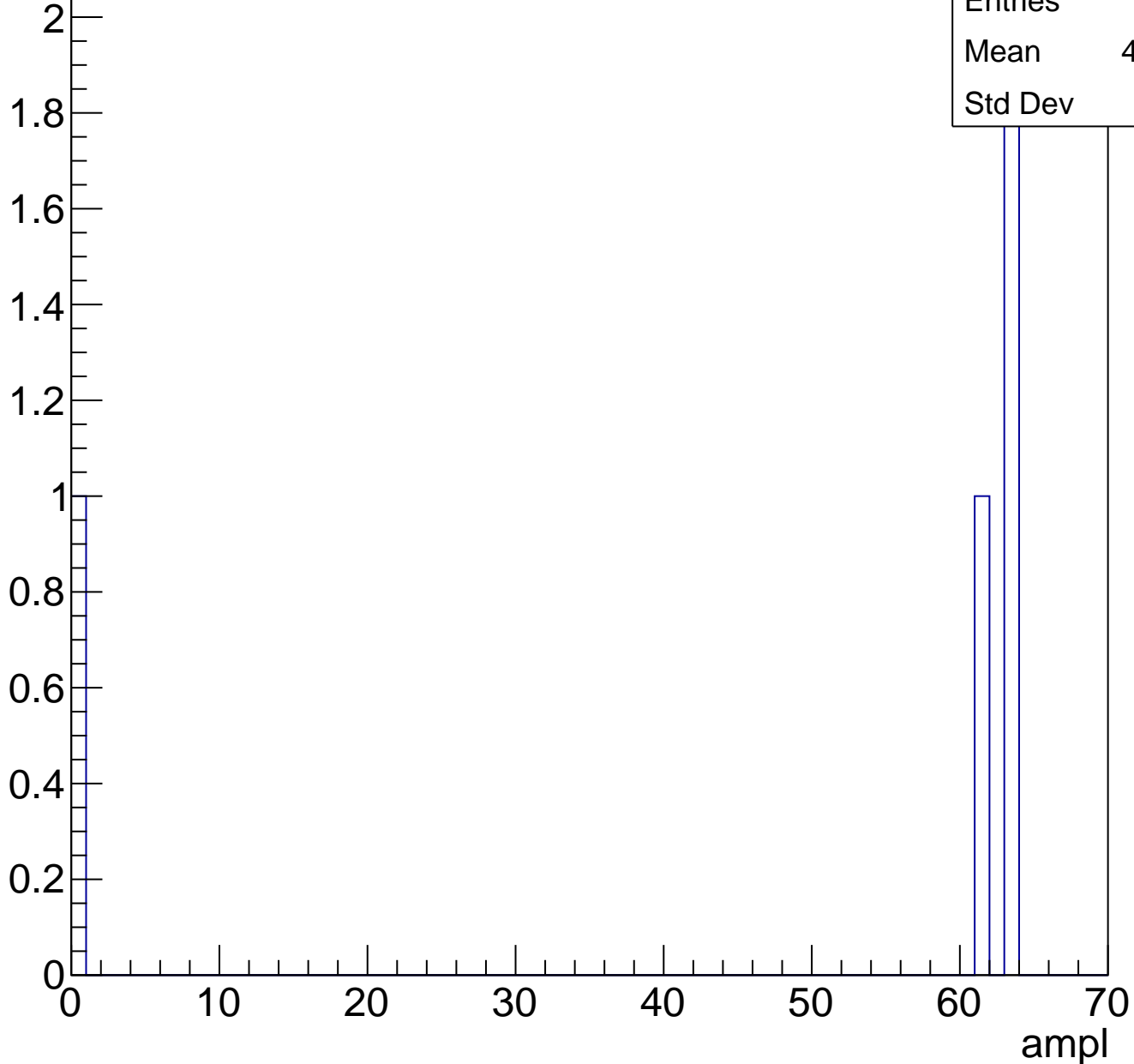
Entries	46
Mean	60.22
Std Dev	2.206



# B0L001S, U21-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

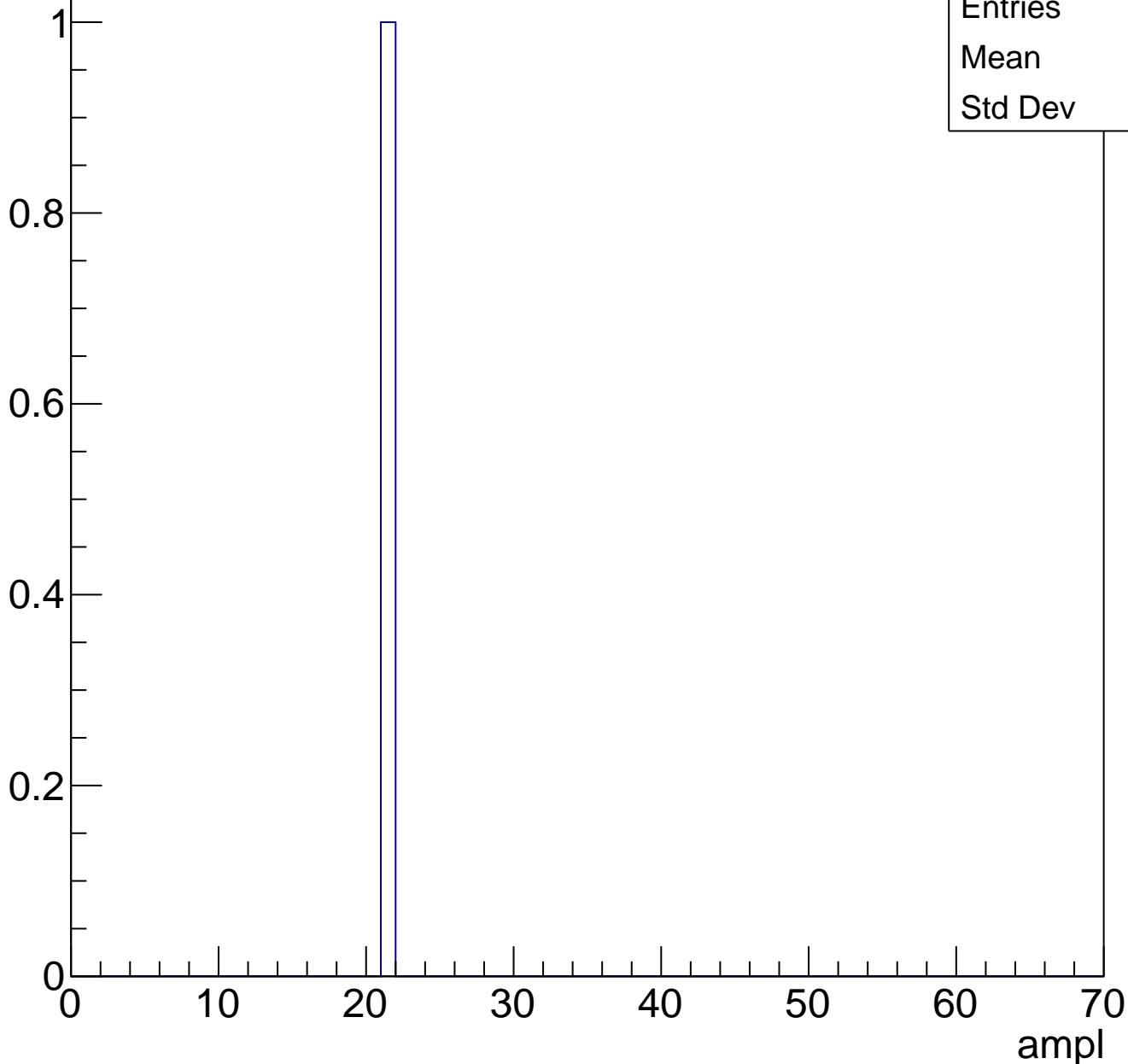




# B0L001S, U21-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch23, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	64
Mean	31.34
Std Dev	4.976

**Gaus mean : 32.1881**

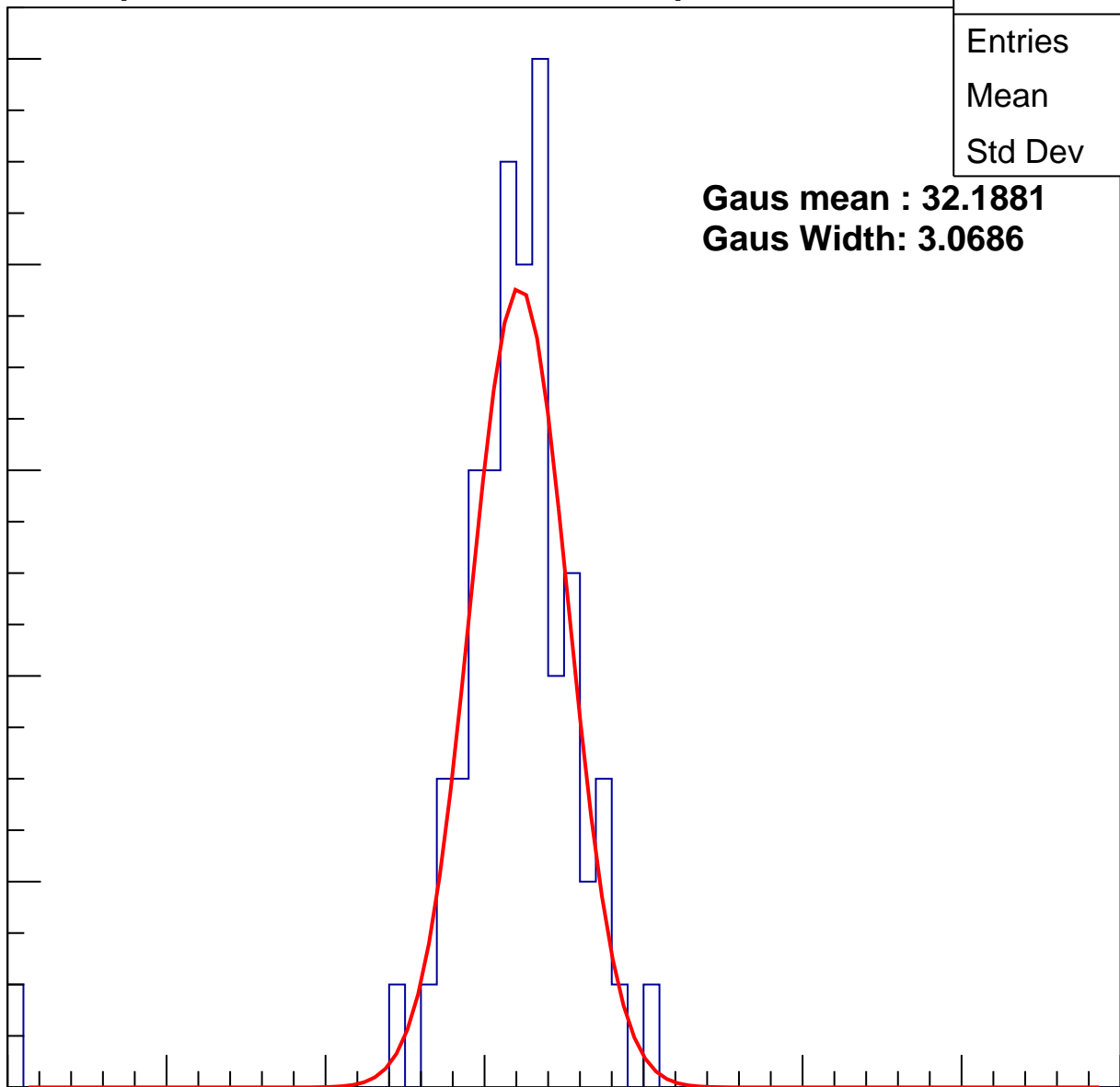
**Gaus Width: 3.0686**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U21-ch23, adc1

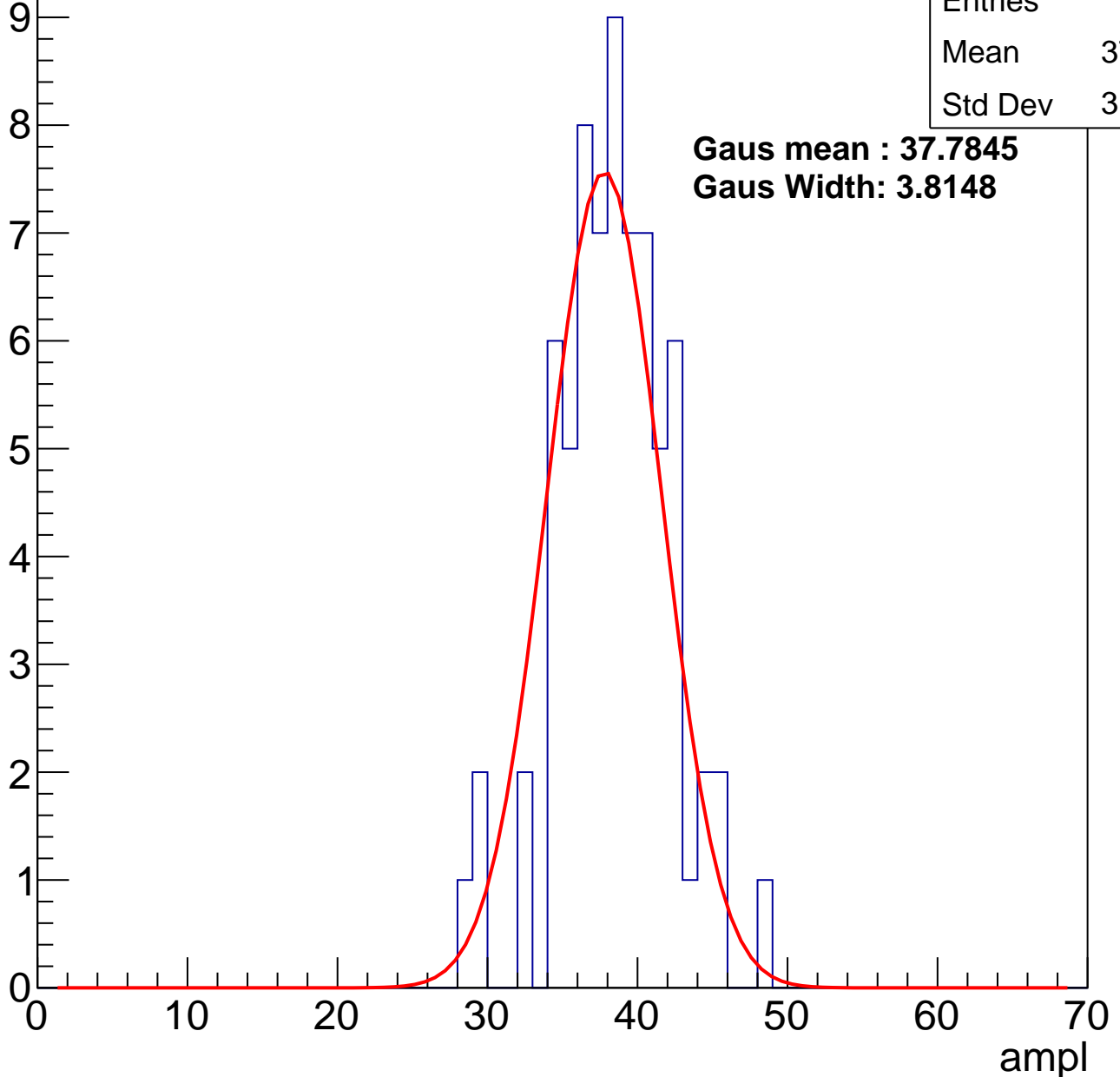
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	37.99
Std Dev	3.725

**Gaus mean : 37.7845**

**Gaus Width: 3.8148**



# B0L001S, U21-ch23, adc2

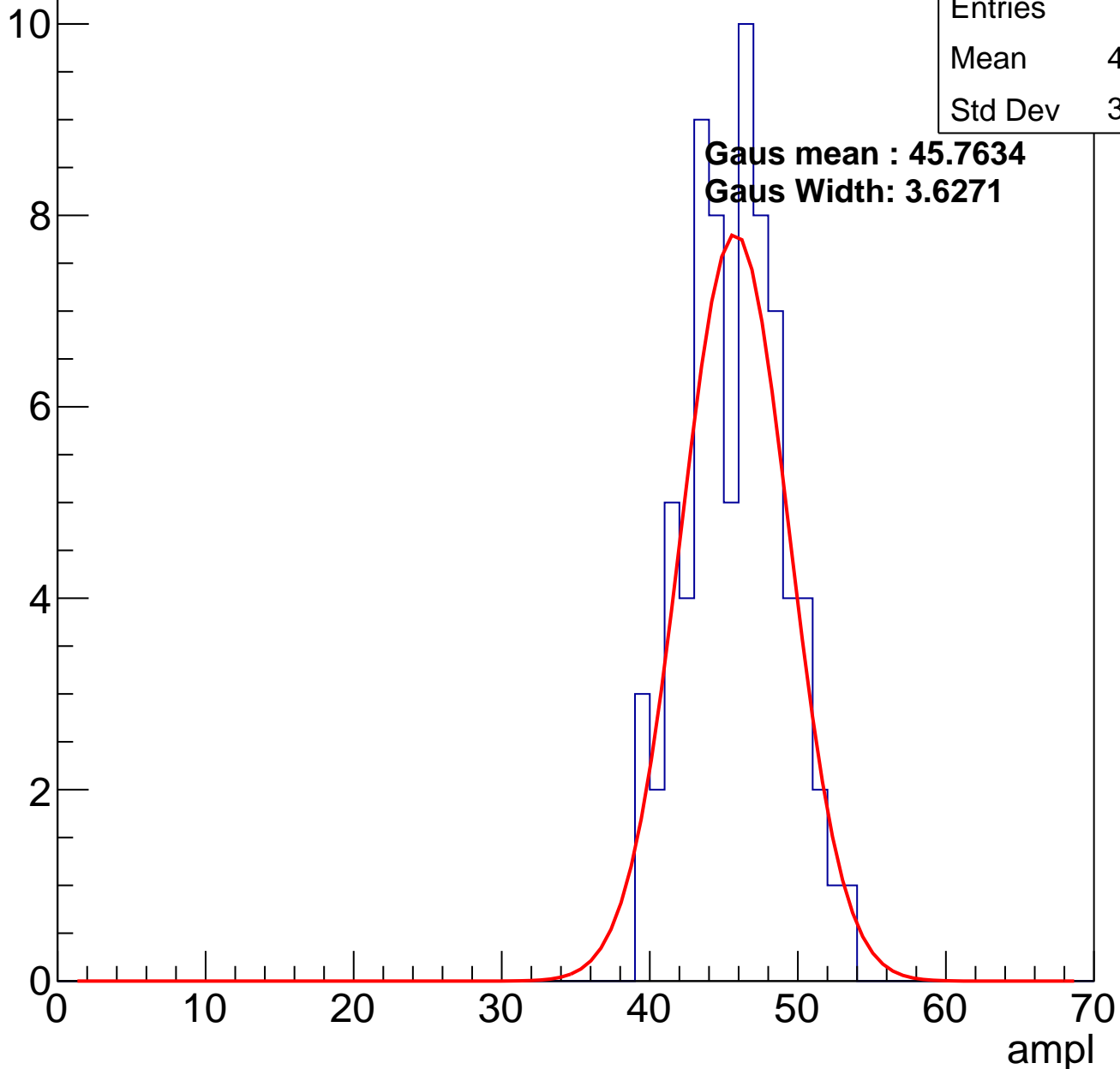
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	73
Mean	45.33
Std Dev	3.235

**Gaus mean : 45.7634**

**Gaus Width: 3.6271**

Entry

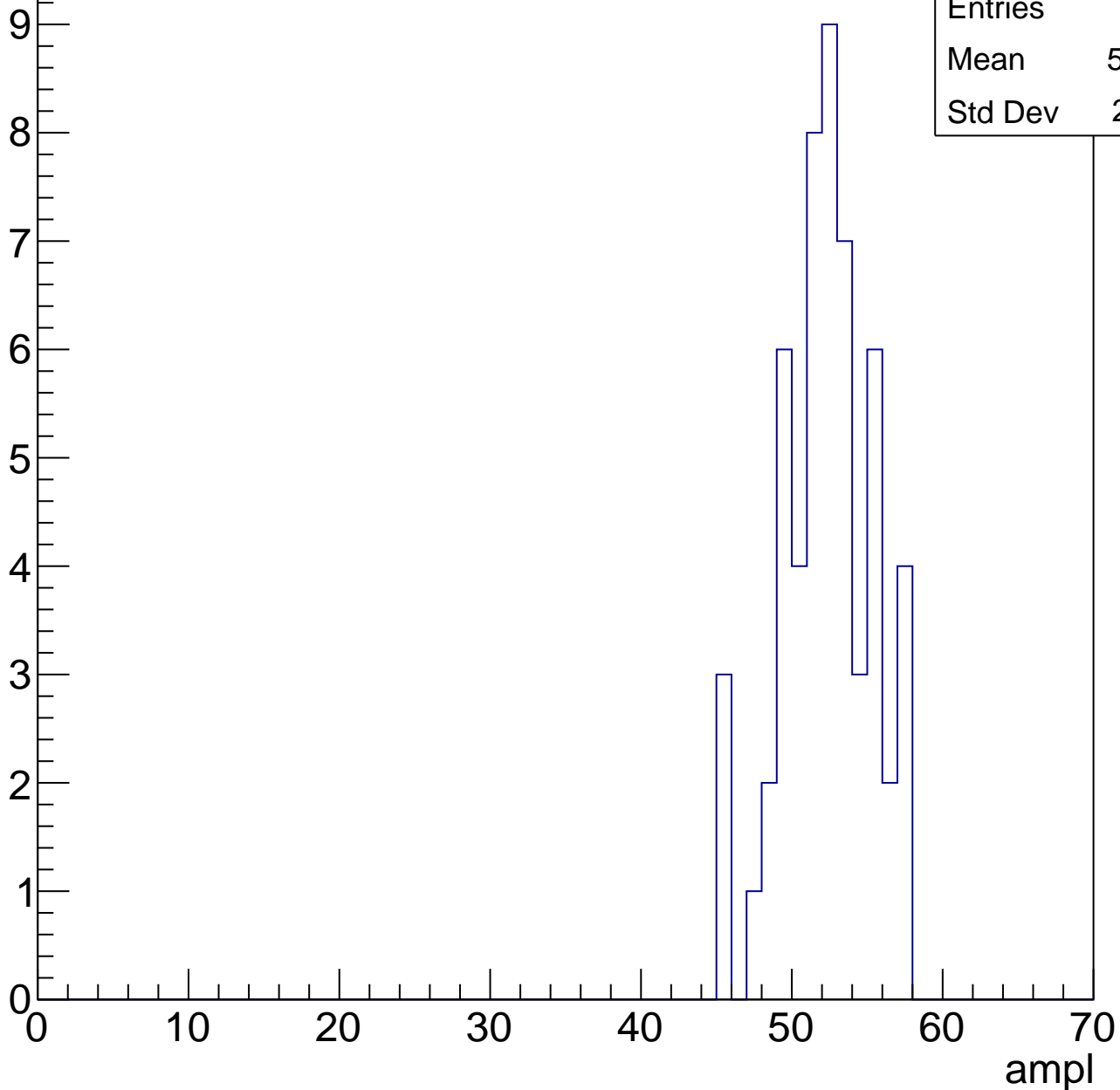


# B0L001S, U21-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	51.84
Std Dev	2.971

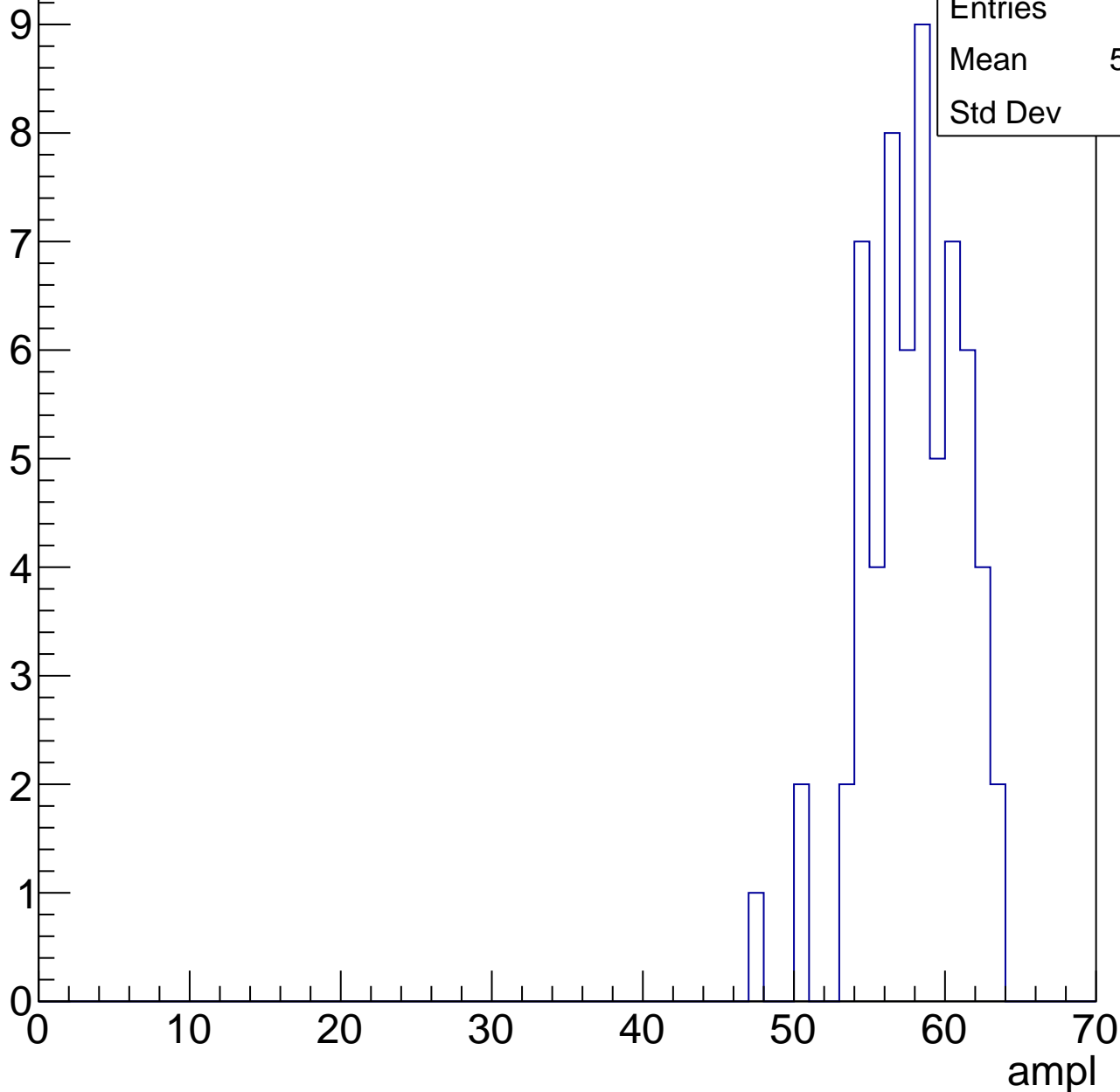


# B0L001S, U21-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	57.43
Std Dev	3.25

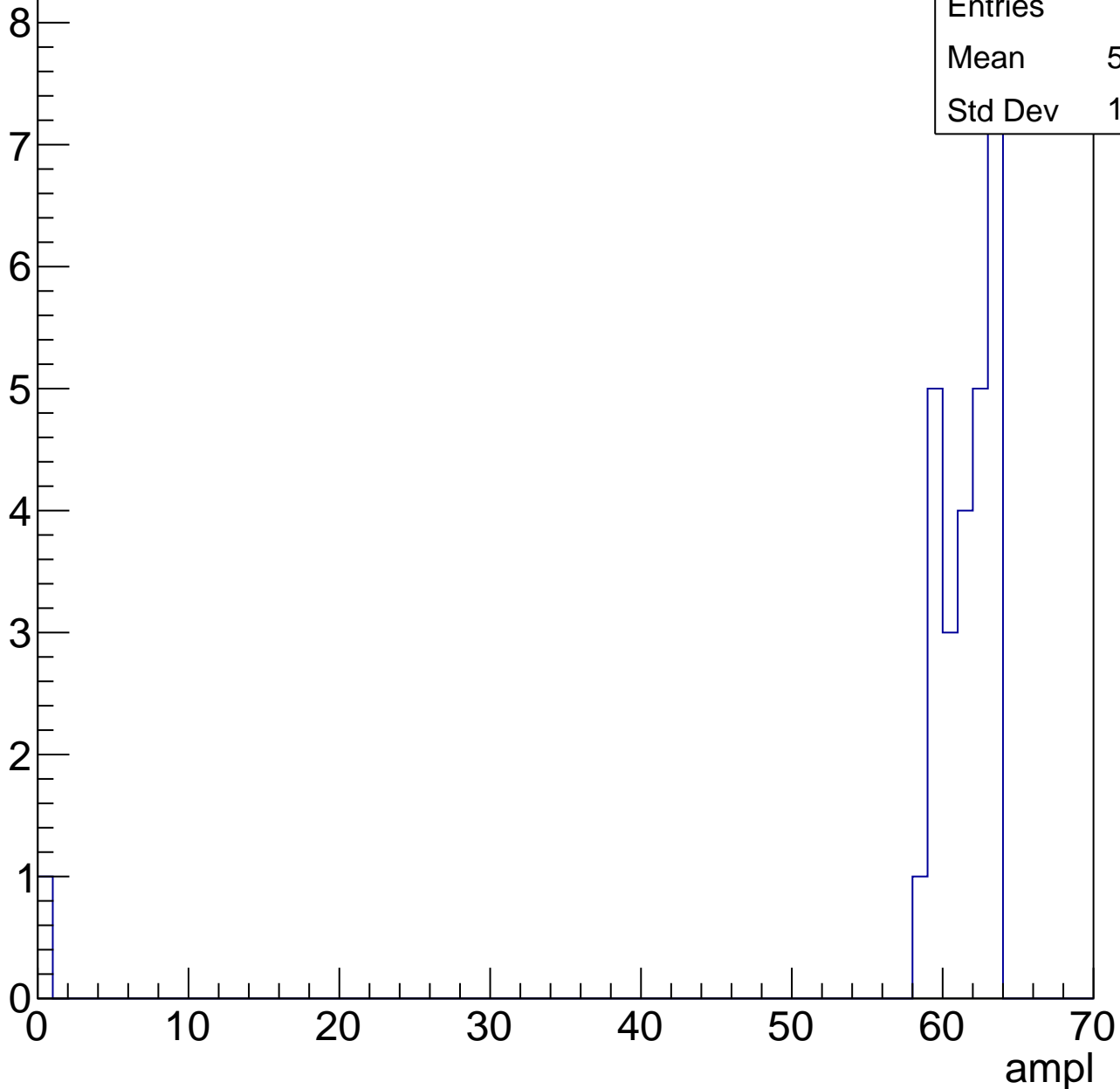


# B0L001S, U21-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	27
Mean	58.93
Std Dev	11.66



# B0L001S, U21-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch24, adc0

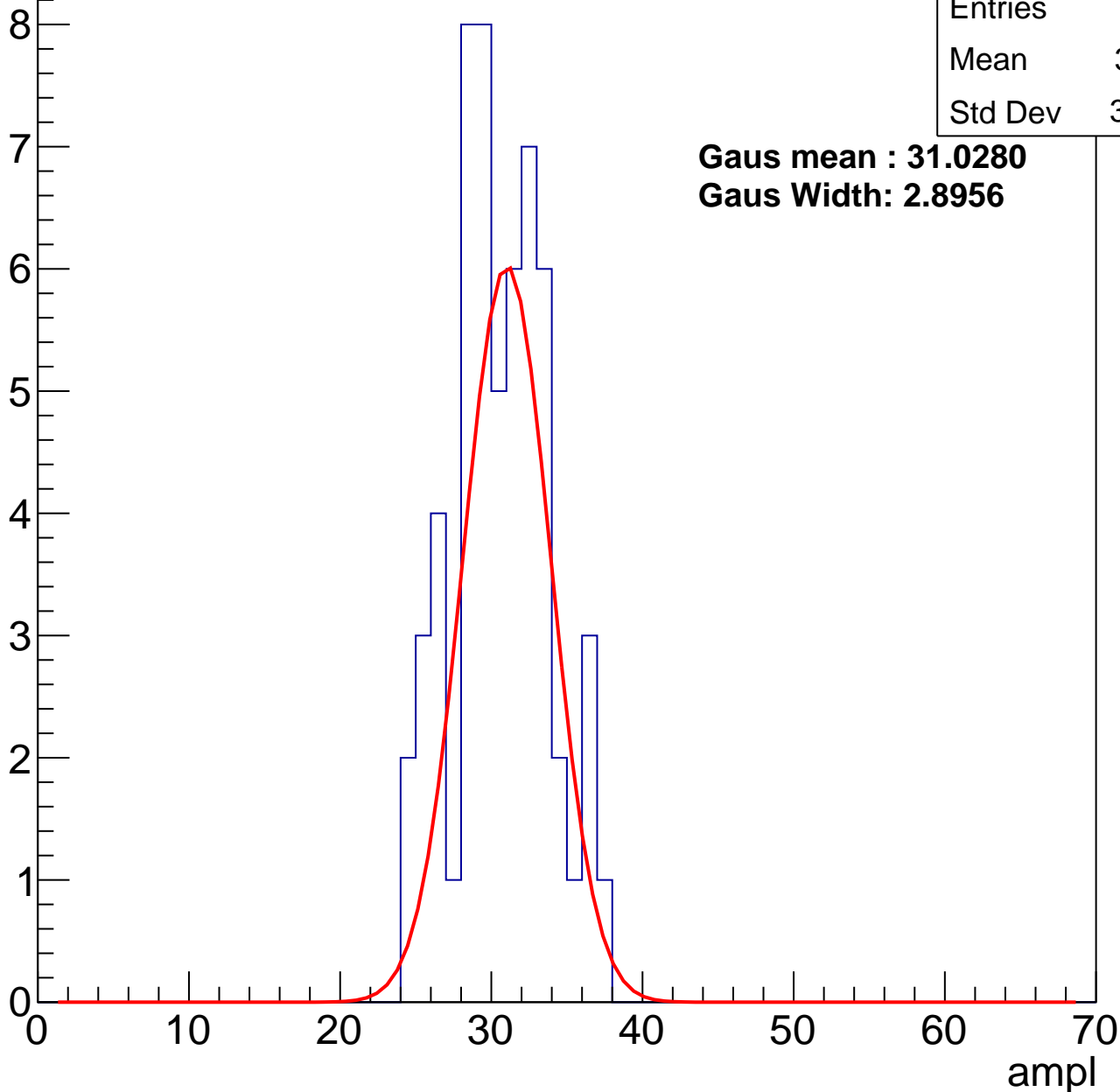
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	30.11
Std Dev	3.138

**Gaus mean : 31.0280**

**Gaus Width: 2.8956**



# B0L001S, U21-ch24, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	98
Mean	37.83
Std Dev	3.946

**Gaus mean : 38.2657**

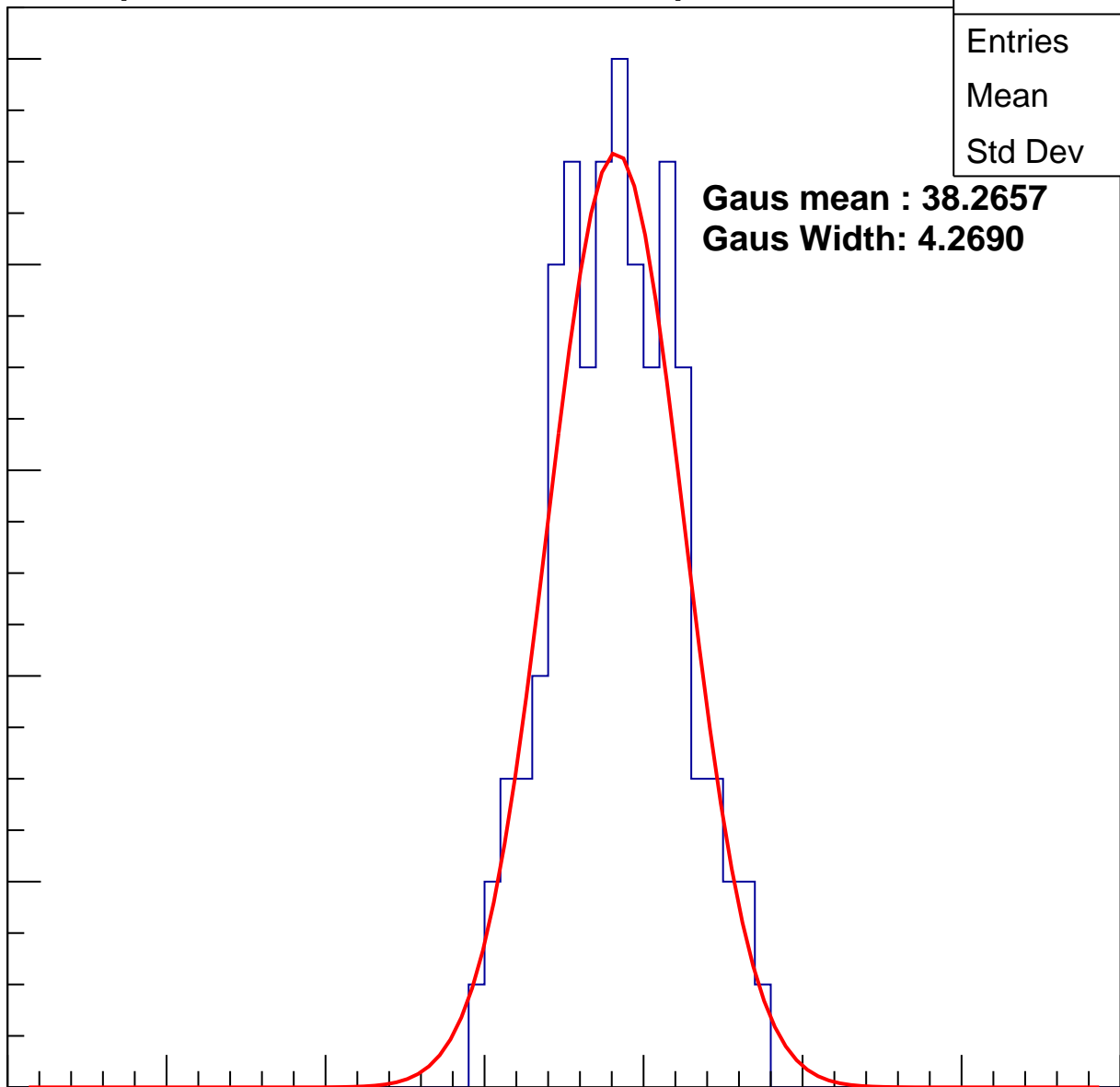
**Gaus Width: 4.2690**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U21-ch24, adc2

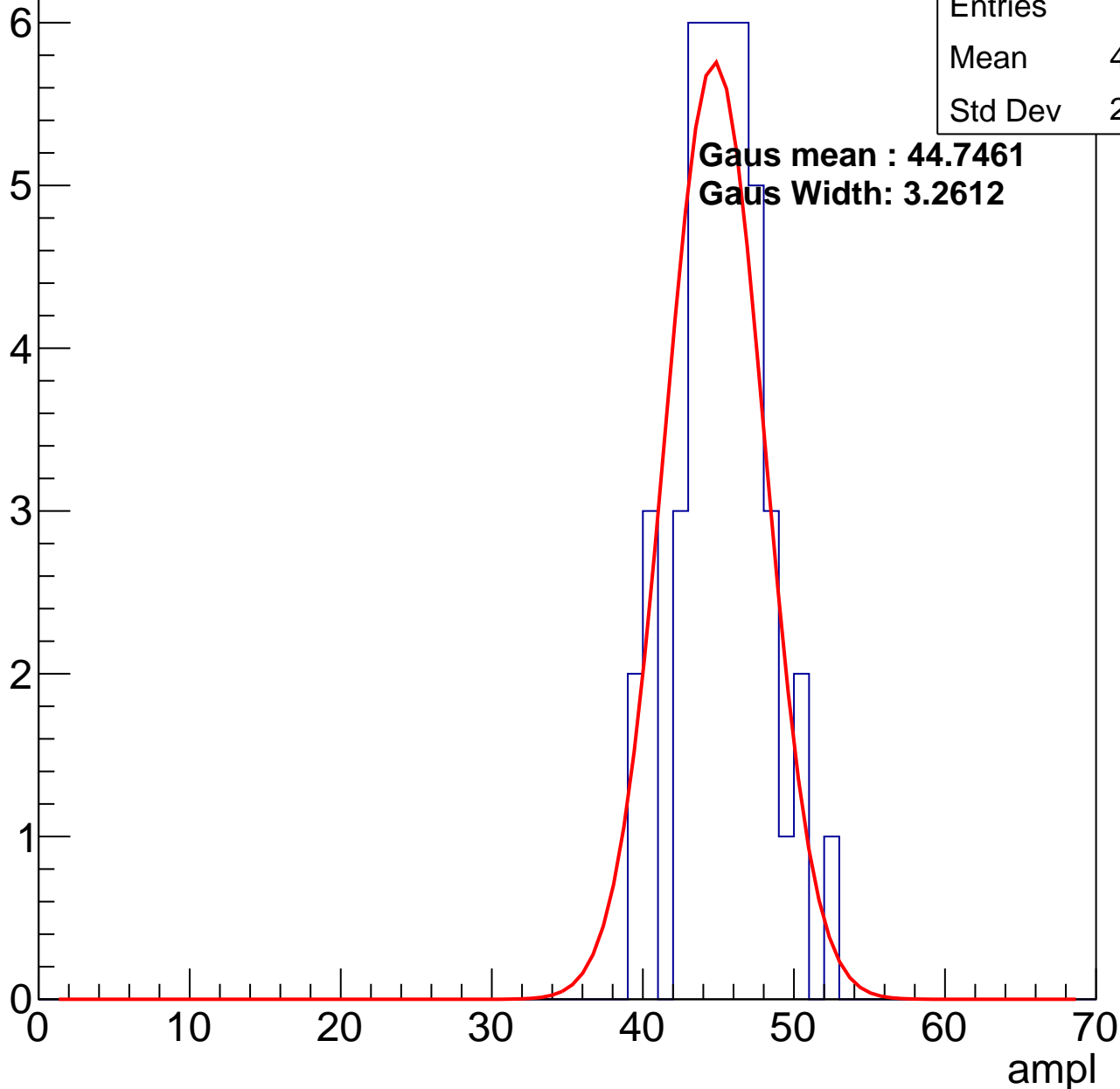
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	44
Mean	44.82
Std Dev	2.902

**Gaus mean : 44.7461**

**Gaus Width: 3.2612**

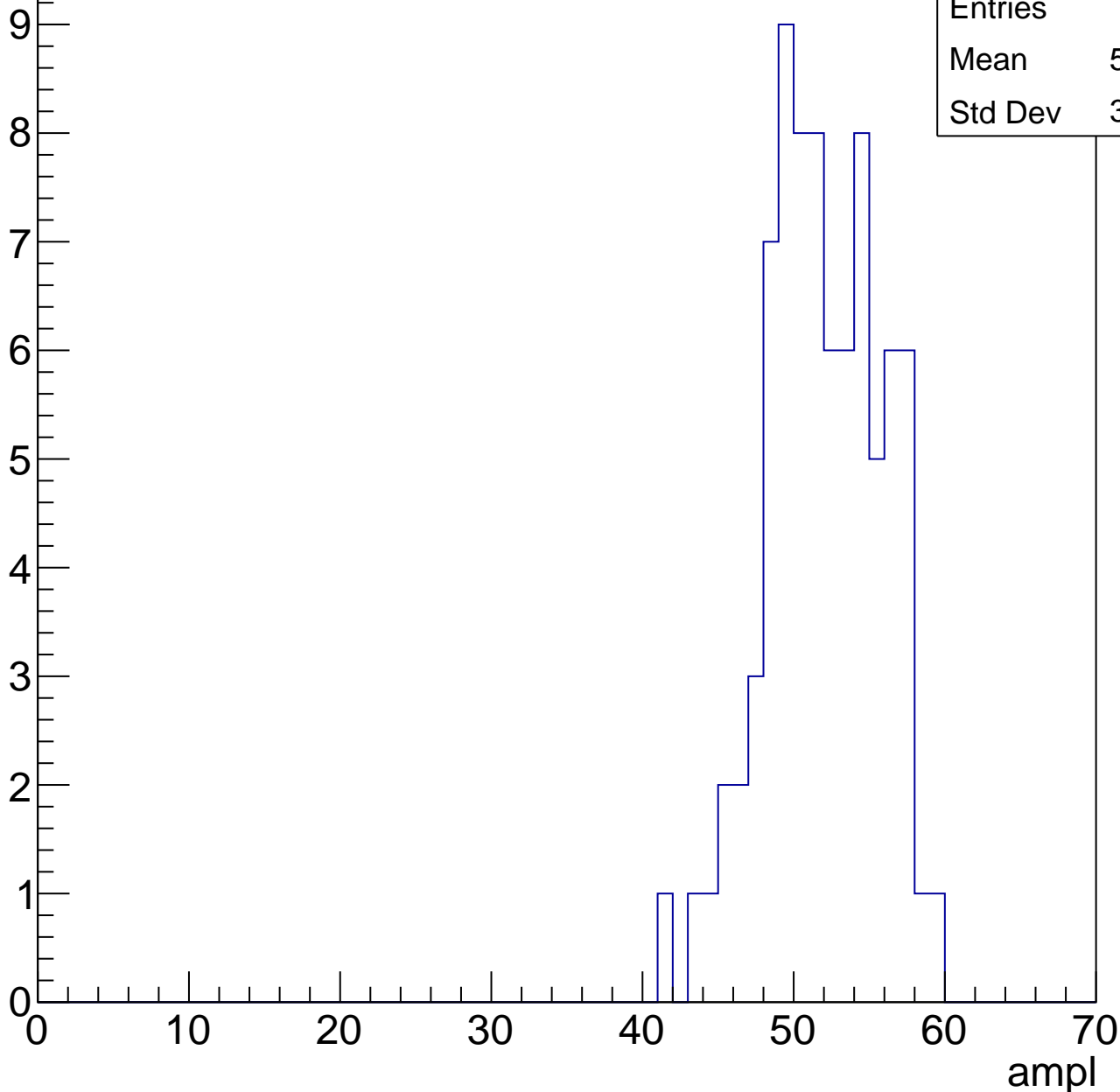


# B0L001S, U21-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	51.46
Std Dev	3.742

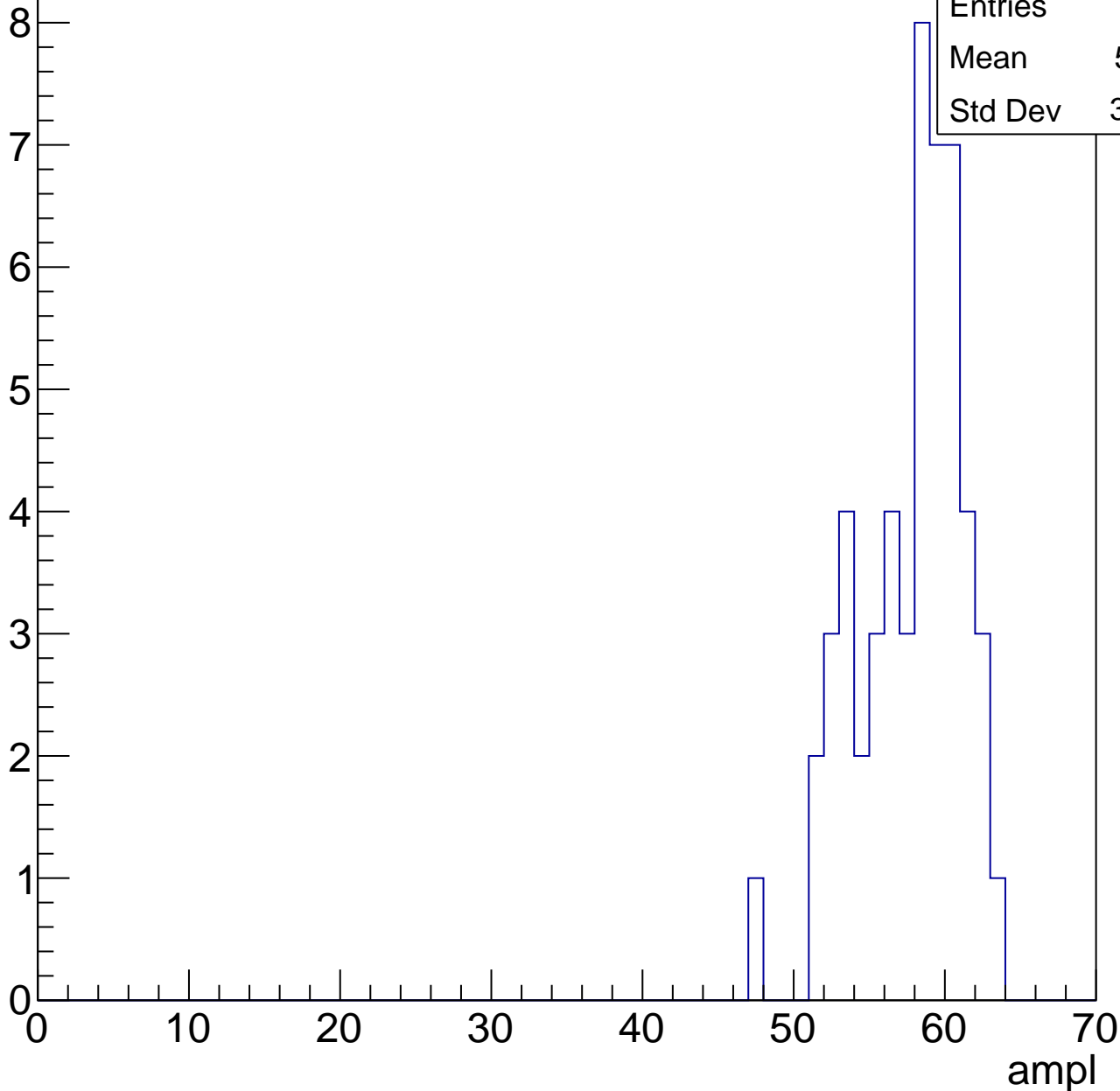


# B0L001S, U21-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	57.21
Std Dev	3.444

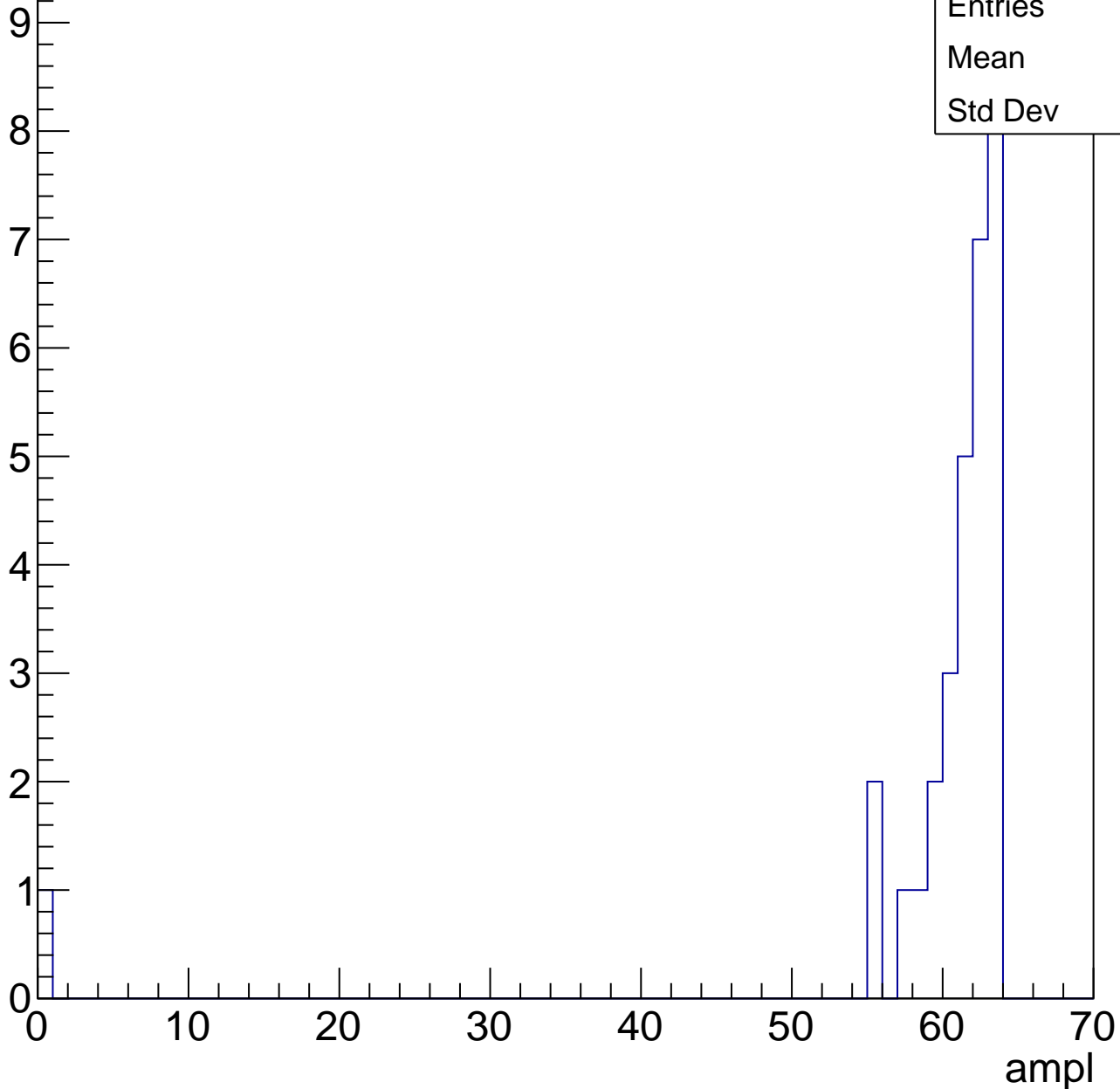


# B0L001S, U21-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	31
Mean	59
Std Dev	11



# B0L001S, U21-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U21-ch25, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	79
Mean	30.71
Std Dev	3.383

**Gaus mean : 31.4834**

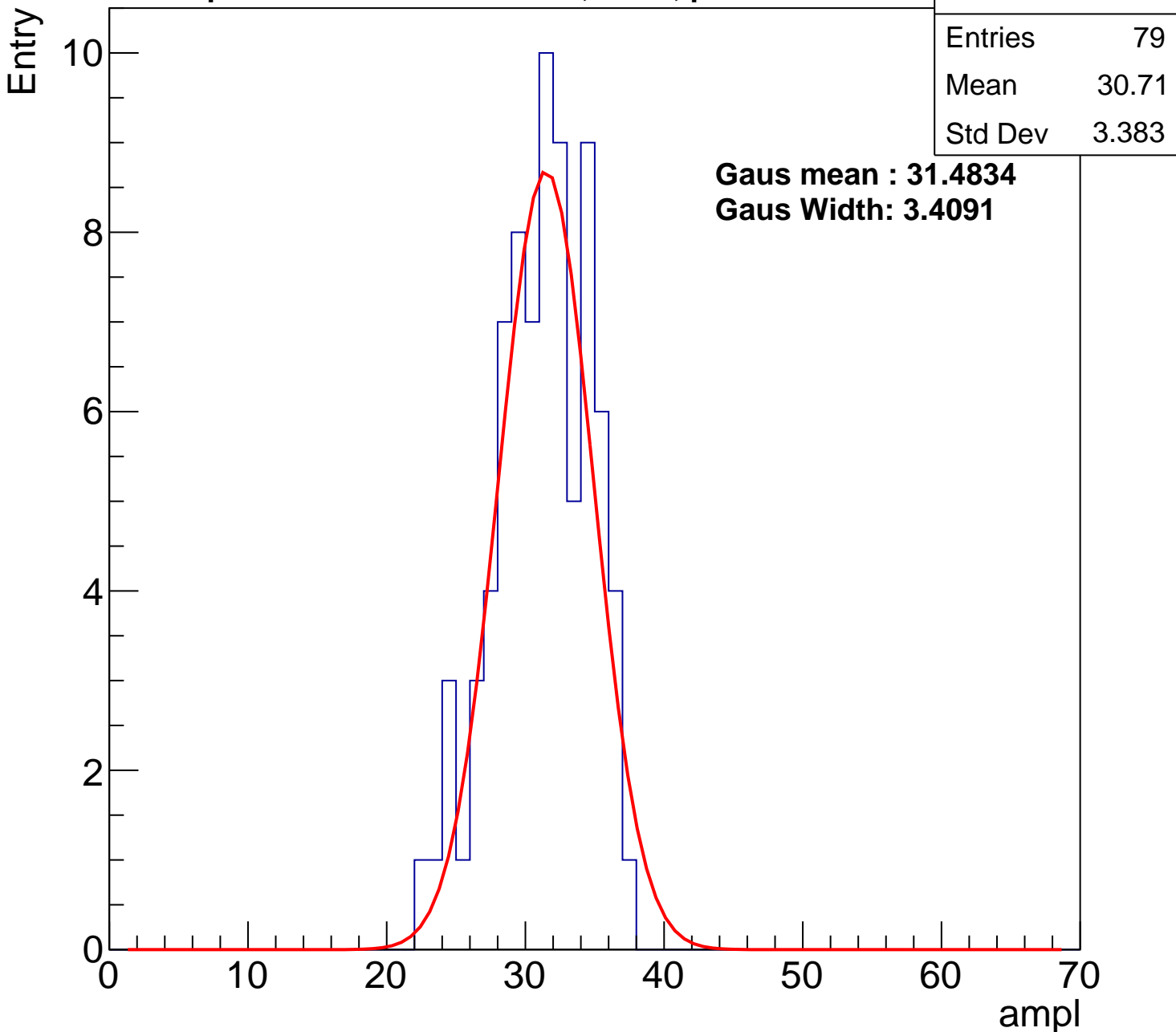
**Gaus Width: 3.4091**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U21-ch25, adc1

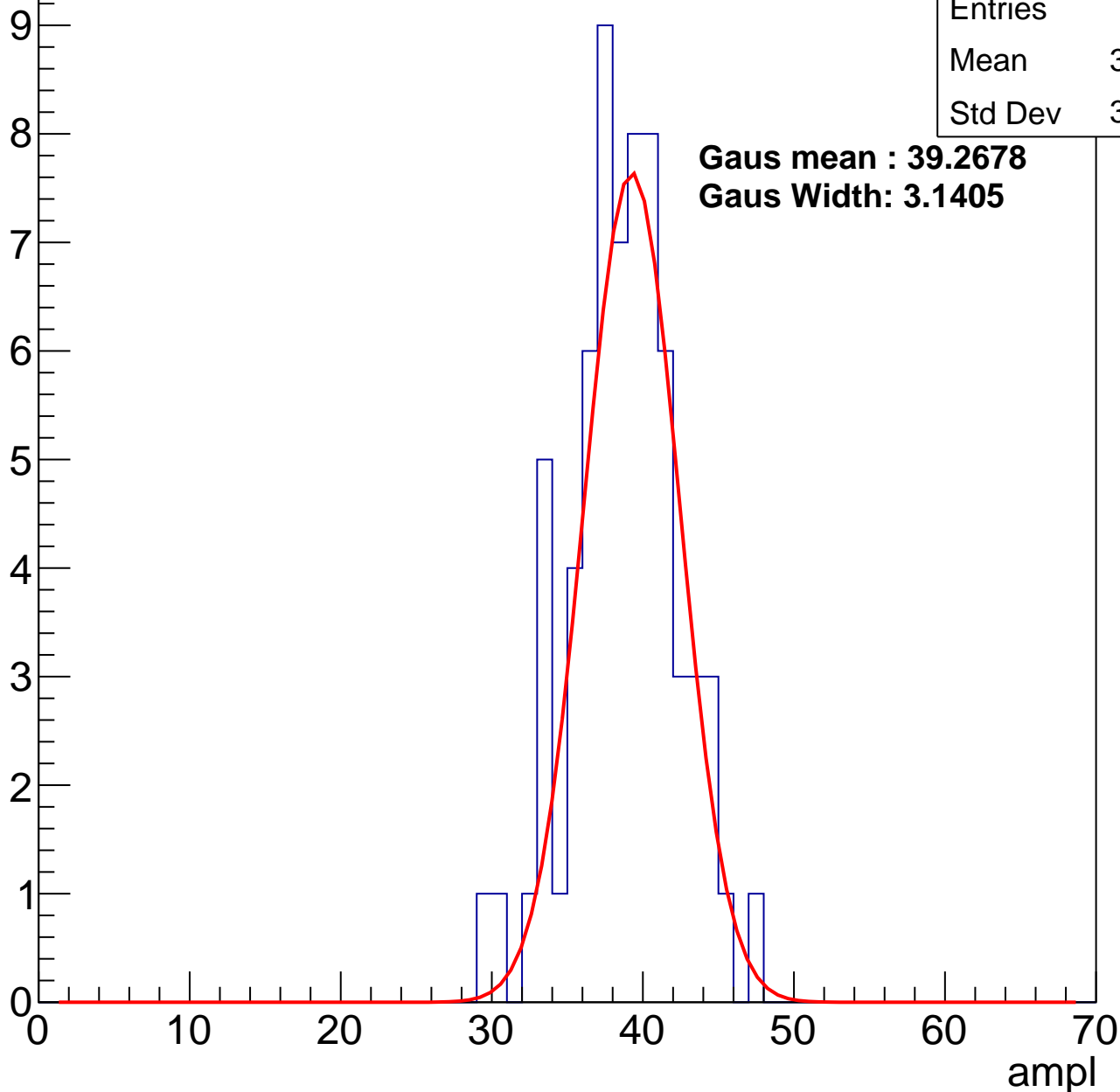
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	38.26
Std Dev	3.517

**Gaus mean : 39.2678**

**Gaus Width: 3.1405**



# B0L001S, U21-ch25, adc2

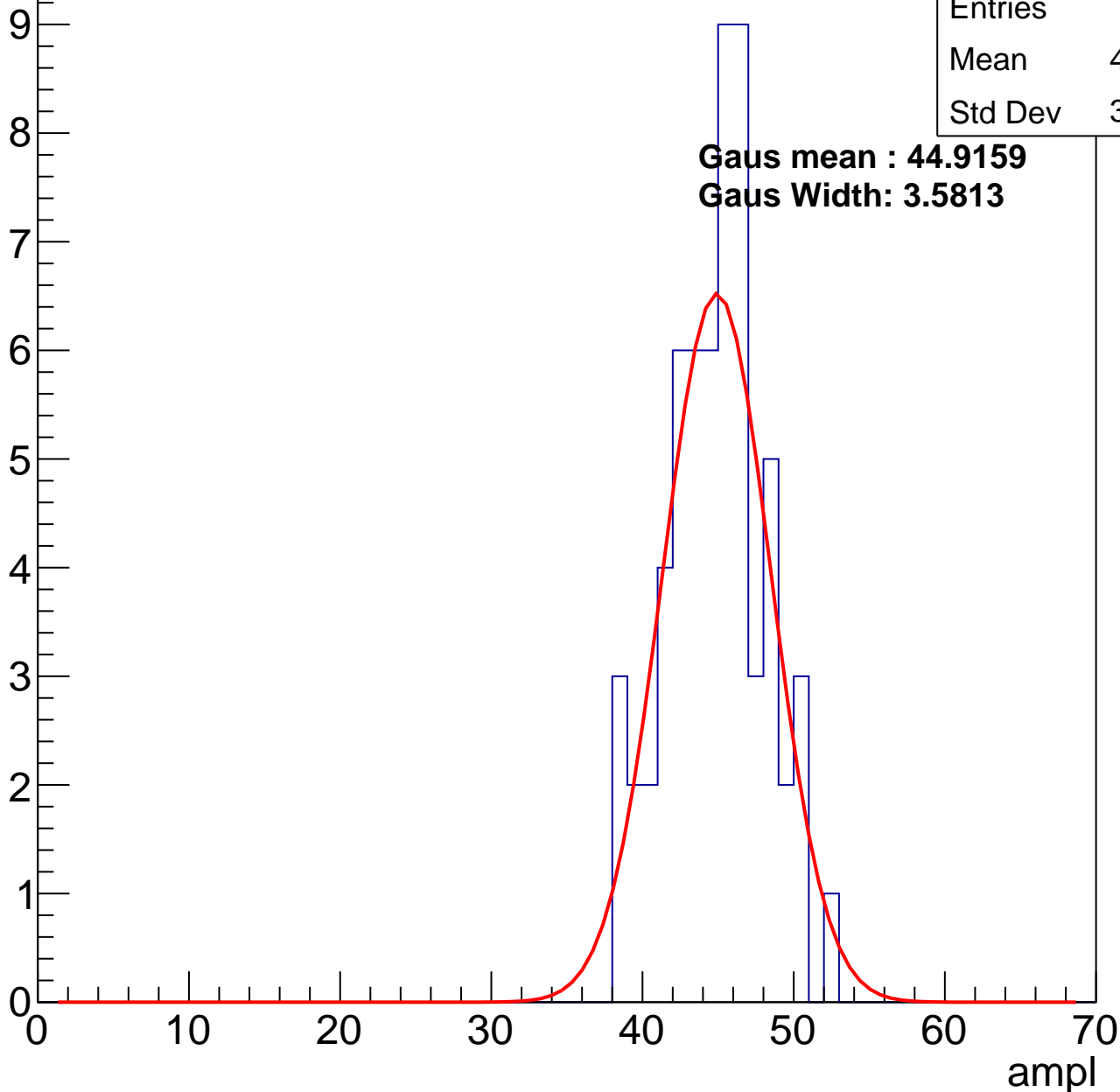
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	44.43
Std Dev	3.185

**Gaus mean : 44.9159**

**Gaus Width: 3.5813**



# B0L001S, U21-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

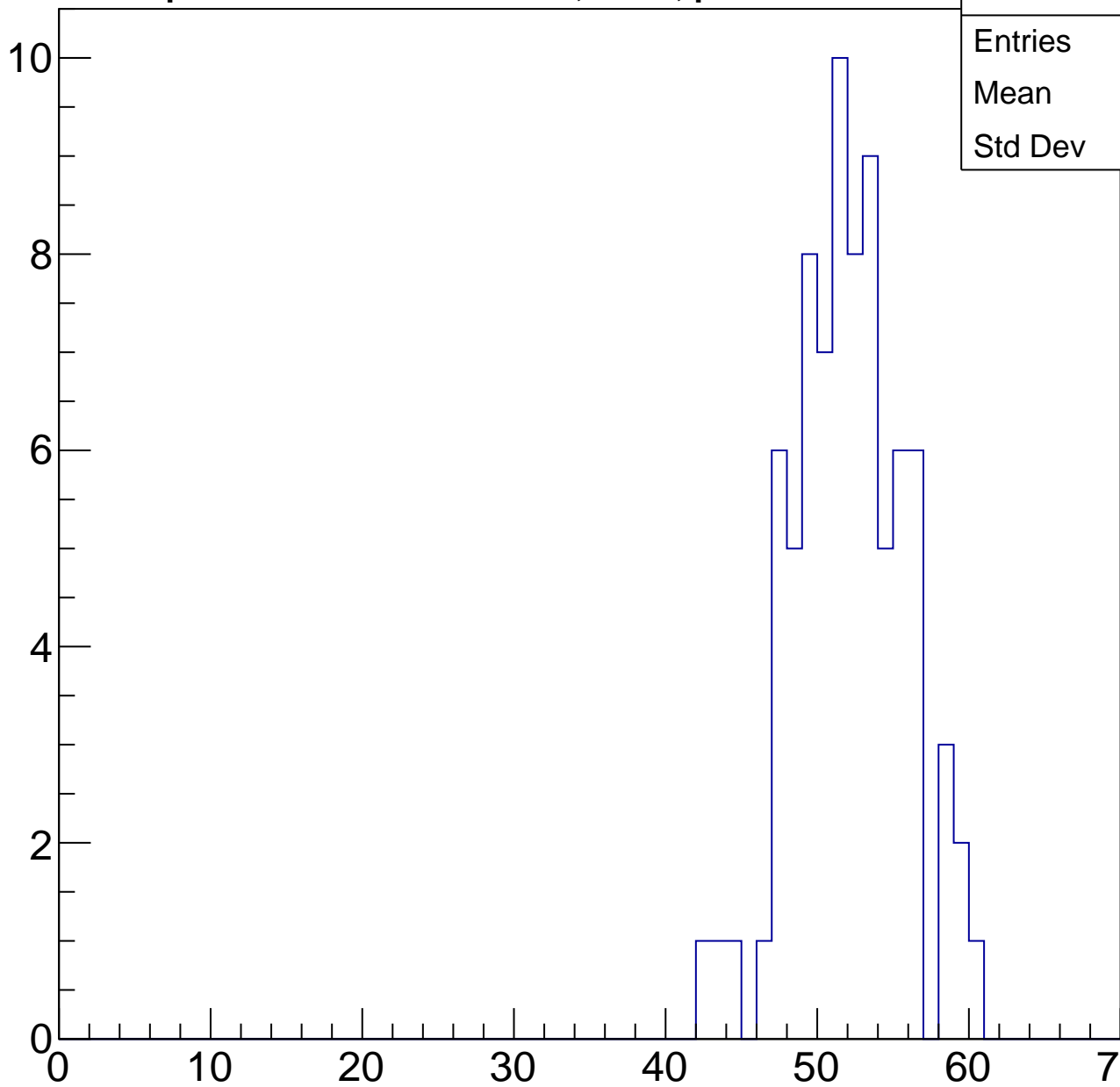
Entries	80
Mean	51.62
Std Dev	3.638

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

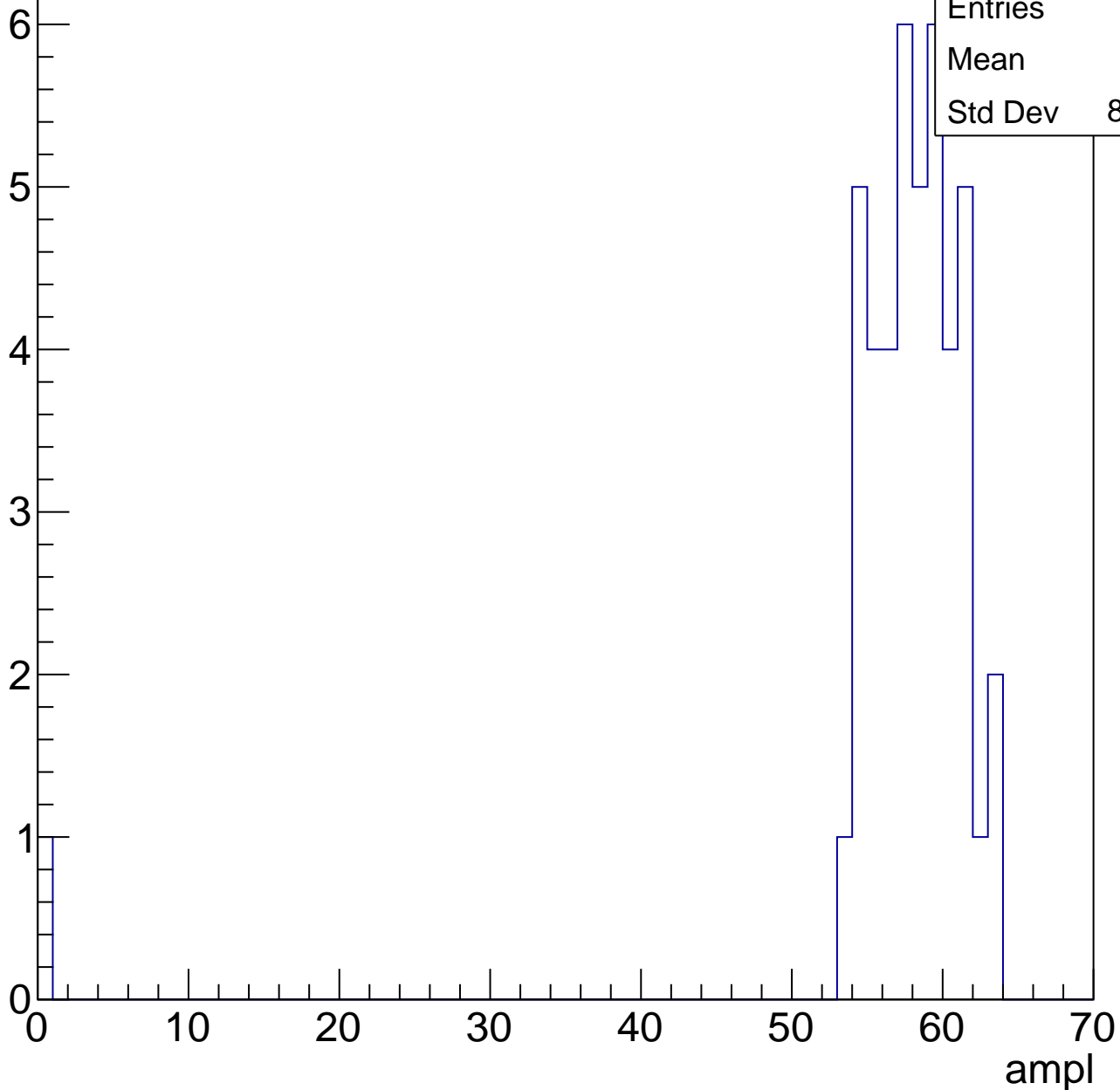


# B0L001S, U21-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	44
Mean	56.5
Std Dev	8.996

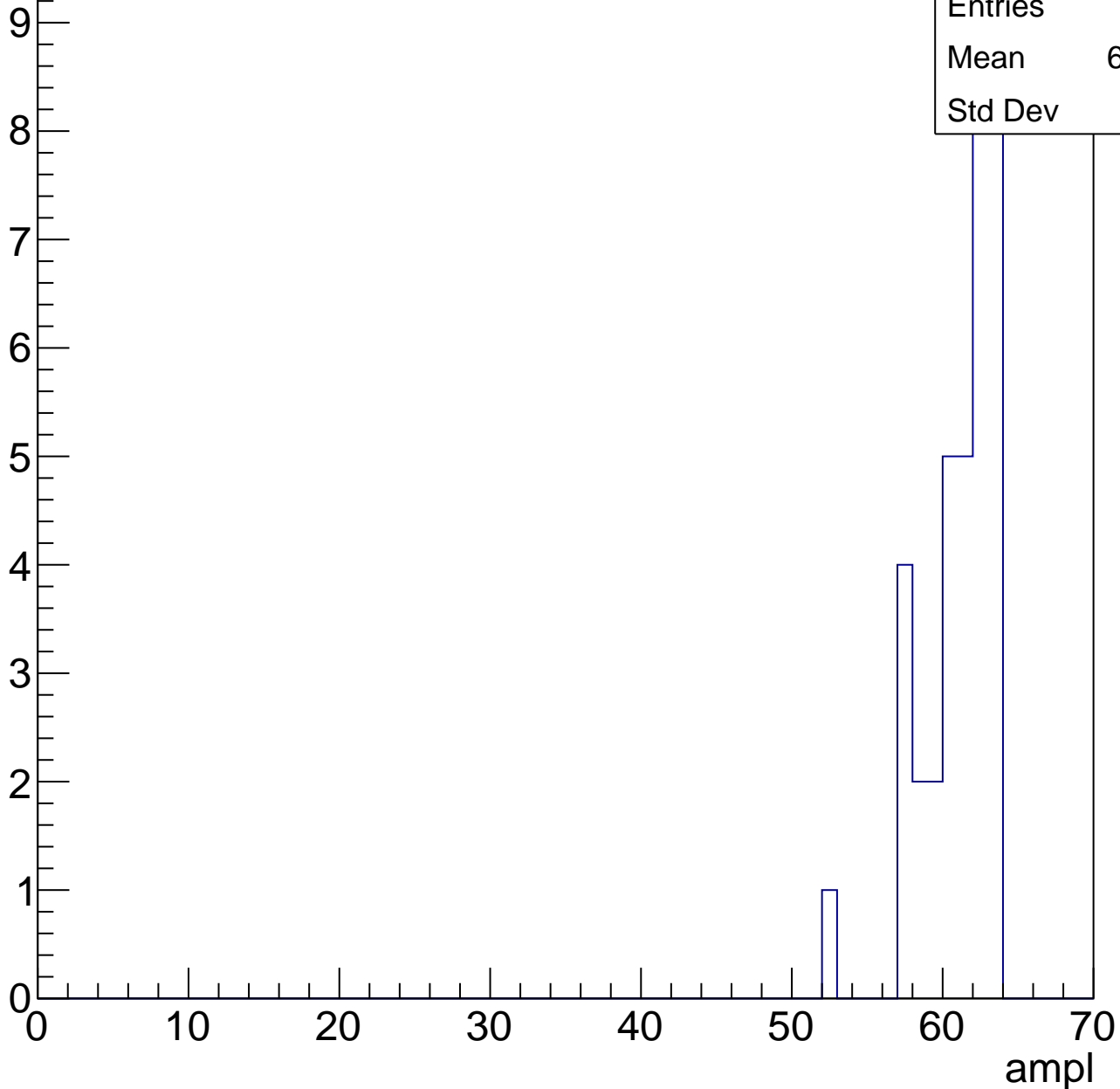


# B0L001S, U21-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	36
Mean	60.58
Std Dev	2.42



# B0L001S, U21-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U21-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U21-ch26, adc0

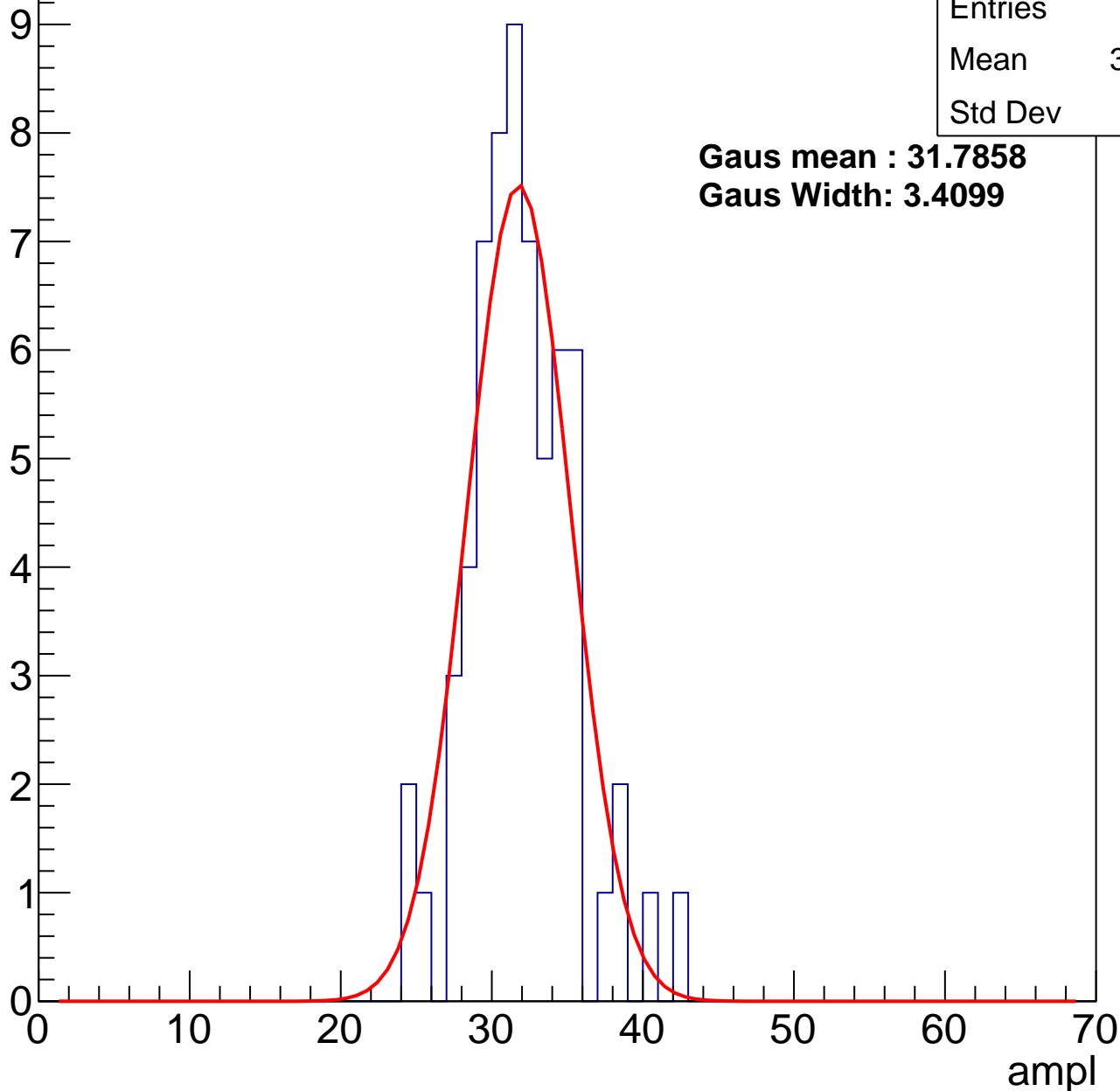
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	31.52
Std Dev	3.45

**Gaus mean : 31.7858**

**Gaus Width: 3.4099**



# B0L001S, U21-ch26, adc1

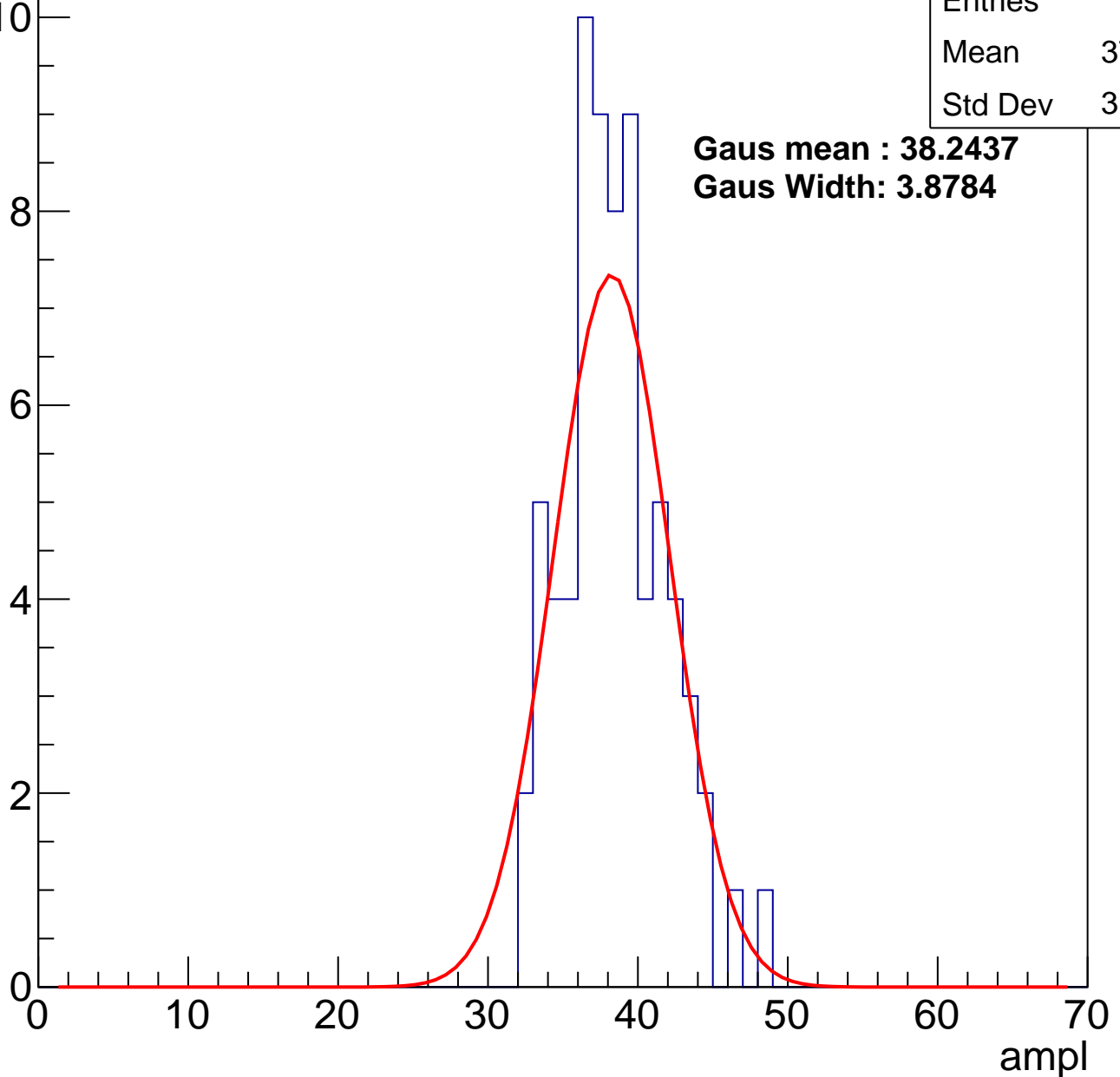
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	37.99
Std Dev	3.338

**Gaus mean : 38.2437**

**Gaus Width: 3.8784**



# B0L001S, U21-ch26, adc2

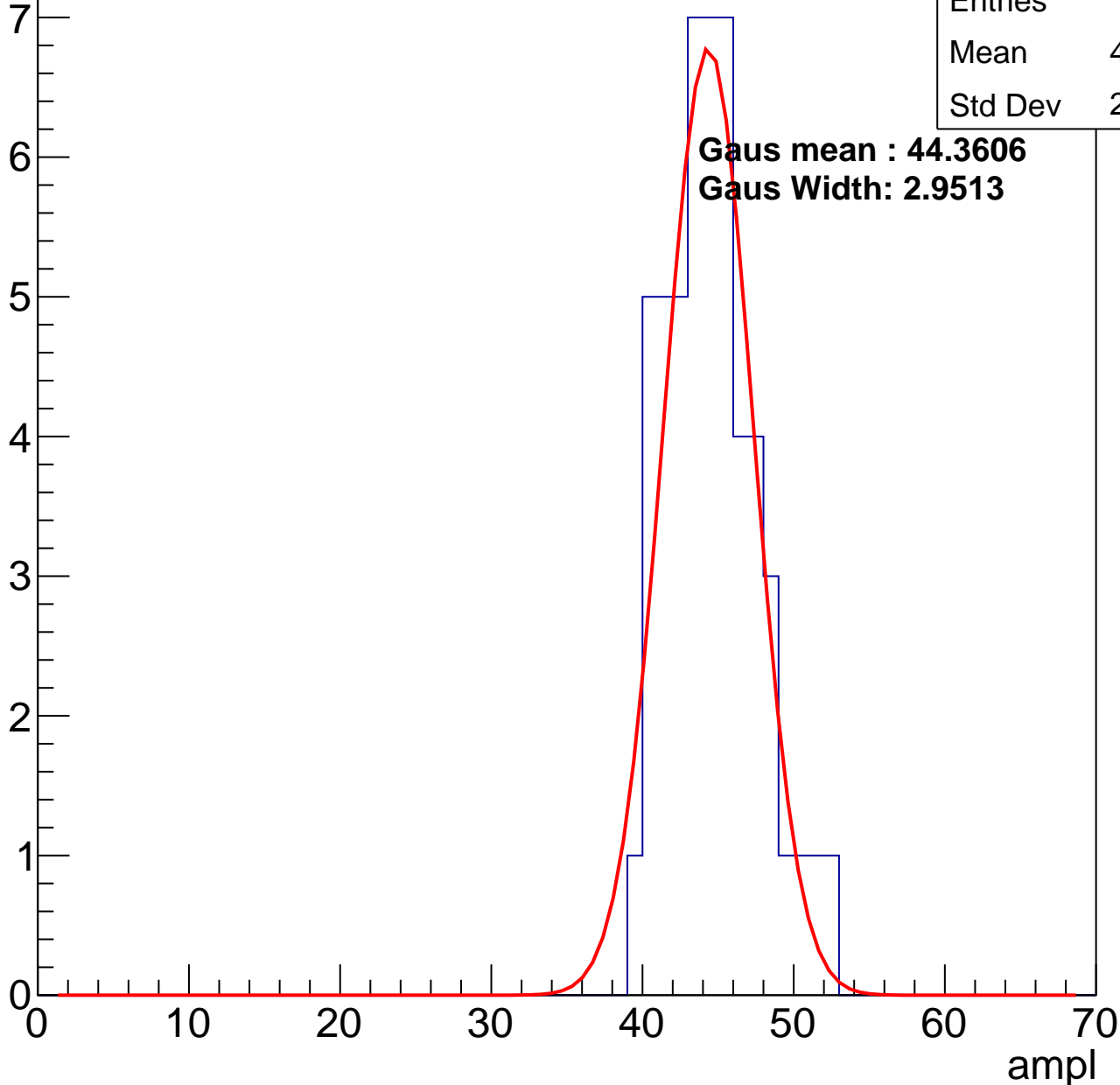
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	44.15
Std Dev	2.964

**Gaus mean : 44.3606**

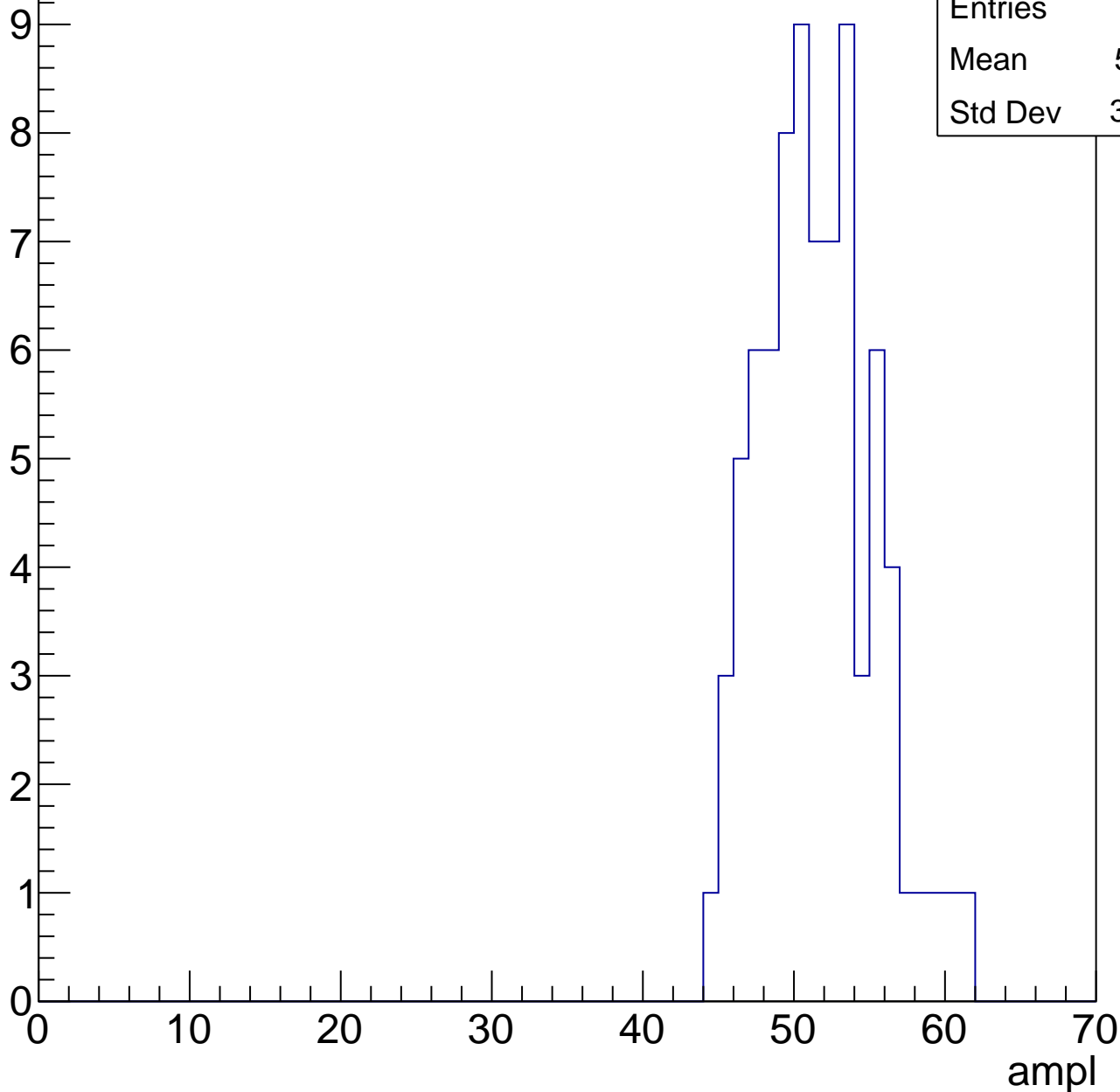
**Gaus Width: 2.9513**



# B0L001S, U21-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



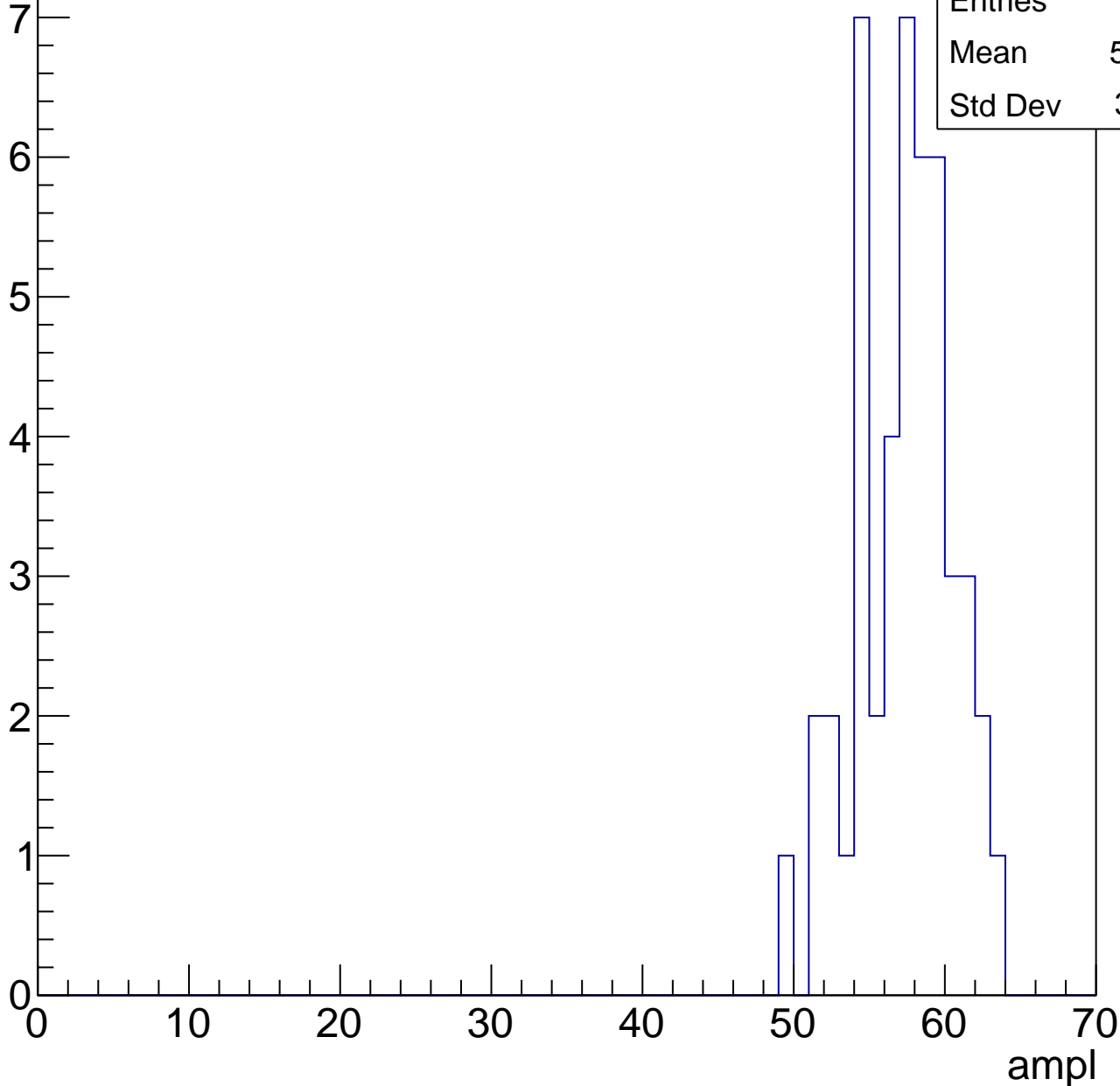
Entries	79
Mean	51.01
Std Dev	3.679

# B0L001S, U21-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	56.83
Std Dev	3.151

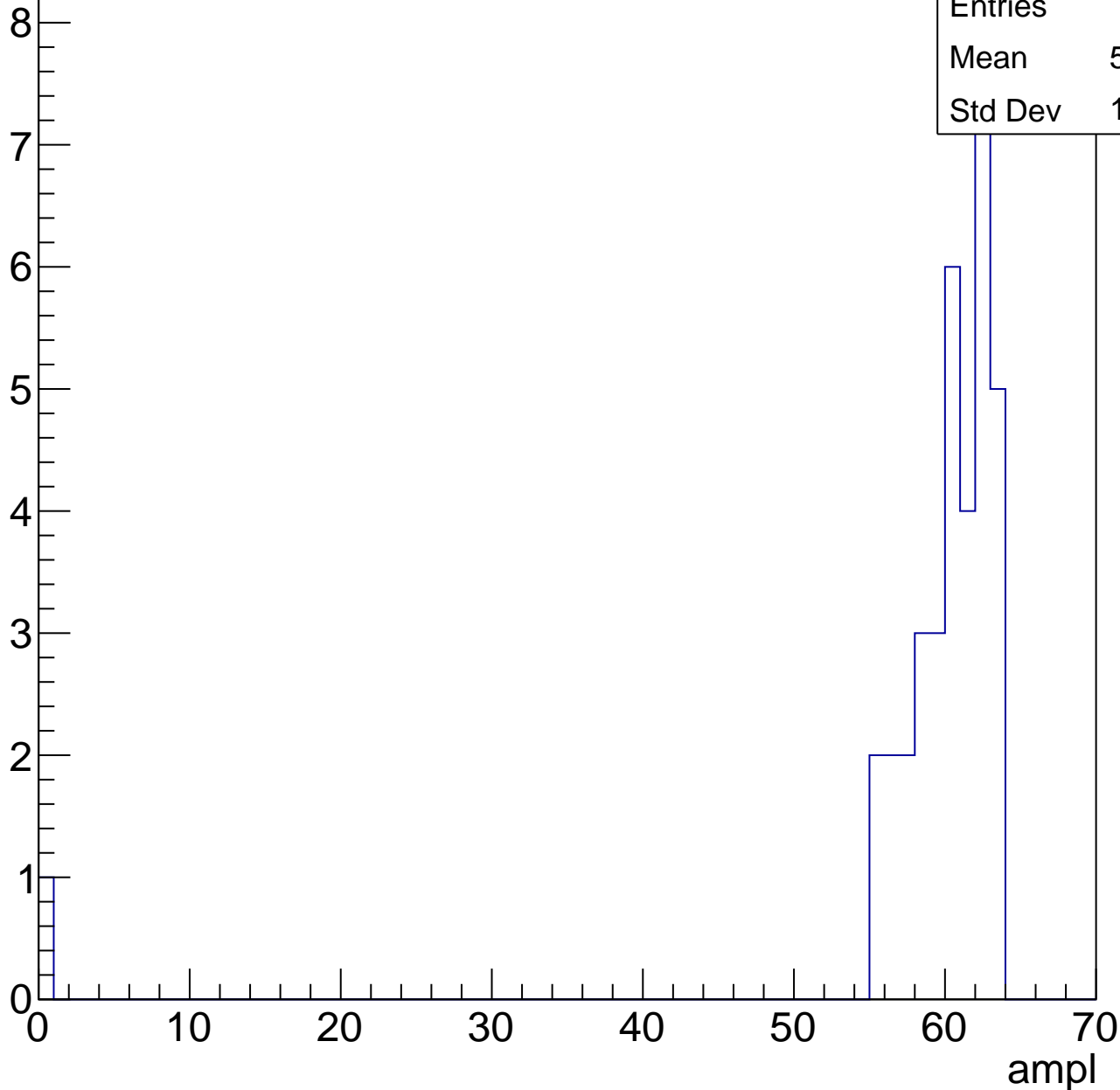


# B0L001S, U21-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

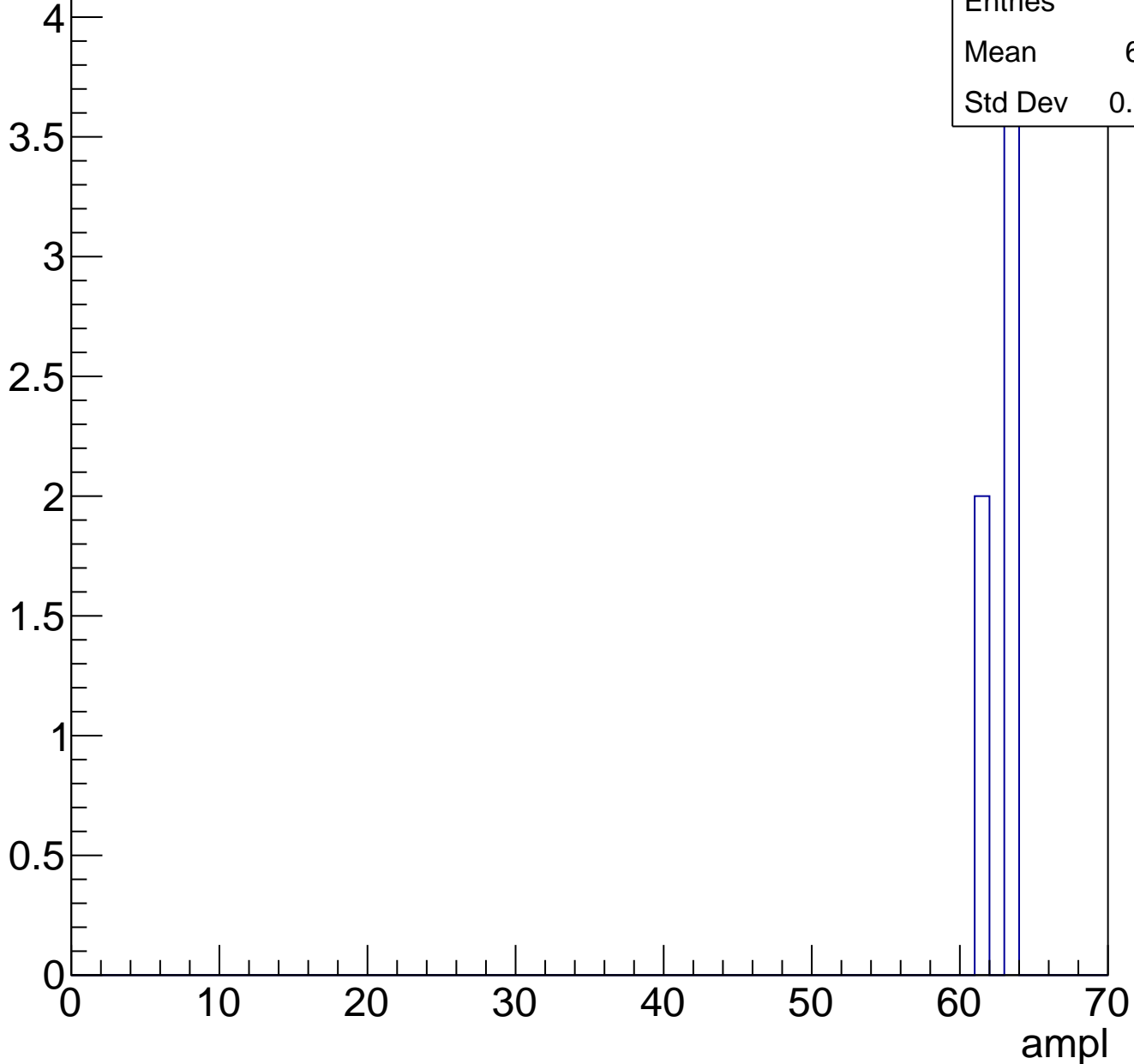
Entries	36
Mean	58.39
Std Dev	10.14



# B0L001S, U21-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch27, adc0

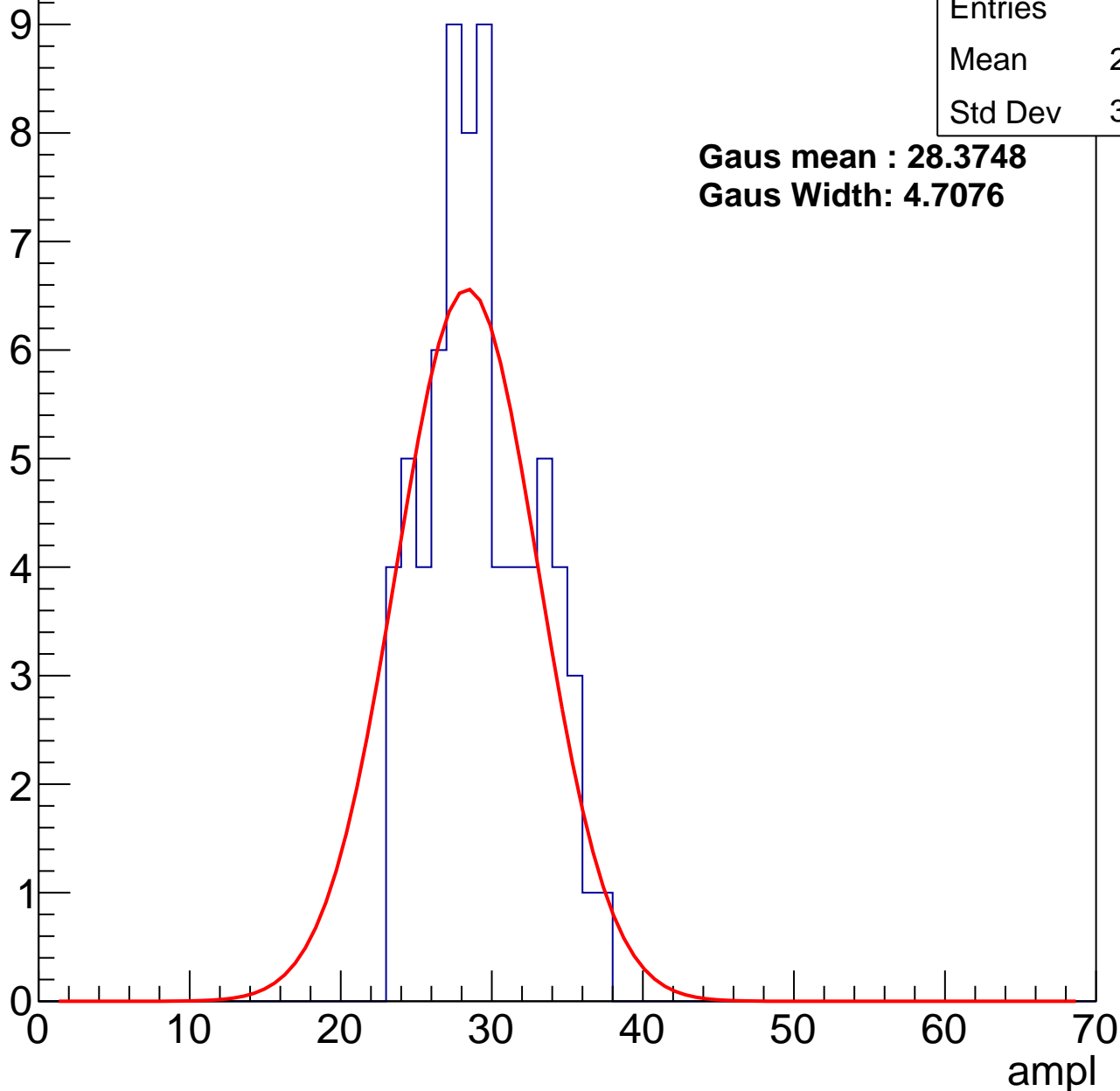
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	28.83
Std Dev	3.532

**Gaus mean : 28.3748**

**Gaus Width: 4.7076**



# B0L001S, U21-ch27, adc1

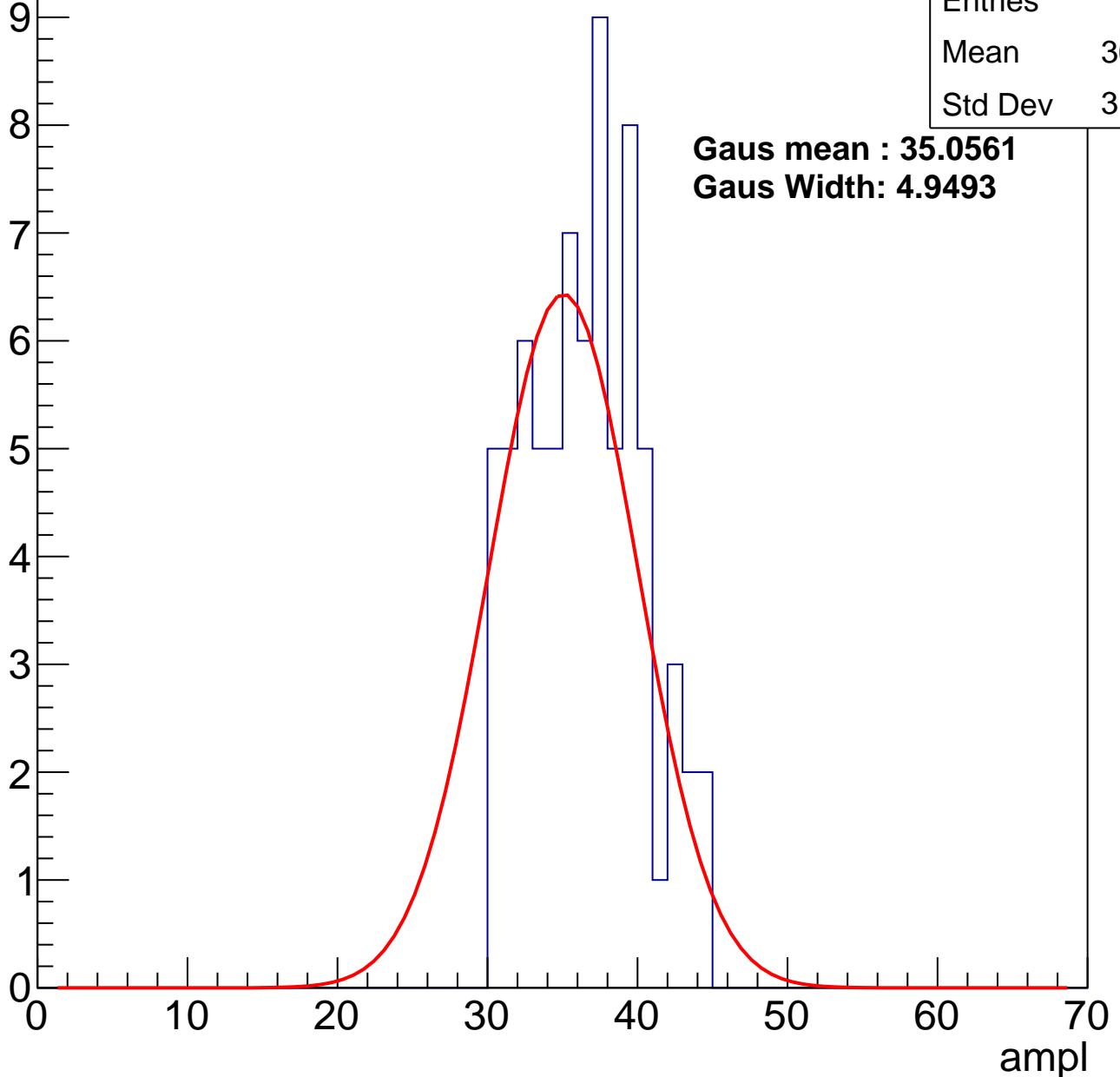
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	36.07
Std Dev	3.699

**Gaus mean : 35.0561**

**Gaus Width: 4.9493**



# B0L001S, U21-ch27, adc2

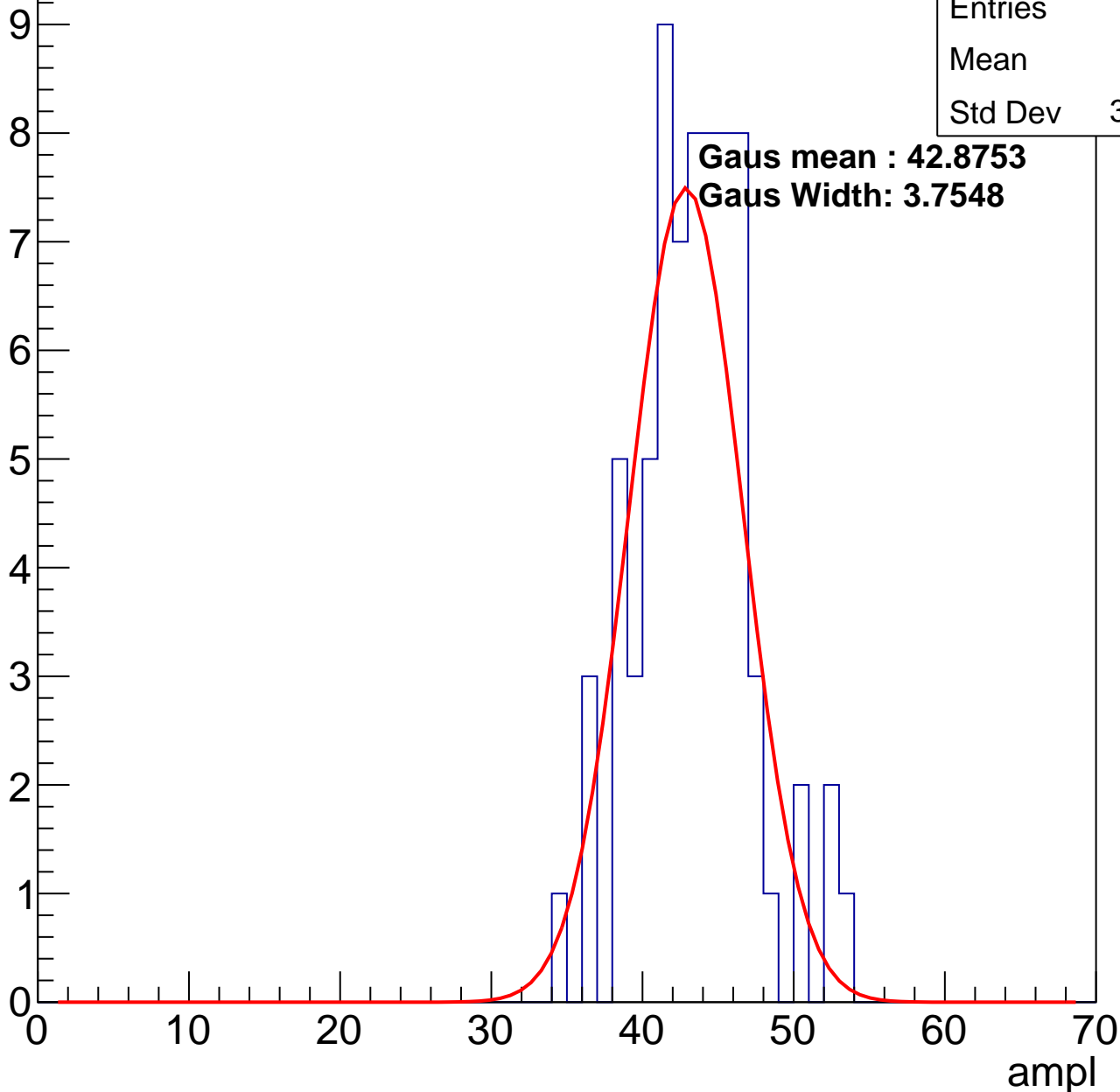
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	43
Std Dev	3.738

**Gaus mean : 42.8753**

**Gaus Width: 3.7548**

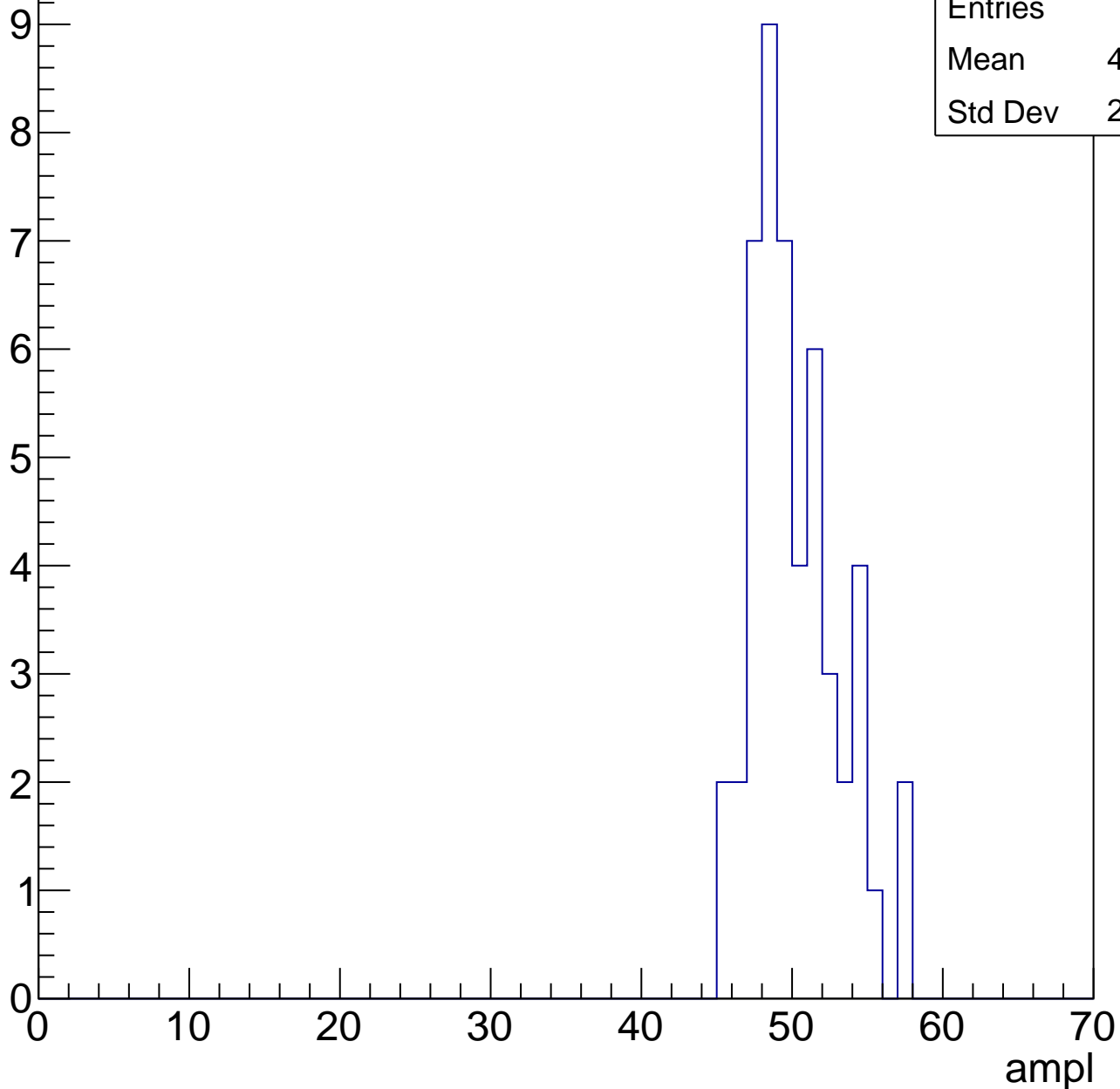


# B0L001S, U21-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

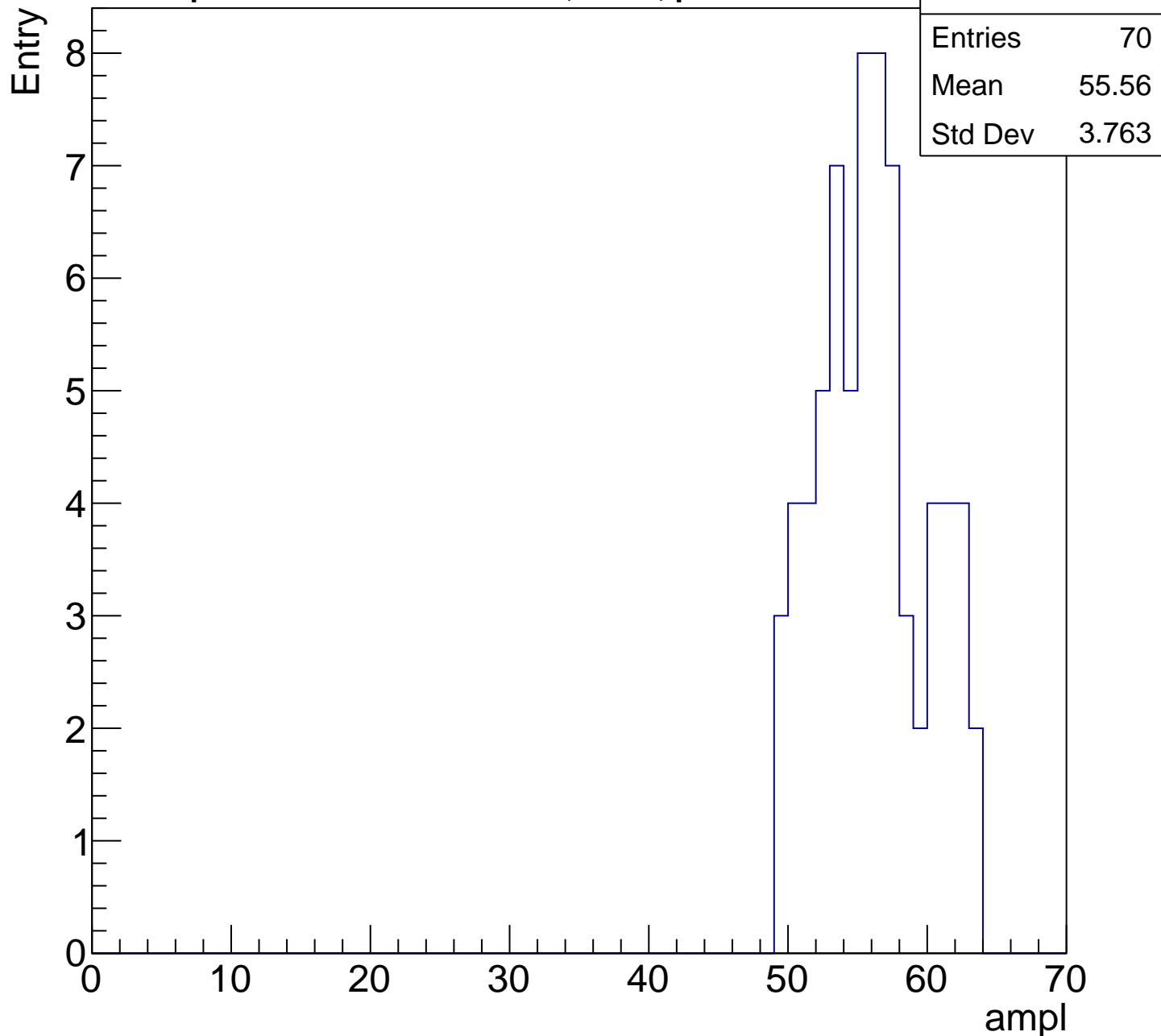
Entry

Entries	49
Mean	49.78
Std Dev	2.887



# B0L001S, U21-ch27, adc4

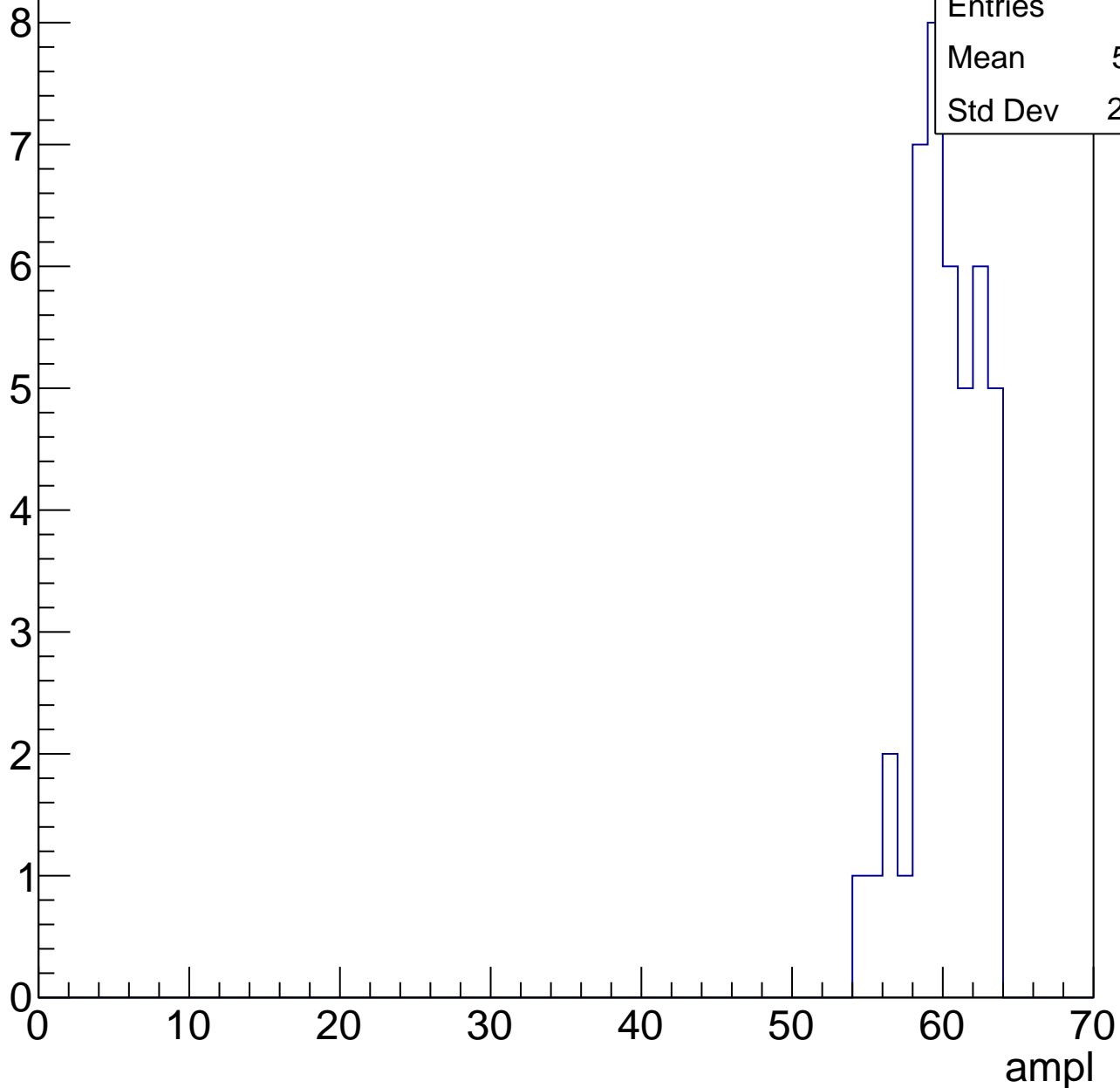
calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U21-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

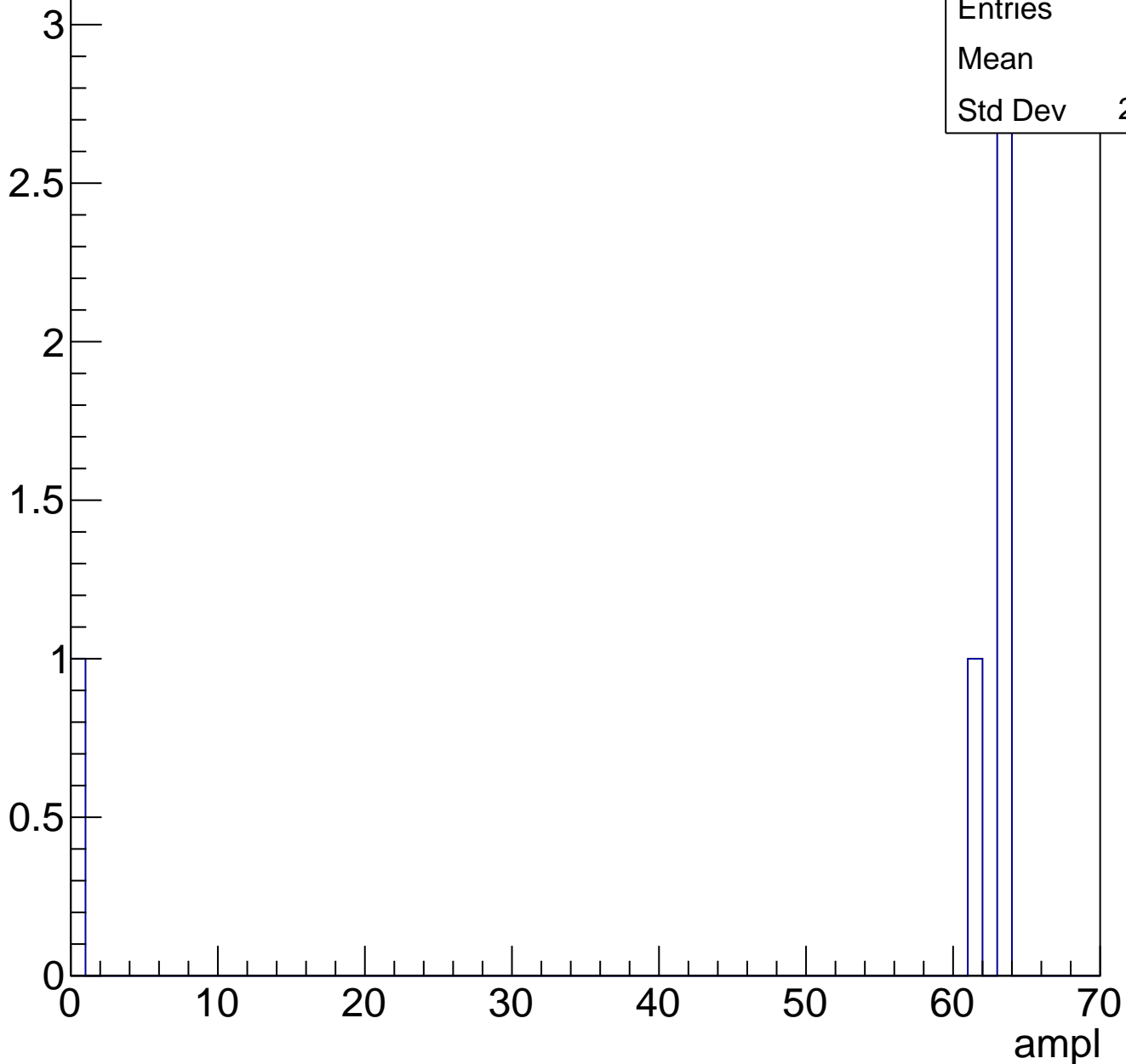


Entries	42
Mean	59.71
Std Dev	2.228

# B0L001S, U21-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U21-ch28, adc0

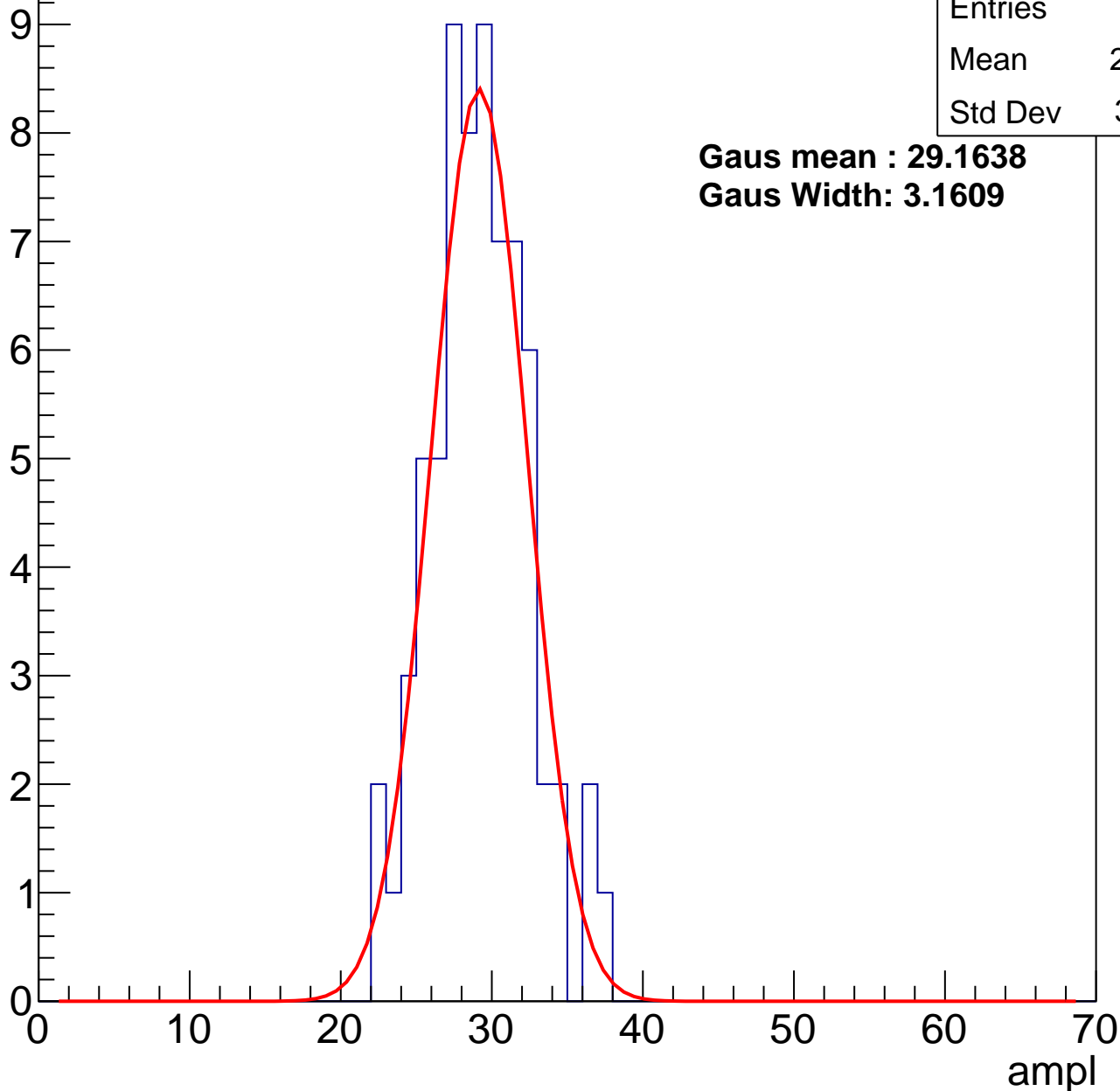
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	28.75
Std Dev	3.201

**Gaus mean : 29.1638**

**Gaus Width: 3.1609**



# B0L001S, U21-ch28, adc1

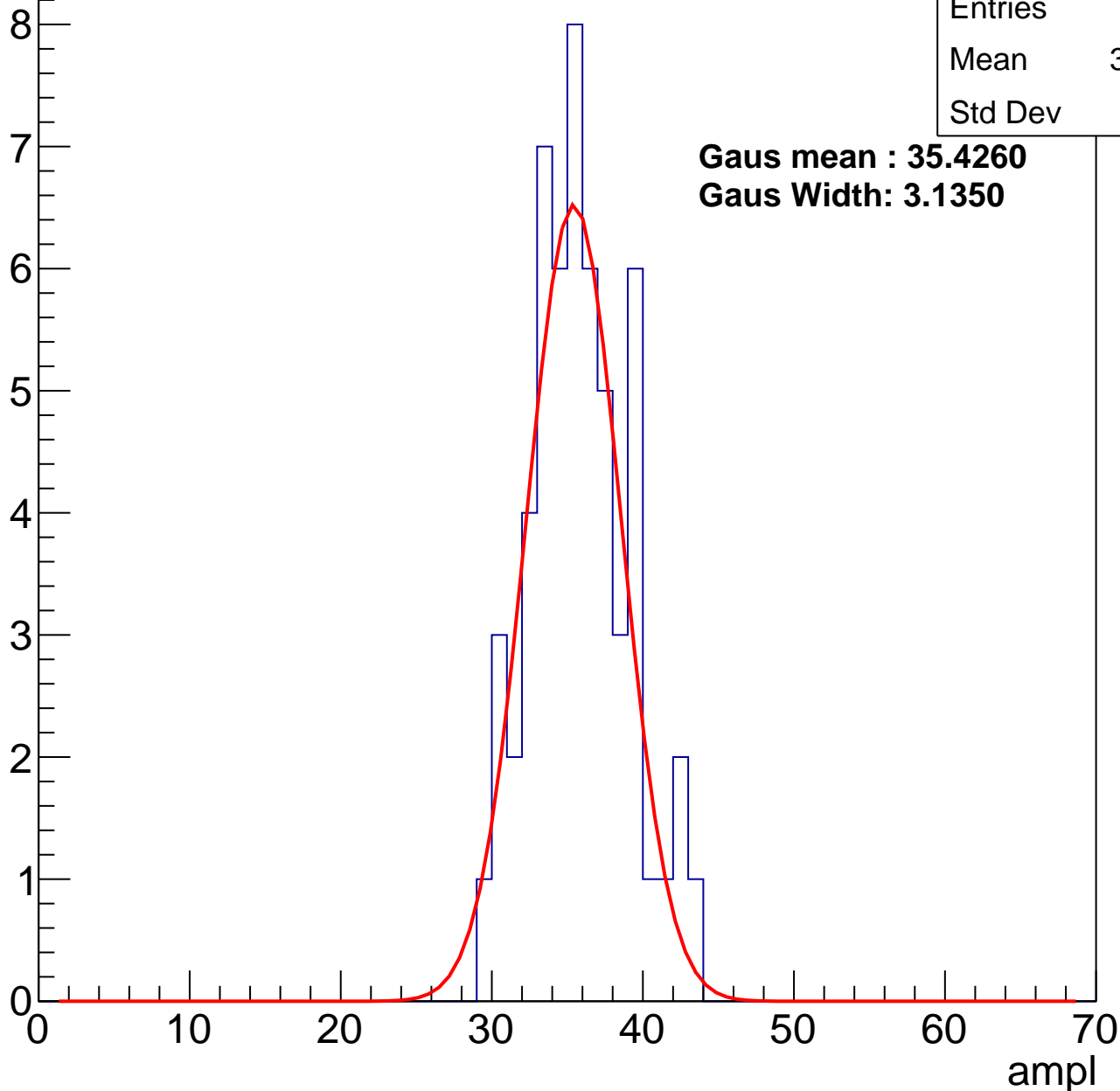
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	35.38
Std Dev	3.21

**Gaus mean : 35.4260**

**Gaus Width: 3.1350**



# B0L001S, U21-ch28, adc2

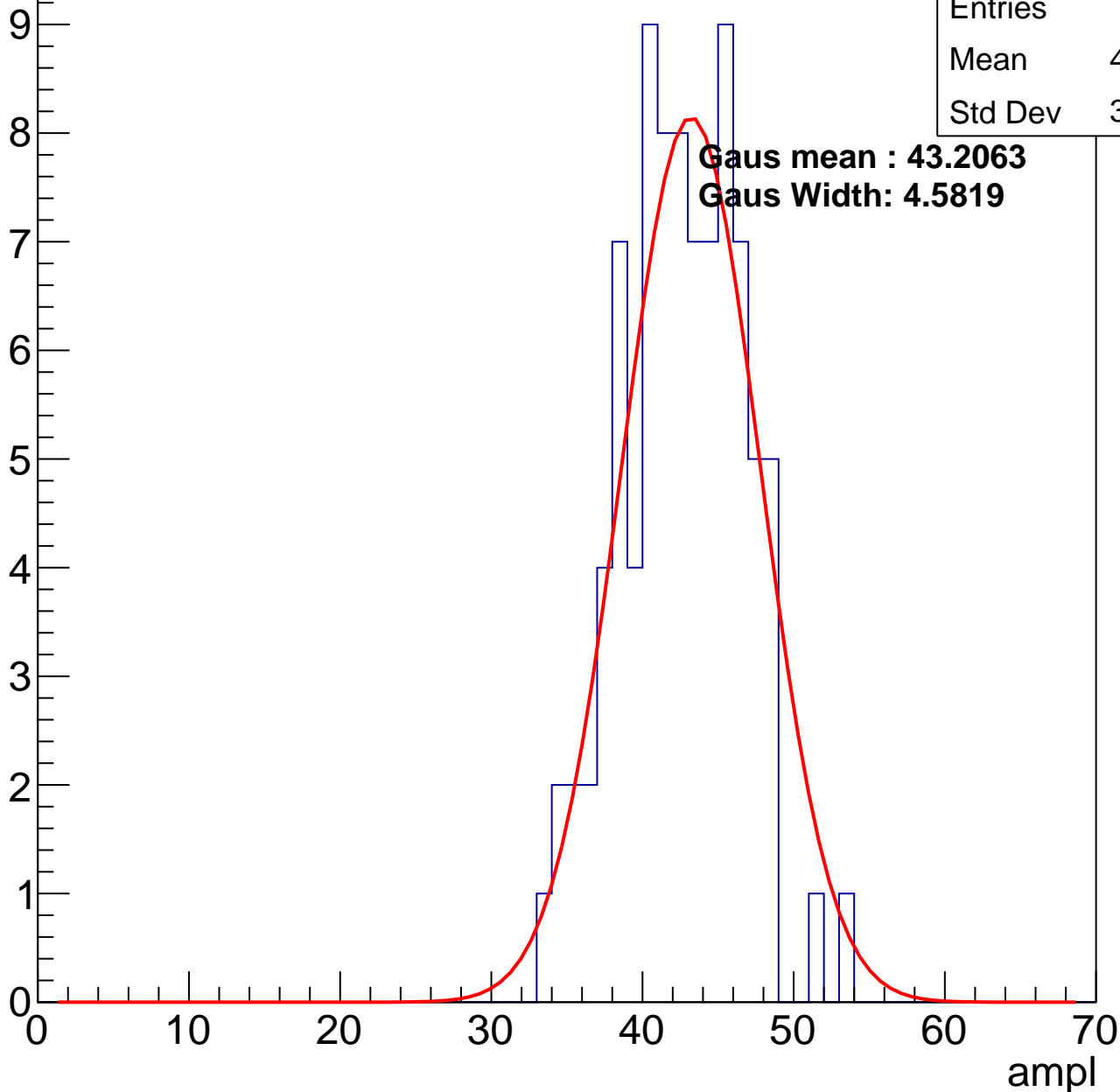
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	89
Mean	42.16
Std Dev	3.972

**Gaus mean : 43.2063**

**Gaus Width: 4.5819**



# B0L001S, U21-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

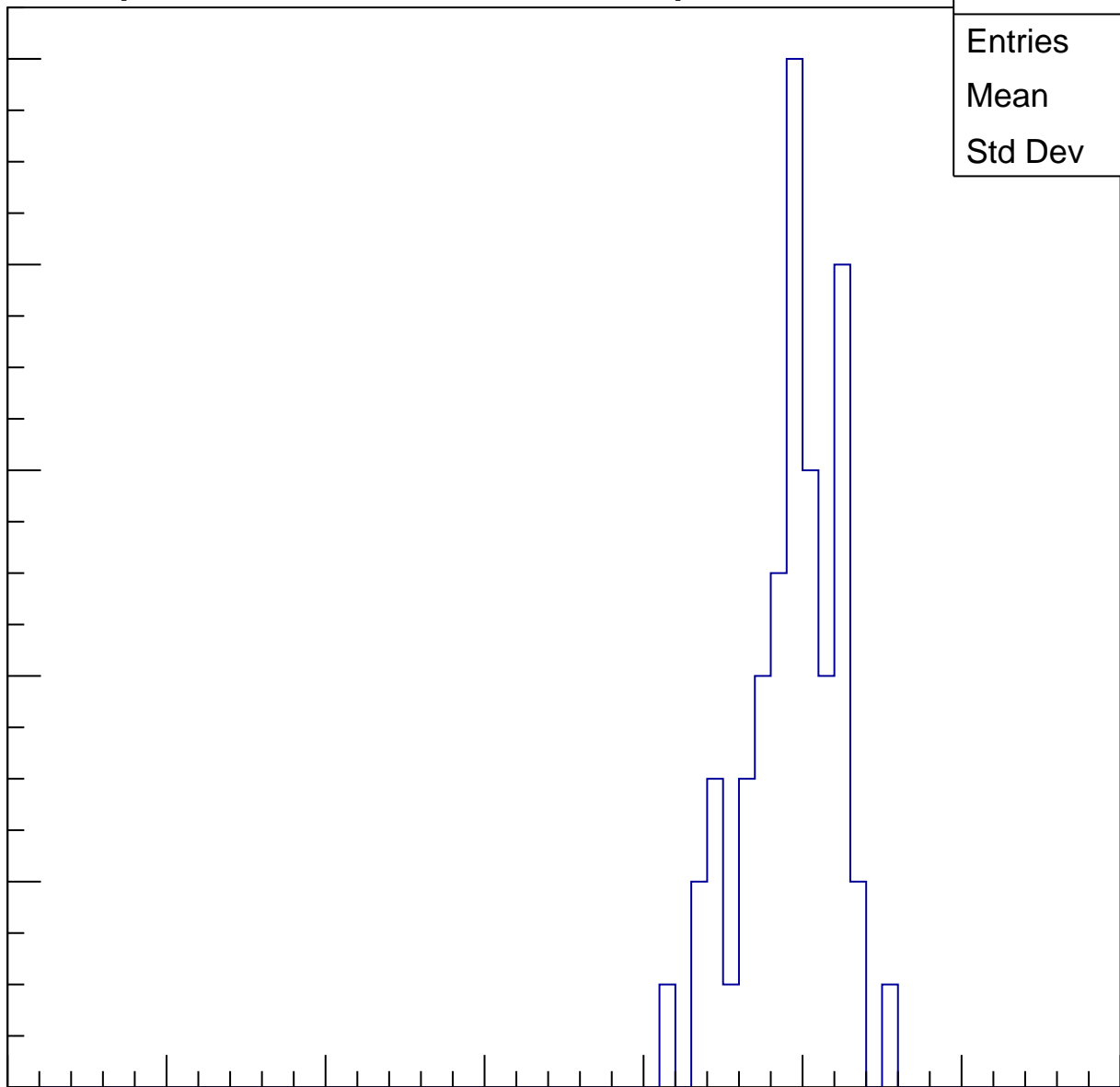
Entries	50
Mean	48.82
Std Dev	2.951

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U21-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	64
Mean	55.31
Std Dev	3.292

Entry

10

8

6

4

2

0

0

10

20

30

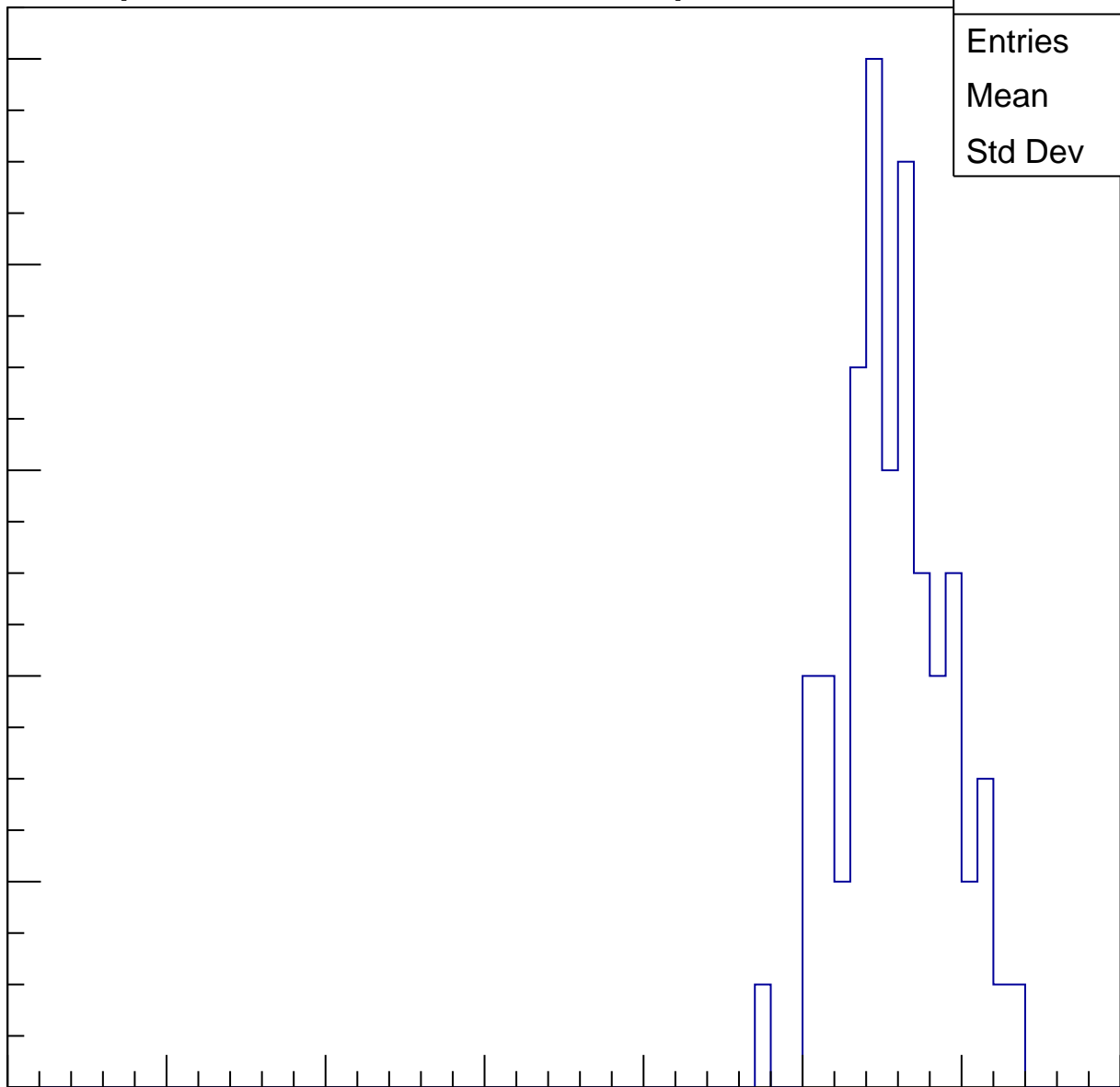
40

50

60

70

ampl

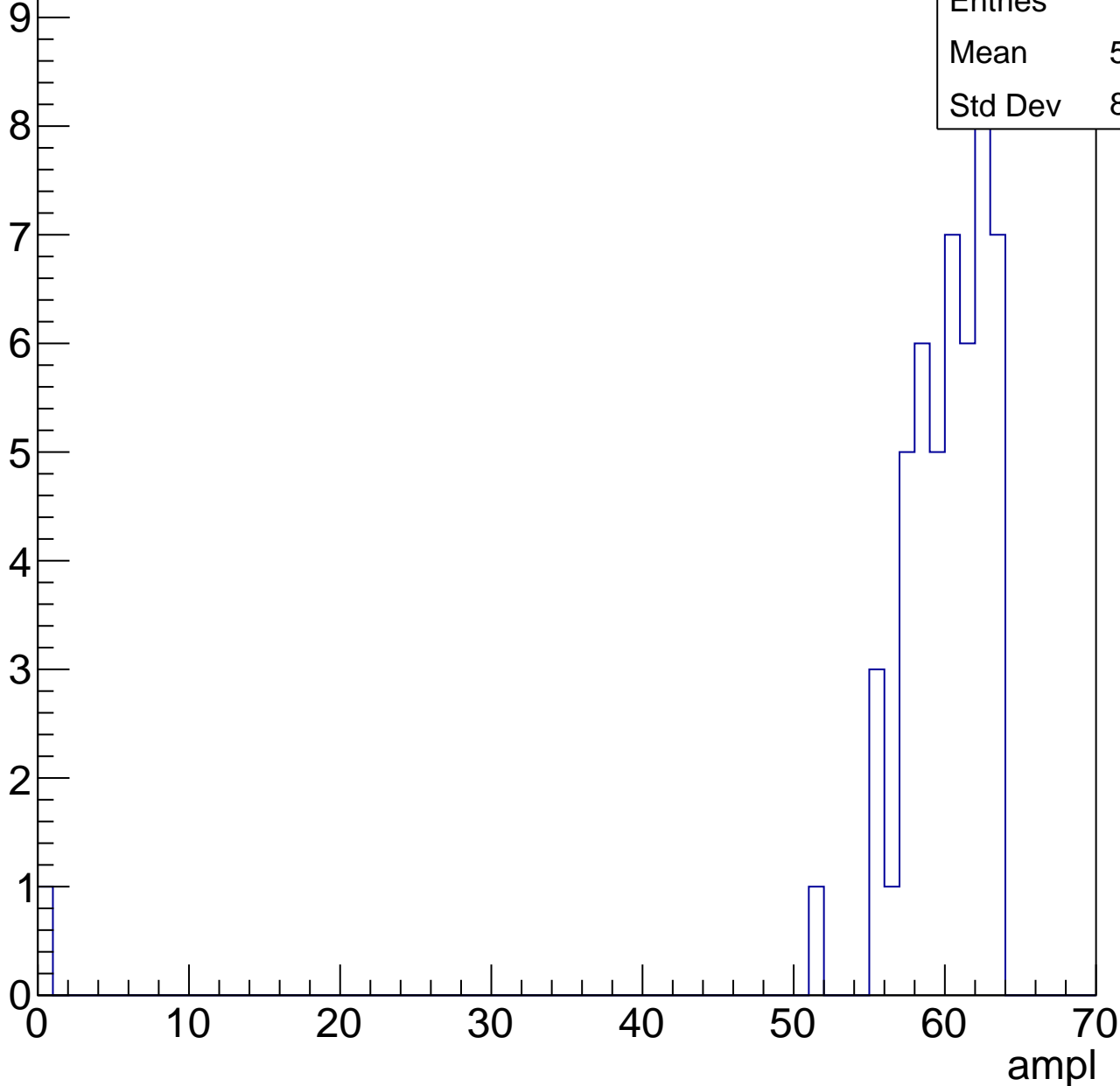


# B0L001S, U21-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	58.53
Std Dev	8.678



# B0L001S, U21-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U21-ch29, adc0

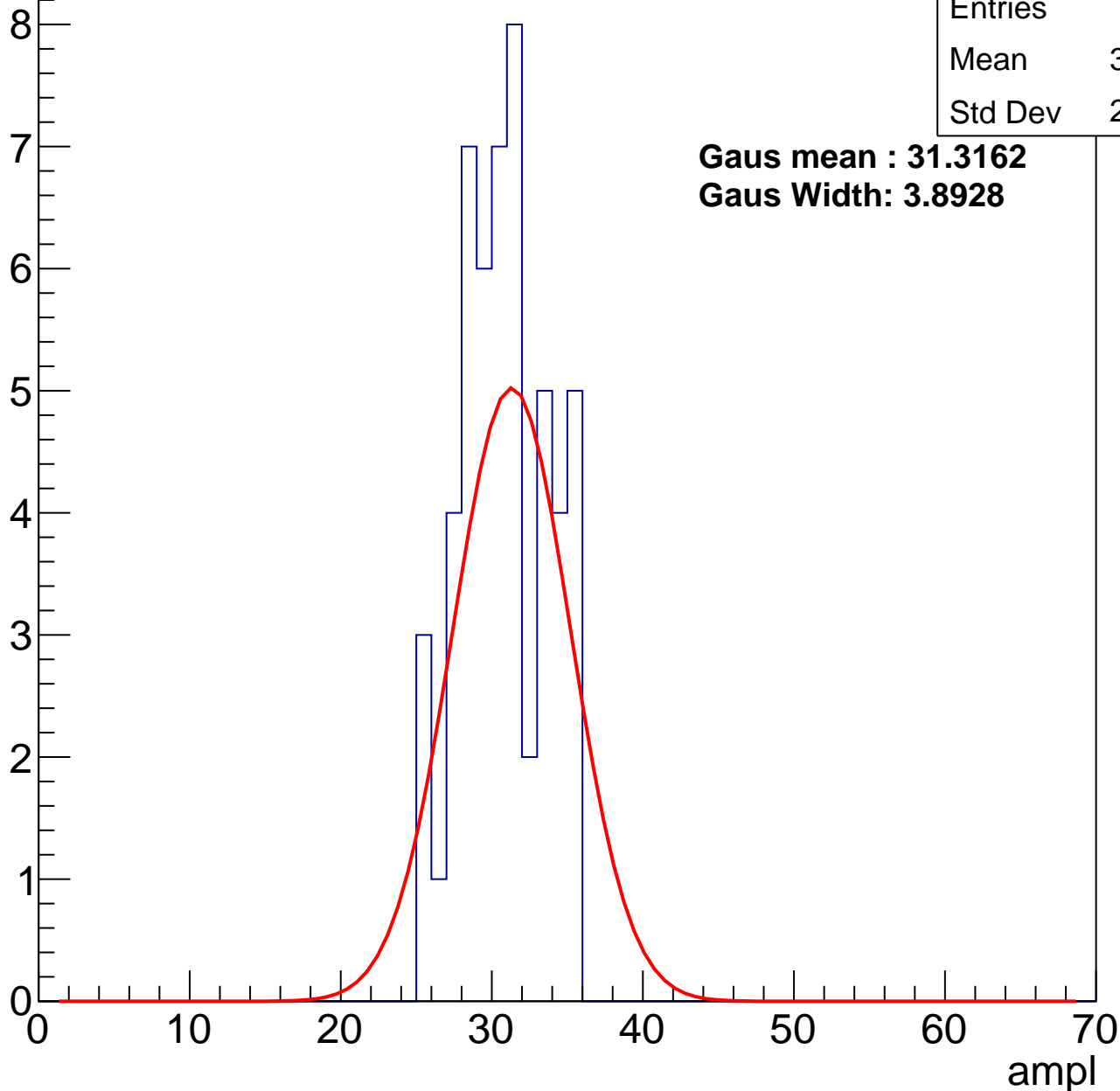
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	30.33
Std Dev	2.792

**Gaus mean : 31.3162**

**Gaus Width: 3.8928**



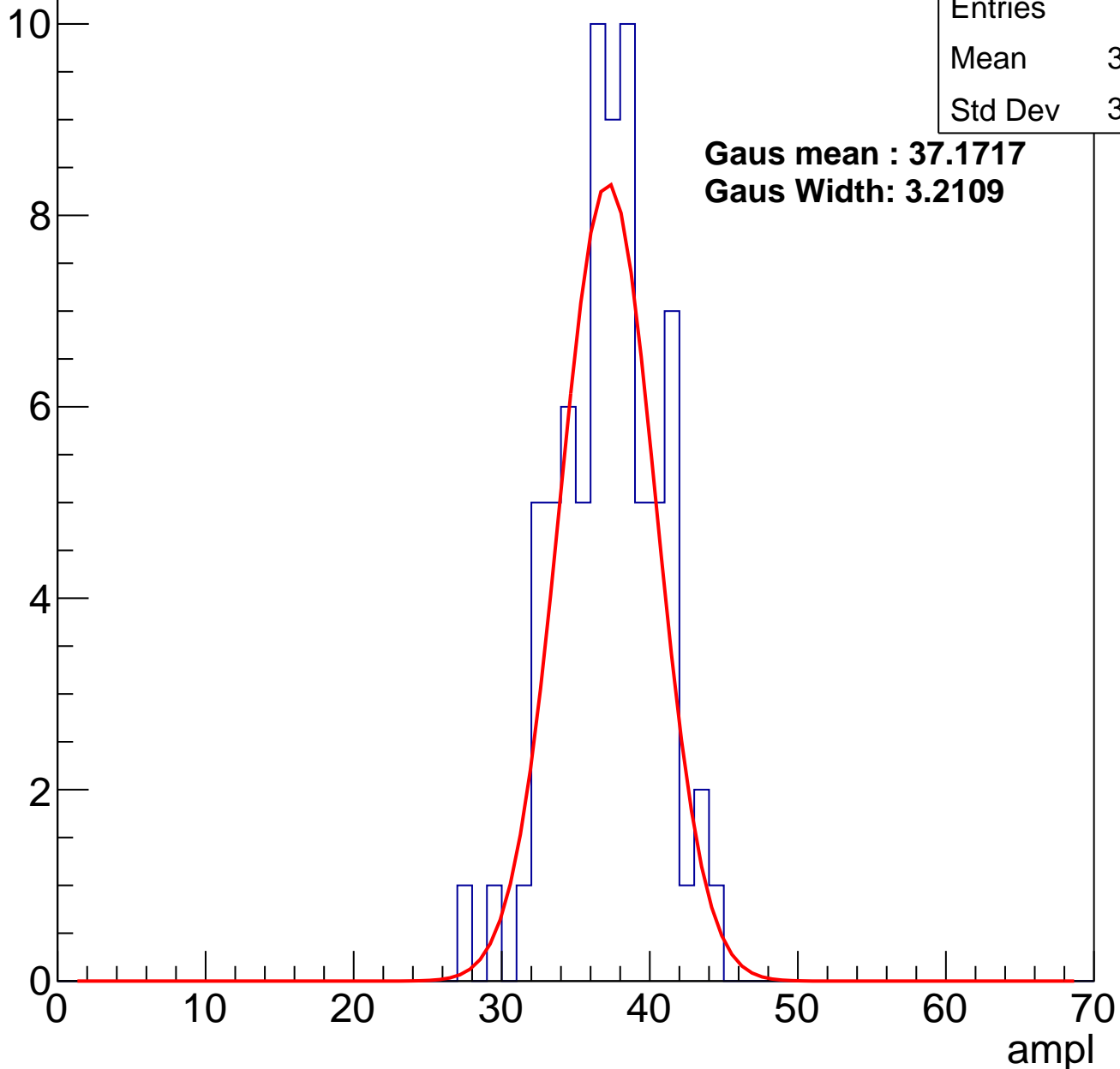
# B0L001S, U21-ch29, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	74
Mean	36.73
Std Dev	3.322

**Gaus mean : 37.1717**  
**Gaus Width: 3.2109**

Entry



# B0L001S, U21-ch29, adc2

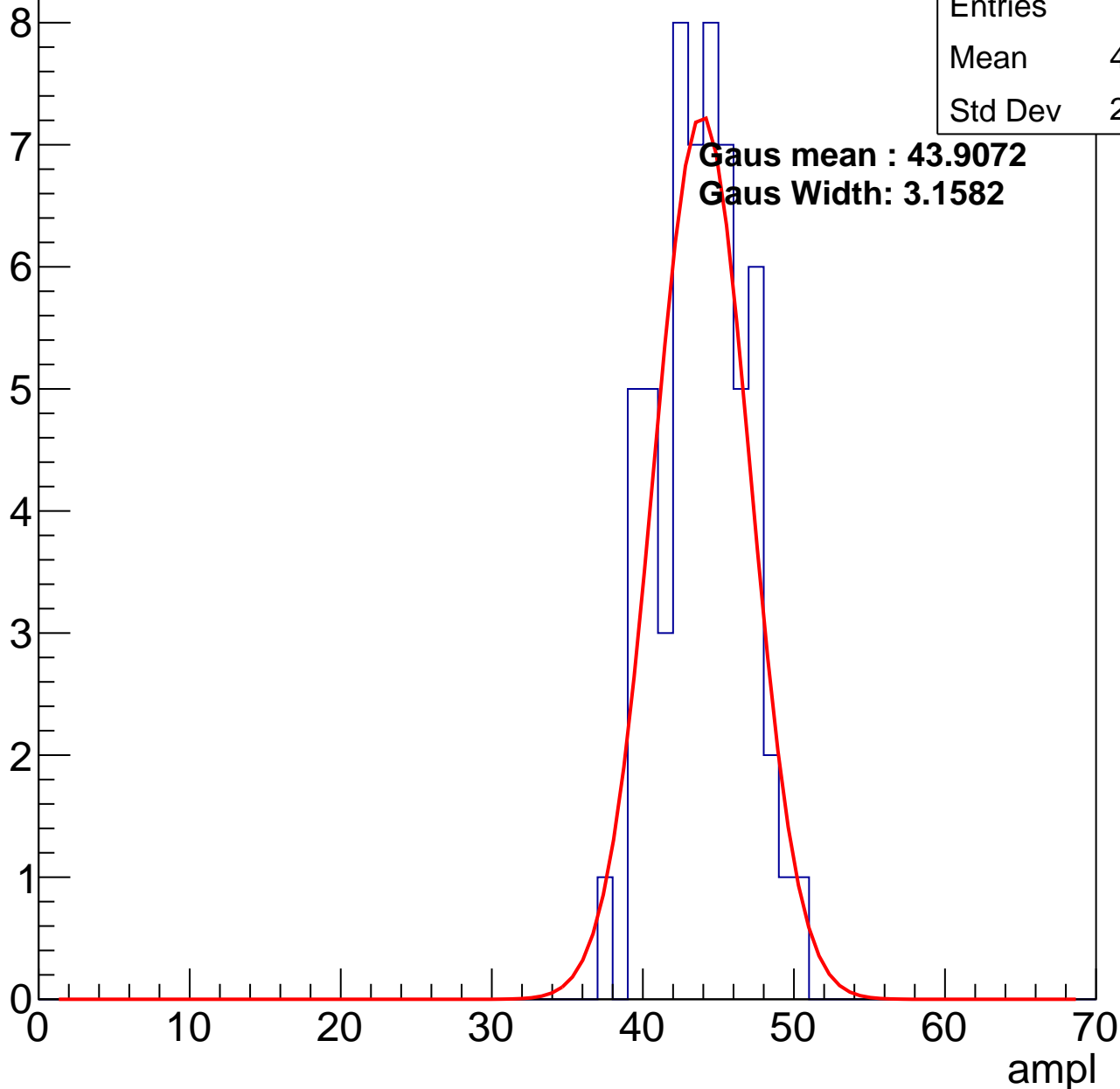
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	43.49
Std Dev	2.849

**Gaus mean : 43.9072**

**Gaus Width: 3.1582**

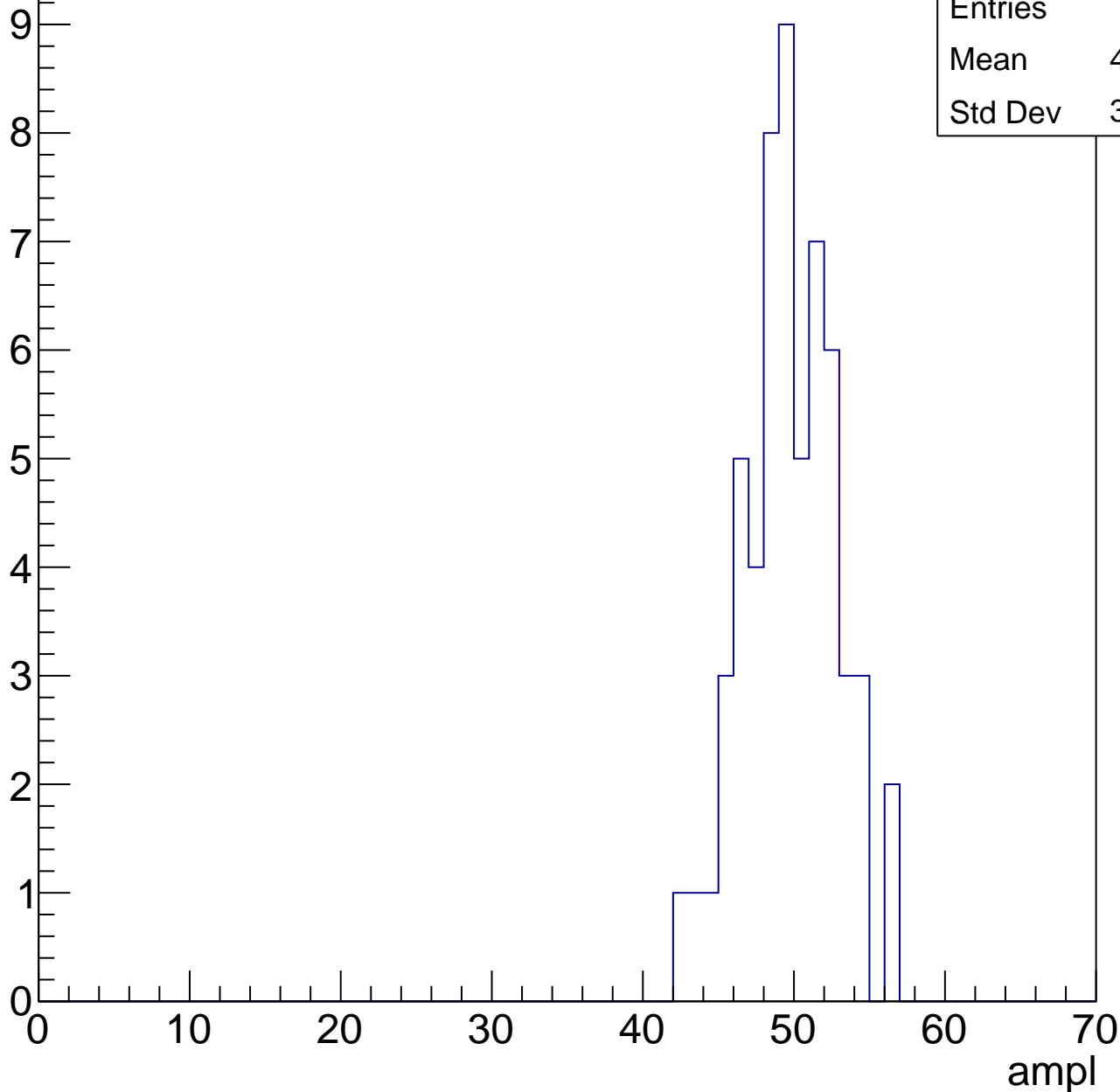


# B0L001S, U21-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

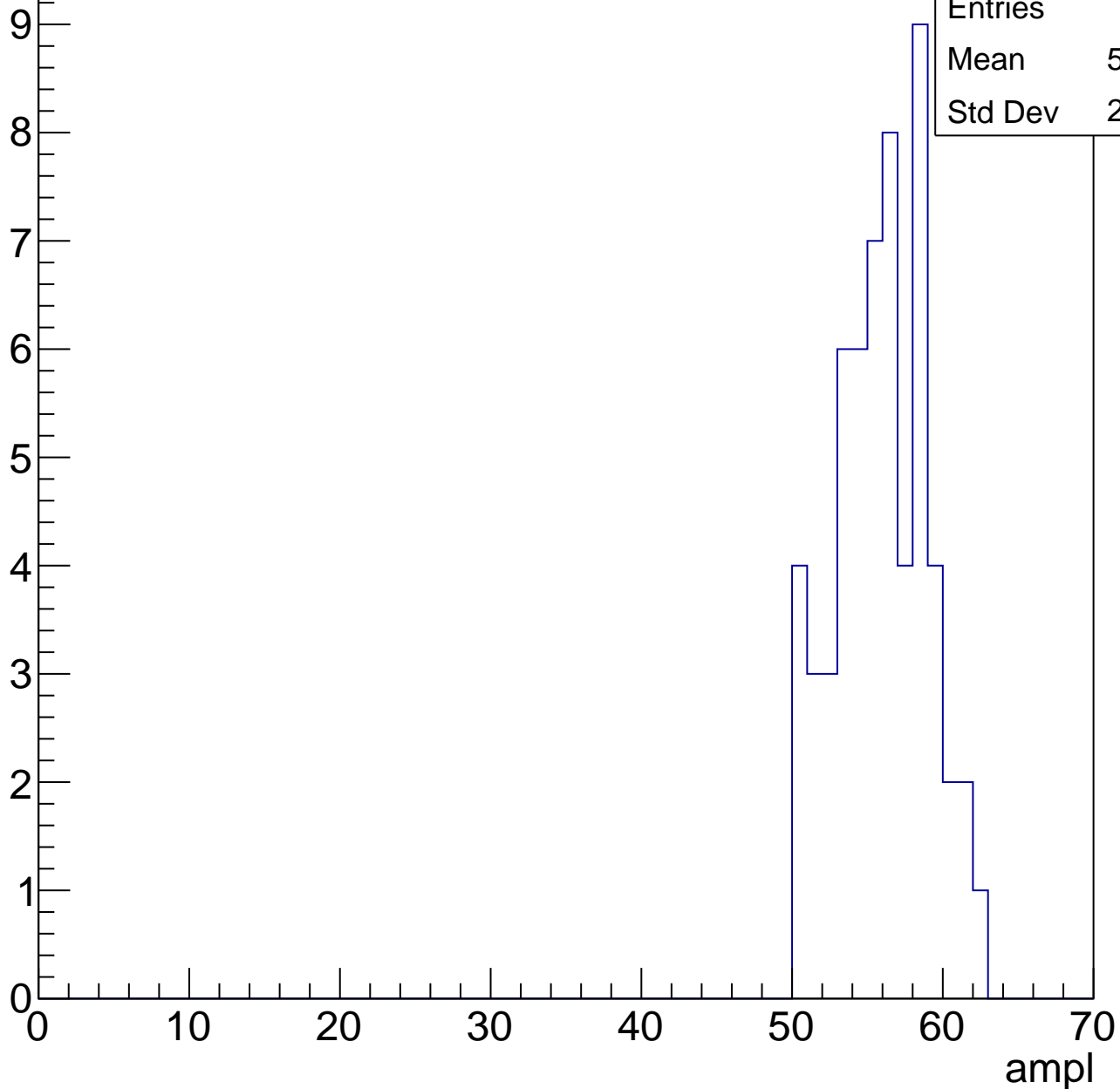
Entries	58
Mean	49.29
Std Dev	3.023



# B0L001S, U21-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

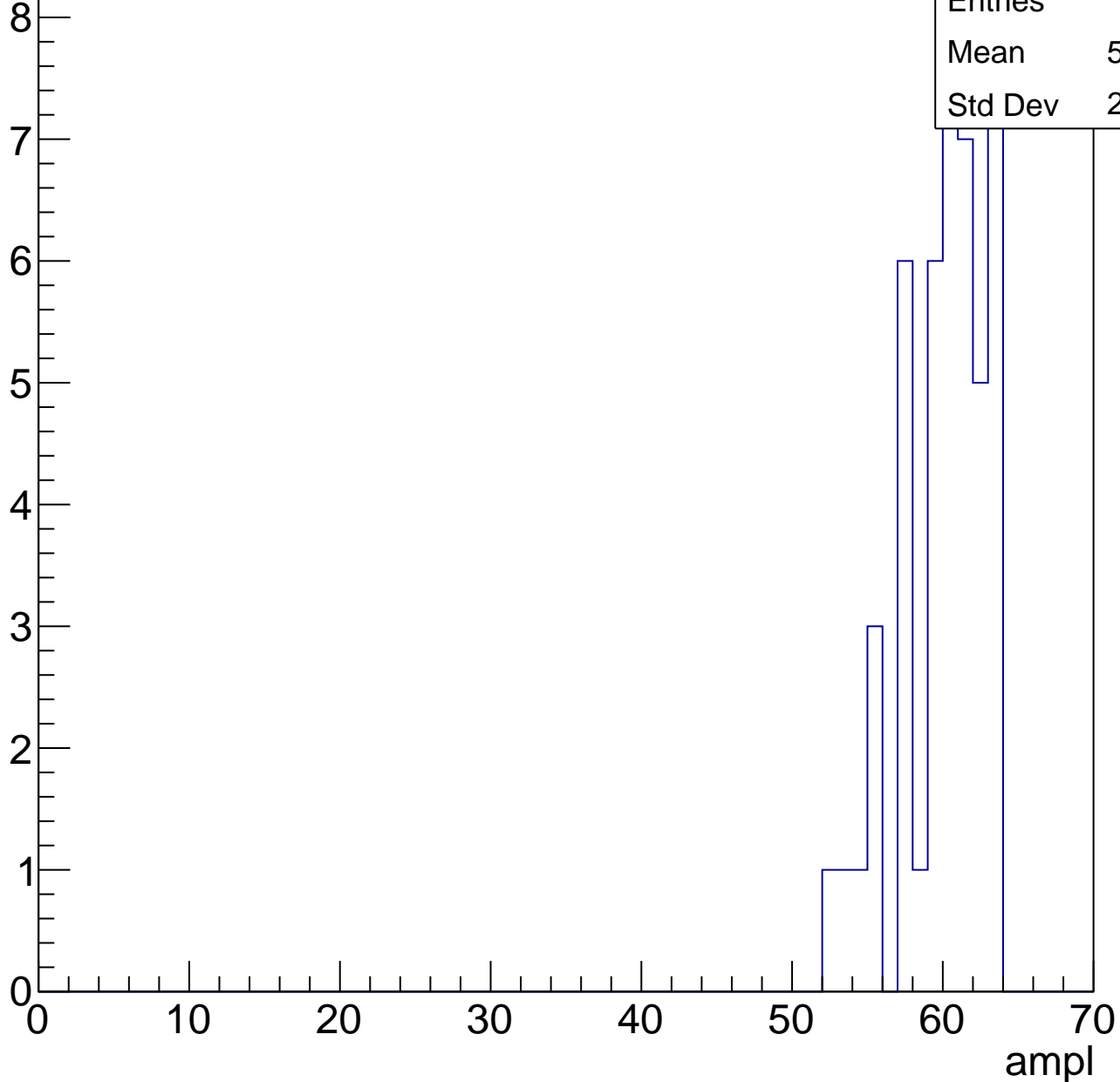
Entry



# B0L001S, U21-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

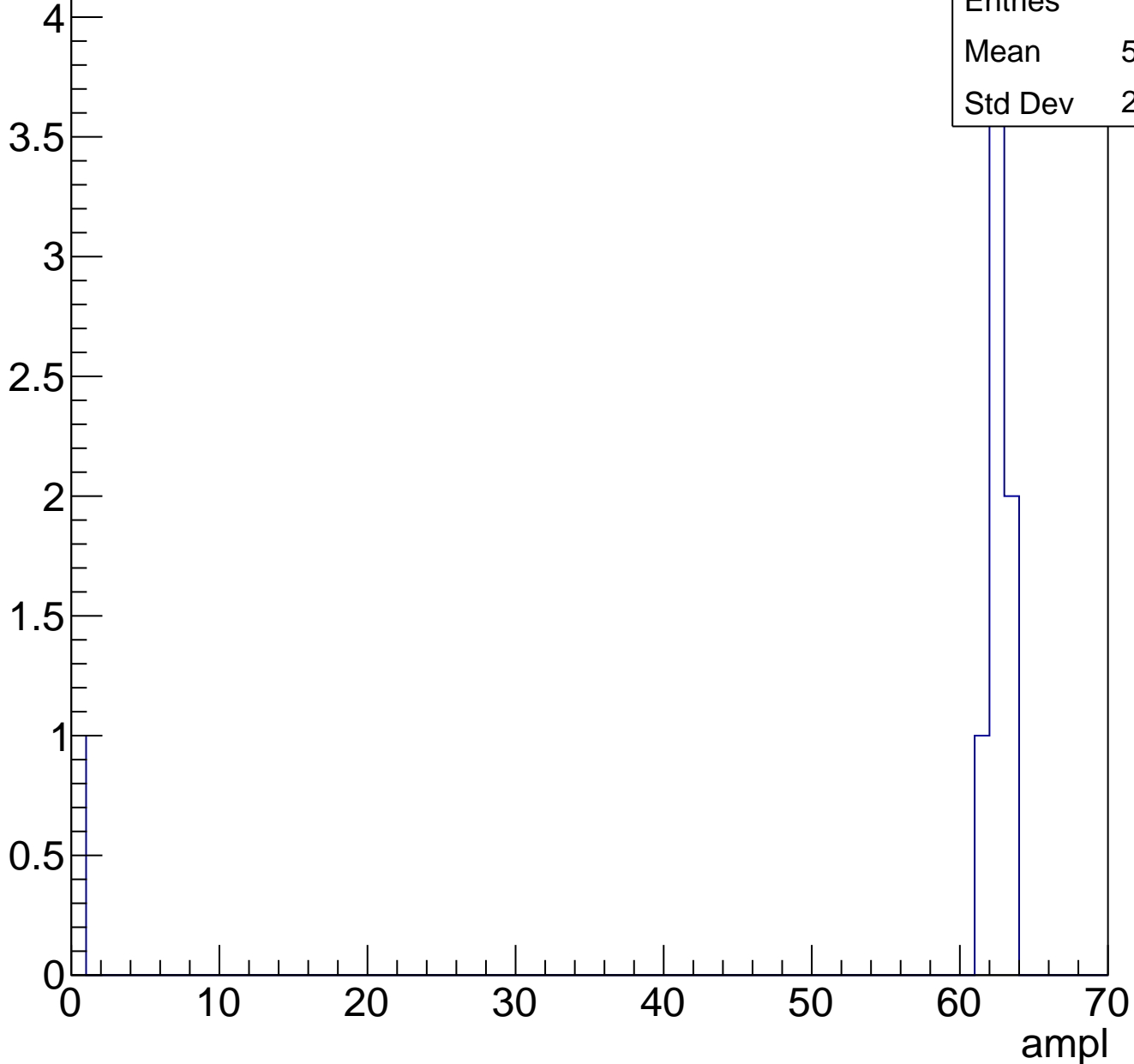
Entry



# B0L001S, U21-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	8
Mean	54.38
Std Dev	20.56



# B0L001S, U21-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch30, adc0

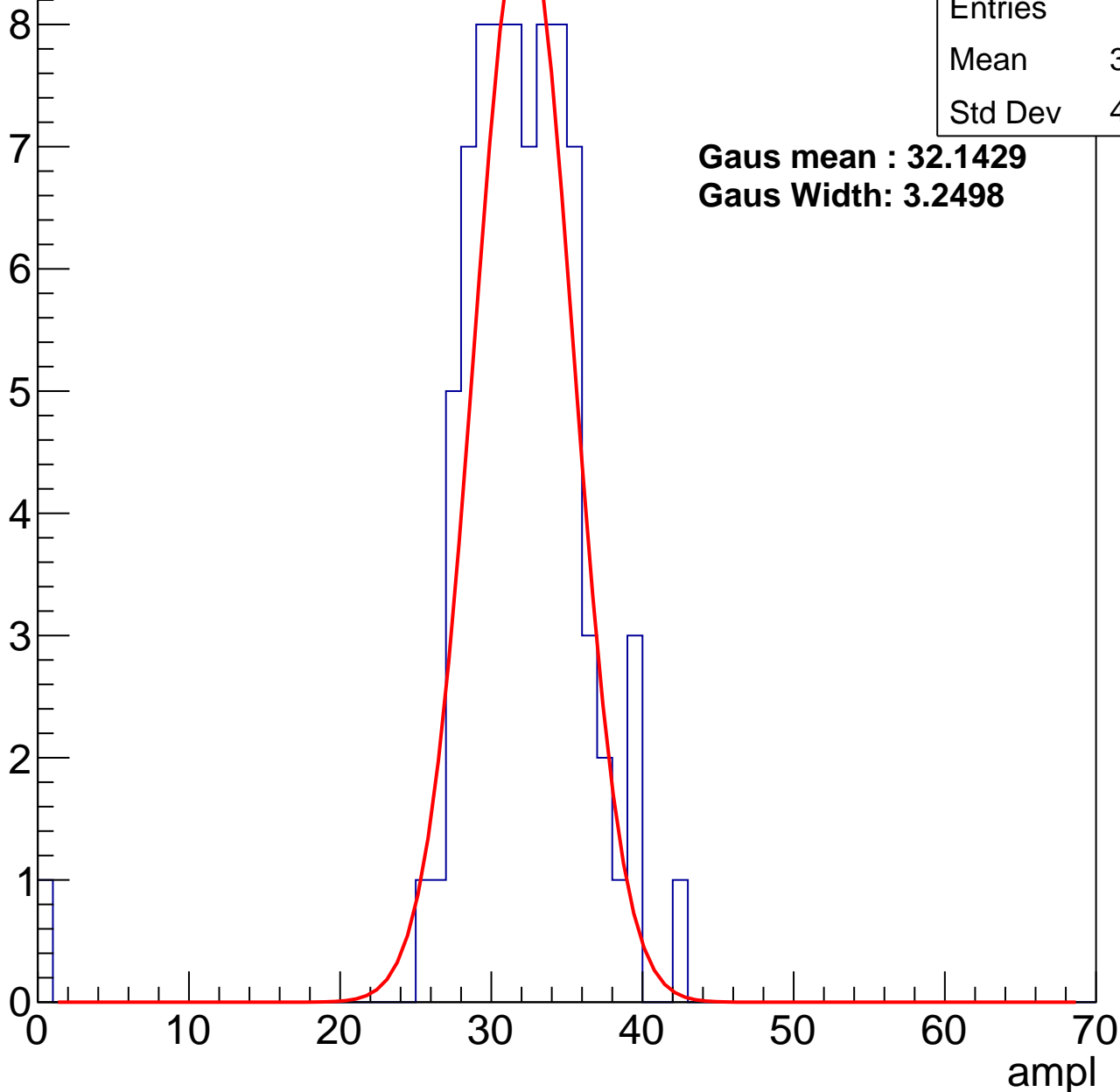
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	31.47
Std Dev	4.929

**Gaus mean : 32.1429**

**Gaus Width: 3.2498**



# B0L001S, U21-ch30, adc1

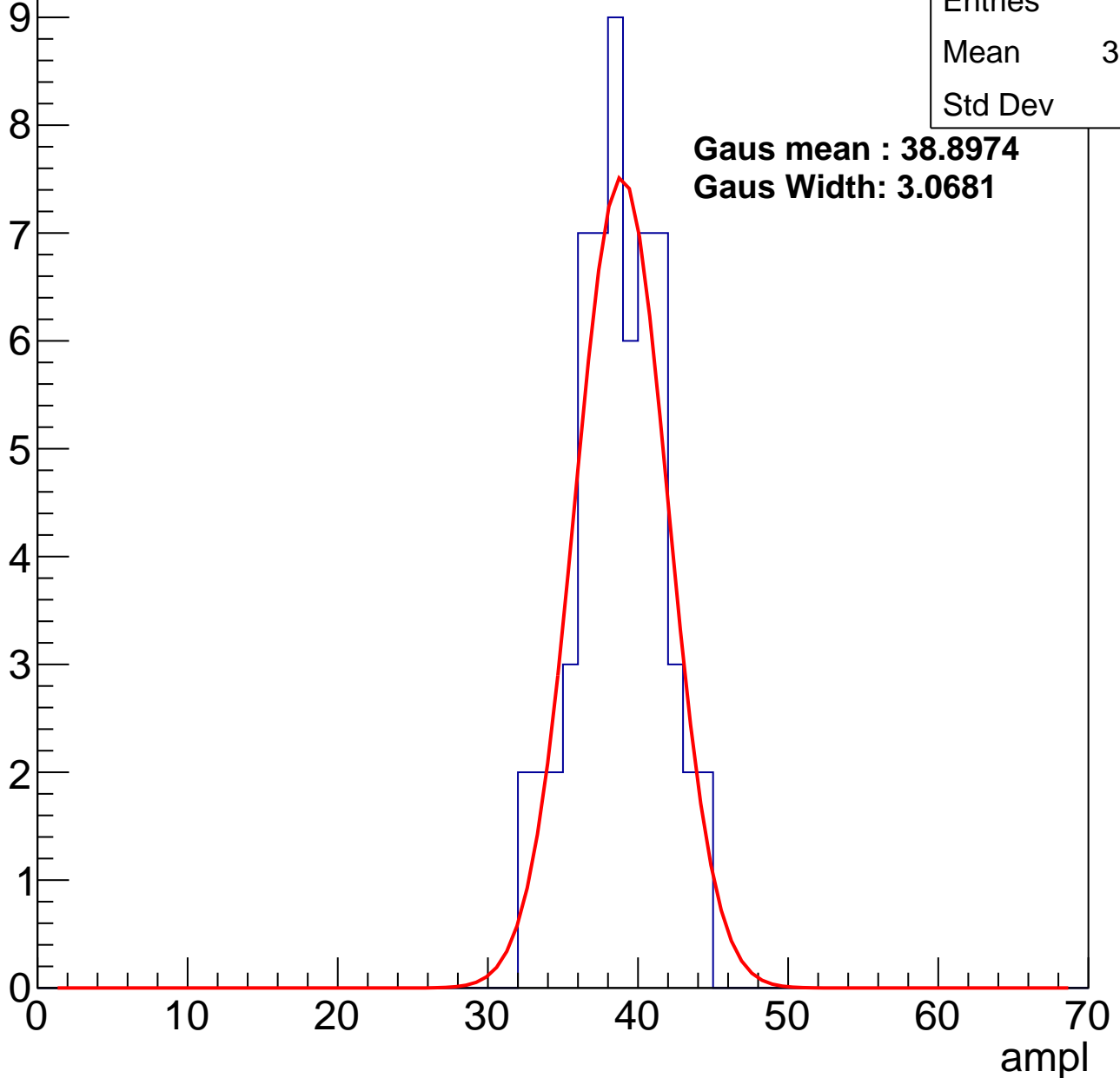
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	38.25
Std Dev	2.85

**Gaus mean : 38.8974**

**Gaus Width: 3.0681**



# B0L001S, U21-ch30, adc2

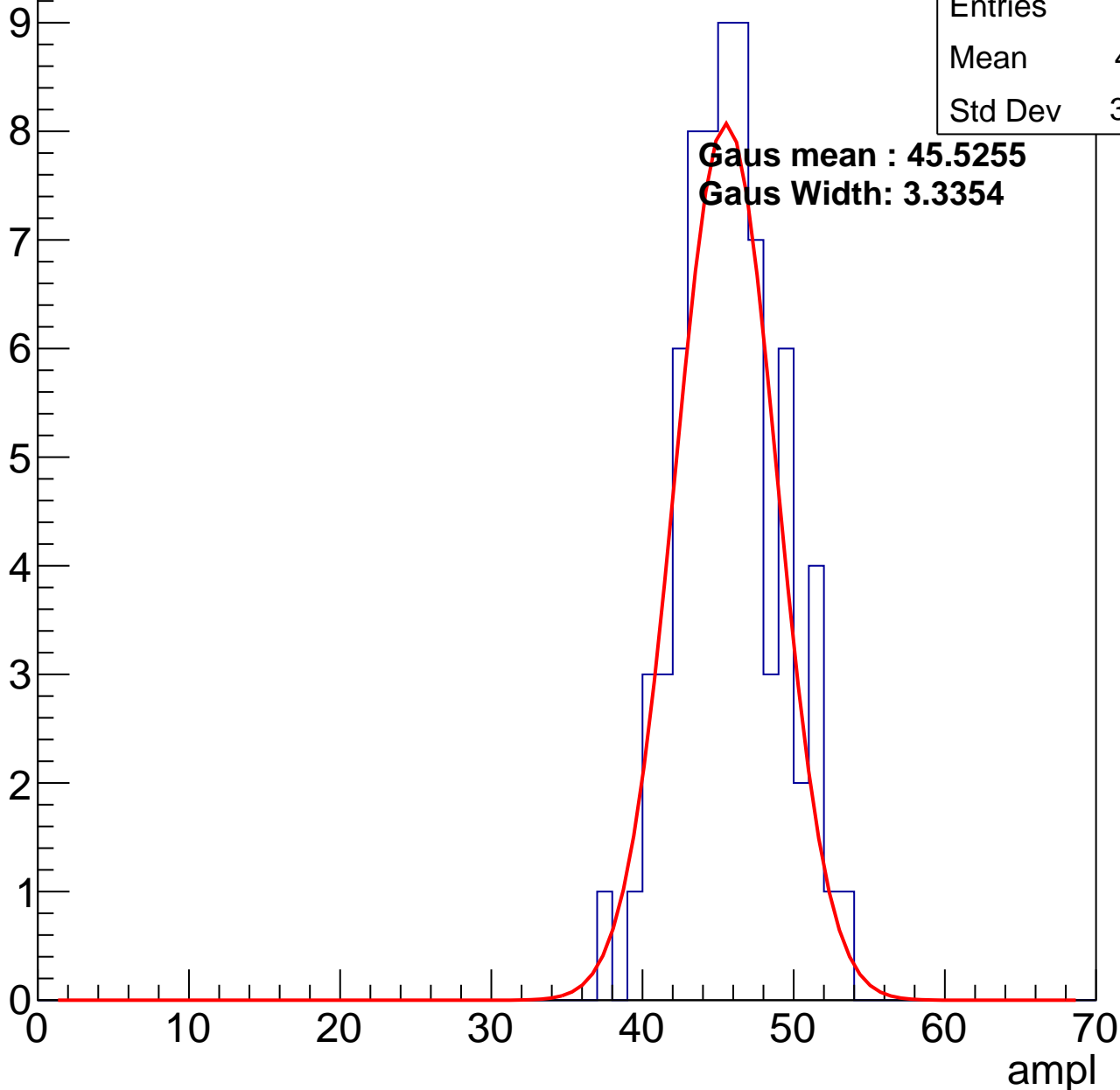
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	45.31
Std Dev	3.286

**Gaus mean : 45.5255**

**Gaus Width: 3.3354**

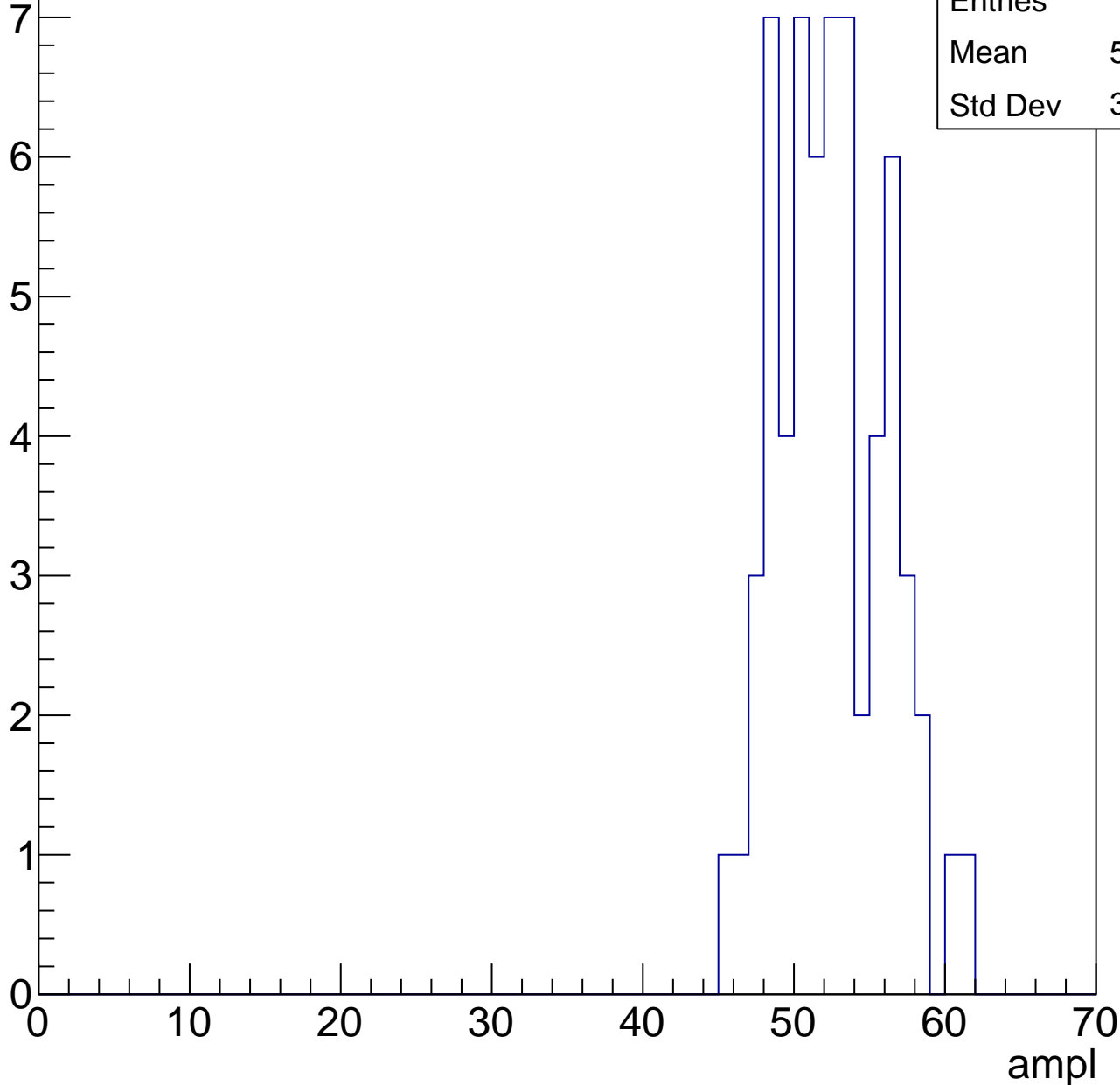


# B0L001S, U21-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	52.05
Std Dev	3.549

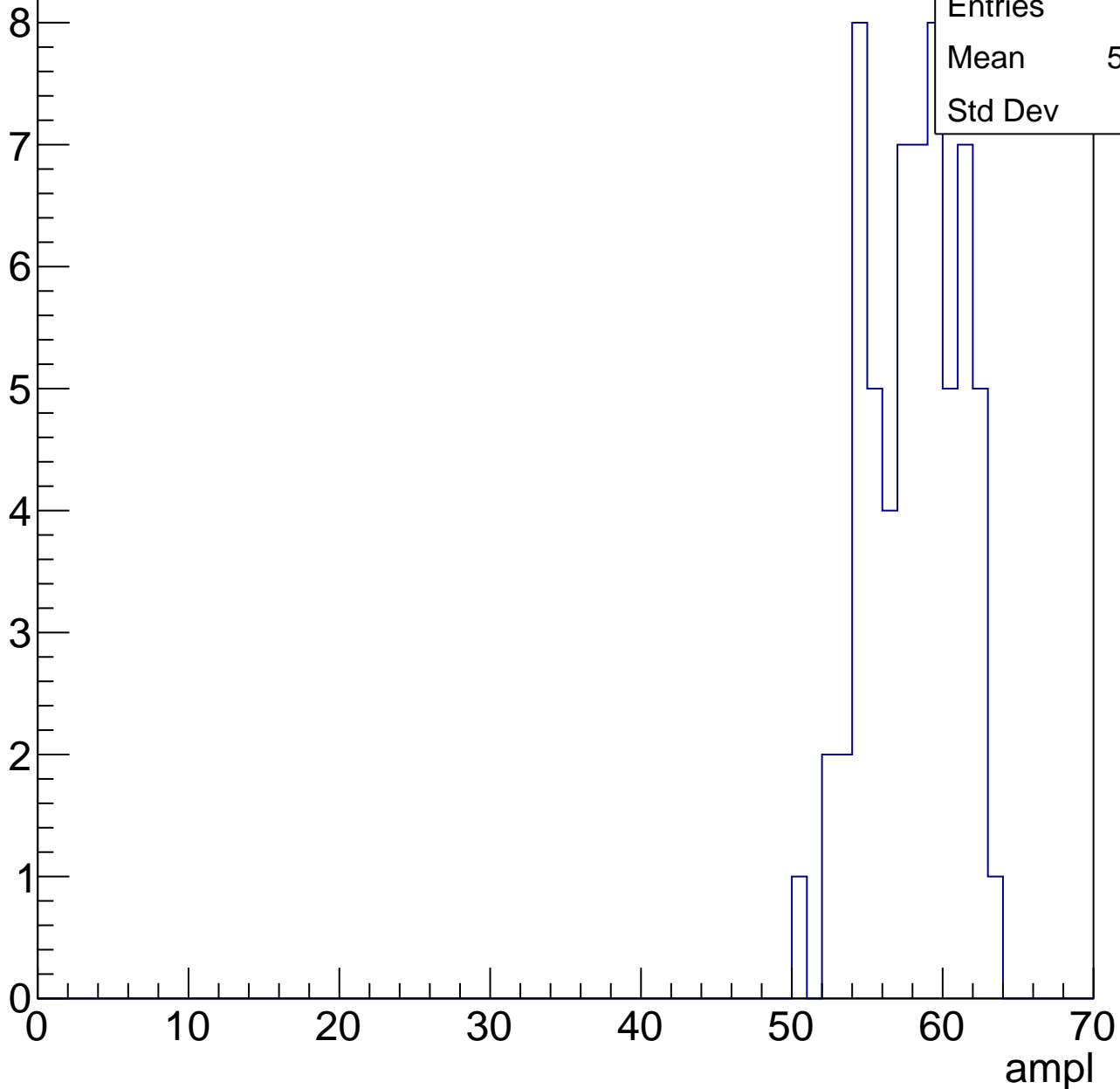


# B0L001S, U21-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	57.55
Std Dev	3.02

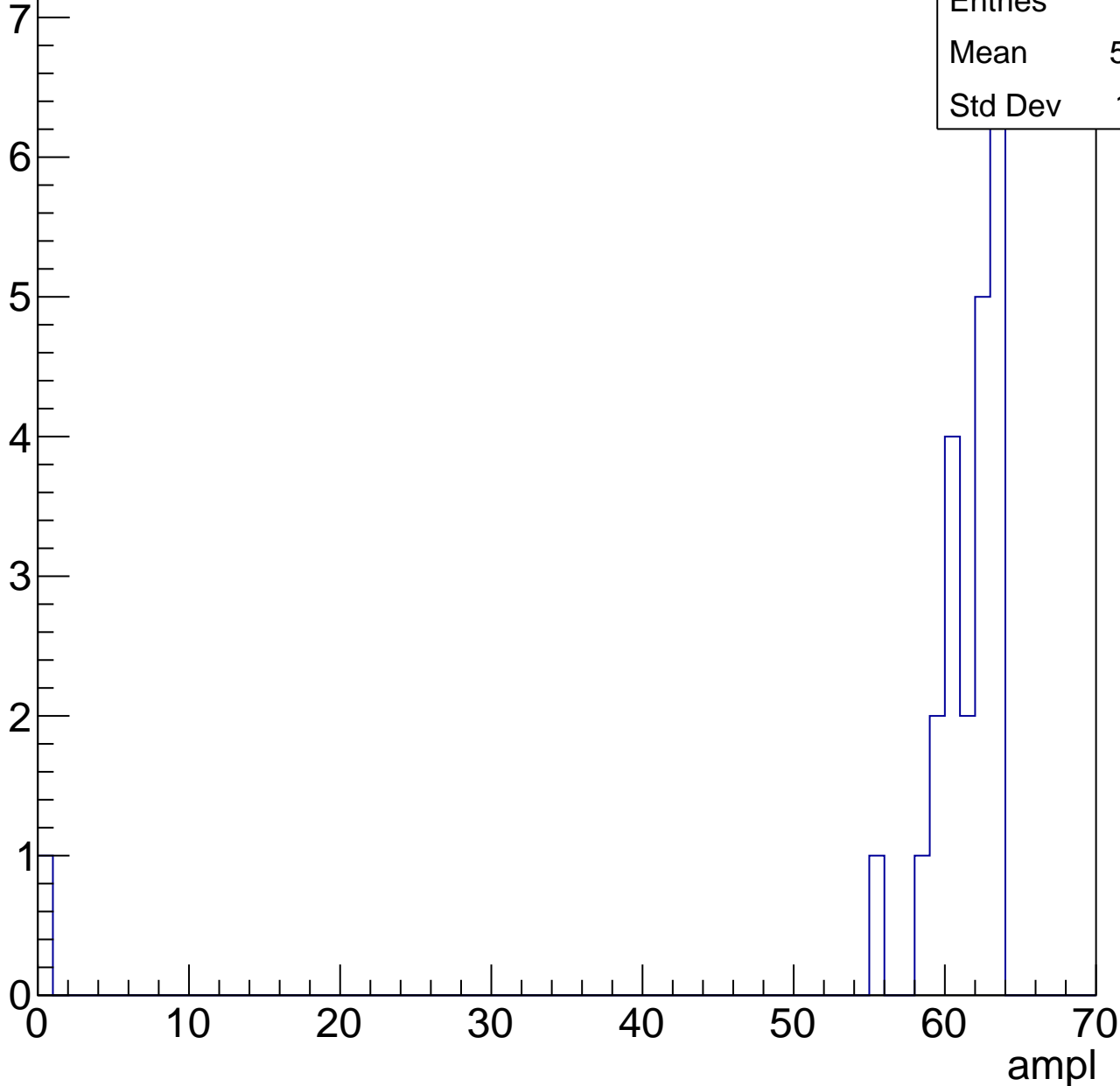


# B0L001S, U21-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	23
Mean	58.43
Std Dev	12.61



# B0L001S, U21-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch31, adc0

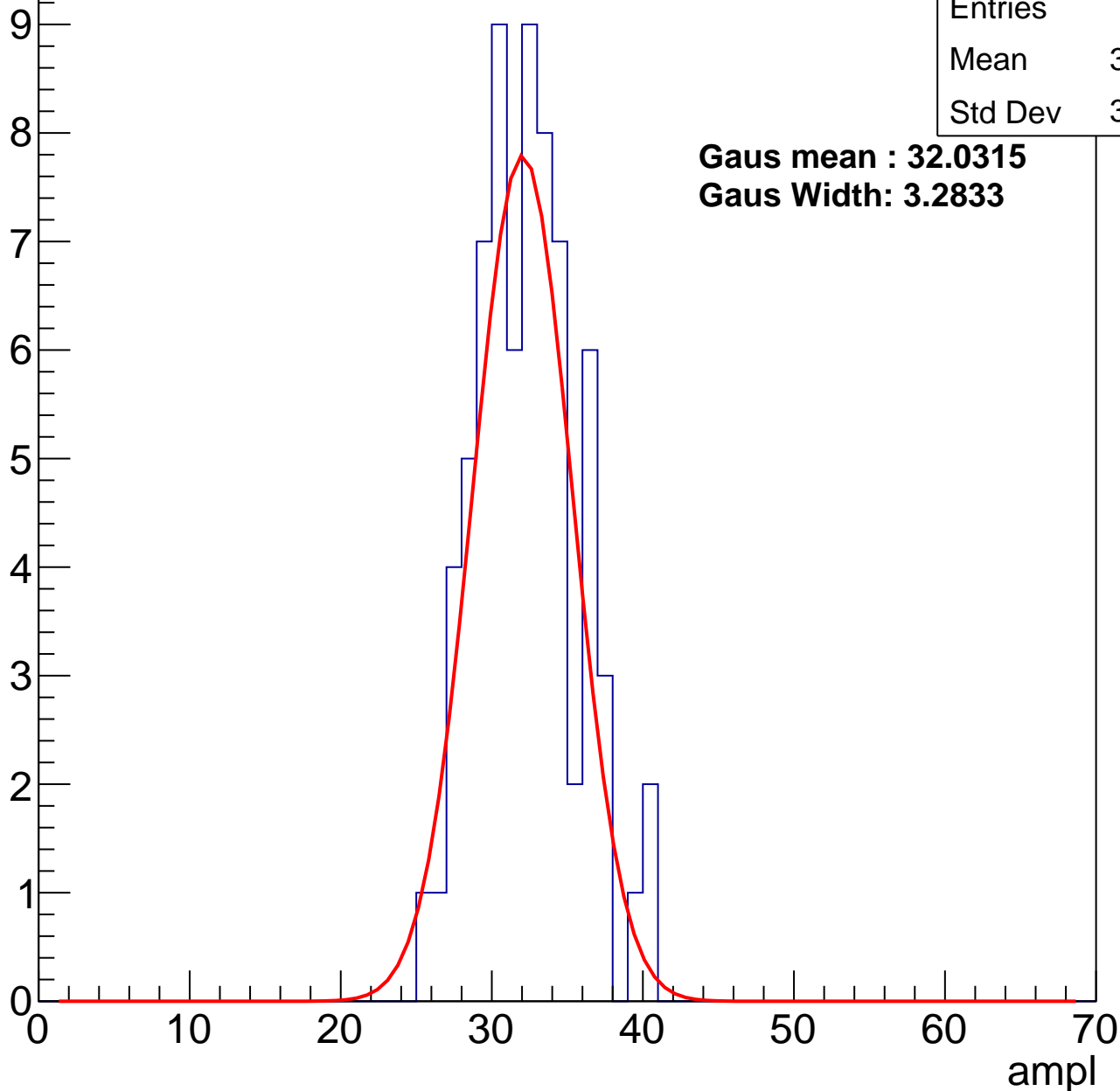
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	31.89
Std Dev	3.296

**Gaus mean : 32.0315**

**Gaus Width: 3.2833**



# B0L001S, U21-ch31, adc1

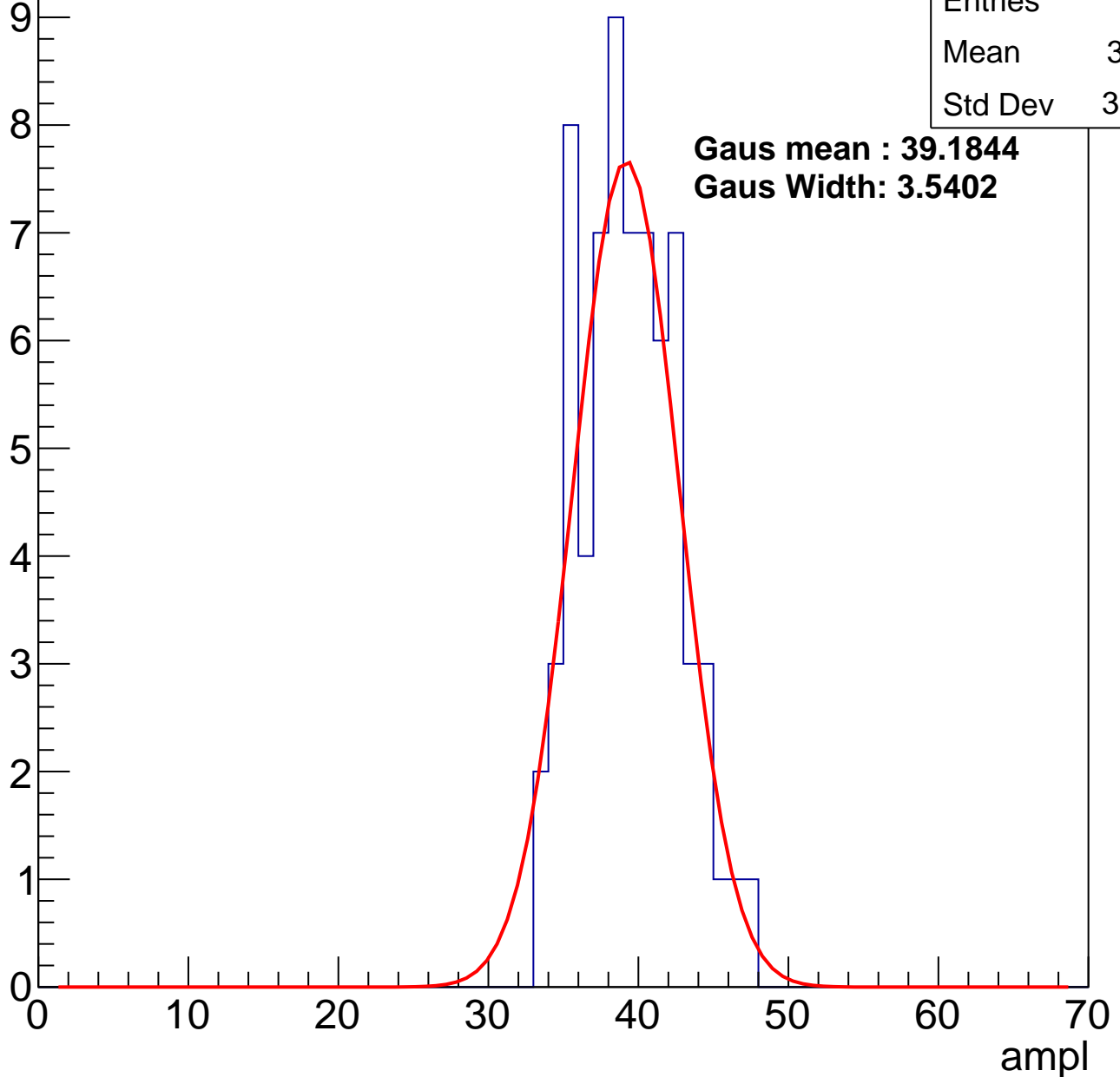
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	38.91
Std Dev	3.216

**Gaus mean : 39.1844**

**Gaus Width: 3.5402**



# B0L001S, U21-ch31, adc2

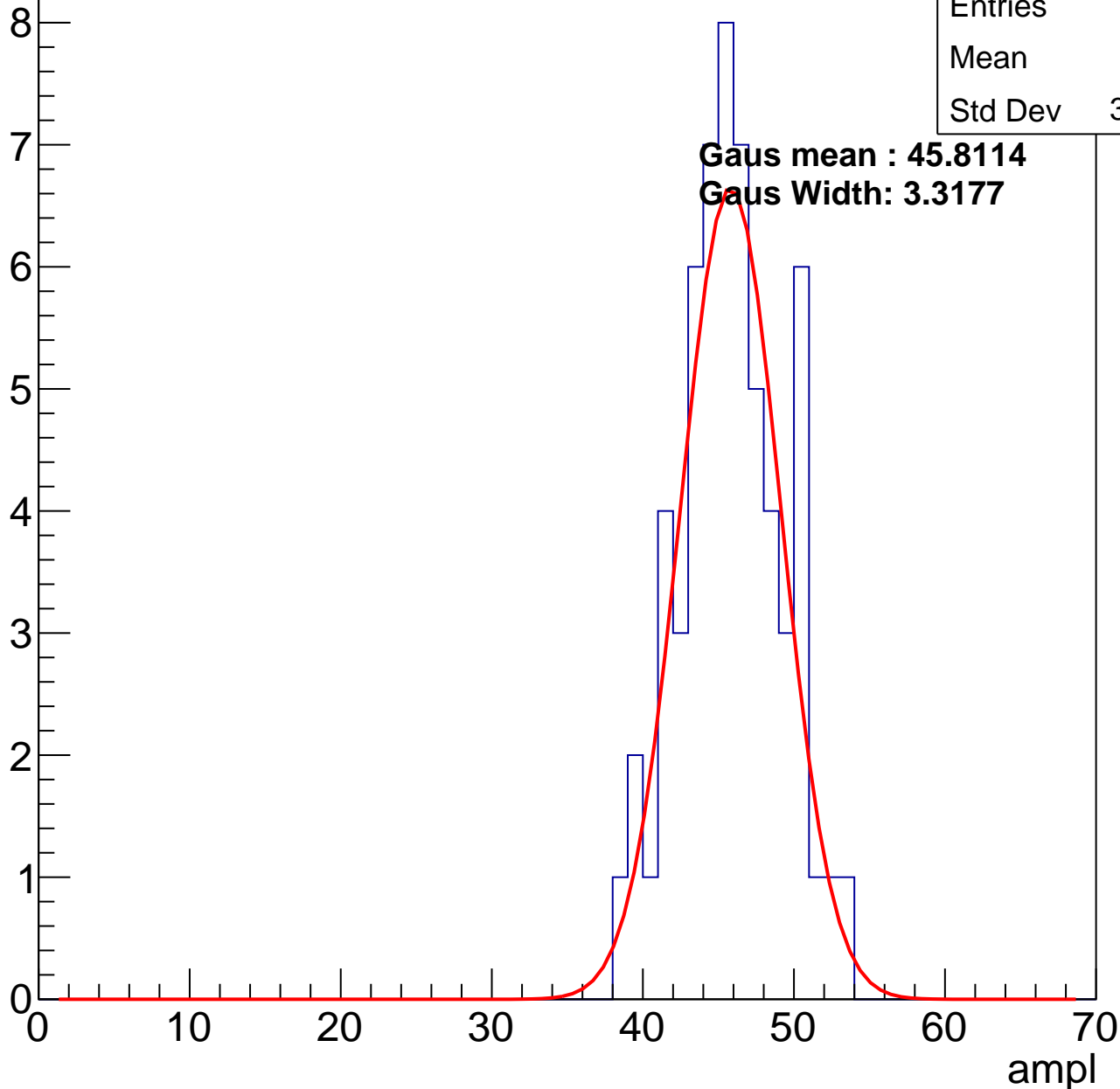
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	45.4
Std Dev	3.338

Gaus mean : 45.8114

Gaus Width: 3.3177

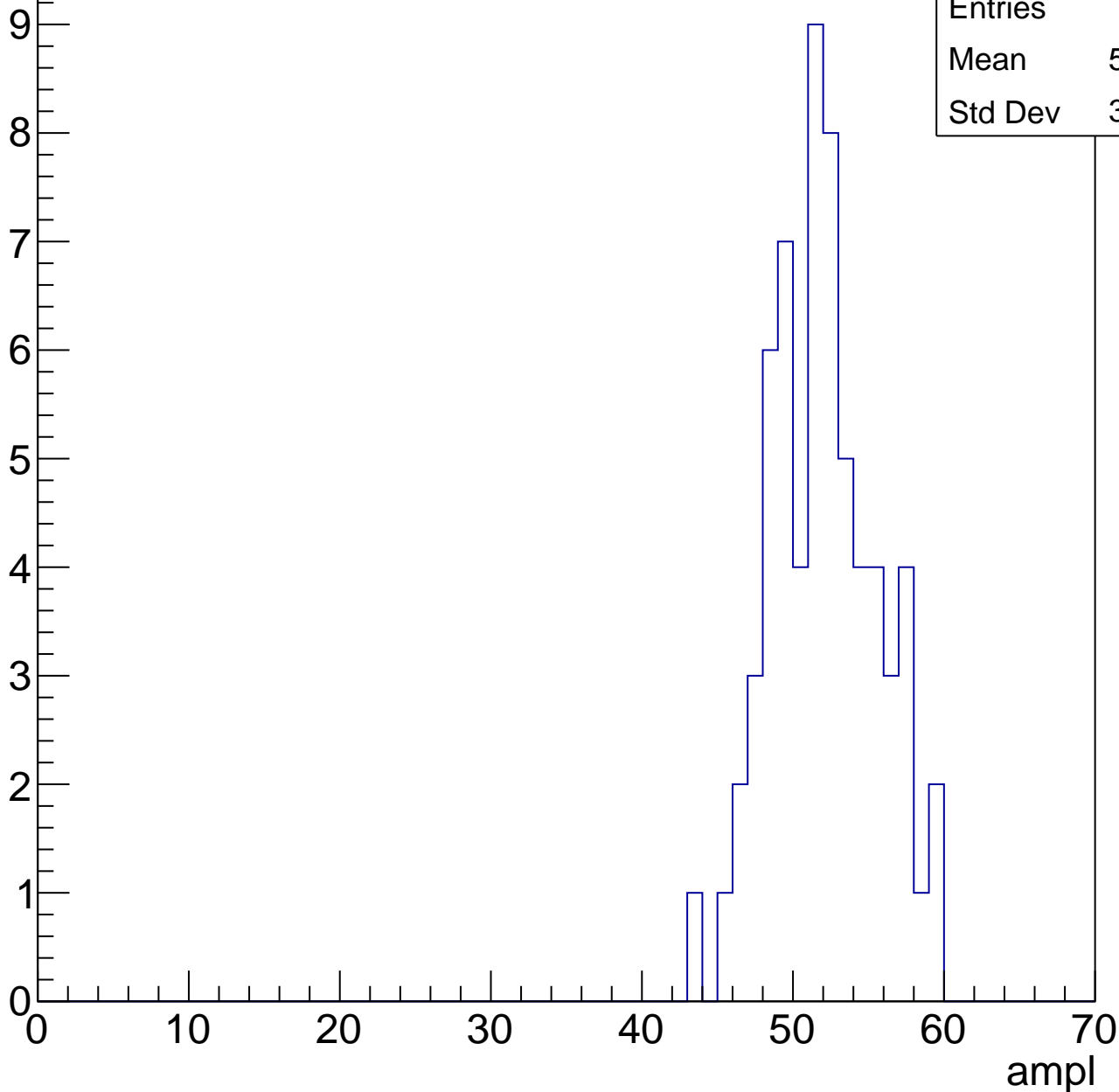


# B0L001S, U21-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	51.56
Std Dev	3.508

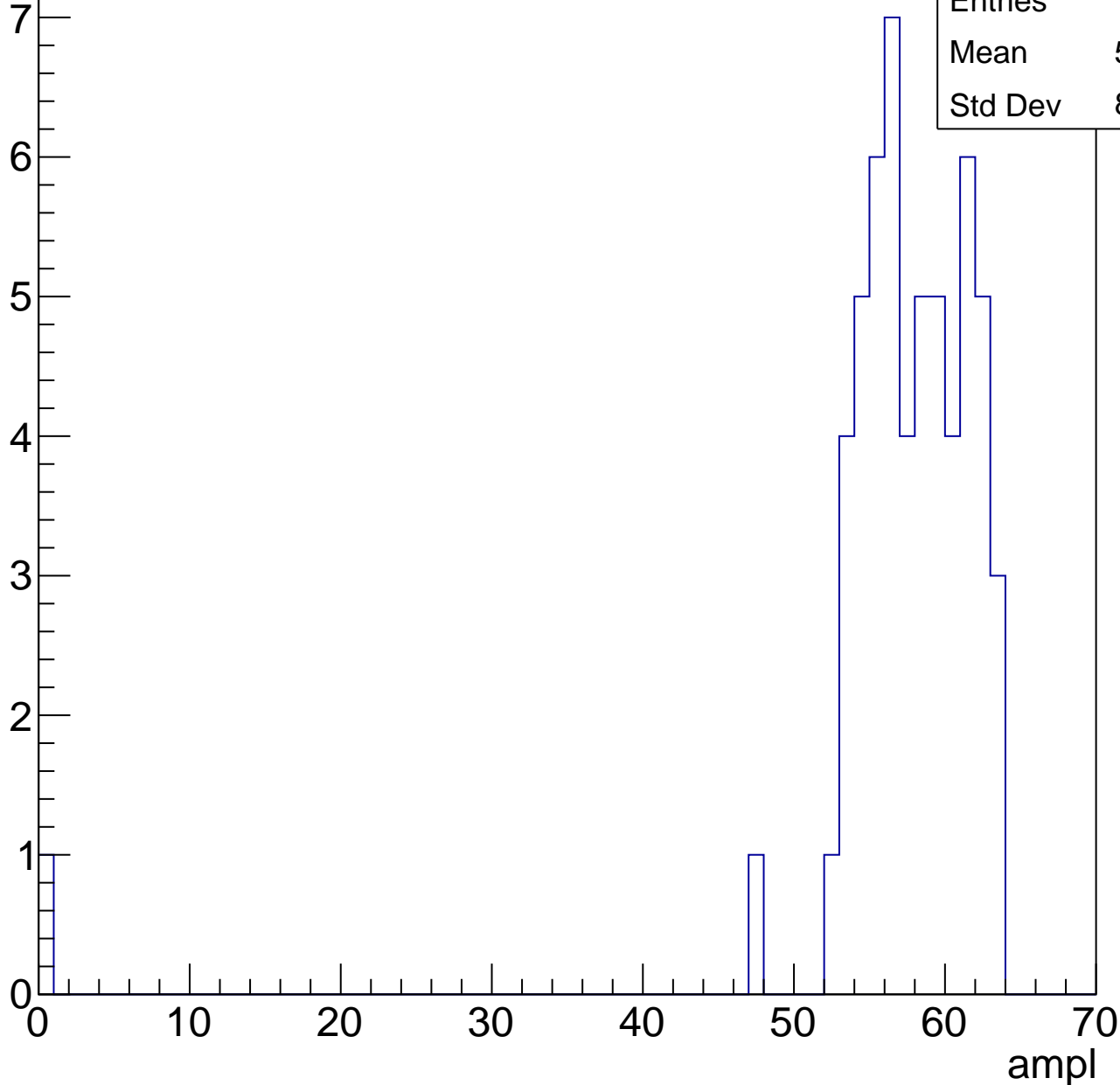


# B0L001S, U21-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	56.51
Std Dev	8.261

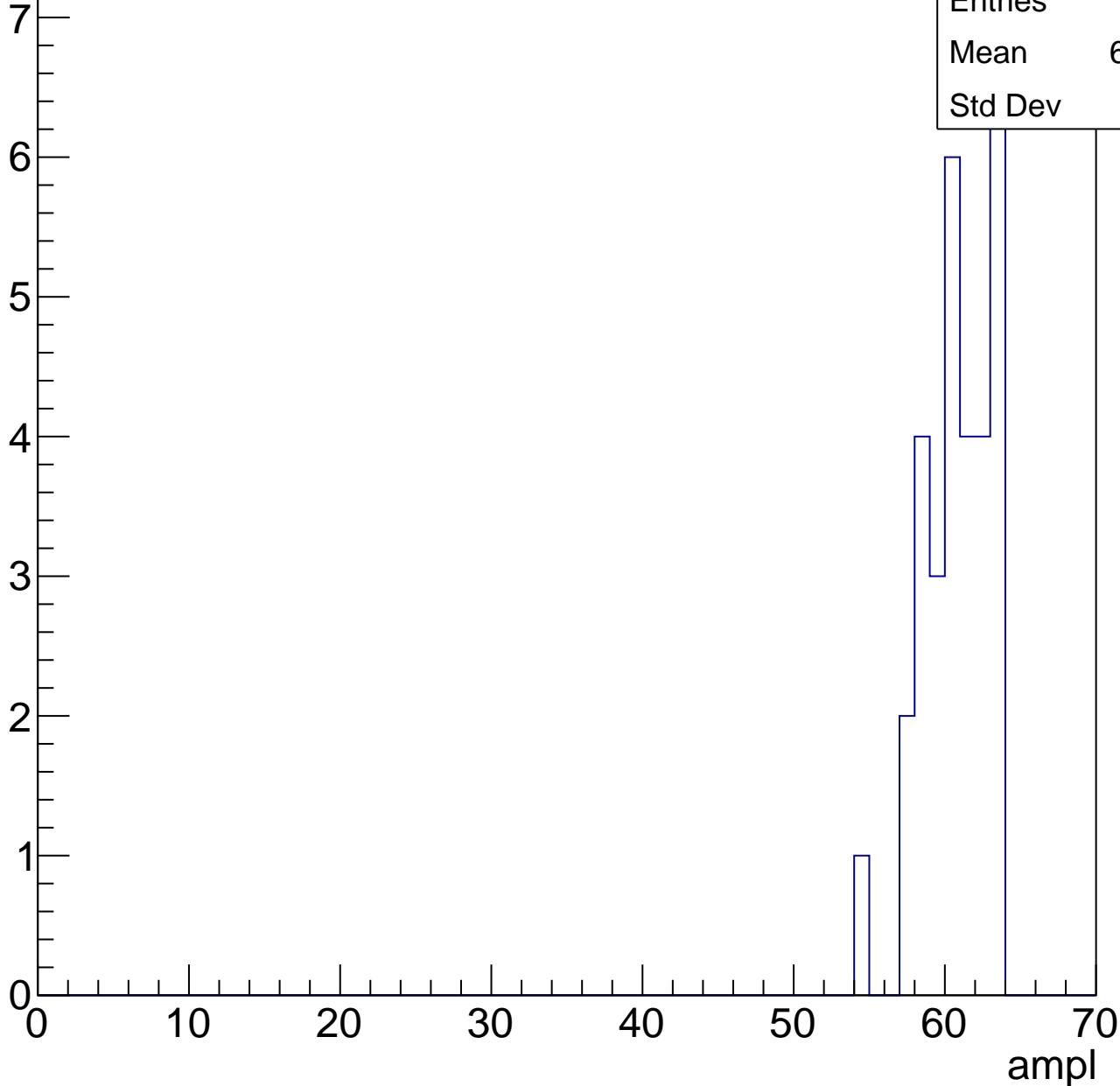


# B0L001S, U21-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	31
Mean	60.32
Std Dev	2.22



# B0L001S, U21-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	24
Std Dev	0

ampl



# B0L001S, U21-ch32, adc0

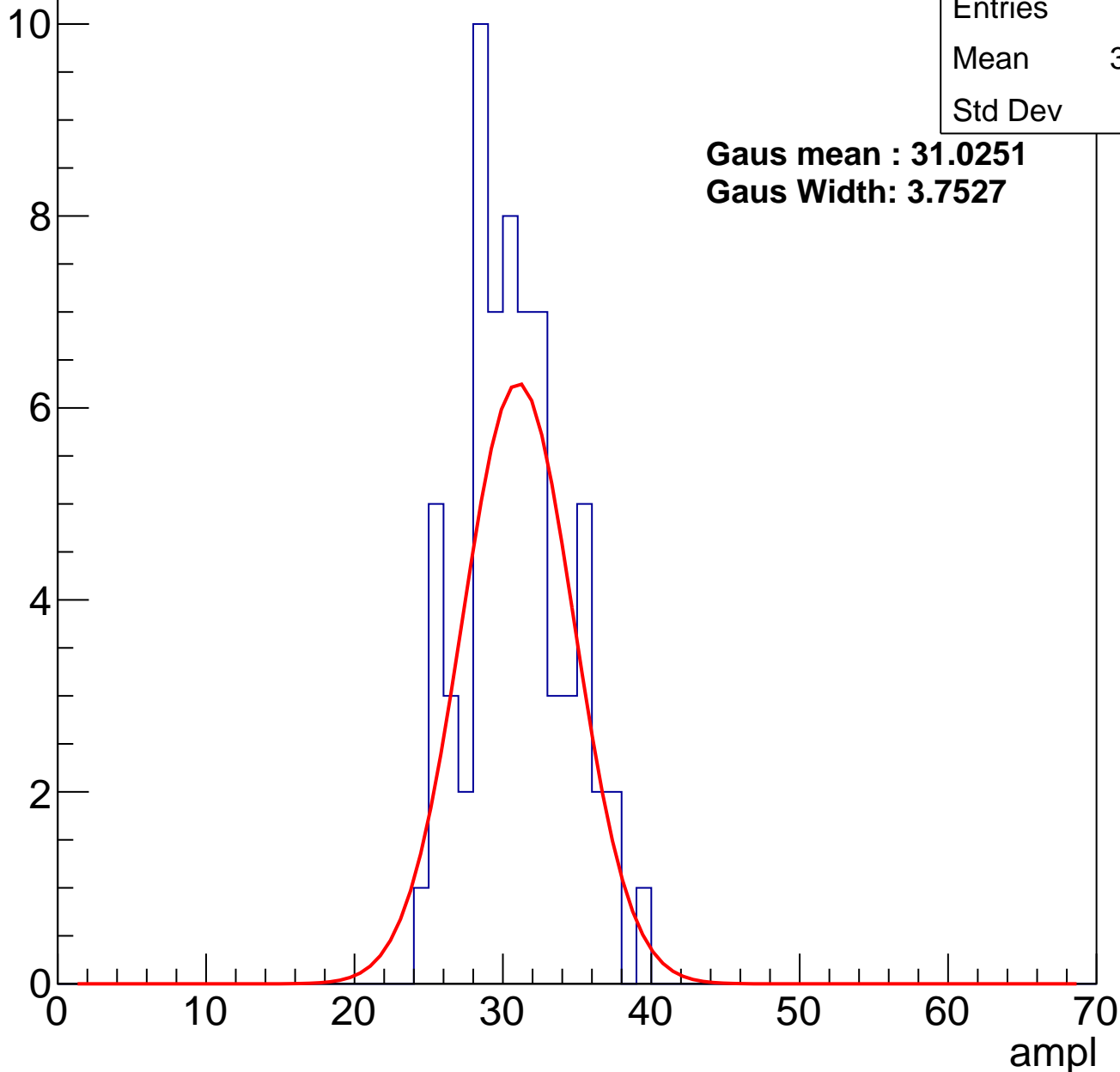
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	66
Mean	30.39
Std Dev	3.37

**Gaus mean : 31.0251**

**Gaus Width: 3.7527**

Entry



# B0L001S, U21-ch32, adc1

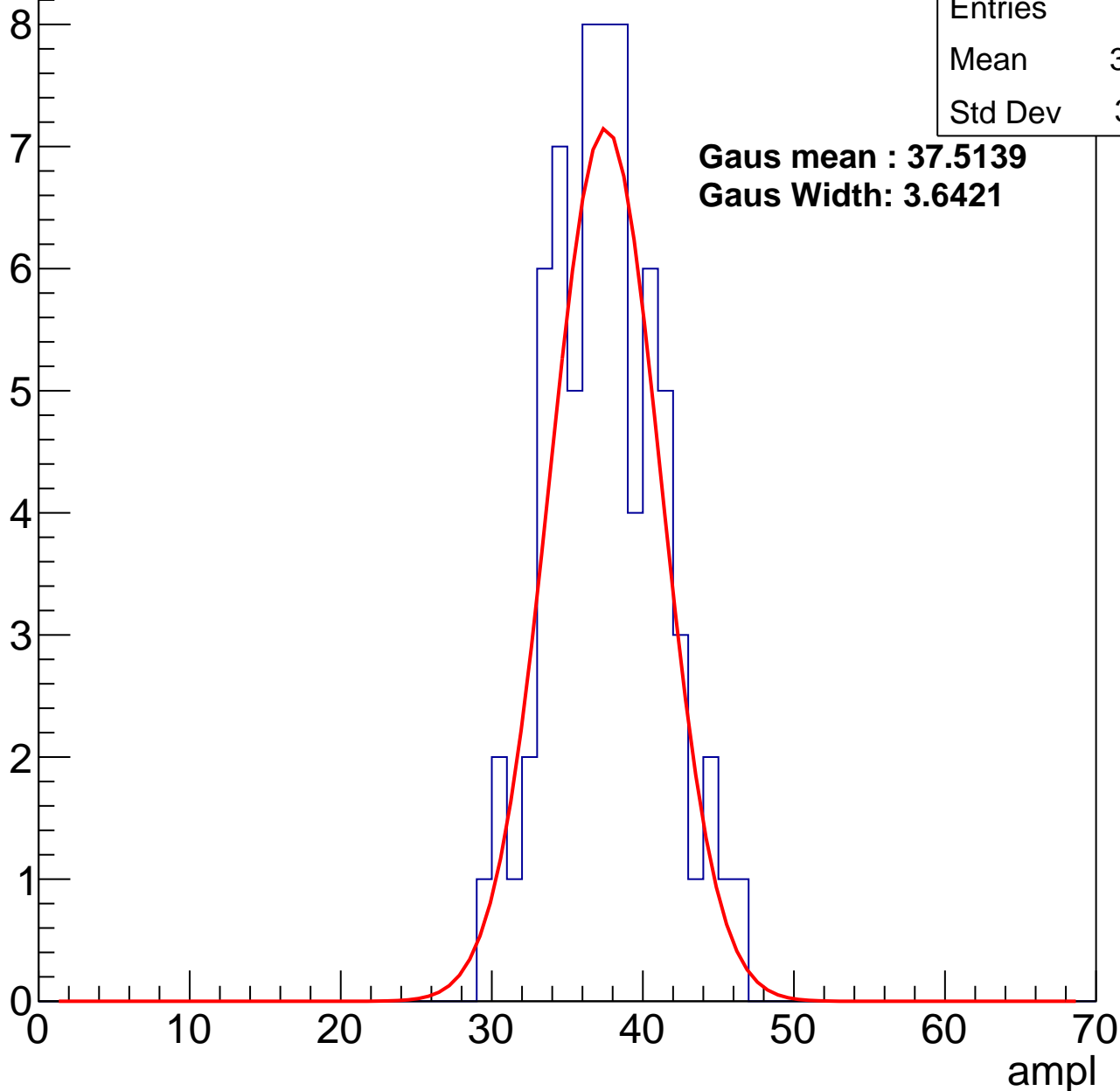
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	37.07
Std Dev	3.651

**Gaus mean : 37.5139**

**Gaus Width: 3.6421**



# B0L001S, U21-ch32, adc2

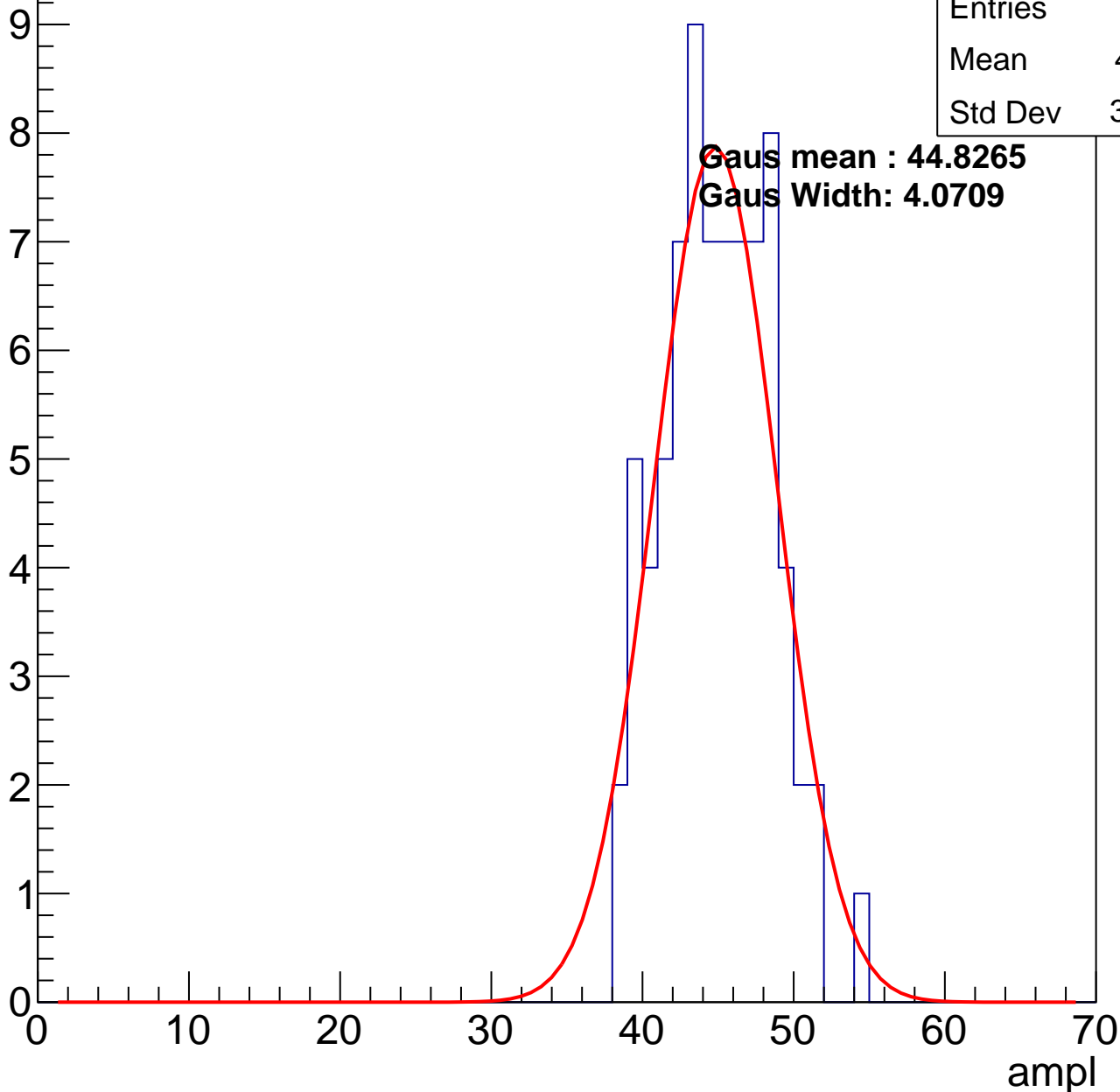
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	44.51
Std Dev	3.455

Gaus mean : 44.8265

Gaus Width: 4.0709

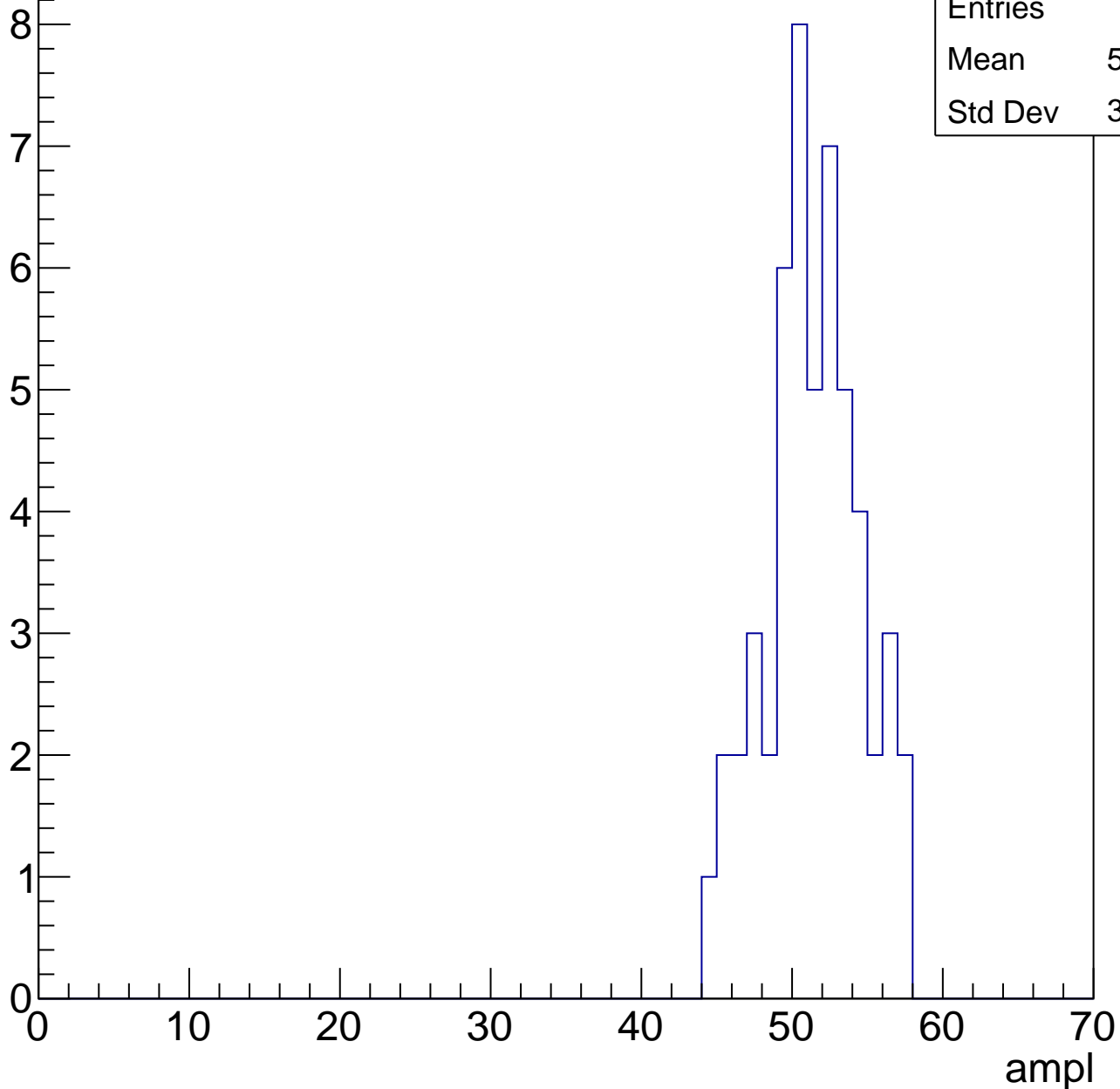


# B0L001S, U21-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

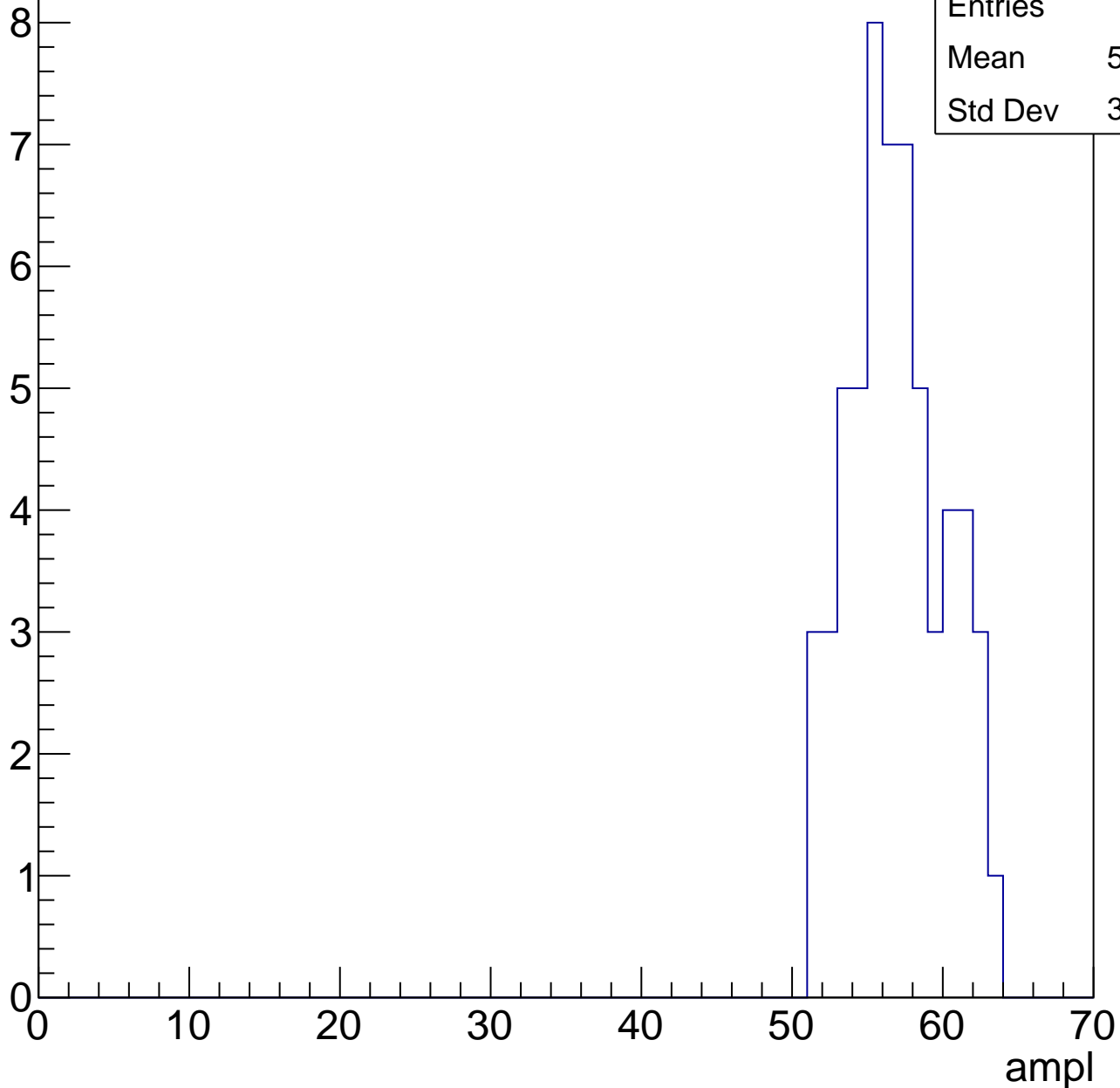
Entries	52
Mean	50.94
Std Dev	3.134



# B0L001S, U21-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



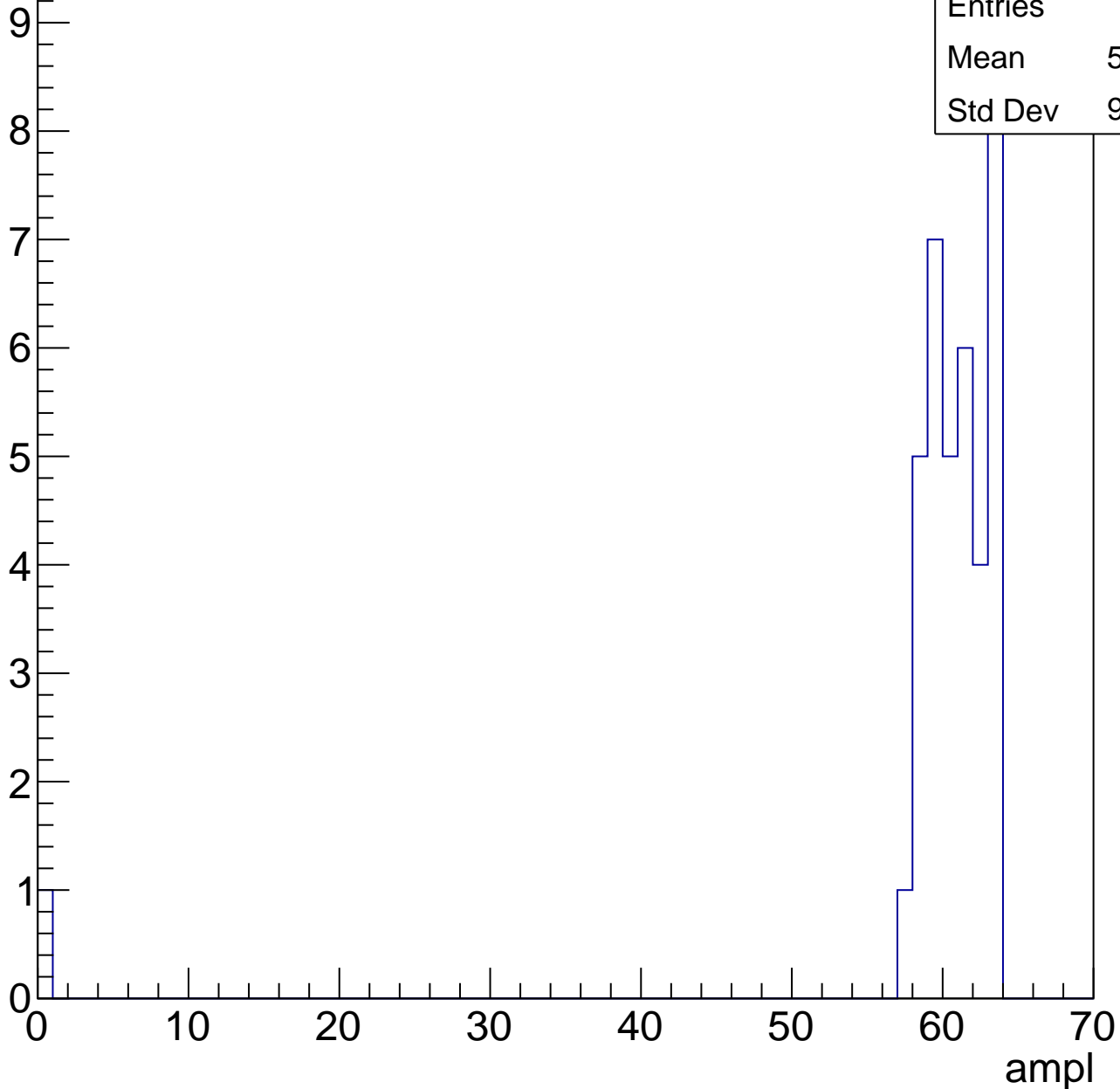
Entries	58
Mean	56.47
Std Dev	3.103

# B0L001S, U21-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

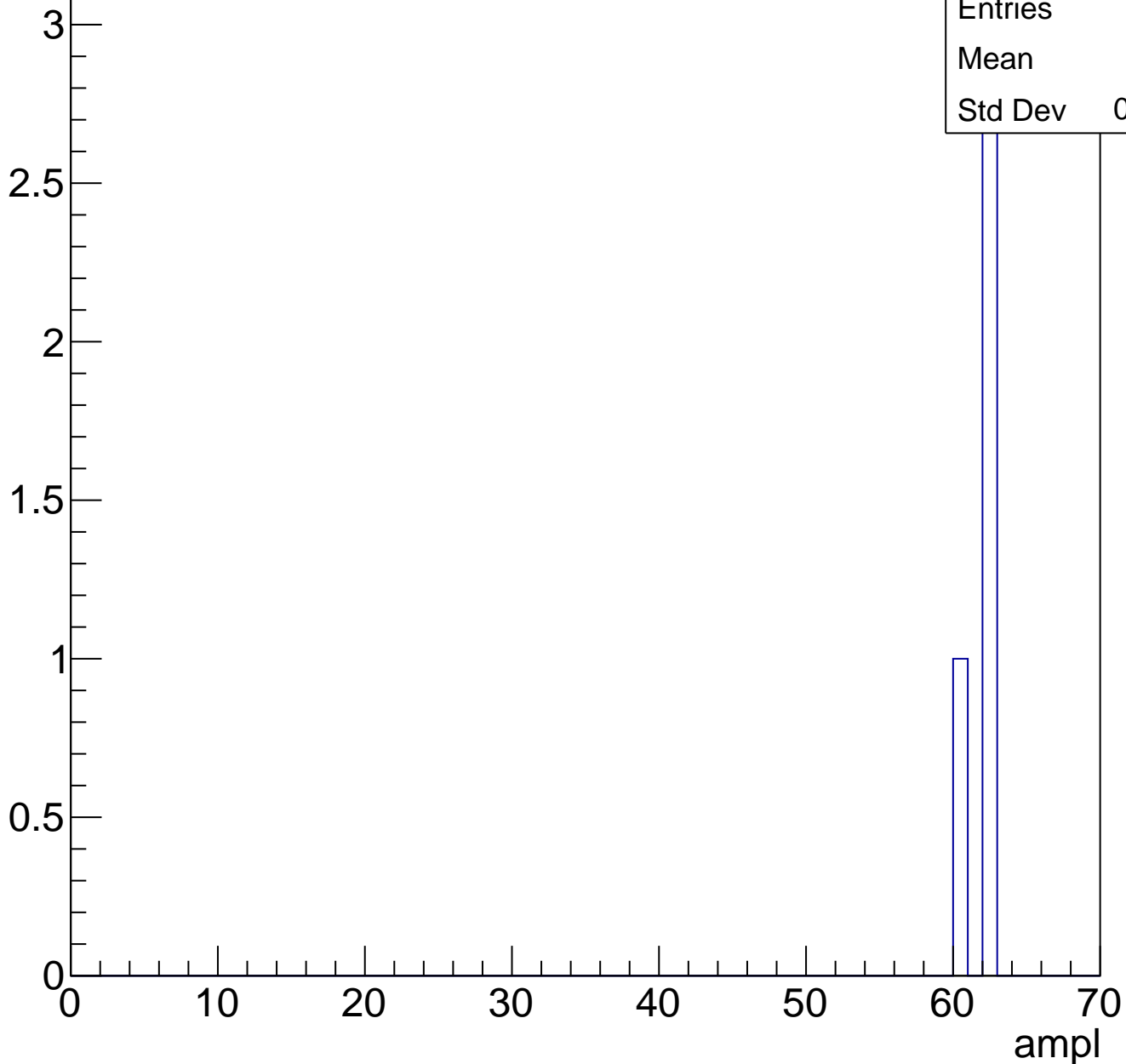
Entries	38
Mean	58.97
Std Dev	9.866



# B0L001S, U21-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	24
Std Dev	0

# B0L001S, U21-ch33, adc0

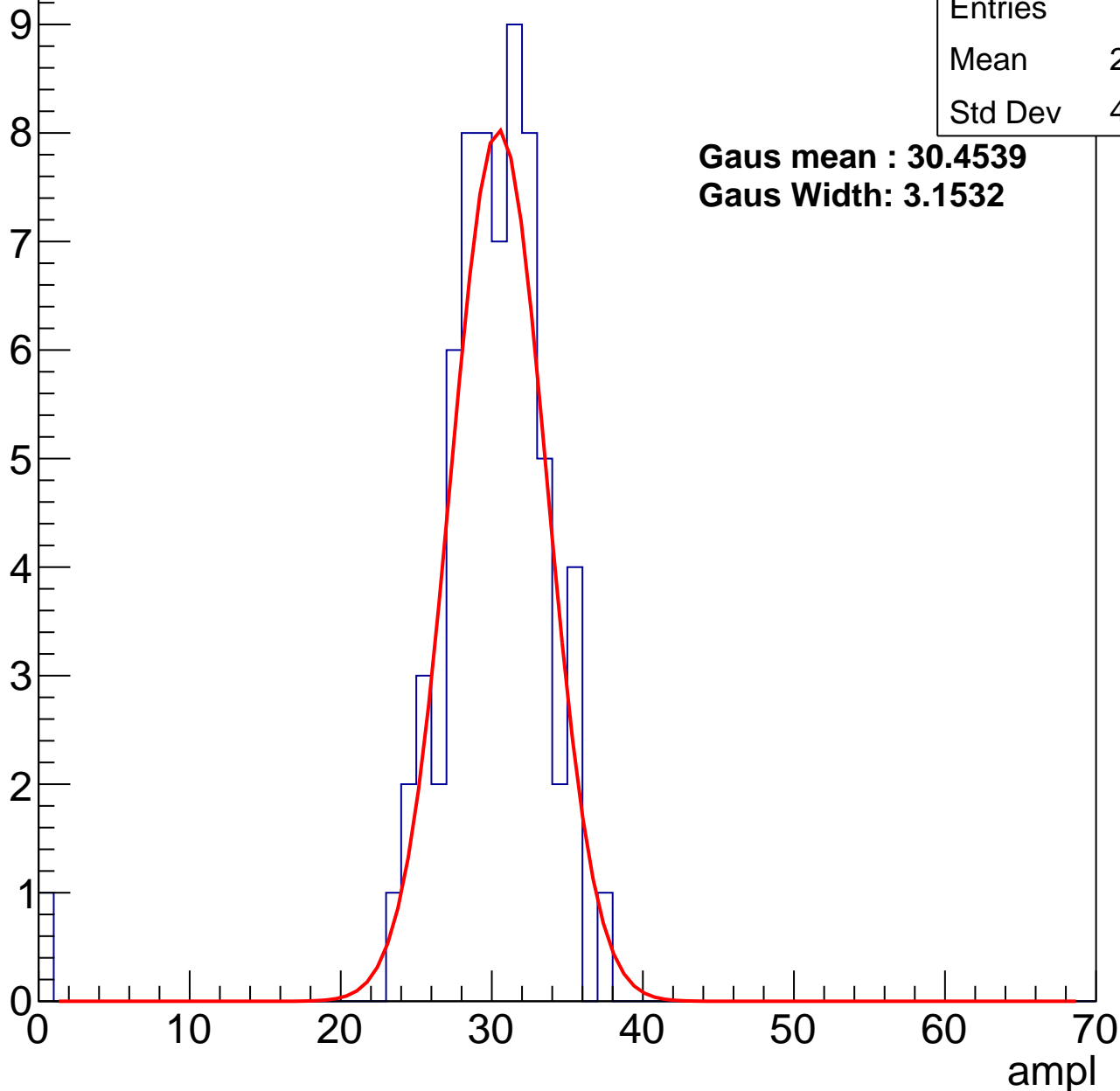
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	29.42
Std Dev	4.678

**Gaus mean : 30.4539**

**Gaus Width: 3.1532**



# B0L001S, U21-ch33, adc1

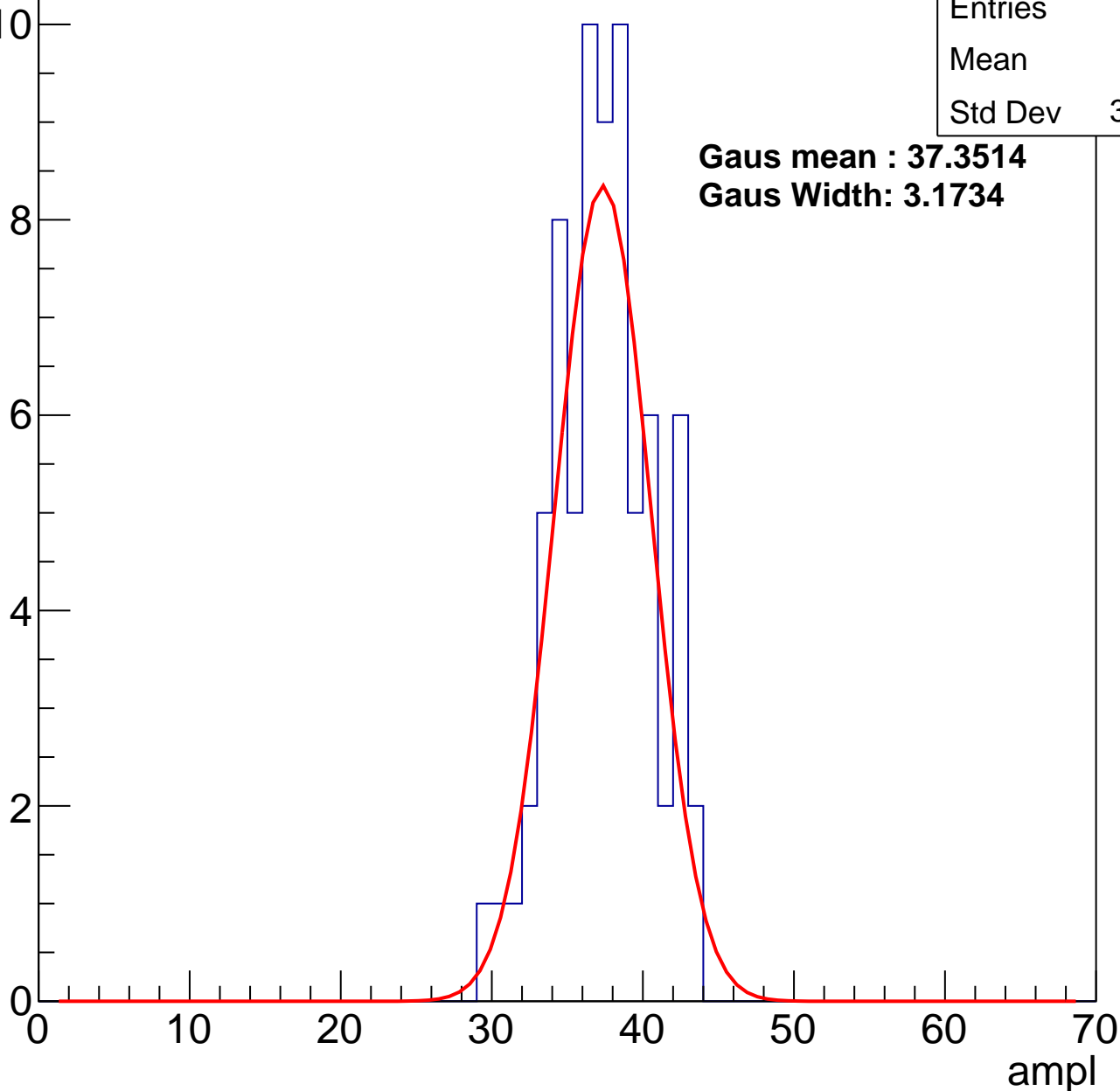
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	36.9
Std Dev	3.137

**Gaus mean : 37.3514**

**Gaus Width: 3.1734**



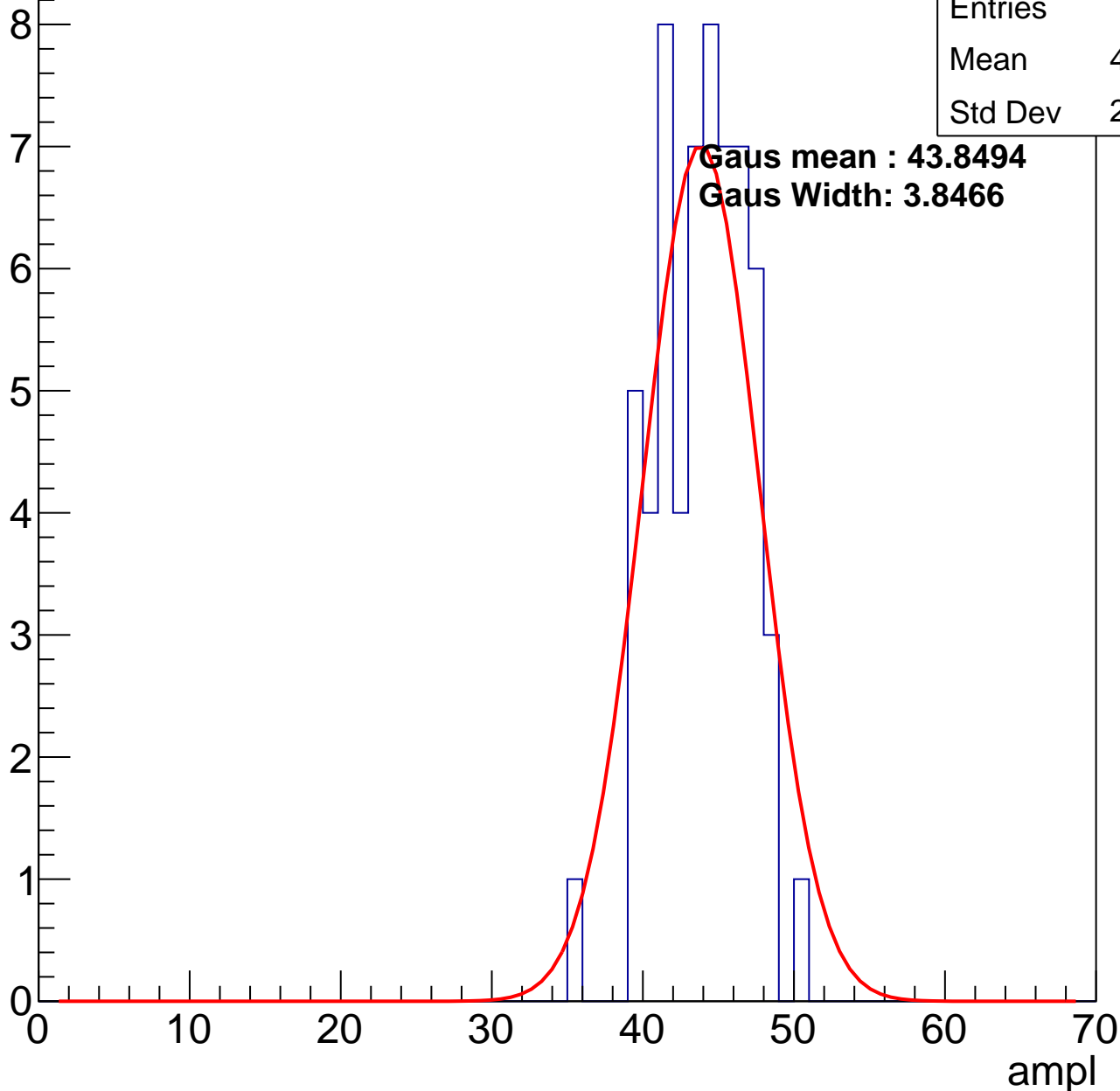
# B0L001S, U21-ch33, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	43.48
Std Dev	2.923

**Gaus mean : 43.8494**  
**Gaus Width: 3.8466**



# B0L001S, U21-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

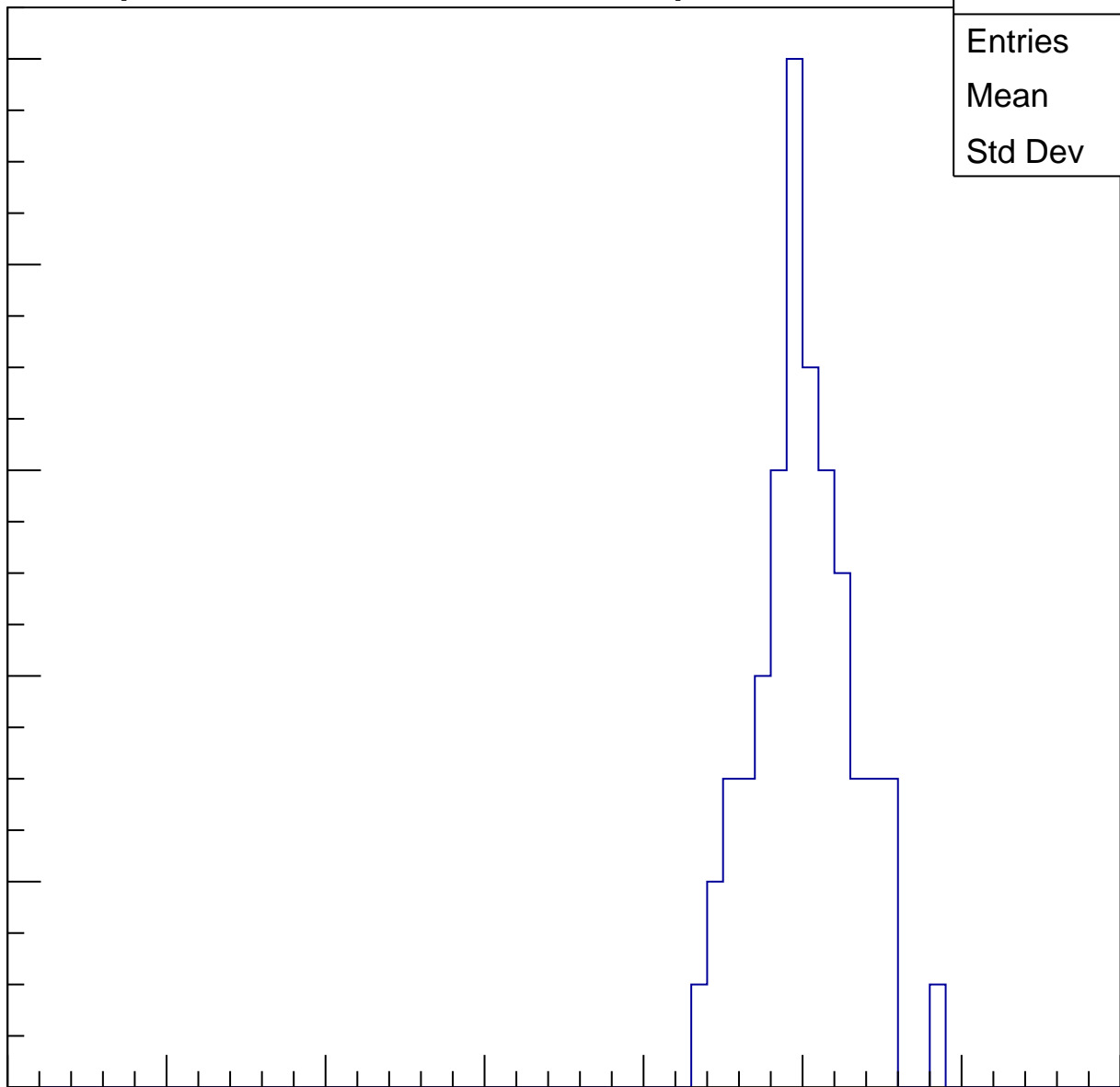
Entries	57
Mean	49.65
Std Dev	3.098

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

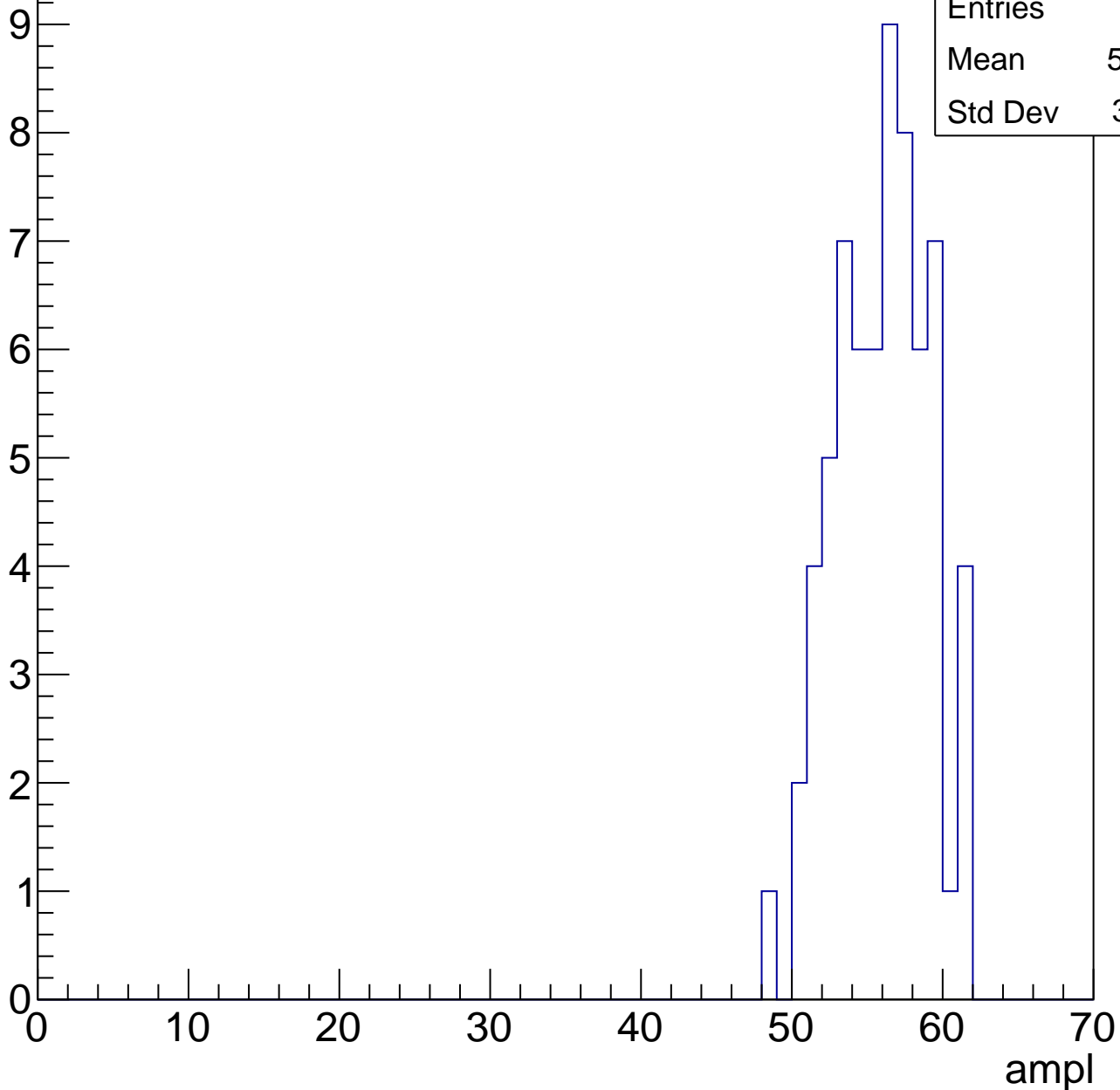


# B0L001S, U21-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

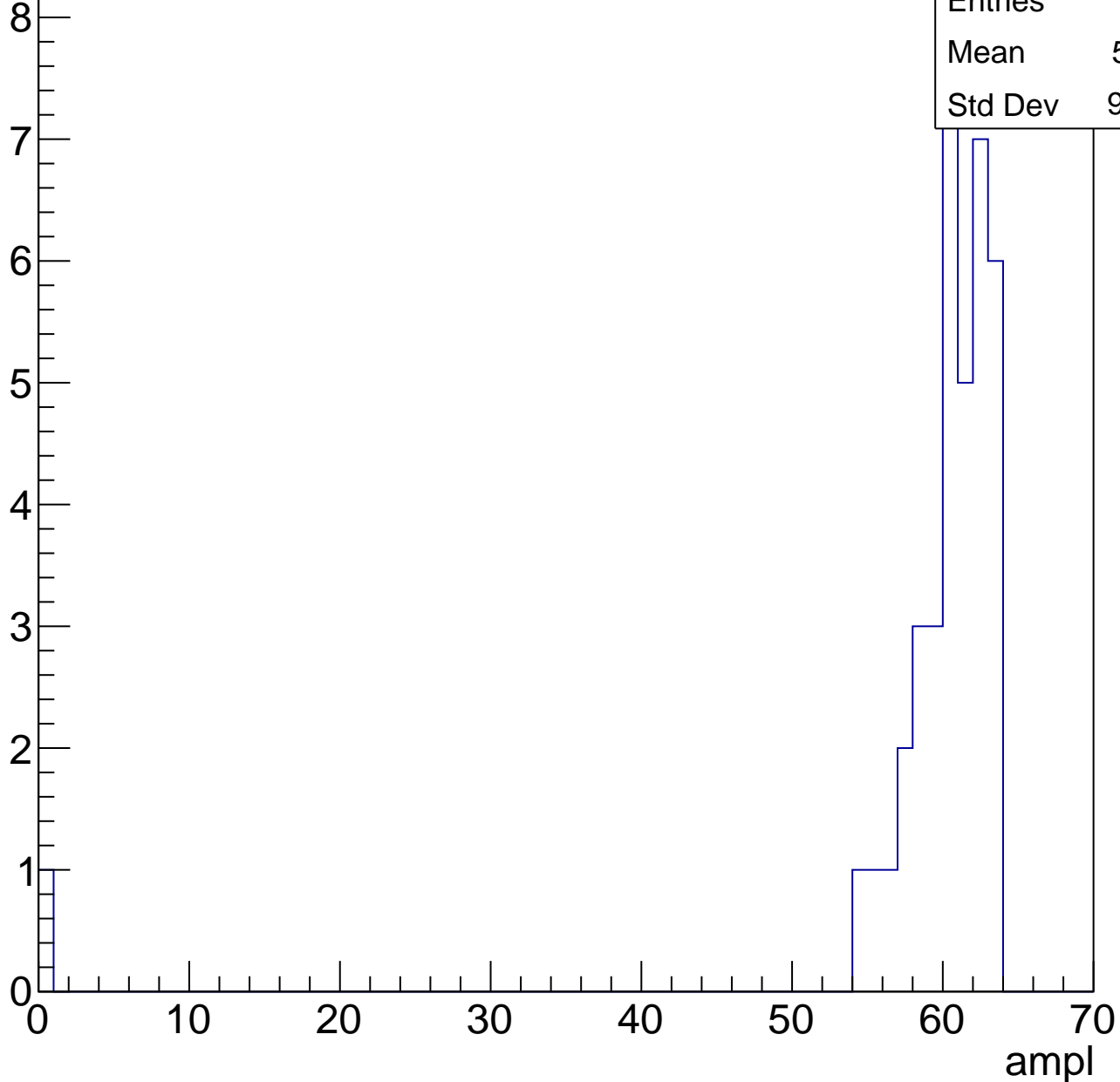
Entries	66
Mean	55.48
Std Dev	3.021



# B0L001S, U21-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U21-ch34, adc0

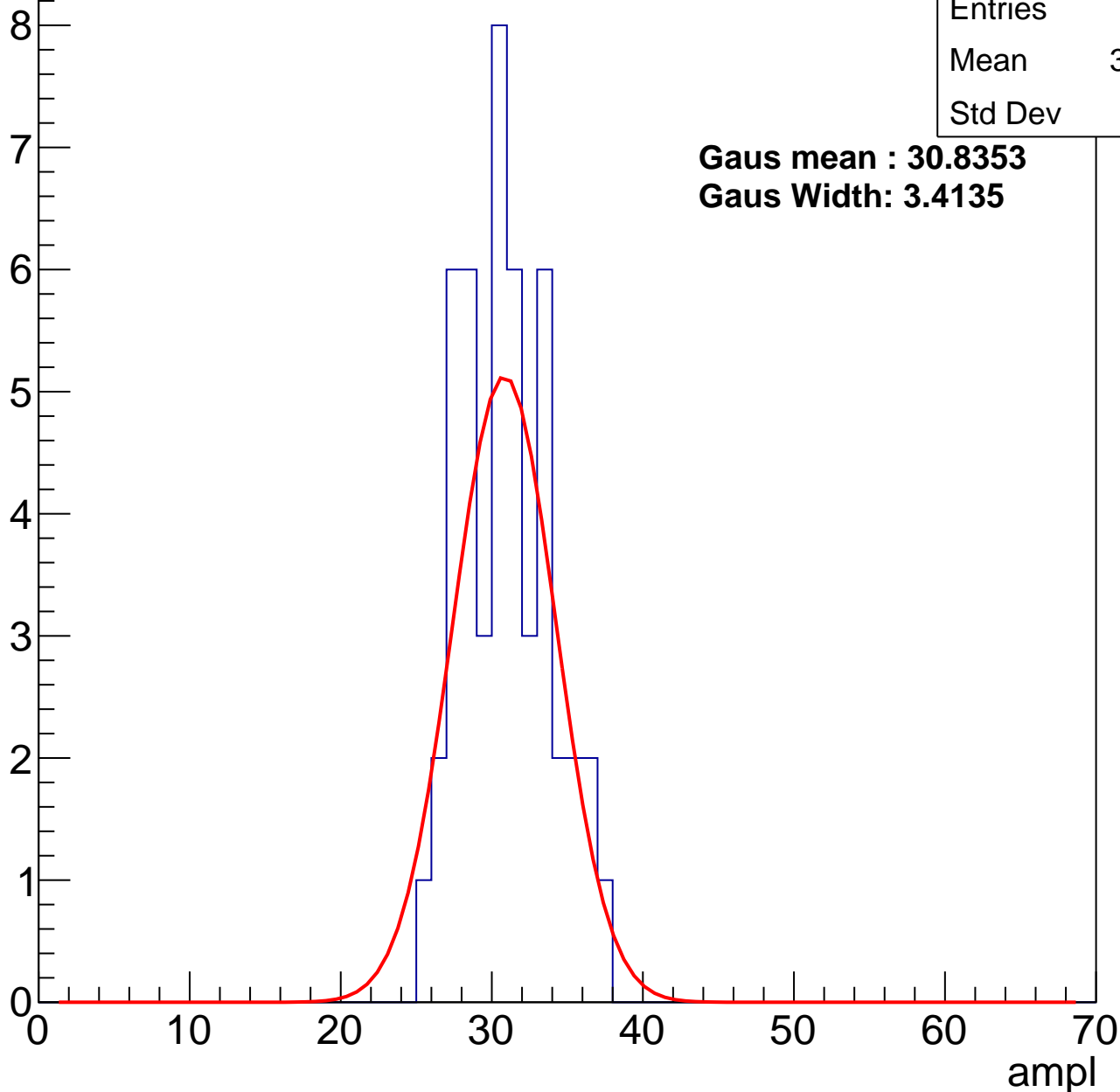
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	30.44
Std Dev	2.9

**Gaus mean : 30.8353**

**Gaus Width: 3.4135**



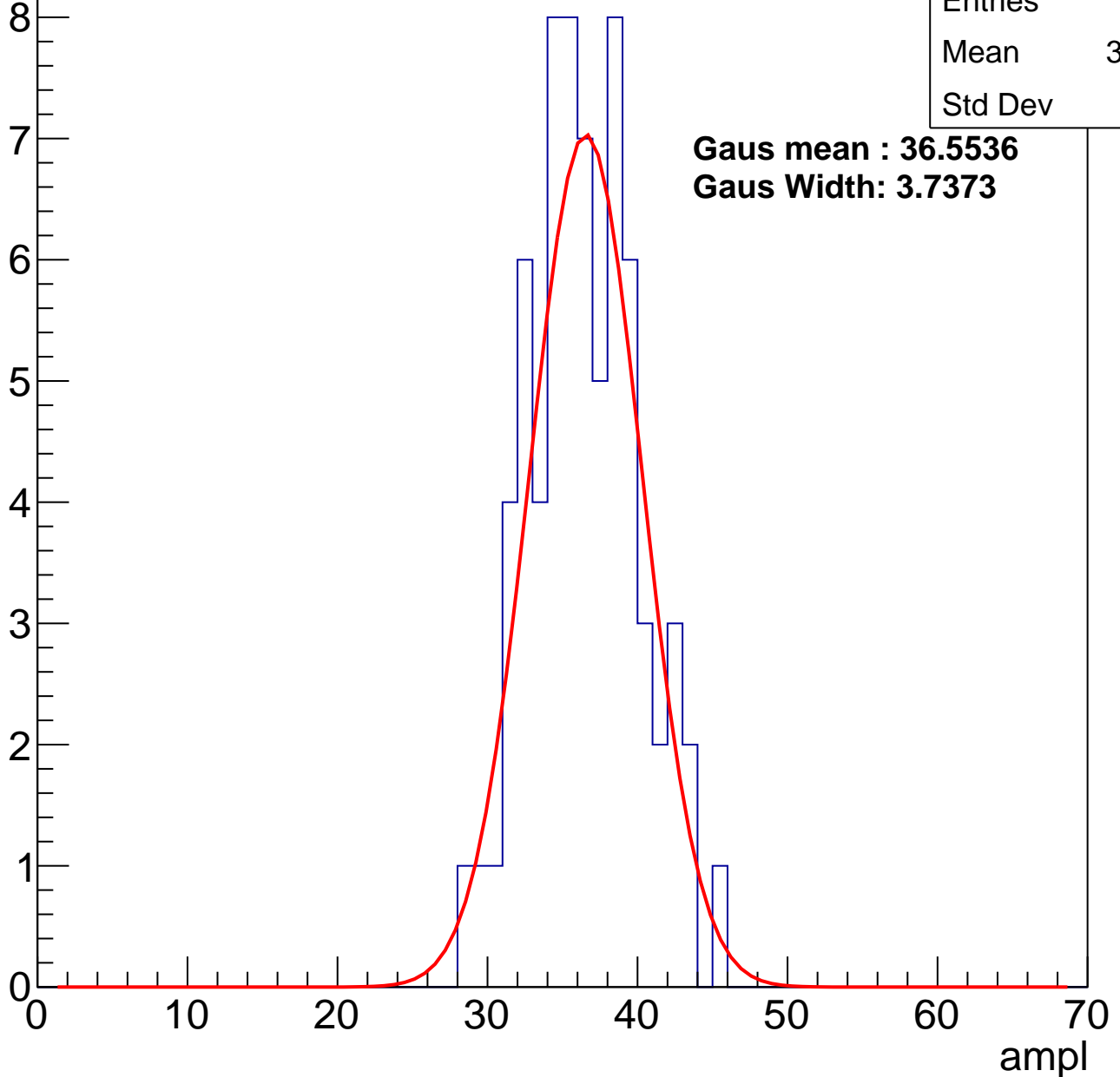
# B0L001S, U21-ch34, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	36.01
Std Dev	3.58

**Gaus mean : 36.5536**  
**Gaus Width: 3.7373**



# B0L001S, U21-ch34, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	87
Mean	43.74
Std Dev	3.789

**Gaus mean : 44.1456**

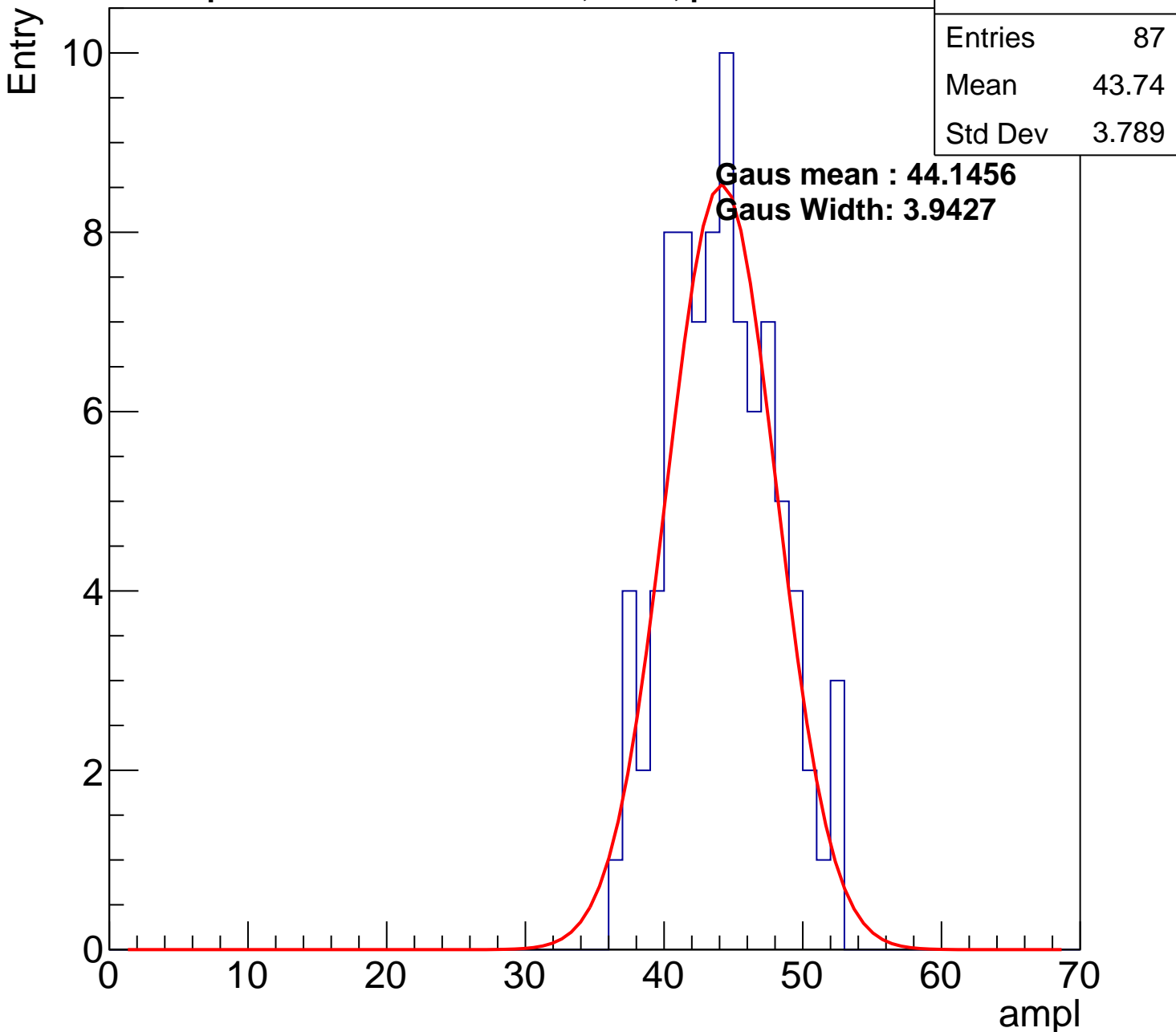
**Gaus Width: 3.9427**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

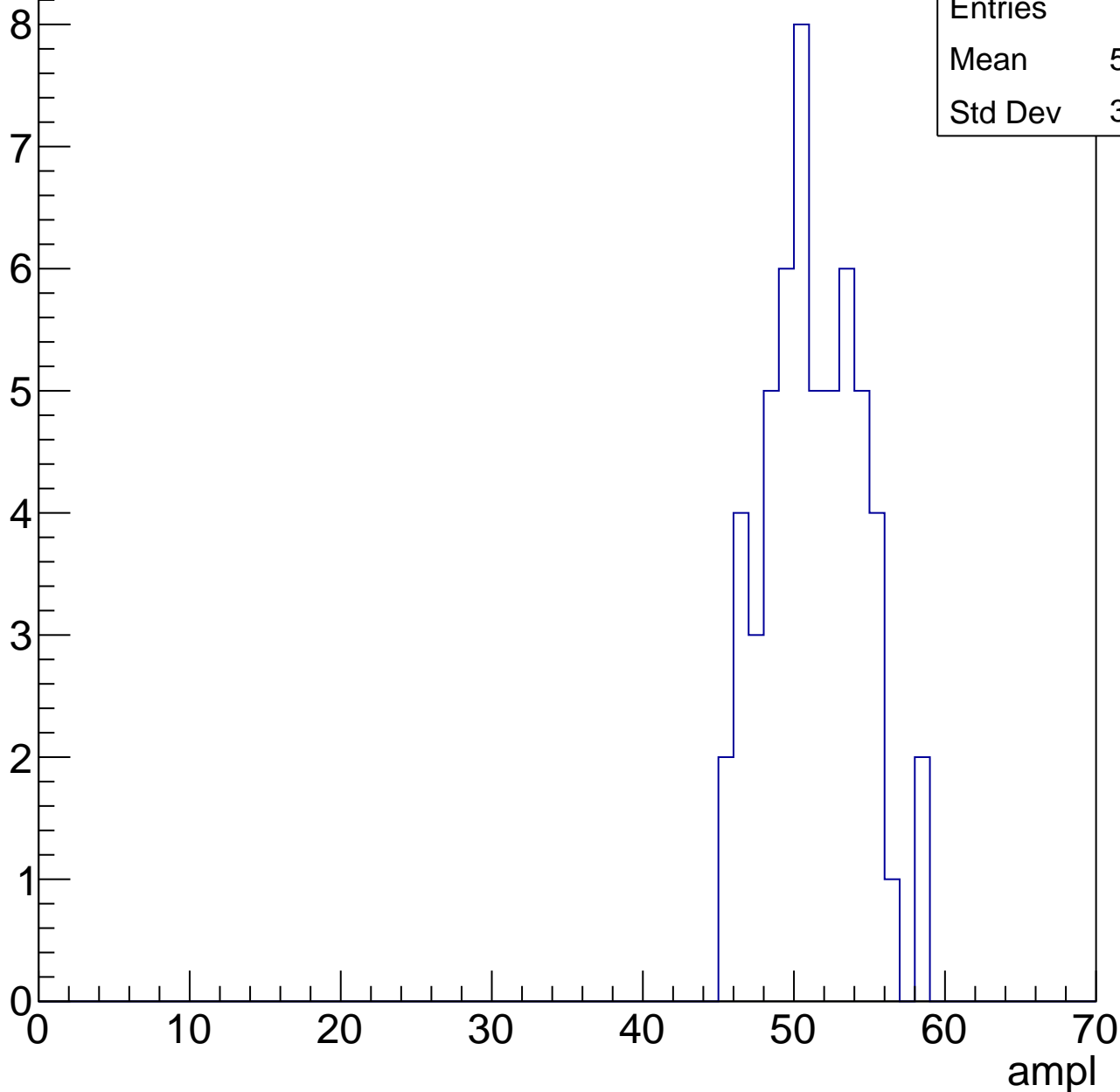


# B0L001S, U21-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	50.79
Std Dev	3.149

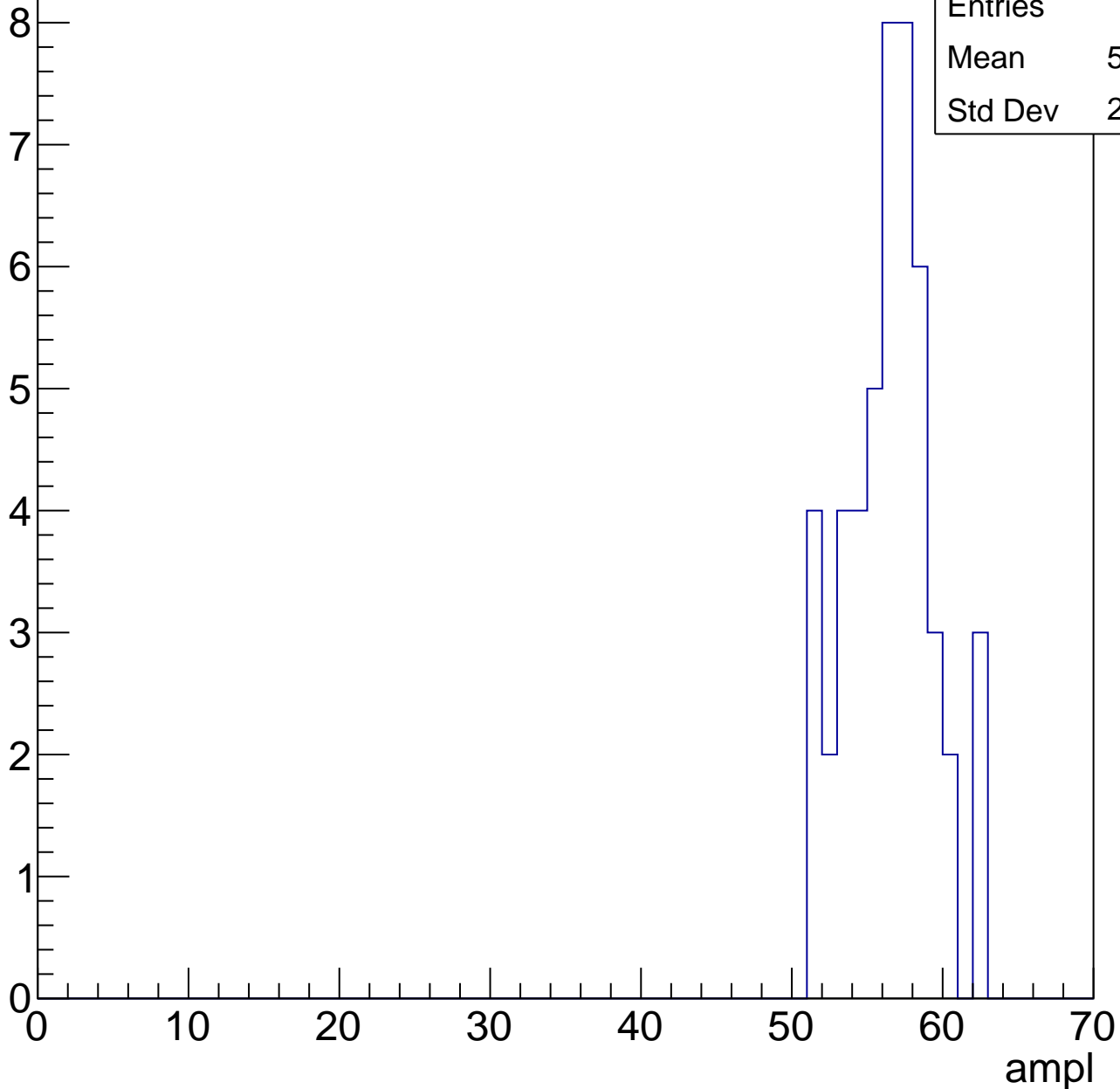


# B0L001S, U21-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	56.04
Std Dev	2.814

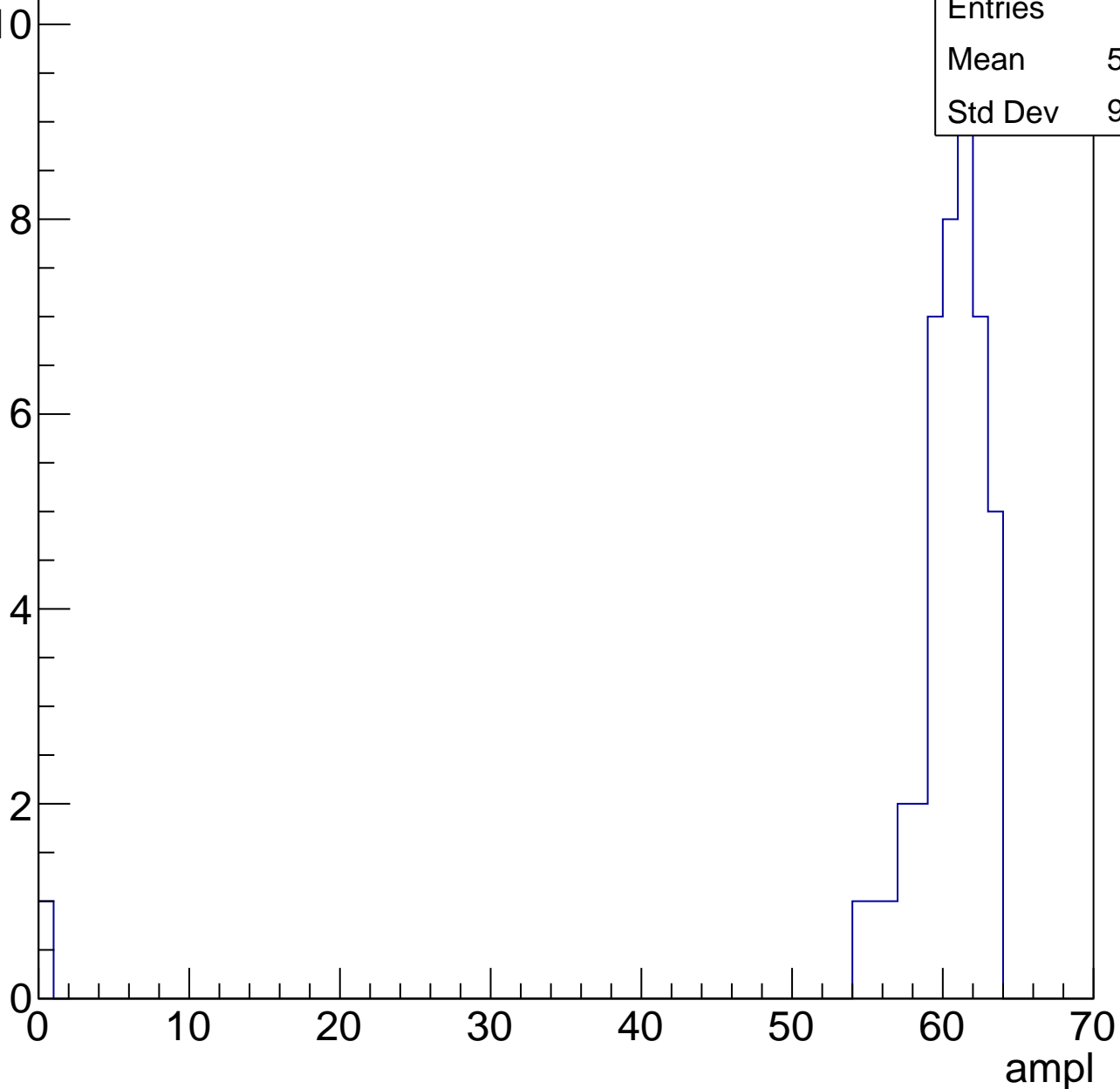


# B0L001S, U21-ch34, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	45
Mean	58.82
Std Dev	9.105



# B0L001S, U21-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch35, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	78
Mean	29.35
Std Dev	4.747

**Gaus mean : 29.8704**

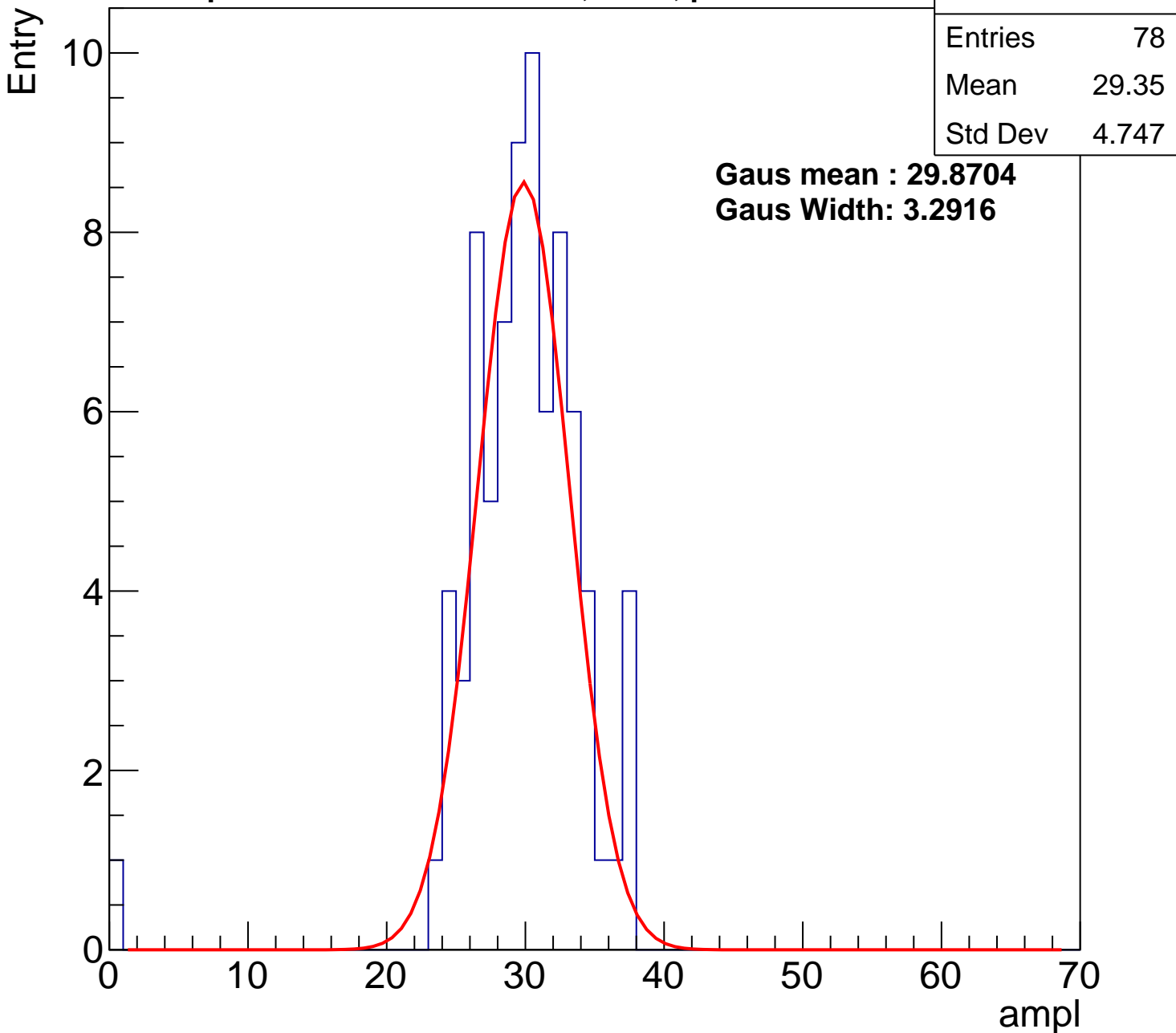
**Gaus Width: 3.2916**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U21-ch35, adc1

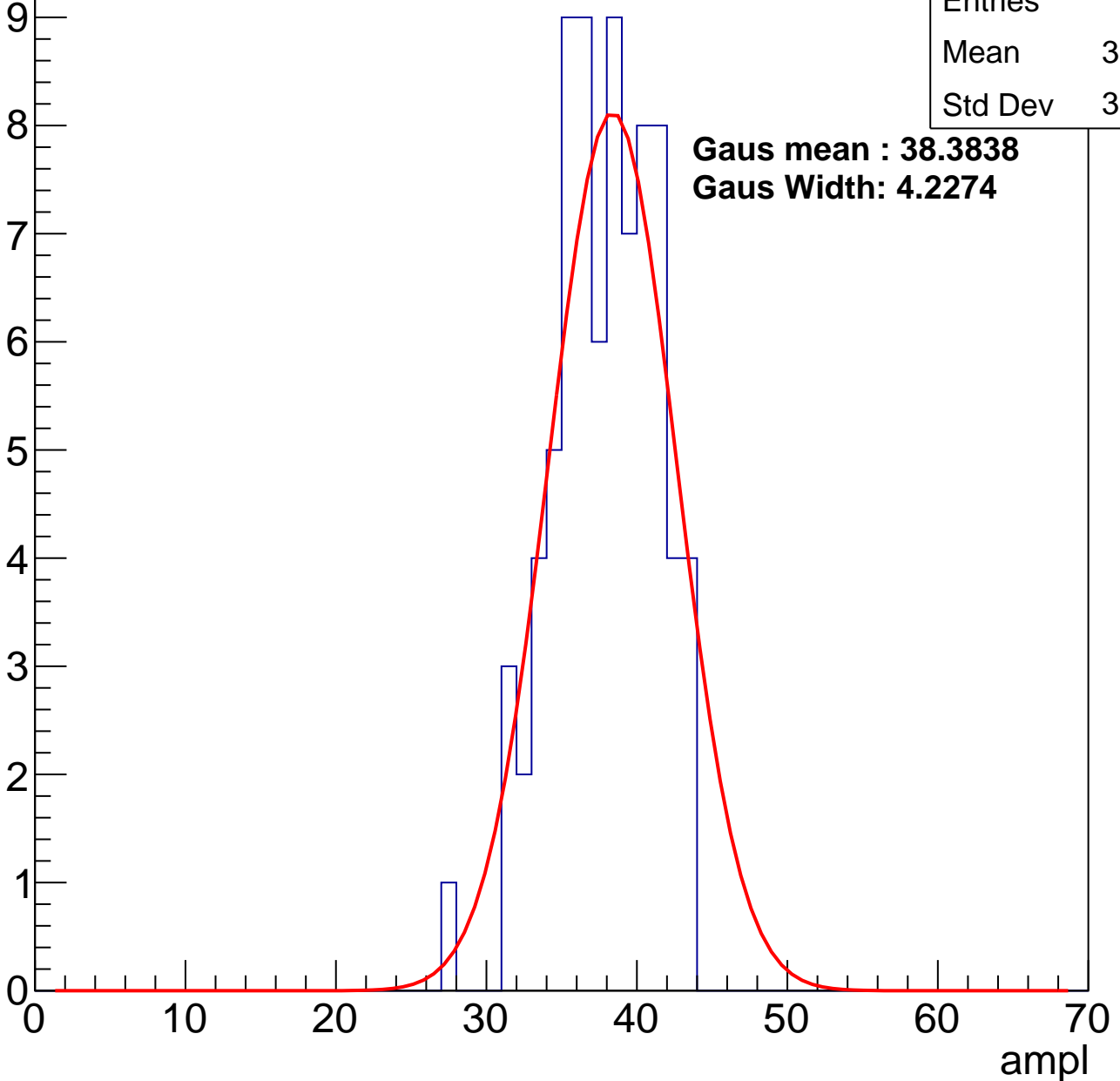
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	37.34
Std Dev	3.345

**Gaus mean : 38.3838**

**Gaus Width: 4.2274**



# B0L001S, U21-ch35, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	82
Mean	45.41
Std Dev	3.396

**Gaus mean : 46.1125**

**Gaus Width: 3.0527**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

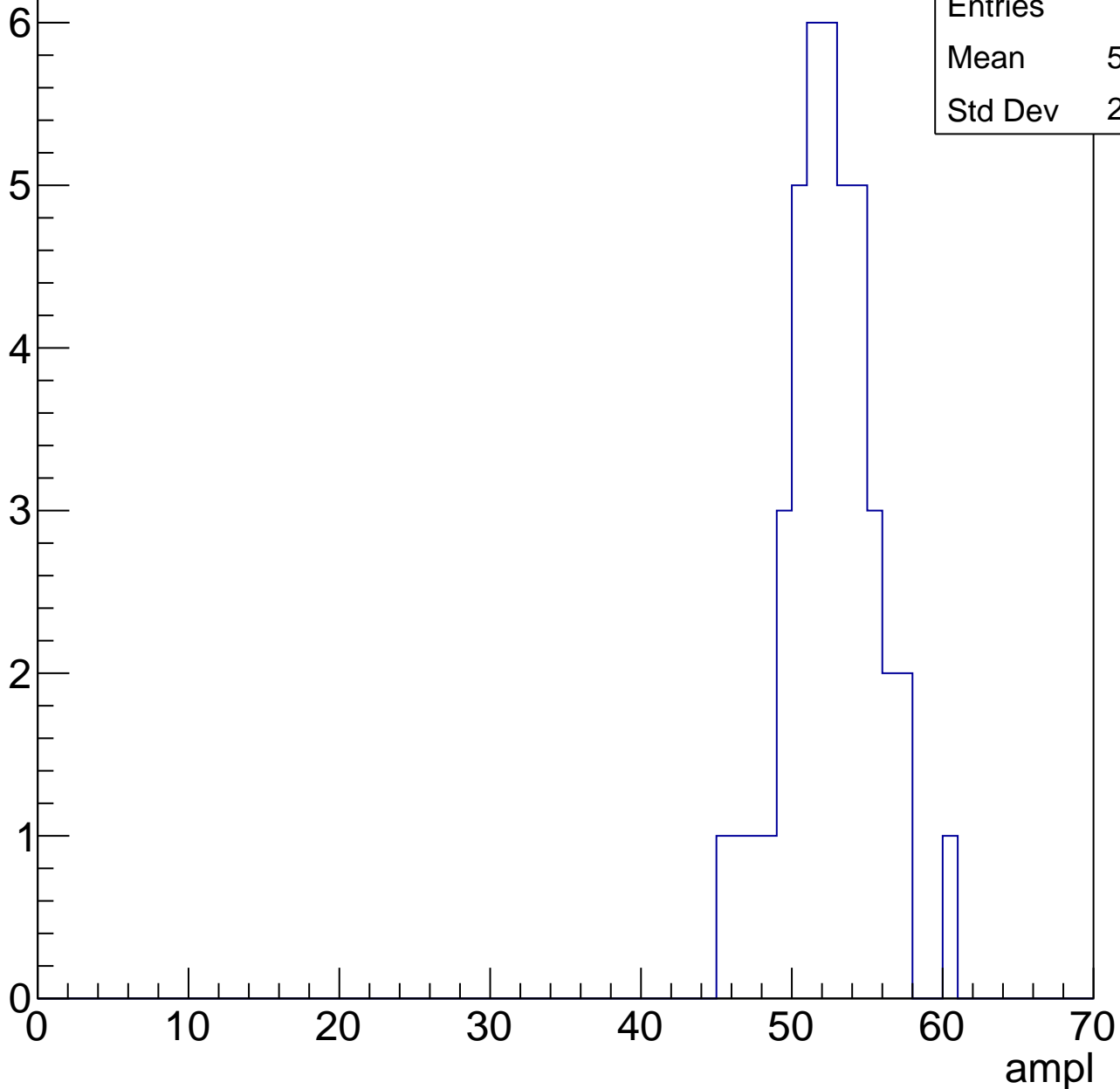


# B0L001S, U21-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

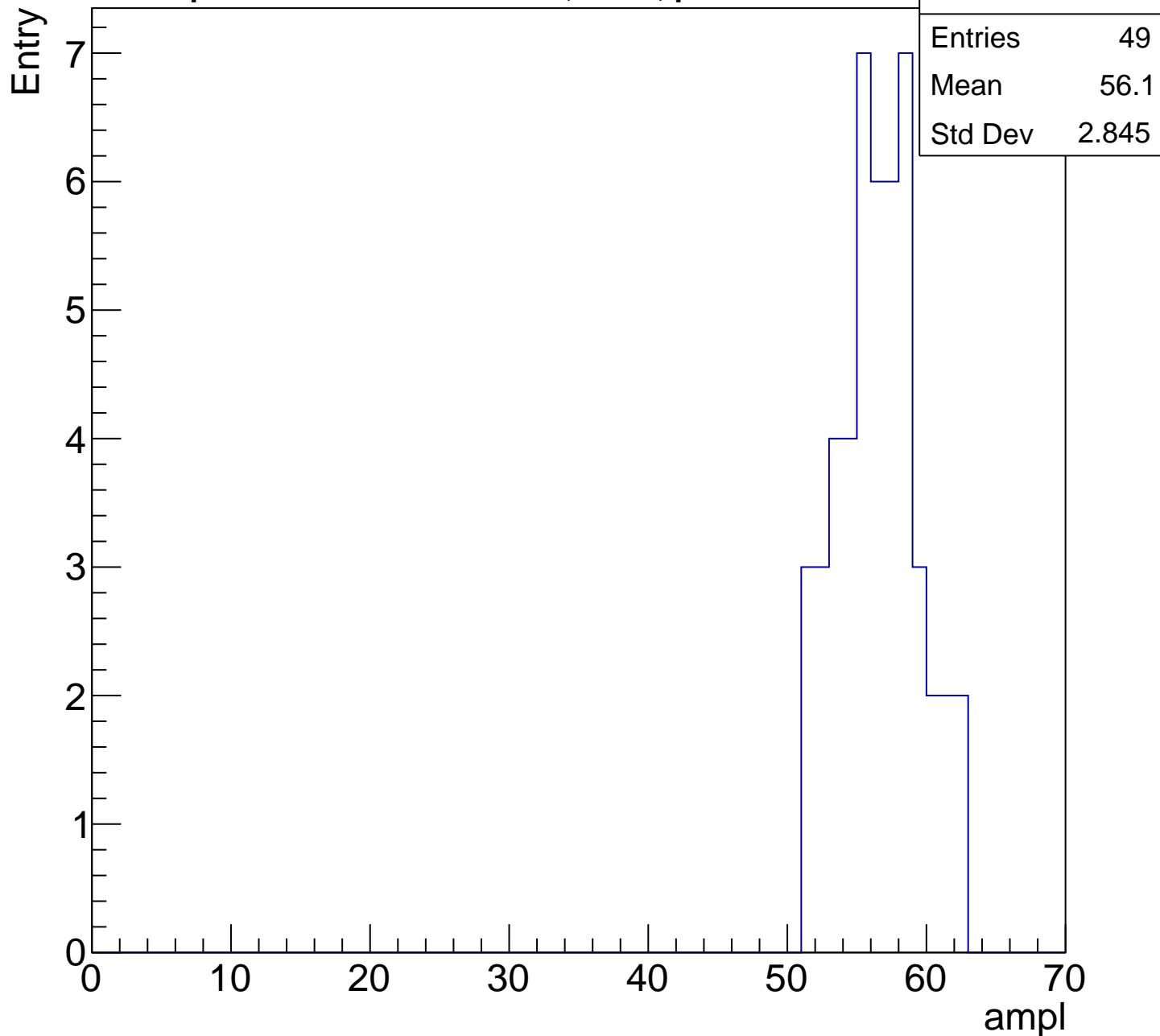
Entry

Entries	42
Mean	52.07
Std Dev	2.995



# B0L001S, U21-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

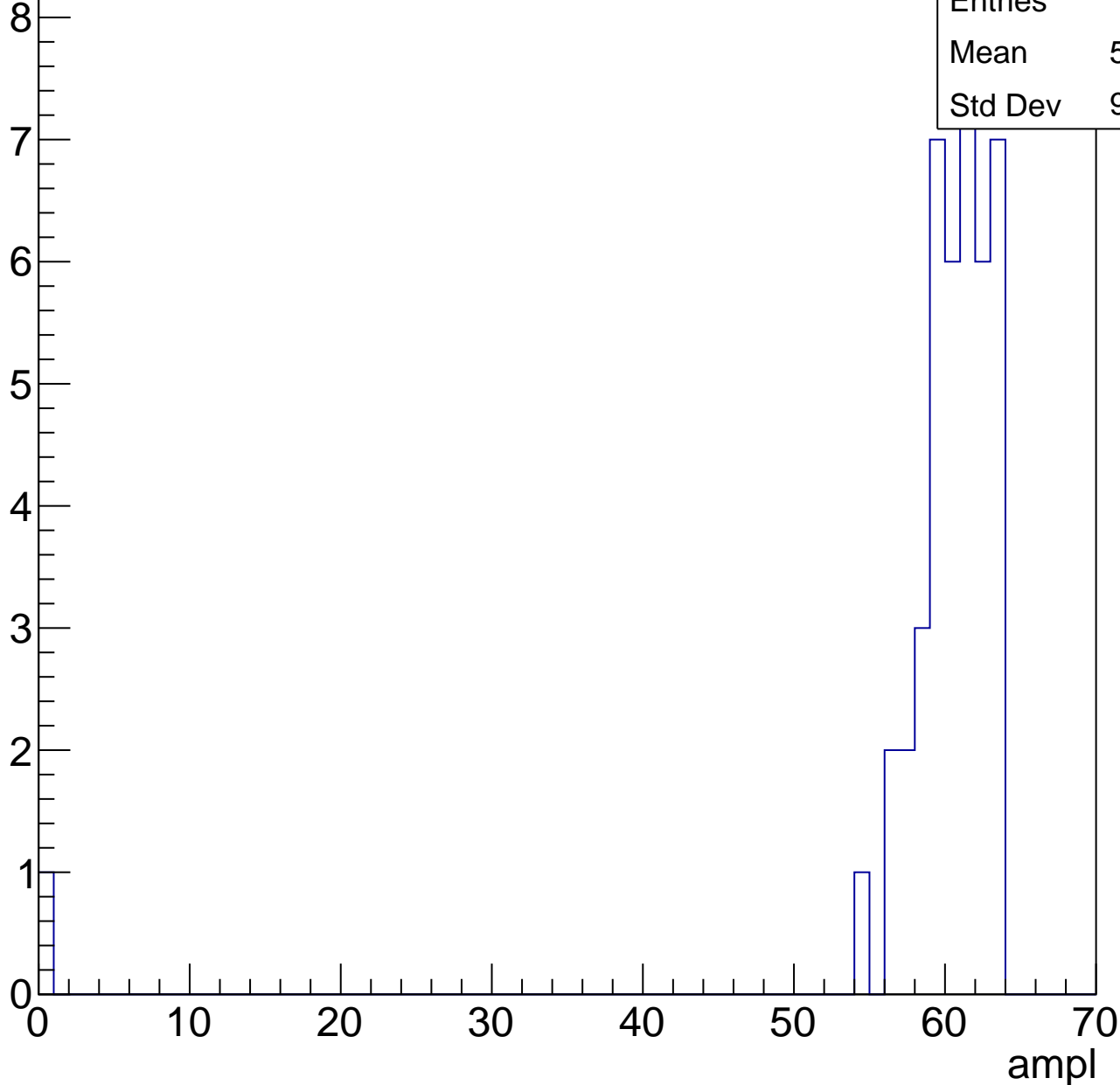


# B0L001S, U21-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	43
Mean	58.79
Std Dev	9.323



# B0L001S, U21-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U21-ch36, adc0

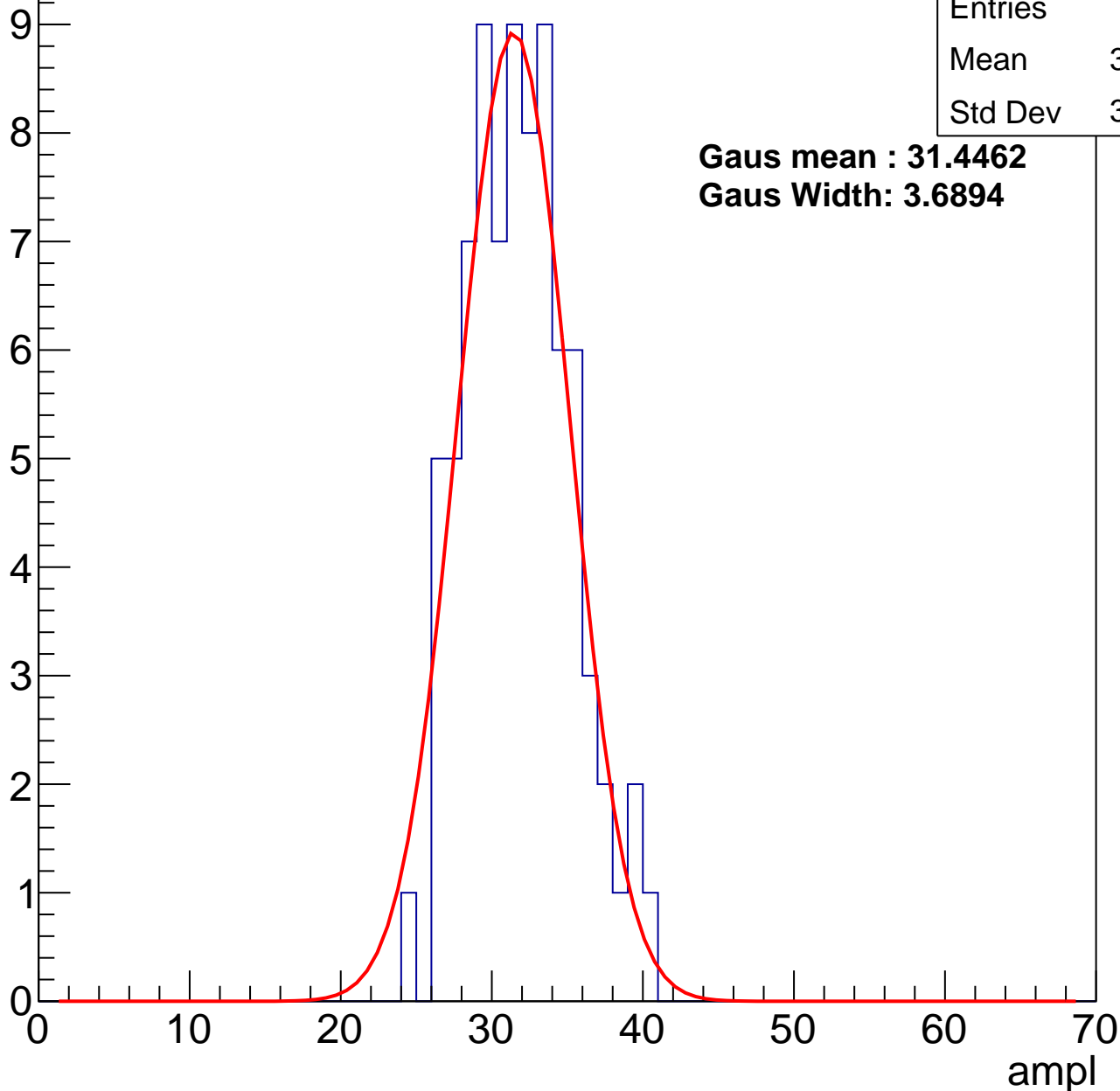
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	31.36
Std Dev	3.422

**Gaus mean : 31.4462**

**Gaus Width: 3.6894**



# B0L001S, U21-ch36, adc1

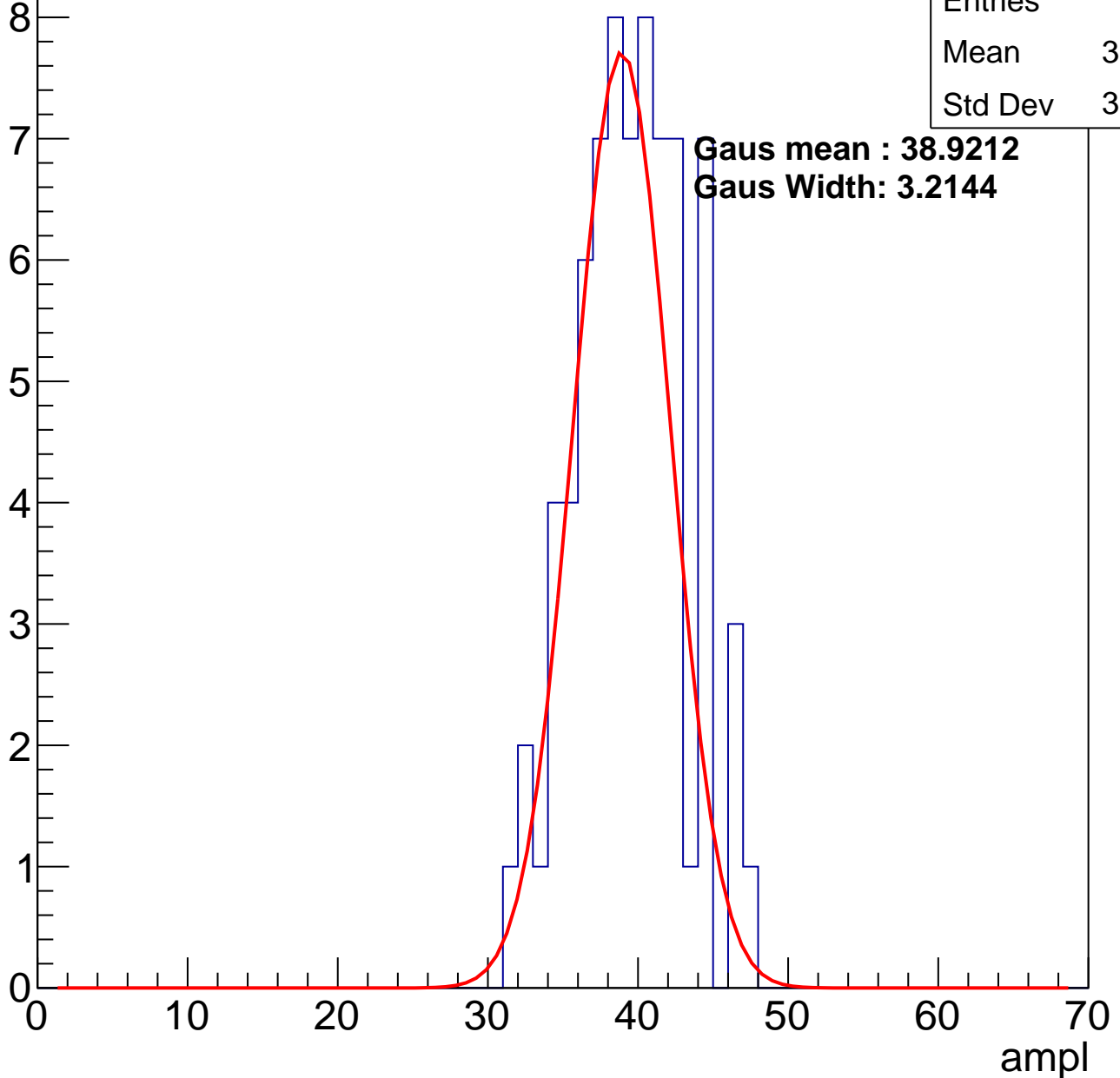
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	39.09
Std Dev	3.587

**Gaus mean : 38.9212**

**Gaus Width: 3.2144**



# B0L001S, U21-ch36, adc2

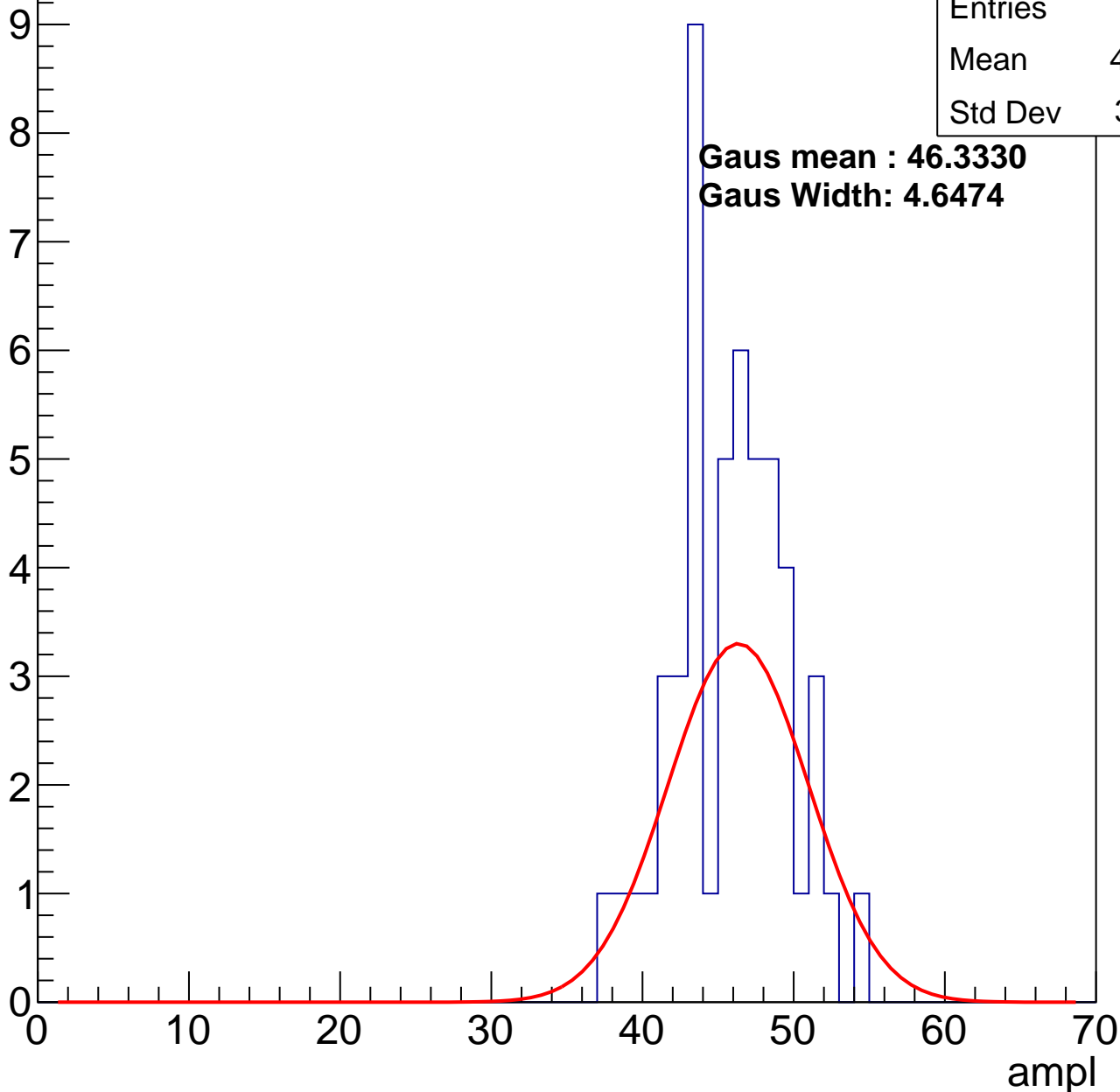
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	45.39
Std Dev	3.641

**Gaus mean : 46.3330**

**Gaus Width: 4.6474**

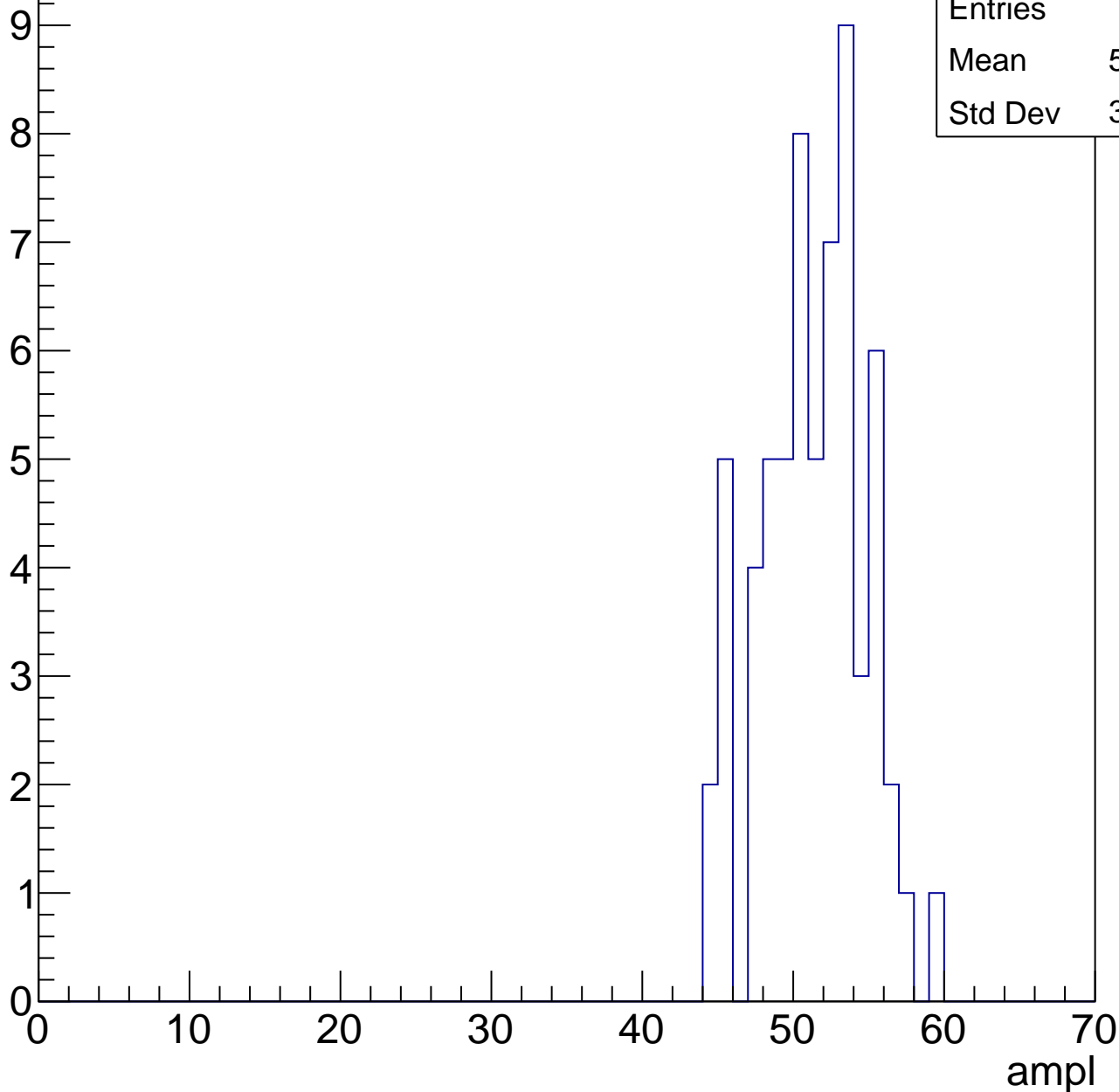


# B0L001S, U21-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

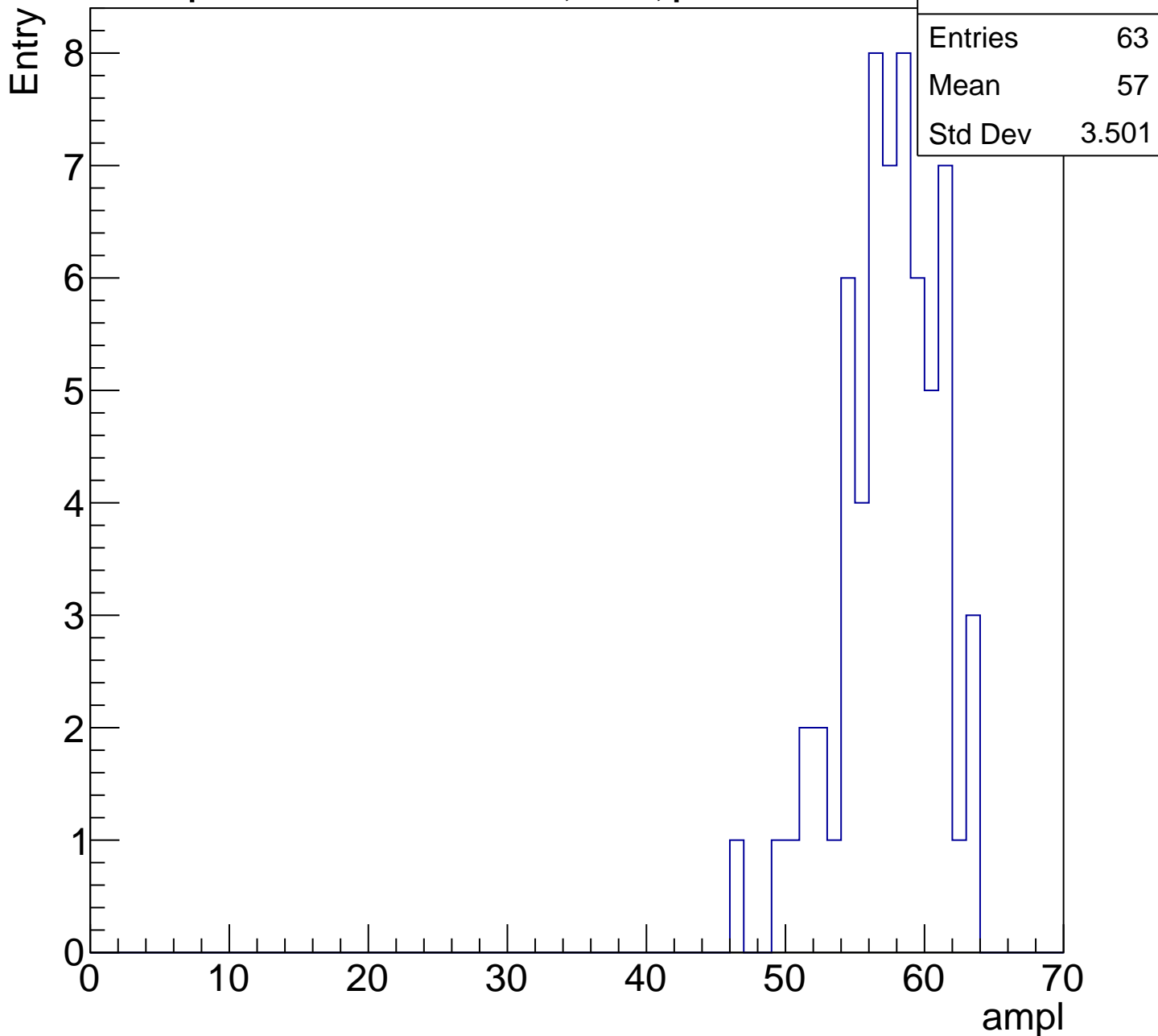
Entry

Entries	63
Mean	50.83
Std Dev	3.402



# B0L001S, U21-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

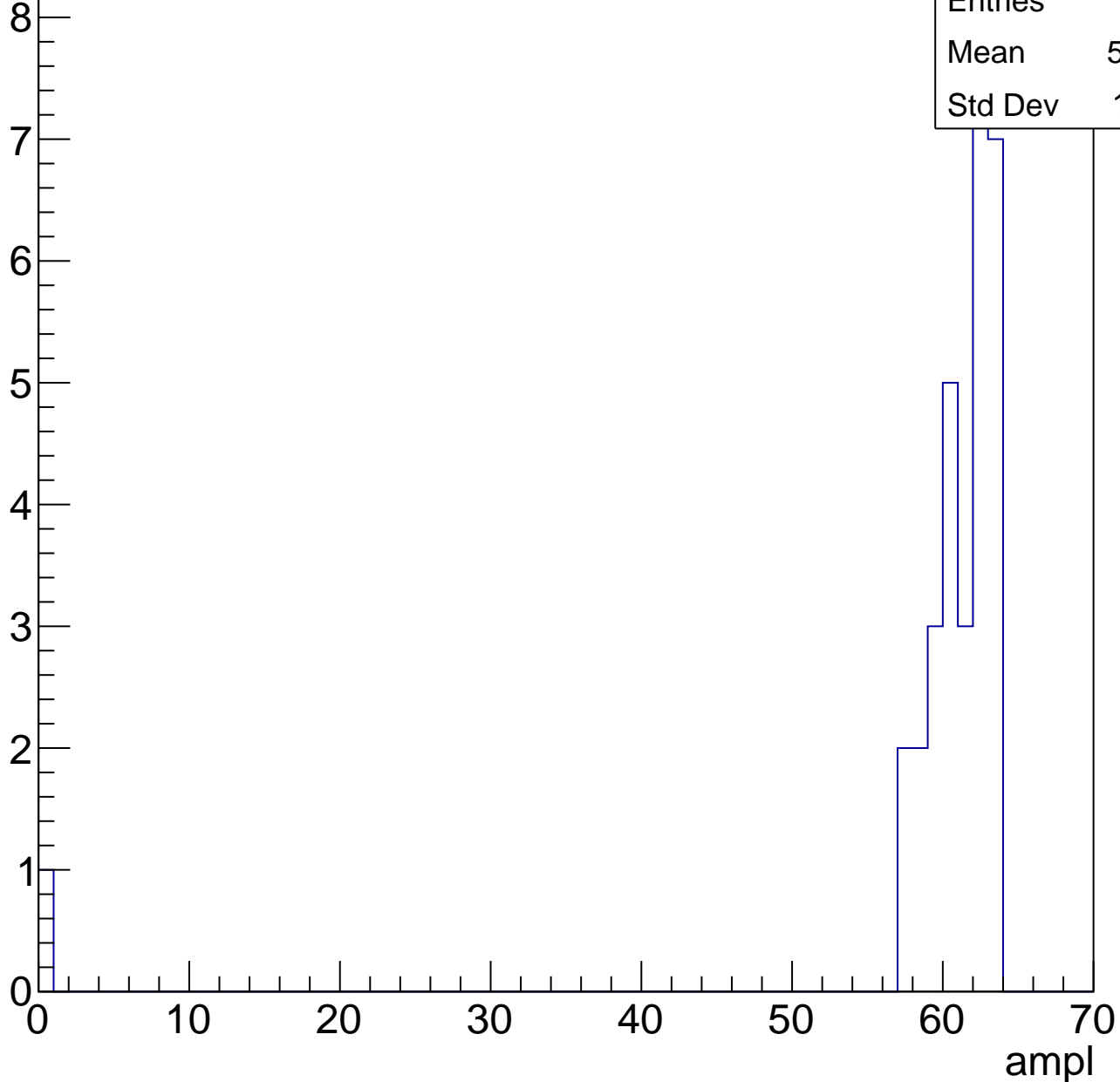


# B0L001S, U21-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	31
Mean	58.94
Std Dev	10.91



# B0L001S, U21-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	62
Std Dev	0



# B0L001S, U21-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U21-ch37, adc0

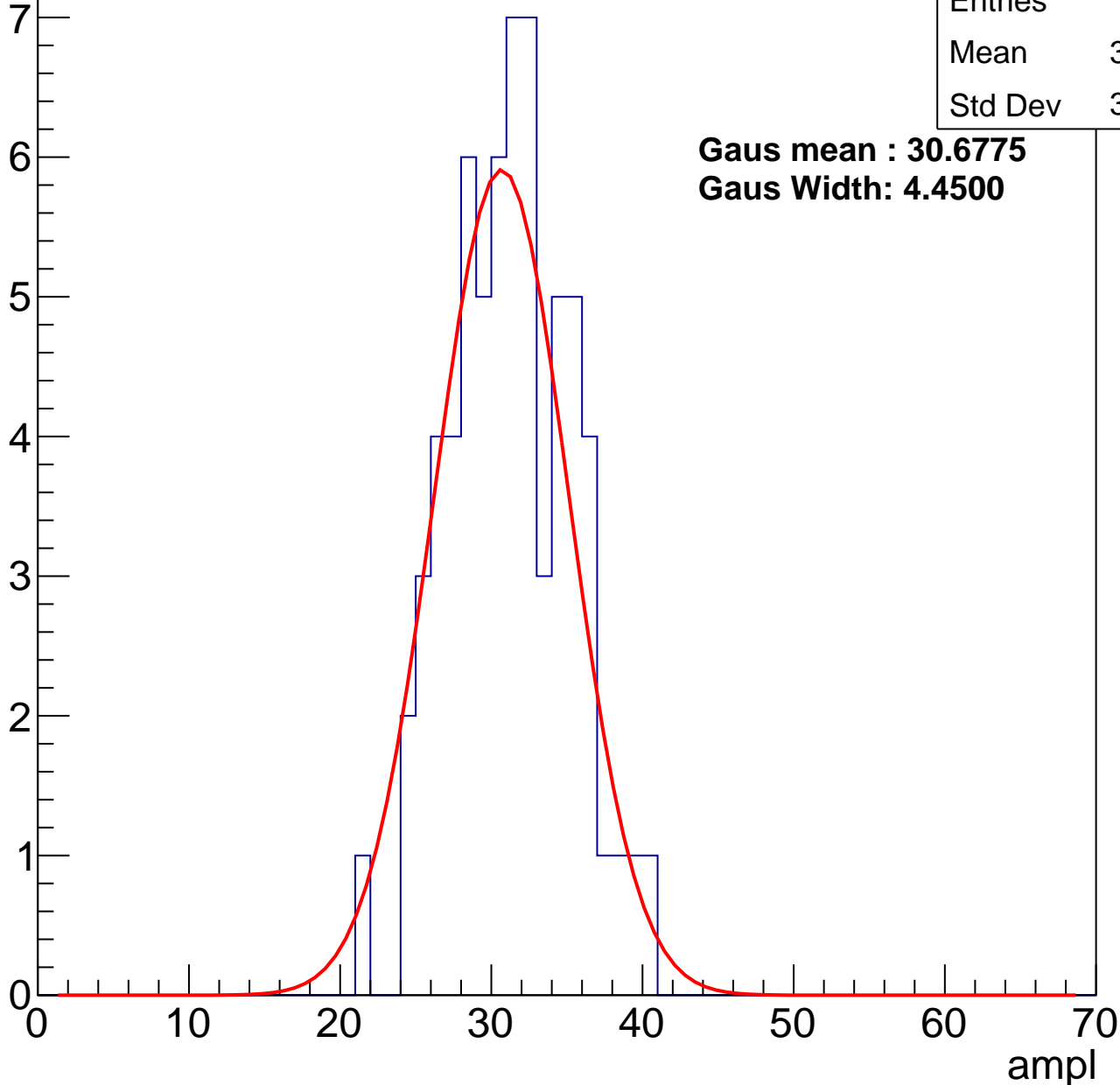
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	30.79
Std Dev	3.933

**Gaus mean : 30.6775**

**Gaus Width: 4.4500**



# B0L001S, U21-ch37, adc1

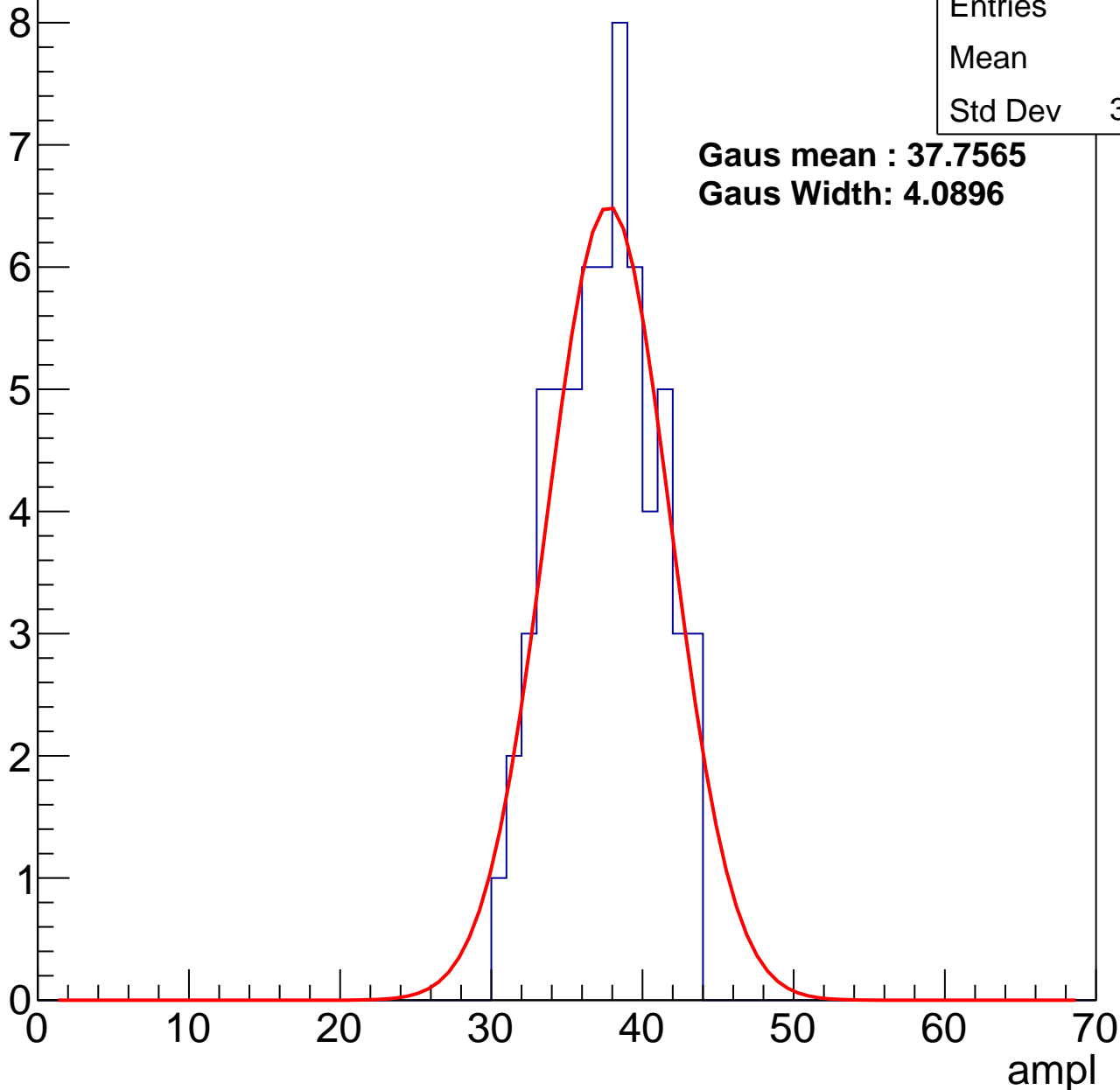
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	37
Std Dev	3.307

**Gaus mean : 37.7565**

**Gaus Width: 4.0896**



# B0L001S, U21-ch37, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	73
Mean	43.58
Std Dev	3.667

**Gaus mean : 44.3366**

**Gaus Width: 3.2329**

Entry

10  
8  
6  
4  
2  
0

ampl

0

10

20

30

40

50

60

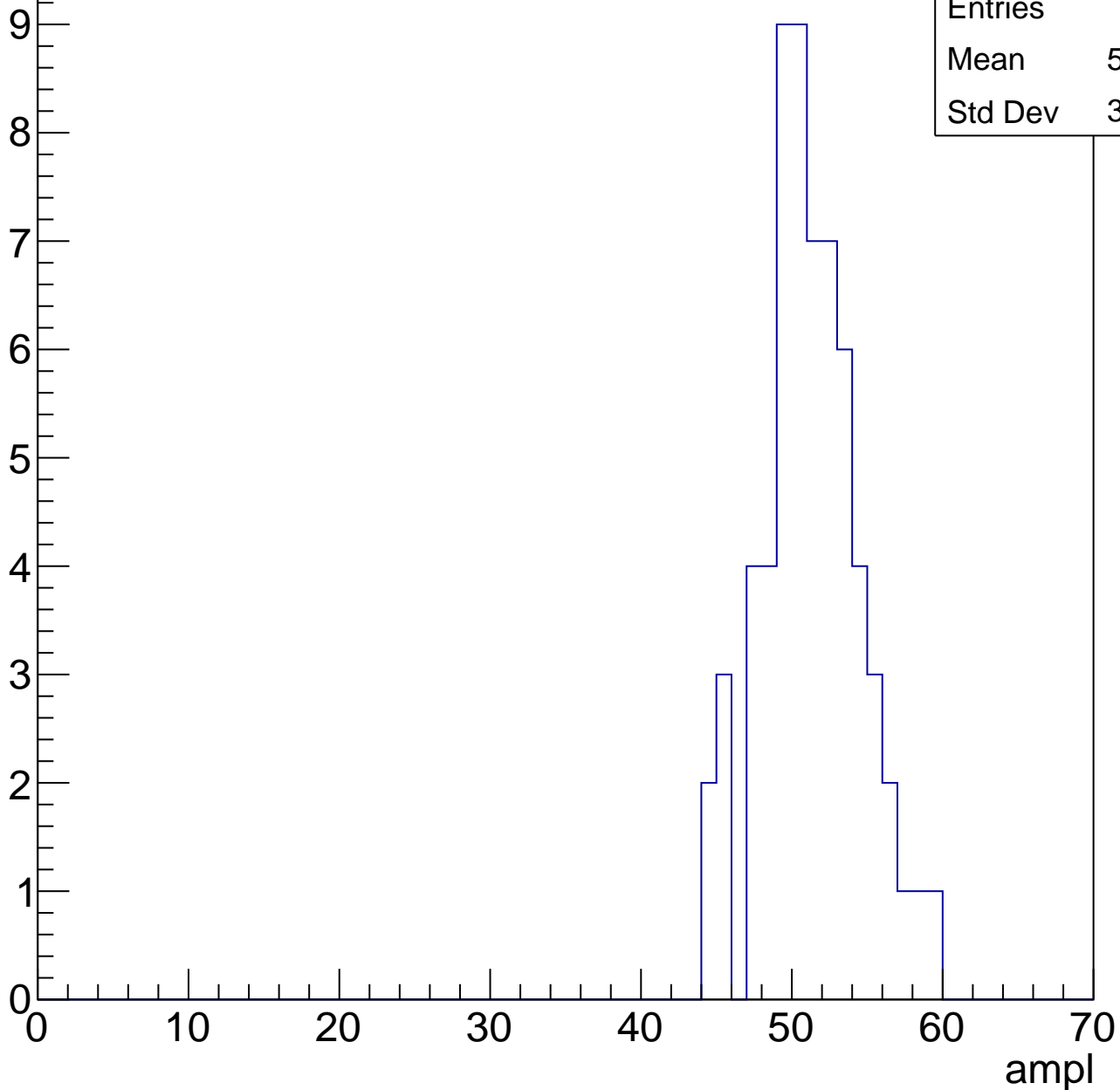
70

# B0L001S, U21-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	50.79
Std Dev	3.242

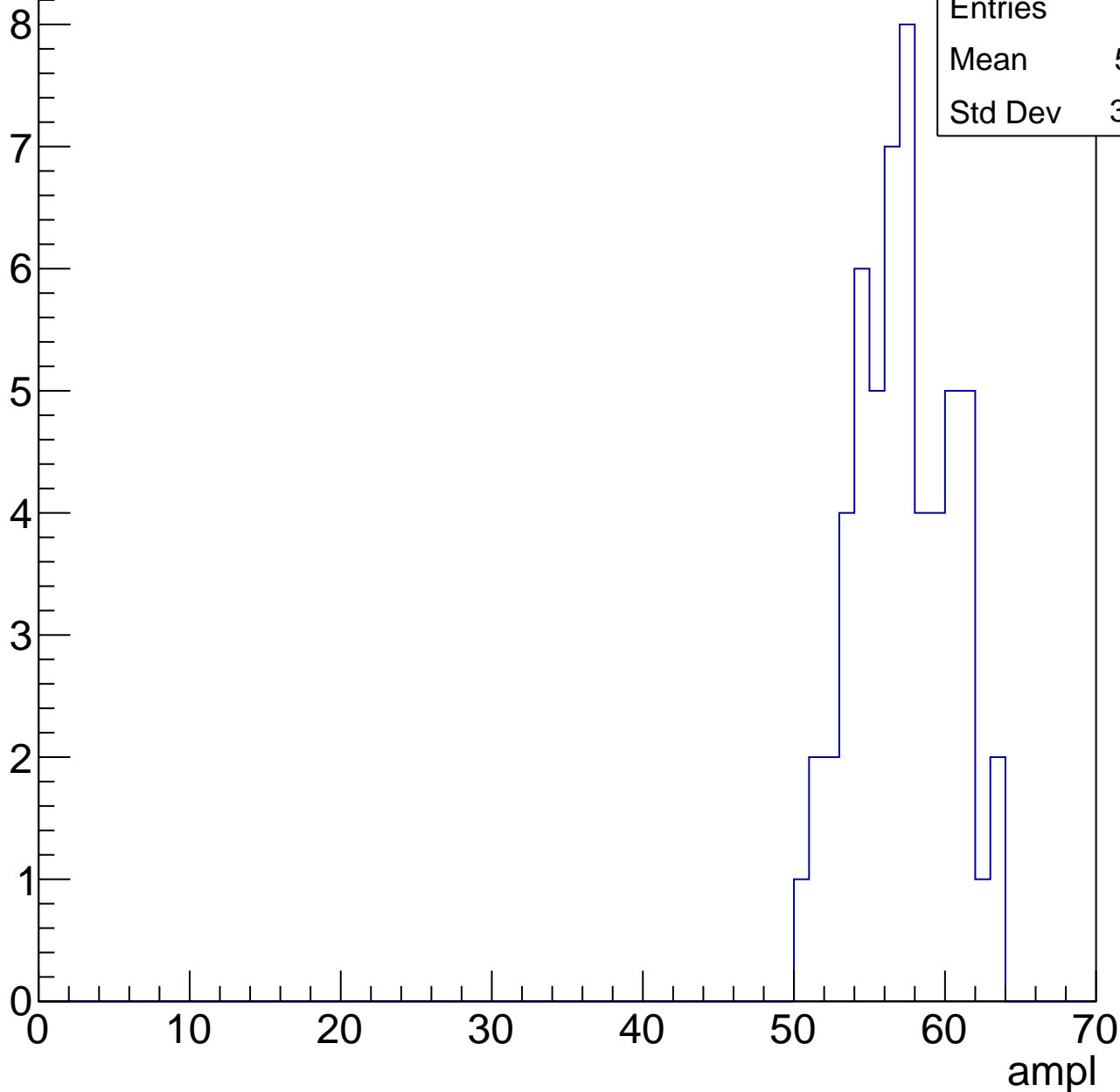


# B0L001S, U21-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	56.71
Std Dev	3.144

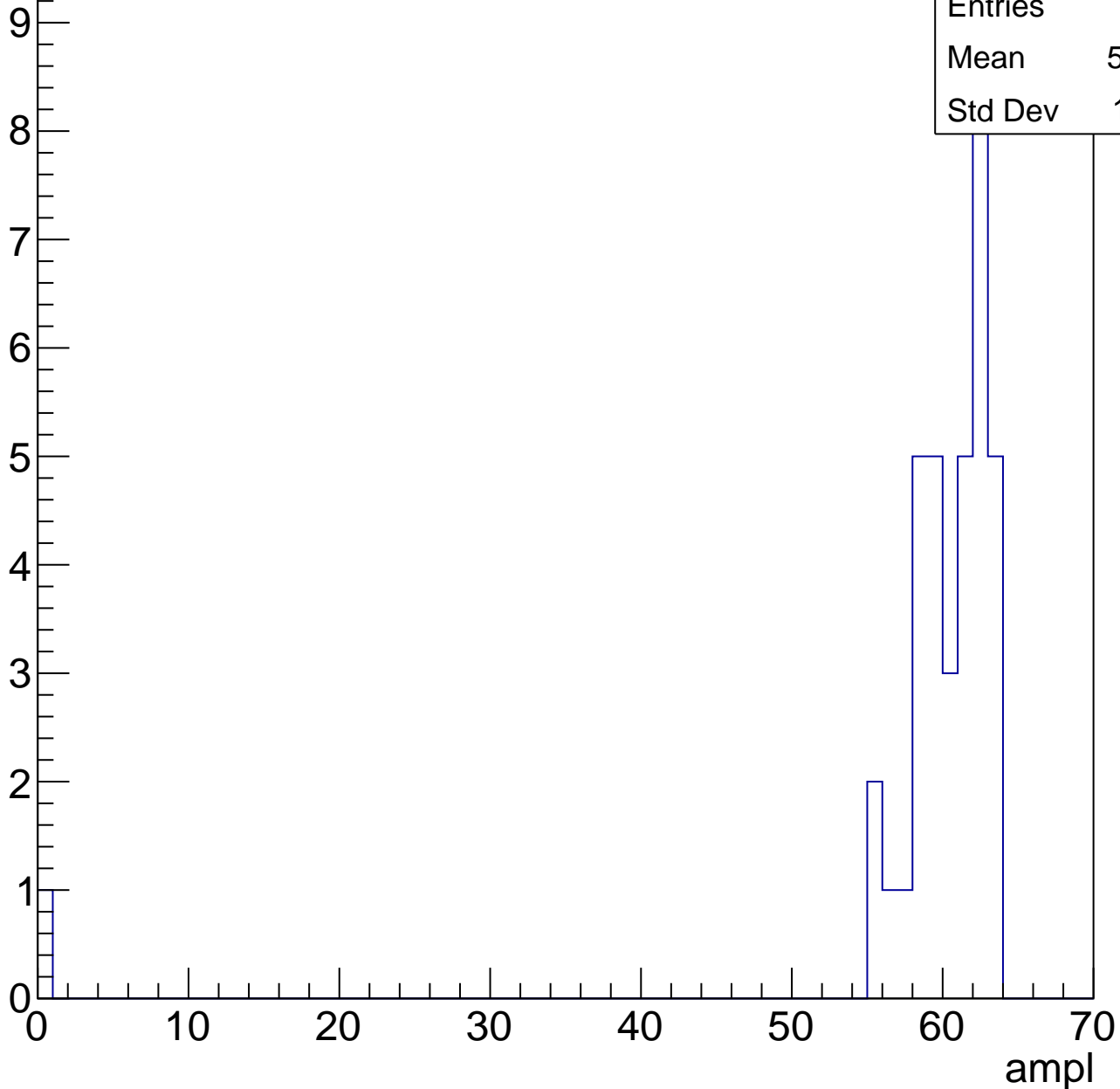


# B0L001S, U21-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

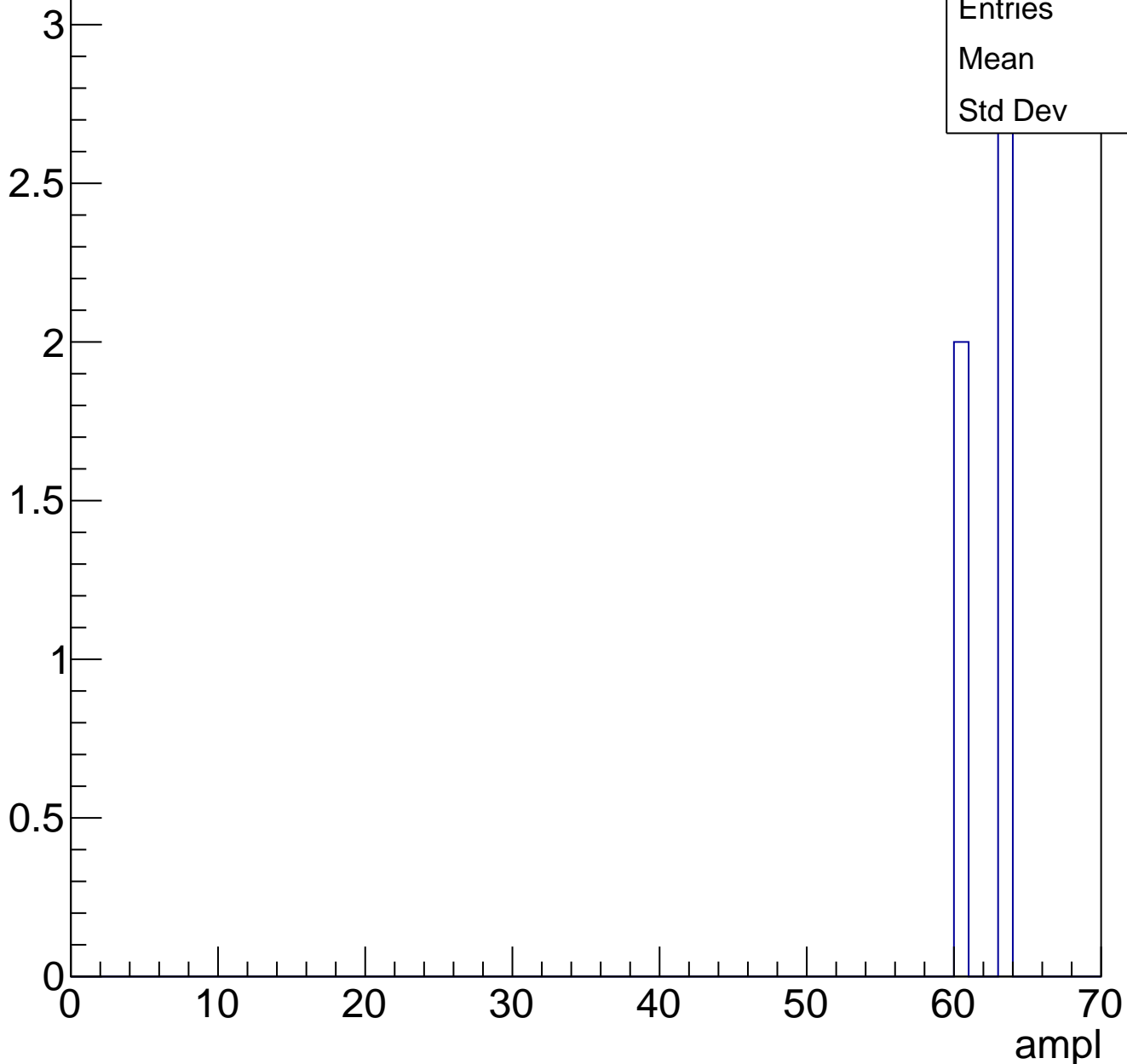
Entries	37
Mean	58.54
Std Dev	10.01



# B0L001S, U21-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U21-ch38, adc0

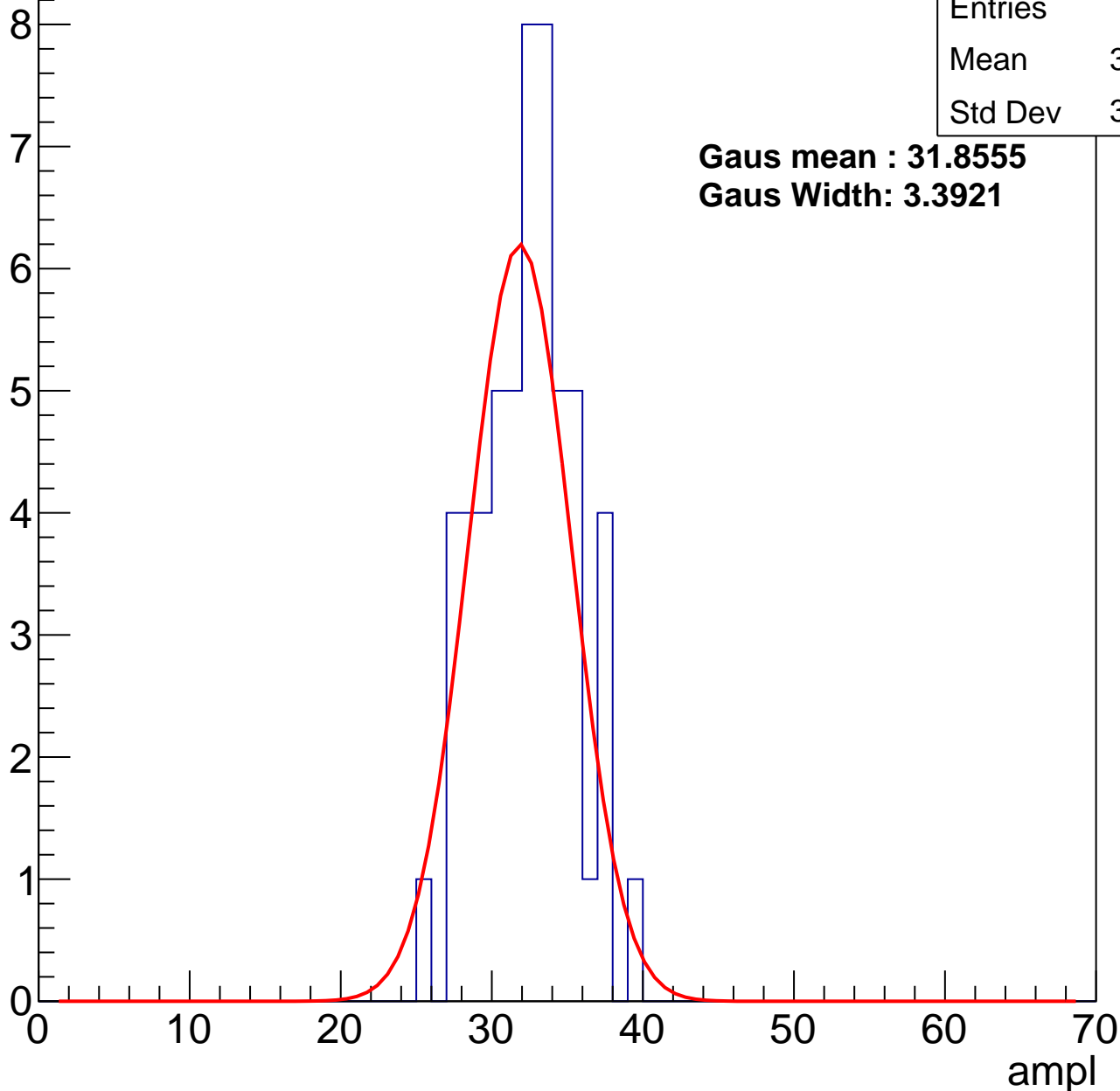
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	31.89
Std Dev	3.049

**Gaus mean : 31.8555**

**Gaus Width: 3.3921**



# B0L001S, U21-ch38, adc1

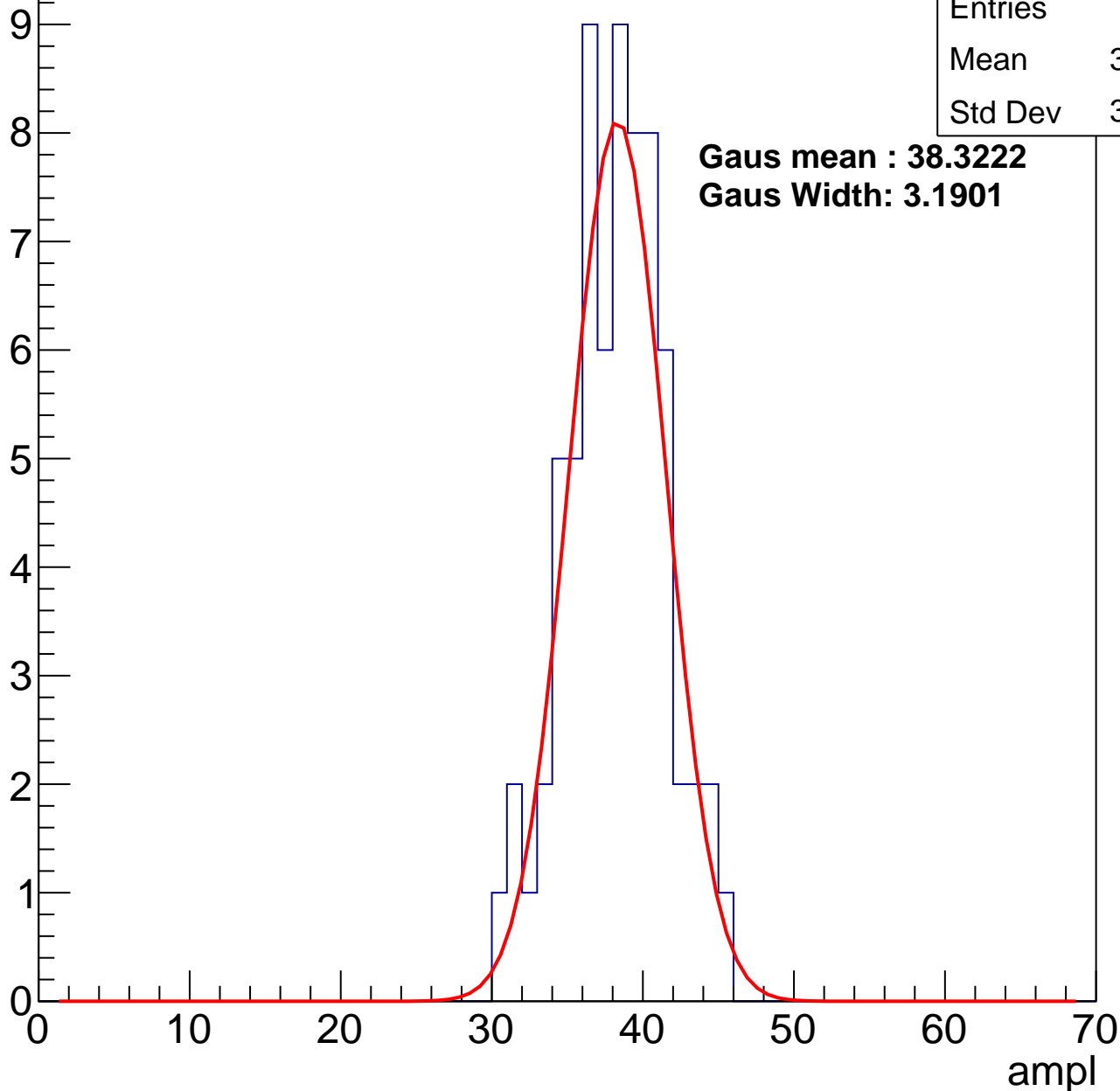
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	37.74
Std Dev	3.202

**Gaus mean : 38.3222**

**Gaus Width: 3.1901**



# B0L001S, U21-ch38, adc2

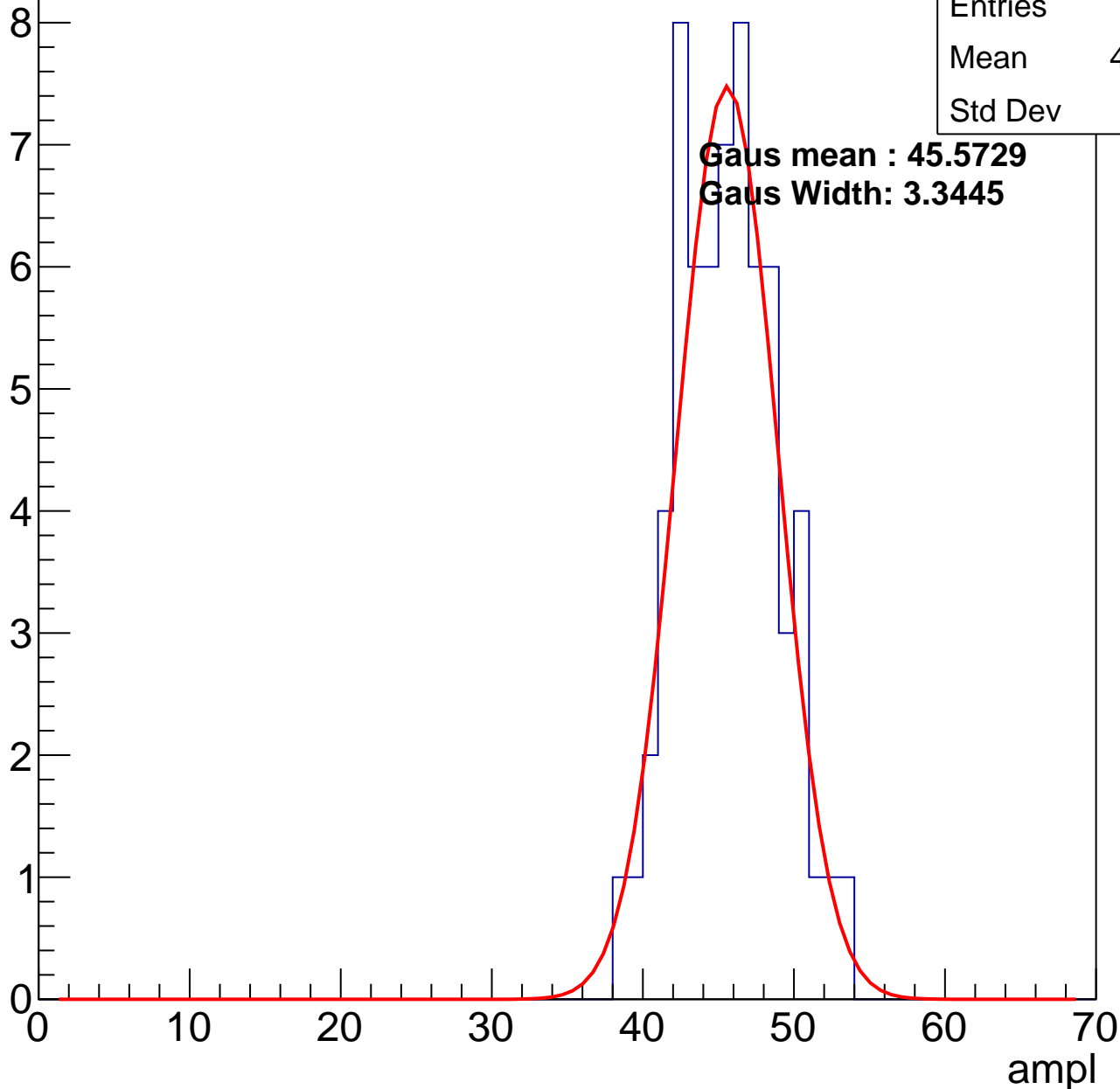
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	45.15
Std Dev	3.24

**Gaus mean : 45.5729**

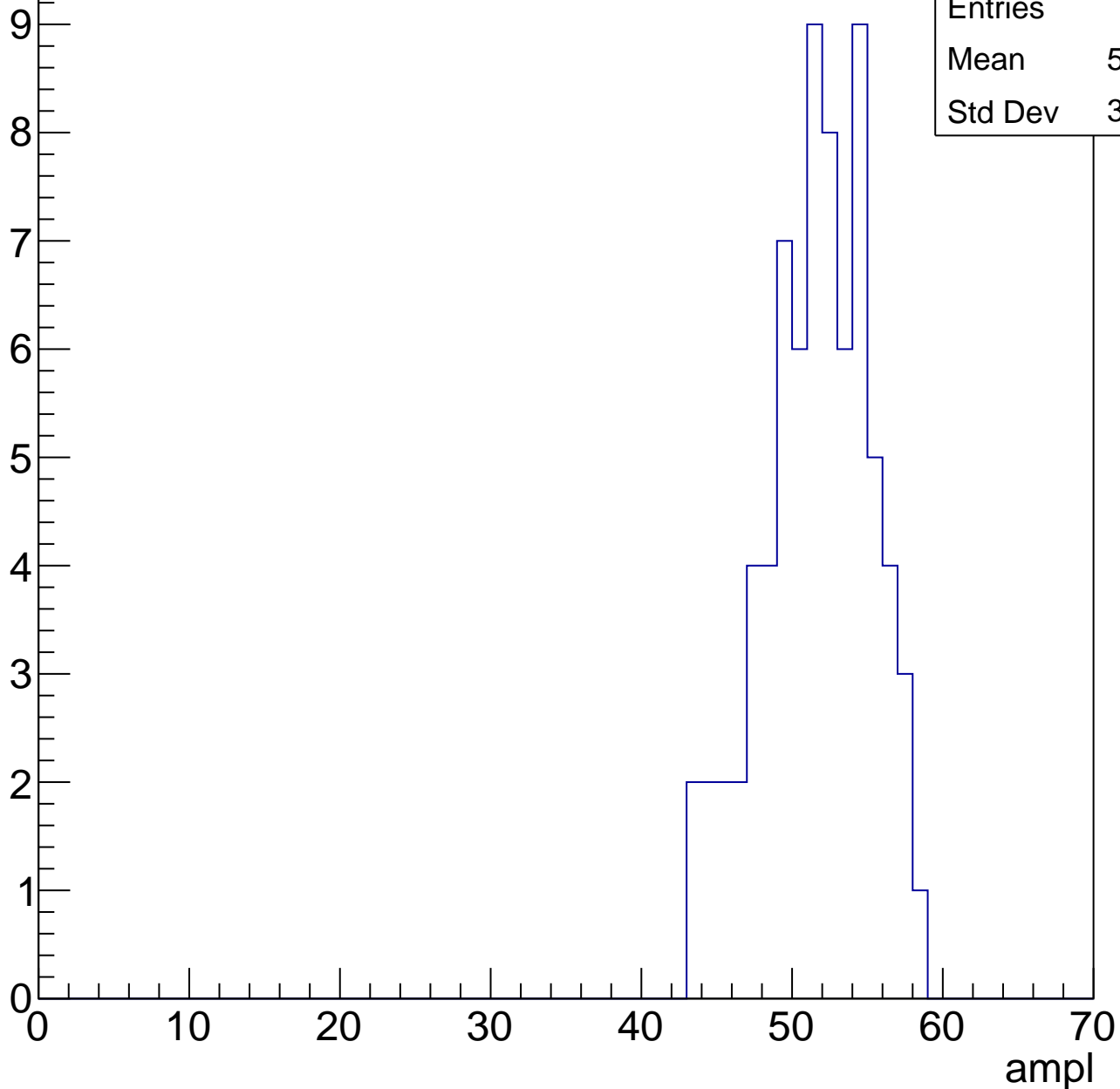
**Gaus Width: 3.3445**



# B0L001S, U21-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

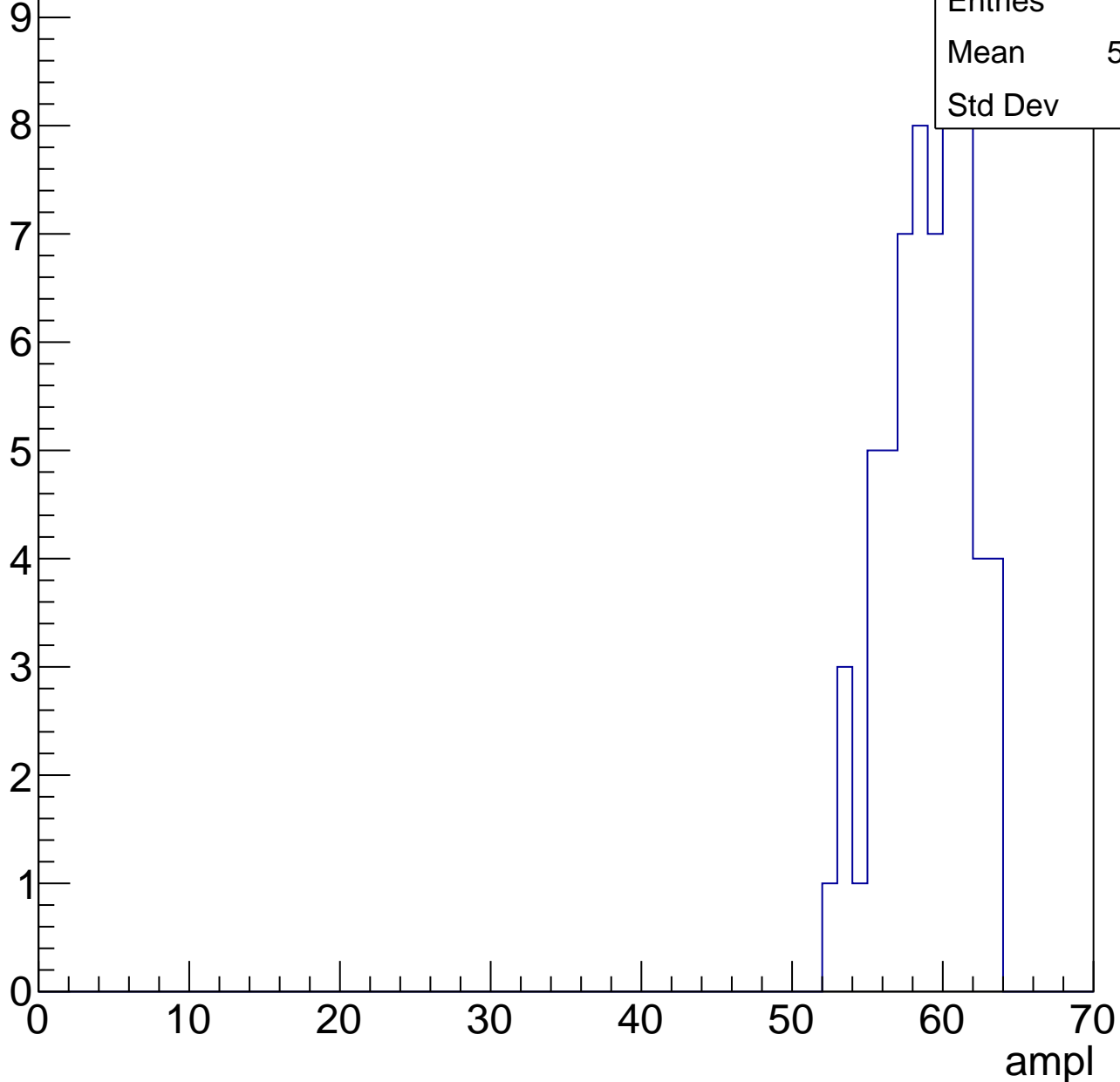


Entries	74
Mean	51.16
Std Dev	3.545

# B0L001S, U21-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

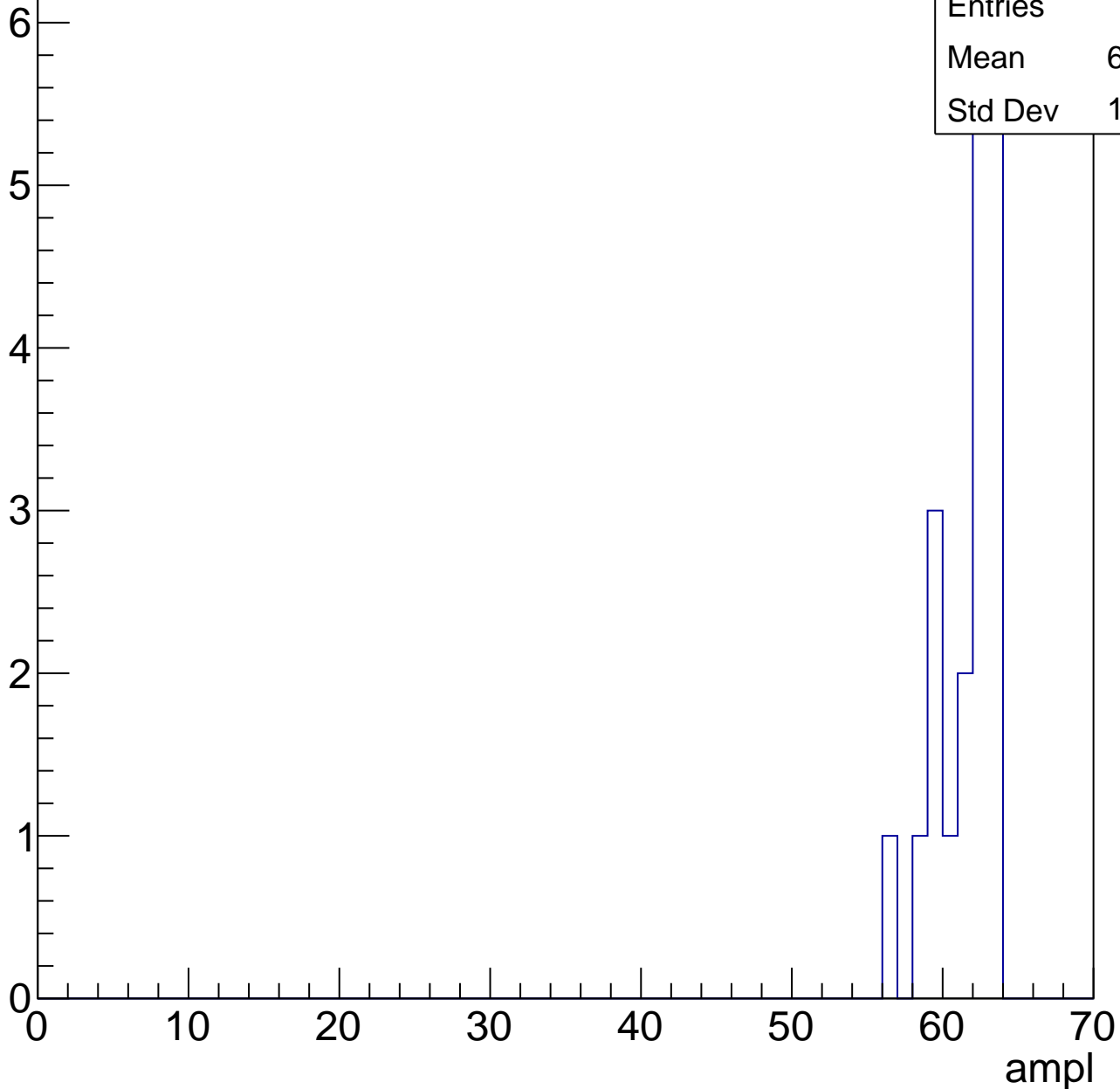


# B0L001S, U21-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	20
Mean	61.15
Std Dev	1.956



# B0L001S, U21-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

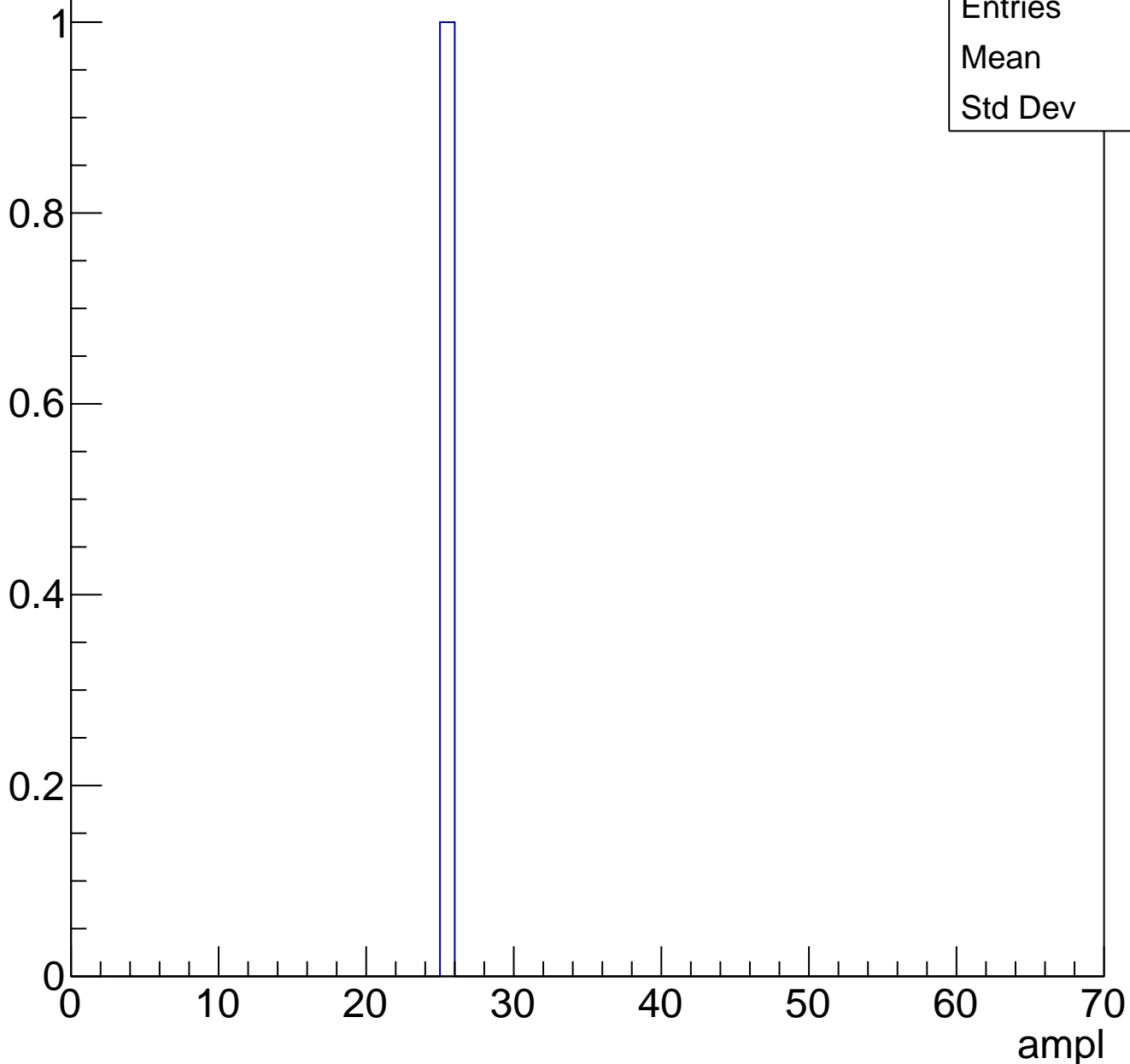




# B0L001S, U21-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	25
Std Dev	0

# B0L001S, U21-ch39, adc0

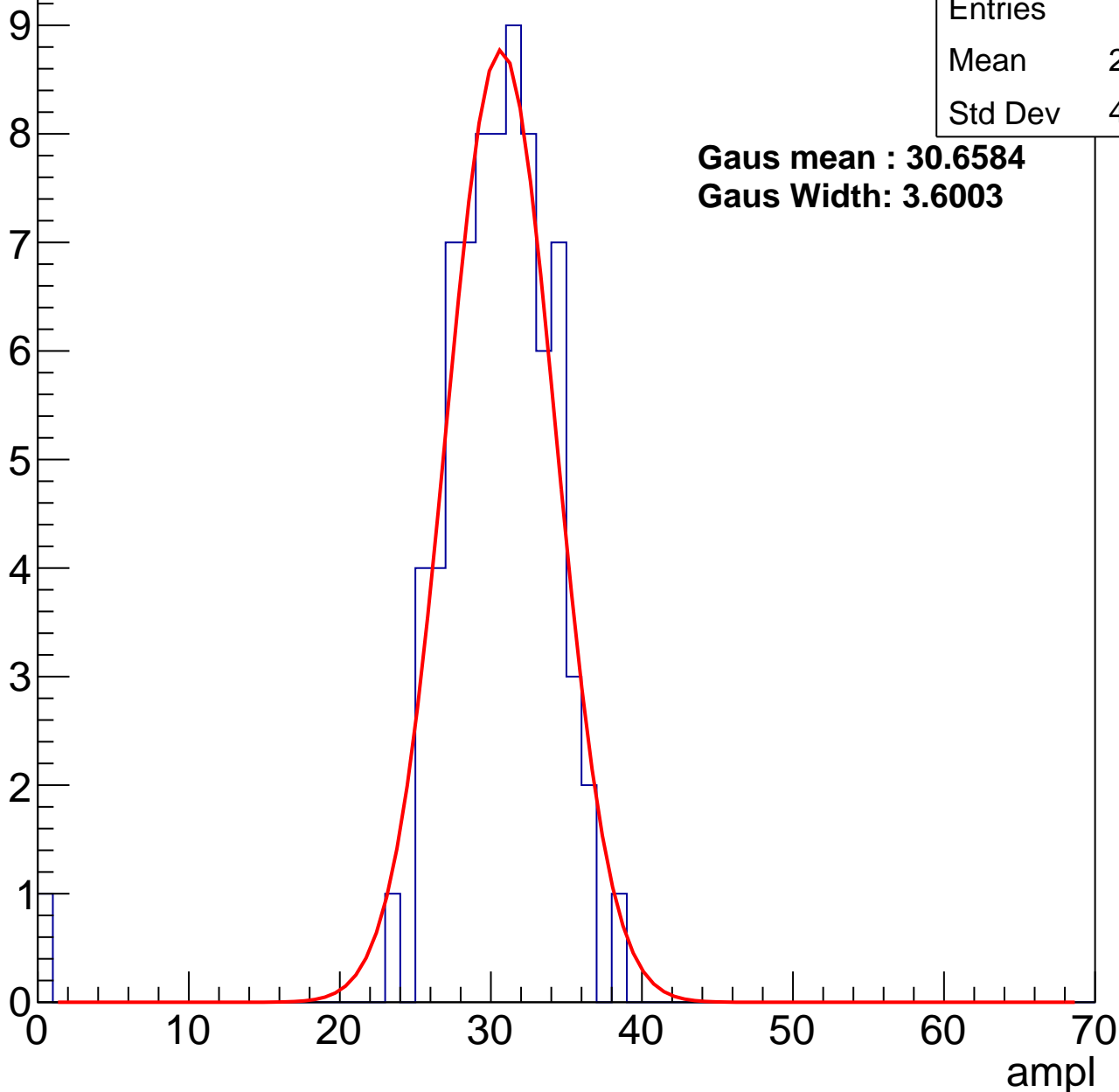
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	29.87
Std Dev	4.629

**Gaus mean : 30.6584**

**Gaus Width: 3.6003**

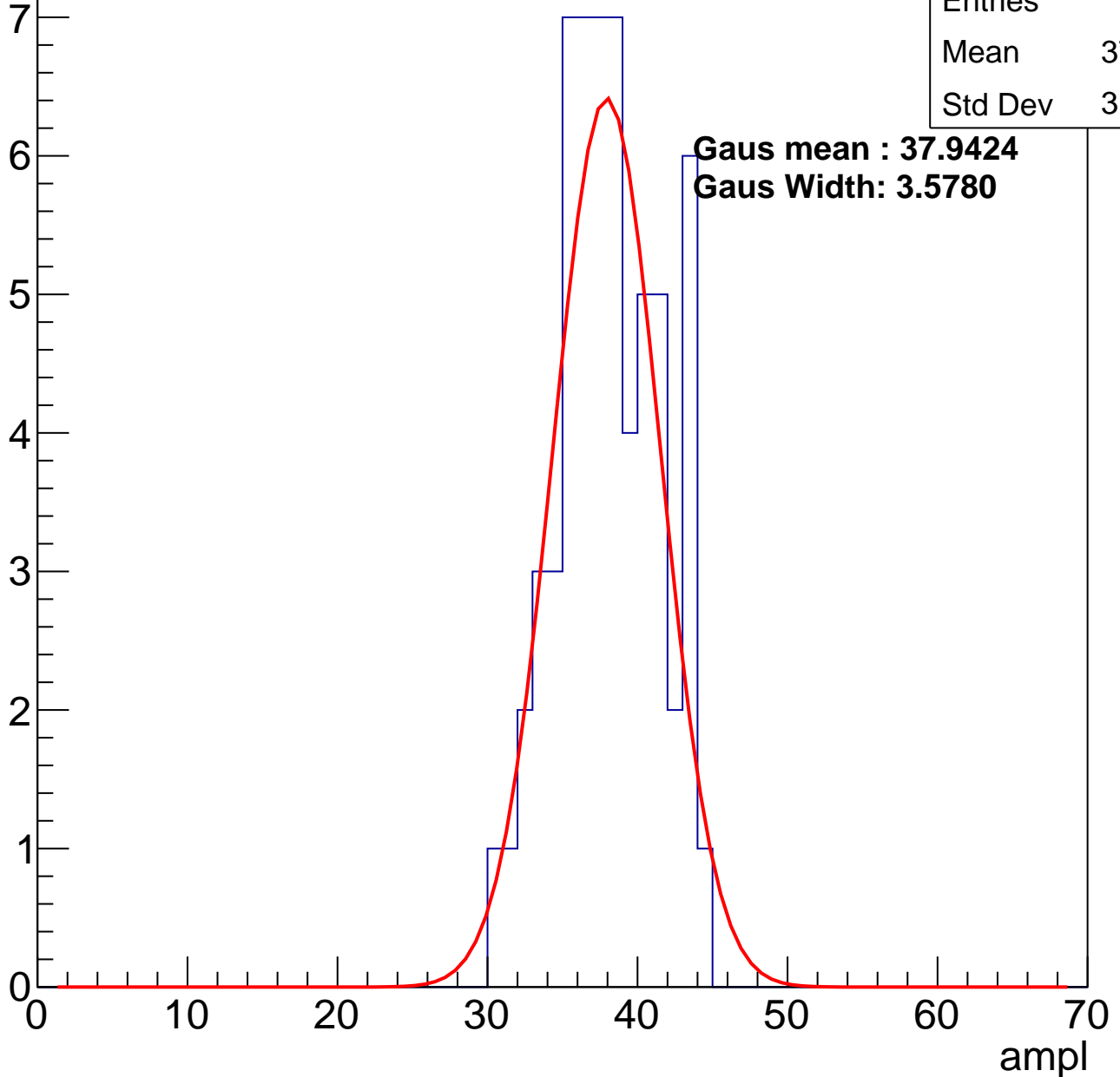


# B0L001S, U21-ch39, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	37.62
Std Dev	3.349



# B0L001S, U21-ch39, adc2

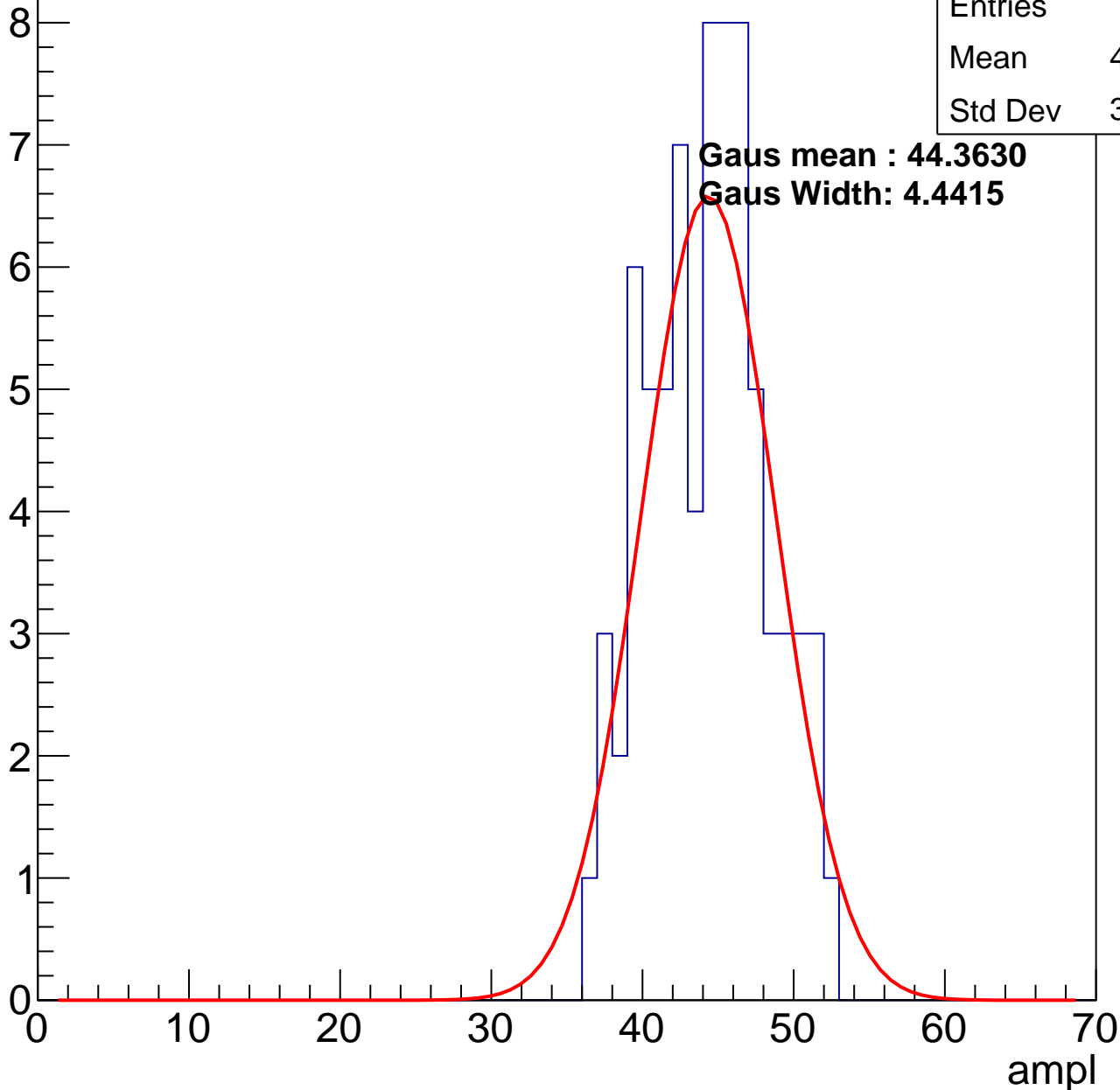
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	43.85
Std Dev	3.856

**Gaus mean : 44.3630**

**Gaus Width: 4.4415**

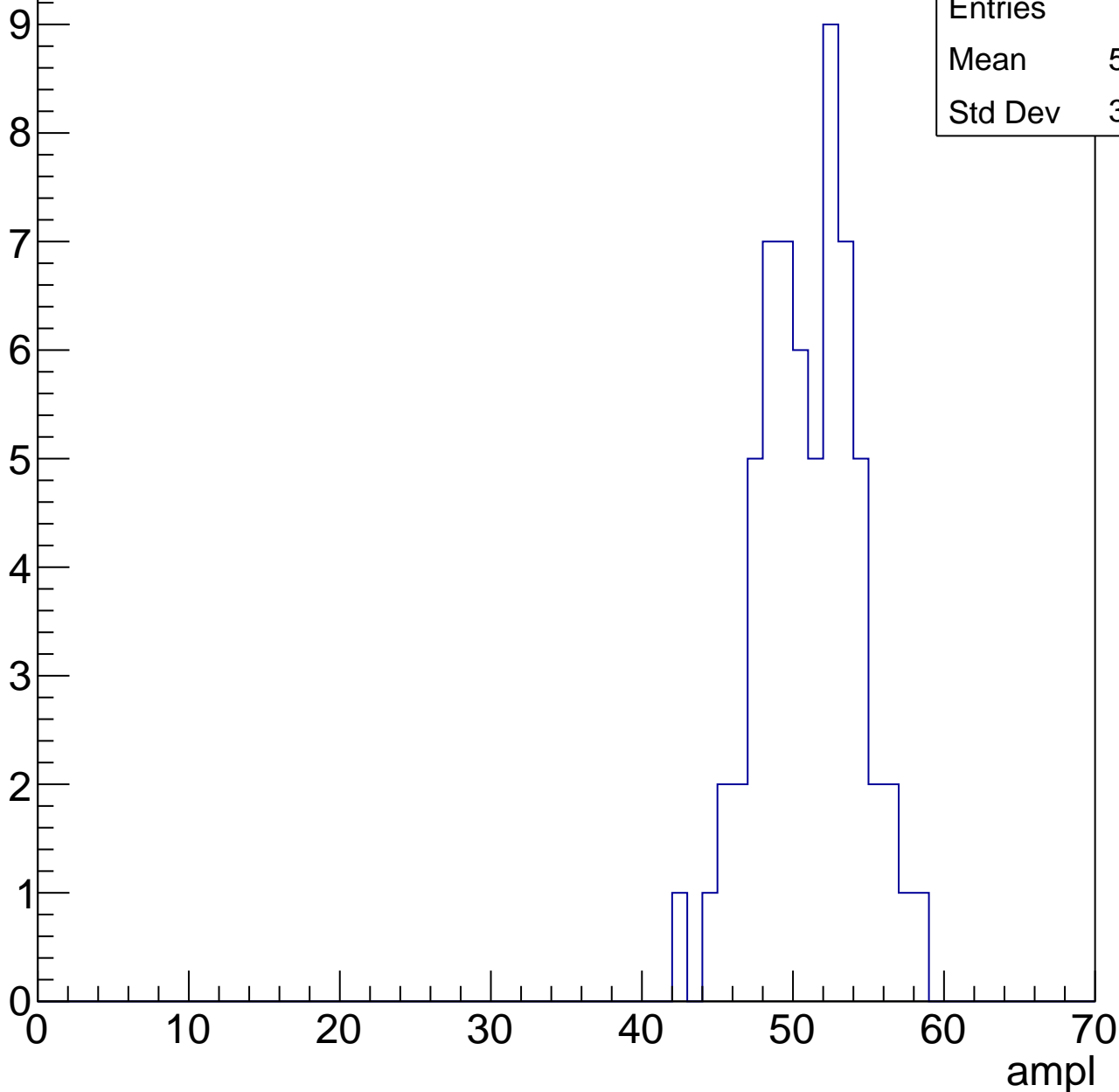


# B0L001S, U21-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	50.52
Std Dev	3.246

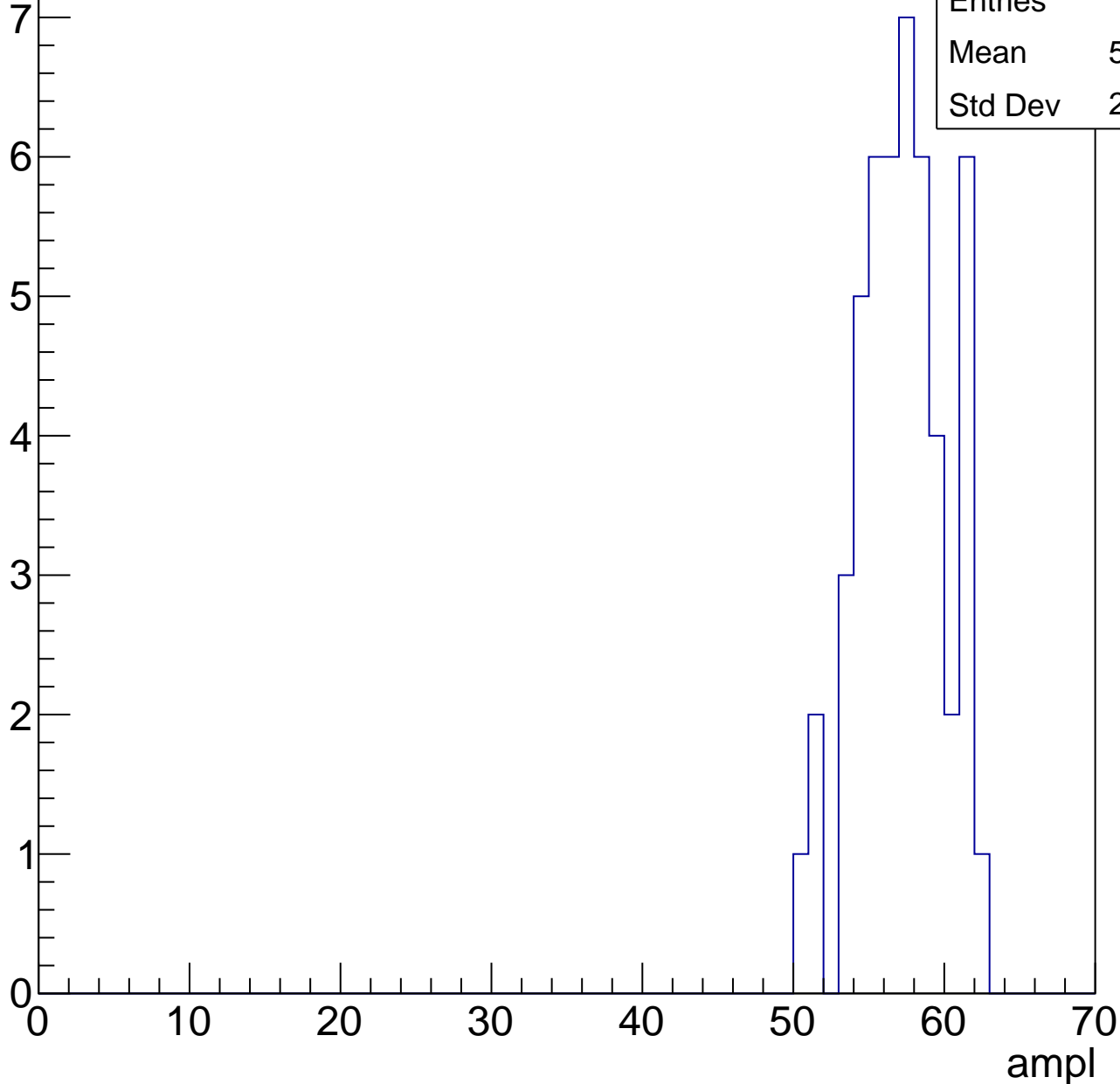


# B0L001S, U21-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

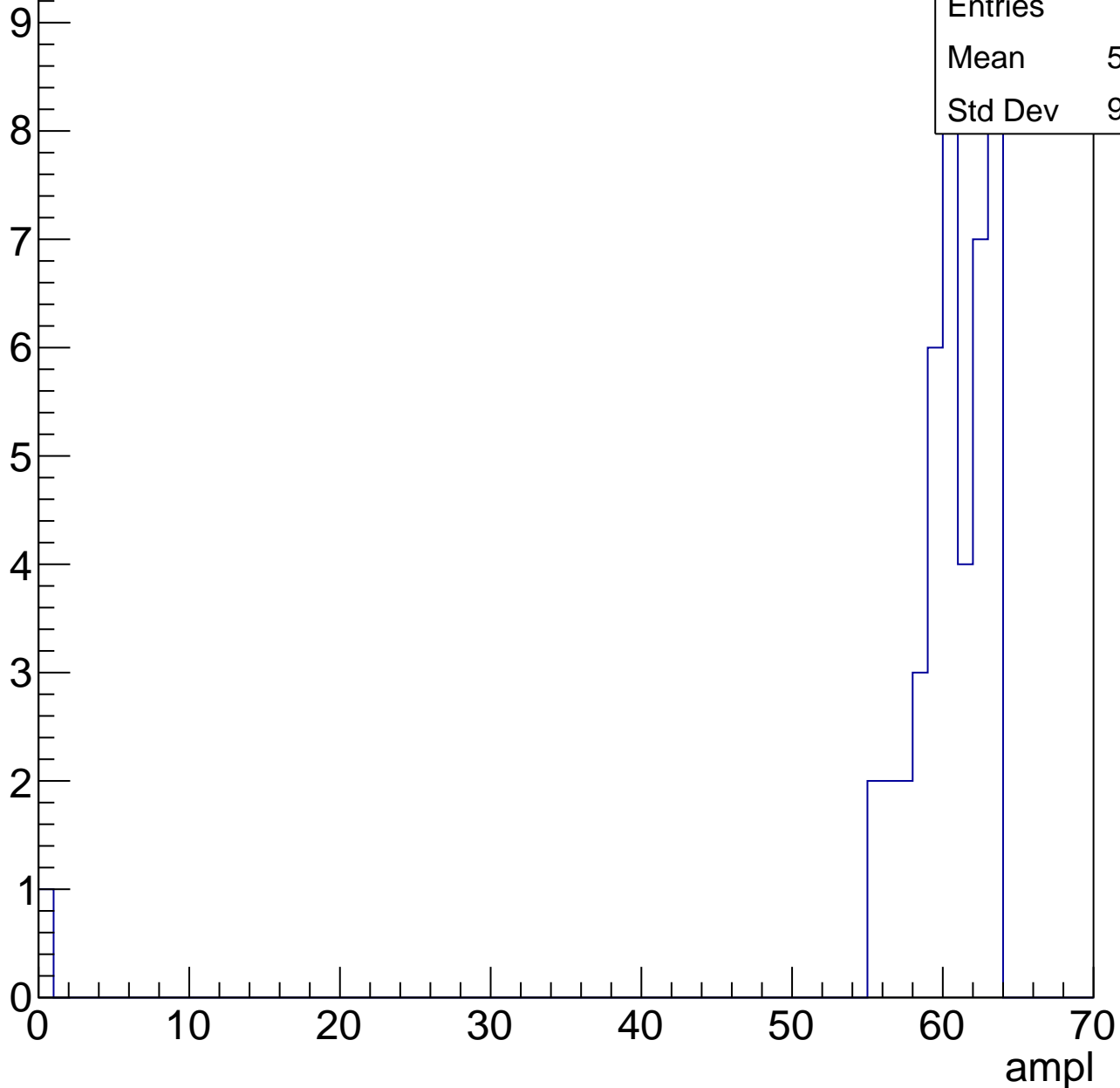
Entries	49
Mean	56.69
Std Dev	2.859



# B0L001S, U21-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B0L001S, U21-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch40, adc0

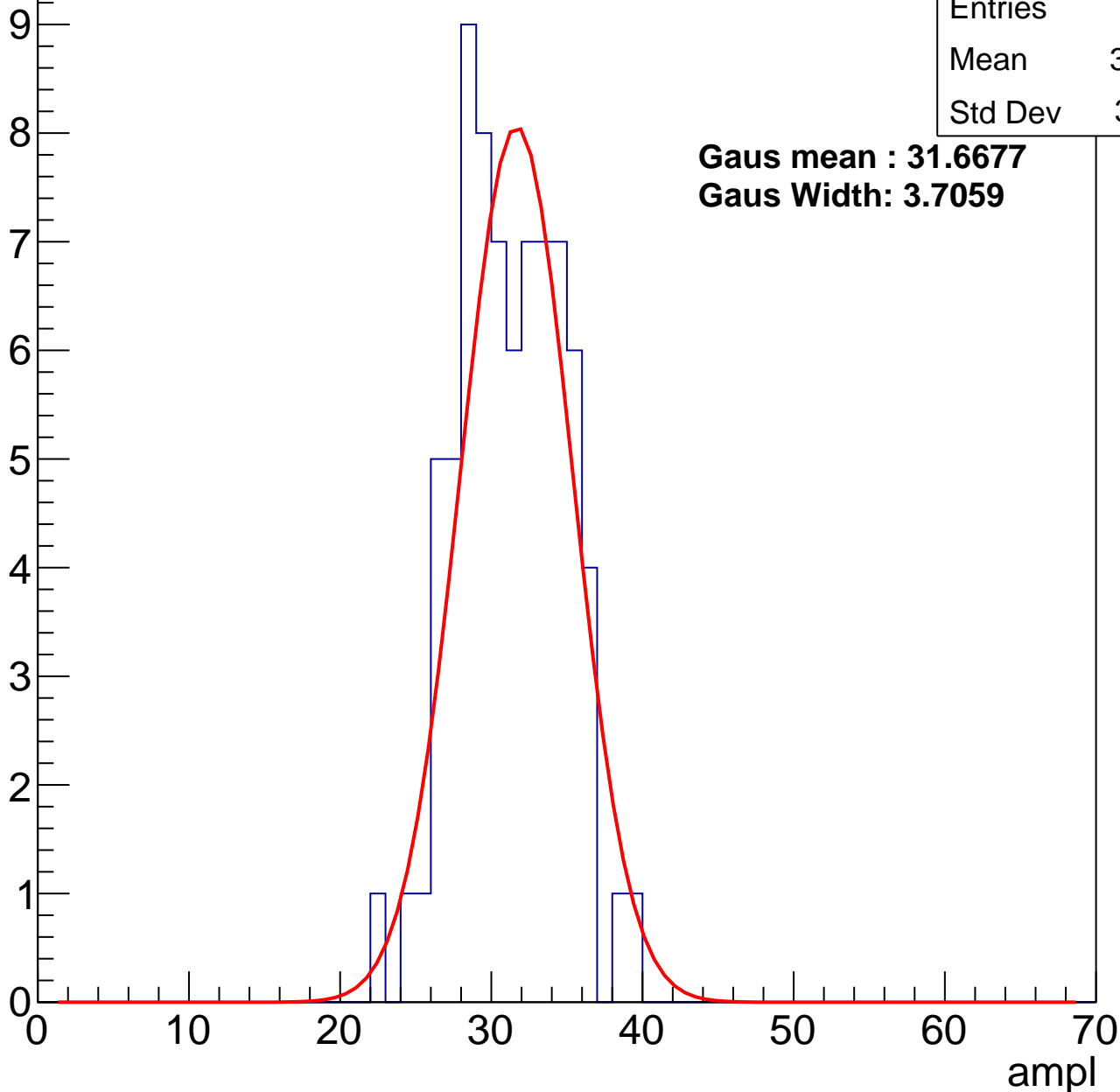
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	30.79
Std Dev	3.431

**Gaus mean : 31.6677**

**Gaus Width: 3.7059**



# B0L001S, U21-ch40, adc1

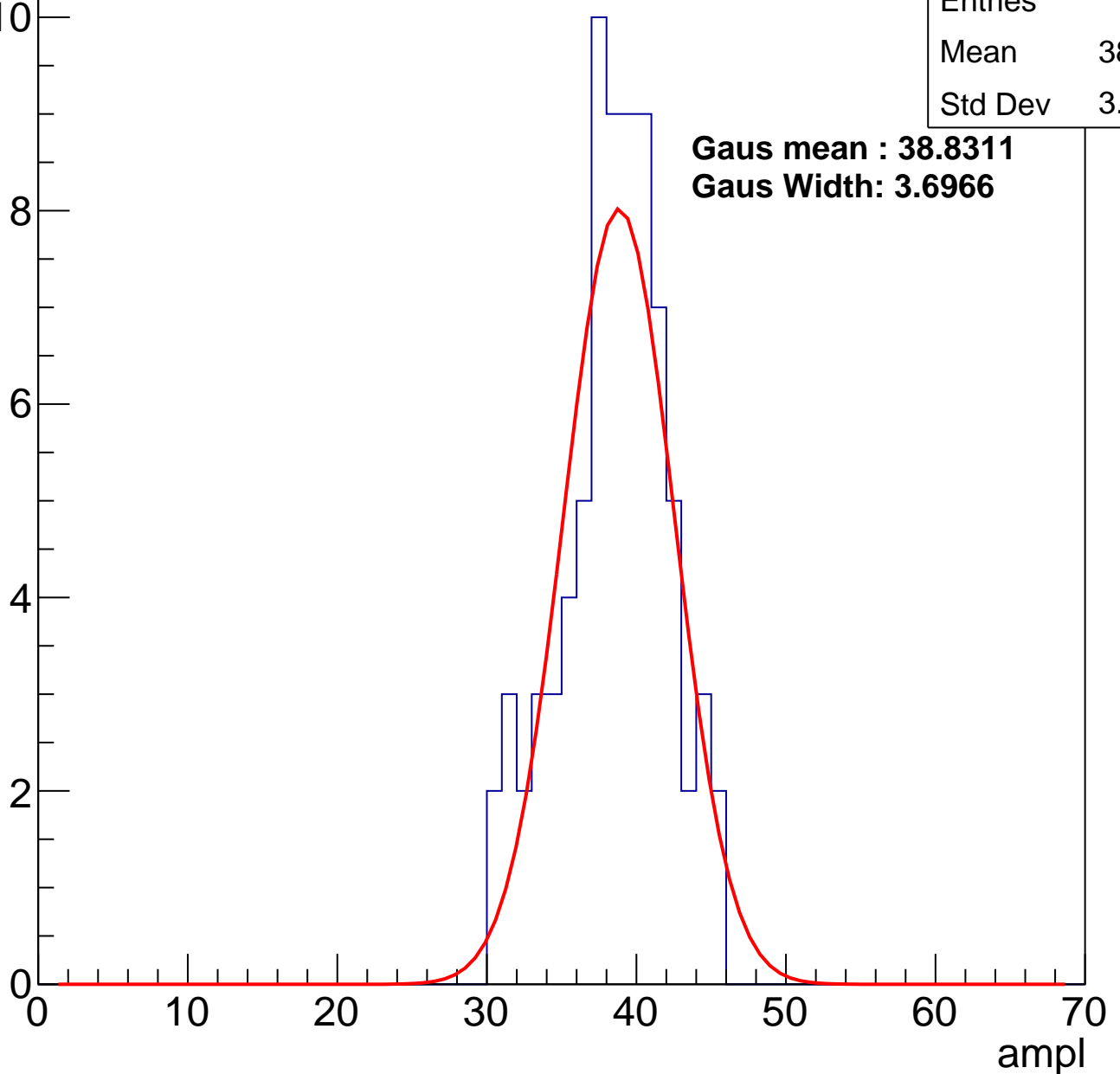
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	38.03
Std Dev	3.544

**Gaus mean : 38.8311**

**Gaus Width: 3.6966**



# B0L001S, U21-ch40, adc2

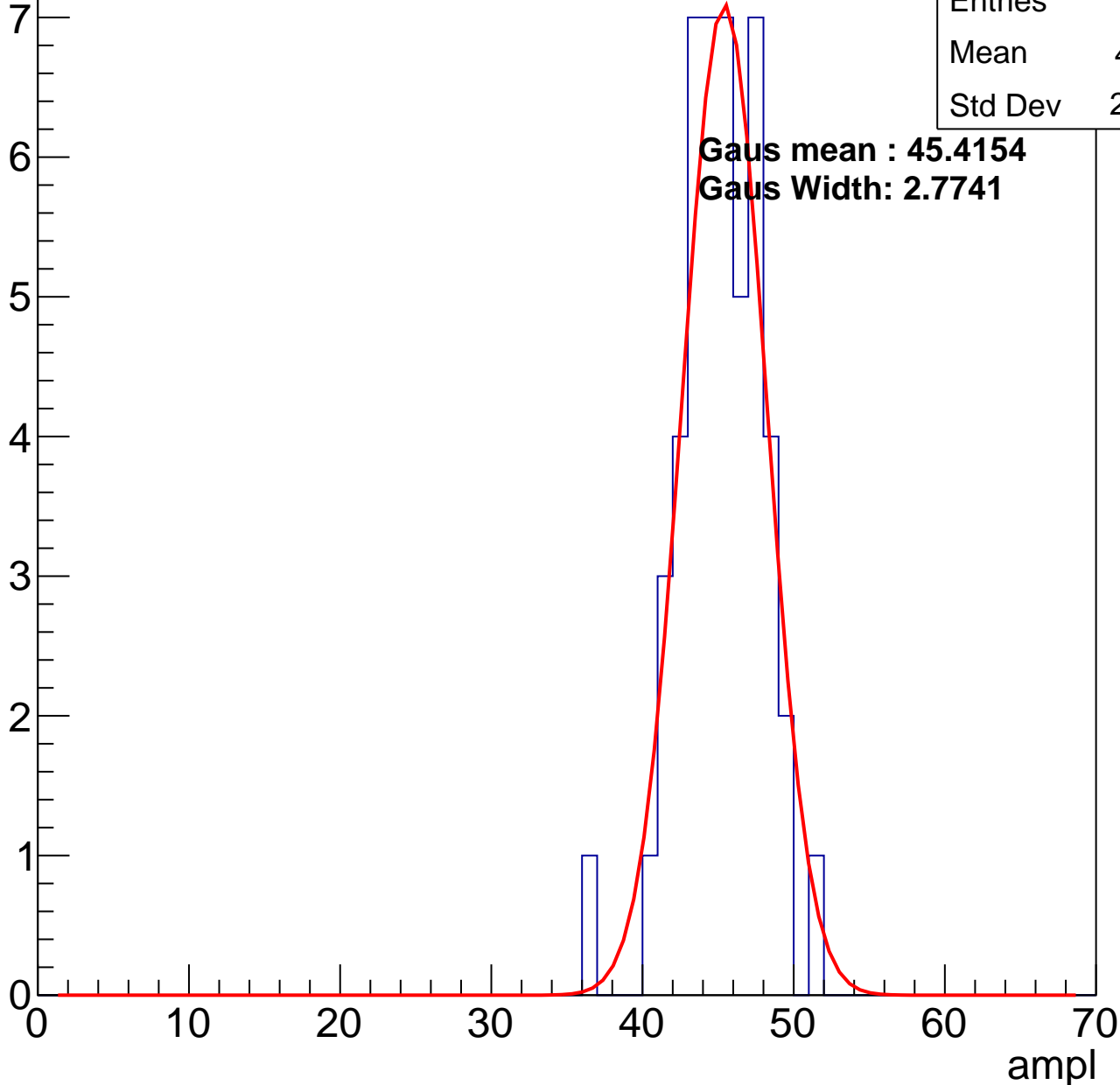
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	44.71
Std Dev	2.703

**Gaus mean : 45.4154**

**Gaus Width: 2.7741**

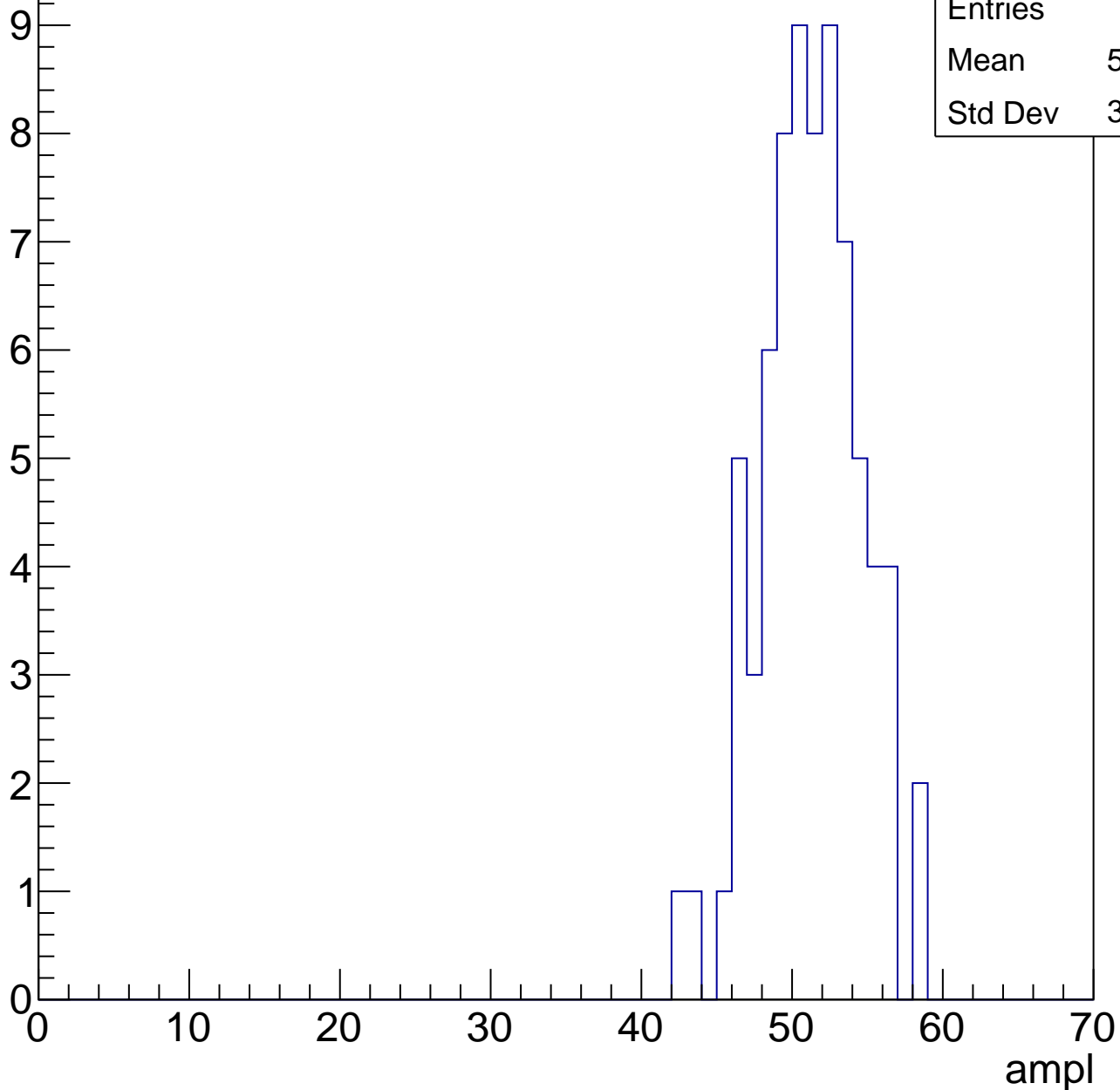


# B0L001S, U21-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	50.79
Std Dev	3.289

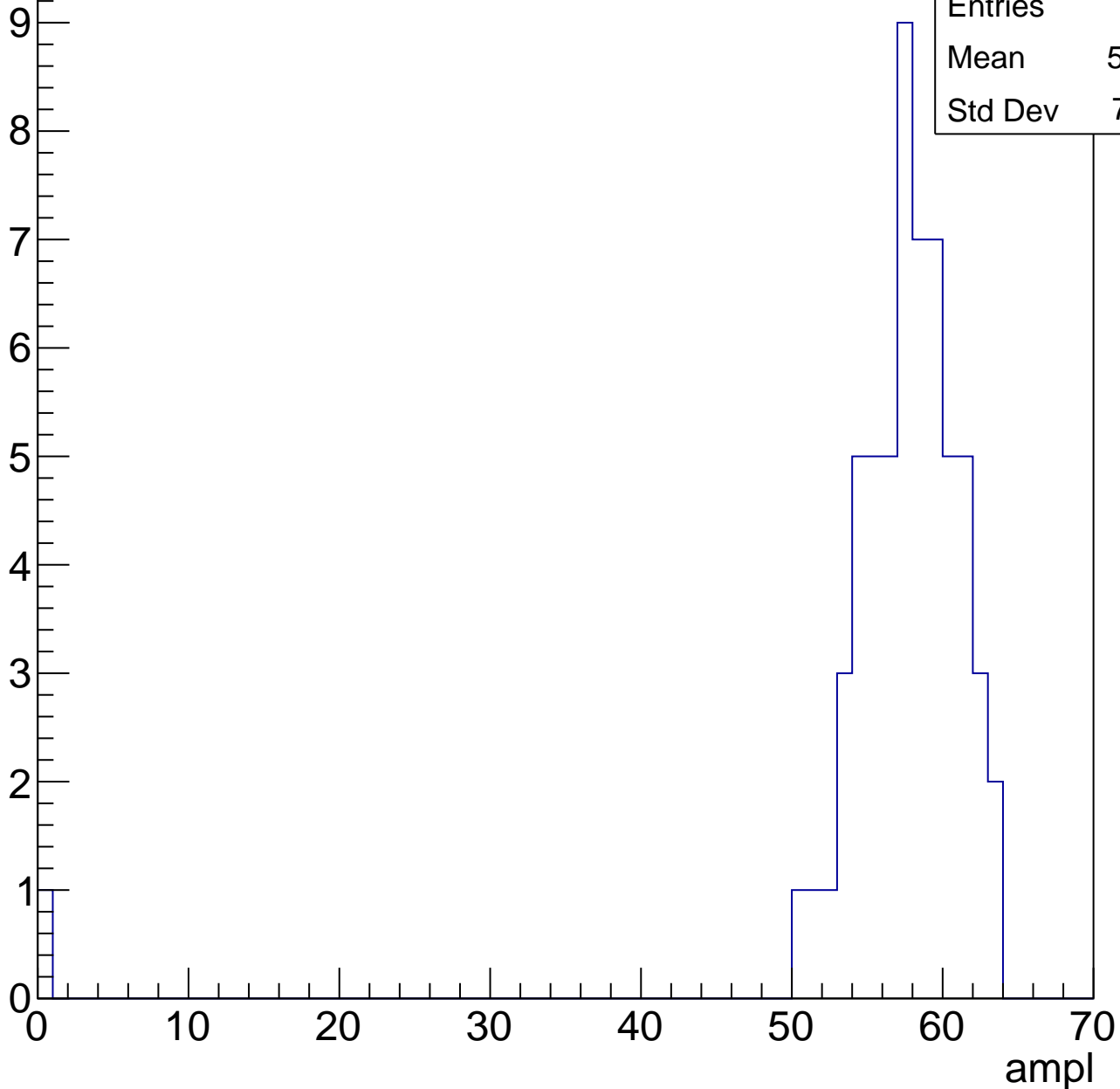


# B0L001S, U21-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	56.43
Std Dev	7.921

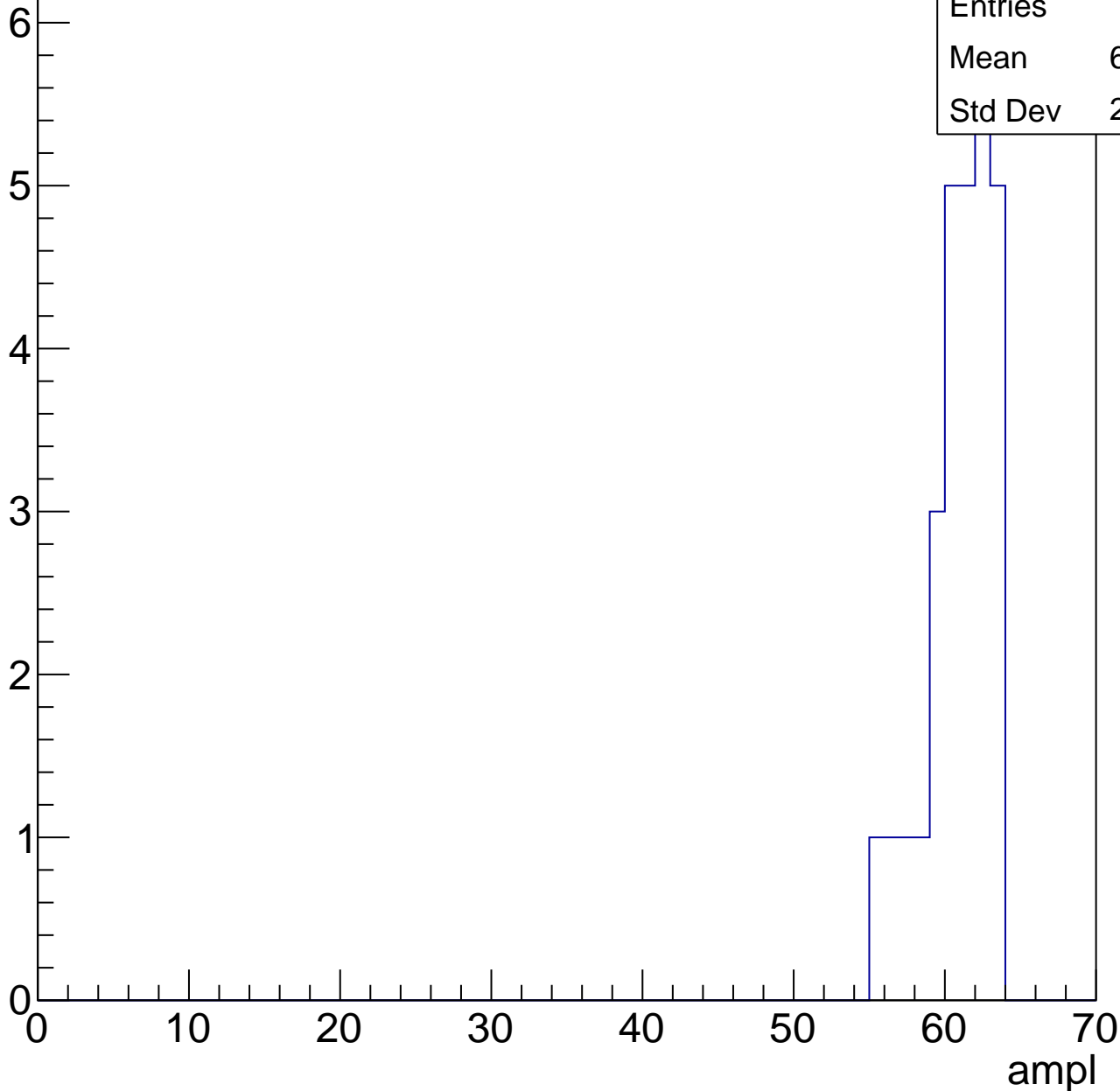


# B0L001S, U21-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	28
Mean	60.54
Std Dev	2.096



# B0L001S, U21-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B0L001S, U21-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch41, adc0

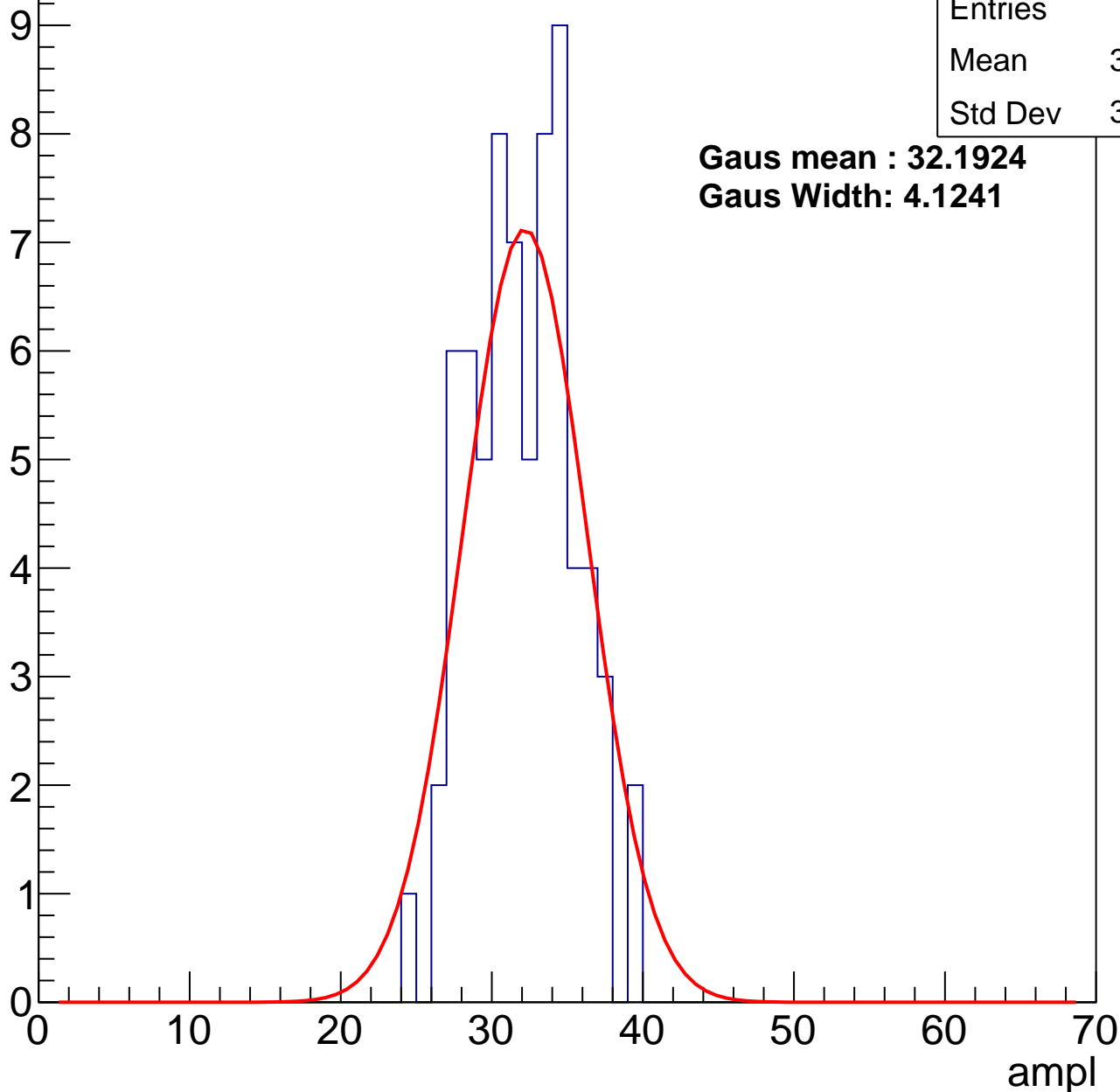
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	31.59
Std Dev	3.319

**Gaus mean : 32.1924**

**Gaus Width: 4.1241**

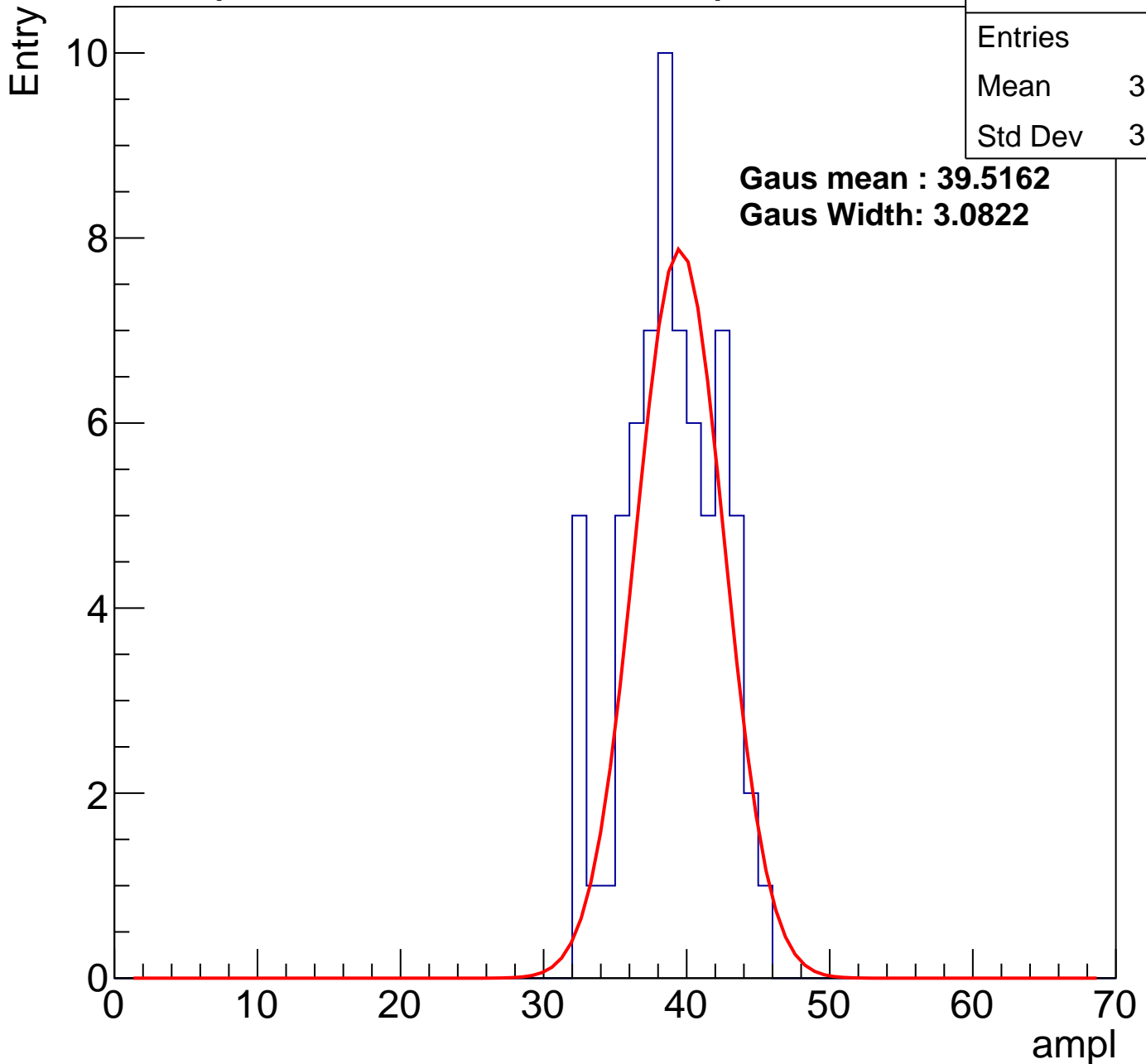


# B0L001S, U21-ch41, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	68
Mean	38.49
Std Dev	3.243

**Gaus mean : 39.5162**  
**Gaus Width: 3.0822**



# B0L001S, U21-ch41, adc2

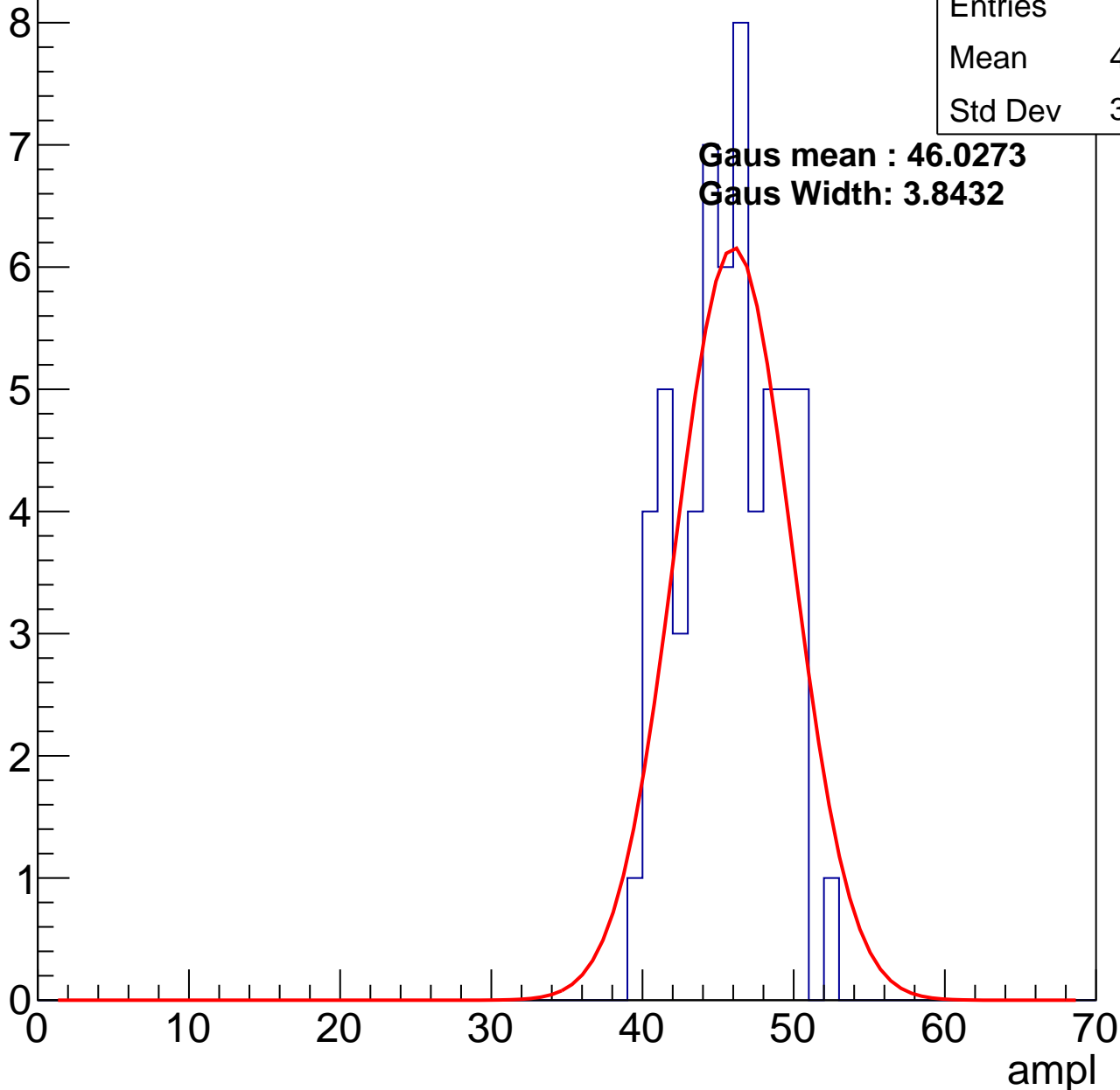
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	45.22
Std Dev	3.179

**Gaus mean : 46.0273**

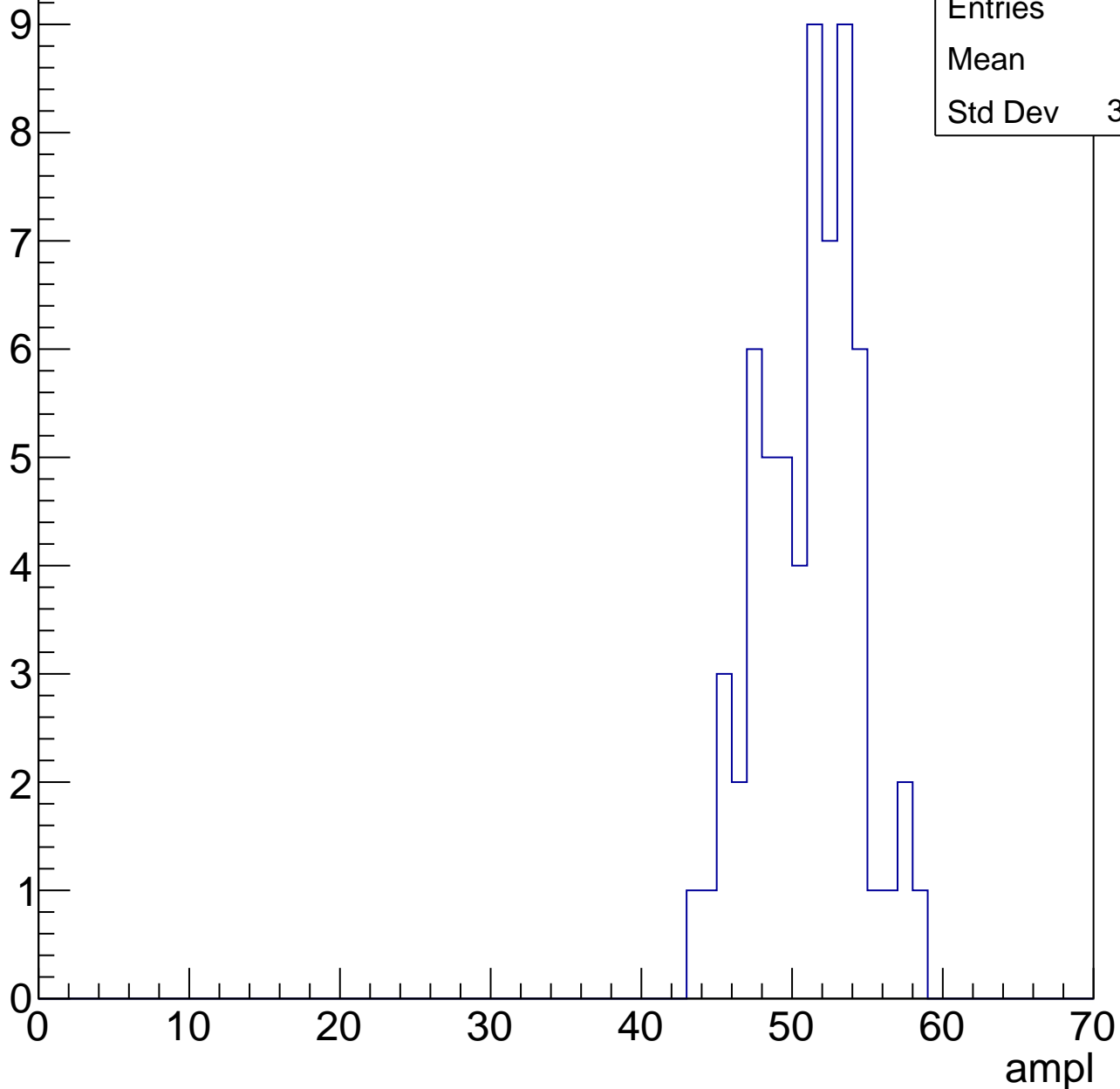
**Gaus Width: 3.8432**



# B0L001S, U21-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

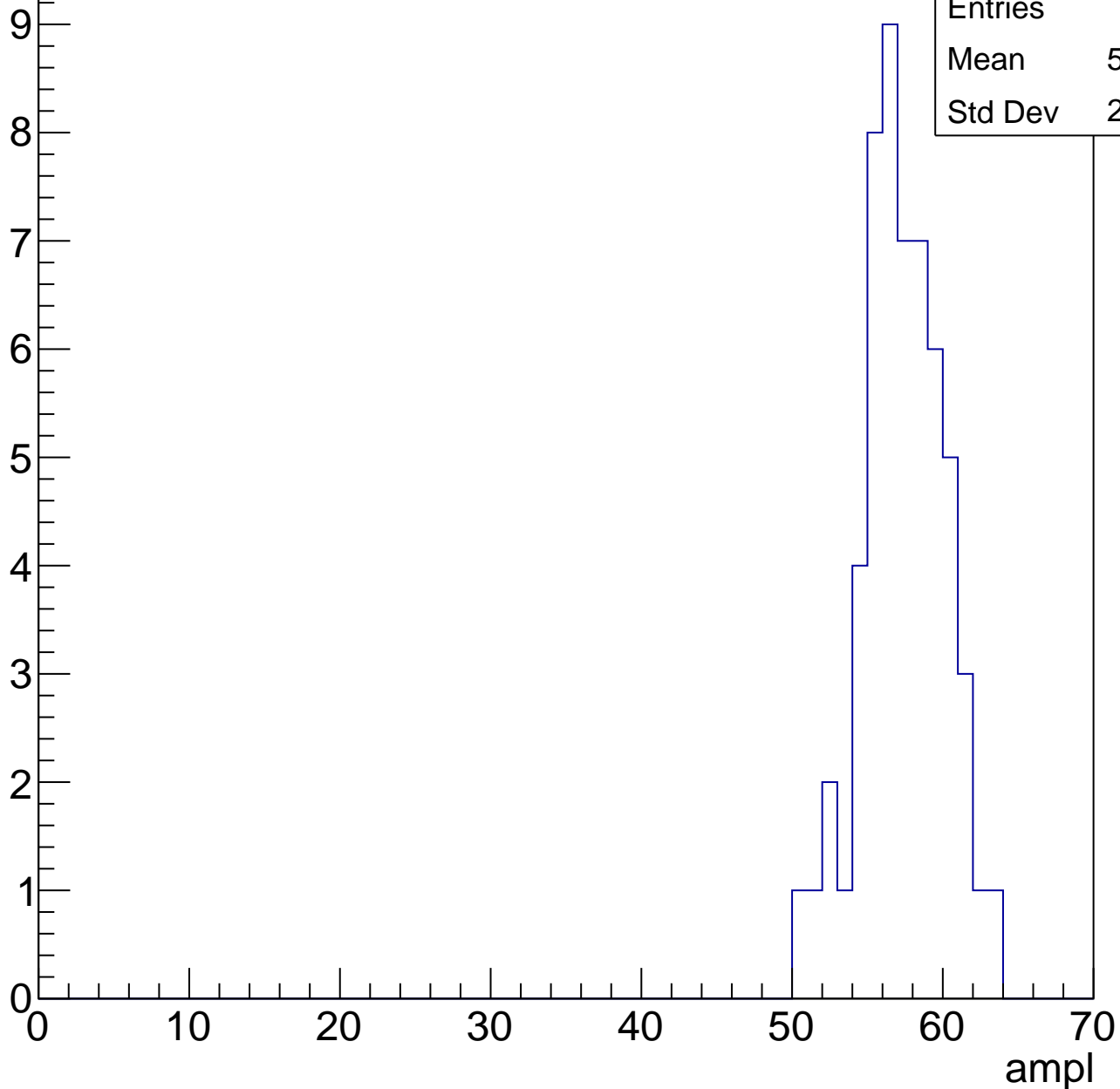
Entry



# B0L001S, U21-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



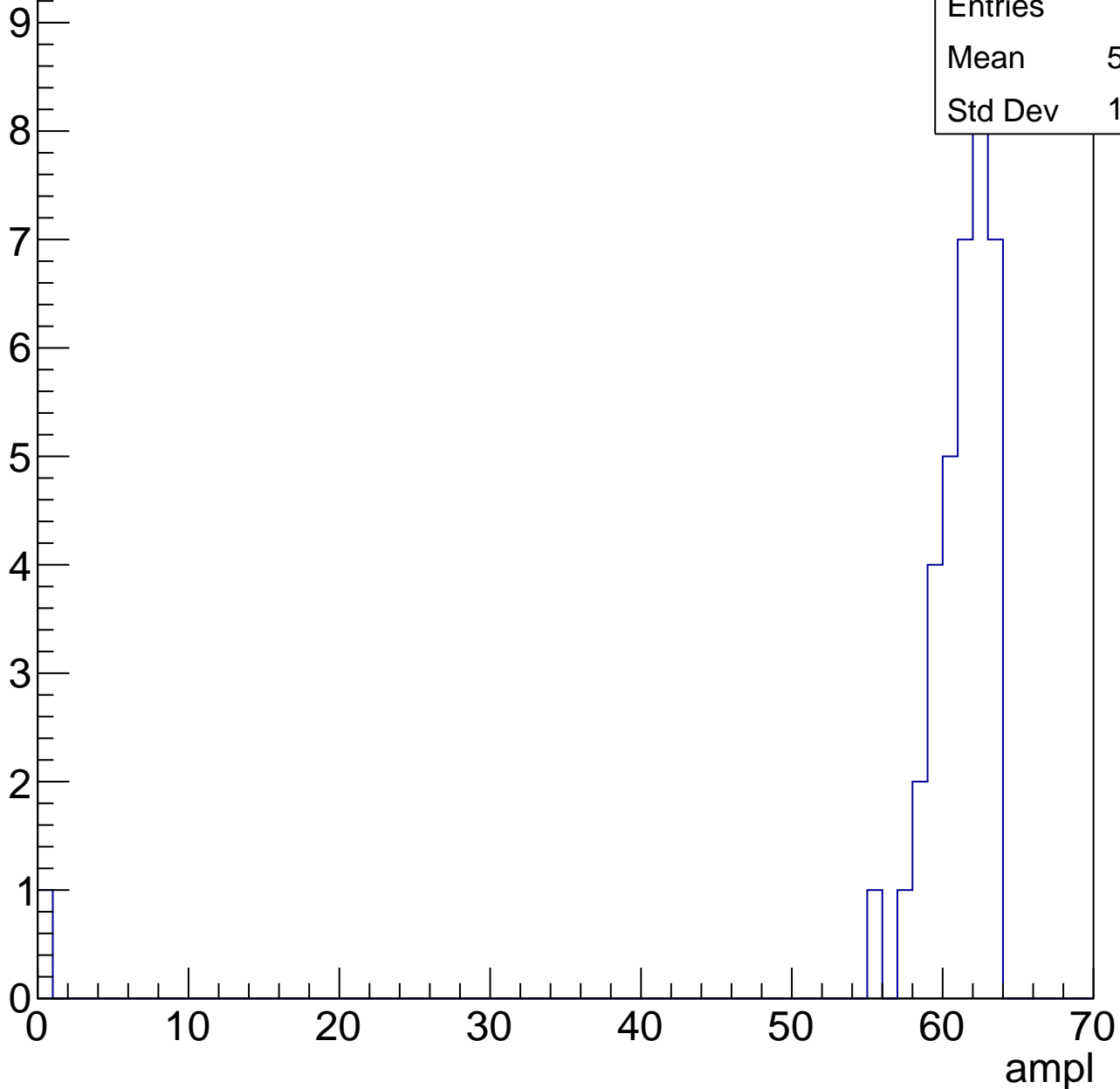
Entries	56
Mean	56.88
Std Dev	2.713

# B0L001S, U21-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	37
Mean	59.19
Std Dev	10.04



# B0L001S, U21-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U21-ch42, adc0

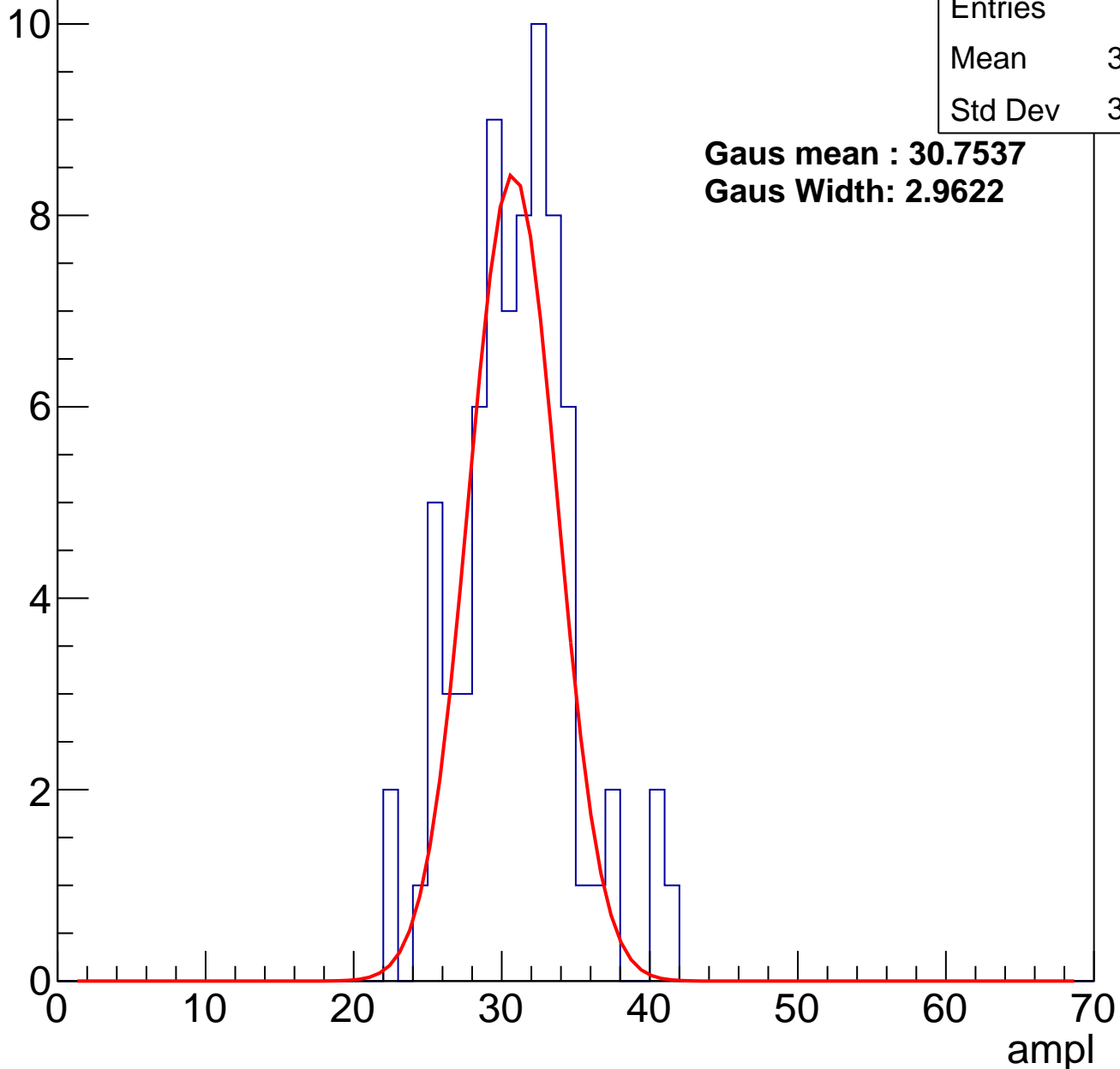
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	75
Mean	30.57
Std Dev	3.774

**Gaus mean : 30.7537**

**Gaus Width: 2.9622**

Entry



# B0L001S, U21-ch42, adc1

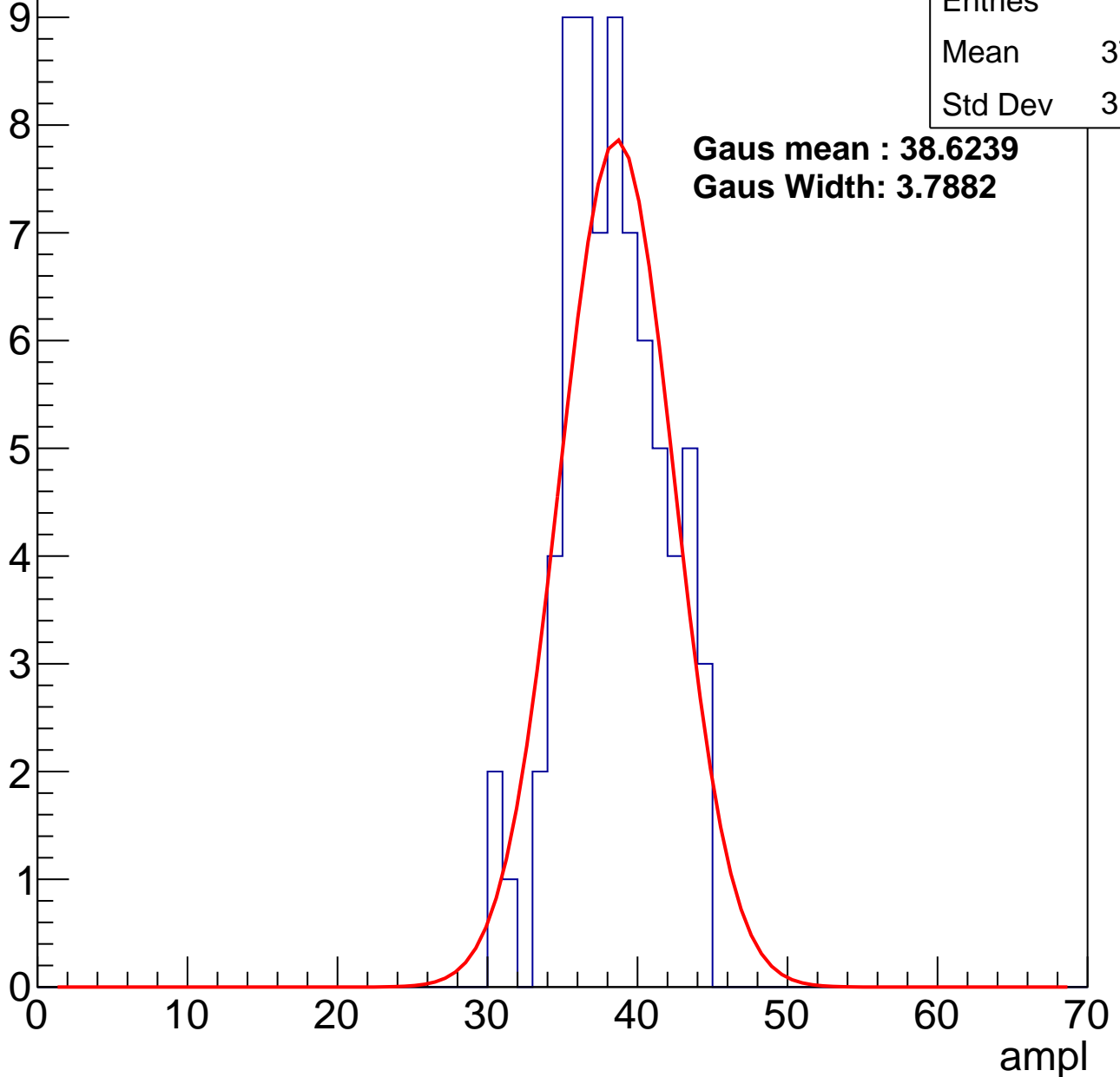
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	37.89
Std Dev	3.284

**Gaus mean : 38.6239**

**Gaus Width: 3.7882**



# B0L001S, U21-ch42, adc2

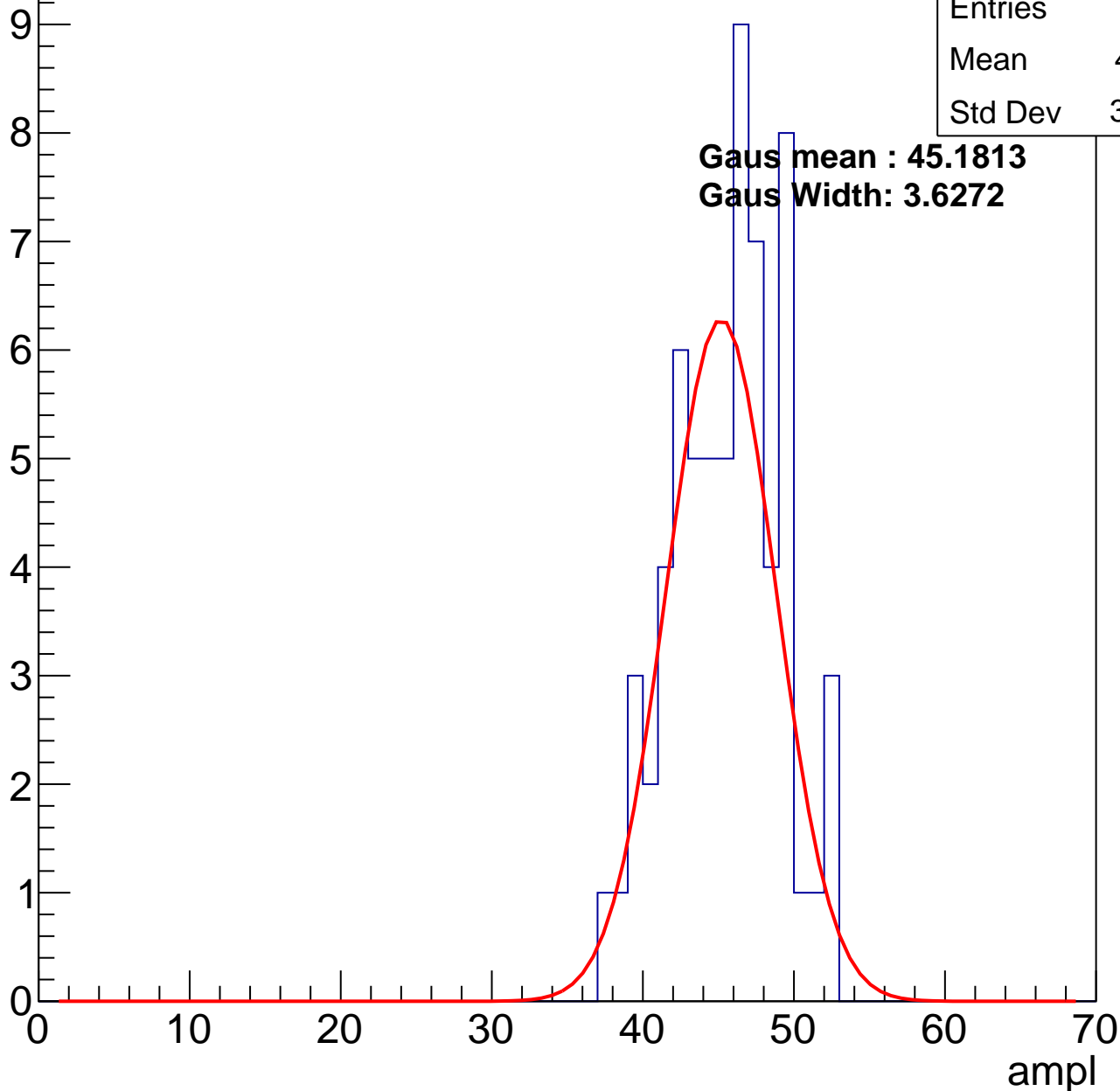
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	45.11
Std Dev	3.557

**Gaus mean : 45.1813**

**Gaus Width: 3.6272**

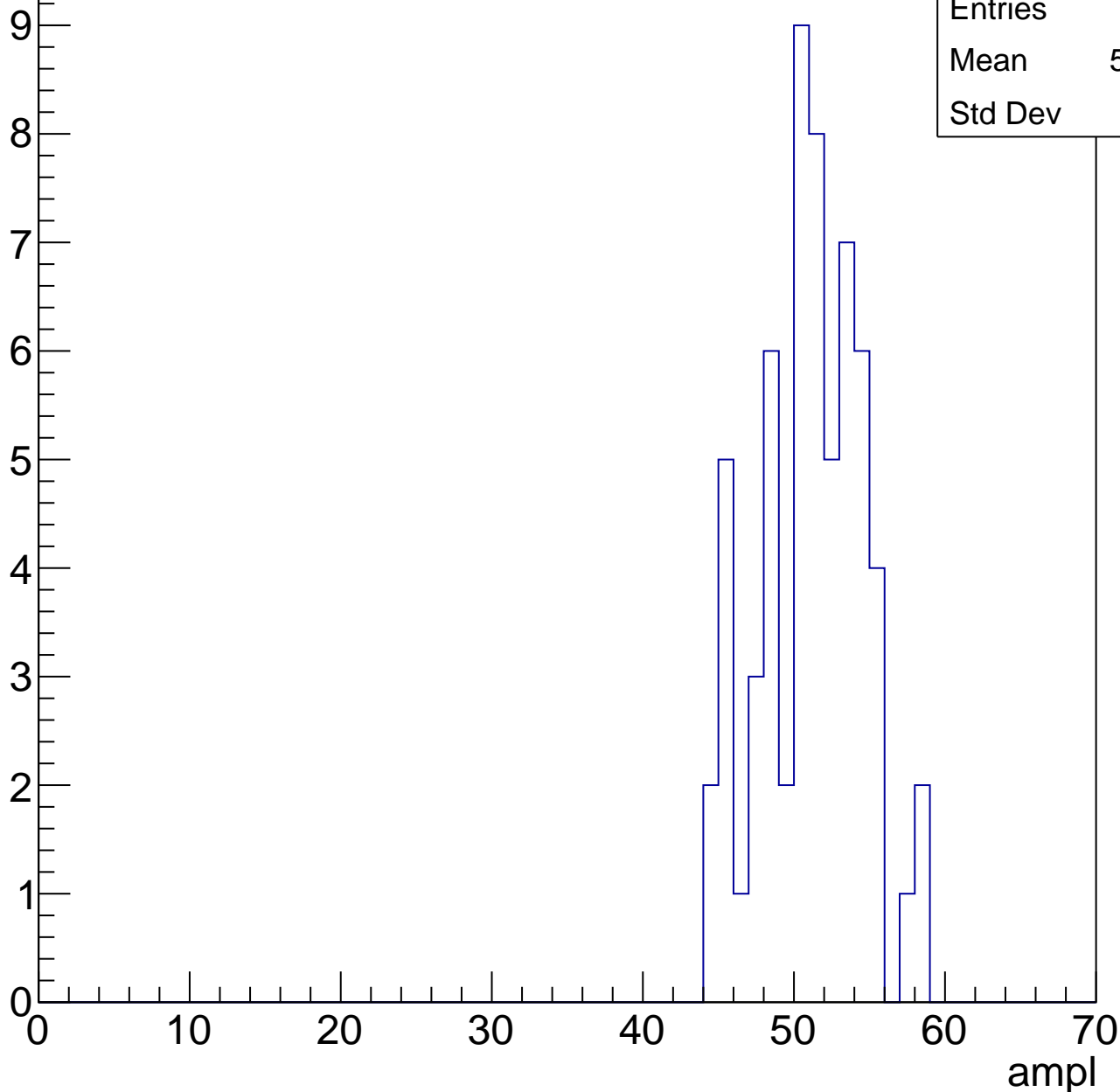


# B0L001S, U21-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	50.69
Std Dev	3.39



# B0L001S, U21-ch42, adc4

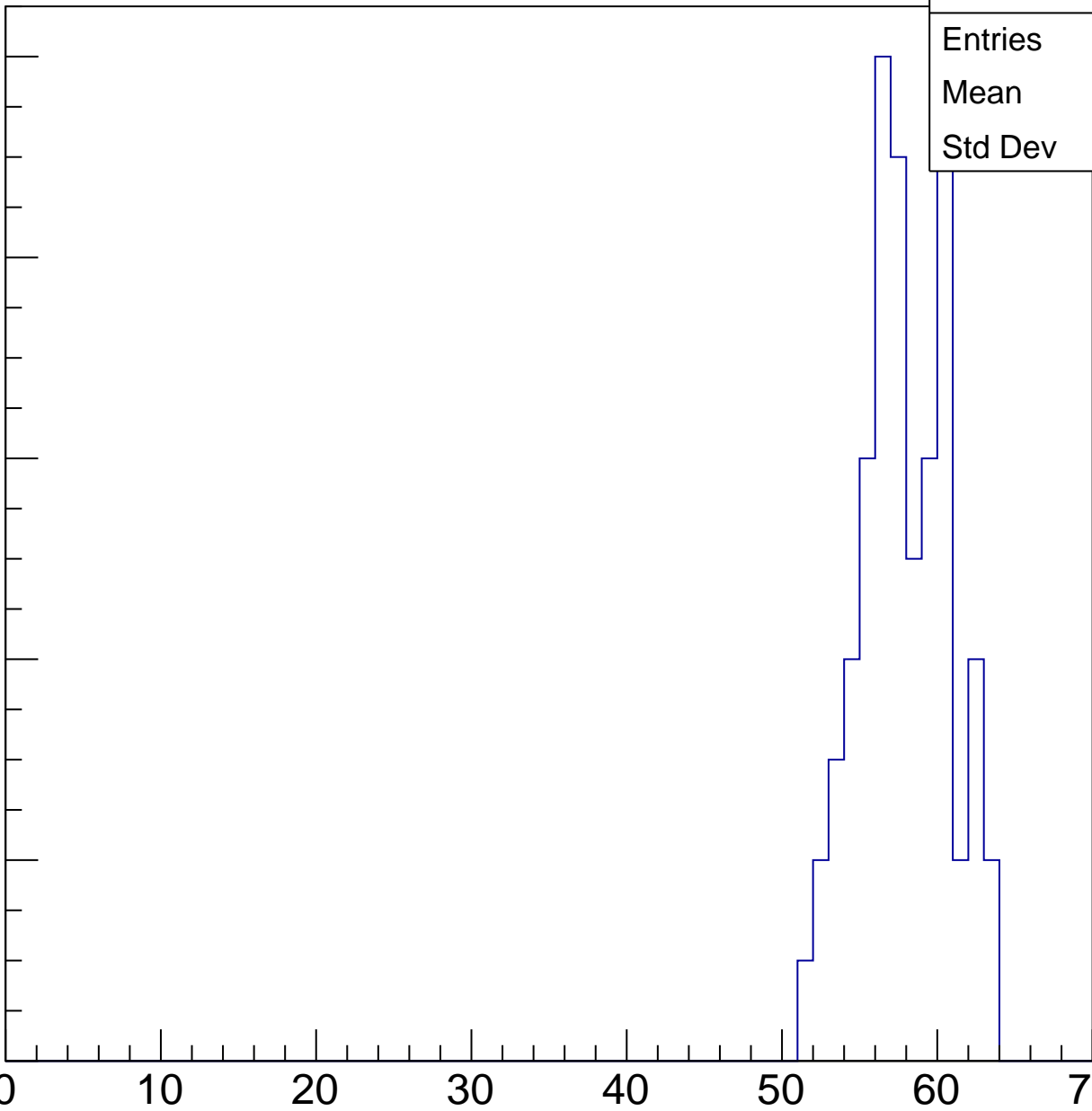
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

10  
8  
6  
4  
2  
0

Entries	63
Mean	57.35
Std Dev	2.846

ampl

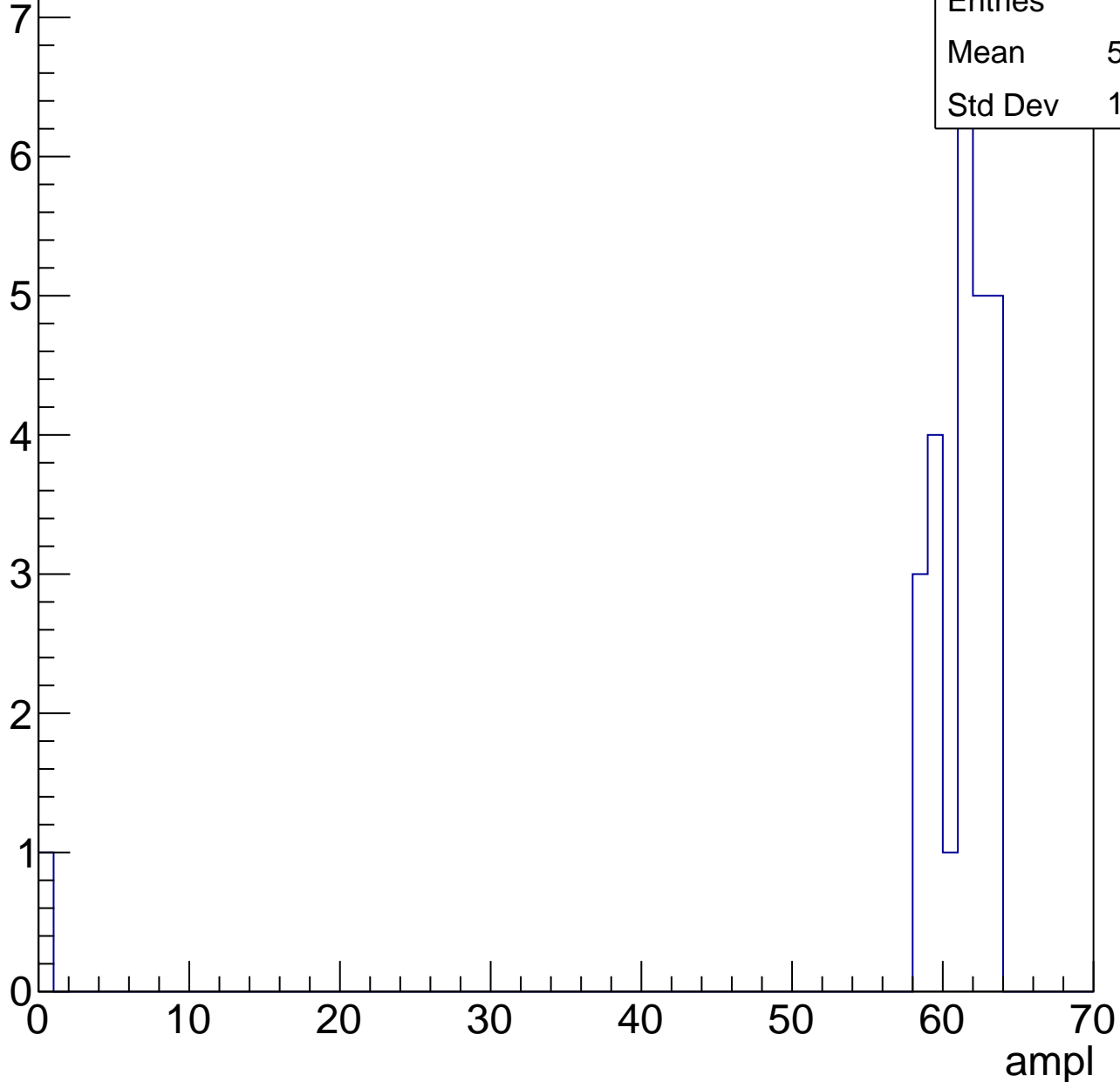


# B0L001S, U21-ch42, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	26
Mean	58.54
Std Dev	11.82



# B0L001S, U21-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U21-ch43, adc0

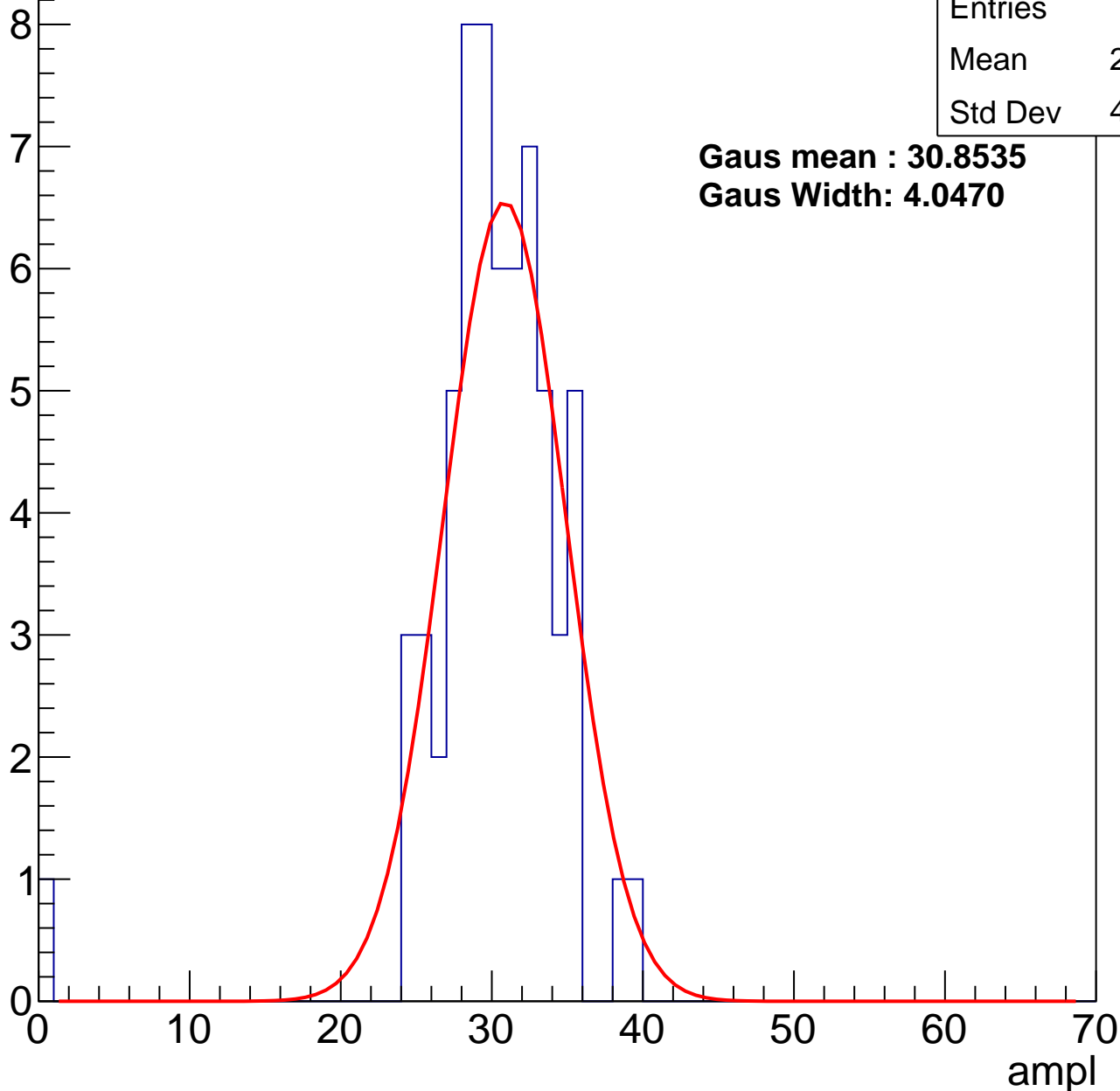
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	29.67
Std Dev	4.985

**Gaus mean : 30.8535**

**Gaus Width: 4.0470**



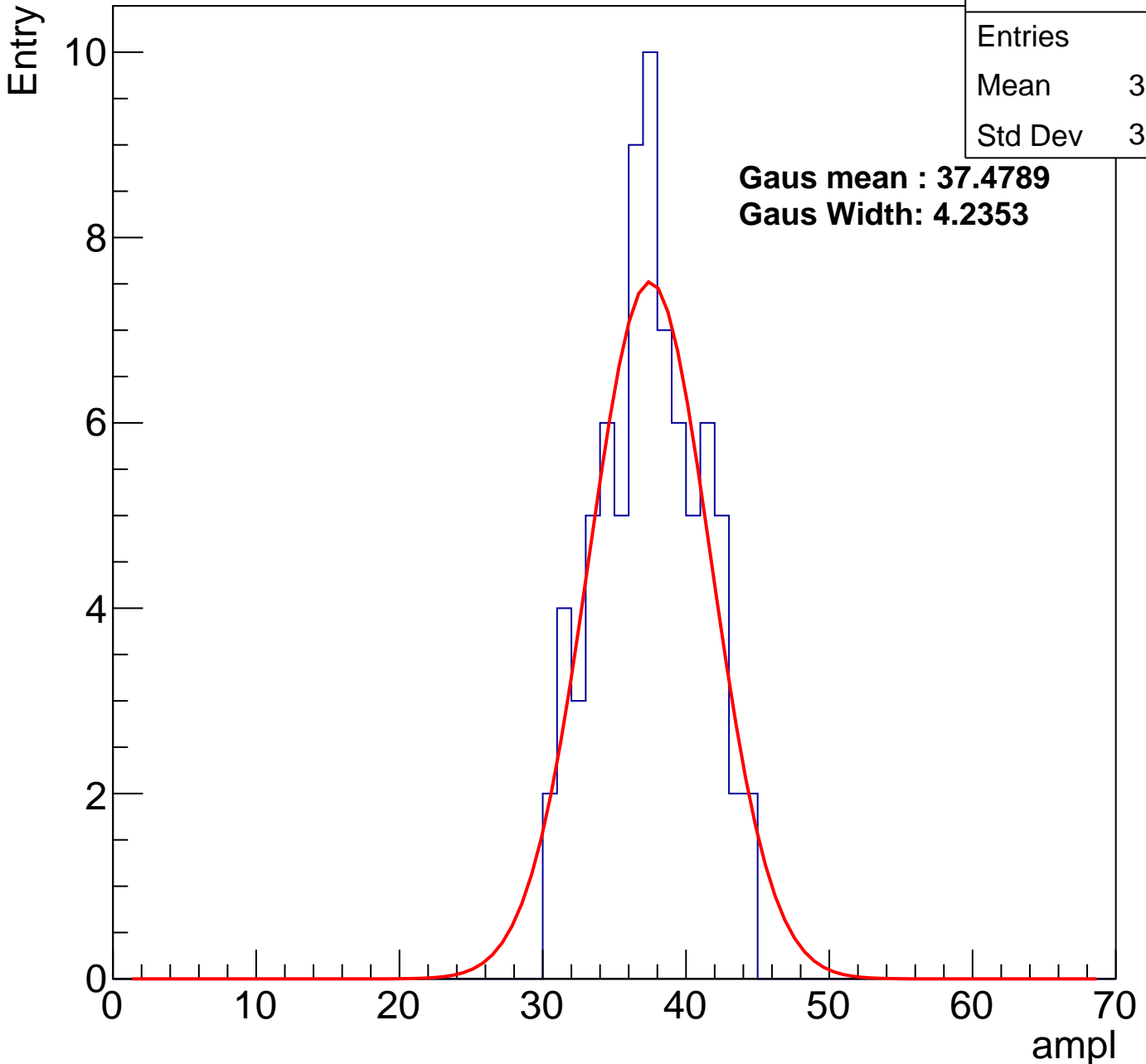
# B0L001S, U21-ch43, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	77
Mean	36.99
Std Dev	3.507

**Gaus mean : 37.4789**

**Gaus Width: 4.2353**



# B0L001S, U21-ch43, adc2

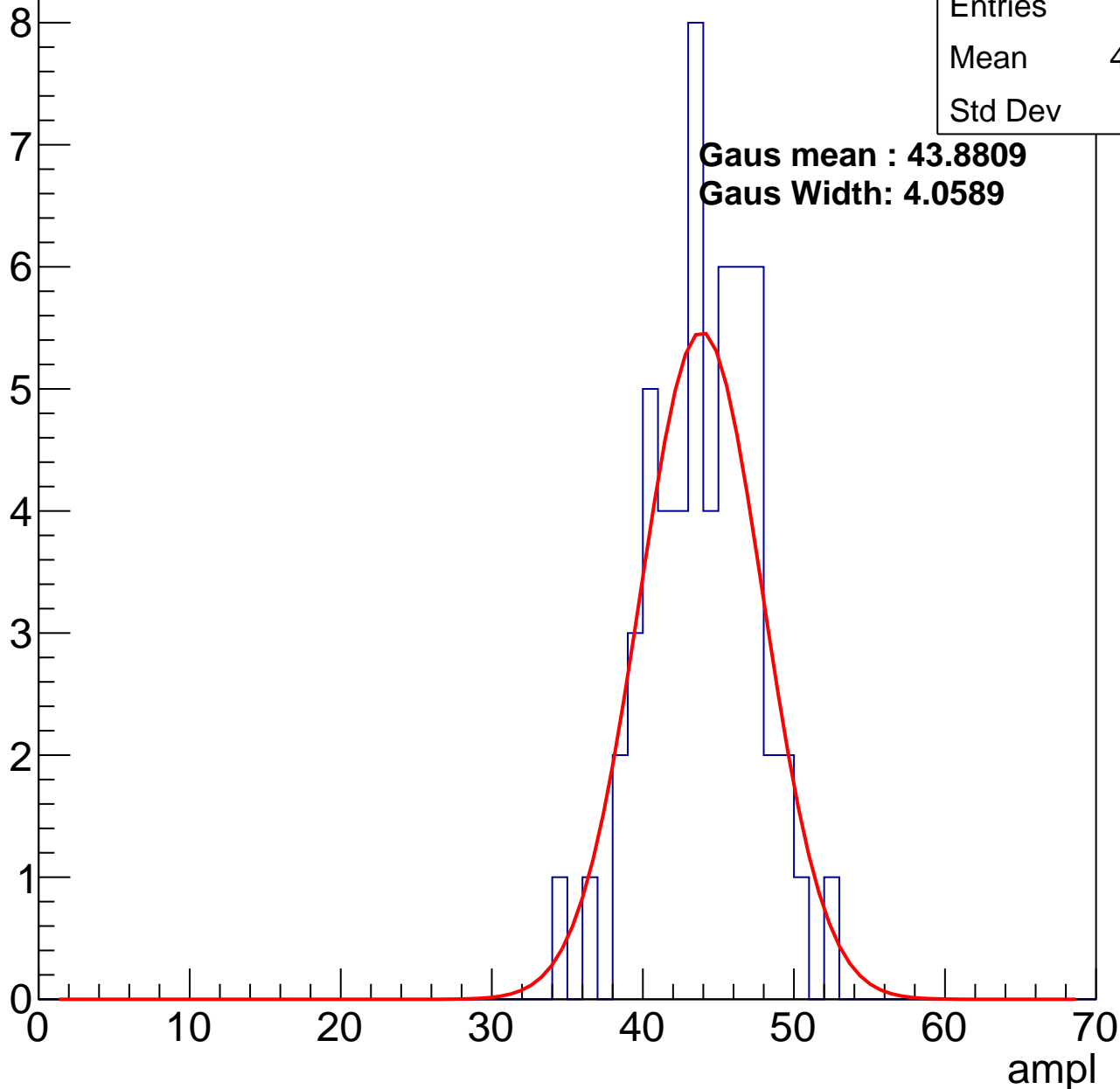
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	43.55
Std Dev	3.55

**Gaus mean : 43.8809**

**Gaus Width: 4.0589**

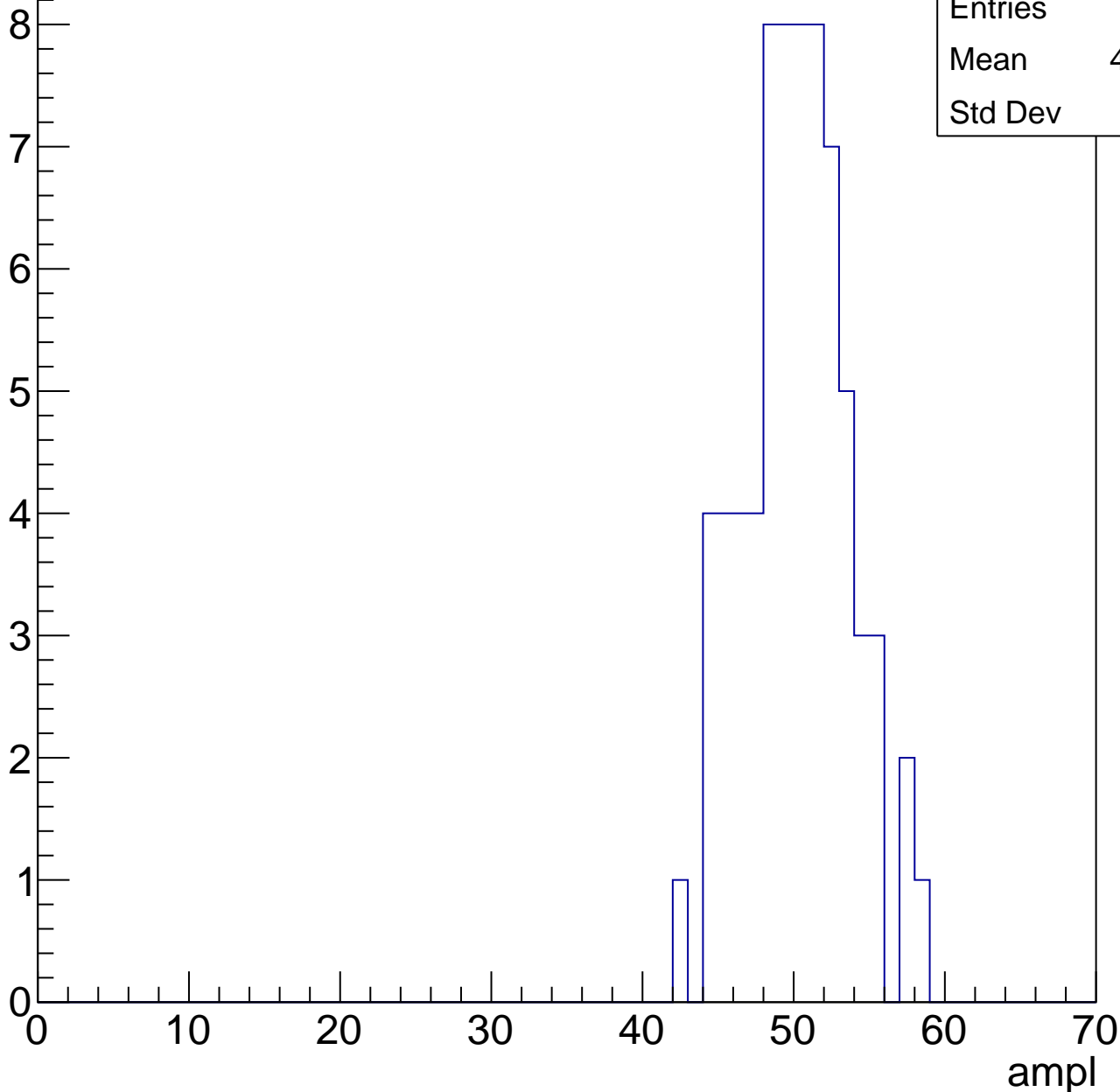


# B0L001S, U21-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	49.74
Std Dev	3.4

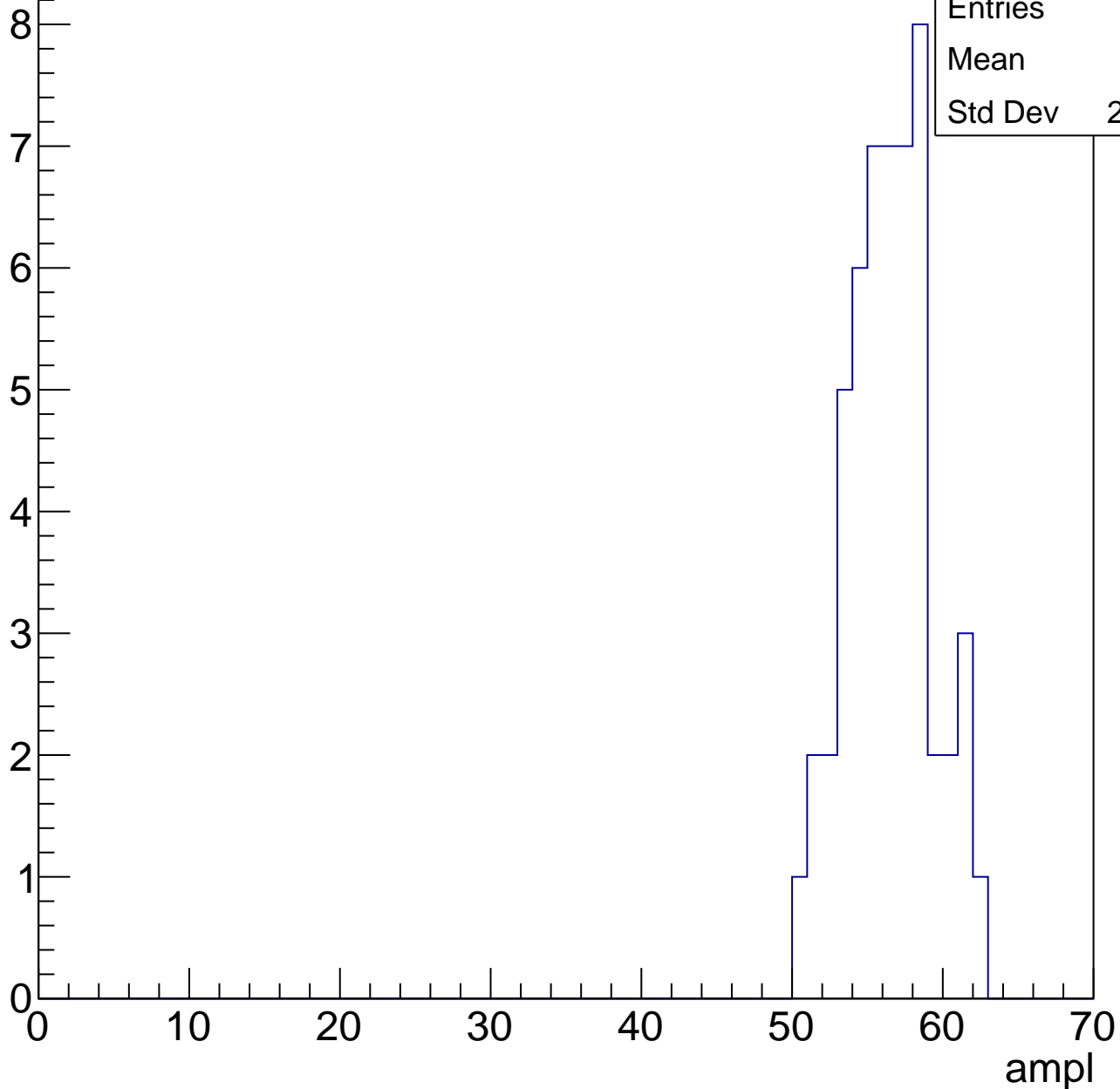


# B0L001S, U21-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	56
Std Dev	2.727

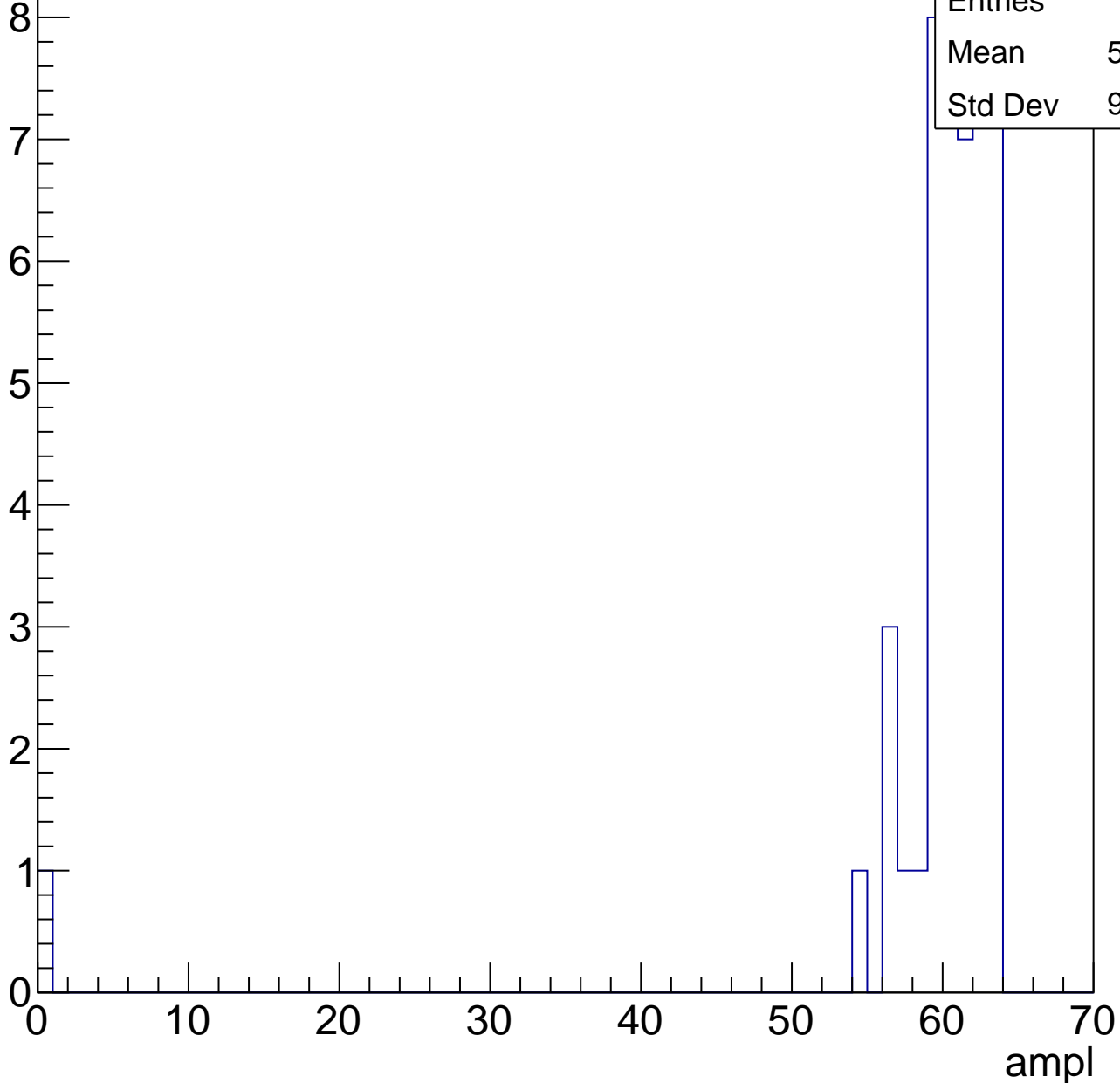


# B0L001S, U21-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	59.04
Std Dev	9.058



# B0L001S, U21-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B0L001S, U21-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch44, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	61
Mean	28.69
Std Dev	6.216

**Gaus mean : 29.4917**

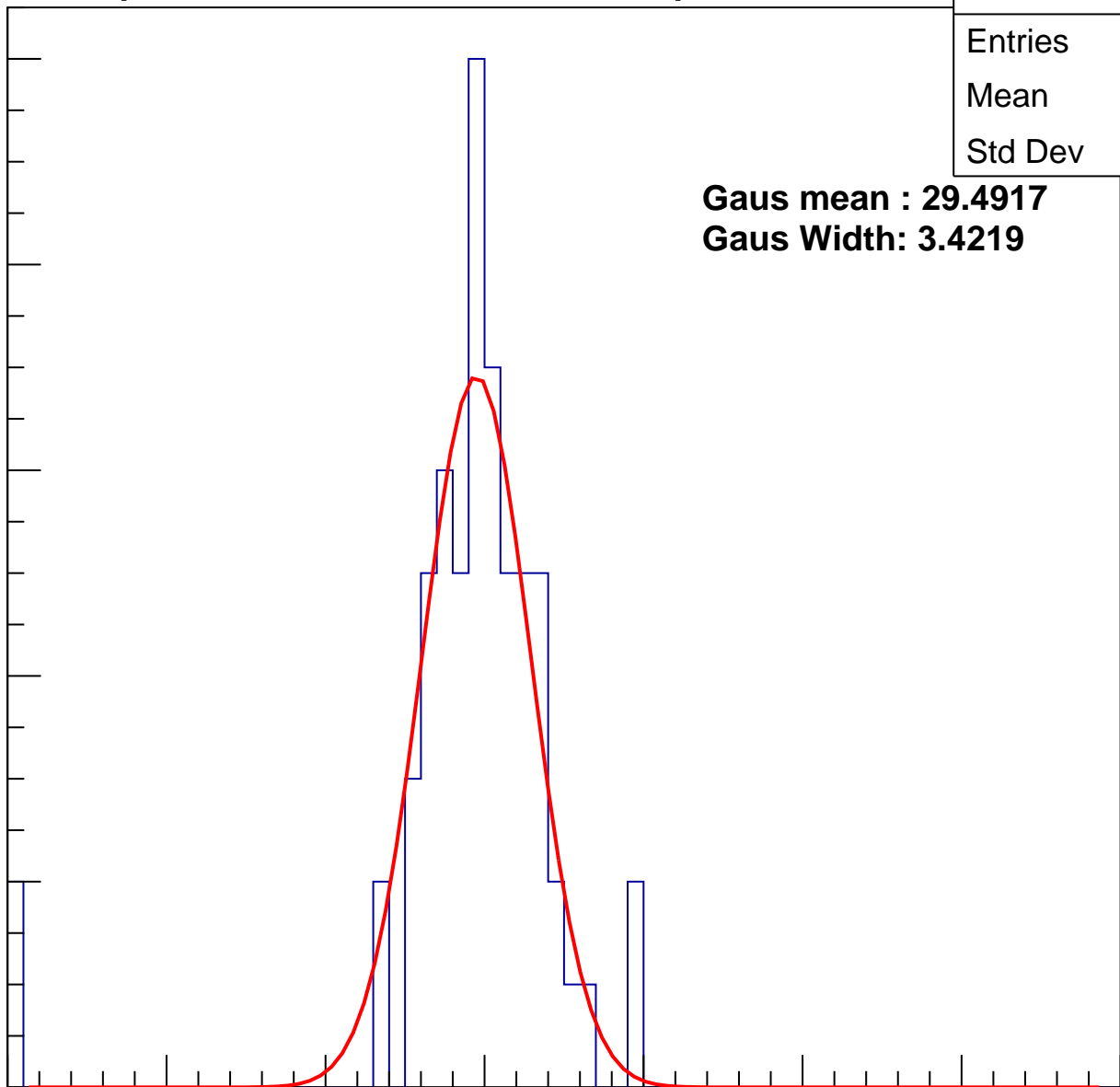
**Gaus Width: 3.4219**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



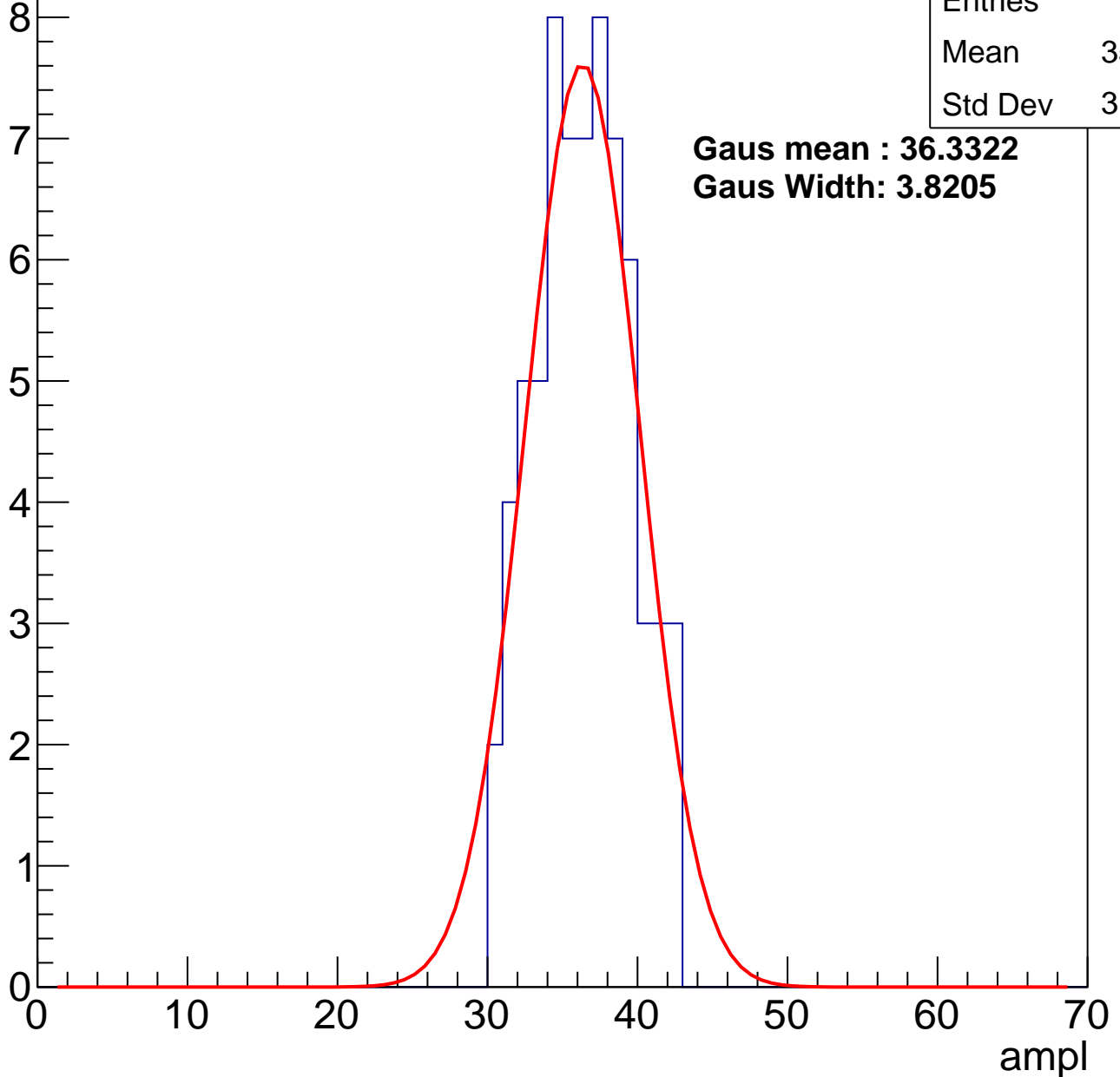
# B0L001S, U21-ch44, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	35.93
Std Dev	3.107

**Gaus mean : 36.3322**  
**Gaus Width: 3.8205**



# B0L001S, U21-ch44, adc2

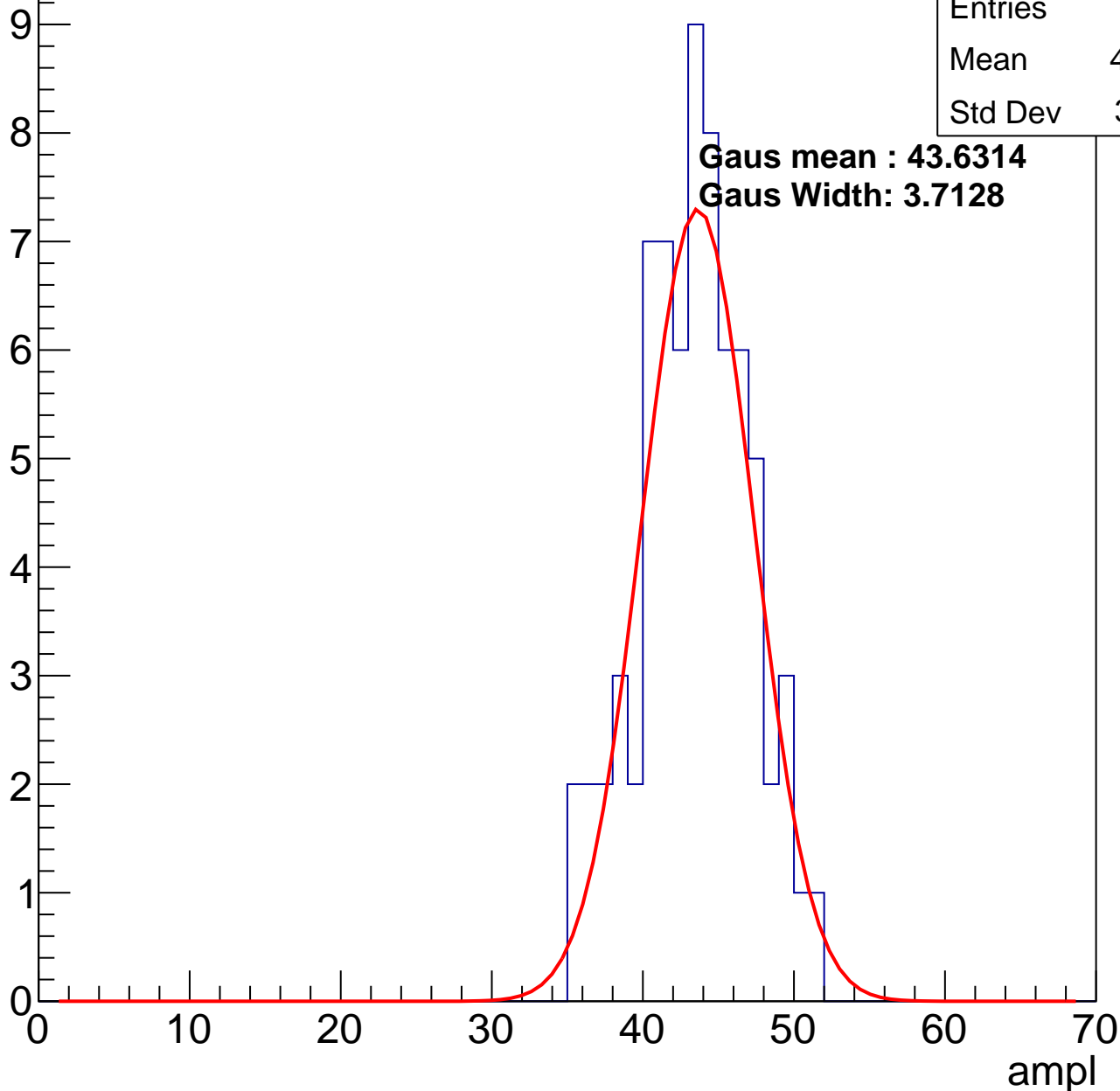
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	42.93
Std Dev	3.611

**Gaus mean : 43.6314**

**Gaus Width: 3.7128**

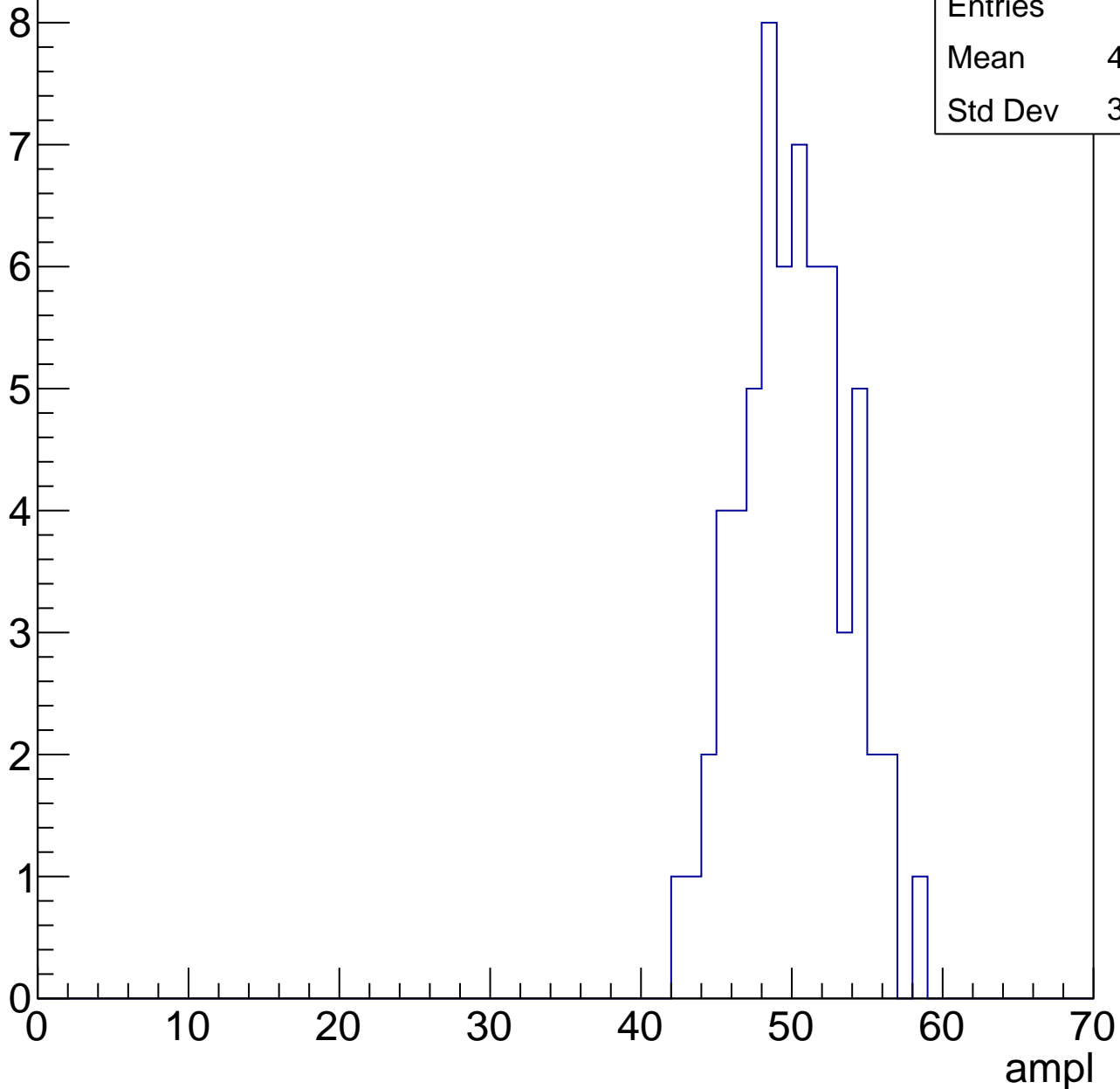


# B0L001S, U21-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	49.63
Std Dev	3.443

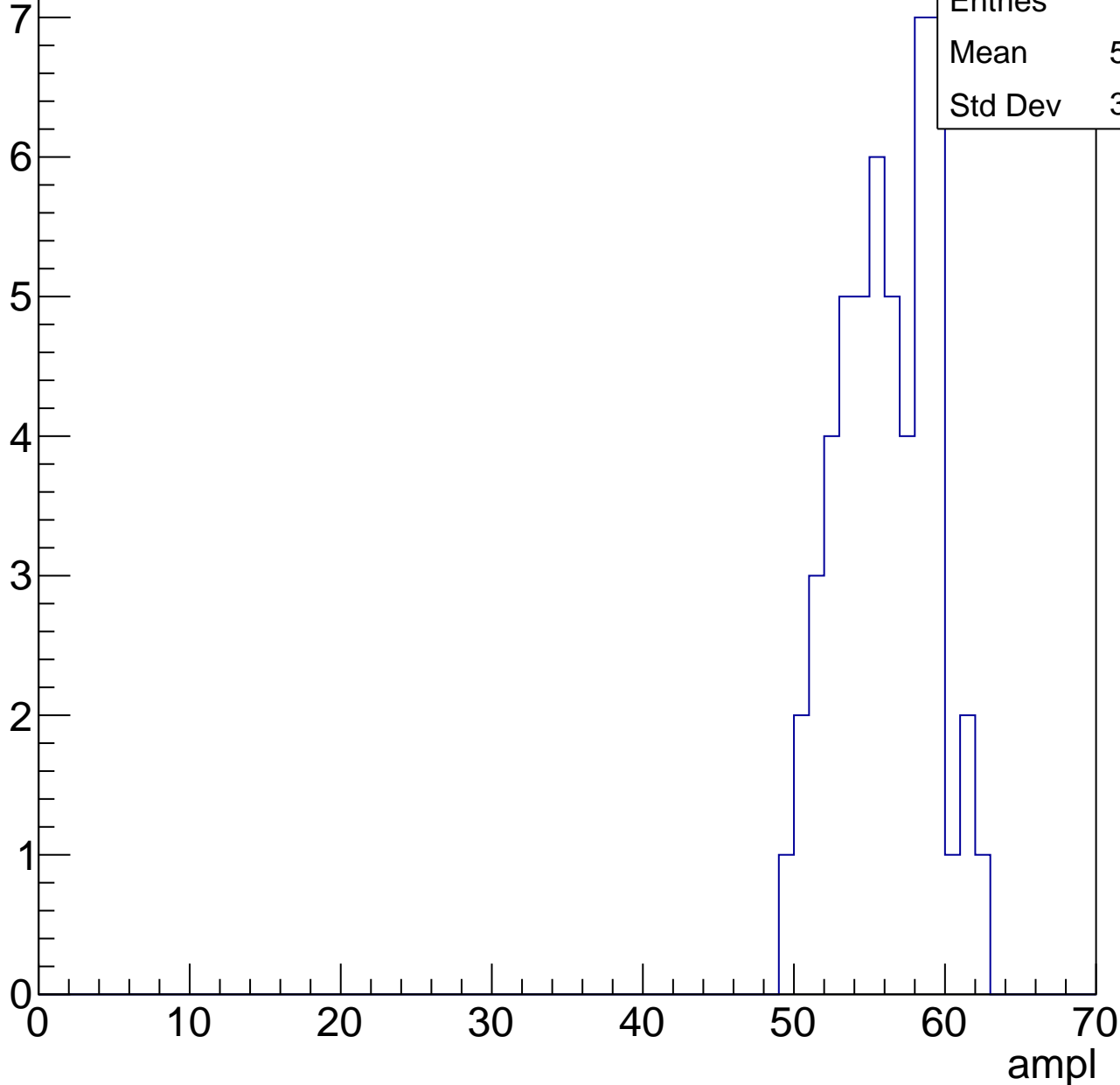


# B0L001S, U21-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	55.58
Std Dev	3.129

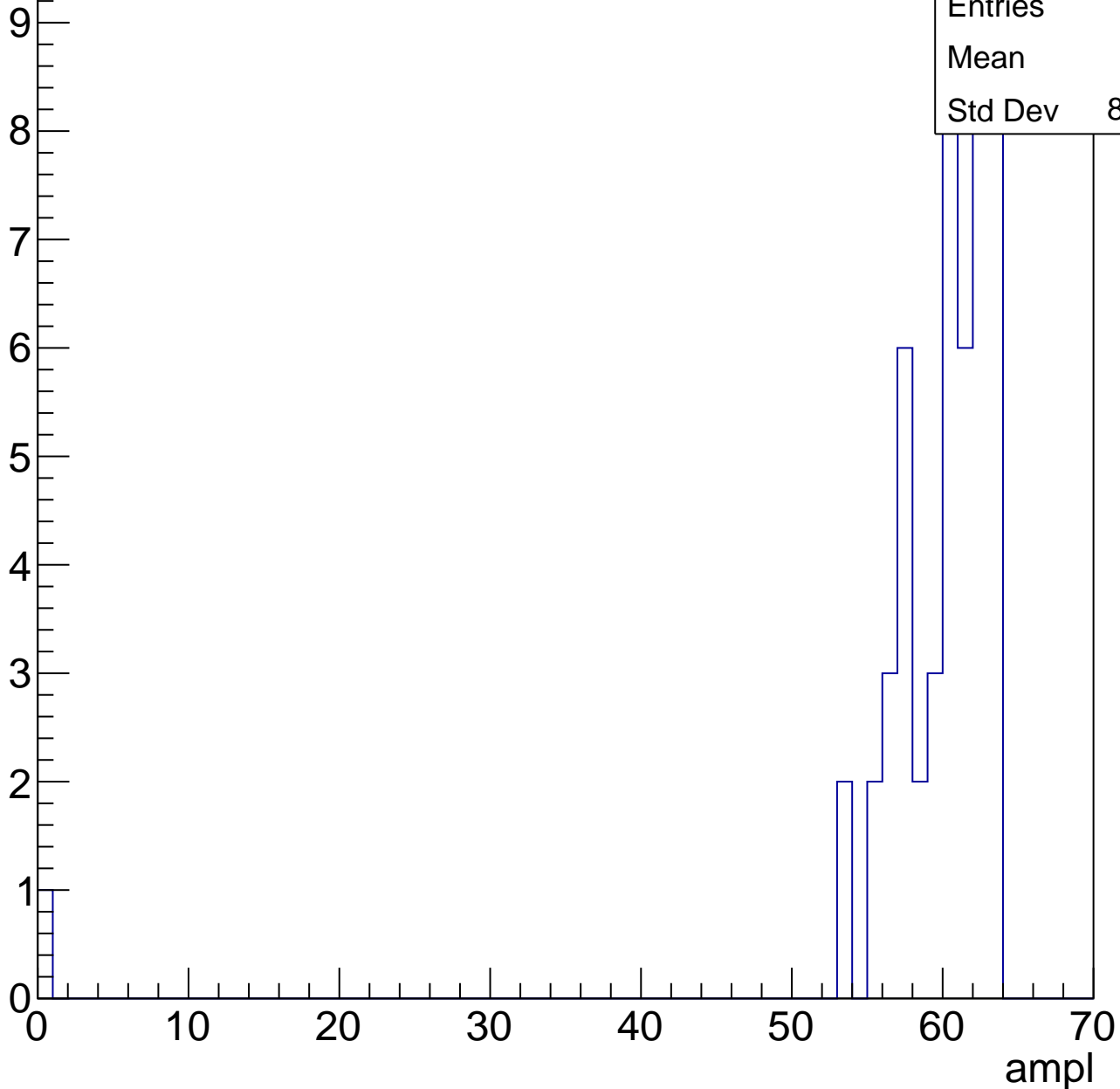


# B0L001S, U21-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

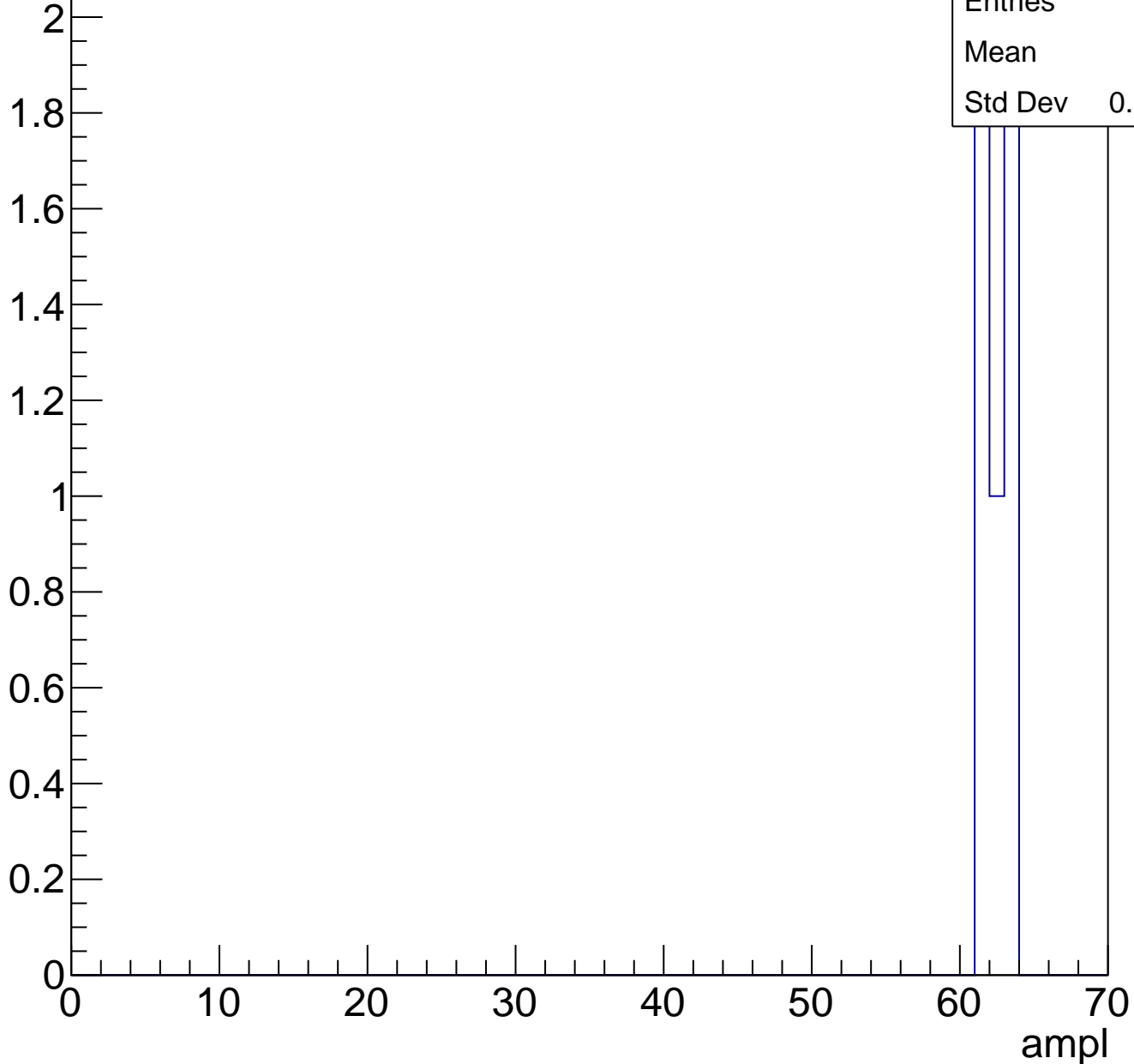
Entries	50
Mean	58.5
Std Dev	8.785



# B0L001S, U21-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L001S, U21-ch45, adc0

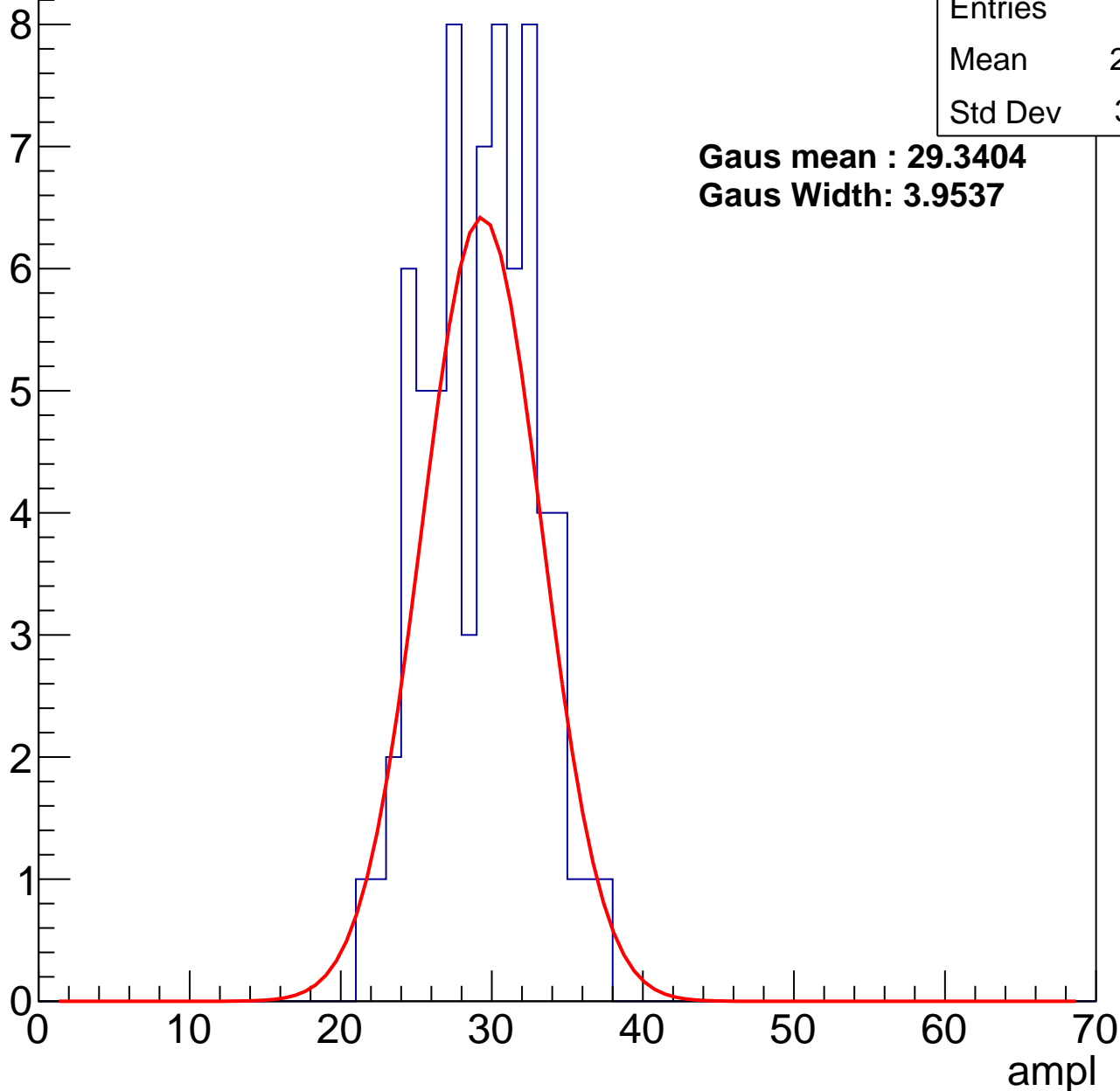
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	28.86
Std Dev	3.581

**Gaus mean : 29.3404**

**Gaus Width: 3.9537**



# B0L001S, U21-ch45, adc1

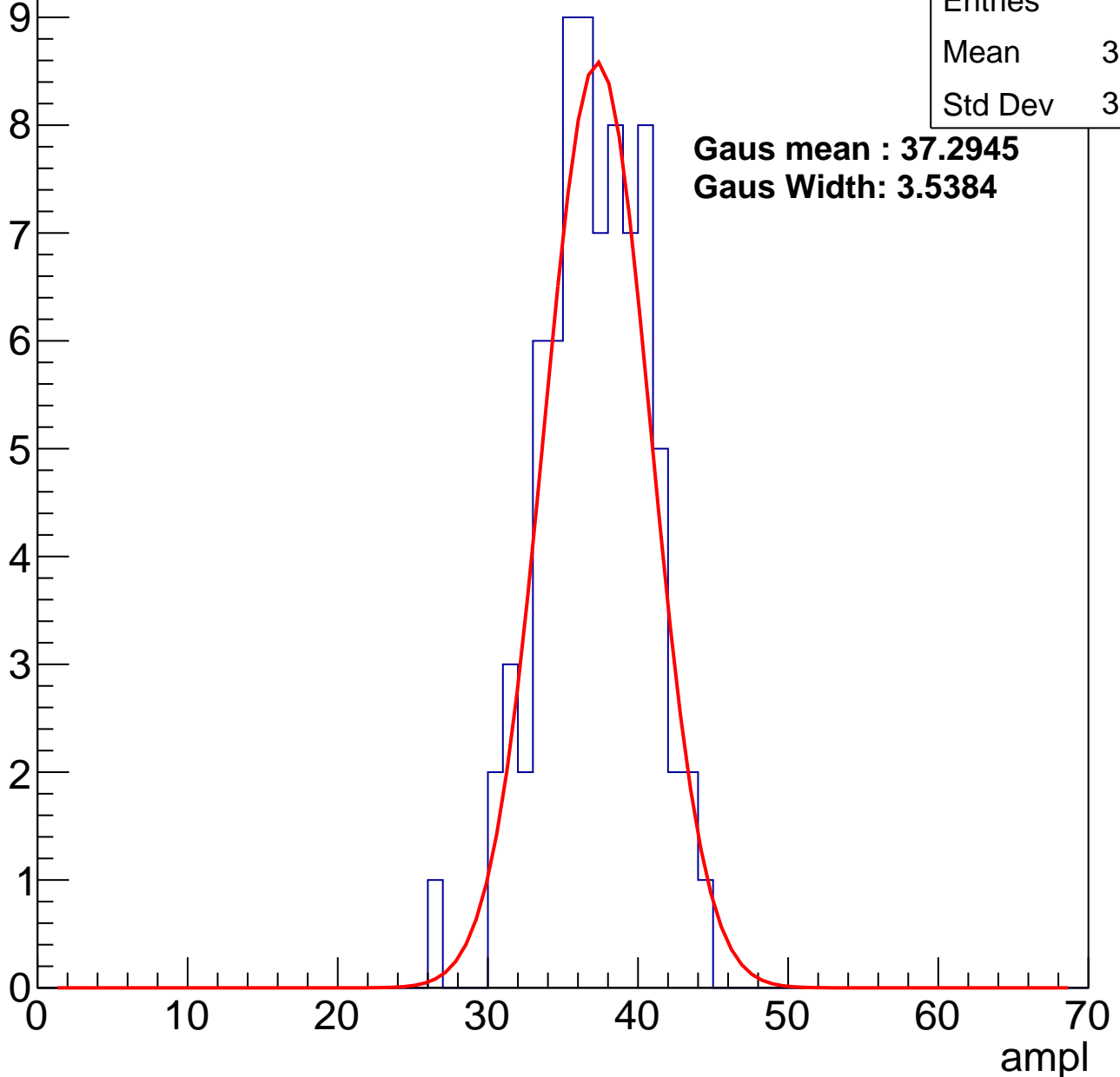
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	36.65
Std Dev	3.437

**Gaus mean : 37.2945**

**Gaus Width: 3.5384**



# B0L001S, U21-ch45, adc2

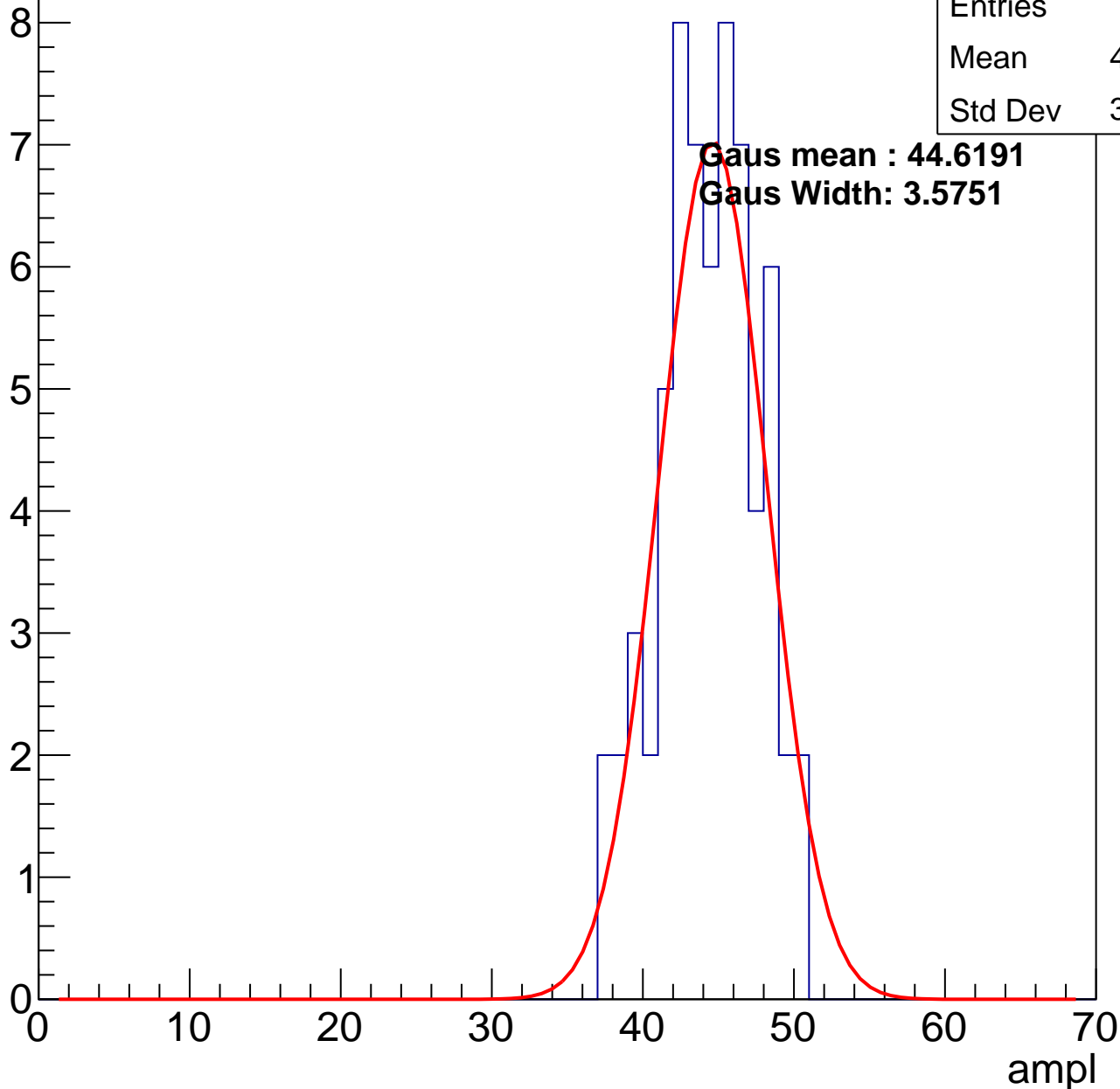
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	43.89
Std Dev	3.187

**Gaus mean : 44.6191**

**Gaus Width: 3.5751**

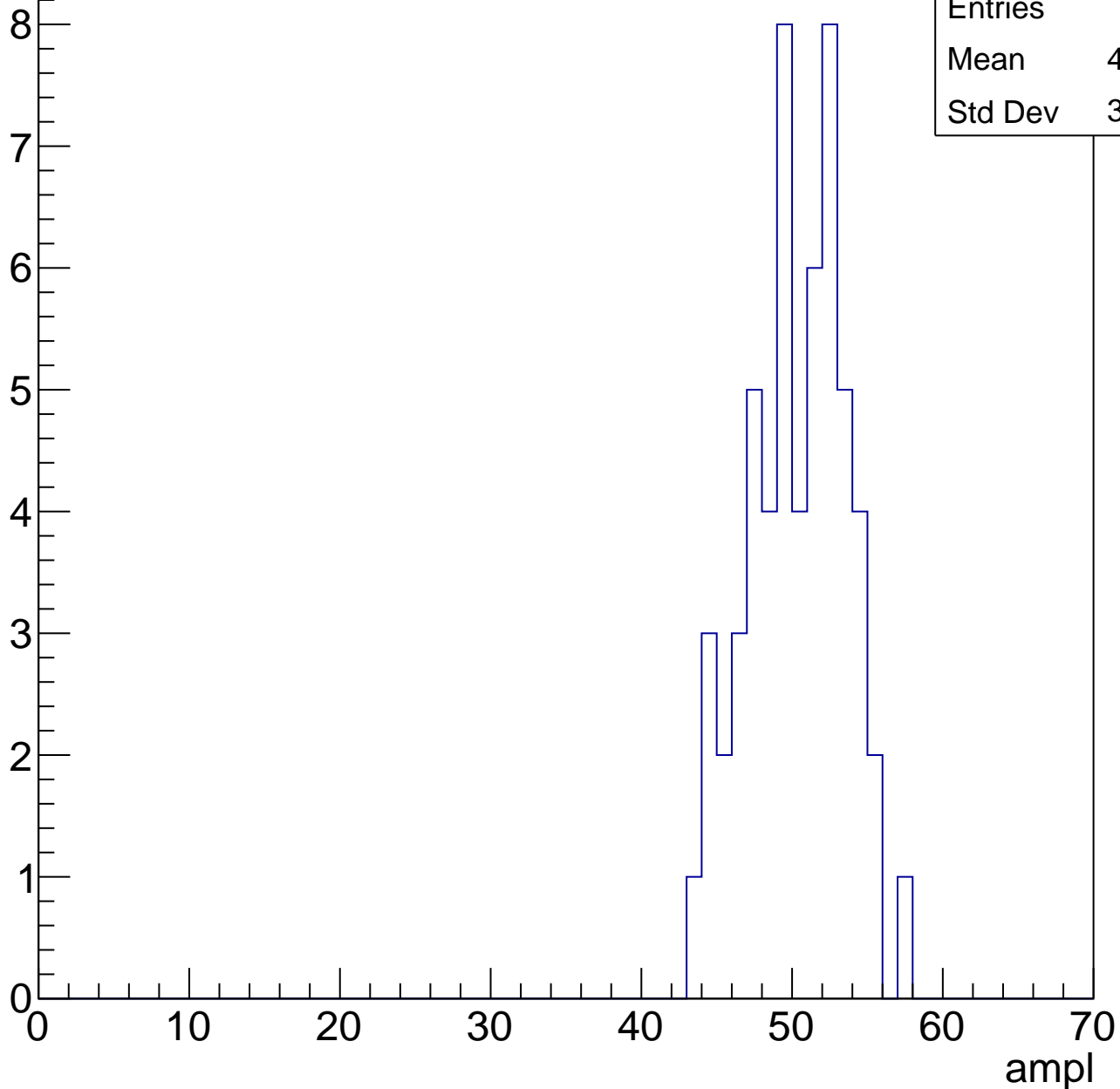


# B0L001S, U21-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	49.86
Std Dev	3.187

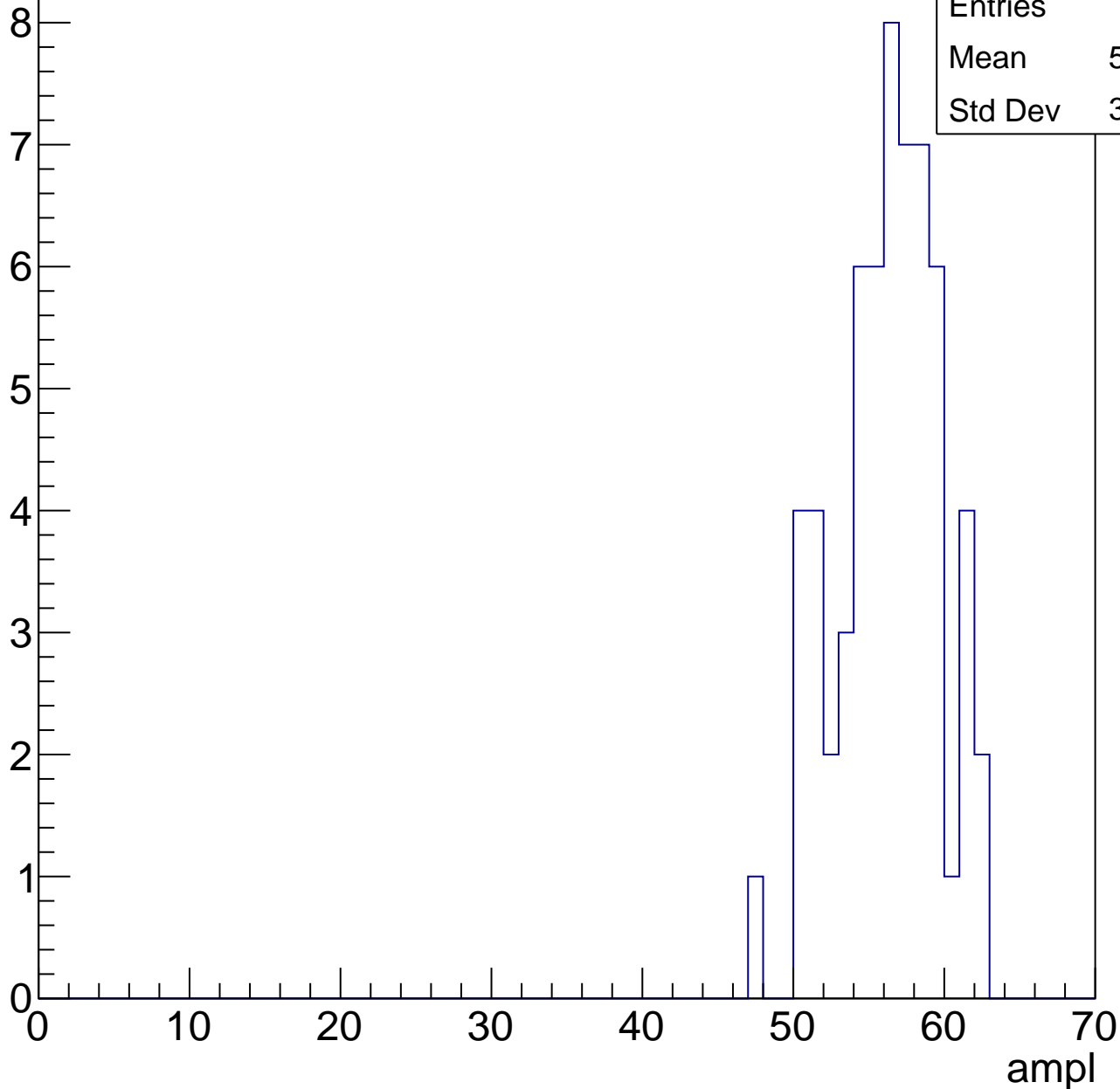


# B0L001S, U21-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	55.79
Std Dev	3.359

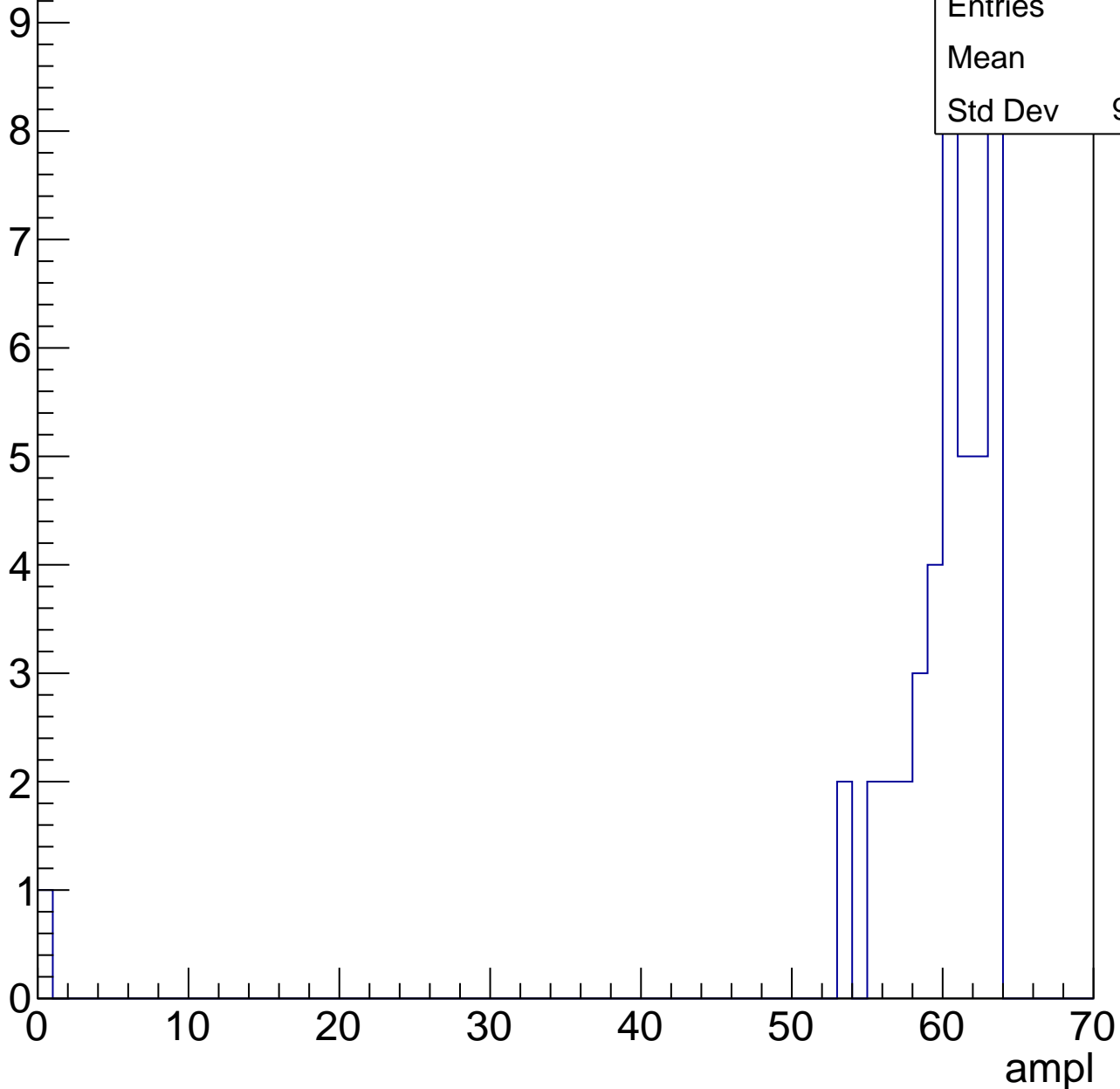


# B0L001S, U21-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

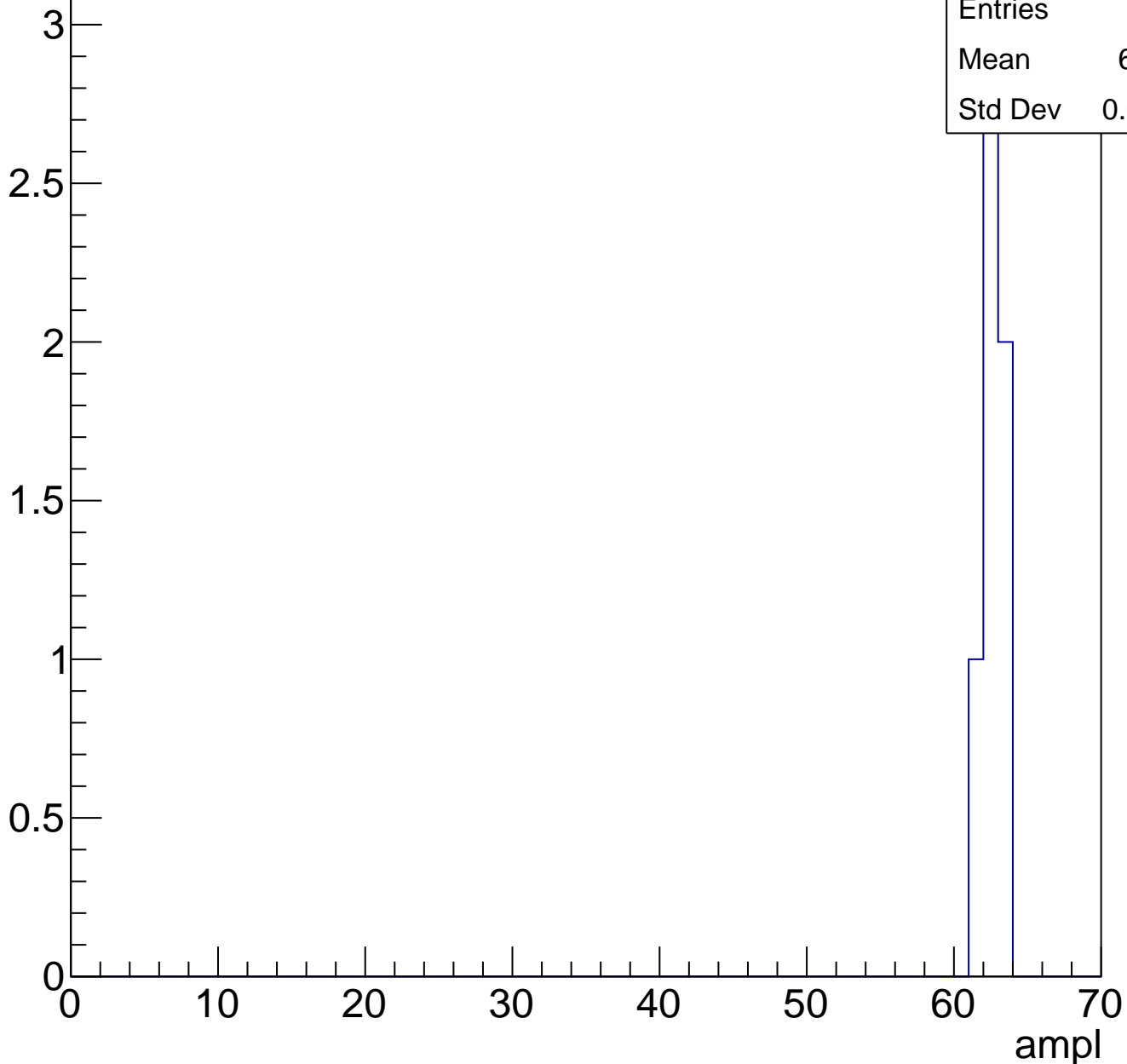
Entries	43
Mean	58.4
Std Dev	9.401



# B0L001S, U21-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U21-ch46, adc0

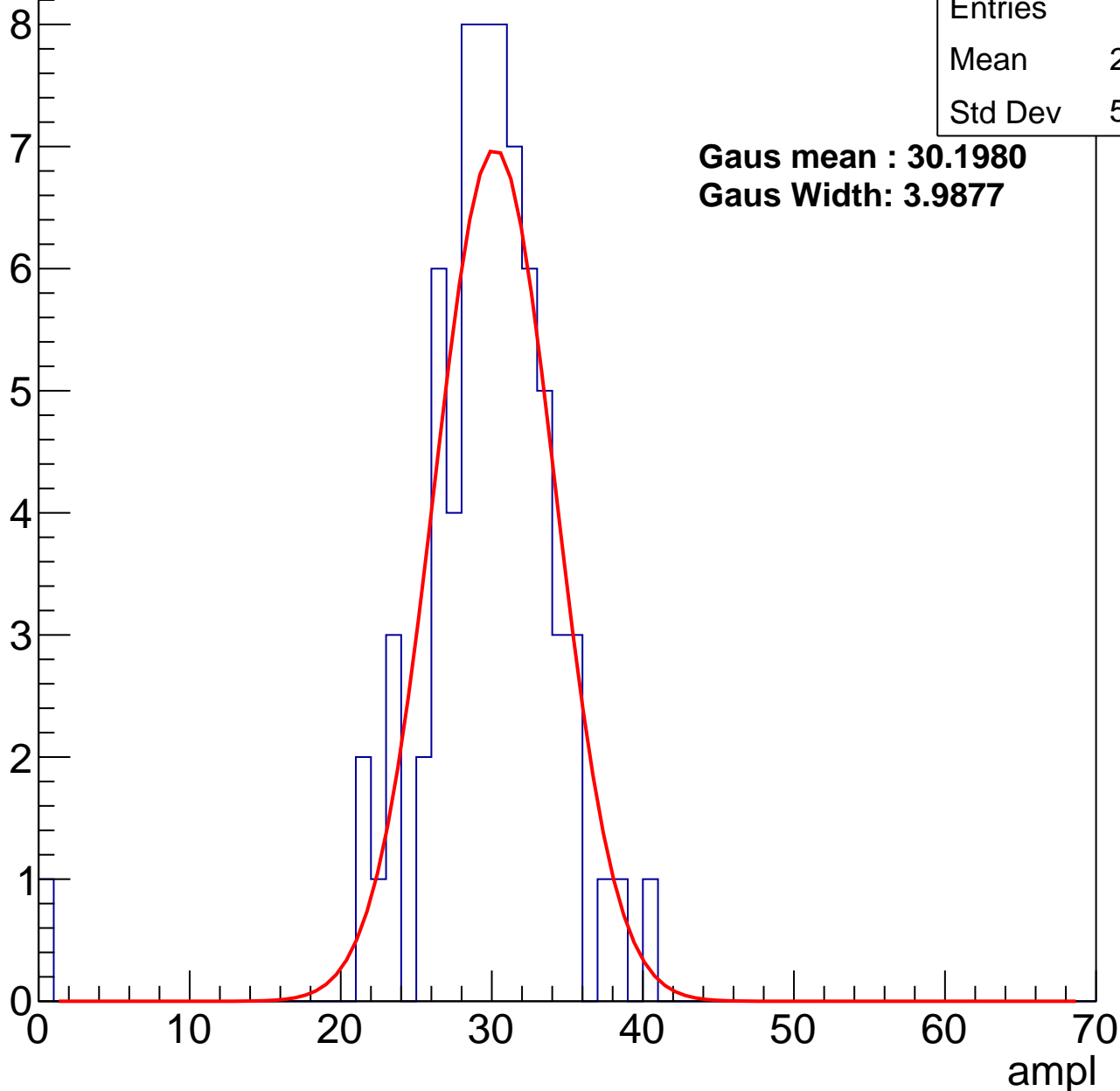
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	29.13
Std Dev	5.146

**Gaus mean : 30.1980**

**Gaus Width: 3.9877**



# B0L001S, U21-ch46, adc1

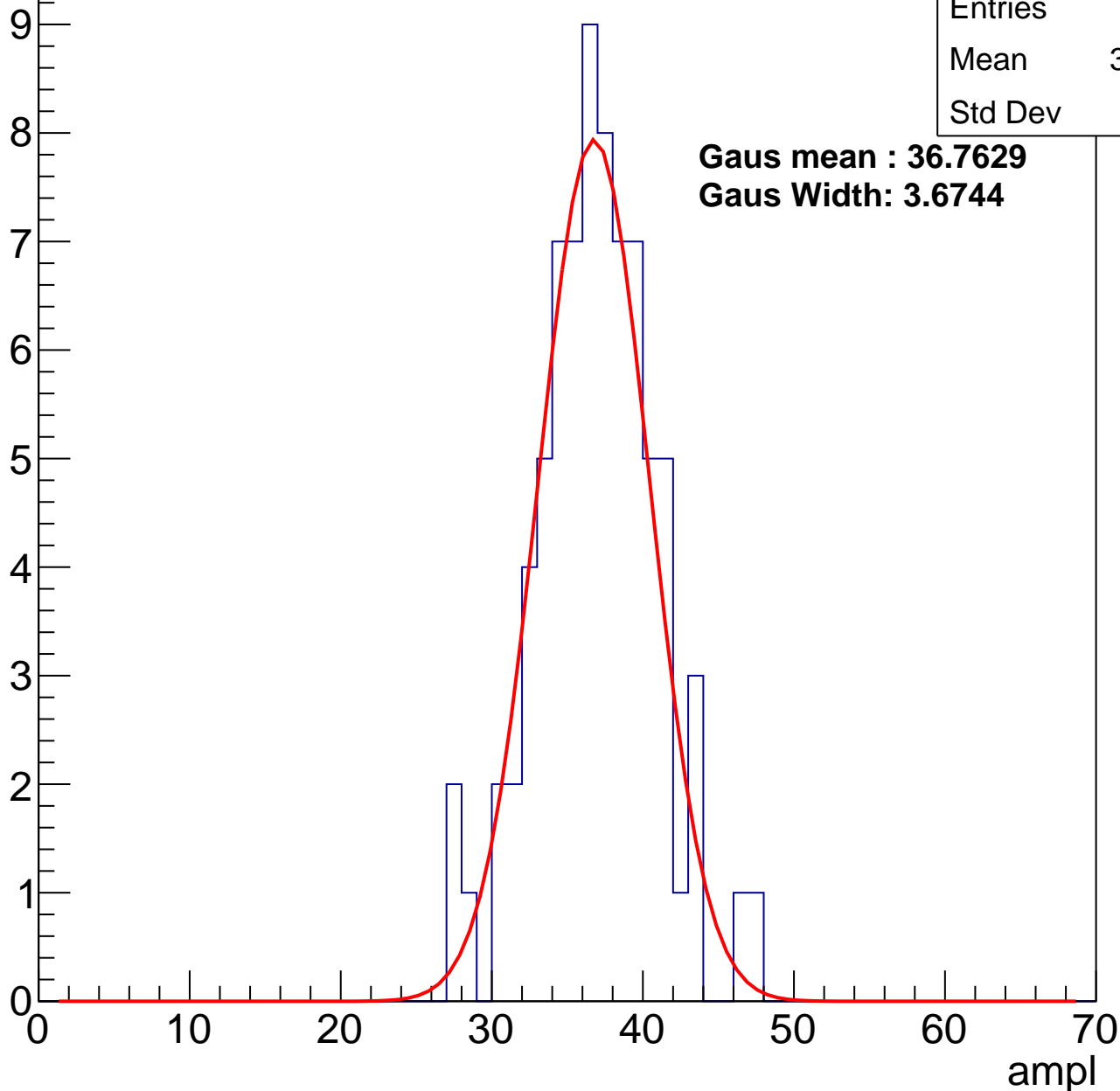
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	36.47
Std Dev	3.92

**Gaus mean : 36.7629**

**Gaus Width: 3.6744**



# B0L001S, U21-ch46, adc2

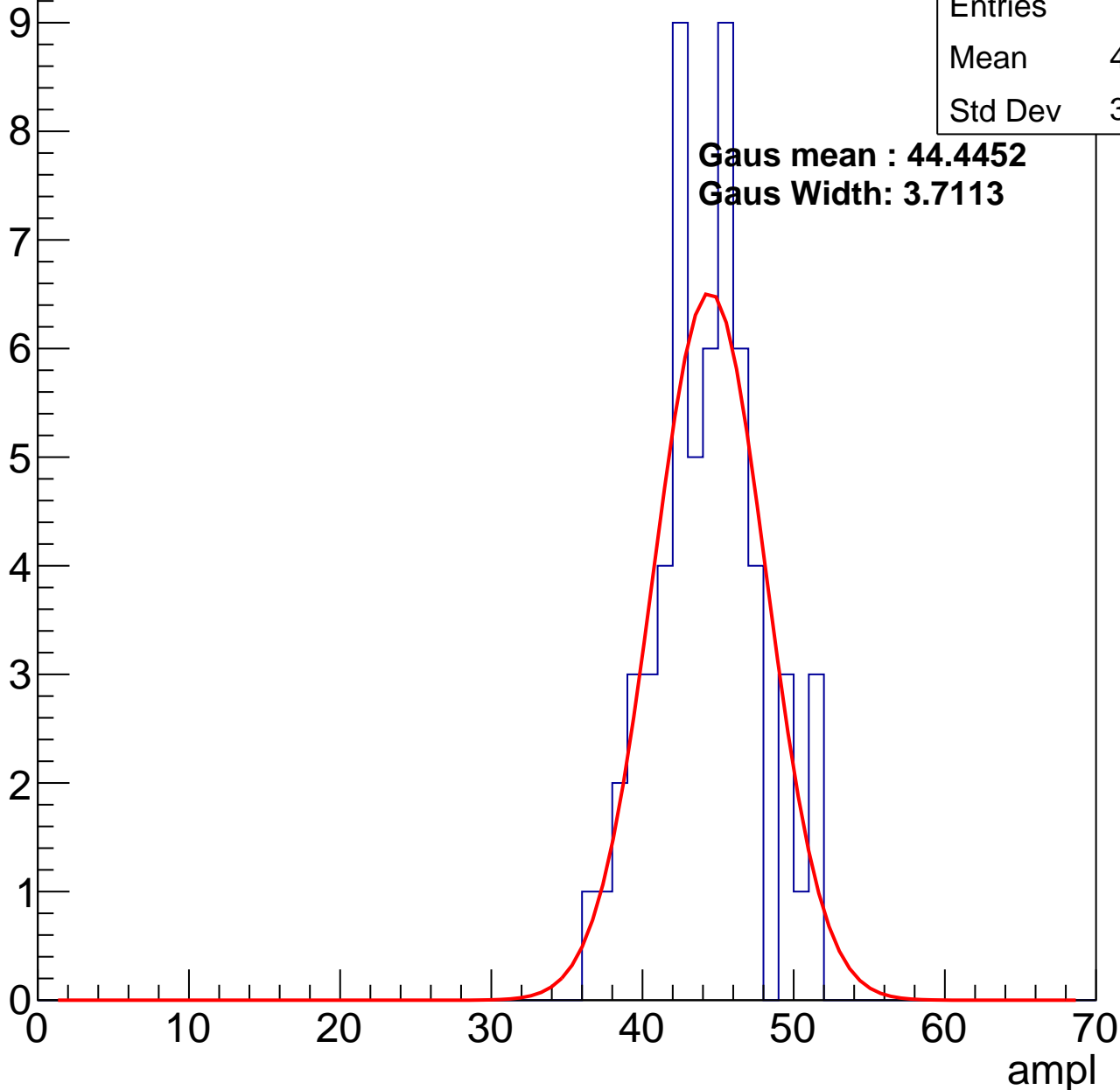
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	43.77
Std Dev	3.437

**Gaus mean : 44.4452**

**Gaus Width: 3.7113**



# B0L001S, U21-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

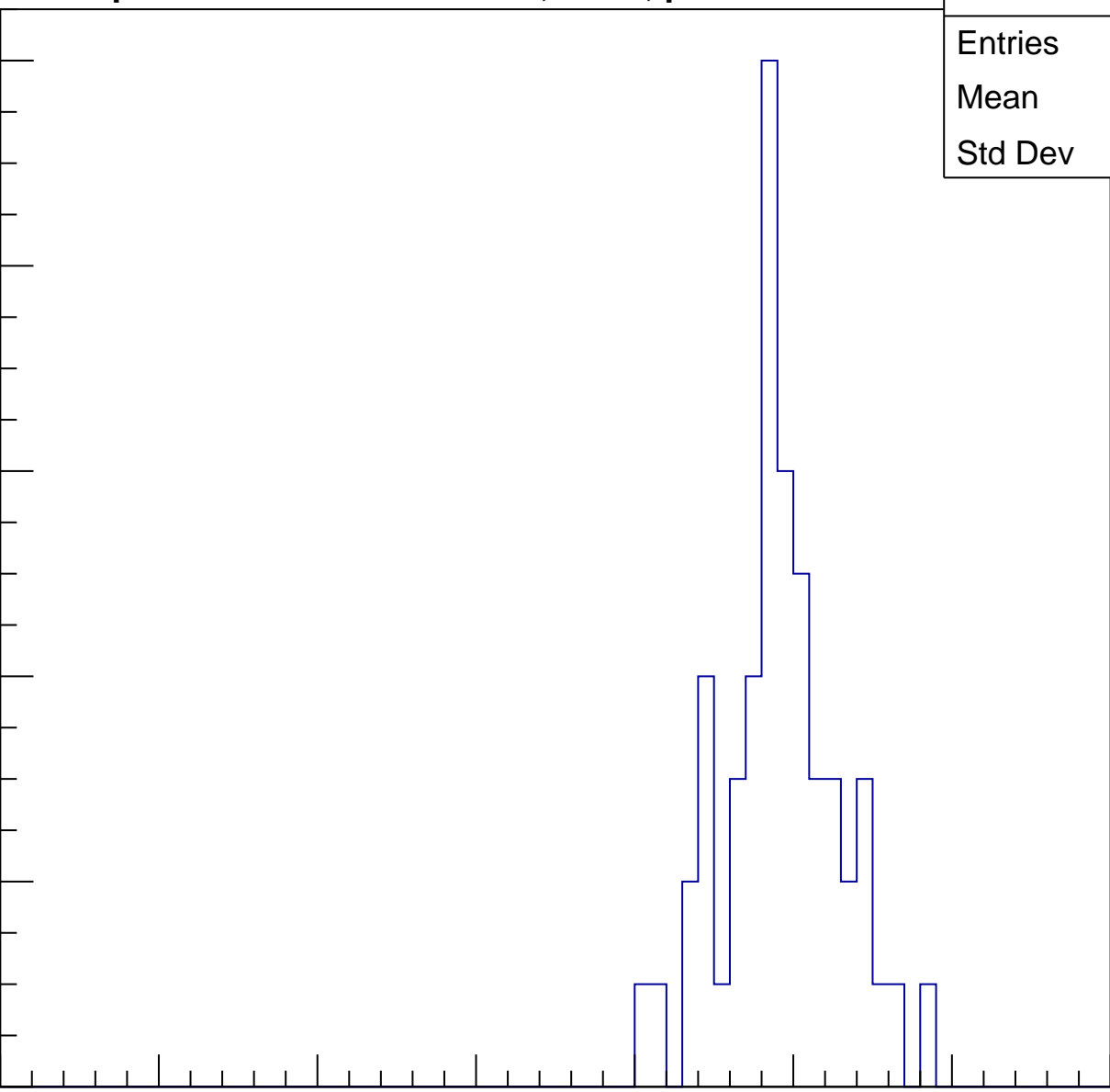
Entries	51
Mean	48.71
Std Dev	3.701

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U21-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	75
Mean	55.21
Std Dev	3.368

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

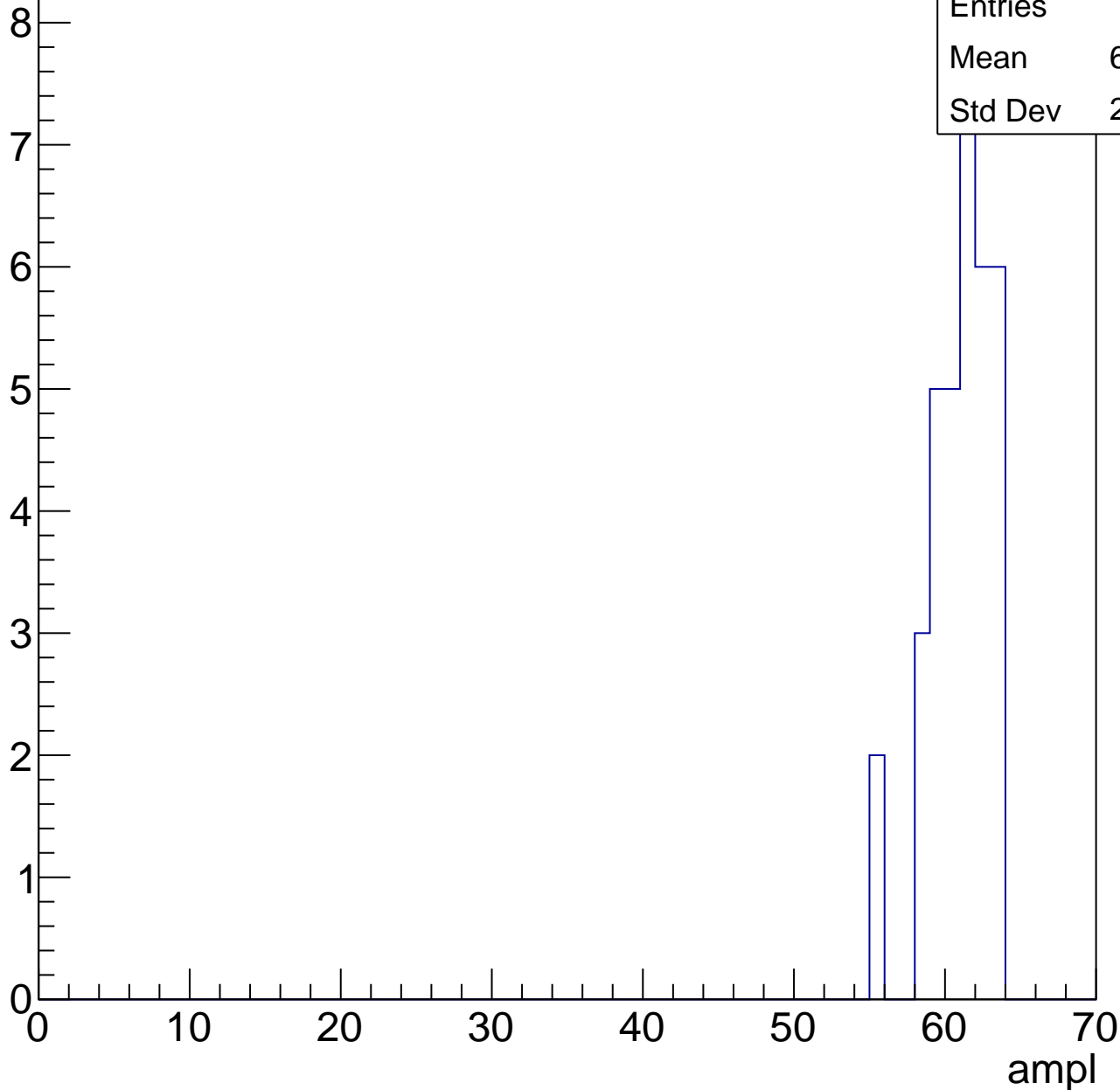
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70

# B0L001S, U21-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

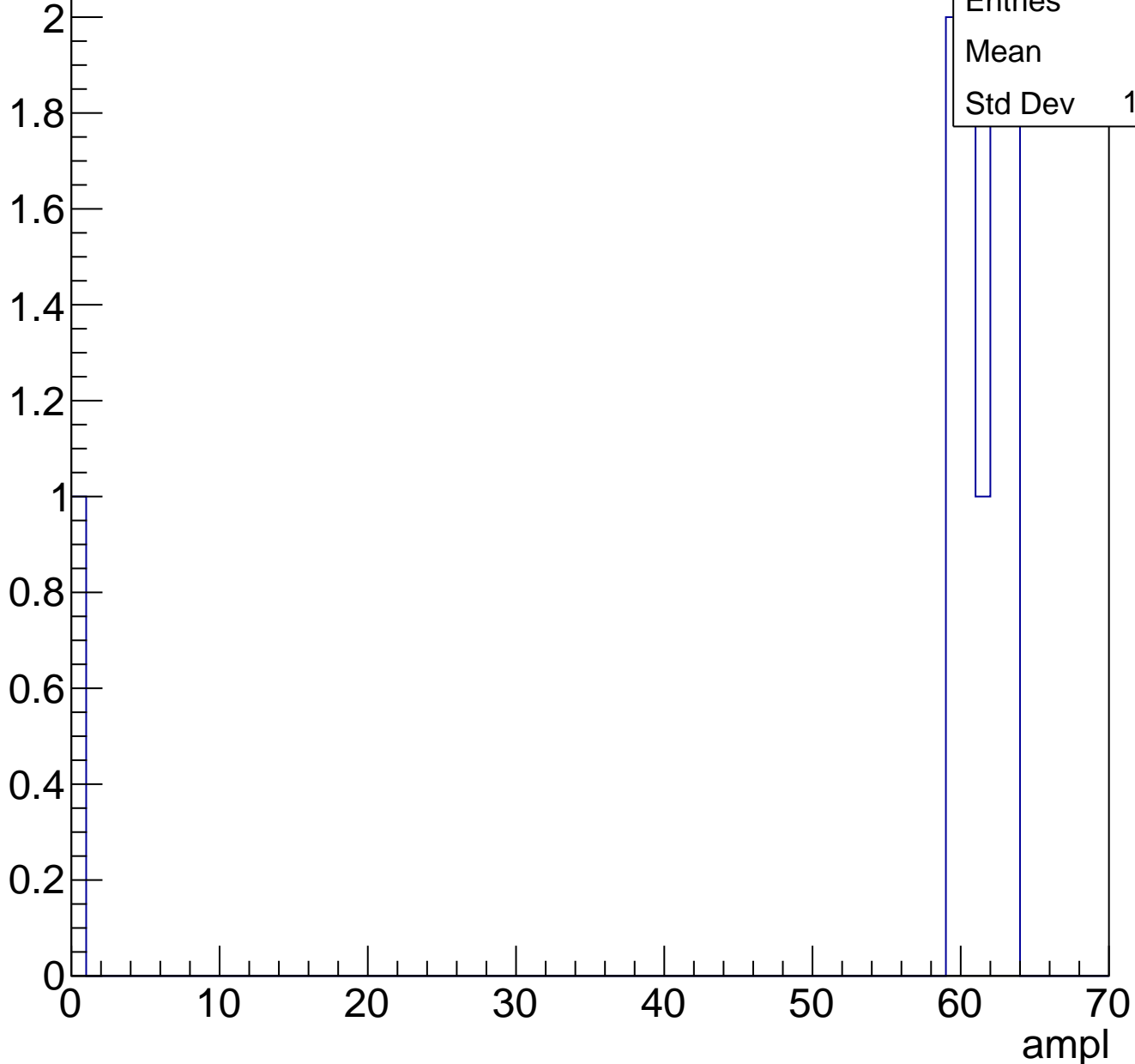
Entries	35
Mean	60.49
Std Dev	2.034



# B0L001S, U21-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U21-ch47, adc0

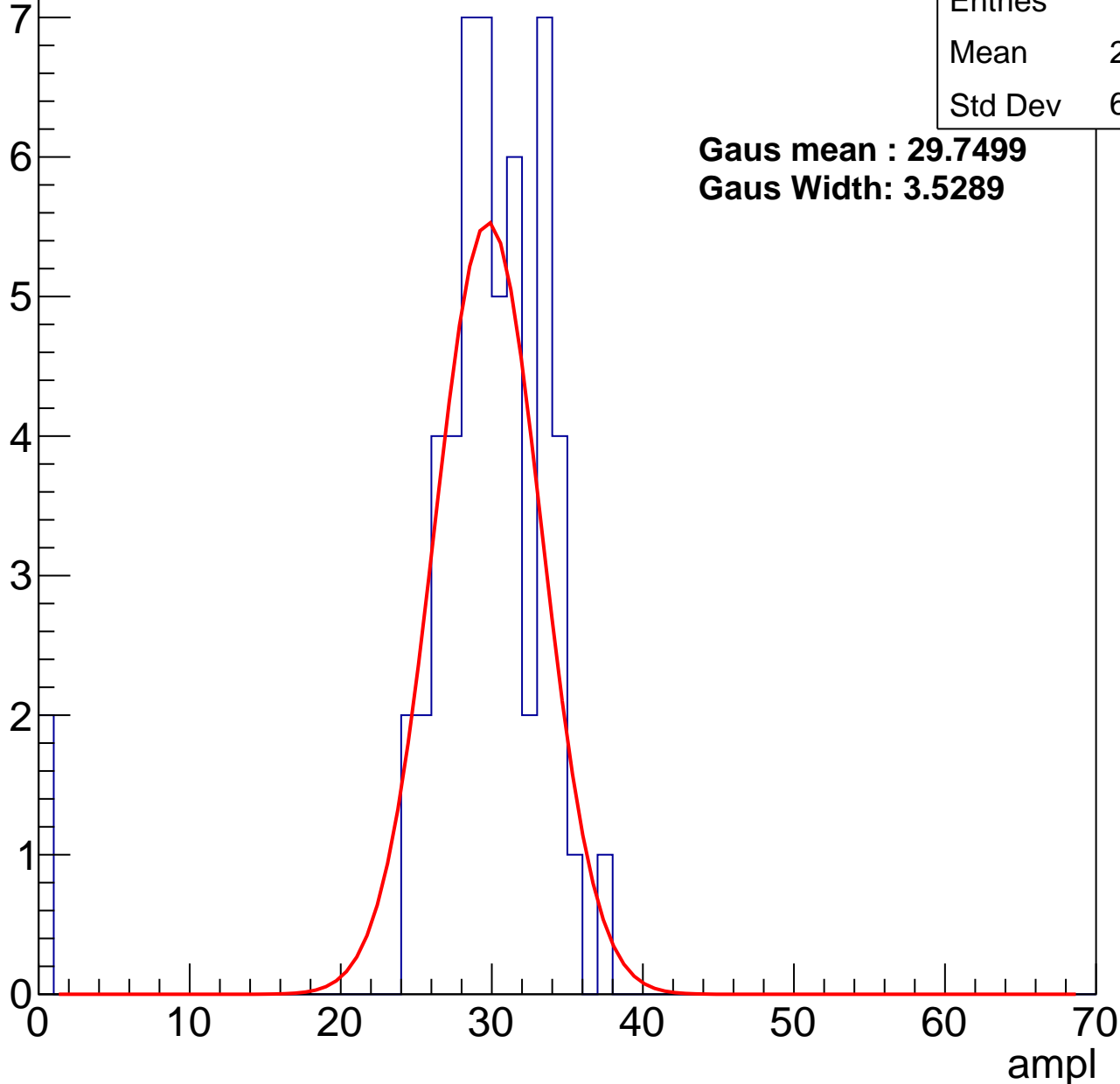
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	28.67
Std Dev	6.348

**Gaus mean : 29.7499**

**Gaus Width: 3.5289**



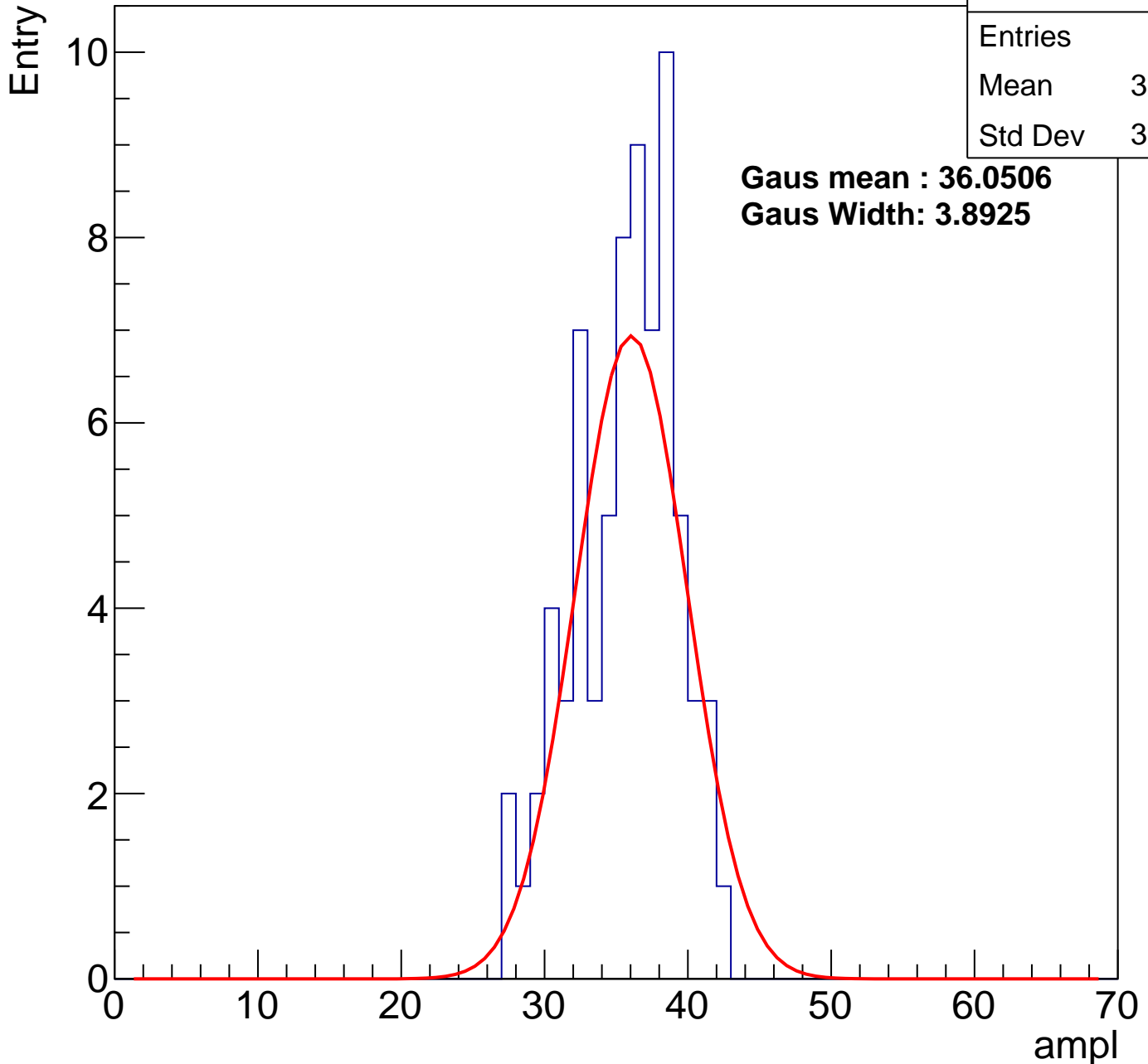
# B0L001S, U21-ch47, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	73
Mean	35.19
Std Dev	3.537

**Gaus mean : 36.0506**

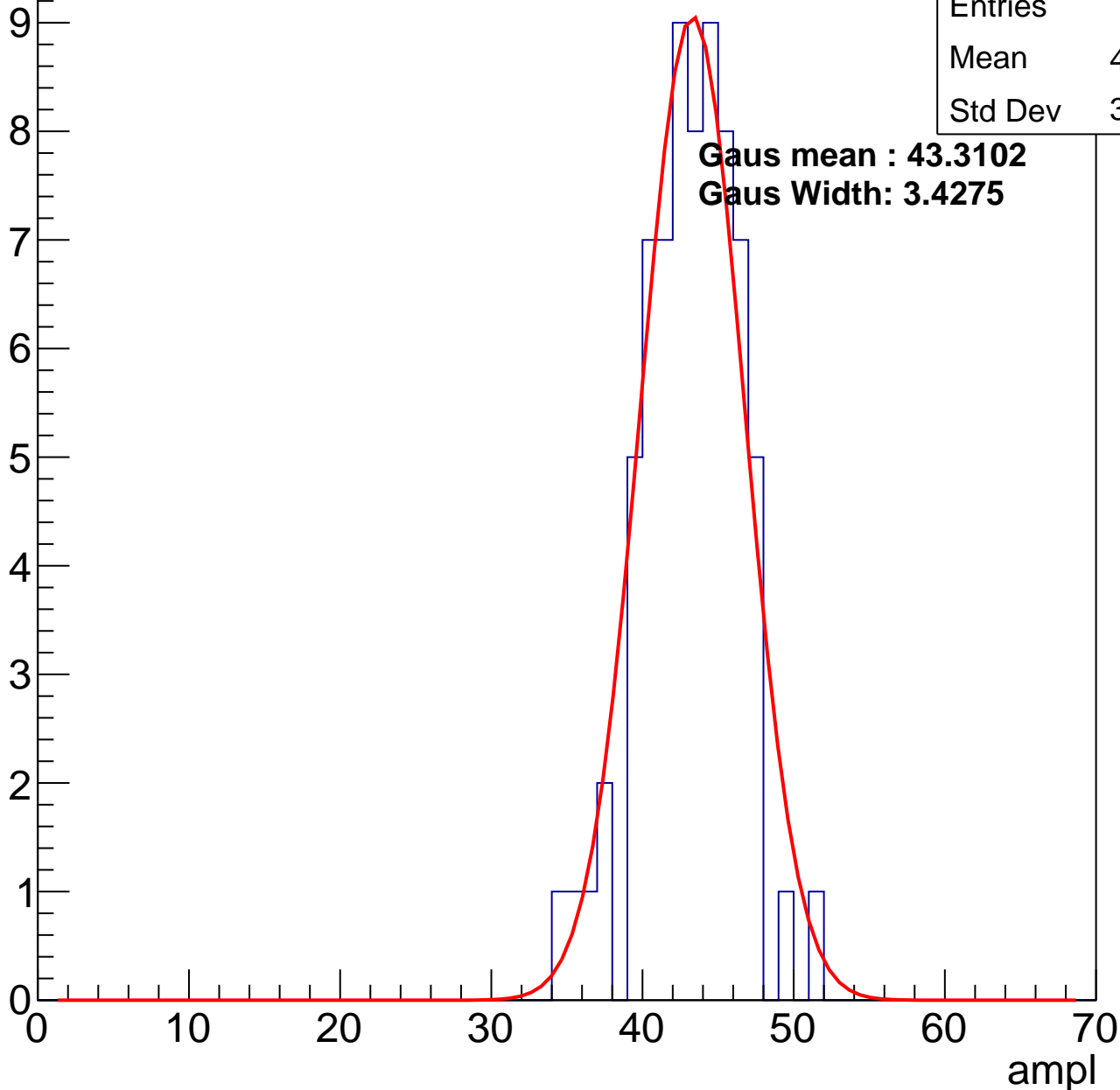
**Gaus Width: 3.8925**



# B0L001S, U21-ch47, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



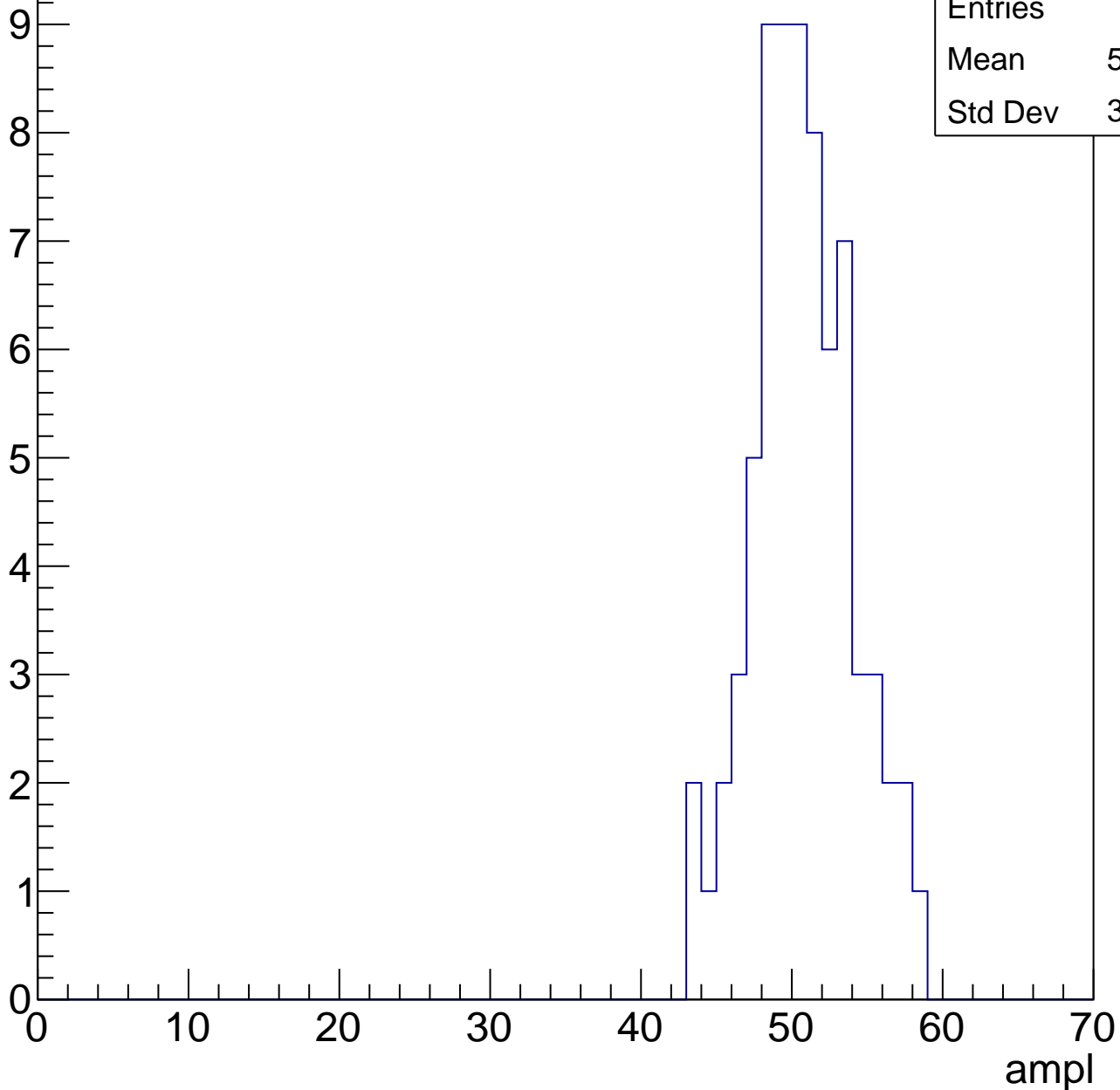
Entries	72
Mean	42.72
Std Dev	3.172

# B0L001S, U21-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	50.25
Std Dev	3.269

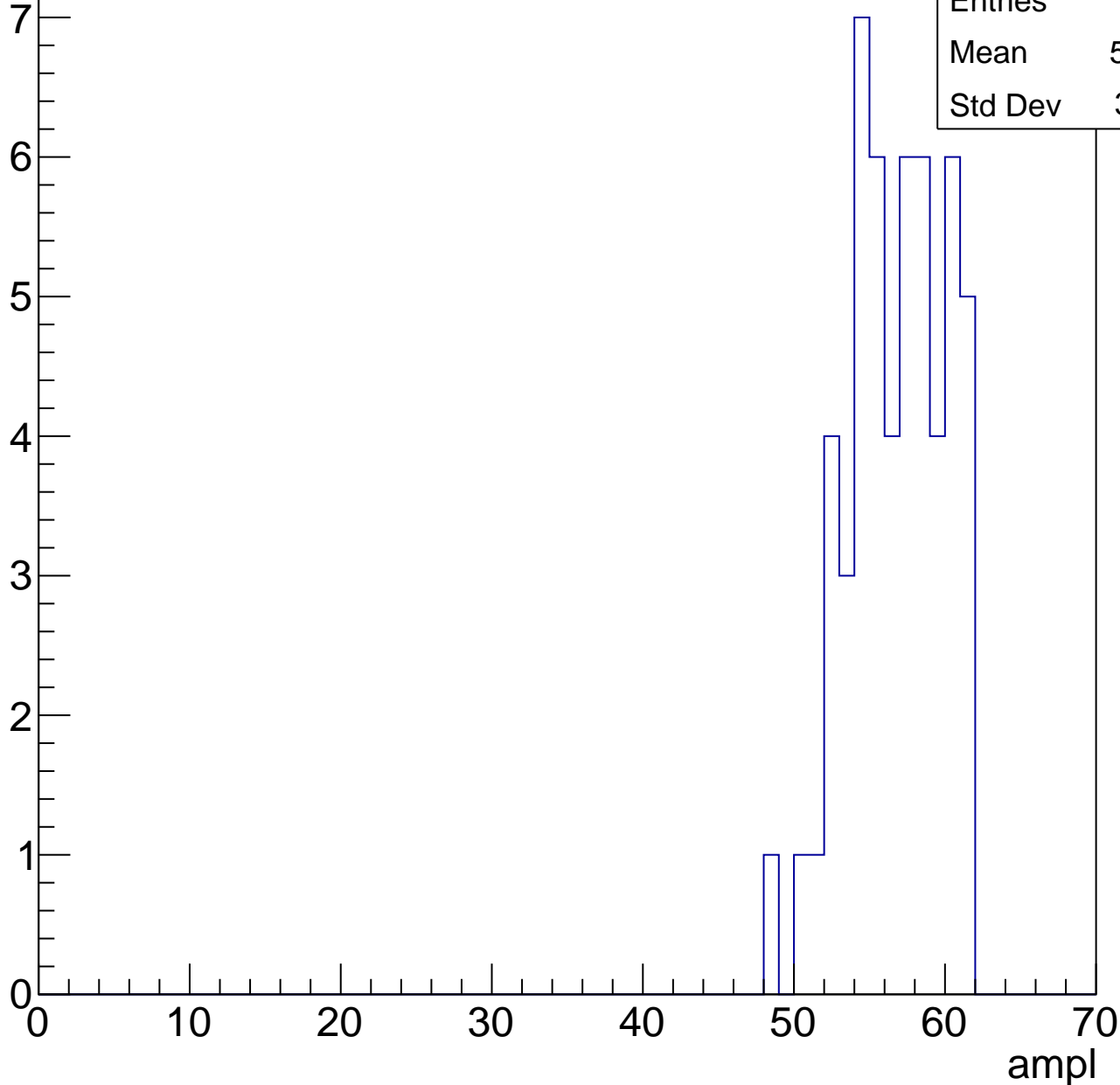


# B0L001S, U21-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	56.28
Std Dev	3.141

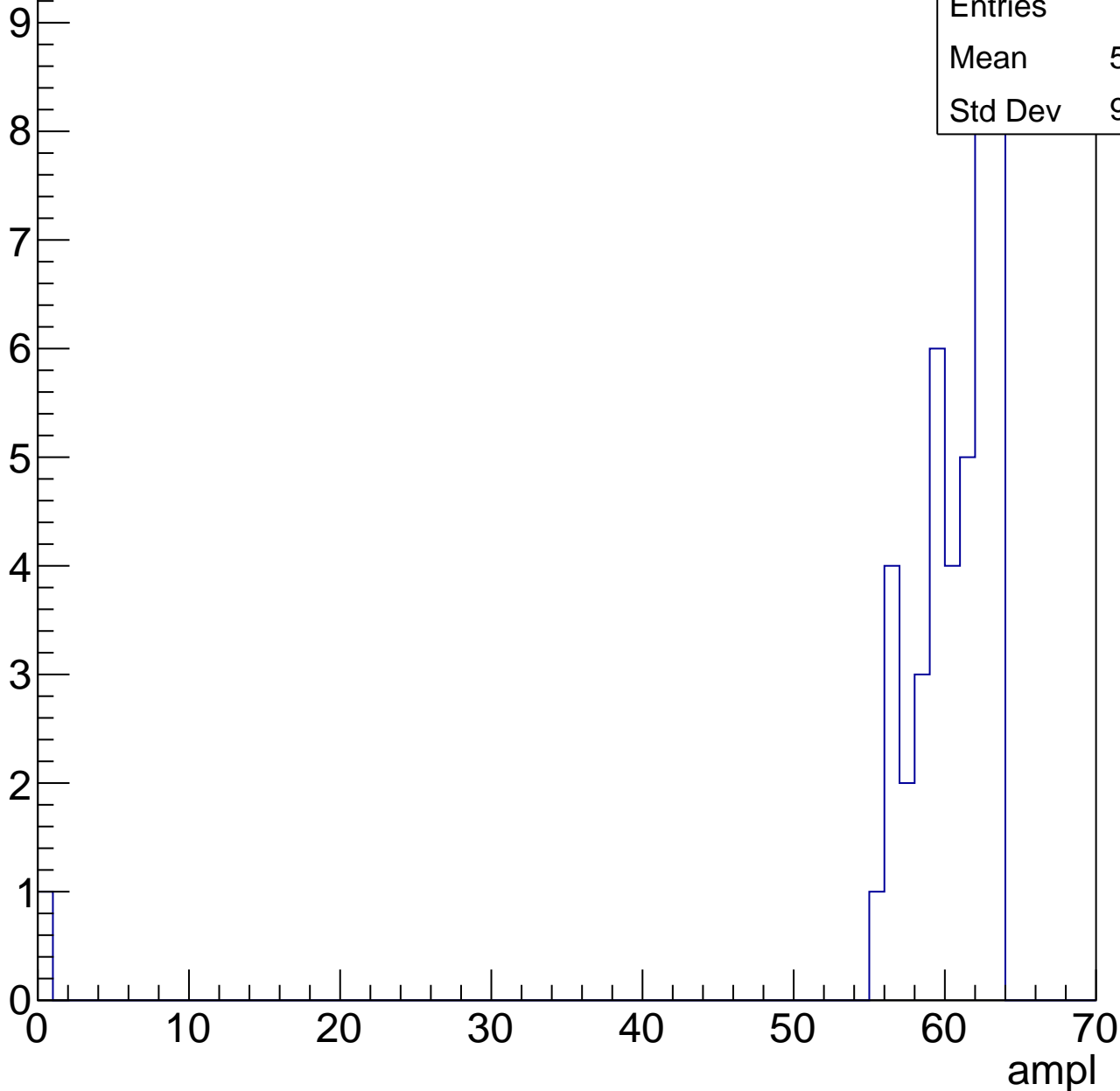


# B0L001S, U21-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	44
Mean	58.89
Std Dev	9.284



# B0L001S, U21-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	4
Mean	0
Std Dev	0

# B0L001S, U21-ch48, adc0

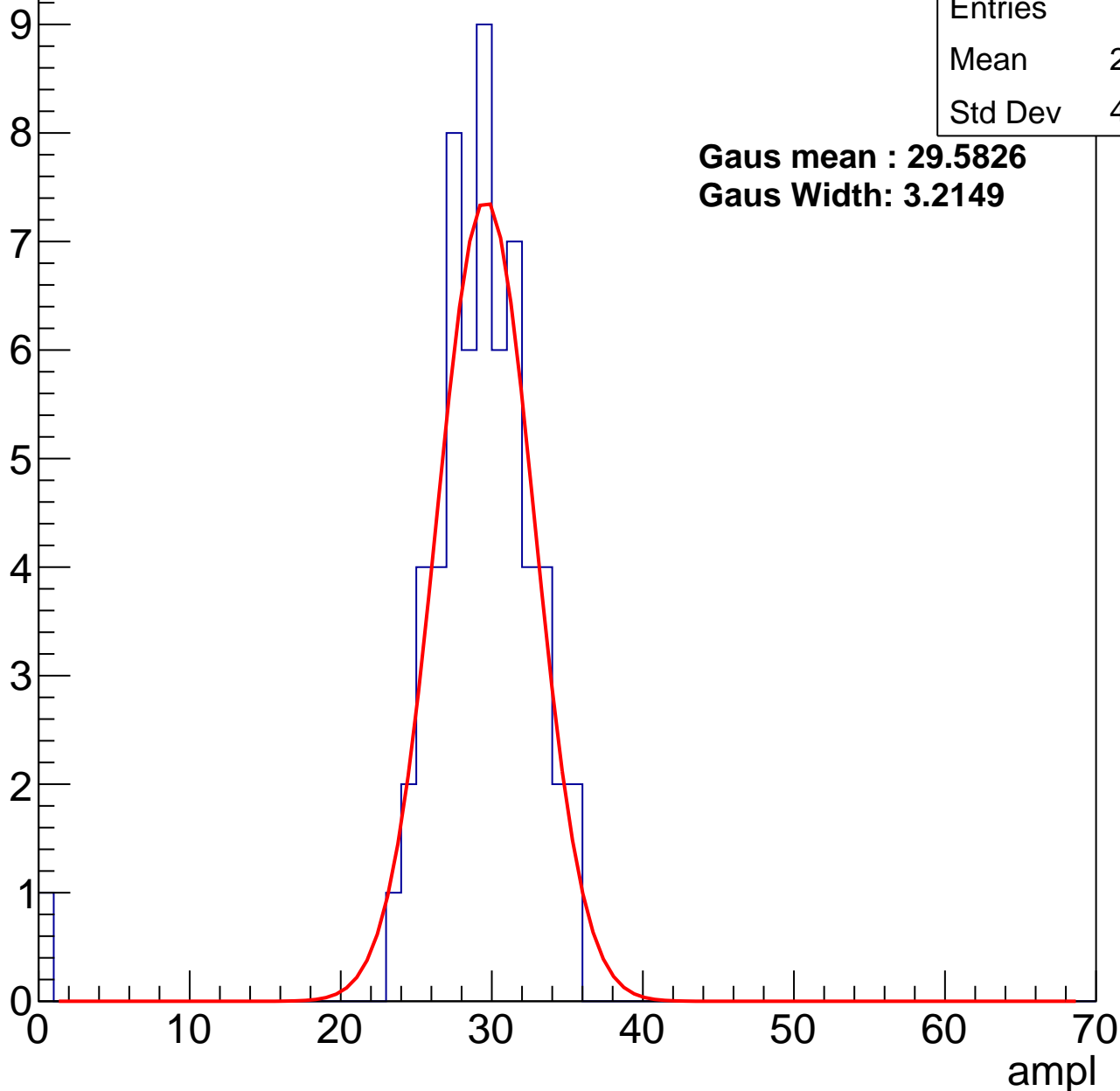
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	28.58
Std Dev	4.674

**Gaus mean : 29.5826**

**Gaus Width: 3.2149**



# B0L001S, U21-ch48, adc1

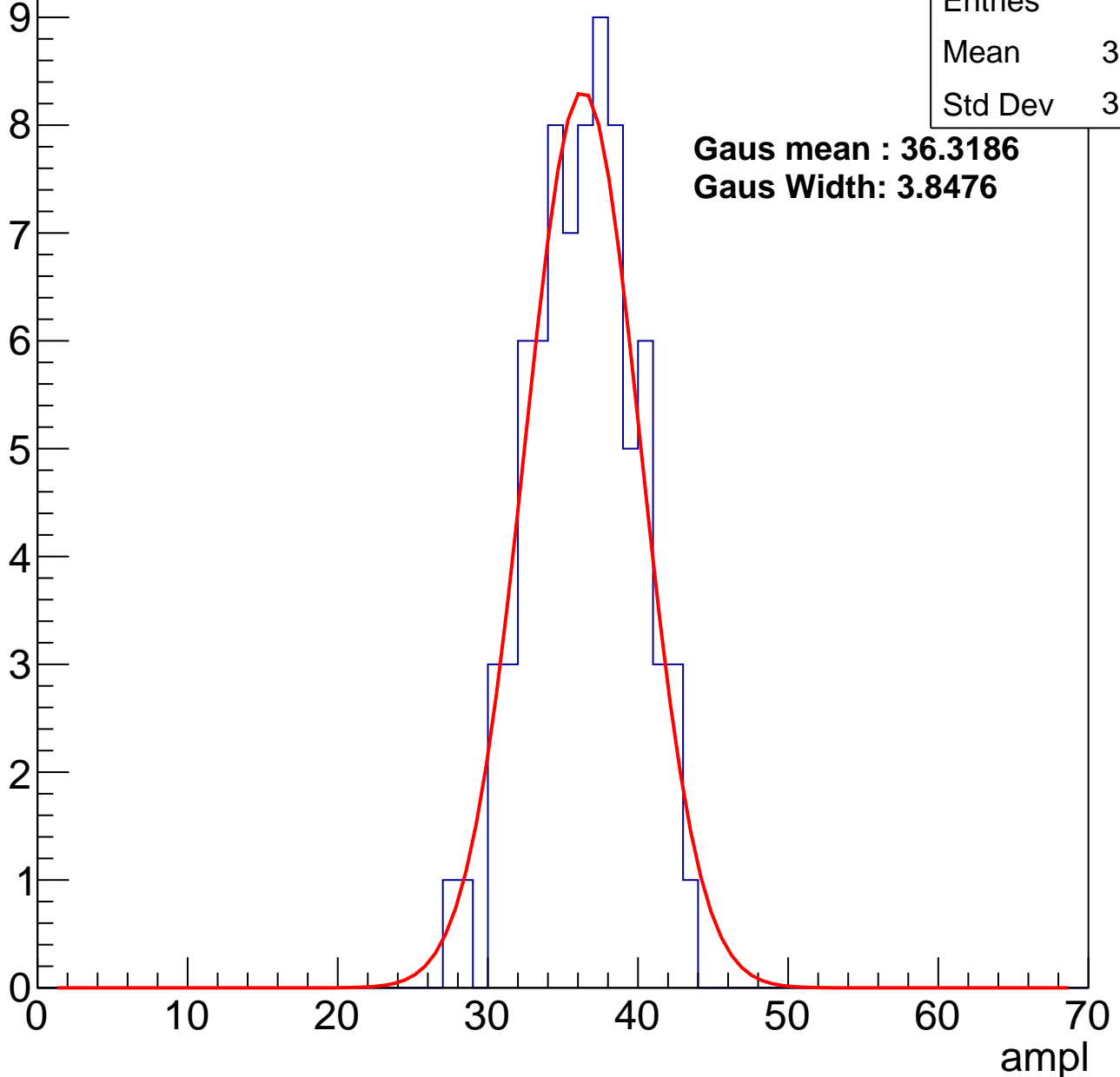
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	35.86
Std Dev	3.452

**Gaus mean : 36.3186**

**Gaus Width: 3.8476**



# B0L001S, U21-ch48, adc2

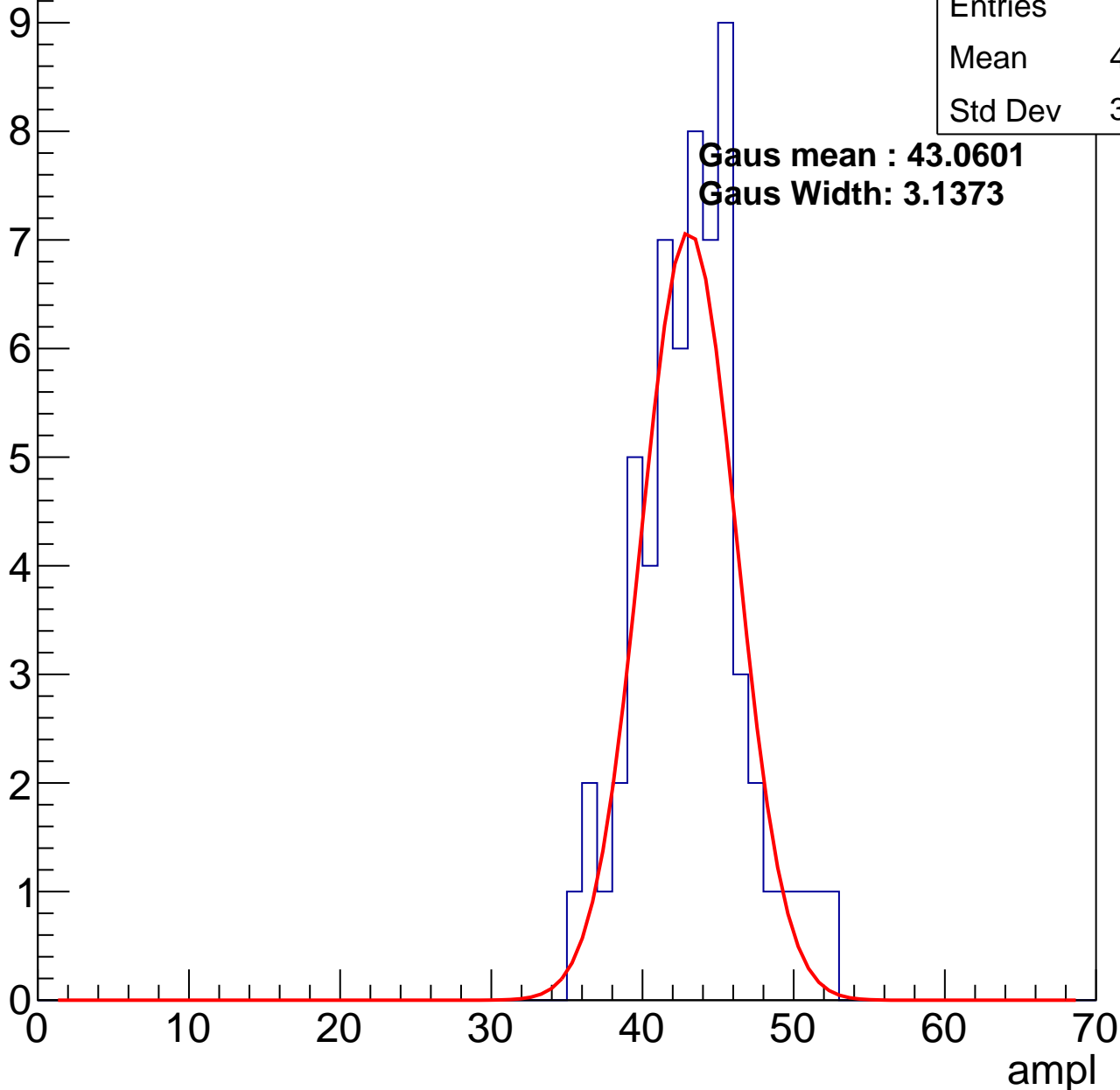
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	42.79
Std Dev	3.483

**Gaus mean : 43.0601**

**Gaus Width: 3.1373**

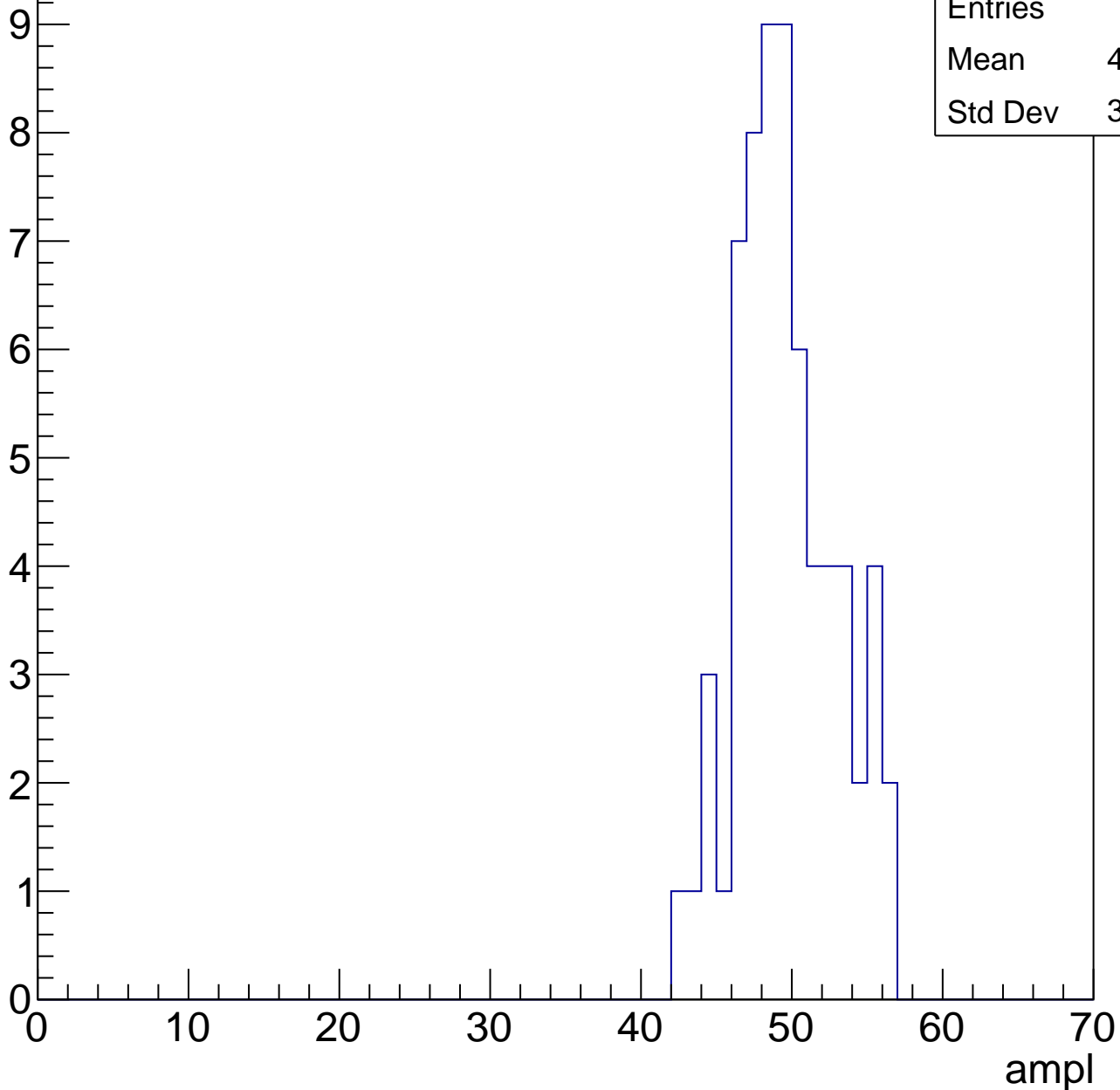


# B0L001S, U21-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	49.18
Std Dev	3.262

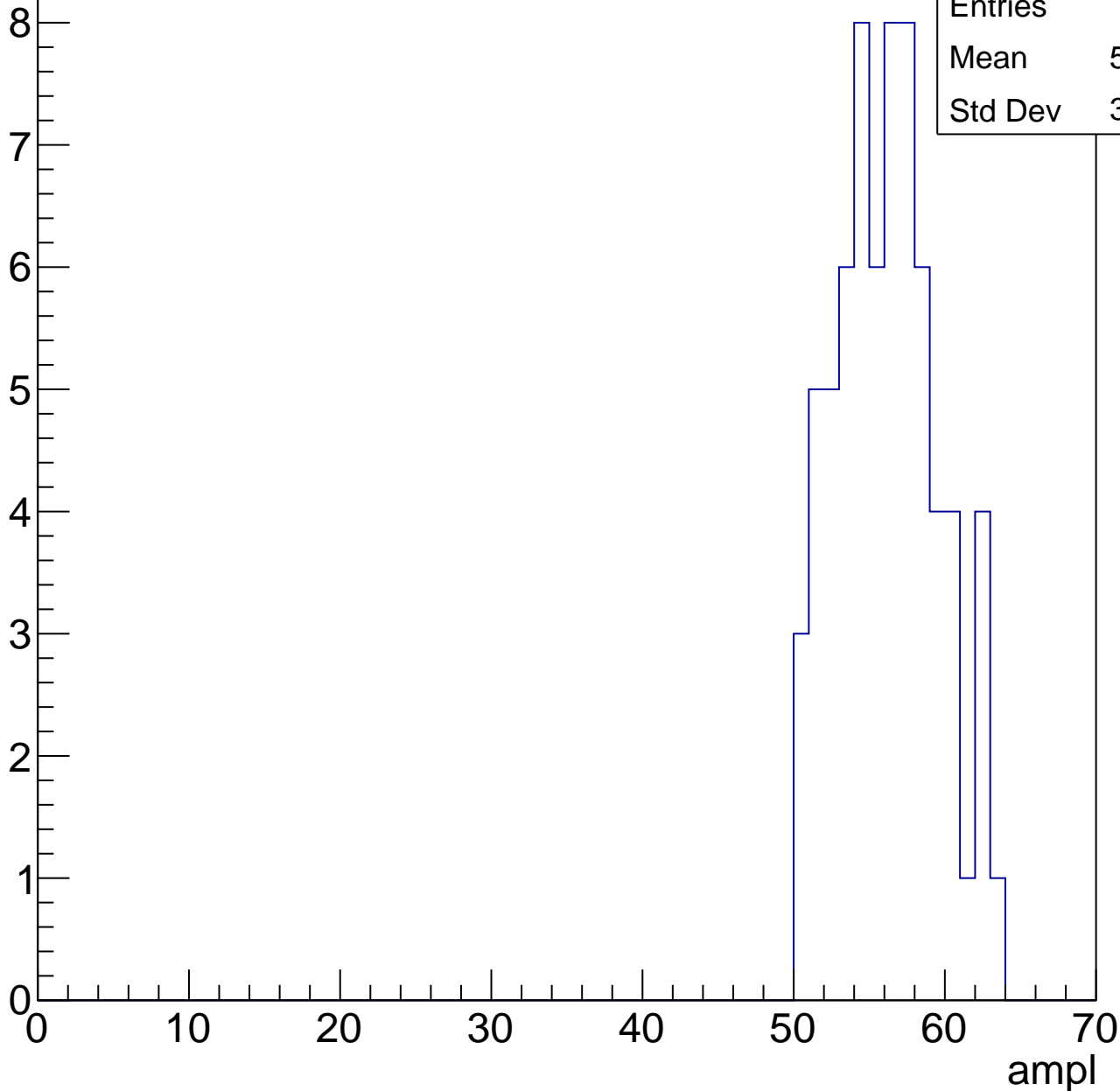


# B0L001S, U21-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	55.72
Std Dev	3.296

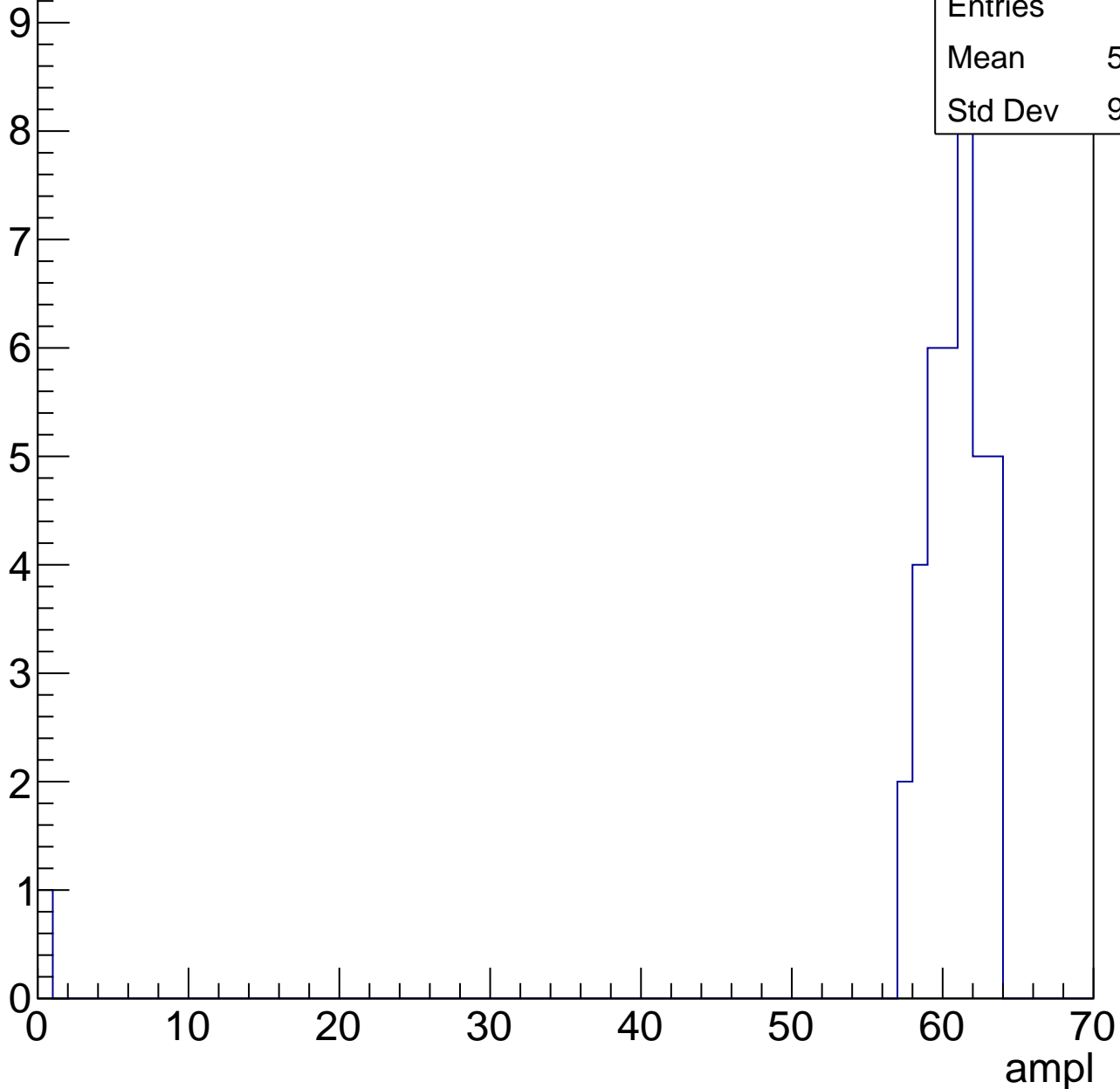


# B0L001S, U21-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

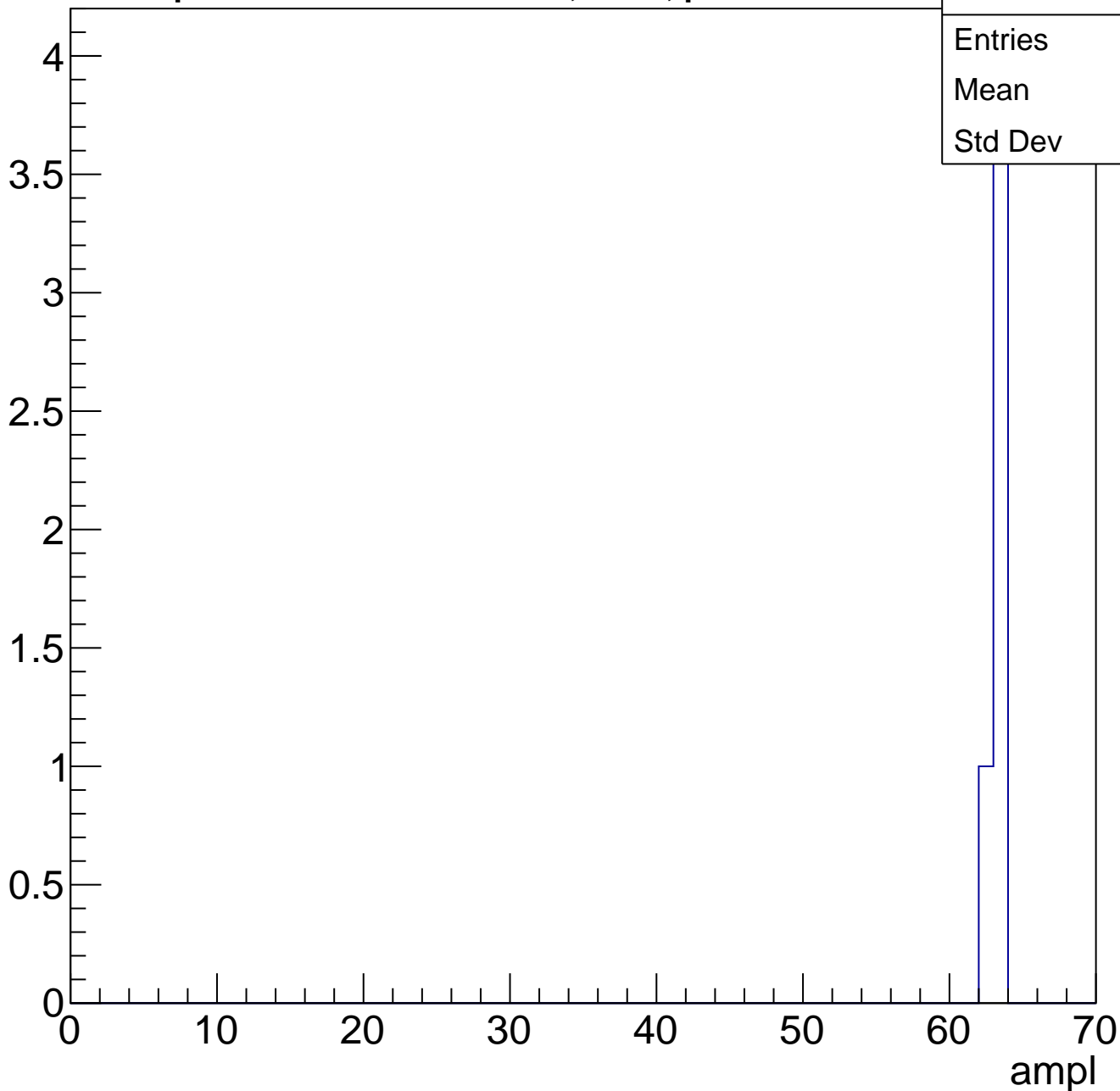
Entries	38
Mean	58.79
Std Dev	9.812



# B0L001S, U21-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	5
Mean	62.8
Std Dev	0.4



# B0L001S, U21-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U21-ch49, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	70
Mean	31.97
Std Dev	3.468

**Gaus mean : 32.4690**

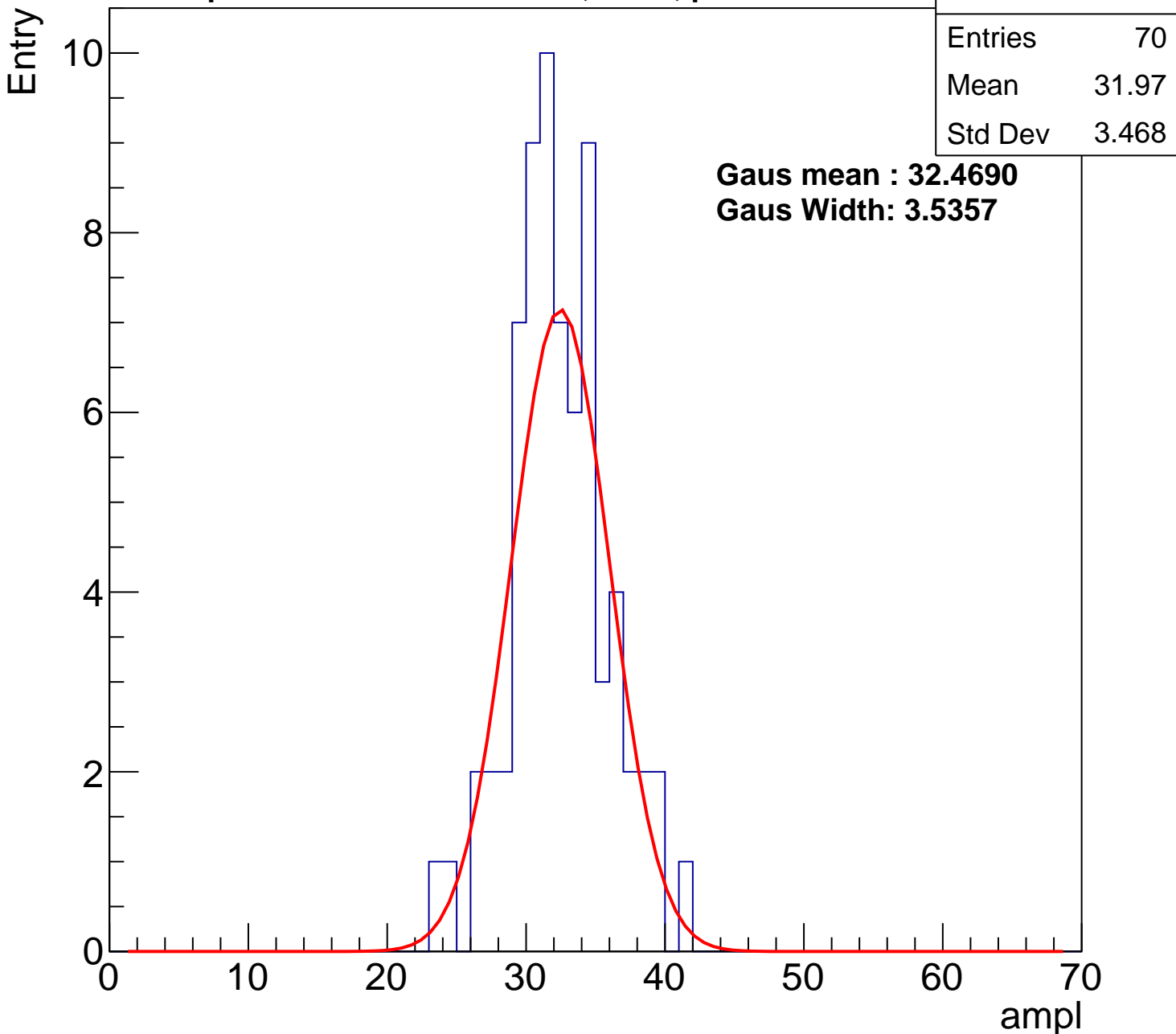
**Gaus Width: 3.5357**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U21-ch49, adc1

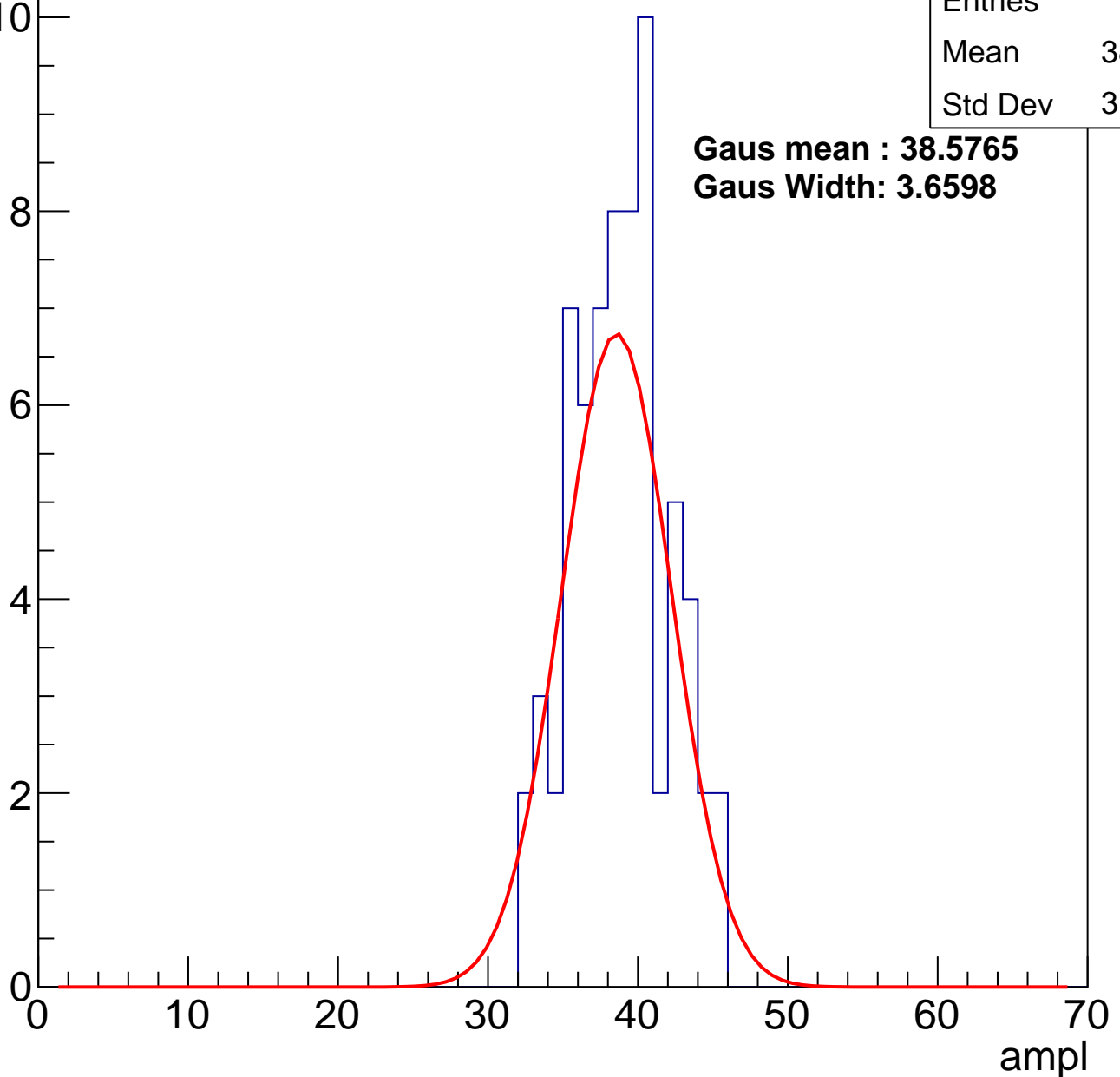
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	38.37
Std Dev	3.162

**Gaus mean : 38.5765**

**Gaus Width: 3.6598**



# B0L001S, U21-ch49, adc2

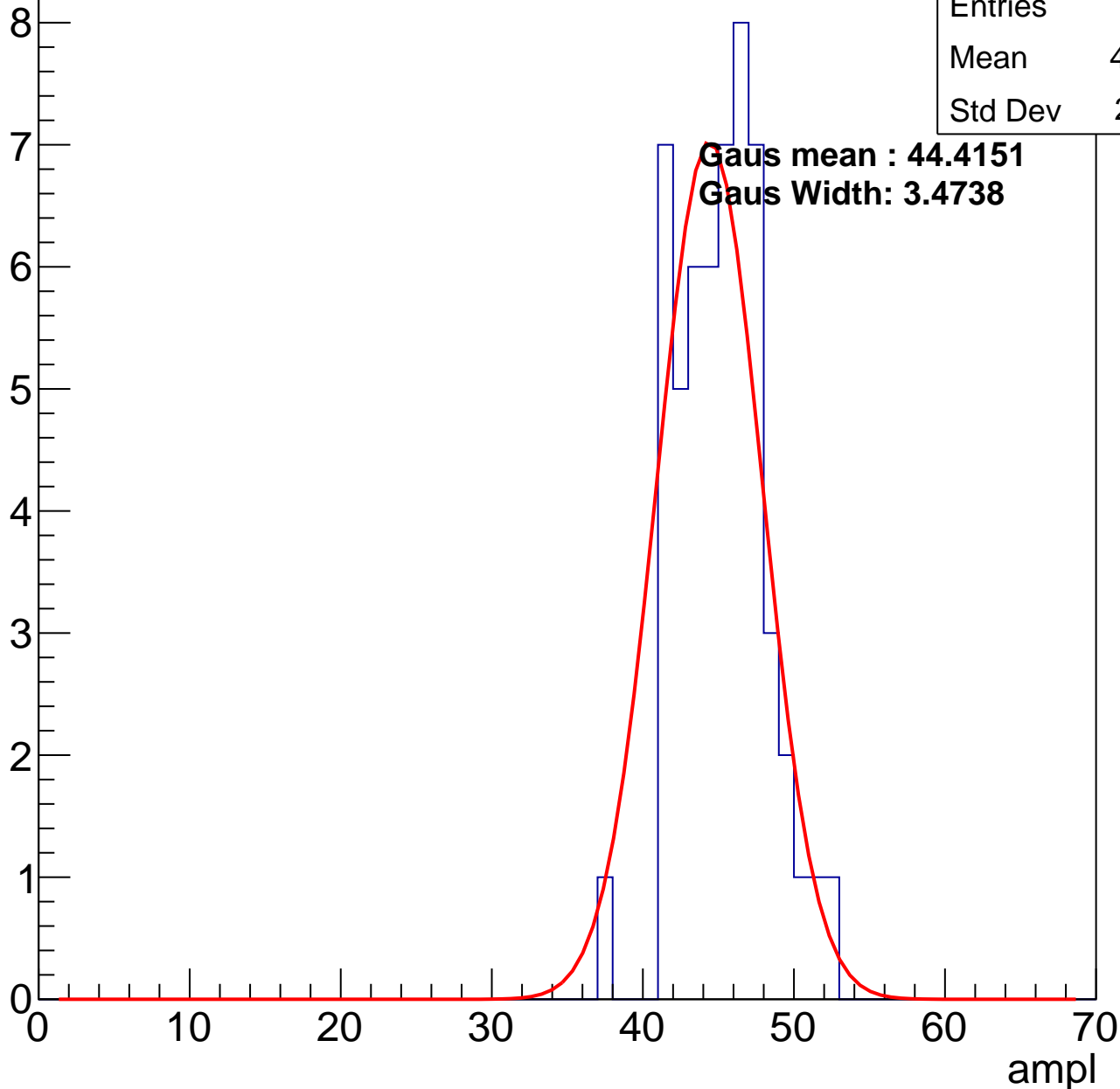
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	44.78
Std Dev	2.871

**Gaus mean : 44.4151**

**Gaus Width: 3.4738**

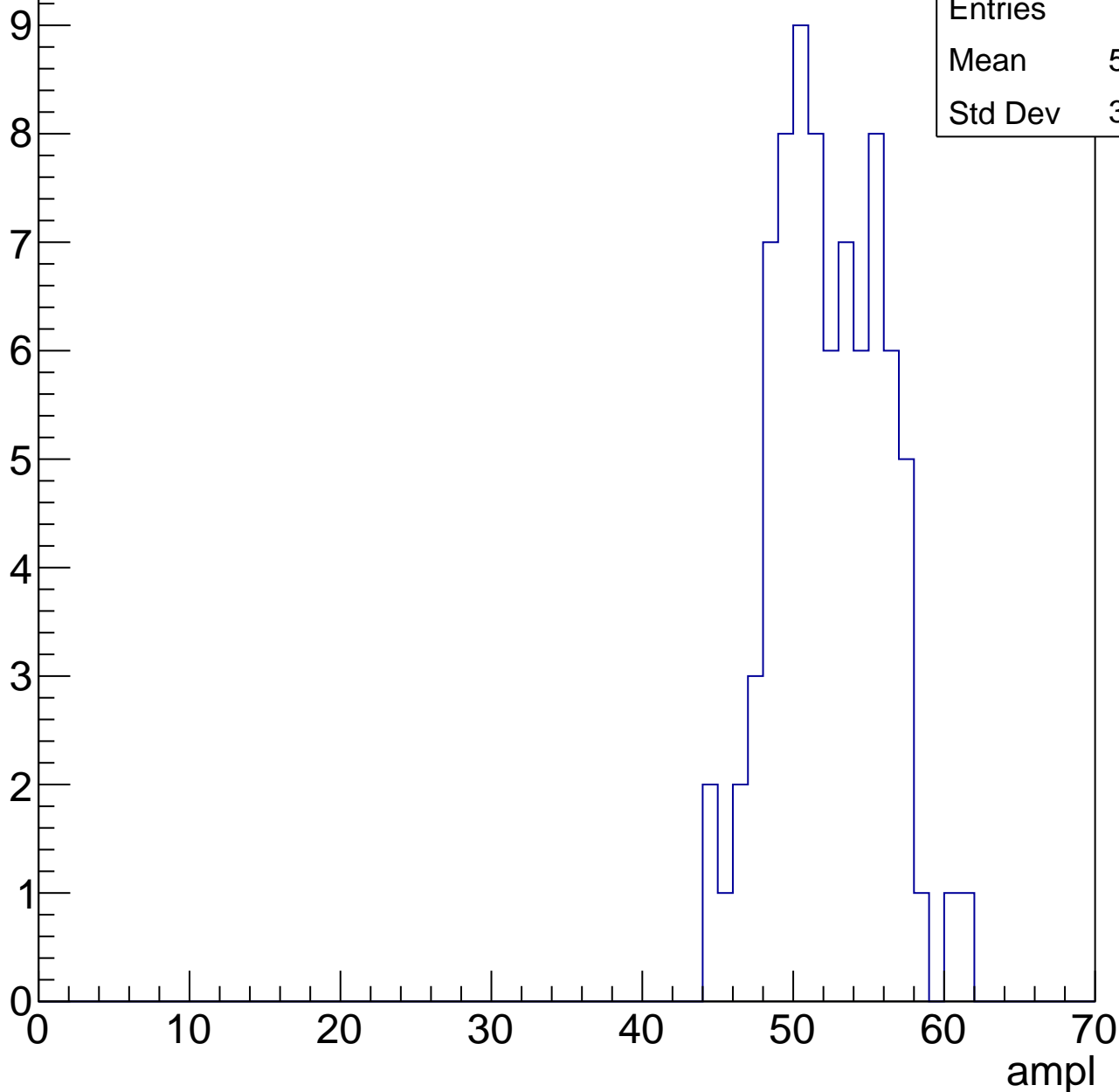


# B0L001S, U21-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

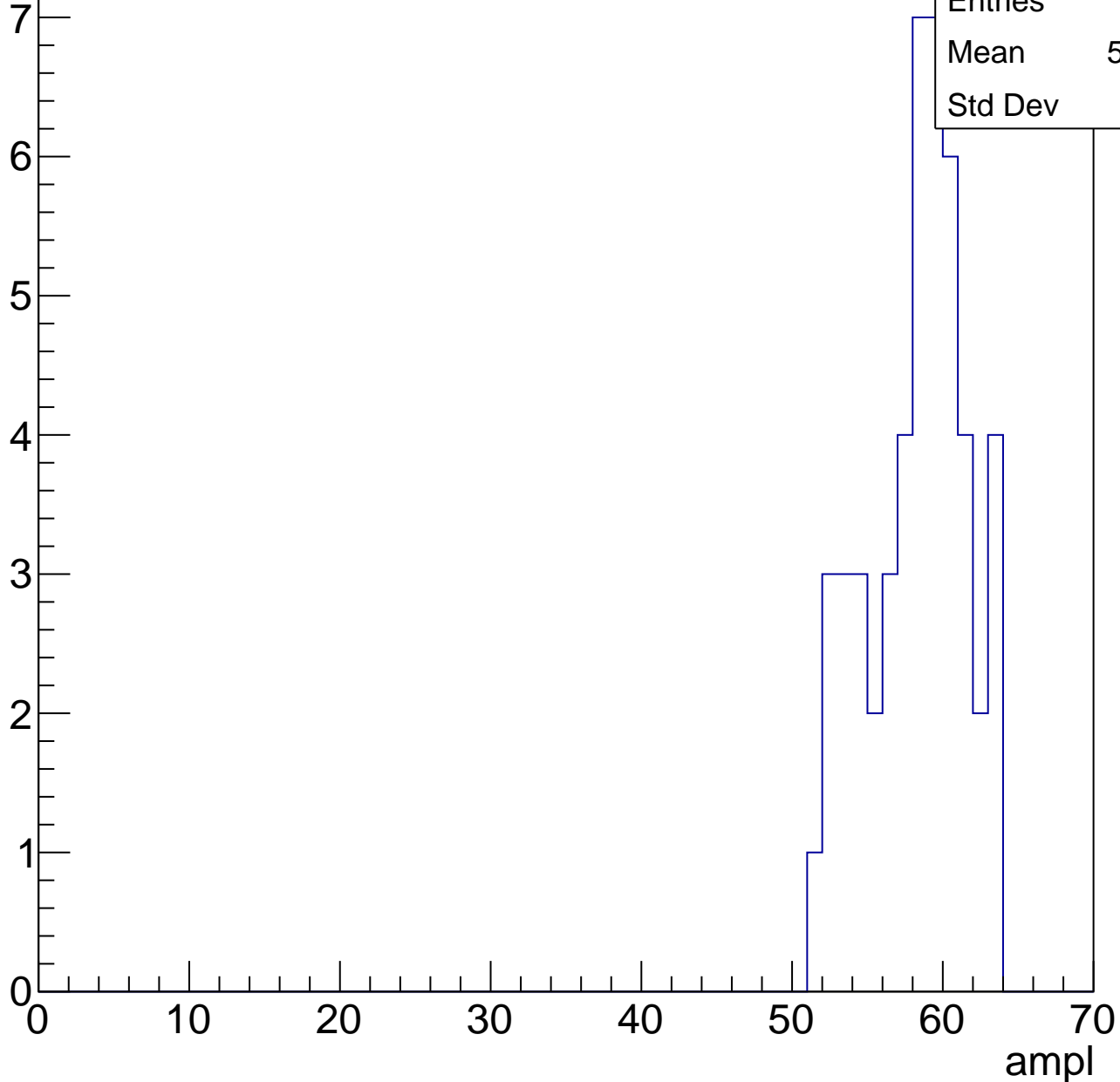
Entries	81
Mean	51.84
Std Dev	3.609



# B0L001S, U21-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

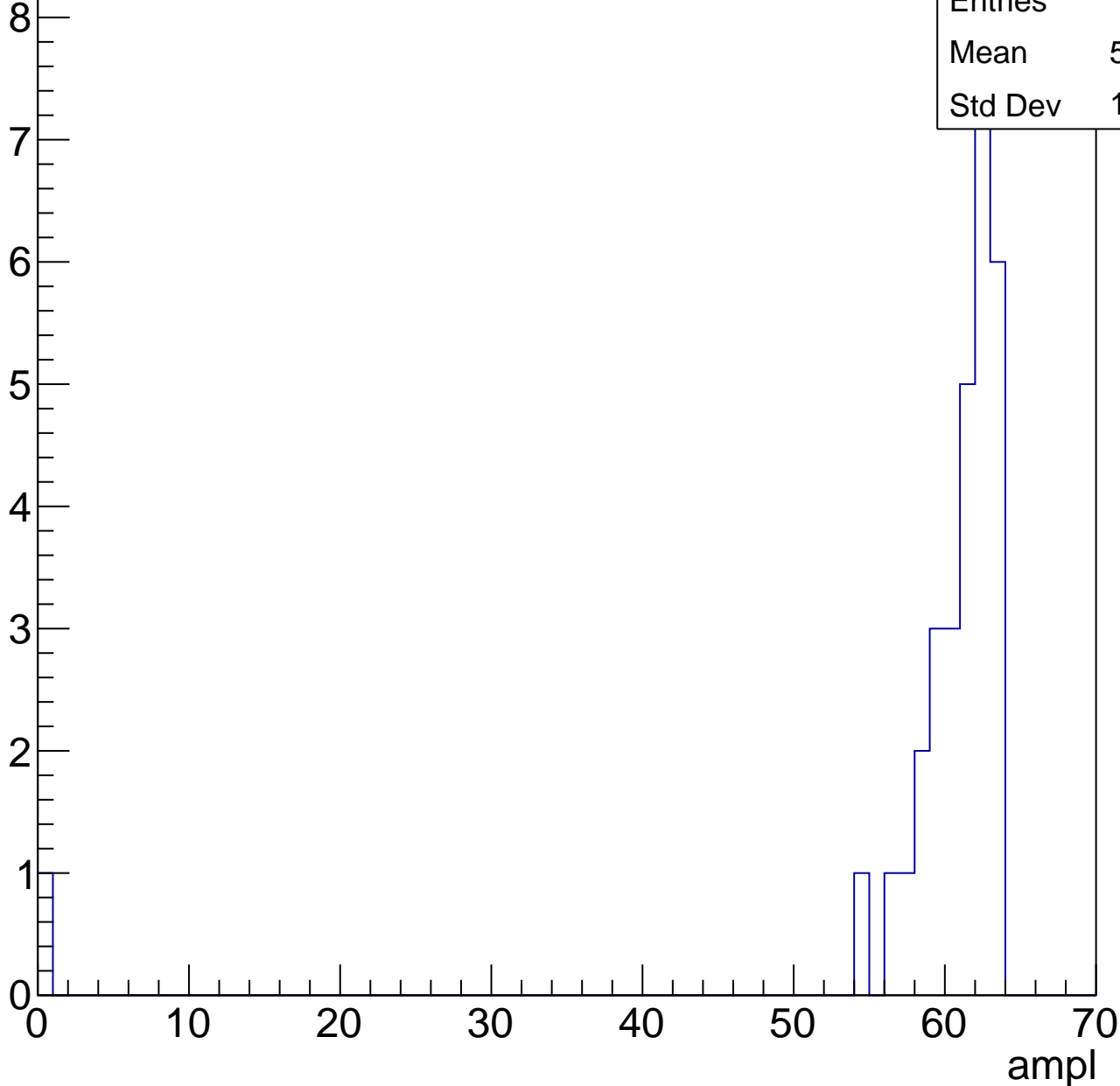


# B0L001S, U21-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	31
Mean	58.68
Std Dev	10.94



# B0L001S, U21-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U21-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch50, adc0

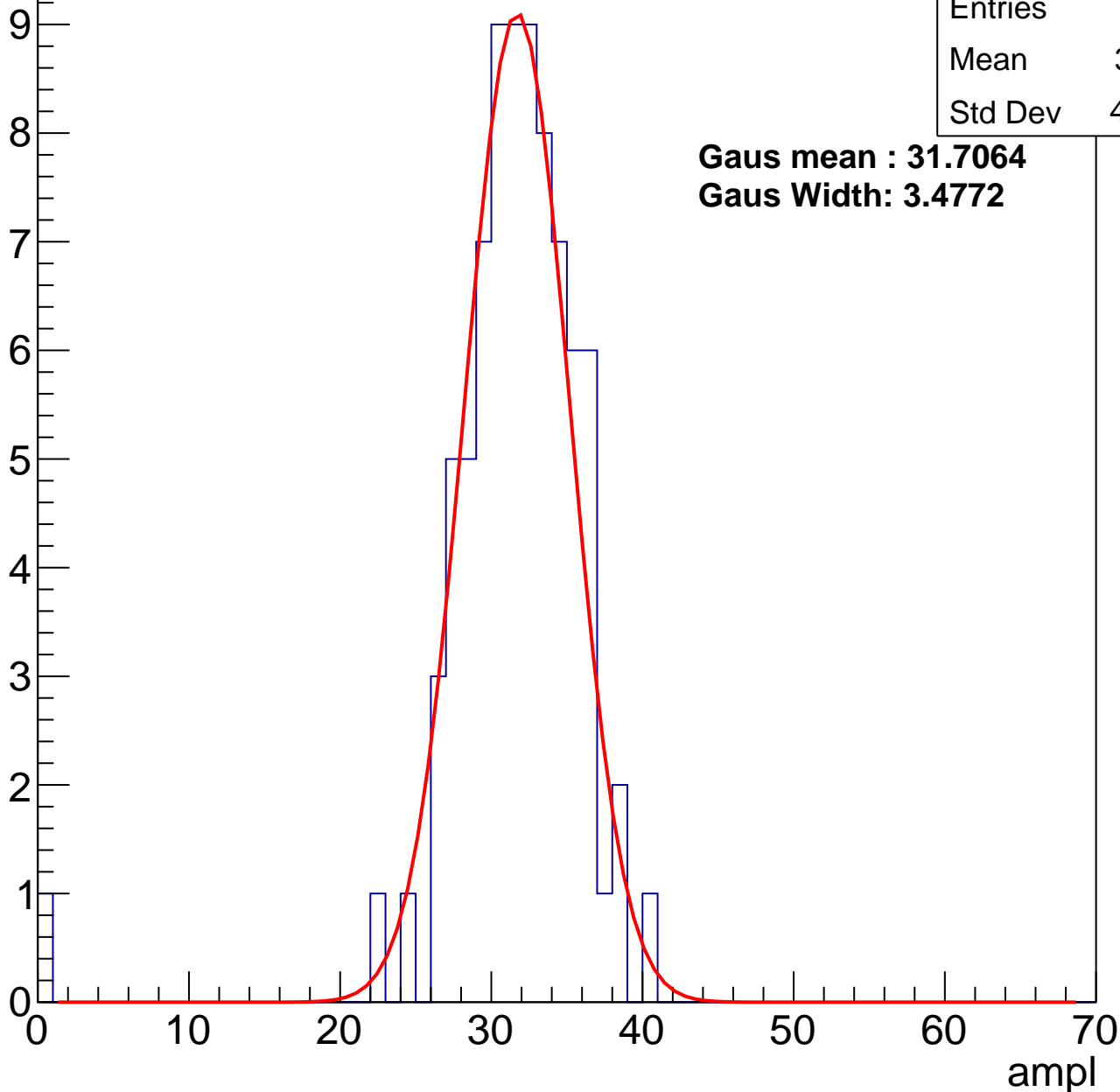
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	31.11
Std Dev	4.833

**Gaus mean : 31.7064**

**Gaus Width: 3.4772**



# B0L001S, U21-ch50, adc1

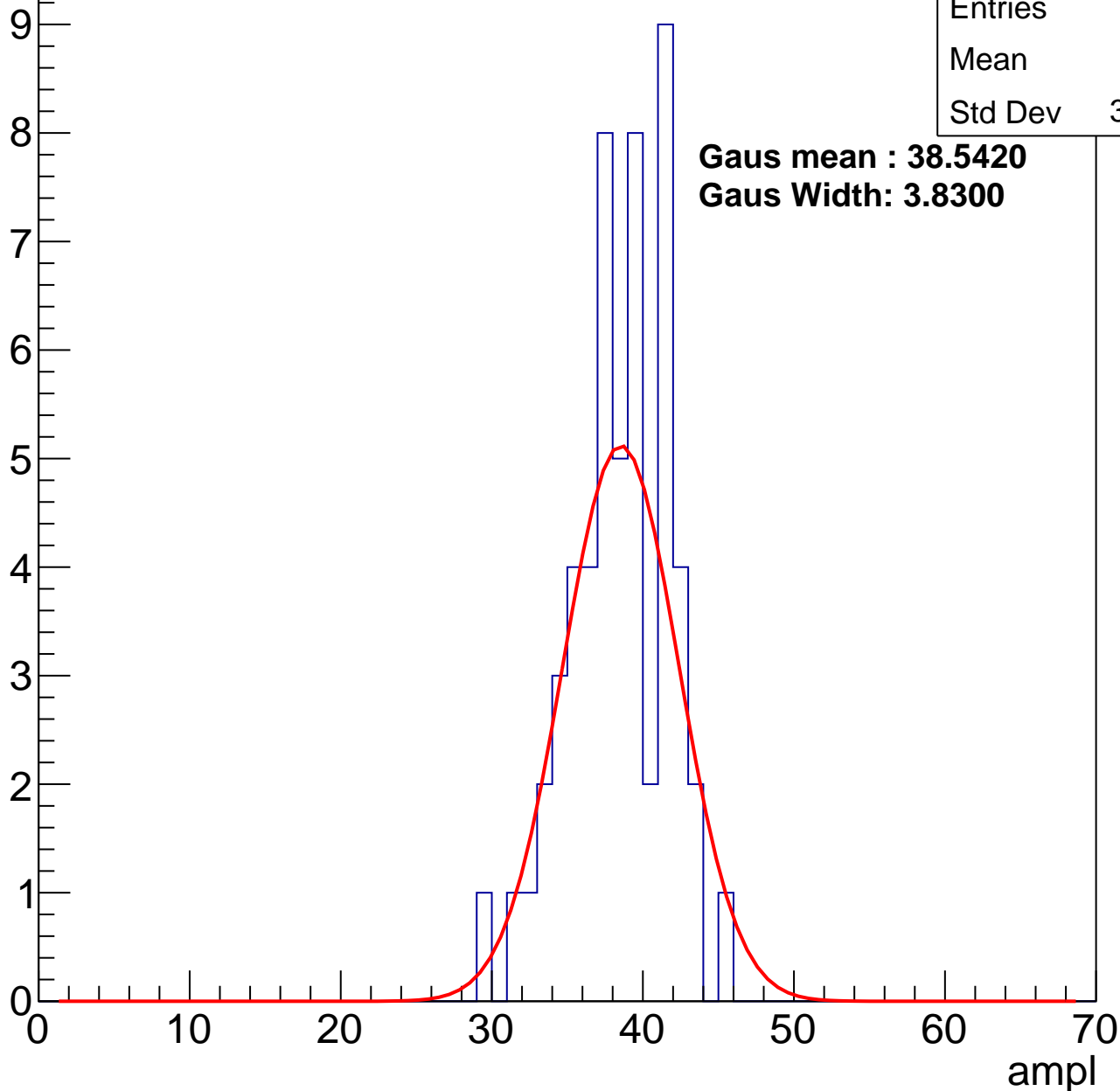
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	38
Std Dev	3.259

**Gaus mean : 38.5420**

**Gaus Width: 3.8300**



# B0L001S, U21-ch50, adc2

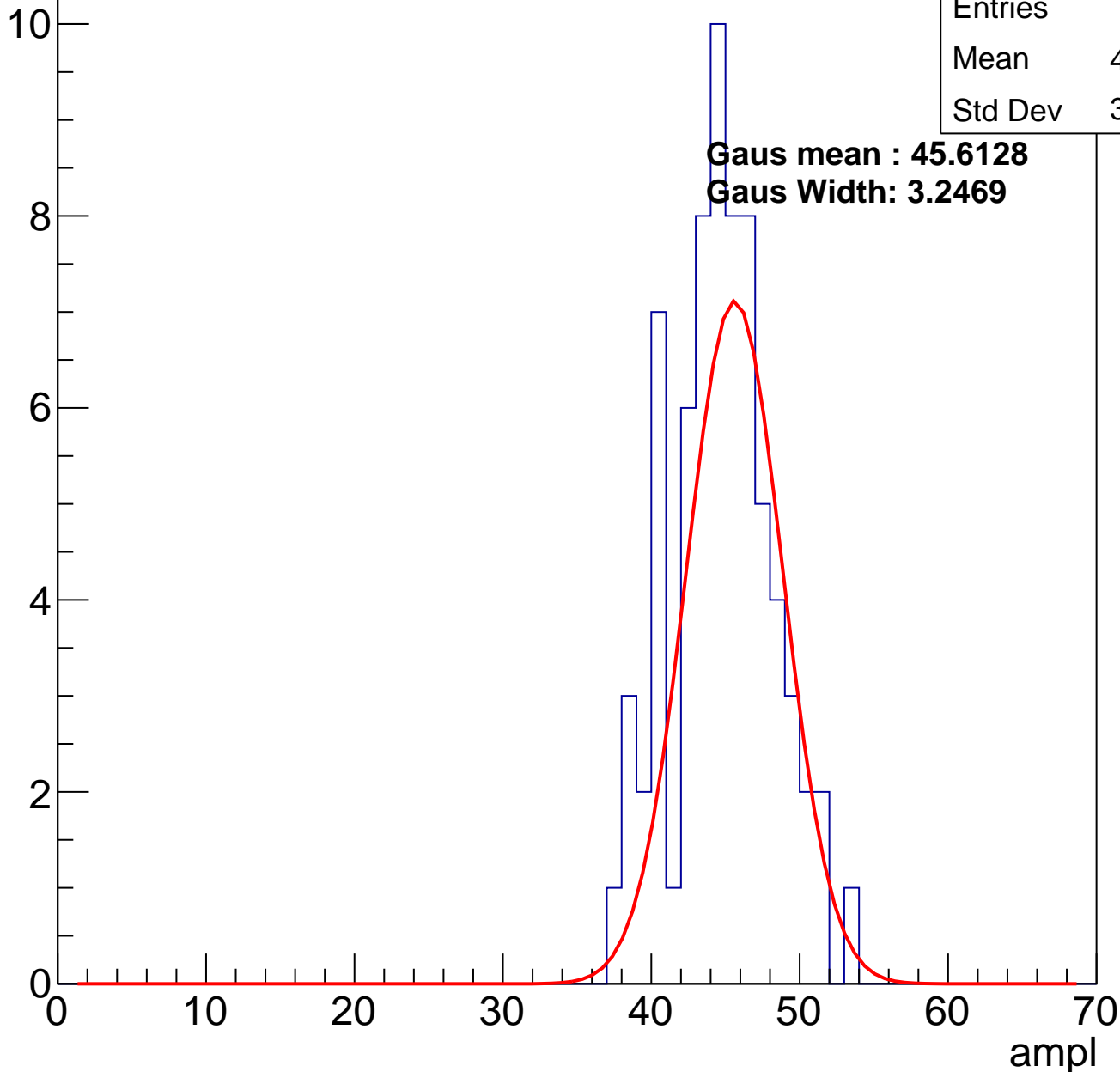
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	71
Mean	44.27
Std Dev	3.419

**Gaus mean : 45.6128**

**Gaus Width: 3.2469**

Entry

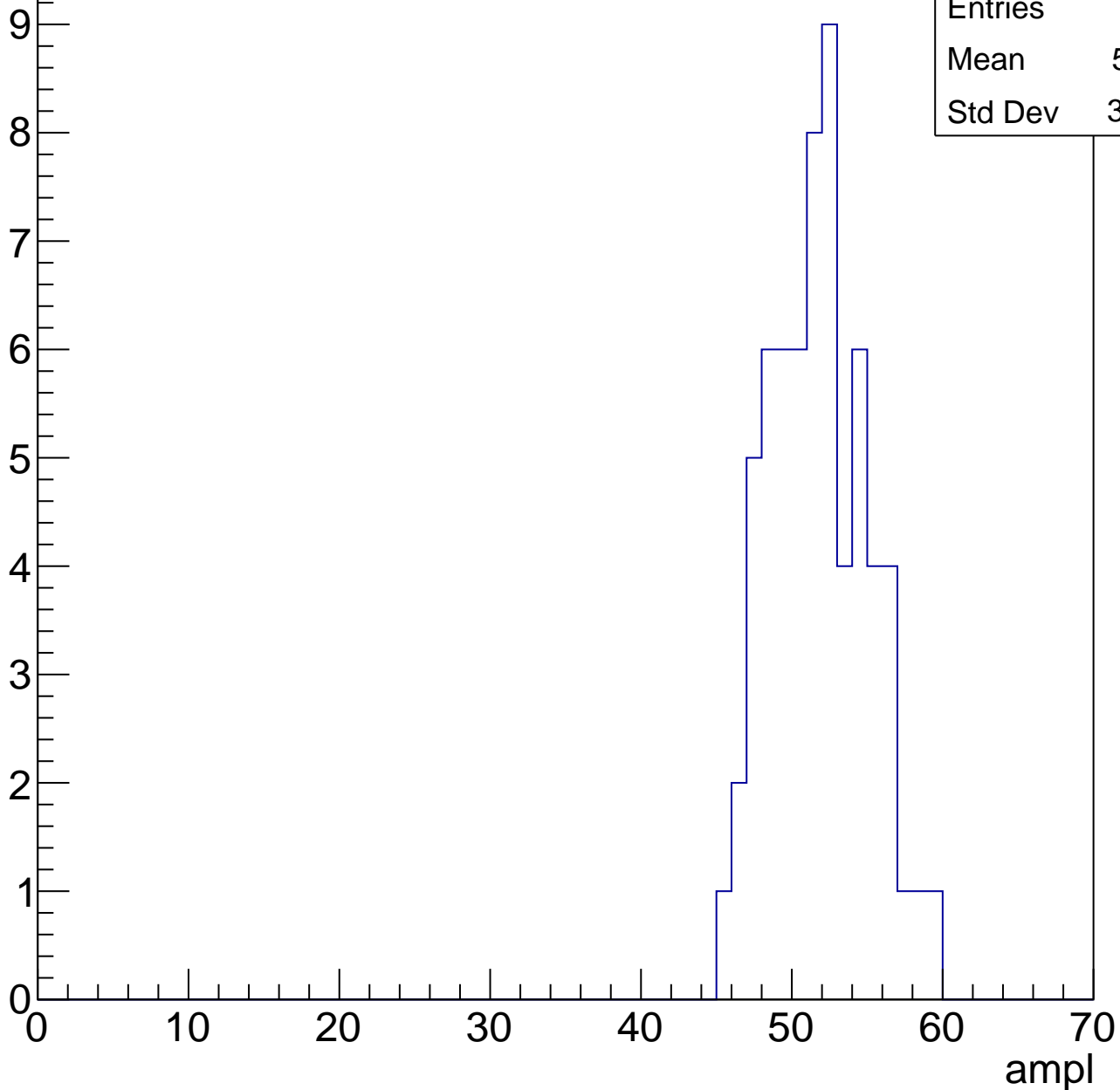


# B0L001S, U21-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	51.31
Std Dev	3.152

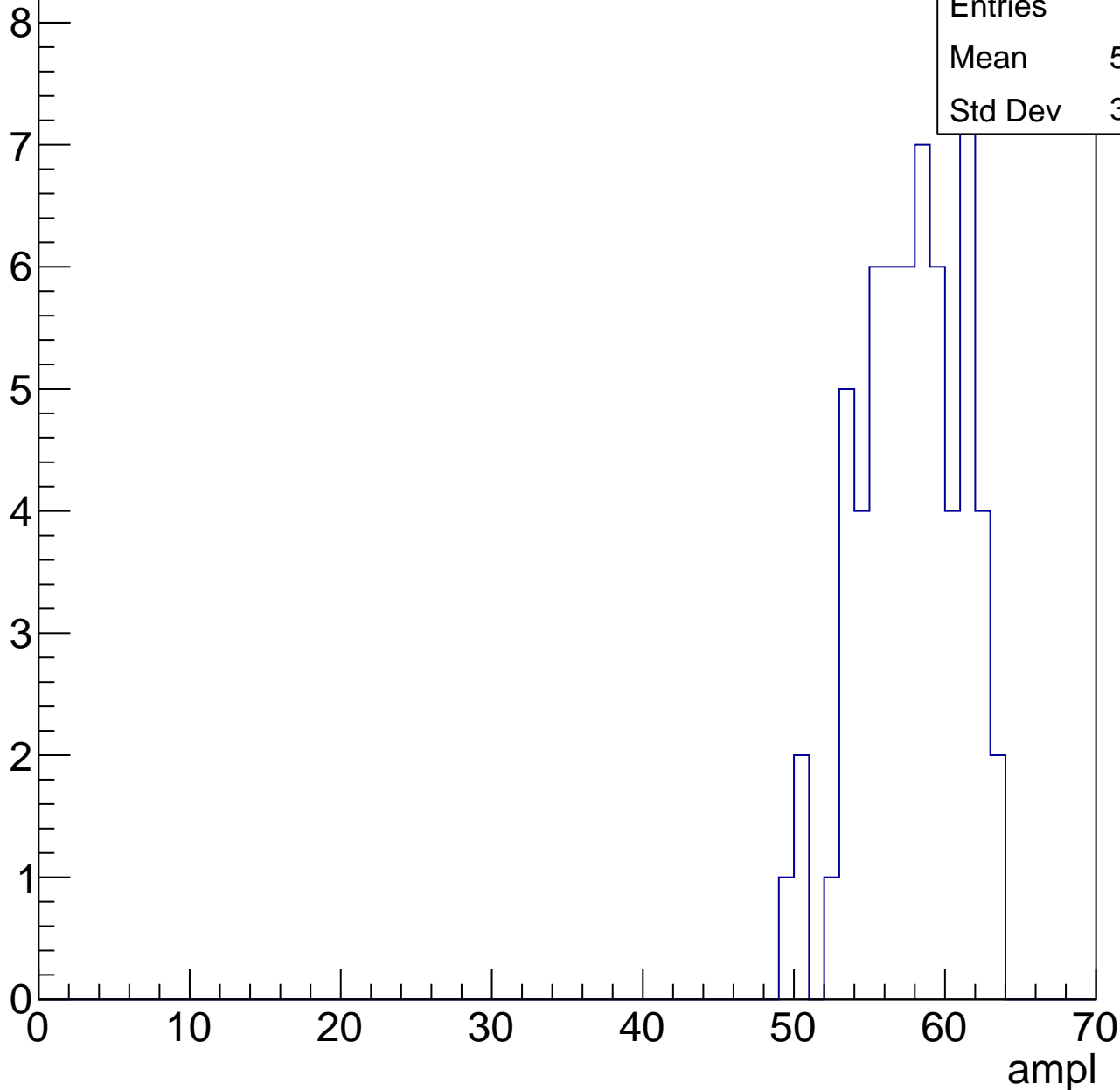


# B0L001S, U21-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	57.29
Std Dev	3.348

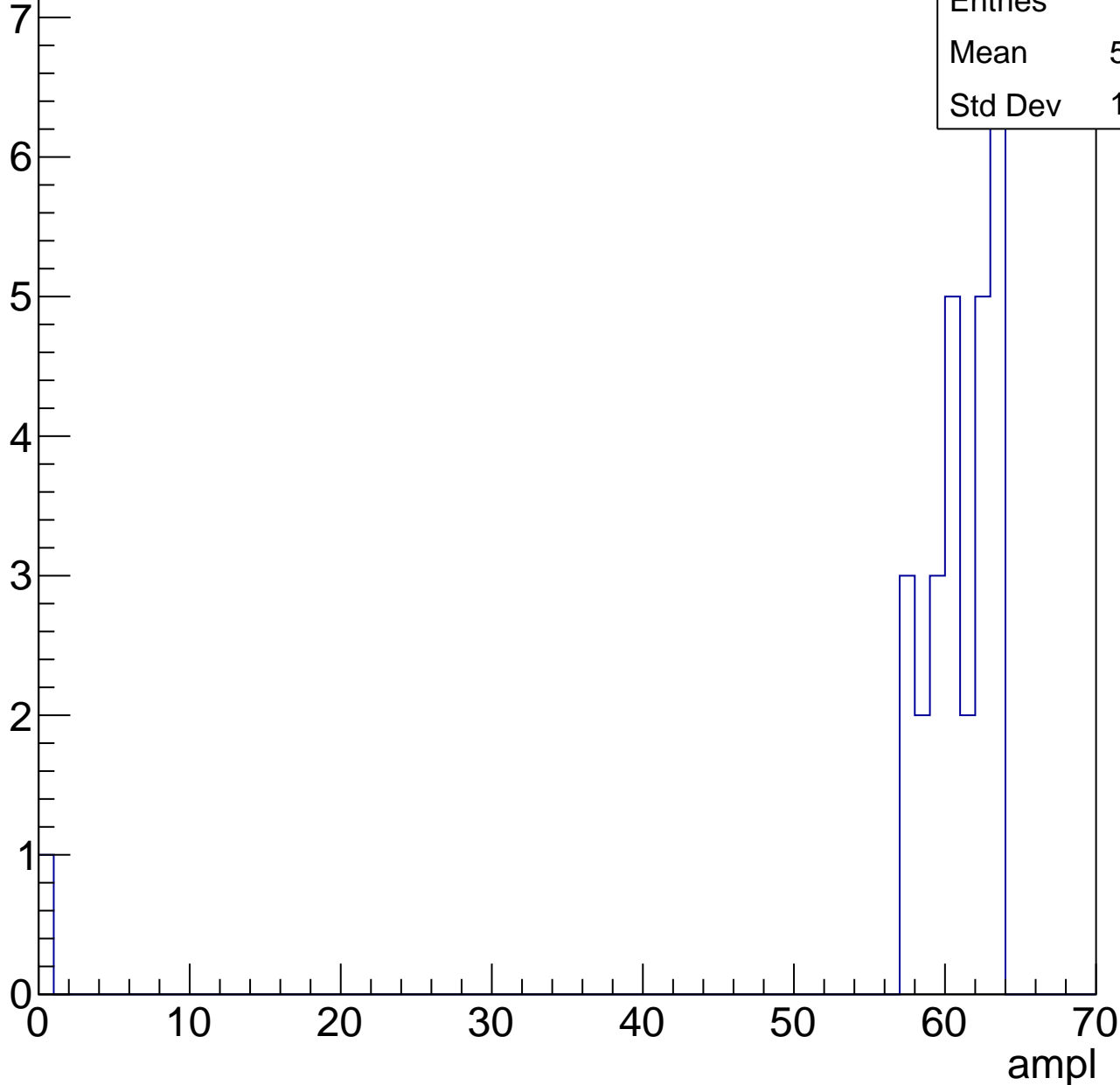


# B0L001S, U21-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	28
Mean	58.46
Std Dev	11.43



# B0L001S, U21-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries	3
Mean	61.67
Std Dev	1.247



# B0L001S, U21-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch51, adc0

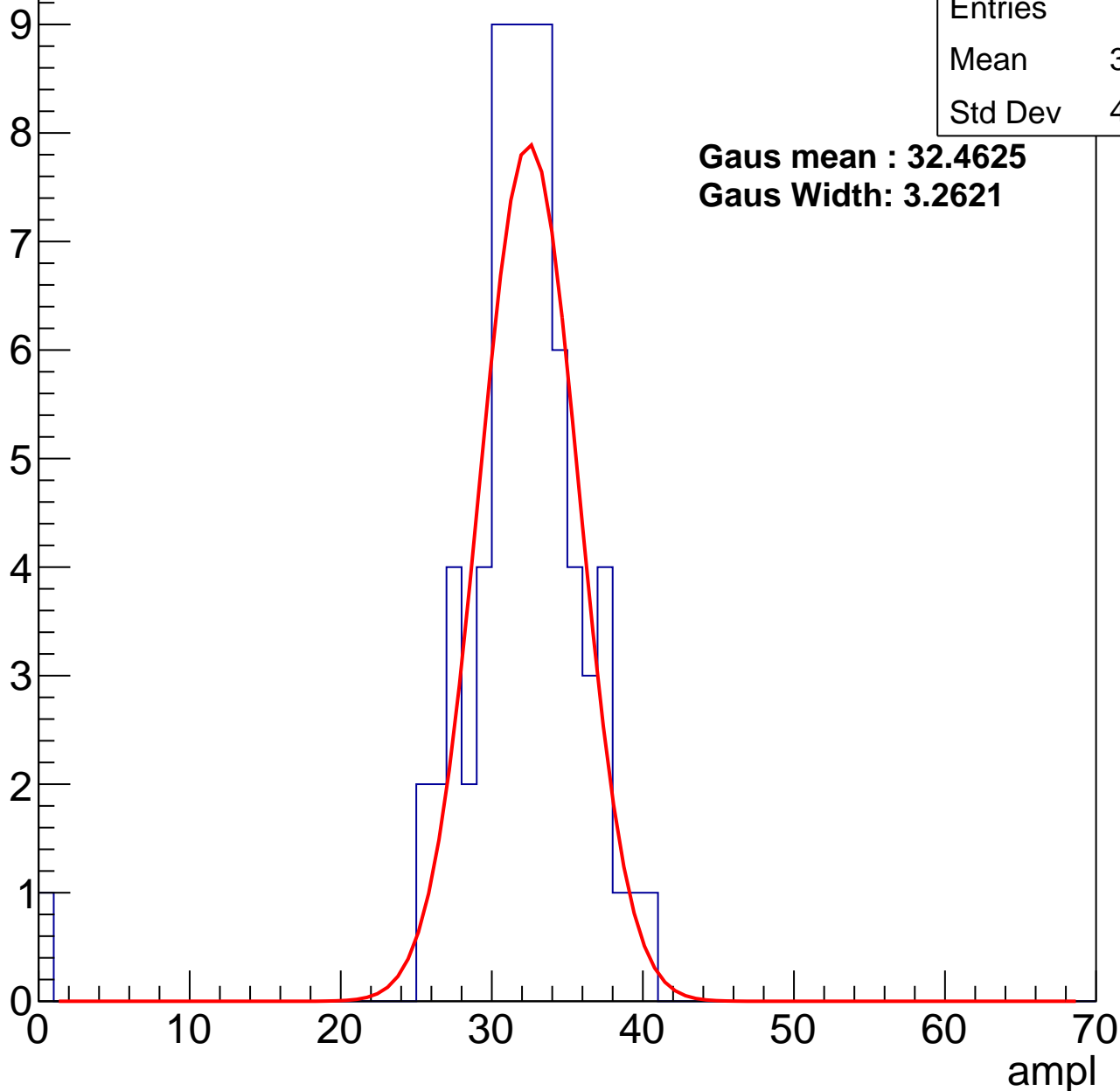
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	31.45
Std Dev	4.967

**Gaus mean : 32.4625**

**Gaus Width: 3.2621**



# B0L001S, U21-ch51, adc1

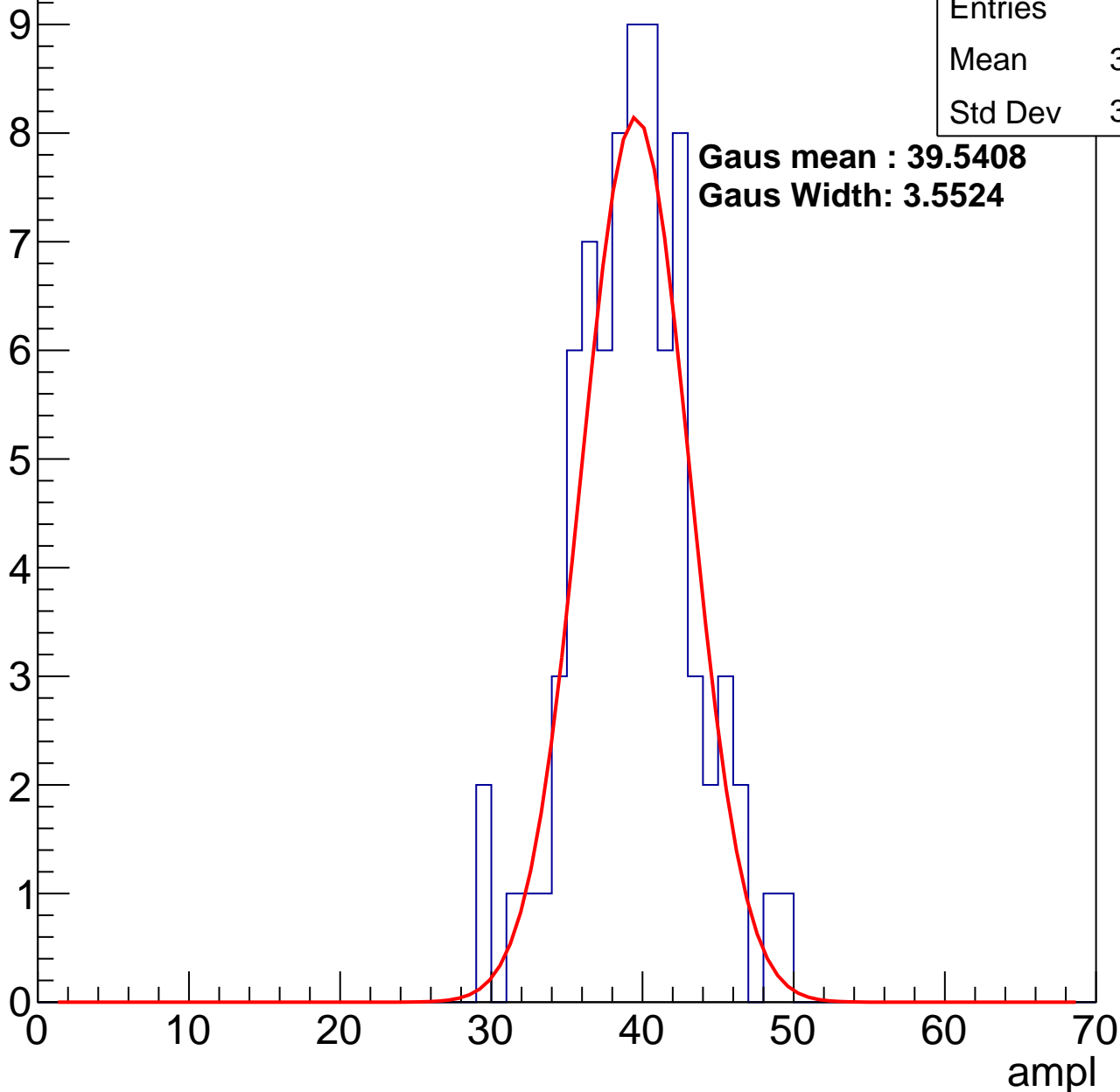
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	38.96
Std Dev	3.905

**Gaus mean : 39.5408**

**Gaus Width: 3.5524**



# B0L001S, U21-ch51, adc2

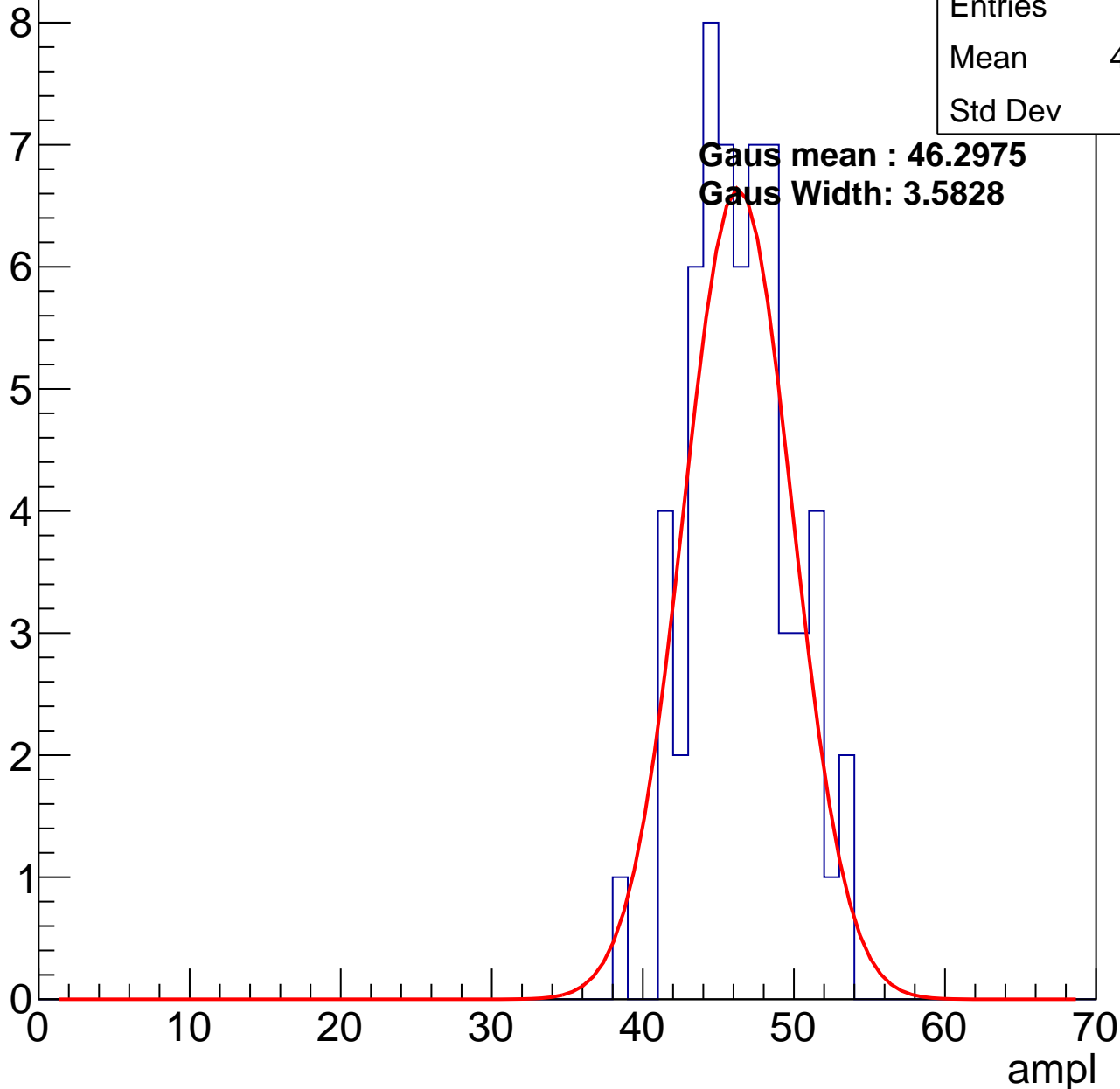
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	46.08
Std Dev	3.22

Gaus mean : 46.2975

Gaus Width: 3.5828

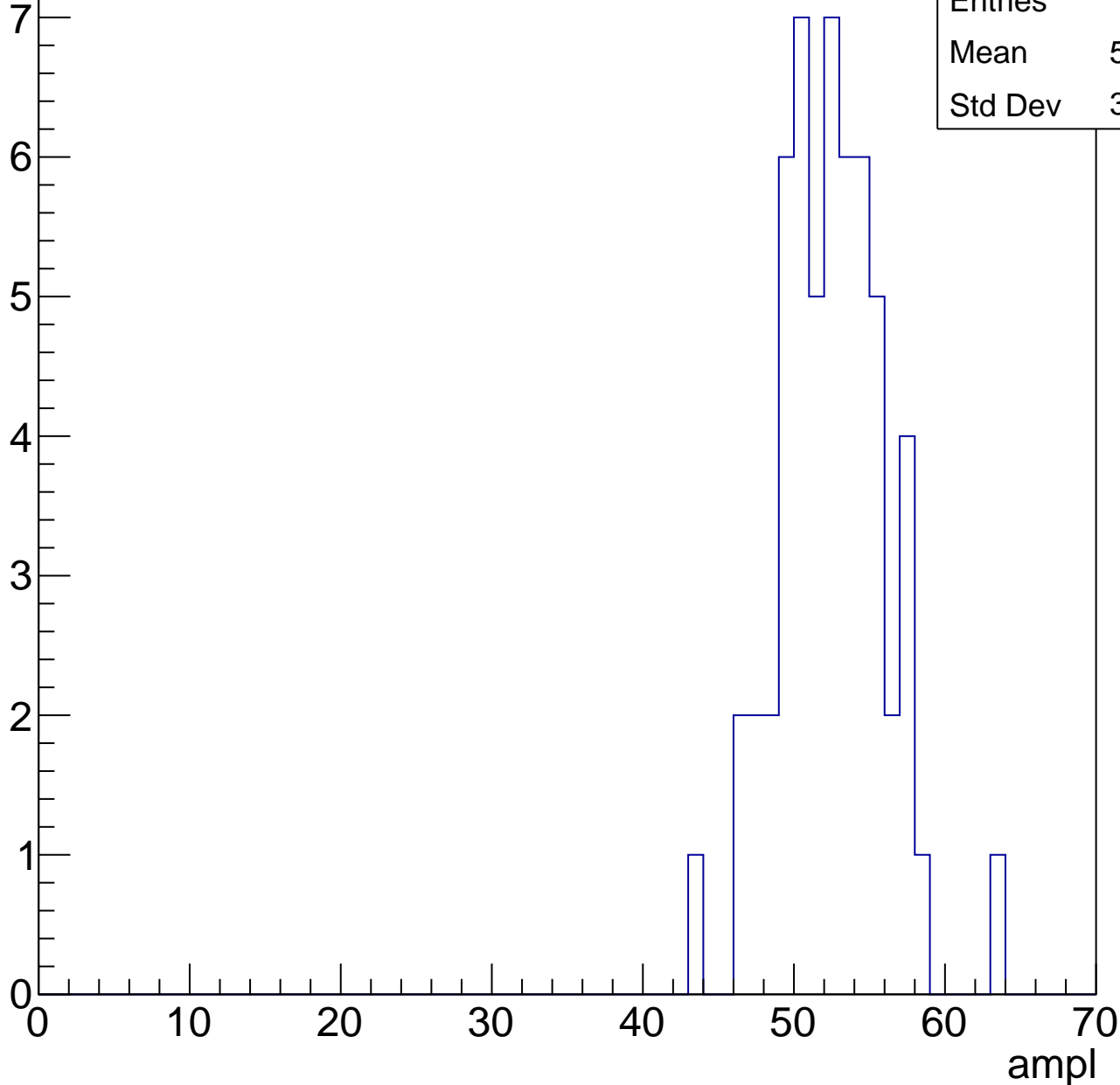


# B0L001S, U21-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	52.04
Std Dev	3.469

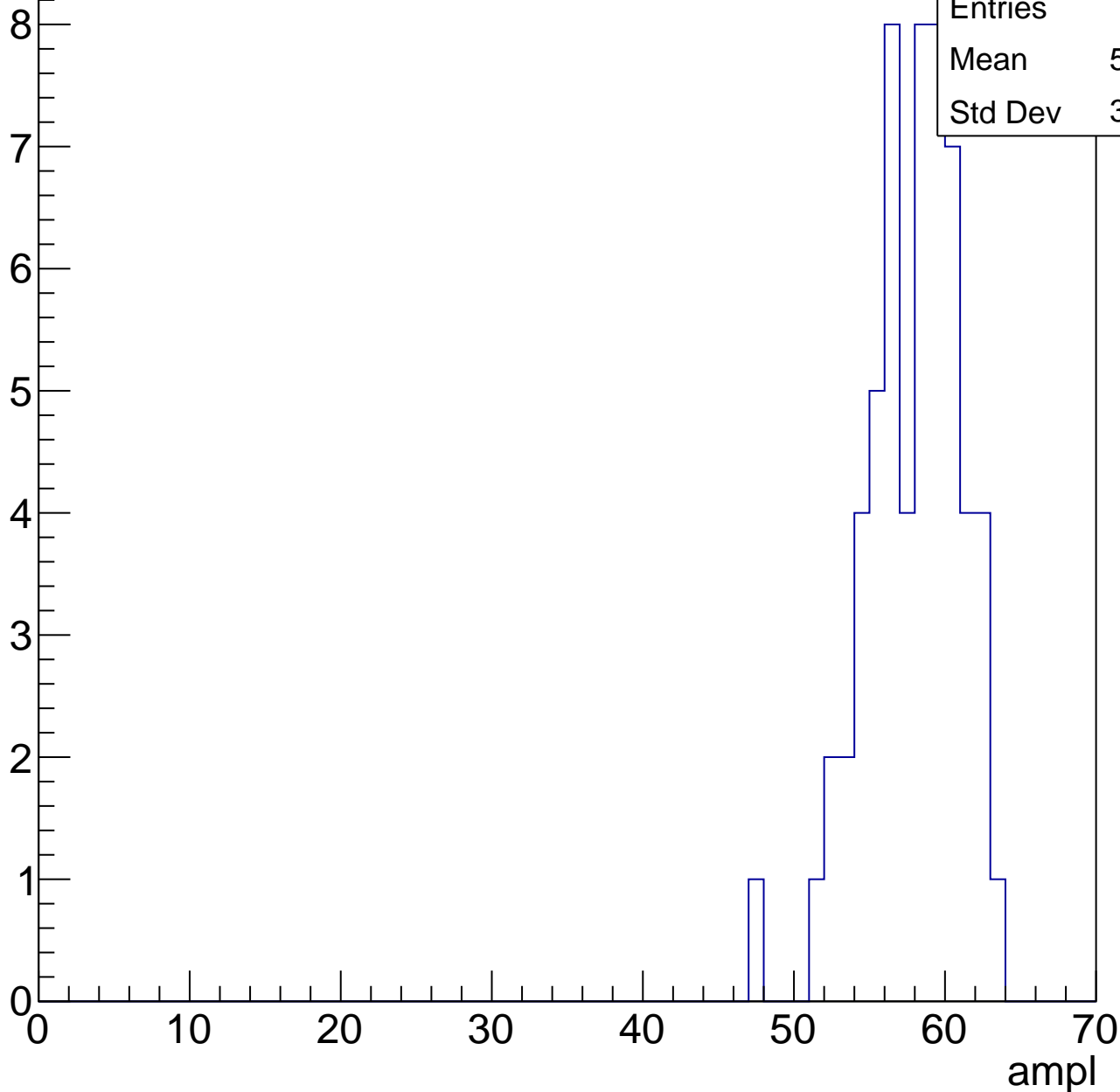


# B0L001S, U21-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	57.39
Std Dev	3.125

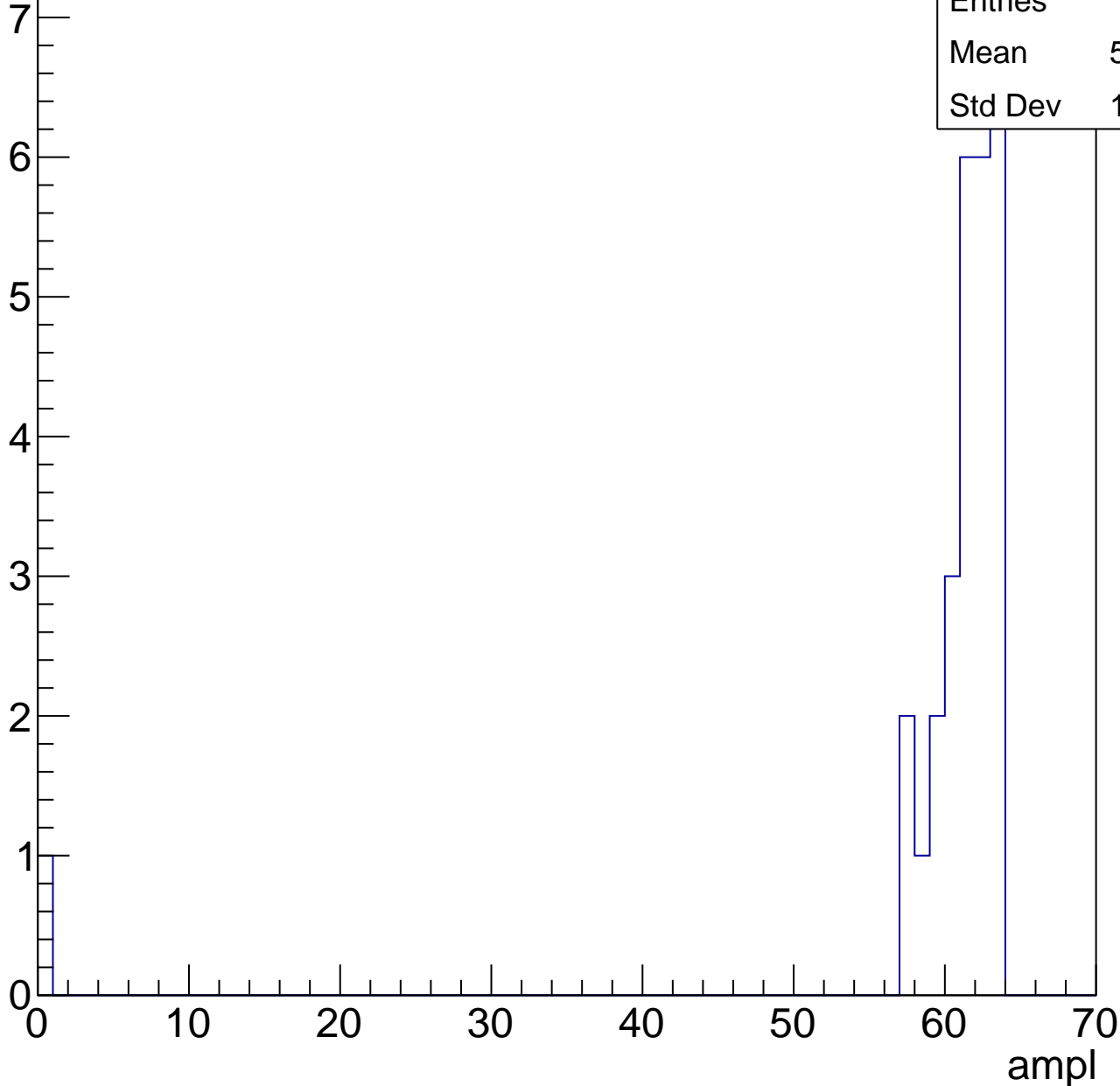


# B0L001S, U21-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	28
Mean	58.89
Std Dev	11.47



# B0L001S, U21-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch52, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	65
Mean	30.77
Std Dev	3.529

**Gaus mean : 30.9635**

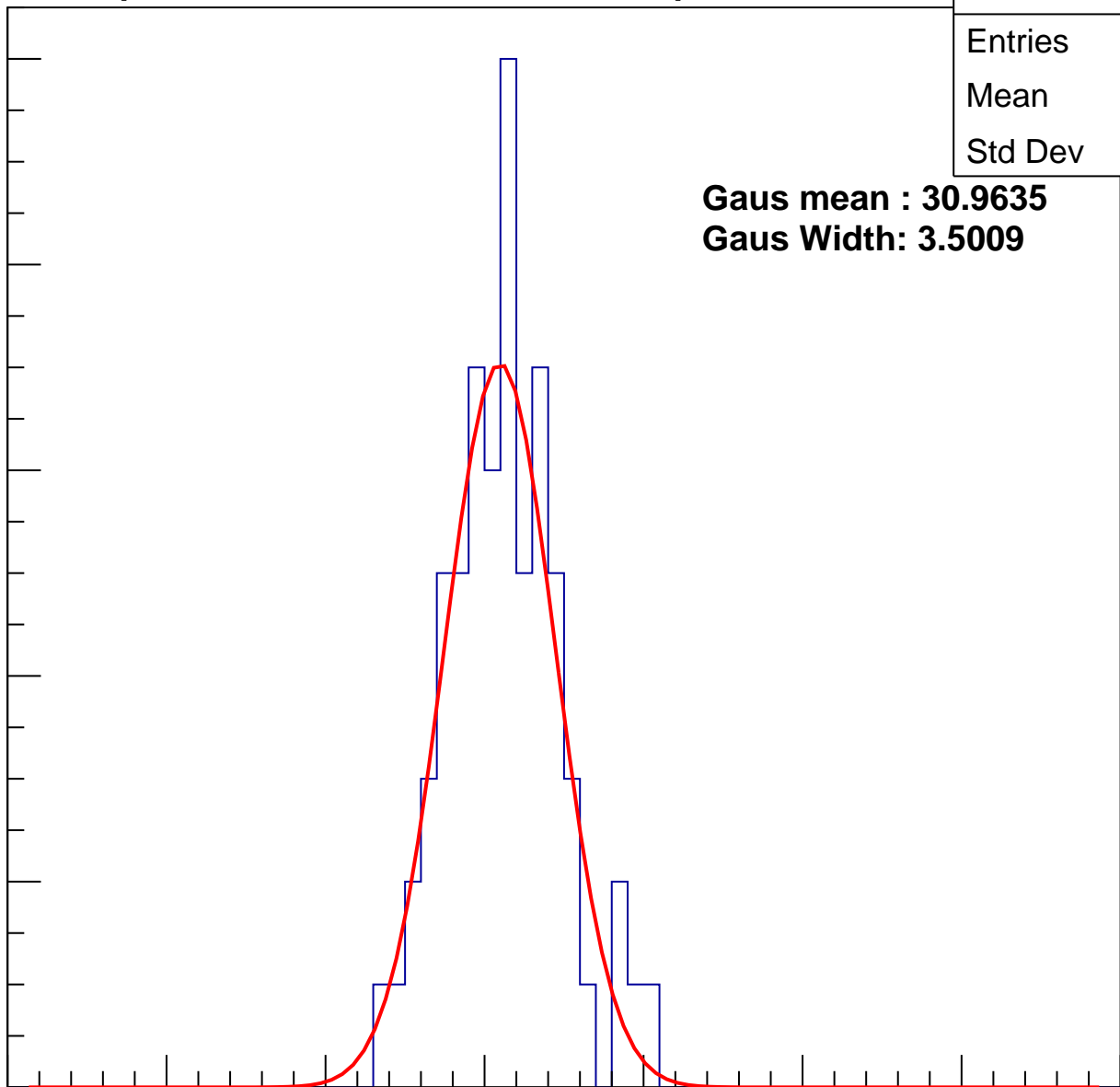
**Gaus Width: 3.5009**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



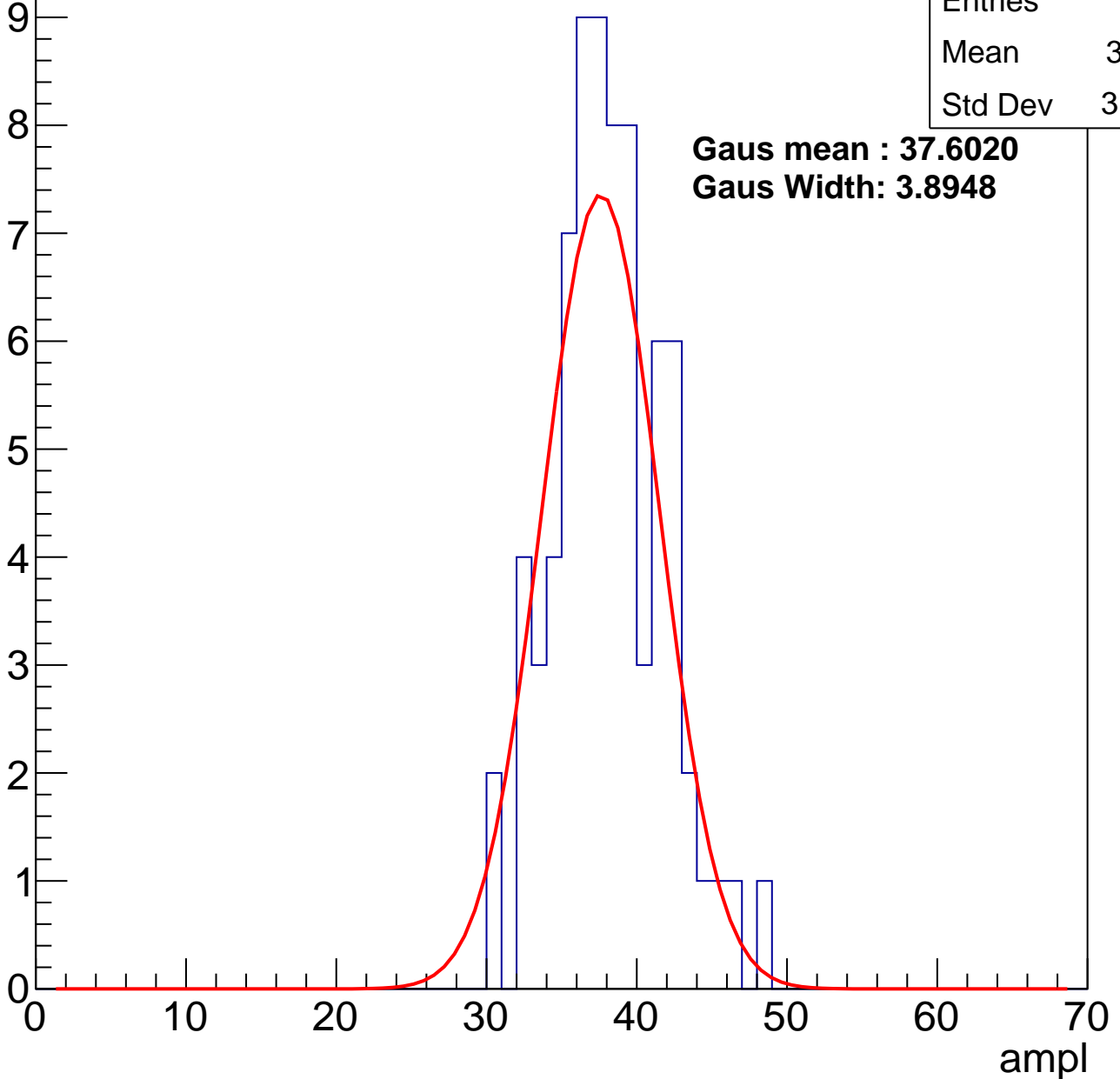
# B0L001S, U21-ch52, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	37.71
Std Dev	3.618

**Gaus mean : 37.6020**  
**Gaus Width: 3.8948**

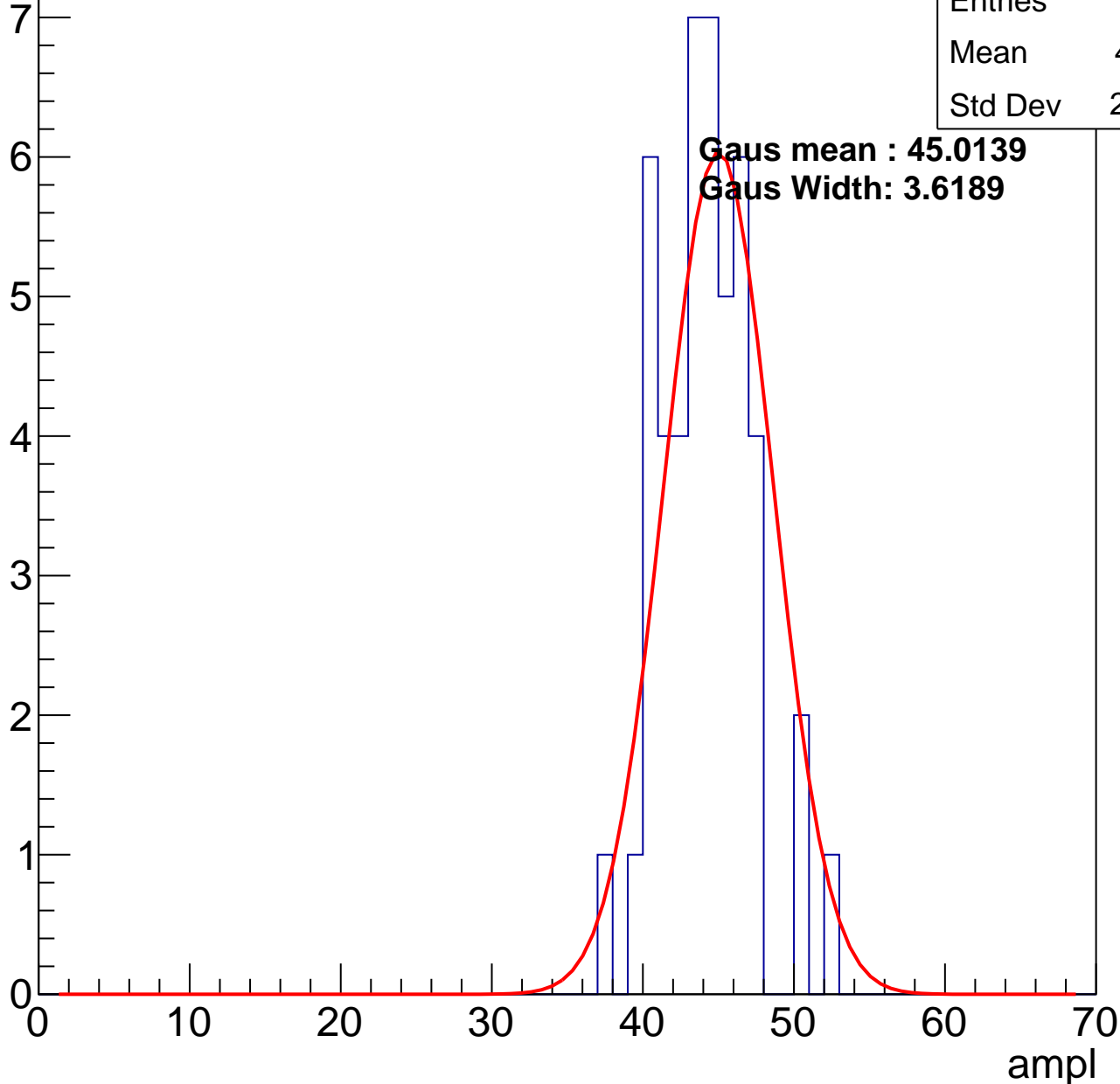


# B0L001S, U21-ch52, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	43.71
Std Dev	2.979

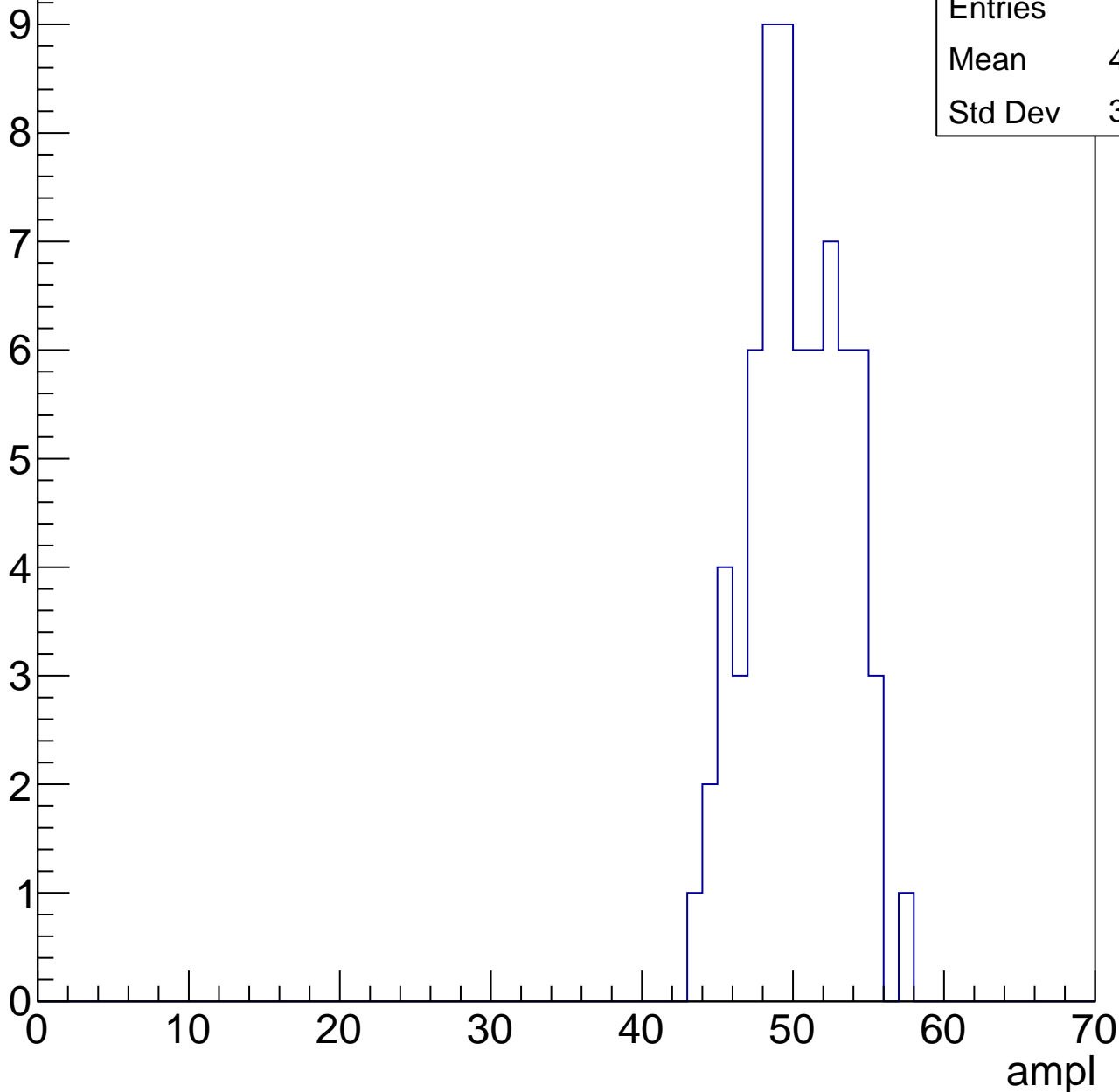


# B0L001S, U21-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	49.83
Std Dev	3.125

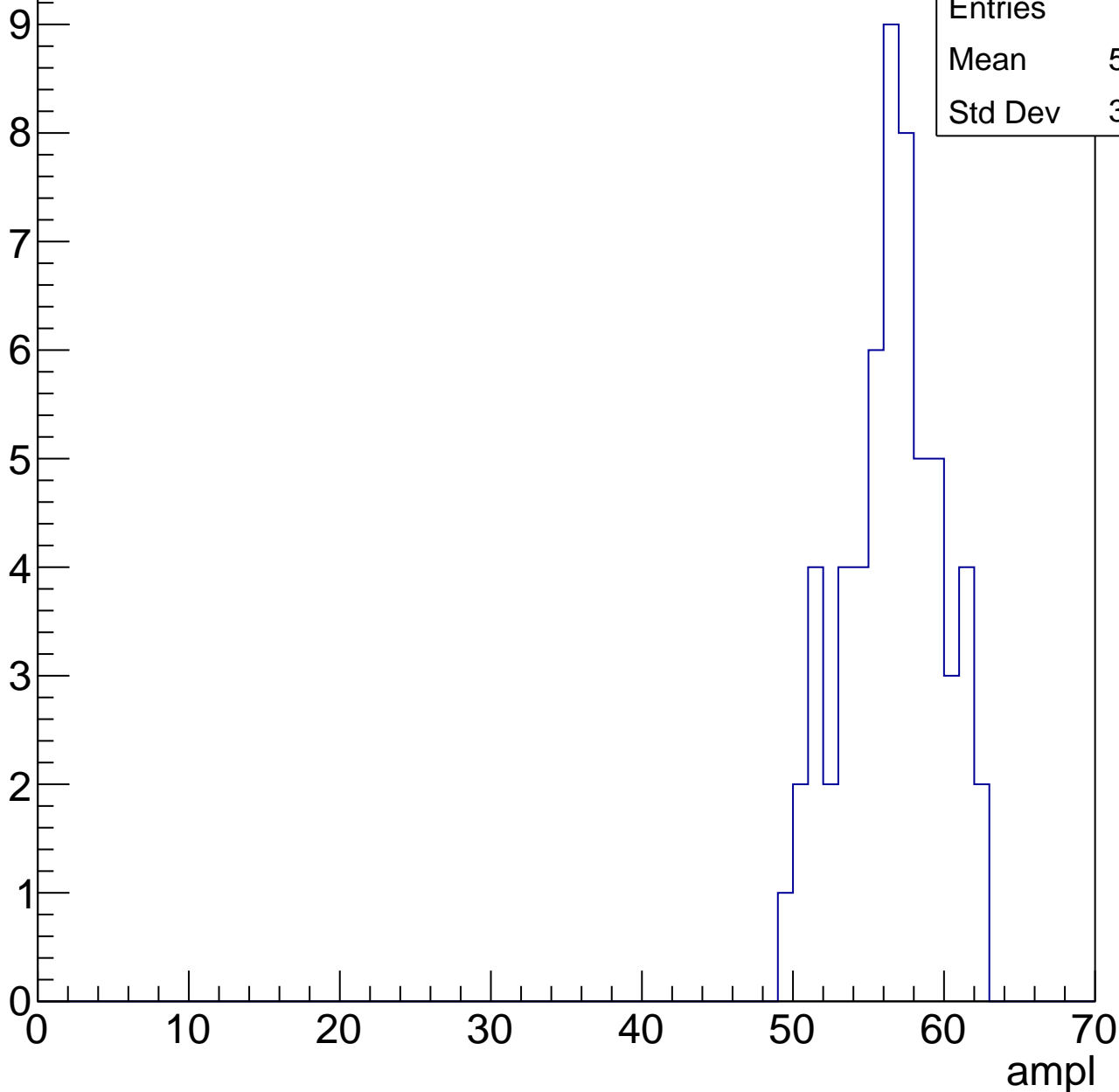


# B0L001S, U21-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	56.07
Std Dev	3.199



# B0L001S, U21-ch52, adc5

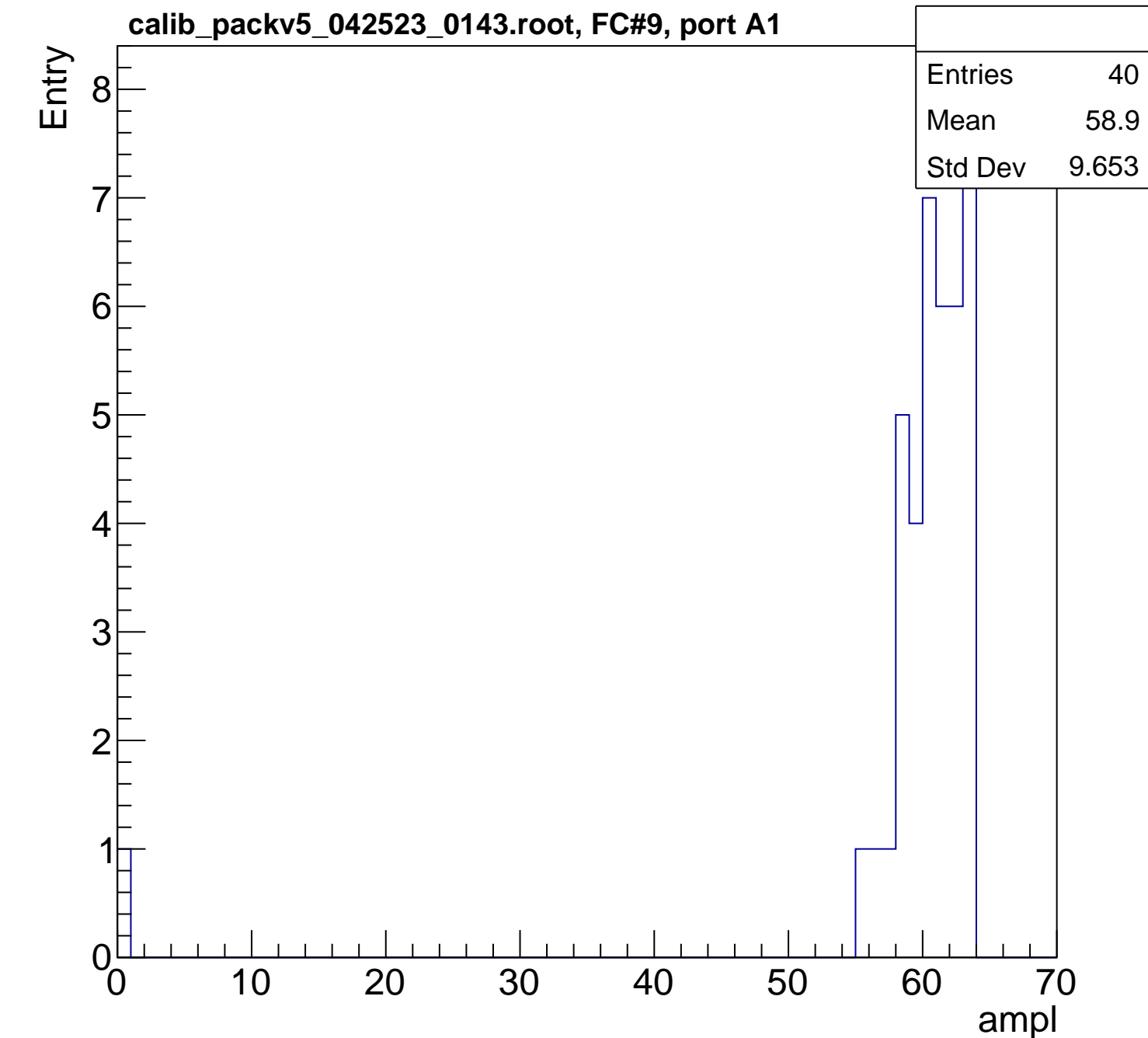
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	40
Mean	58.9
Std Dev	9.653

ampl



# B0L001S, U21-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch53, adc0

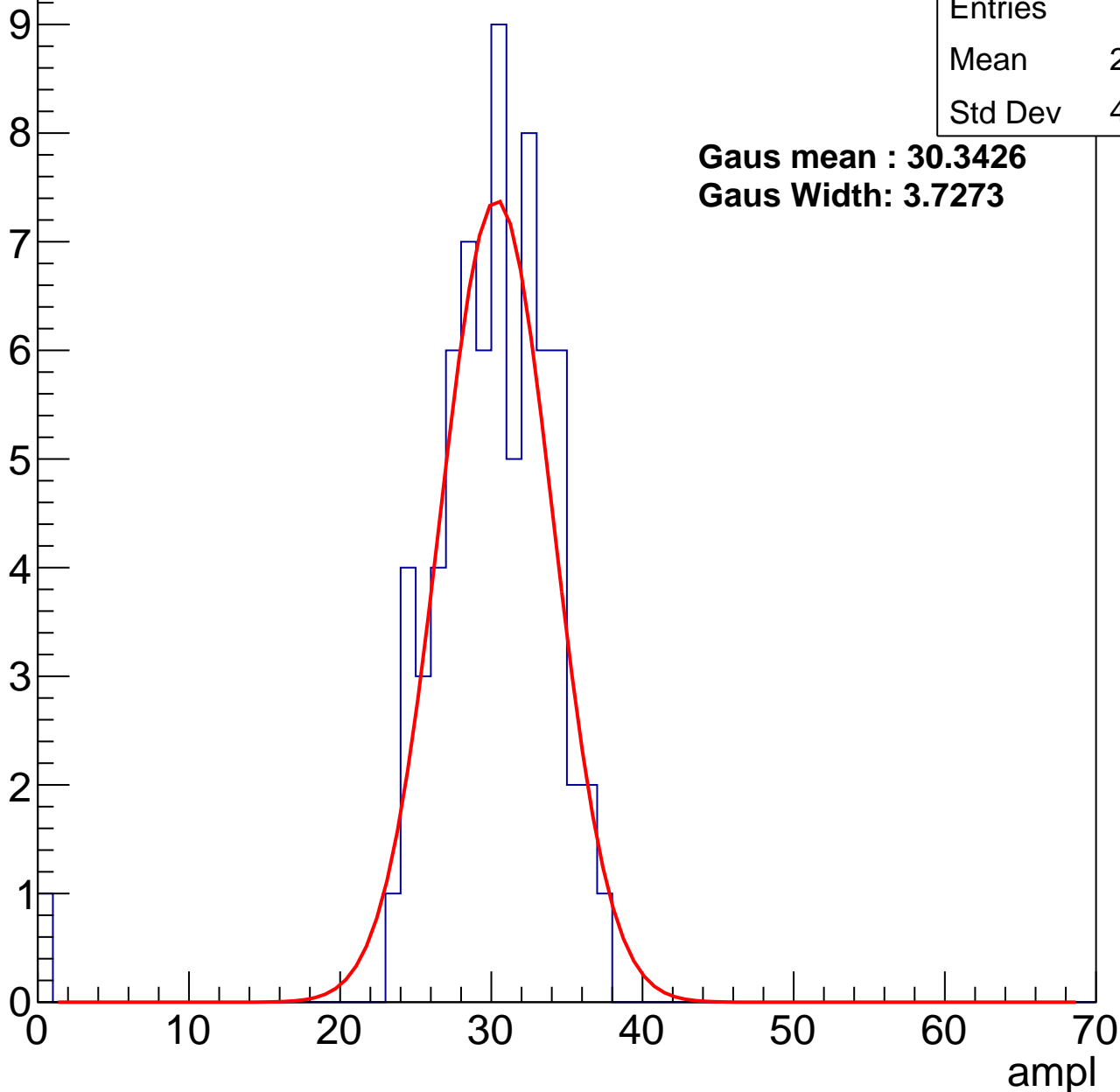
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	29.46
Std Dev	4.832

**Gaus mean : 30.3426**

**Gaus Width: 3.7273**



# B0L001S, U21-ch53, adc1

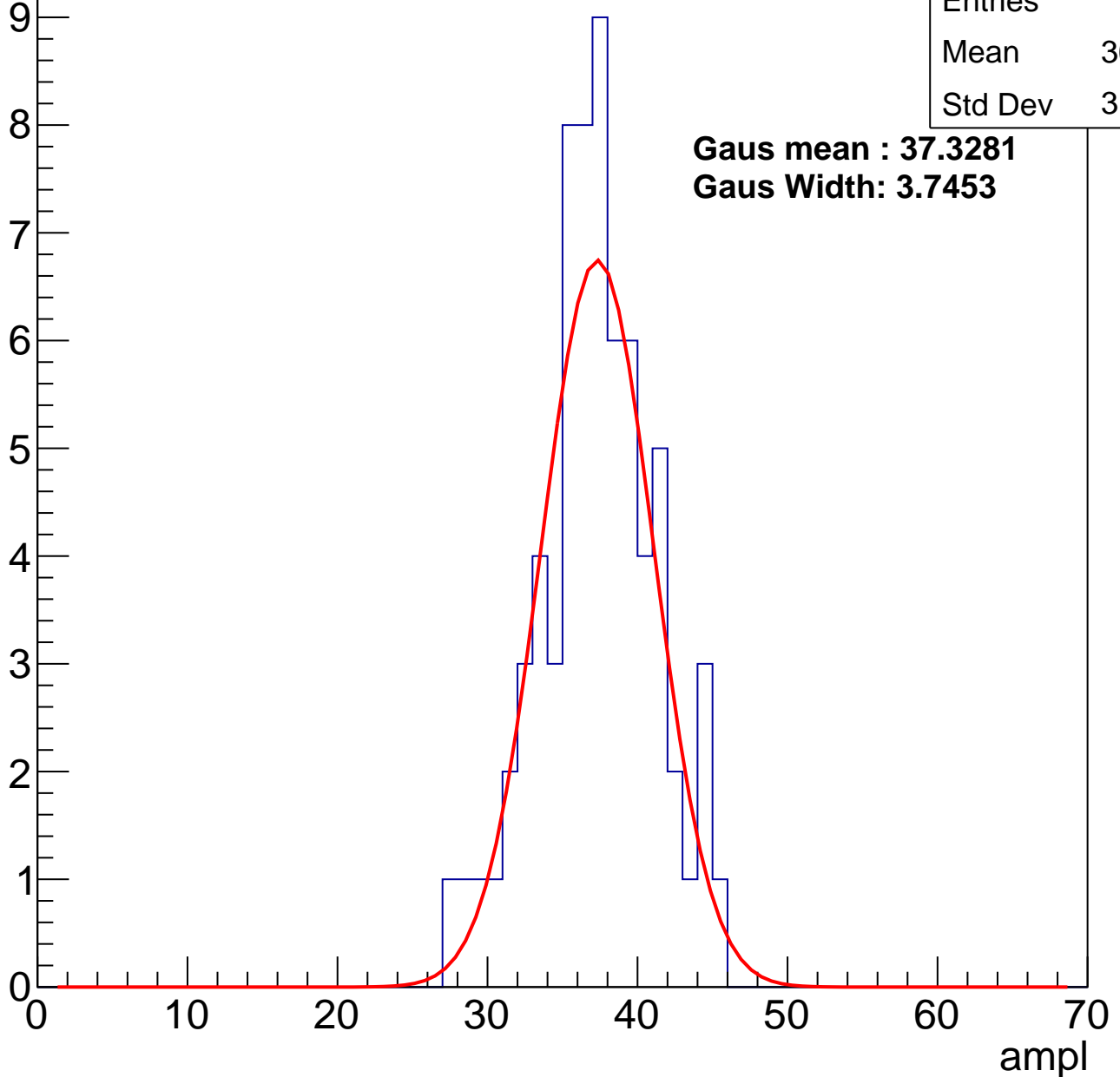
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	36.78
Std Dev	3.829

**Gaus mean : 37.3281**

**Gaus Width: 3.7453**



# B0L001S, U21-ch53, adc2

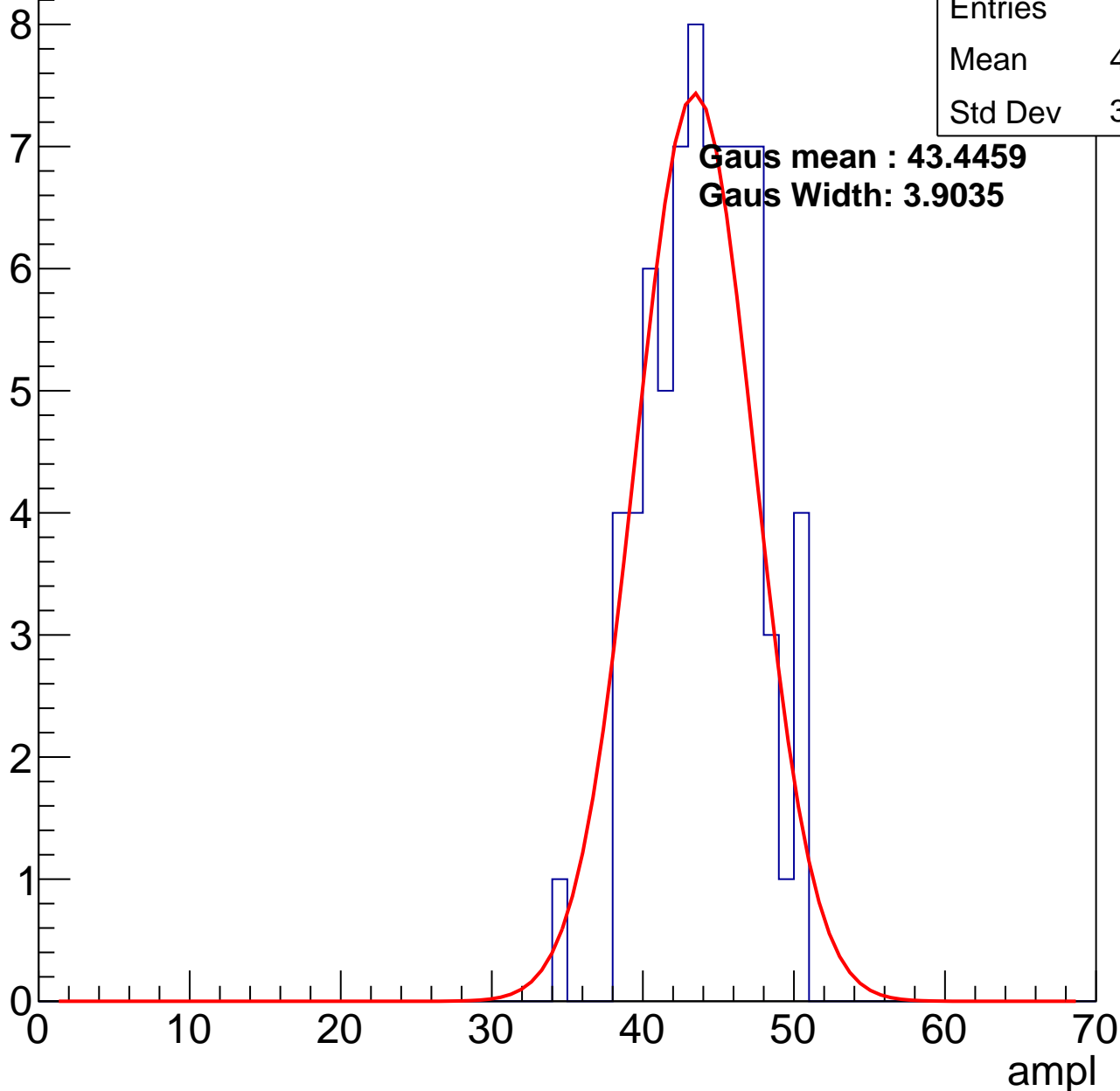
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	43.55
Std Dev	3.402

**Gaus mean : 43.4459**

**Gaus Width: 3.9035**

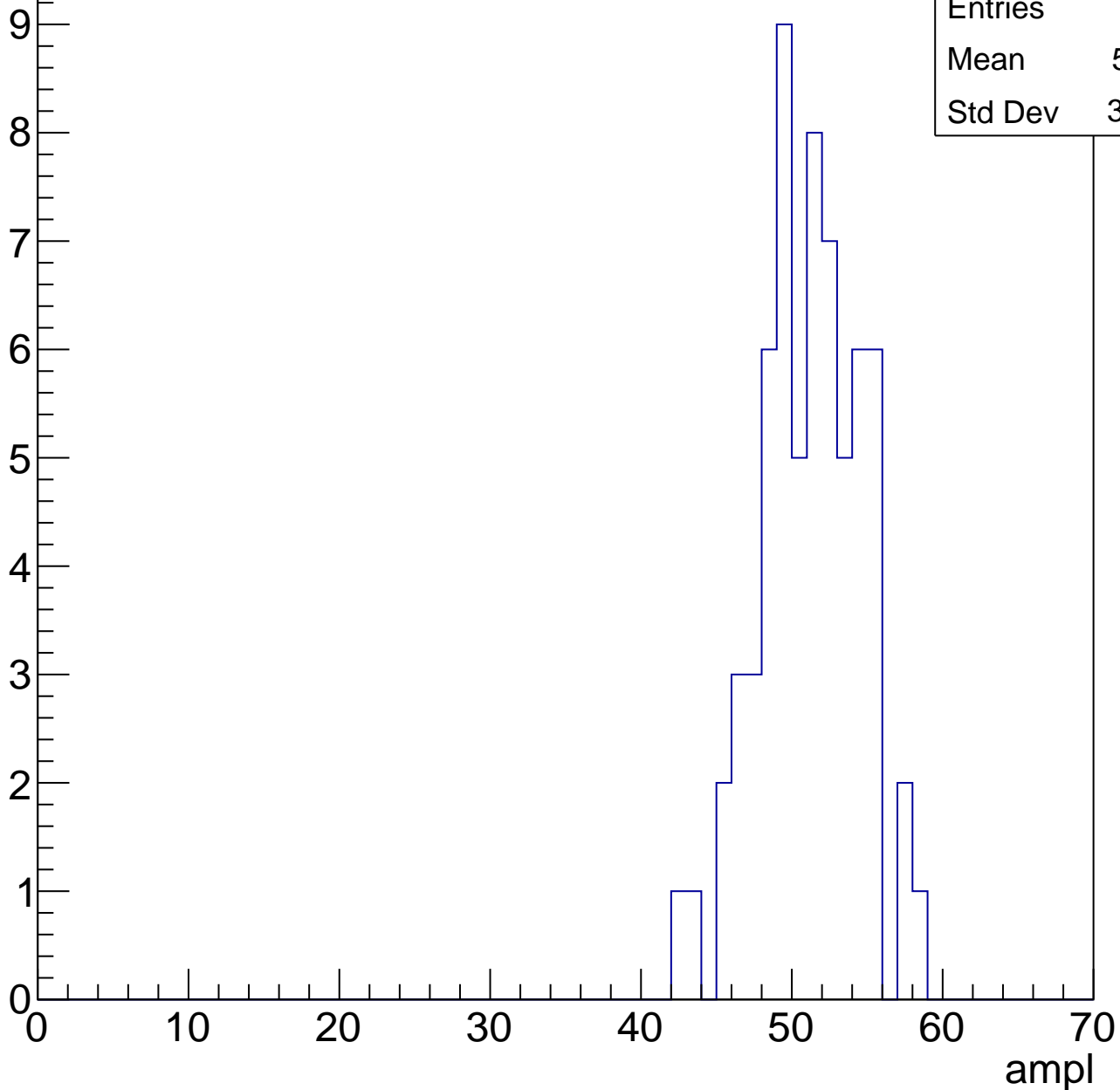


# B0L001S, U21-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	50.71
Std Dev	3.345

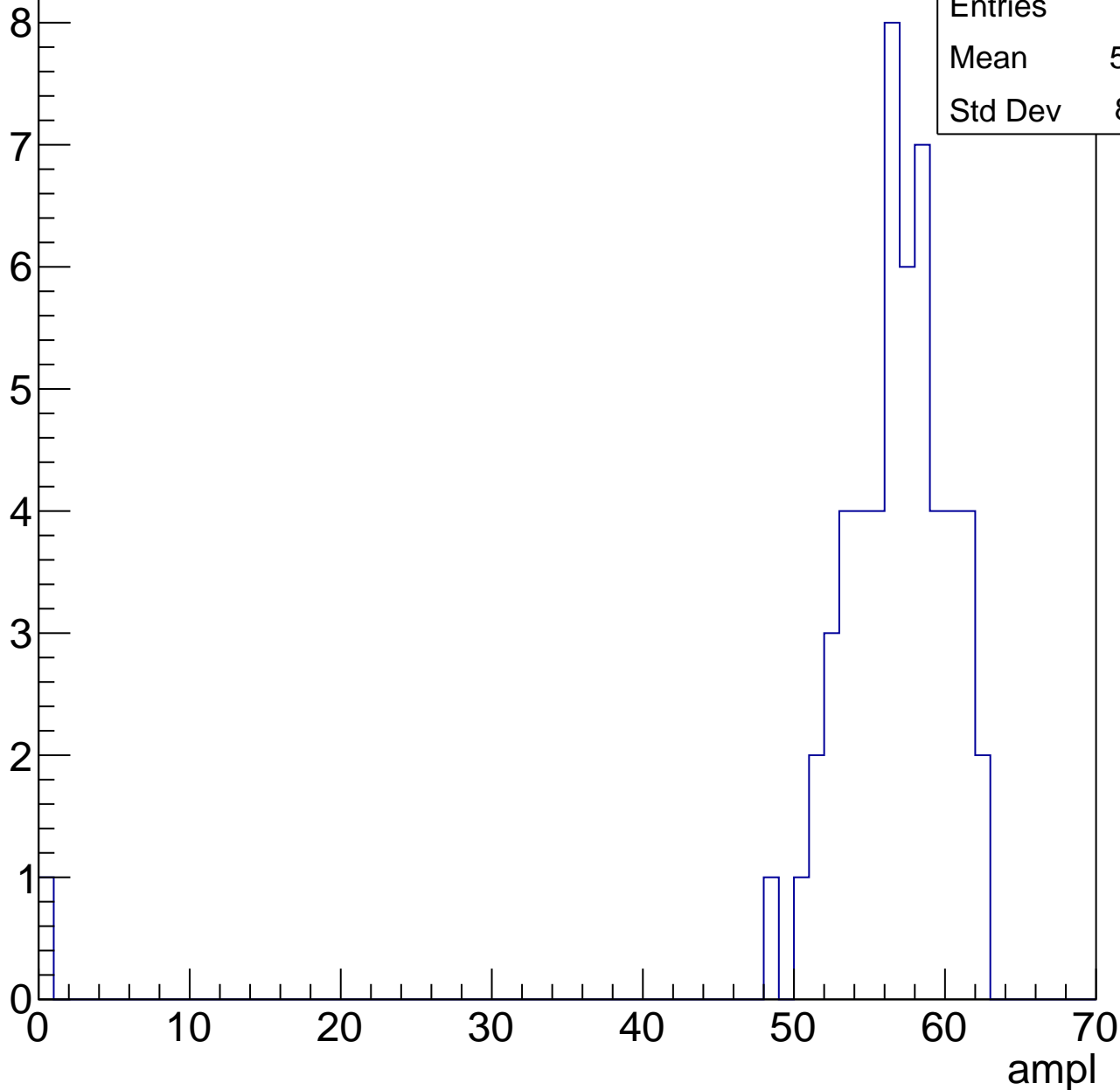


# B0L001S, U21-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	55.35
Std Dev	8.171

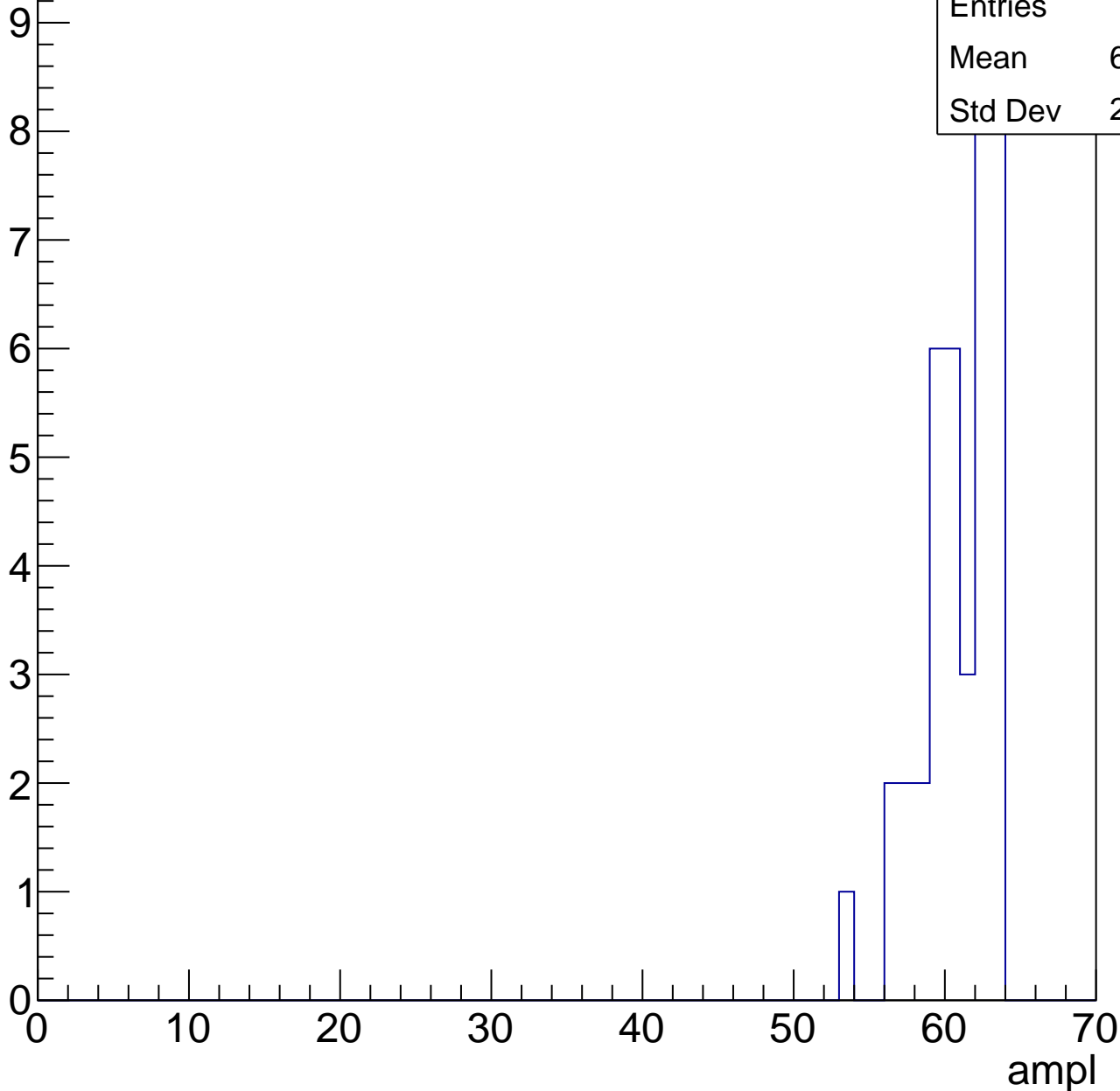


# B0L001S, U21-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

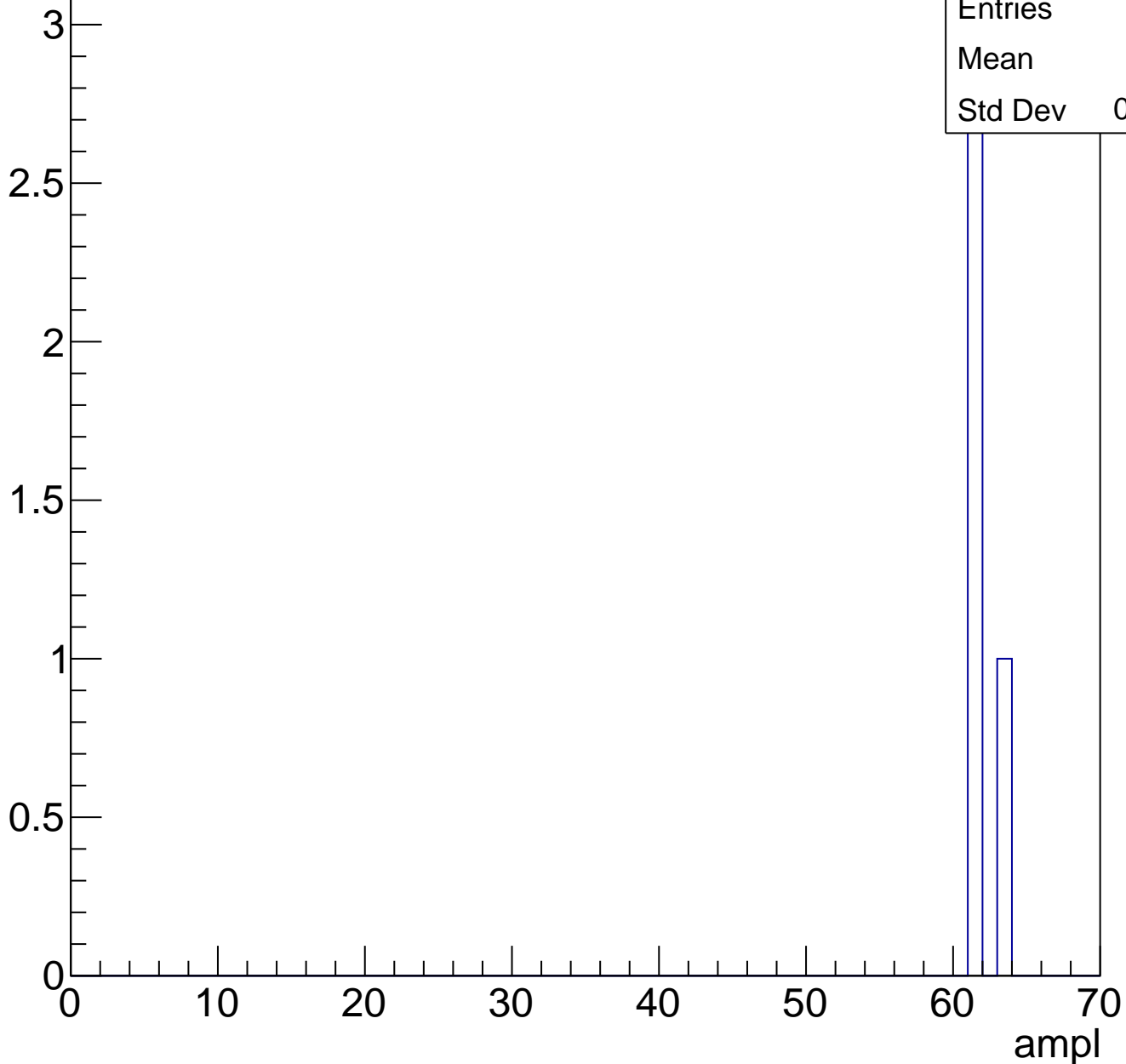
Entries	39
Mean	60.38
Std Dev	2.392



# B0L001S, U21-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

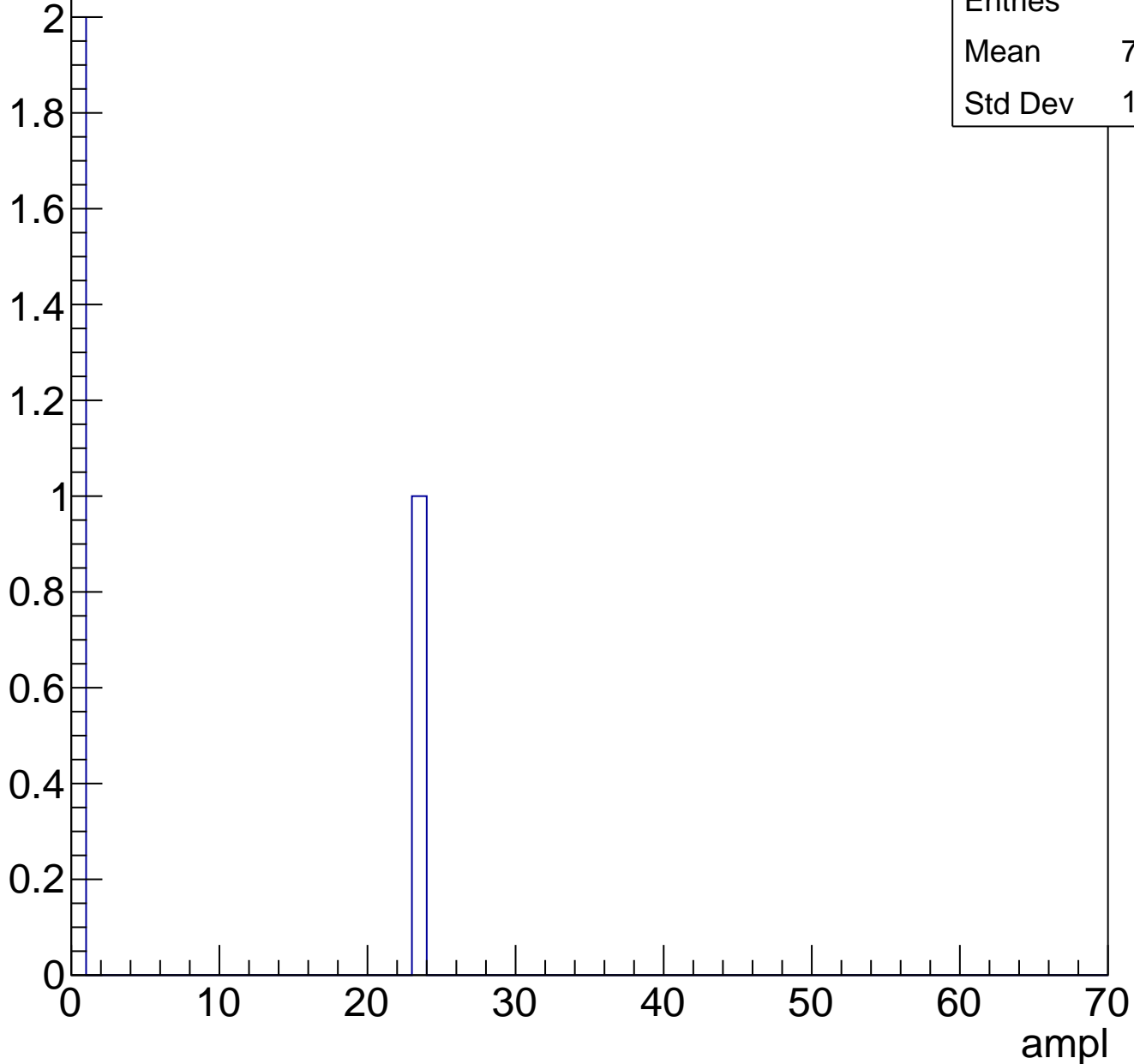




# B0L001S, U21-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	7.667
Std Dev	10.84

# B0L001S, U21-ch54, adc0

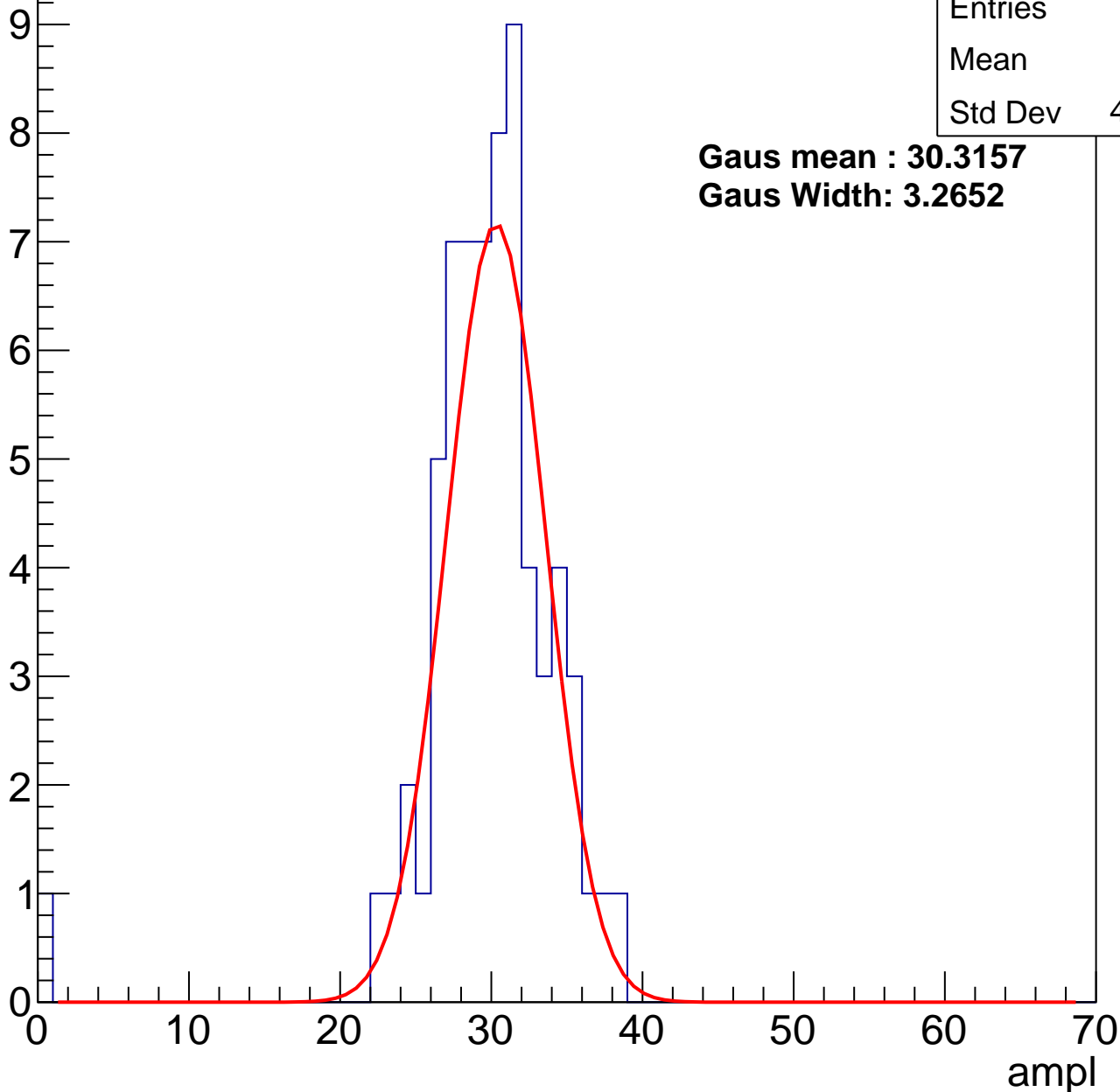
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	29.3
Std Dev	4.917

**Gaus mean : 30.3157**

**Gaus Width: 3.2652**



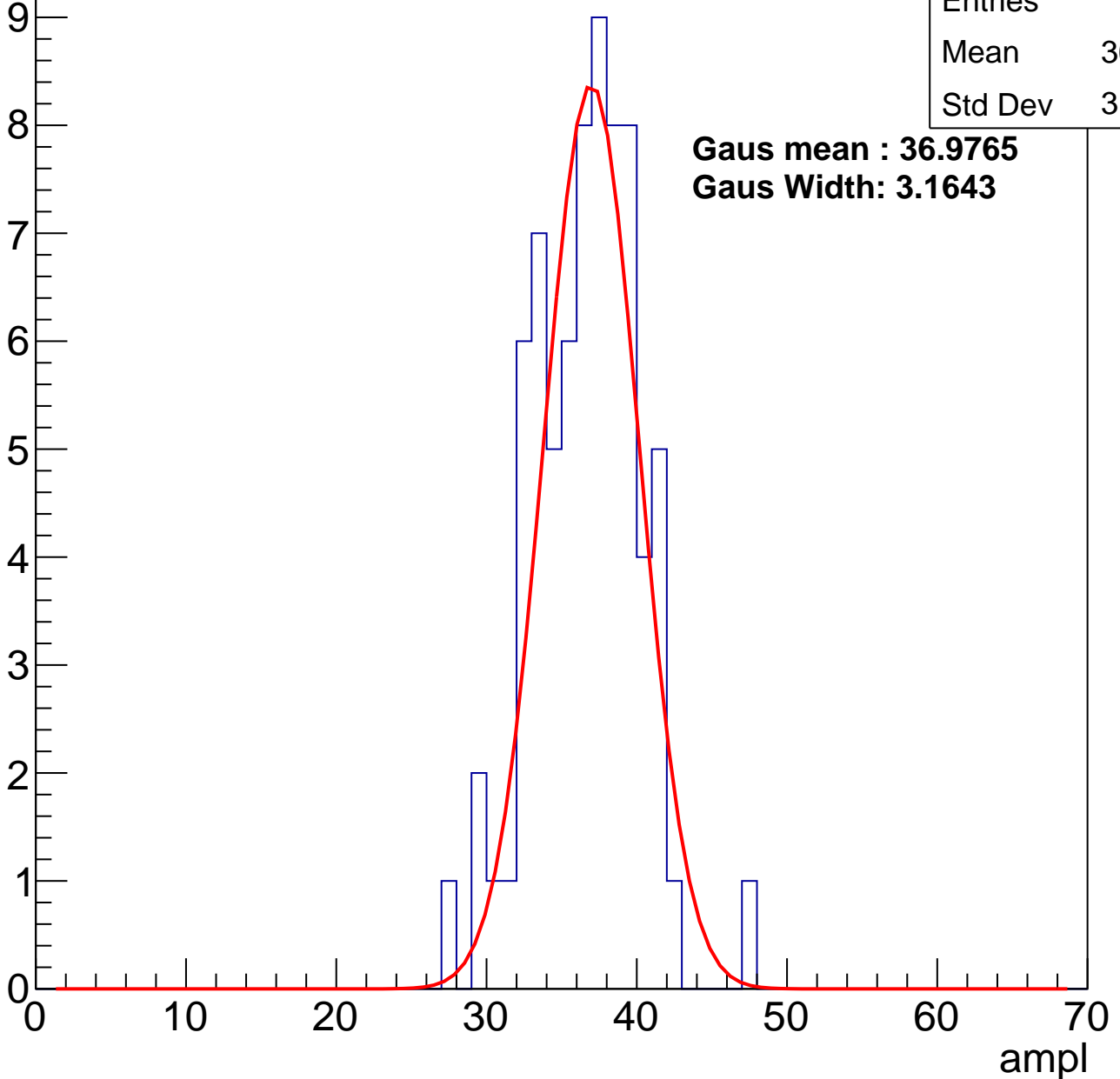
# B0L001S, U21-ch54, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	36.16
Std Dev	3.476

**Gaus mean : 36.9765**  
**Gaus Width: 3.1643**



# B0L001S, U21-ch54, adc2

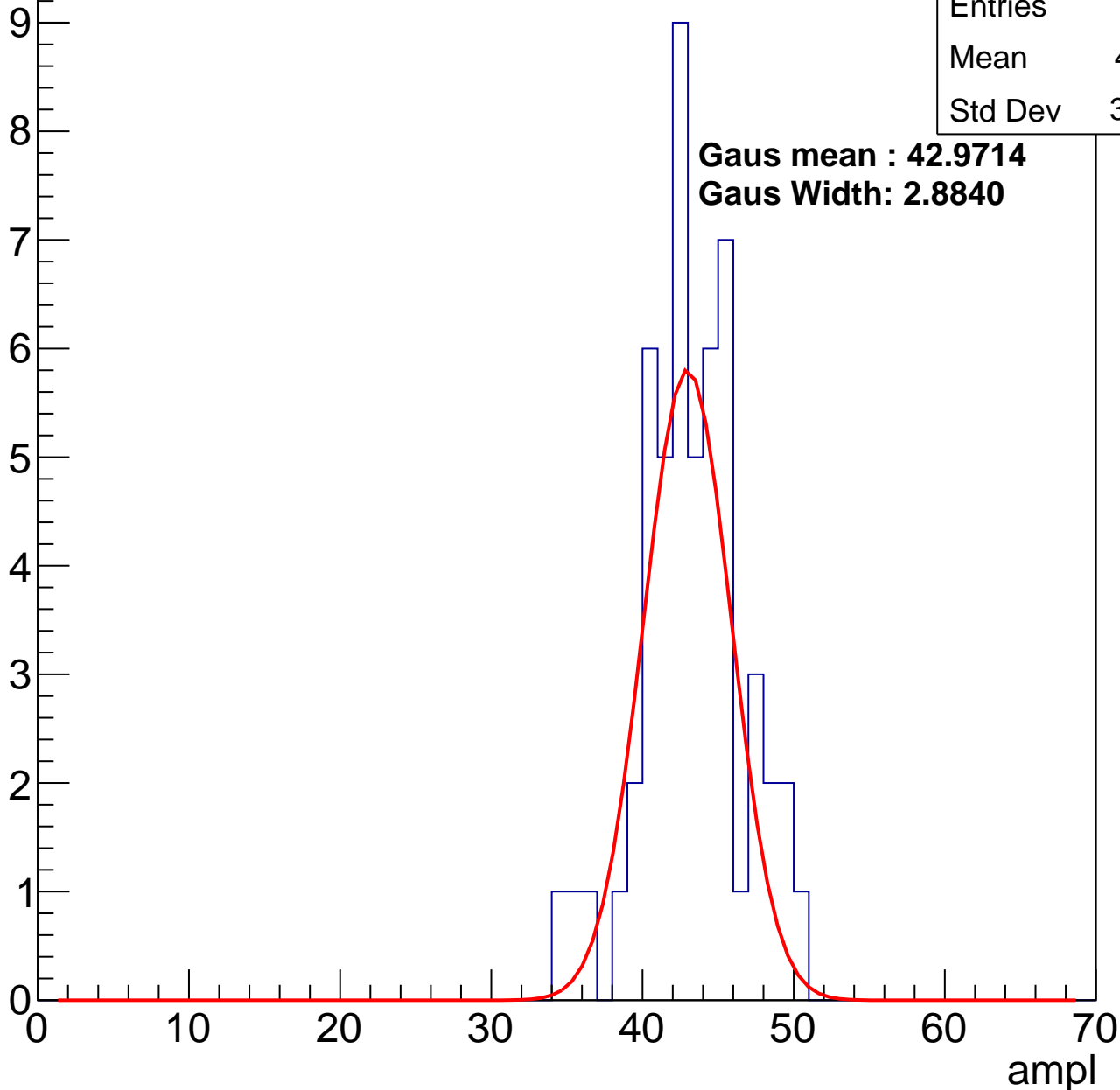
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	42.81
Std Dev	3.348

**Gaus mean : 42.9714**

**Gaus Width: 2.8840**

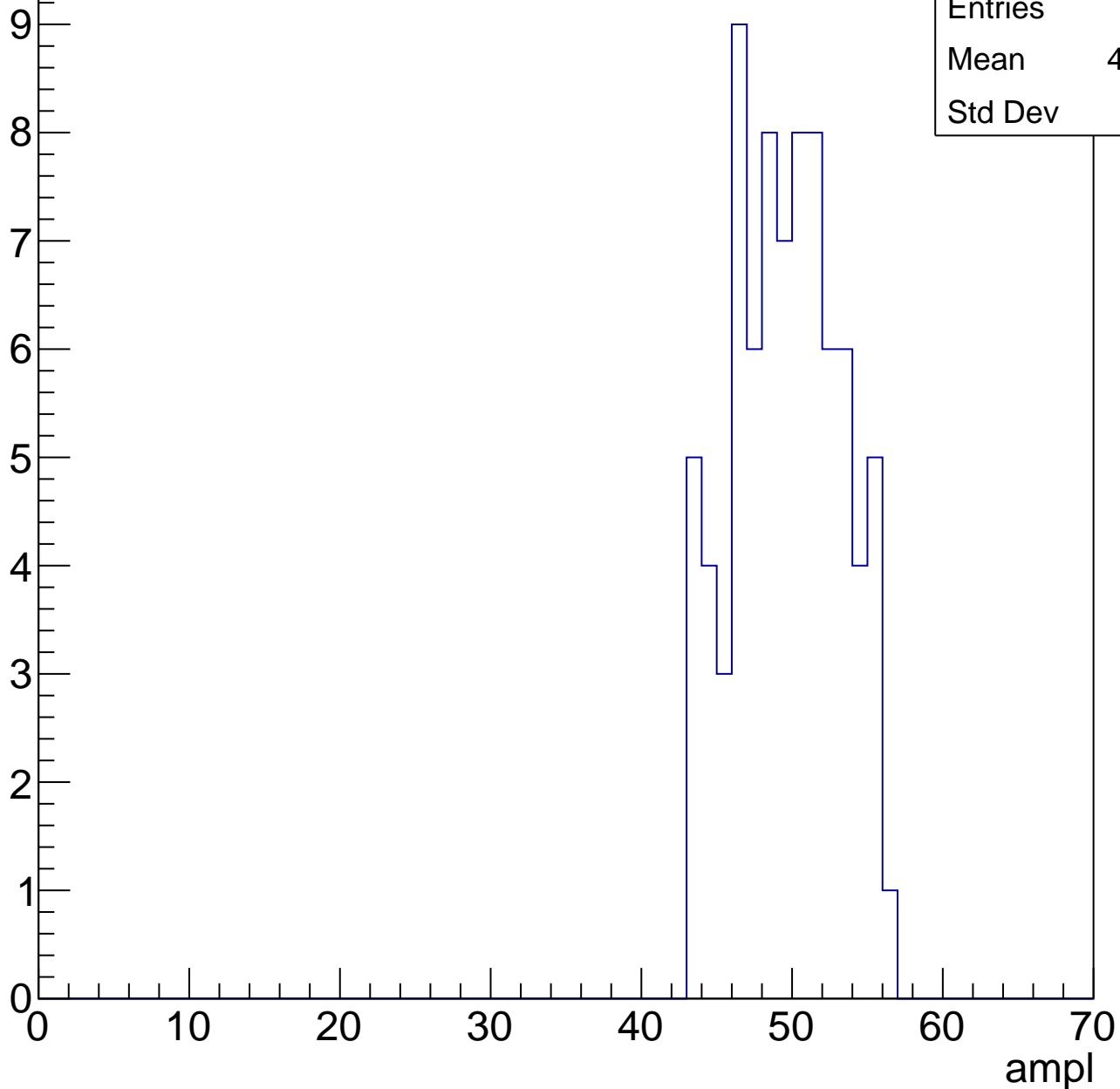


# B0L001S, U21-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	80
Mean	49.17
Std Dev	3.46

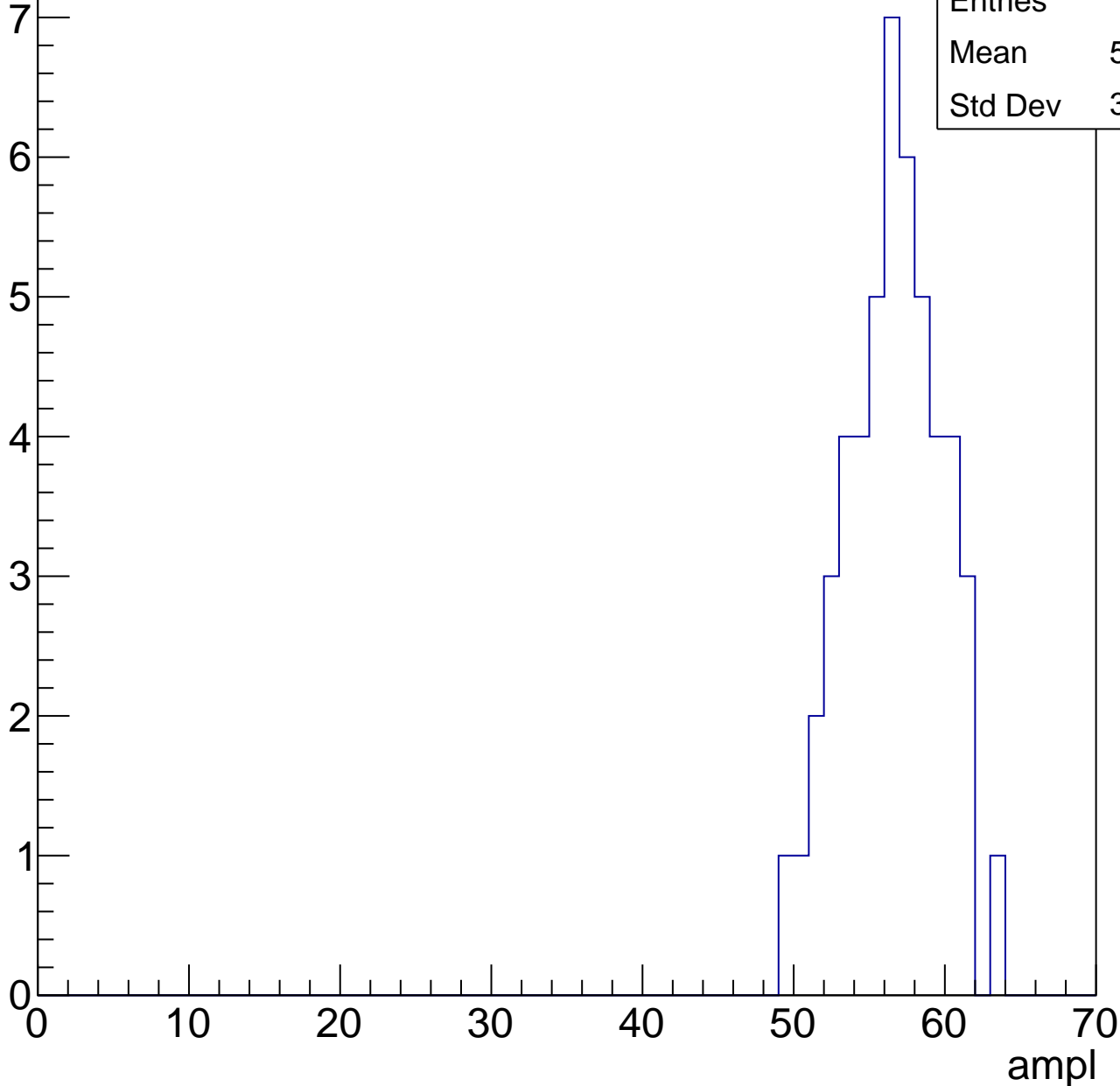


# B0L001S, U21-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	56.12
Std Dev	3.128

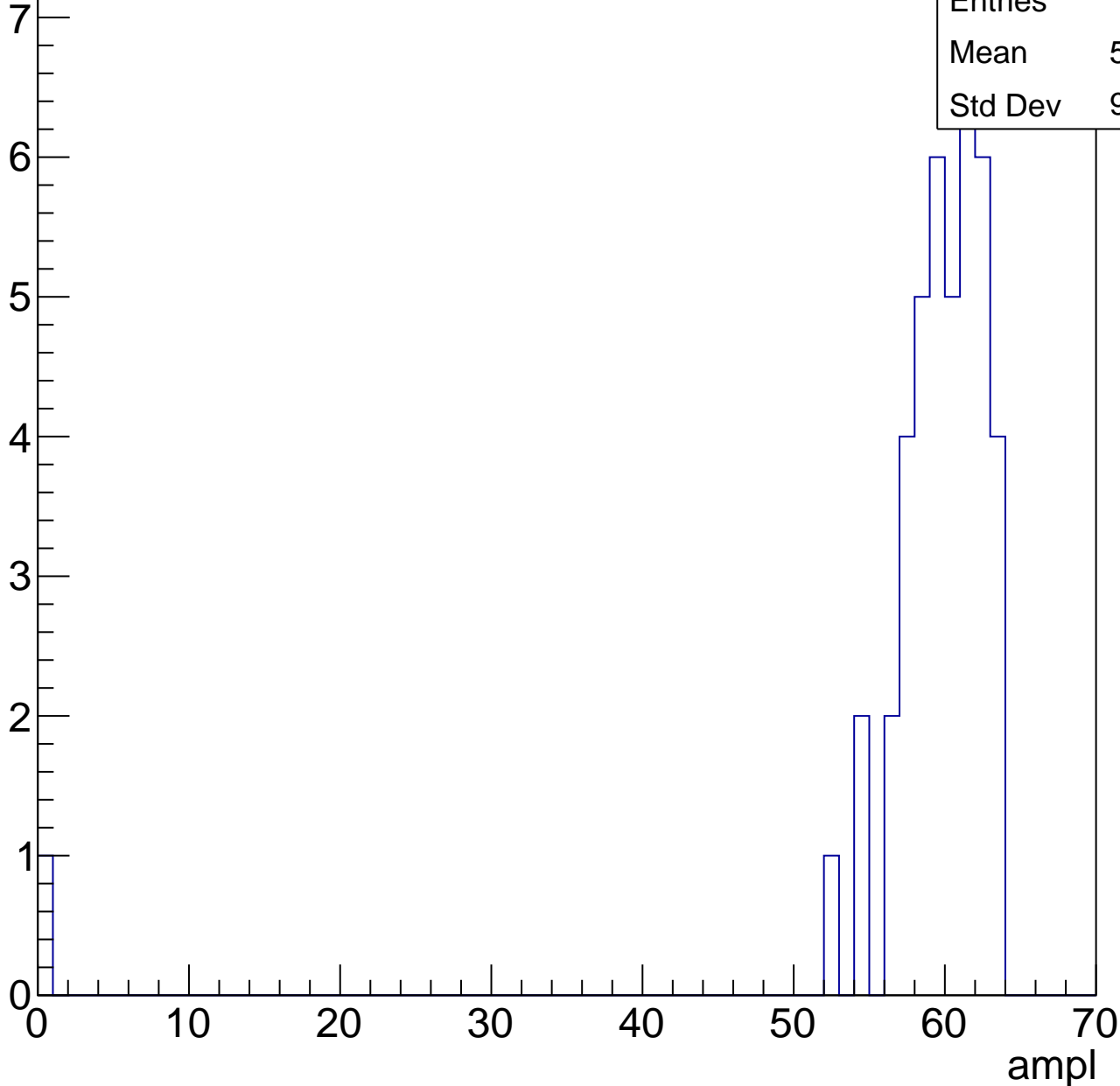


# B0L001S, U21-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	43
Mean	58.02
Std Dev	9.312

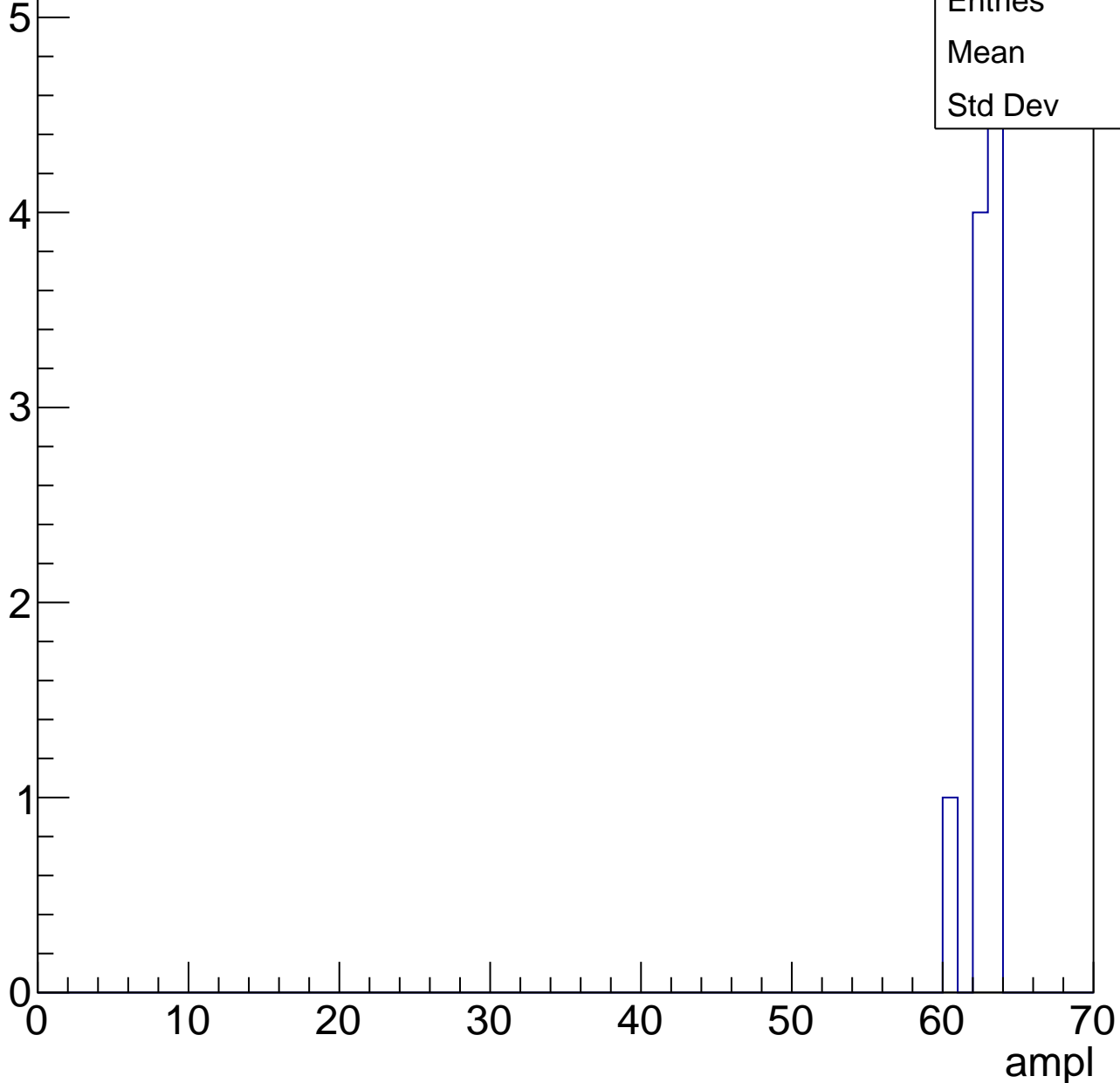


# B0L001S, U21-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	10
Mean	62.3
Std Dev	0.9





# B0L001S, U21-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch55, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	71
Mean	30.31
Std Dev	6.438

**Gaus mean : 31.6590**

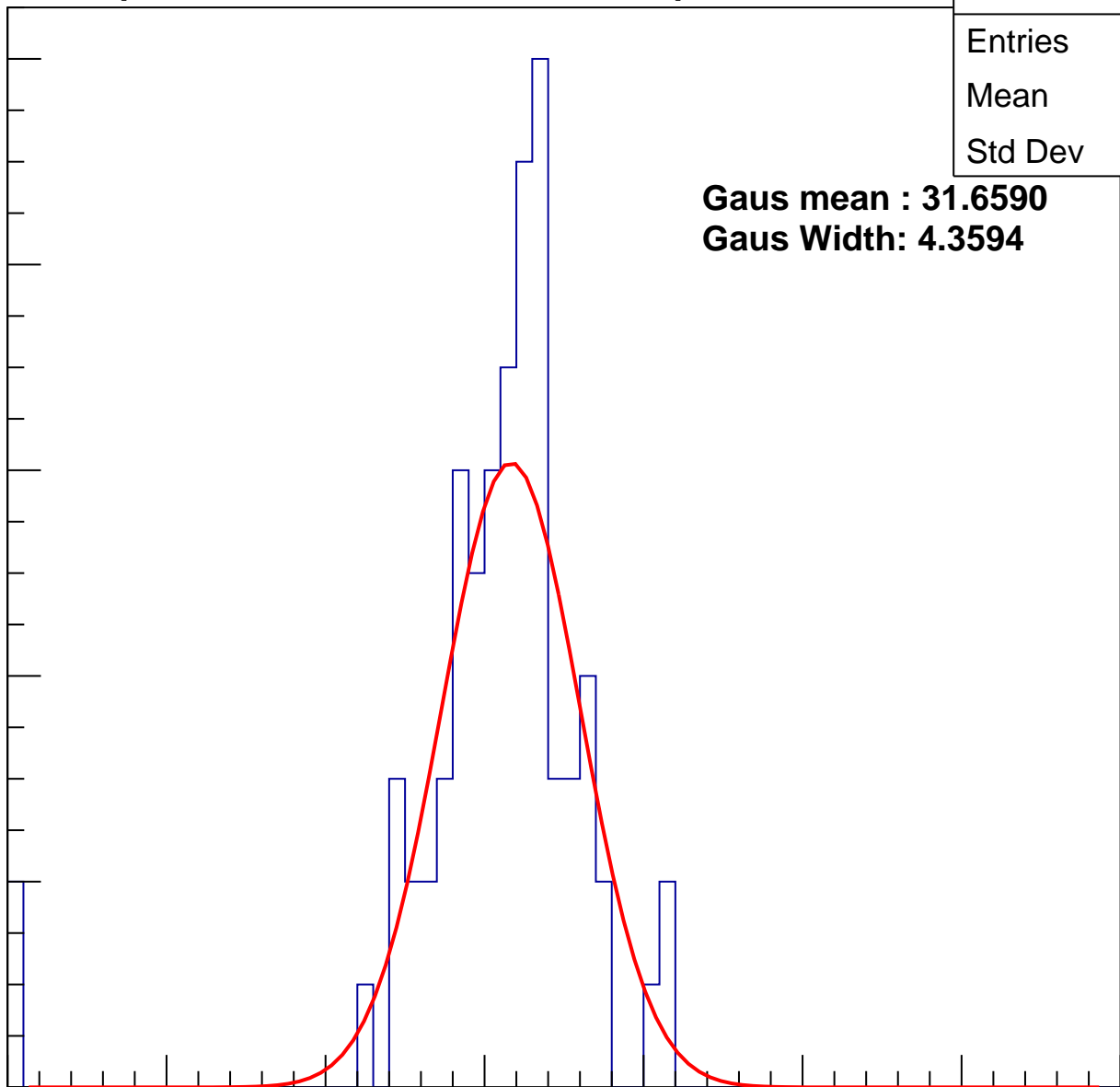
**Gaus Width: 4.3594**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

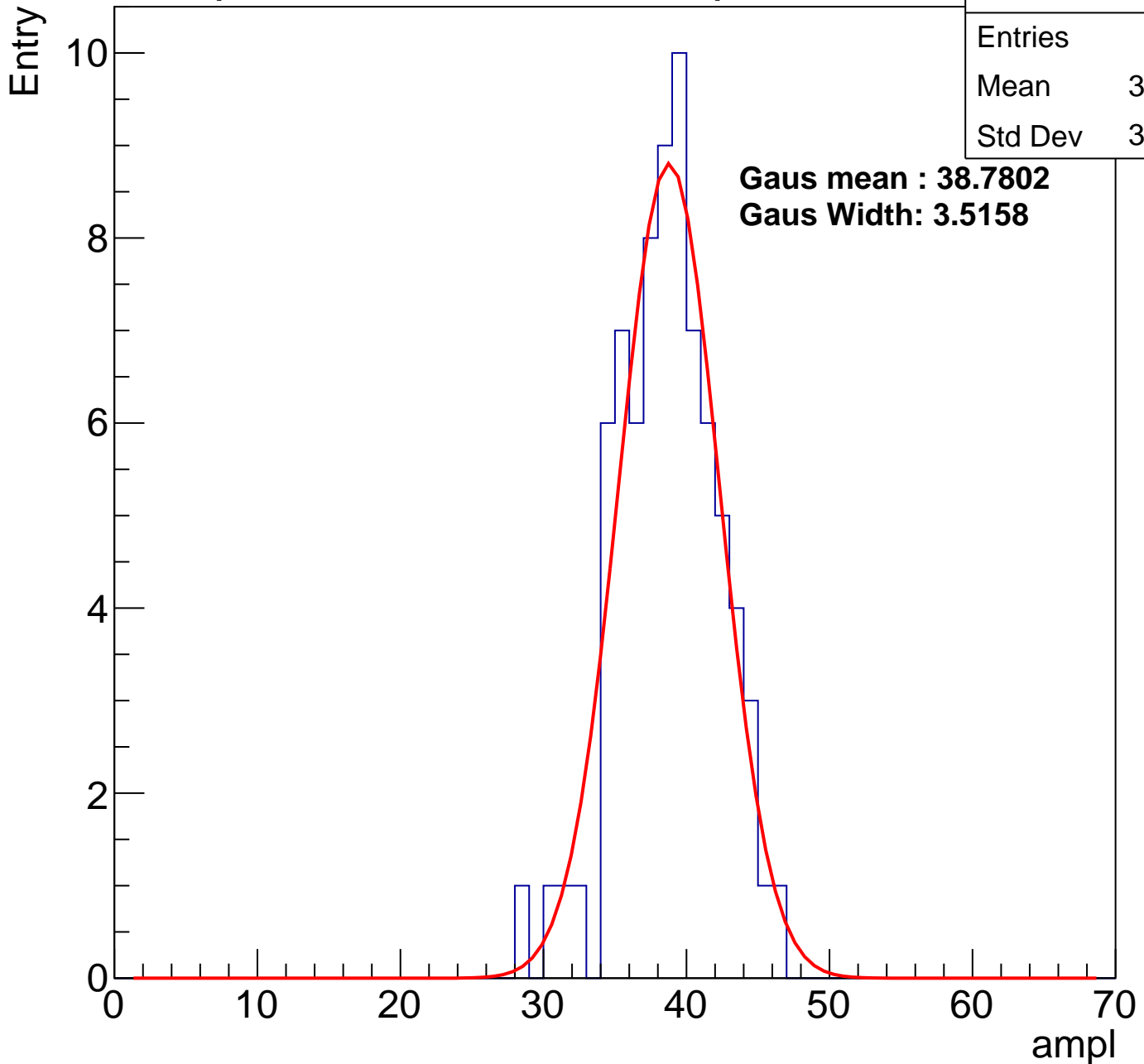


# B0L001S, U21-ch55, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	77
Mean	38.25
Std Dev	3.472

**Gaus mean : 38.7802**  
**Gaus Width: 3.5158**



# B0L001S, U21-ch55, adc2

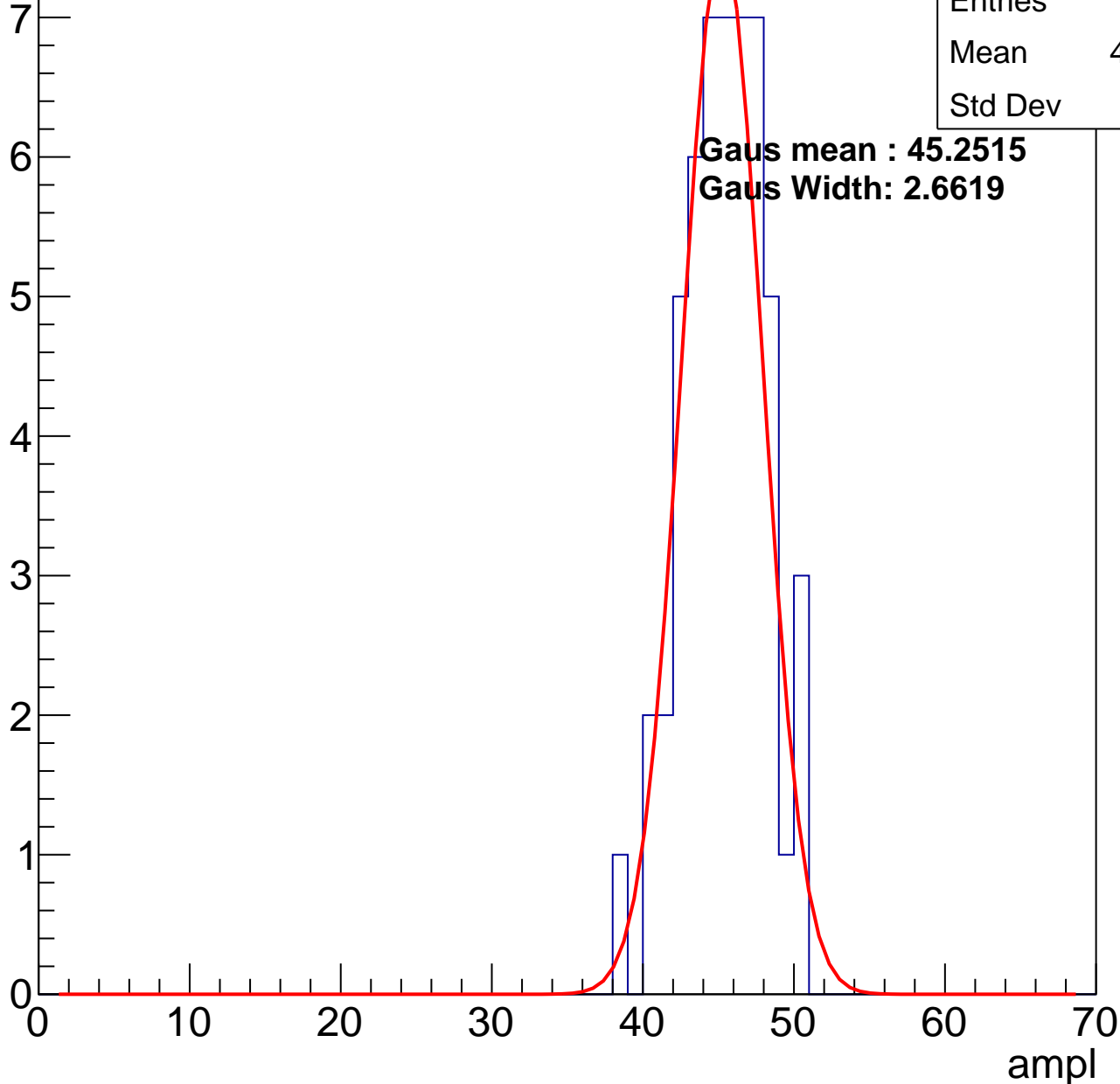
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	44.92
Std Dev	2.67

**Gaus mean : 45.2515**

**Gaus Width: 2.6619**

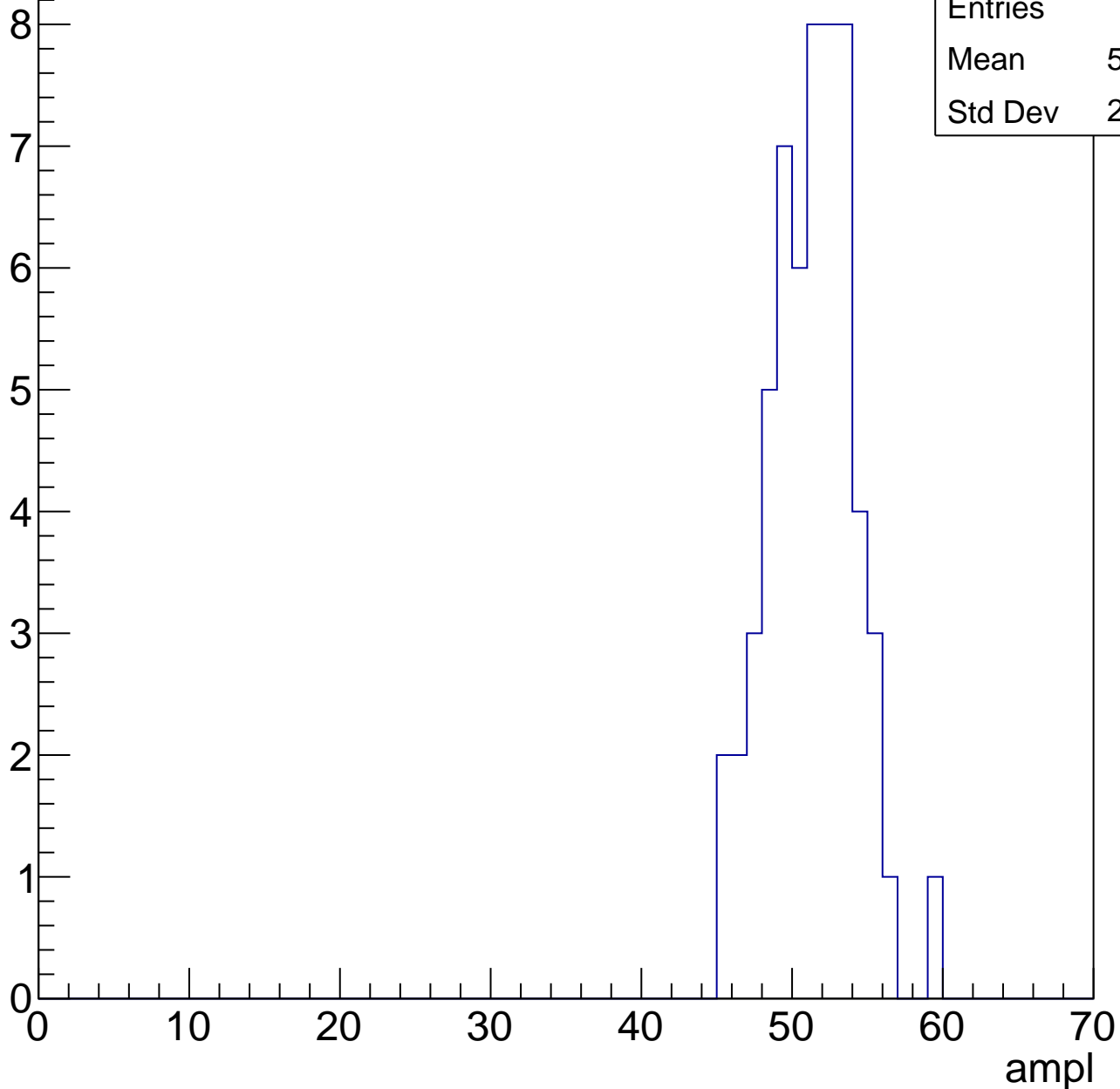


# B0L001S, U21-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	50.86
Std Dev	2.819

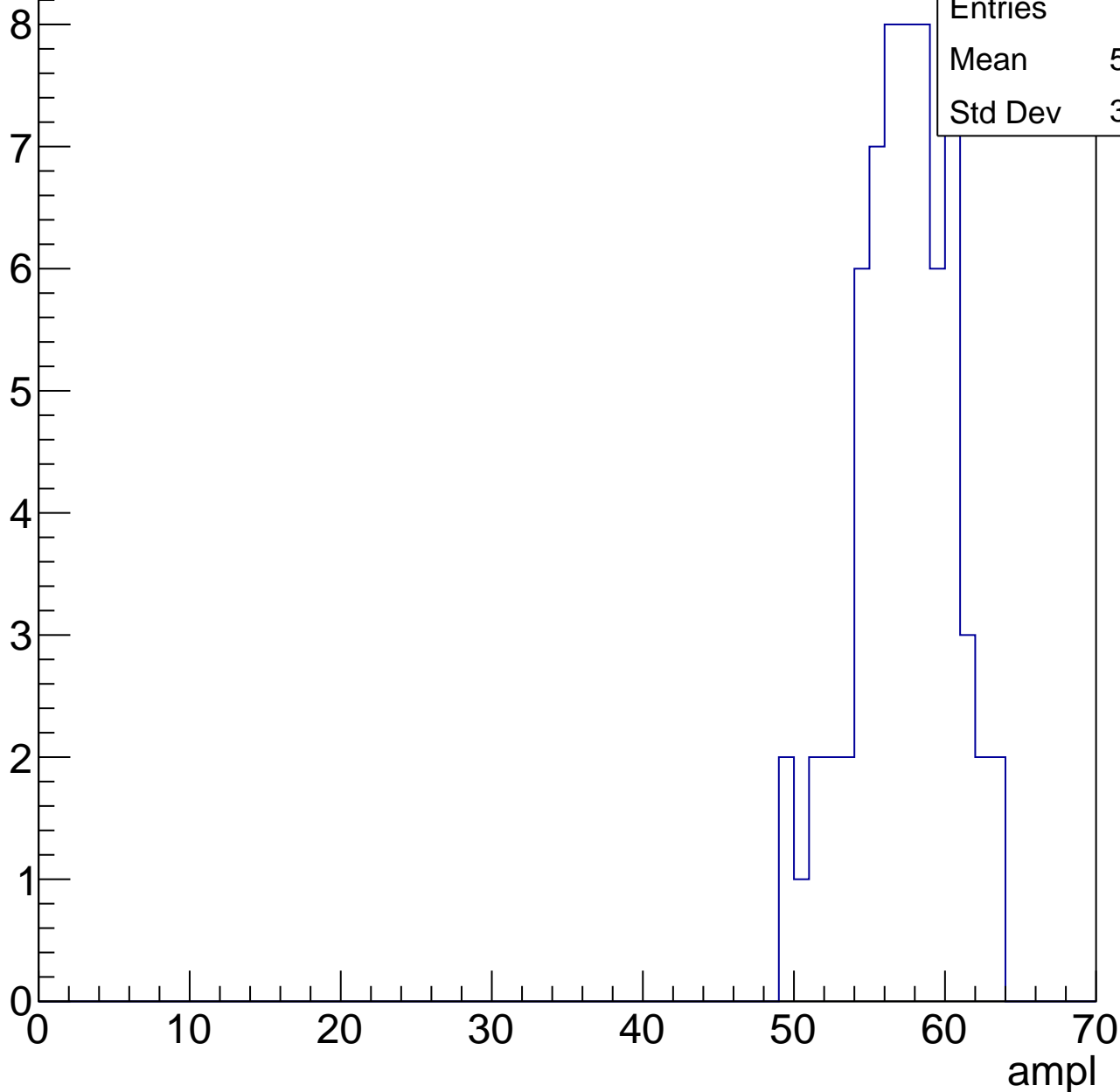


# B0L001S, U21-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	56.78
Std Dev	3.213

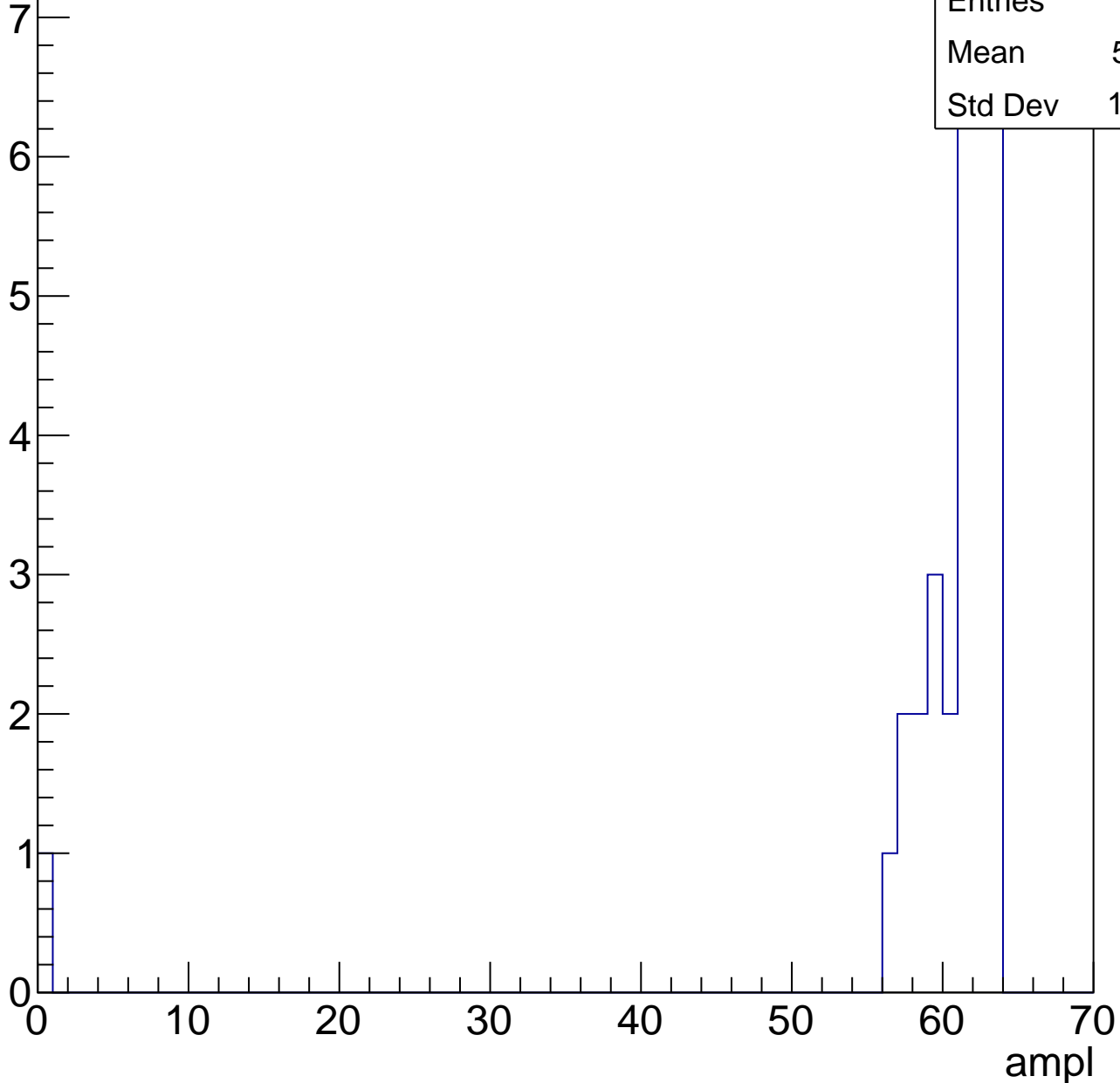


# B0L001S, U21-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	32
Mean	58.91
Std Dev	10.76



# B0L001S, U21-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

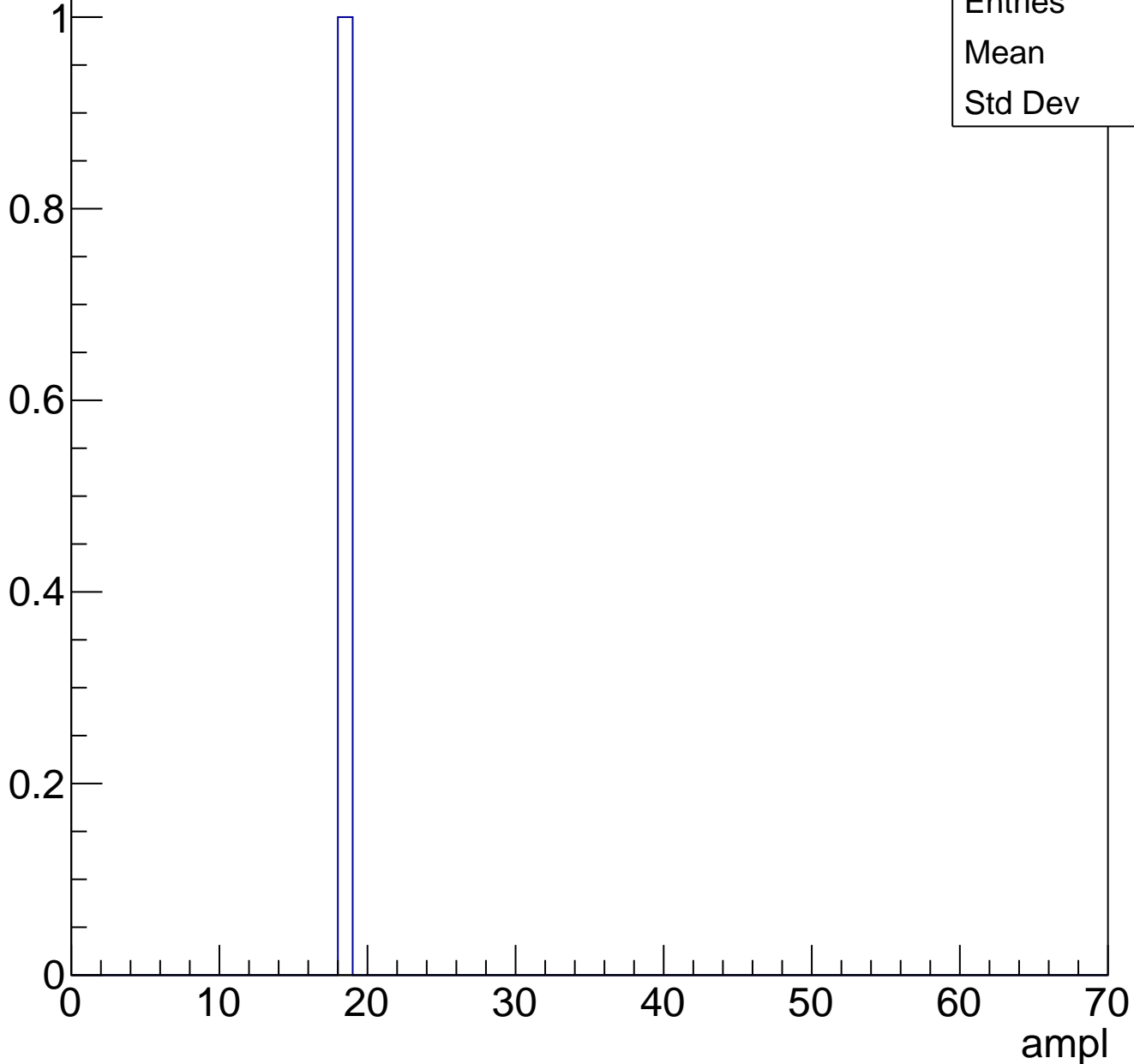




# B0L001S, U21-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	18
Std Dev	0

# B0L001S, U21-ch56, adc0

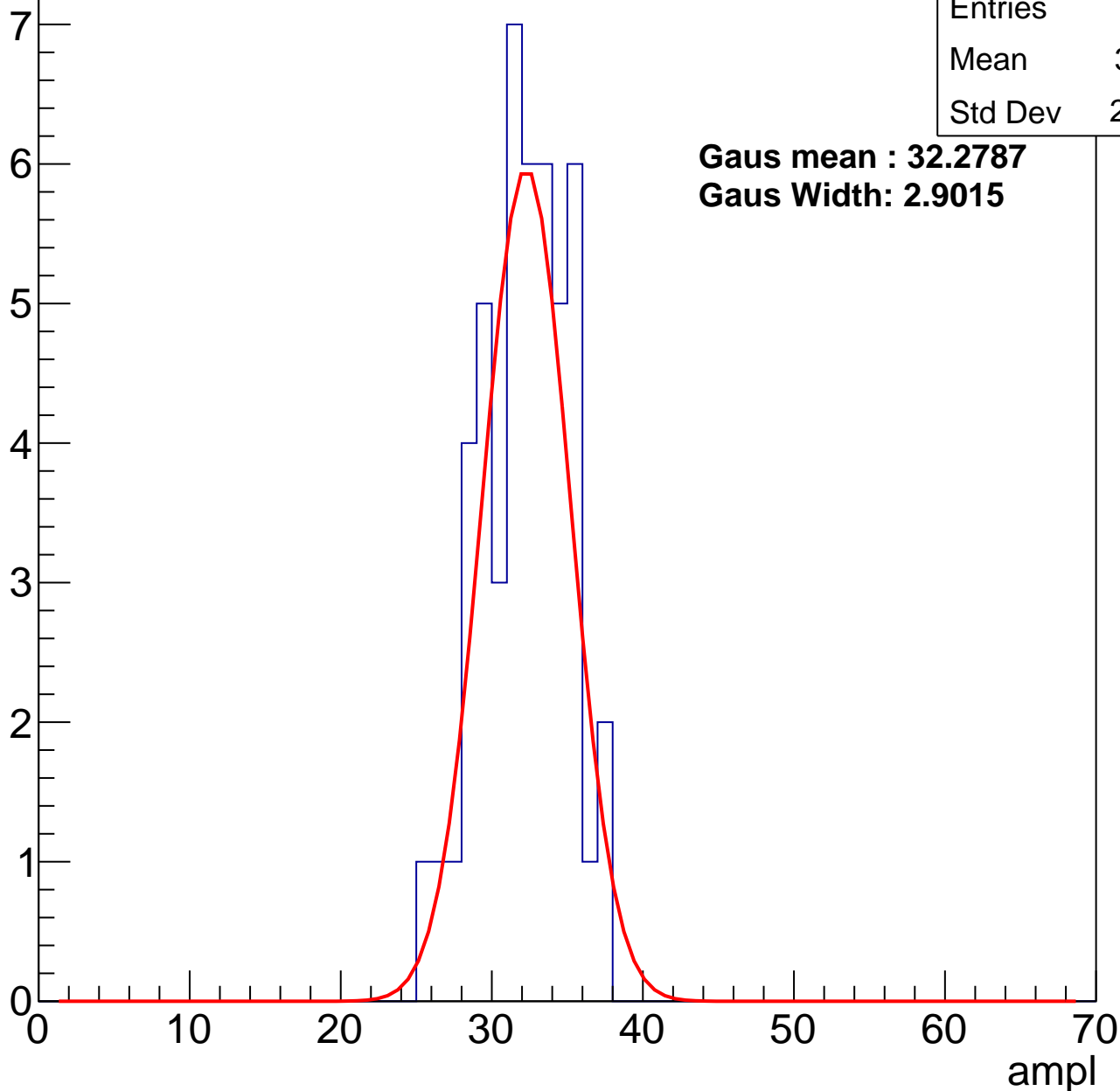
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	31.71
Std Dev	2.813

**Gaus mean : 32.2787**

**Gaus Width: 2.9015**



# B0L001S, U21-ch56, adc1

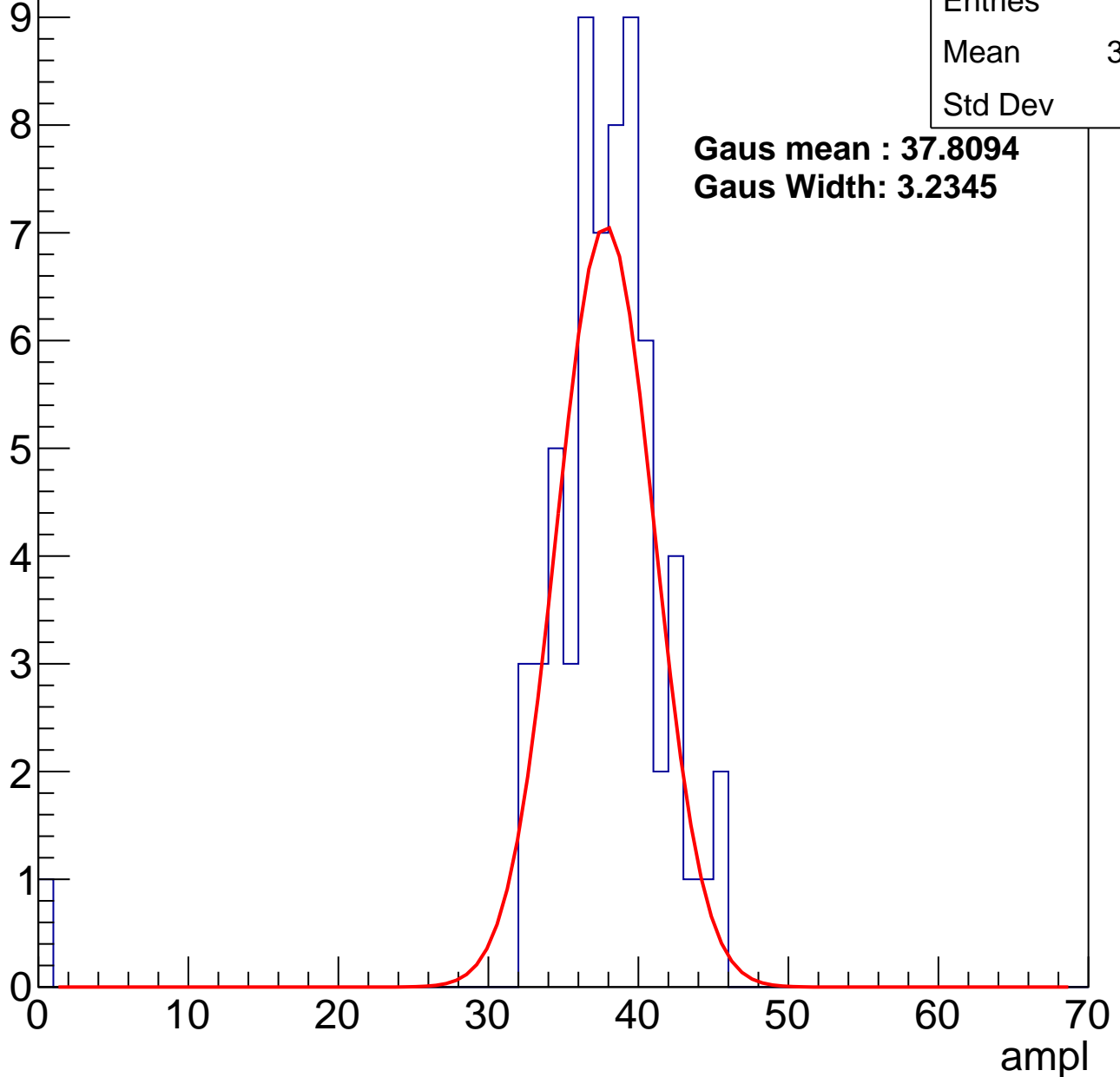
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	37.11
Std Dev	5.59

**Gaus mean : 37.8094**

**Gaus Width: 3.2345**



# B0L001S, U21-ch56, adc2

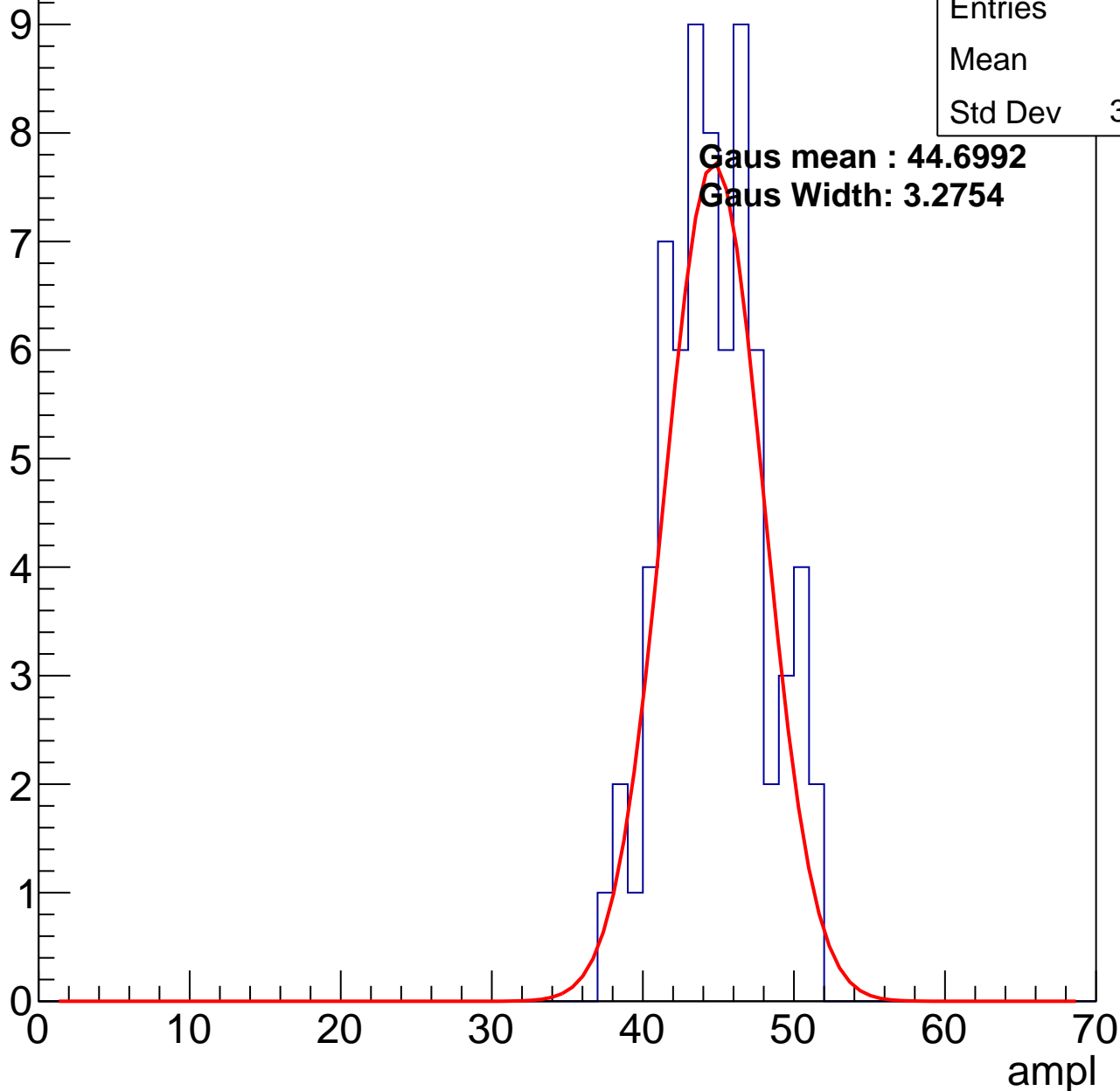
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	44.3
Std Dev	3.262

**Gaus mean : 44.6992**

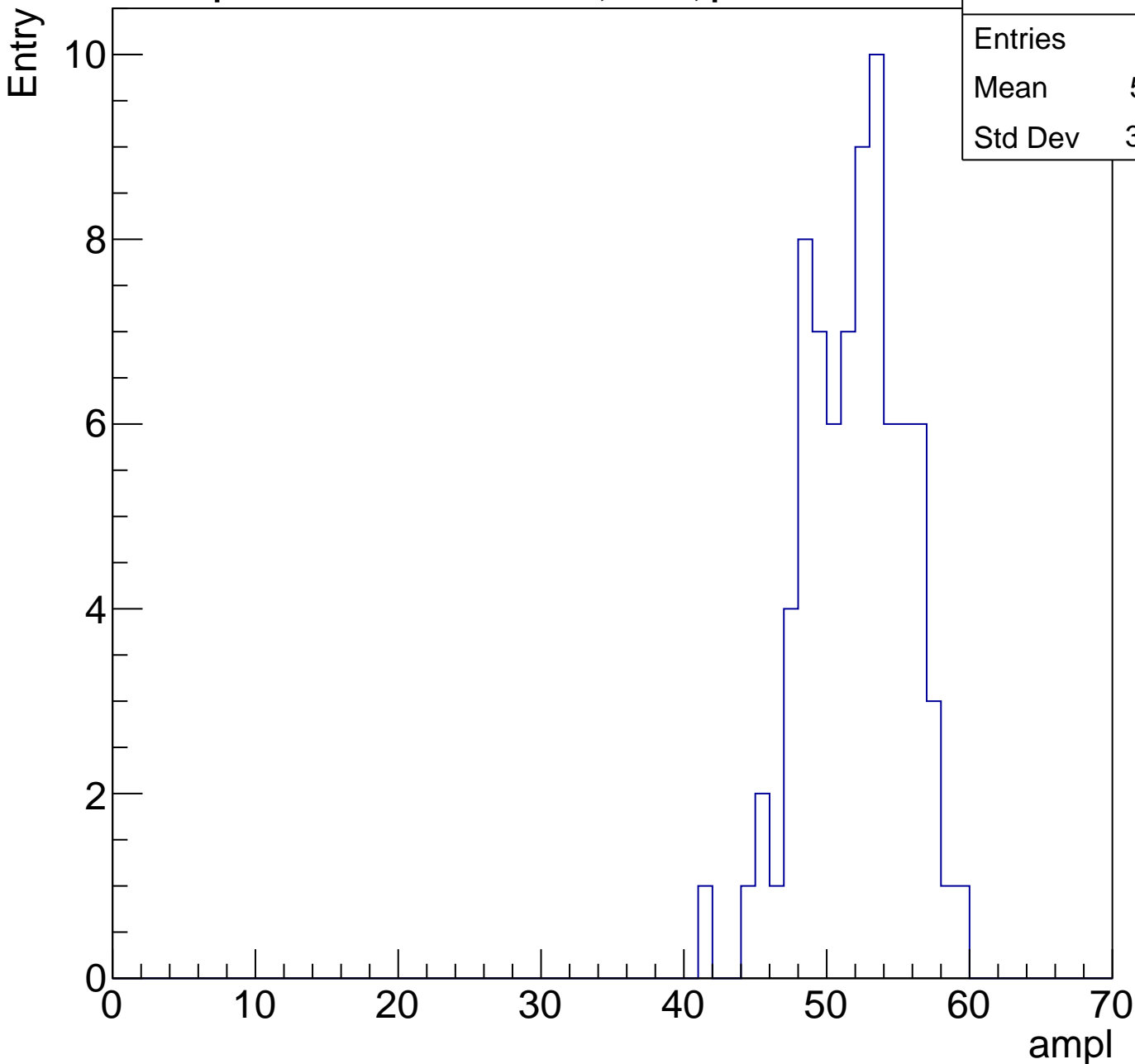
**Gaus Width: 3.2754**



# B0L001S, U21-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	79
Mean	51.51
Std Dev	3.496

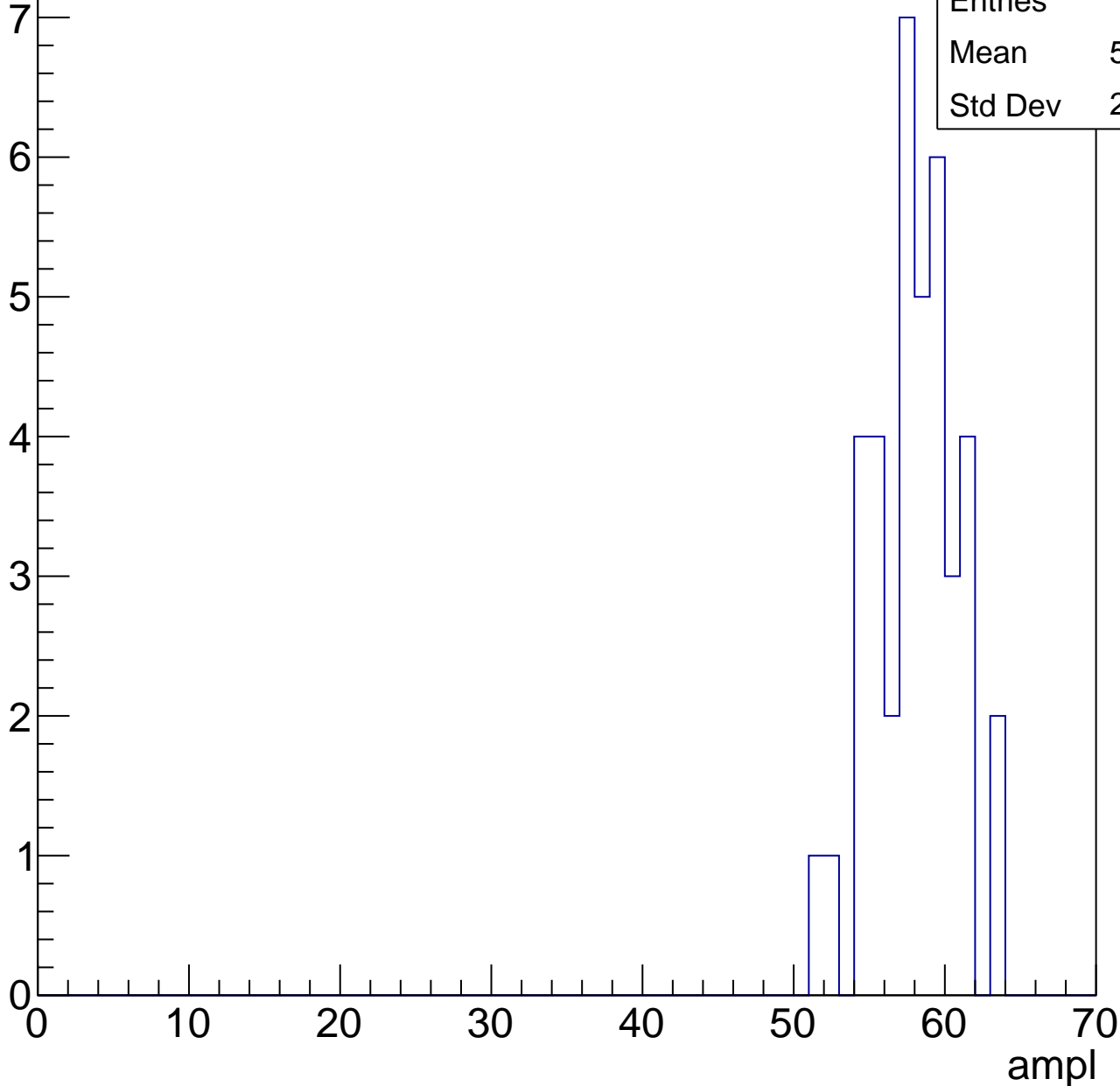


# B0L001S, U21-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	39
Mean	57.54
Std Dev	2.754



# B0L001S, U21-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	40
Mean	59.2
Std Dev	9.662

Entry

10

8

6

4

2

0

0

10

20

30

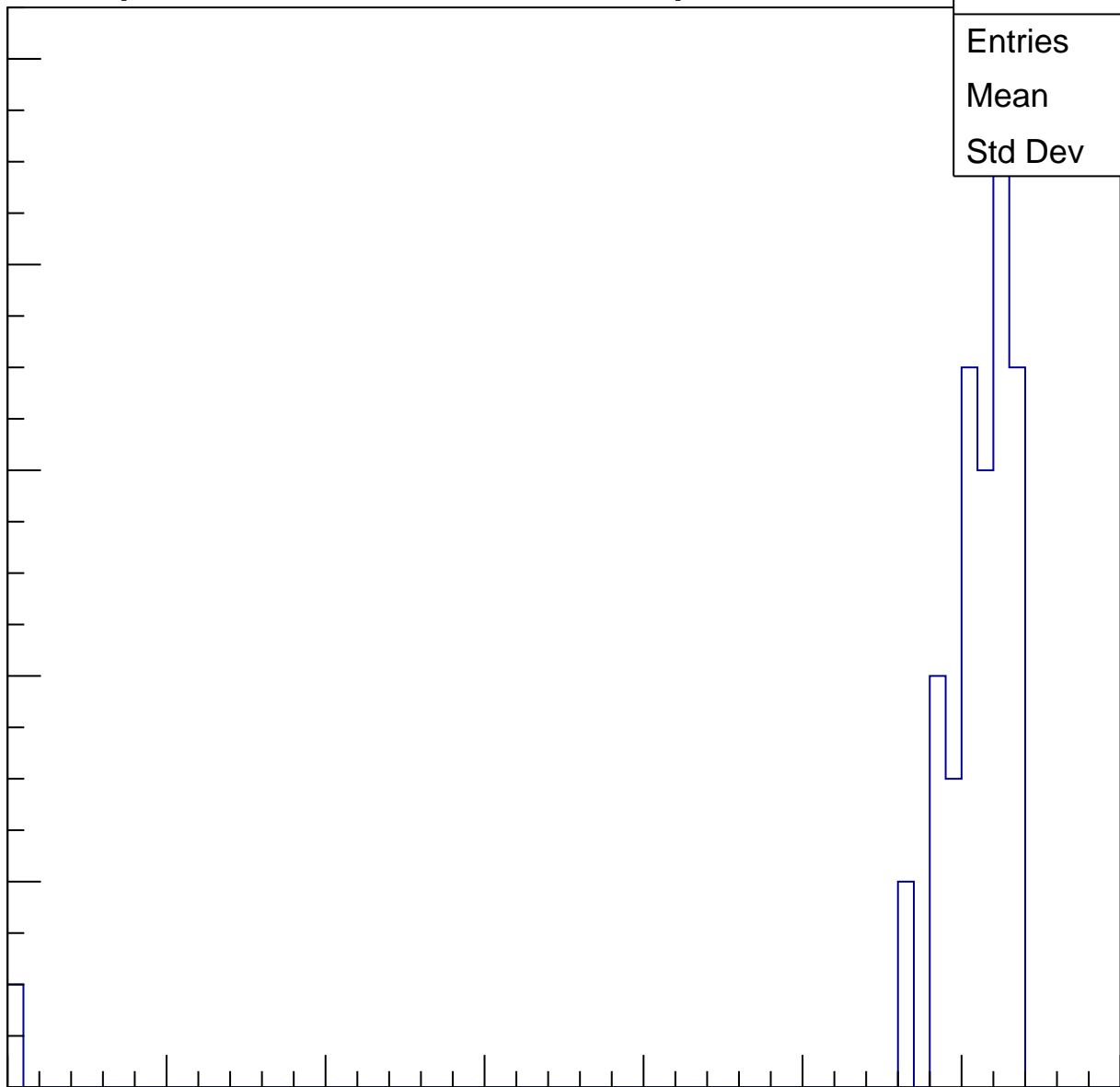
40

50

60

70

ampl



# B0L001S, U21-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch57, adc0

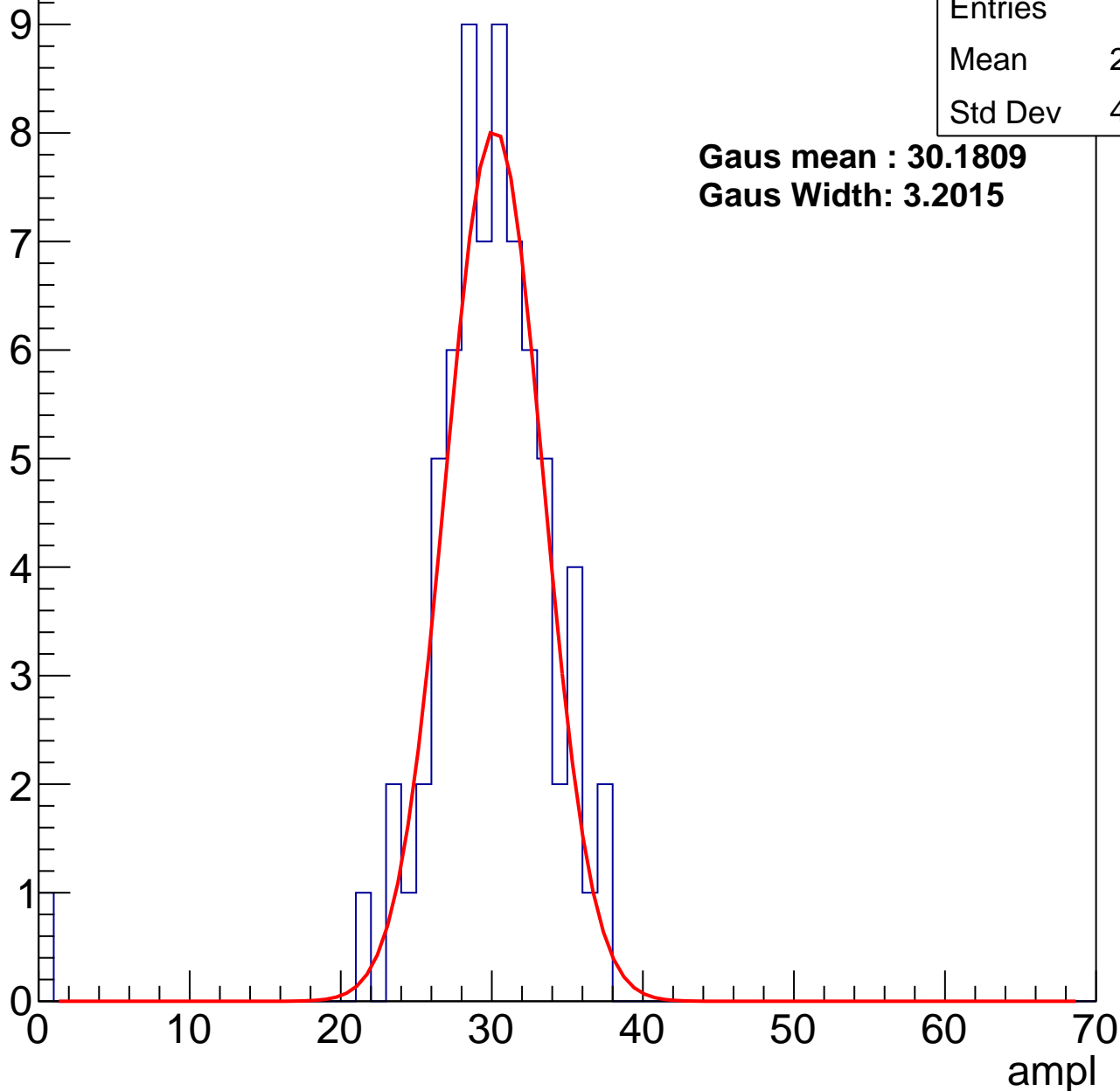
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	29.29
Std Dev	4.853

**Gaus mean : 30.1809**

**Gaus Width: 3.2015**



# B0L001S, U21-ch57, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	77
Mean	37.13
Std Dev	3.397

**Gaus mean : 37.5672**

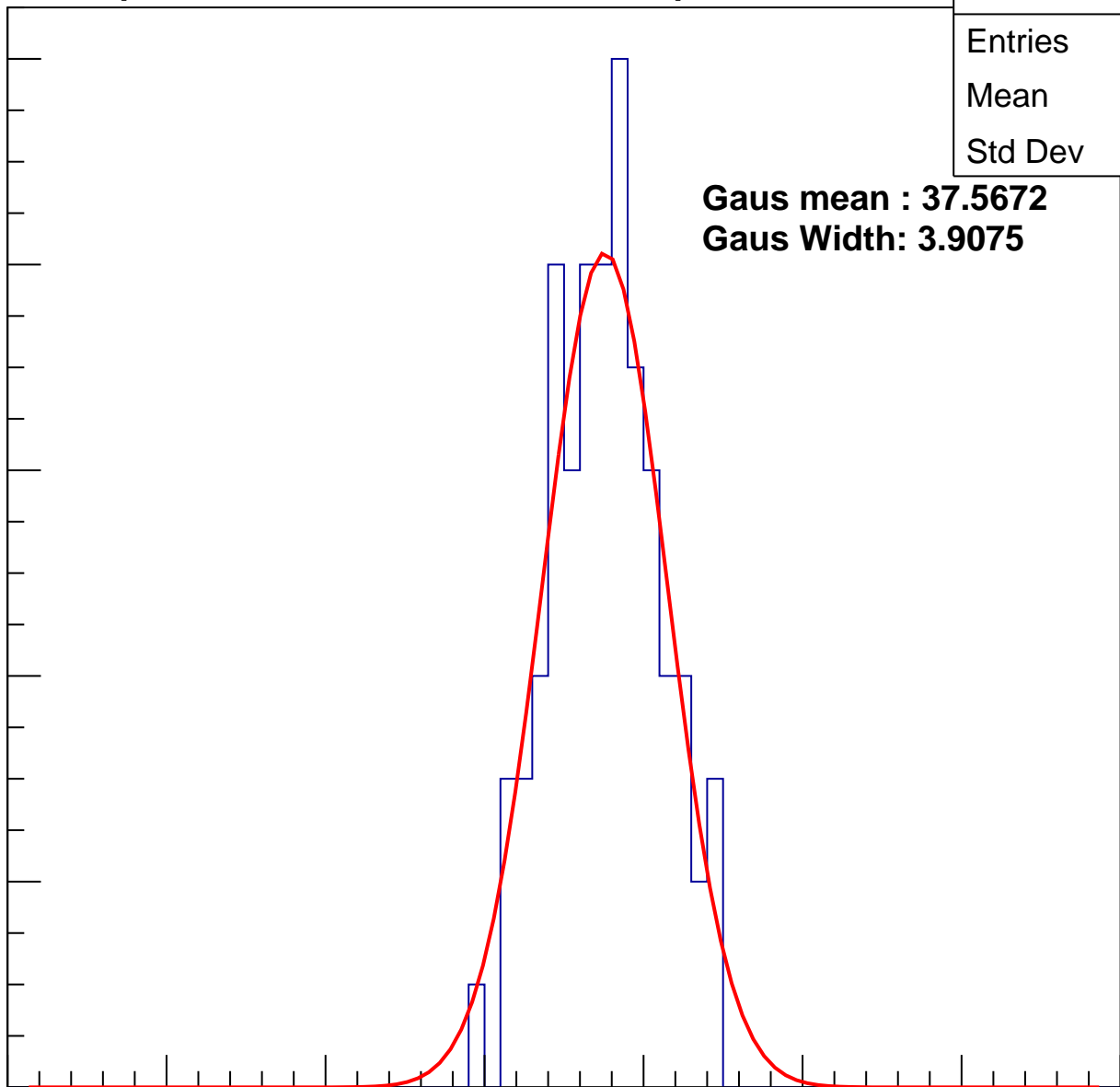
**Gaus Width: 3.9075**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

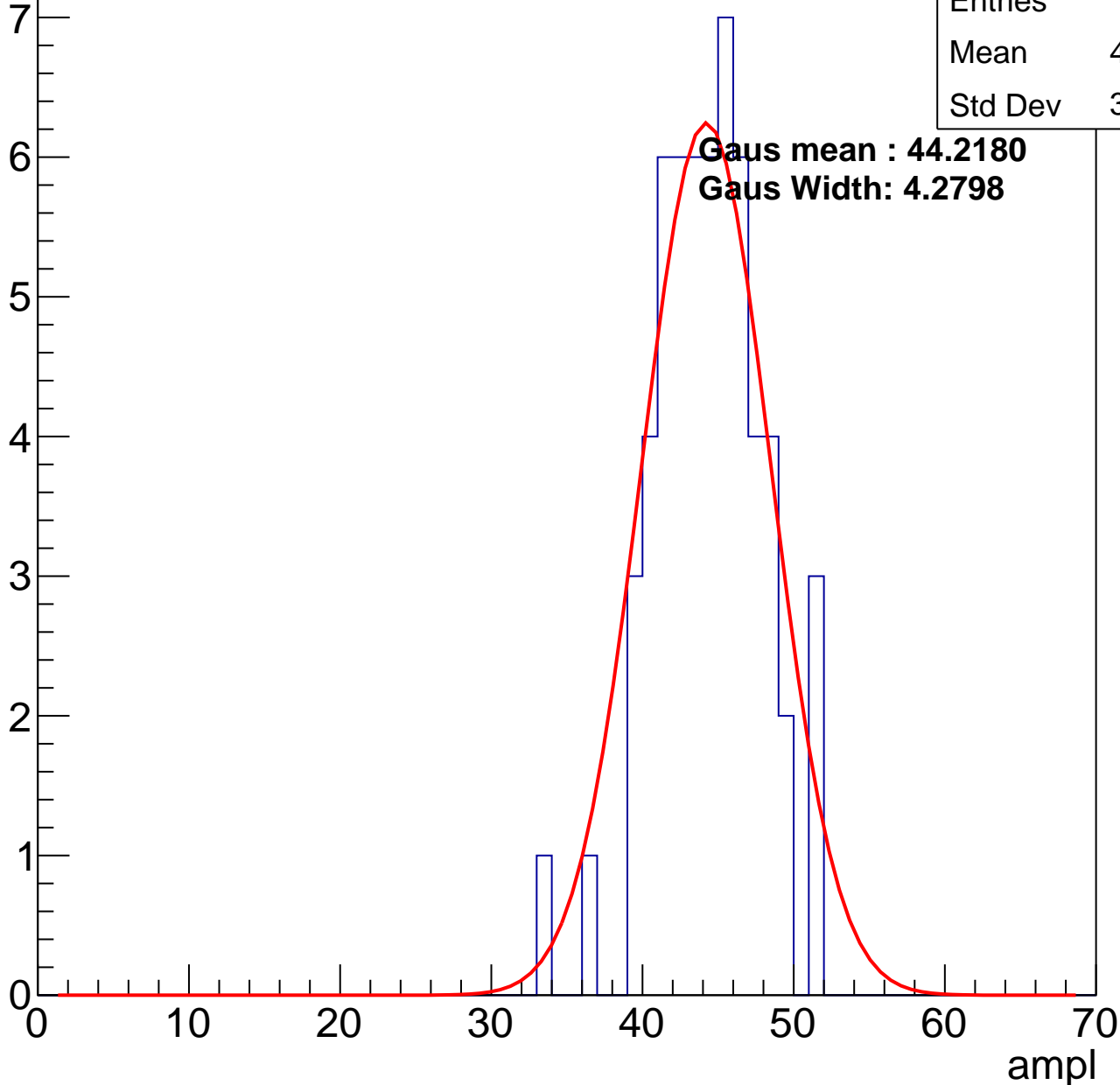


# B0L001S, U21-ch57, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	43.86
Std Dev	3.529



# B0L001S, U21-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

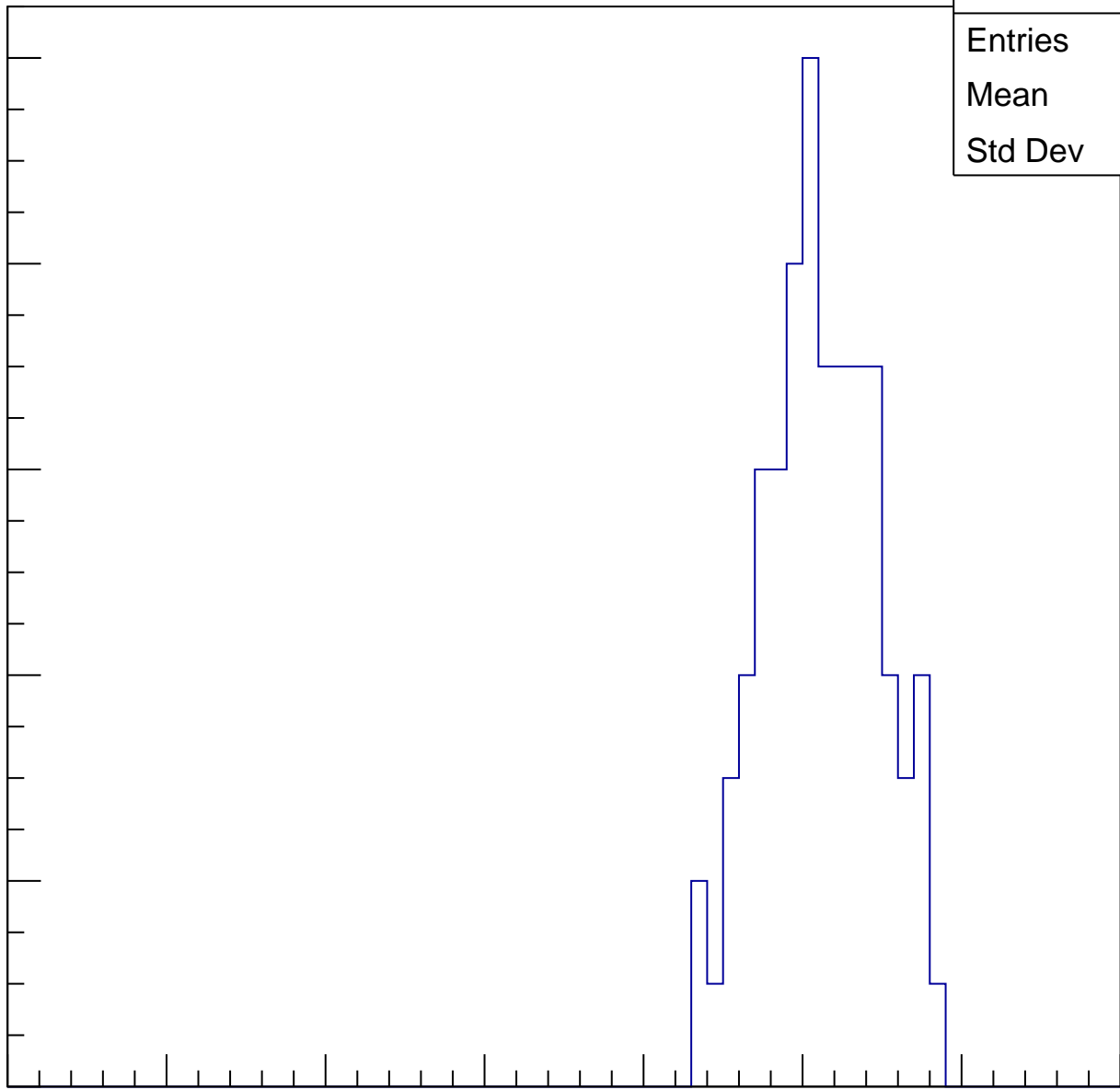
Entries	80
Mean	50.69
Std Dev	3.534

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U21-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

6

5

4

3

2

1

0

Entries	49
Mean	56.33
Std Dev	8.691

10

20

30

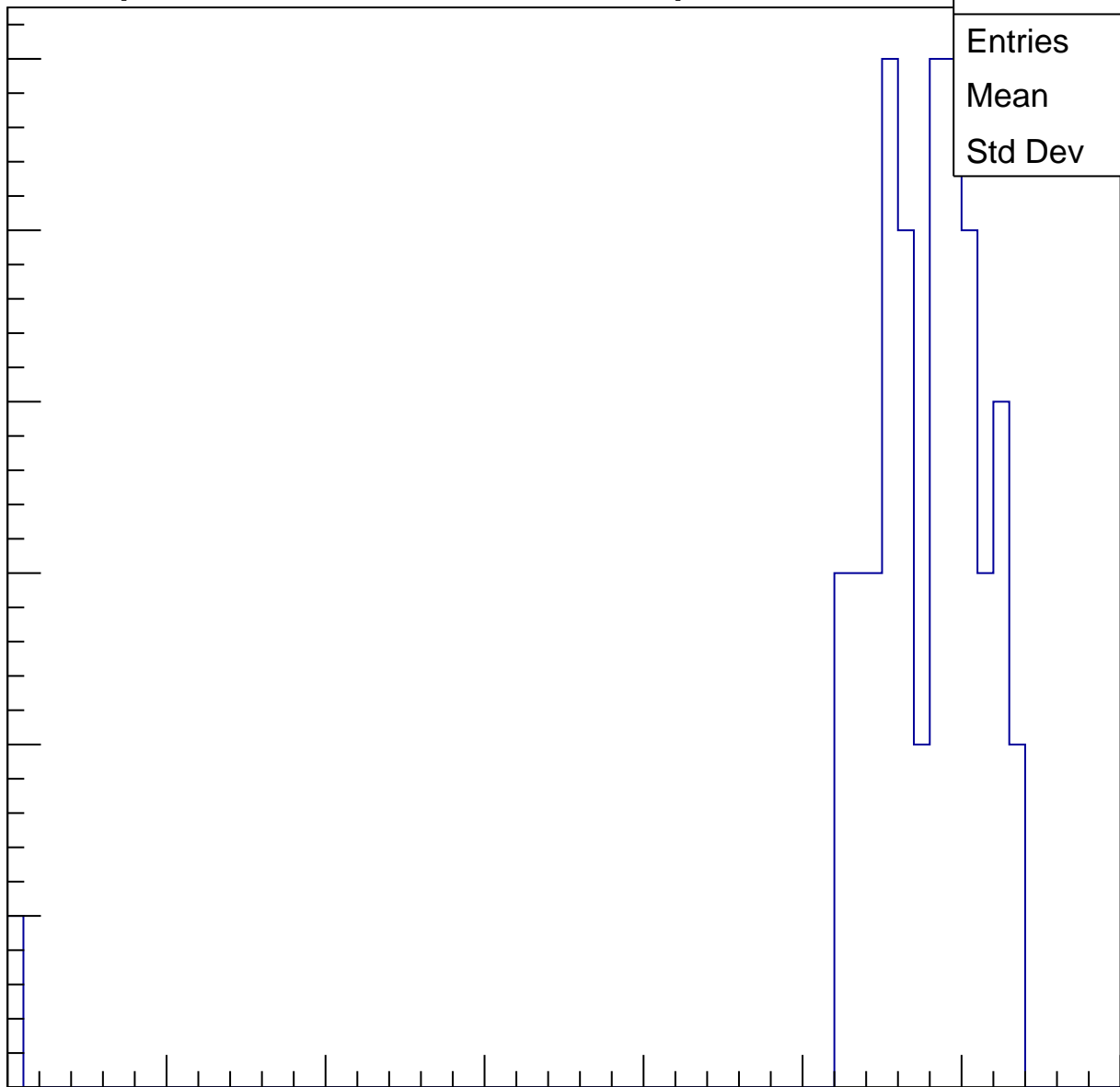
40

50

60

70

ampl



# B0L001S, U21-ch57, adc5

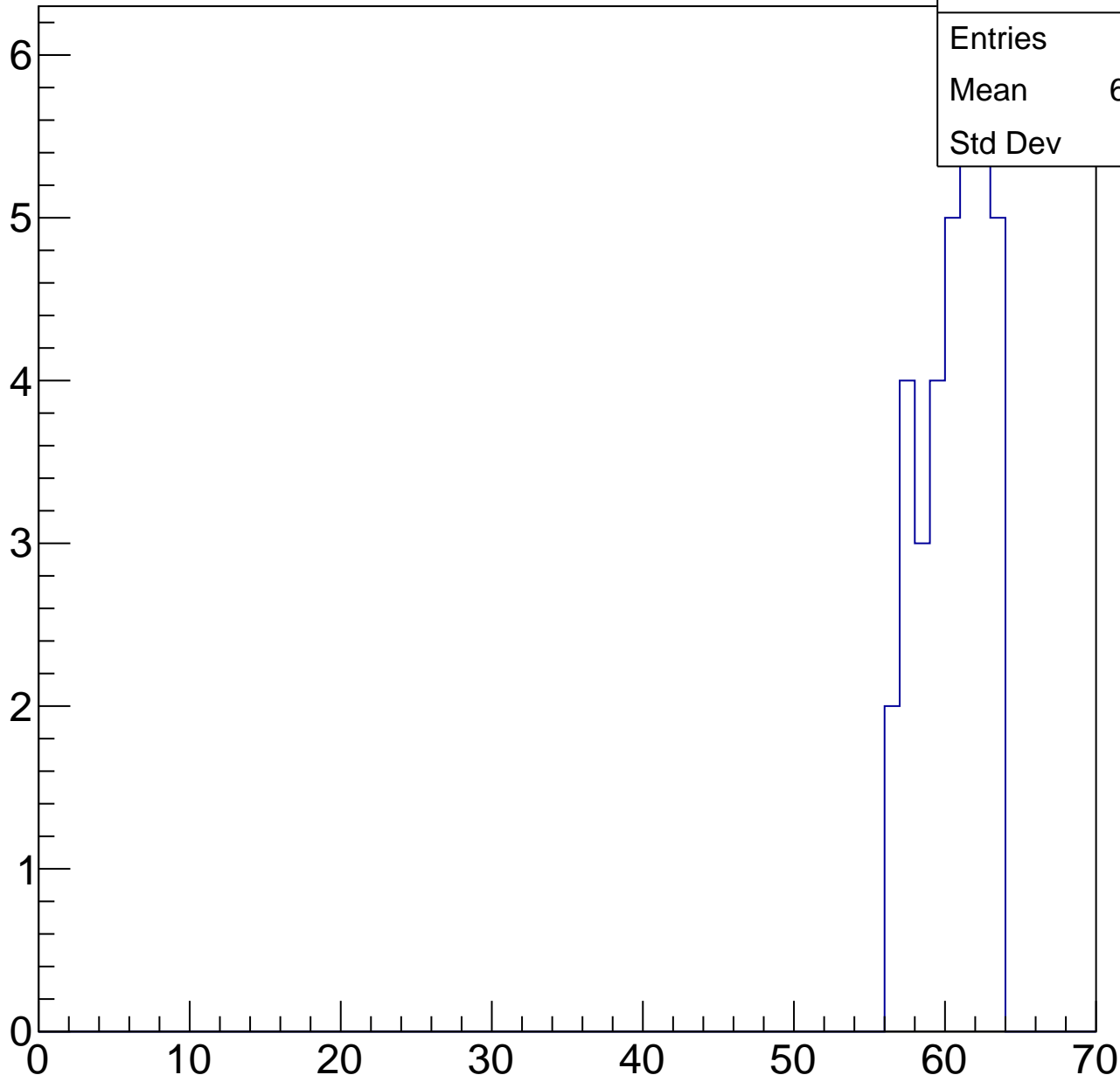
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

6  
5  
4  
3  
2  
1  
0

Entries	35
Mean	60.09
Std Dev	2.13

ampl



# B0L001S, U21-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch58, adc0

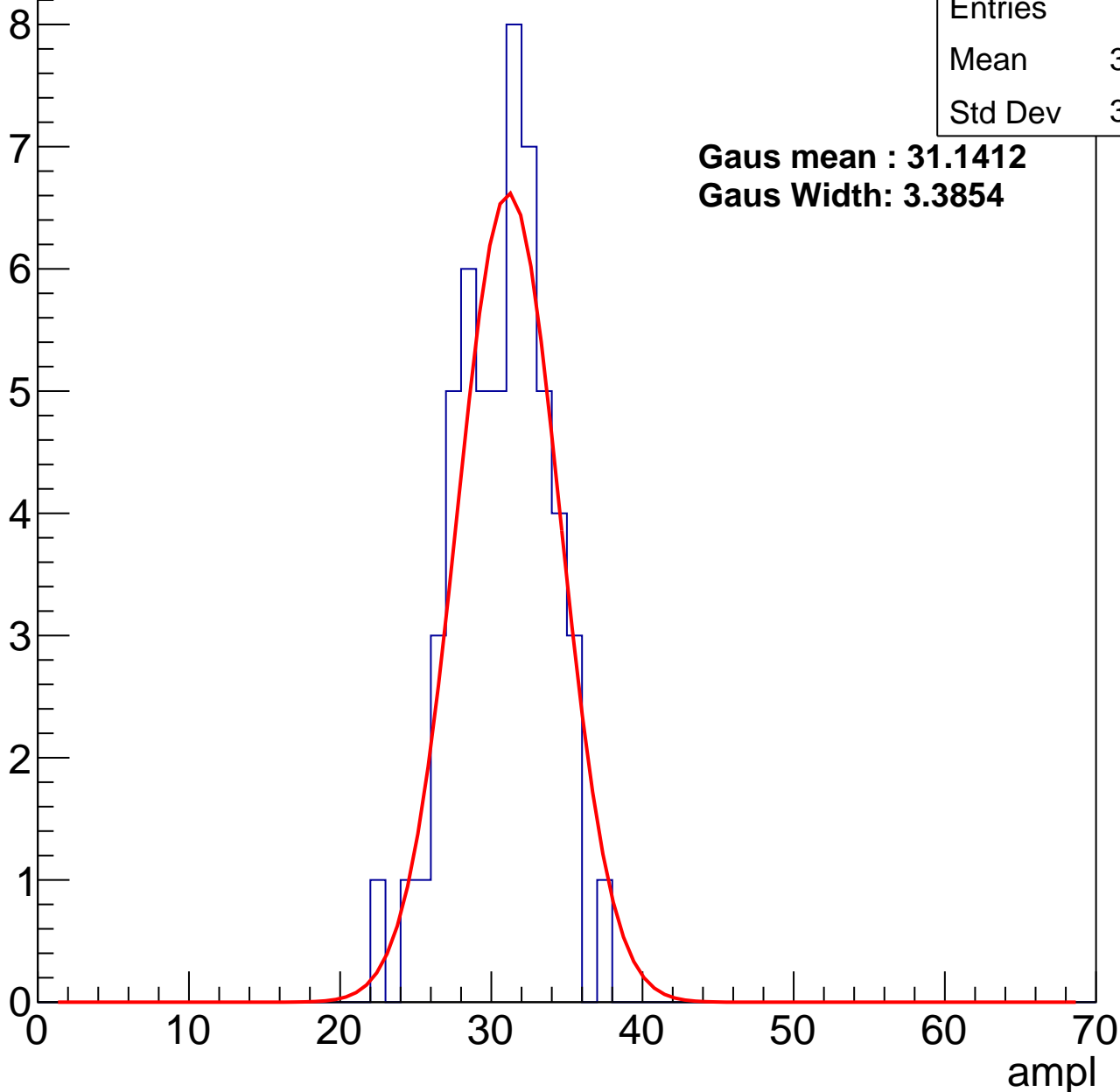
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	30.22
Std Dev	3.055

**Gaus mean : 31.1412**

**Gaus Width: 3.3854**



# B0L001S, U21-ch58, adc1

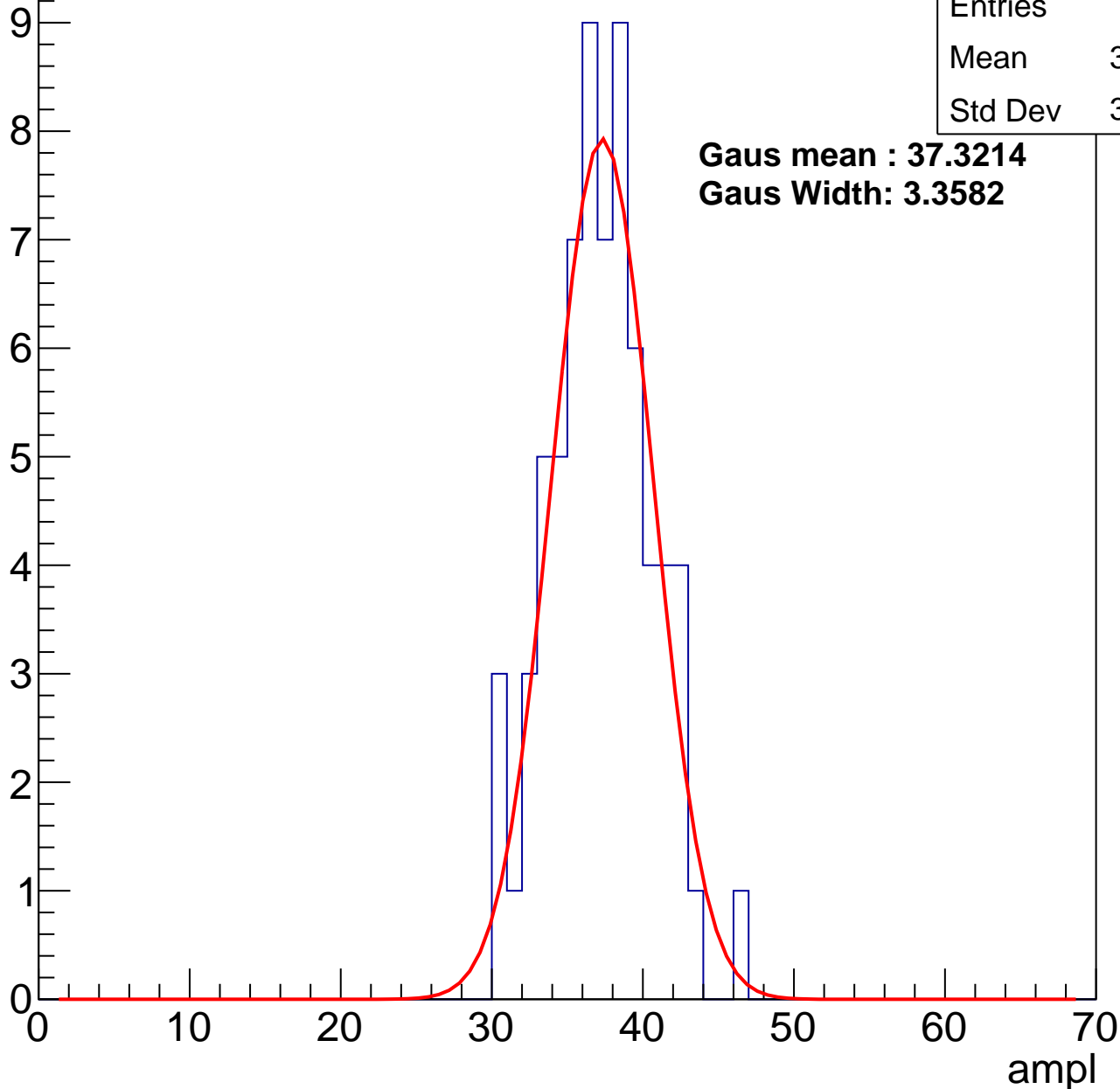
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	36.77
Std Dev	3.333

**Gaus mean : 37.3214**

**Gaus Width: 3.3582**



# B0L001S, U21-ch58, adc2

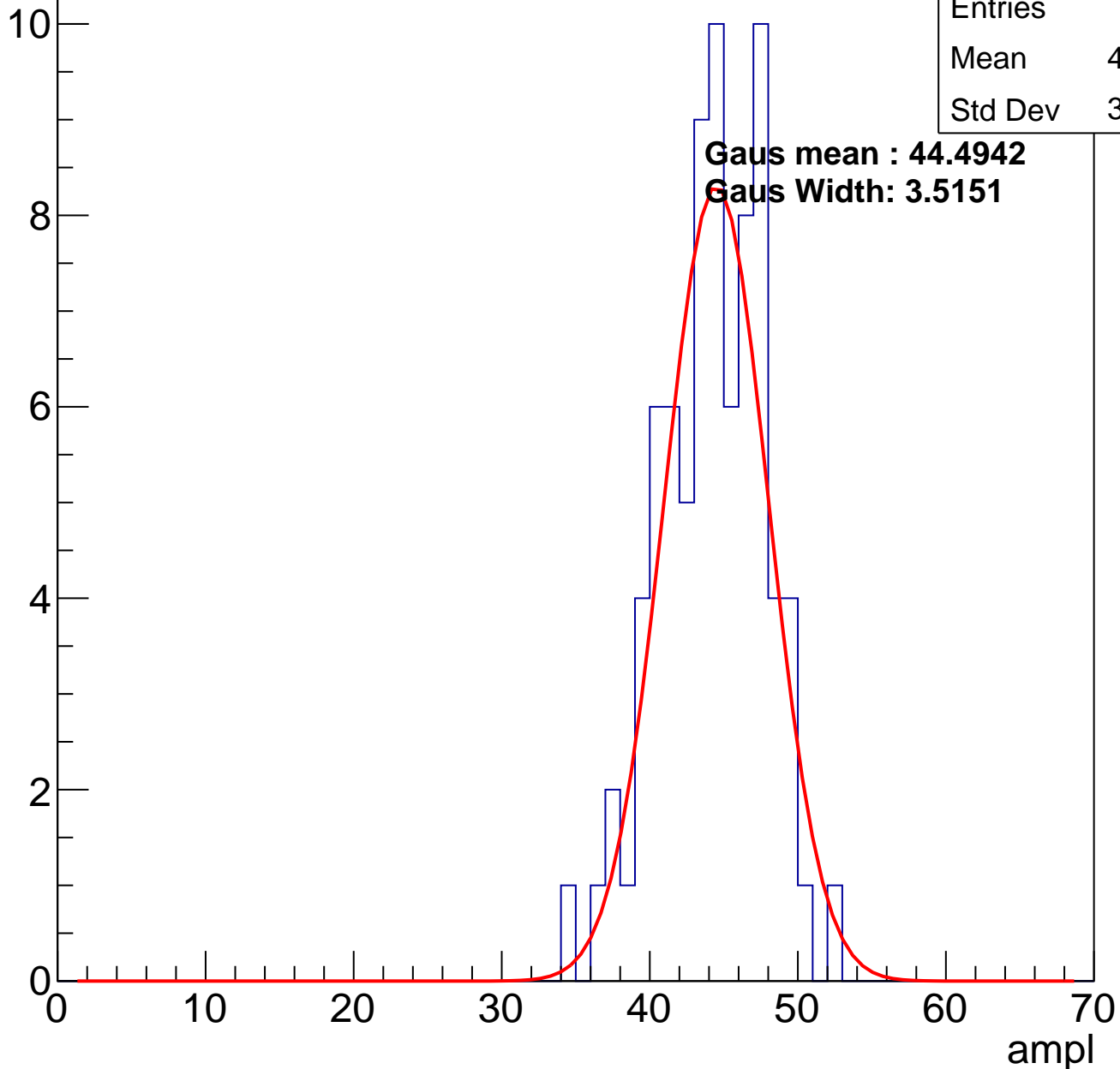
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	79
Mean	43.78
Std Dev	3.496

**Gaus mean : 44.4942**

**Gaus Width: 3.5151**

Entry

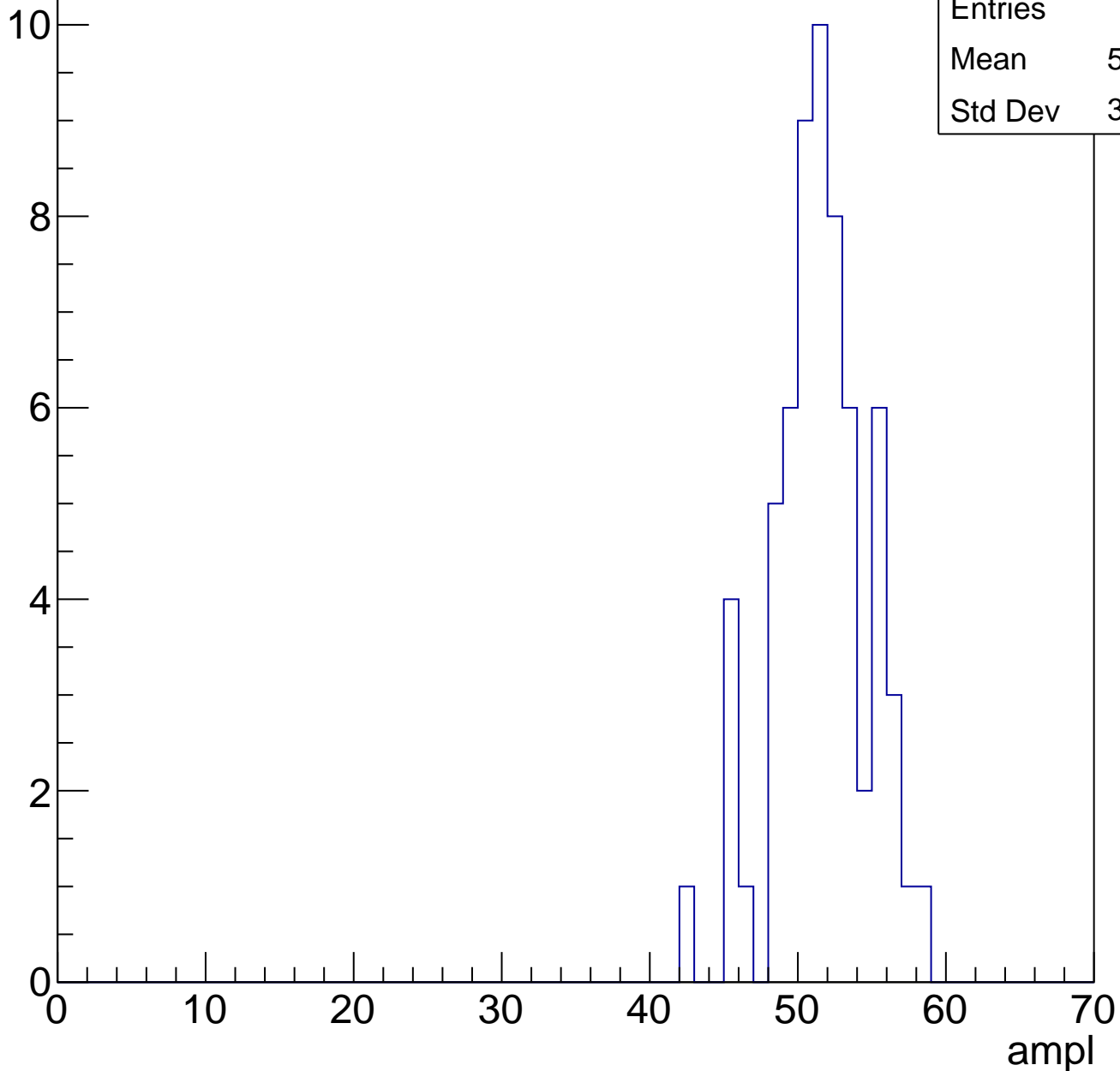


# B0L001S, U21-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	63
Mean	51.06
Std Dev	3.172

Entry

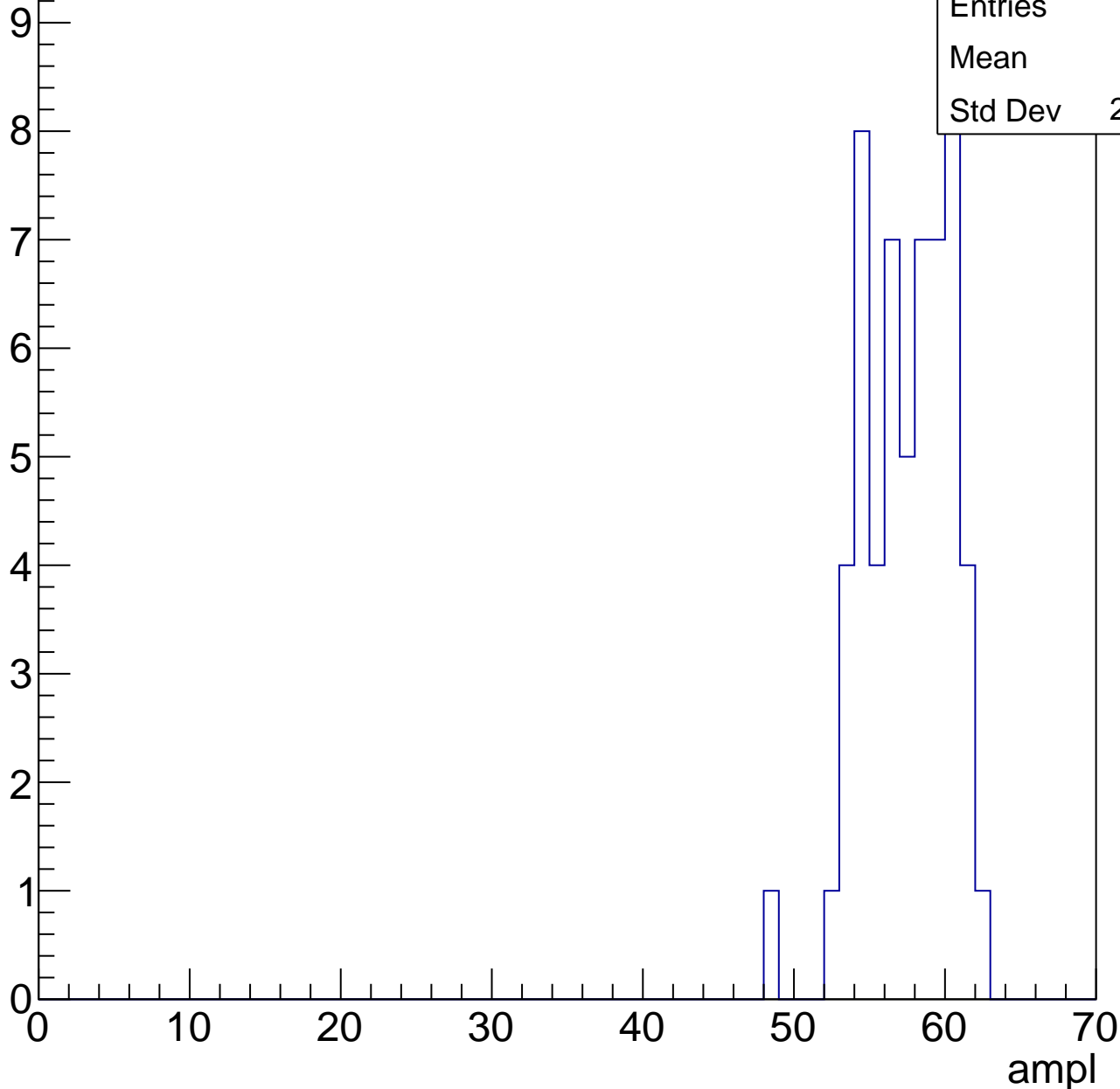


# B0L001S, U21-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	57
Std Dev	2.847

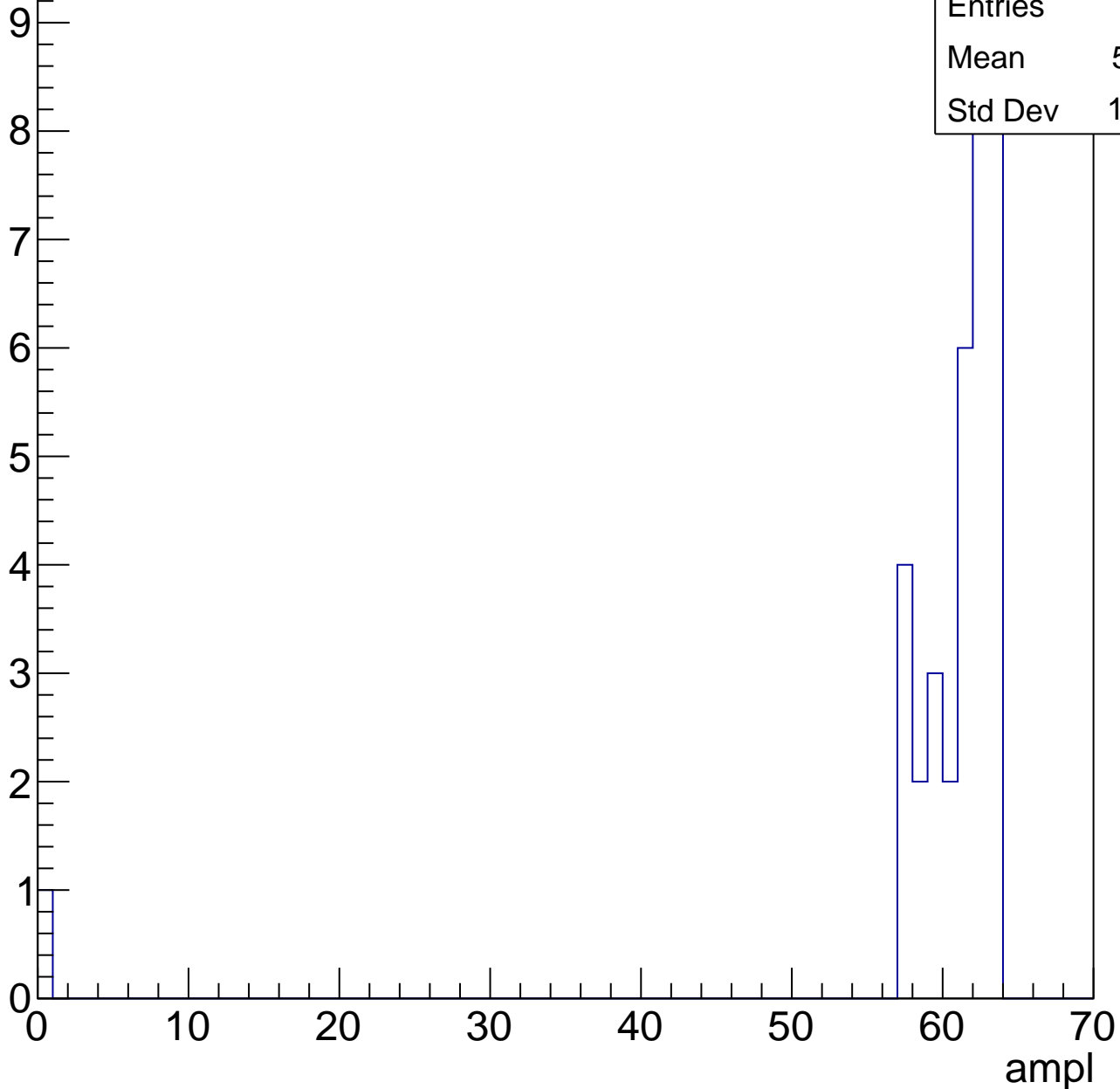


# B0L001S, U21-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	35
Mean	59.11
Std Dev	10.33



# B0L001S, U21-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

ampl



# B0L001S, U21-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch59, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	68
Mean	30.18
Std Dev	4.786

**Gaus mean : 30.9783**

**Gaus Width: 3.1158**

Entry

10

8

6

4

2

0

0

10

20

30

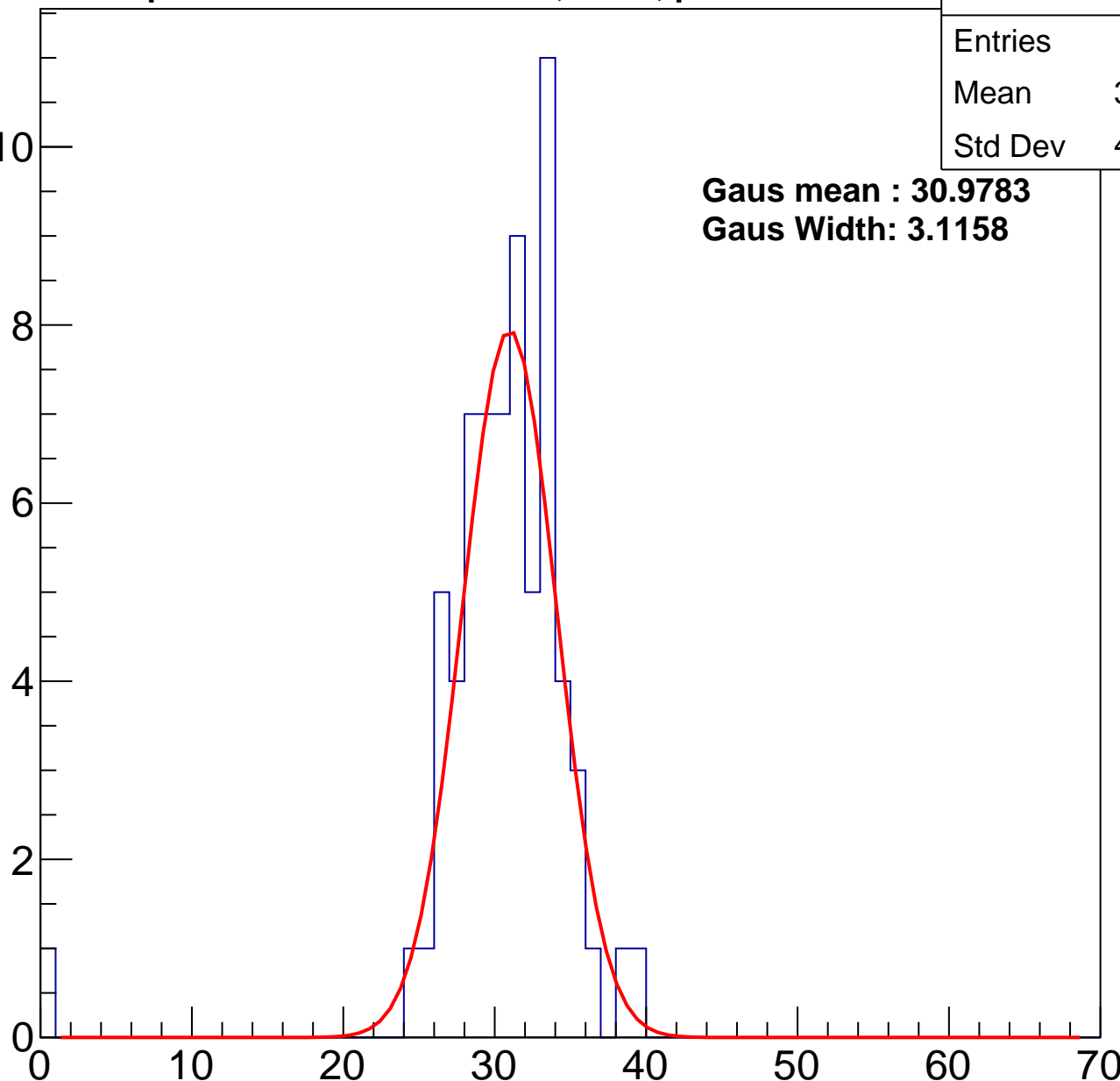
40

50

60

70

ampl



# B0L001S, U21-ch59, adc1

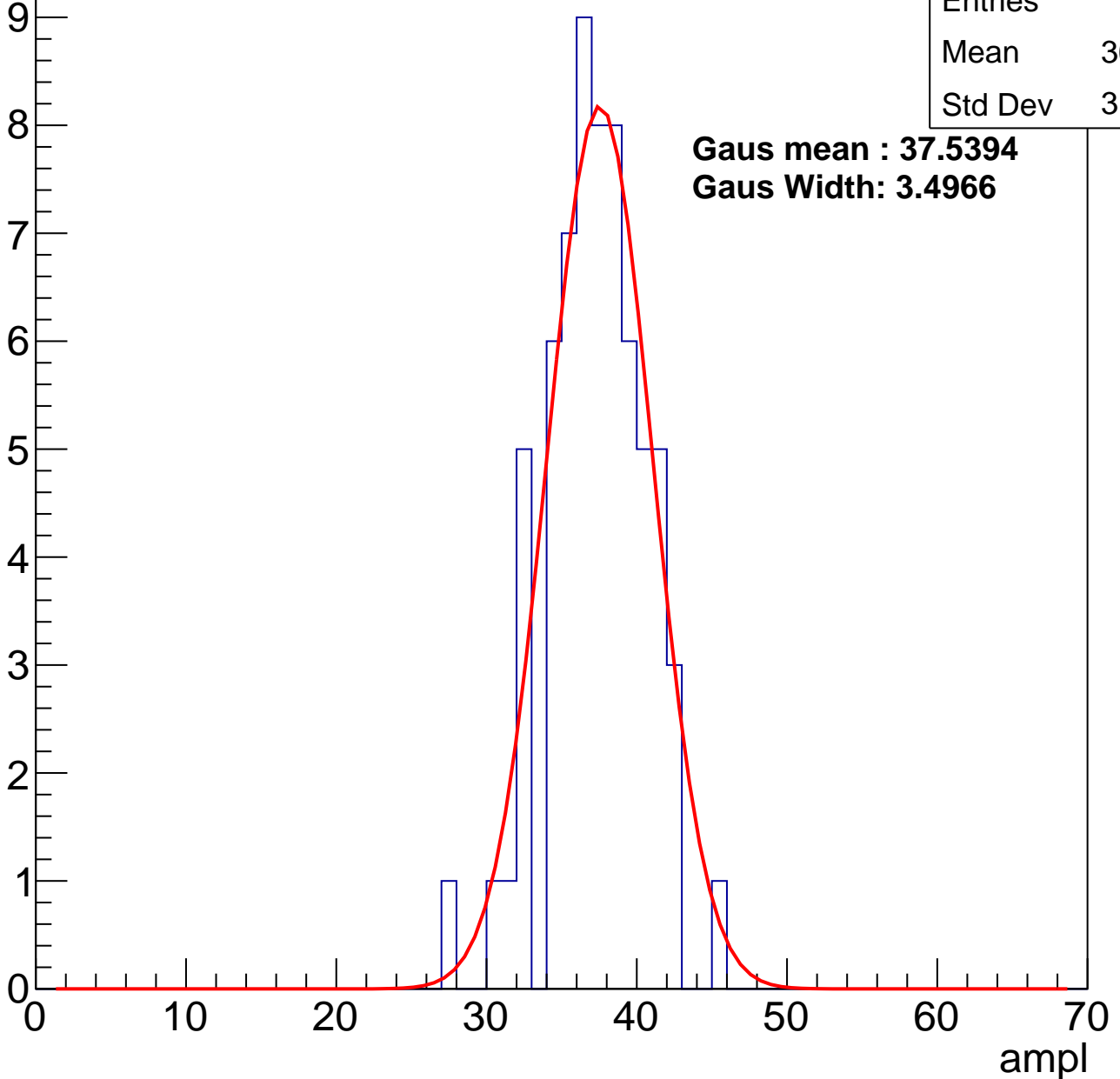
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	36.83
Std Dev	3.245

**Gaus mean : 37.5394**

**Gaus Width: 3.4966**



# B0L001S, U21-ch59, adc2

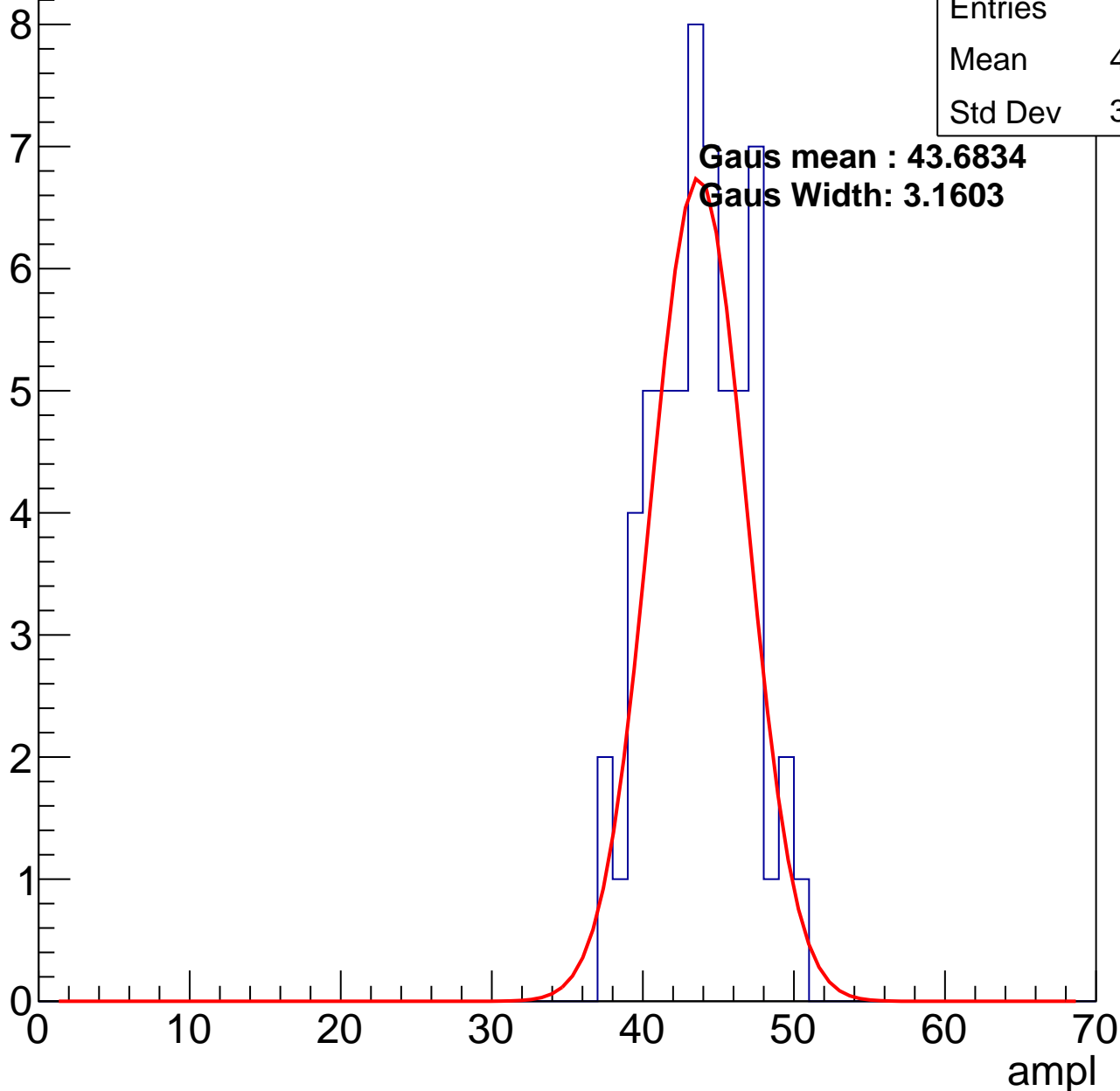
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	43.36
Std Dev	3.089

**Gaus mean : 43.6834**

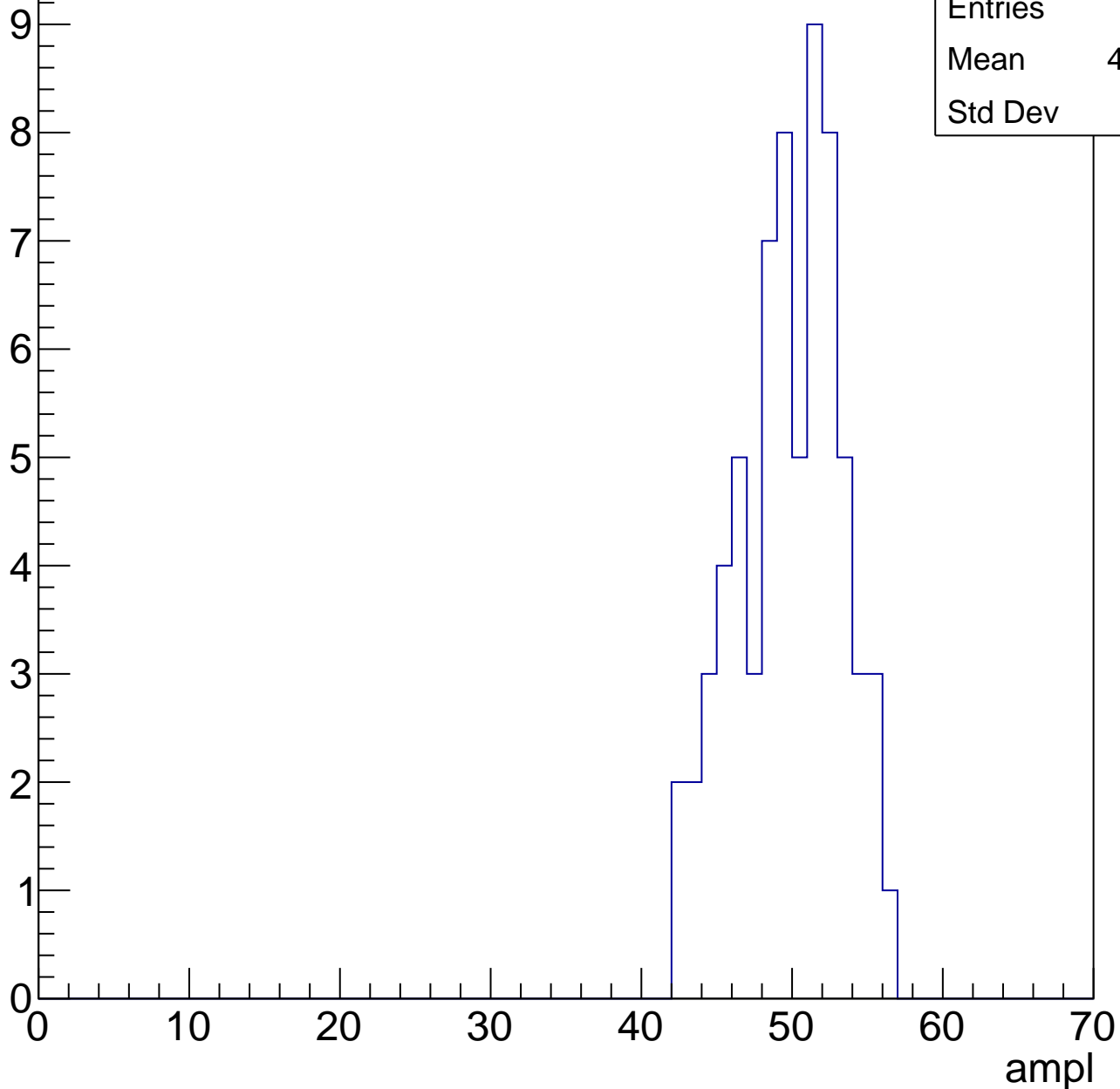
**Gaus Width: 3.1603**



# B0L001S, U21-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

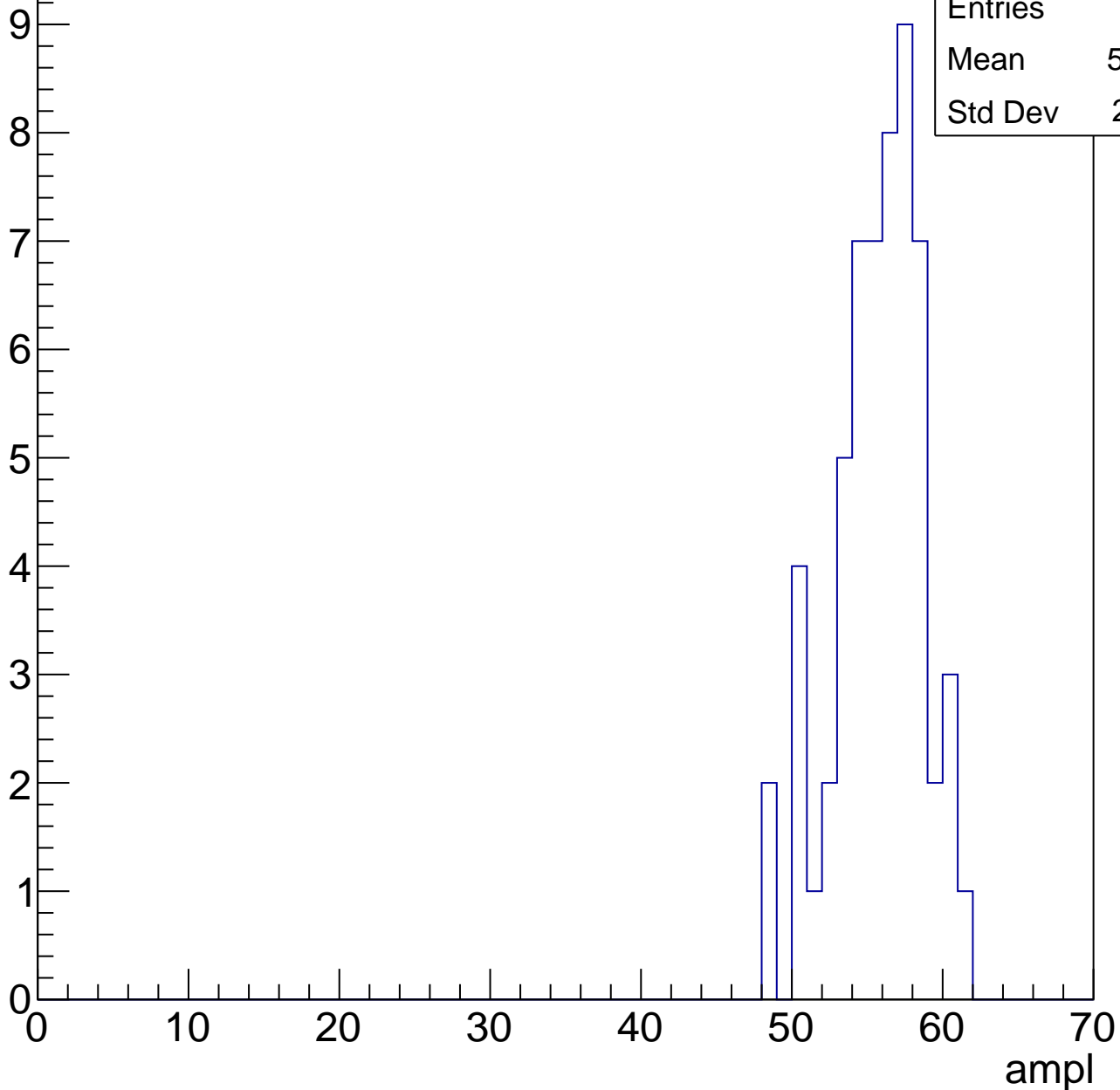


# B0L001S, U21-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	55.26
Std Dev	2.951



# B0L001S, U21-ch59, adc5

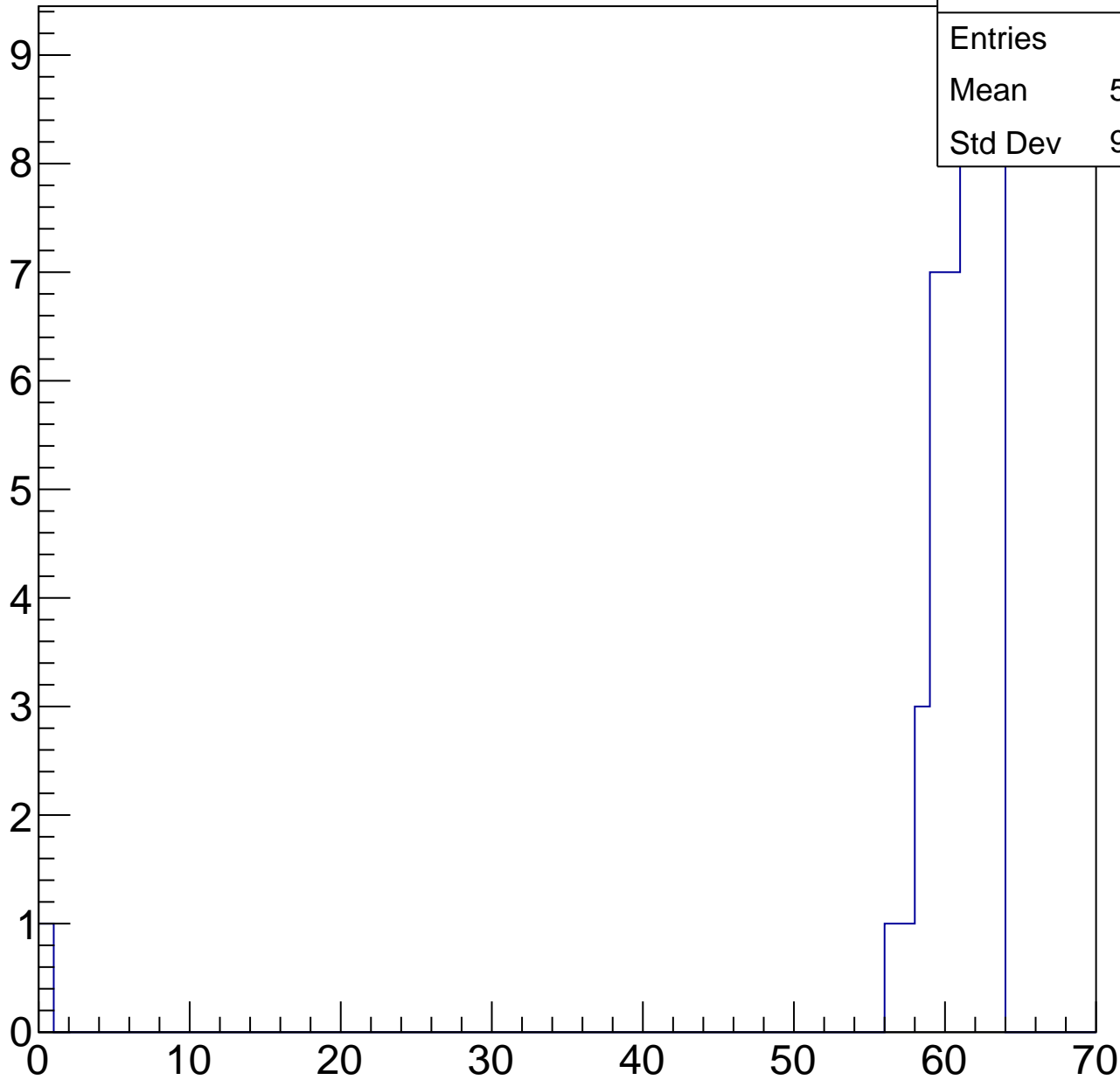
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	45
Mean	59.33
Std Dev	9.117

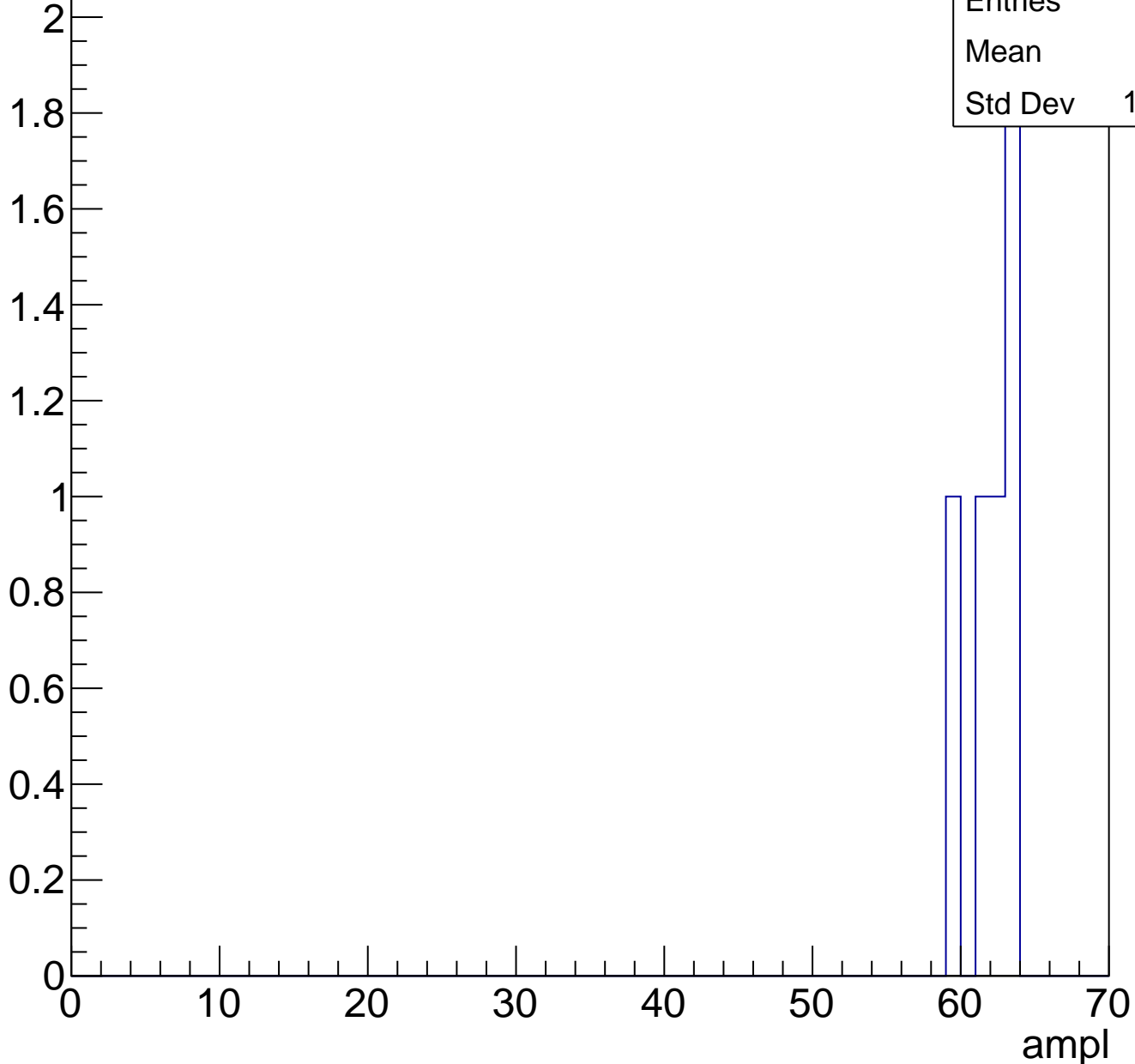
ampl



# B0L001S, U21-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch60, adc0

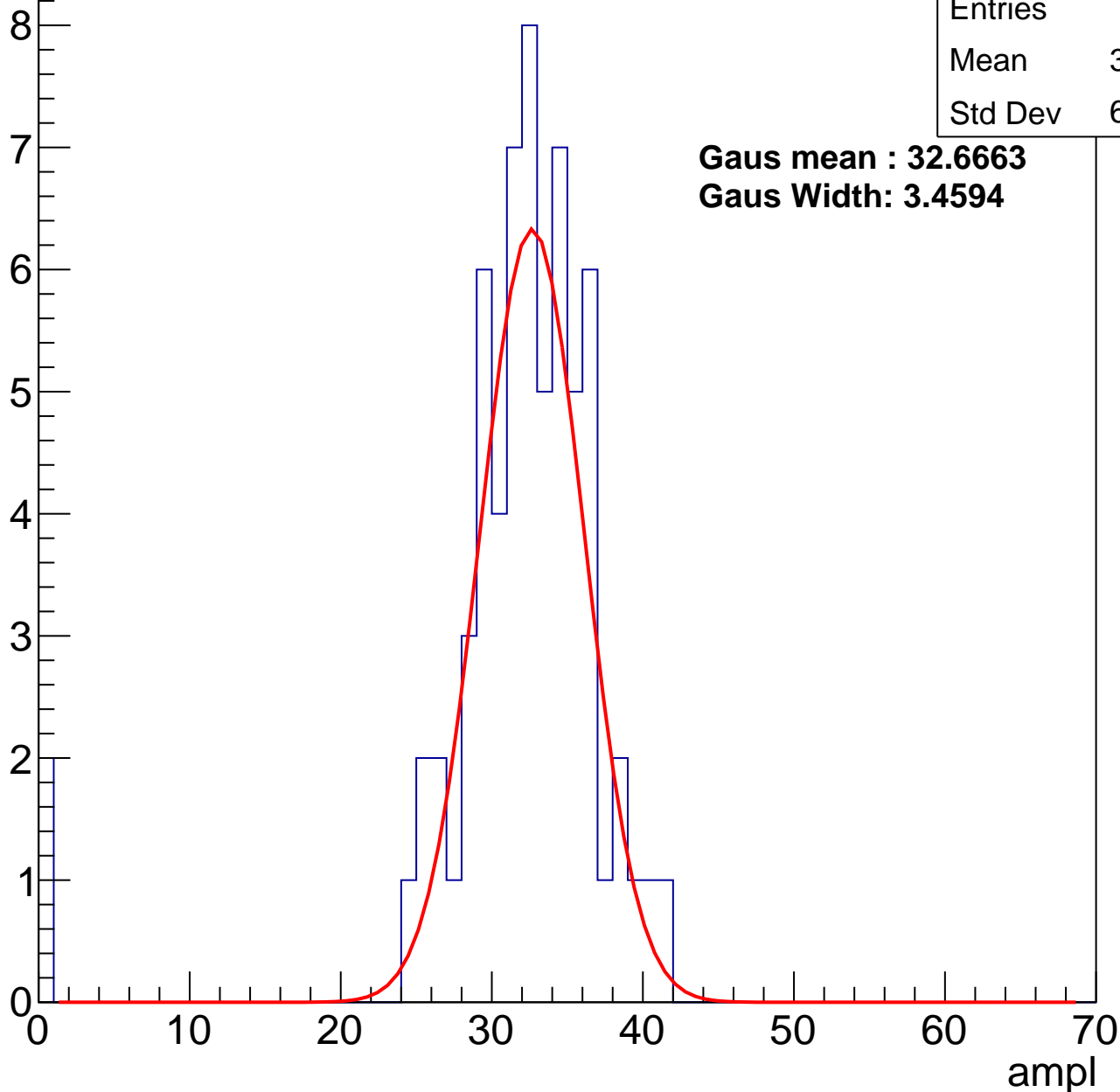
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	31.25
Std Dev	6.633

**Gaus mean : 32.6663**

**Gaus Width: 3.4594**



# B0L001S, U21-ch60, adc1

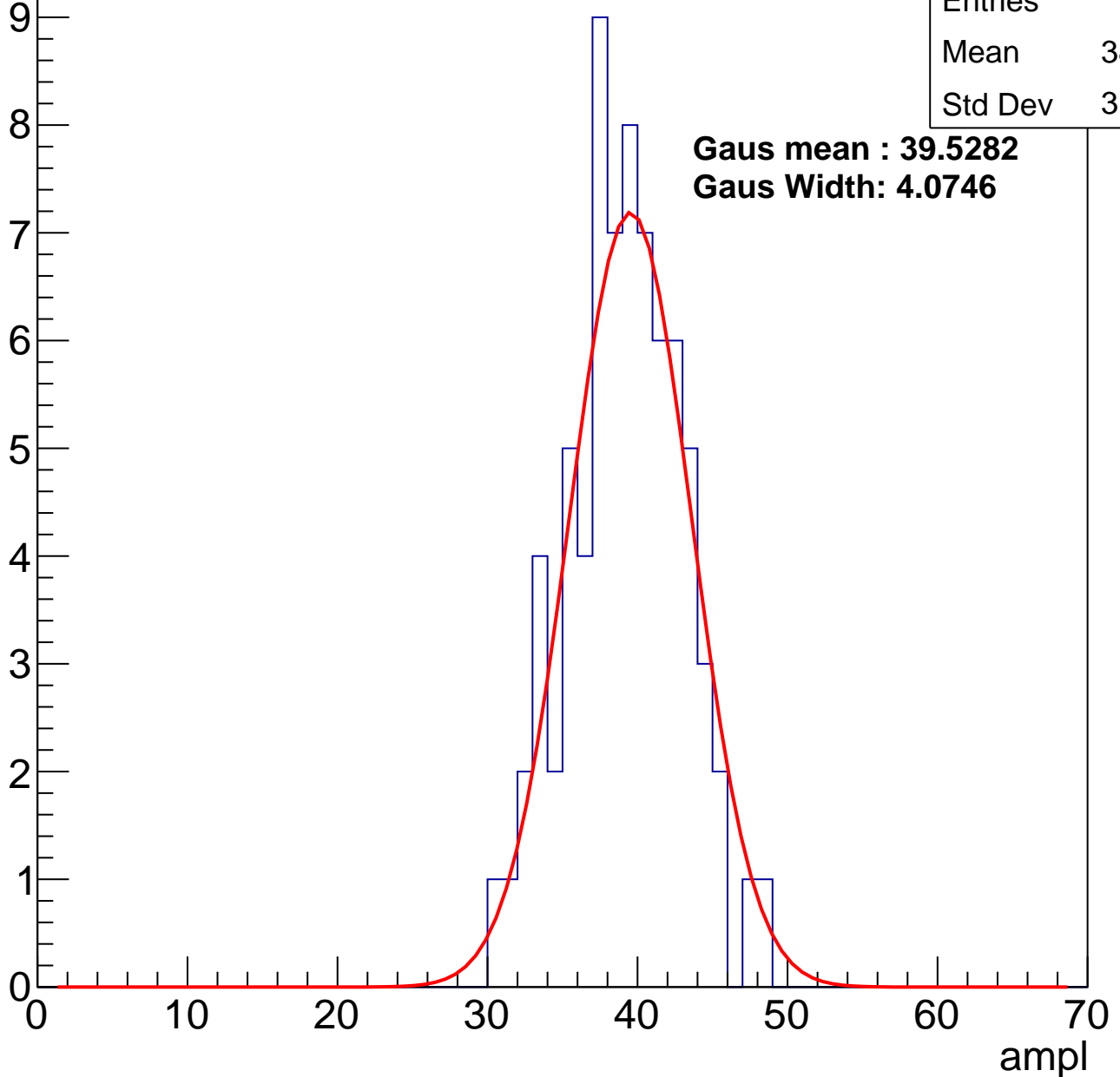
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	38.72
Std Dev	3.762

**Gaus mean : 39.5282**

**Gaus Width: 4.0746**



# B0L001S, U21-ch60, adc2

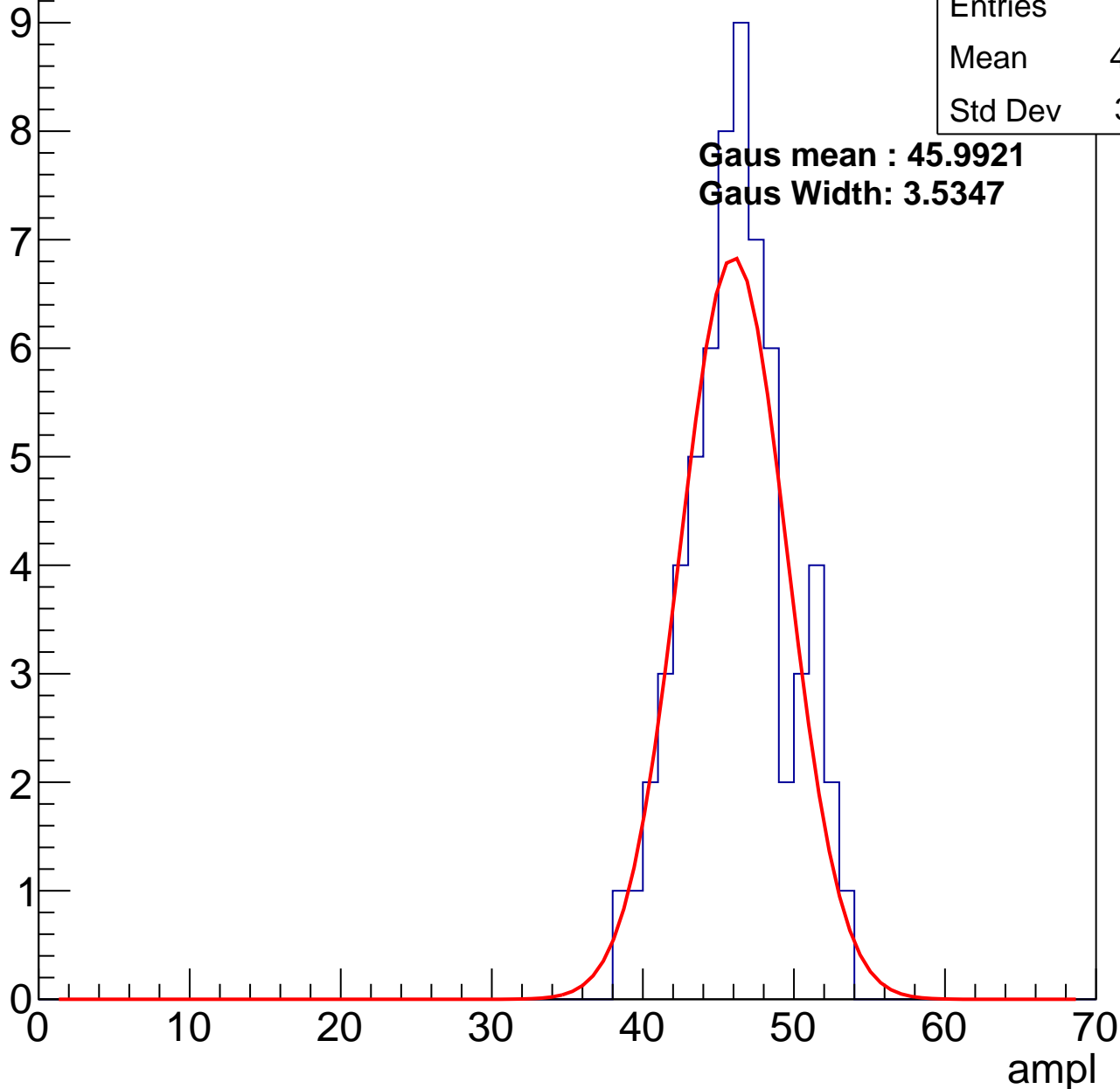
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	45.73
Std Dev	3.341

**Gaus mean : 45.9921**

**Gaus Width: 3.5347**

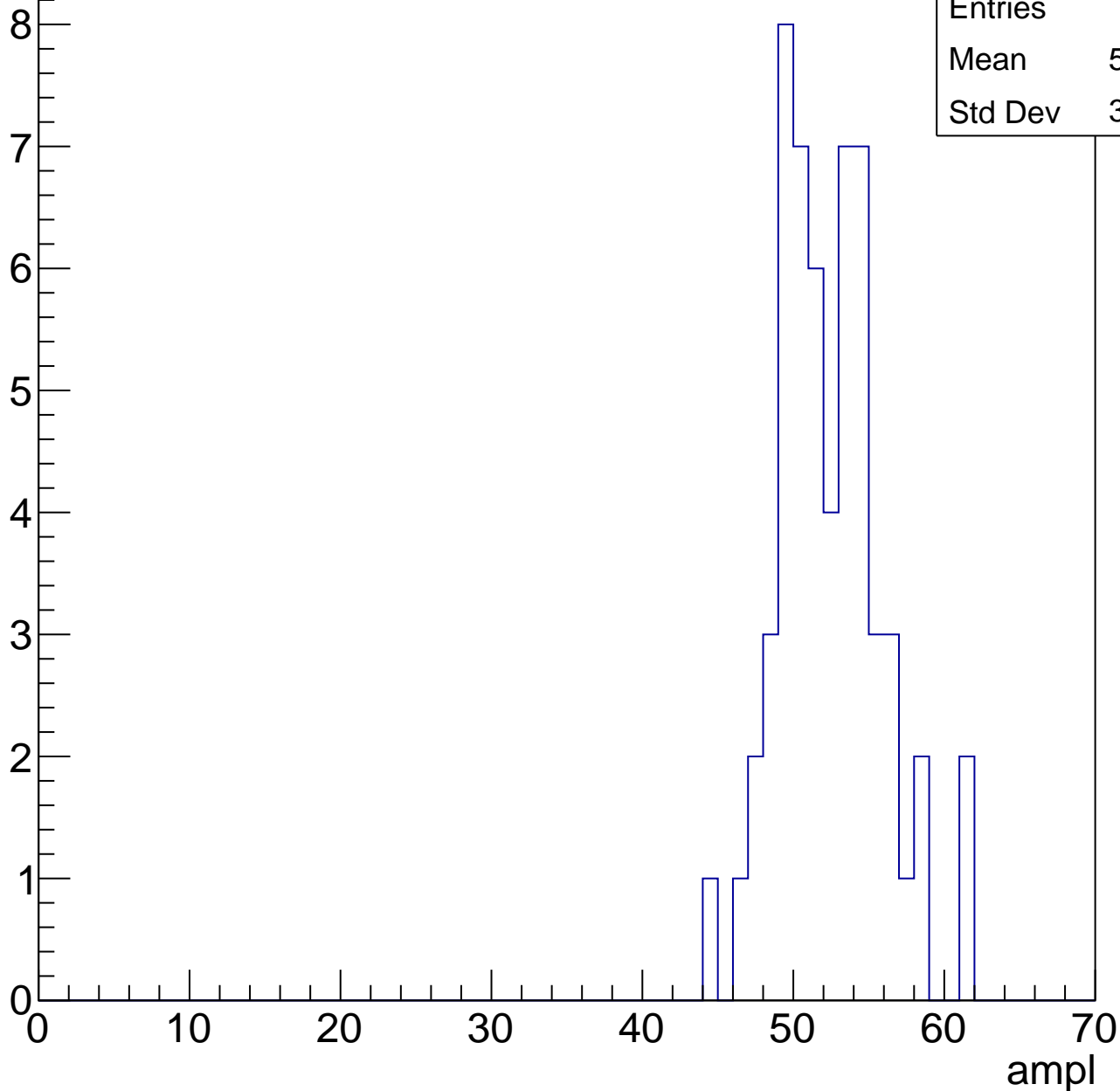


# B0L001S, U21-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

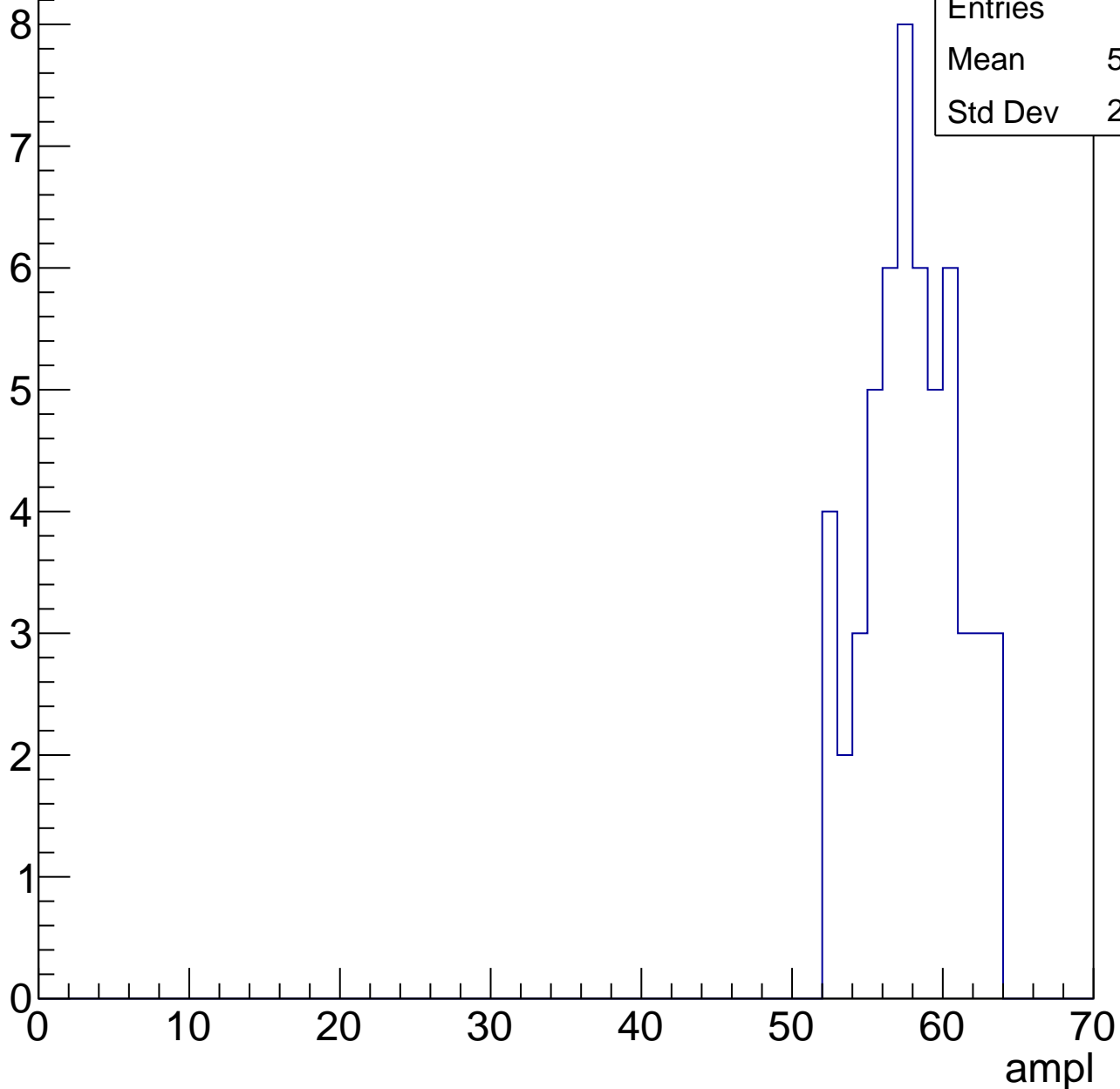
Entries	57
Mean	51.95
Std Dev	3.436



# B0L001S, U21-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



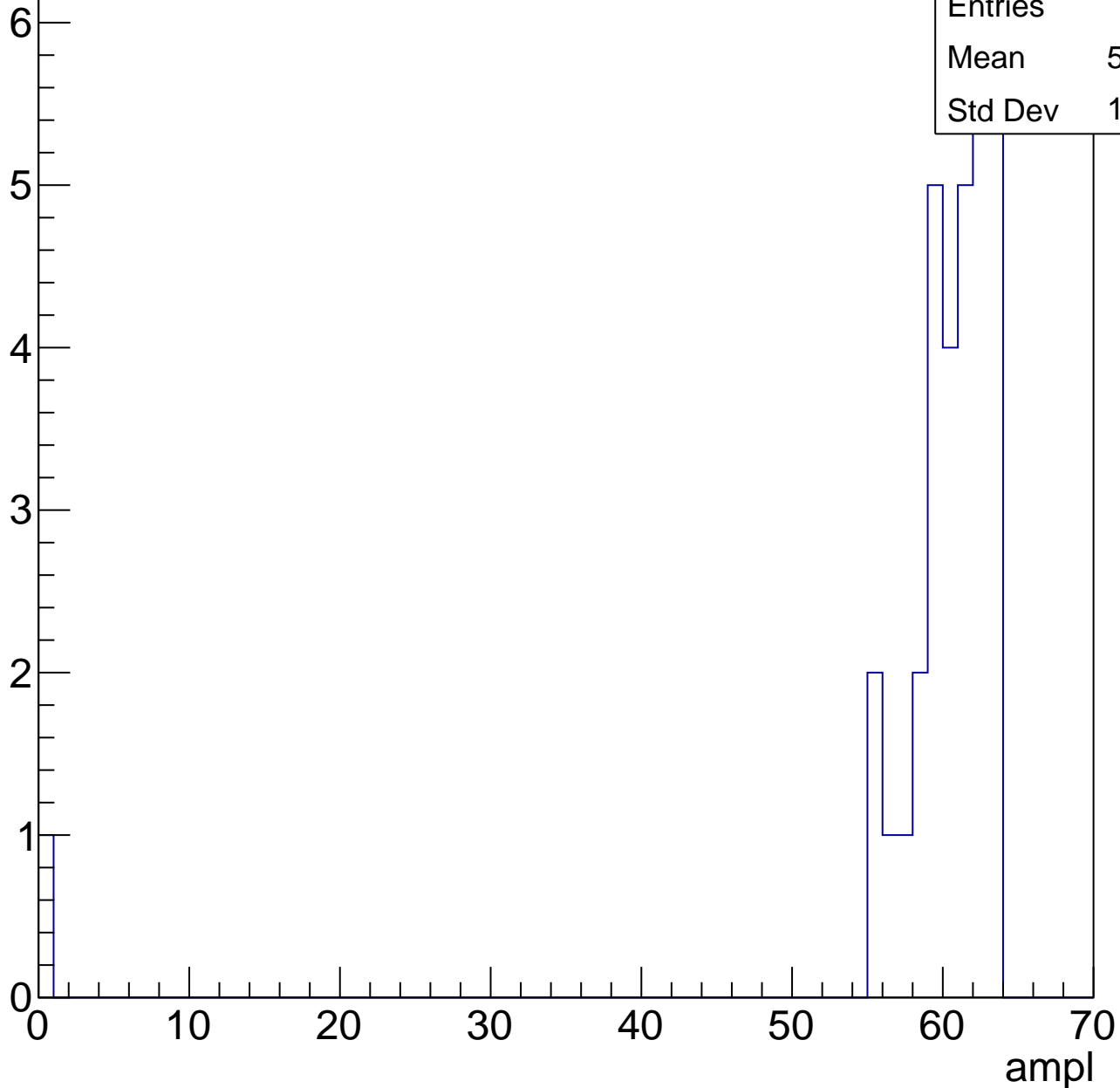
Entries	54
Mean	57.48
Std Dev	2.992

# B0L001S, U21-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	33
Mean	58.45
Std Dev	10.58



# B0L001S, U21-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U21-ch61, adc0

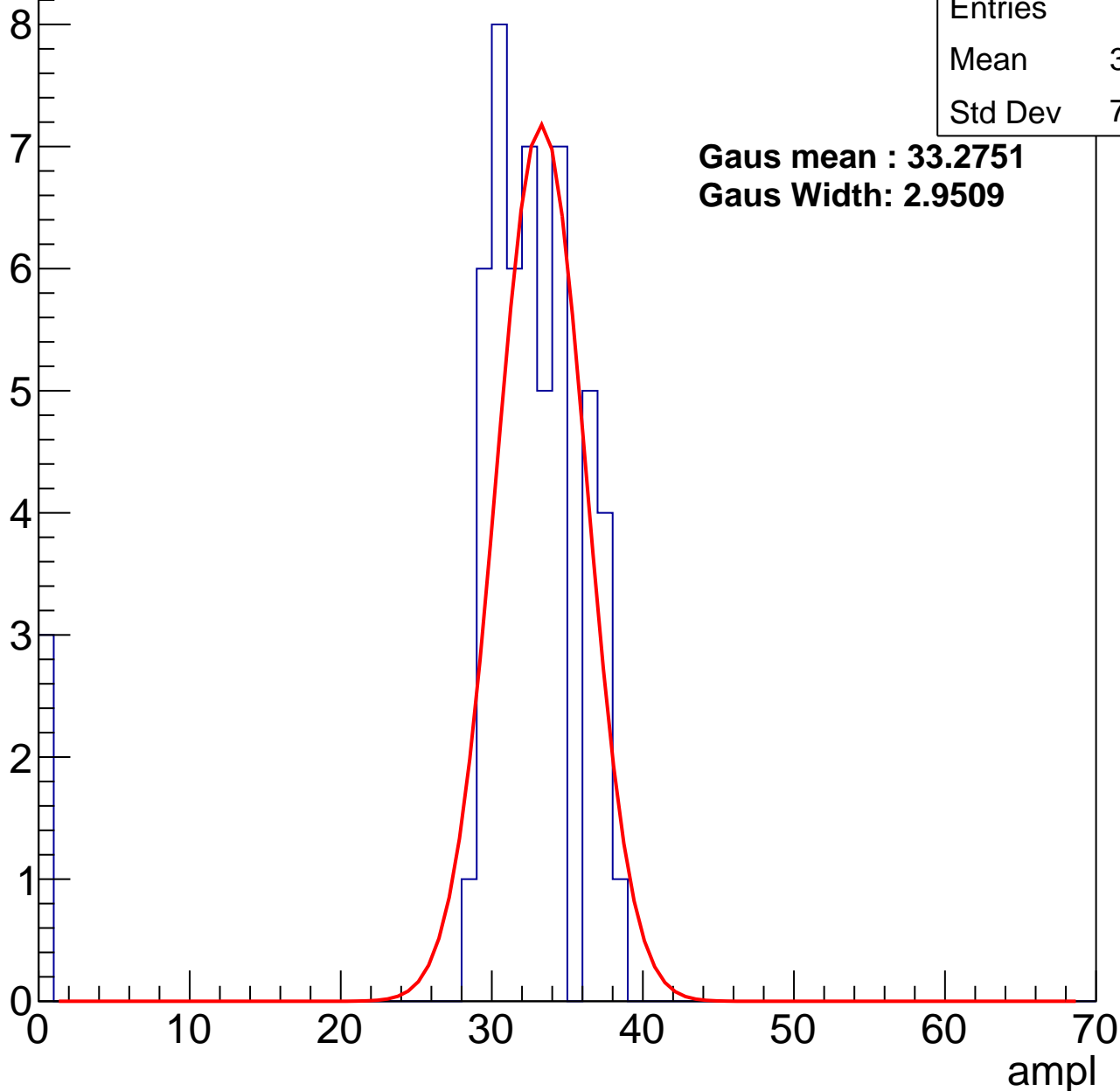
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	30.58
Std Dev	7.918

**Gaus mean : 33.2751**

**Gaus Width: 2.9509**

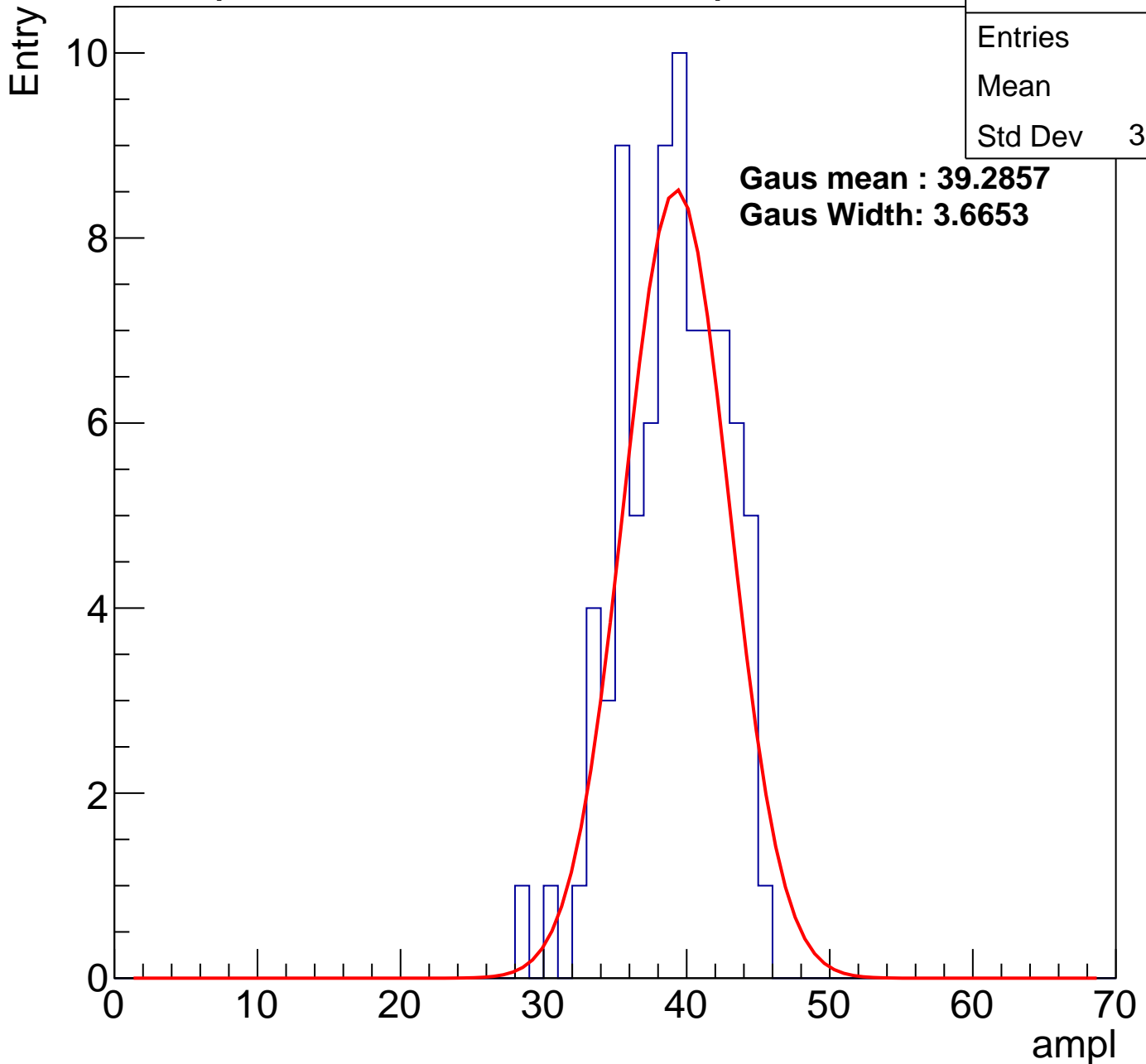


# B0L001S, U21-ch61, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	82
Mean	38.5
Std Dev	3.538

**Gaus mean : 39.2857**  
**Gaus Width: 3.6653**



# B0L001S, U21-ch61, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	68
Mean	46.4
Std Dev	3.232

**Gaus mean : 46.7905**

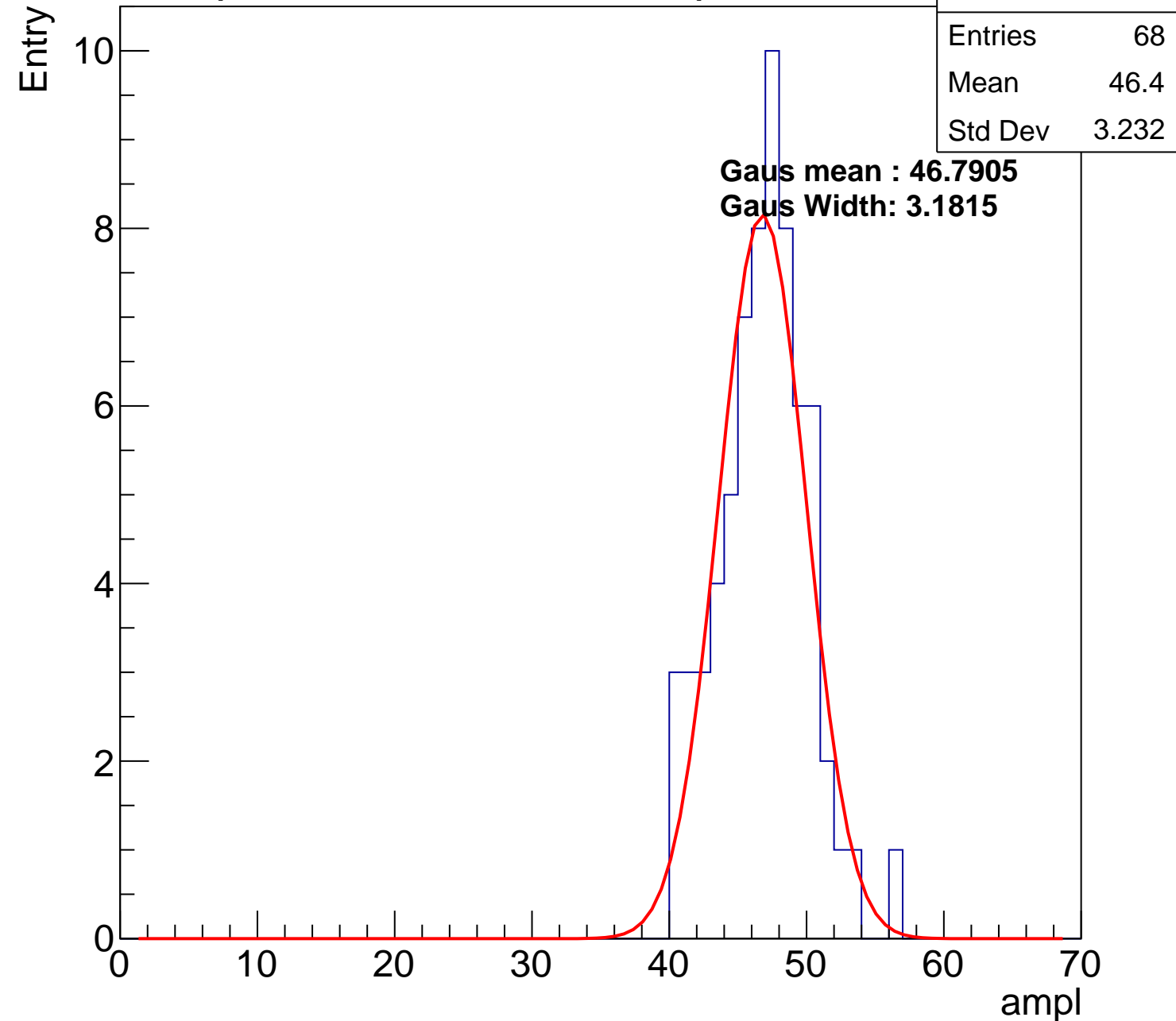
**Gaus Width: 3.1815**

Entry

10  
8  
6  
4  
2  
0

ampl

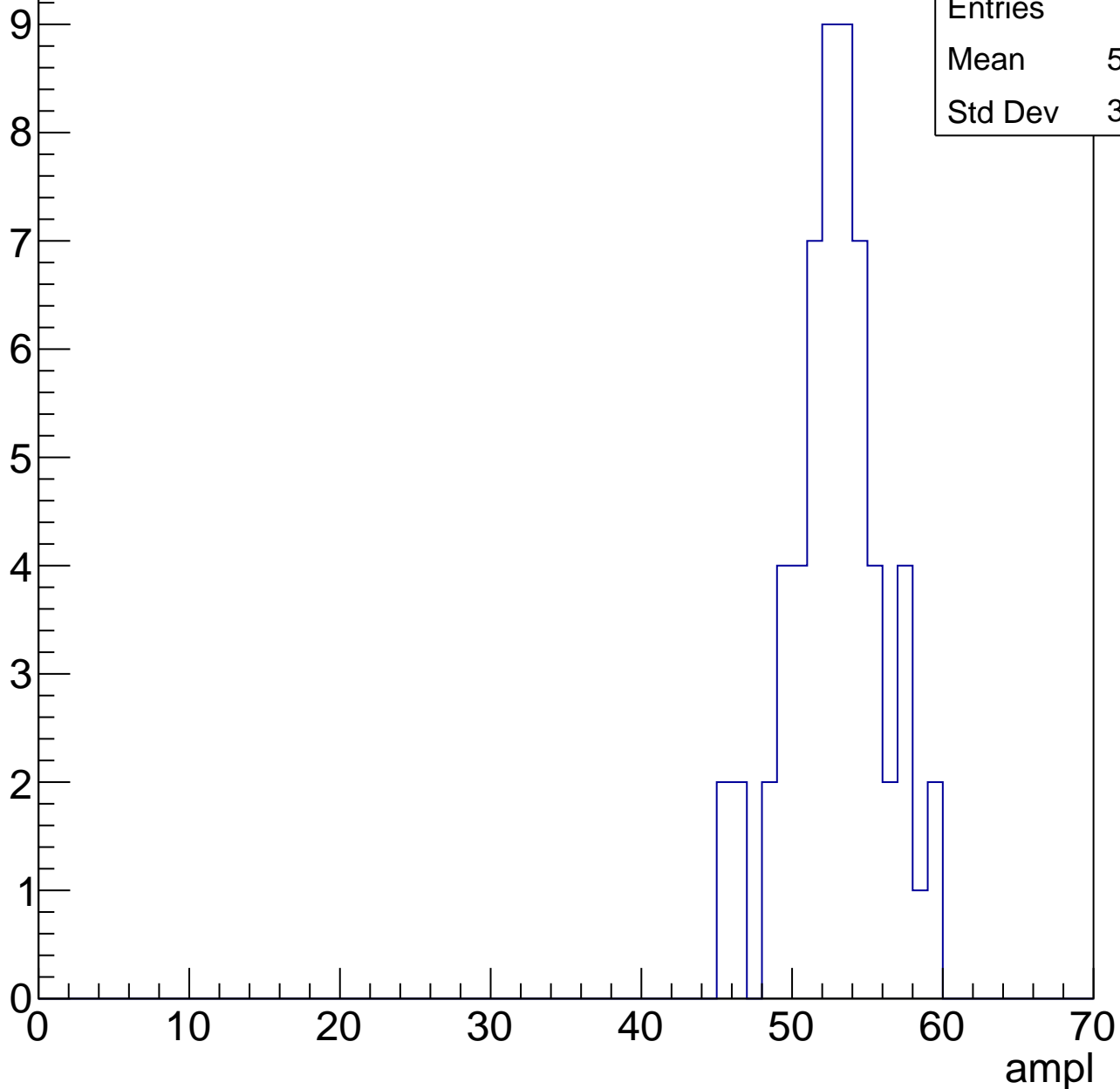
0 10 20 30 40 50 60 70



# B0L001S, U21-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	59
Mean	52.37
Std Dev	3.167

# B0L001S, U21-ch61, adc4

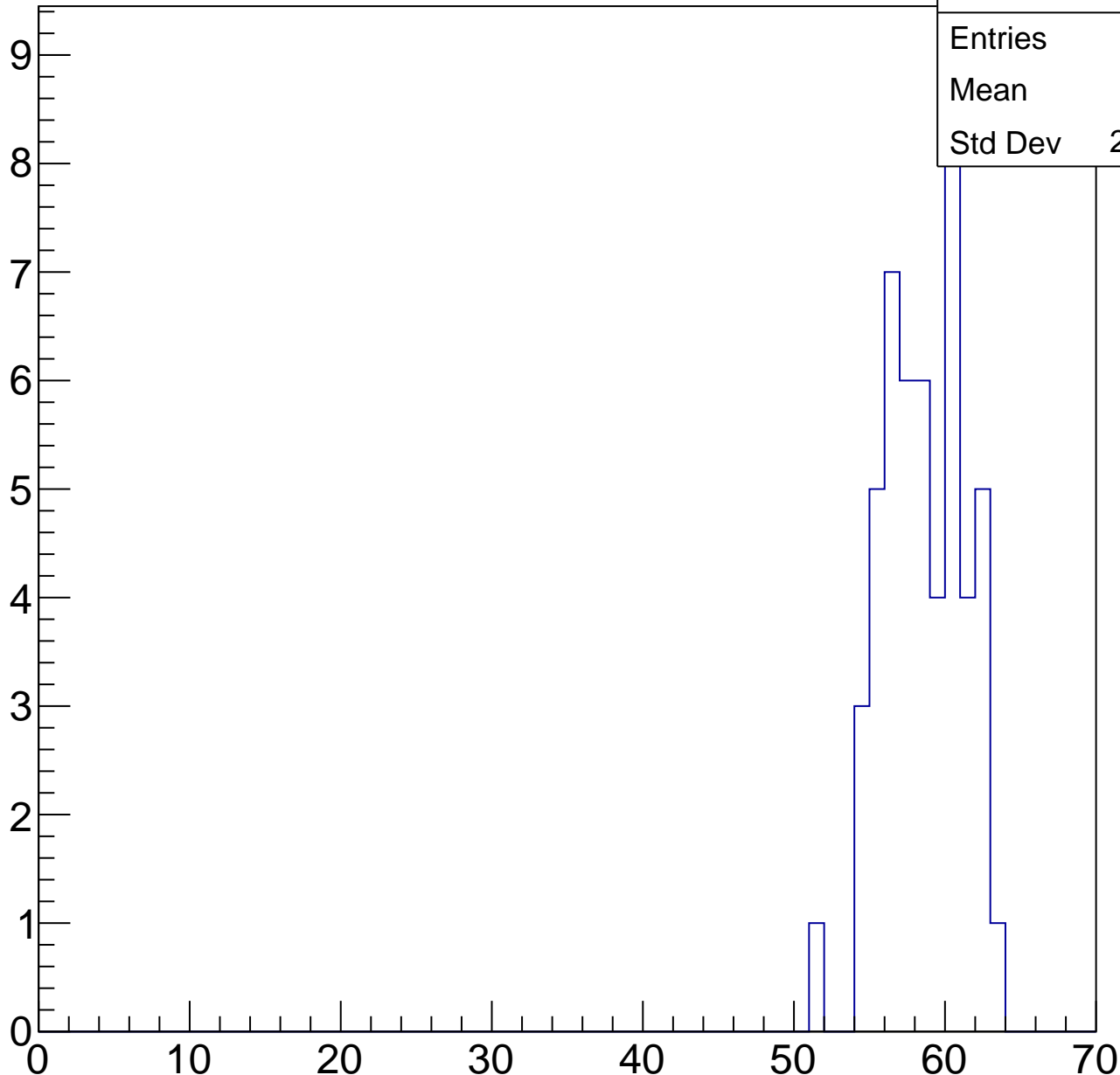
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	58.1
Std Dev	2.644

ampl

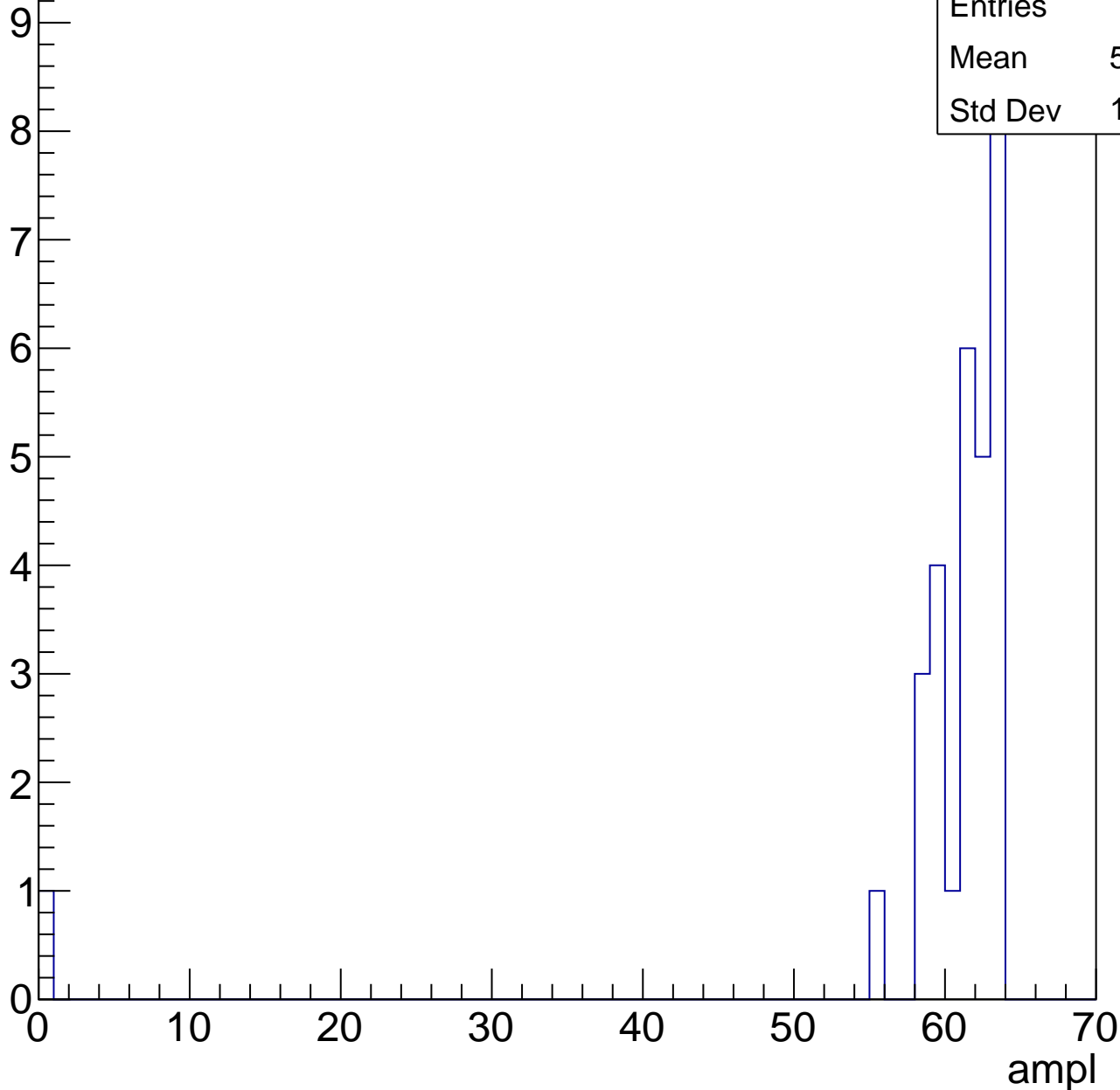


# B0L001S, U21-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	30
Mean	58.93
Std Dev	11.13



# B0L001S, U21-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U21-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L001S, U21-ch62, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	30.38
Std Dev	3.618

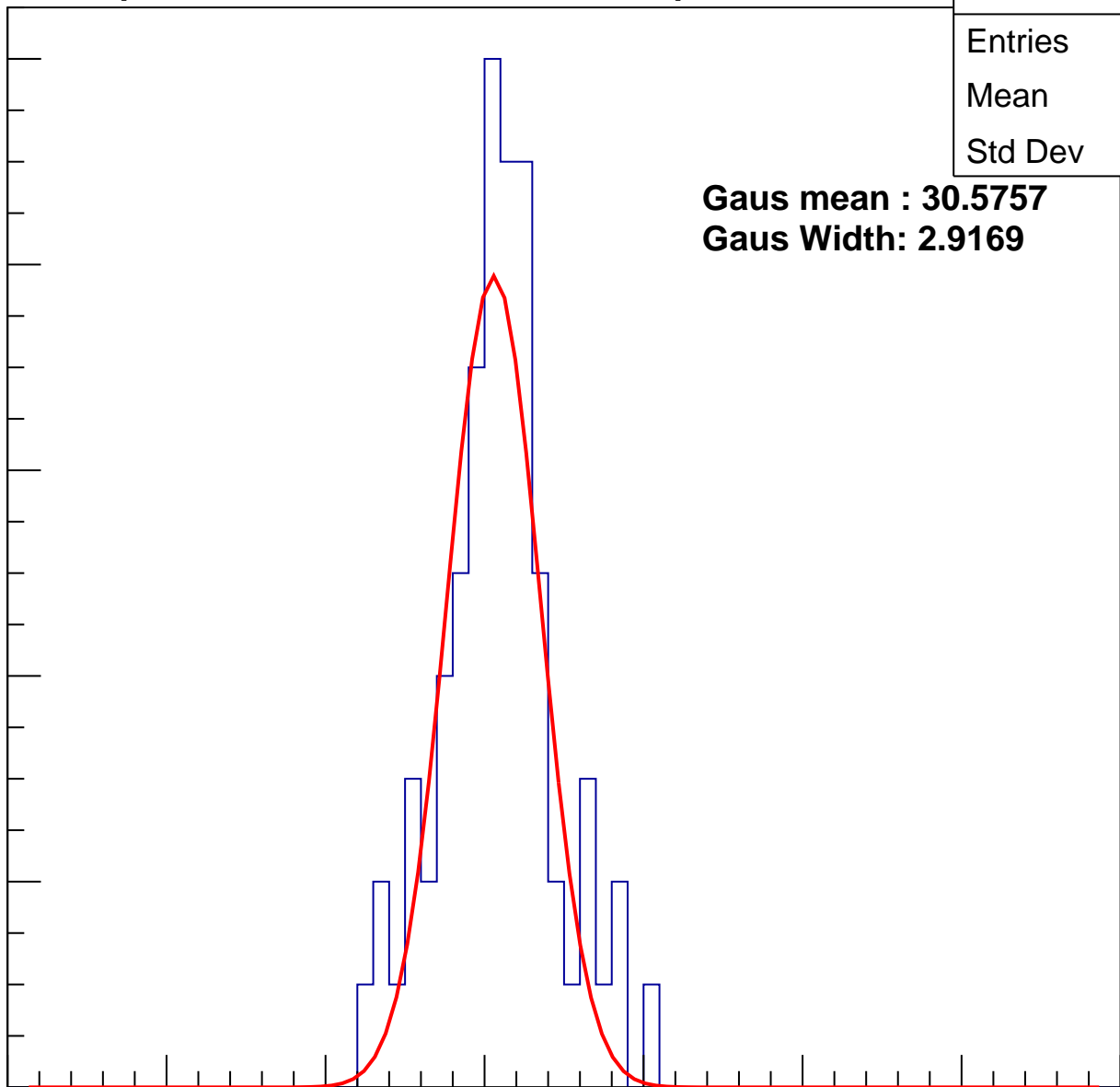
**Gaus mean : 30.5757**

**Gaus Width: 2.9169**

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



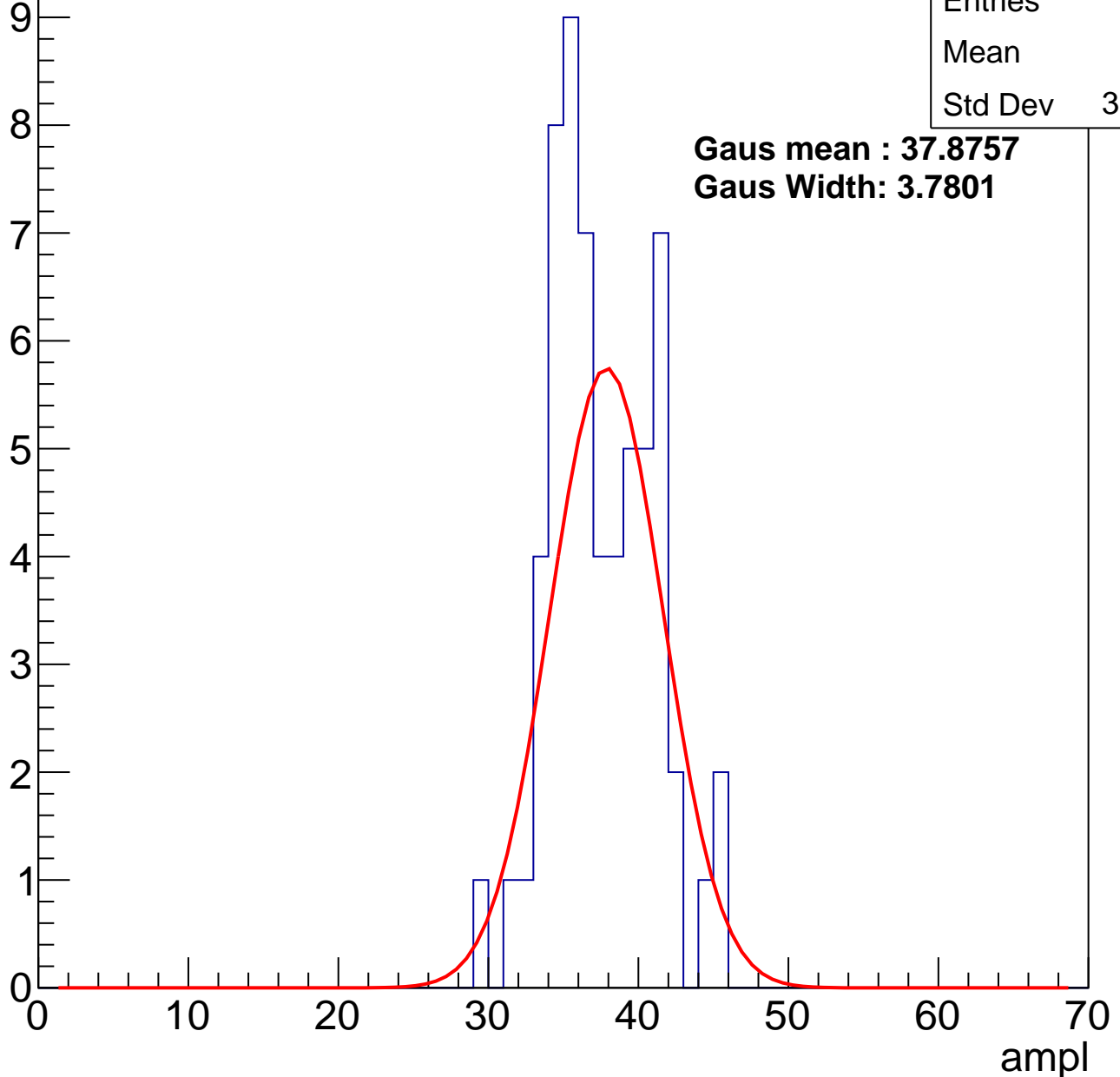
# B0L001S, U21-ch62, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	37.1
Std Dev	3.415

**Gaus mean : 37.8757**  
**Gaus Width: 3.7801**



# B0L001S, U21-ch62, adc2

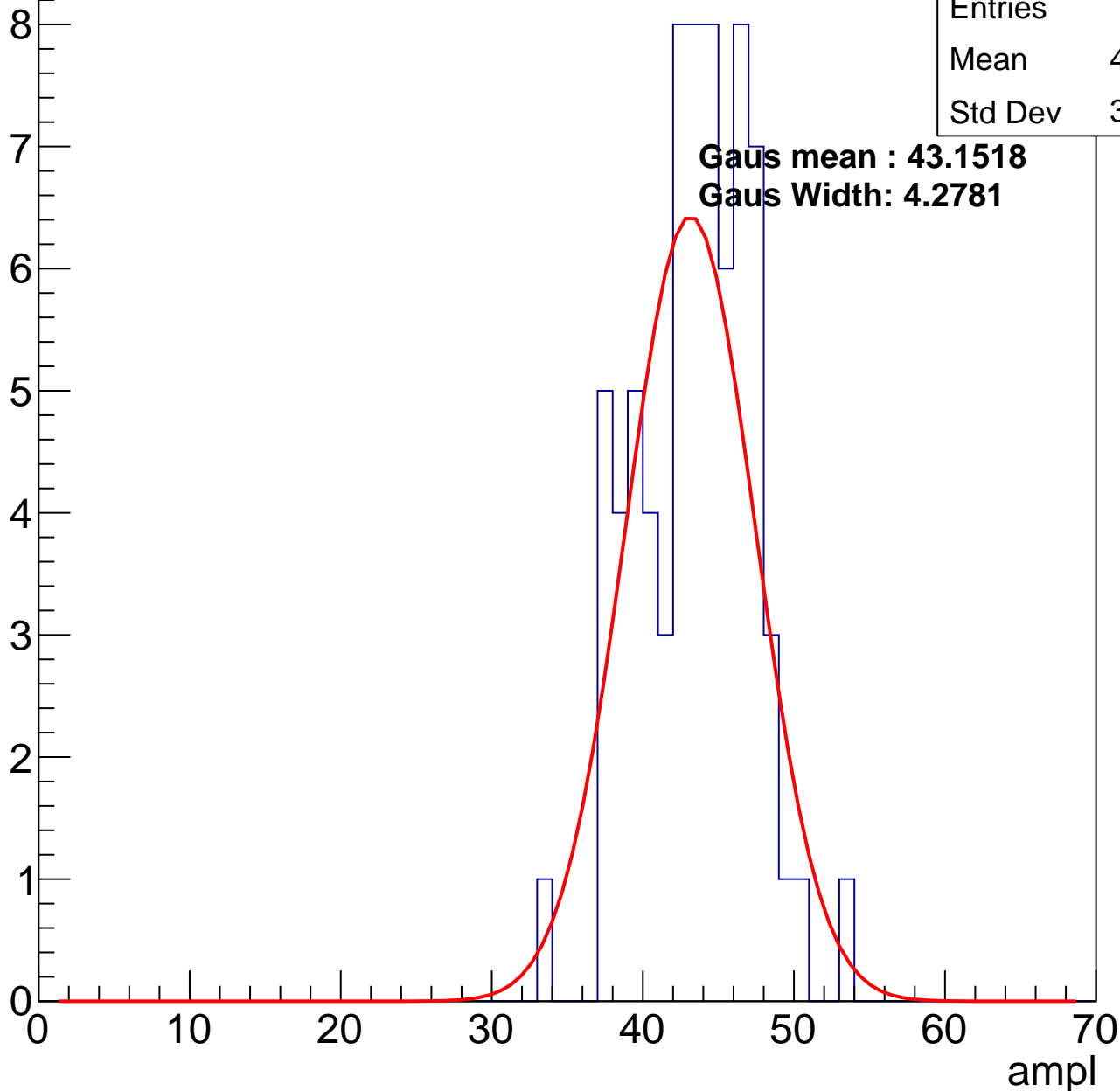
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	43.05
Std Dev	3.686

**Gaus mean : 43.1518**

**Gaus Width: 4.2781**

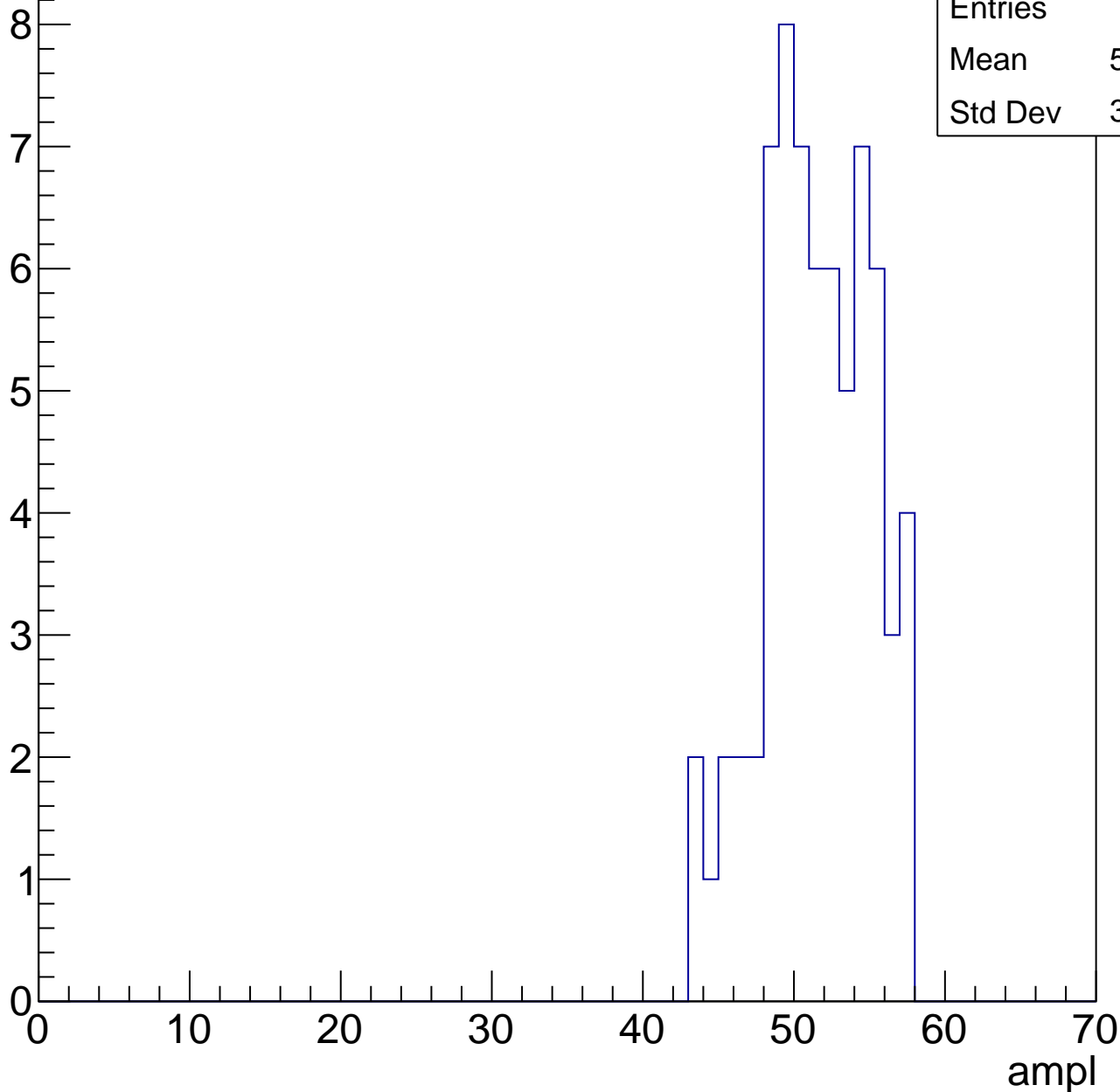


# B0L001S, U21-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	51.04
Std Dev	3.508

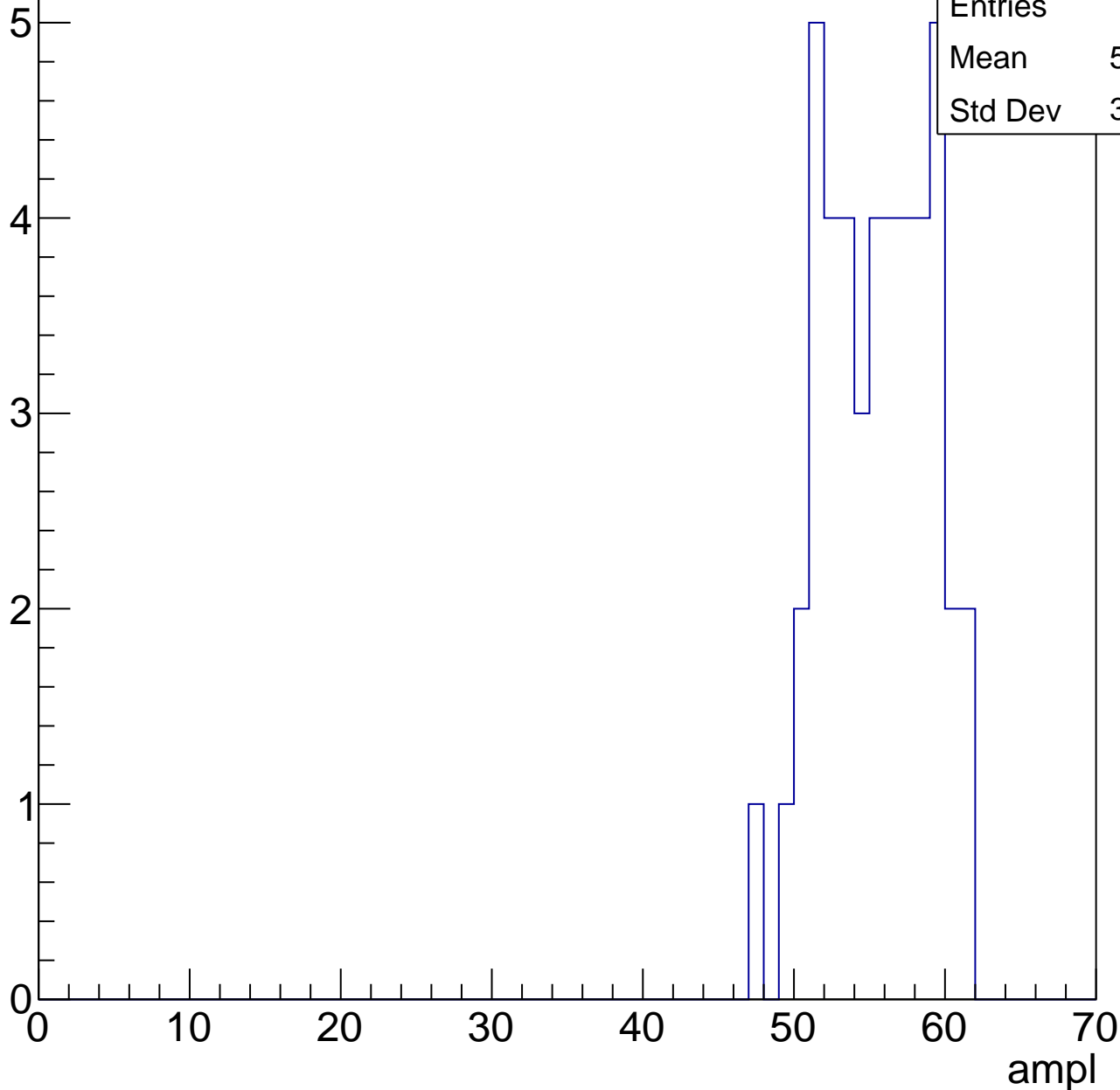


# B0L001S, U21-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

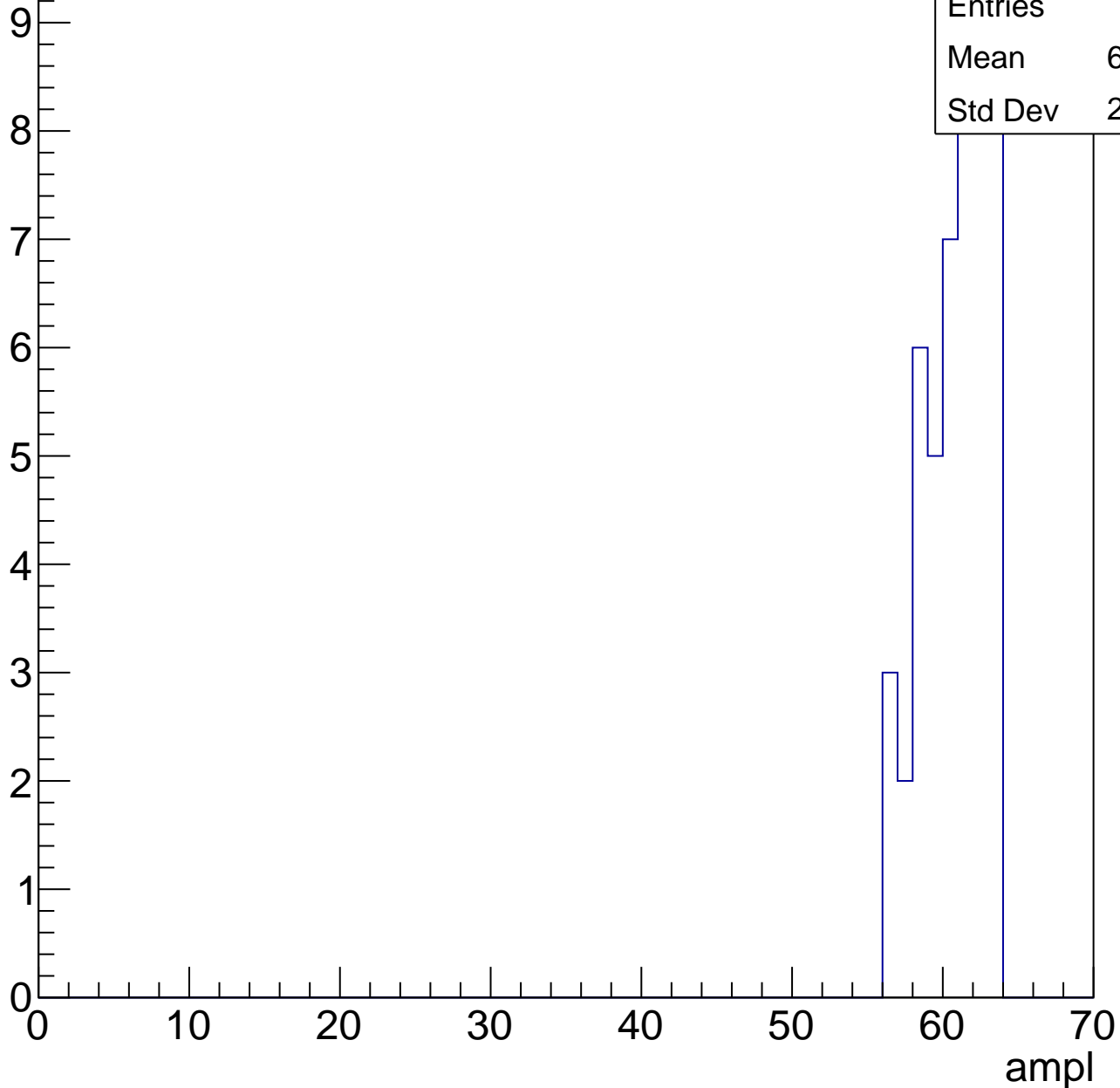
Entries	45
Mean	54.98
Std Dev	3.474



# B0L001S, U21-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

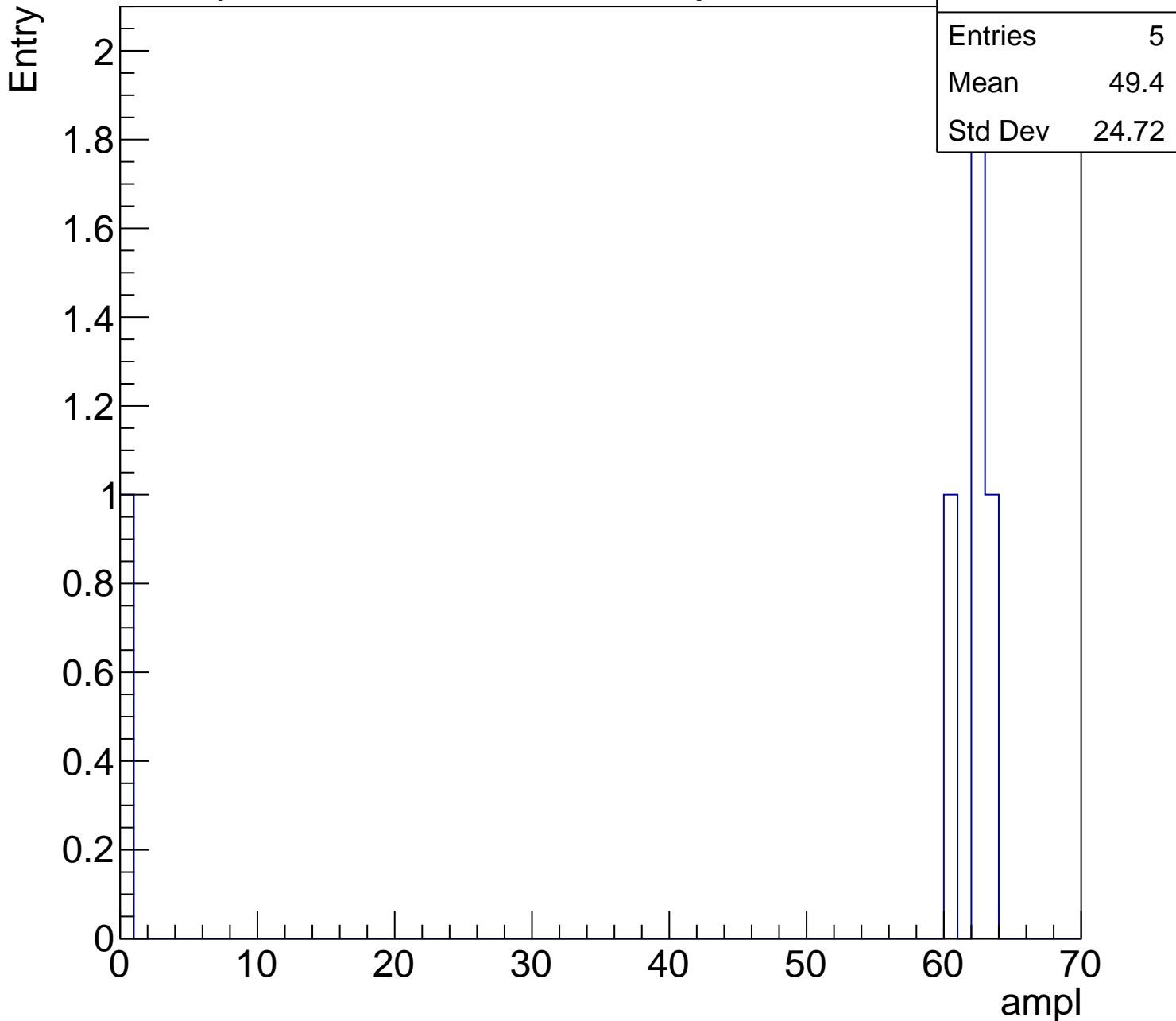
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	49.4
Std Dev	24.72

0 10 20 30 40 50 60 70

ampl





# B0L001S, U21-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U21-ch63, adc0

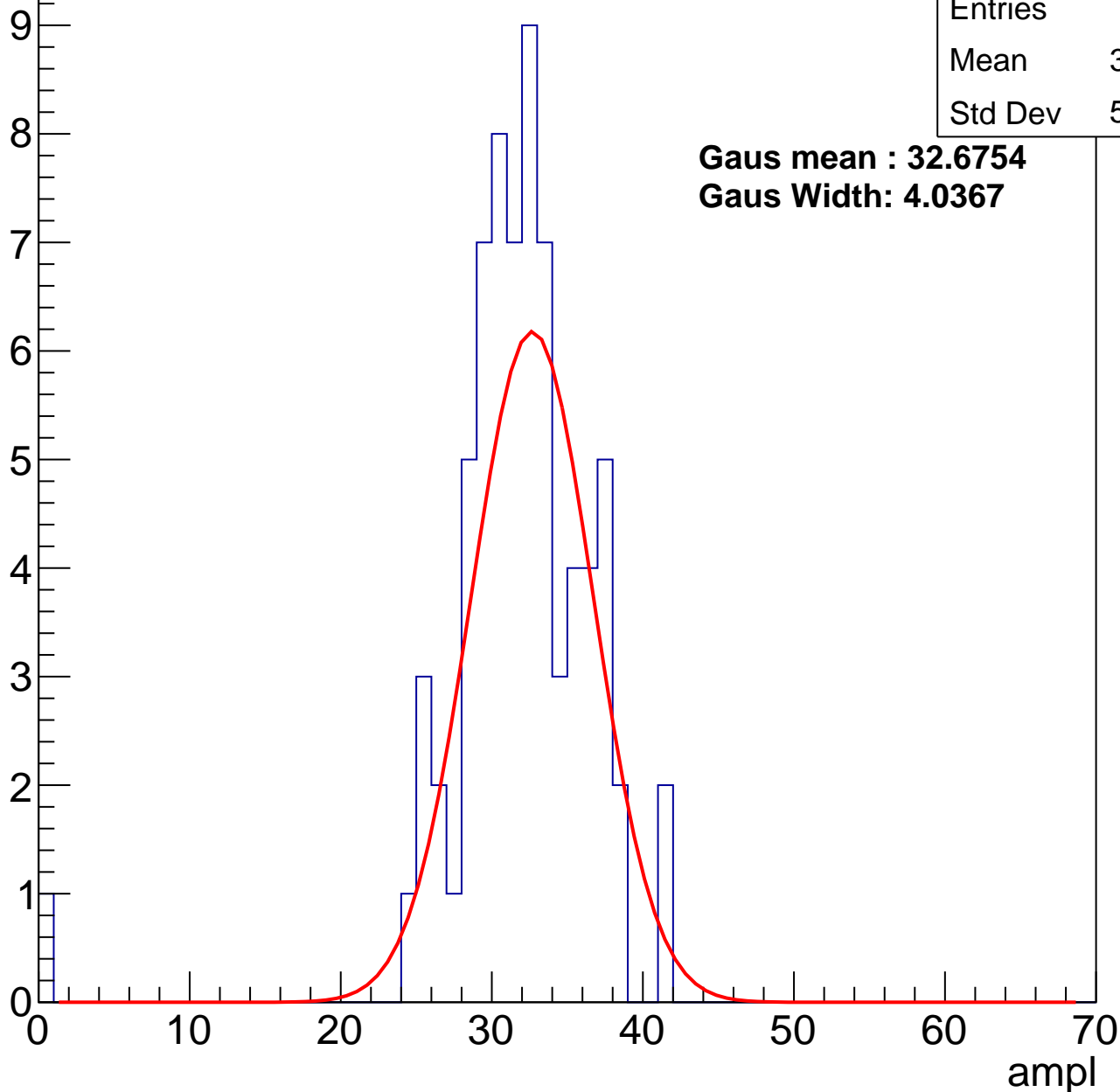
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	31.35
Std Dev	5.257

**Gaus mean : 32.6754**

**Gaus Width: 4.0367**



# B0L001S, U21-ch63, adc1

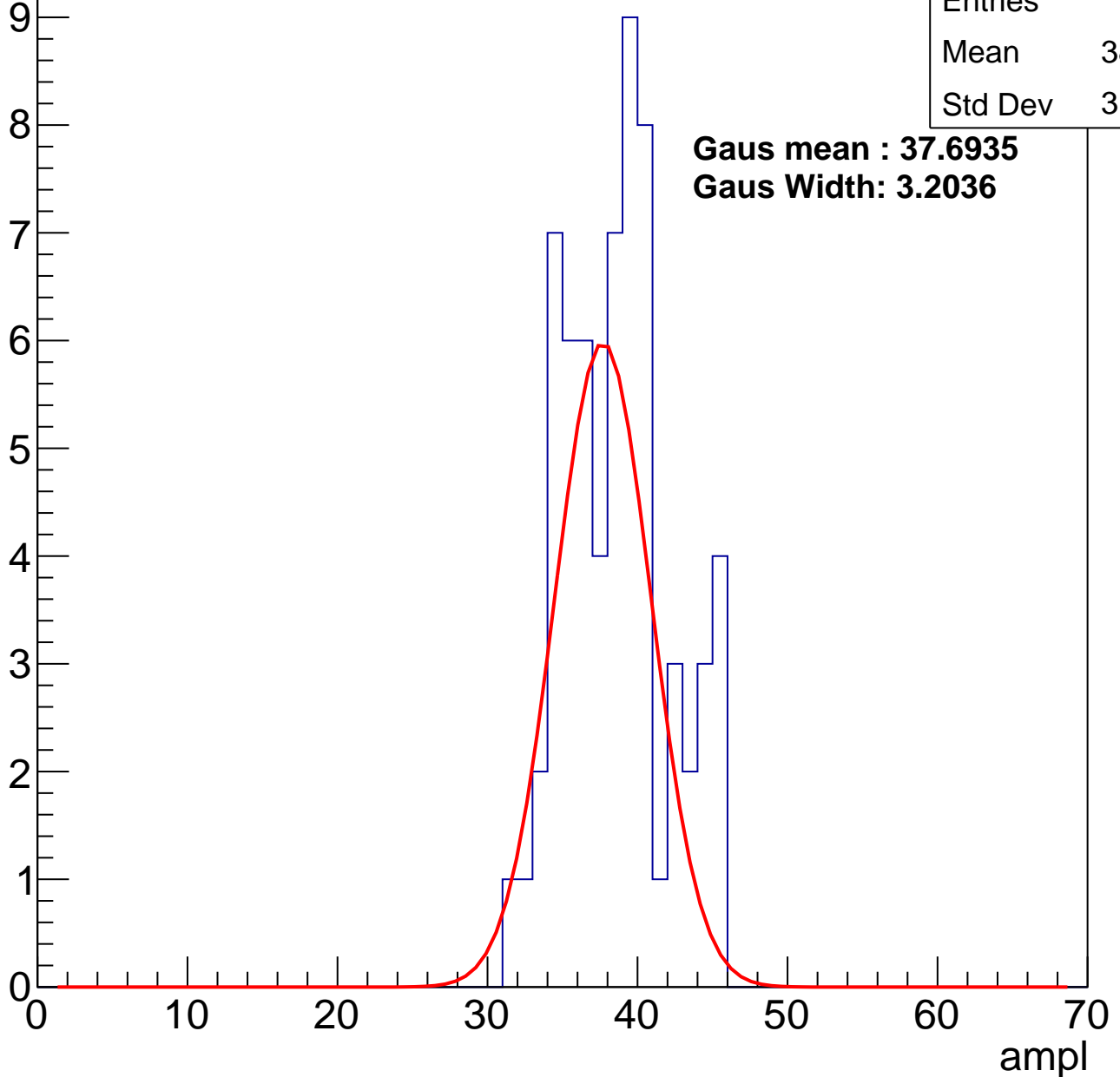
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	38.17
Std Dev	3.489

**Gaus mean : 37.6935**

**Gaus Width: 3.2036**



# B0L001S, U21-ch63, adc2

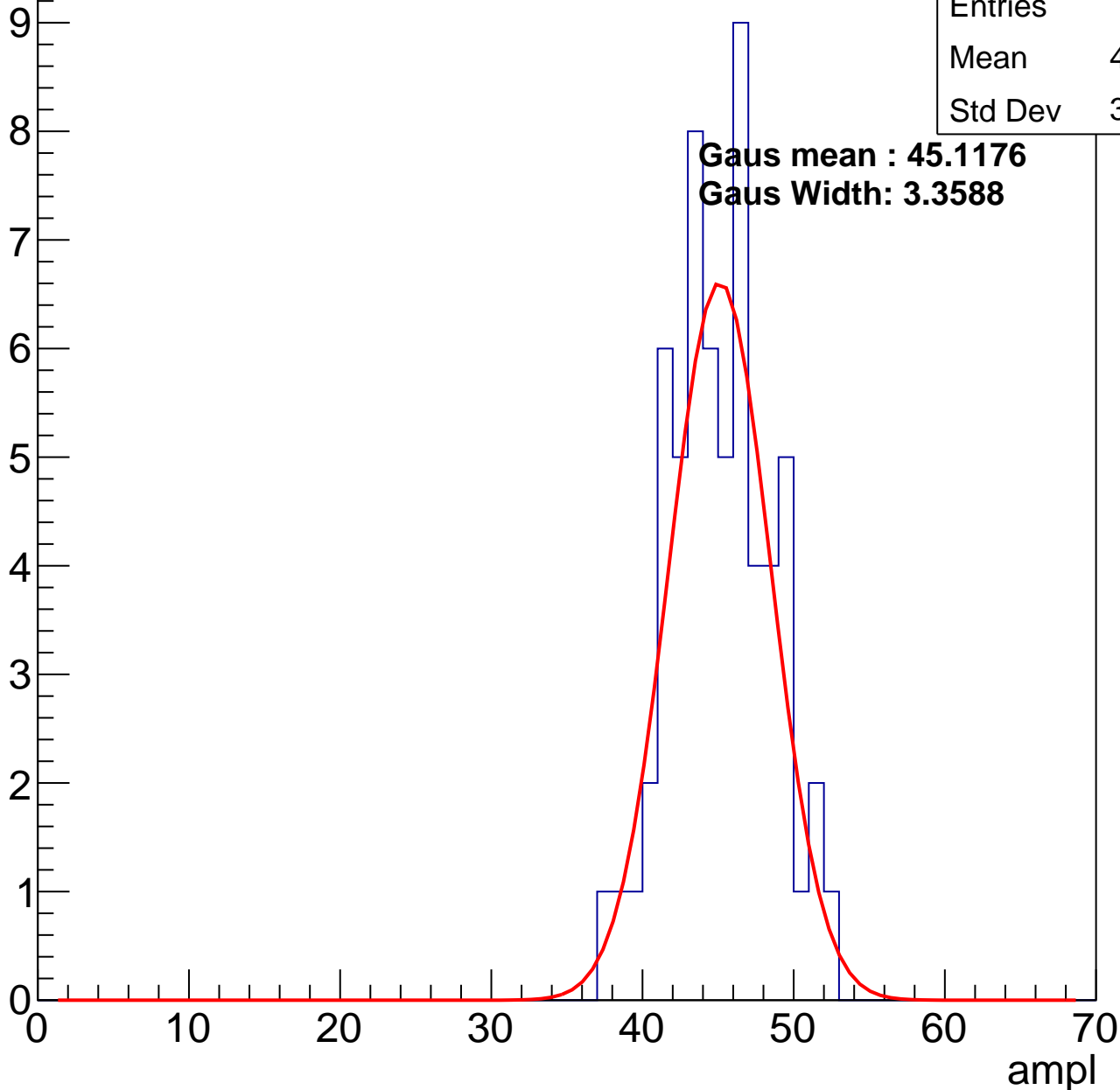
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	44.69
Std Dev	3.287

**Gaus mean : 45.1176**

**Gaus Width: 3.3588**

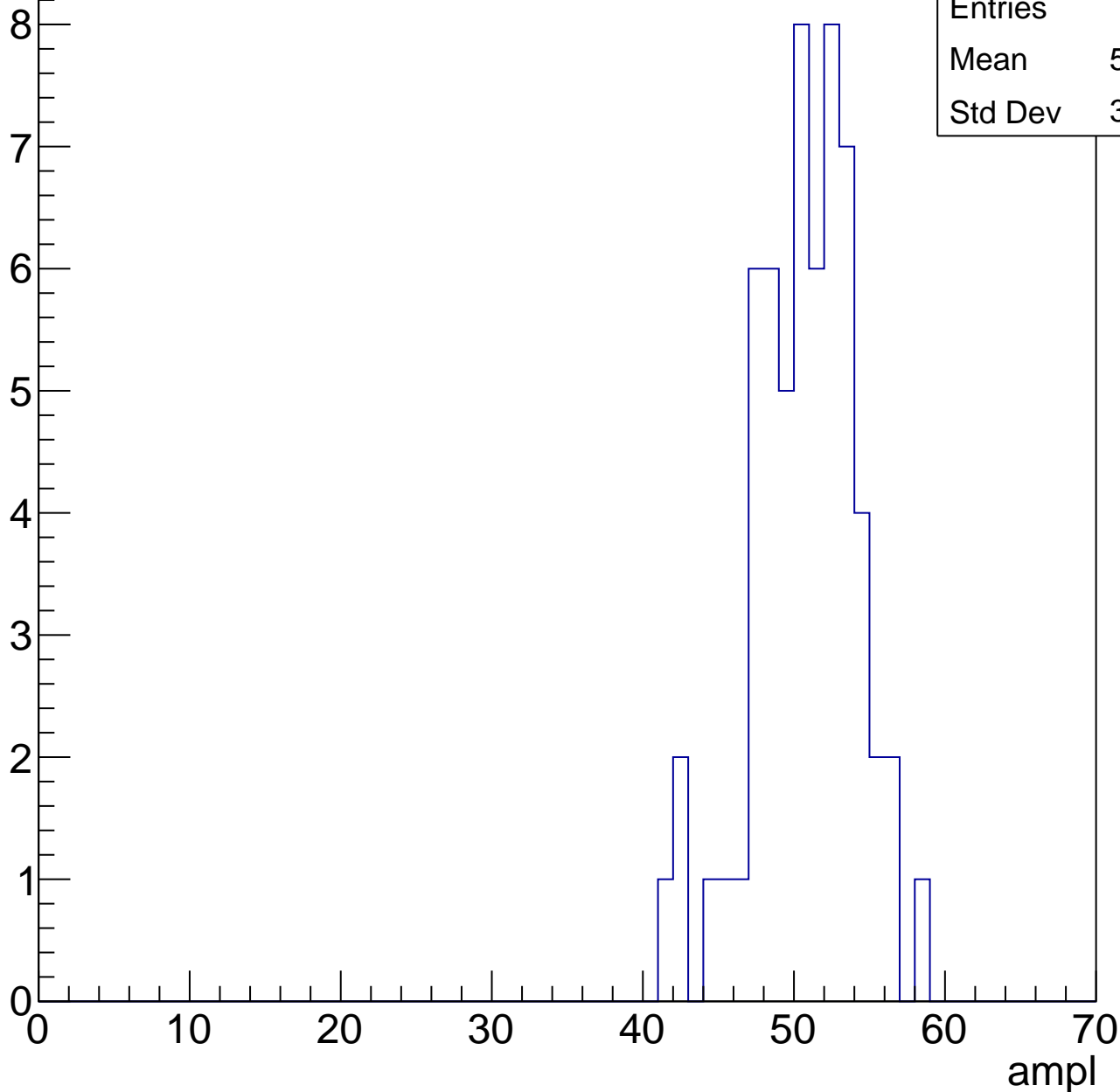


# B0L001S, U21-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	50.23
Std Dev	3.428

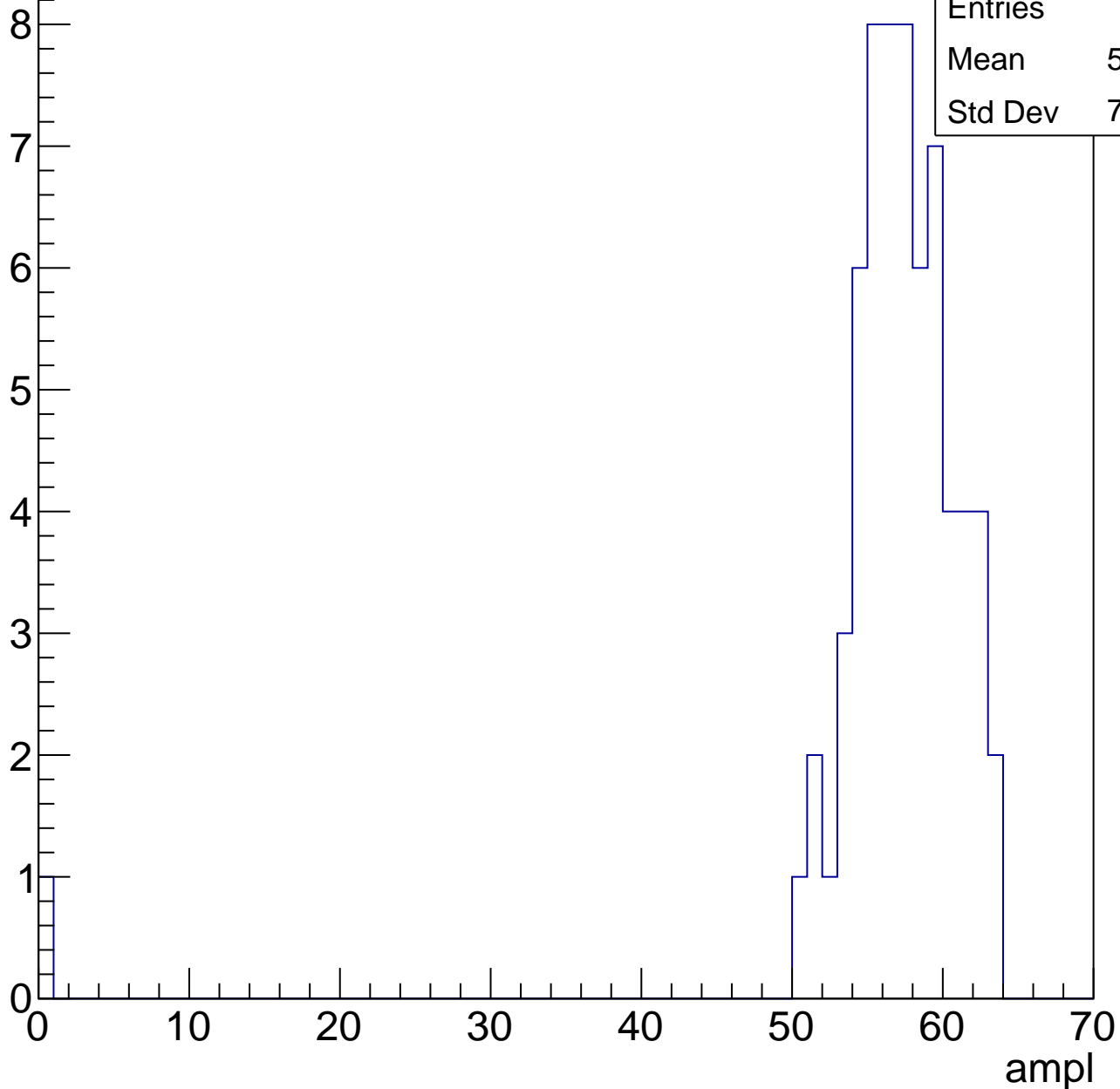


# B0L001S, U21-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	56.15
Std Dev	7.642

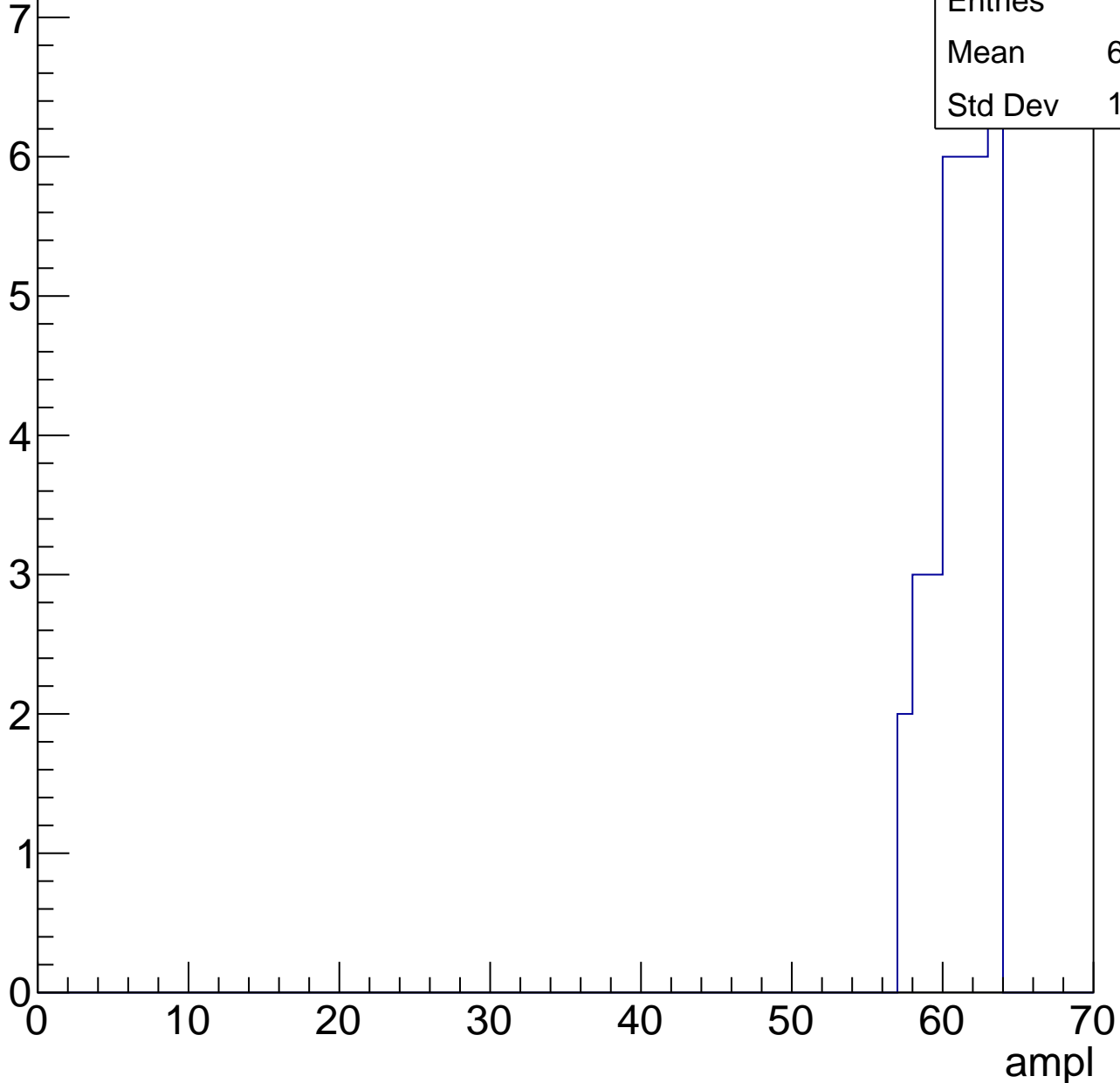


# B0L001S, U21-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	33
Mean	60.73
Std Dev	1.814



# B0L001S, U21-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

1

Mean

63

Std Dev

0



# B0L001S, U21-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U21-ch64, adc0

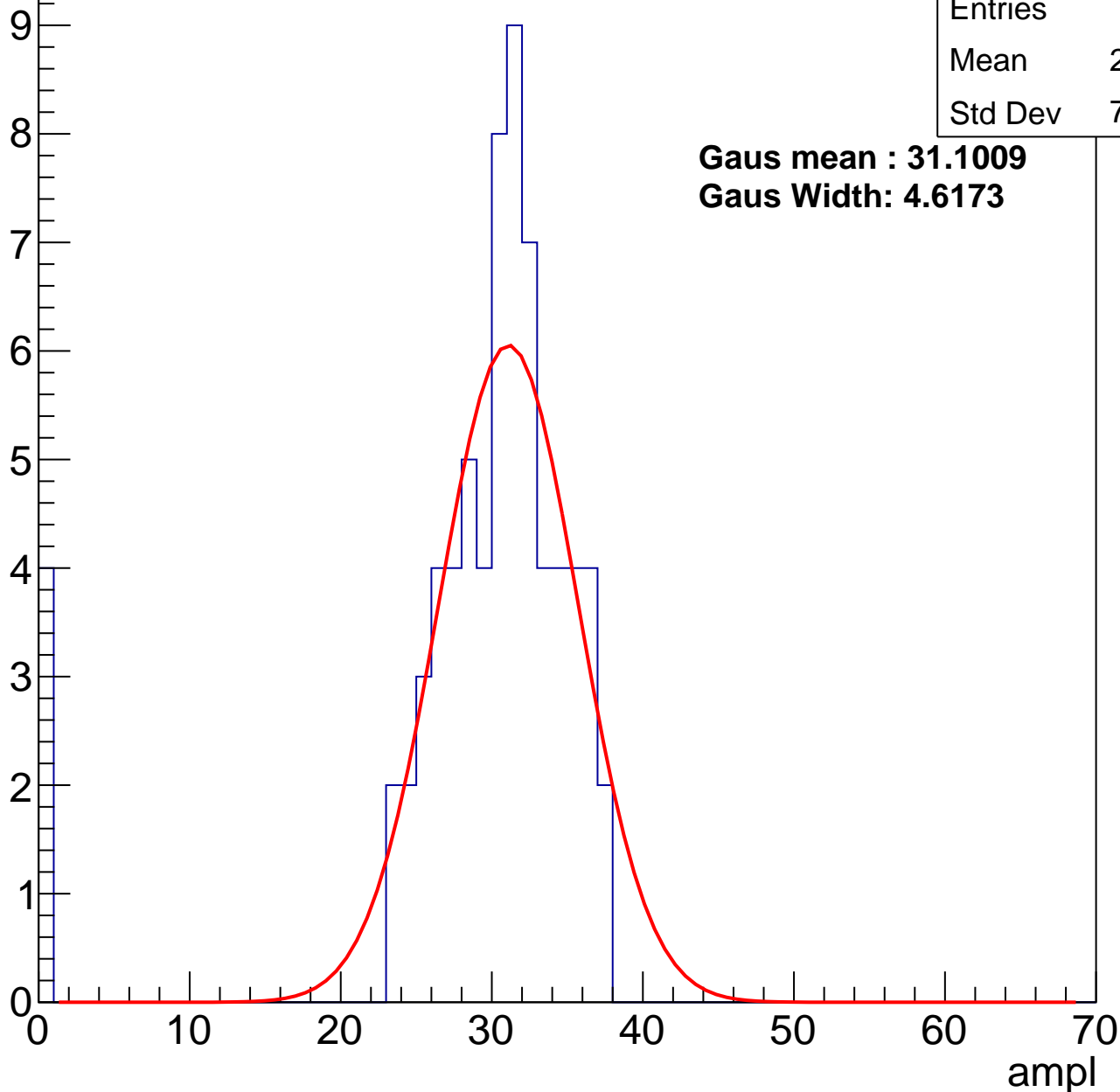
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	28.66
Std Dev	7.857

**Gaus mean : 31.1009**

**Gaus Width: 4.6173**



# B0L001S, U21-ch64, adc1

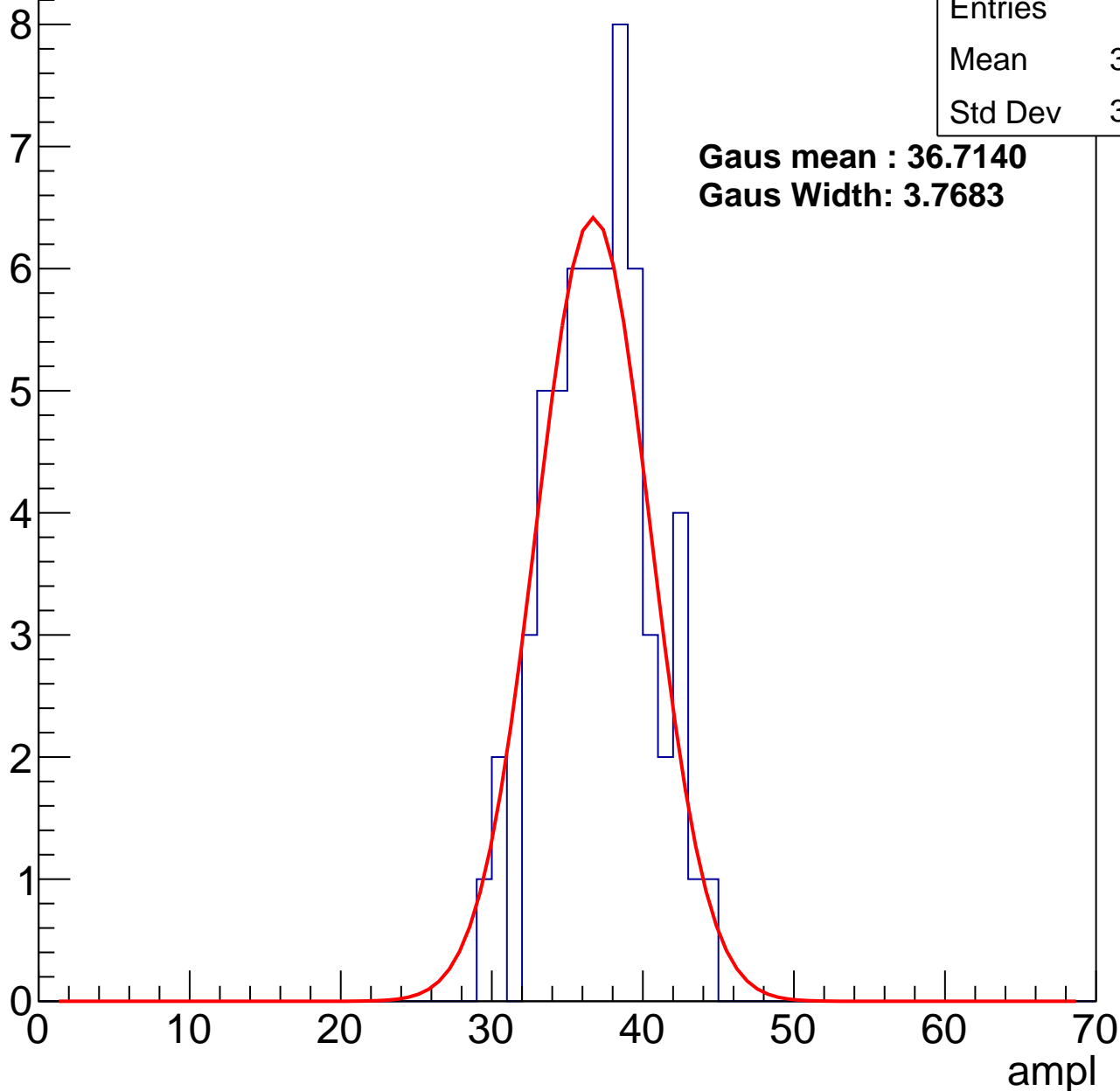
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	36.66
Std Dev	3.348

**Gaus mean : 36.7140**

**Gaus Width: 3.7683**



# B0L001S, U21-ch64, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	79
Mean	43.47
Std Dev	3.788

**Gaus mean : 43.7309**

**Gaus Width: 3.6964**

Entry

10

8

6

4

2

0

0

10

20

30

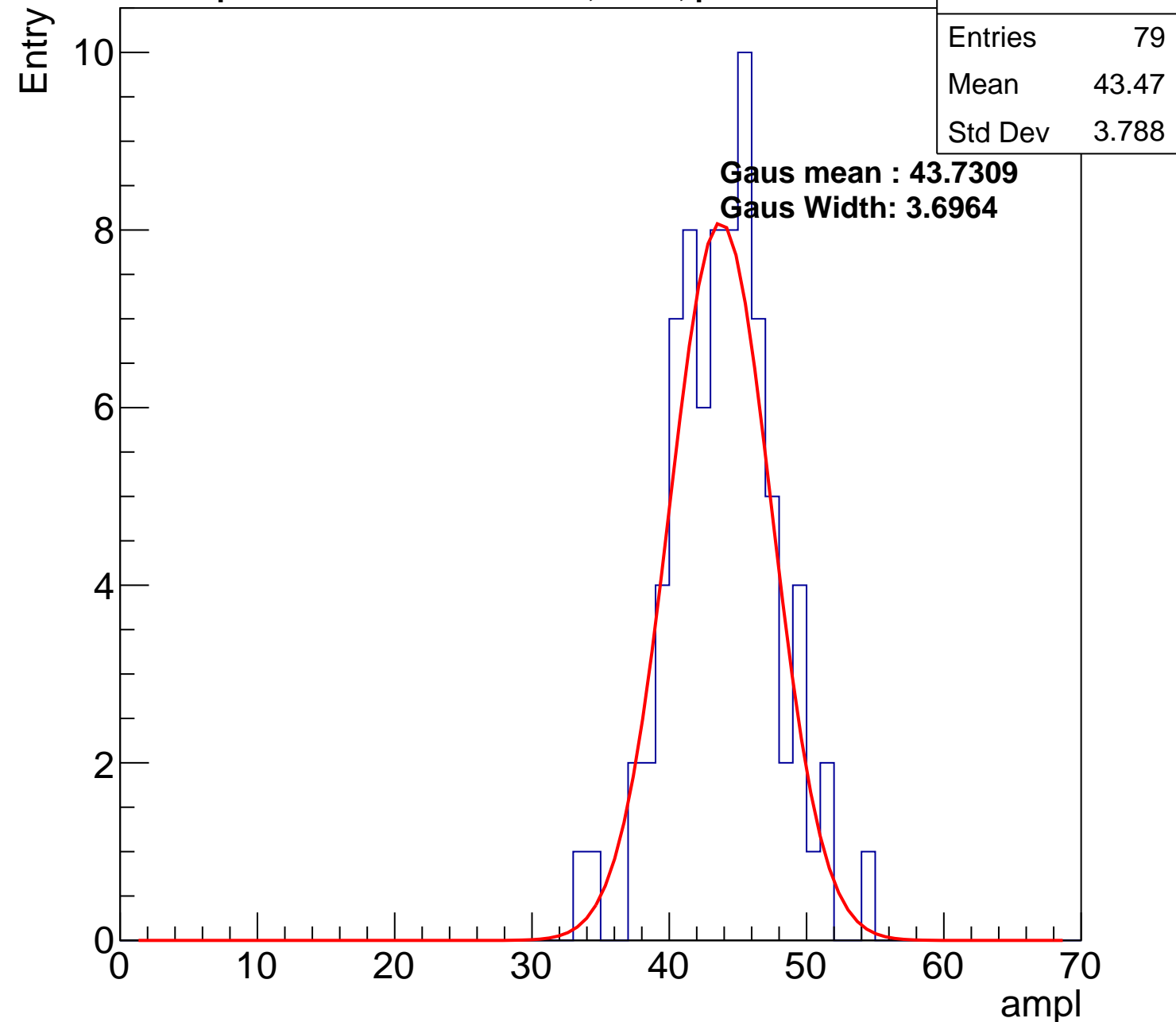
40

50

60

70

ampl

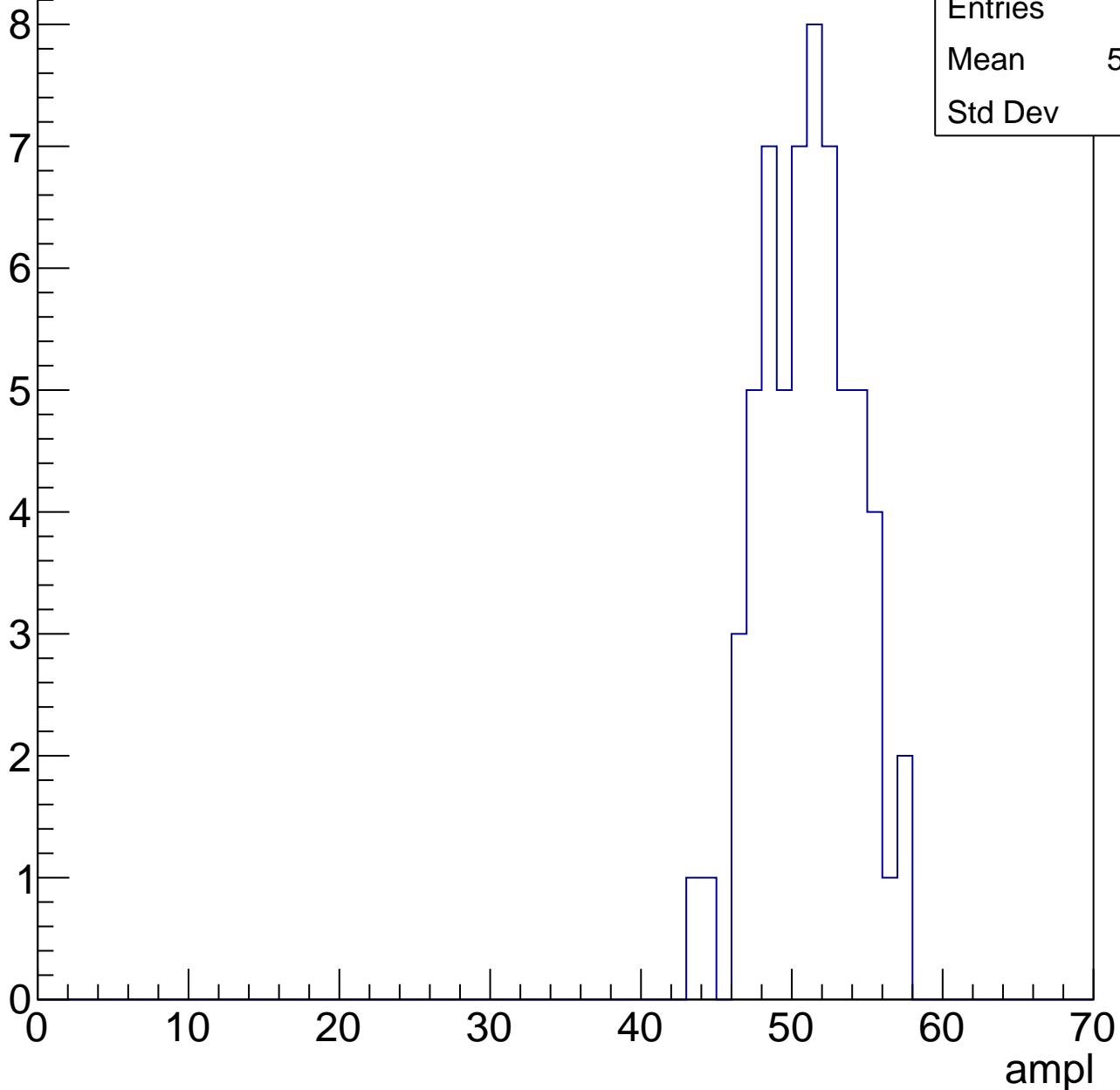


# B0L001S, U21-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

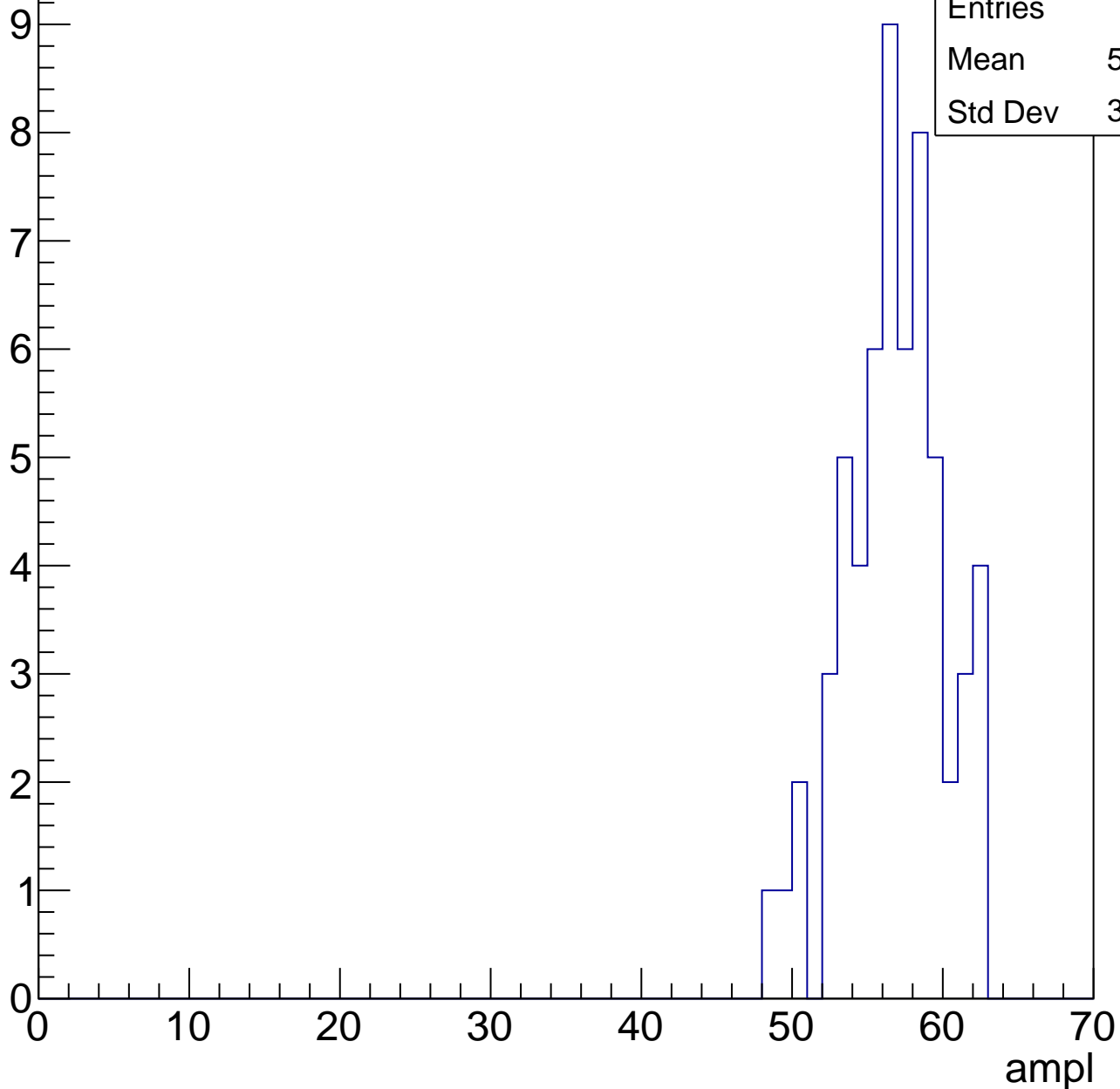
Entries	61
Mean	50.62
Std Dev	3.09



# B0L001S, U21-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

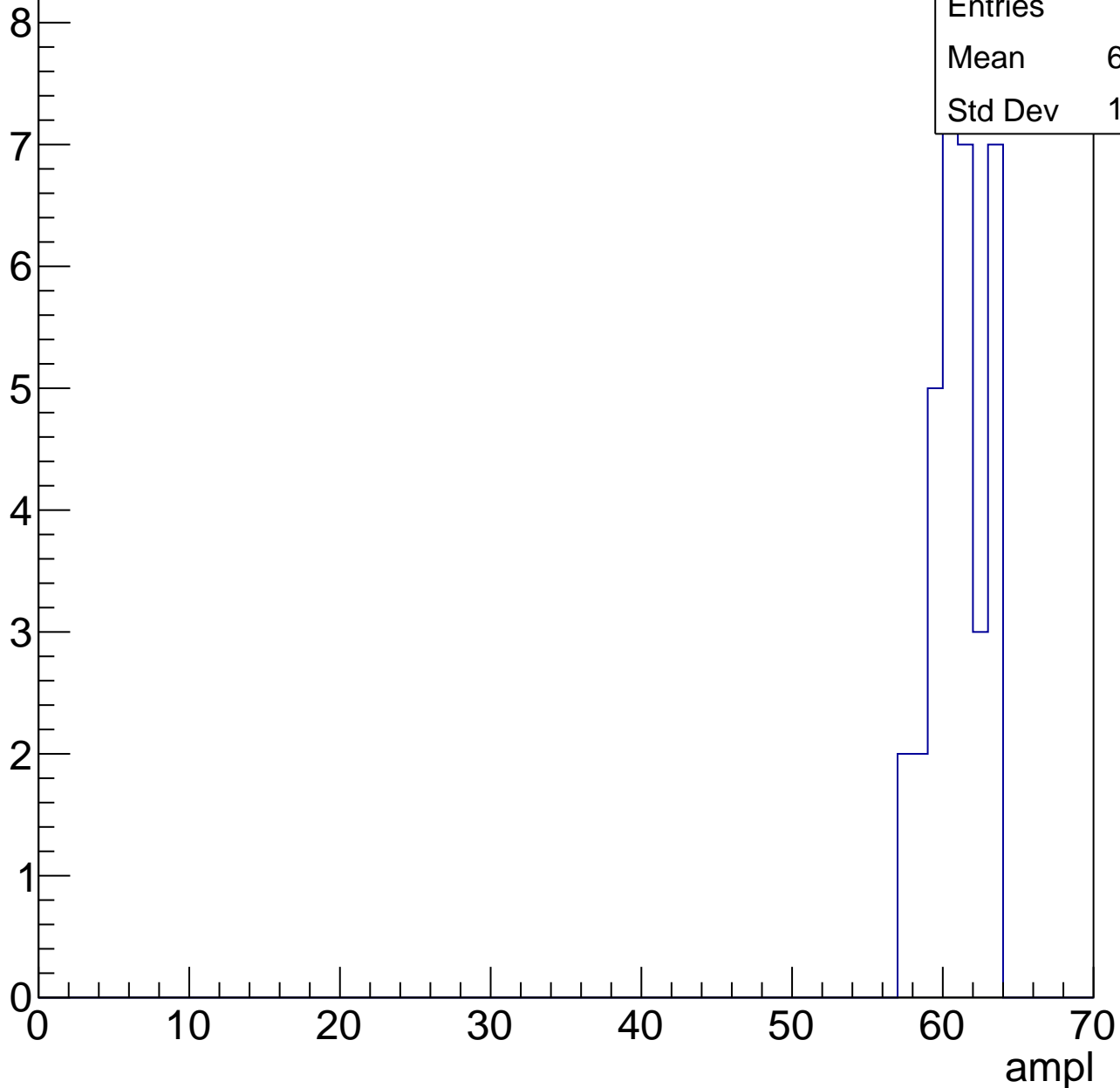


Entries	59
Mean	56.27
Std Dev	3.267

# B0L001S, U21-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

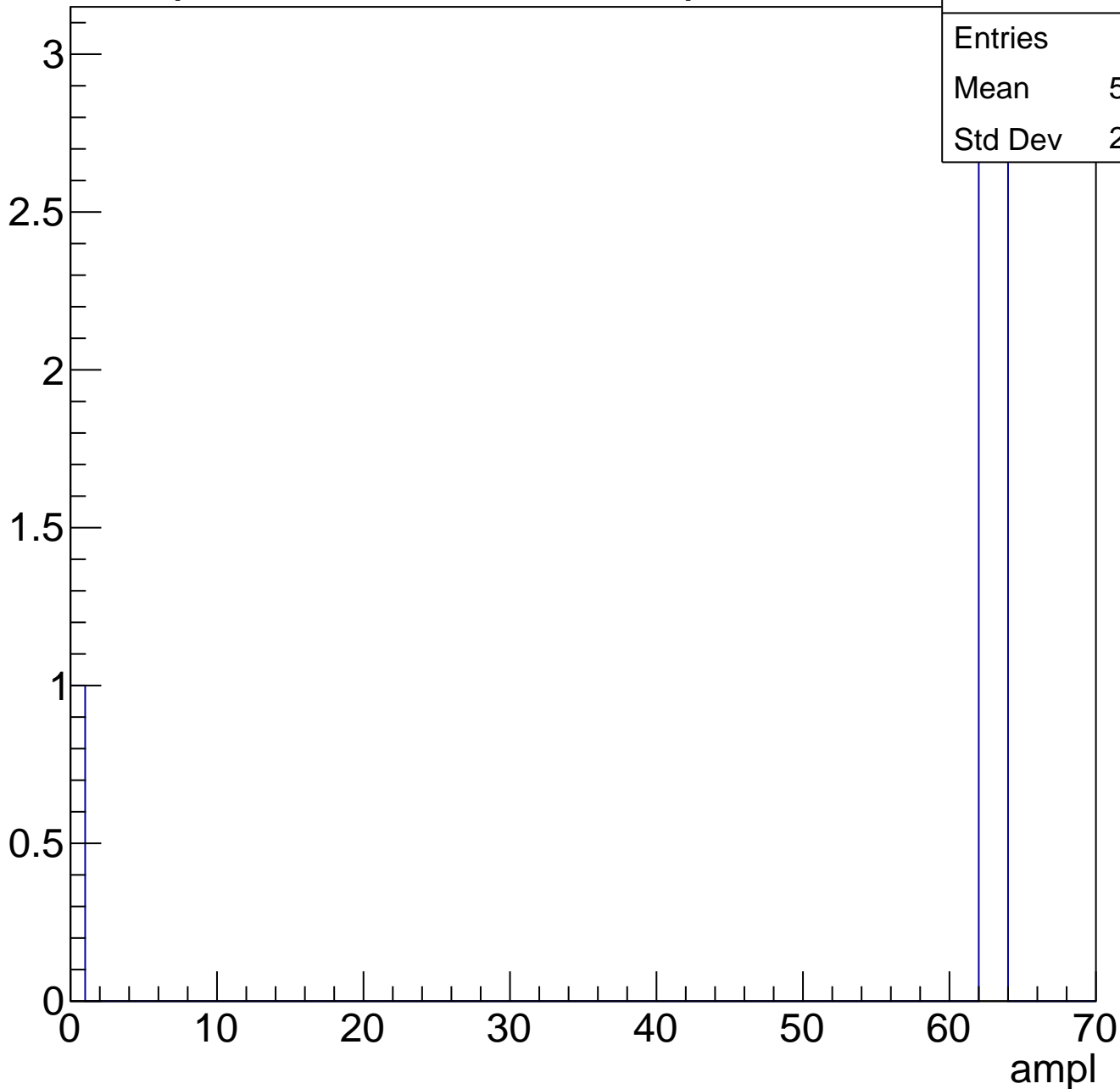


Entries	34
Mean	60.56
Std Dev	1.735

# B0L001S, U21-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch65, adc0

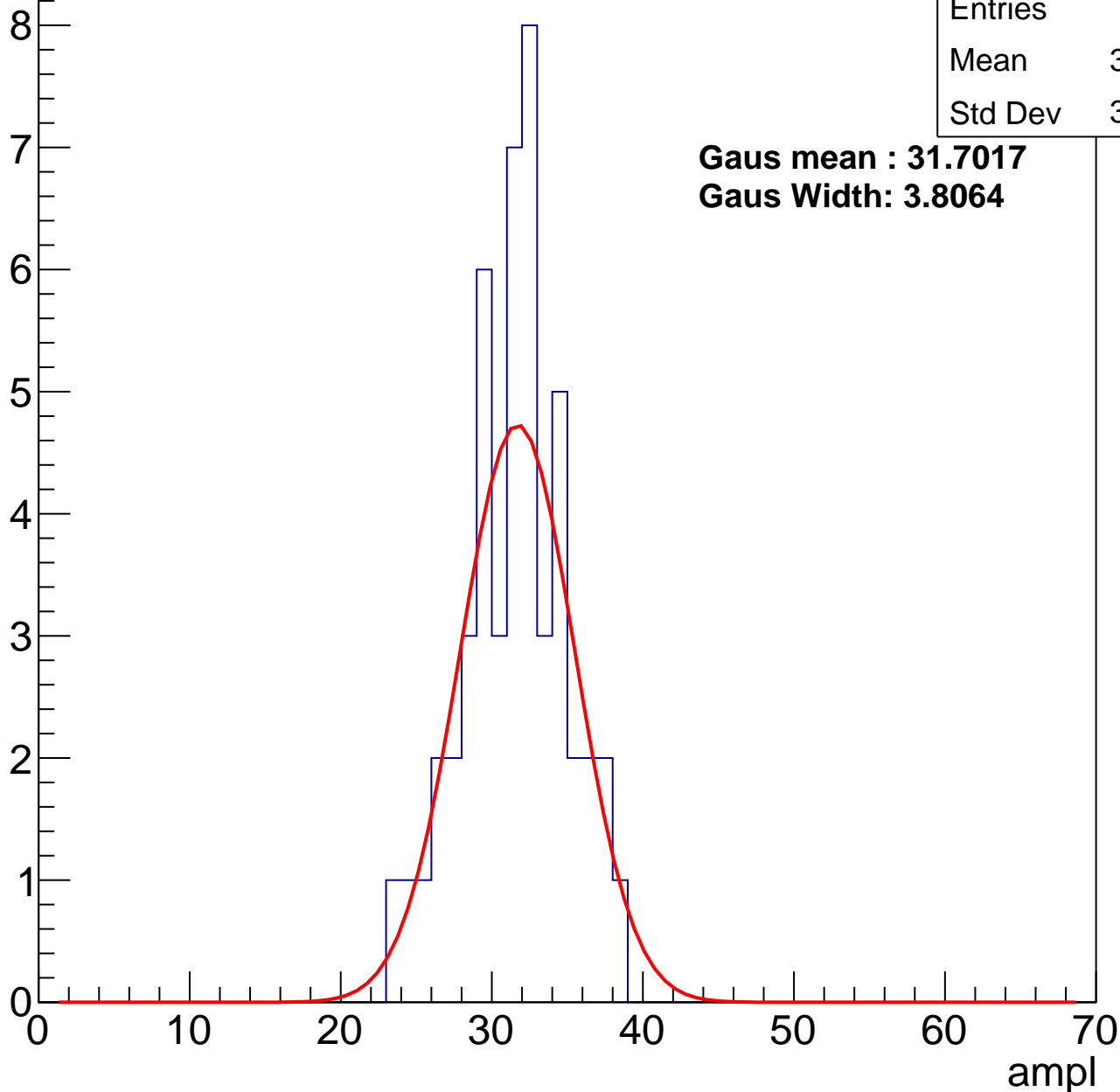
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	31.06
Std Dev	3.359

**Gaus mean : 31.7017**

**Gaus Width: 3.8064**



# B0L001S, U21-ch65, adc1

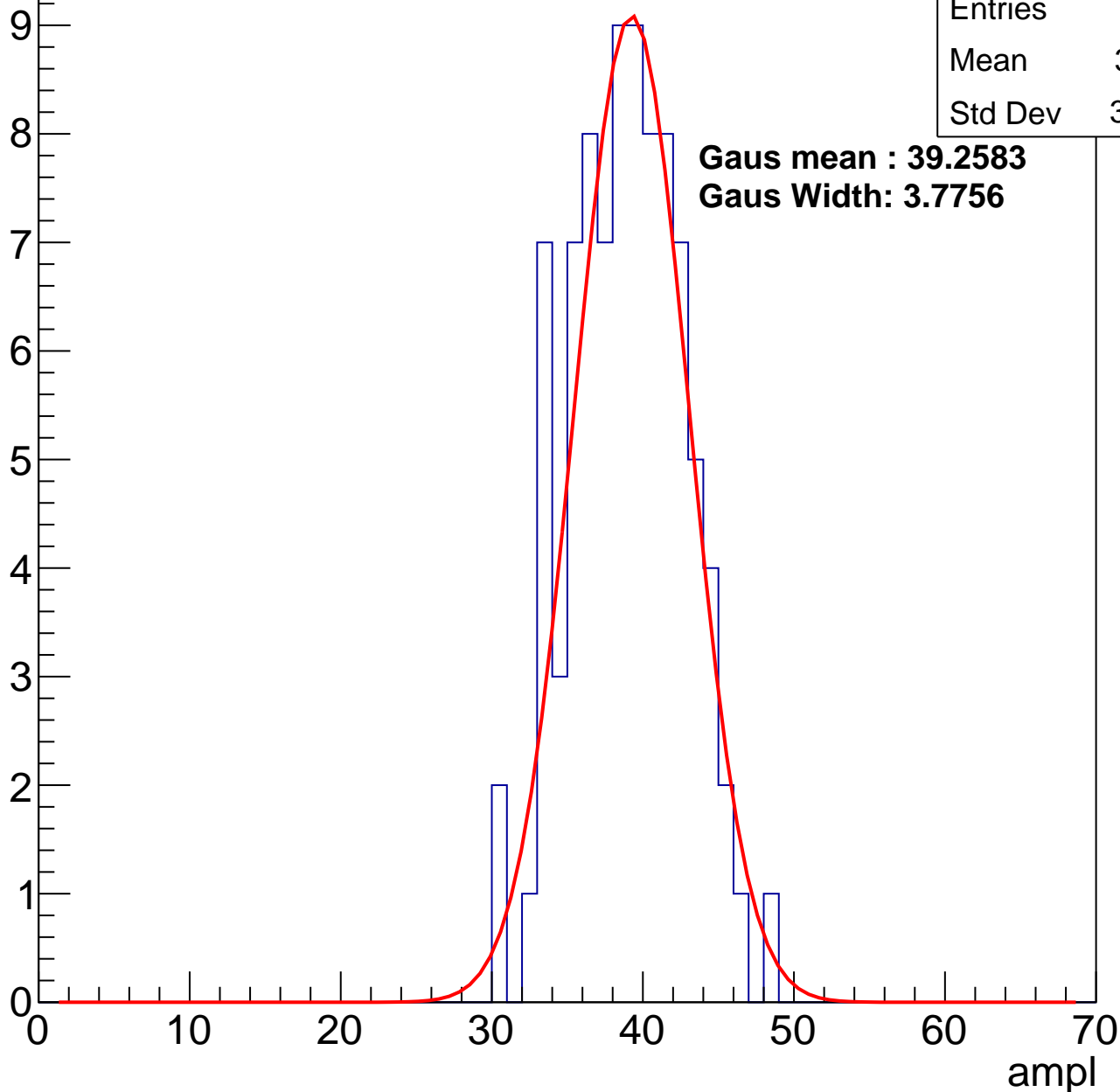
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	89
Mean	38.51
Std Dev	3.706

**Gaus mean : 39.2583**

**Gaus Width: 3.7756**



# B0L001S, U21-ch65, adc2

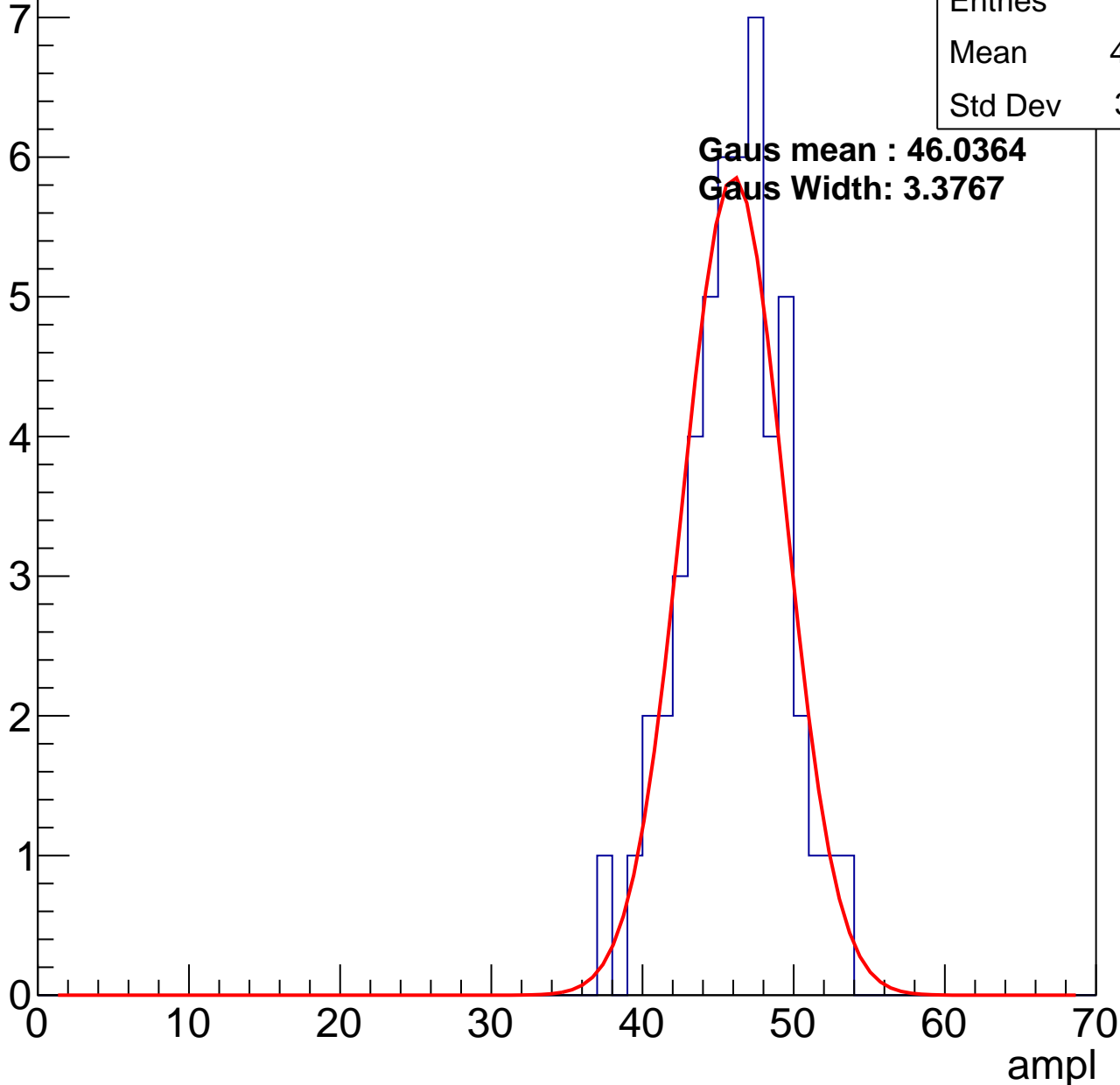
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	45.57
Std Dev	3.321

**Gaus mean : 46.0364**

**Gaus Width: 3.3767**

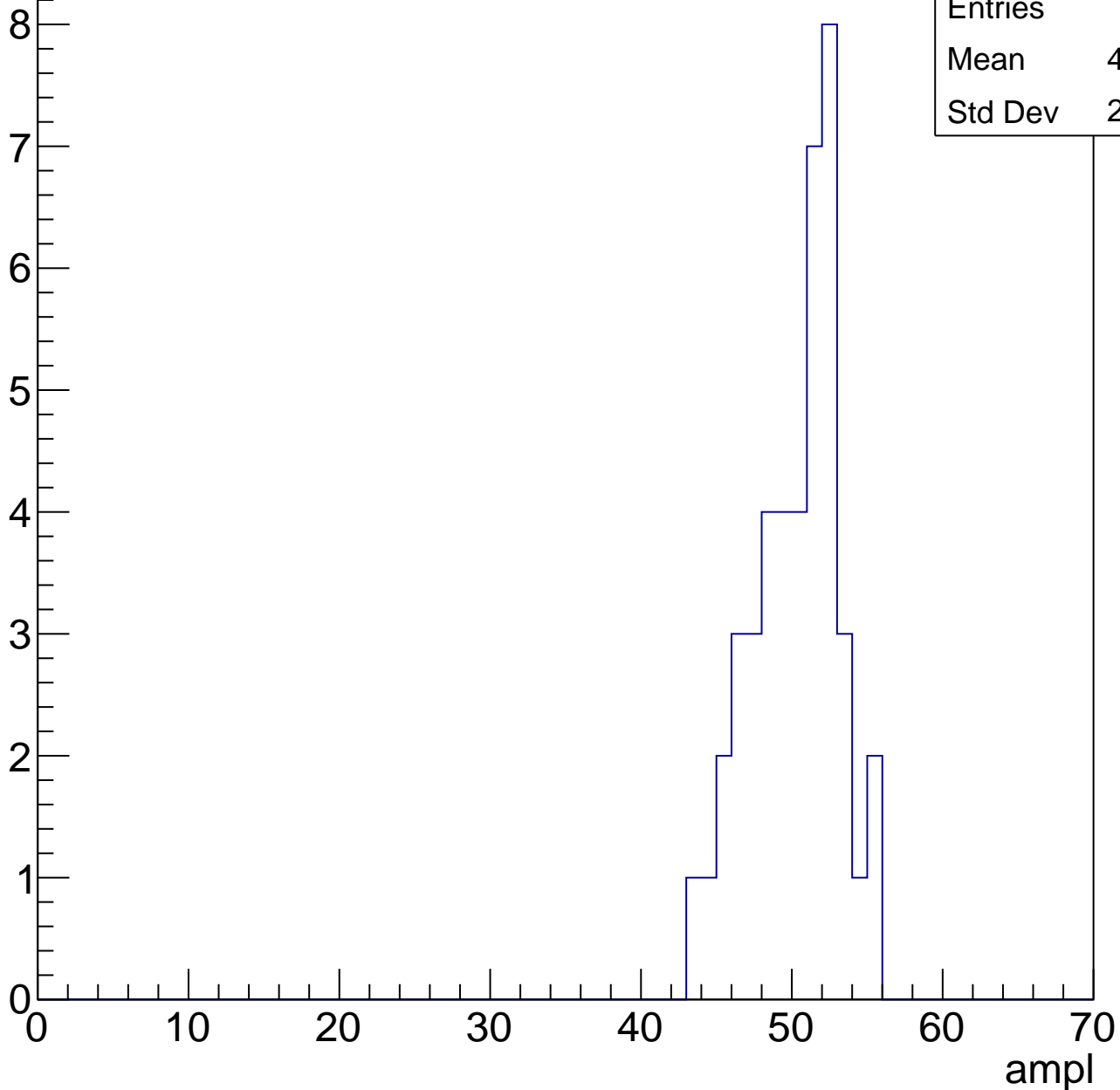


# B0L001S, U21-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	43
Mean	49.77
Std Dev	2.892

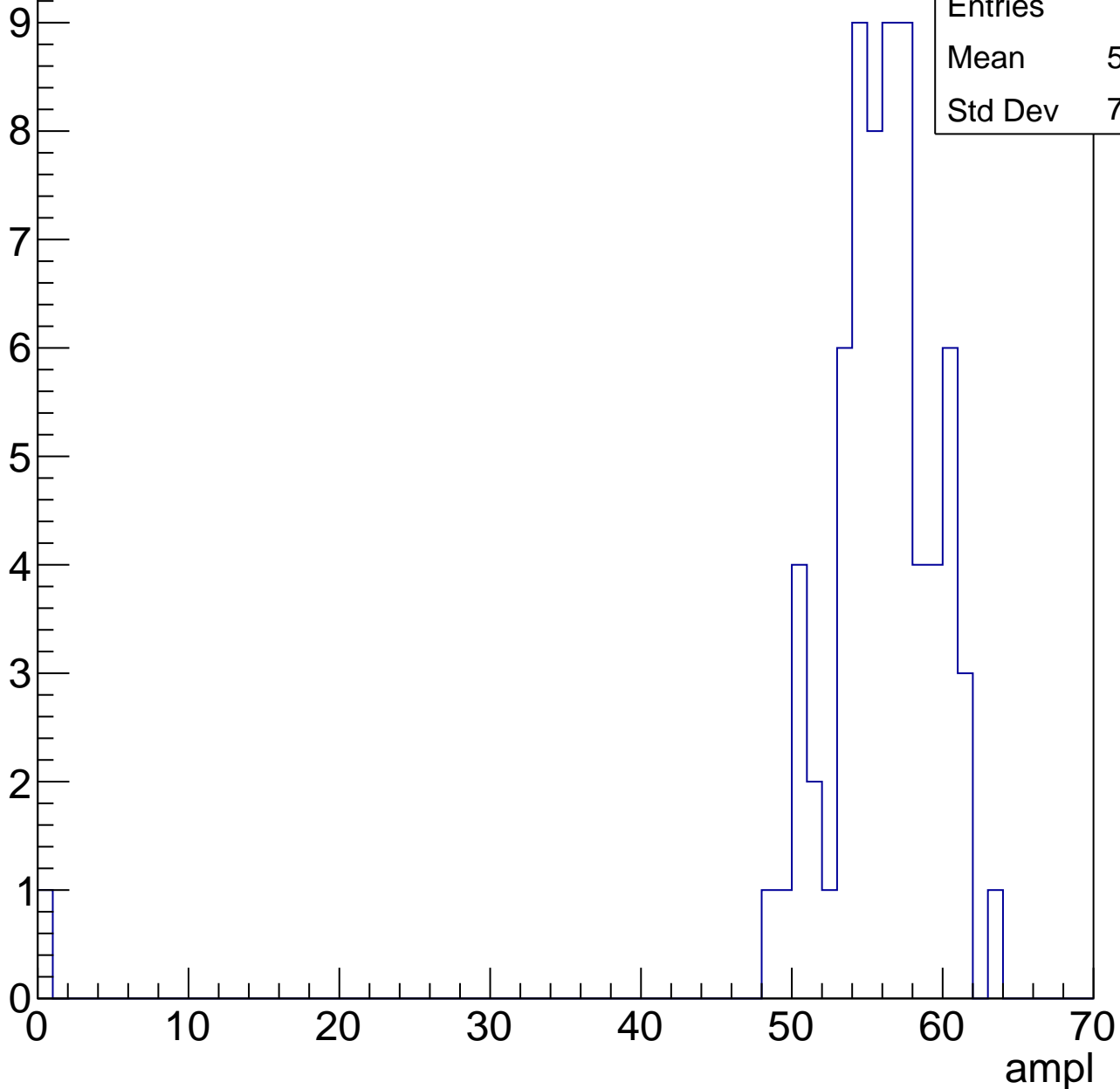


# B0L001S, U21-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	54.87
Std Dev	7.372

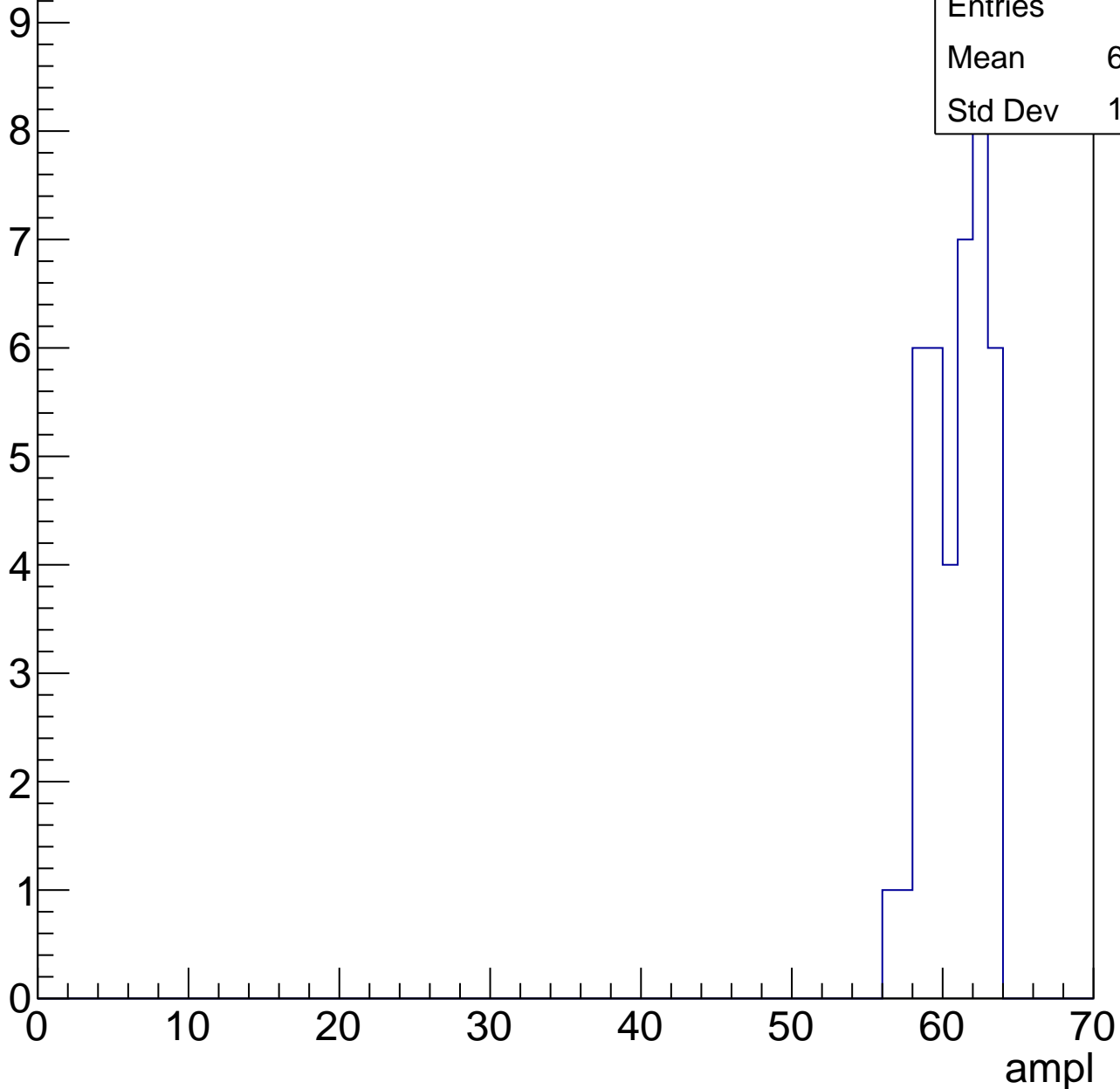


# B0L001S, U21-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	40
Mean	60.45
Std Dev	1.897



# B0L001S, U21-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	23
Std Dev	0

ampl

# B0L001S, U21-ch66, adc0

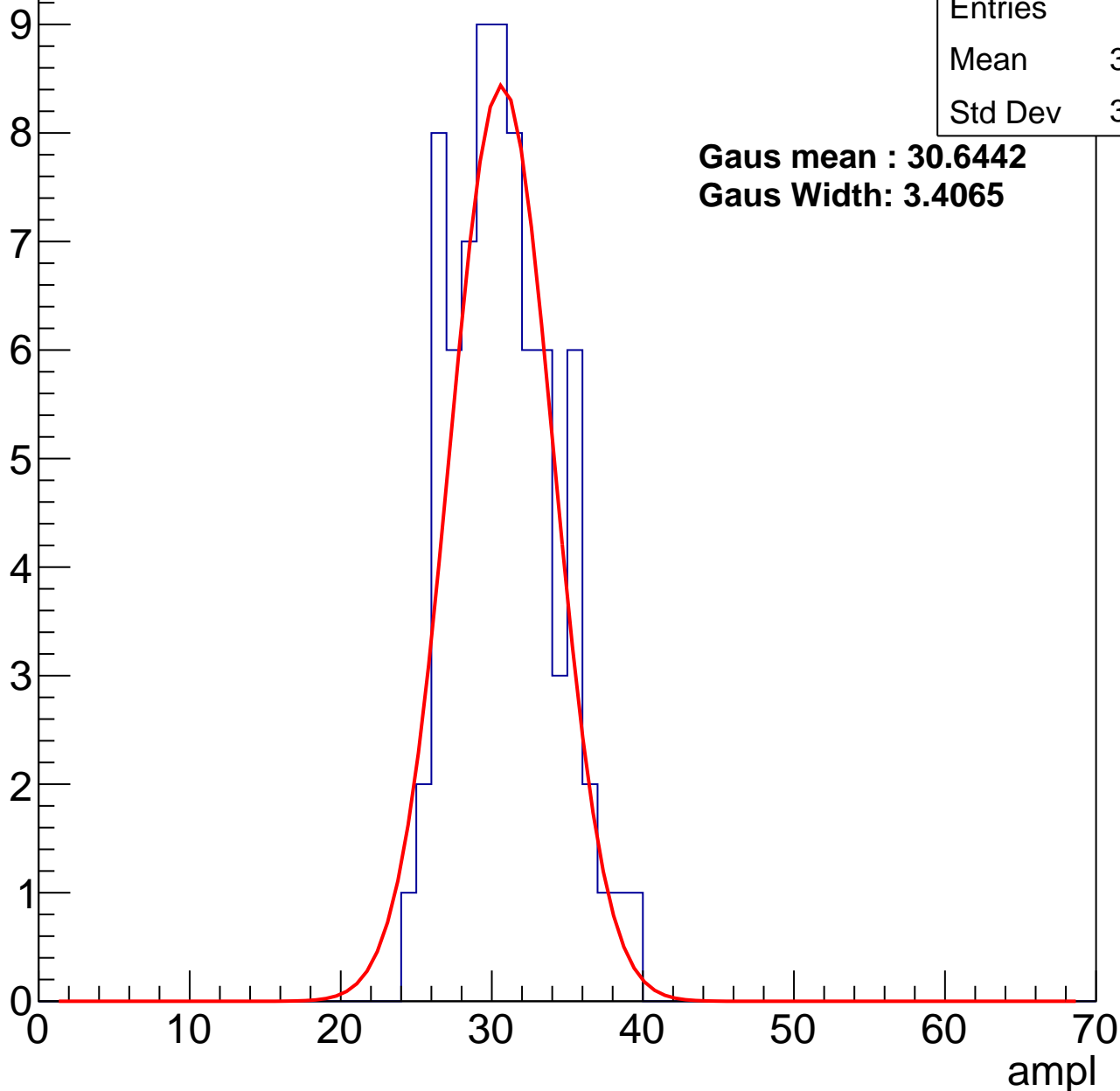
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	30.36
Std Dev	3.335

**Gaus mean : 30.6442**

**Gaus Width: 3.4065**



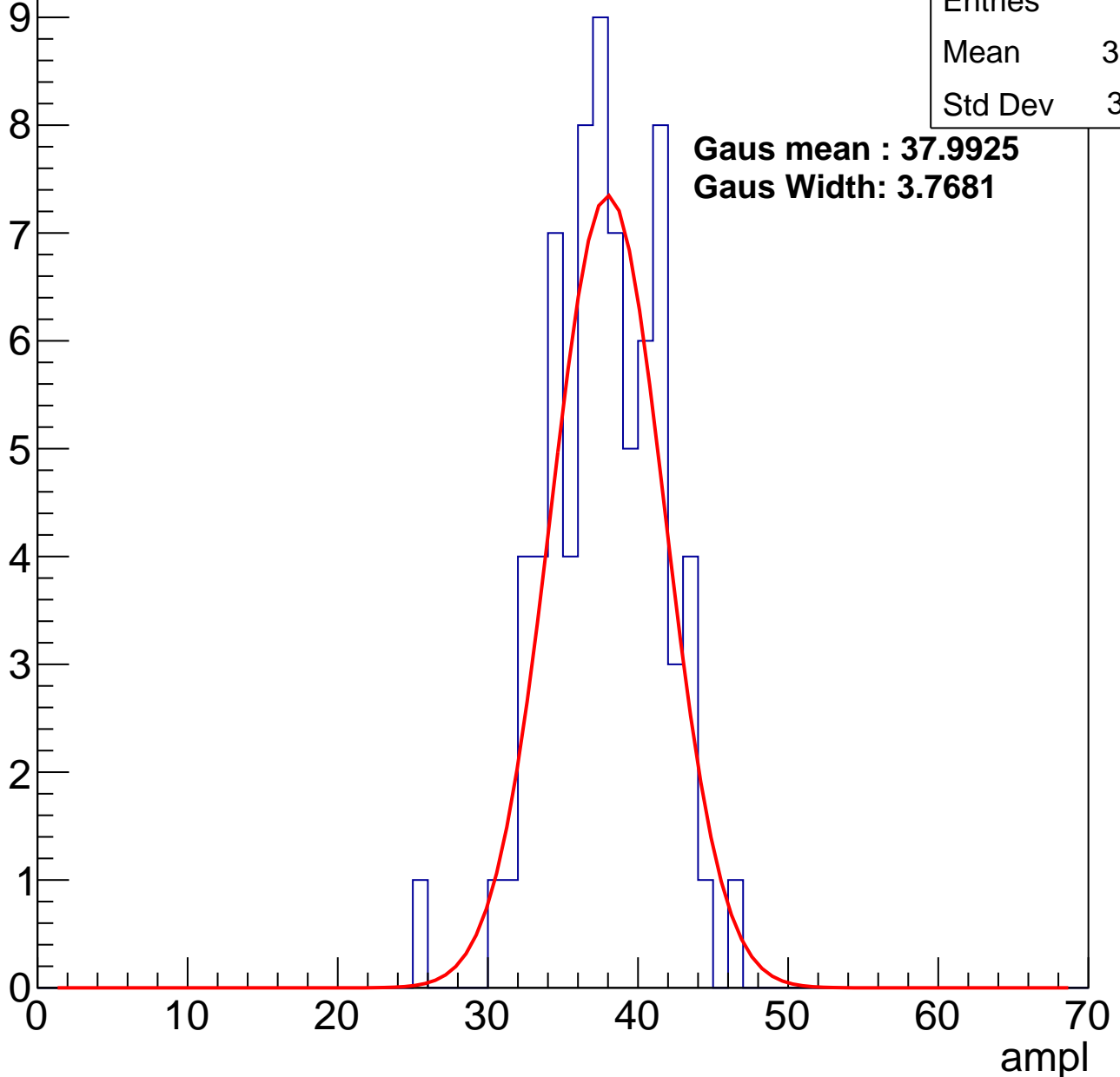
# B0L001S, U21-ch66, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	37.32
Std Dev	3.731

**Gaus mean : 37.9925**  
**Gaus Width: 3.7681**



# B0L001S, U21-ch66, adc2

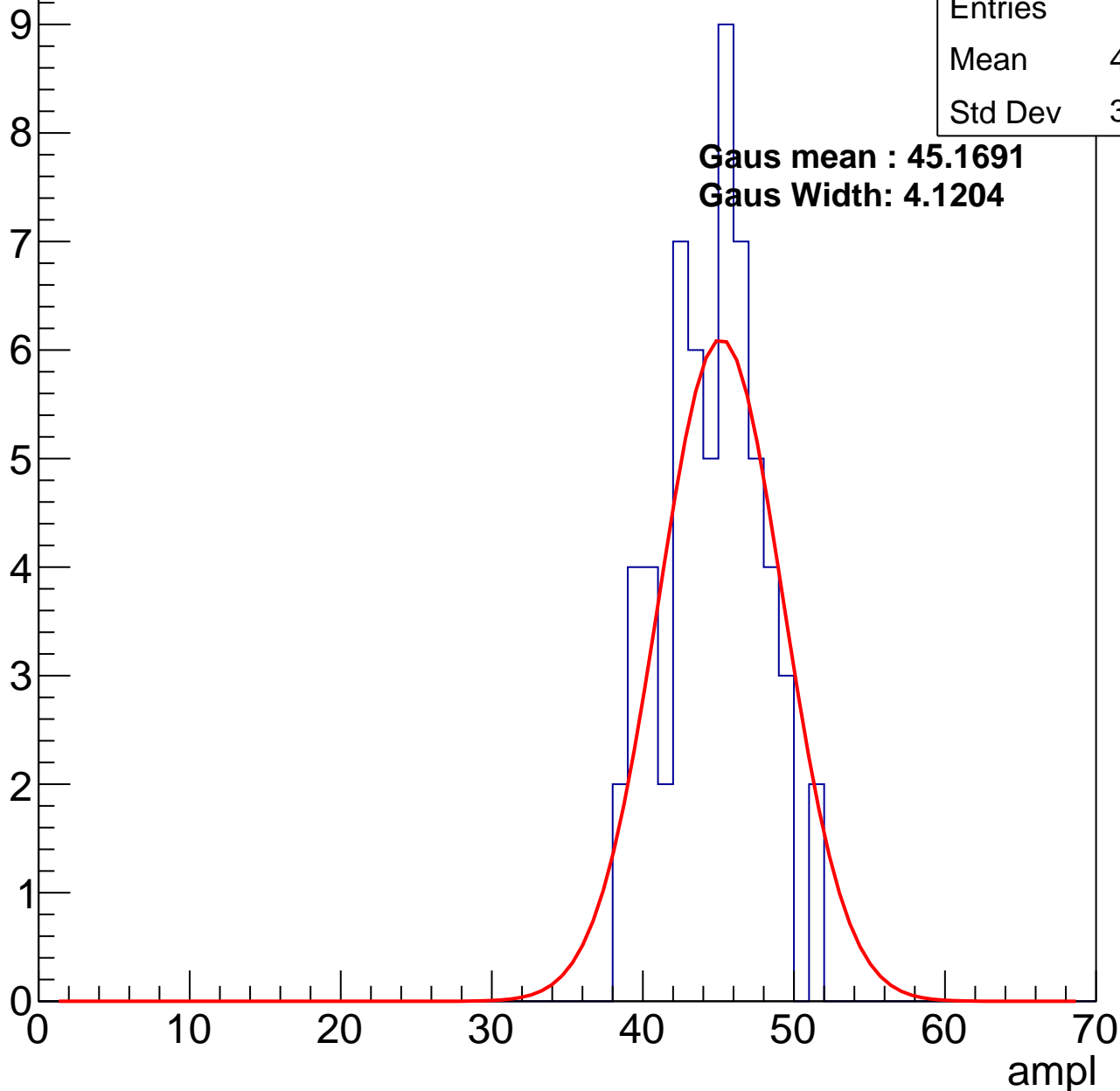
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	44.15
Std Dev	3.177

**Gaus mean : 45.1691**

**Gaus Width: 4.1204**

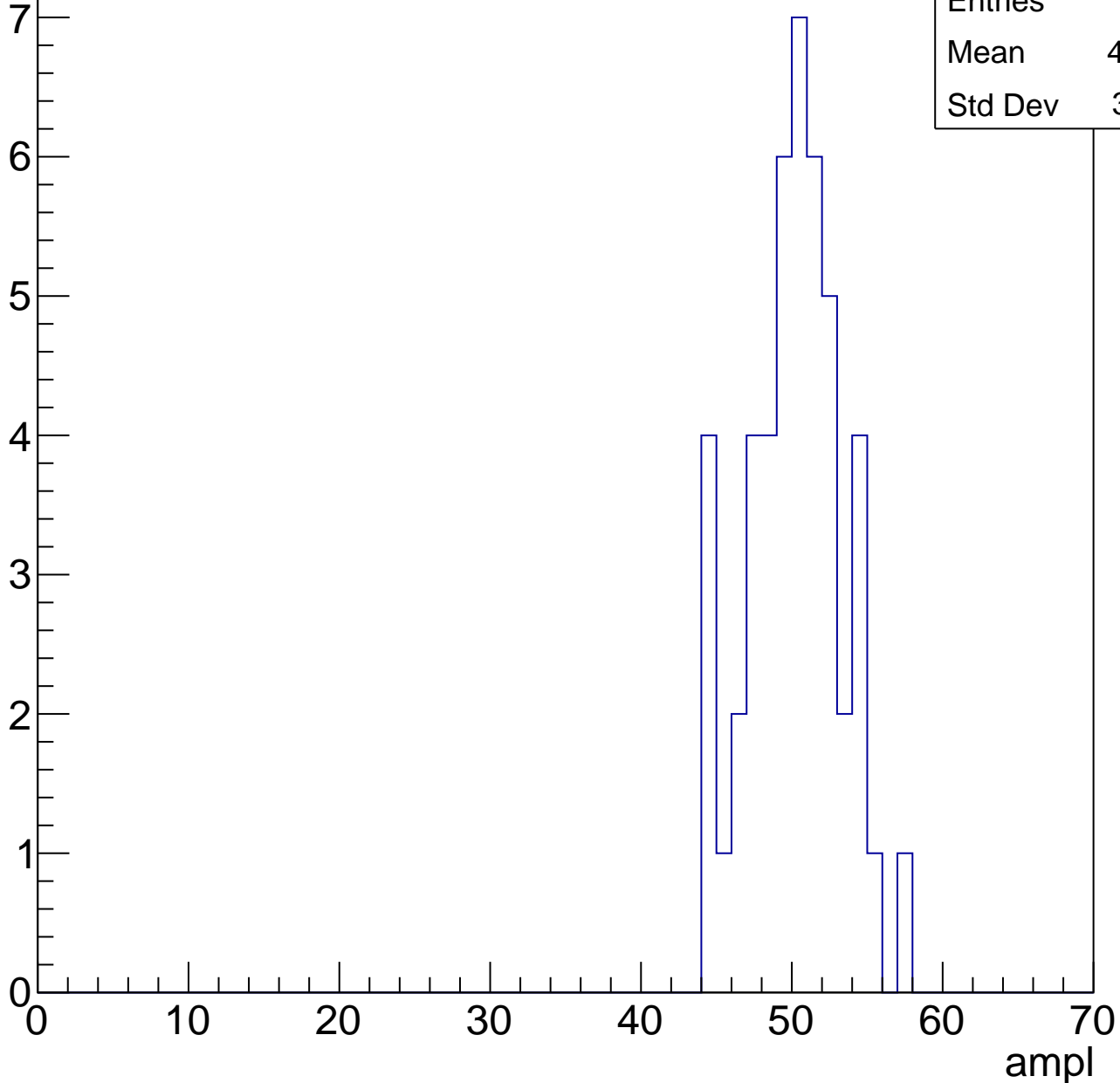


# B0L001S, U21-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	49.72
Std Dev	3.051



# B0L001S, U21-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	75
Mean	55.6
Std Dev	3.544

Entry

10

8

6

4

2

0

0

10

20

30

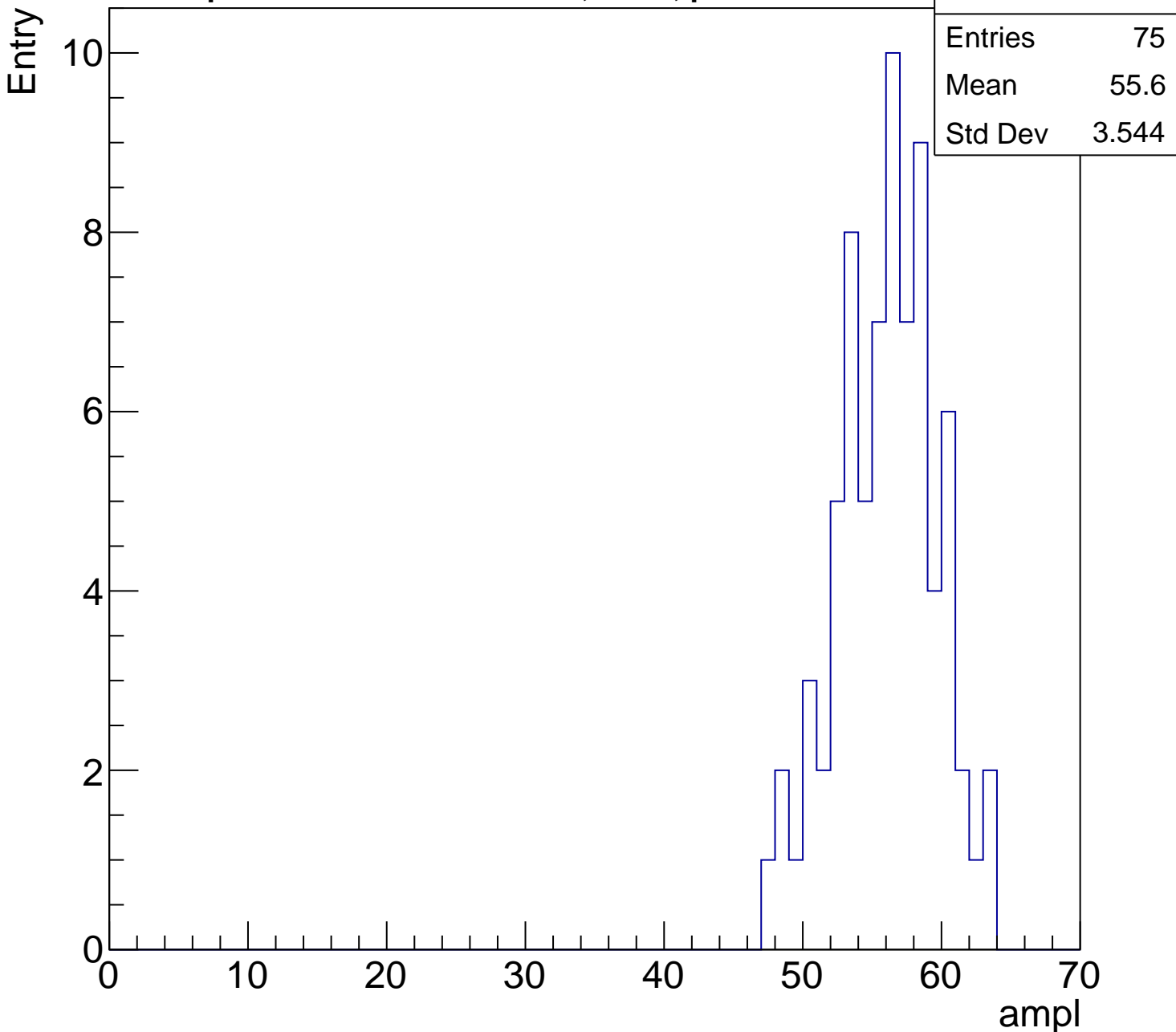
40

50

60

ampl

70

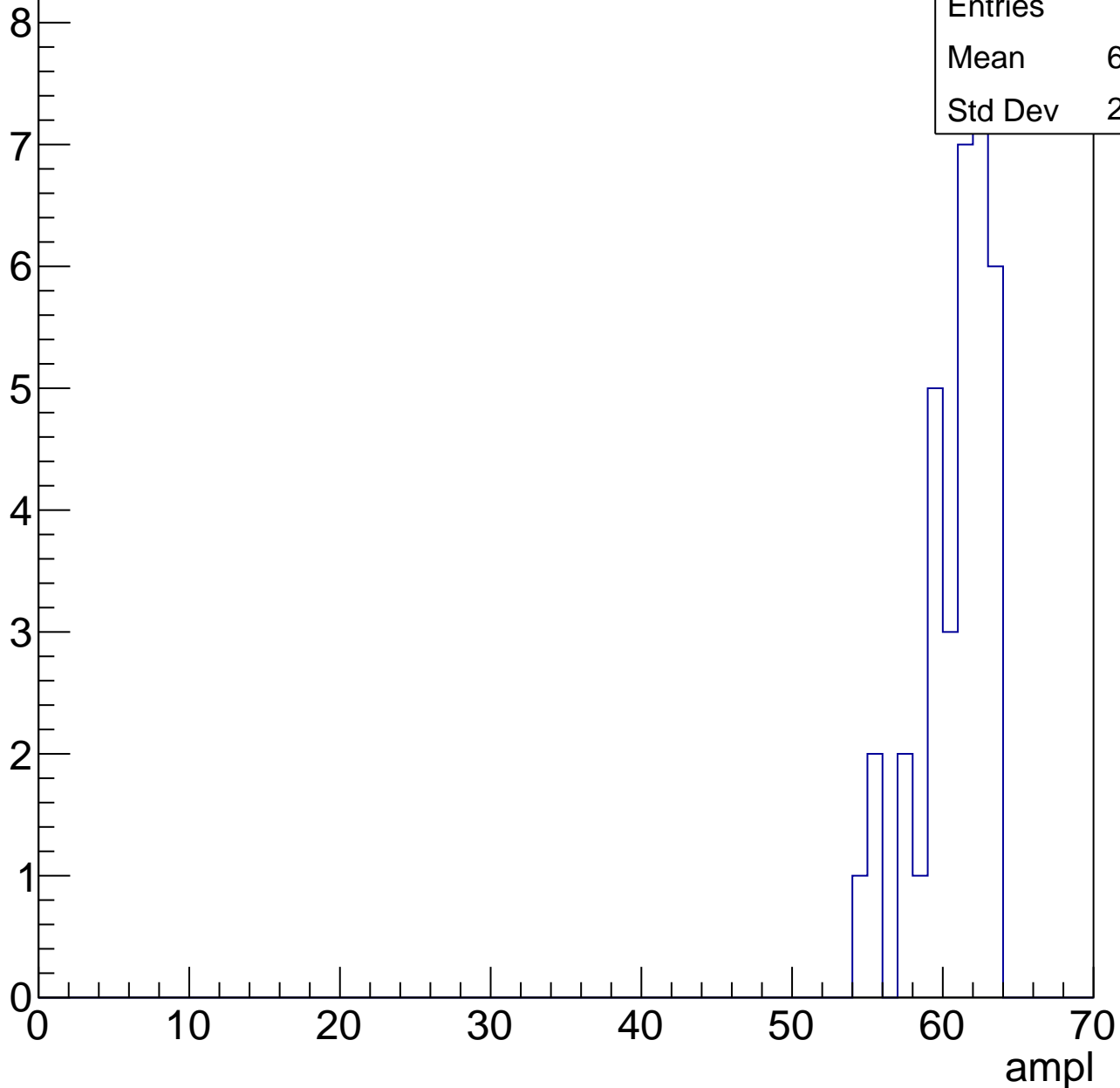


# B0L001S, U21-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

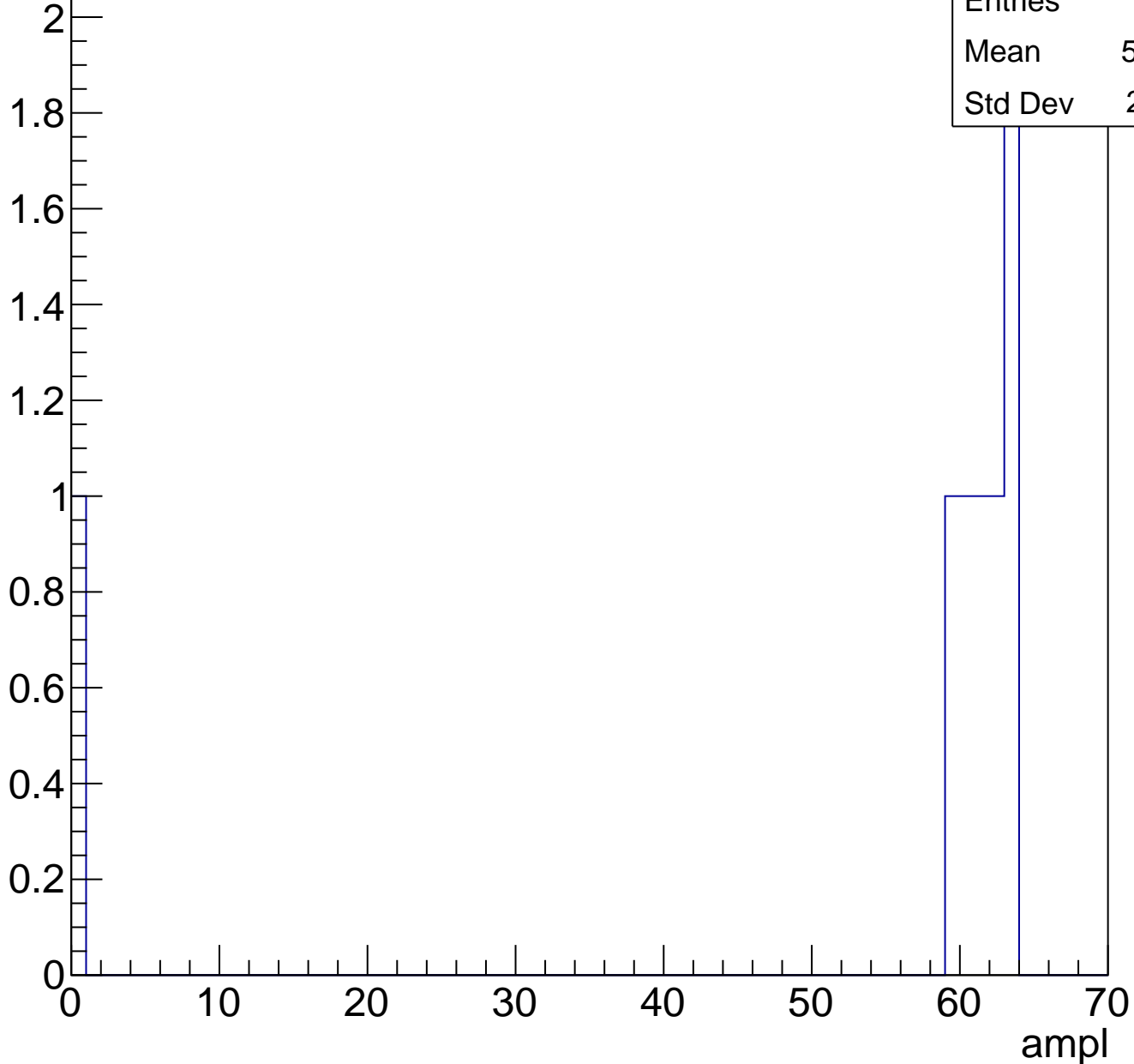
Entries	35
Mean	60.34
Std Dev	2.402



# B0L001S, U21-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	8
Std Dev	11.31

# B0L001S, U21-ch67, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	76
Mean	31.04
Std Dev	6.265

**Gaus mean : 32.1608**

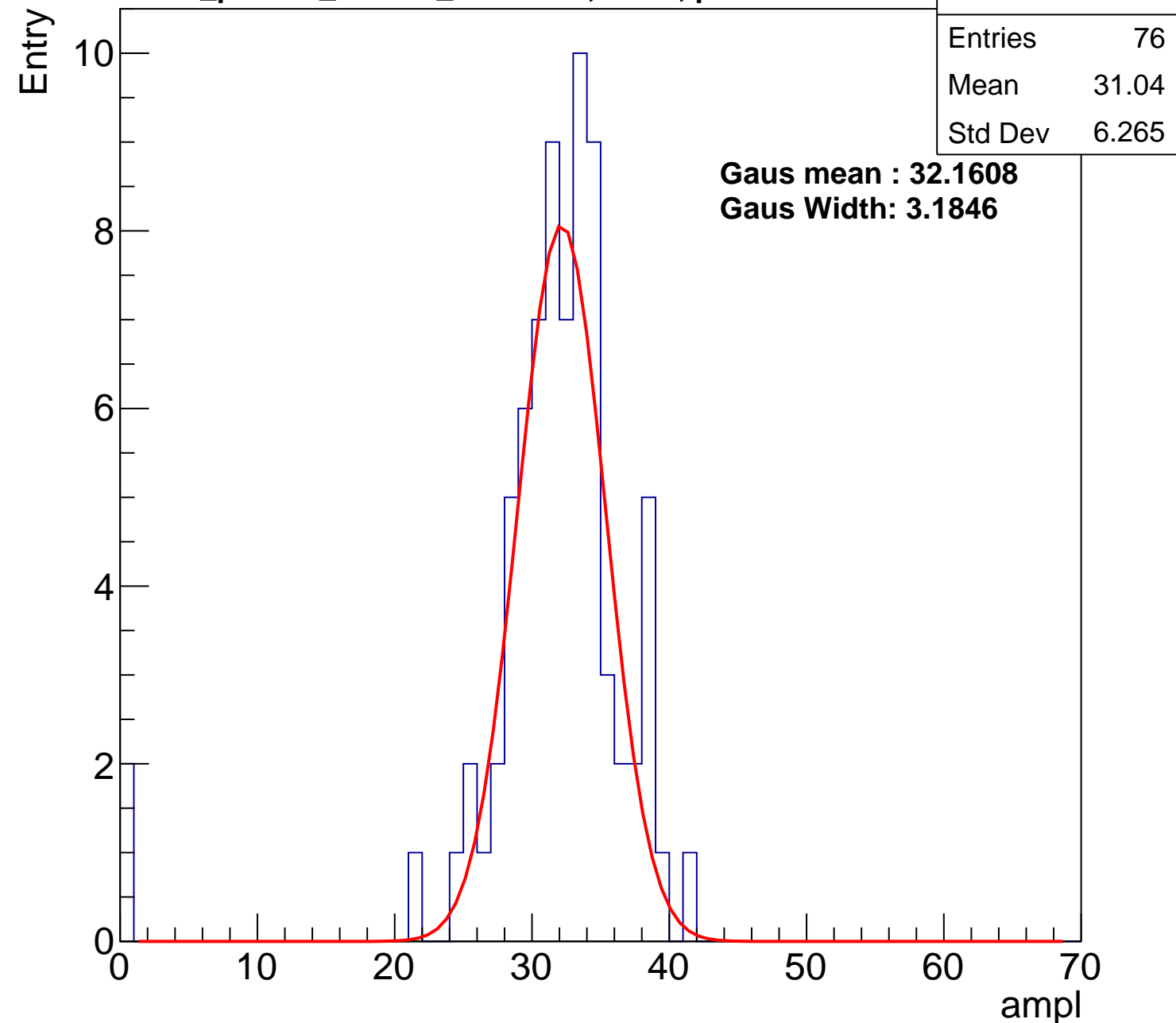
**Gaus Width: 3.1846**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U21-ch67, adc1

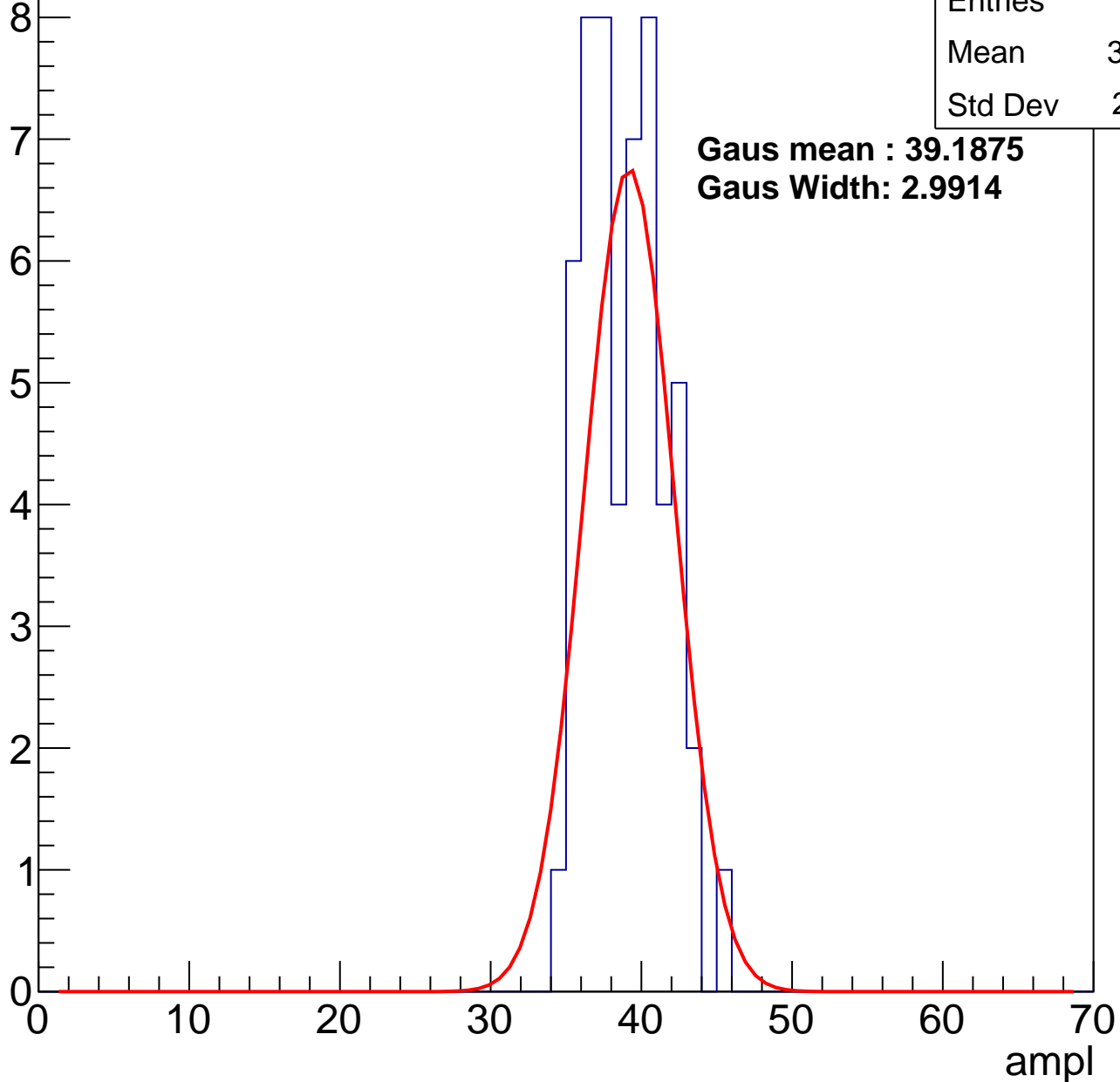
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	38.48
Std Dev	2.551

**Gaus mean : 39.1875**

**Gaus Width: 2.9914**



# B0L001S, U21-ch67, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	45.06
Std Dev	3.112

**Gaus mean : 45.7913**

**Gaus Width: 3.6761**

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

0

2

4

6

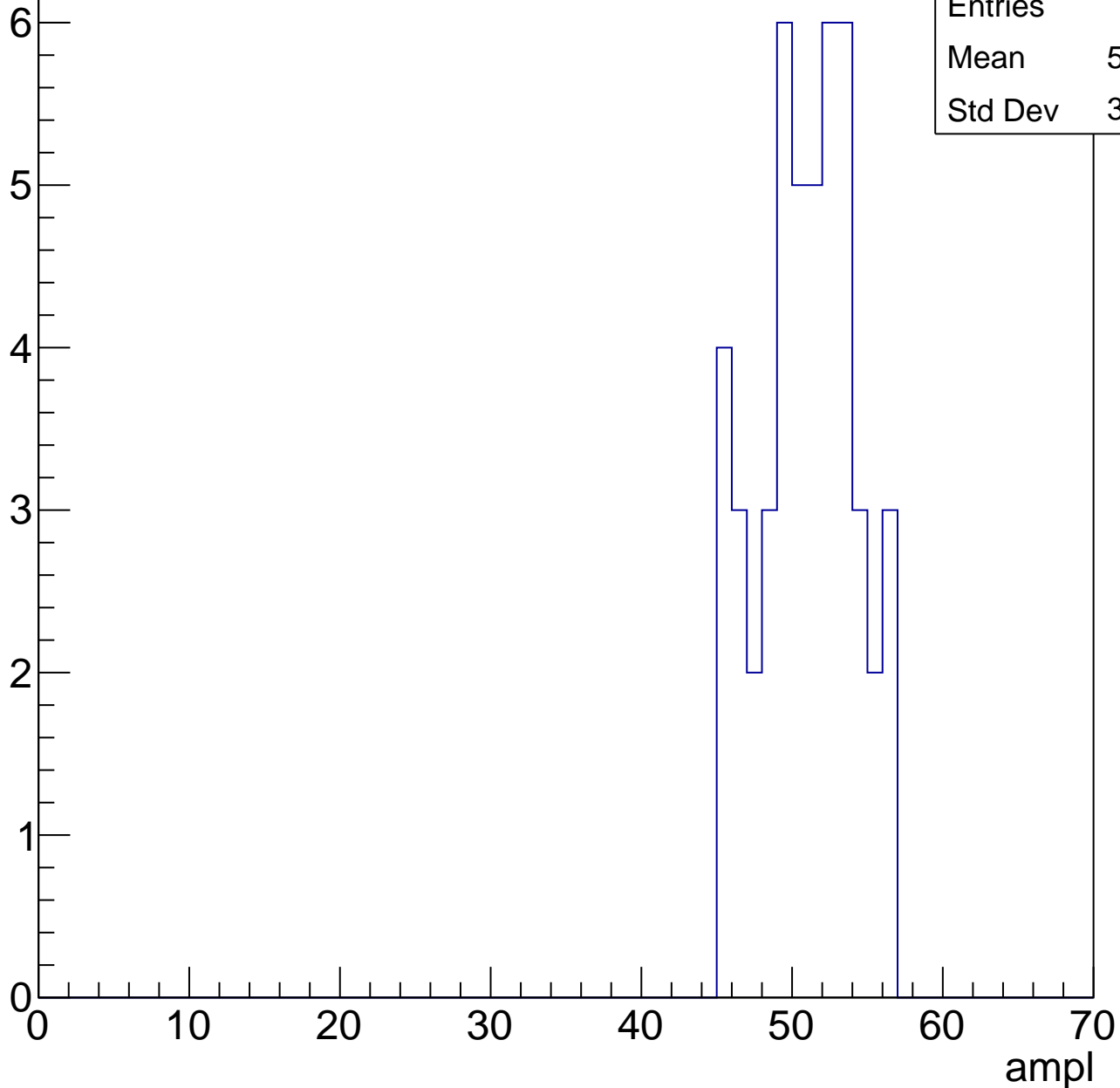
8

10

# B0L001S, U21-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

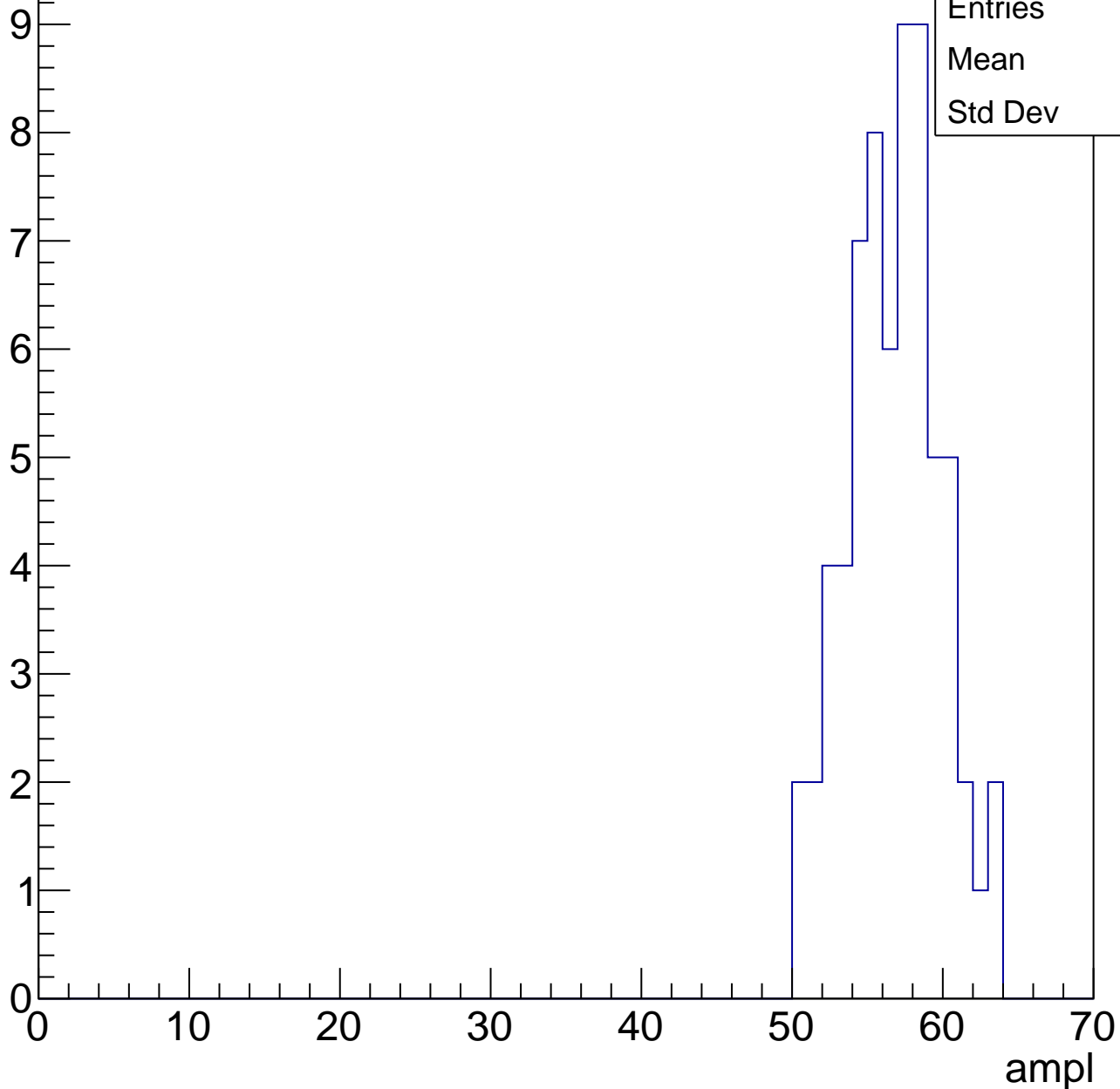
Entry



# B0L001S, U21-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

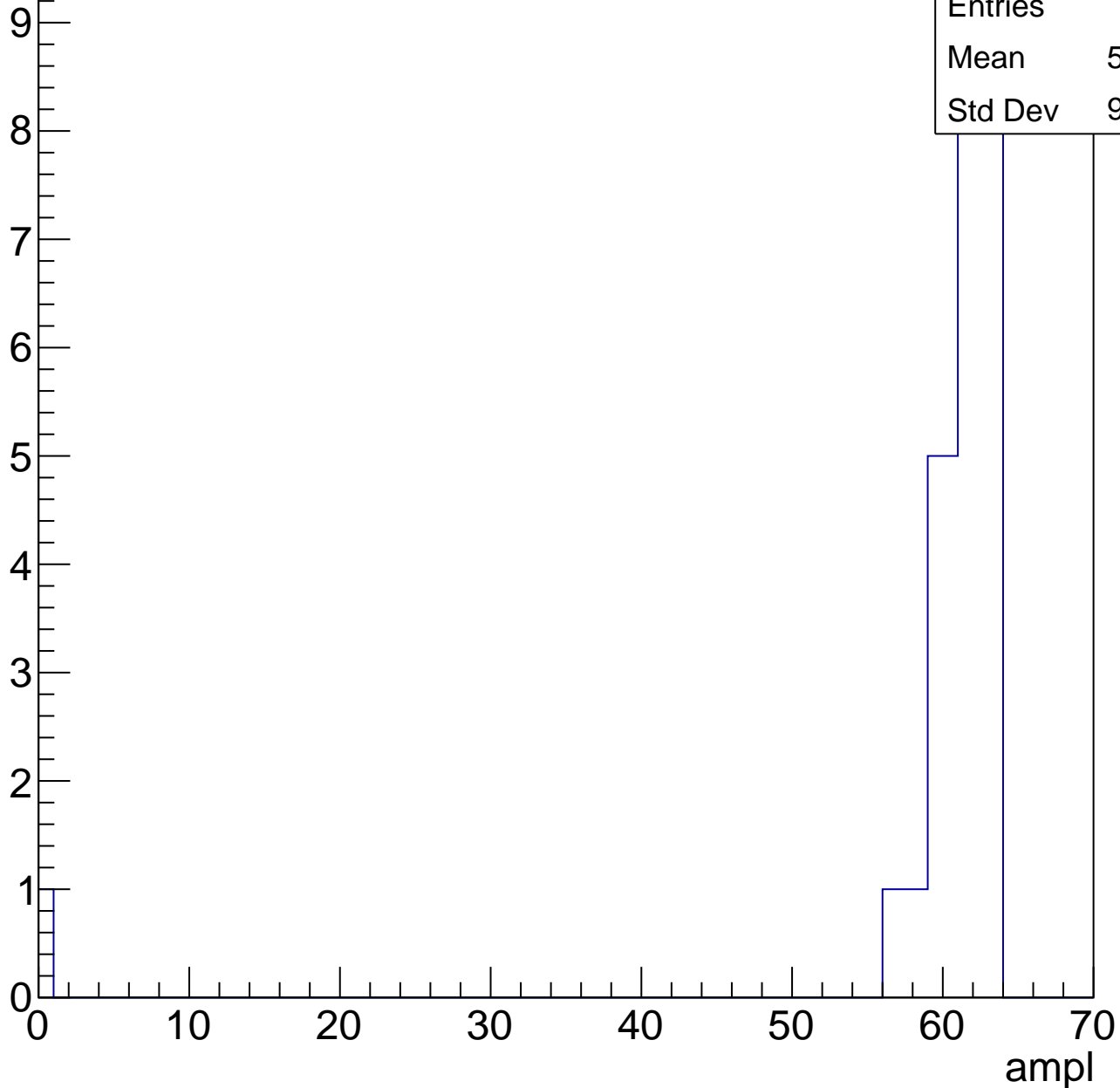


Entries	66
Mean	56.3
Std Dev	3.03

# B0L001S, U21-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U21-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U21-ch68, adc0

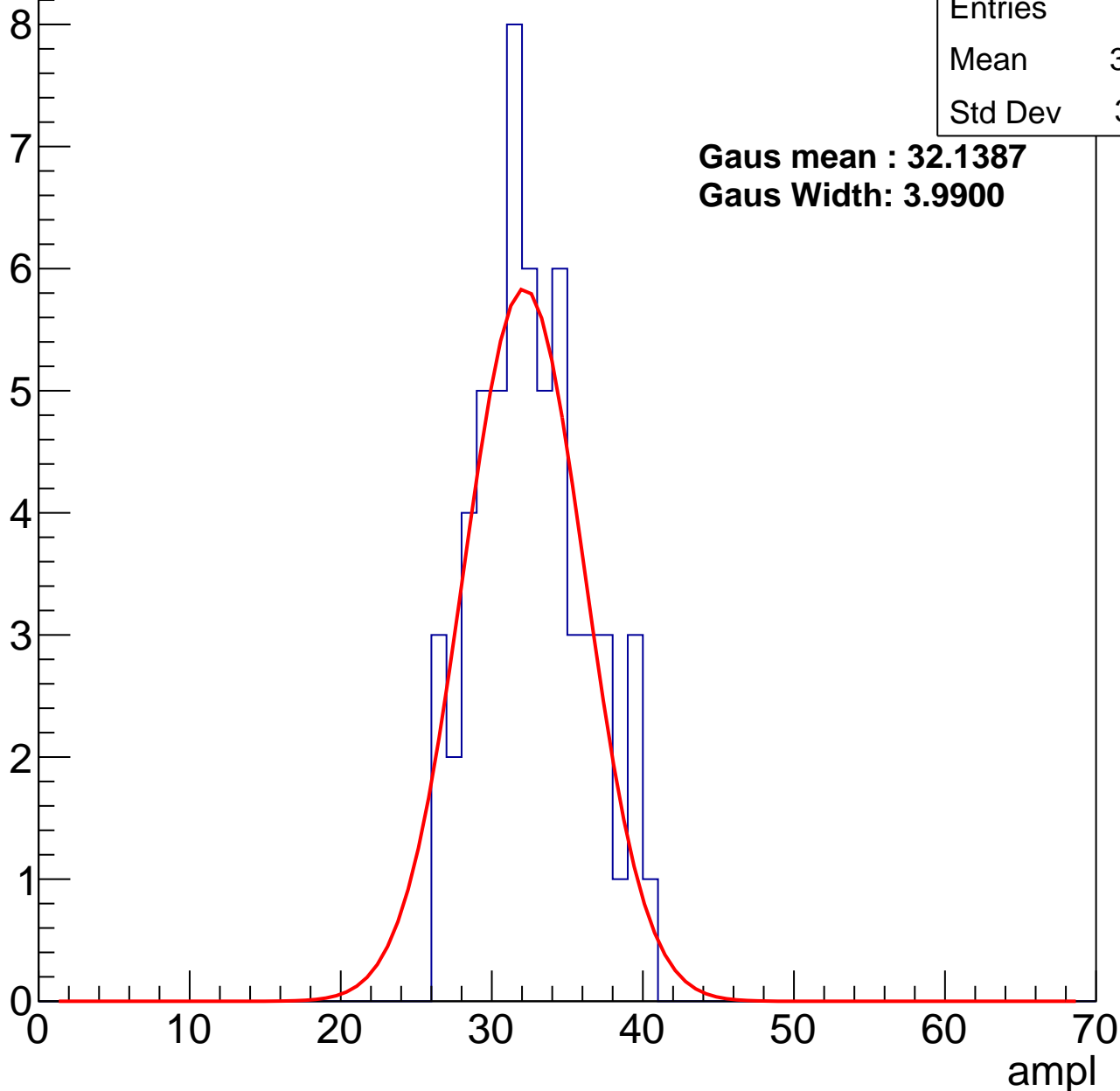
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	32.19
Std Dev	3.521

**Gaus mean : 32.1387**

**Gaus Width: 3.9900**



# B0L001S, U21-ch68, adc1

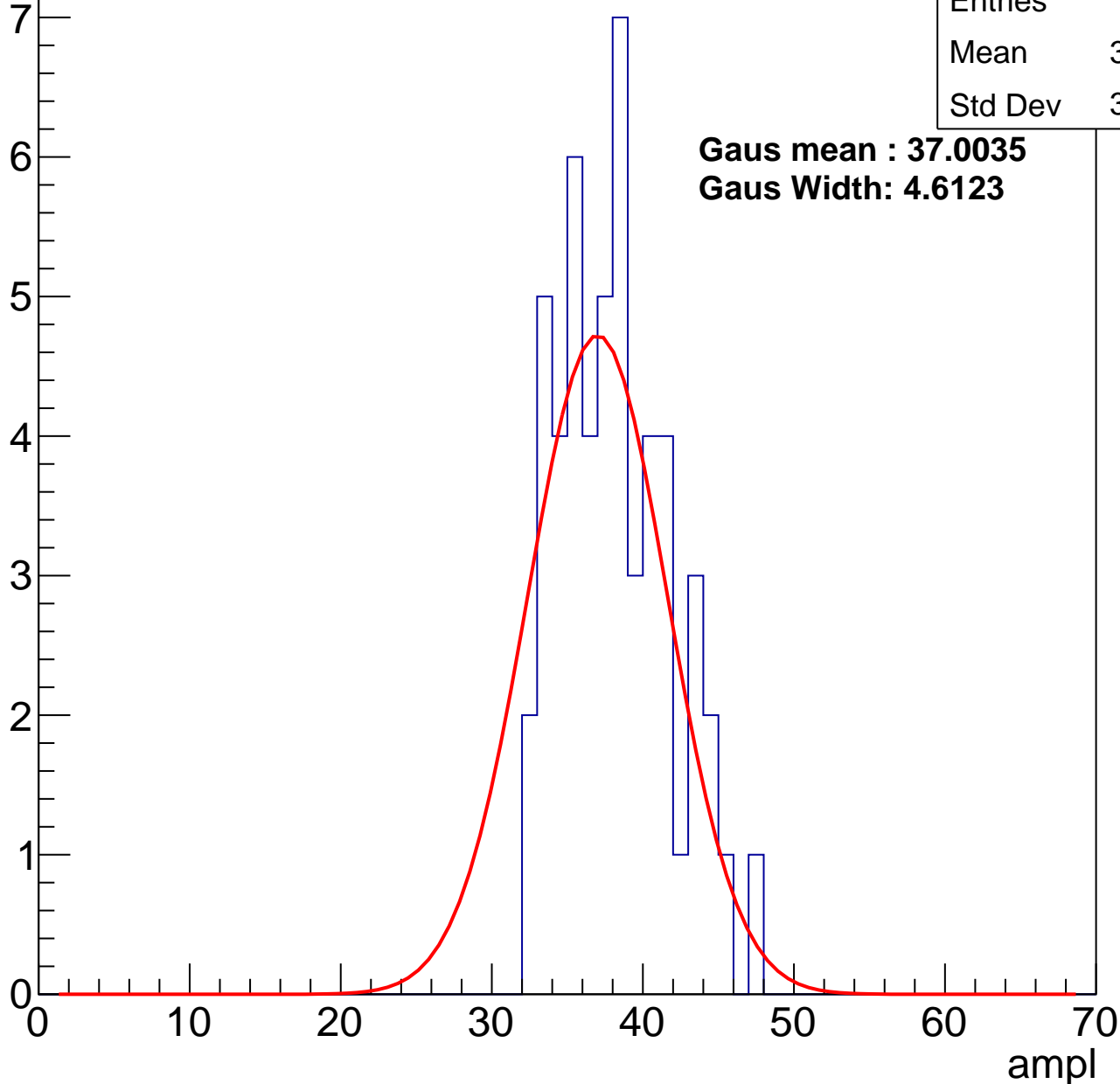
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	37.73
Std Dev	3.617

**Gaus mean : 37.0035**

**Gaus Width: 4.6123**



# B0L001S, U21-ch68, adc2

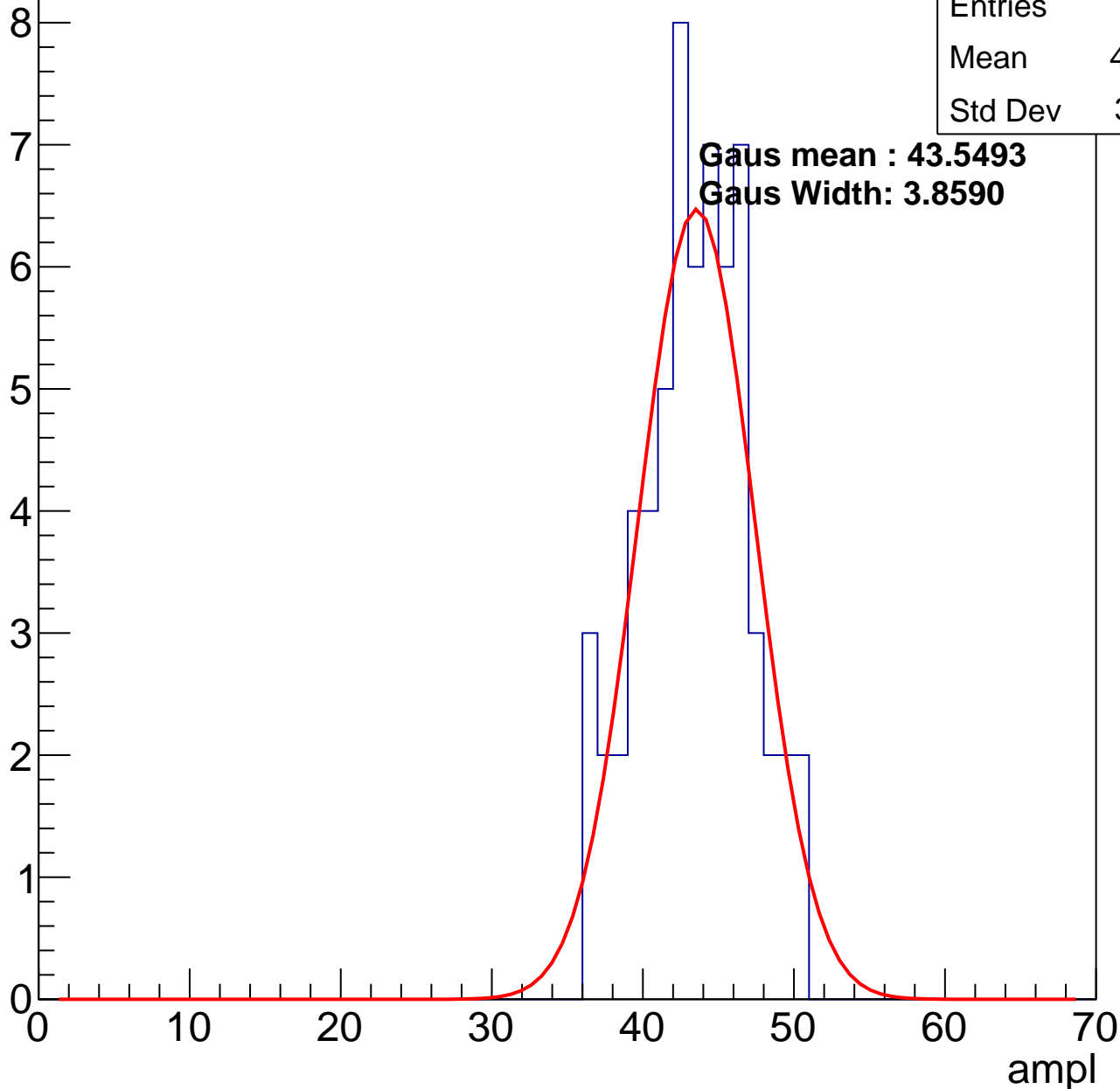
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	42.98
Std Dev	3.471

**Gaus mean : 43.5493**

**Gaus Width: 3.8590**

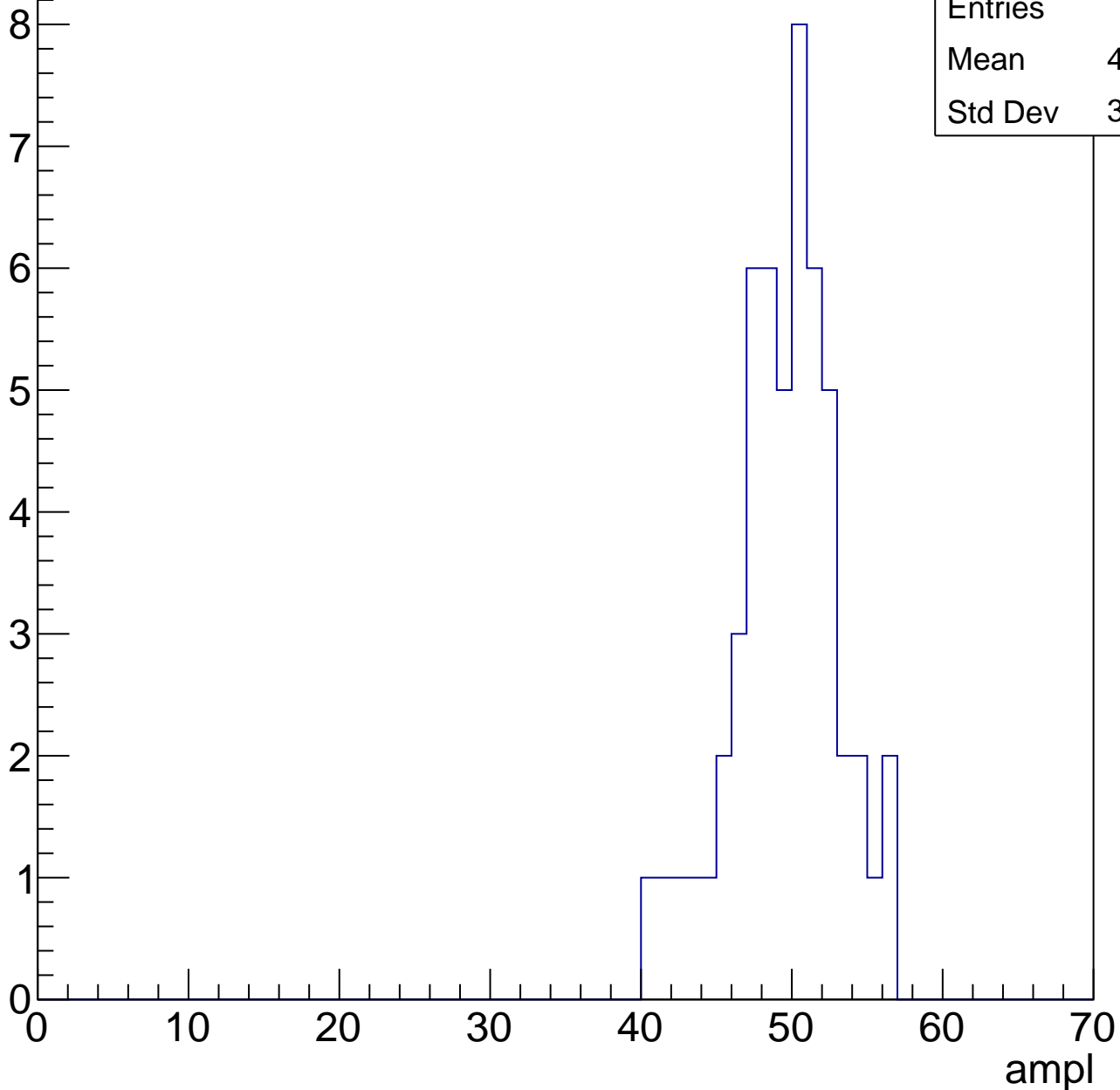


# B0L001S, U21-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

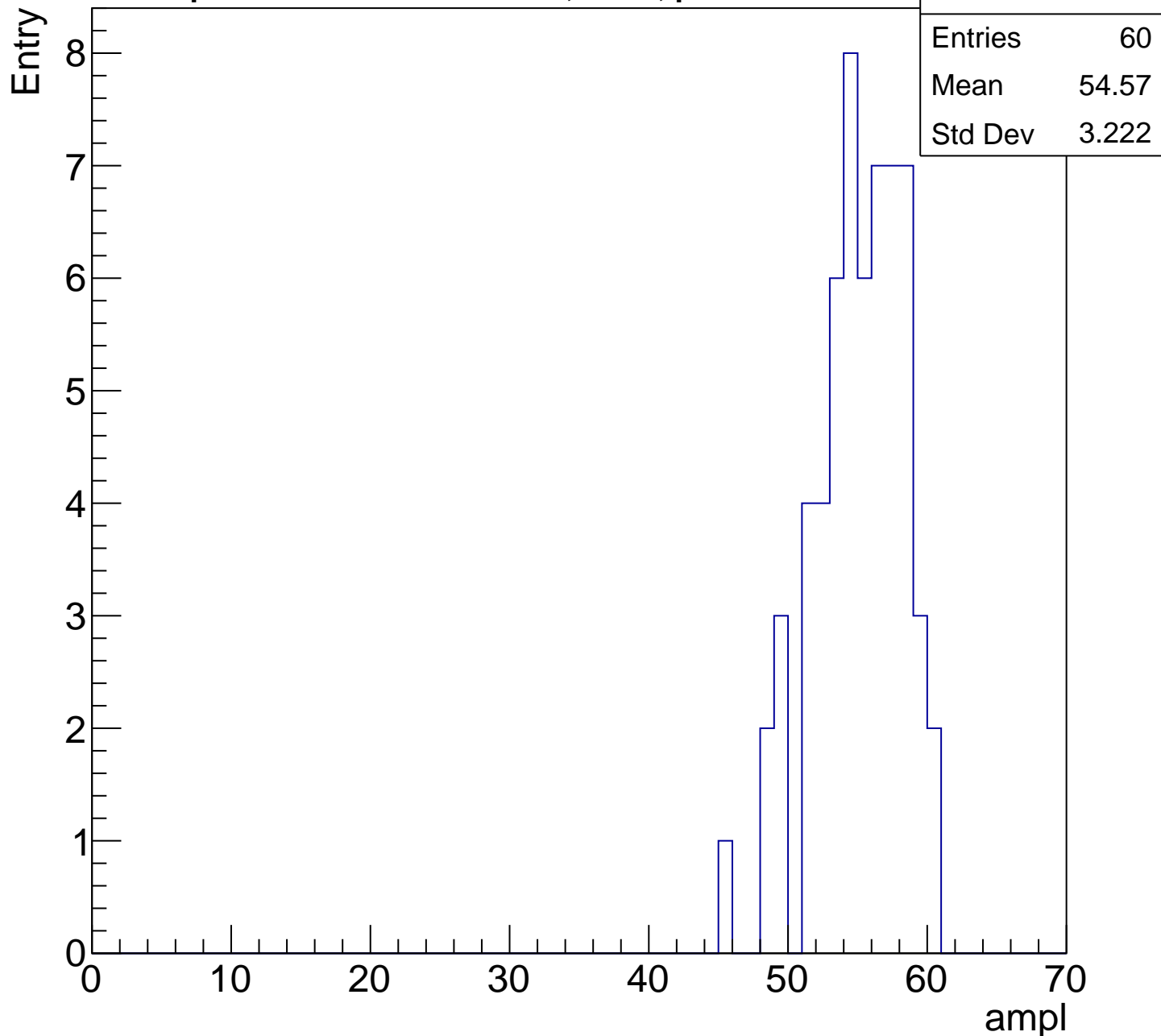
Entry

Entries	53
Mean	49.06
Std Dev	3.466



# B0L001S, U21-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U21-ch68, adc5

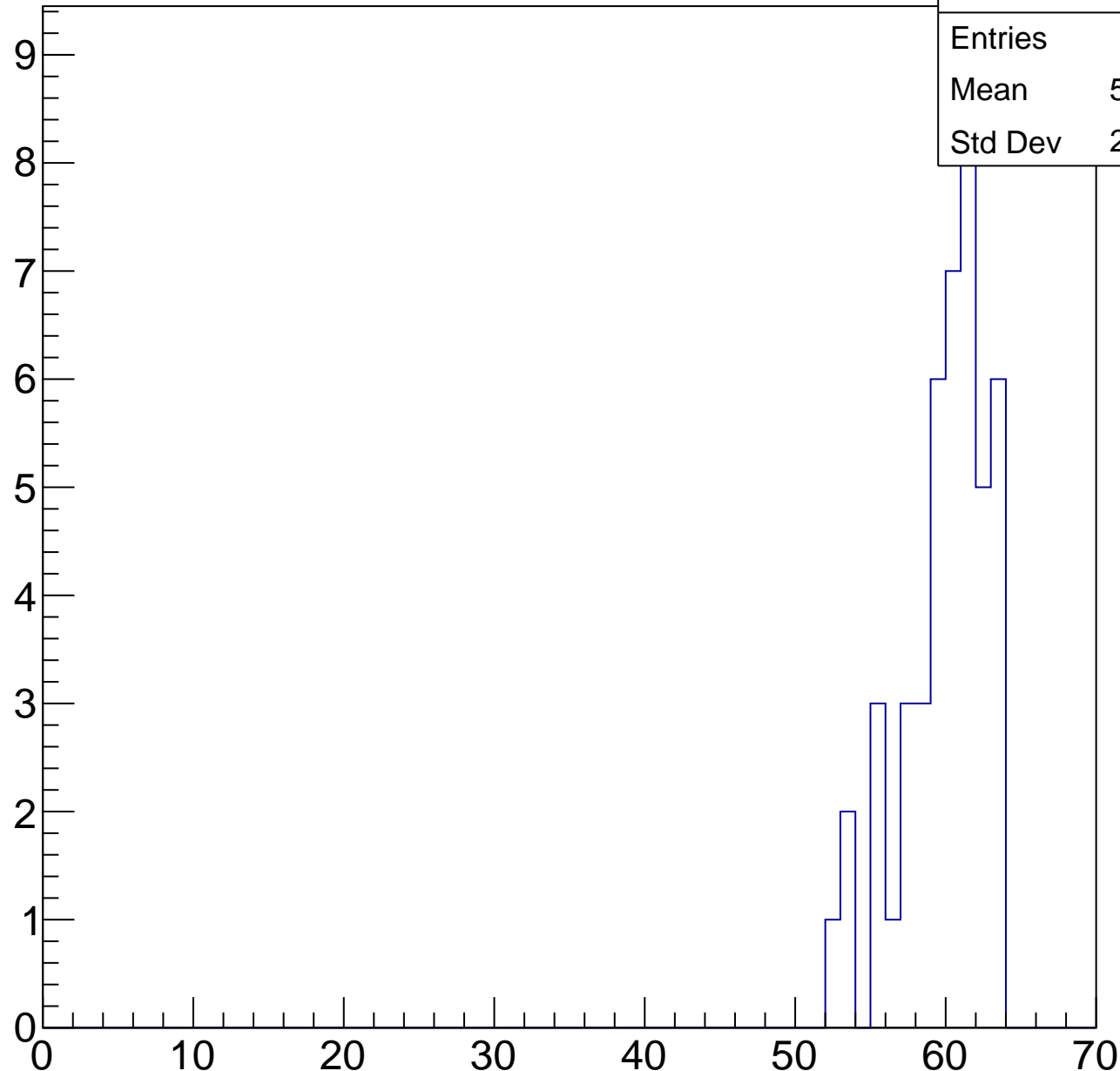
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	46
Mean	59.46
Std Dev	2.826

ampl

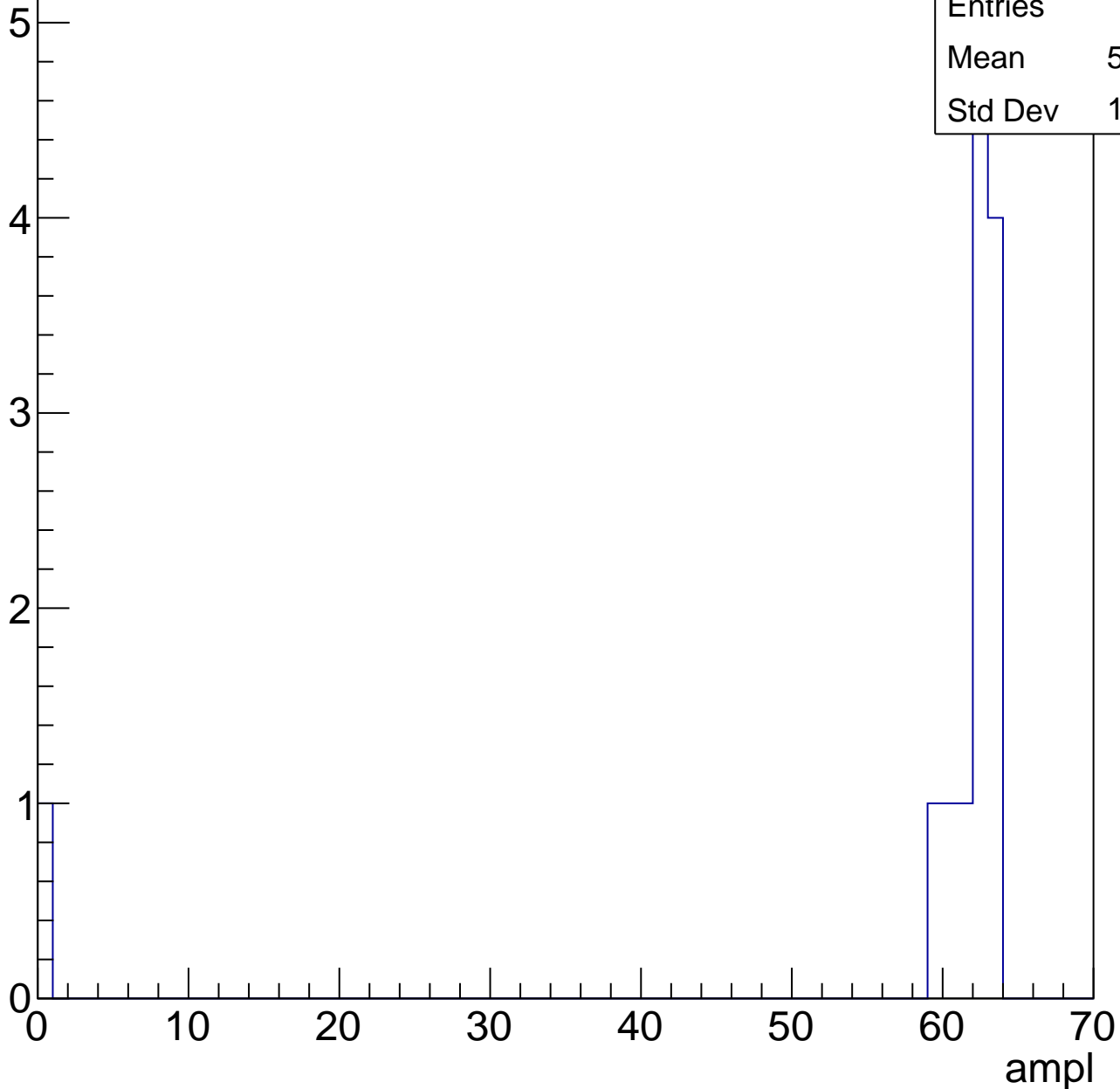


# B0L001S, U21-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	13
Mean	57.08
Std Dev	16.52





# B0L001S, U21-ch68, adc7

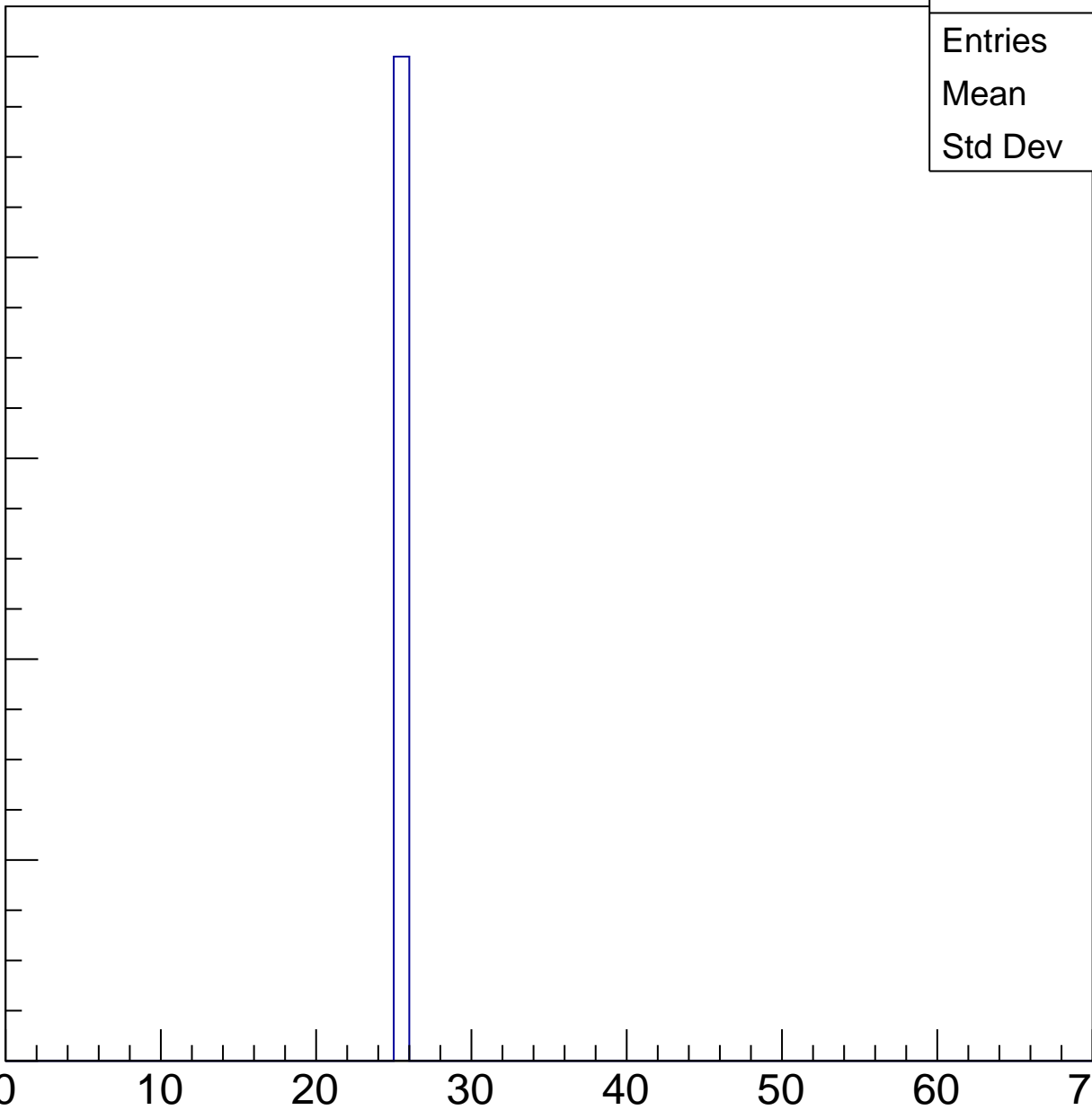
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	25
Std Dev	0

ampl



# B0L001S, U21-ch69, adc0

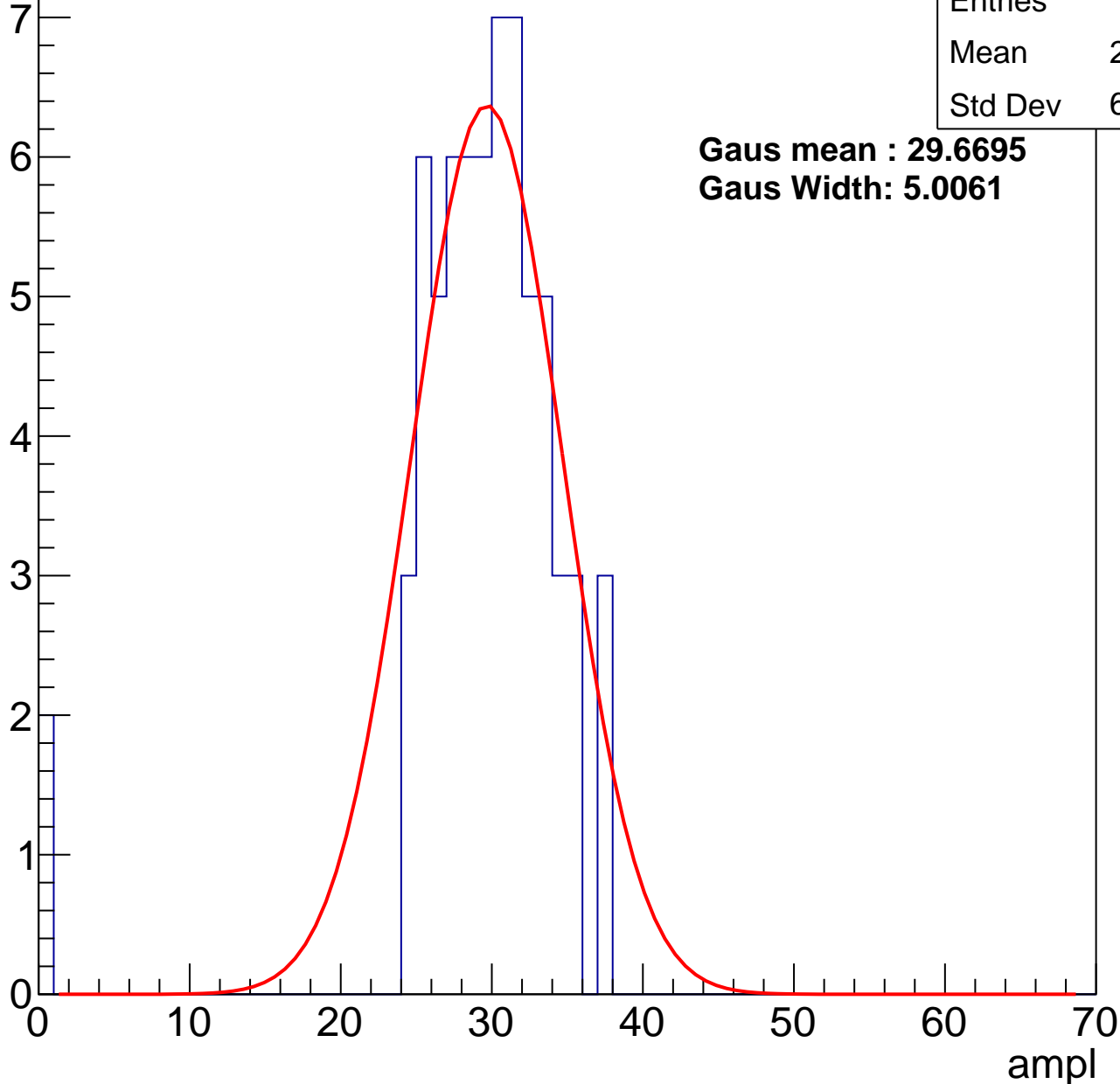
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	28.75
Std Dev	6.058

**Gaus mean : 29.6695**

**Gaus Width: 5.0061**



# B0L001S, U21-ch69, adc1

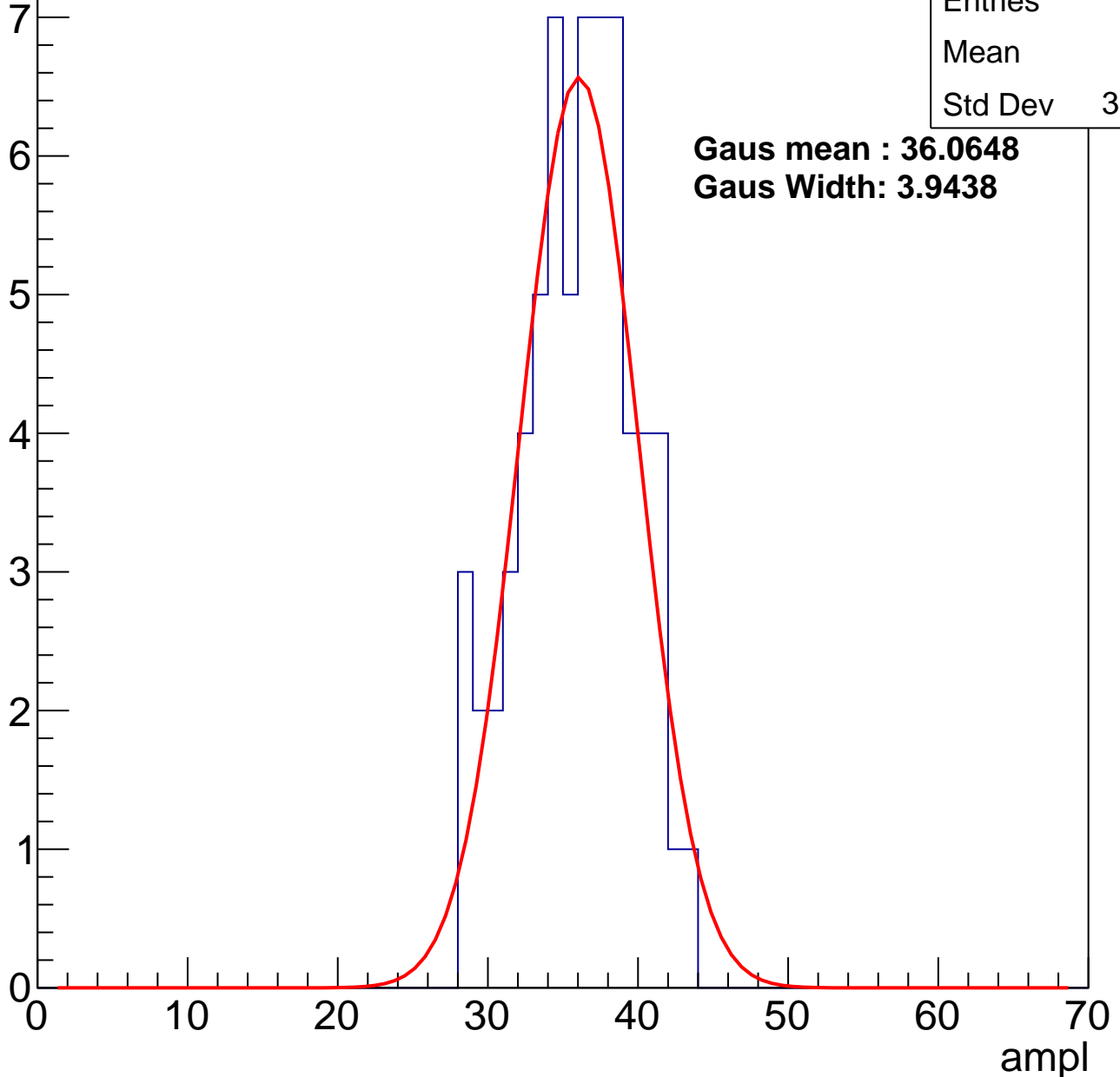
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	35.5
Std Dev	3.657

**Gaus mean : 36.0648**

**Gaus Width: 3.9438**



# B0L001S, U21-ch69, adc2

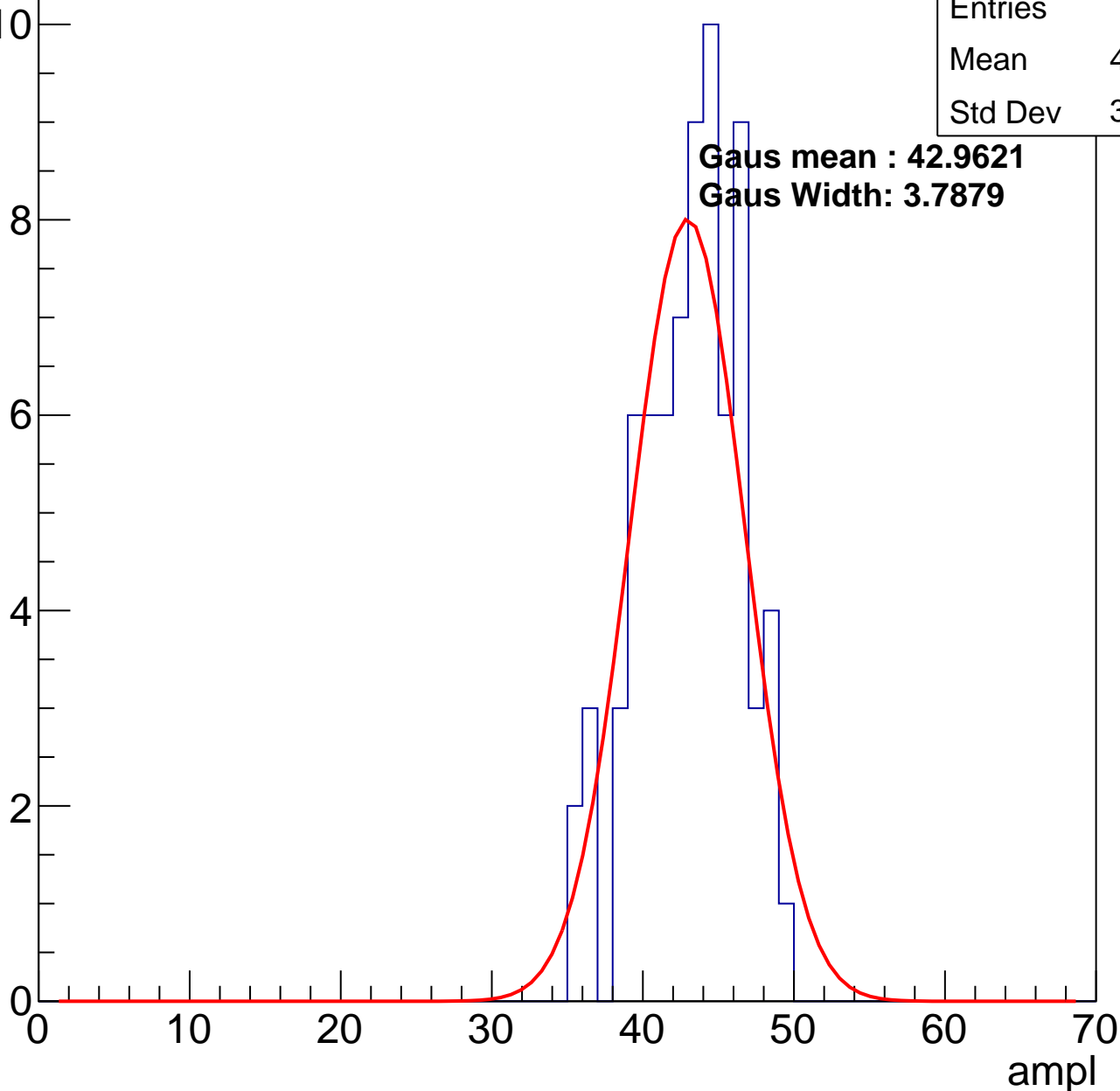
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	42.65
Std Dev	3.309

**Gaus mean : 42.9621**

**Gaus Width: 3.7879**

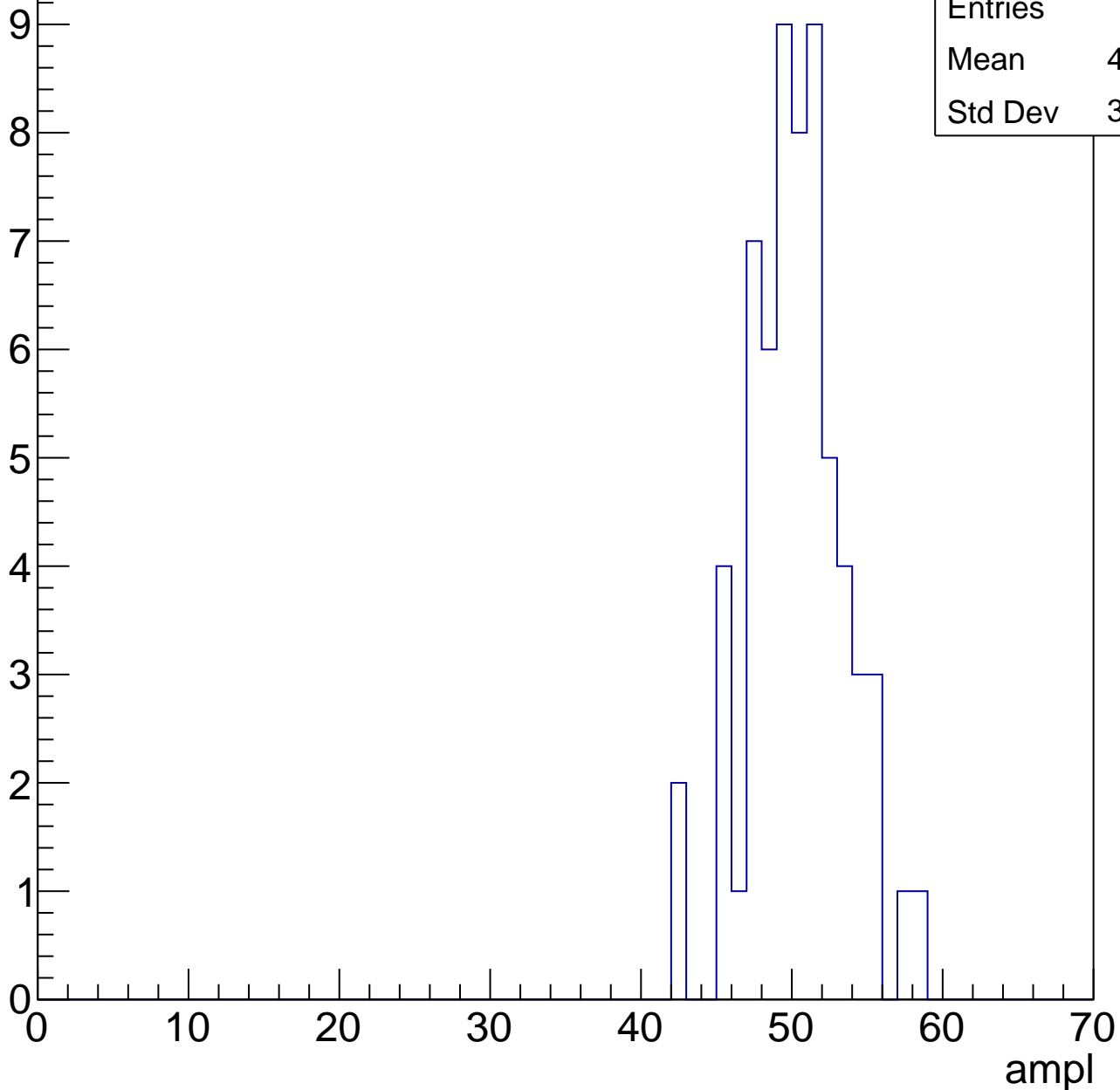


# B0L001S, U21-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	49.86
Std Dev	3.187

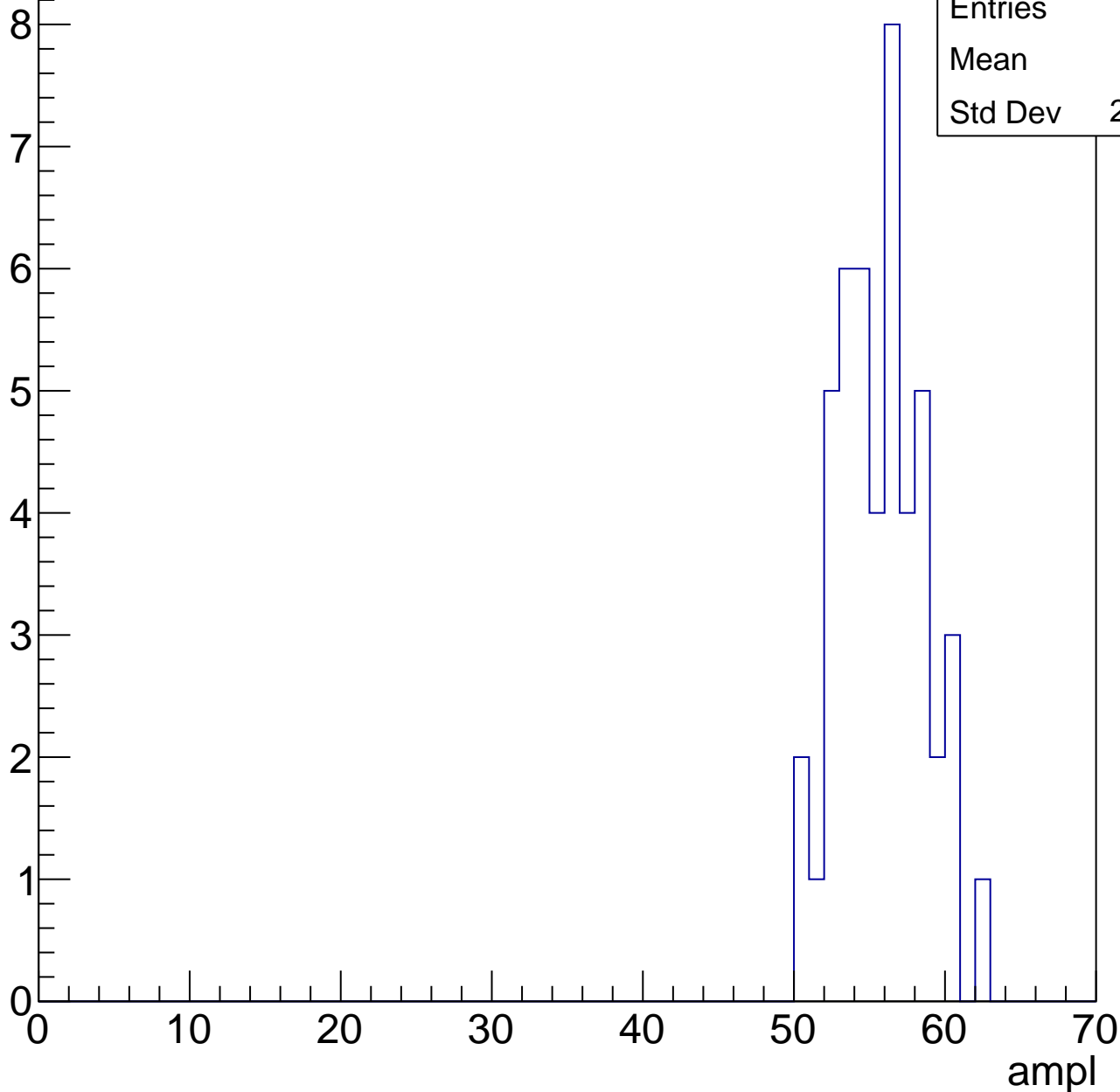


# B0L001S, U21-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	55.3
Std Dev	2.775



# B0L001S, U21-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

10

8

6

4

2

0

0

10

20

30

40

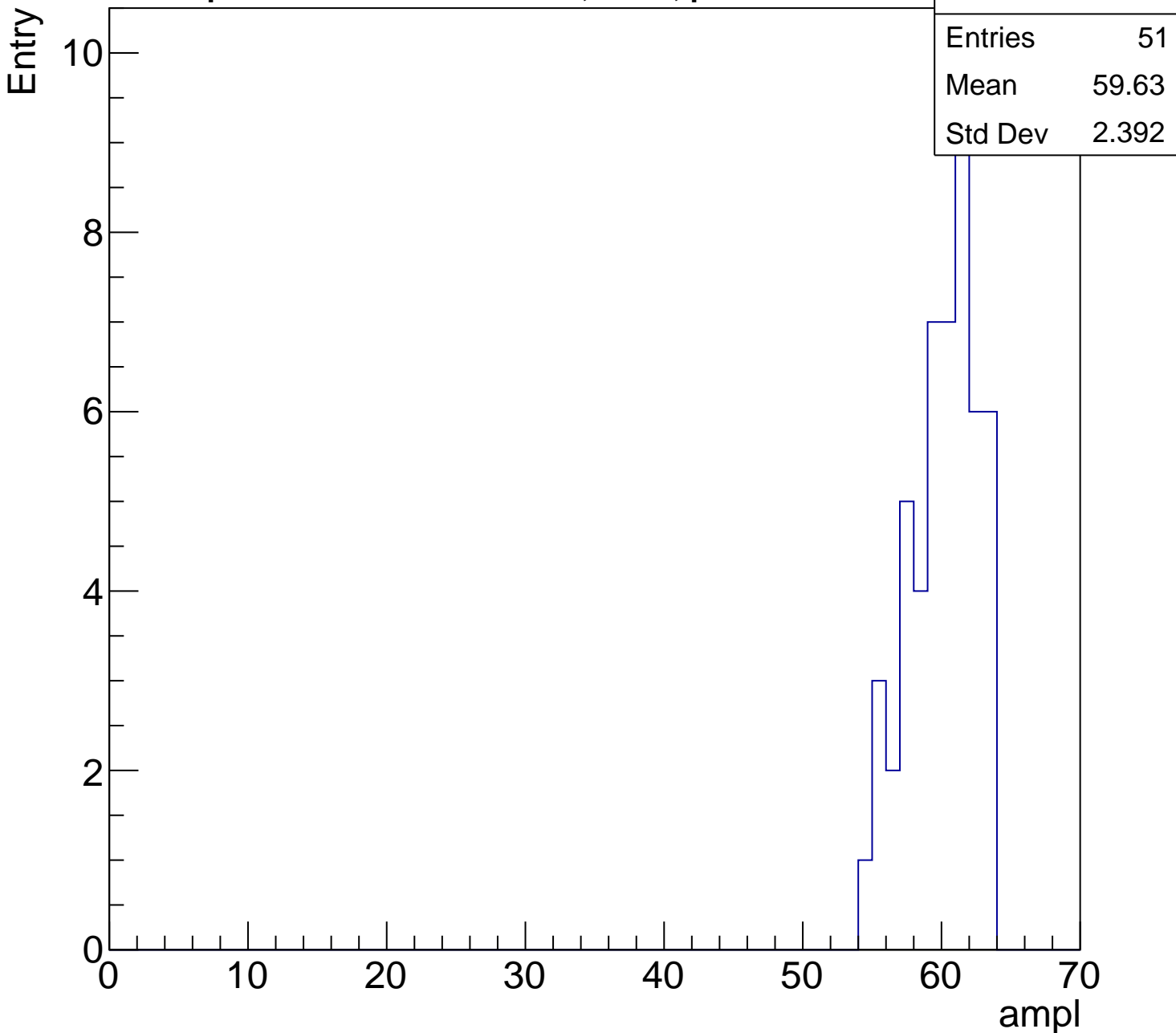
50

60

70

ampl

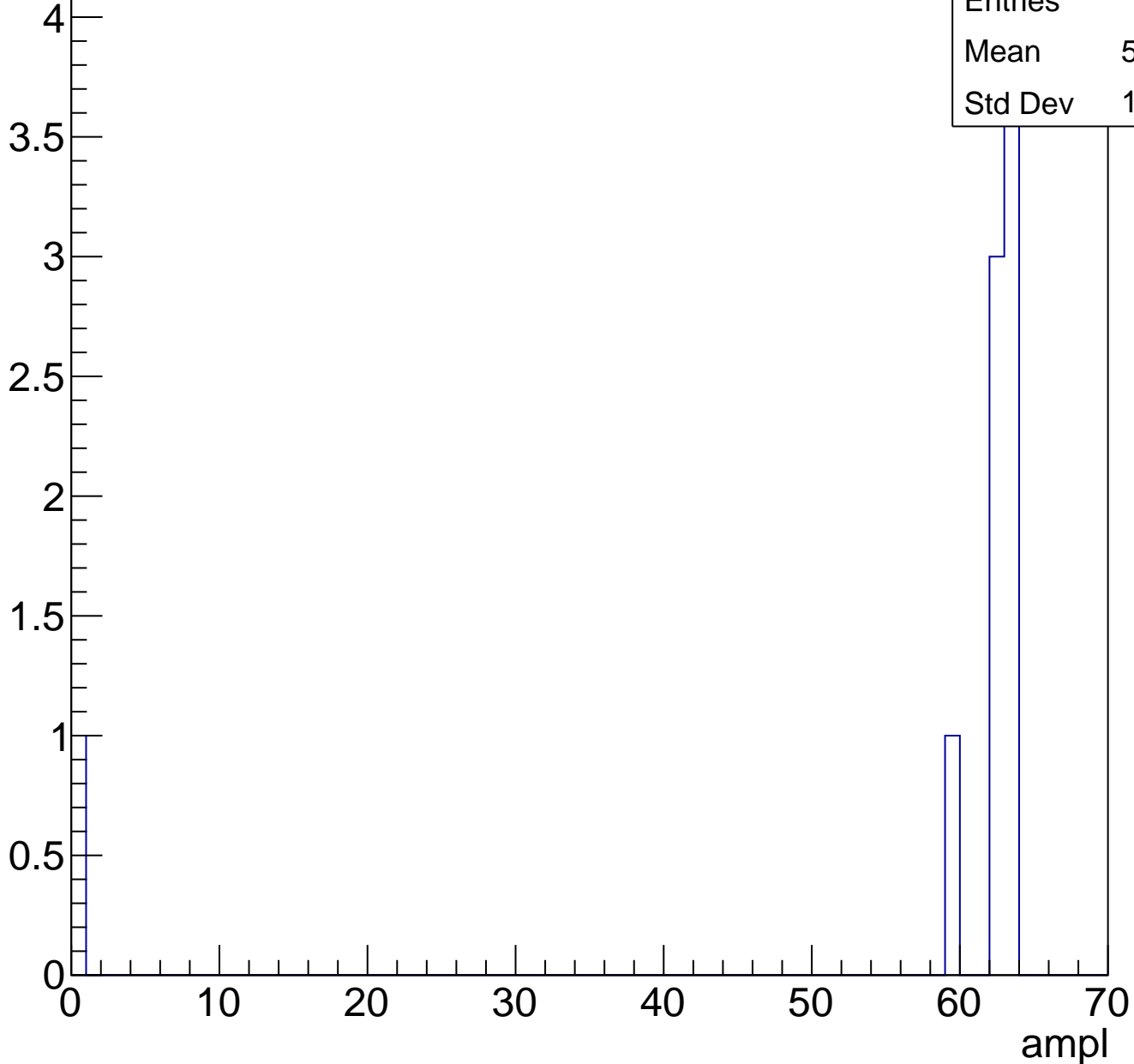
Entries	51
Mean	59.63
Std Dev	2.392



# B0L001S, U21-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch70, adc0

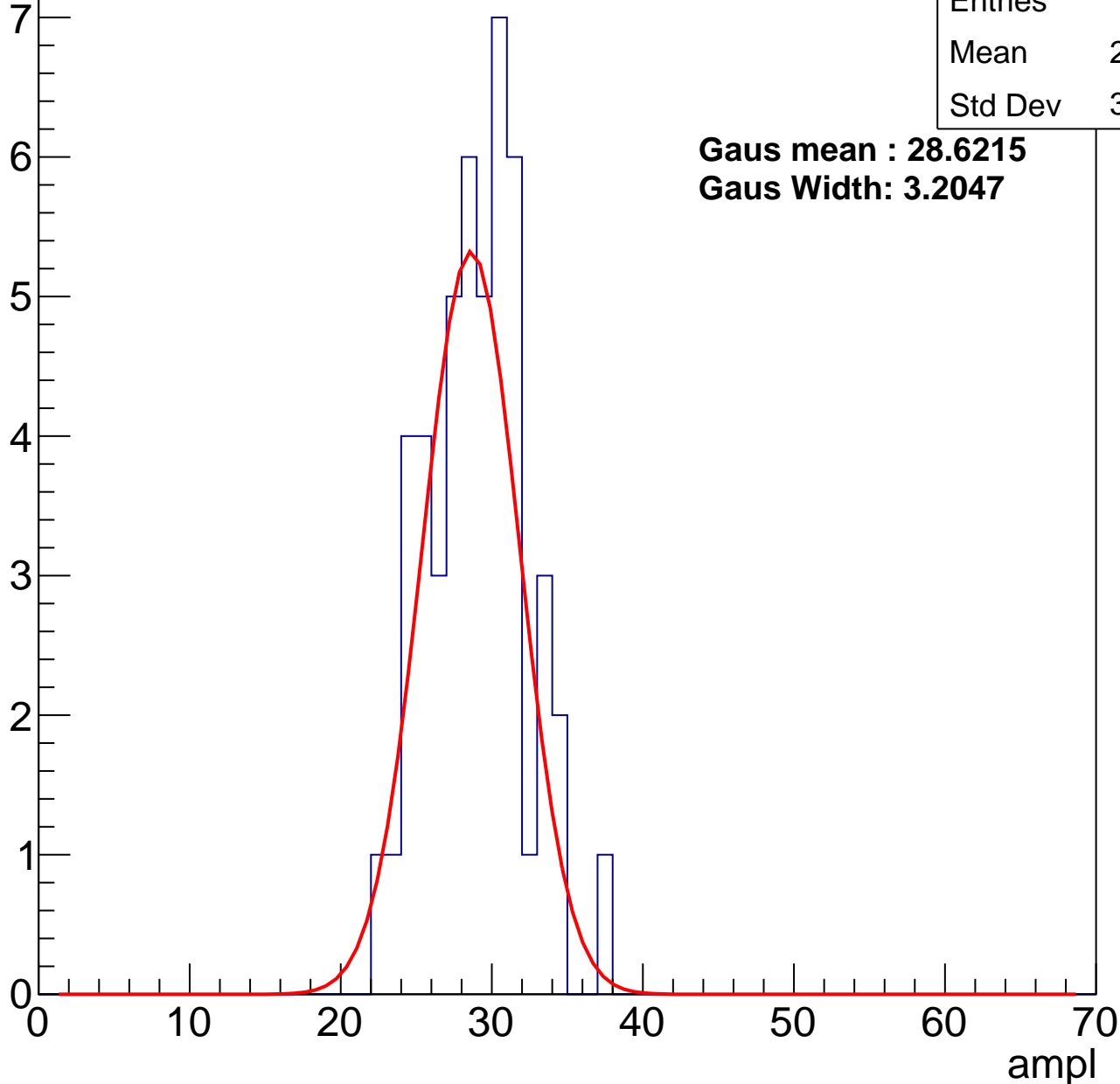
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	28.55
Std Dev	3.176

**Gaus mean : 28.6215**

**Gaus Width: 3.2047**



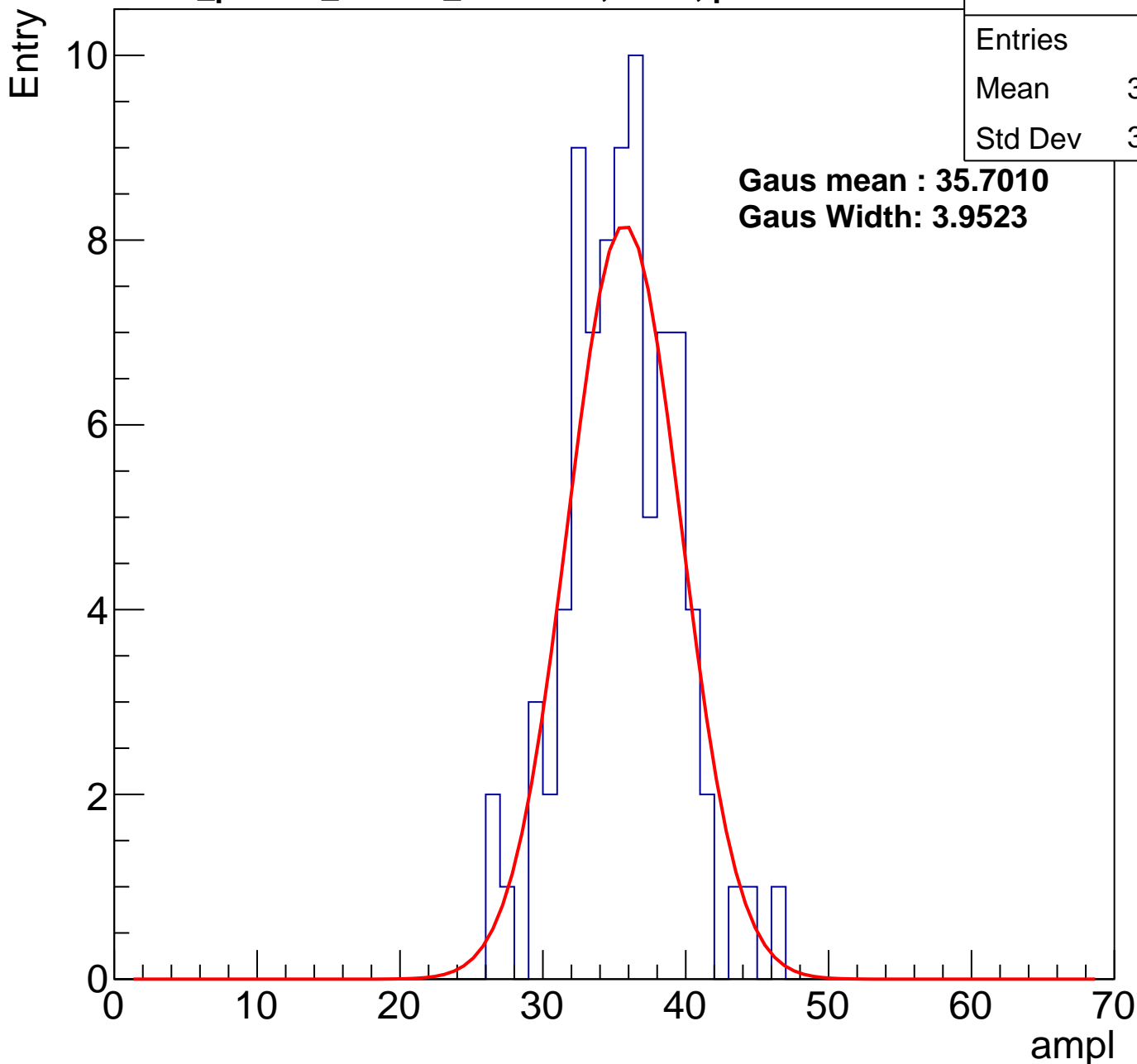
# B0L001S, U21-ch70, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	83
Mean	35.12
Std Dev	3.813

**Gaus mean : 35.7010**

**Gaus Width: 3.9523**



# B0L001S, U21-ch70, adc2

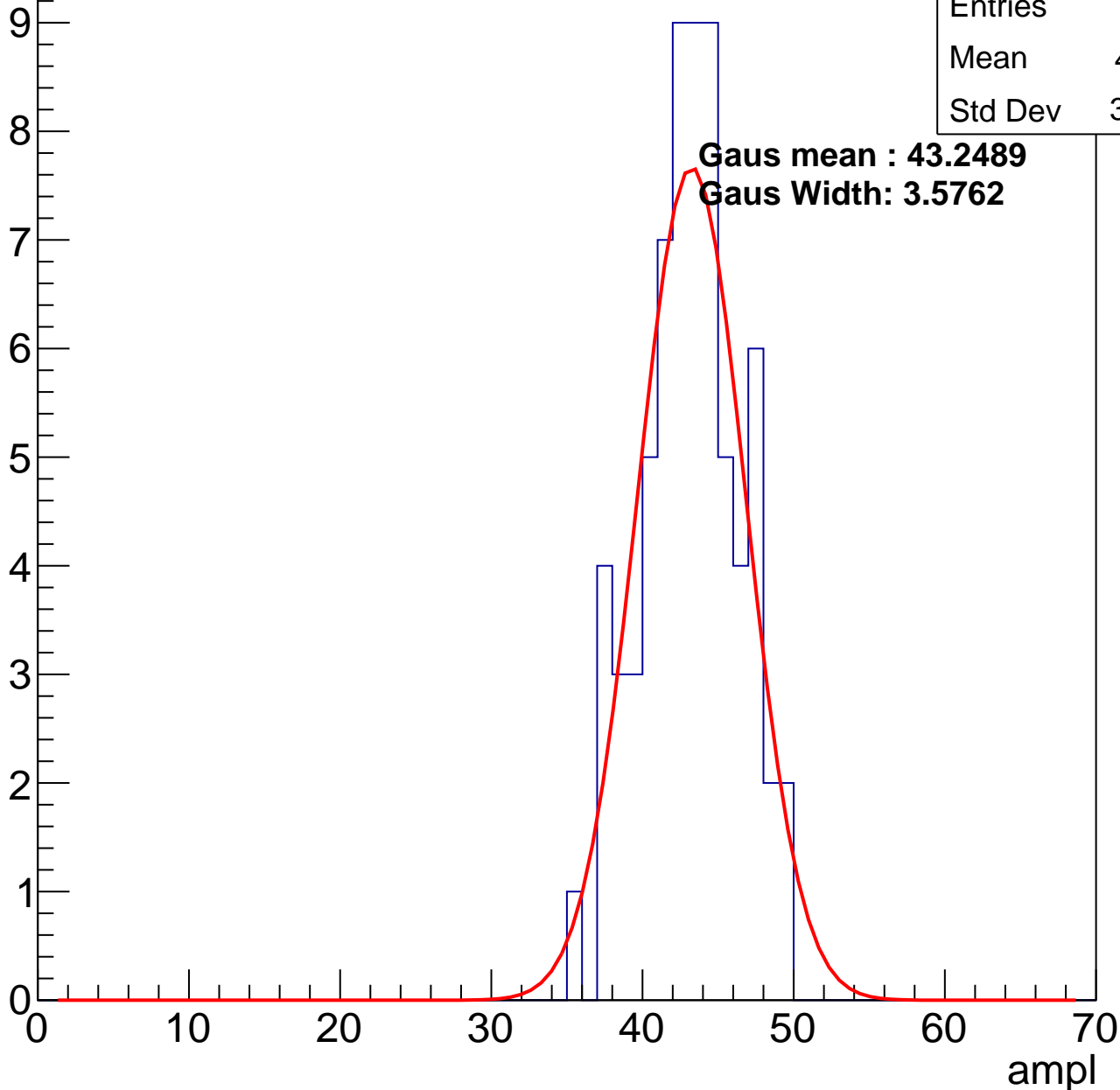
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	42.71
Std Dev	3.163

**Gaus mean : 43.2489**

**Gaus Width: 3.5762**



# B0L001S, U21-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	67
Mean	49.58
Std Dev	3.49

Entry

10

8

6

4

2

0

0

10

20

30

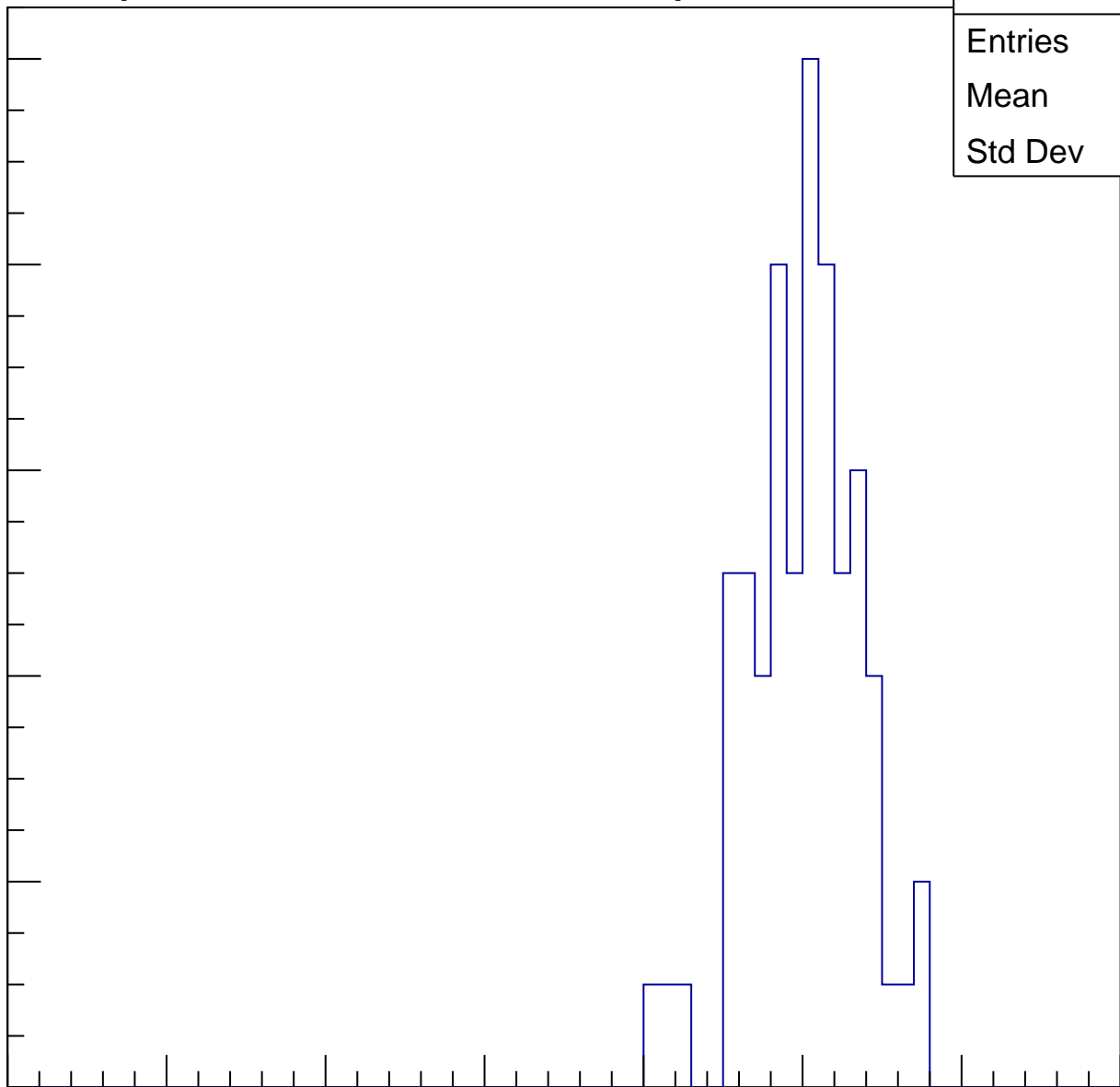
40

50

60

70

ampl

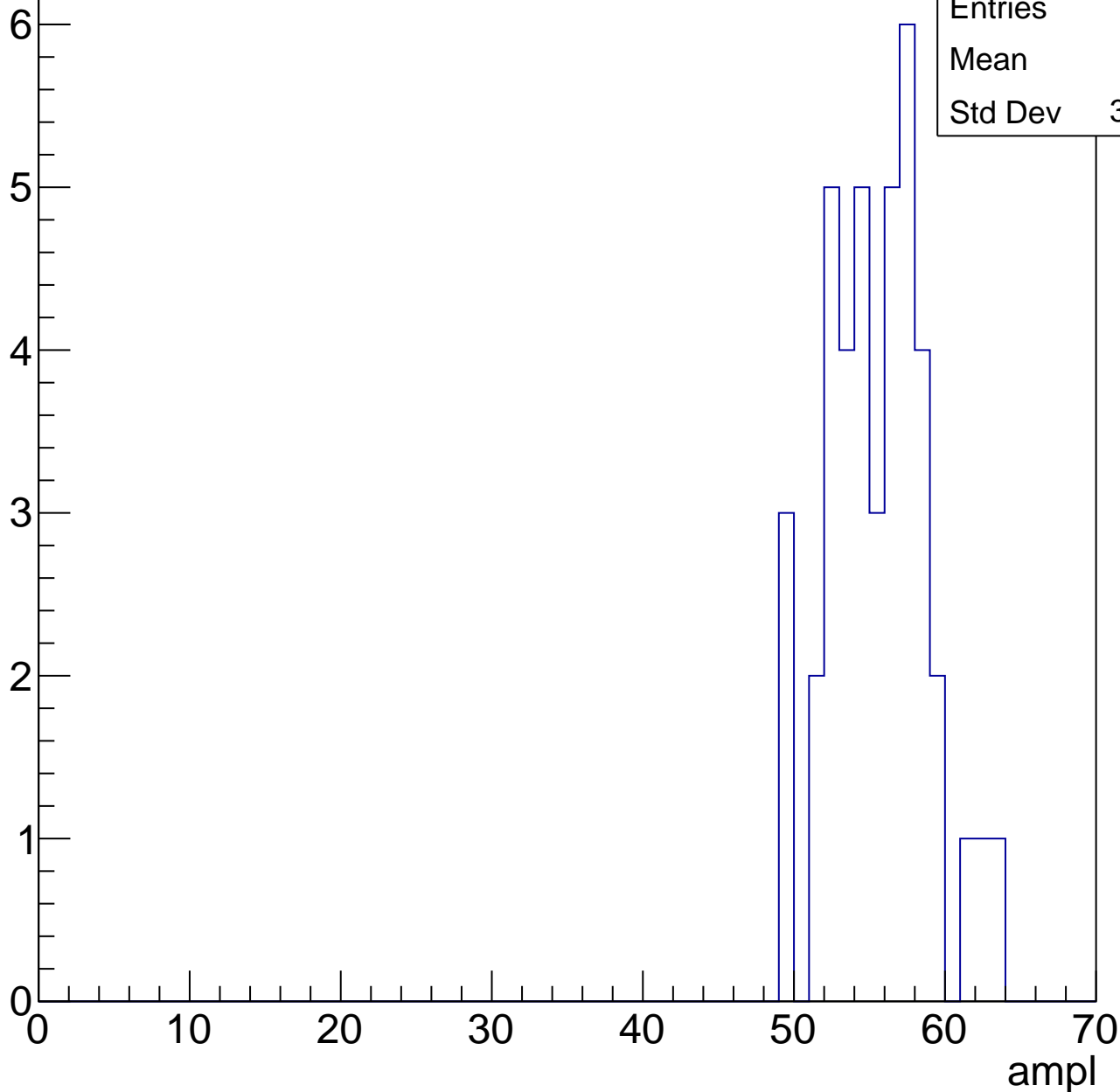


# B0L001S, U21-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	42
Mean	55.1
Std Dev	3.279

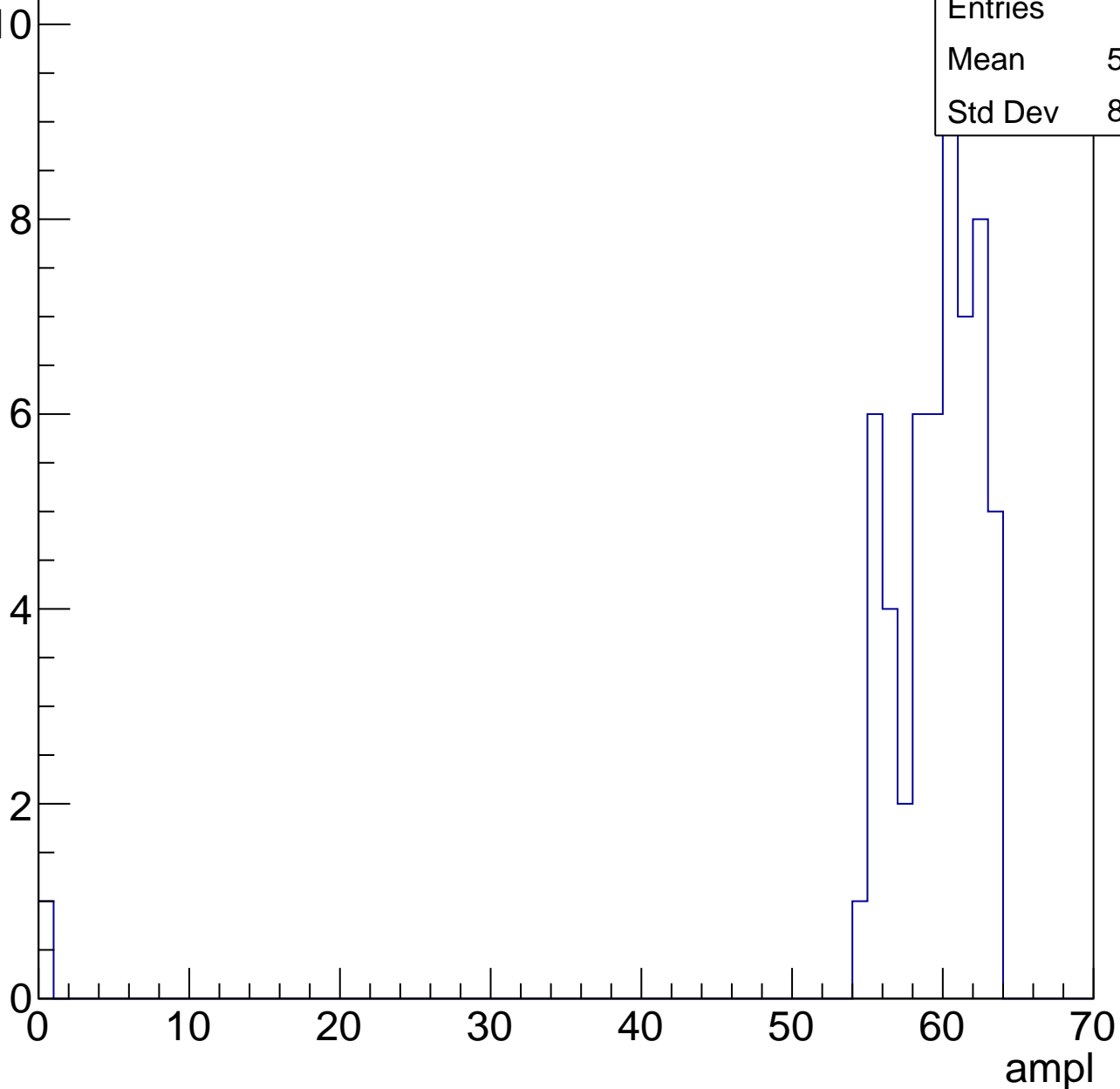


# B0L001S, U21-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

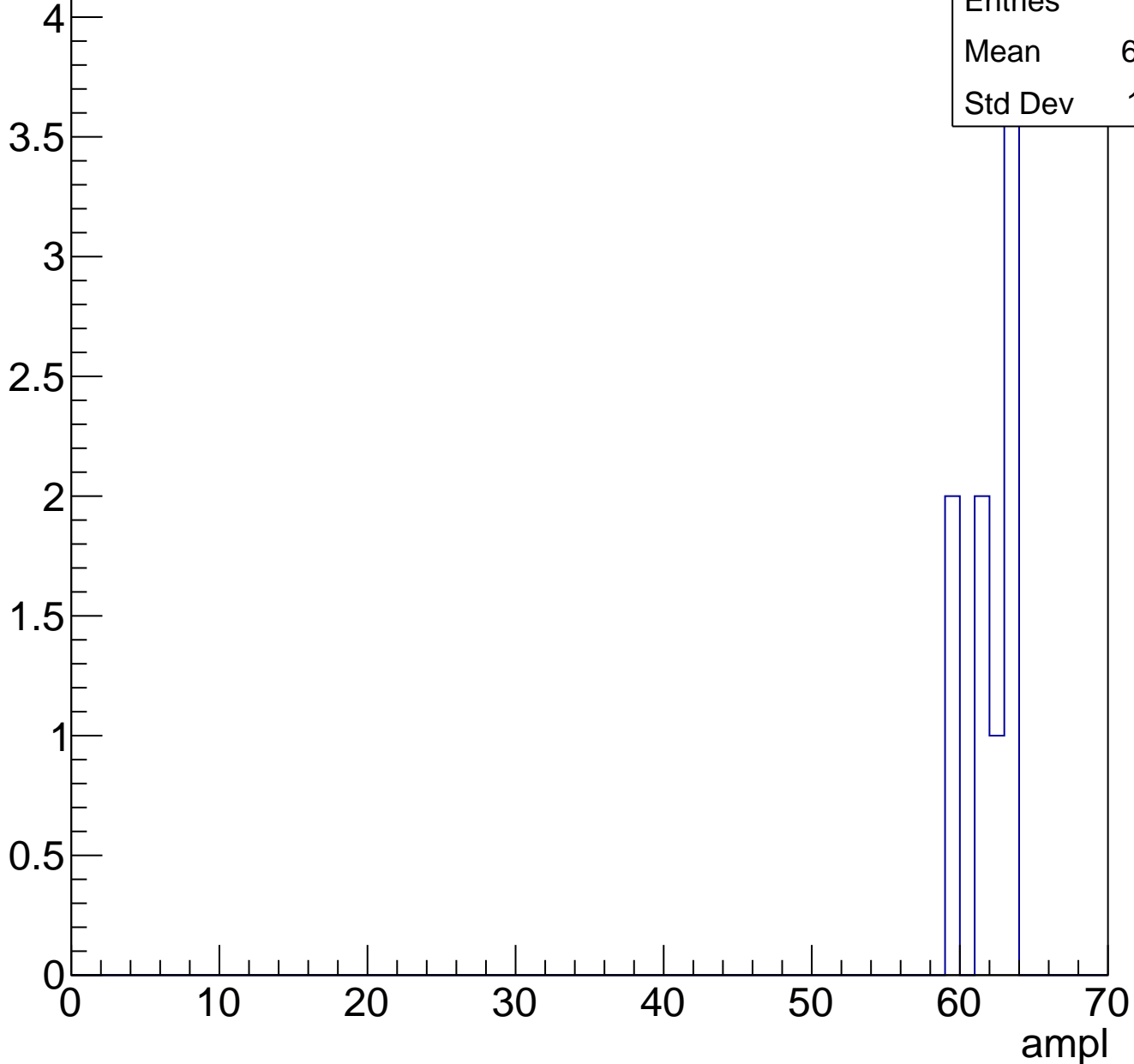
Entries	56
Mean	58.25
Std Dev	8.249



# B0L001S, U21-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	9
Mean	61.56
Std Dev	1.571



# B0L001S, U21-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U21-ch71, adc0

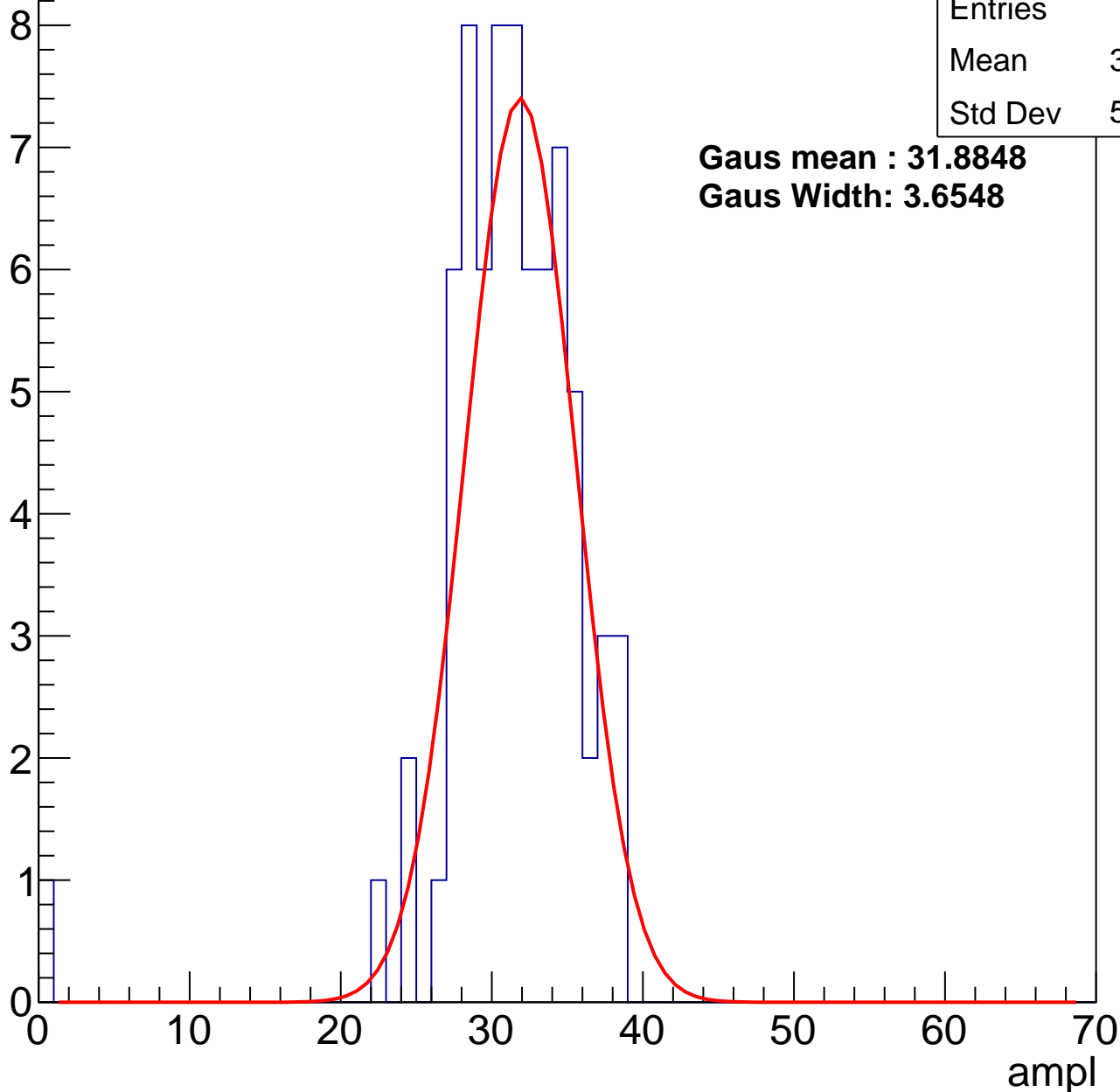
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	30.74
Std Dev	5.018

**Gaus mean : 31.8848**

**Gaus Width: 3.6548**



# B0L001S, U21-ch71, adc1

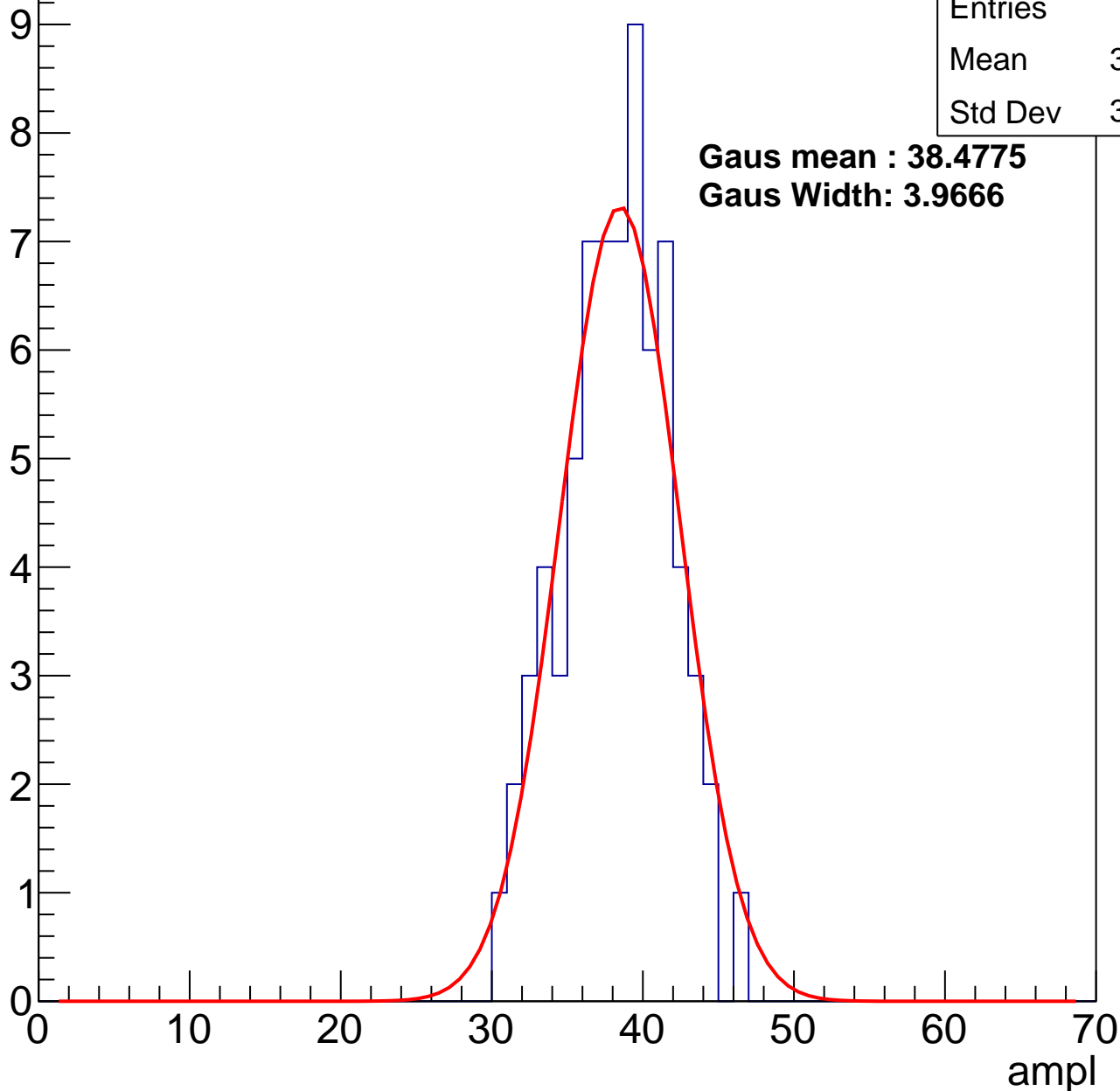
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	37.79
Std Dev	3.492

**Gaus mean : 38.4775**

**Gaus Width: 3.9666**



# B0L001S, U21-ch71, adc2

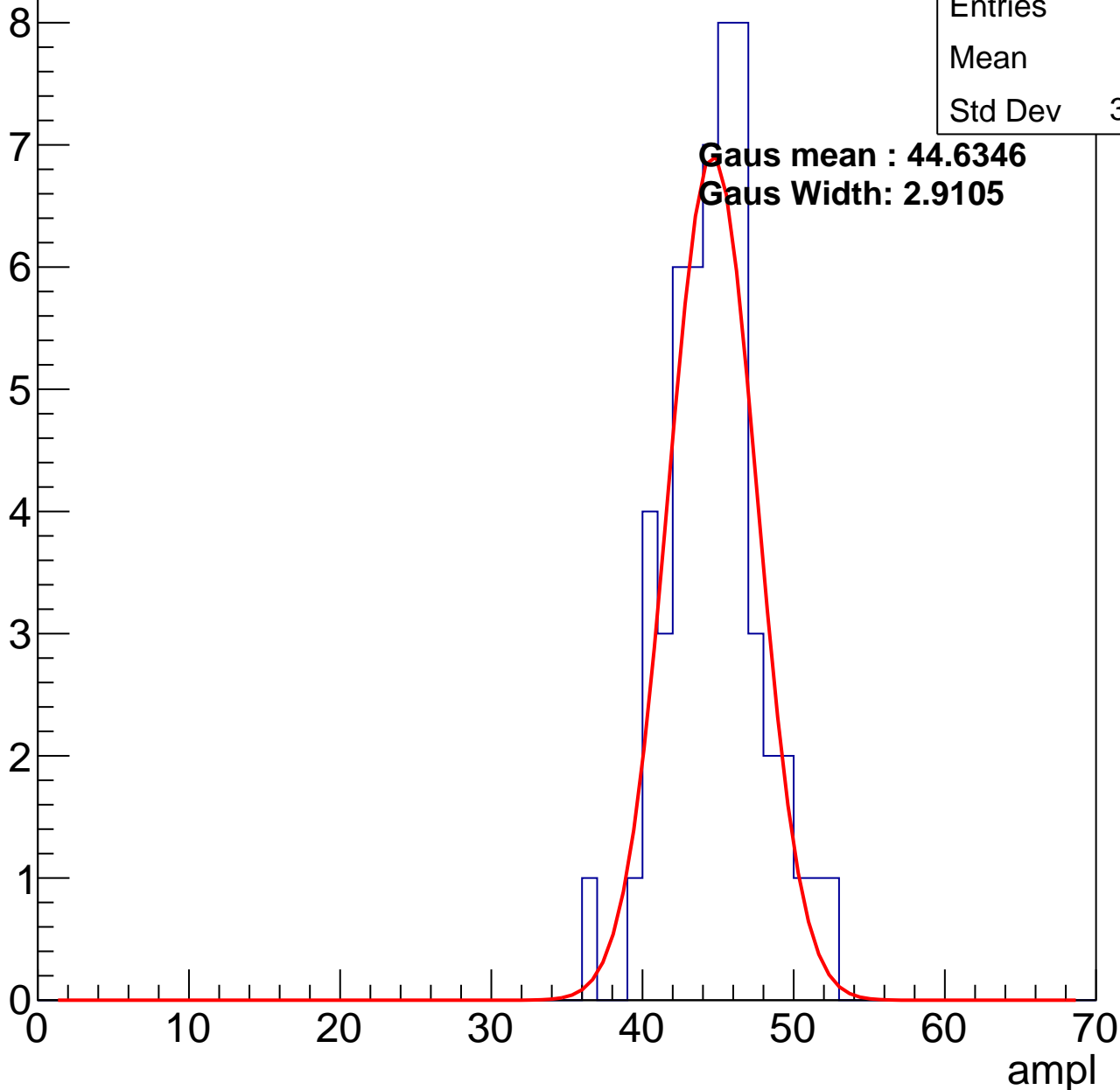
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	44.3
Std Dev	3.053

**Gaus mean : 44.6346**

**Gaus Width: 2.9105**

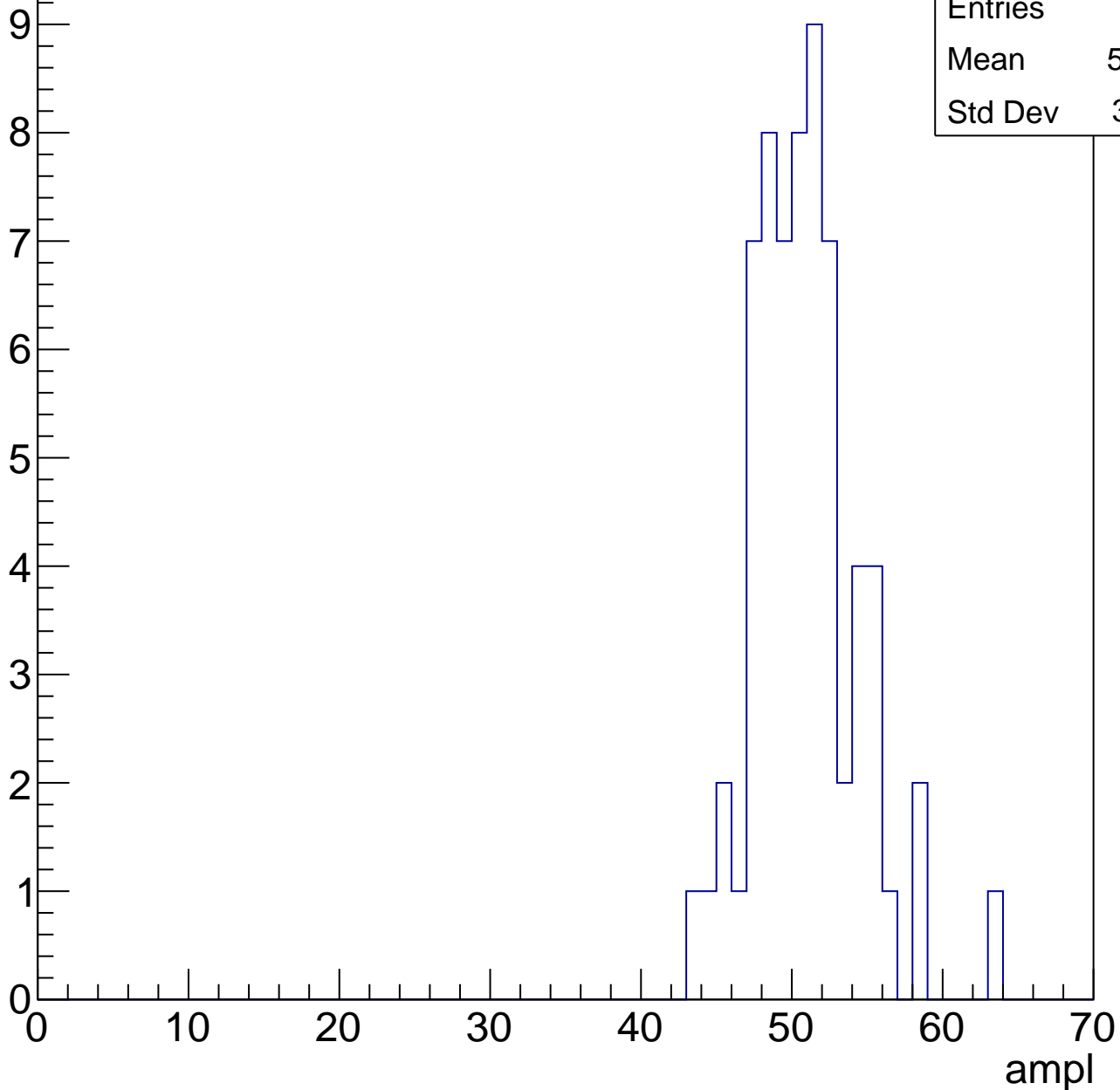


# B0L001S, U21-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	50.45
Std Dev	3.491

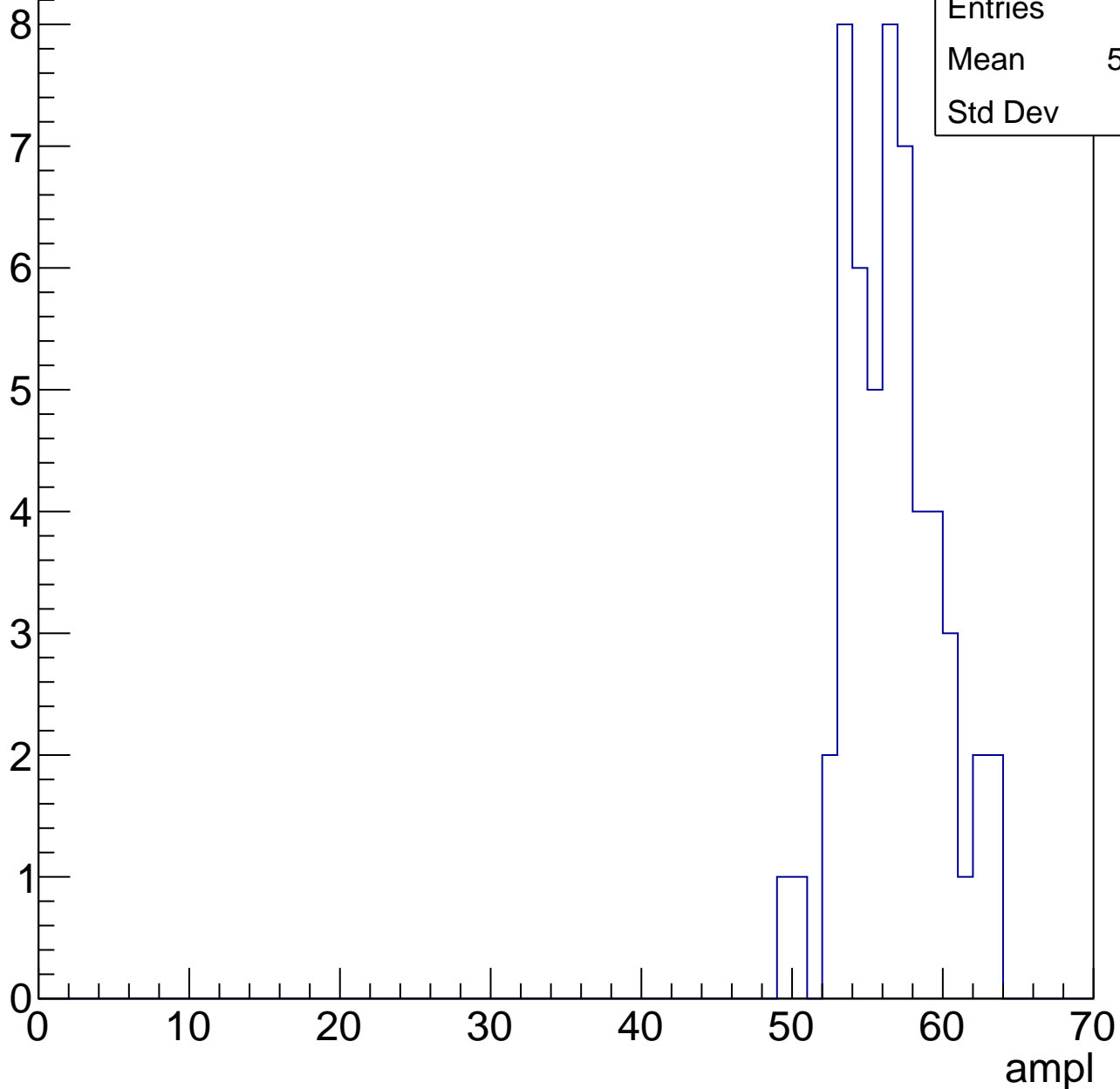


# B0L001S, U21-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	56.15
Std Dev	3.1

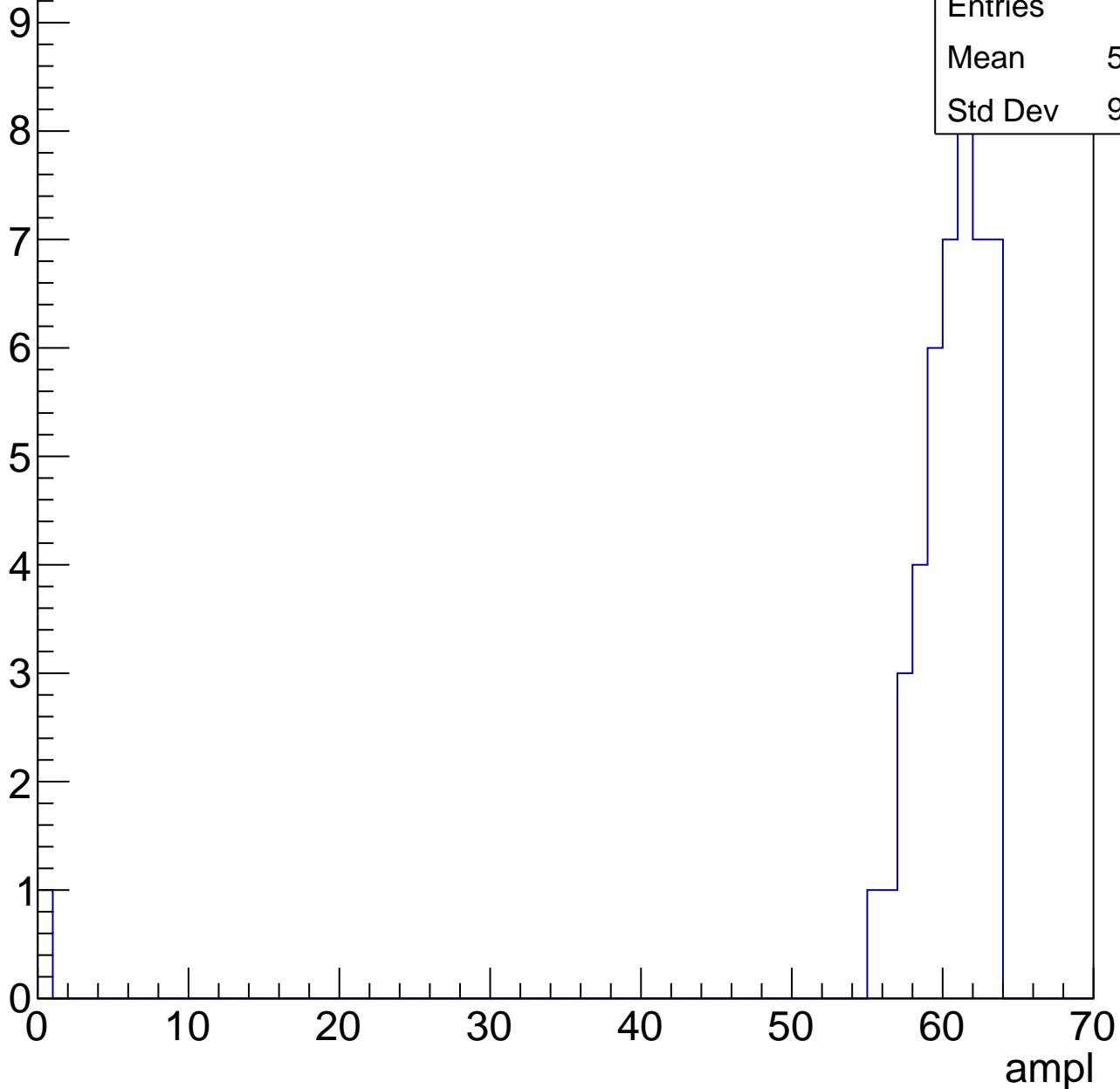


# B0L001S, U21-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	58.96
Std Dev	9.017



# B0L001S, U21-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U21-ch72, adc0

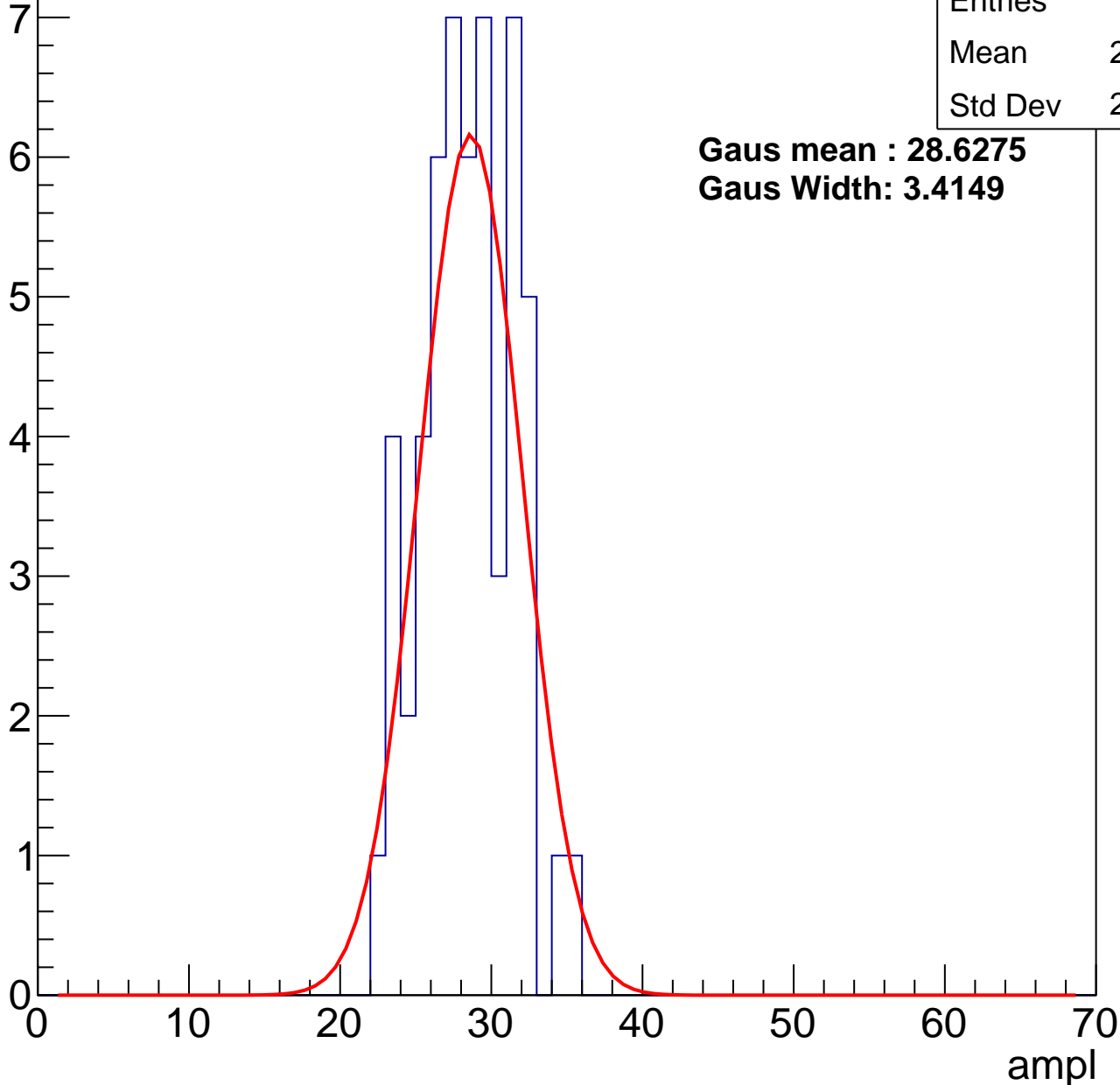
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	28.04
Std Dev	2.987

**Gaus mean : 28.6275**

**Gaus Width: 3.4149**



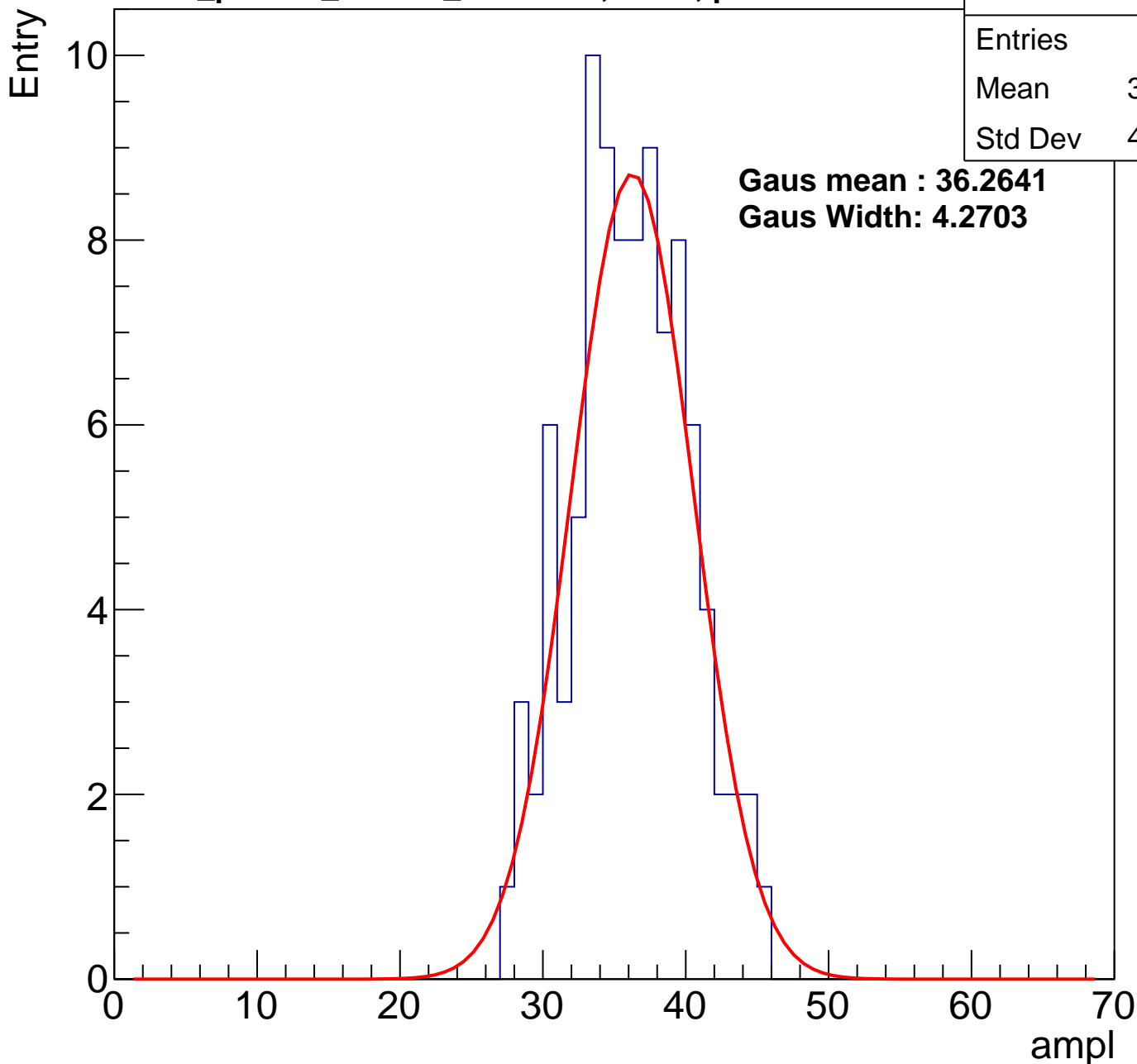
# B0L001S, U21-ch72, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	96
Mean	35.67
Std Dev	4.017

**Gaus mean : 36.2641**

**Gaus Width: 4.2703**

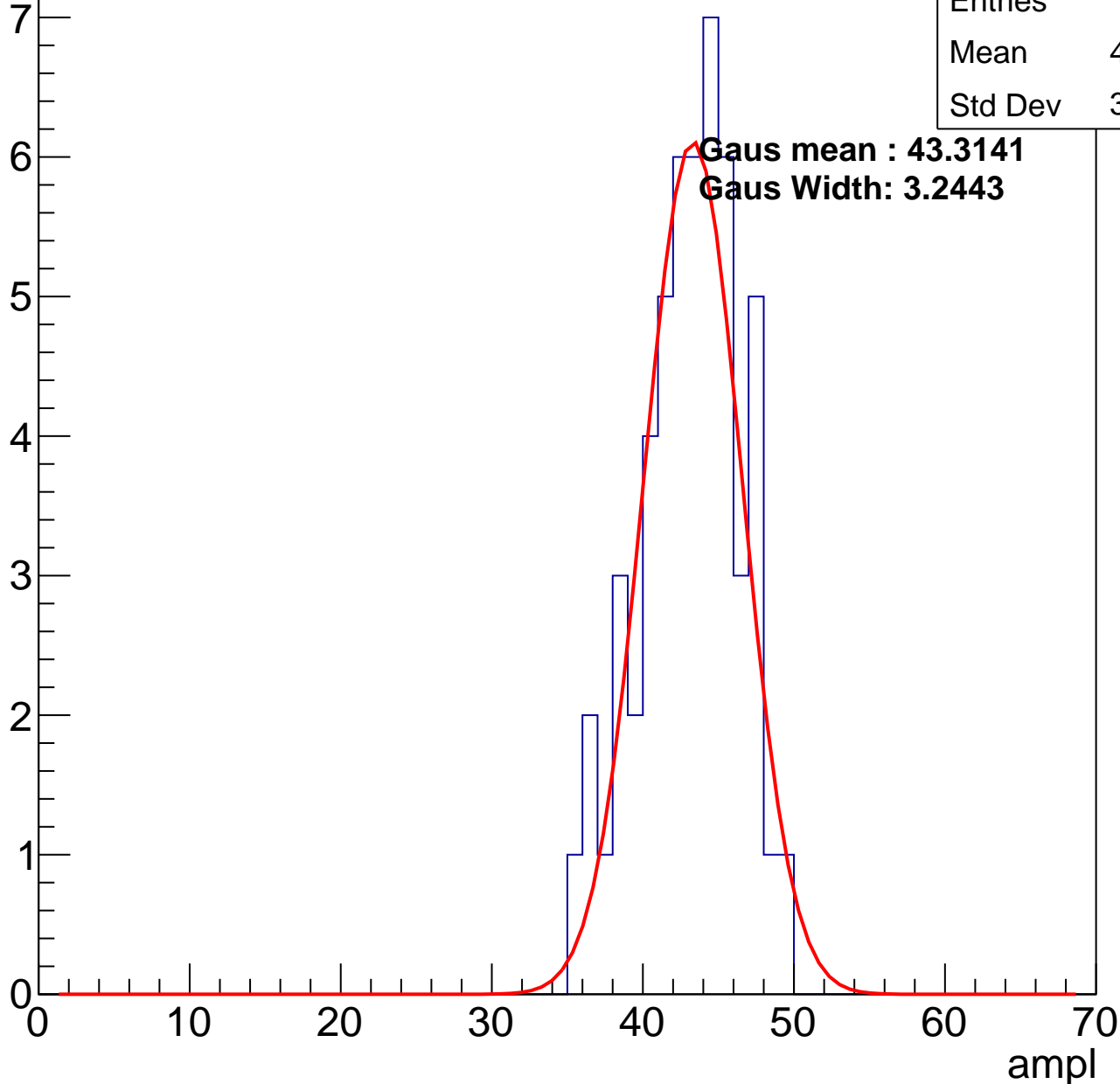


# B0L001S, U21-ch72, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	42.62
Std Dev	3.246

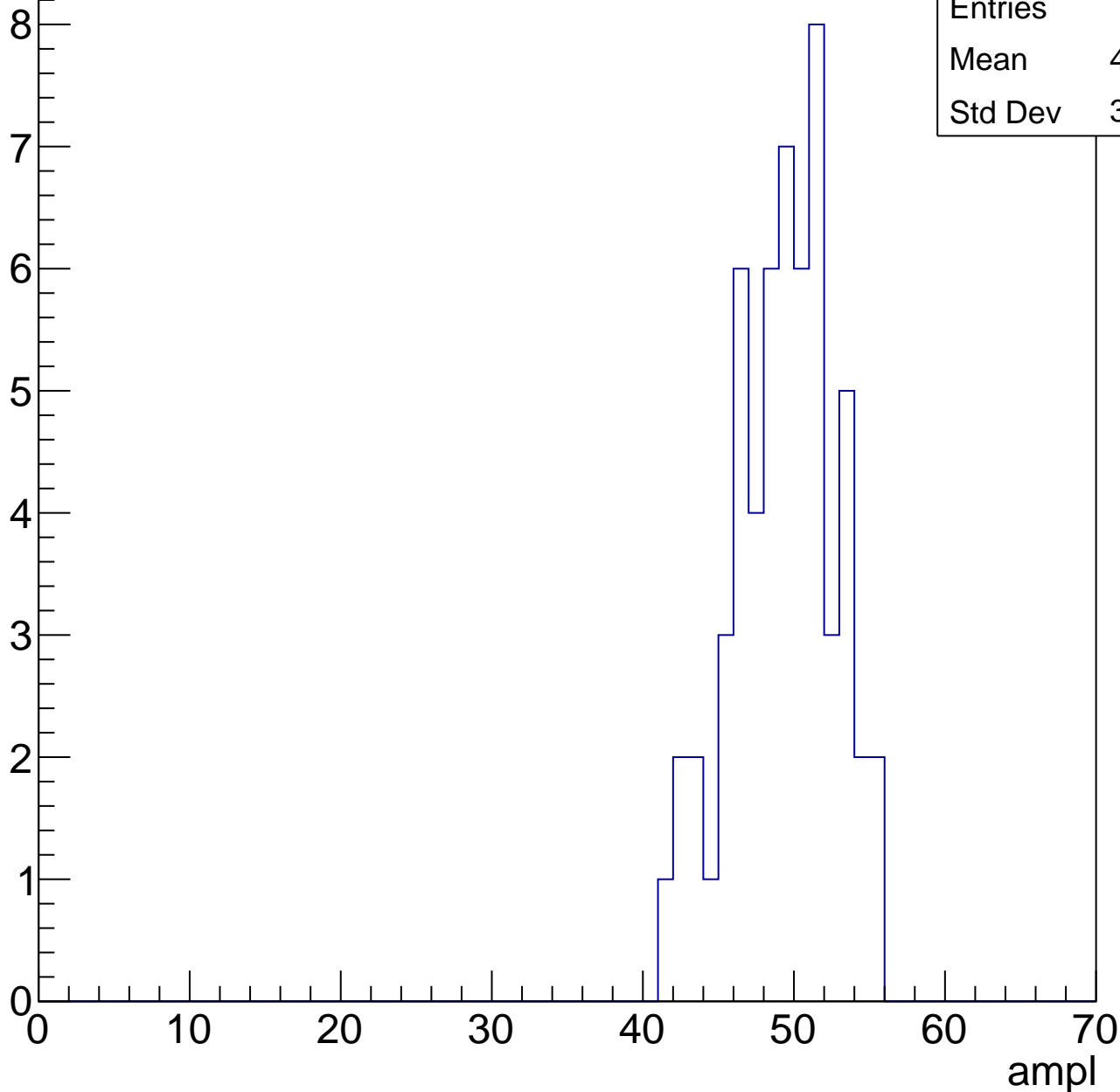


# B0L001S, U21-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	48.83
Std Dev	3.343

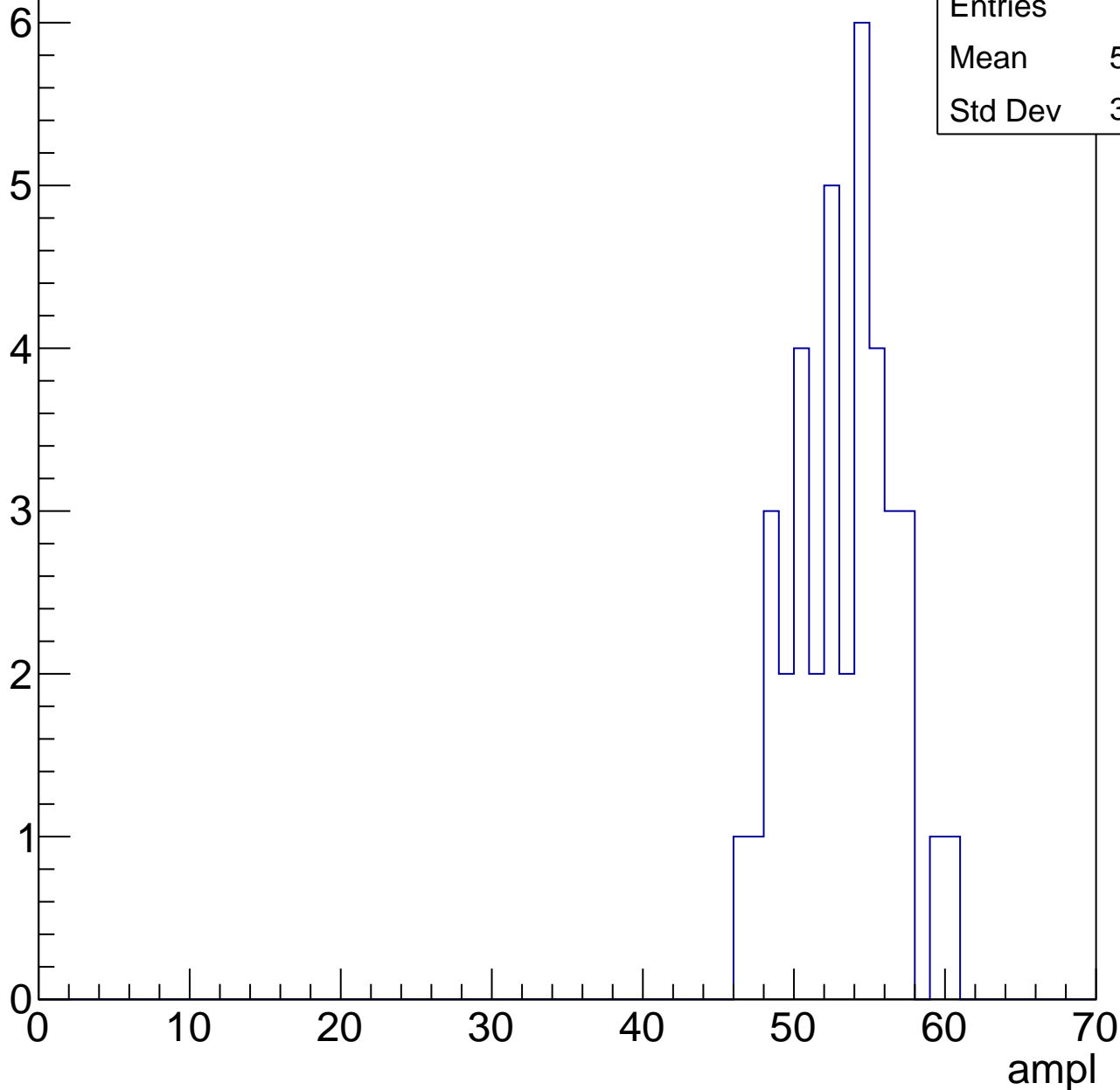


# B0L001S, U21-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	38
Mean	52.76
Std Dev	3.328



# B0L001S, U21-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

10

Entries 69

Mean 58.26

Std Dev 2.733

8

6

4

2

0

0

10

20

30

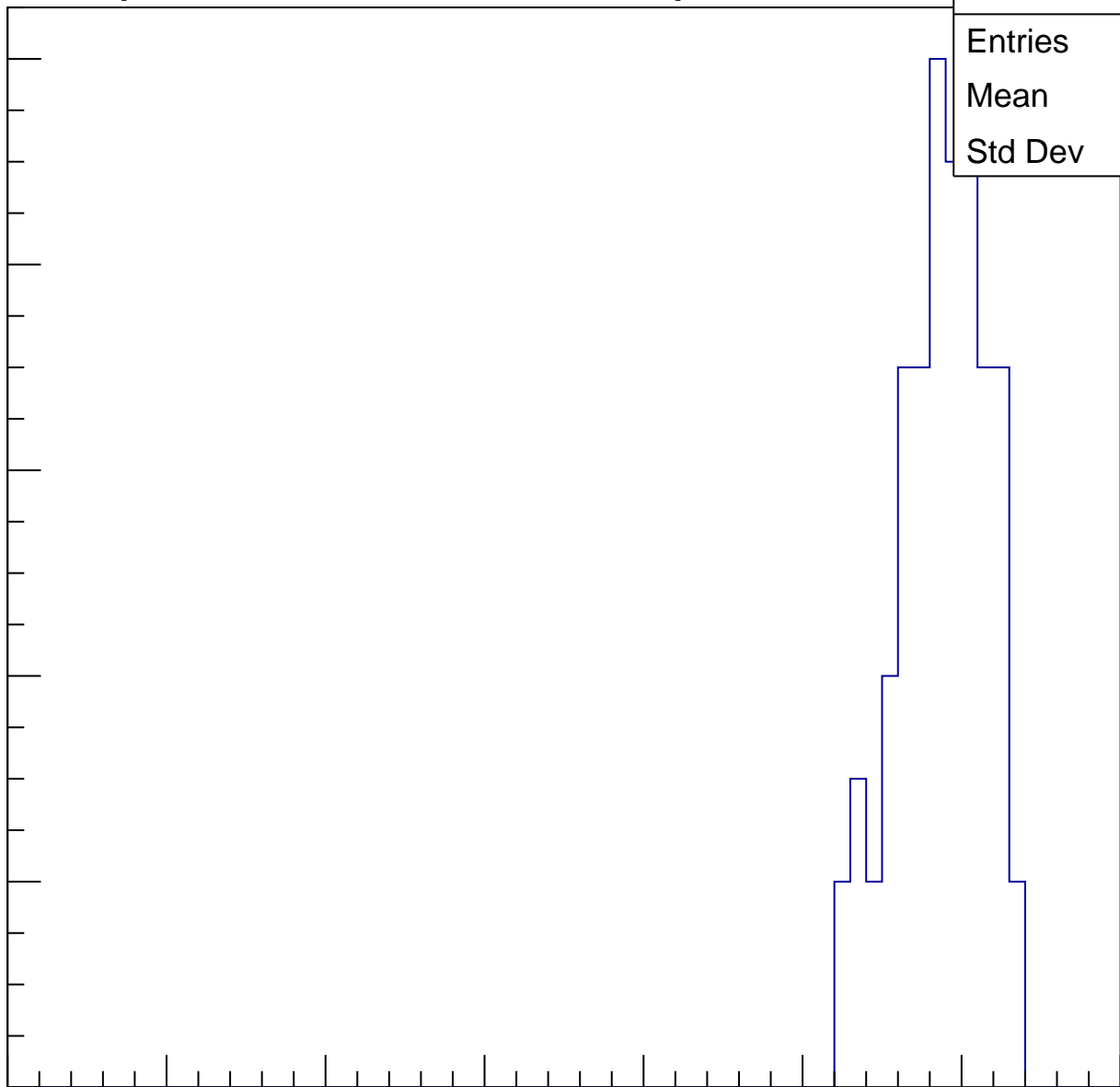
40

50

60

70

ampl

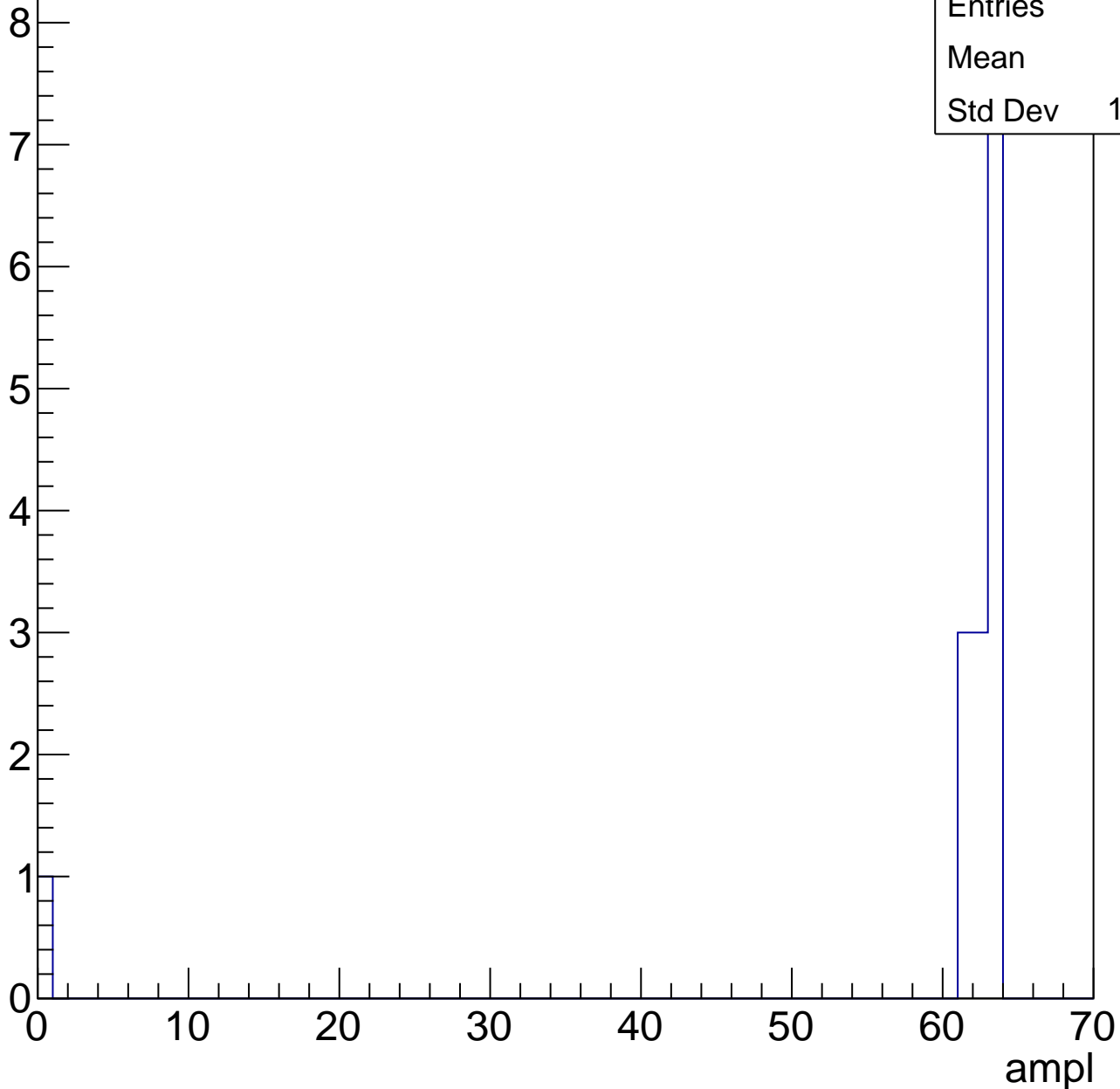


# B0L001S, U21-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	15
Mean	58.2
Std Dev	15.57





# B0L001S, U21-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U21-ch73, adc0

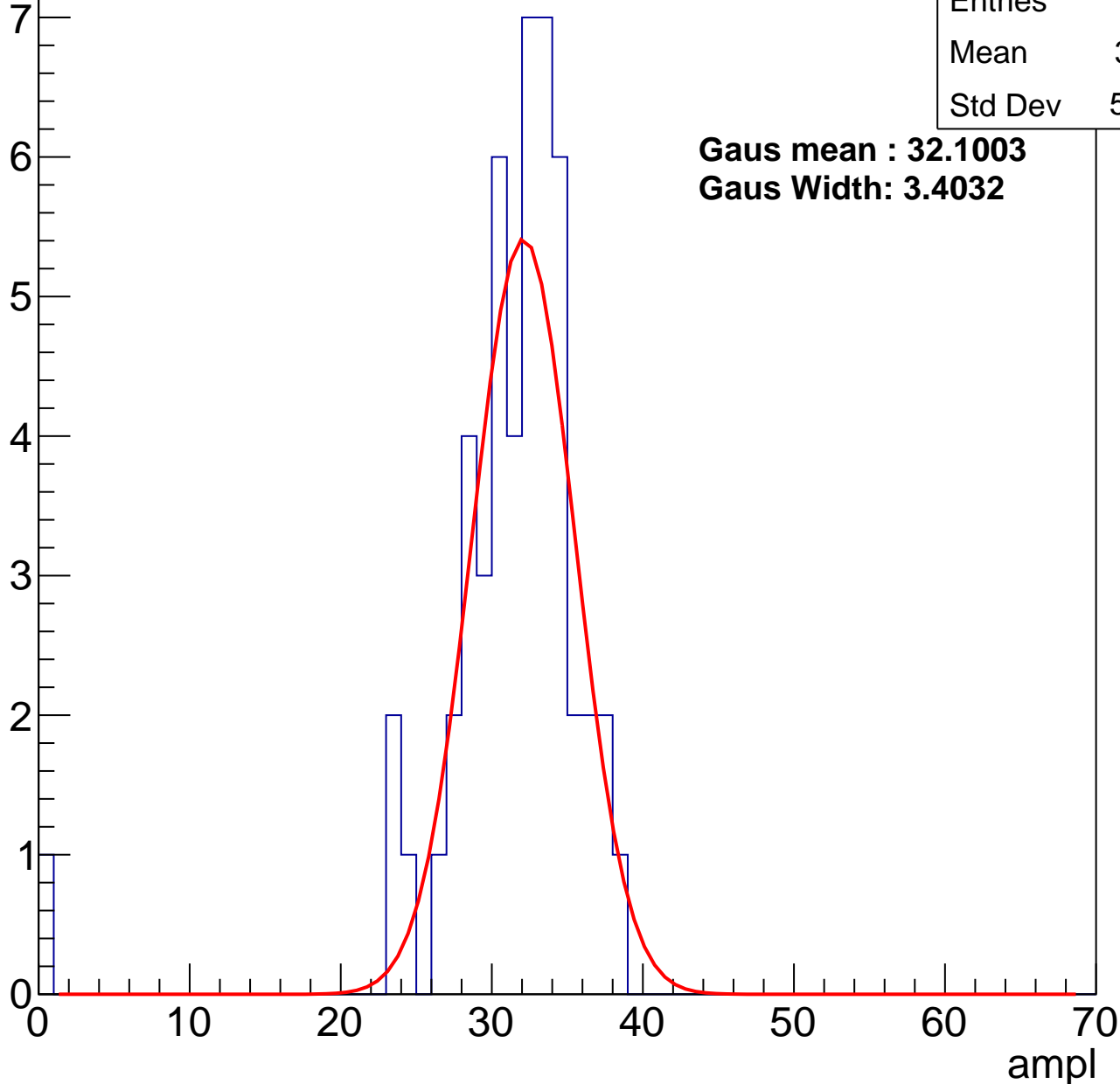
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	30.71
Std Dev	5.489

**Gaus mean : 32.1003**

**Gaus Width: 3.4032**



# B0L001S, U21-ch73, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	79
Mean	37.95
Std Dev	3.624

**Gaus mean : 38.6190**

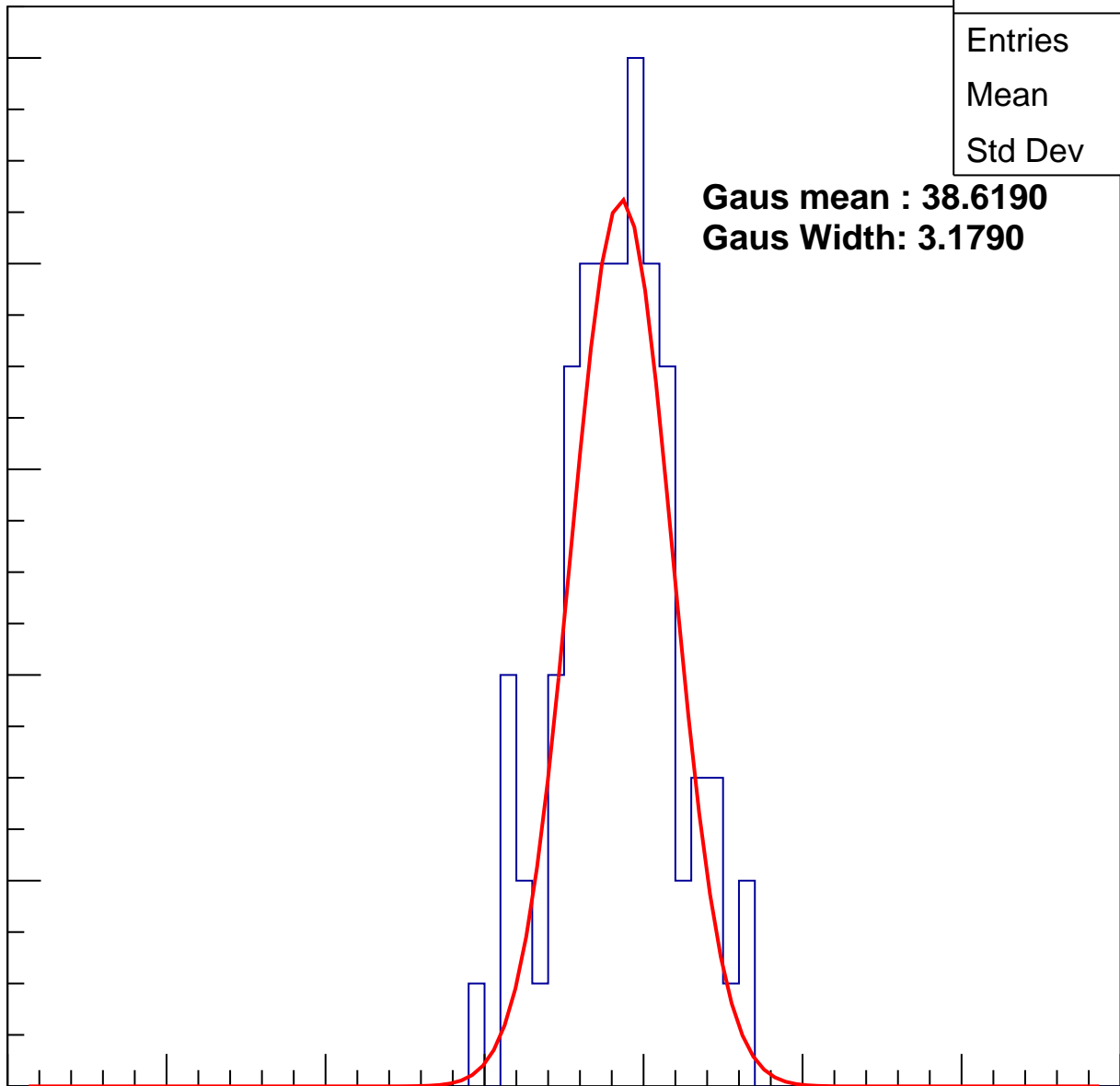
**Gaus Width: 3.1790**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U21-ch73, adc2

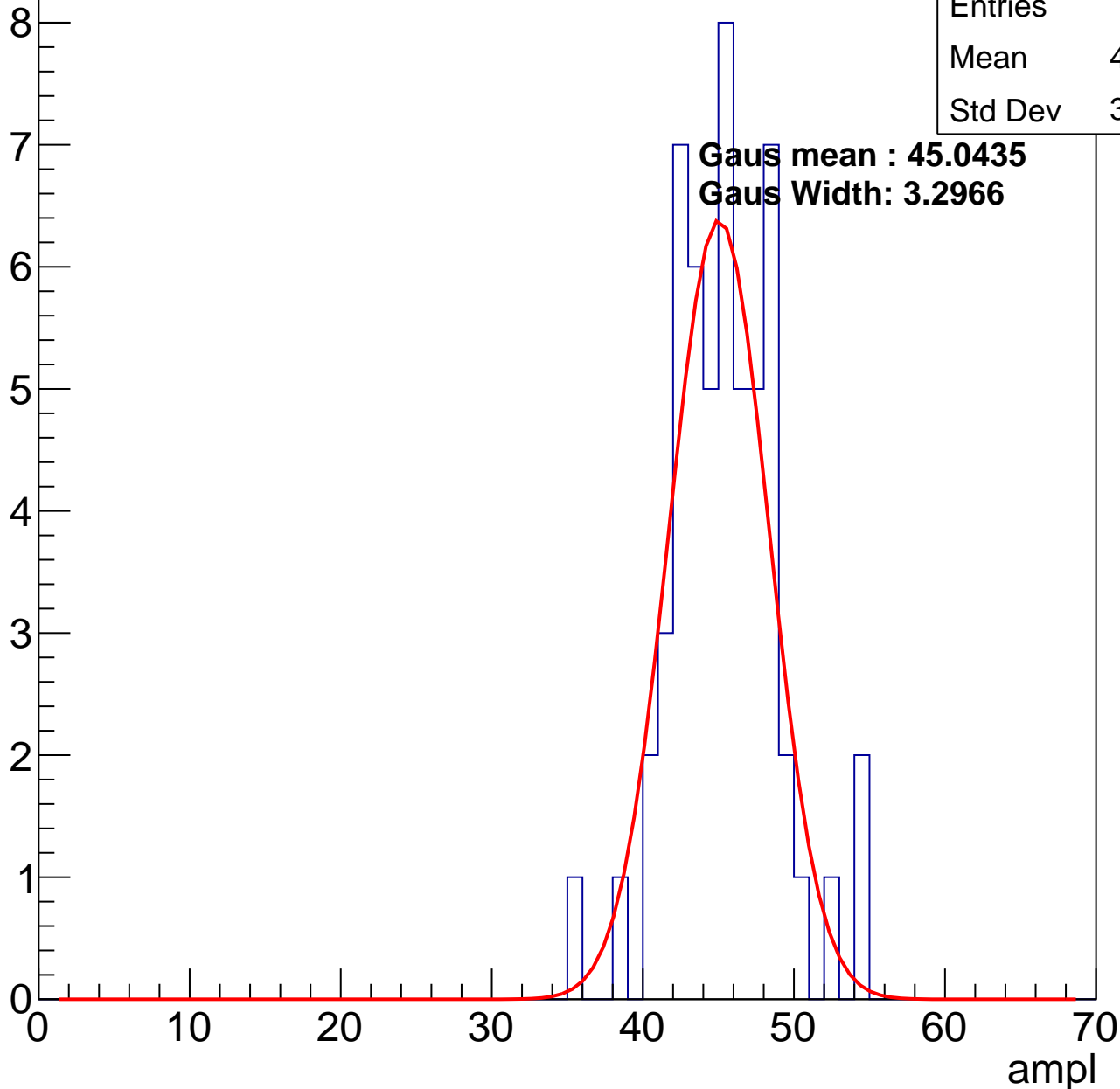
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	44.95
Std Dev	3.522

**Gaus mean : 45.0435**

**Gaus Width: 3.2966**



# B0L001S, U21-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

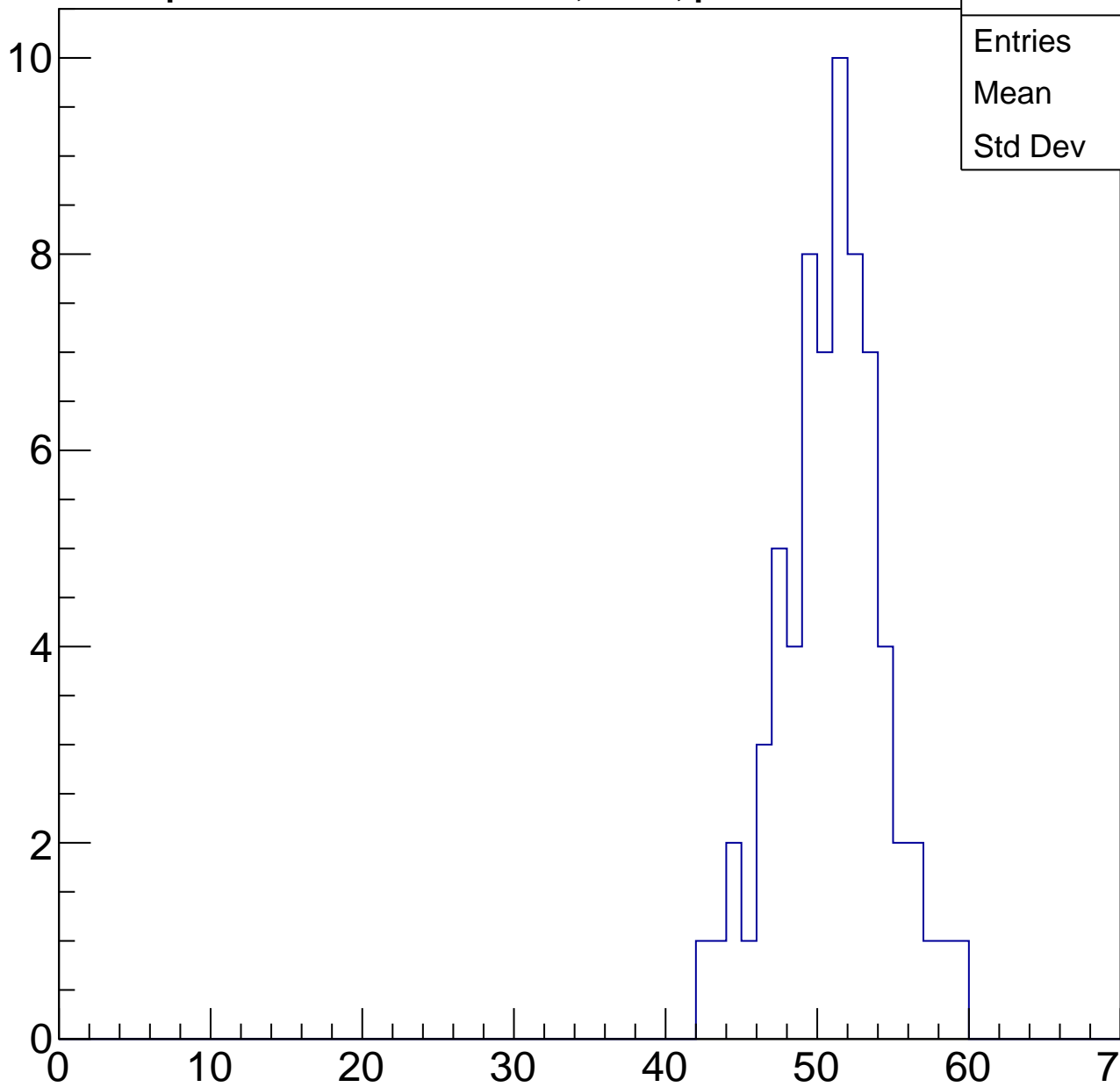
Entries	68
Mean	50.5
Std Dev	3.419

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

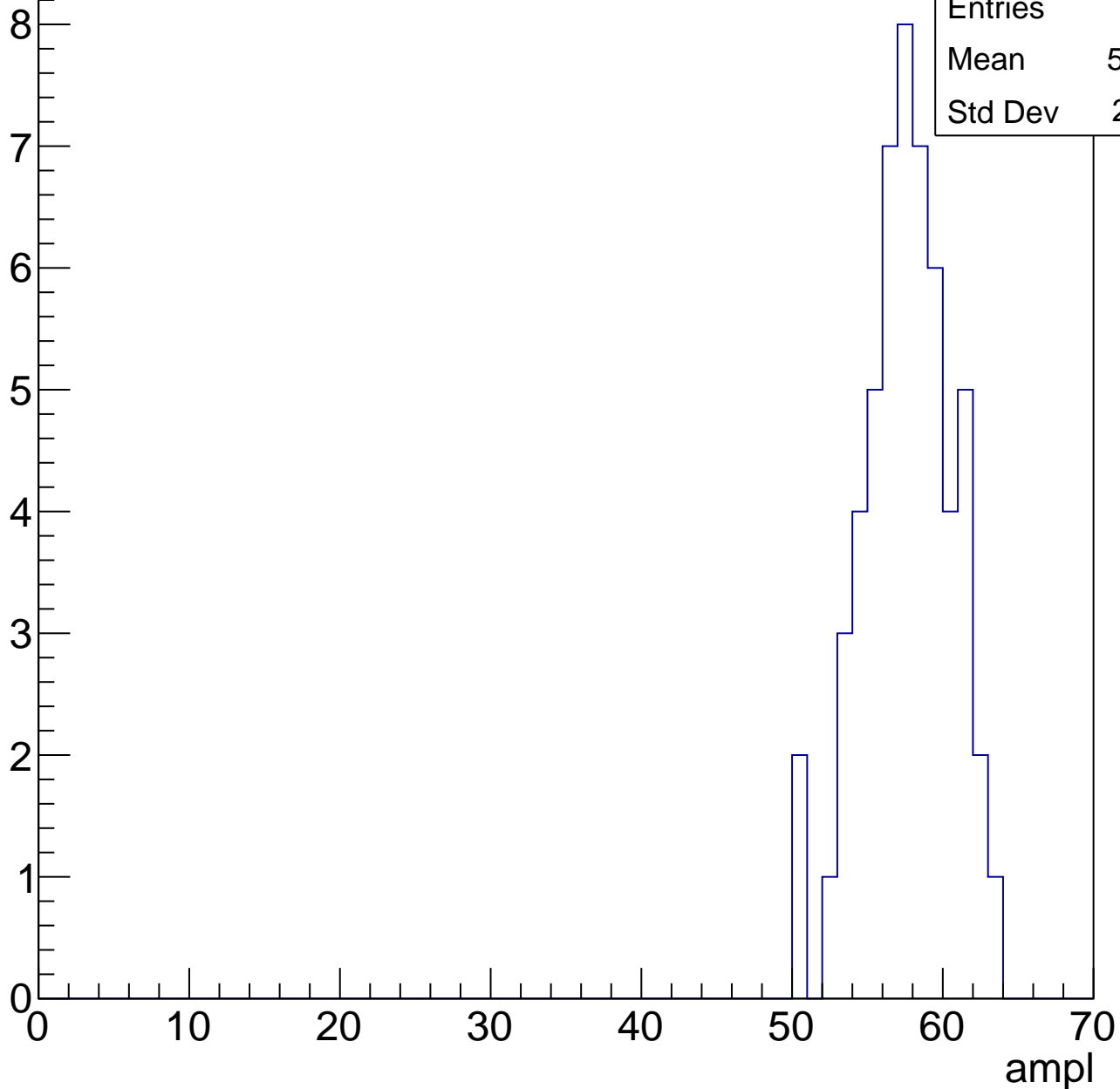


# B0L001S, U21-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	57.13
Std Dev	2.911

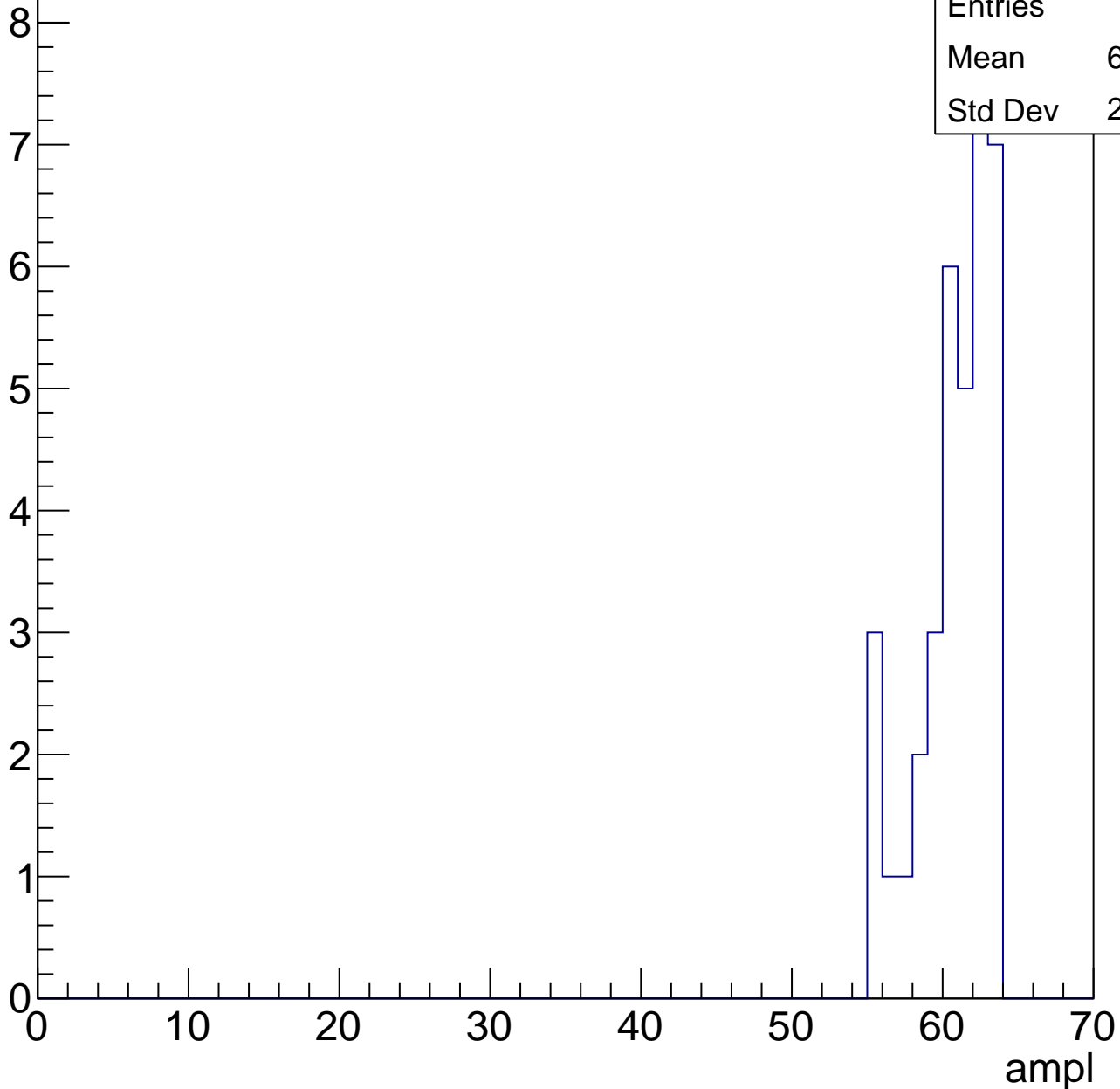


# B0L001S, U21-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	36
Mean	60.36
Std Dev	2.394



# B0L001S, U21-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	11.5
Std Dev	11.5

# B0L001S, U21-ch74, adc0

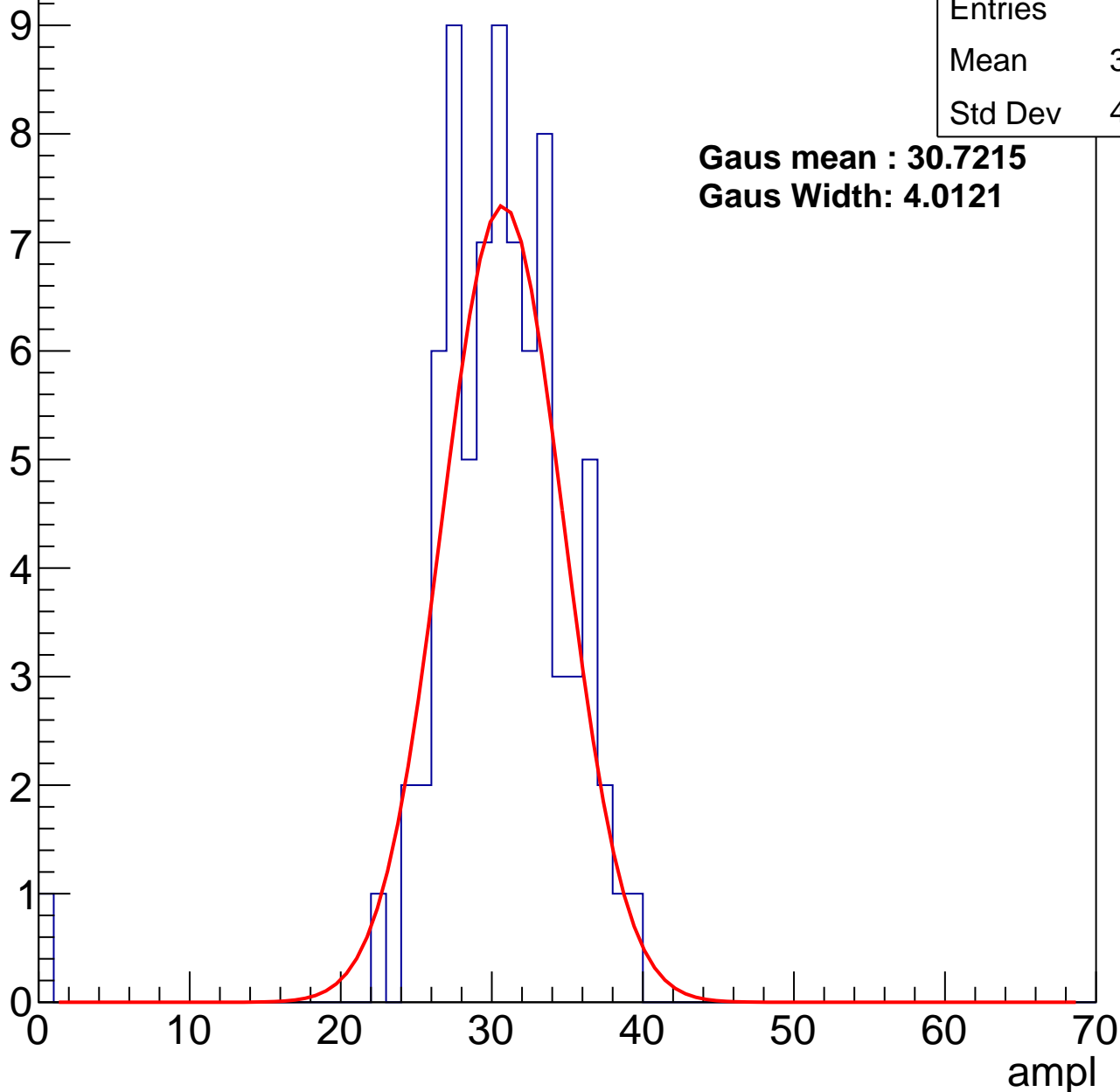
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	30.04
Std Dev	4.986

**Gaus mean : 30.7215**

**Gaus Width: 4.0121**



# B0L001S, U21-ch74, adc1

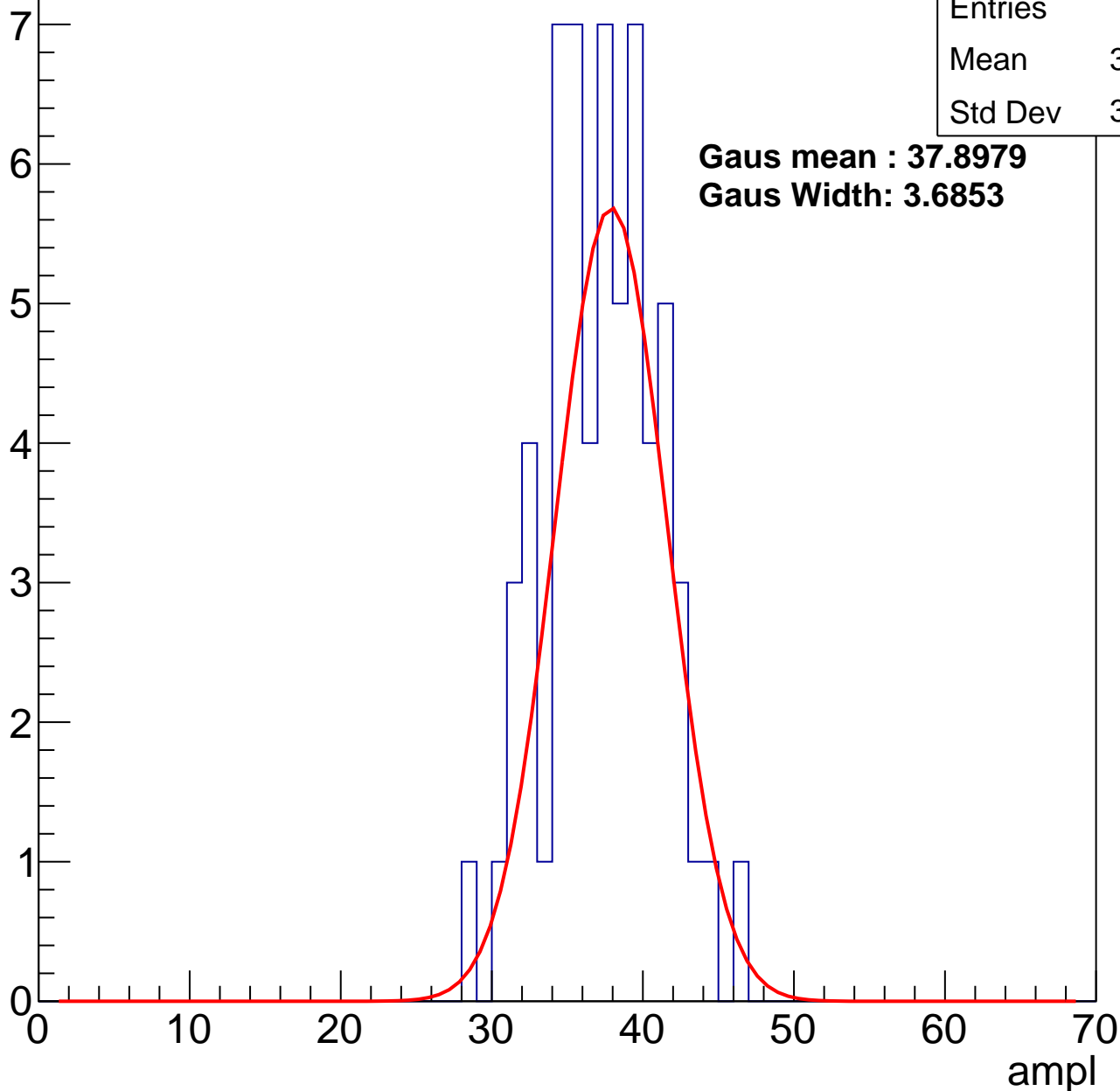
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	36.85
Std Dev	3.676

**Gaus mean : 37.8979**

**Gaus Width: 3.6853**



# B0L001S, U21-ch74, adc2

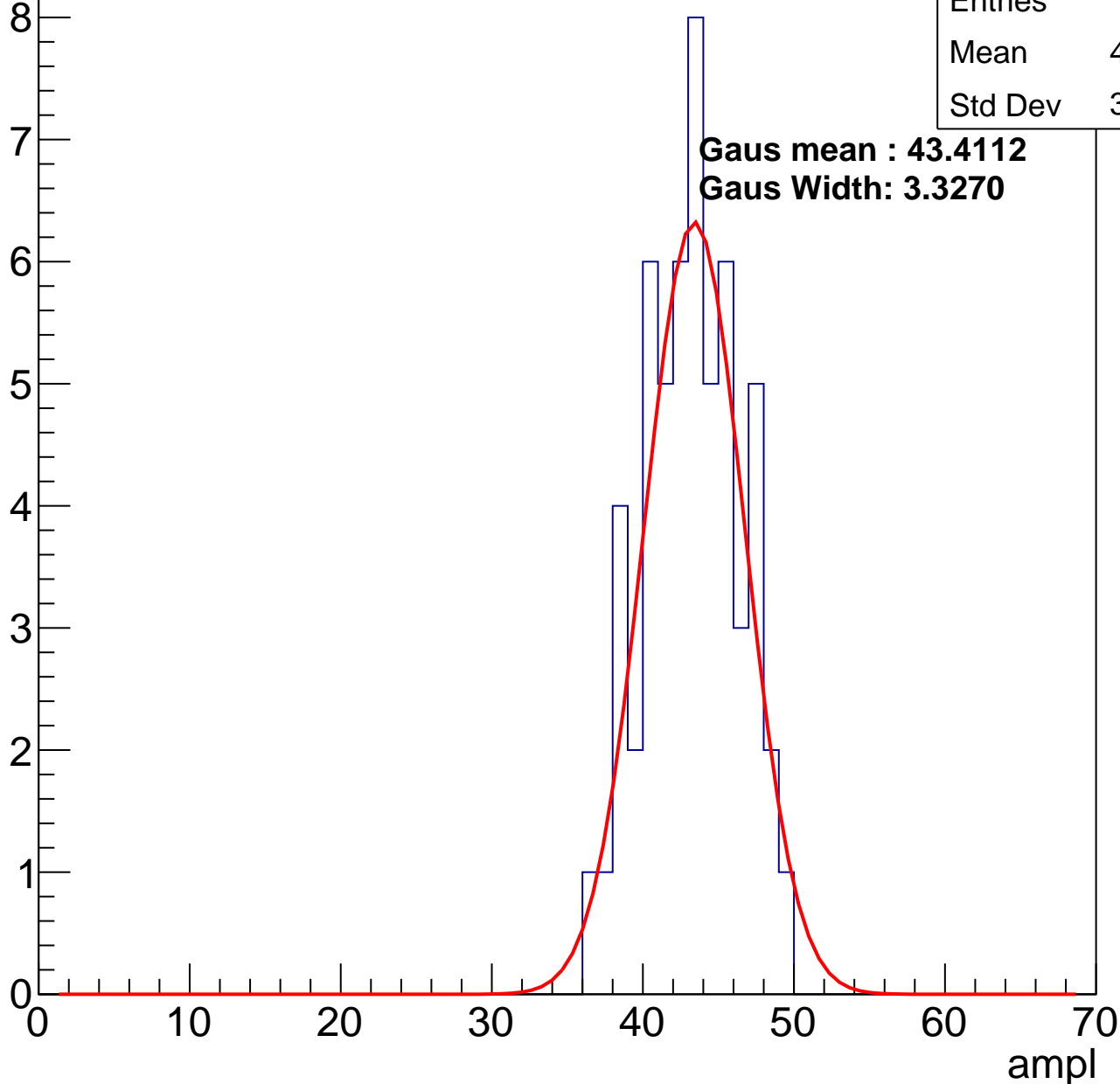
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	42.76
Std Dev	3.063

**Gaus mean : 43.4112**

**Gaus Width: 3.3270**

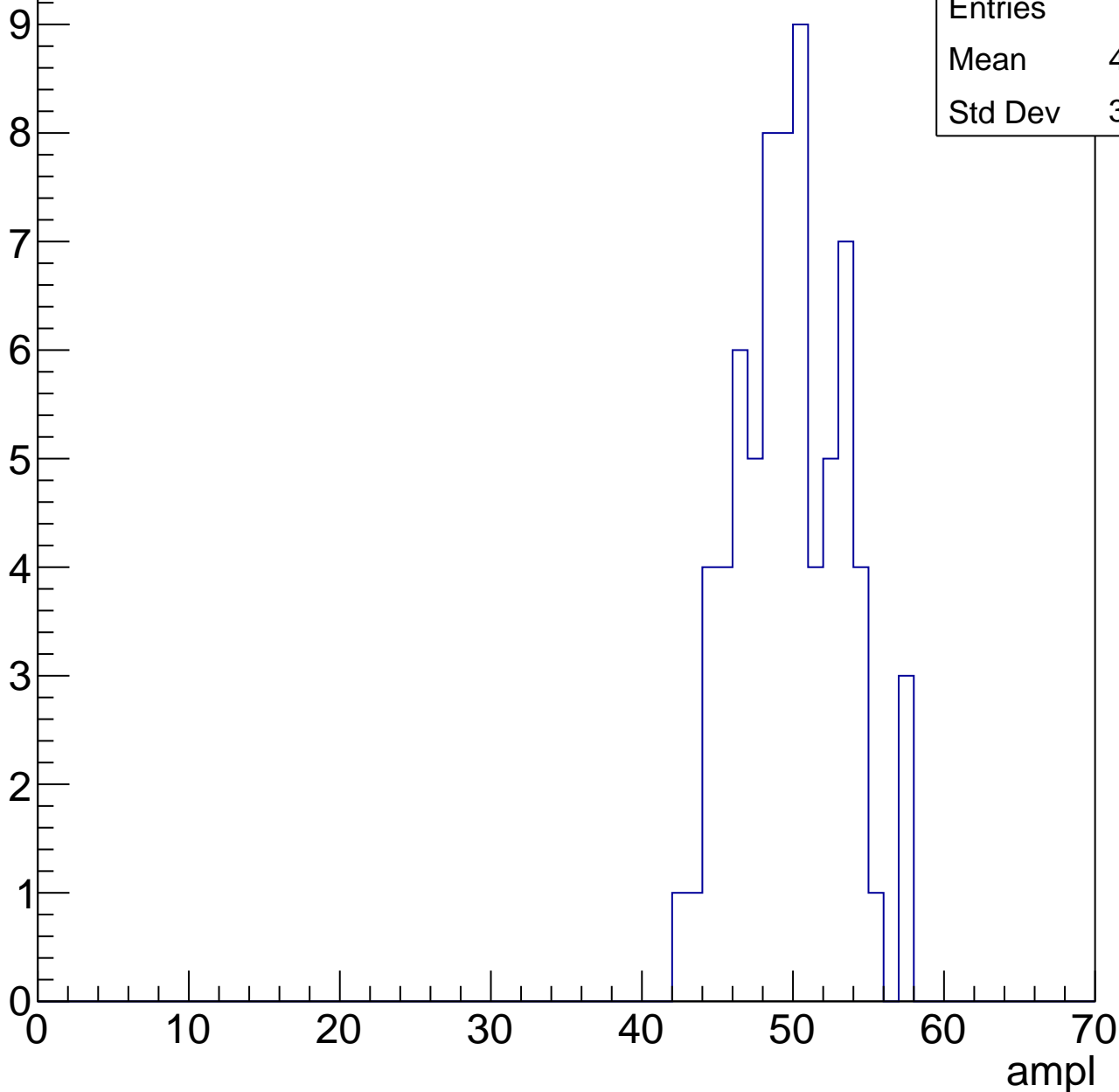


# B0L001S, U21-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	49.36
Std Dev	3.448

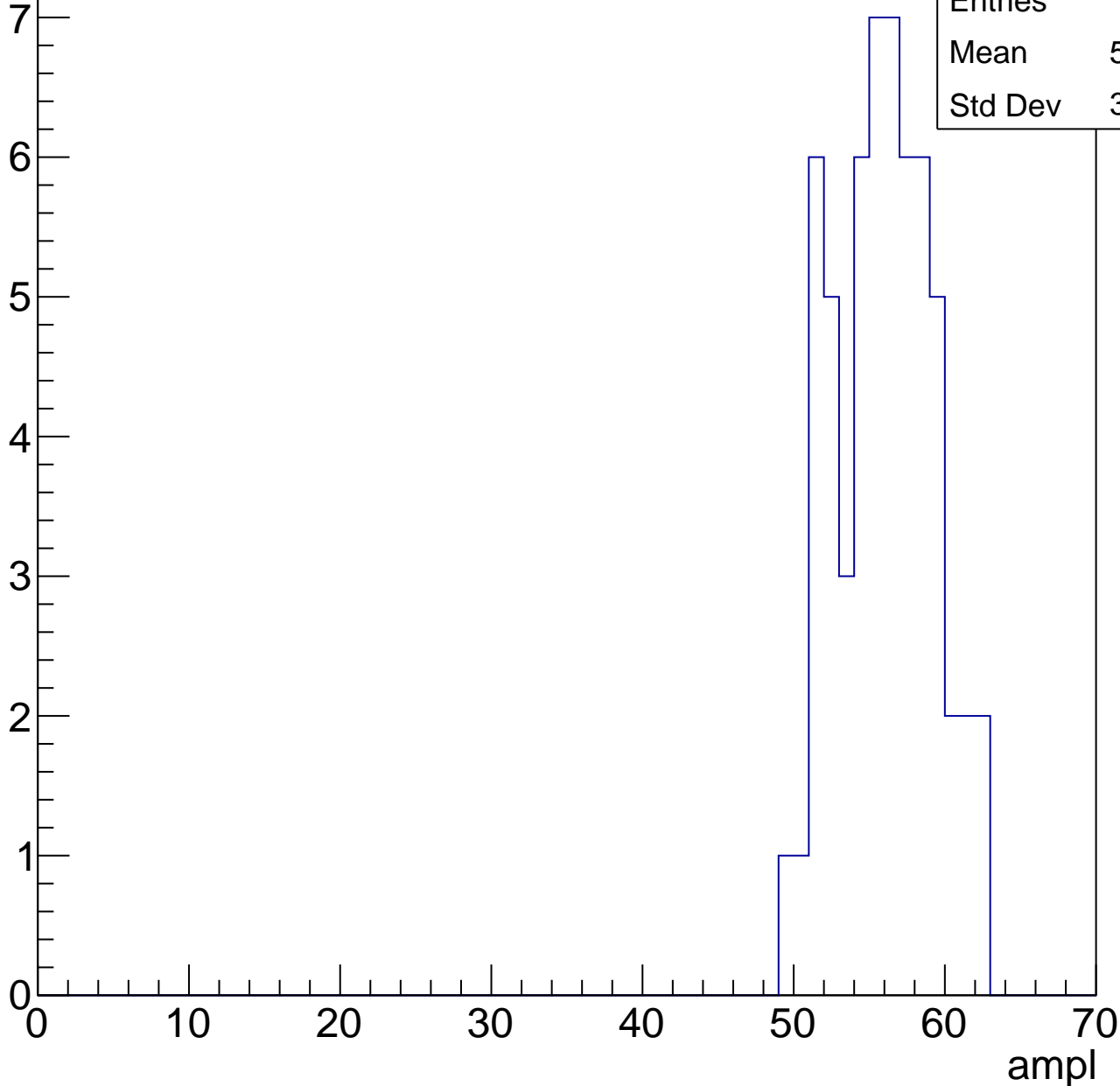


# B0L001S, U21-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	55.53
Std Dev	3.159

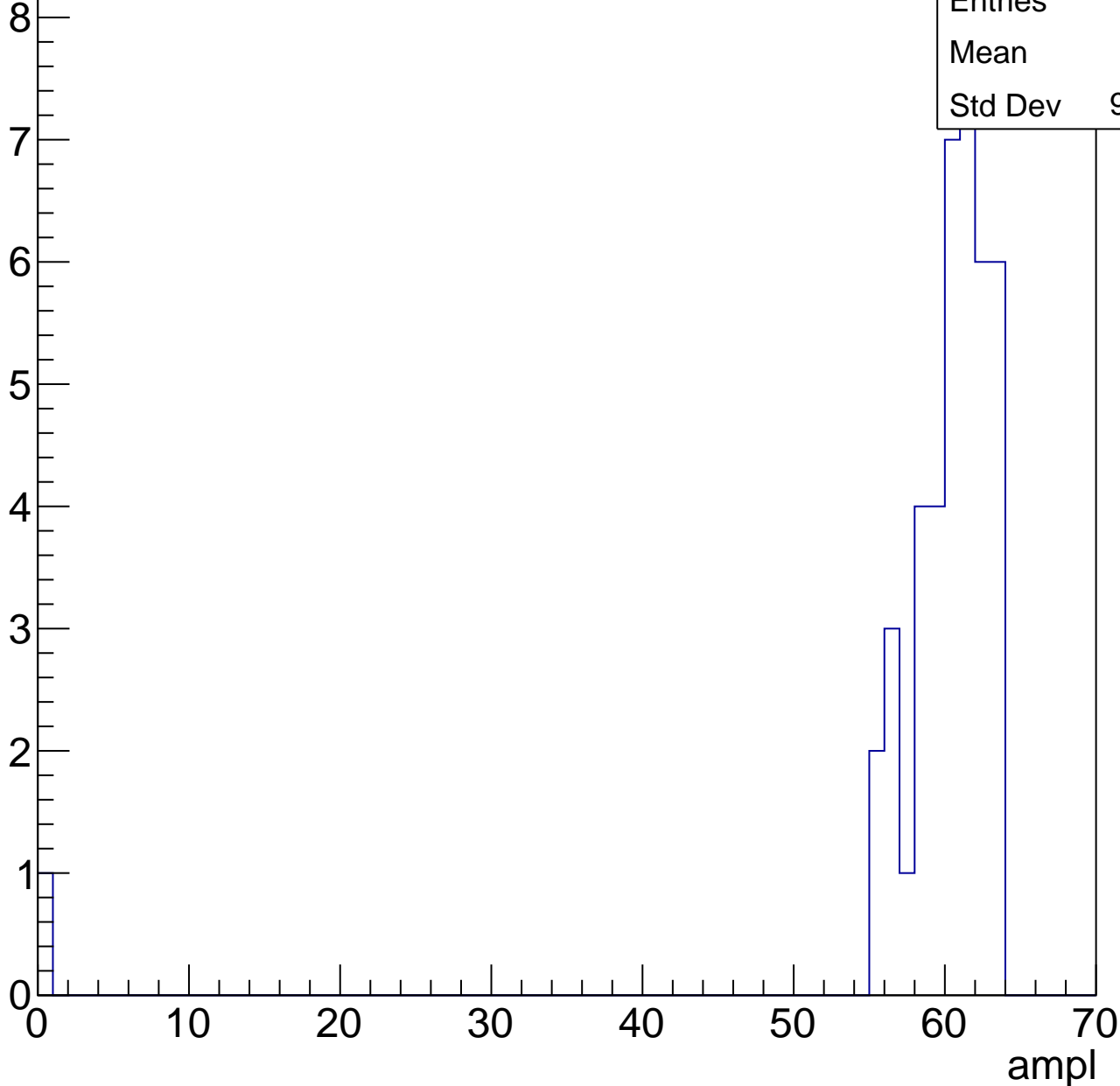


# B0L001S, U21-ch74, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

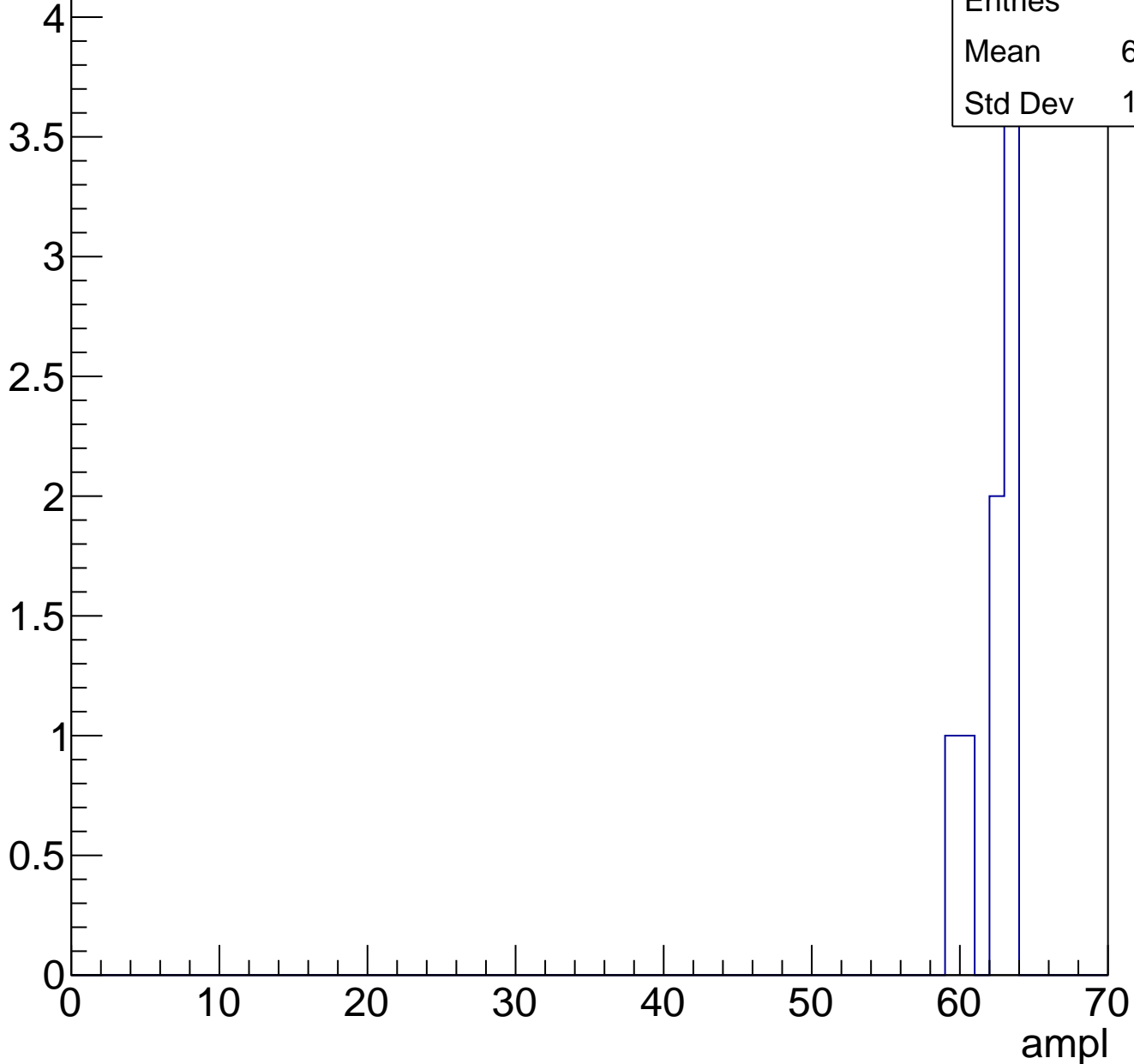
Entries	42
Mean	58.6
Std Dev	9.424



# B0L001S, U21-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch75, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	70
Mean	31.76
Std Dev	4.932

**Gaus mean : 32.2480**

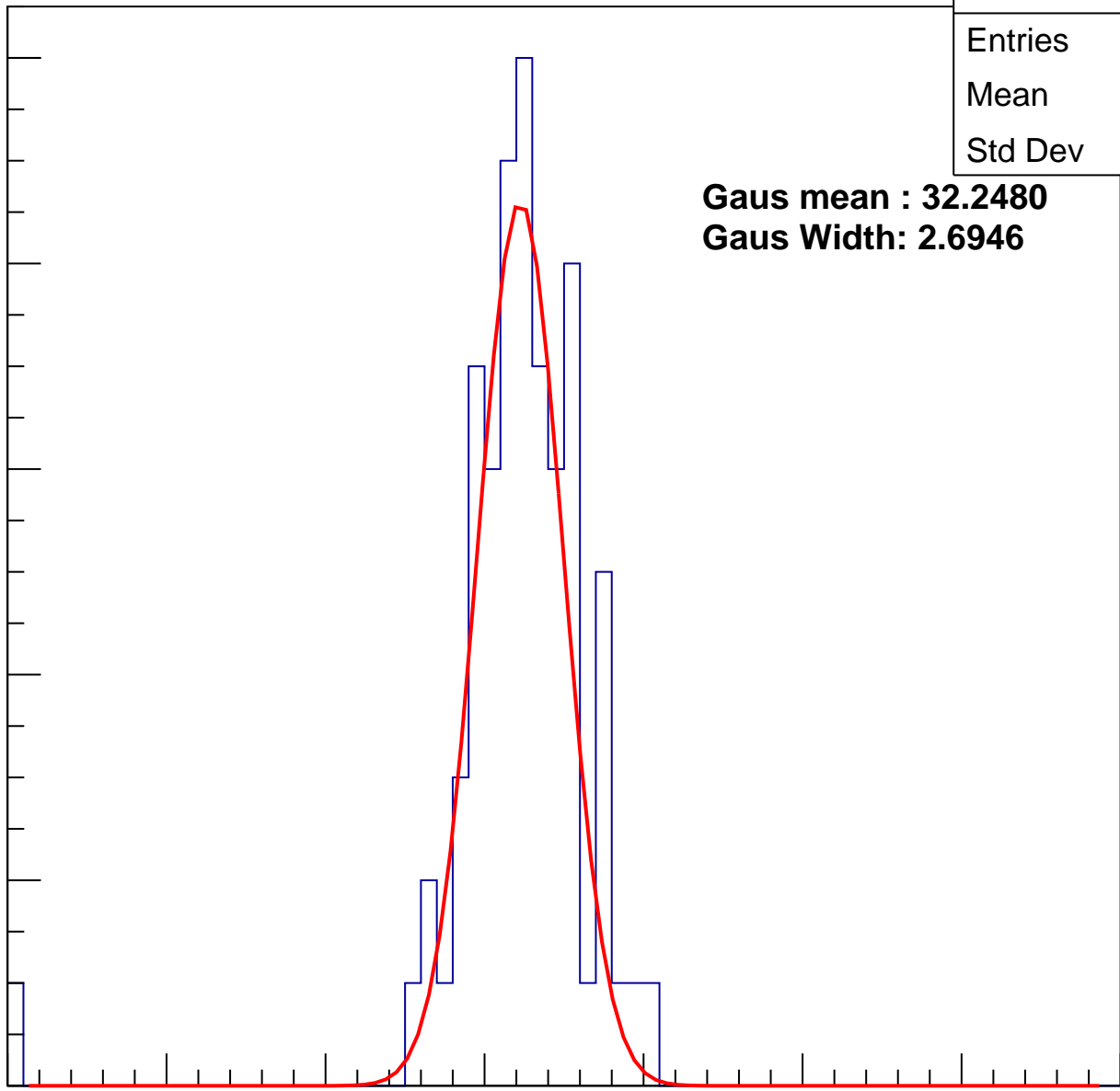
**Gaus Width: 2.6946**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U21-ch75, adc1

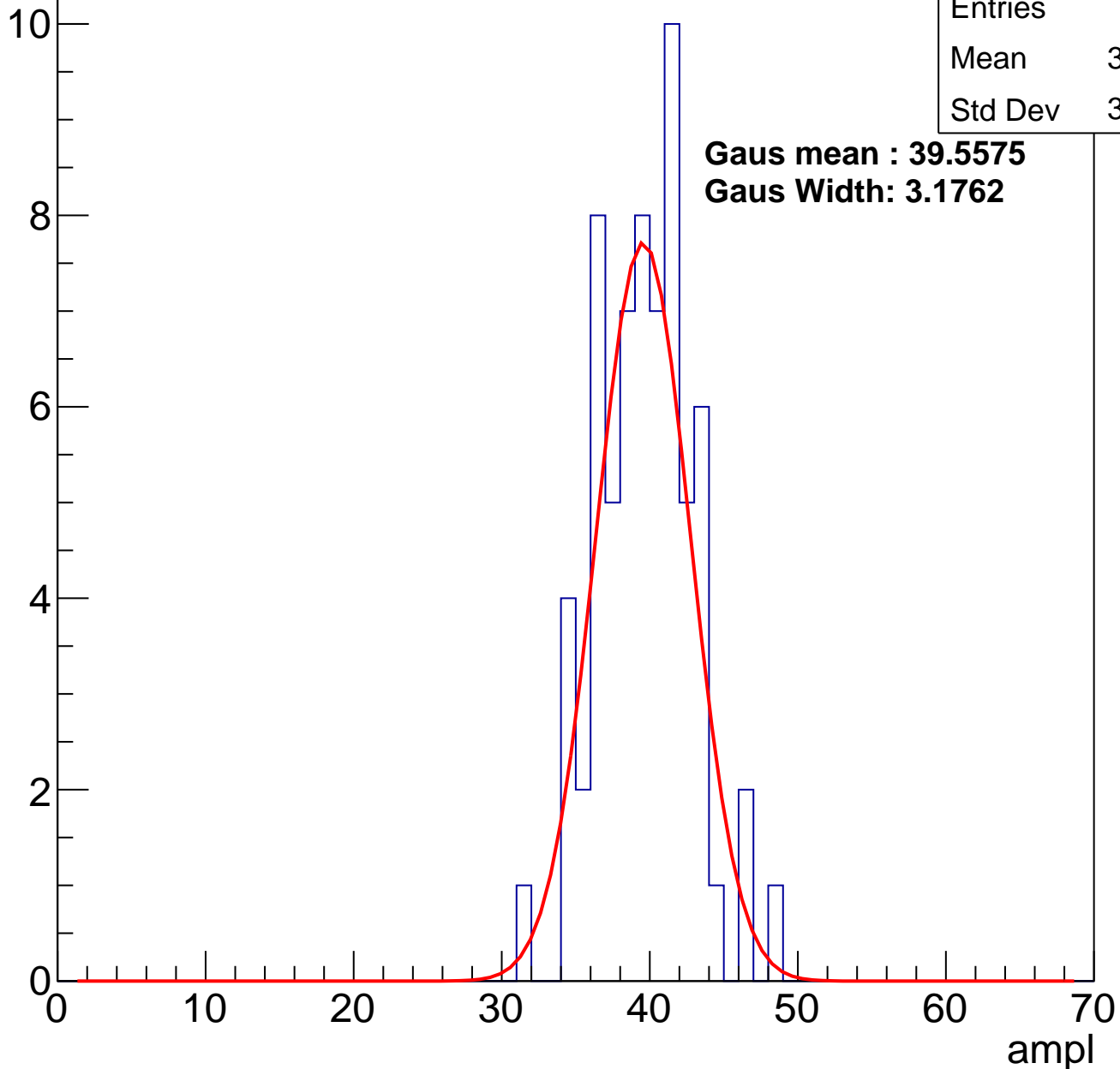
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	67
Mean	39.25
Std Dev	3.192

**Gaus mean : 39.5575**

**Gaus Width: 3.1762**

Entry



# B0L001S, U21-ch75, adc2

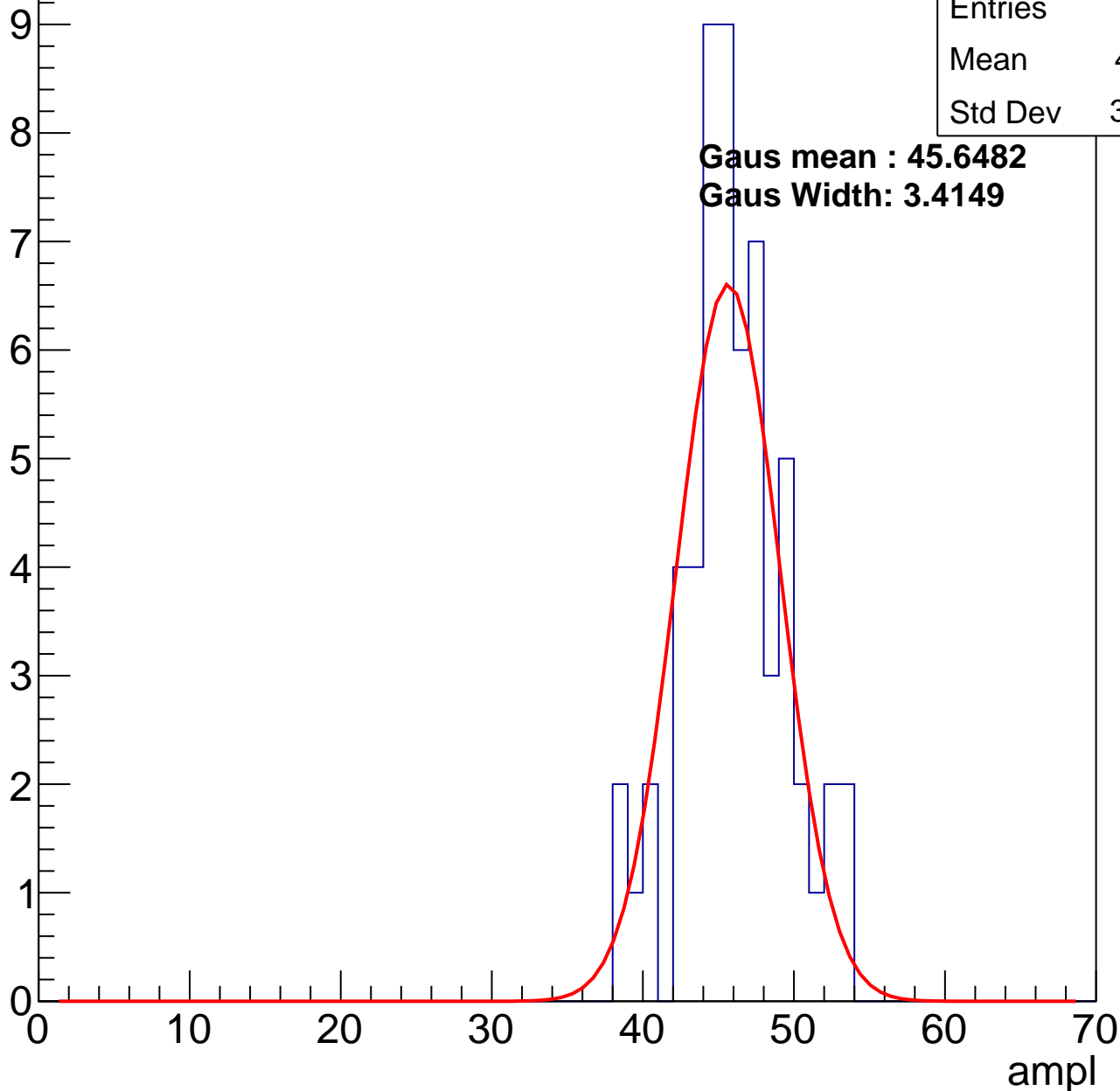
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	45.61
Std Dev	3.385

**Gaus mean : 45.6482**

**Gaus Width: 3.4149**

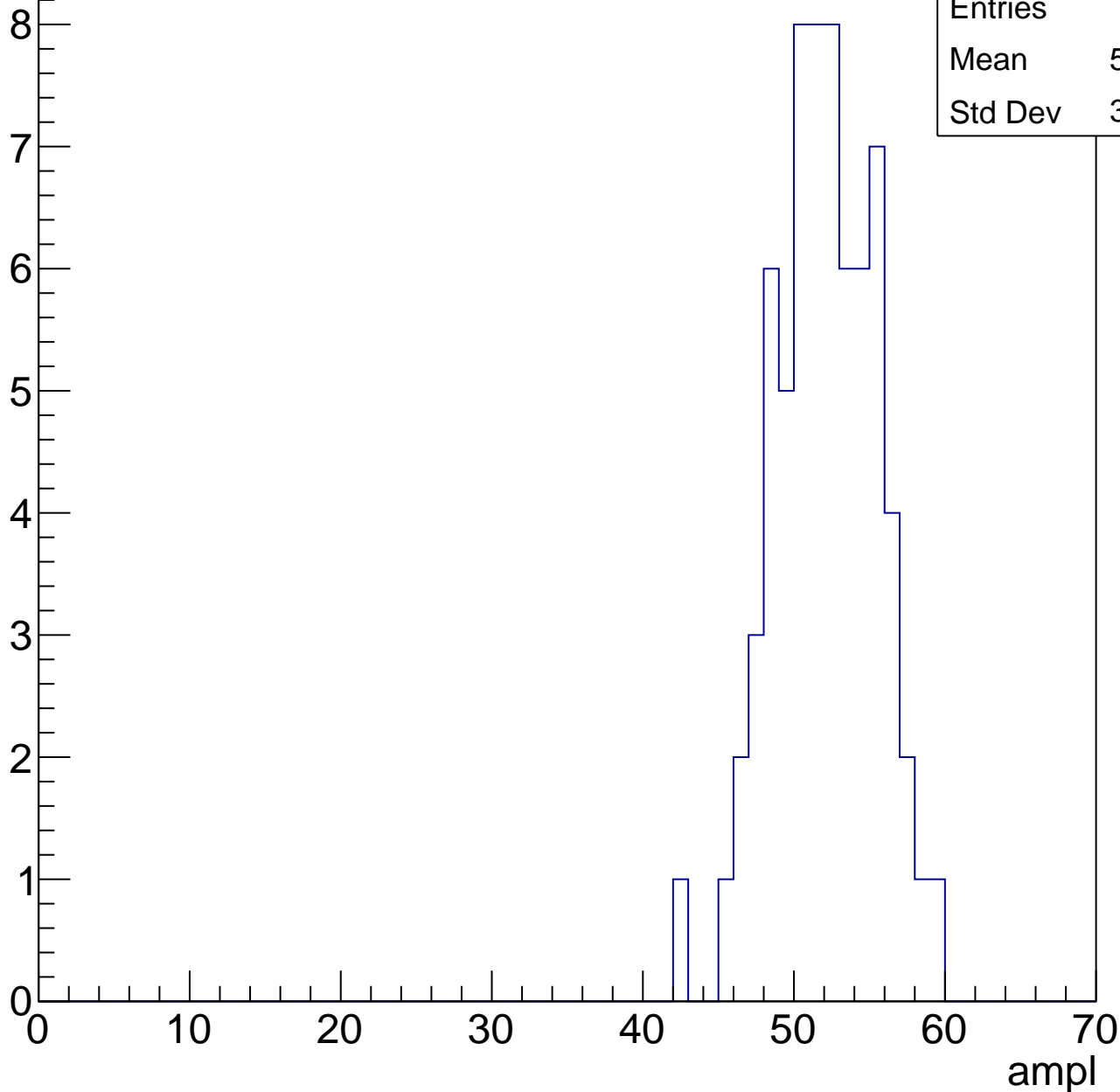


# B0L001S, U21-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	51.58
Std Dev	3.312

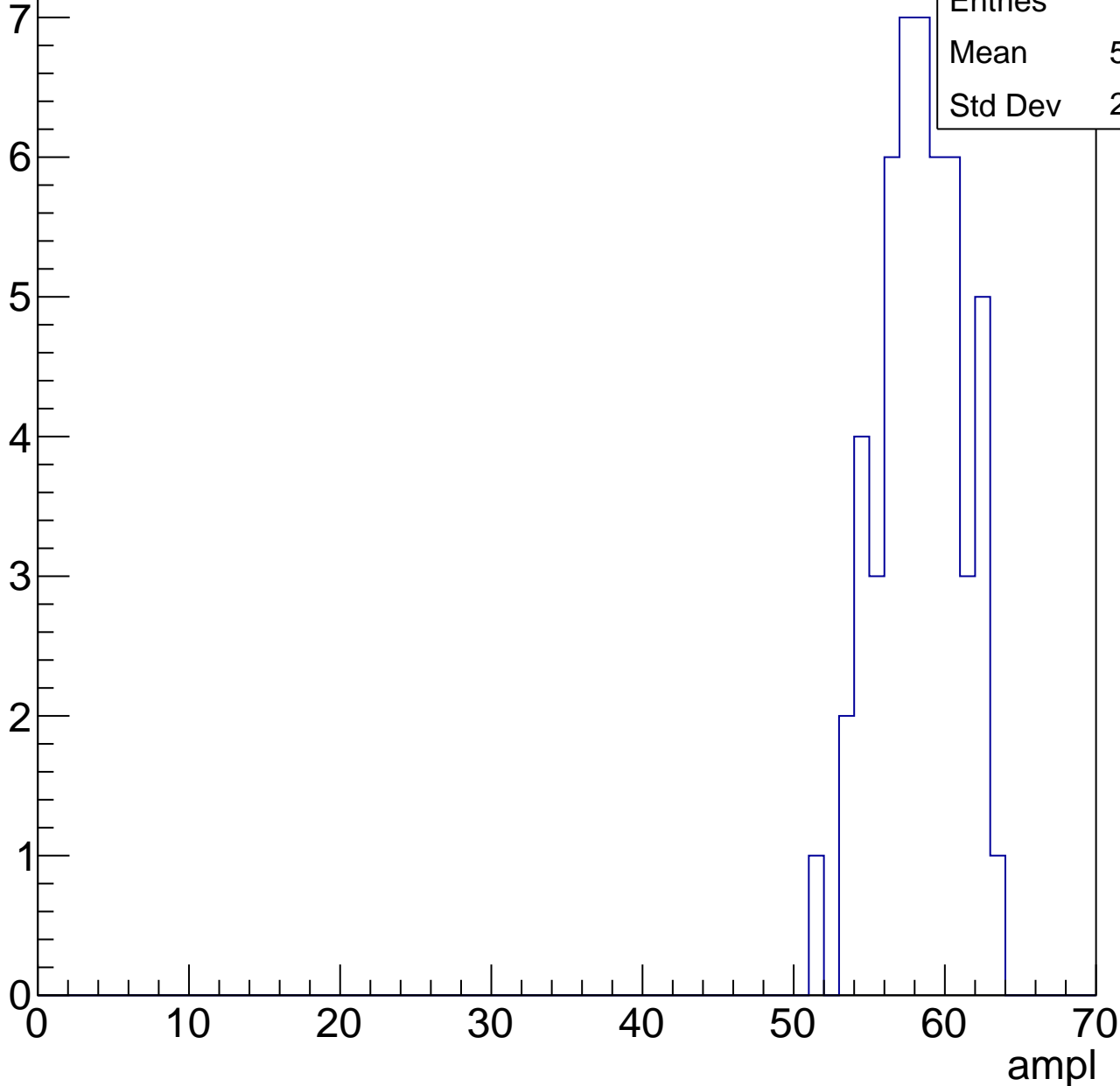


# B0L001S, U21-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	57.82
Std Dev	2.735

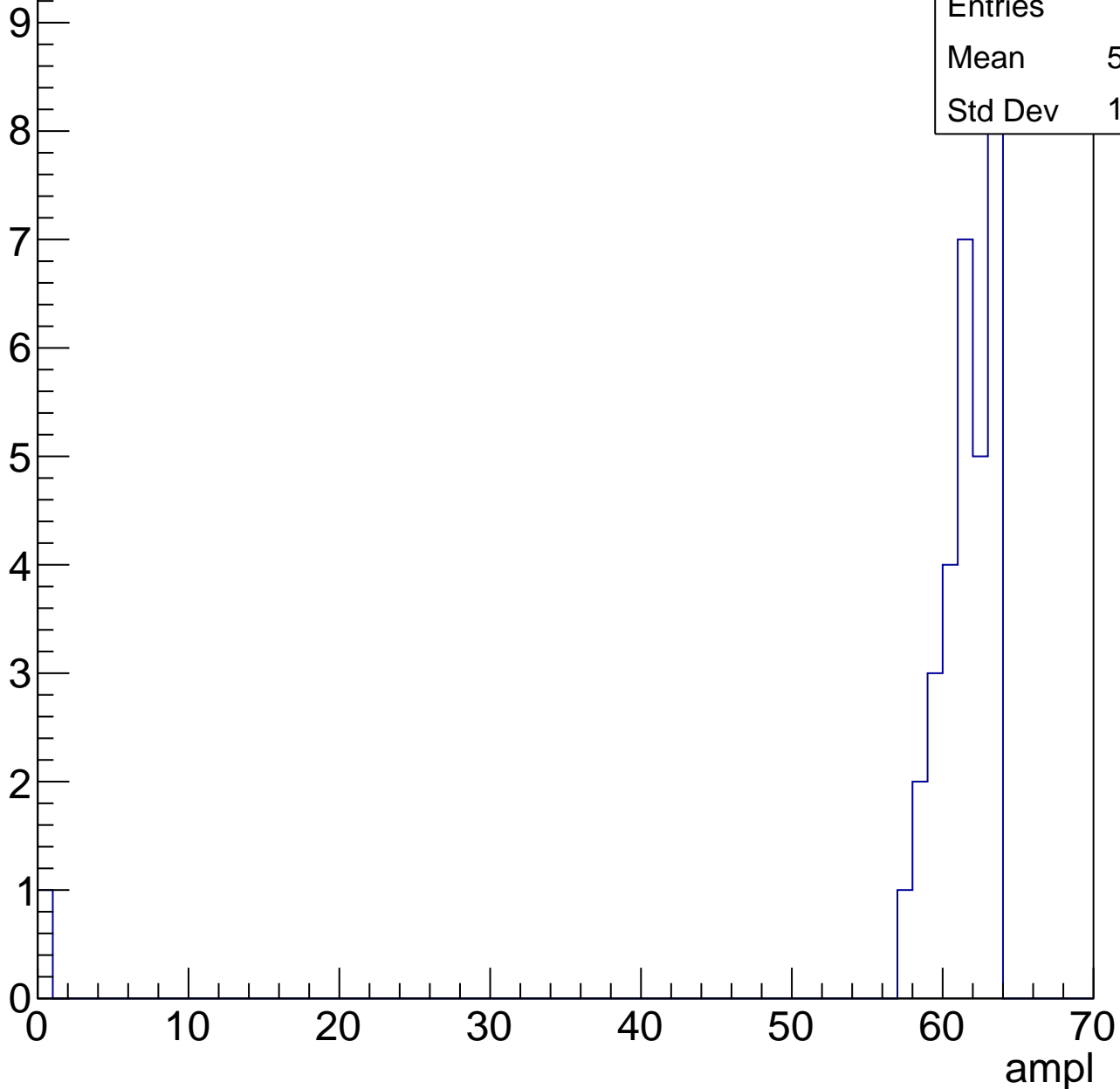


# B0L001S, U21-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	32
Mean	59.19
Std Dev	10.76



# B0L001S, U21-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch76, adc0

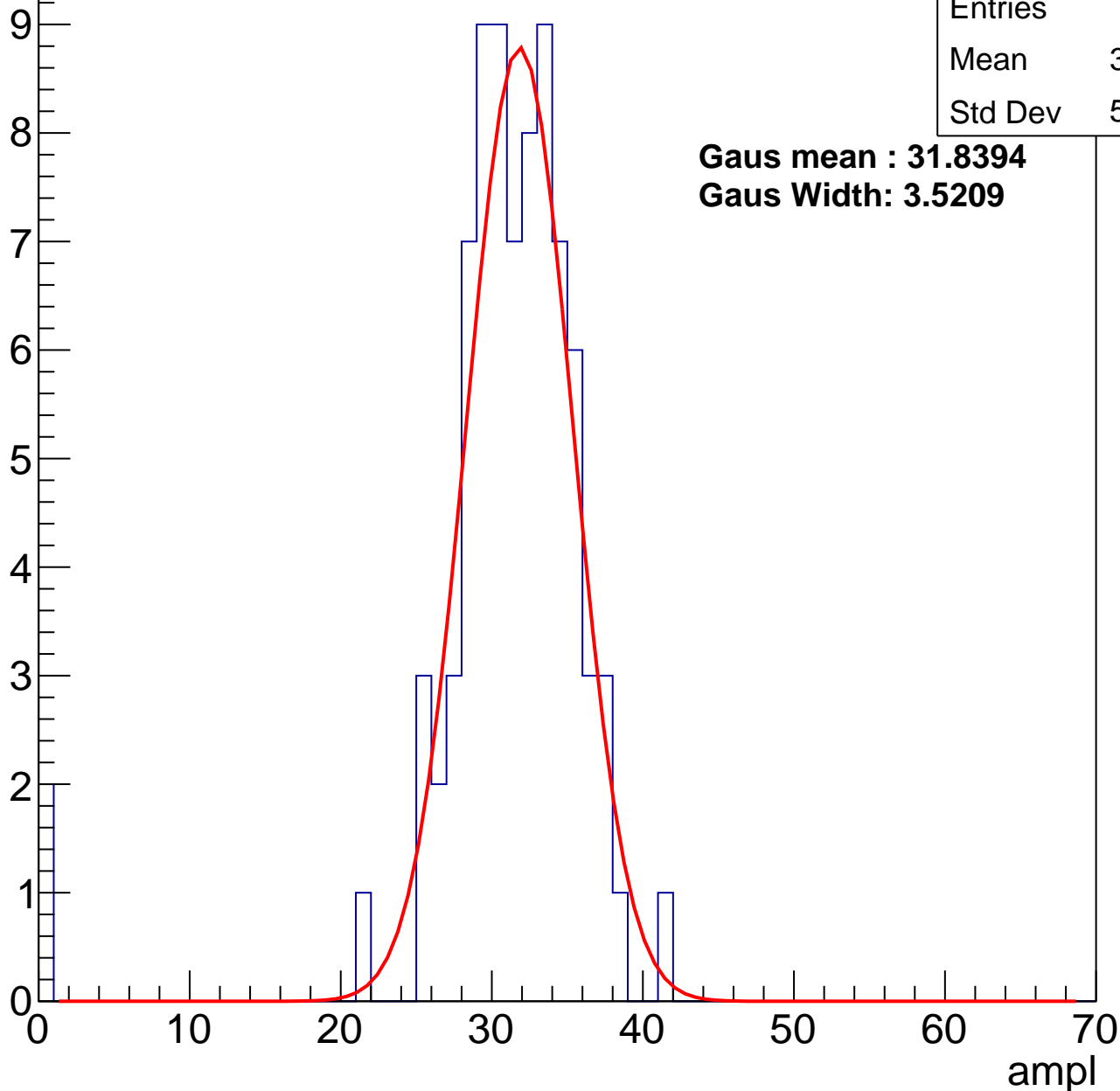
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	30.52
Std Dev	5.934

**Gaus mean : 31.8394**

**Gaus Width: 3.5209**



# B0L001S, U21-ch76, adc1

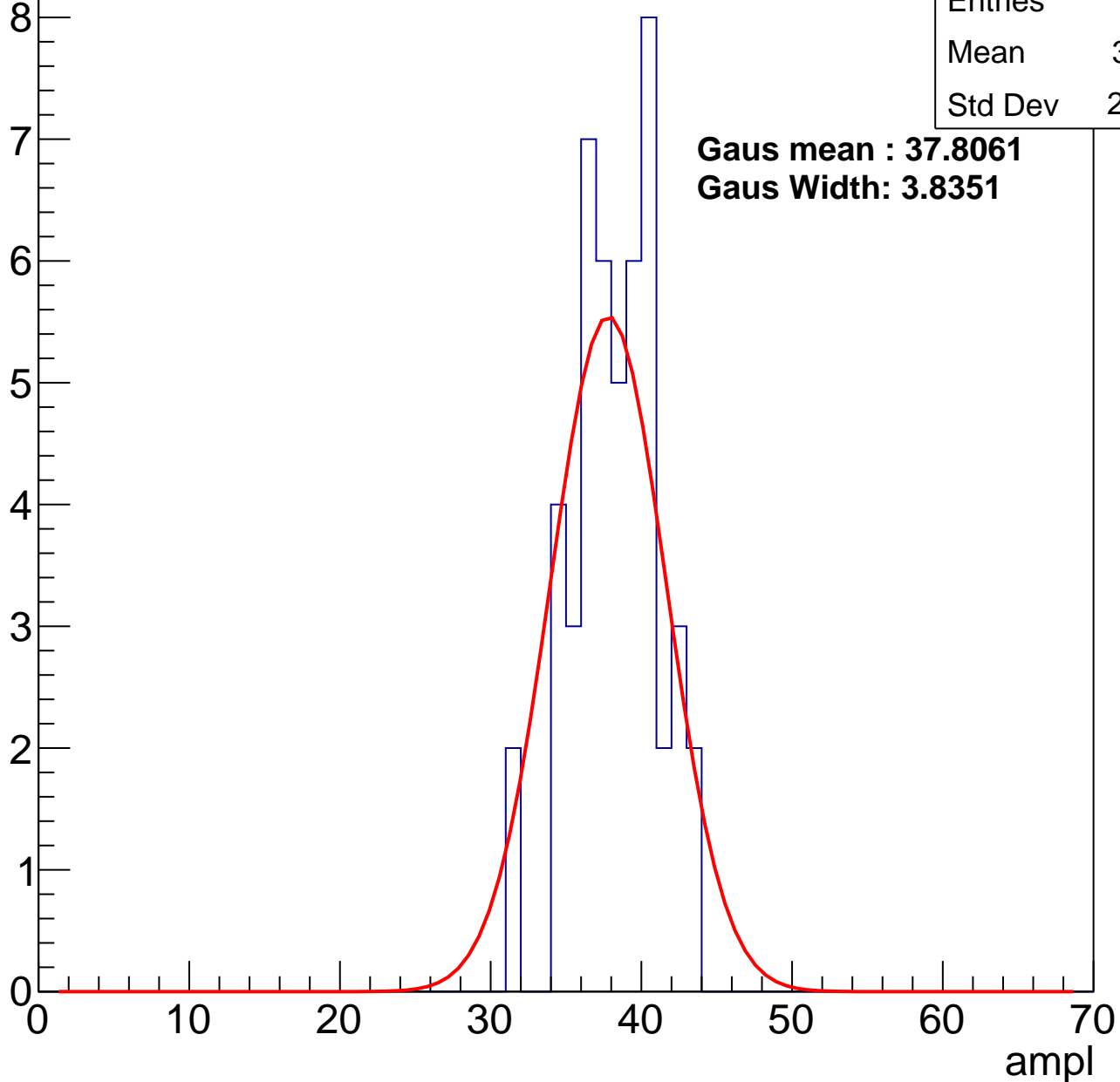
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	37.81
Std Dev	2.796

**Gaus mean : 37.8061**

**Gaus Width: 3.8351**



# B0L001S, U21-ch76, adc2

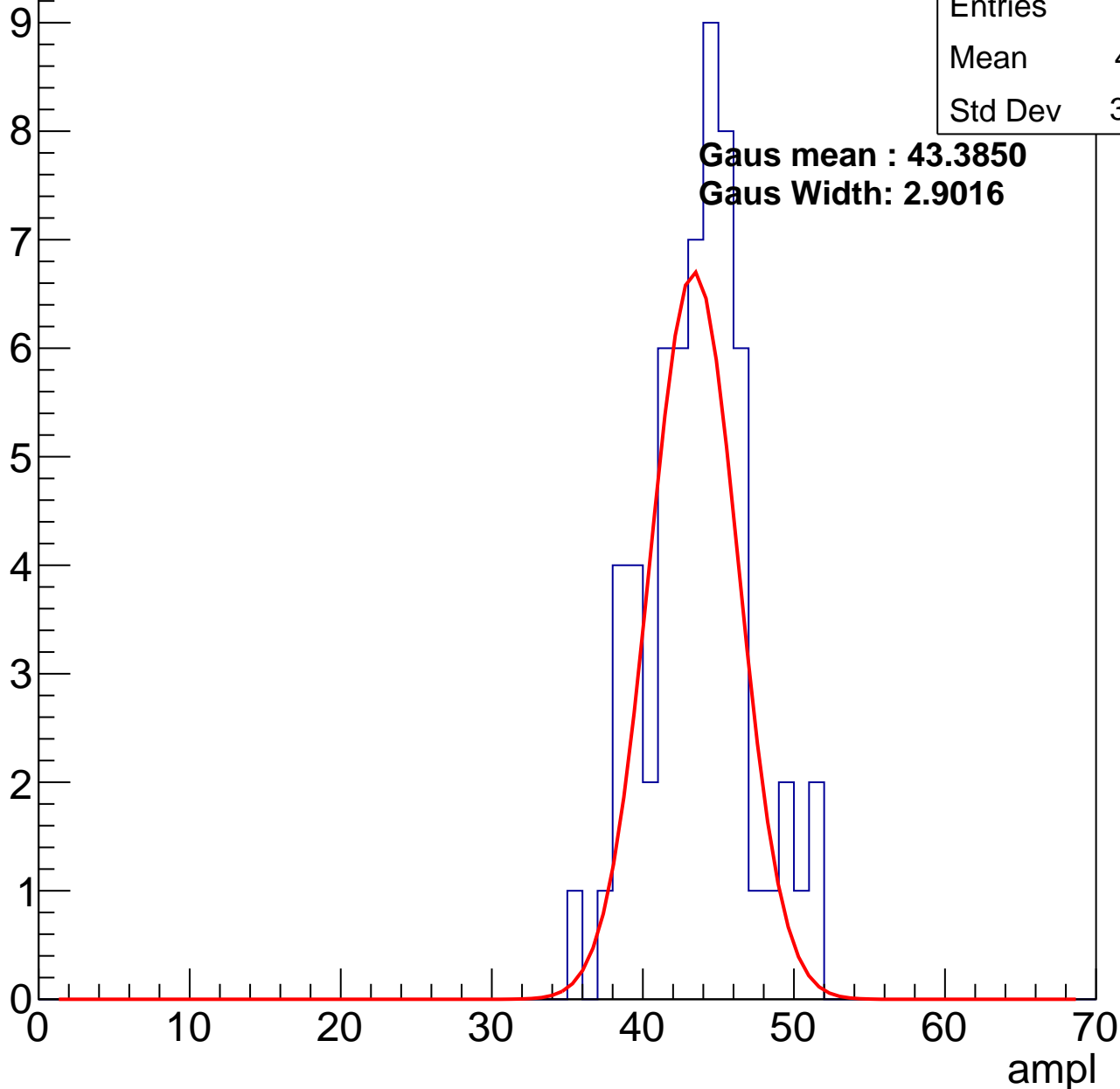
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	43.21
Std Dev	3.374

**Gaus mean : 43.3850**

**Gaus Width: 2.9016**

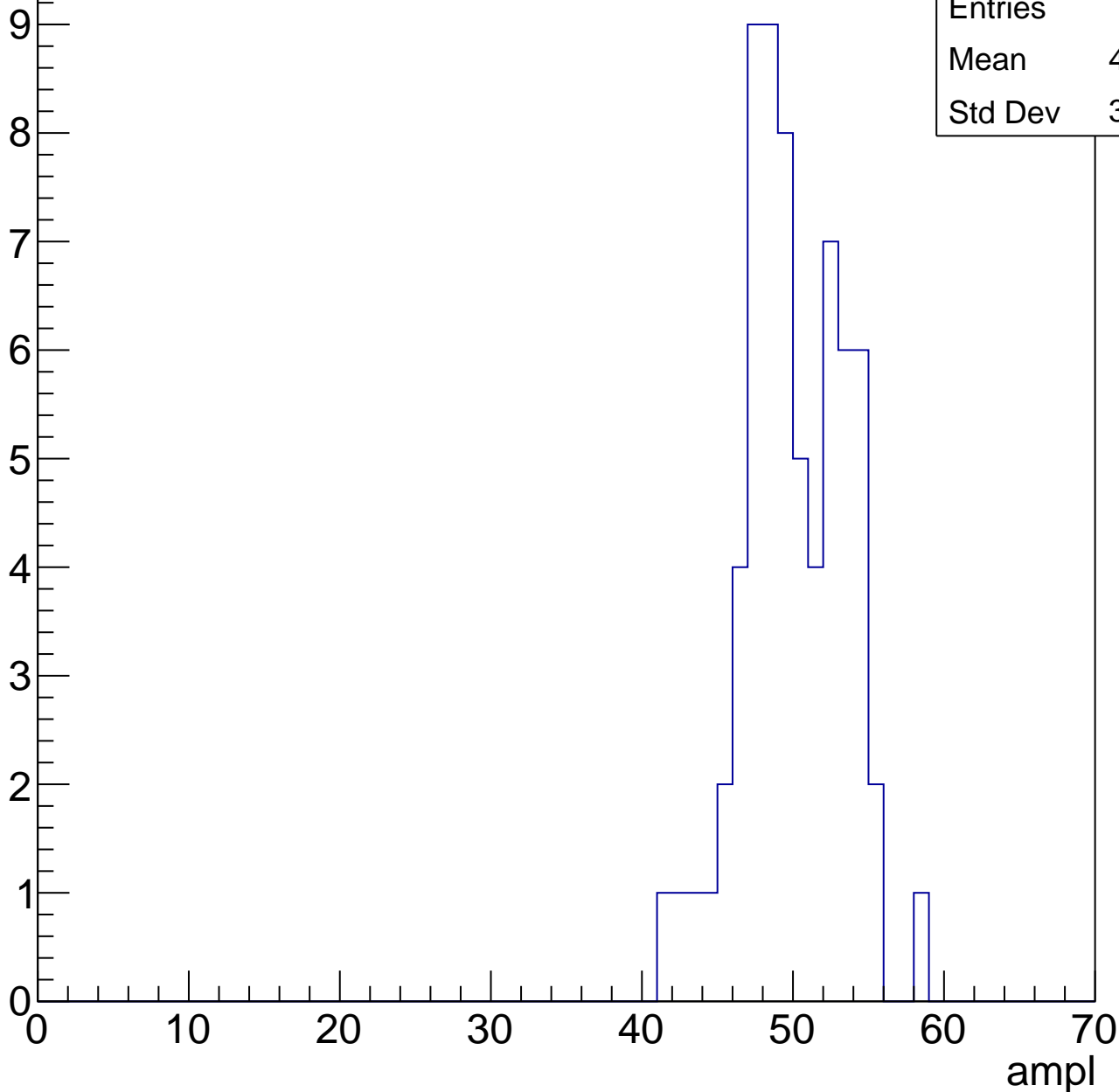


# B0L001S, U21-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	49.54
Std Dev	3.347

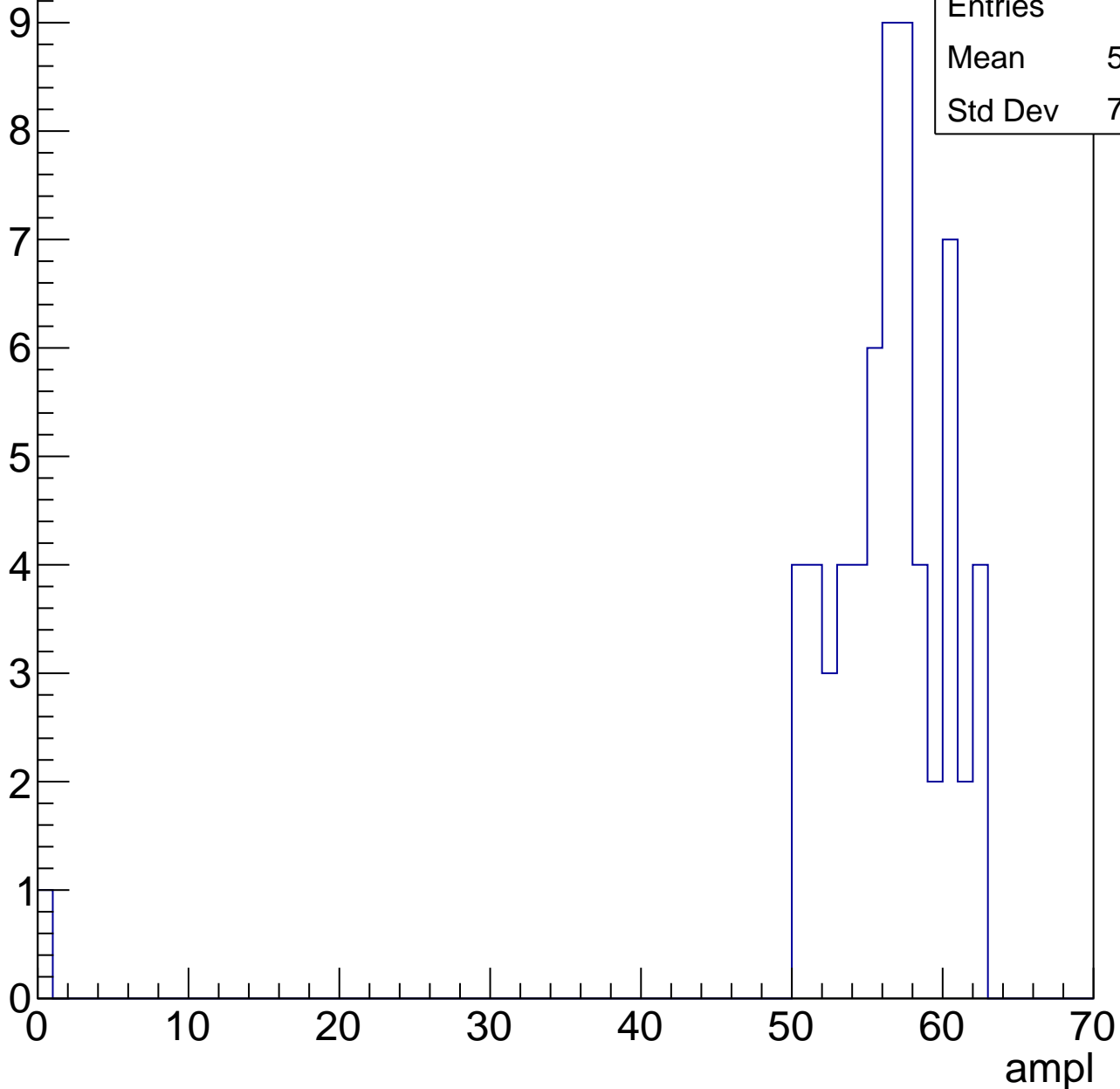


# B0L001S, U21-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

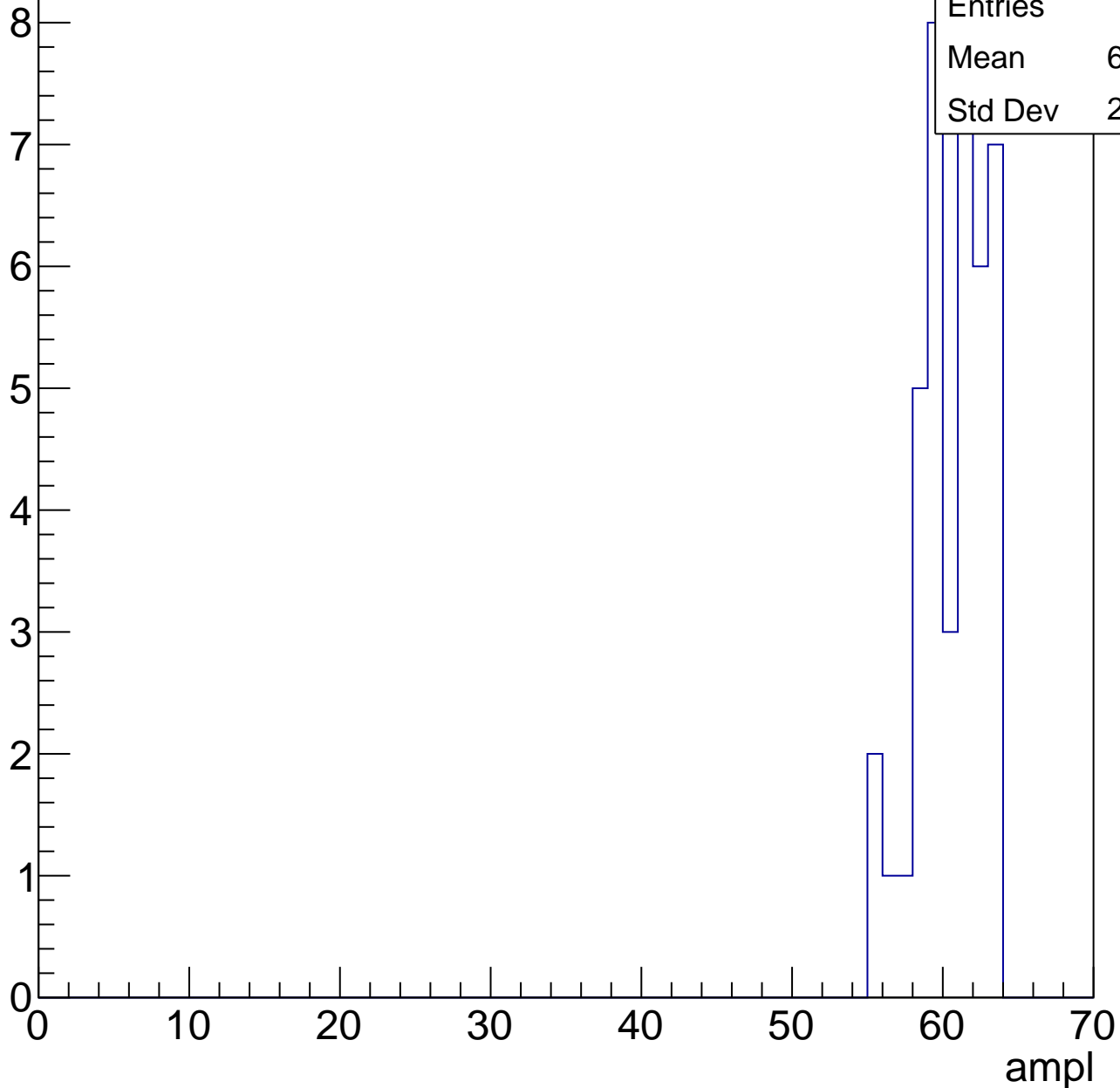
Entries	63
Mean	55.16
Std Dev	7.757



# B0L001S, U21-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	41
Mean	60.15
Std Dev	2.193

# B0L001S, U21-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch77, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	77
Mean	30.87
Std Dev	3.424

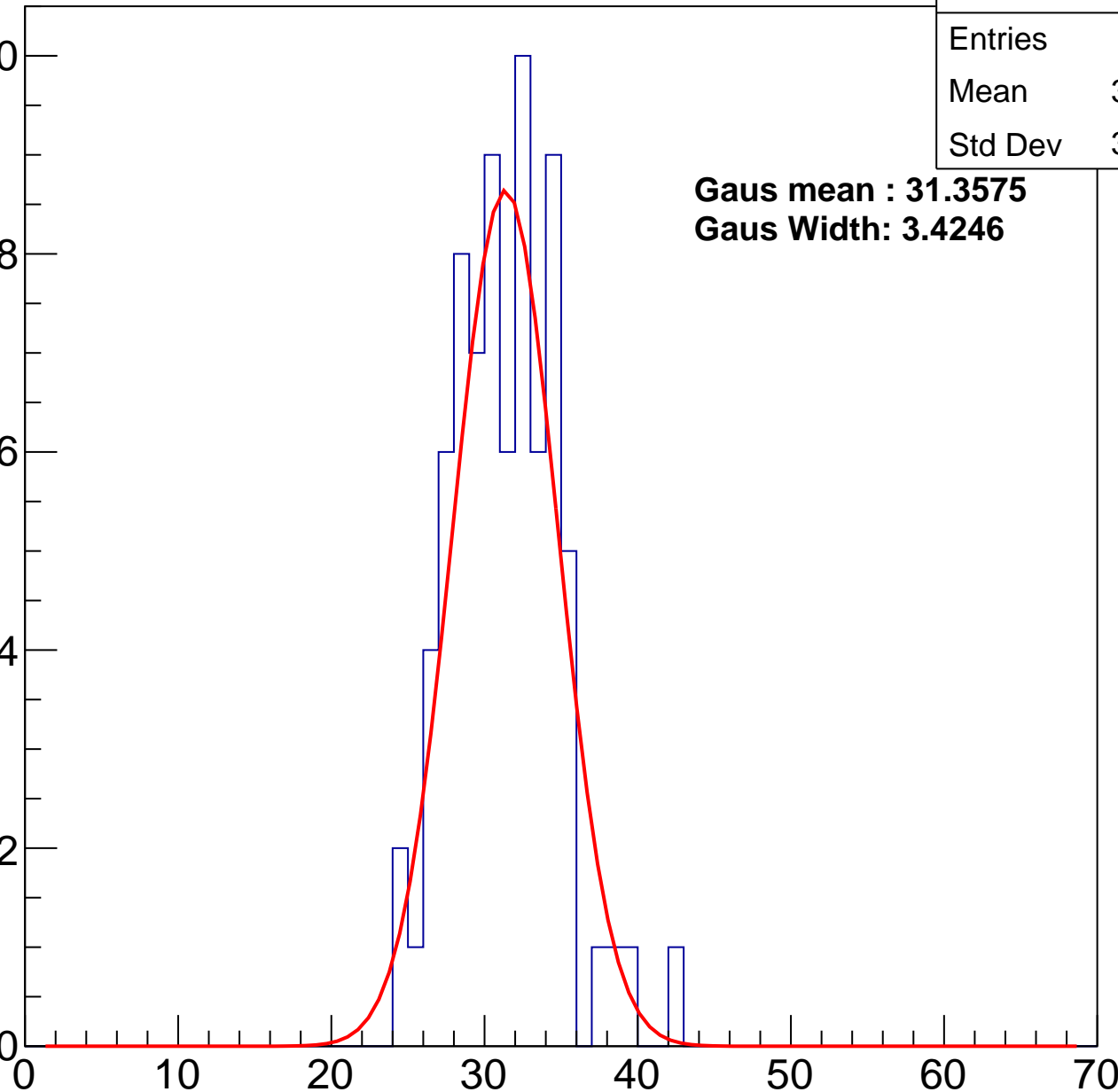
**Gaus mean : 31.3575**

**Gaus Width: 3.4246**

Entry

10  
8  
6  
4  
2  
0

ampl



# B0L001S, U21-ch77, adc1

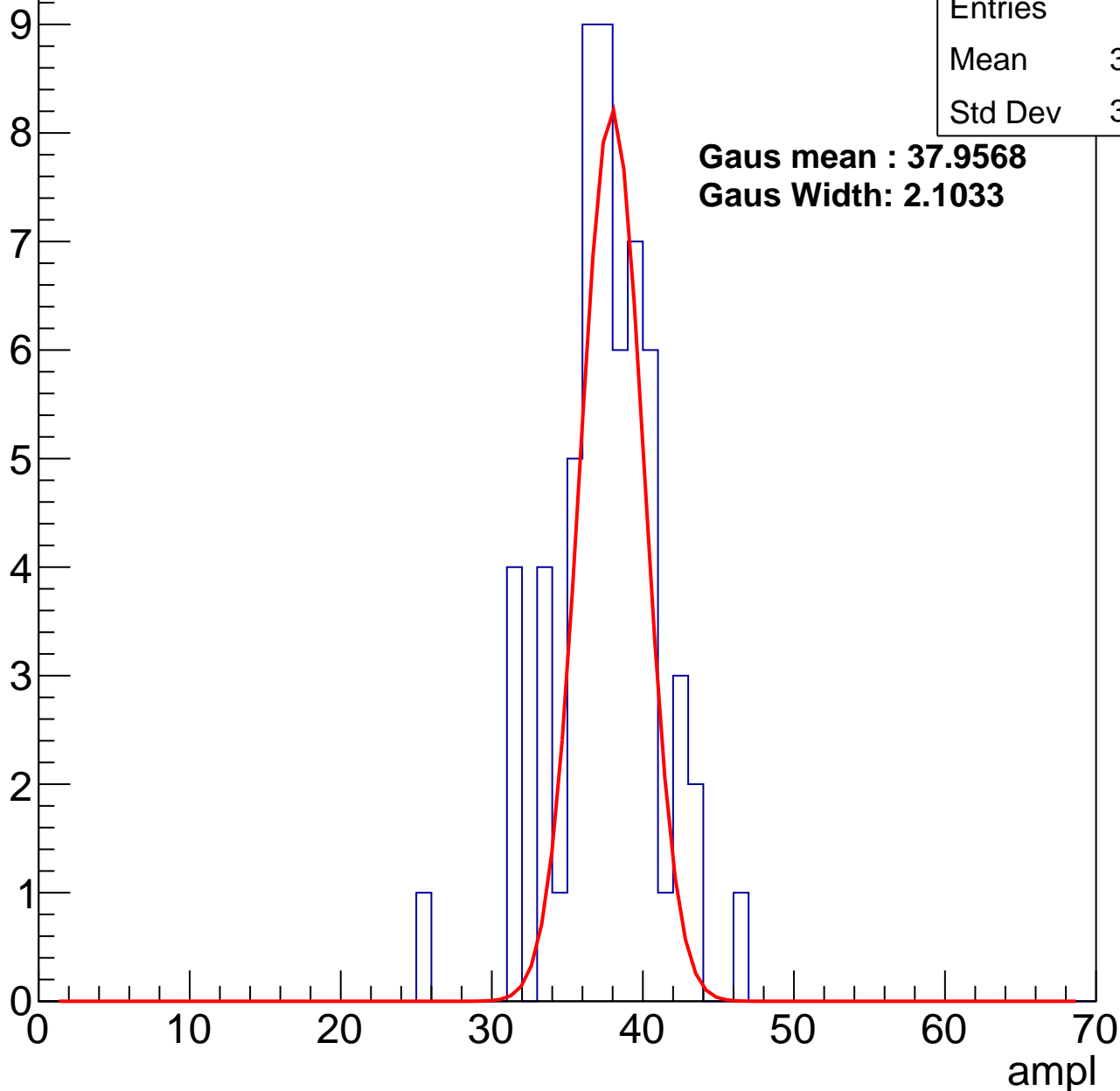
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	37.07
Std Dev	3.498

**Gaus mean : 37.9568**

**Gaus Width: 2.1033**



# B0L001S, U21-ch77, adc2

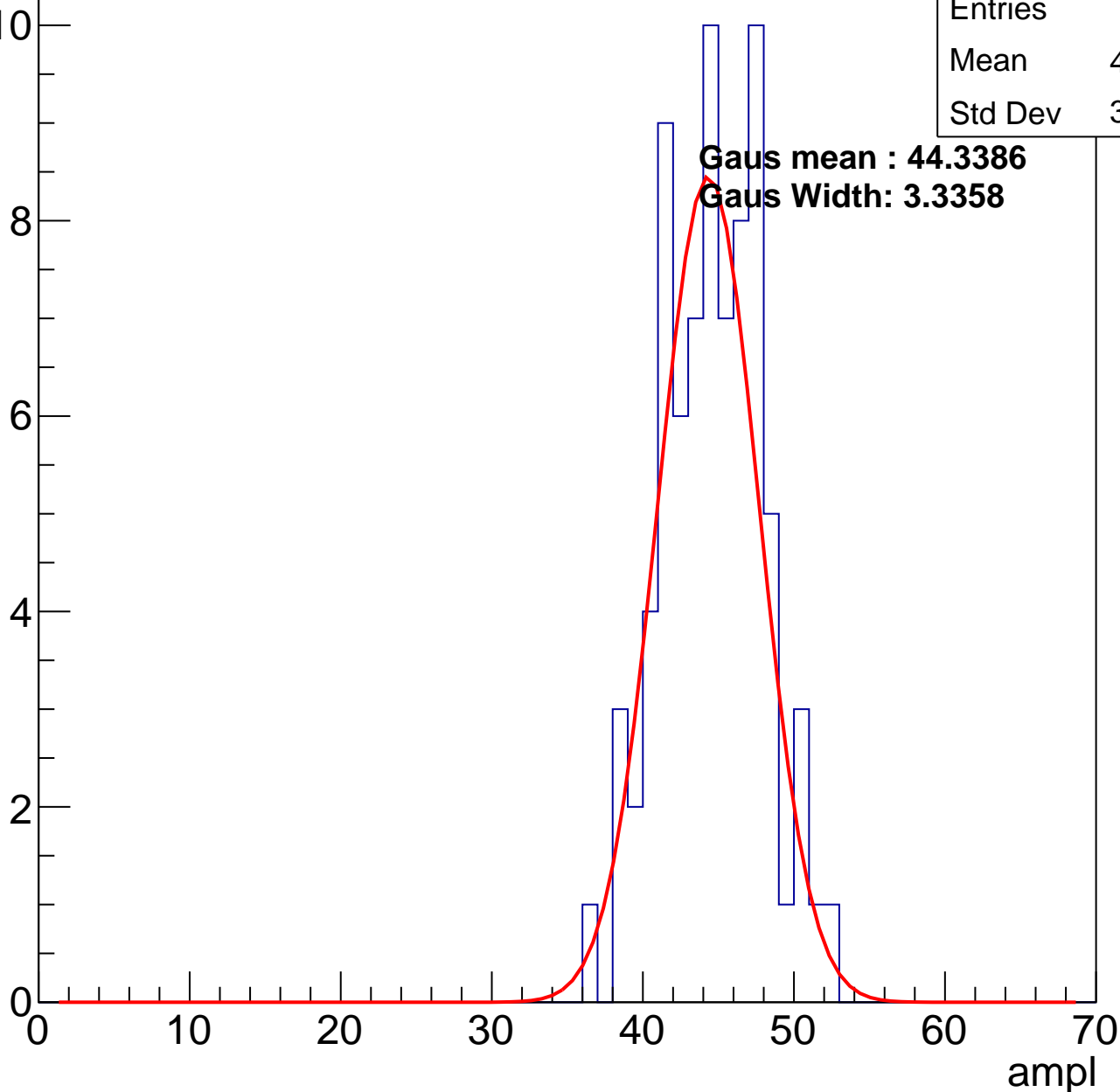
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	44.17
Std Dev	3.303

**Gaus mean : 44.3386**

**Gaus Width: 3.3358**

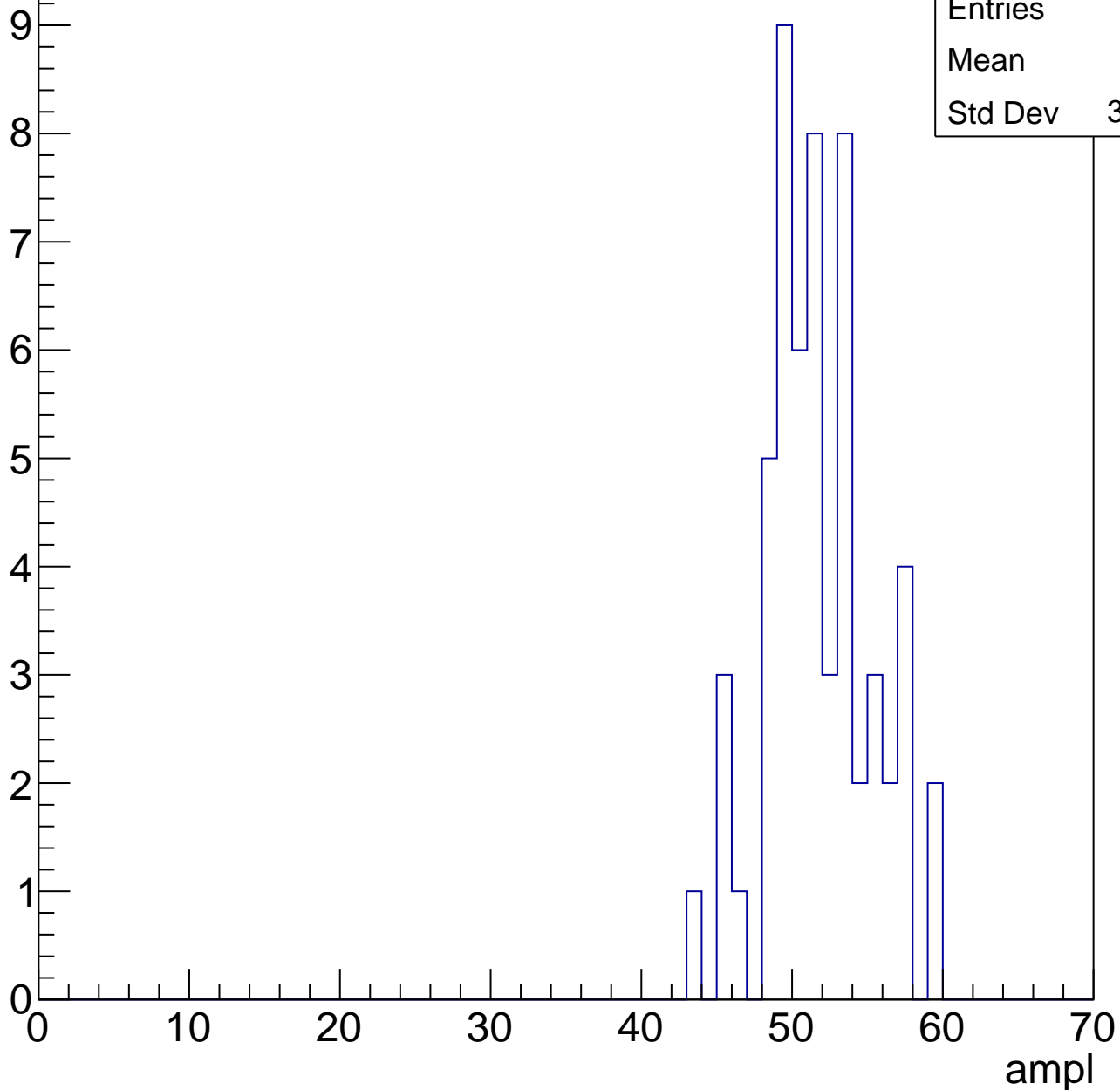


# B0L001S, U21-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

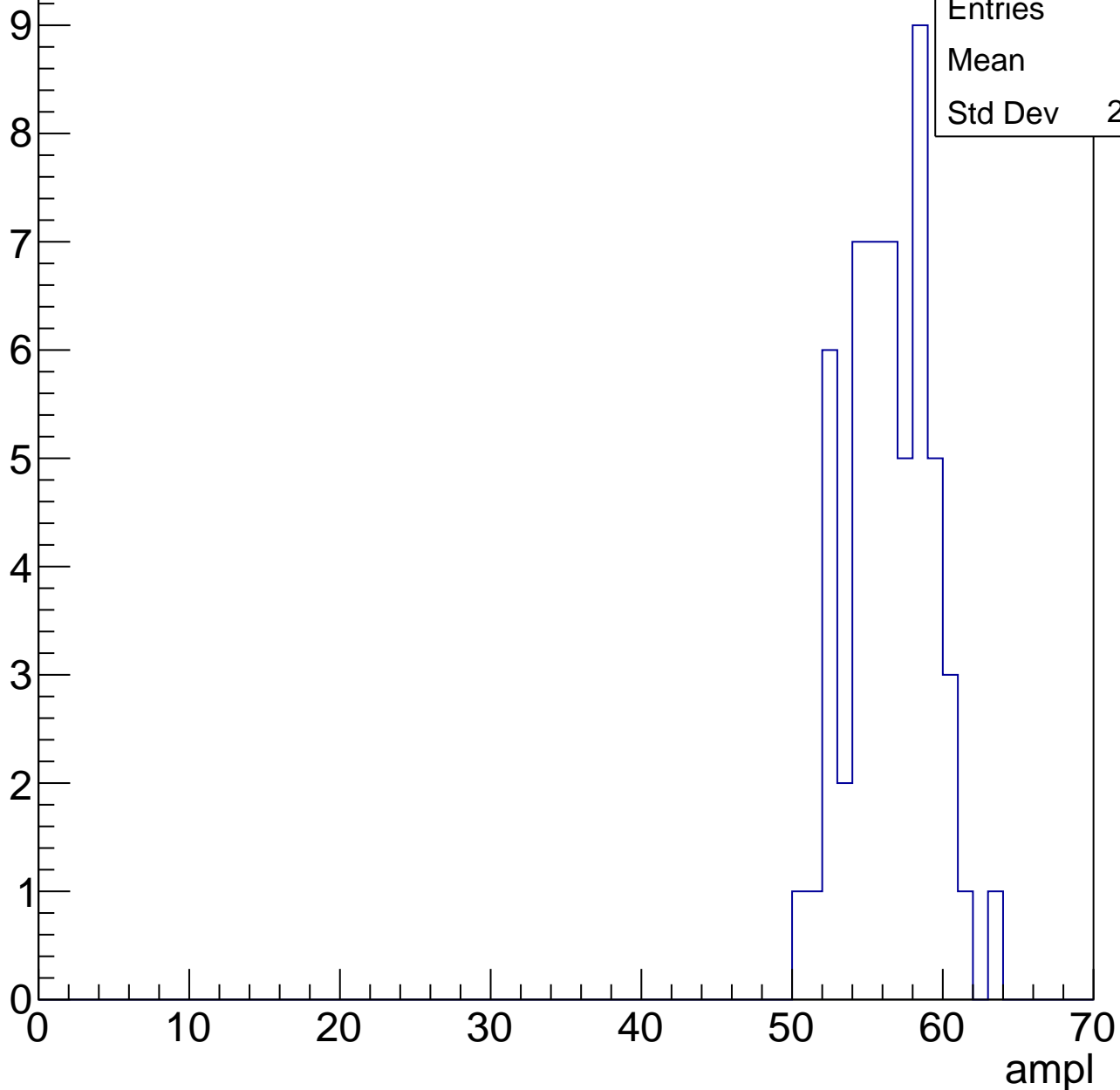
Entries	57
Mean	51.3
Std Dev	3.509



# B0L001S, U21-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

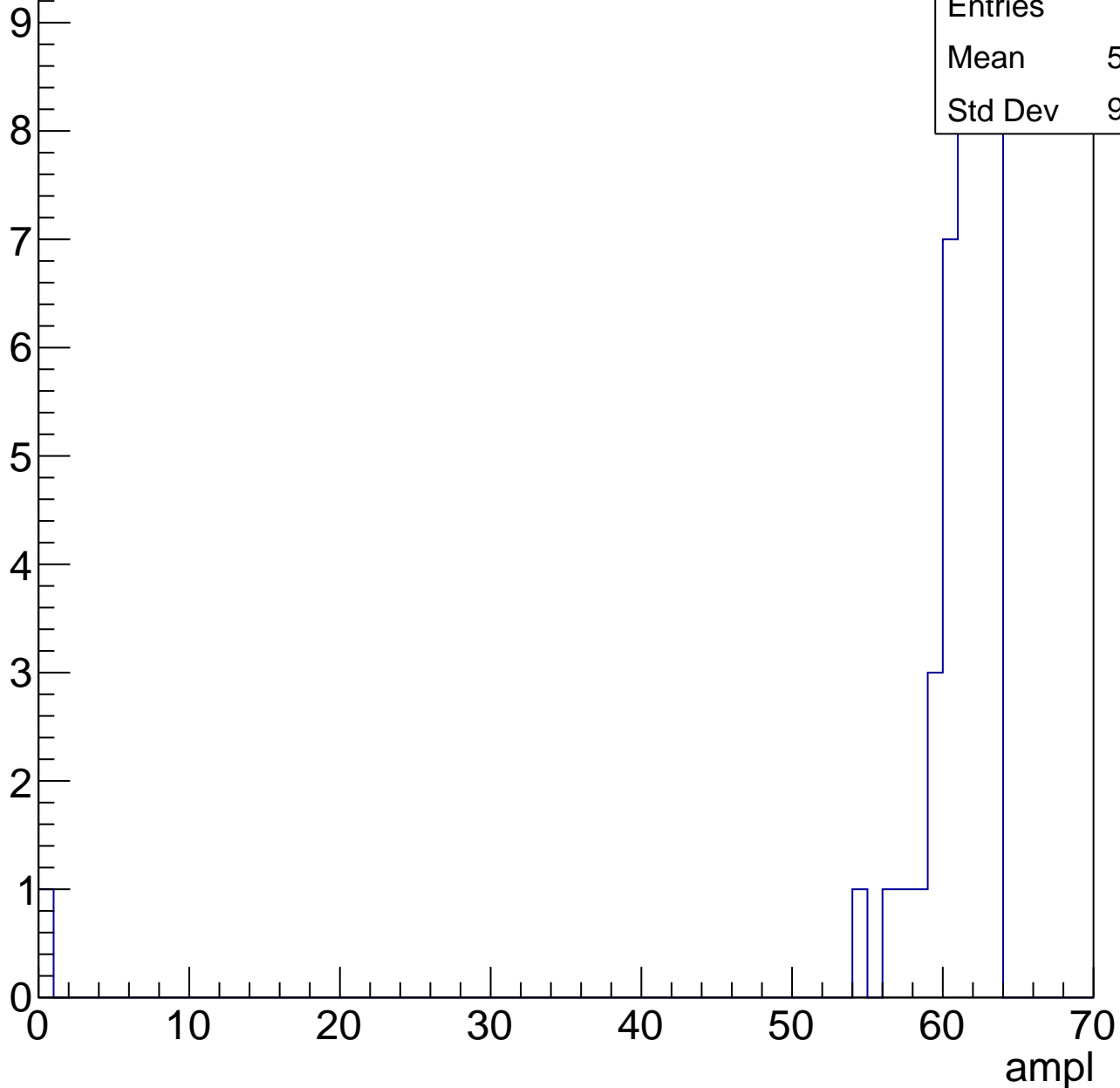
Entry



# B0L001S, U21-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B0L001S, U21-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch78, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	68
Mean	30.53
Std Dev	4.888

**Gaus mean : 31.8466**

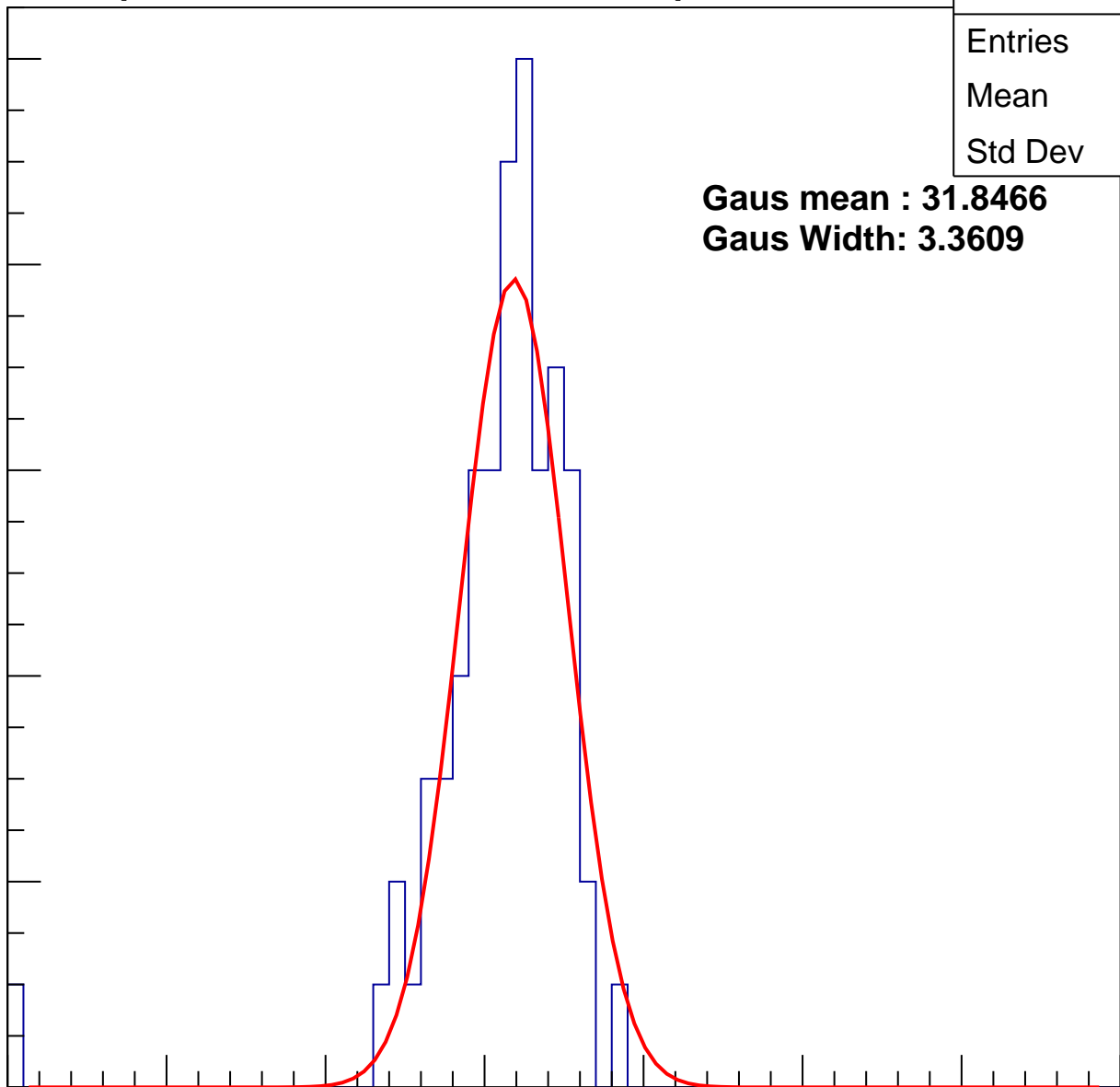
**Gaus Width: 3.3609**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



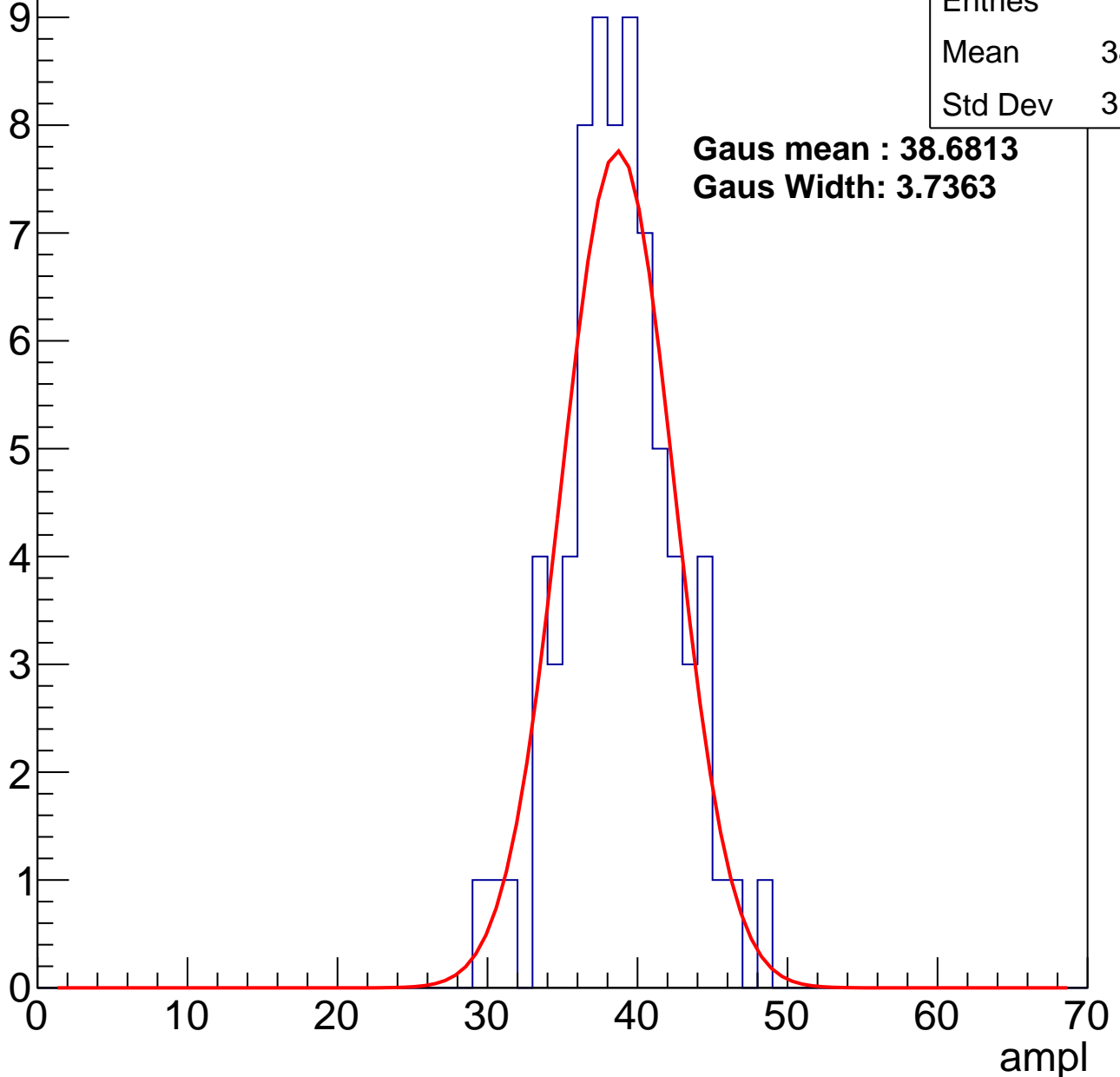
# B0L001S, U21-ch78, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	38.34
Std Dev	3.655

**Gaus mean : 38.6813**  
**Gaus Width: 3.7363**

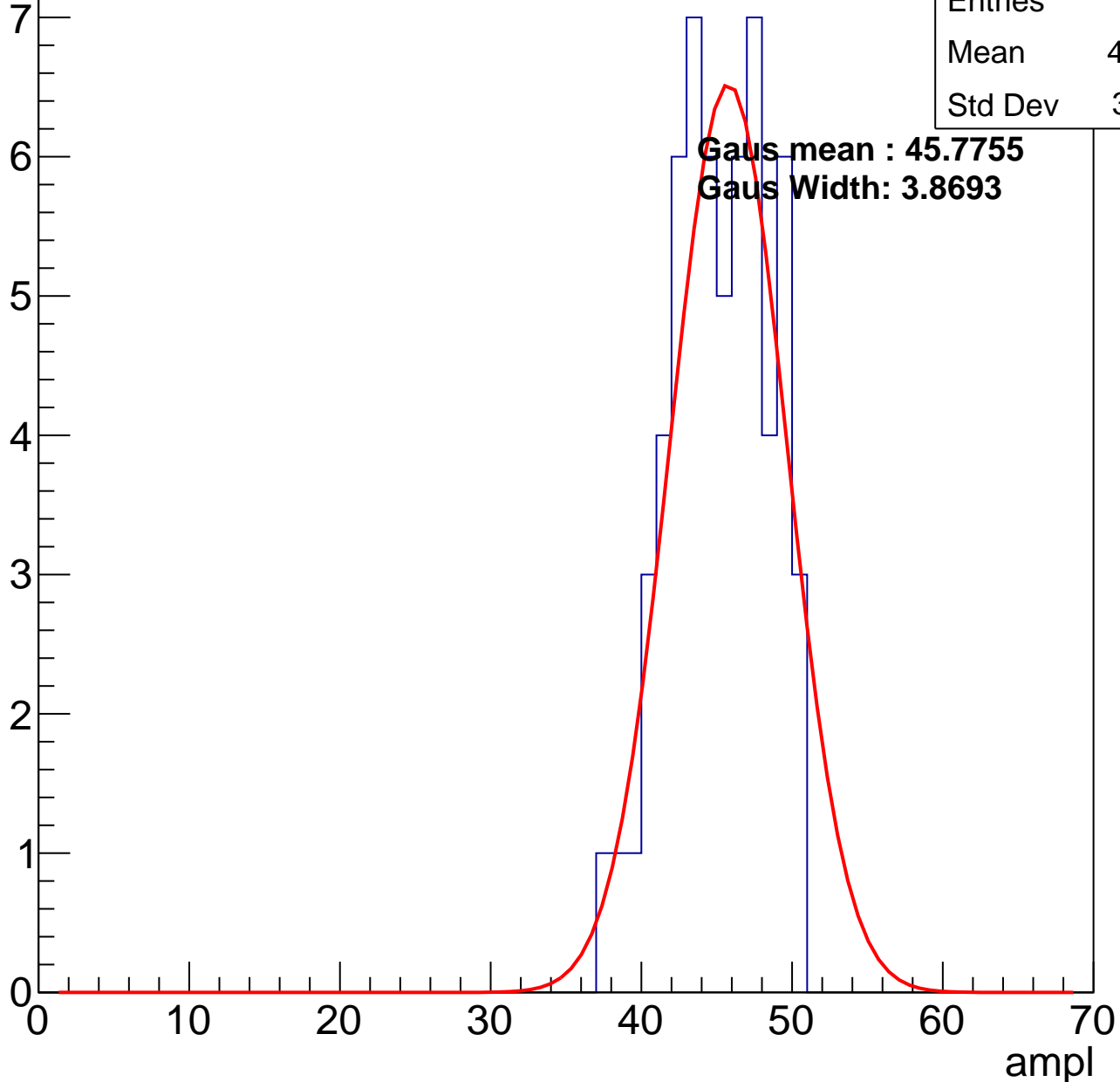


# B0L001S, U21-ch78, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

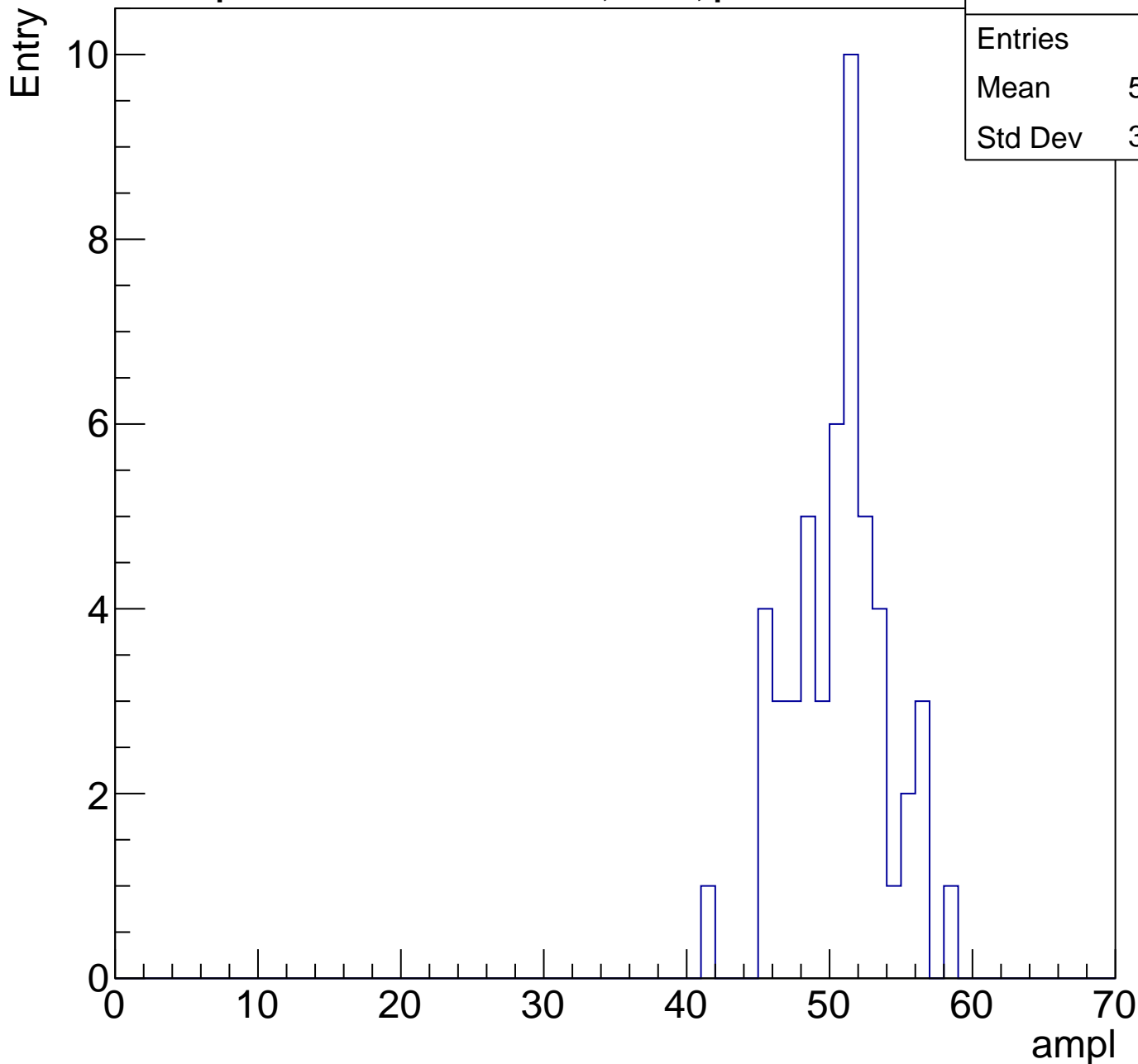
Entries	60
Mean	44.68
Std Dev	3.191



# B0L001S, U21-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

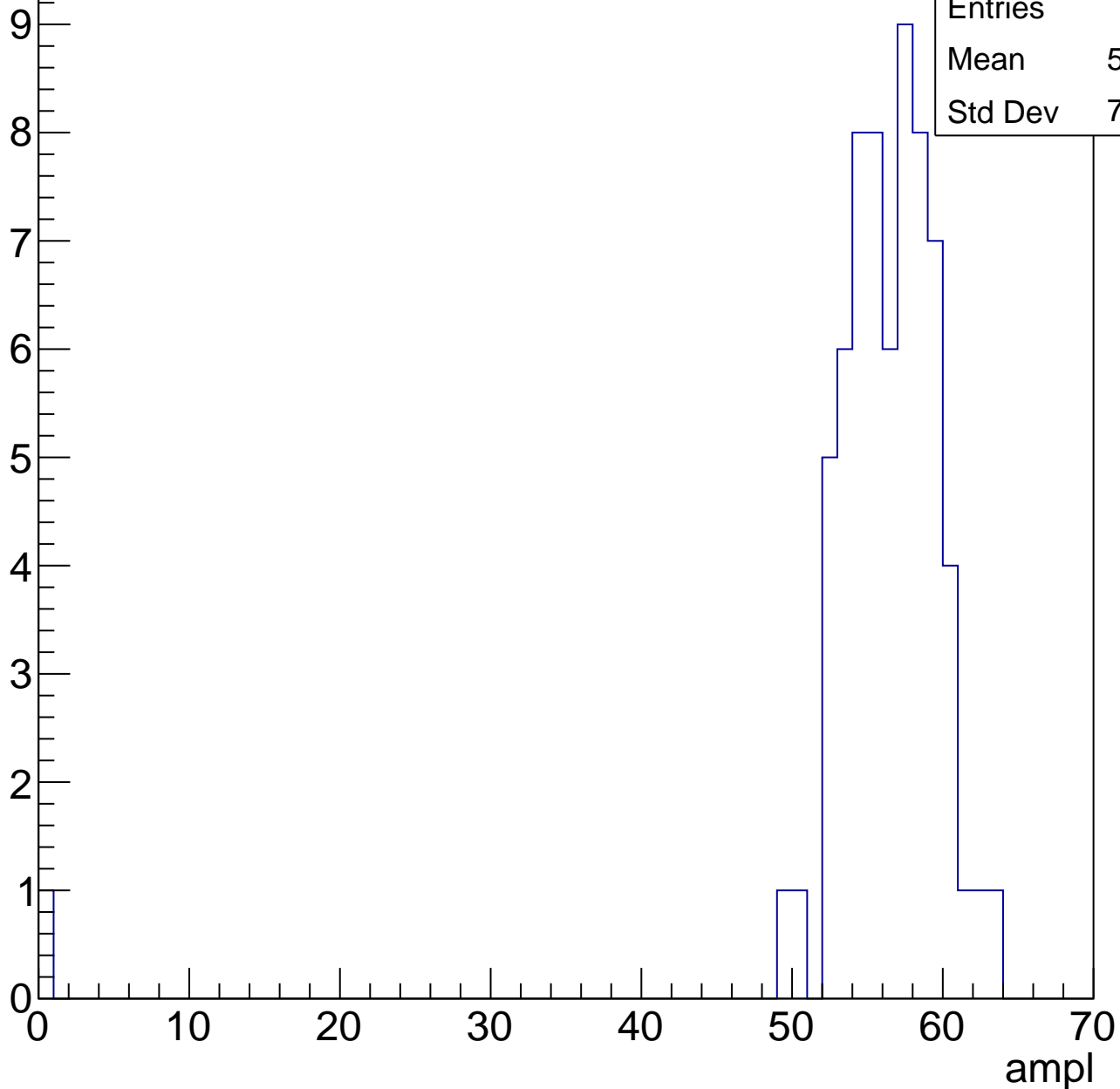
Entries	51
Mean	50.18
Std Dev	3.376



# B0L001S, U21-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

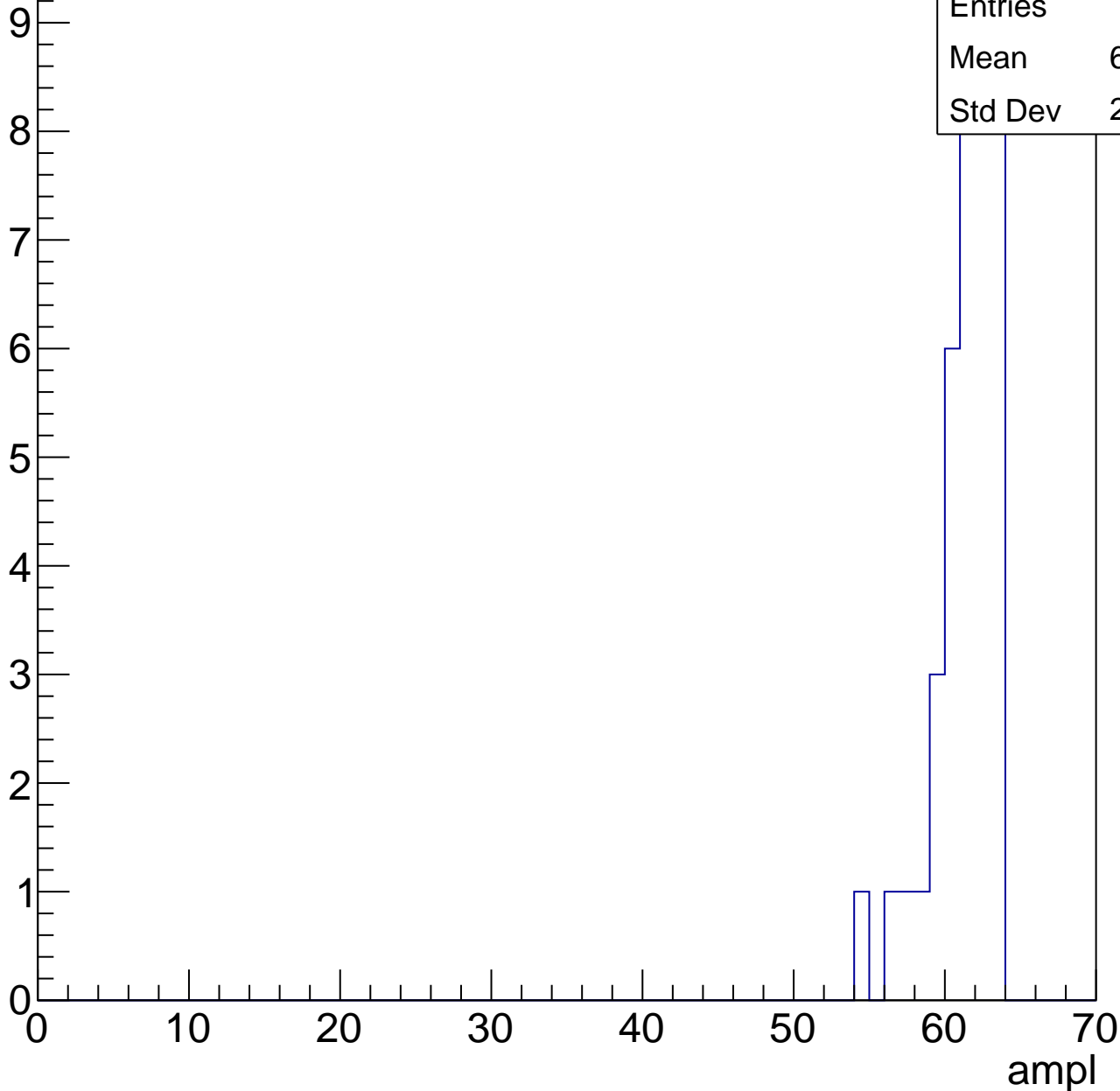


# B0L001S, U21-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	38
Mean	60.84
Std Dev	2.033



# B0L001S, U21-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U21-ch79, adc0

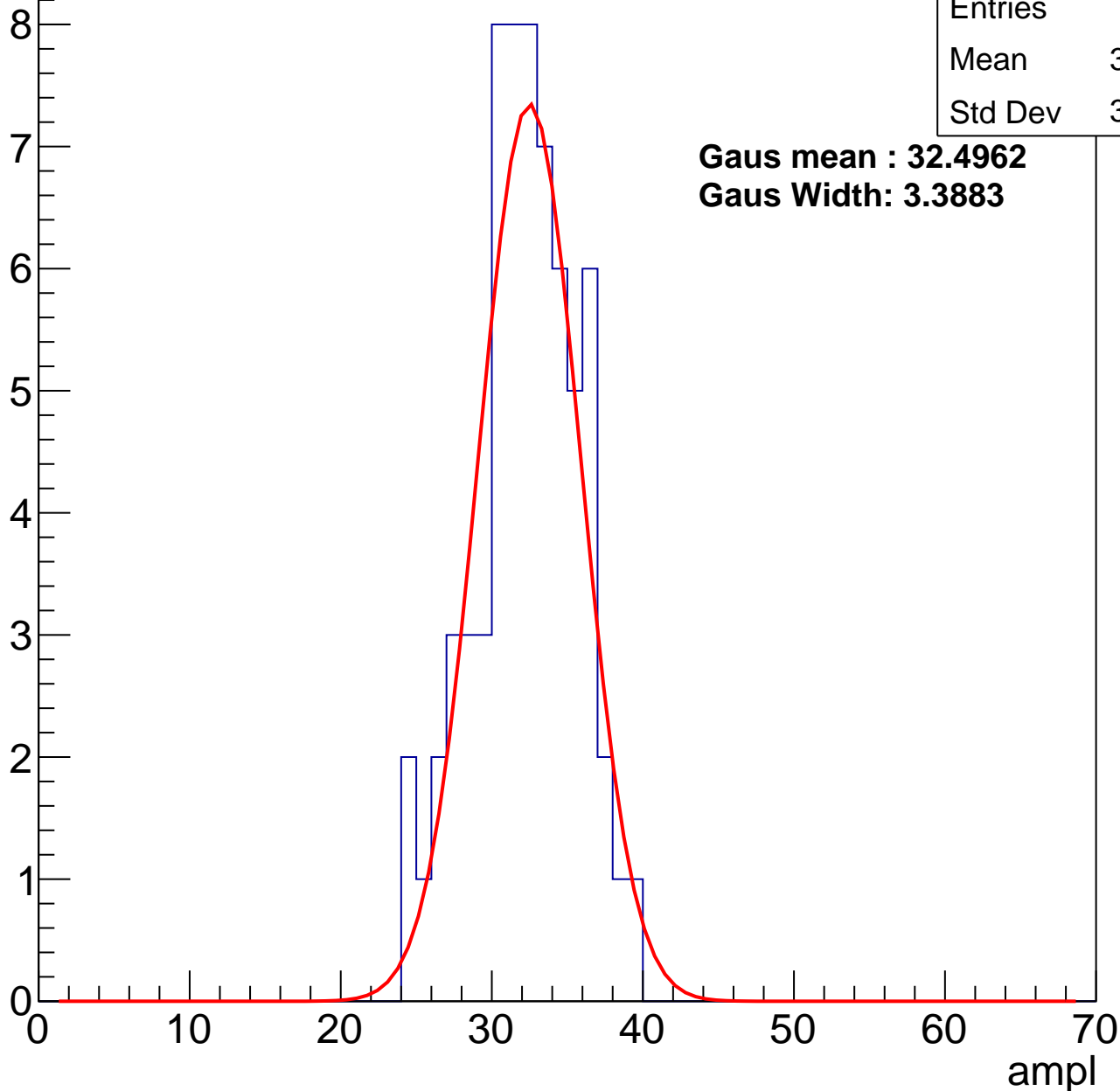
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	31.79
Std Dev	3.355

**Gaus mean : 32.4962**

**Gaus Width: 3.3883**



# B0L001S, U21-ch79, adc1

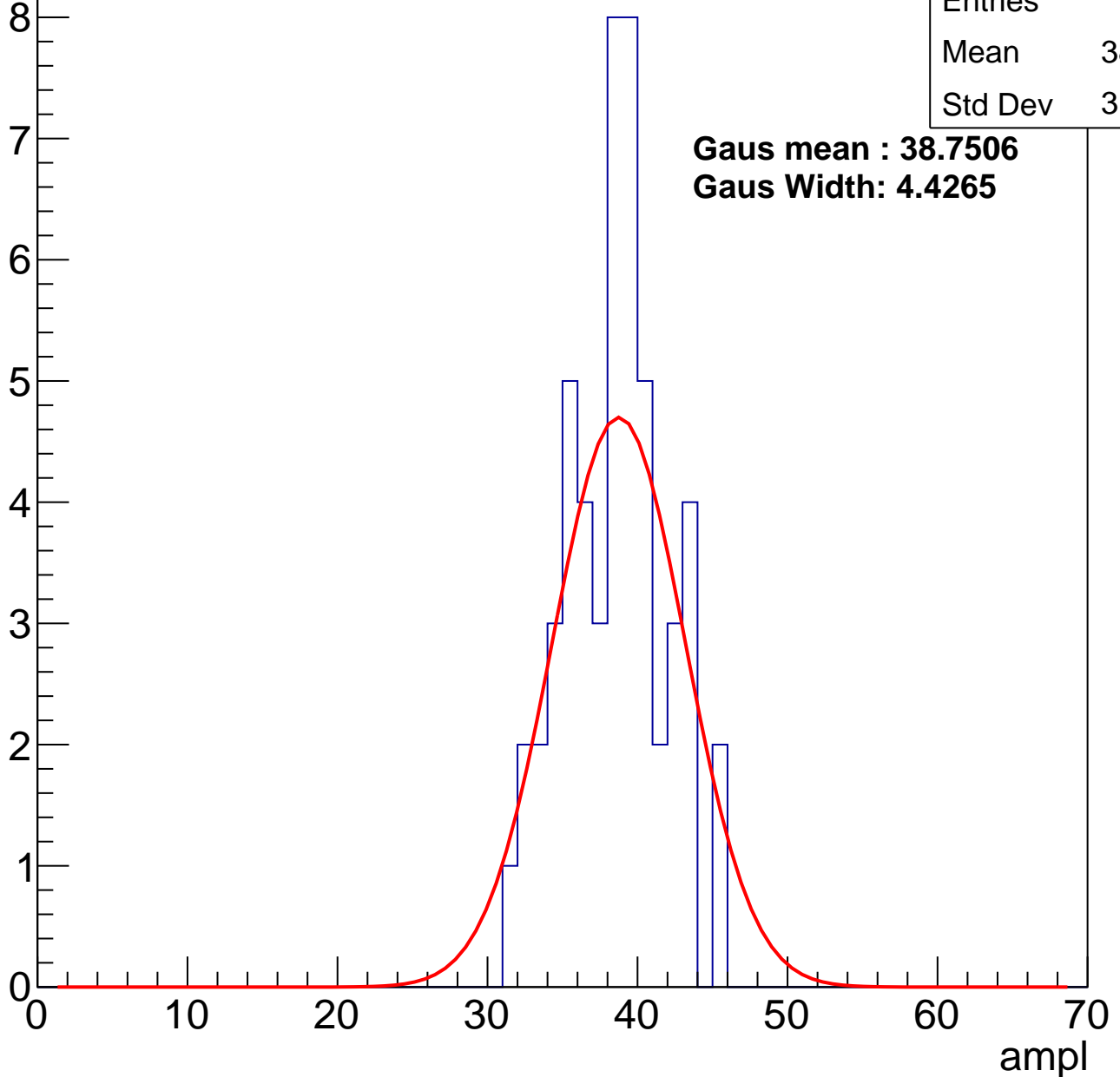
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	38.06
Std Dev	3.325

**Gaus mean : 38.7506**

**Gaus Width: 4.4265**



# B0L001S, U21-ch79, adc2

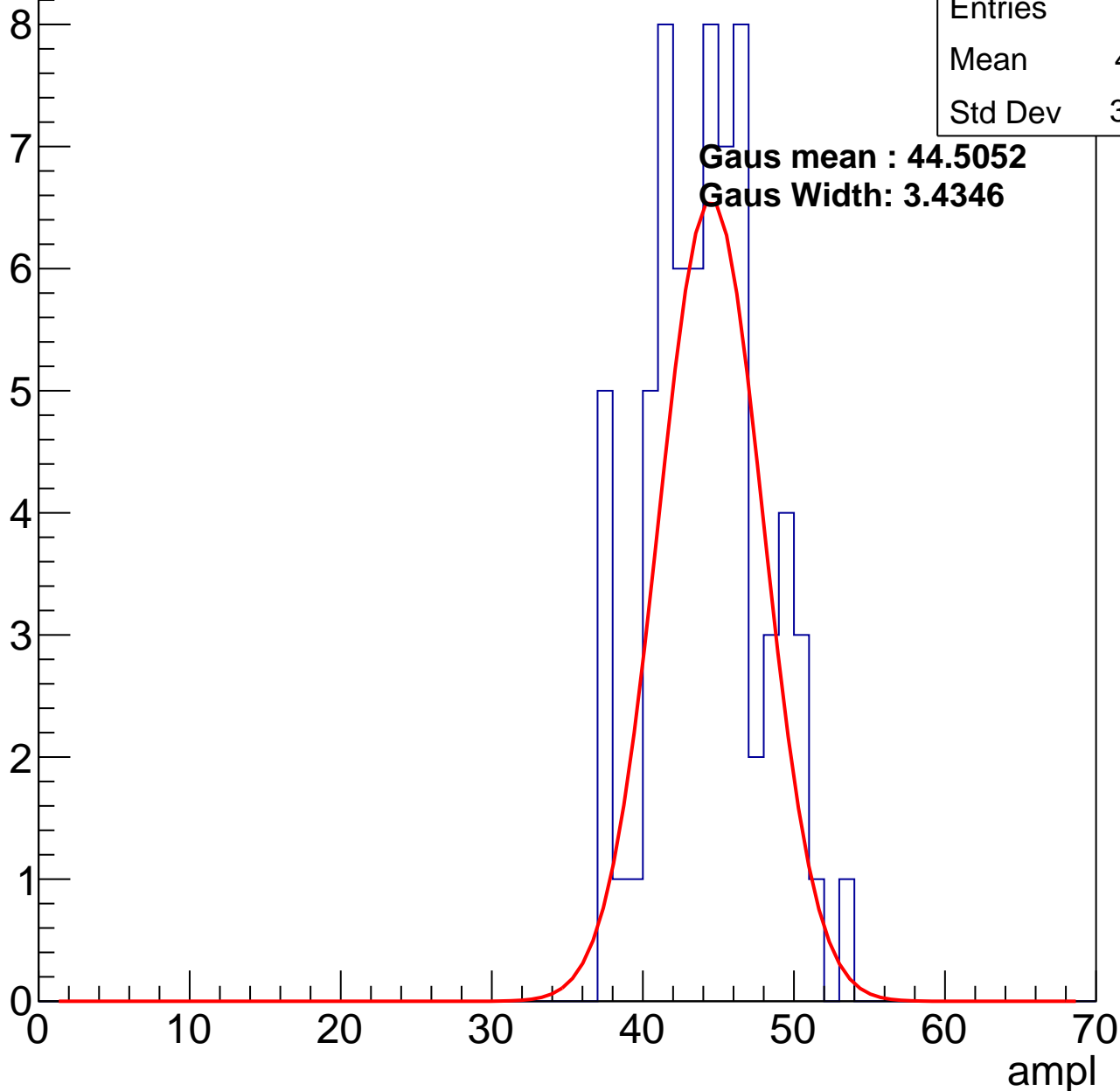
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	43.81
Std Dev	3.668

**Gaus mean : 44.5052**

**Gaus Width: 3.4346**

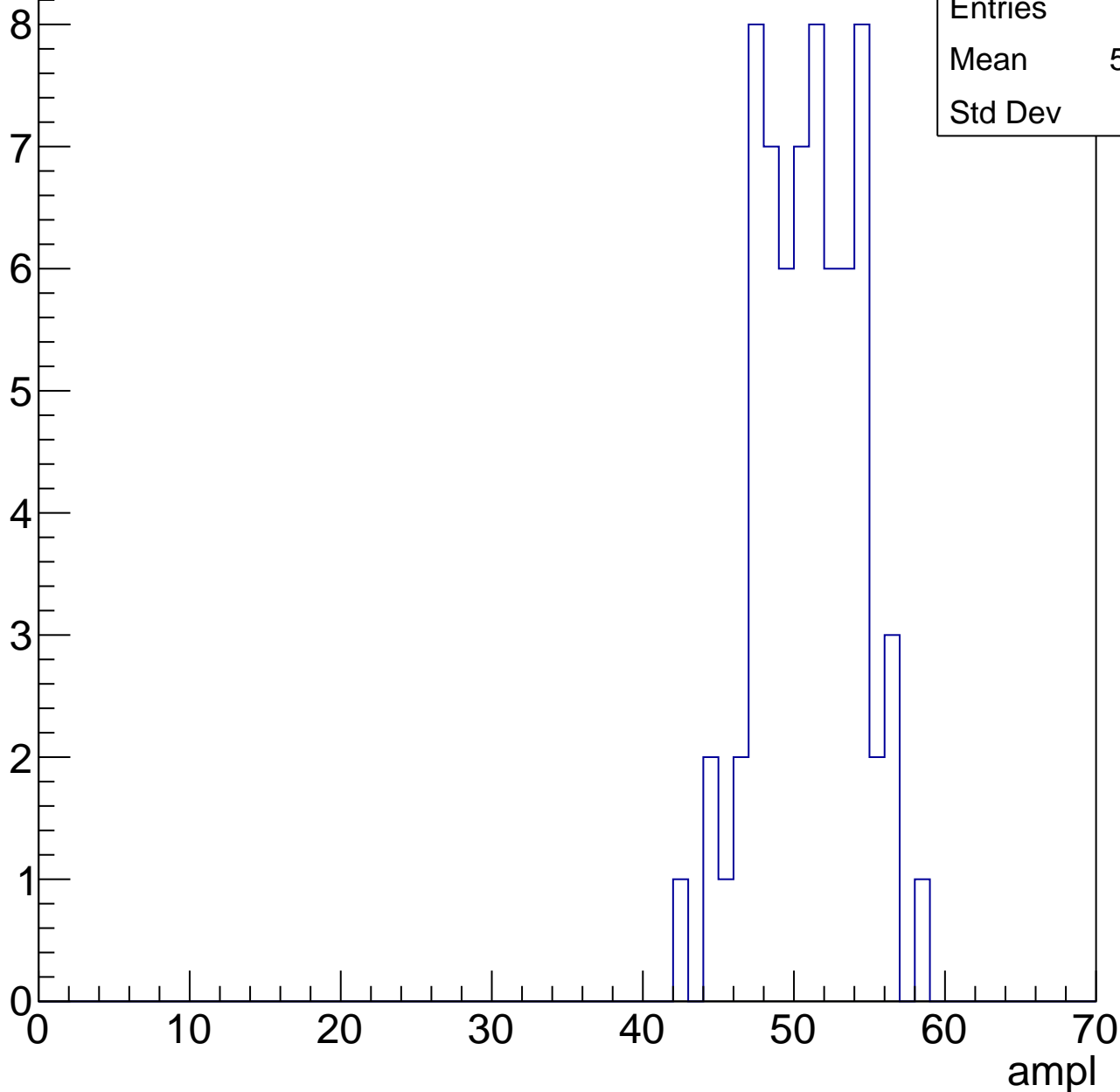


# B0L001S, U21-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

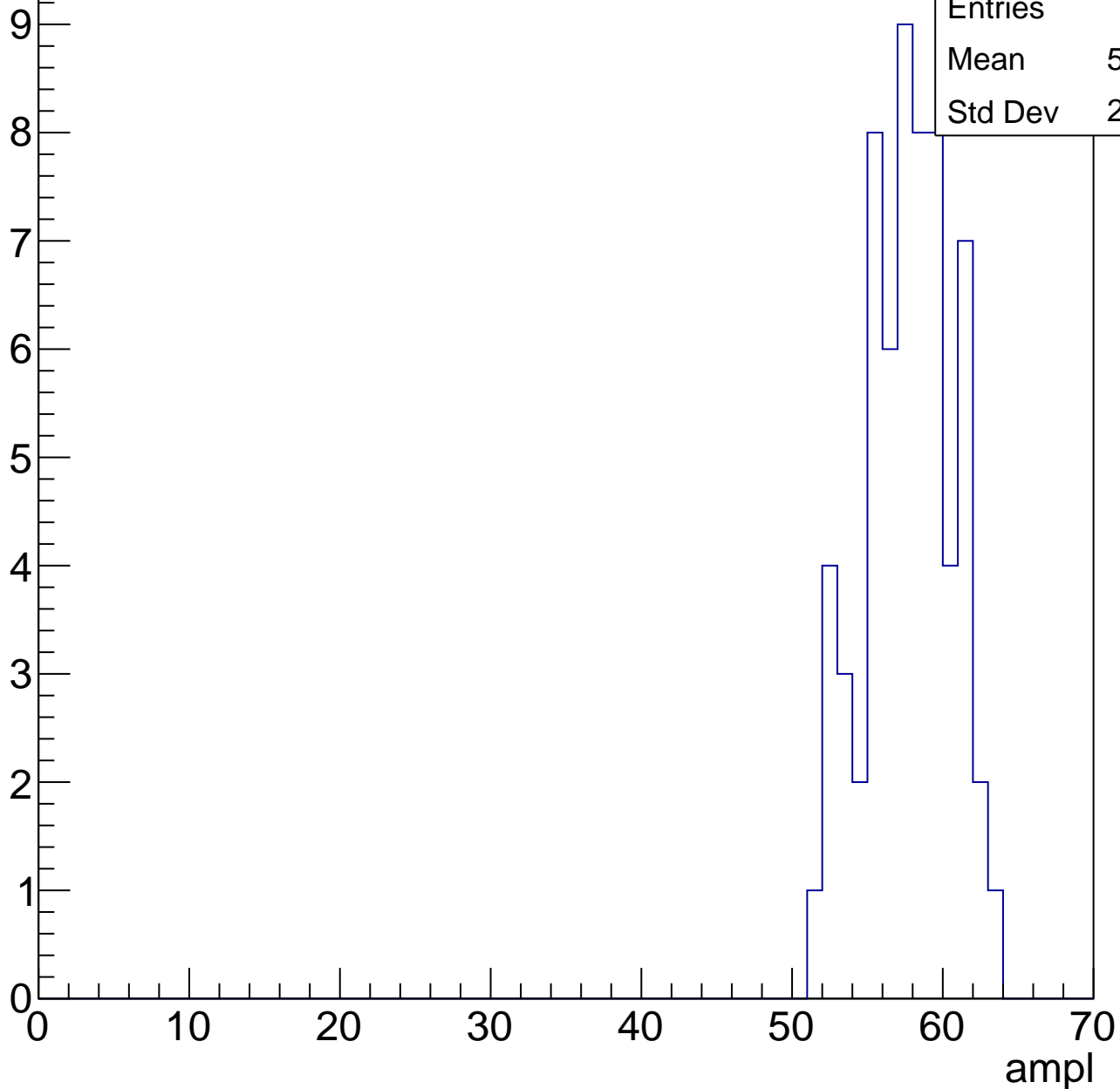
Entries	68
Mean	50.43
Std Dev	3.26



# B0L001S, U21-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



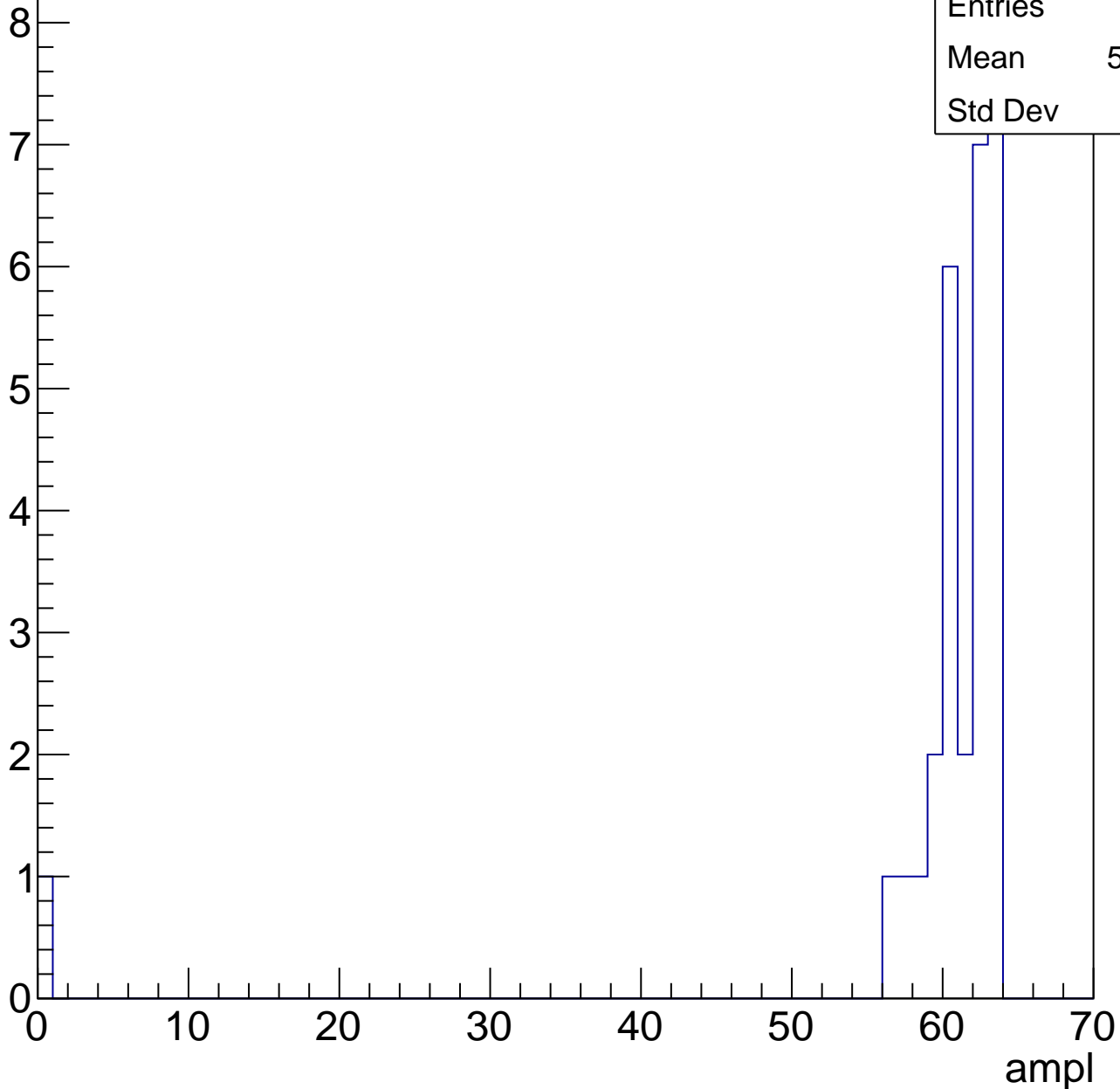
Entries	63
Mean	57.22
Std Dev	2.848

# B0L001S, U21-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	29
Mean	58.93
Std Dev	11.3



# B0L001S, U21-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch80, adc0

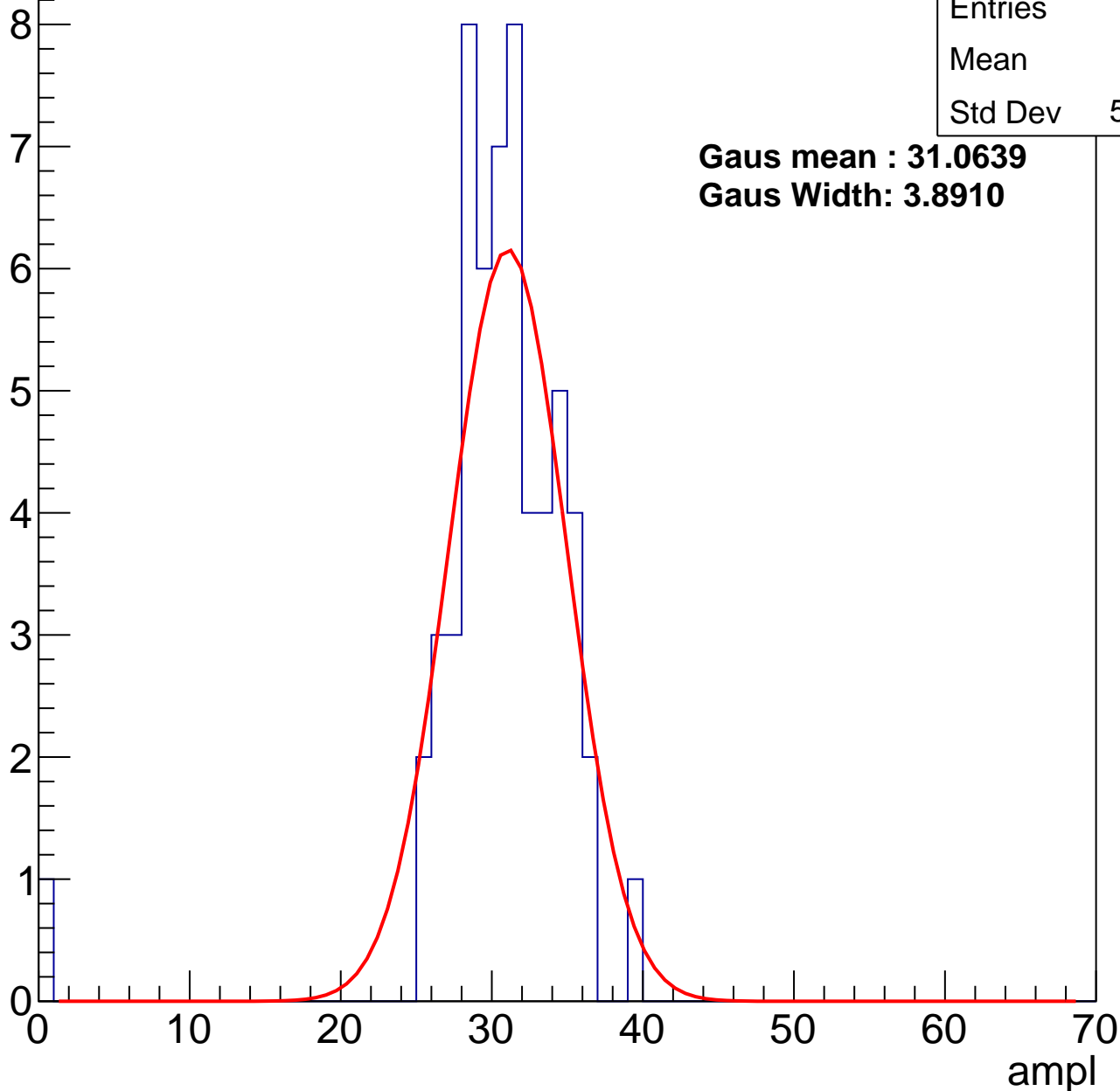
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	30.1
Std Dev	5.009

**Gaus mean : 31.0639**

**Gaus Width: 3.8910**



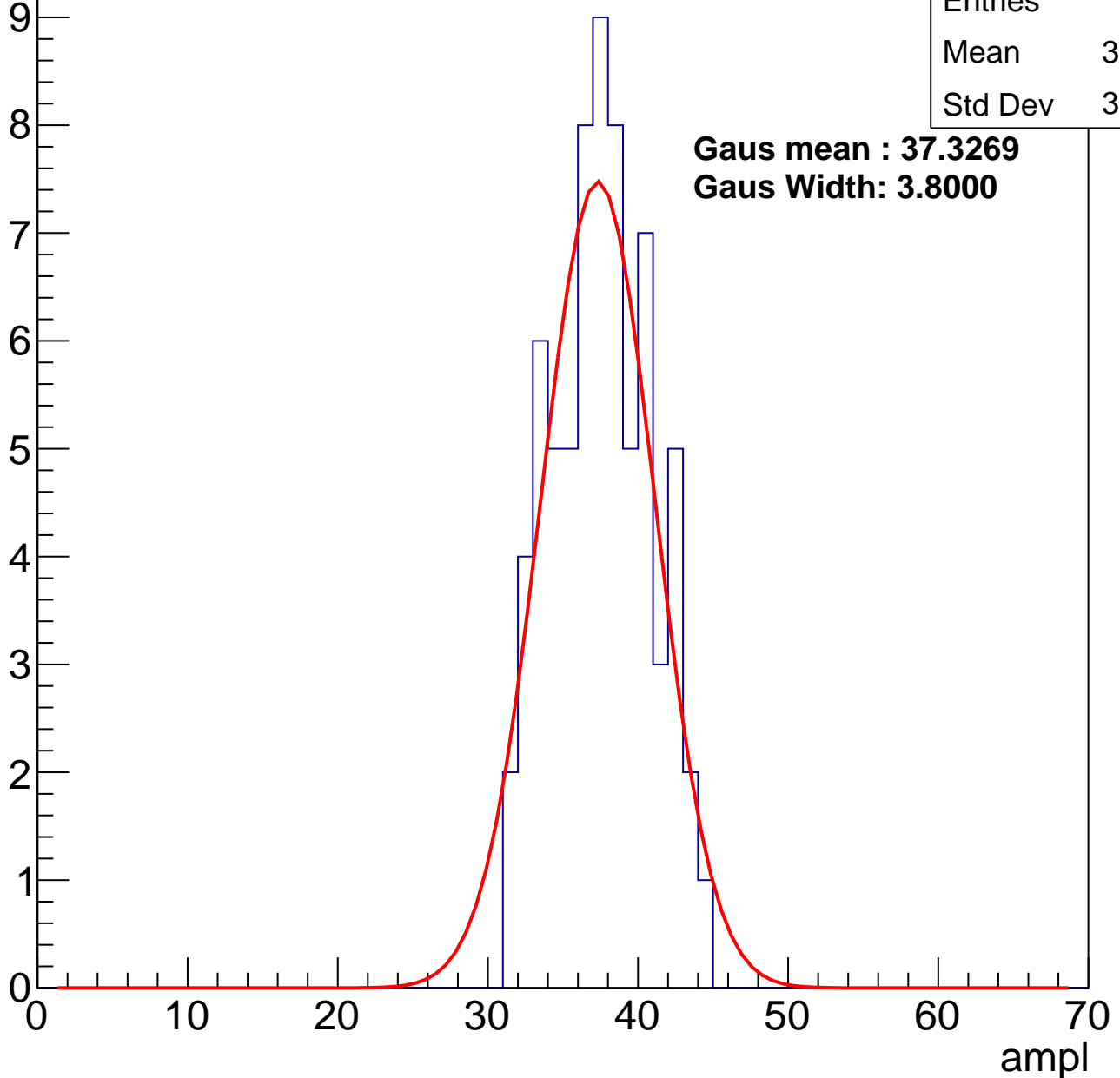
# B0L001S, U21-ch80, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	37.09
Std Dev	3.219

**Gaus mean : 37.3269**  
**Gaus Width: 3.8000**



# B0L001S, U21-ch80, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	44.45
Std Dev	3.503

**Gaus mean : 44.8746**

**Gaus Width: 3.7749**

10

8

6

4

2

0

0

2

4

6

8

ampl

0

10

20

30

40

50

60

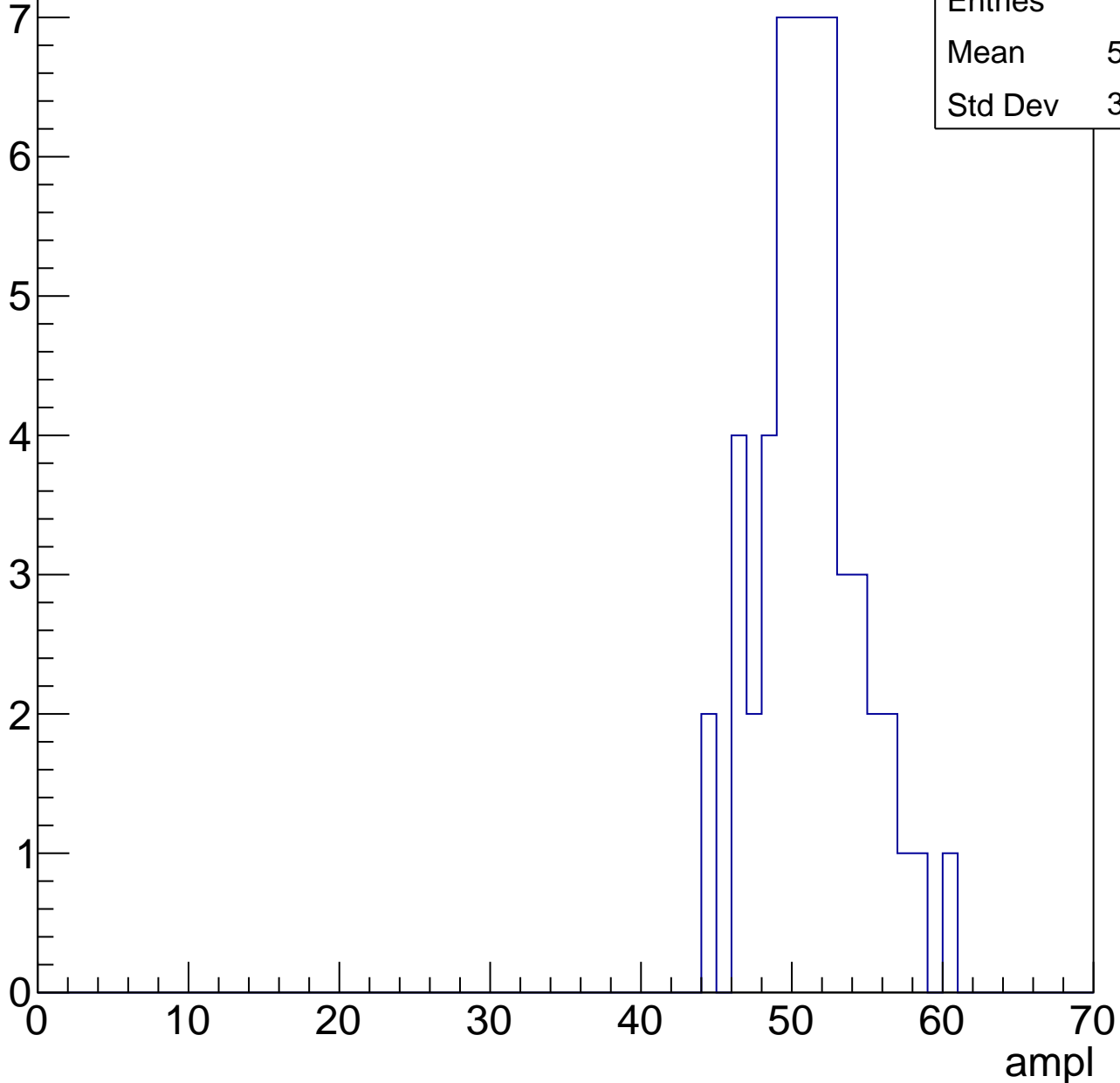
70

# B0L001S, U21-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	50.75
Std Dev	3.342

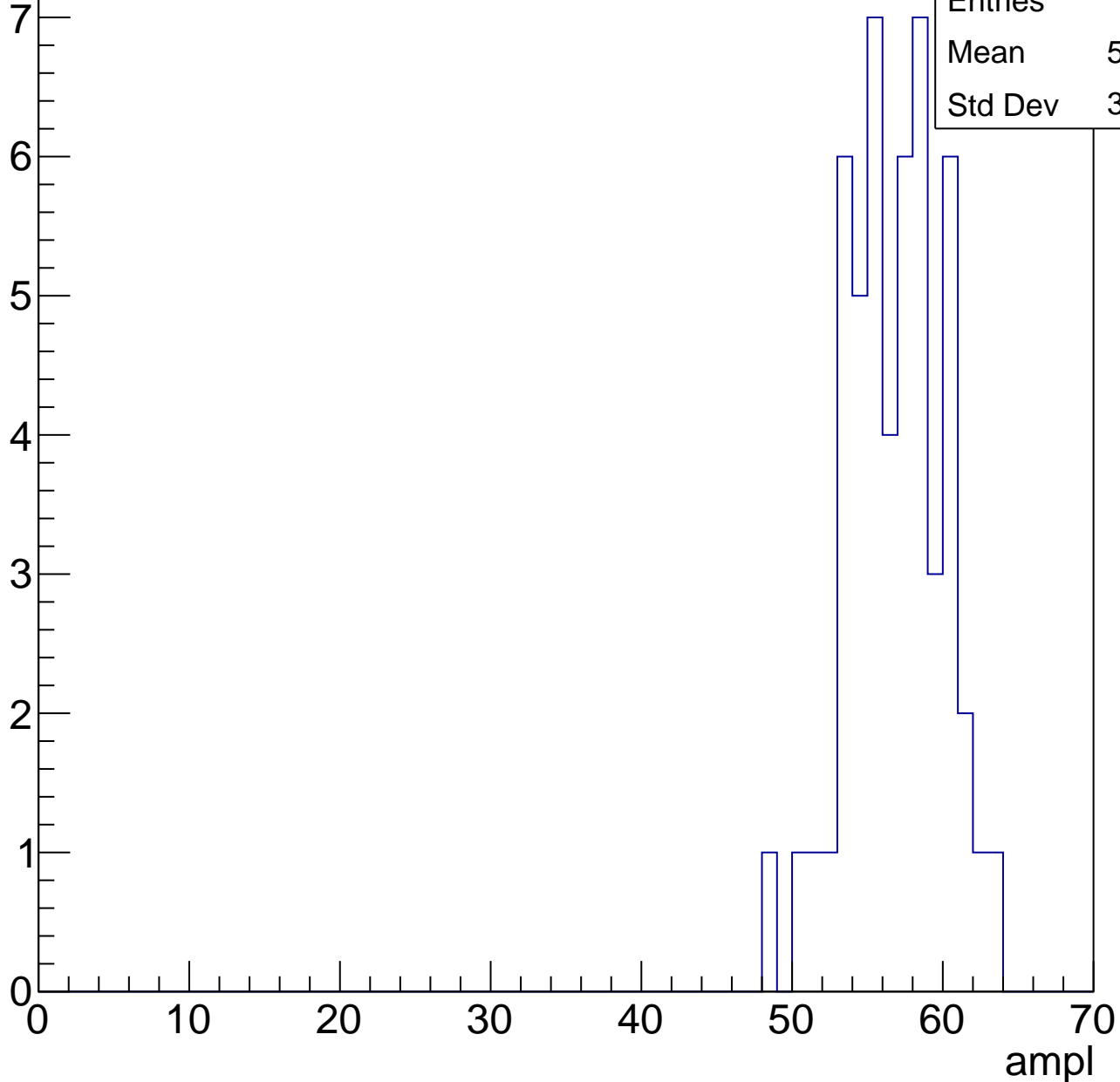


# B0L001S, U21-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	56.35
Std Dev	3.125

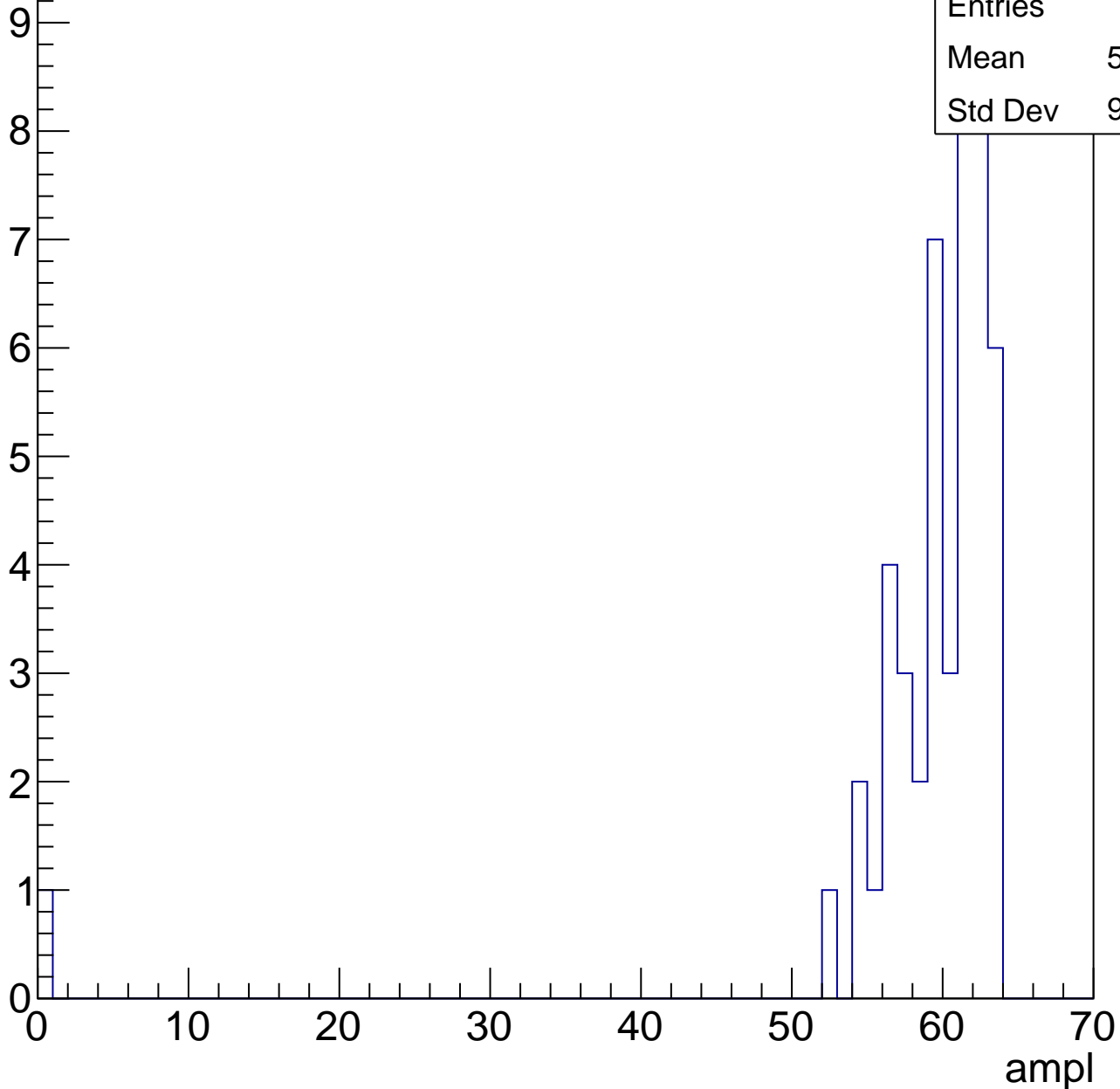


# B0L001S, U21-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	58.36
Std Dev	9.038



# B0L001S, U21-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U21-ch81, adc0

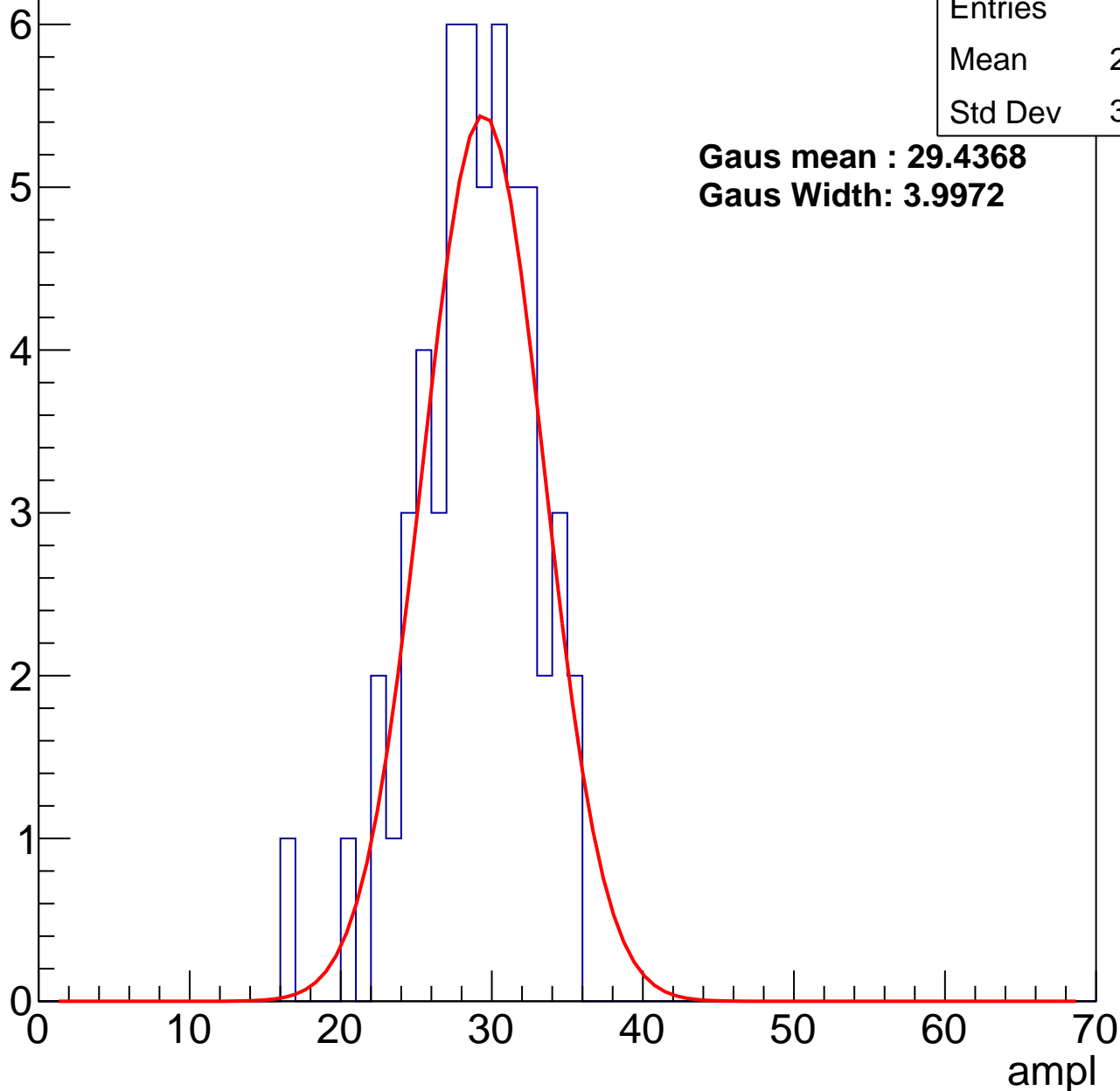
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	28.38
Std Dev	3.835

**Gaus mean : 29.4368**

**Gaus Width: 3.9972**



# B0L001S, U21-ch81, adc1

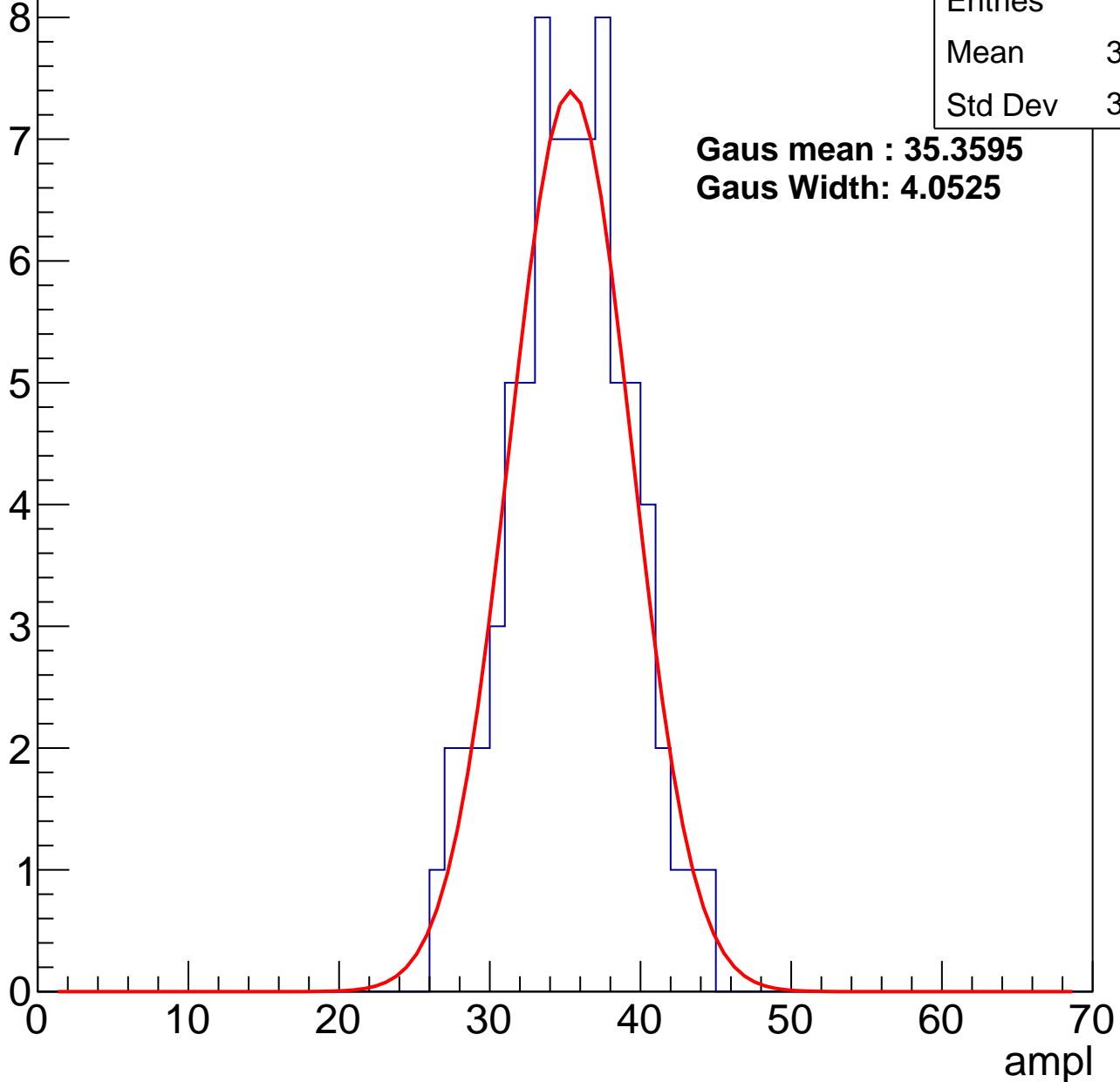
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	34.87
Std Dev	3.884

**Gaus mean : 35.3595**

**Gaus Width: 4.0525**



# B0L001S, U21-ch81, adc2

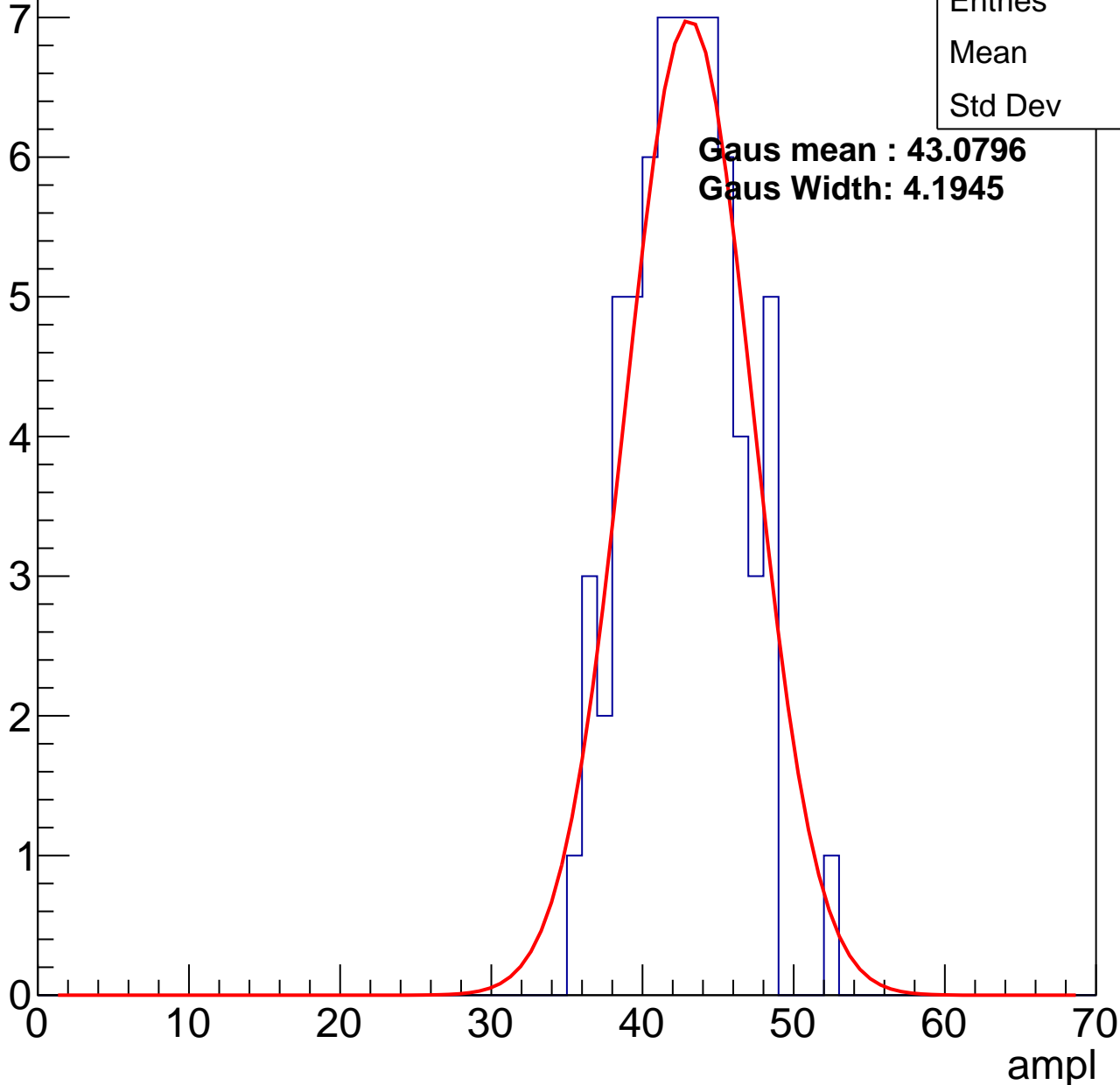
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	42.3
Std Dev	3.54

**Gaus mean : 43.0796**

**Gaus Width: 4.1945**

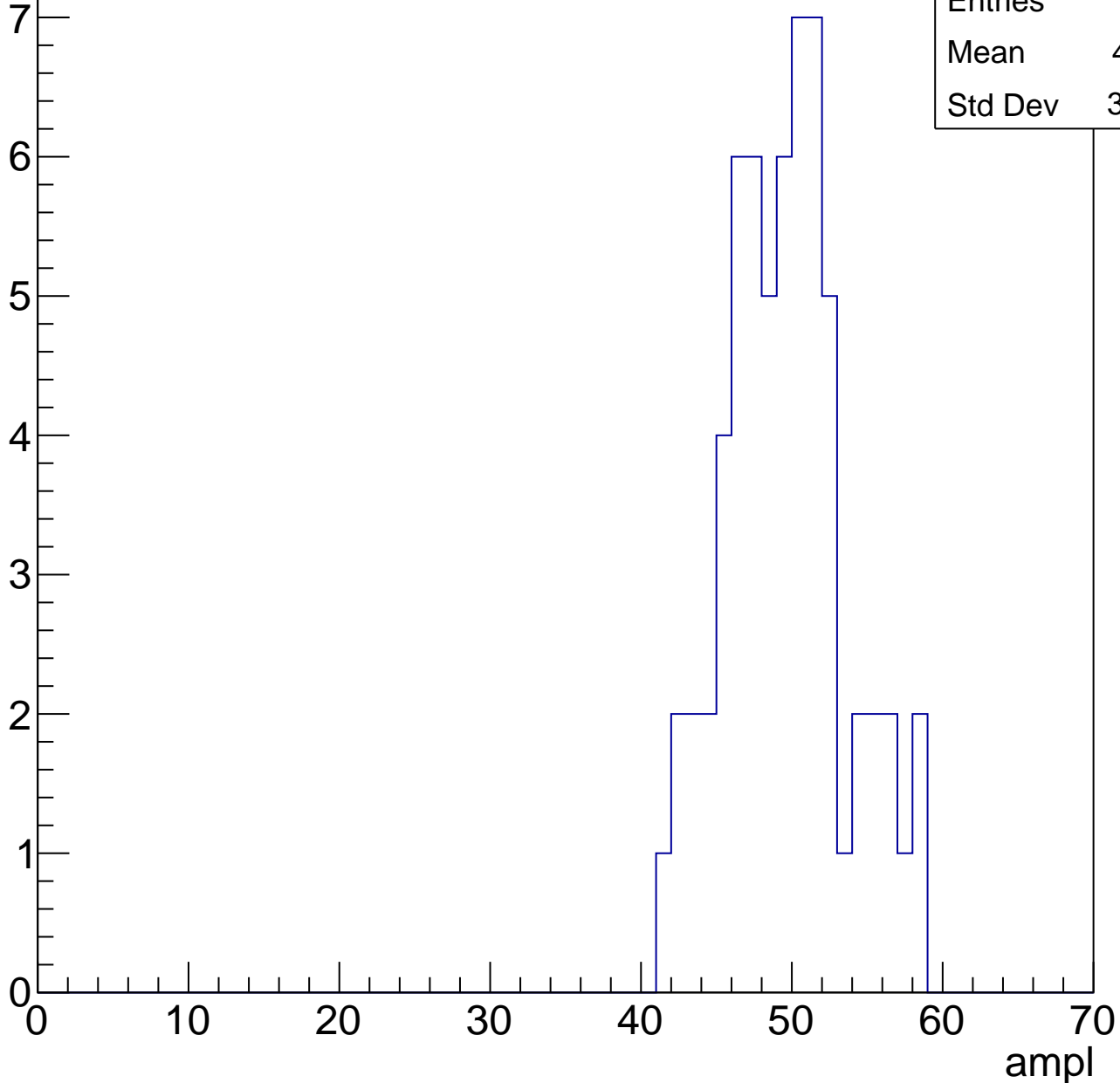


# B0L001S, U21-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	49.11
Std Dev	3.928

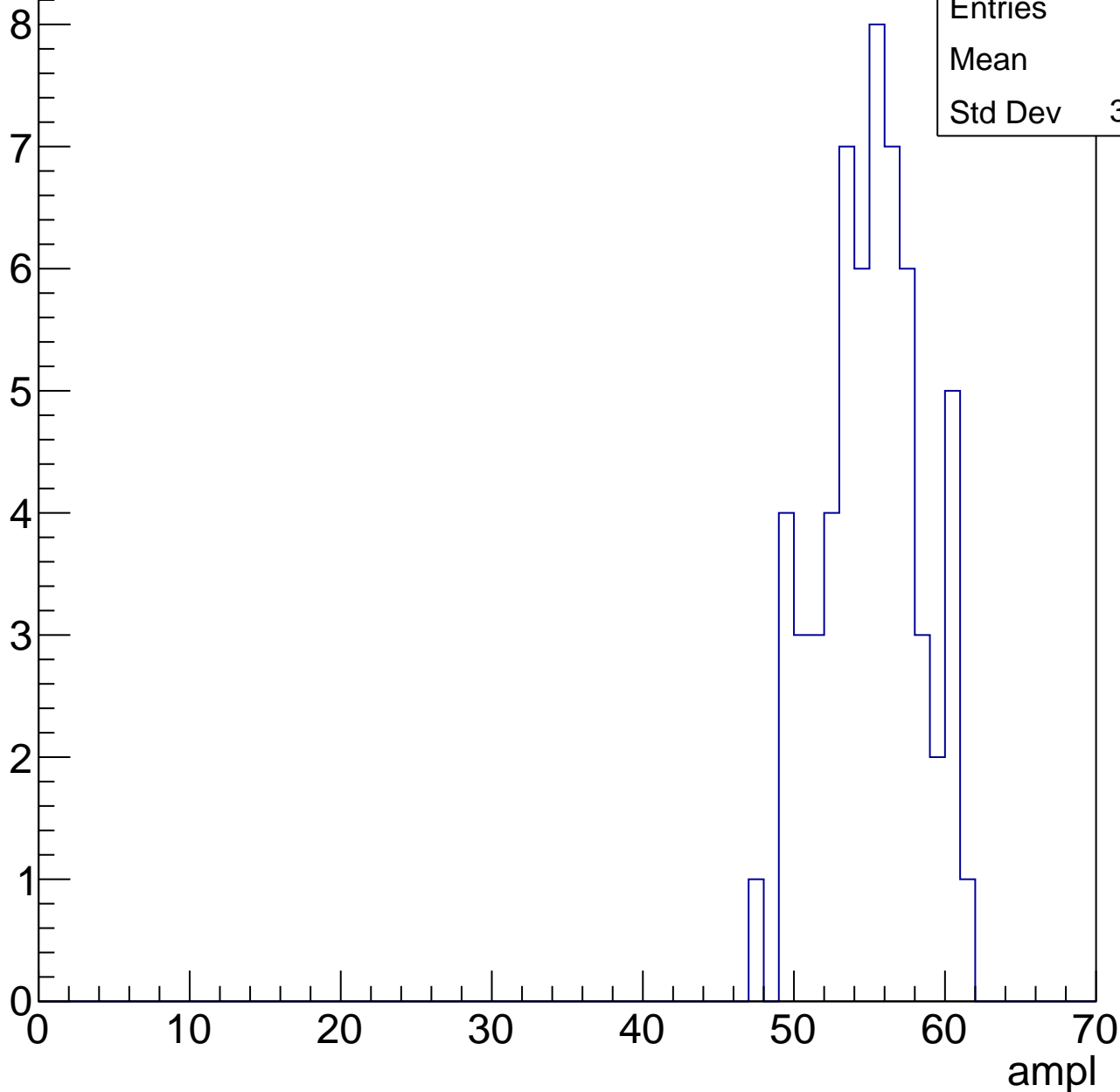


# B0L001S, U21-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

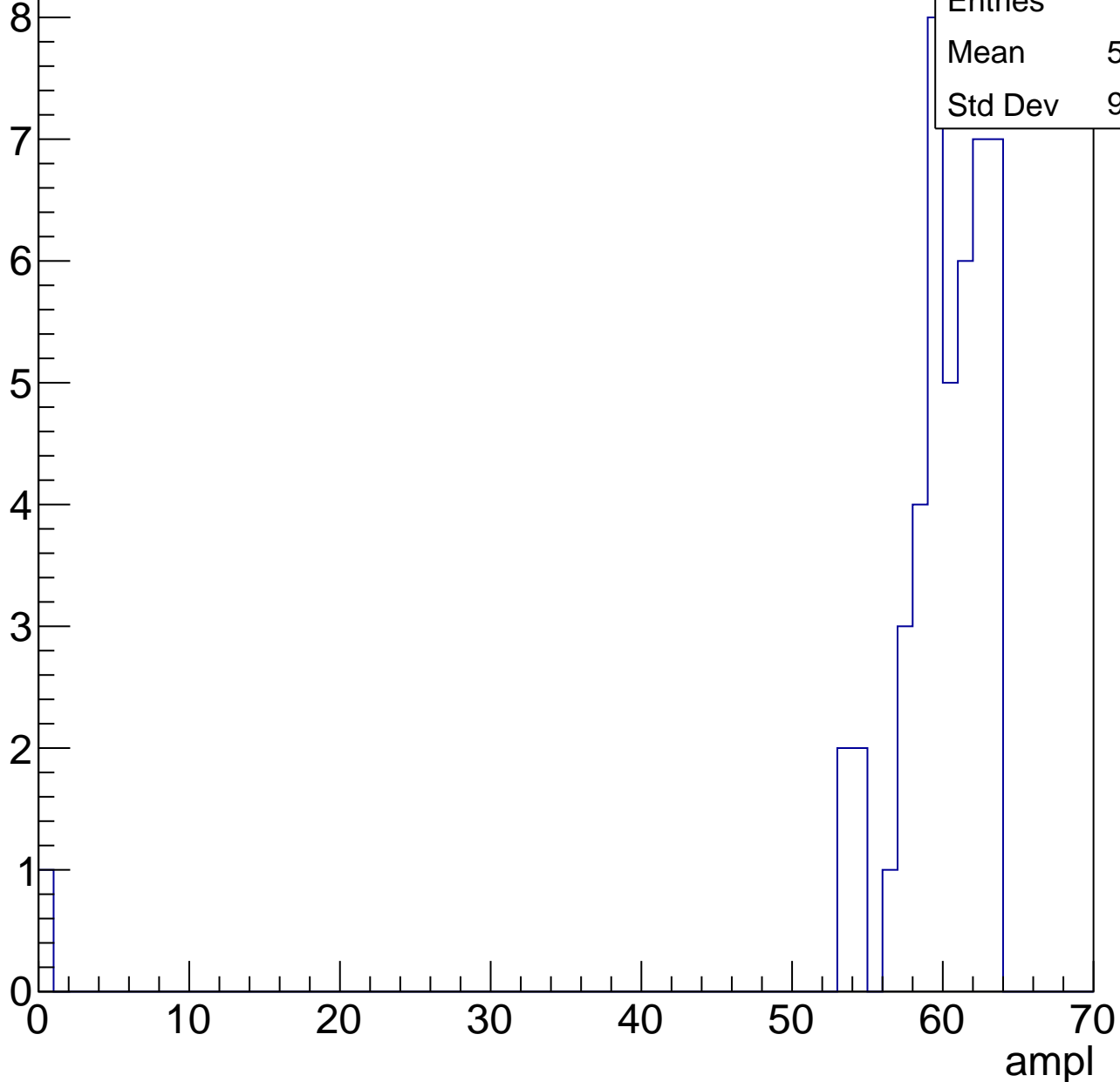
Entries	60
Mean	54.6
Std Dev	3.272



# B0L001S, U21-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

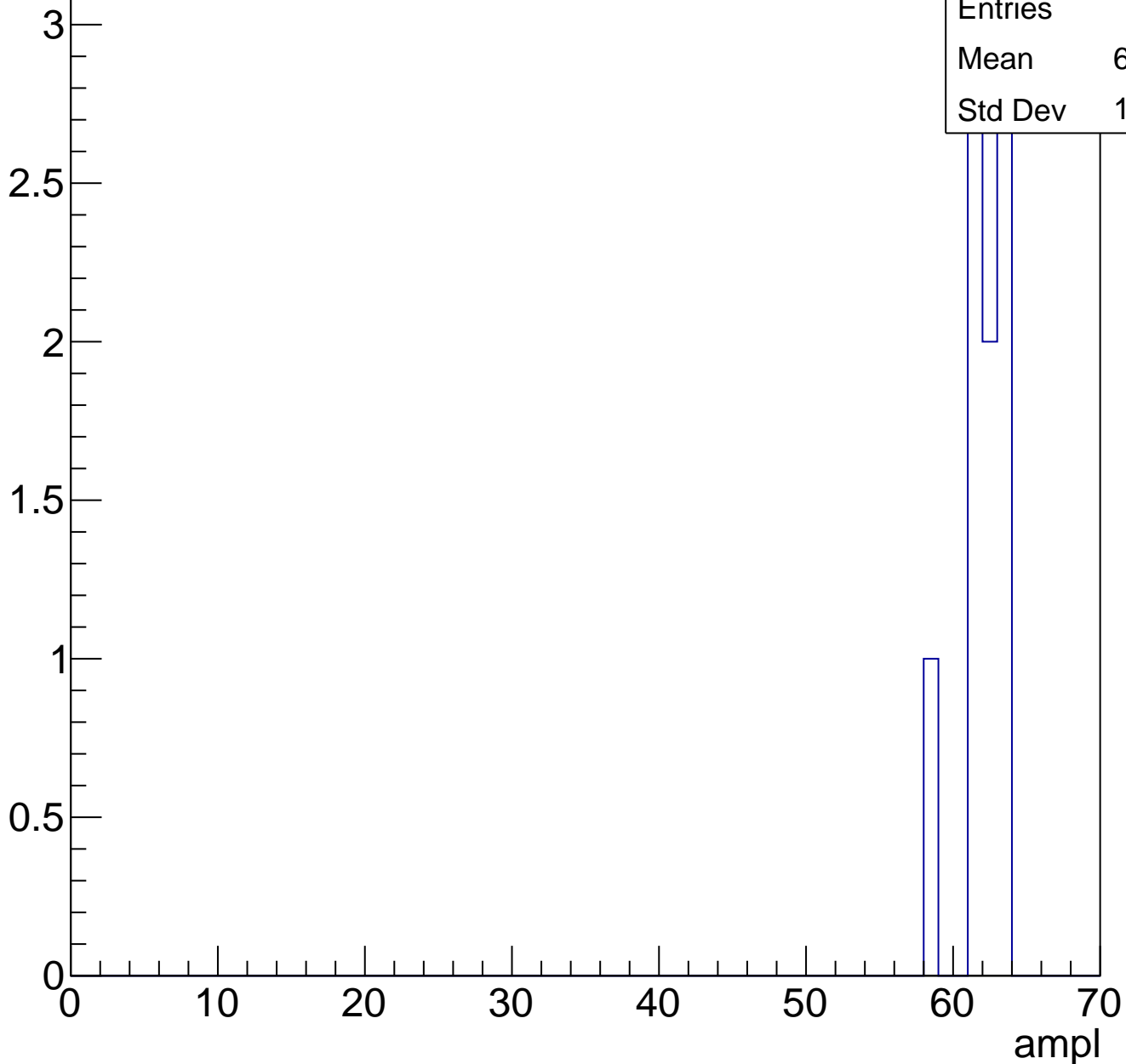
Entry



# B0L001S, U21-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	20.67
Std Dev	29.23

# B0L001S, U21-ch82, adc0

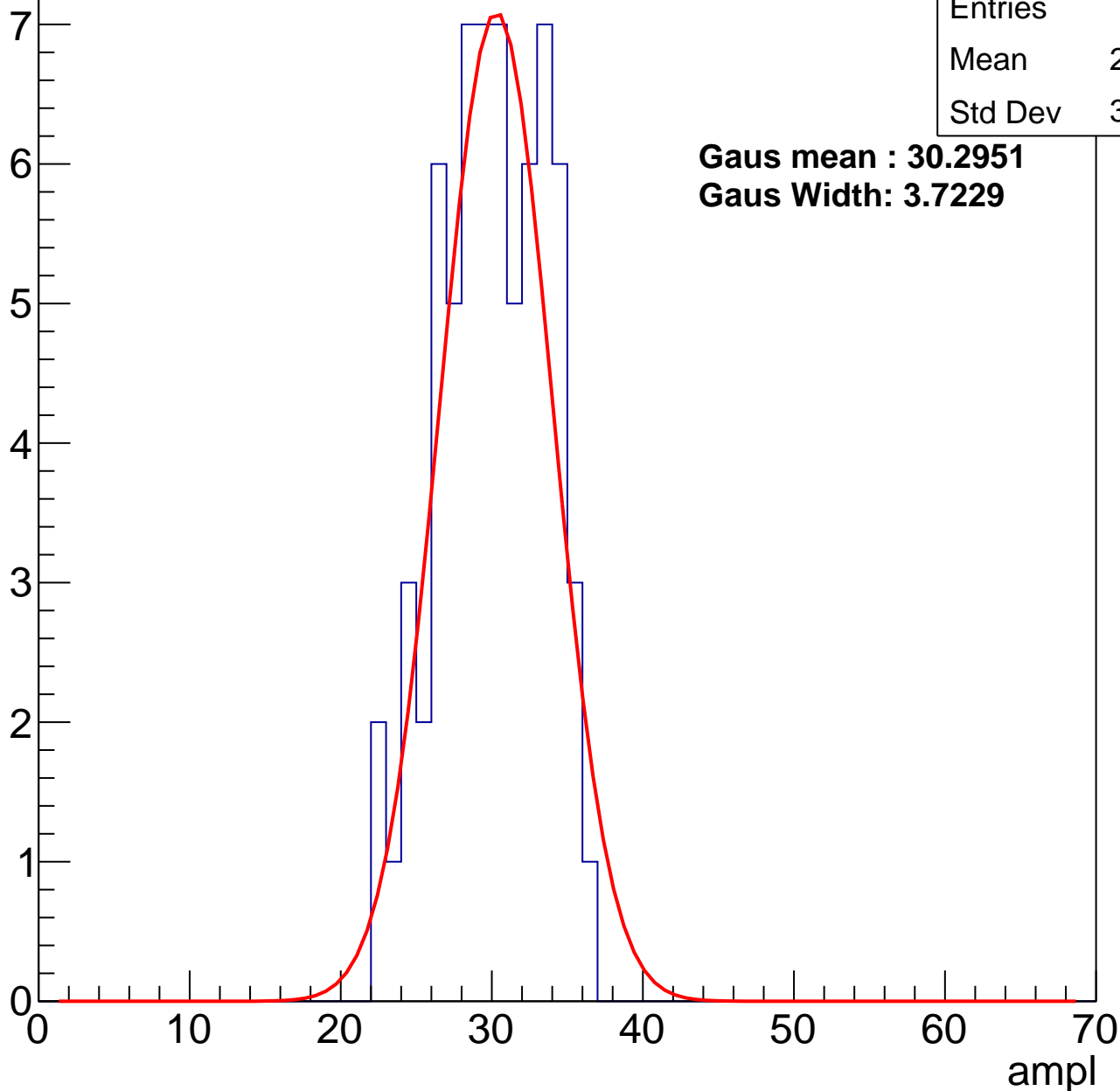
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	29.59
Std Dev	3.427

**Gaus mean : 30.2951**

**Gaus Width: 3.7229**



# B0L001S, U21-ch82, adc1

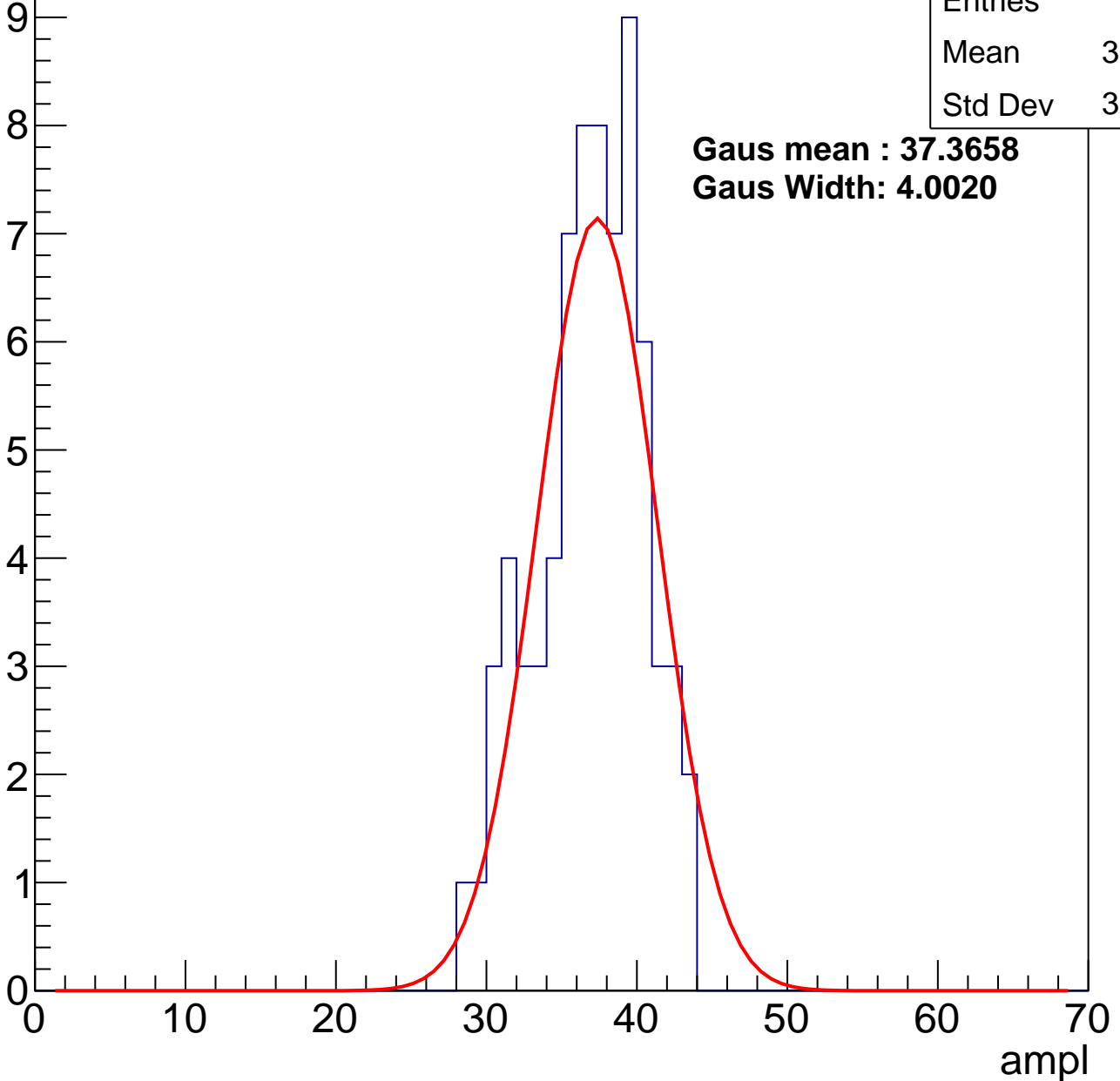
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	36.43
Std Dev	3.535

**Gaus mean : 37.3658**

**Gaus Width: 4.0020**



# B0L001S, U21-ch82, adc2

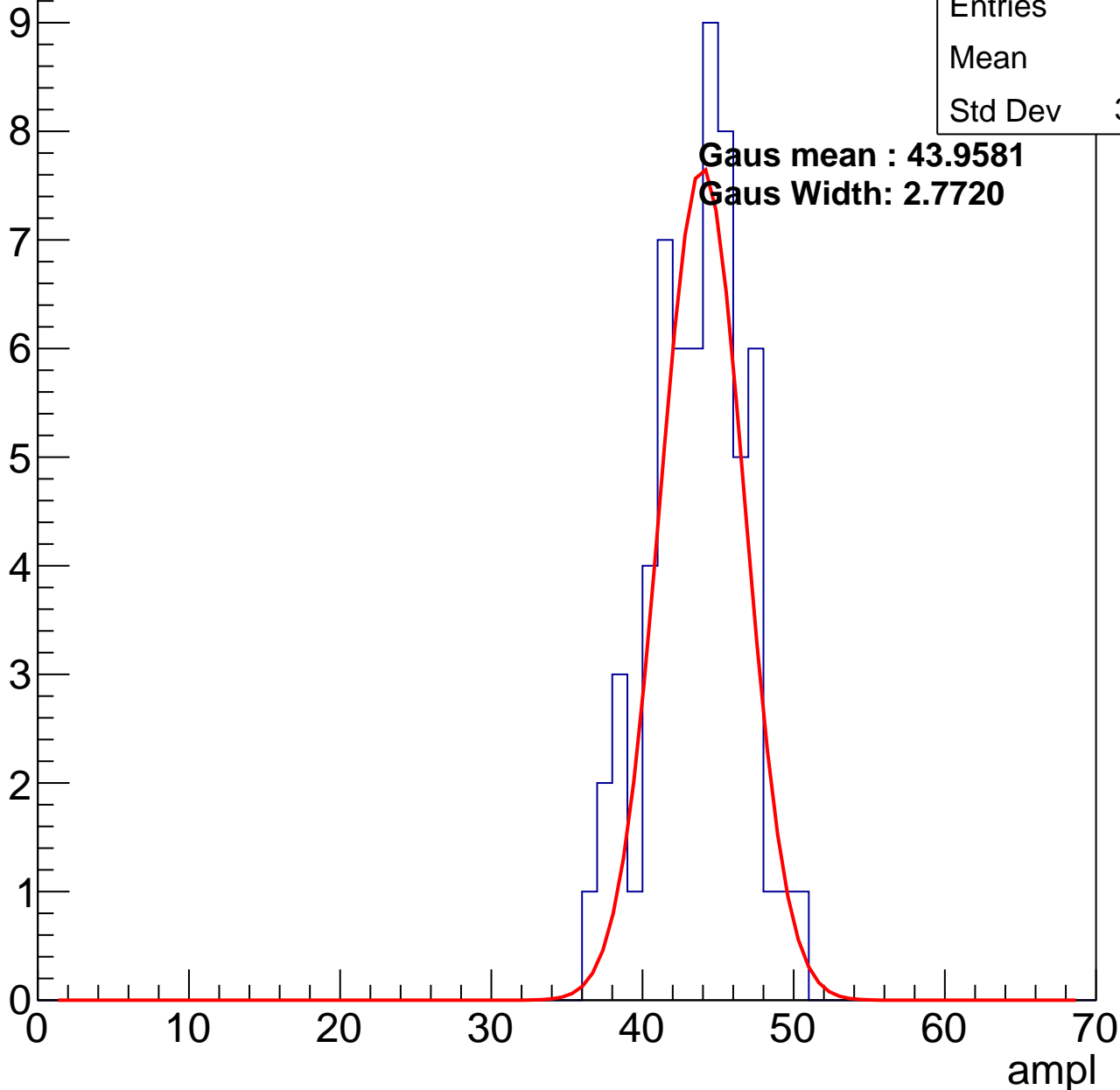
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	43.2
Std Dev	3.061

**Gaus mean : 43.9581**

**Gaus Width: 2.7720**

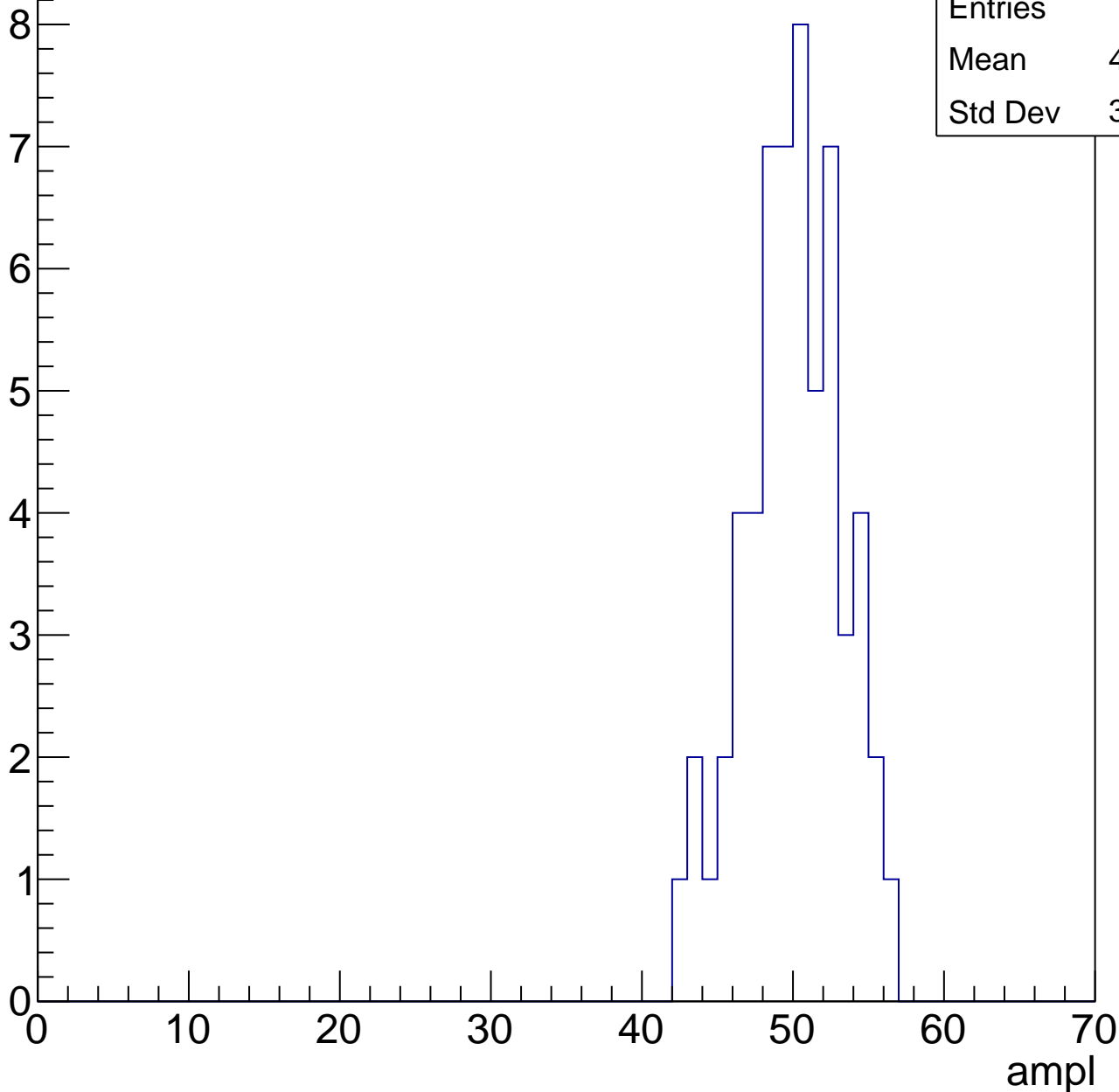


# B0L001S, U21-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	49.53
Std Dev	3.163

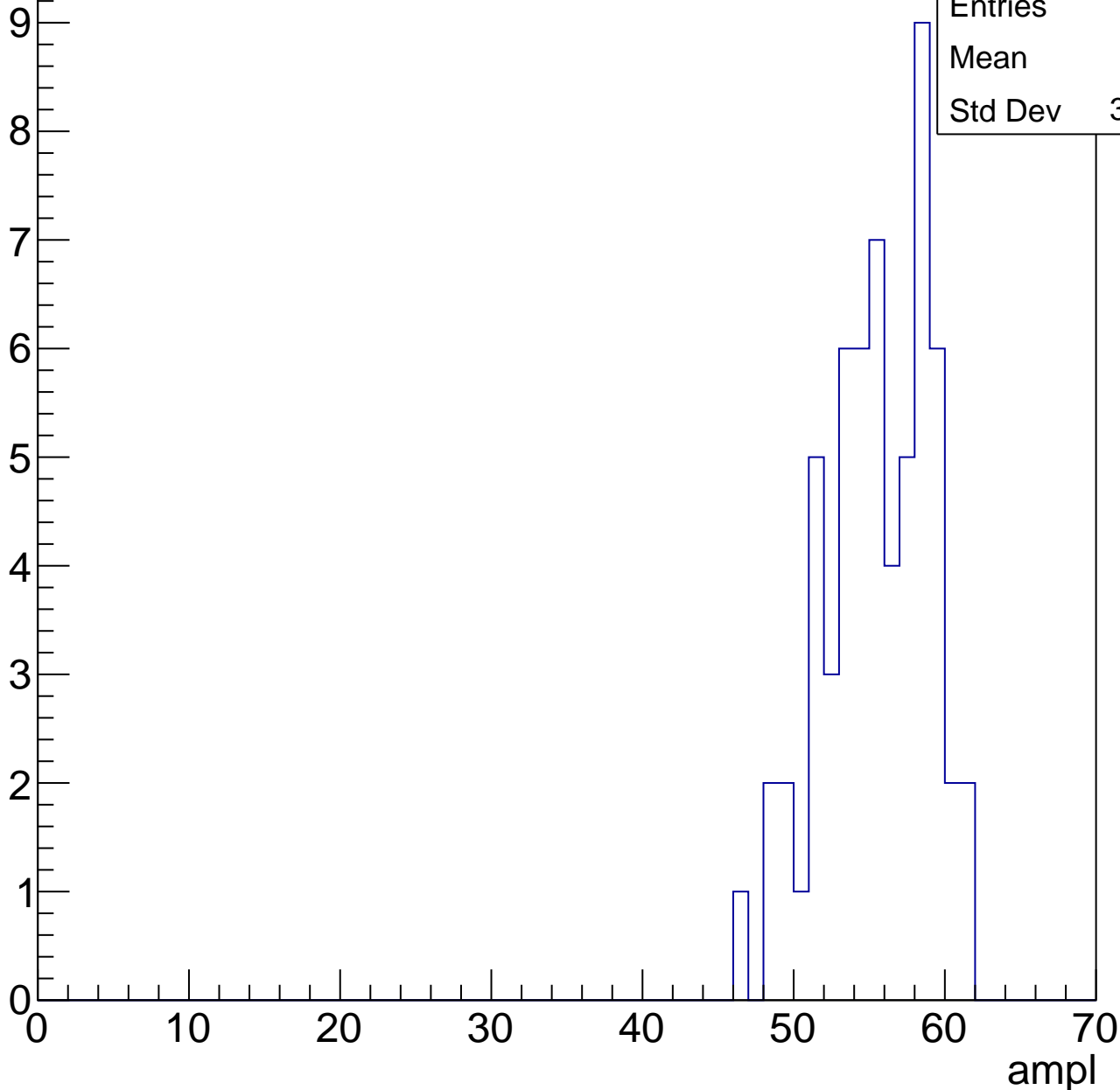


# B0L001S, U21-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	55
Std Dev	3.474

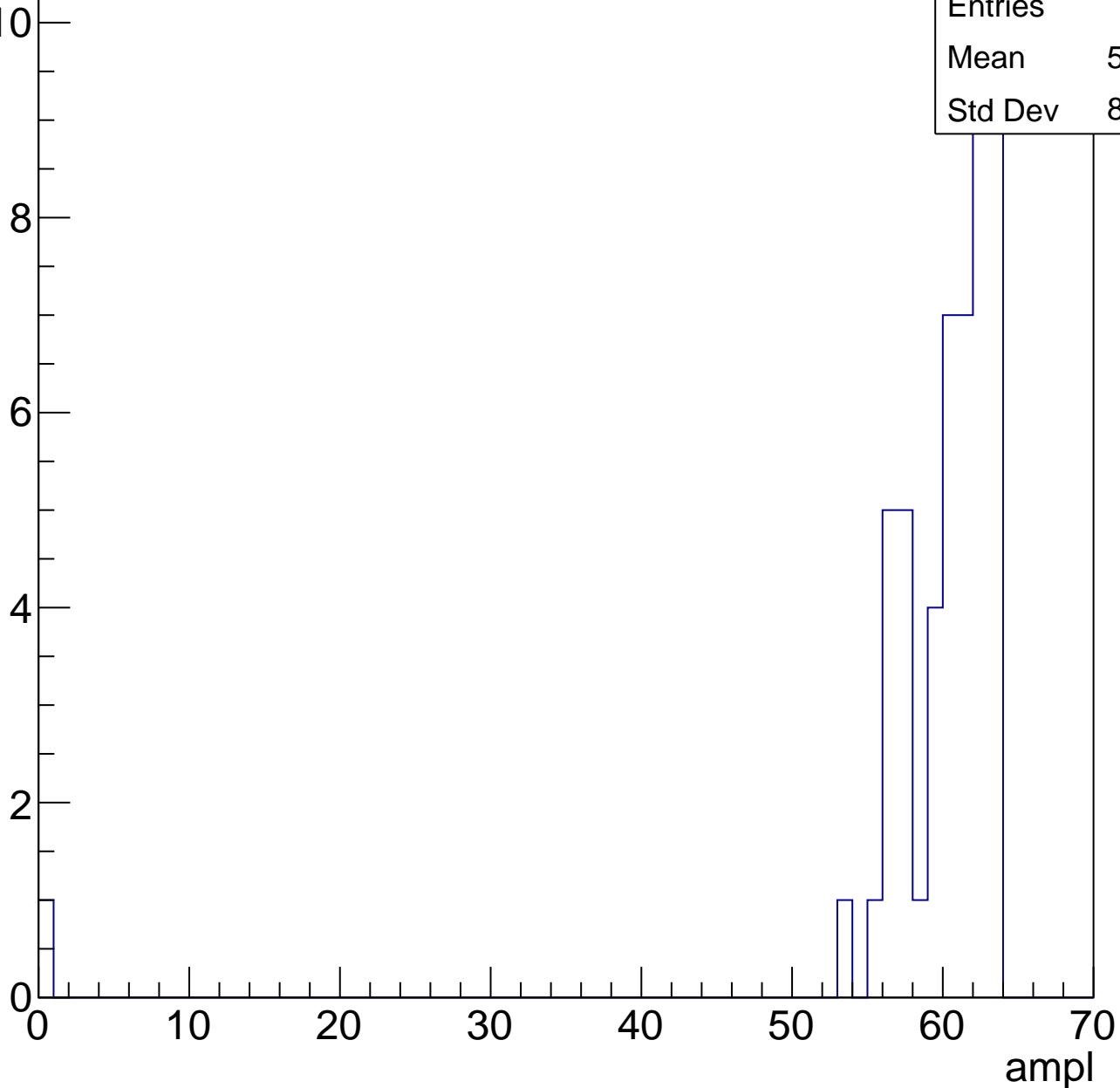


# B0L001S, U21-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

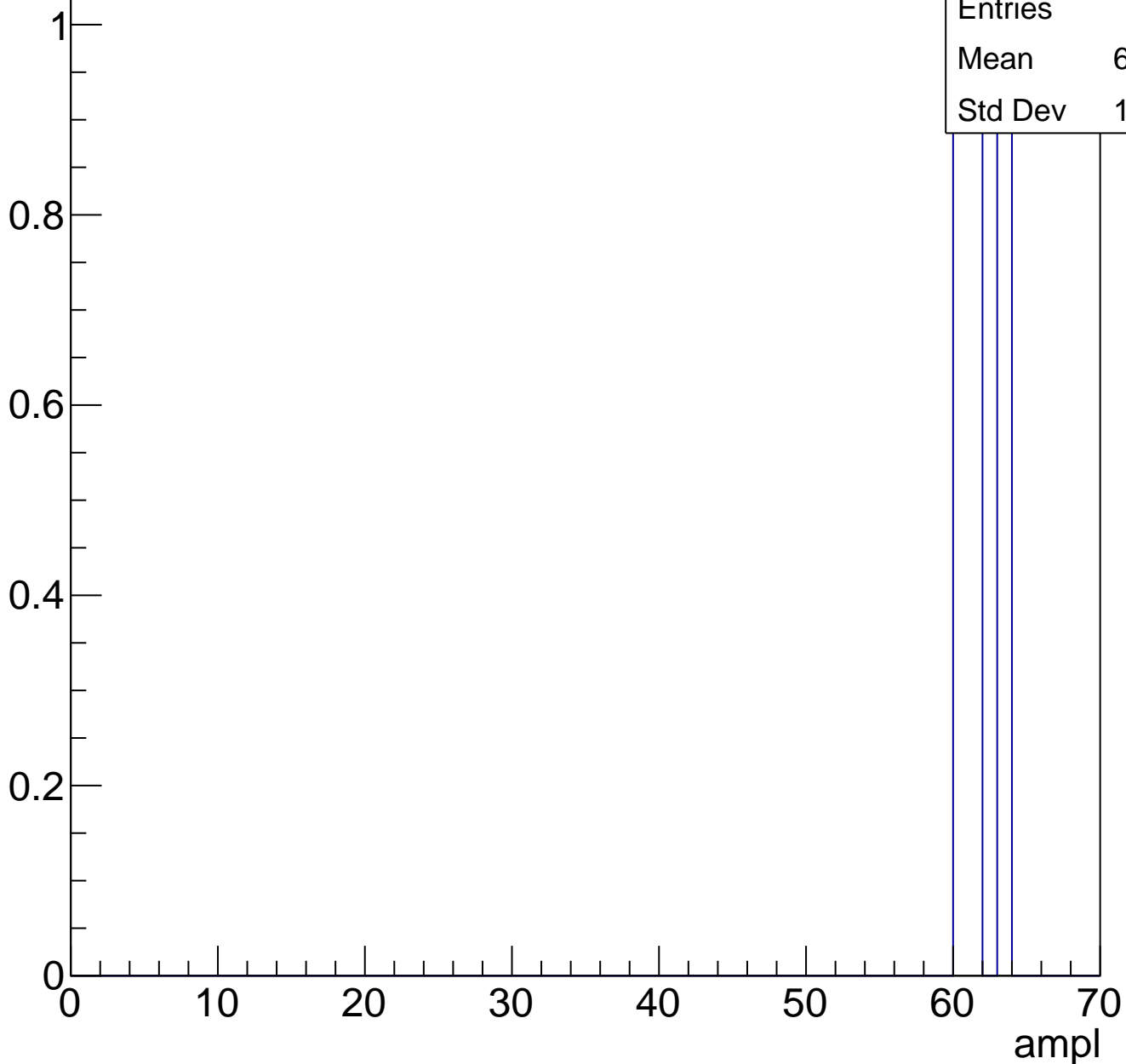
Entries	51
Mean	58.84
Std Dev	8.707



# B0L001S, U21-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U21-ch83, adc0

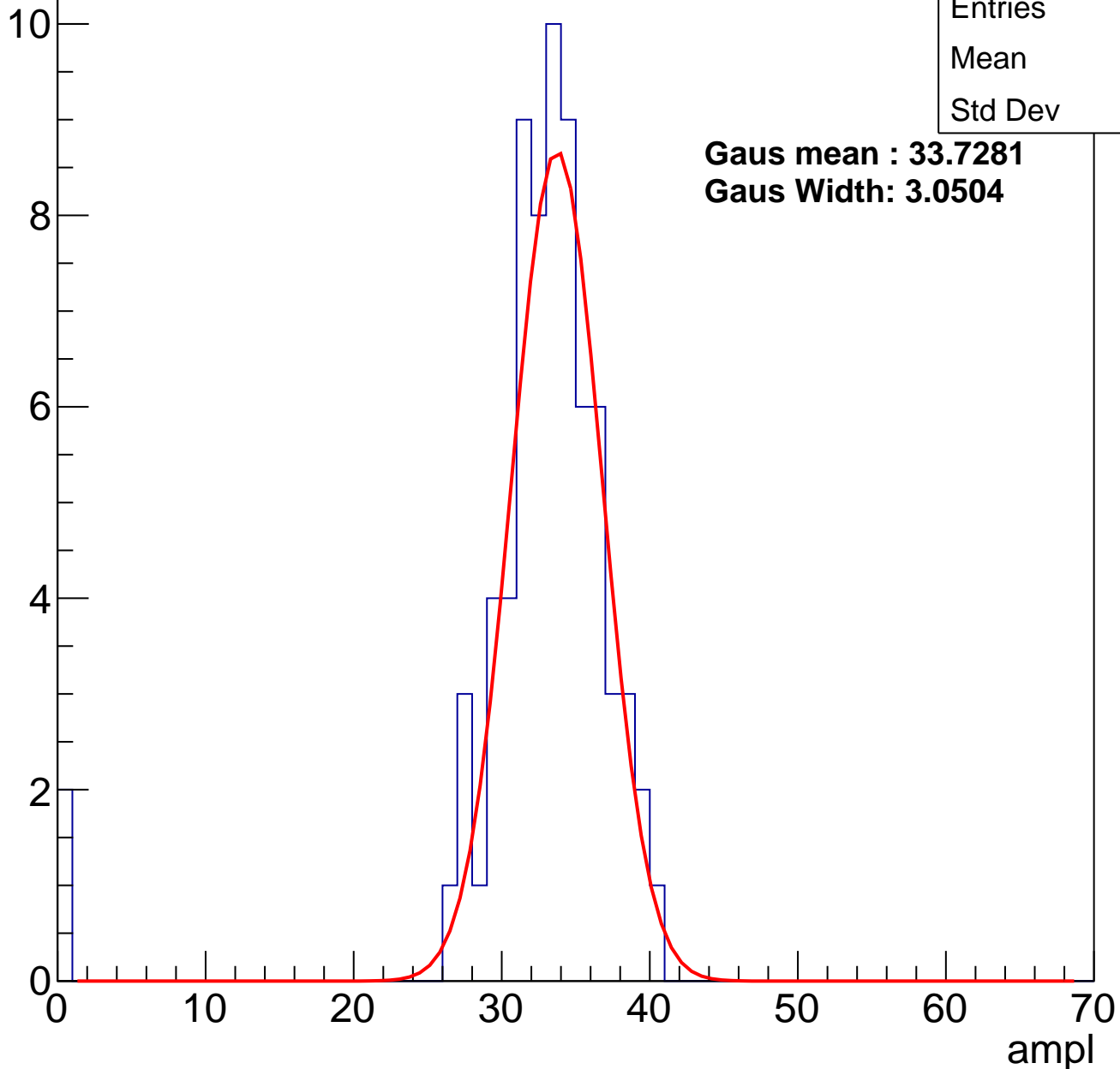
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	72
Mean	32.1
Std Dev	6.21

**Gaus mean : 33.7281**

**Gaus Width: 3.0504**

Entry



# B0L001S, U21-ch83, adc1

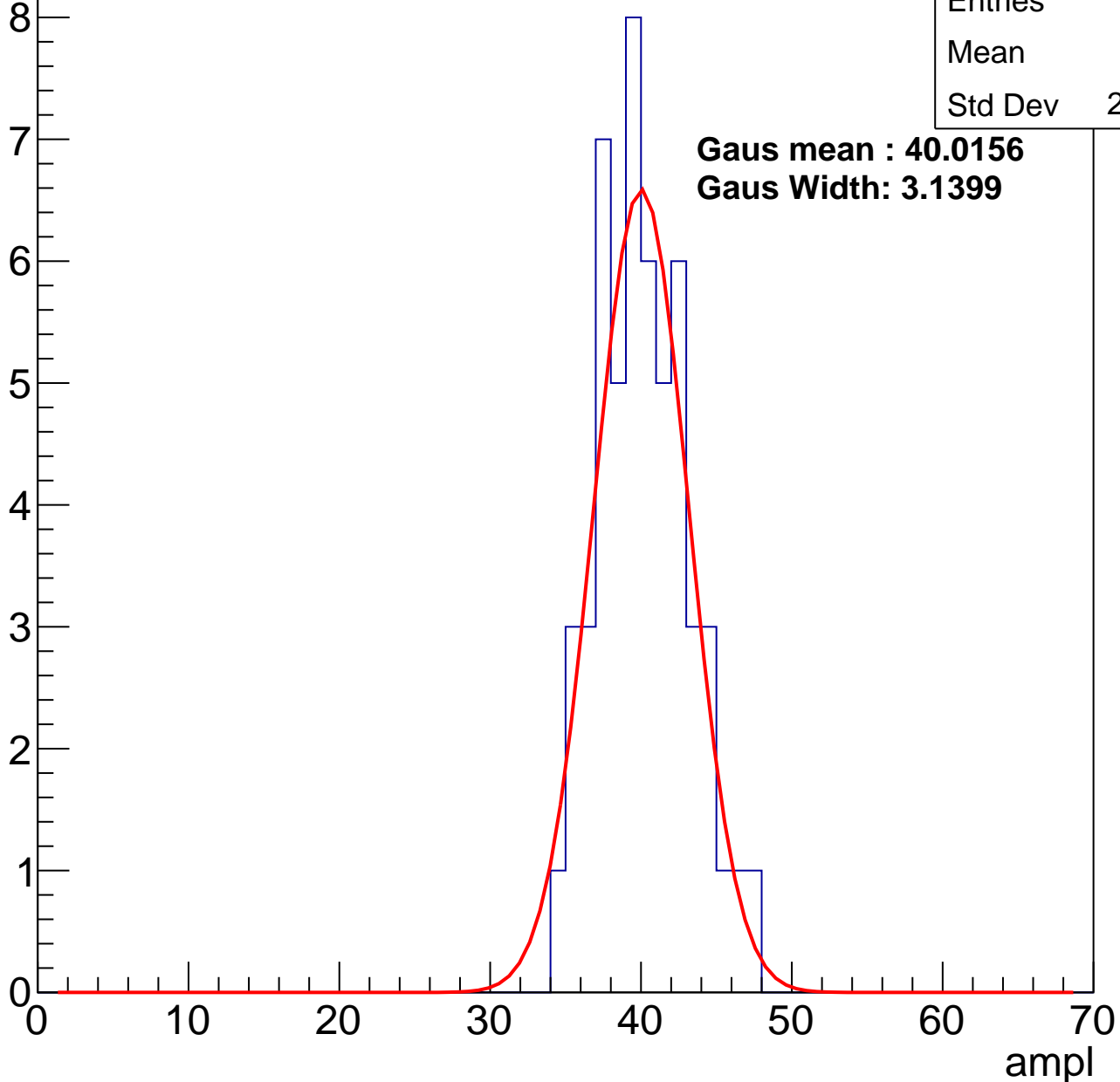
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	39.7
Std Dev	2.943

**Gaus mean : 40.0156**

**Gaus Width: 3.1399**



# B0L001S, U21-ch83, adc2

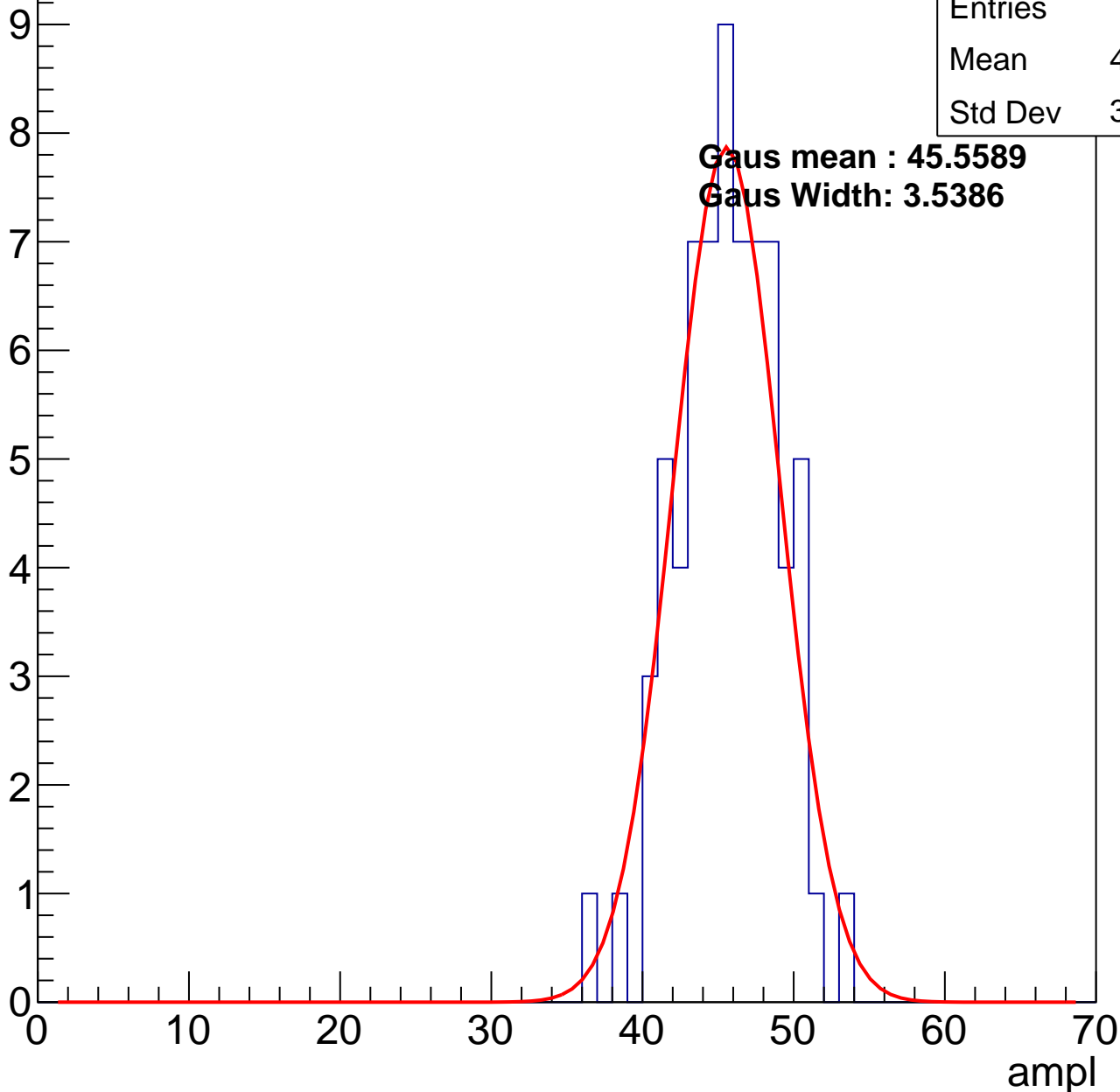
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	45.19
Std Dev	3.276

**Gaus mean : 45.5589**

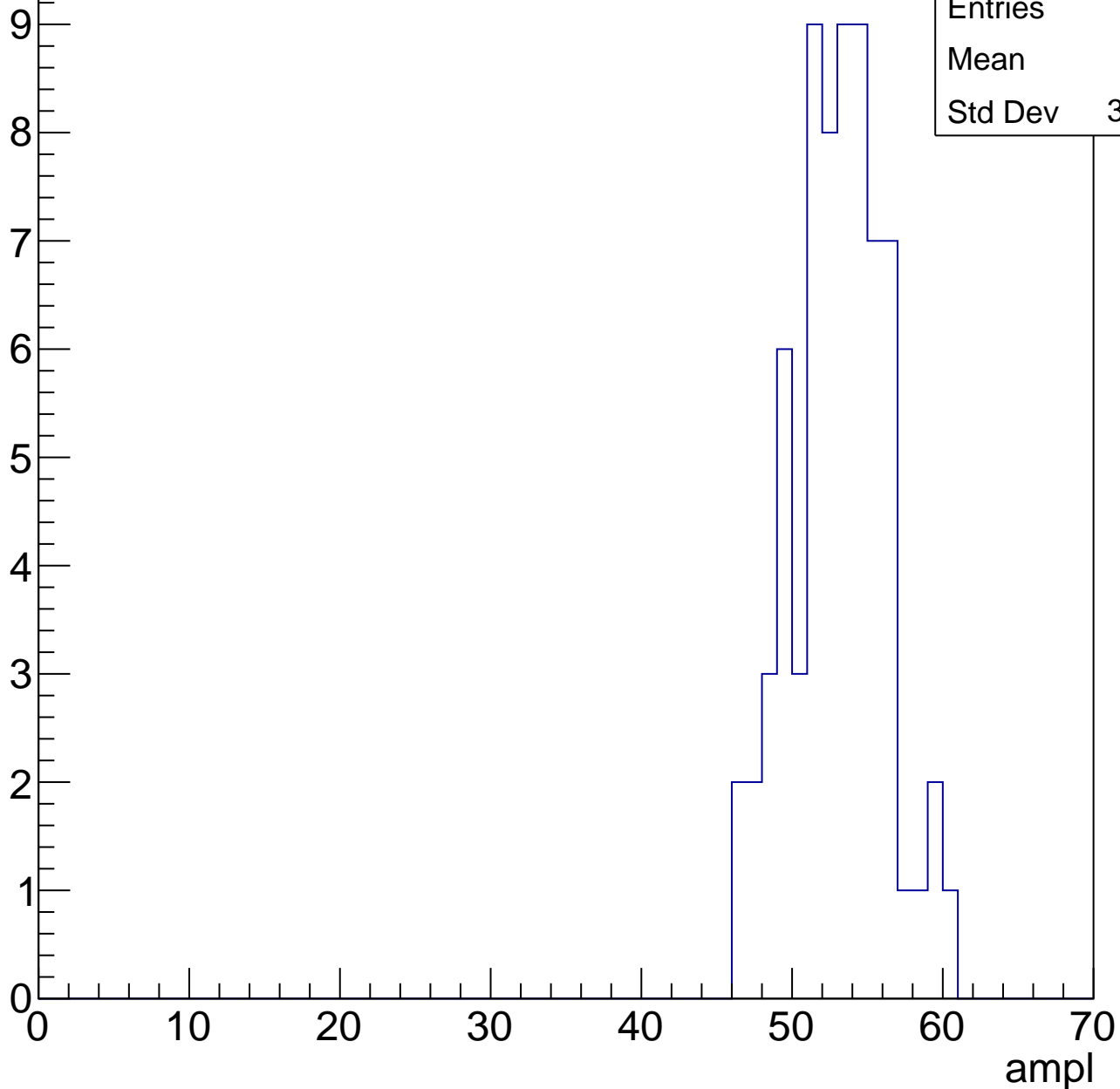
**Gaus Width: 3.5386**



# B0L001S, U21-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

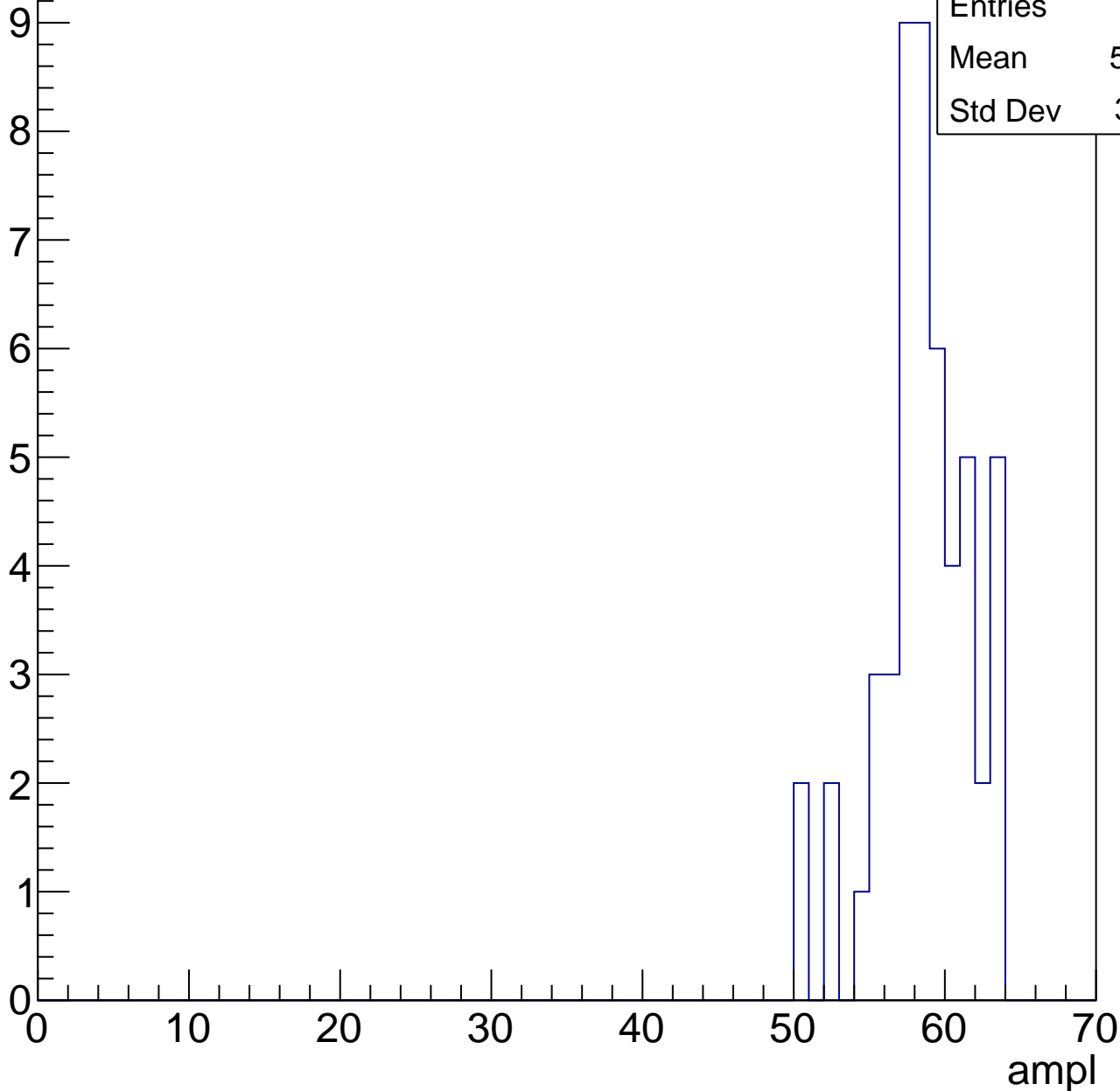


# B0L001S, U21-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	58.12
Std Dev	3.091

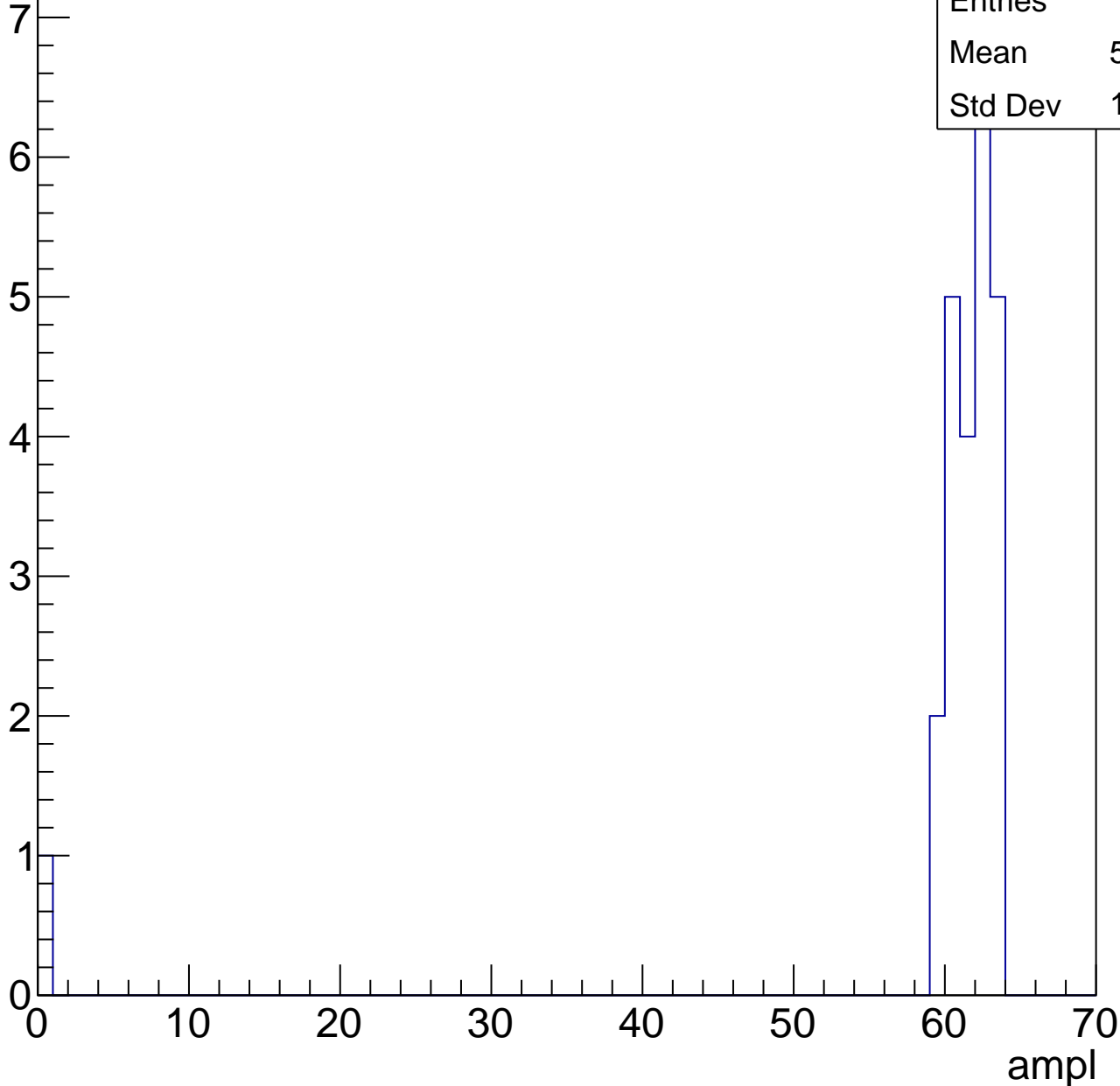


# B0L001S, U21-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	24
Mean	58.79
Std Dev	12.32



# B0L001S, U21-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U21-ch84, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	72
Mean	29.83
Std Dev	3.539

**Gaus mean : 30.8068**

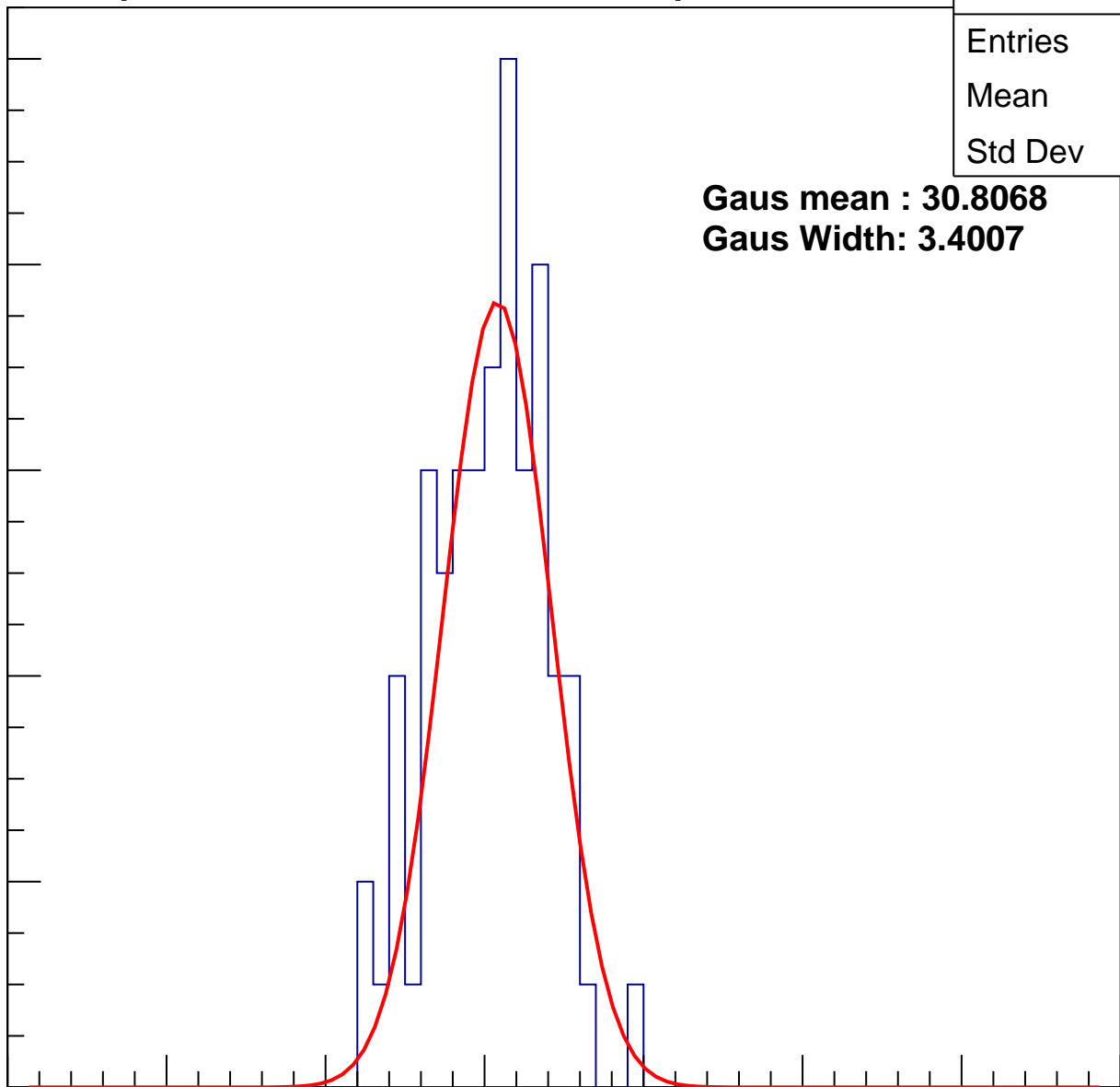
**Gaus Width: 3.4007**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U21-ch84, adc1

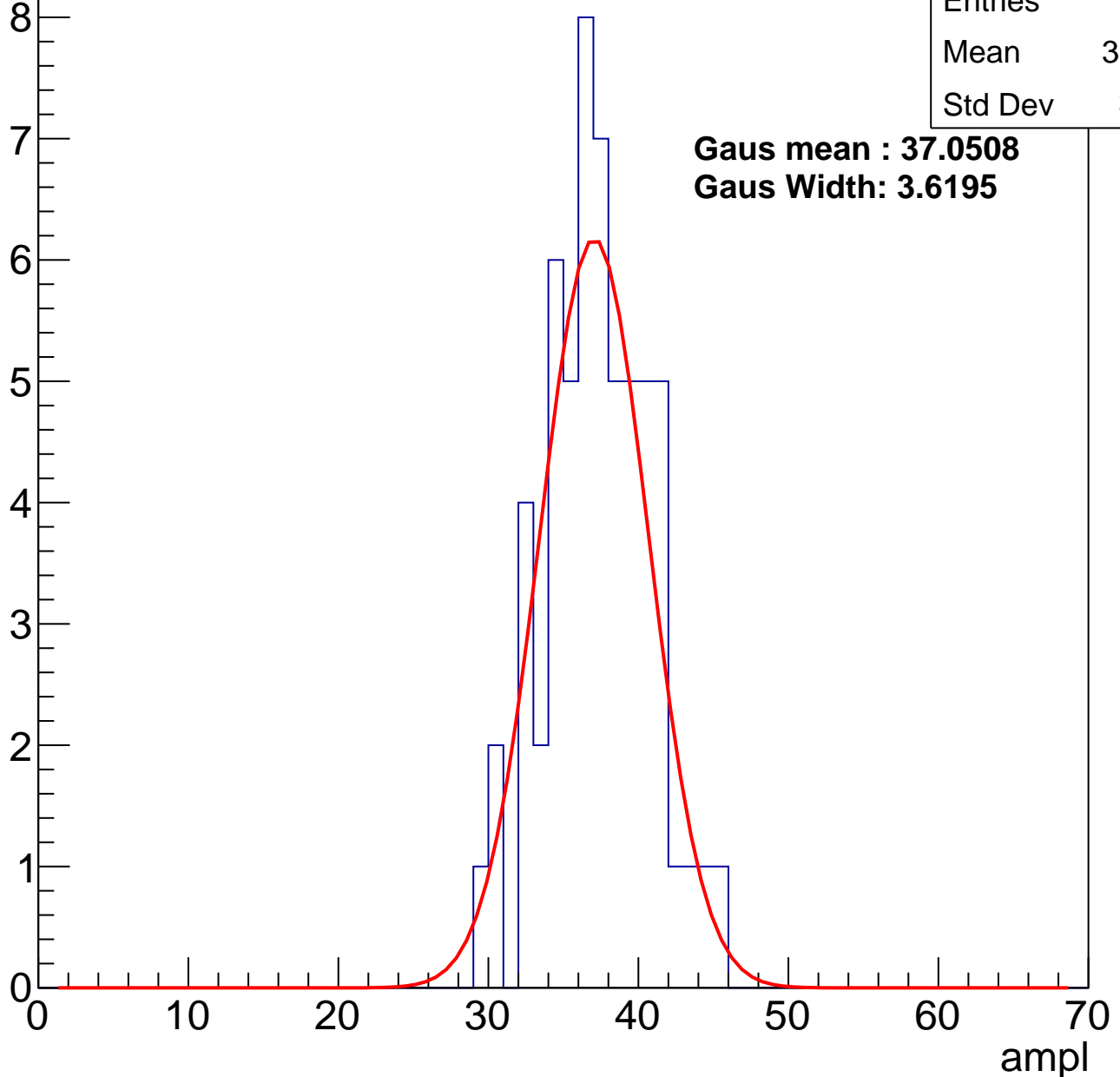
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	36.83
Std Dev	3.44

**Gaus mean : 37.0508**

**Gaus Width: 3.6195**



# B0L001S, U21-ch84, adc2

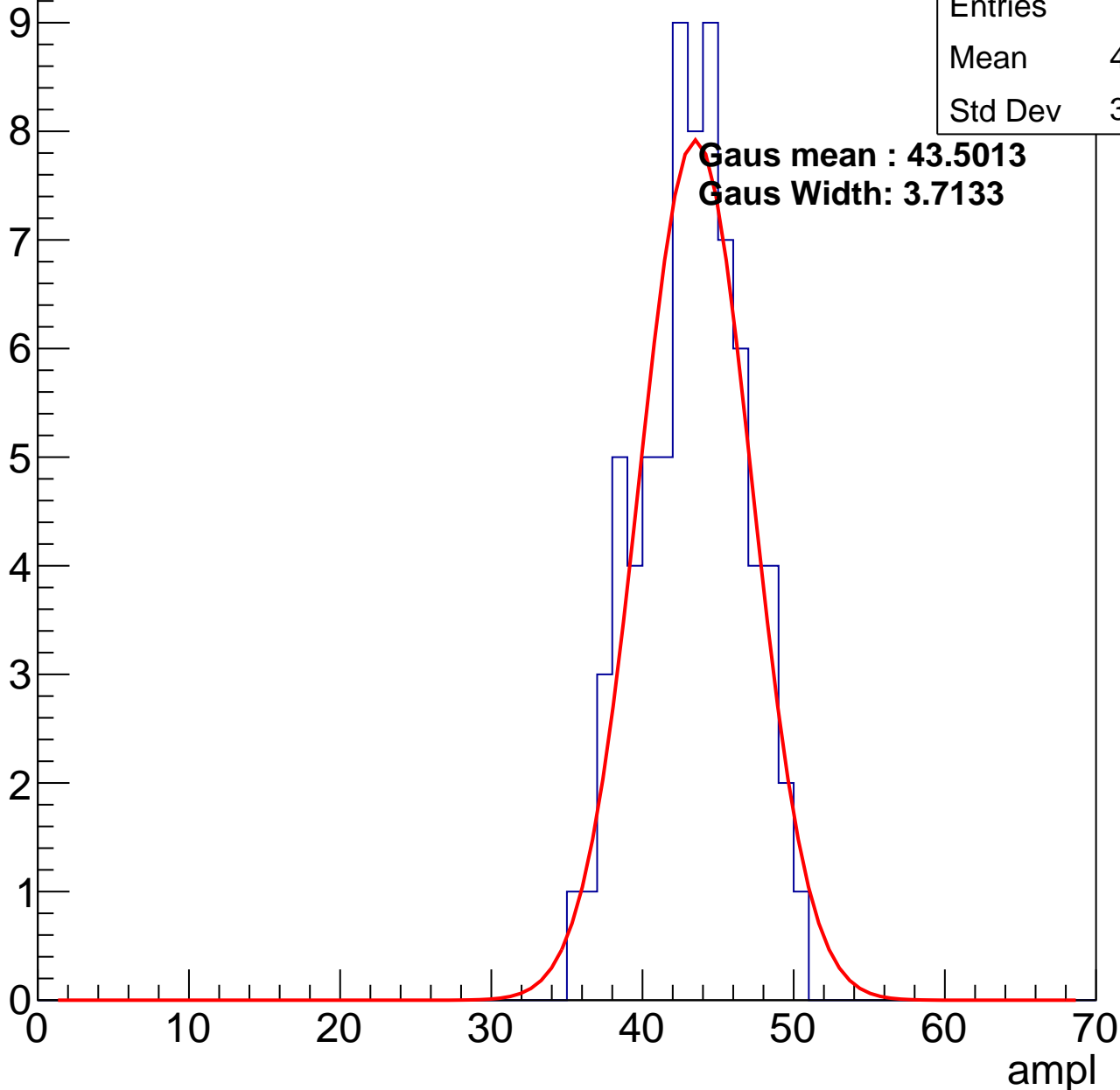
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	42.84
Std Dev	3.405

**Gaus mean : 43.5013**

**Gaus Width: 3.7133**

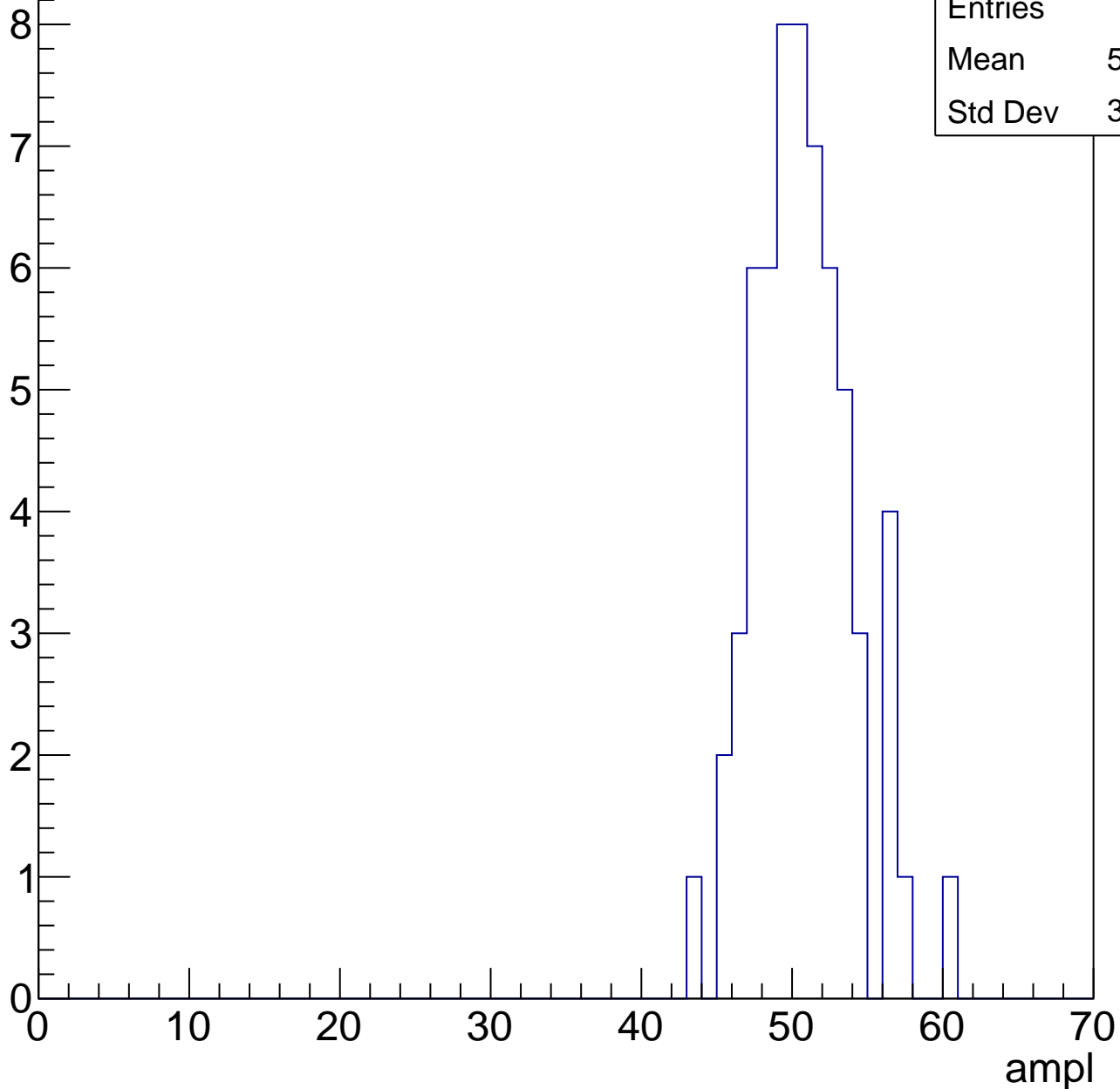


# B0L001S, U21-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	50.33
Std Dev	3.248



# B0L001S, U21-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	58
Mean	55.59
Std Dev	3.162

Entry

10

8

6

4

2

0

0

10

20

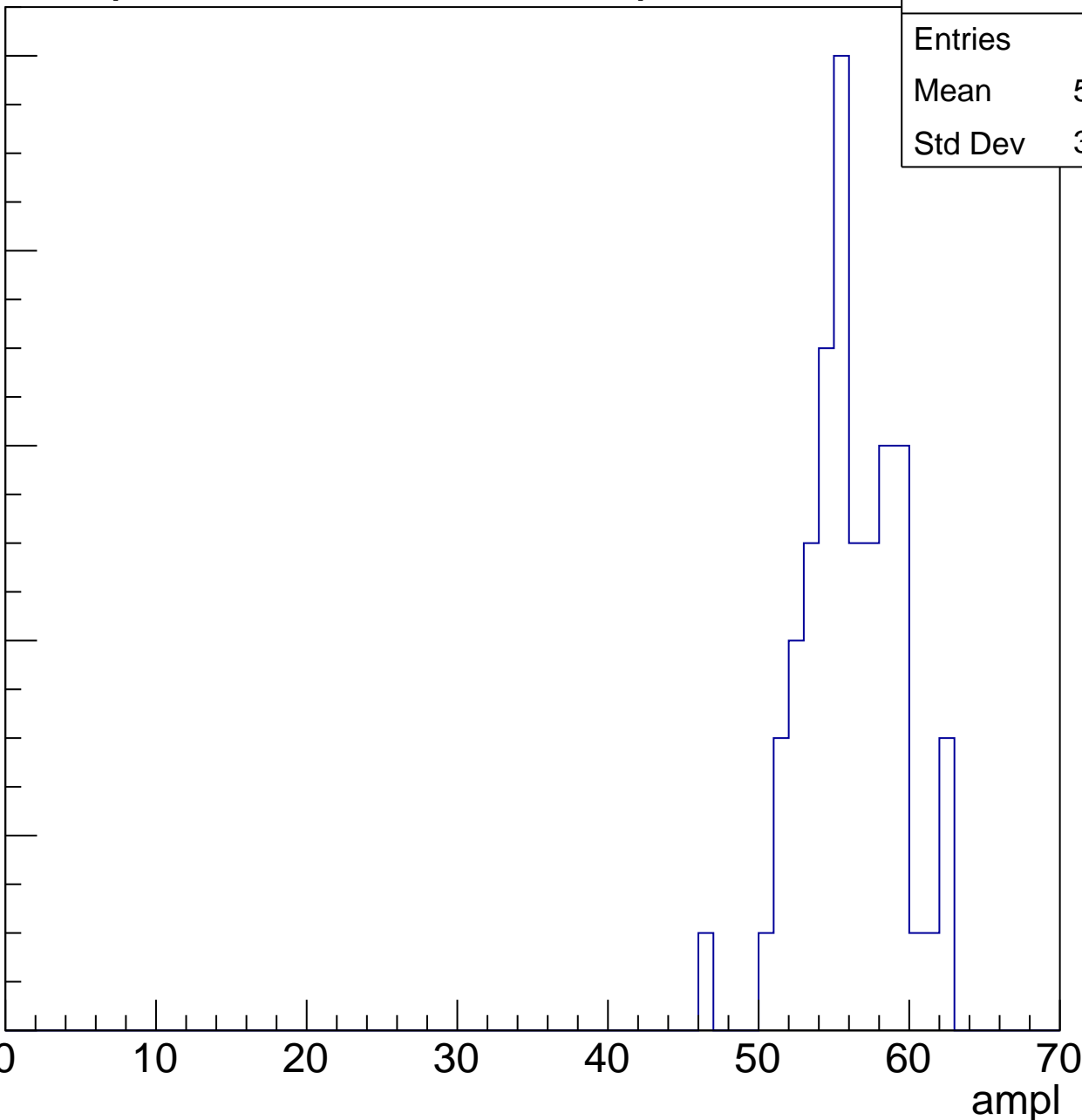
30

40

50

60

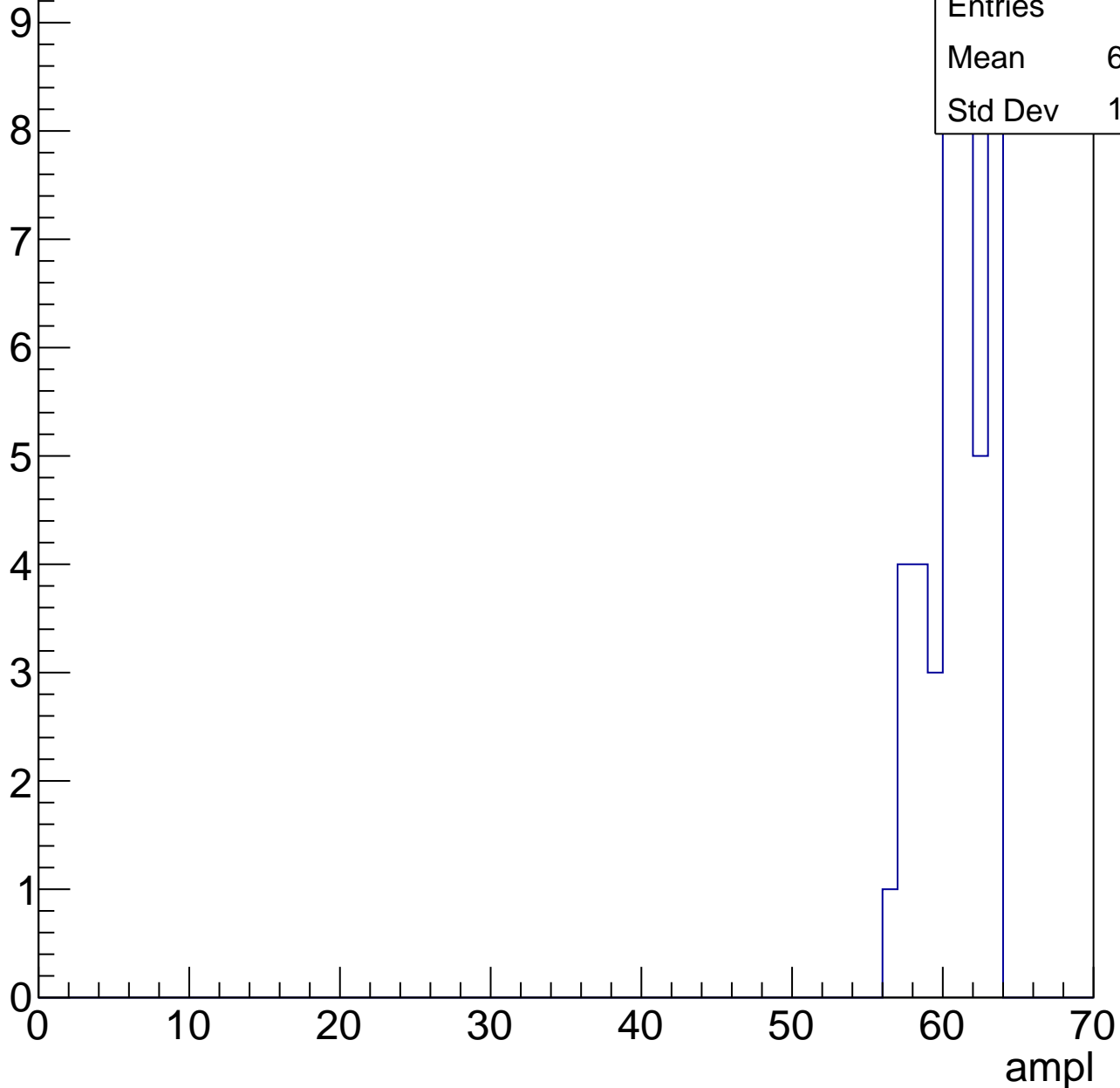
ampl



# B0L001S, U21-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

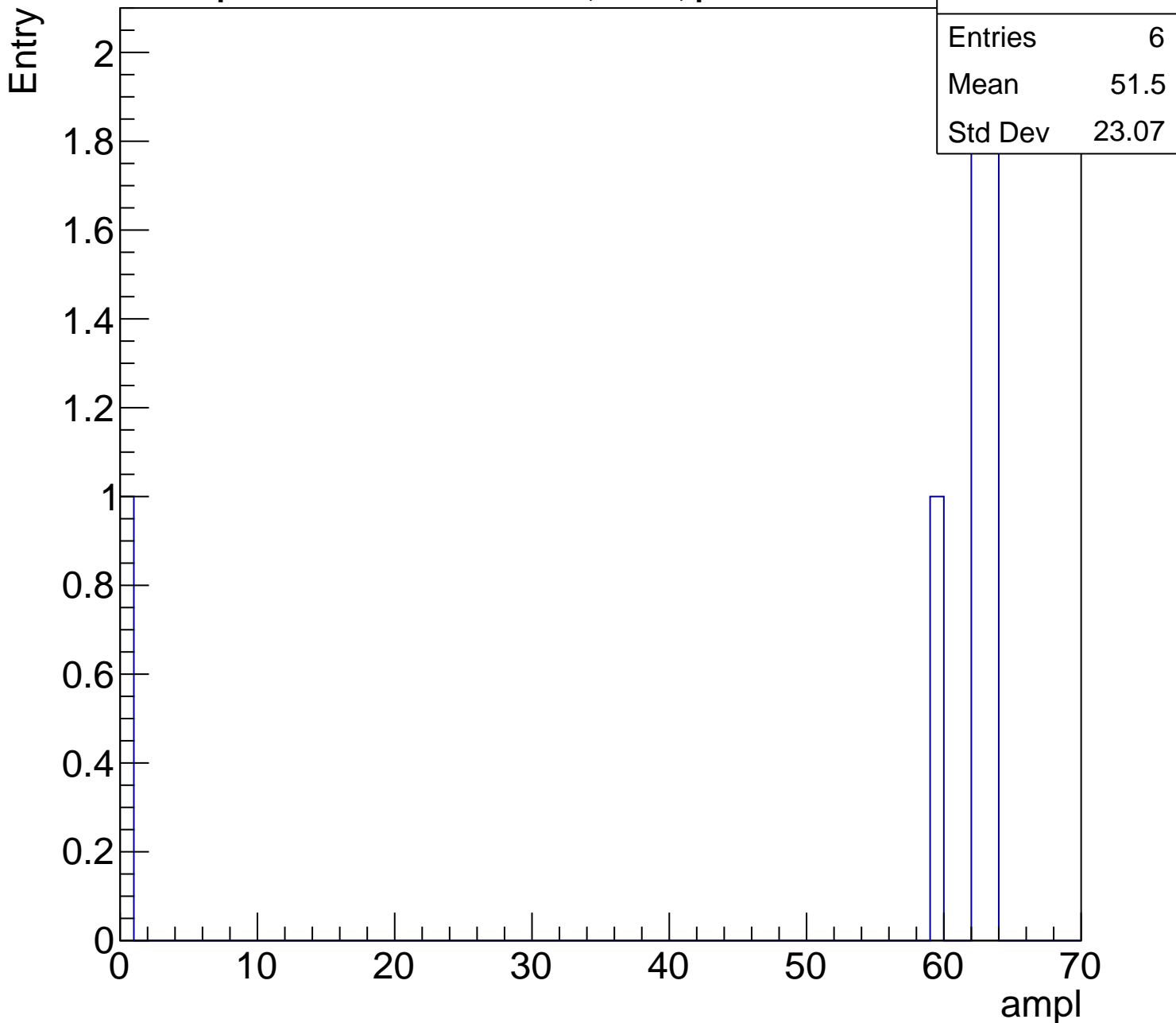
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	51.5
Std Dev	23.07

0 10 20 30 40 50 60 70

ampl





# B0L001S, U21-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch85, adc0

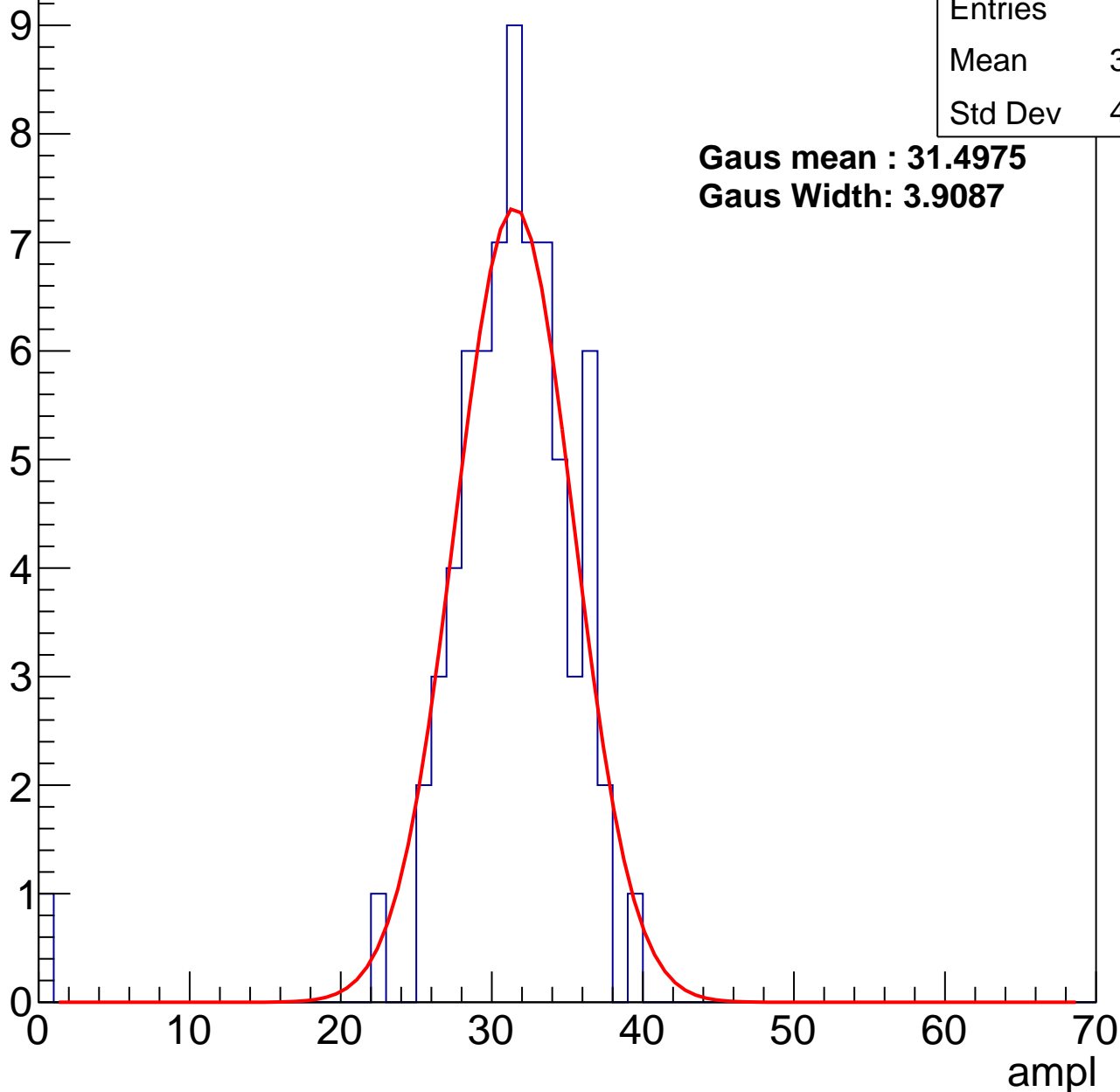
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	30.69
Std Dev	4.993

**Gaus mean : 31.4975**

**Gaus Width: 3.9087**



# B0L001S, U21-ch85, adc1

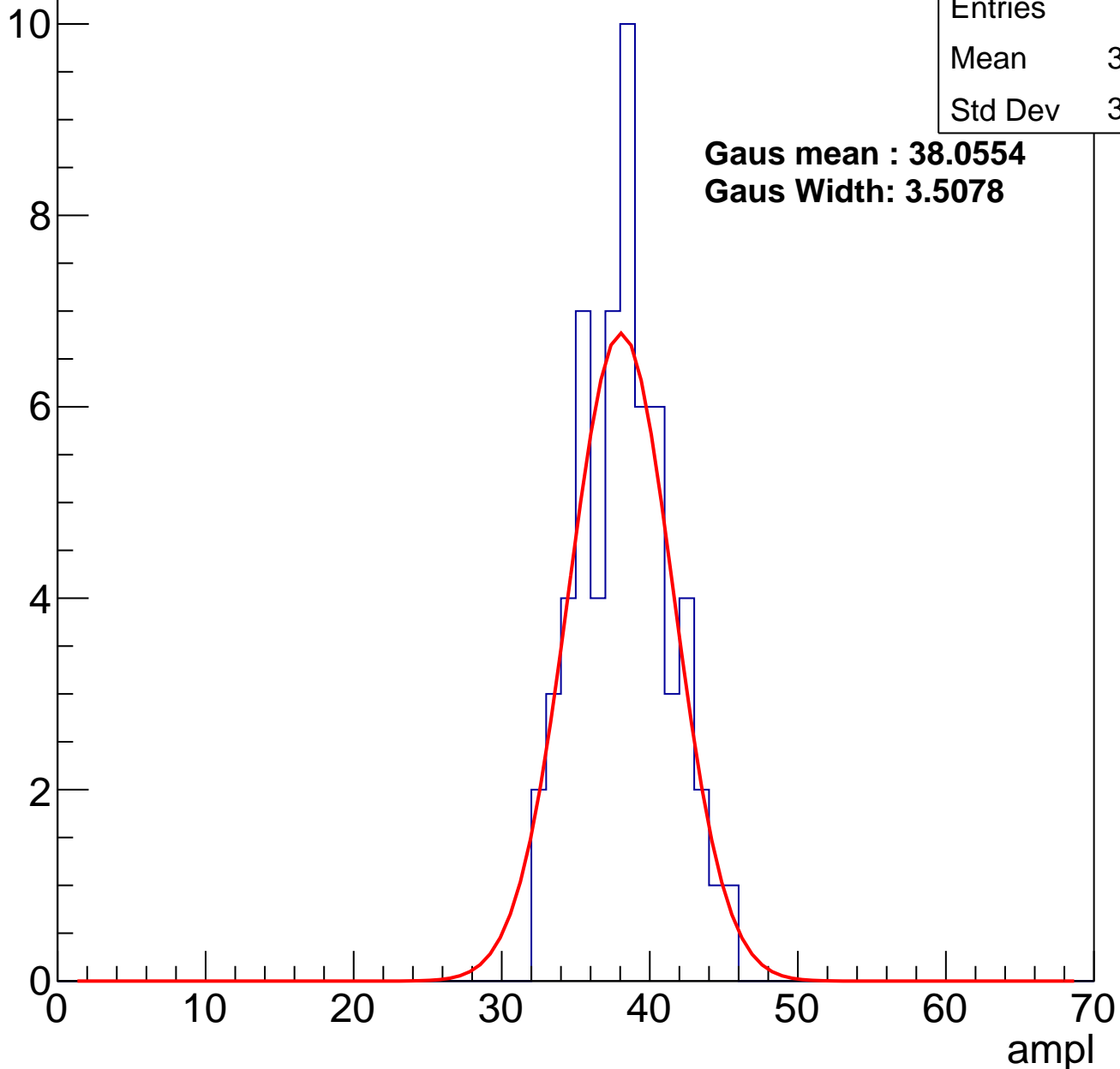
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	60
Mean	37.78
Std Dev	3.028

**Gaus mean : 38.0554**

**Gaus Width: 3.5078**

Entry



# B0L001S, U21-ch85, adc2

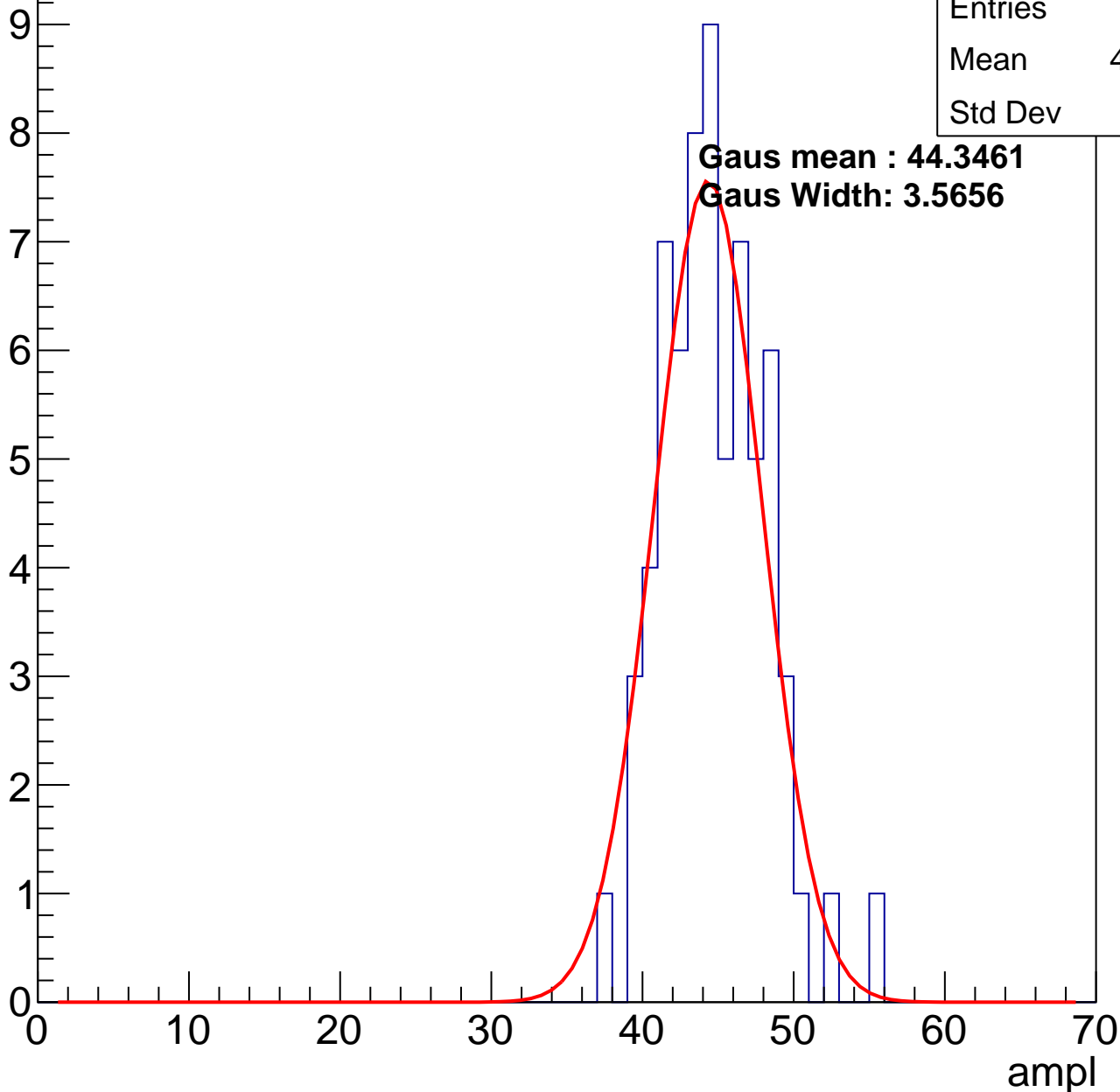
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	44.28
Std Dev	3.34

**Gaus mean : 44.3461**

**Gaus Width: 3.5656**



# B0L001S, U21-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	74
Mean	51.08
Std Dev	3.303

Entry

10

8

6

4

2

0

0

10

20

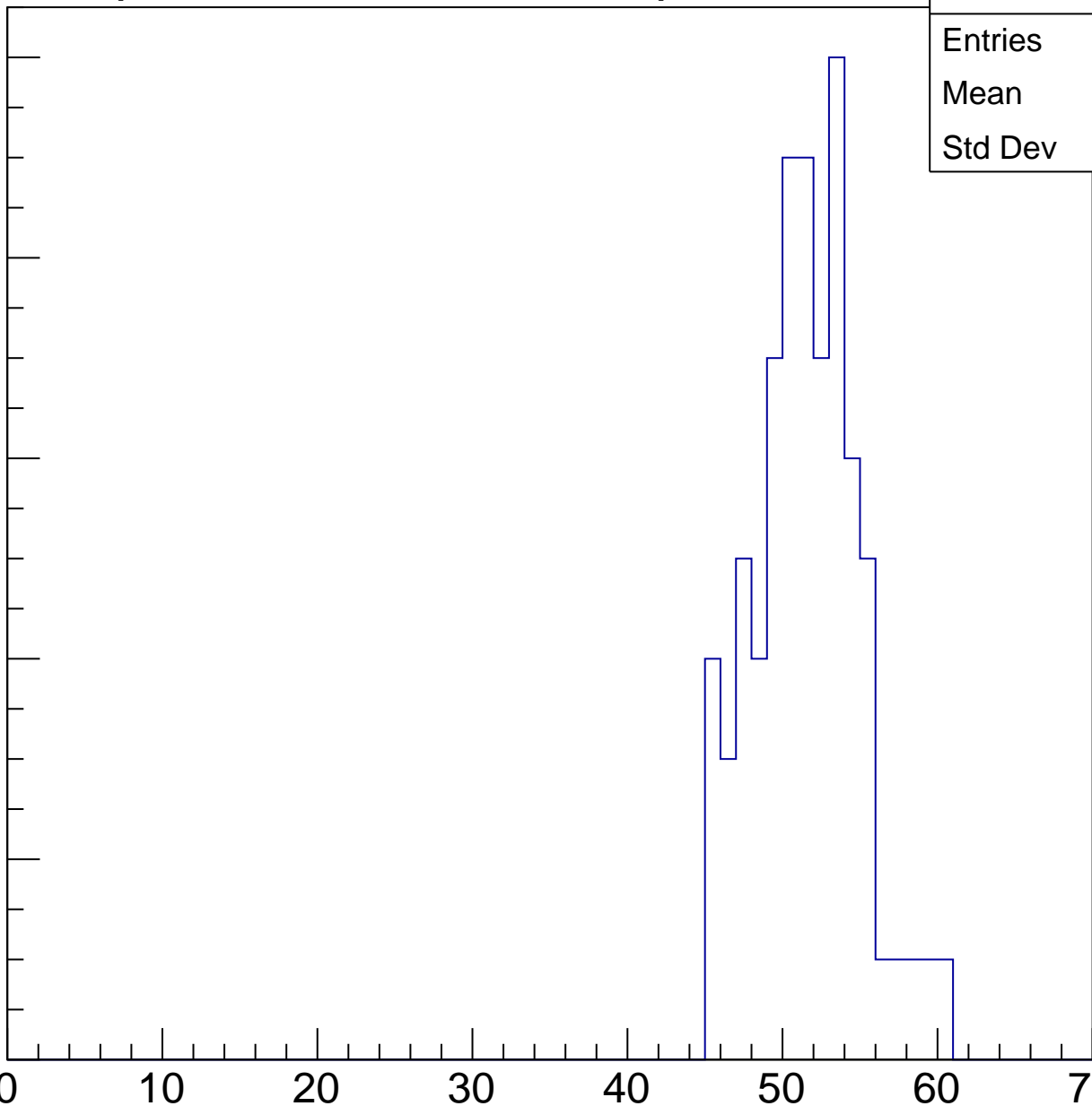
30

40

50

60

ampl

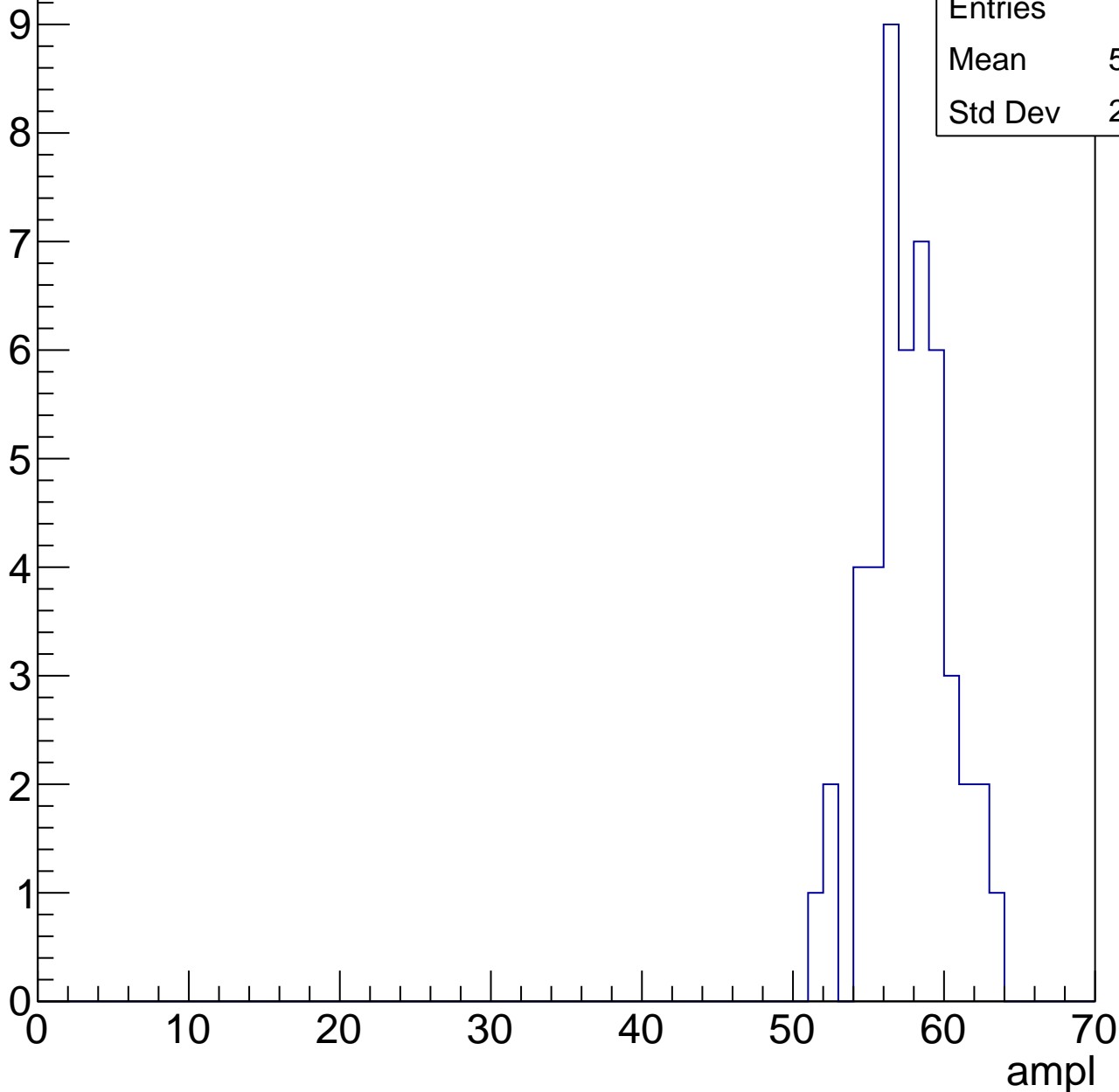


# B0L001S, U21-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	57.15
Std Dev	2.617

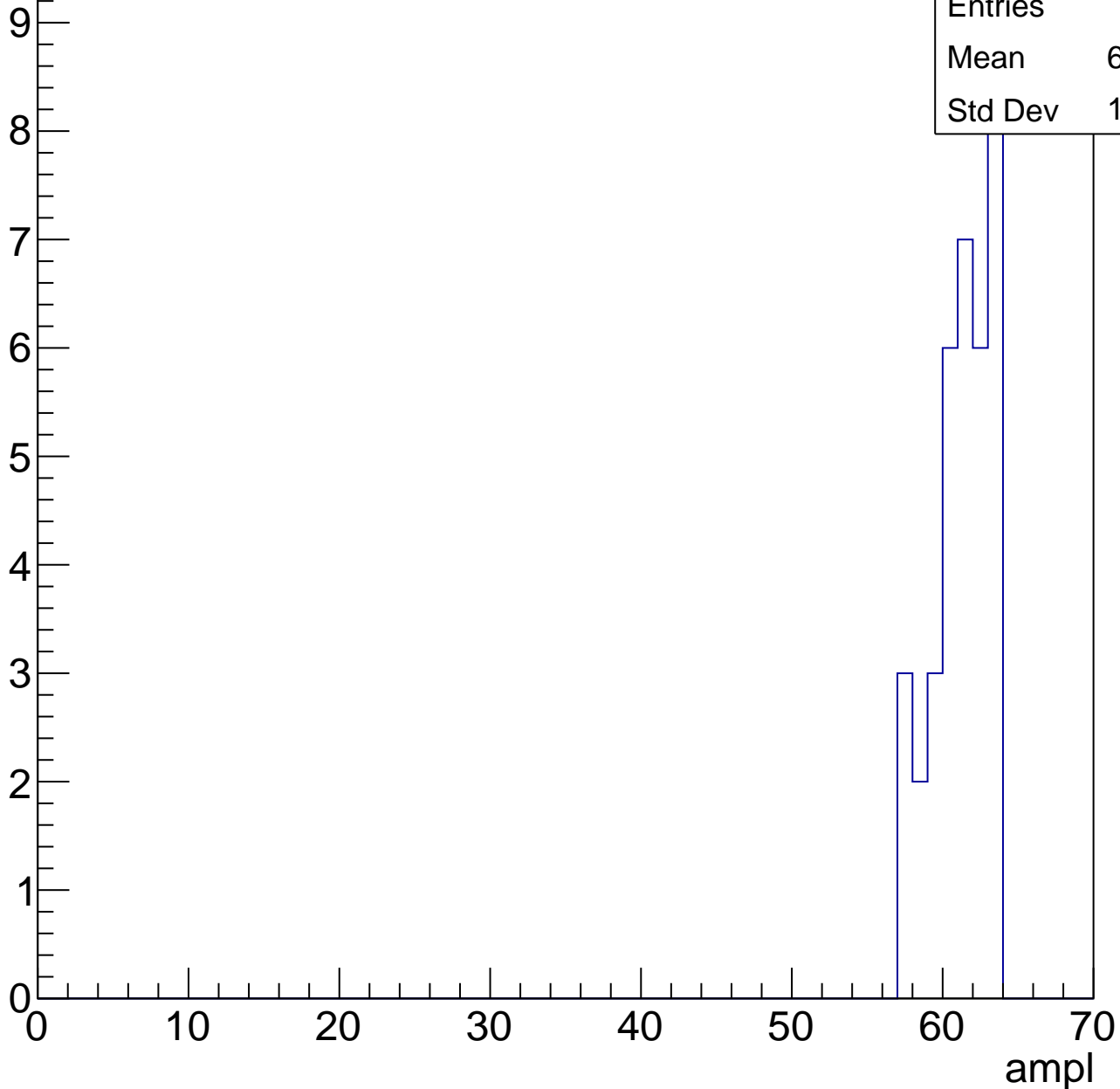


# B0L001S, U21-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

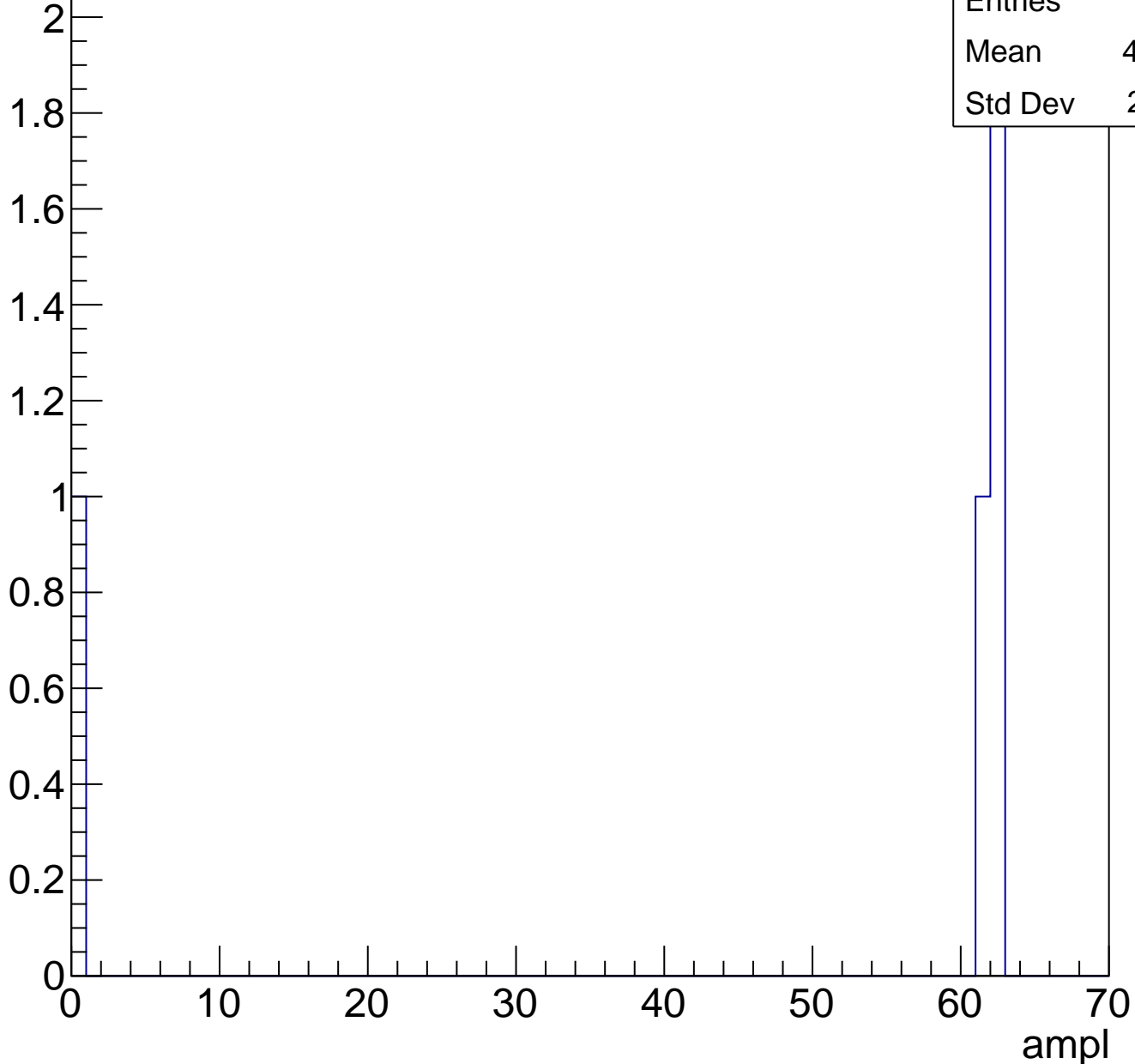
Entries	36
Mean	60.83
Std Dev	1.863



# B0L001S, U21-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch86, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	57
Mean	28.25
Std Dev	6.314

**Gaus mean : 29.6853**

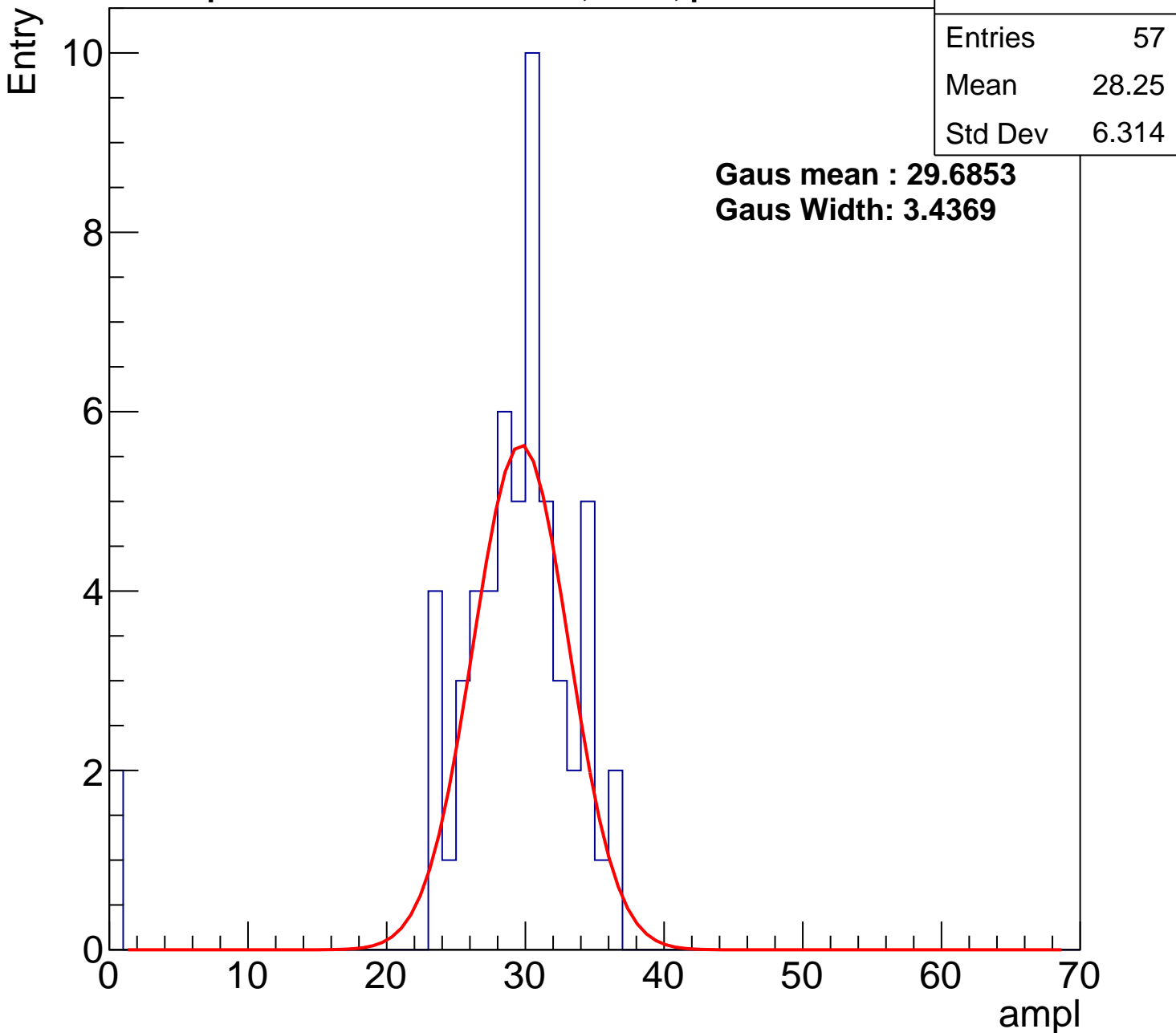
**Gaus Width: 3.4369**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U21-ch86, adc1

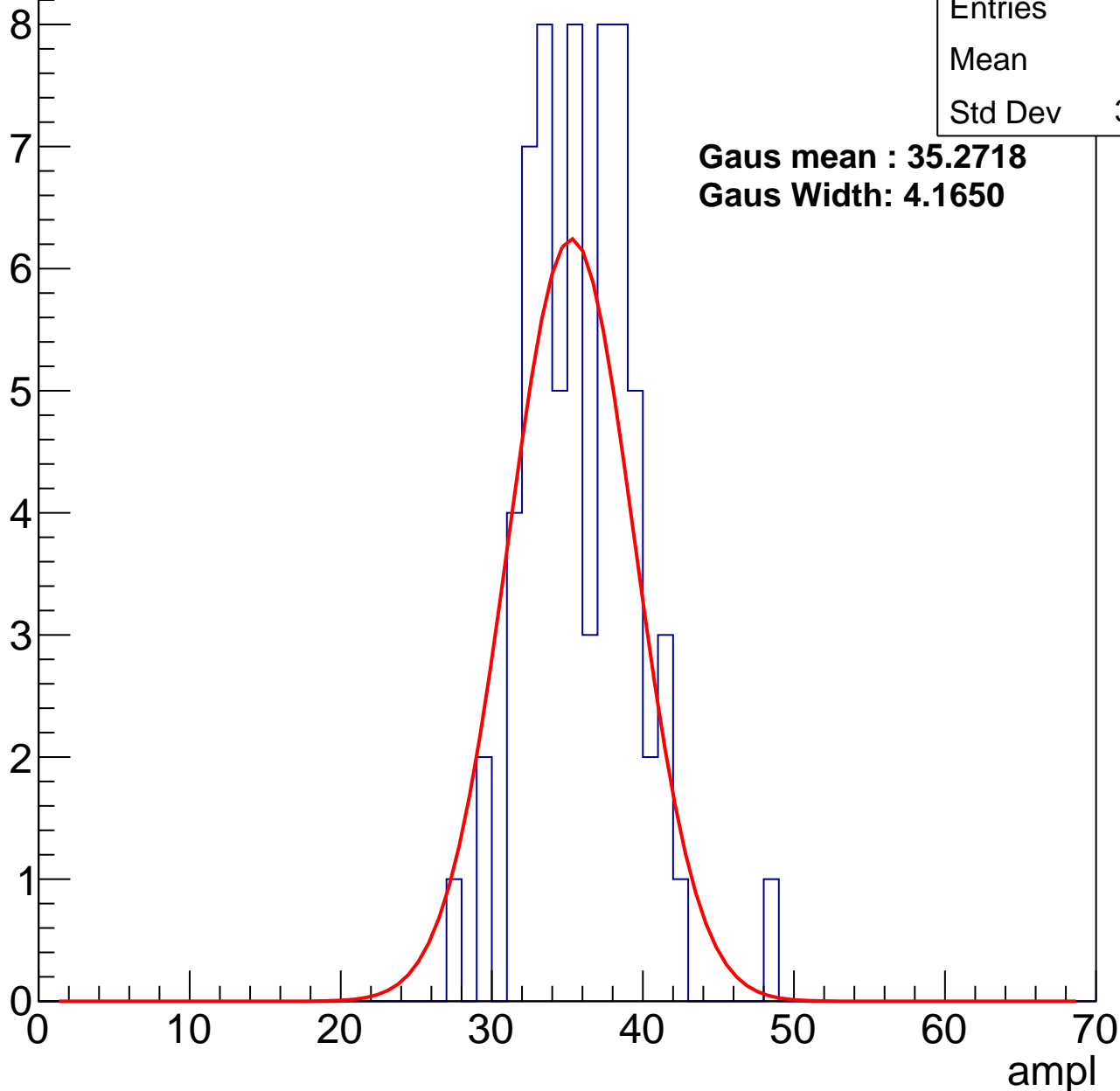
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	35.5
Std Dev	3.581

**Gaus mean : 35.2718**

**Gaus Width: 4.1650**



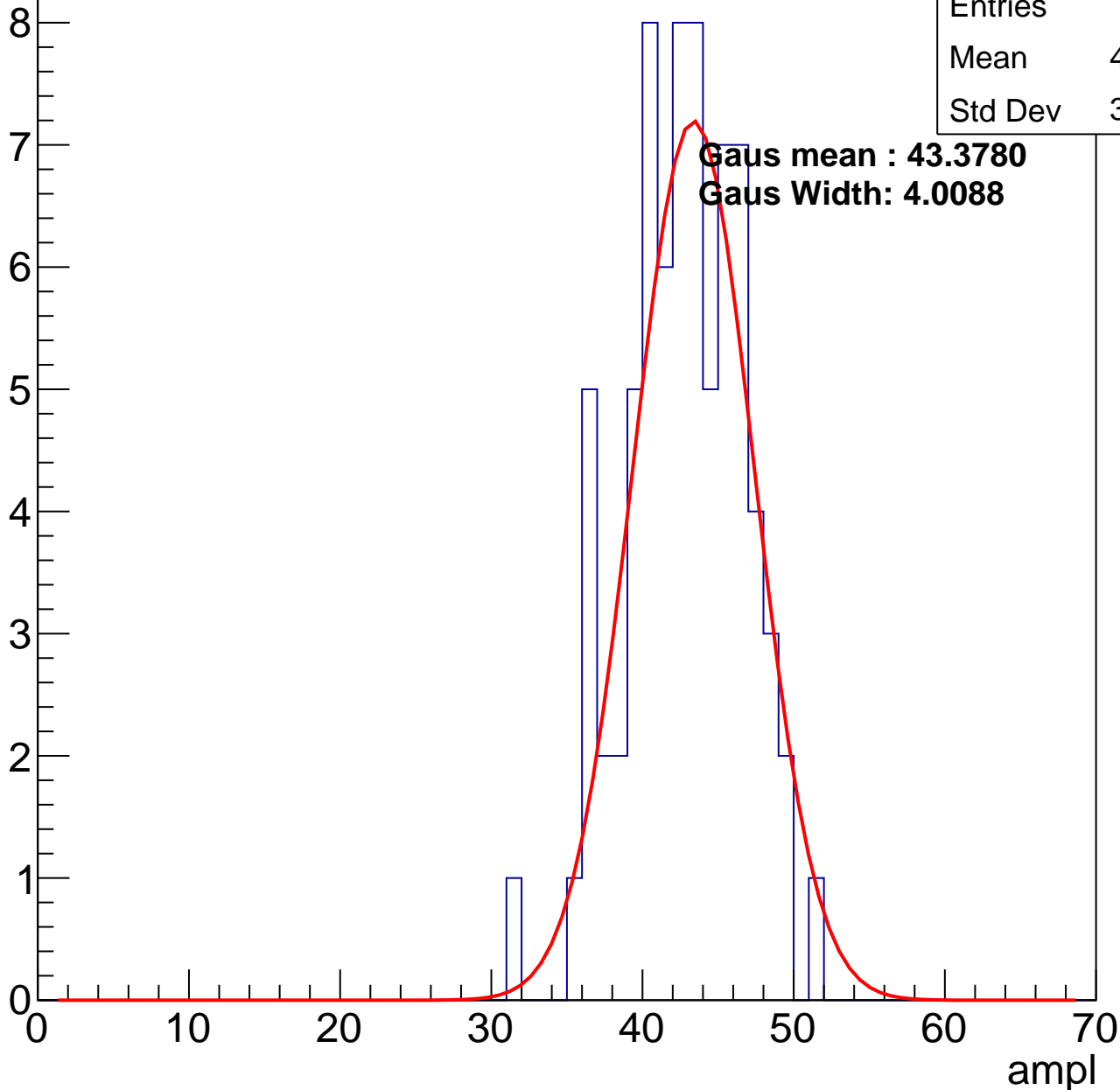
# B0L001S, U21-ch86, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	42.33
Std Dev	3.824

**Gaus mean : 43.3780**  
**Gaus Width: 4.0088**

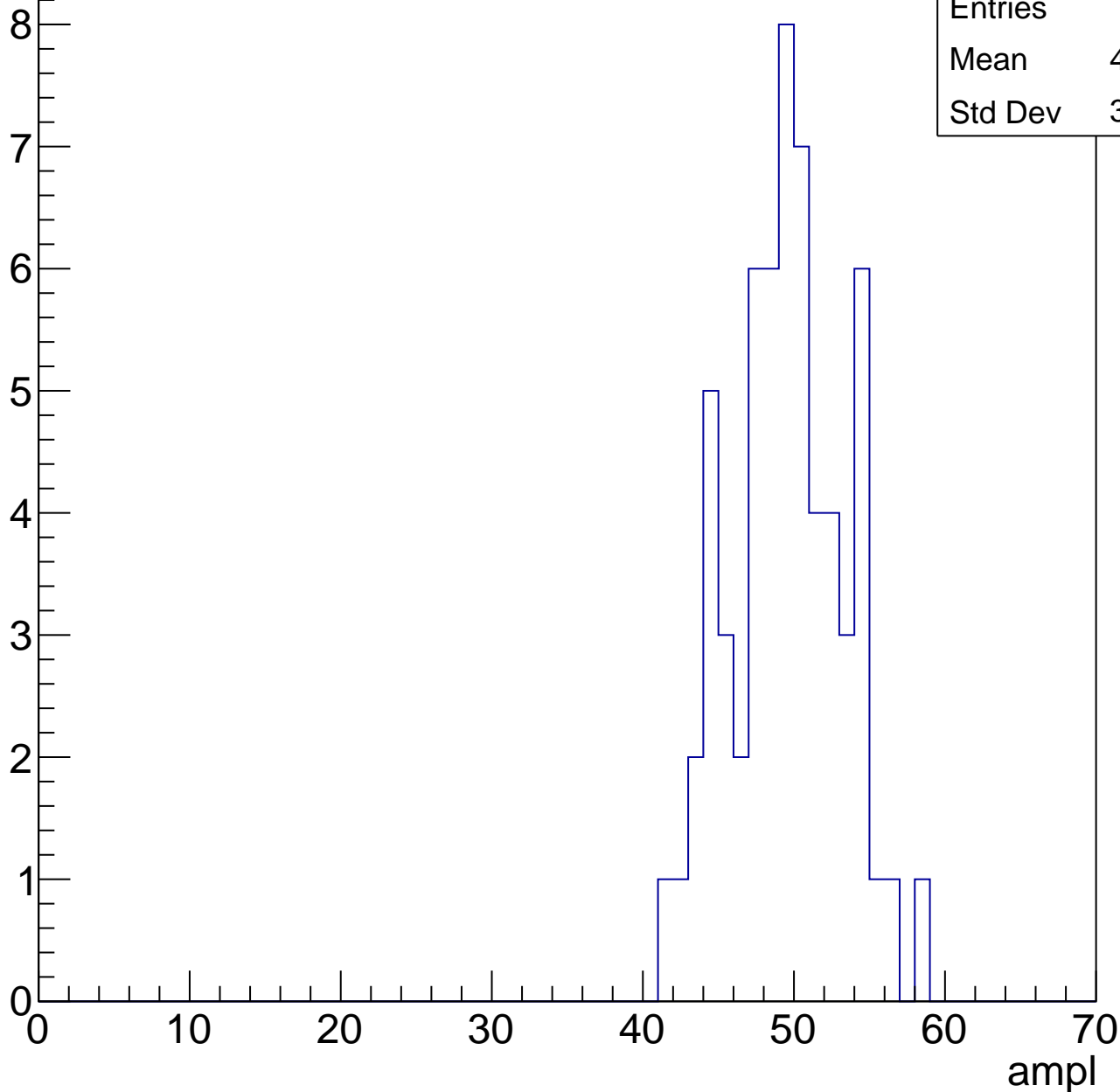


# B0L001S, U21-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	49.05
Std Dev	3.686

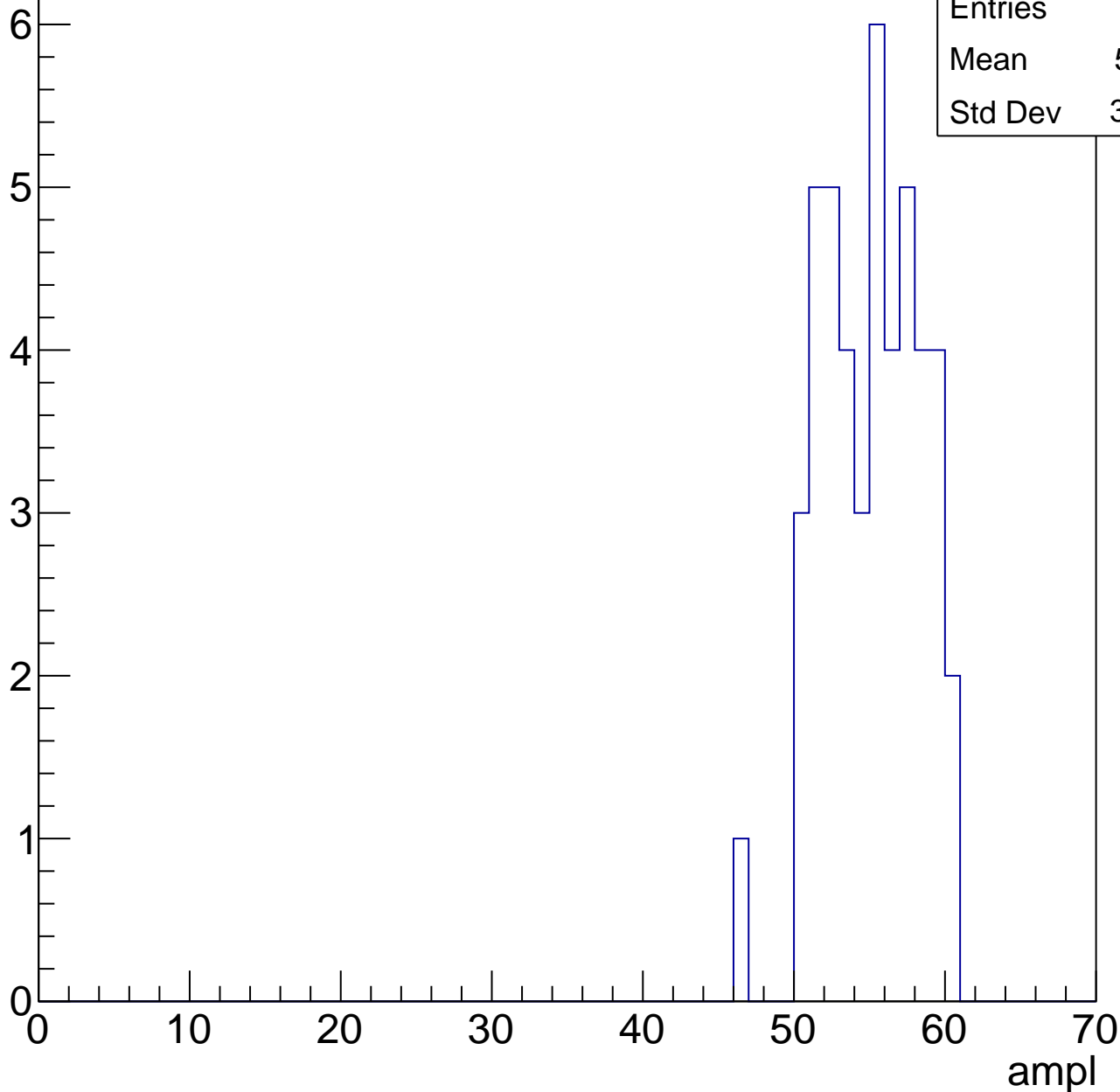


# B0L001S, U21-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	54.61
Std Dev	3.186

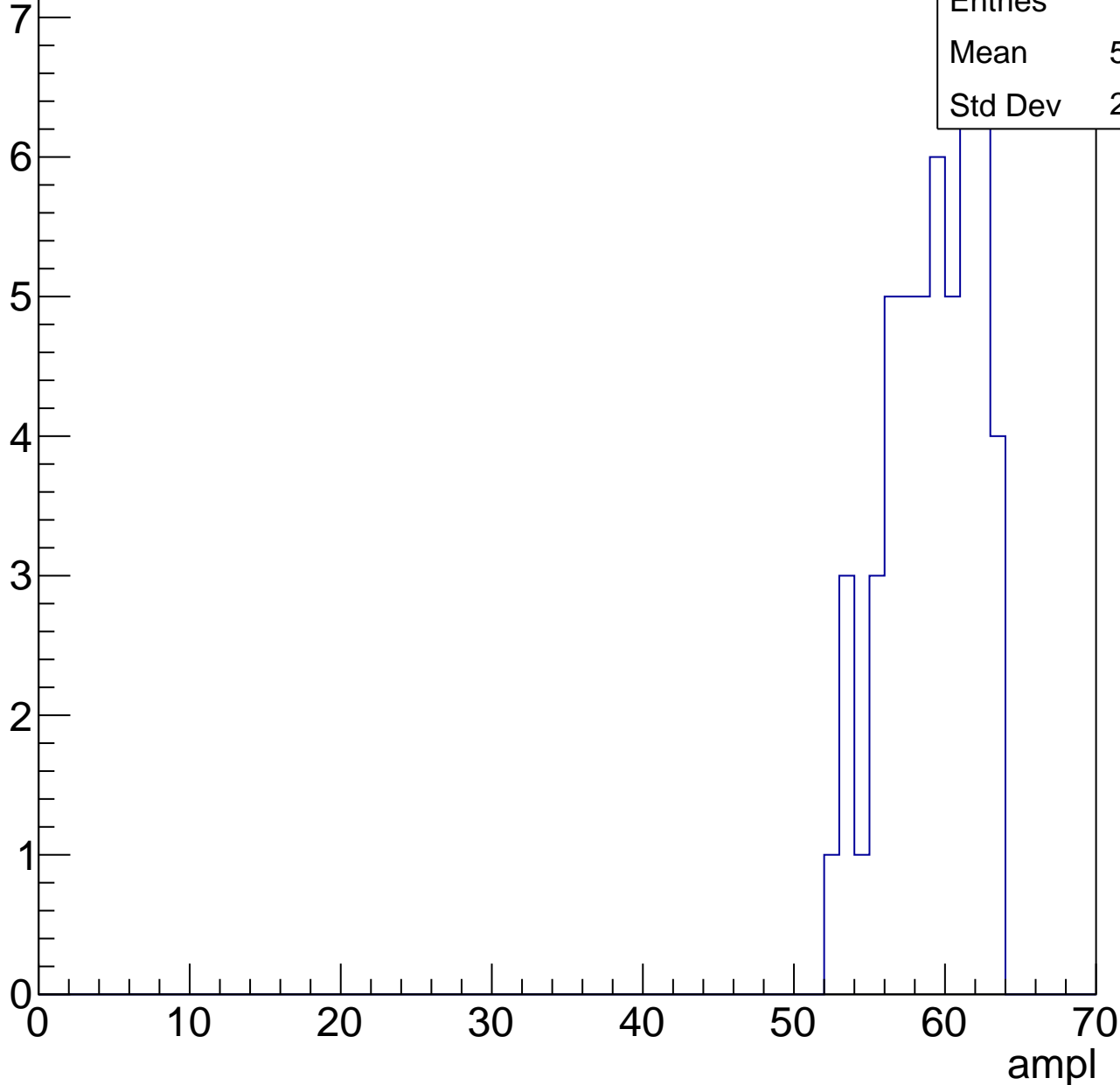


# B0L001S, U21-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	58.69
Std Dev	2.958

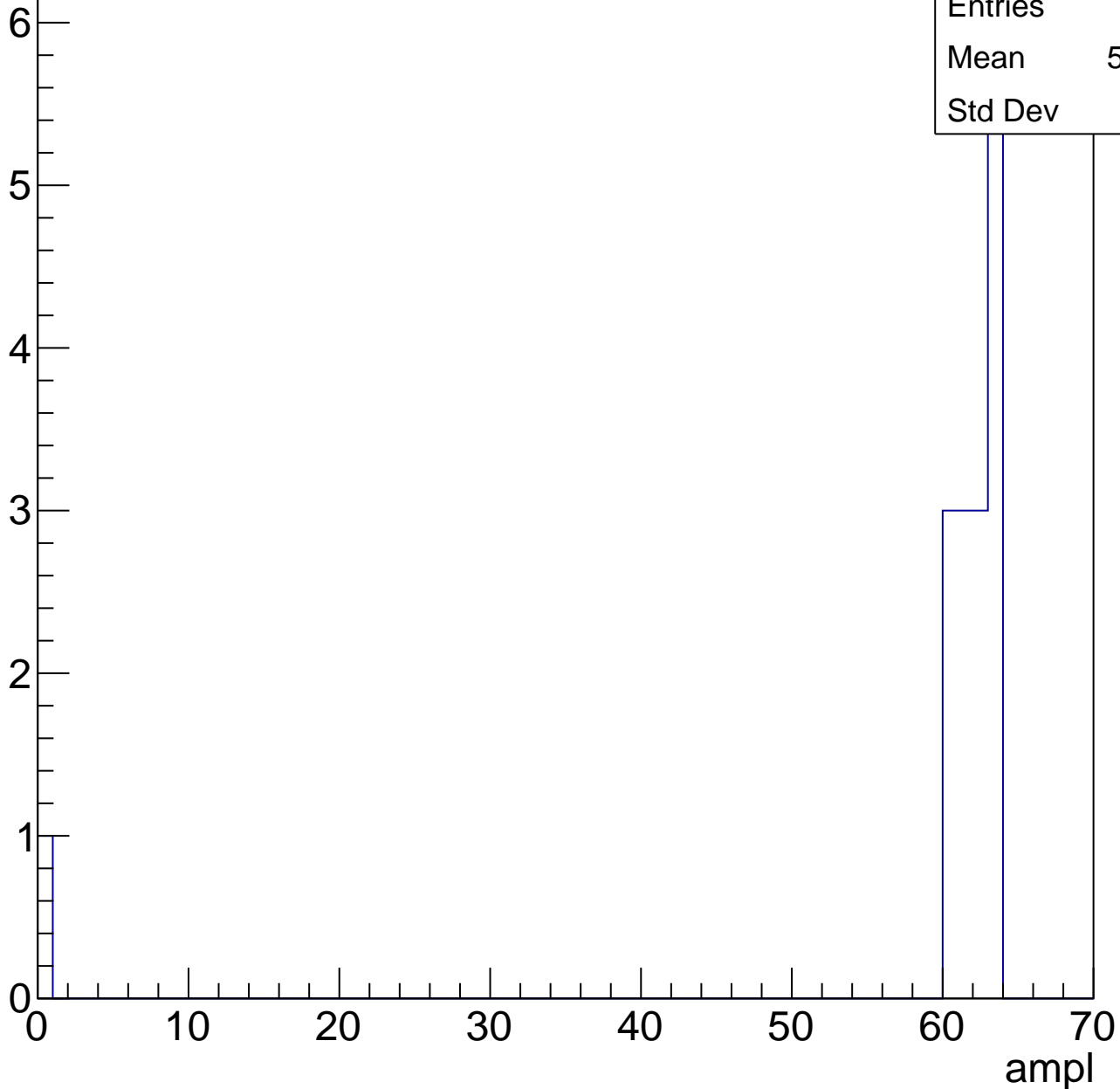


# B0L001S, U21-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	16
Mean	57.94
Std Dev	15





# B0L001S, U21-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch87, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	64
Mean	31.81
Std Dev	3.005

**Gaus mean : 31.9036**

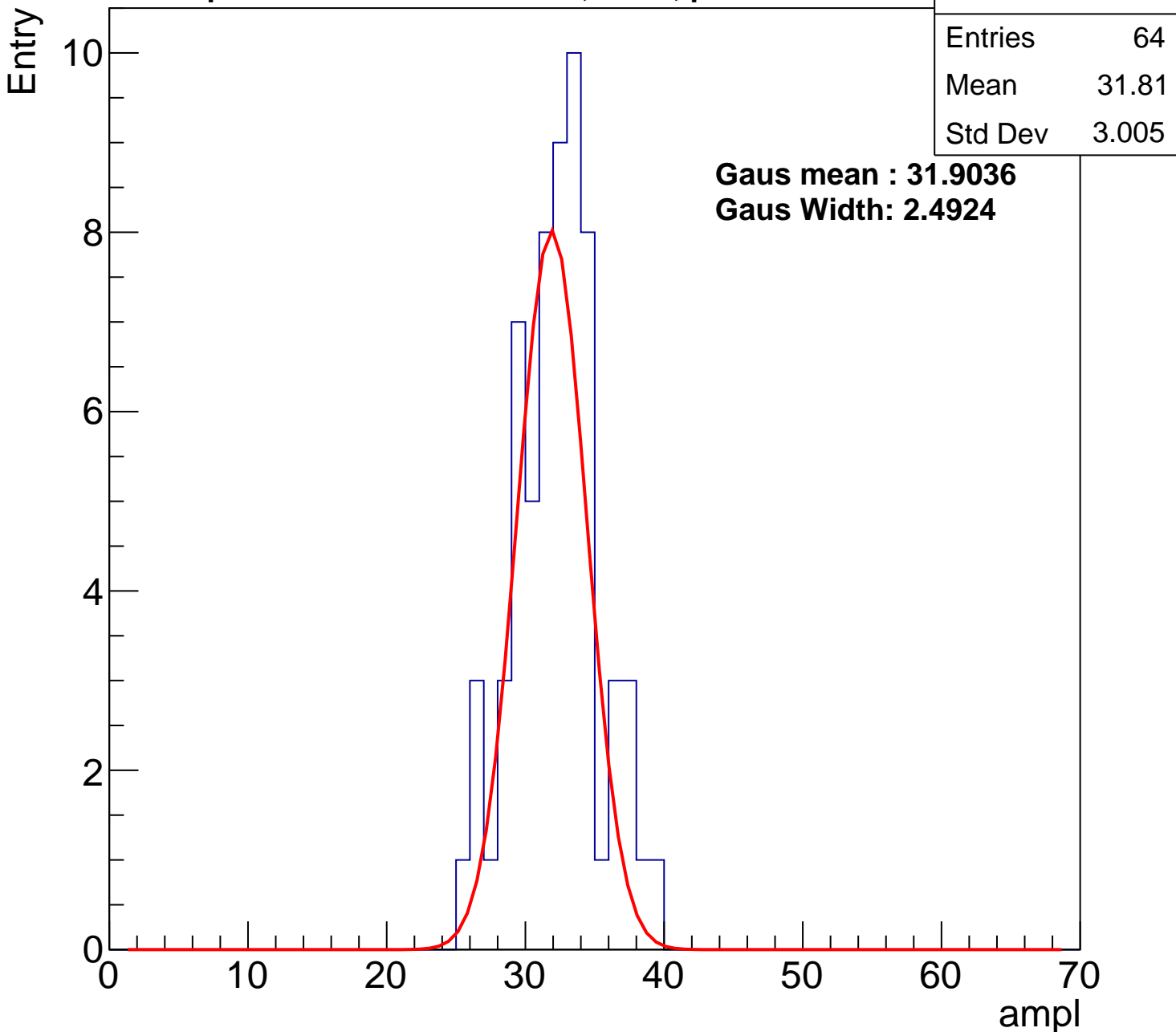
**Gaus Width: 2.4924**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U21-ch87, adc1

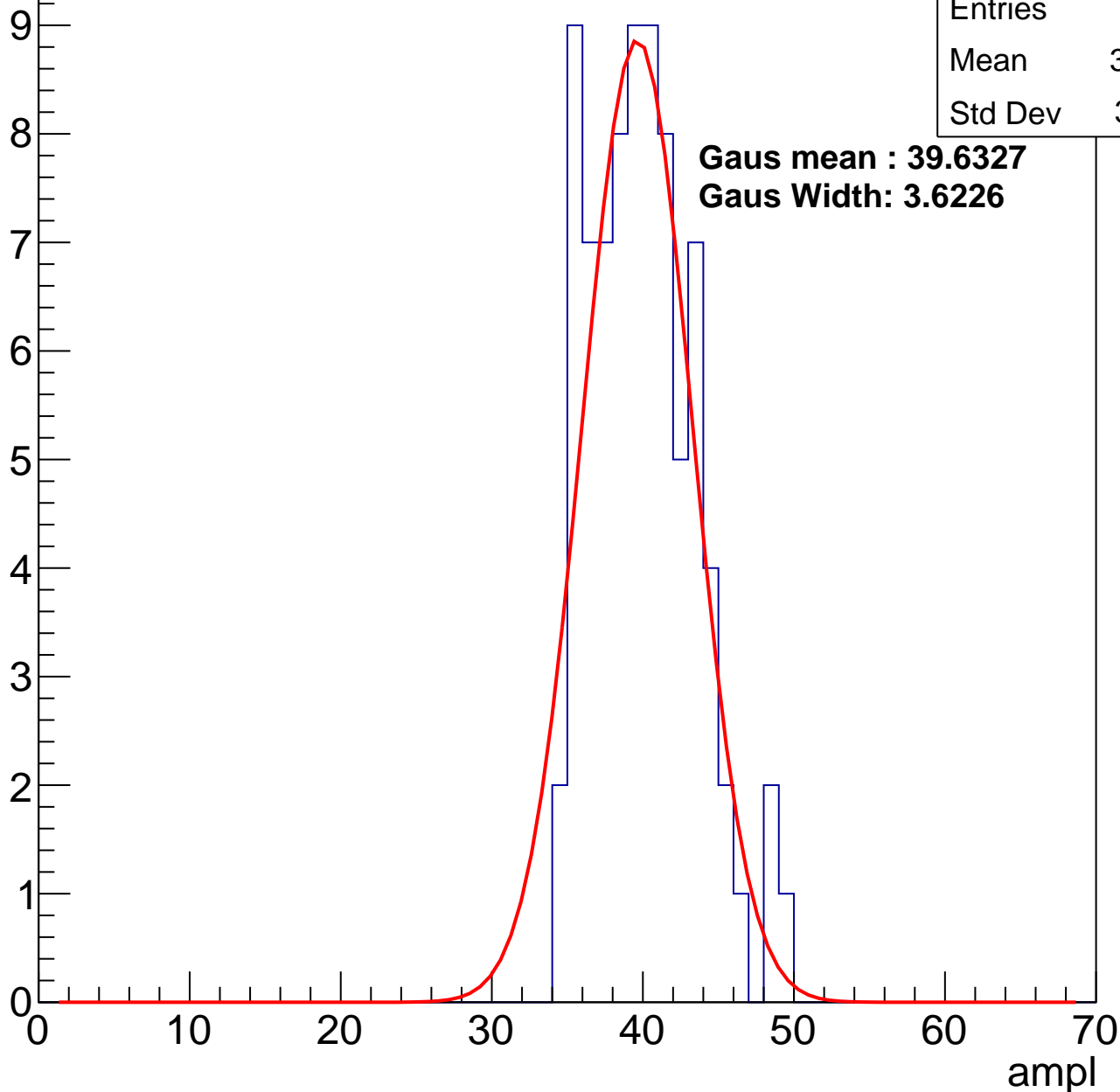
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	39.57
Std Dev	3.421

**Gaus mean : 39.6327**

**Gaus Width: 3.6226**



# B0L001S, U21-ch87, adc2

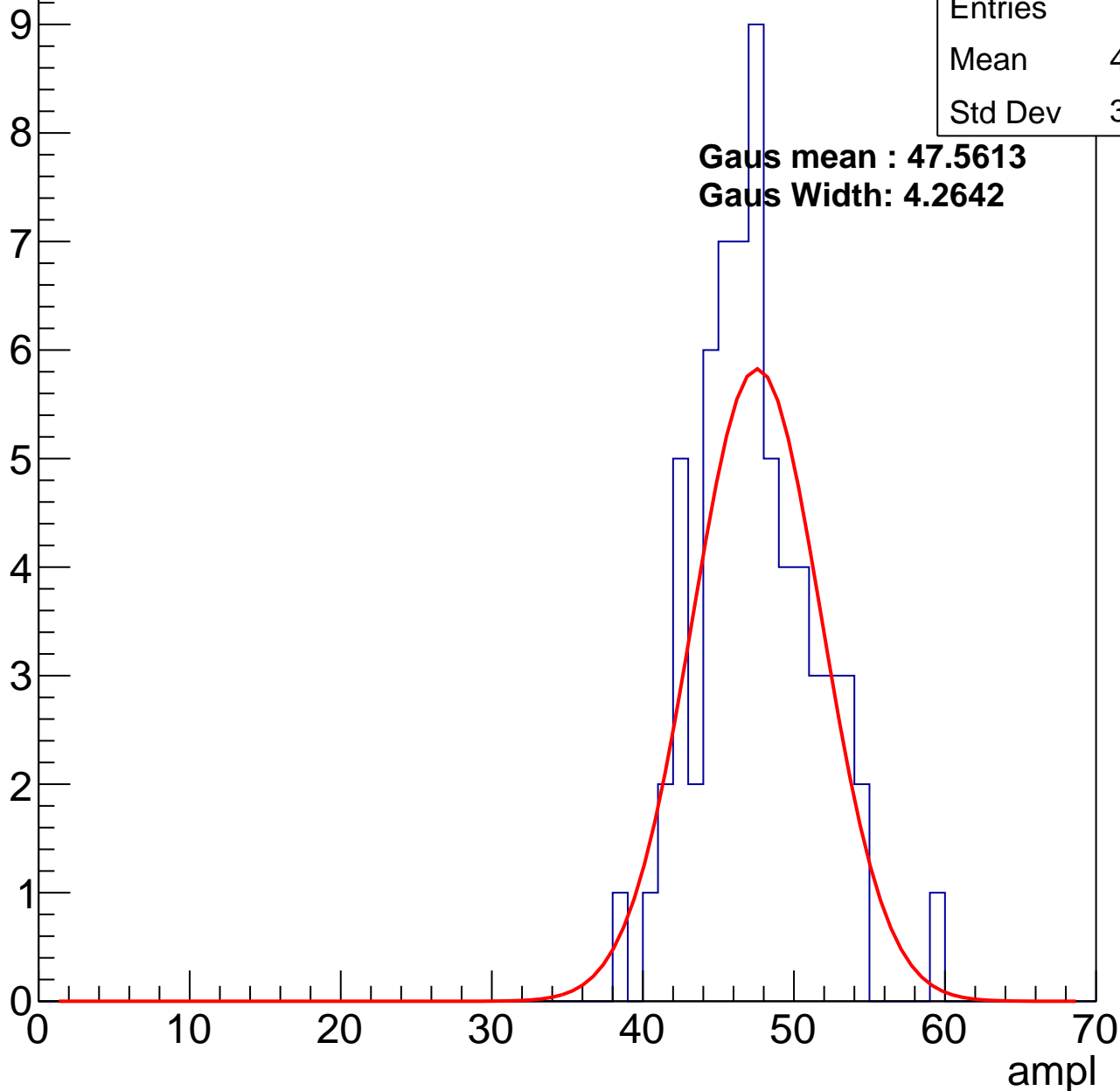
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	46.94
Std Dev	3.878

**Gaus mean : 47.5613**

**Gaus Width: 4.2642**

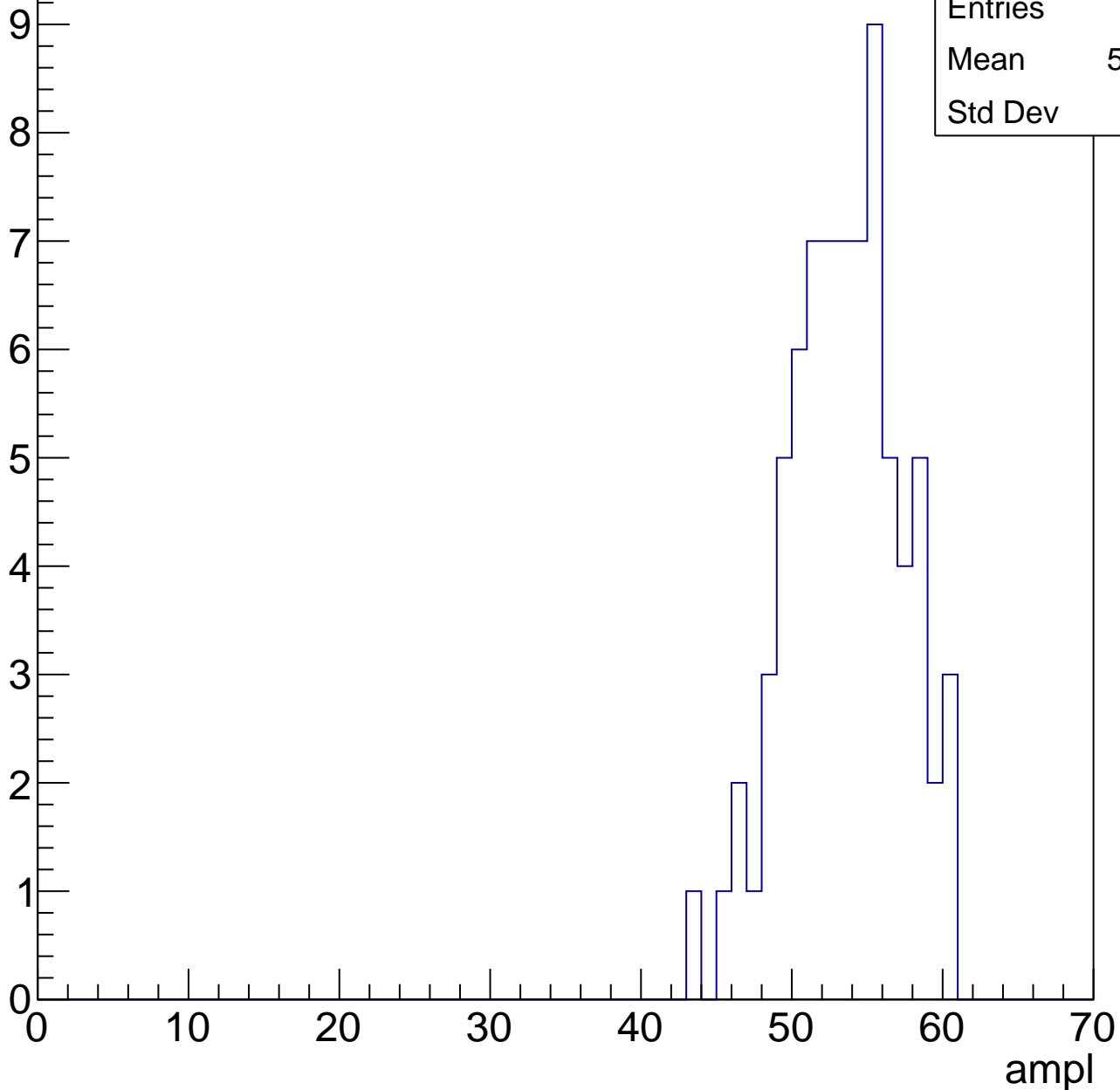


# B0L001S, U21-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	53.03
Std Dev	3.72



# B0L001S, U21-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

7

6

5

4

3

2

1

0

Entries

45

Mean

59.4

Std Dev

2.462

ampl

0

10

20

30

40

50

60

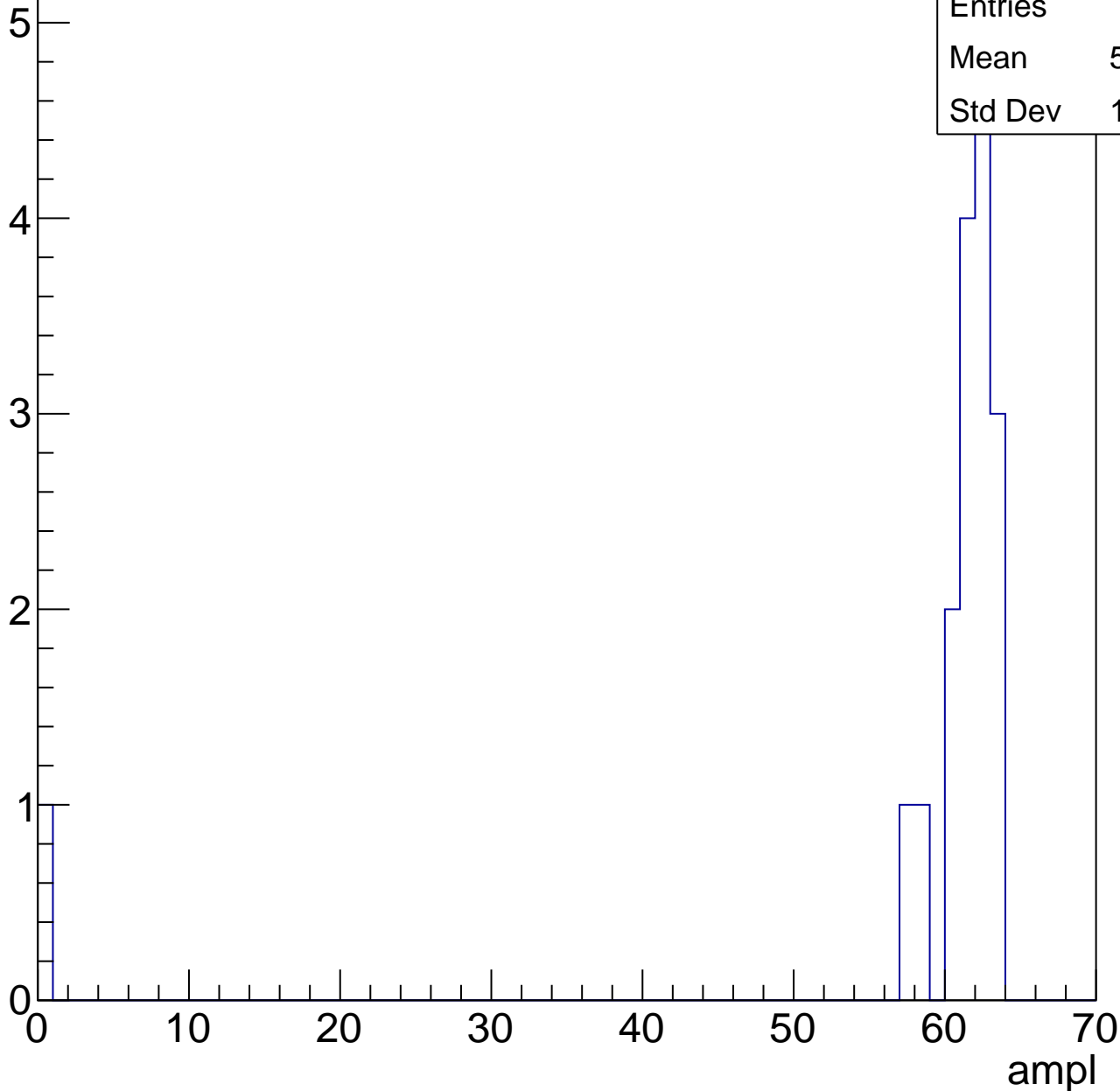
70

# B0L001S, U21-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	17
Mean	57.53
Std Dev	14.47



# B0L001S, U21-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch88, adc0

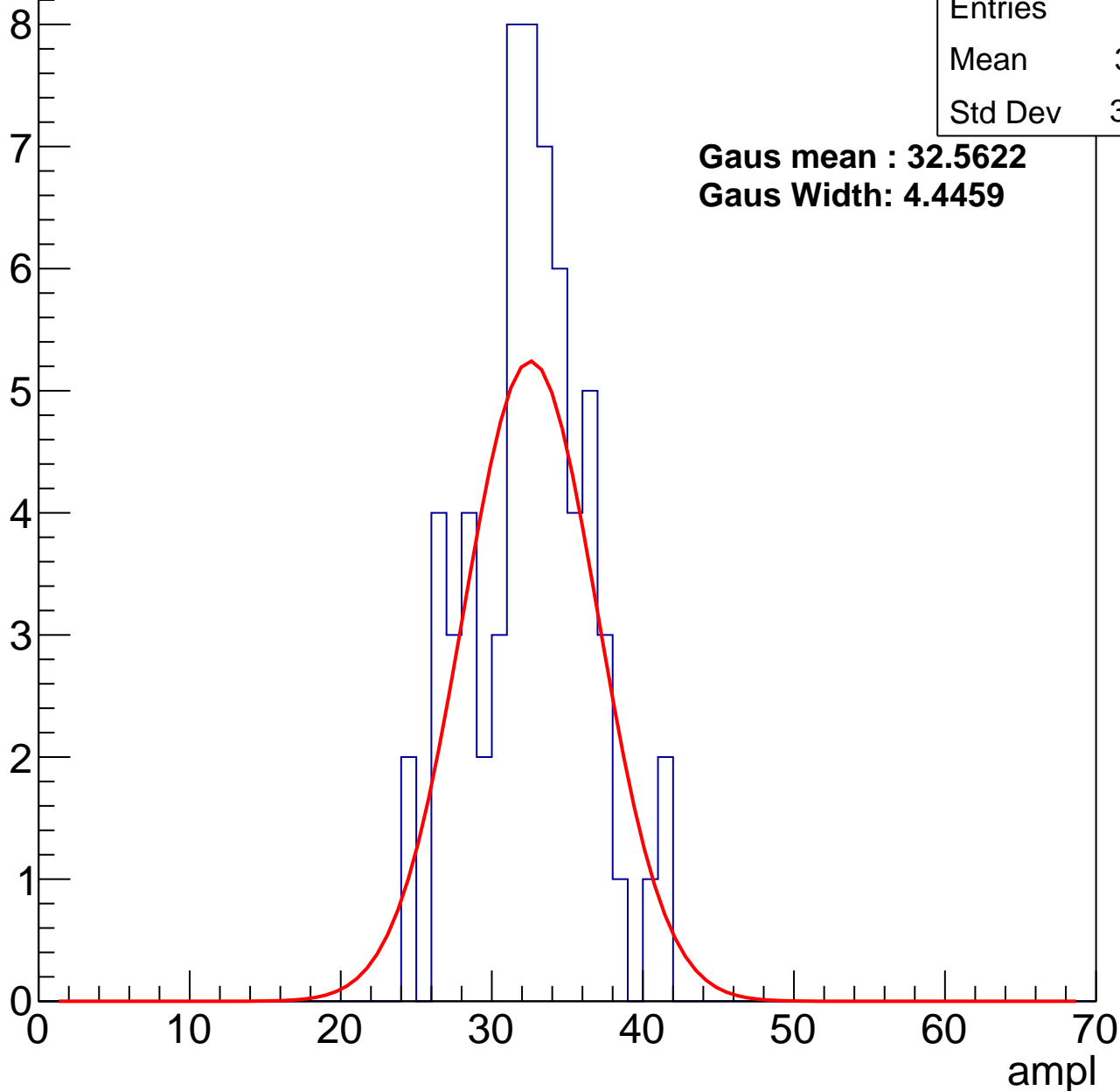
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	32.11
Std Dev	3.847

**Gaus mean : 32.5622**

**Gaus Width: 4.4459**



# B0L001S, U21-ch88, adc1

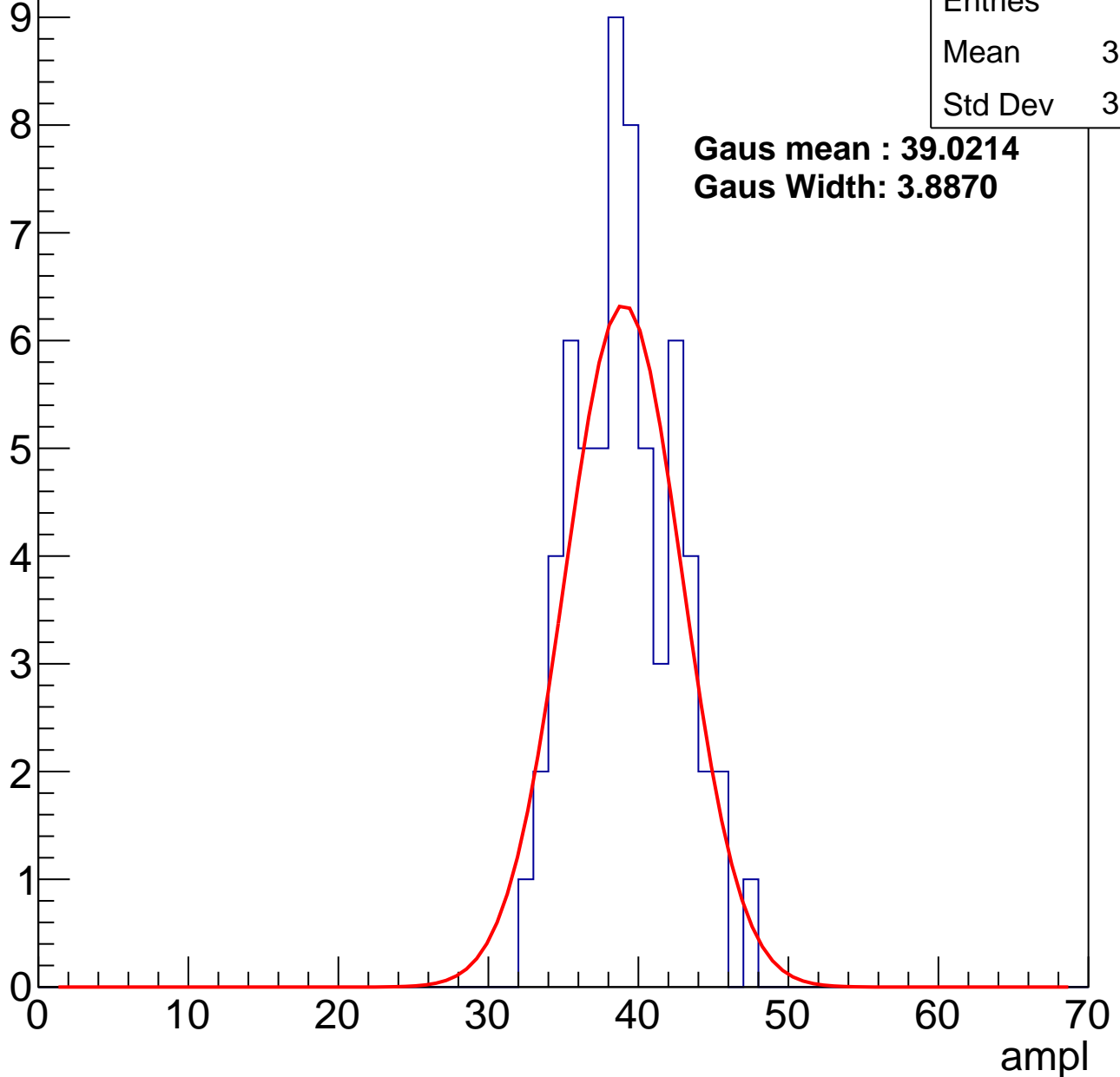
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	38.65
Std Dev	3.344

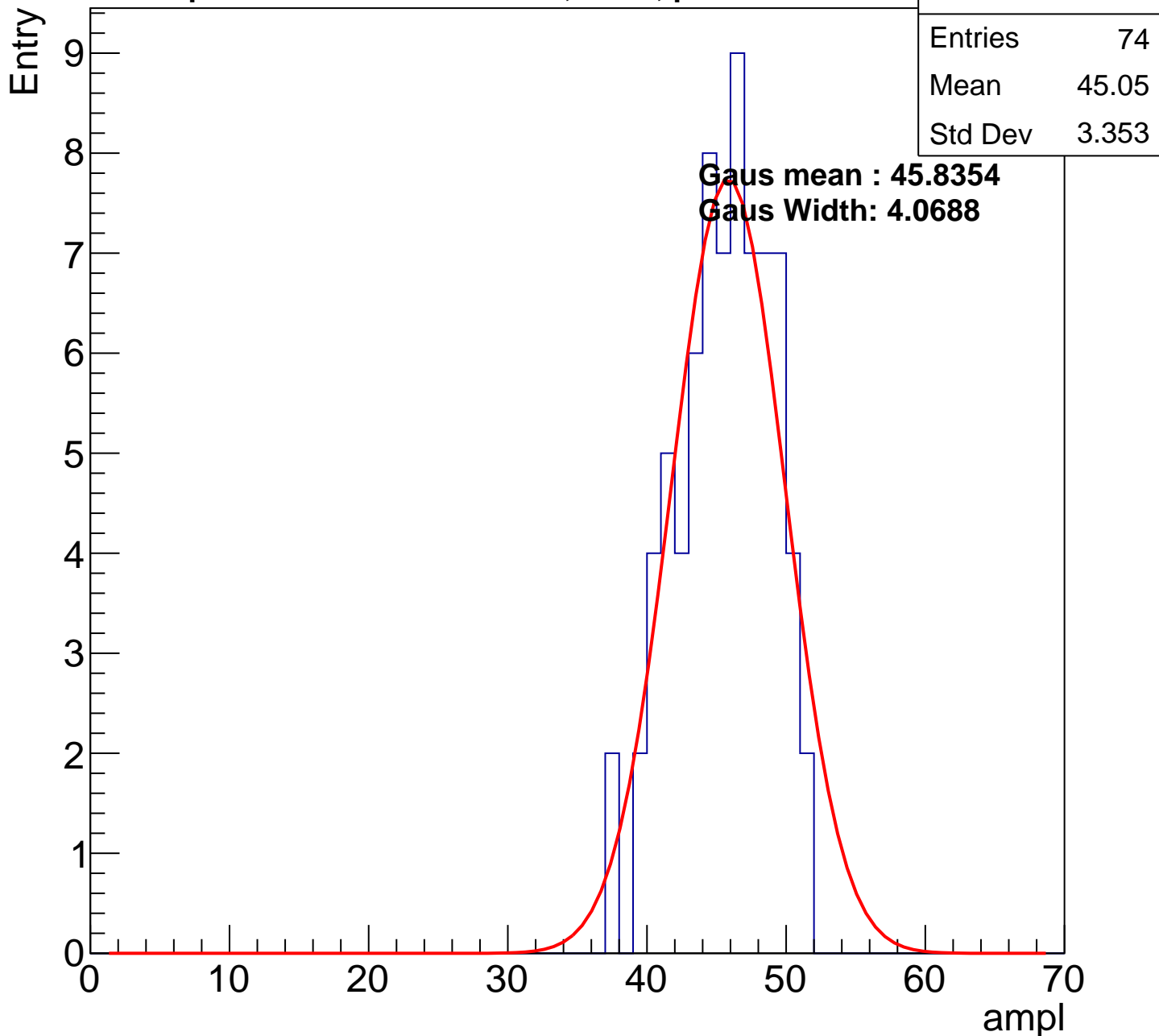
**Gaus mean : 39.0214**

**Gaus Width: 3.8870**



# B0L001S, U21-ch88, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U21-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	56
Mean	52
Std Dev	3.036

Entry

10

8

6

4

2

0

0

10

20

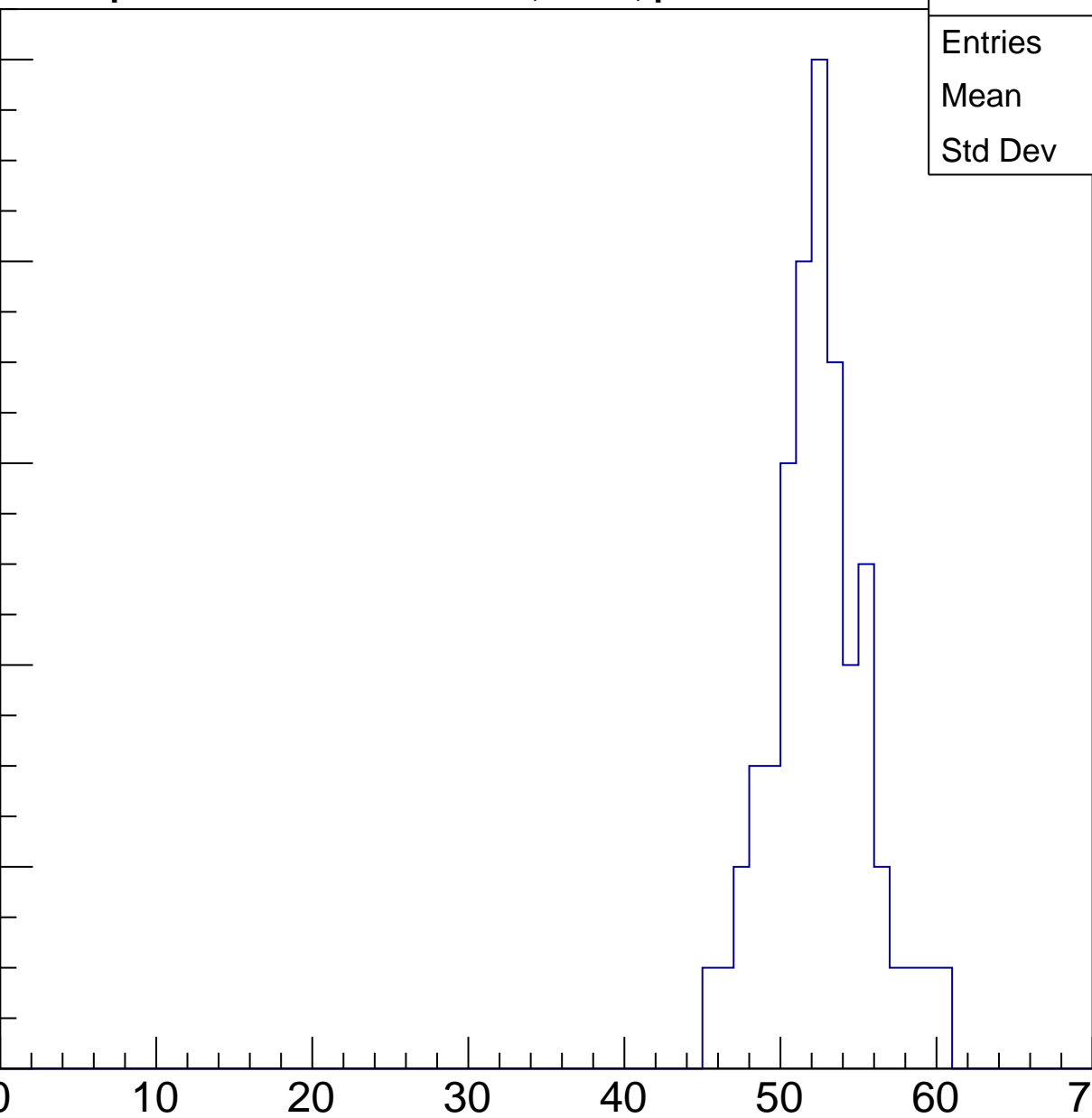
30

40

50

60

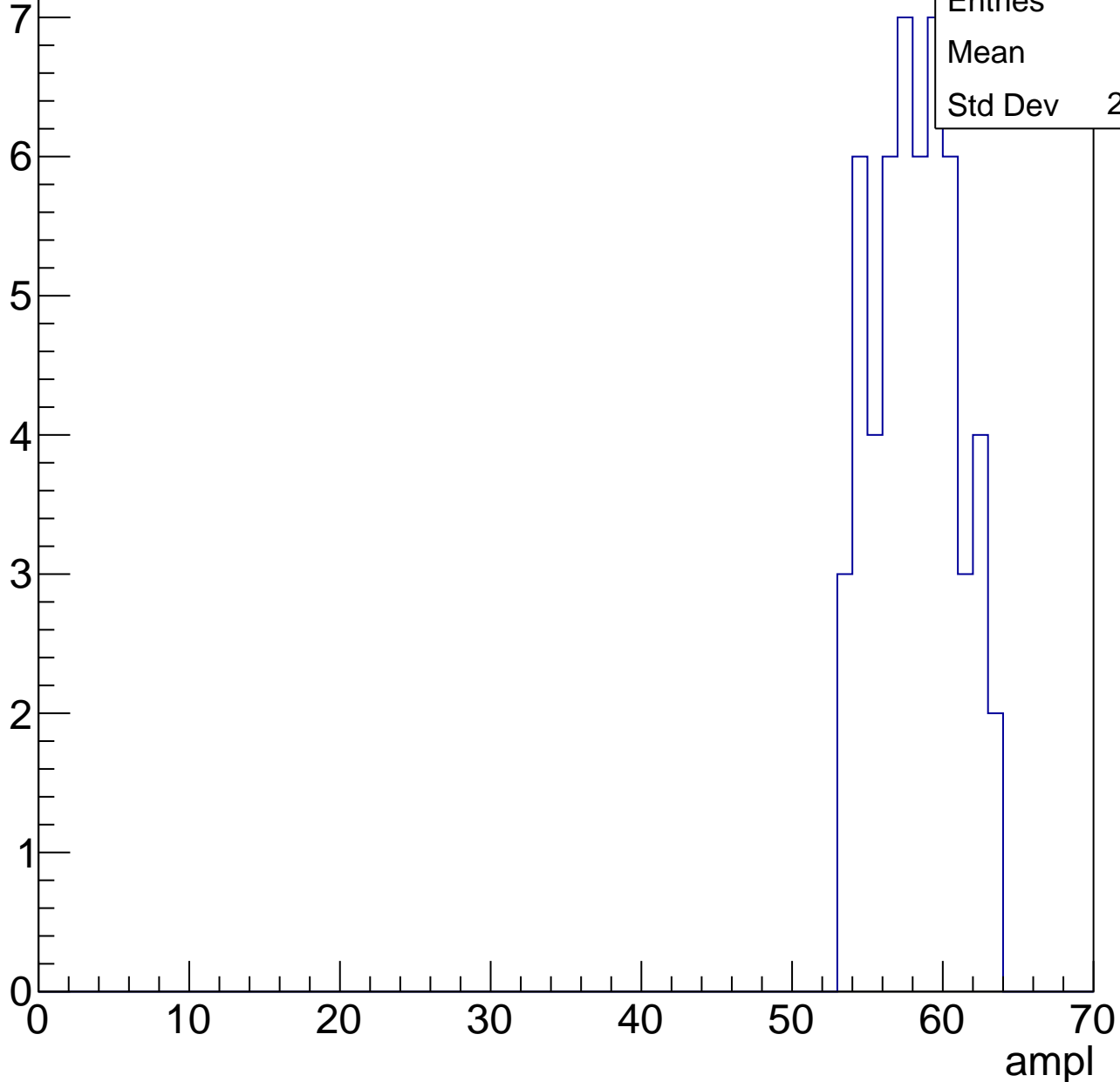
ampl



# B0L001S, U21-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

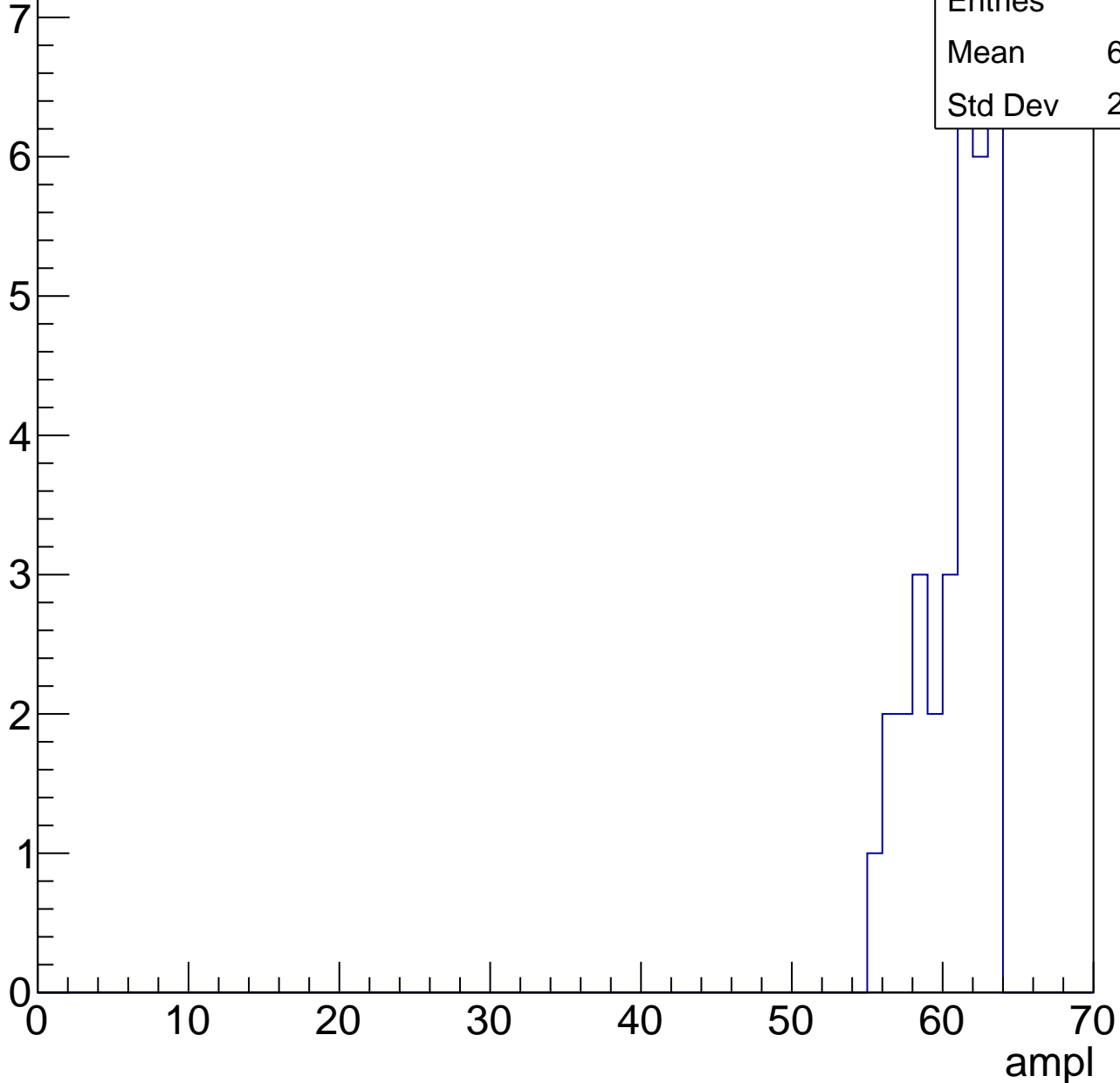


# B0L001S, U21-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	33
Mean	60.39
Std Dev	2.322



# B0L001S, U21-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch89, adc0

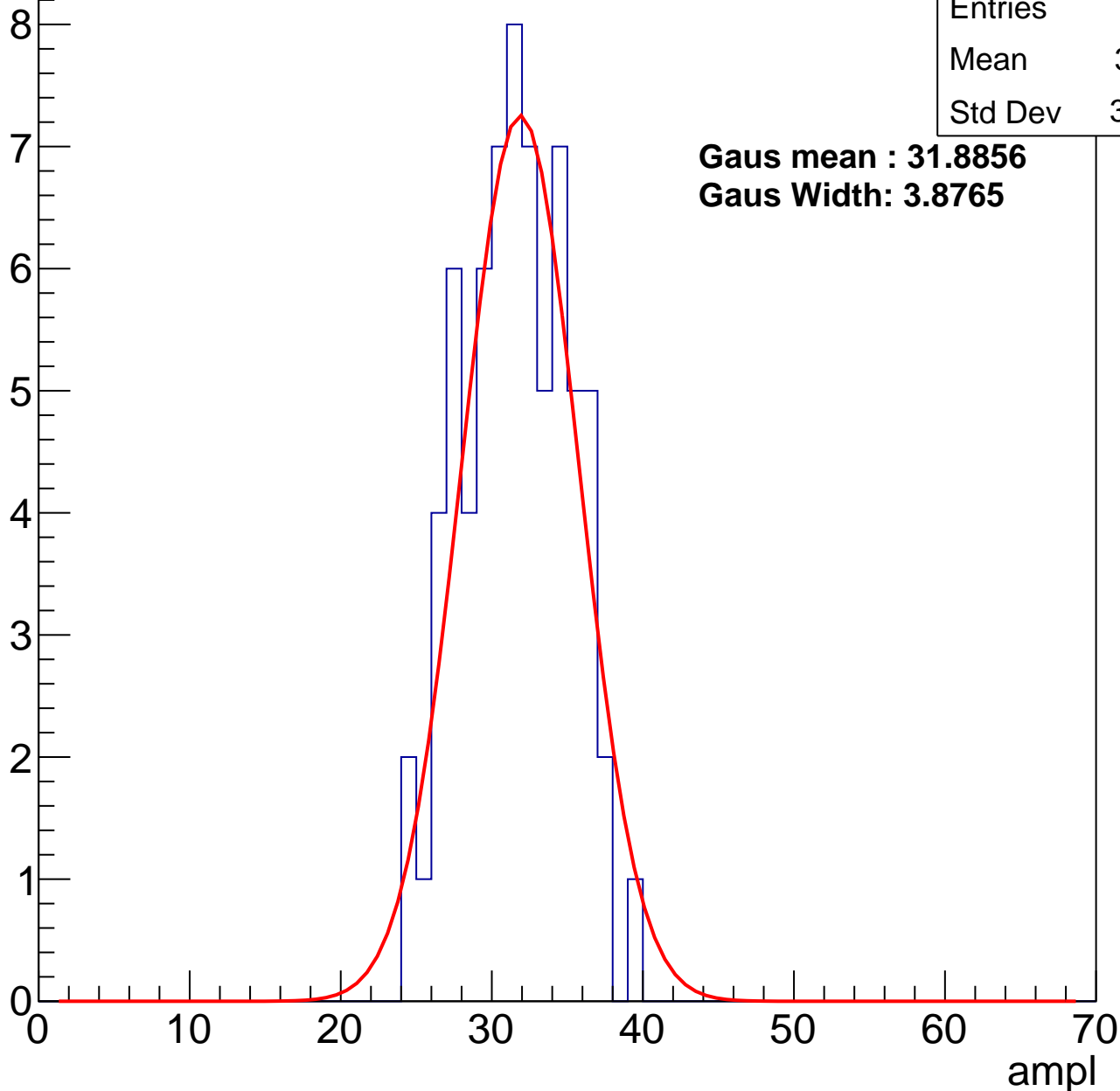
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	31.11
Std Dev	3.437

**Gaus mean : 31.8856**

**Gaus Width: 3.8765**



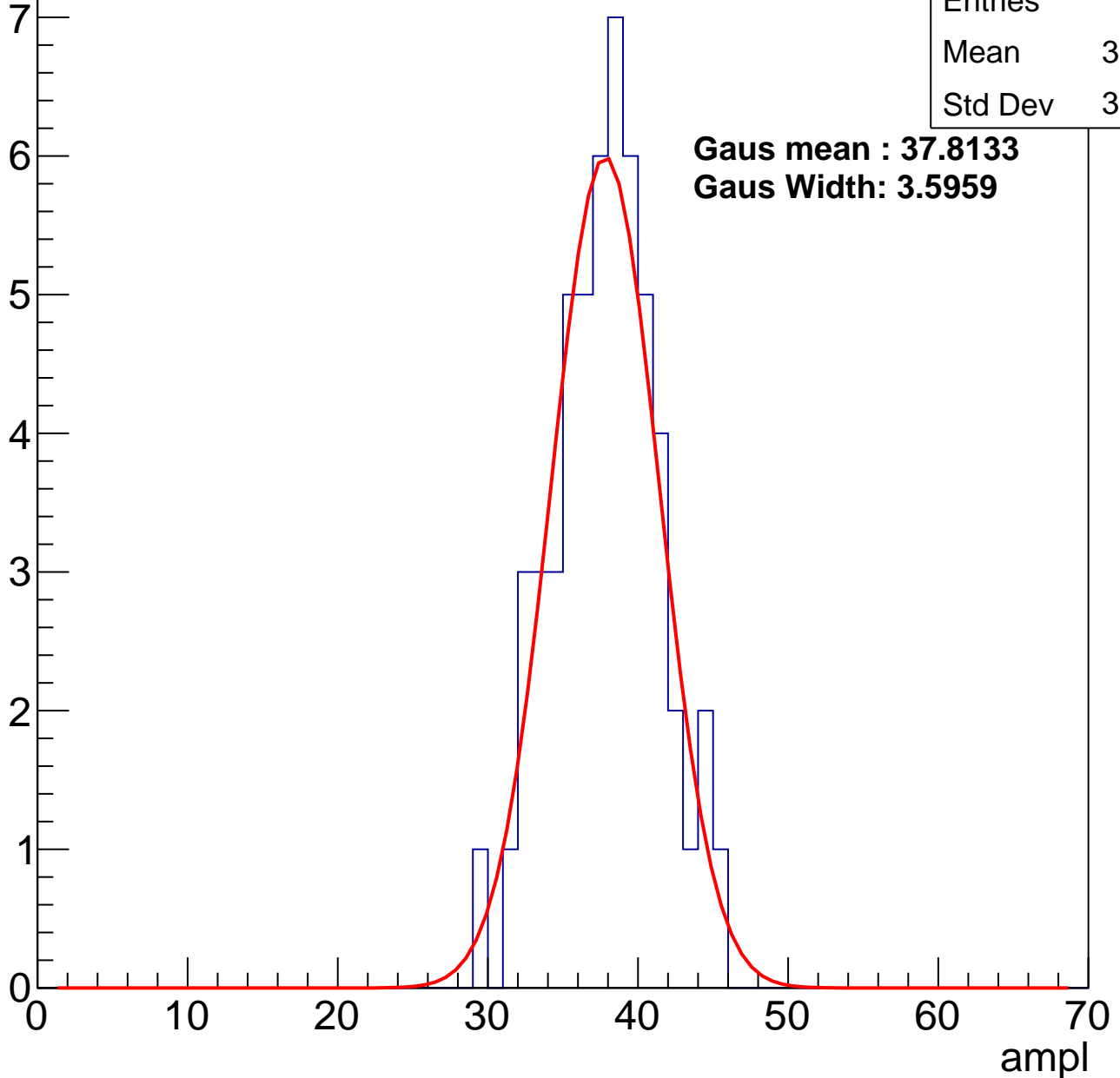
# B0L001S, U21-ch89, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	37.42
Std Dev	3.447

**Gaus mean : 37.8133**  
**Gaus Width: 3.5959**



# B0L001S, U21-ch89, adc2

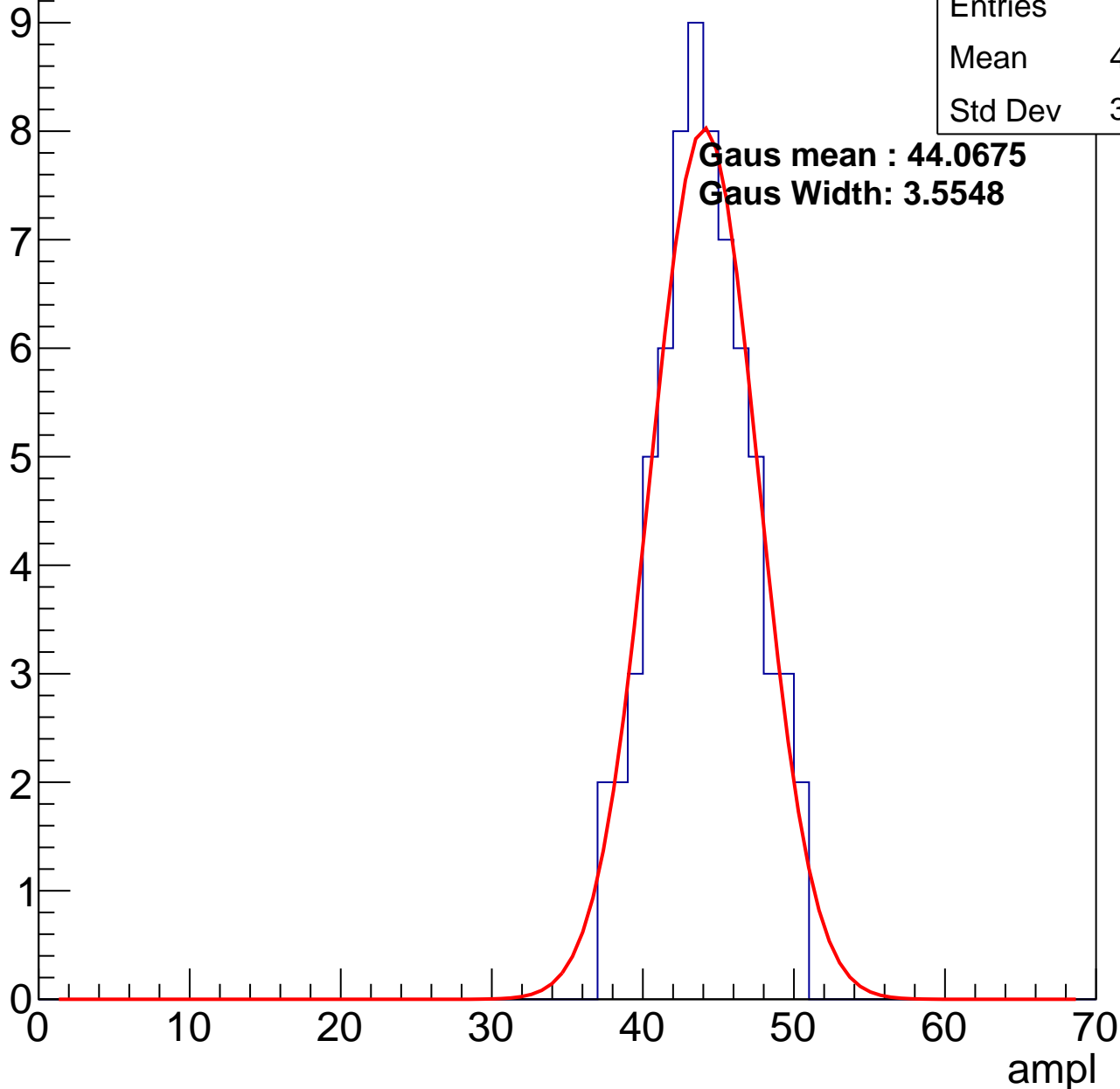
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	43.55
Std Dev	3.133

**Gaus mean : 44.0675**

**Gaus Width: 3.5548**

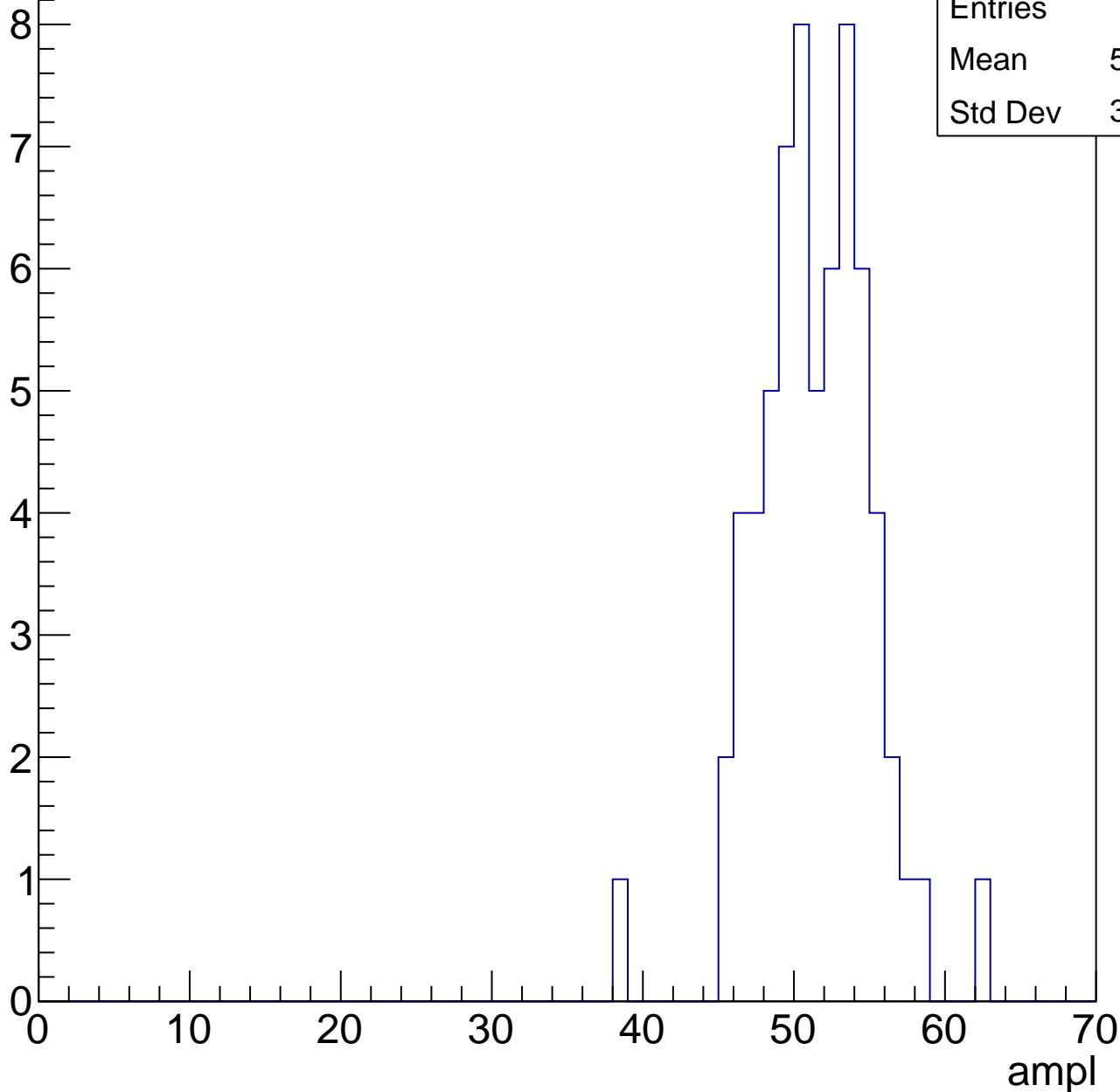


# B0L001S, U21-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	50.88
Std Dev	3.715

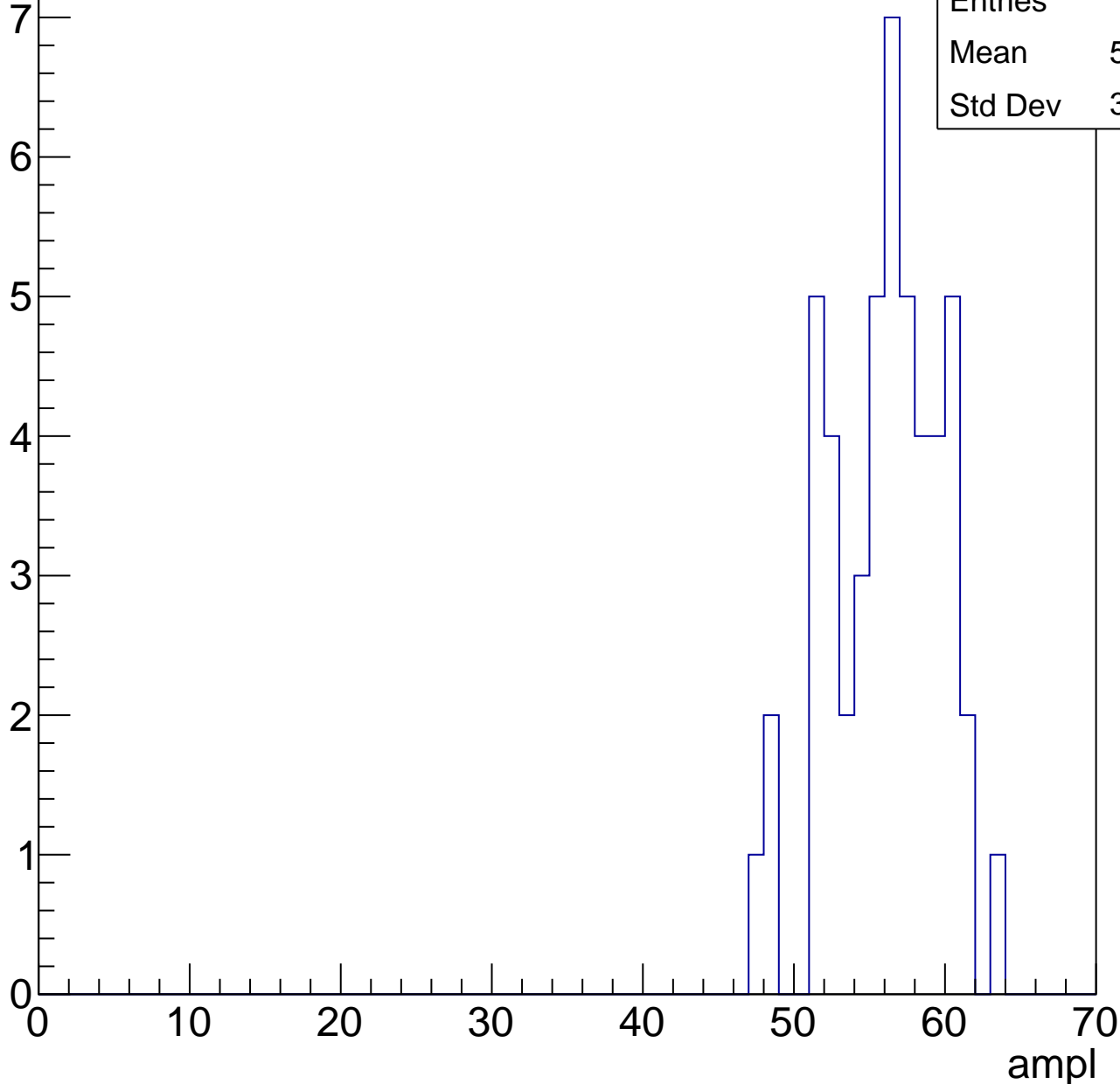


# B0L001S, U21-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	55.58
Std Dev	3.634



# B0L001S, U21-ch89, adc5

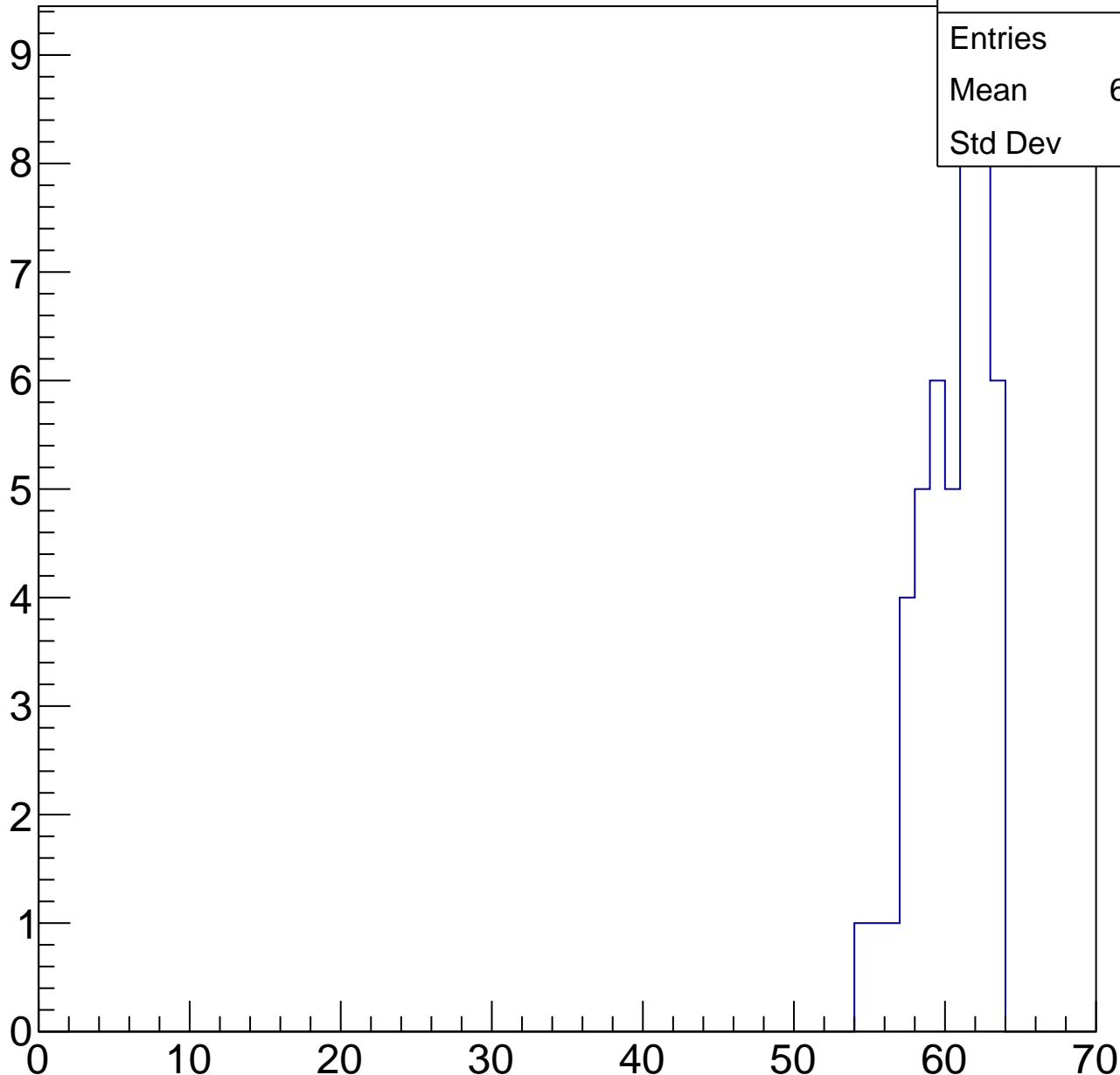
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	46
Mean	60.02
Std Dev	2.27

ampl



# B0L001S, U21-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



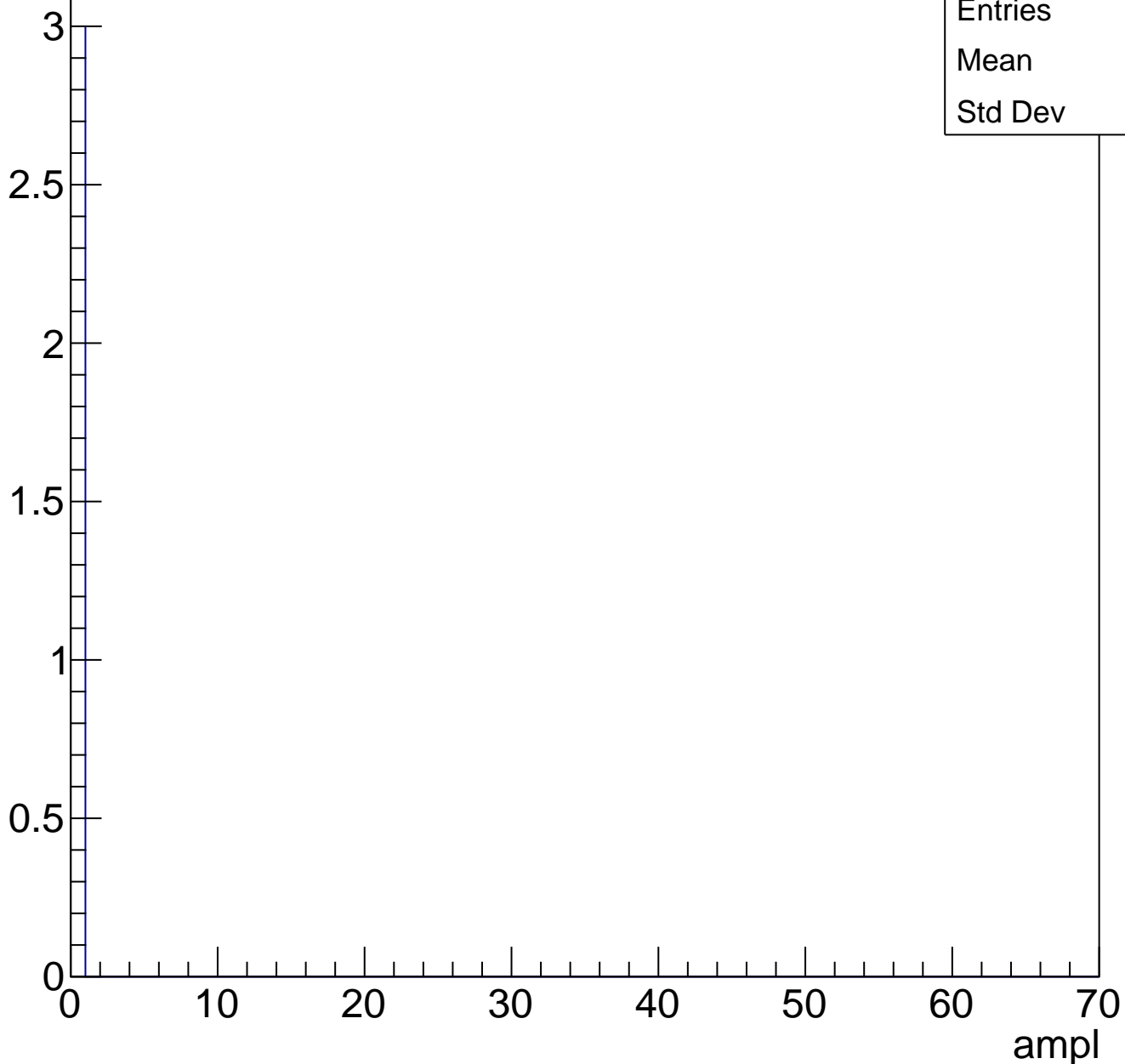
Entries	3
Mean	63
Std Dev	0



# B0L001S, U21-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	0
Std Dev	0

# B0L001S, U21-ch90, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	72
Mean	31.36
Std Dev	3.177

**Gaus mean : 31.9591**

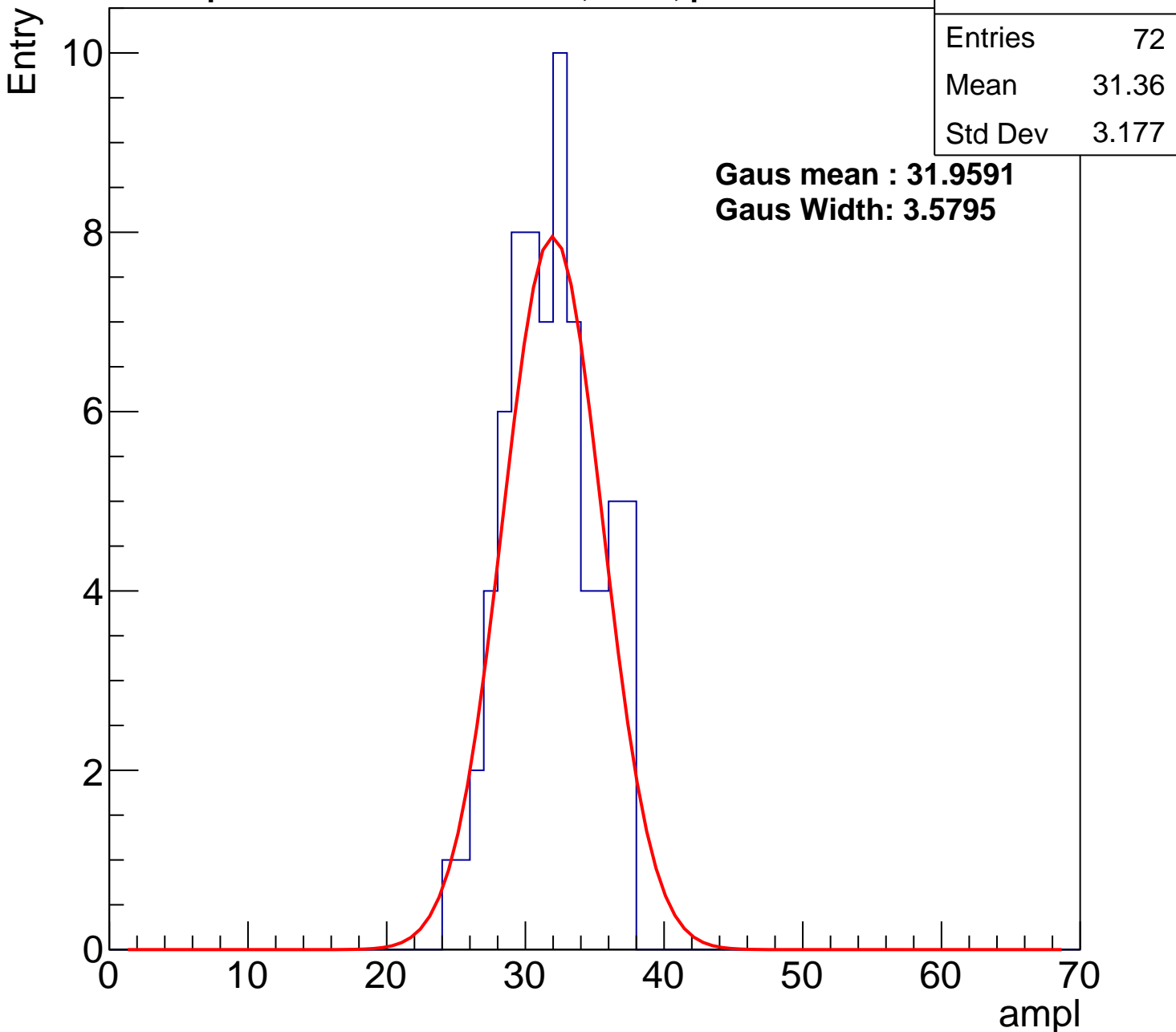
**Gaus Width: 3.5795**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U21-ch90, adc1

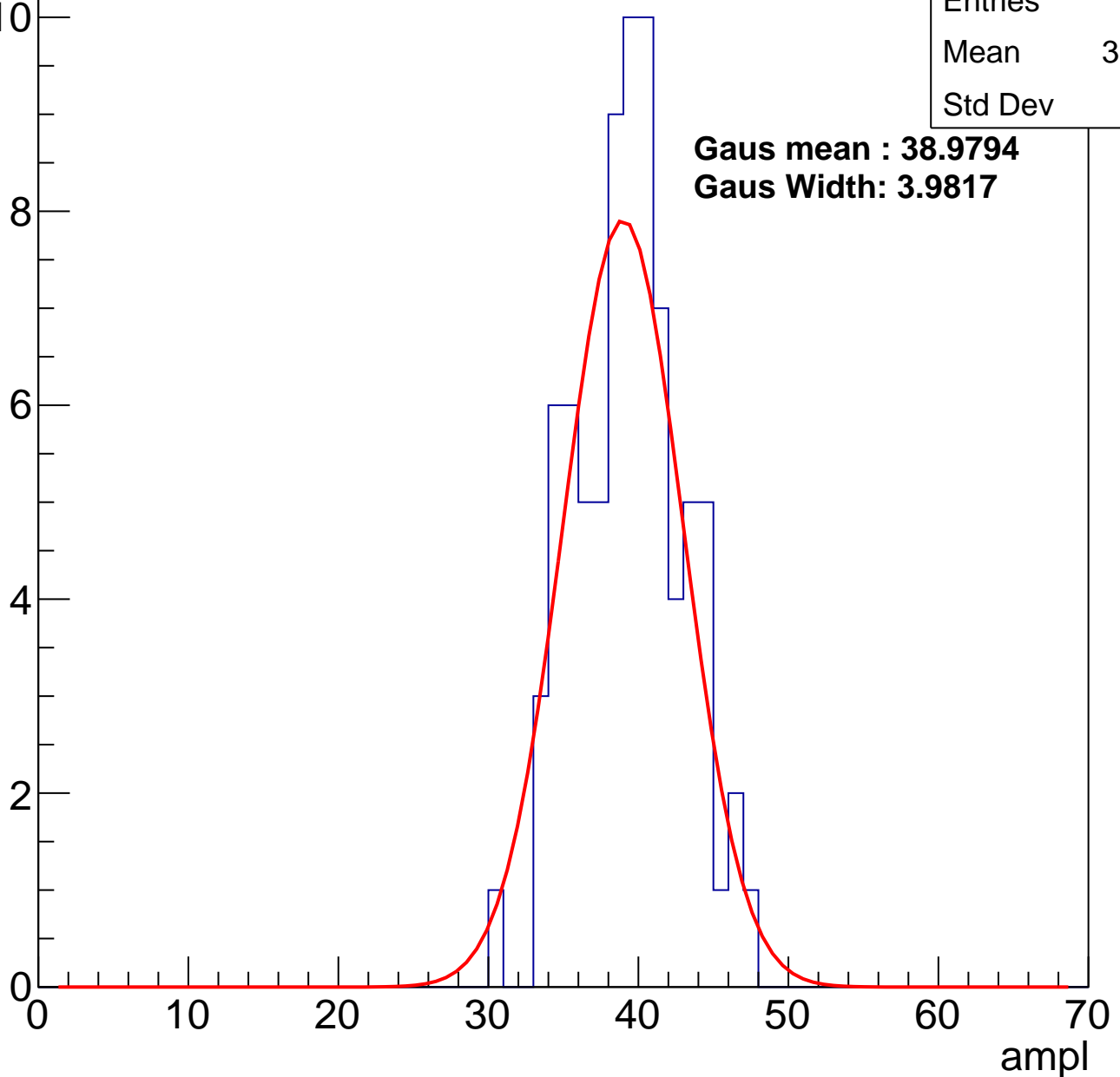
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	80
Mean	38.92
Std Dev	3.51

**Gaus mean : 38.9794**

**Gaus Width: 3.9817**



# B0L001S, U21-ch90, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	73
Mean	46.63
Std Dev	3.406

**Gaus mean : 46.4668**

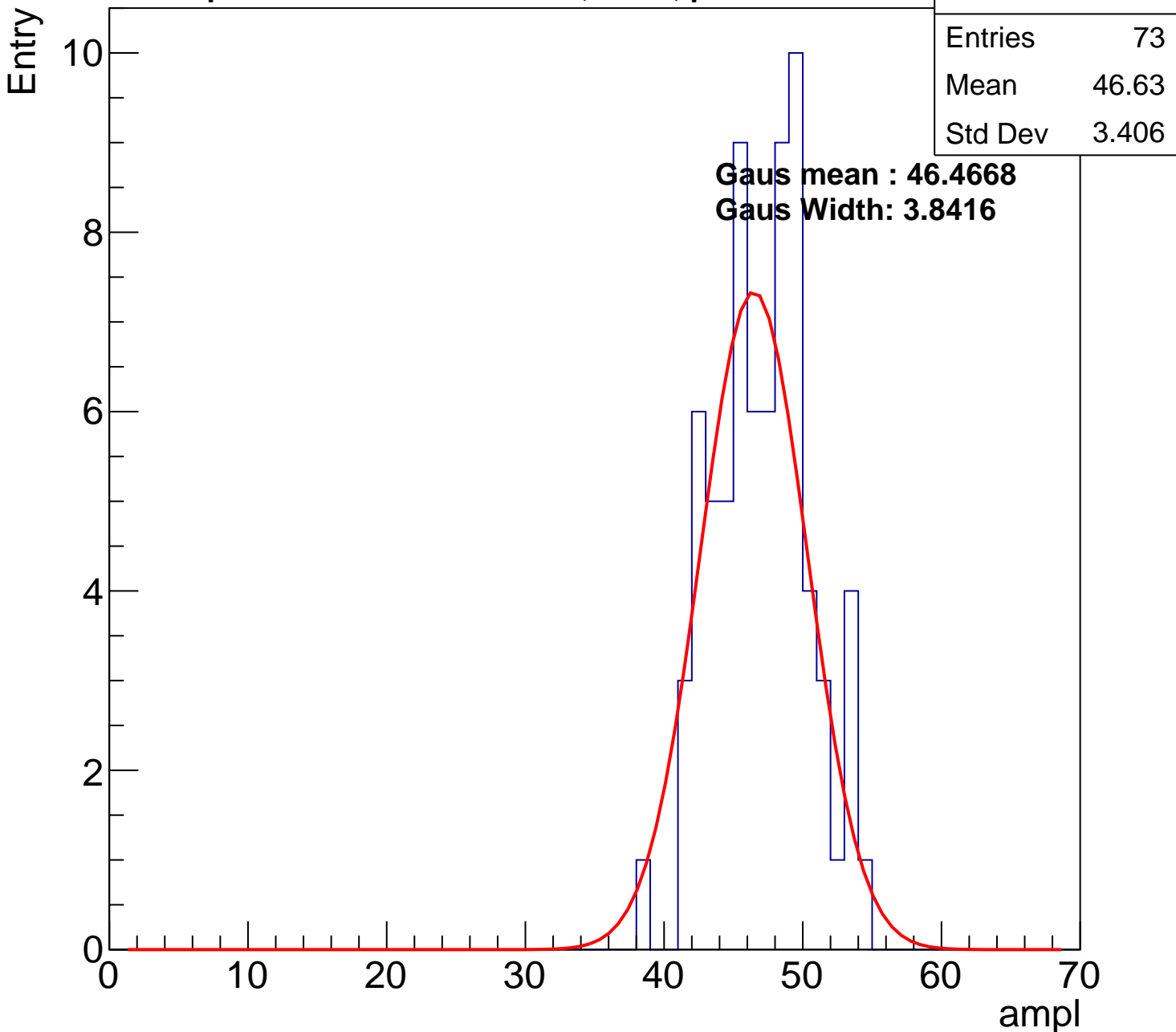
**Gaus Width: 3.8416**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

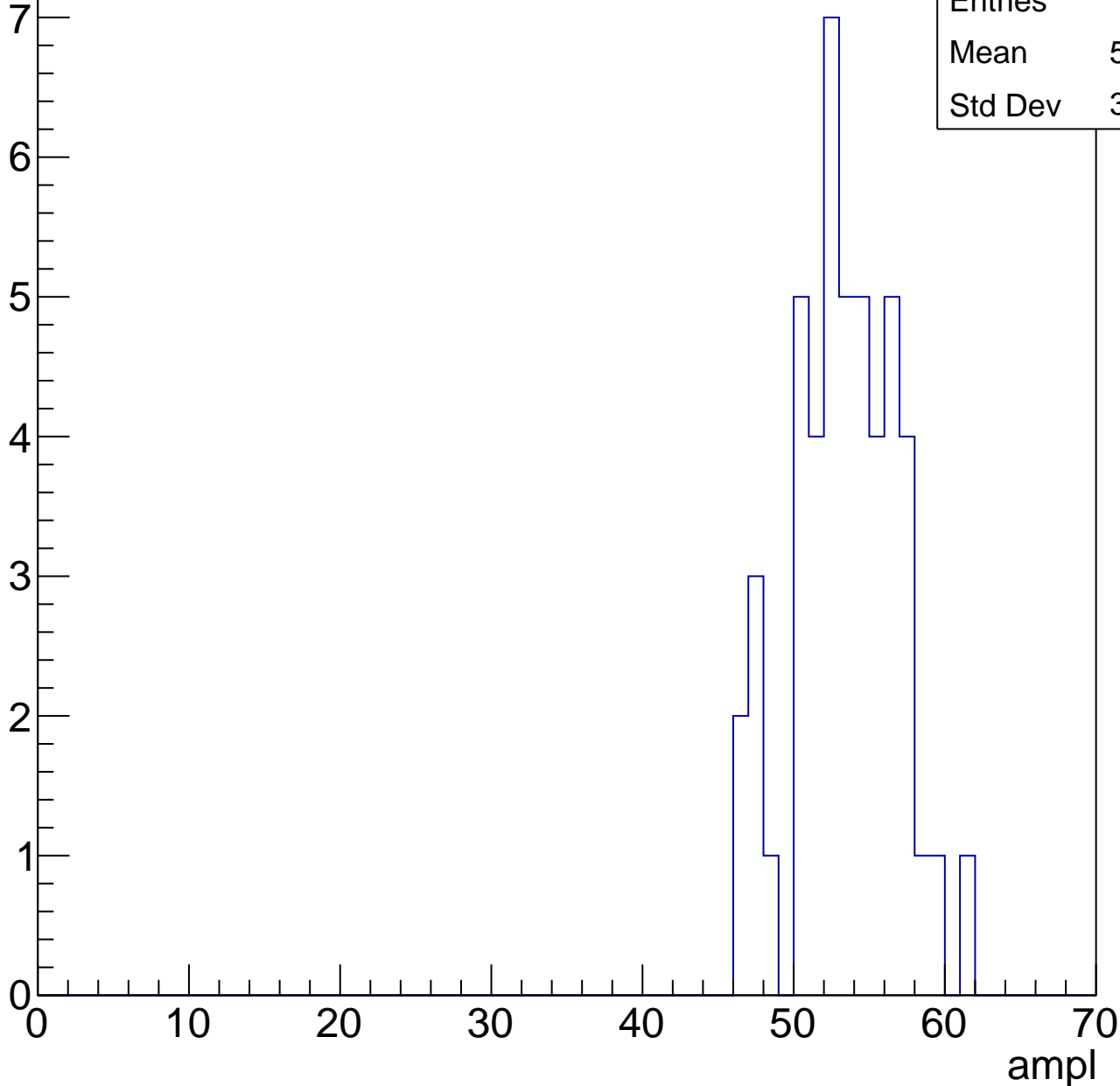


# B0L001S, U21-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	52.92
Std Dev	3.396

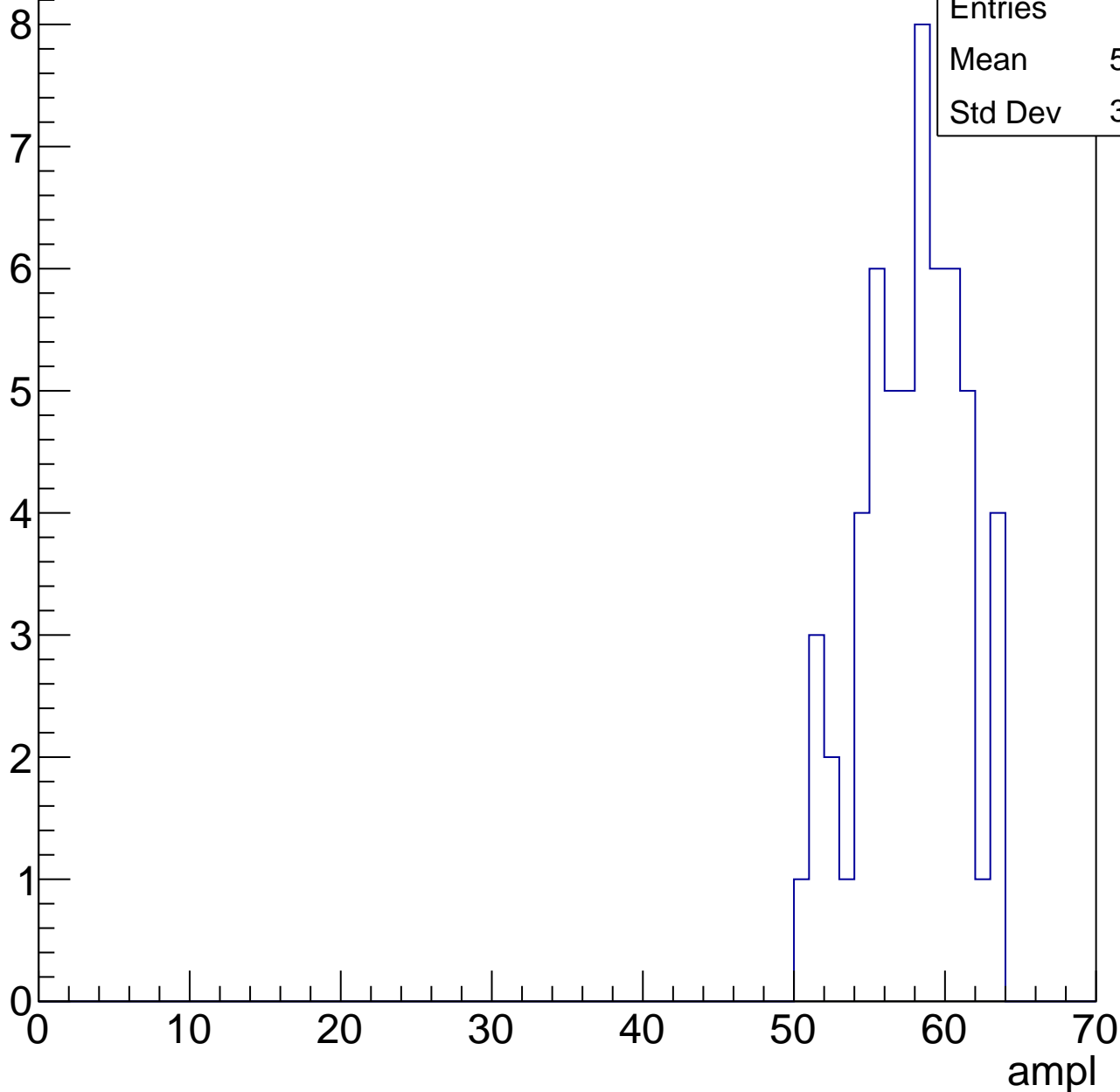


# B0L001S, U21-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	57.33
Std Dev	3.289

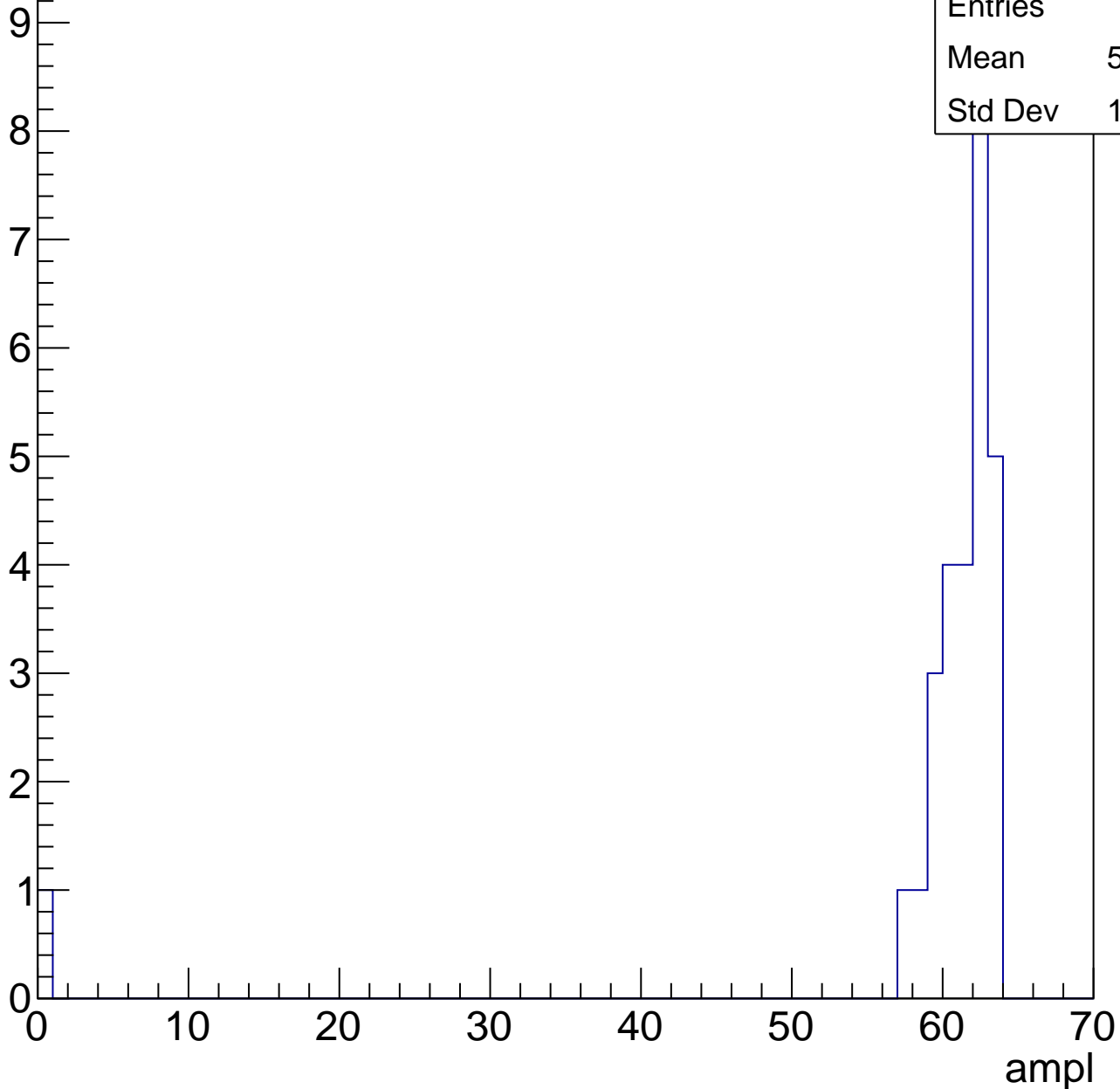


# B0L001S, U21-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	28
Mean	58.89
Std Dev	11.44



# B0L001S, U21-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U21-ch91, adc0

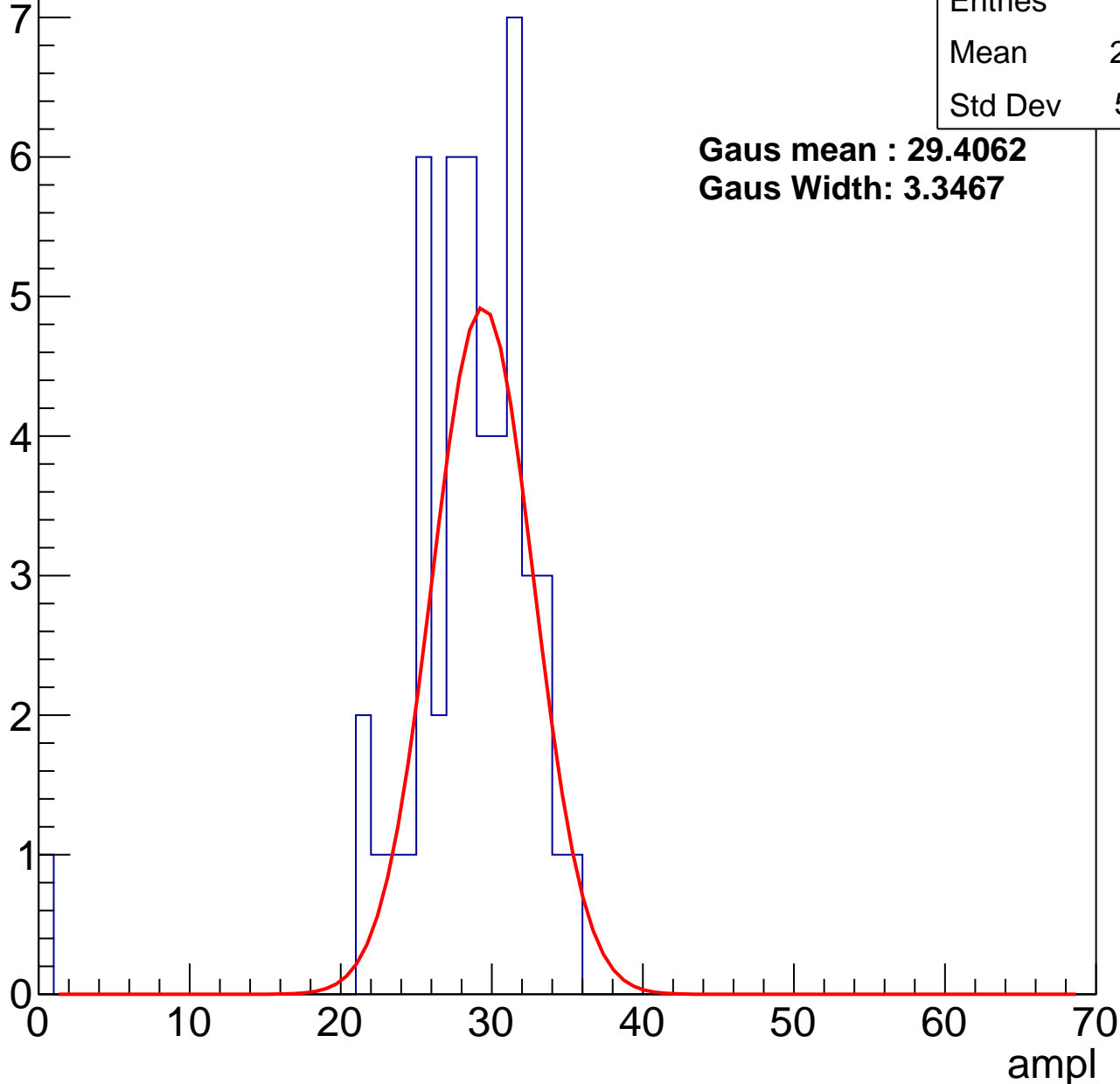
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	27.76
Std Dev	5.181

**Gaus mean : 29.4062**

**Gaus Width: 3.3467**



# B0L001S, U21-ch91, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	89
Mean	35.9
Std Dev	3.687

**Gaus mean : 36.0428**

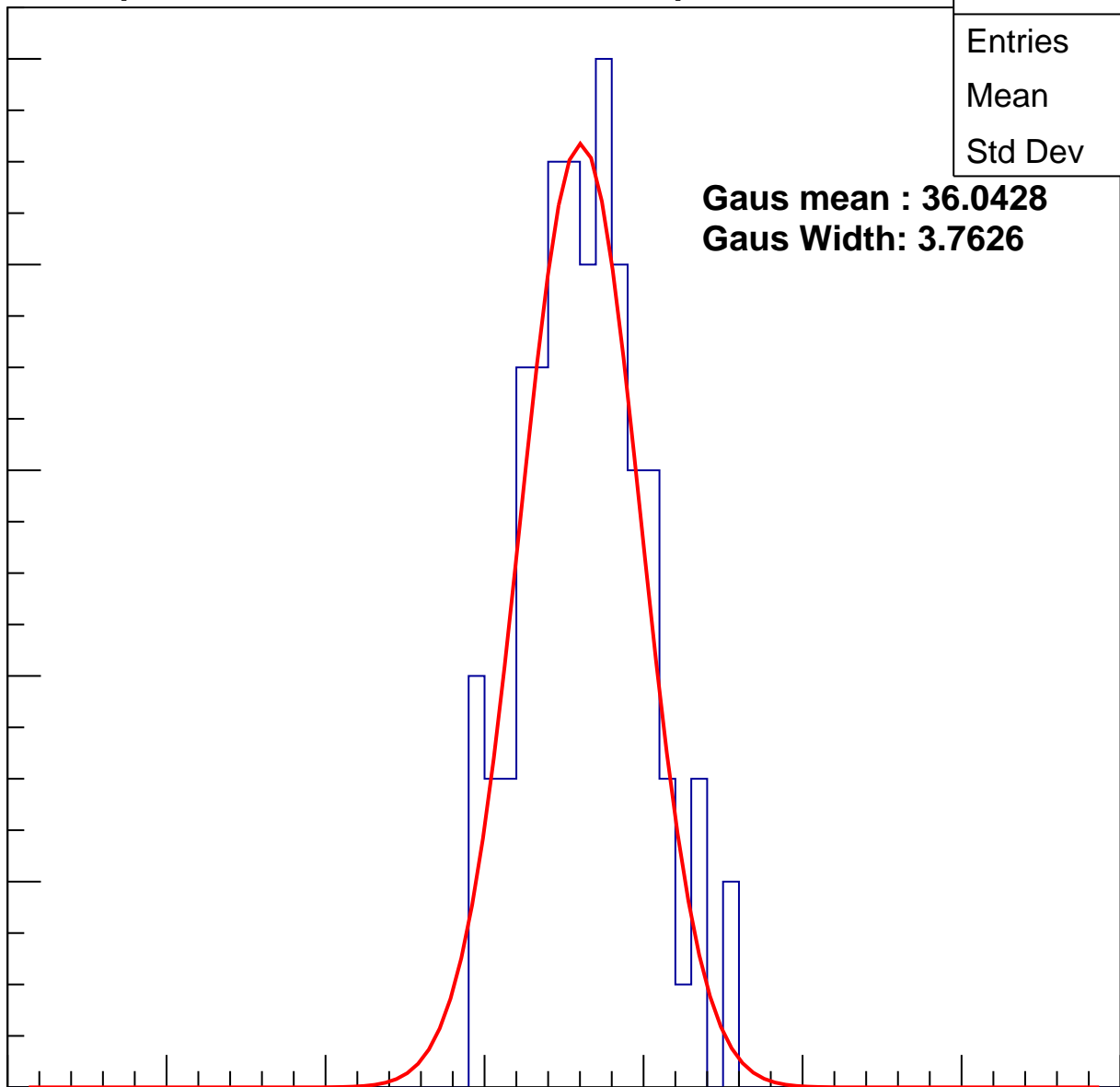
**Gaus Width: 3.7626**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U21-ch91, adc2

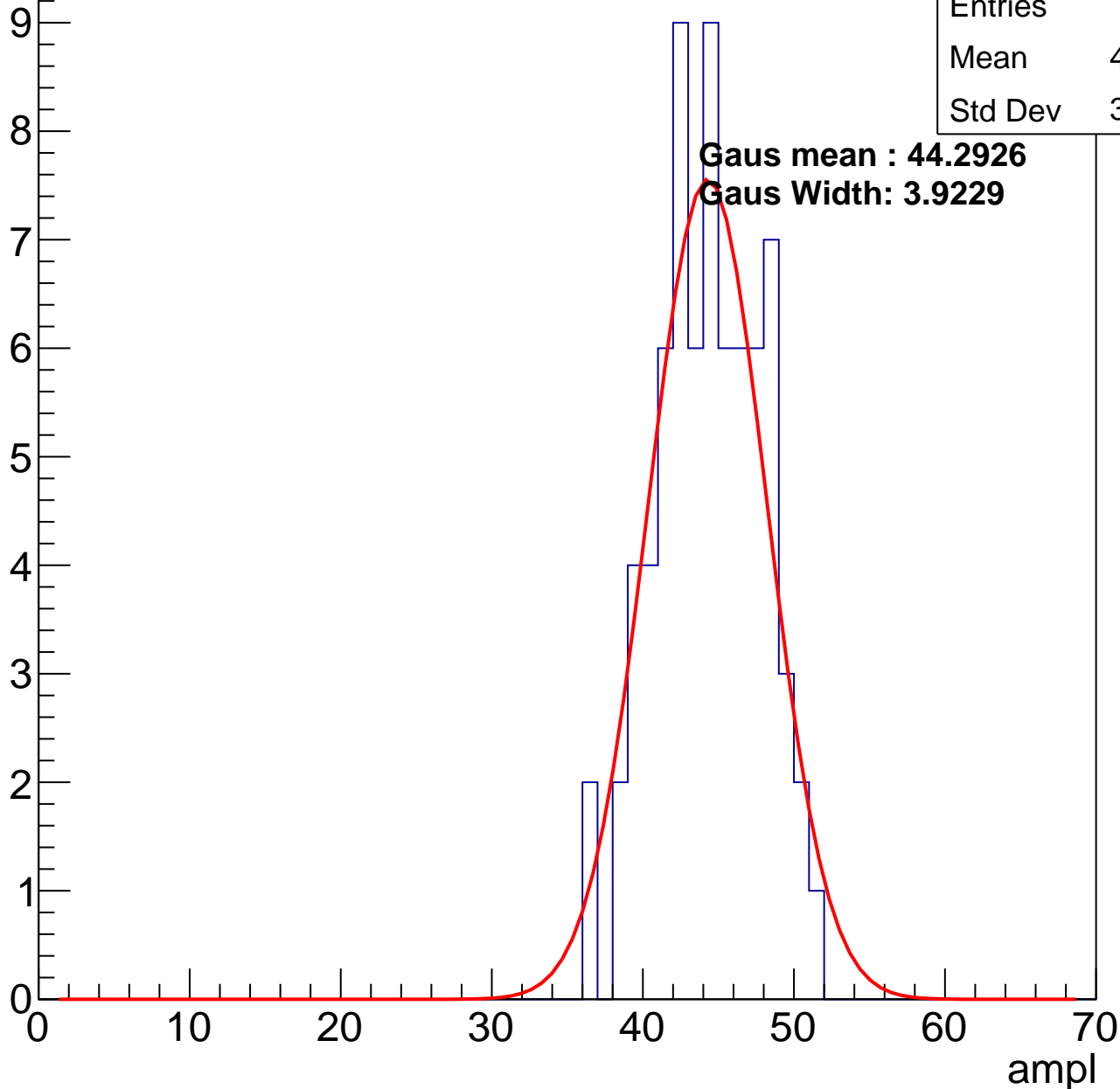
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	43.89
Std Dev	3.415

**Gaus mean : 44.2926**

**Gaus Width: 3.9229**

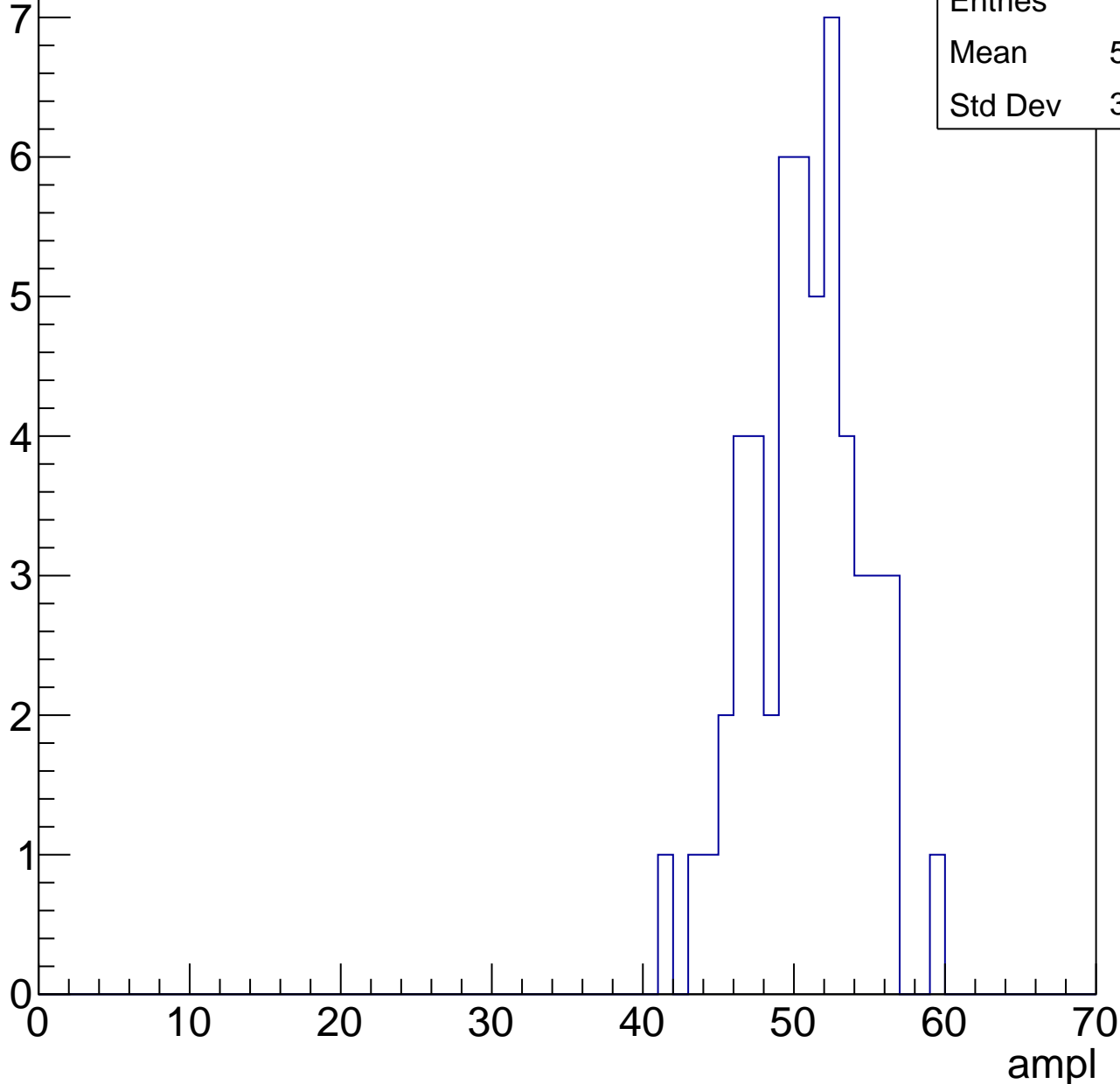


# B0L001S, U21-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	50.28
Std Dev	3.652

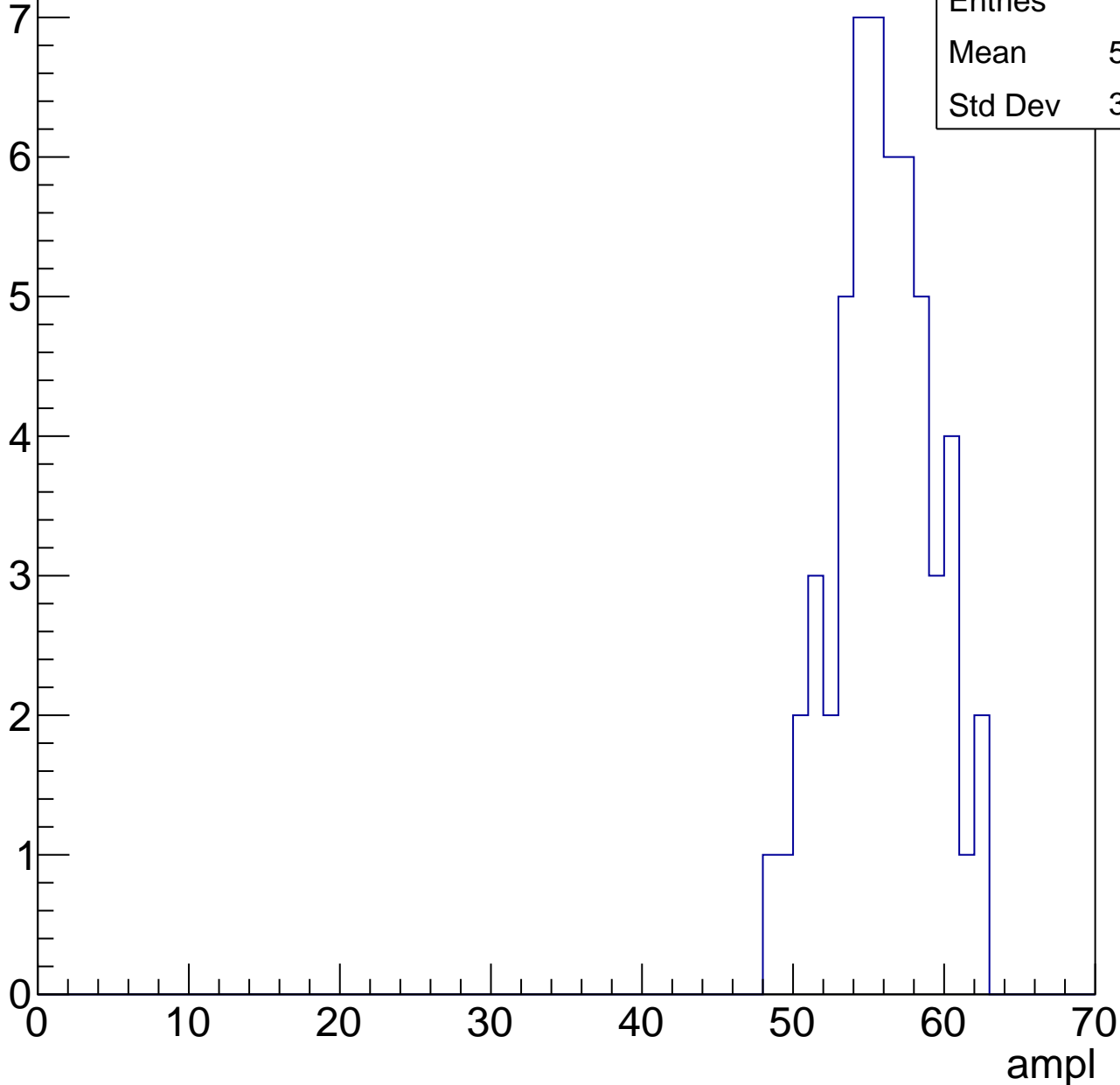


# B0L001S, U21-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	55.49
Std Dev	3.224

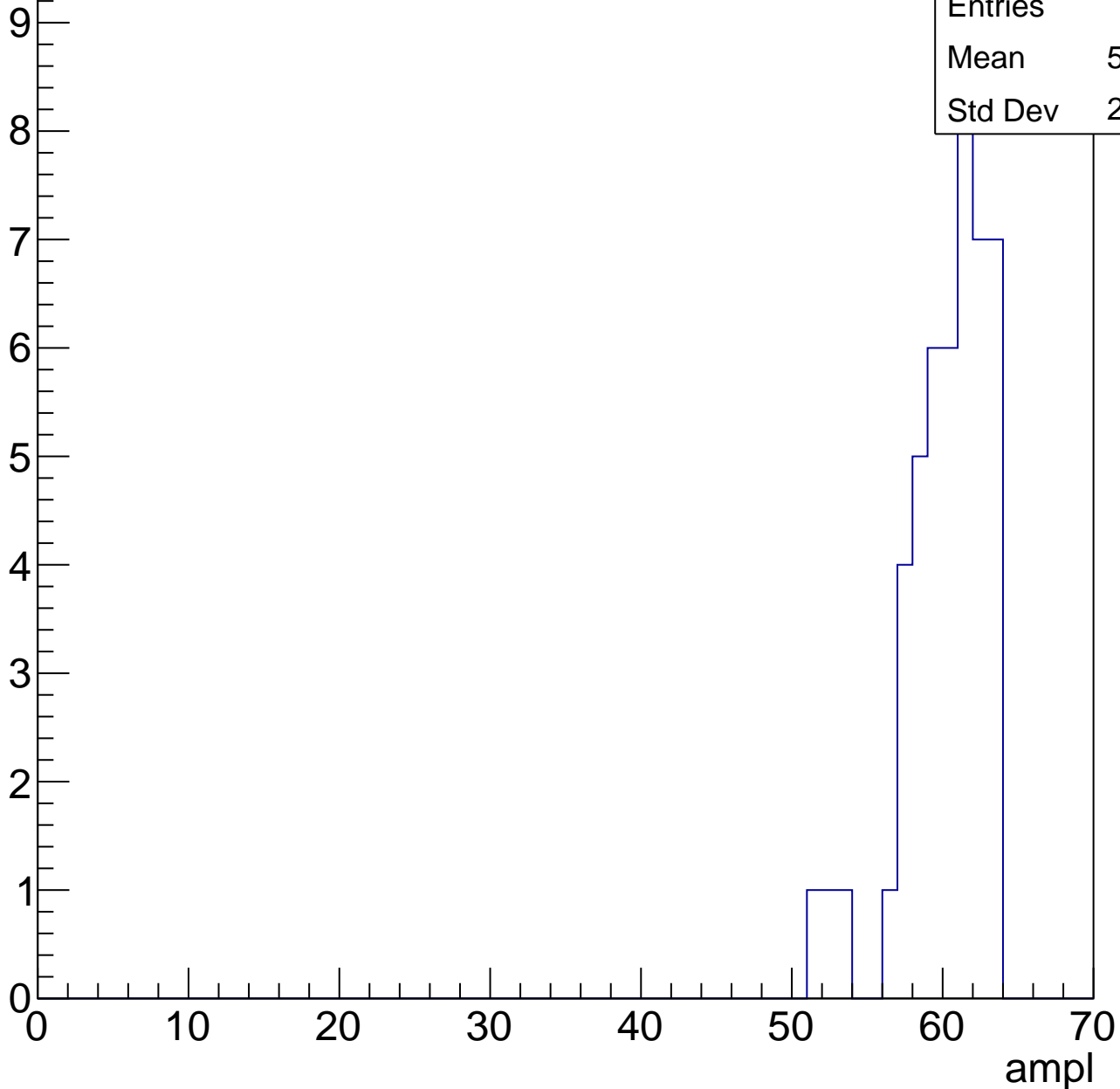


# B0L001S, U21-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	59.75
Std Dev	2.773



# B0L001S, U21-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch92, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	68
Mean	29.41
Std Dev	3.695

**Gaus mean : 29.9491**

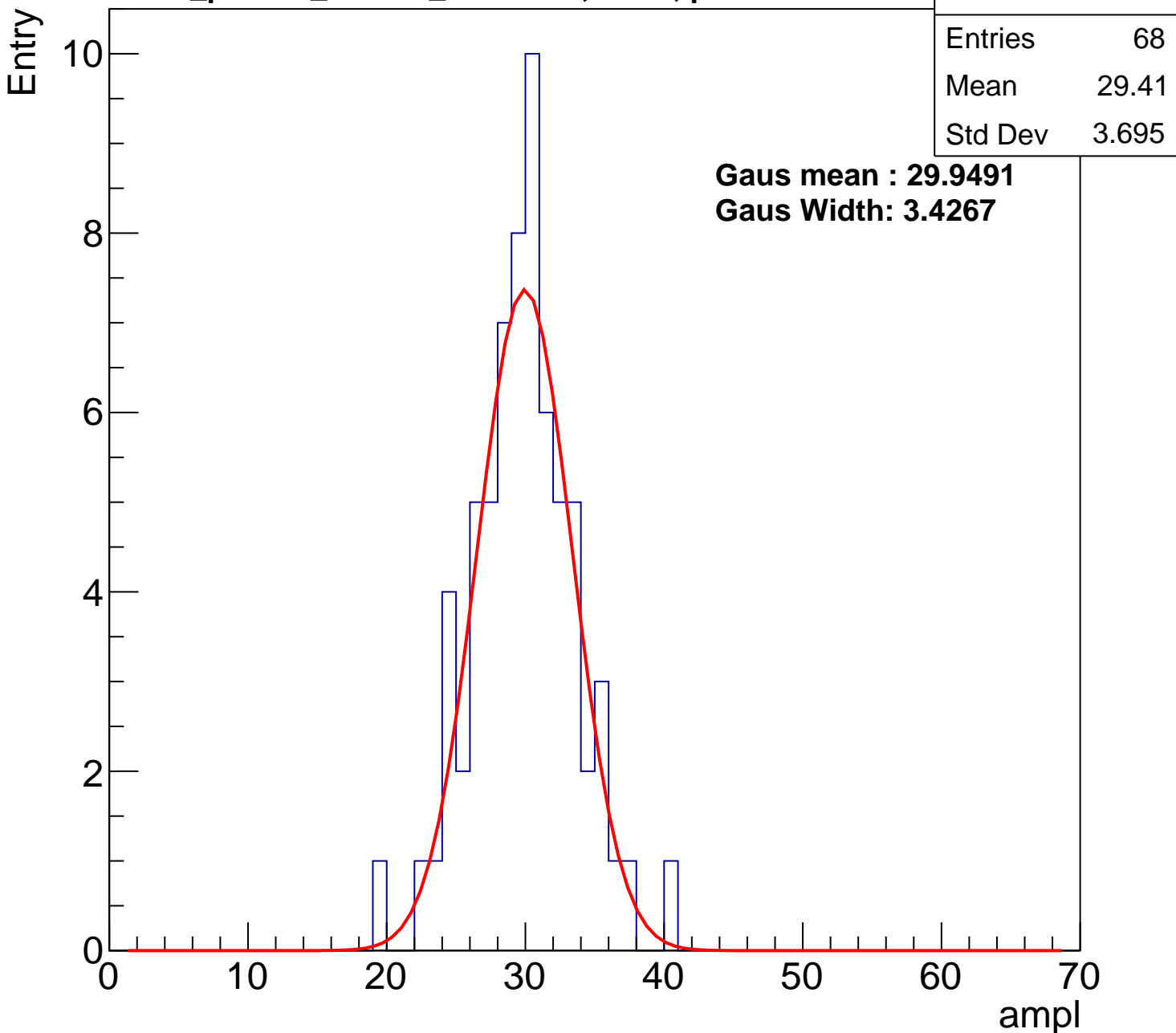
**Gaus Width: 3.4267**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U21-ch92, adc1

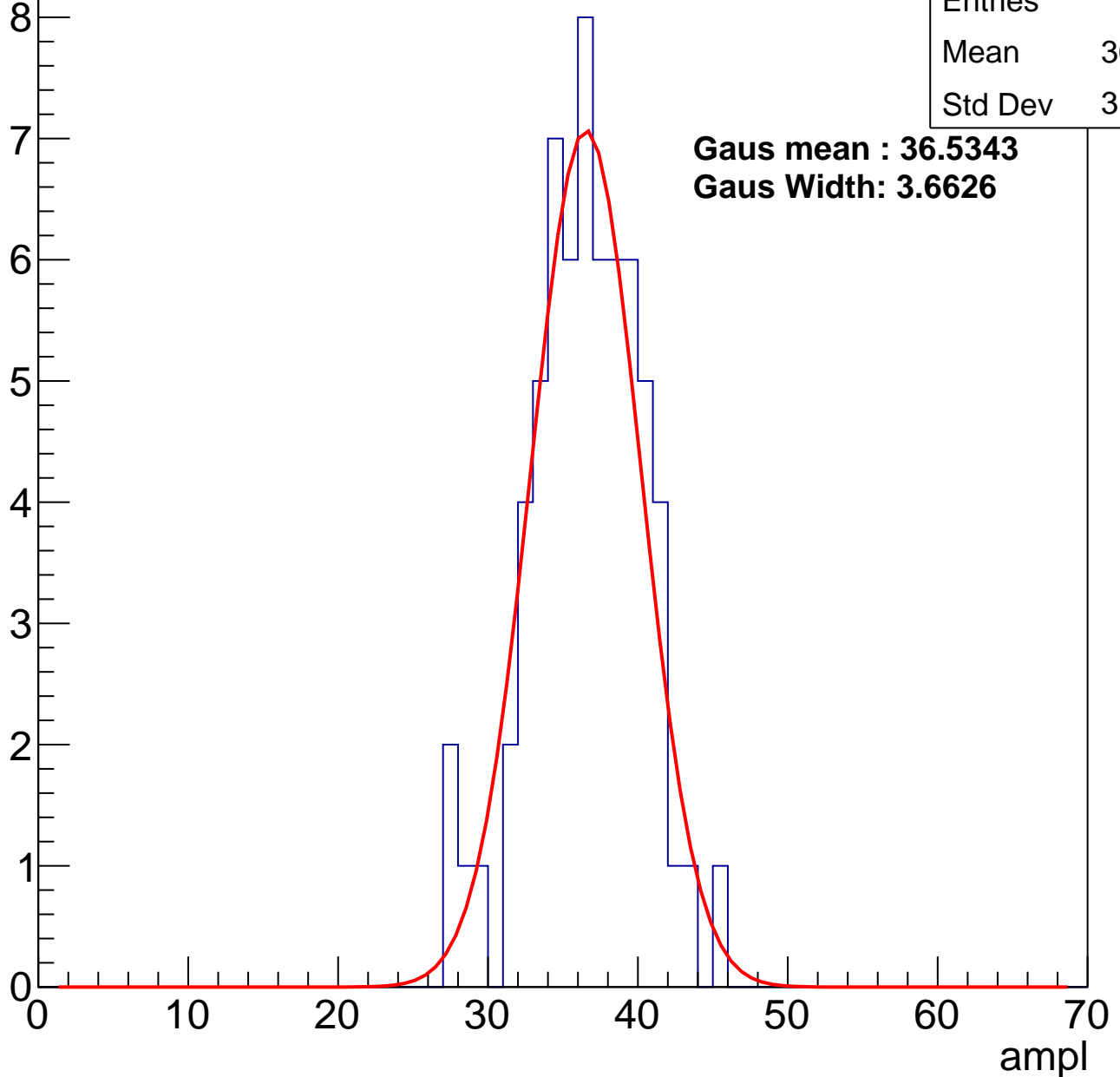
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	36.06
Std Dev	3.688

**Gaus mean : 36.5343**

**Gaus Width: 3.6626**



# B0L001S, U21-ch92, adc2

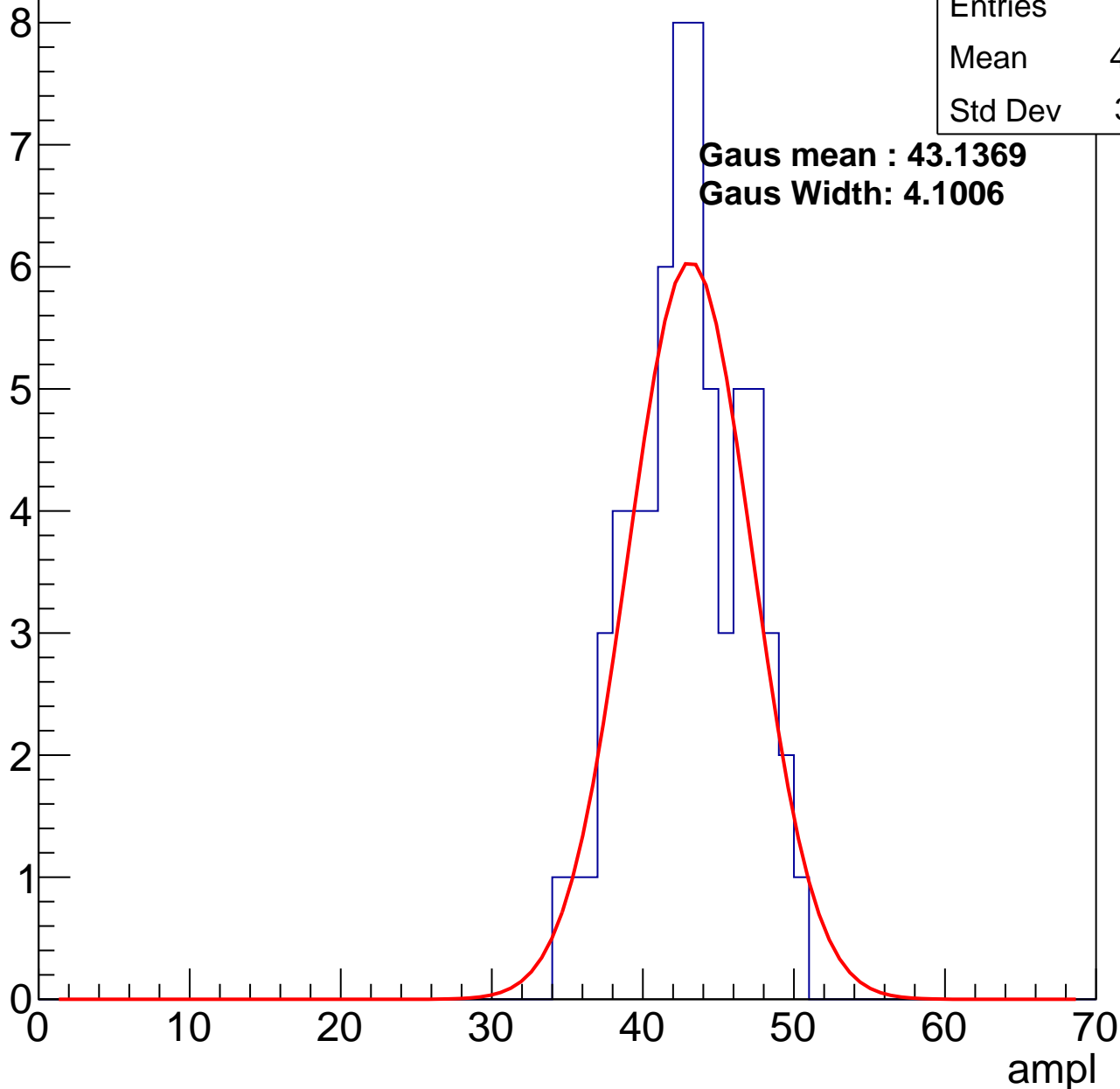
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	42.53
Std Dev	3.661

**Gaus mean : 43.1369**

**Gaus Width: 4.1006**

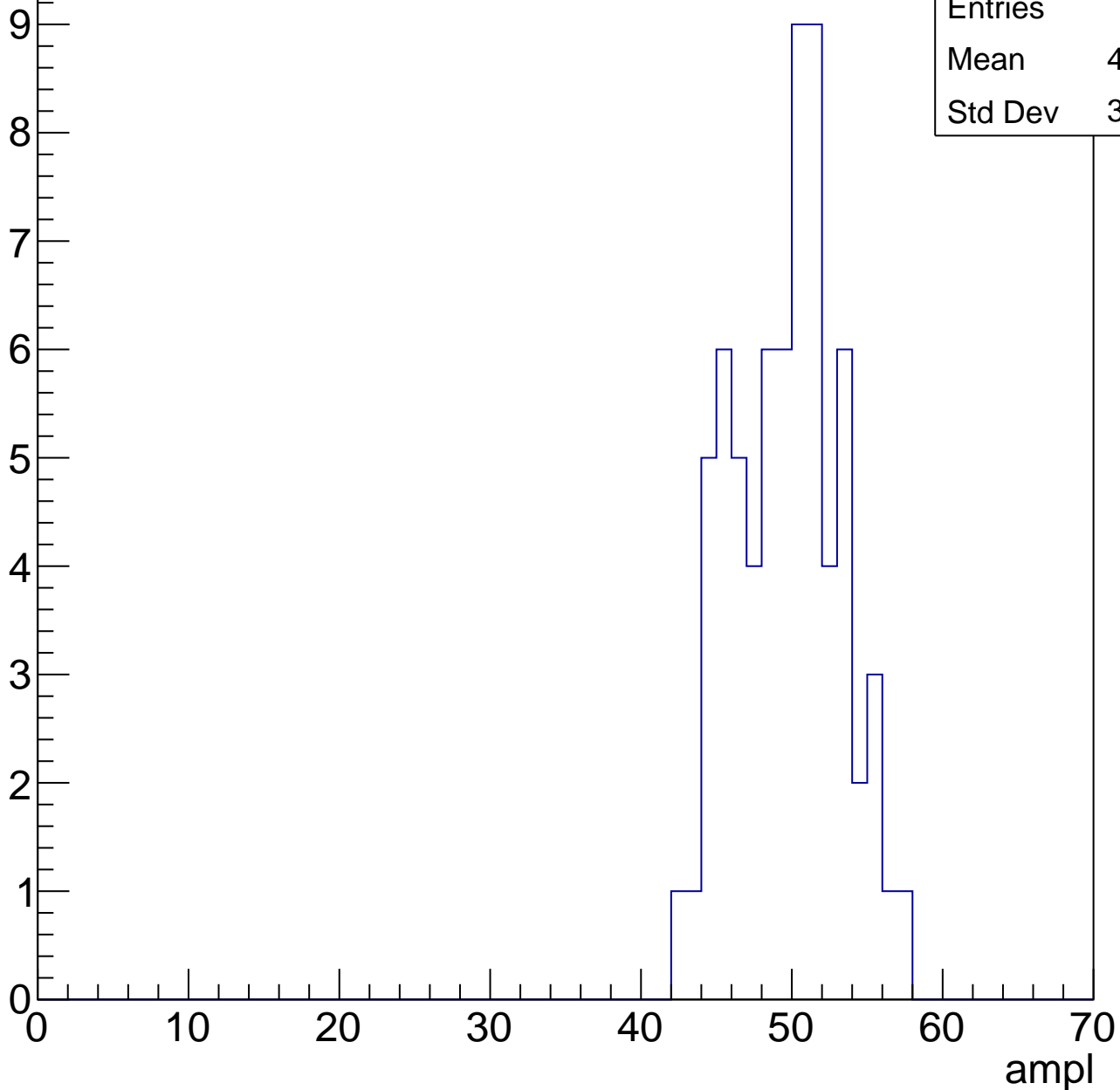


# B0L001S, U21-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

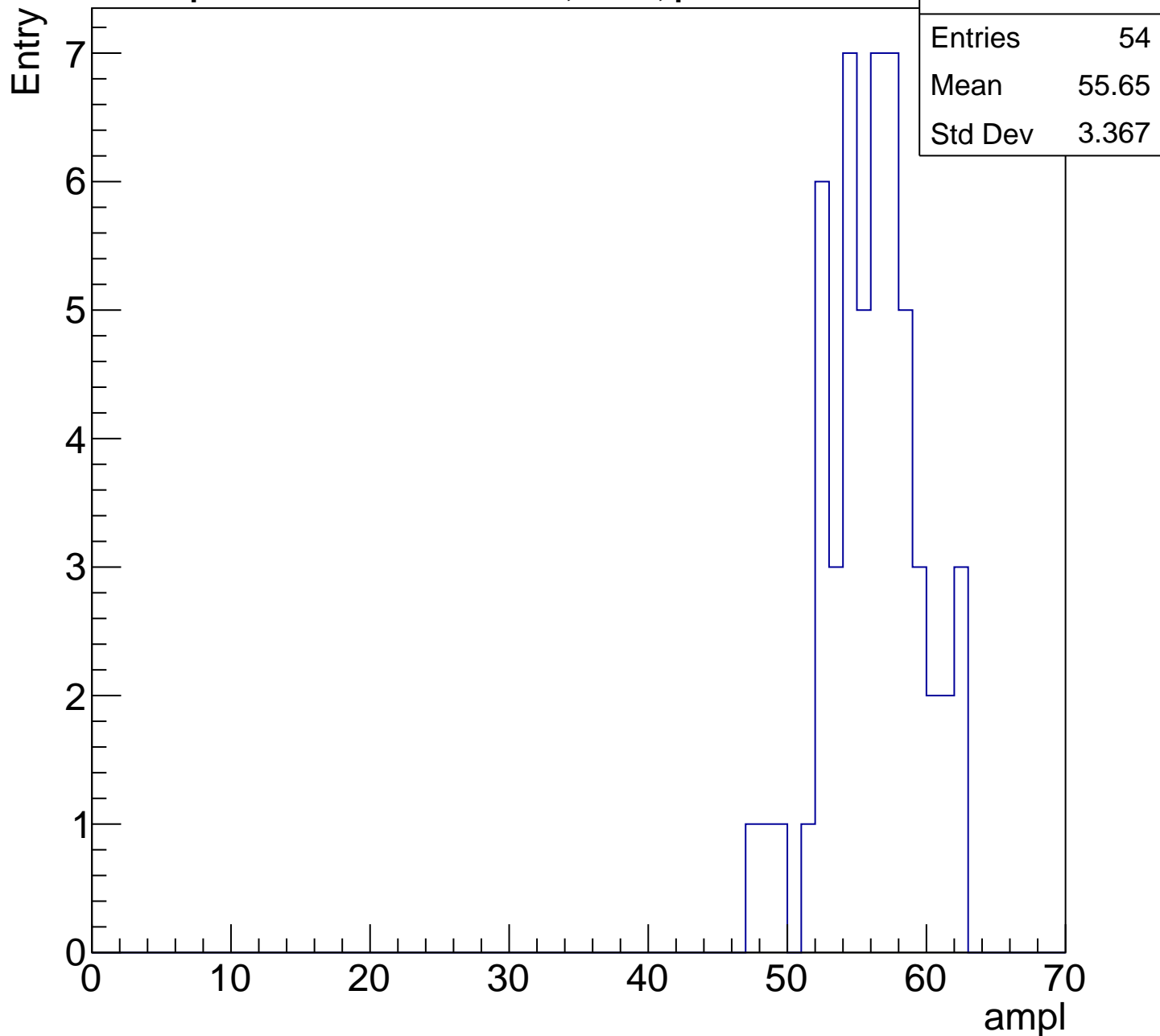
Entry

Entries	69
Mean	49.22
Std Dev	3.443



# B0L001S, U21-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1



# B0L001S, U21-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

7

6

5

4

3

2

1

0

Entries	47
Mean	58.11
Std Dev	9.051

ampl

10

20

30

40

50

60

70

# B0L001S, U21-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

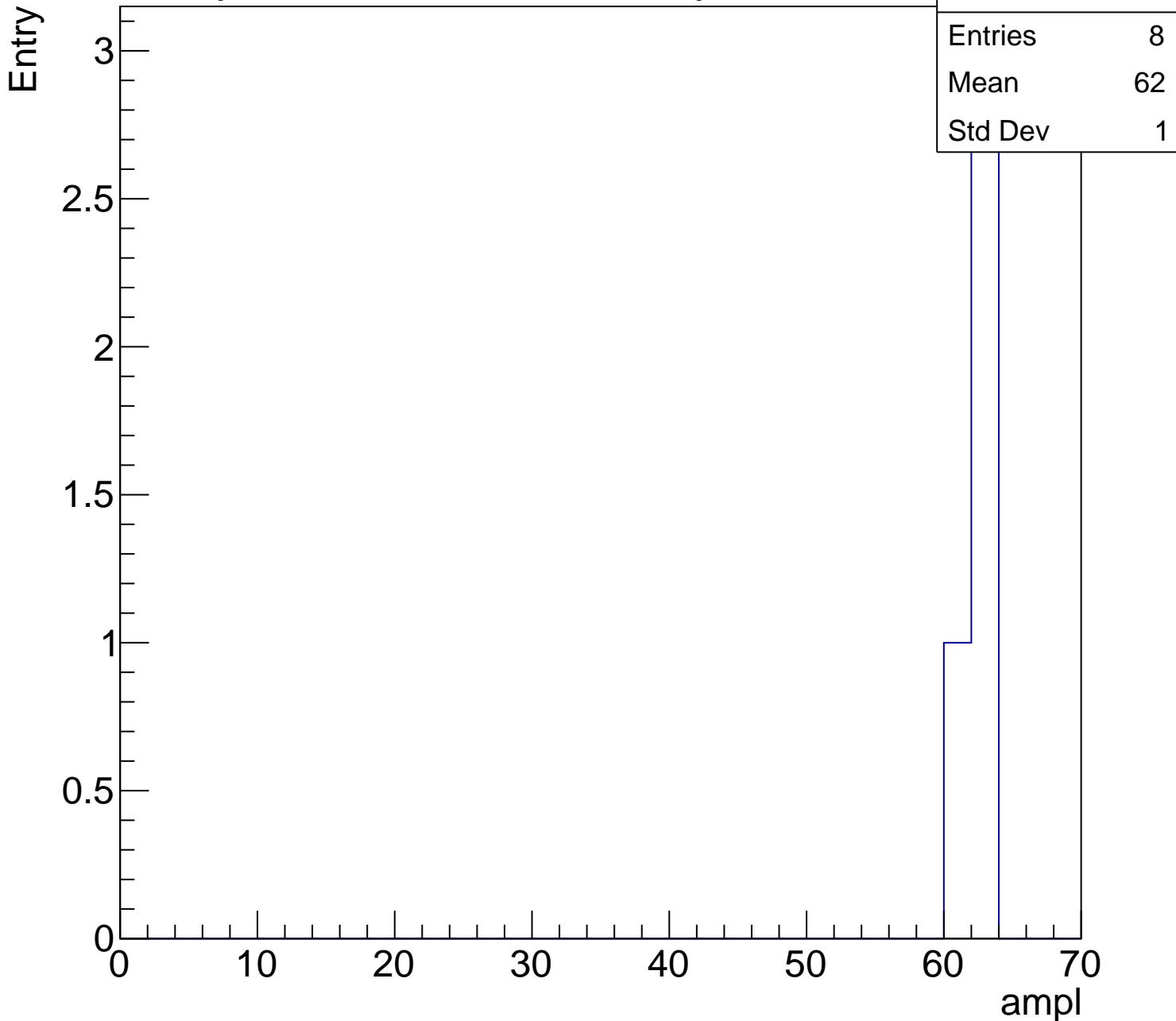
Entry

3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	8
Mean	62
Std Dev	1

ampl

0 10 20 30 40 50 60 70





# B0L001S, U21-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U21-ch93, adc0

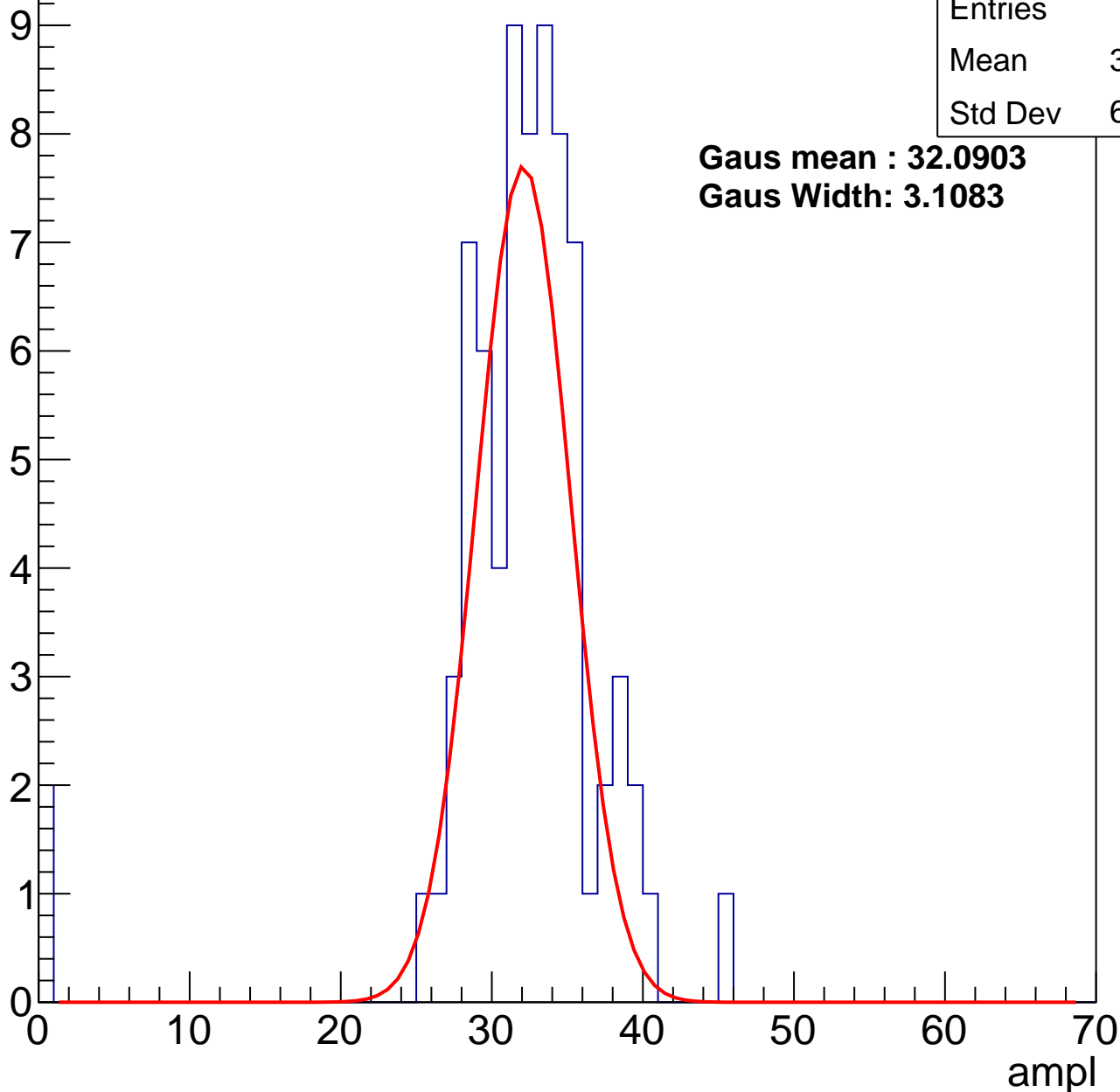
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	75
Mean	31.44
Std Dev	6.308

**Gaus mean : 32.0903**

**Gaus Width: 3.1083**



# B0L001S, U21-ch93, adc1

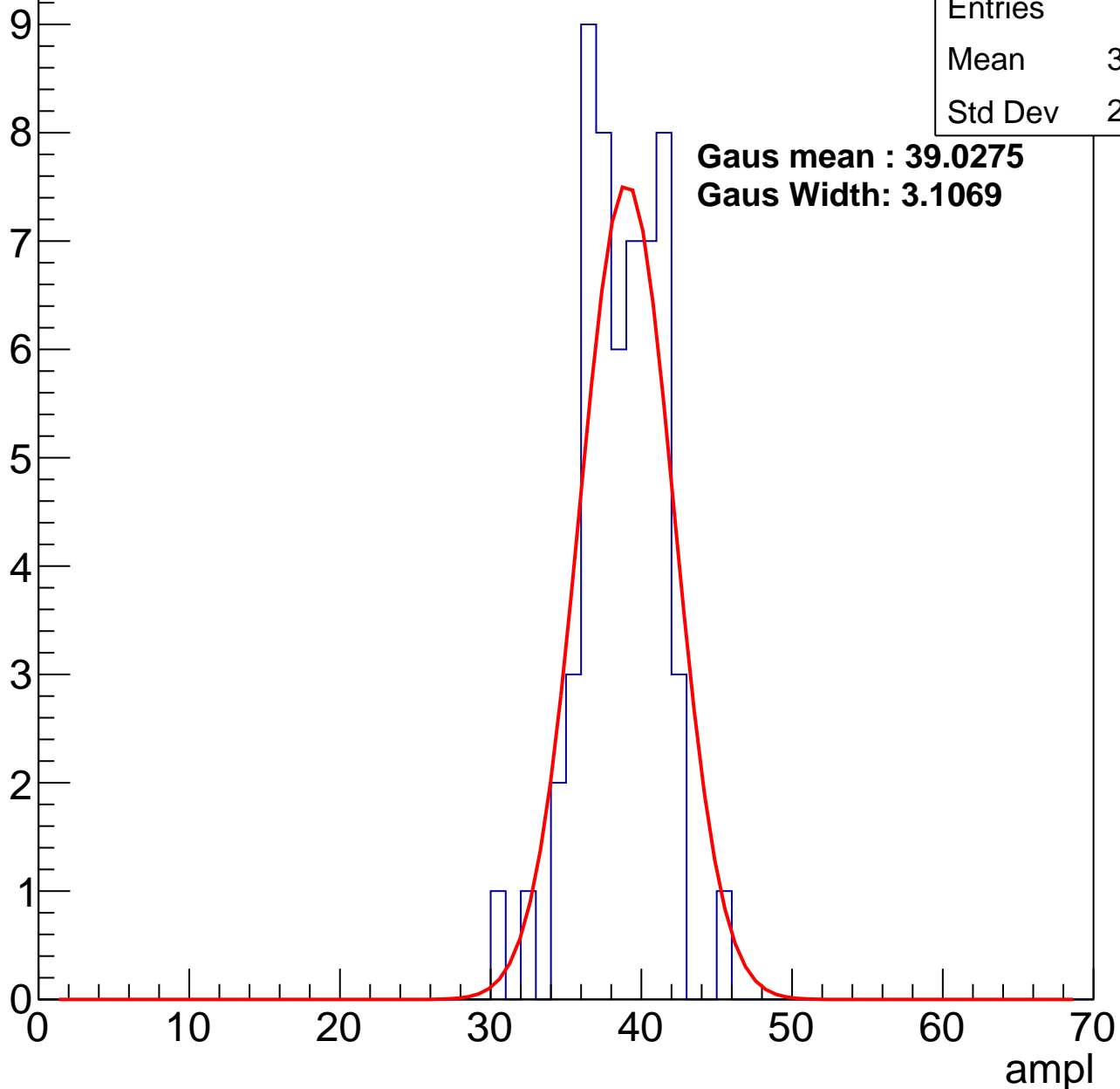
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	38.12
Std Dev	2.693

**Gaus mean : 39.0275**

**Gaus Width: 3.1069**



# B0L001S, U21-ch93, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	52
Mean	44.46
Std Dev	2.825

**Gaus mean : 46.2007**

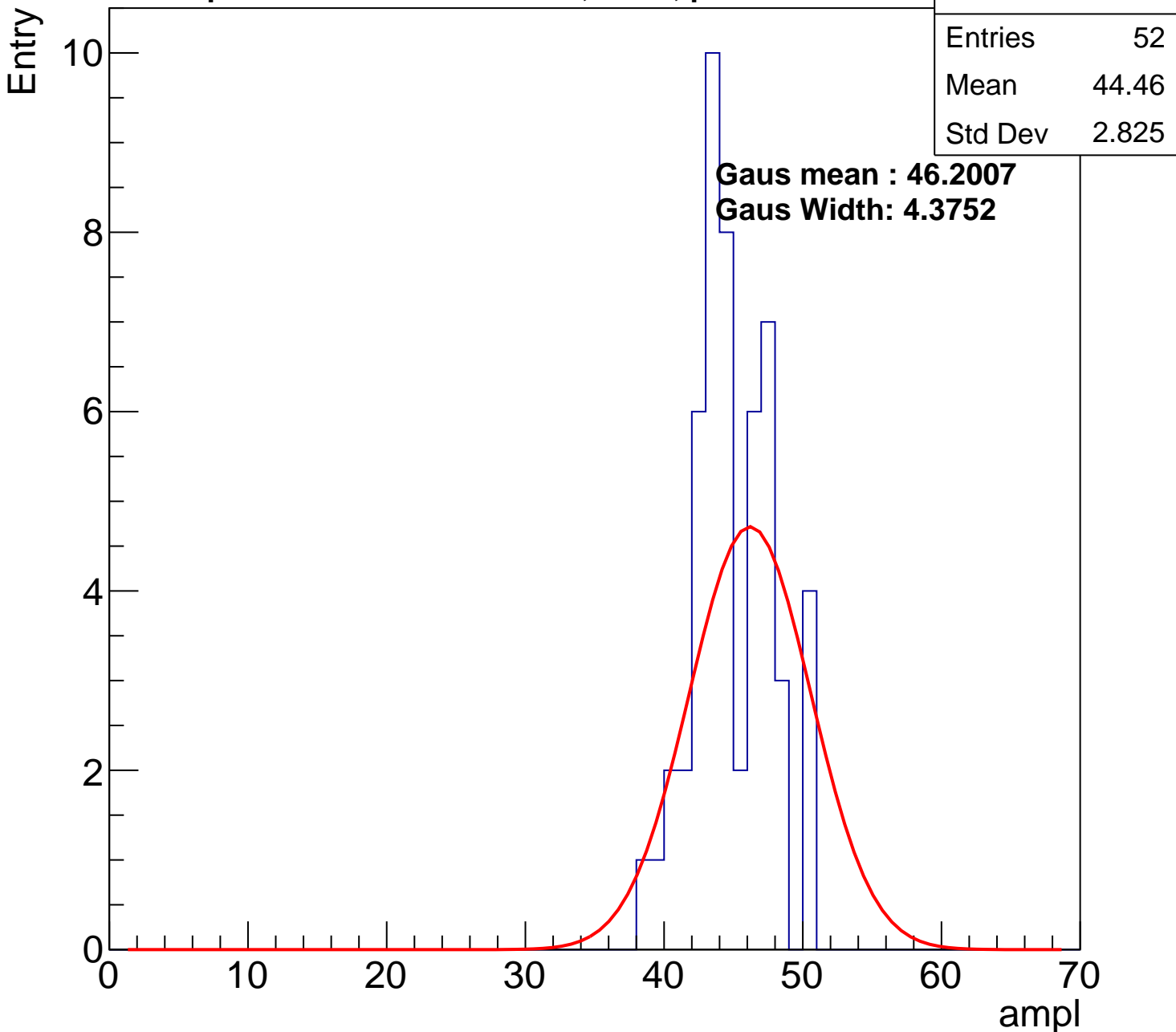
**Gaus Width: 4.3752**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

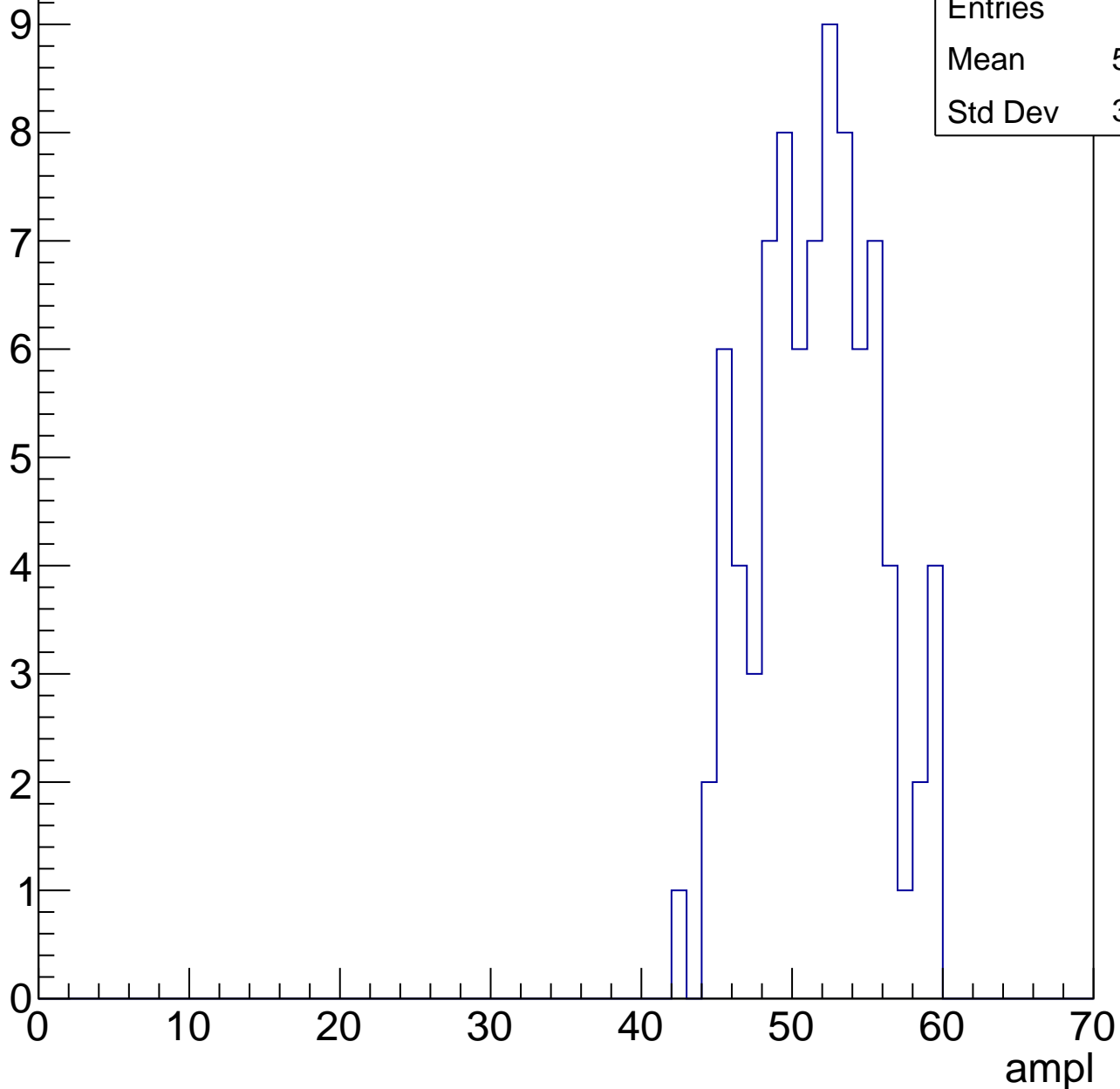


# B0L001S, U21-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	85
Mean	51.11
Std Dev	3.971

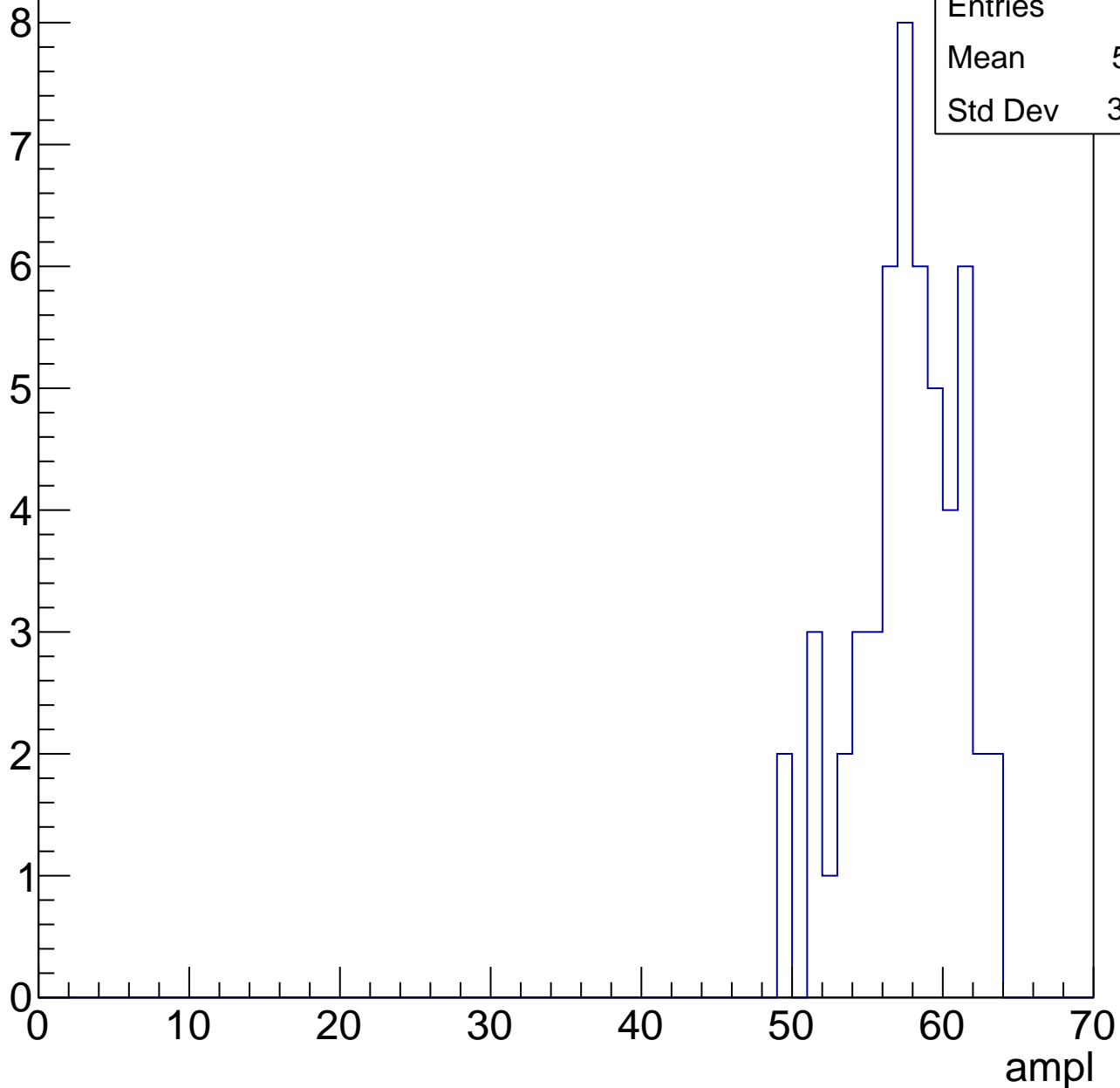


# B0L001S, U21-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	57.11
Std Dev	3.413

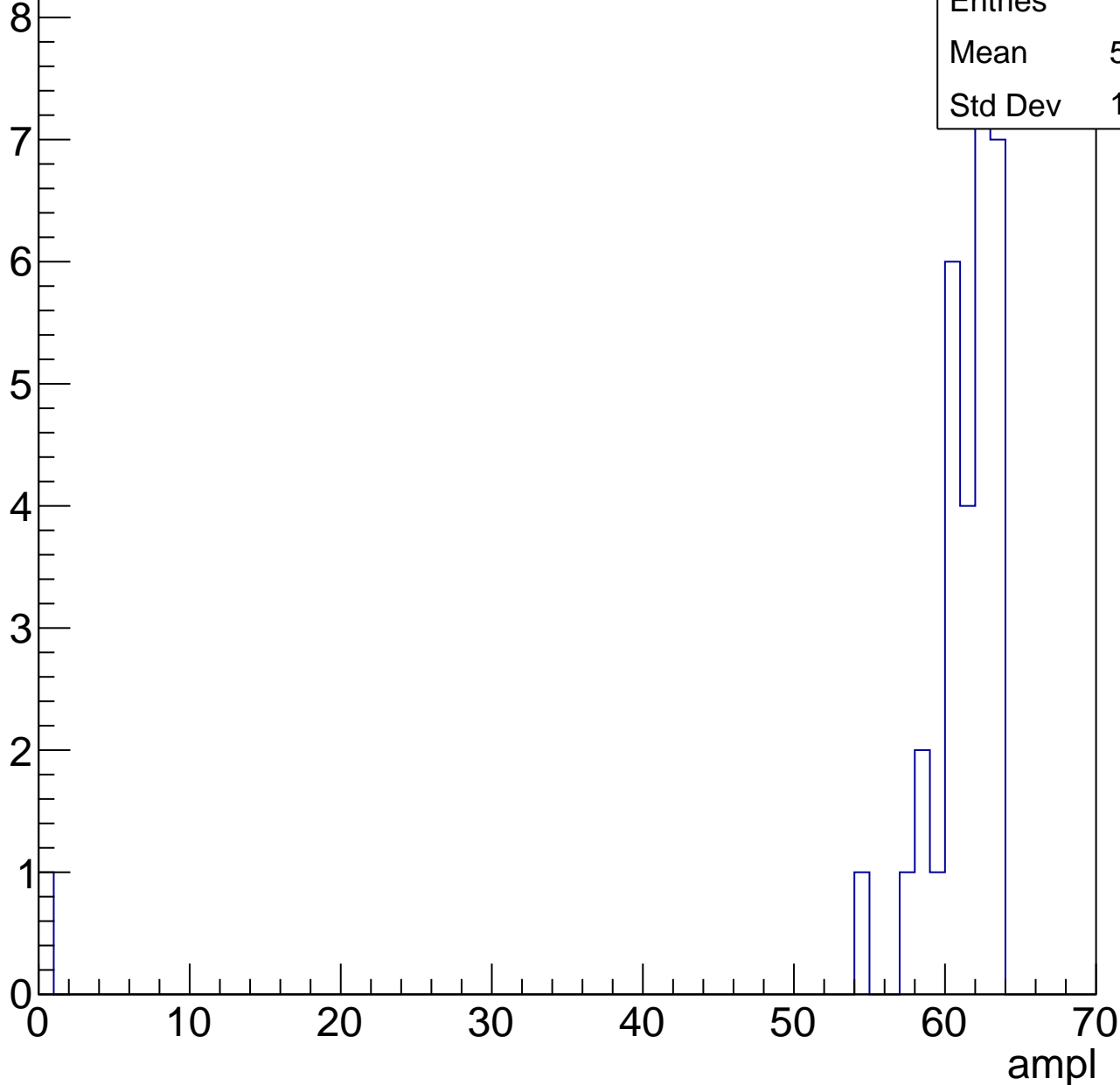


# B0L001S, U21-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	31
Mean	58.94
Std Dev	10.95



# B0L001S, U21-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch94, adc0

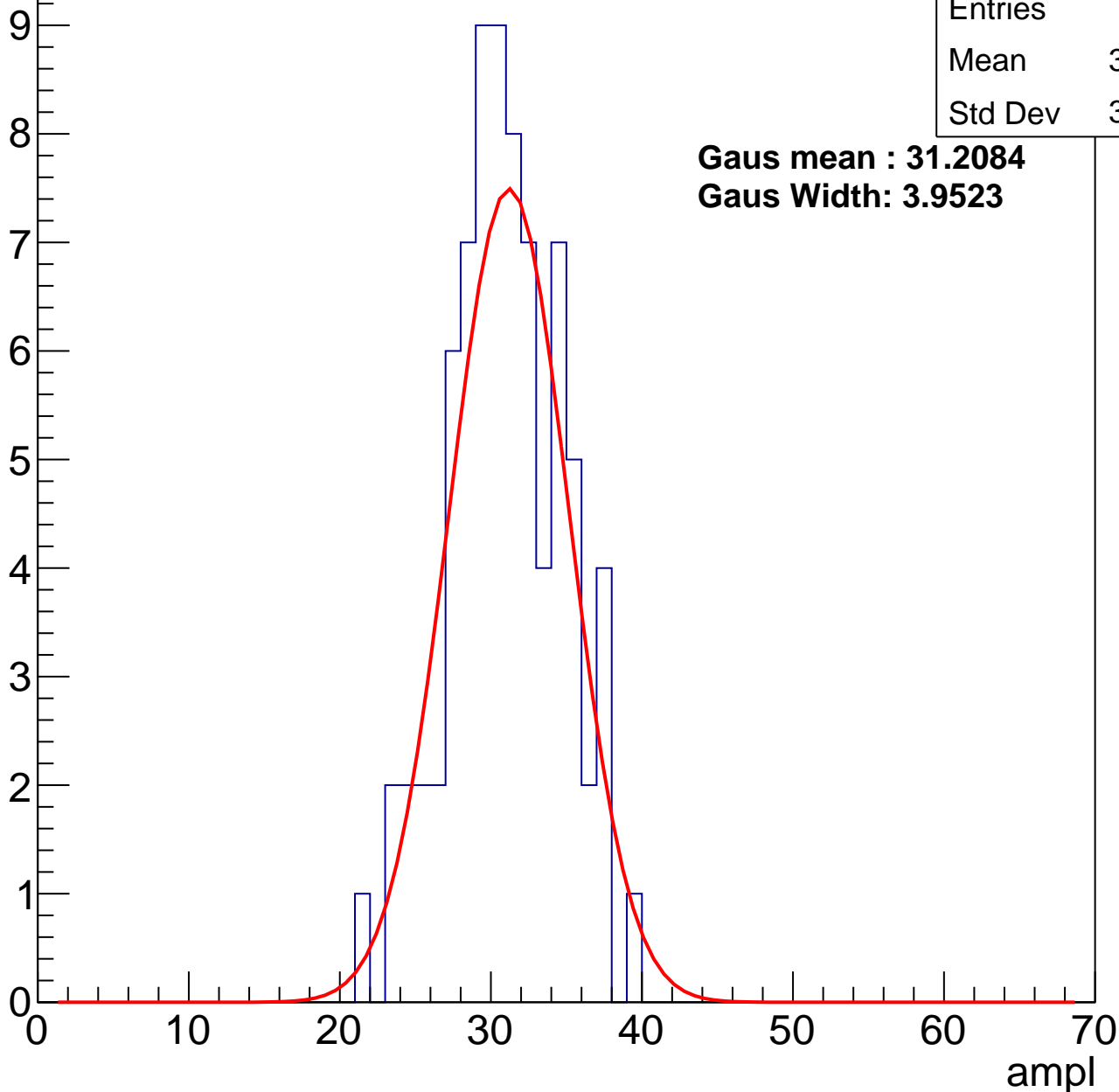
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	30.54
Std Dev	3.685

**Gaus mean : 31.2084**

**Gaus Width: 3.9523**



# B0L001S, U21-ch94, adc1

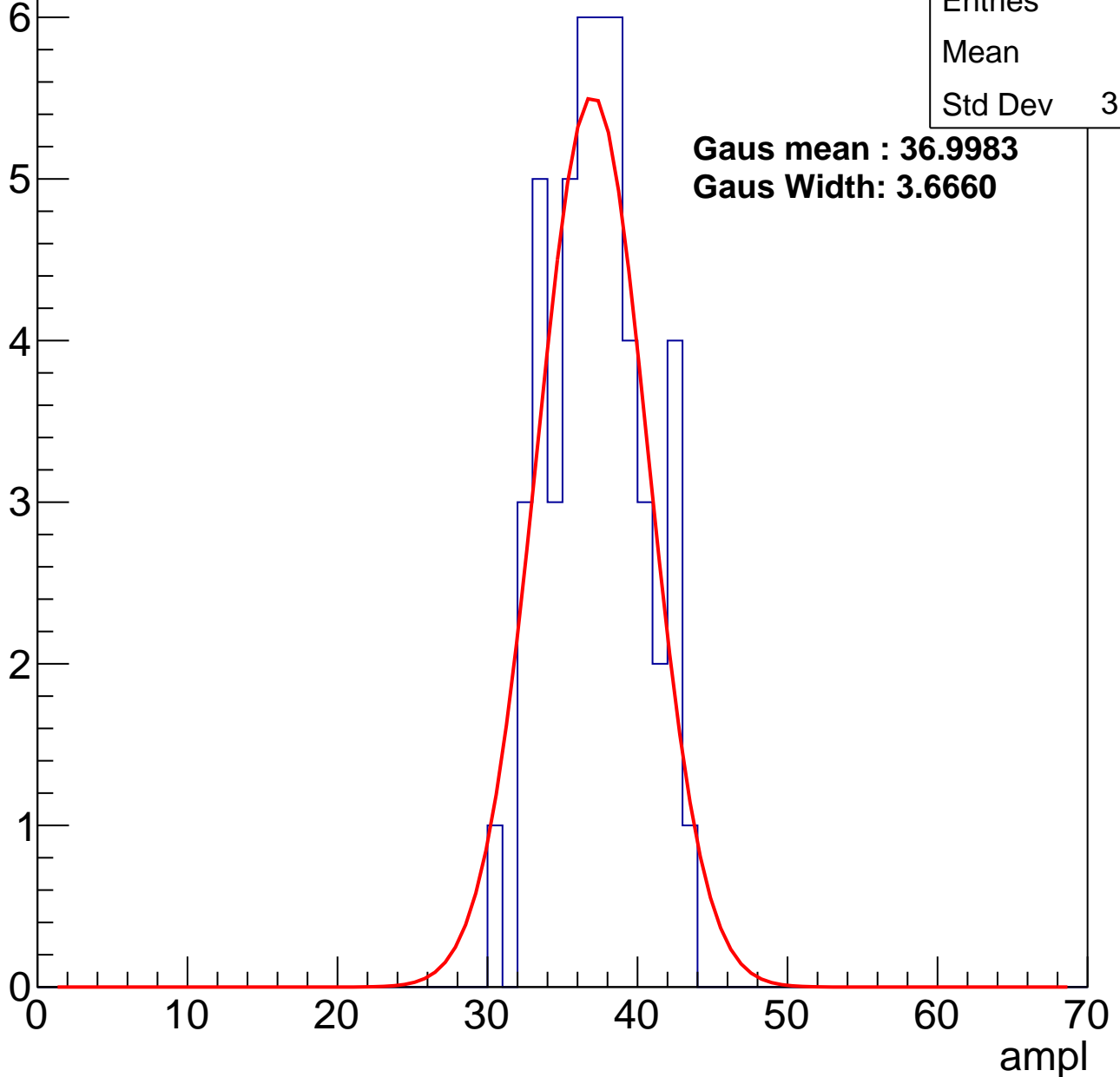
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	36.8
Std Dev	3.104

**Gaus mean : 36.9983**

**Gaus Width: 3.6660**



# B0L001S, U21-ch94, adc2

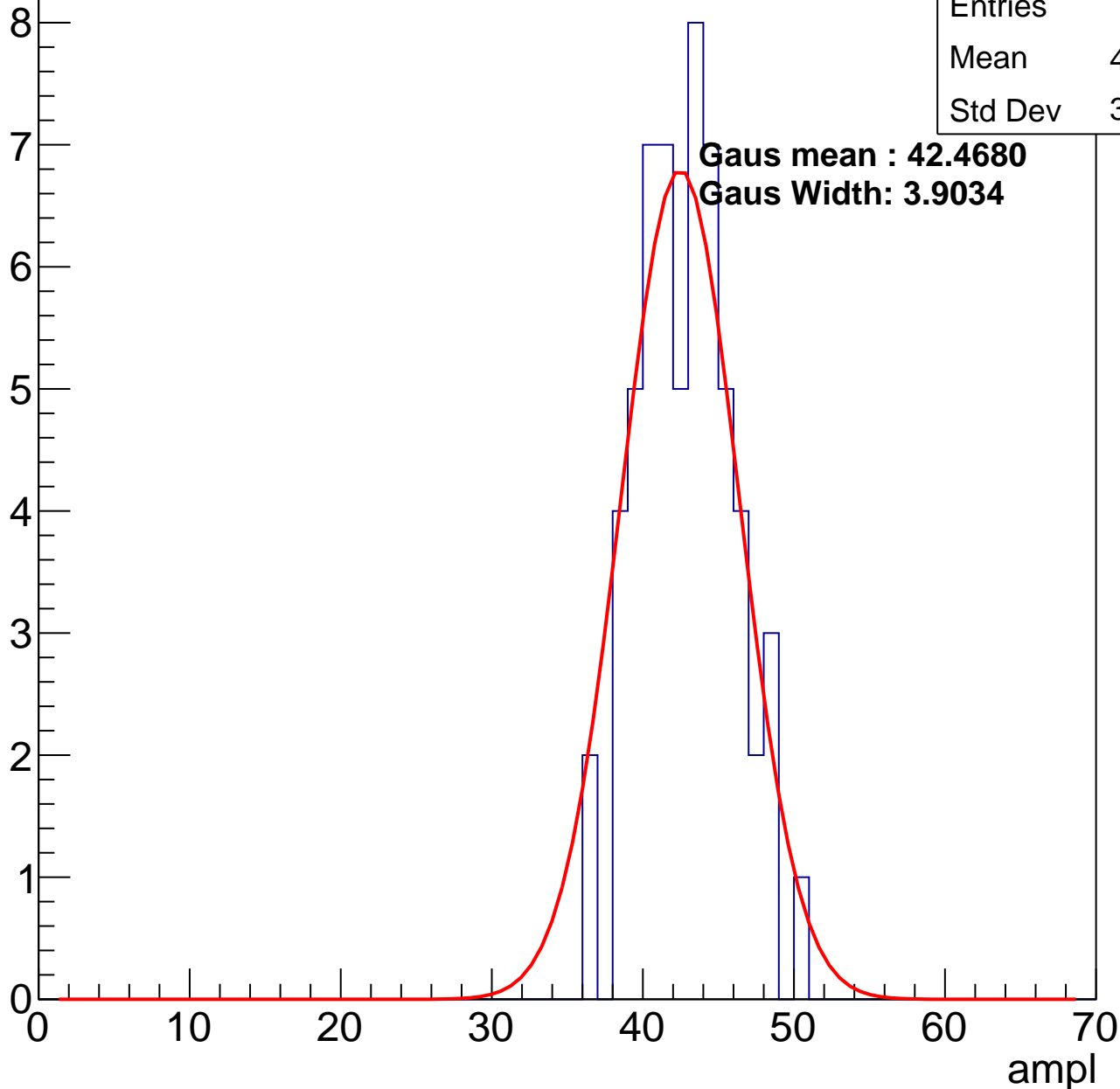
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	42.42
Std Dev	3.089

**Gaus mean : 42.4680**

**Gaus Width: 3.9034**

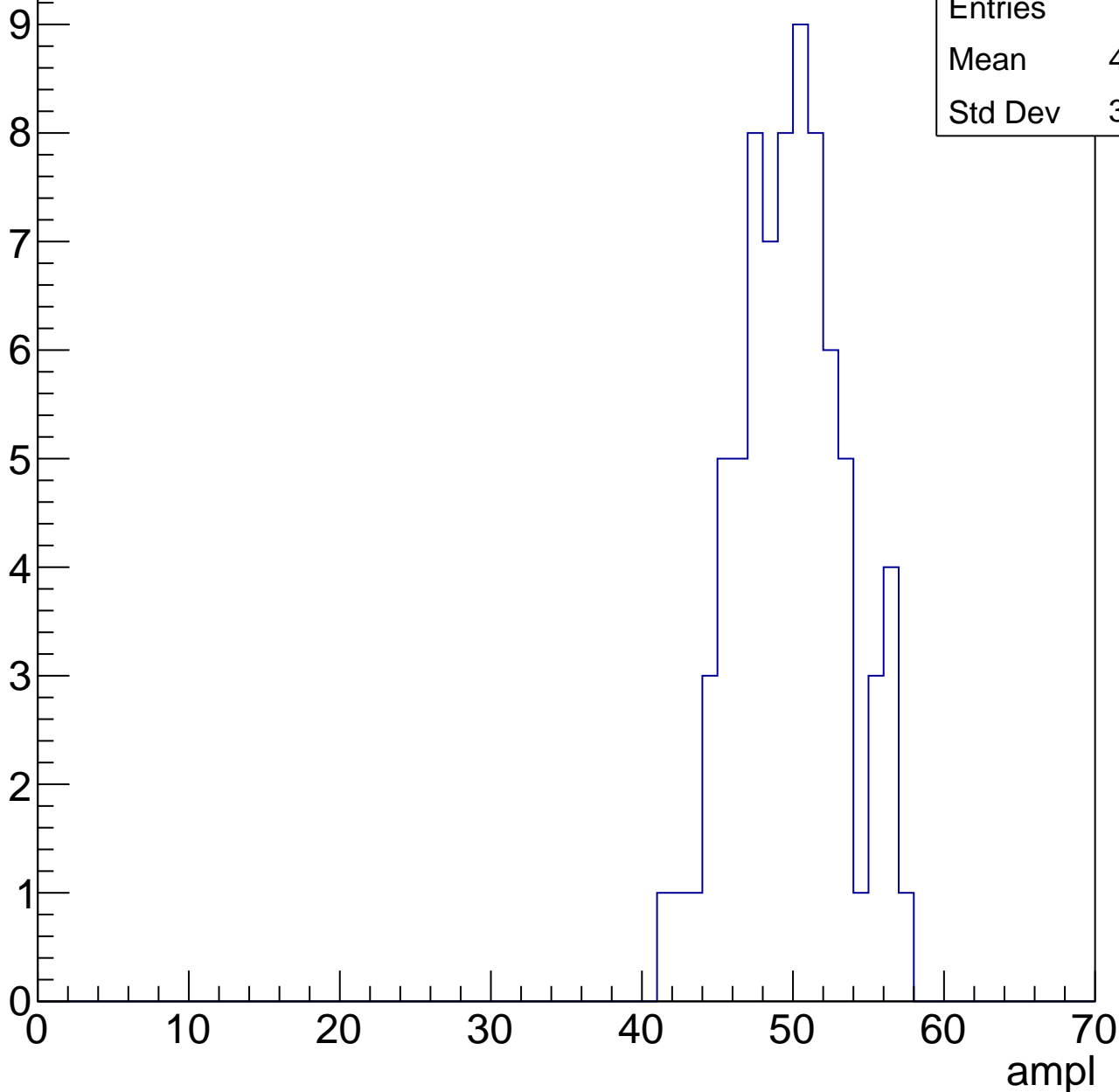


# B0L001S, U21-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	49.37
Std Dev	3.527

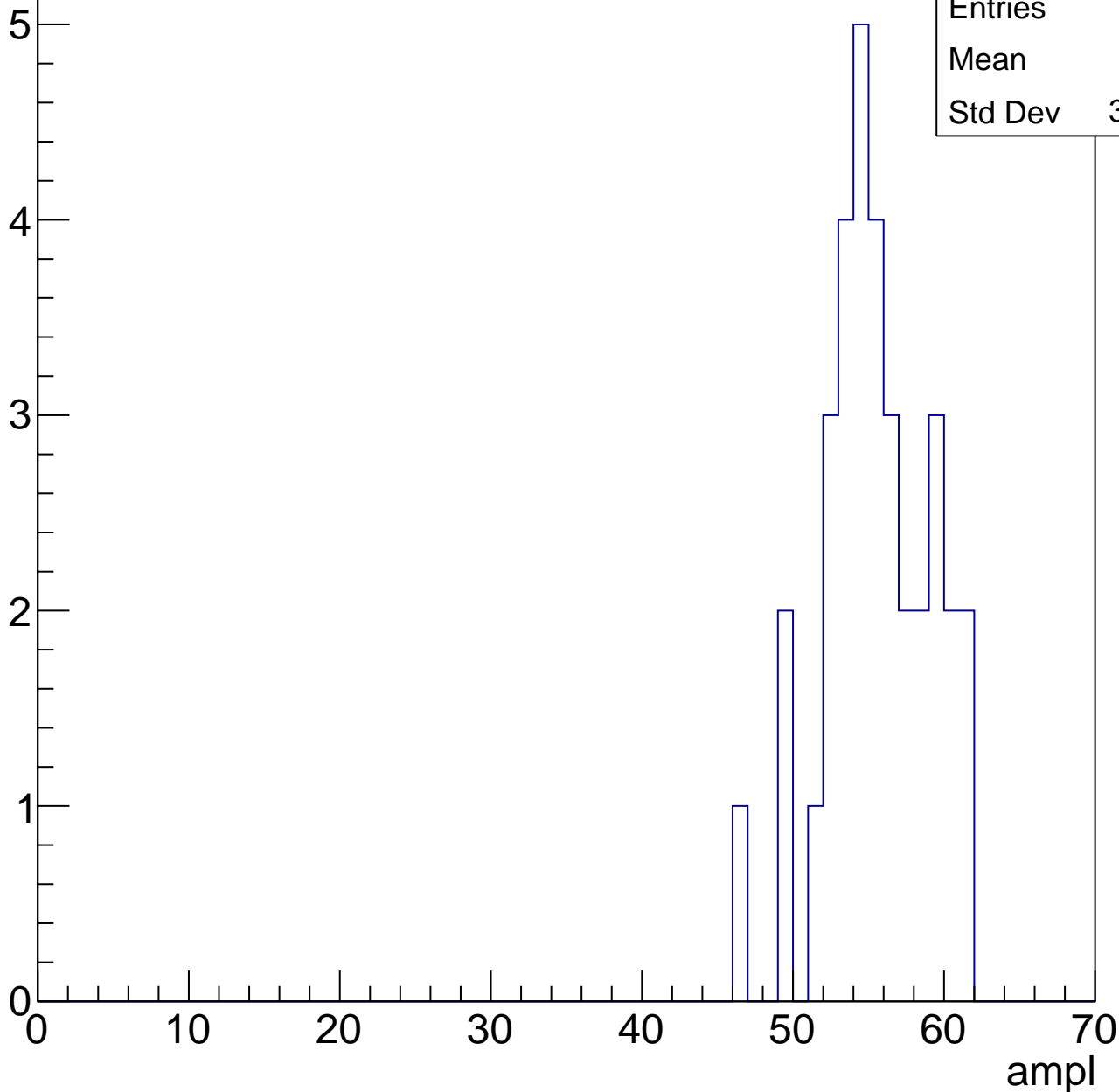


# B0L001S, U21-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	34
Mean	55
Std Dev	3.498

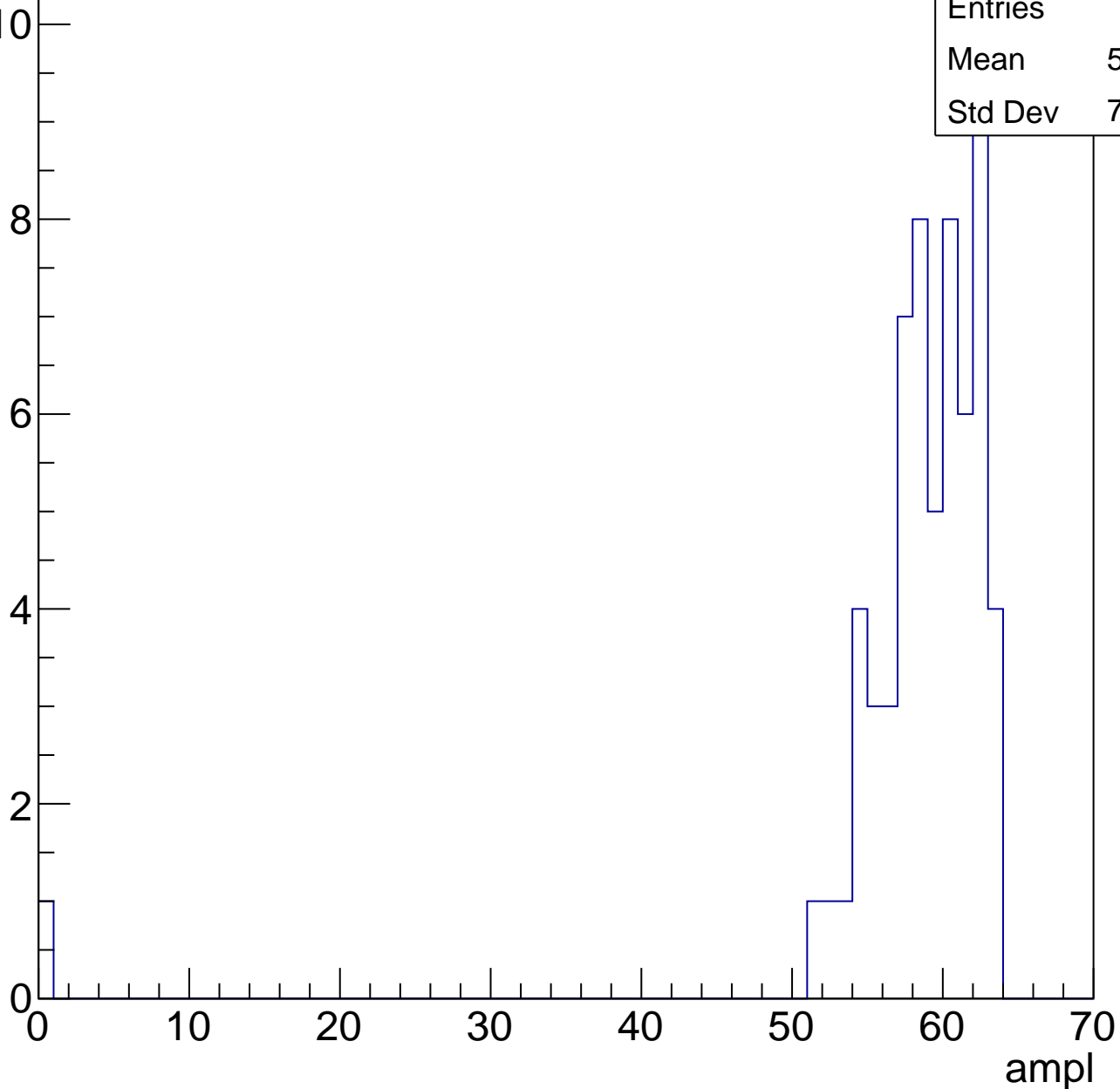


# B0L001S, U21-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	57.76
Std Dev	7.963

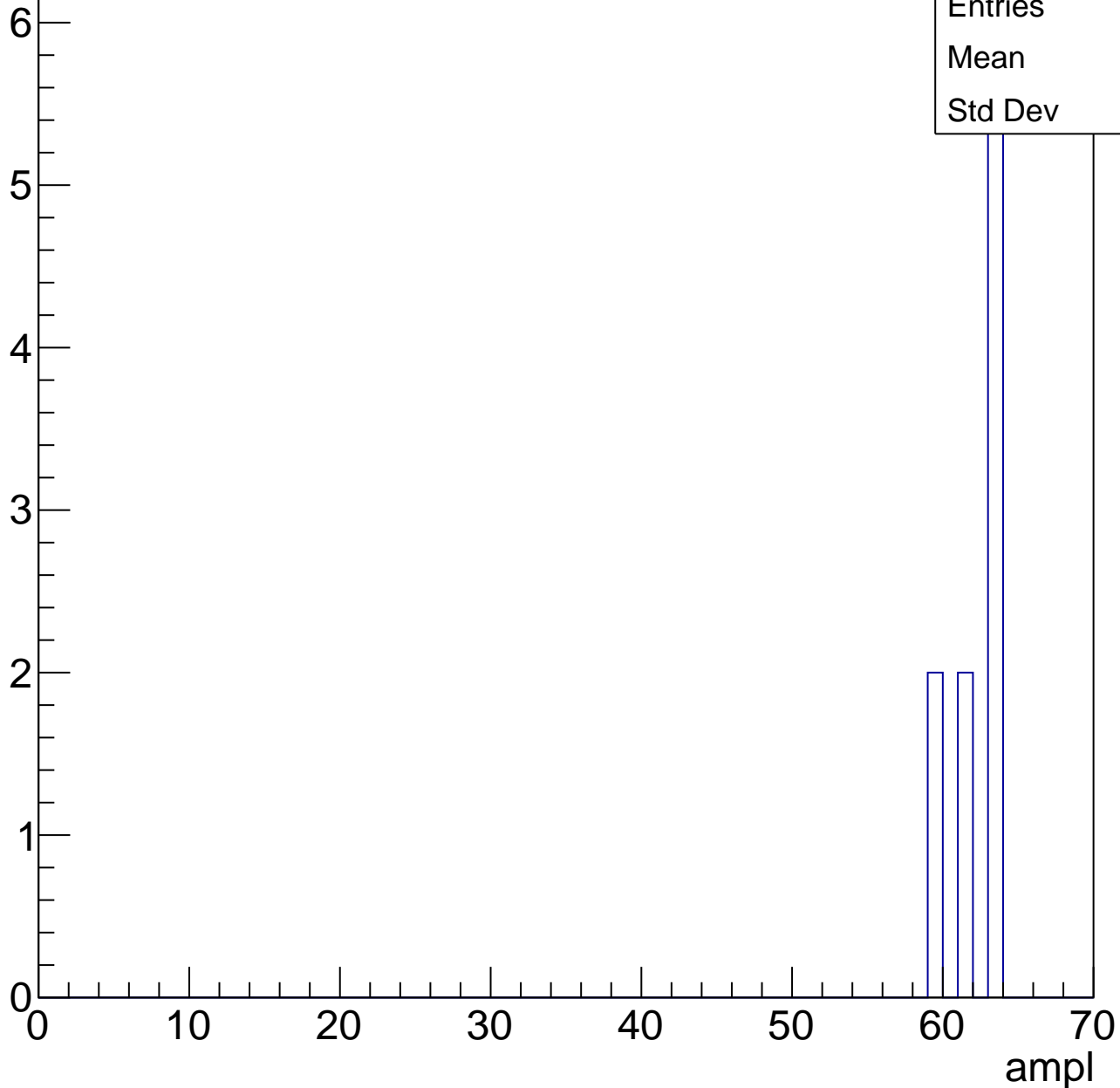


# B0L001S, U21-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	10
Mean	61.8
Std Dev	1.6





# B0L001S, U21-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U21-ch95, adc0

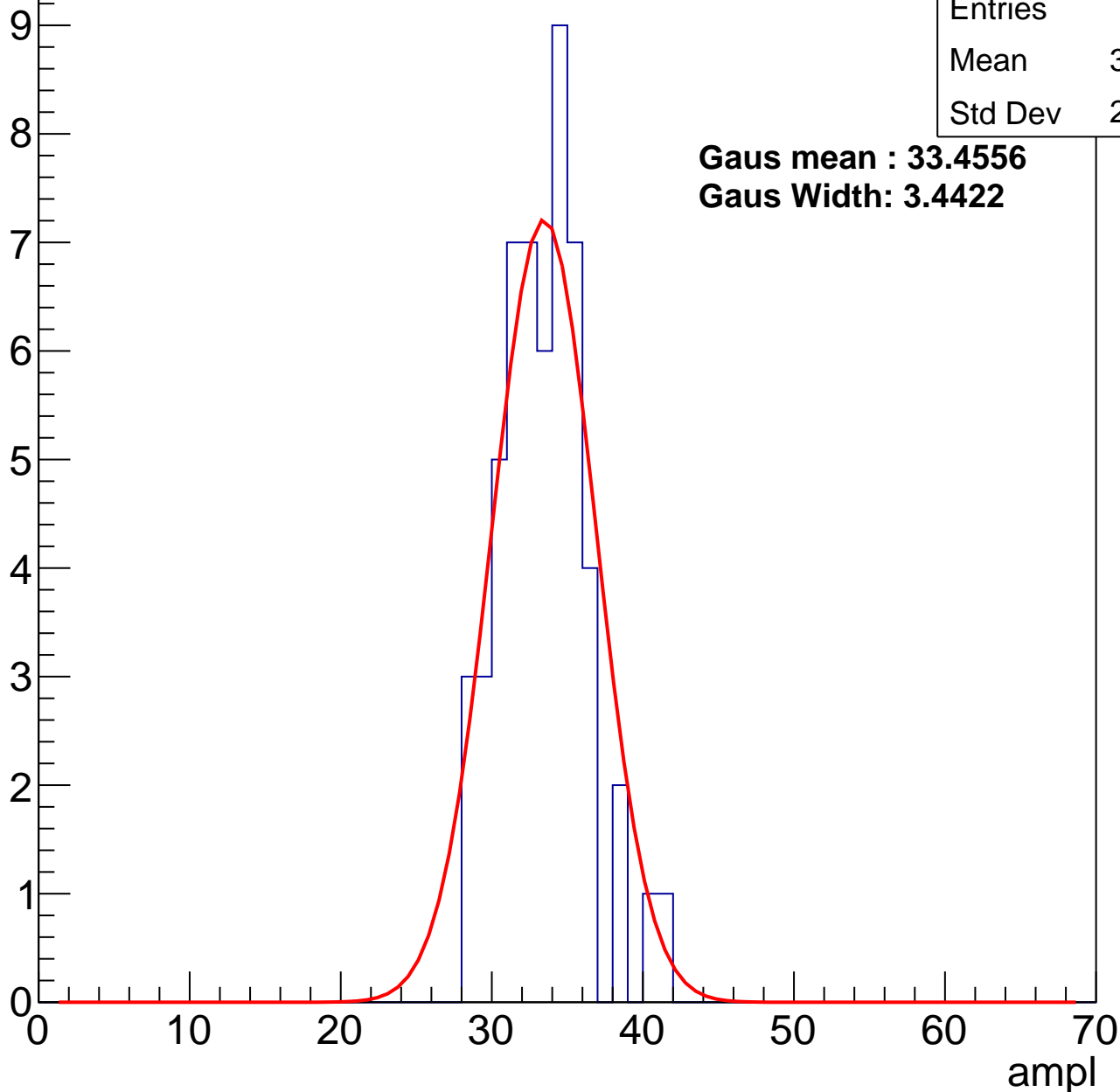
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	32.95
Std Dev	2.825

**Gaus mean : 33.4556**

**Gaus Width: 3.4422**



# B0L001S, U21-ch95, adc1

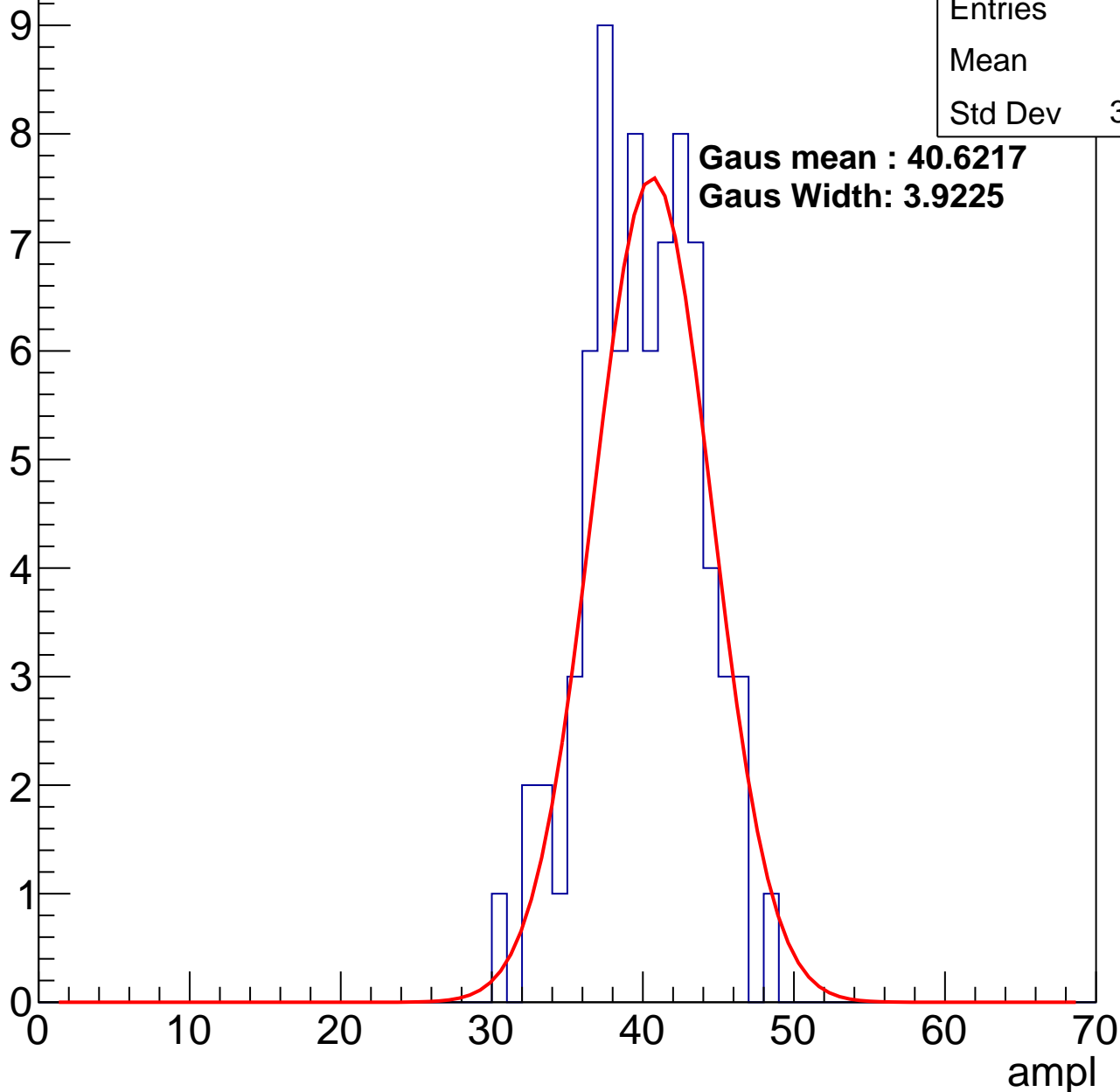
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	39.6
Std Dev	3.687

**Gaus mean : 40.6217**

**Gaus Width: 3.9225**



# B0L001S, U21-ch95, adc2

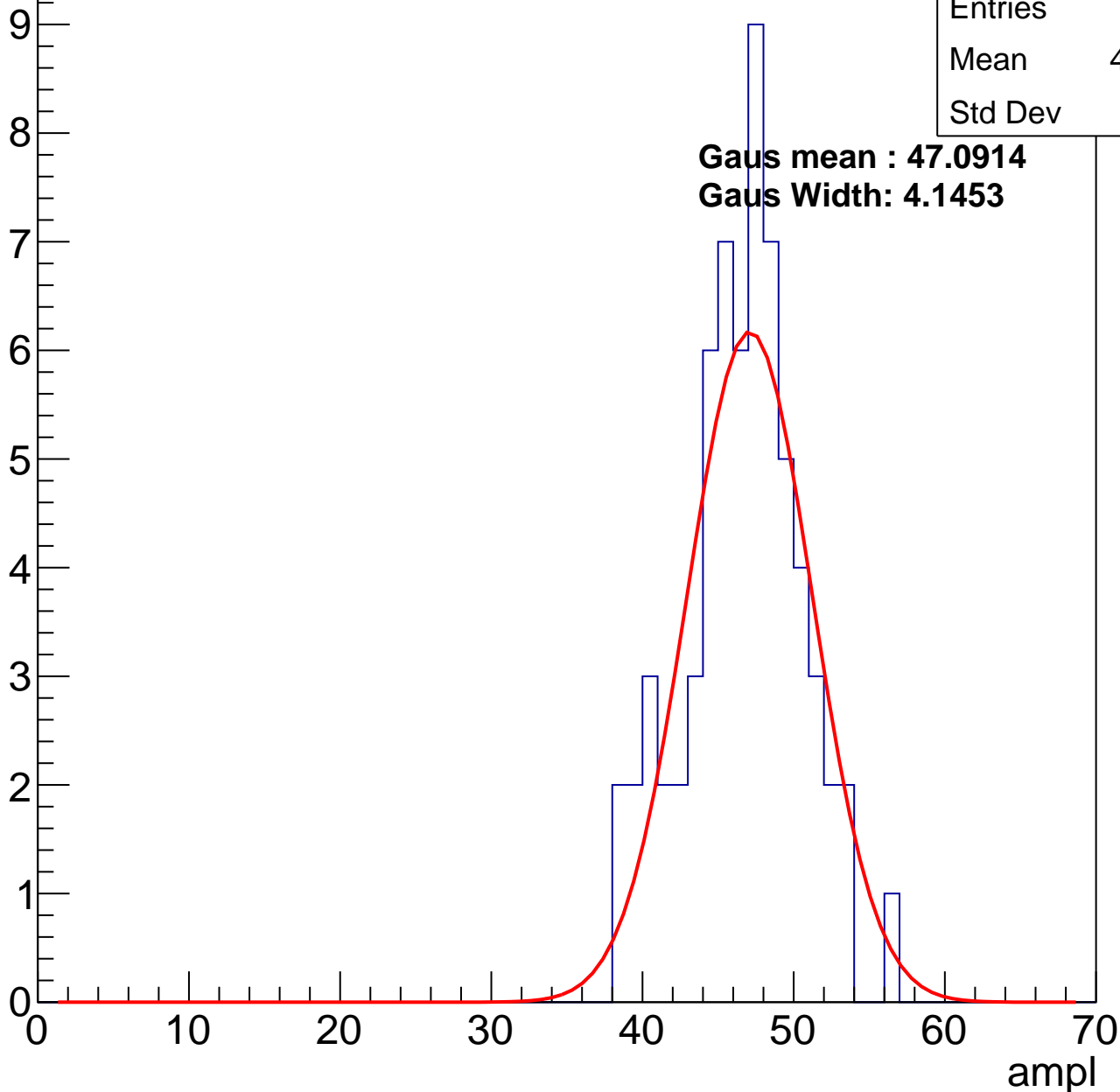
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	46.17
Std Dev	3.82

**Gaus mean : 47.0914**

**Gaus Width: 4.1453**

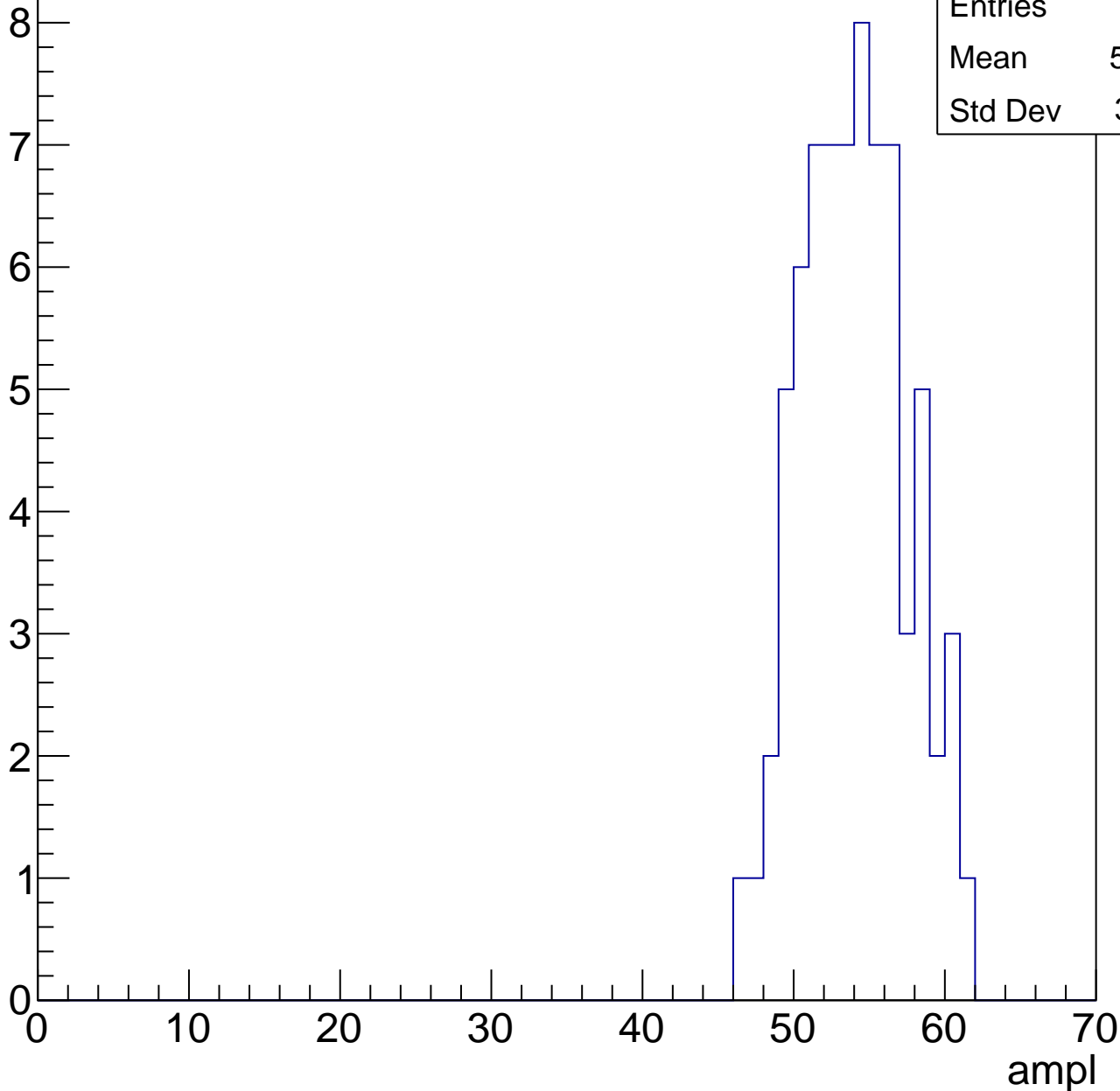


# B0L001S, U21-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

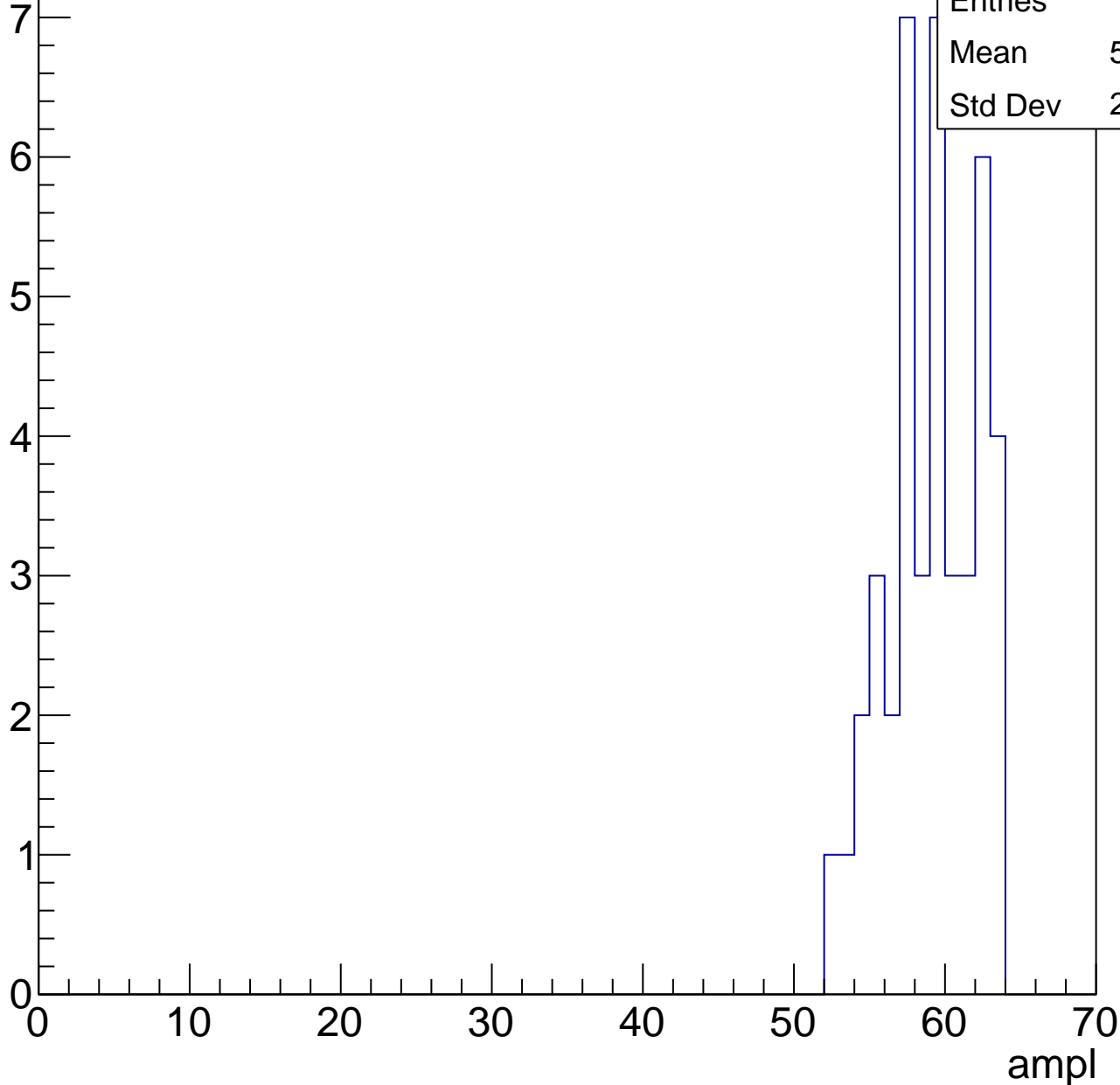
Entries	72
Mean	53.54
Std Dev	3.411



# B0L001S, U21-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

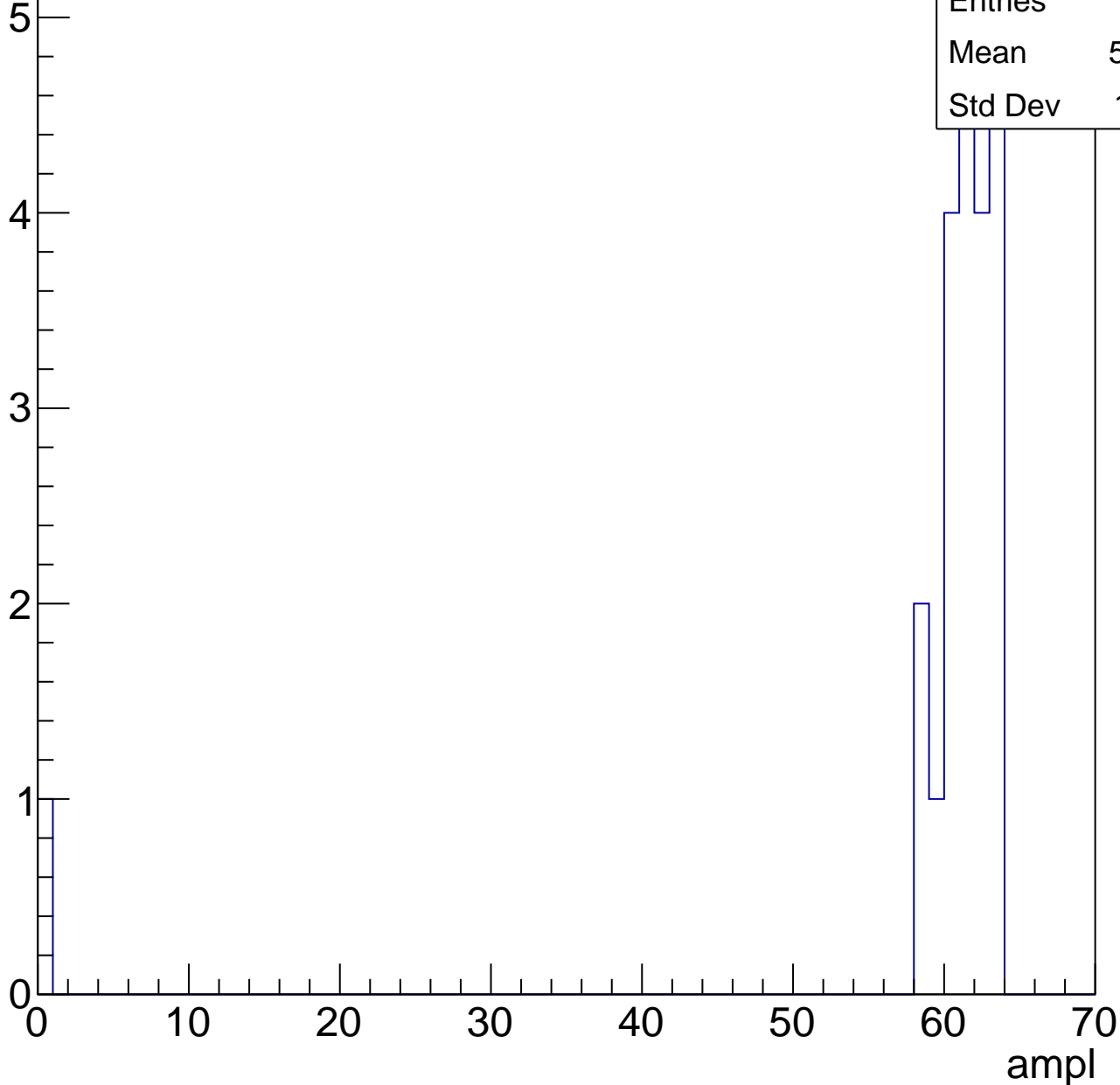


# B0L001S, U21-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	22
Mean	58.32
Std Dev	12.81



# B0L001S, U21-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	27
Std Dev	0

ampl

0 10 20 30 40 50 60 70

# B0L001S, U21-ch96, adc0

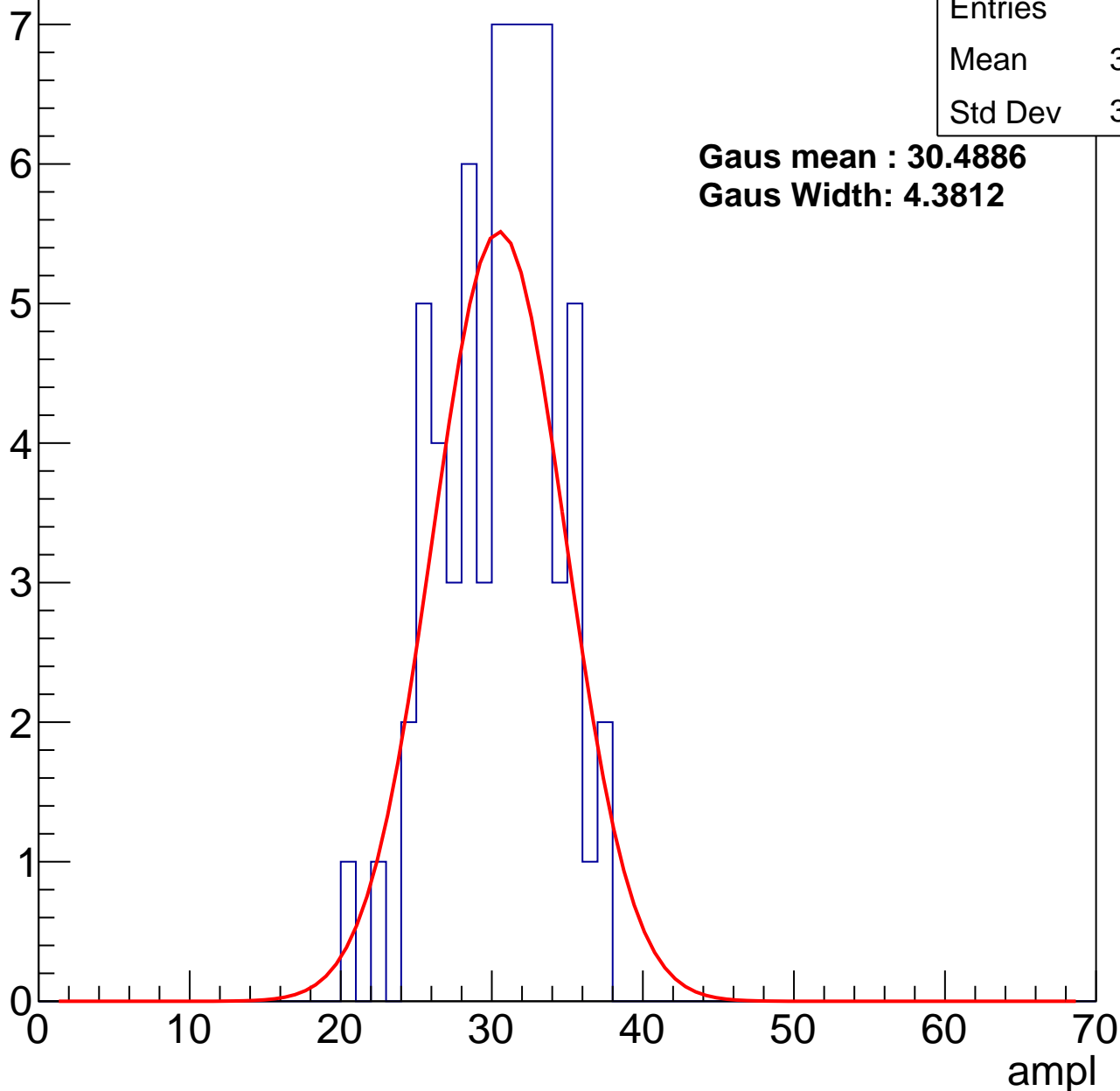
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	30.06
Std Dev	3.716

**Gaus mean : 30.4886**

**Gaus Width: 4.3812**



# B0L001S, U21-ch96, adc1

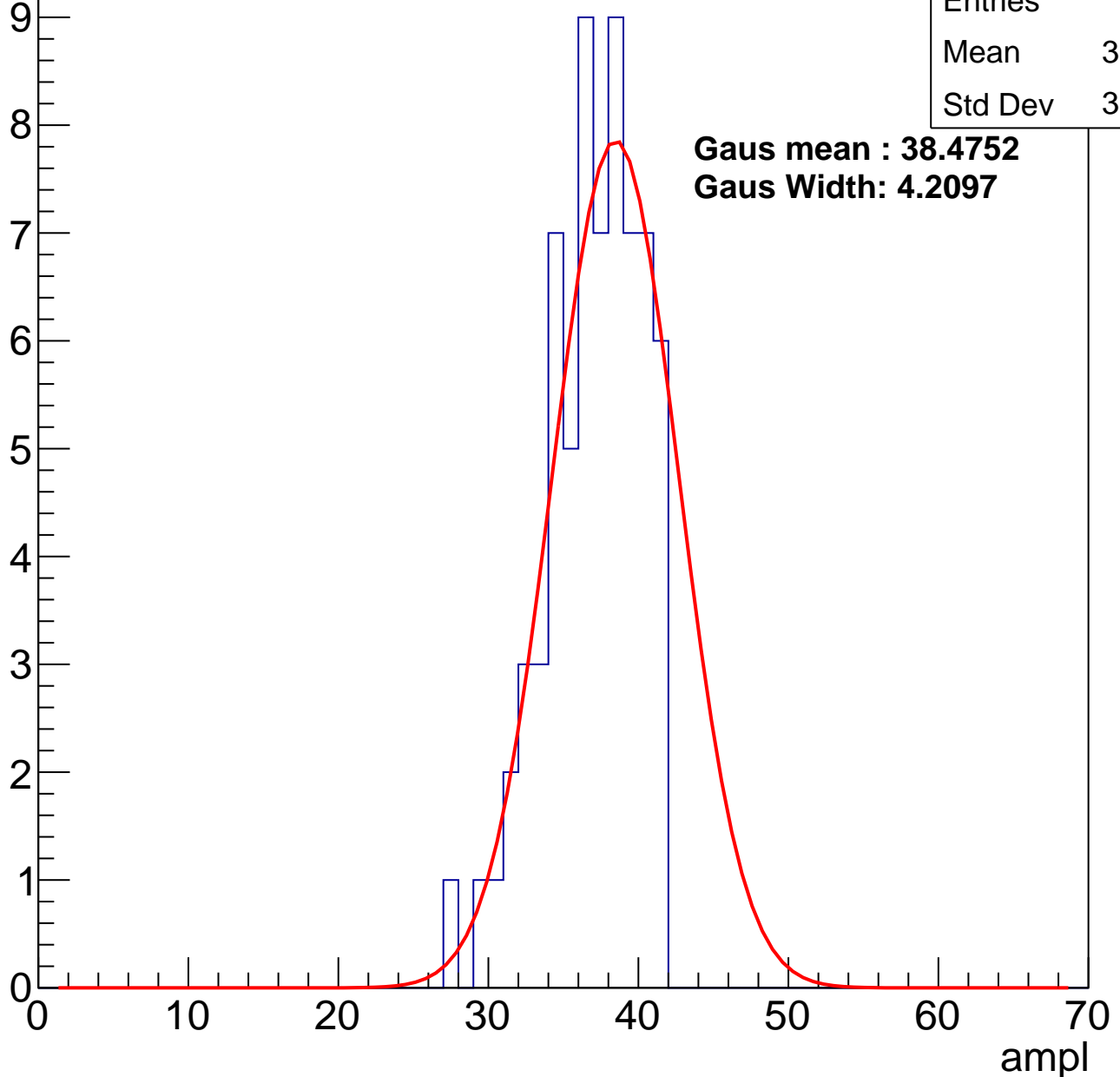
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	36.47
Std Dev	3.155

**Gaus mean : 38.4752**

**Gaus Width: 4.2097**



# B0L001S, U21-ch96, adc2

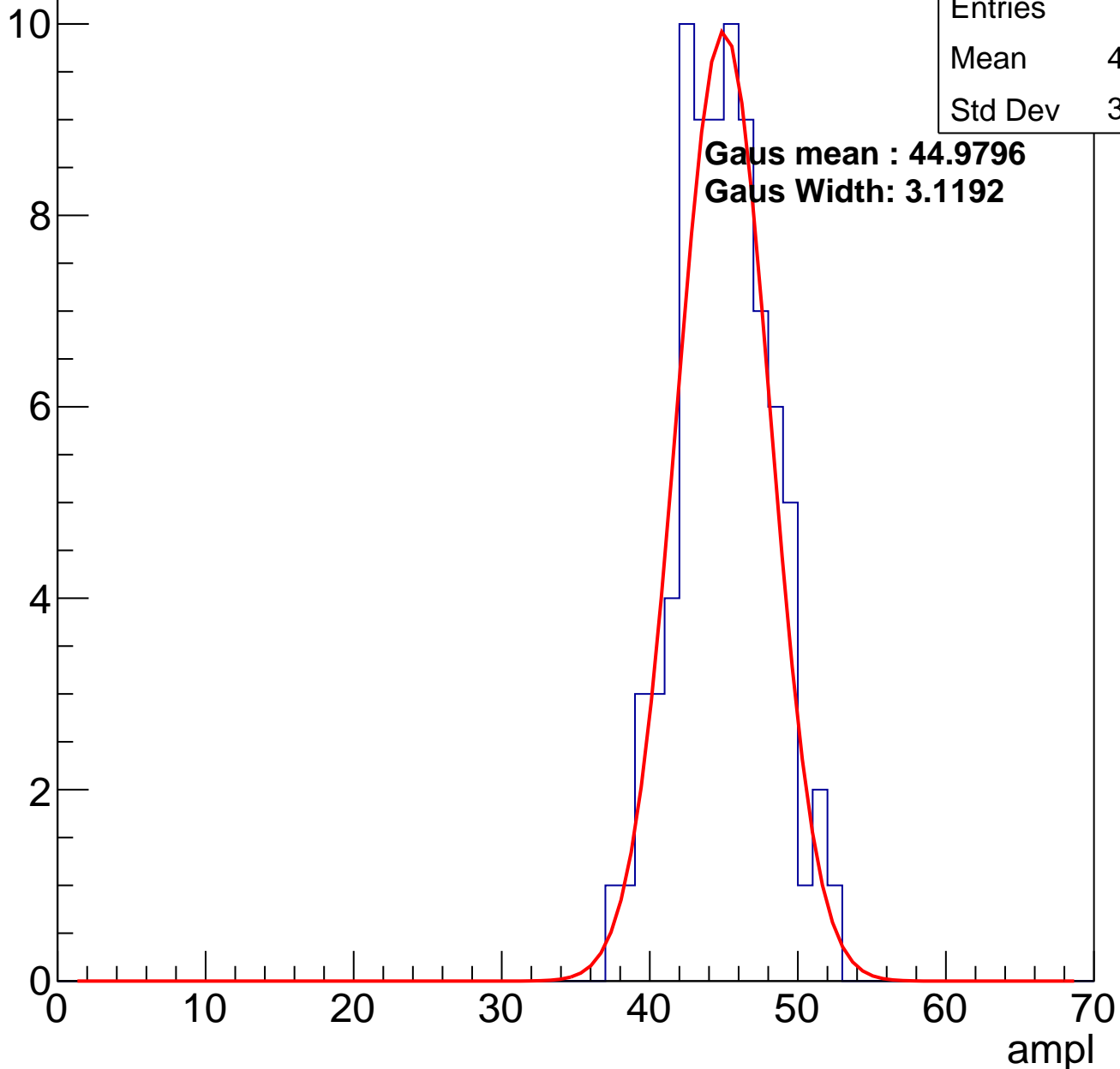
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	81
Mean	44.56
Std Dev	3.135

**Gaus mean : 44.9796**

**Gaus Width: 3.1192**

Entry

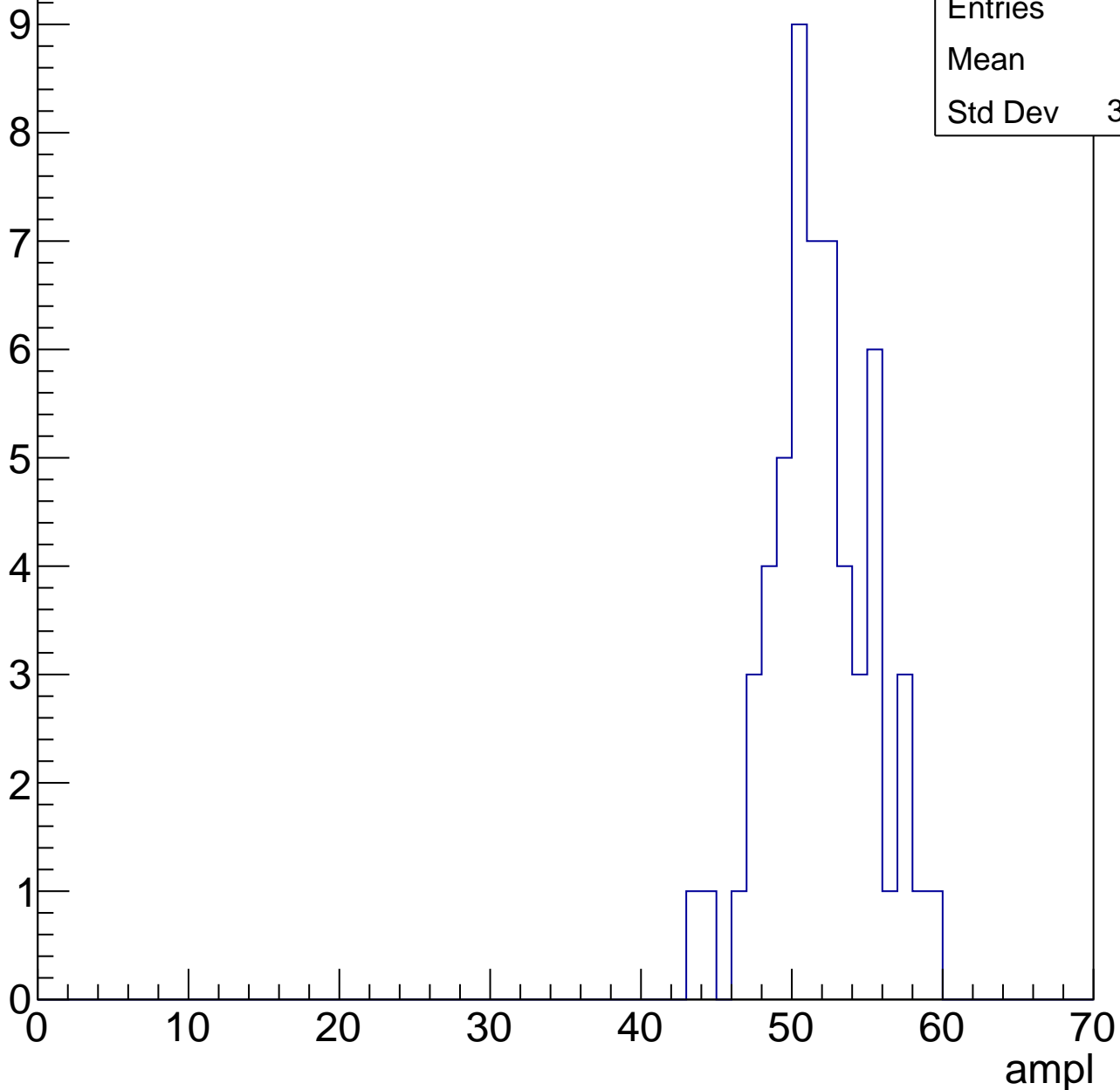


# B0L001S, U21-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	51.4
Std Dev	3.334

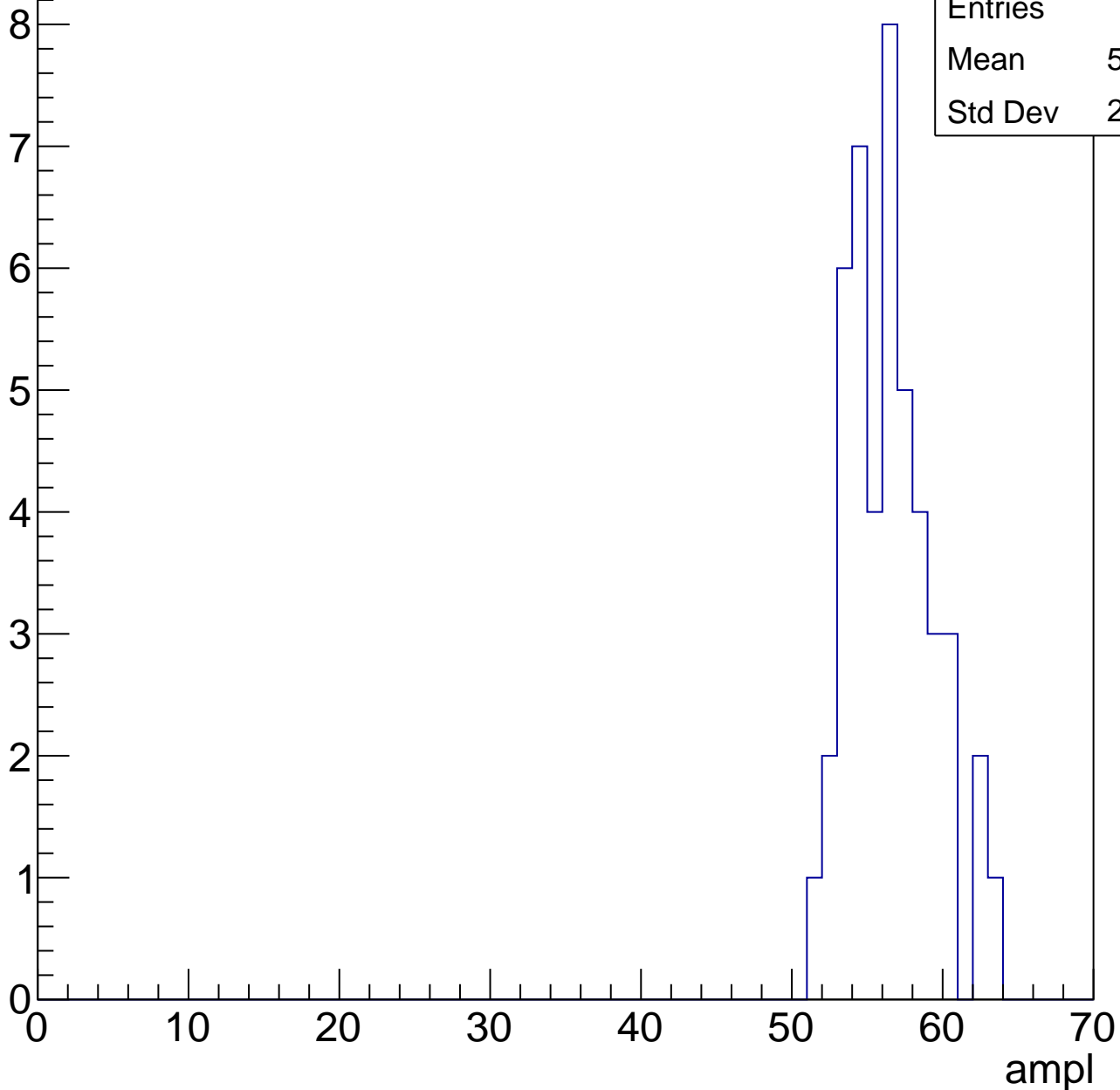


# B0L001S, U21-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	56.09
Std Dev	2.796

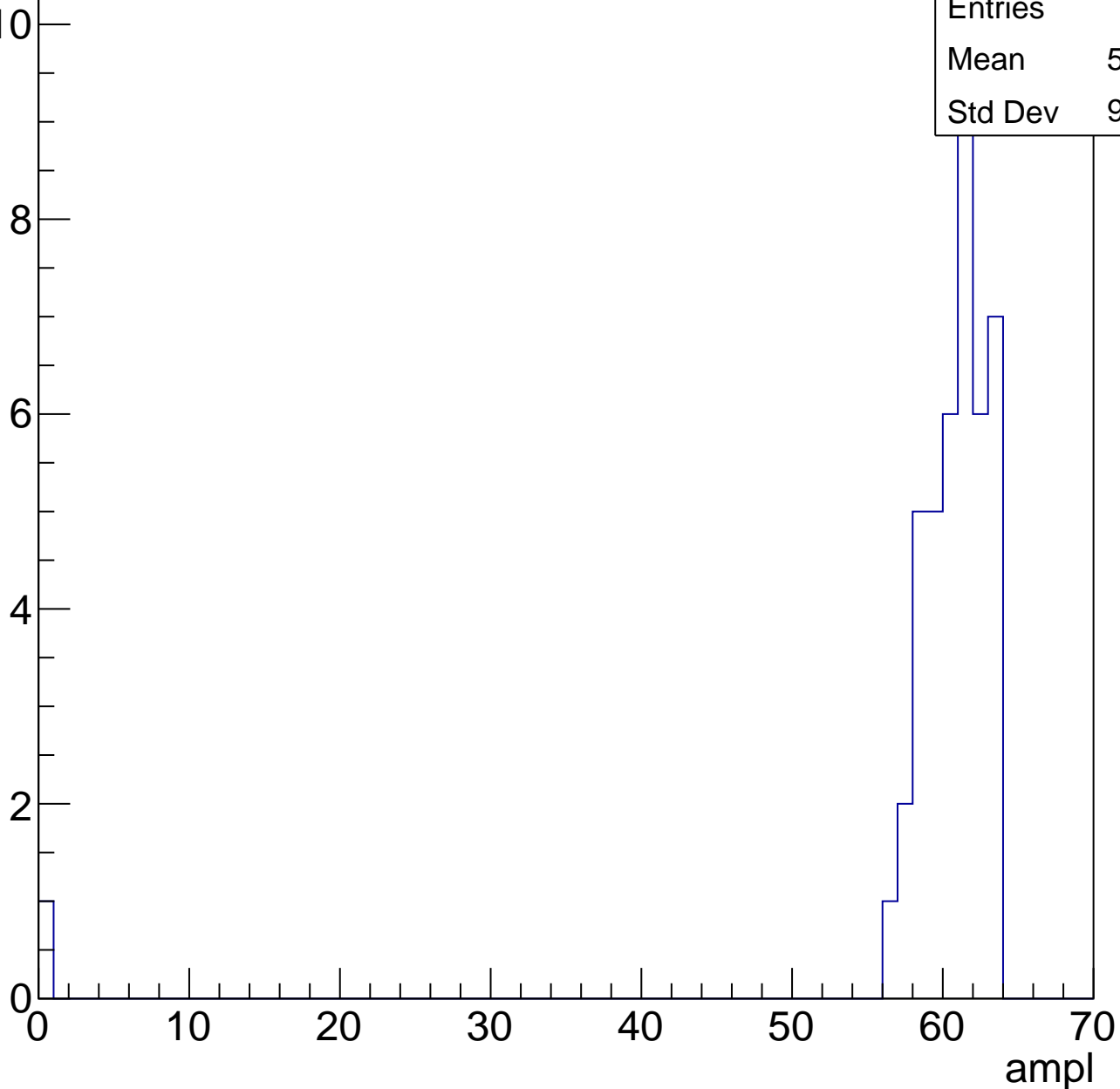


# B0L001S, U21-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

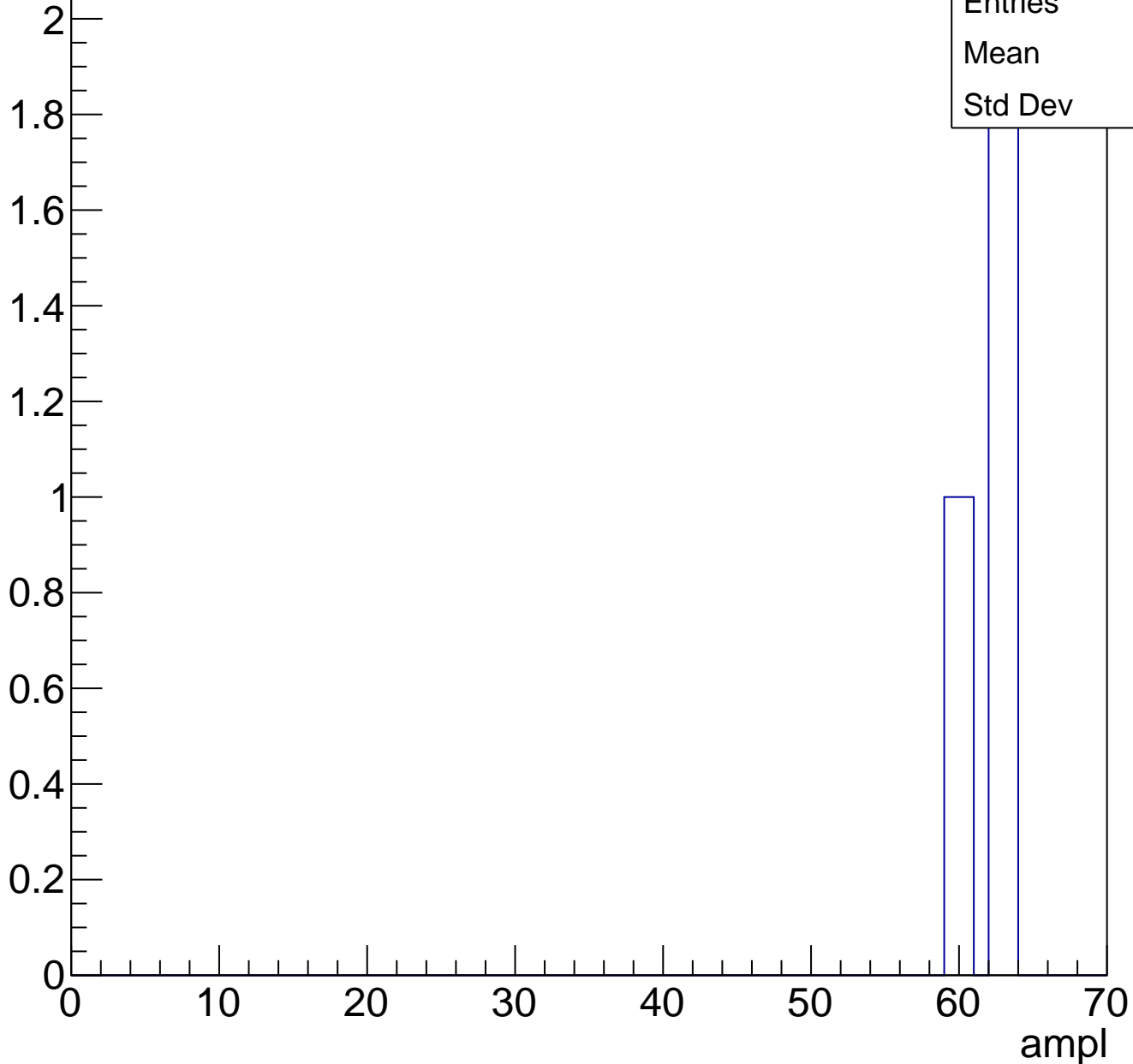
Entries	43
Mean	59.02
Std Dev	9.295



# B0L001S, U21-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U21-ch97, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	82
Mean	31.26
Std Dev	3.679

**Gaus mean : 31.5756**

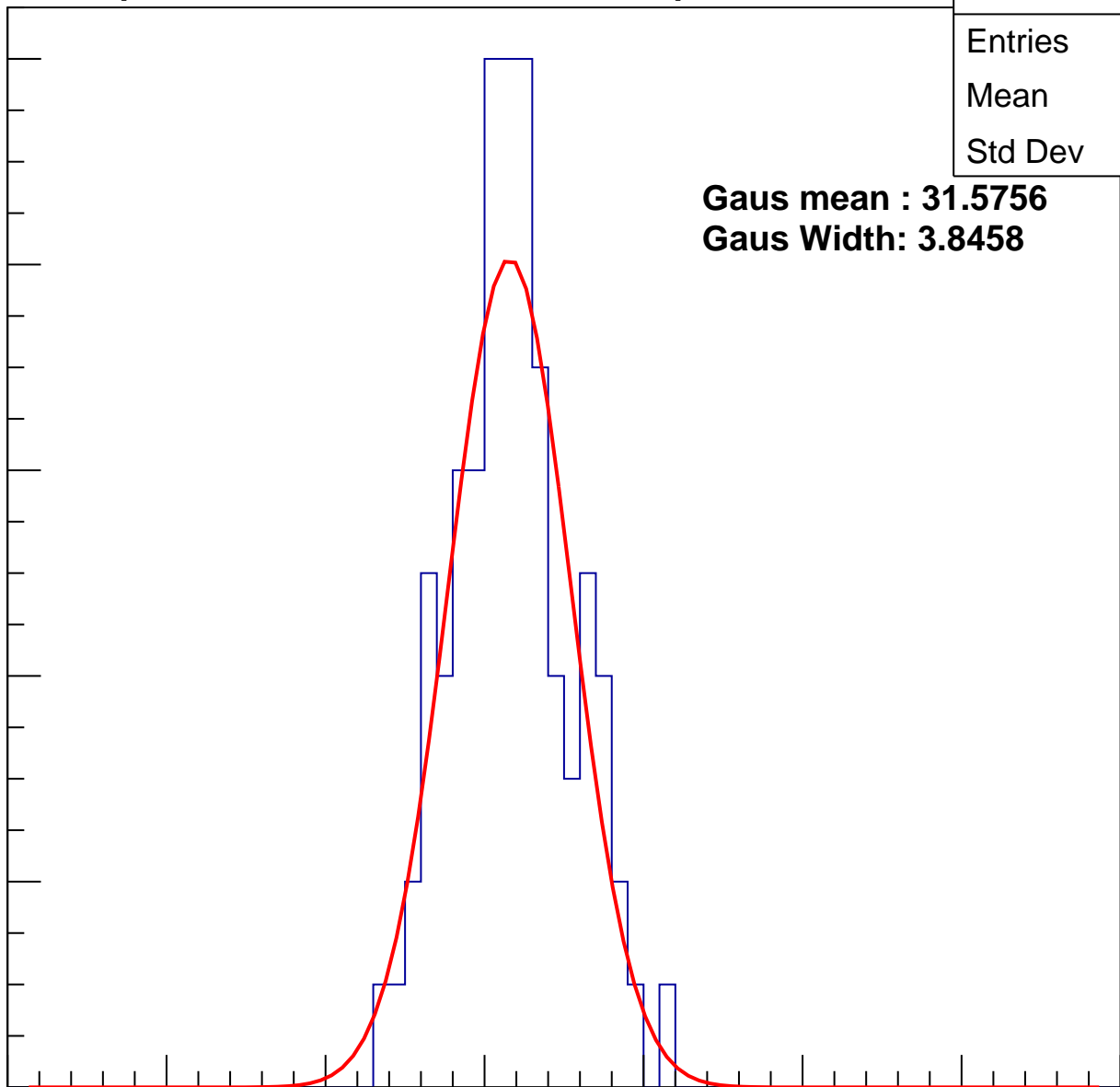
**Gaus Width: 3.8458**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



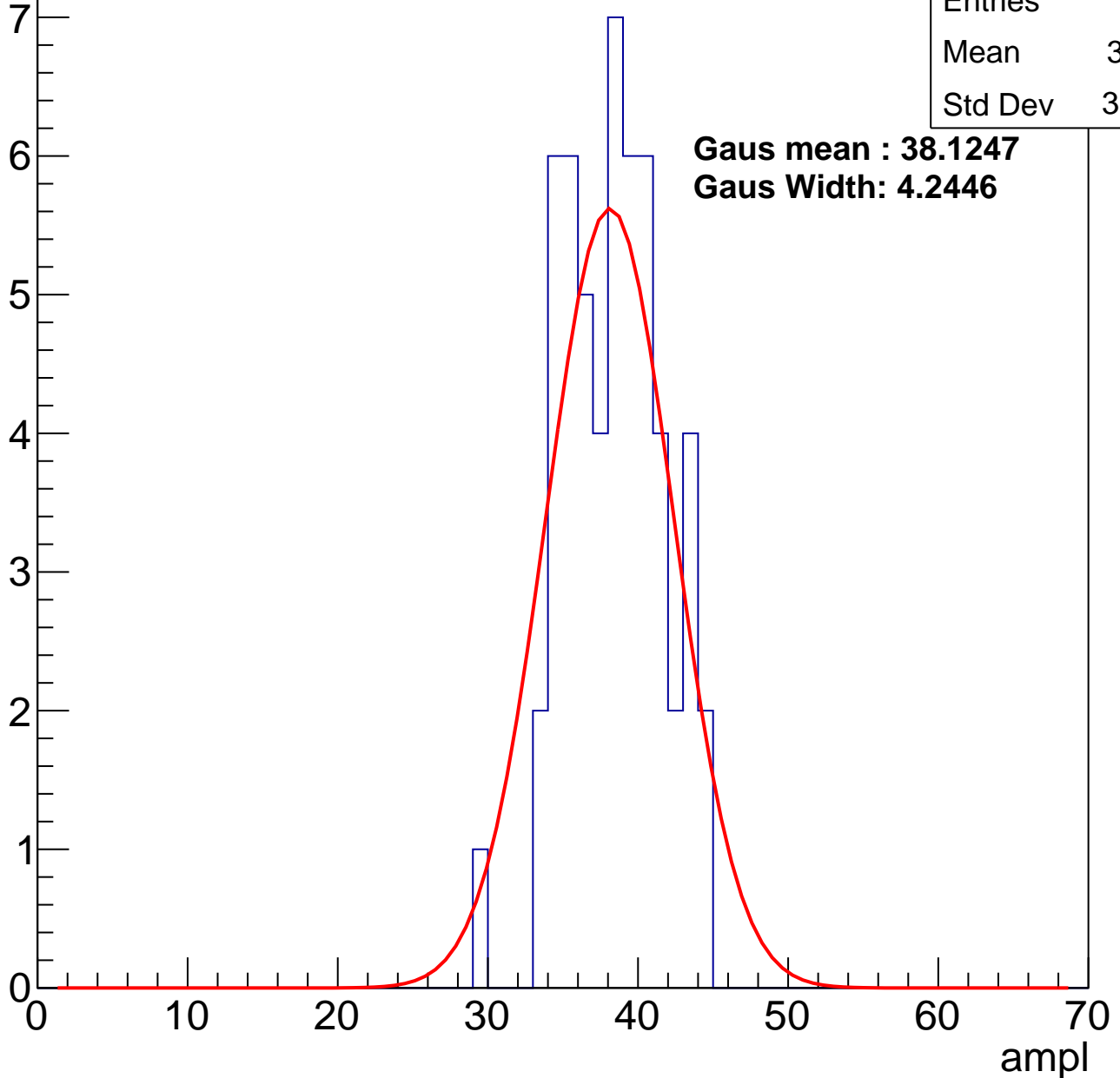
# B0L001S, U21-ch97, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	37.91
Std Dev	3.232

**Gaus mean : 38.1247**  
**Gaus Width: 4.2446**



# B0L001S, U21-ch97, adc2

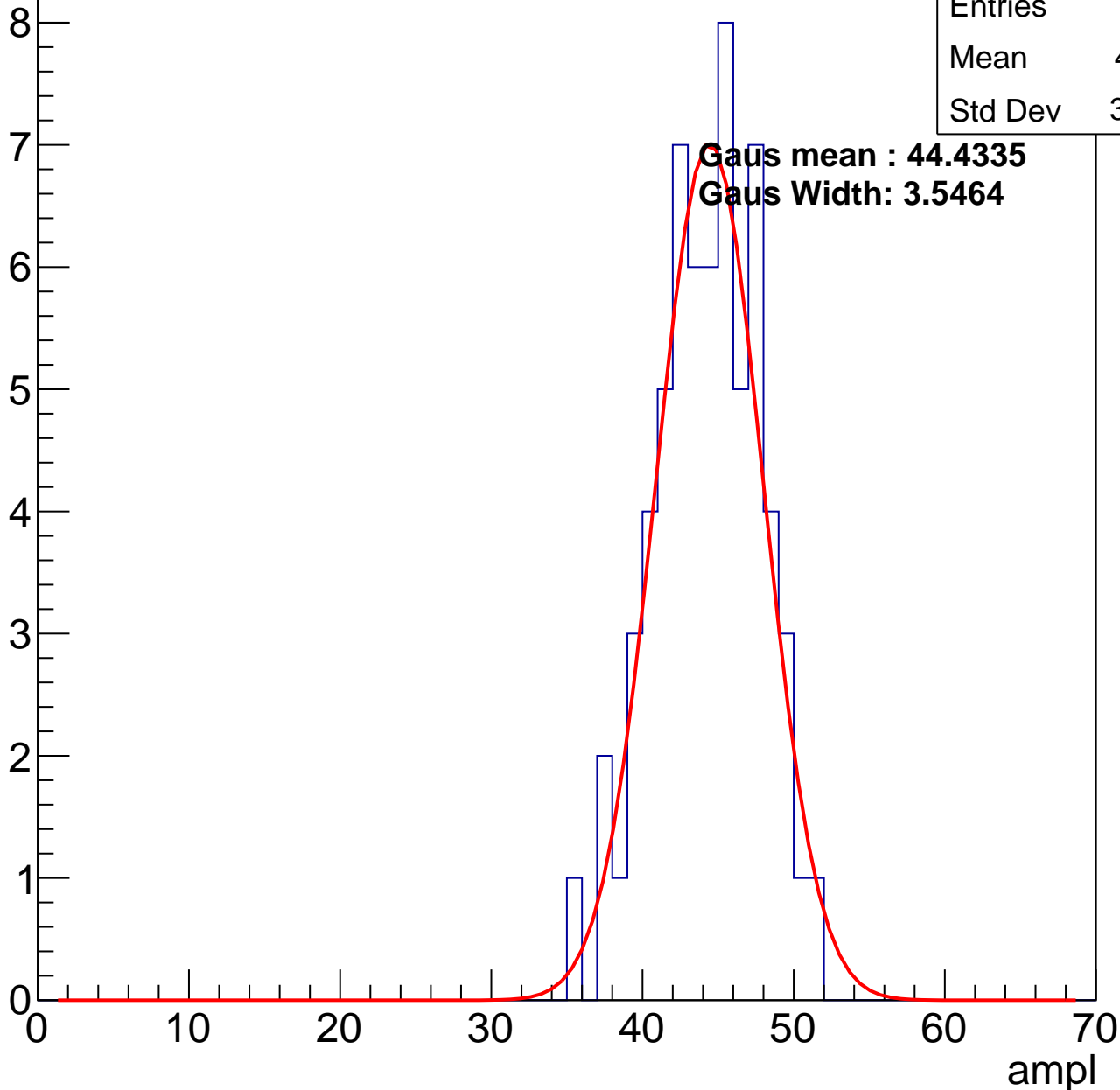
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	43.81
Std Dev	3.414

**Gaus mean : 44.4335**

**Gaus Width: 3.5464**

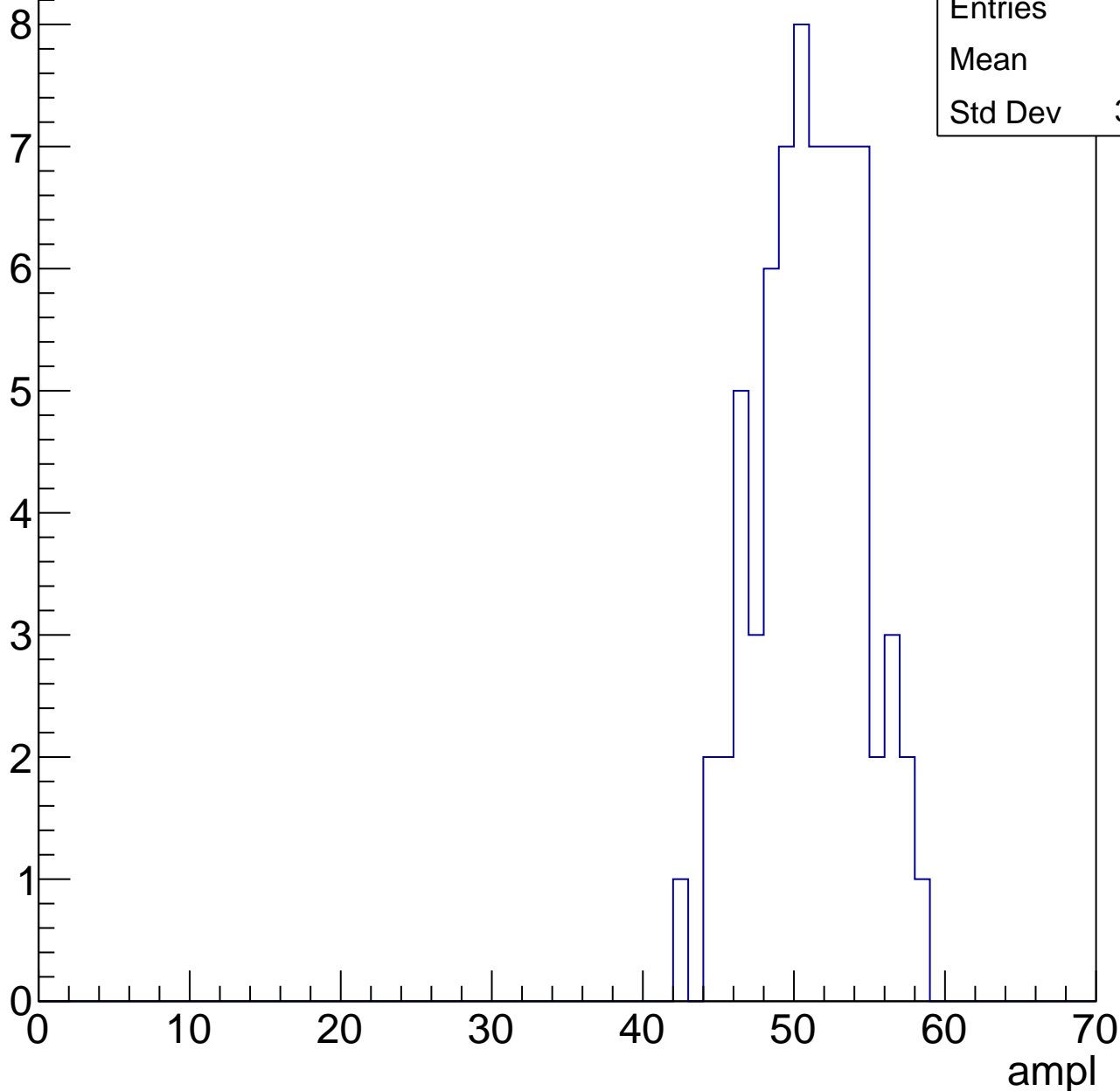


# B0L001S, U21-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	50.6
Std Dev	3.441

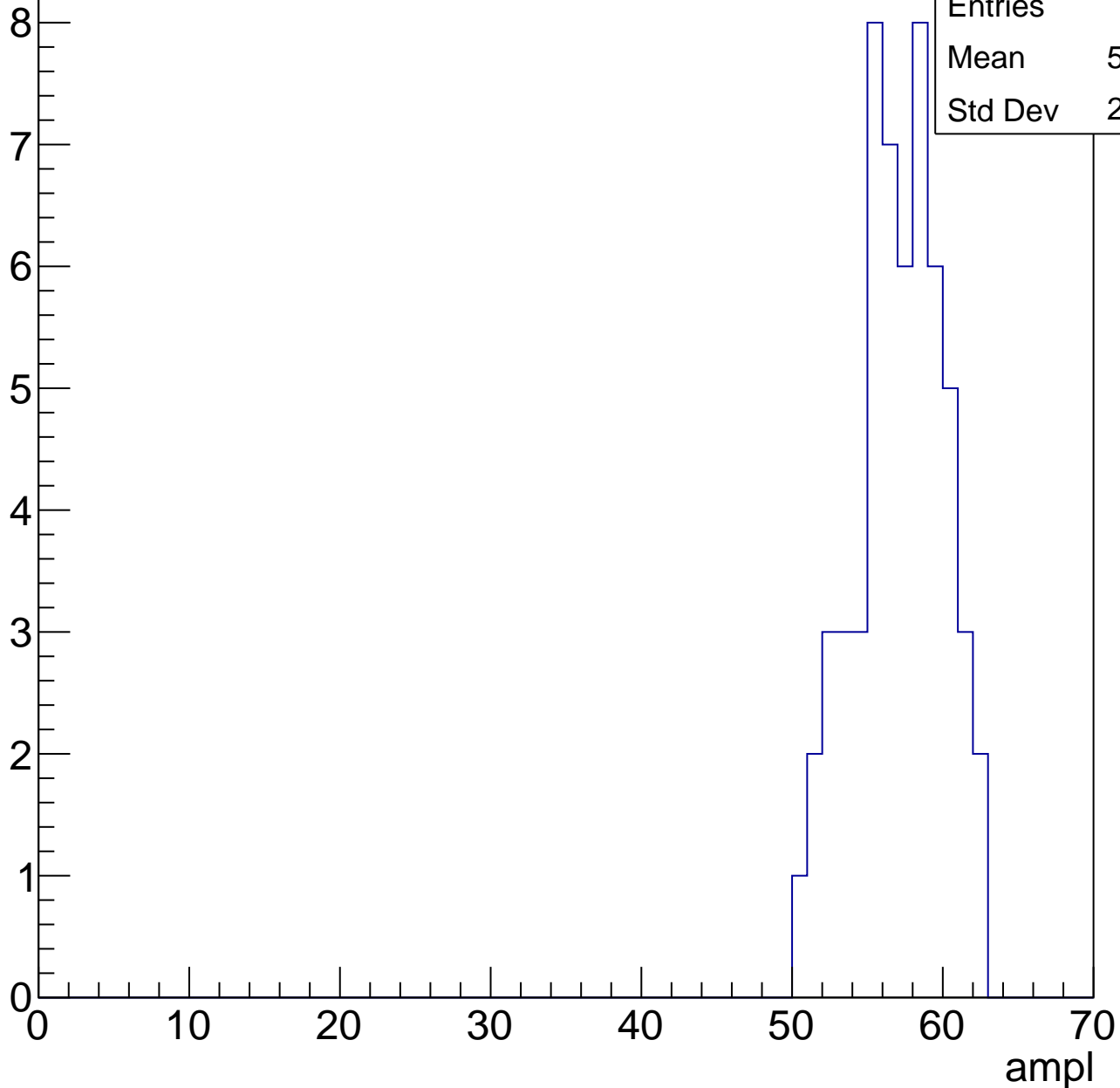


# B0L001S, U21-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	56.63
Std Dev	2.894

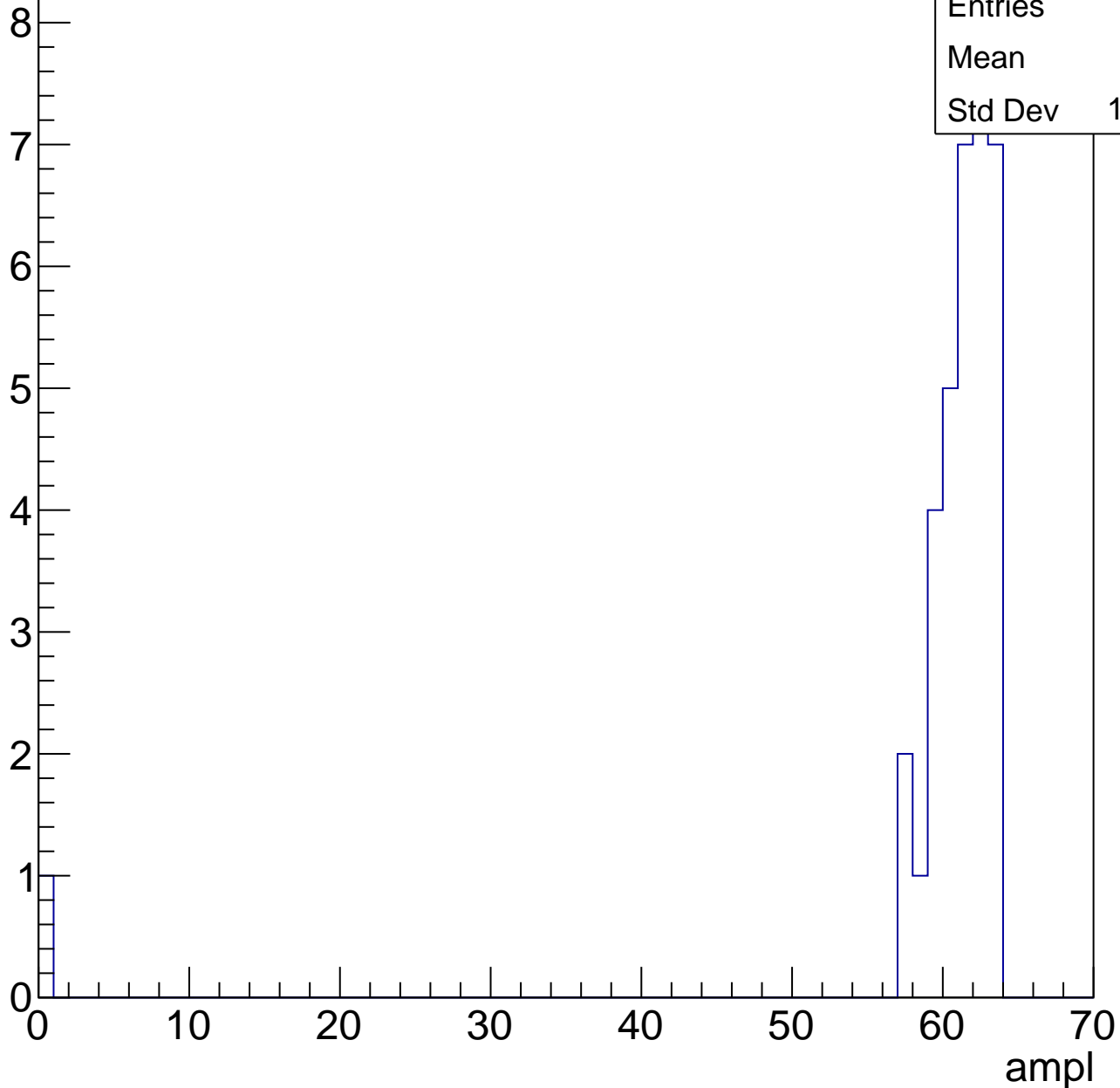


# B0L001S, U21-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	35
Mean	59.2
Std Dev	10.29



# B0L001S, U21-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

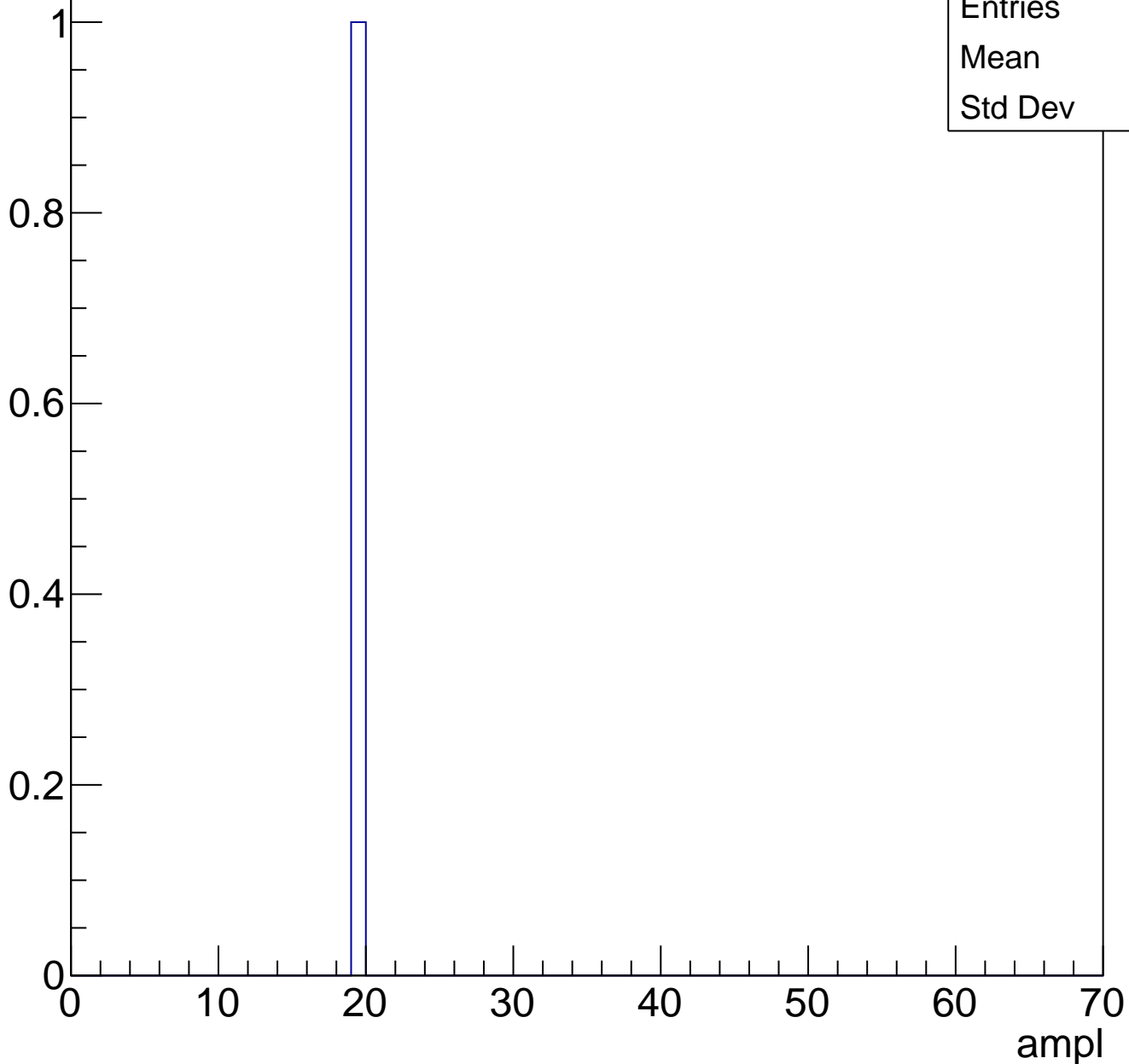




# B0L001S, U21-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch98, adc0

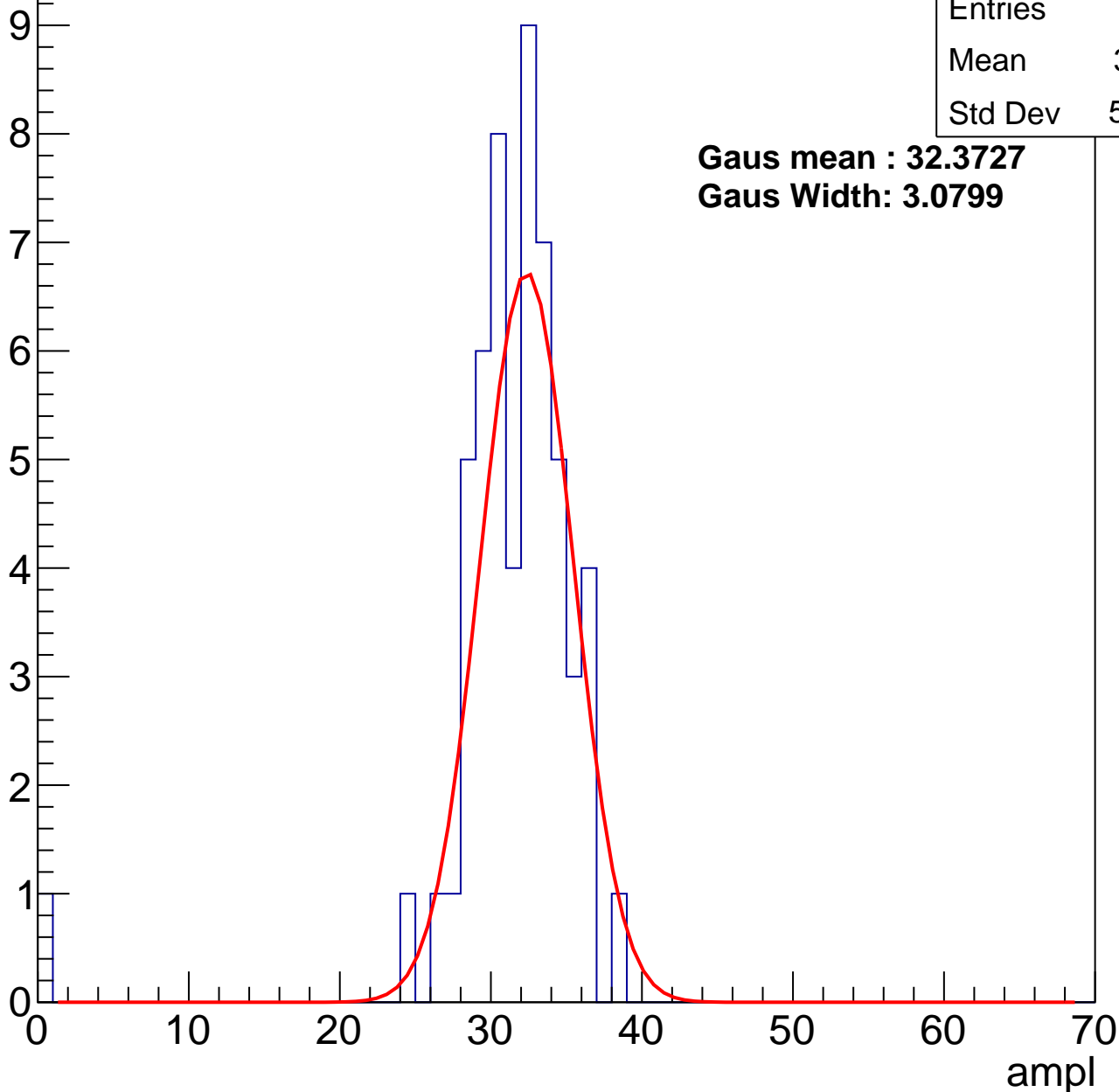
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	30.91
Std Dev	5.012

**Gaus mean : 32.3727**

**Gaus Width: 3.0799**



# B0L001S, U21-ch98, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	67
Mean	38.54
Std Dev	3.542

**Gaus mean : 38.9367**

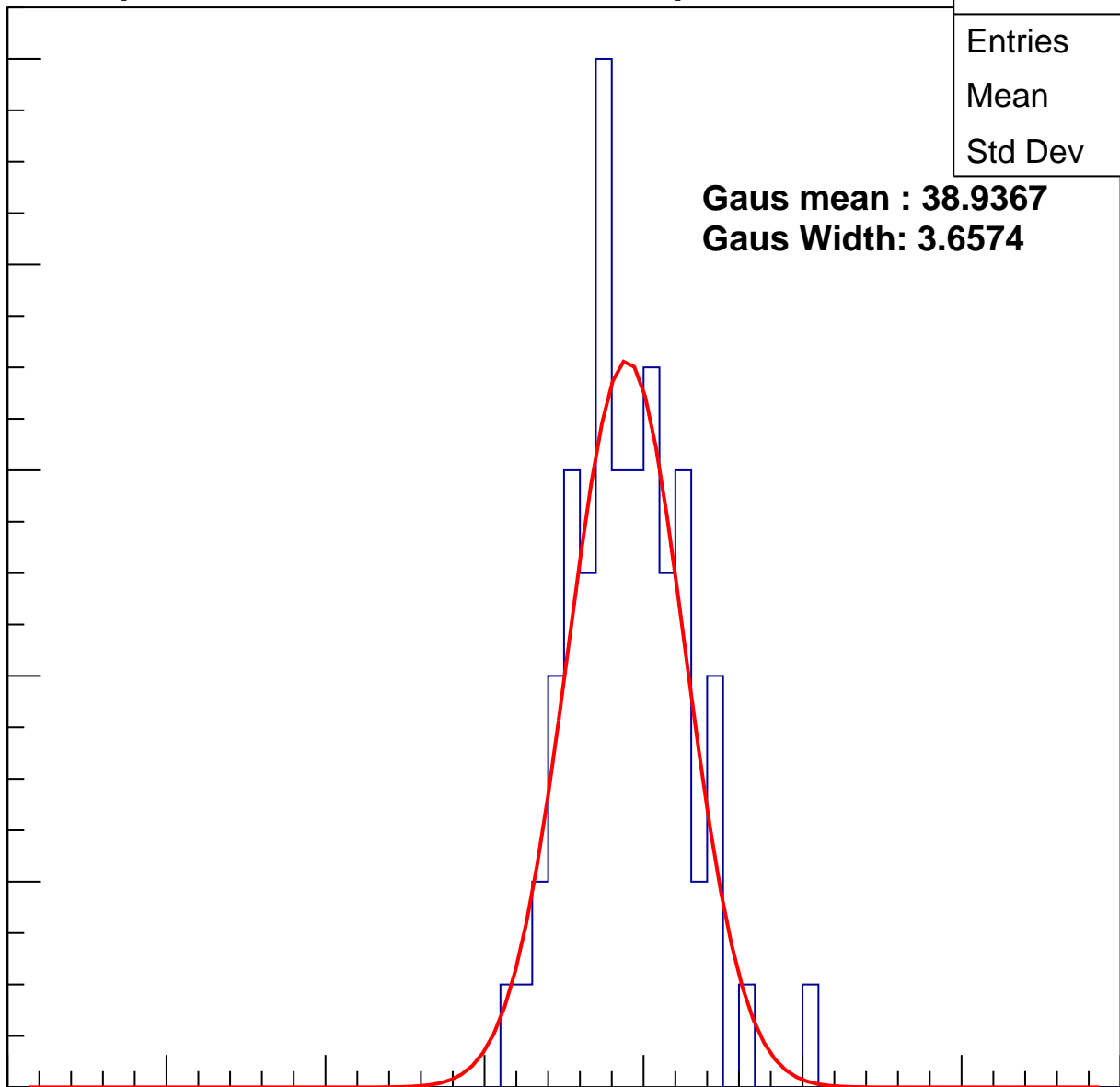
**Gaus Width: 3.6574**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U21-ch98, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	44.58
Std Dev	3.641

**Gaus mean : 45.1070**

**Gaus Width: 4.3966**

10

8

6

4

2

0

0

10

20

30

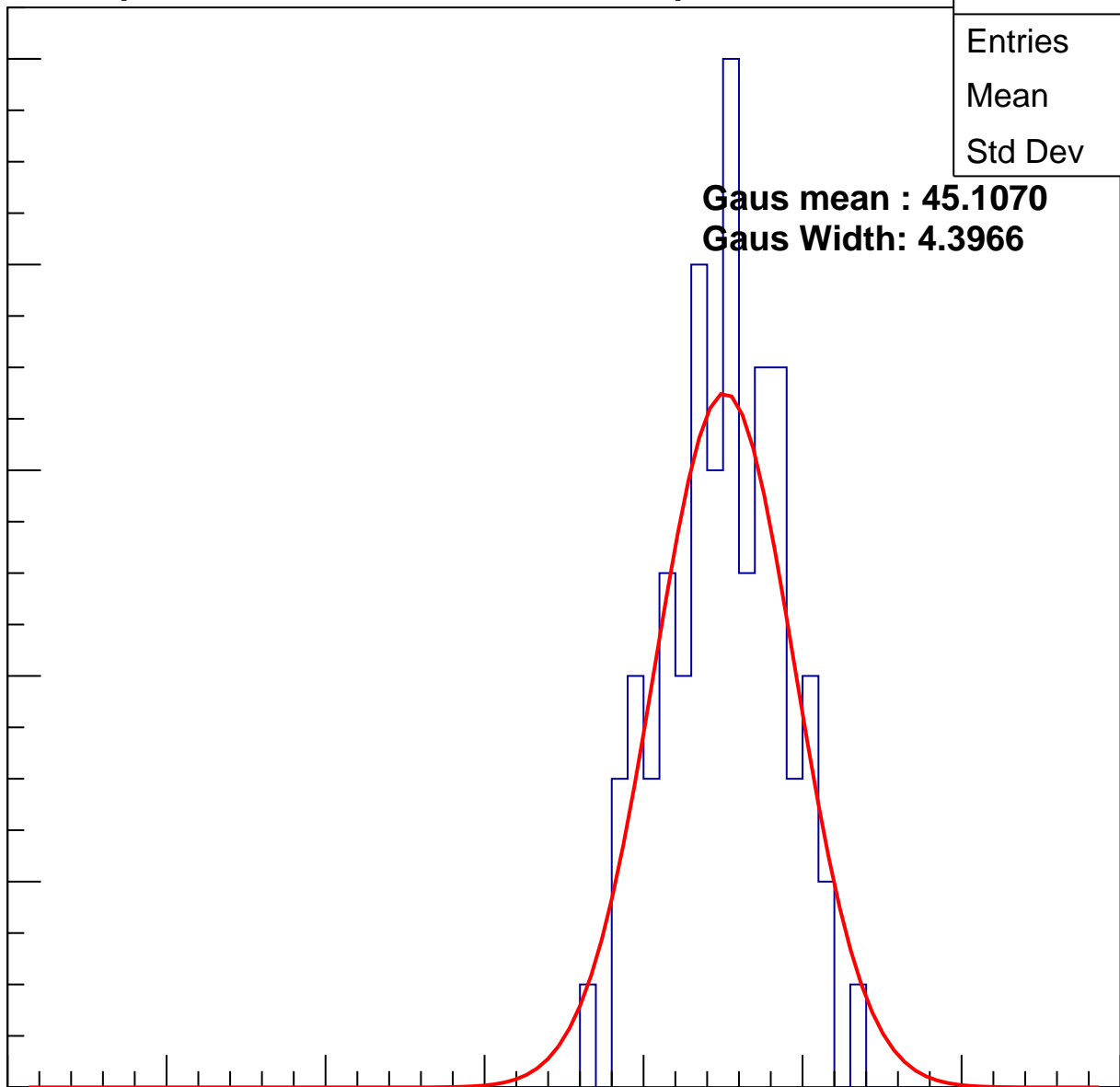
40

50

60

70

ampl

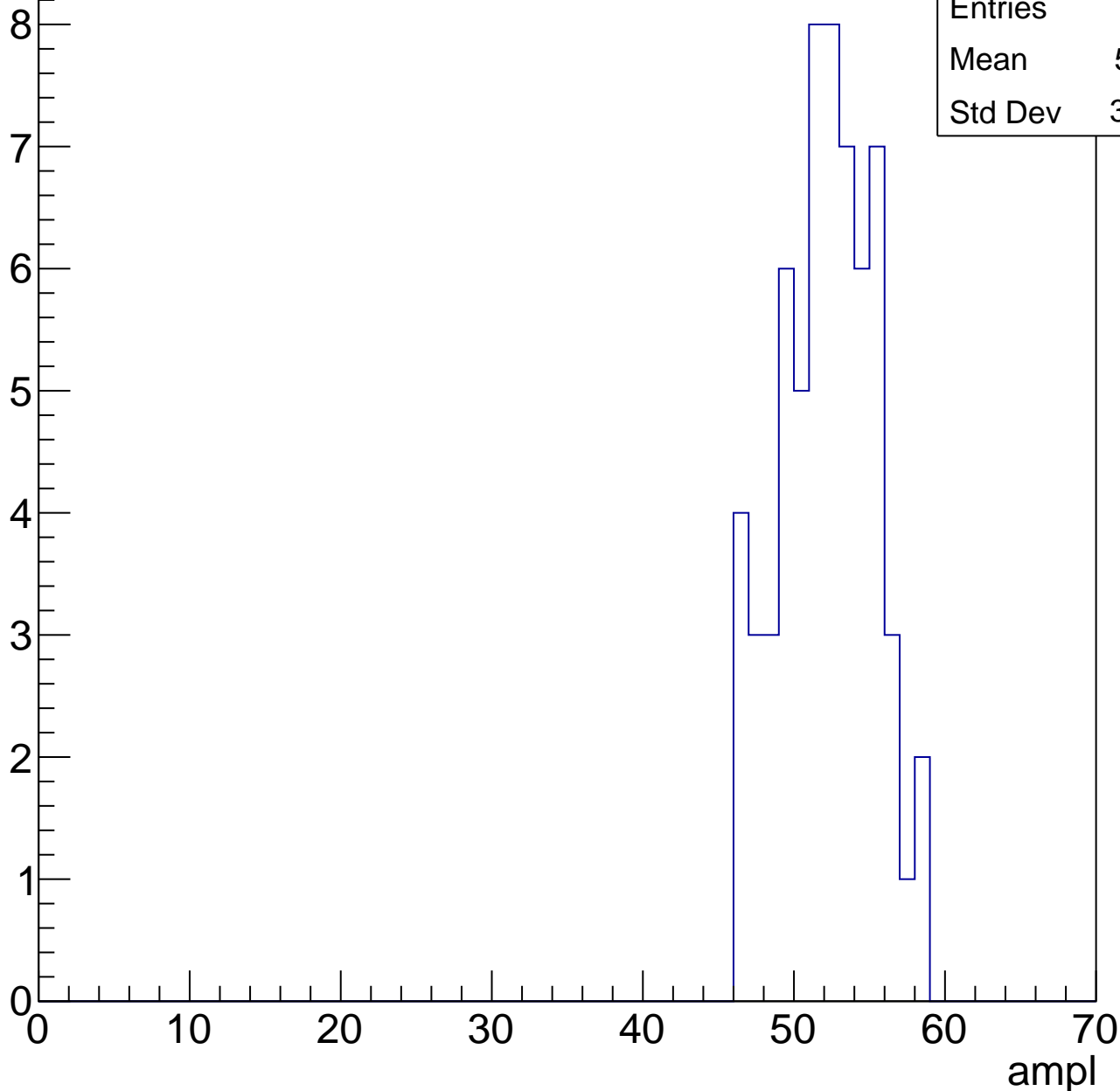


# B0L001S, U21-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	51.71
Std Dev	3.042

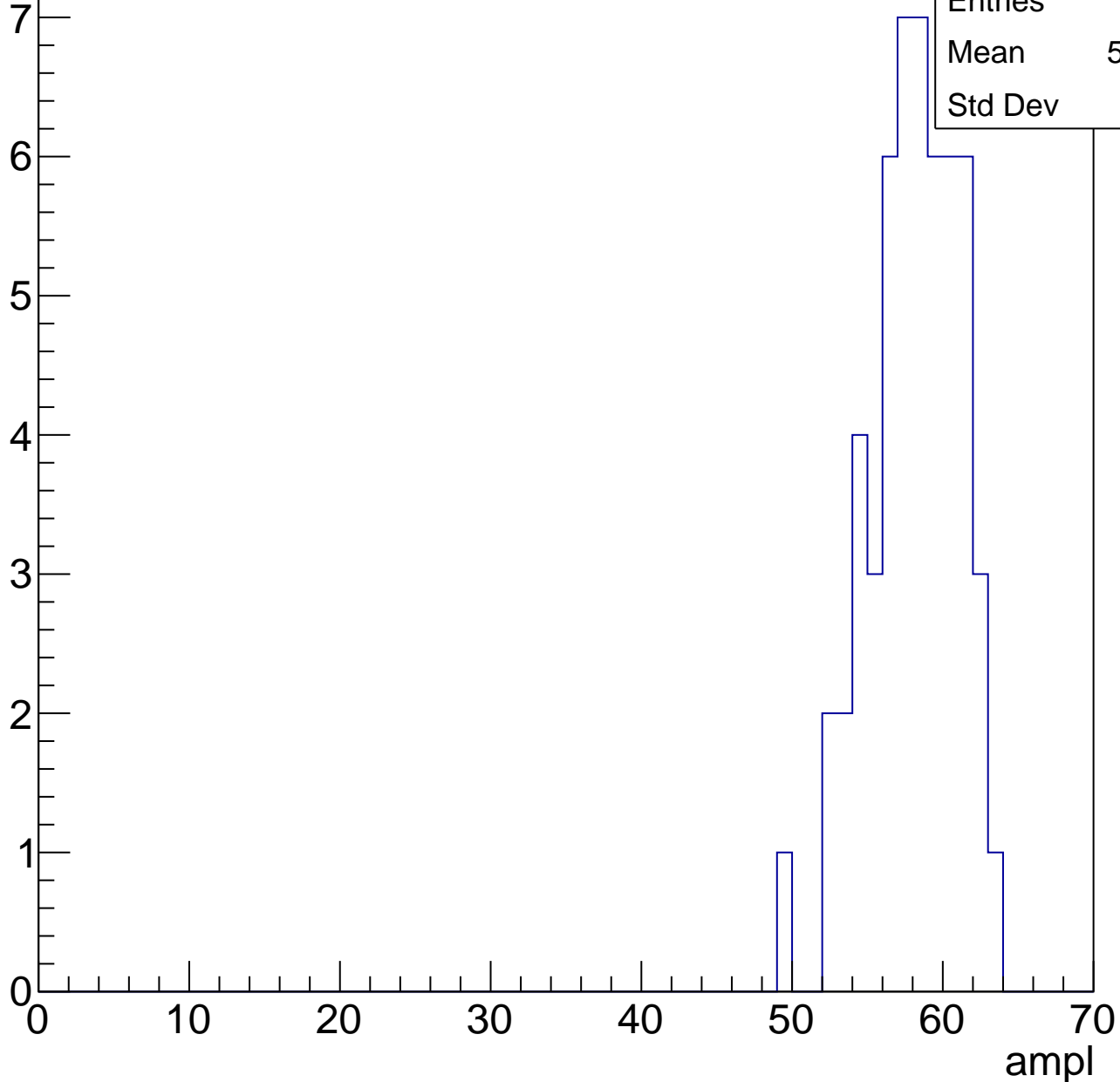


# B0L001S, U21-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	57.59
Std Dev	2.96

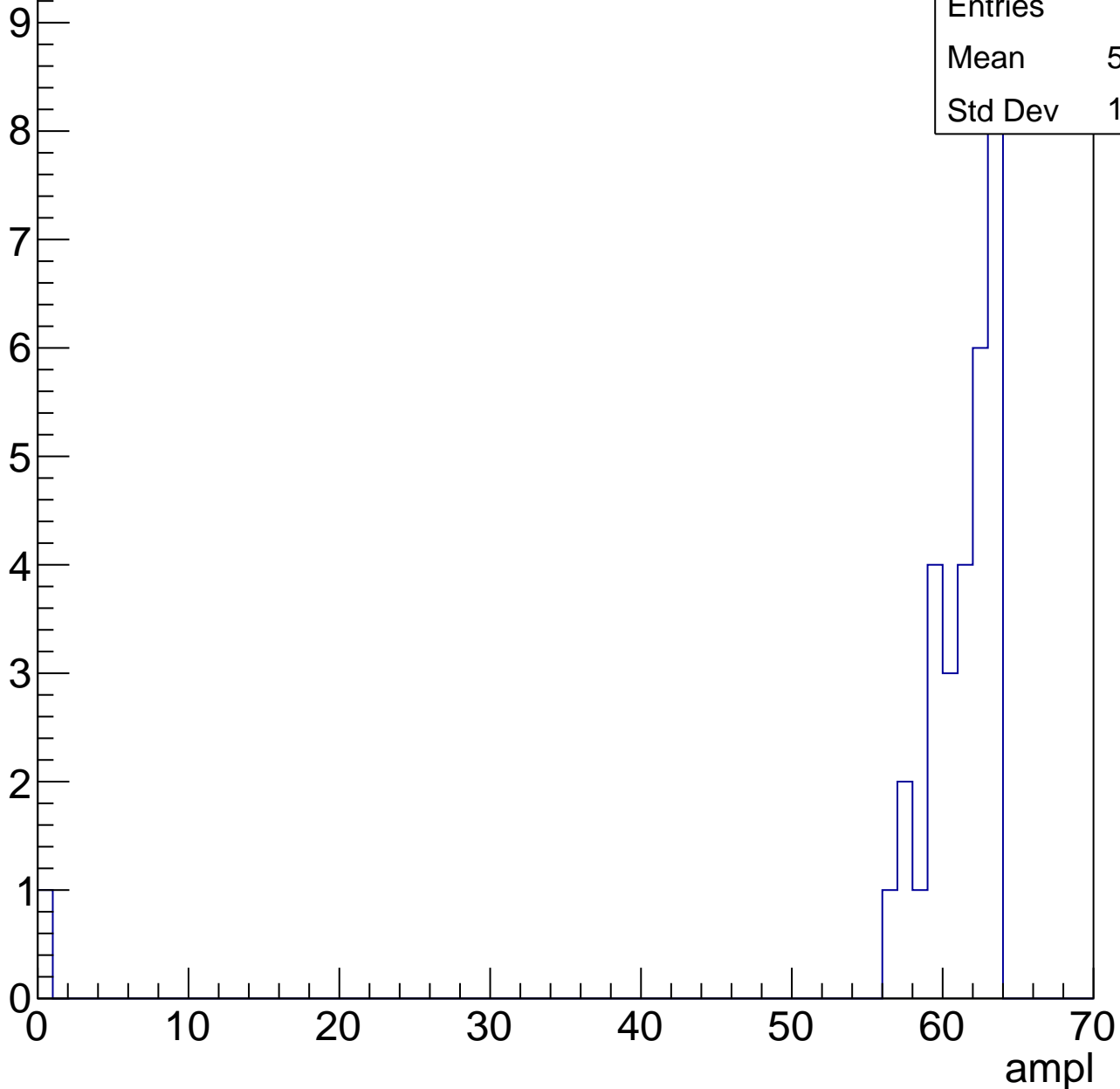


# B0L001S, U21-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	31
Mean	58.94
Std Dev	10.95



# B0L001S, U21-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch99, adc0

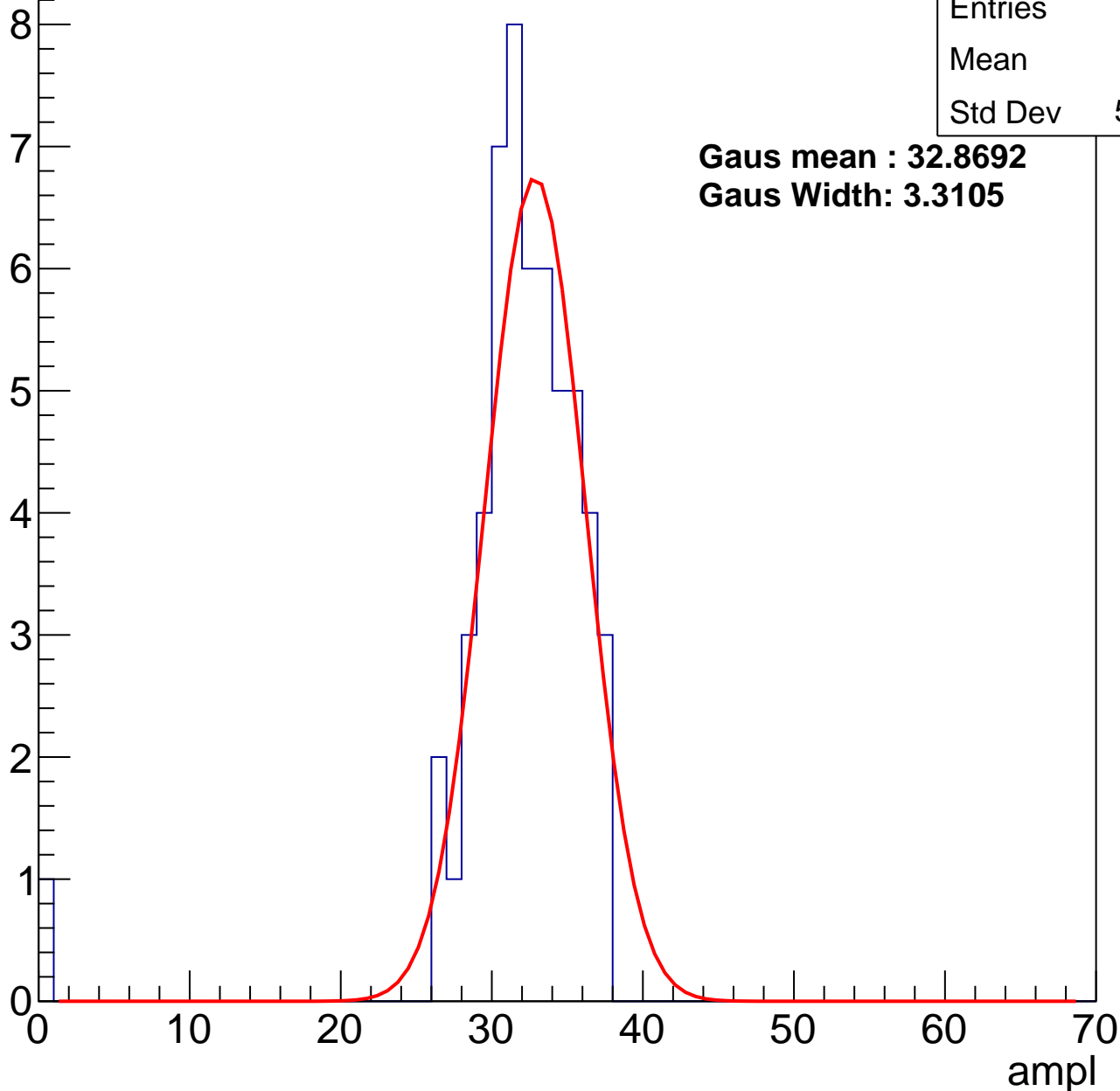
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	31.4
Std Dev	5.101

**Gaus mean : 32.8692**

**Gaus Width: 3.3105**



# B0L001S, U21-ch99, adc1

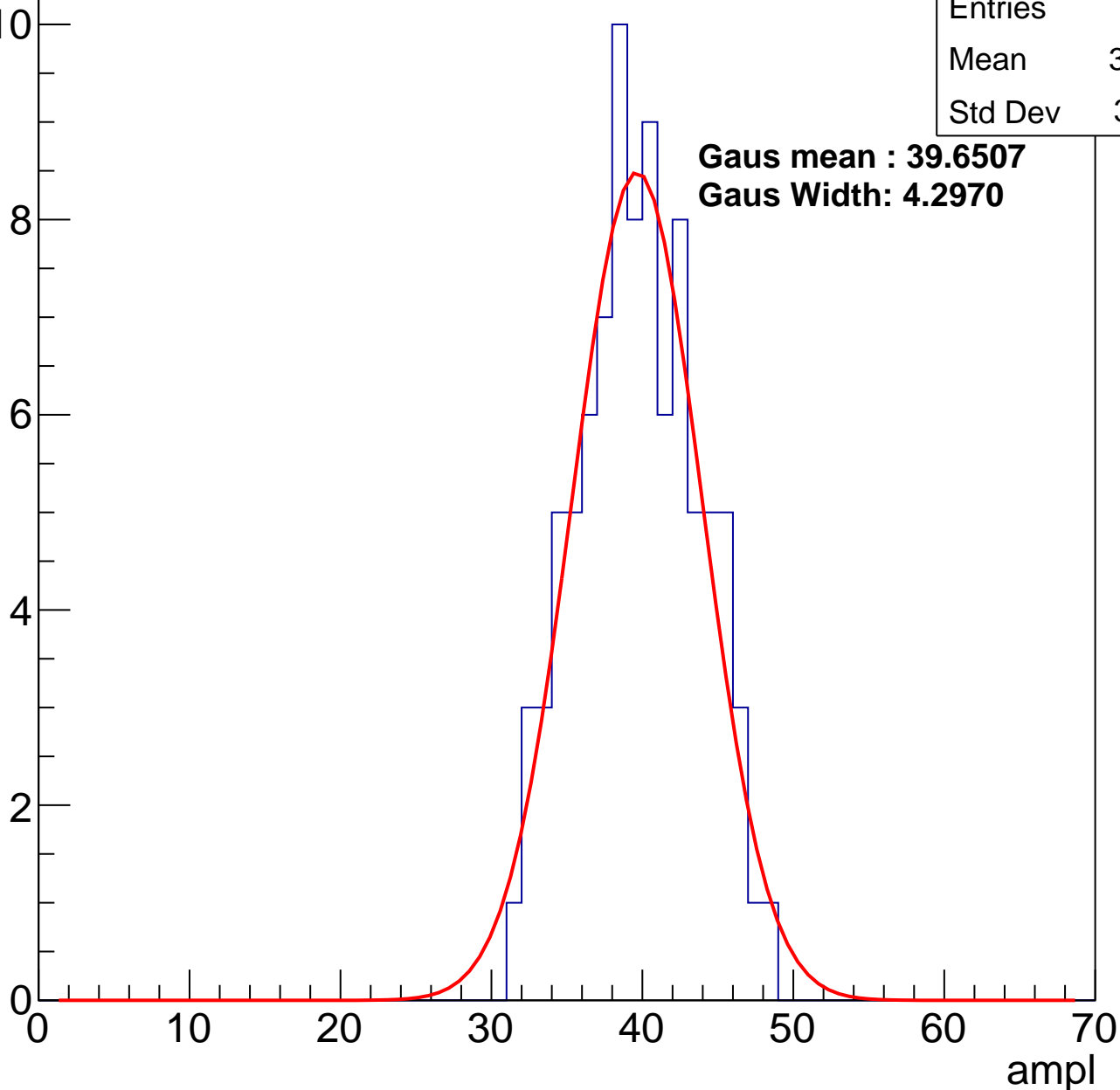
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	91
Mean	39.26
Std Dev	3.911

**Gaus mean : 39.6507**

**Gaus Width: 4.2970**



# B0L001S, U21-ch99, adc2

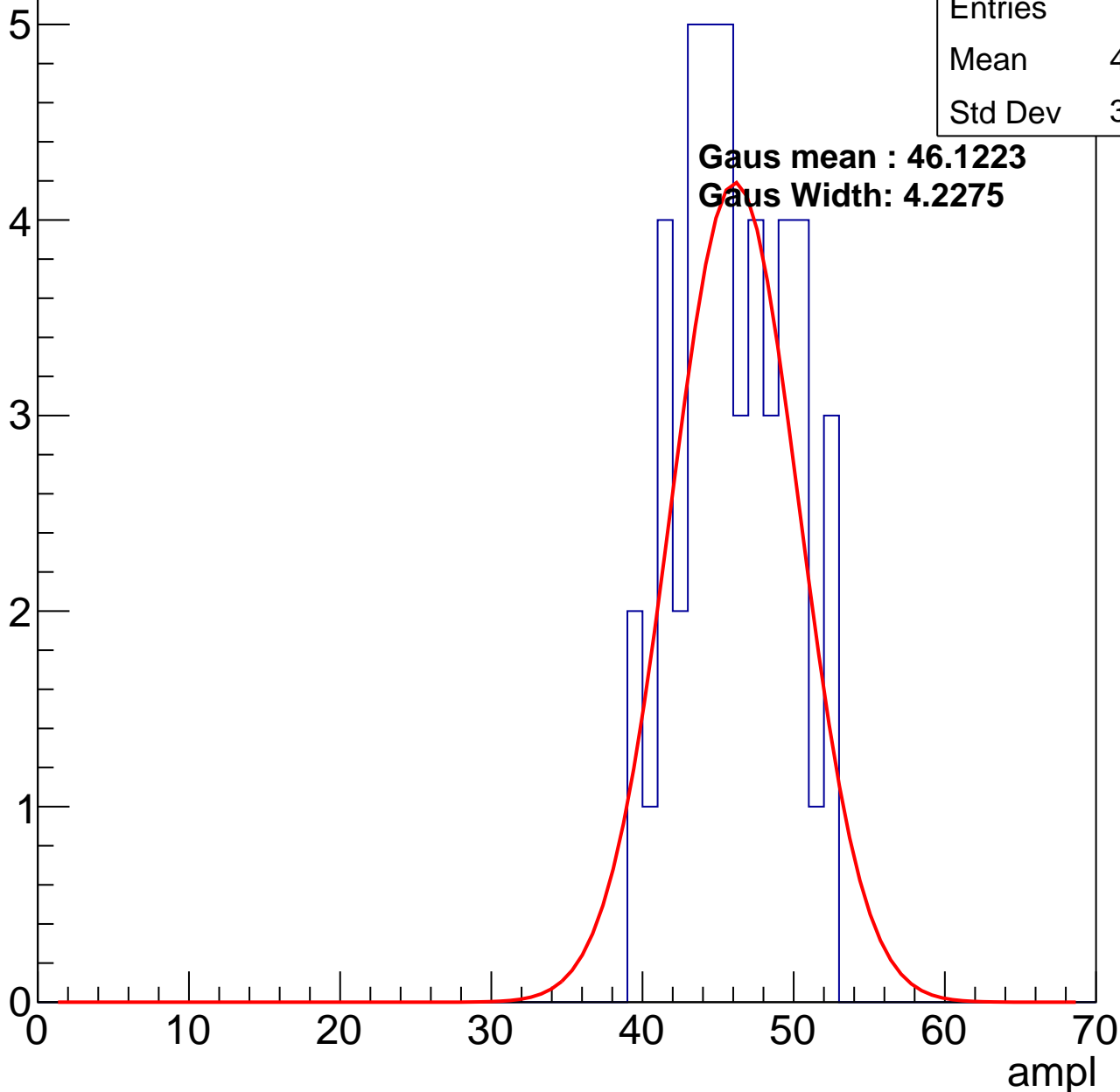
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	46
Mean	45.63
Std Dev	3.547

**Gaus mean : 46.1223**

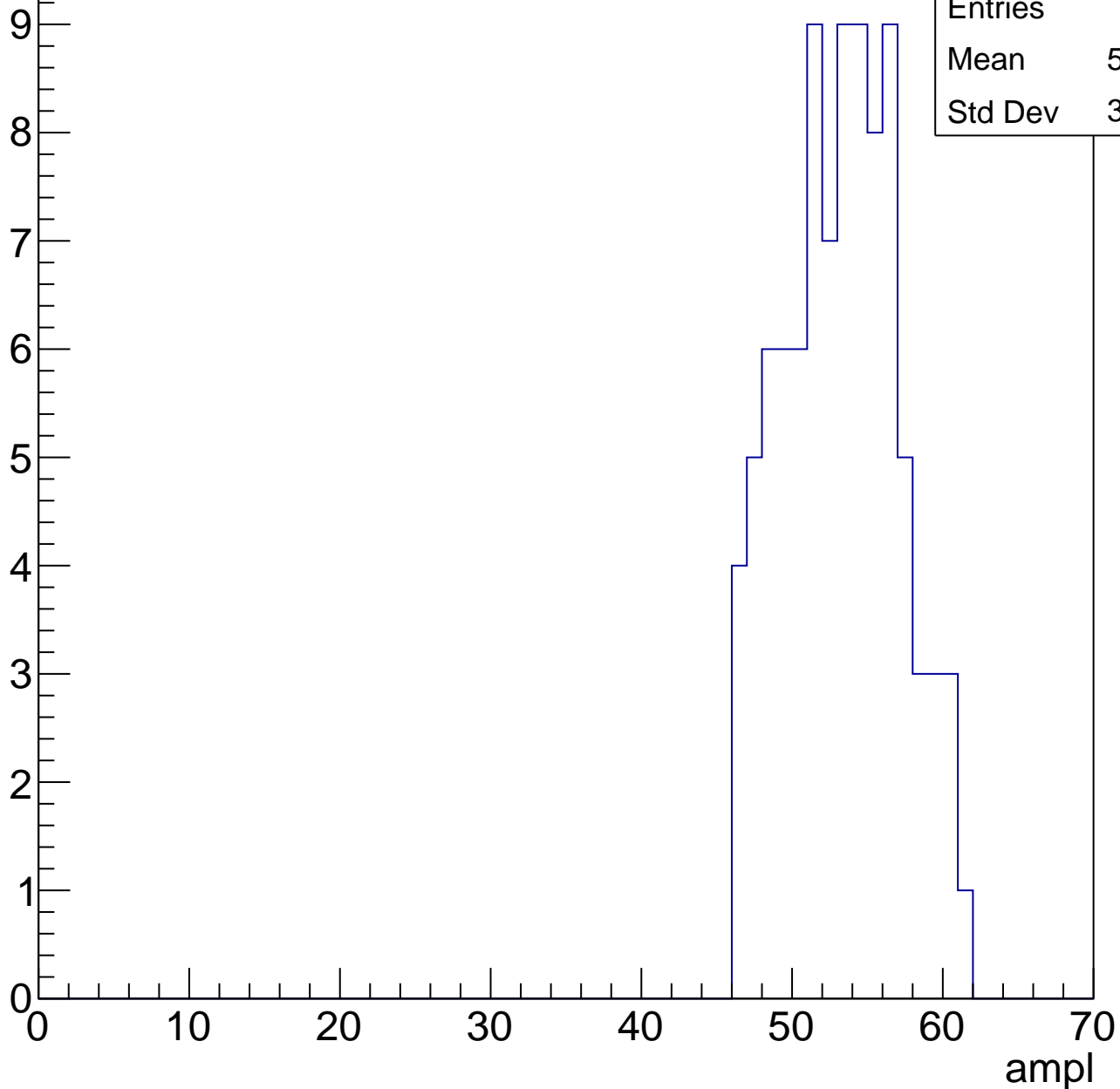
**Gaus Width: 4.2275**



# B0L001S, U21-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

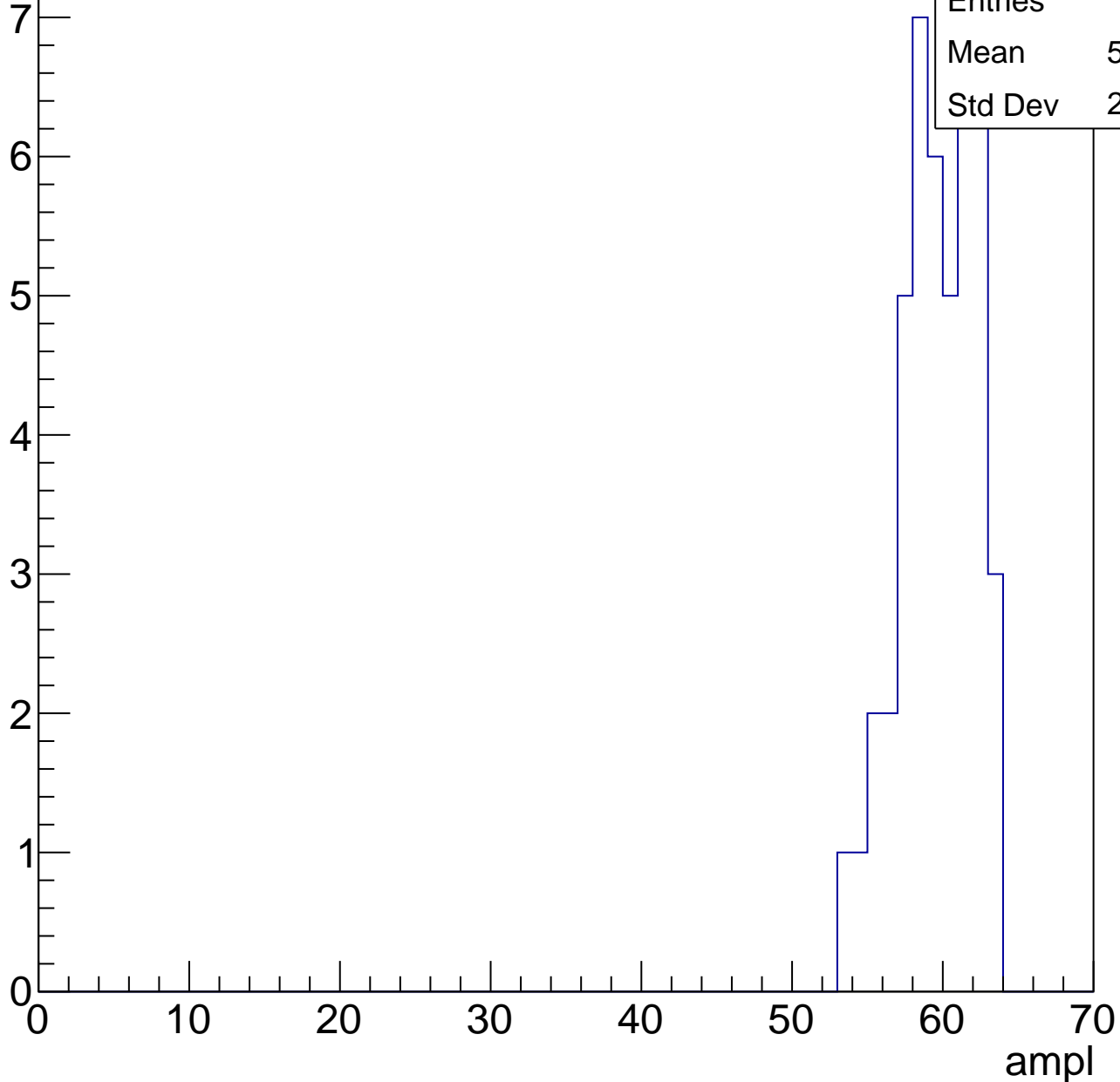


Entries	93
Mean	52.77
Std Dev	3.754

# B0L001S, U21-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

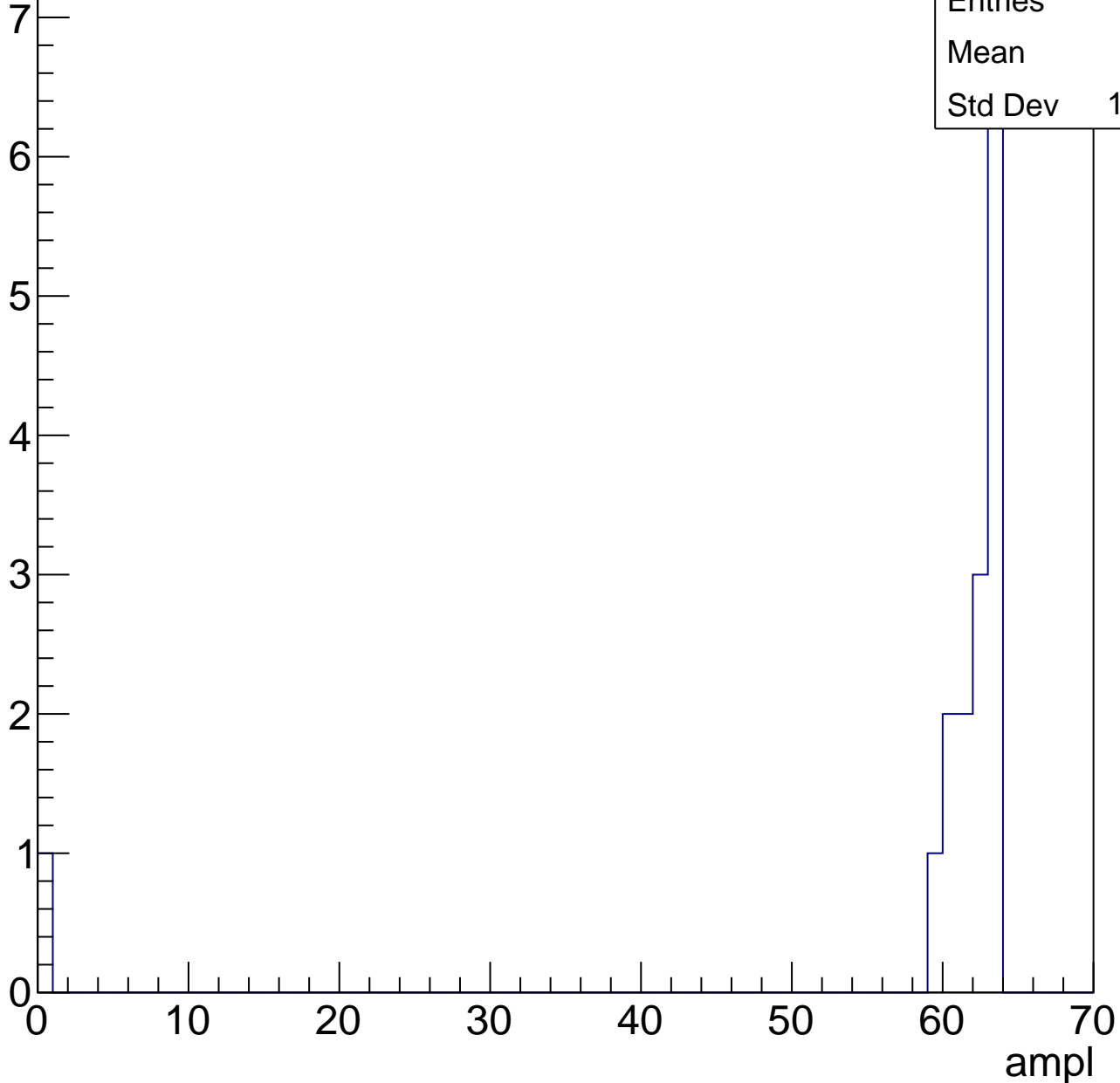


# B0L001S, U21-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	16
Mean	58
Std Dev	15.03



# B0L001S, U21-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U21-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch100, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	67
Mean	29.87
Std Dev	6.171

**Gaus mean : 30.4795**

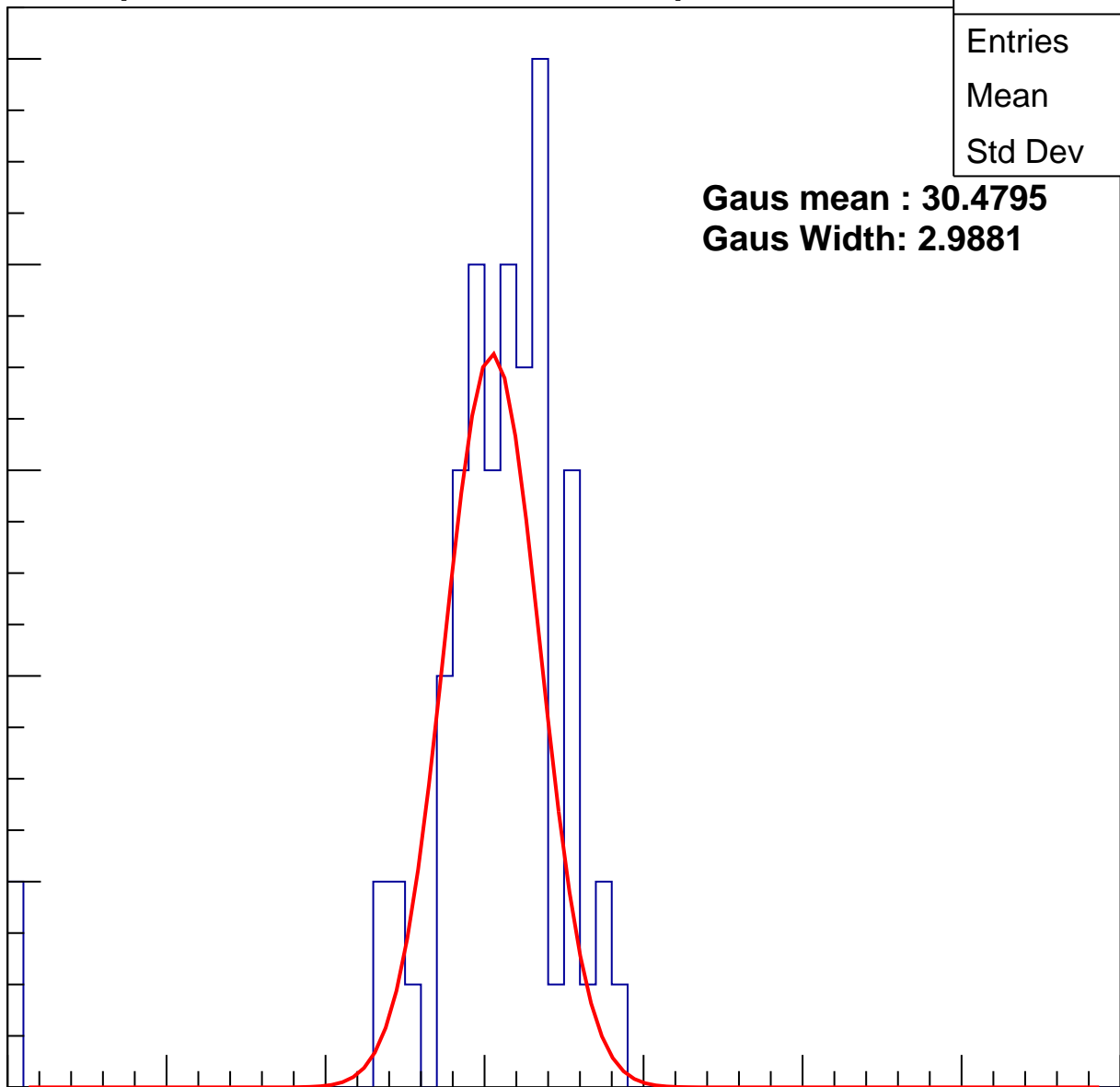
**Gaus Width: 2.9881**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U21-ch100, adc1

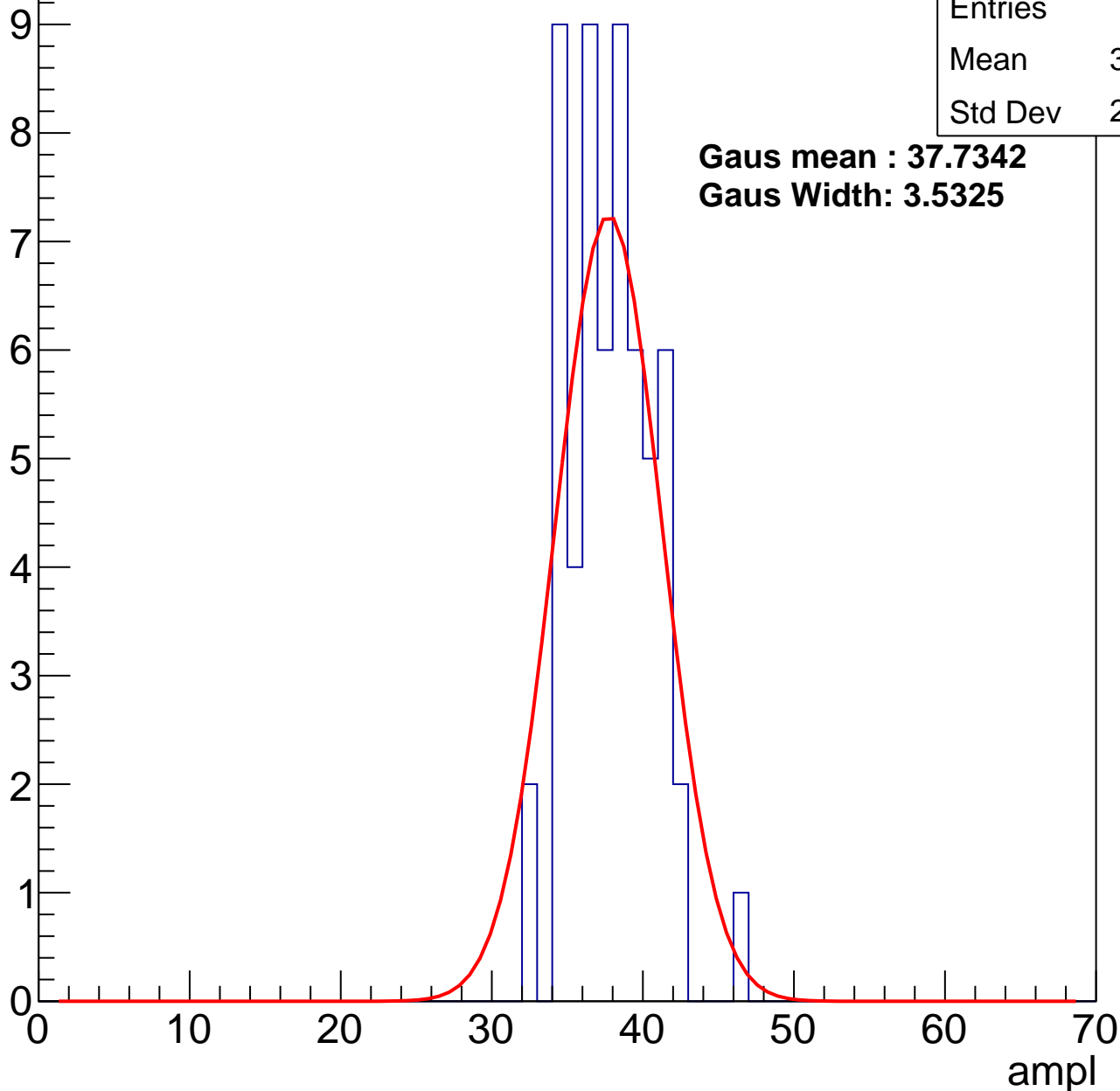
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	37.42
Std Dev	2.763

**Gaus mean : 37.7342**

**Gaus Width: 3.5325**



# B0L001S, U21-ch100, adc2

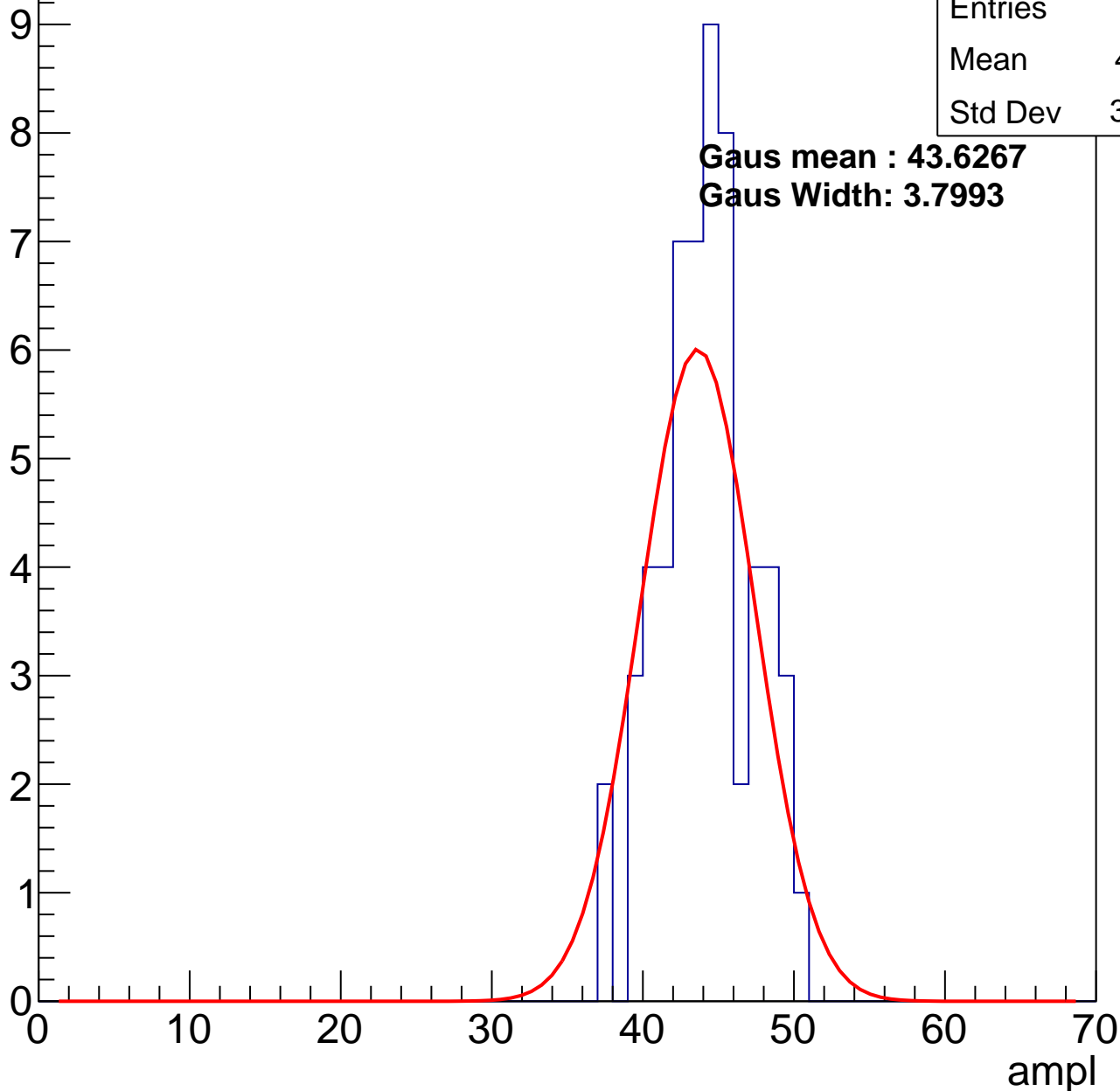
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	43.71
Std Dev	3.023

**Gaus mean : 43.6267**

**Gaus Width: 3.7993**

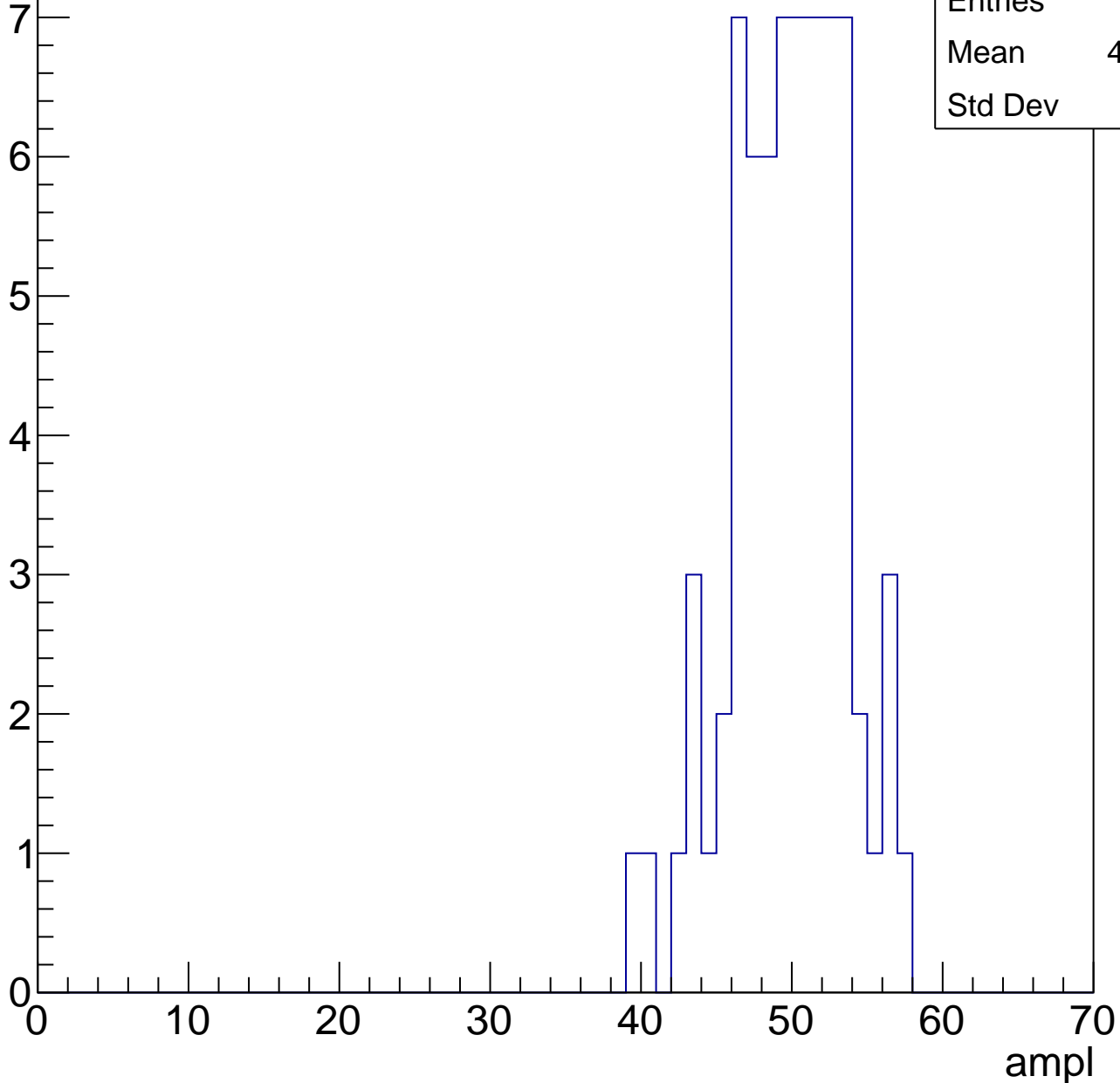


# B0L001S, U21-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	49.27
Std Dev	3.76

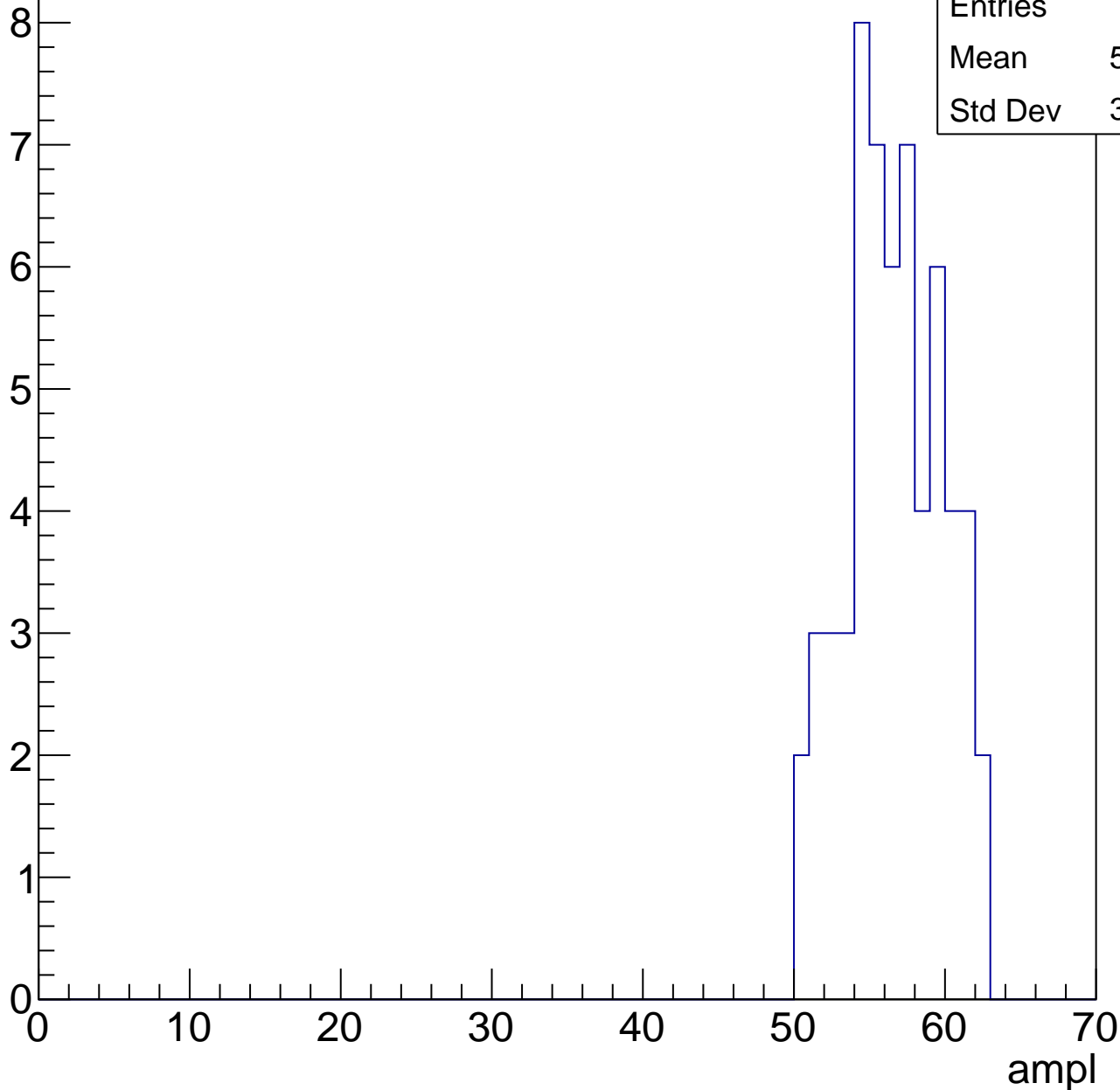


# B0L001S, U21-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	56.17
Std Dev	3.114

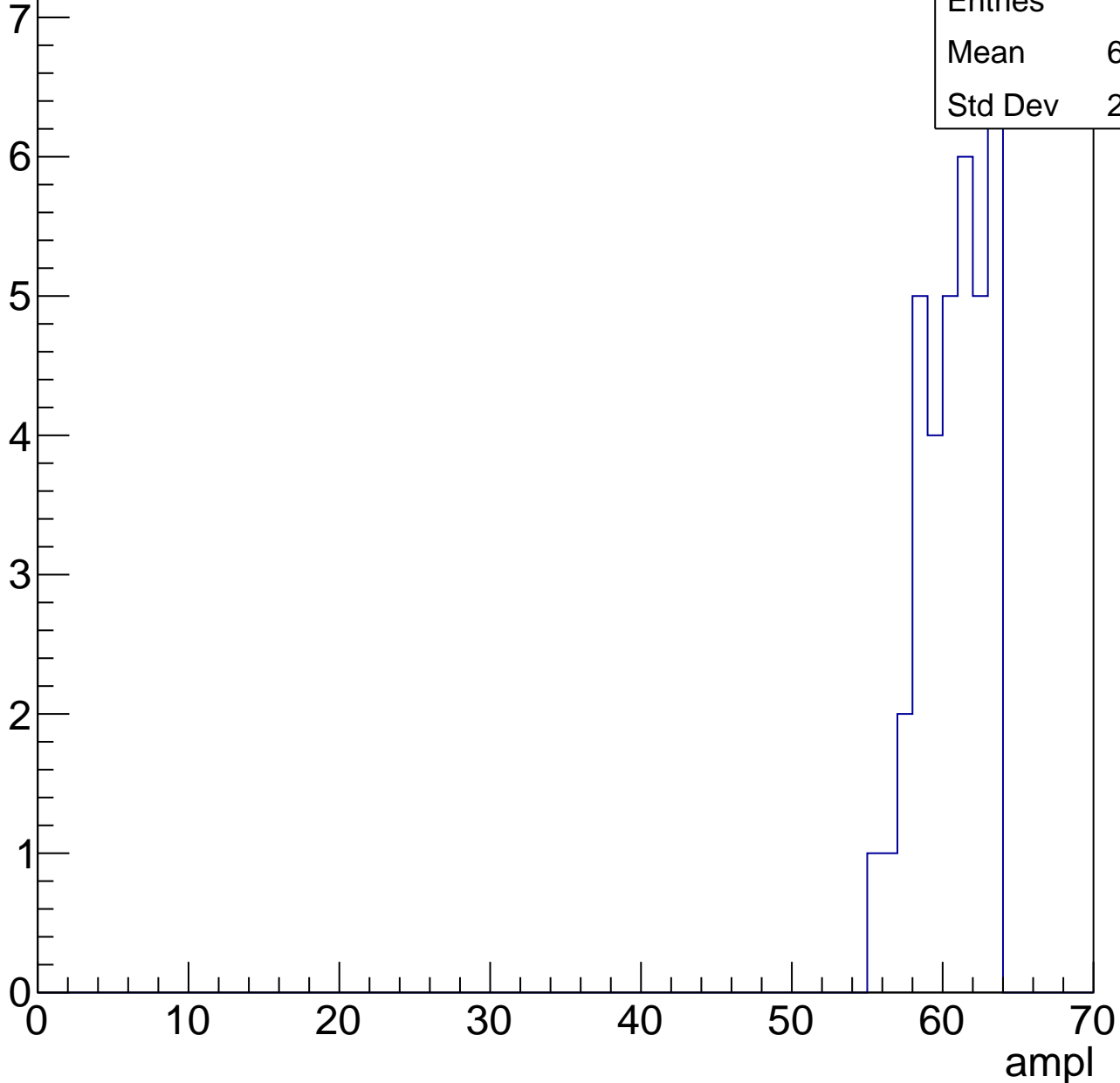


# B0L001S, U21-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

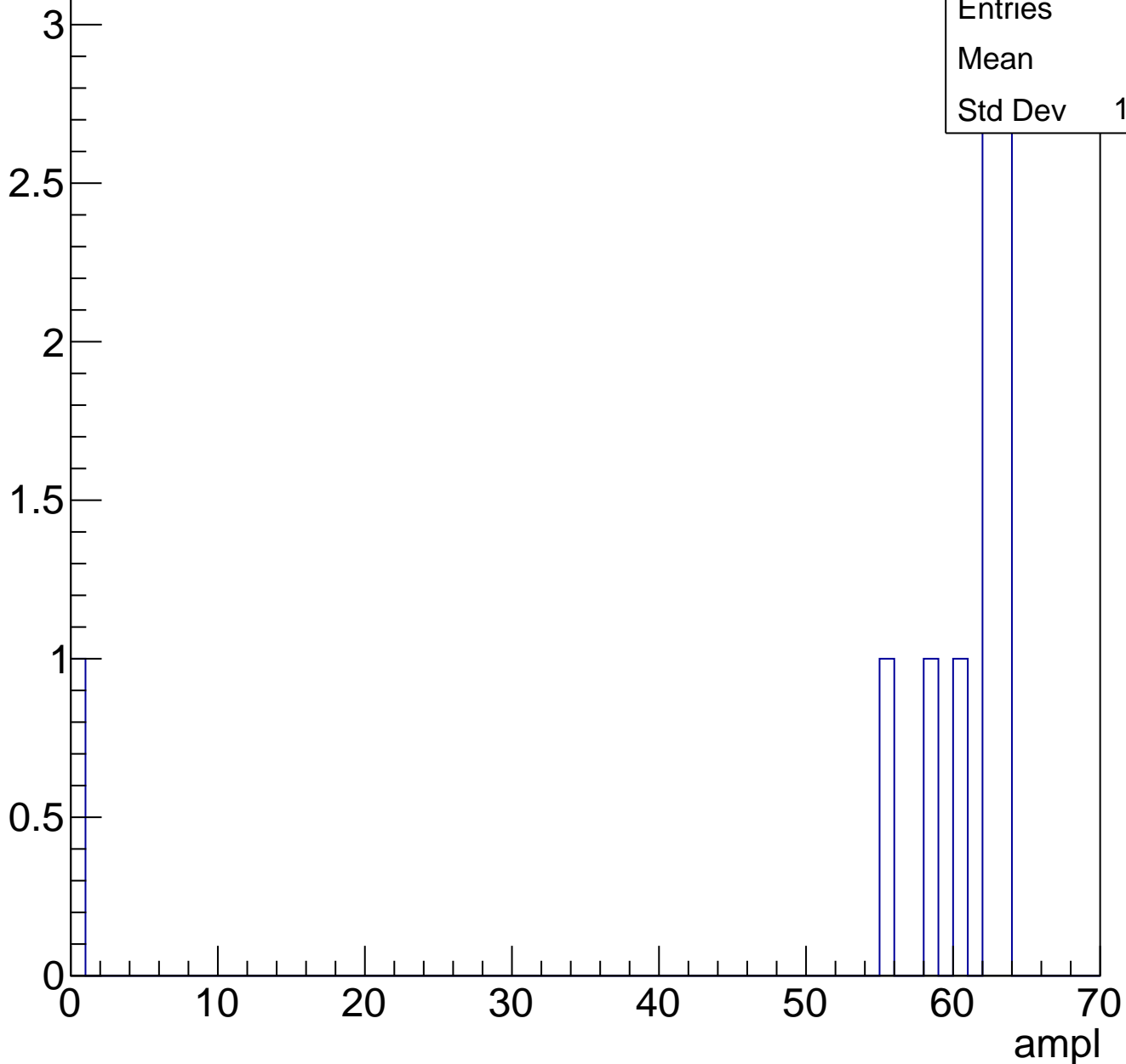
Entries	36
Mean	60.22
Std Dev	2.174



# B0L001S, U21-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch101, adc0

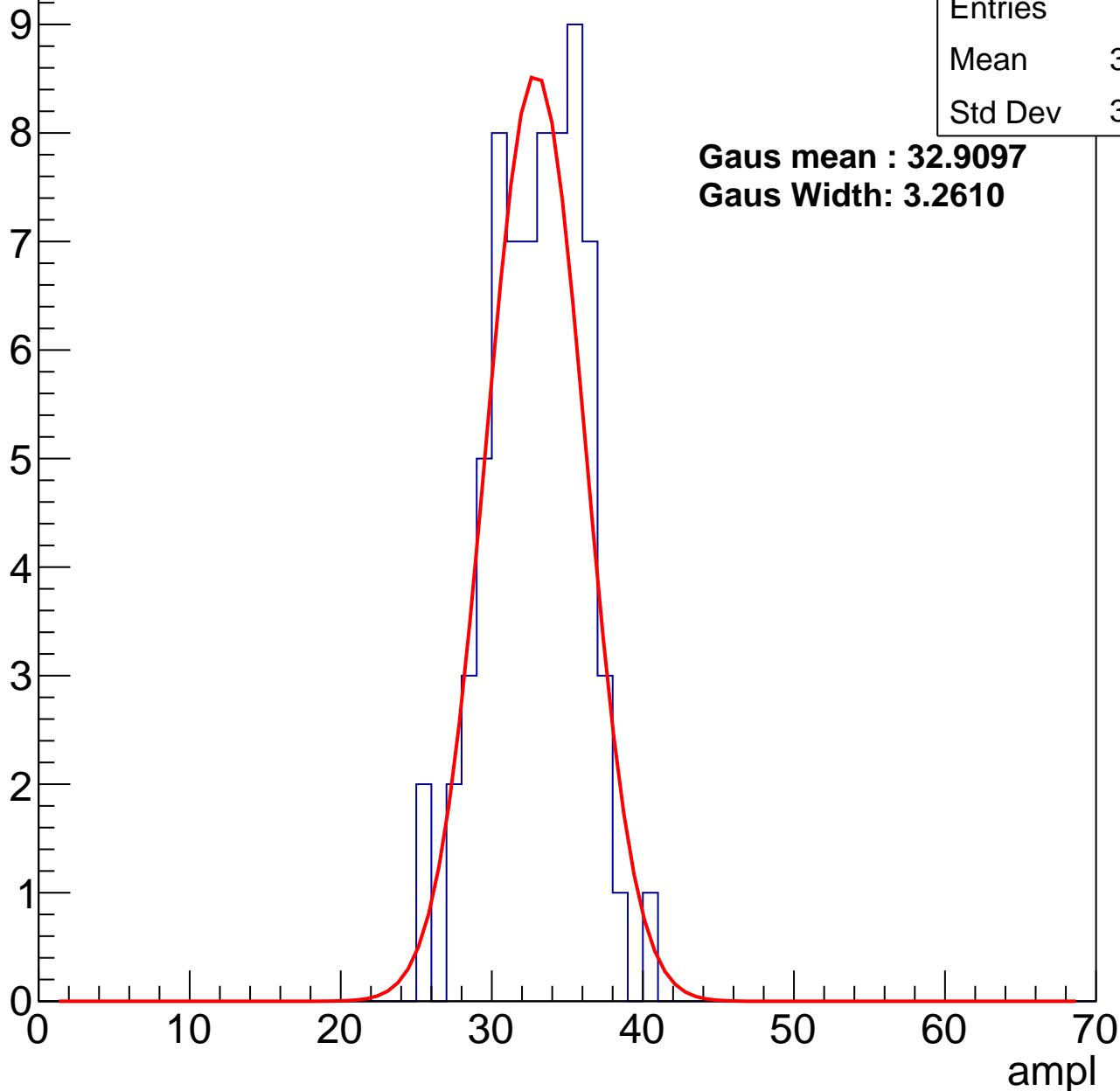
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	32.48
Std Dev	3.076

**Gaus mean : 32.9097**

**Gaus Width: 3.2610**



# B0L001S, U21-ch101, adc1

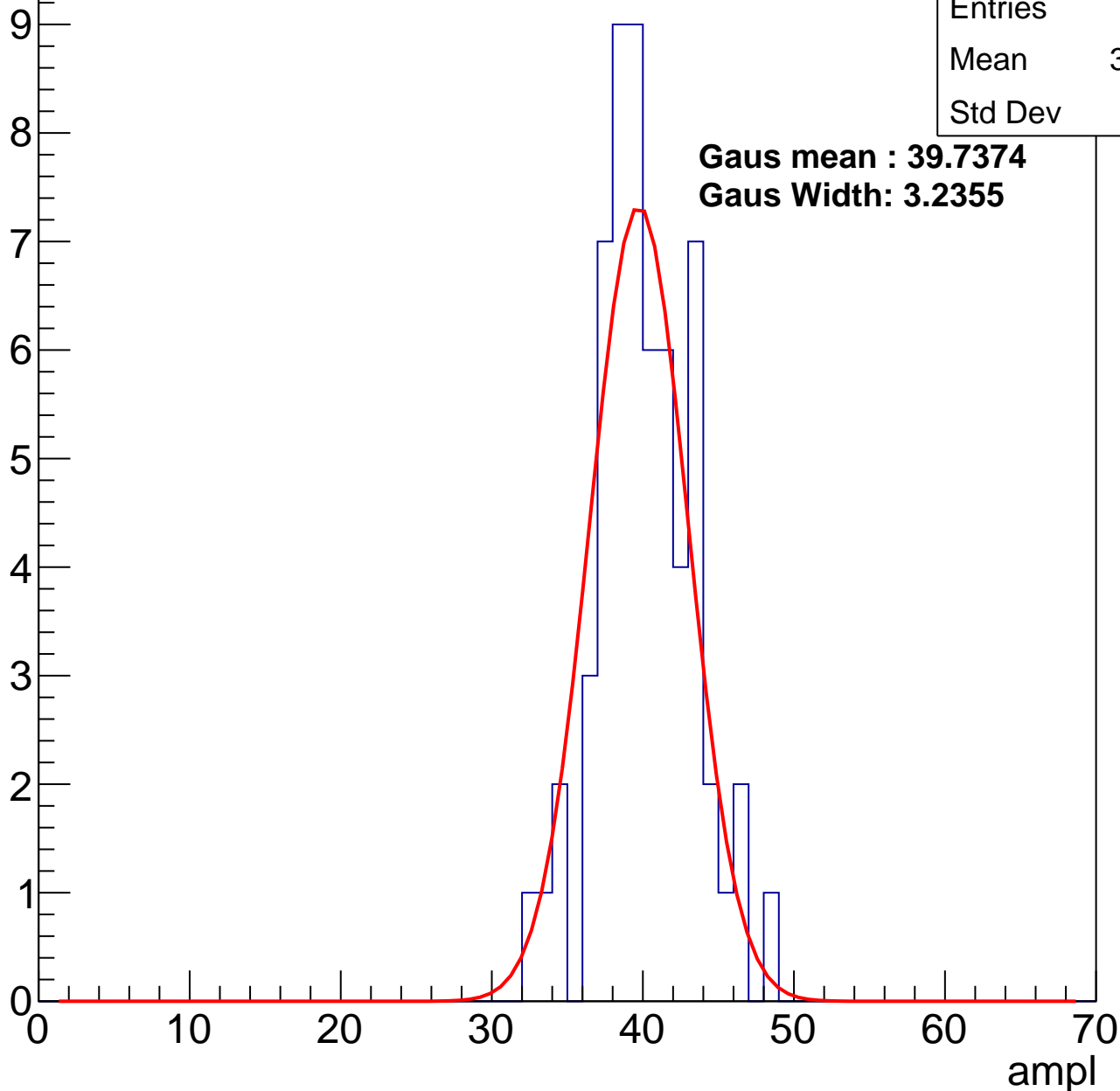
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	39.69
Std Dev	3.17

**Gaus mean : 39.7374**

**Gaus Width: 3.2355**



# B0L001S, U21-ch101, adc2

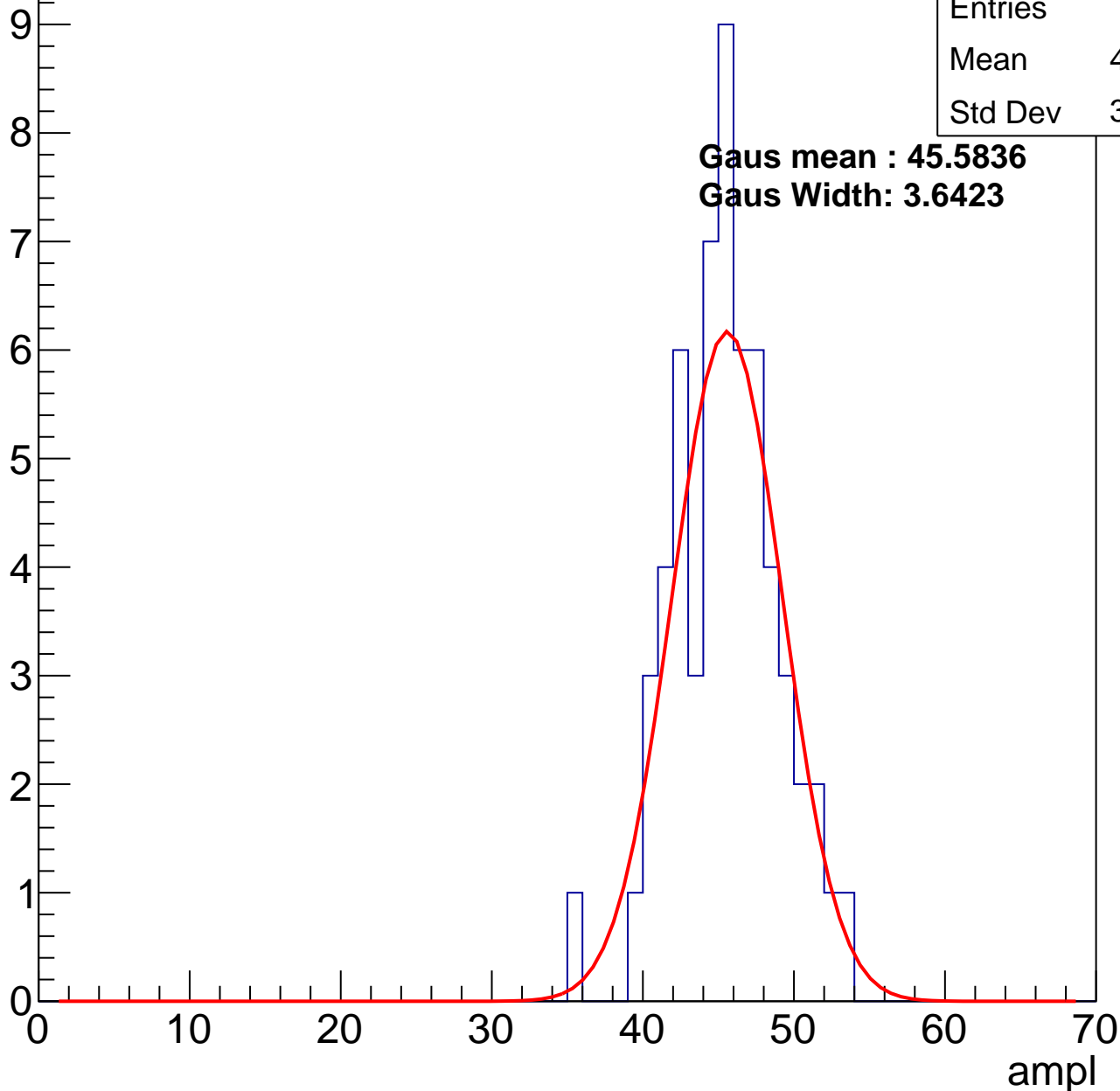
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	45.02
Std Dev	3.437

**Gaus mean : 45.5836**

**Gaus Width: 3.6423**

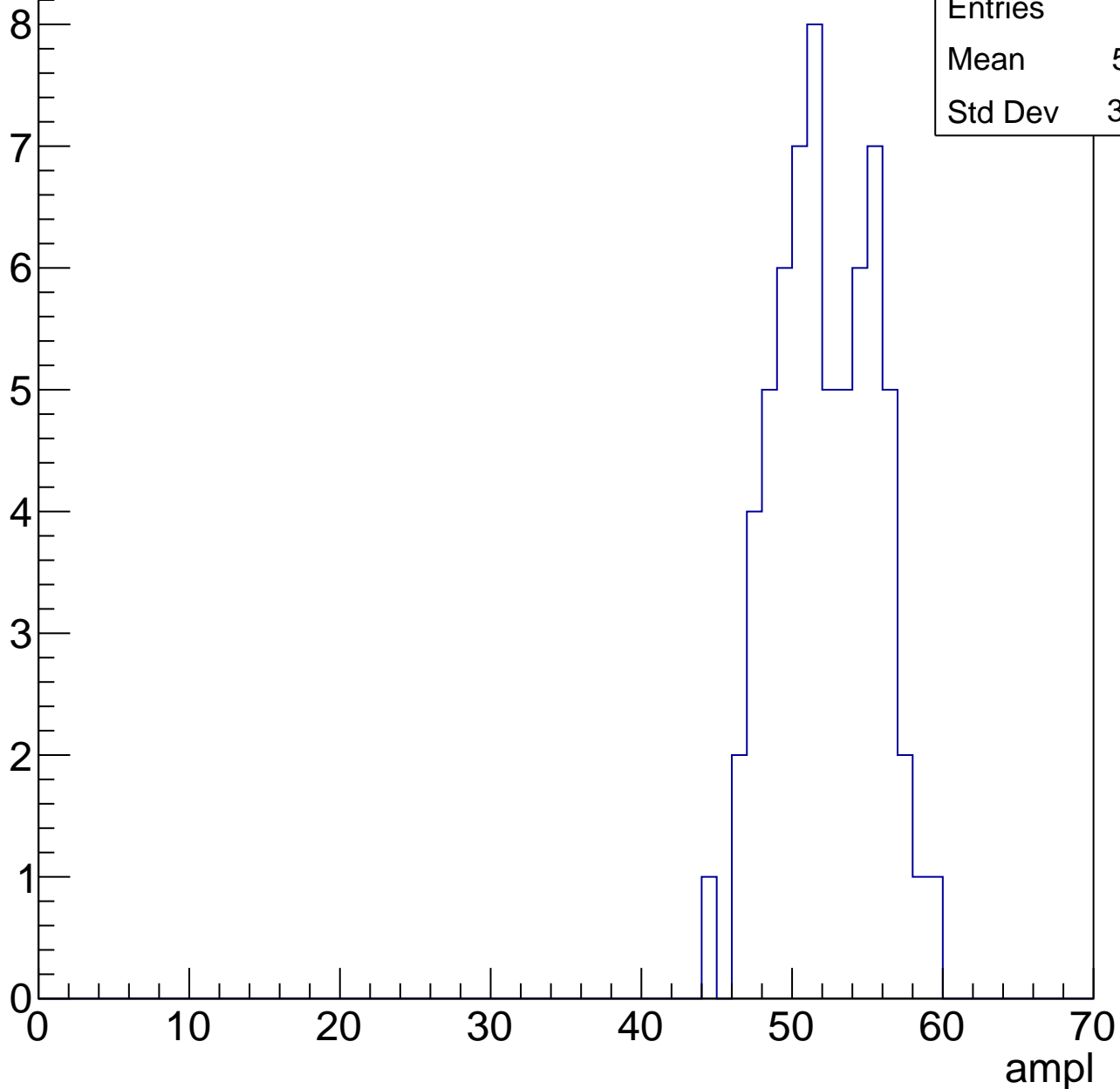


# B0L001S, U21-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	51.71
Std Dev	3.299

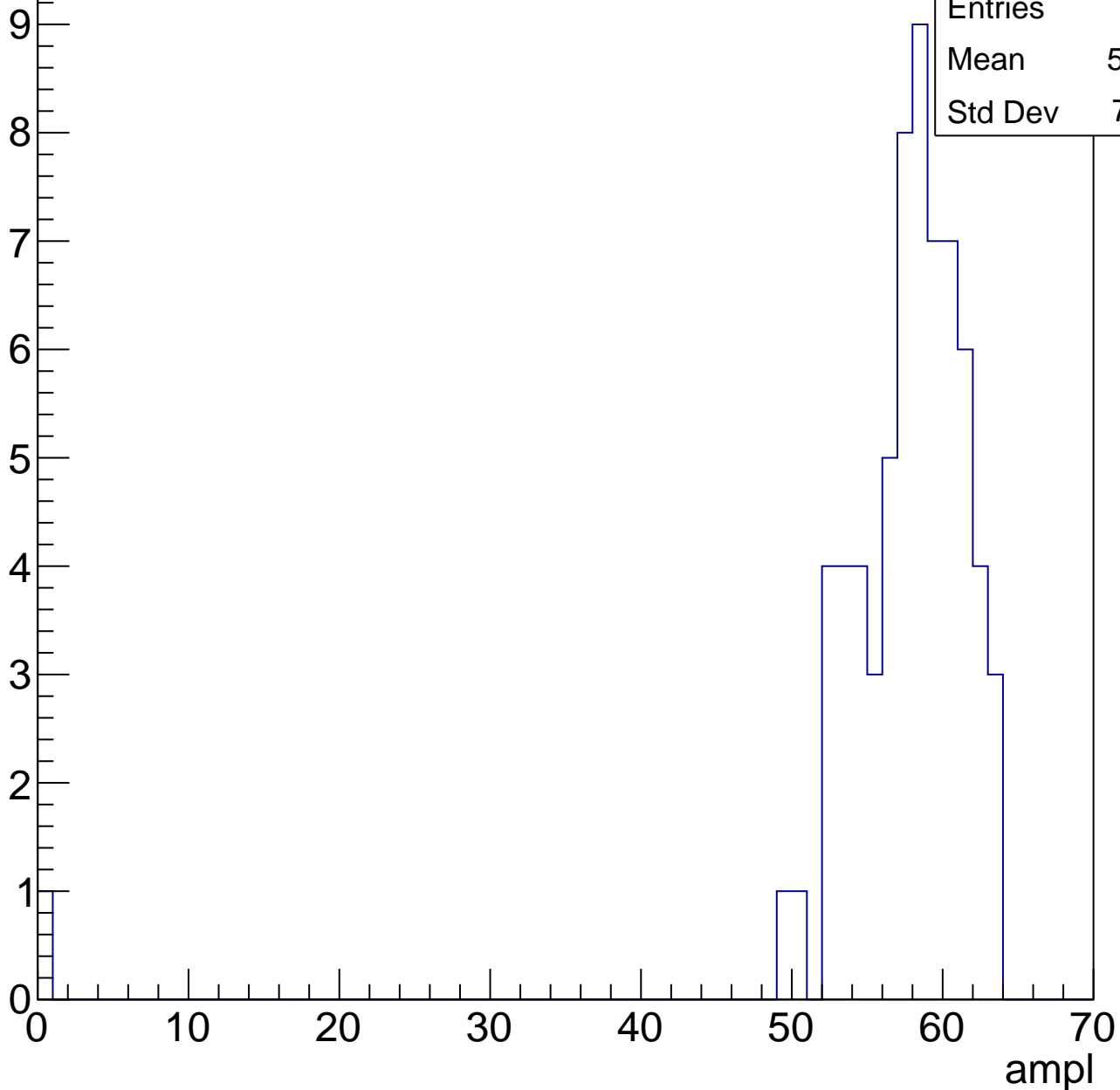


# B0L001S, U21-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	56.63
Std Dev	7.701

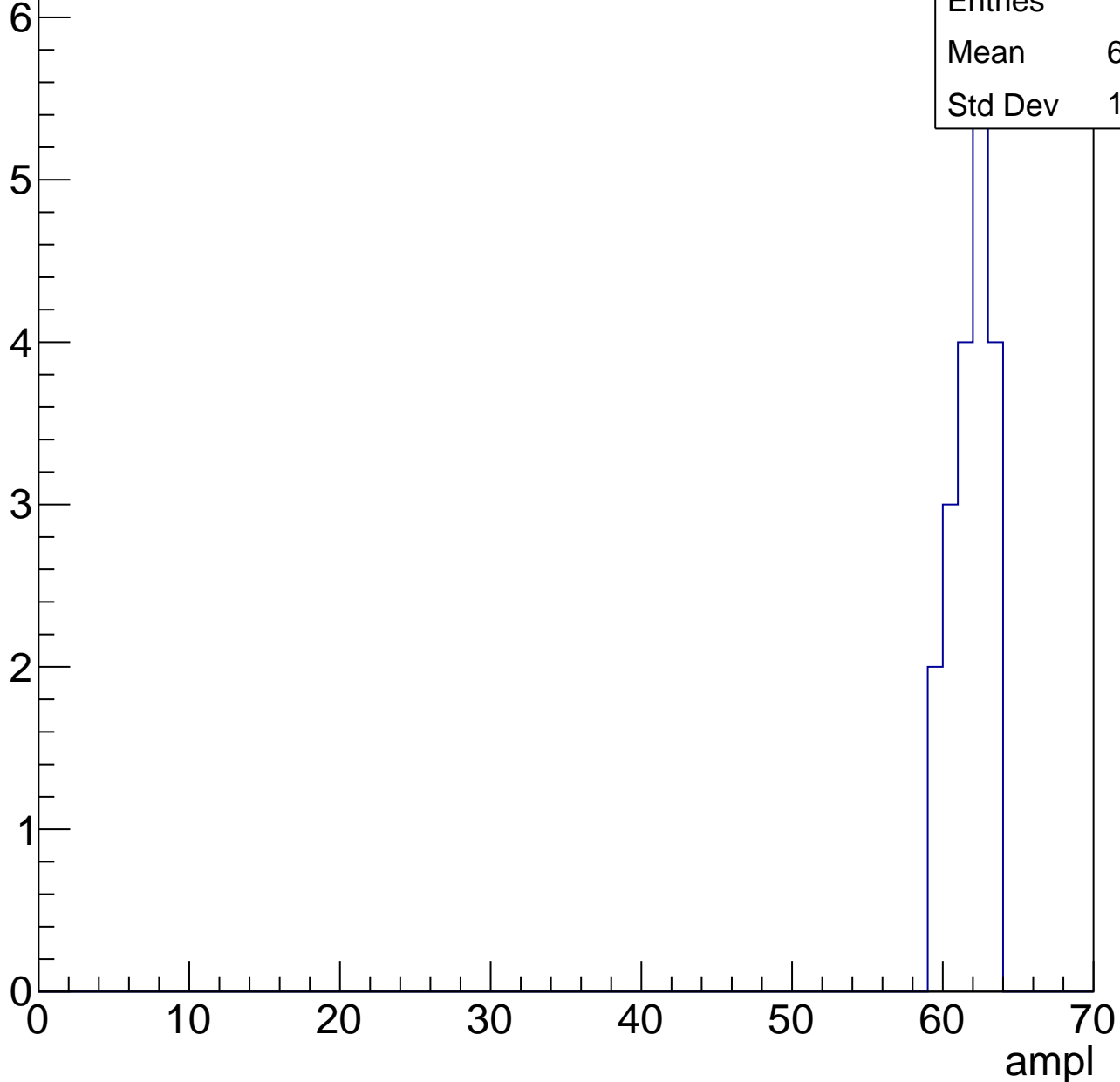


# B0L001S, U21-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	19
Mean	61.37
Std Dev	1.265



# B0L001S, U21-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	63
Std Dev	0



# B0L001S, U21-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U21-ch102, adc0

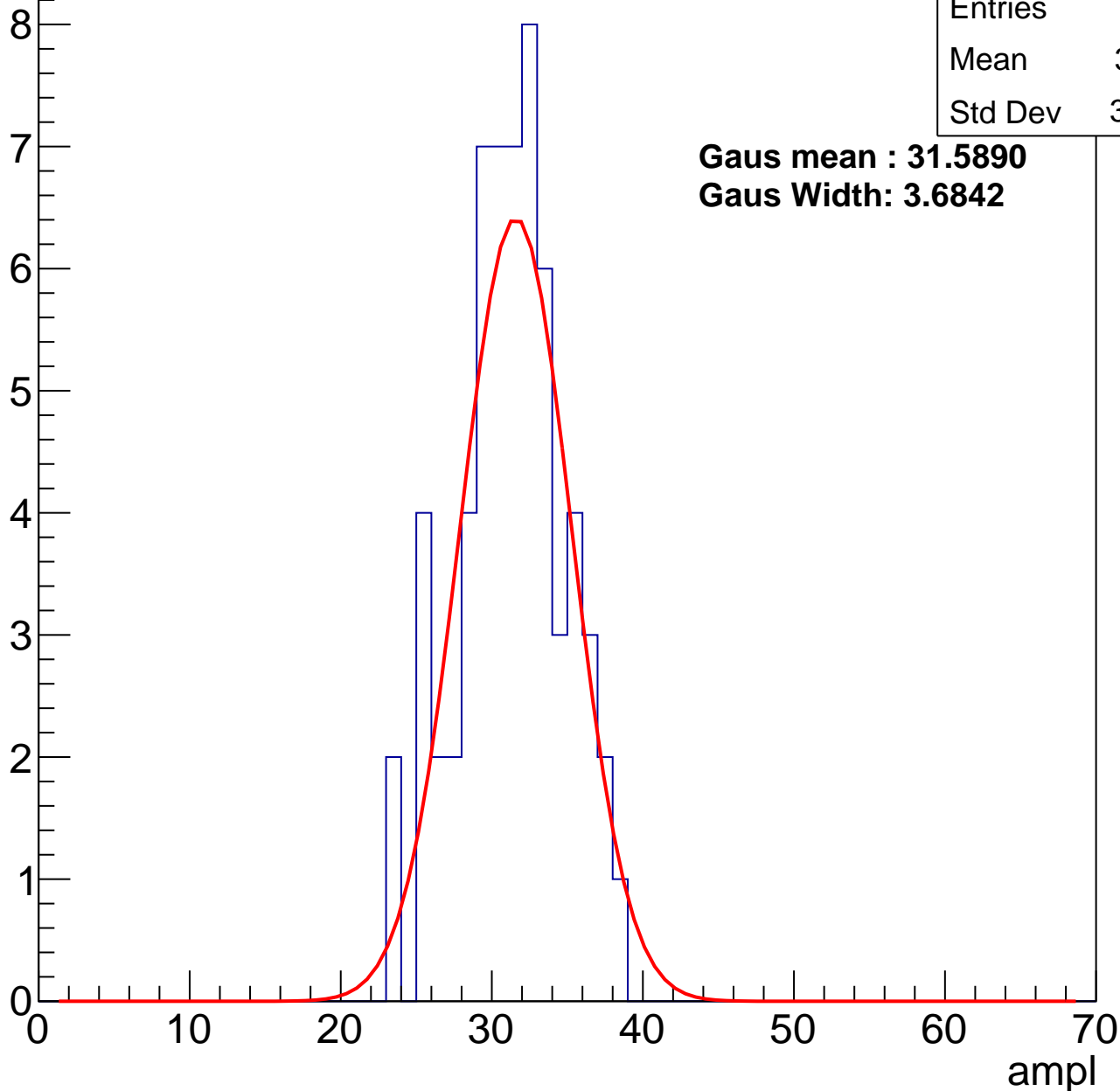
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	30.81
Std Dev	3.459

**Gaus mean : 31.5890**

**Gaus Width: 3.6842**



# B0L001S, U21-ch102, adc1

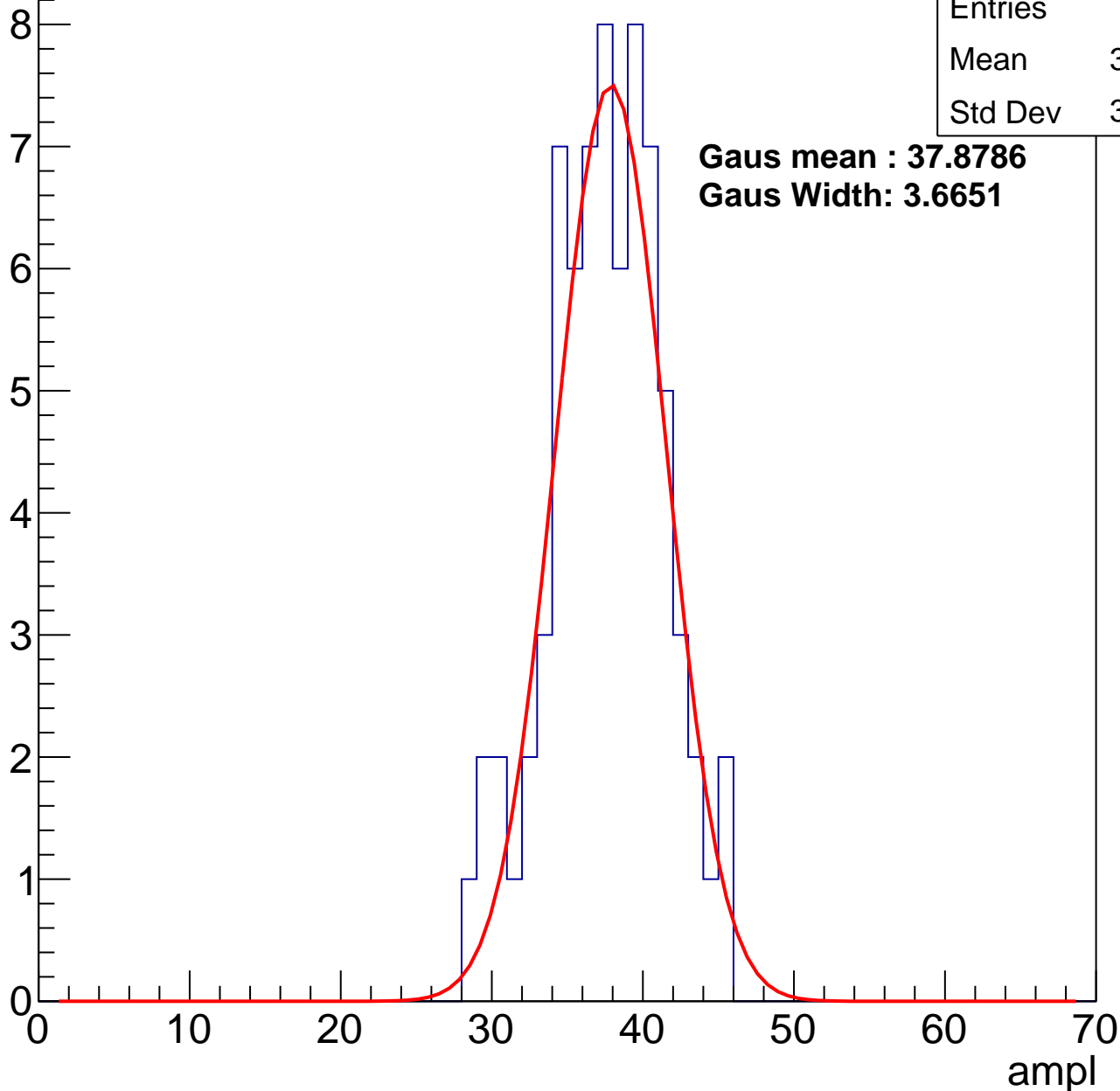
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	37.08
Std Dev	3.774

**Gaus mean : 37.8786**

**Gaus Width: 3.6651**



# B0L001S, U21-ch102, adc2

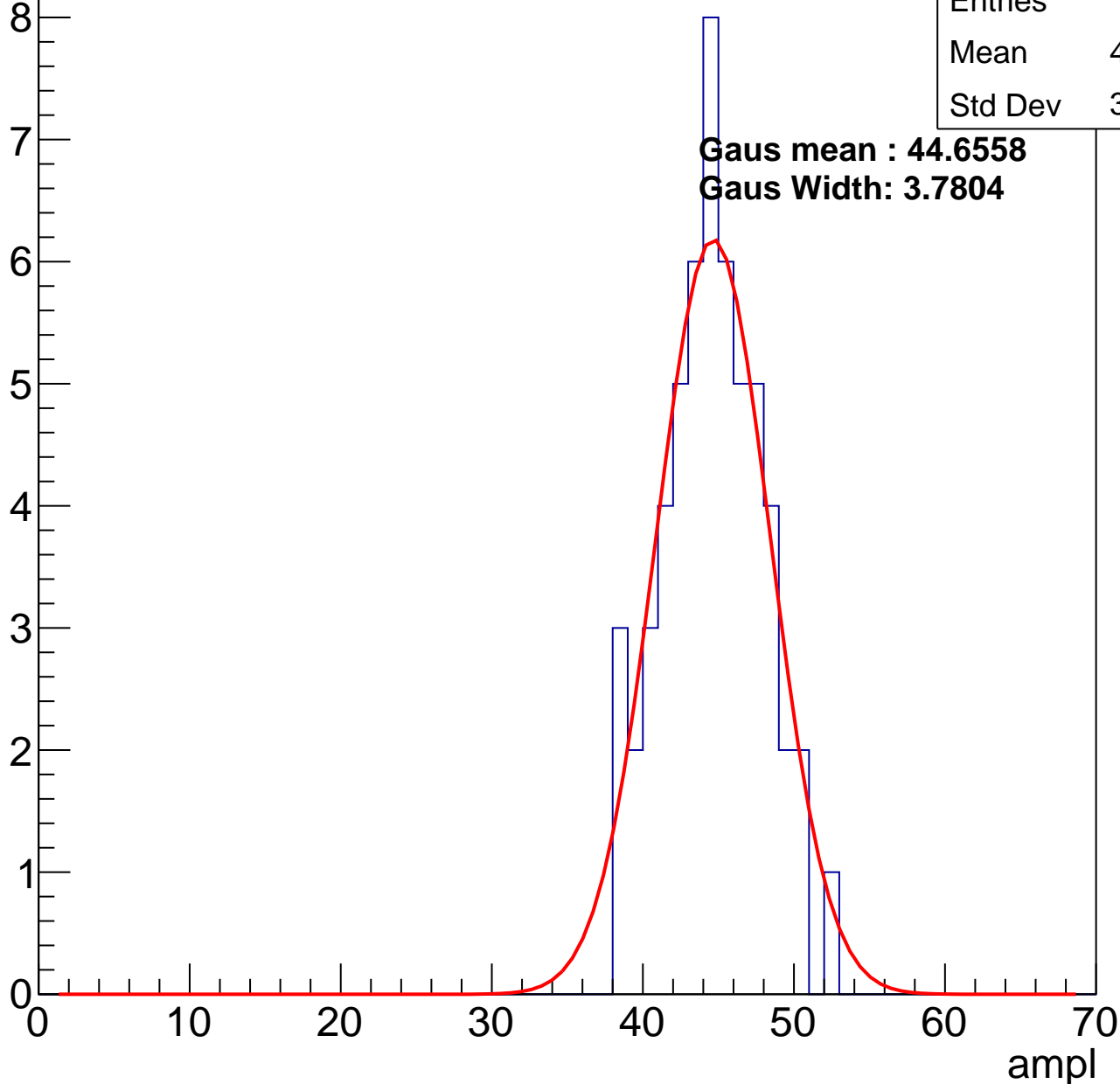
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	44.16
Std Dev	3.239

**Gaus mean : 44.6558**

**Gaus Width: 3.7804**

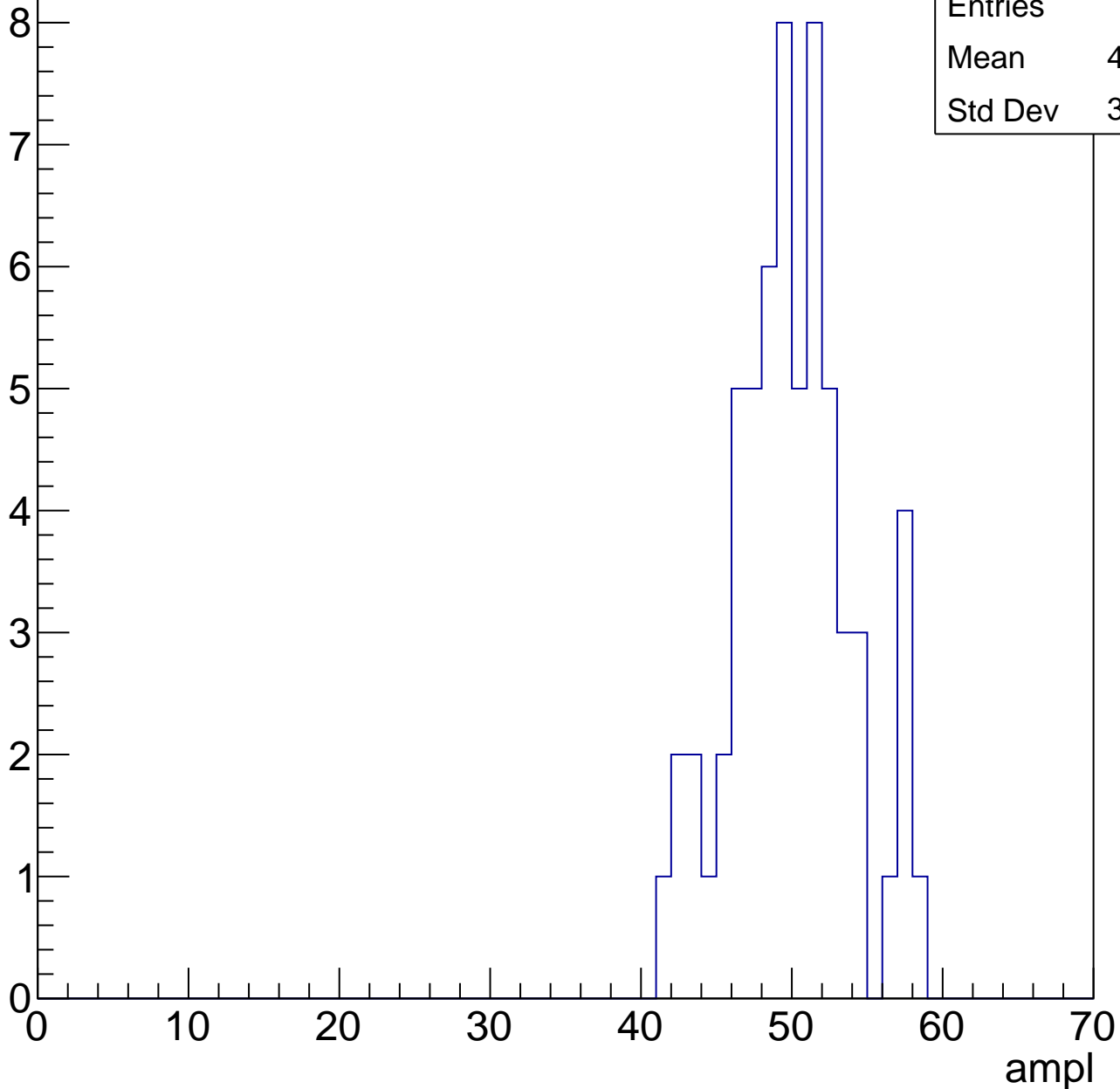


# B0L001S, U21-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

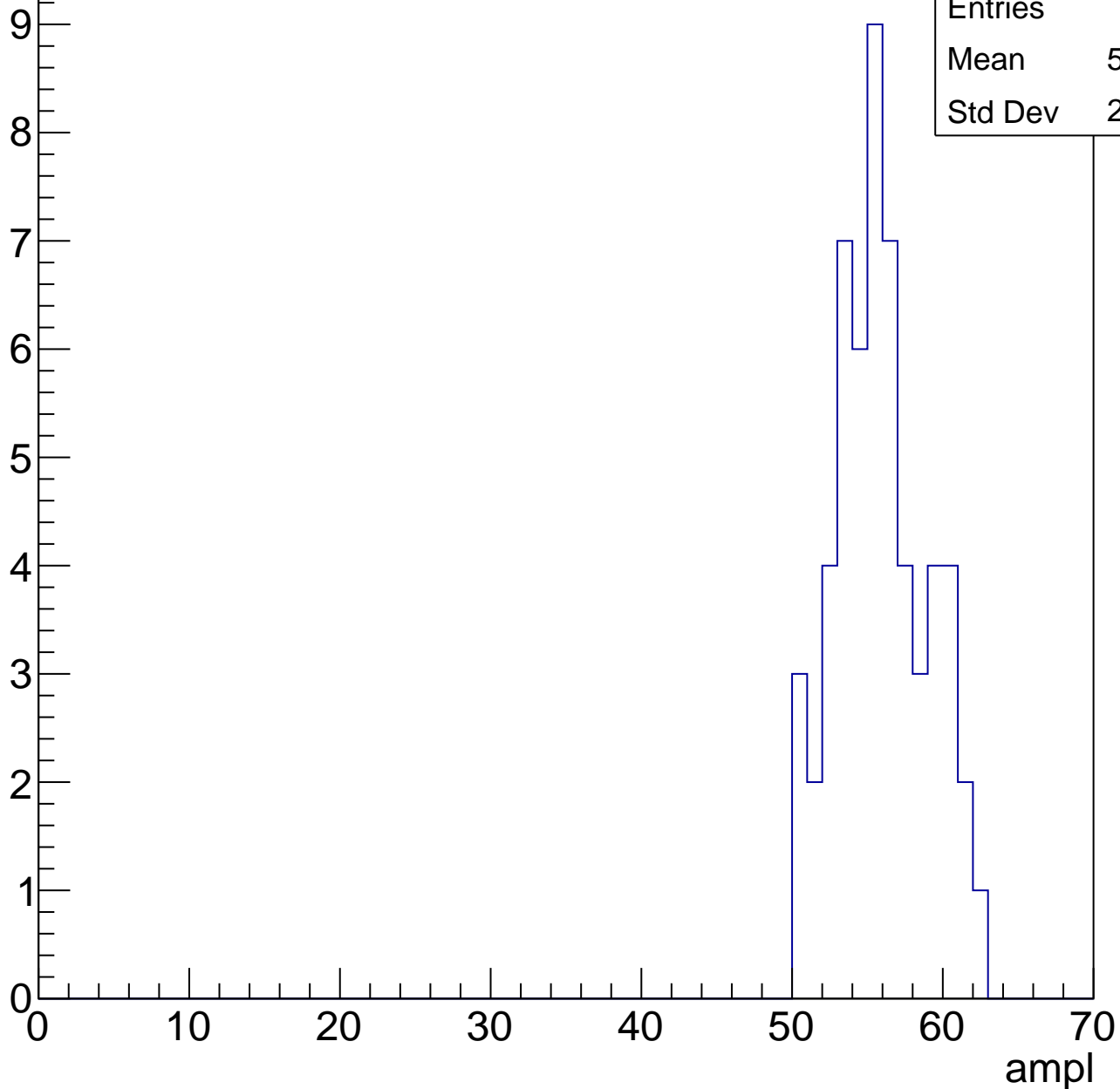
Entries	62
Mean	49.53
Std Dev	3.884



# B0L001S, U21-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



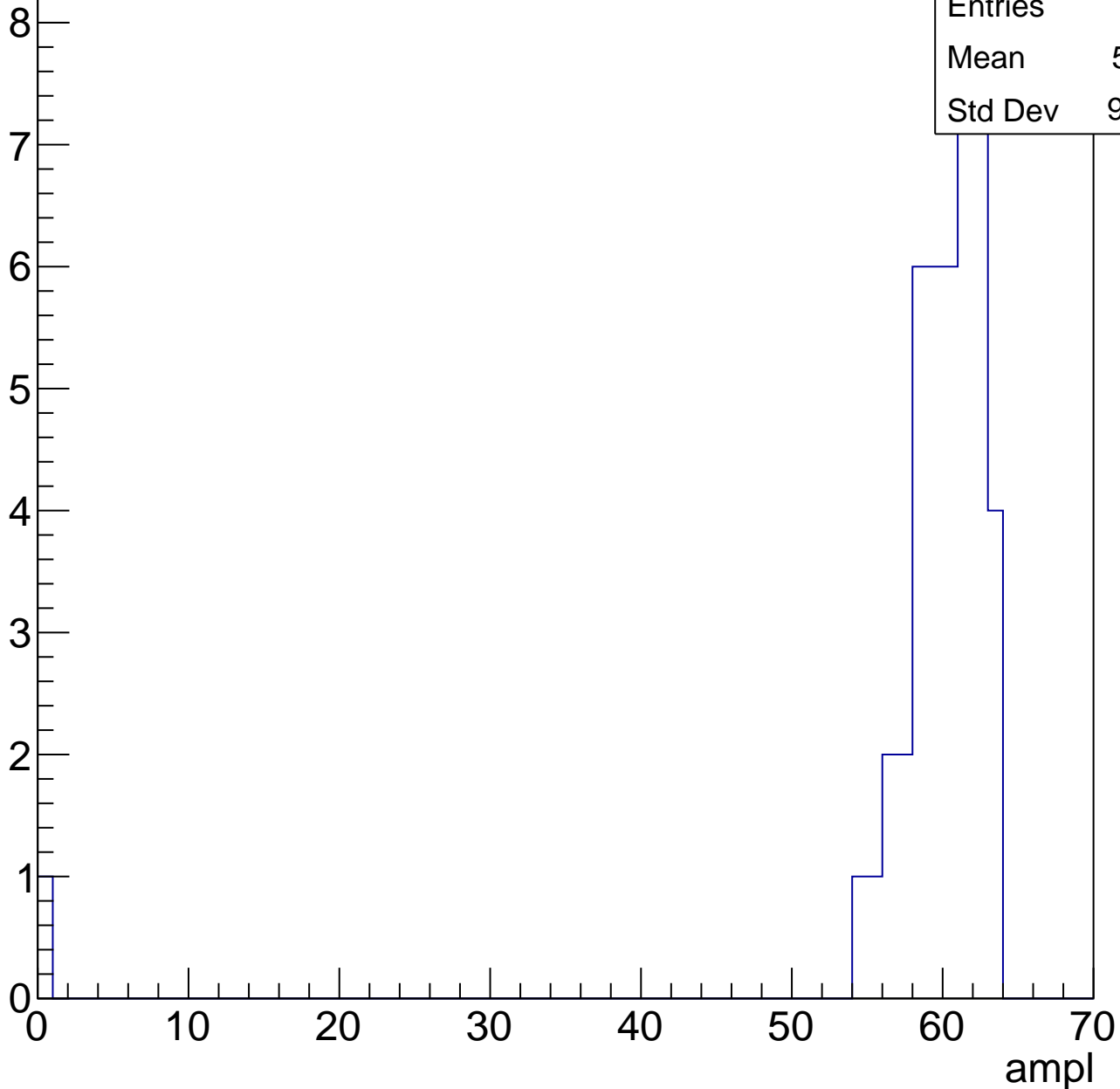
Entries	56
Mean	55.43
Std Dev	2.993

# B0L001S, U21-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	45
Mean	58.51
Std Dev	9.089

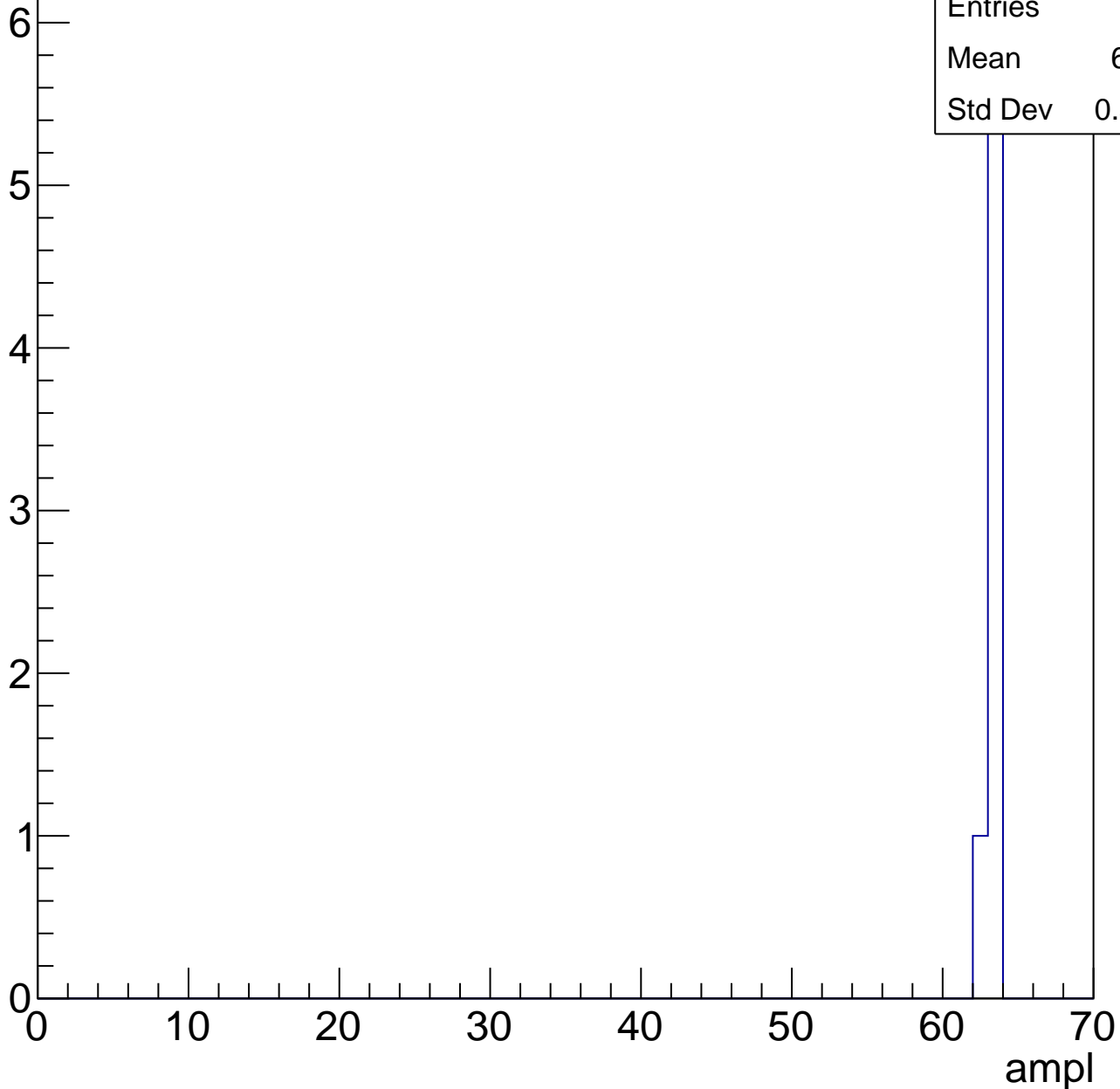


# B0L001S, U21-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	7
Mean	62.86
Std Dev	0.3499

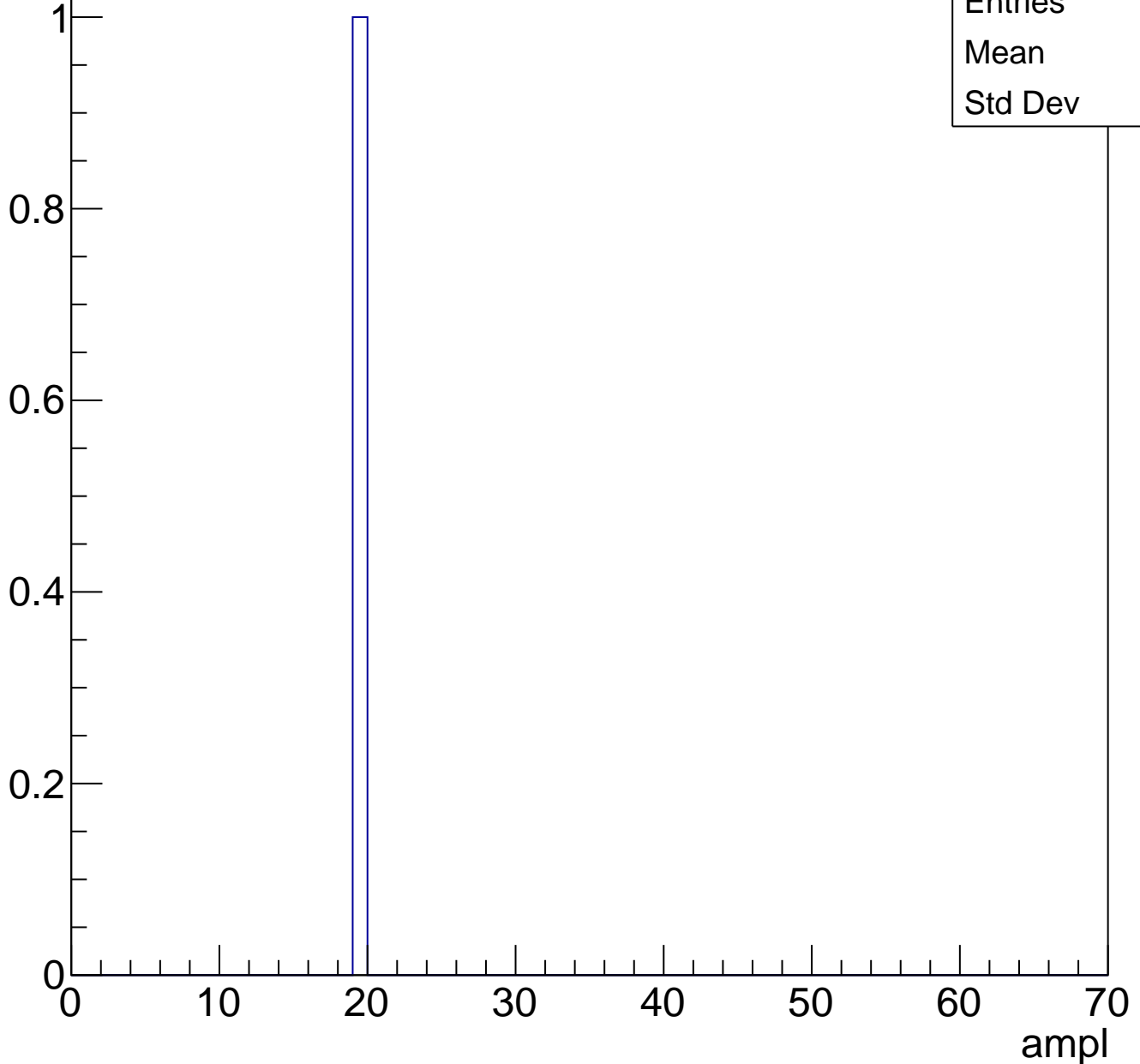




# B0L001S, U21-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch103, adc0

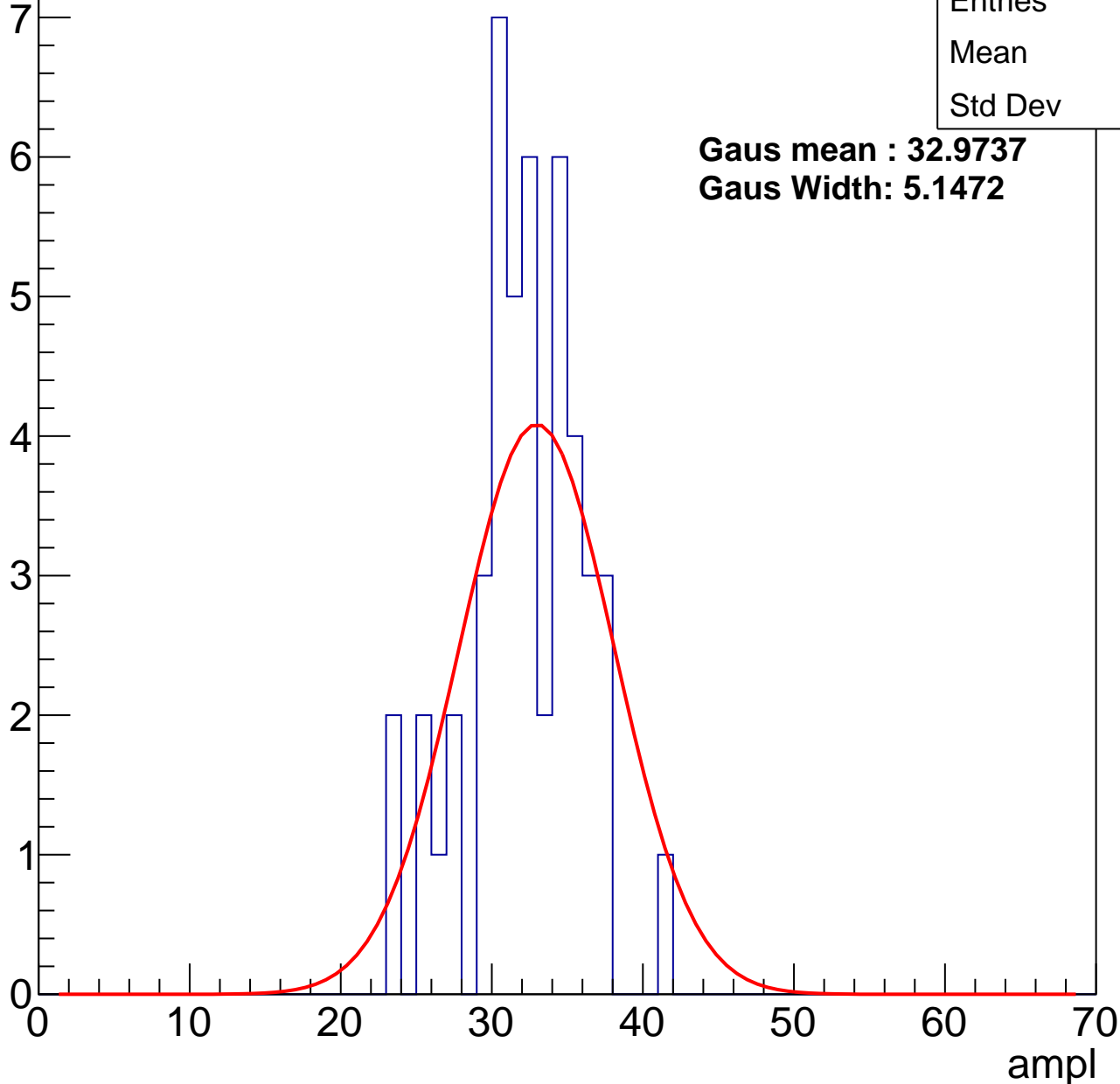
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	31.7
Std Dev	3.77

**Gaus mean : 32.9737**

**Gaus Width: 5.1472**



# B0L001S, U21-ch103, adc1

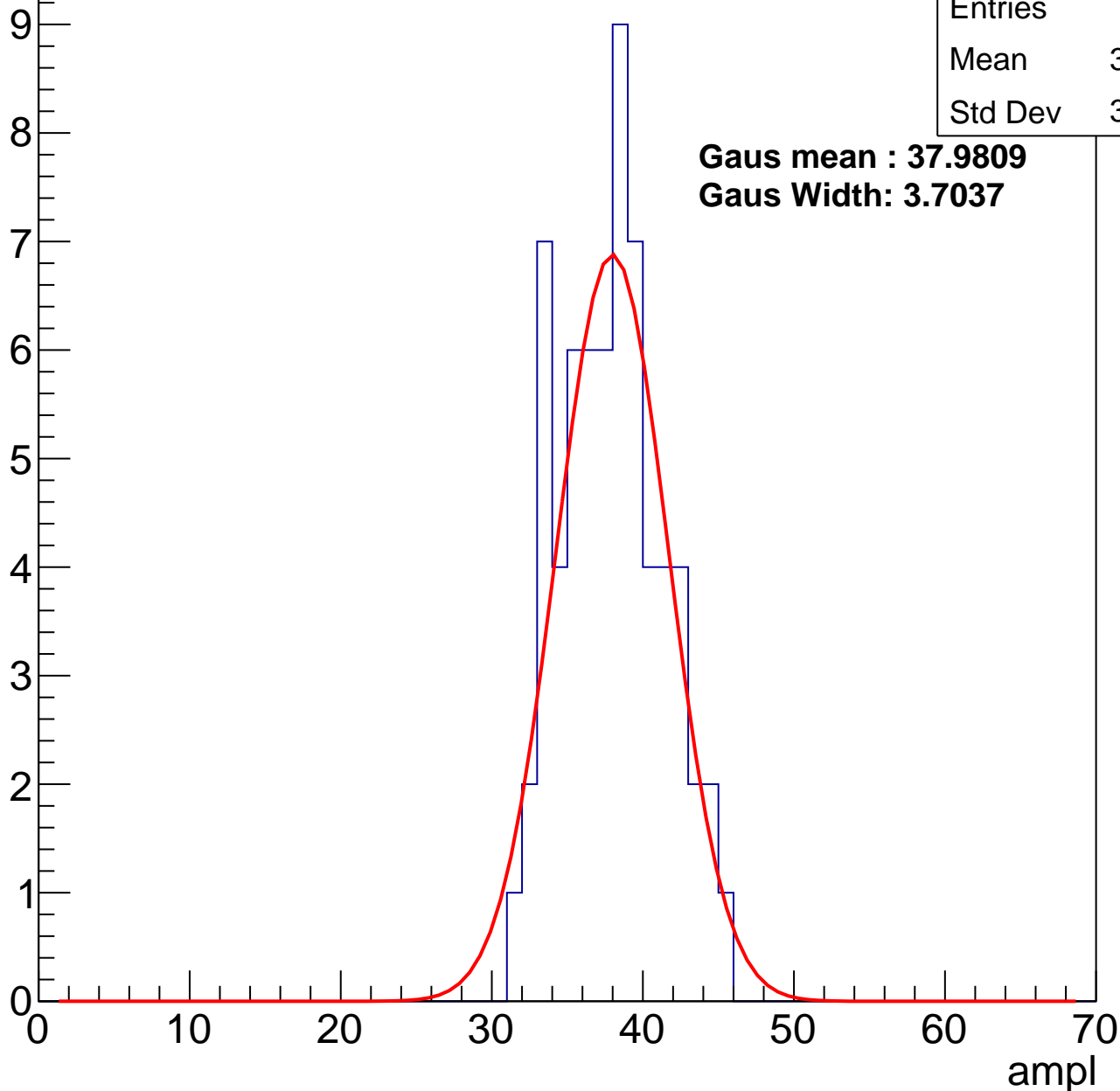
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	37.48
Std Dev	3.329

**Gaus mean : 37.9809**

**Gaus Width: 3.7037**



# B0L001S, U21-ch103, adc2

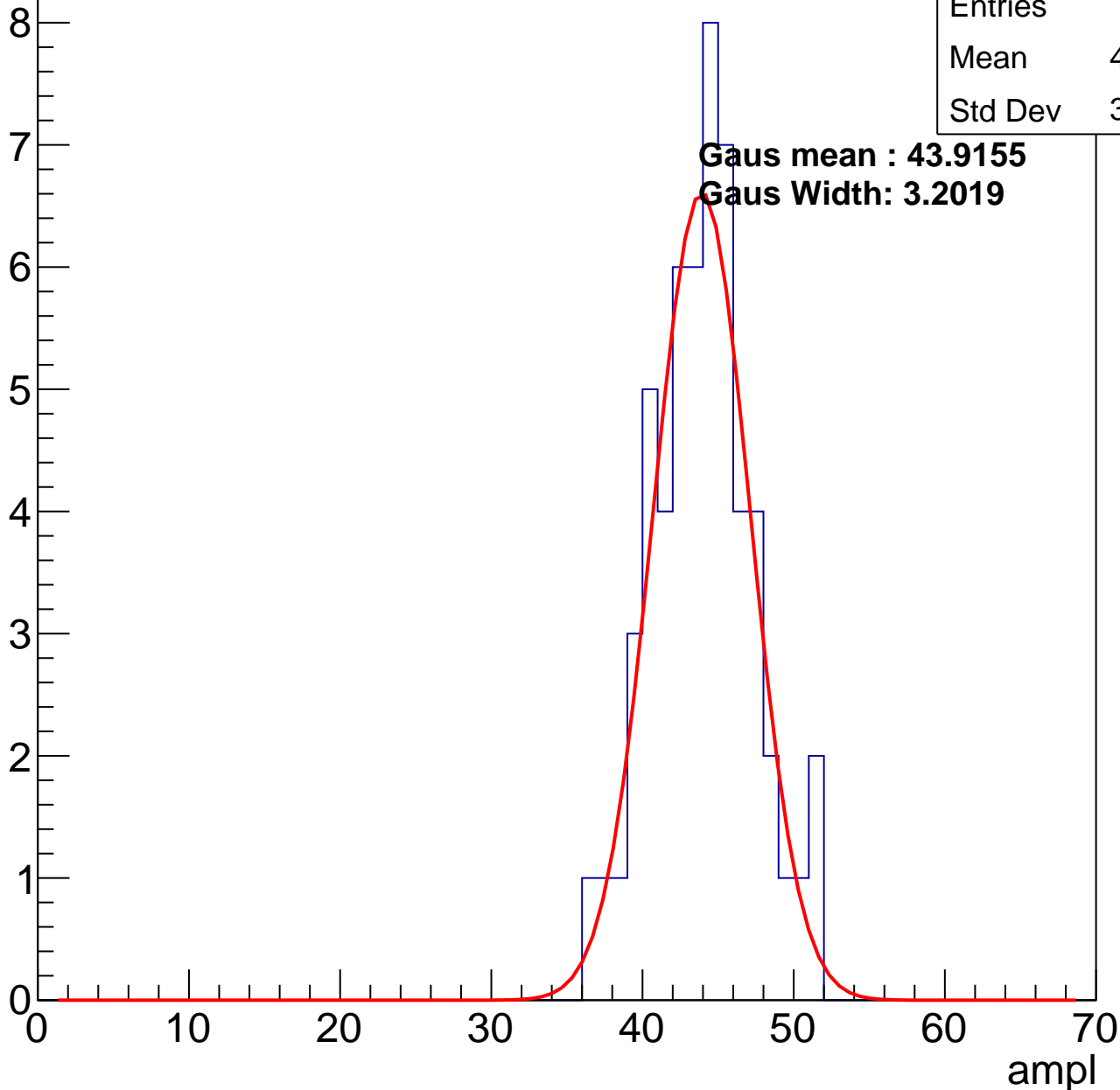
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	43.54
Std Dev	3.295

**Gaus mean : 43.9155**

**Gaus Width: 3.2019**



# B0L001S, U21-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

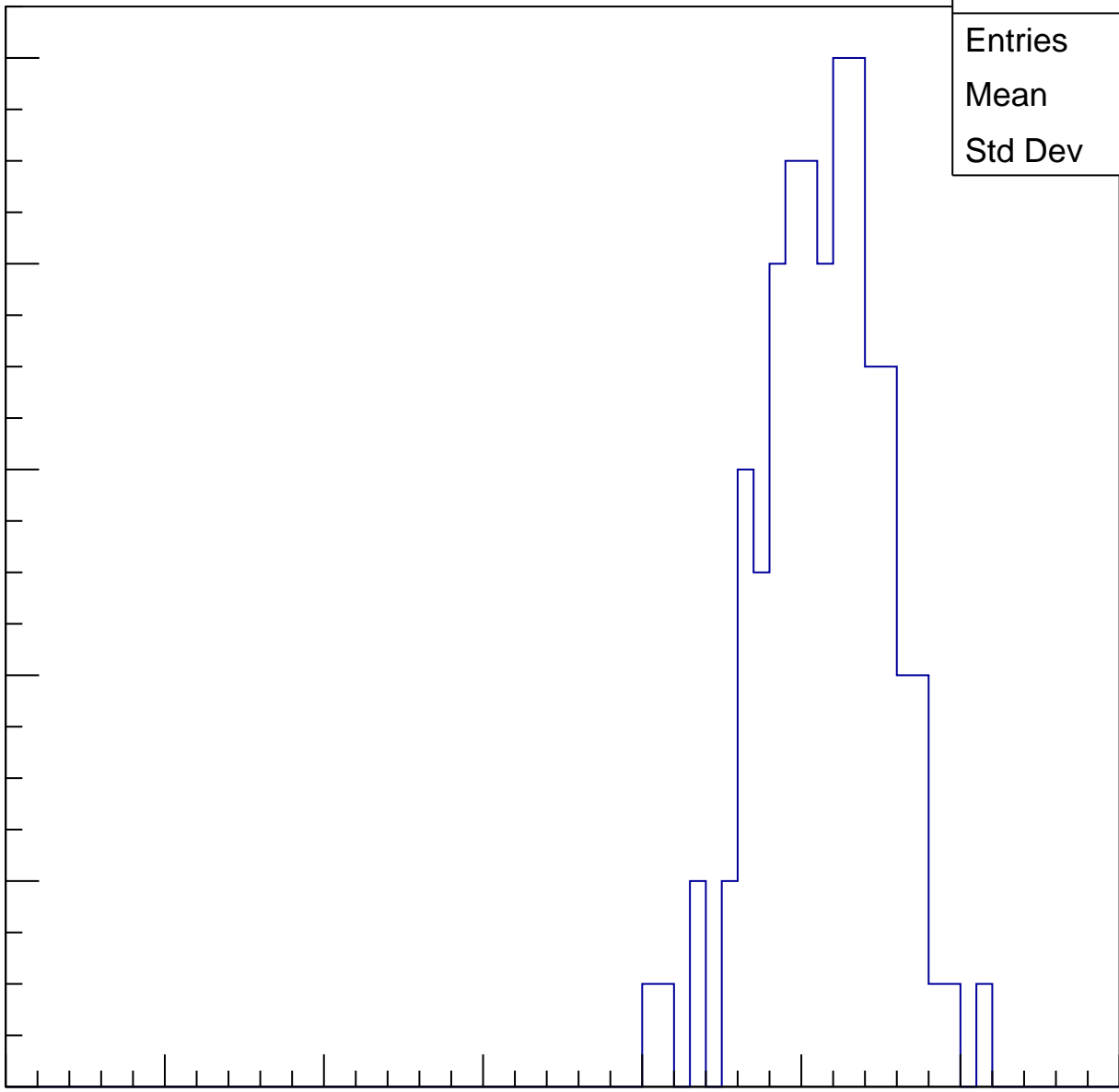
Entries	96
Mean	50.98
Std Dev	3.886

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

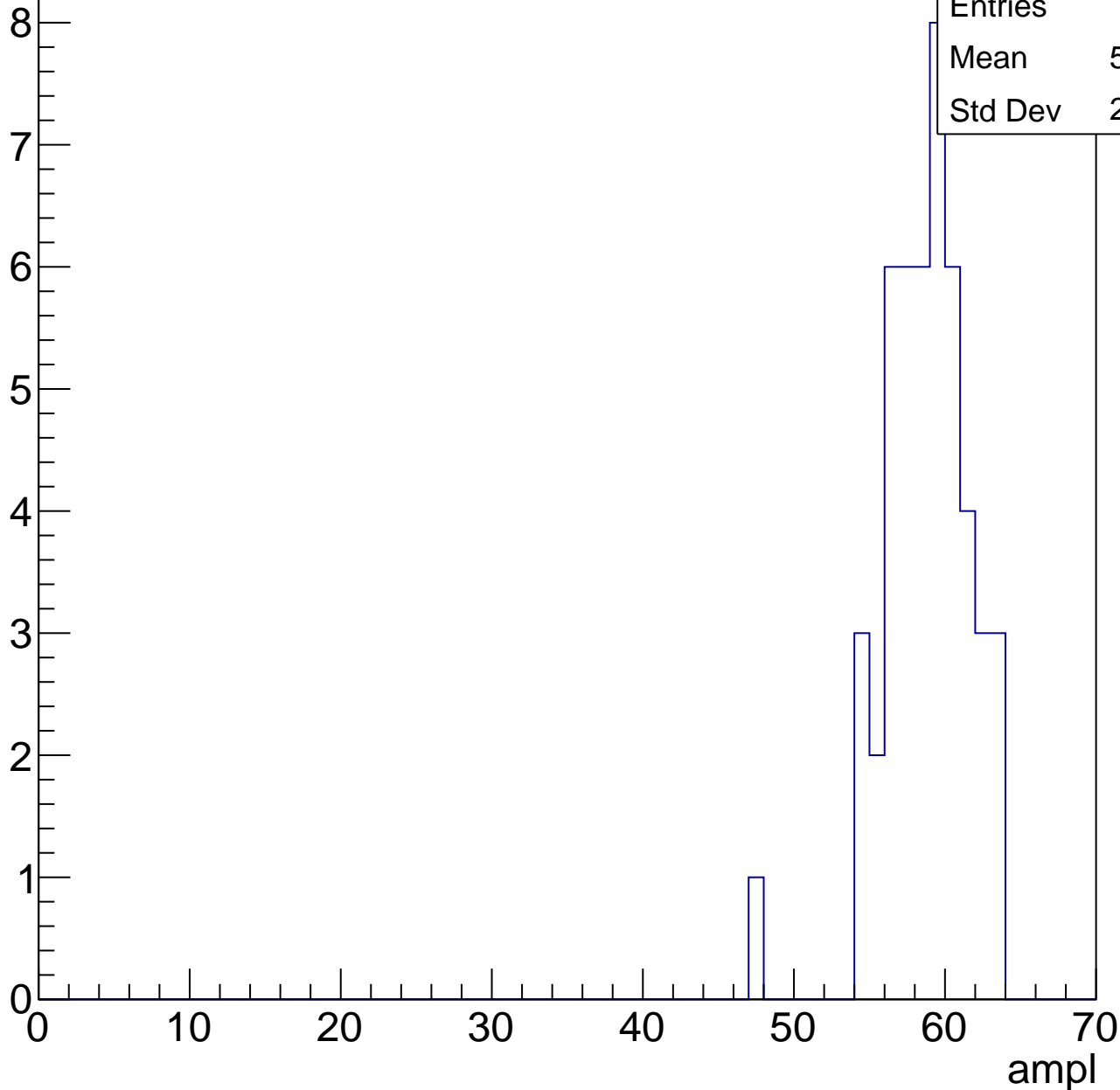


# B0L001S, U21-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	58.25
Std Dev	2.905

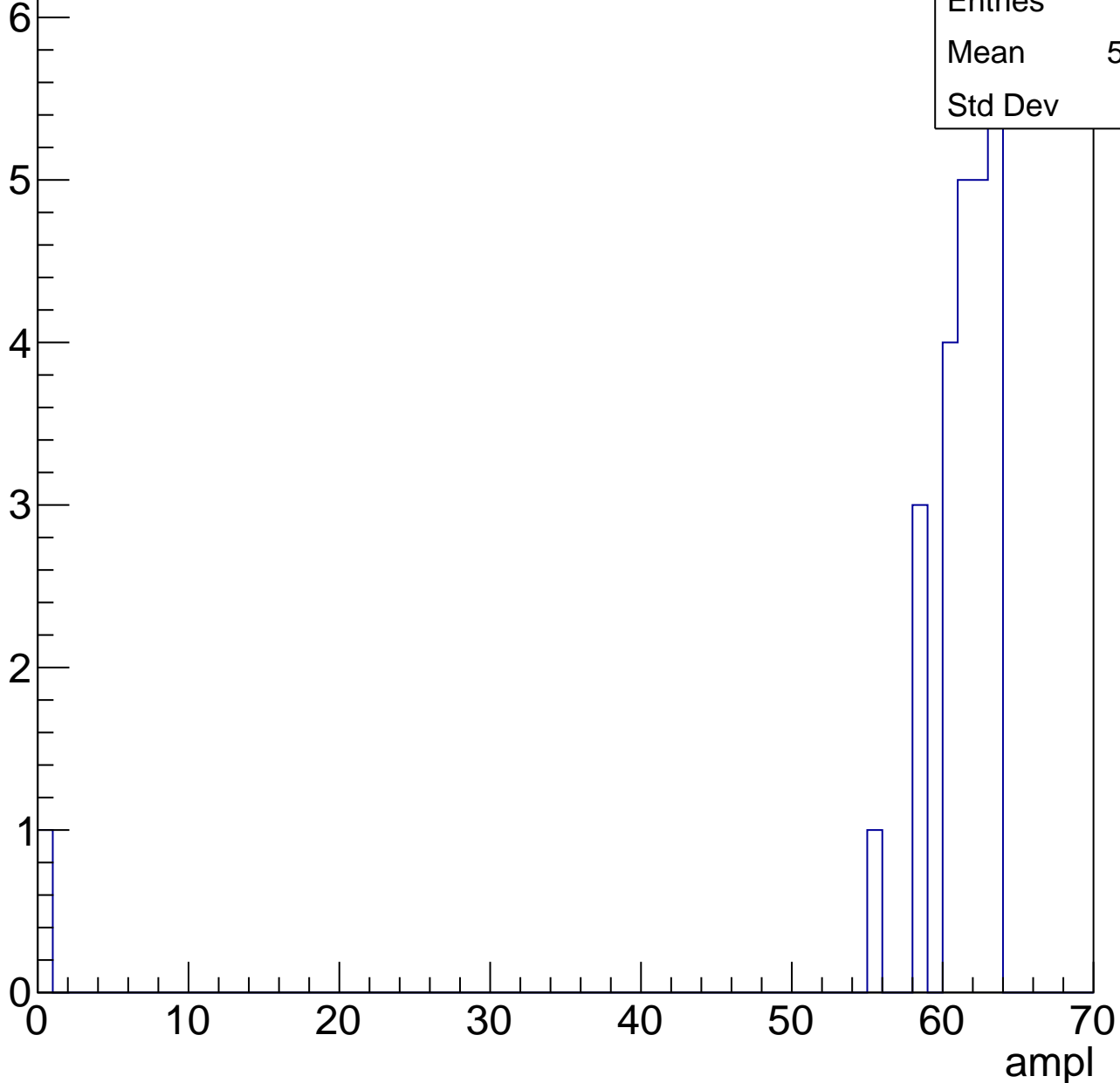


# B0L001S, U21-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	25
Mean	58.48
Std Dev	12.1



# B0L001S, U21-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

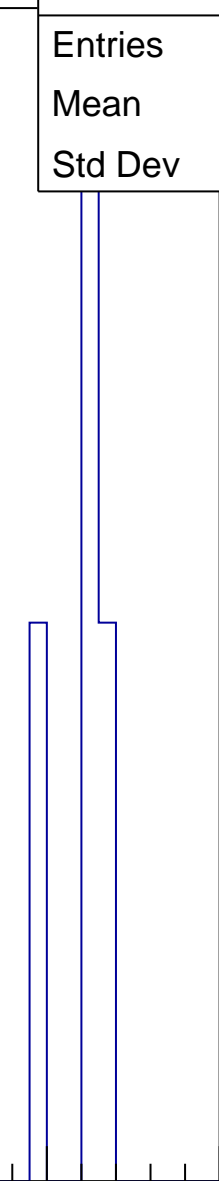
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	61.5
Std Dev	1.5

0 10 20 30 40 50 60 70

ampl





# B0L001S, U21-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U21-ch104, adc0

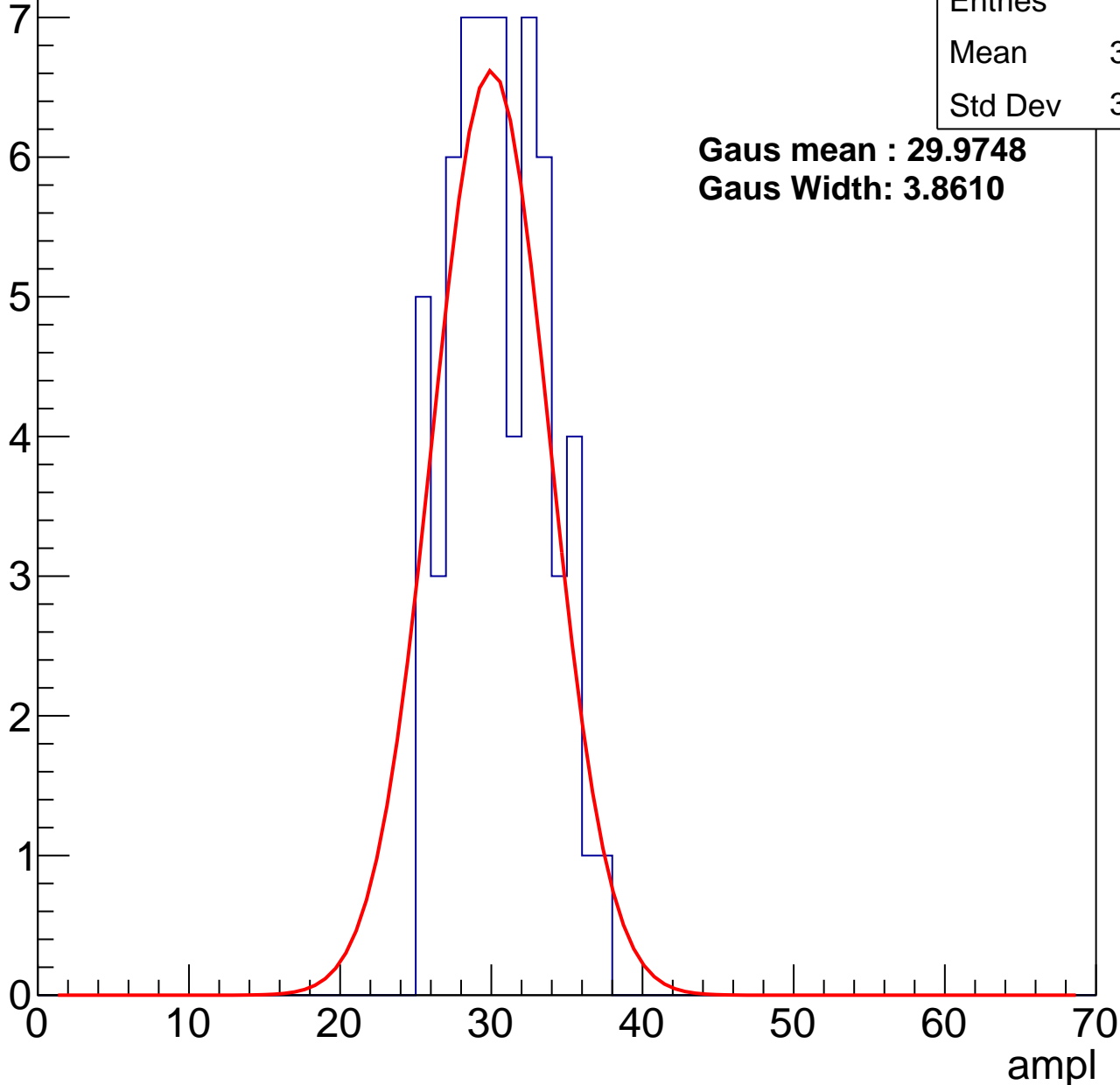
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	30.08
Std Dev	3.085

**Gaus mean : 29.9748**

**Gaus Width: 3.8610**



# B0L001S, U21-ch104, adc1

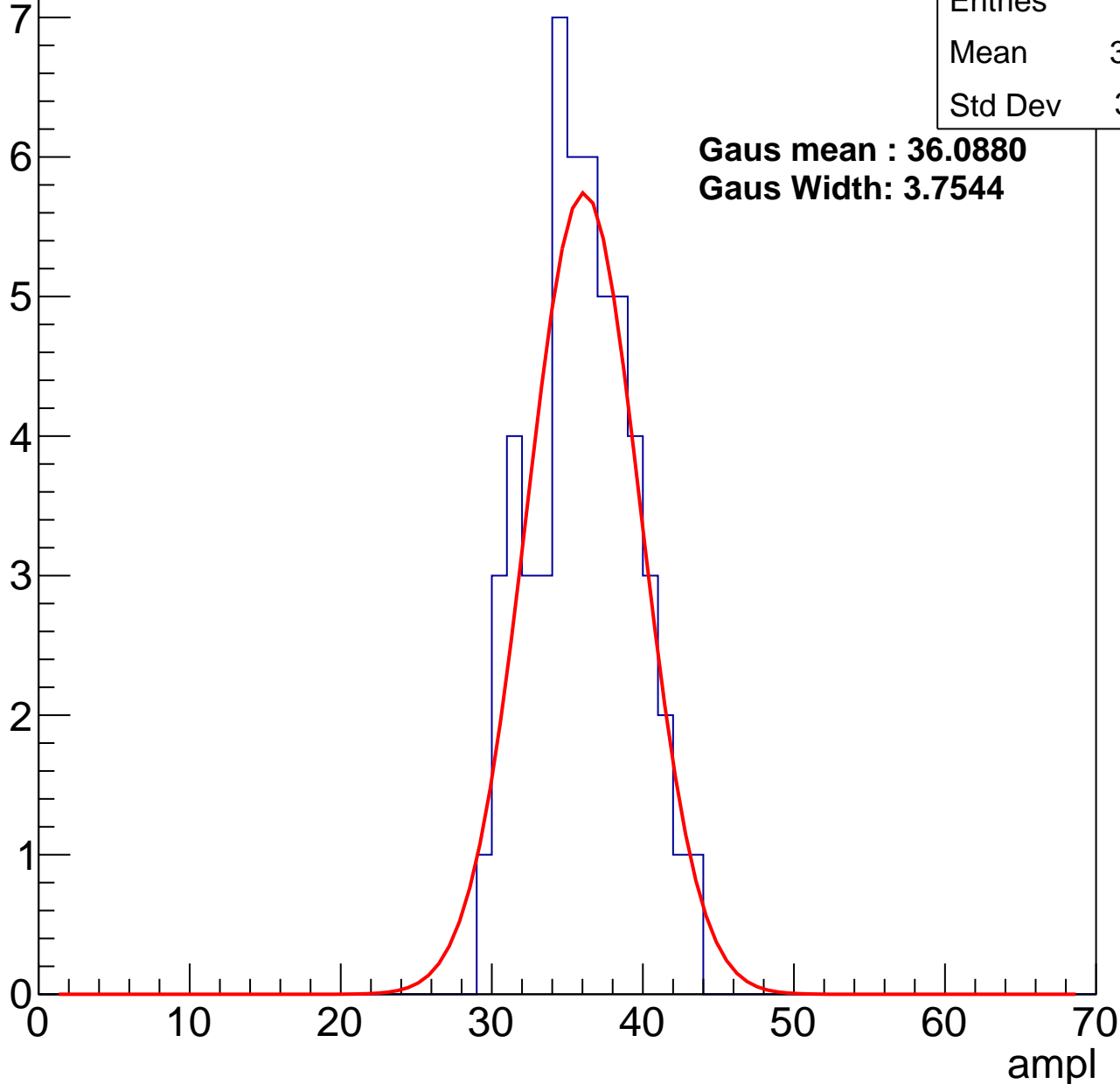
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	35.56
Std Dev	3.331

**Gaus mean : 36.0880**

**Gaus Width: 3.7544**



# B0L001S, U21-ch104, adc2

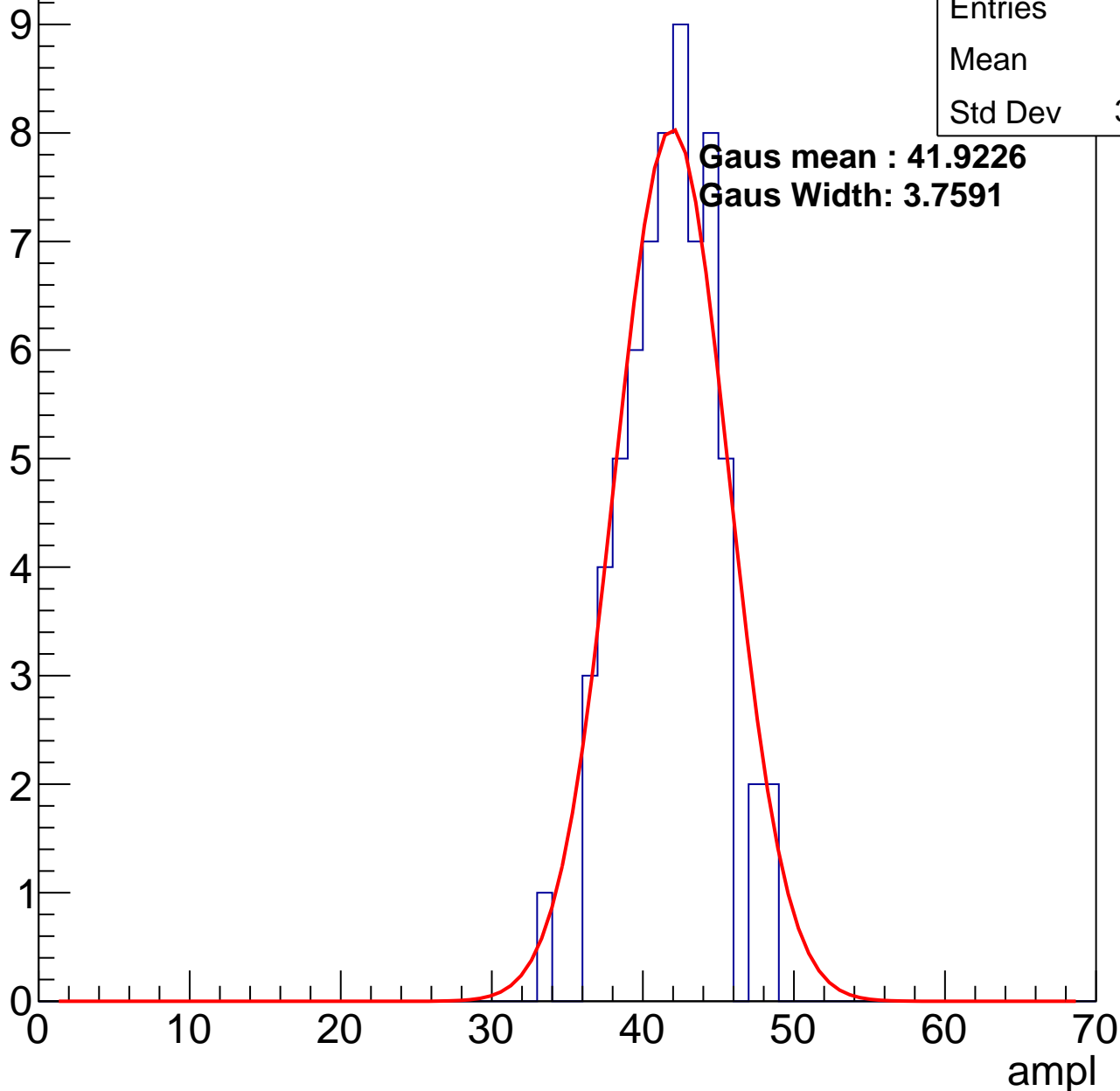
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	41.3
Std Dev	3.071

**Gaus mean : 41.9226**

**Gaus Width: 3.7591**



# B0L001S, U21-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

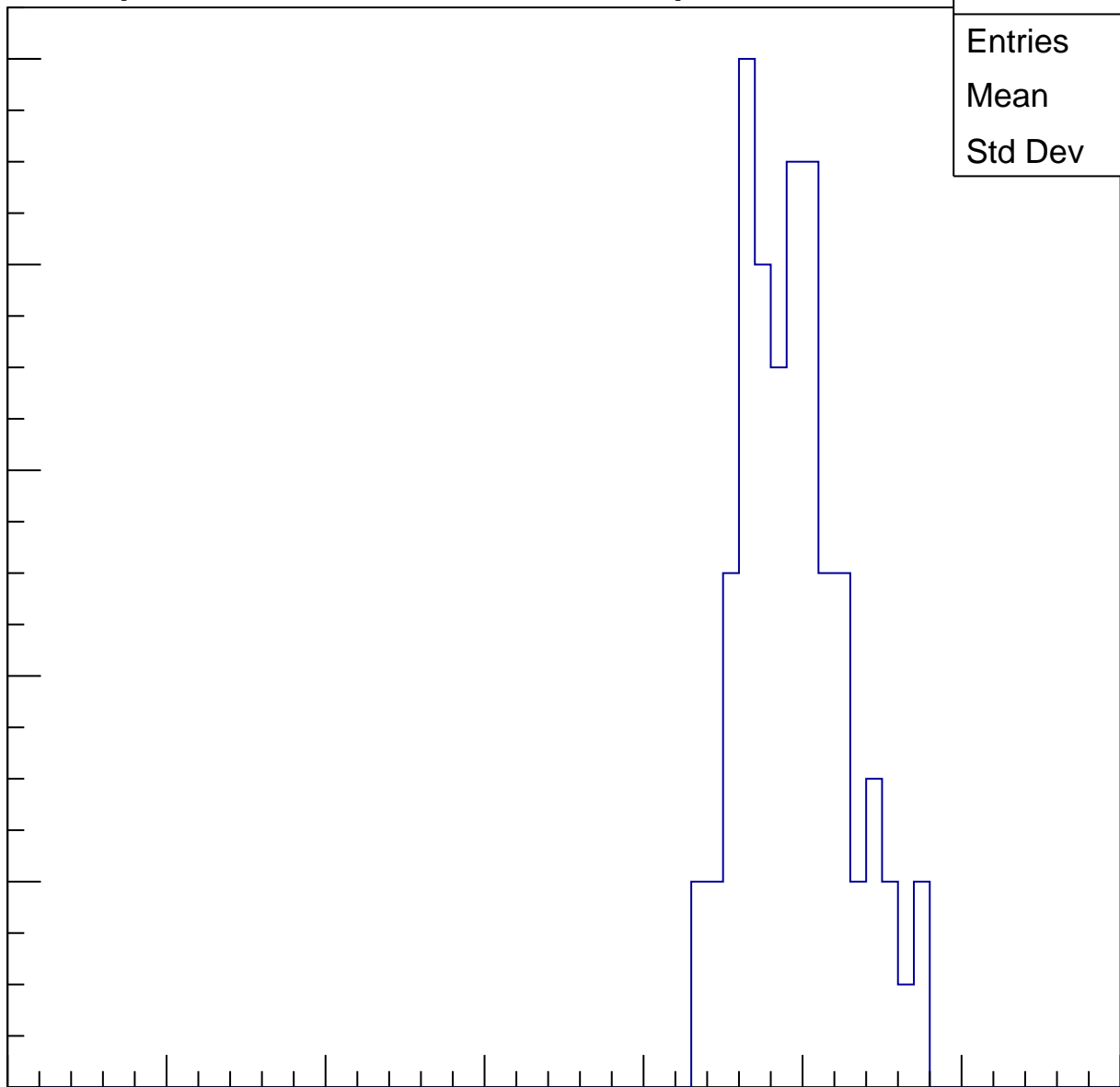
Entries	72
Mean	48.96
Std Dev	3.251

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

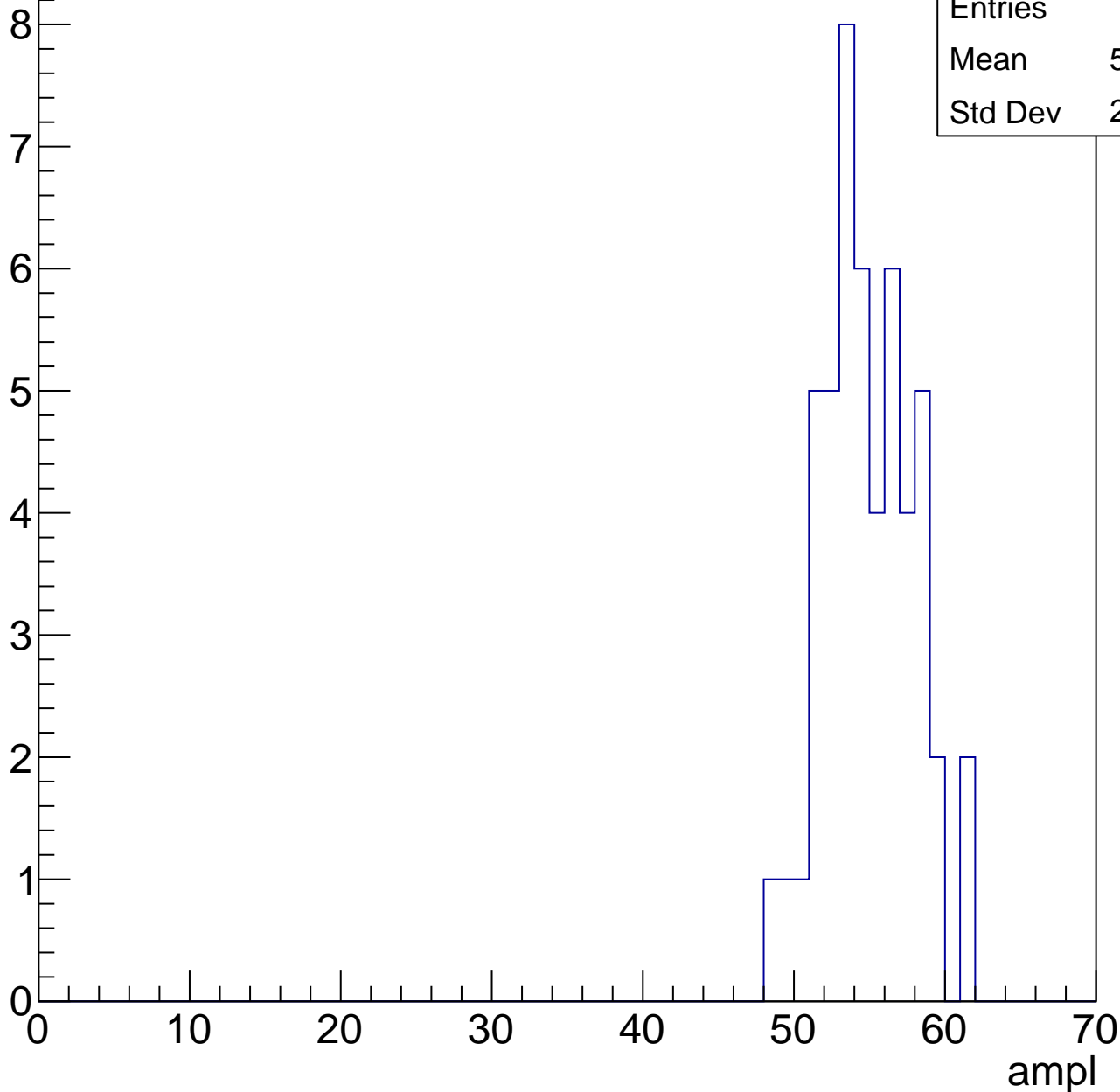


# B0L001S, U21-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

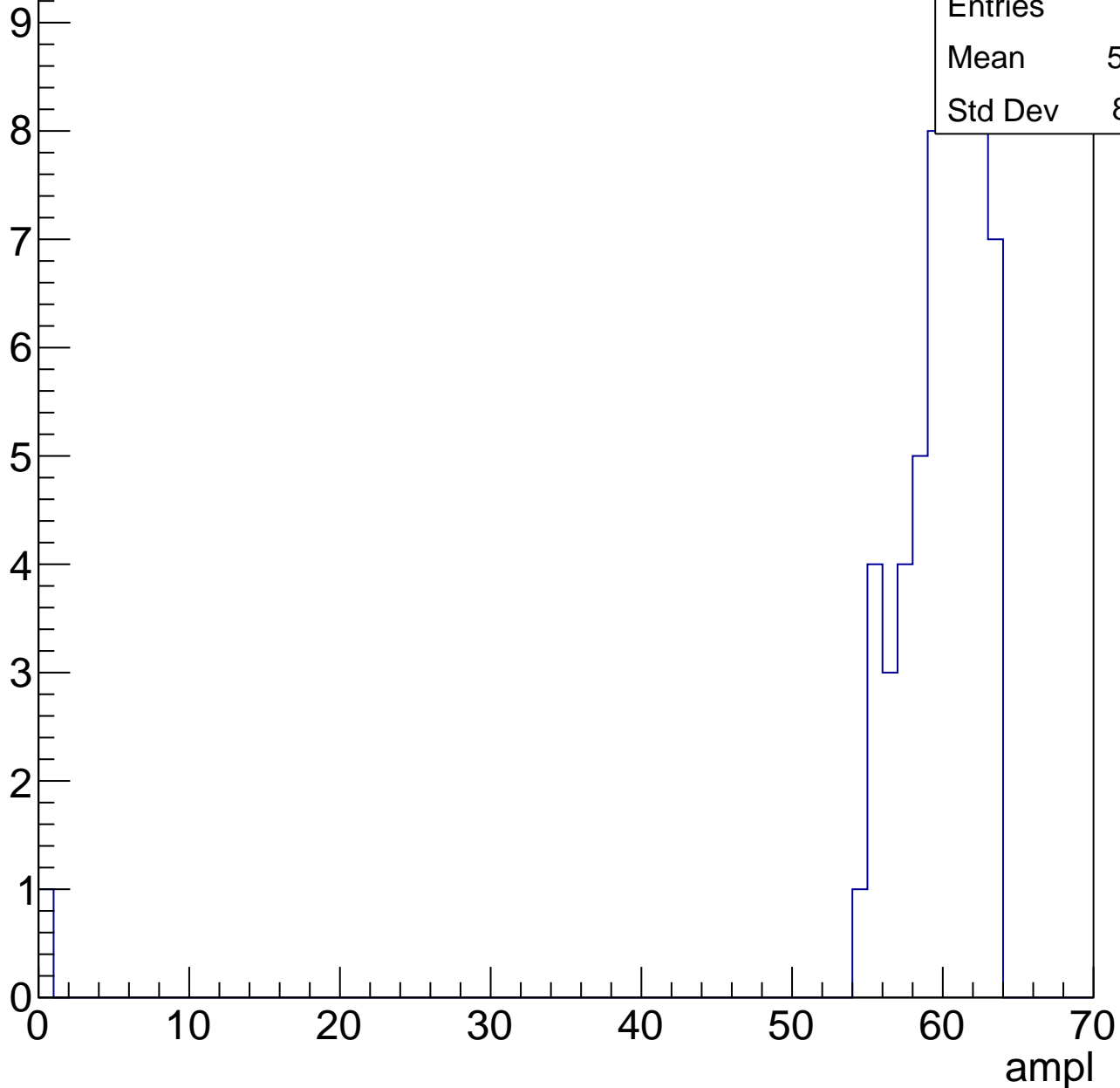
Entries	50
Mean	54.48
Std Dev	2.934



# B0L001S, U21-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U21-ch105, adc0

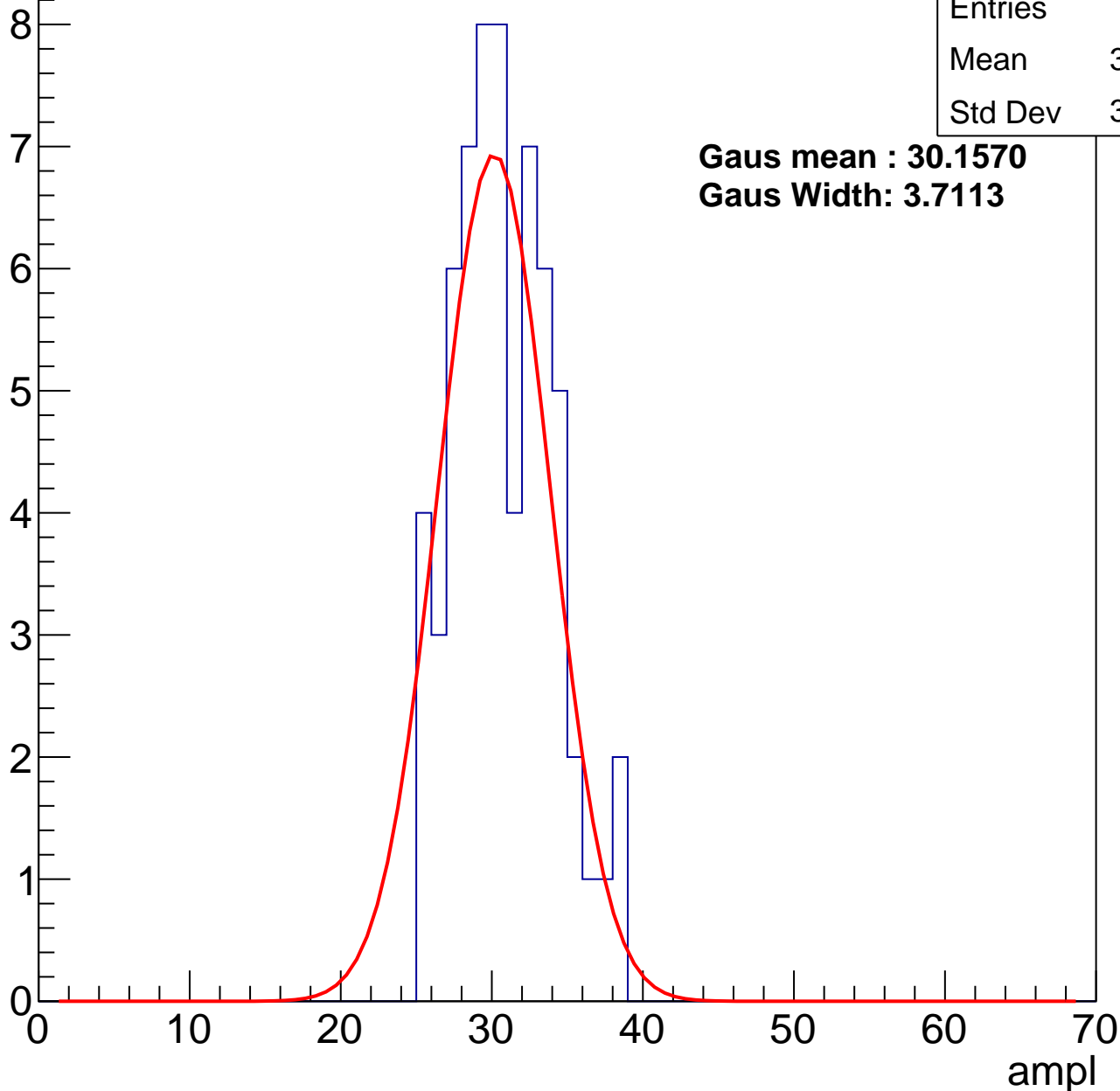
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	30.36
Std Dev	3.208

**Gaus mean : 30.1570**

**Gaus Width: 3.7113**



# B0L001S, U21-ch105, adc1

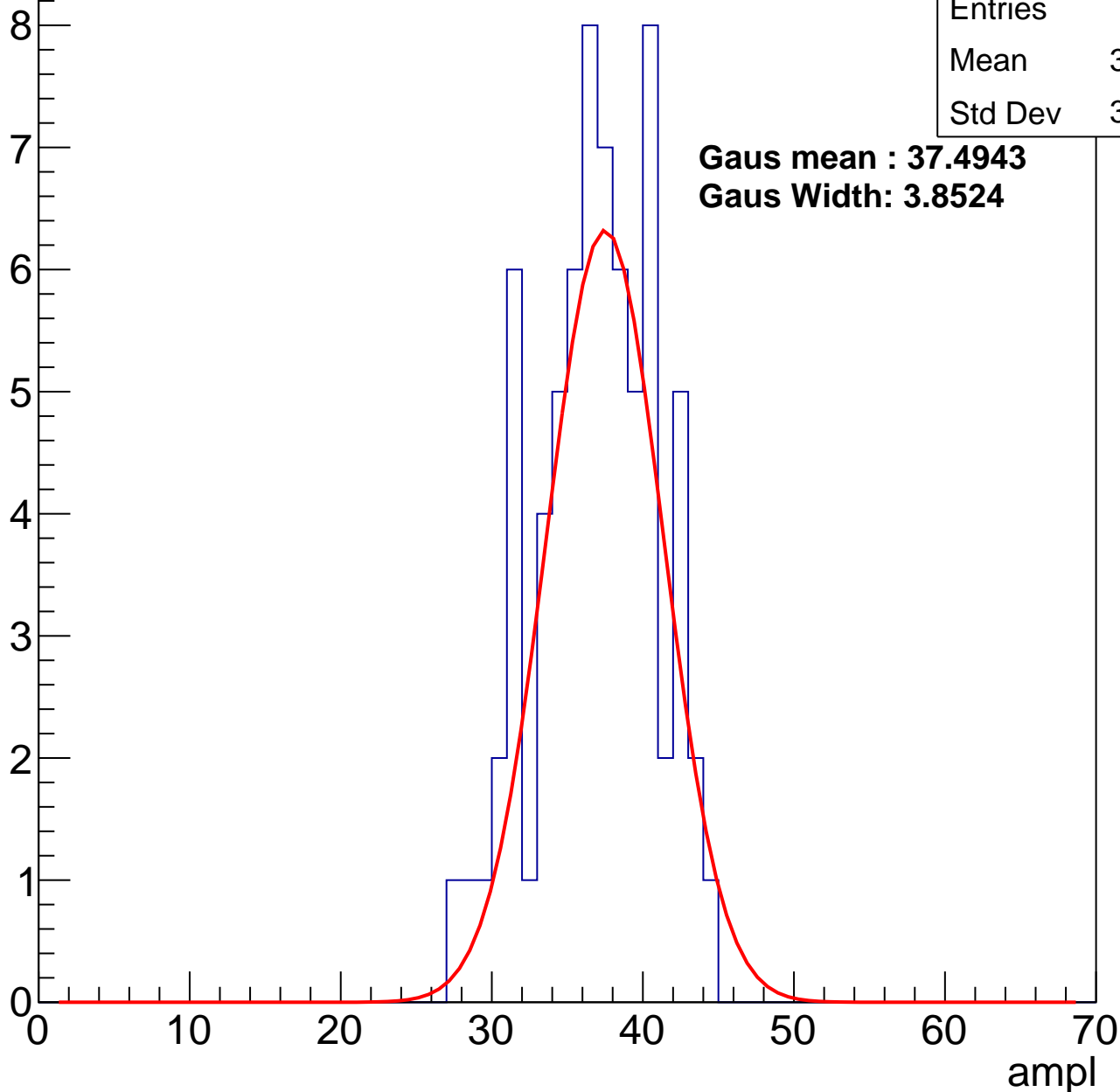
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	36.42
Std Dev	3.895

**Gaus mean : 37.4943**

**Gaus Width: 3.8524**



# B0L001S, U21-ch105, adc2

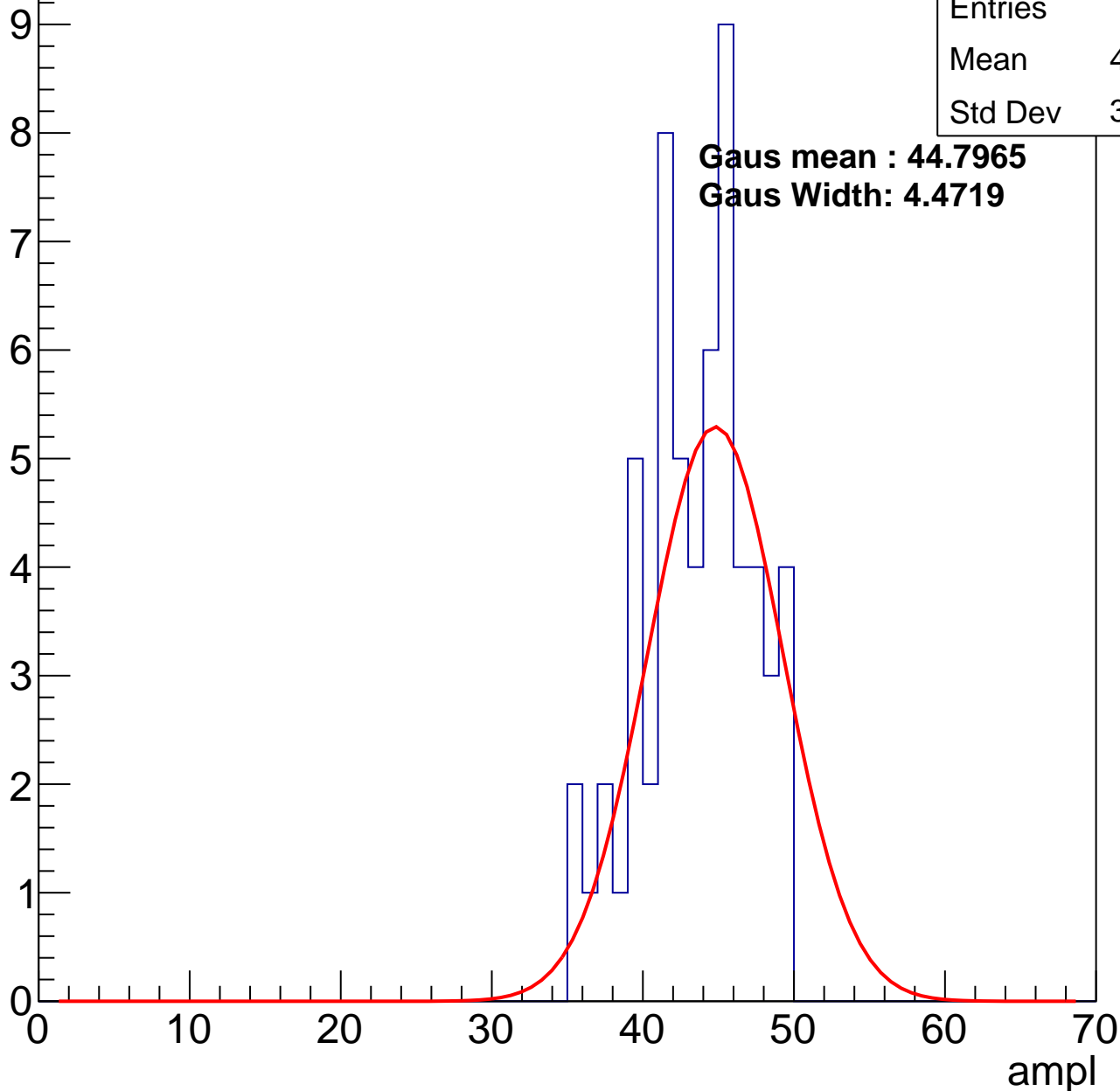
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	43.07
Std Dev	3.582

**Gaus mean : 44.7965**

**Gaus Width: 4.4719**

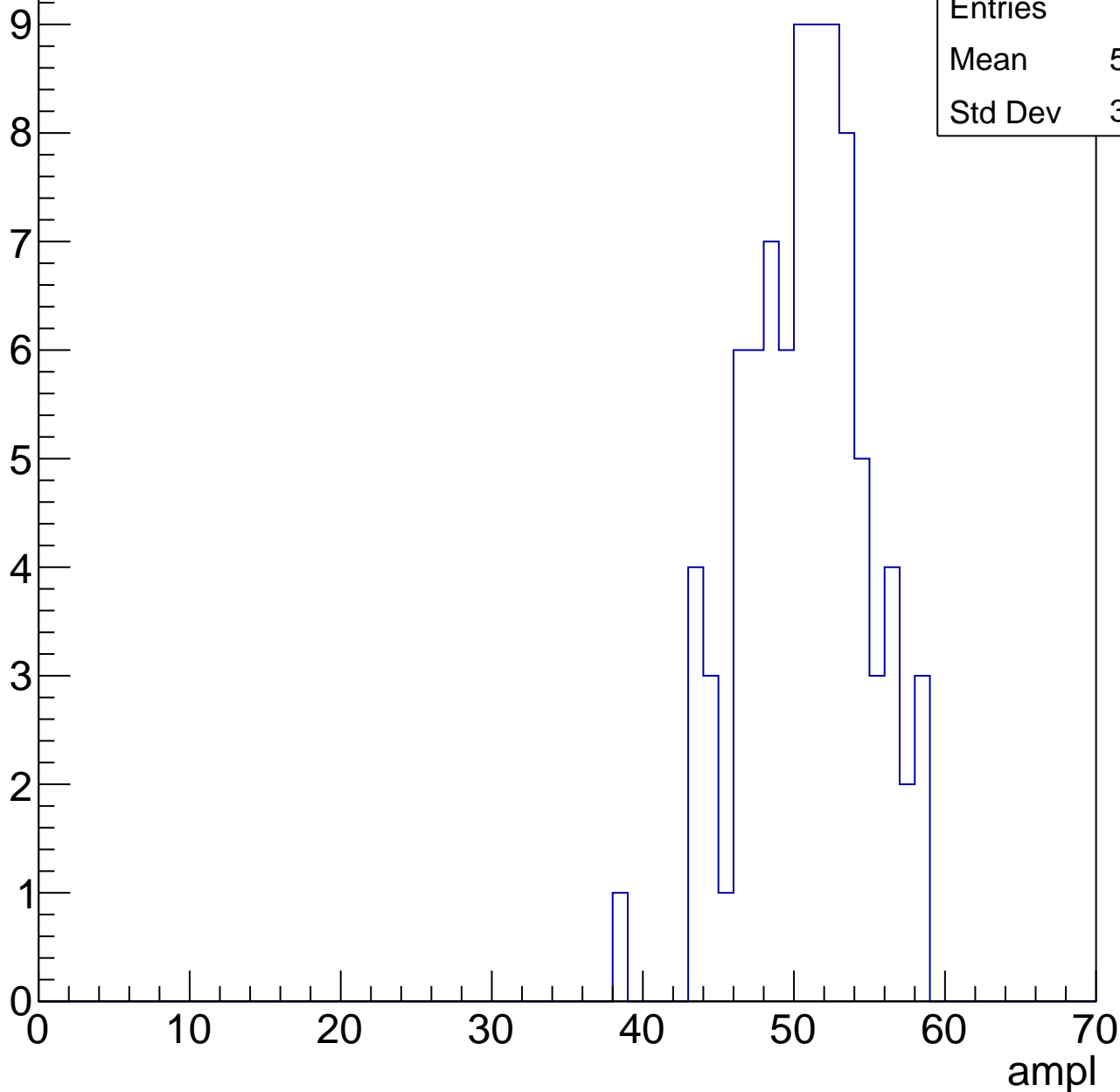


# B0L001S, U21-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	86
Mean	50.27
Std Dev	3.972

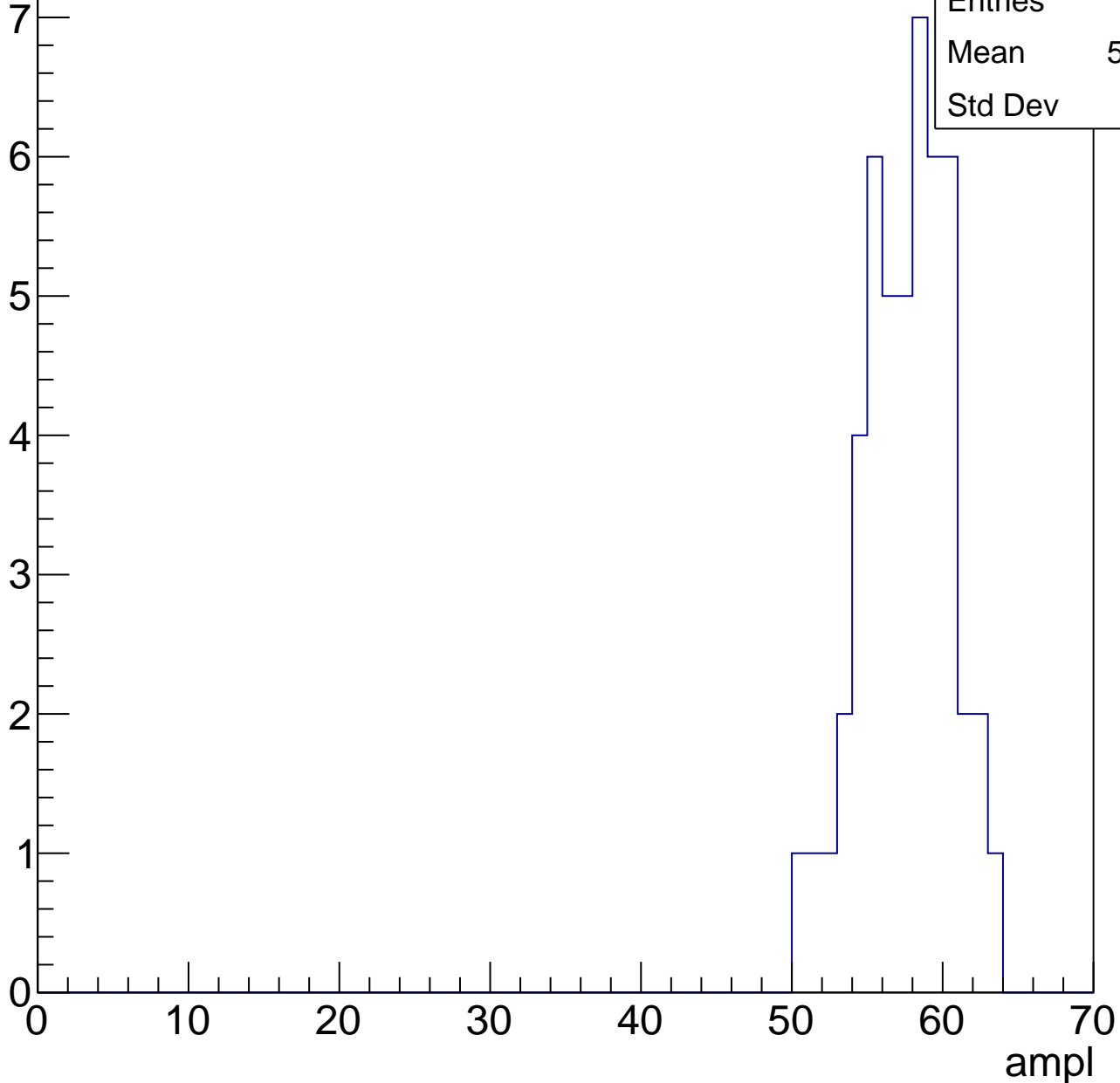


# B0L001S, U21-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	57.12
Std Dev	2.89

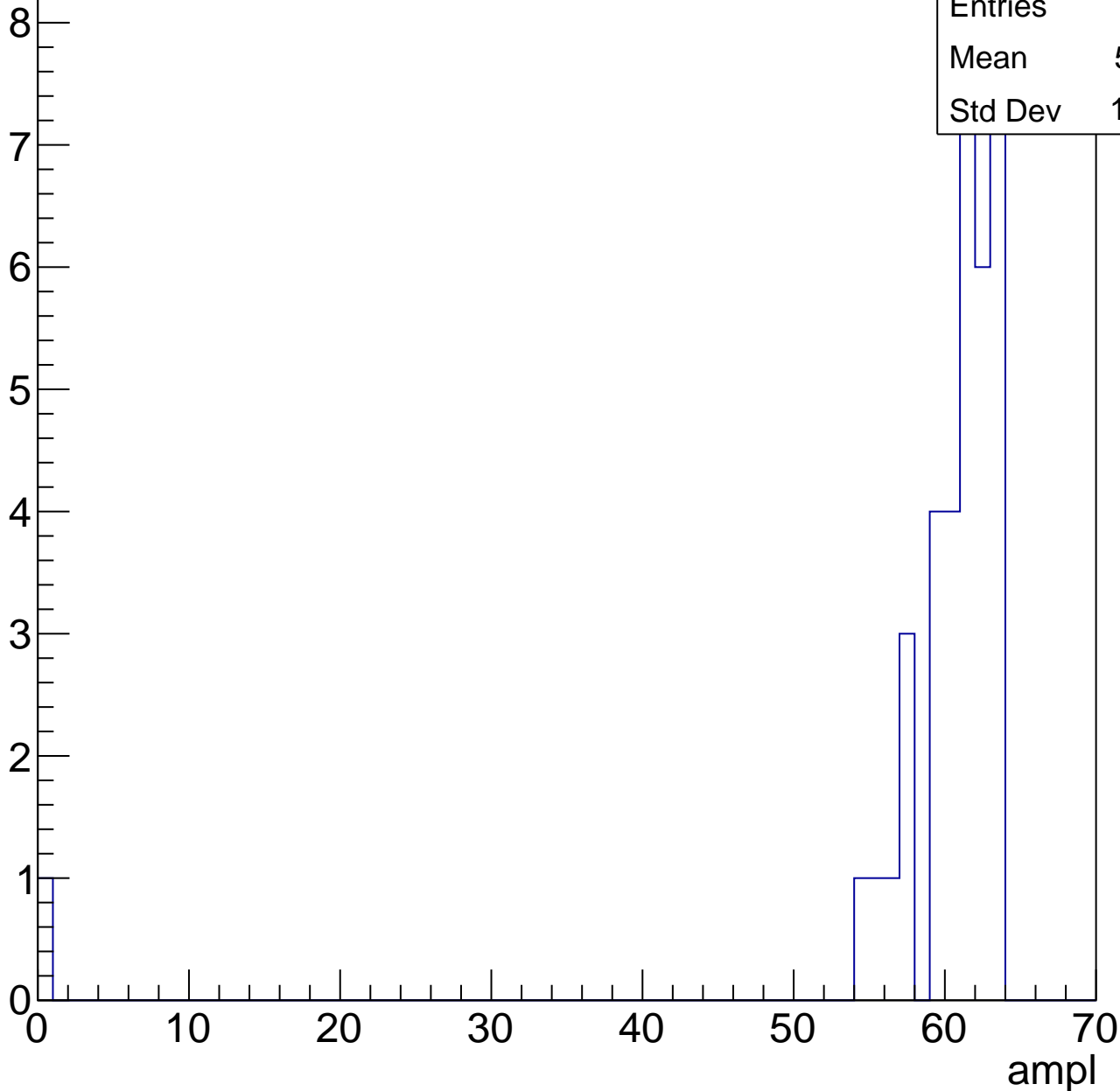


# B0L001S, U21-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	37
Mean	58.81
Std Dev	10.08



# B0L001S, U21-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch106, adc0

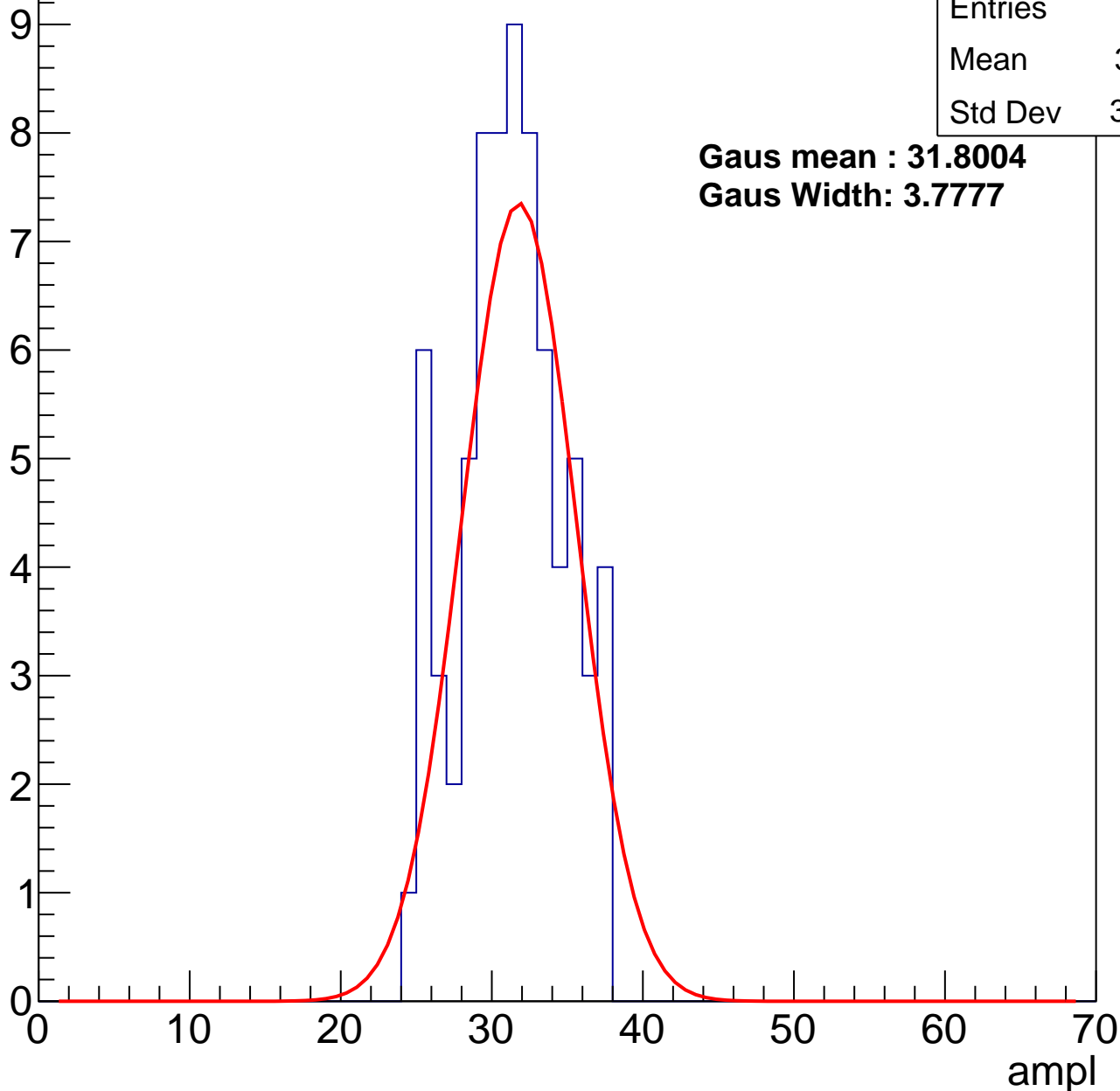
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	30.81
Std Dev	3.377

**Gaus mean : 31.8004**

**Gaus Width: 3.7777**



# B0L001S, U21-ch106, adc1

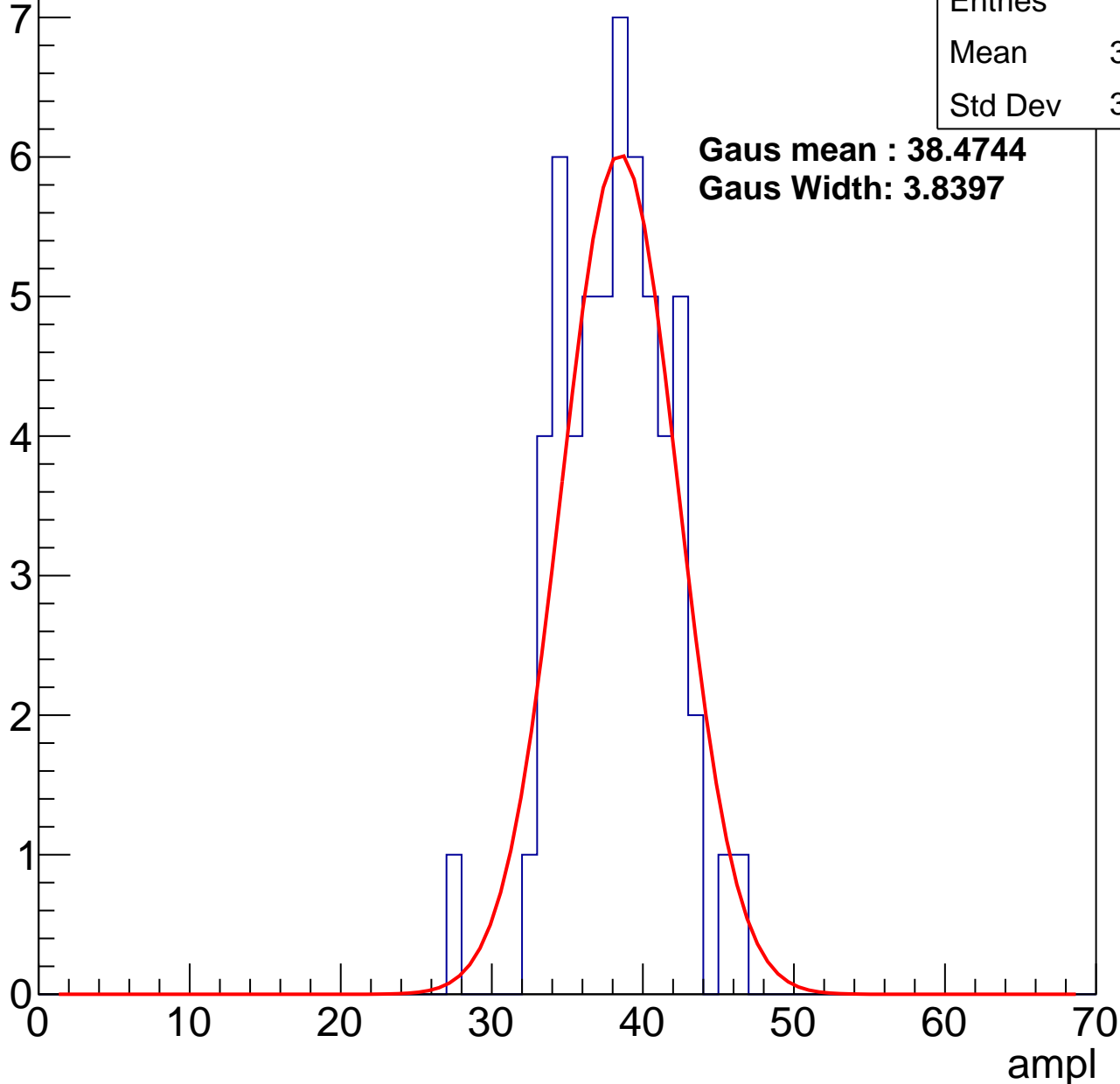
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	37.74
Std Dev	3.542

**Gaus mean : 38.4744**

**Gaus Width: 3.8397**



# B0L001S, U21-ch106, adc2

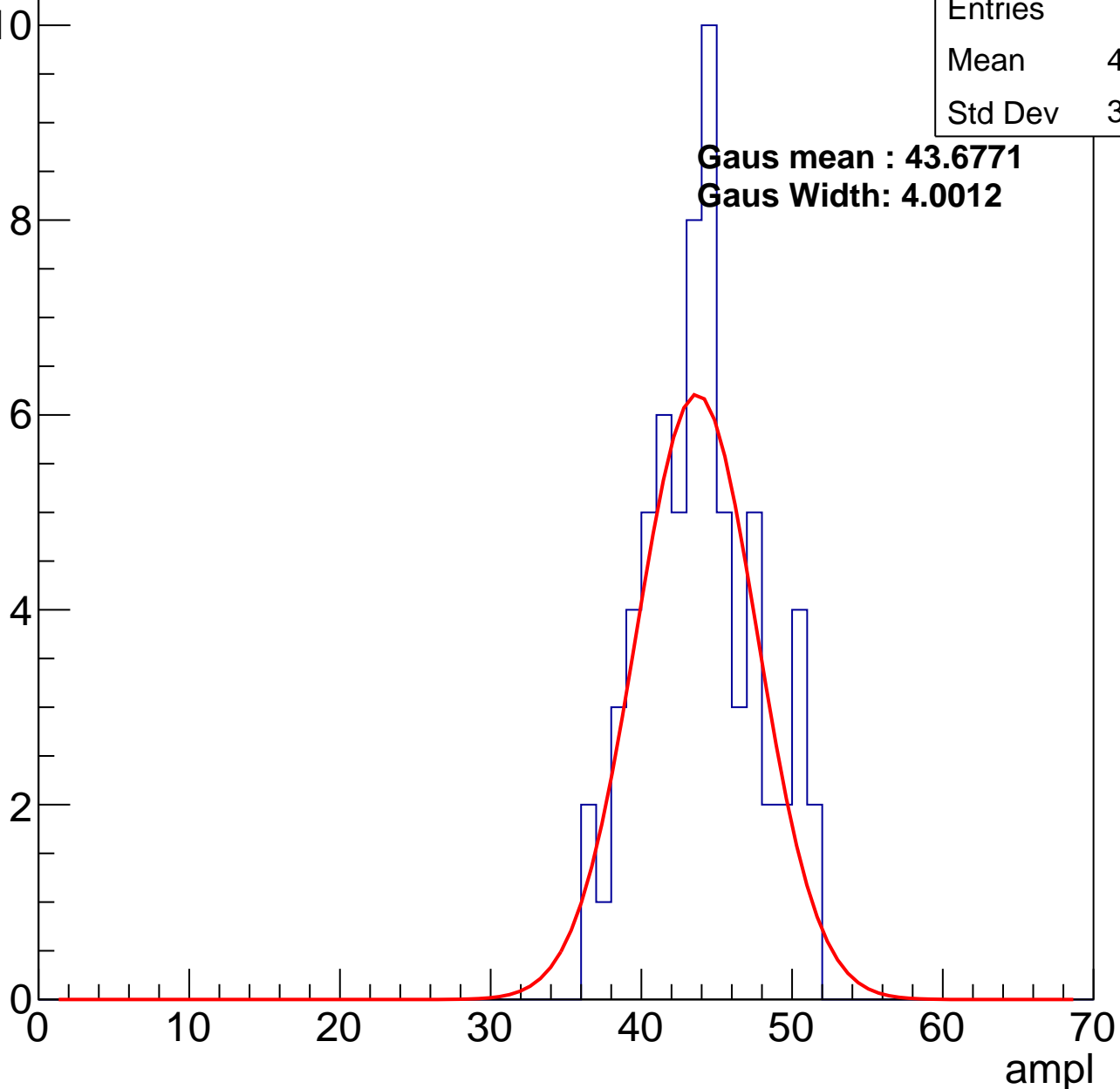
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	43.48
Std Dev	3.695

**Gaus mean : 43.6771**

**Gaus Width: 4.0012**

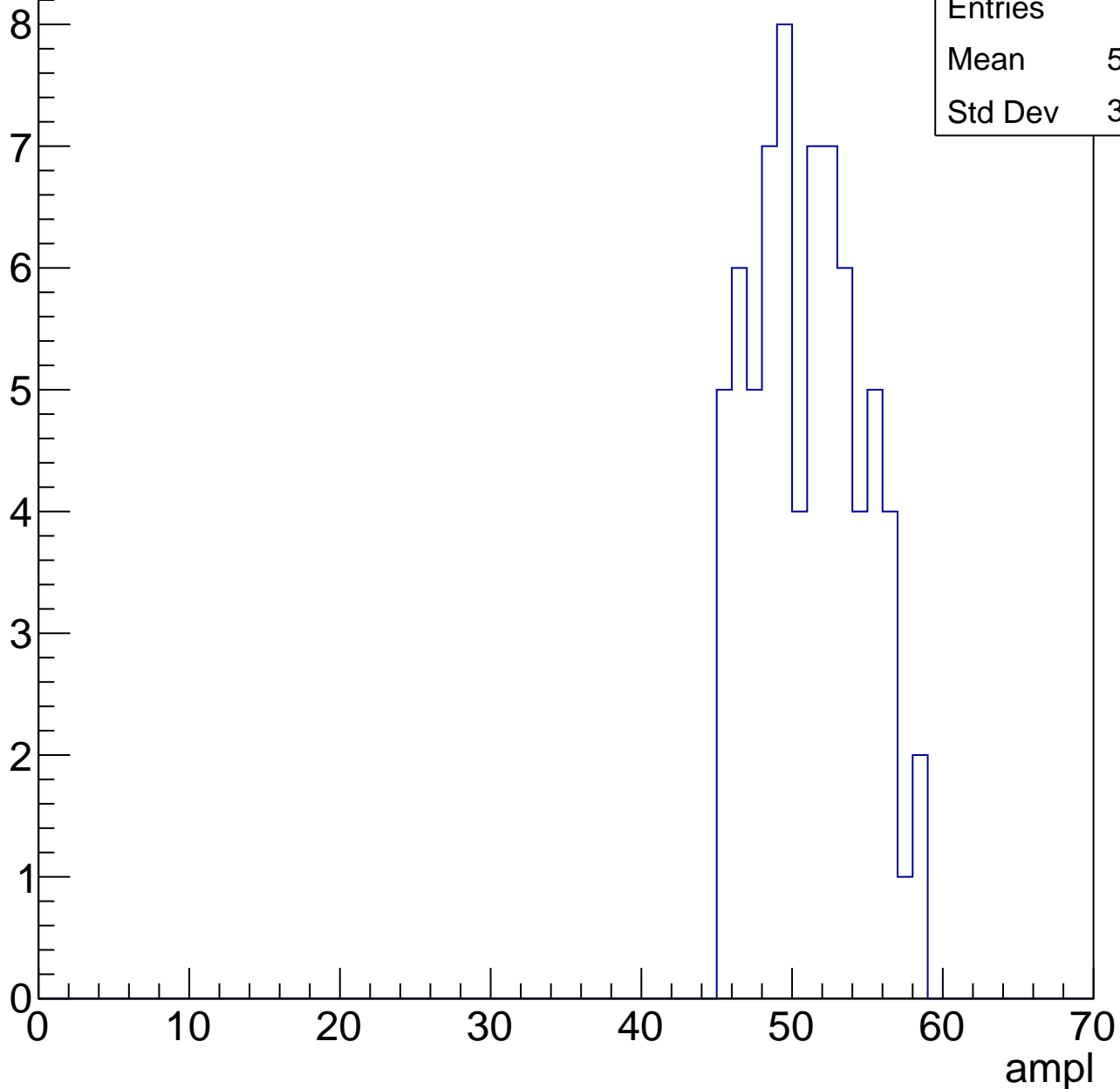


# B0L001S, U21-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	50.58
Std Dev	3.515

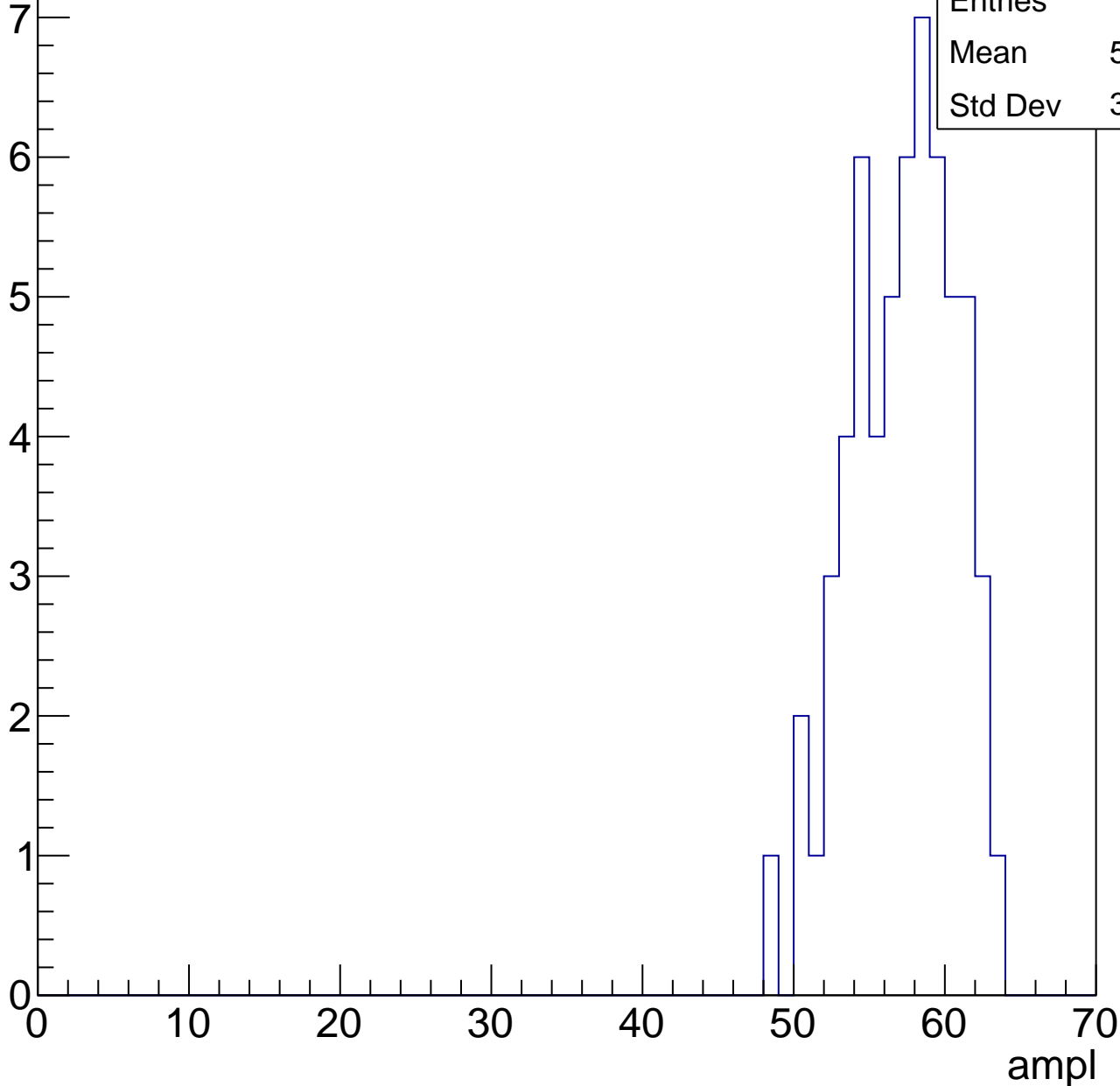


# B0L001S, U21-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	56.73
Std Dev	3.424

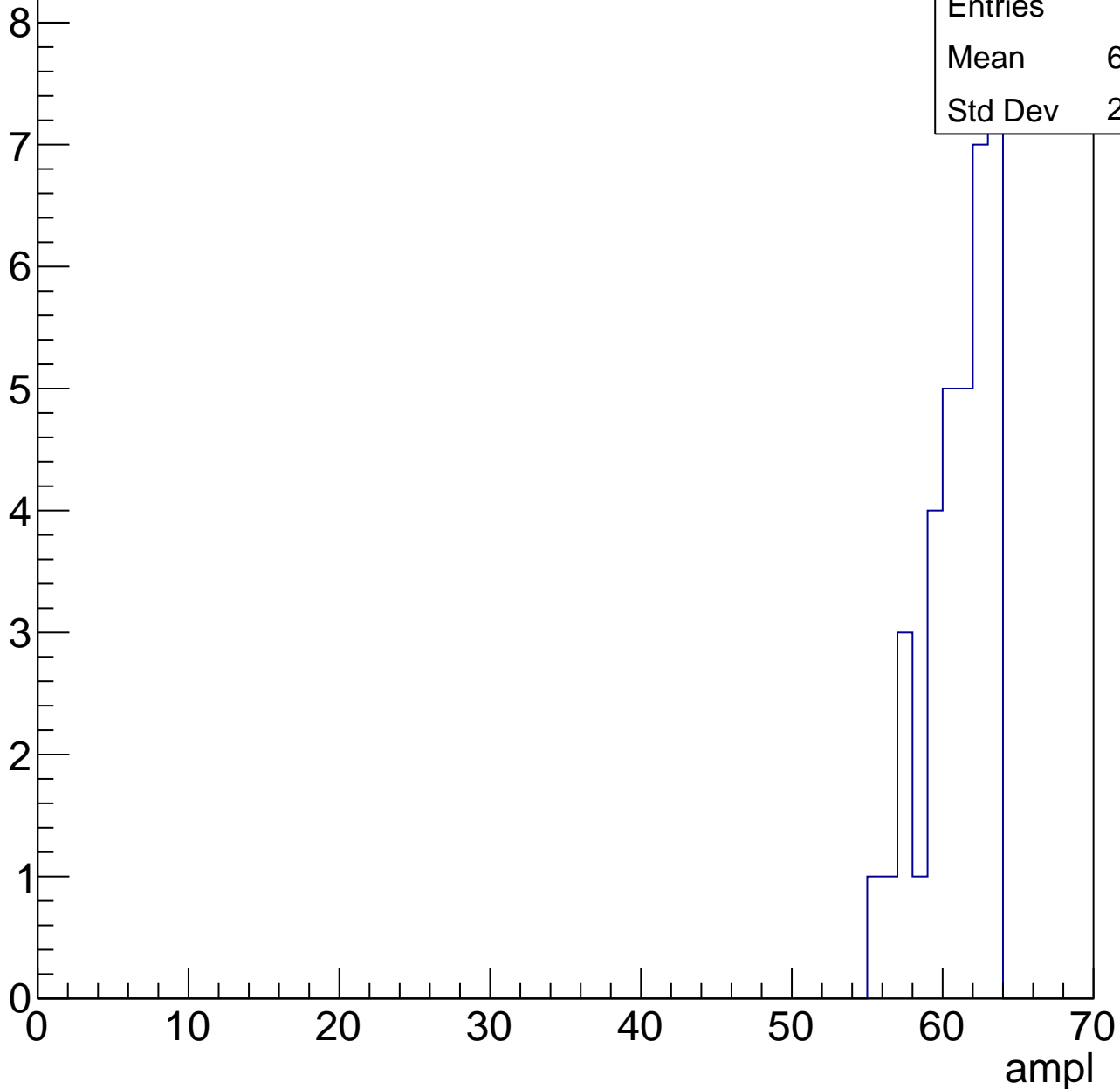


# B0L001S, U21-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

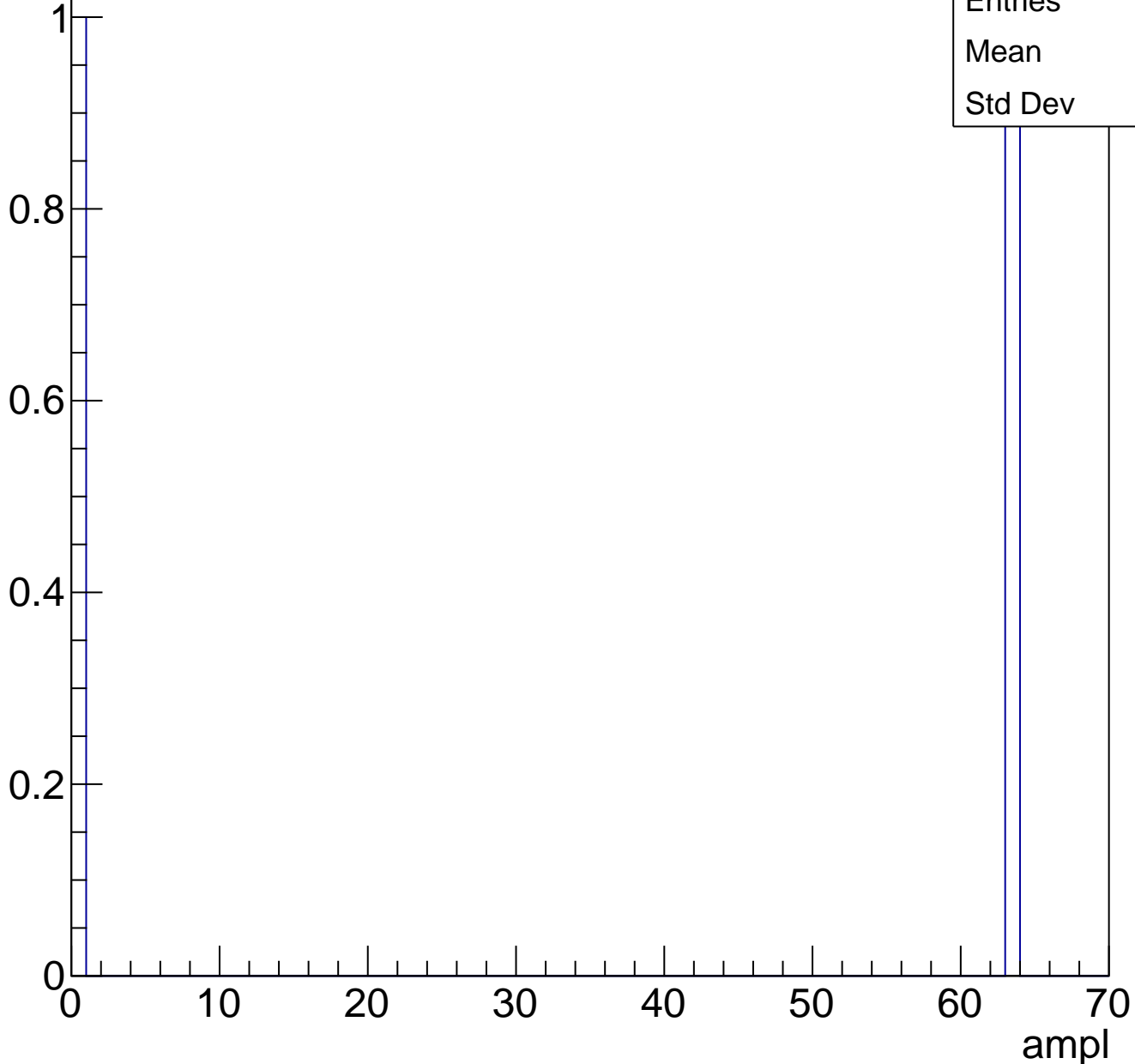
Entries	35
Mean	60.54
Std Dev	2.208



# B0L001S, U21-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch107, adc0

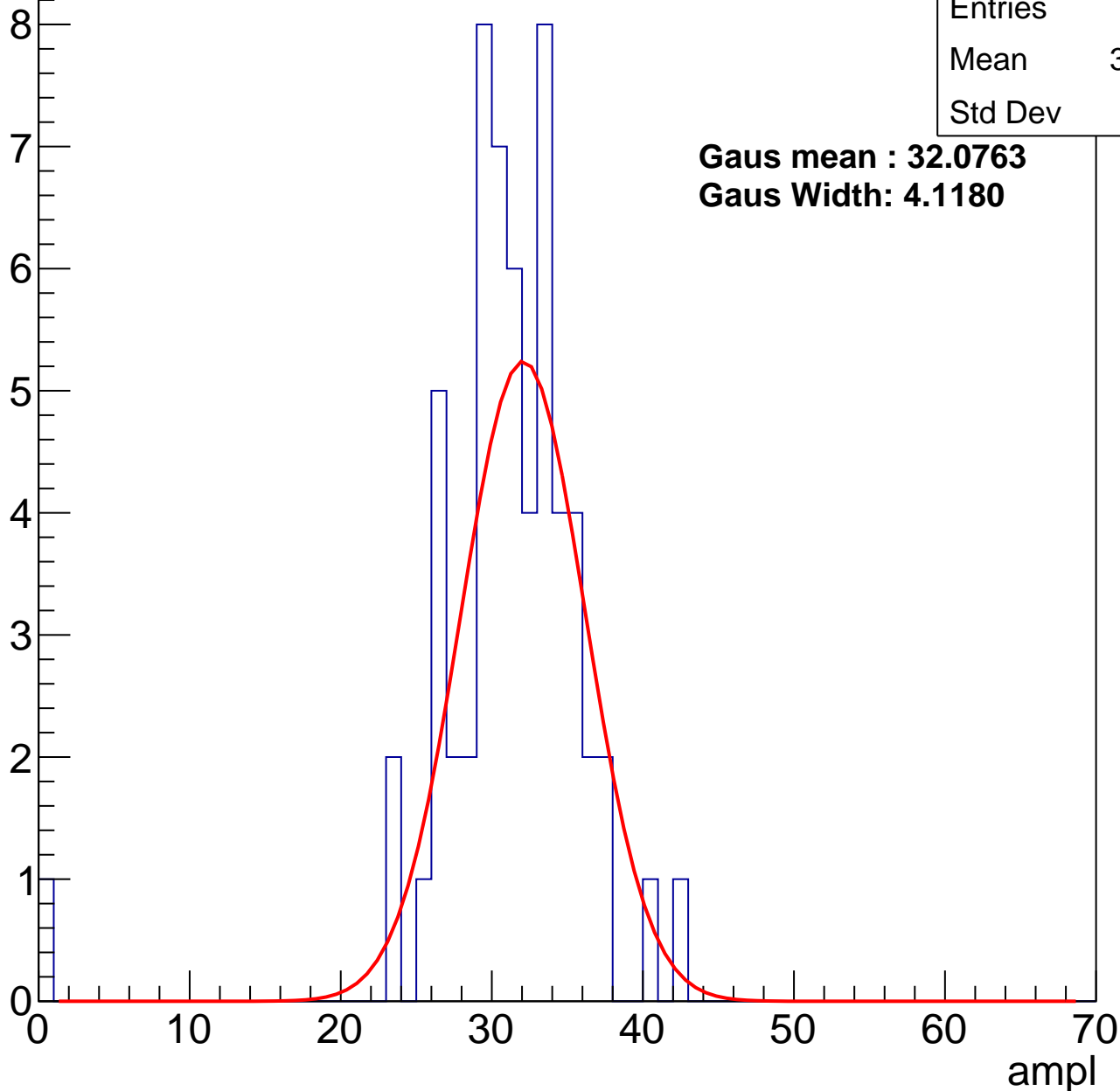
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	30.58
Std Dev	5.46

**Gaus mean : 32.0763**

**Gaus Width: 4.1180**



# B0L001S, U21-ch107, adc1

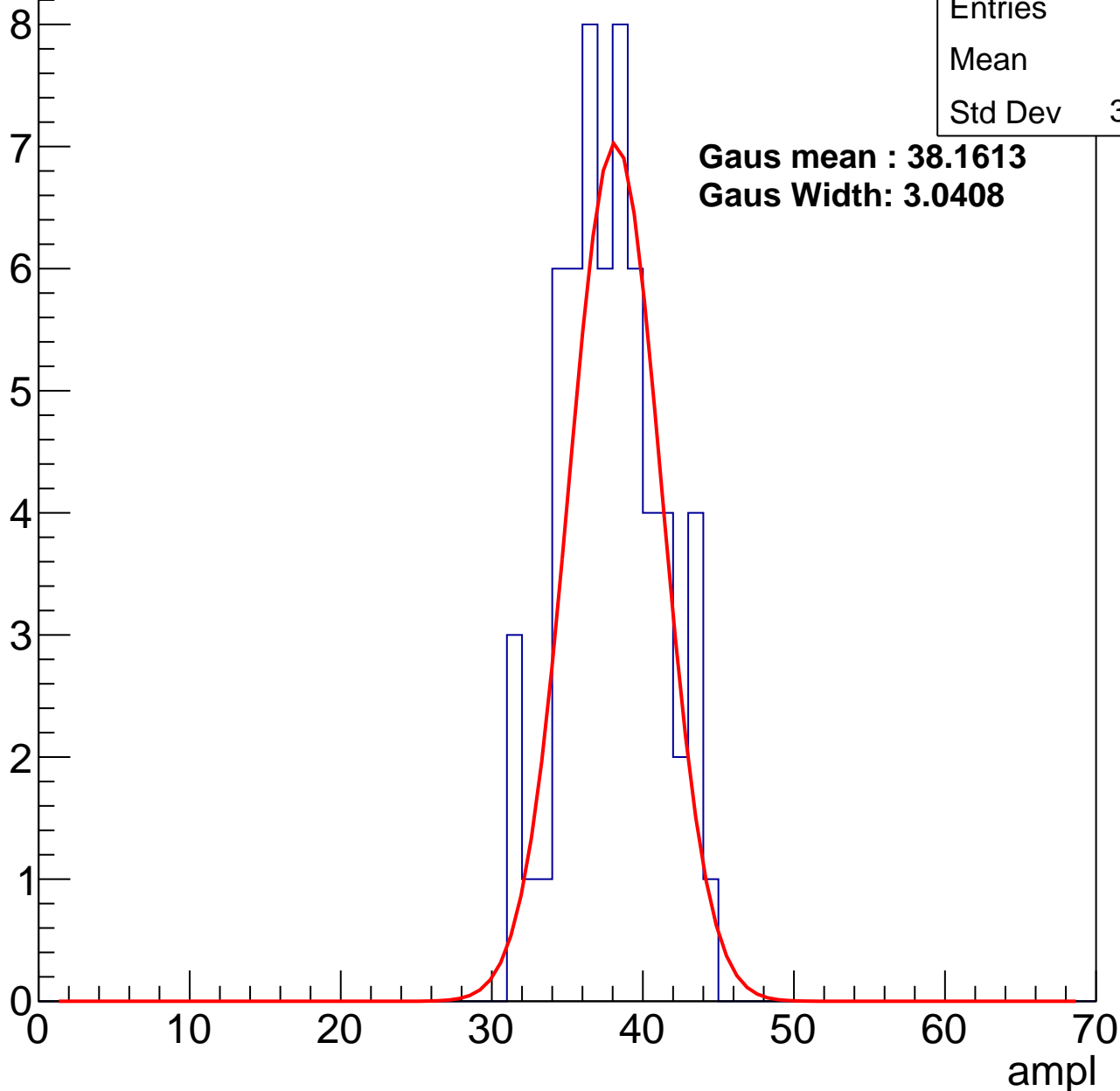
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	37.4
Std Dev	3.163

**Gaus mean : 38.1613**

**Gaus Width: 3.0408**



# B0L001S, U21-ch107, adc2

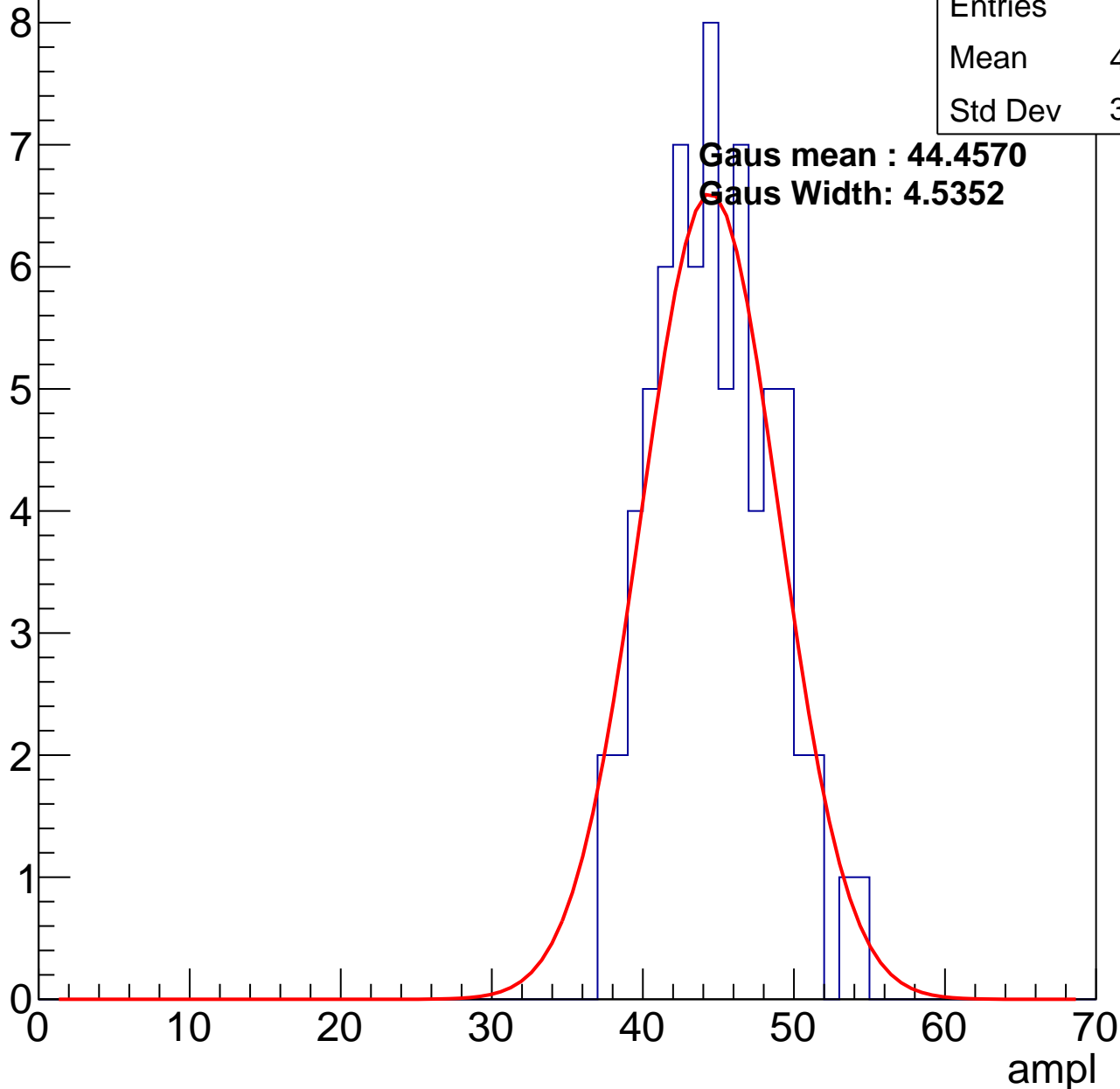
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	44.24
Std Dev	3.835

**Gaus mean : 44.4570**

**Gaus Width: 4.5352**

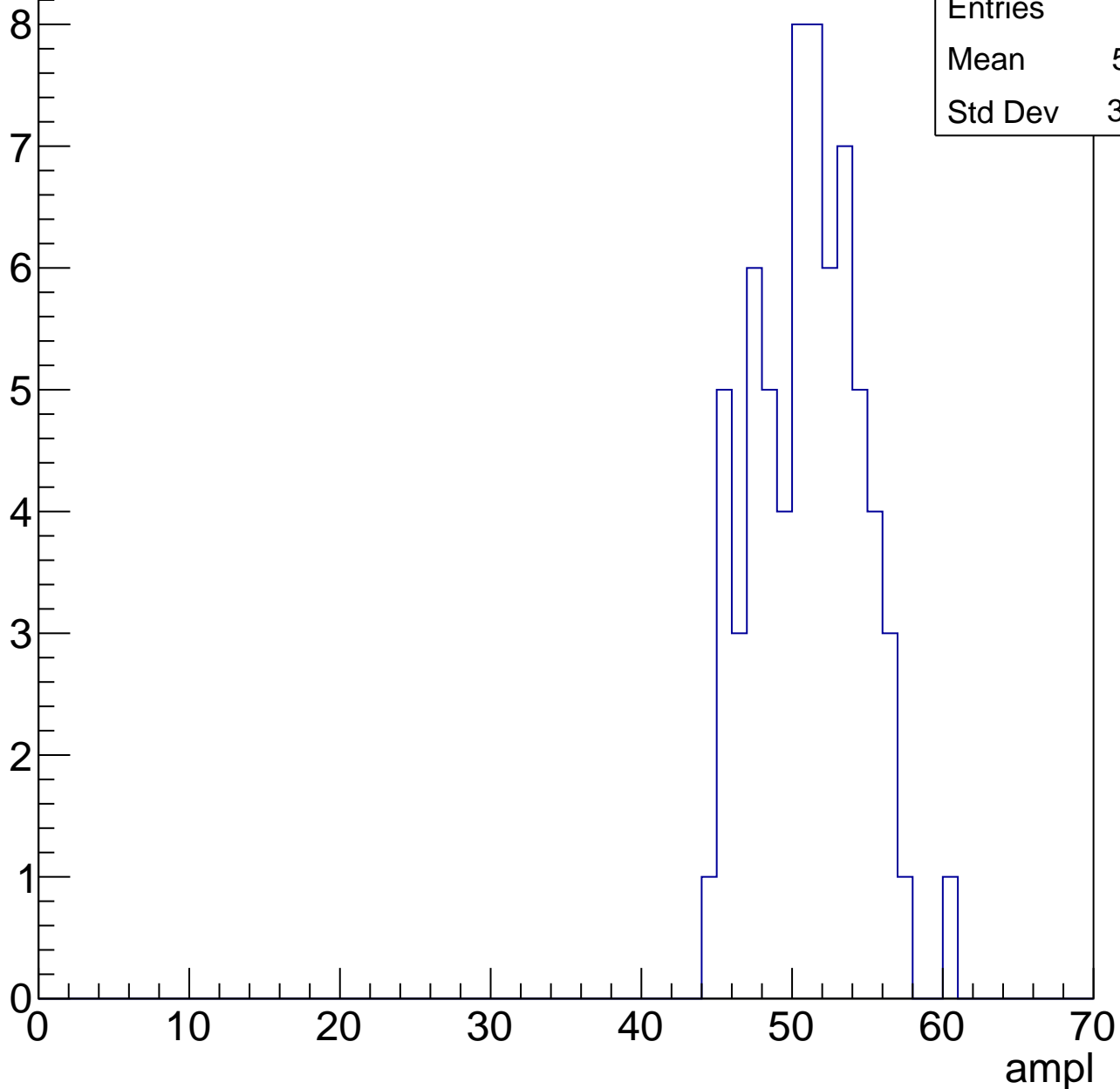


# B0L001S, U21-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	50.61
Std Dev	3.442

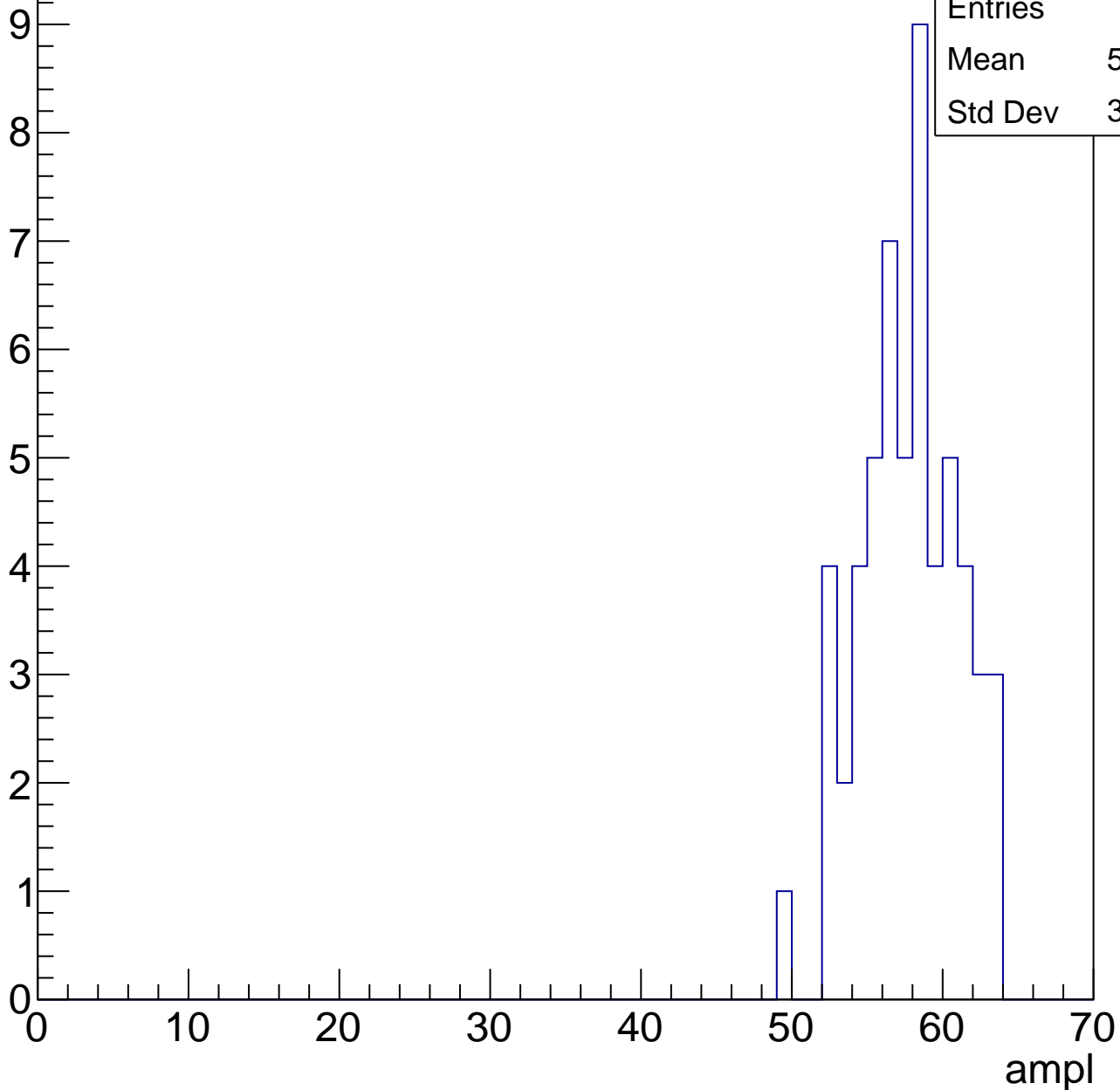


# B0L001S, U21-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	57.29
Std Dev	3.194

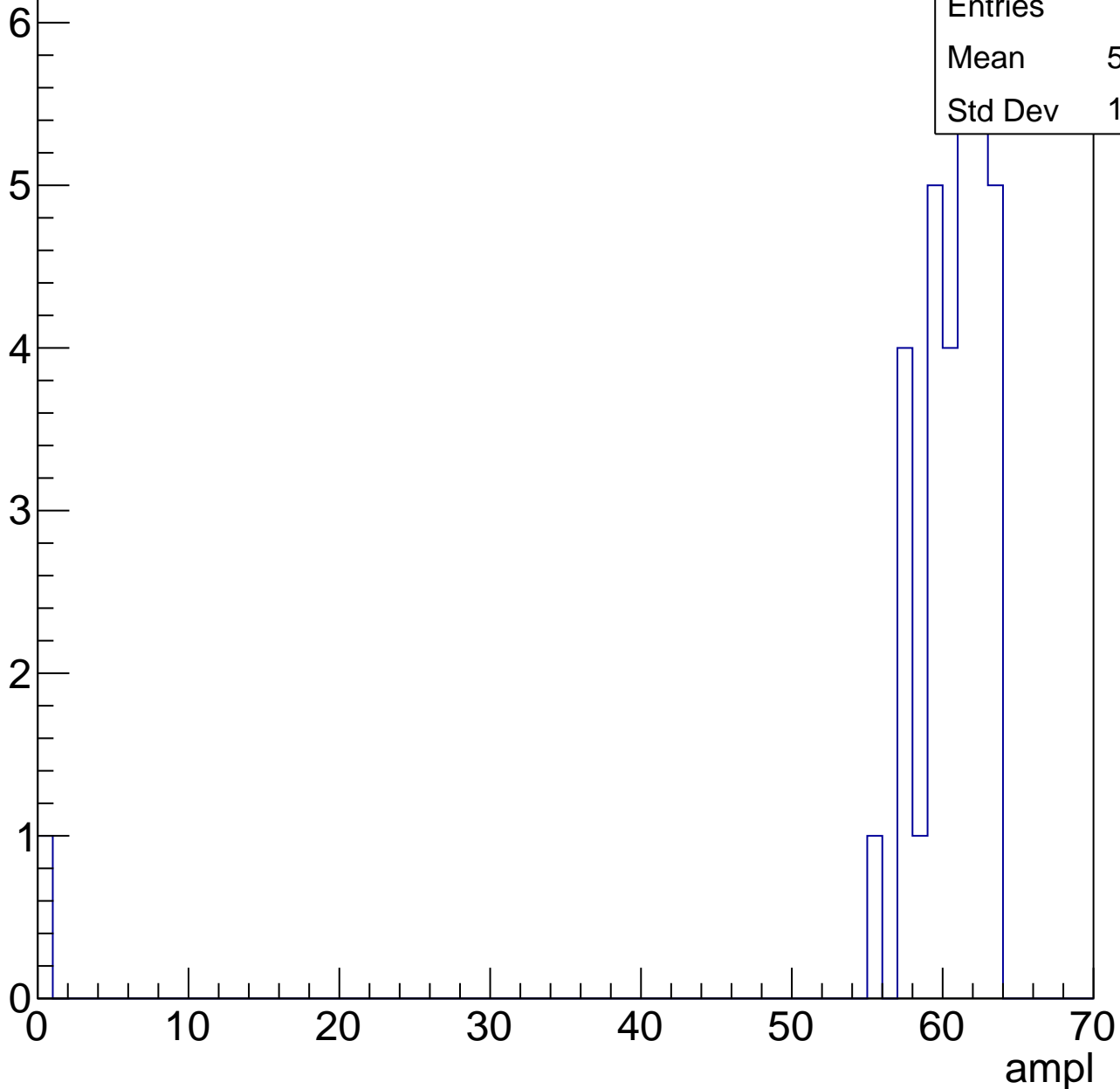


# B0L001S, U21-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	33
Mean	58.45
Std Dev	10.54



# B0L001S, U21-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U21-ch108, adc0

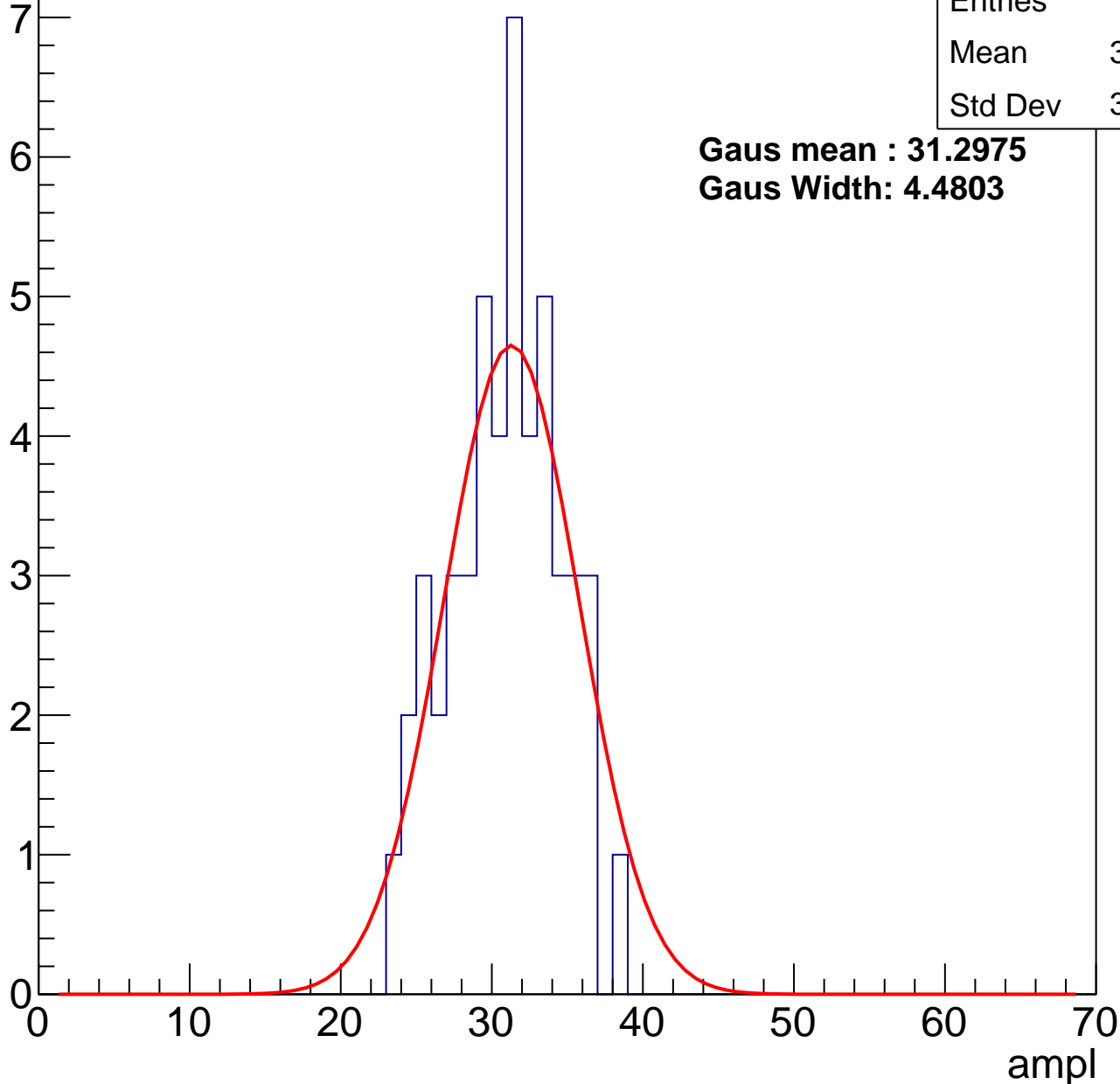
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	30.43
Std Dev	3.574

**Gaus mean : 31.2975**

**Gaus Width: 4.4803**



# B0L001S, U21-ch108, adc1

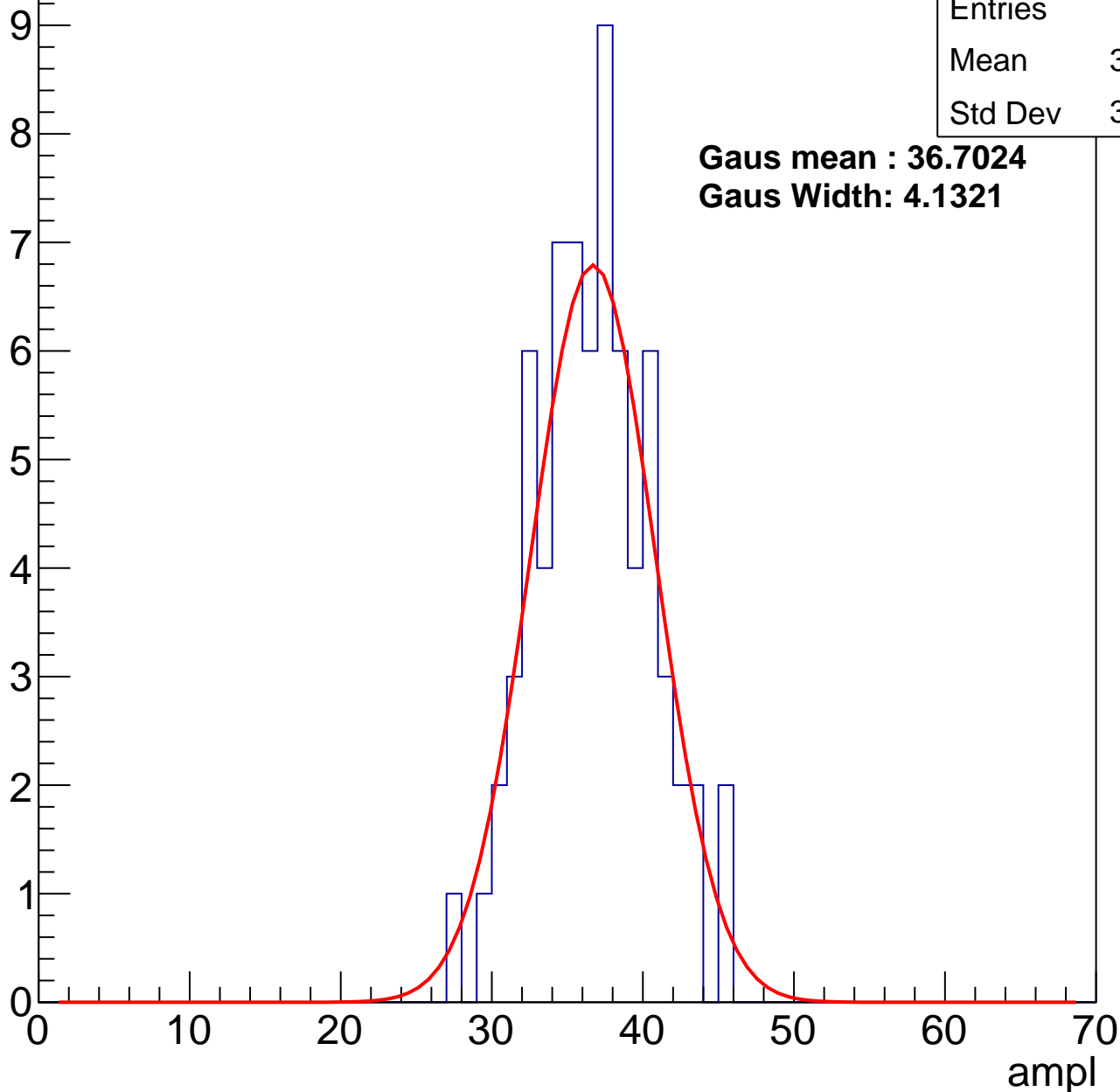
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	36.23
Std Dev	3.776

**Gaus mean : 36.7024**

**Gaus Width: 4.1321**



# B0L001S, U21-ch108, adc2

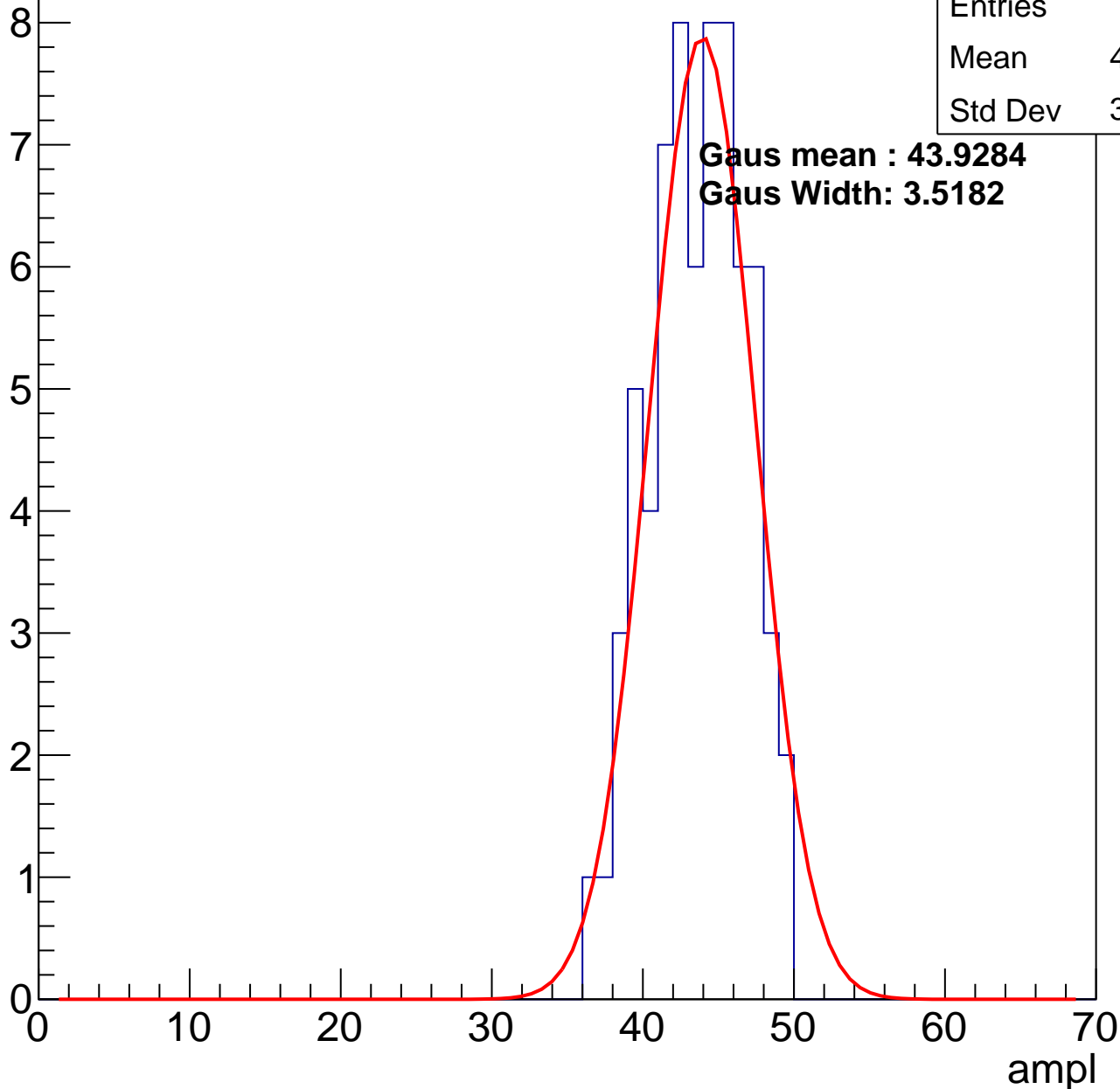
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	43.16
Std Dev	3.085

**Gaus mean : 43.9284**

**Gaus Width: 3.5182**

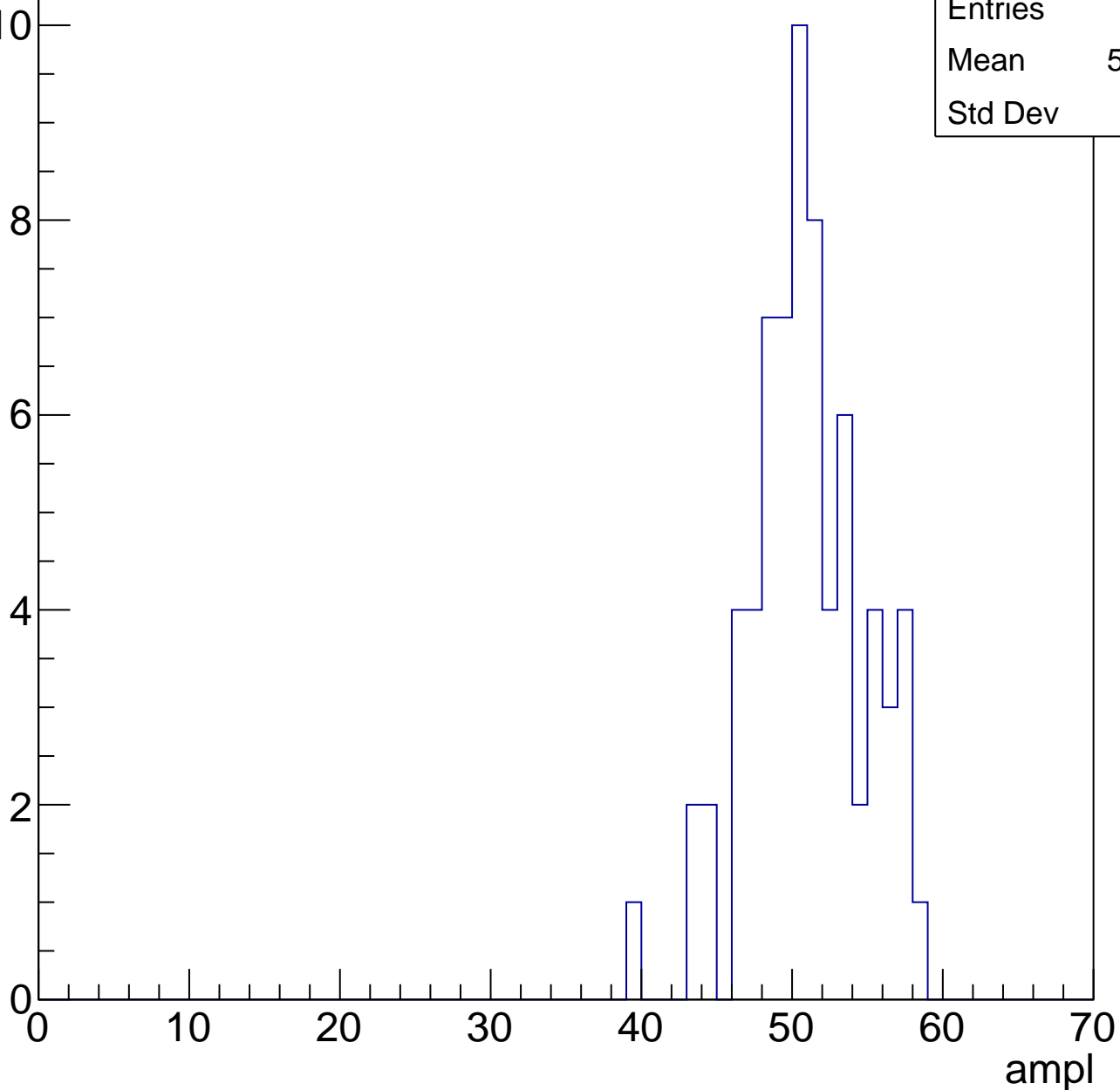


# B0L001S, U21-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	50.43
Std Dev	3.79

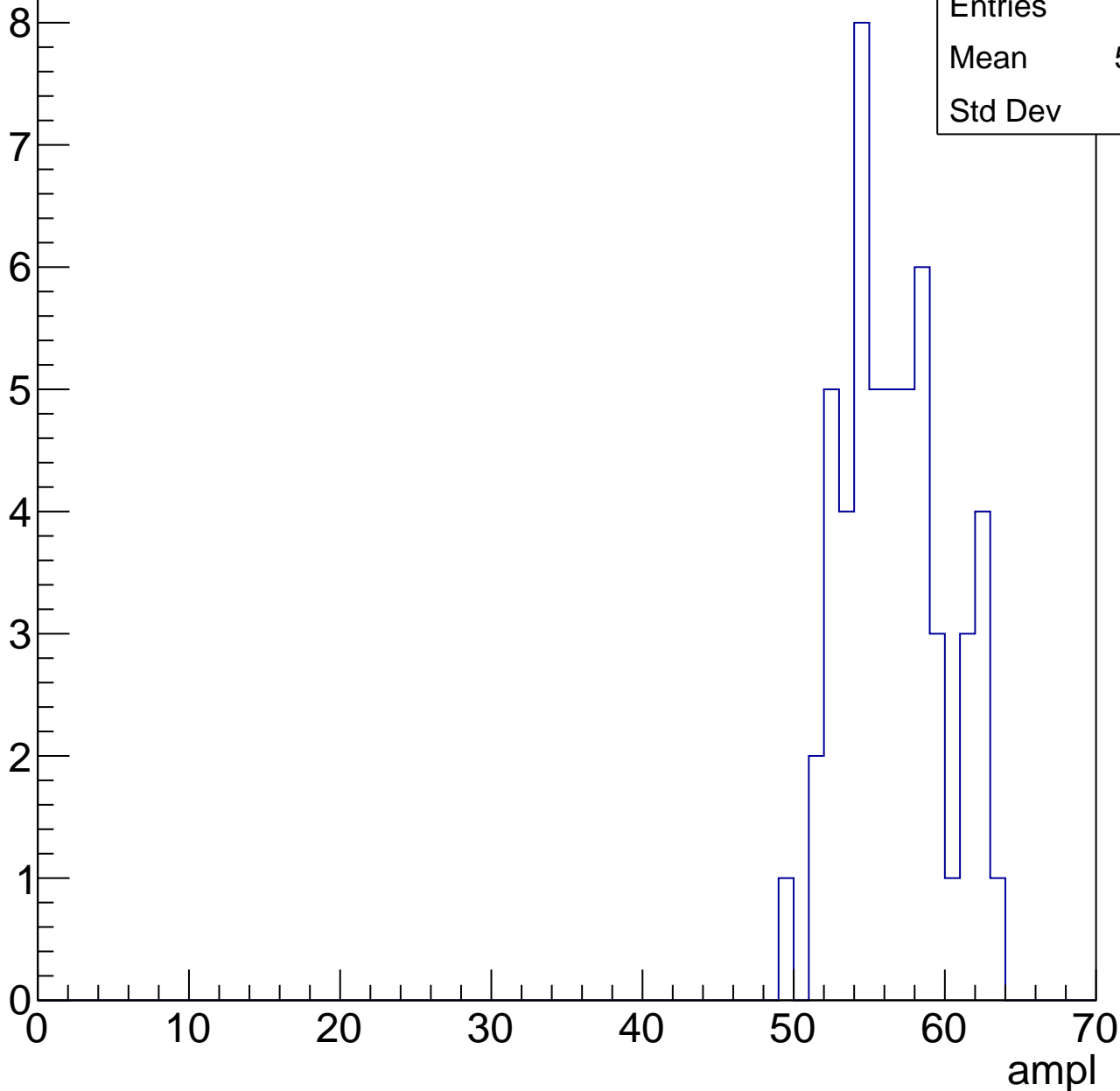


# B0L001S, U21-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	56.11
Std Dev	3.34

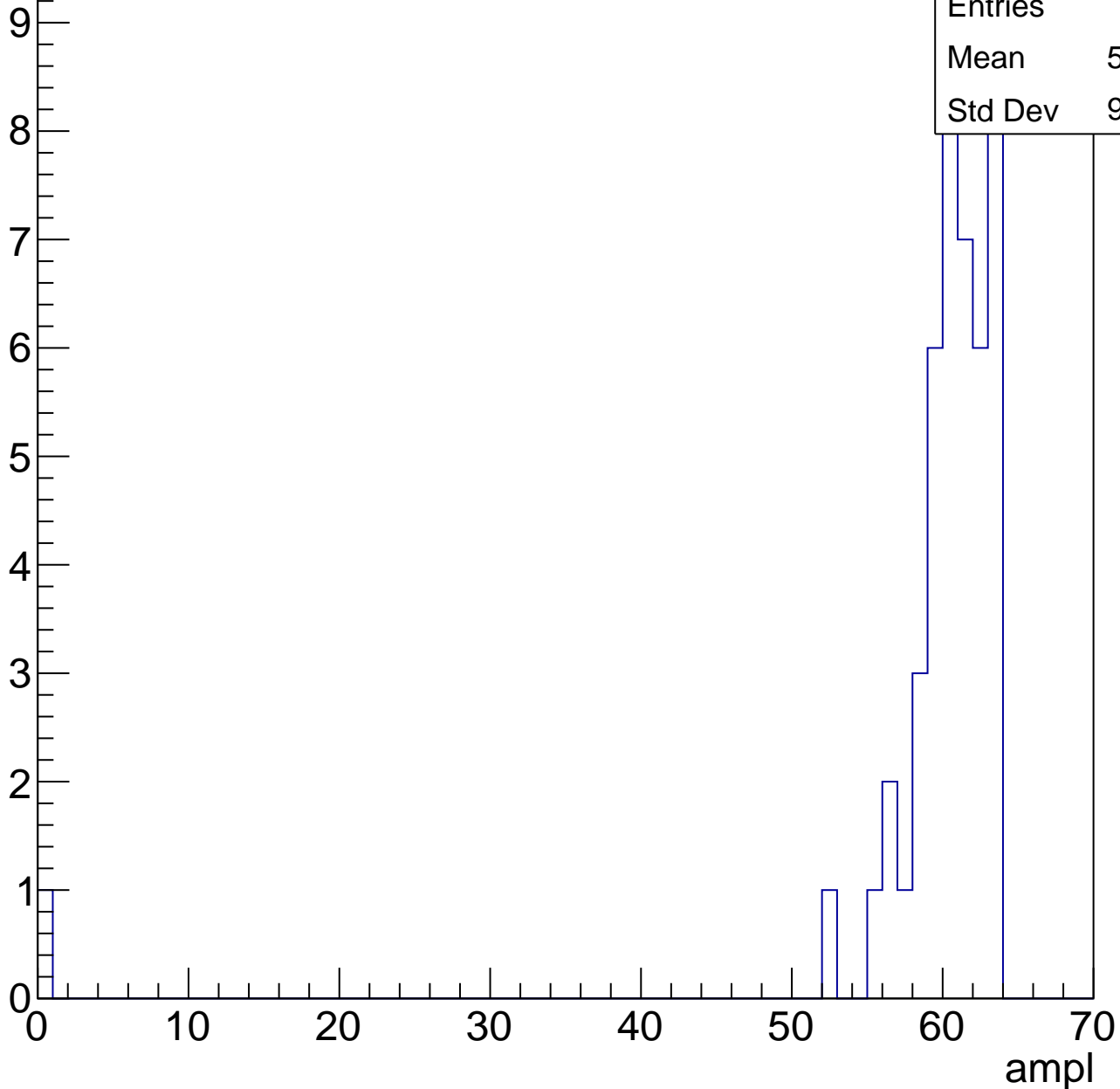


# B0L001S, U21-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	45
Mean	58.82
Std Dev	9.176



# B0L001S, U21-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch109, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	59
Mean	31.24
Std Dev	2.959

**Gaus mean : 32.4119**

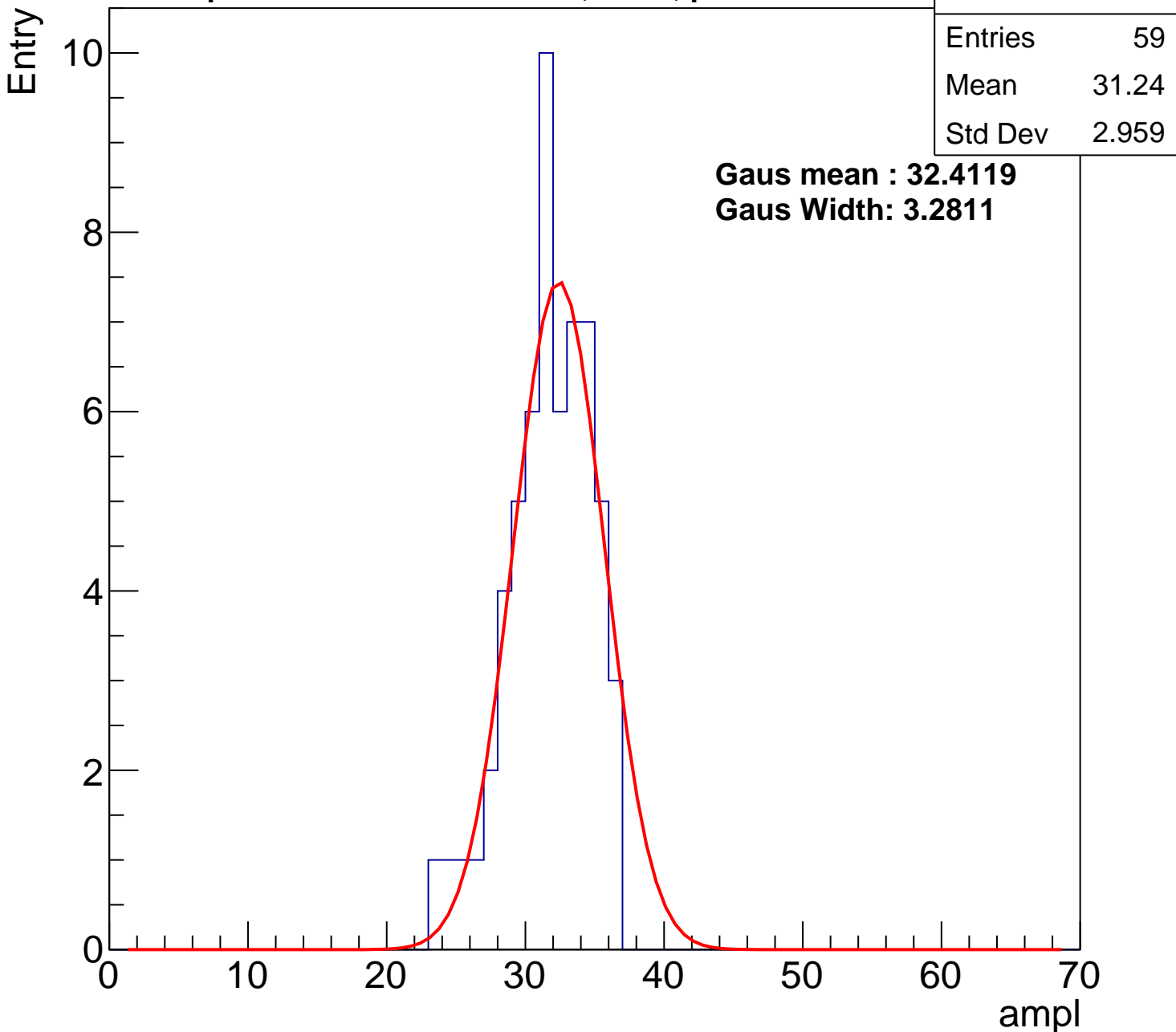
**Gaus Width: 3.2811**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U21-ch109, adc1

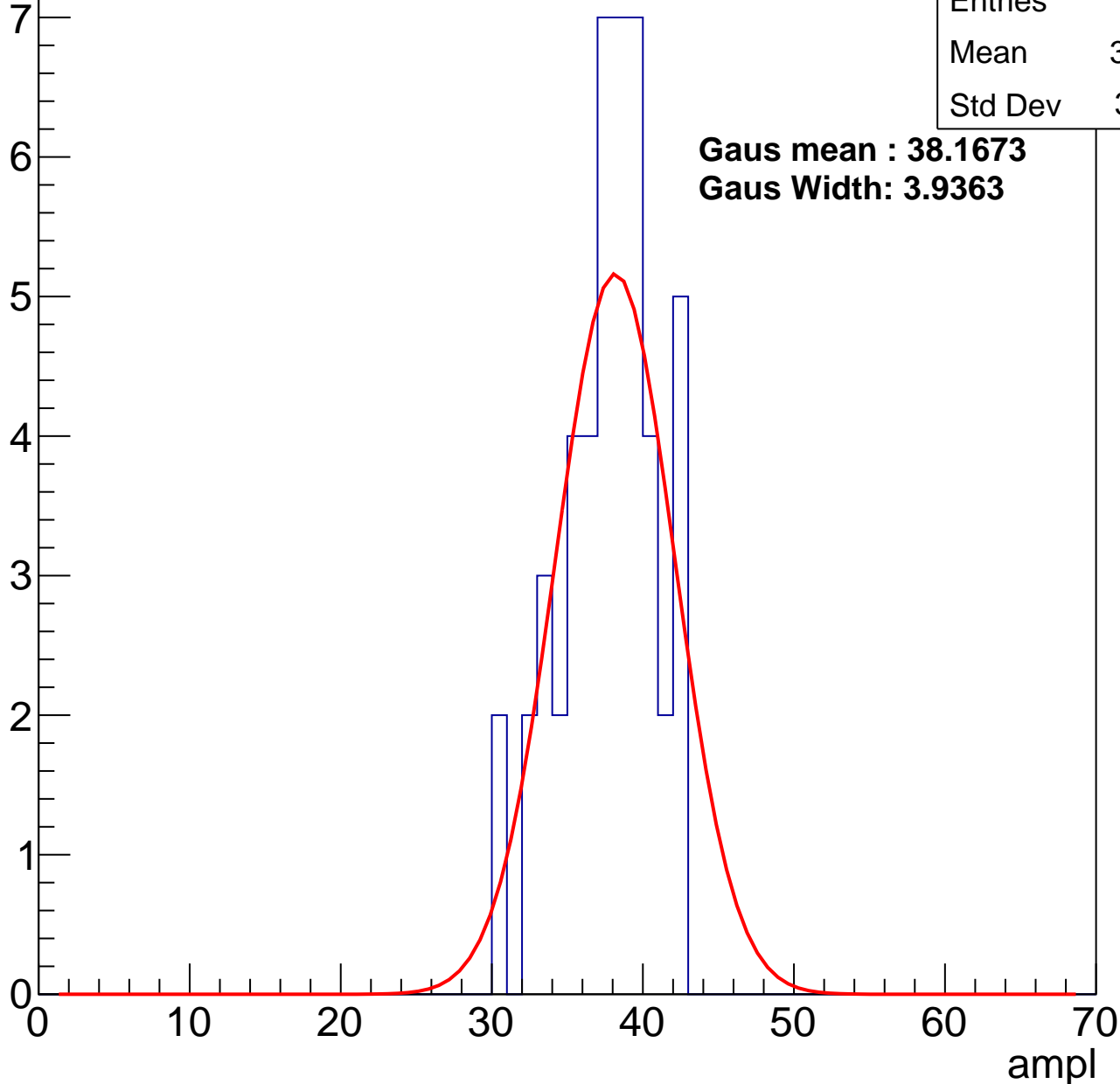
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	37.24
Std Dev	3.061

**Gaus mean : 38.1673**

**Gaus Width: 3.9363**



# B0L001S, U21-ch109, adc2

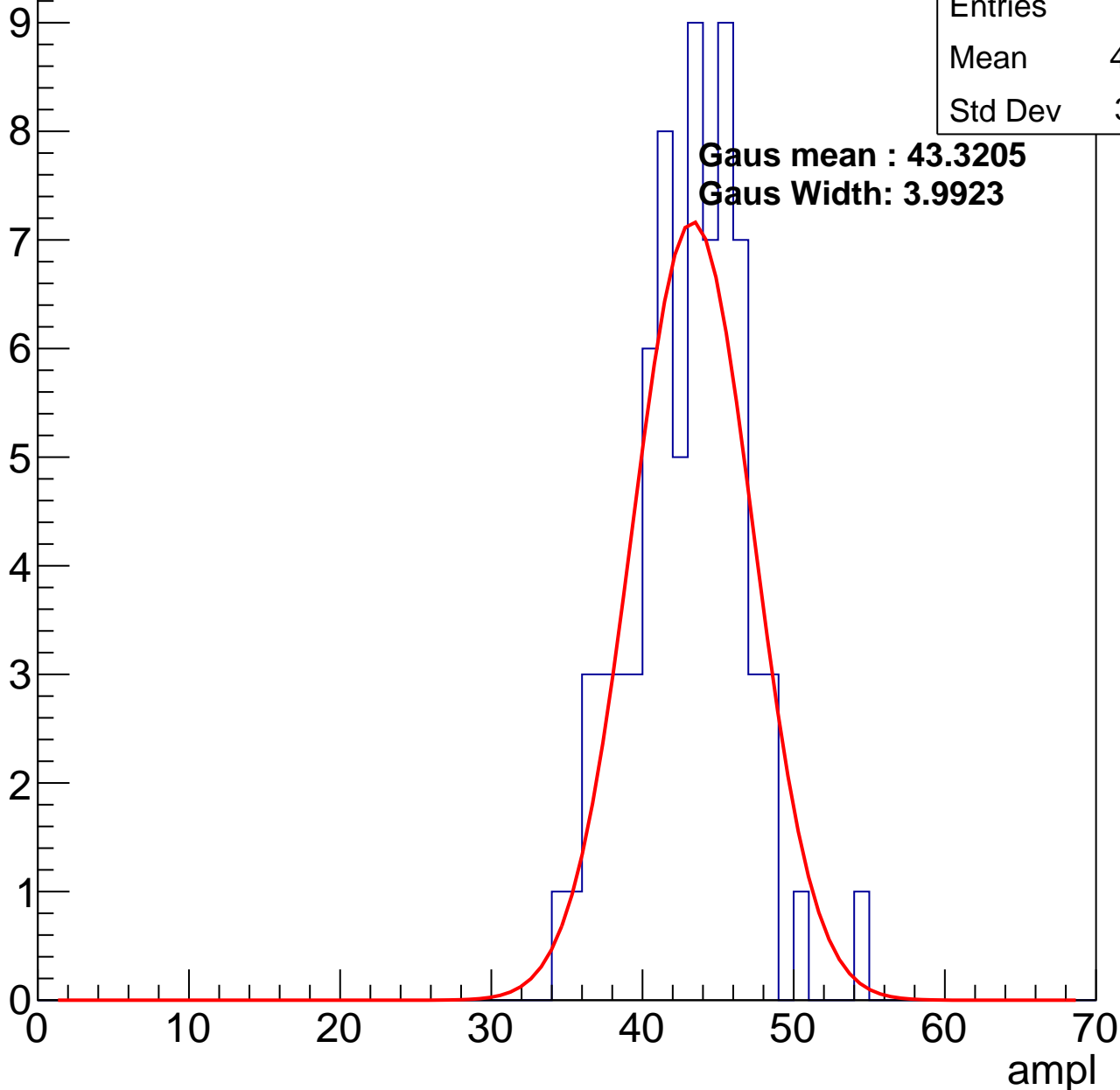
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	42.58
Std Dev	3.701

**Gaus mean : 43.3205**

**Gaus Width: 3.9923**

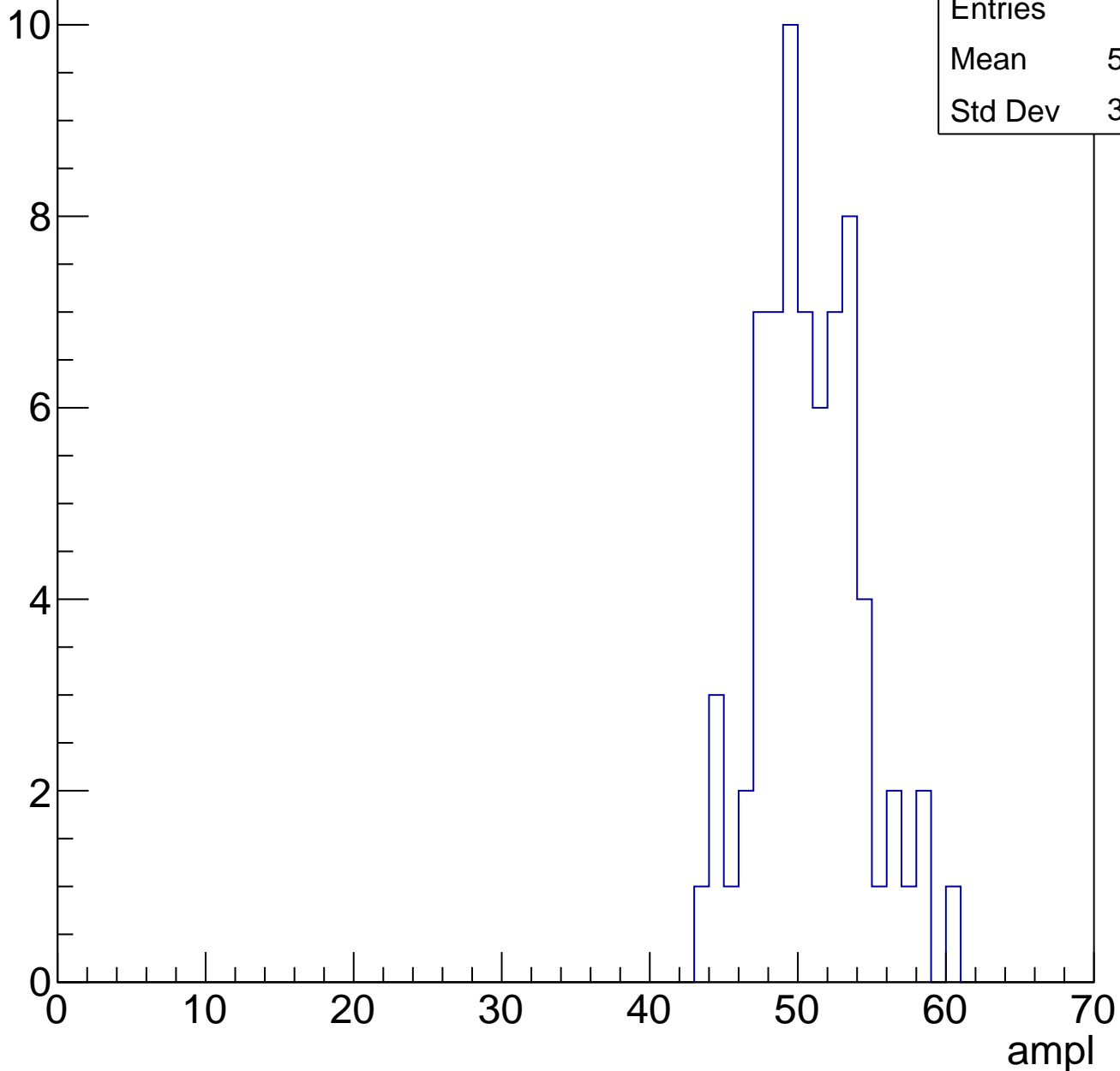


# B0L001S, U21-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	70
Mean	50.39
Std Dev	3.482

Entry

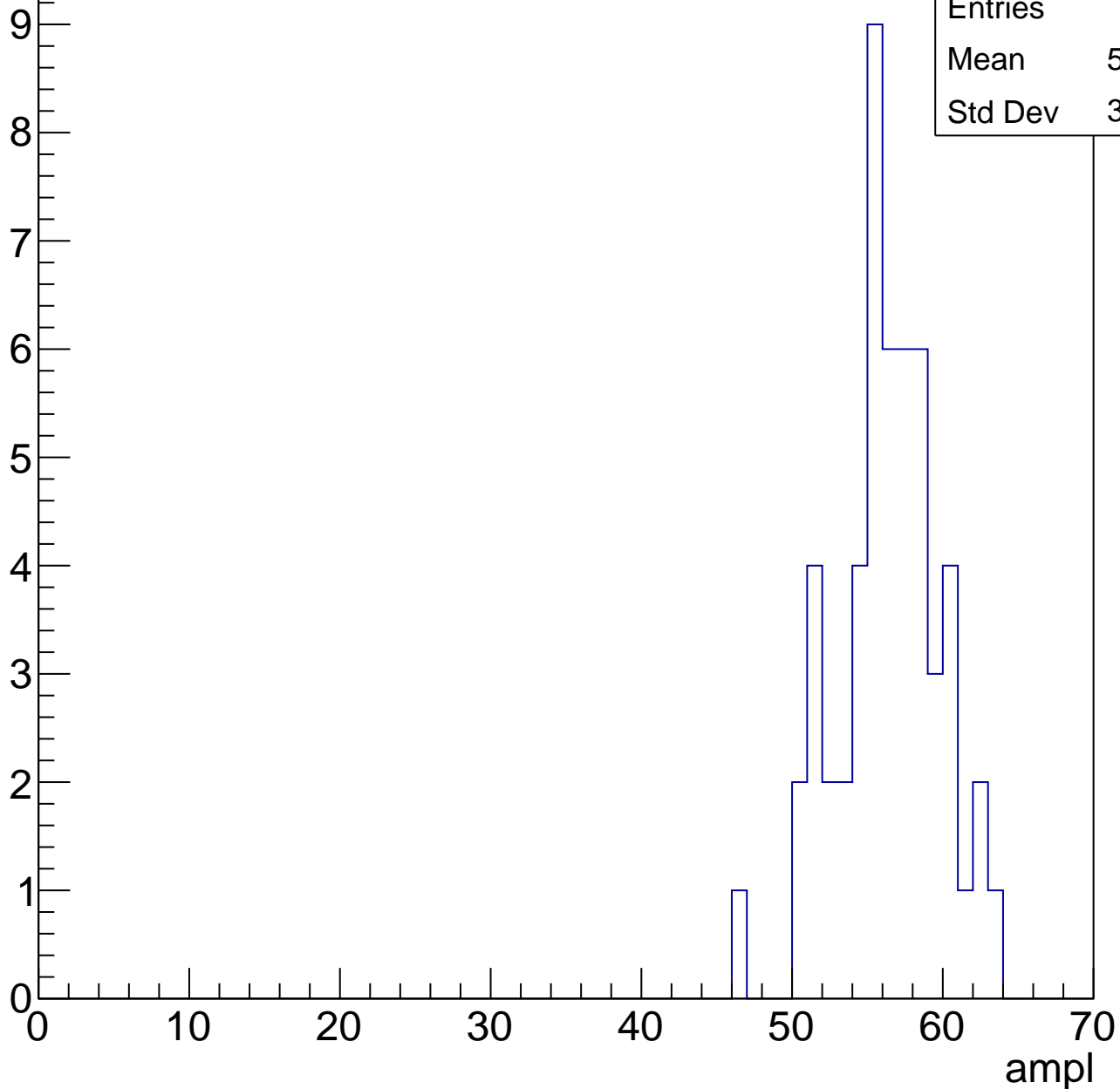


# B0L001S, U21-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	55.89
Std Dev	3.402

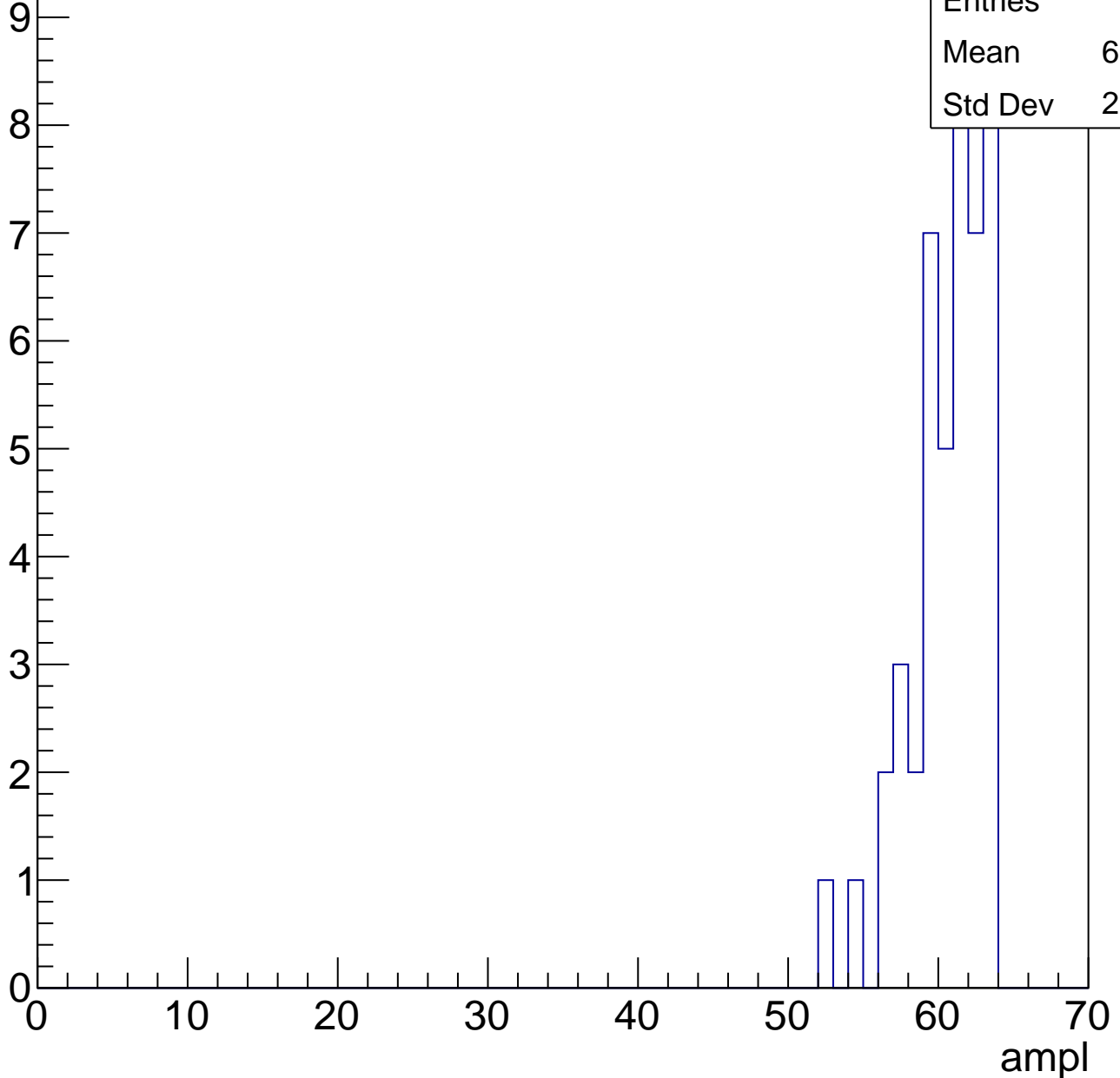


# B0L001S, U21-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	45
Mean	60.16
Std Dev	2.538



# B0L001S, U21-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

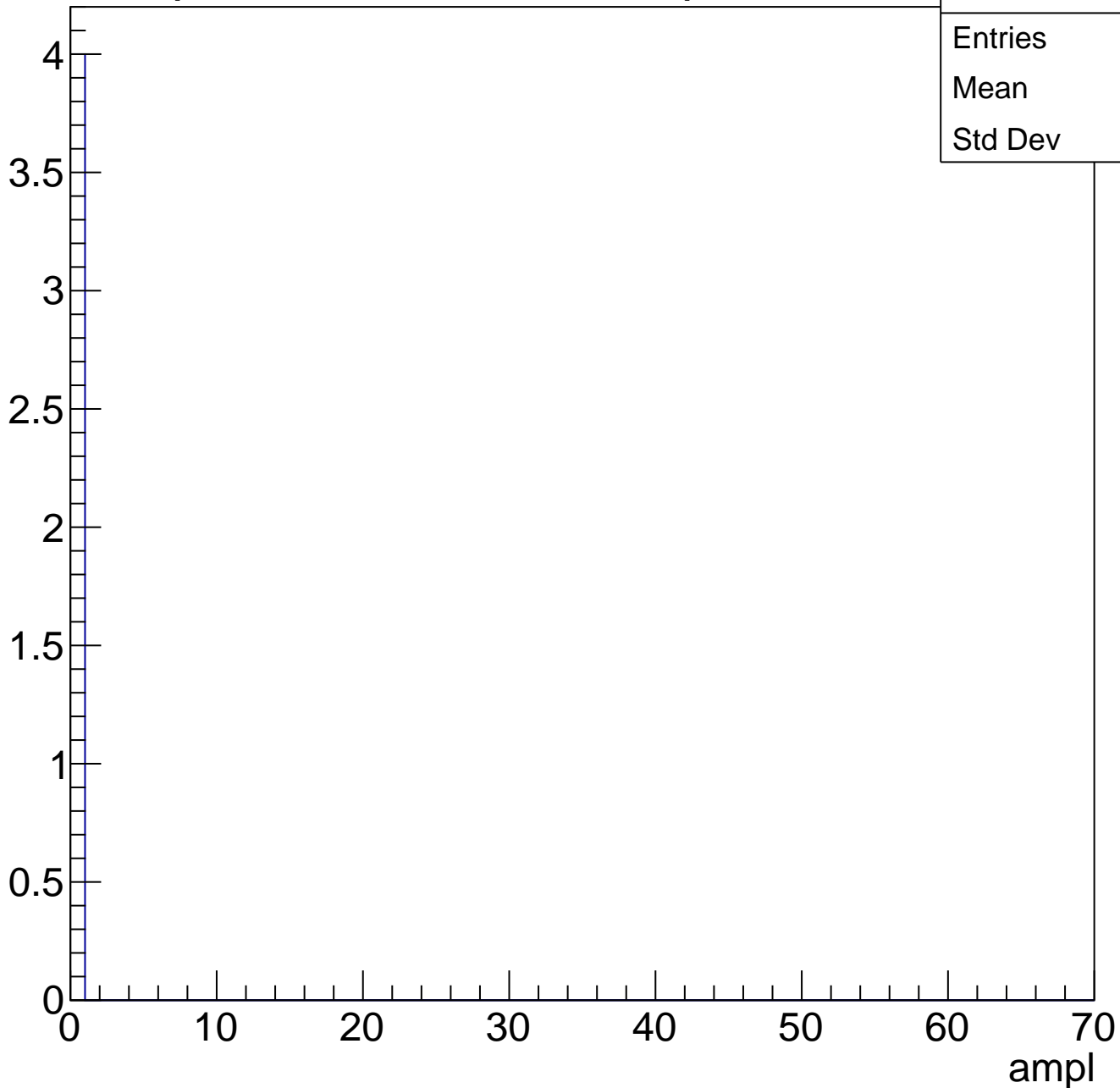




# B0L001S, U21-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	4
Mean	0
Std Dev	0

# B0L001S, U21-ch110, adc0

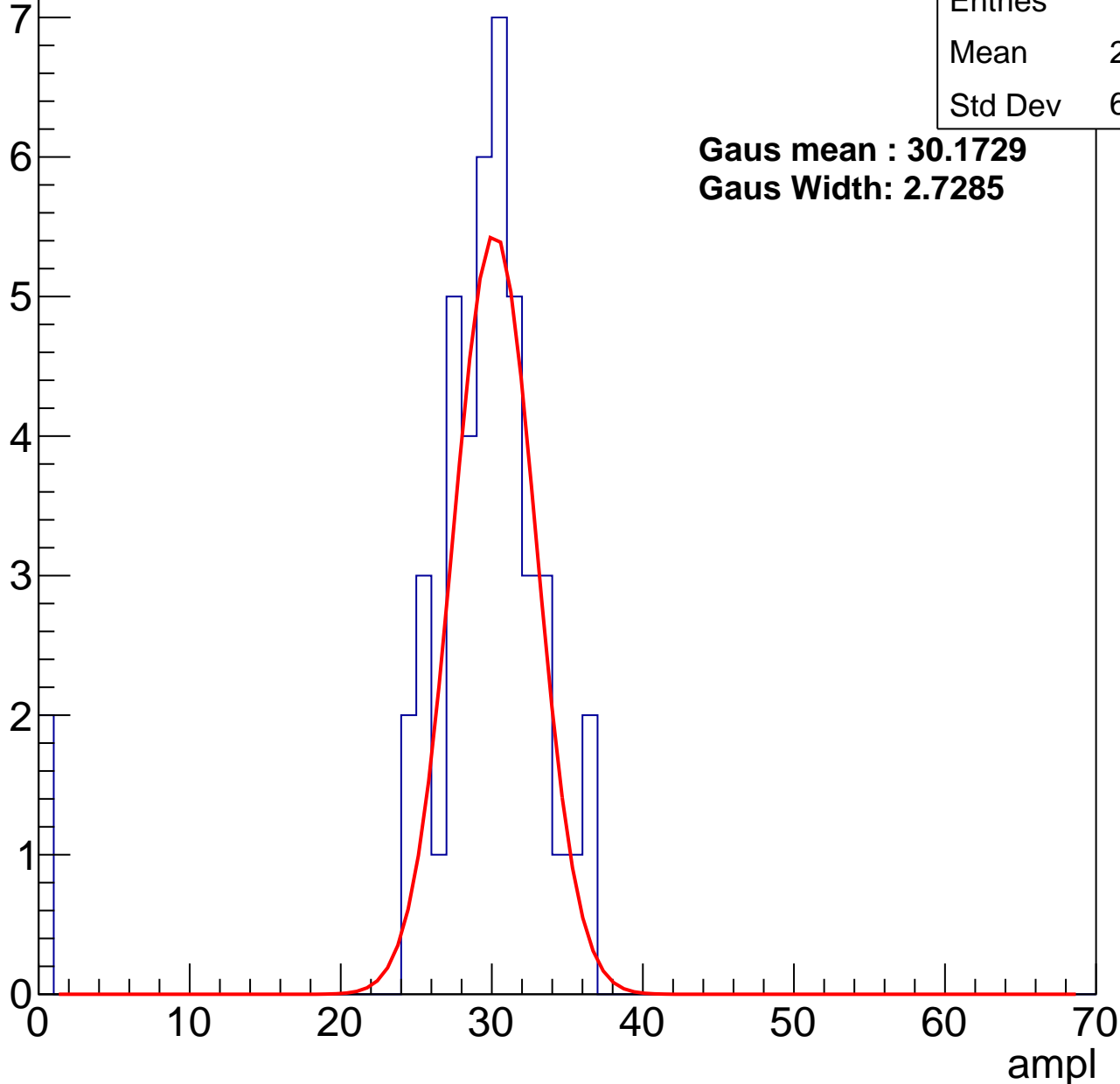
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	45
Mean	28.24
Std Dev	6.747

**Gaus mean : 30.1729**

**Gaus Width: 2.7285**



# B0L001S, U21-ch110, adc1

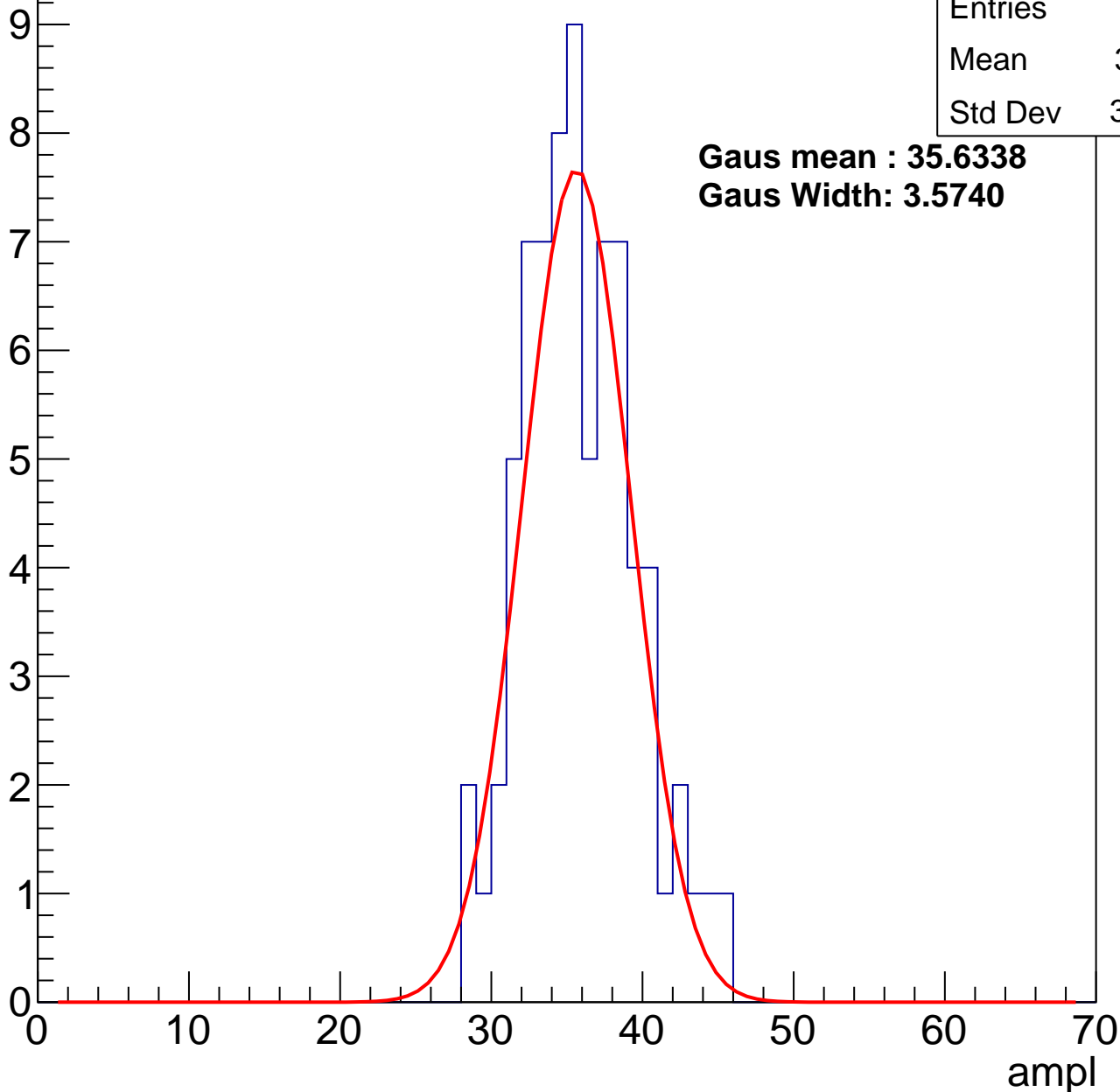
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	35.41
Std Dev	3.657

**Gaus mean : 35.6338**

**Gaus Width: 3.5740**



# B0L001S, U21-ch110, adc2

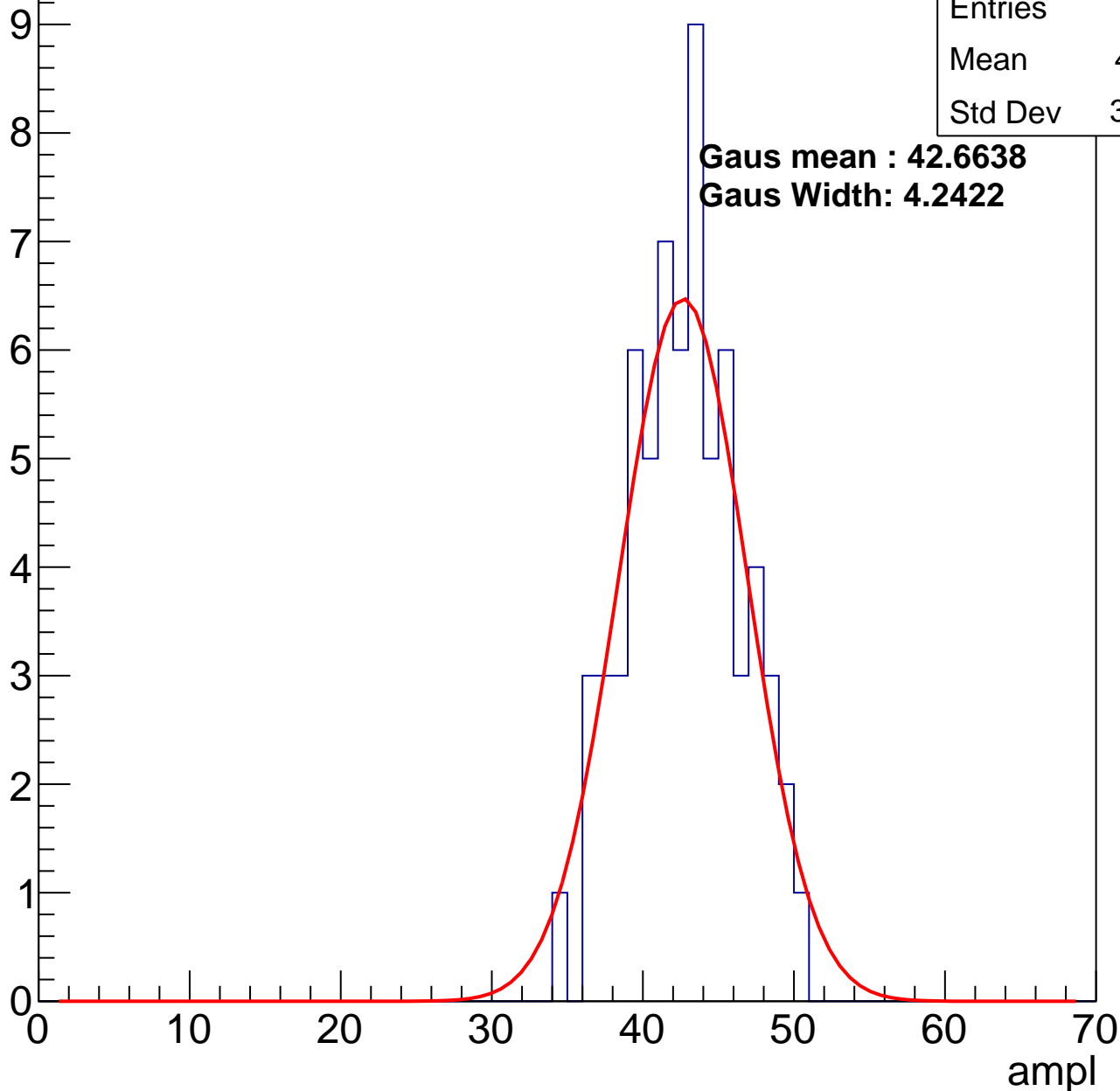
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	42.31
Std Dev	3.604

**Gaus mean : 42.6638**

**Gaus Width: 4.2422**

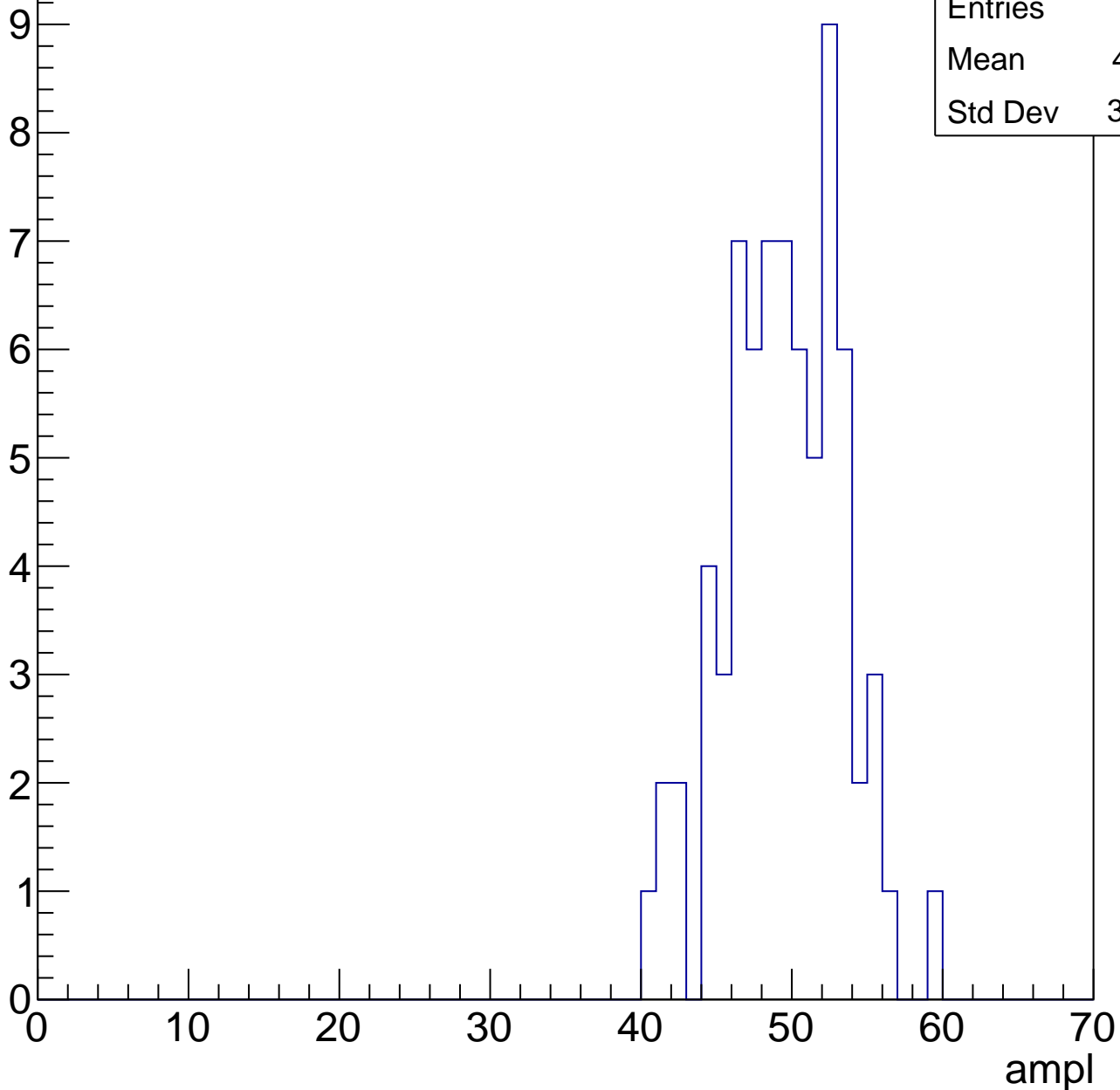


# B0L001S, U21-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	72
Mean	49.01
Std Dev	3.835

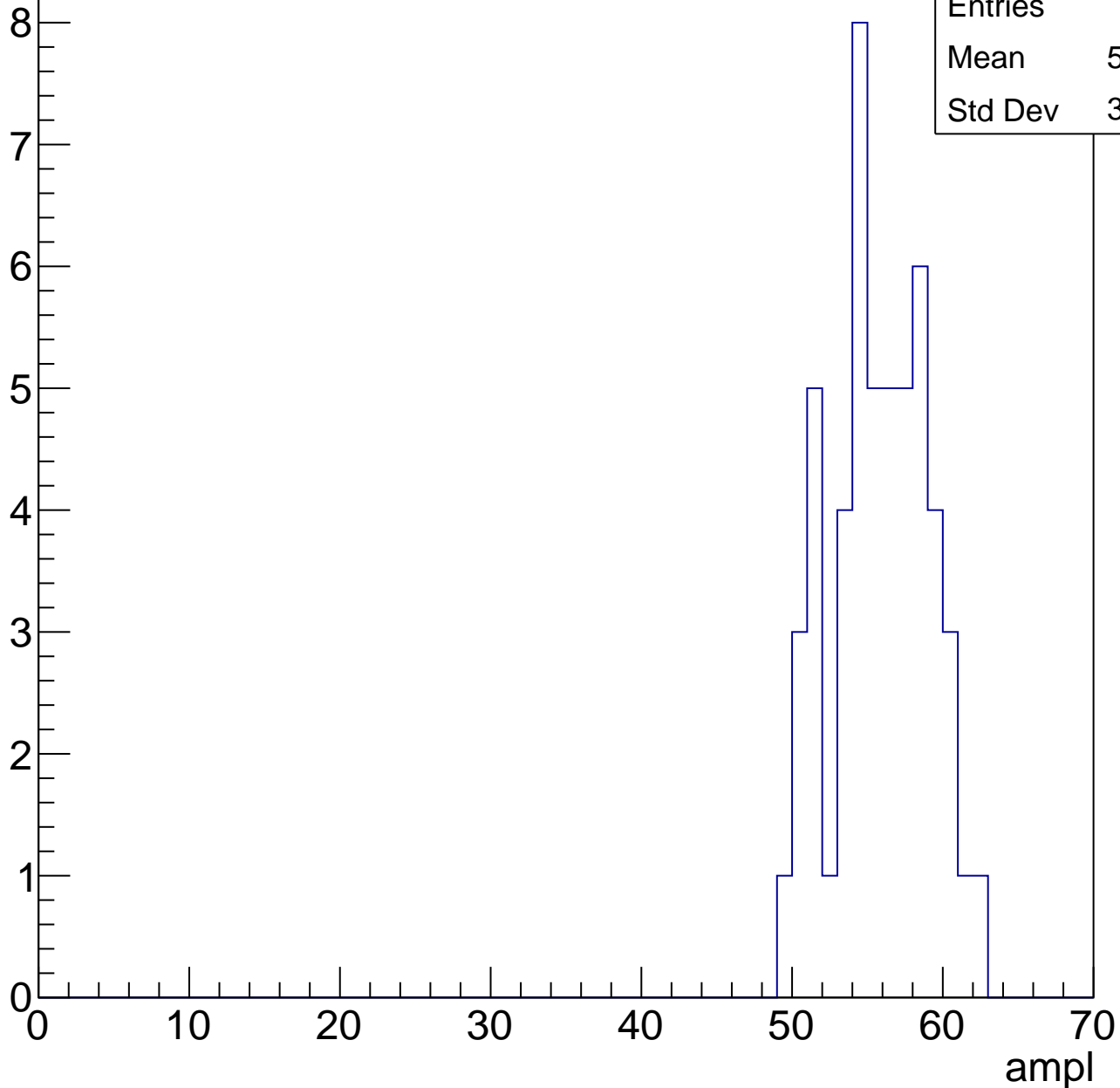


# B0L001S, U21-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	52
Mean	55.33
Std Dev	3.167

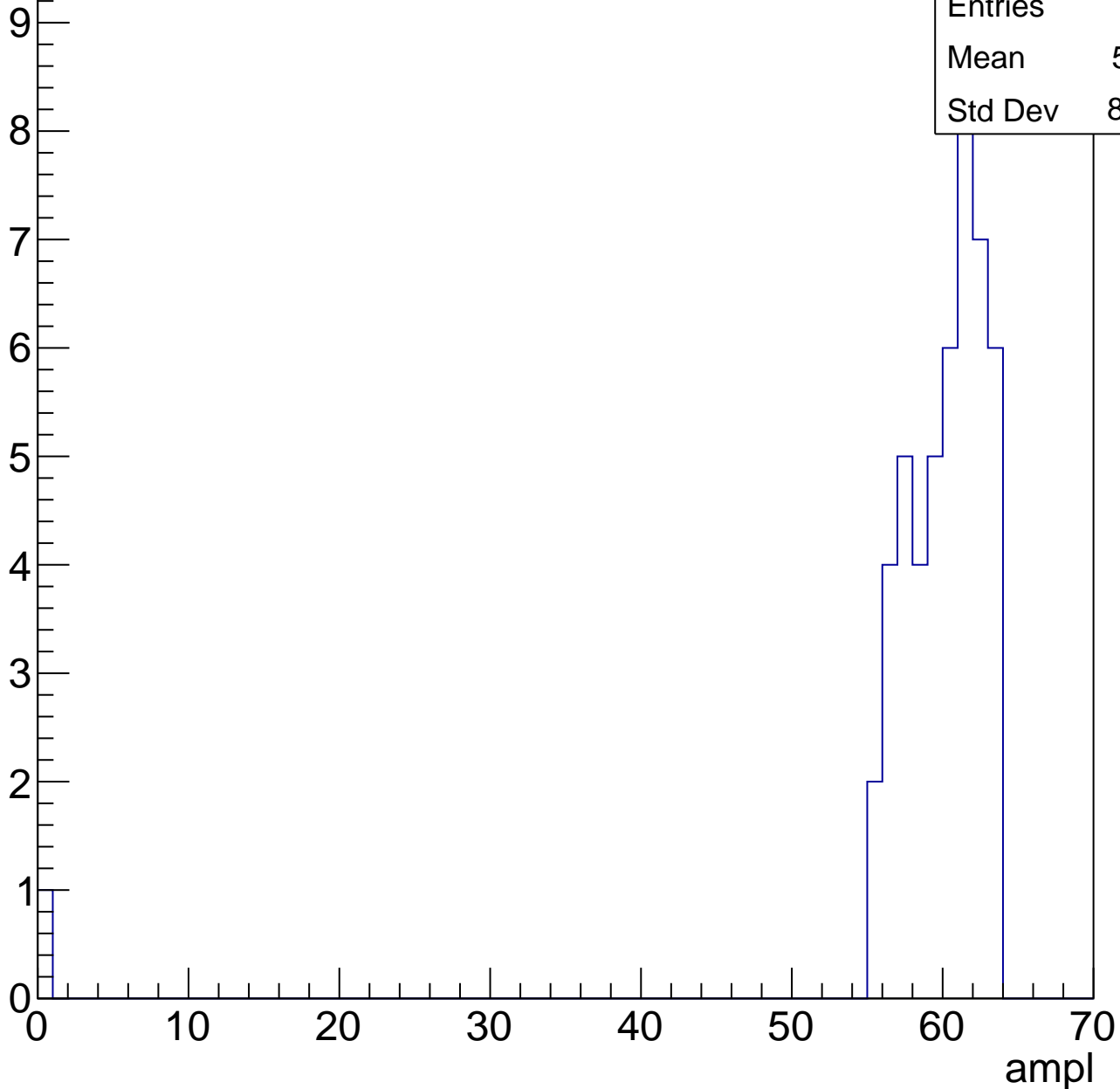


# B0L001S, U21-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	49
Mean	58.51
Std Dev	8.762



# B0L001S, U21-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U21-ch111, adc0

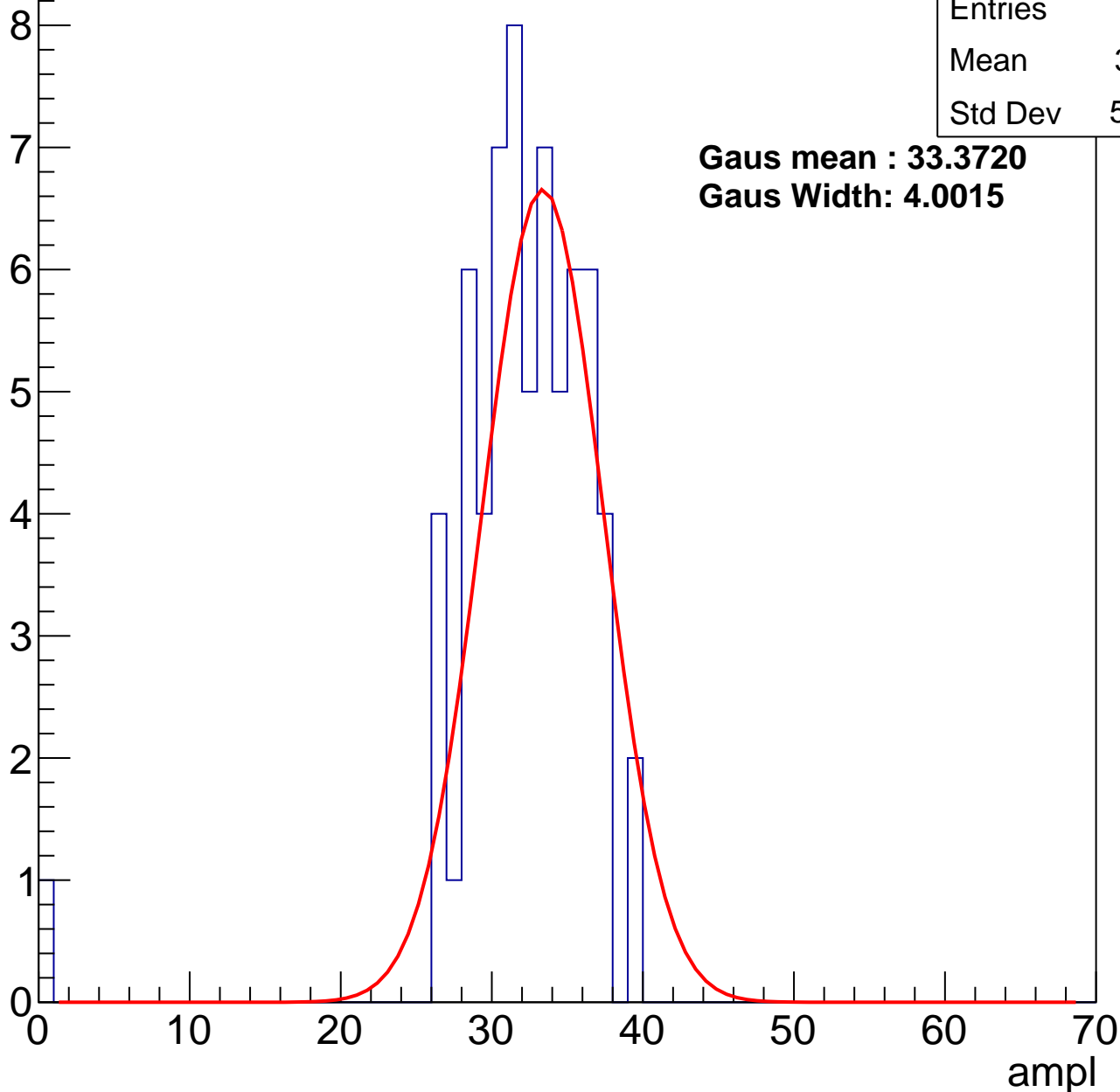
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	31.61
Std Dev	5.113

**Gaus mean : 33.3720**

**Gaus Width: 4.0015**



# B0L001S, U21-ch111, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	68
Mean	38.41
Std Dev	3.735

**Gaus mean : 39.2588**

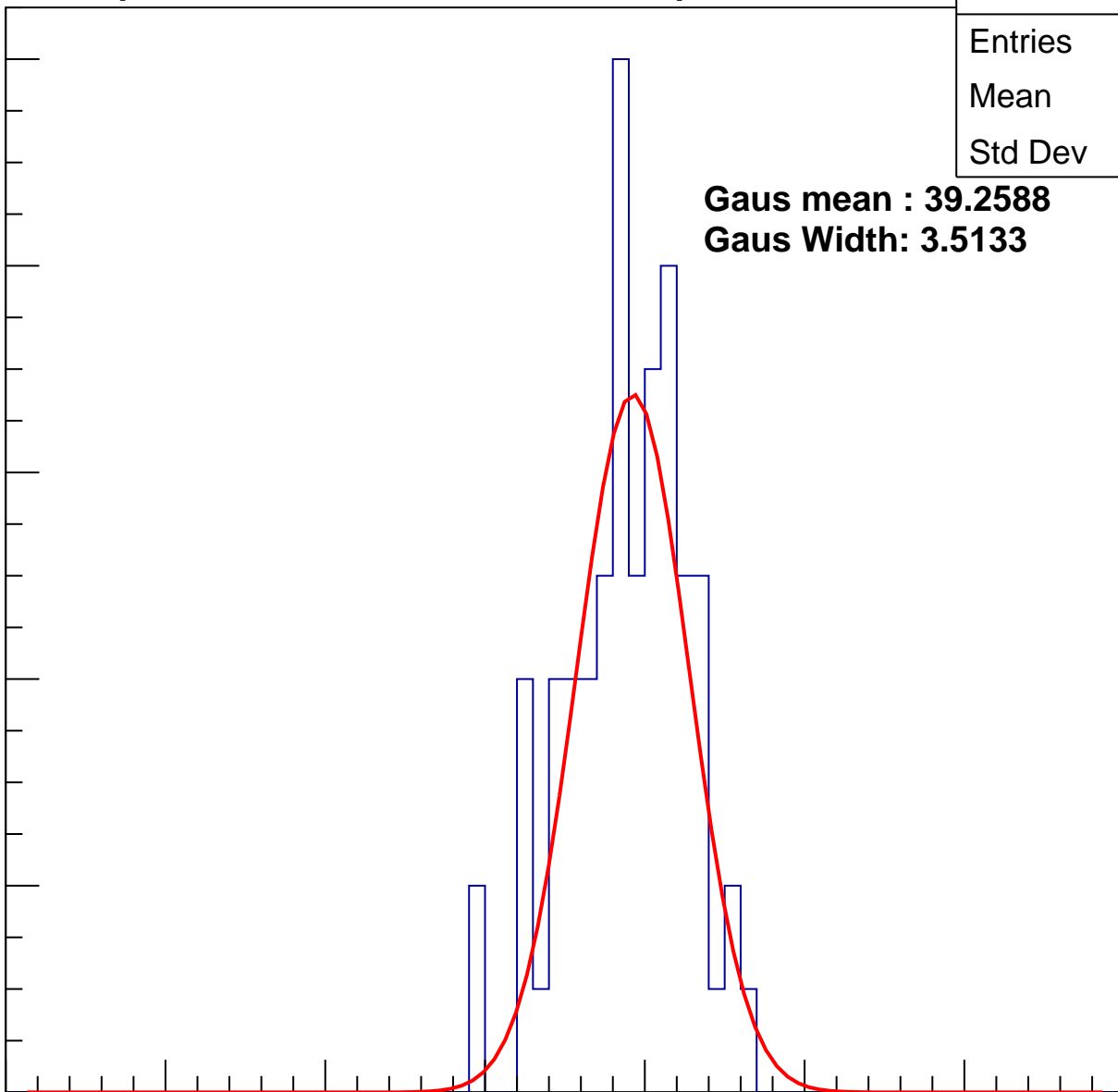
**Gaus Width: 3.5133**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U21-ch111, adc2

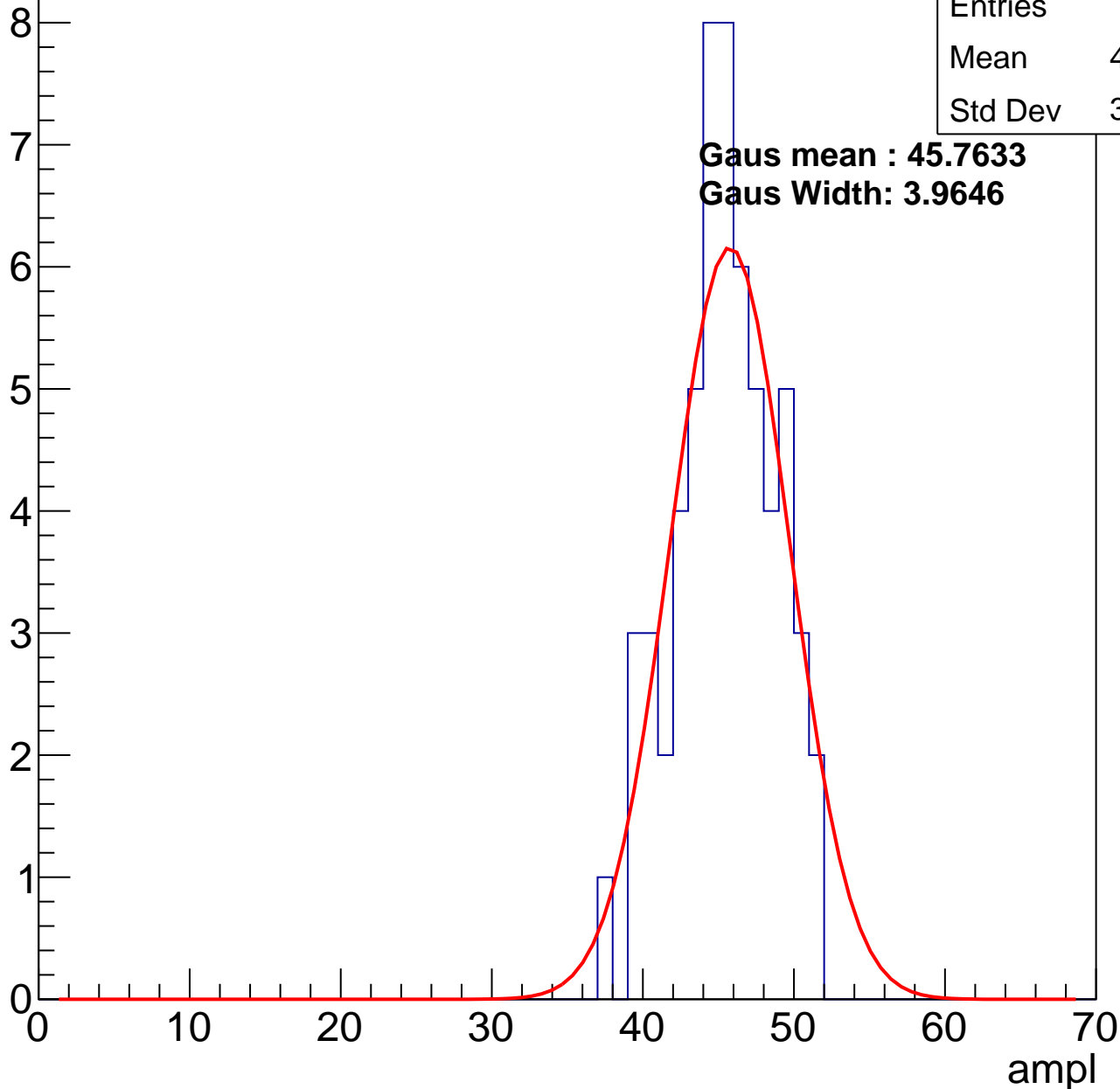
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	44.93
Std Dev	3.272

**Gaus mean : 45.7633**

**Gaus Width: 3.9646**

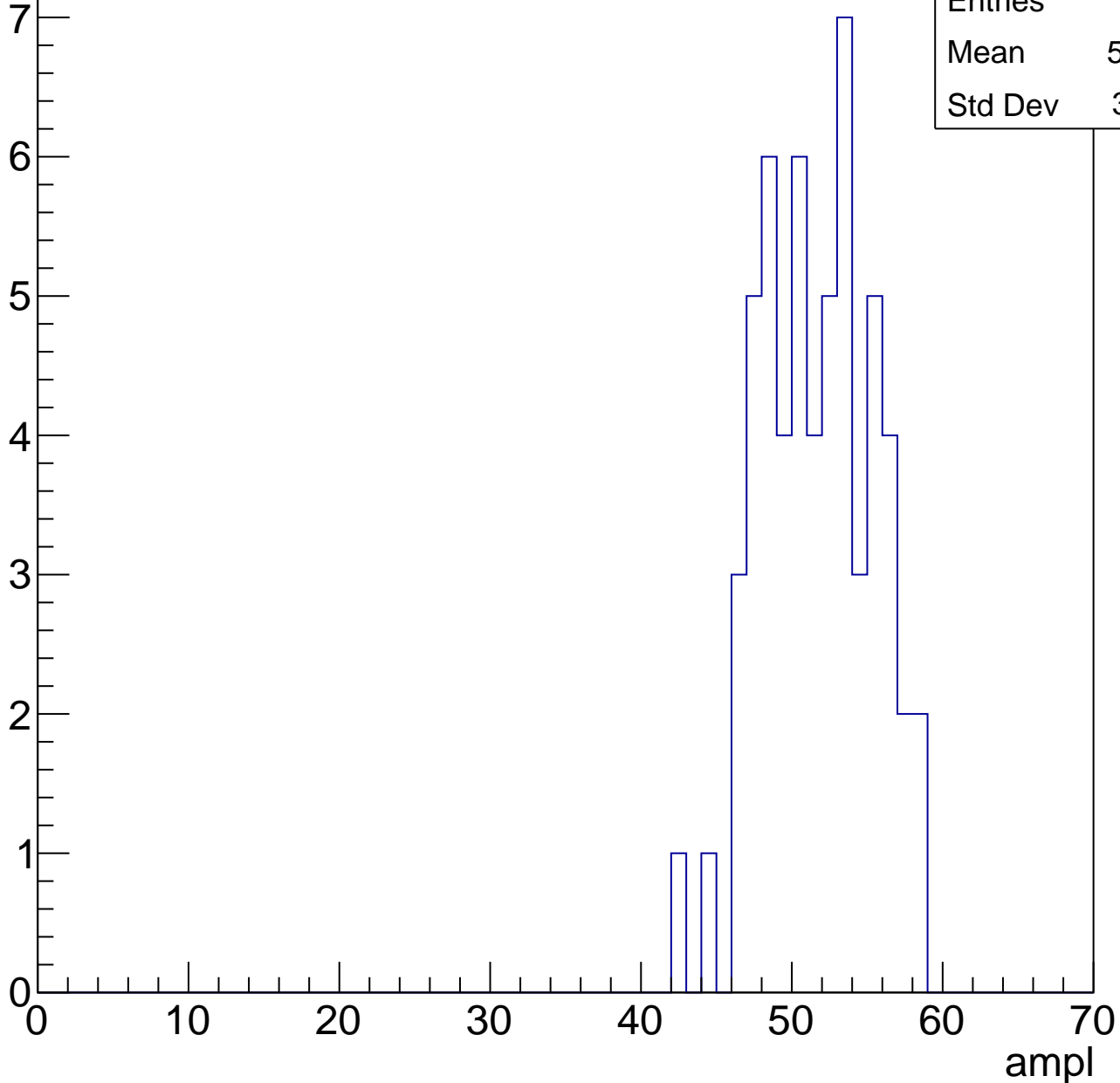


# B0L001S, U21-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	51.19
Std Dev	3.641

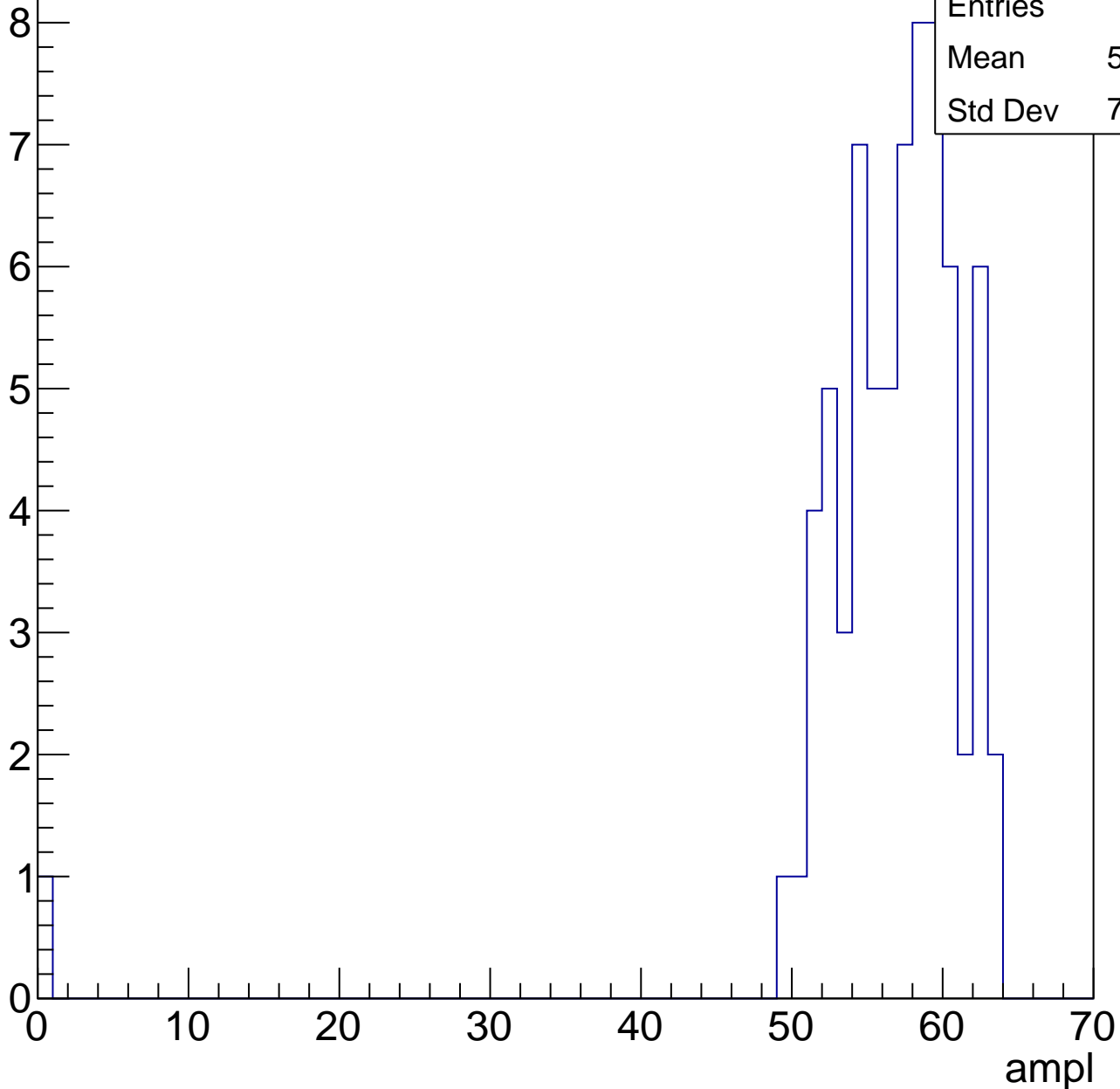


# B0L001S, U21-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	55.92
Std Dev	7.535

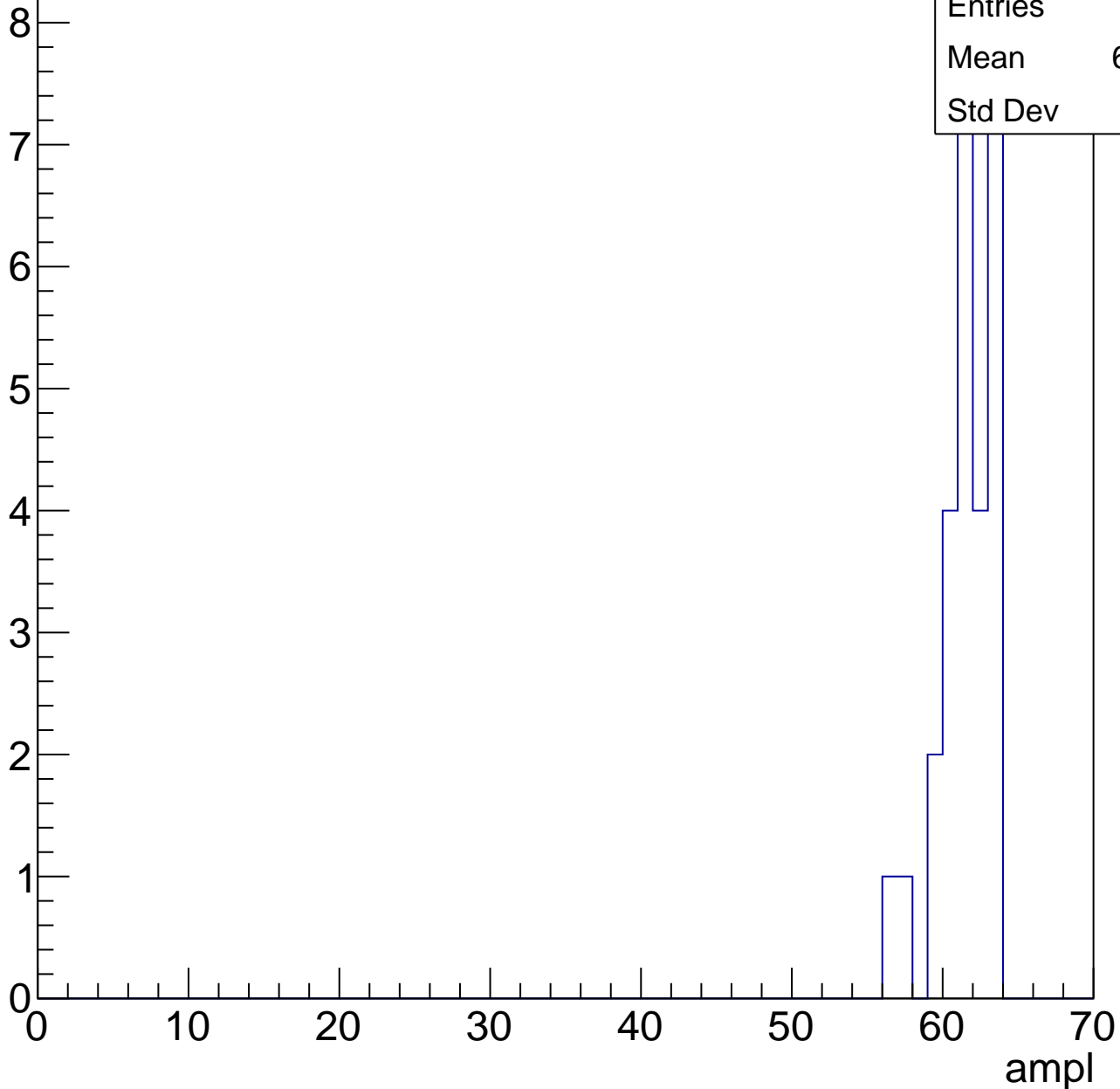


# B0L001S, U21-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	28
Mean	61.11
Std Dev	1.78



# B0L001S, U21-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



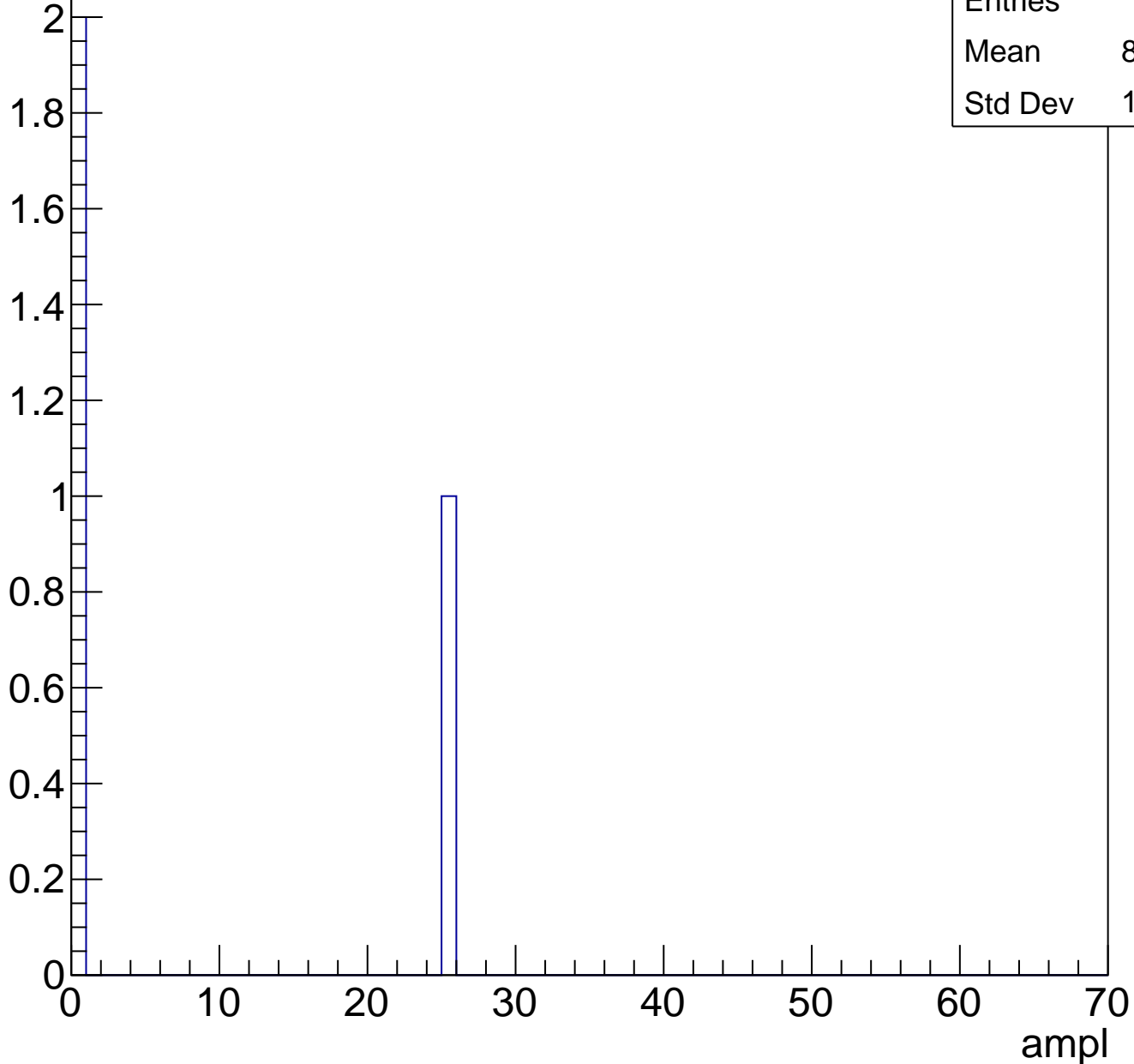
Entries	0
Mean	0
Std Dev	0



# B0L001S, U21-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	8.333
Std Dev	11.79

# B0L001S, U21-ch112, adc0

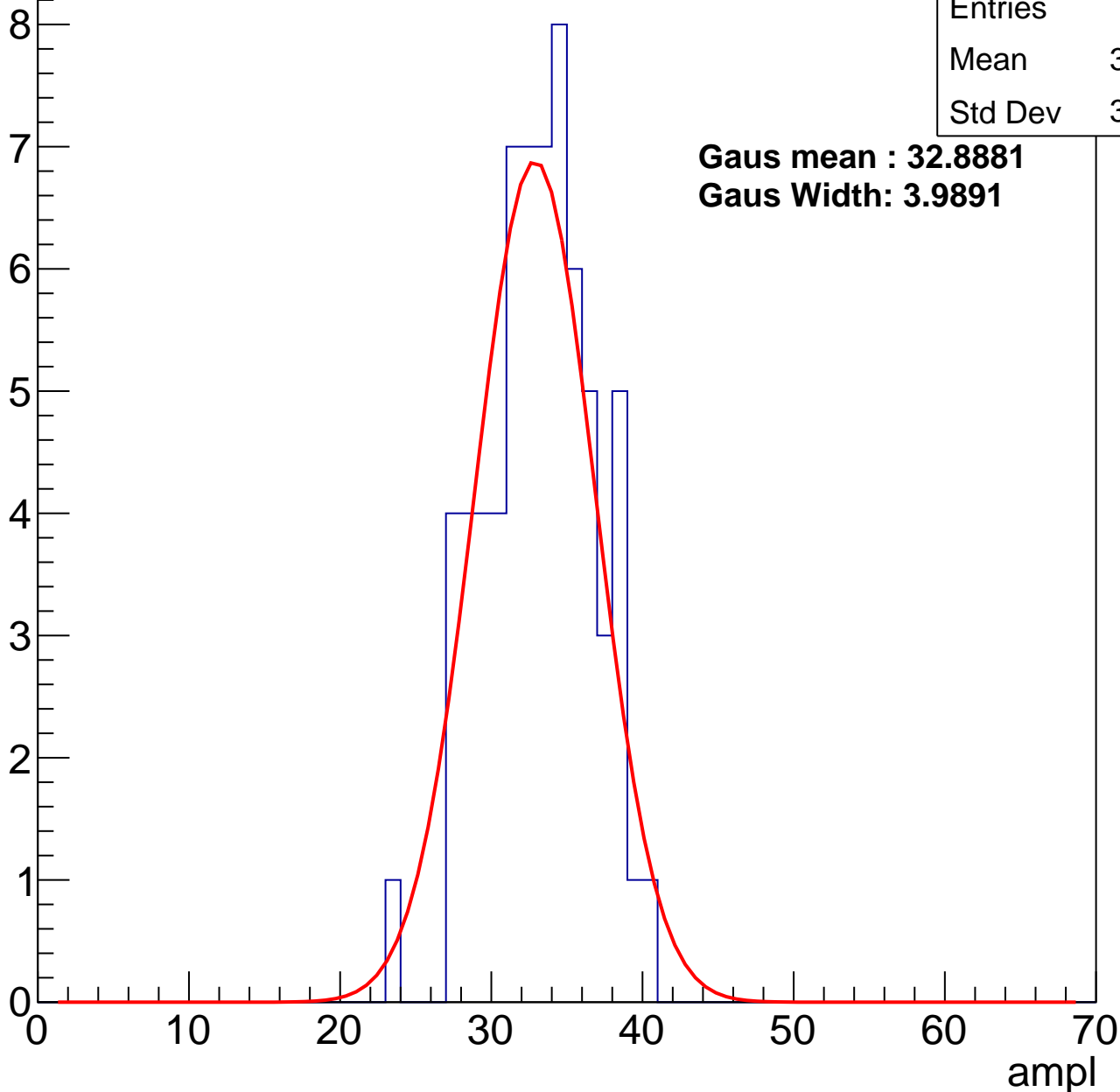
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	32.73
Std Dev	3.475

**Gaus mean : 32.8881**

**Gaus Width: 3.9891**



# B0L001S, U21-ch112, adc1

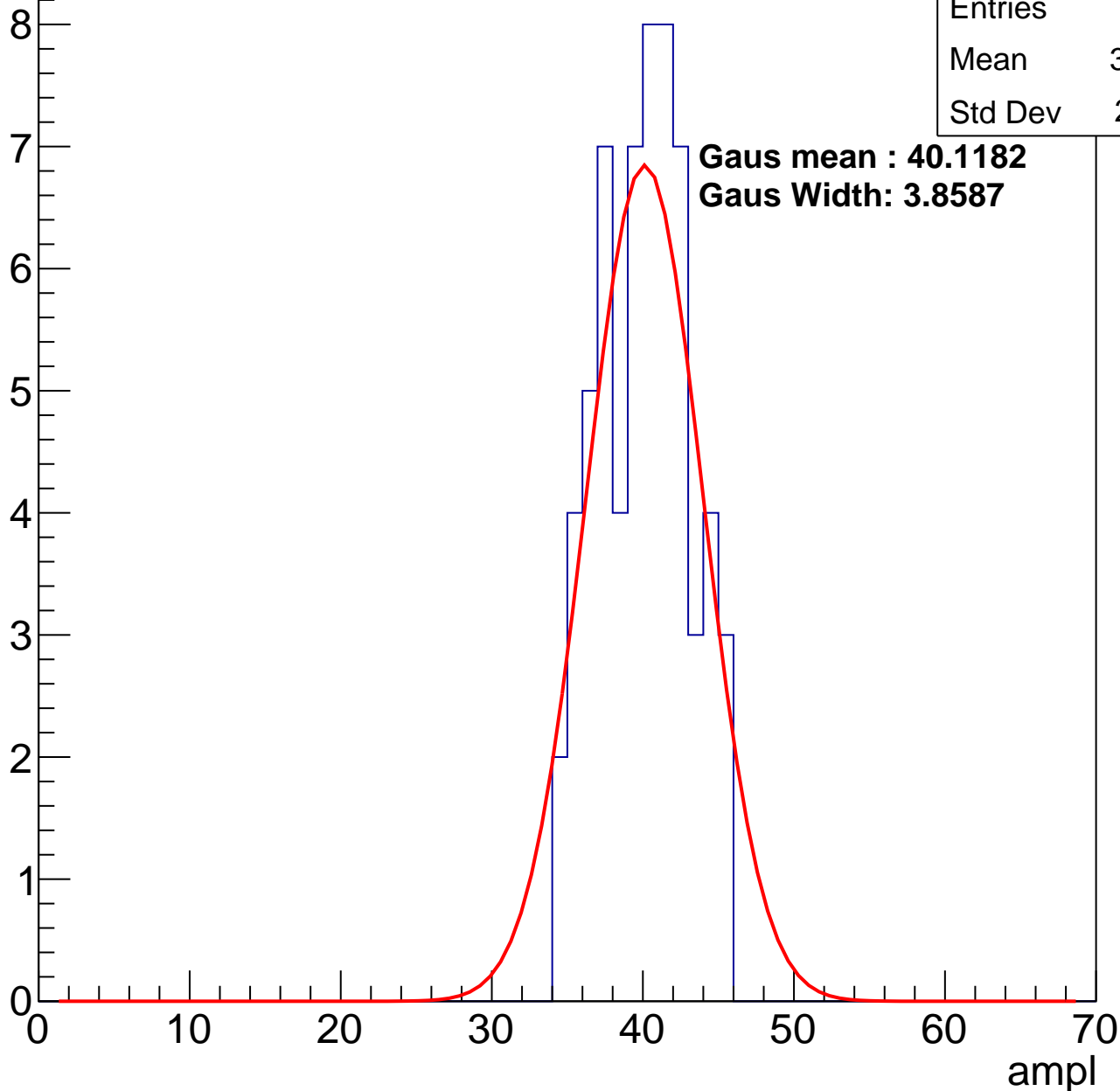
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	39.58
Std Dev	2.921

**Gaus mean : 40.1182**

**Gaus Width: 3.8587**



# B0L001S, U21-ch112, adc2

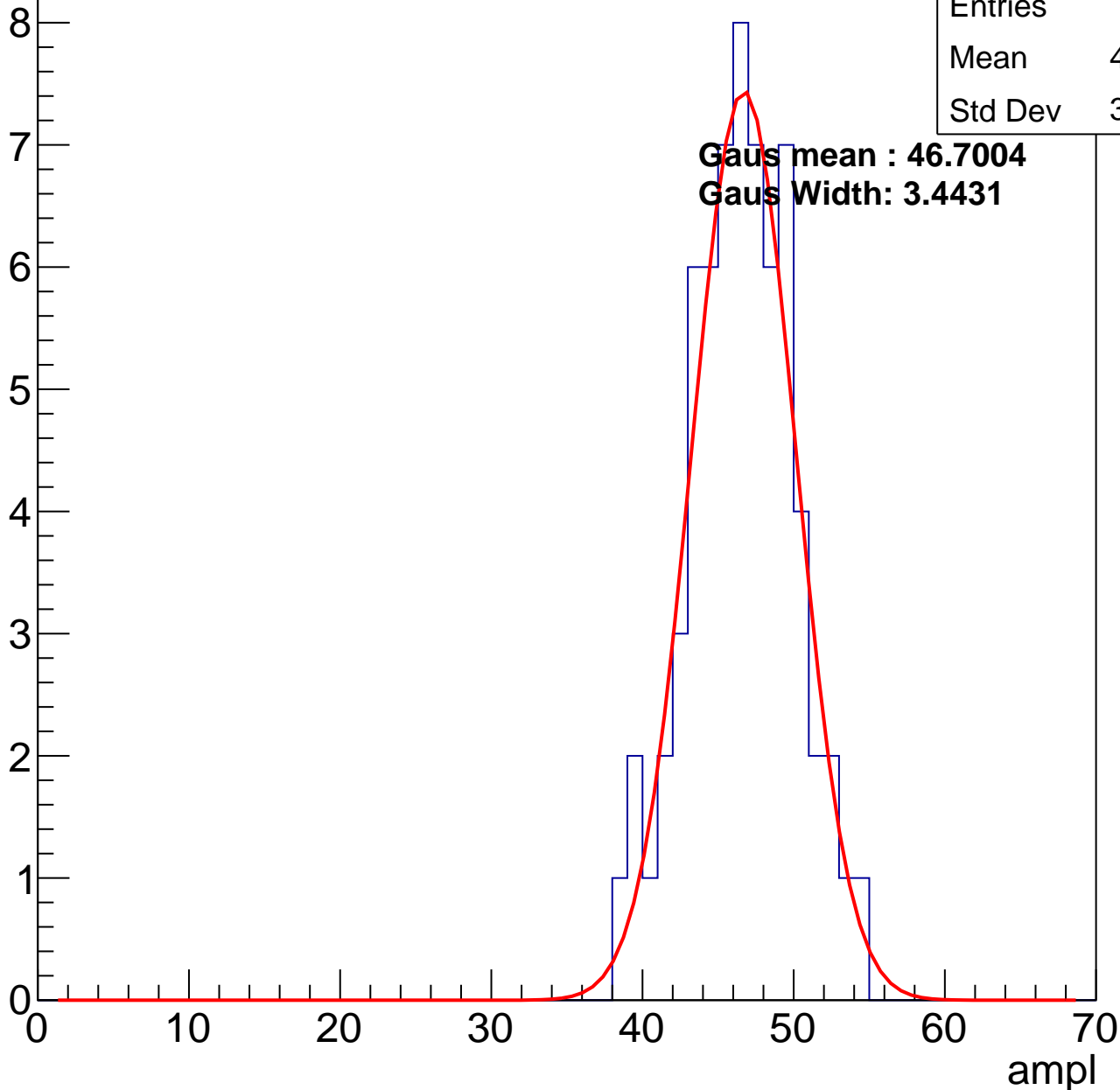
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	46.09
Std Dev	3.423

Gaus mean : 46.7004

Gaus Width: 3.4431

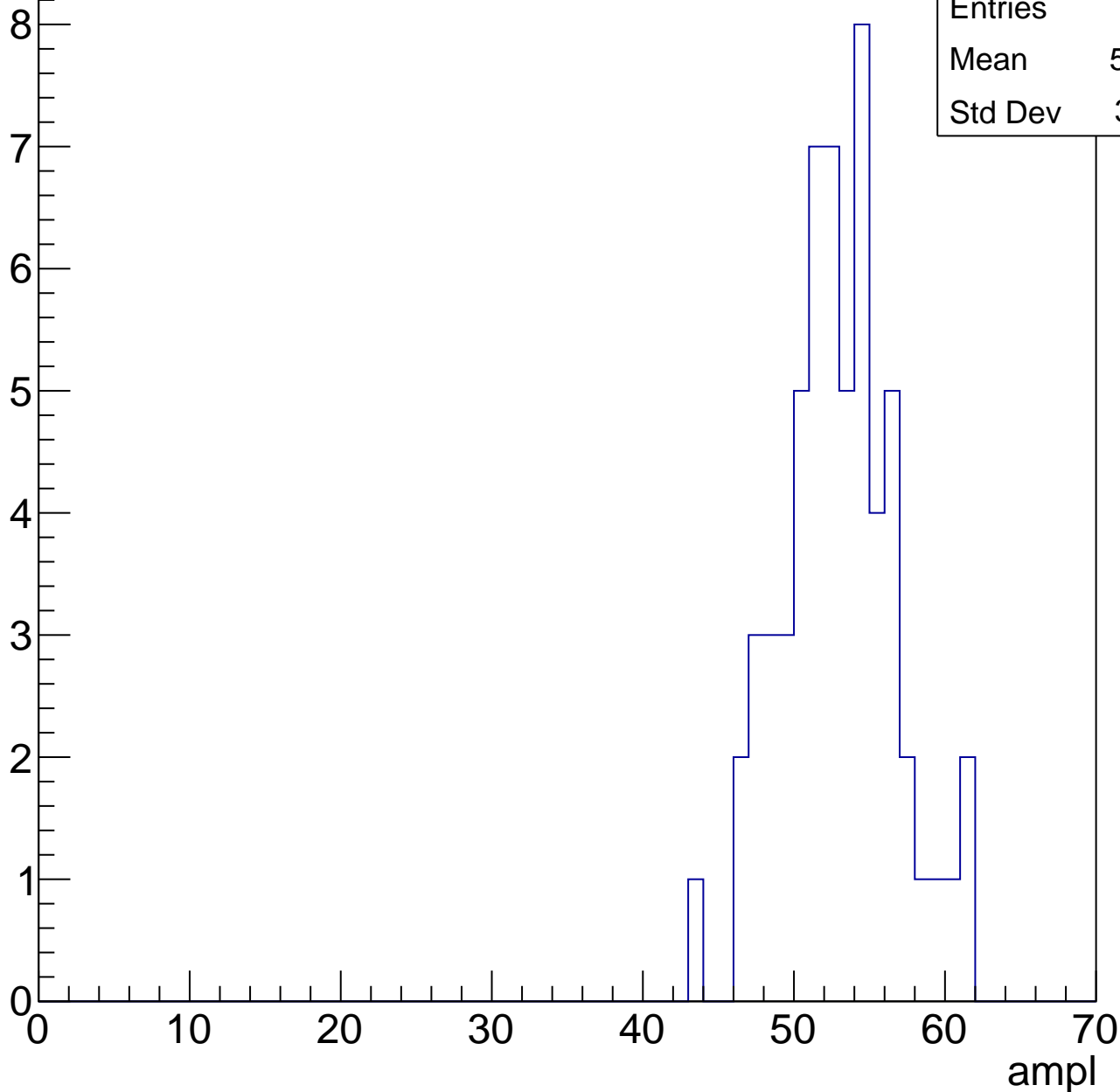


# B0L001S, U21-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	52.47
Std Dev	3.721

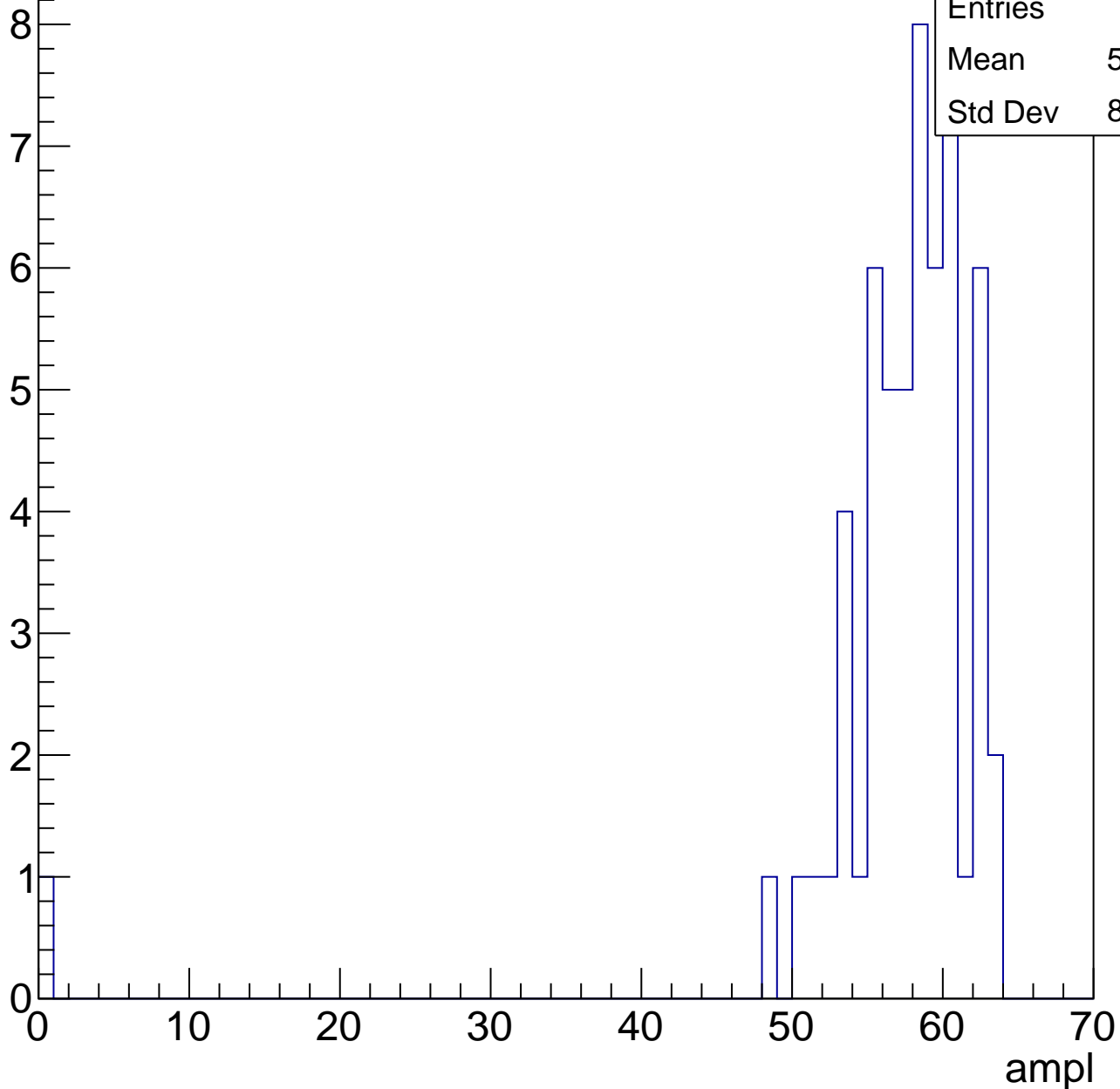


# B0L001S, U21-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	56.47
Std Dev	8.238

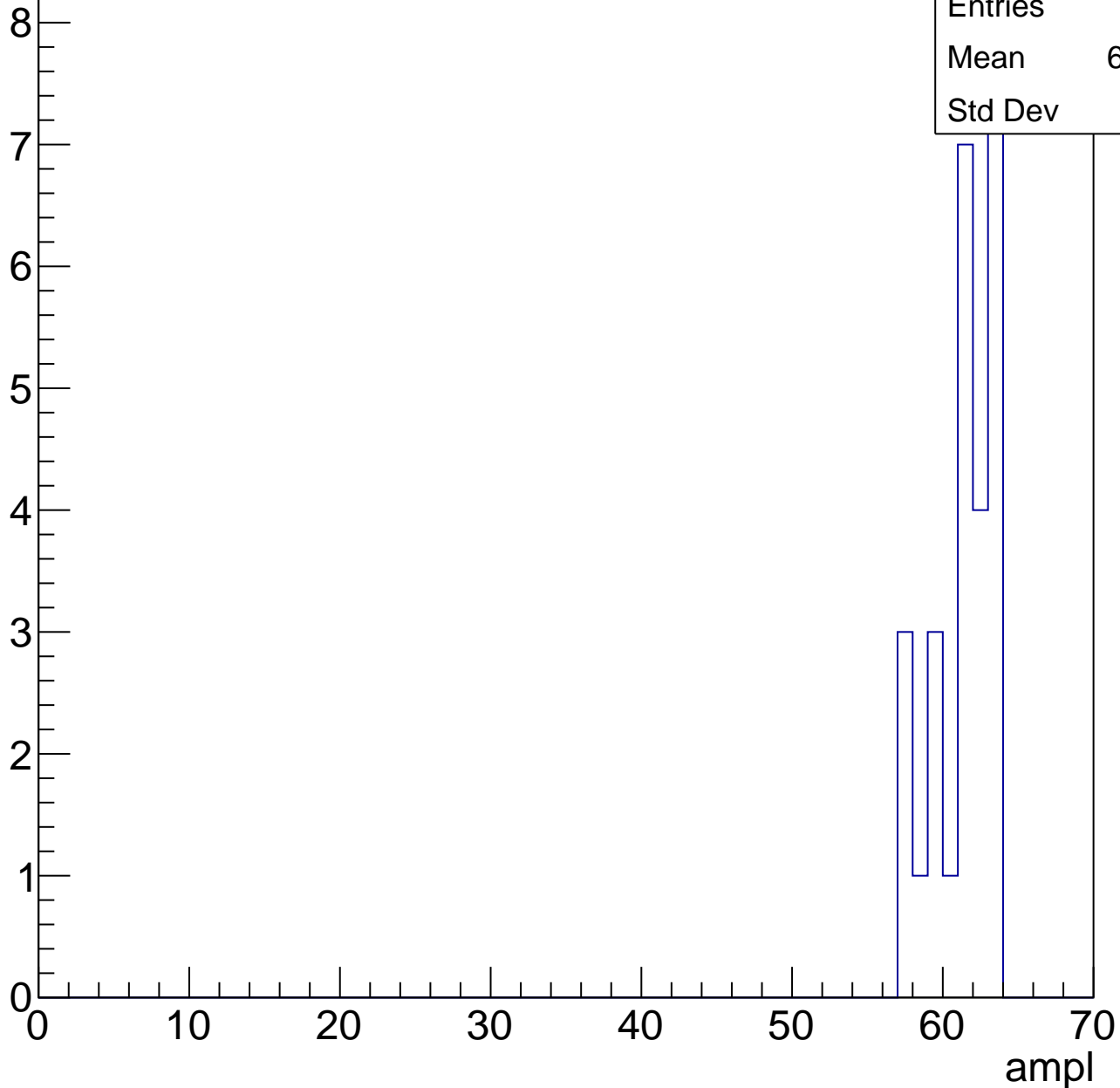


# B0L001S, U21-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	27
Mean	60.93
Std Dev	1.98



# B0L001S, U21-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U21-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U21-ch113, adc0

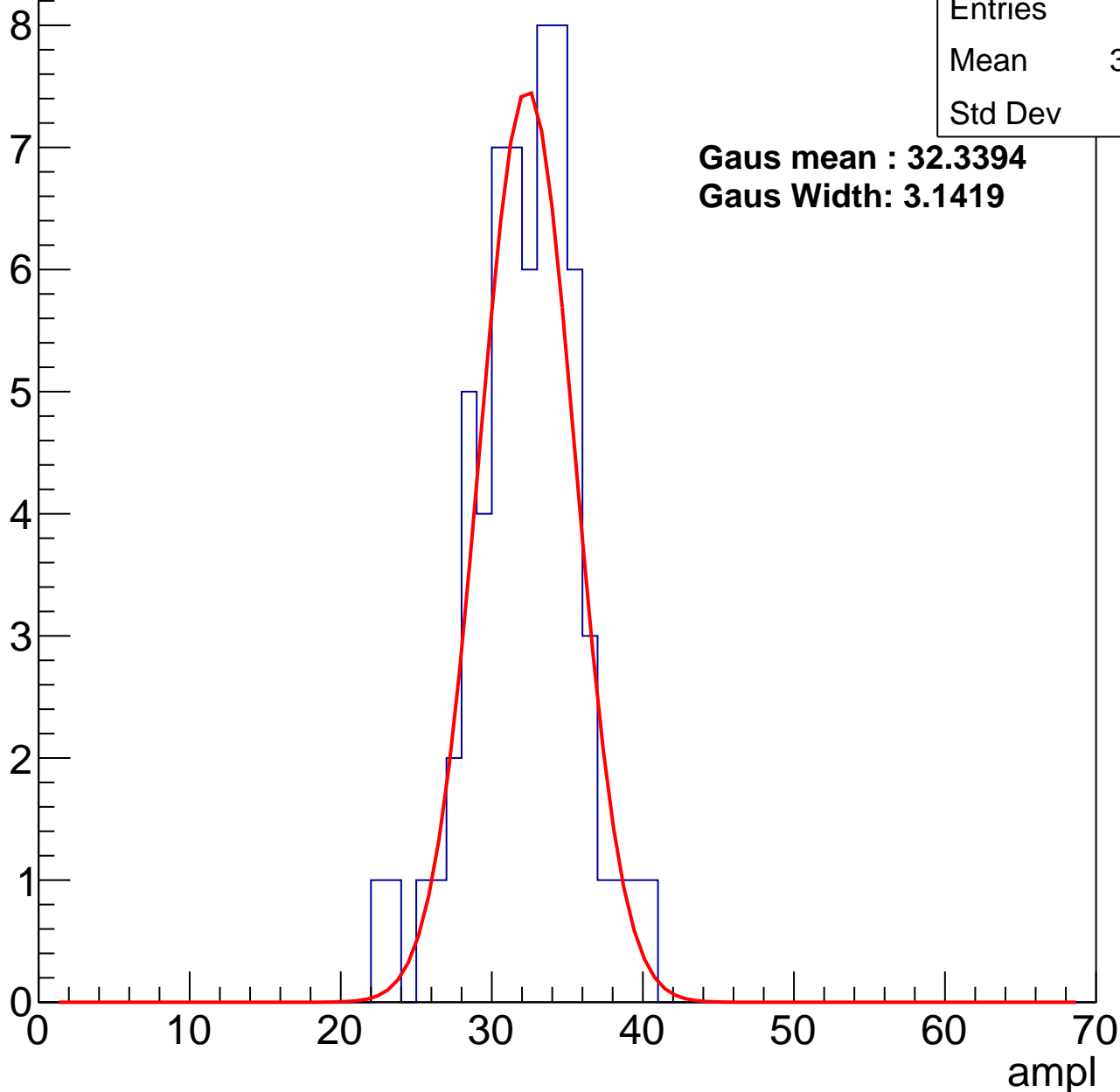
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	64
Mean	31.77
Std Dev	3.49

**Gaus mean : 32.3394**

**Gaus Width: 3.1419**



# B0L001S, U21-ch113, adc1

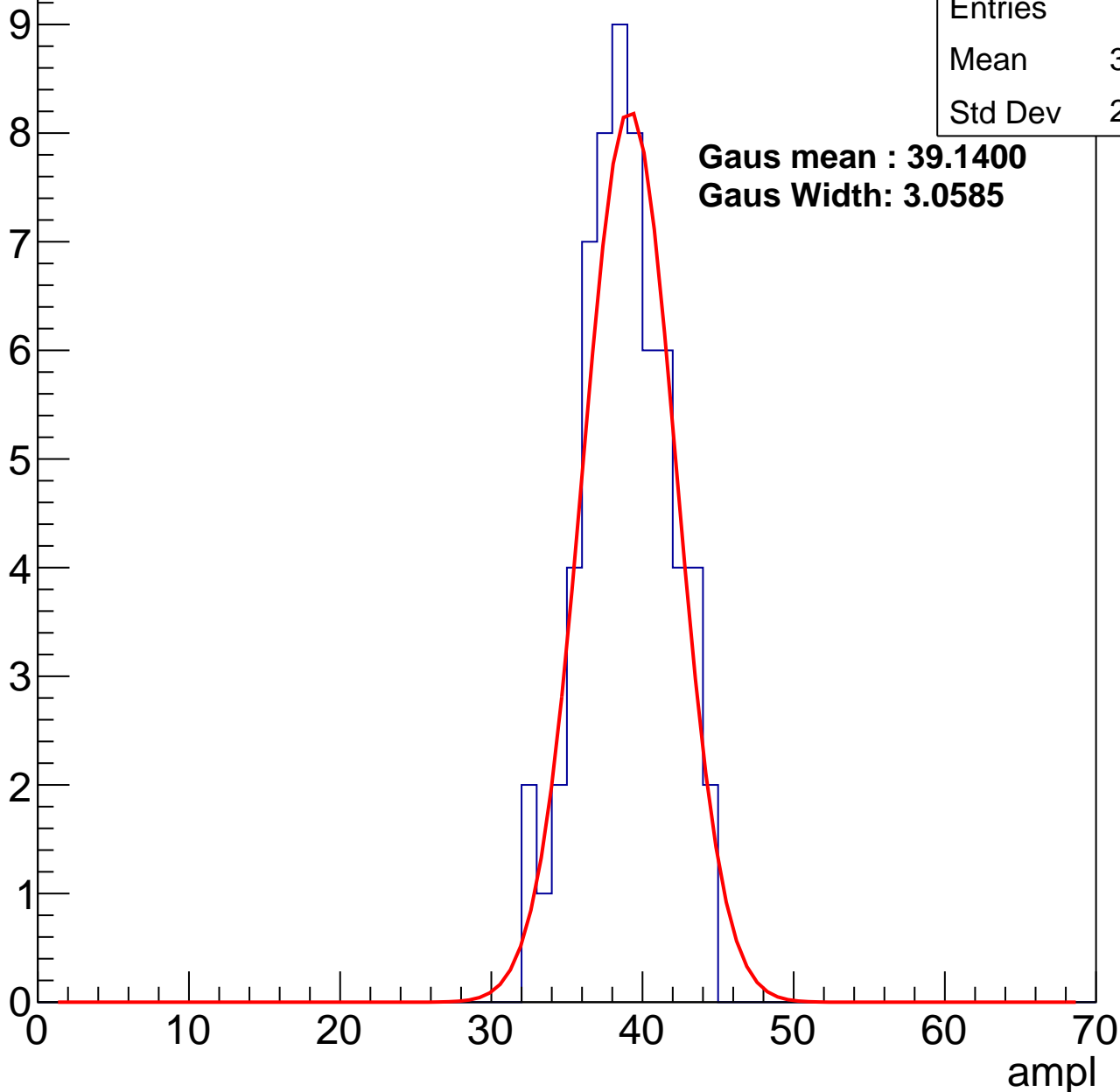
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	38.43
Std Dev	2.849

**Gaus mean : 39.1400**

**Gaus Width: 3.0585**



# B0L001S, U21-ch113, adc2

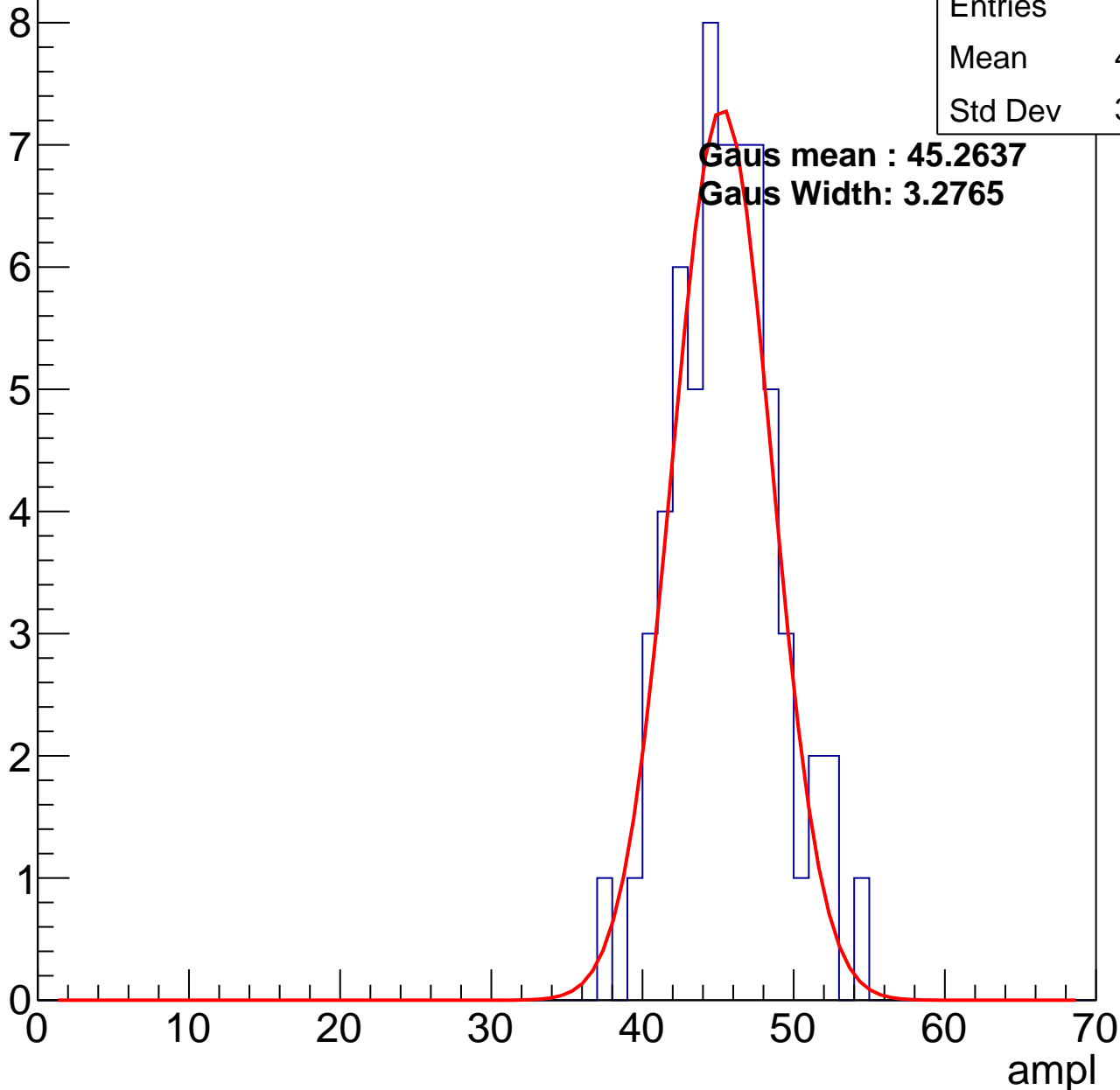
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	45.11
Std Dev	3.391

**Gaus mean : 45.2637**

**Gaus Width: 3.2765**

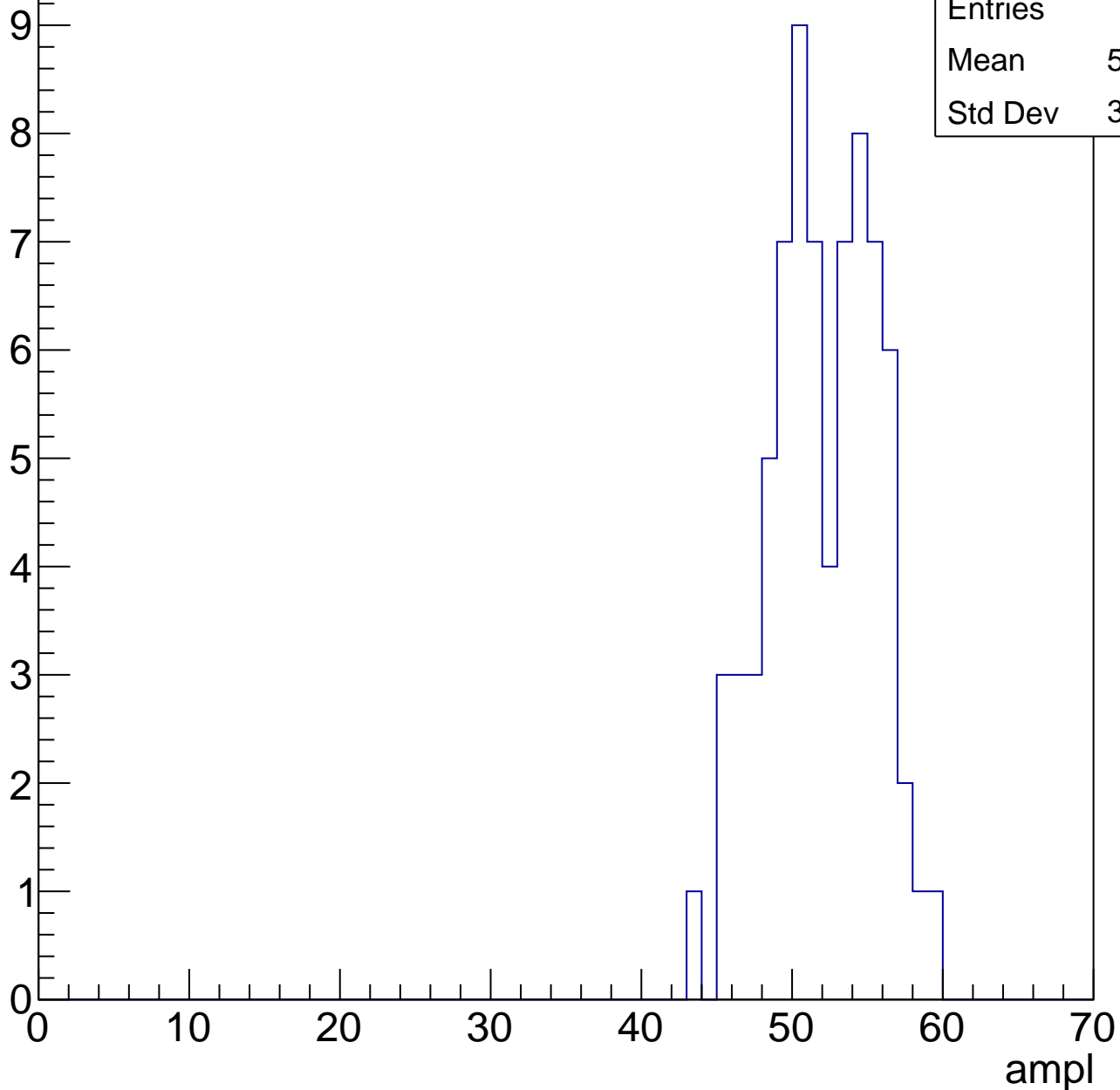


# B0L001S, U21-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

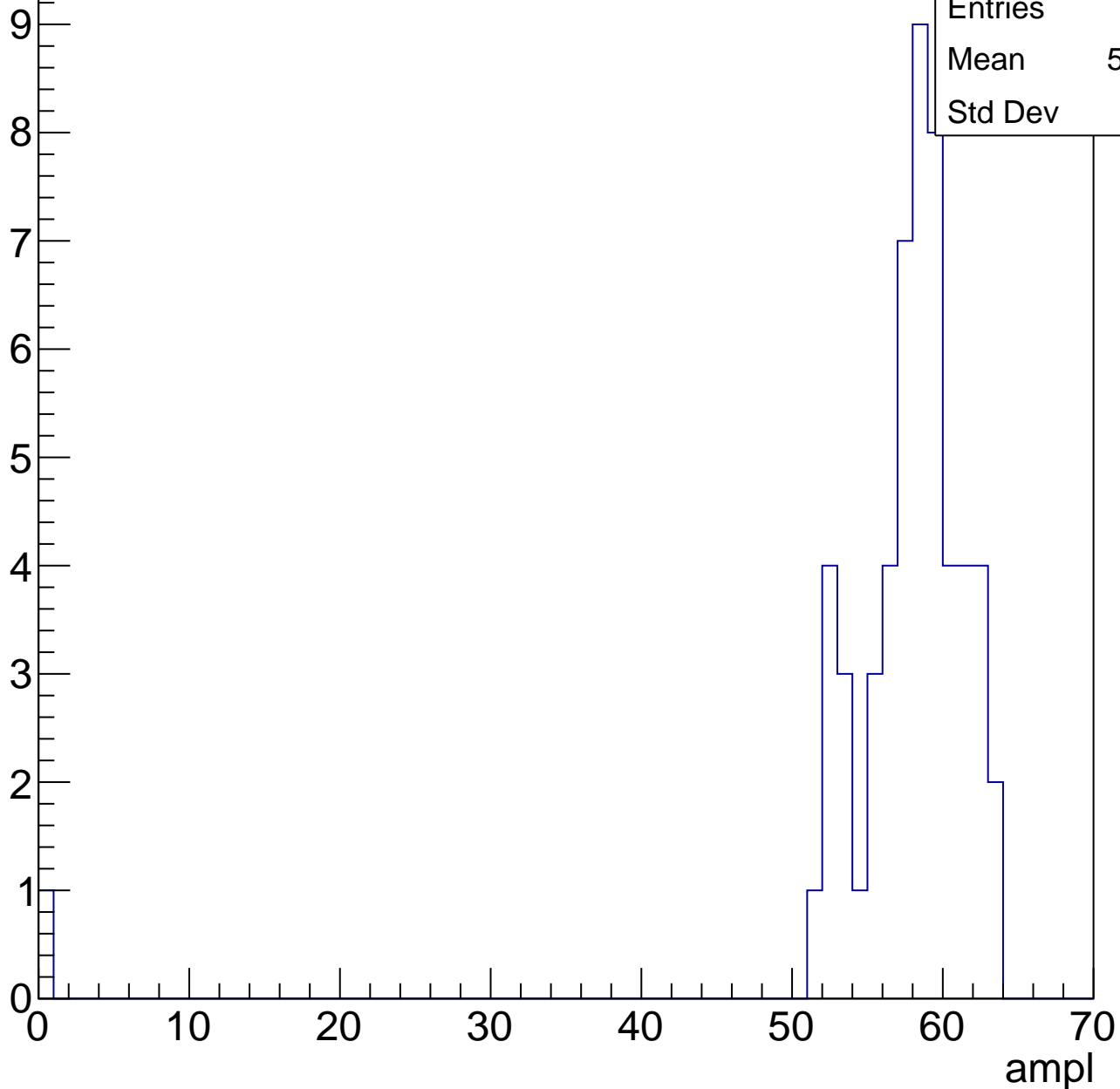
Entries	74
Mean	51.49
Std Dev	3.508



# B0L001S, U21-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

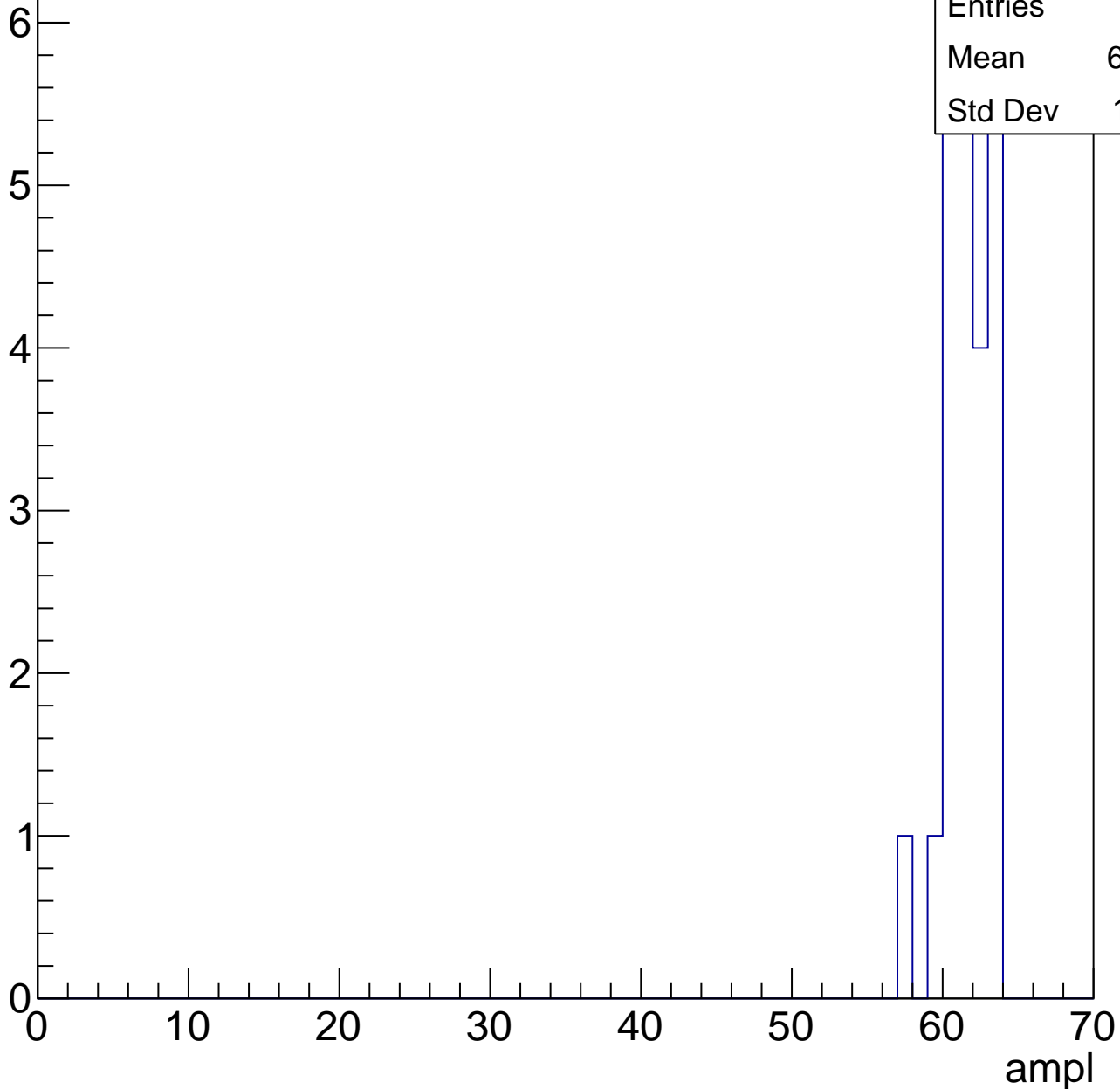


# B0L001S, U21-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	24
Mean	61.17
Std Dev	1.491



# B0L001S, U21-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U21-ch114, adc0

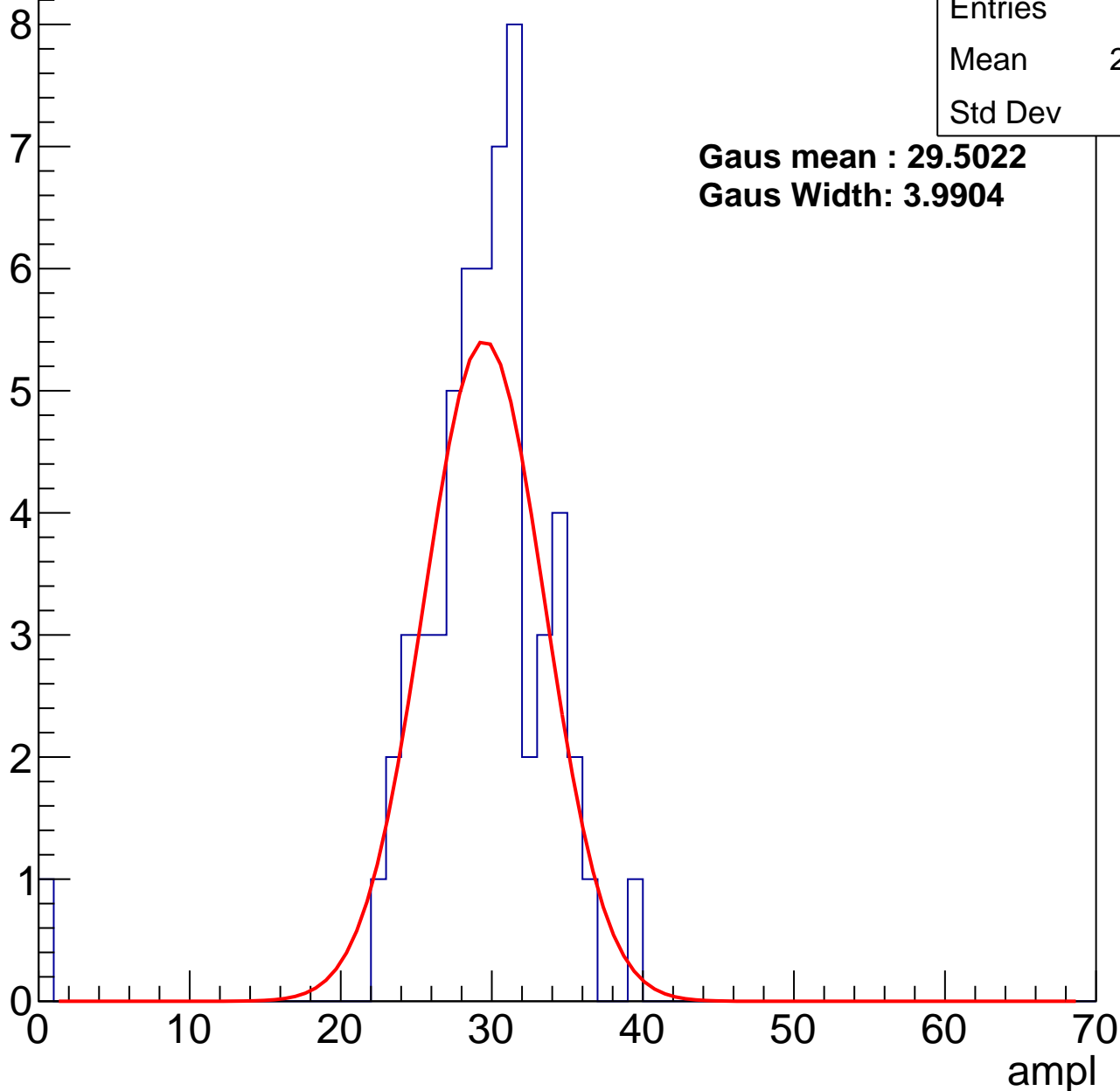
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	28.83
Std Dev	5.19

**Gaus mean : 29.5022**

**Gaus Width: 3.9904**



# B0L001S, U21-ch114, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	82
Mean	36.6
Std Dev	3.338

**Gaus mean : 37.1597**

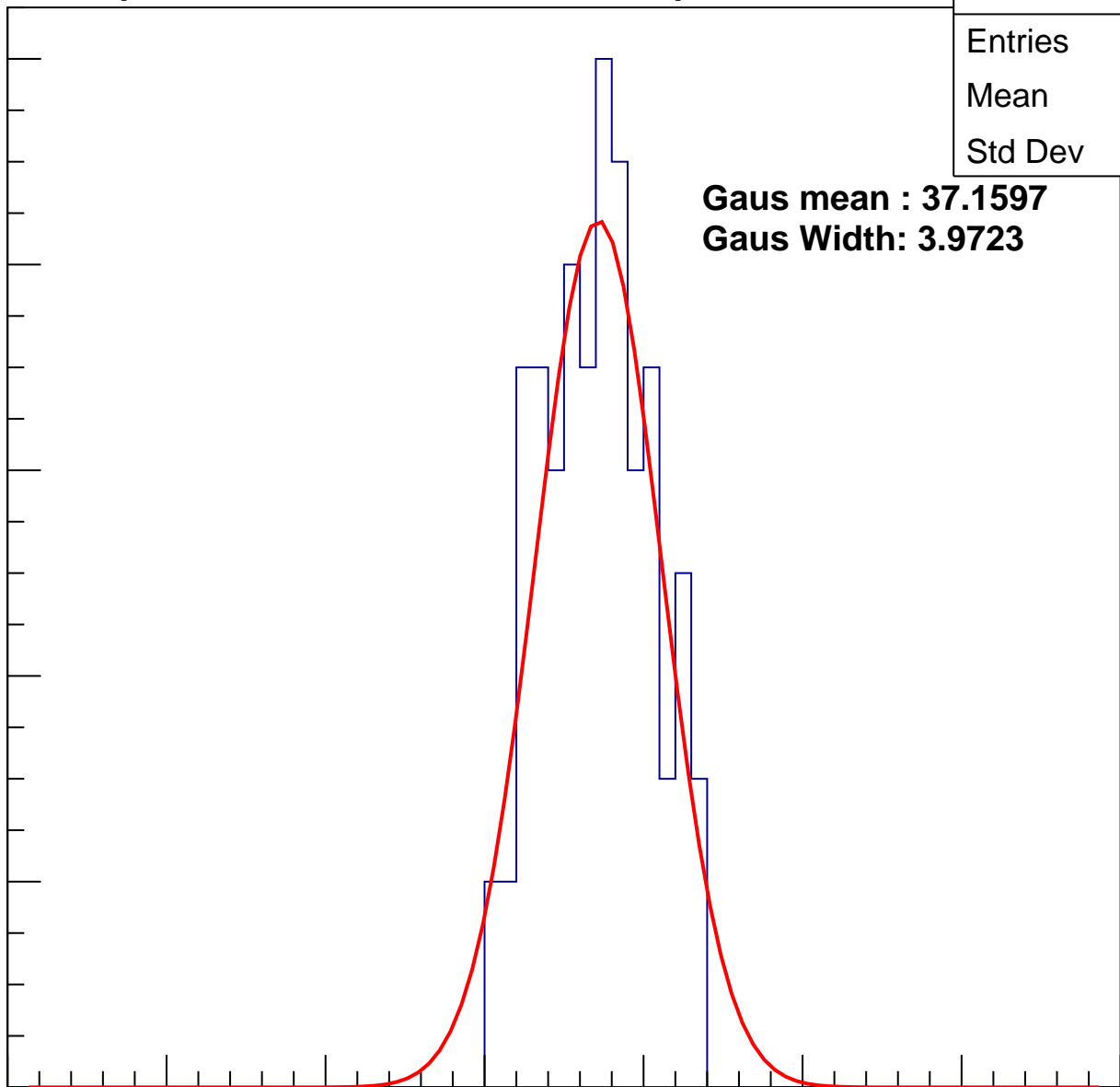
**Gaus Width: 3.9723**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

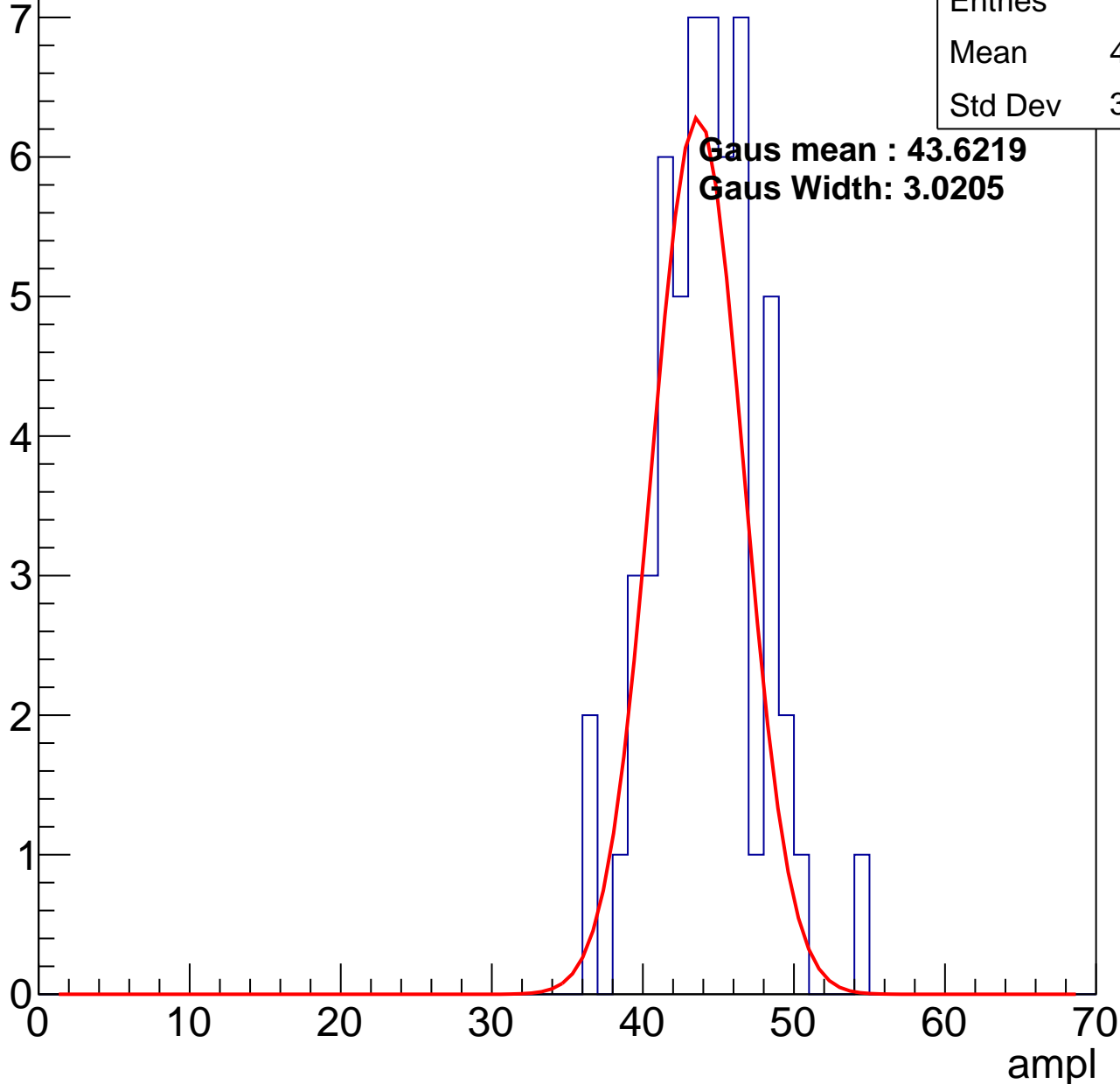


# B0L001S, U21-ch114, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	43.74
Std Dev	3.436

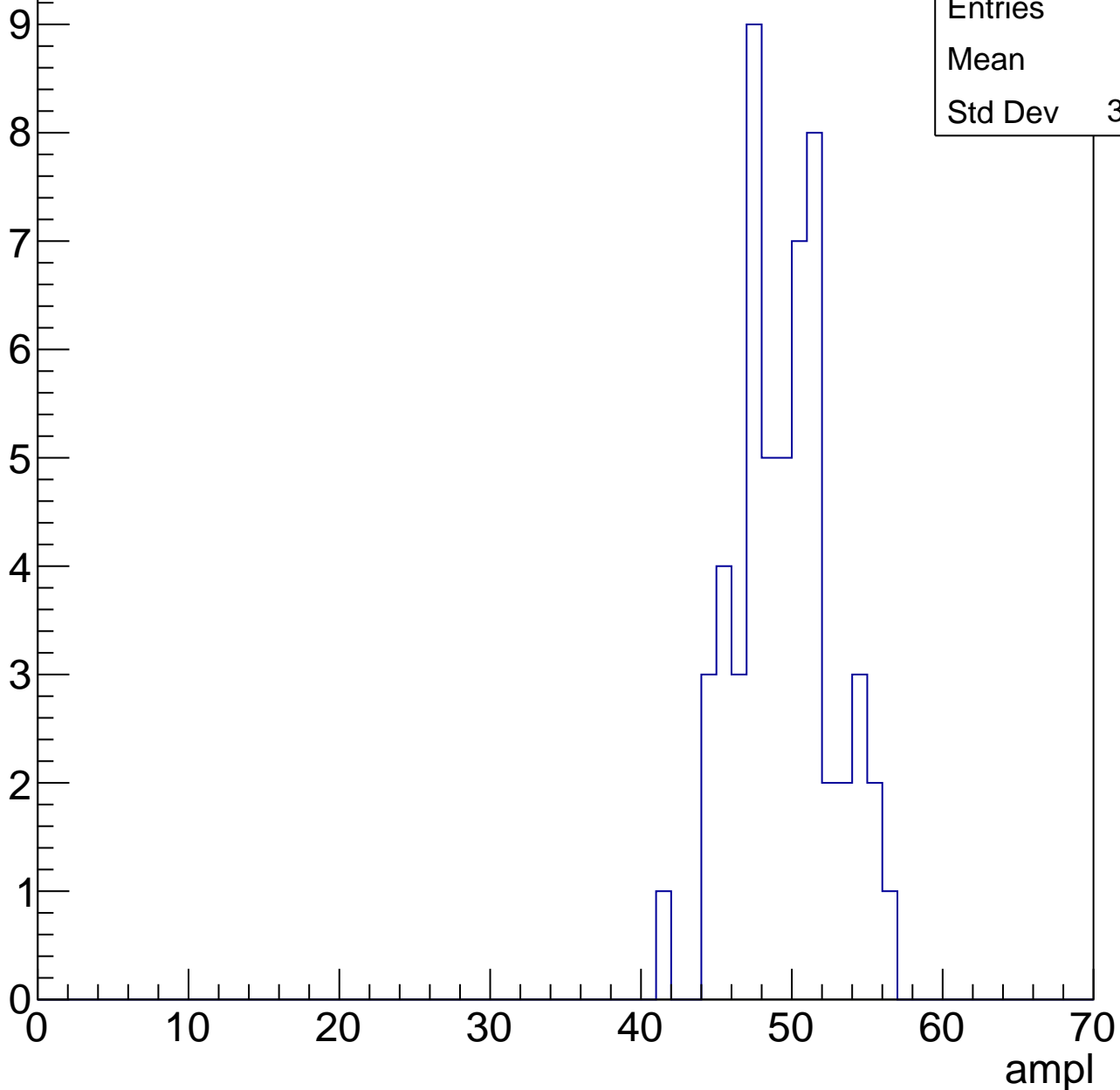


# B0L001S, U21-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	49
Std Dev	3.179

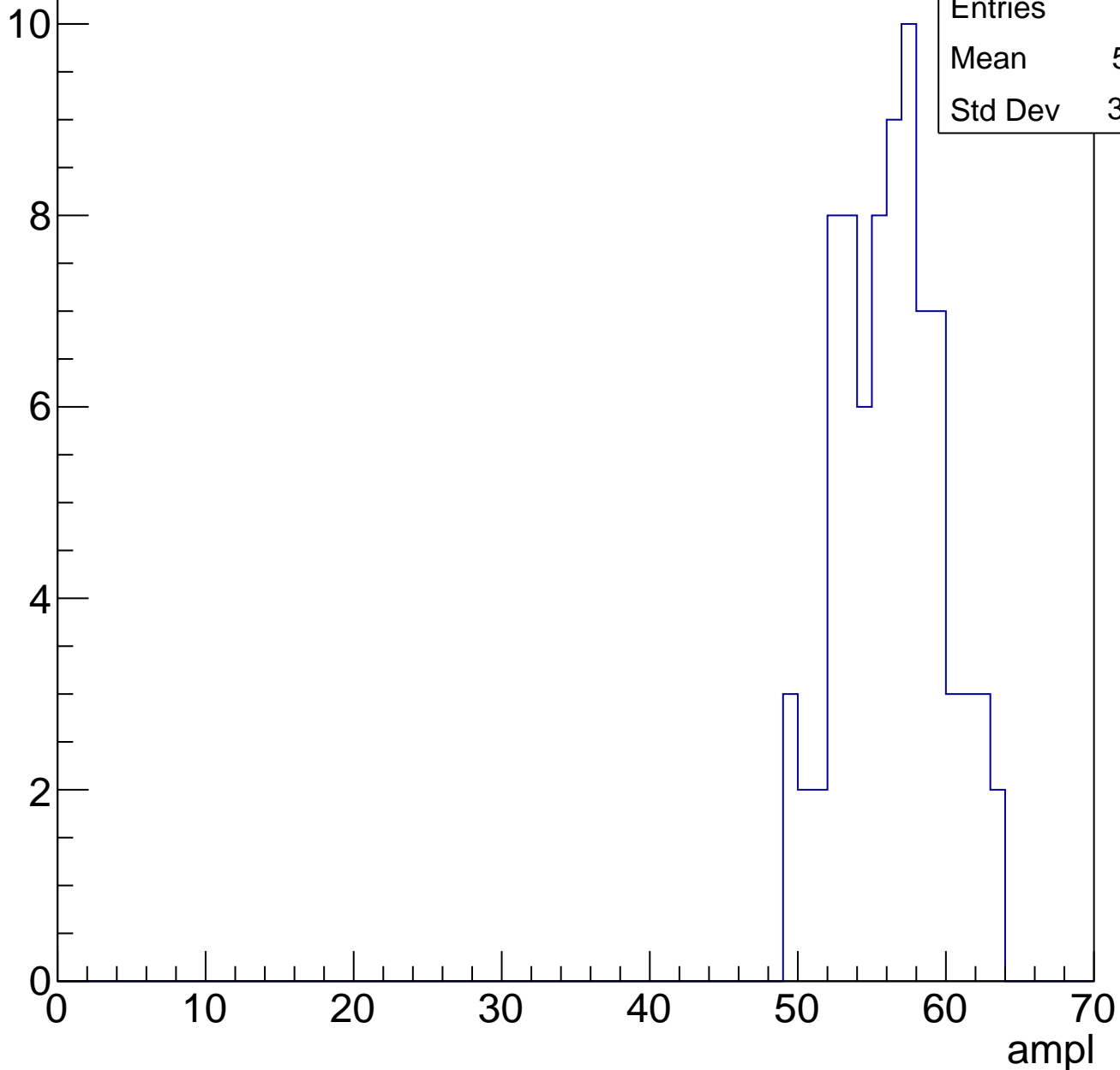


# B0L001S, U21-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	81
Mean	55.81
Std Dev	3.385

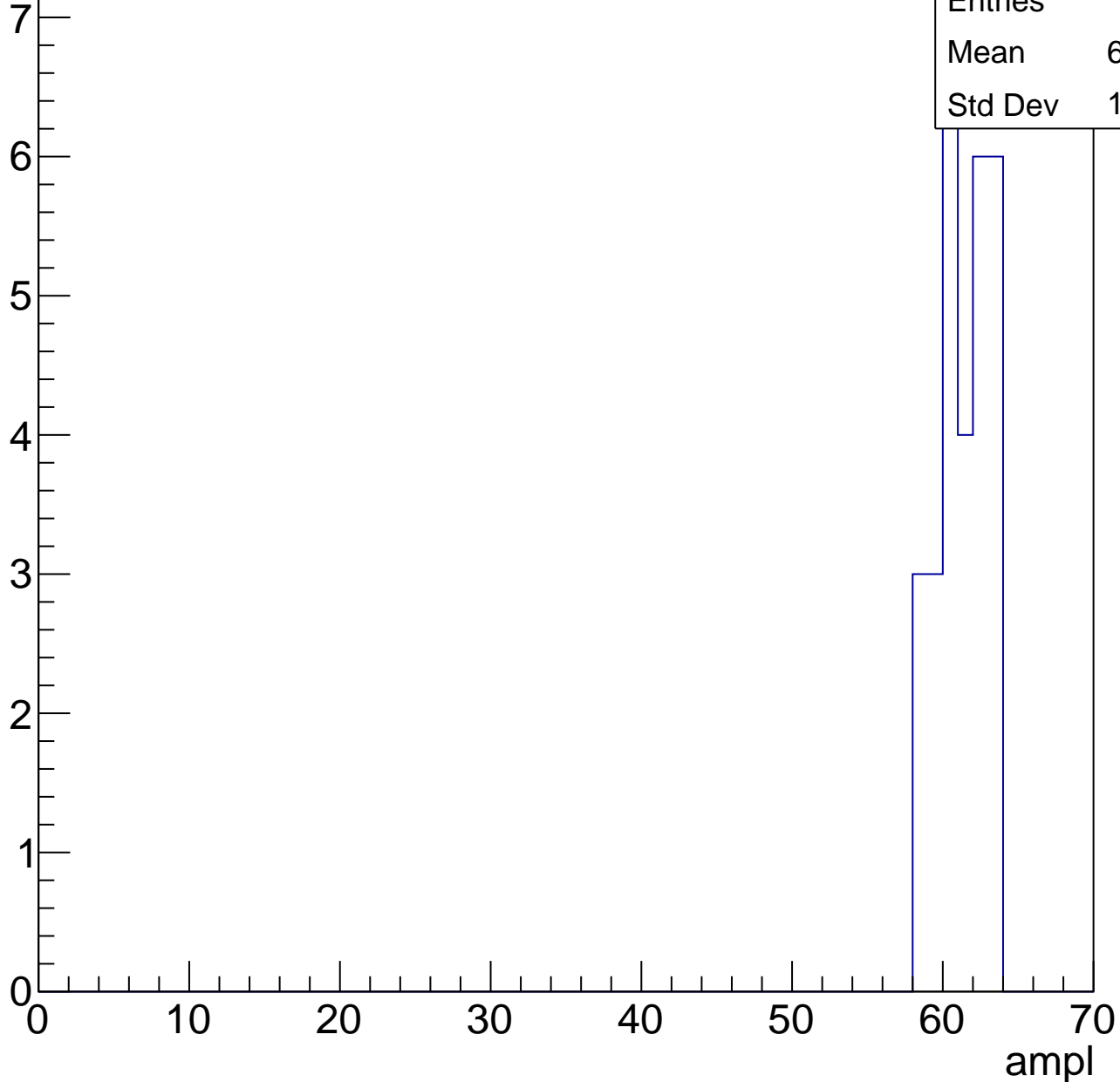
Entry



# B0L001S, U21-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

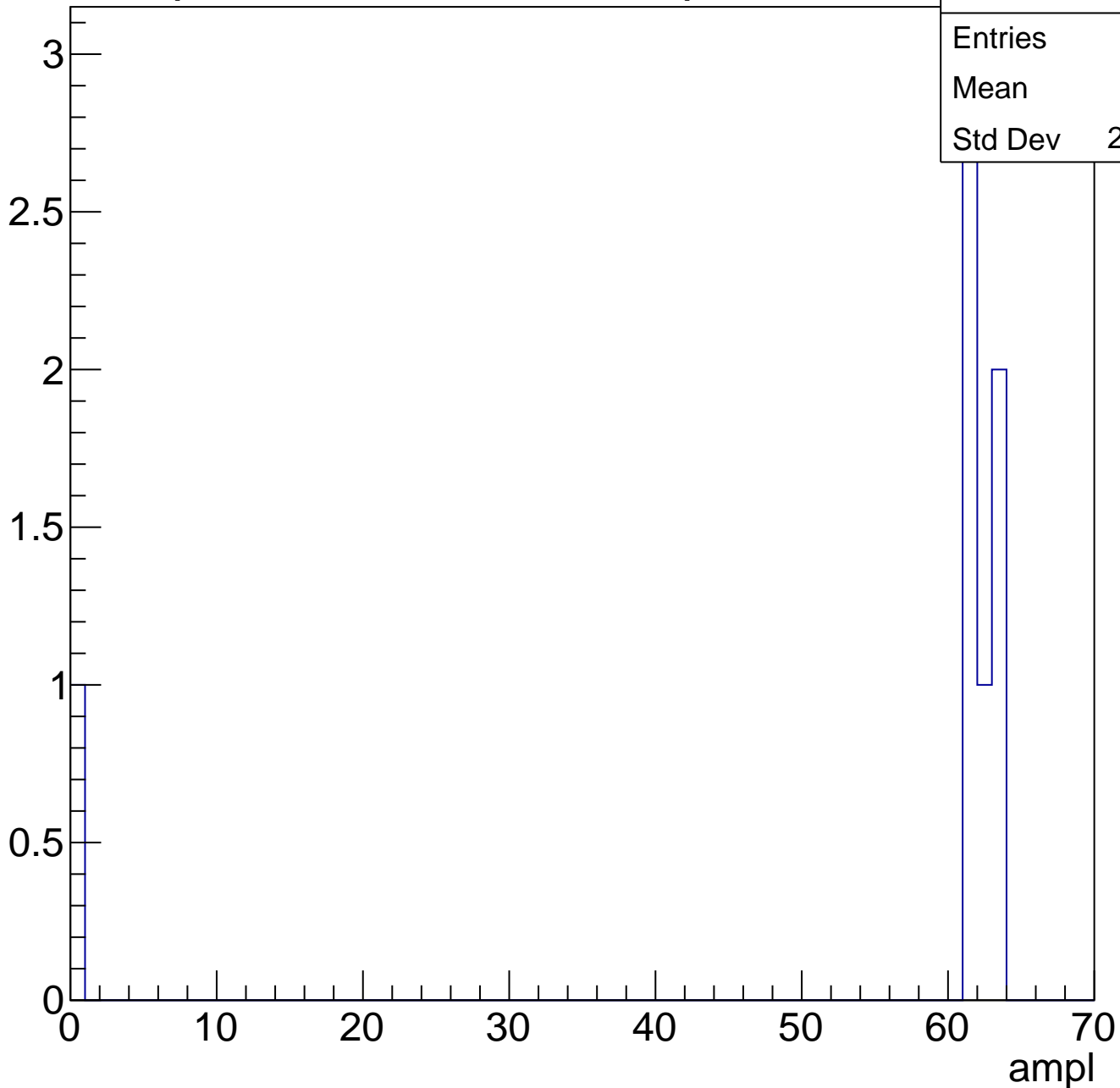
Entry



# B0L001S, U21-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

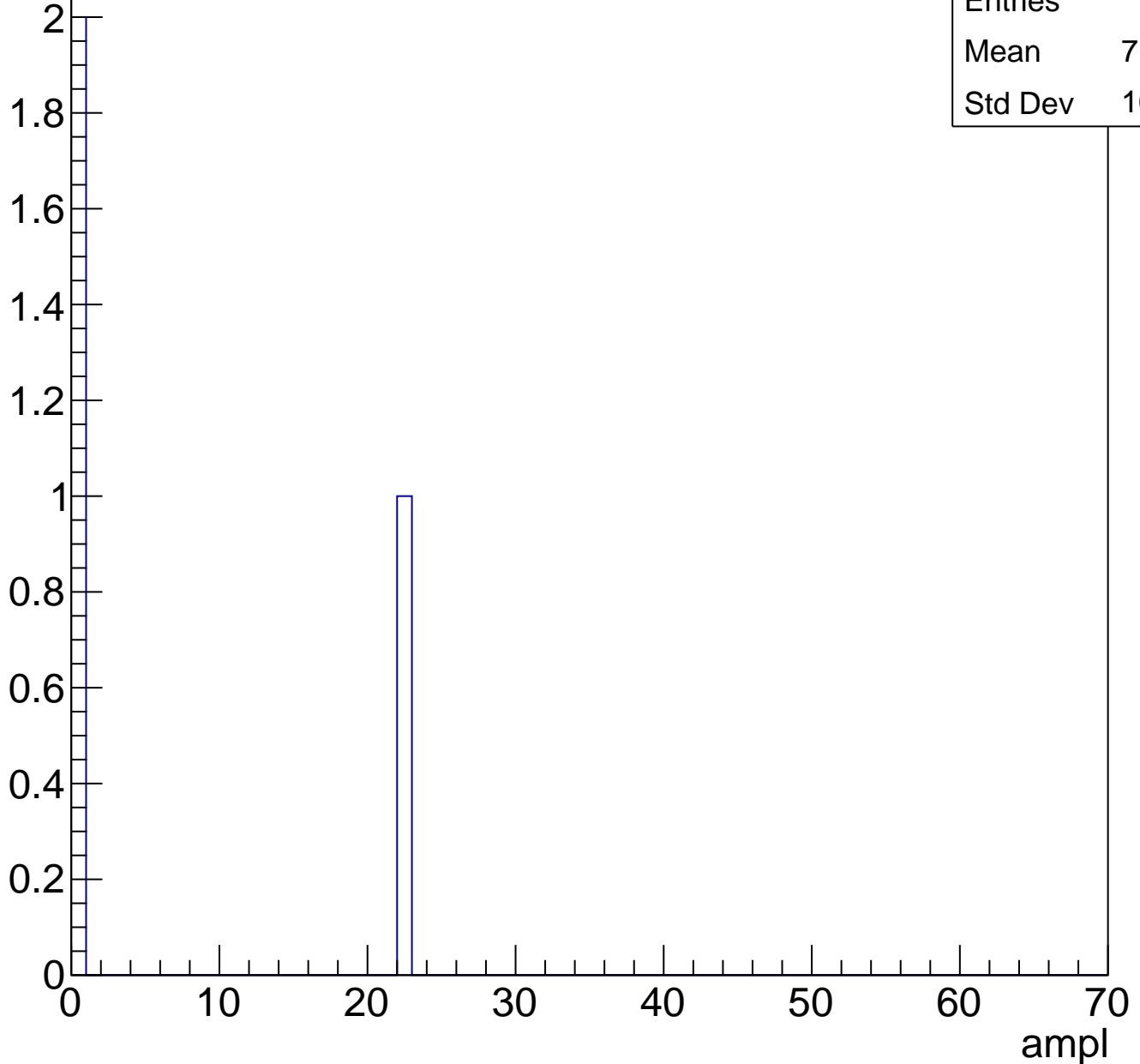




# B0L001S, U21-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	3
Mean	7.333
Std Dev	10.37

# B0L001S, U21-ch115, adc0

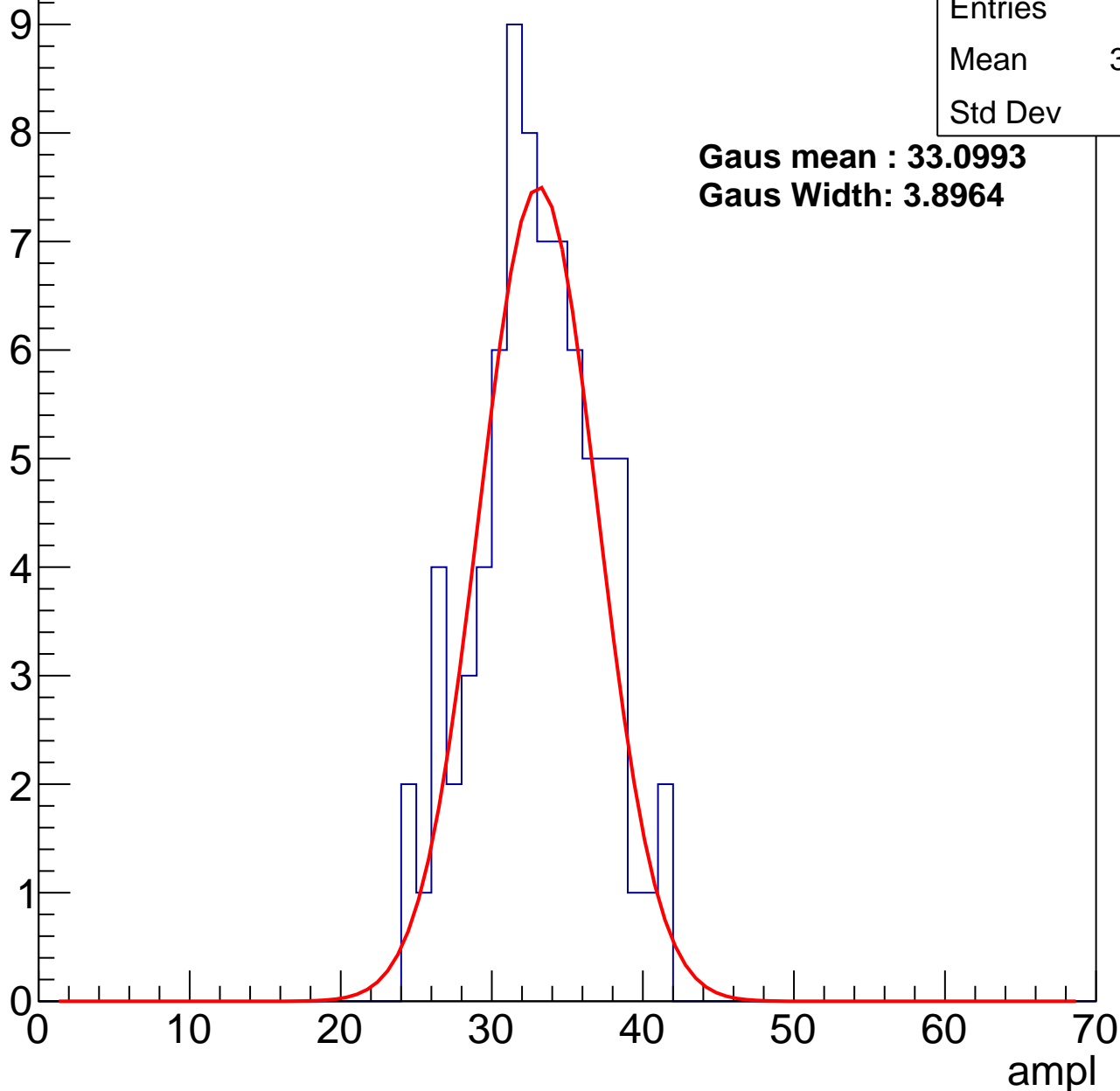
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	78
Mean	32.58
Std Dev	3.94

**Gaus mean : 33.0993**

**Gaus Width: 3.8964**



# B0L001S, U21-ch115, adc1

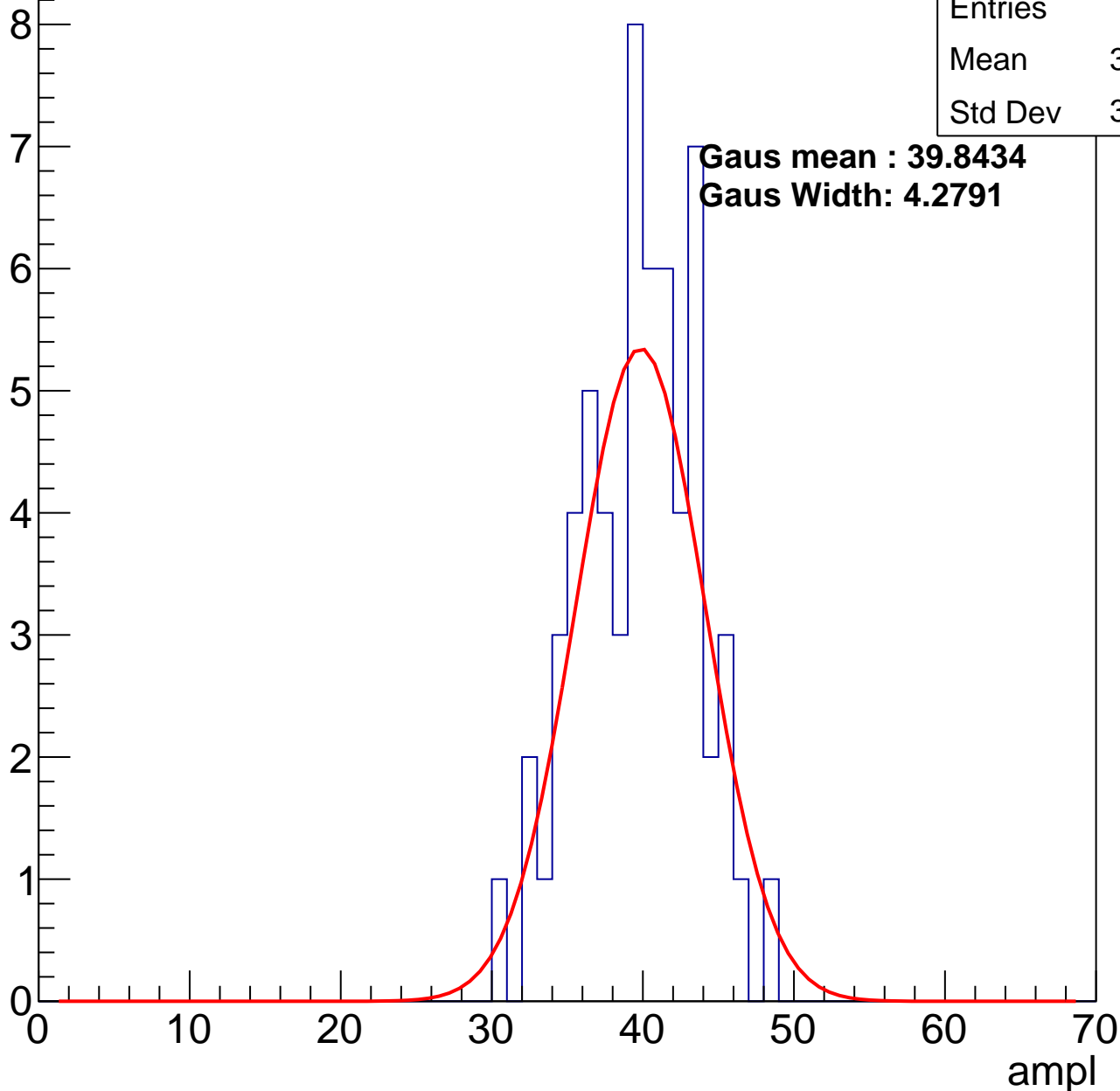
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	61
Mean	39.26
Std Dev	3.798

**Gaus mean : 39.8434**

**Gaus Width: 4.2791**



# B0L001S, U21-ch115, adc2

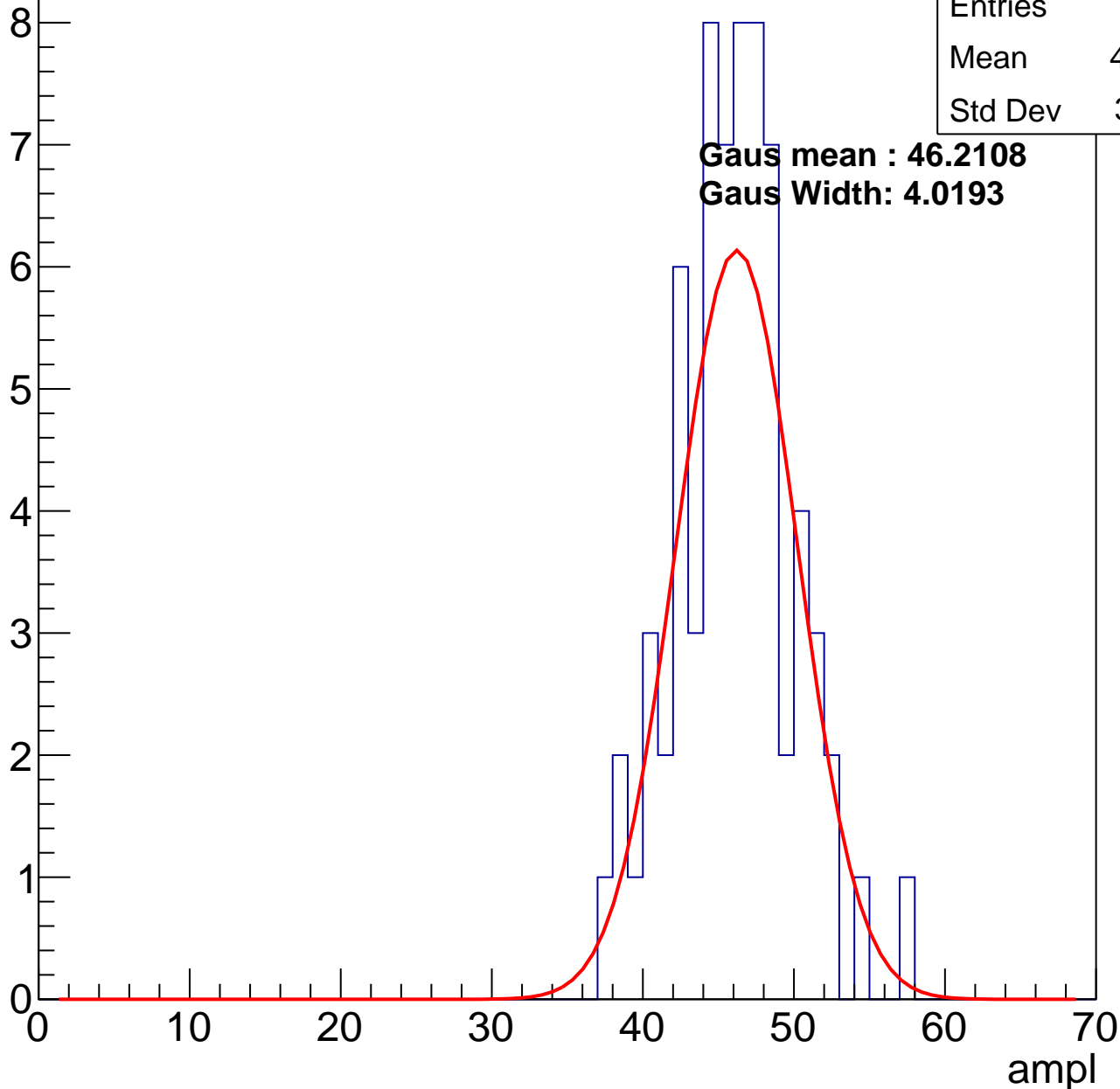
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	45.62
Std Dev	3.841

Gaus mean : 46.2108

Gaus Width: 4.0193

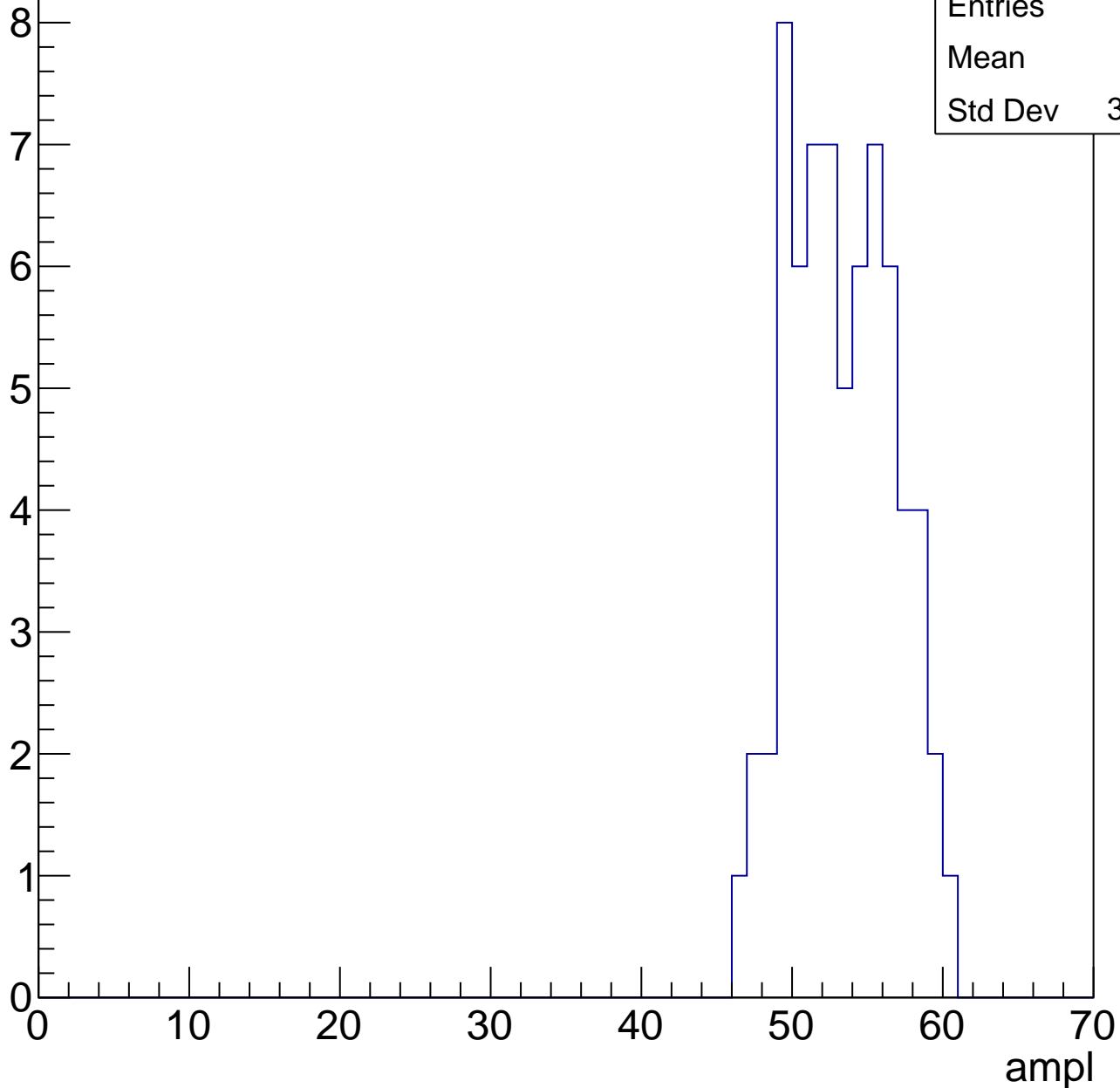


# B0L001S, U21-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	52.9
Std Dev	3.344

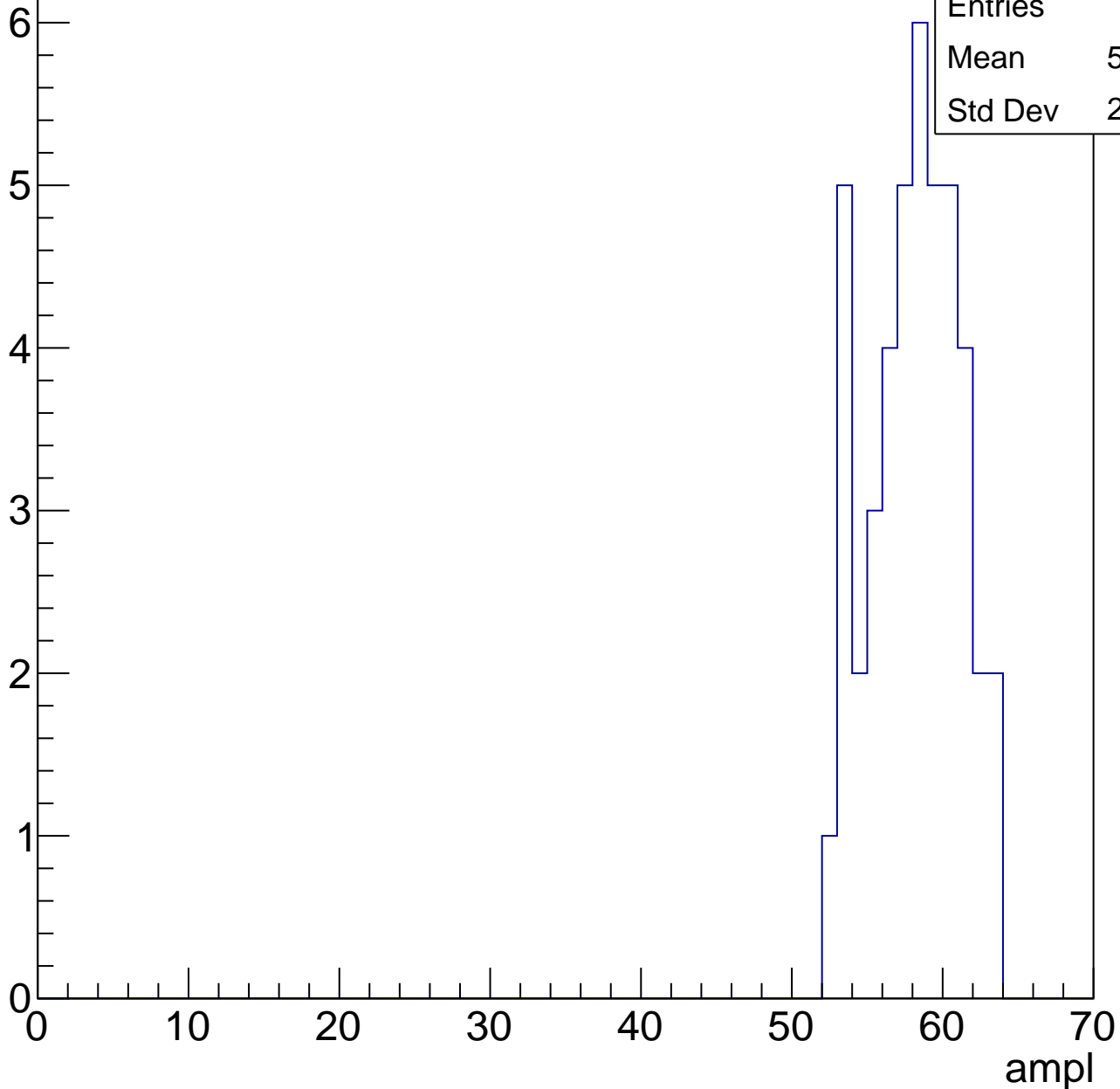


# B0L001S, U21-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	44
Mean	57.64
Std Dev	2.932

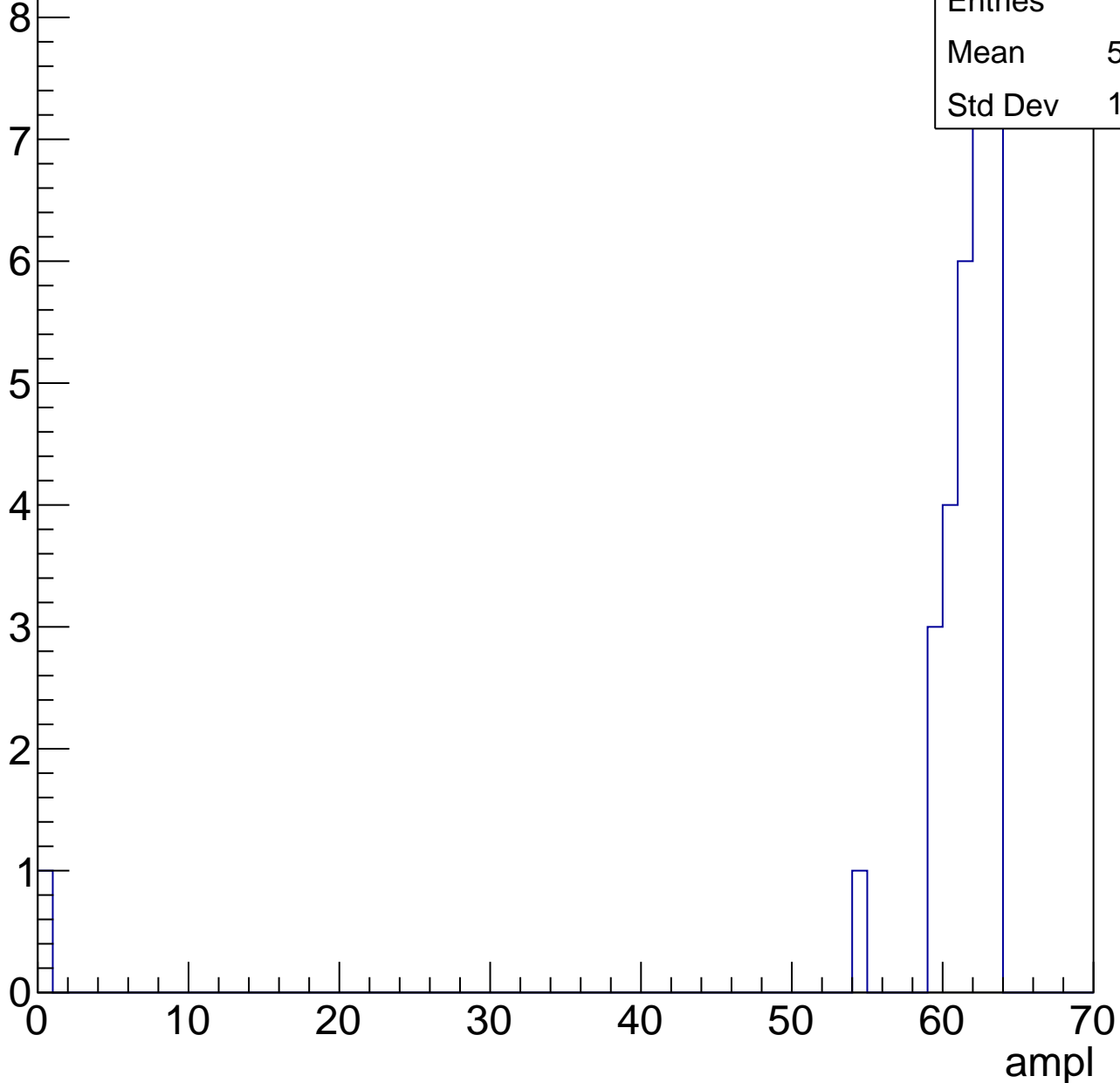


# B0L001S, U21-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	31
Mean	59.26
Std Dev	10.97



# B0L001S, U21-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U21-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U21-ch116, adc0

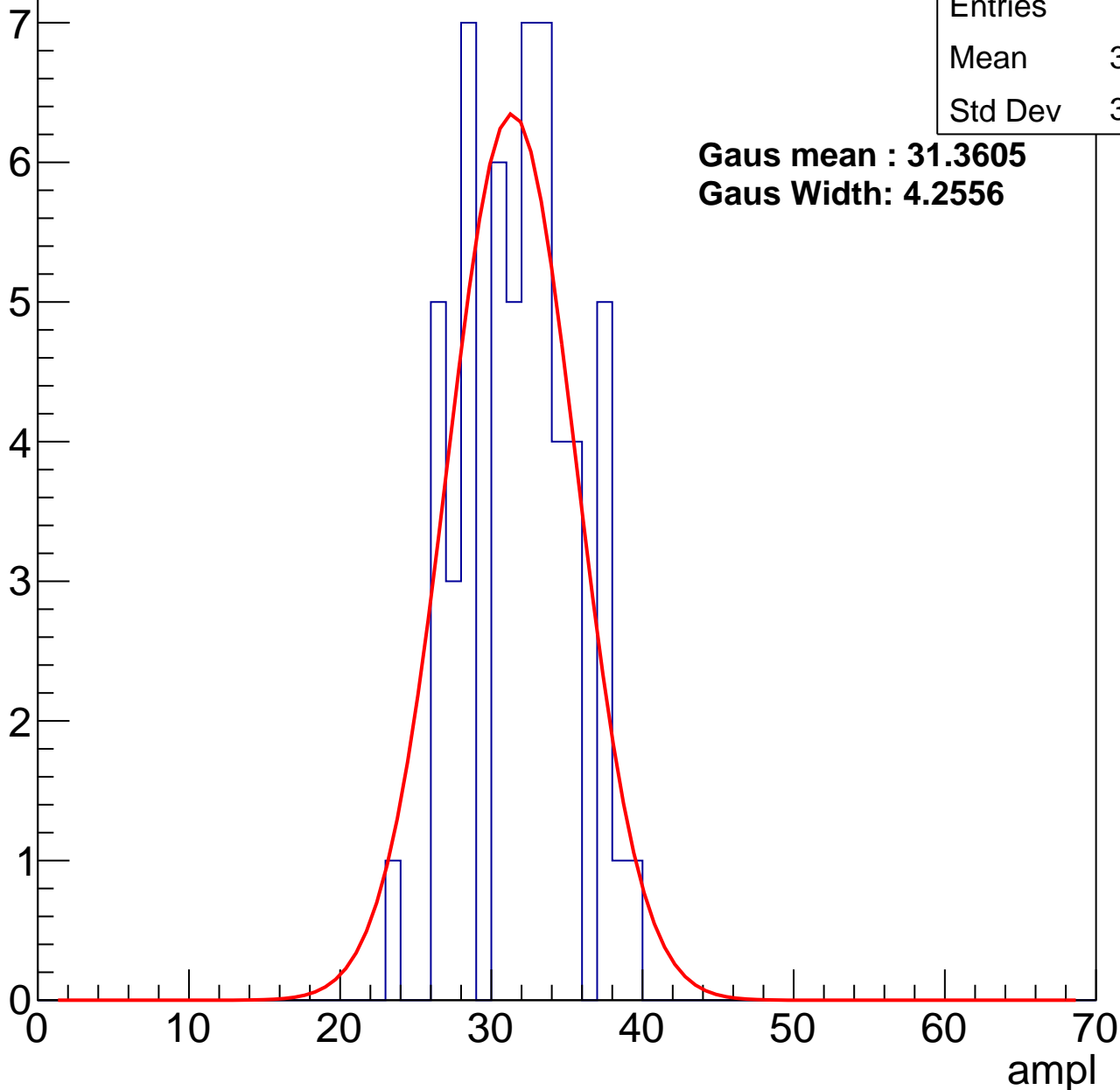
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	56
Mean	31.39
Std Dev	3.599

**Gaus mean : 31.3605**

**Gaus Width: 4.2556**



# B0L001S, U21-ch116, adc1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	62
Mean	38.03
Std Dev	3.316

**Gaus mean : 38.2505**

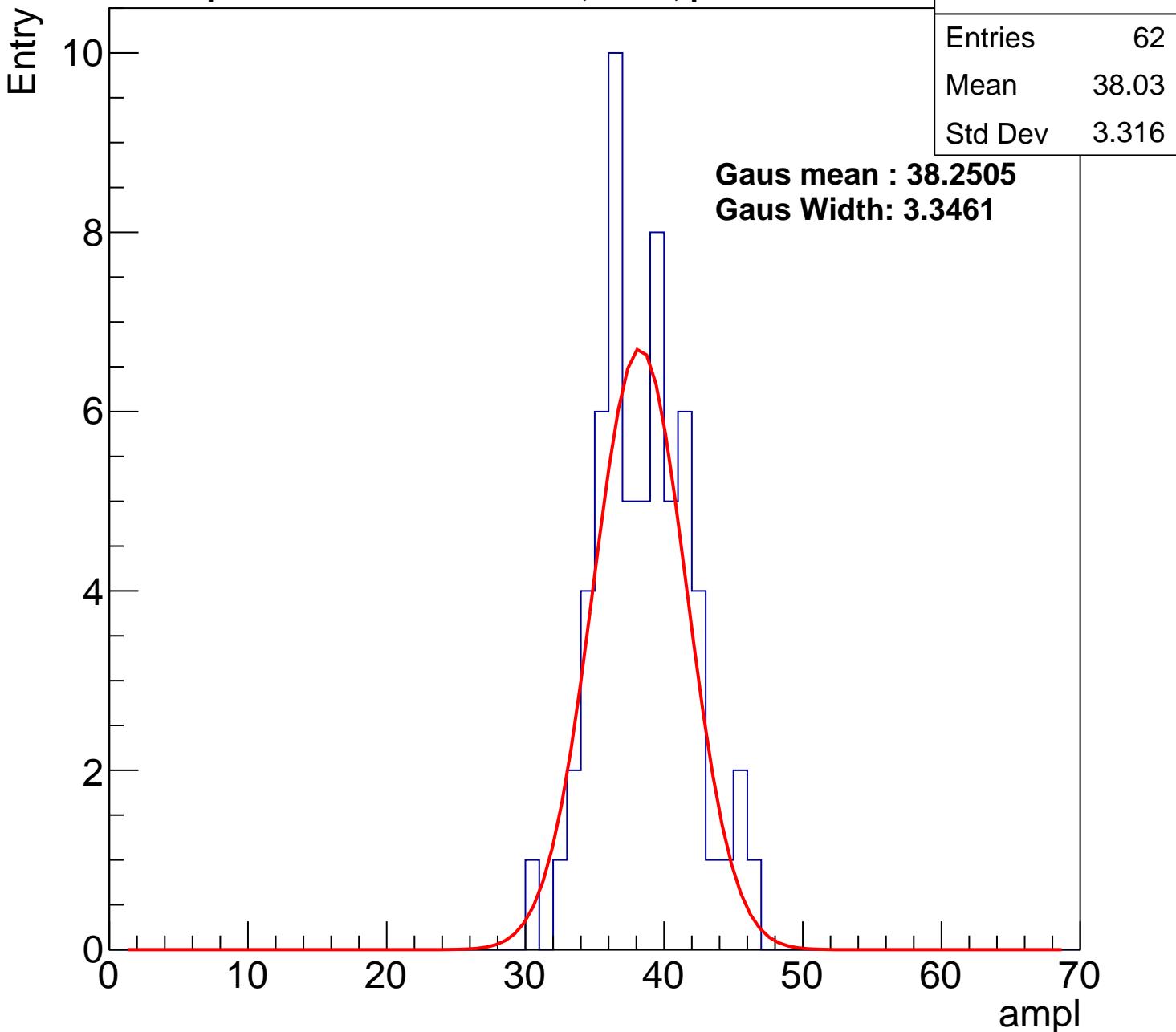
**Gaus Width: 3.3461**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U21-ch116, adc2

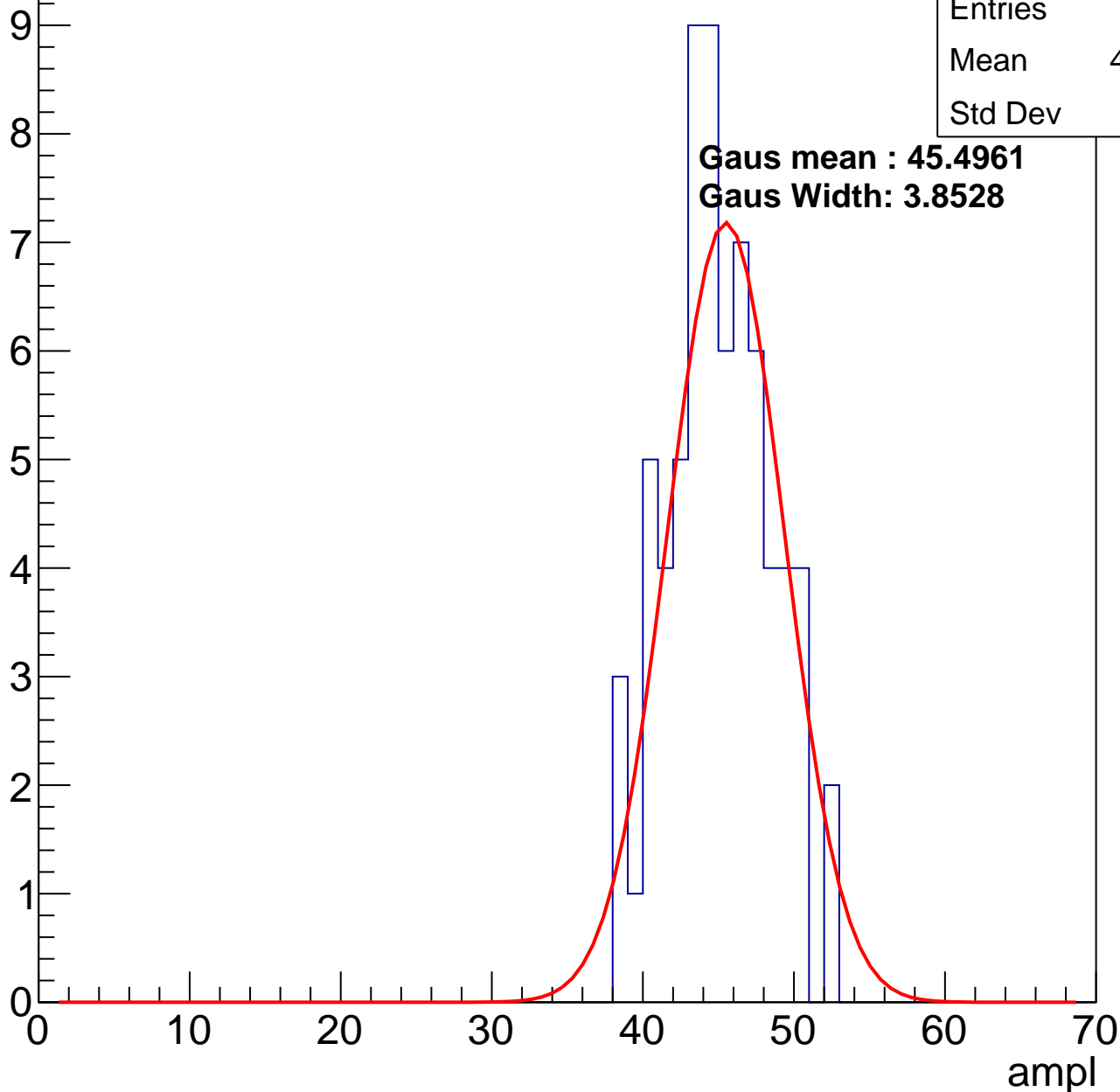
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	69
Mean	44.58
Std Dev	3.36

**Gaus mean : 45.4961**

**Gaus Width: 3.8528**

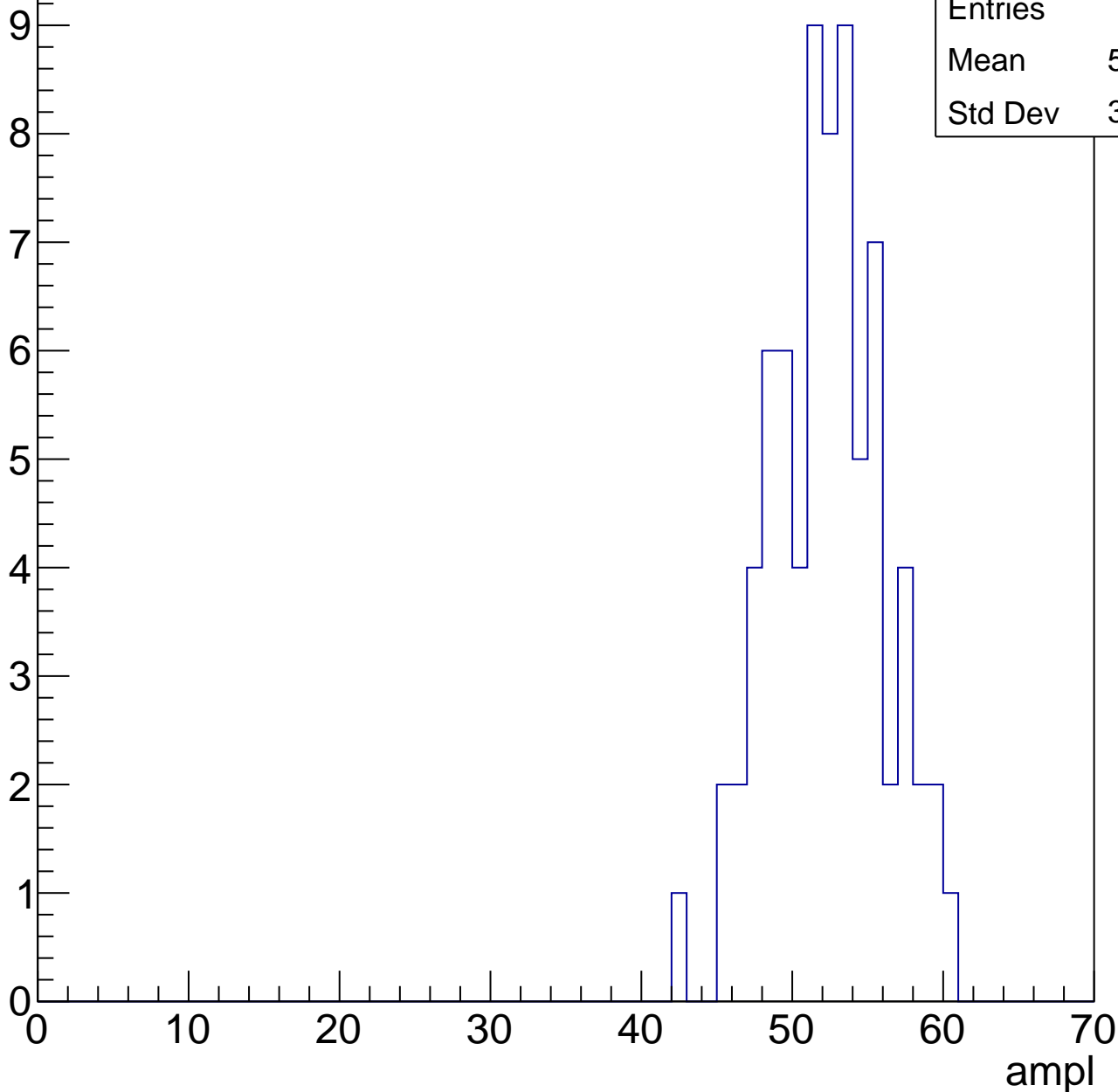


# B0L001S, U21-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	51.82
Std Dev	3.677

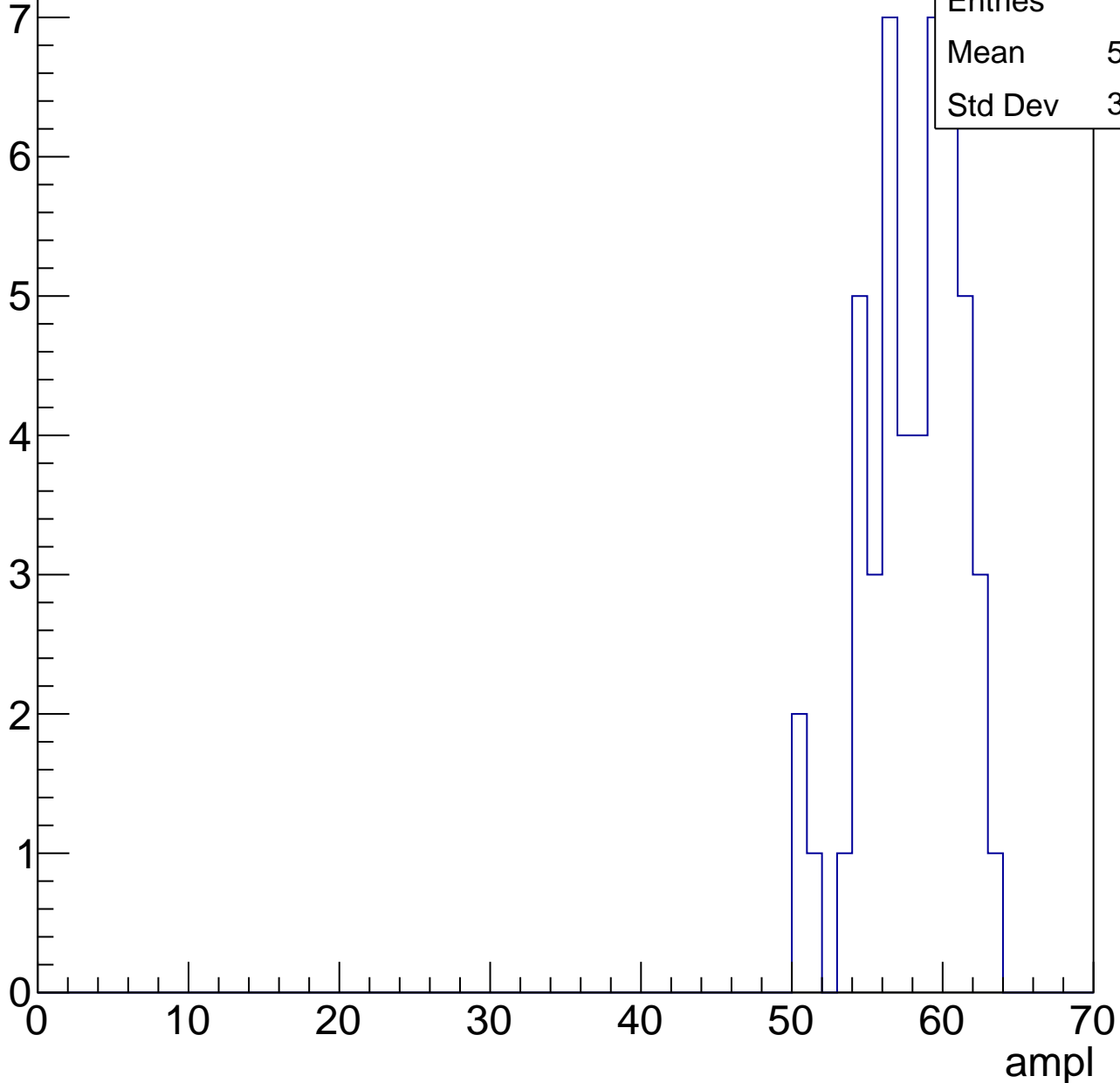


# B0L001S, U21-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	57.56
Std Dev	3.112

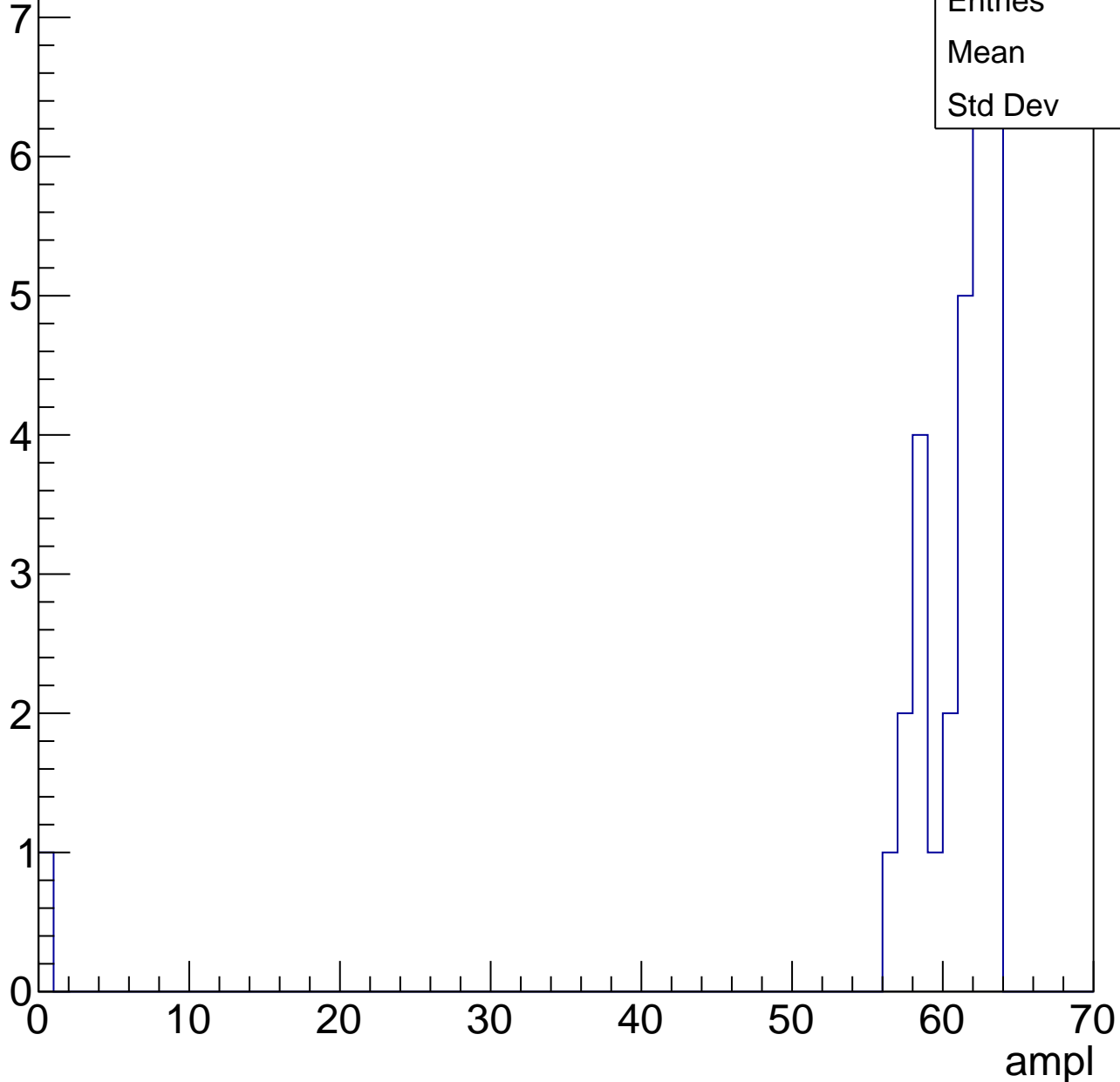


# B0L001S, U21-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	30
Mean	58.7
Std Dev	11.1



# B0L001S, U21-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

0 10 20 30 40 50 60 70

ampl



# B0L001S, U21-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U21-ch117, adc0

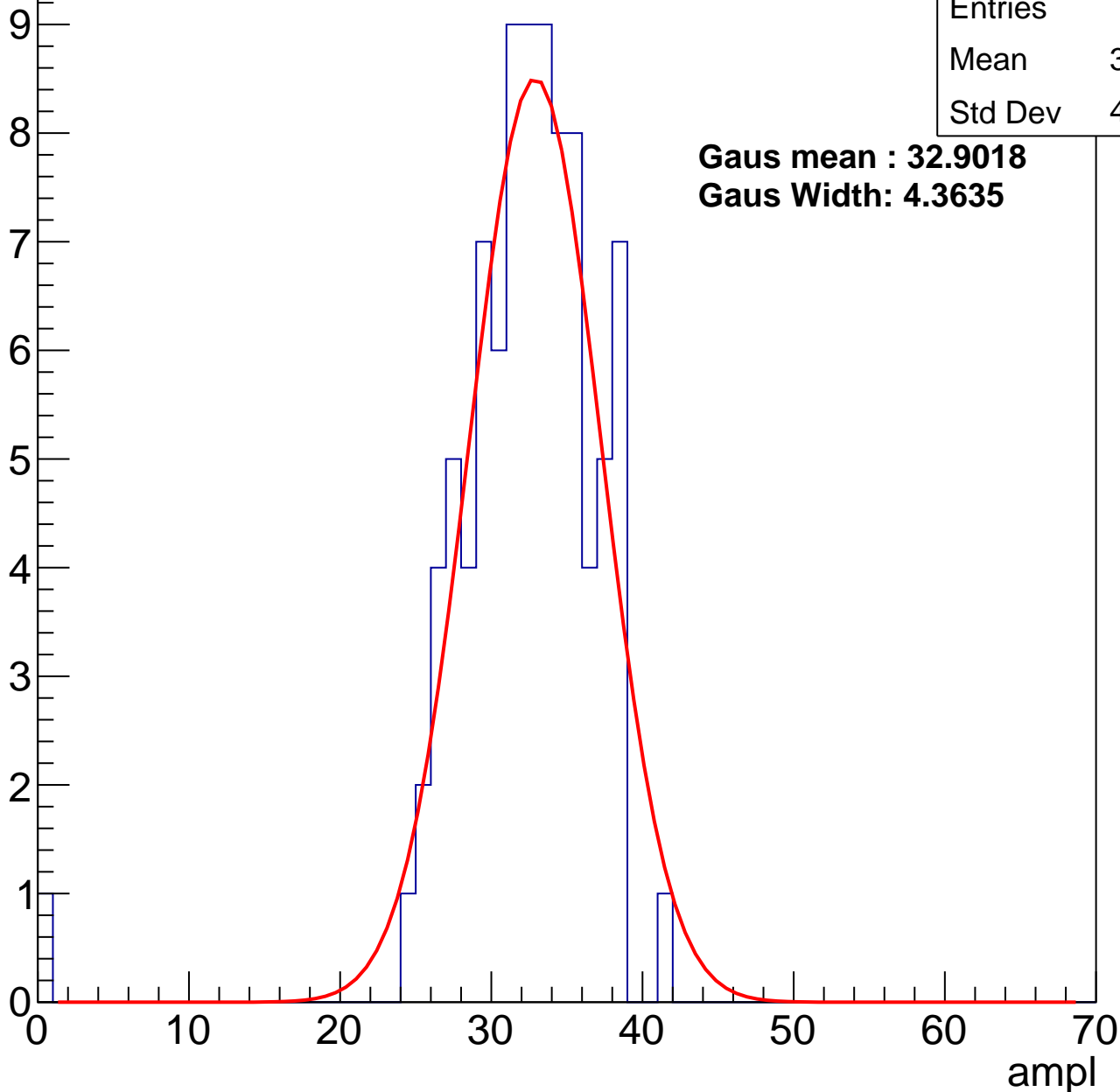
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	90
Mean	31.78
Std Dev	4.995

**Gaus mean : 32.9018**

**Gaus Width: 4.3635**



# B0L001S, U21-ch117, adc1

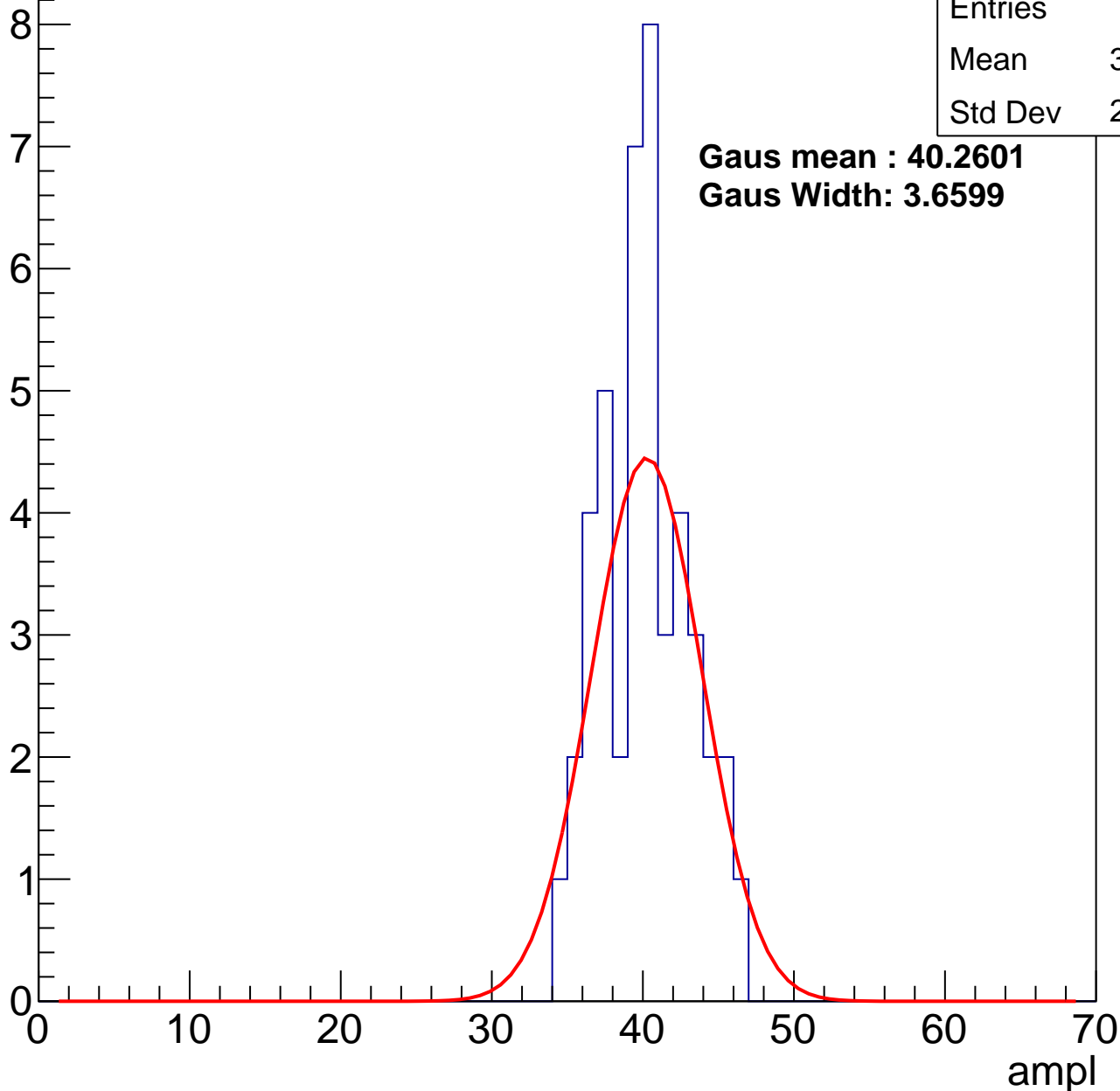
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	44
Mean	39.68
Std Dev	2.898

**Gaus mean : 40.2601**

**Gaus Width: 3.6599**

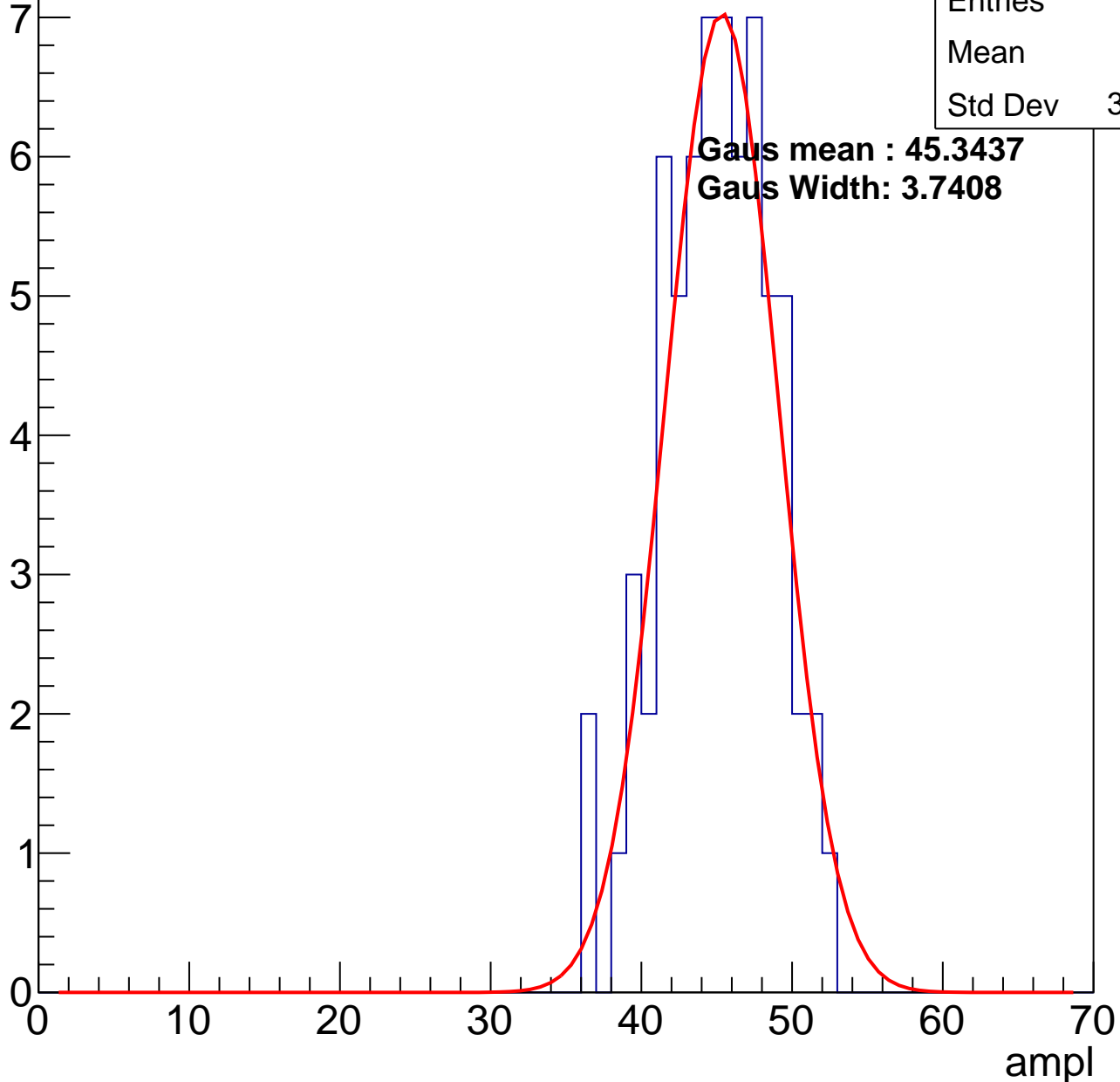


# B0L001S, U21-ch117, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	67
Mean	44.6
Std Dev	3.583

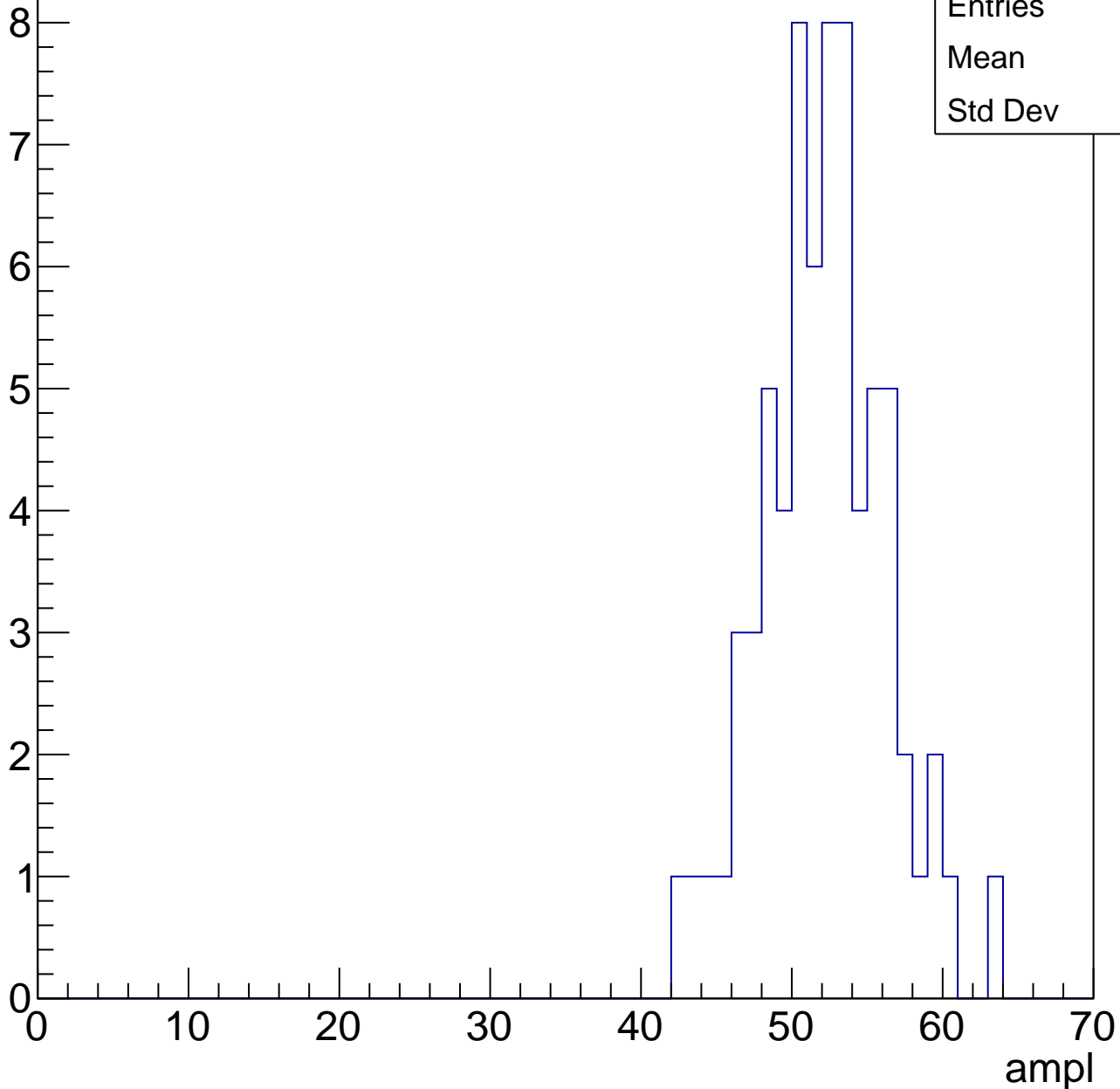


# B0L001S, U21-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	51.7
Std Dev	4.04

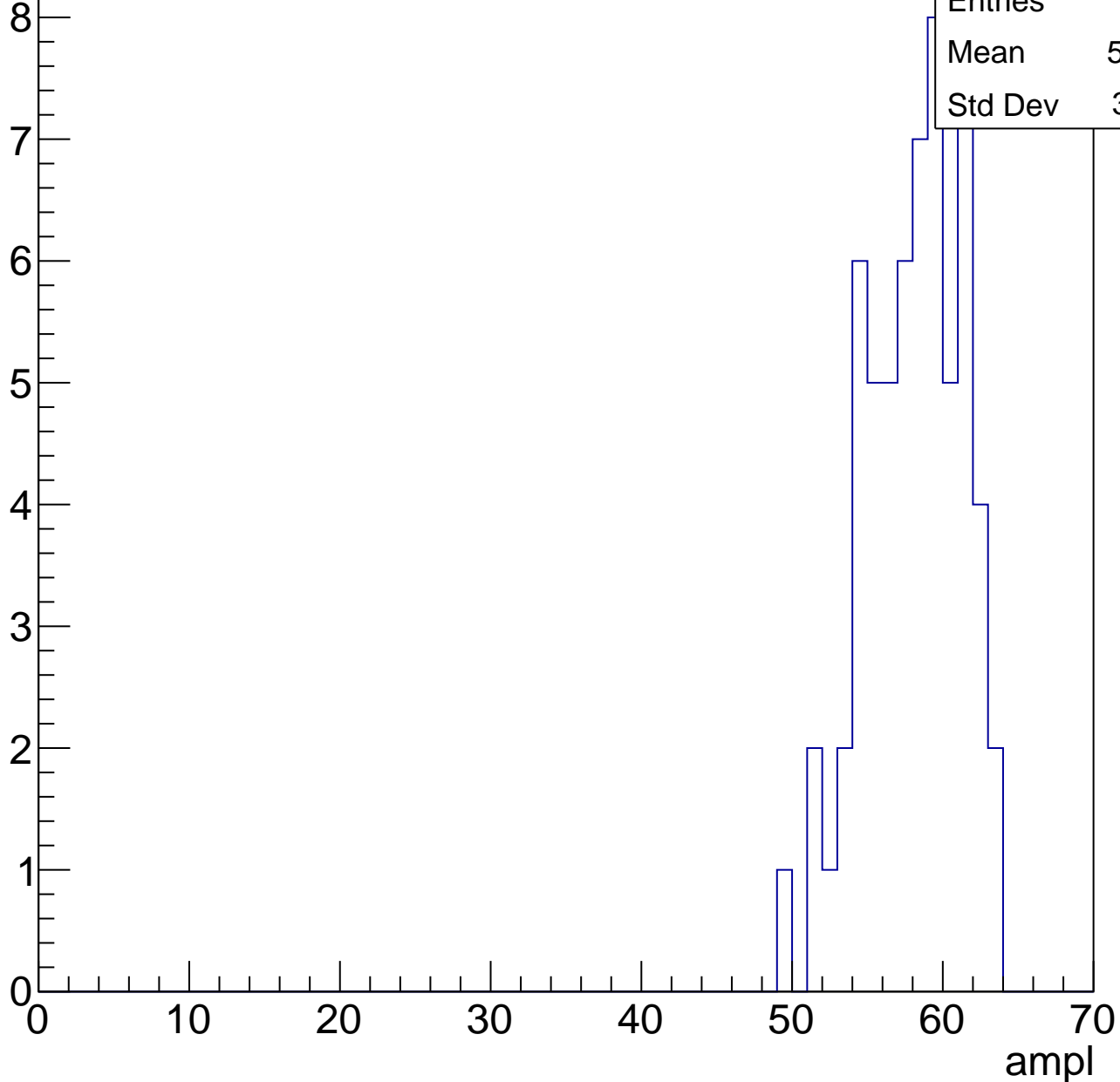


# B0L001S, U21-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	57.58
Std Dev	3.201

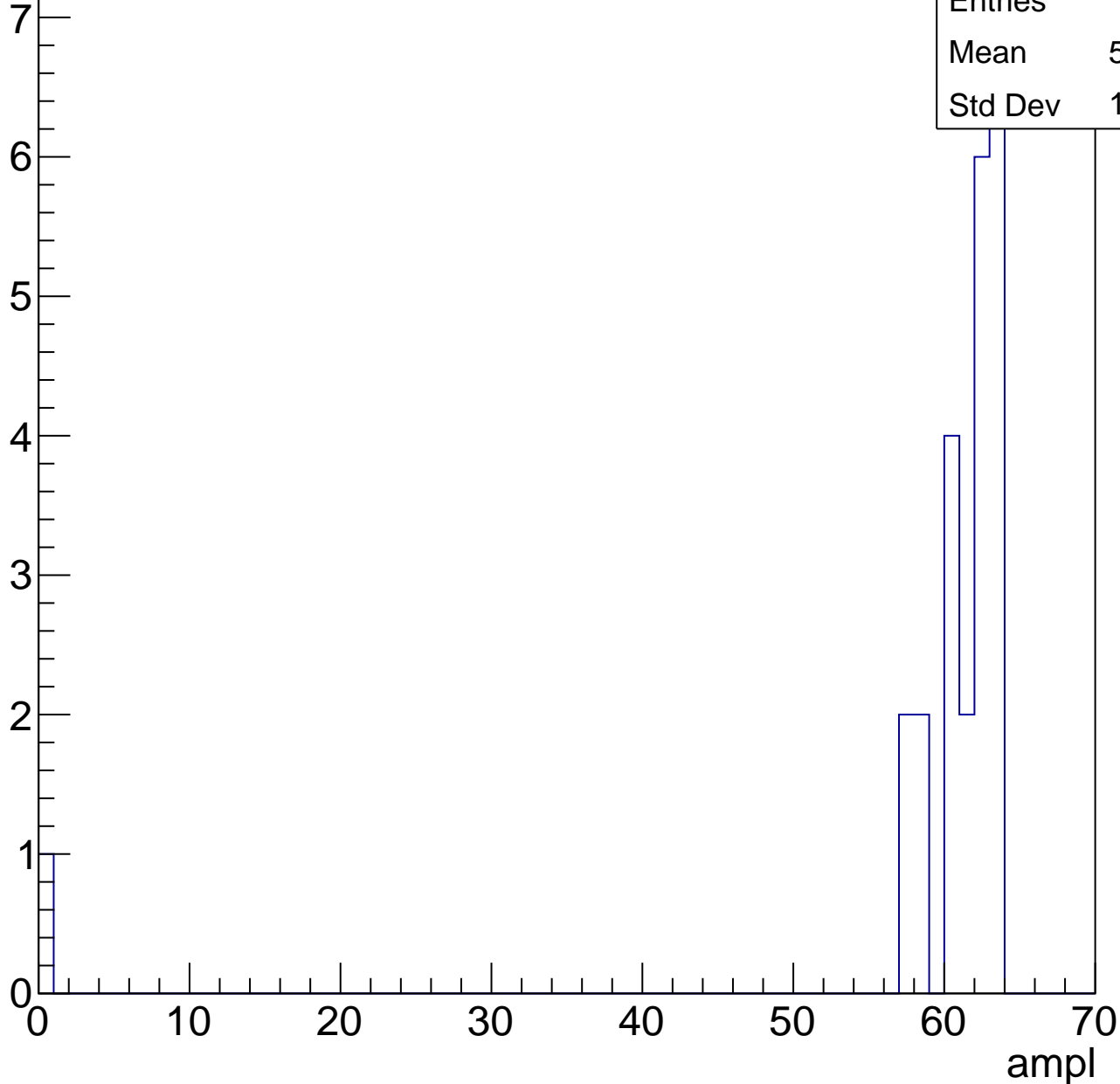


# B0L001S, U21-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	24
Mean	58.54
Std Dev	12.36



# B0L001S, U21-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0



# B0L001S, U21-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0

# B0L001S, U21-ch118, adc0

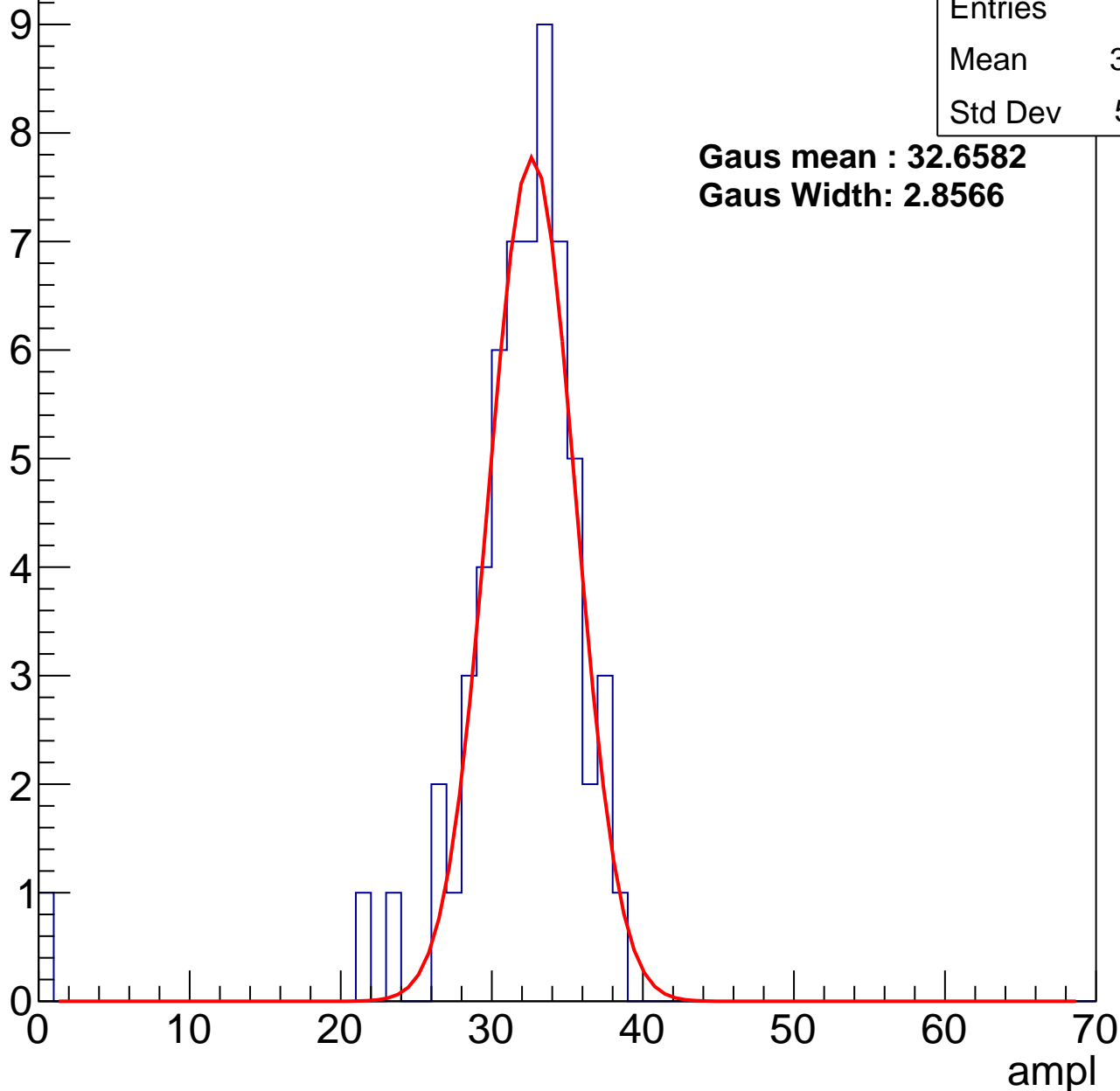
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	31.25
Std Dev	5.211

**Gaus mean : 32.6582**

**Gaus Width: 2.8566**



# B0L001S, U21-ch118, adc1

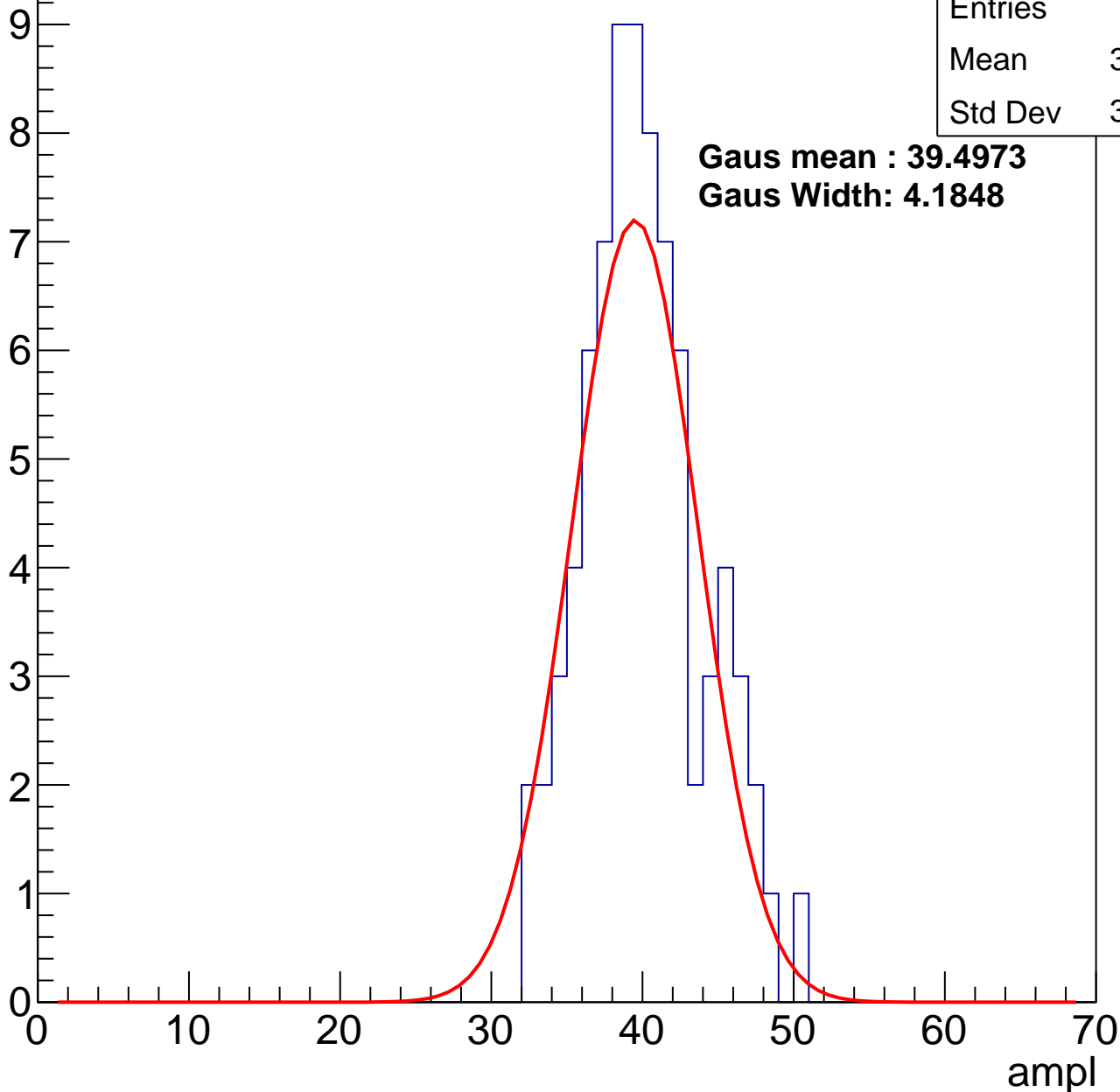
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	79
Mean	39.58
Std Dev	3.883

**Gaus mean : 39.4973**

**Gaus Width: 4.1848**



# B0L001S, U21-ch118, adc2

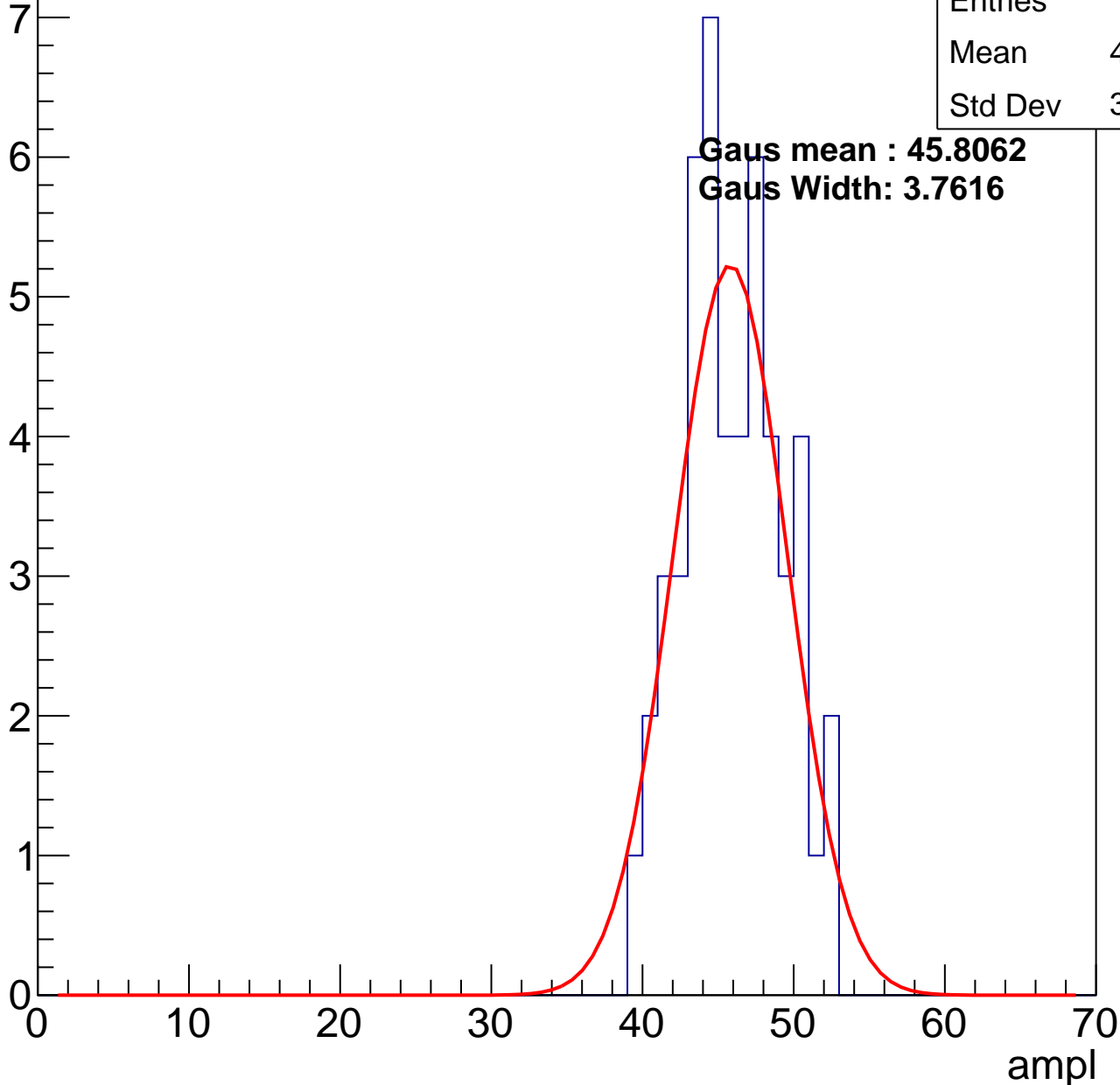
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	50
Mean	45.48
Std Dev	3.245

**Gaus mean : 45.8062**

**Gaus Width: 3.7616**

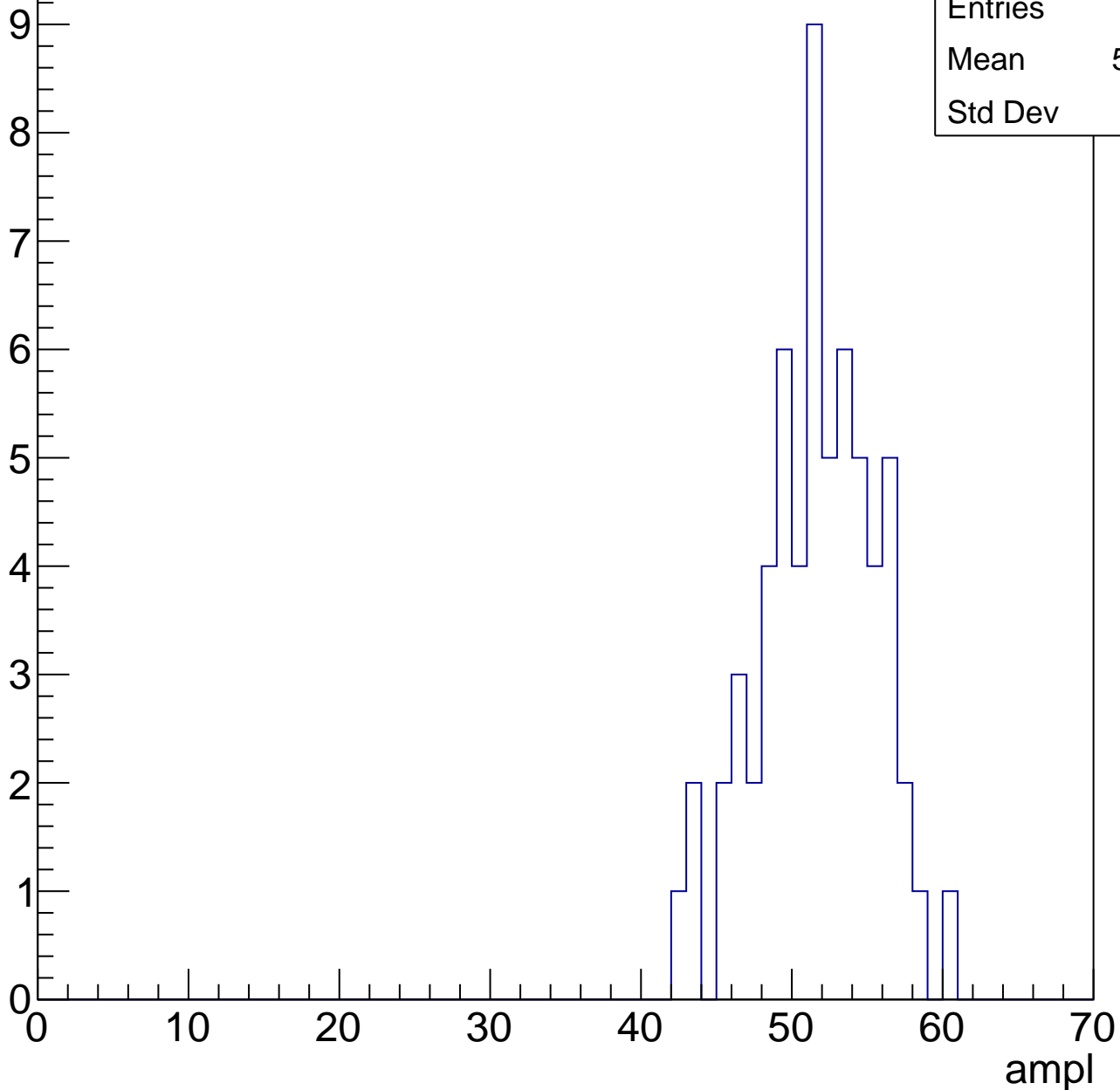


# B0L001S, U21-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	51.21
Std Dev	3.84

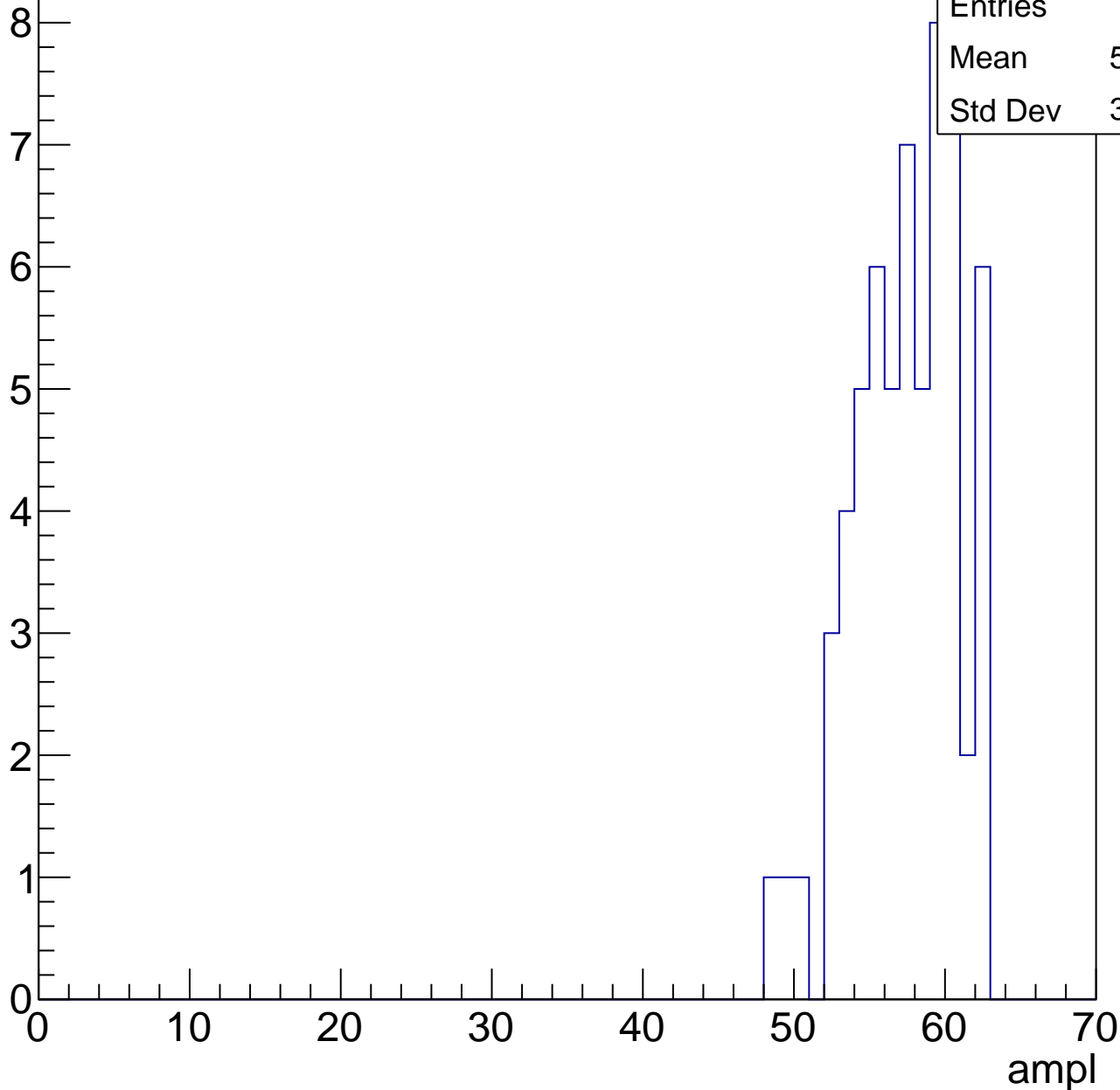


# B0L001S, U21-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	56.94
Std Dev	3.355

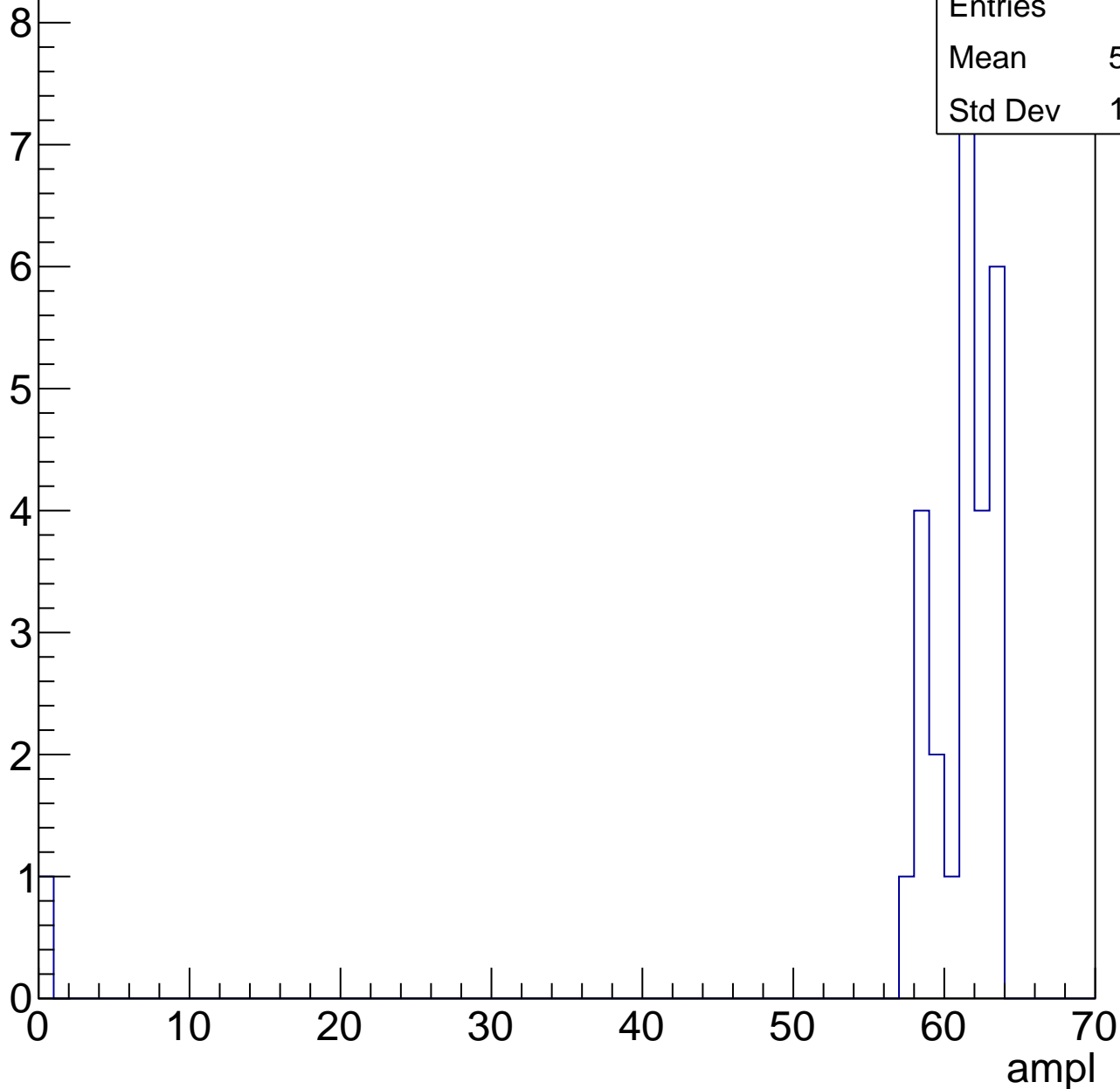


# B0L001S, U21-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

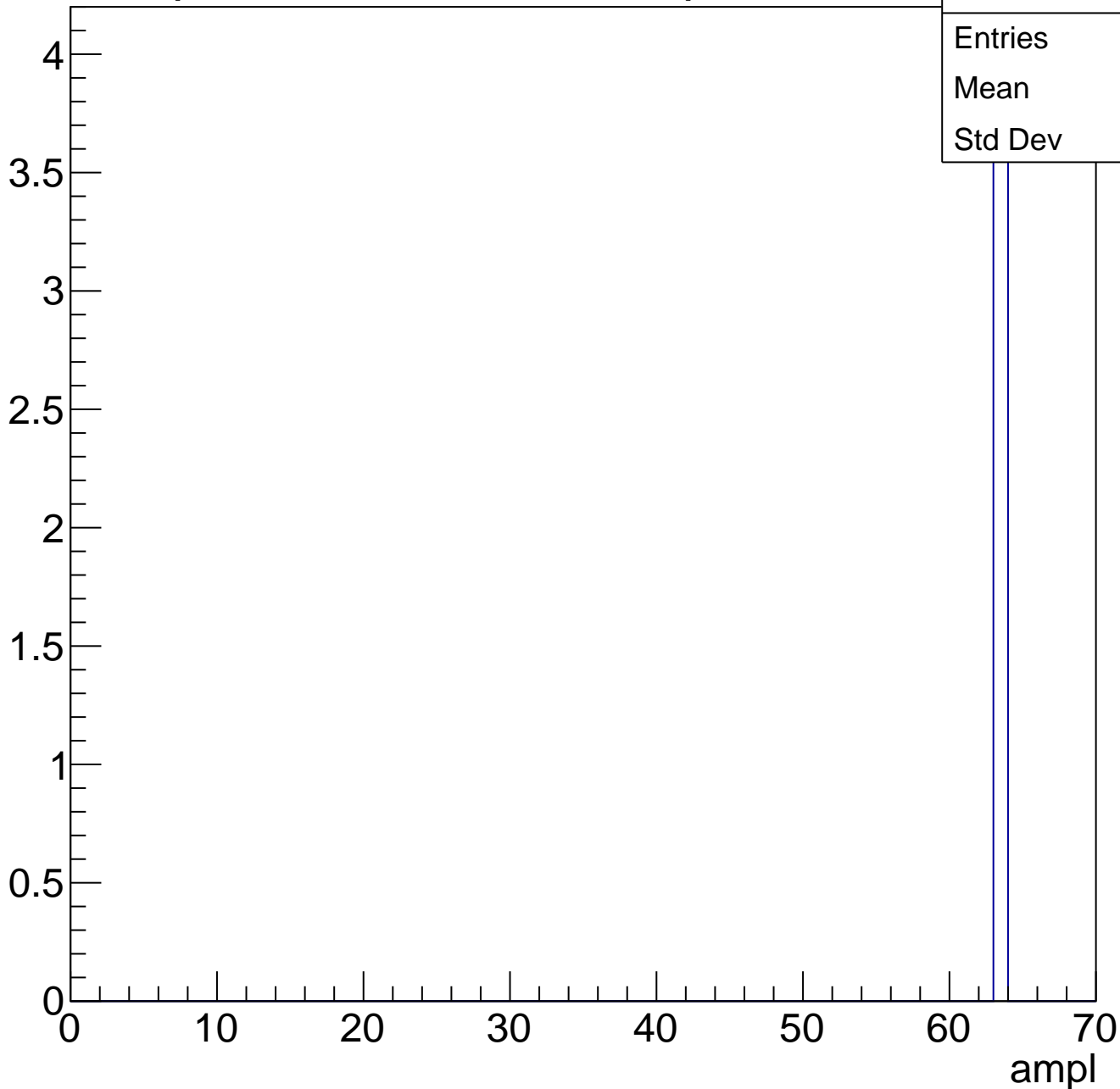
Entries	27
Mean	58.56
Std Dev	11.62



# B0L001S, U21-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	4
Mean	63
Std Dev	0



# B0L001S, U21-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U21-ch119, adc0

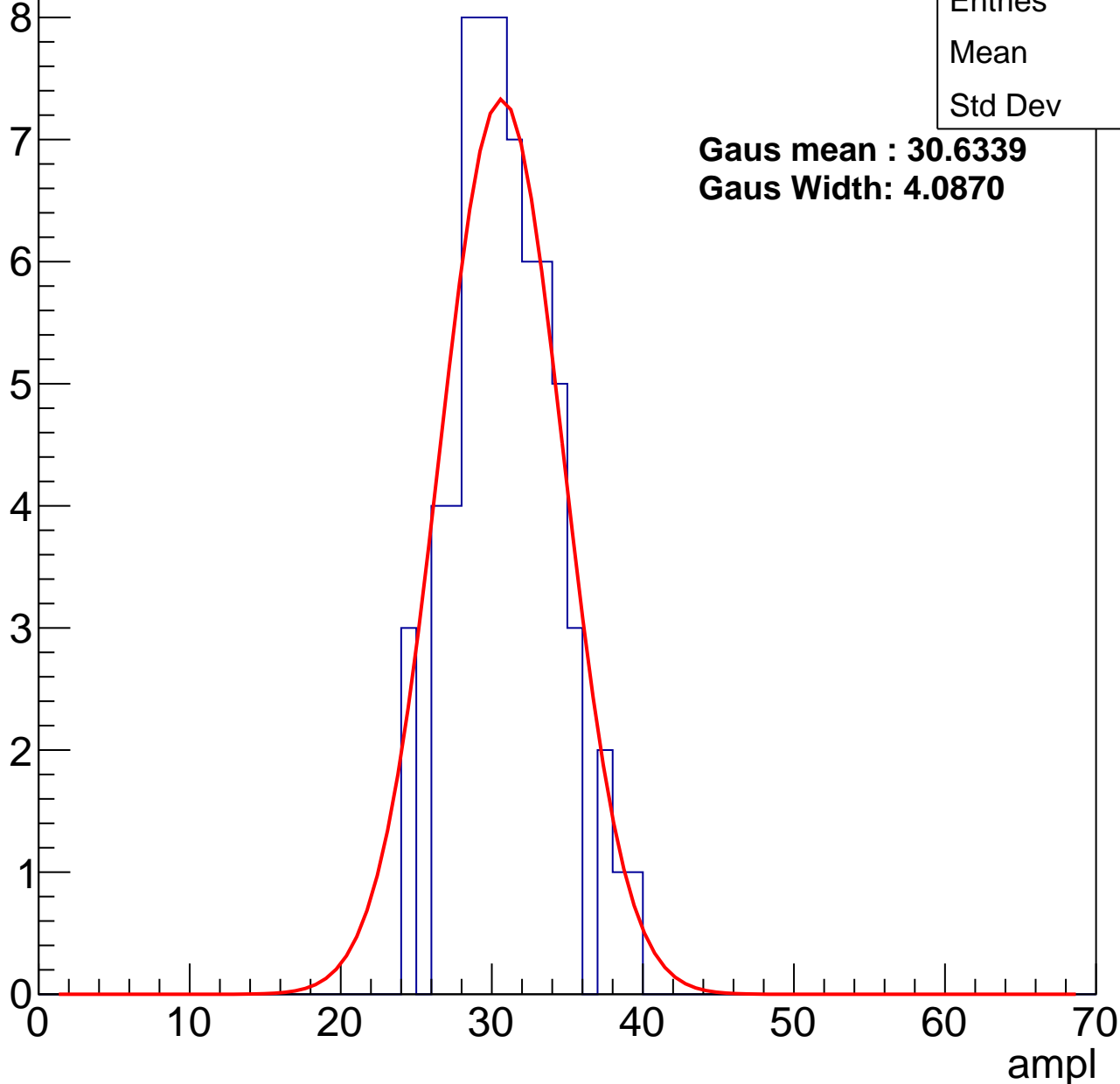
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	30.5
Std Dev	3.29

**Gaus mean : 30.6339**

**Gaus Width: 4.0870**



# B0L001S, U21-ch119, adc1

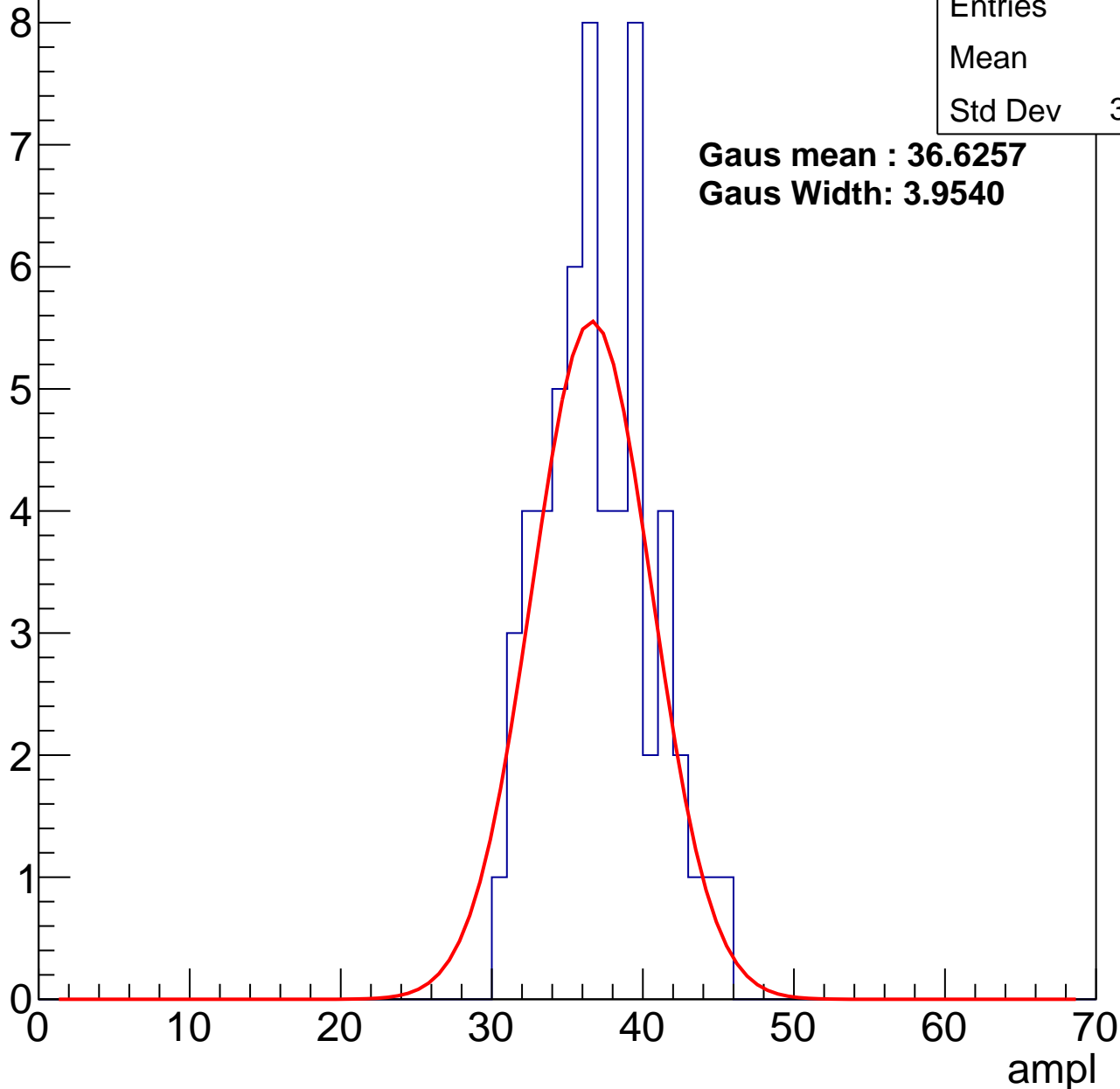
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	36.6
Std Dev	3.489

**Gaus mean : 36.6257**

**Gaus Width: 3.9540**



# B0L001S, U21-ch119, adc2

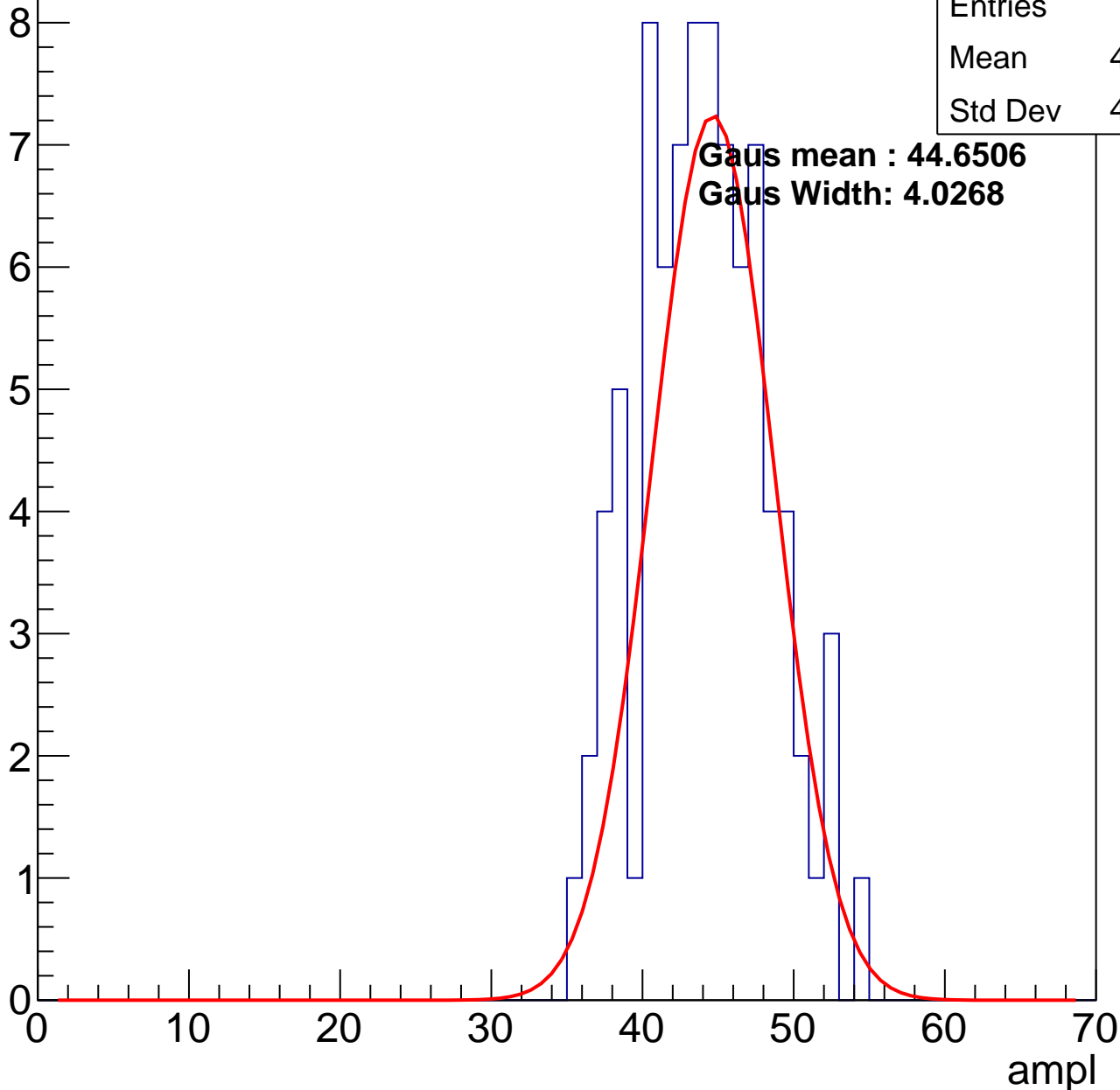
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	85
Mean	43.64
Std Dev	4.184

**Gaus mean : 44.6506**

**Gaus Width: 4.0268**

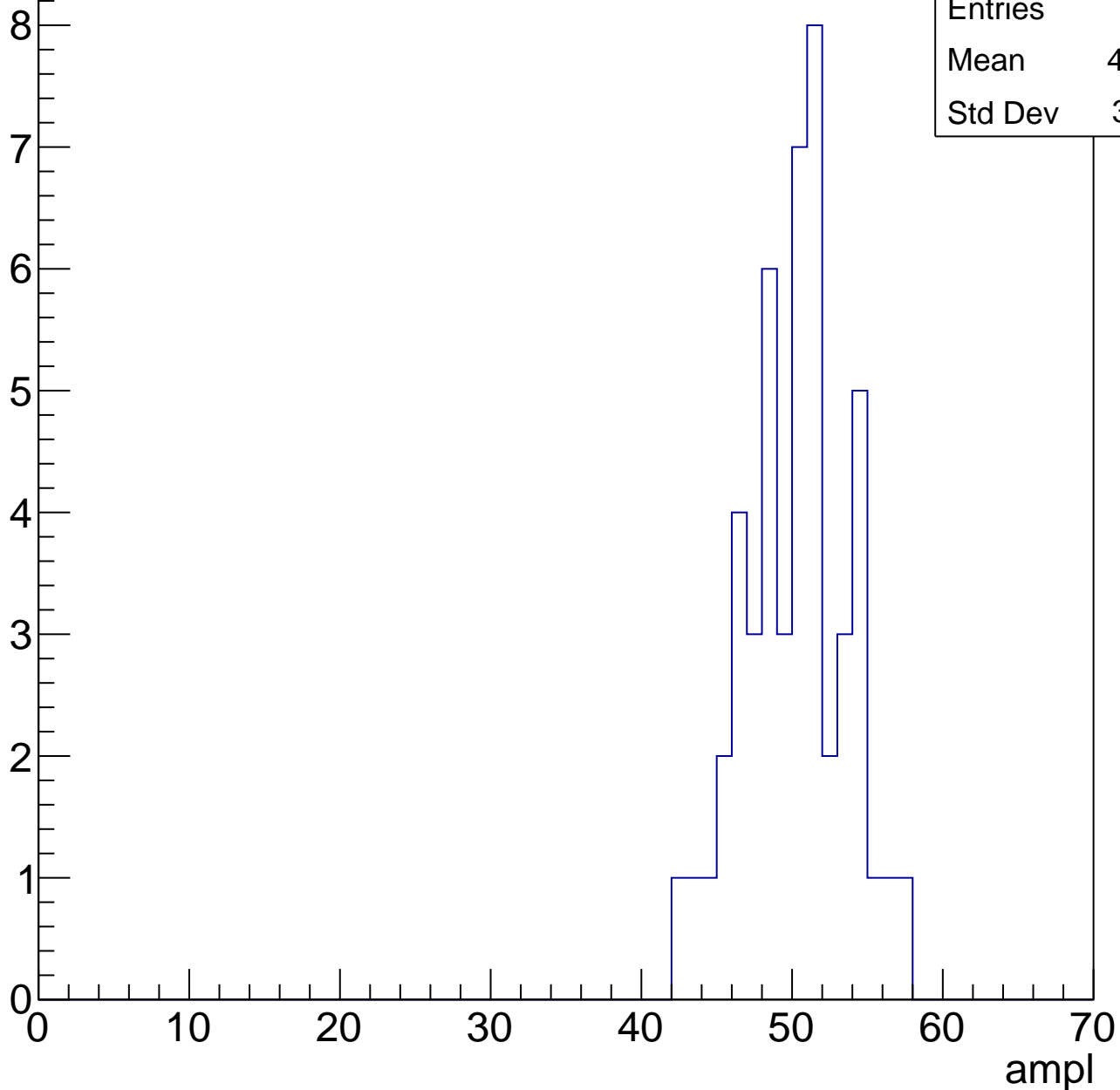


# B0L001S, U21-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

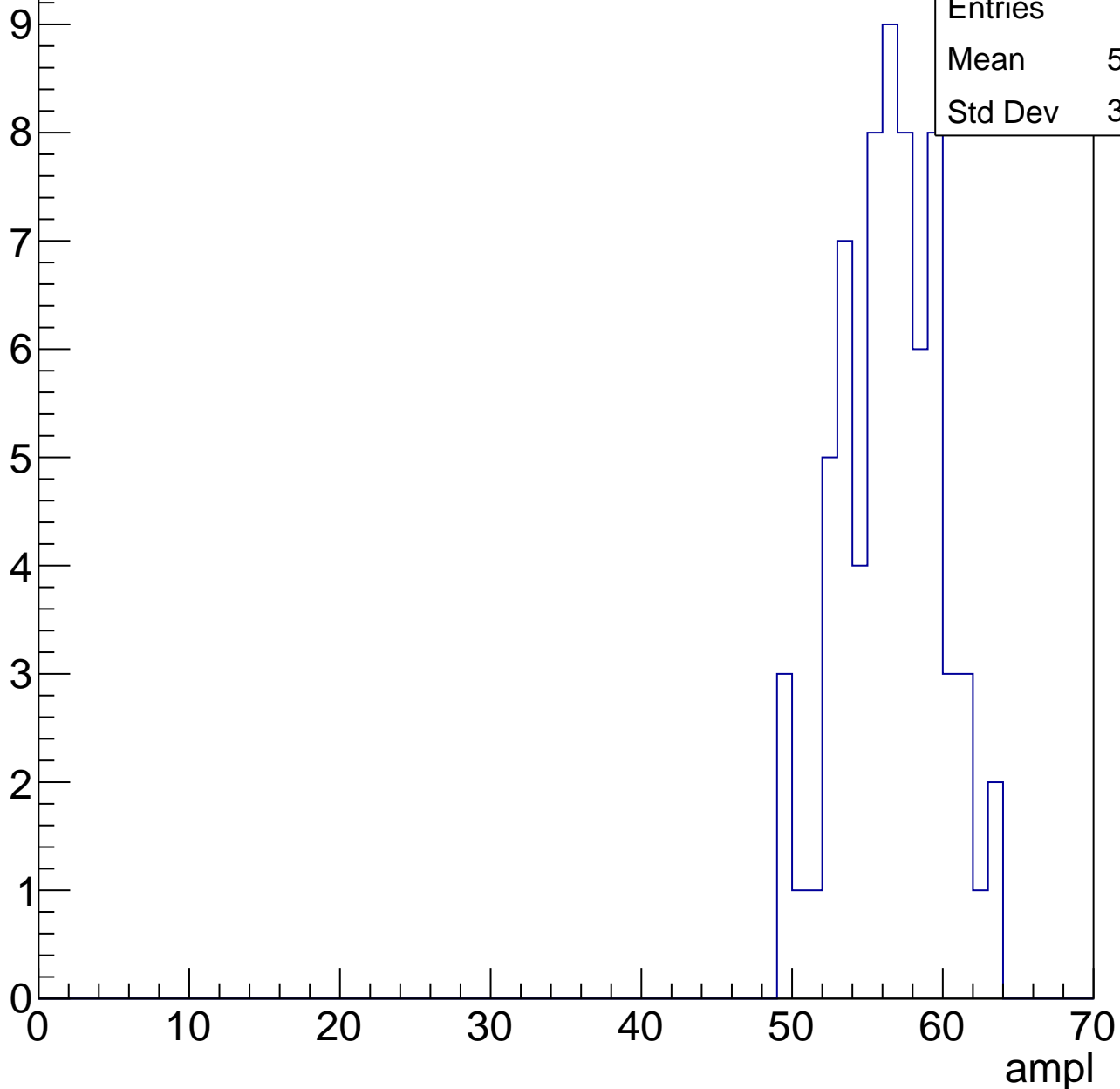
Entries	49
Mean	49.76
Std Dev	3.341



# B0L001S, U21-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



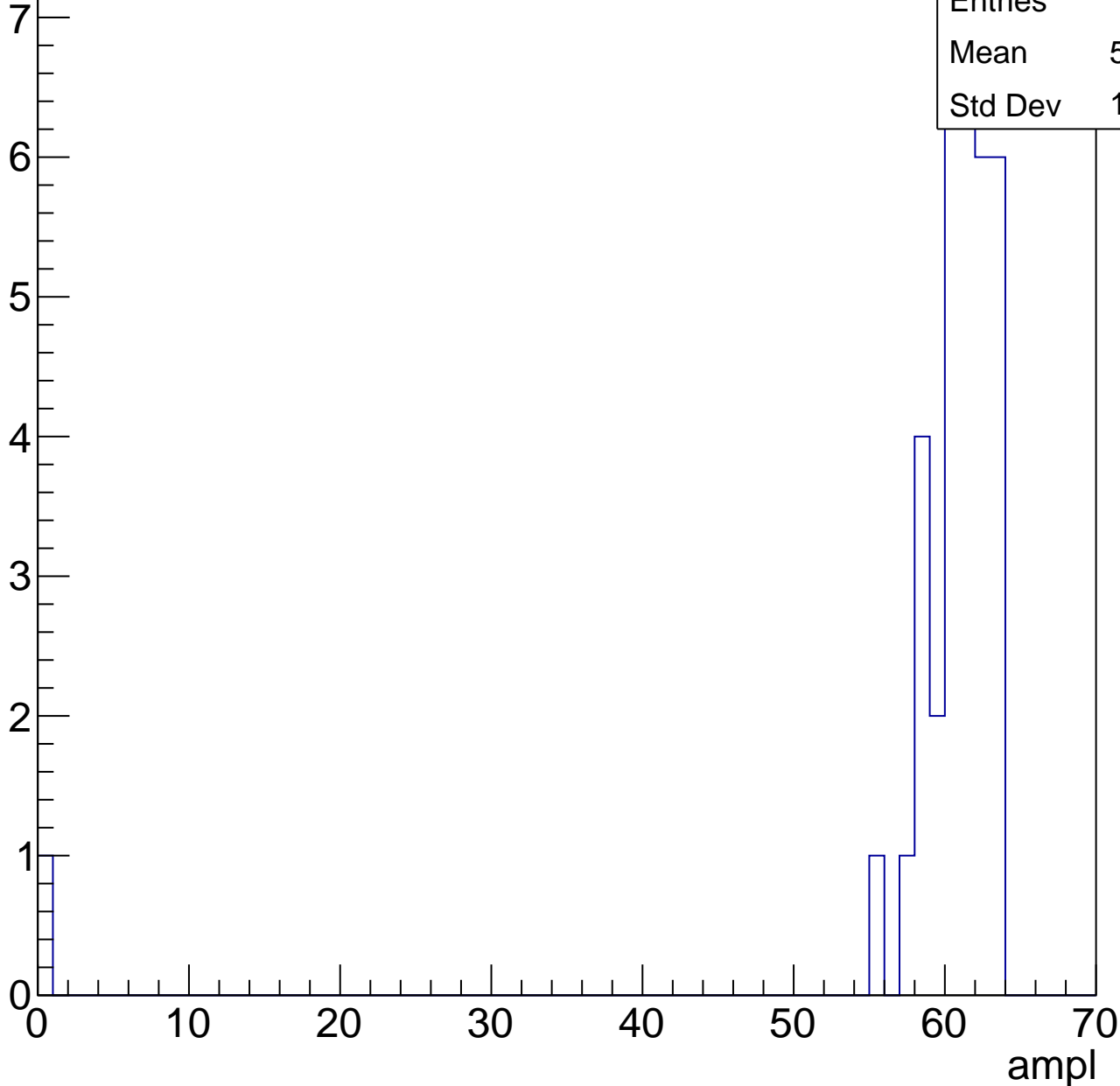
Entries	69
Mean	56.03
Std Dev	3.266

# B0L001S, U21-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	35
Mean	58.83
Std Dev	10.27



# B0L001S, U21-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch119, adc7

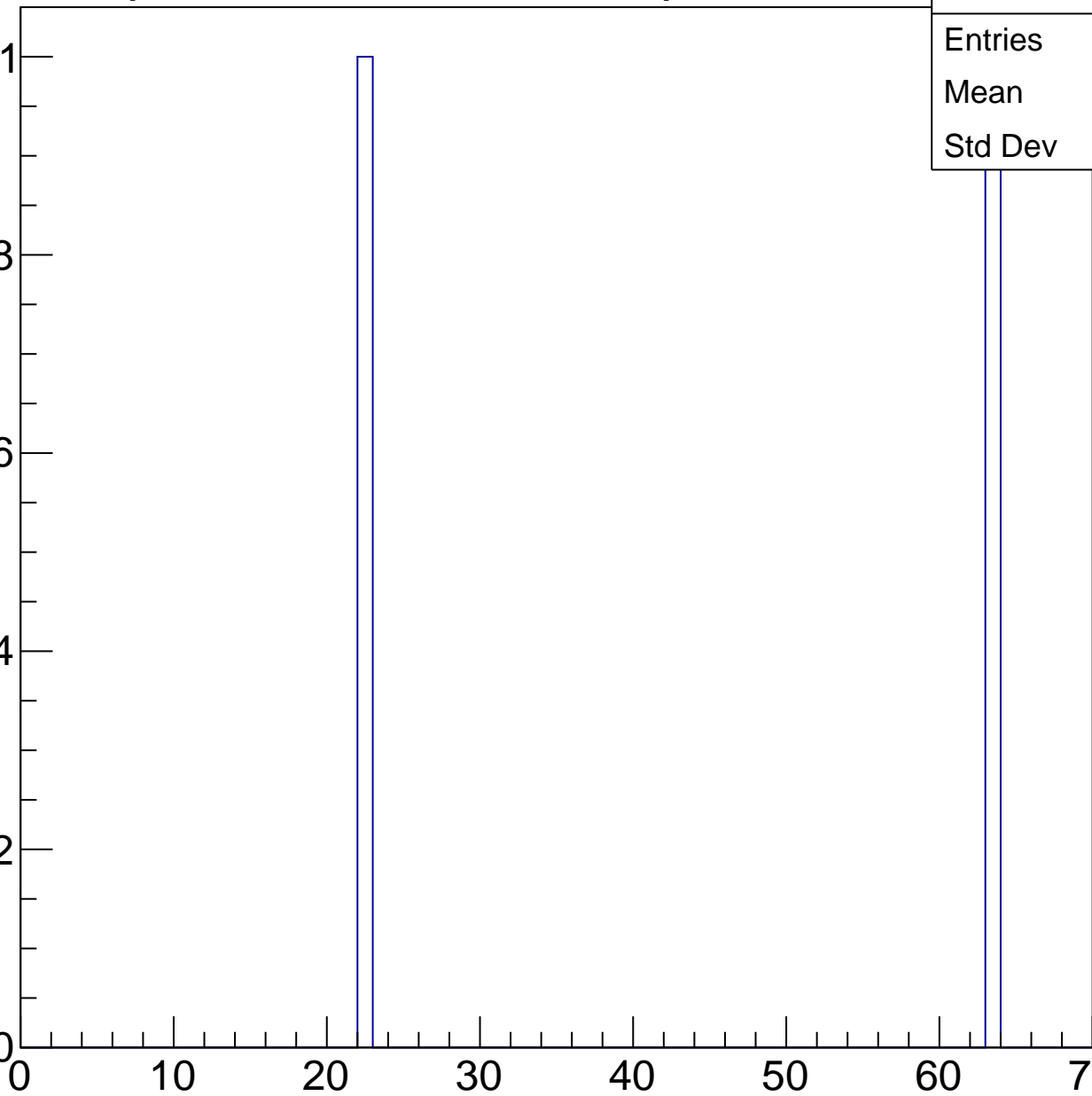
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	42.5
Std Dev	20.5

ampl



# B0L001S, U21-ch120, adc0

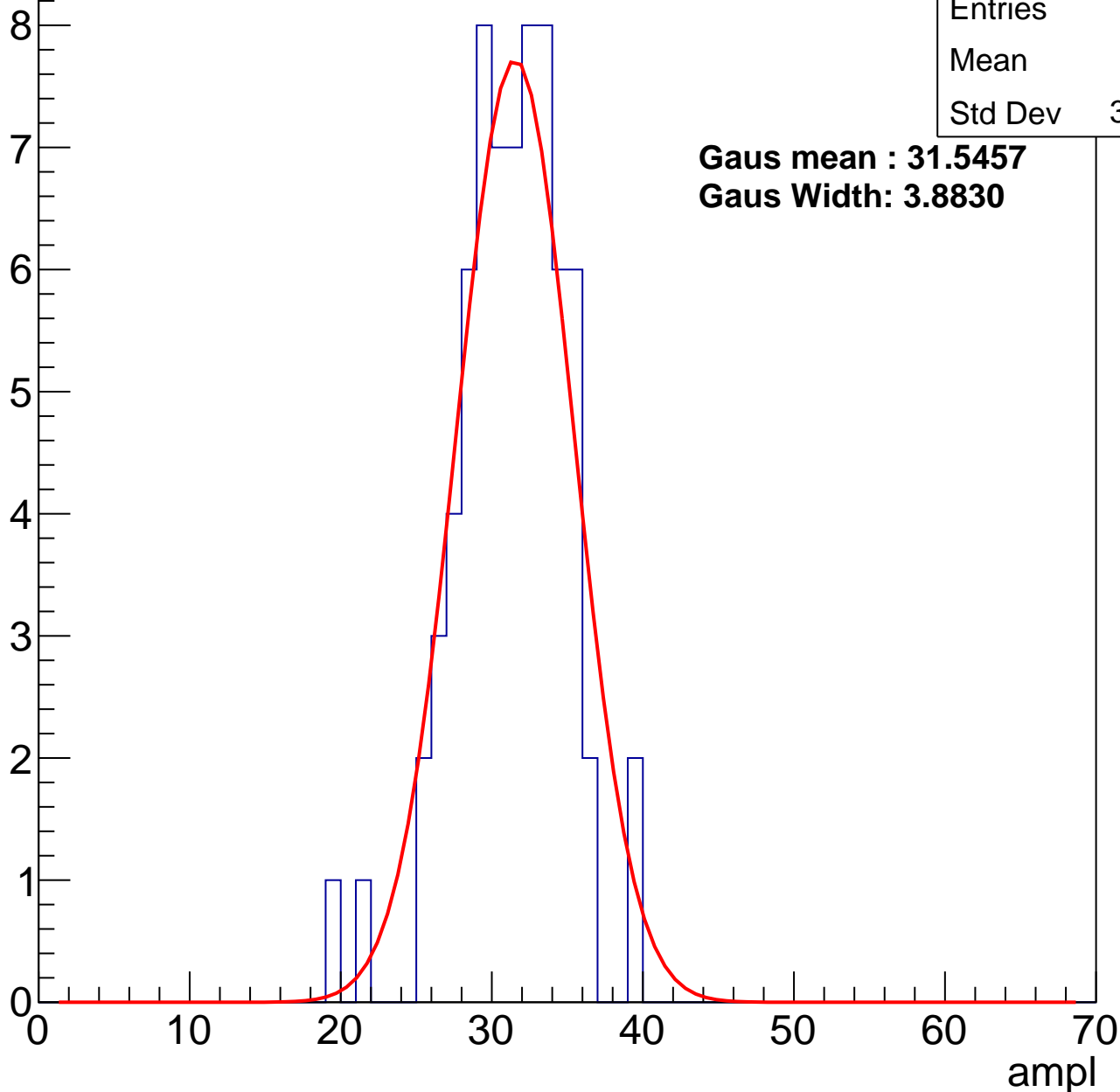
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	71
Mean	30.8
Std Dev	3.586

**Gaus mean : 31.5457**

**Gaus Width: 3.8830**



# B0L001S, U21-ch120, adc1

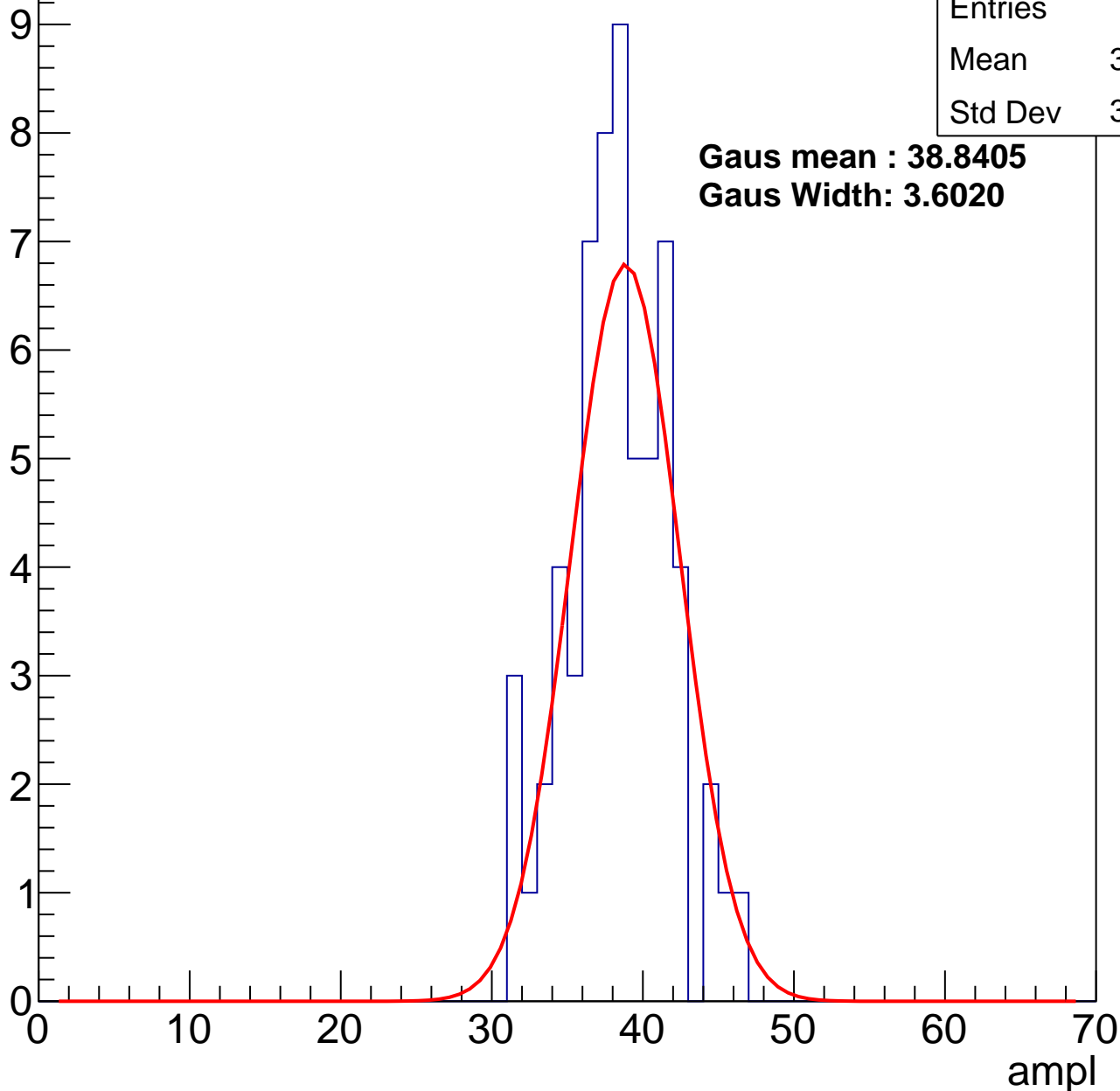
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	37.92
Std Dev	3.352

**Gaus mean : 38.8405**

**Gaus Width: 3.6020**



# B0L001S, U21-ch120, adc2

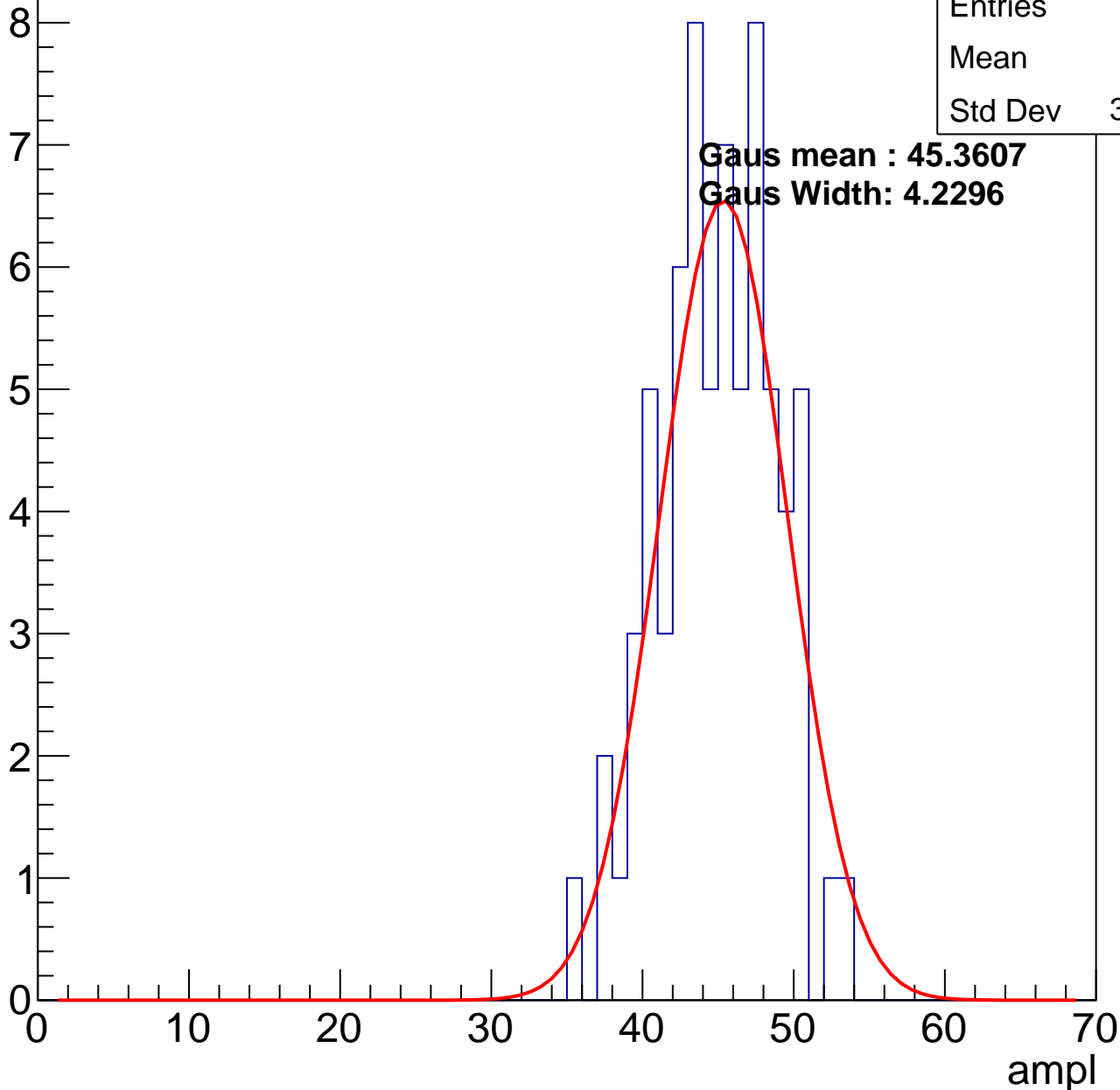
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	44.5
Std Dev	3.809

**Gaus mean : 45.3607**

**Gaus Width: 4.2296**

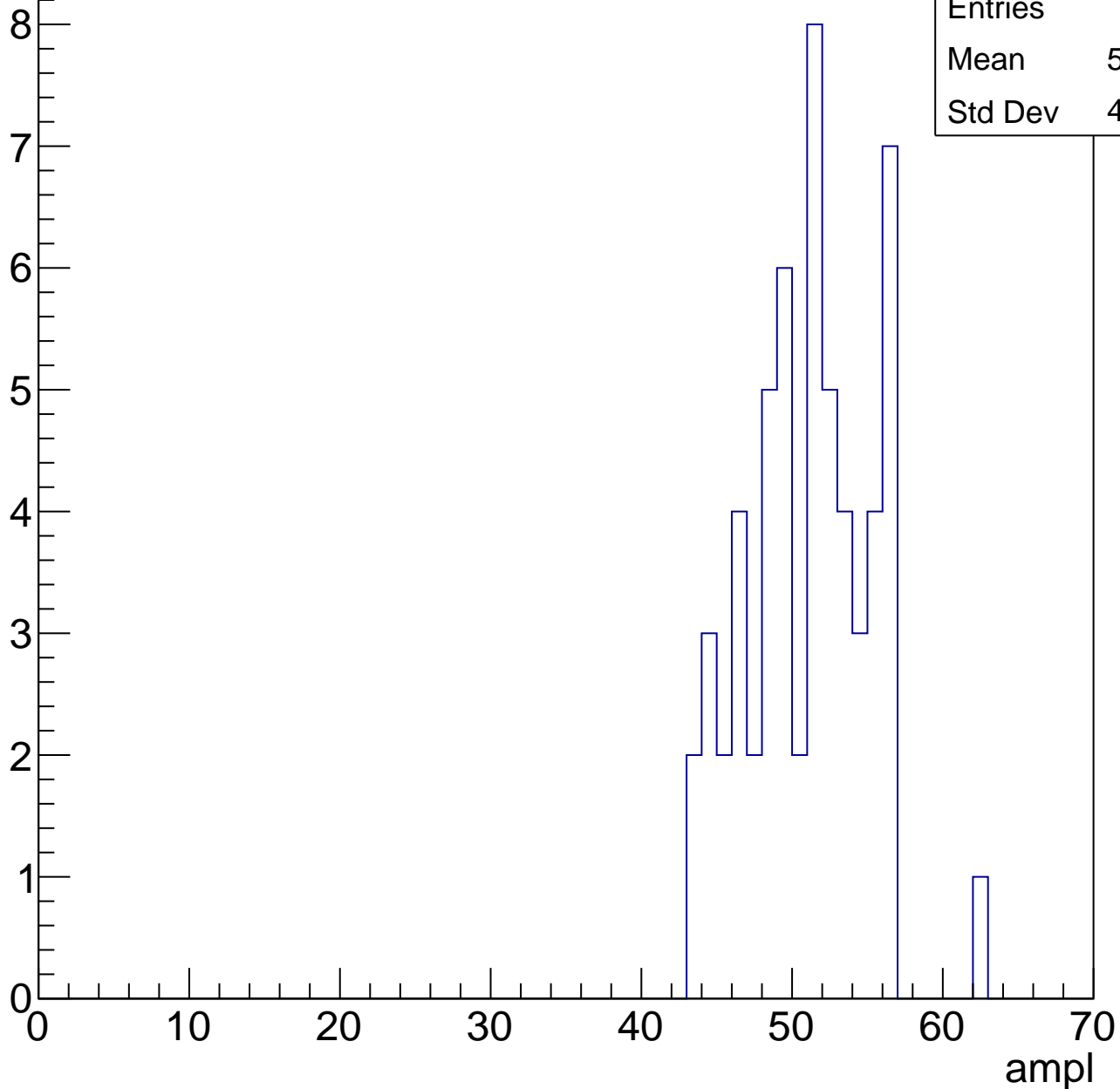


# B0L001S, U21-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	50.62
Std Dev	4.046

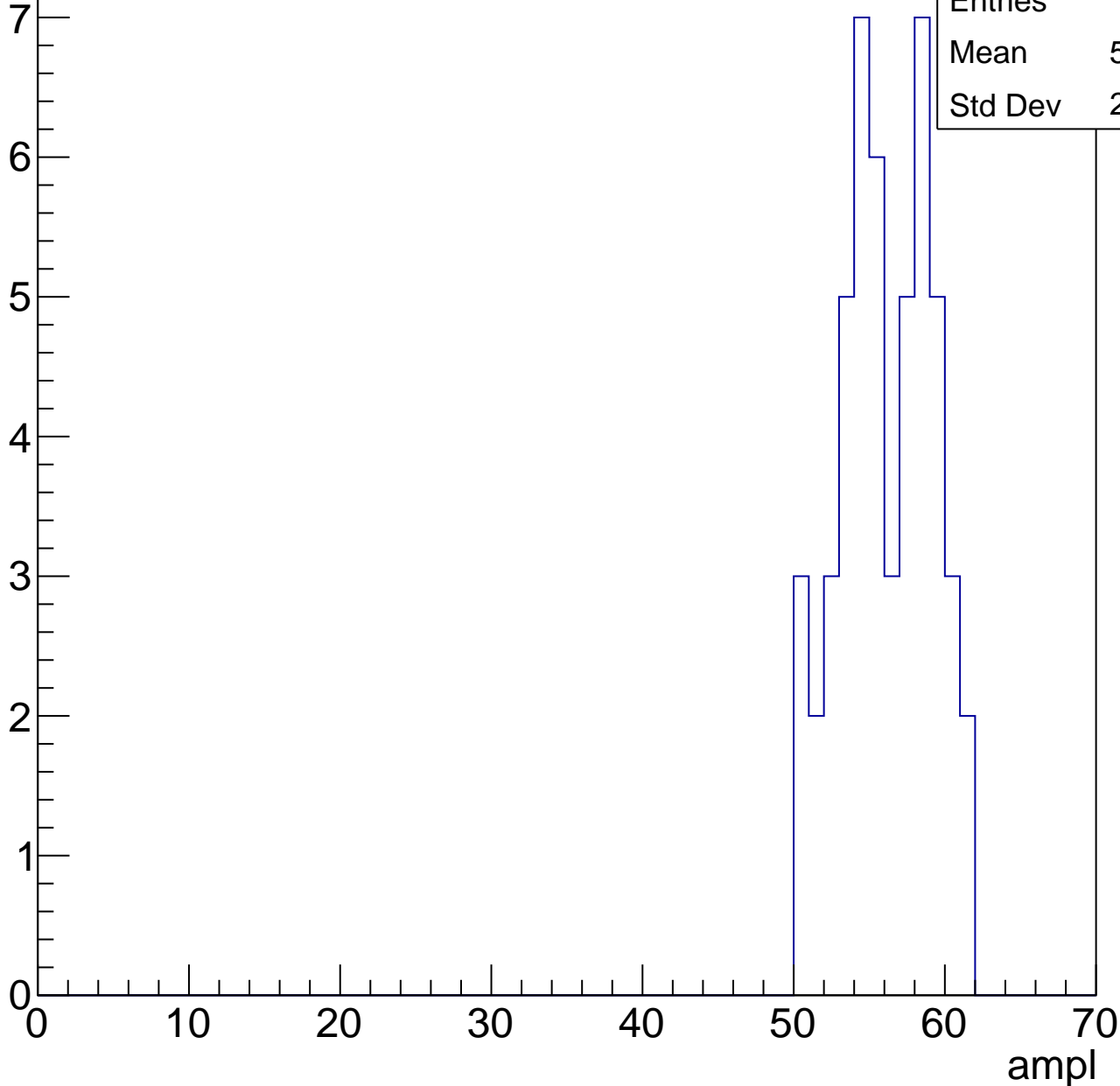


# B0L001S, U21-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	55.63
Std Dev	2.983



# B0L001S, U21-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

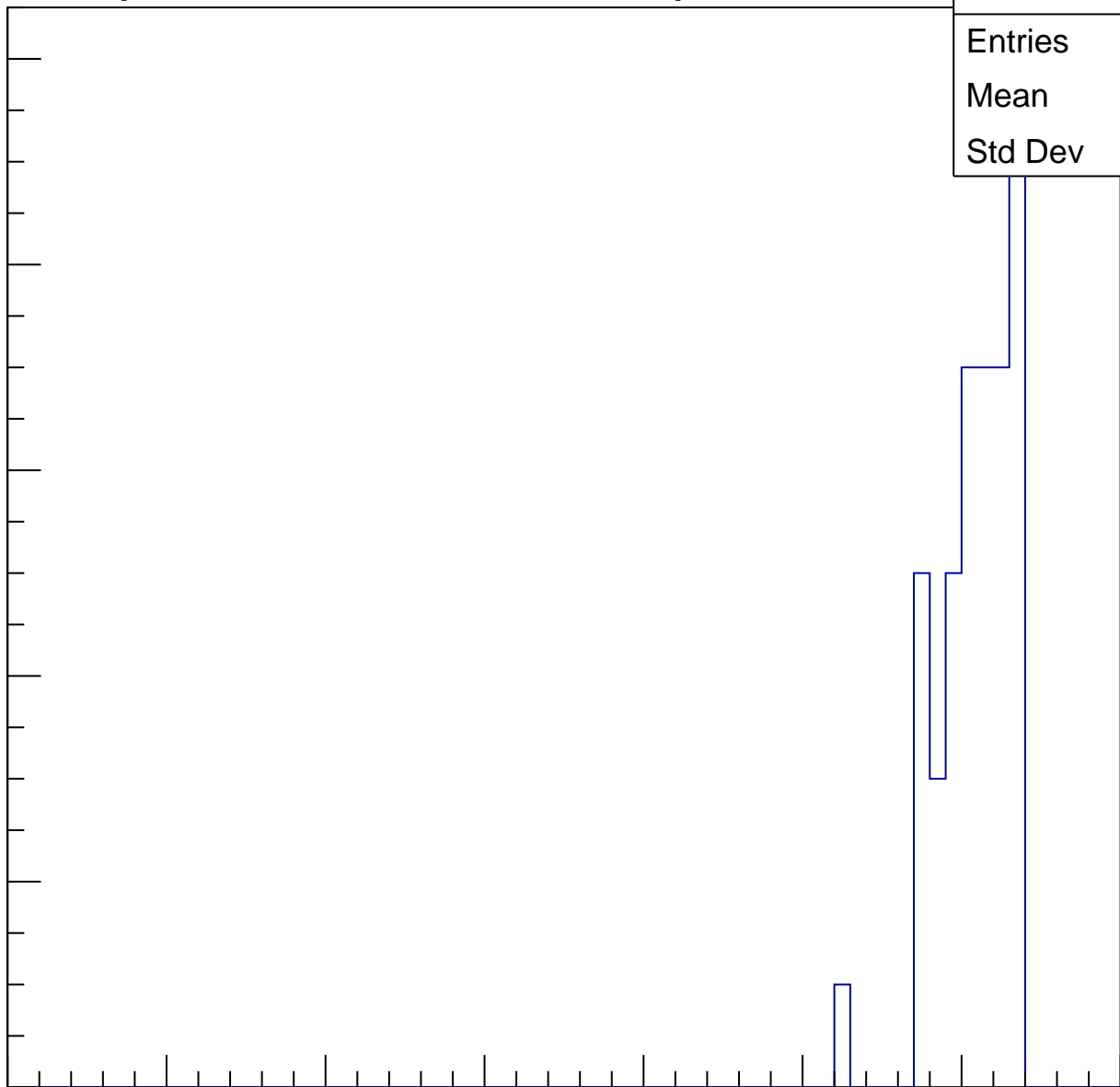
Entries	45
Mean	60.38
Std Dev	2.331

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

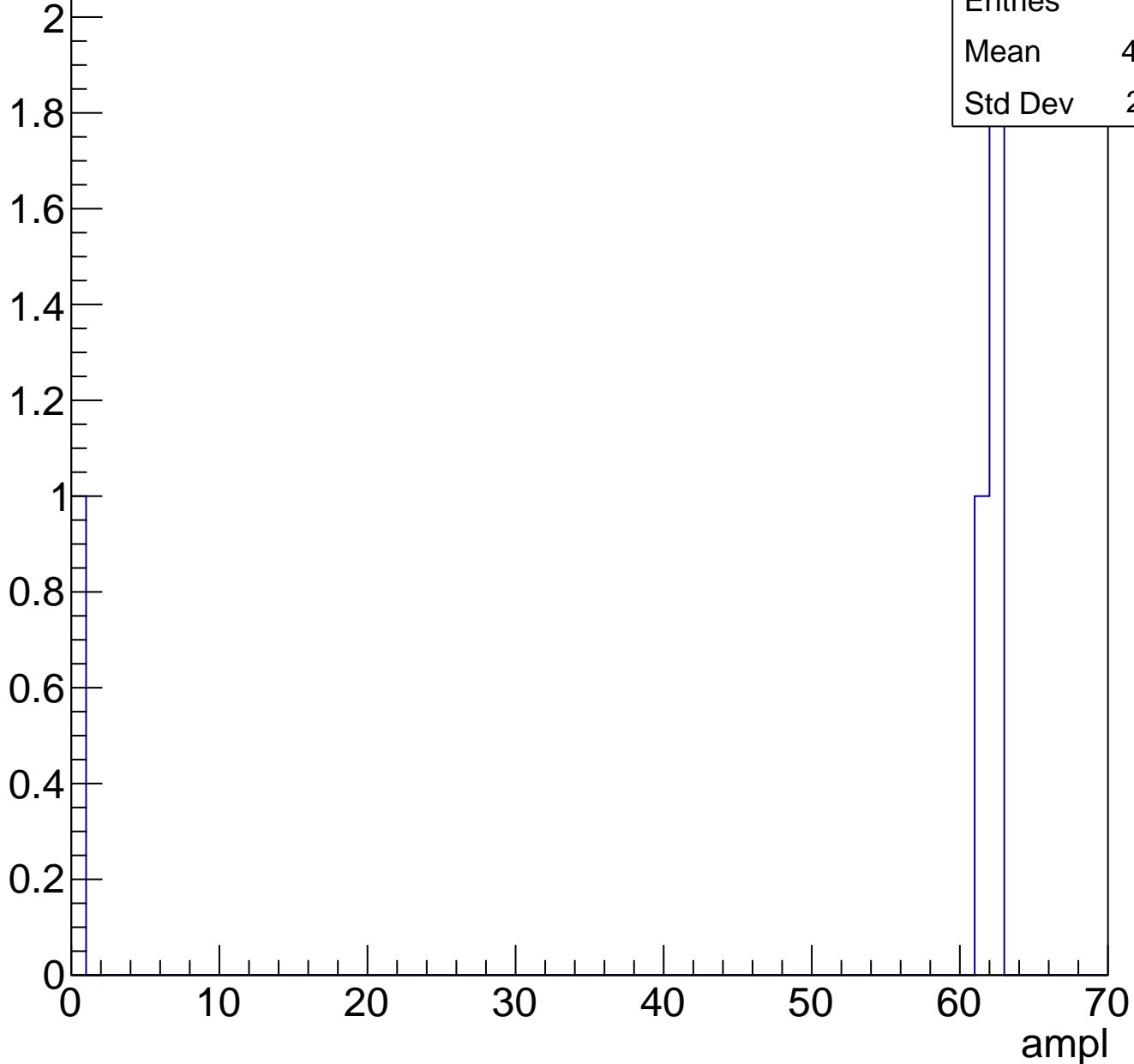
ampl



# B0L001S, U21-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch121, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	90
Mean	30.11
Std Dev	4.023

**Gaus mean : 30.4343**

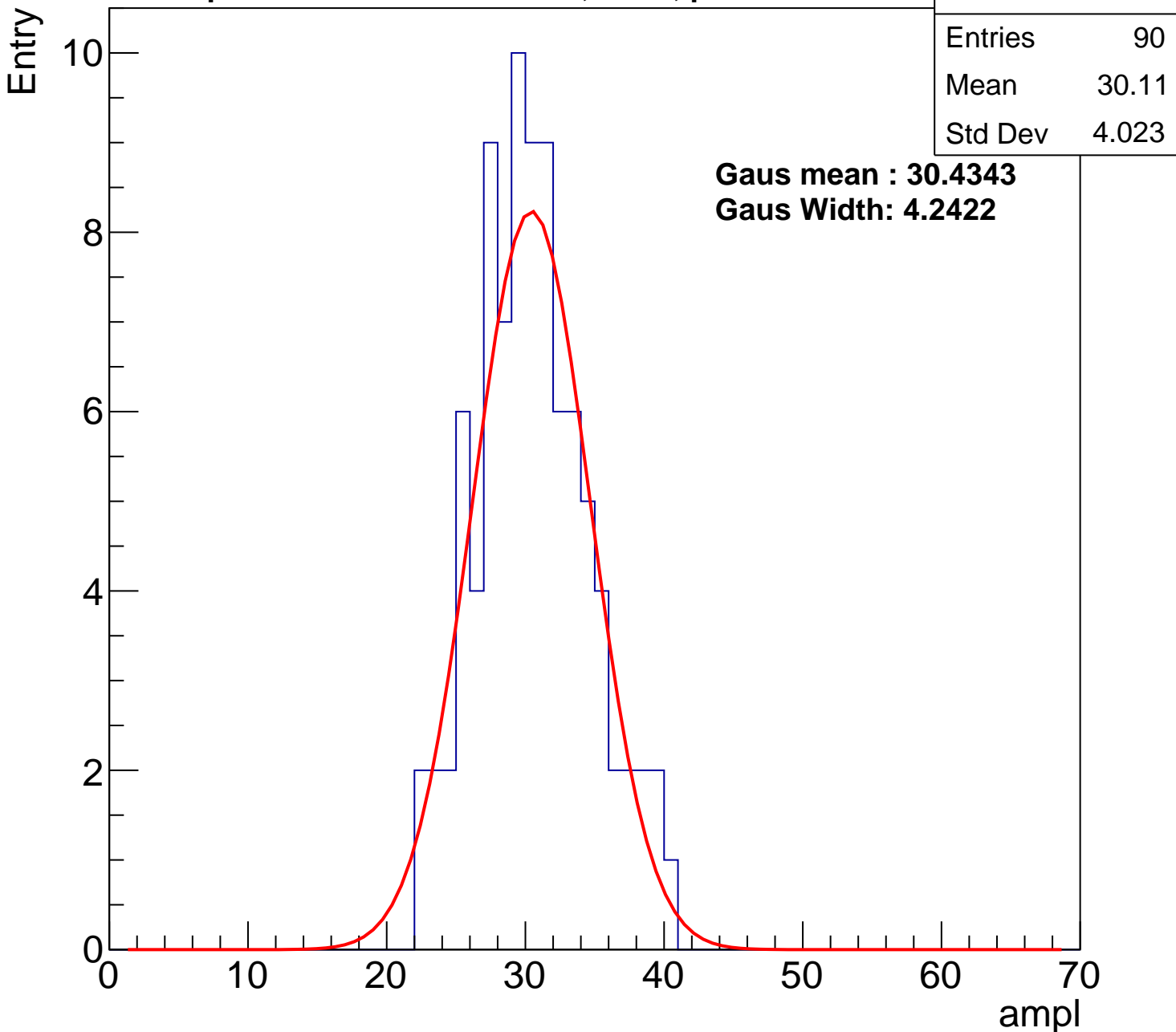
**Gaus Width: 4.2422**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U21-ch121, adc1

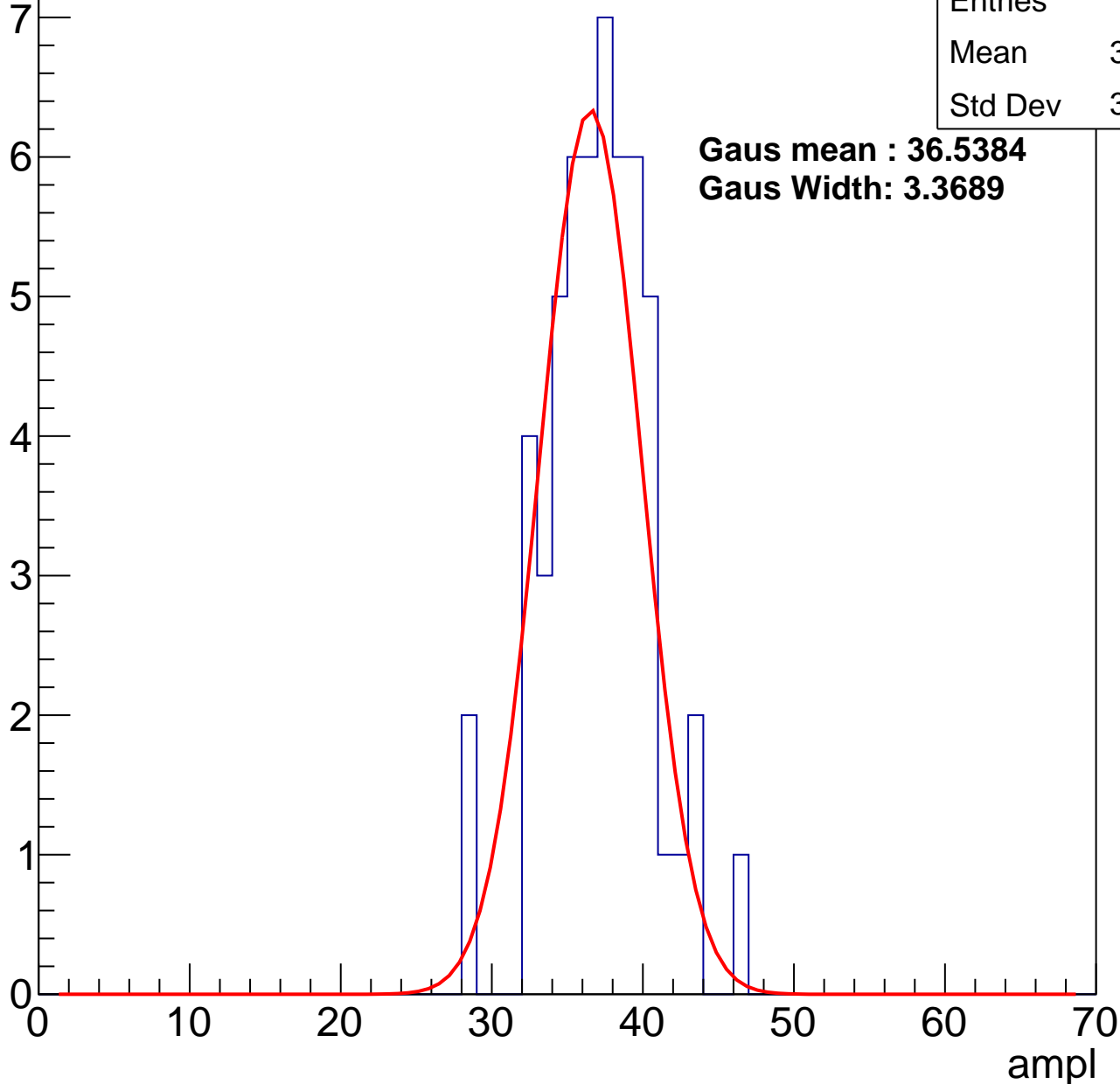
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	55
Mean	36.64
Std Dev	3.429

**Gaus mean : 36.5384**

**Gaus Width: 3.3689**



# B0L001S, U21-ch121, adc2

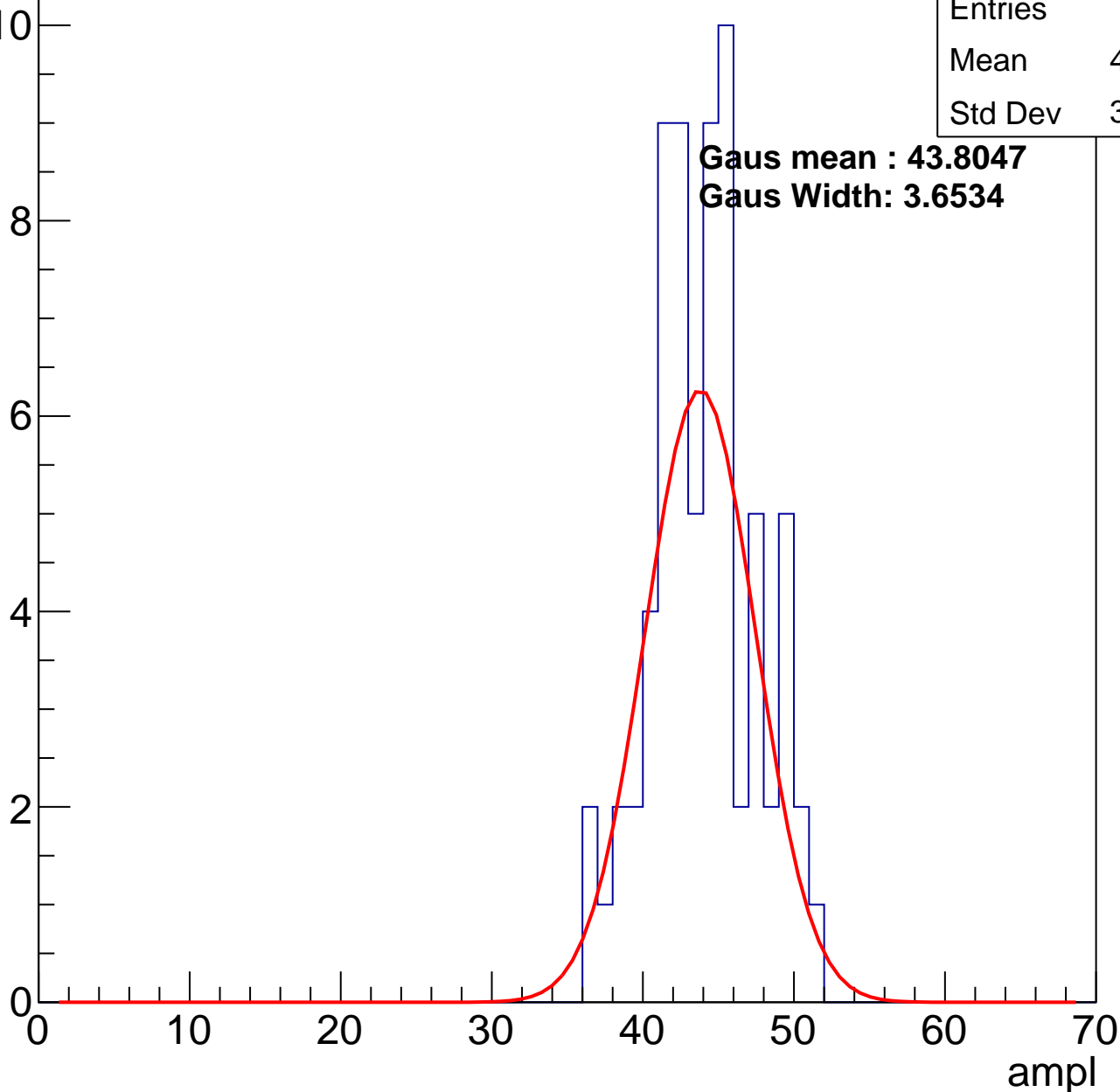
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	43.57
Std Dev	3.408

**Gaus mean : 43.8047**

**Gaus Width: 3.6534**

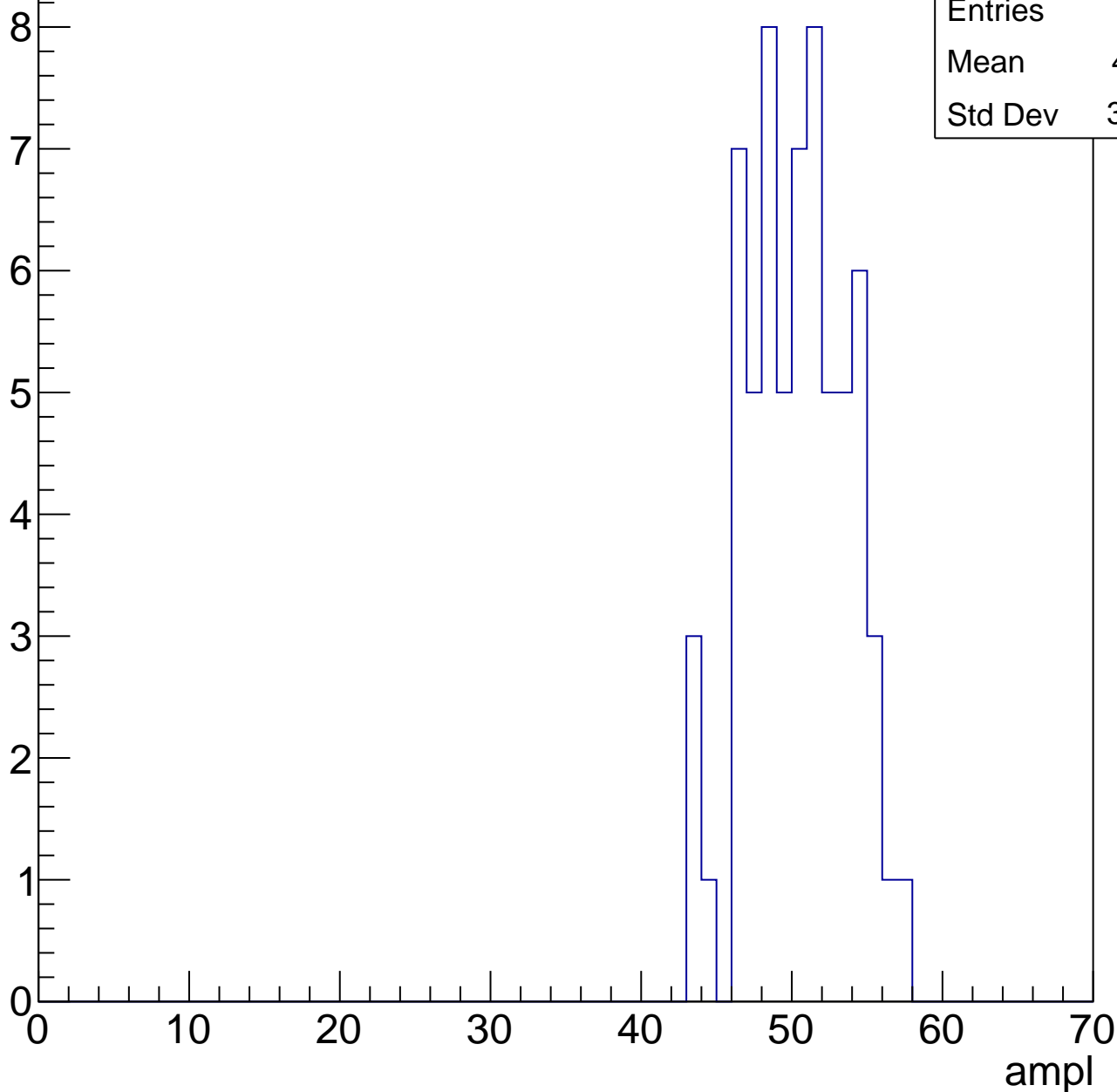


# B0L001S, U21-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	49.91
Std Dev	3.294

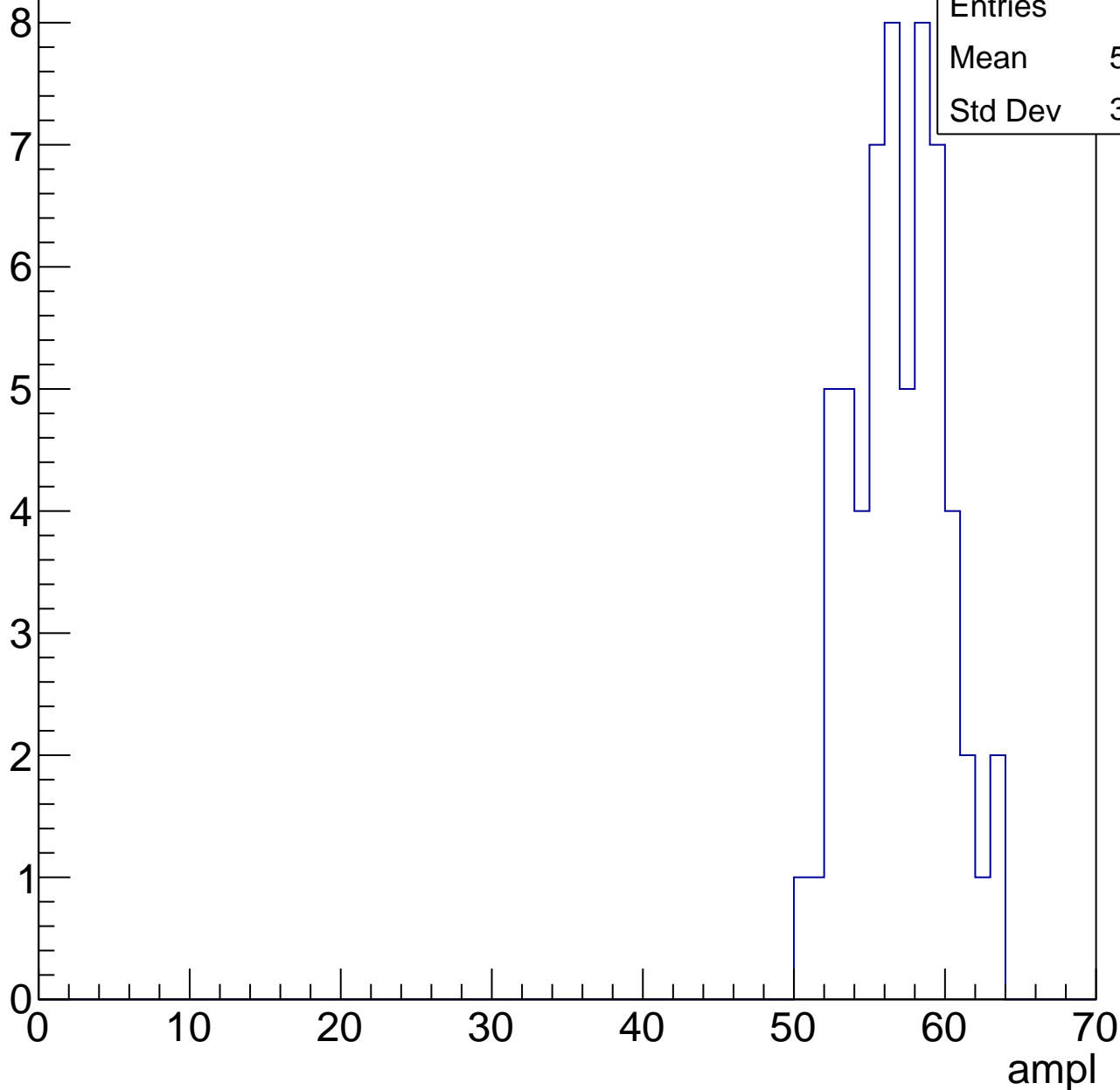


# B0L001S, U21-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	60
Mean	56.45
Std Dev	3.013

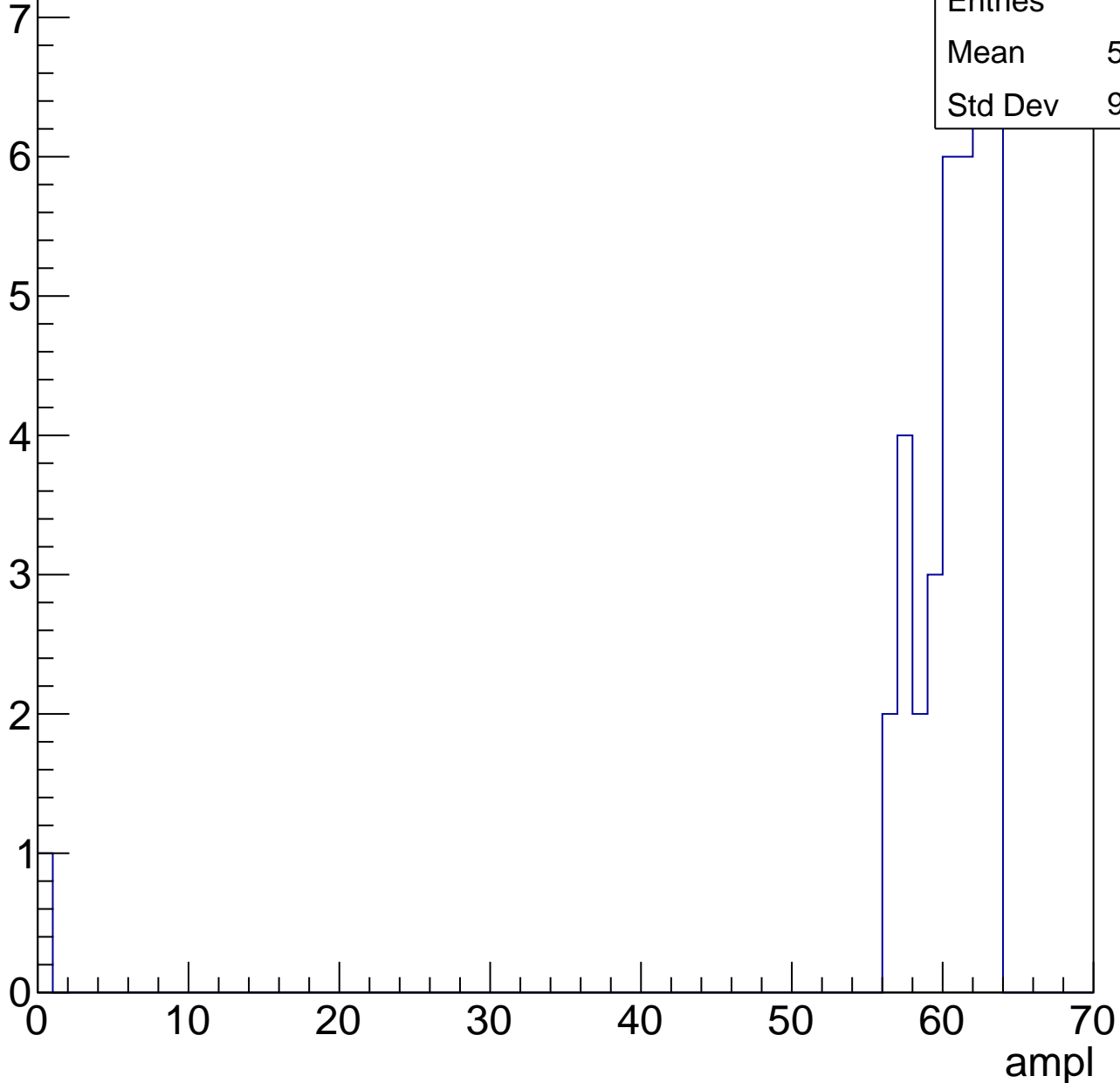


# B0L001S, U21-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

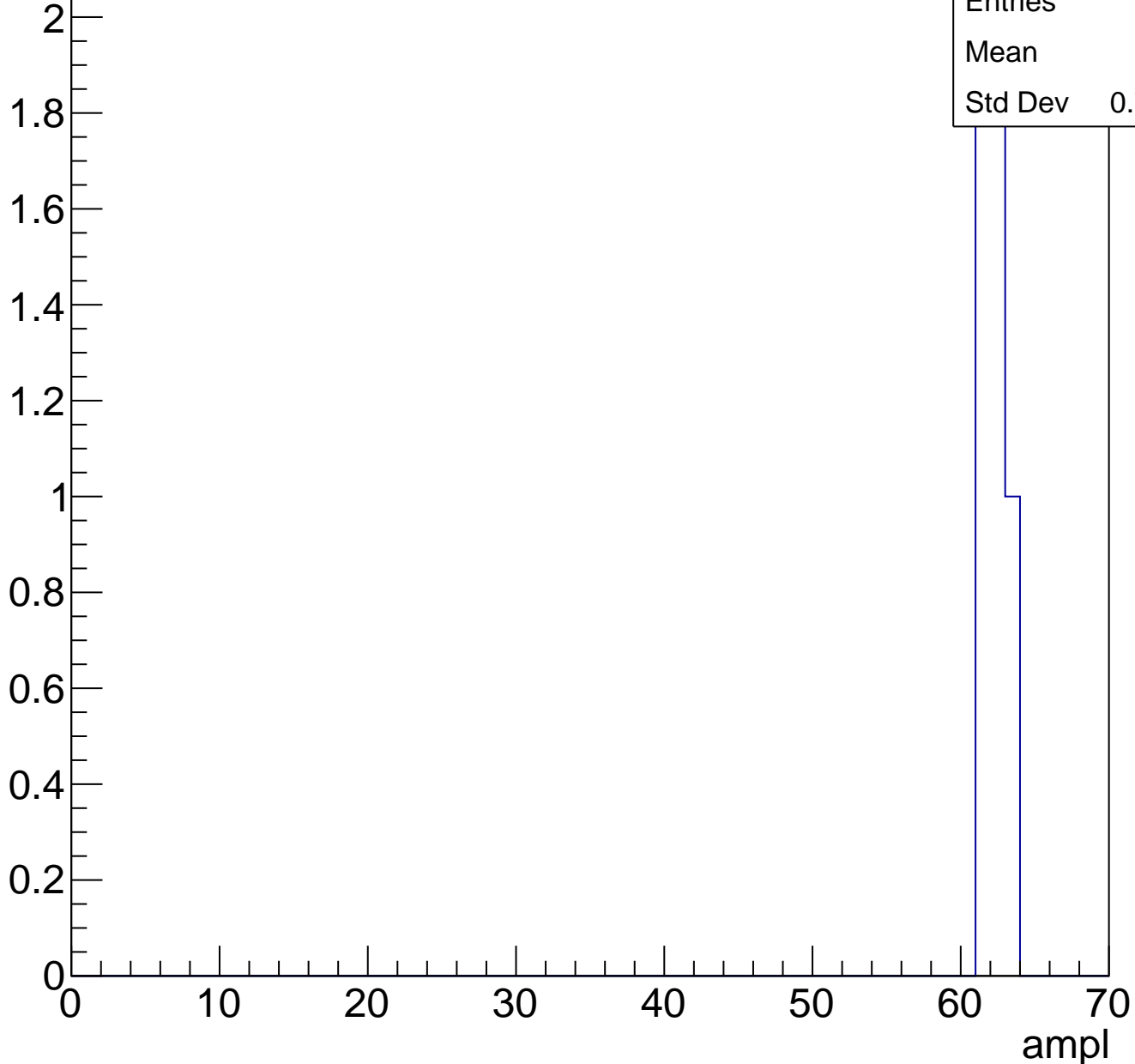
Entries	38
Mean	58.79
Std Dev	9.895



# B0L001S, U21-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	5
Mean	61.8
Std Dev	0.7483



# B0L001S, U21-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U21-ch122, adc0

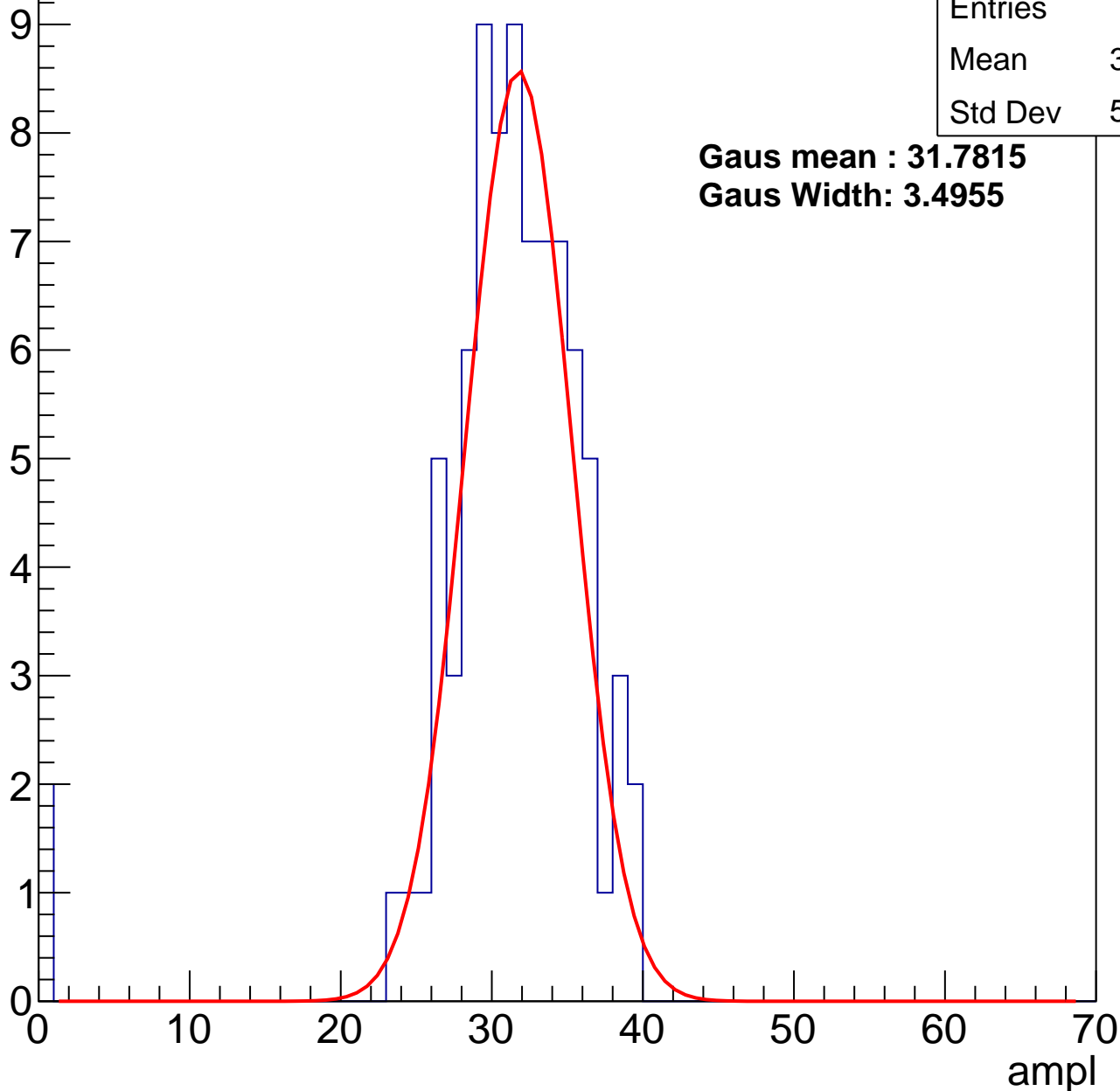
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	83
Mean	30.64
Std Dev	5.973

**Gaus mean : 31.7815**

**Gaus Width: 3.4955**



# B0L001S, U21-ch122, adc1

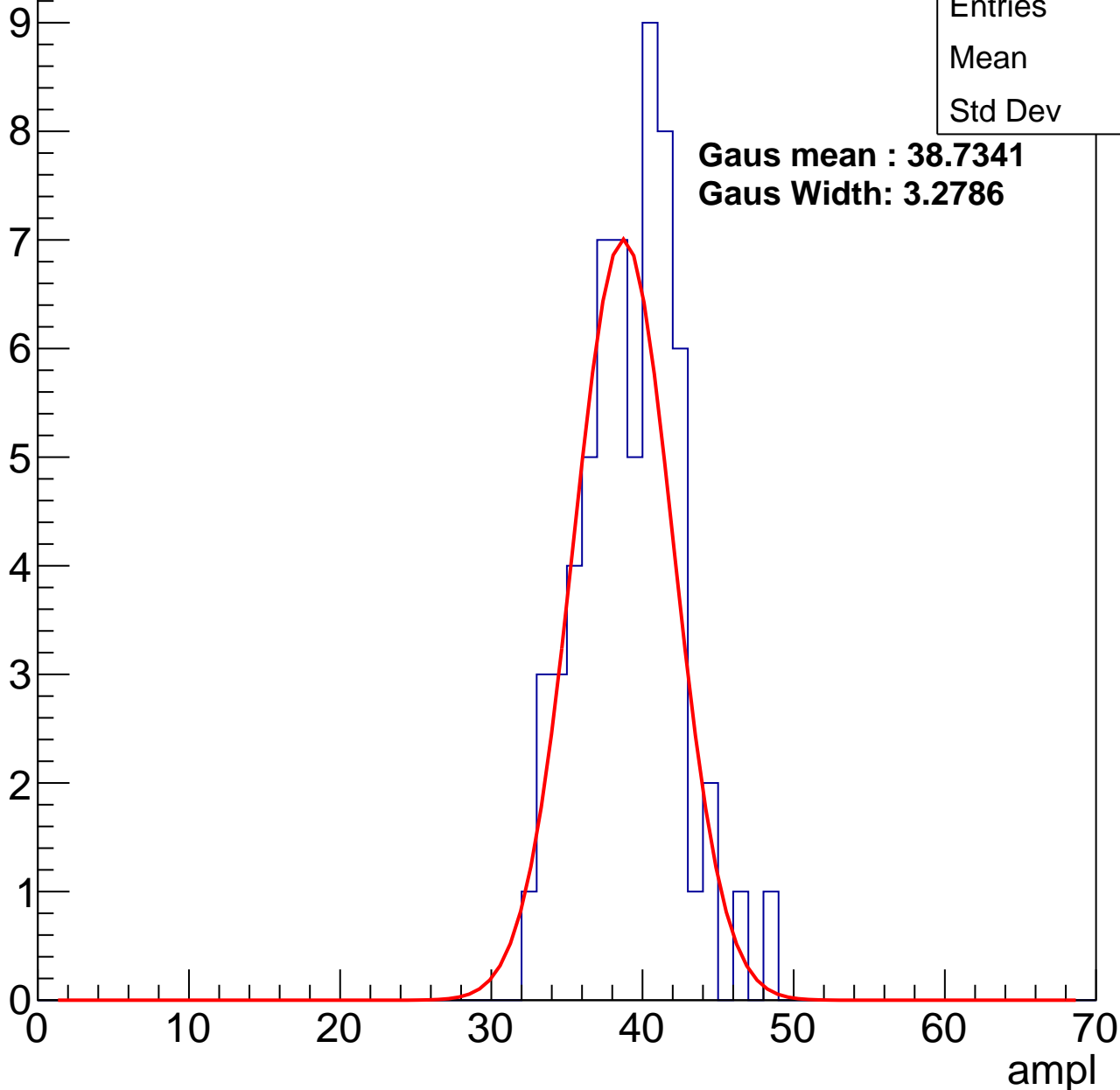
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	63
Mean	38.7
Std Dev	3.24

**Gaus mean : 38.7341**

**Gaus Width: 3.2786**



# B0L001S, U21-ch122, adc2

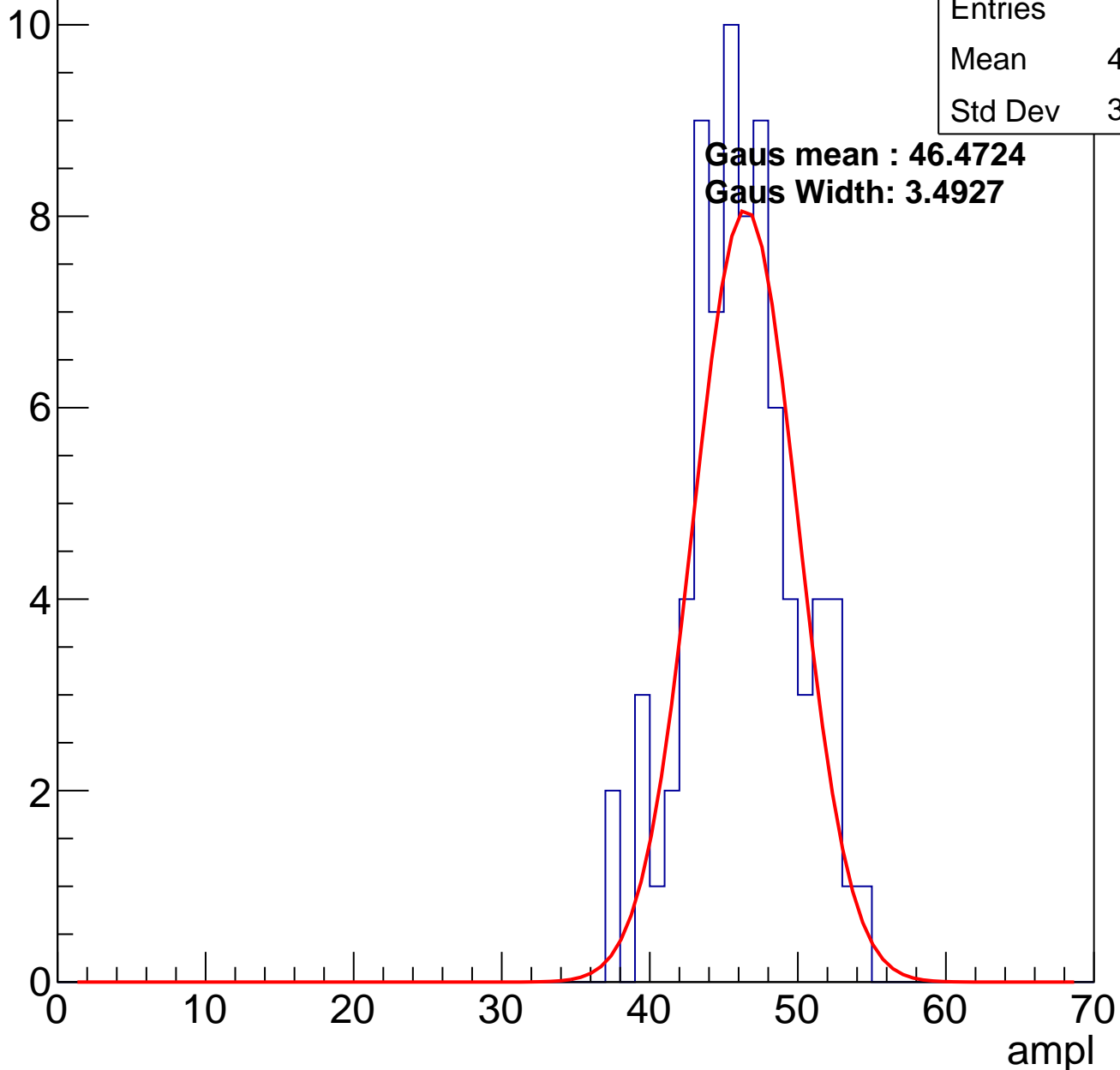
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	78
Mean	45.77
Std Dev	3.665

**Gaus mean : 46.4724**

**Gaus Width: 3.4927**

Entry

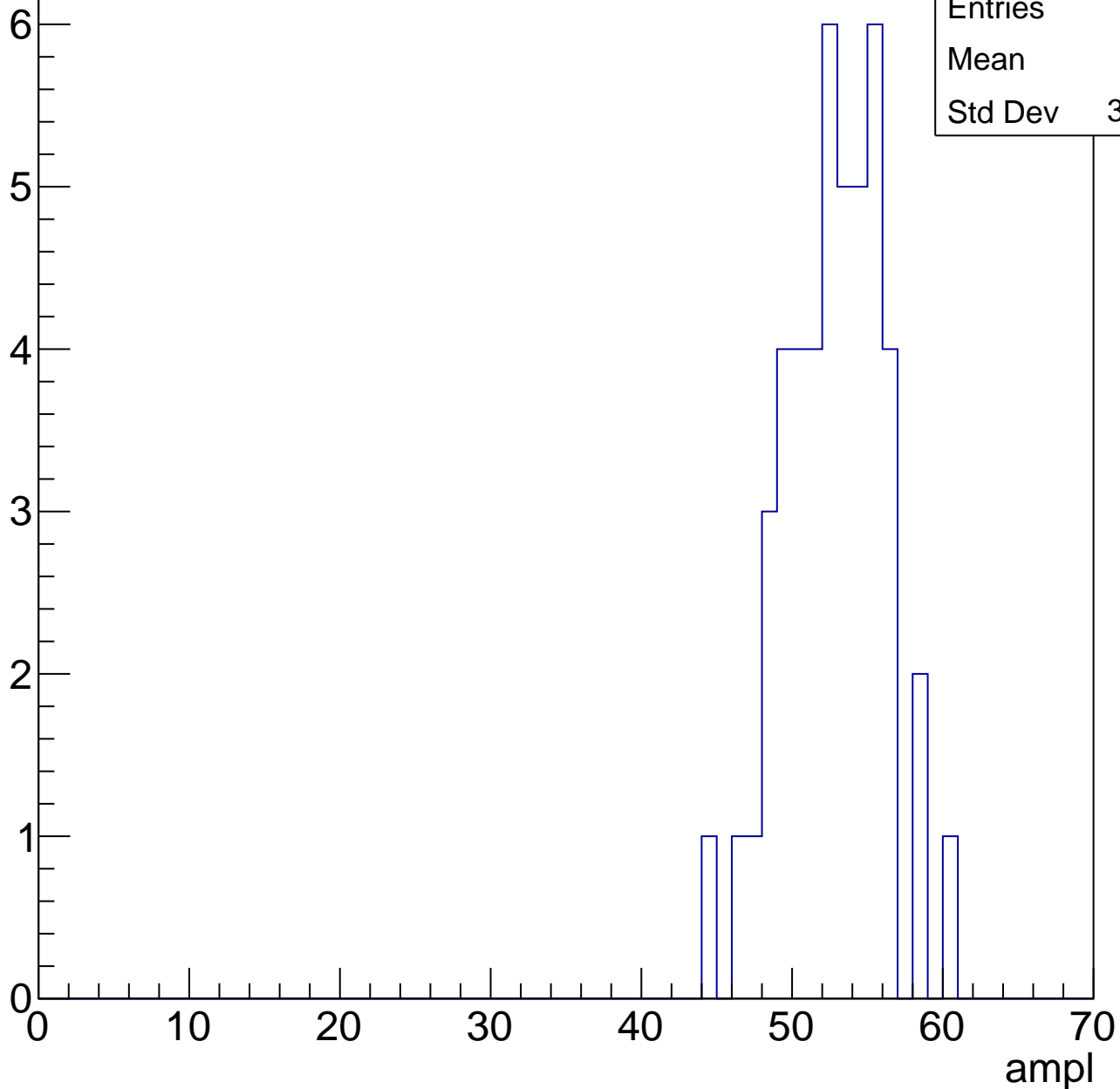


# B0L001S, U21-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	52.3
Std Dev	3.274

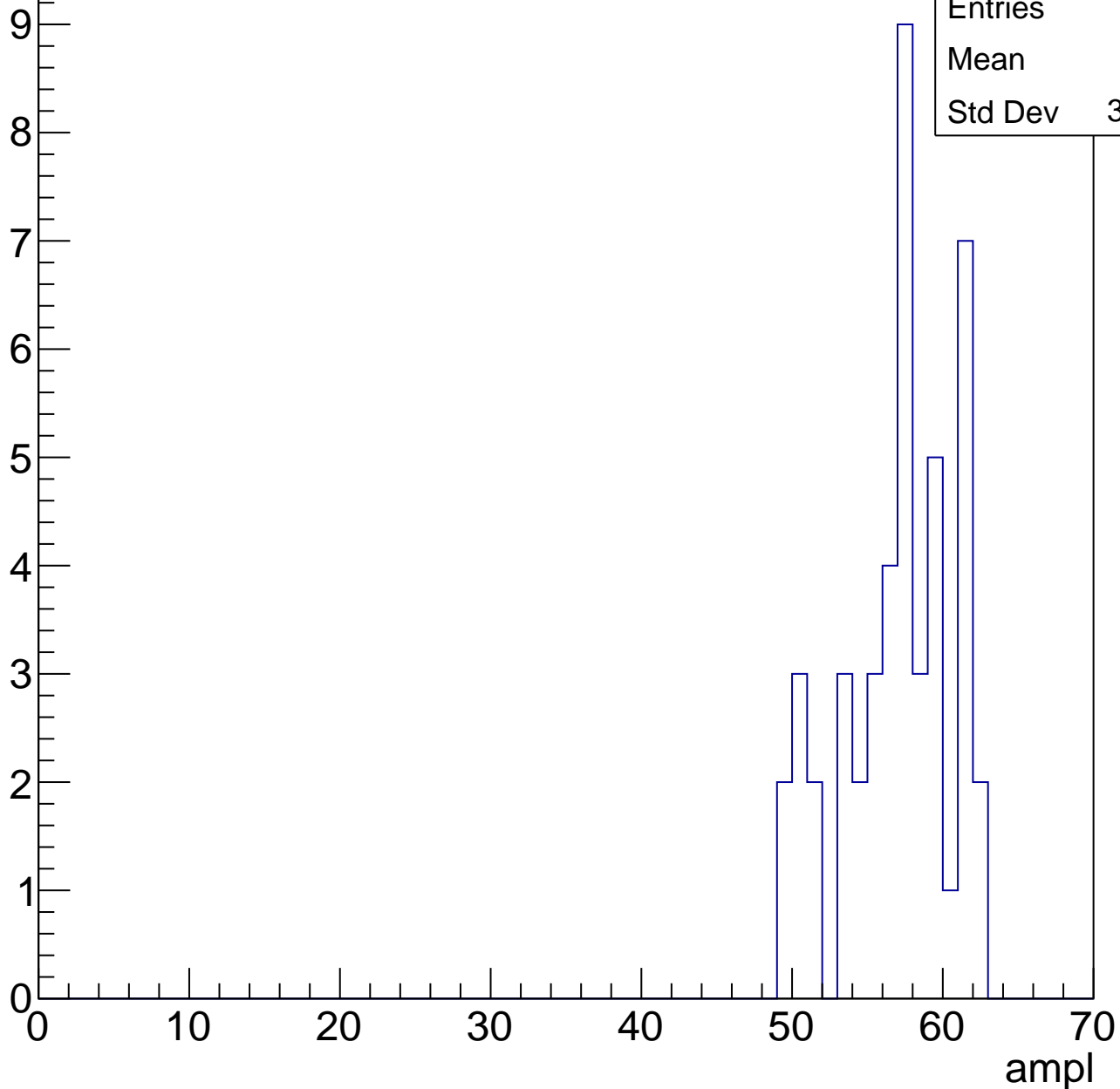


# B0L001S, U21-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

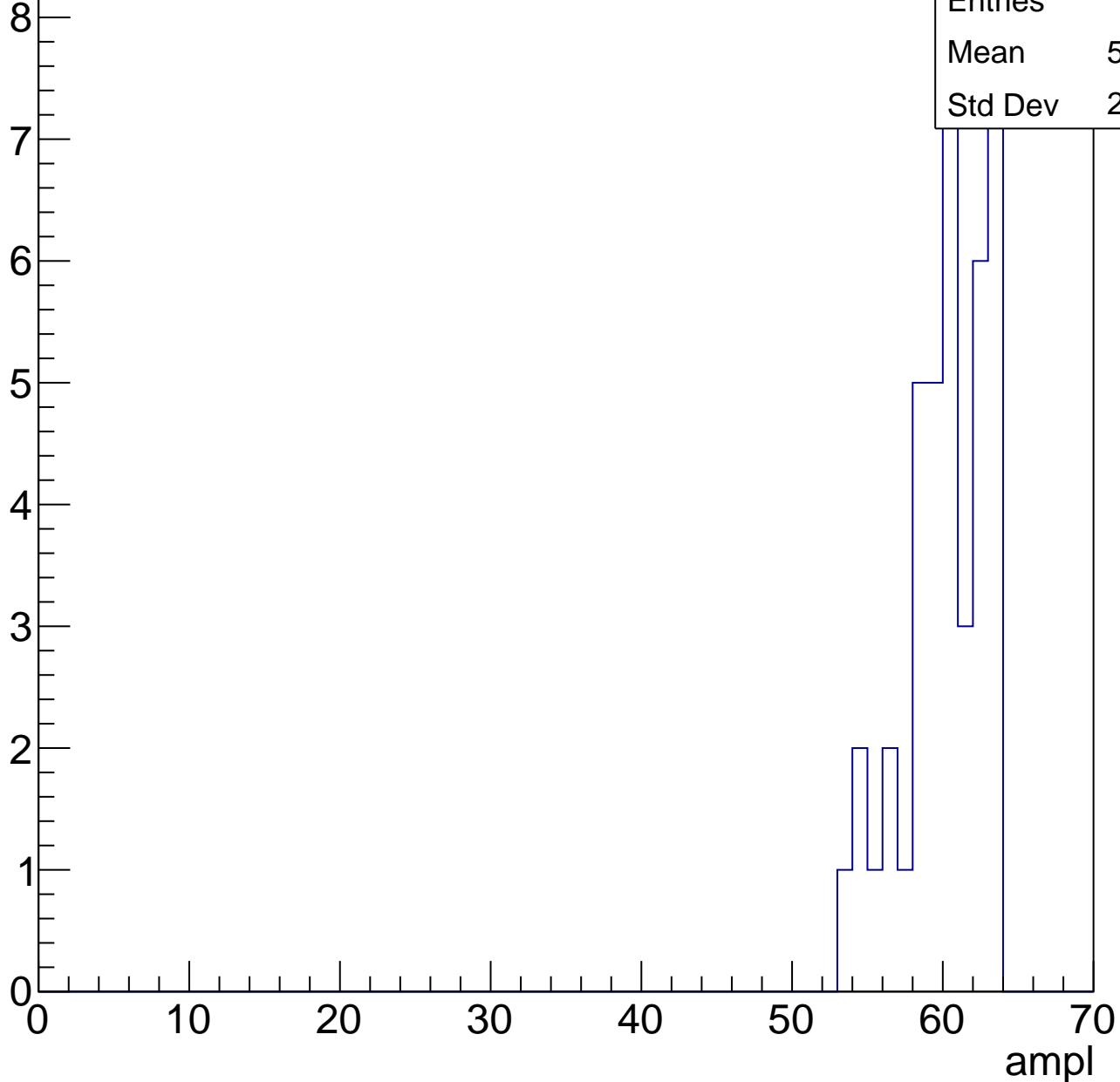
Entries	46
Mean	56.5
Std Dev	3.646



# B0L001S, U21-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

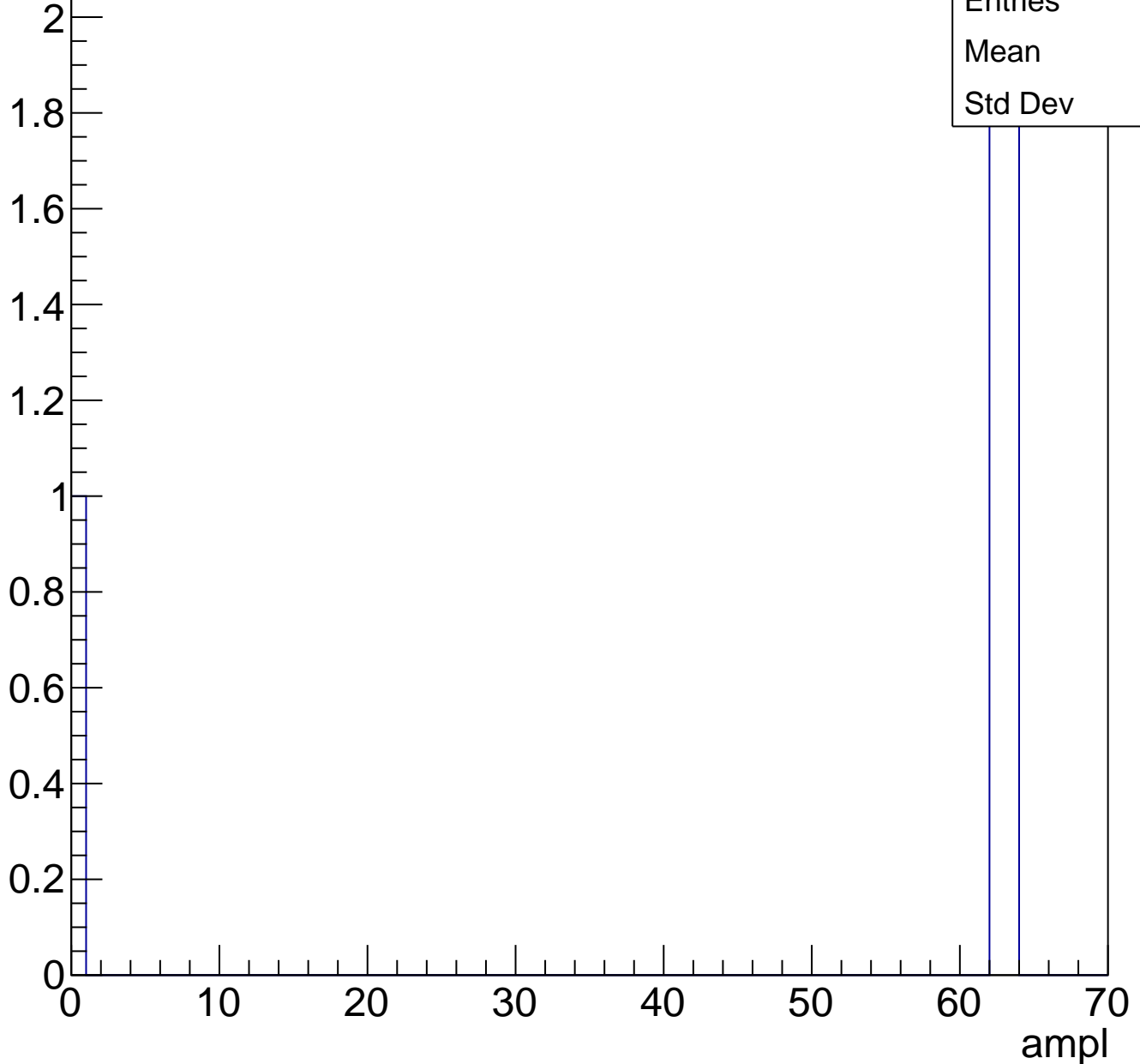
Entry



# B0L001S, U21-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	5
Mean	50
Std Dev	25



# B0L001S, U21-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U21-ch123, adc0

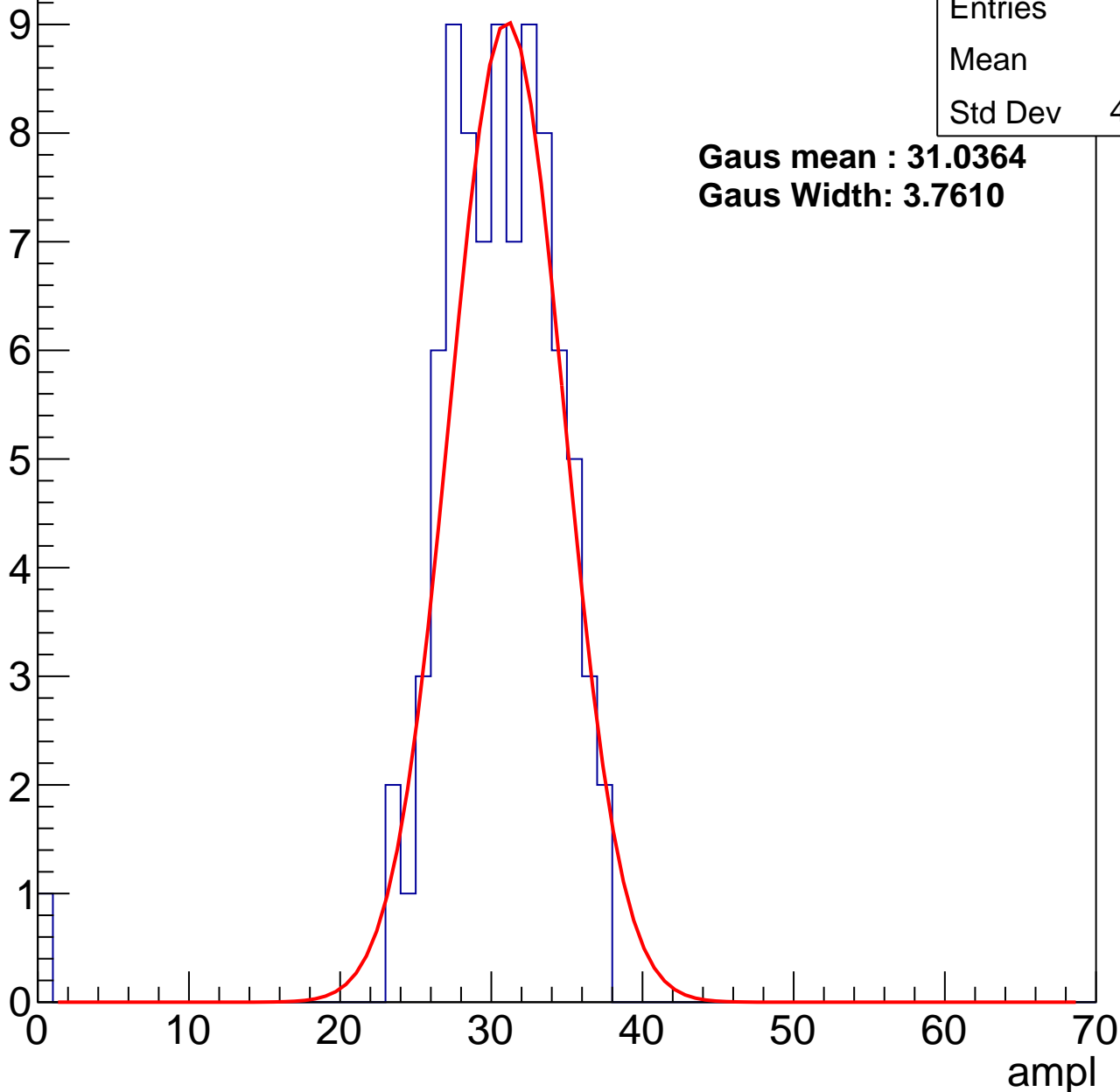
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	86
Mean	29.9
Std Dev	4.658

**Gaus mean : 31.0364**

**Gaus Width: 3.7610**



# B0L001S, U21-ch123, adc1

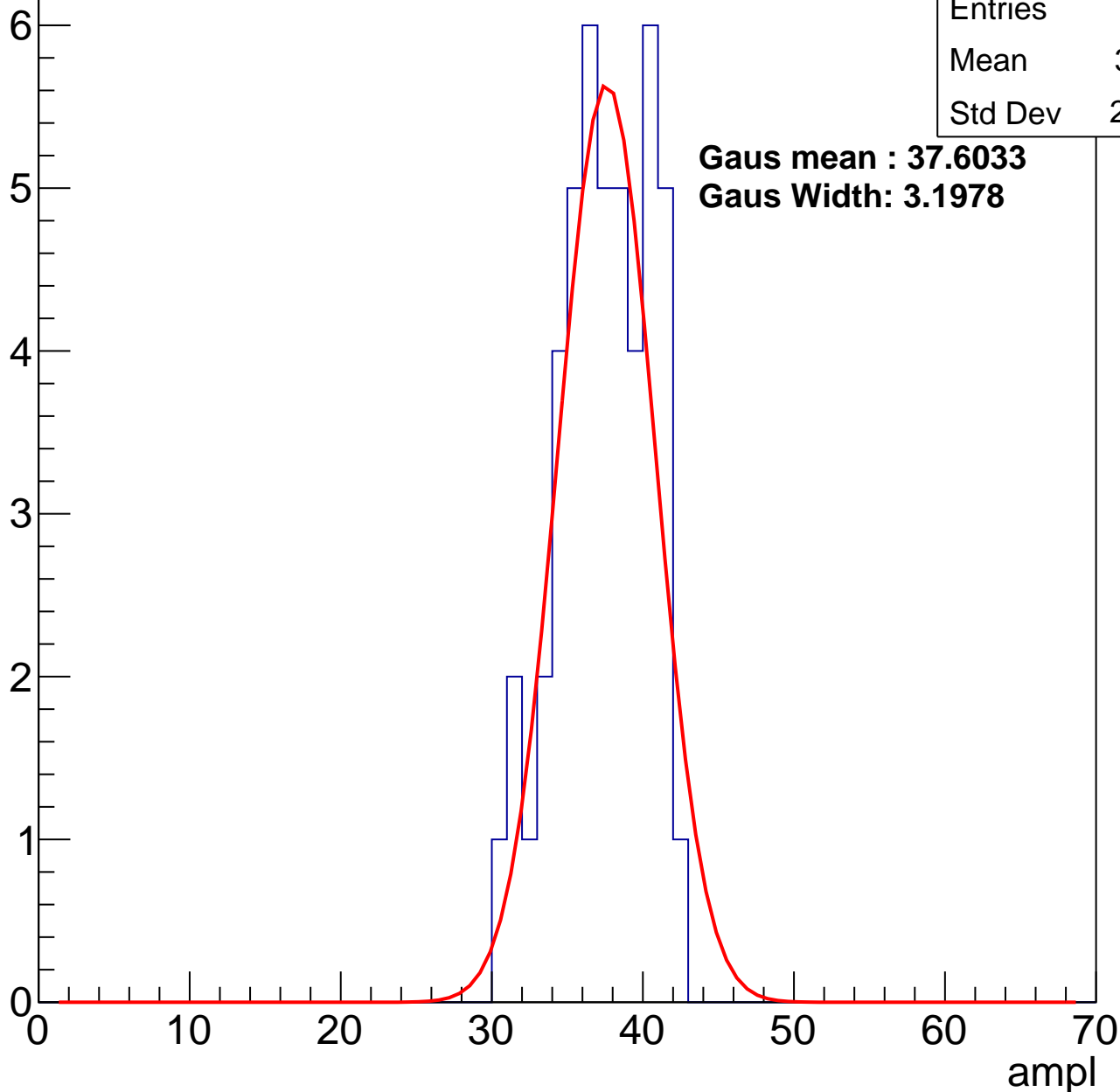
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	36.91
Std Dev	2.988

**Gaus mean : 37.6033**

**Gaus Width: 3.1978**



# B0L001S, U21-ch123, adc2

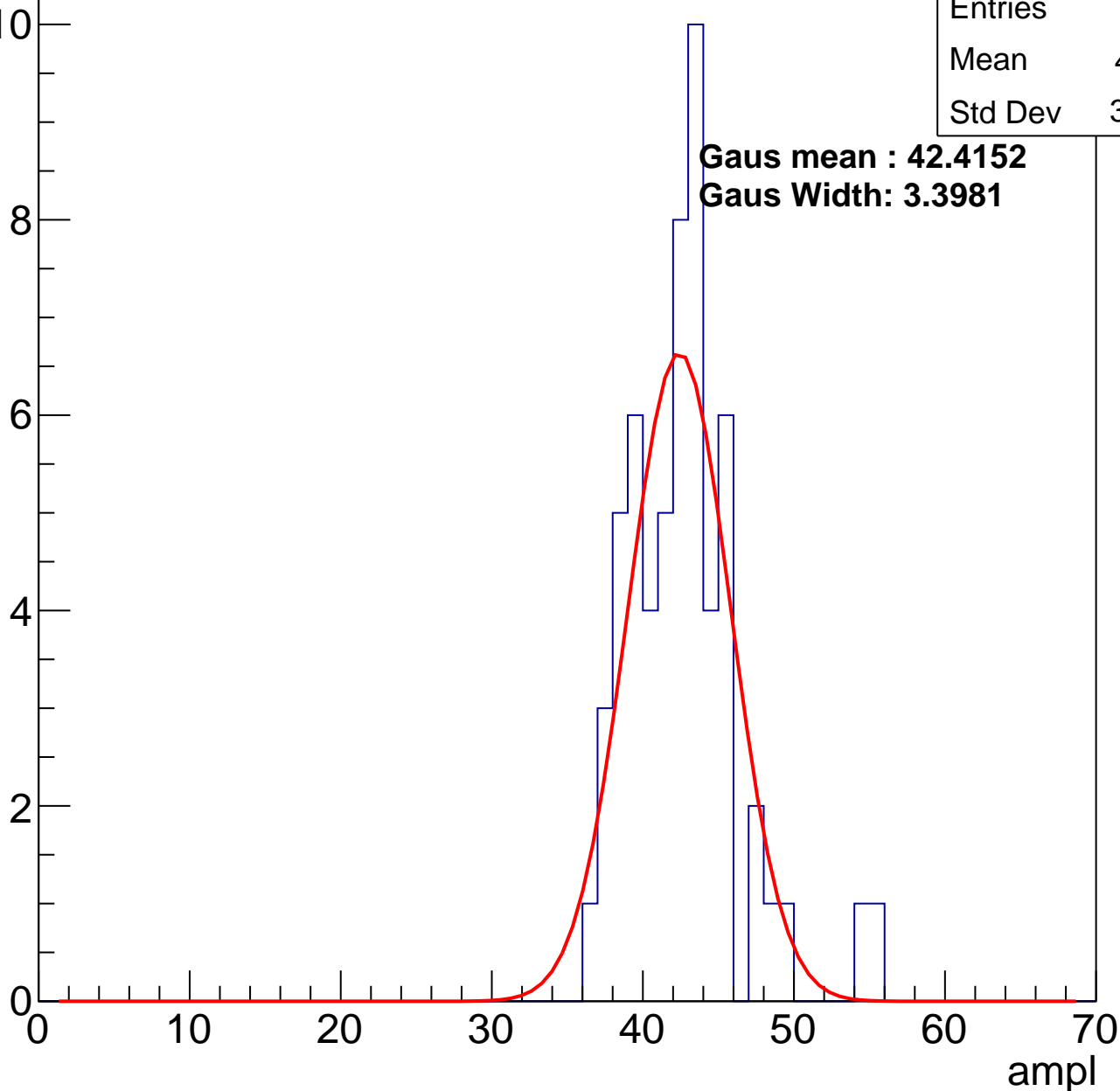
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	58
Mean	42.21
Std Dev	3.694

**Gaus mean : 42.4152**

**Gaus Width: 3.3981**

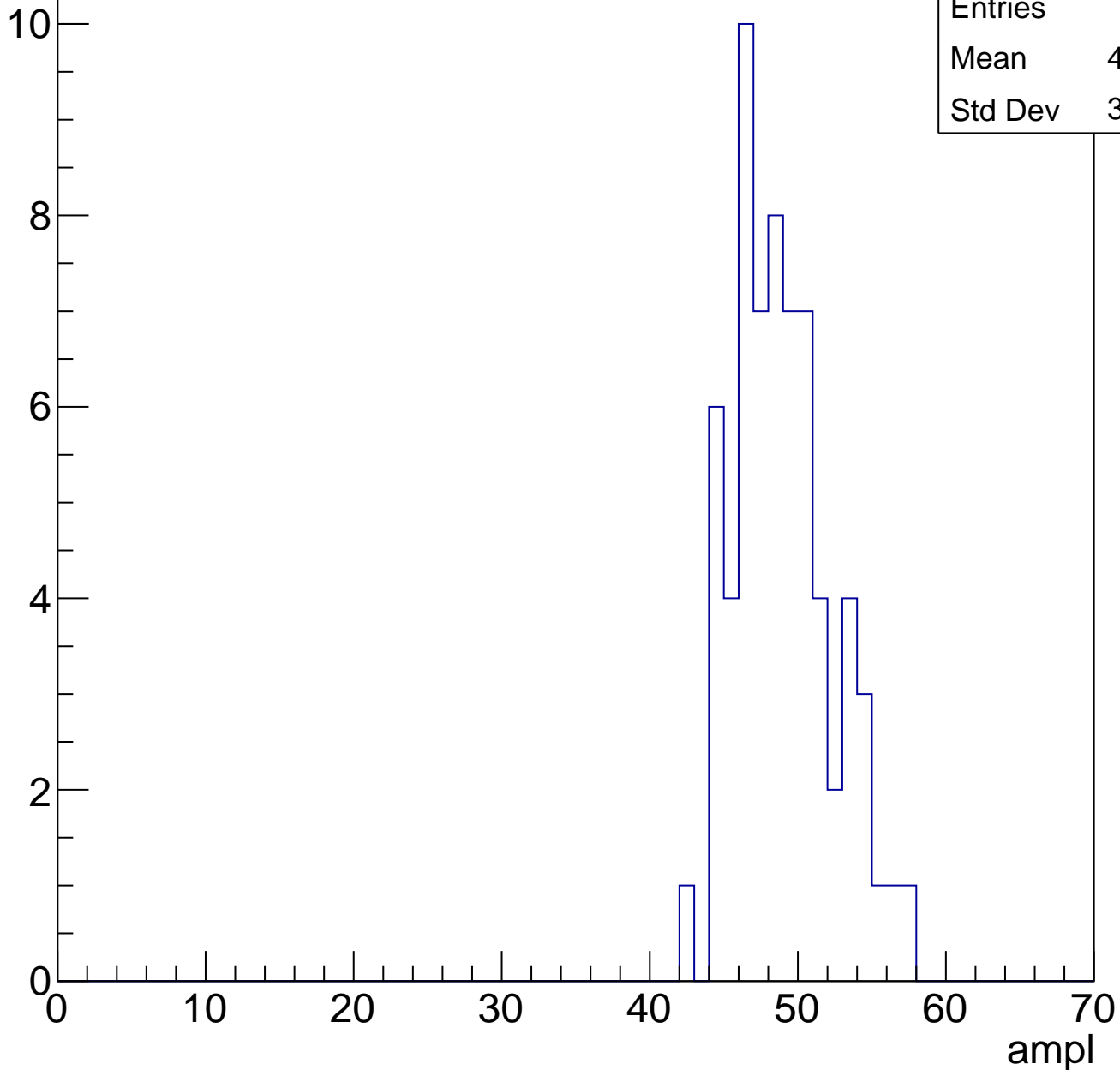


# B0L001S, U21-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	66
Mean	48.52
Std Dev	3.262

Entry

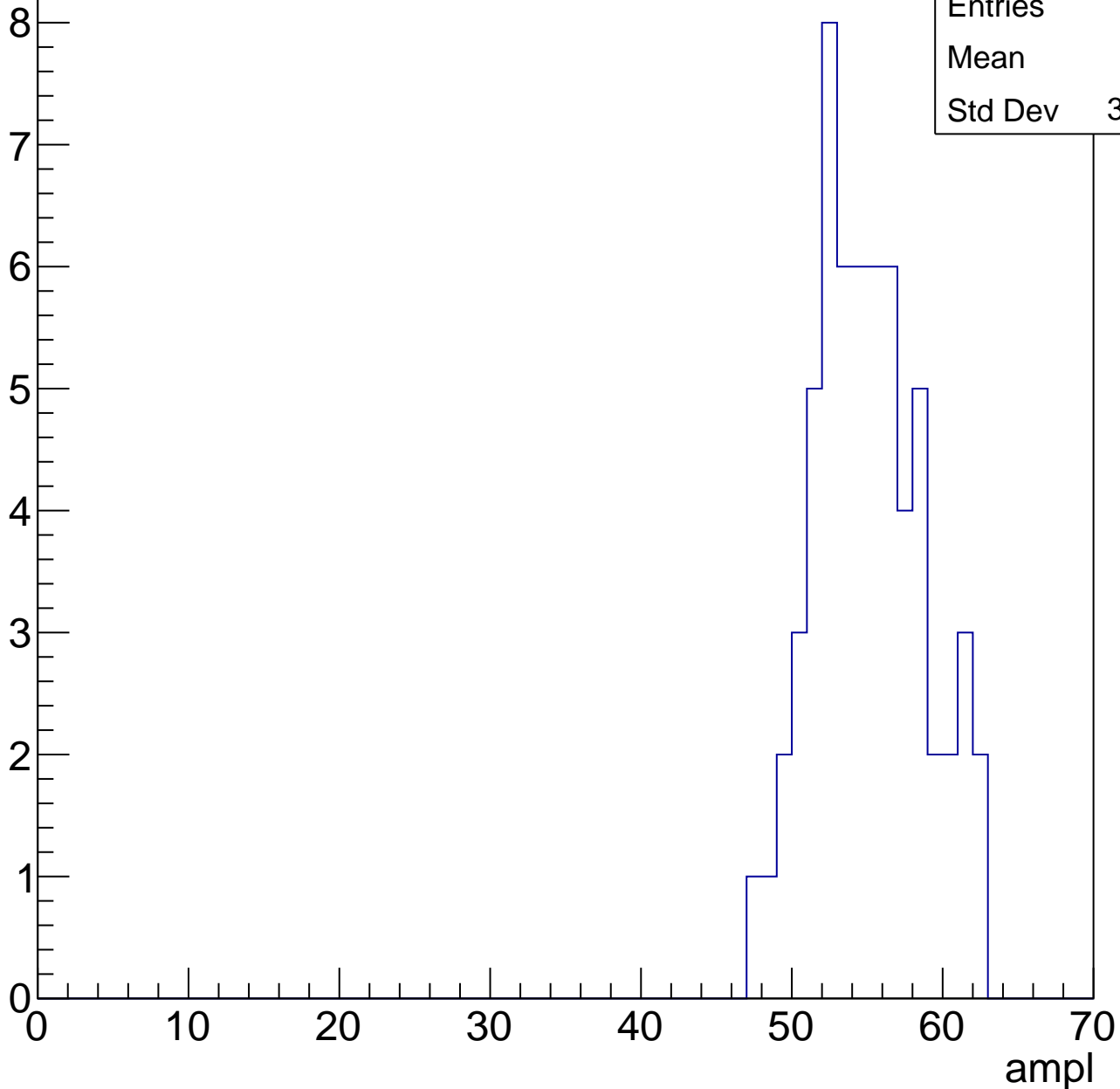


# B0L001S, U21-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	62
Mean	54.6
Std Dev	3.563

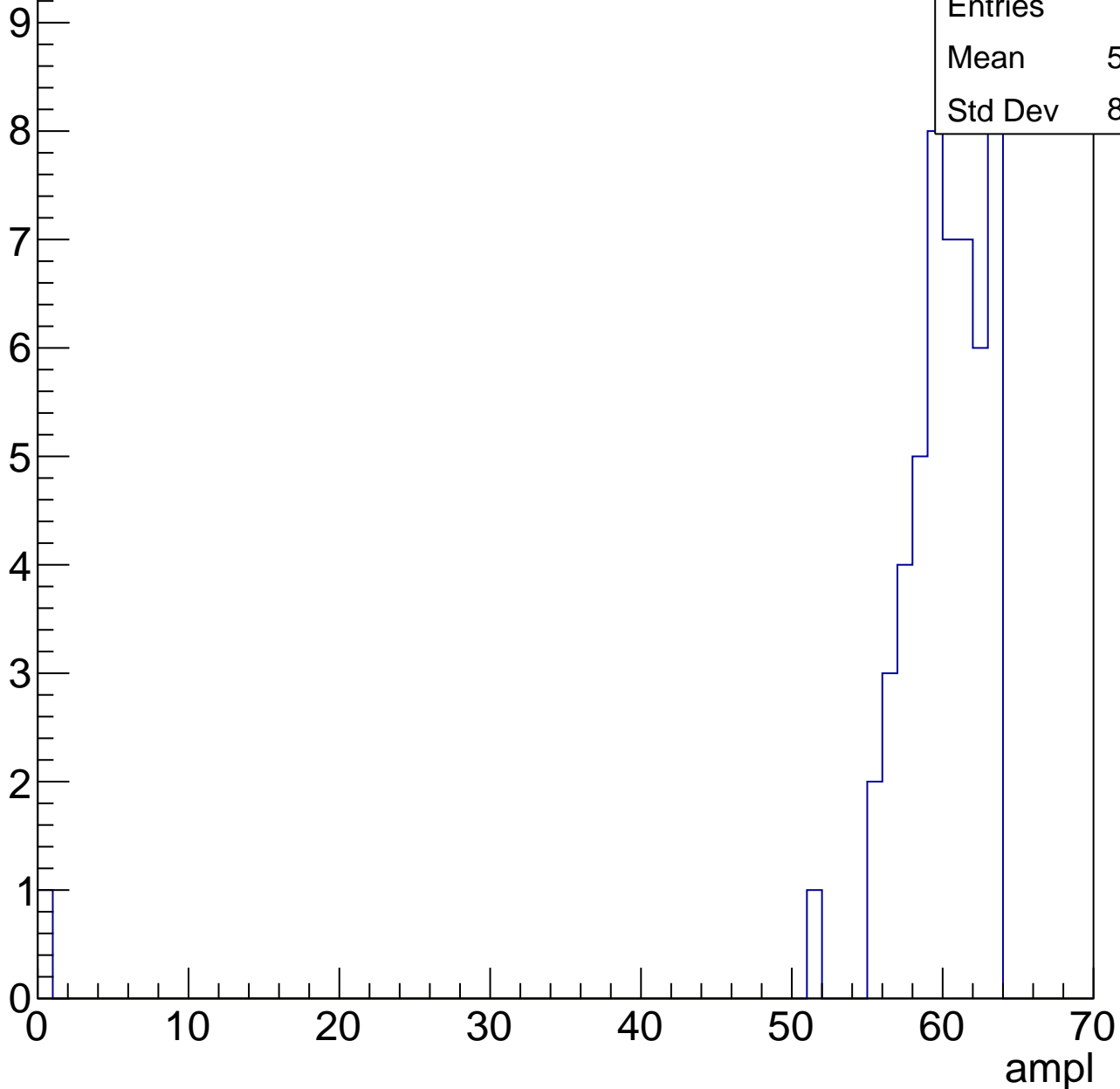


# B0L001S, U21-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	53
Mean	58.58
Std Dev	8.522



# B0L001S, U21-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	60.8
Std Dev	2.135

ampl

0 10 20 30 40 50 60 70



# B0L001S, U21-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U21-ch124, adc0

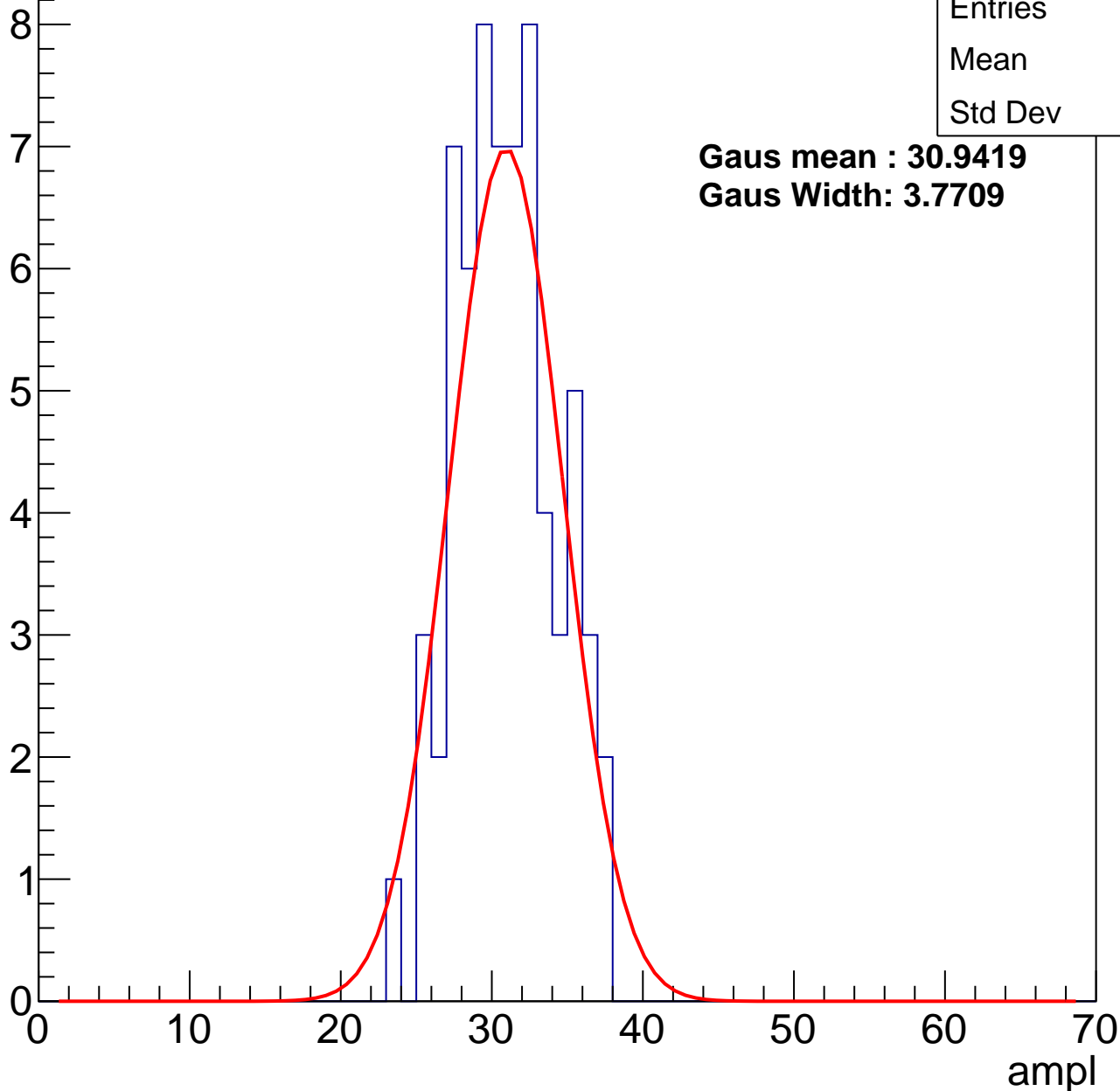
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	30.5
Std Dev	3.23

**Gaus mean : 30.9419**

**Gaus Width: 3.7709**



# B0L001S, U21-ch124, adc1

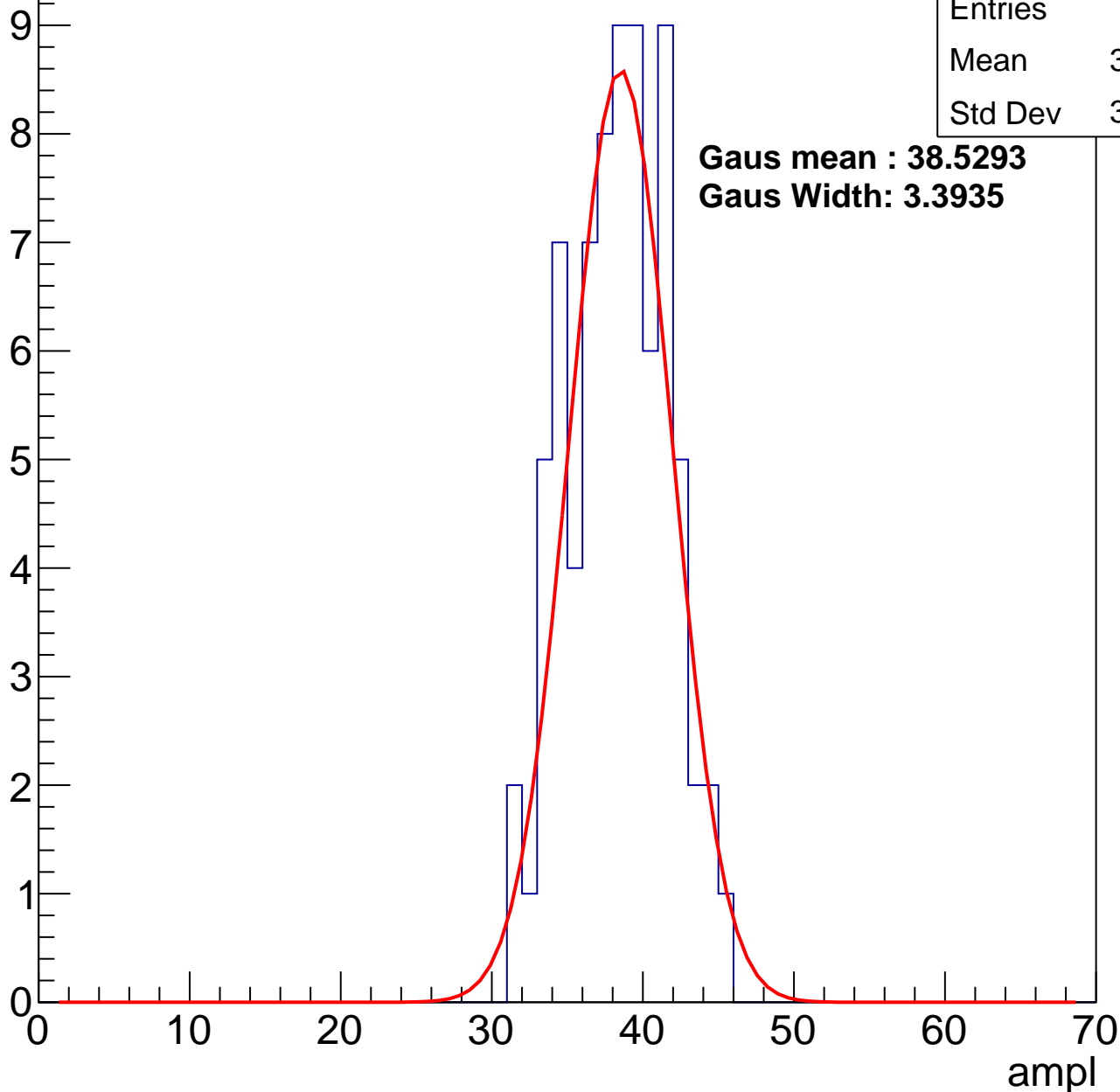
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	77
Mean	37.87
Std Dev	3.237

**Gaus mean : 38.5293**

**Gaus Width: 3.3935**

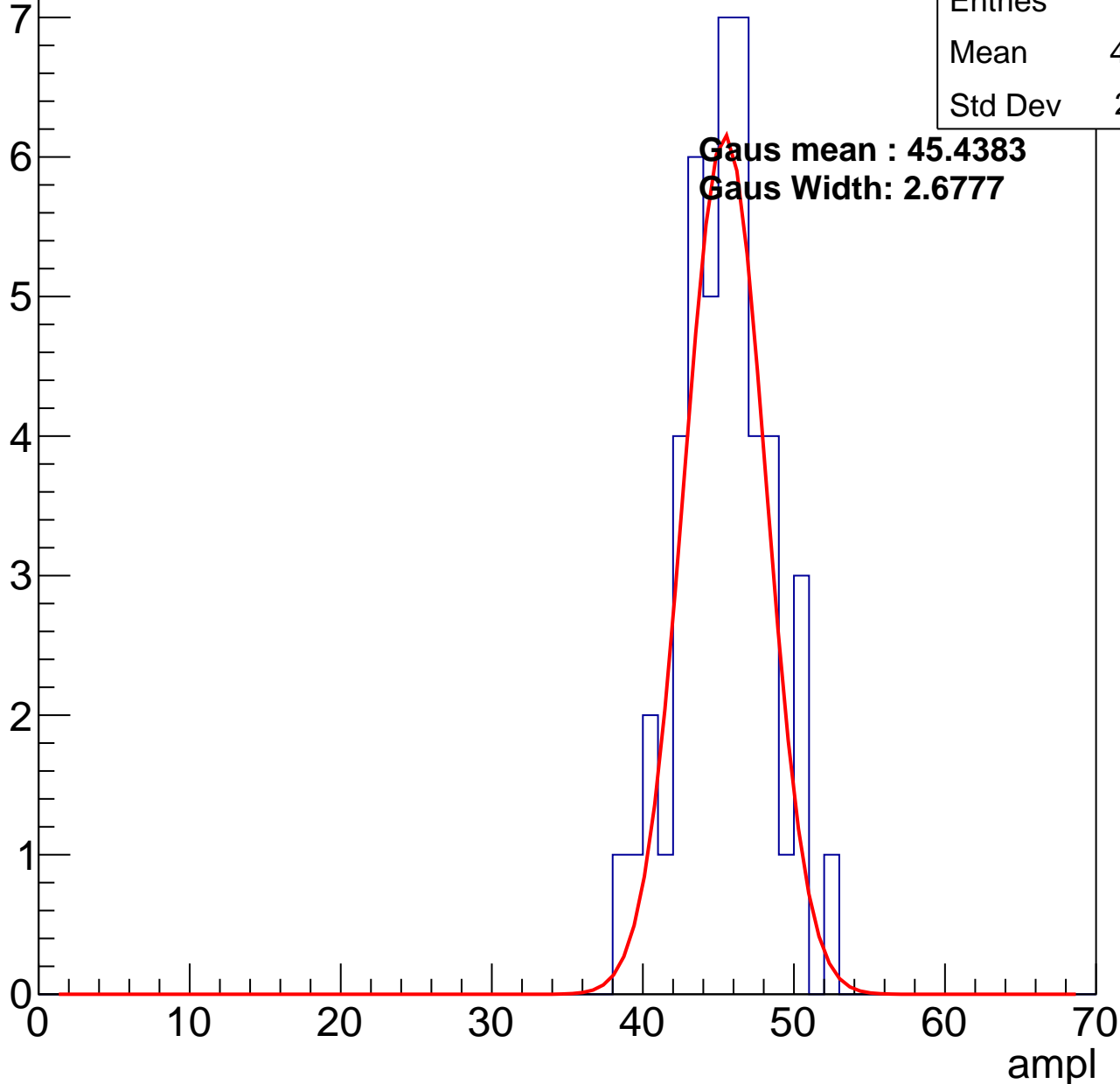


# B0L001S, U21-ch124, adc2

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	44.94
Std Dev	2.971

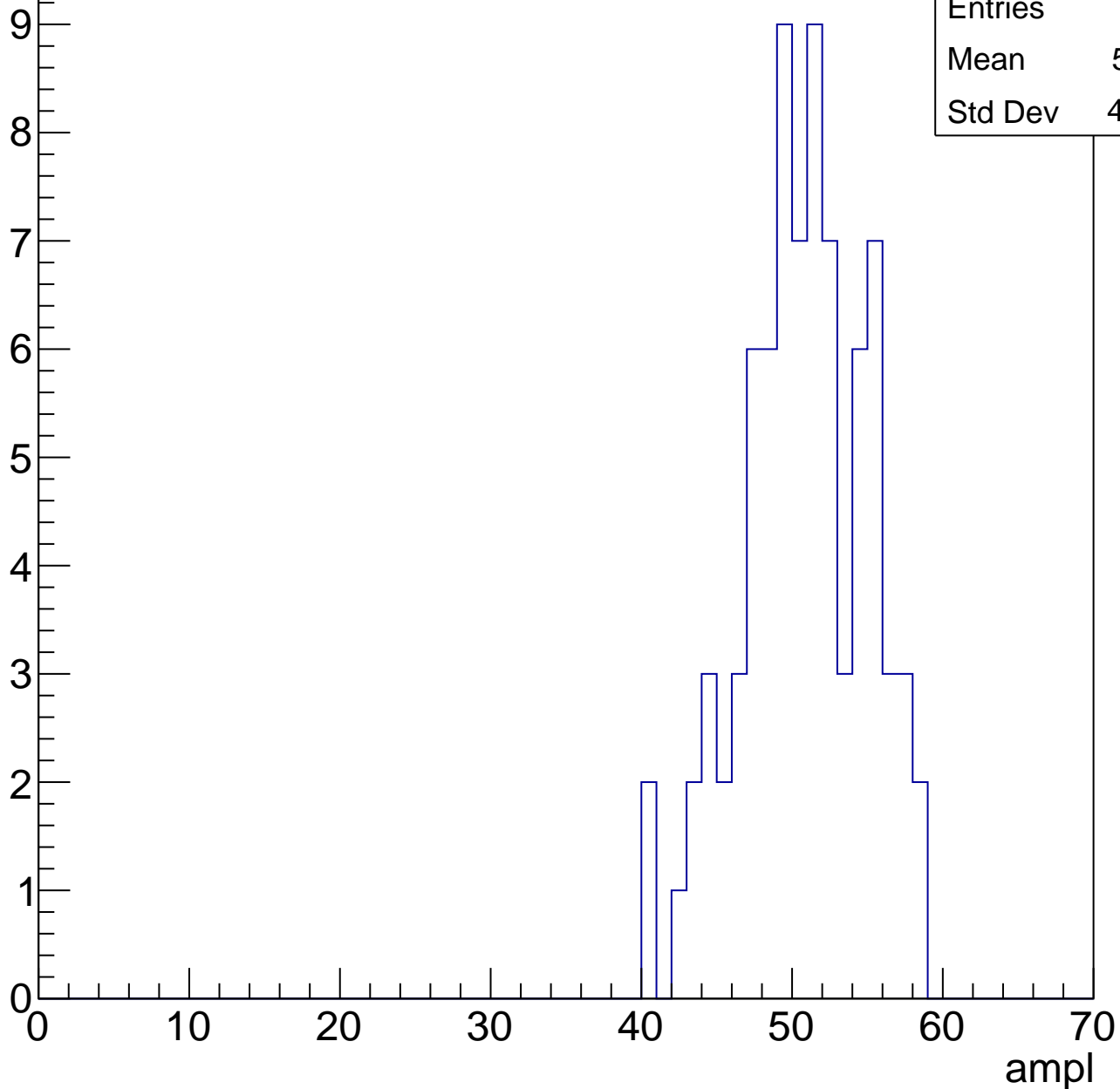


# B0L001S, U21-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	81
Mean	50.31
Std Dev	4.106

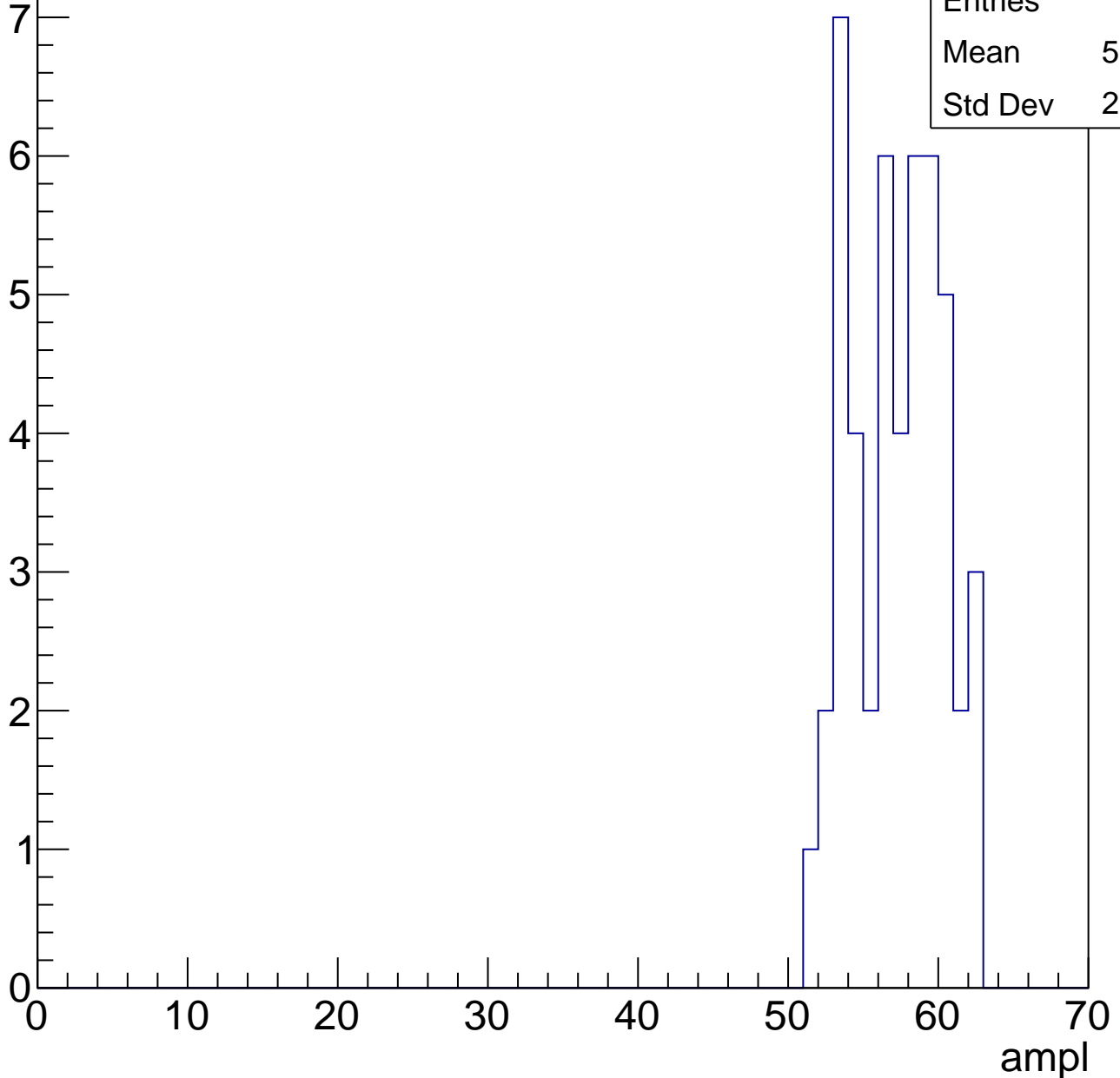


# B0L001S, U21-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	56.79
Std Dev	2.986

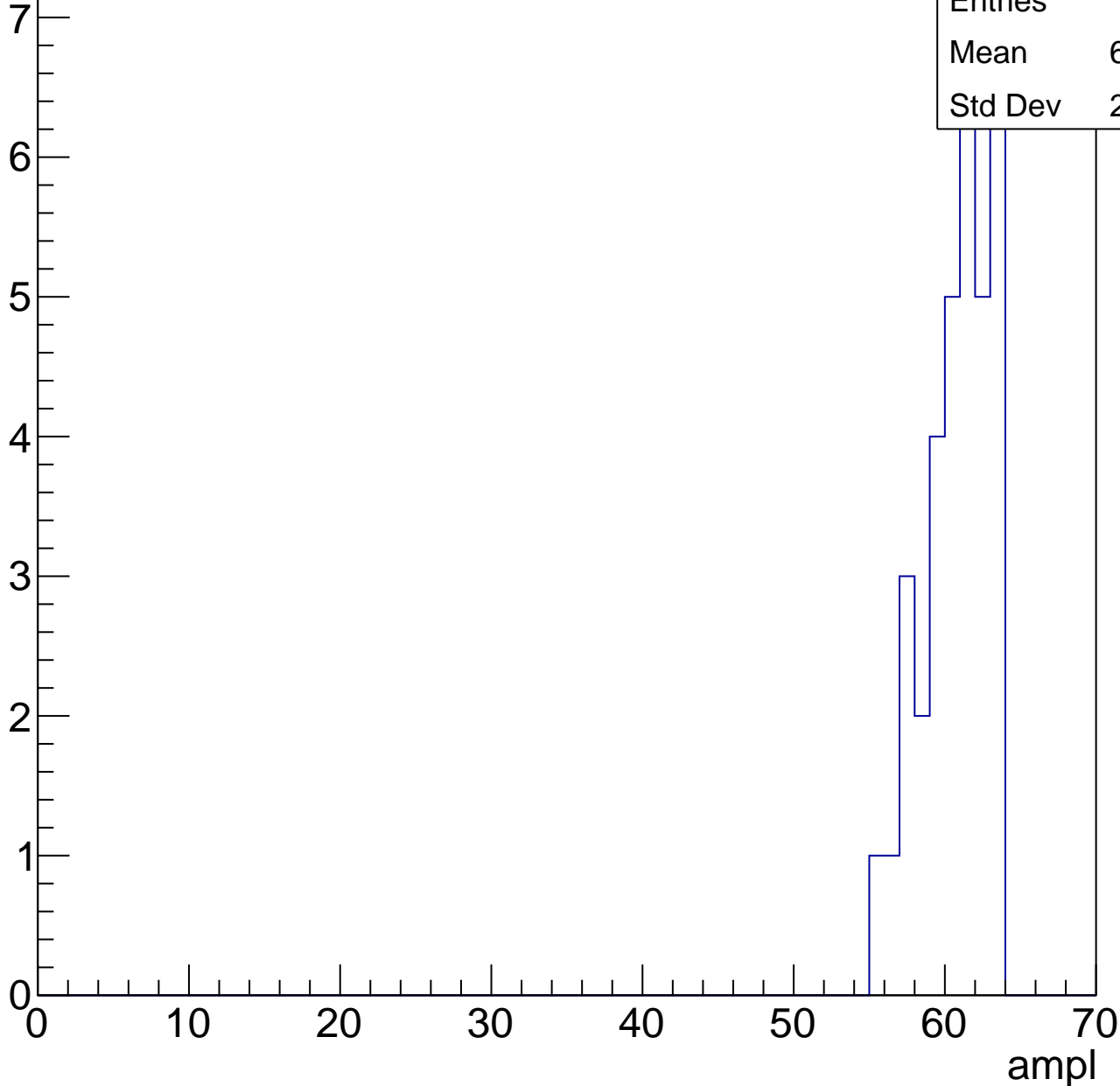


# B0L001S, U21-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	35
Mean	60.34
Std Dev	2.177



# B0L001S, U21-ch124, adc6

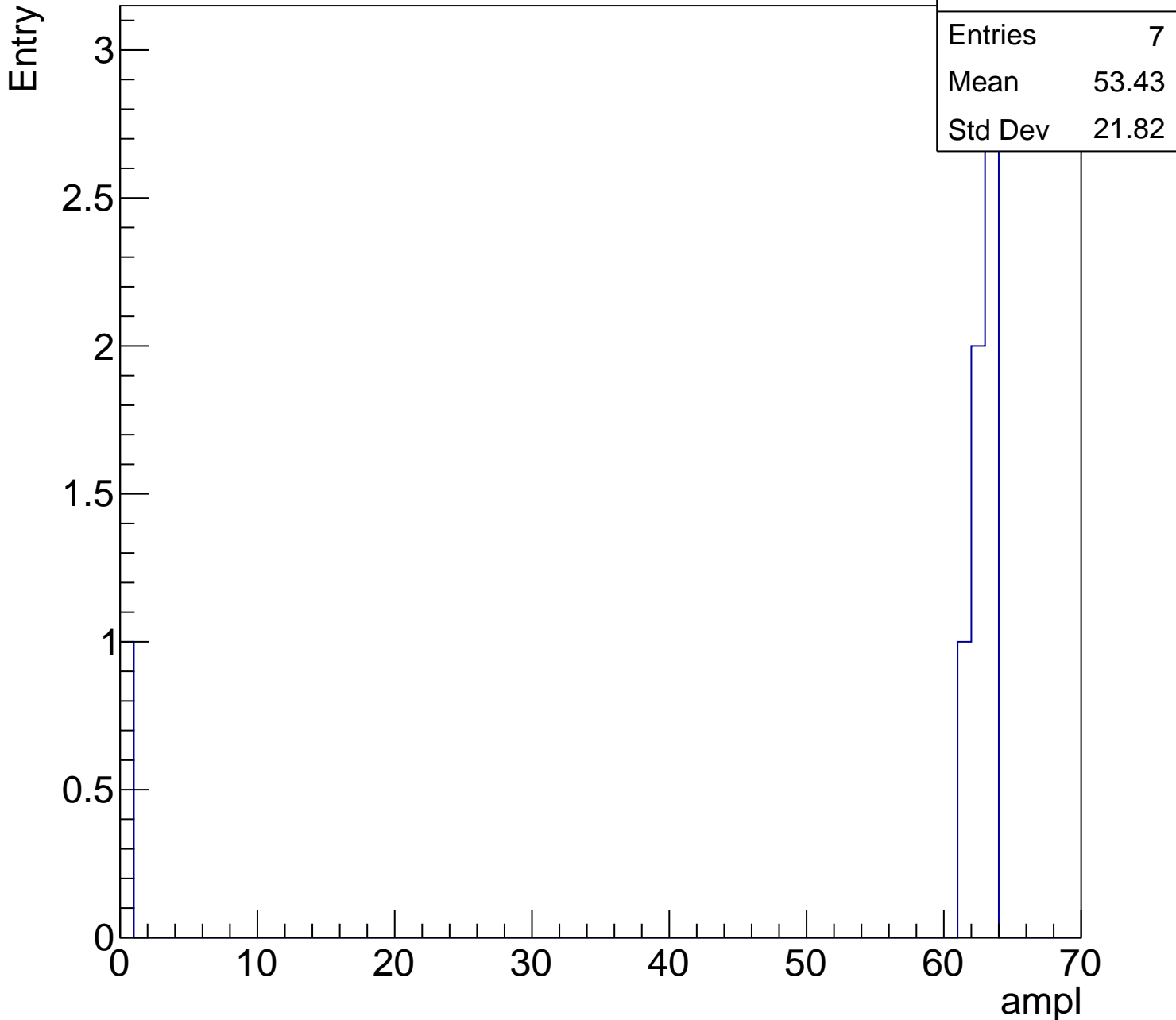
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	7
Mean	53.43
Std Dev	21.82

ampl





# B0L001S, U21-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	1
Mean	0
Std Dev	0

# B0L001S, U21-ch125, adc0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	67
Mean	29.07
Std Dev	4.618

**Gaus mean : 29.7732**

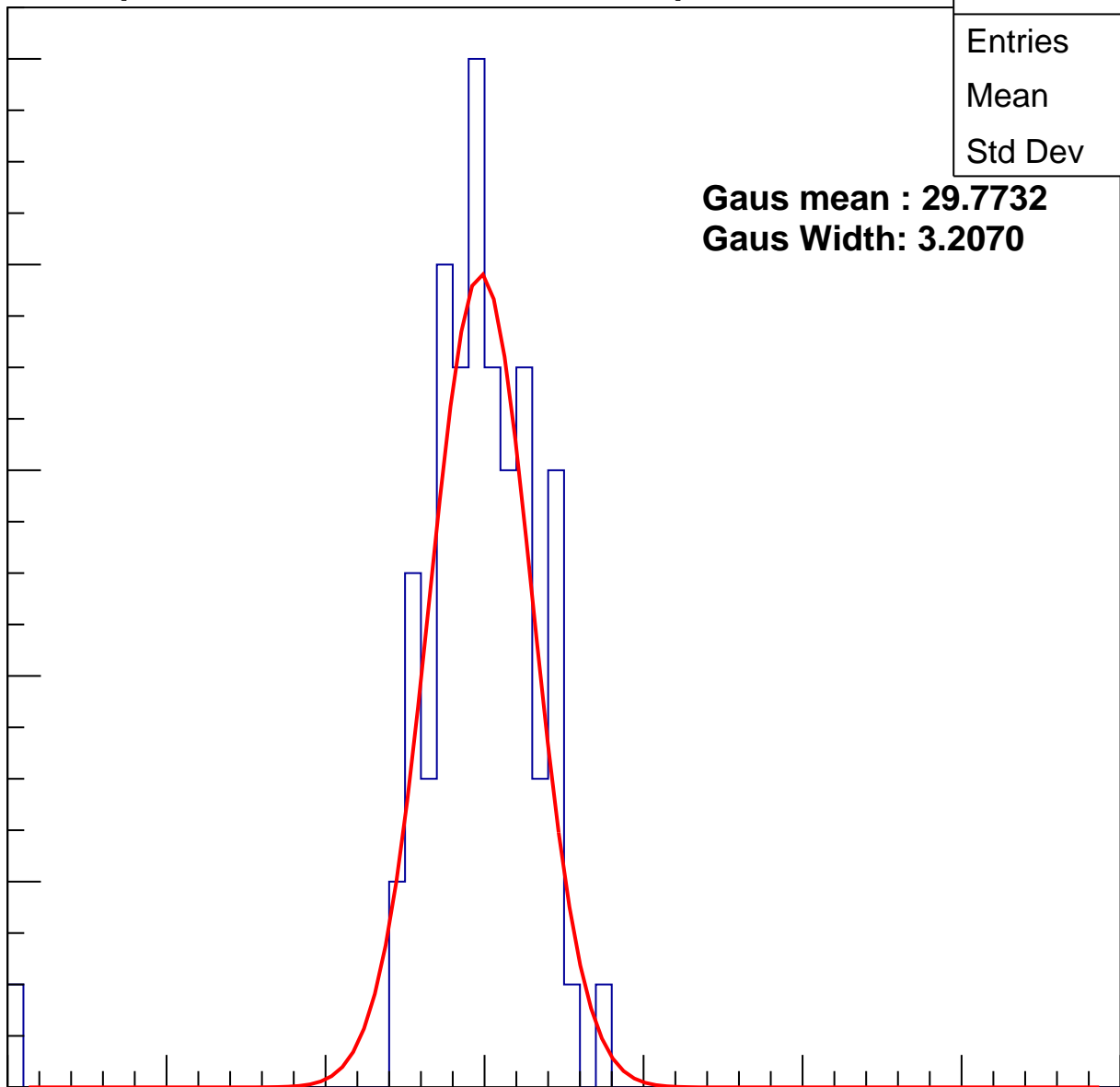
**Gaus Width: 3.2070**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L001S, U21-ch125, adc1

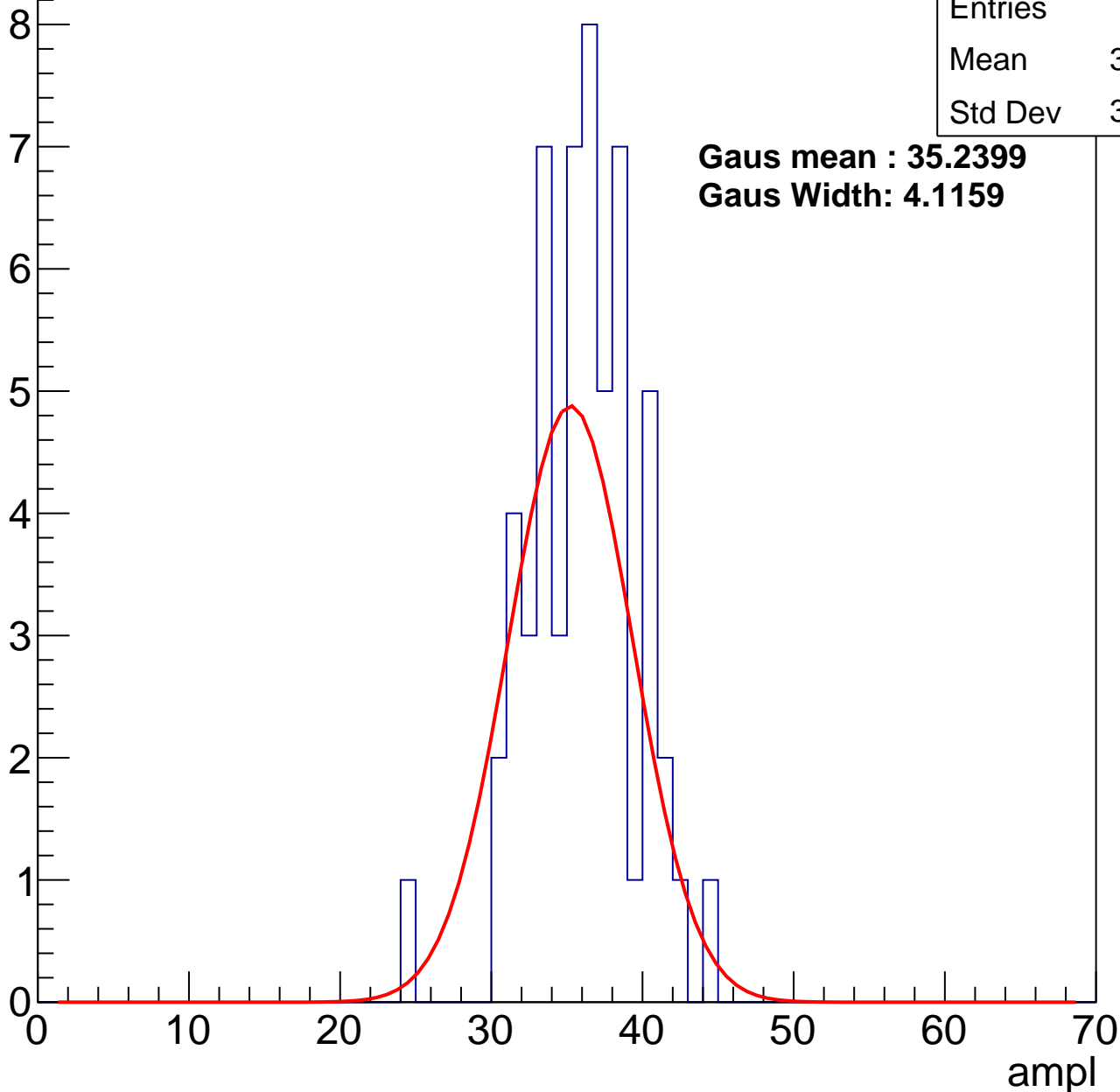
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	57
Mean	35.58
Std Dev	3.524

**Gaus mean : 35.2399**

**Gaus Width: 4.1159**



# B0L001S, U21-ch125, adc2

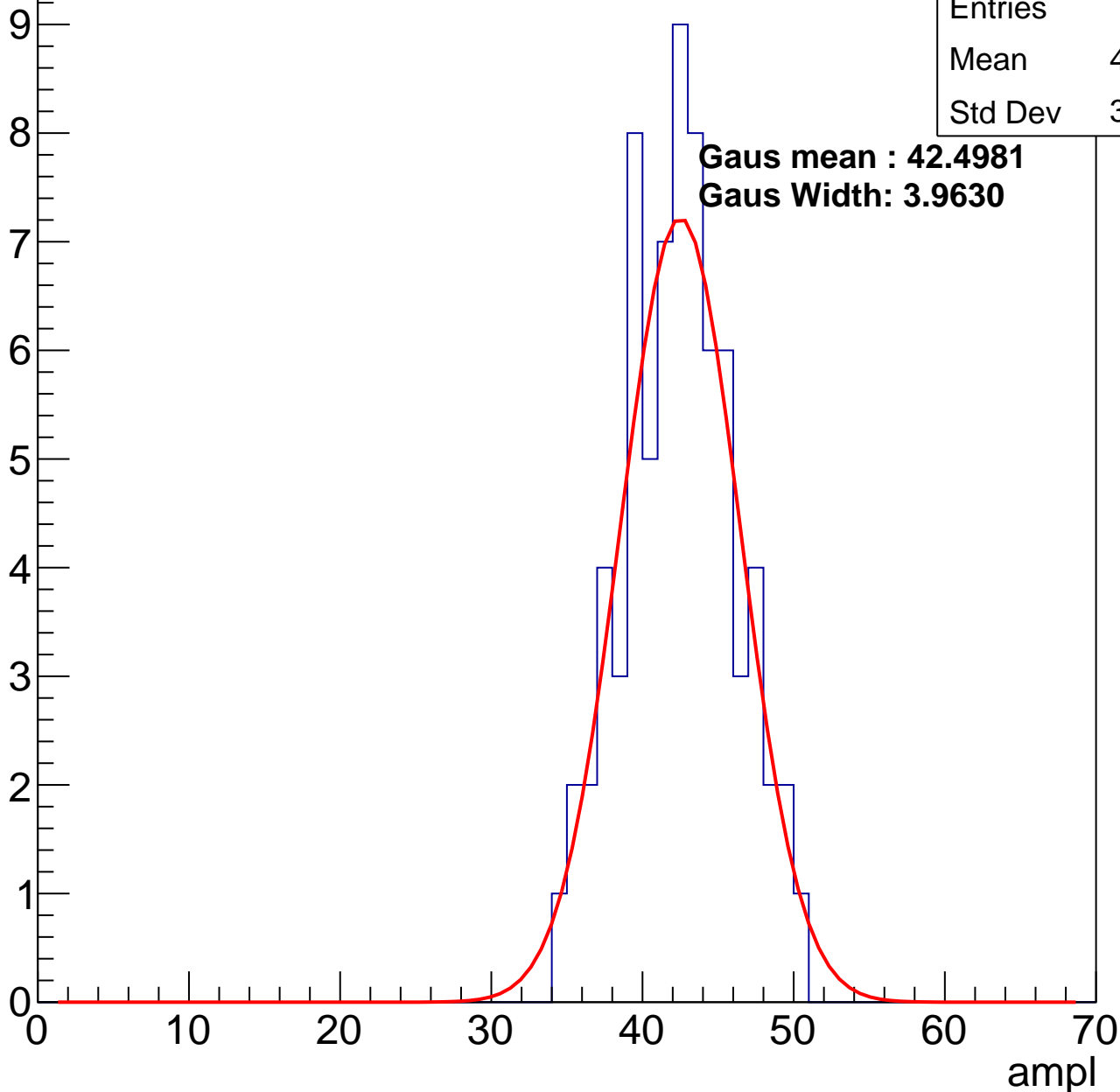
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	41.96
Std Dev	3.605

**Gaus mean : 42.4981**

**Gaus Width: 3.9630**

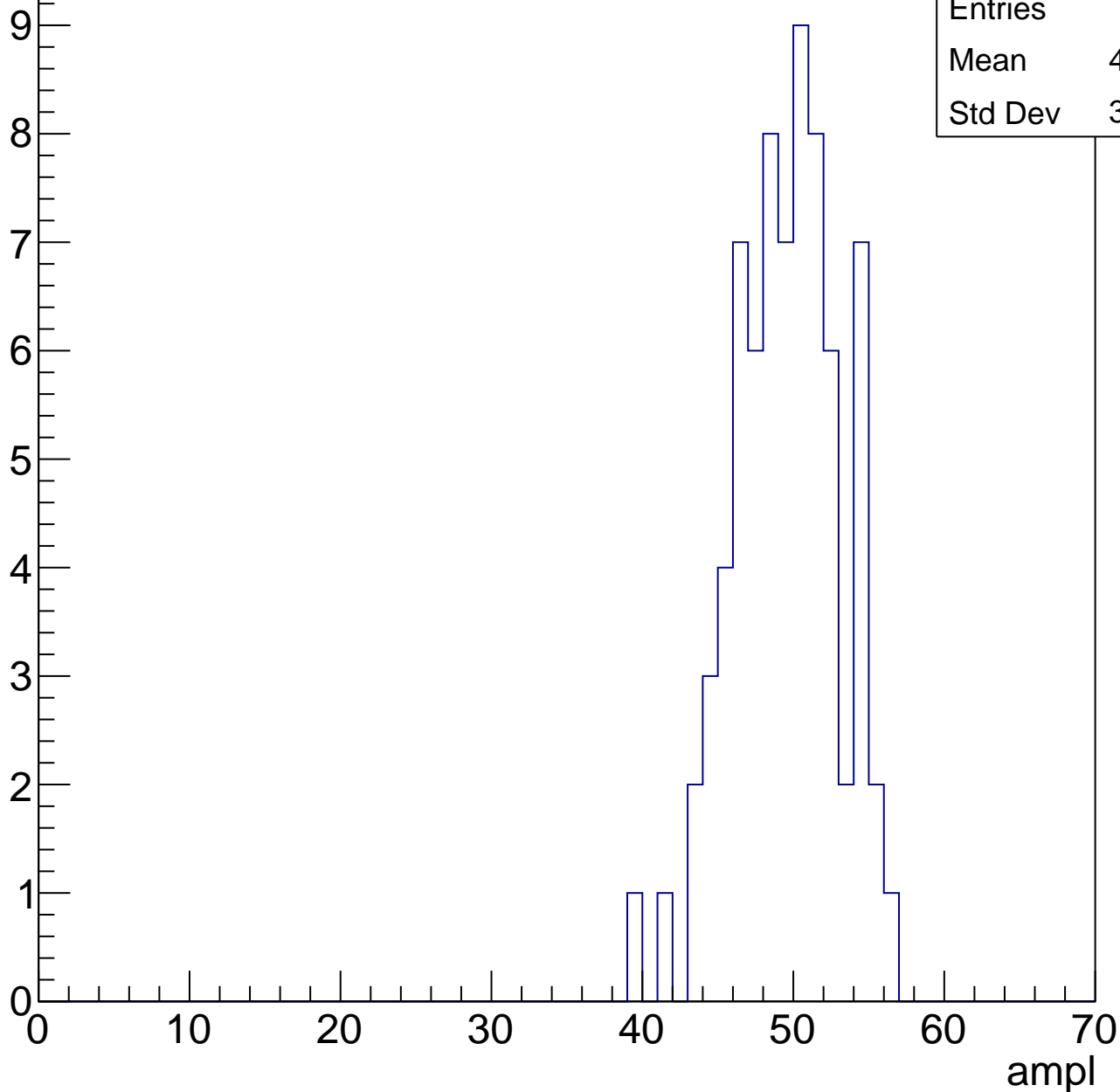


# B0L001S, U21-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	74
Mean	49.04
Std Dev	3.474

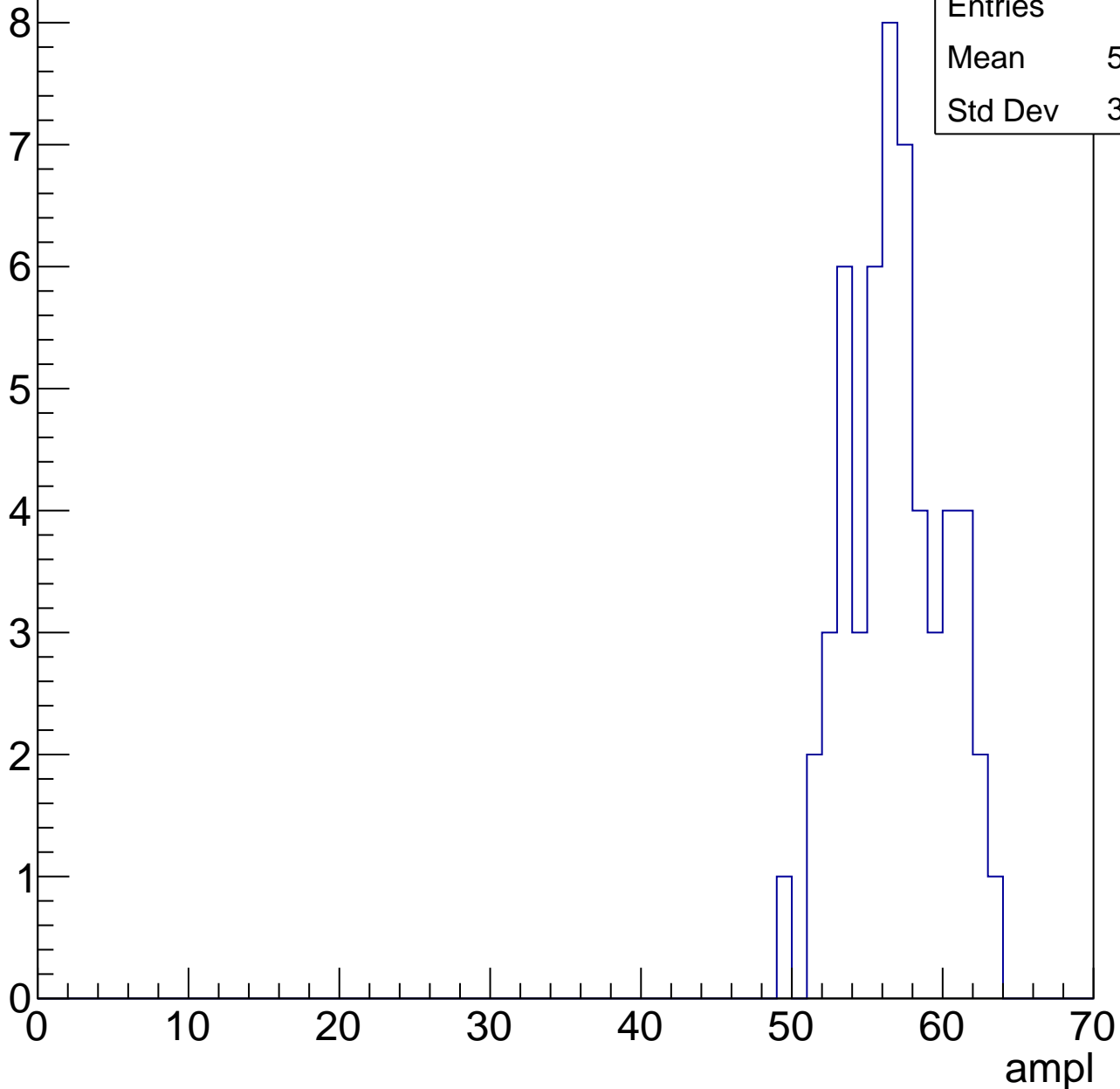


# B0L001S, U21-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	54
Mean	56.37
Std Dev	3.182

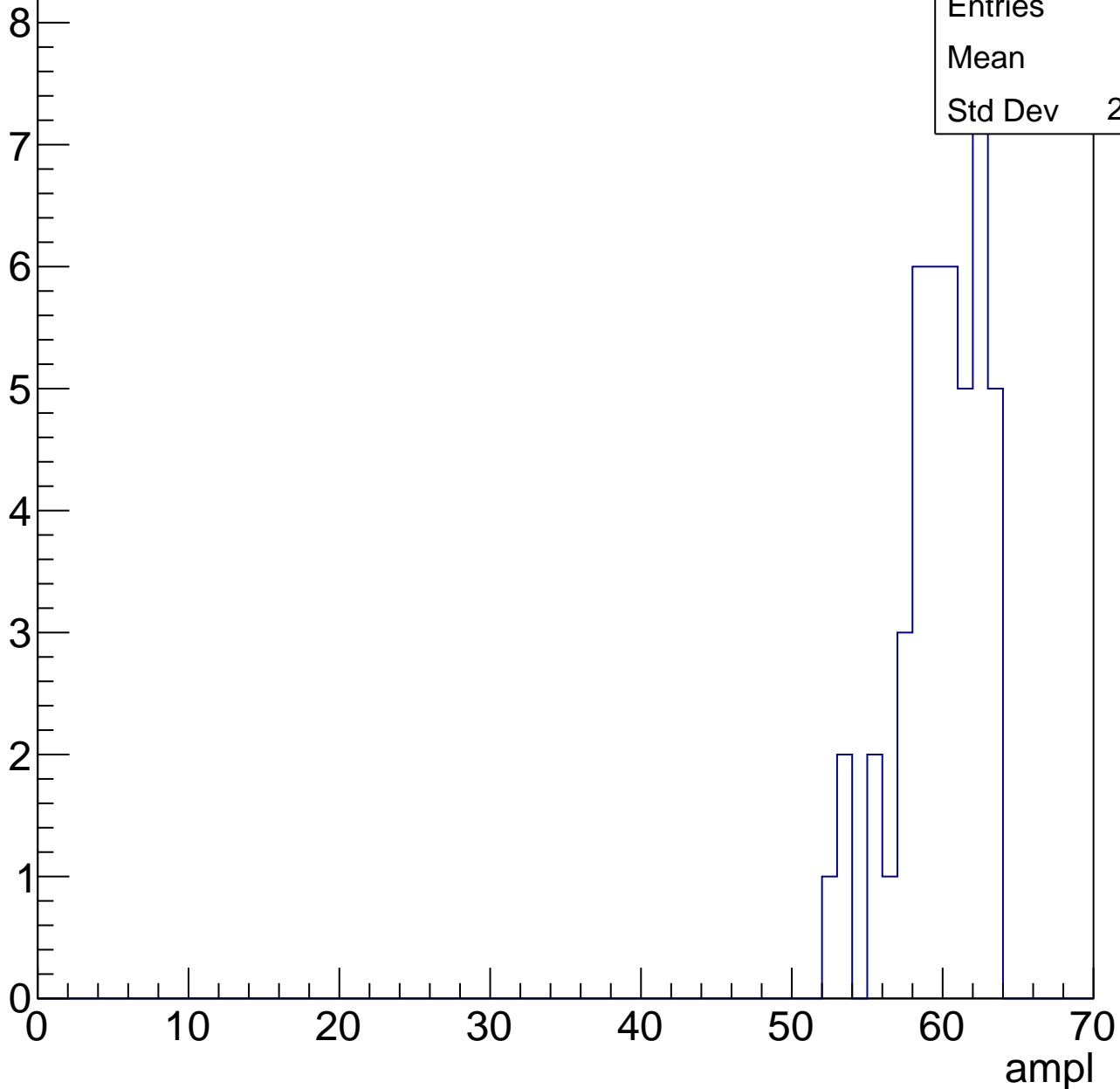


# B0L001S, U21-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

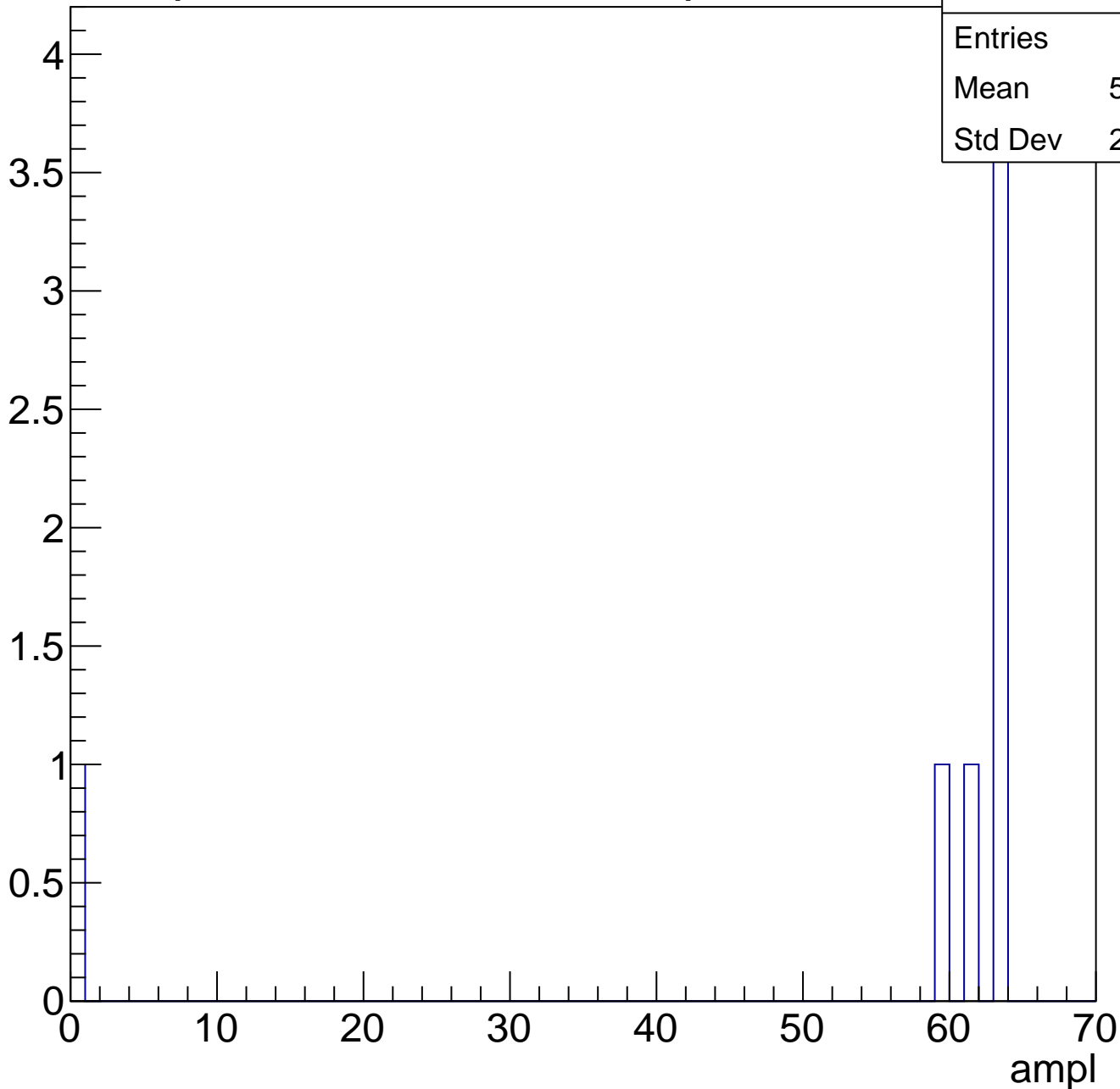
Entries	45
Mean	59.4
Std Dev	2.792



# B0L001S, U21-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	0
Mean	0
Std Dev	0

# B0L001S, U21-ch126, adc0

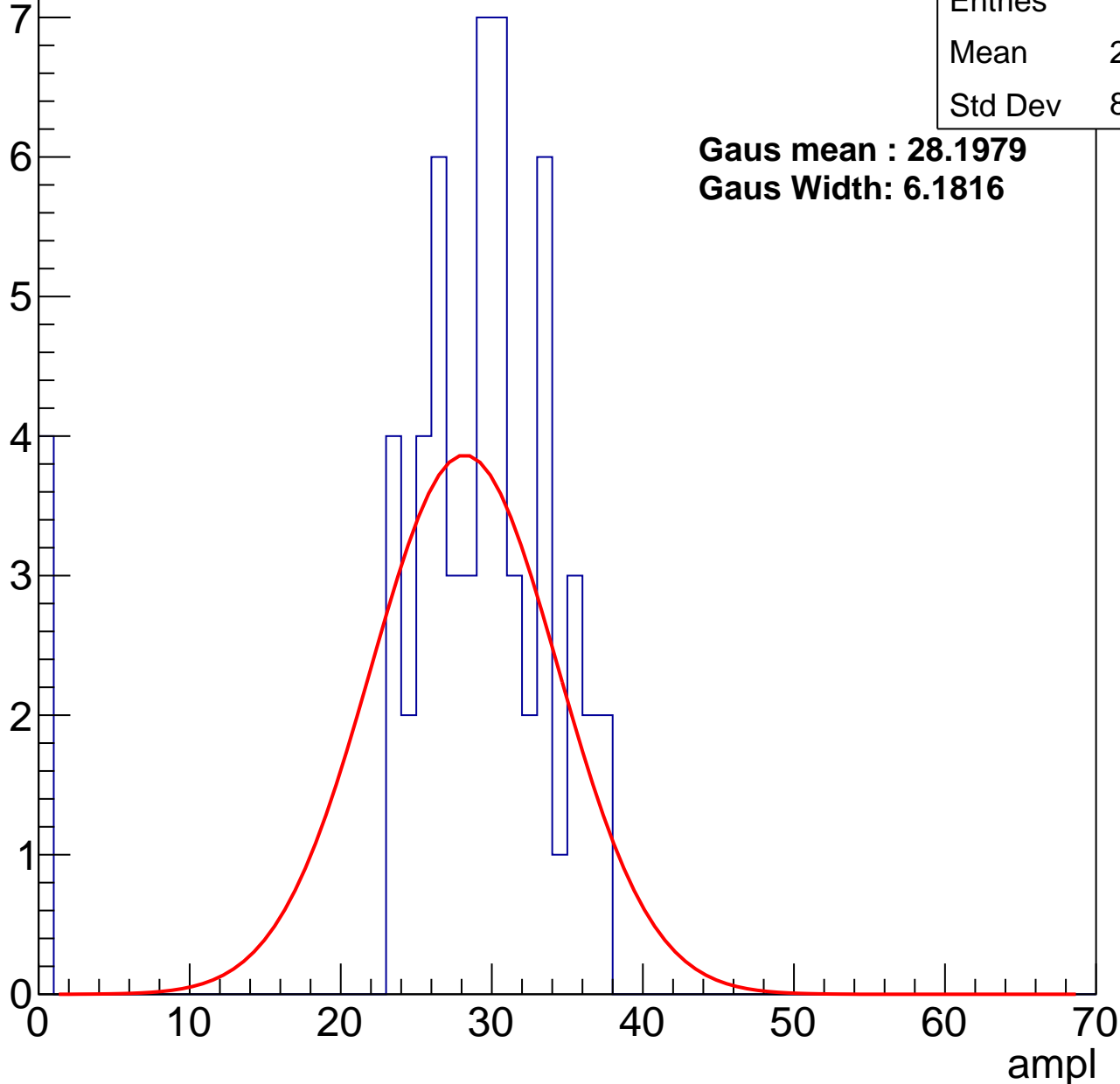
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	59
Mean	27.36
Std Dev	8.258

**Gaus mean : 28.1979**

**Gaus Width: 6.1816**



# B0L001S, U21-ch126, adc1

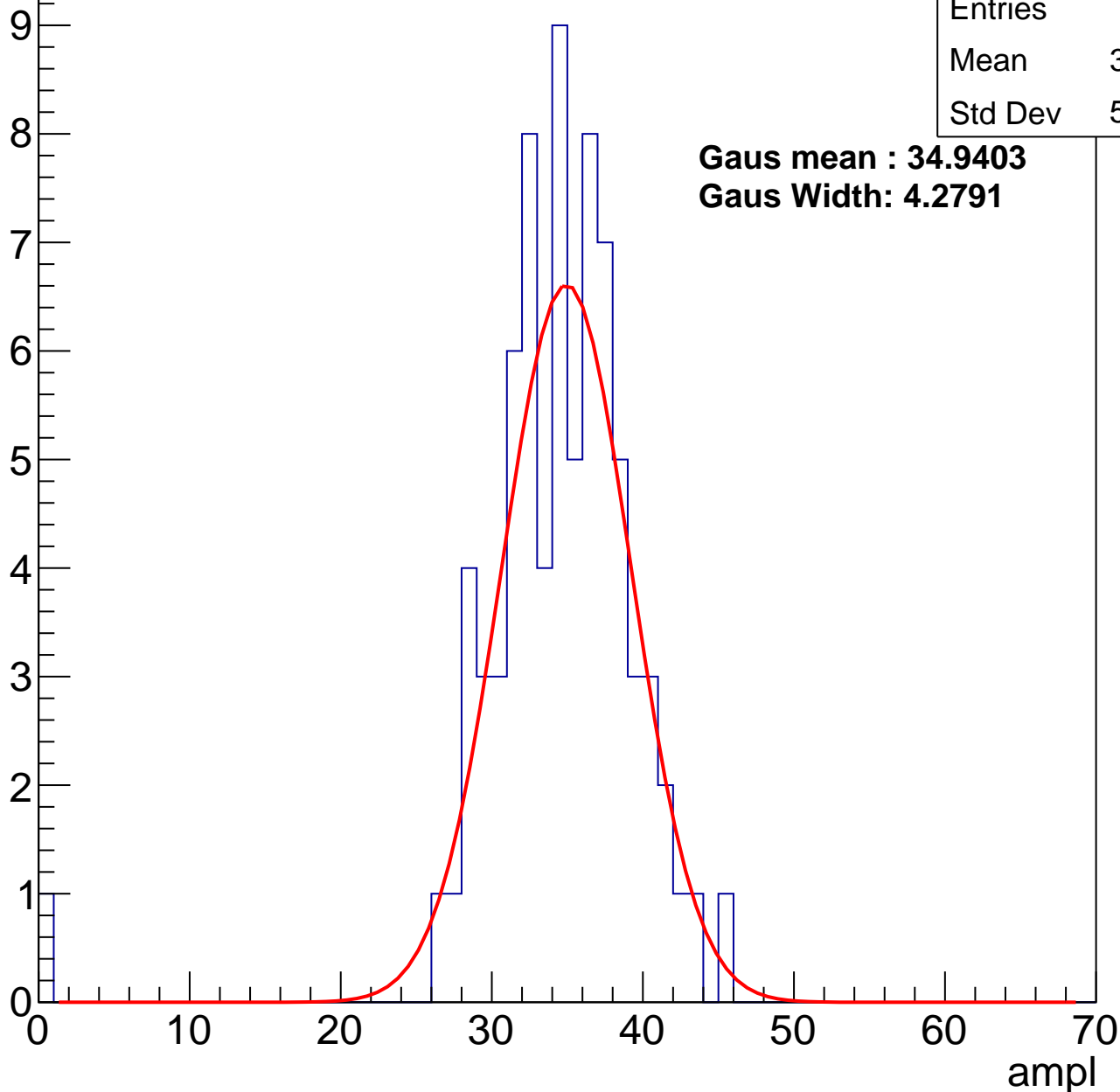
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	76
Mean	33.99
Std Dev	5.564

**Gaus mean : 34.9403**

**Gaus Width: 4.2791**



# B0L001S, U21-ch126, adc2

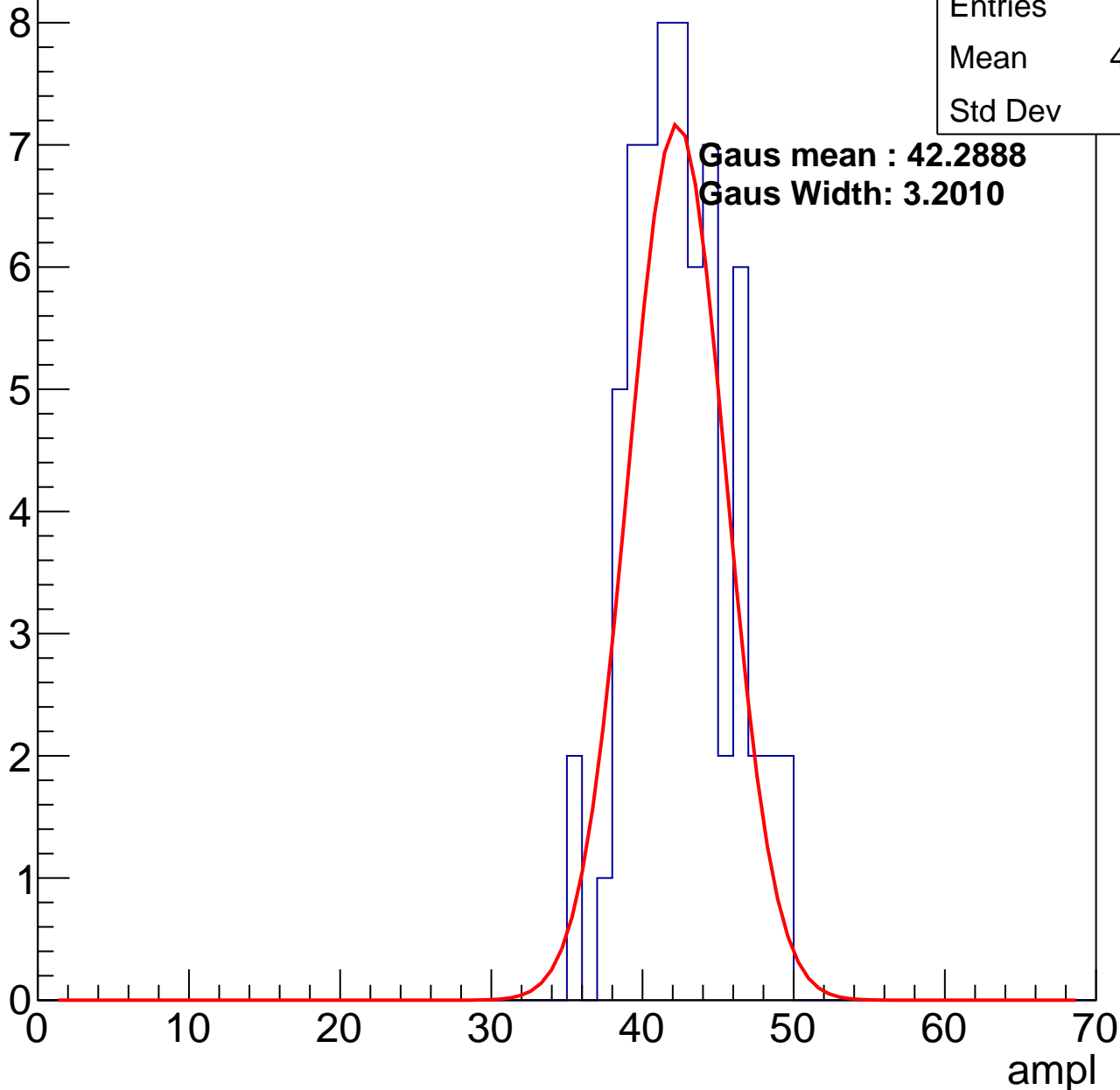
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	65
Mean	42.06
Std Dev	3.21

**Gaus mean : 42.2888**

**Gaus Width: 3.2010**

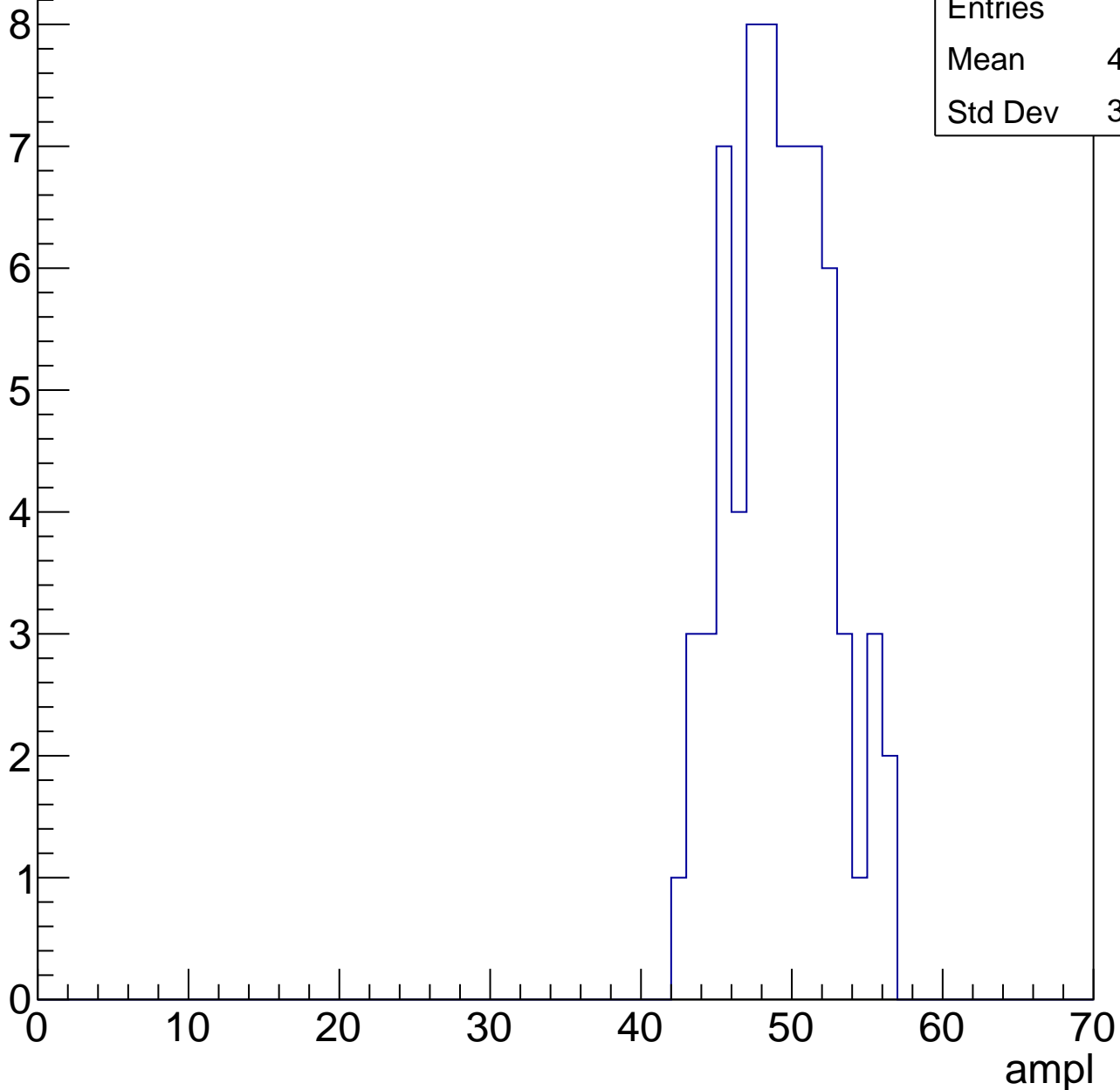


# B0L001S, U21-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	70
Mean	48.77
Std Dev	3.347

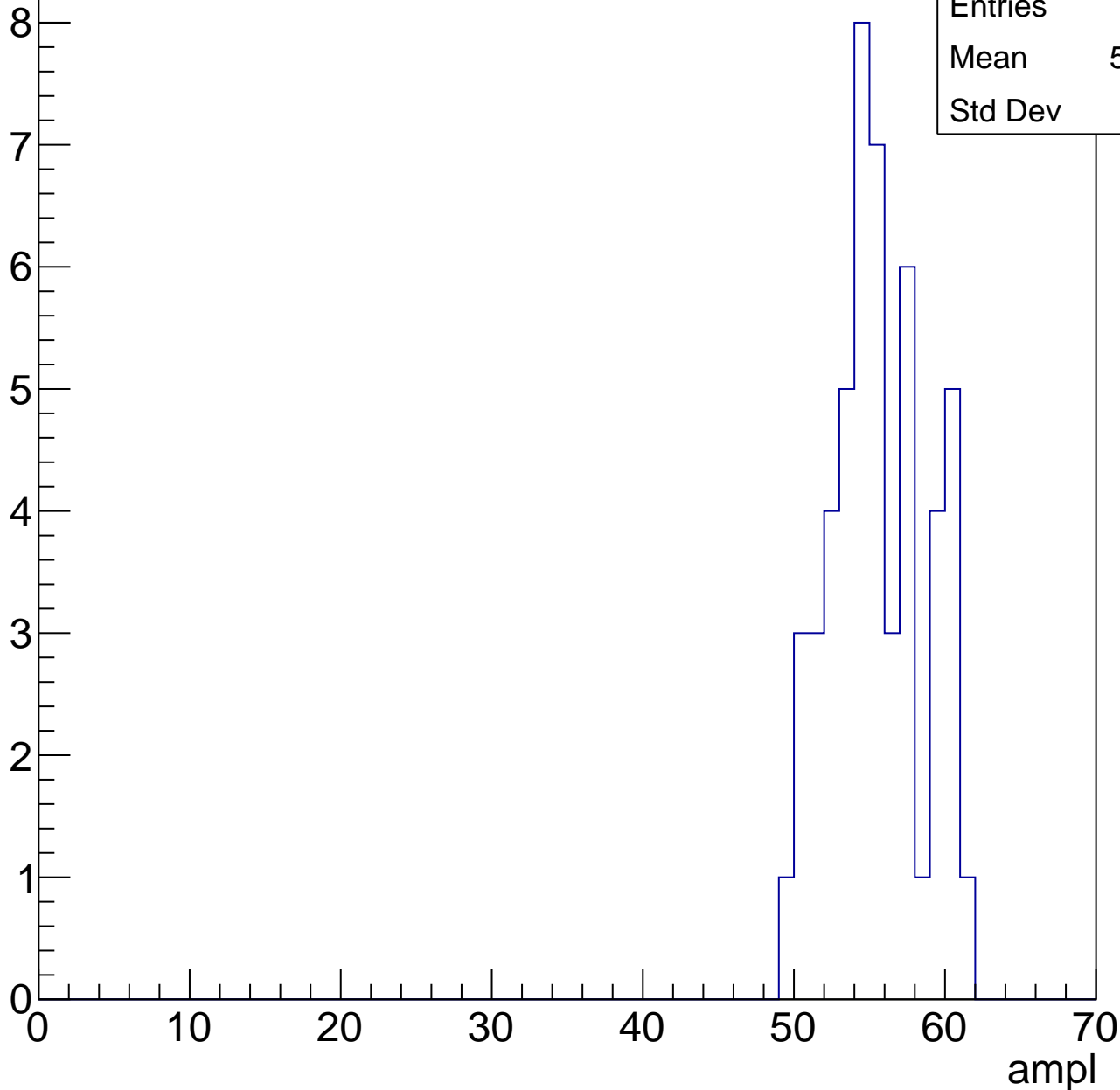


# B0L001S, U21-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	51
Mean	55.04
Std Dev	3.08

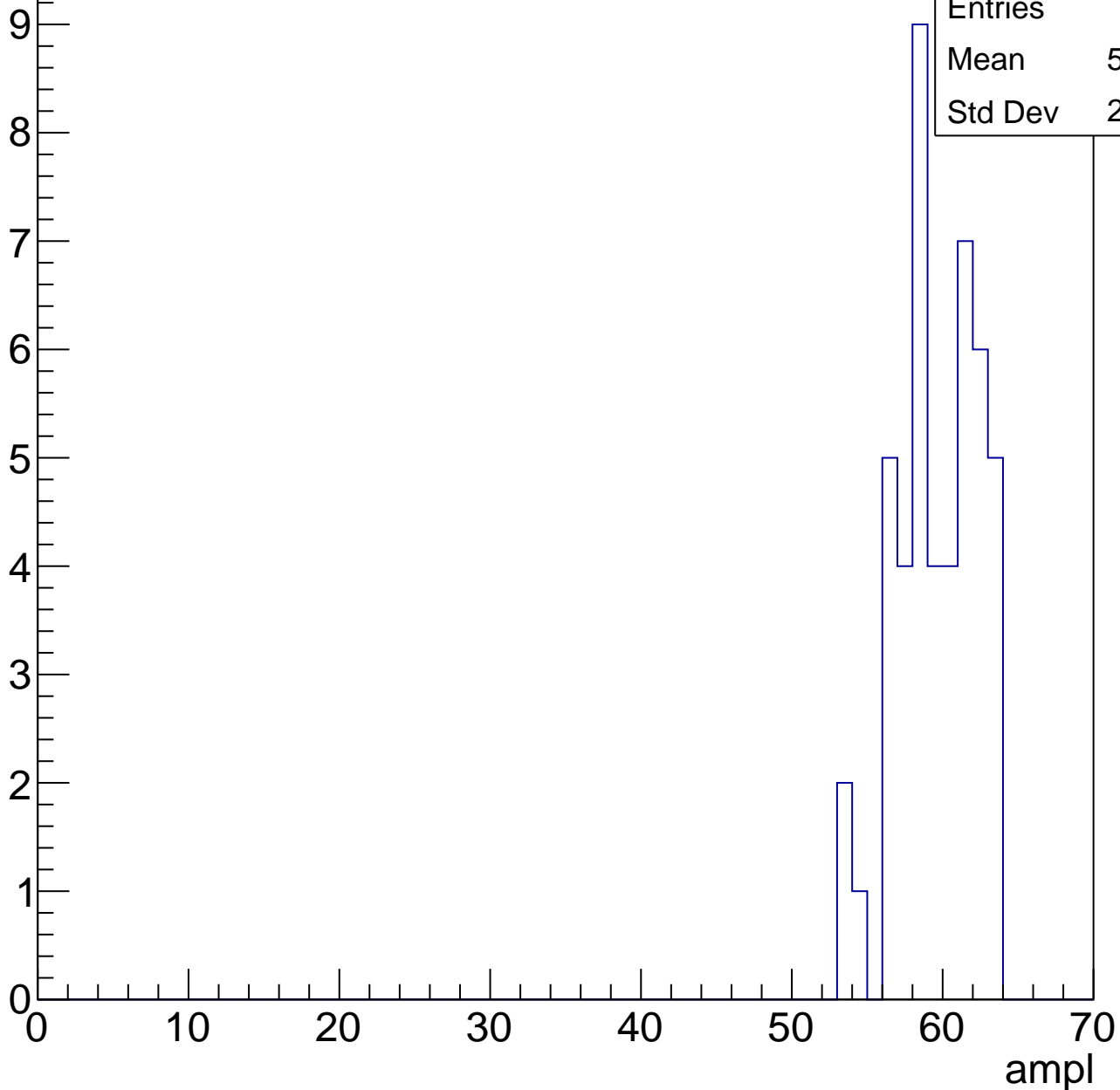


# B0L001S, U21-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	47
Mean	59.15
Std Dev	2.658

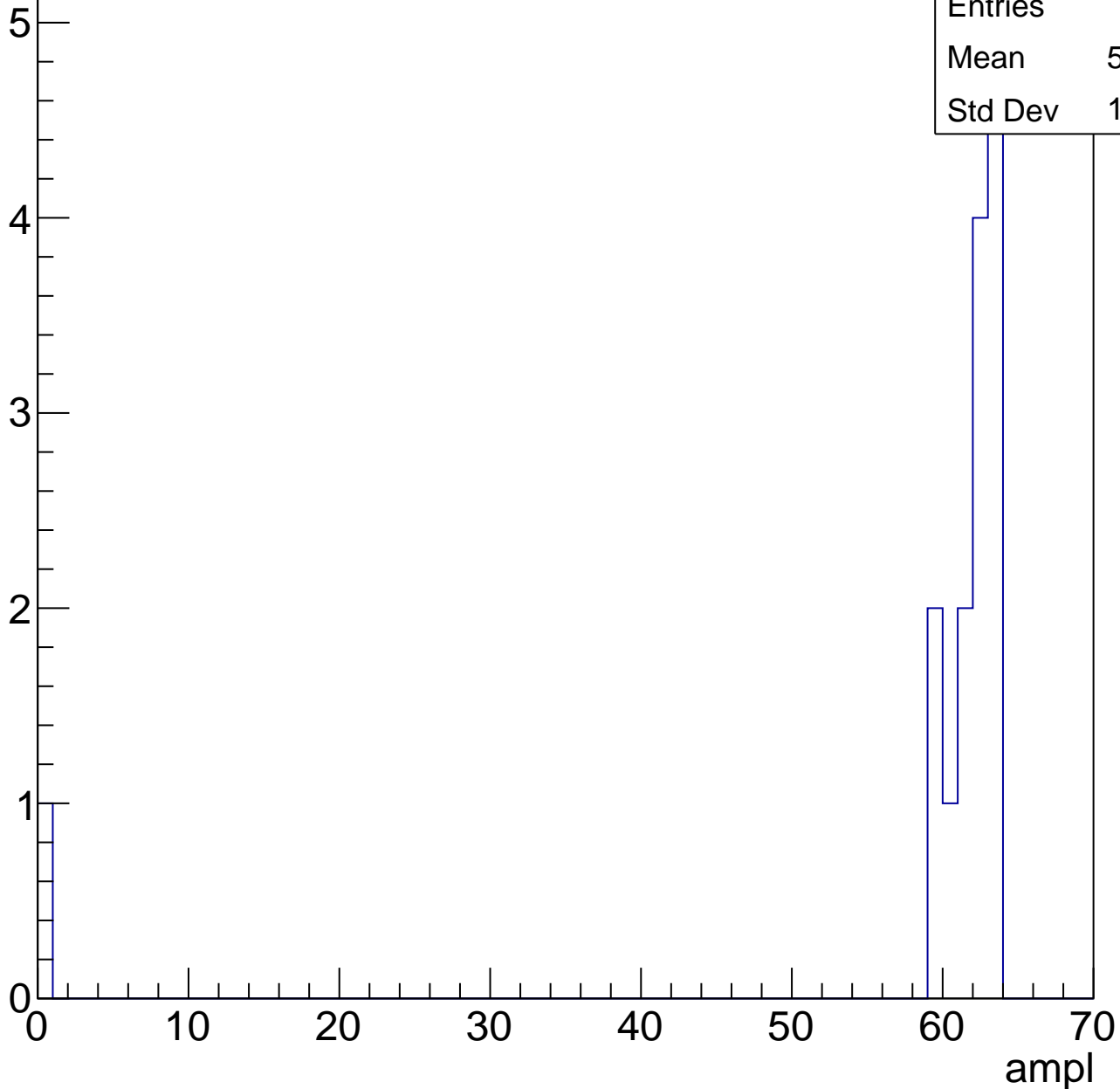


# B0L001S, U21-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	15
Mean	57.53
Std Dev	15.44





# B0L001S, U21-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



# B0L001S, U21-ch127, adc0

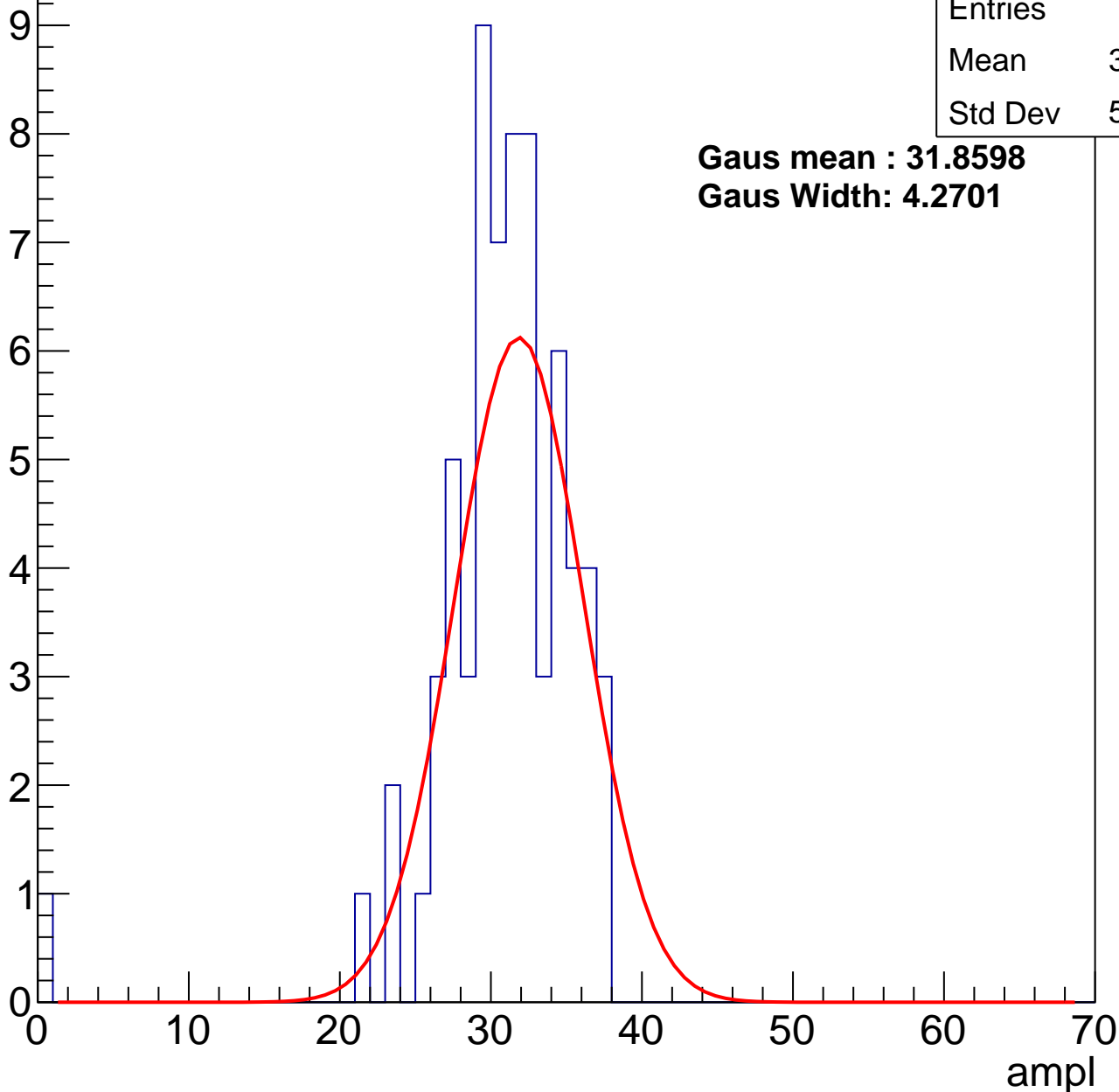
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	68
Mean	30.32
Std Dev	5.095

**Gaus mean : 31.8598**

**Gaus Width: 4.2701**



# B0L001S, U21-ch127, adc1

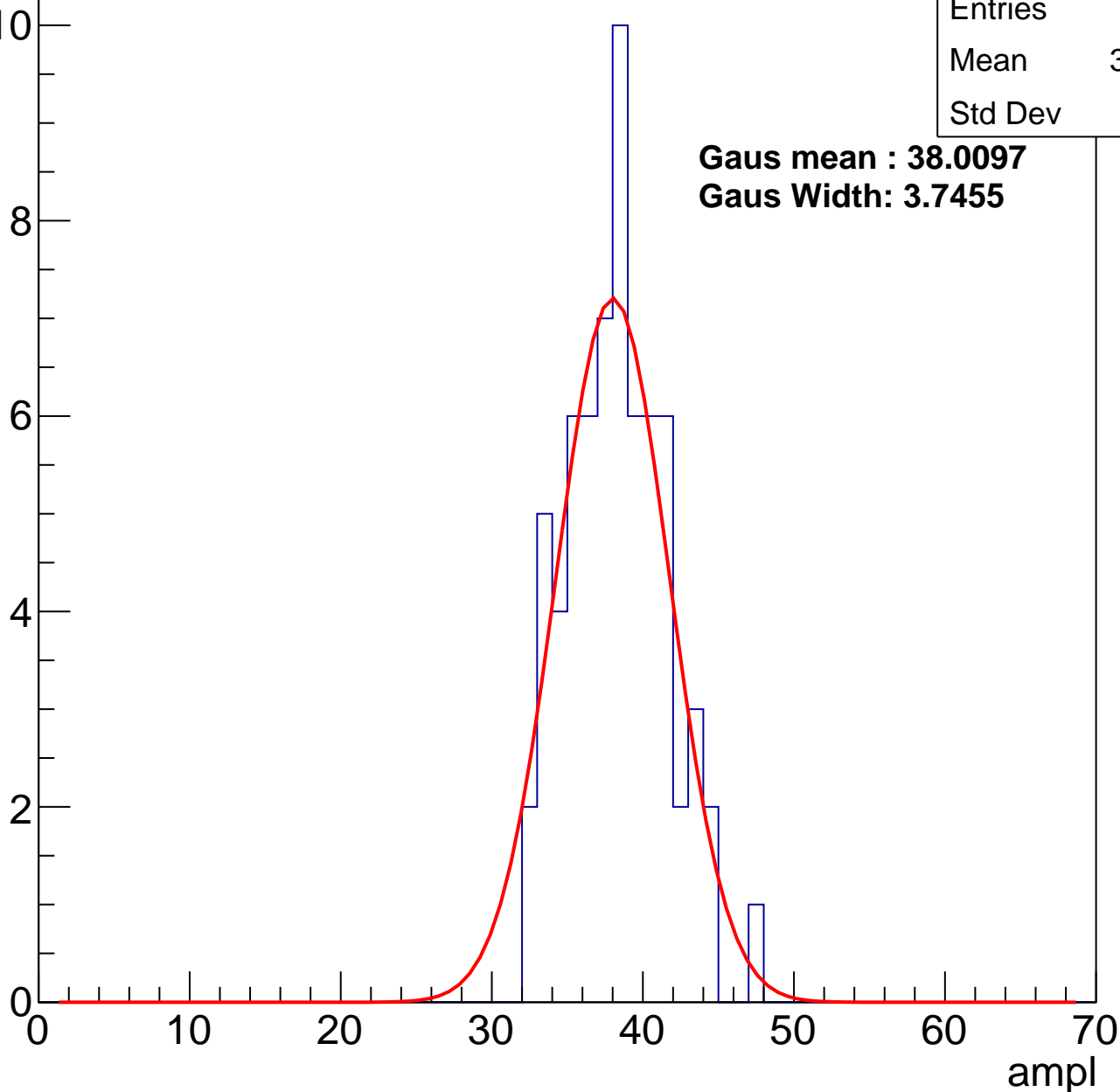
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	37.85
Std Dev	3.23

**Gaus mean : 38.0097**

**Gaus Width: 3.7455**



# B0L001S, U21-ch127, adc2

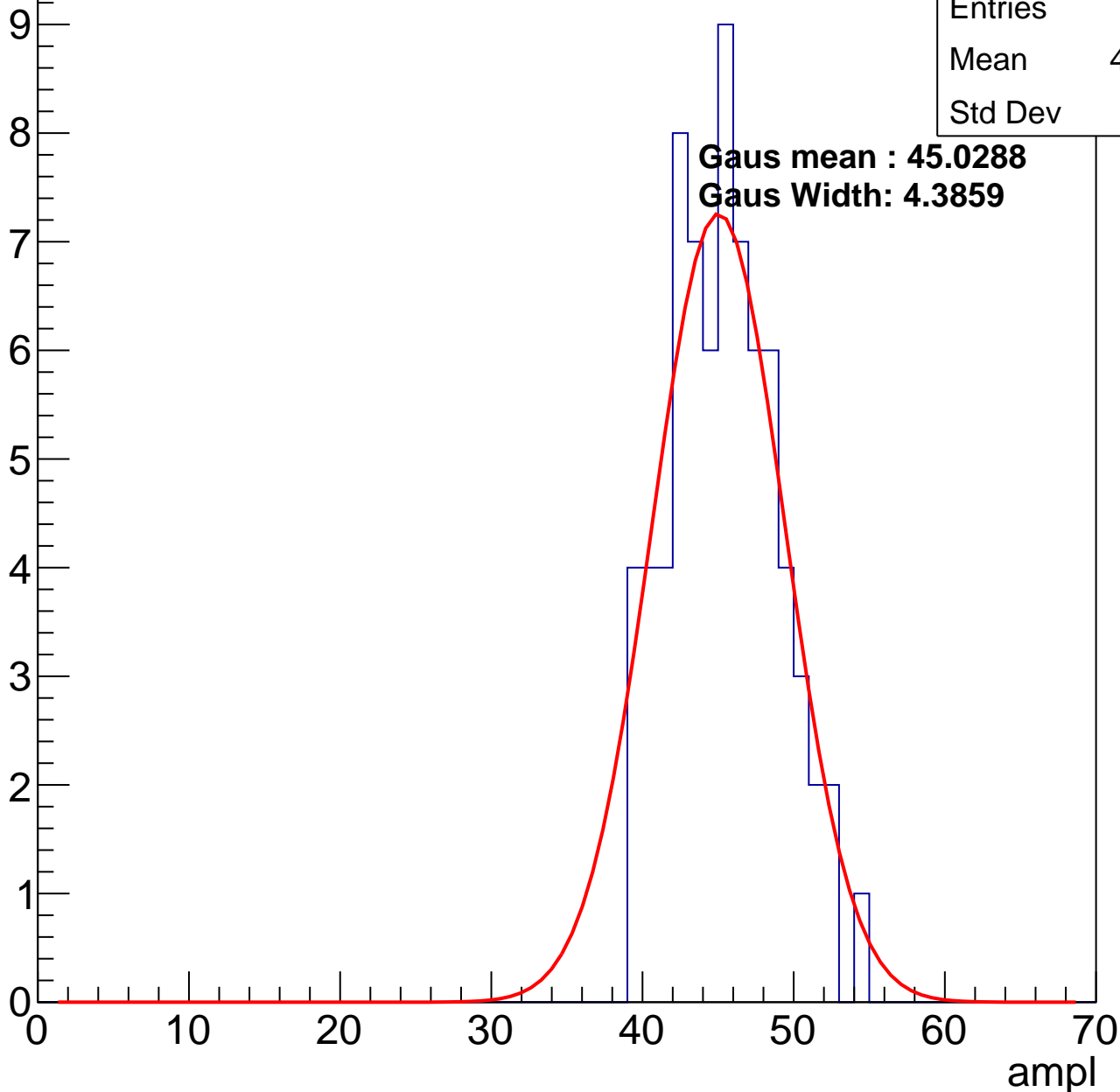
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	73
Mean	44.99
Std Dev	3.49

**Gaus mean : 45.0288**

**Gaus Width: 4.3859**

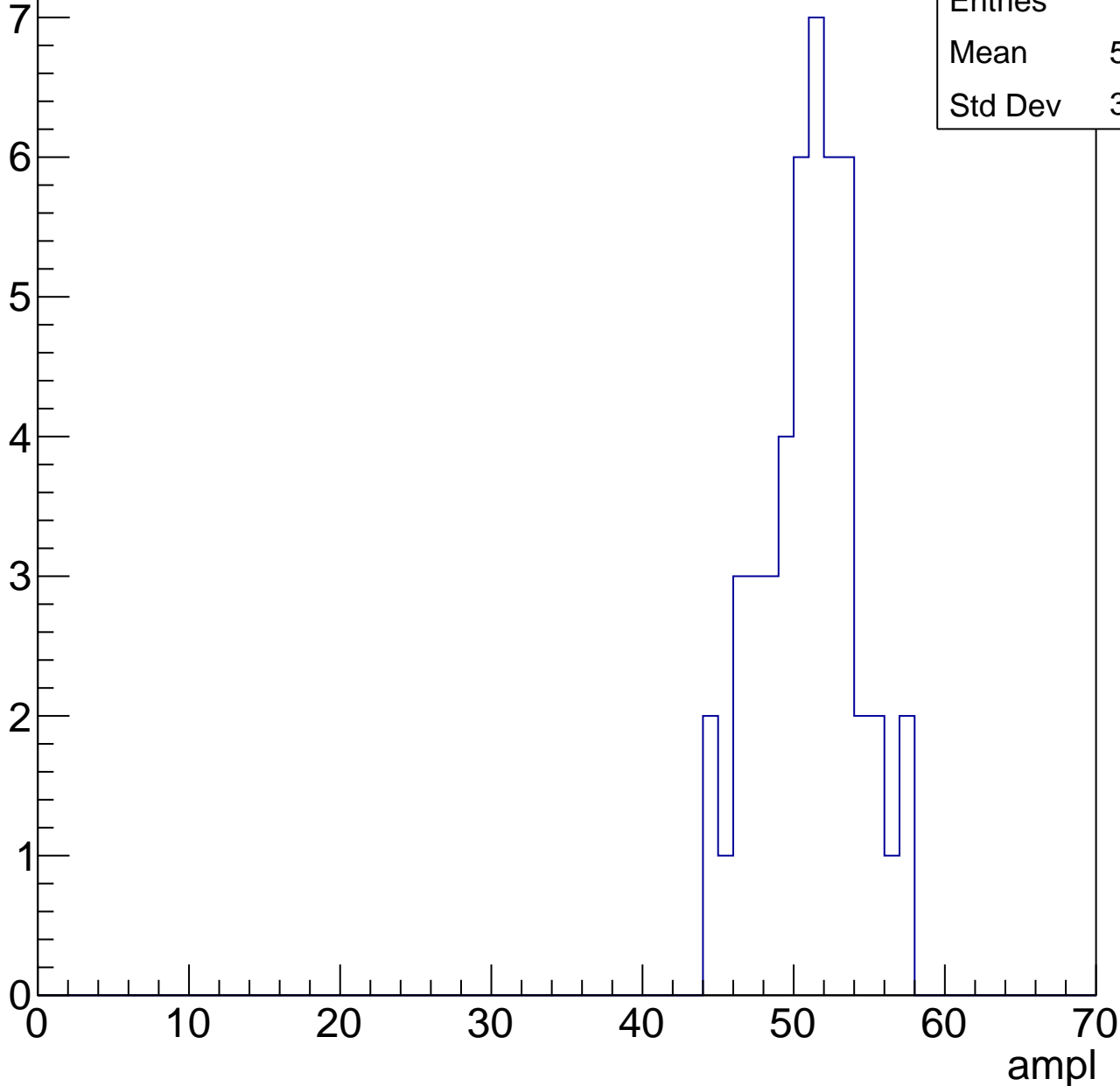


# B0L001S, U21-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	48
Mean	50.56
Std Dev	3.142

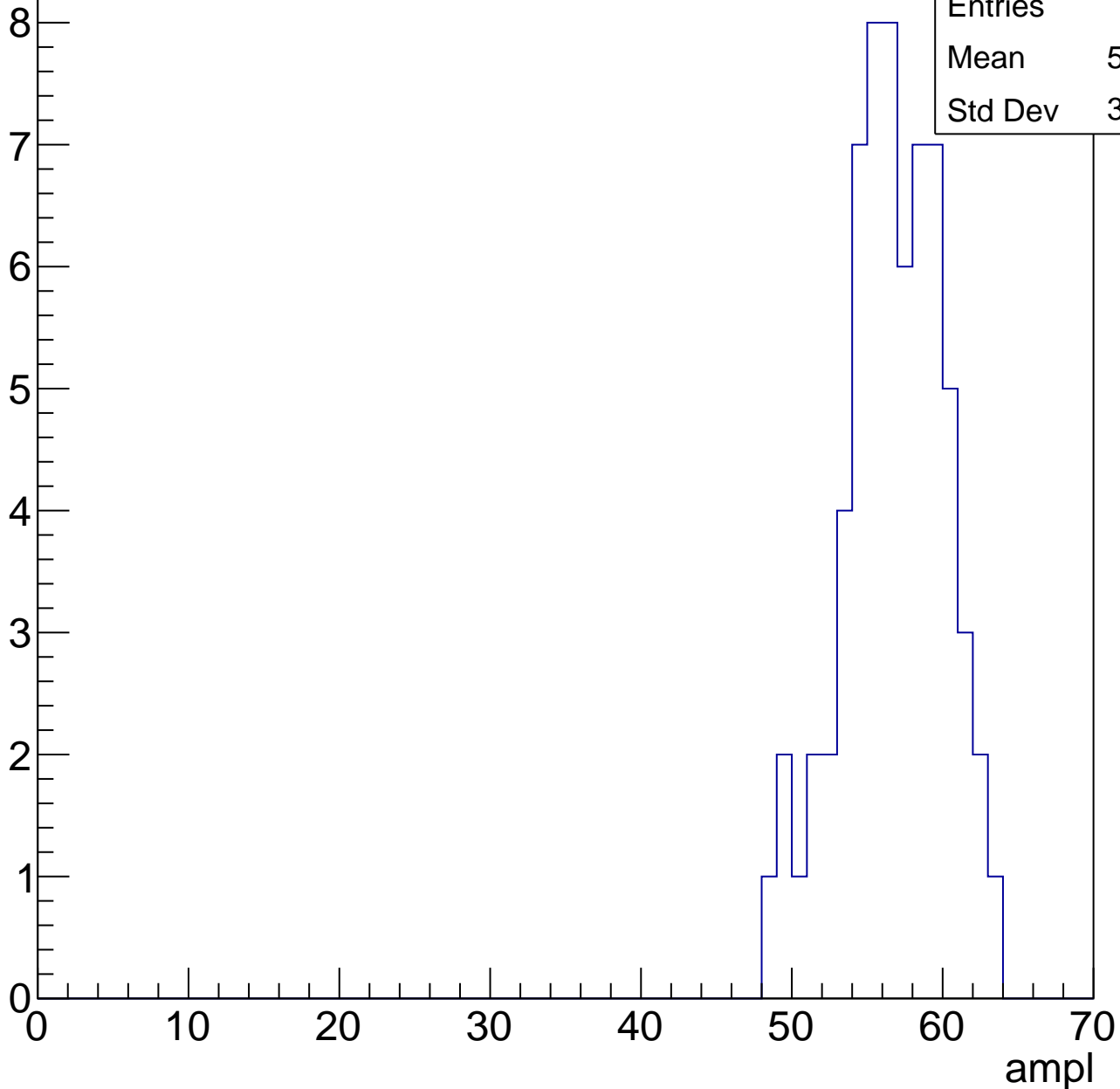


# B0L001S, U21-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	66
Mean	56.23
Std Dev	3.307

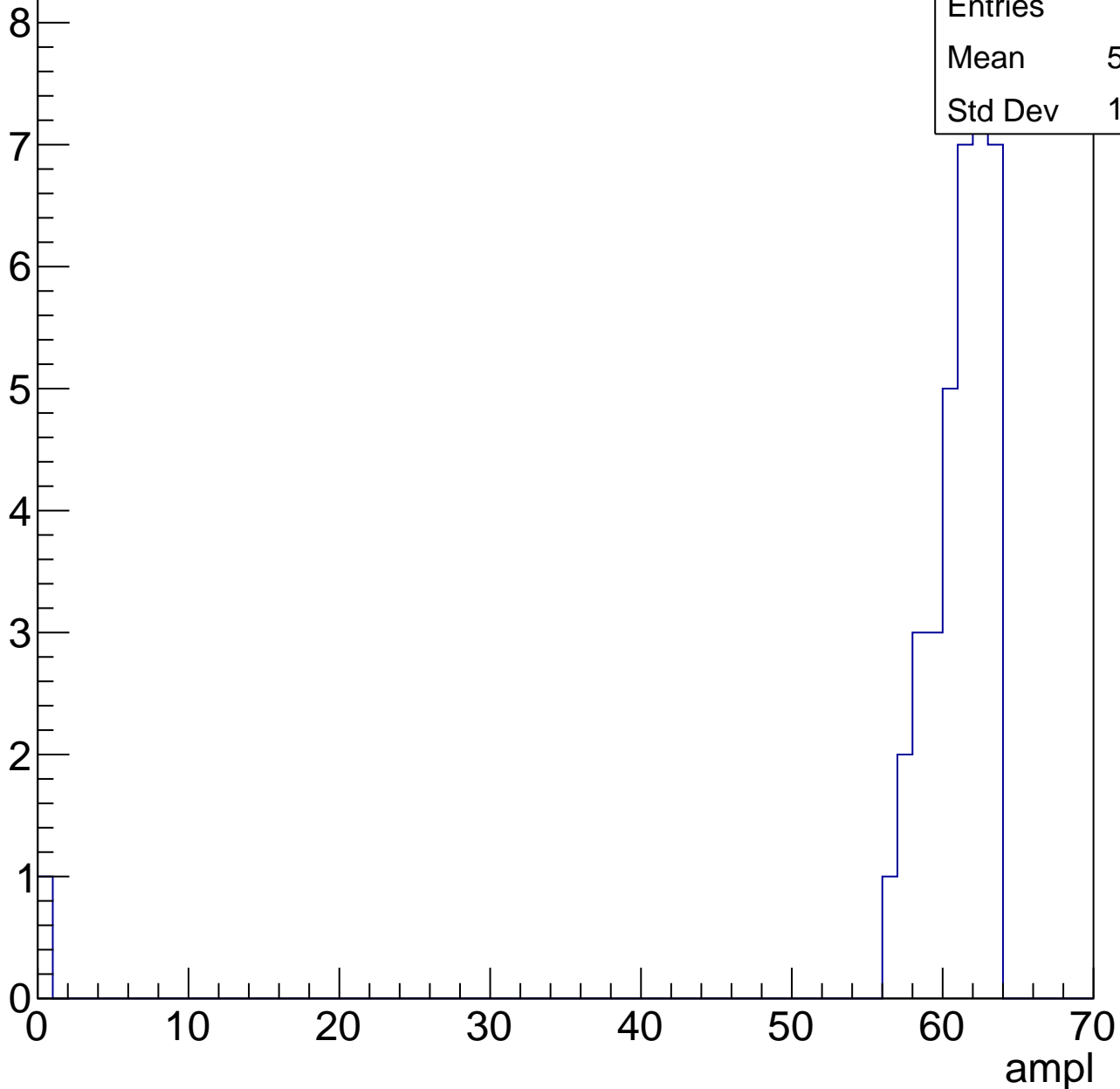


# B0L001S, U21-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

Entries	37
Mean	59.05
Std Dev	10.02



# B0L001S, U21-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry





# B0L001S, U21-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry

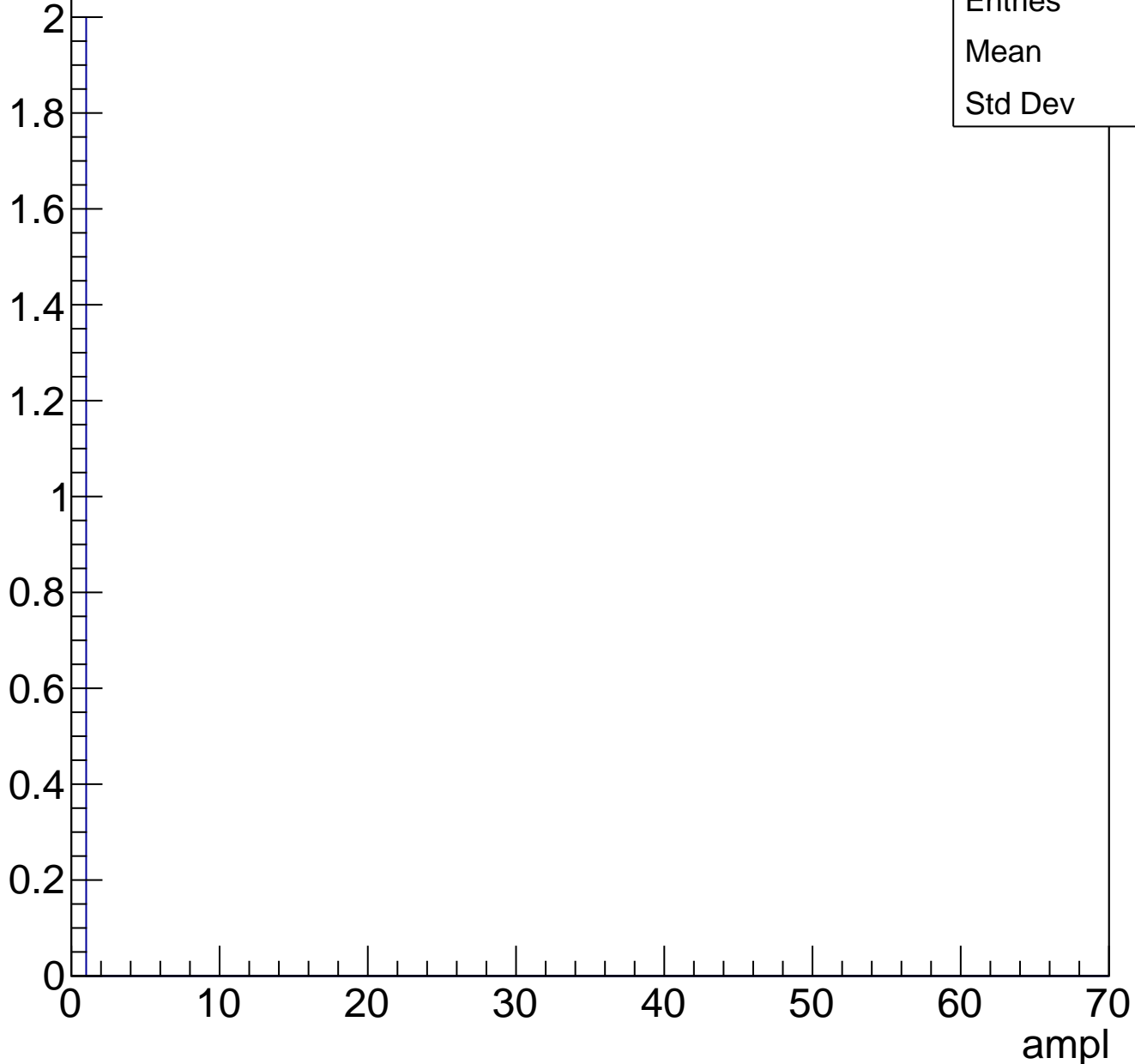


Entries	2
Mean	0
Std Dev	0

# B0L001S, U21-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entry



Entries	2
Mean	0
Std Dev	0