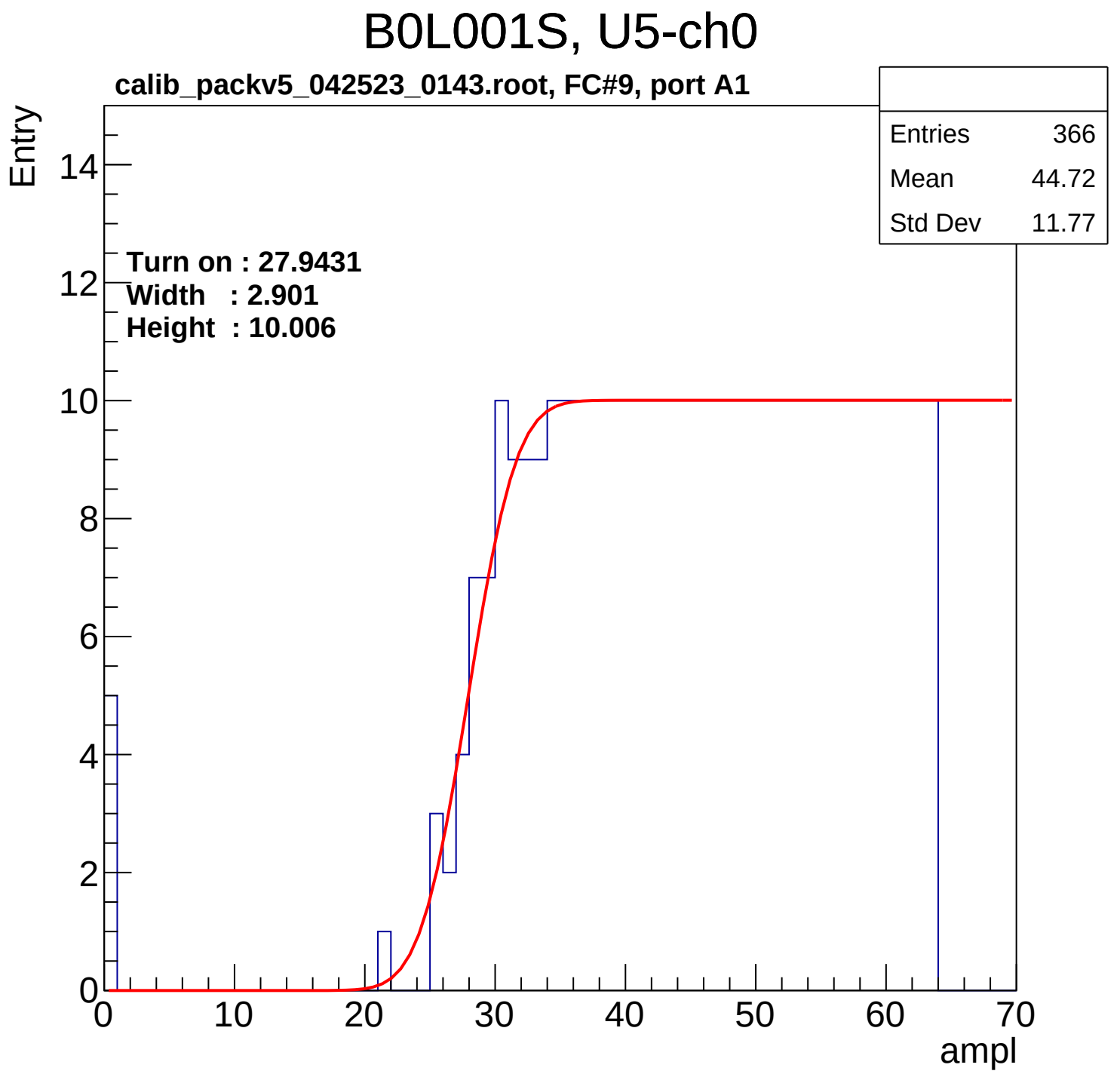
B0L001S, U5-ch0
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.72
Std Dev 11.77
Turn on : 27.9431
Width : 2.901
Height : 10.006
Entry
ampl
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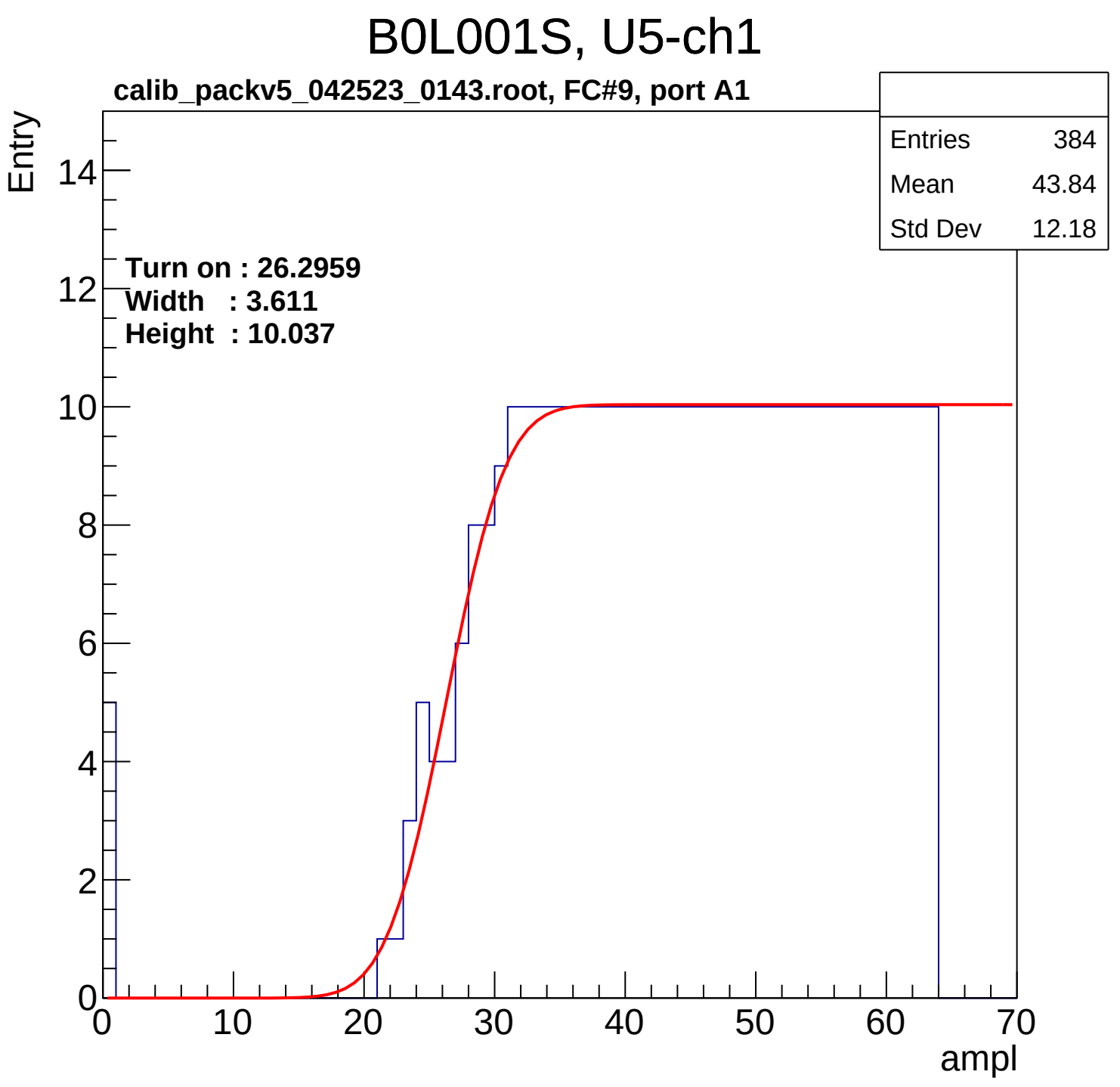
B0L001S, U5-ch1
calib_packv5_042523_0143.root, FC#9, port A1
Entries 384
Mean 43.84
Std Dev 12.18
Turn on : 26.2959
Width : 3.611
Height : 10.037
Entry
ampl
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2
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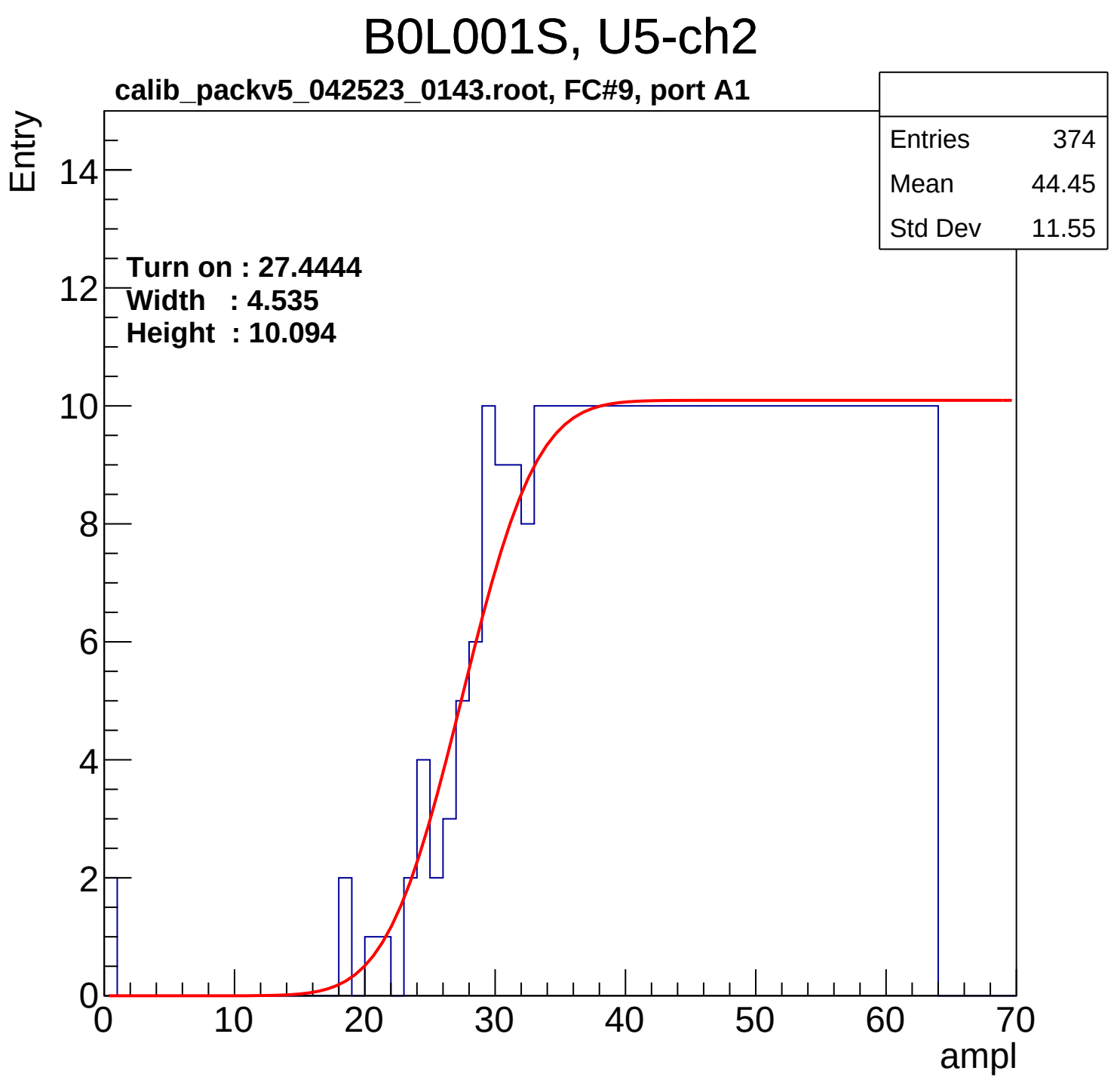
B0L001S, U5-ch2
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.45
Std Dev 11.55
Turn on : 27.4444
Width : 4.535
Height : 10.094
Entry
ampl
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2
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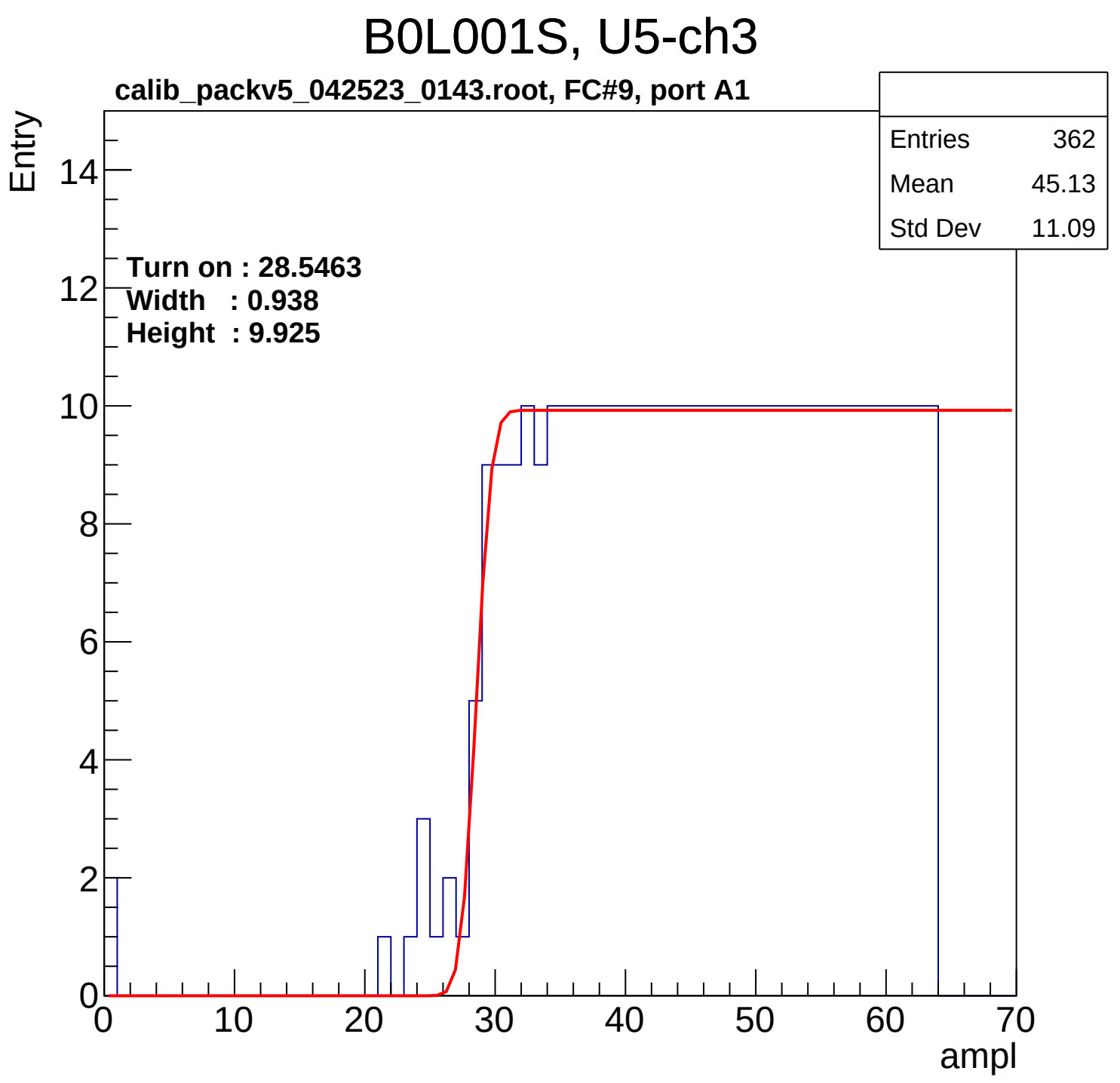
B0L001S, U5-ch3
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.13
Std Dev 11.09
Turn on : 28.5463
Width : 0.938
Height : 9.925
Entry
ampl
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2
4
6
8
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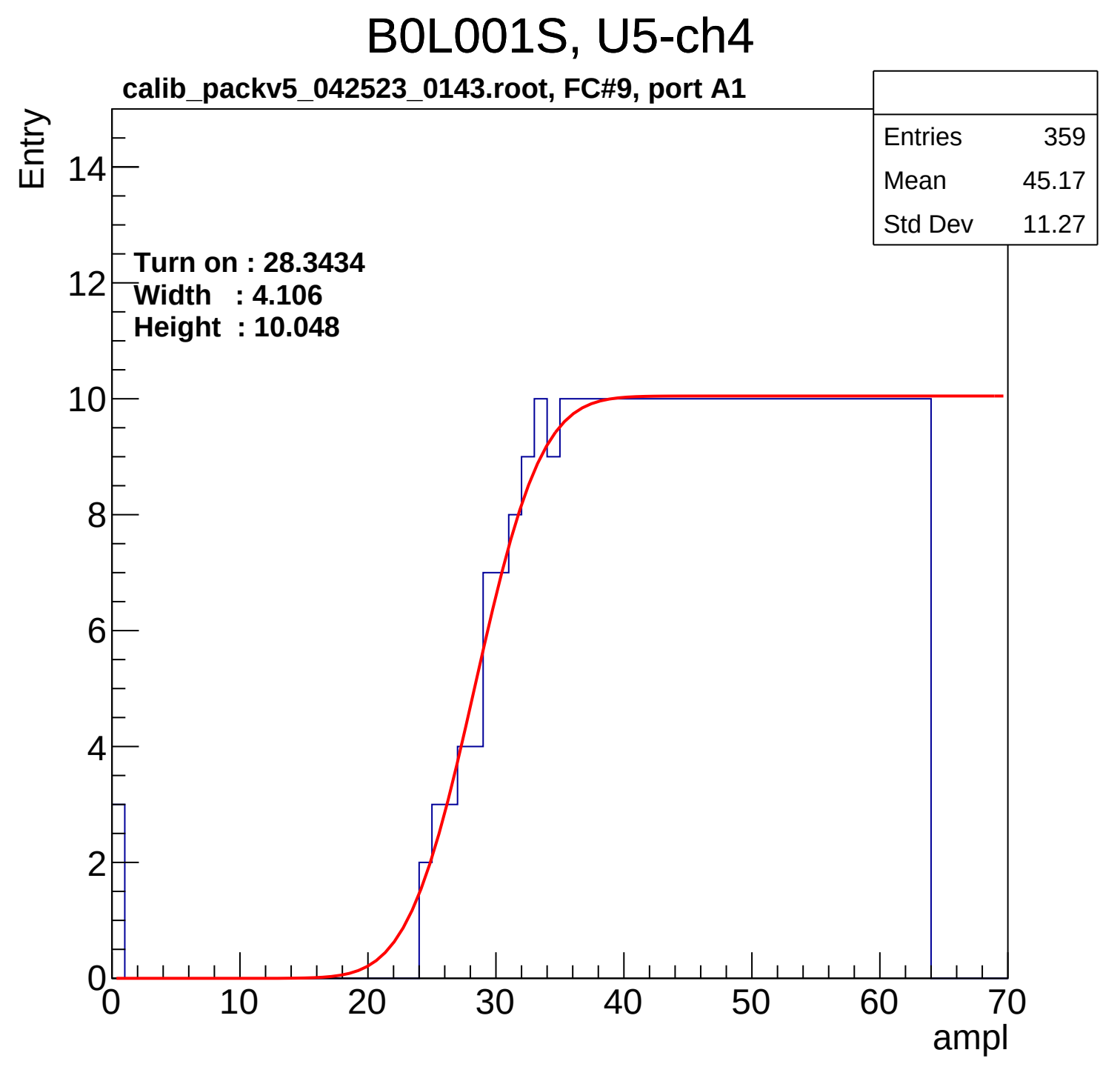
B0L001S, U5-ch4
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.17
Std Dev 11.27
Turn on : 28.3434
Width : 4.106
Height : 10.048
Entry
ampl
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2
4
6
8
10
12
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0
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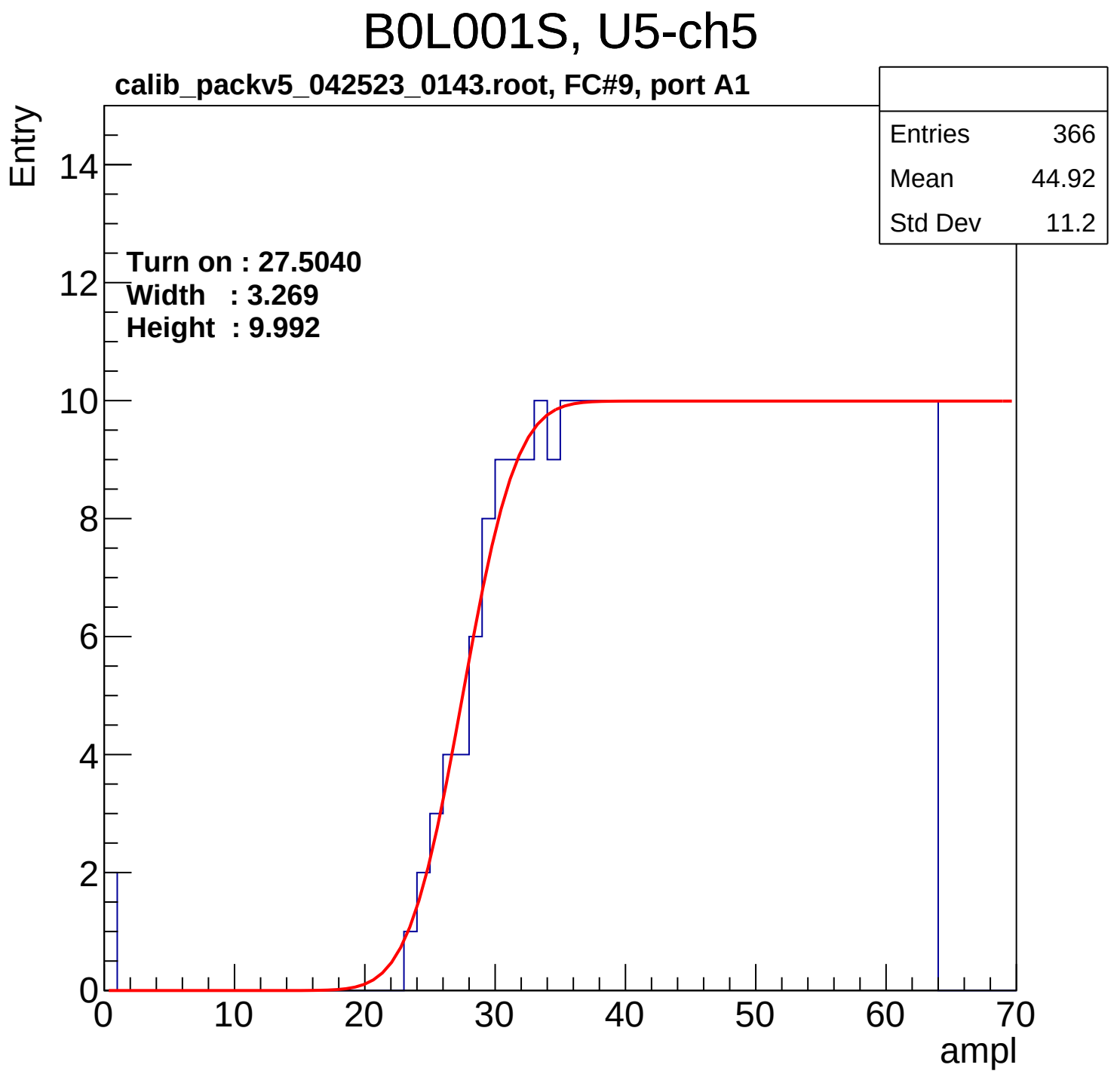
B0L001S, U5-ch5
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.92
Std Dev 11.2
Turn on : 27.5040
Width : 3.269
Height : 9.992
Entry
ampl
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2
4
6
8
10
12
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0
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60
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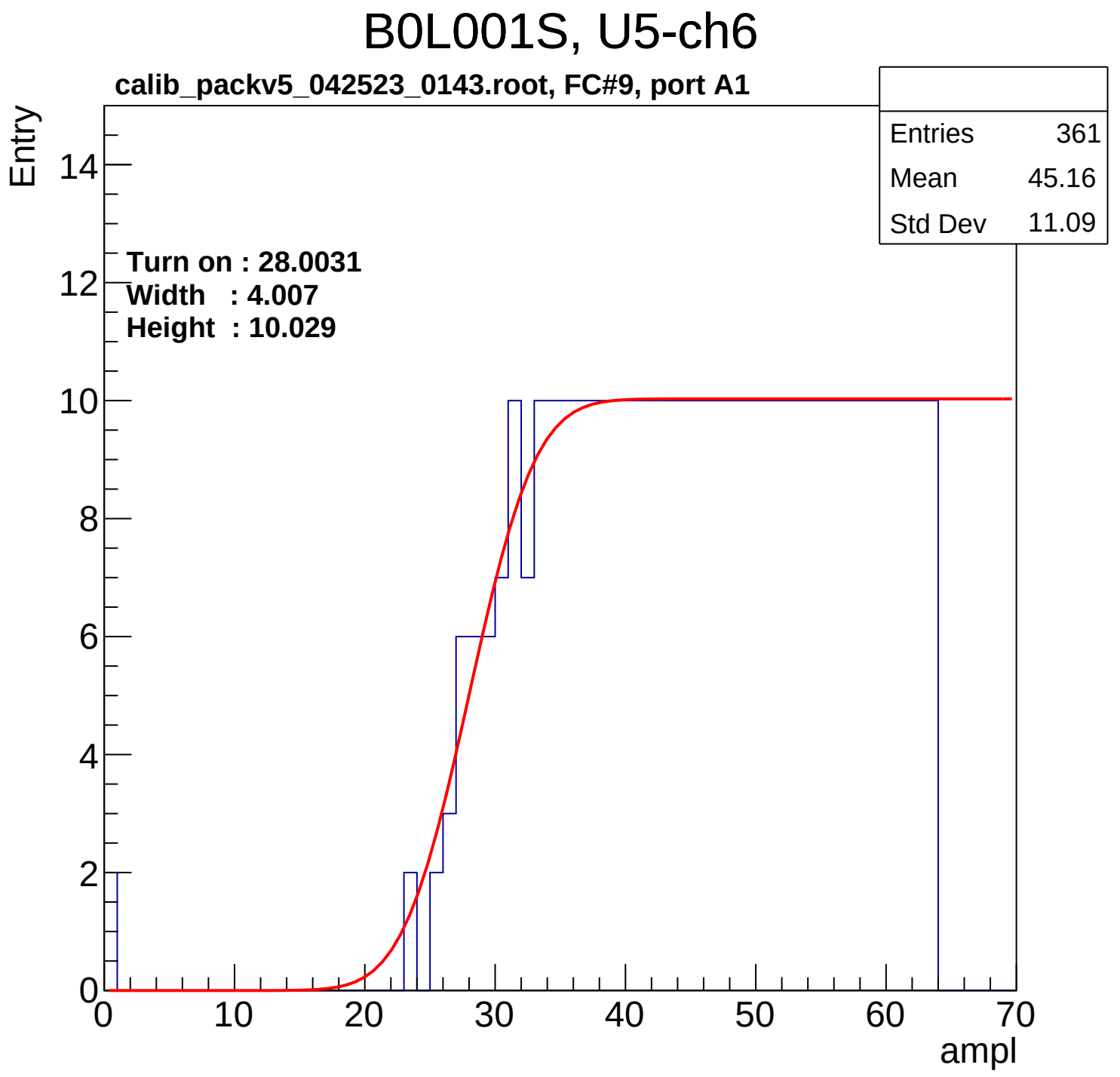
B0L001S, U5-ch6
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.16
Std Dev 11.09
Turn on : 28.0031
Width : 4.007
Height : 10.029
Entry
ampl
0
2
4
6
8
10
12
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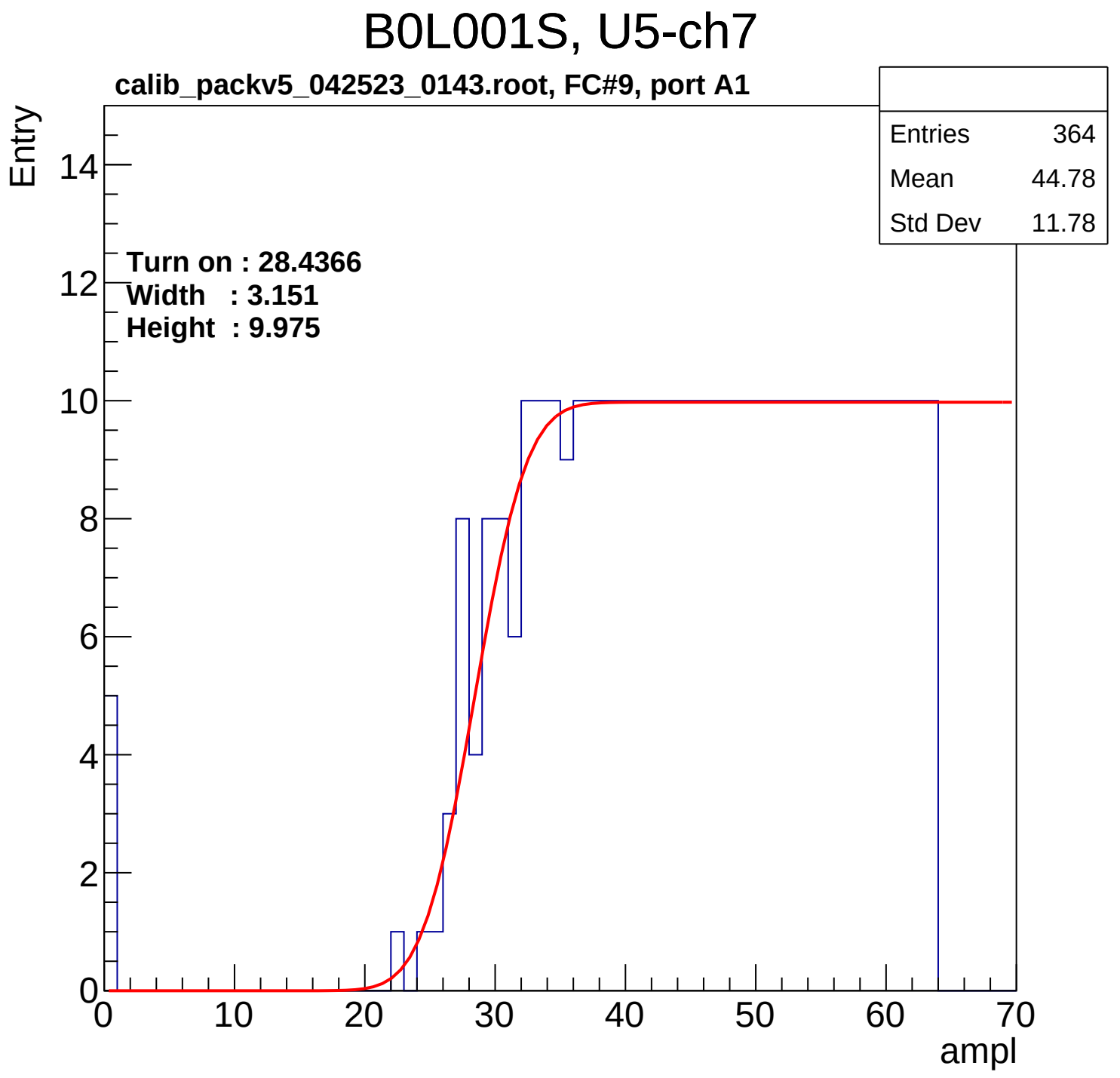
B0L001S, U5-ch7
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.78
Std Dev 11.78
Turn on : 28.4366
Width : 3.151
Height : 9.975
Entry
ampl
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4
6
8
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12
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0
10
20
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40
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60
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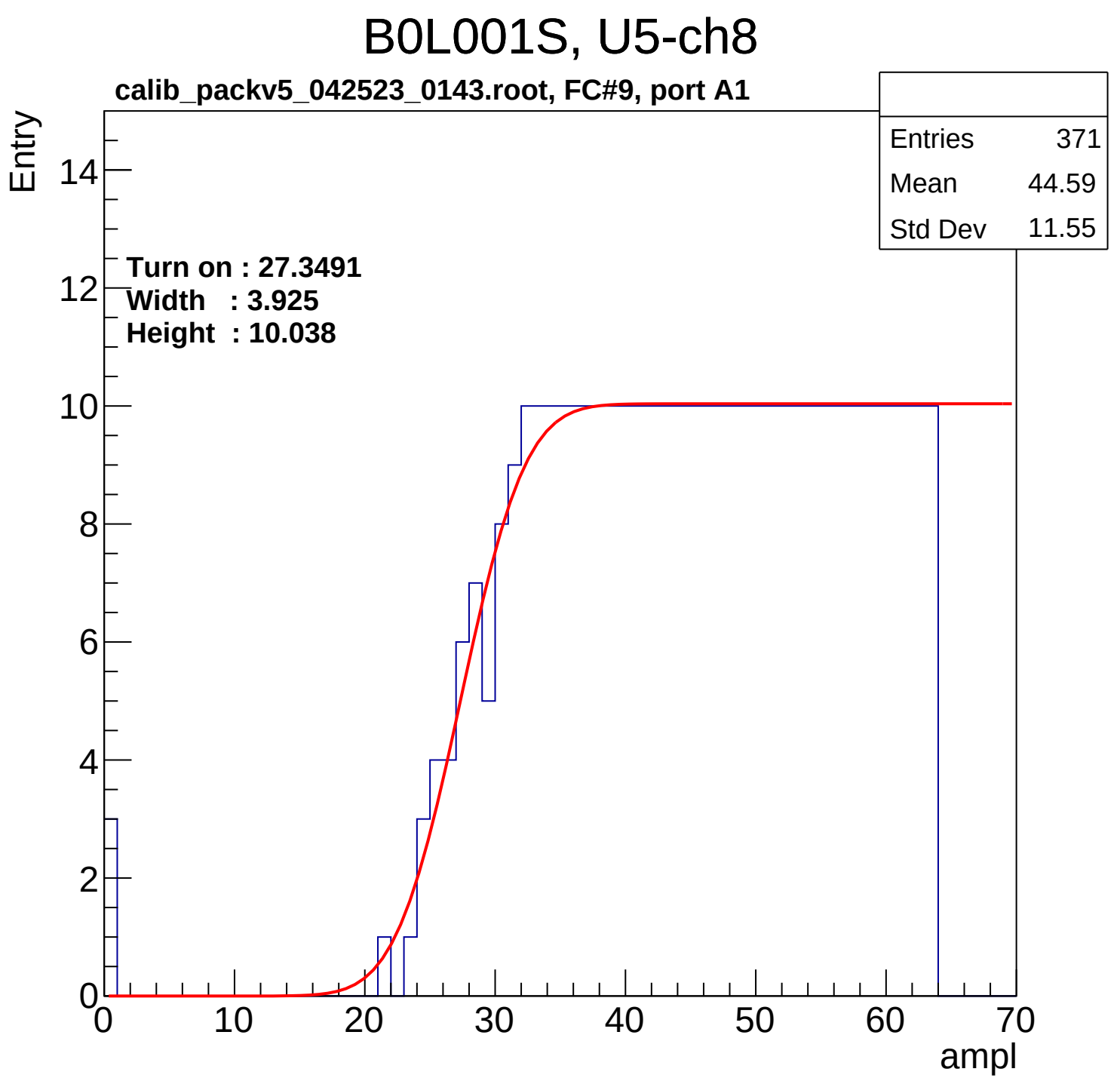
B0L001S, U5-ch8
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.59
Std Dev 11.55
Turn on : 27.3491
Width : 3.925
Height : 10.038
Entry
ampl
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4
6
8
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0
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60
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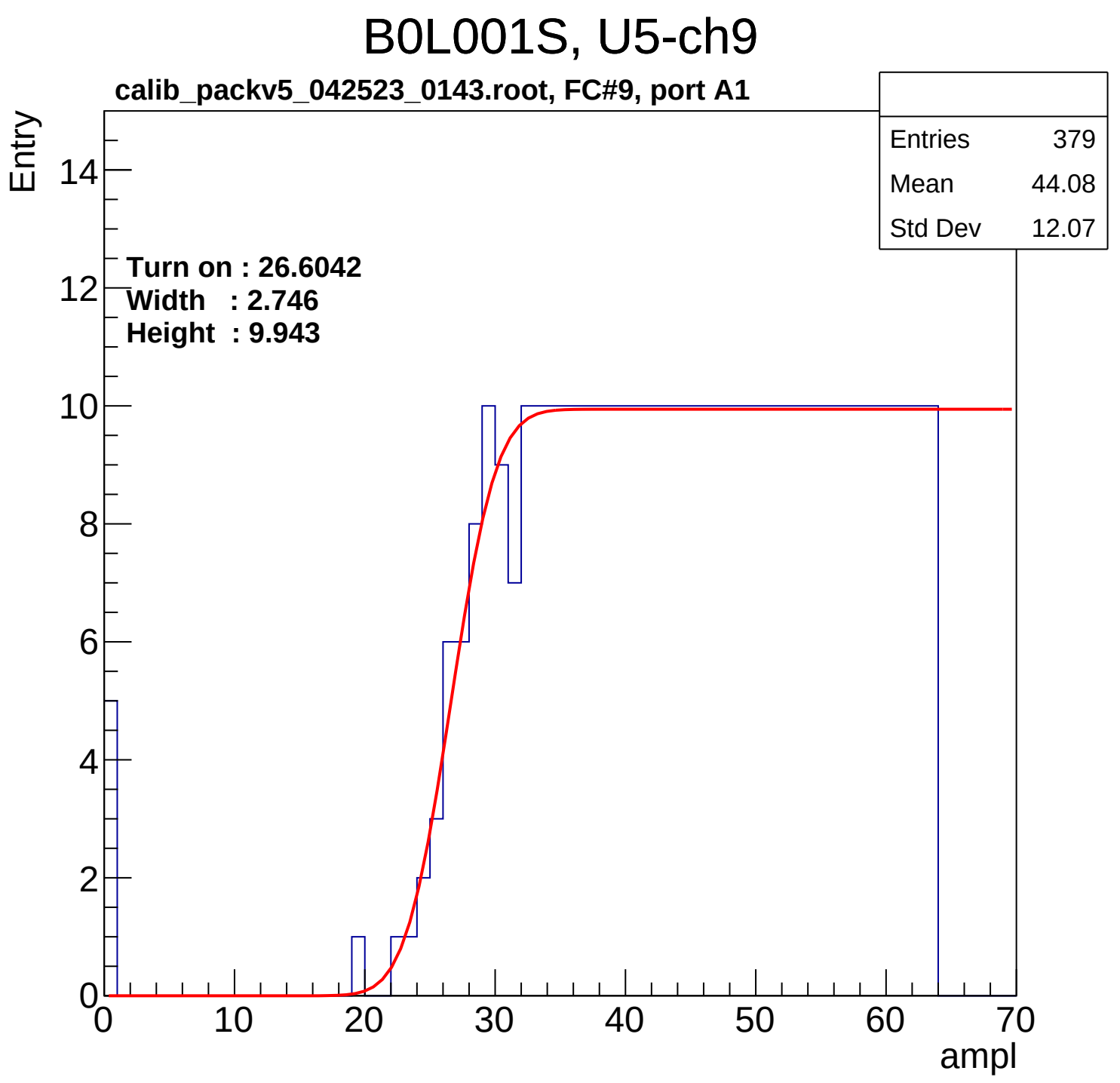
B0L001S, U5-ch9
calib_packv5_042523_0143.root, FC#9, port A1
Entries 379
Mean 44.08
Std Dev 12.07
Turn on : 26.6042
Width : 2.746
Height : 9.943
Entry
ampl
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2
4
6
8
10
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0
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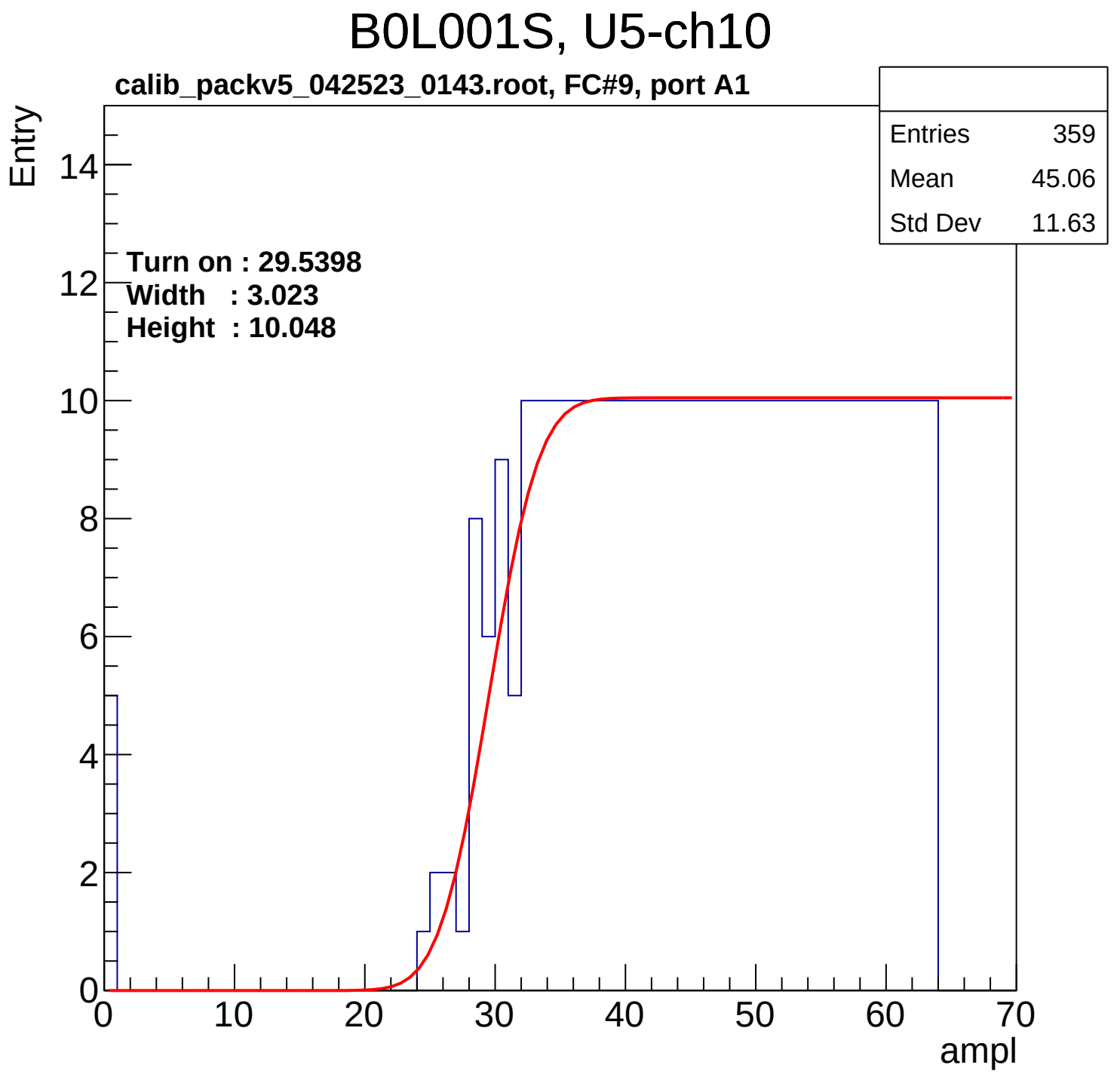
B0L001S, U5-ch10
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.06
Std Dev 11.63
Turn on : 29.5398
Width : 3.023
Height : 10.048
Entry
ampl
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4
6
8
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0
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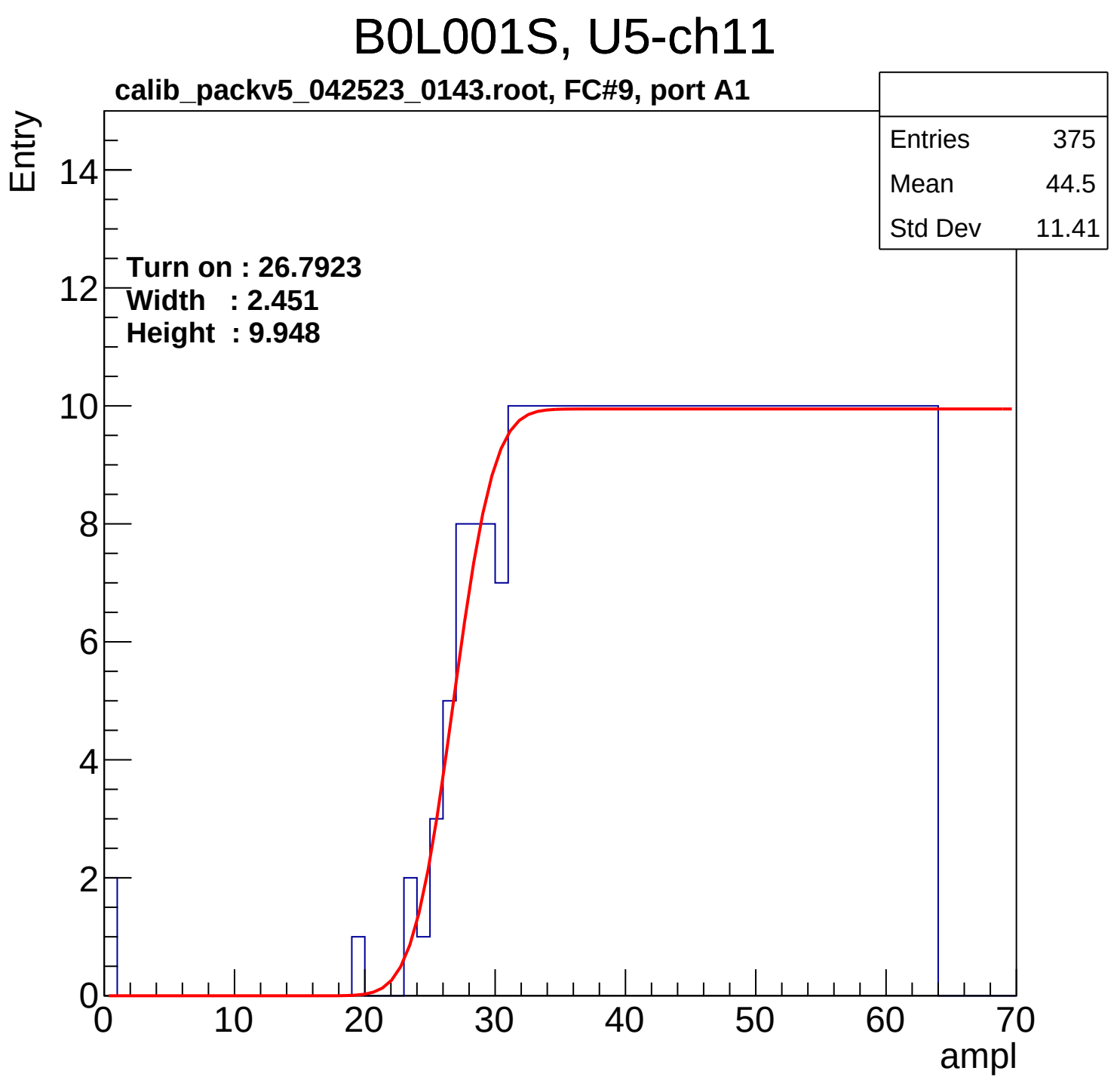
B0L001S, U5-ch11
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.5
Std Dev 11.41
Turn on : 26.7923
Width : 2.451
Height : 9.948
Entry
ampl
0
2
4
6
8
10
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0
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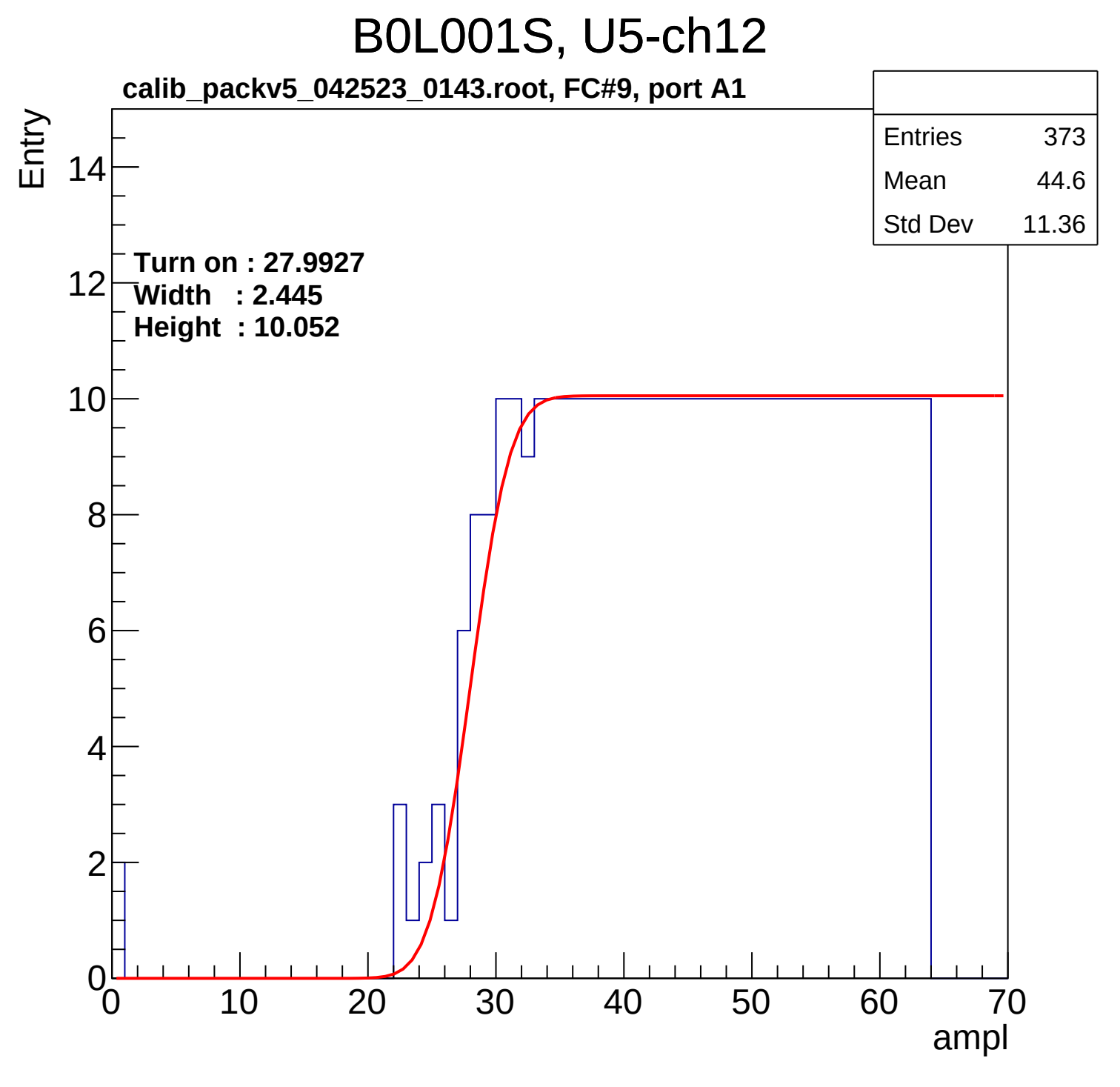
B0L001S, U5-ch12
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.6
Std Dev 11.36
Turn on : 27.9927
Width : 2.445
Height : 10.052
Entry
ampl
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2
4
6
8
10
12
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0
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20
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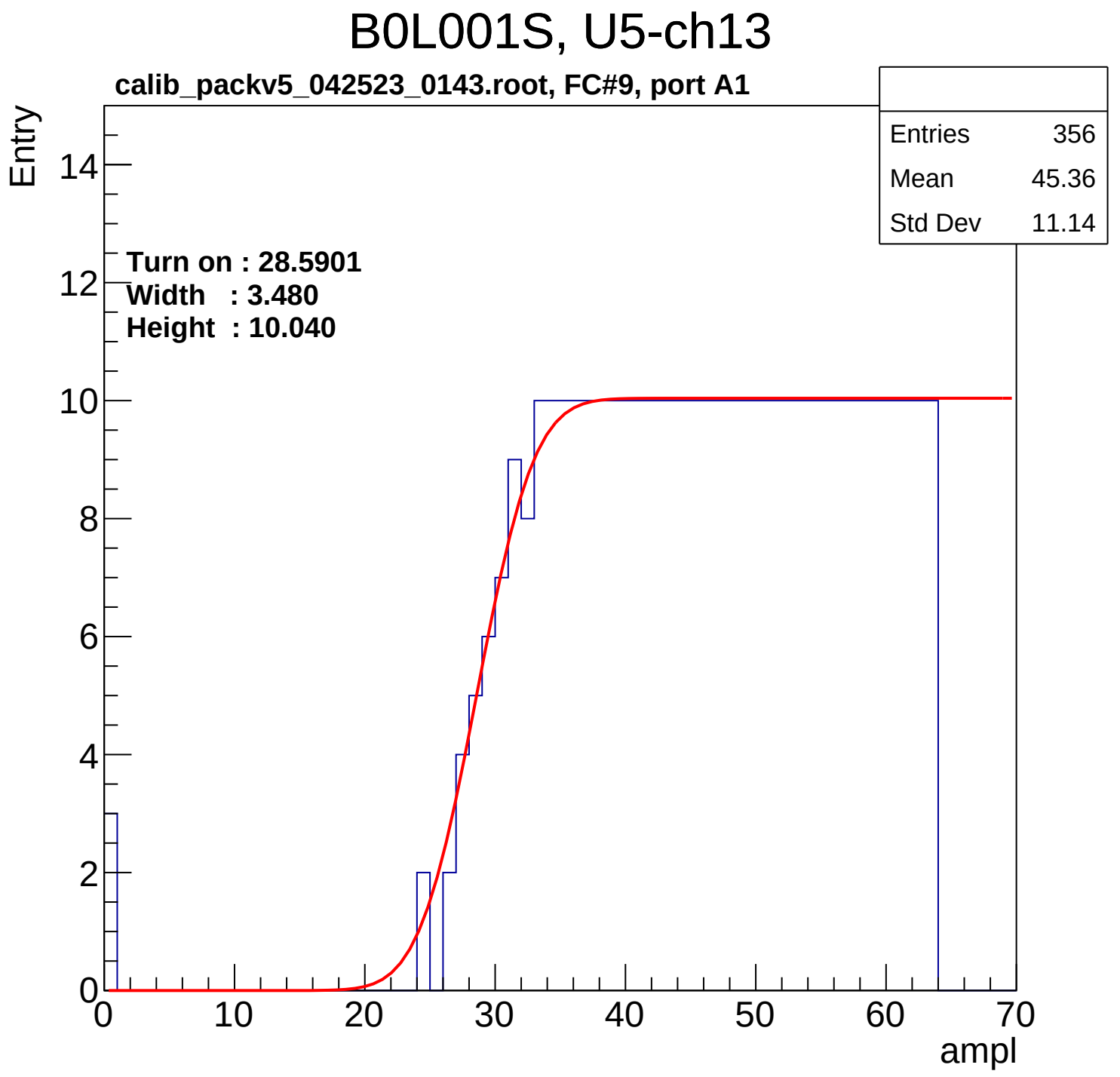
B0L001S, U5-ch13
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.36
Std Dev 11.14
Turn on : 28.5901
Width : 3.480
Height : 10.040
Entry
ampl
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2
4
6
8
10
12
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0
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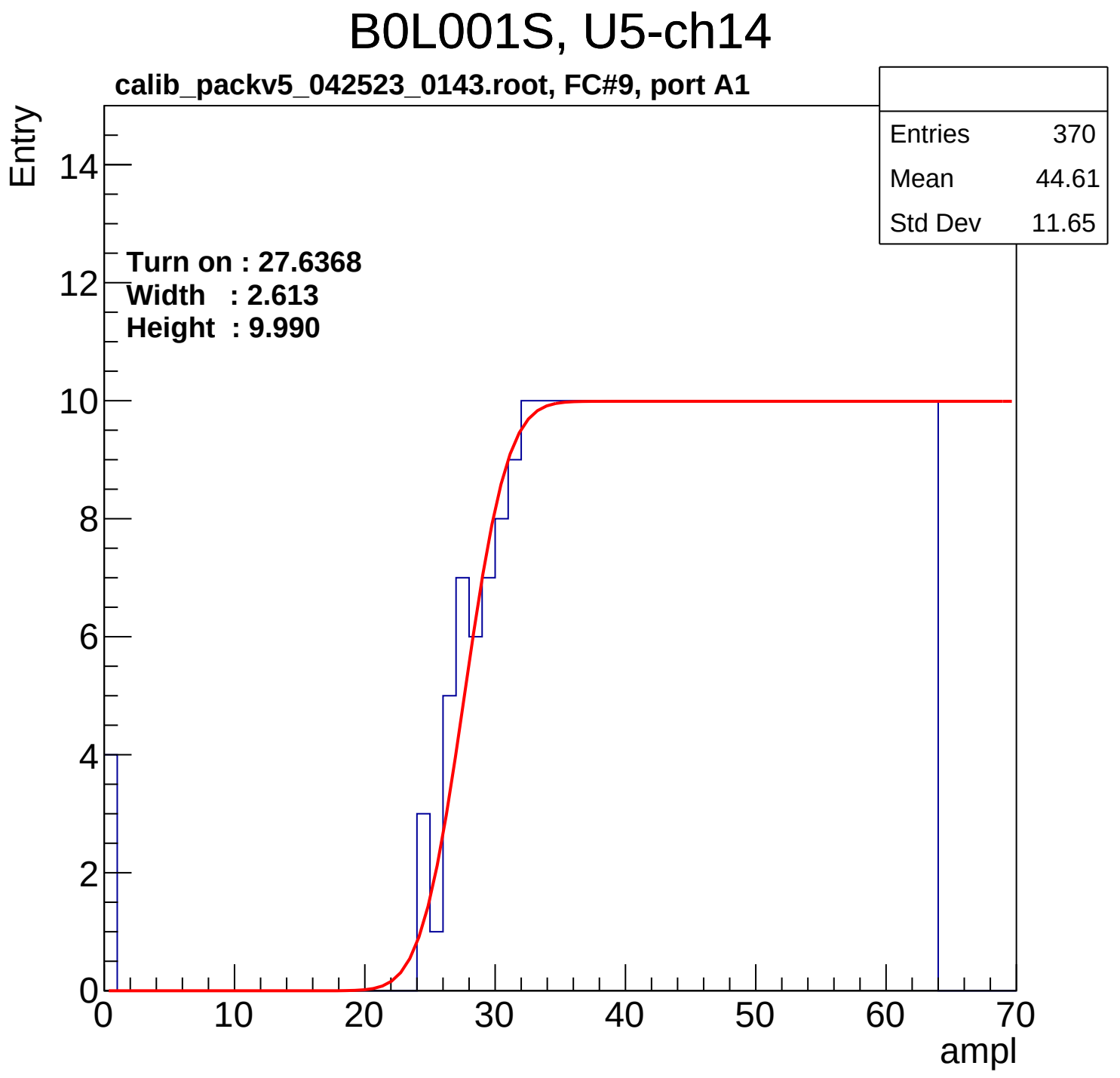
B0L001S, U5-ch14
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.61
Std Dev 11.65
Turn on : 27.6368
Width : 2.613
Height : 9.990
Entry
ampl
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4
6
8
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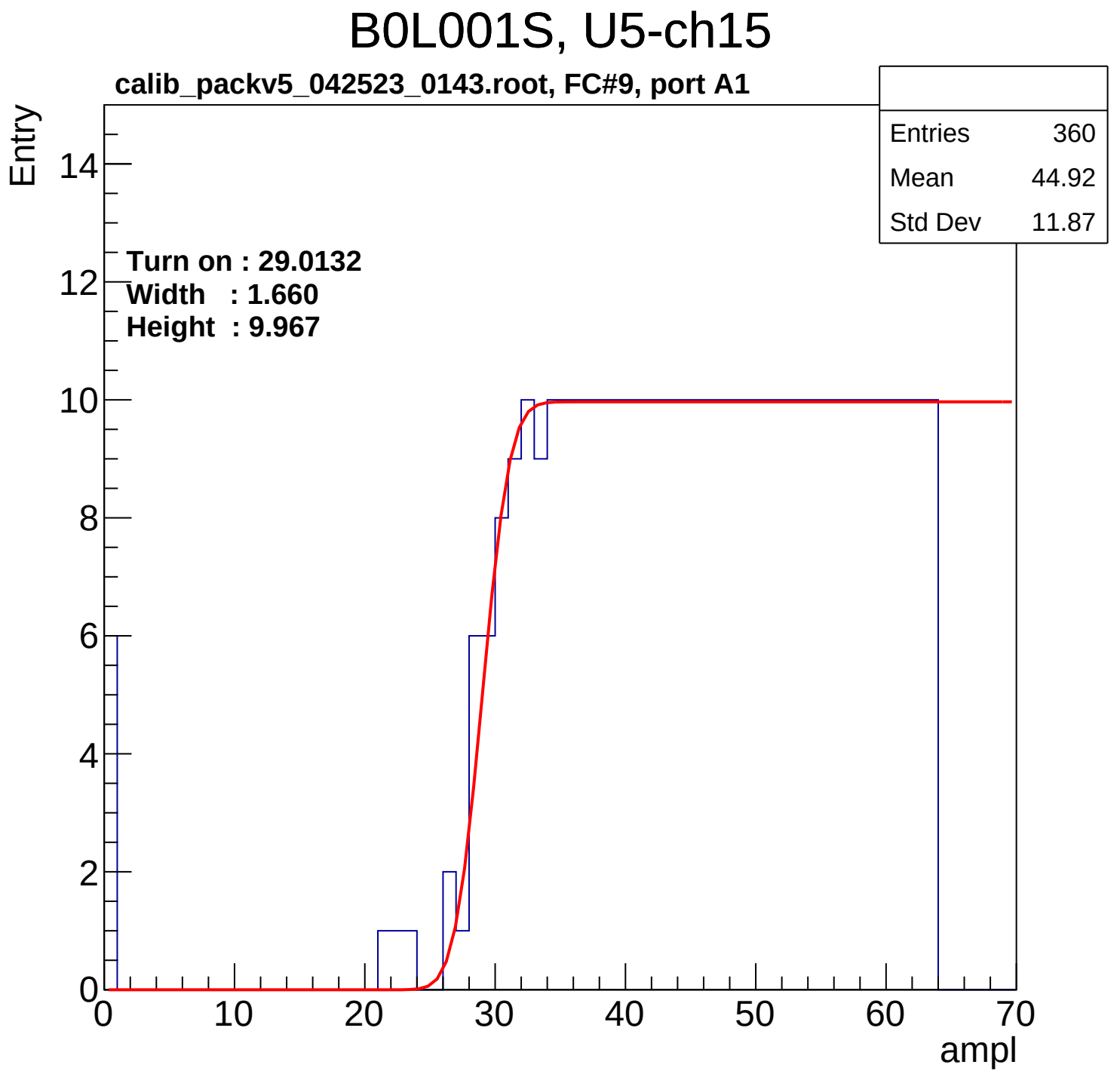
B0L001S, U5-ch15
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 44.92
Std Dev 11.87
Turn on : 29.0132
Width : 1.660
Height : 9.967
Entry
ampl
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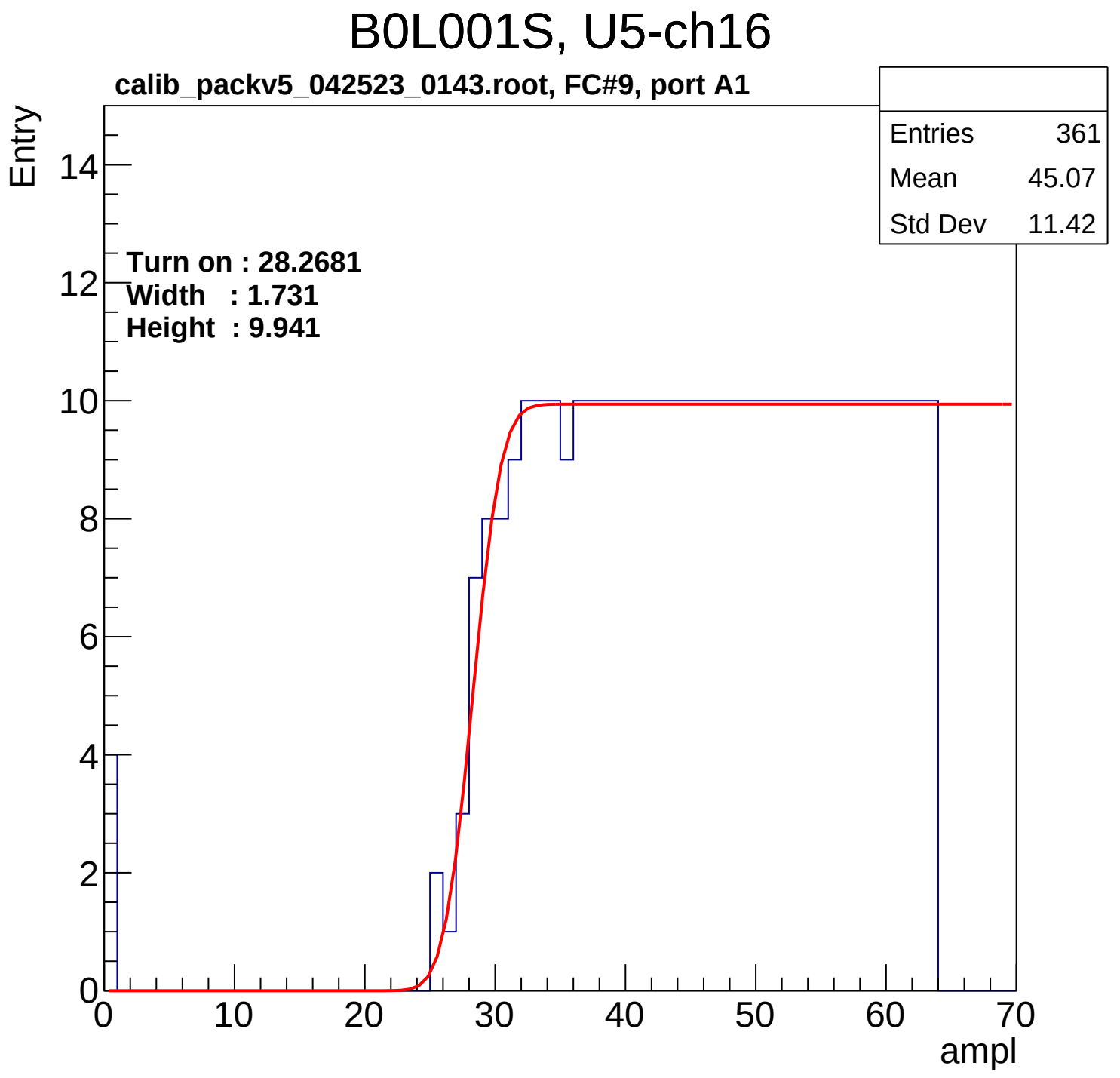
B0L001S, U5-ch16
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.07
Std Dev 11.42
Turn on : 28.2681
Width : 1.731
Height : 9.941
Entry
ampl
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2
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6
8
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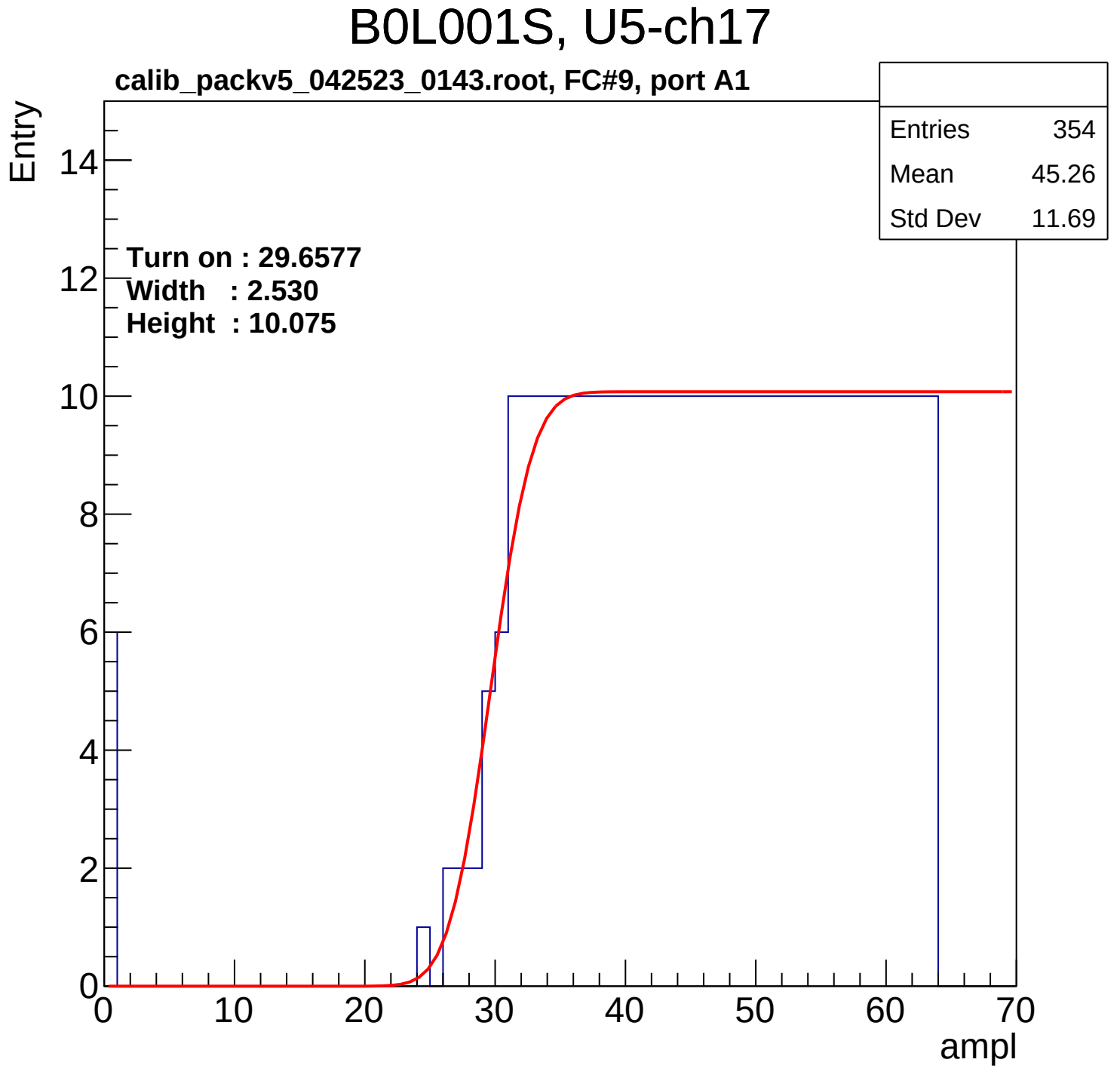
B0L001S, U5-ch17
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.26
Std Dev 11.69
Turn on : 29.6577
Width : 2.530
Height : 10.075
Entry
ampl
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8
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60
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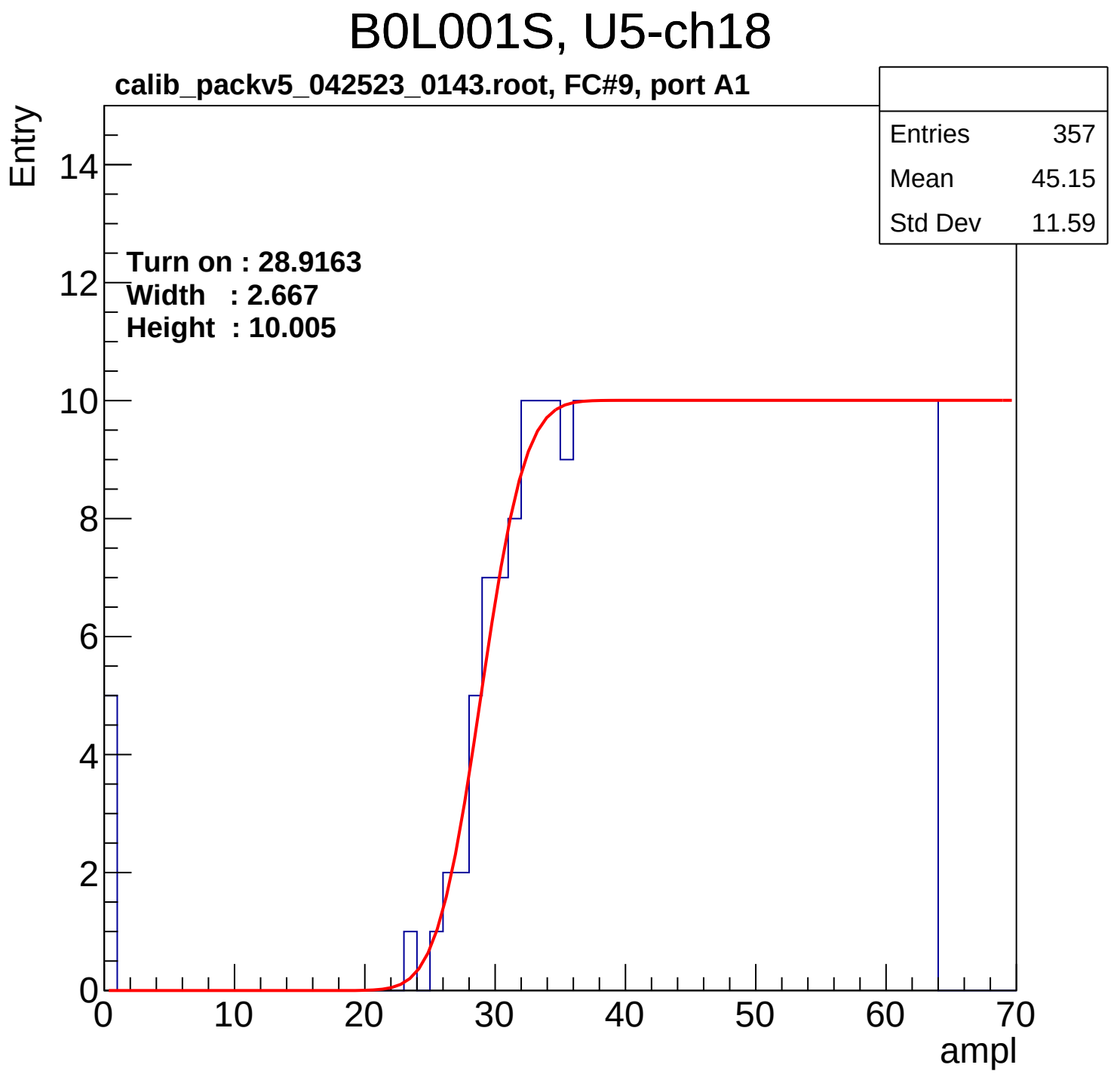
B0L001S, U5-ch18
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.15
Std Dev 11.59
Turn on : 28.9163
Width : 2.667
Height : 10.005
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ampl
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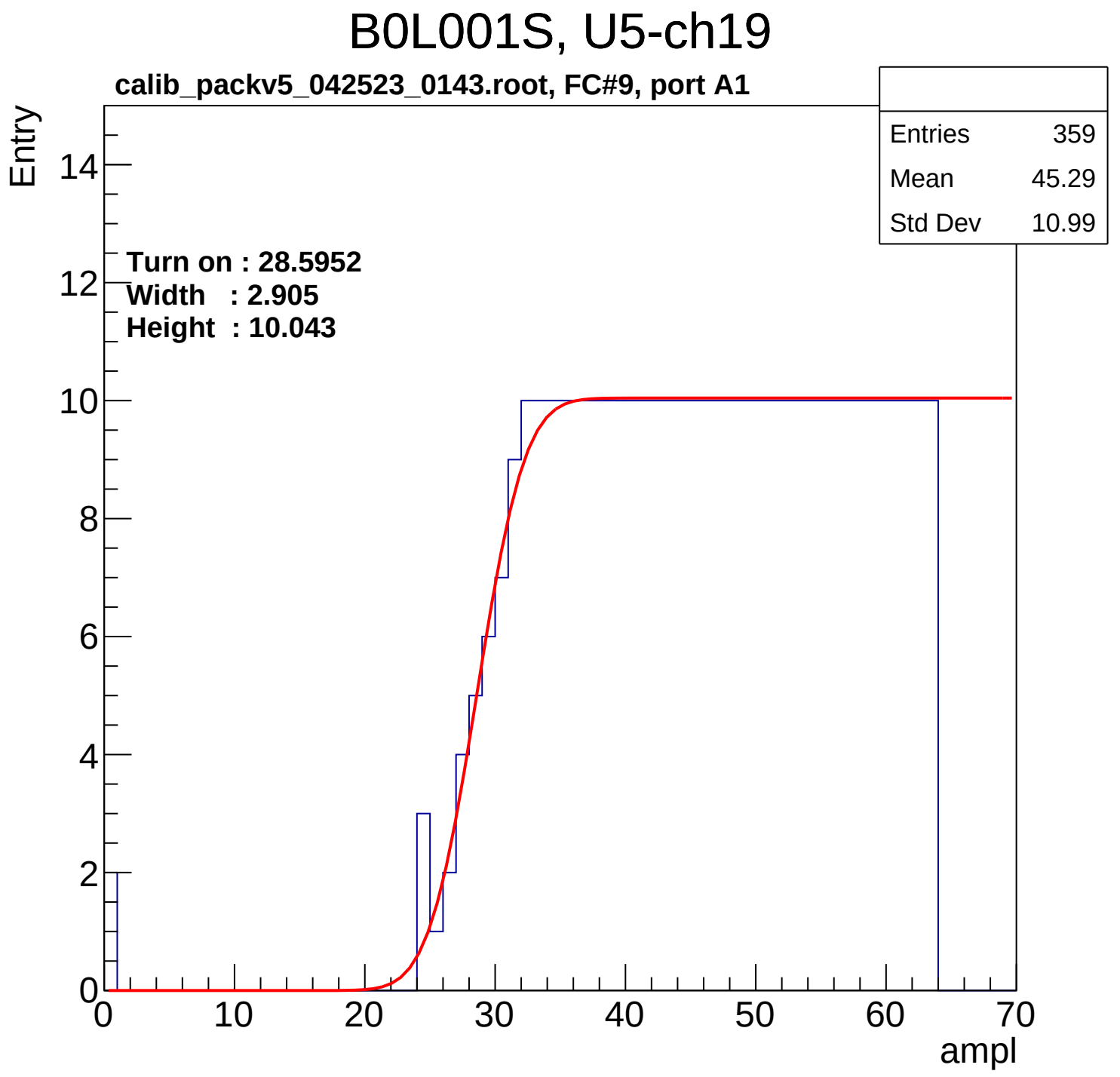
B0L001S, U5-ch19
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.29
Std Dev 10.99
Turn on : 28.5952
Width : 2.905
Height : 10.043
Entry
ampl
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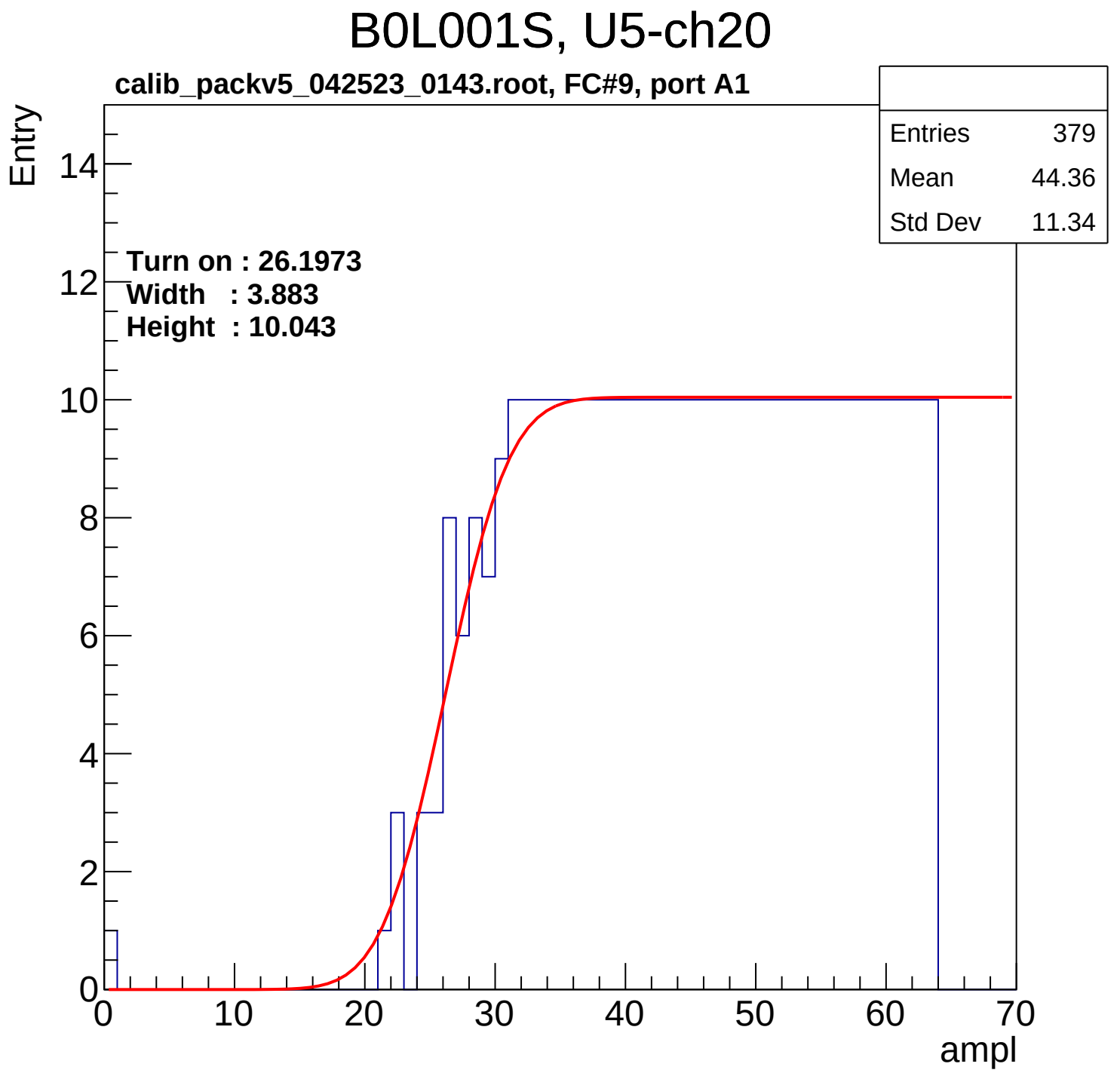
B0L001S, U5-ch20
calib_packv5_042523_0143.root, FC#9, port A1
Entries 379
Mean 44.36
Std Dev 11.34
Turn on : 26.1973
Width : 3.883
Height : 10.043
Entry
ampl
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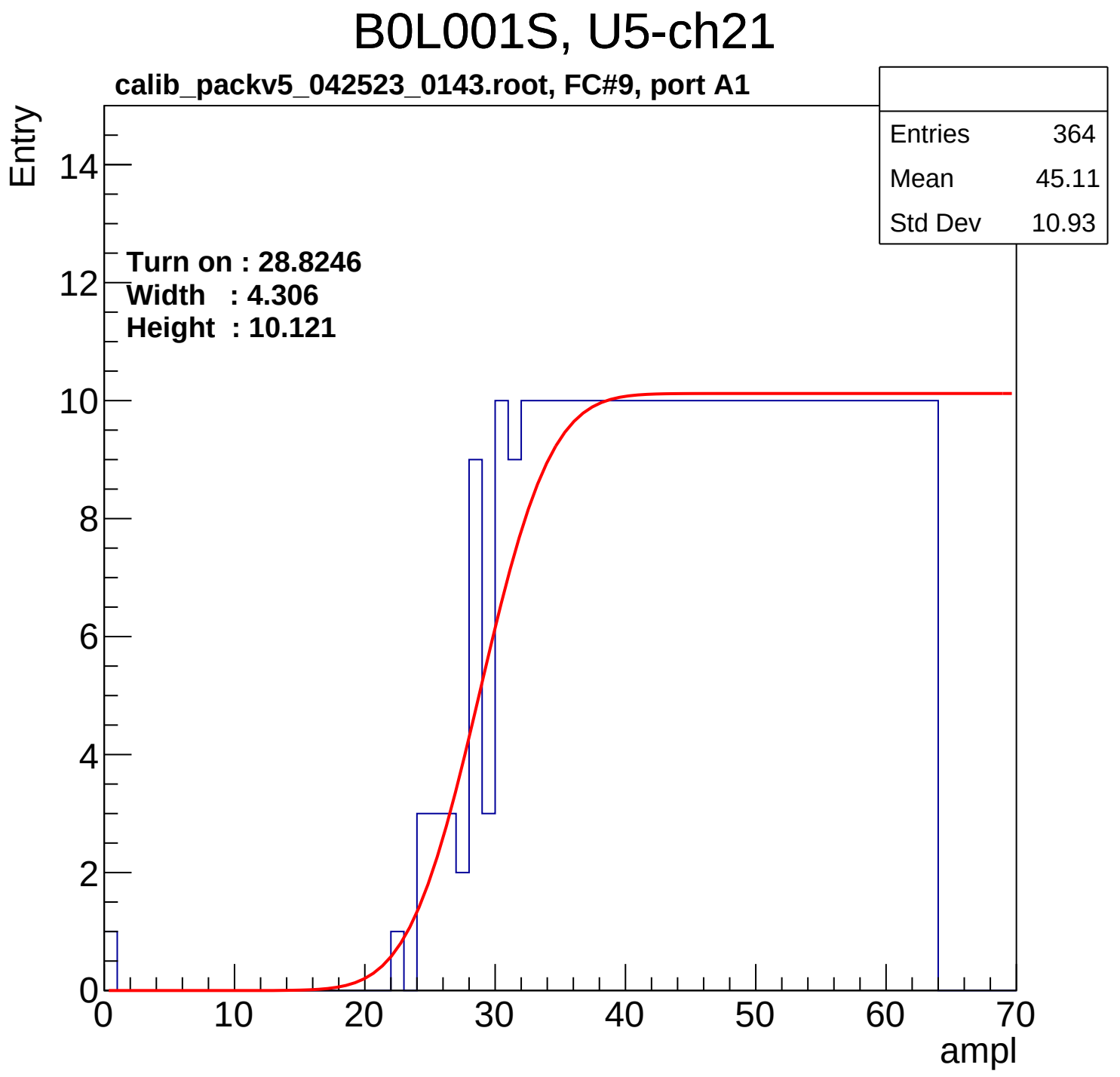
B0L001S, U5-ch21
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 45.11
Std Dev 10.93
Turn on : 28.8246
Width : 4.306
Height : 10.121
Entry
ampl
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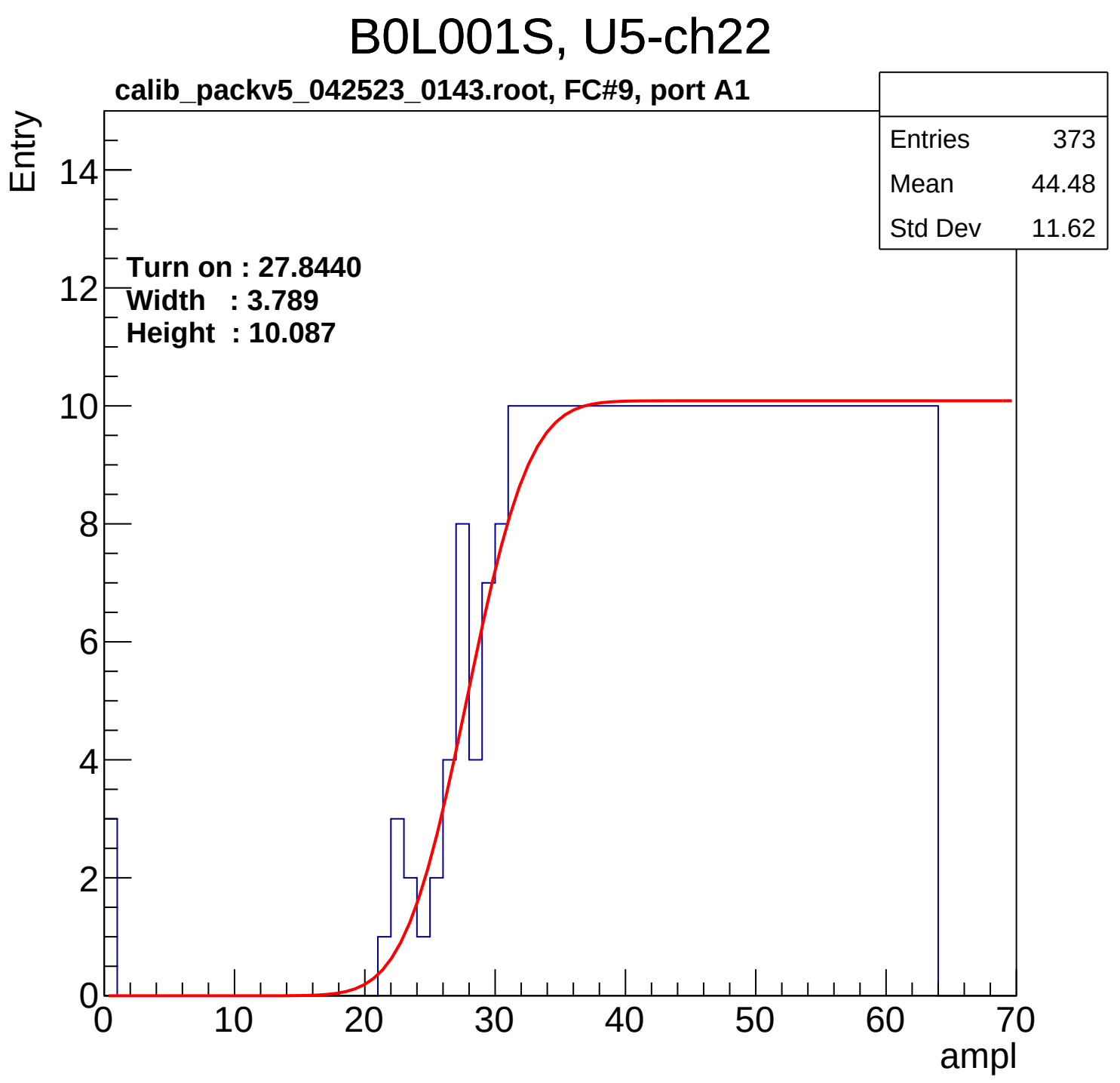
B0L001S, U5-ch22
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.48
Std Dev 11.62
Turn on : 27.8440
Width : 3.789
Height : 10.087
Entry
ampl
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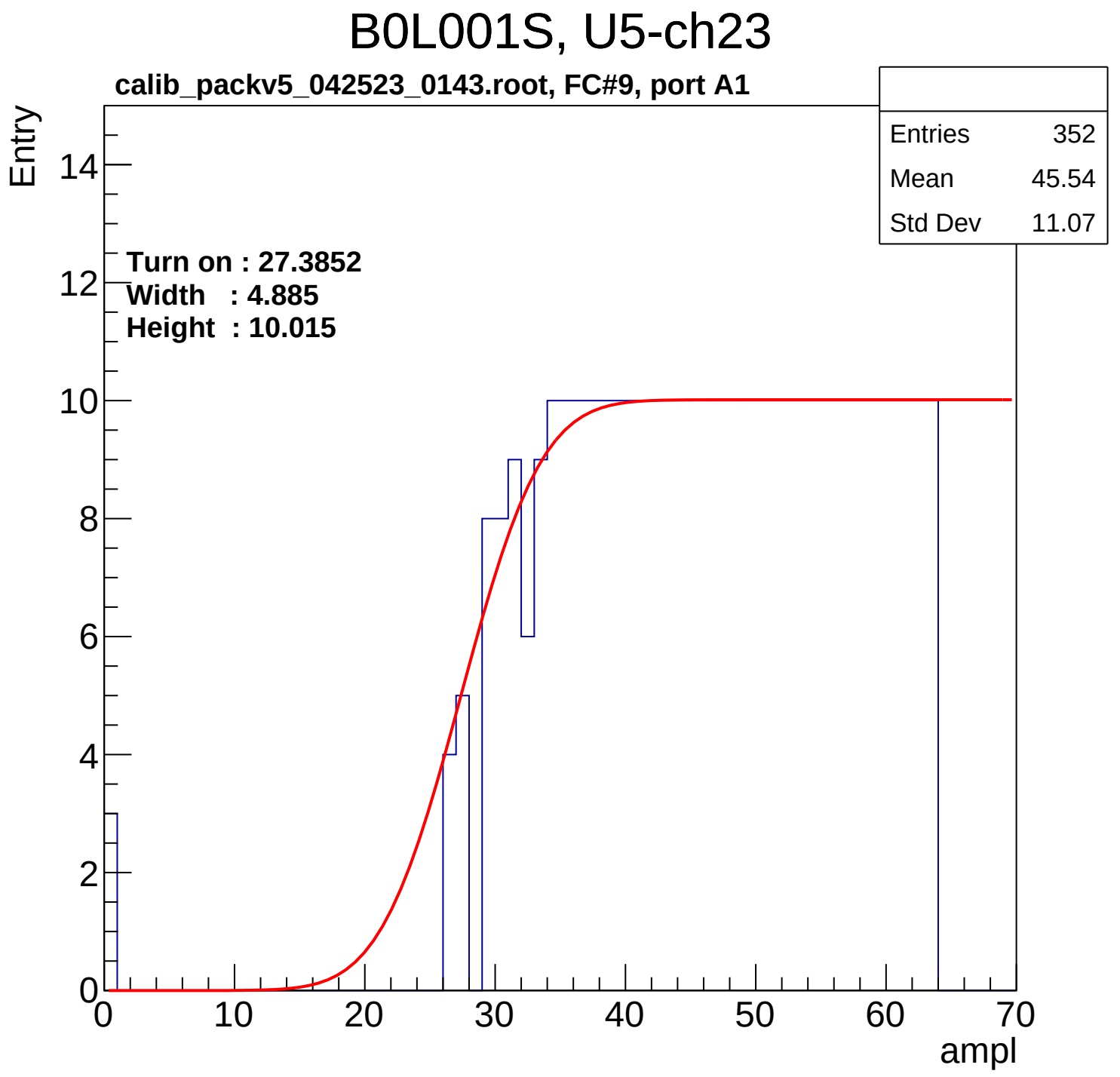
B0L001S, U5-ch23
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.54
Std Dev 11.07
Turn on : 27.3852
Width : 4.885
Height : 10.015
Entry
ampl
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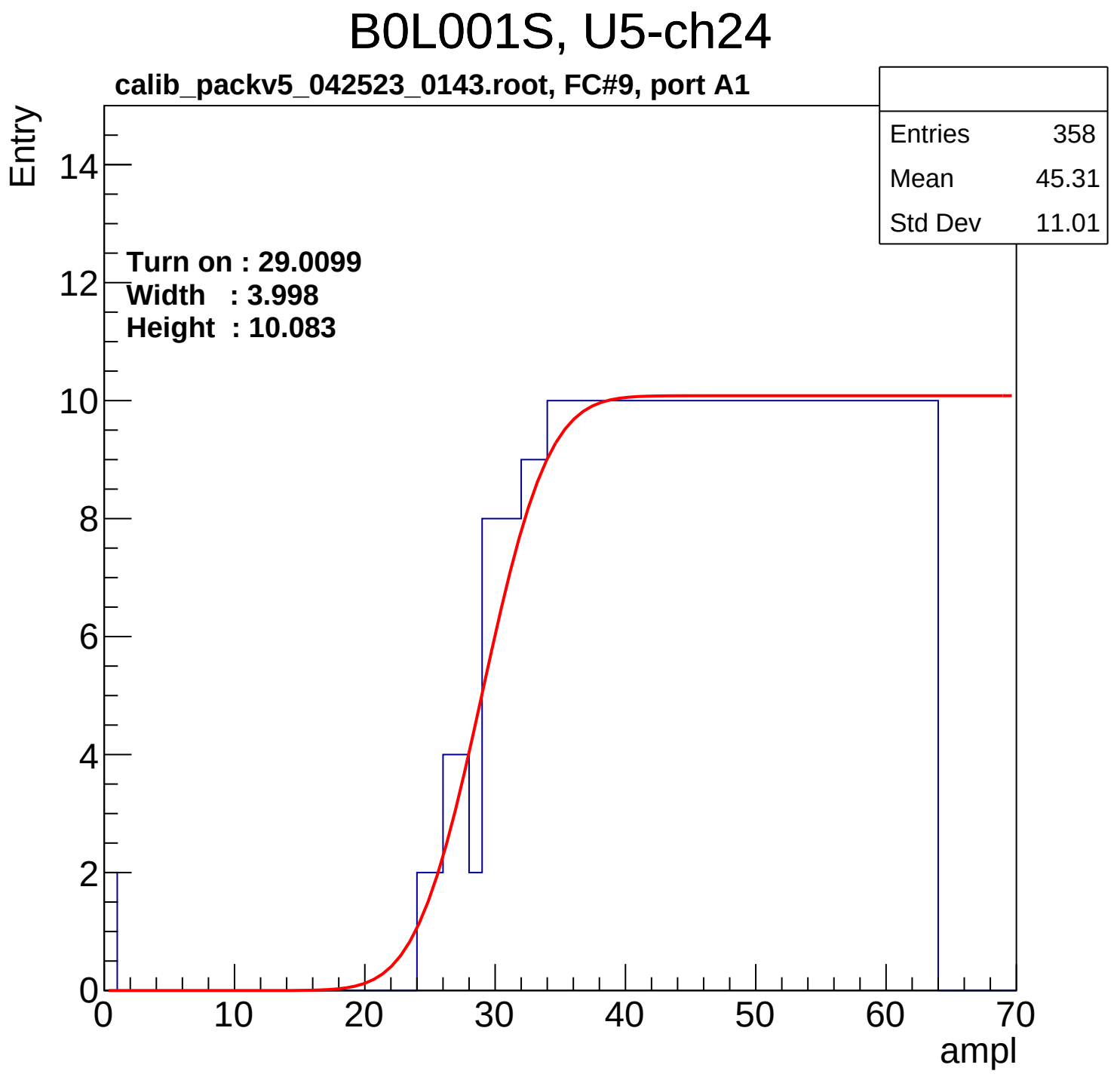
B0L001S, U5-ch24
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.31
Std Dev 11.01
Turn on : 29.0099
Width : 3.998
Height : 10.083
Entry
ampl
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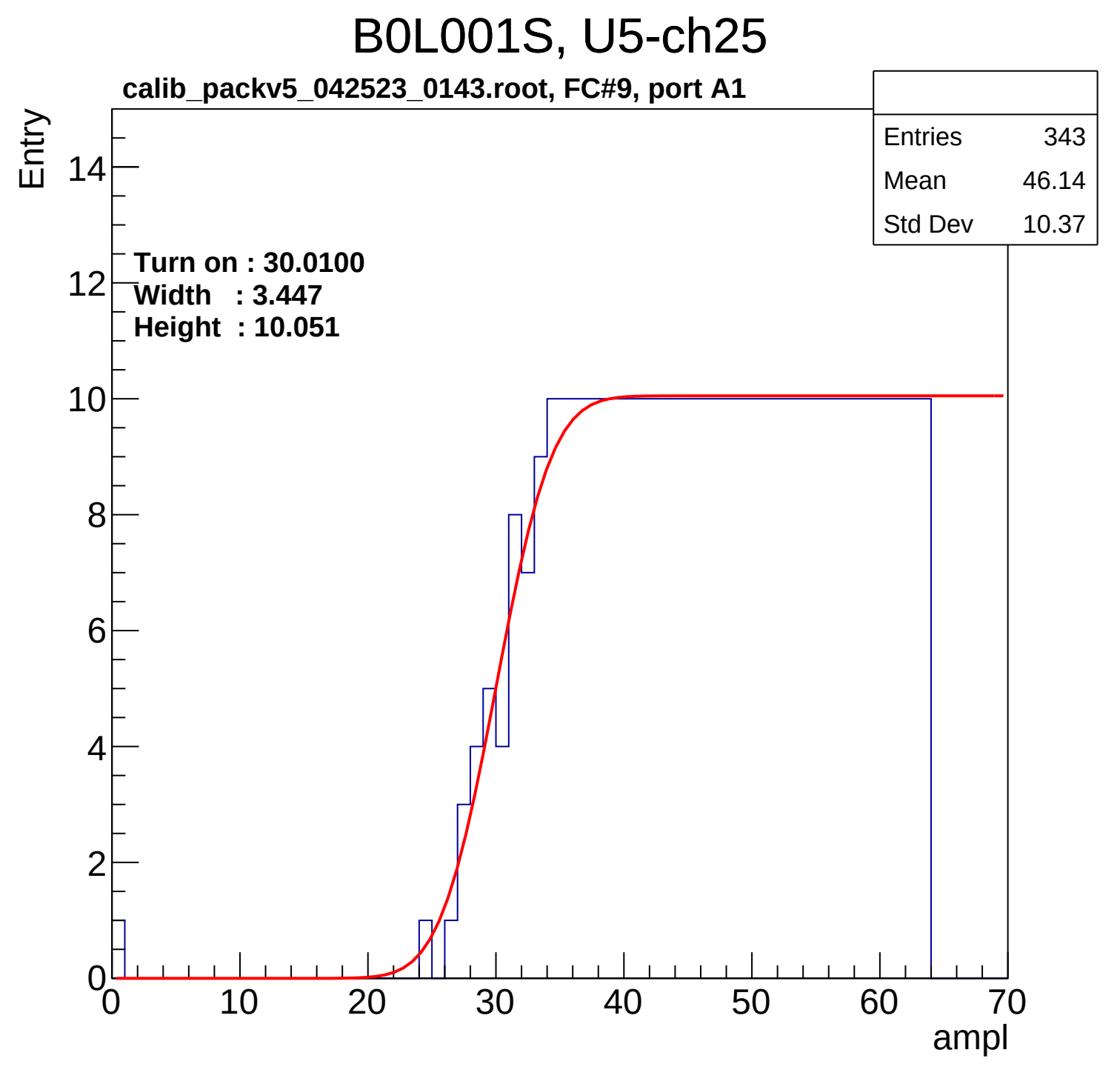
B0L001S, U5-ch25
calib_packv5_042523_0143.root, FC#9, port A1
Entries 343
Mean 46.14
Std Dev 10.37
Turn on : 30.0100
Width : 3.447
Height : 10.051
Entry
ampl
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2
4
6
8
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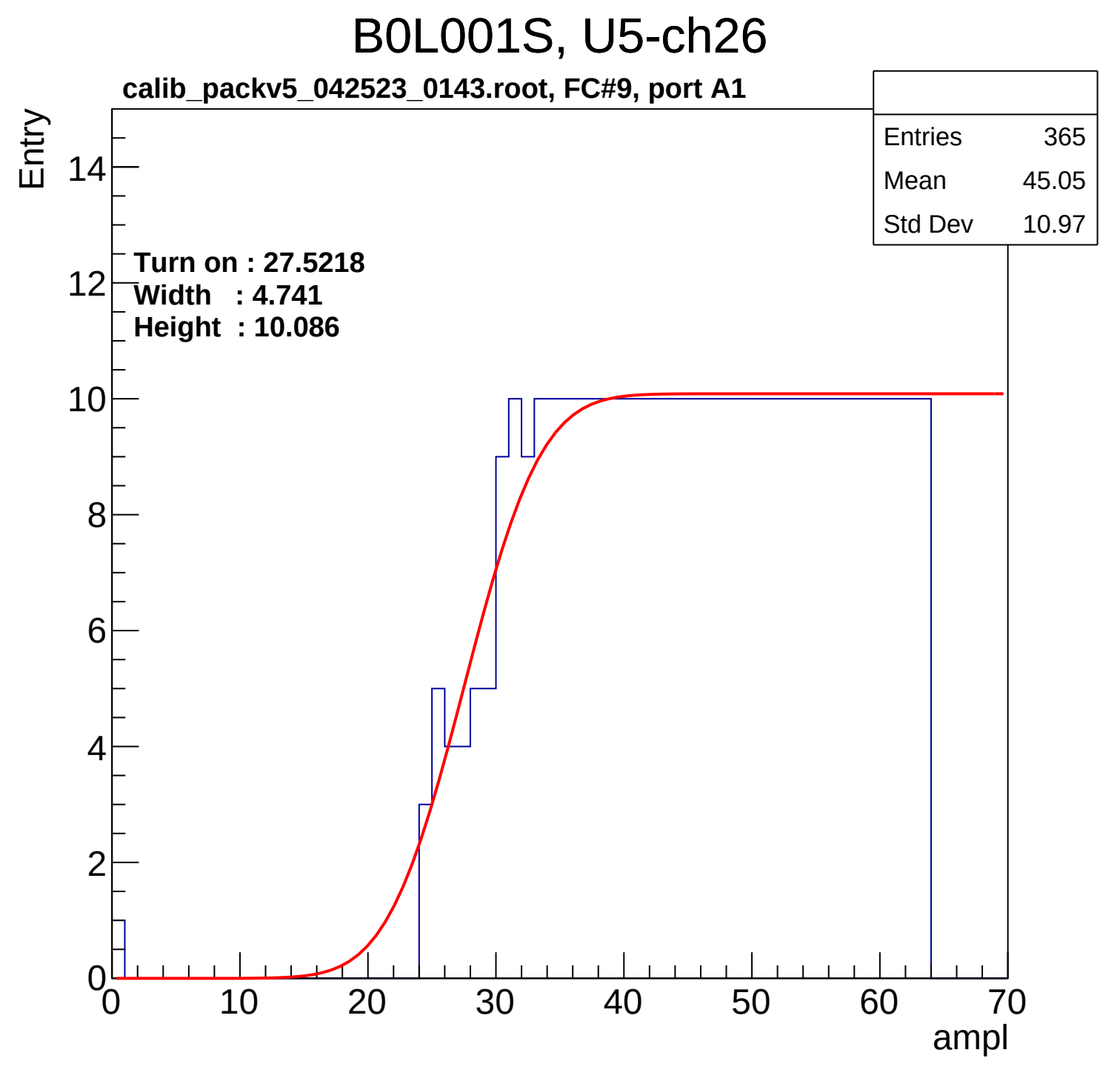
B0L001S, U5-ch26
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 45.05
Std Dev 10.97
Turn on : 27.5218
Width : 4.741
Height : 10.086
Entry
ampl
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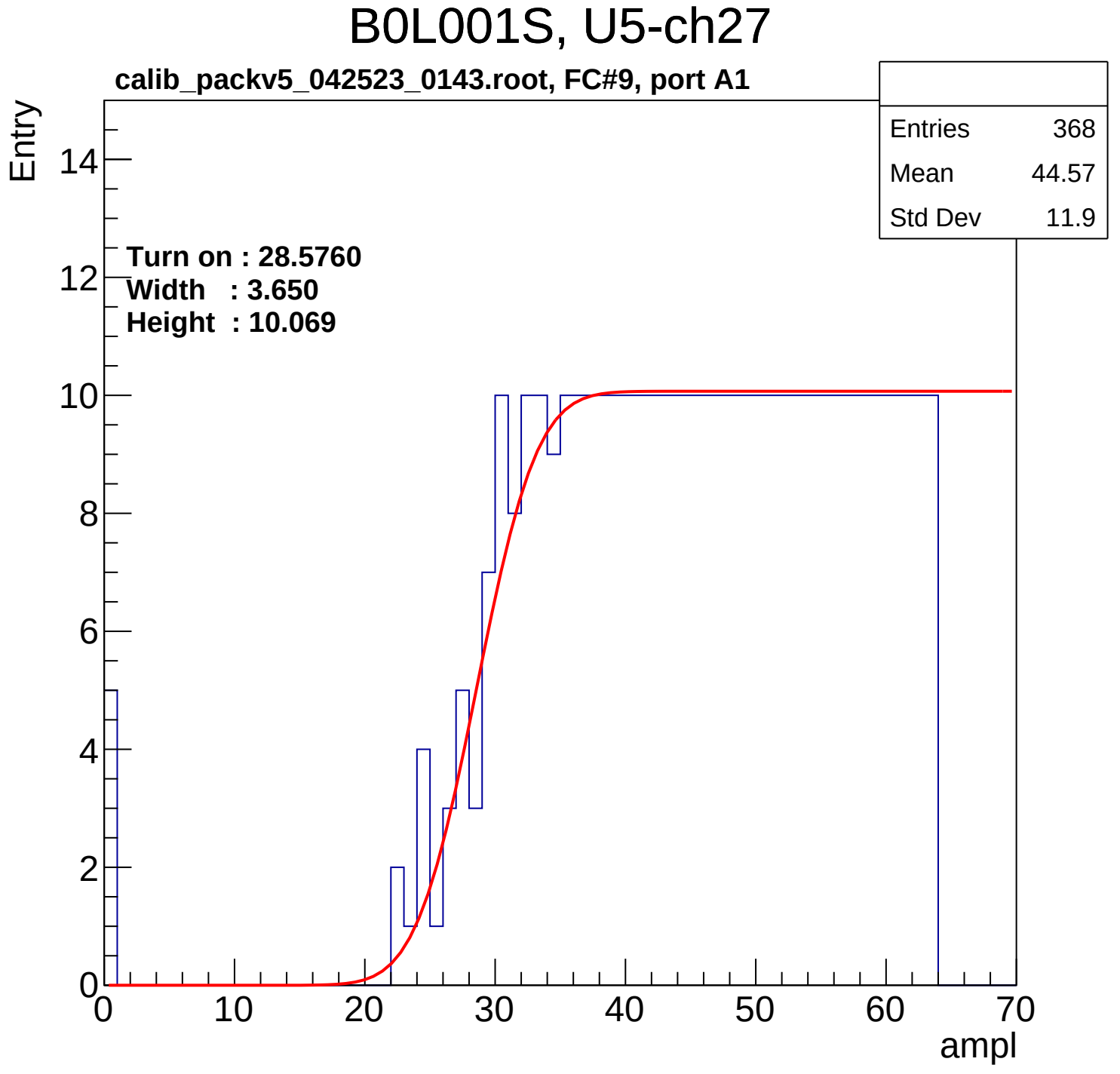
B0L001S, U5-ch27
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.57
Std Dev 11.9
Turn on : 28.5760
Width : 3.650
Height : 10.069
Entry
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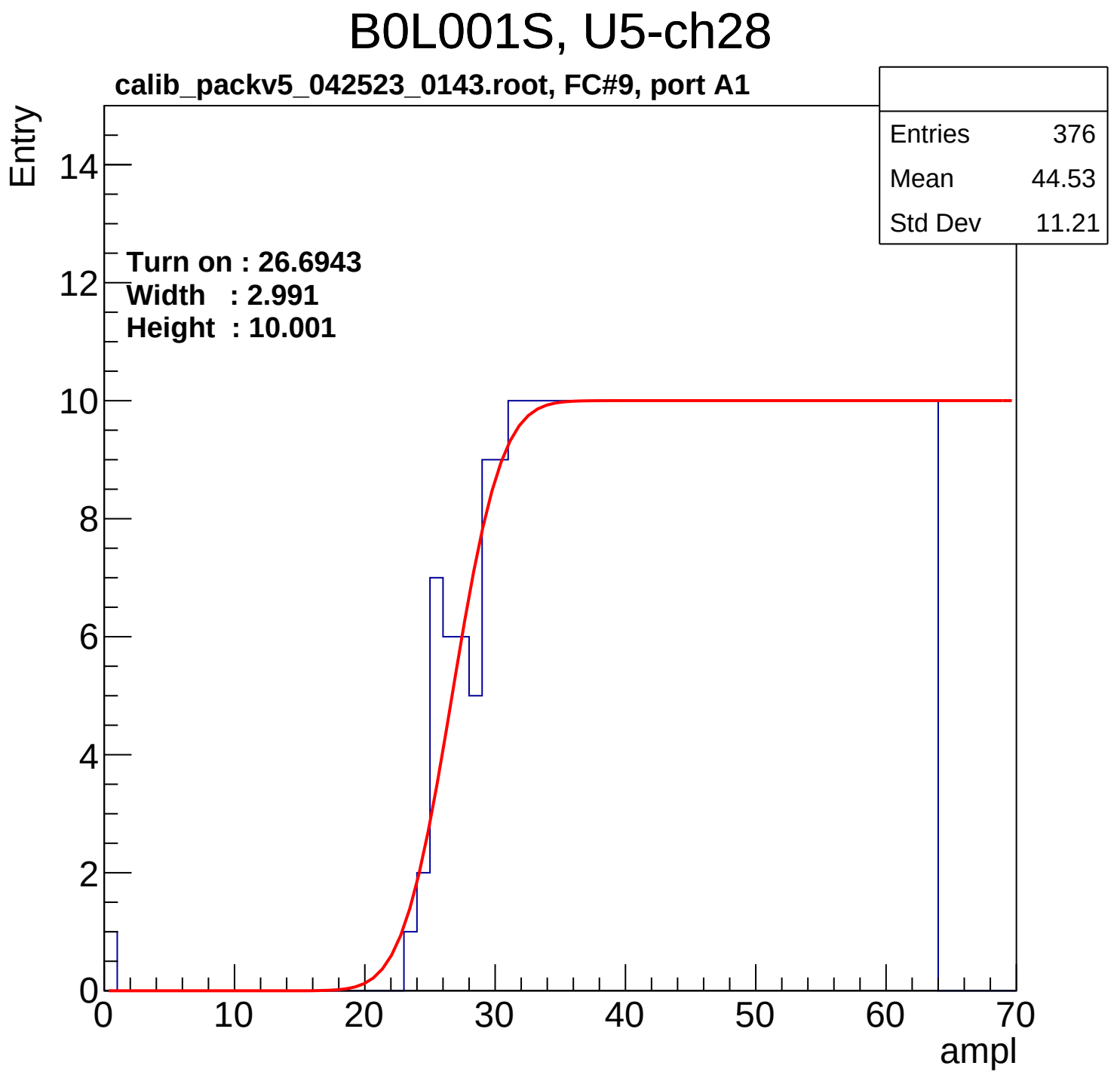
B0L001S, U5-ch28
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.53
Std Dev 11.21
Turn on : 26.6943
Width : 2.991
Height : 10.001
Entry
ampl
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4
6
8
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12
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10
20
30
40
50
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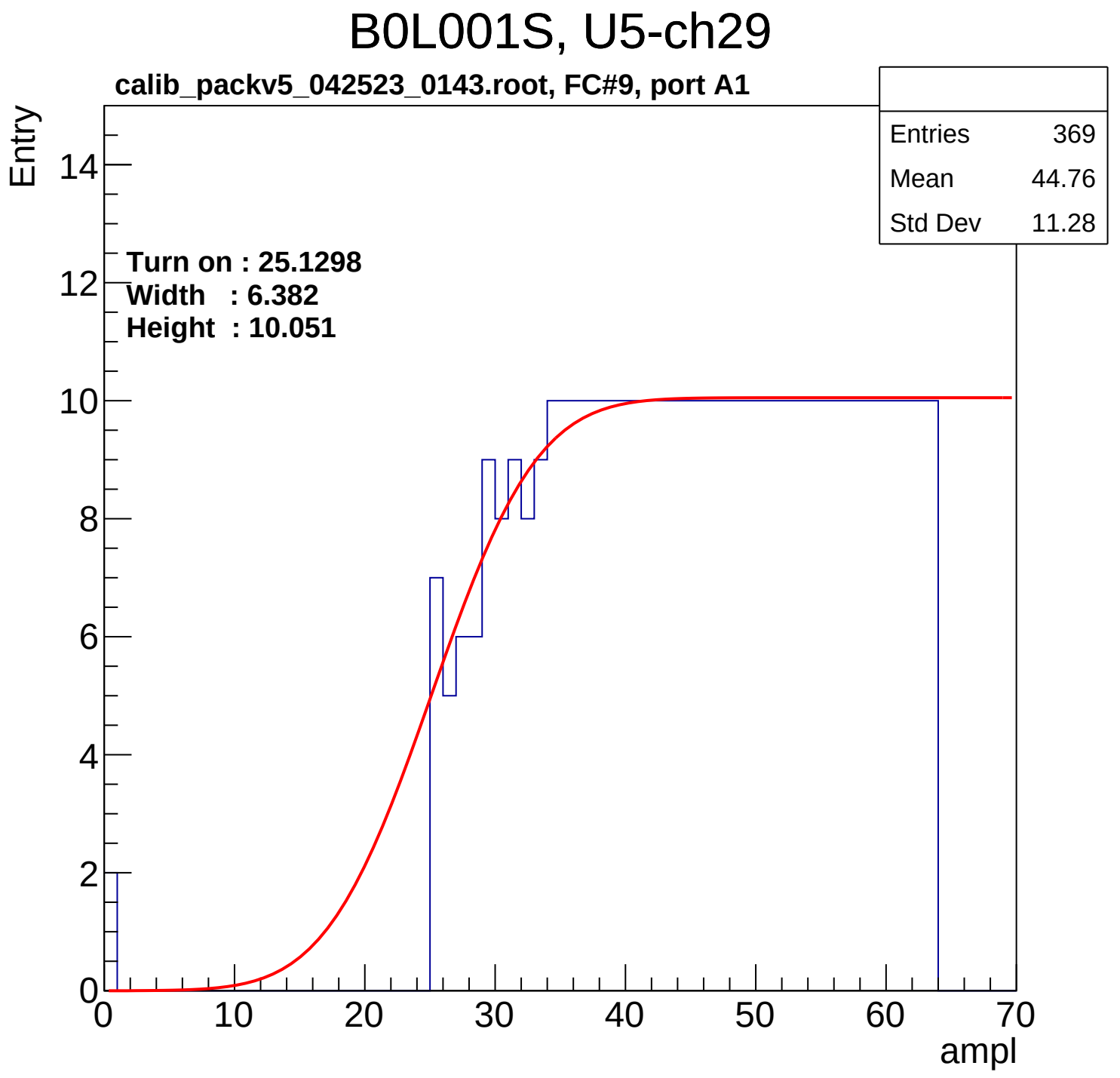
B0L001S, U5-ch29
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.76
Std Dev 11.28
Turn on : 25.1298
Width : 6.382
Height : 10.051
Entry
ampl
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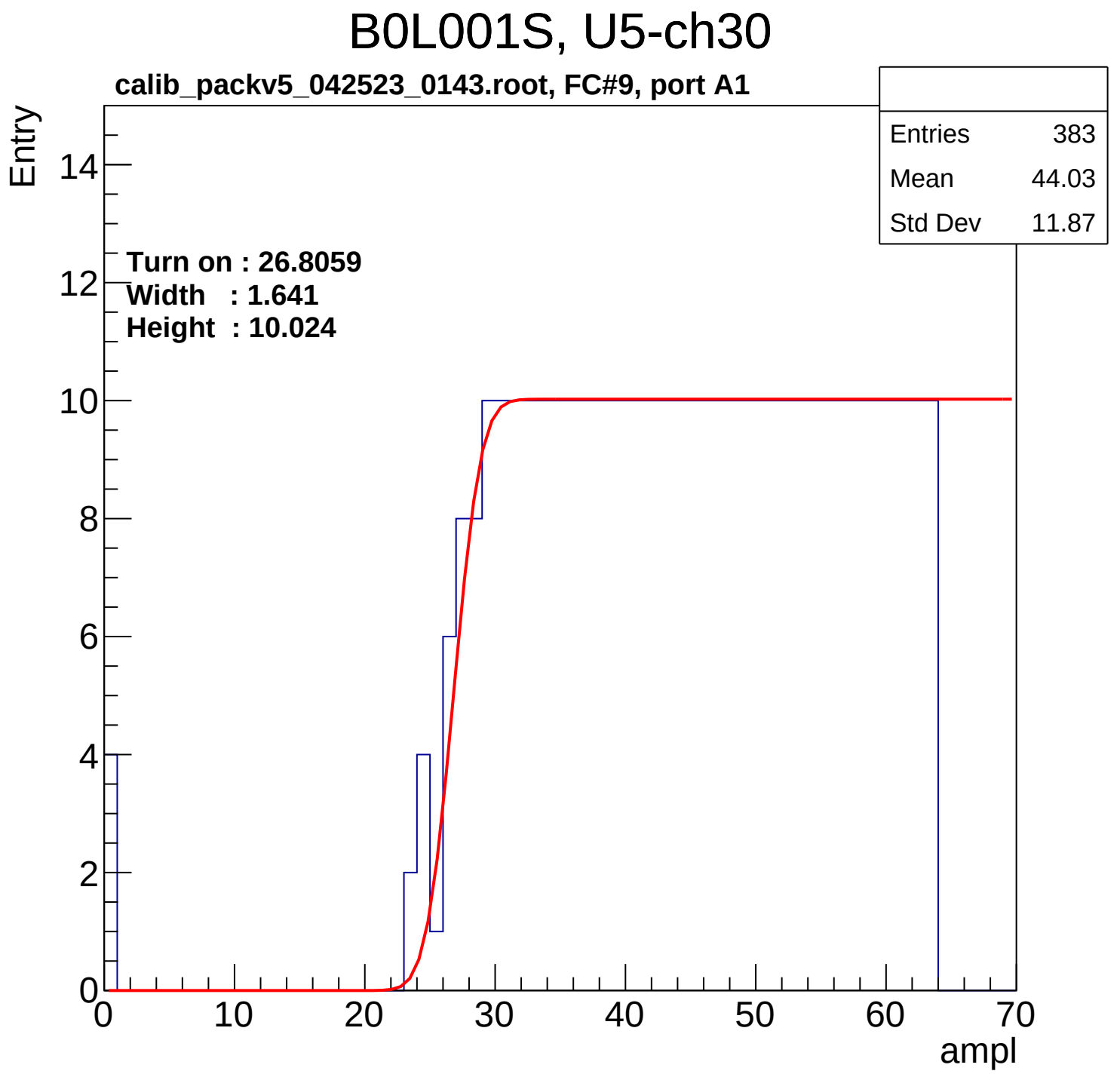
B0L001S, U5-ch30
calib_packv5_042523_0143.root, FC#9, port A1
Entries 383
Mean 44.03
Std Dev 11.87
Turn on : 26.8059
Width : 1.641
Height : 10.024
Entry
ampl
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2
4
6
8
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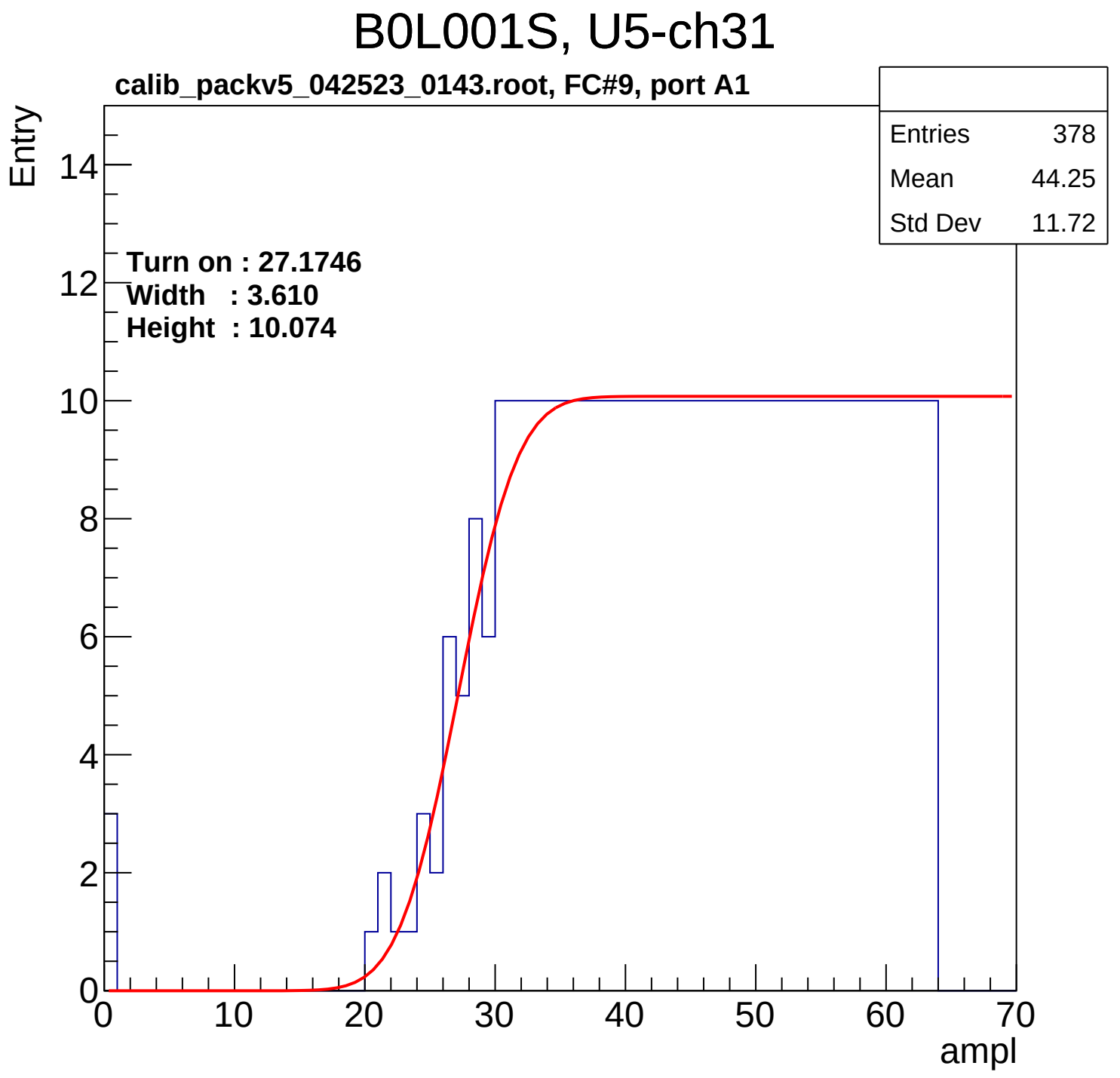
B0L001S, U5-ch31
calib_packv5_042523_0143.root, FC#9, port A1
Entries 378
Mean 44.25
Std Dev 11.72
Turn on : 27.1746
Width : 3.610
Height : 10.074
Entry
ampl
0
2
4
6
8
10
12
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0
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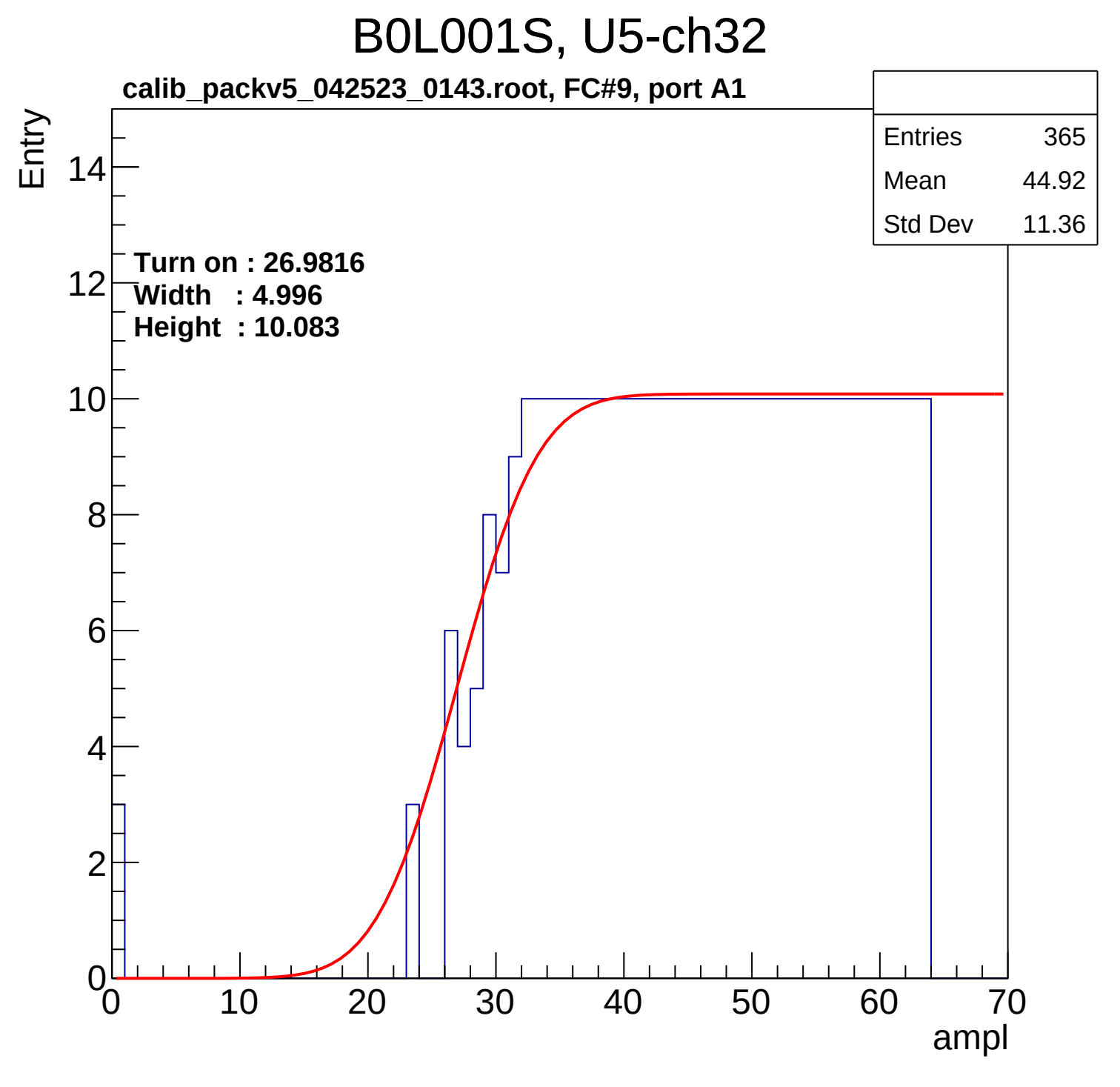
B0L001S, U5-ch32
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.92
Std Dev 11.36
Turn on : 26.9816
Width : 4.996
Height : 10.083
Entry
ampl
0
2
4
6
8
10
12
14
0
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40
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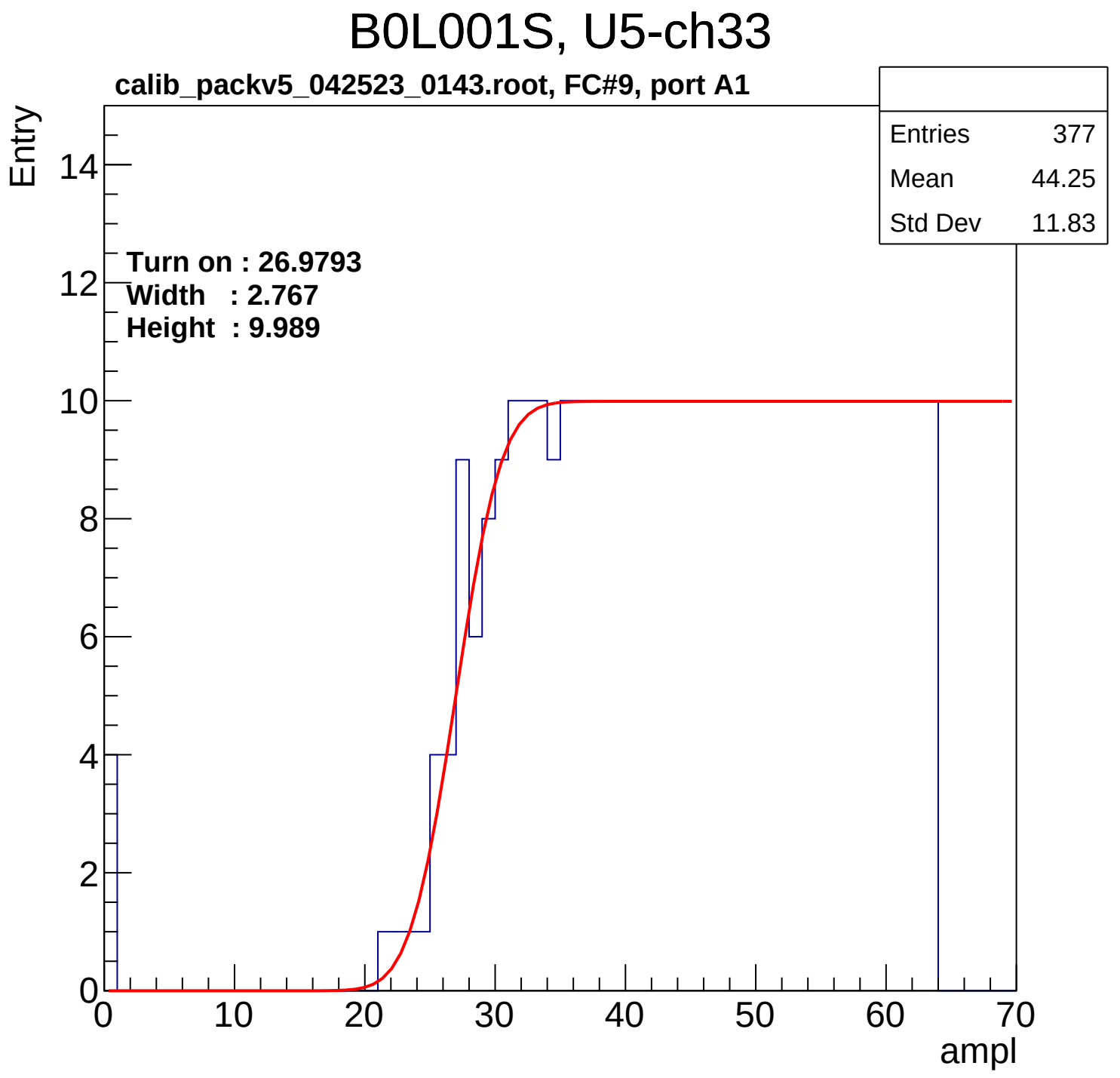
B0L001S, U5-ch33
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.25
Std Dev 11.83
Turn on : 26.9793
Width : 2.767
Height : 9.989
Entry
ampl
0
2
4
6
8
10
12
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0
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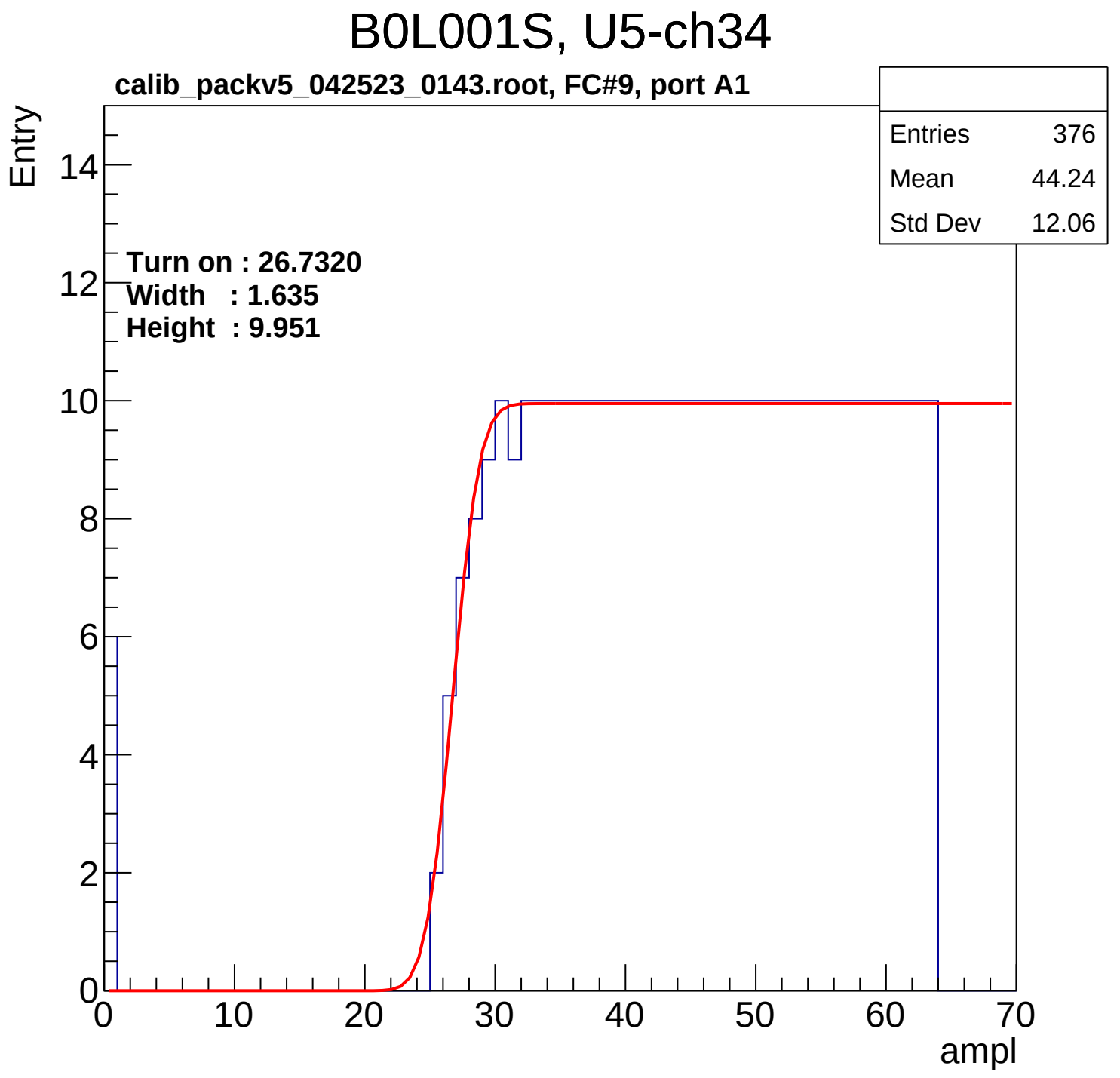
B0L001S, U5-ch34
calib_packv5_042523_0143.root, FC#9, port A1
Entries 376
Mean 44.24
Std Dev 12.06
Turn on : 26.7320
Width : 1.635
Height : 9.951
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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40
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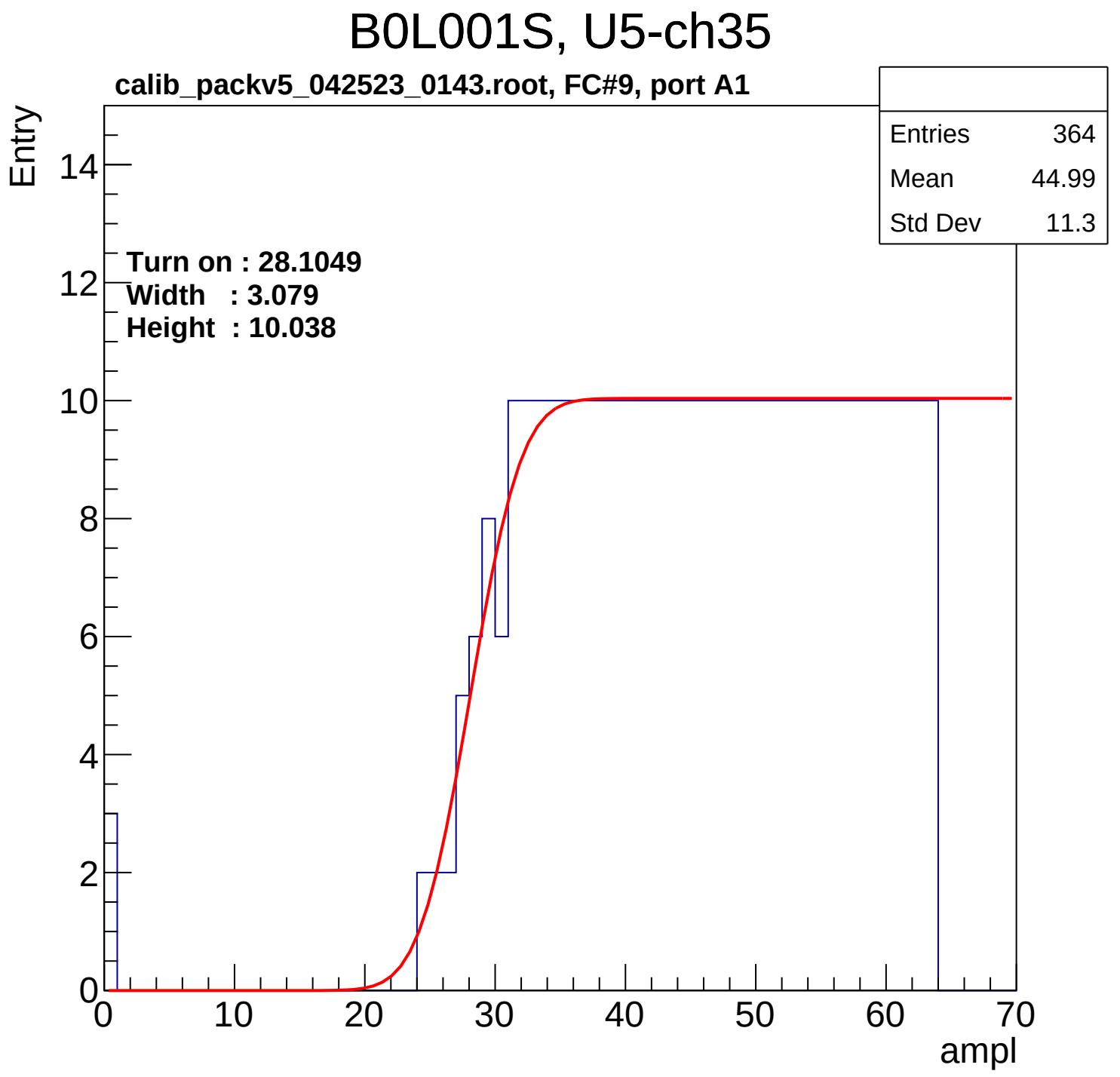
B0L001S, U5-ch35
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.99
Std Dev 11.3
Turn on : 28.1049
Width : 3.079
Height : 10.038
Entry
ampl
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2
4
6
8
10
12
14
0
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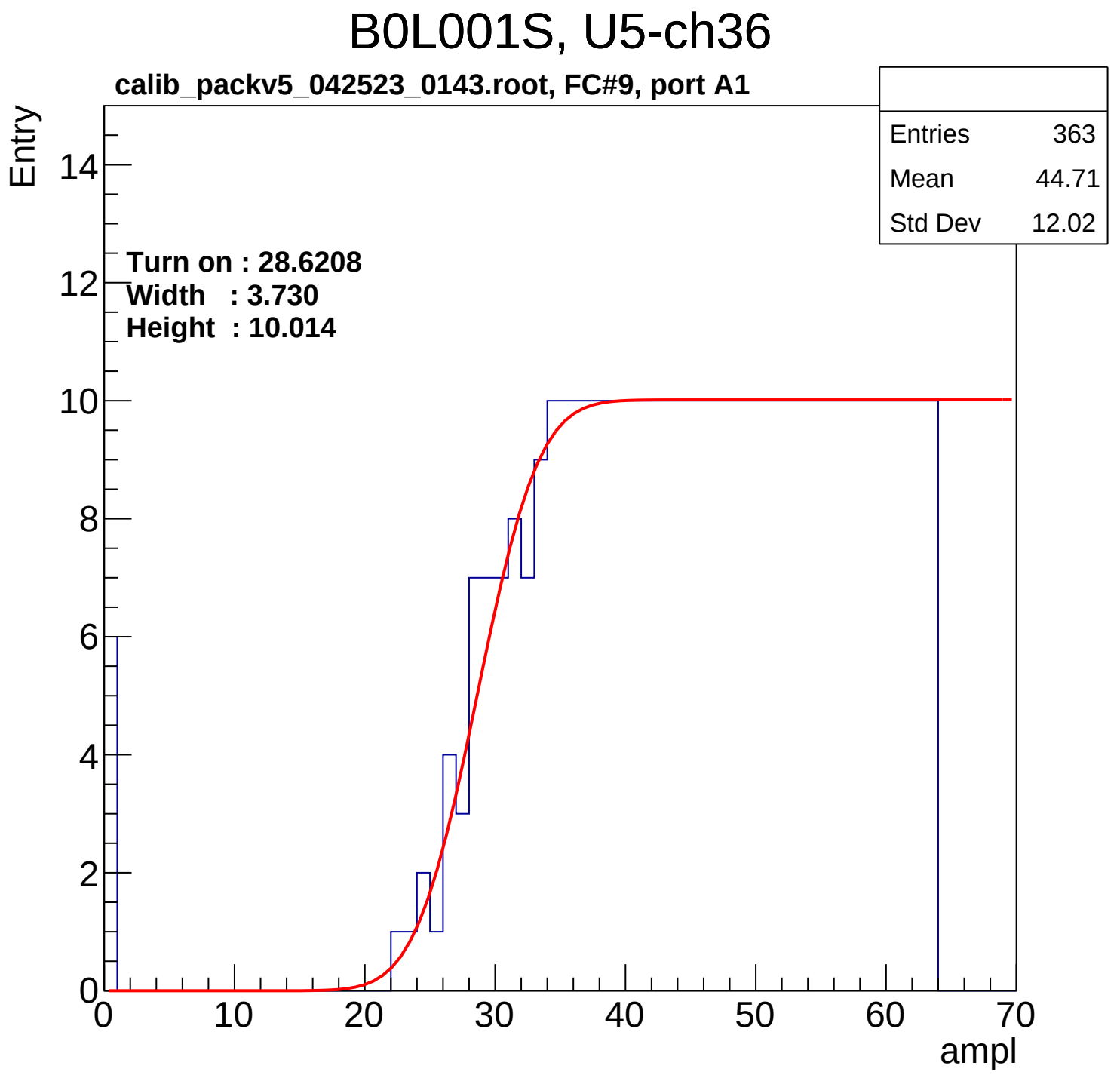
B0L001S, U5-ch36
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 44.71
Std Dev 12.02
Turn on : 28.6208
Width : 3.730
Height : 10.014
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
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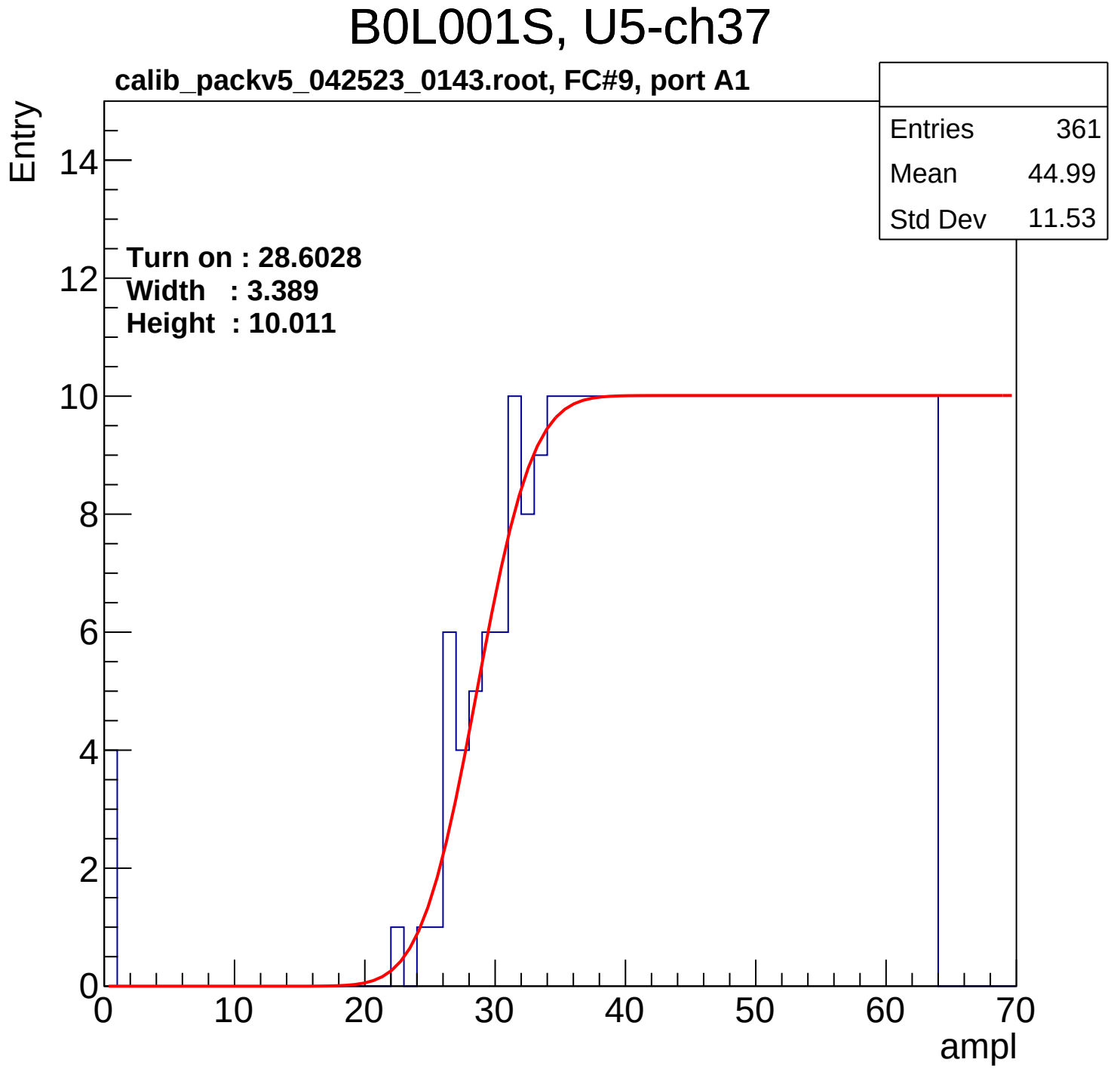
60
70


B0L001S, U5-ch37
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 44.99
Std Dev 11.53
Turn on : 28.6028
Width : 3.389
Height : 10.011
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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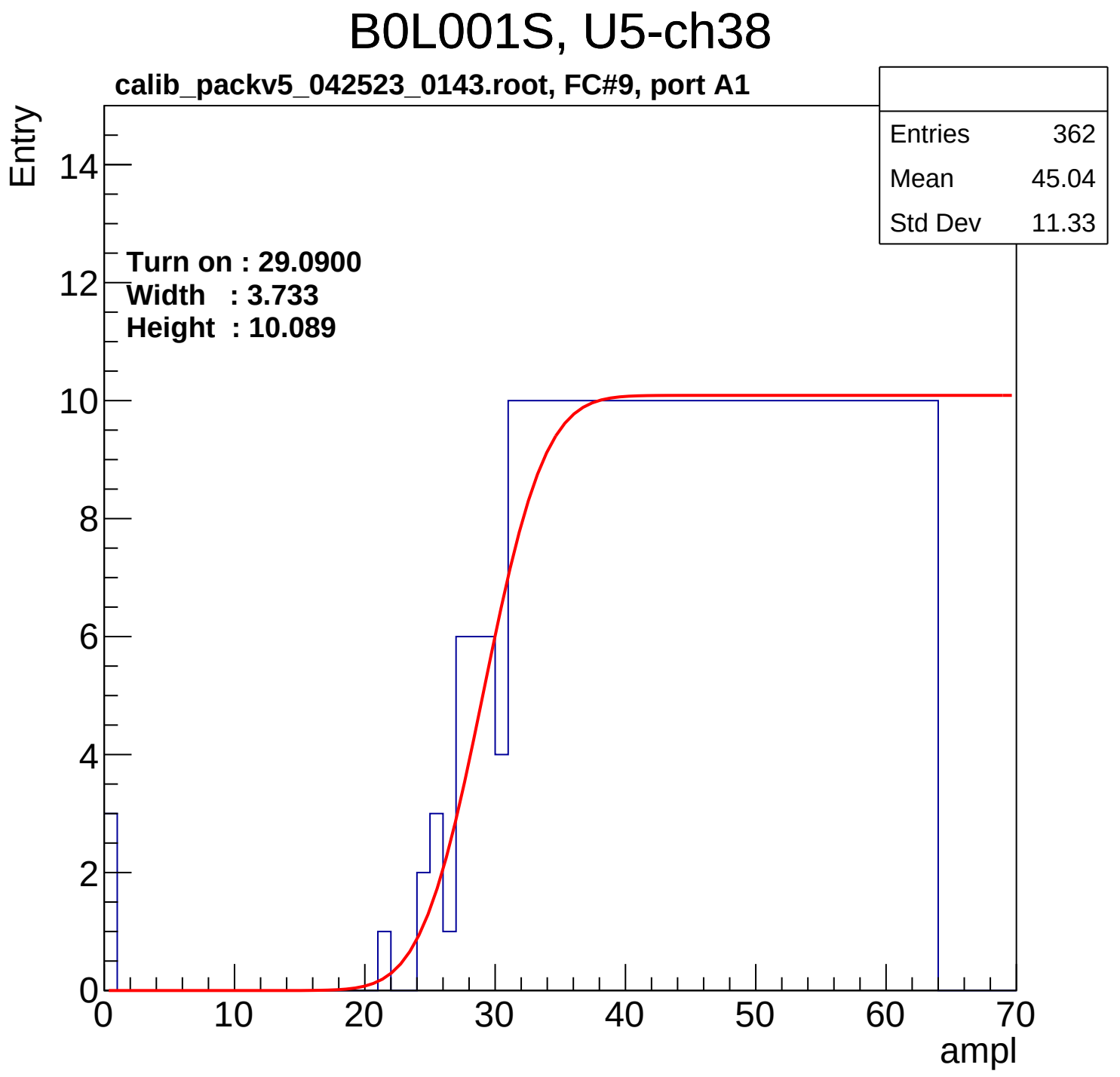
B0L001S, U5-ch38
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.04
Std Dev 11.33
Turn on : 29.0900
Width : 3.733
Height : 10.089
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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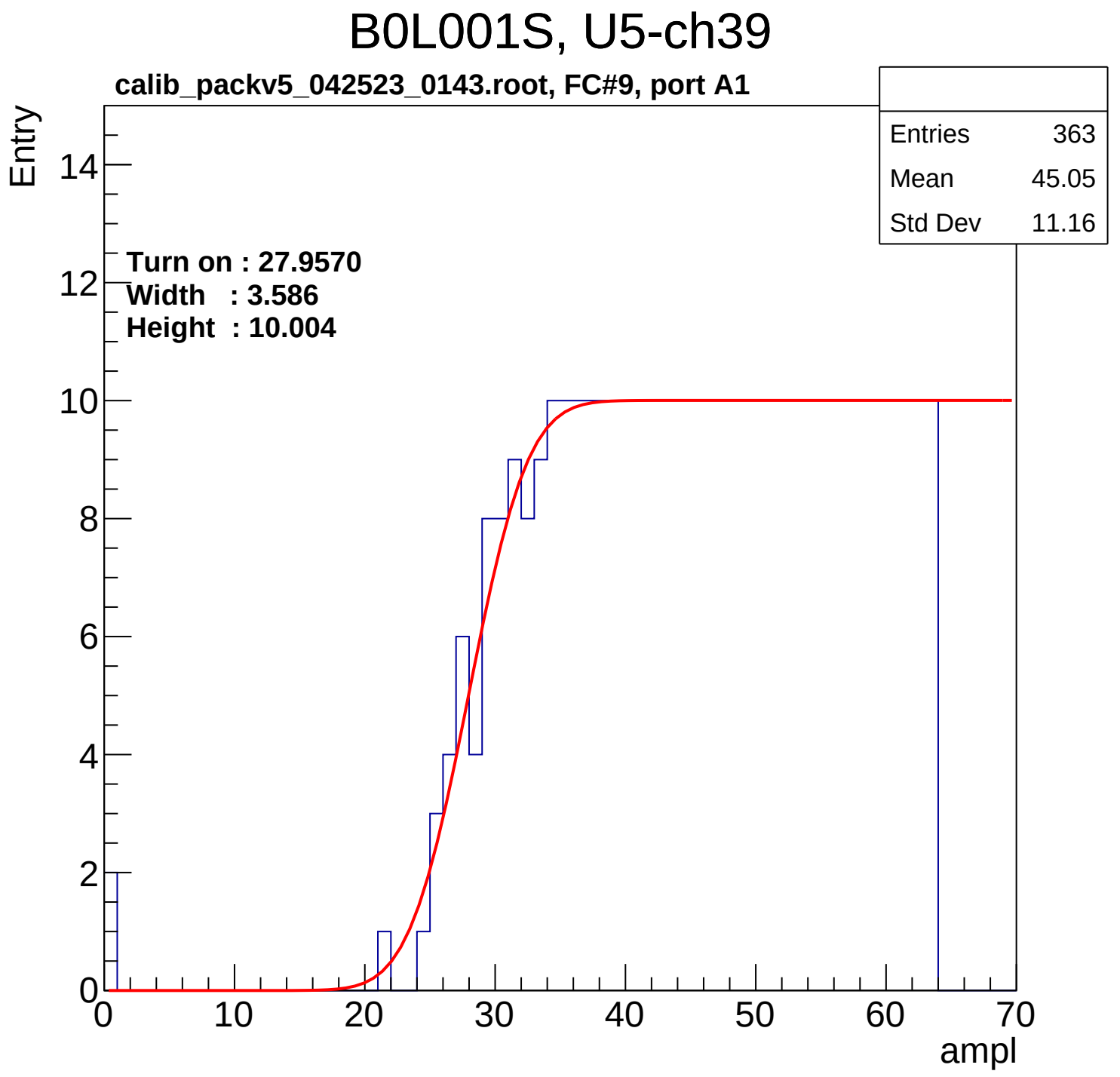
B0L001S, U5-ch39
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 45.05
Std Dev 11.16
Turn on : 27.9570
Width : 3.586
Height : 10.004
Entry
ampl
0
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4
6
8
10
12
14
0
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60
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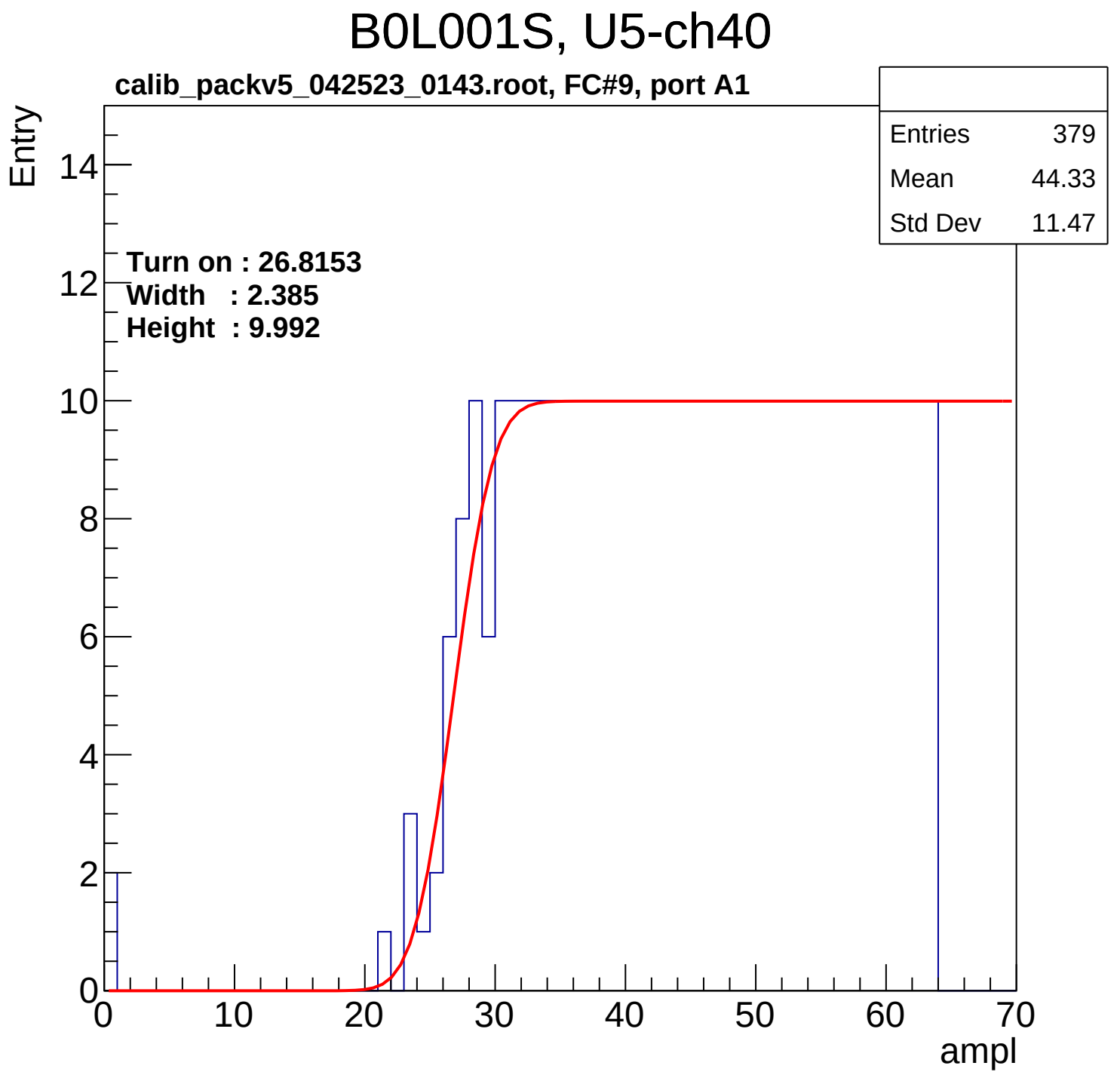
B0L001S, U5-ch40
calib_packv5_042523_0143.root, FC#9, port A1
Entries 379
Mean 44.33
Std Dev 11.47
Turn on : 26.8153
Width : 2.385
Height : 9.992
Entry
ampl
0
2
4
6
8
10
12
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0
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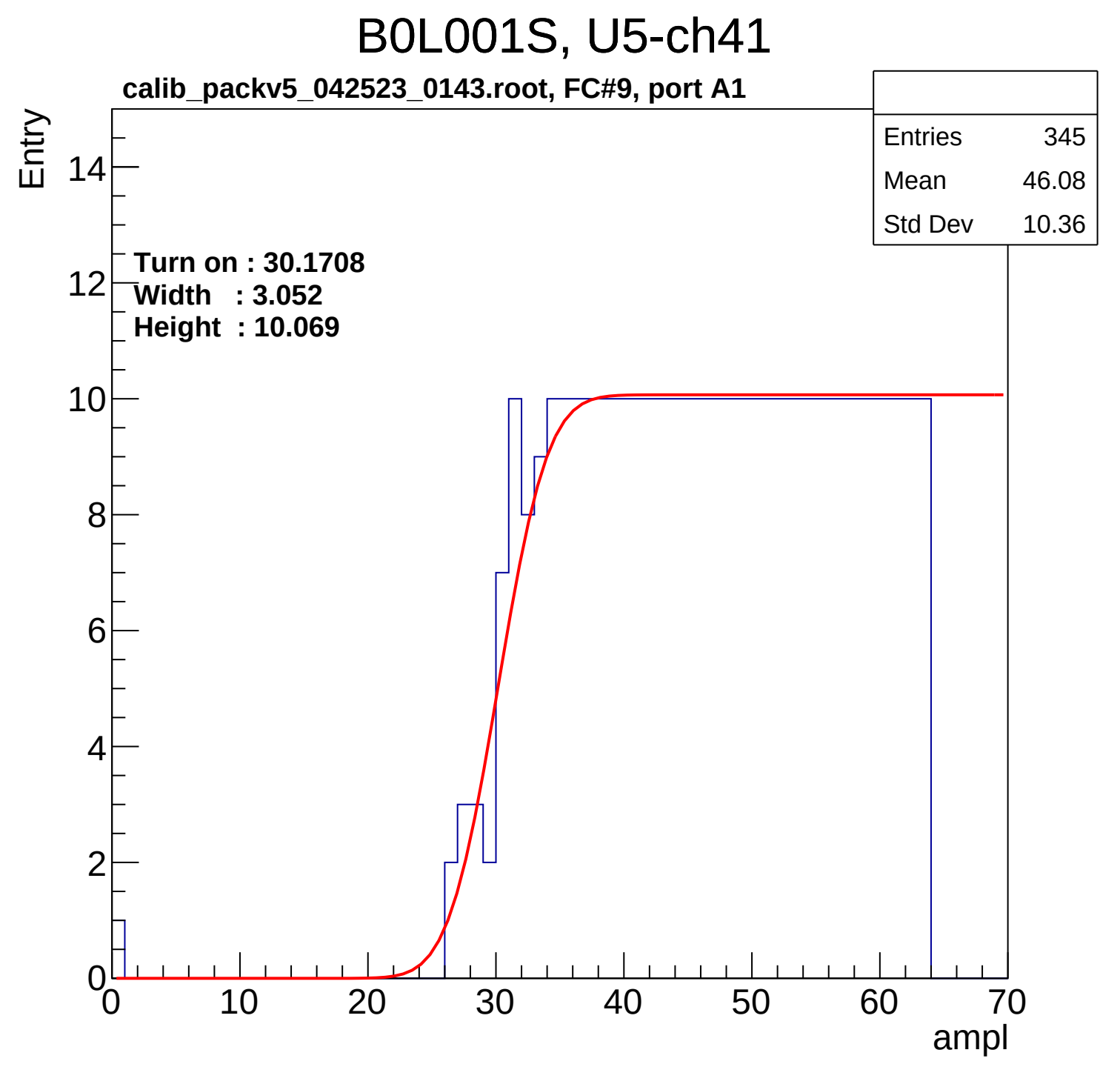
B0L001S, U5-ch41
calib_packv5_042523_0143.root, FC#9, port A1
Entries 345
Mean 46.08
Std Dev 10.36
Turn on : 30.1708
Width : 3.052
Height : 10.069
Entry
ampl
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2
4
6
8
10
12
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0
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20
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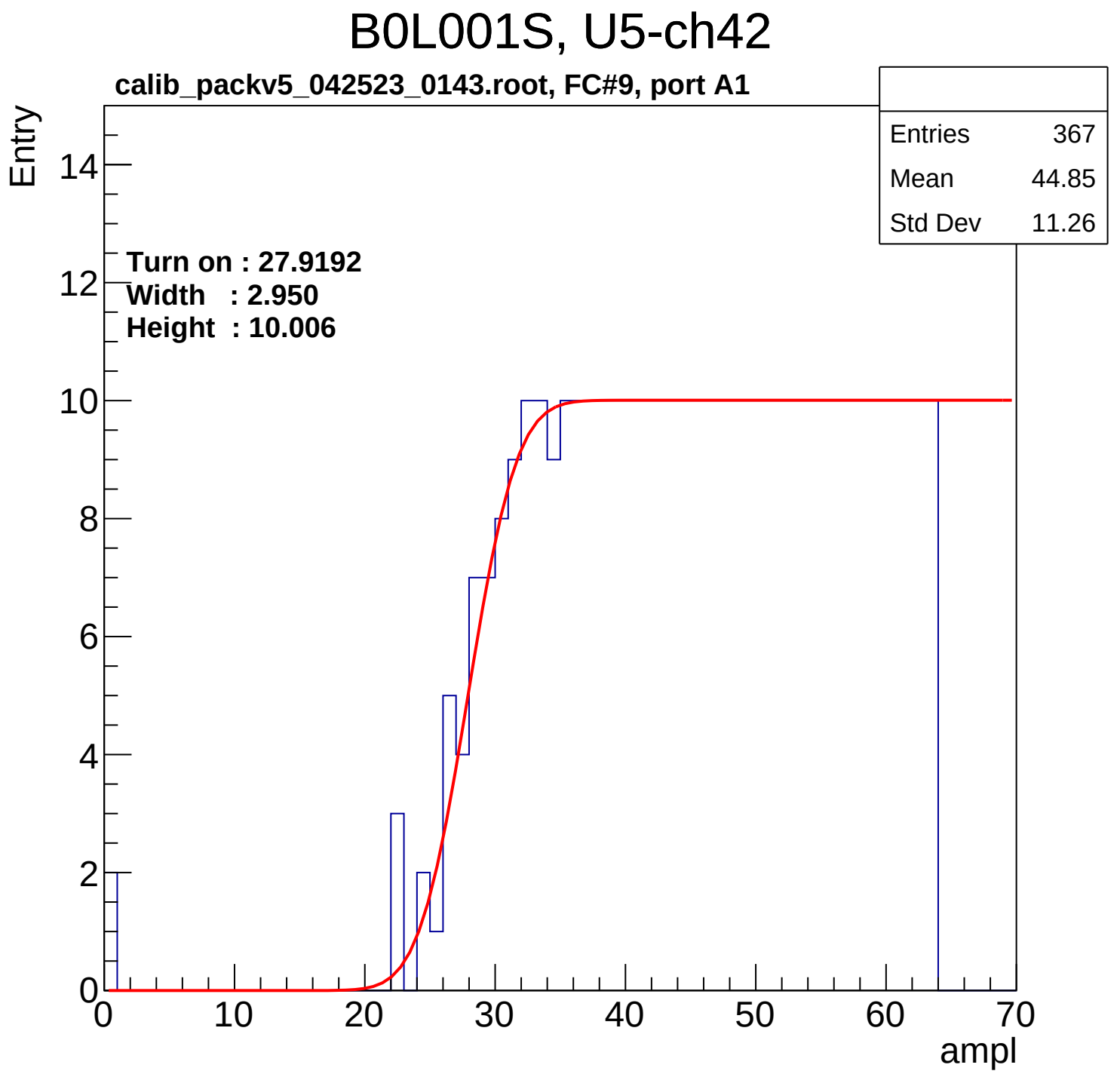
B0L001S, U5-ch42
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.85
Std Dev 11.26
Turn on : 27.9192
Width : 2.950
Height : 10.006
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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60
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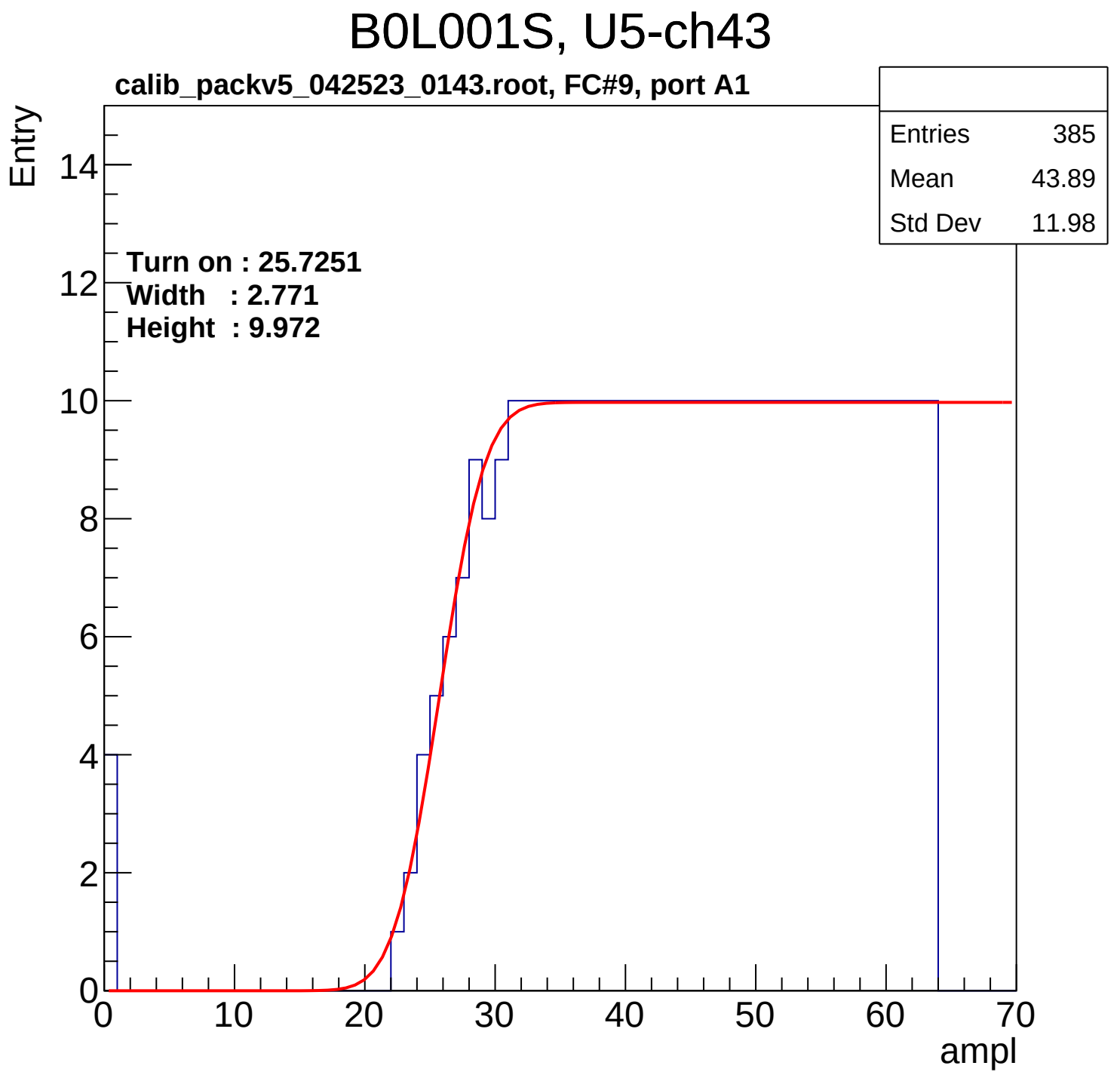
B0L001S, U5-ch43
calib_packv5_042523_0143.root, FC#9, port A1
Entries 385
Mean 43.89
Std Dev 11.98
Turn on : 25.7251
Width : 2.771
Height : 9.972
Entry
ampl
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2
4
6
8
10
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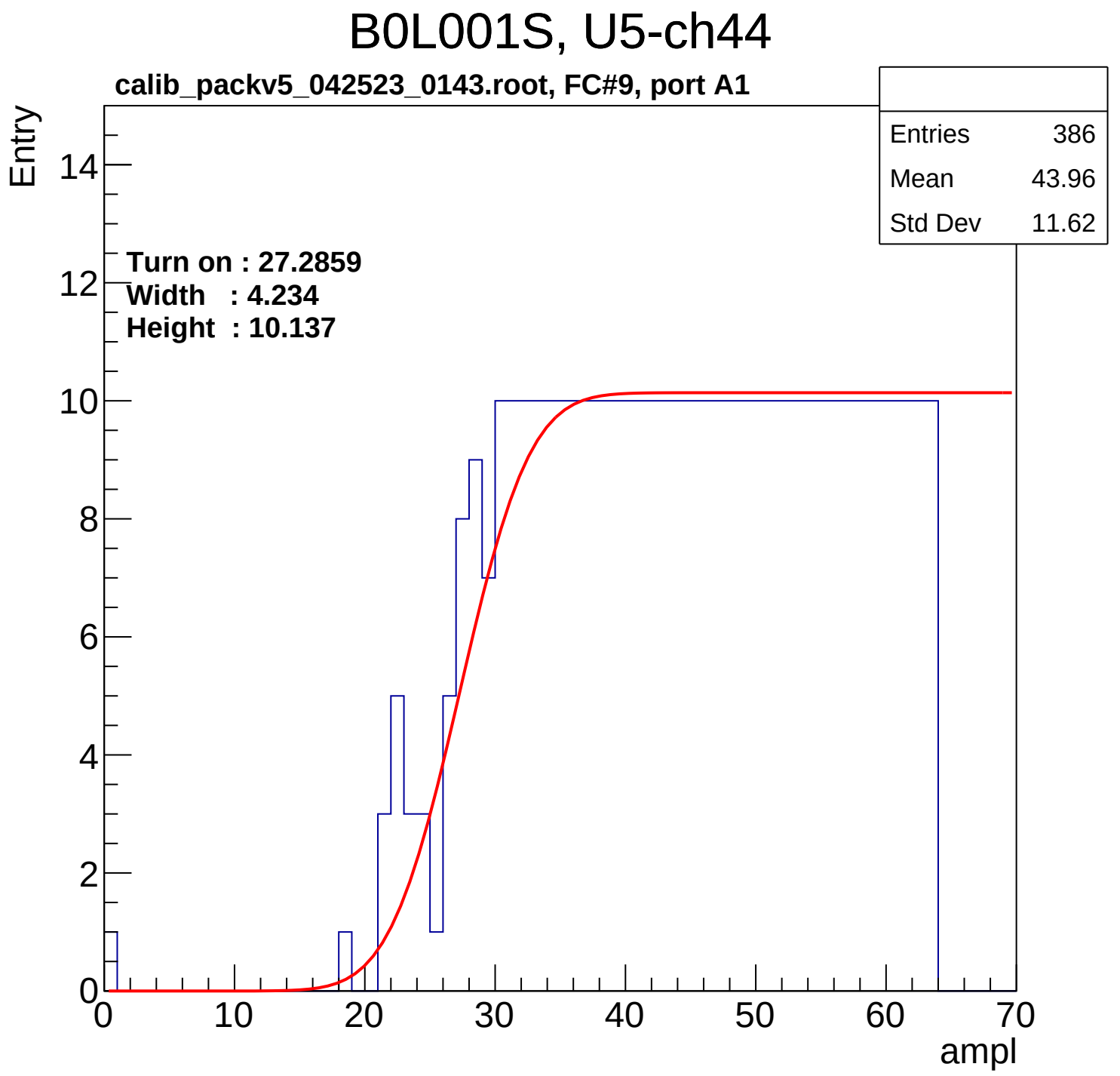
B0L001S, U5-ch44
calib_packv5_042523_0143.root, FC#9, port A1
Entries 386
Mean 43.96
Std Dev 11.62
Turn on : 27.2859
Width : 4.234
Height : 10.137
Entry
ampl
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2
4
6
8
10
12
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0
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60
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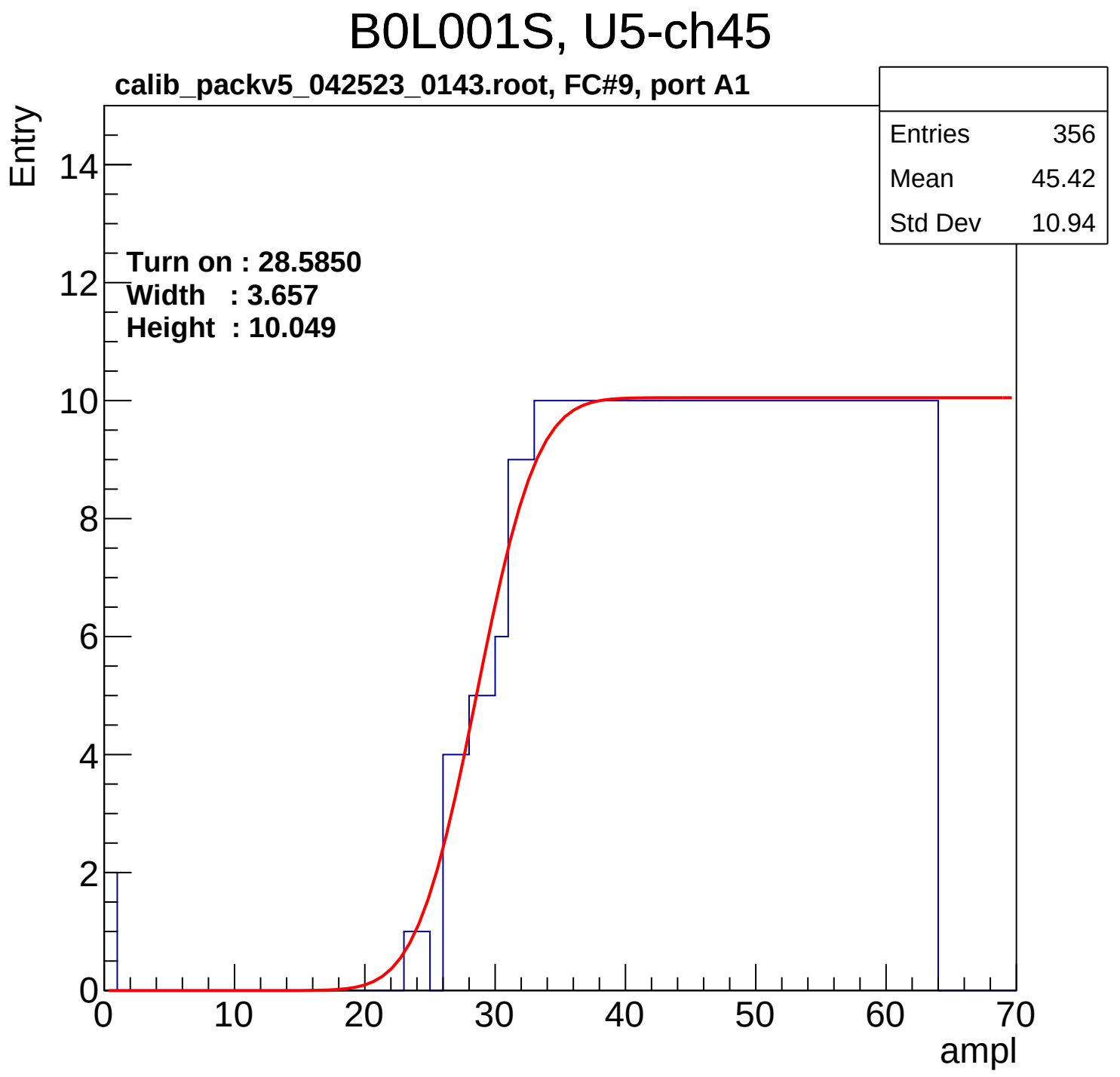
B0L001S, U5-ch45
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.42
Std Dev 10.94
Turn on : 28.5850
Width : 3.657
Height : 10.049
Entry
ampl
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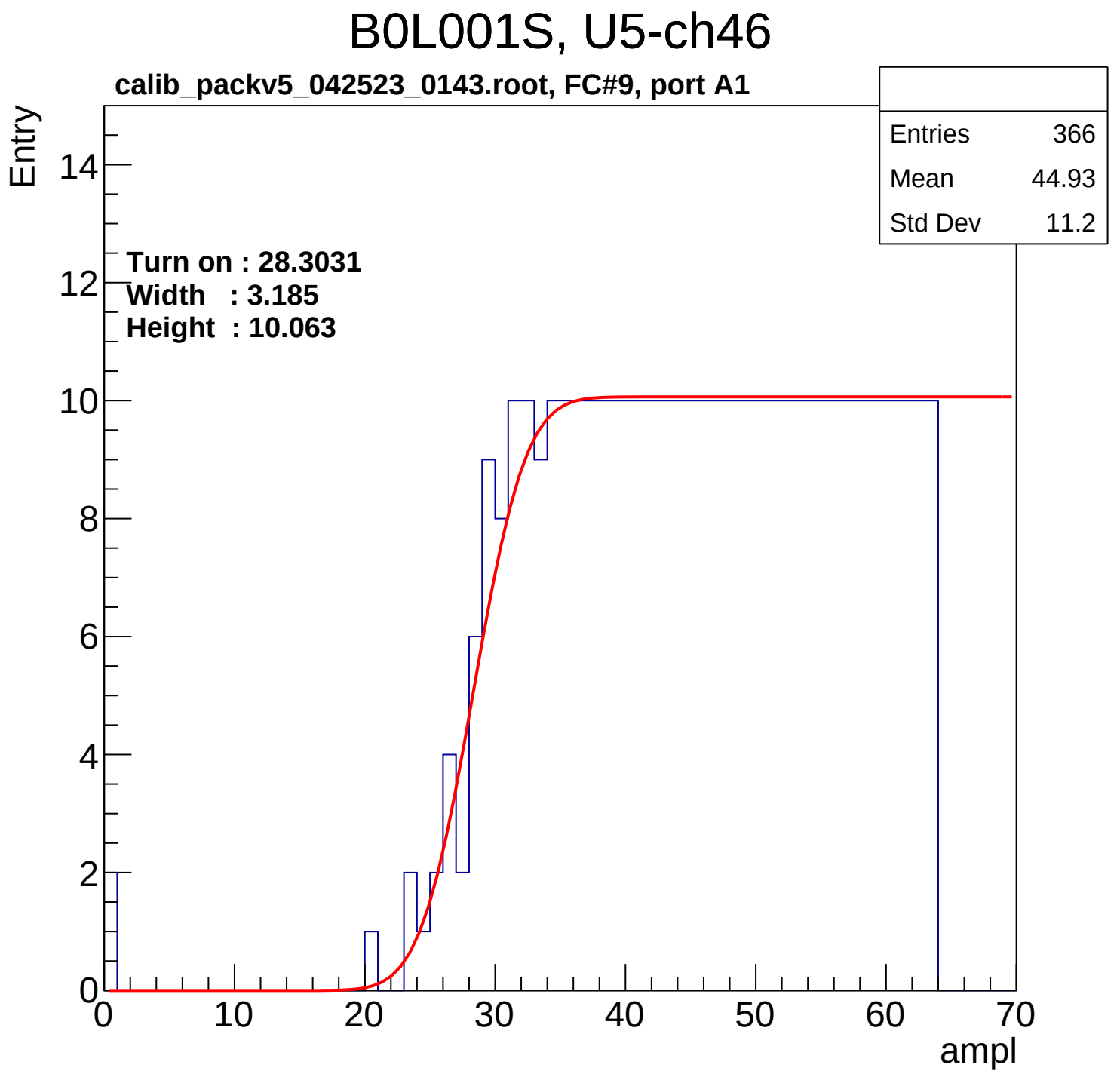
B0L001S, U5-ch46
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.93
Std Dev 11.2
Turn on : 28.3031
Width : 3.185
Height : 10.063
Entry
ampl
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8
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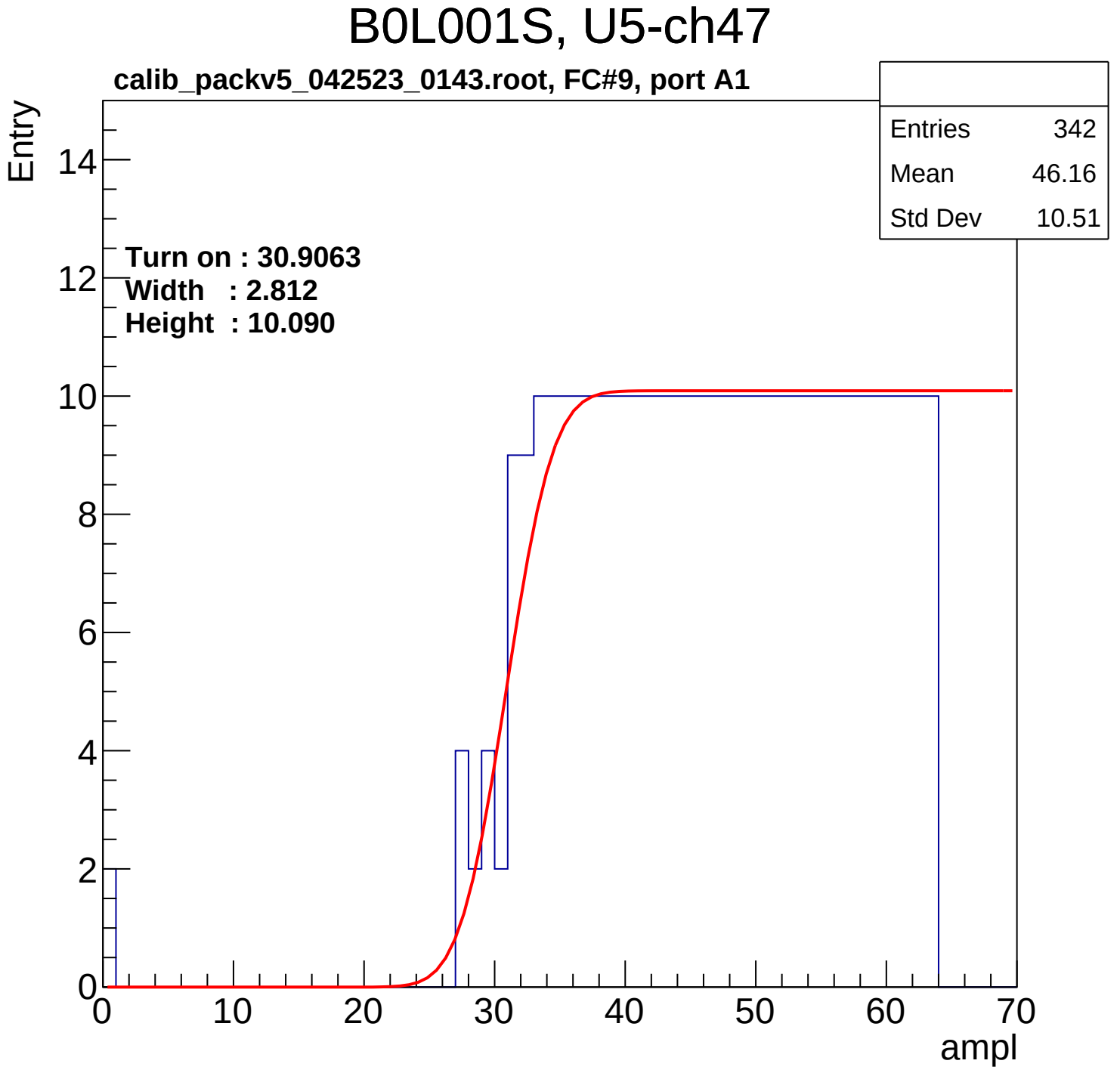
B0L001S, U5-ch47
calib_packv5_042523_0143.root, FC#9, port A1
Entries 342
Mean 46.16
Std Dev 10.51
Turn on : 30.9063
Width : 2.812
Height : 10.090
Entry
ampl
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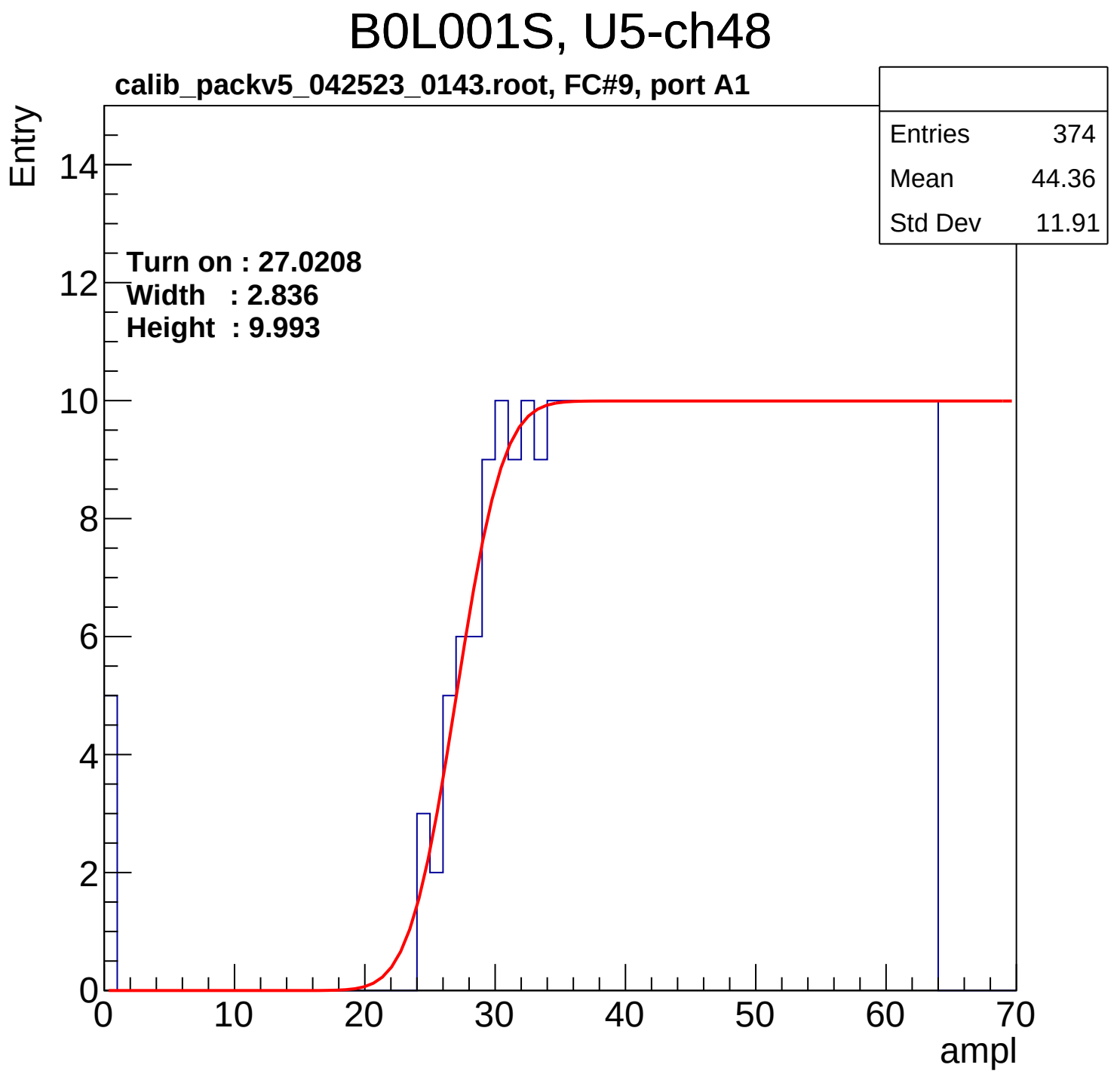
B0L001S, U5-ch48
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.36
Std Dev 11.91
Turn on : 27.0208
Width : 2.836
Height : 9.993
Entry
ampl
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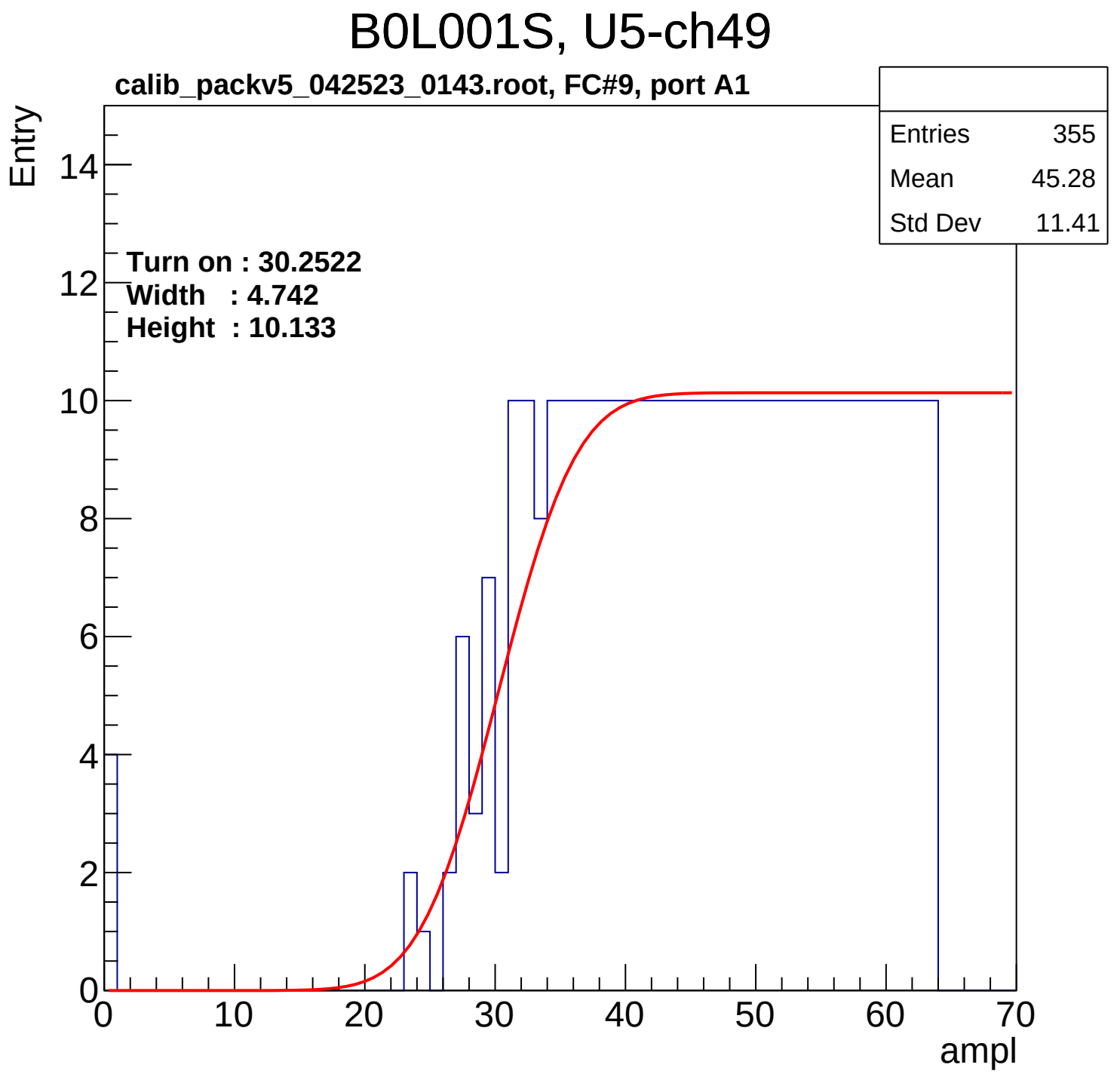
B0L001S, U5-ch49
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.28
Std Dev 11.41
Turn on : 30.2522
Width : 4.742
Height : 10.133
Entry
ampl
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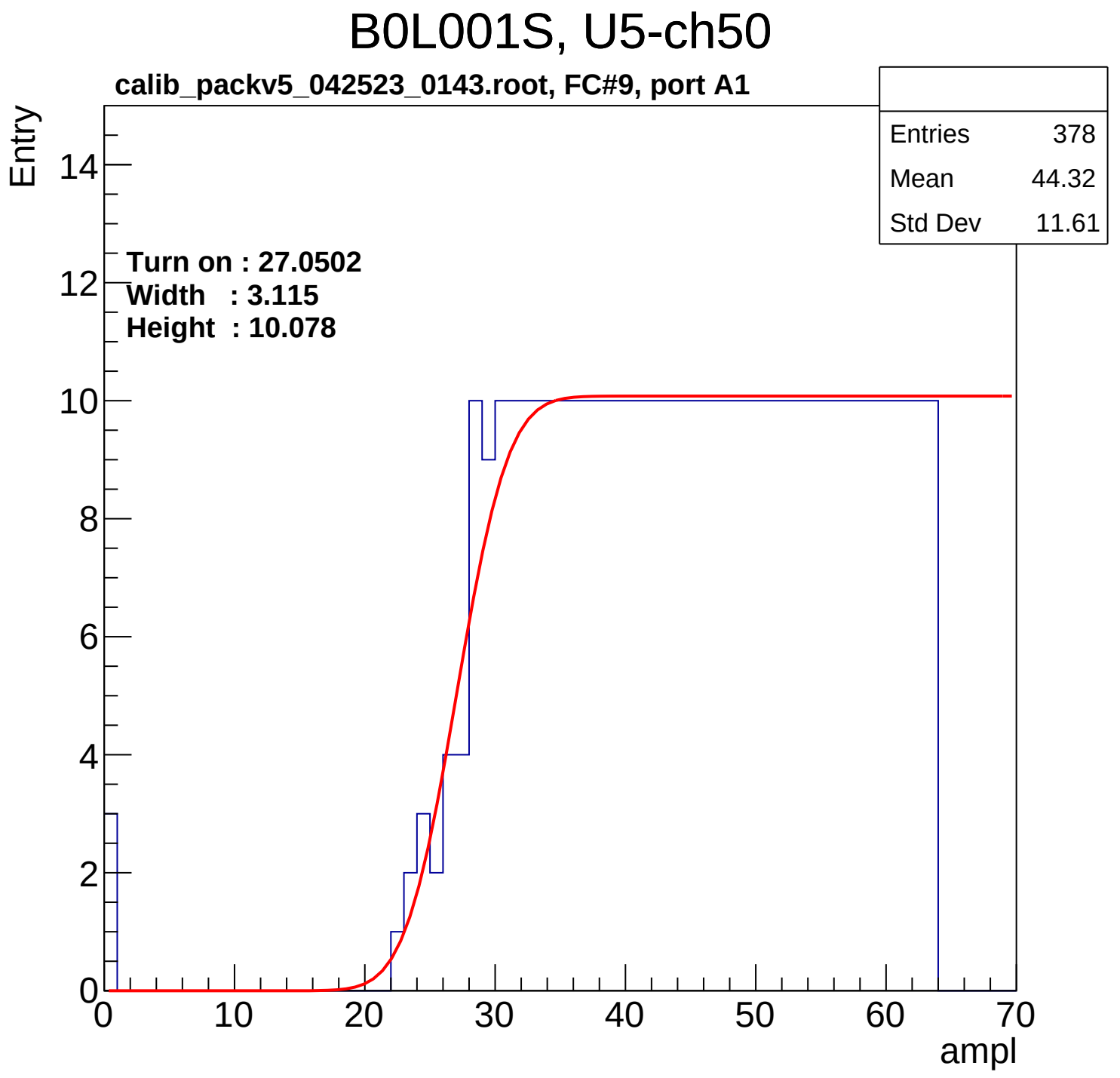
B0L001S, U5-ch50
calib_packv5_042523_0143.root, FC#9, port A1
Entries 378
Mean 44.32
Std Dev 11.61
Turn on : 27.0502
Width : 3.115
Height : 10.078
Entry
ampl
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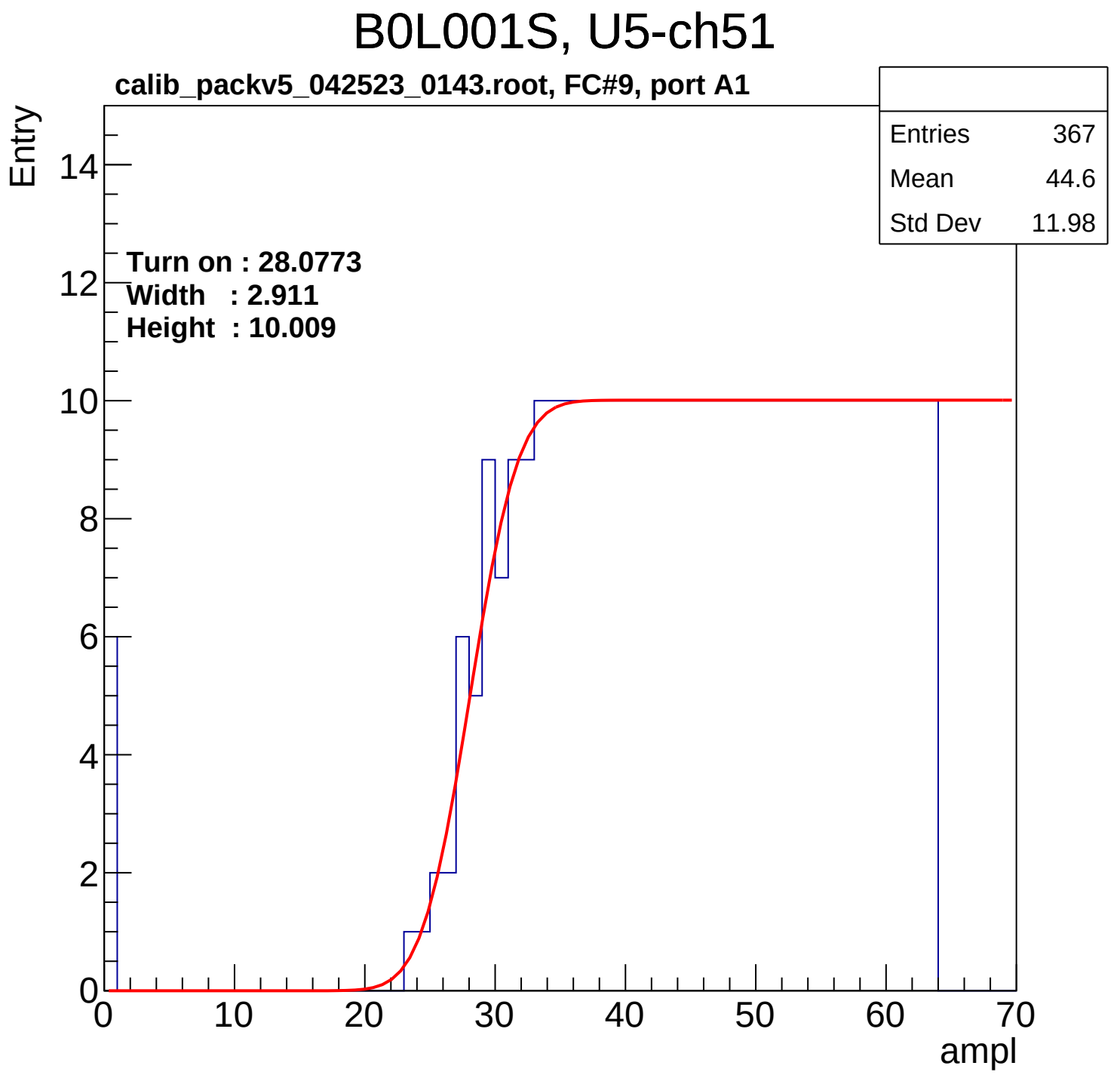
B0L001S, U5-ch51
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.6
Std Dev 11.98
Turn on : 28.0773
Width : 2.911
Height : 10.009
Entry
ampl
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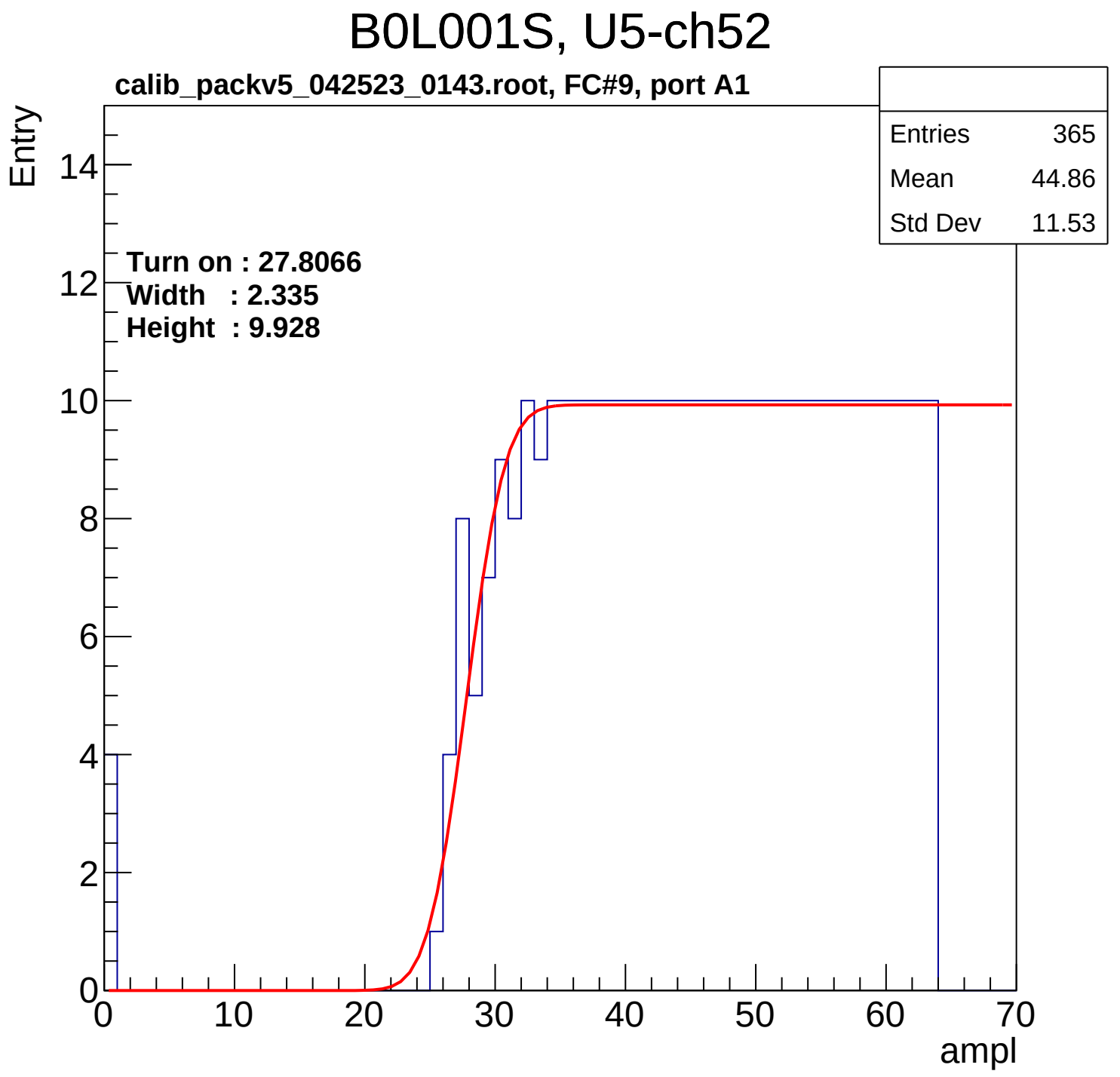
B0L001S, U5-ch52
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.86
Std Dev 11.53
Turn on : 27.8066
Width : 2.335
Height : 9.928
Entry
ampl
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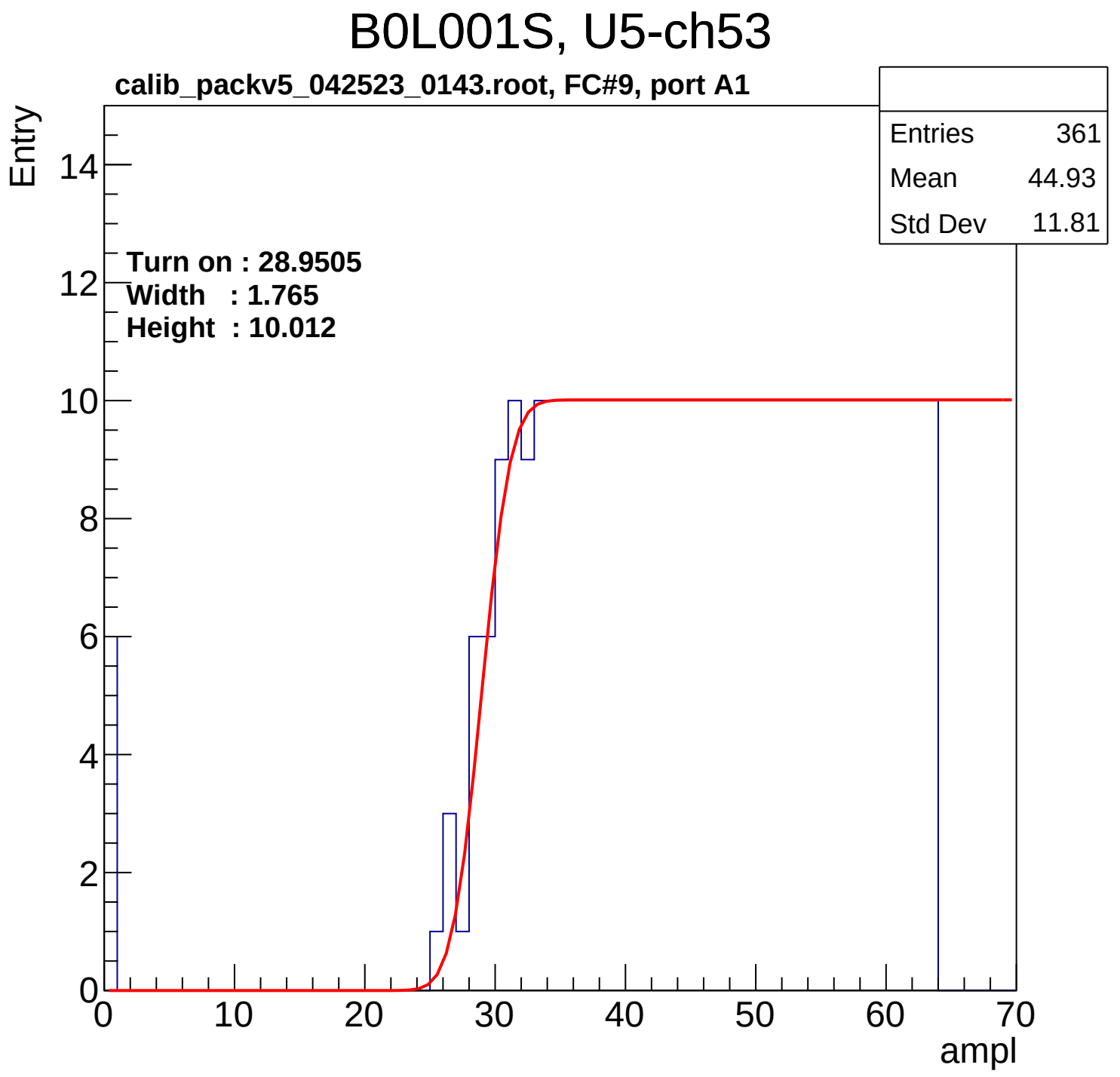
B0L001S, U5-ch53
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 44.93
Std Dev 11.81
Turn on : 28.9505
Width : 1.765
Height : 10.012
Entry
ampl
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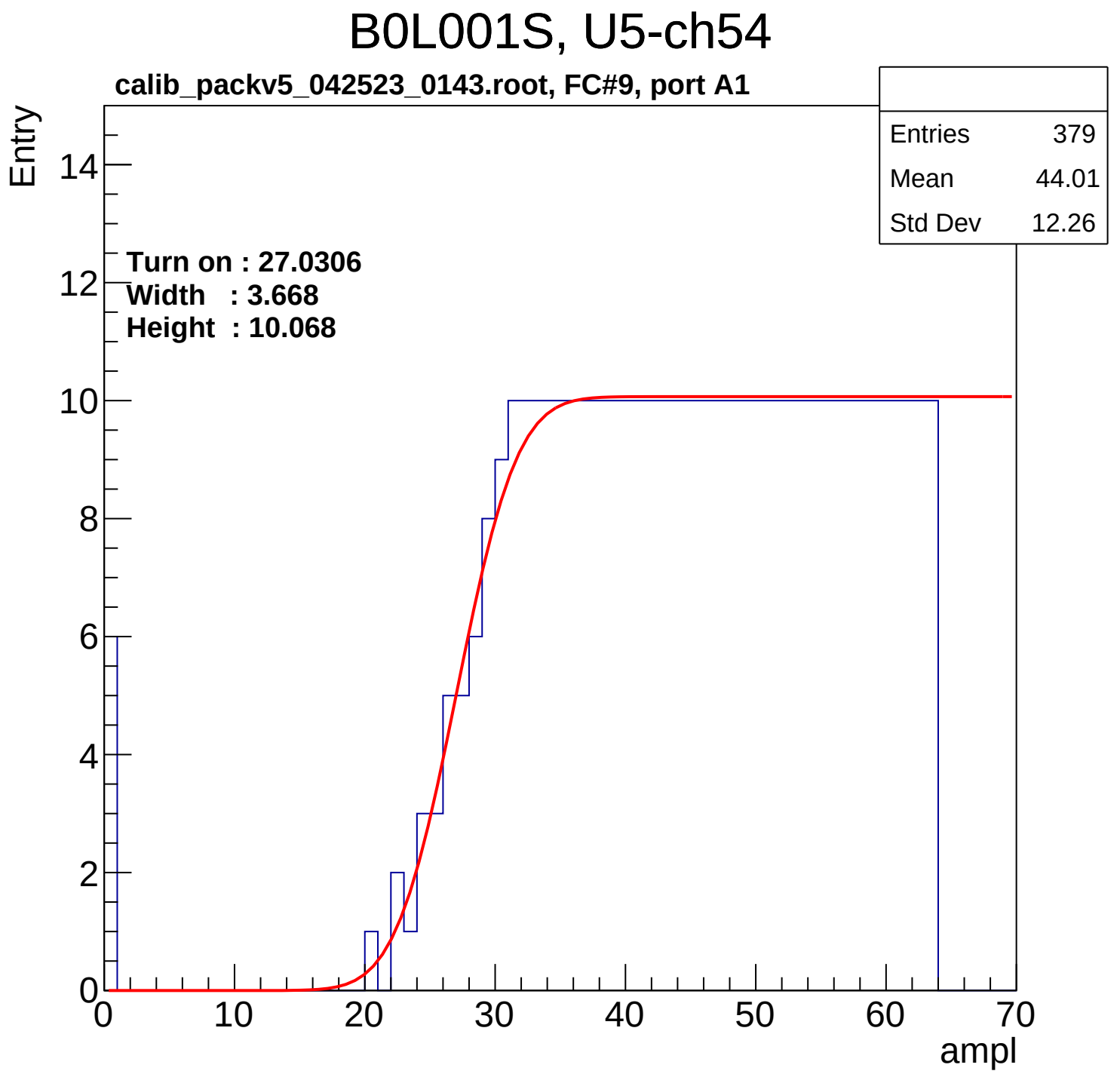
B0L001S, U5-ch54
calib_packv5_042523_0143.root, FC#9, port A1
Entries 379
Mean 44.01
Std Dev 12.26
Turn on : 27.0306
Width : 3.668
Height : 10.068
Entry
ampl
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4
6
8
10
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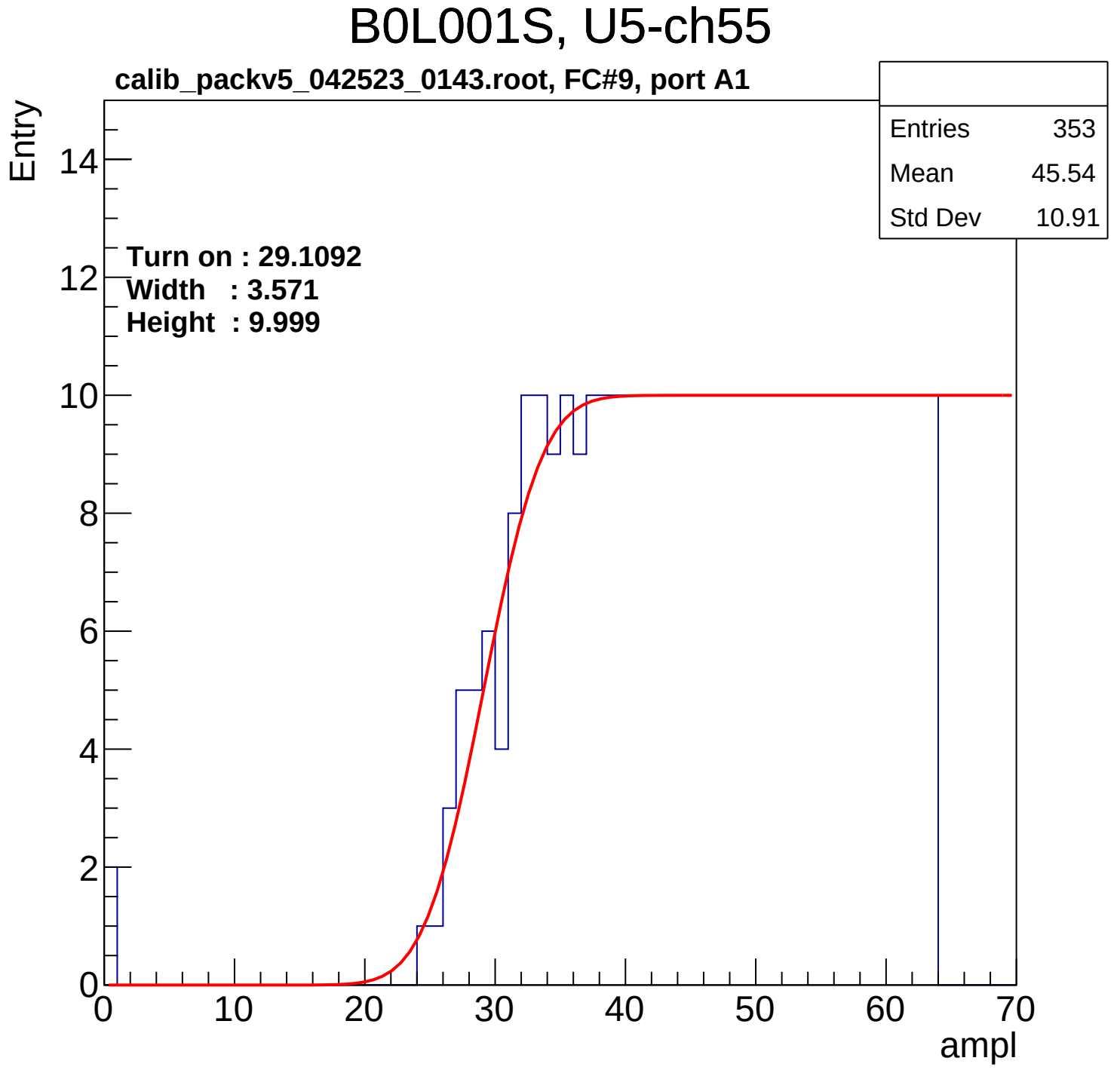
B0L001S, U5-ch55
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.54
Std Dev 10.91
Turn on : 29.1092
Width : 3.571
Height : 9.999
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ampl
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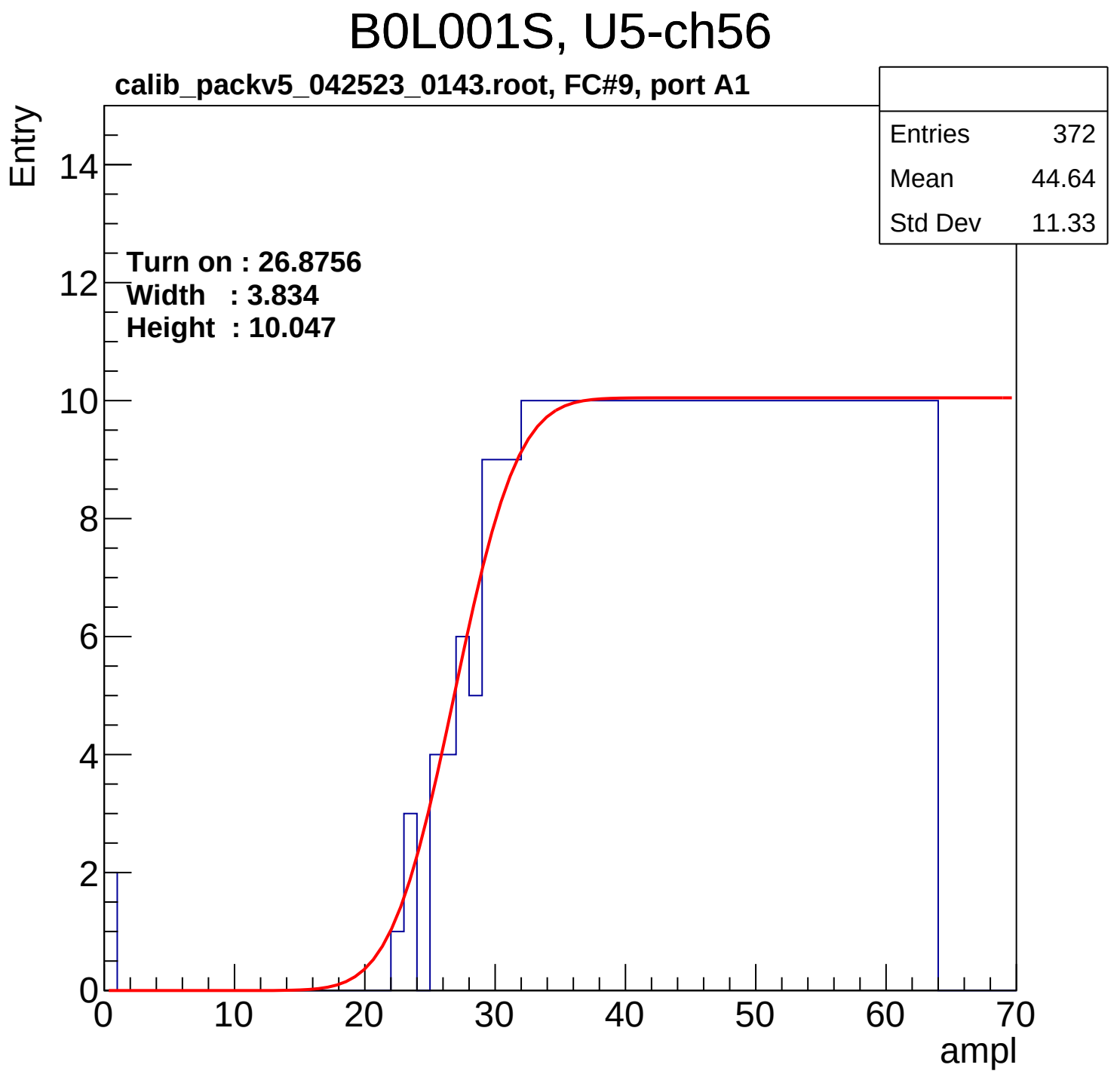
B0L001S, U5-ch56
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.64
Std Dev 11.33
Turn on : 26.8756
Width : 3.834
Height : 10.047
Entry
ampl
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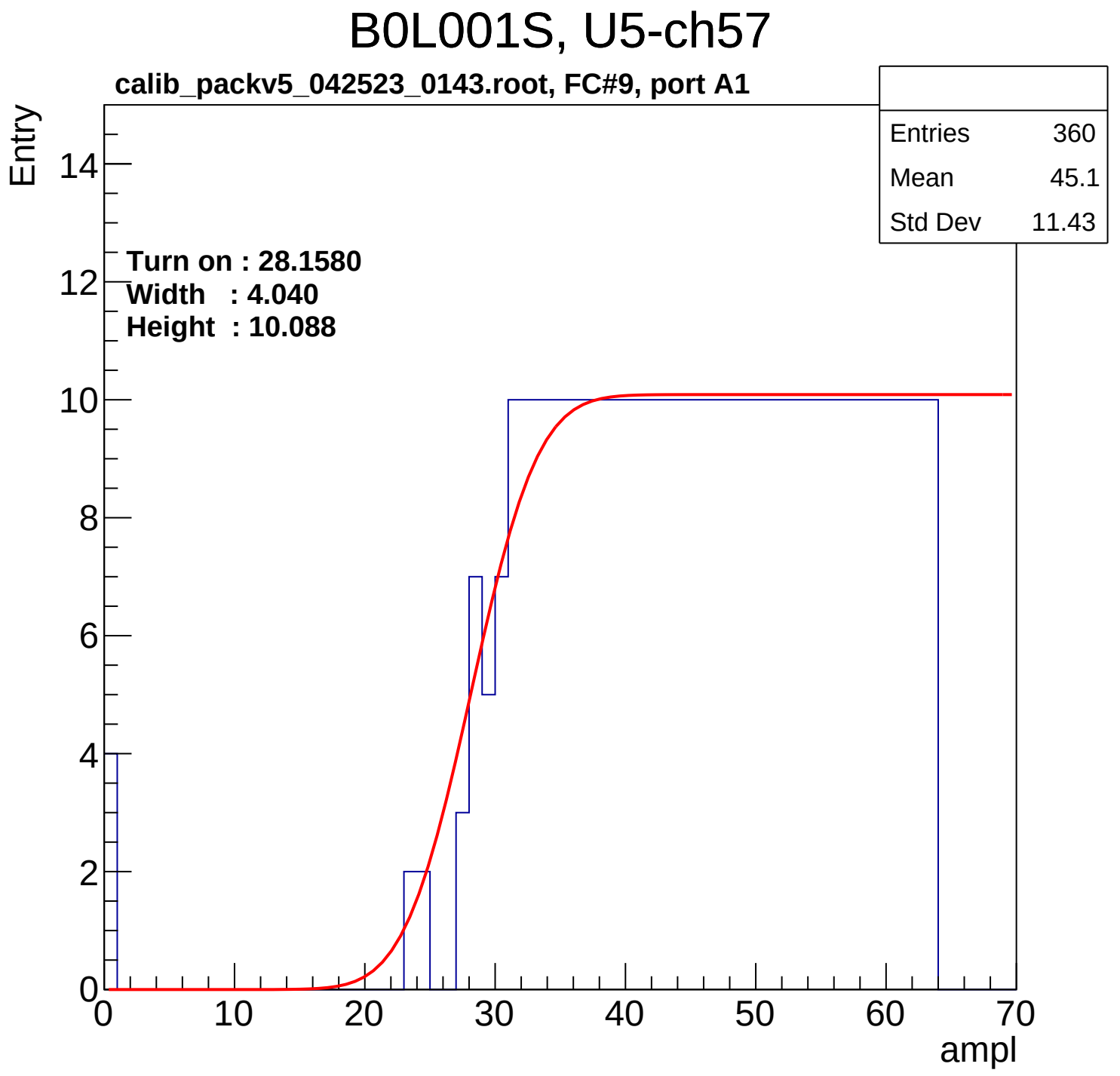
B0L001S, U5-ch57
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.1
Std Dev 11.43
Turn on : 28.1580
Width : 4.040
Height : 10.088
Entry
ampl
0
2
4
6
8
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10
20
30
40
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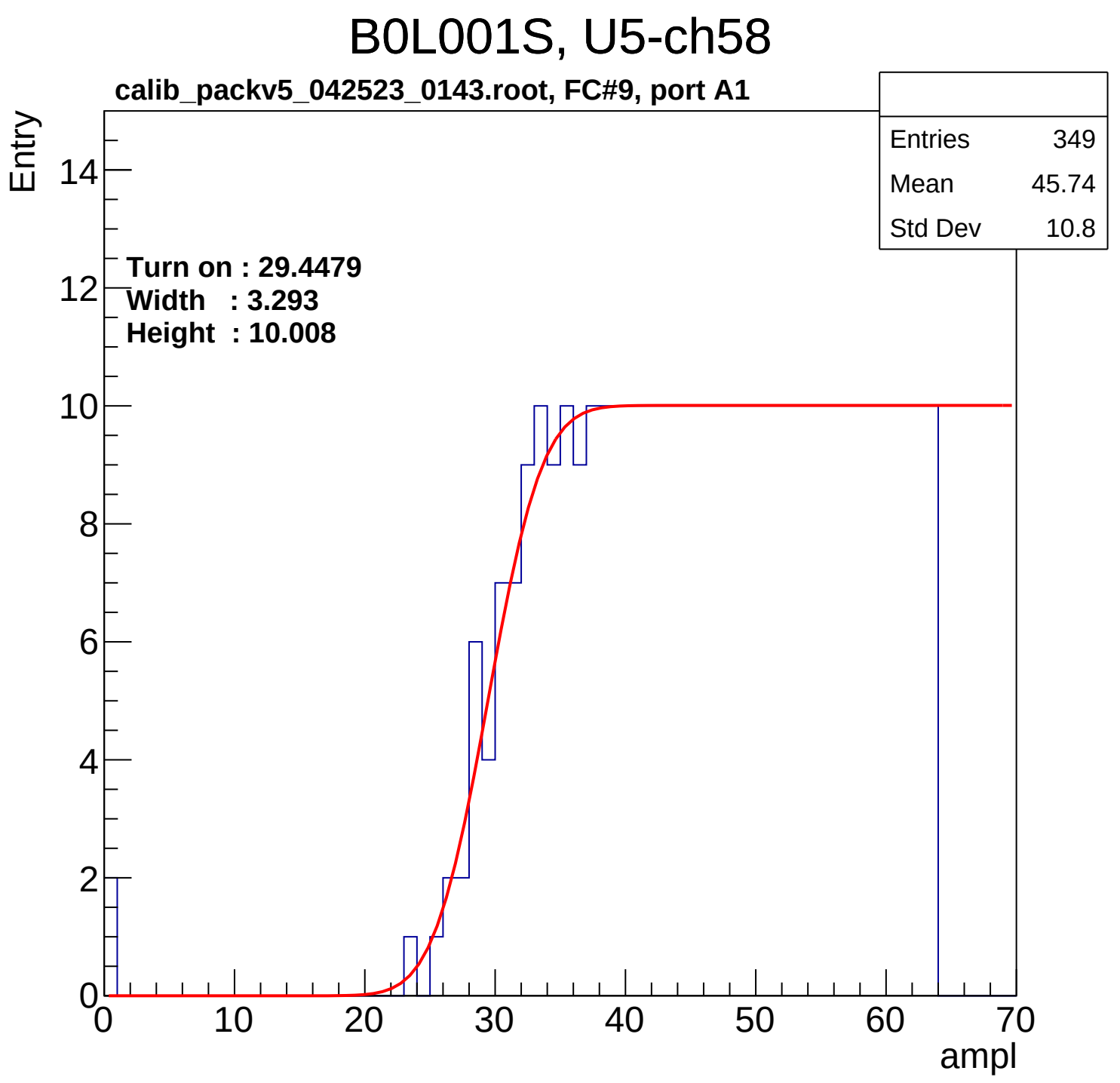
B0L001S, U5-ch58
calib_packv5_042523_0143.root, FC#9, port A1
Entries 349
Mean 45.74
Std Dev 10.8
Turn on : 29.4479
Width : 3.293
Height : 10.008
Entry
ampl
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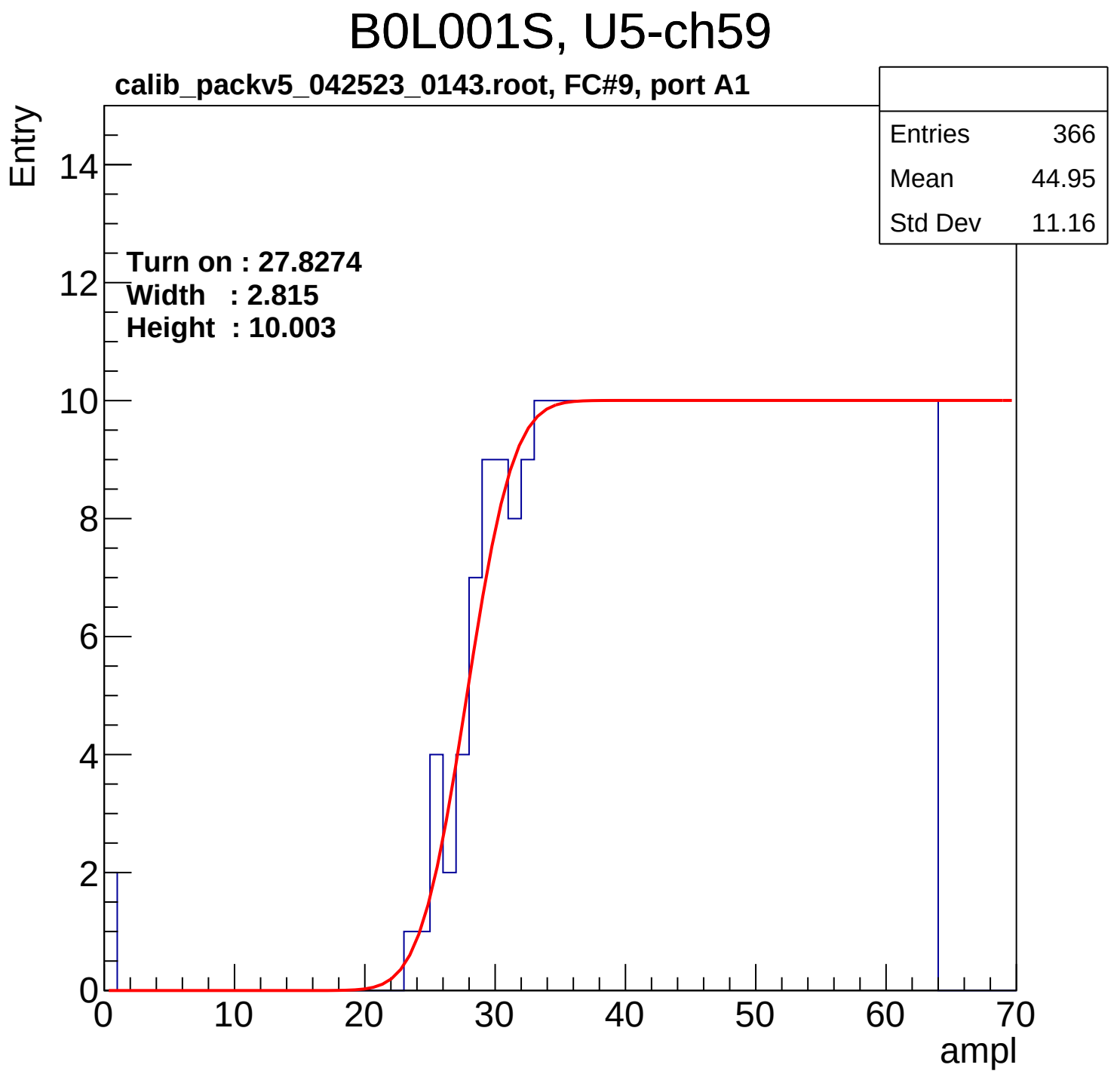
B0L001S, U5-ch59
calib_packv5_042523_0143.root, FC#9, port A1
Entries 366
Mean 44.95
Std Dev 11.16
Turn on : 27.8274
Width : 2.815
Height : 10.003
Entry
ampl
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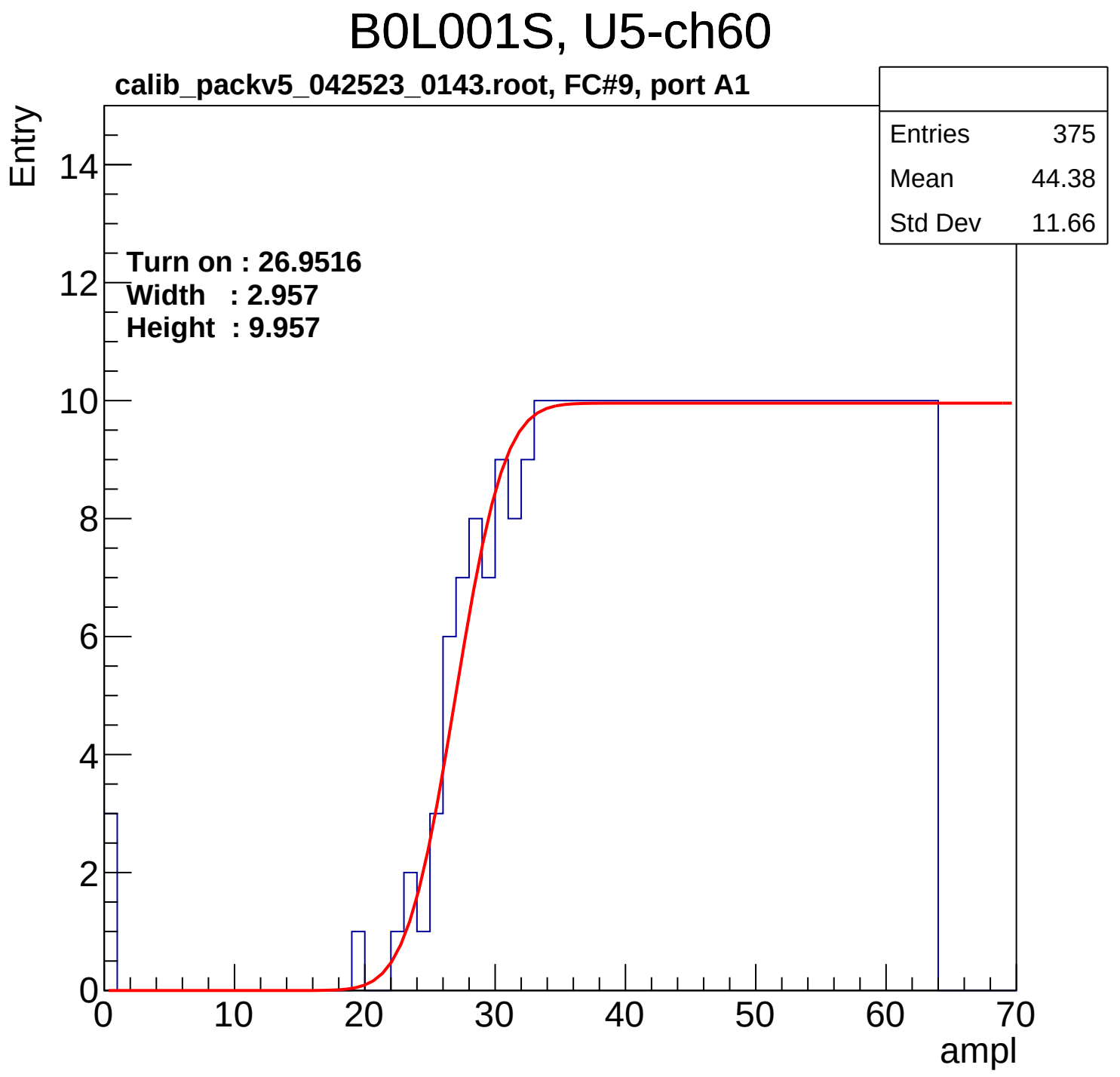
B0L001S, U5-ch60
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.38
Std Dev 11.66
Turn on : 26.9516
Width : 2.957
Height : 9.957
Entry
ampl
0
2
4
6
8
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60
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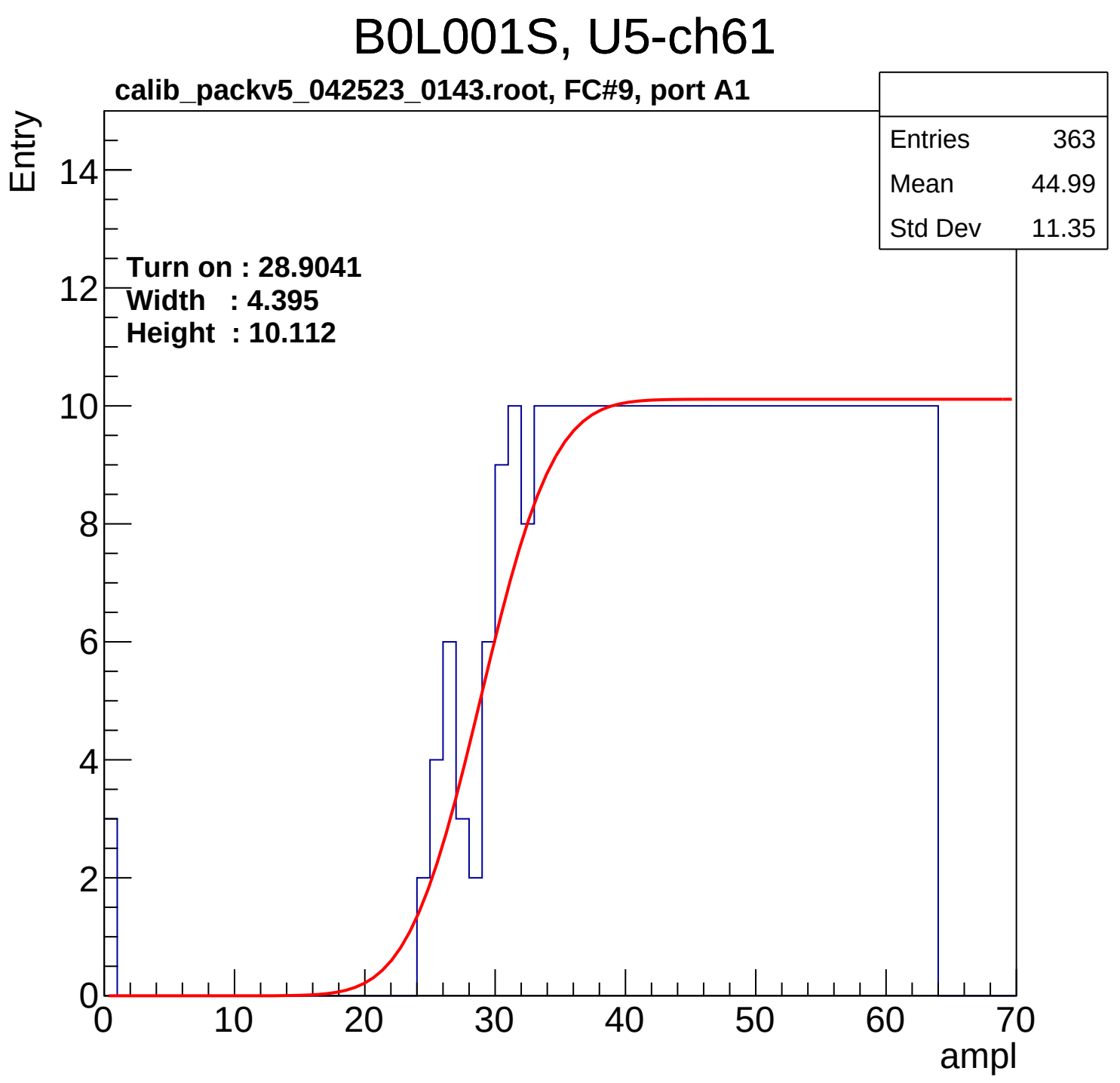
B0L001S, U5-ch61
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 44.99
Std Dev 11.35
Turn on : 28.9041
Width : 4.395
Height : 10.112
Entry
ampl
0
2
4
6
8
10
12
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0
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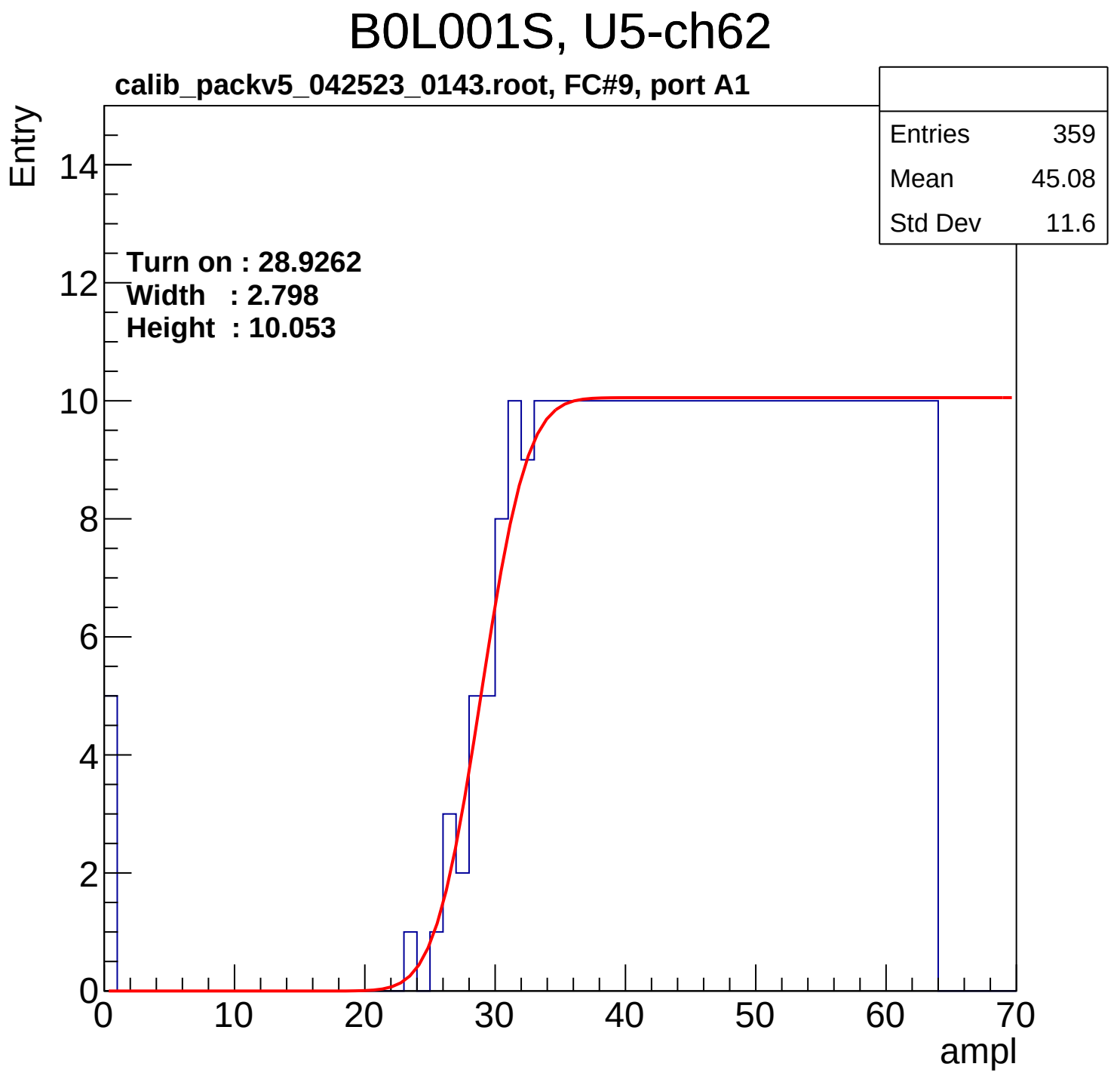
B0L001S, U5-ch62
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.08
Std Dev 11.6
Turn on : 28.9262
Width : 2.798
Height : 10.053
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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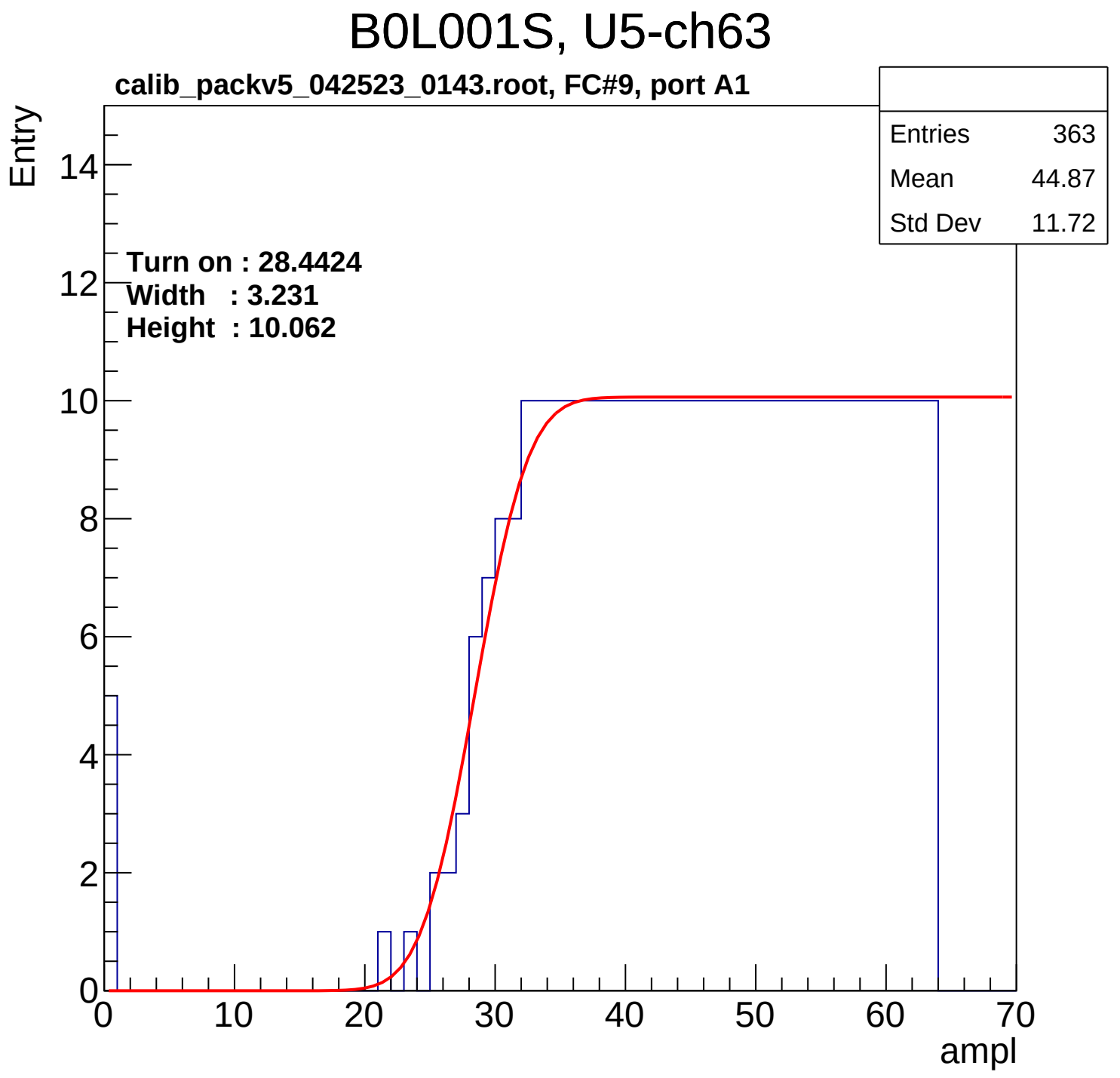
B0L001S, U5-ch63
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 44.87
Std Dev 11.72
Turn on : 28.4424
Width : 3.231
Height : 10.062
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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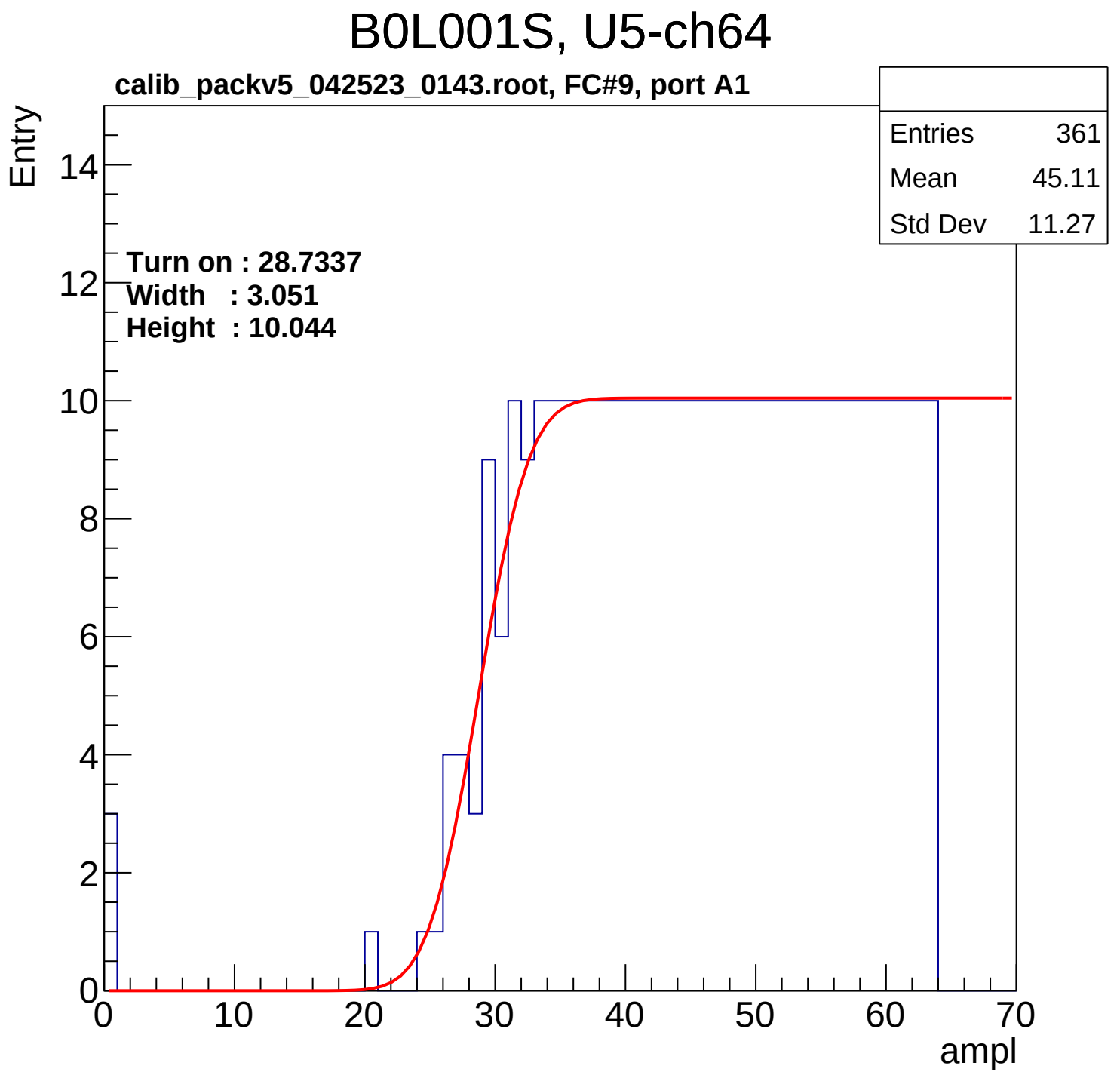
B0L001S, U5-ch64
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.11
Std Dev 11.27
Turn on : 28.7337
Width : 3.051
Height : 10.044
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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40
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60
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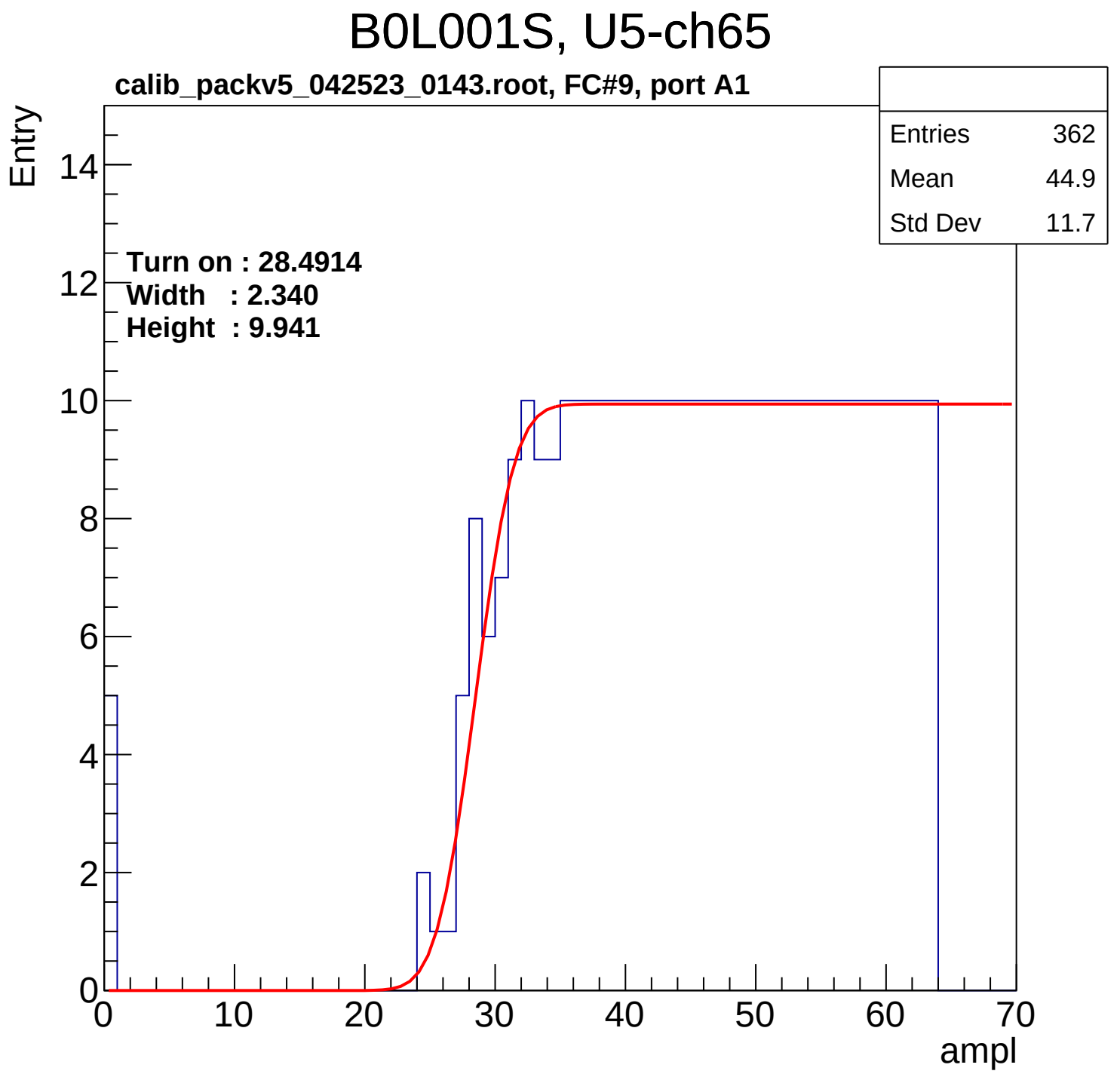
B0L001S, U5-ch65
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 44.9
Std Dev 11.7
Turn on : 28.4914
Width : 2.340
Height : 9.941
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
50
60
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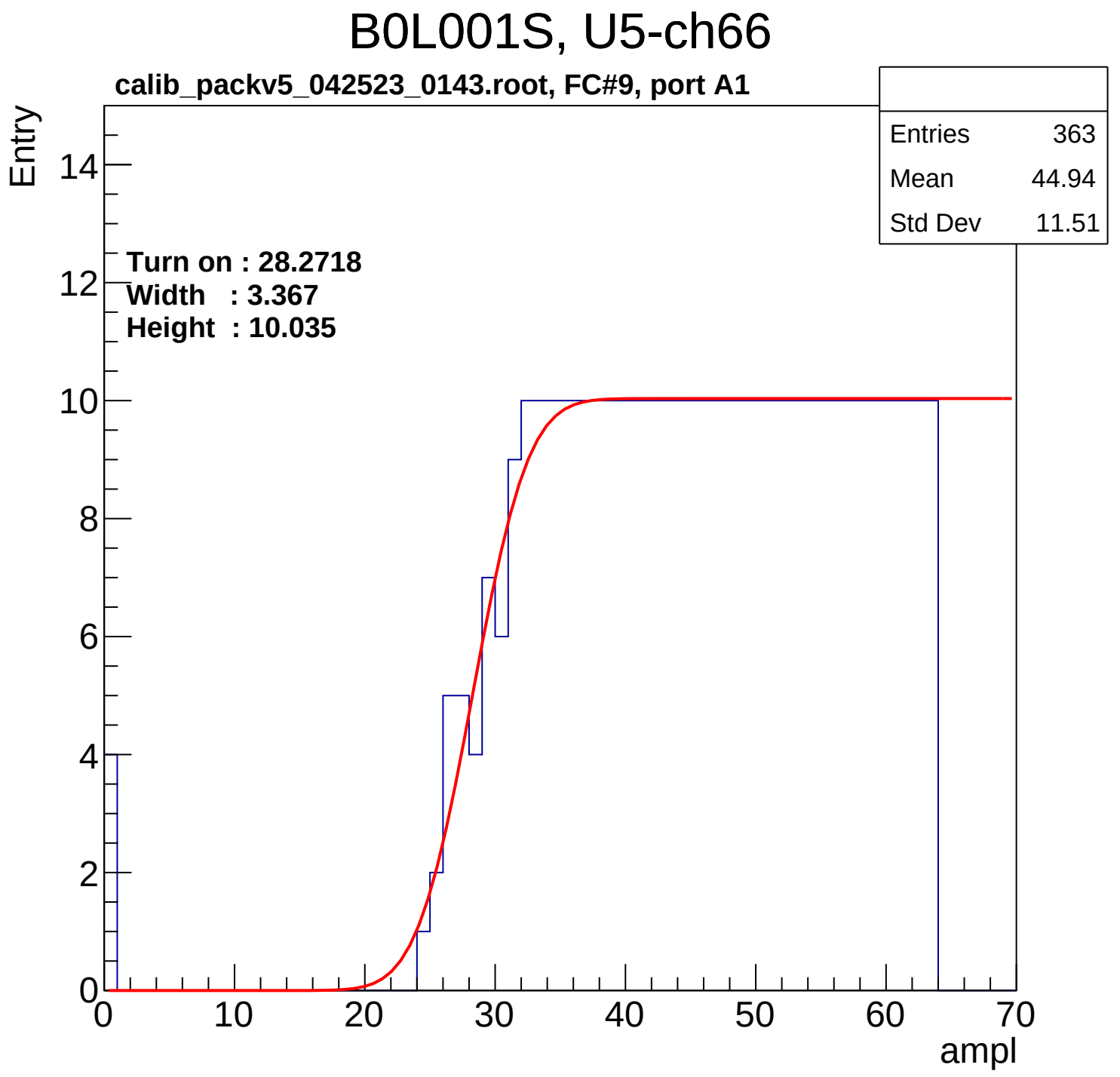
B0L001S, U5-ch66
calib_packv5_042523_0143.root, FC#9, port A1
Entries 363
Mean 44.94
Std Dev 11.51
Turn on : 28.2718
Width : 3.367
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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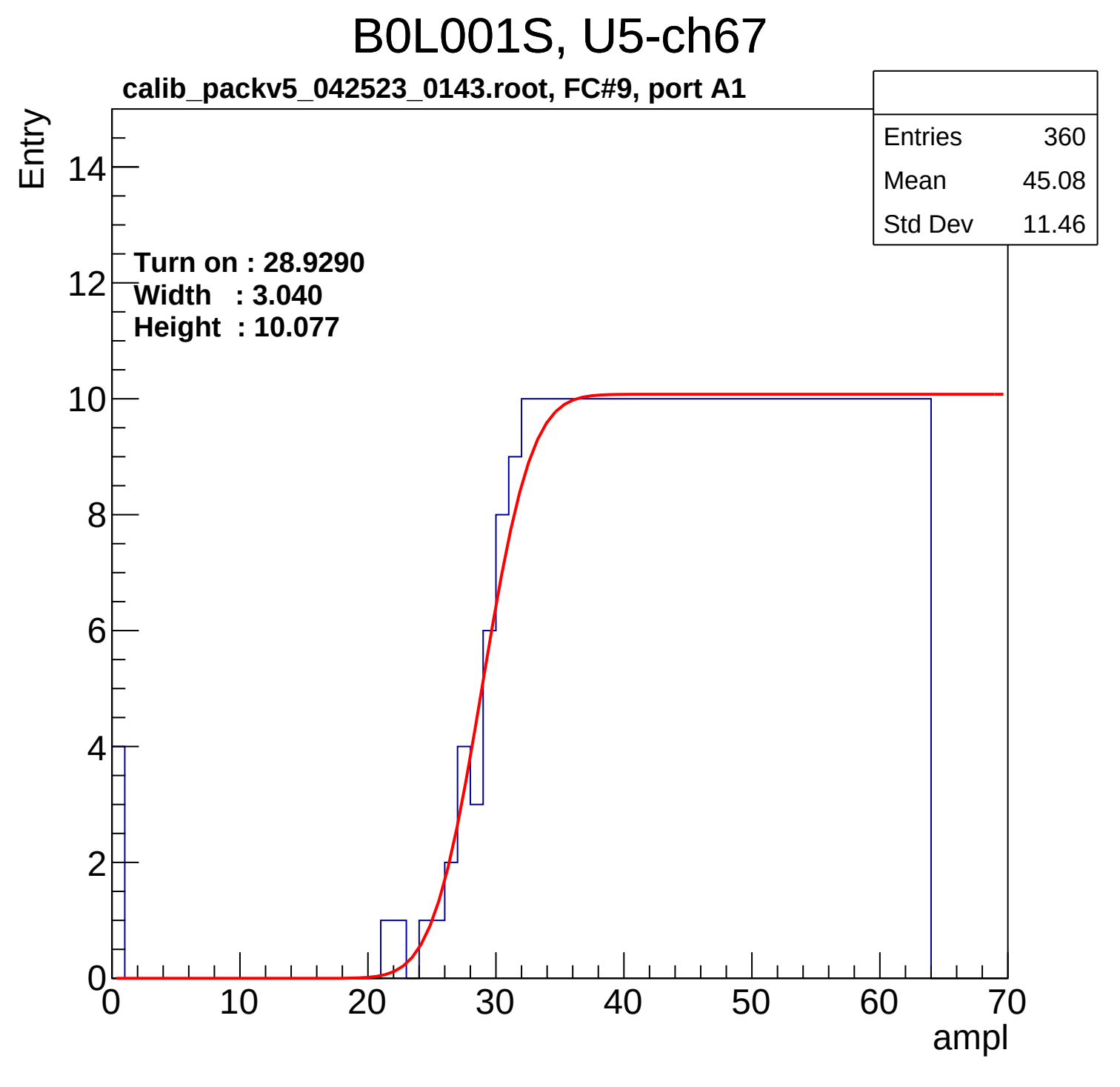
B0L001S, U5-ch67
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.08
Std Dev 11.46
Turn on : 28.9290
Width : 3.040
Height : 10.077
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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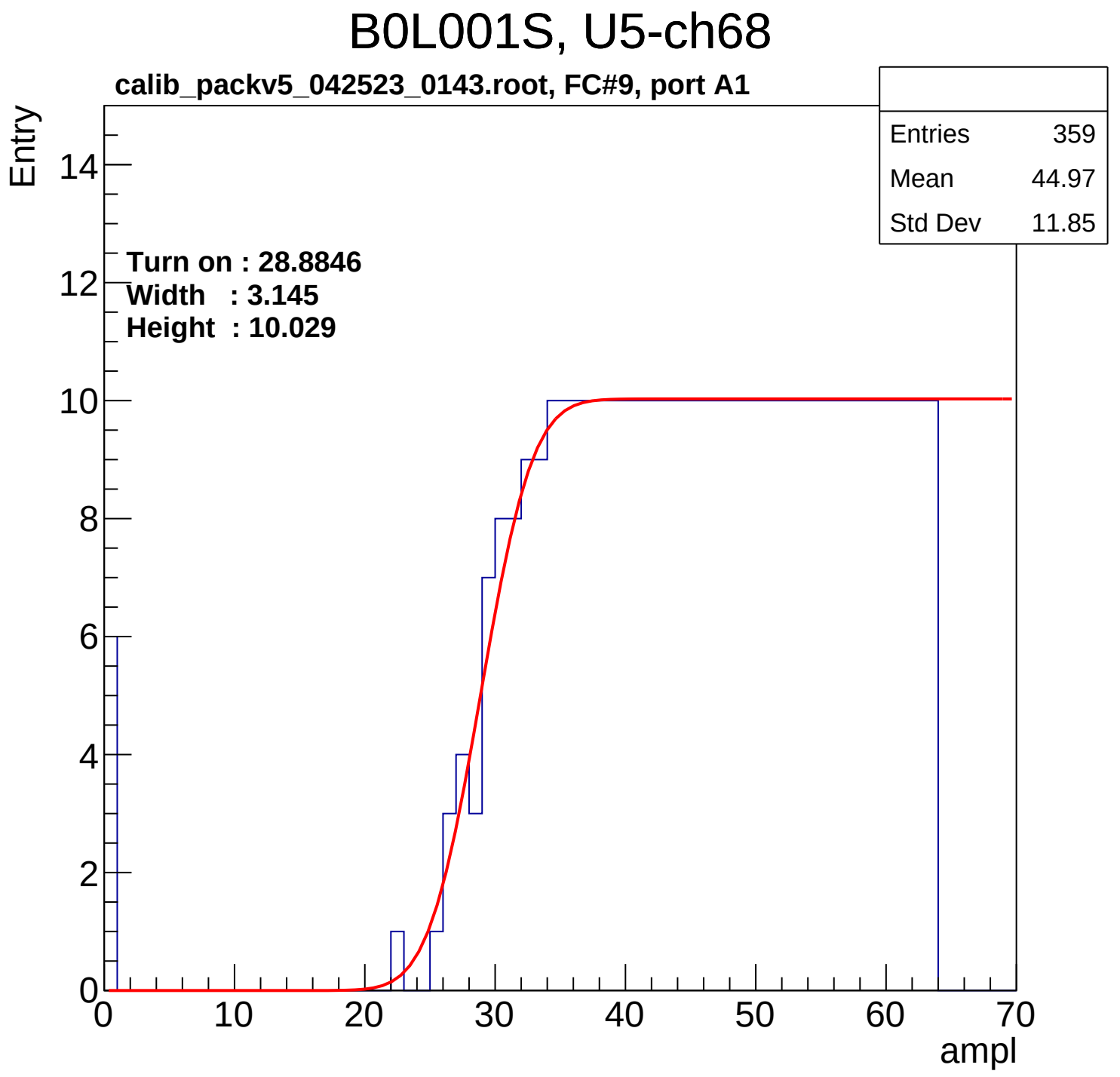
B0L001S, U5-ch68
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 44.97
Std Dev 11.85
Turn on : 28.8846
Width : 3.145
Height : 10.029
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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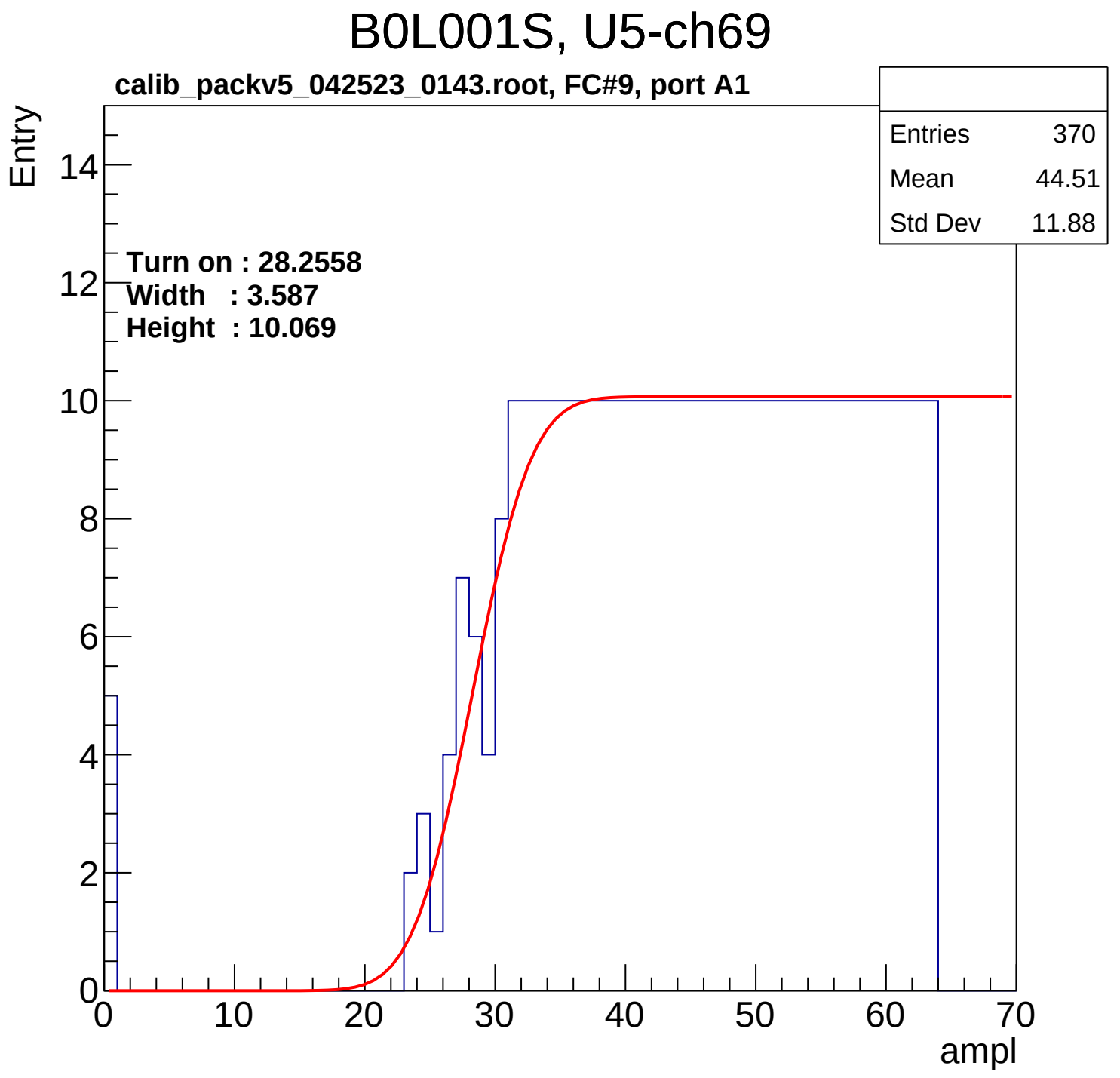
B0L001S, U5-ch69
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.51
Std Dev 11.88
Turn on : 28.2558
Width : 3.587
Height : 10.069
Entry
ampl
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2
4
6
8
10
12
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0
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20
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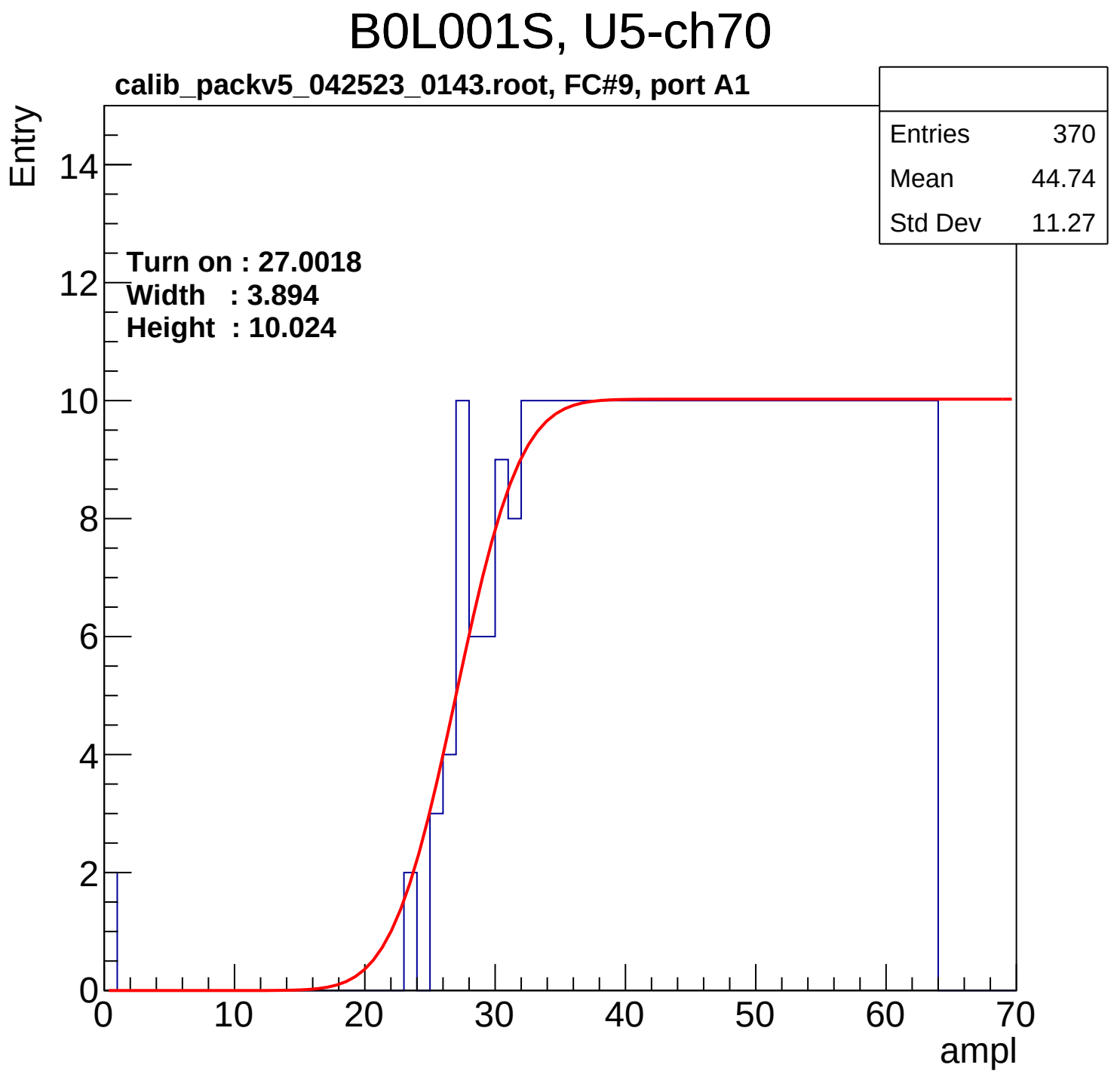
B0L001S, U5-ch70
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.74
Std Dev 11.27
Turn on : 27.0018
Width : 3.894
Height : 10.024
Entry
ampl
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4
6
8
10
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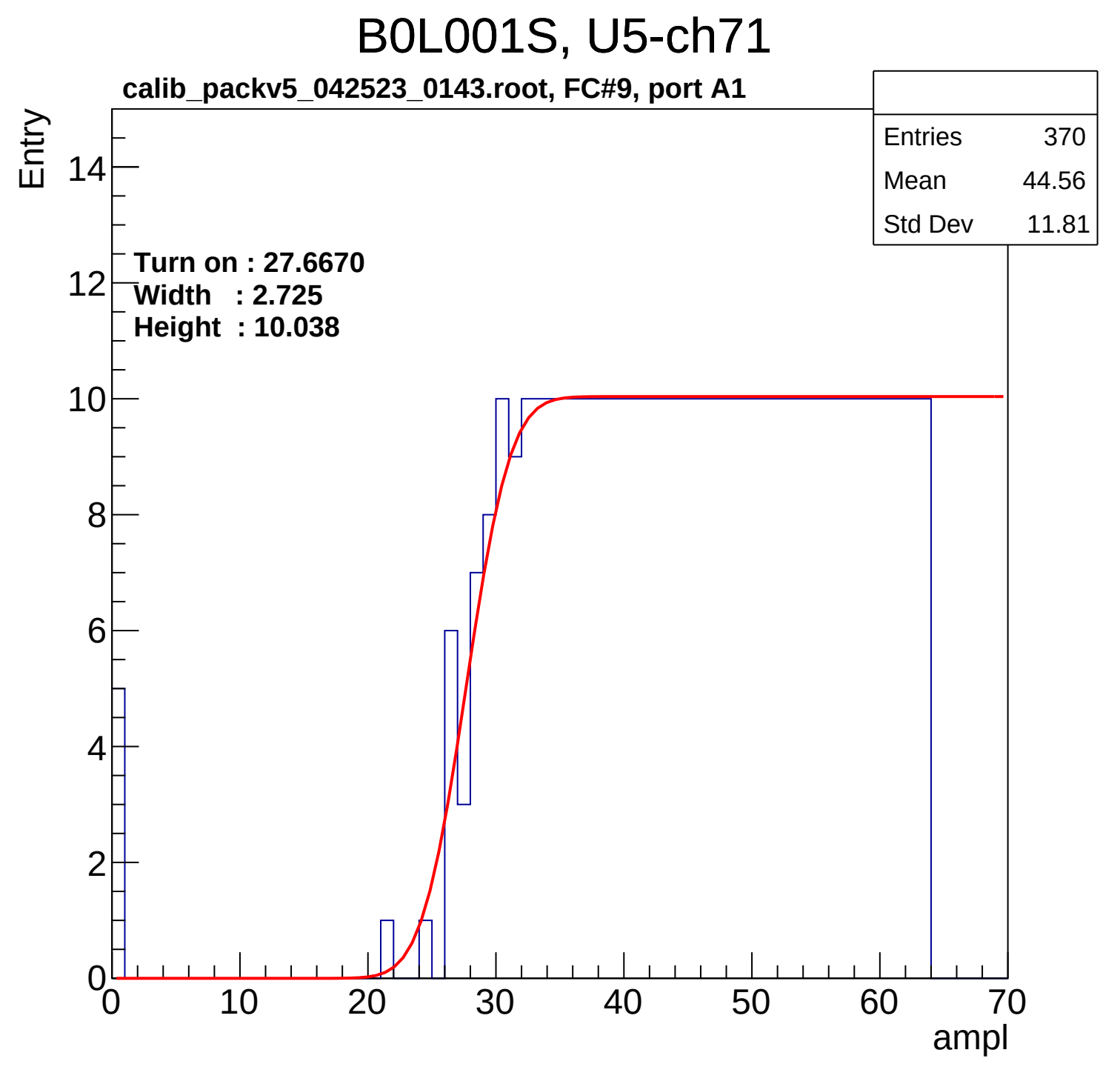
B0L001S, U5-ch71
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.56
Std Dev 11.81
Turn on : 27.6670
Width : 2.725
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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60
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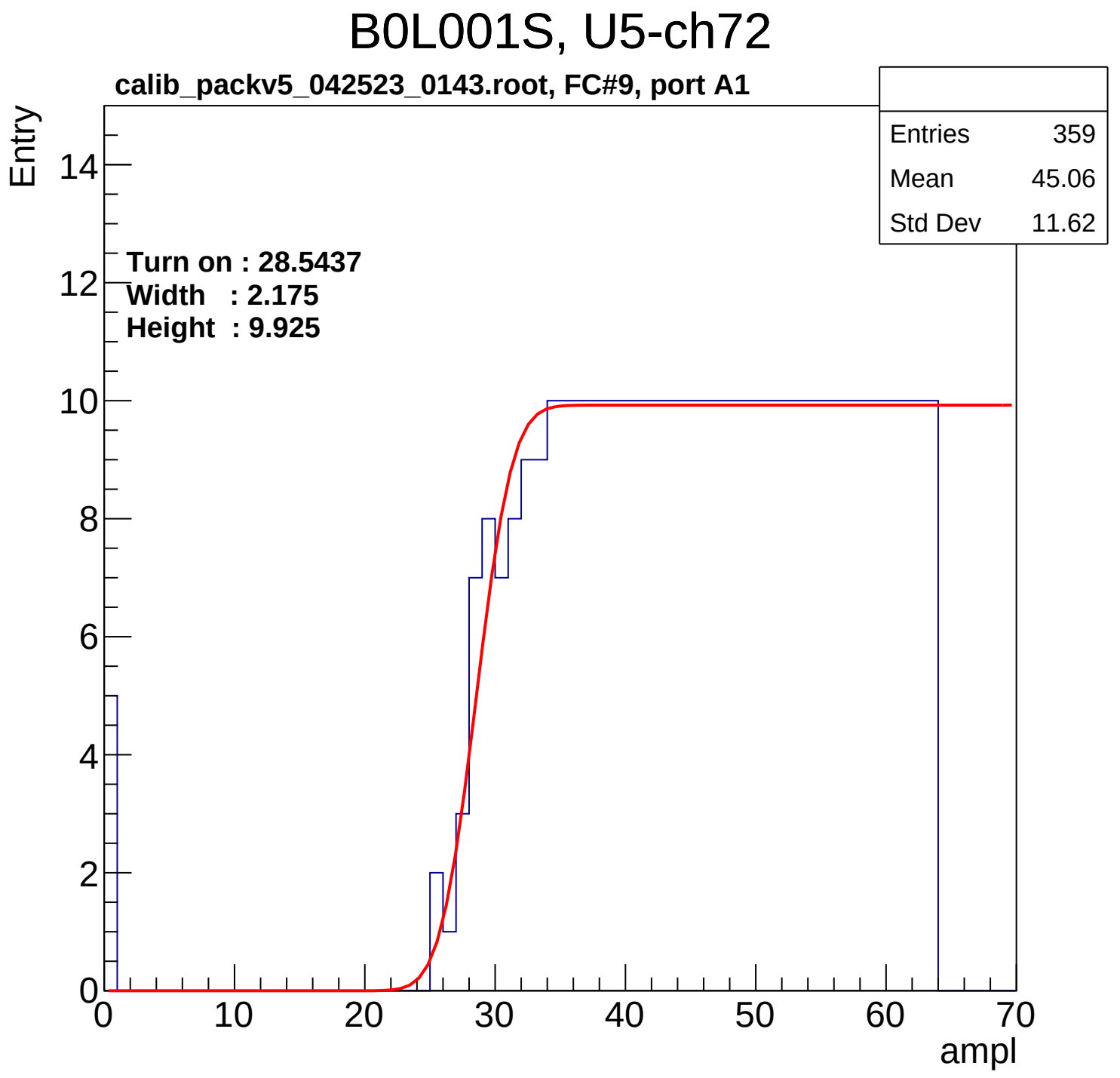
B0L001S, U5-ch72
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.06
Std Dev 11.62
Turn on : 28.5437
Width : 2.175
Height : 9.925
Entry
ampl
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6
8
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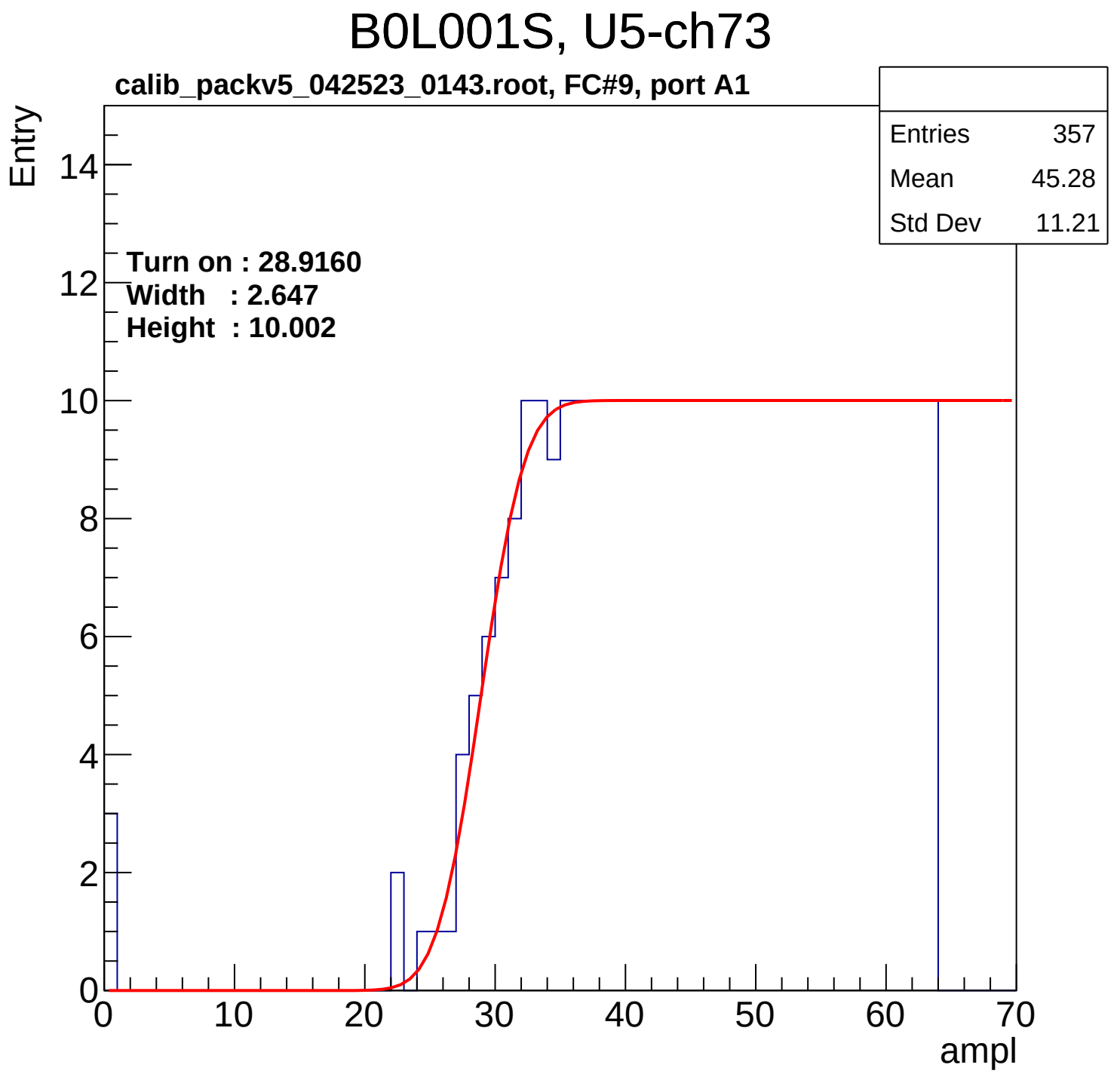
B0L001S, U5-ch73
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 45.28
Std Dev 11.21
Turn on : 28.9160
Width : 2.647
Height : 10.002
Entry
ampl
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8
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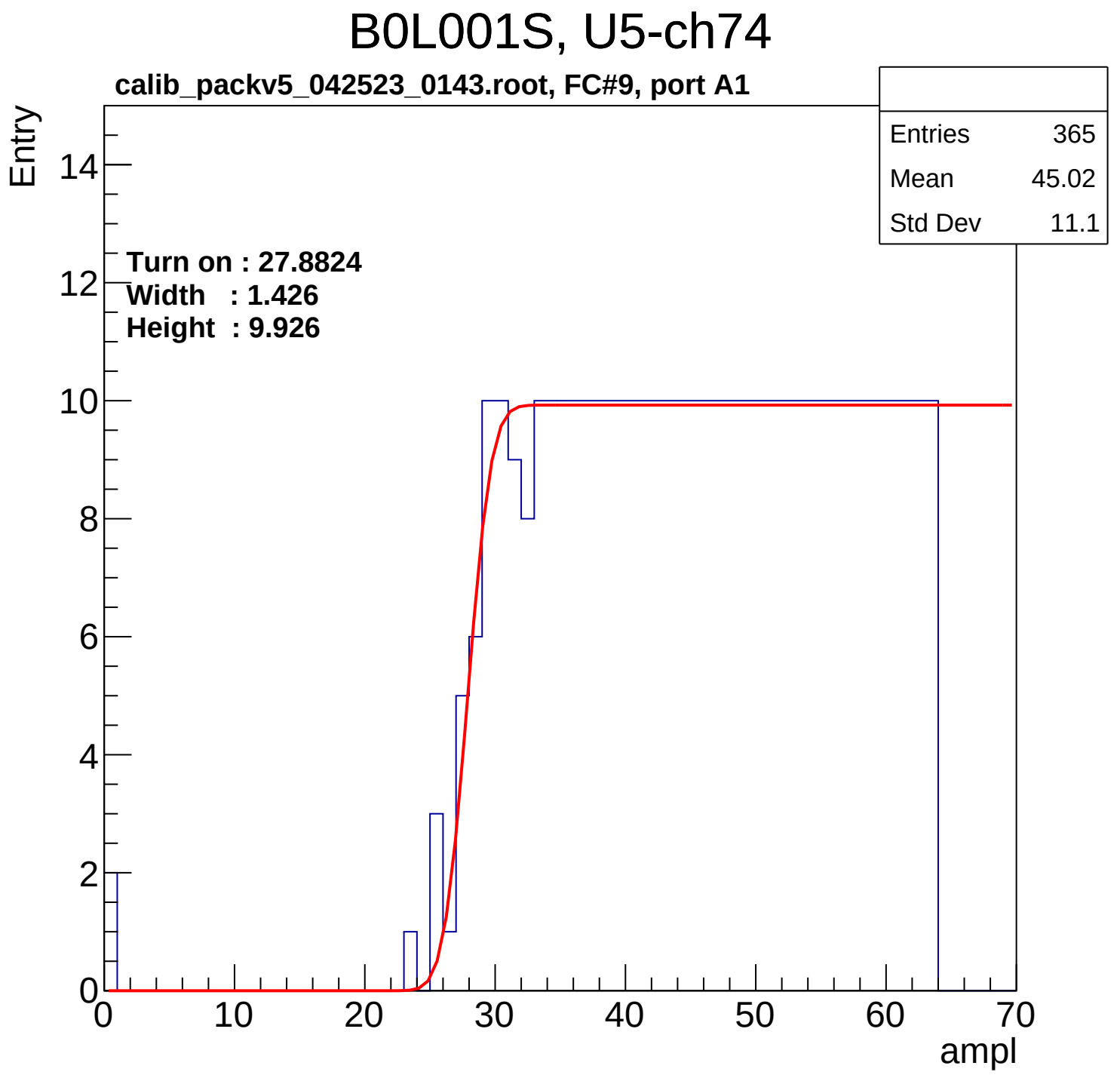
B0L001S, U5-ch74
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 45.02
Std Dev 11.1
Turn on : 27.8824
Width : 1.426
Height : 9.926
Entry
ampl
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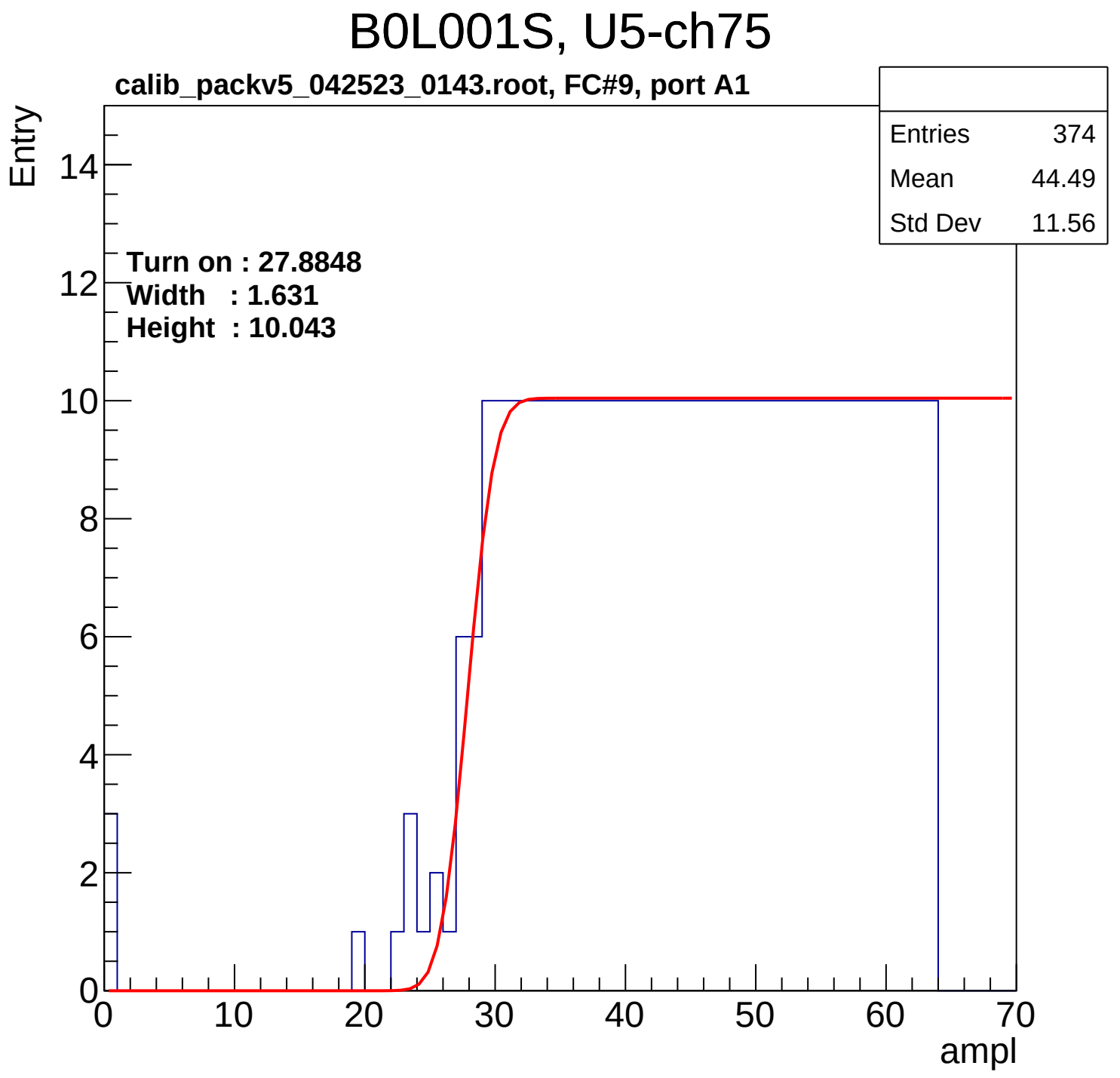
B0L001S, U5-ch75
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.49
Std Dev 11.56
Turn on : 27.8848
Width : 1.631
Height : 10.043
Entry
ampl
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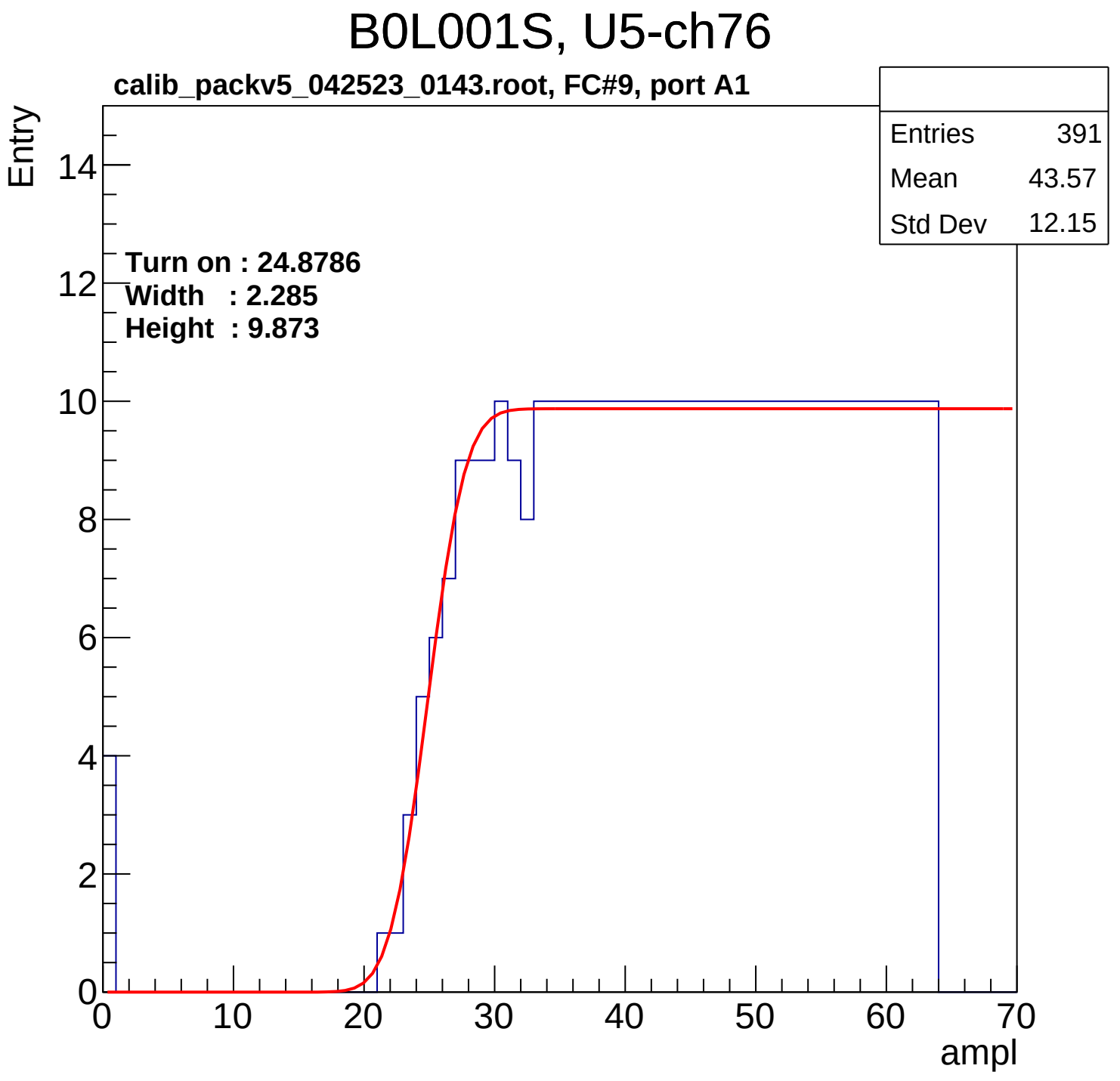
B0L001S, U5-ch76
calib_packv5_042523_0143.root, FC#9, port A1
Entries 391
Mean 43.57
Std Dev 12.15
Turn on : 24.8786
Width : 2.285
Height : 9.873
Entry
ampl
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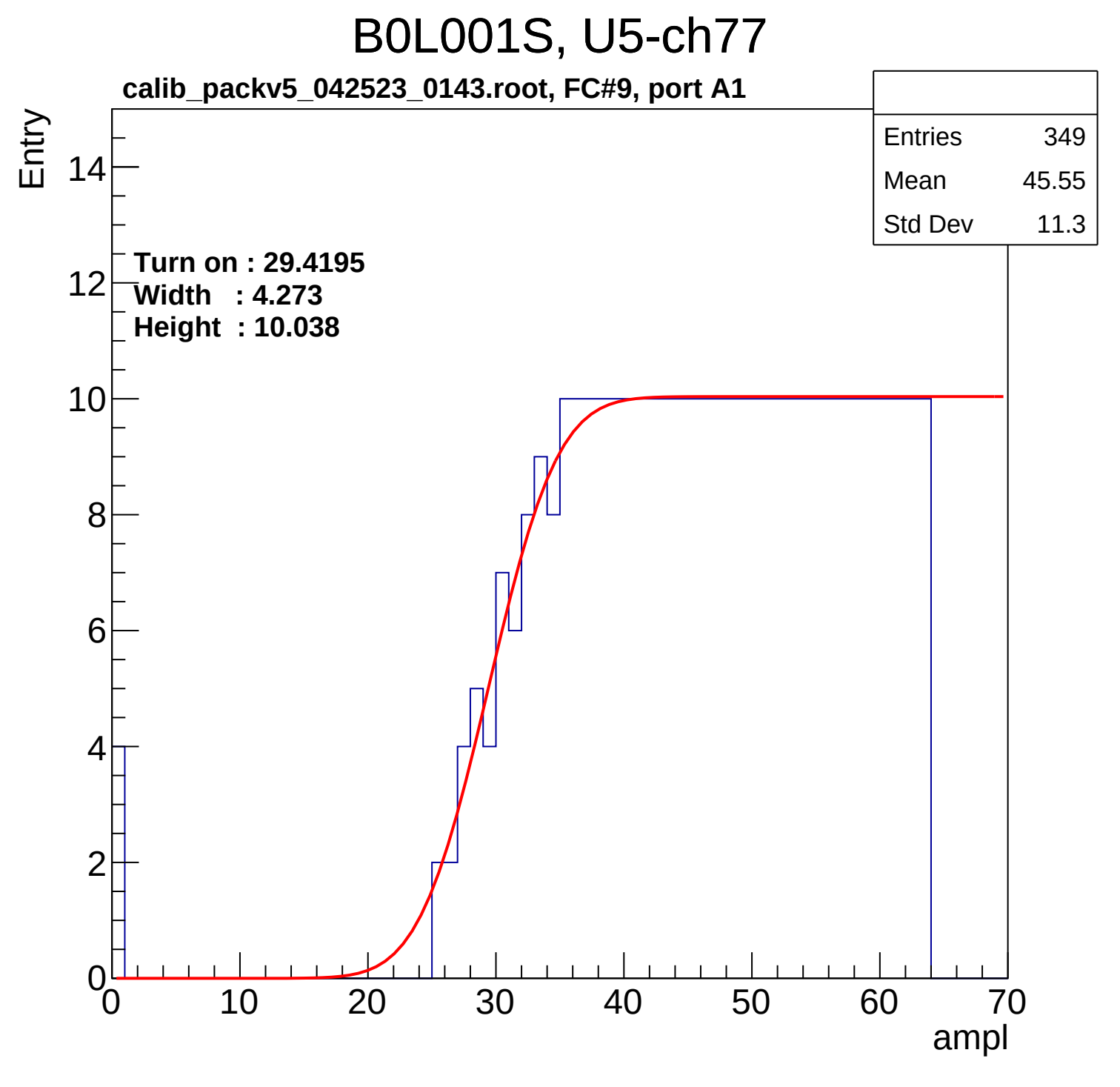
B0L001S, U5-ch77
calib_packv5_042523_0143.root, FC#9, port A1
Entries 349
Mean 45.55
Std Dev 11.3
Turn on : 29.4195
Width : 4.273
Height : 10.038
Entry
ampl
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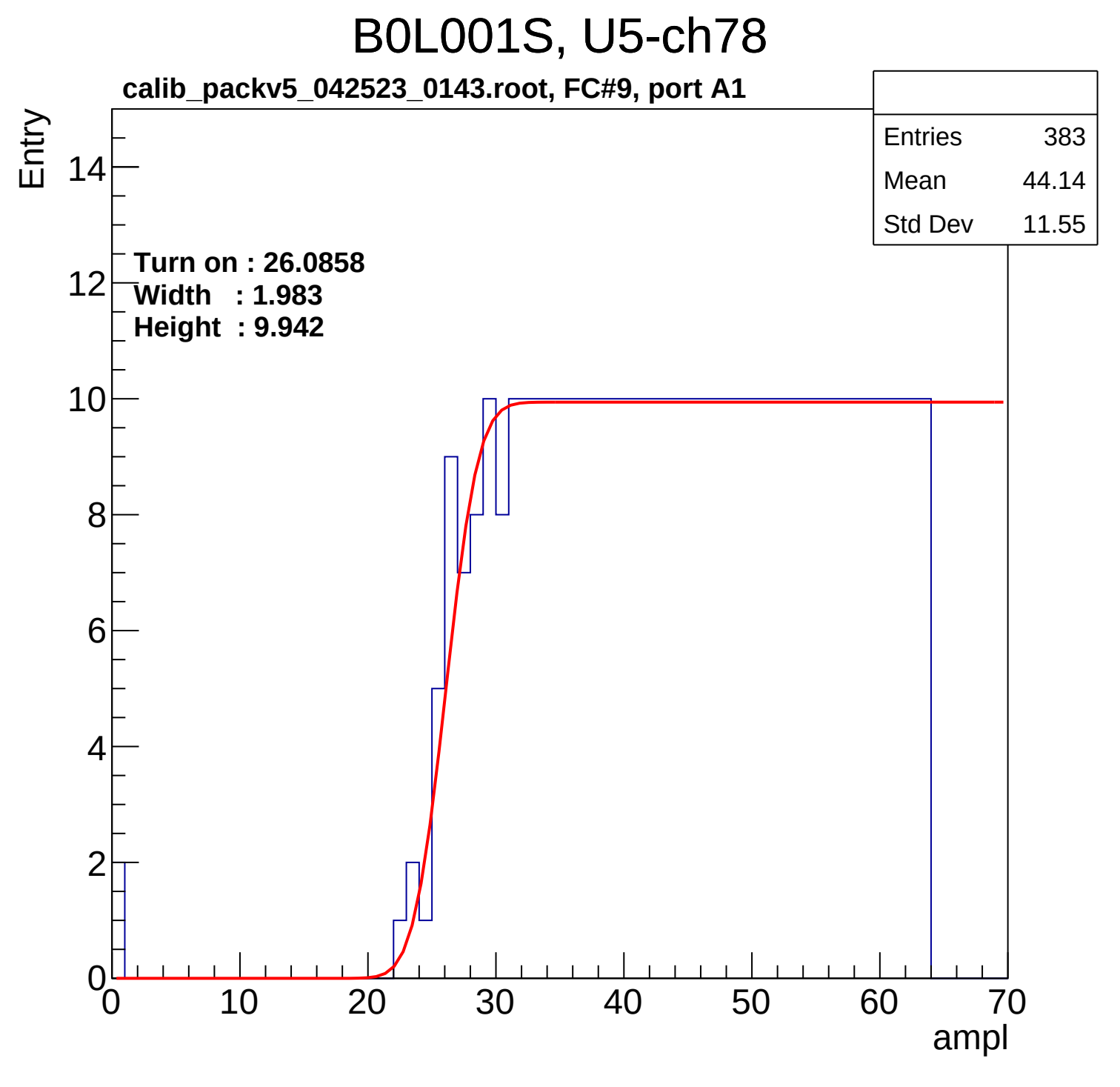
B0L001S, U5-ch78
calib_packv5_042523_0143.root, FC#9, port A1
Entries 383
Mean 44.14
Std Dev 11.55
Turn on : 26.0858
Width : 1.983
Height : 9.942
Entry
ampl
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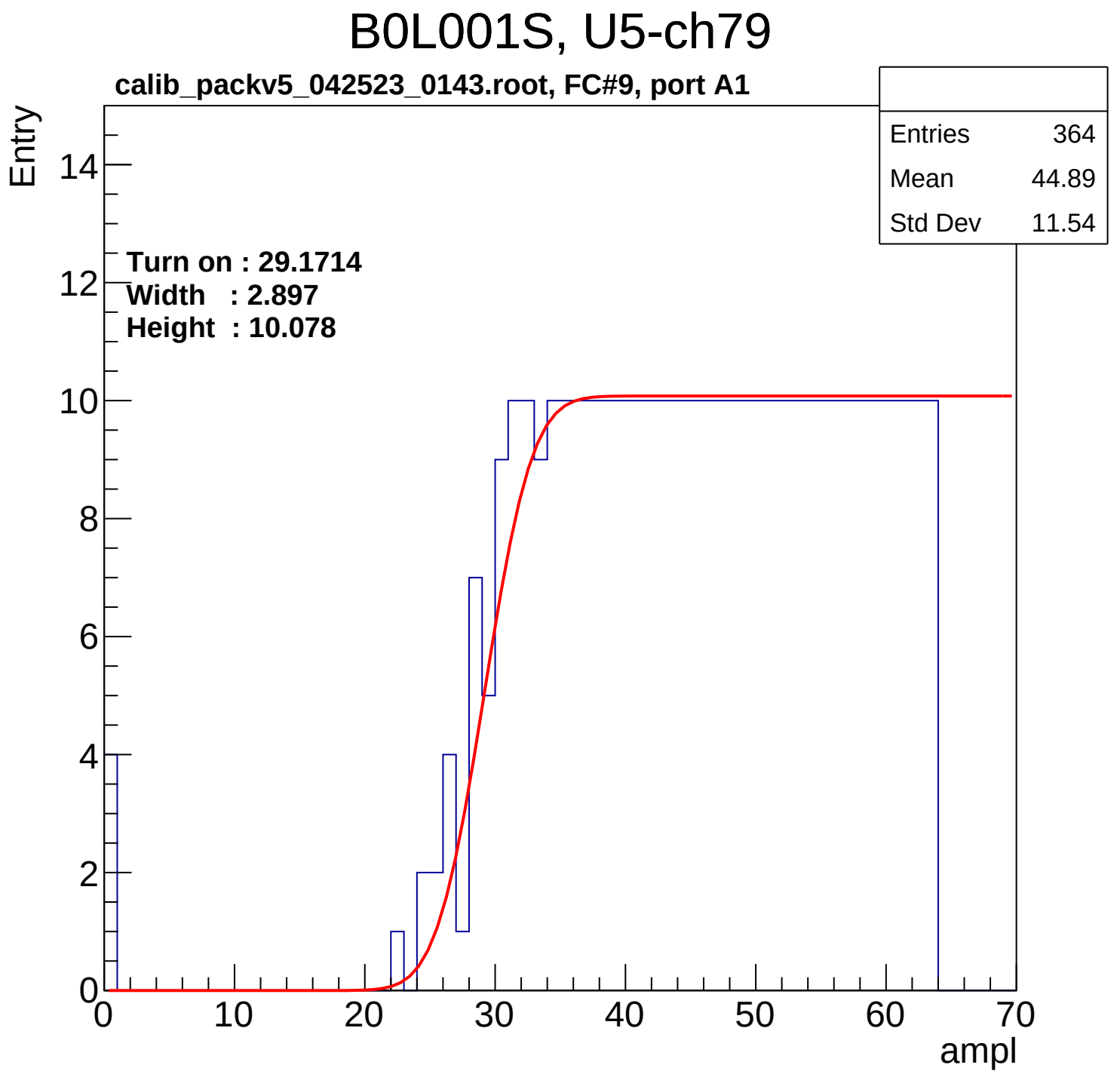
B0L001S, U5-ch79
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.89
Std Dev 11.54
Turn on : 29.1714
Width : 2.897
Height : 10.078
Entry
ampl
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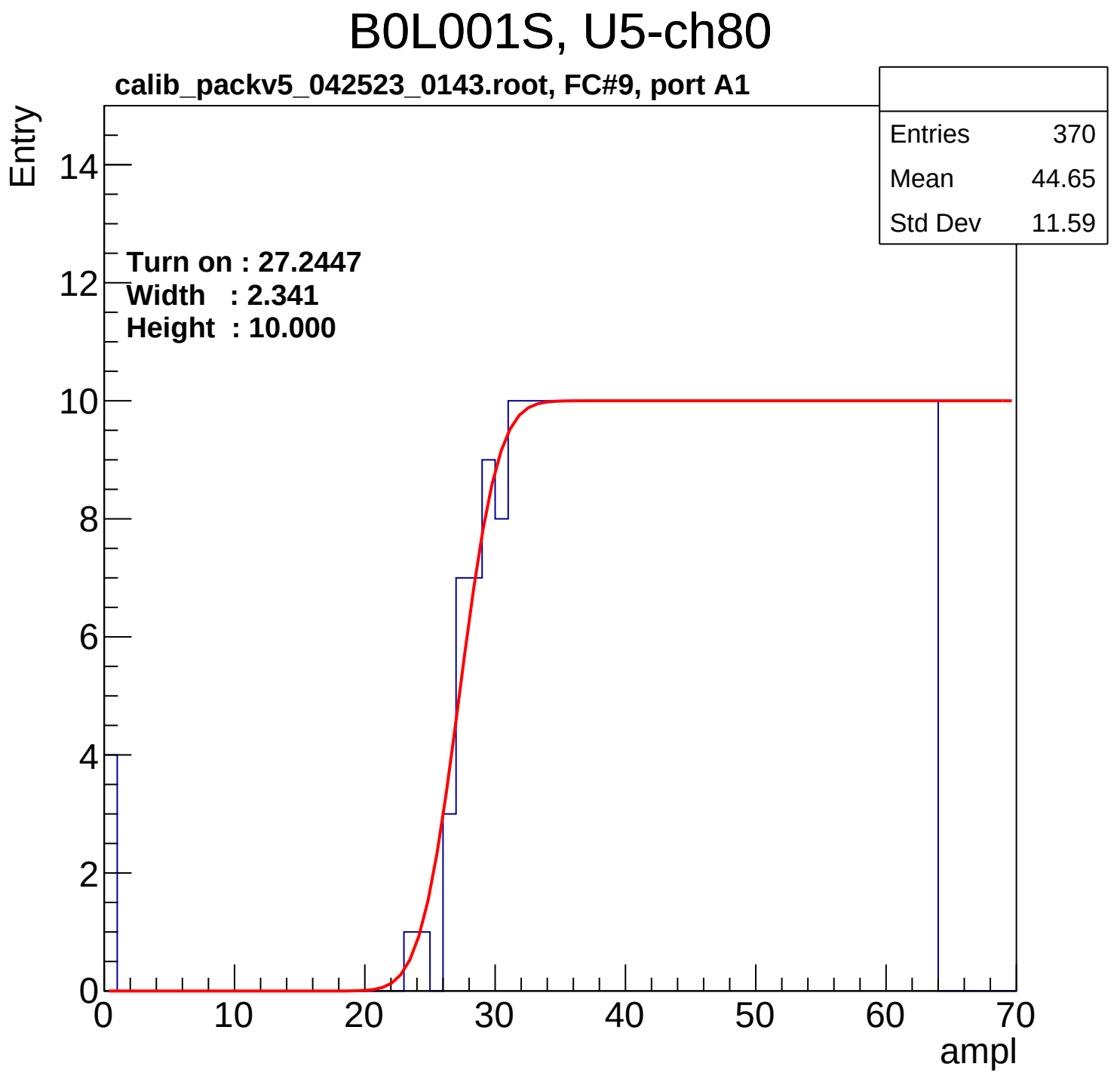
B0L001S, U5-ch80
calib_packv5_042523_0143.root, FC#9, port A1
Entries 370
Mean 44.65
Std Dev 11.59
Turn on : 27.2447
Width : 2.341
Height : 10.000
Entry
ampl
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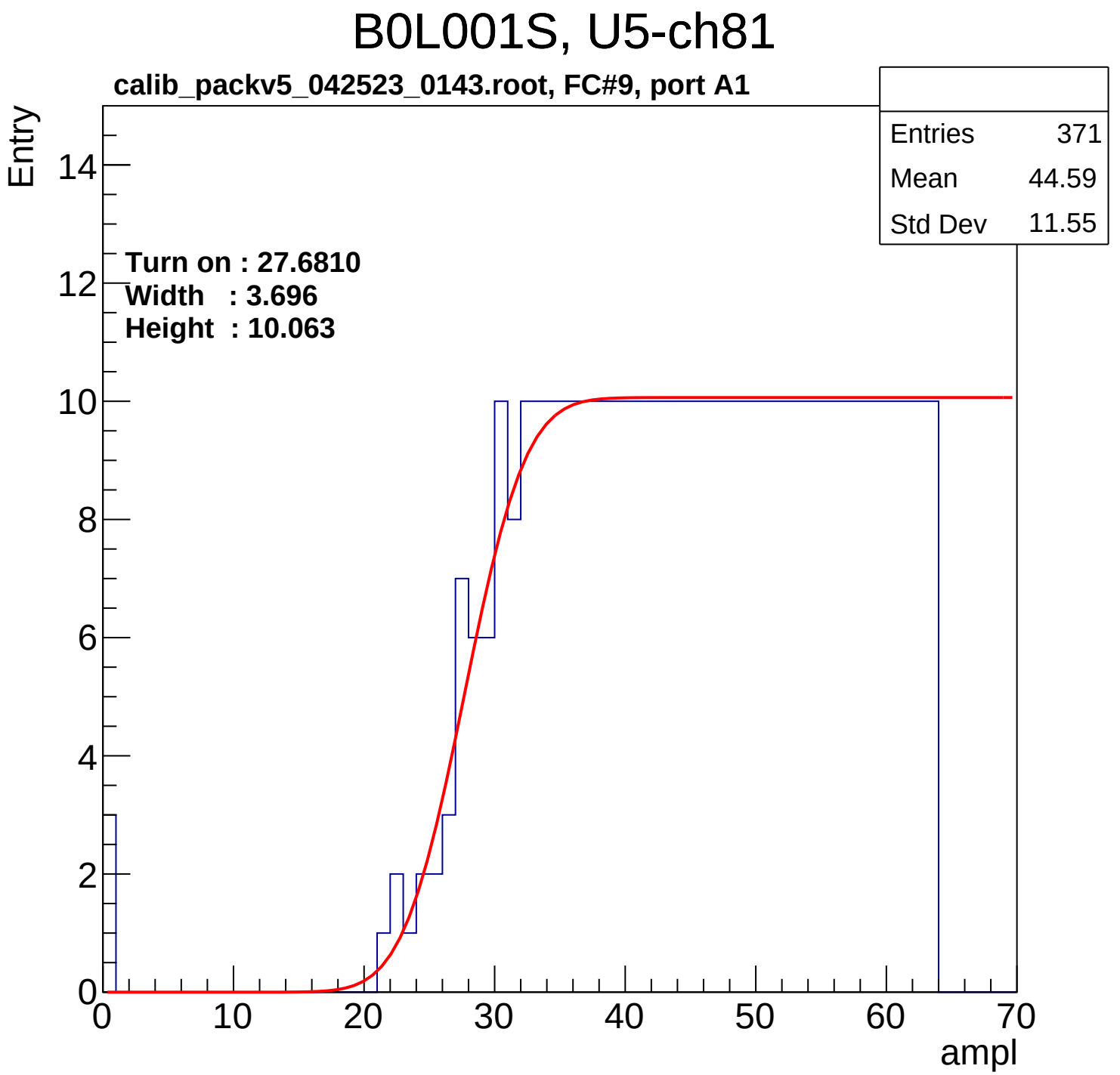
B0L001S, U5-ch81
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.59
Std Dev 11.55
Turn on : 27.6810
Width : 3.696
Height : 10.063
Entry
ampl
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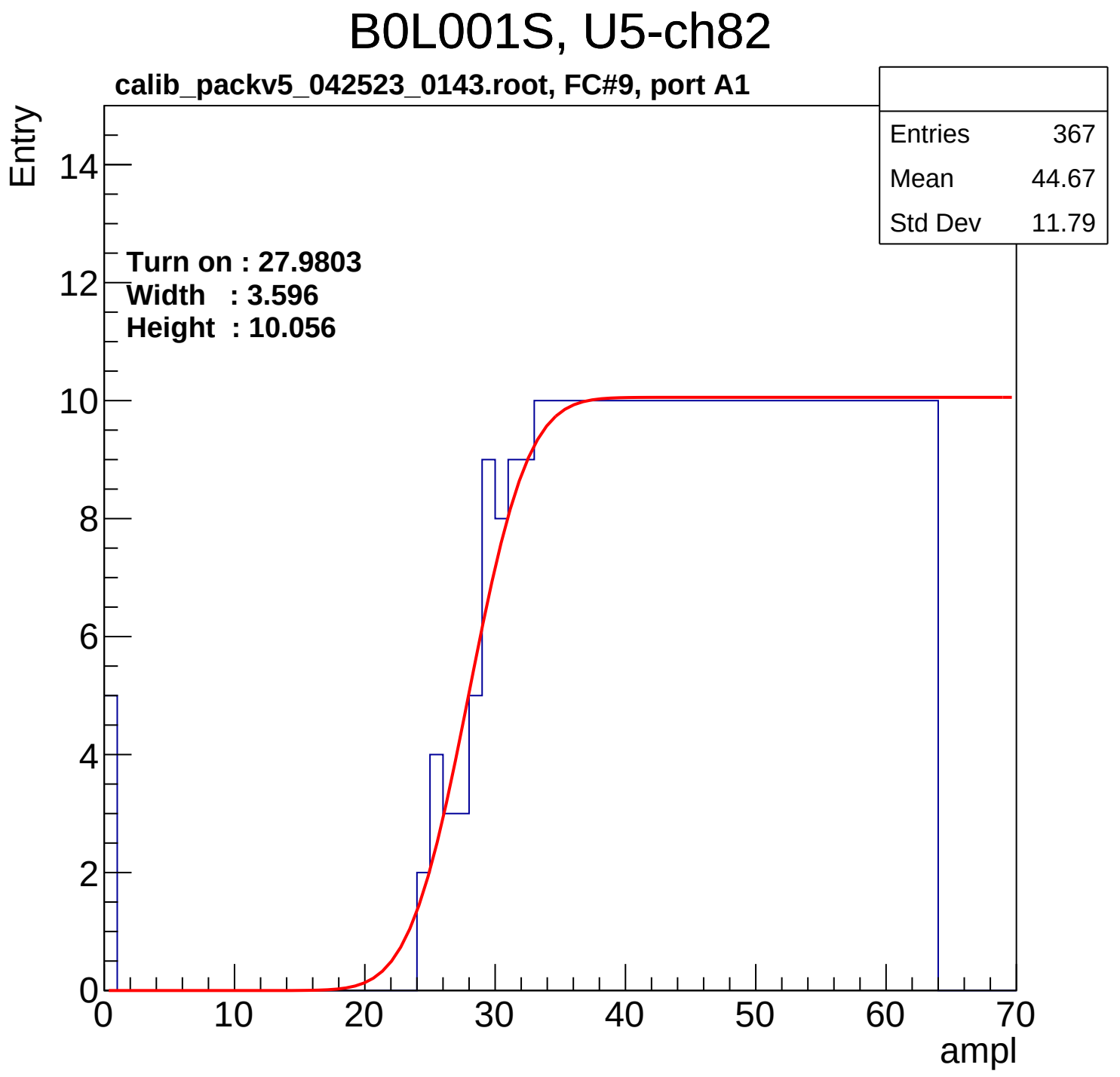
B0L001S, U5-ch82
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.67
Std Dev 11.79
Turn on : 27.9803
Width : 3.596
Height : 10.056
Entry
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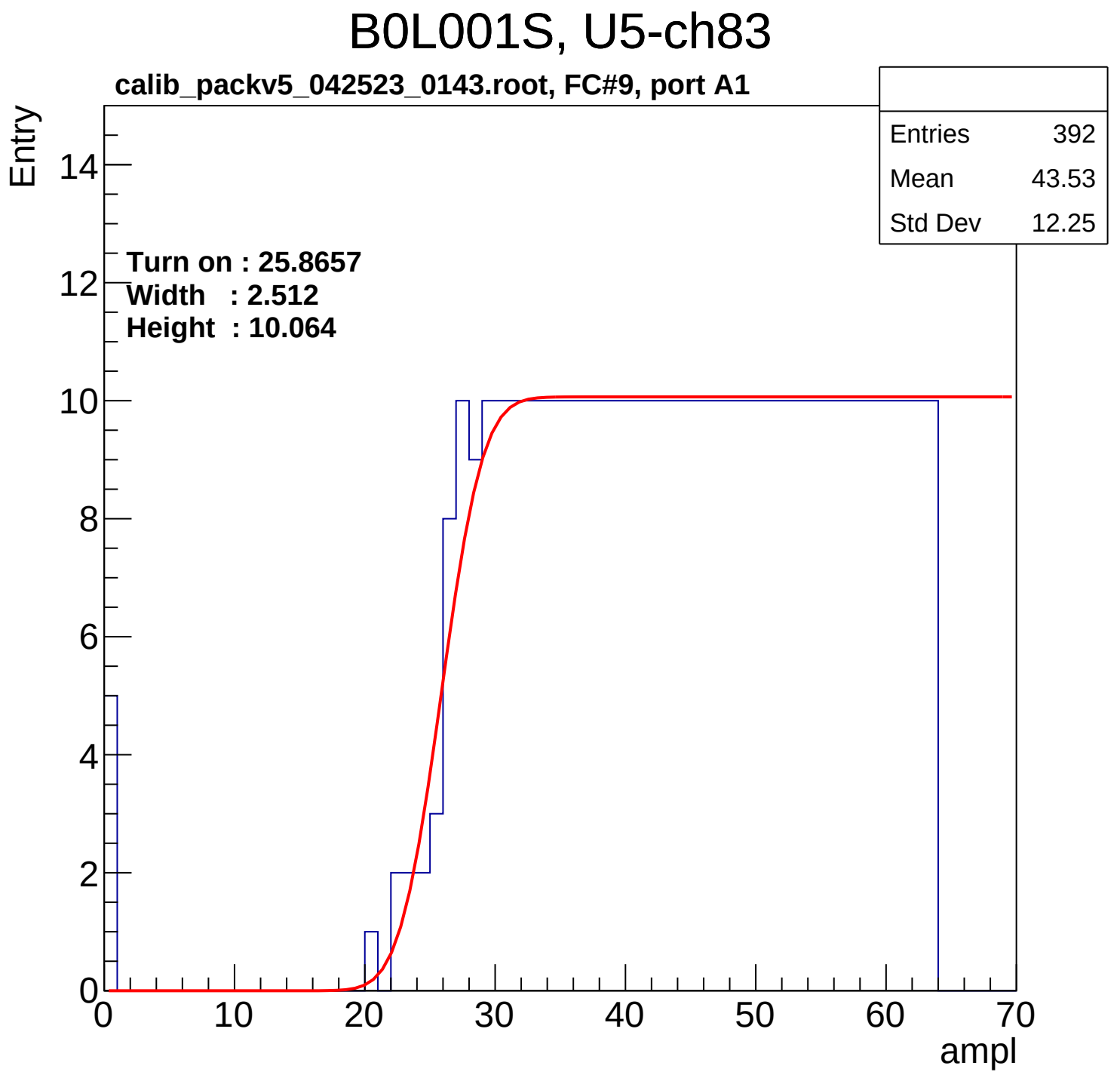
B0L001S, U5-ch83
calib_packv5_042523_0143.root, FC#9, port A1
Entries 392
Mean 43.53
Std Dev 12.25
Turn on : 25.8657
Width : 2.512
Height : 10.064
Entry
ampl
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8
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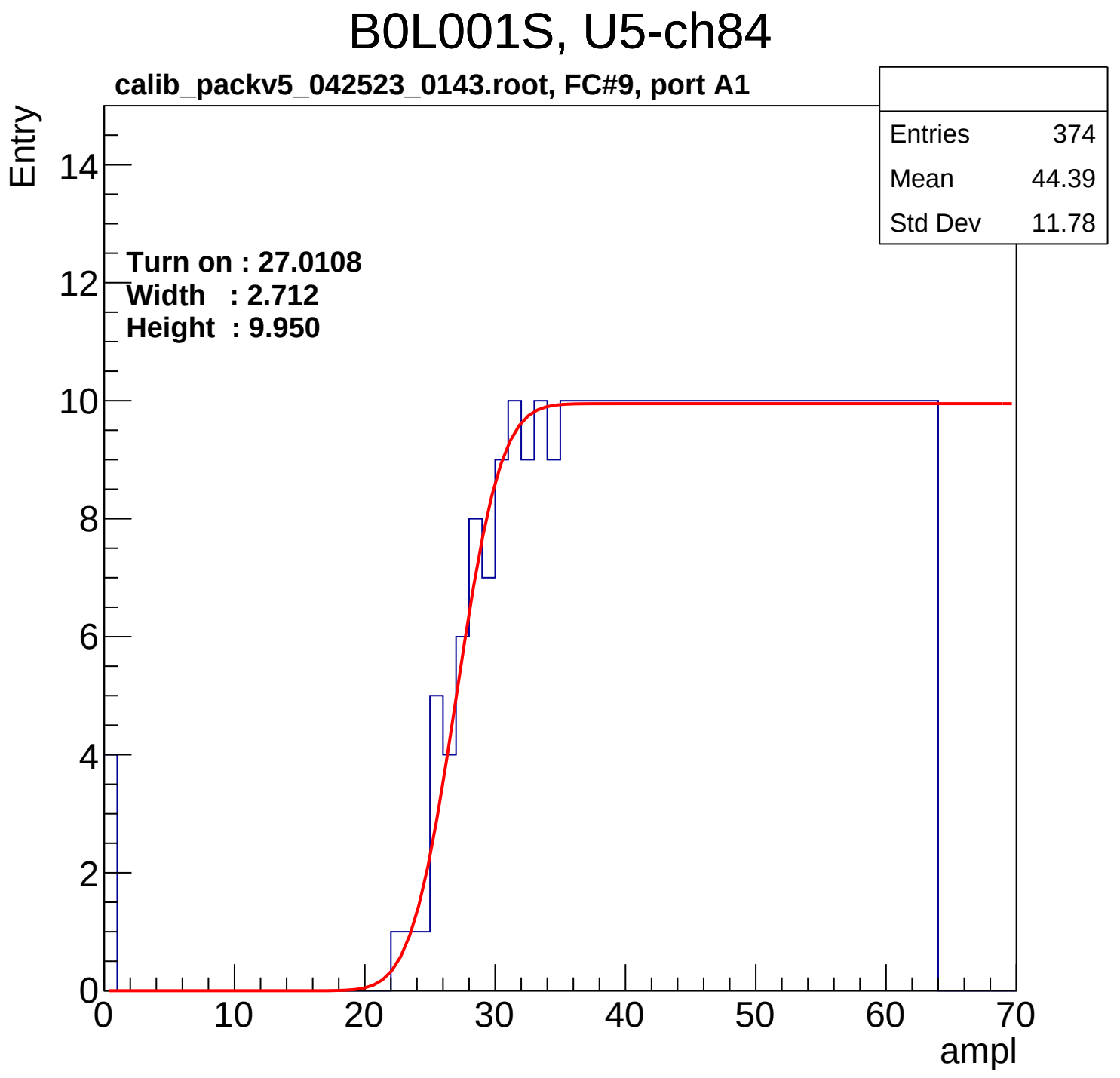
B0L001S, U5-ch84
calib_packv5_042523_0143.root, FC#9, port A1
Entries 374
Mean 44.39
Std Dev 11.78
Turn on : 27.0108
Width : 2.712
Height : 9.950
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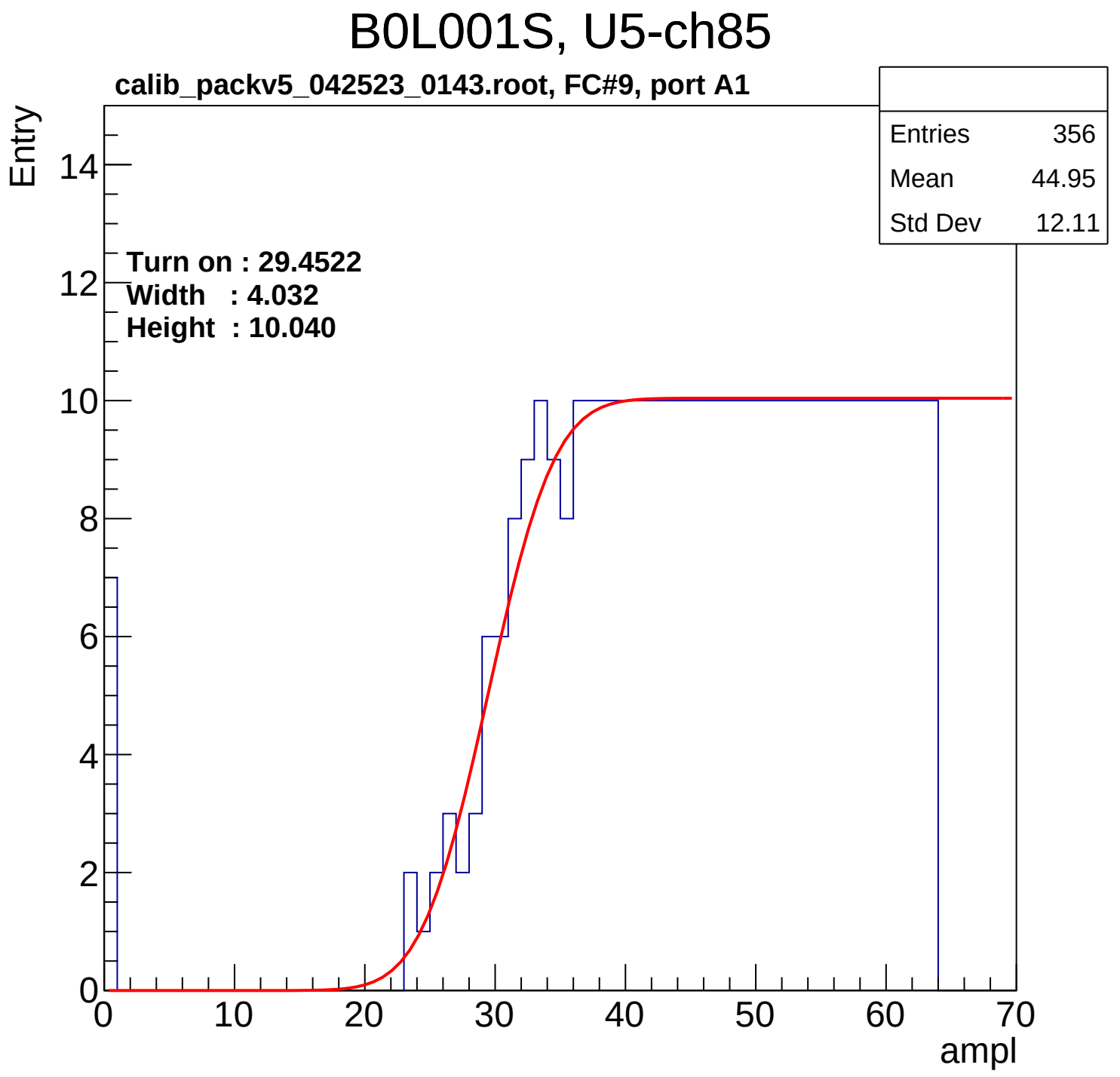
B0L001S, U5-ch85
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 44.95
Std Dev 12.11
Turn on : 29.4522
Width : 4.032
Height : 10.040
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ampl
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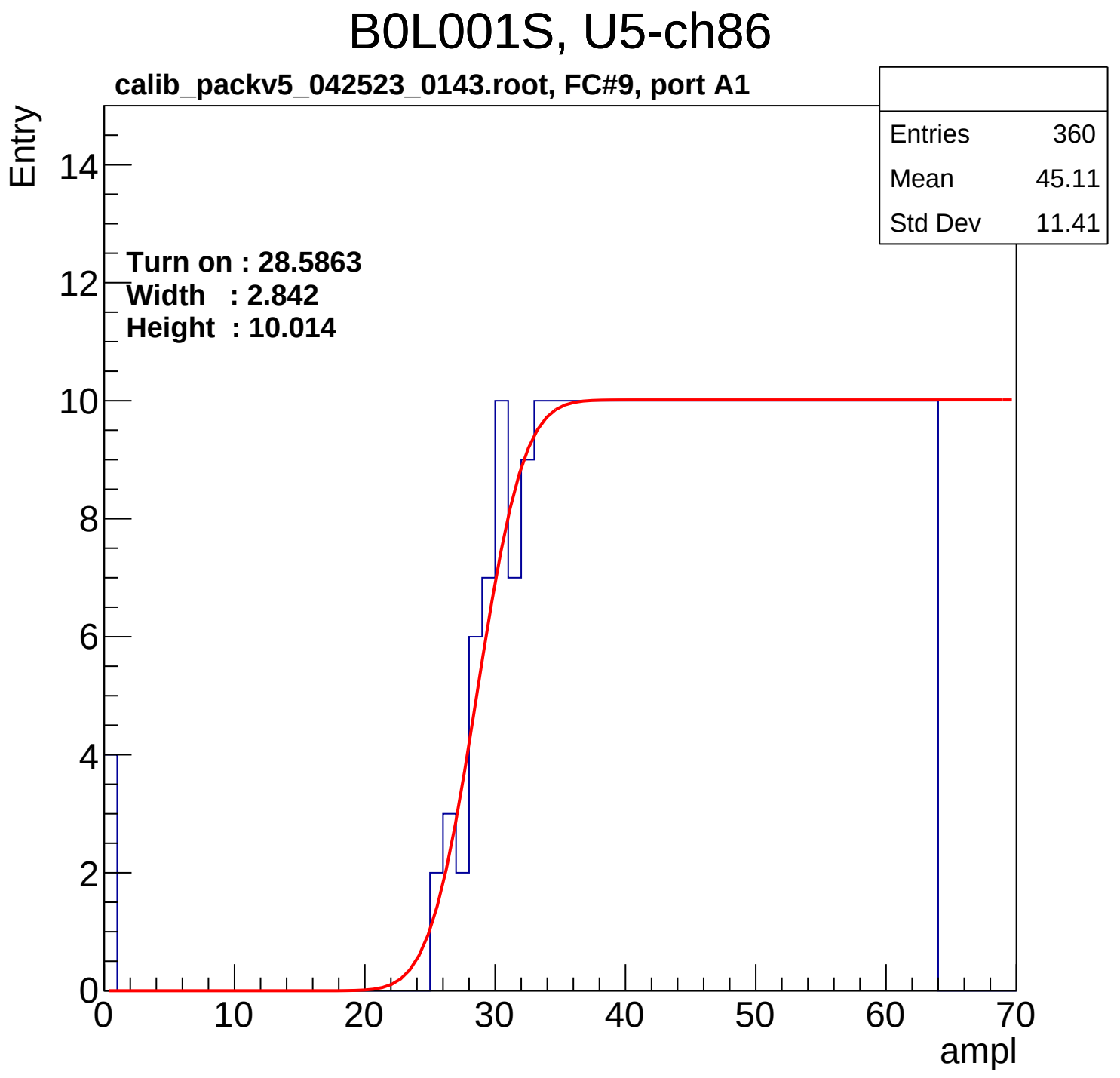
B0L001S, U5-ch86
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.11
Std Dev 11.41
Turn on : 28.5863
Width : 2.842
Height : 10.014
Entry
ampl
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4
6
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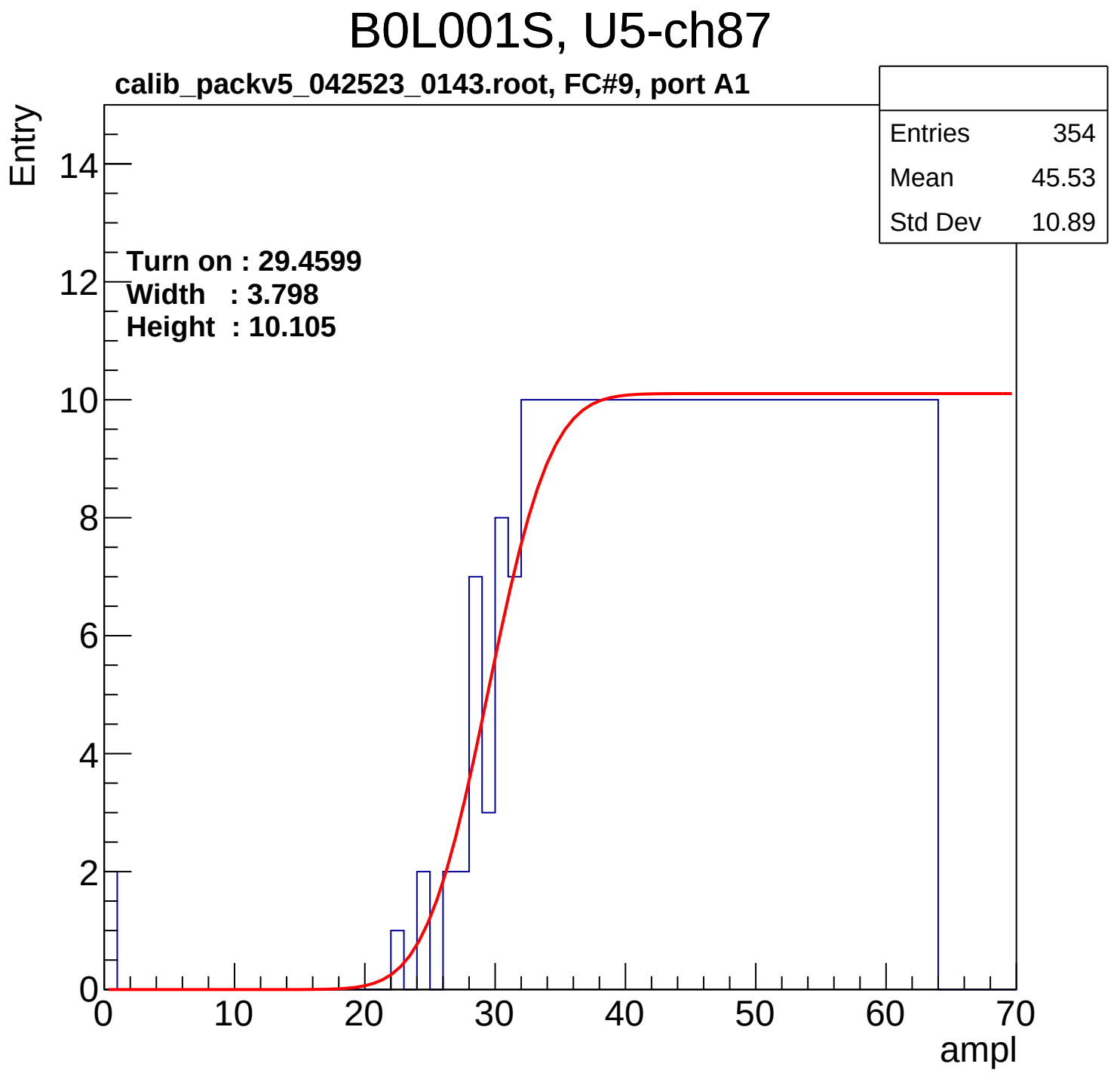
B0L001S, U5-ch87
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.53
Std Dev 10.89
Turn on : 29.4599
Width : 3.798
Height : 10.105
Entry
ampl
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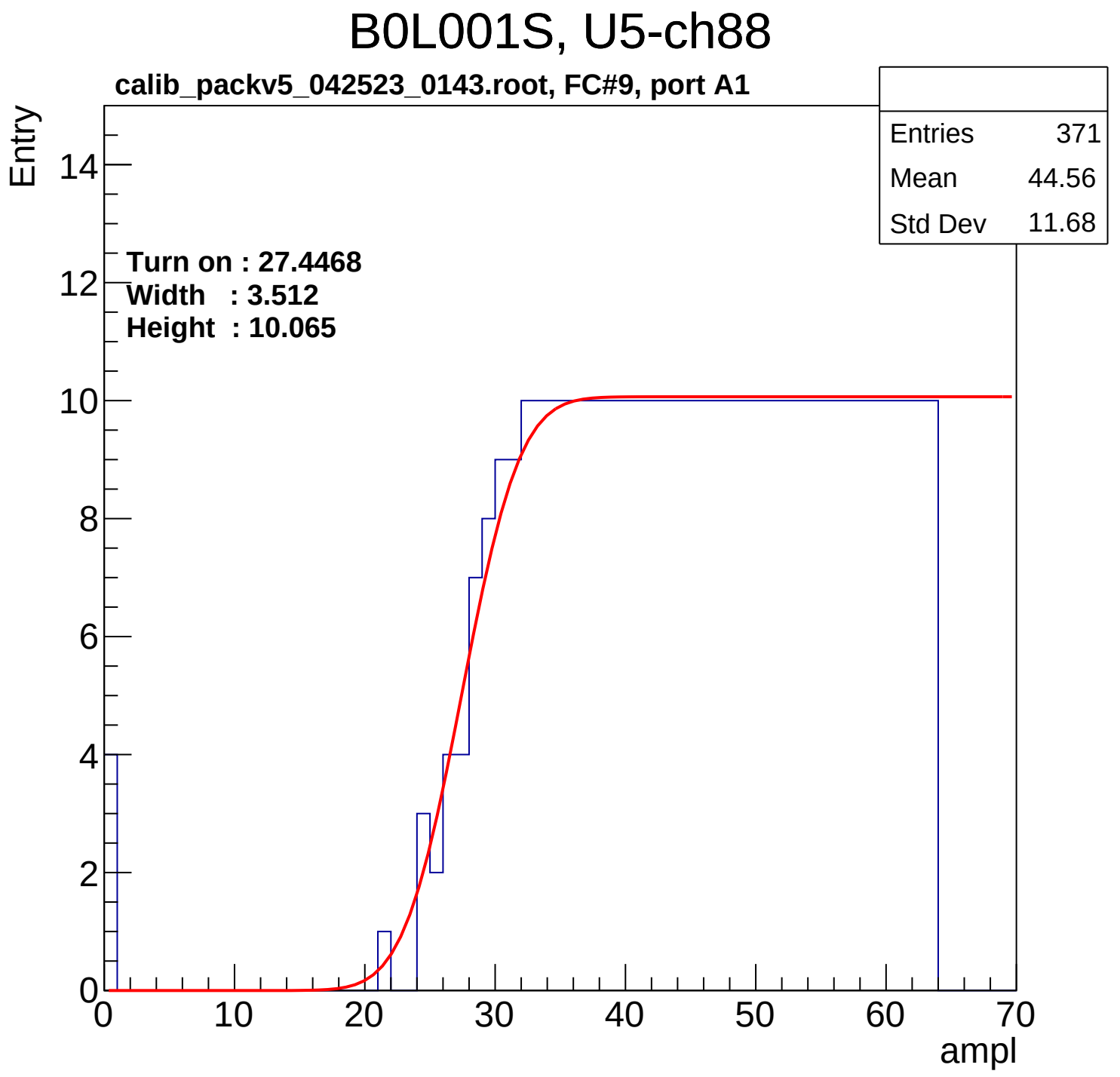
B0L001S, U5-ch88
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.56
Std Dev 11.68
Turn on : 27.4468
Width : 3.512
Height : 10.065
Entry
ampl
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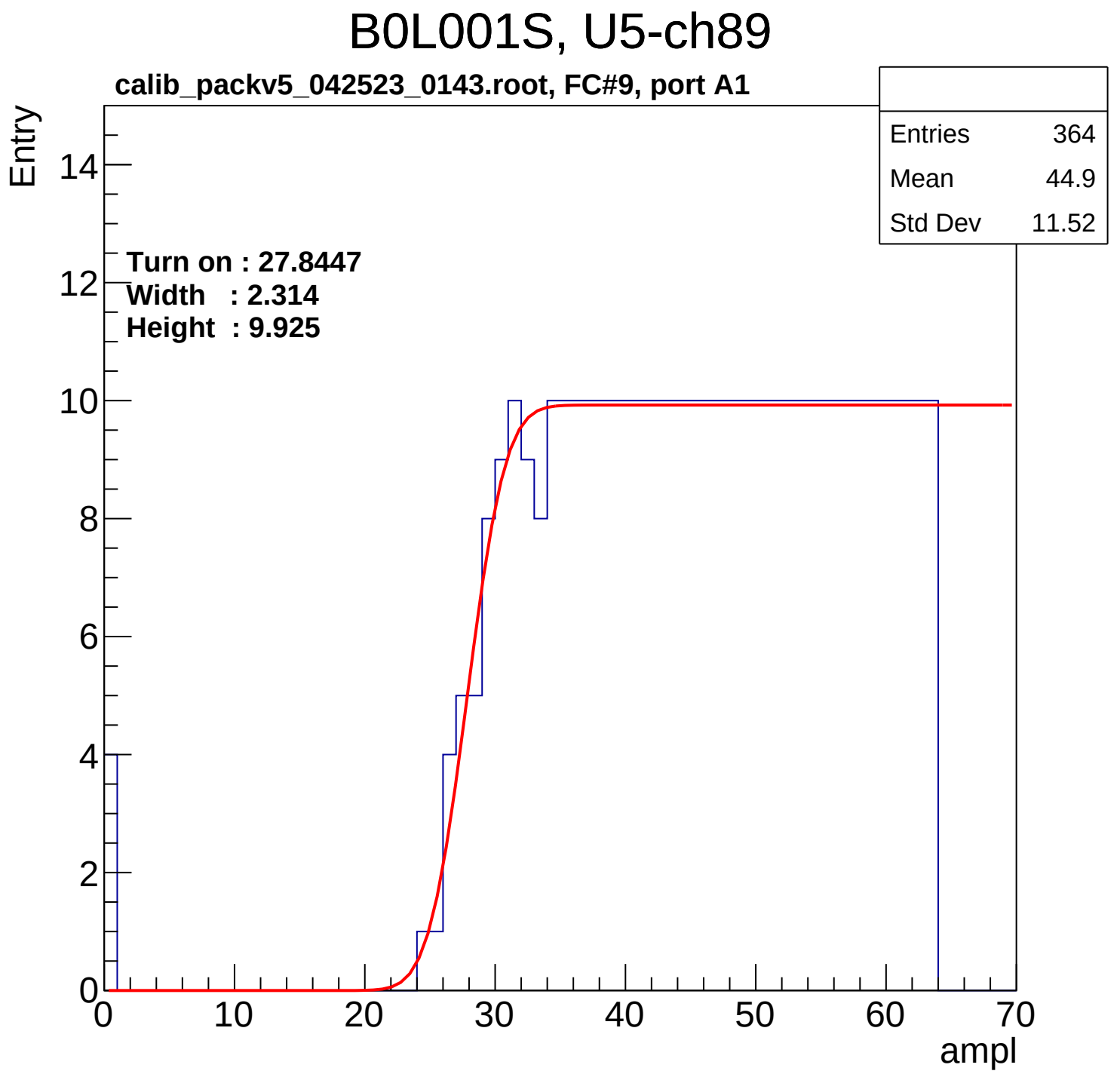
B0L001S, U5-ch89
calib_packv5_042523_0143.root, FC#9, port A1
Entries 364
Mean 44.9
Std Dev 11.52
Turn on : 27.8447
Width : 2.314
Height : 9.925
Entry
ampl
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2
4
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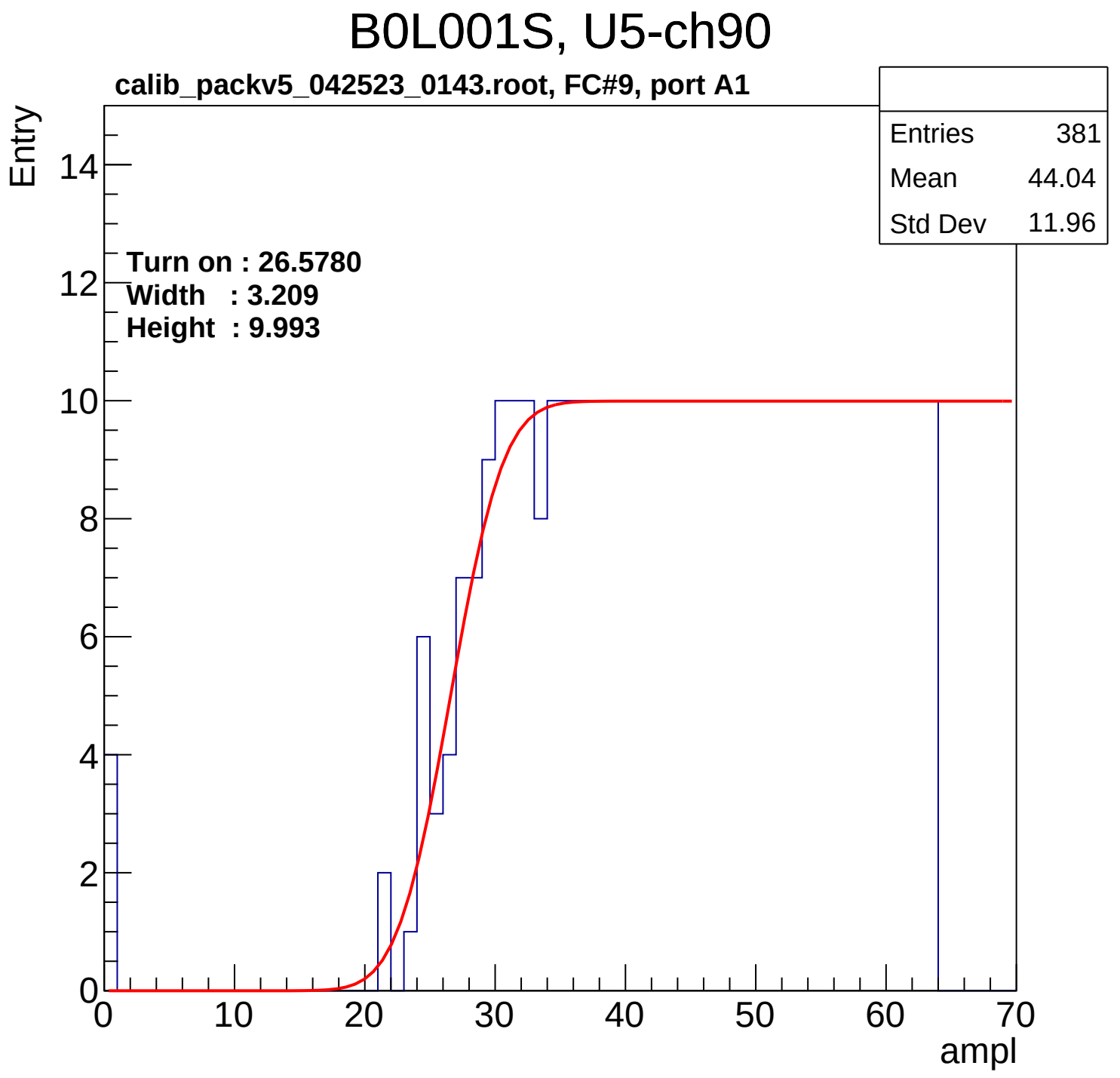
B0L001S, U5-ch90
calib_packv5_042523_0143.root, FC#9, port A1
Entries 381
Mean 44.04
Std Dev 11.96
Turn on : 26.5780
Width : 3.209
Height : 9.993
Entry
ampl
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2
4
6
8
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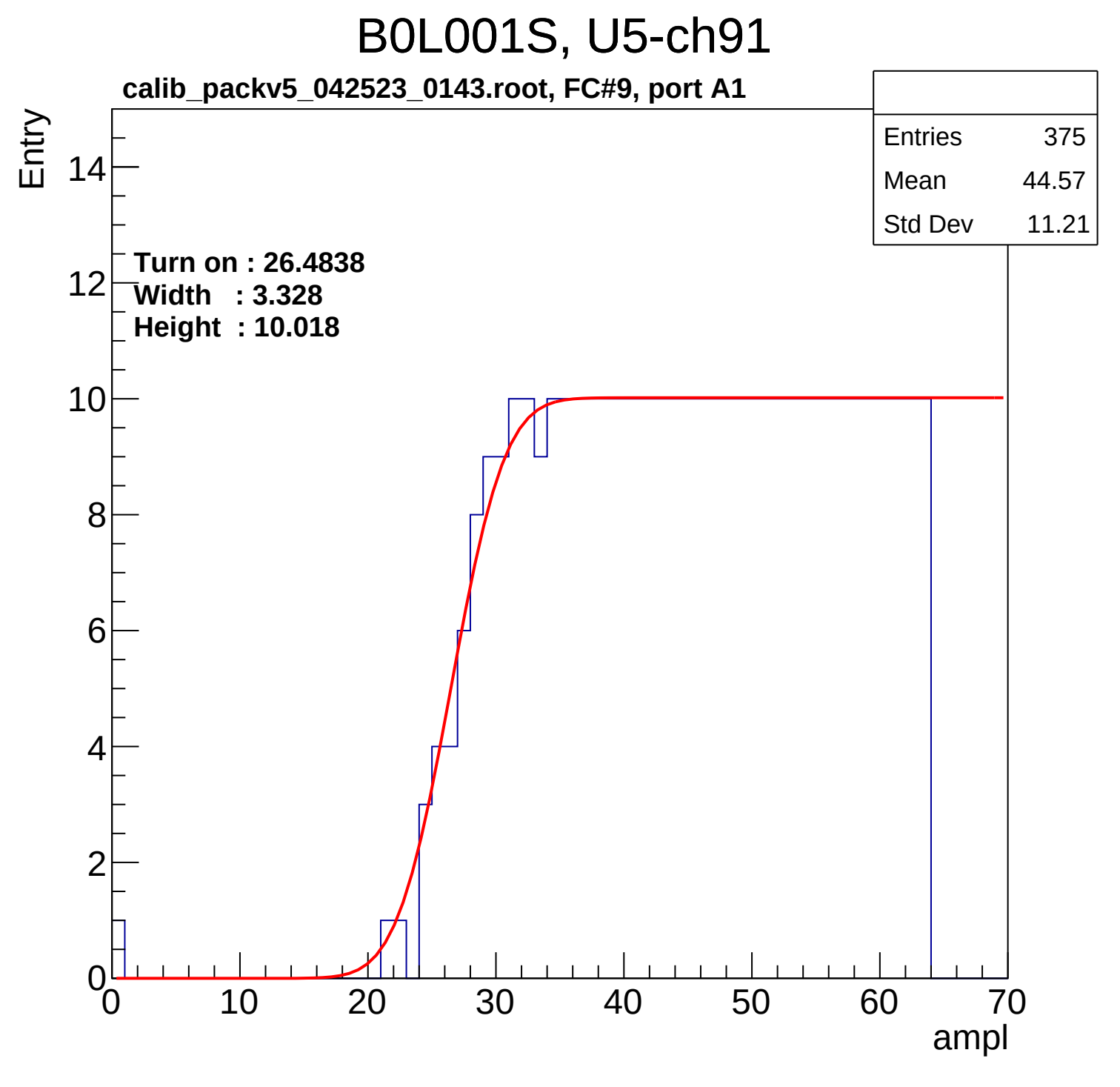
B0L001S, U5-ch91
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.57
Std Dev 11.21
Turn on : 26.4838
Width : 3.328
Height : 10.018
Entry
ampl
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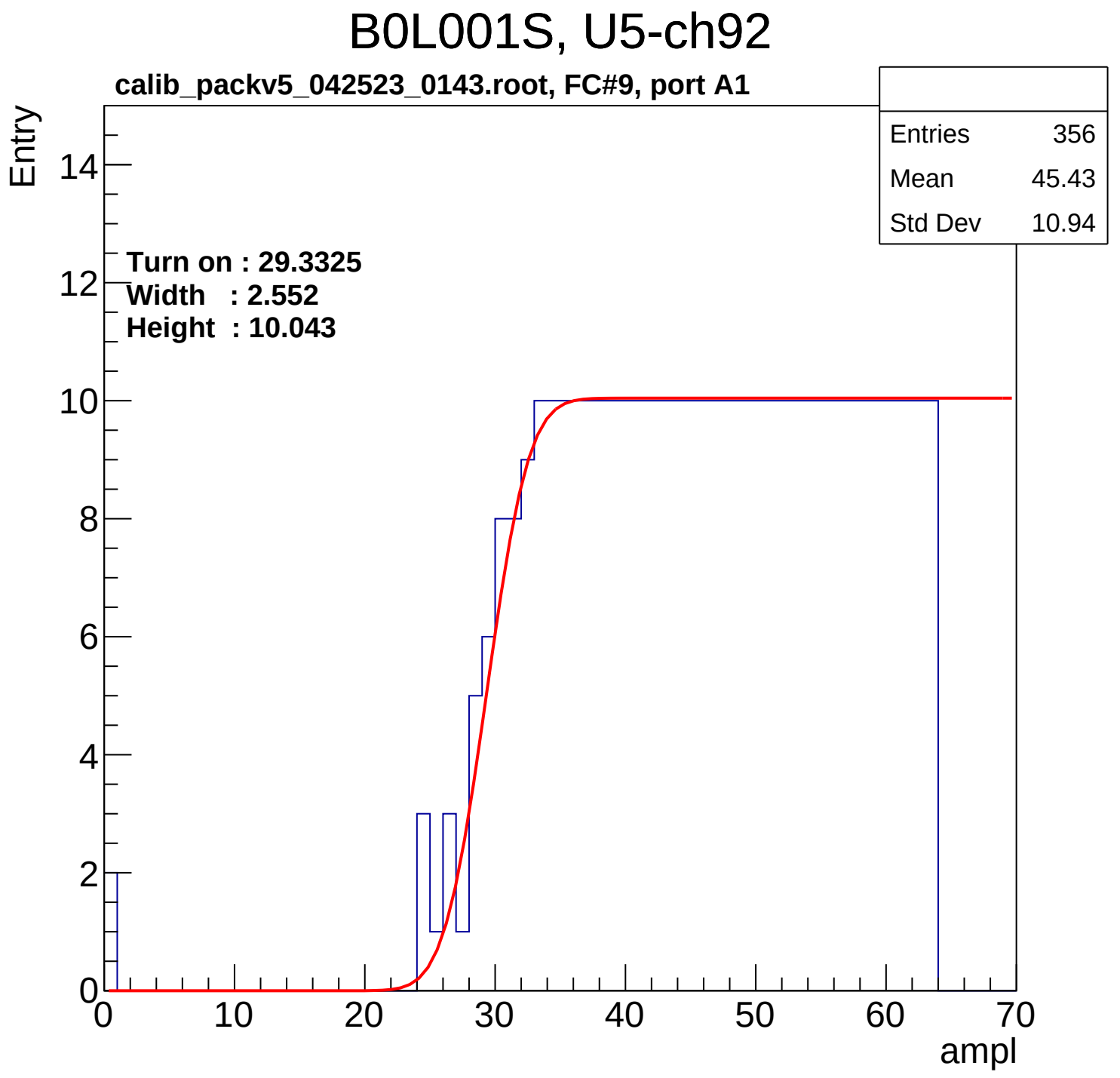
B0L001S, U5-ch92
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.43
Std Dev 10.94
Turn on : 29.3325
Width : 2.552
Height : 10.043
Entry
ampl
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2
4
6
8
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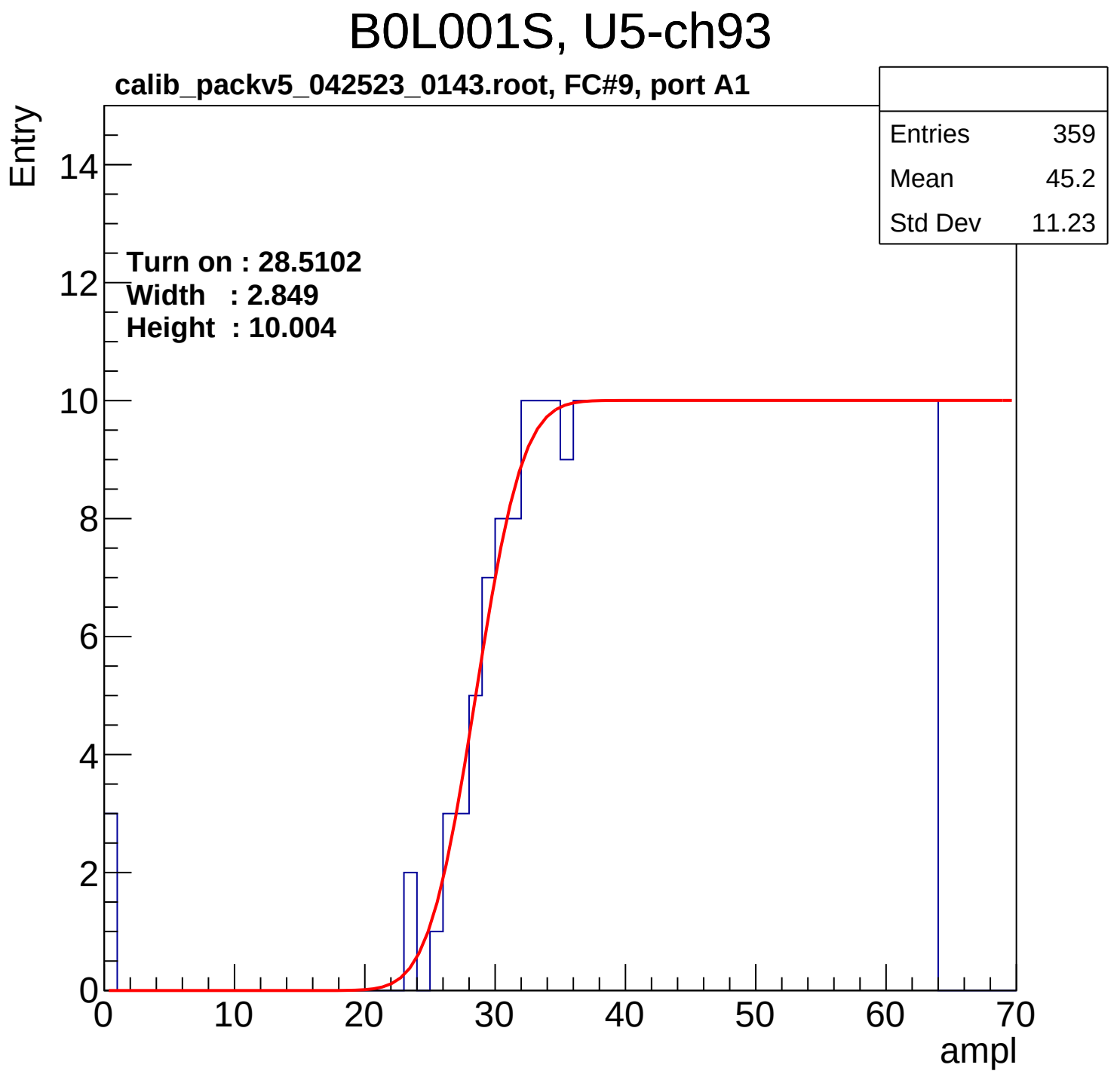
B0L001S, U5-ch93
calib_packv5_042523_0143.root, FC#9, port A1
Entries 359
Mean 45.2
Std Dev 11.23
Turn on : 28.5102
Width : 2.849
Height : 10.004
Entry
ampl
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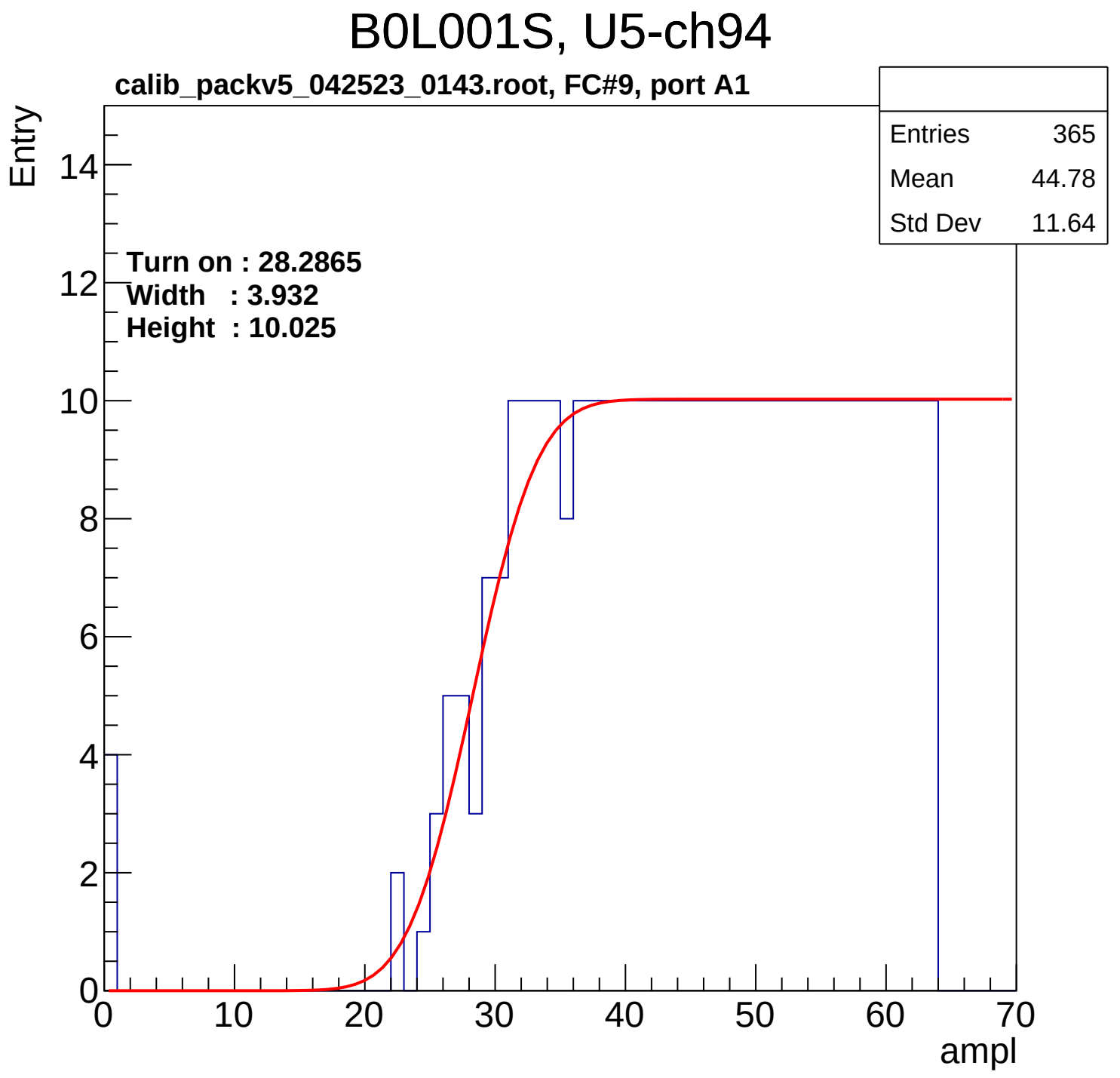
B0L001S, U5-ch94
calib_packv5_042523_0143.root, FC#9, port A1
Entries 365
Mean 44.78
Std Dev 11.64
Turn on : 28.2865
Width : 3.932
Height : 10.025
Entry
ampl
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2
4
6
8
10
12
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0
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60
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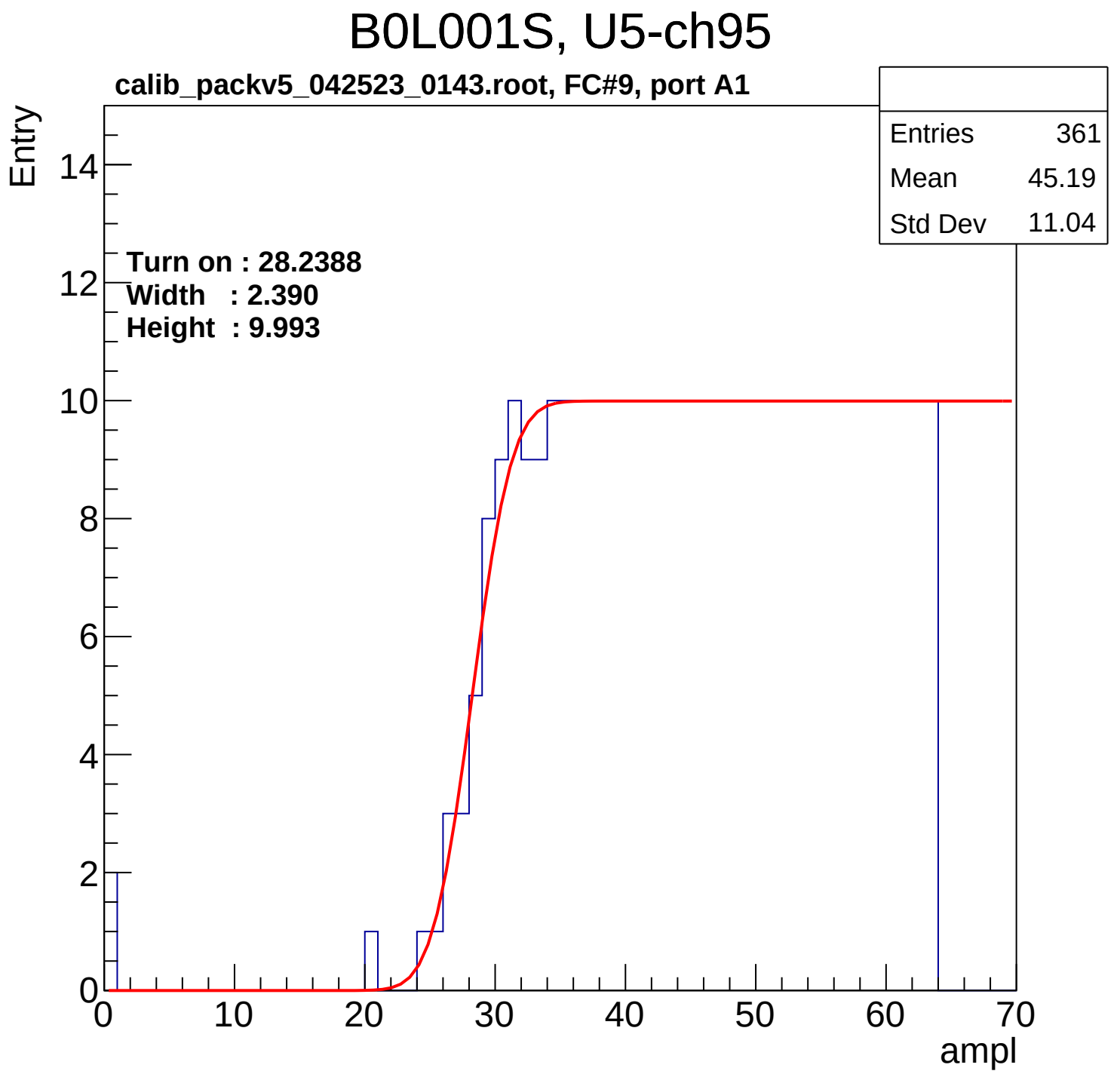
B0L001S, U5-ch95
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.19
Std Dev 11.04
Turn on : 28.2388
Width : 2.390
Height : 9.993
Entry
ampl
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4
6
8
10
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0
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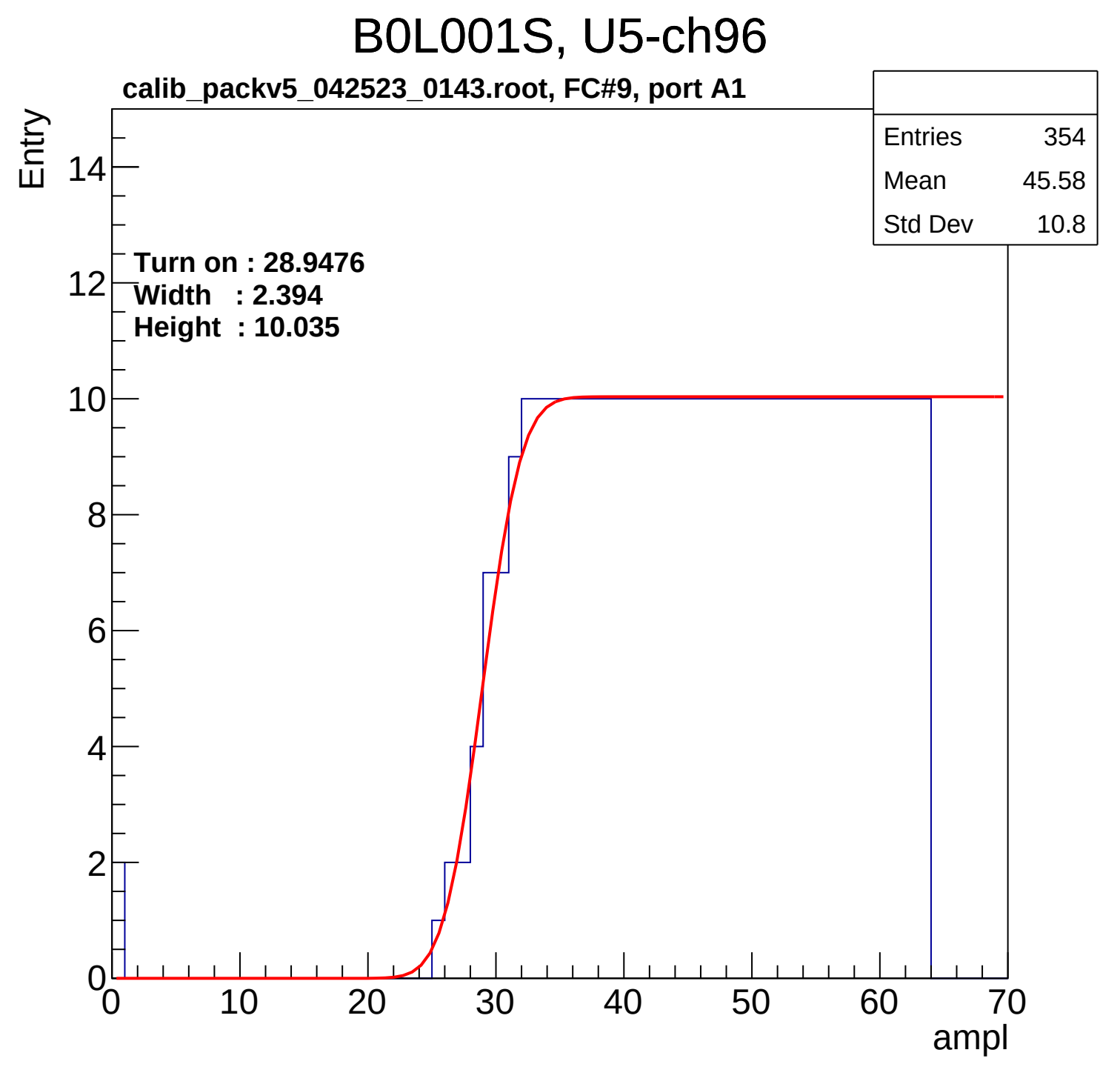
B0L001S, U5-ch96
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.58
Std Dev 10.8
Turn on : 28.9476
Width : 2.394
Height : 10.035
Entry
ampl
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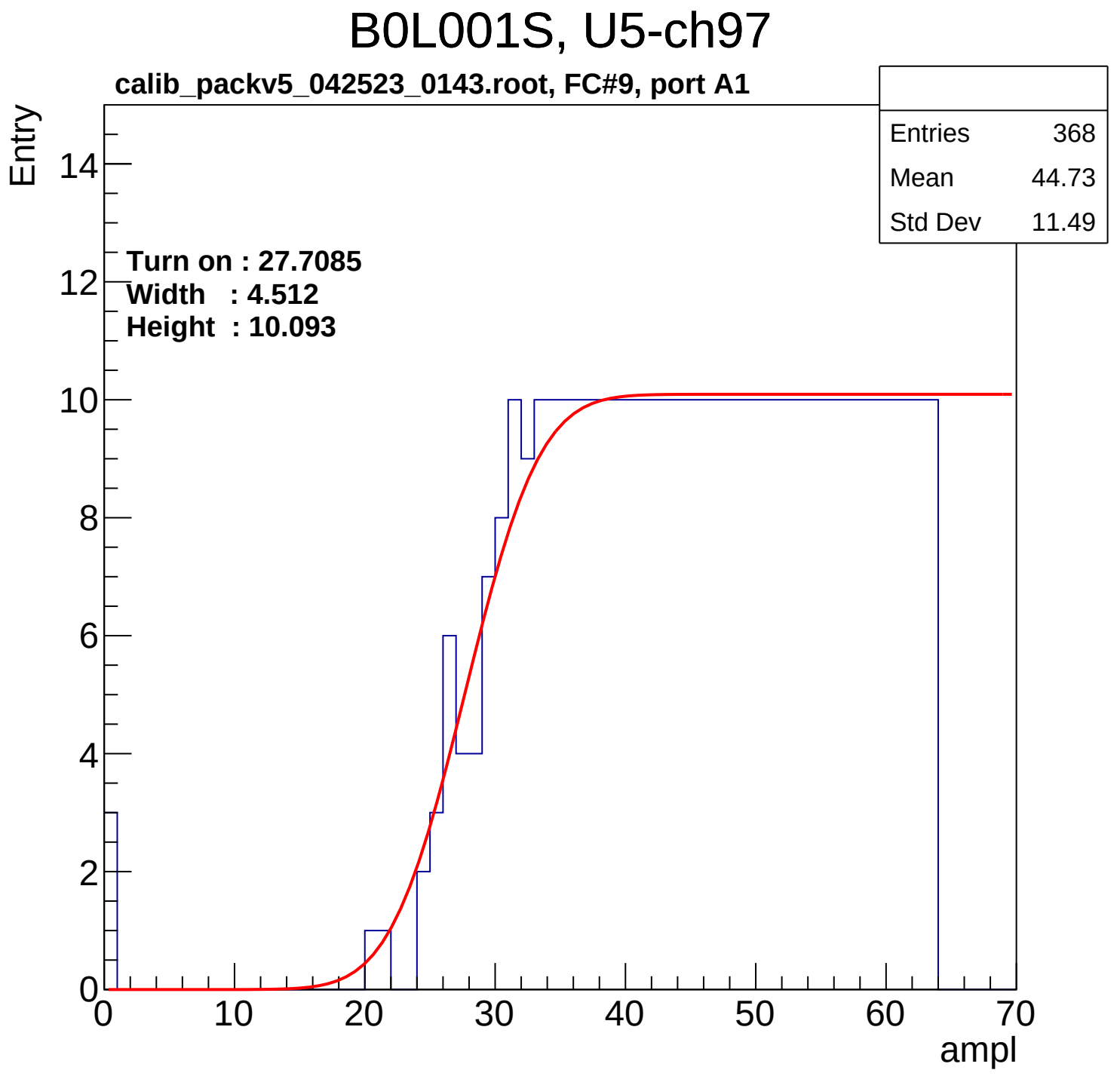
B0L001S, U5-ch97
calib_packv5_042523_0143.root, FC#9, port A1
Entries 368
Mean 44.73
Std Dev 11.49
Turn on : 27.7085
Width : 4.512
Height : 10.093
Entry
ampl
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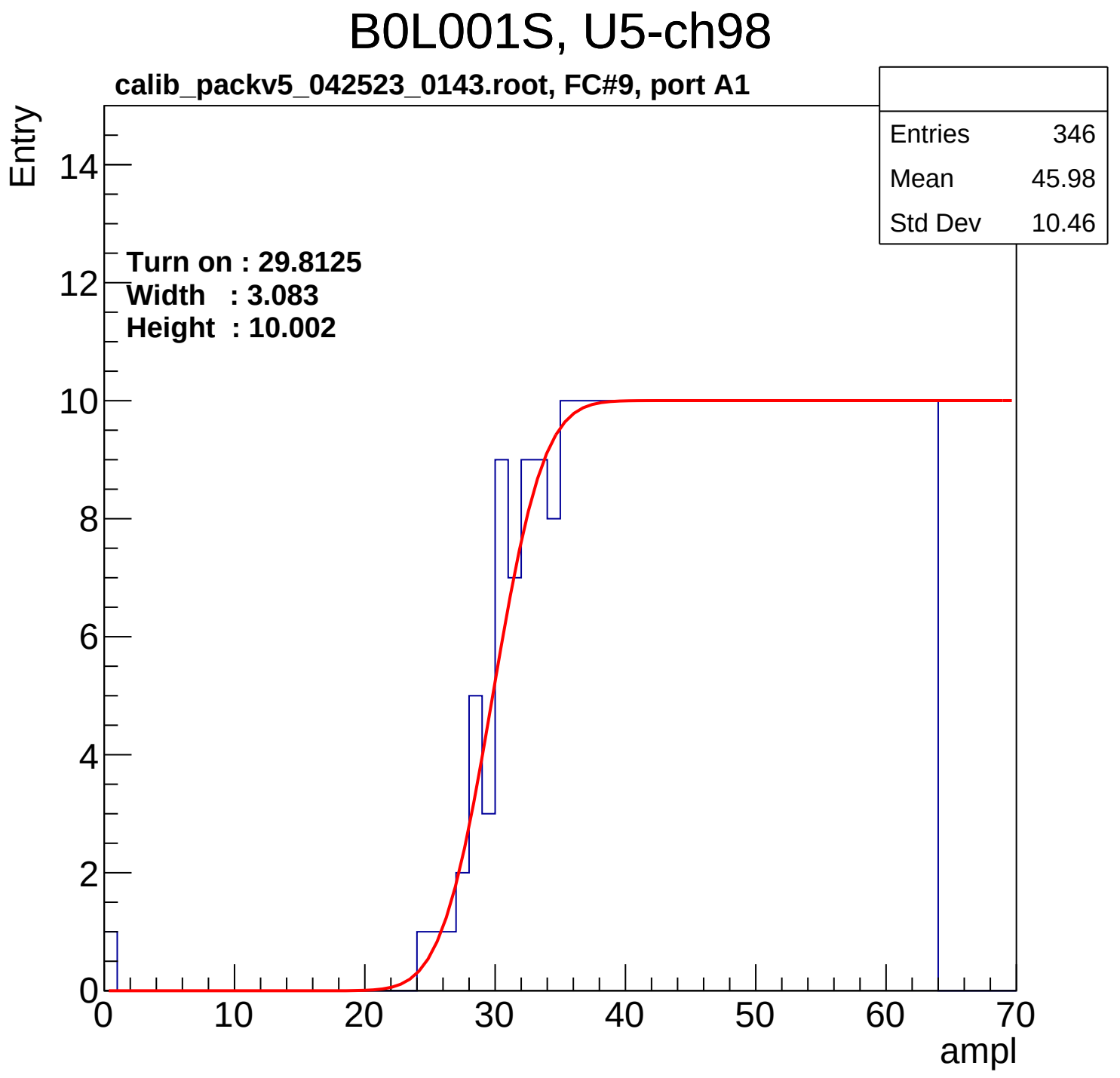
B0L001S, U5-ch98
calib_packv5_042523_0143.root, FC#9, port A1
Entries 346
Mean 45.98
Std Dev 10.46
Turn on : 29.8125
Width : 3.083
Height : 10.002
Entry
ampl
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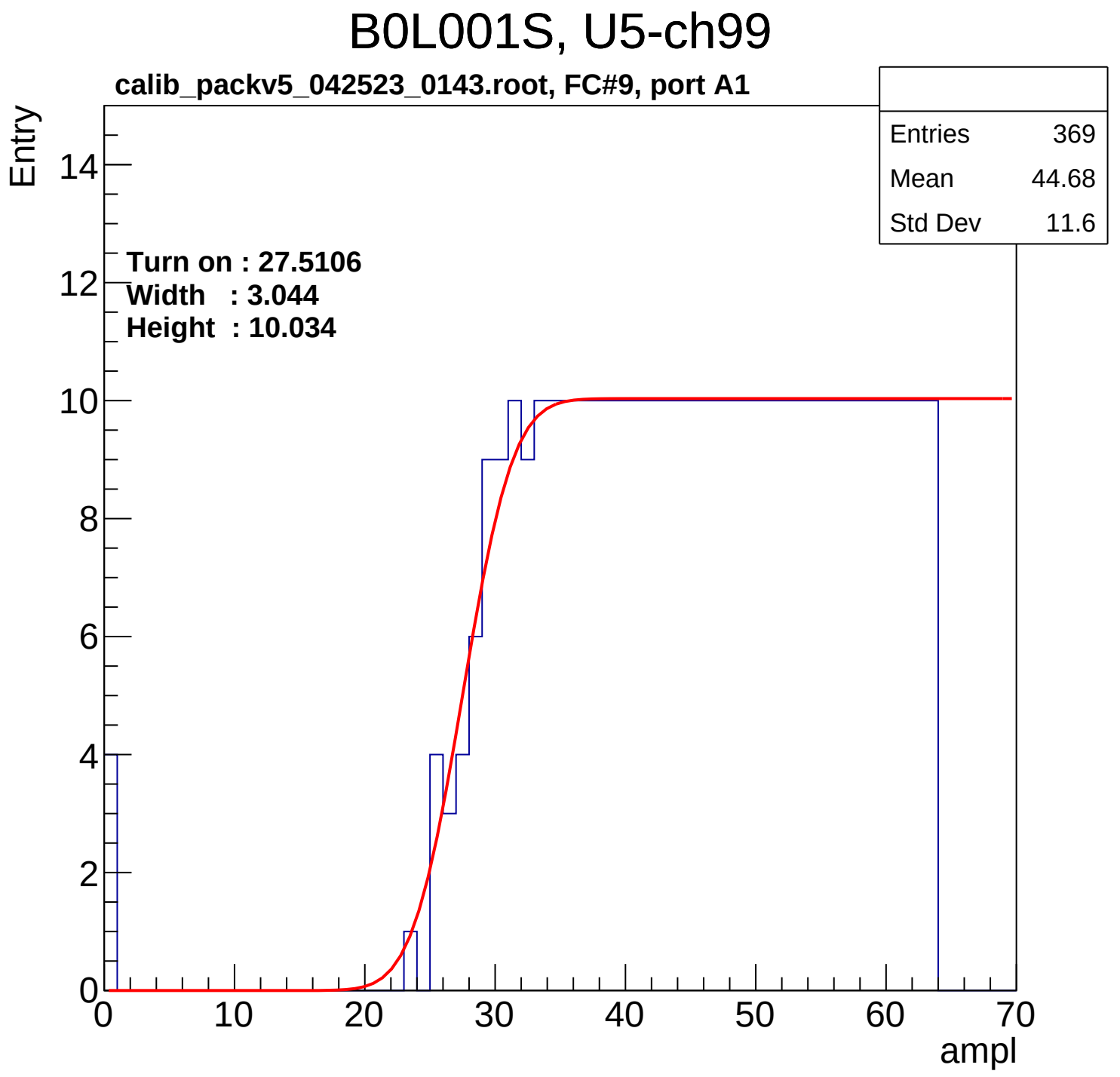
B0L001S, U5-ch99
calib_packv5_042523_0143.root, FC#9, port A1
Entries 369
Mean 44.68
Std Dev 11.6
Turn on : 27.5106
Width : 3.044
Height : 10.034
Entry
ampl
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6
8
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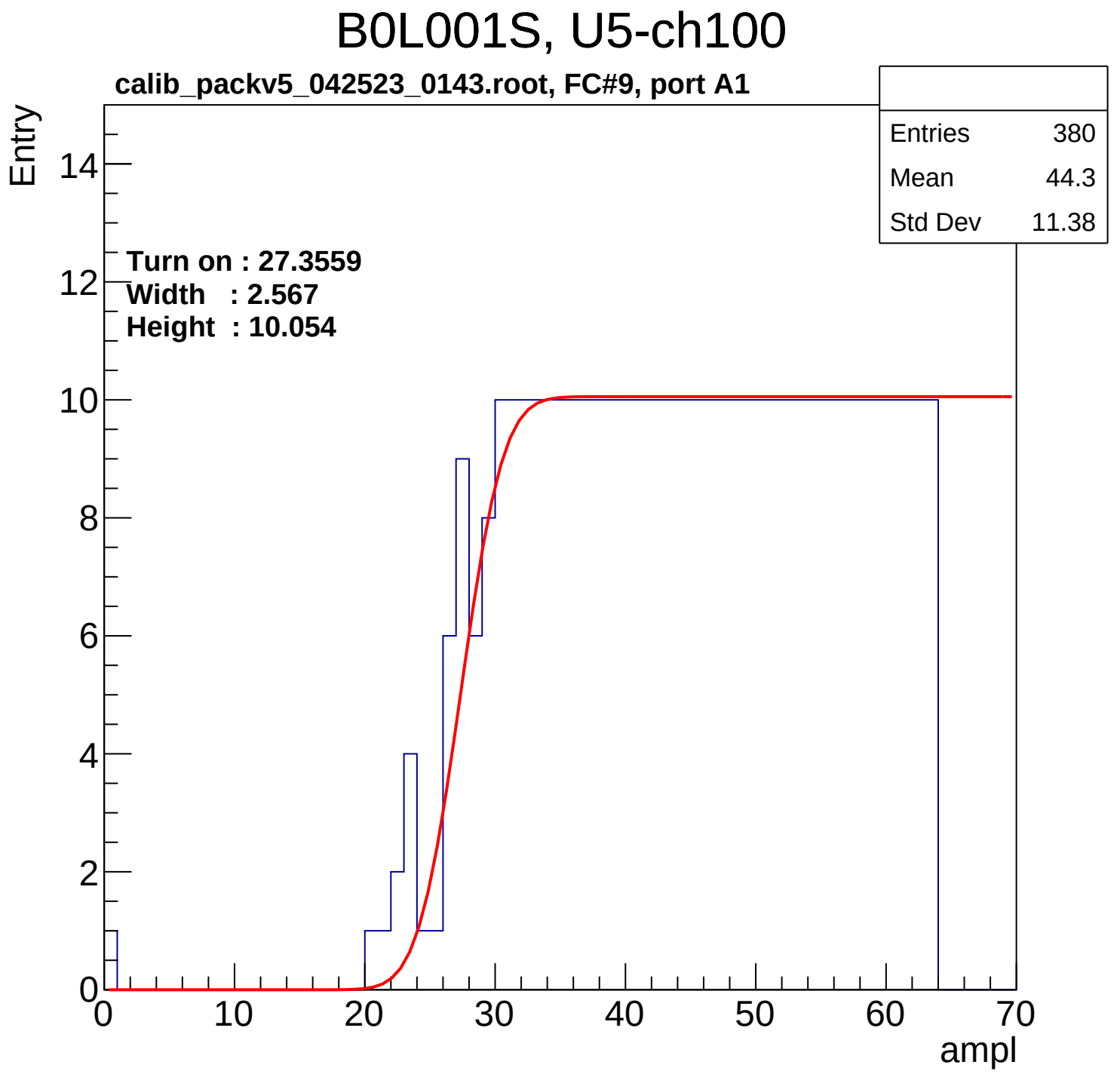
B0L001S, U5-ch100
calib_packv5_042523_0143.root, FC#9, port A1
Entries 380
Mean 44.3
Std Dev 11.38
Turn on : 27.3559
Width : 2.567
Height : 10.054
Entry
ampl
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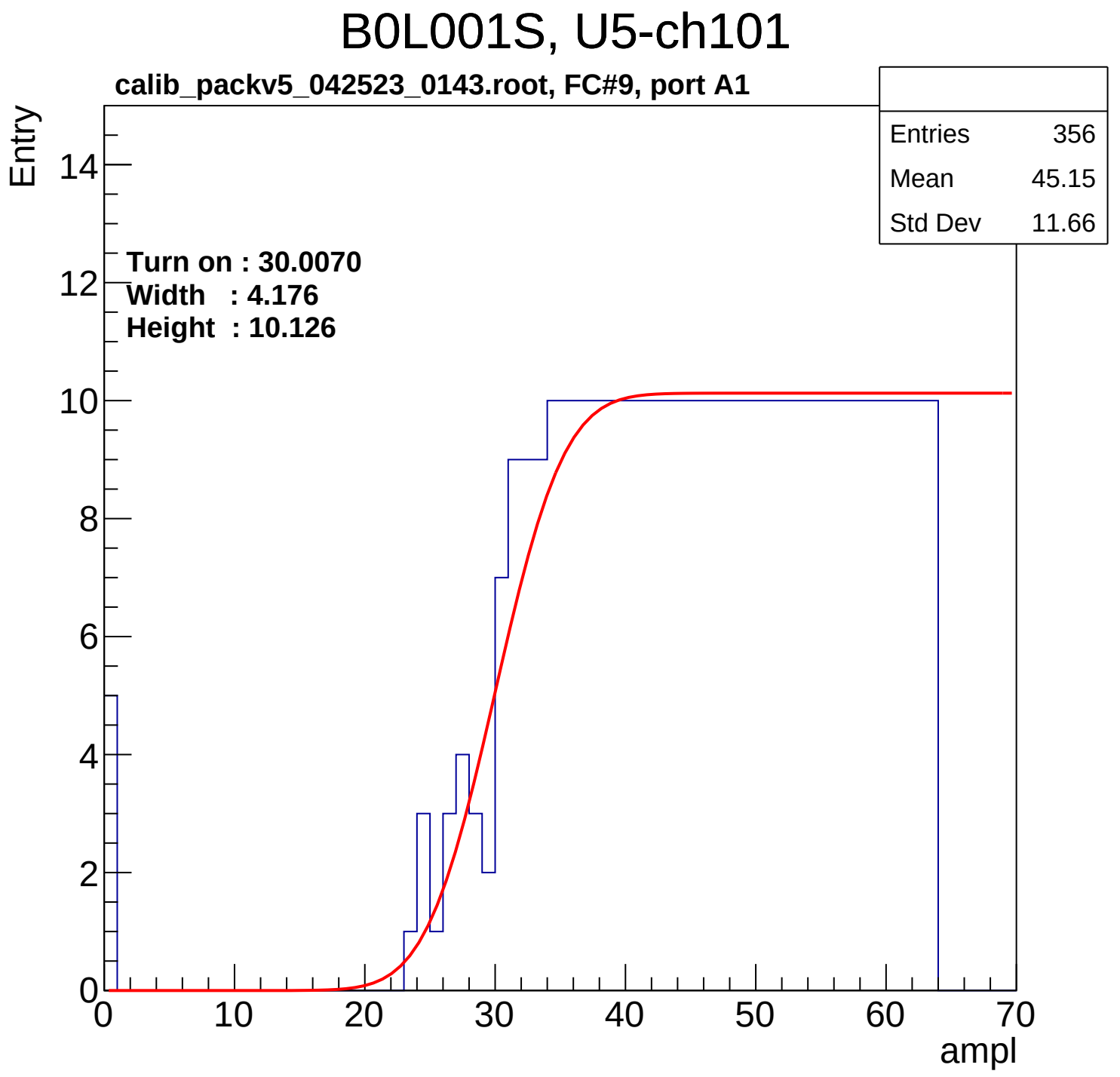
B0L001S, U5-ch101
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 45.15
Std Dev 11.66
Turn on : 30.0070
Width : 4.176
Height : 10.126
Entry
ampl
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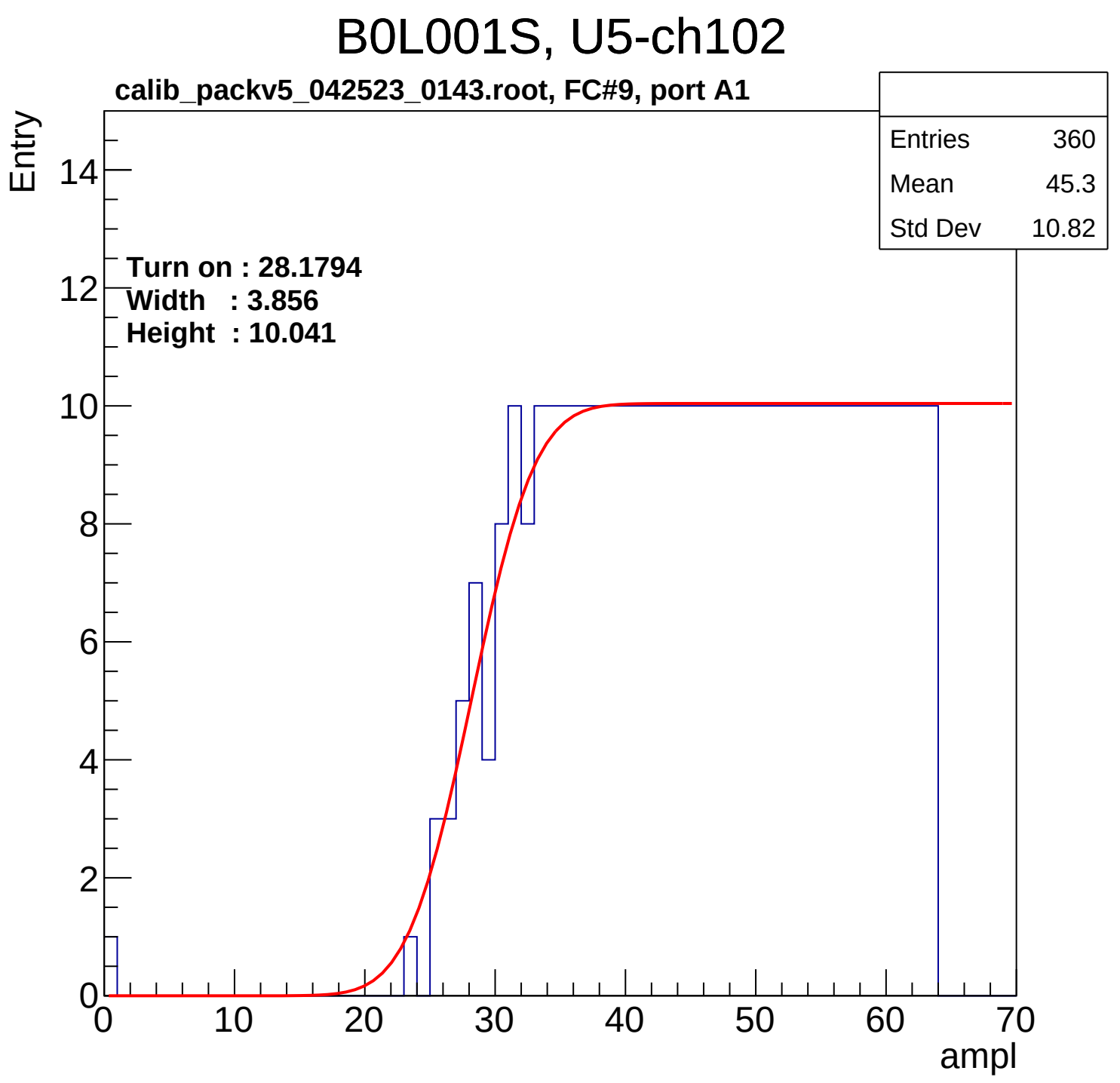
B0L001S, U5-ch102
calib_packv5_042523_0143.root, FC#9, port A1
Entries 360
Mean 45.3
Std Dev 10.82
Turn on : 28.1794
Width : 3.856
Height : 10.041
Entry
ampl
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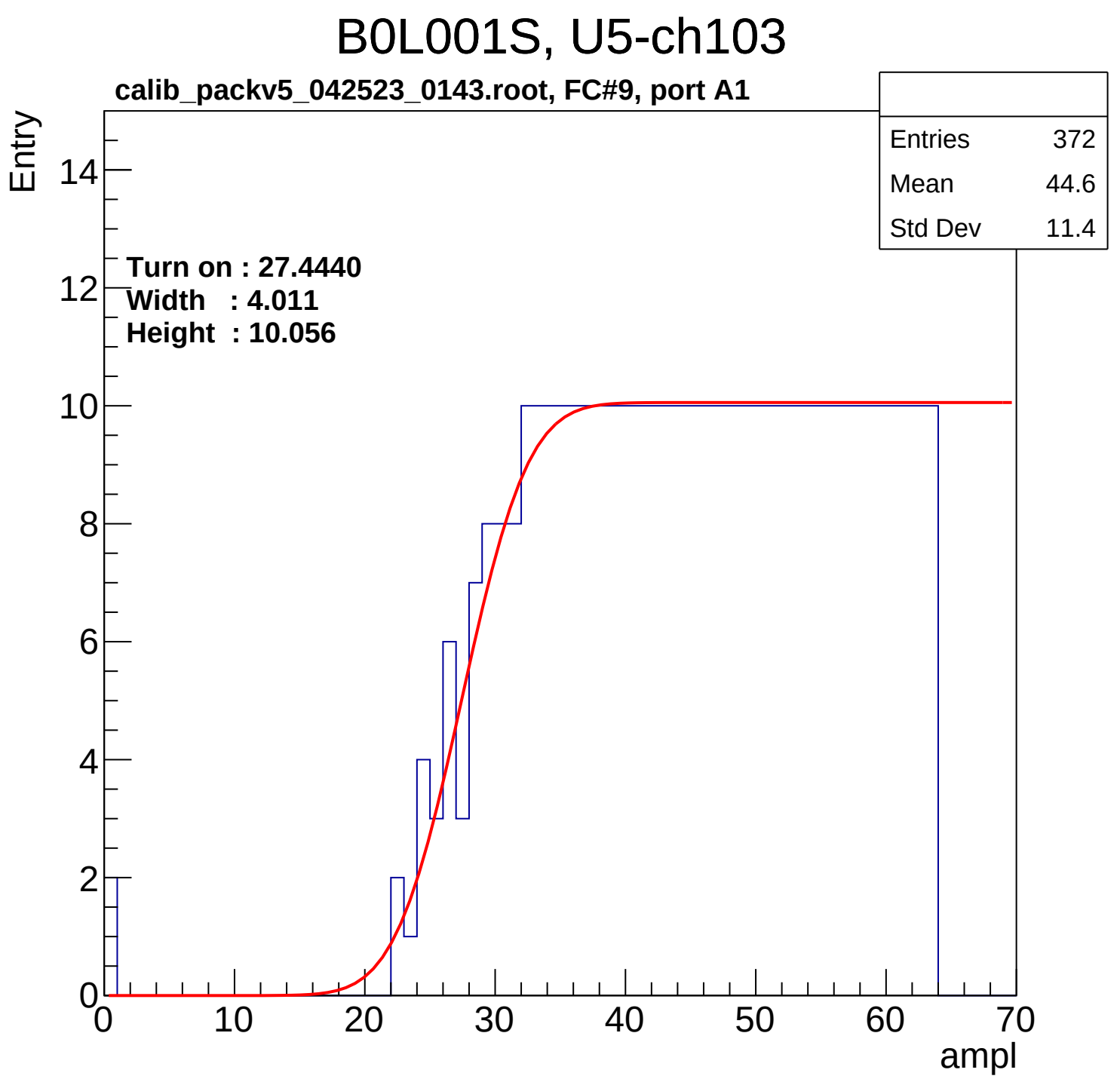
B0L001S, U5-ch103
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.6
Std Dev 11.4
Turn on : 27.4440
Width : 4.011
Height : 10.056
Entry
ampl
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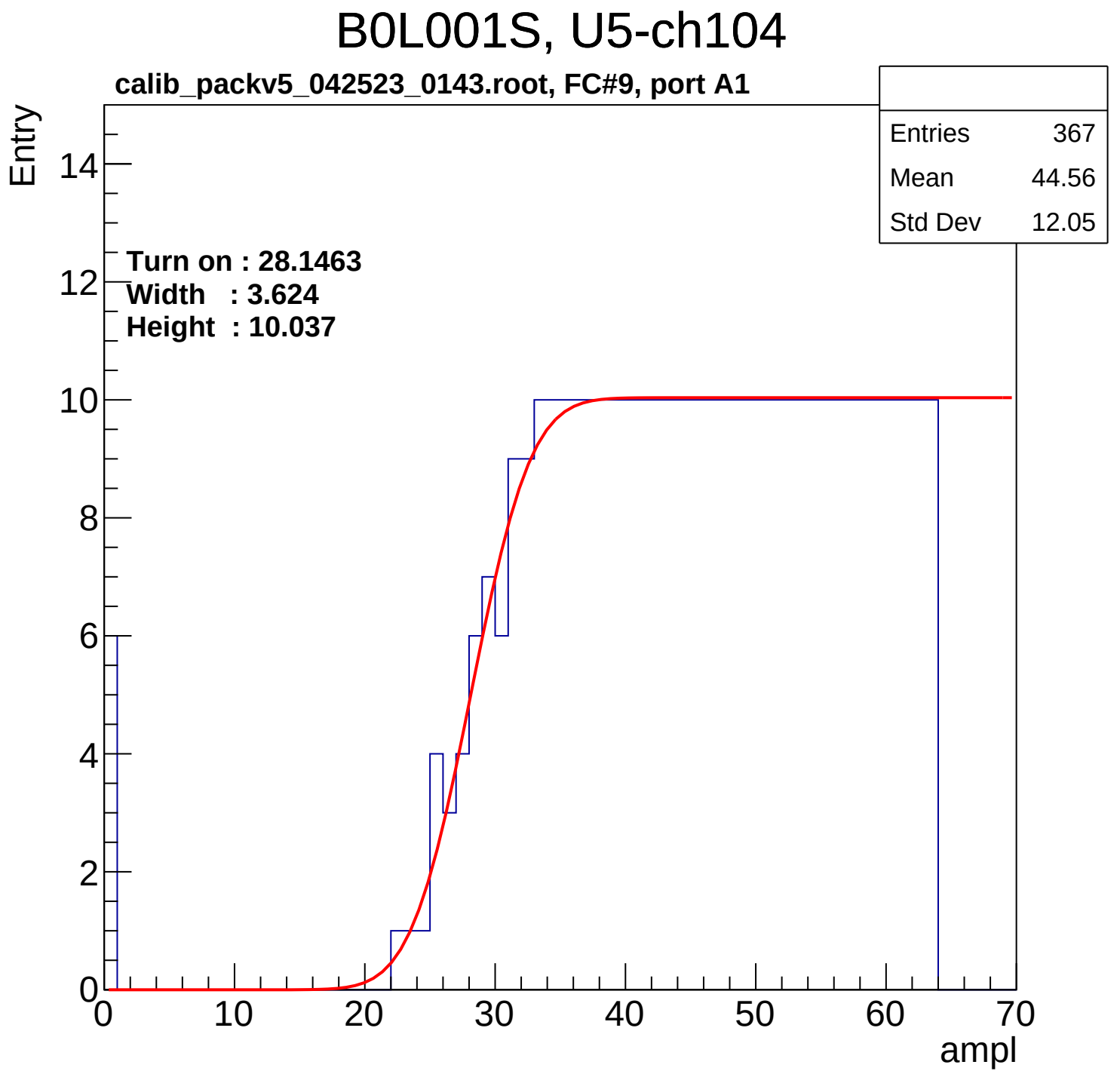
B0L001S, U5-ch104
calib_packv5_042523_0143.root, FC#9, port A1
Entries 367
Mean 44.56
Std Dev 12.05
Turn on : 28.1463
Width : 3.624
Height : 10.037
Entry
ampl
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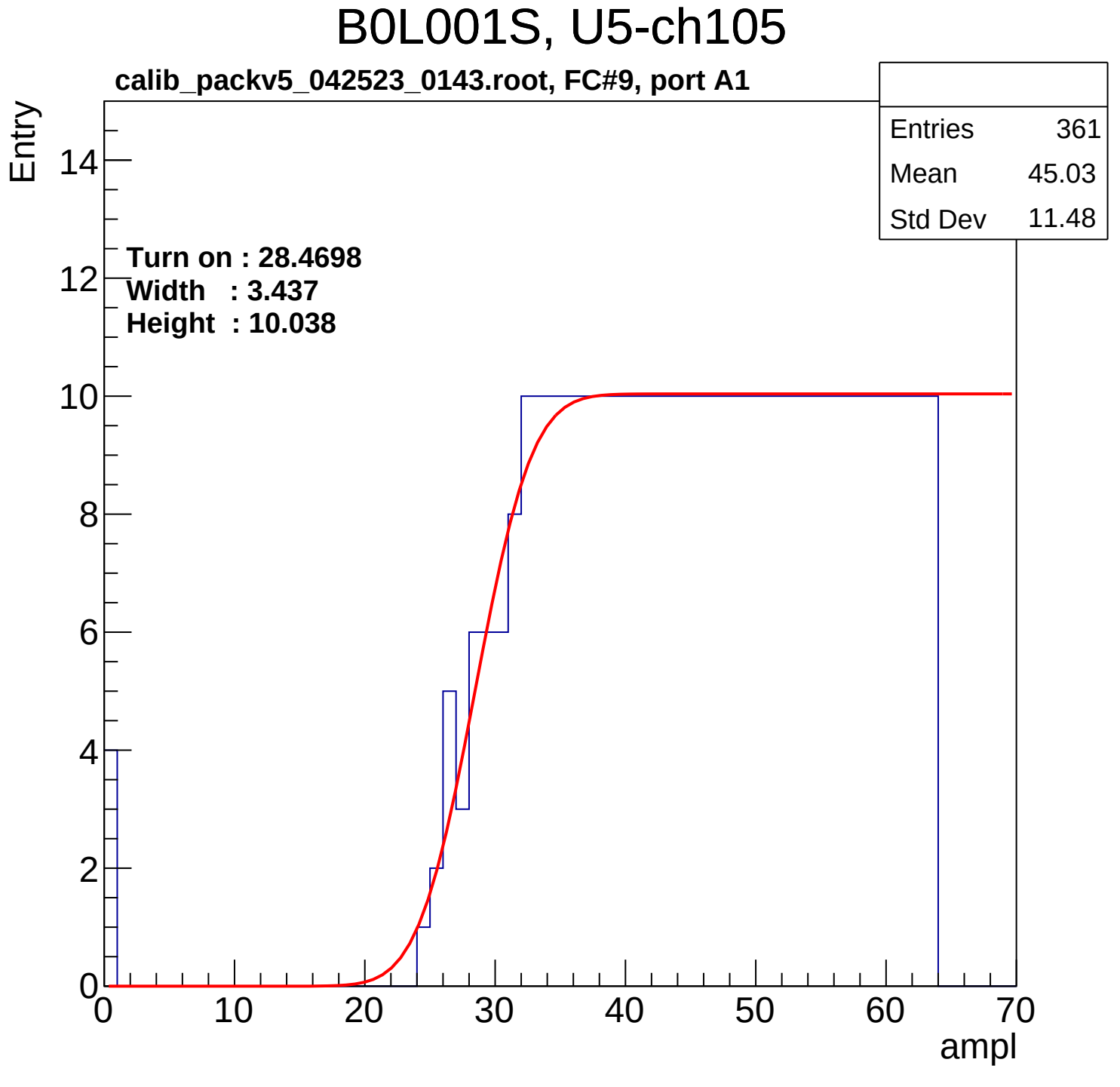
B0L001S, U5-ch105
calib_packv5_042523_0143.root, FC#9, port A1
Entries 361
Mean 45.03
Std Dev 11.48
Turn on : 28.4698
Width : 3.437
Height : 10.038
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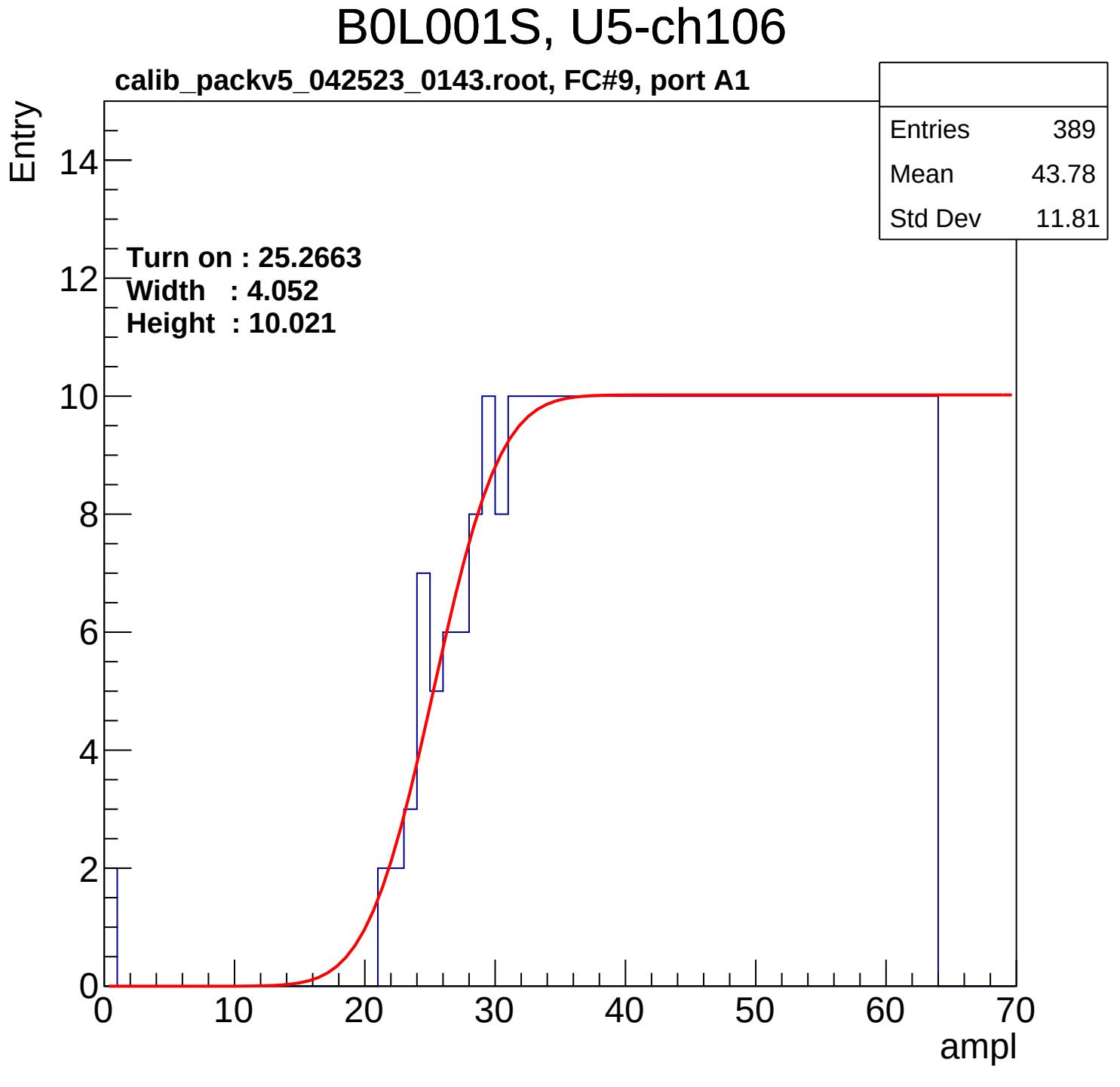
B0L001S, U5-ch106
calib_packv5_042523_0143.root, FC#9, port A1
Entries 389
Mean 43.78
Std Dev 11.81
Turn on : 25.2663
Width : 4.052
Height : 10.021
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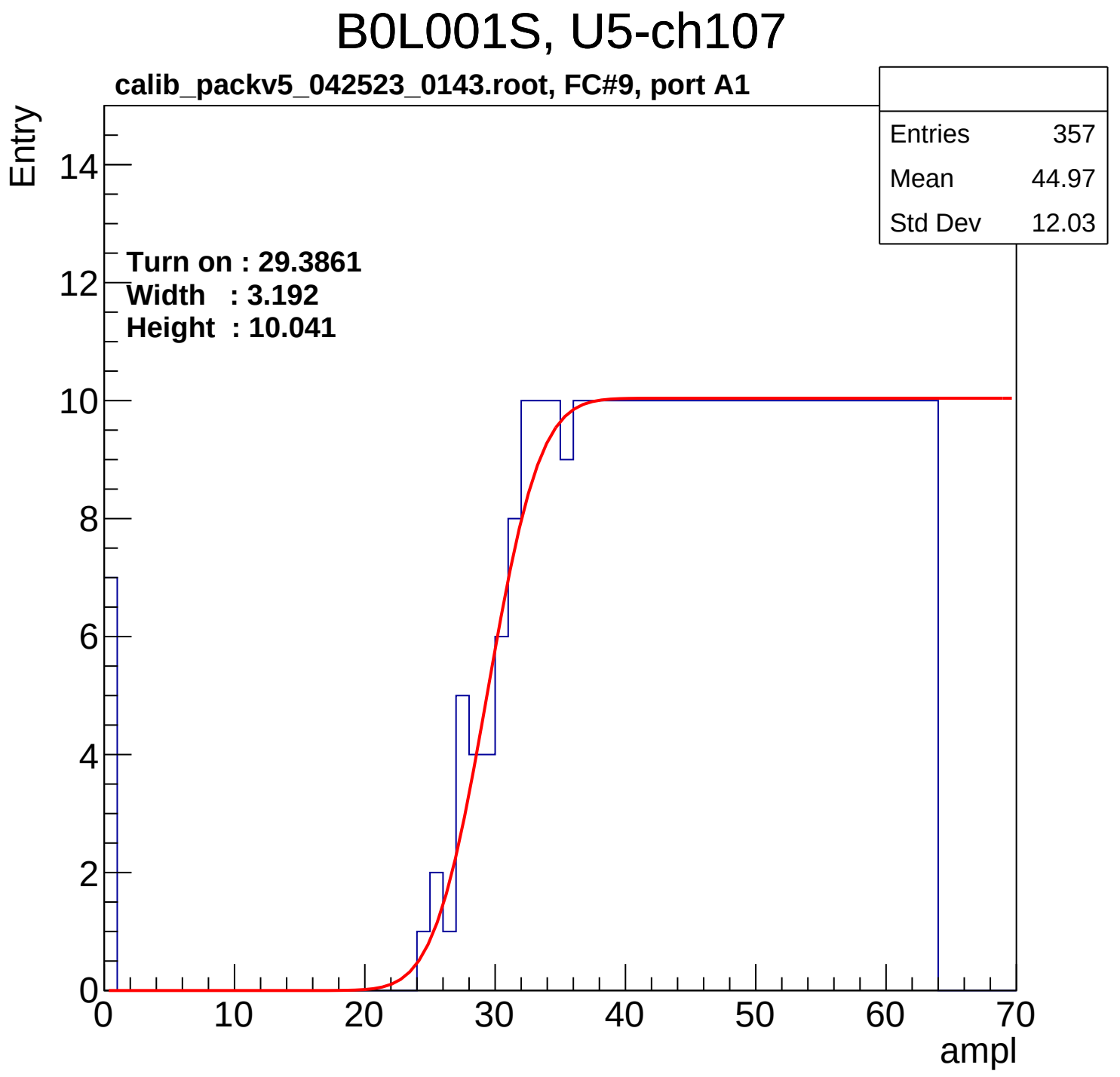
B0L001S, U5-ch107
calib_packv5_042523_0143.root, FC#9, port A1
Entries 357
Mean 44.97
Std Dev 12.03
Turn on : 29.3861
Width : 3.192
Height : 10.041
Entry
ampl
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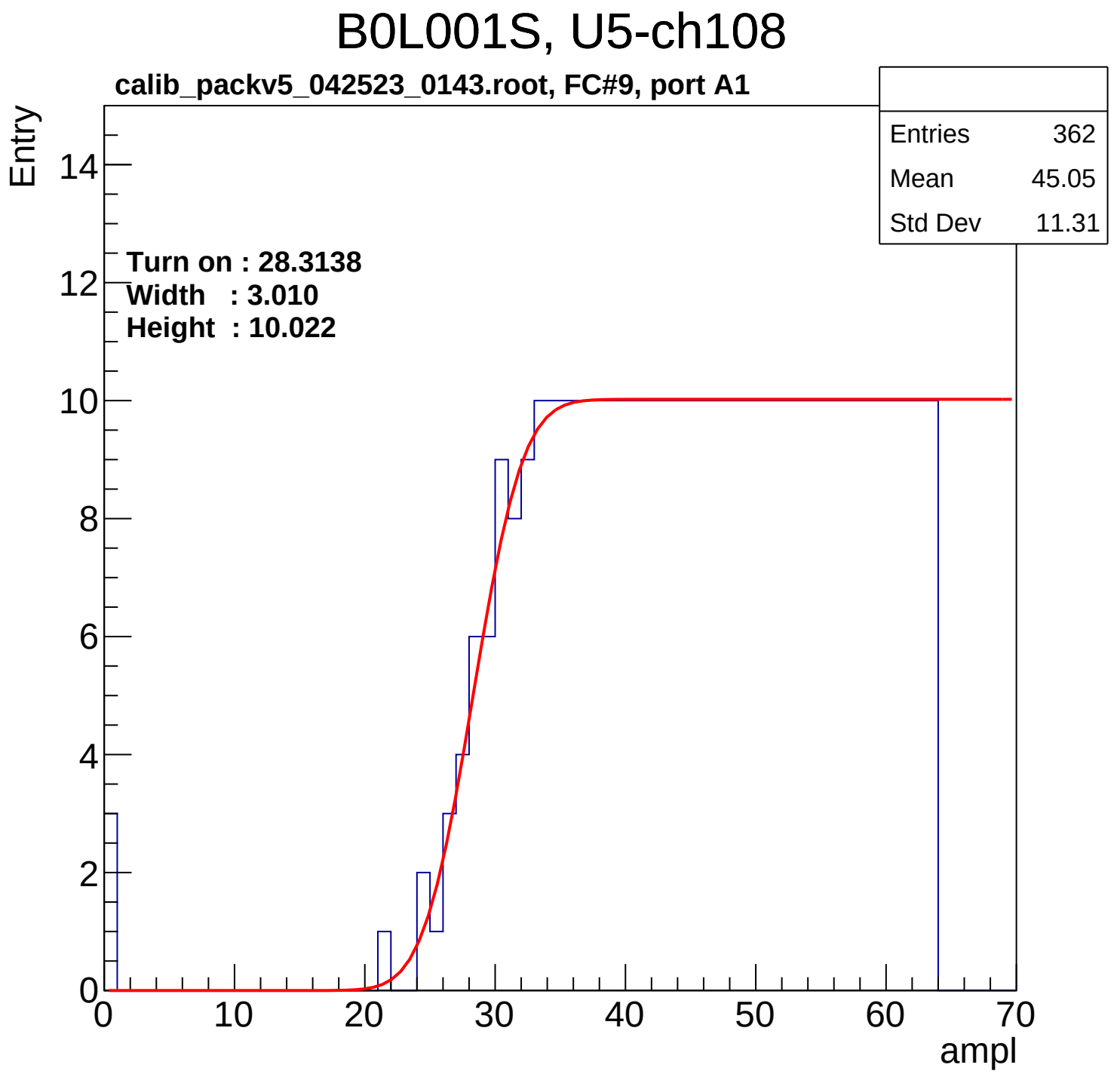
B0L001S, U5-ch108
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 45.05
Std Dev 11.31
Turn on : 28.3138
Width : 3.010
Height : 10.022
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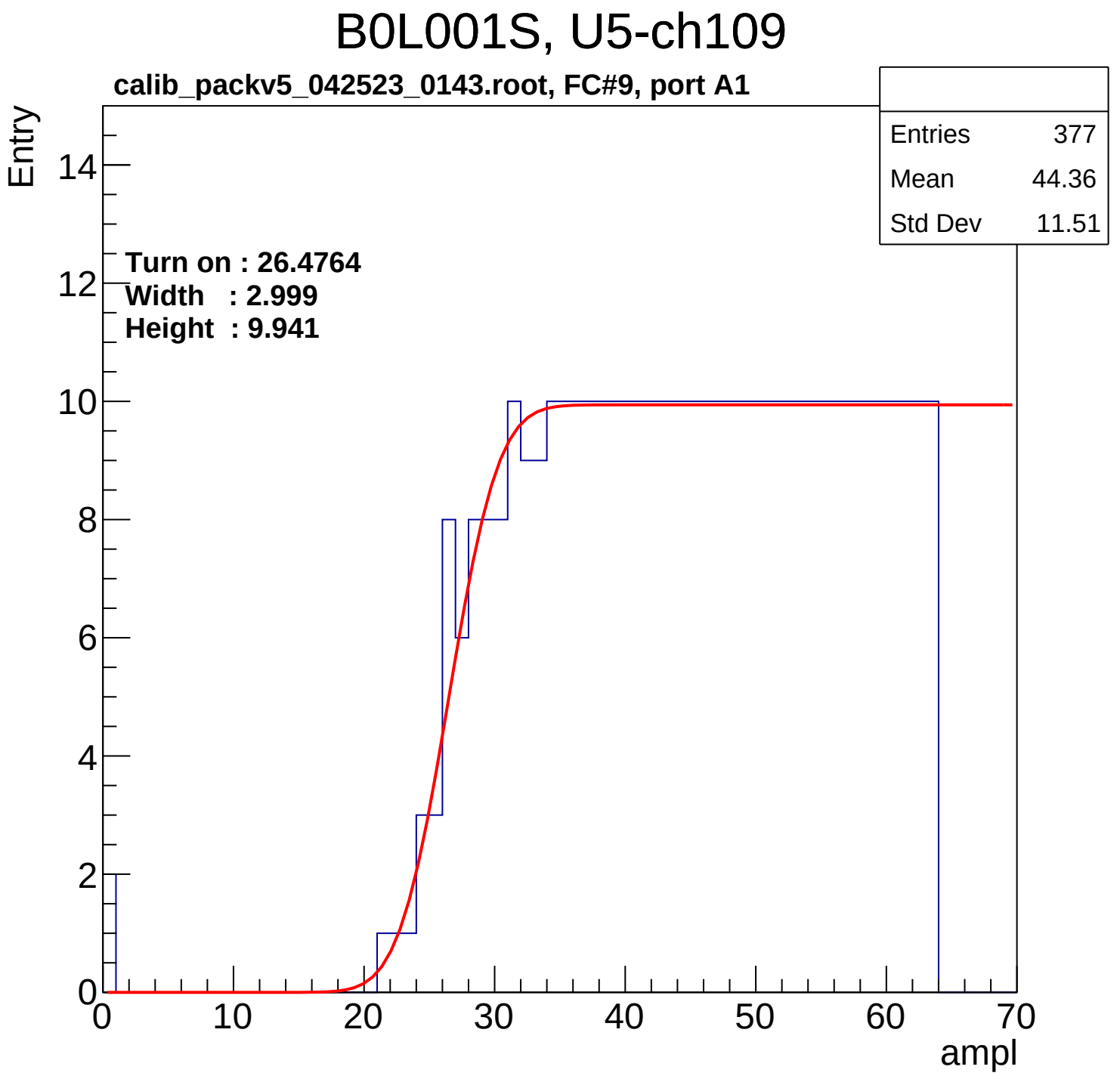
B0L001S, U5-ch109
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.36
Std Dev 11.51
Turn on : 26.4764
Width : 2.999
Height : 9.941
Entry
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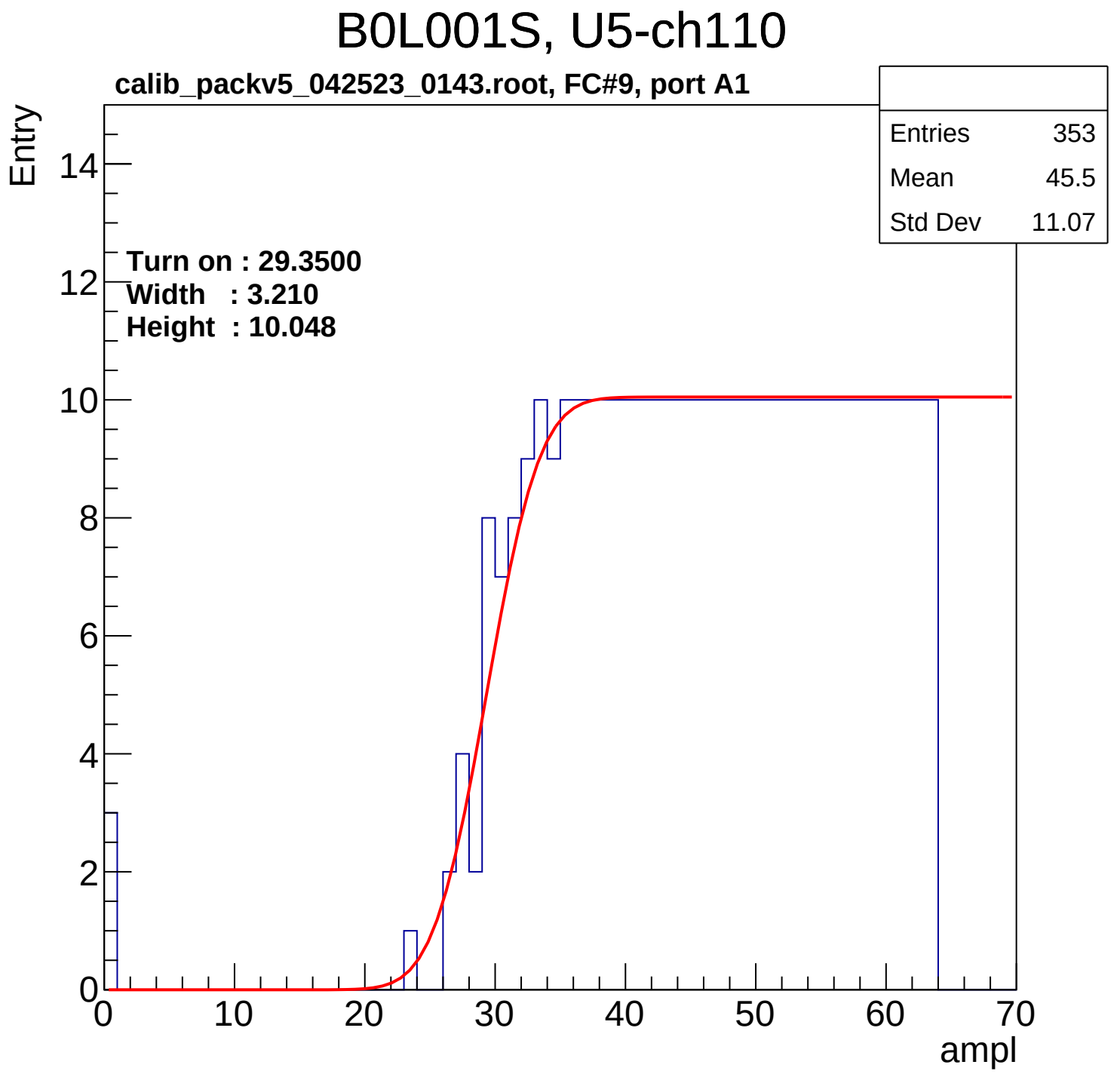
B0L001S, U5-ch110
calib_packv5_042523_0143.root, FC#9, port A1
Entries 353
Mean 45.5
Std Dev 11.07
Turn on : 29.3500
Width : 3.210
Height : 10.048
Entry
ampl
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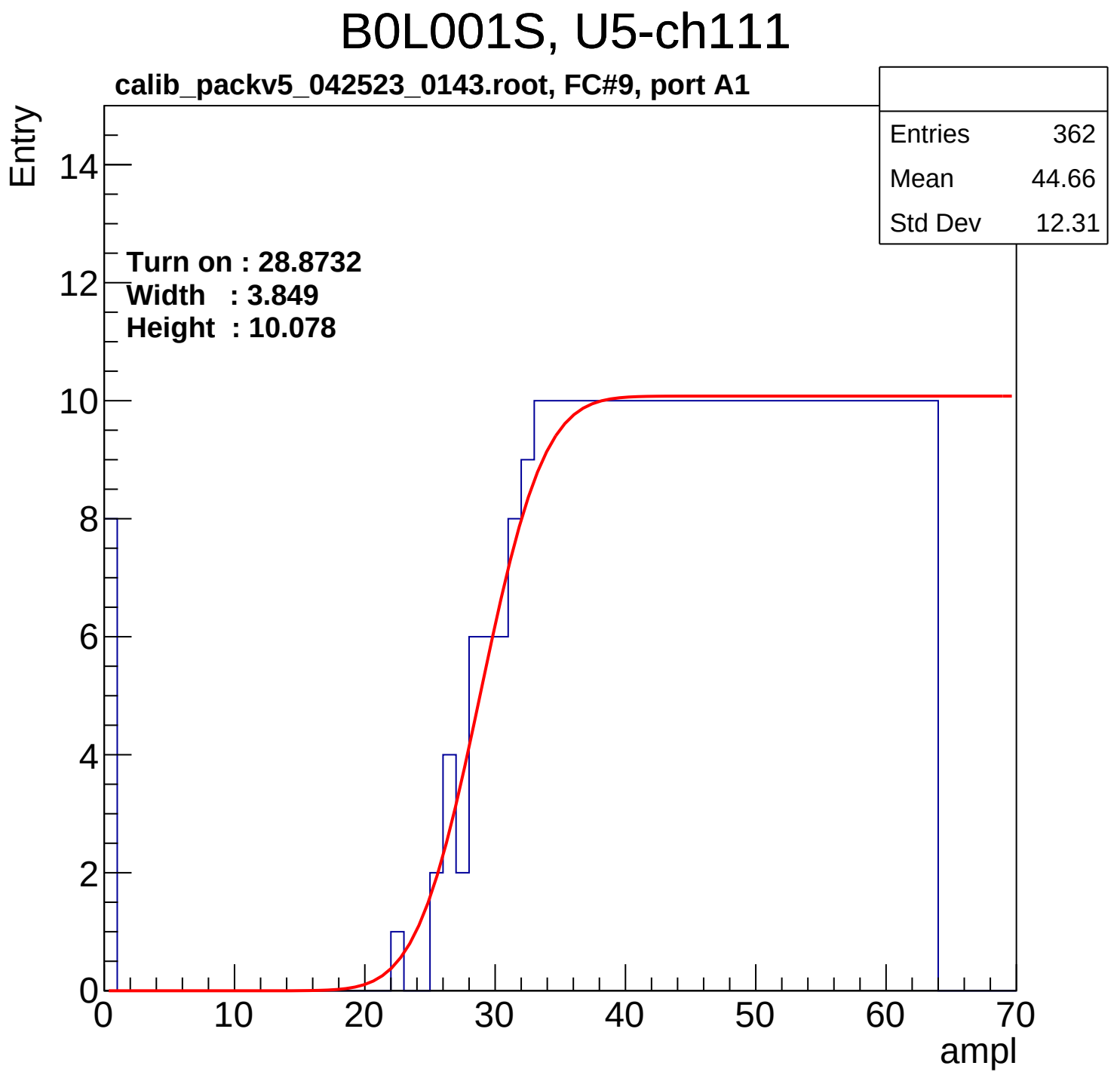
B0L001S, U5-ch111
calib_packv5_042523_0143.root, FC#9, port A1
Entries 362
Mean 44.66
Std Dev 12.31
Turn on : 28.8732
Width : 3.849
Height : 10.078
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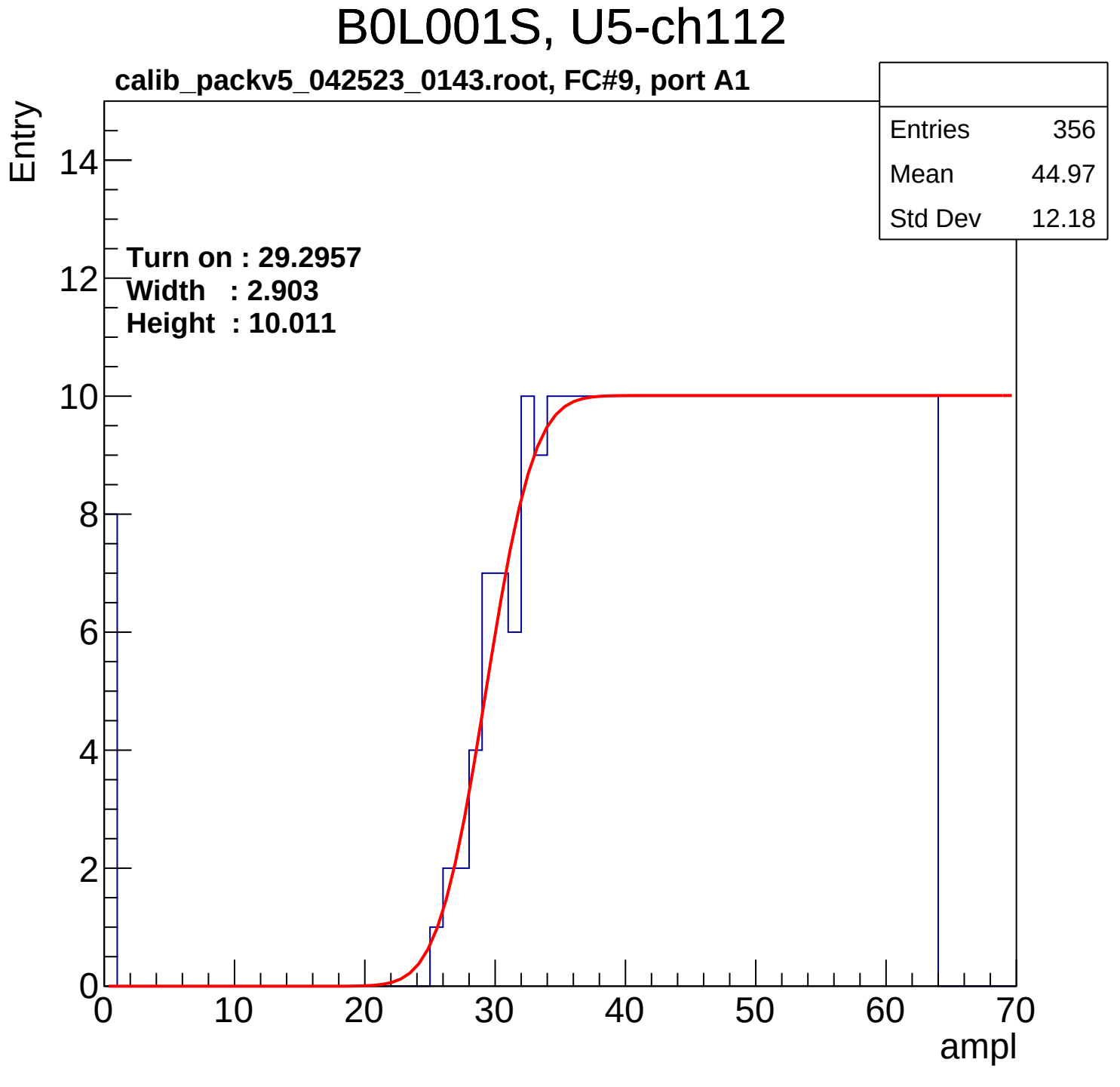
B0L001S, U5-ch112
calib_packv5_042523_0143.root, FC#9, port A1
Entries 356
Mean 44.97
Std Dev 12.18
Turn on : 29.2957
Width : 2.903
Height : 10.011
Entry
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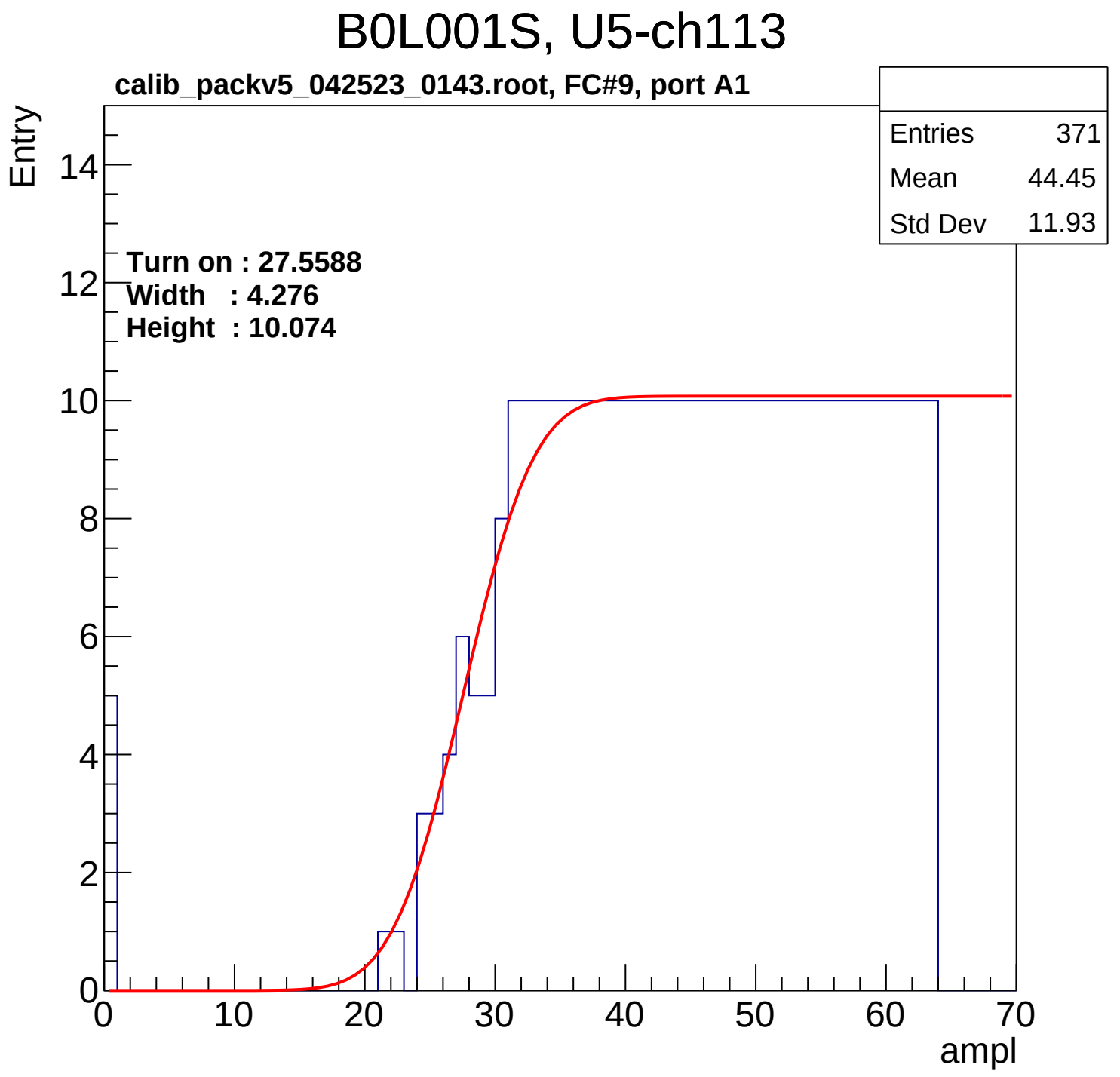
B0L001S, U5-ch113
calib_packv5_042523_0143.root, FC#9, port A1
Entries 371
Mean 44.45
Std Dev 11.93
Turn on : 27.5588
Width : 4.276
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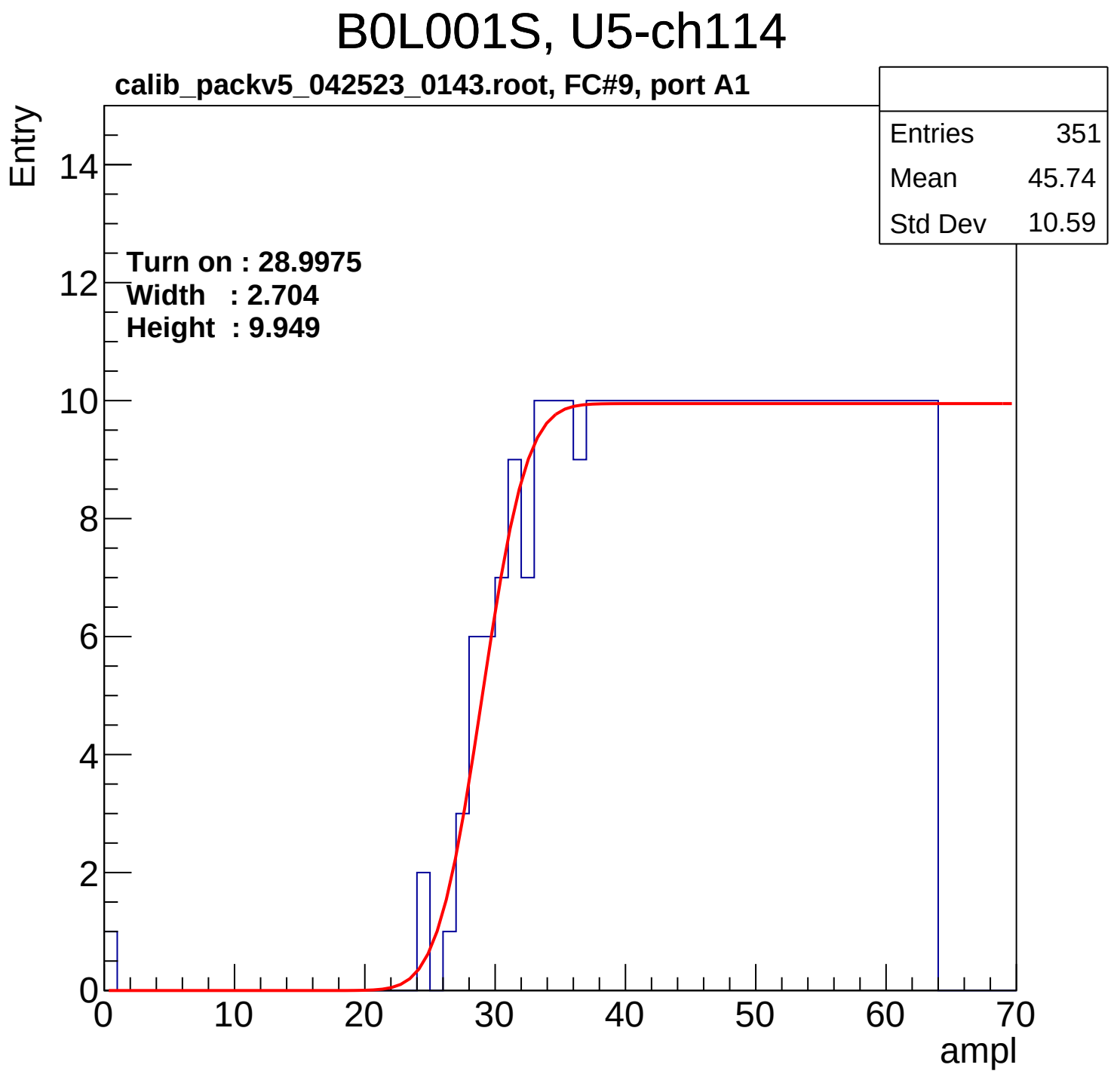
B0L001S, U5-ch114
calib_packv5_042523_0143.root, FC#9, port A1
Entries 351
Mean 45.74
Std Dev 10.59
Turn on : 28.9975
Width : 2.704
Height : 9.949
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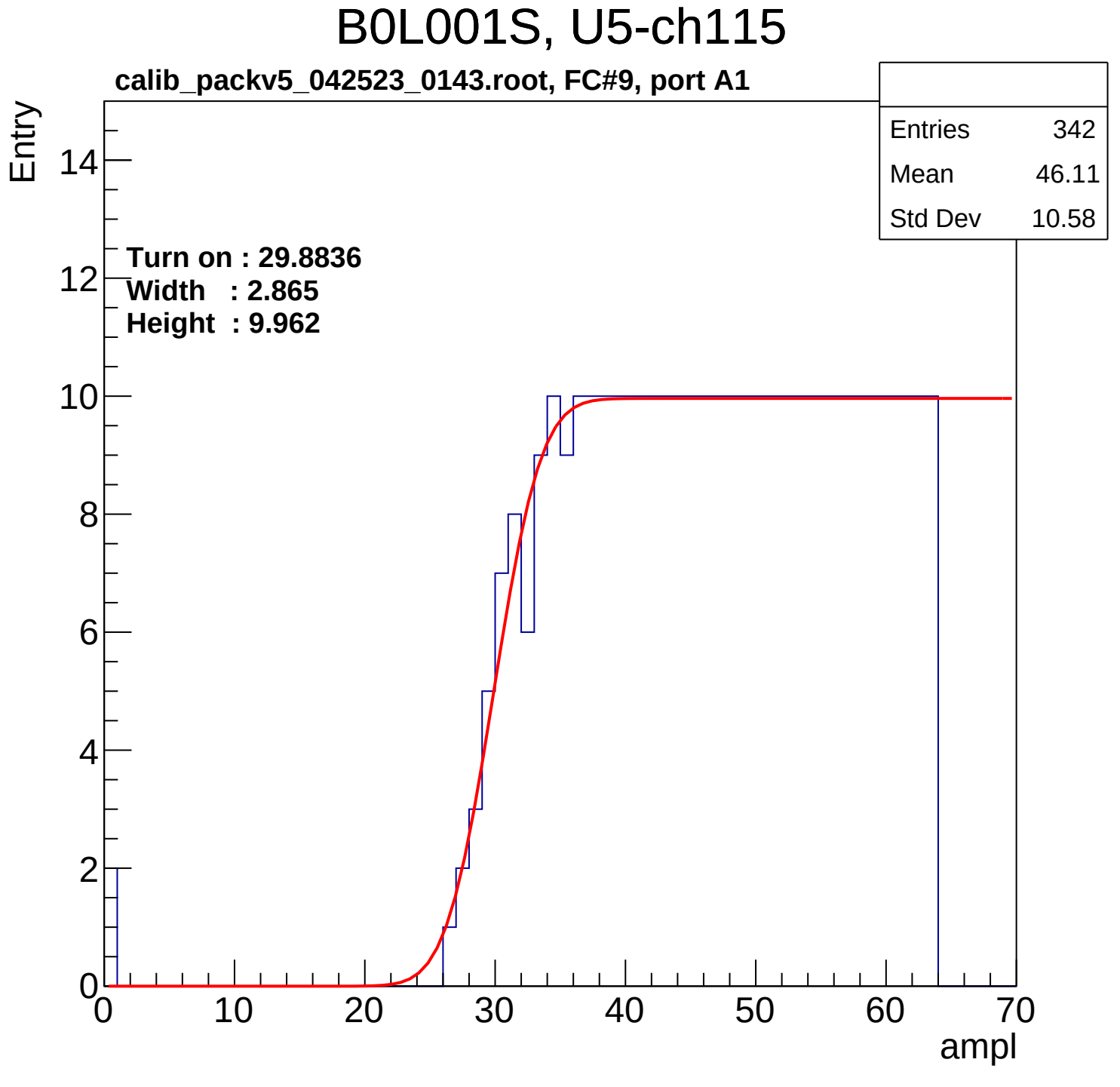
B0L001S, U5-ch115
calib_packv5_042523_0143.root, FC#9, port A1
Entries 342
Mean 46.11
Std Dev 10.58
Turn on : 29.8836
Width : 2.865
Height : 9.962
Entry
ampl
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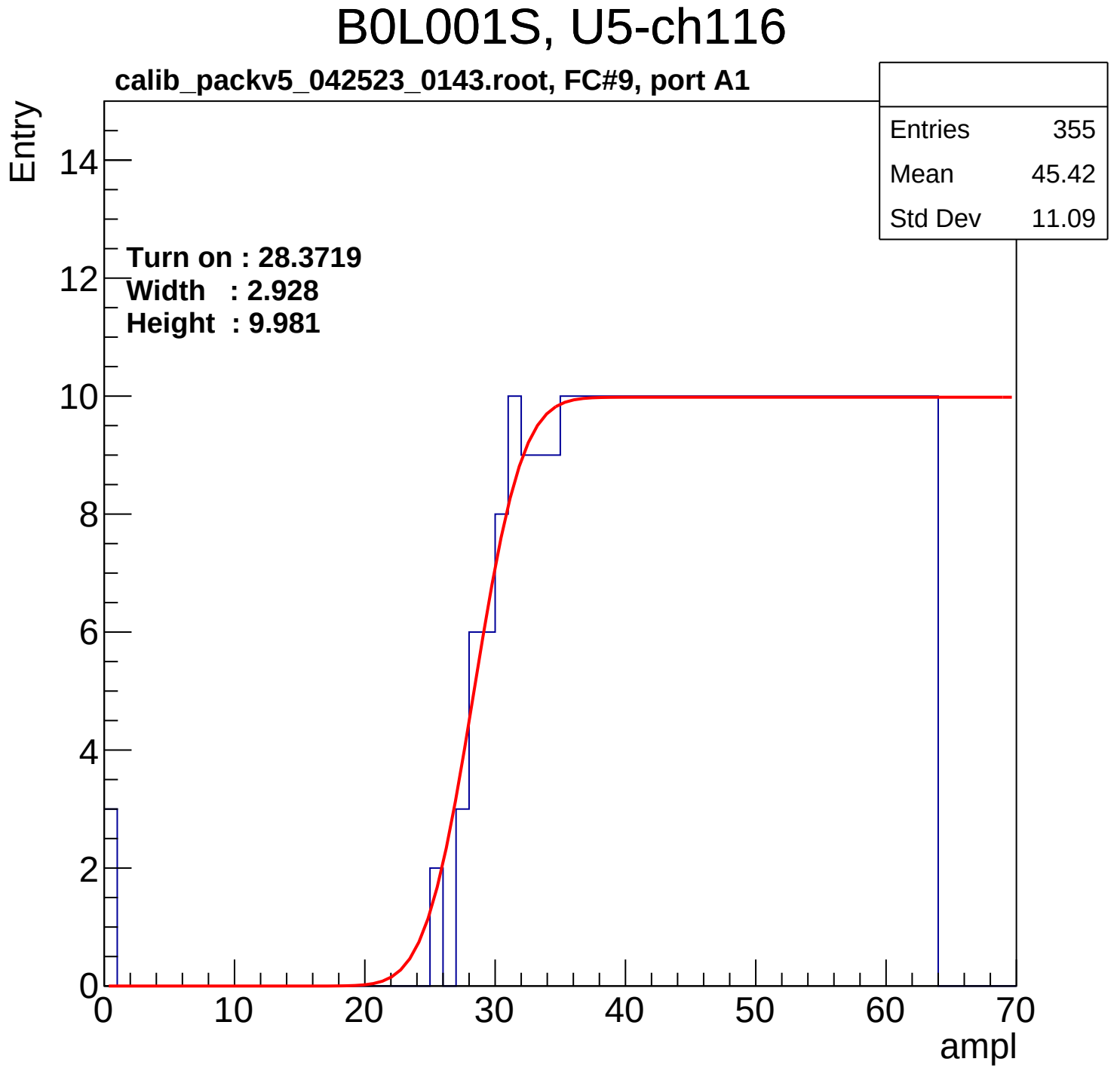
B0L001S, U5-ch116
calib_packv5_042523_0143.root, FC#9, port A1
Entries 355
Mean 45.42
Std Dev 11.09
Turn on : 28.3719
Width : 2.928
Height : 9.981
Entry
ampl
0
2
4
6
8
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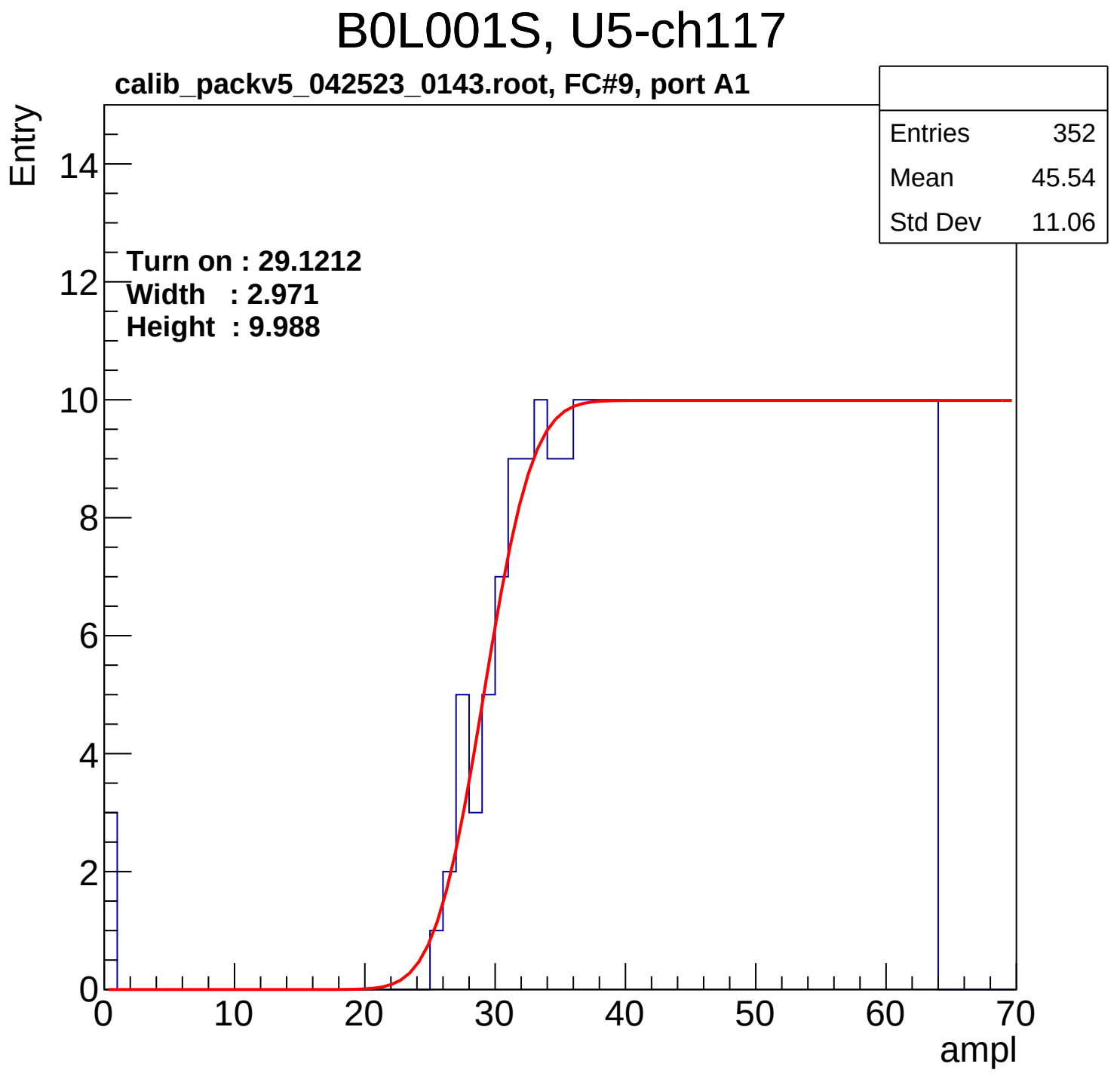
B0L001S, U5-ch117
calib_packv5_042523_0143.root, FC#9, port A1
Entries 352
Mean 45.54
Std Dev 11.06
Turn on : 29.1212
Width : 2.971
Height : 9.988
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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60
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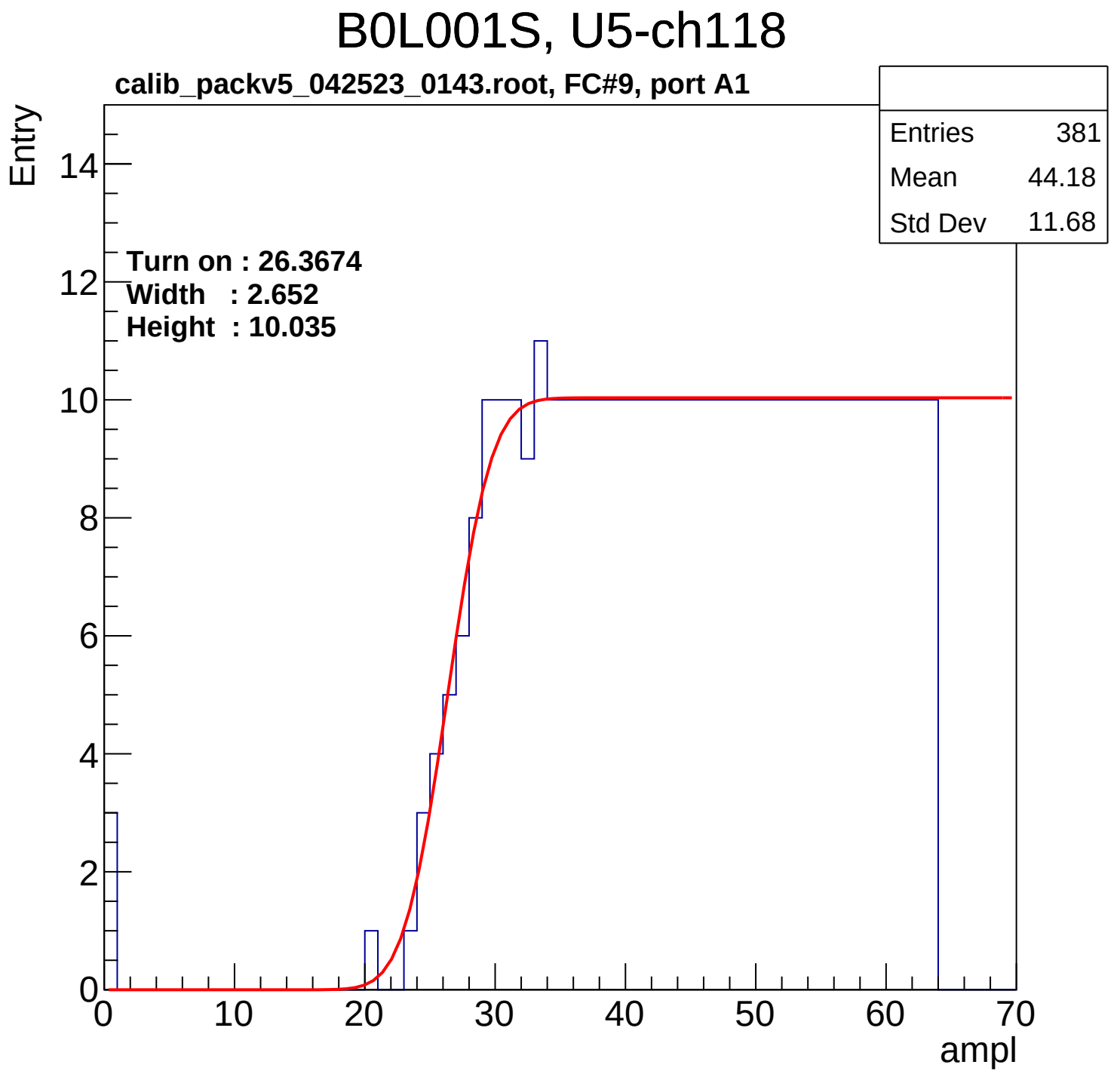
B0L001S, U5-ch118
calib_packv5_042523_0143.root, FC#9, port A1
Entries 381
Mean 44.18
Std Dev 11.68
Turn on : 26.3674
Width : 2.652
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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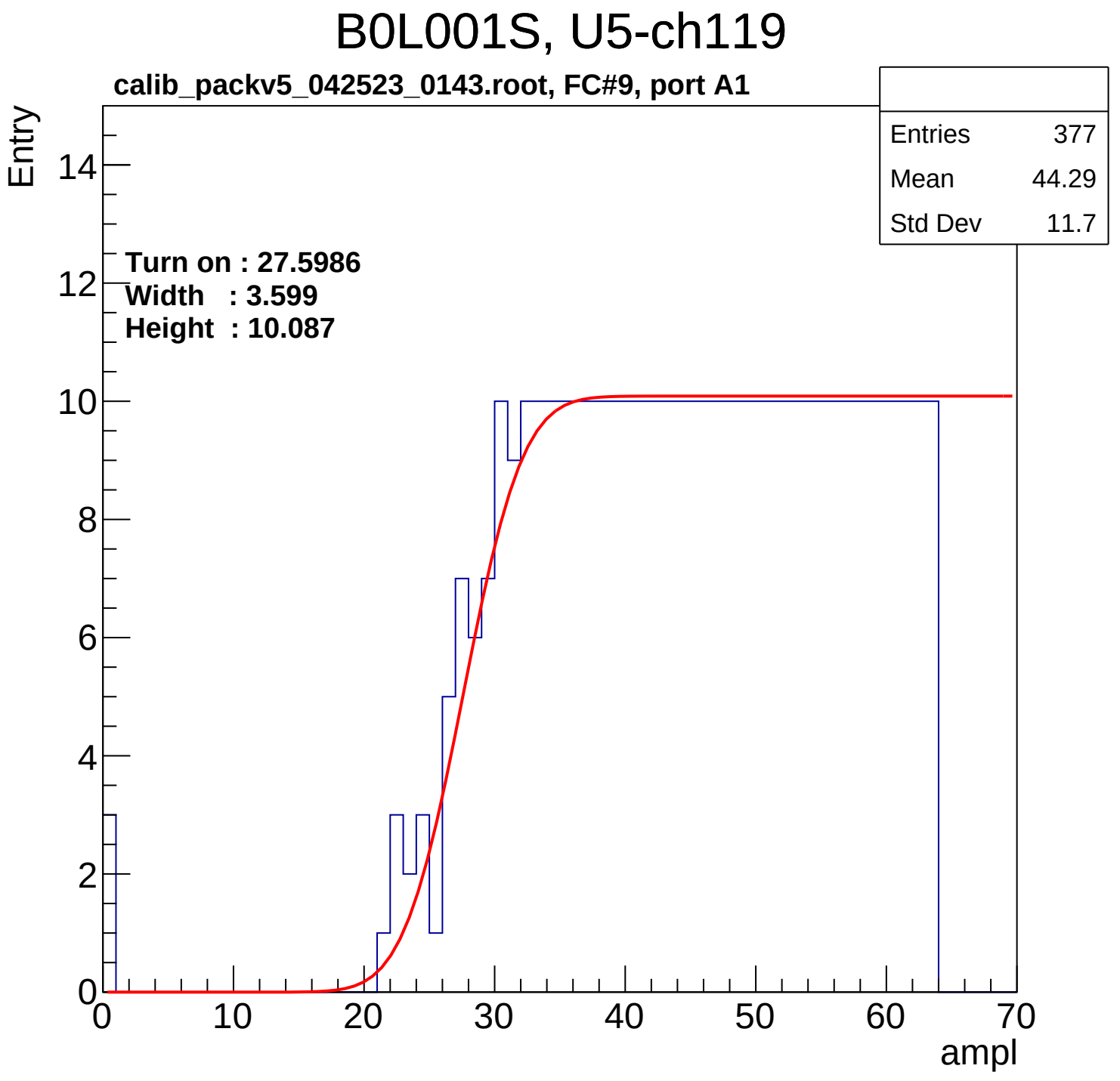
B0L001S, U5-ch119
calib_packv5_042523_0143.root, FC#9, port A1
Entries 377
Mean 44.29
Std Dev 11.7
Turn on : 27.5986
Width : 3.599
Height : 10.087
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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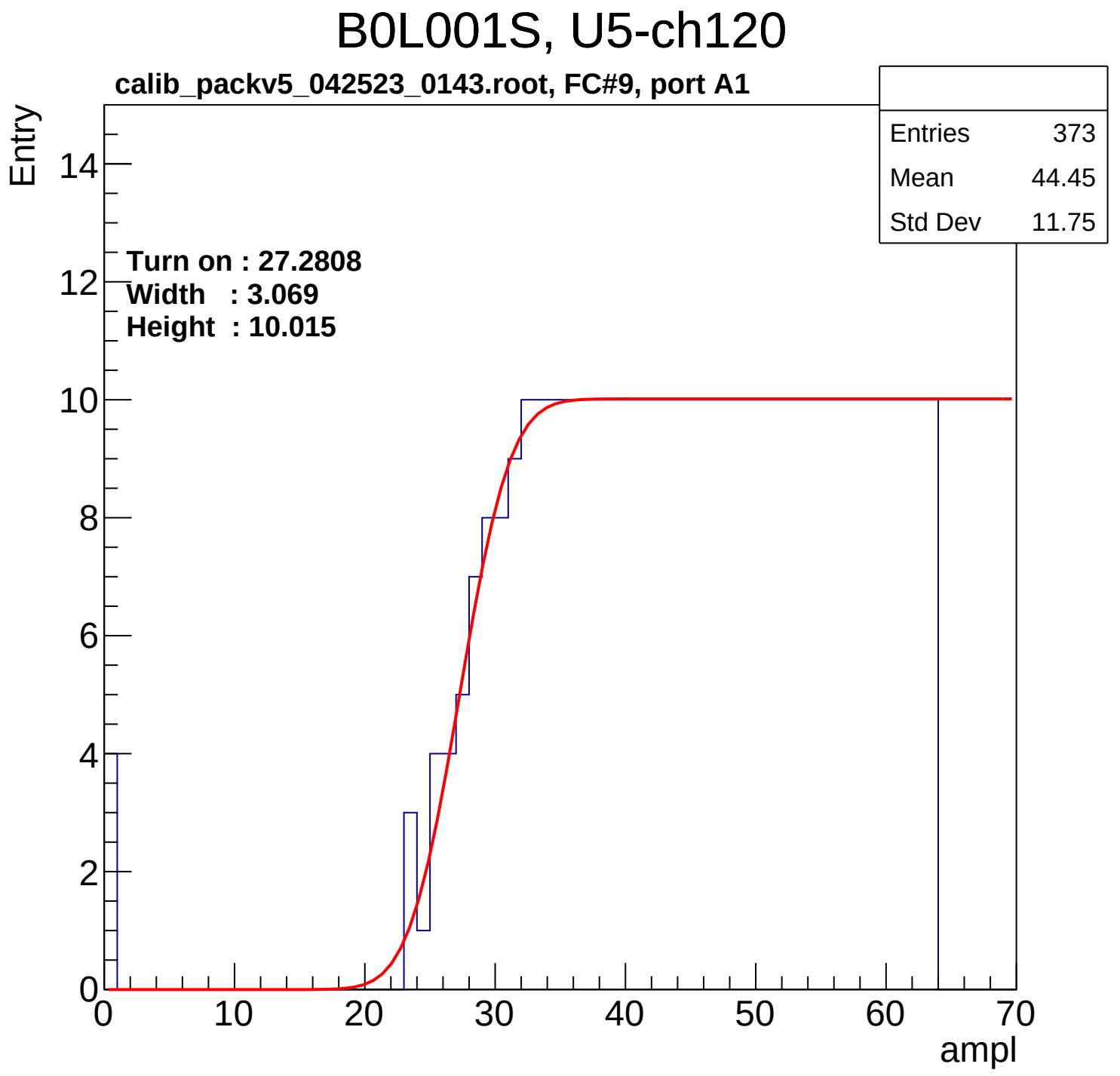
B0L001S, U5-ch120
calib_packv5_042523_0143.root, FC#9, port A1
Entries 373
Mean 44.45
Std Dev 11.75
Turn on : 27.2808
Width : 3.069
Height : 10.015
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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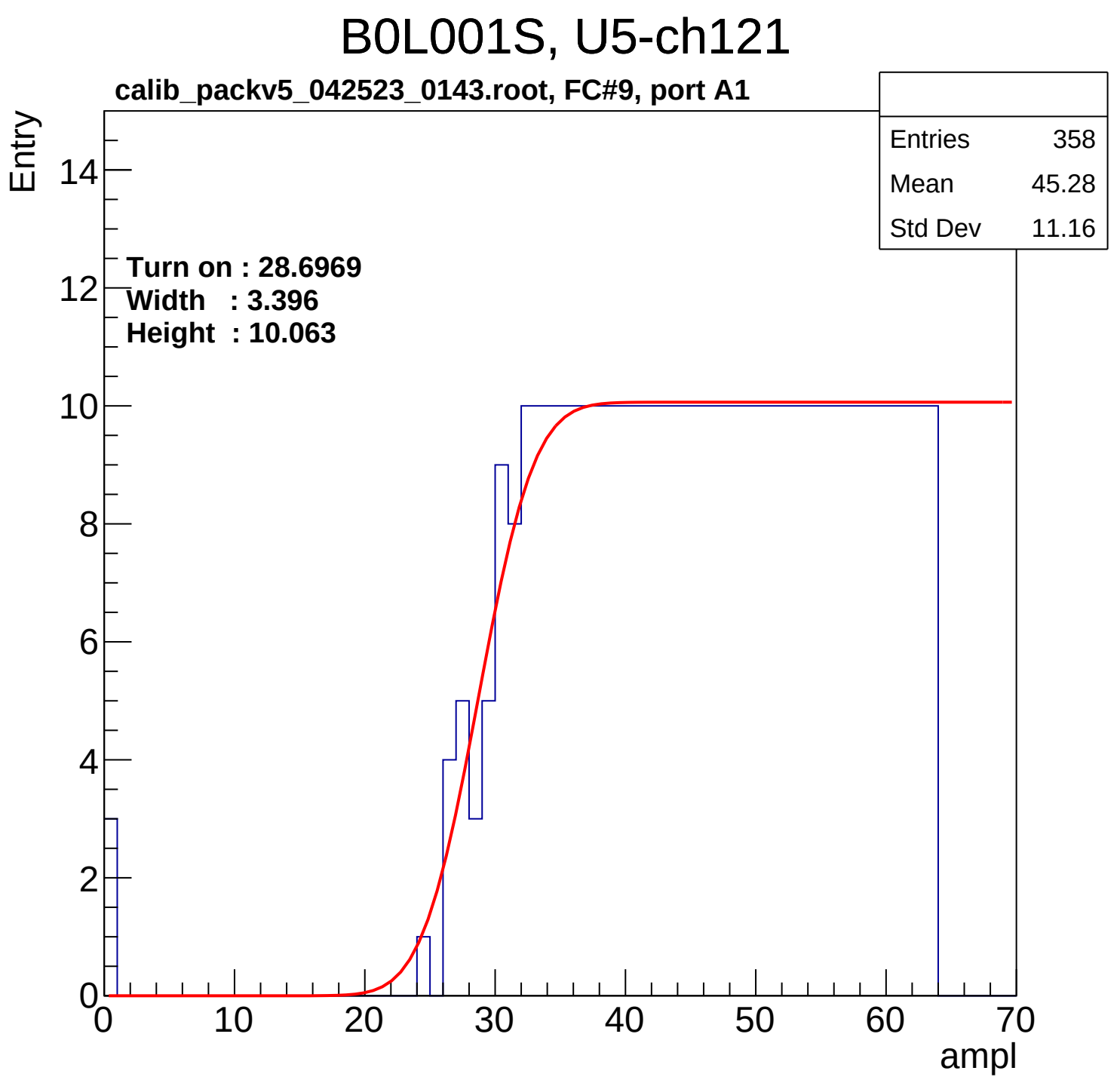
B0L001S, U5-ch121
calib_packv5_042523_0143.root, FC#9, port A1
Entries 358
Mean 45.28
Std Dev 11.16
Turn on : 28.6969
Width : 3.396
Height : 10.063
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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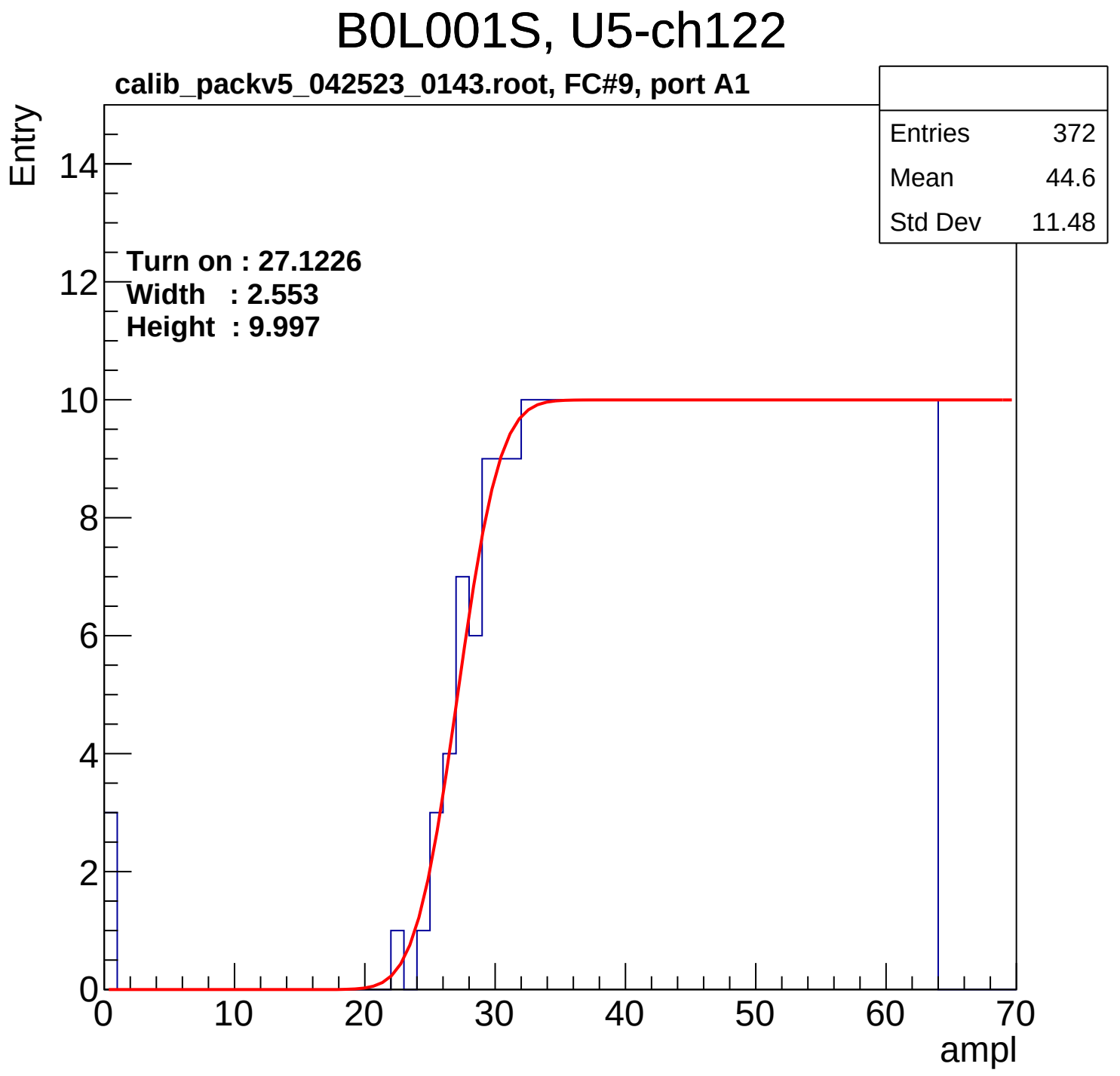
B0L001S, U5-ch122
calib_packv5_042523_0143.root, FC#9, port A1
Entries 372
Mean 44.6
Std Dev 11.48
Turn on : 27.1226
Width : 2.553
Height : 9.997
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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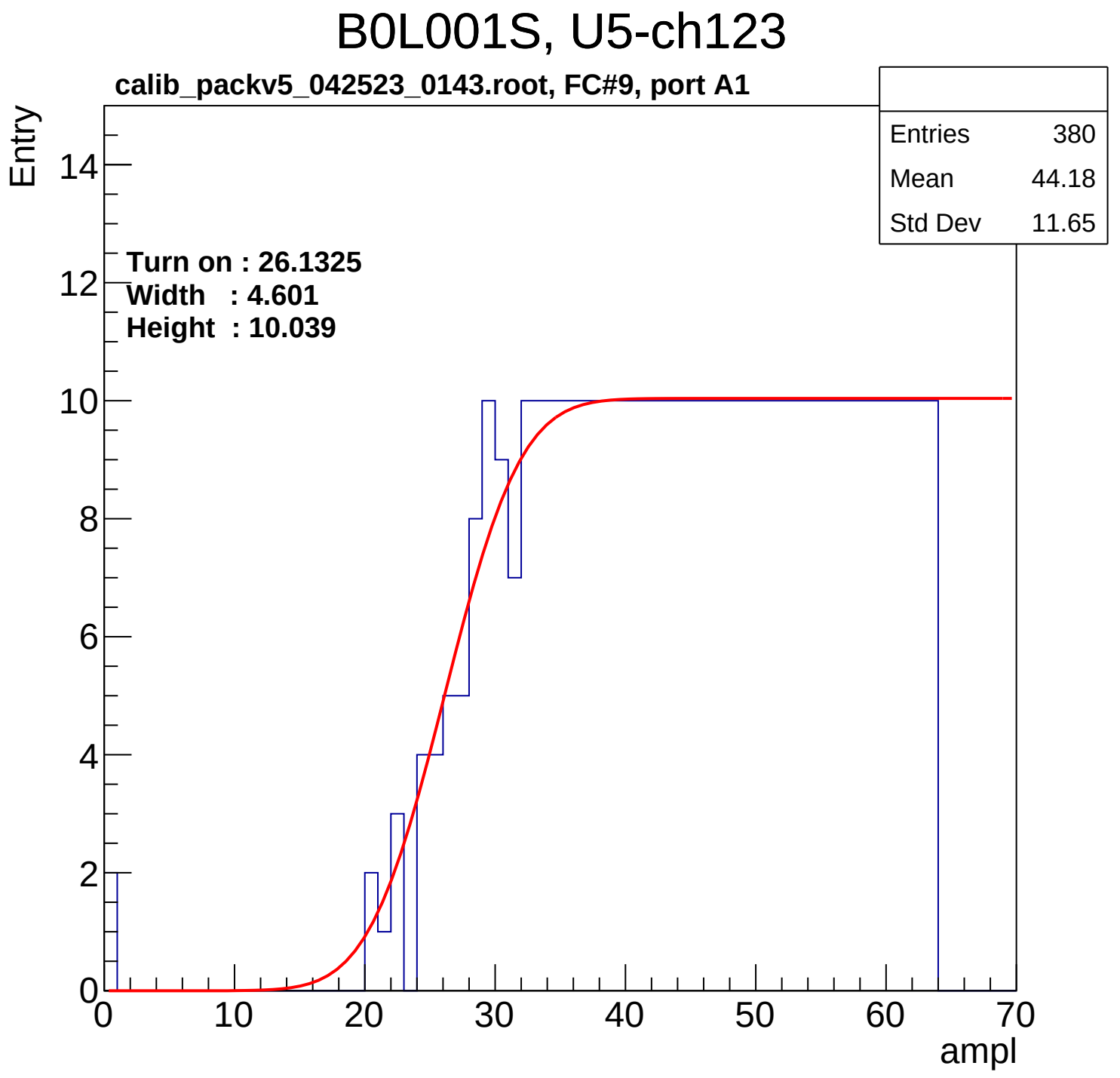
B0L001S, U5-ch123
calib_packv5_042523_0143.root, FC#9, port A1
Entries 380
Mean 44.18
Std Dev 11.65
Turn on : 26.1325
Width : 4.601
Height : 10.039
Entry
ampl
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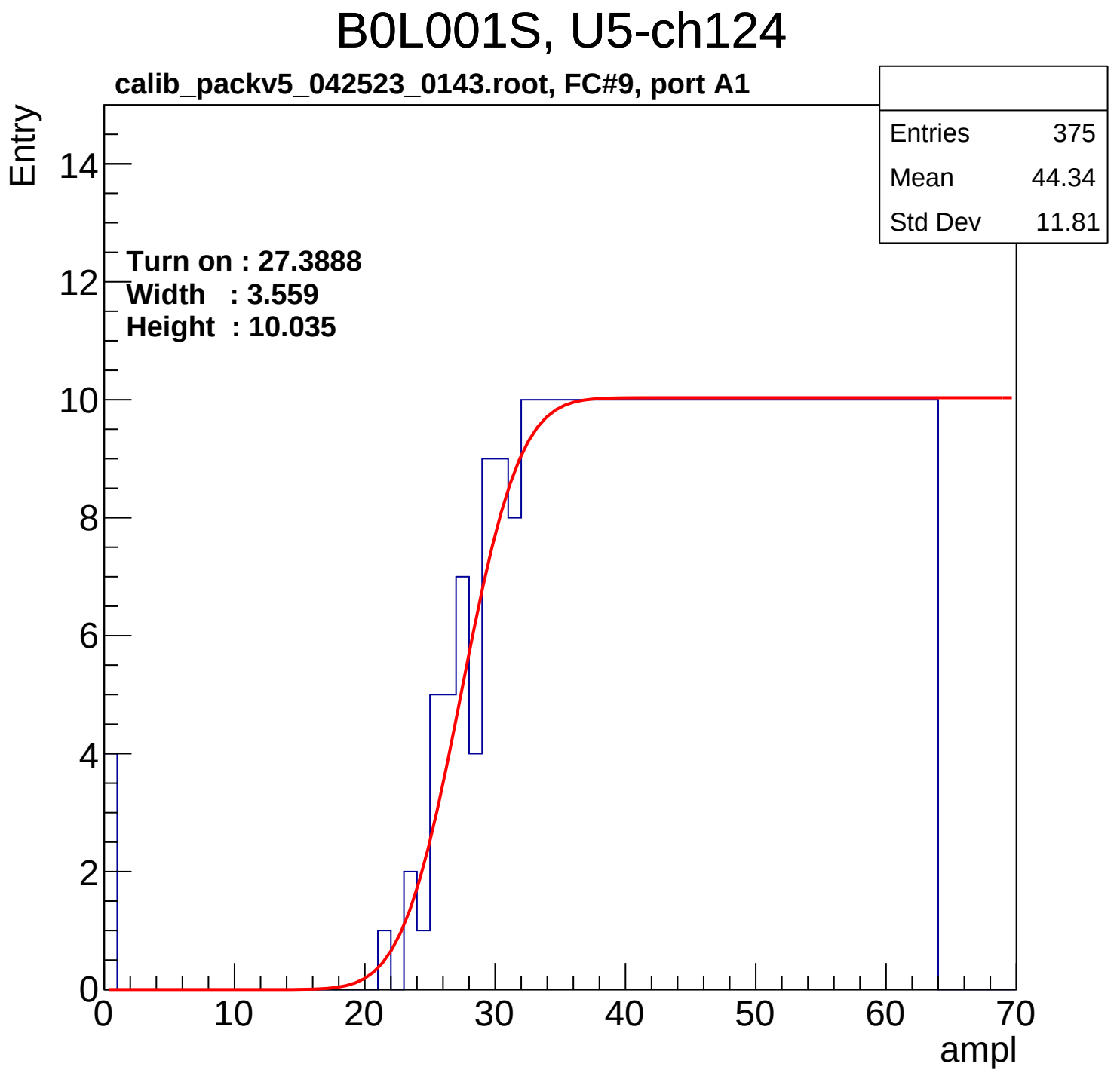
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U5-ch124
calib_packv5_042523_0143.root, FC#9, port A1
Entries 375
Mean 44.34
Std Dev 11.81
Turn on : 27.3888
Width : 3.559
Height : 10.035
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
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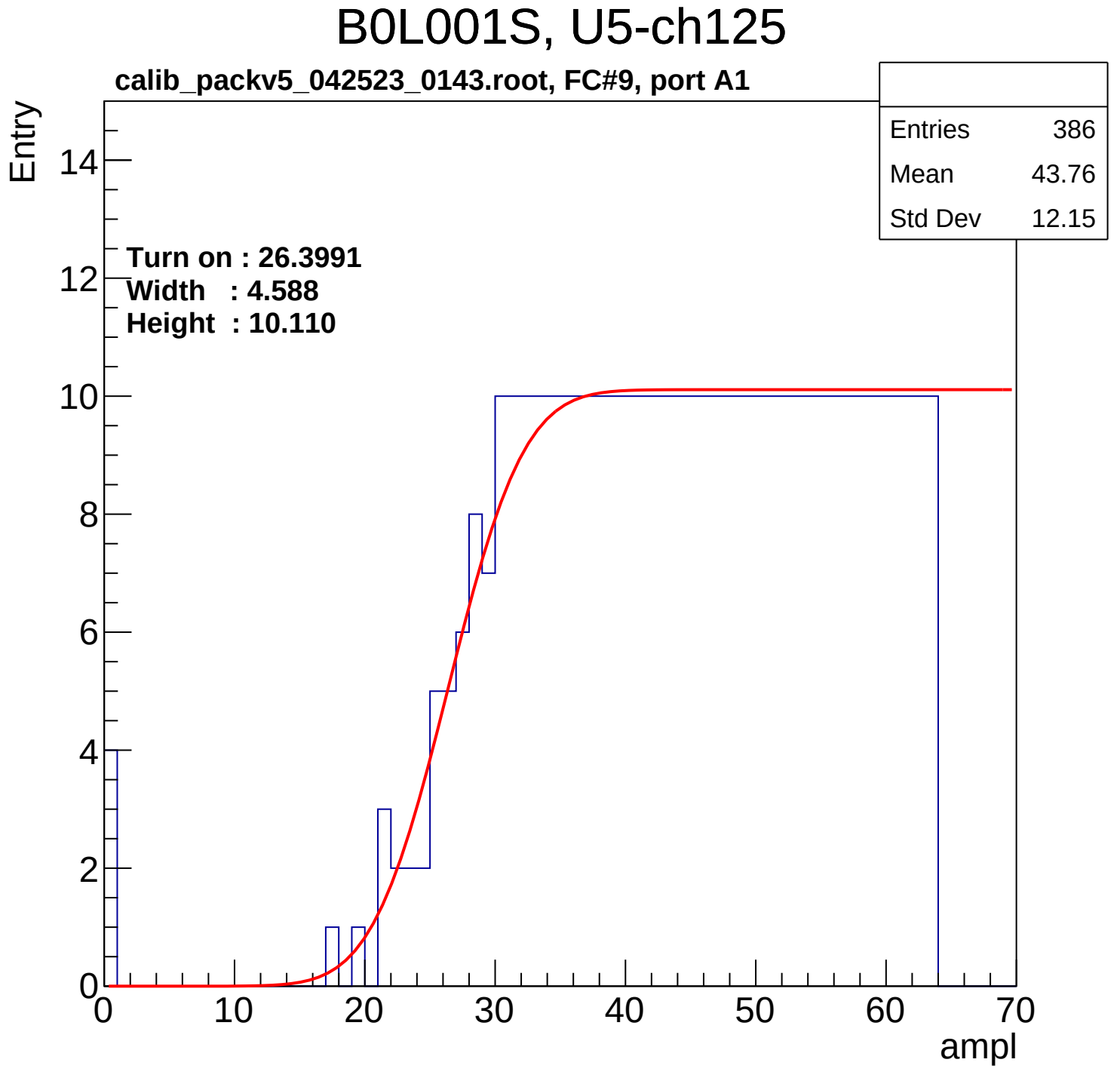
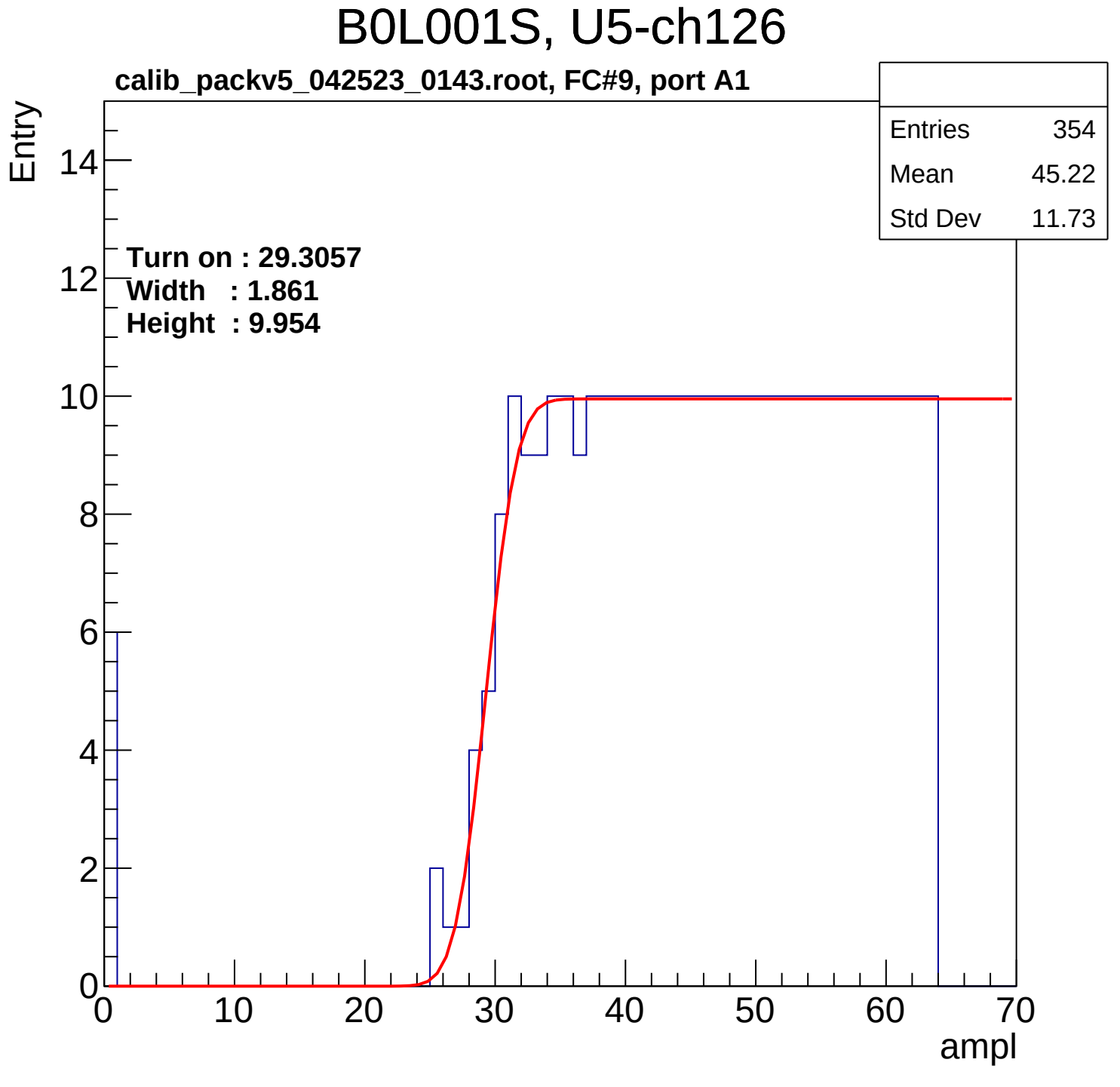
60
70


B0L001S, U5-ch125
calib_packv5_042523_0143.root, FC#9, port A1
Entries 386
Mean 43.76
Std Dev 12.15
Turn on : 26.3991
Width : 4.588
Height : 10.110
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U5-ch126
calib_packv5_042523_0143.root, FC#9, port A1
Entries 354
Mean 45.22
Std Dev 11.73
Turn on : 29.3057
Width : 1.861
Height : 9.954
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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40
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60
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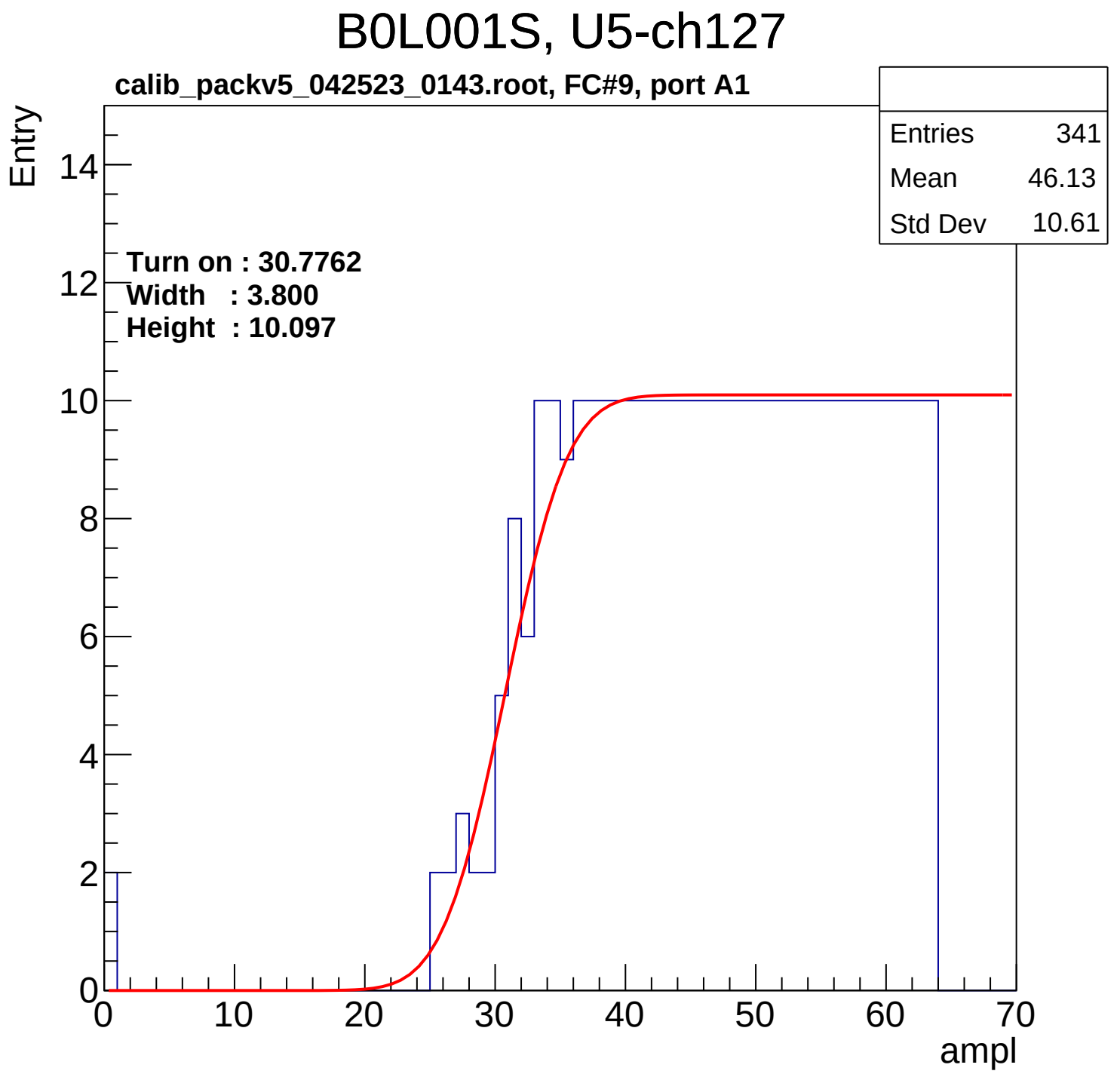
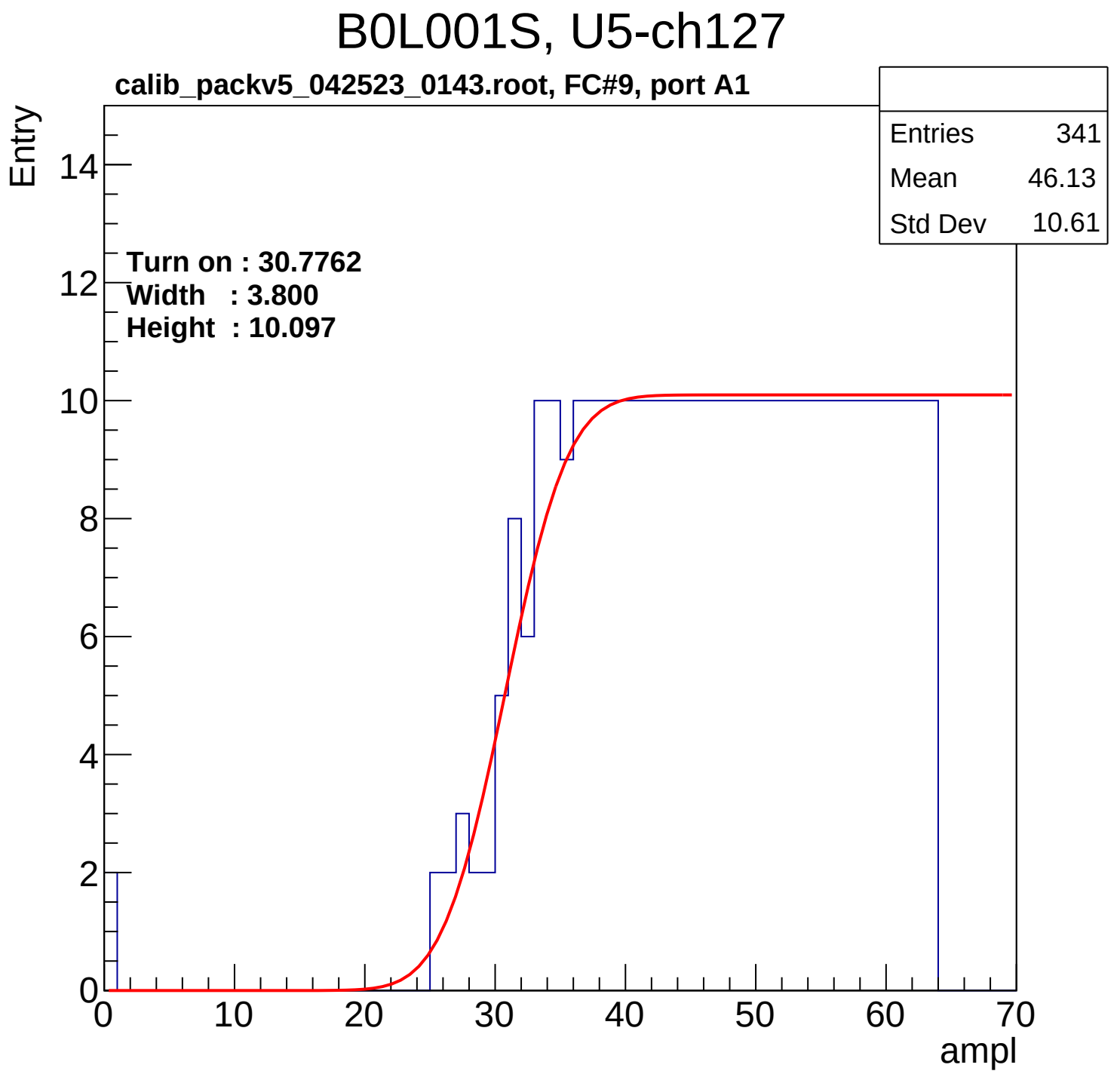

B0L001S, U5-ch127
calib_packv5_042523_0143.root, FC#9, port A1
Entries 341
Mean 46.13
Std Dev 10.61
Turn on : 30.7762
Width : 3.800
Height : 10.097
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L001S, U5-ch127
calib_packv5_042523_0143.root, FC#9, port A1
Entries 341
Mean 46.13
Std Dev 10.61
Turn on : 30.7762
Width : 3.800
Height : 10.097
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70