



# B1L101S, U9-ch0, adc0

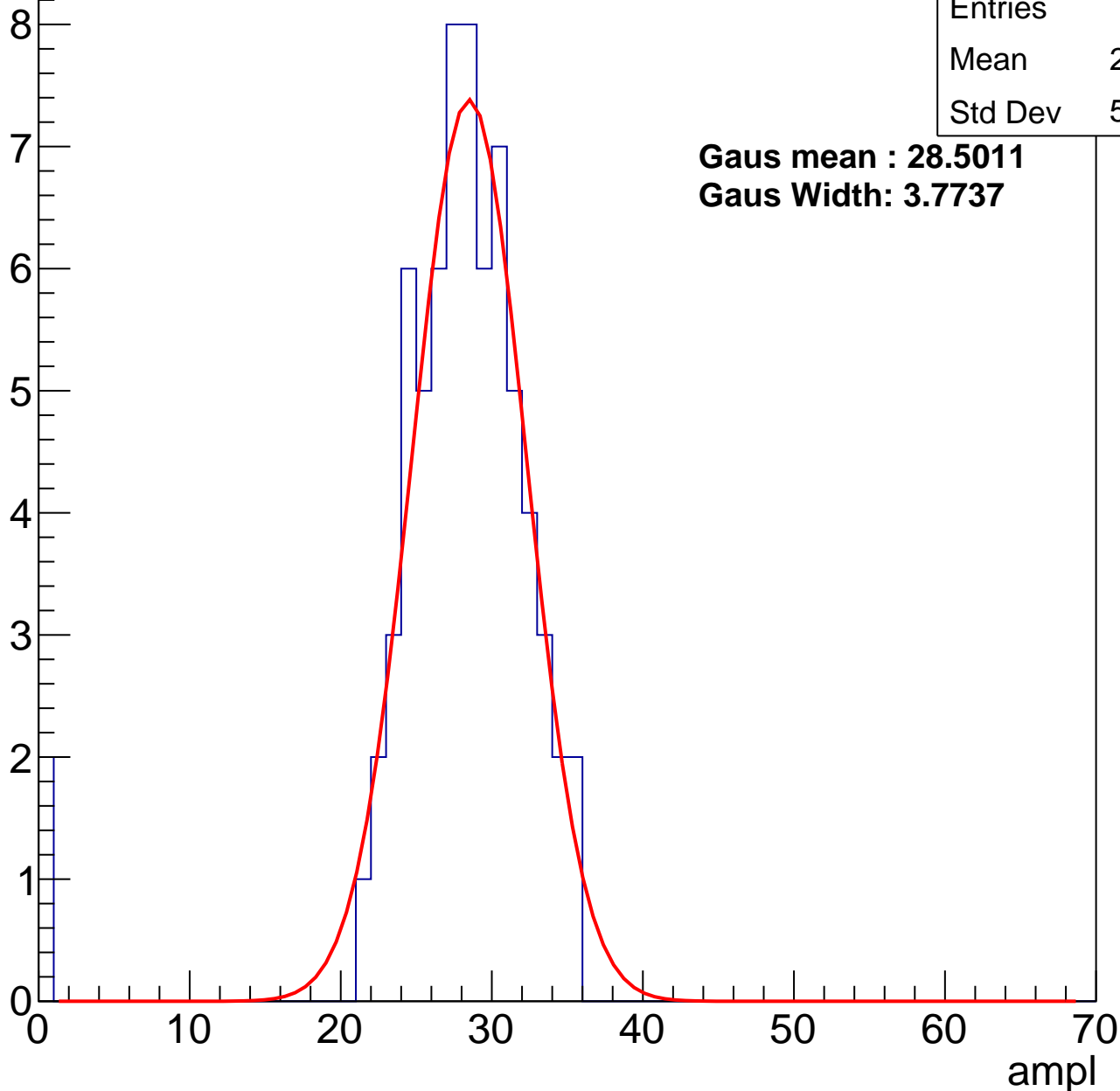
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	27.19
Std Dev	5.705

**Gaus mean : 28.5011**

**Gaus Width: 3.7737**



# B1L101S, U9-ch0, adc1

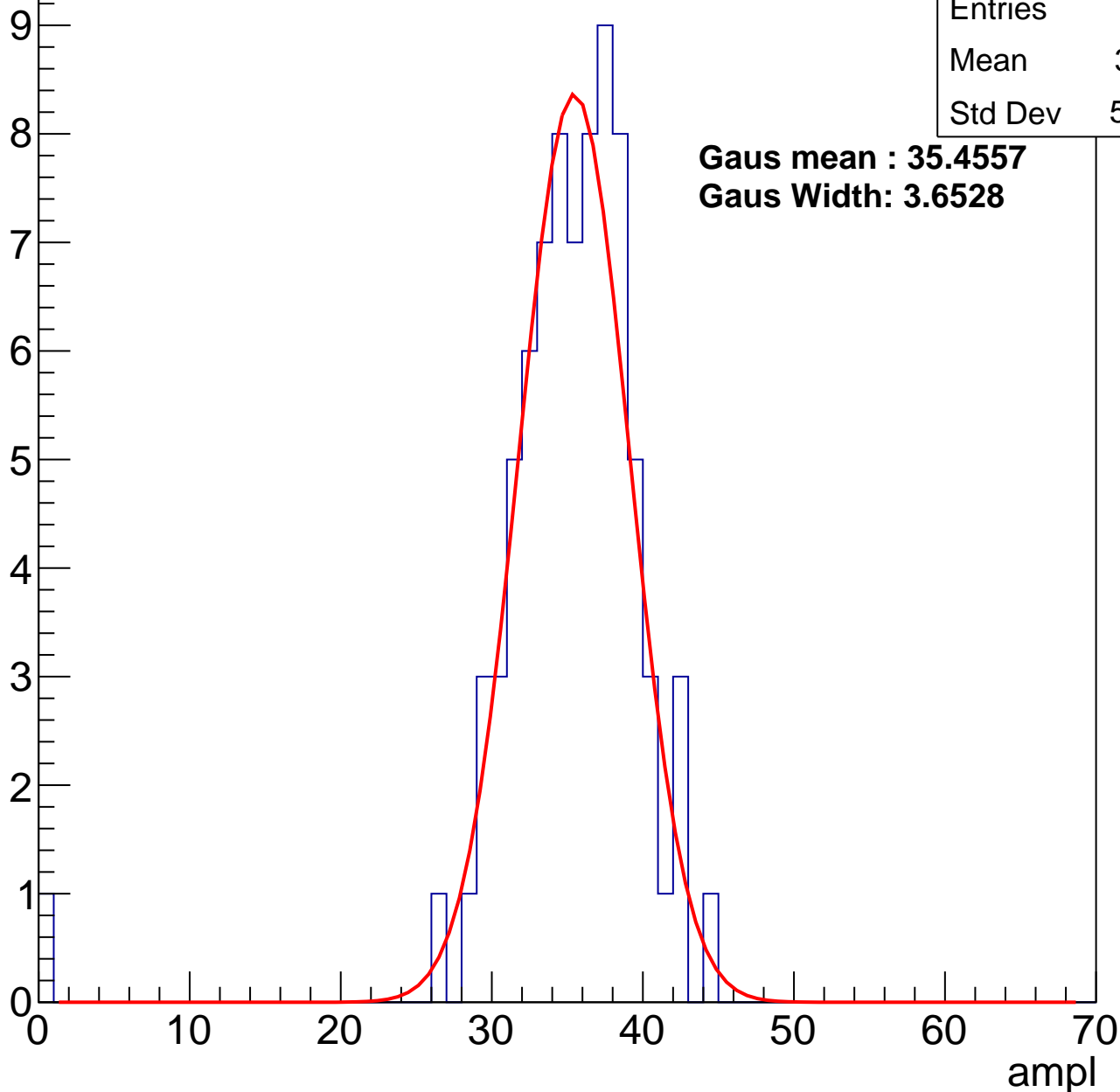
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	34.71
Std Dev	5.287

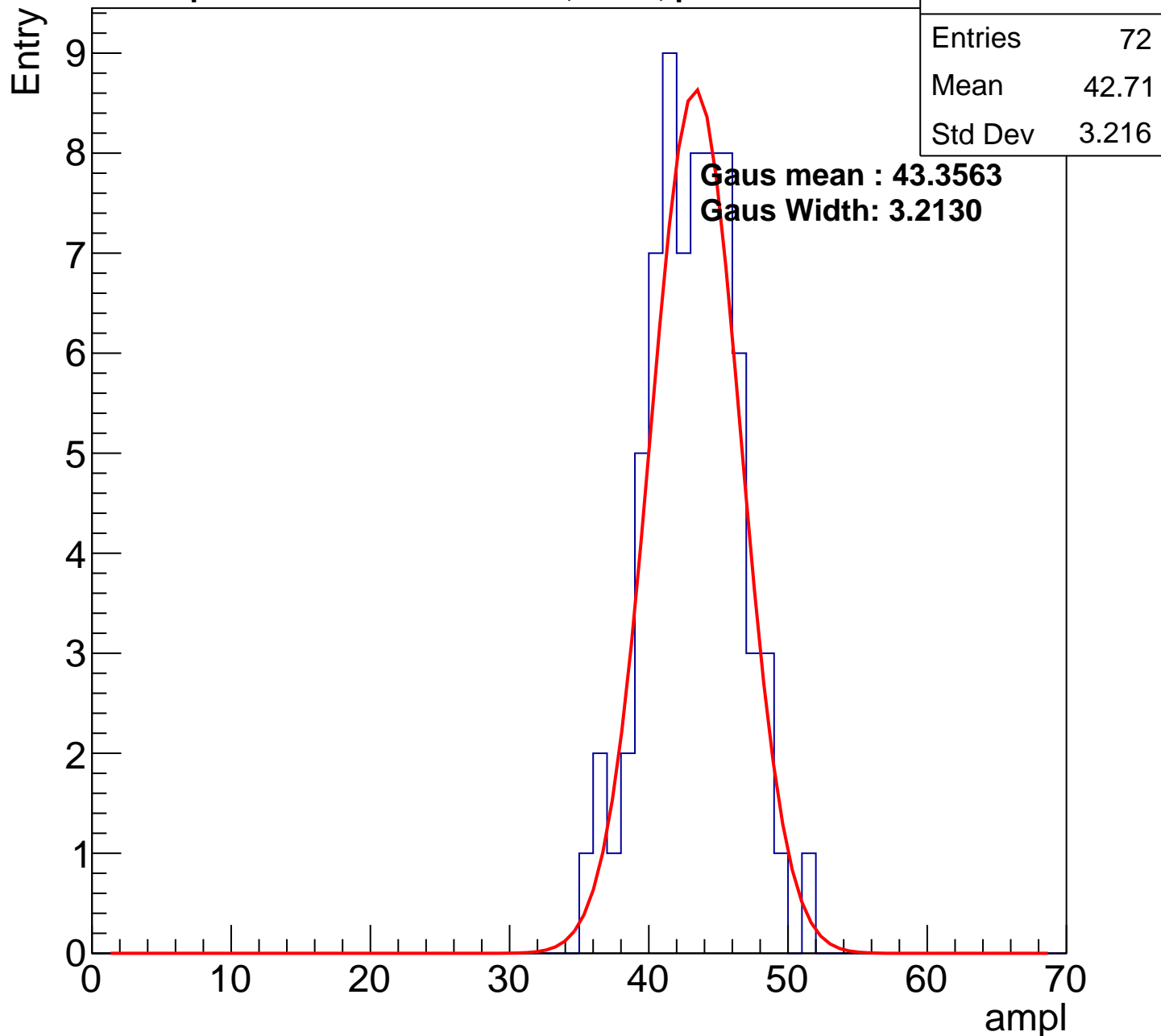
**Gaus mean : 35.4557**

**Gaus Width: 3.6528**



# B1L101S, U9-ch0, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

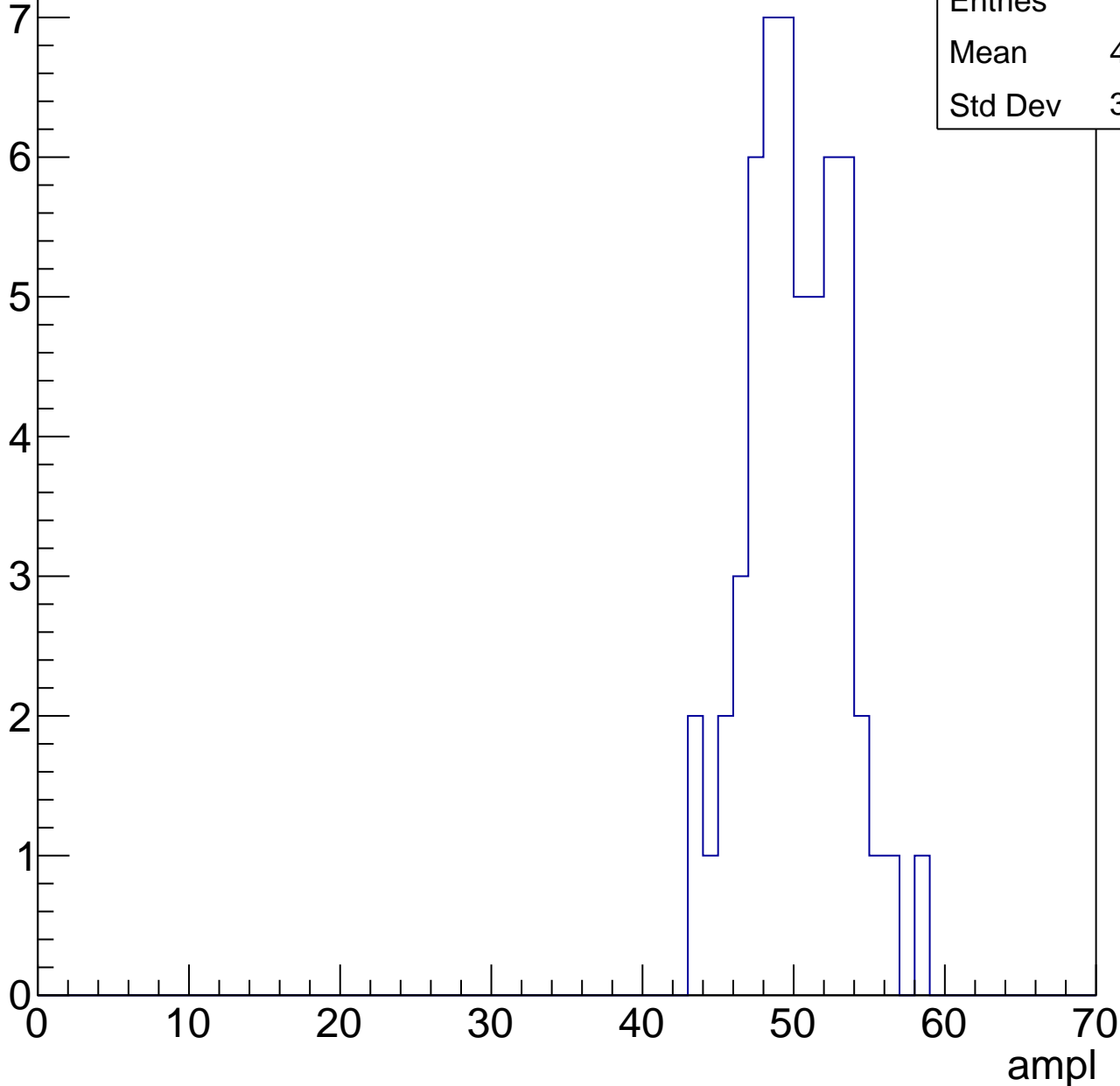


# B1L101S, U9-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

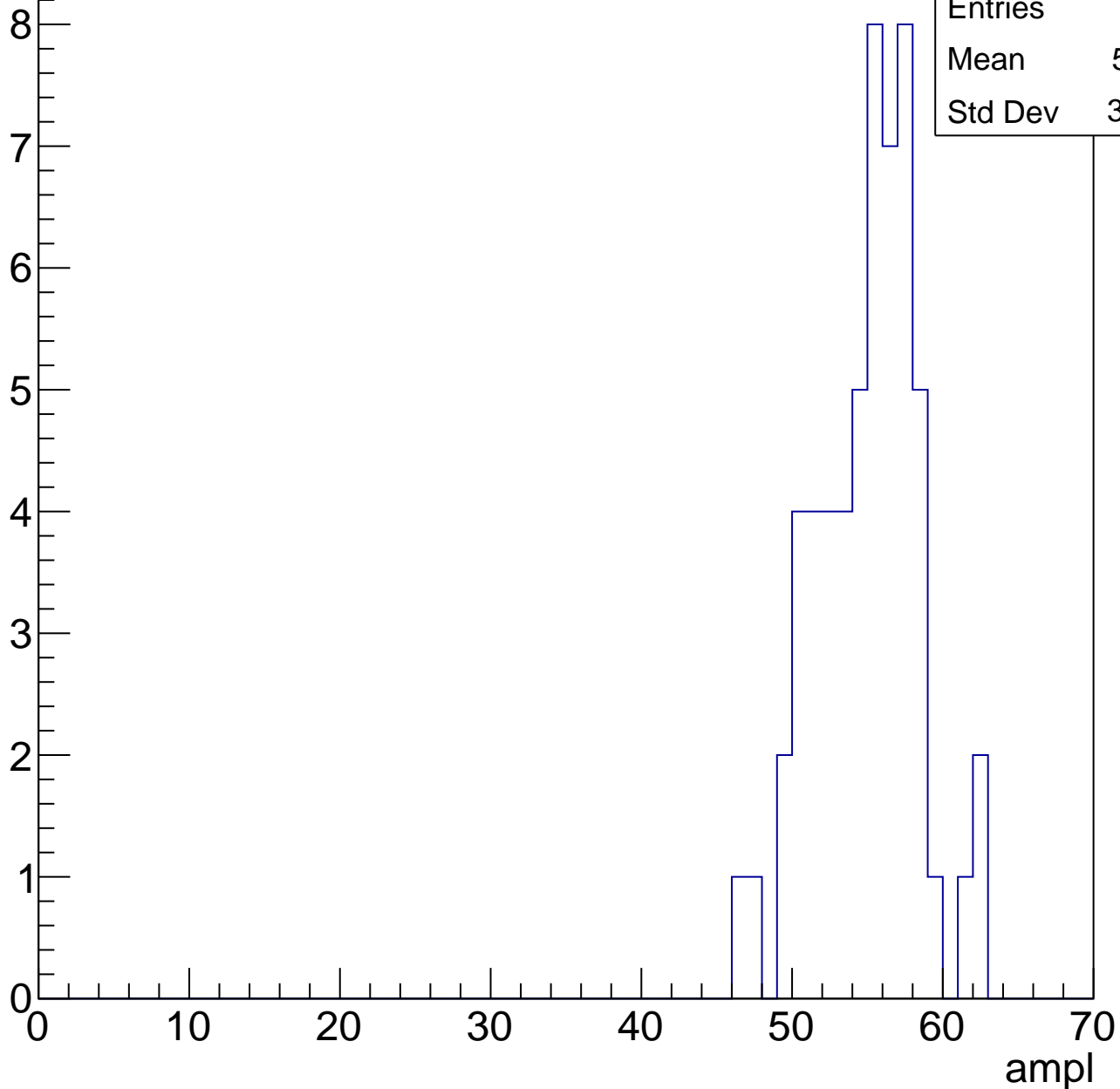
Entries	55
Mean	49.65
Std Dev	3.175



# B1L101S, U9-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

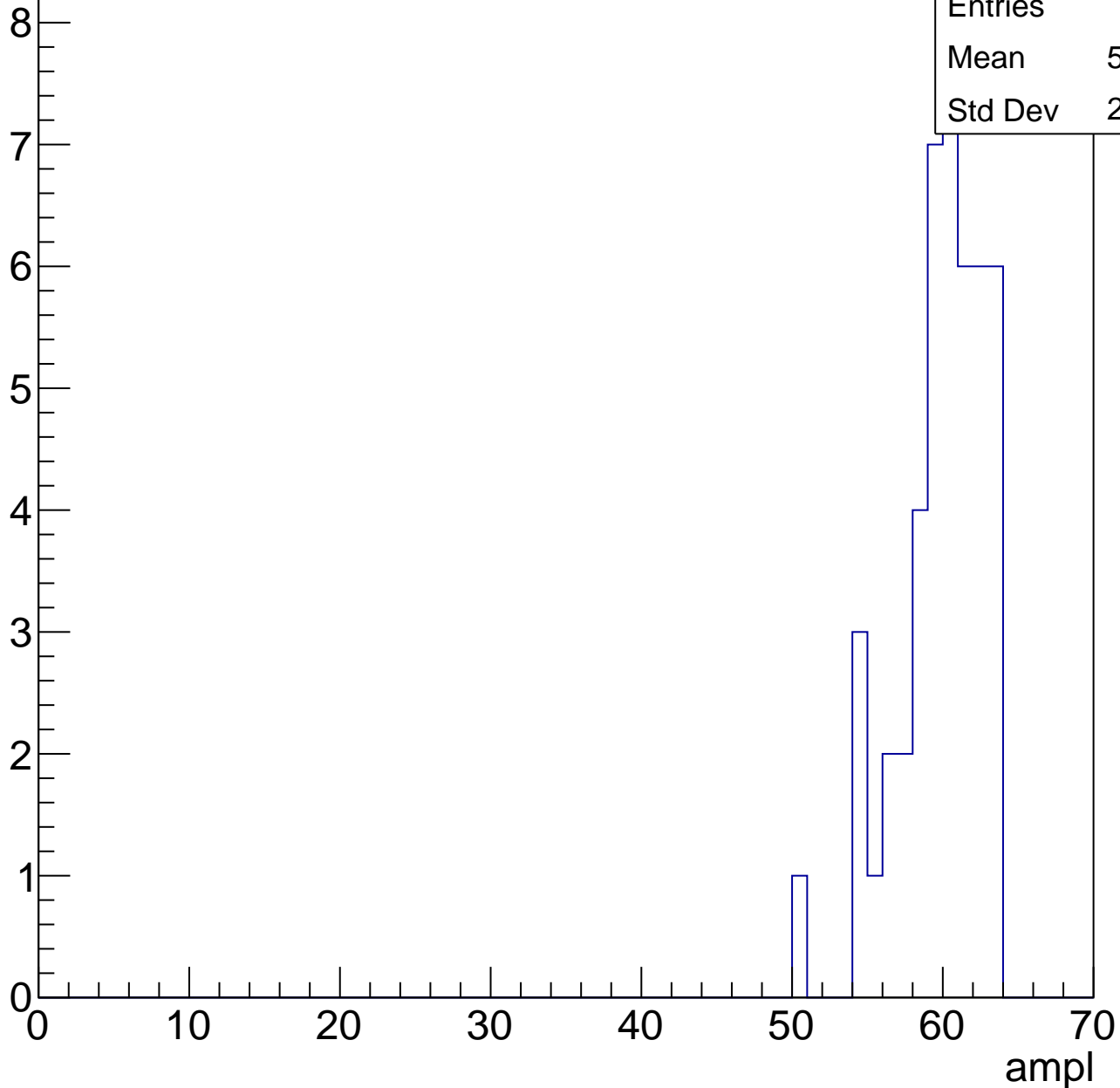
Entry



# B1L101S, U9-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

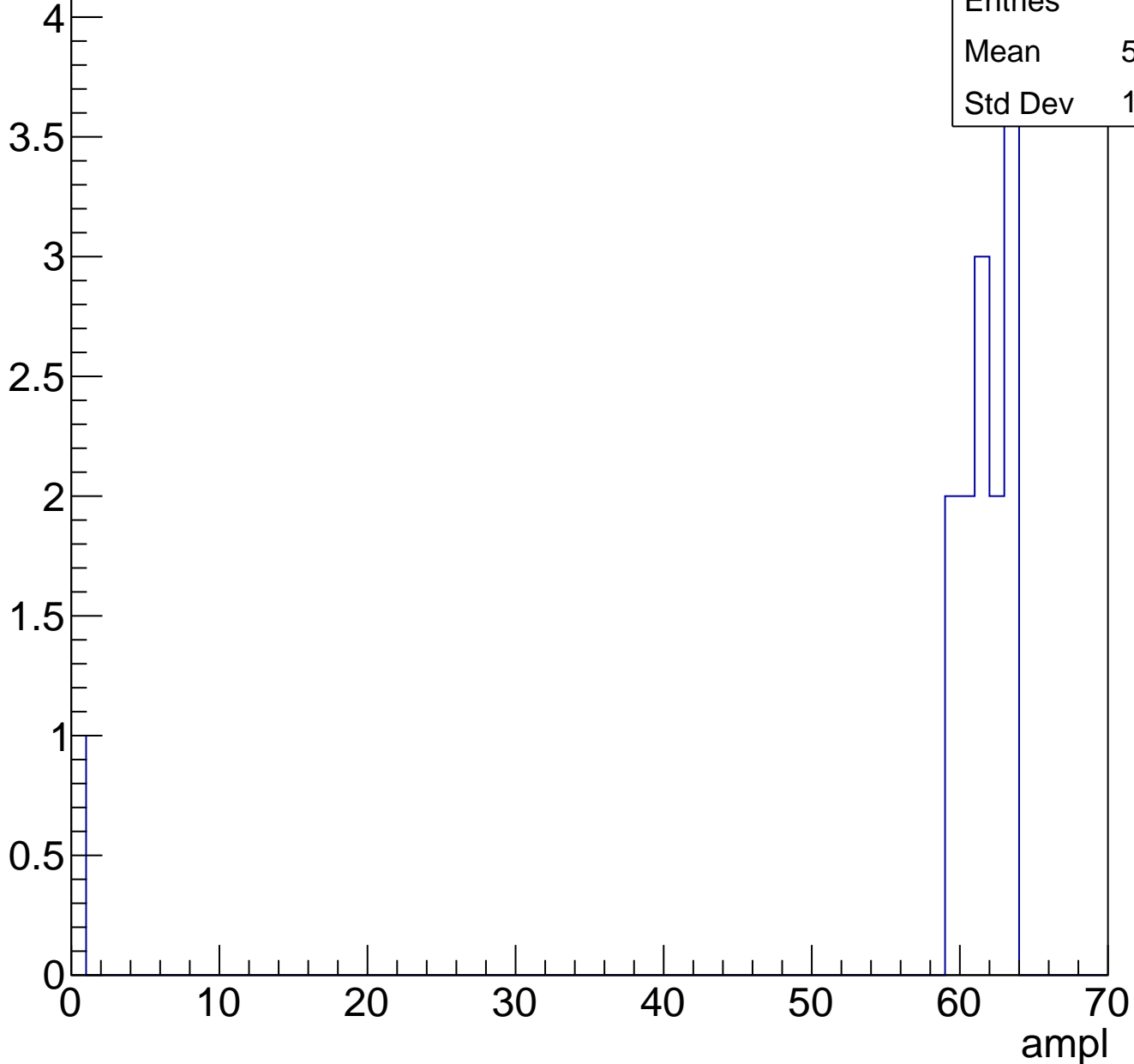
Entry



# B1L101S, U9-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



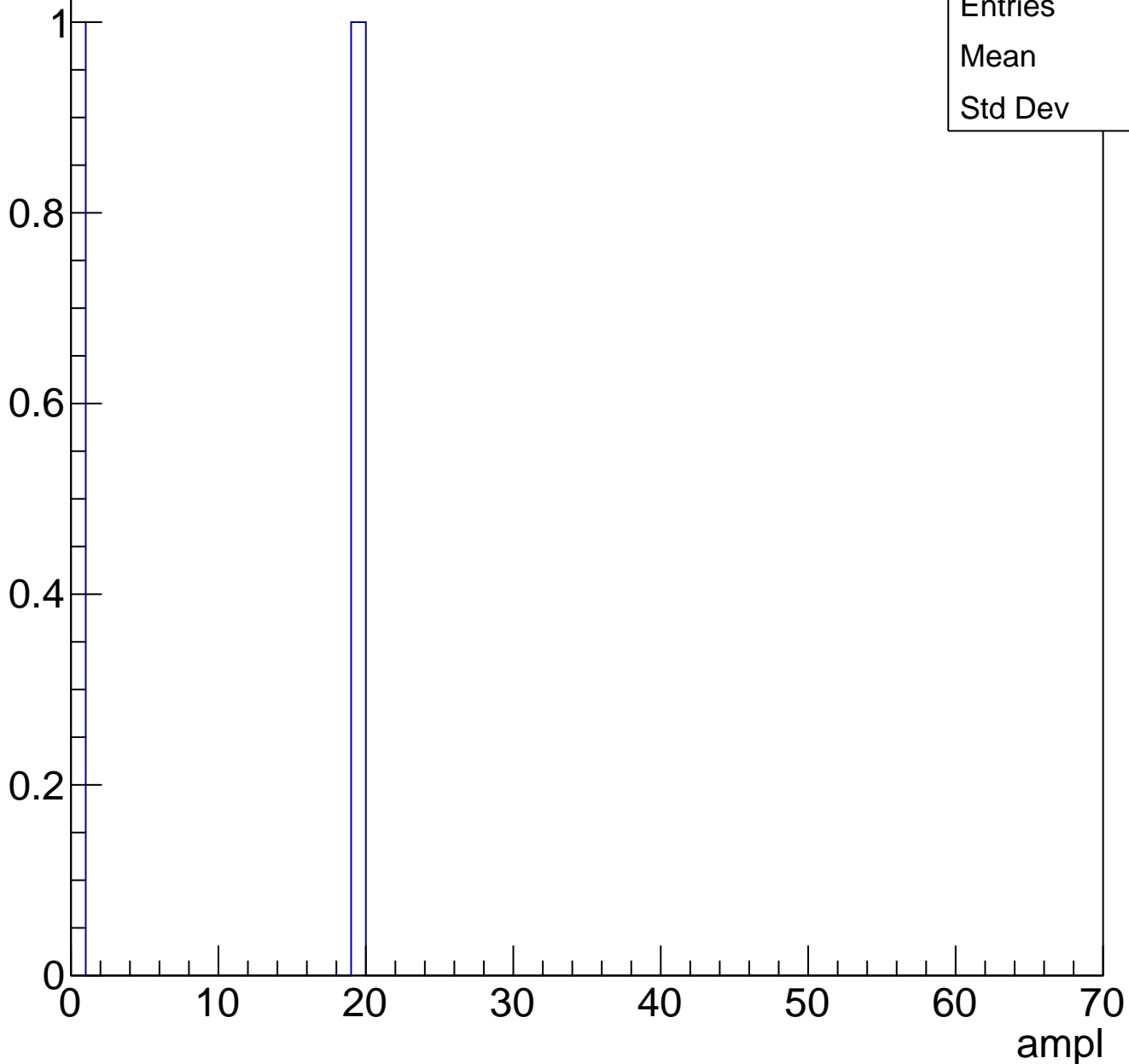
Entries	14
Mean	56.93
Std Dev	15.85



# B1L101S, U9-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch1, adc0

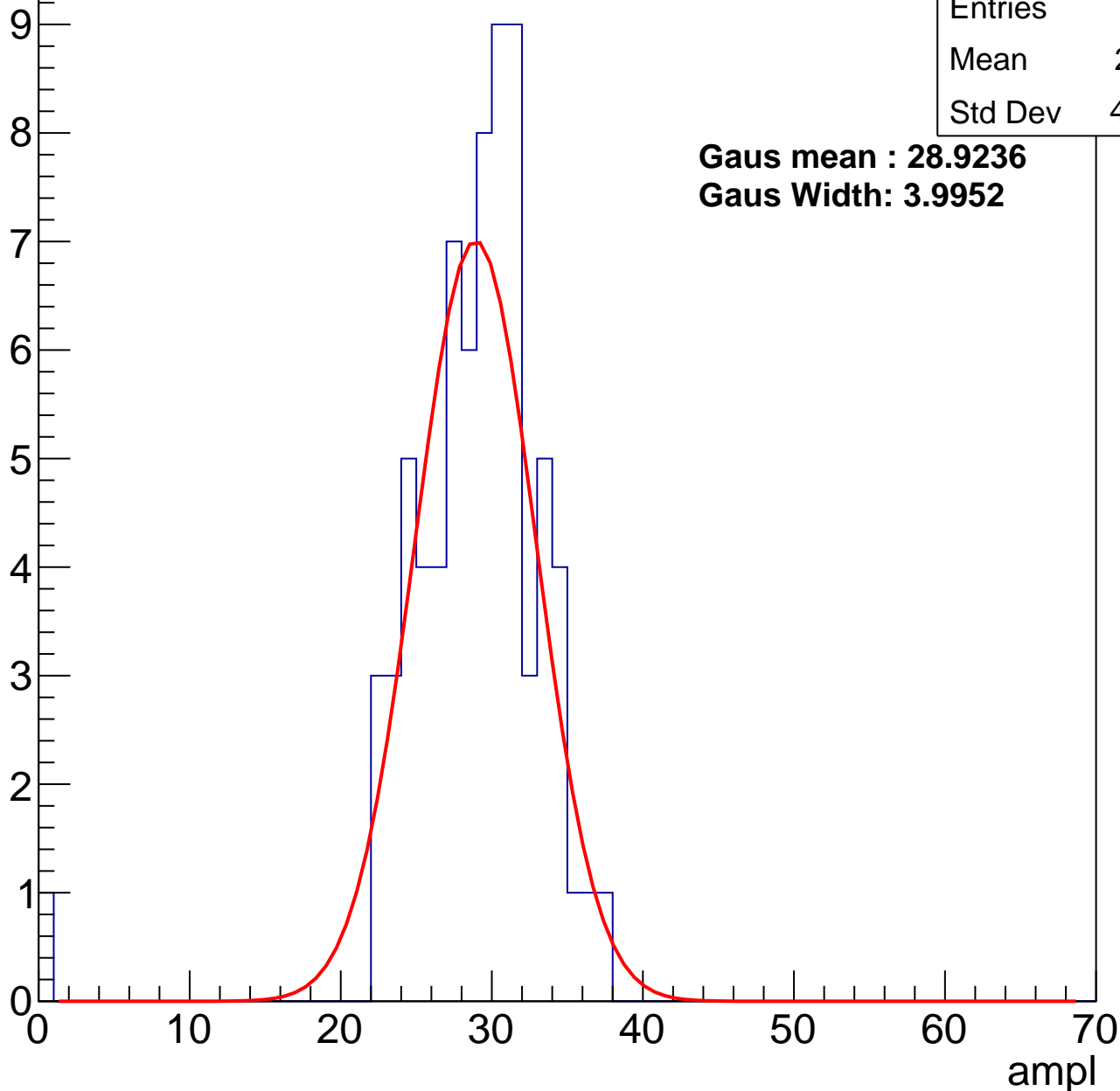
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	28.41
Std Dev	4.835

**Gaus mean : 28.9236**

**Gaus Width: 3.9952**



# B1L101S, U9-ch1, adc1

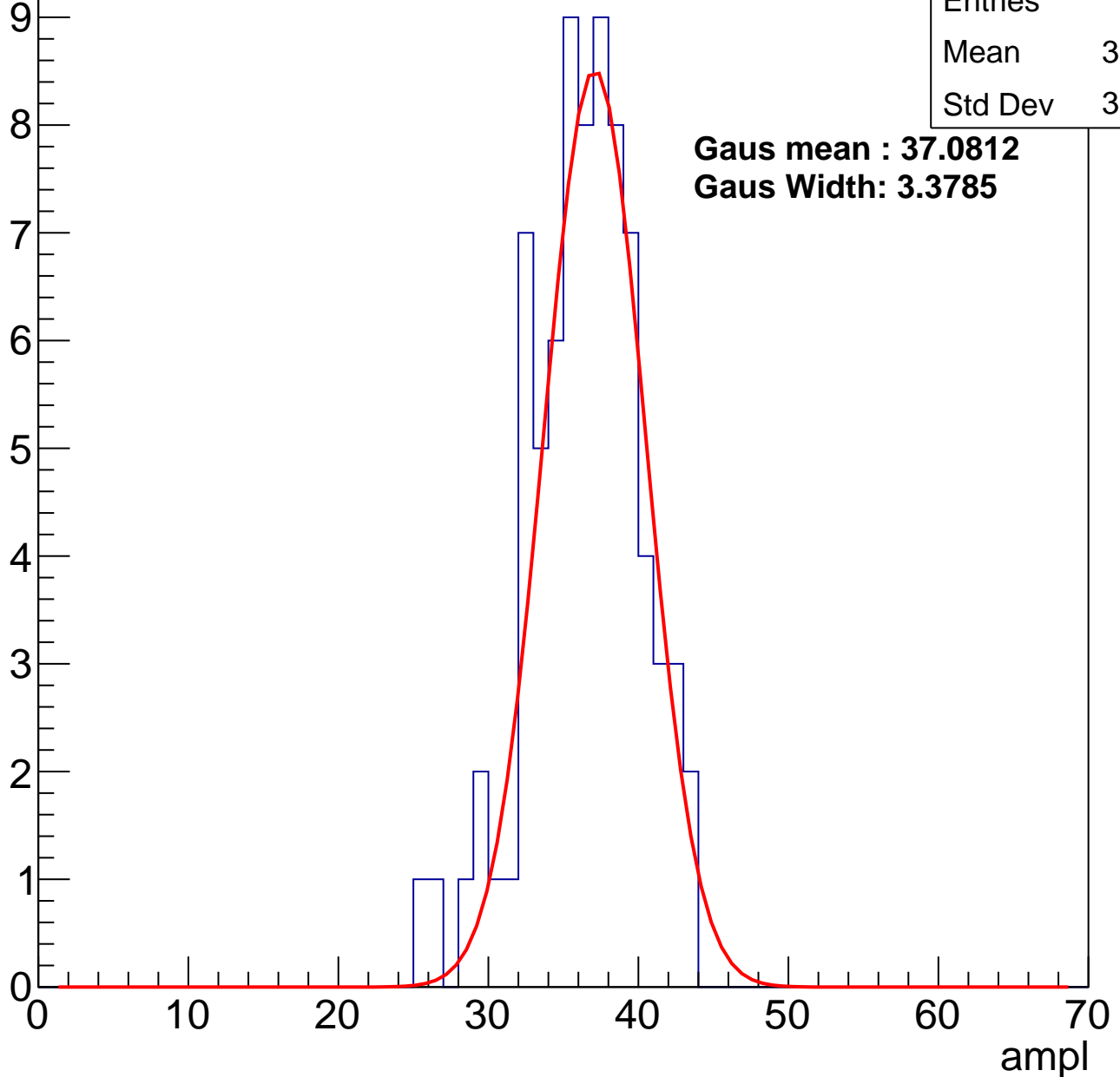
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	35.88
Std Dev	3.724

**Gaus mean : 37.0812**

**Gaus Width: 3.3785**



# B1L101S, U9-ch1, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	62
Mean	43.26
Std Dev	2.929

**Gaus mean : 43.5938**

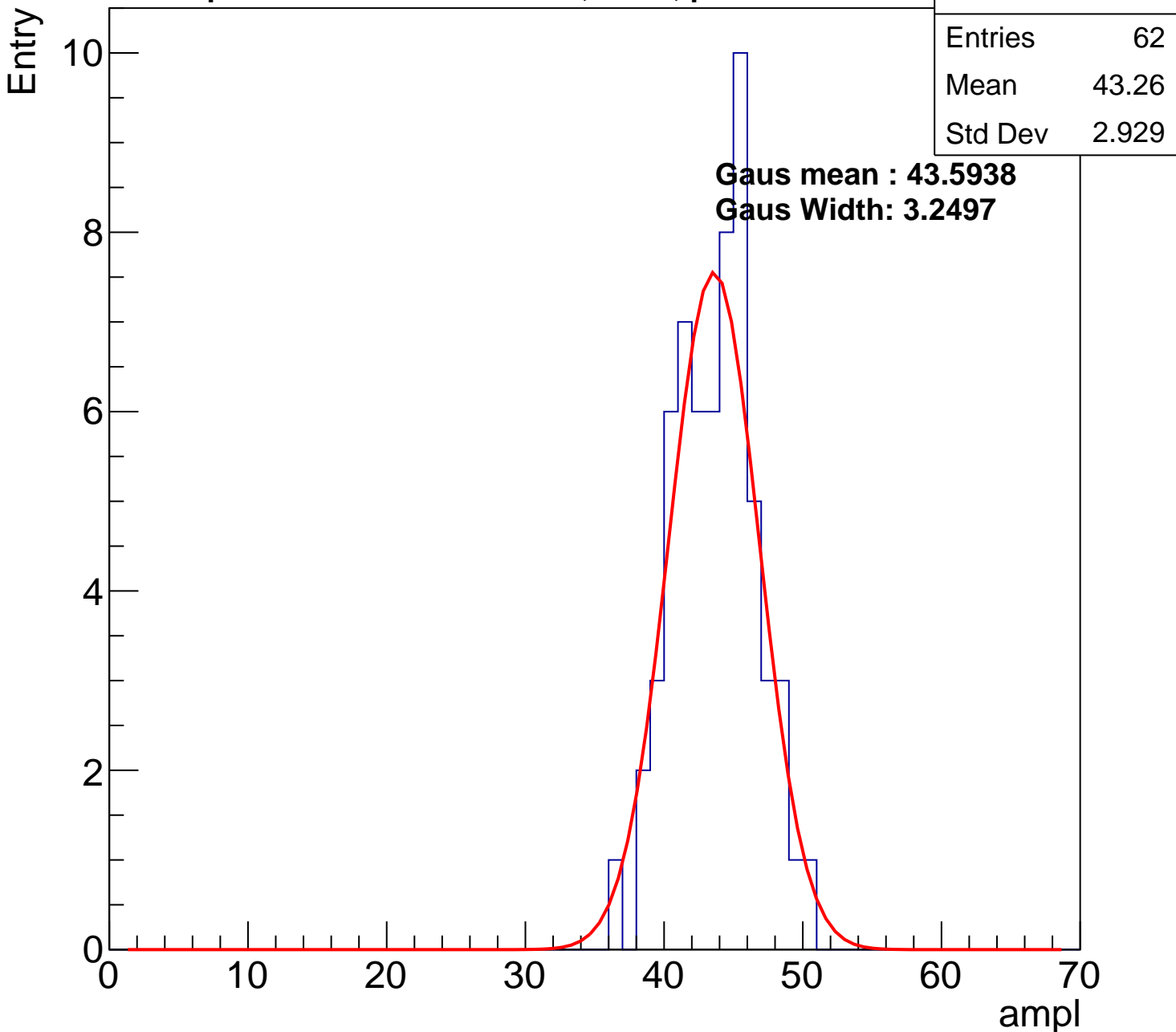
**Gaus Width: 3.2497**

Entry

10  
8  
6  
4  
2  
0

ampl

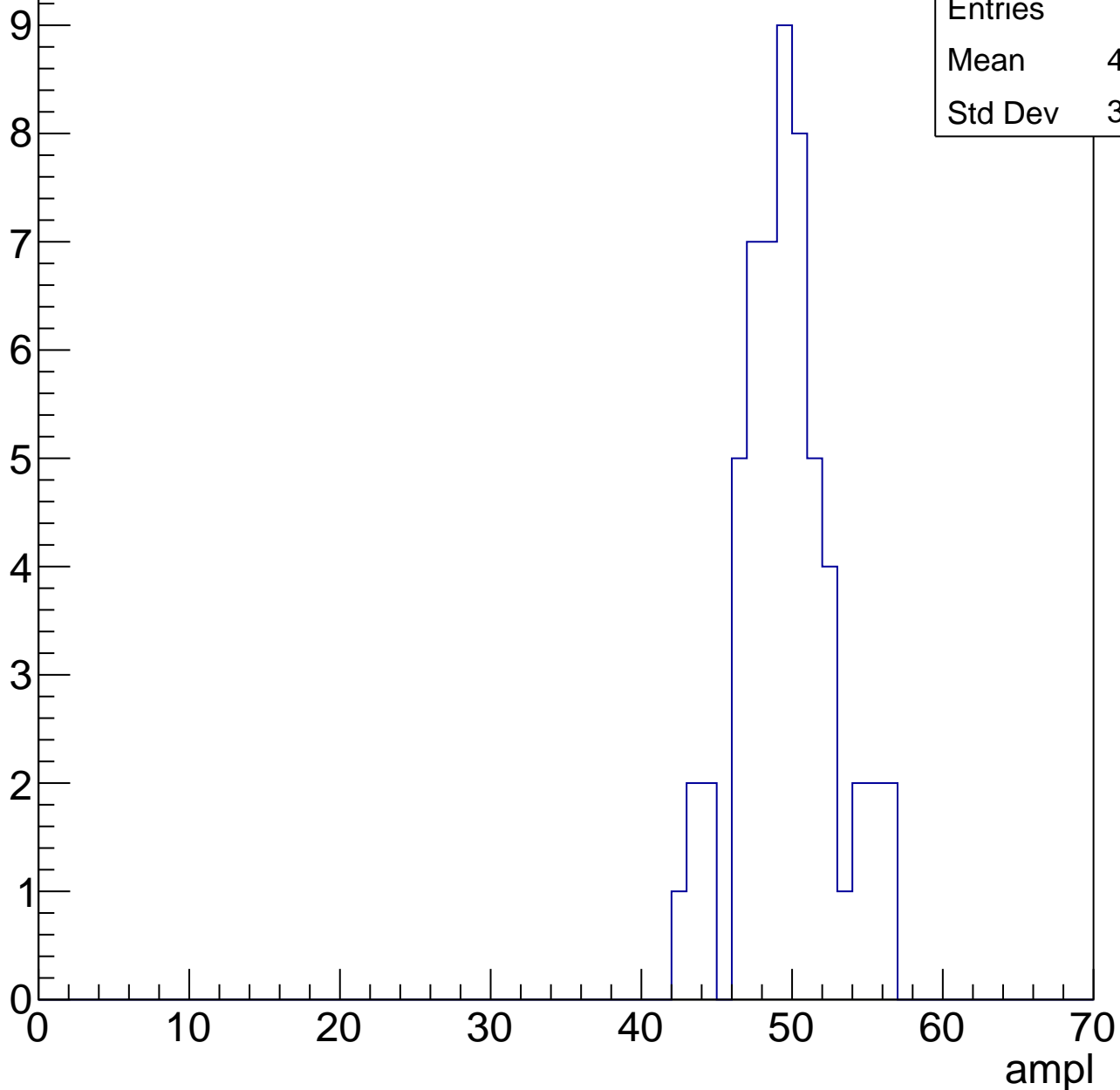
0 10 20 30 40 50 60 70



# B1L101S, U9-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



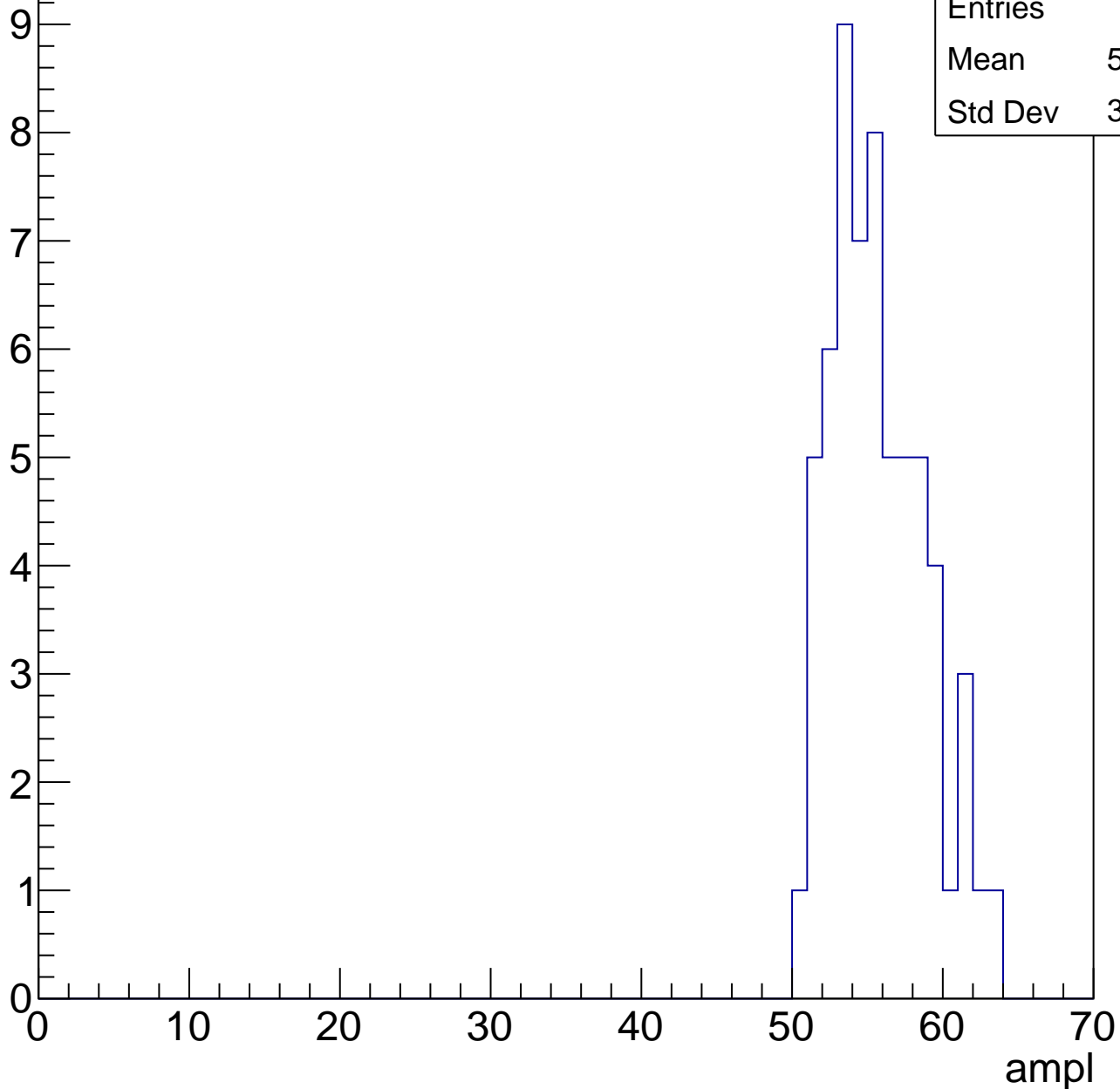
Entries	57
Mean	49.09
Std Dev	3.108

# B1L101S, U9-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	55.26
Std Dev	3.078

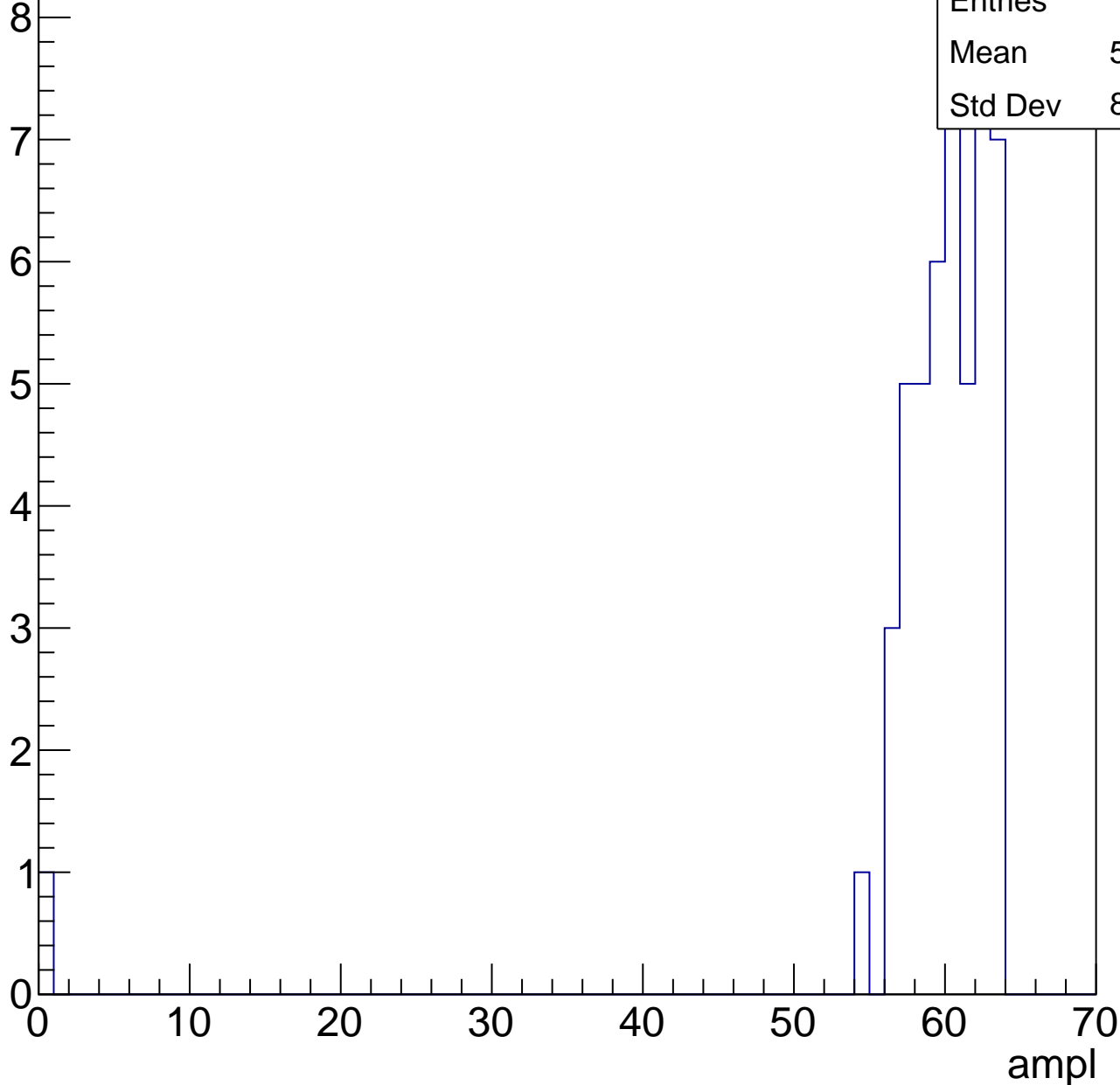


# B1L101S, U9-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	58.63
Std Dev	8.764



# B1L101S, U9-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.67
Std Dev	1.106

ampl

0 10 20 30 40 50 60 70



# B1L101S, U9-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U9-ch2, adc0

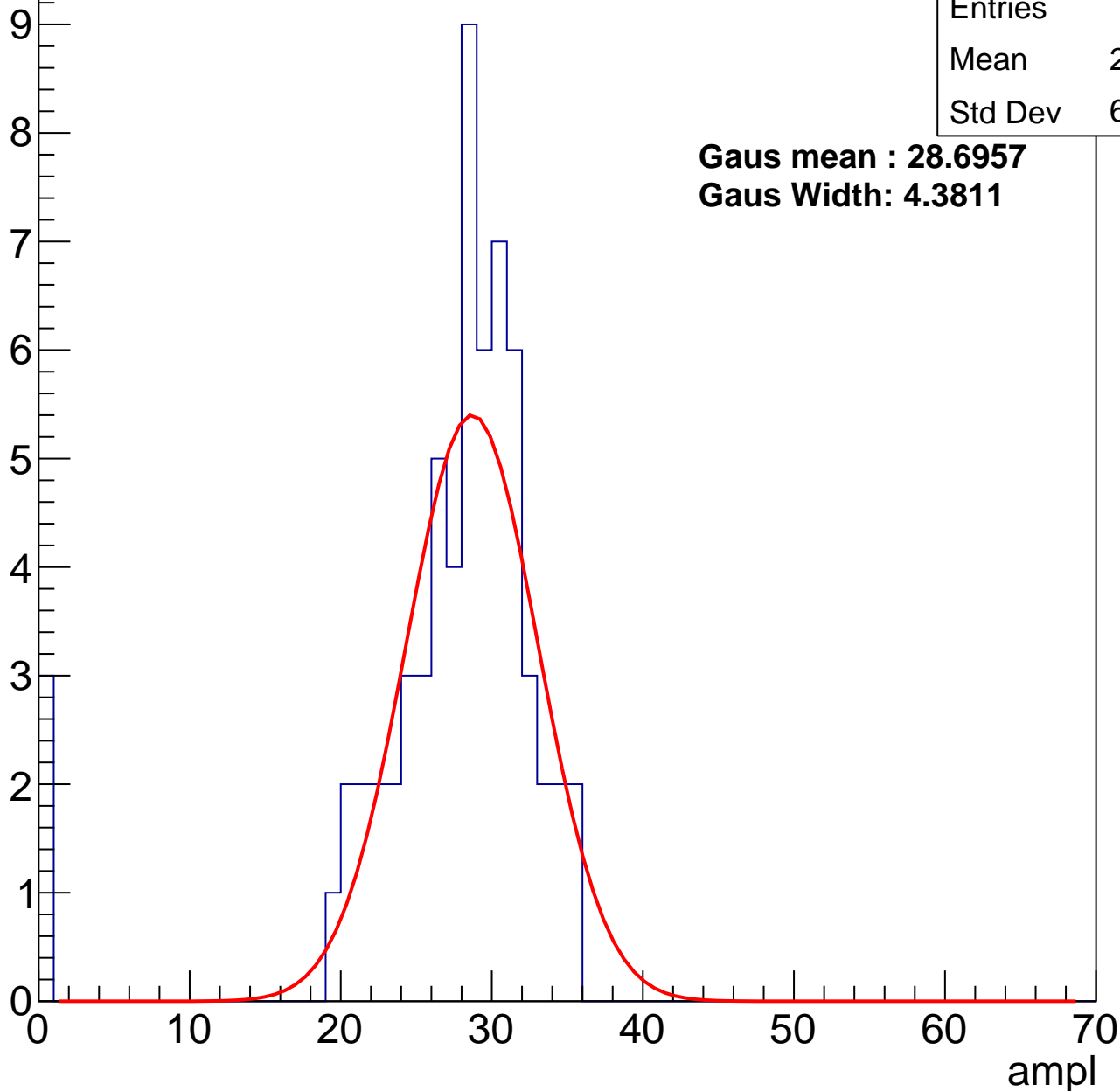
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	26.53
Std Dev	6.957

**Gaus mean : 28.6957**

**Gaus Width: 4.3811**



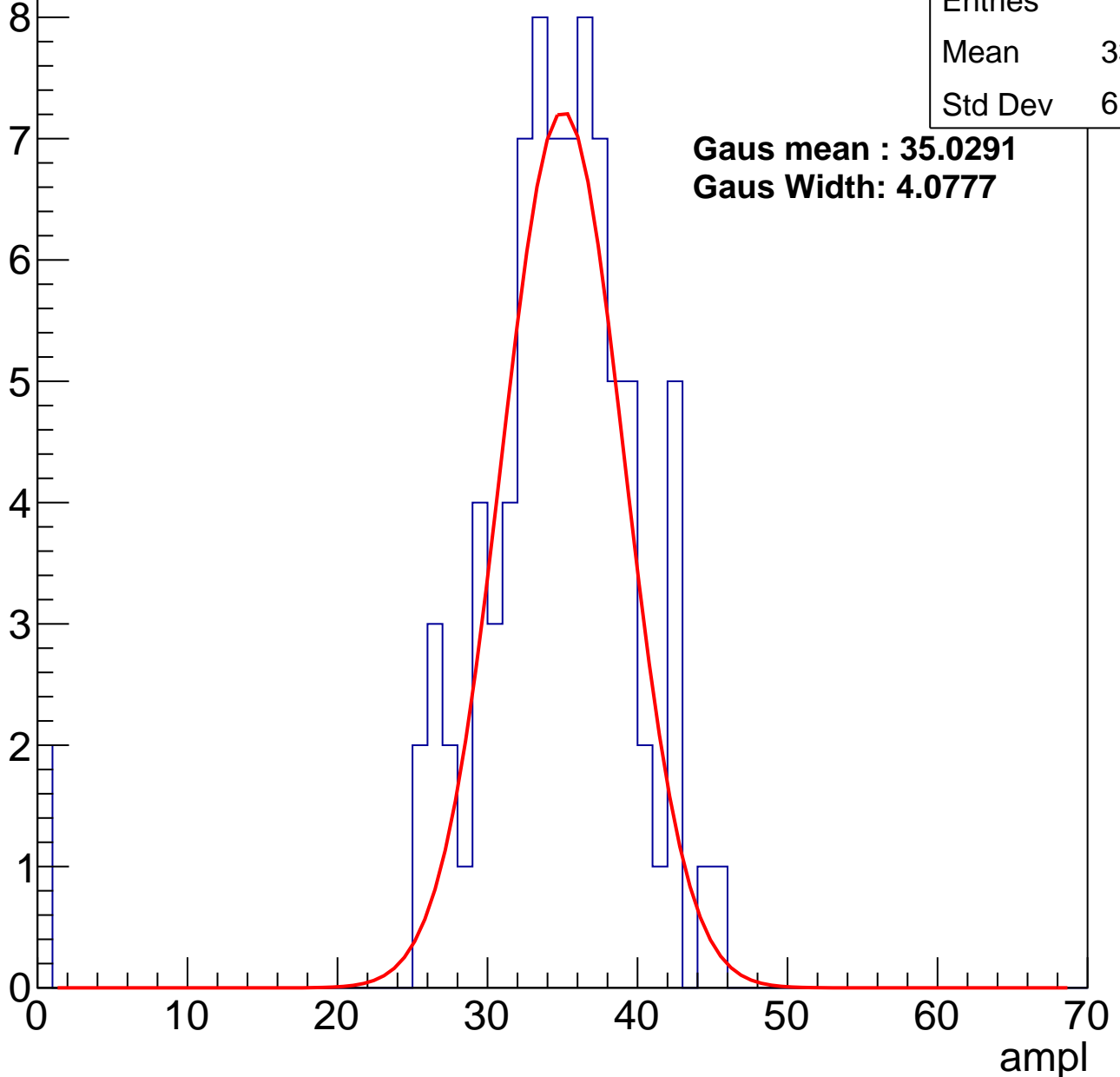
# B1L101S, U9-ch2, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	85
Mean	33.68
Std Dev	6.843

**Gaus mean : 35.0291**  
**Gaus Width: 4.0777**



# B1L101S, U9-ch2, adc2

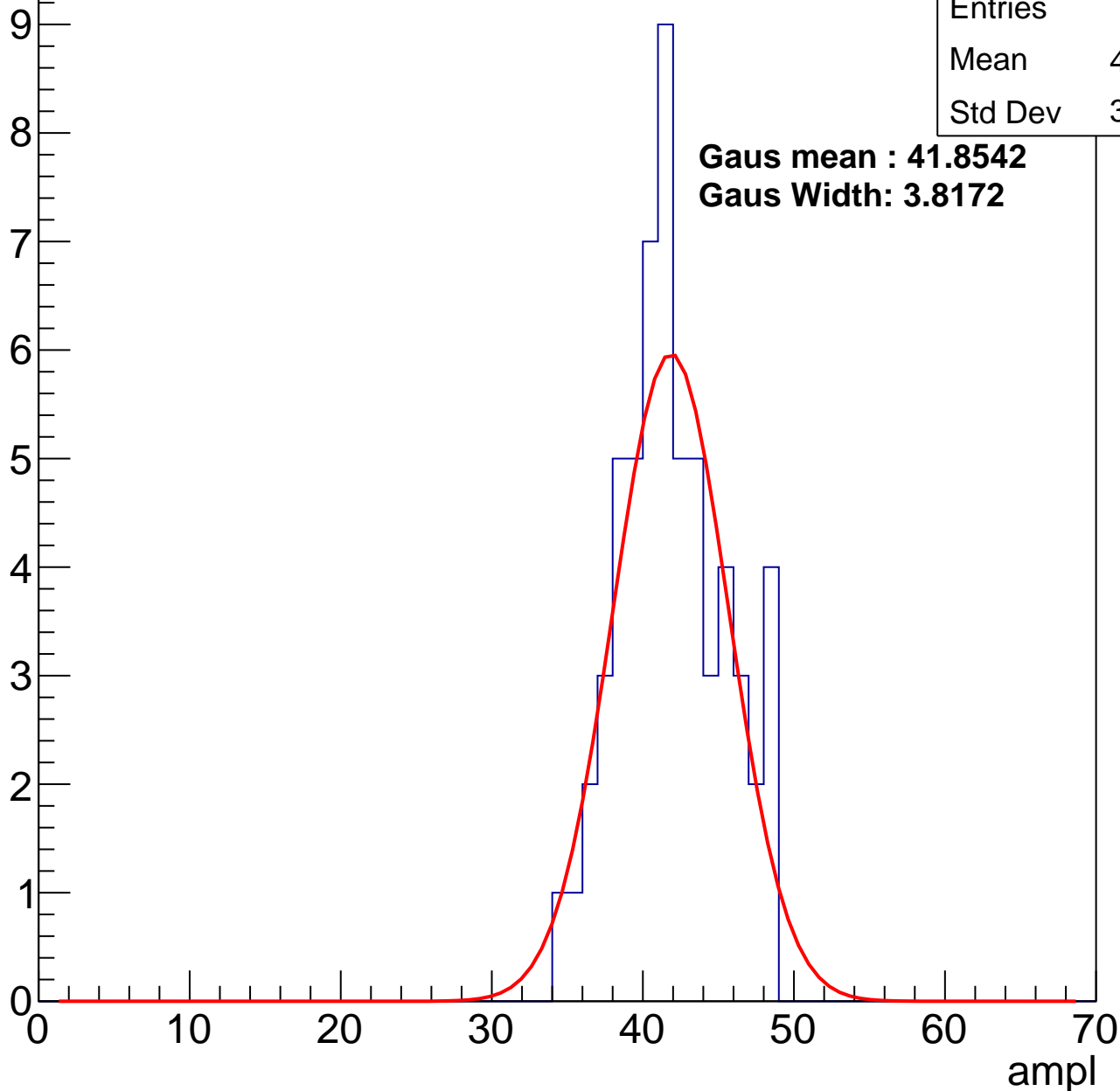
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	41.47
Std Dev	3.446

**Gaus mean : 41.8542**

**Gaus Width: 3.8172**

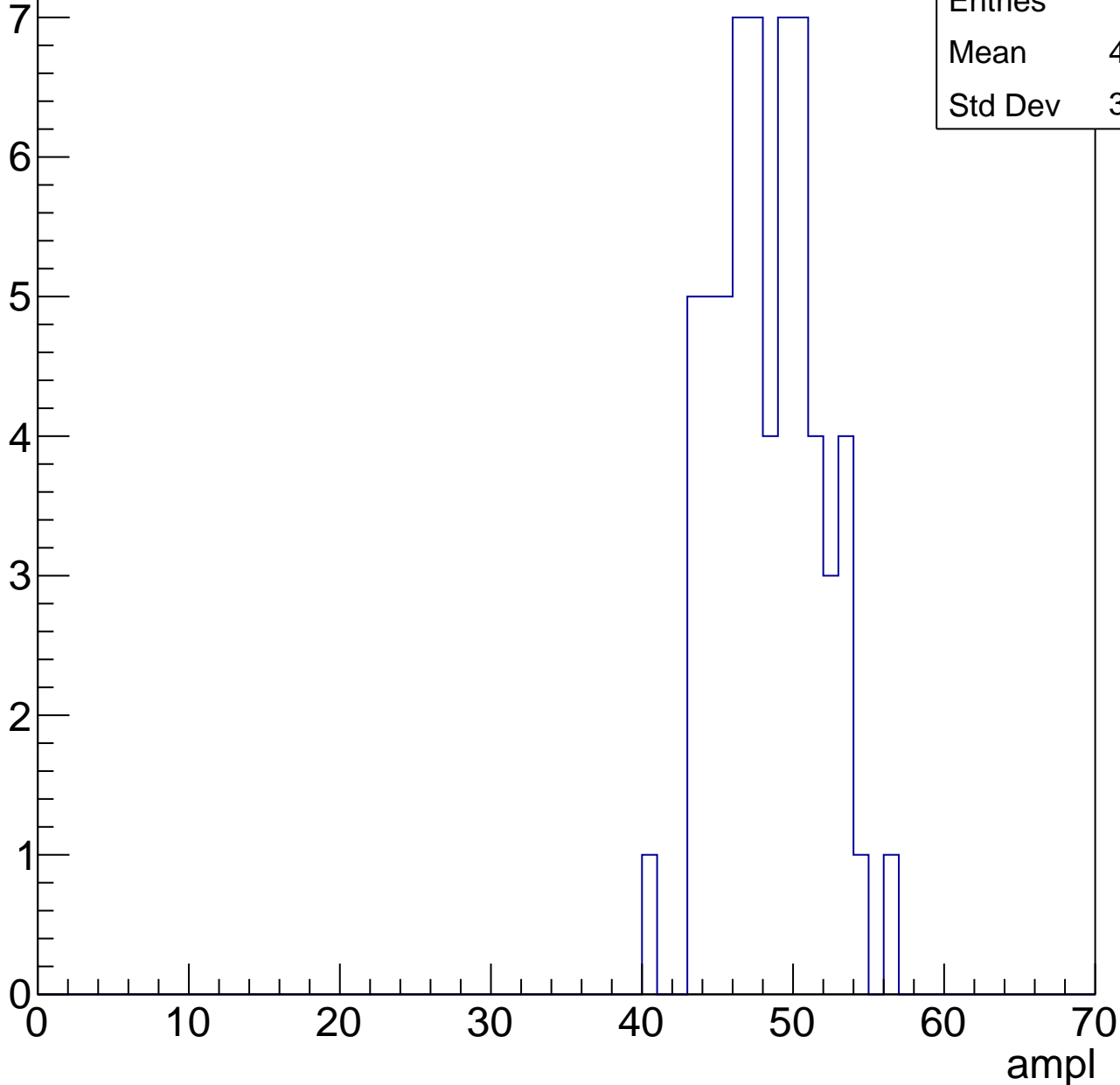


# B1L101S, U9-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	47.84
Std Dev	3.305

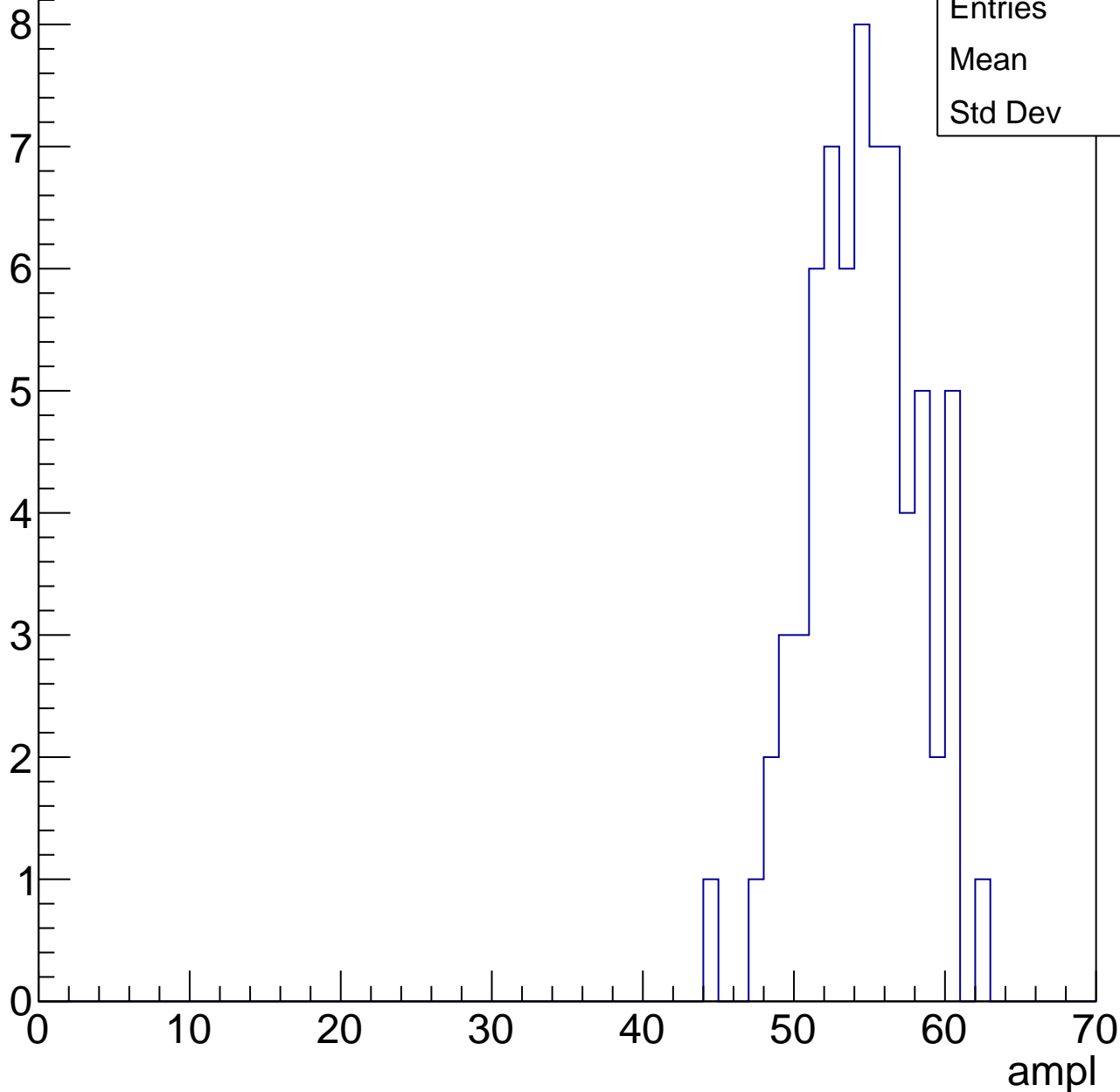


# B1L101S, U9-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

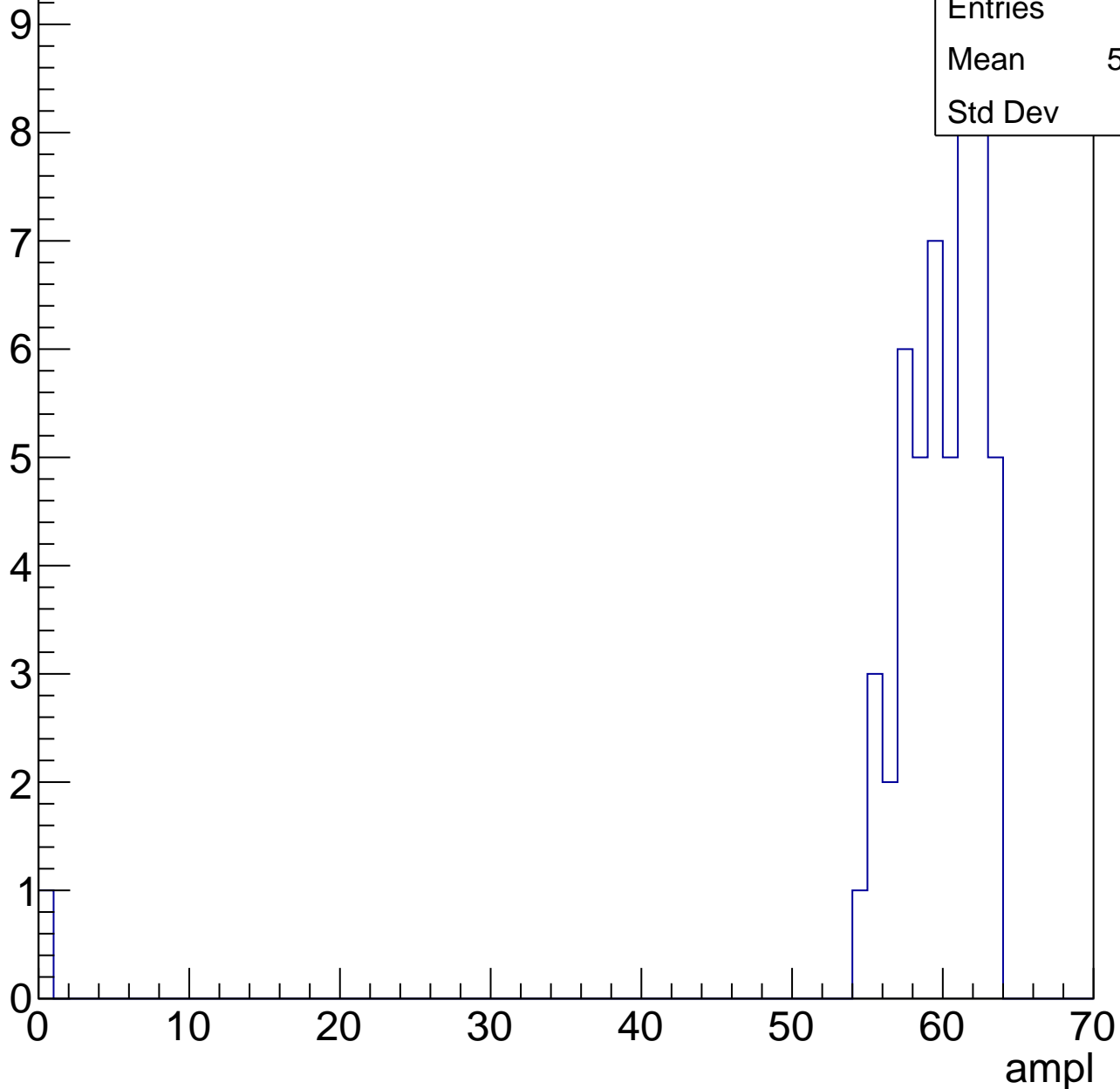
Entries	68
Mean	54.1
Std Dev	3.59



# B1L101S, U9-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

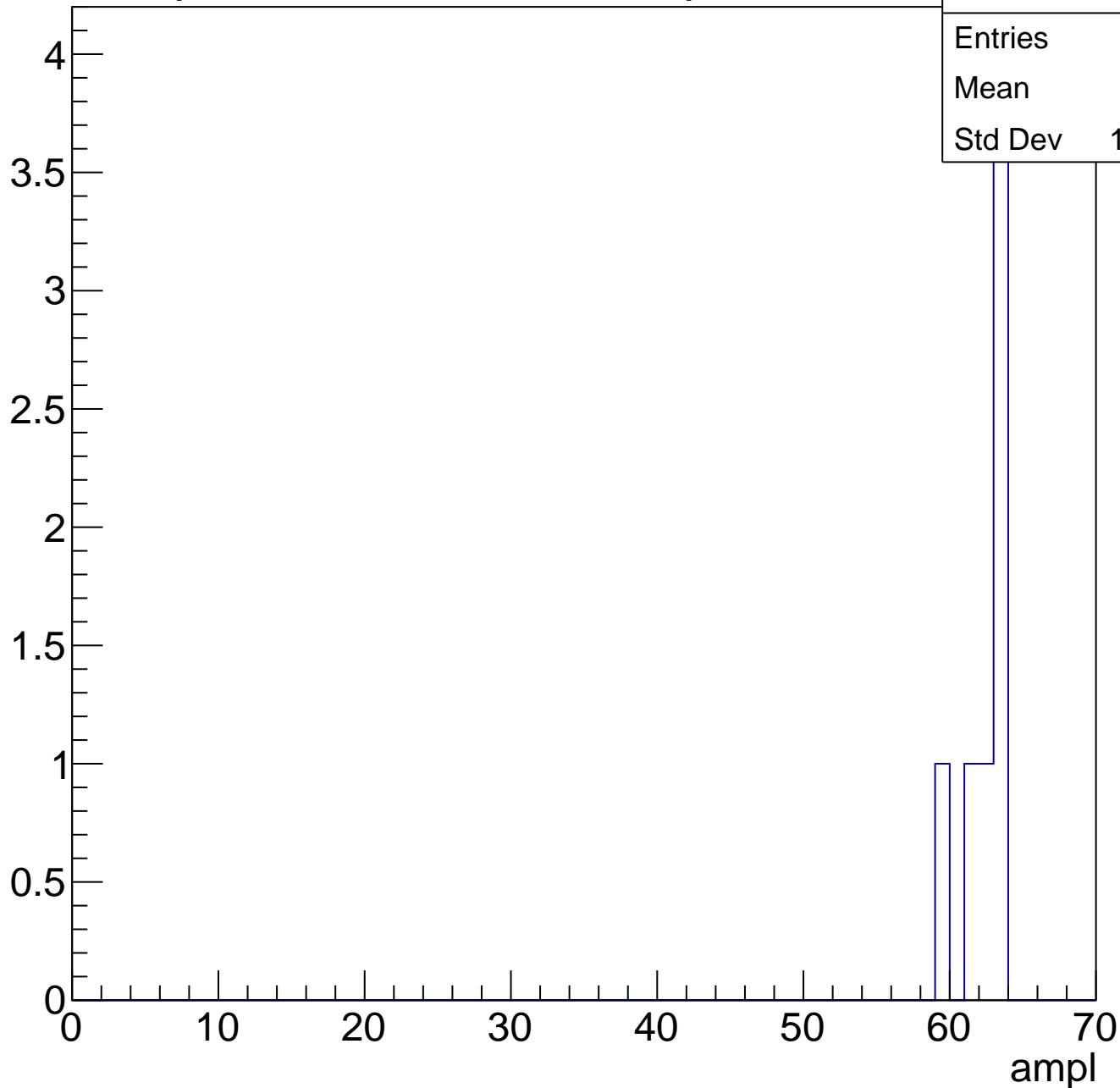
Entry



# B1L101S, U9-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch3, adc0

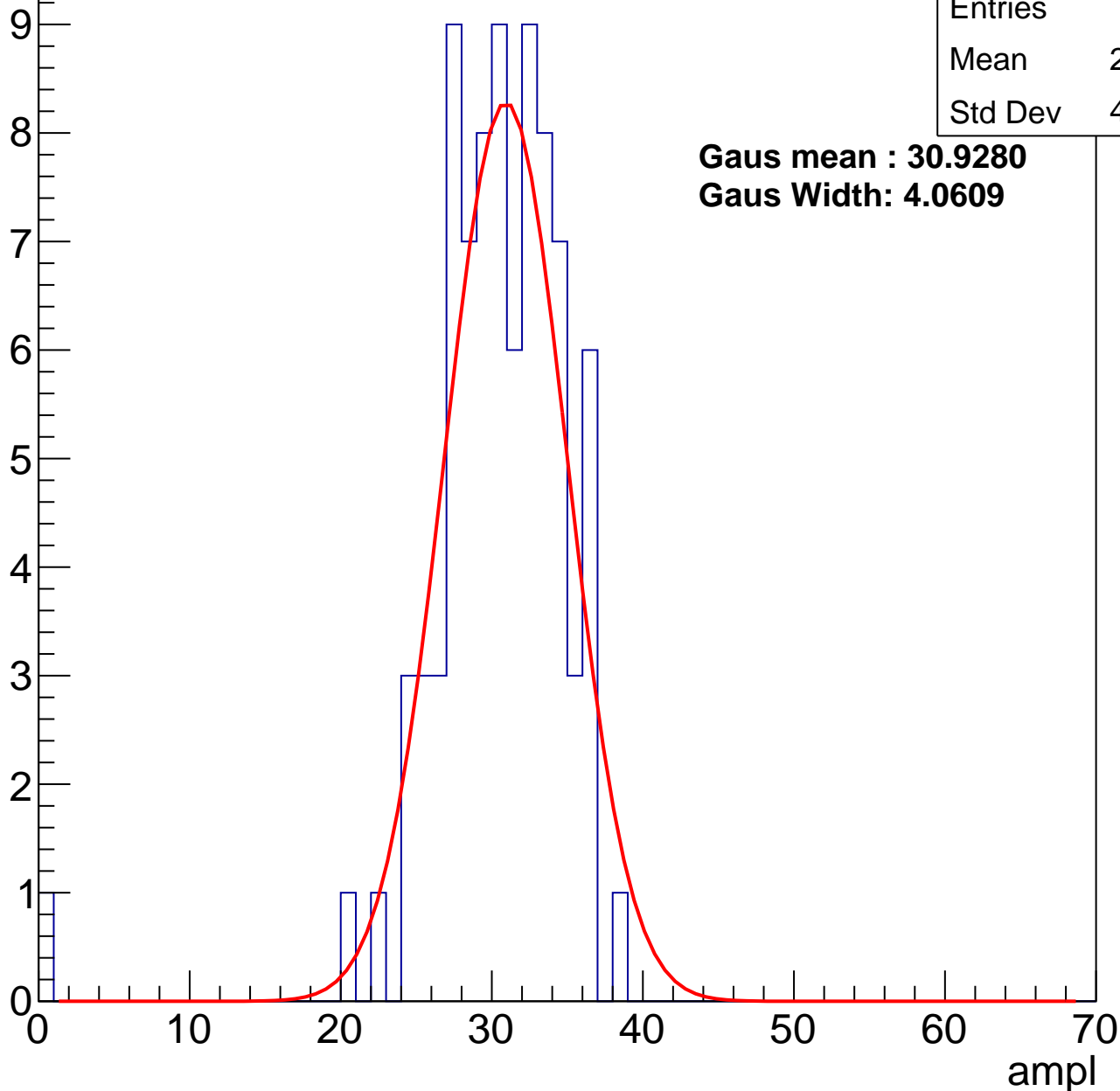
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	85
Mean	29.92
Std Dev	4.842

**Gaus mean : 30.9280**

**Gaus Width: 4.0609**



# B1L101S, U9-ch3, adc1

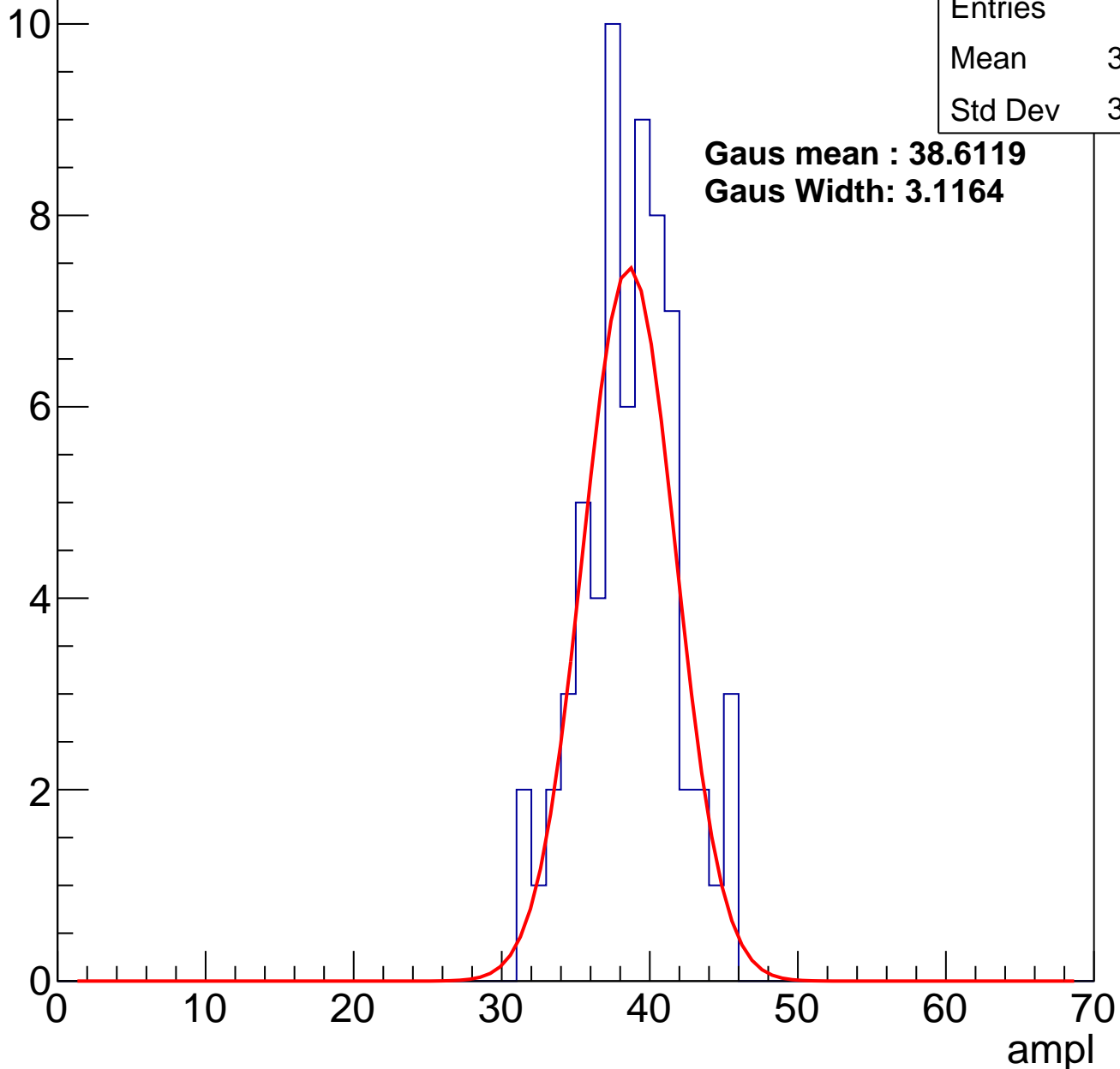
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	65
Mean	38.25
Std Dev	3.206

**Gaus mean : 38.6119**

**Gaus Width: 3.1164**

Entry



# B1L101S, U9-ch3, adc2

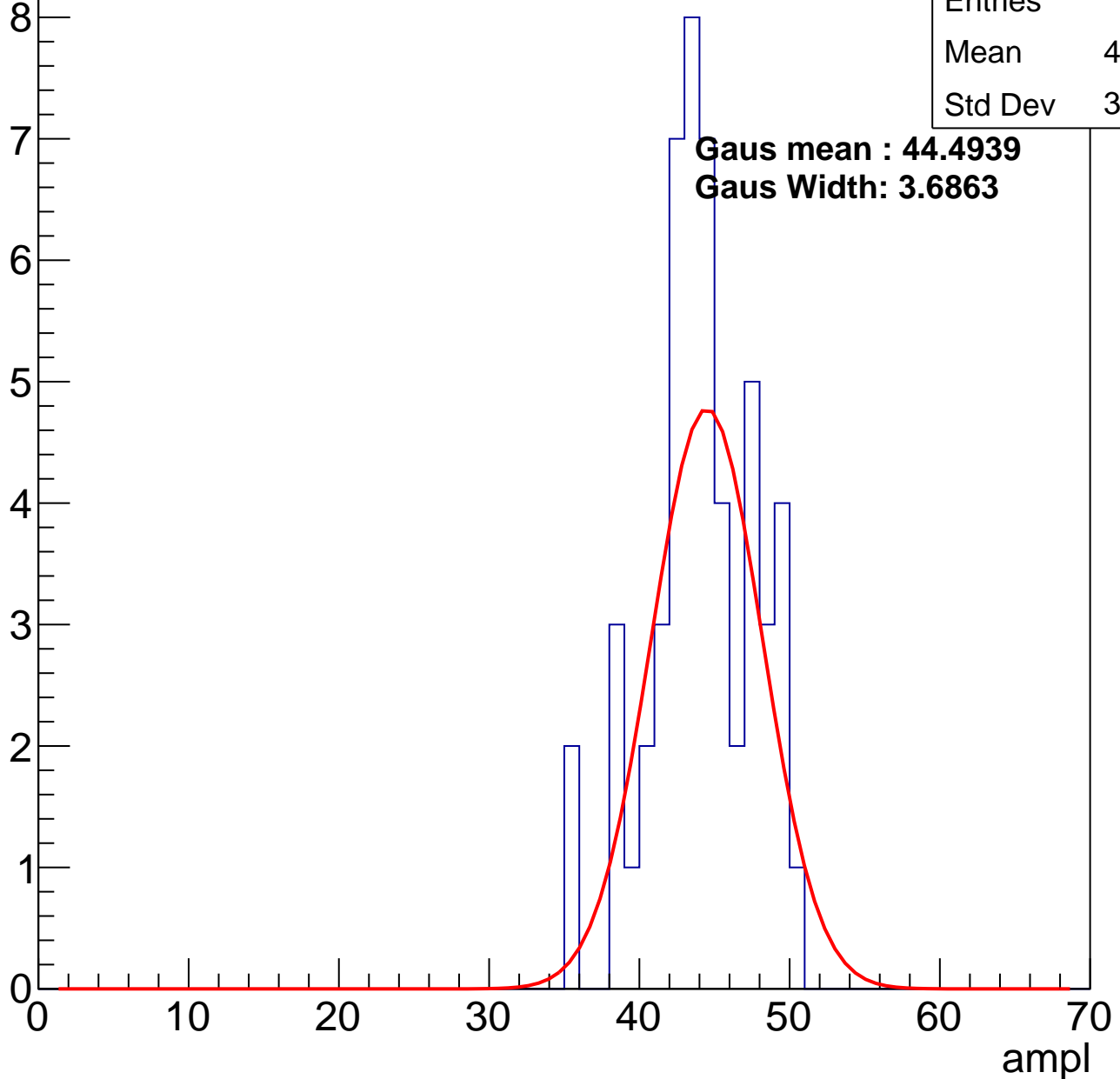
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	43.63
Std Dev	3.464

**Gaus mean : 44.4939**

**Gaus Width: 3.6863**



# B1L101S, U9-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

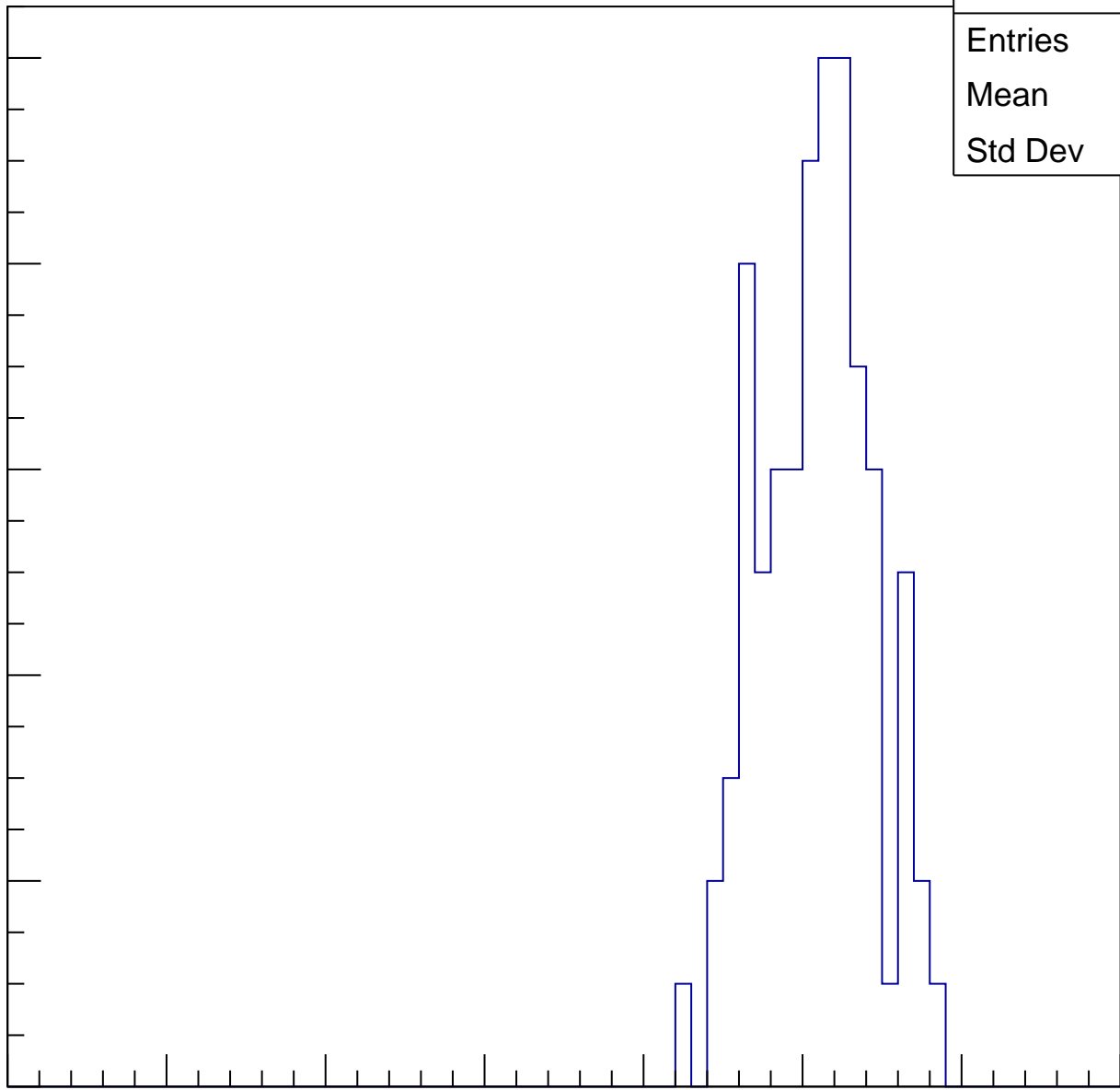
Entries	82
Mean	50.39
Std Dev	3.453

Entry

10  
8  
6  
4  
2  
0

ampl

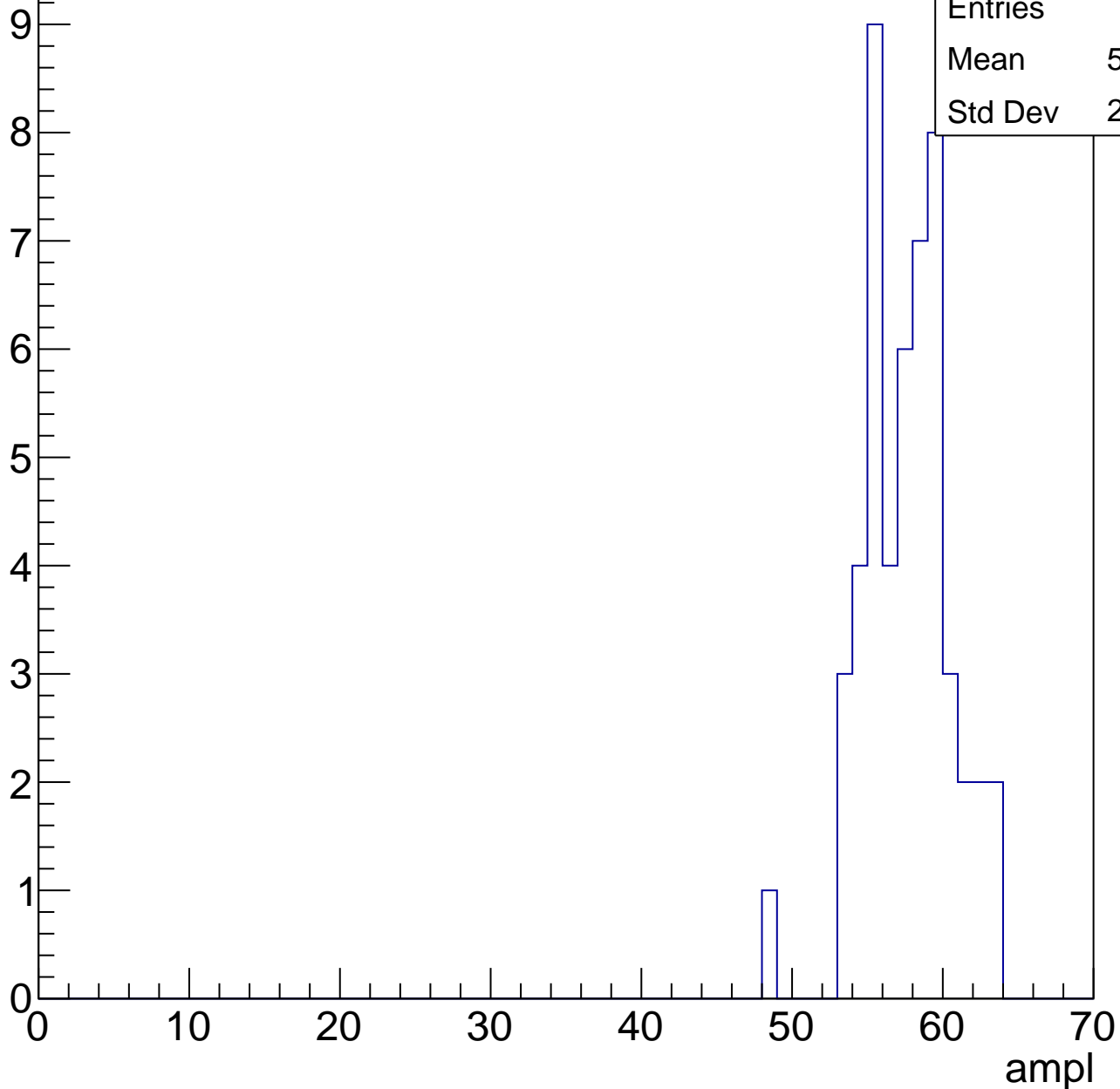
0 10 20 30 40 50 60 70



# B1L101S, U9-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

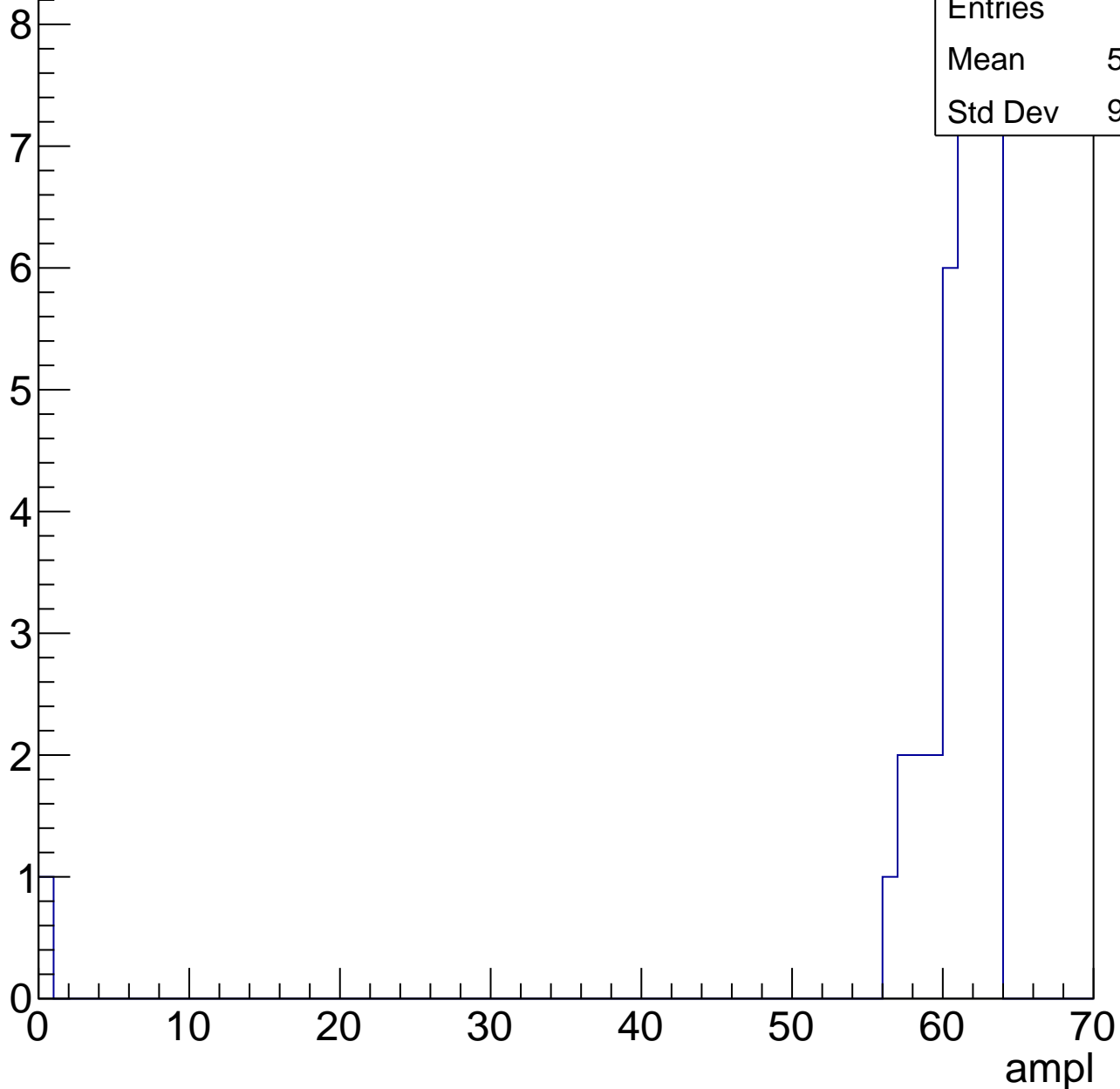


Entries	51
Mean	57.14
Std Dev	2.883

# B1L101S, U9-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	60
Std Dev	0

ampl



# B1L101S, U9-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U9-ch4, adc0

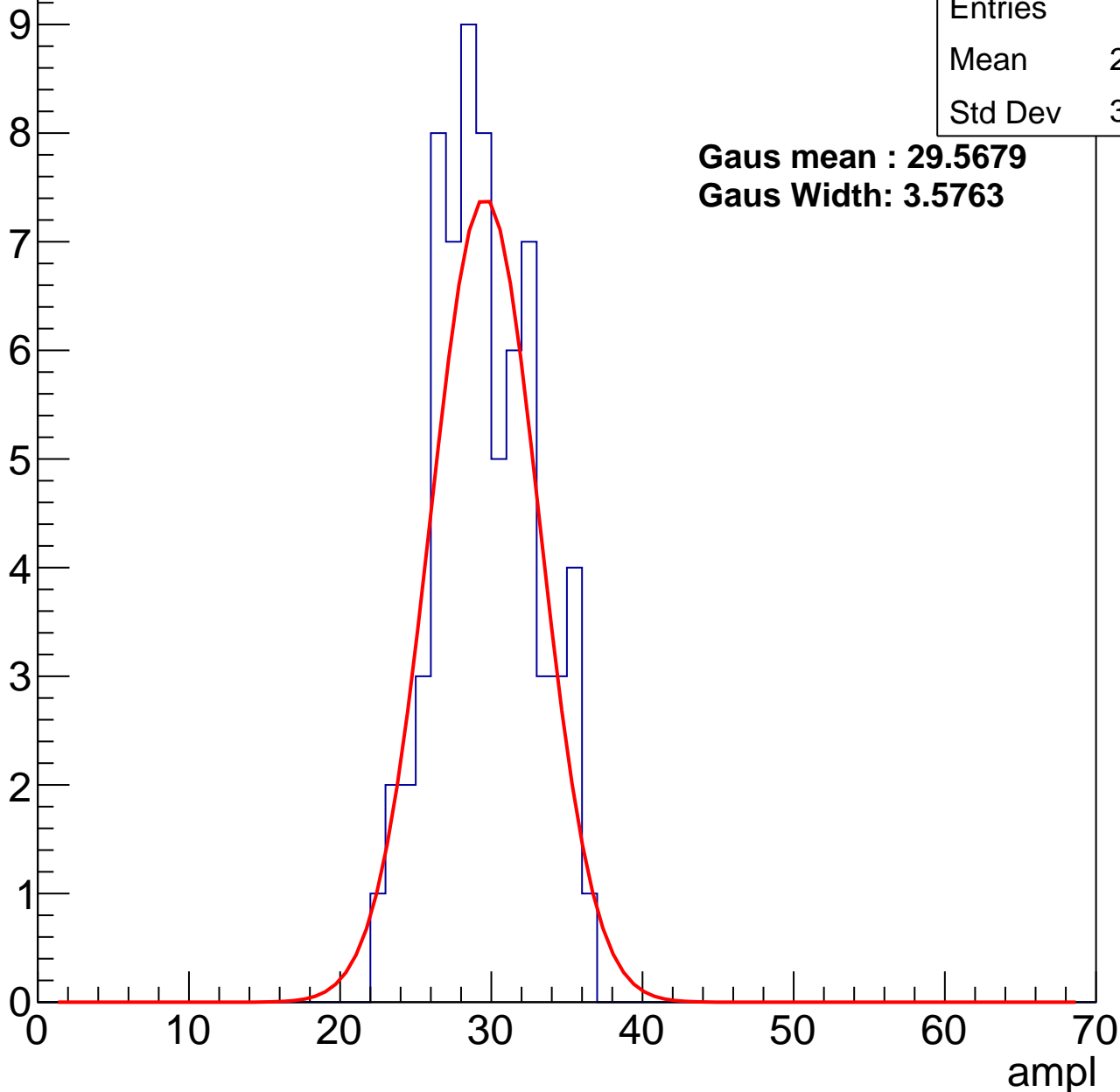
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	29.12
Std Dev	3.264

**Gaus mean : 29.5679**

**Gaus Width: 3.5763**



# B1L101S, U9-ch4, adc1

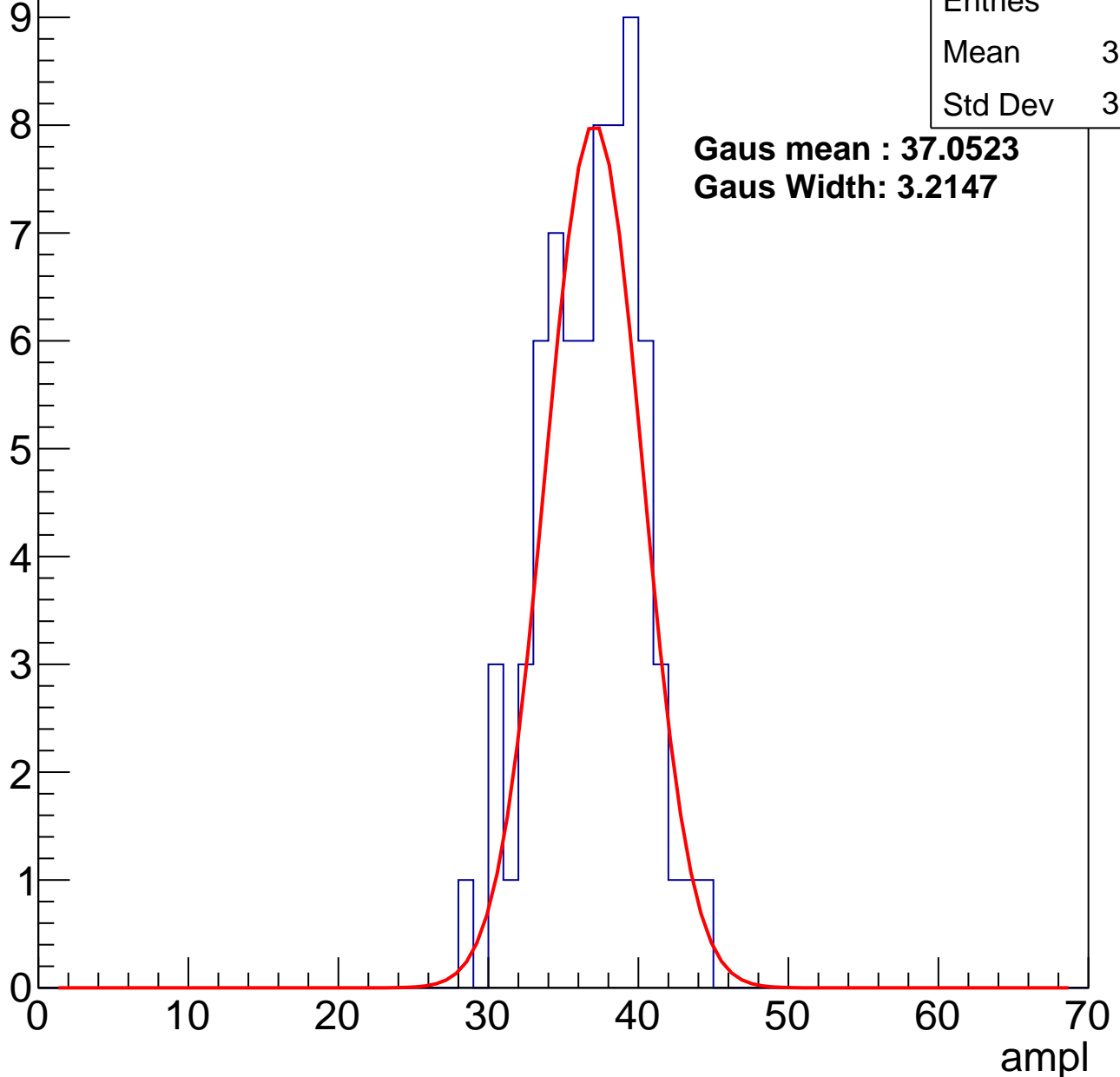
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	36.43
Std Dev	3.297

**Gaus mean : 37.0523**

**Gaus Width: 3.2147**



# B1L101S, U9-ch4, adc2

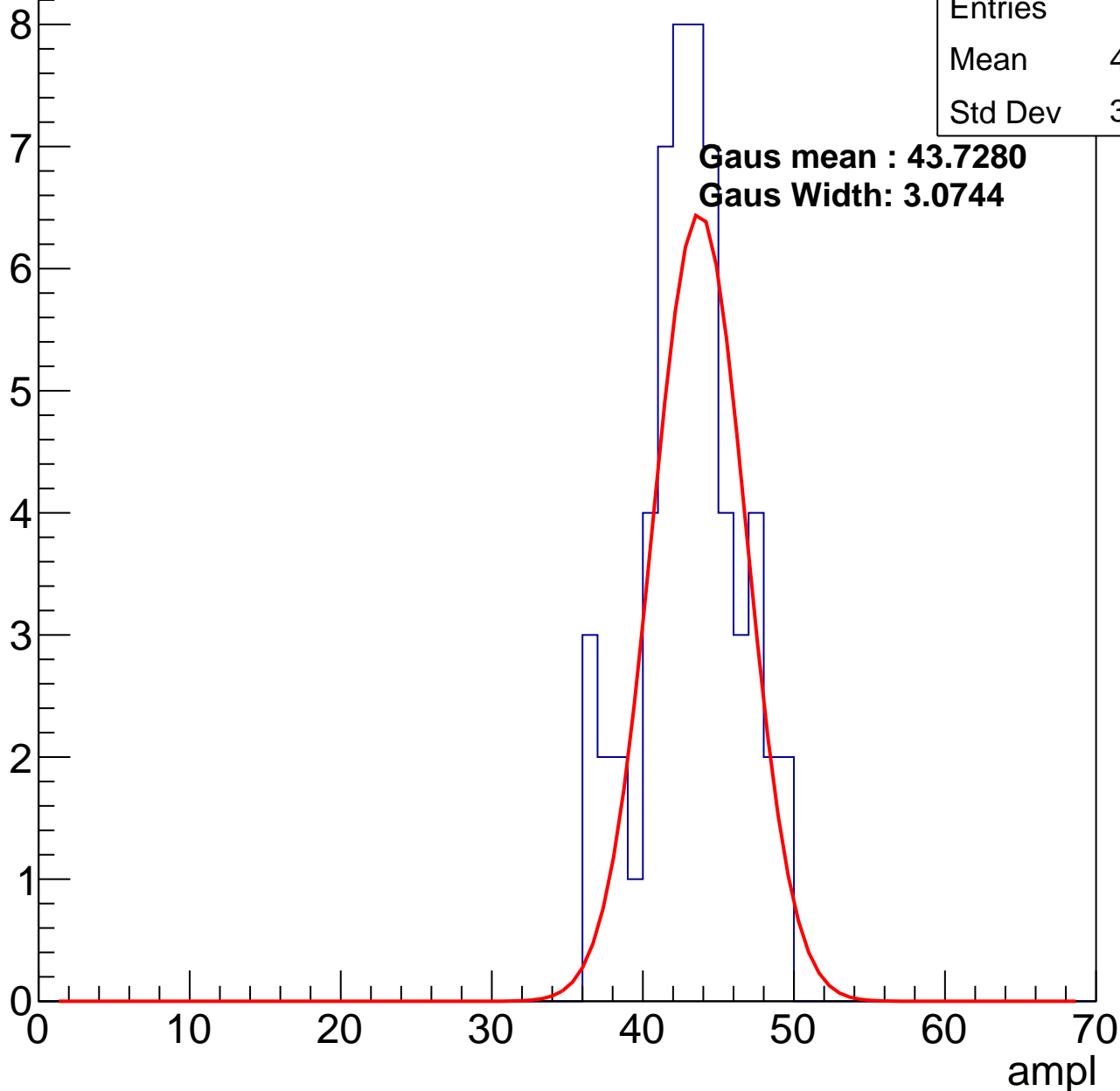
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	42.67
Std Dev	3.208

**Gaus mean : 43.7280**

**Gaus Width: 3.0744**

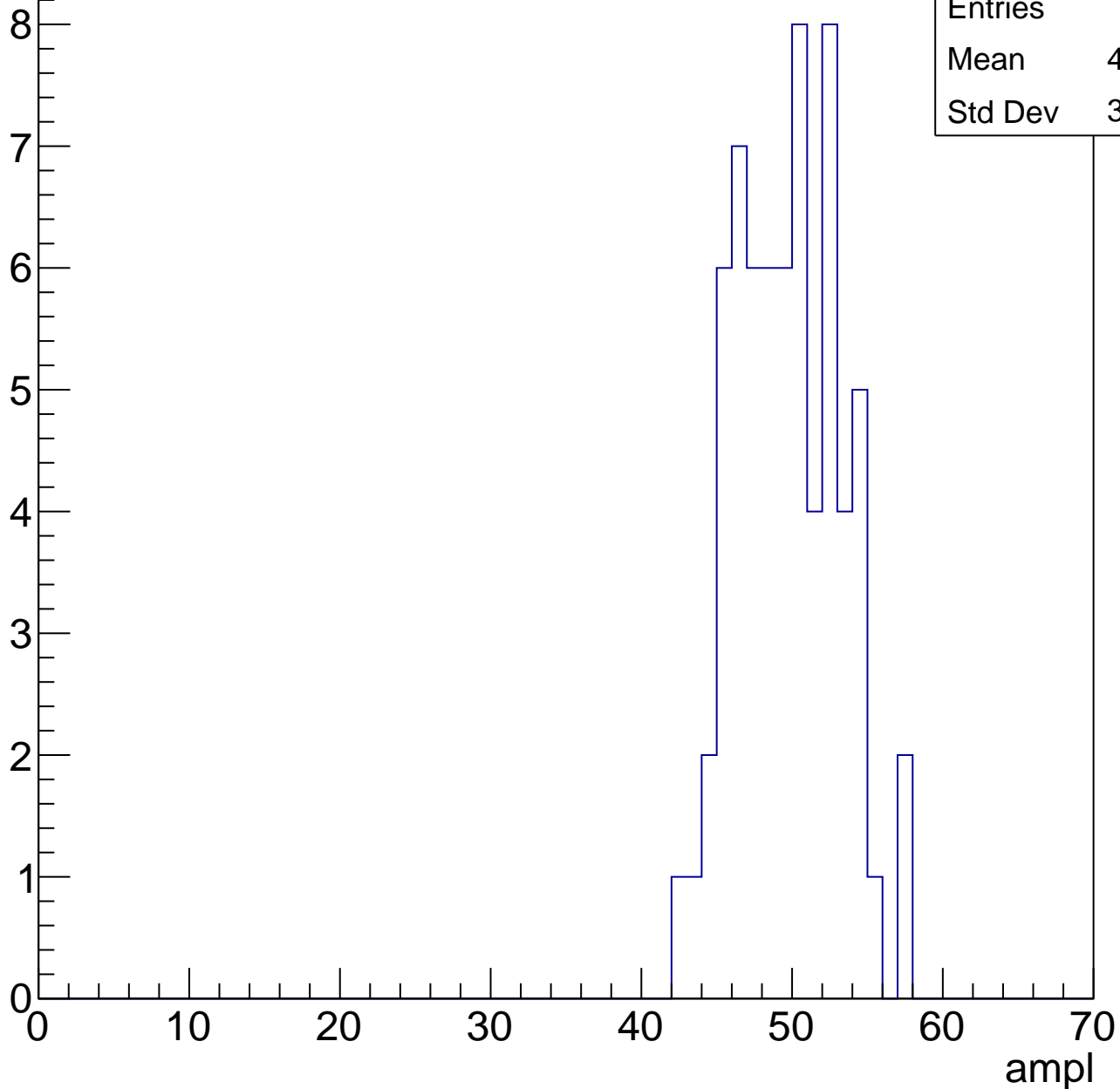


# B1L101S, U9-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

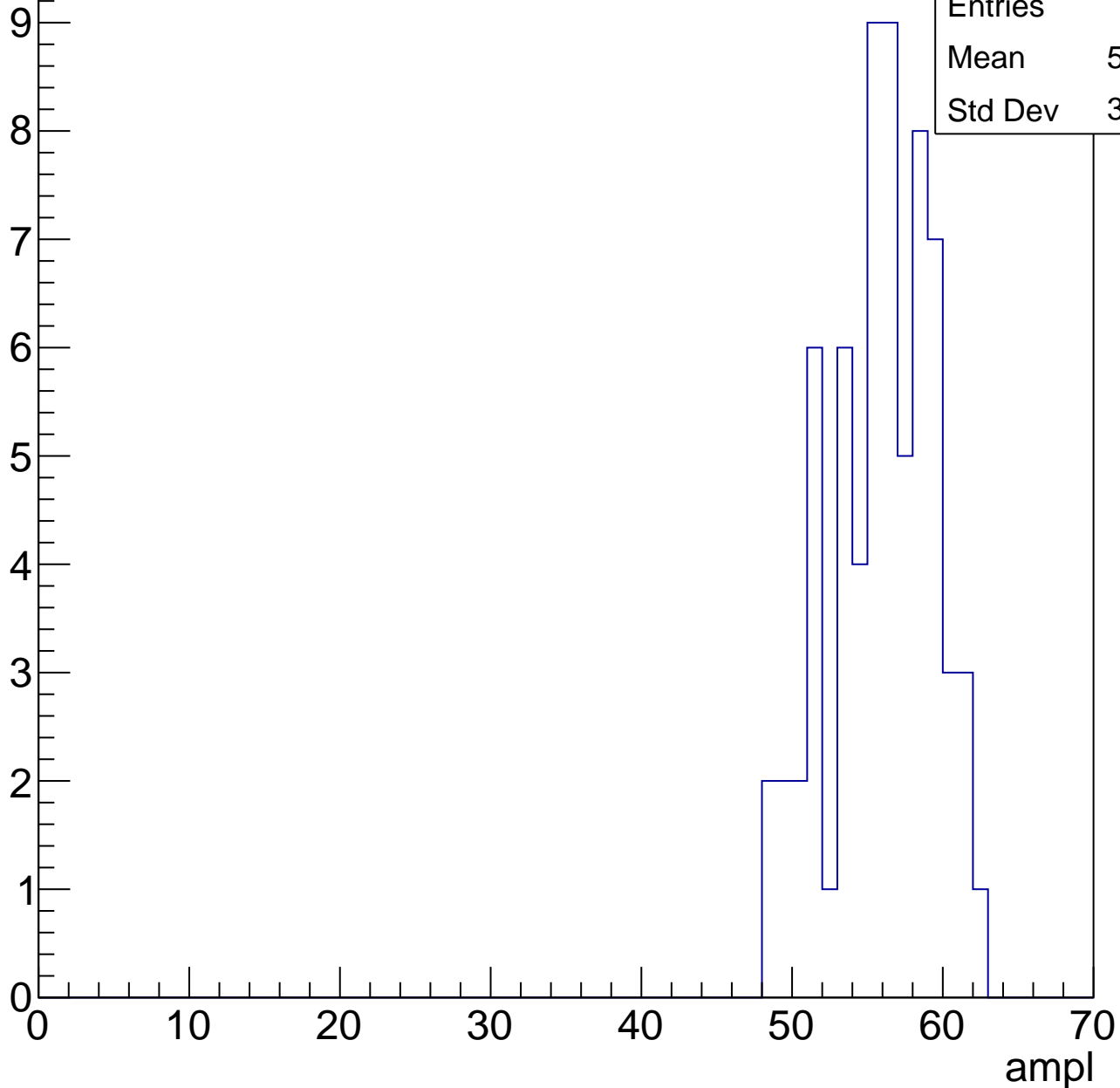
Entries	67
Mean	49.25
Std Dev	3.387



# B1L101S, U9-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

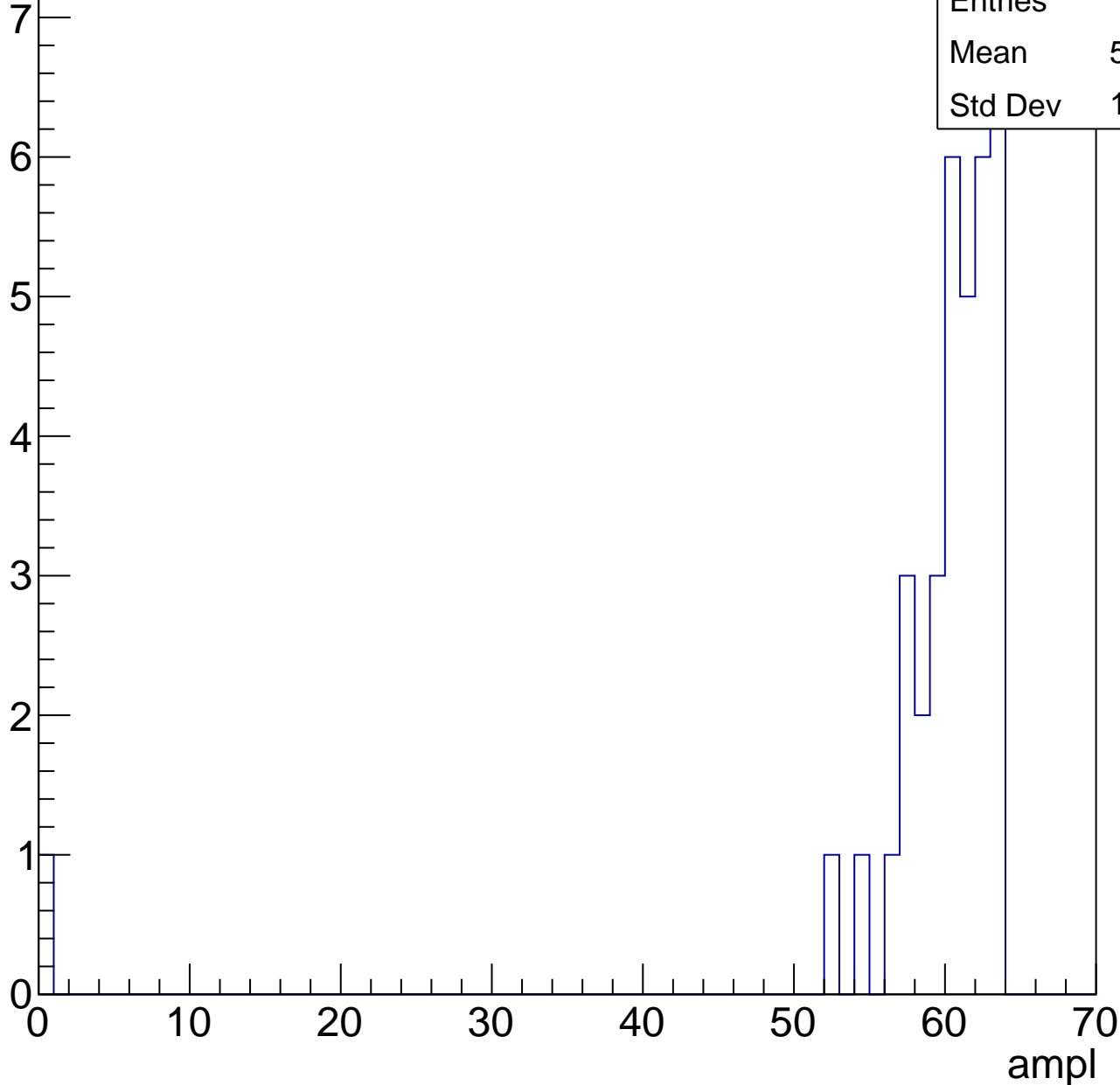


# B1L101S, U9-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	36
Mean	58.44
Std Dev	10.22



# B1L101S, U9-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

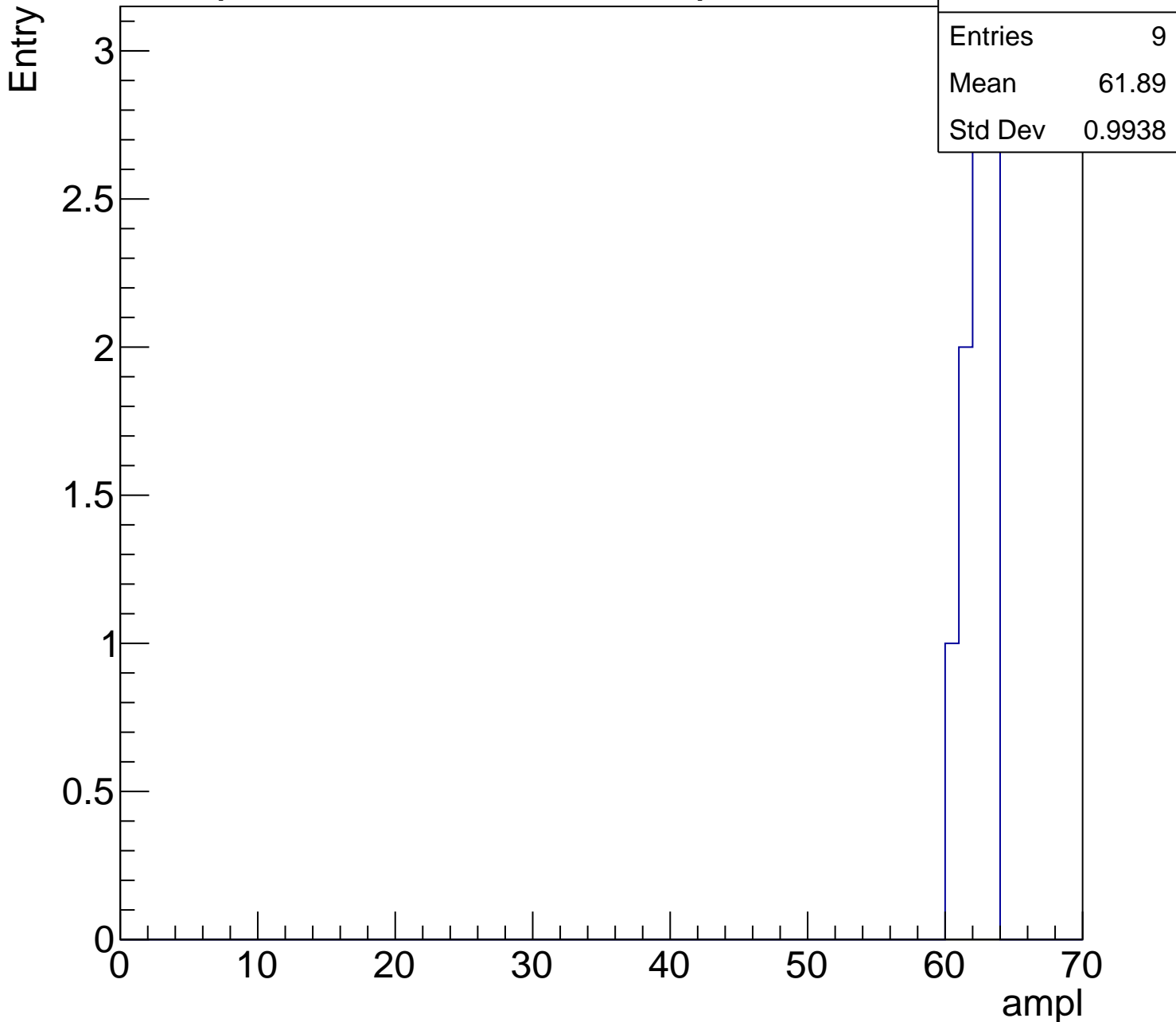
9

Mean

61.89

Std Dev

0.9938





# B1L101S, U9-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	21
Std Dev	0

ampl

# B1L101S, U9-ch5, adc0

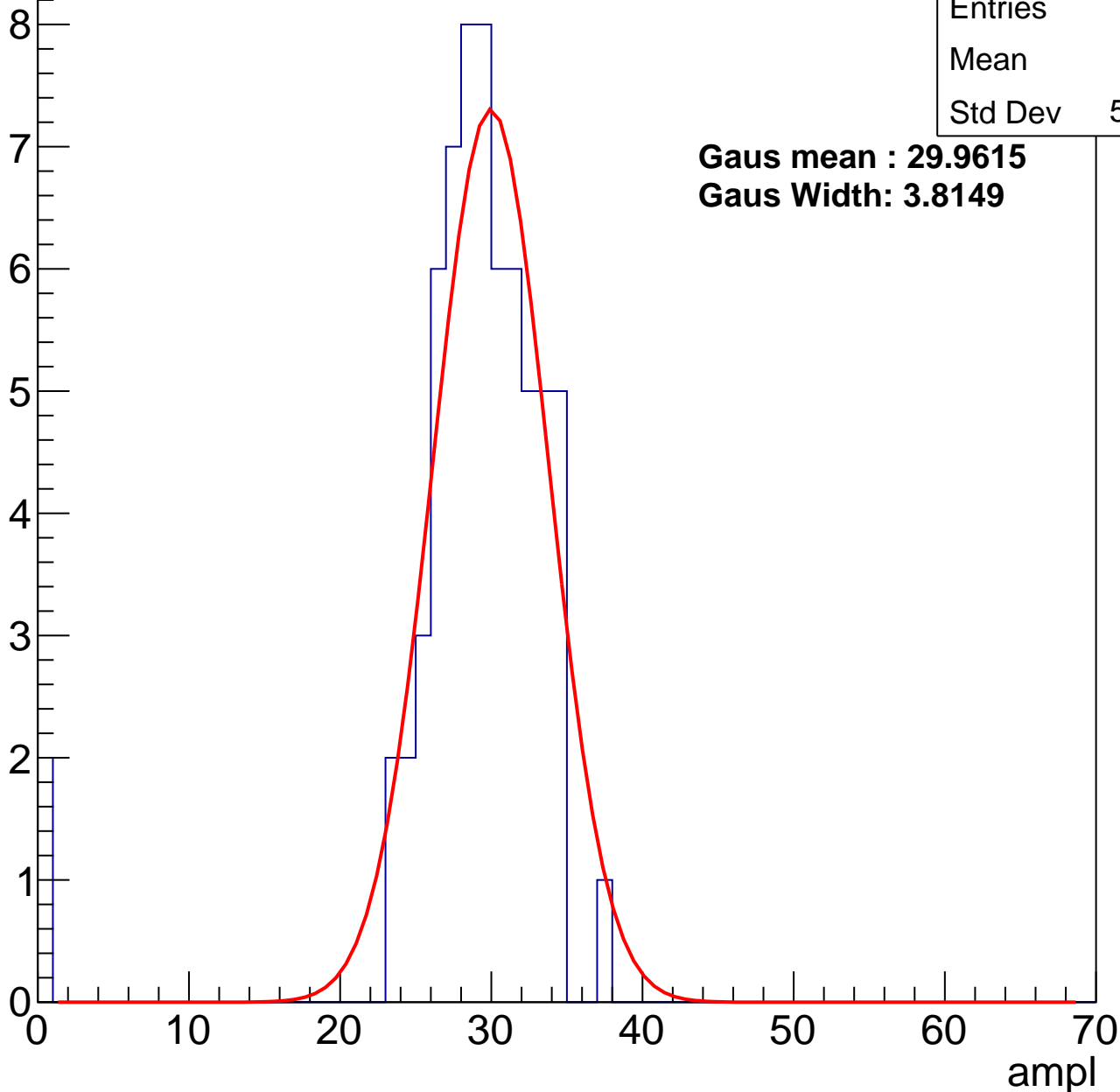
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	28.3
Std Dev	5.844

**Gaus mean : 29.9615**

**Gaus Width: 3.8149**



# B1L101S, U9-ch5, adc1

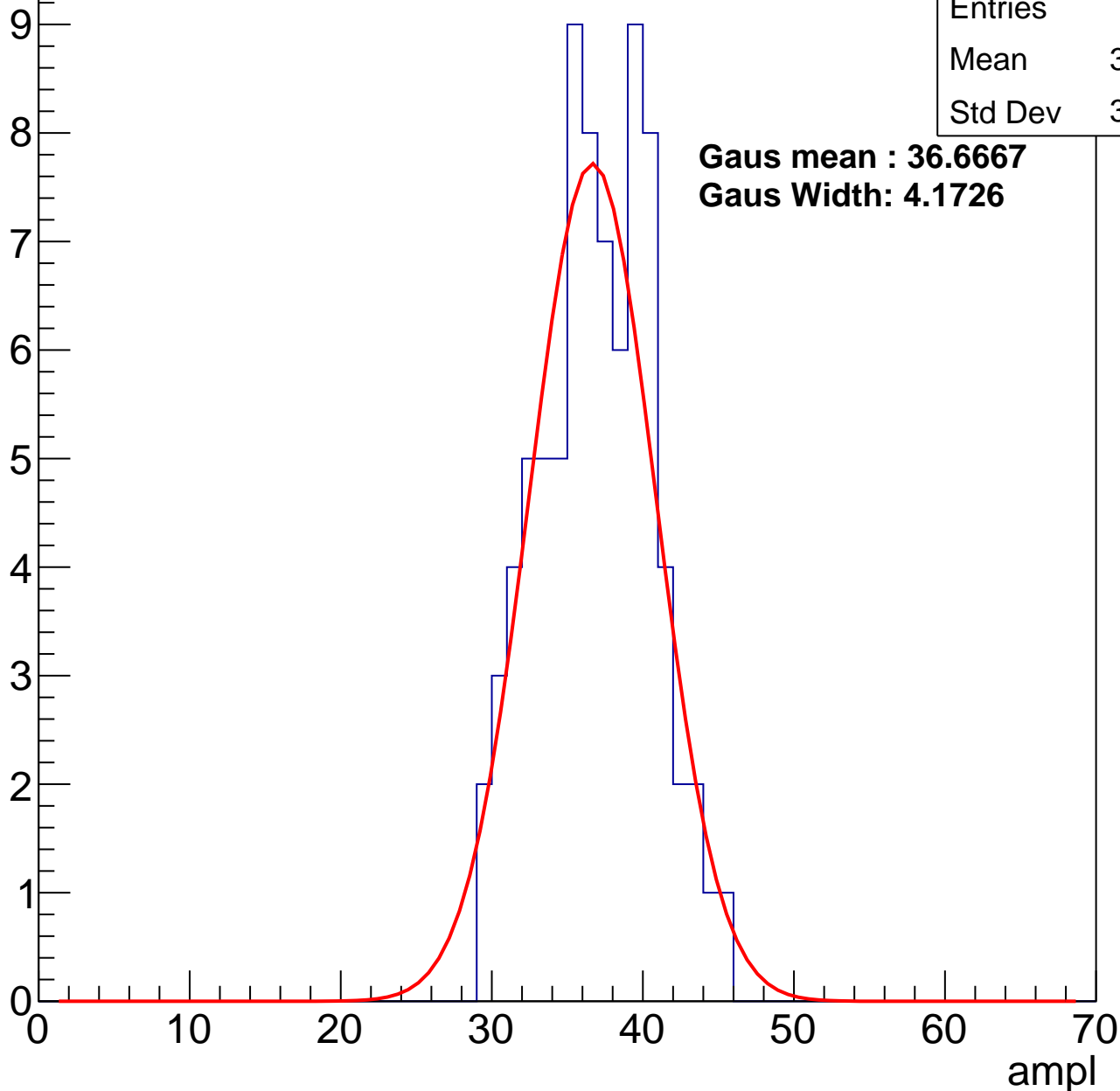
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	36.43
Std Dev	3.685

**Gaus mean : 36.6667**

**Gaus Width: 4.1726**



# B1L101S, U9-ch5, adc2

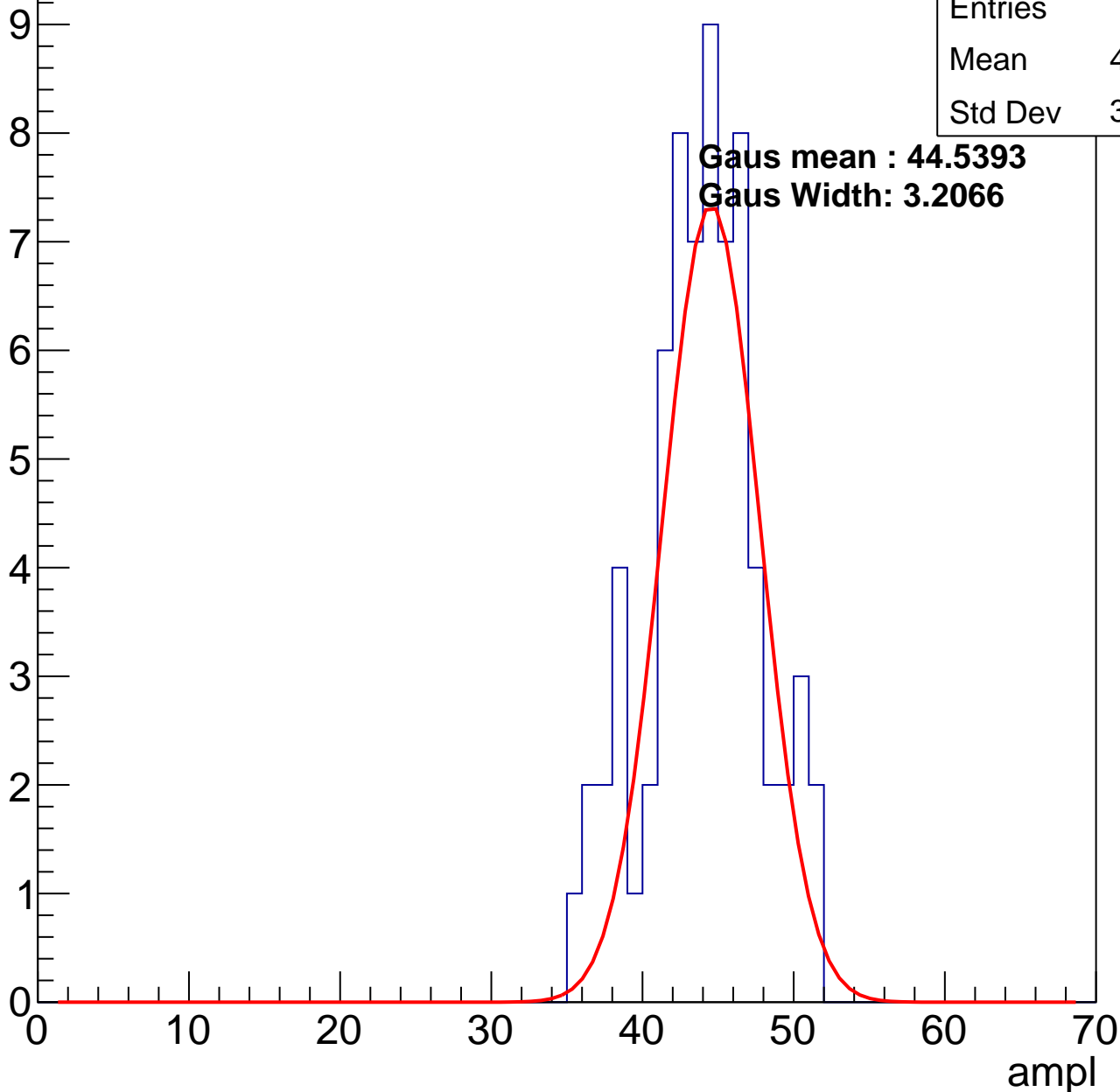
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	43.54
Std Dev	3.683

**Gaus mean : 44.5393**

**Gaus Width: 3.2066**

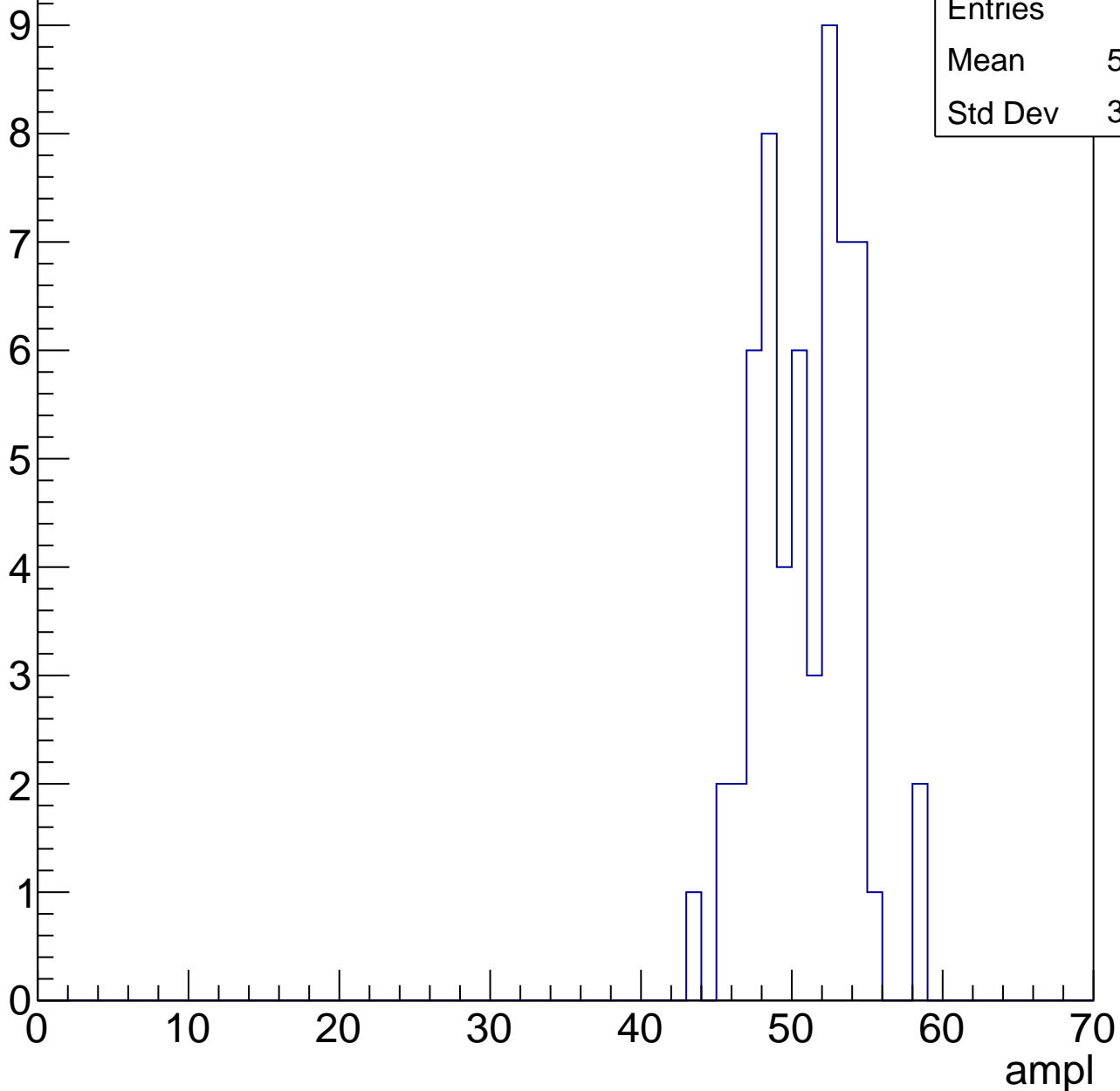


# B1L101S, U9-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	50.48
Std Dev	3.147

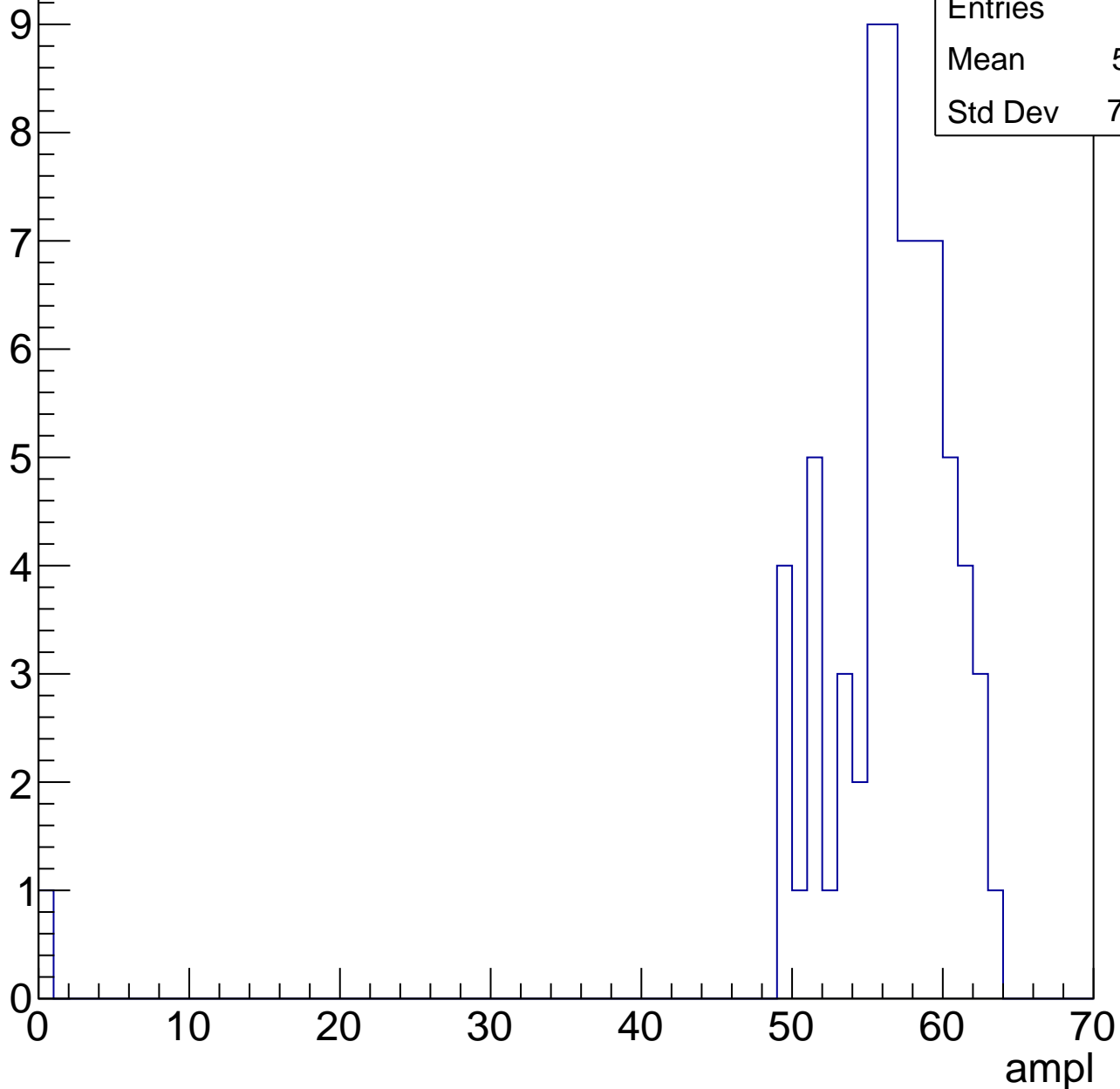


# B1L101S, U9-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	55.51
Std Dev	7.586

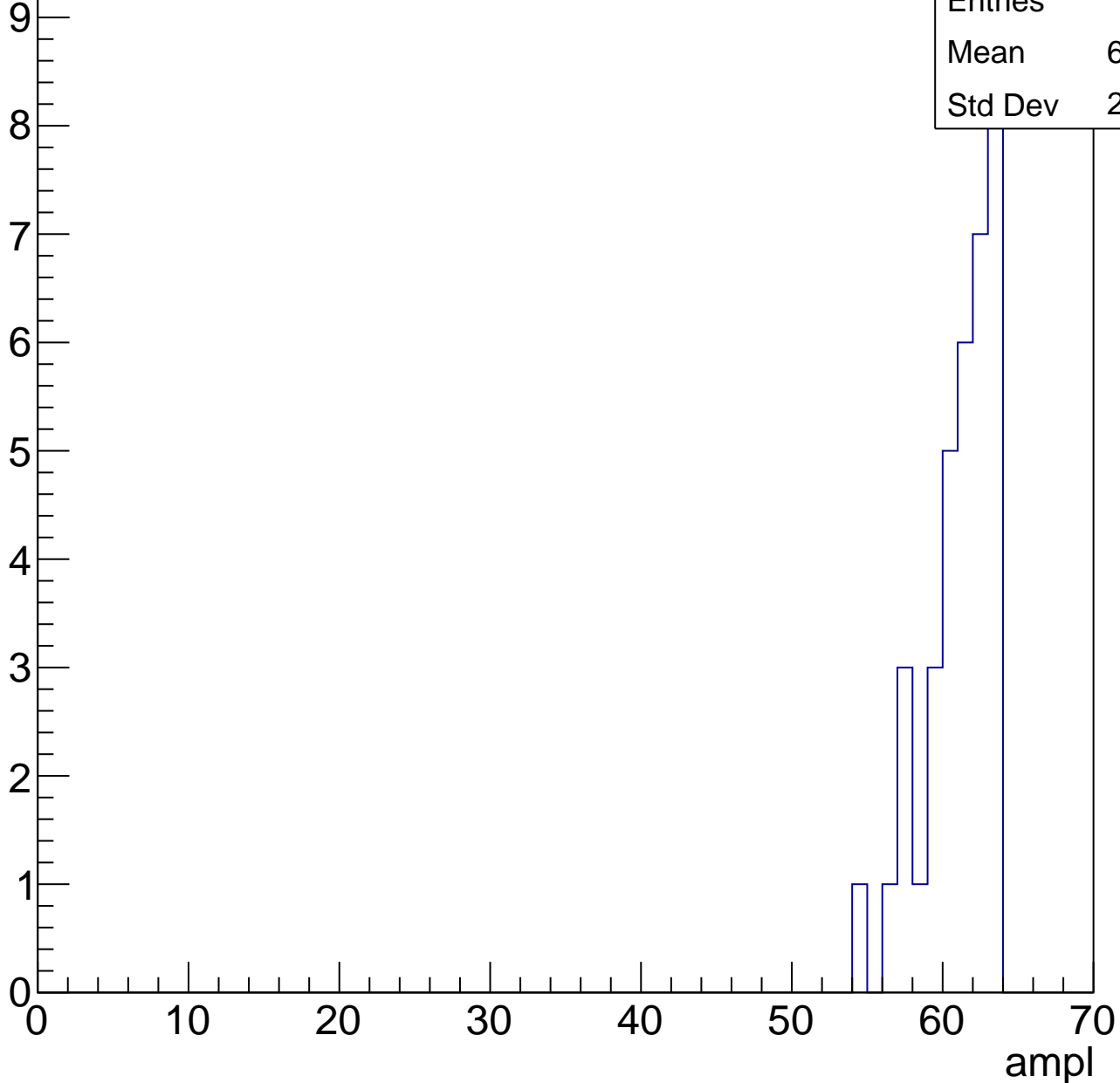


# B1L101S, U9-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	36
Mean	60.64
Std Dev	2.275



# B1L101S, U9-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L101S, U9-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U9-ch6, adc0

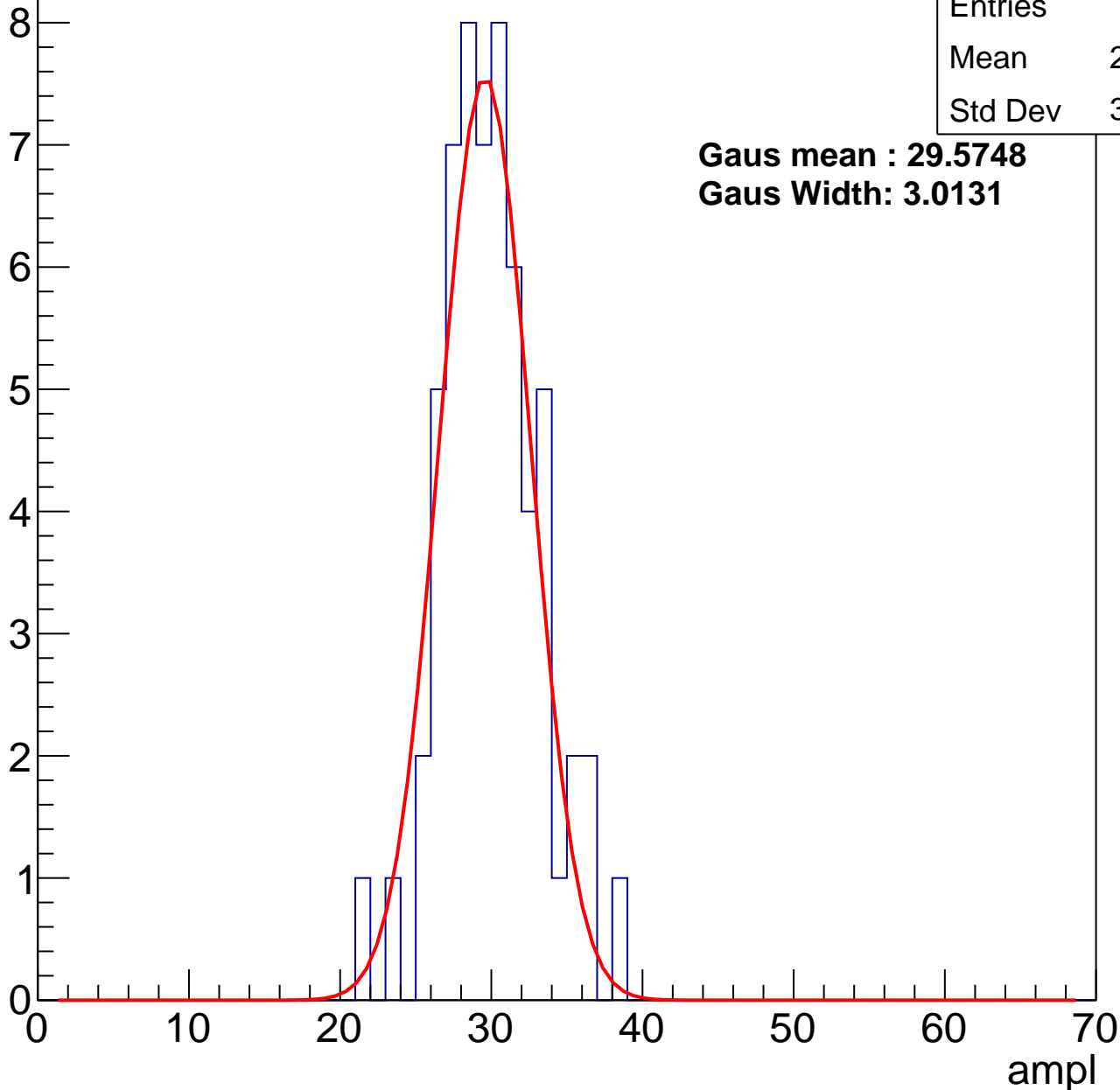
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	29.55
Std Dev	3.212

**Gaus mean : 29.5748**

**Gaus Width: 3.0131**



# B1L101S, U9-ch6, adc1

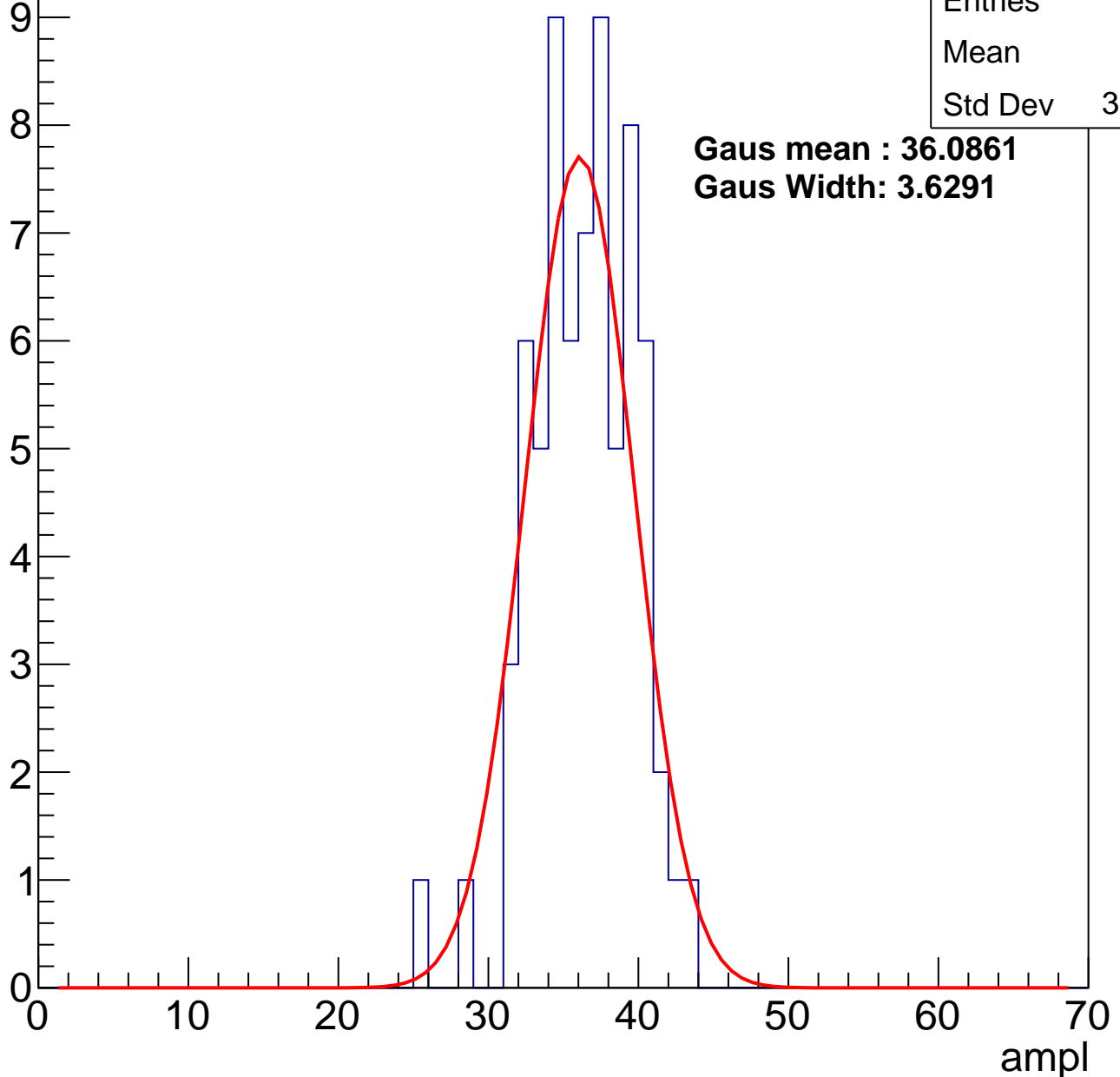
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	35.9
Std Dev	3.326

**Gaus mean : 36.0861**

**Gaus Width: 3.6291**



# B1L101S, U9-ch6, adc2

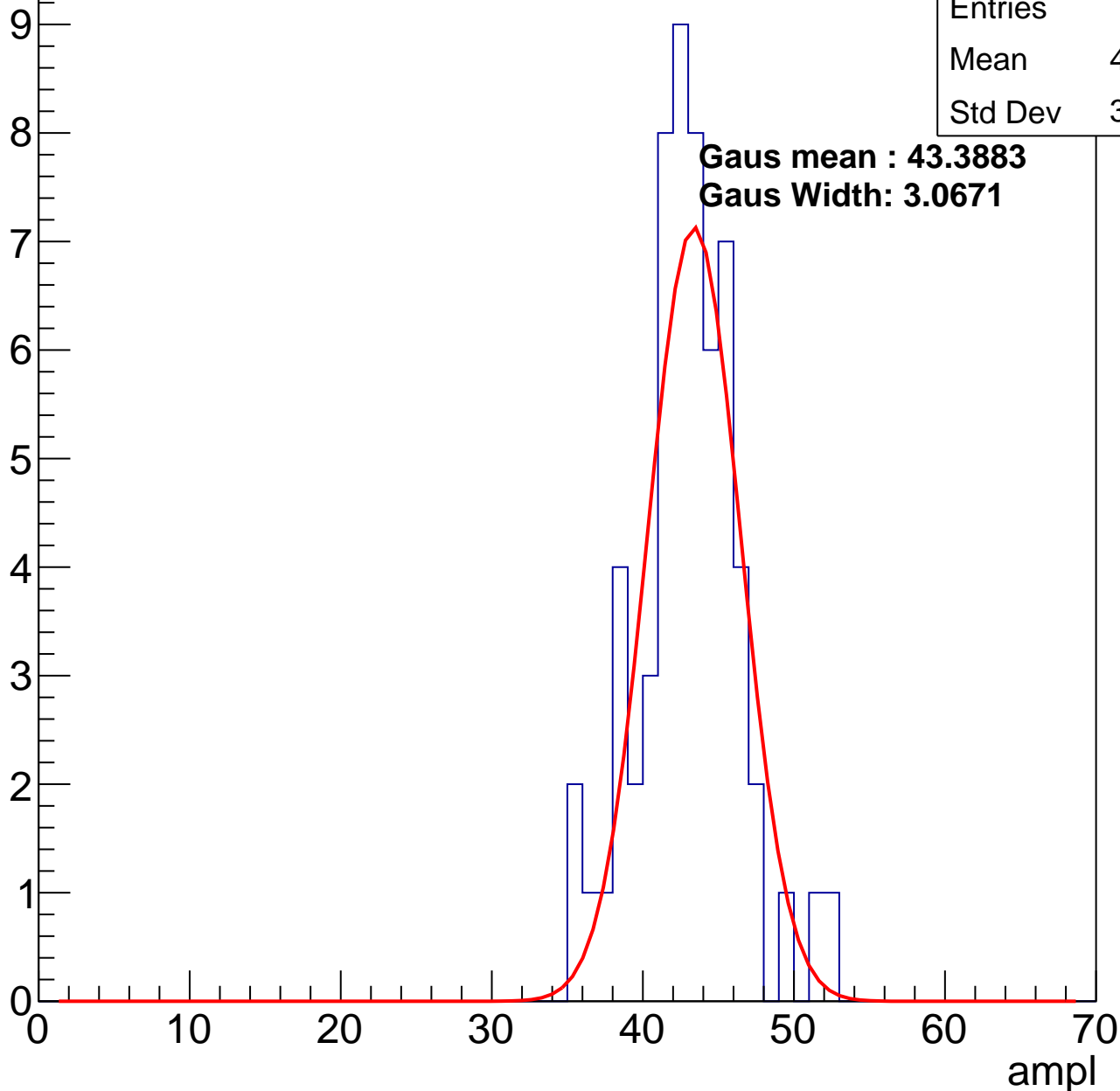
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	42.53
Std Dev	3.374

**Gaus mean : 43.3883**

**Gaus Width: 3.0671**

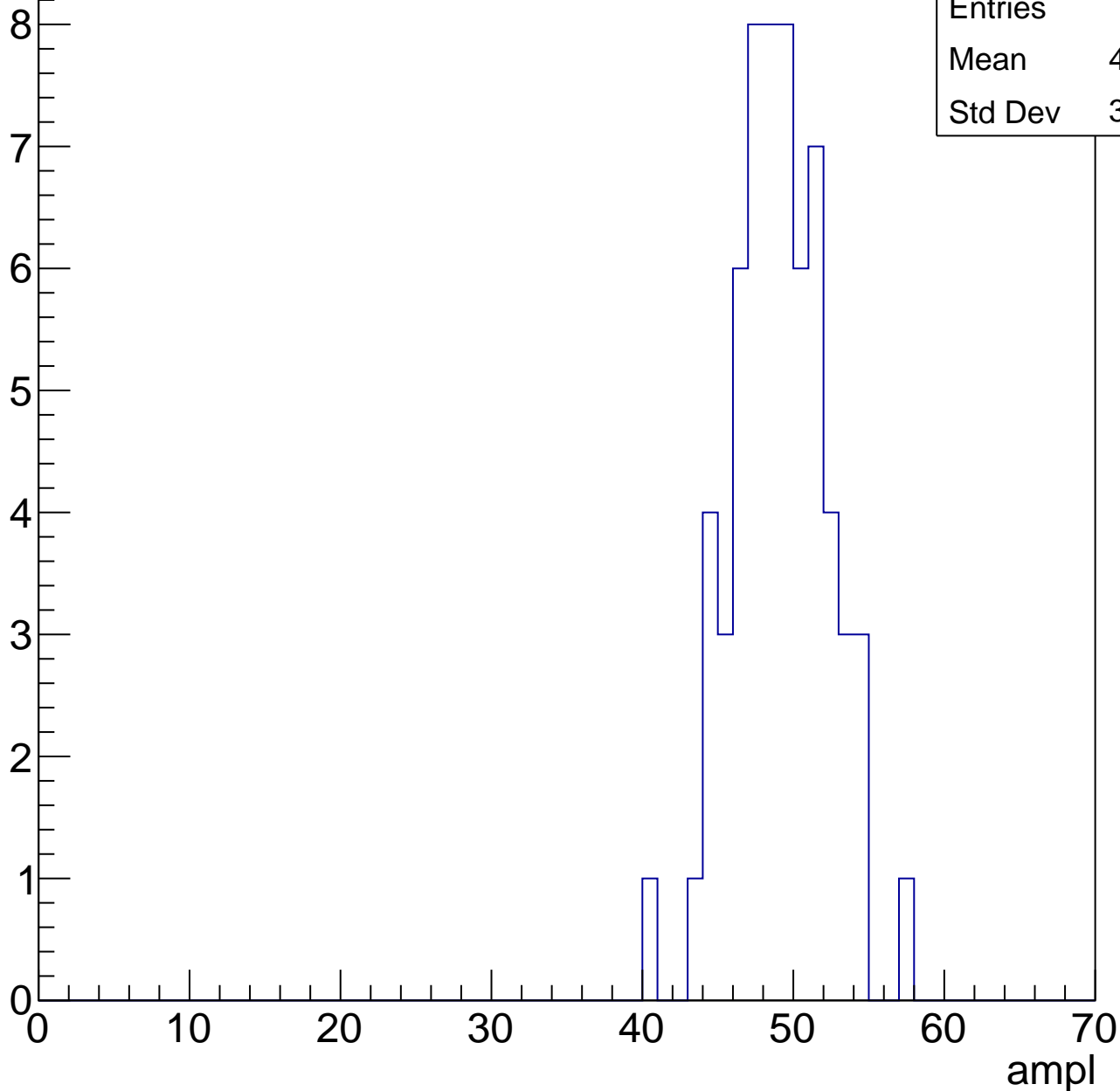


# B1L101S, U9-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	48.65
Std Dev	3.107

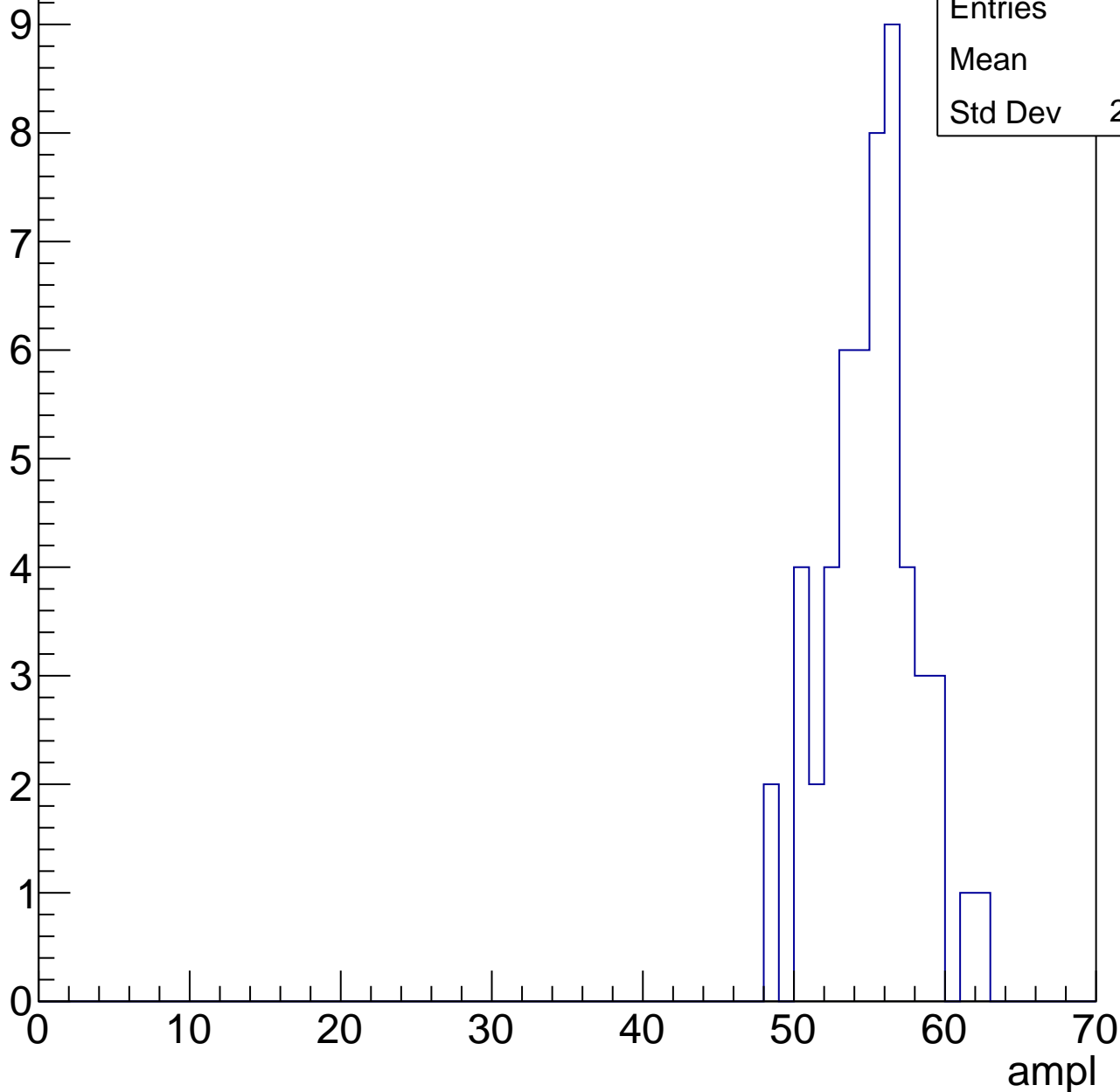


# B1L101S, U9-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	54.6
Std Dev	2.986



# B1L101S, U9-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

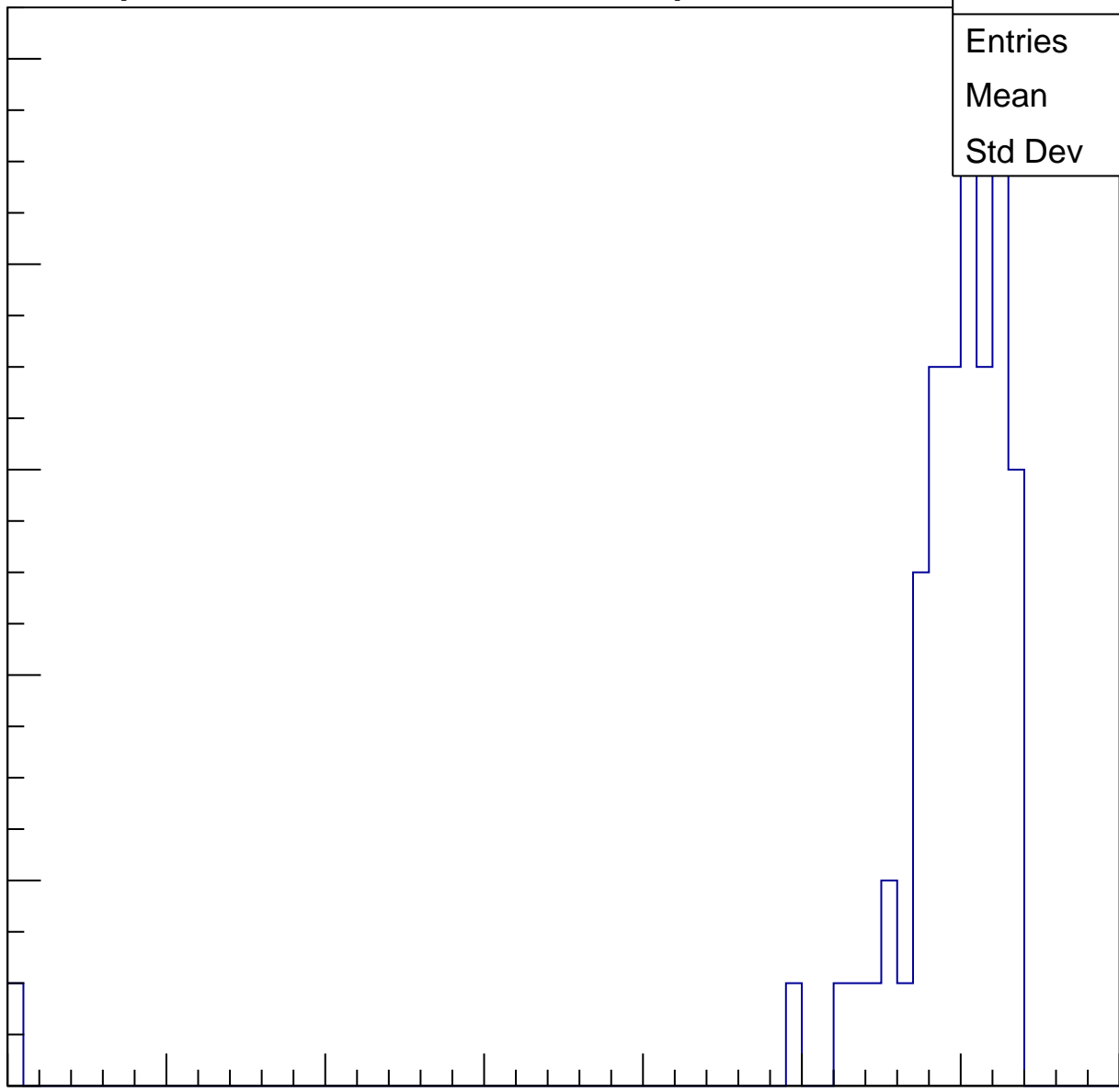
Entries	59
Mean	58.32
Std Dev	8.179

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

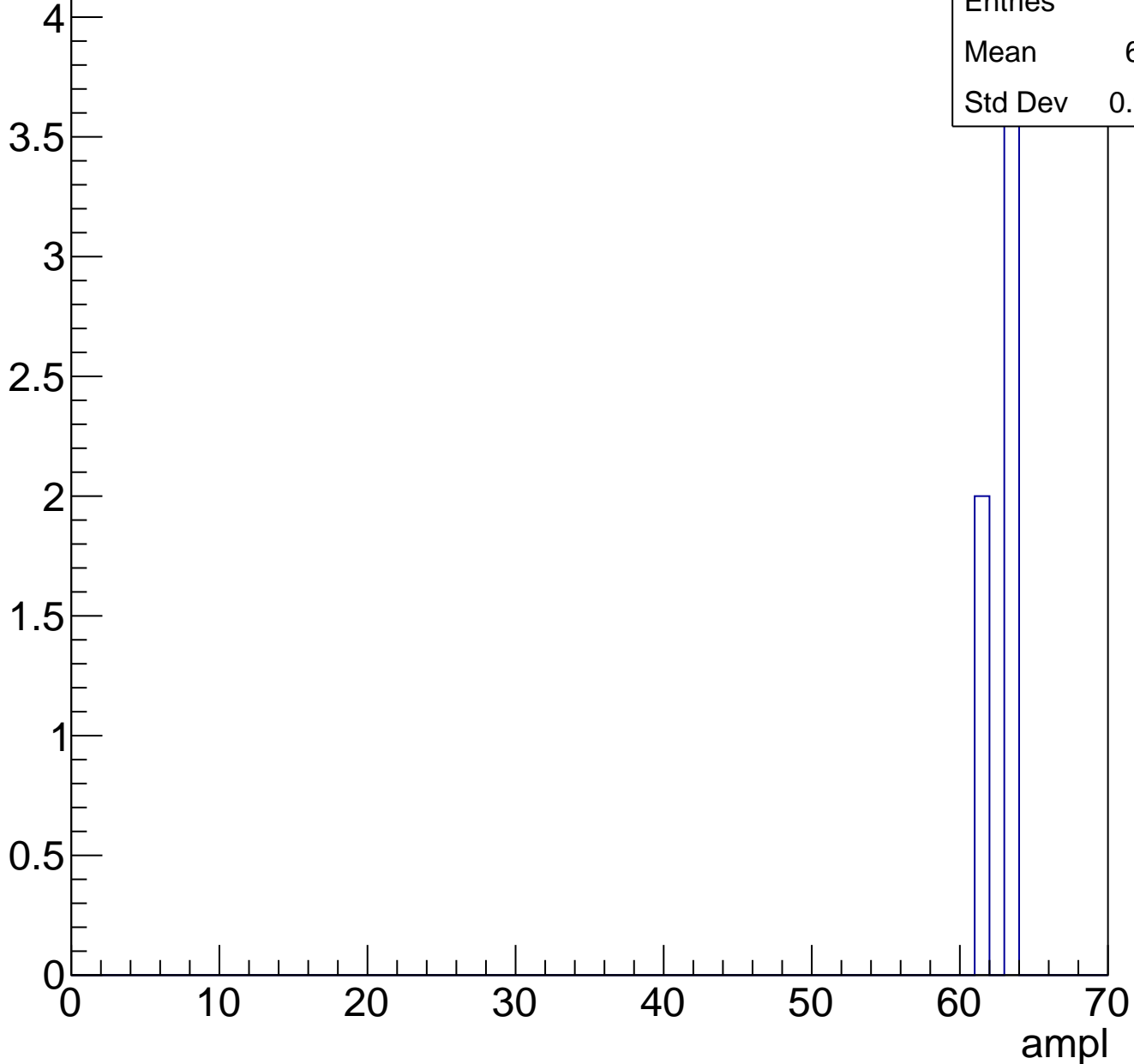
ampl



# B1L101S, U9-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch7, adc0

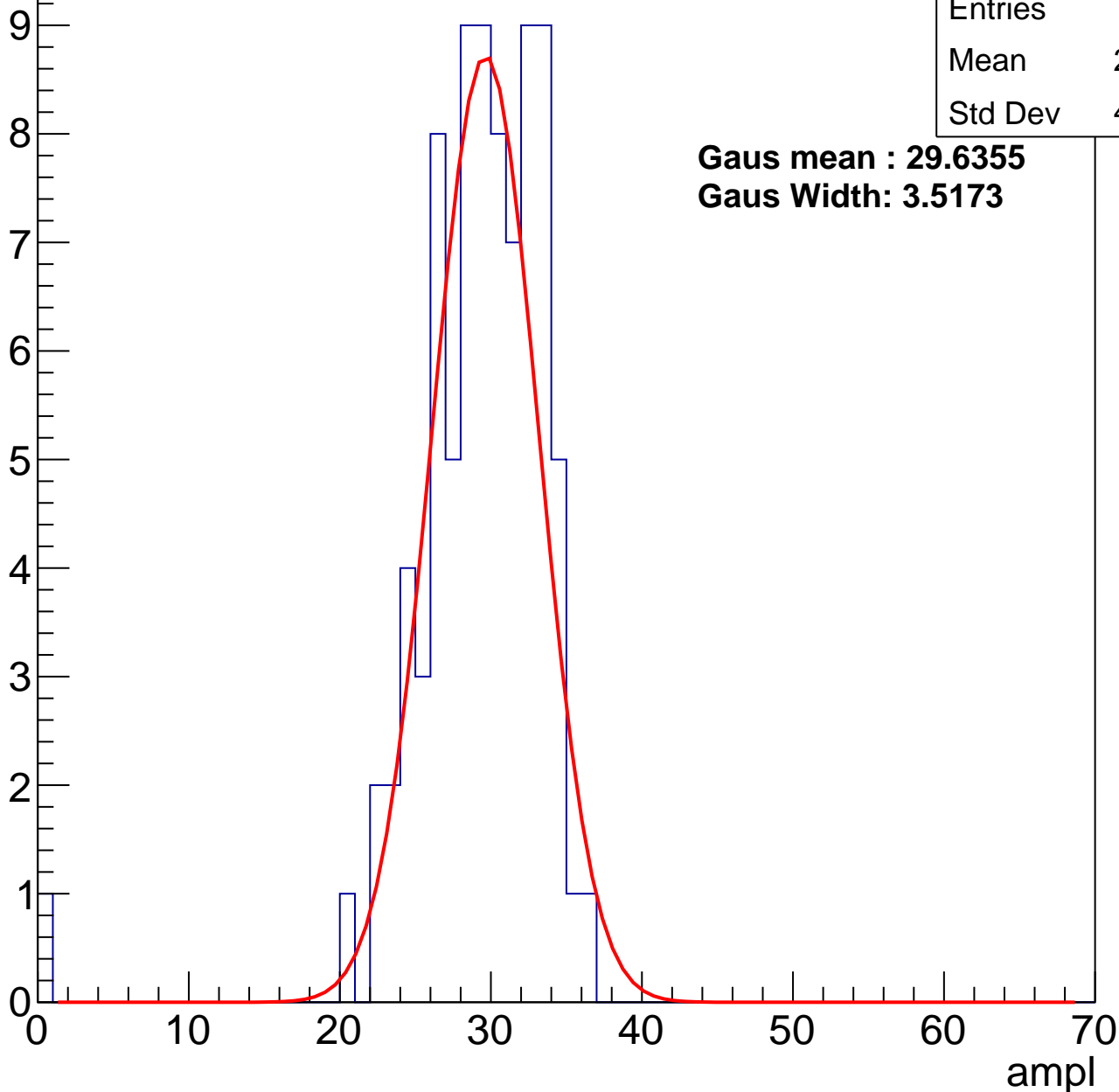
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	84
Mean	28.81
Std Dev	4.641

**Gaus mean : 29.6355**

**Gaus Width: 3.5173**



# B1L101S, U9-ch7, adc1

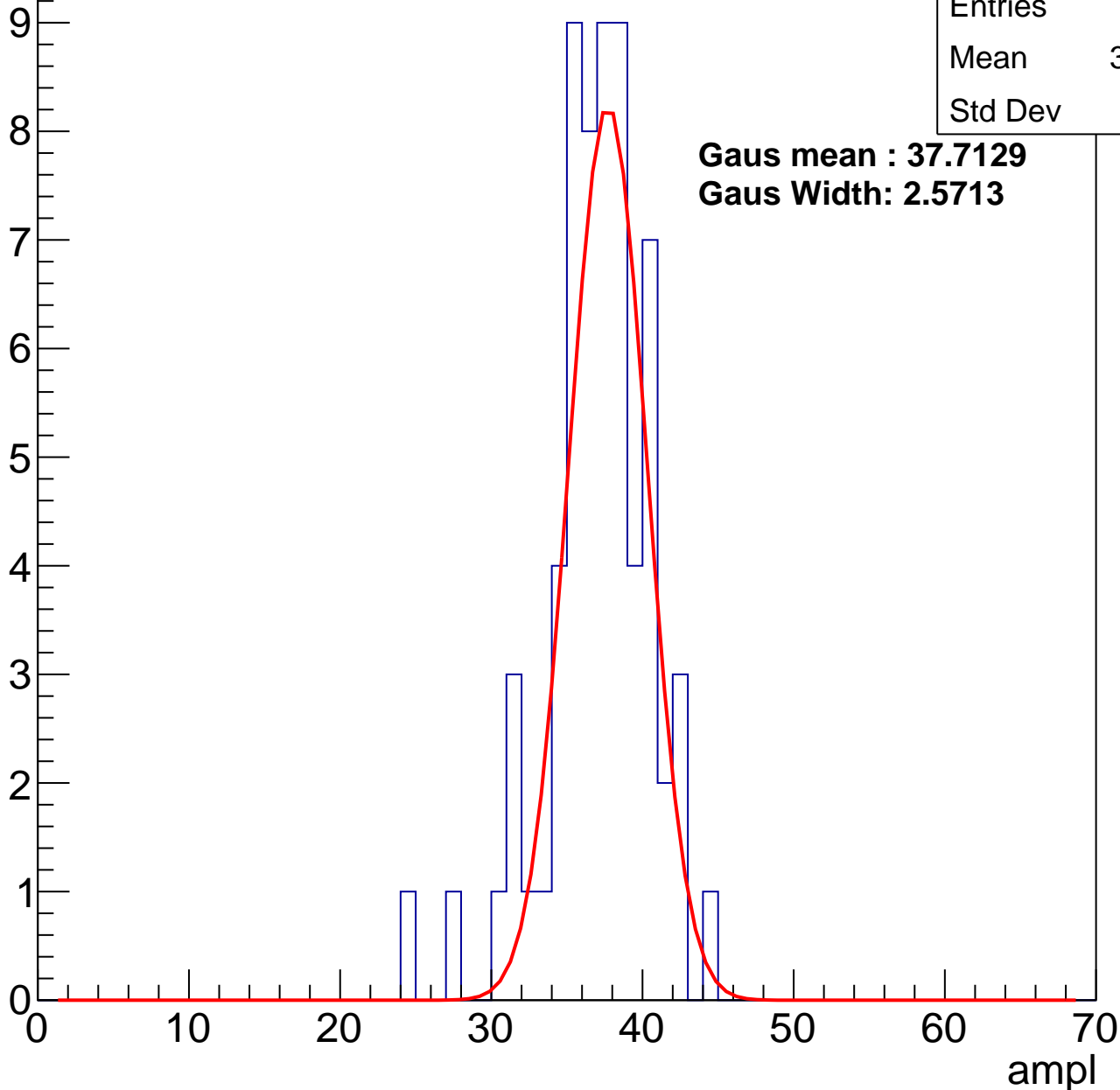
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	36.58
Std Dev	3.49

**Gaus mean : 37.7129**

**Gaus Width: 2.5713**



# B1L101S, U9-ch7, adc2

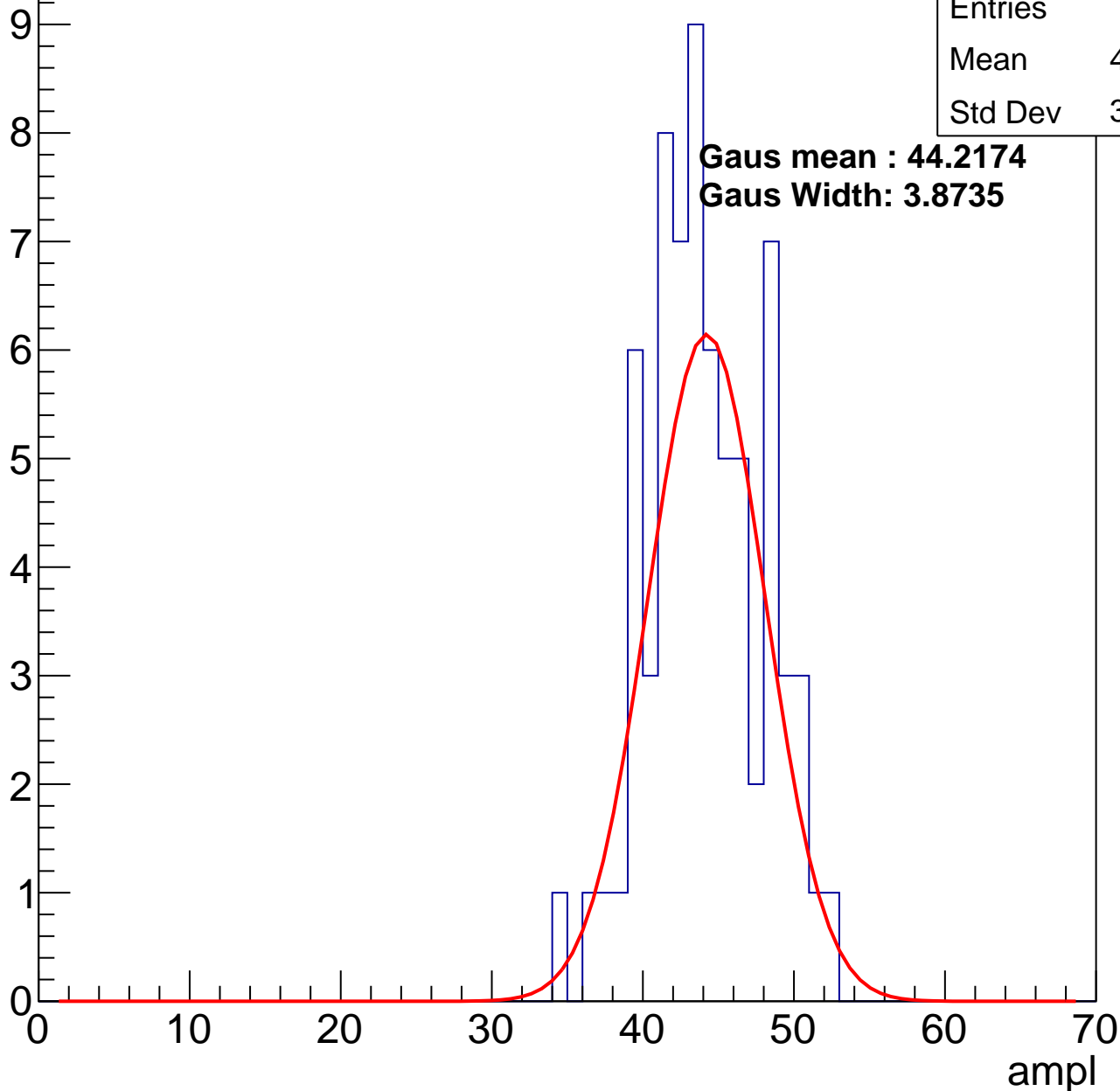
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	43.67
Std Dev	3.779

**Gaus mean : 44.2174**

**Gaus Width: 3.8735**

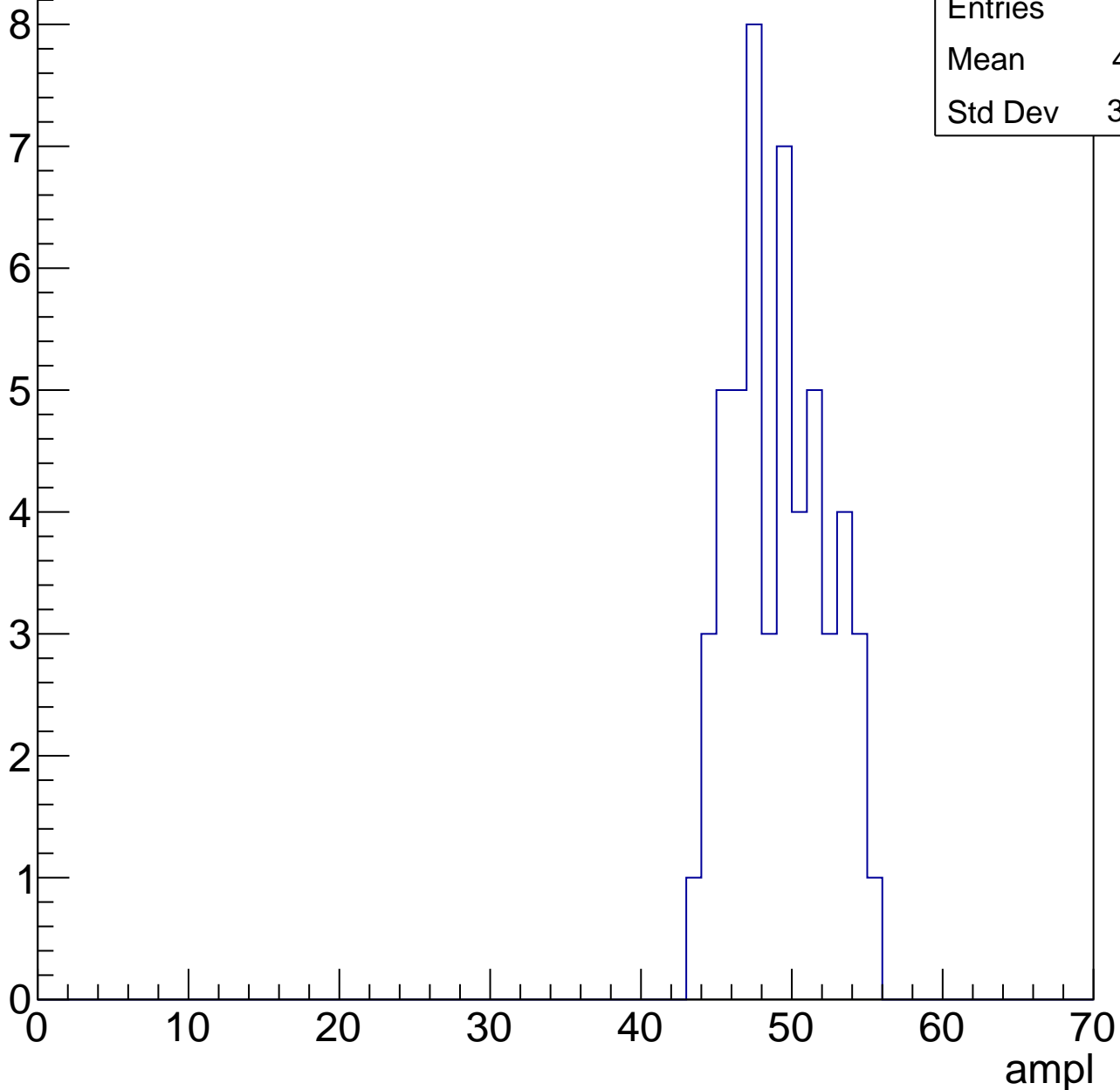


# B1L101S, U9-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	48.71
Std Dev	3.078



# B1L101S, U9-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

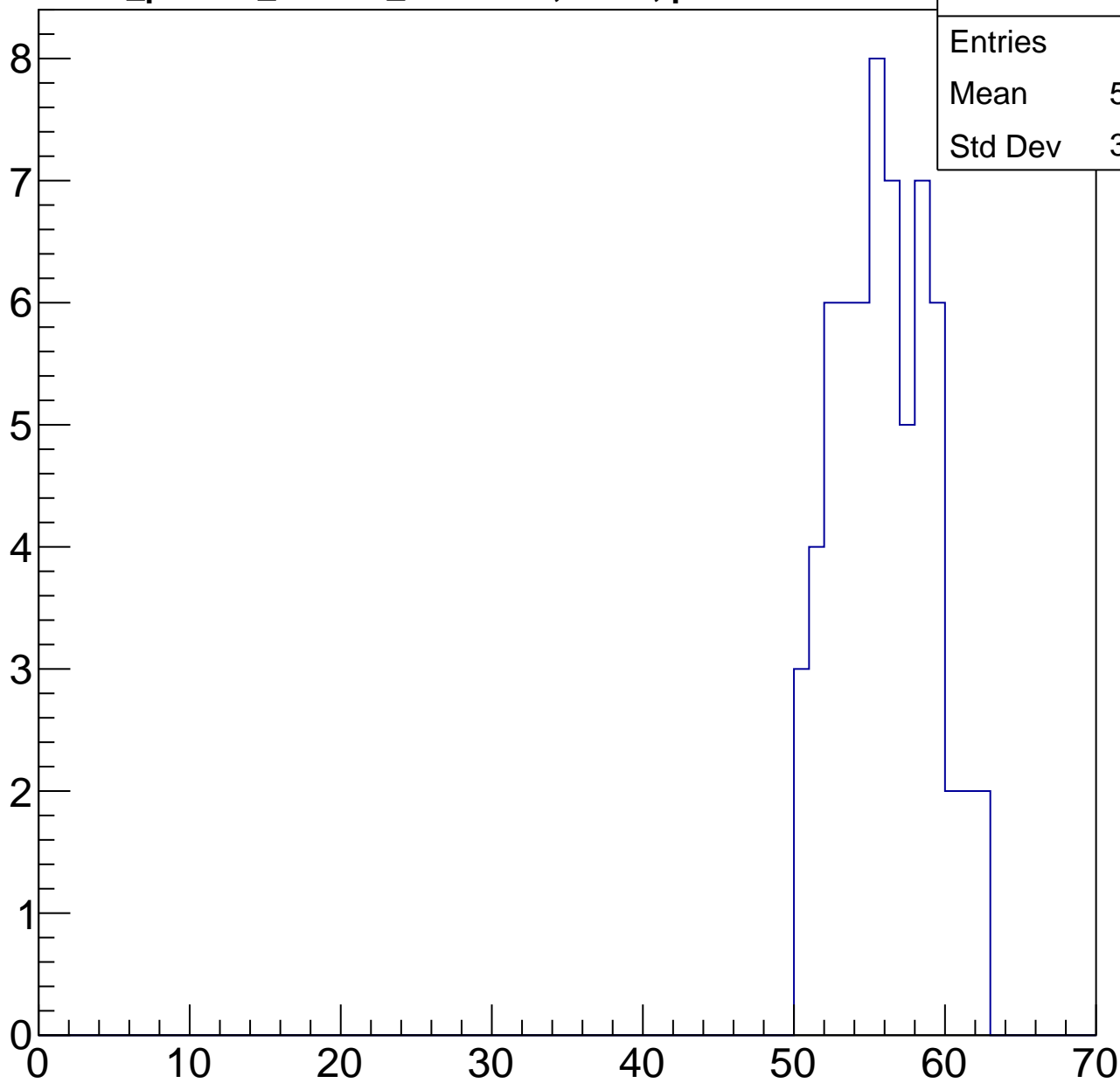
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	64
Mean	55.48
Std Dev	3.097

ampl

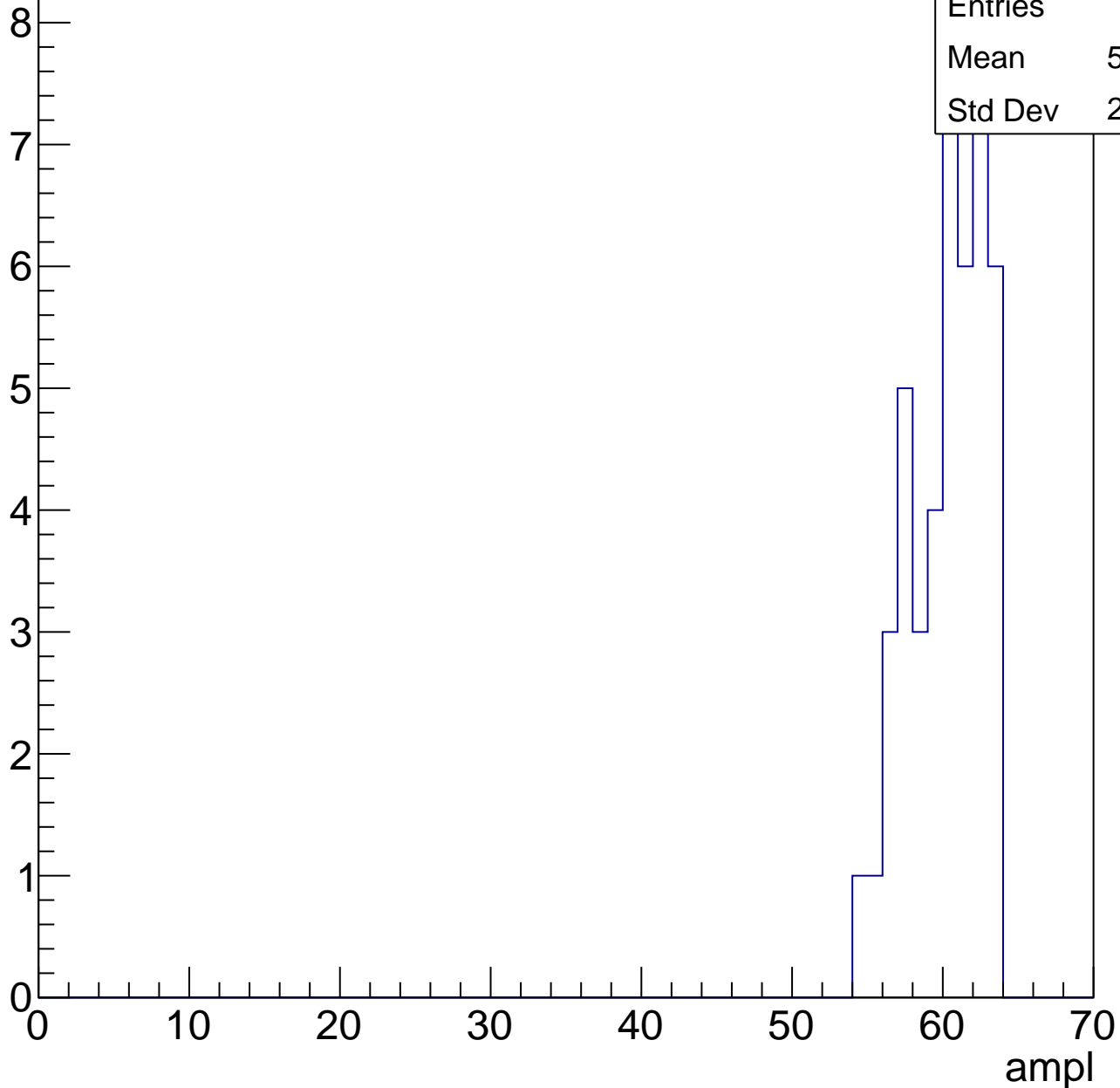
0 10 20 30 40 50 60 70



# B1L101S, U9-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

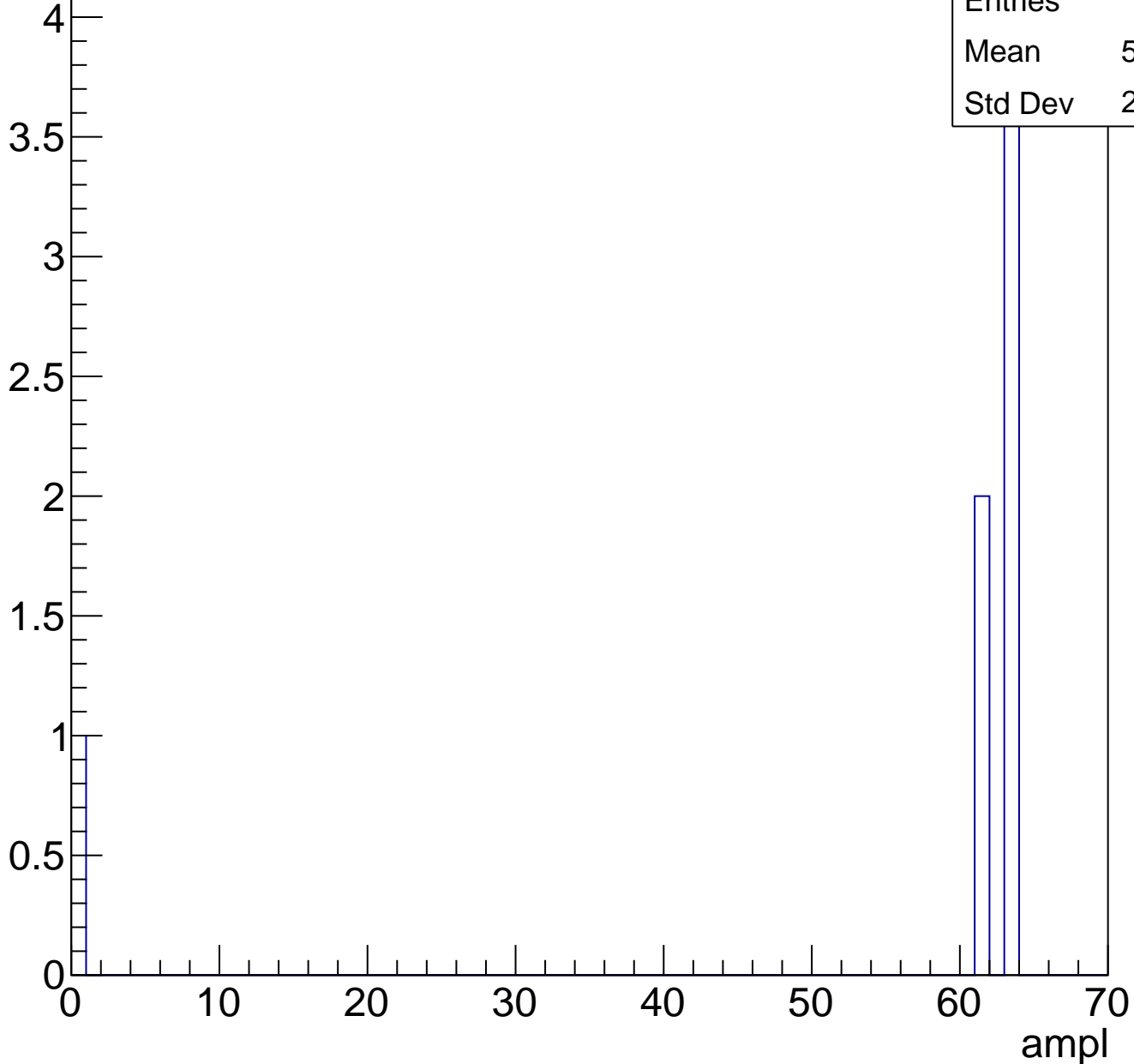
Entry



# B1L101S, U9-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U9-ch8, adc0

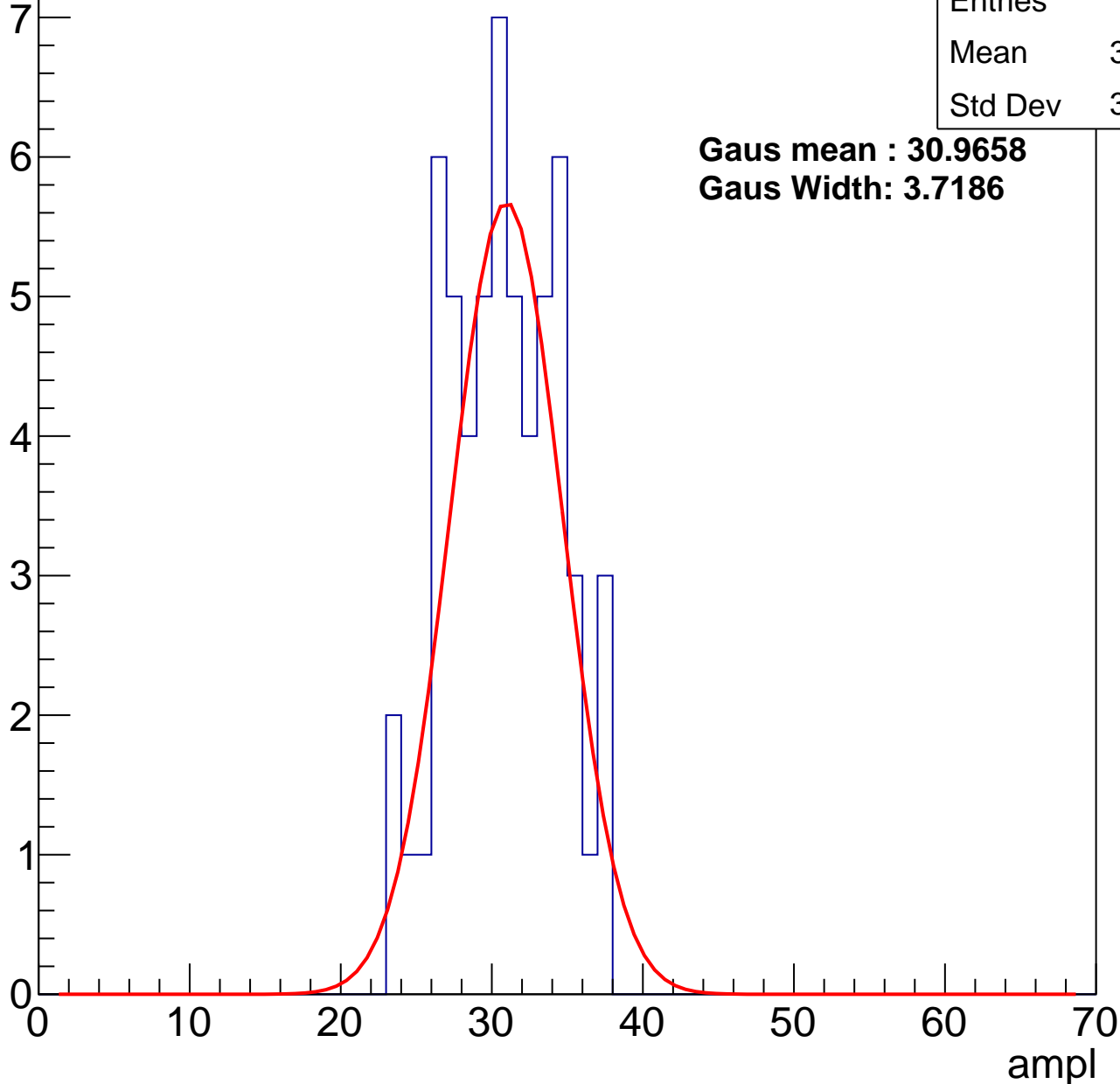
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	30.29
Std Dev	3.562

**Gaus mean : 30.9658**

**Gaus Width: 3.7186**



# B1L101S, U9-ch8, adc1

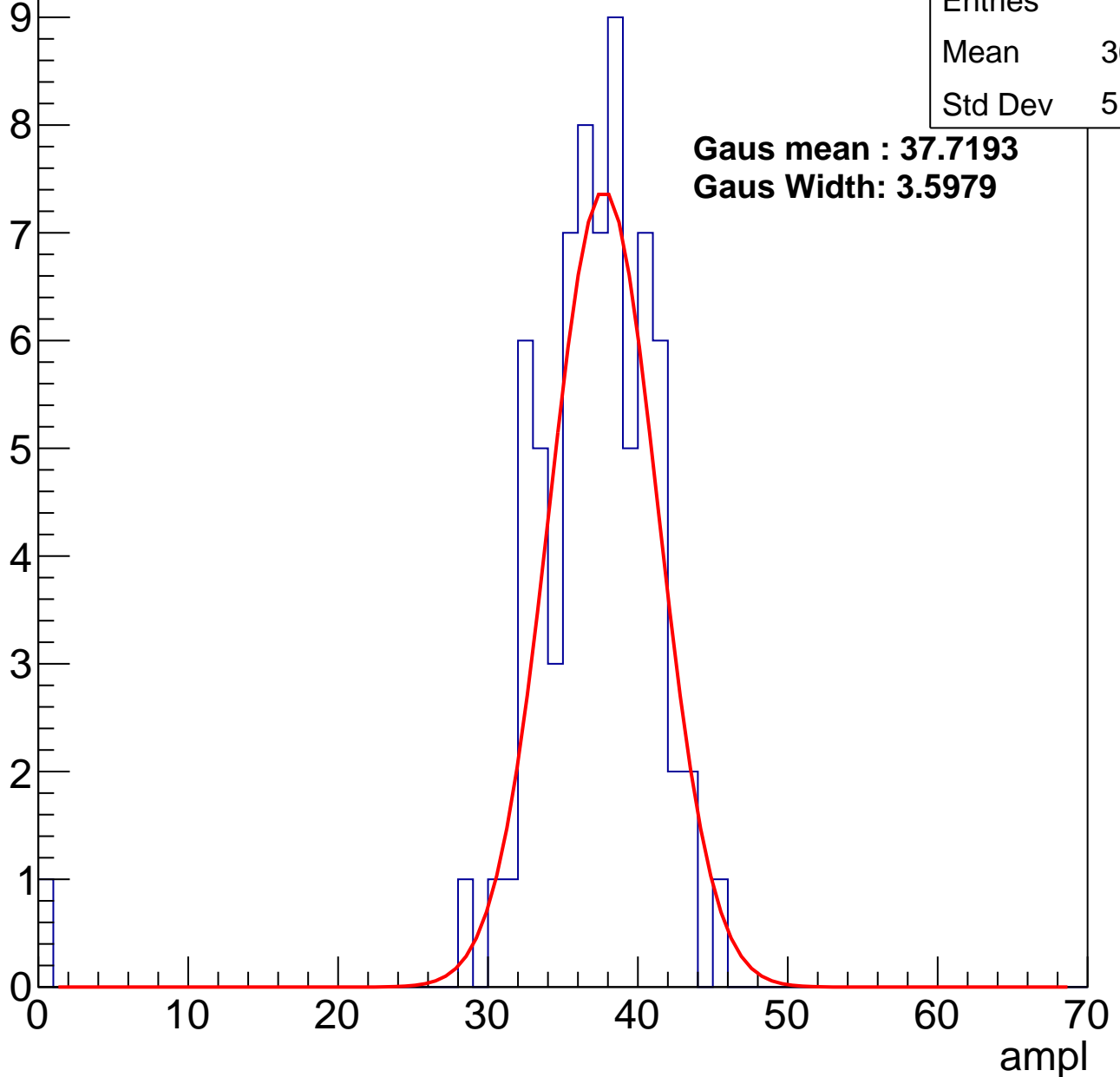
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	36.36
Std Dev	5.493

**Gaus mean : 37.7193**

**Gaus Width: 3.5979**



# B1L101S, U9-ch8, adc2

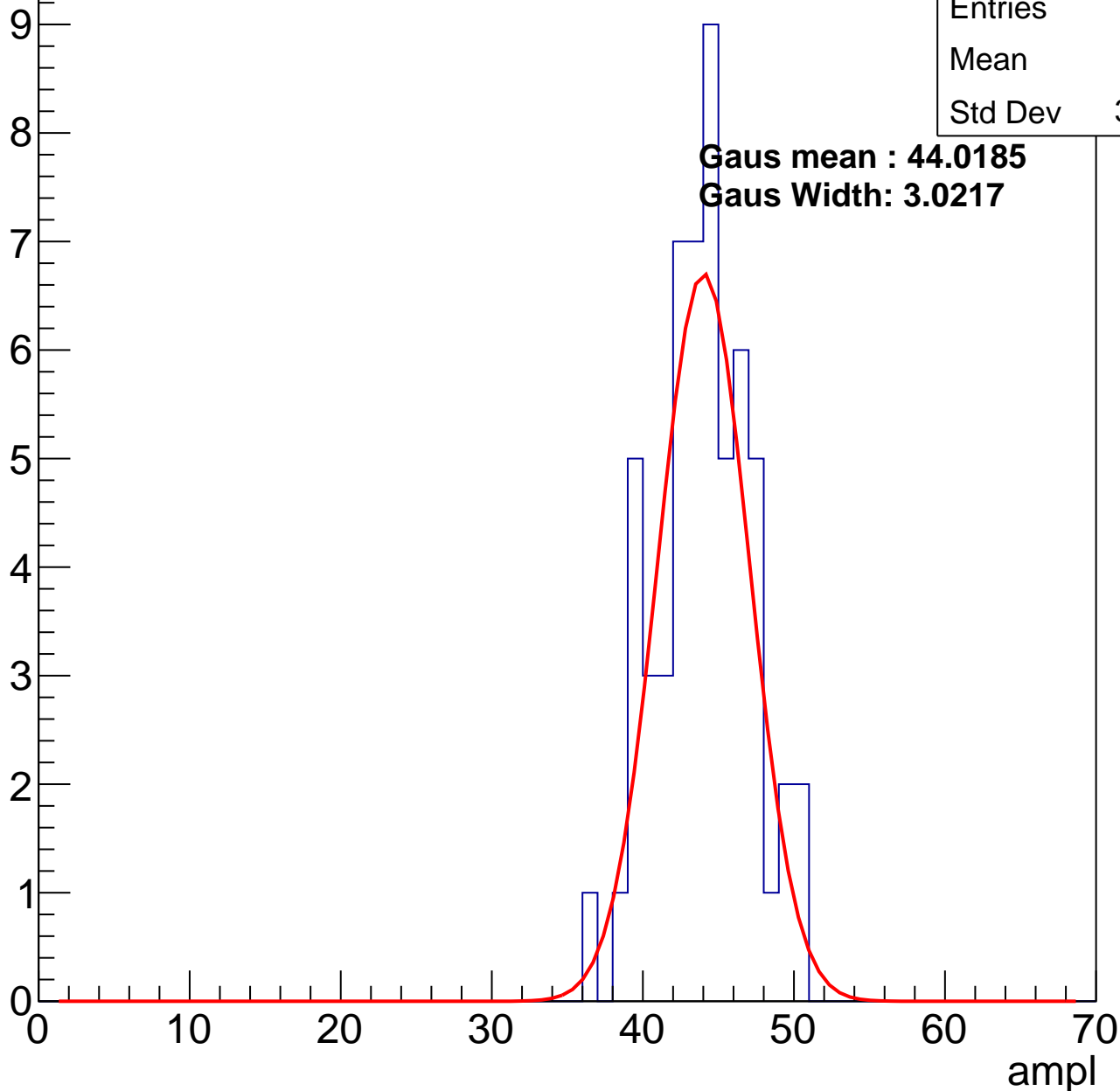
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	43.6
Std Dev	3.071

**Gaus mean : 44.0185**

**Gaus Width: 3.0217**

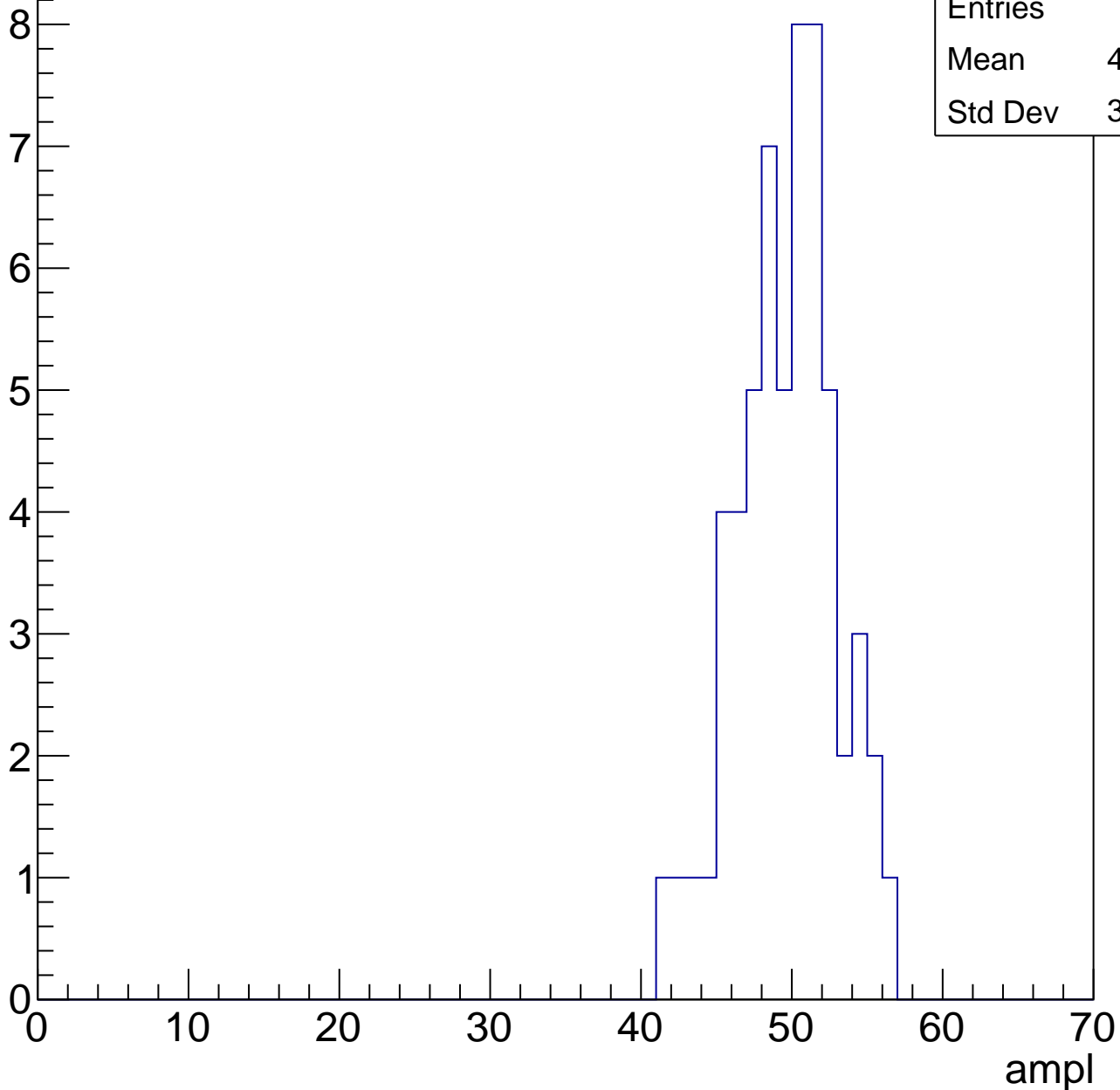


# B1L101S, U9-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

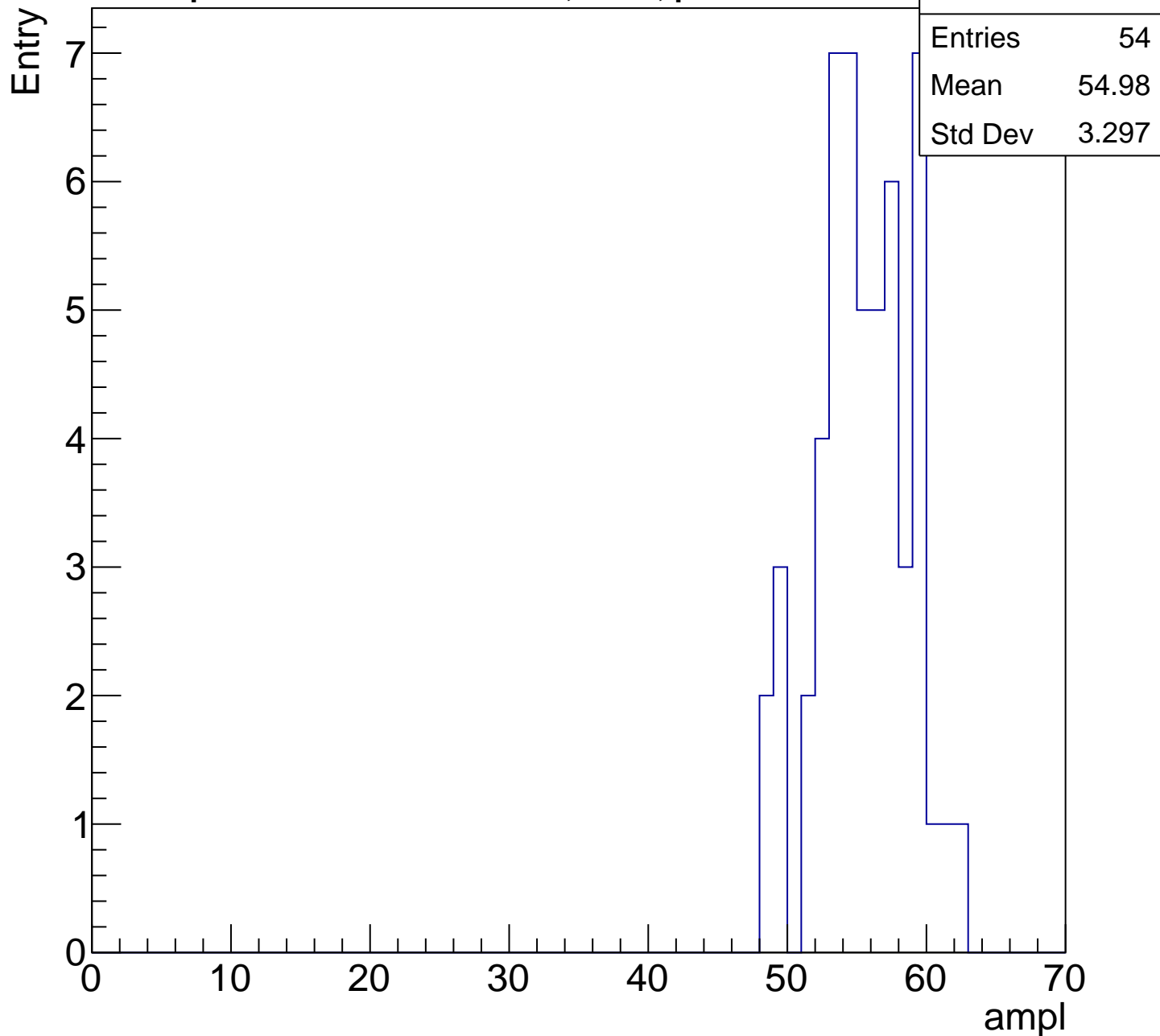
Entry

Entries	58
Mean	49.17
Std Dev	3.249



# B1L101S, U9-ch8, adc4

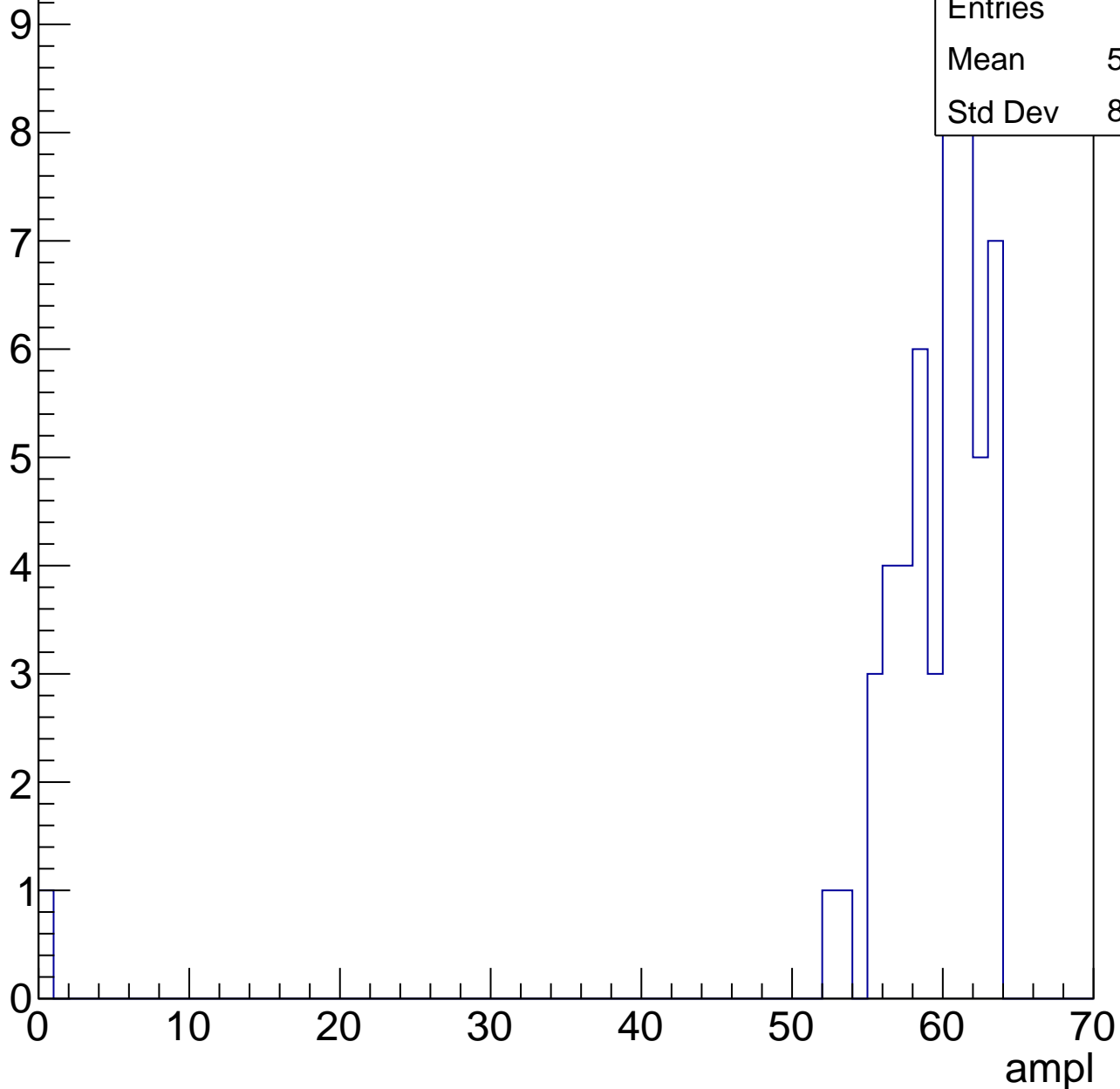
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

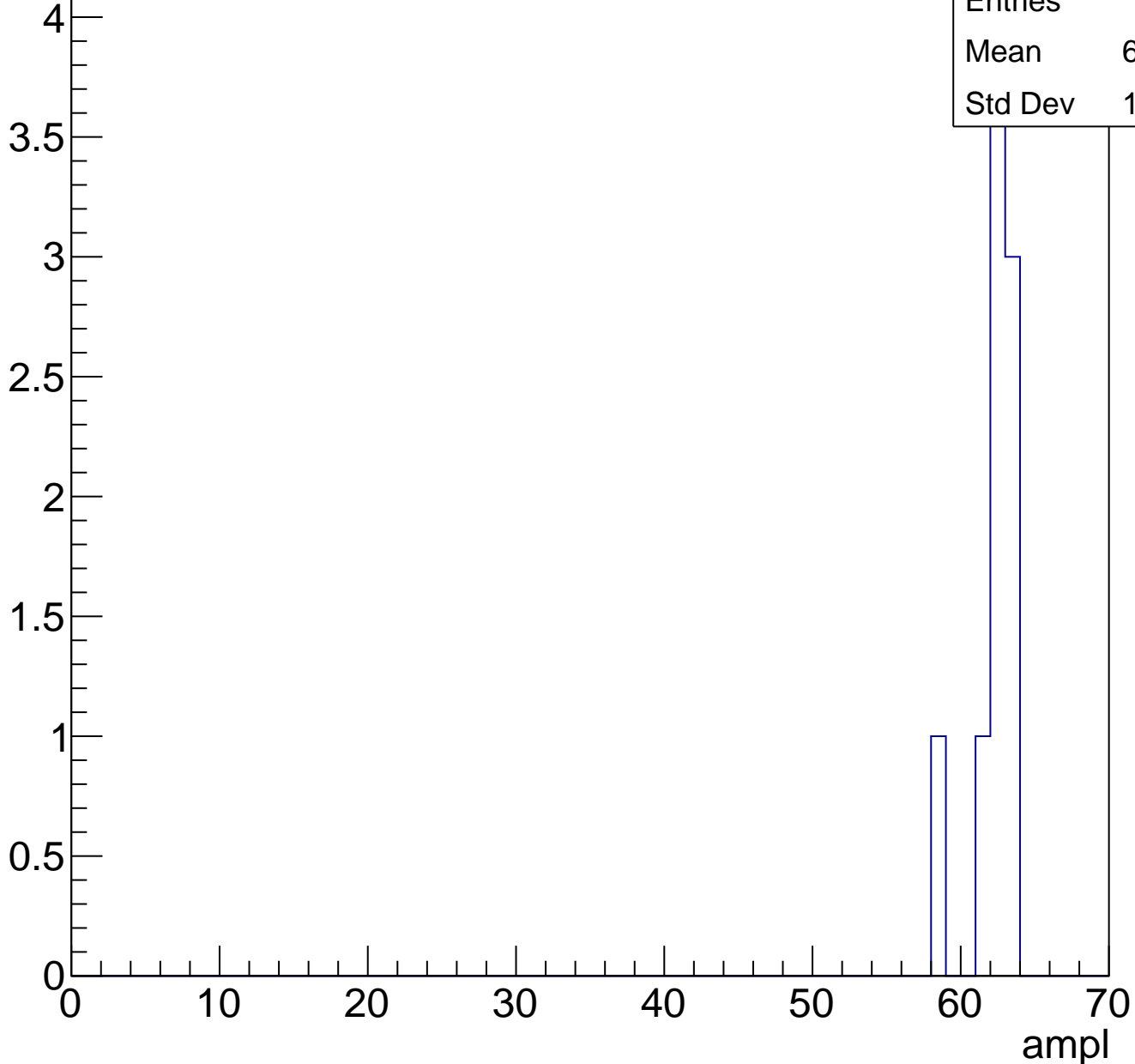
Entry



# B1L101S, U9-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



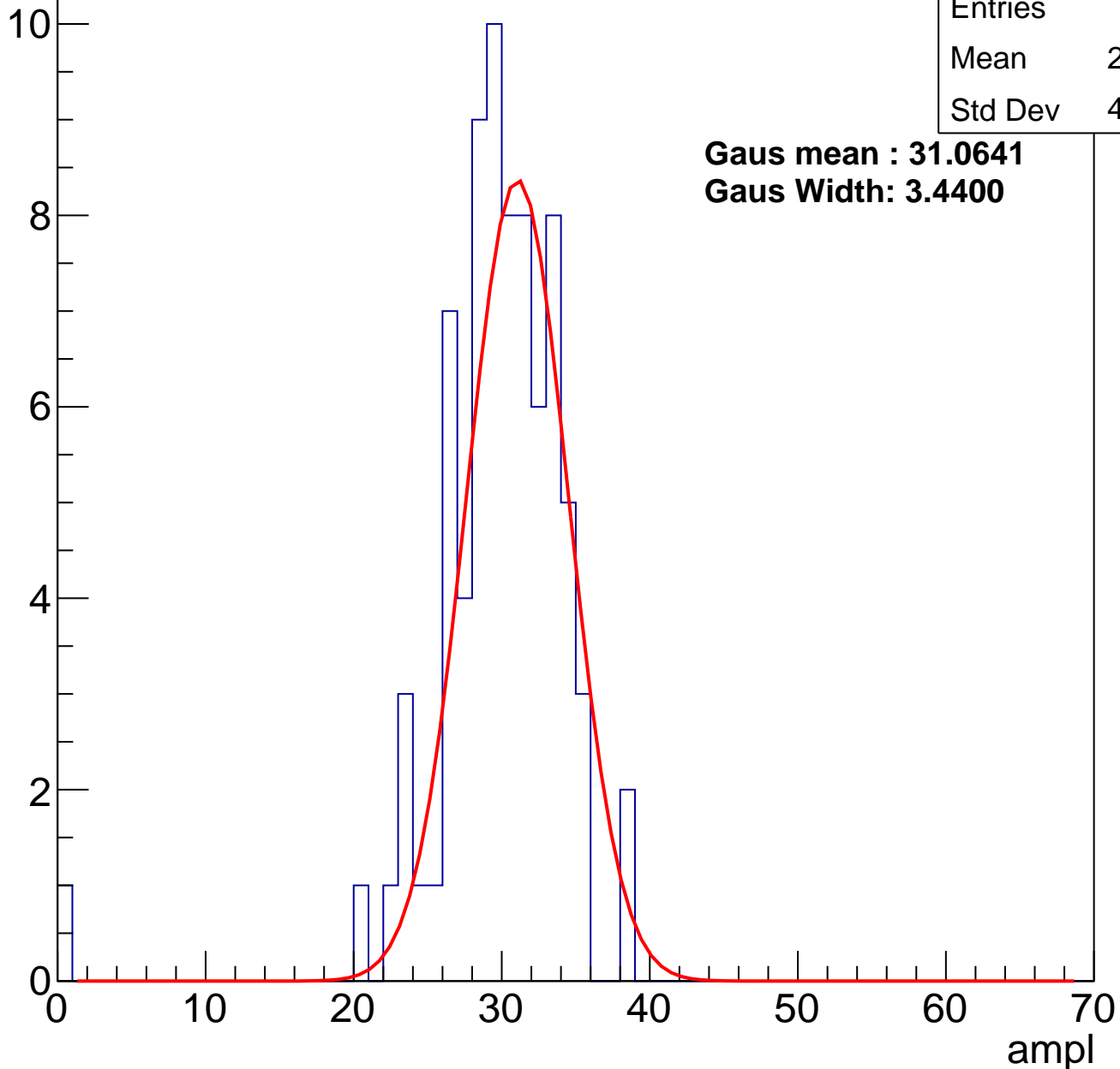
# B1L101S, U9-ch9, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	78
Mean	29.32
Std Dev	4.826

**Gaus mean : 31.0641**  
**Gaus Width: 3.4400**

Entry



# B1L101S, U9-ch9, adc1

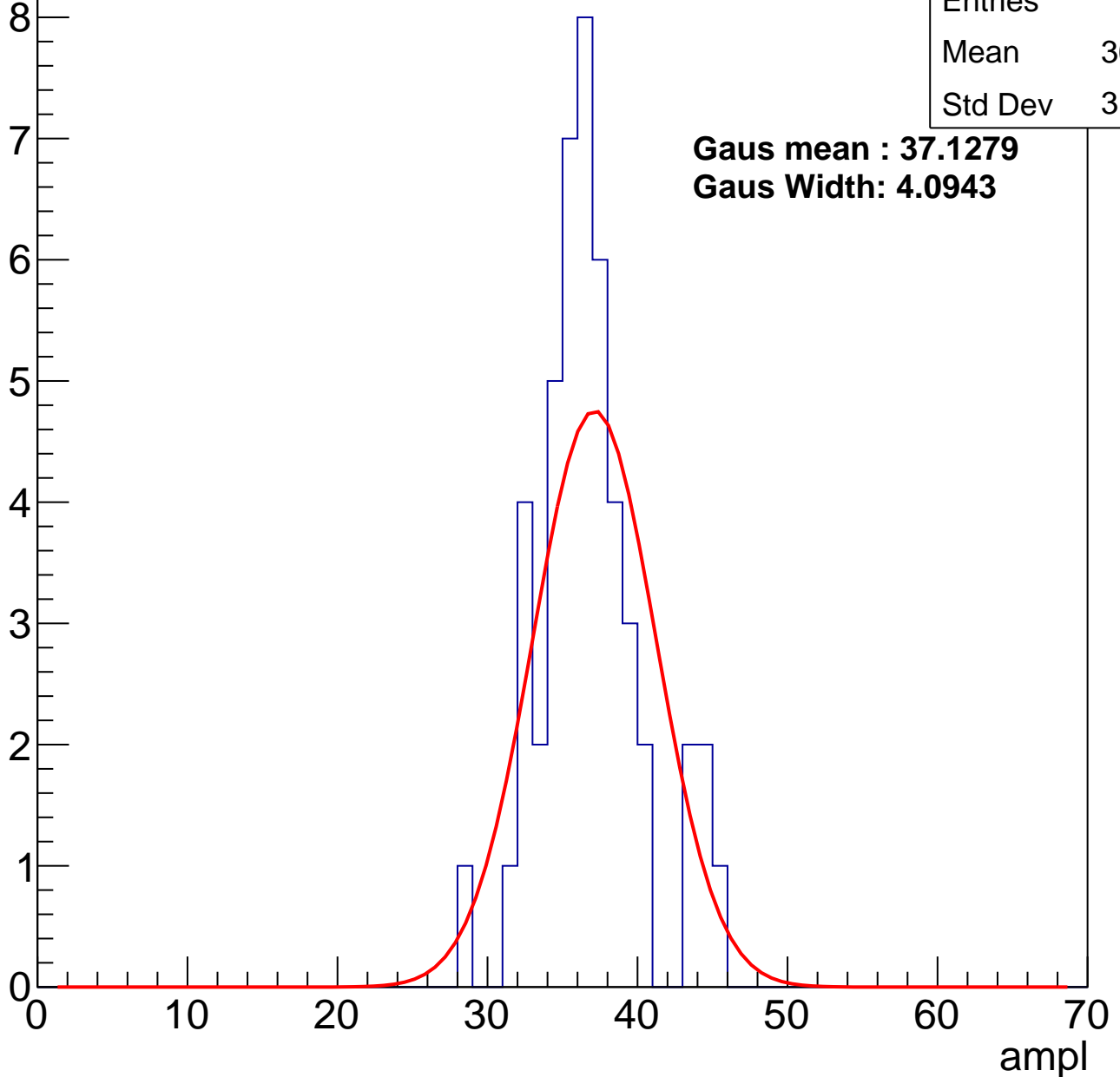
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	36.38
Std Dev	3.474

**Gaus mean : 37.1279**

**Gaus Width: 4.0943**



# B1L101S, U9-ch9, adc2

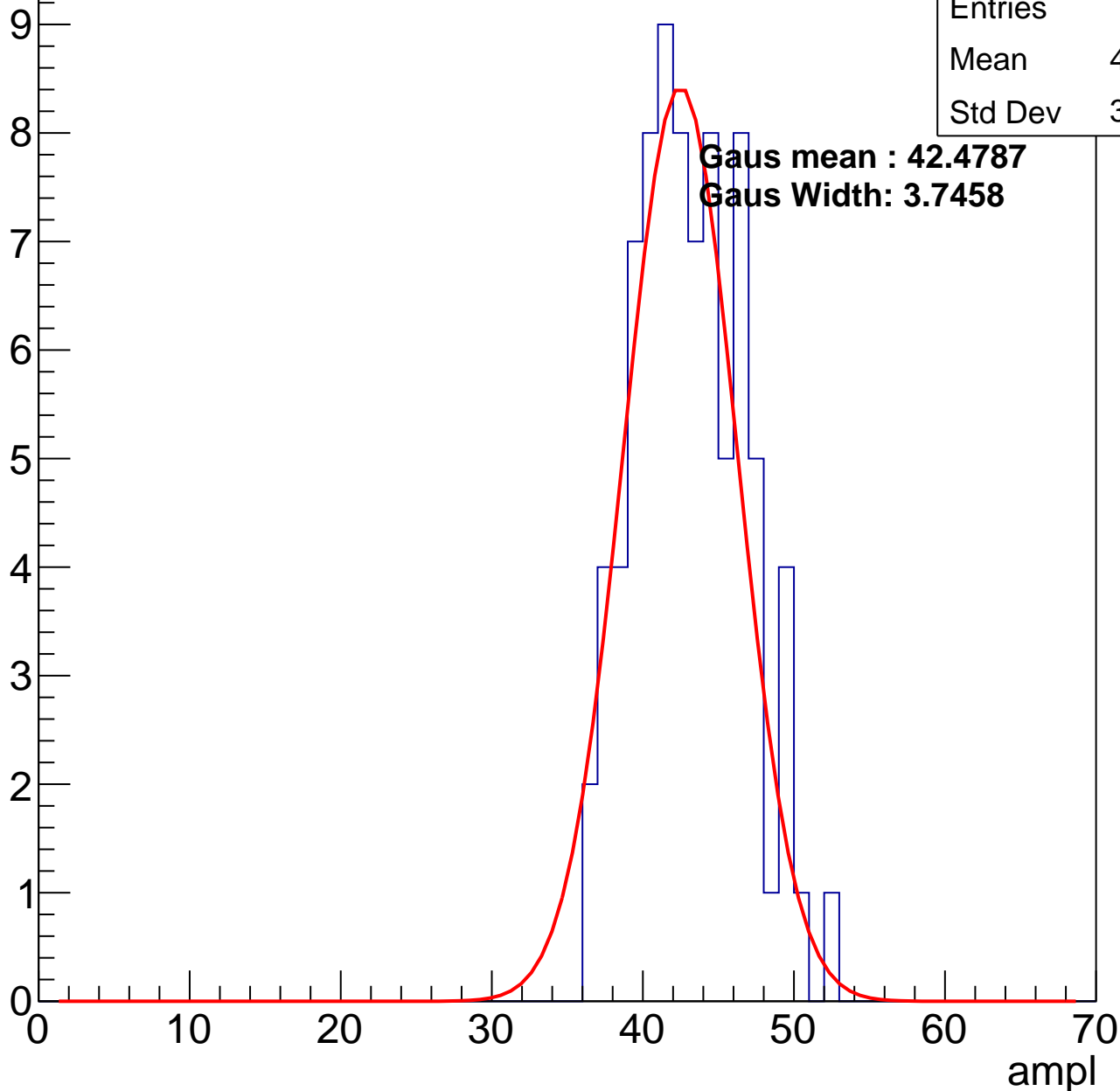
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	42.65
Std Dev	3.559

**Gaus mean : 42.4787**

**Gaus Width: 3.7458**

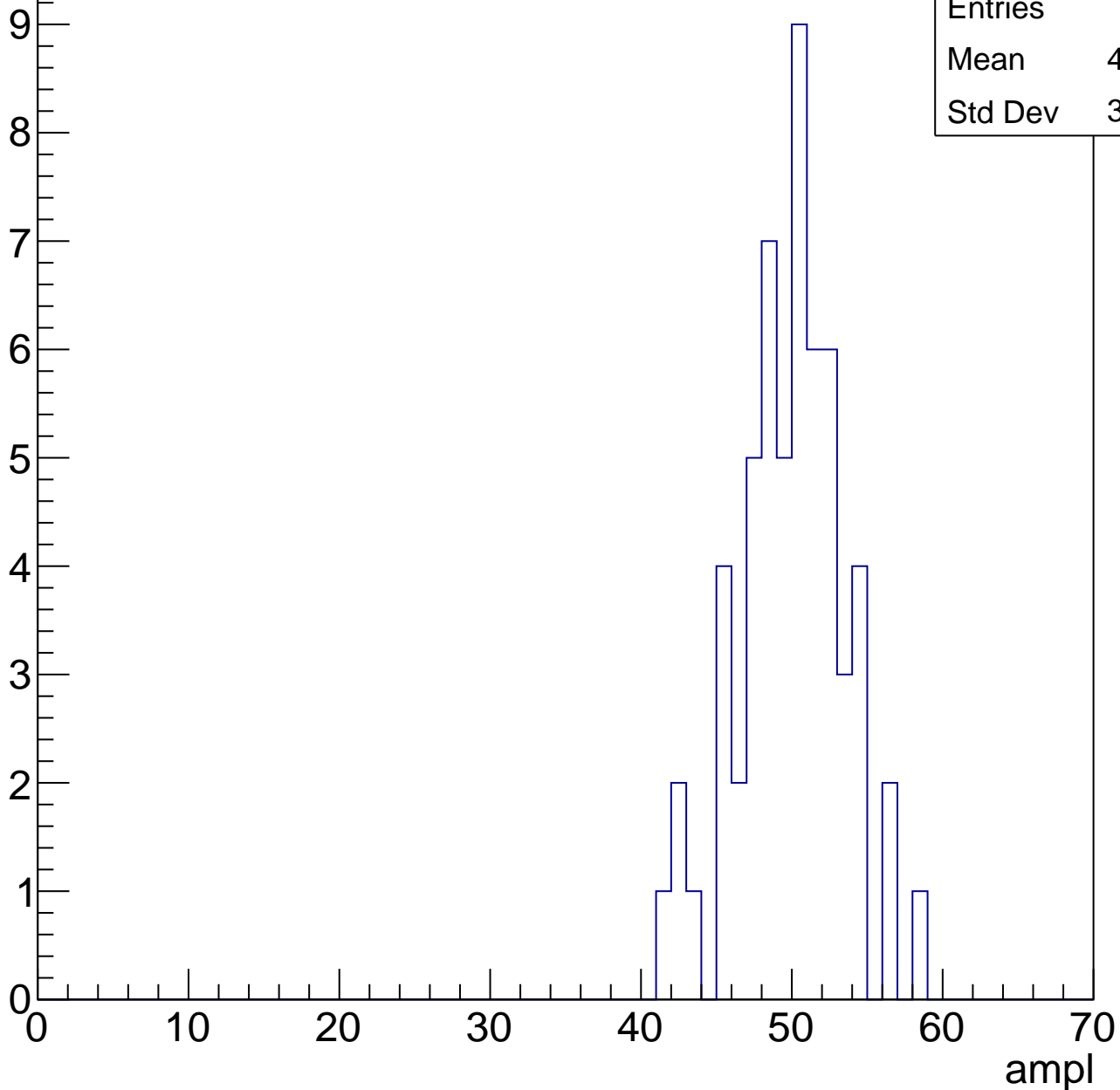


# B1L101S, U9-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	49.47
Std Dev	3.495

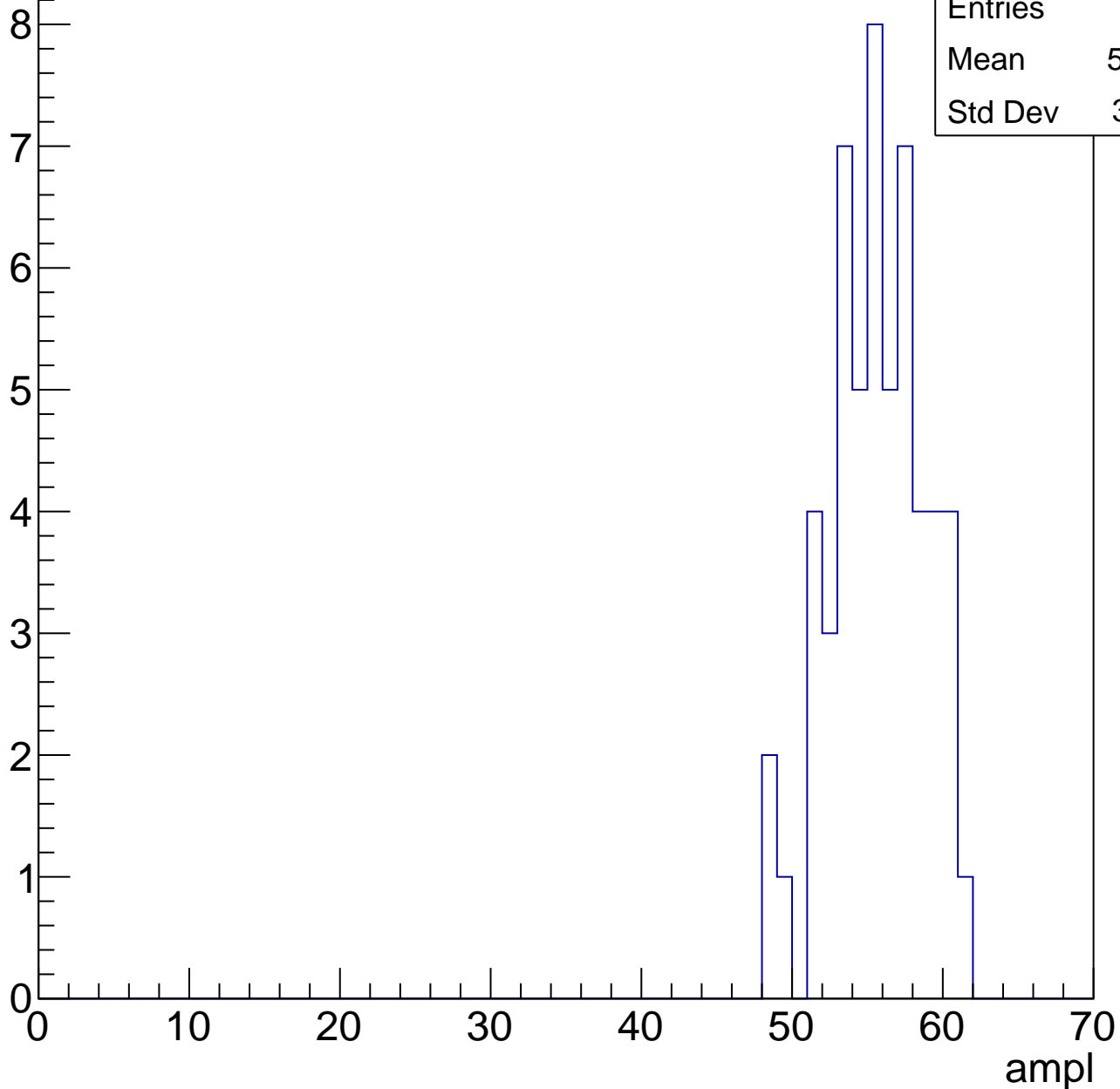


# B1L101S, U9-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	55.16
Std Dev	3.091



# B1L101S, U9-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	53
Mean	58.96
Std Dev	8.534

Entry

10

8

6

4

2

0

0

10

20

30

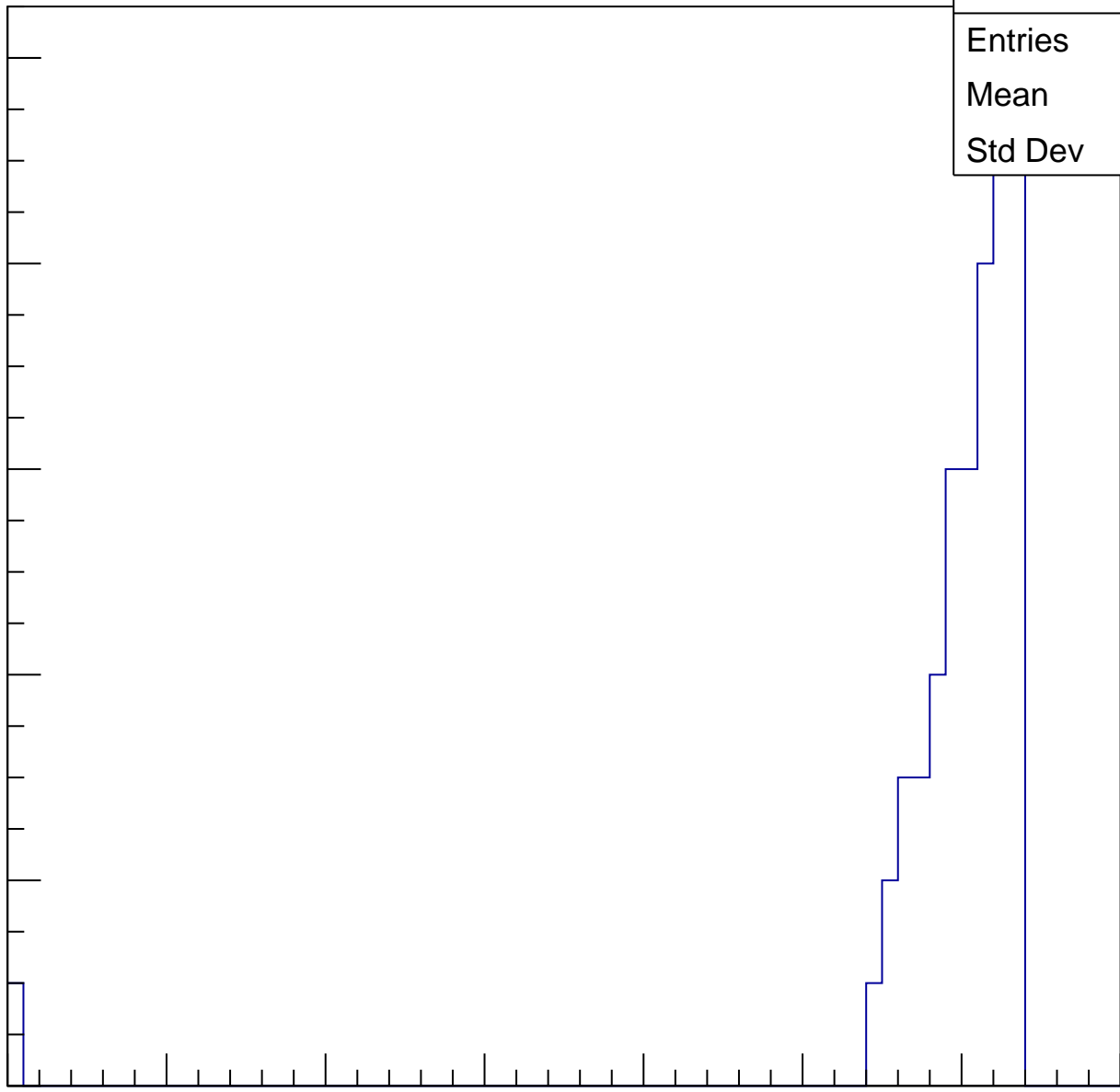
40

50

60

70

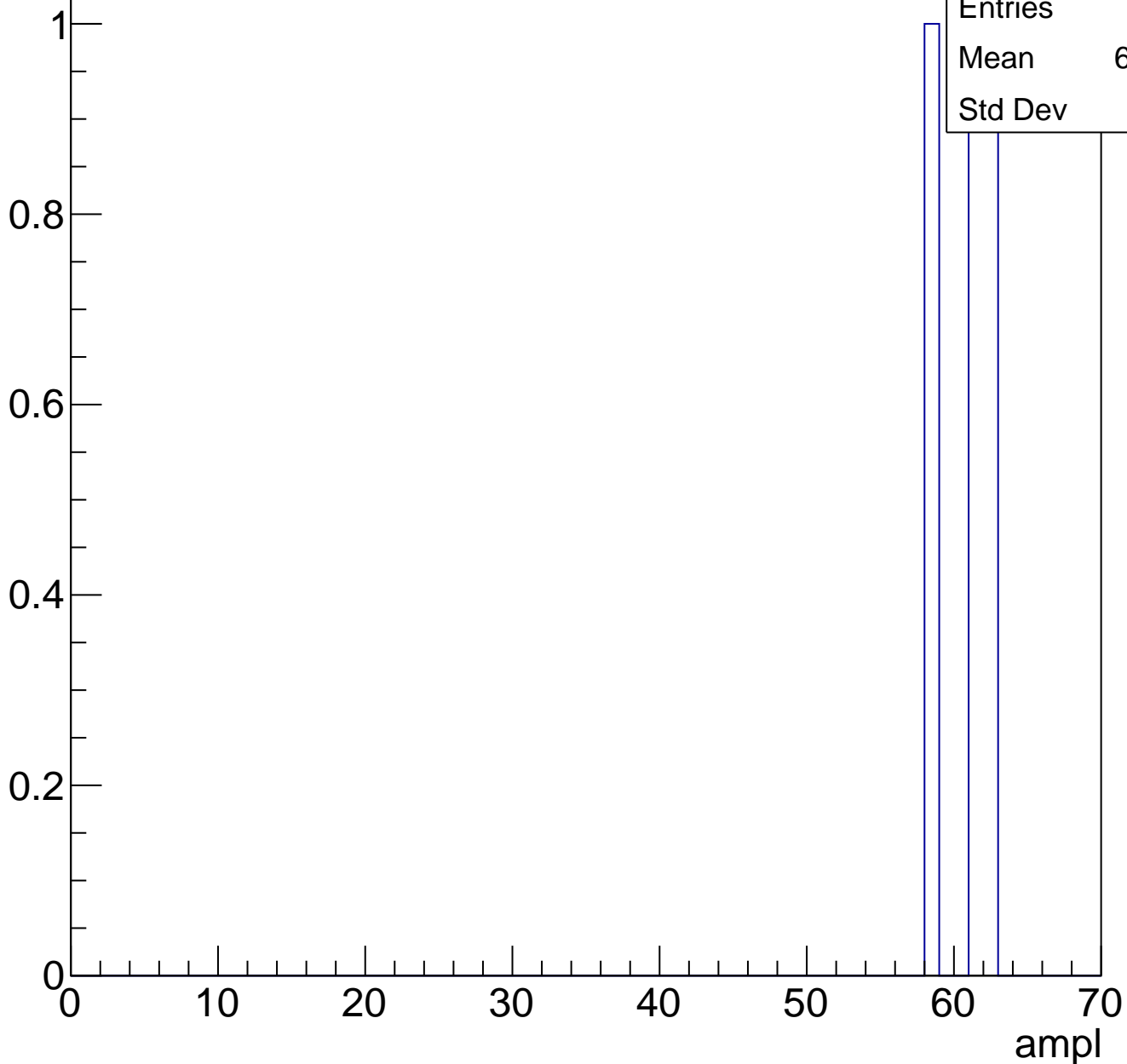
ampl



# B1L101S, U9-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U9-ch10, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	109
Mean	29
Std Dev	5.521

**Gaus mean : 29.9058**

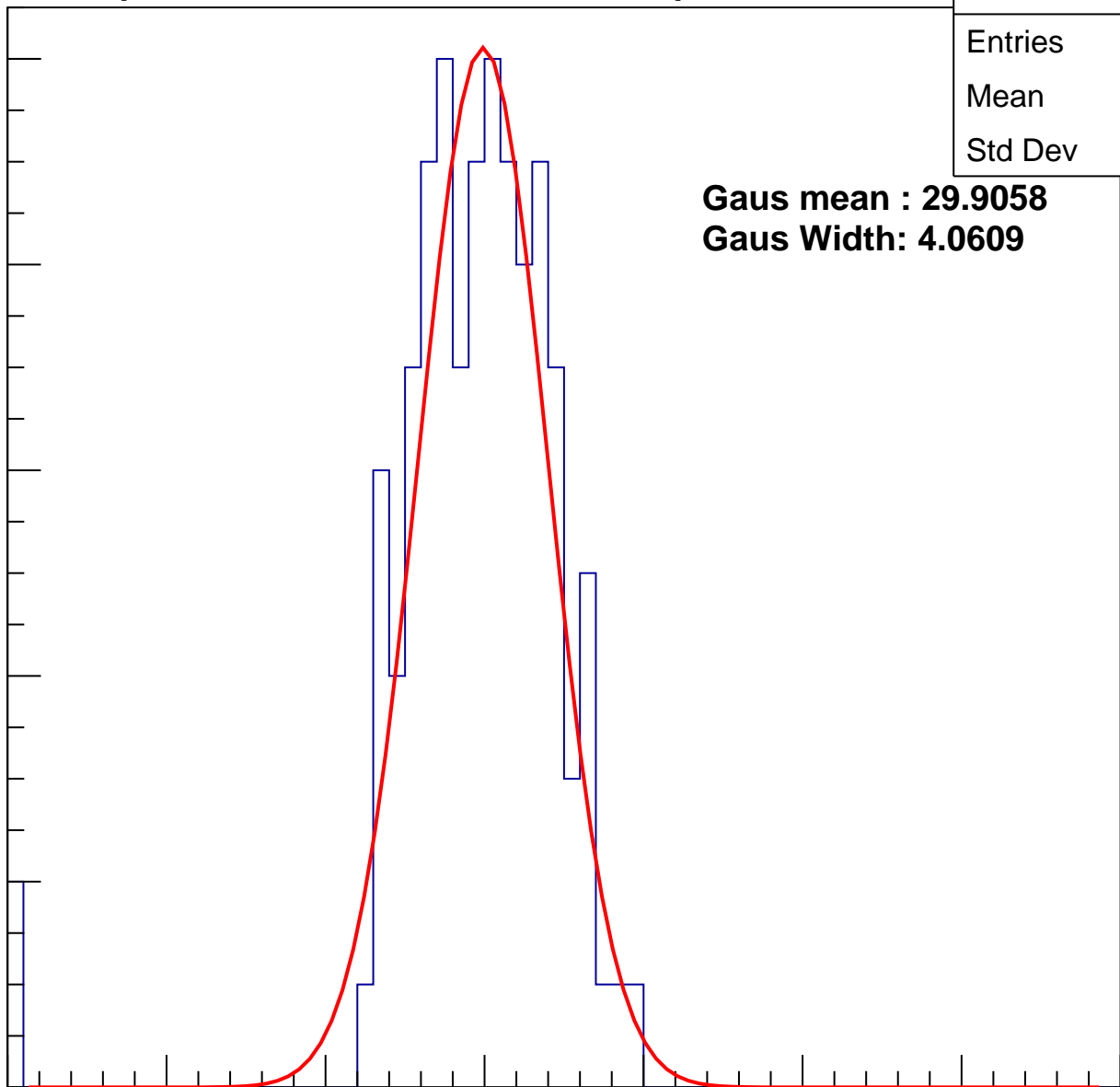
**Gaus Width: 4.0609**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U9-ch10, adc1

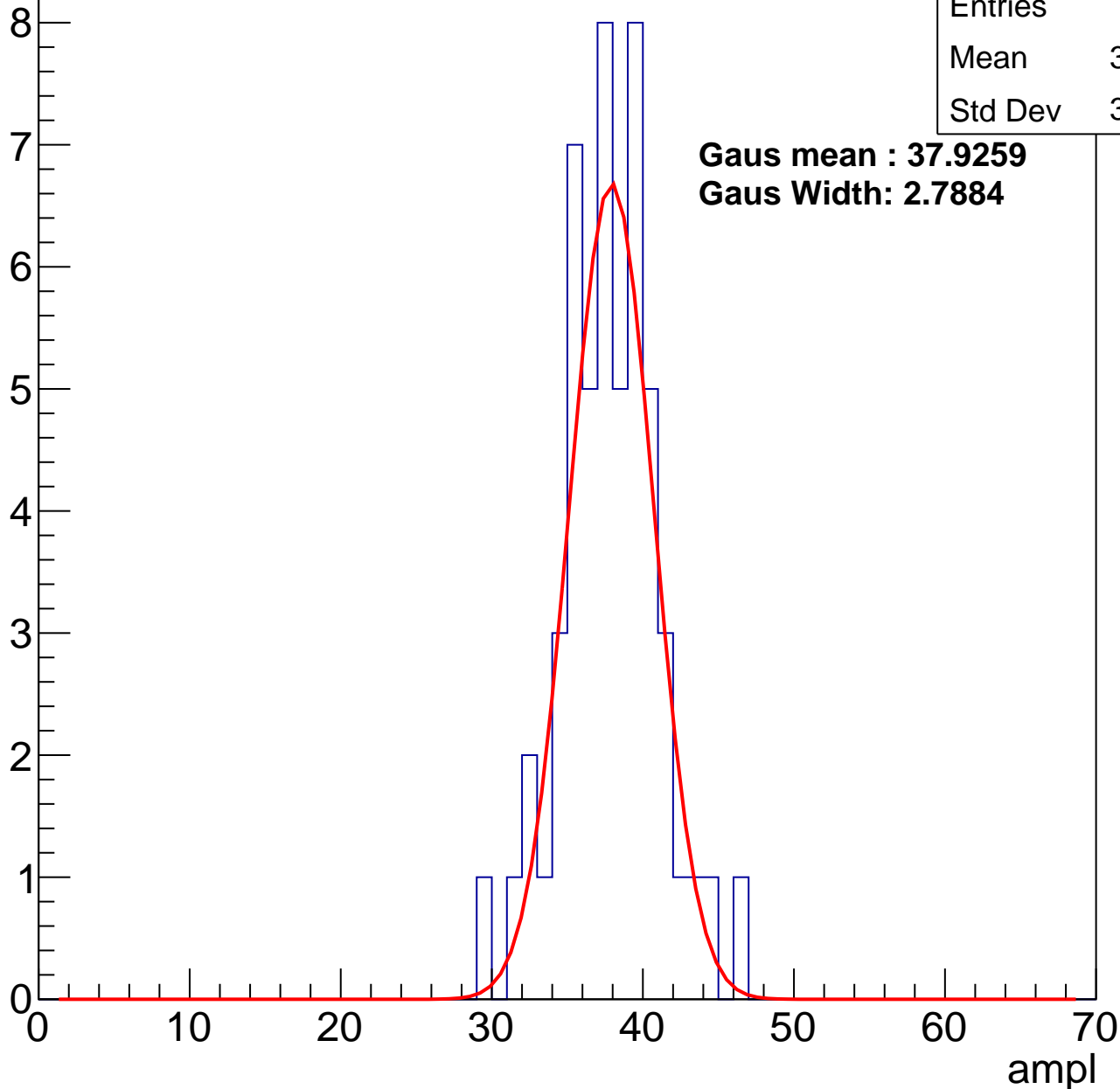
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	37.36
Std Dev	3.193

**Gaus mean : 37.9259**

**Gaus Width: 2.7884**



# B1L101S, U9-ch10, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

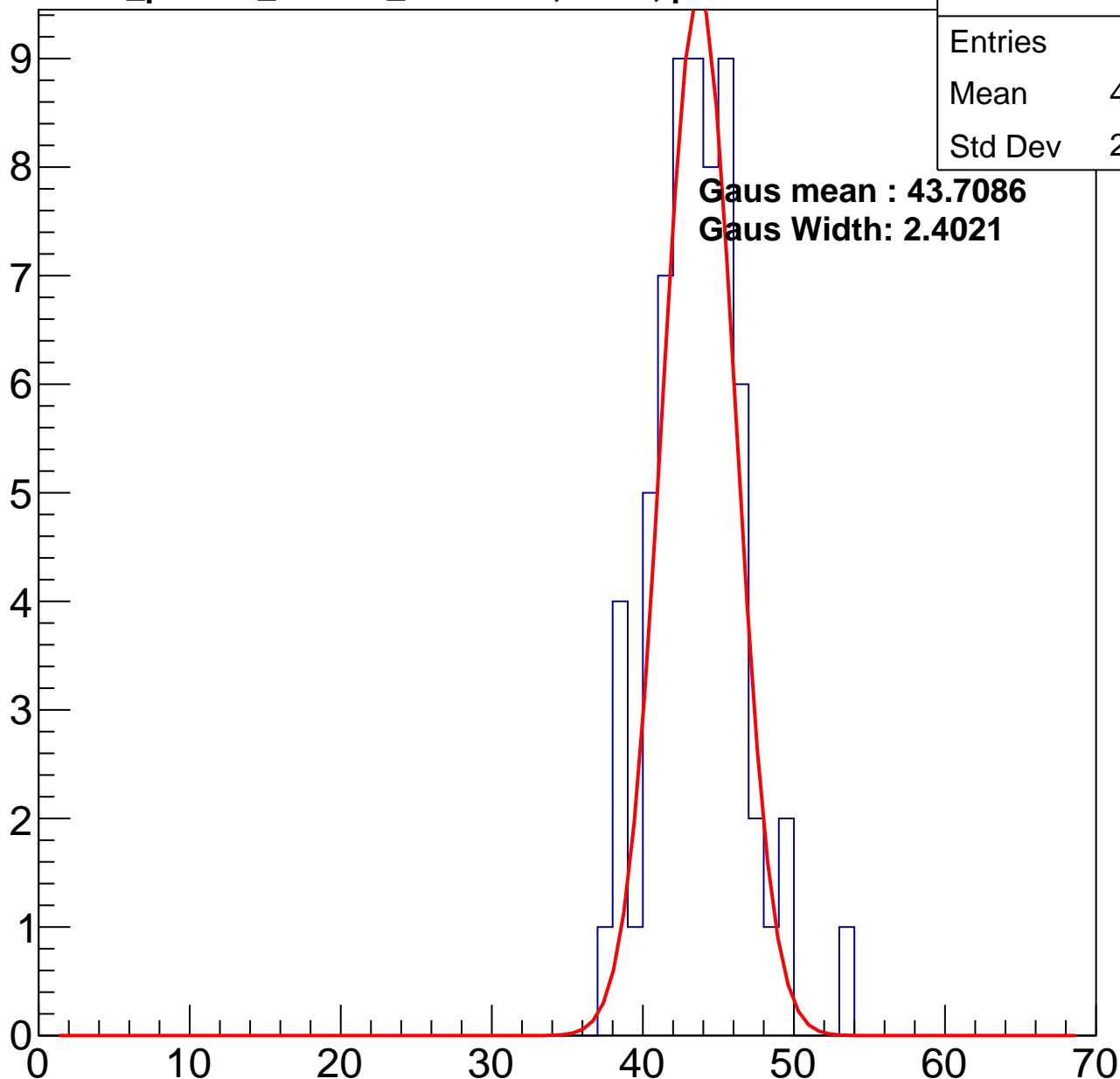
9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	65
Mean	43.17
Std Dev	2.933

**Gaus mean : 43.7086**

**Gaus Width: 2.4021**

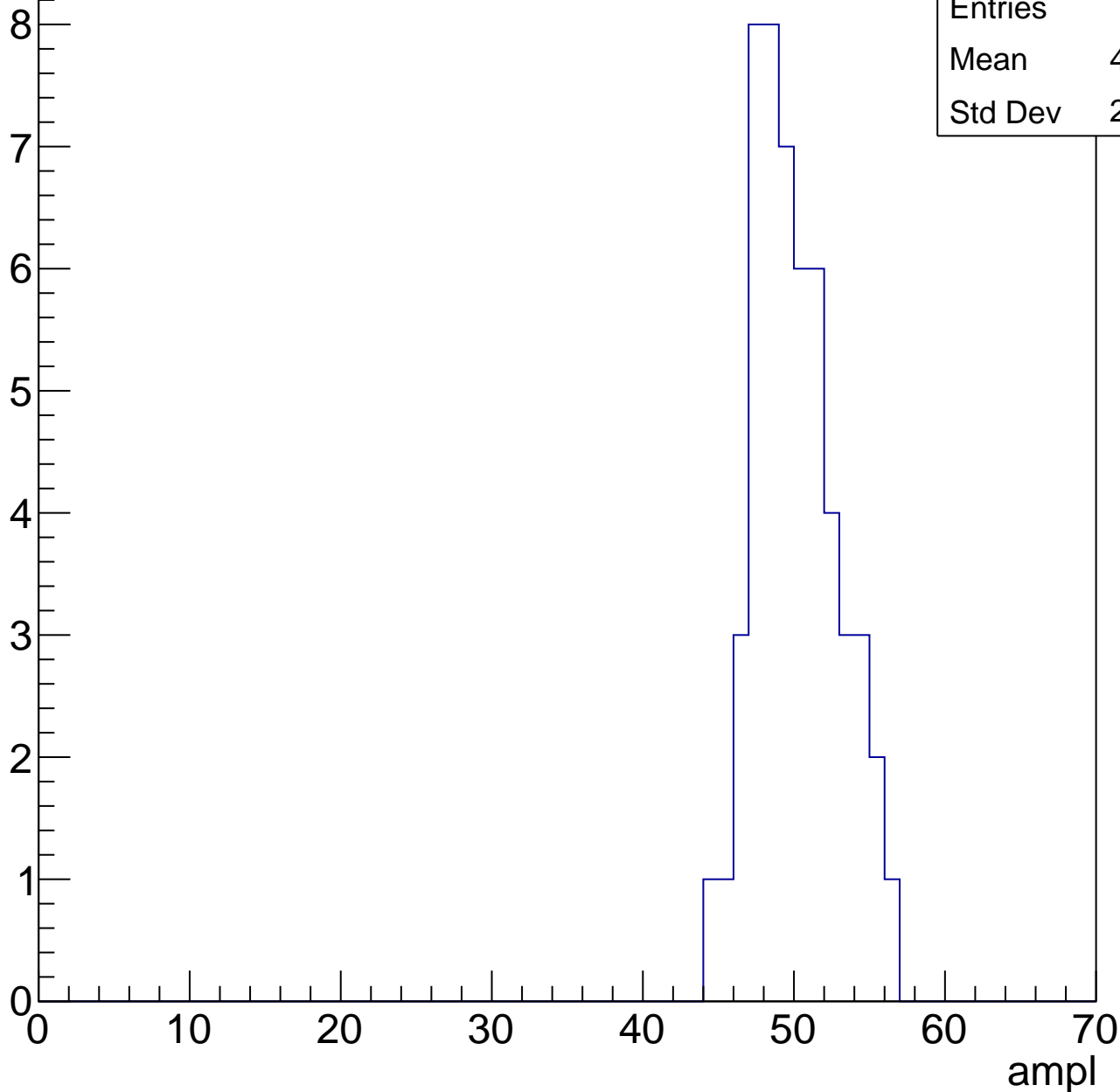
ampl



# B1L101S, U9-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



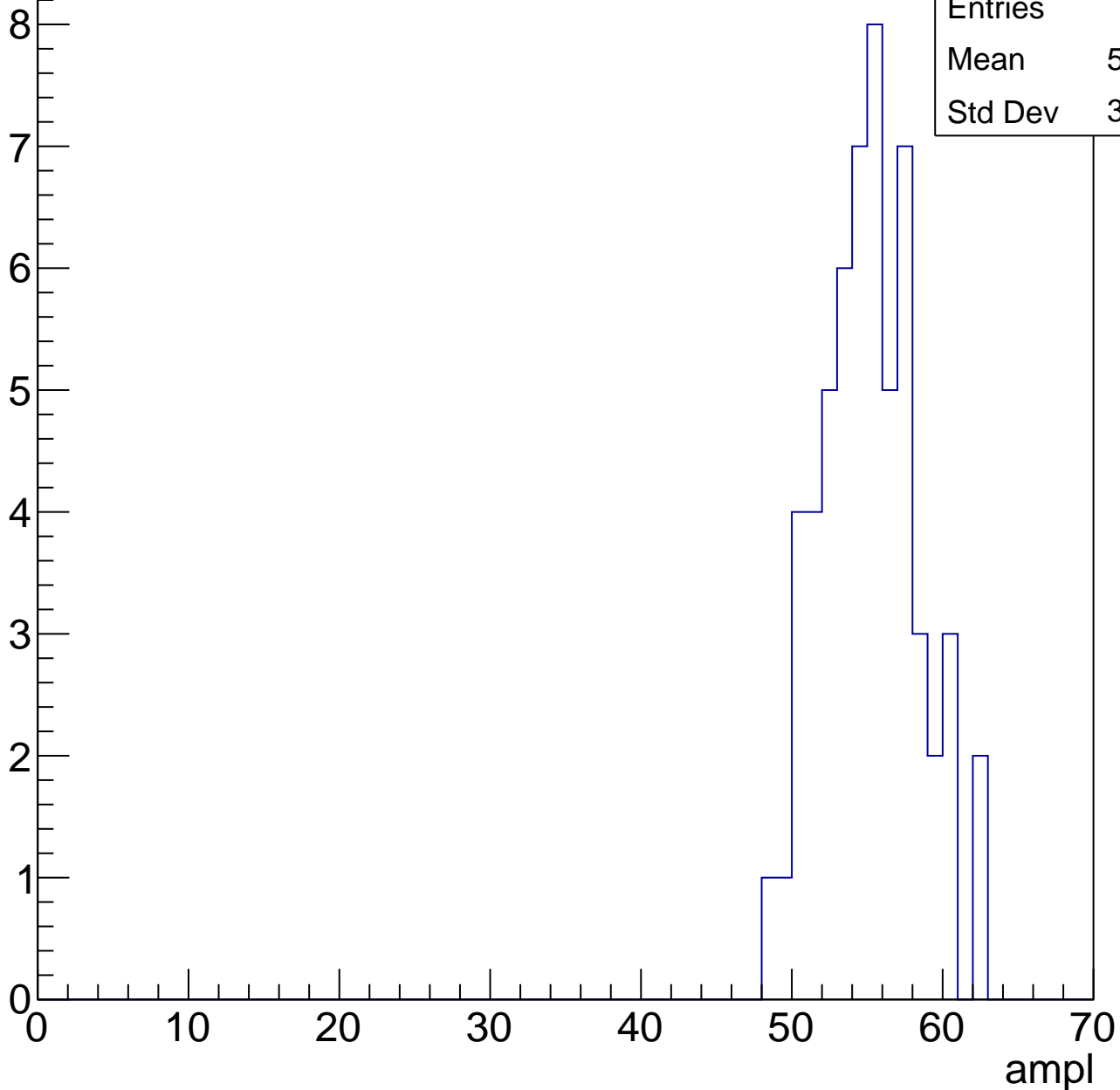
Entries	53
Mean	49.64
Std Dev	2.734

# B1L101S, U9-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	54.69
Std Dev	3.174

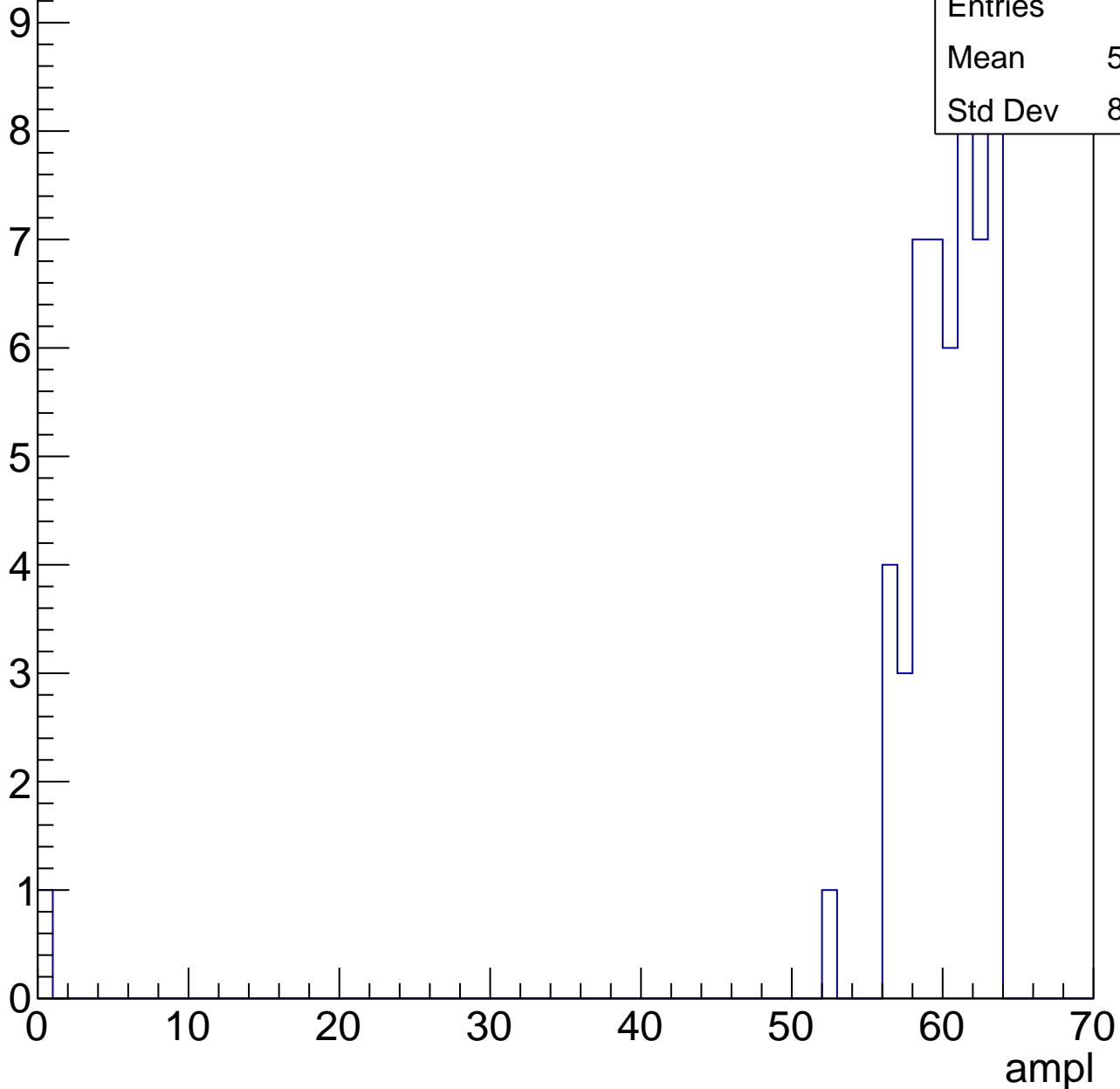


# B1L101S, U9-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	58.74
Std Dev	8.483



# B1L101S, U9-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

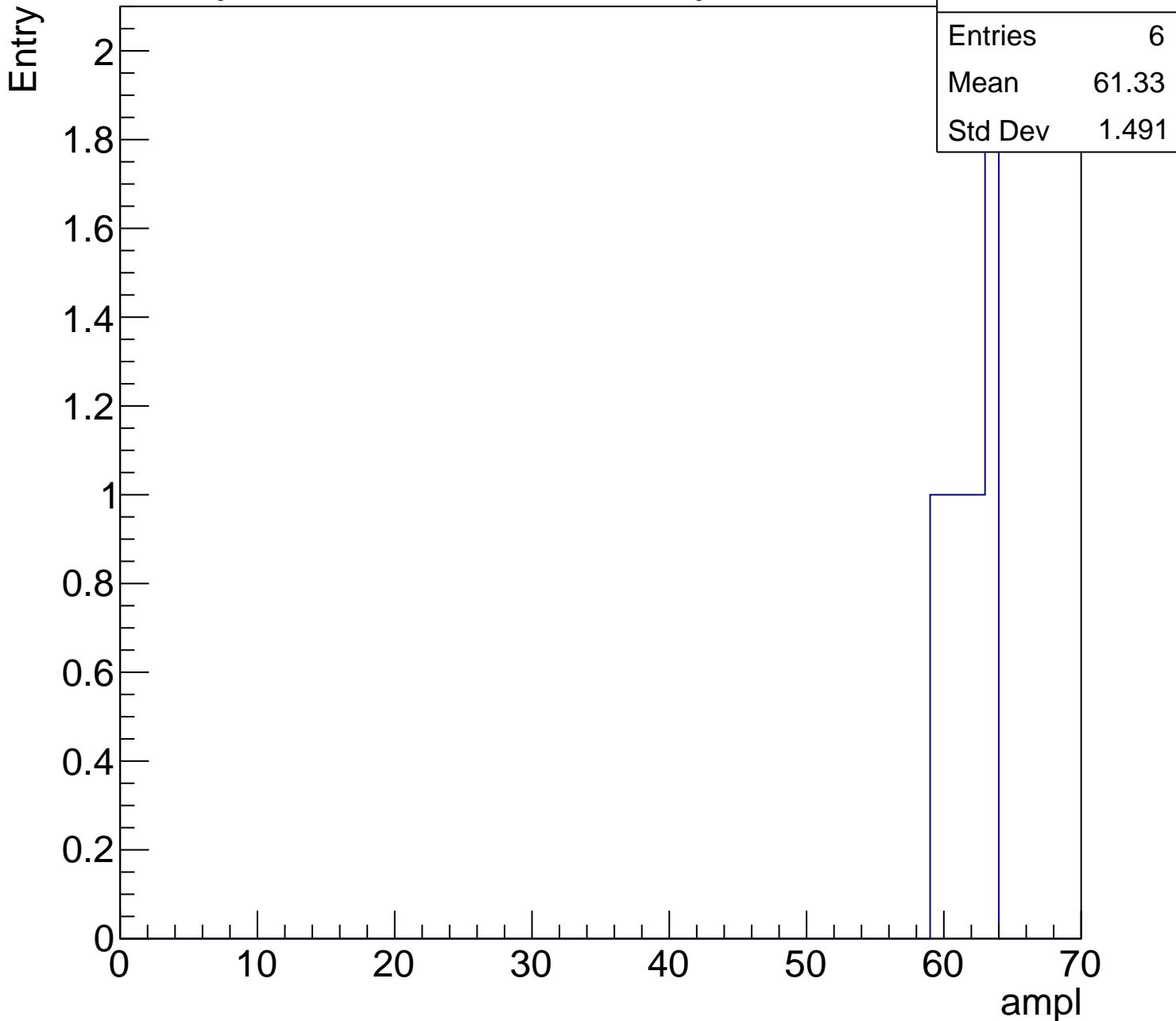
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.33
Std Dev	1.491

0 10 20 30 40 50 60 70

ampl





# B1L101S, U9-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	10.5
Std Dev	10.5

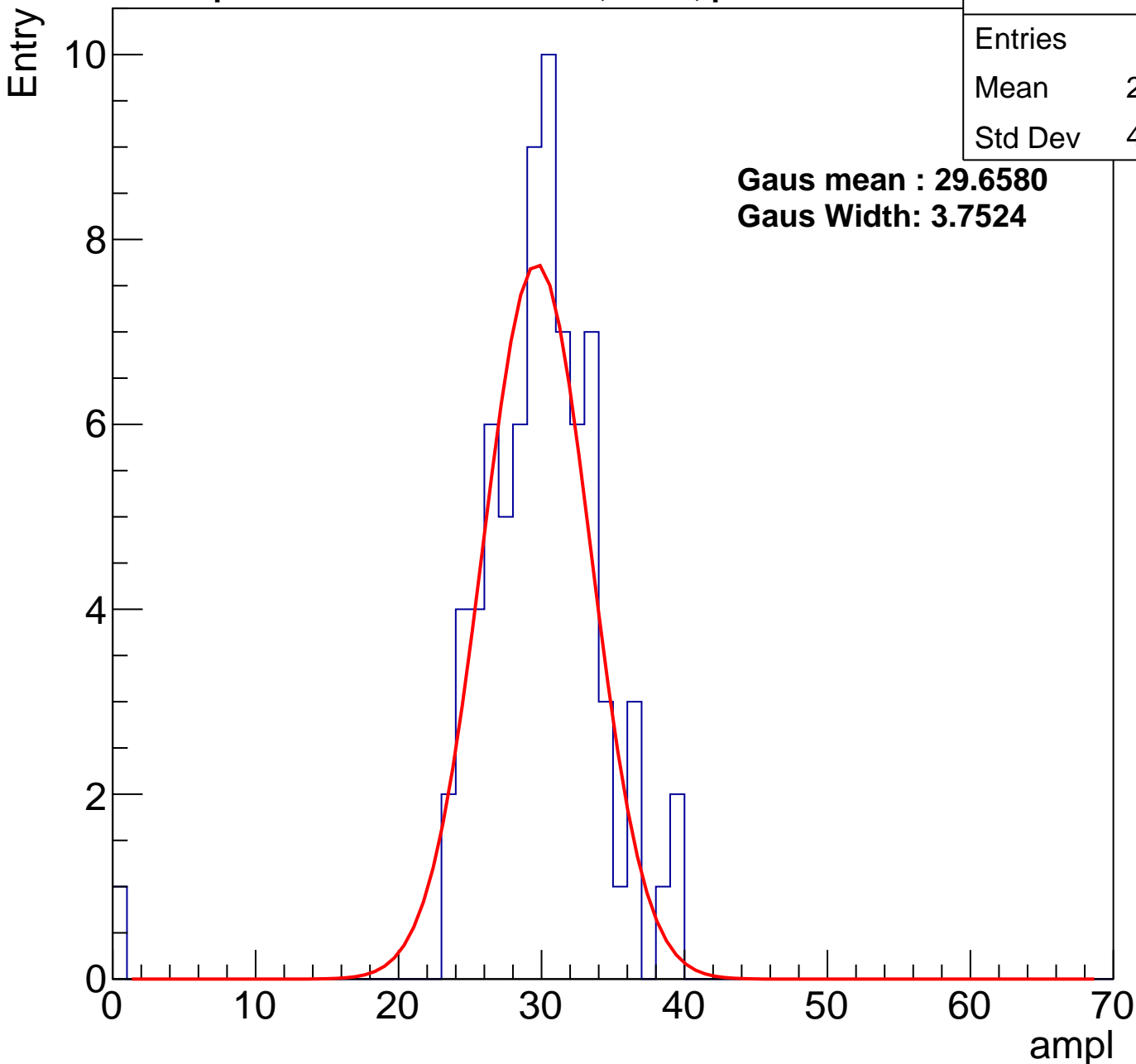
# B1L101S, U9-ch11, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	77
Mean	29.39
Std Dev	4.952

**Gaus mean : 29.6580**

**Gaus Width: 3.7524**



# B1L101S, U9-ch11, adc1

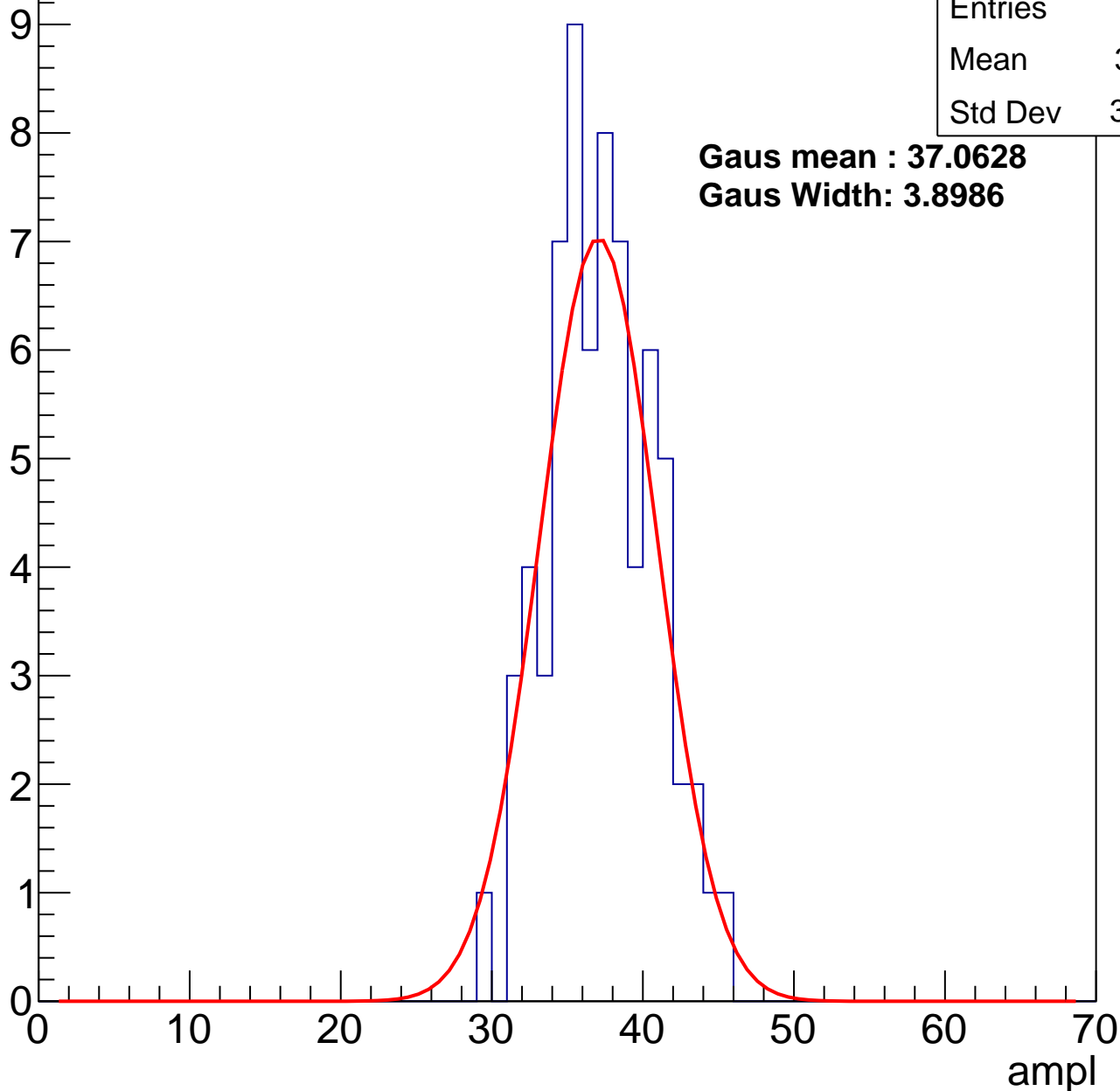
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	36.81
Std Dev	3.436

**Gaus mean : 37.0628**

**Gaus Width: 3.8986**

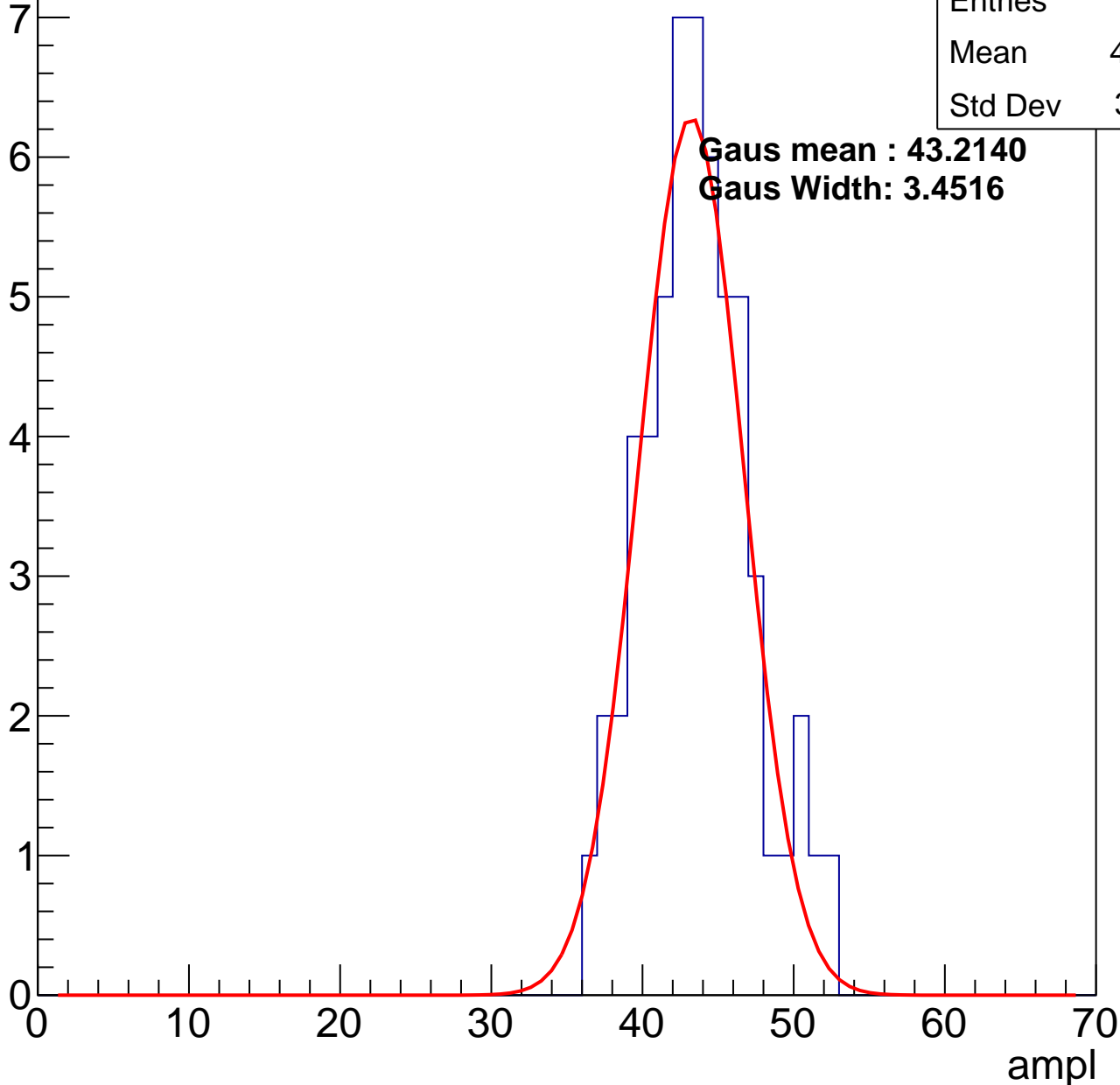


# B1L101S, U9-ch11, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	43.19
Std Dev	3.551

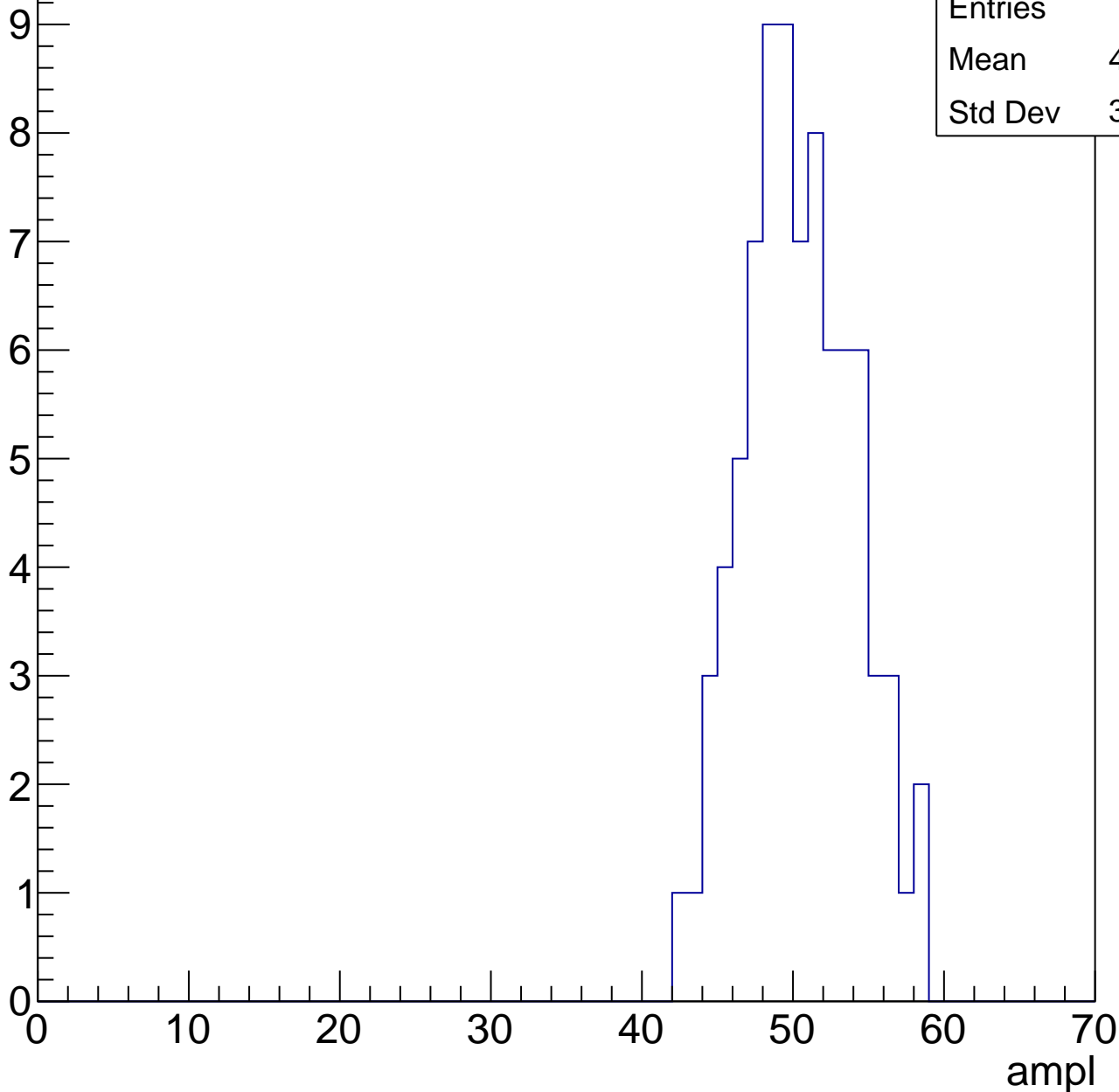


# B1L101S, U9-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	49.96
Std Dev	3.602



# B1L101S, U9-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

6

5

4

3

2

1

0

Entries	49
Mean	56.39
Std Dev	2.905

ampl

10

20

30

40

50

60

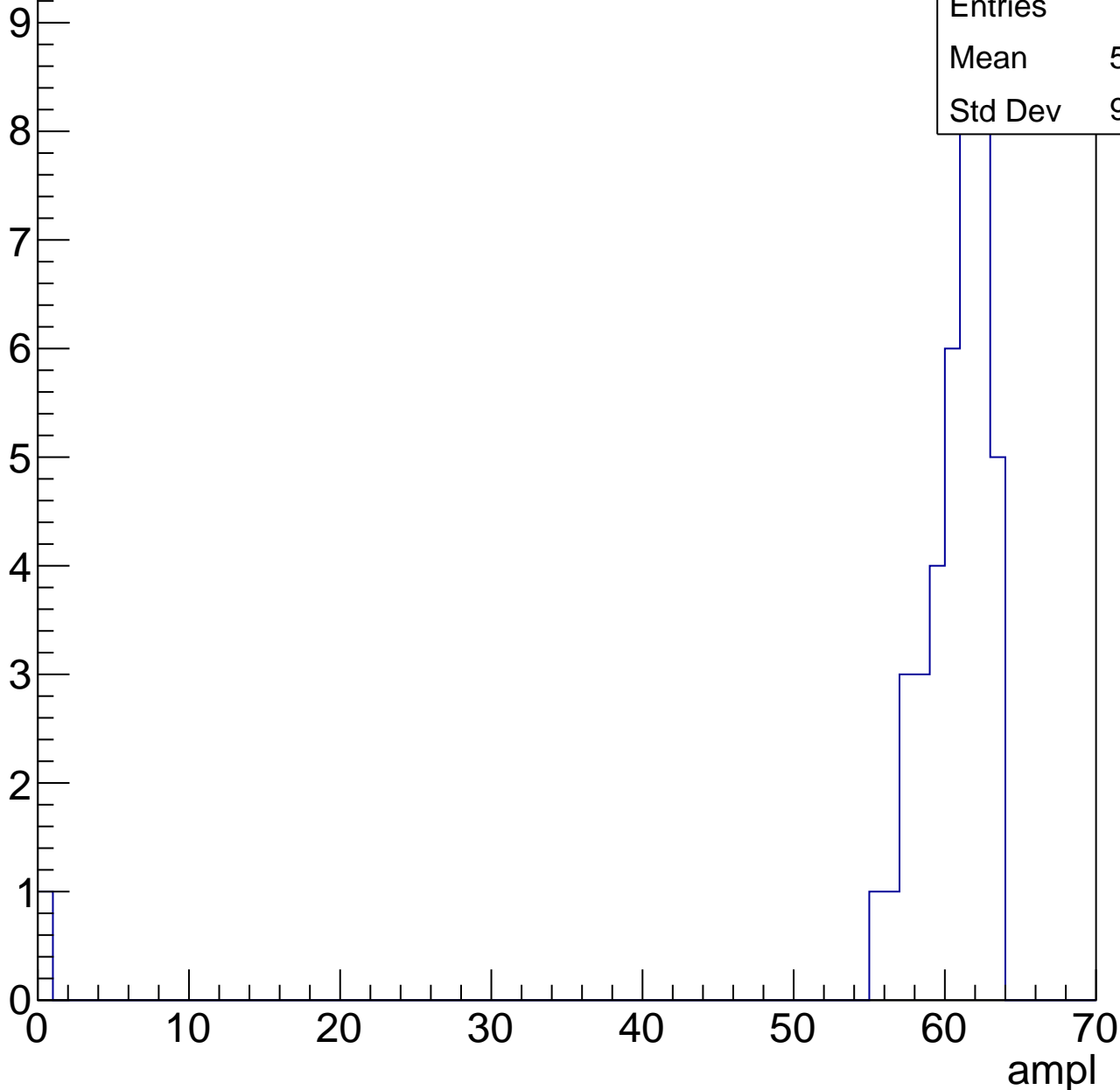
70

# B1L101S, U9-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

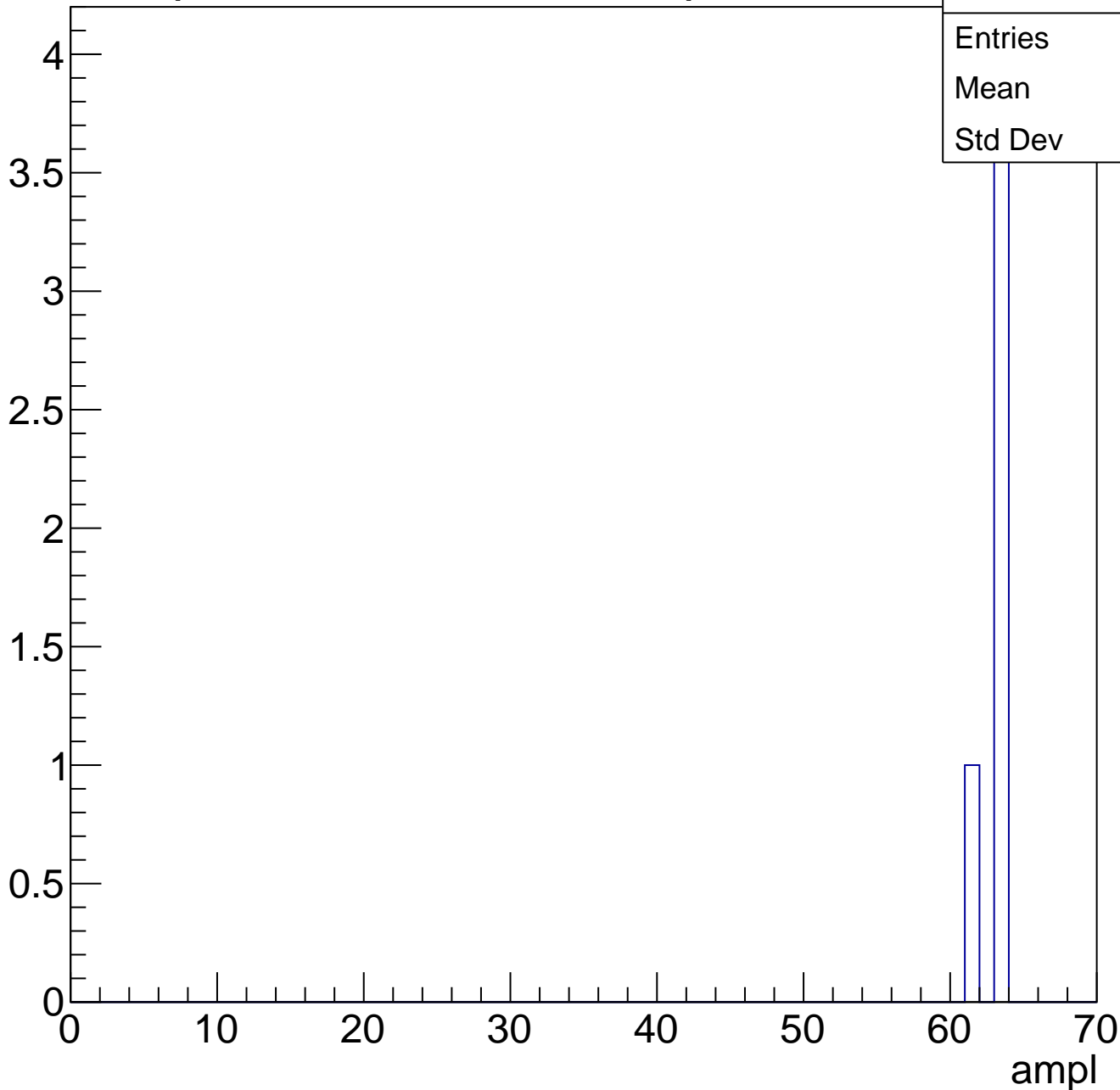
Entries	41
Mean	58.85
Std Dev	9.524



# B1L101S, U9-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch12, adc0

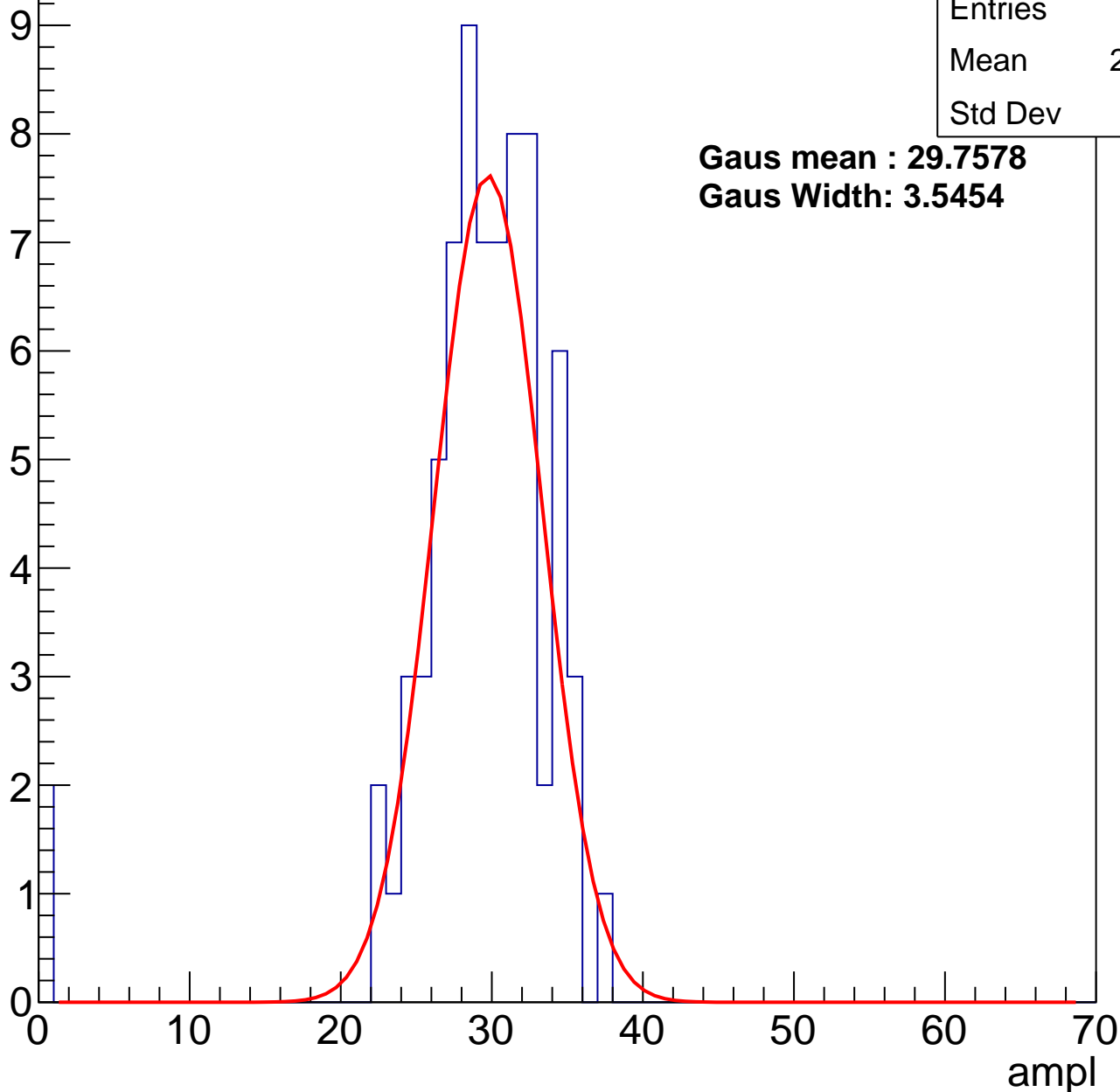
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	28.57
Std Dev	5.78

**Gaus mean : 29.7578**

**Gaus Width: 3.5454**



# B1L101S, U9-ch12, adc1

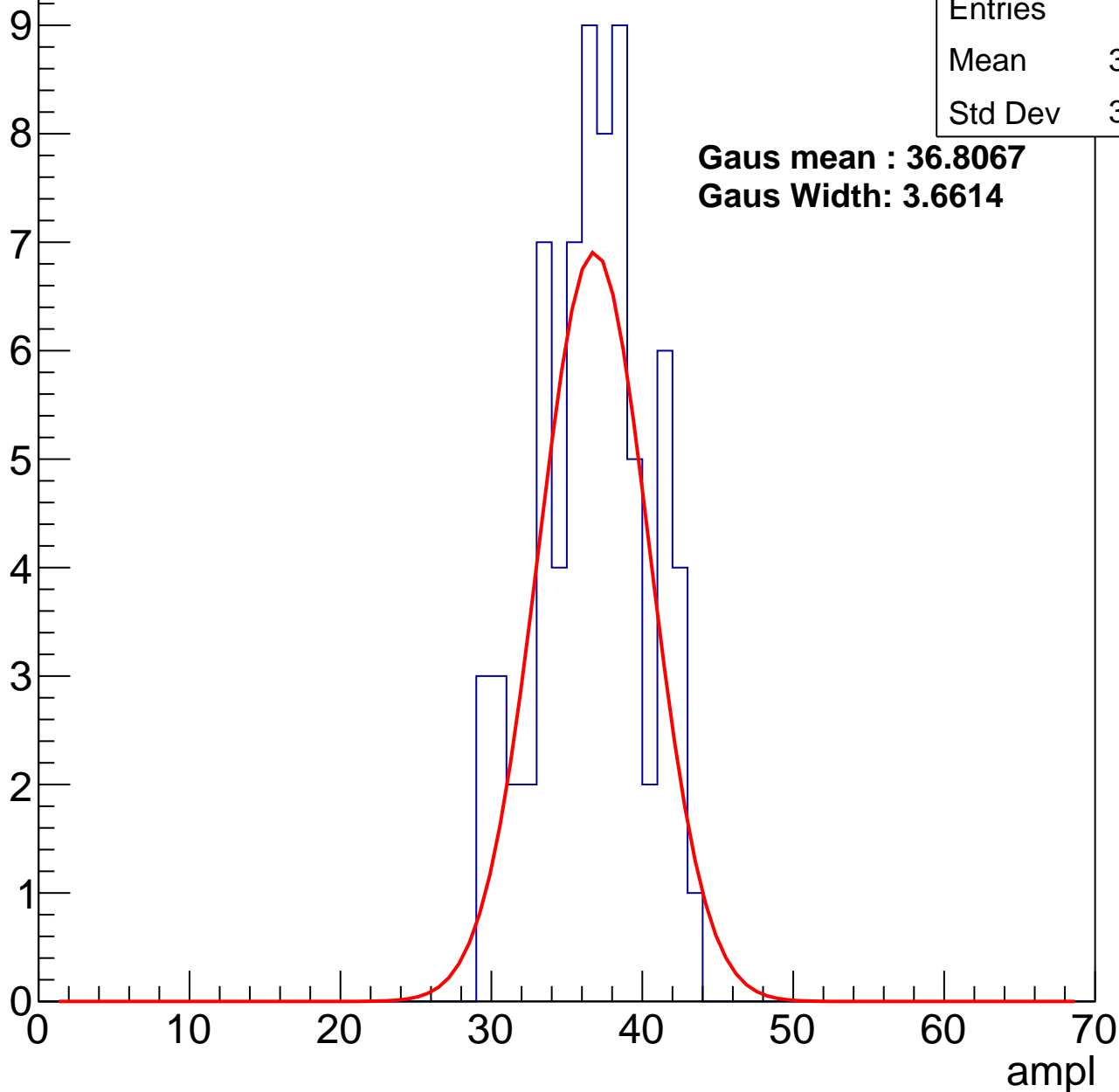
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	36.24
Std Dev	3.502

**Gaus mean : 36.8067**

**Gaus Width: 3.6614**



# B1L101S, U9-ch12, adc2

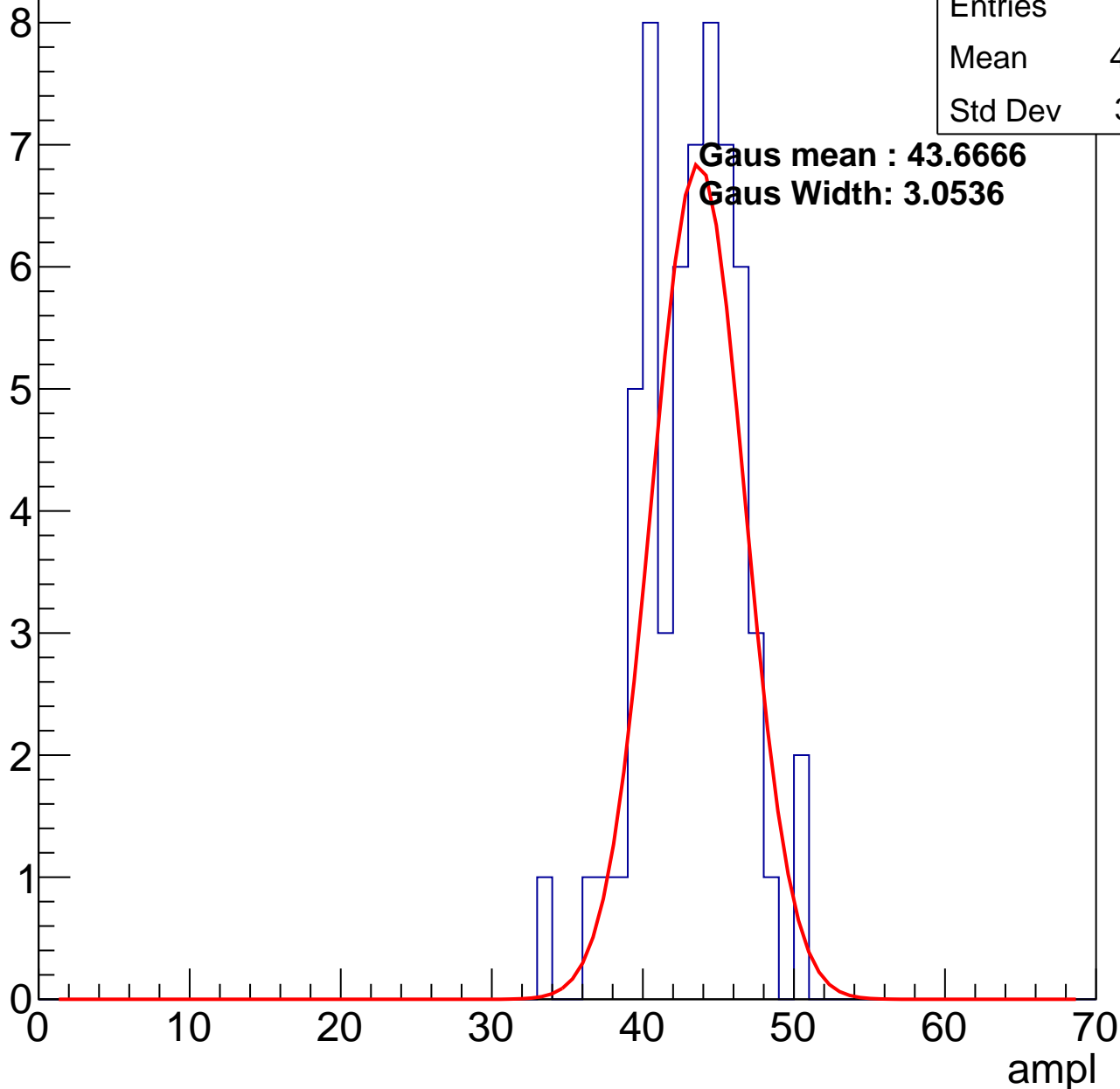
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	42.78
Std Dev	3.261

**Gaus mean : 43.6666**

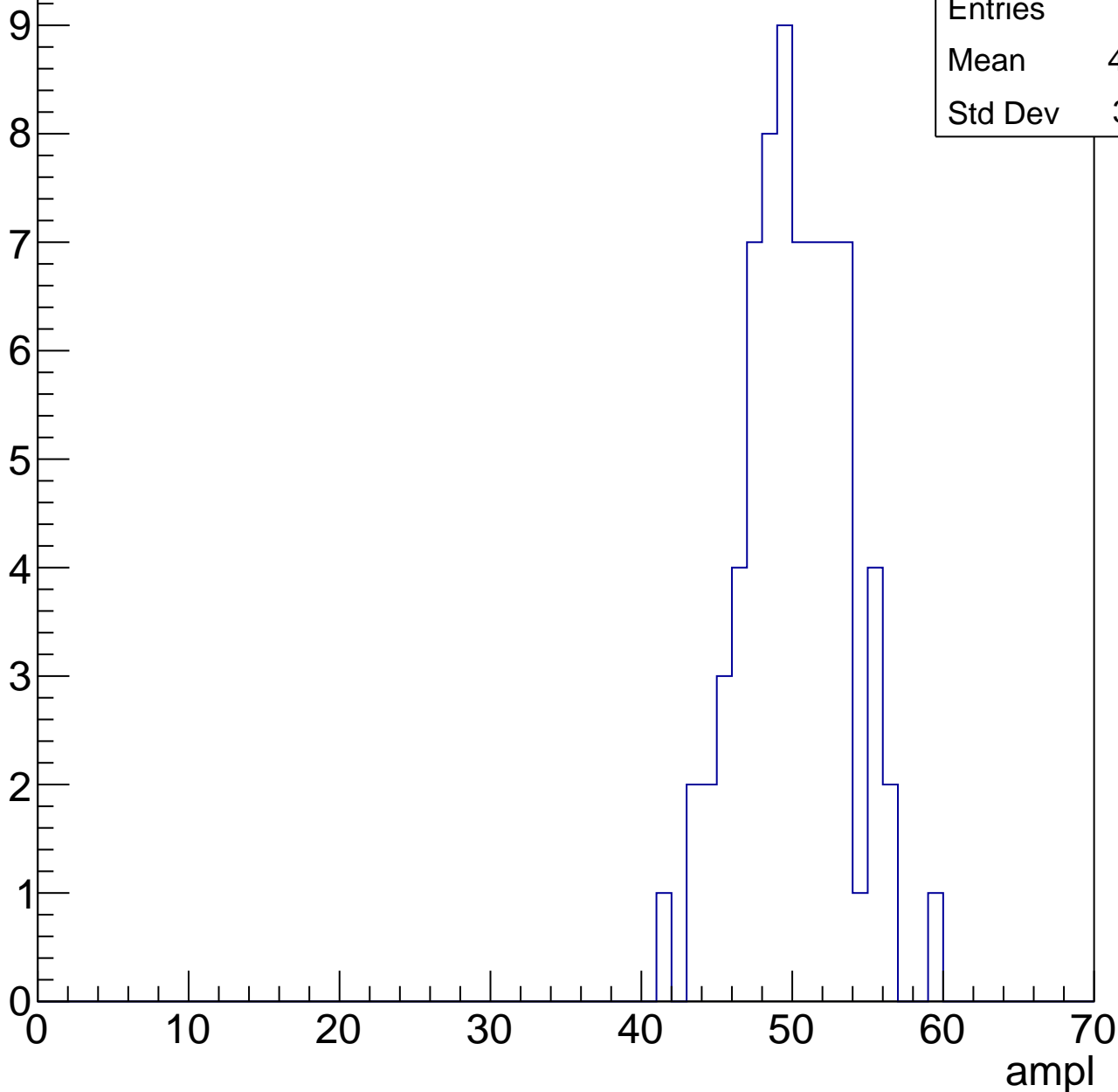
**Gaus Width: 3.0536**



# B1L101S, U9-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

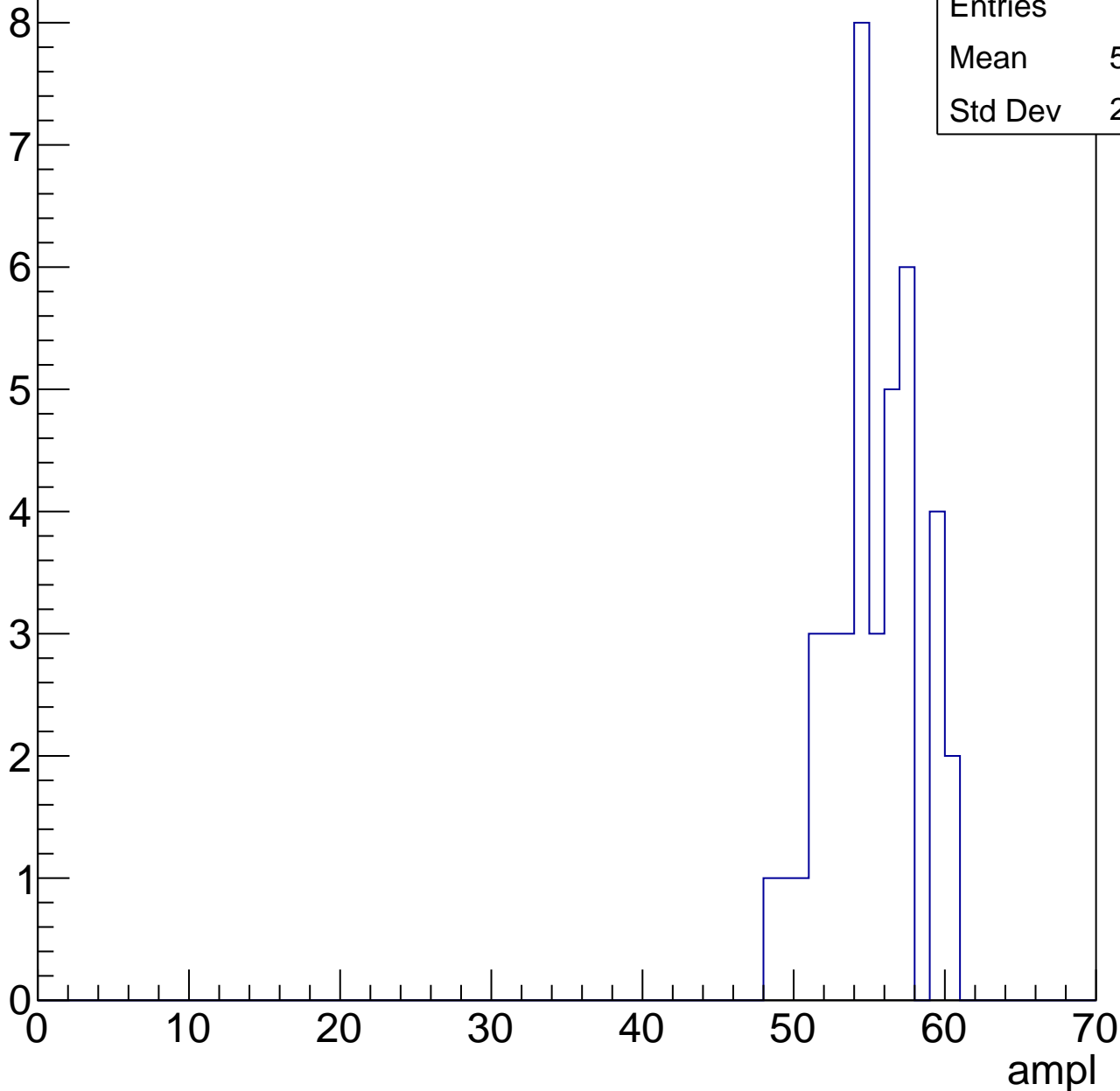


# B1L101S, U9-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	40
Mean	54.75
Std Dev	2.939



# B1L101S, U9-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

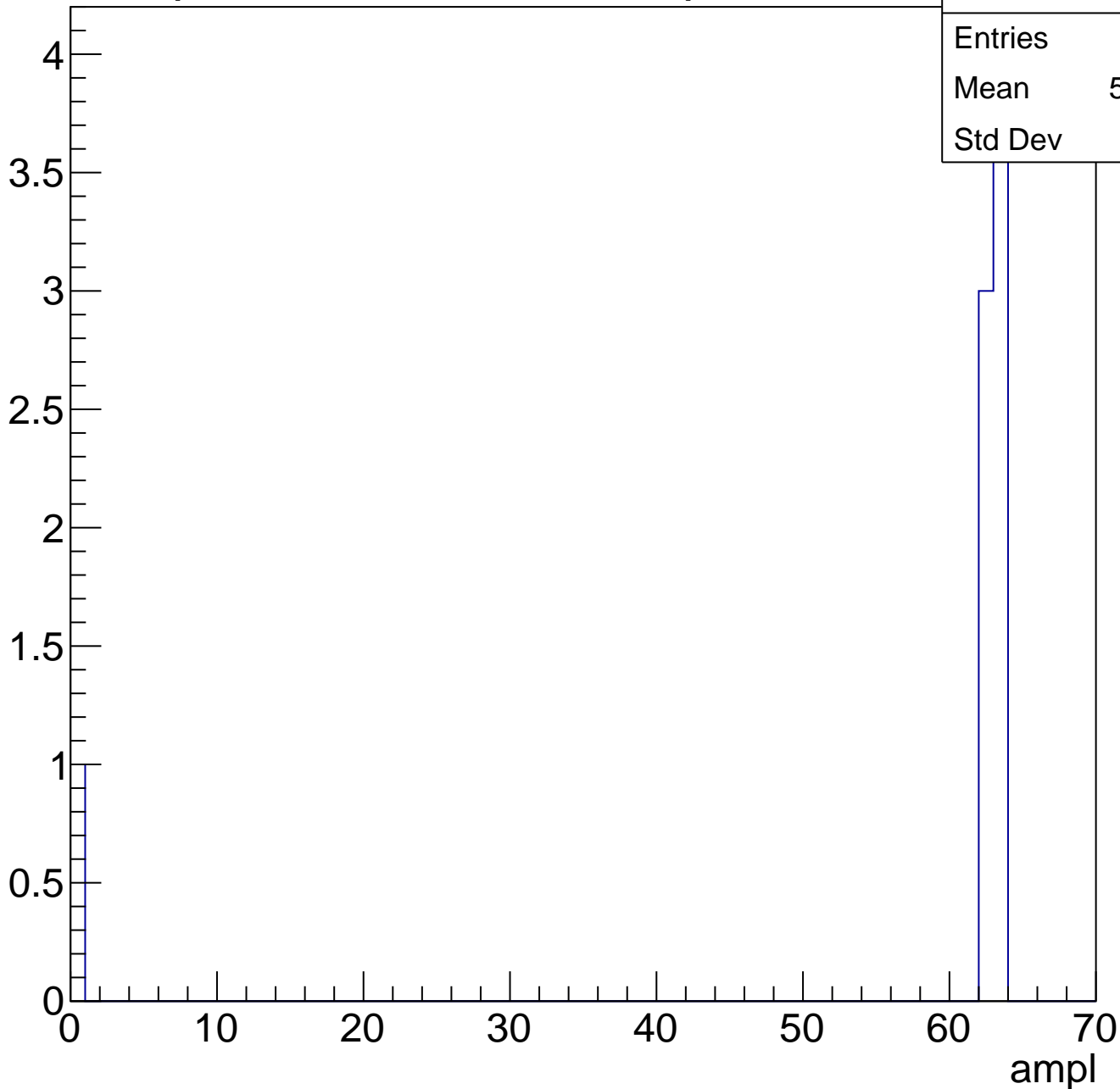
ampl

Entries	57
Mean	59.51
Std Dev	2.363

# B1L101S, U9-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U9-ch13, adc0

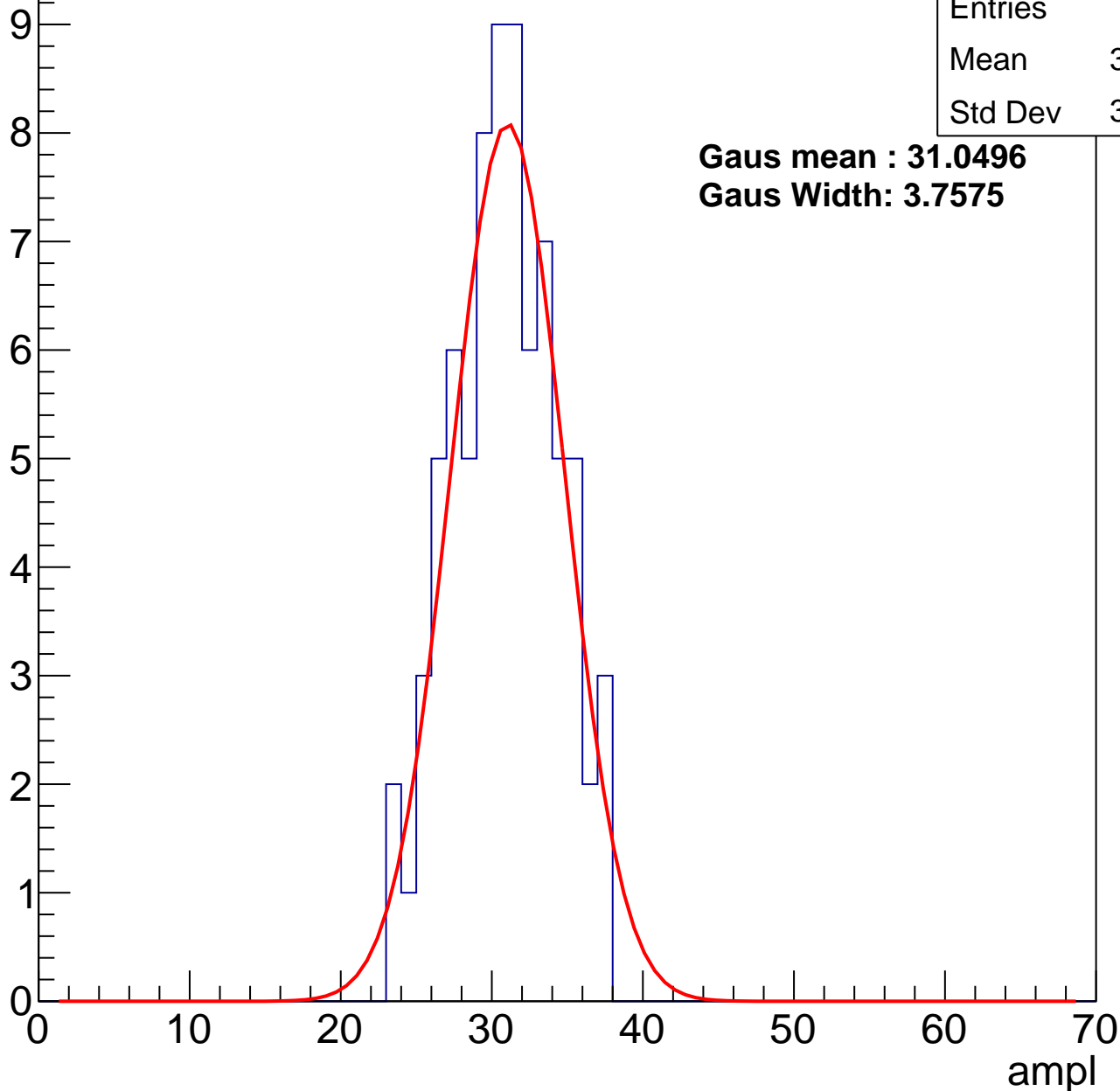
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	30.38
Std Dev	3.403

**Gaus mean : 31.0496**

**Gaus Width: 3.7575**



# B1L101S, U9-ch13, adc1

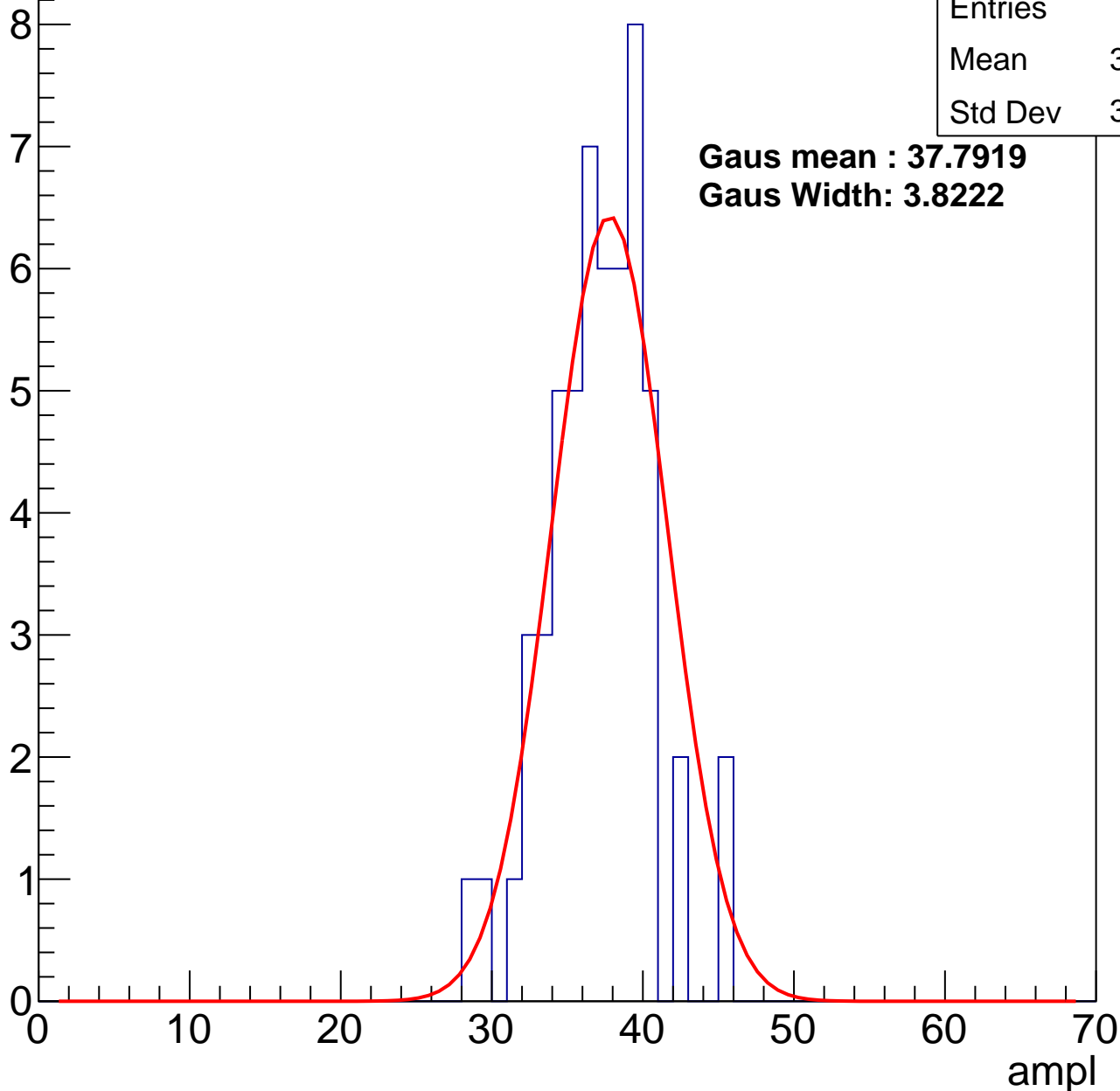
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	36.65
Std Dev	3.386

**Gaus mean : 37.7919**

**Gaus Width: 3.8222**



# B1L101S, U9-ch13, adc2

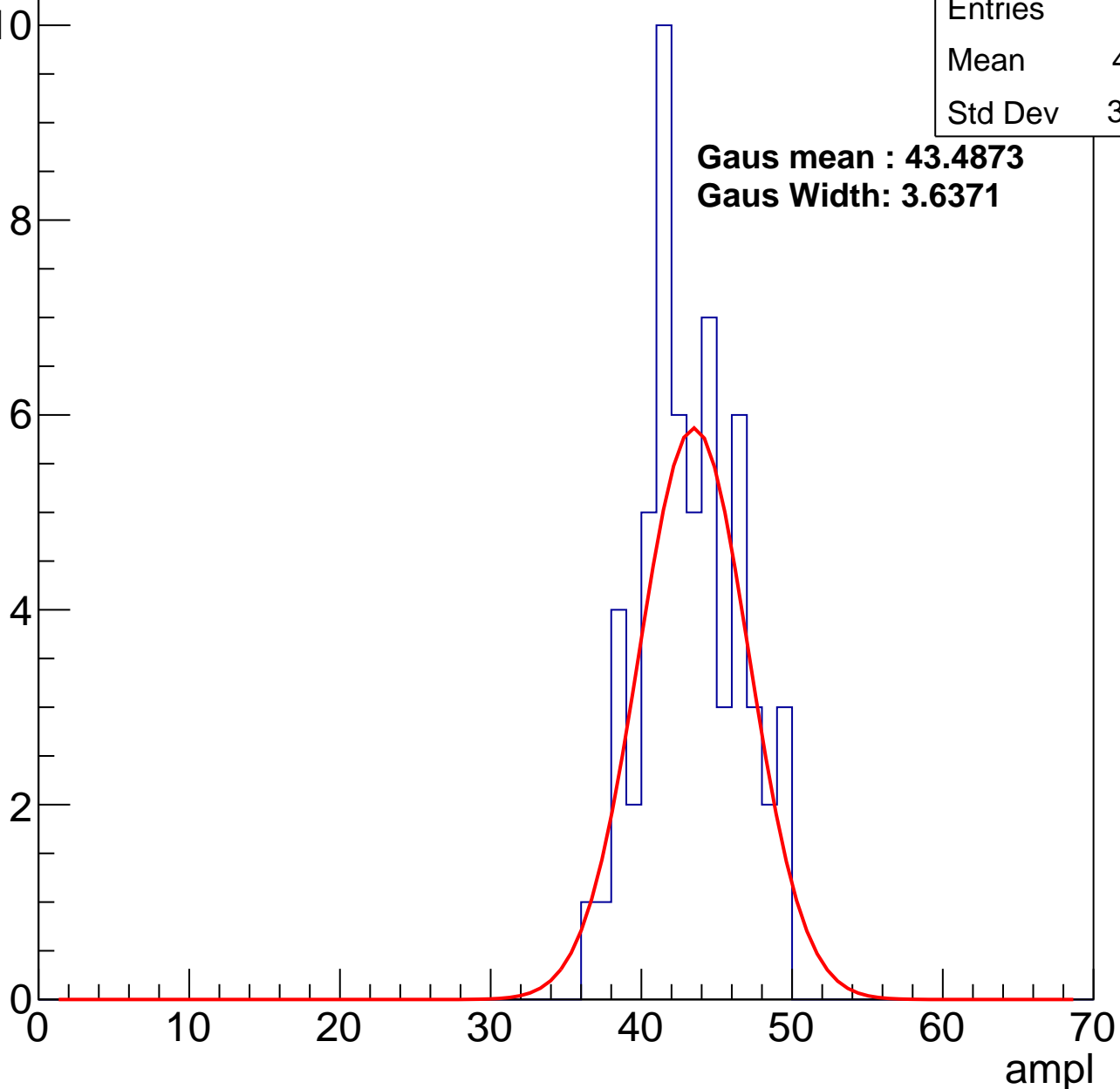
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	42.81
Std Dev	3.176

**Gaus mean : 43.4873**

**Gaus Width: 3.6371**



# B1L101S, U9-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

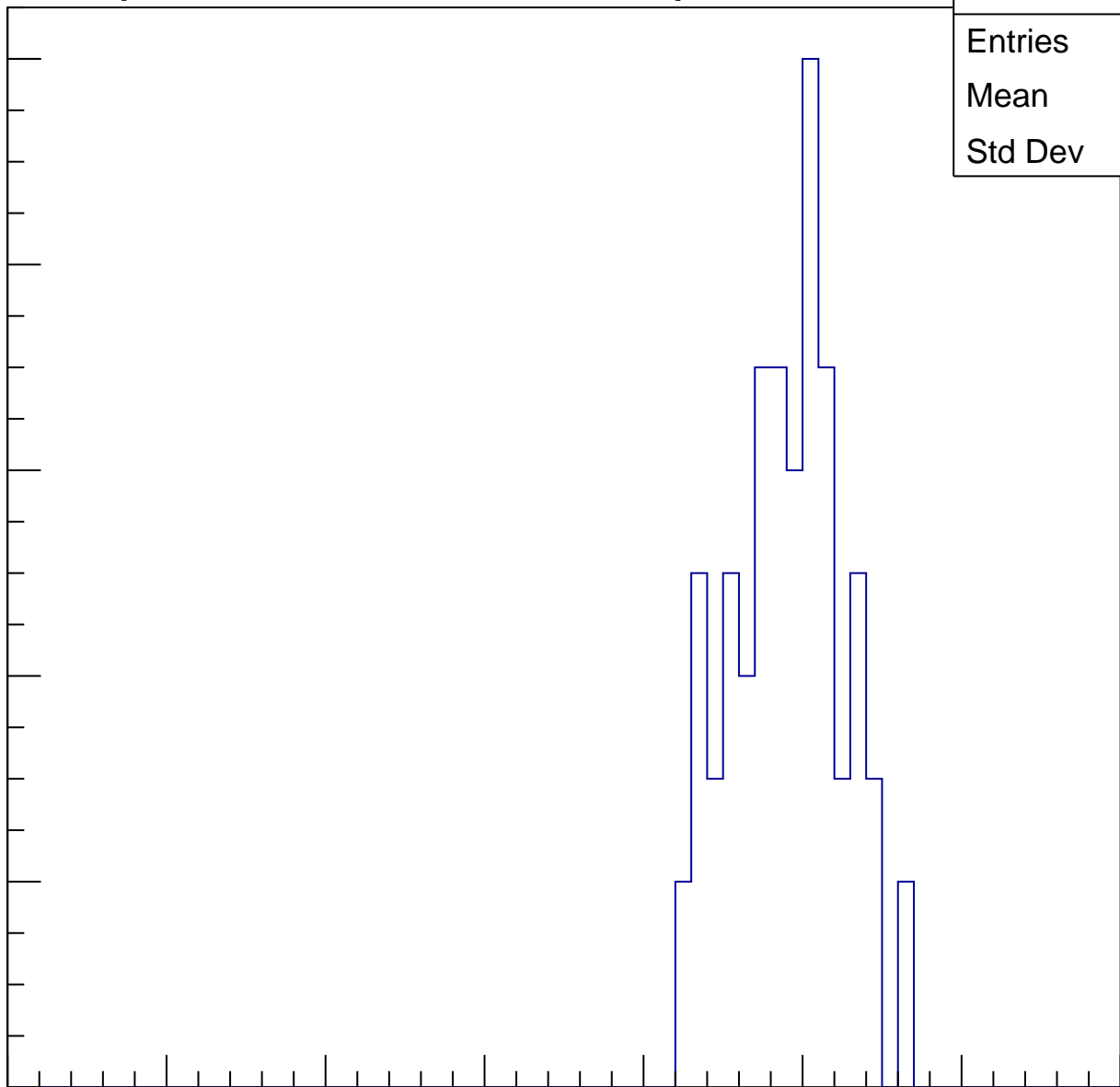
Entries	69
Mean	48.57
Std Dev	3.424

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

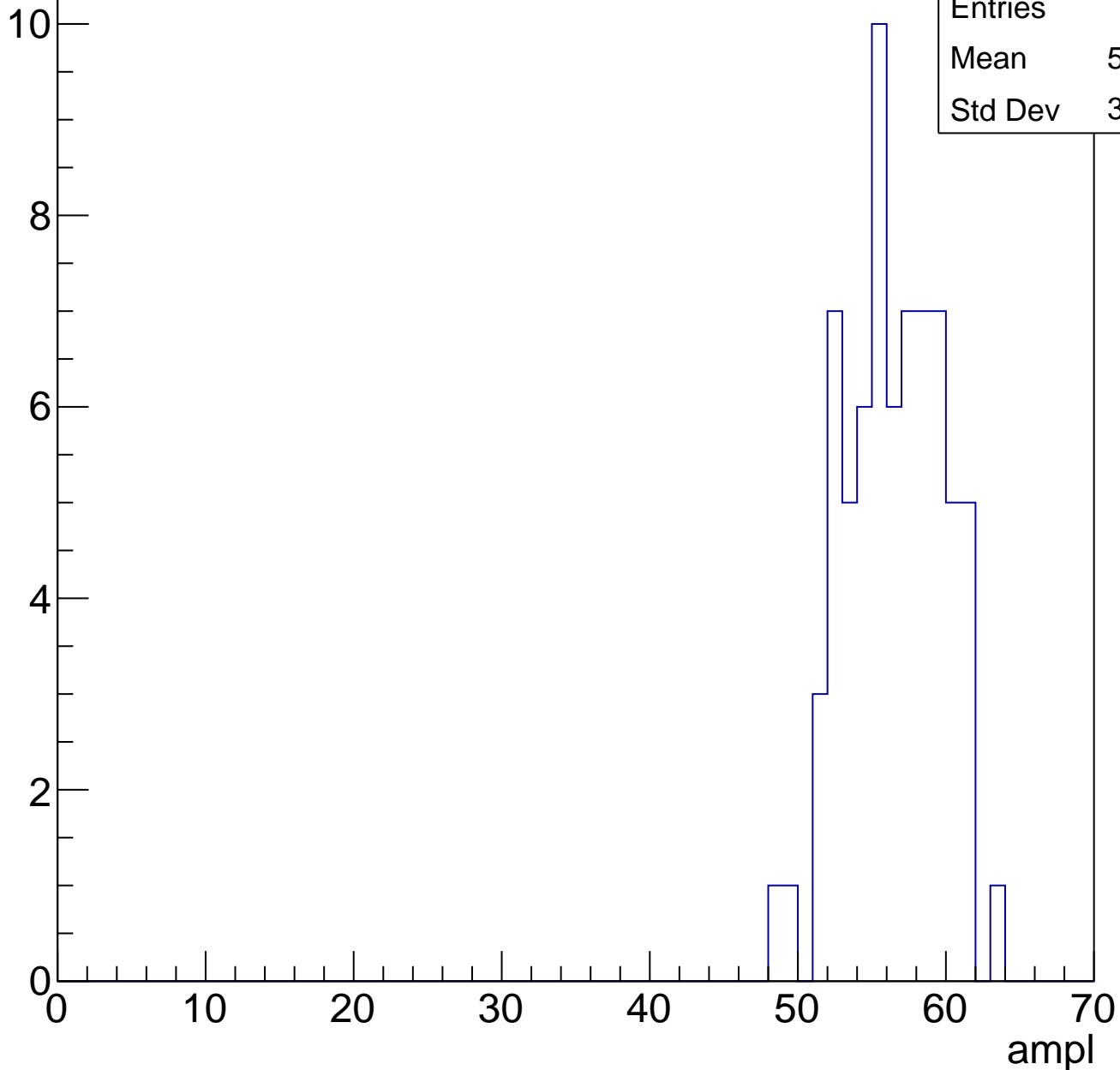


# B1L101S, U9-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	71
Mean	55.99
Std Dev	3.209

Entry

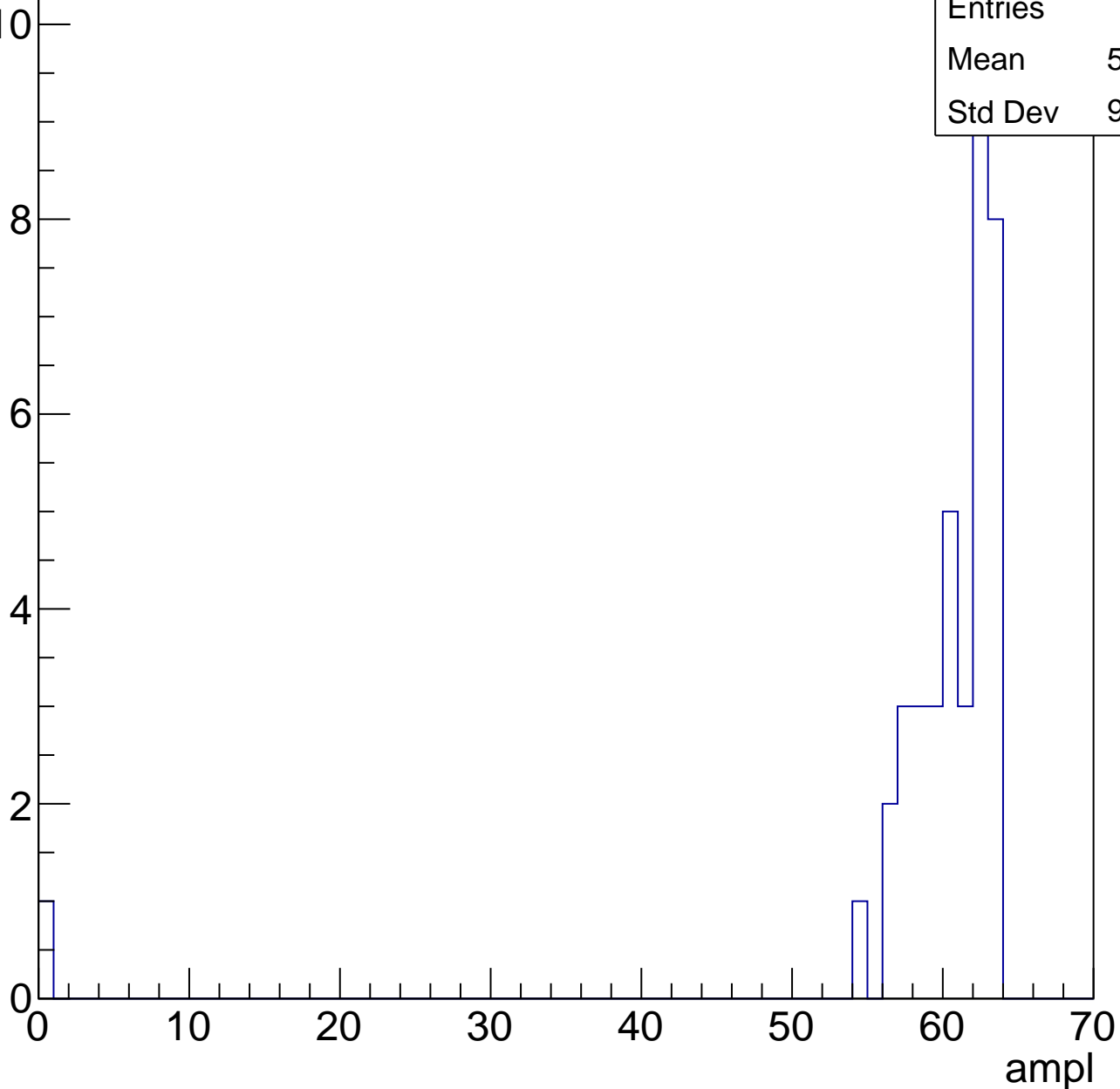


# B1L101S, U9-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	39
Mean	58.85
Std Dev	9.836



# B1L101S, U9-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U9-ch14, adc0

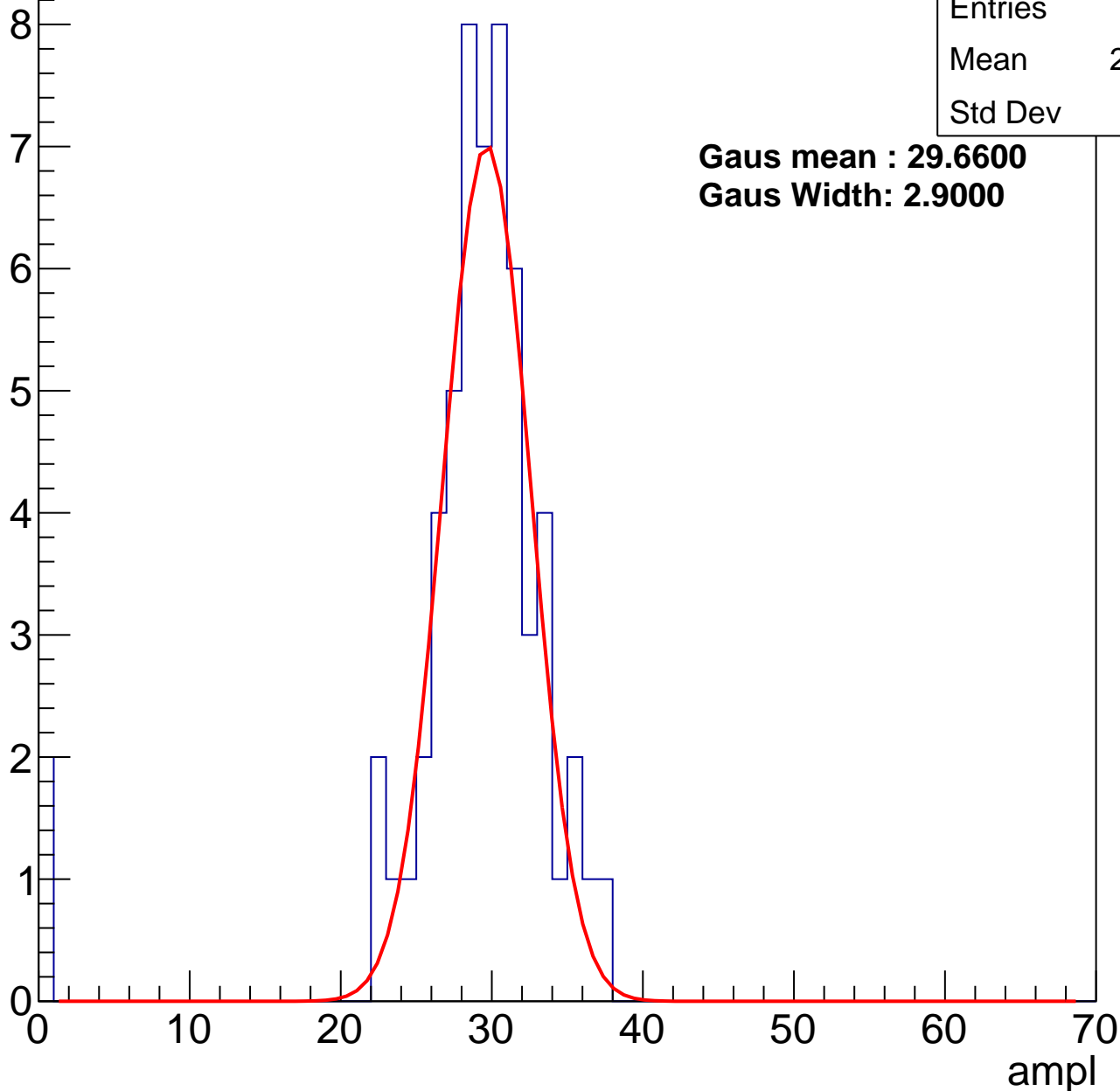
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	28.24
Std Dev	6.21

**Gaus mean : 29.6600**

**Gaus Width: 2.9000**



# B1L101S, U9-ch14, adc1

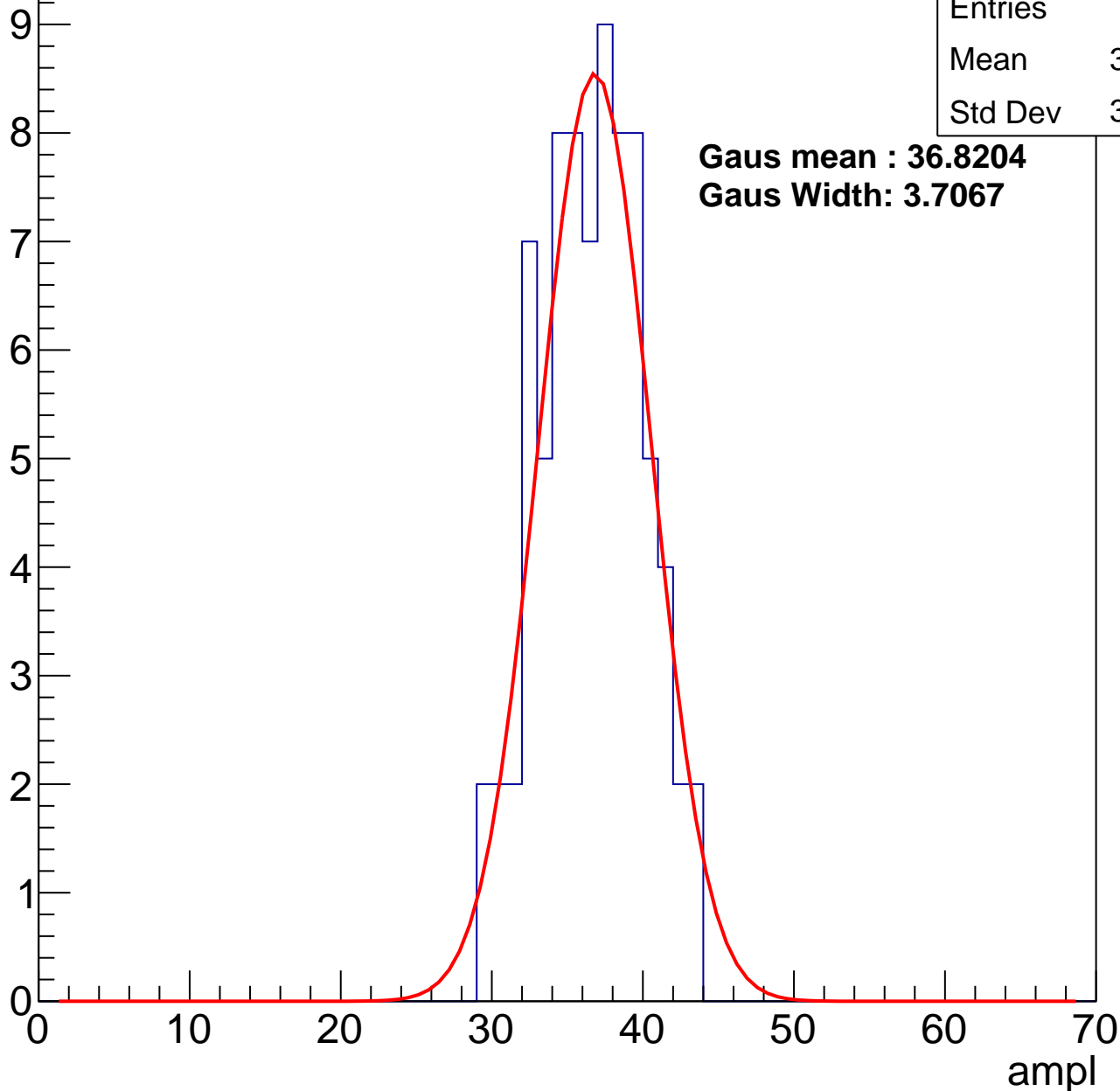
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	36.15
Std Dev	3.334

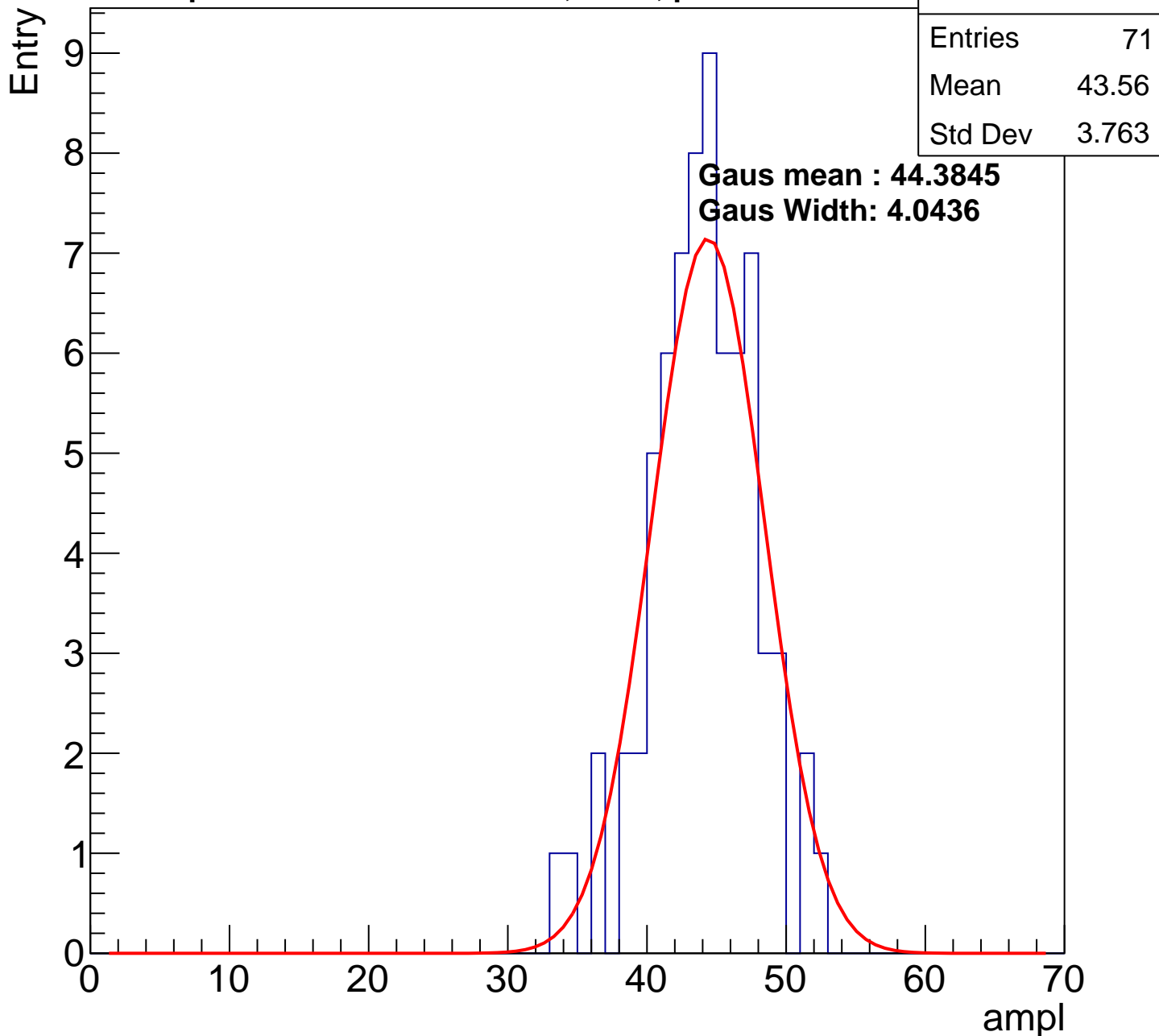
**Gaus mean : 36.8204**

**Gaus Width: 3.7067**



# B1L101S, U9-ch14, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

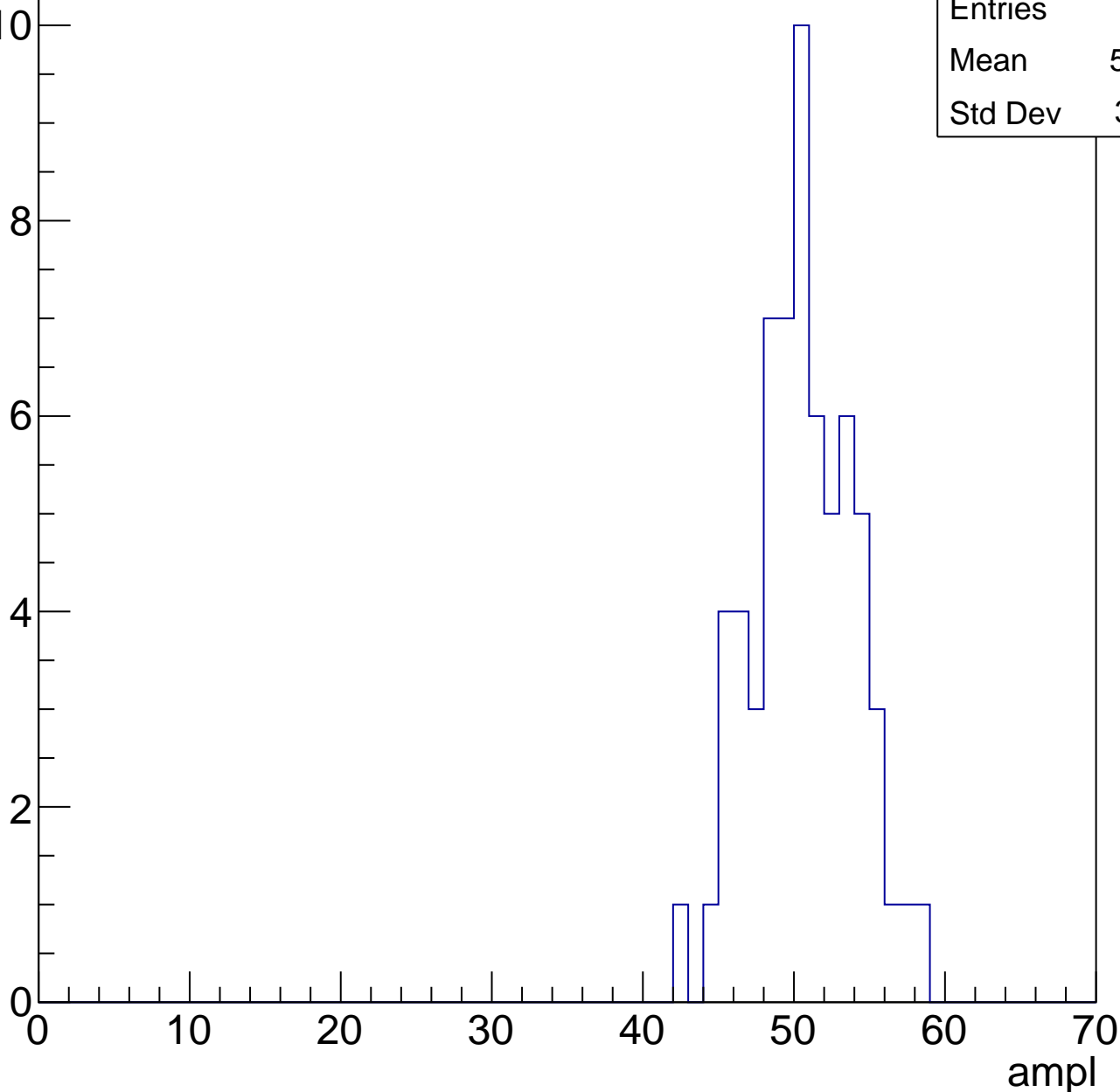


# B1L101S, U9-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

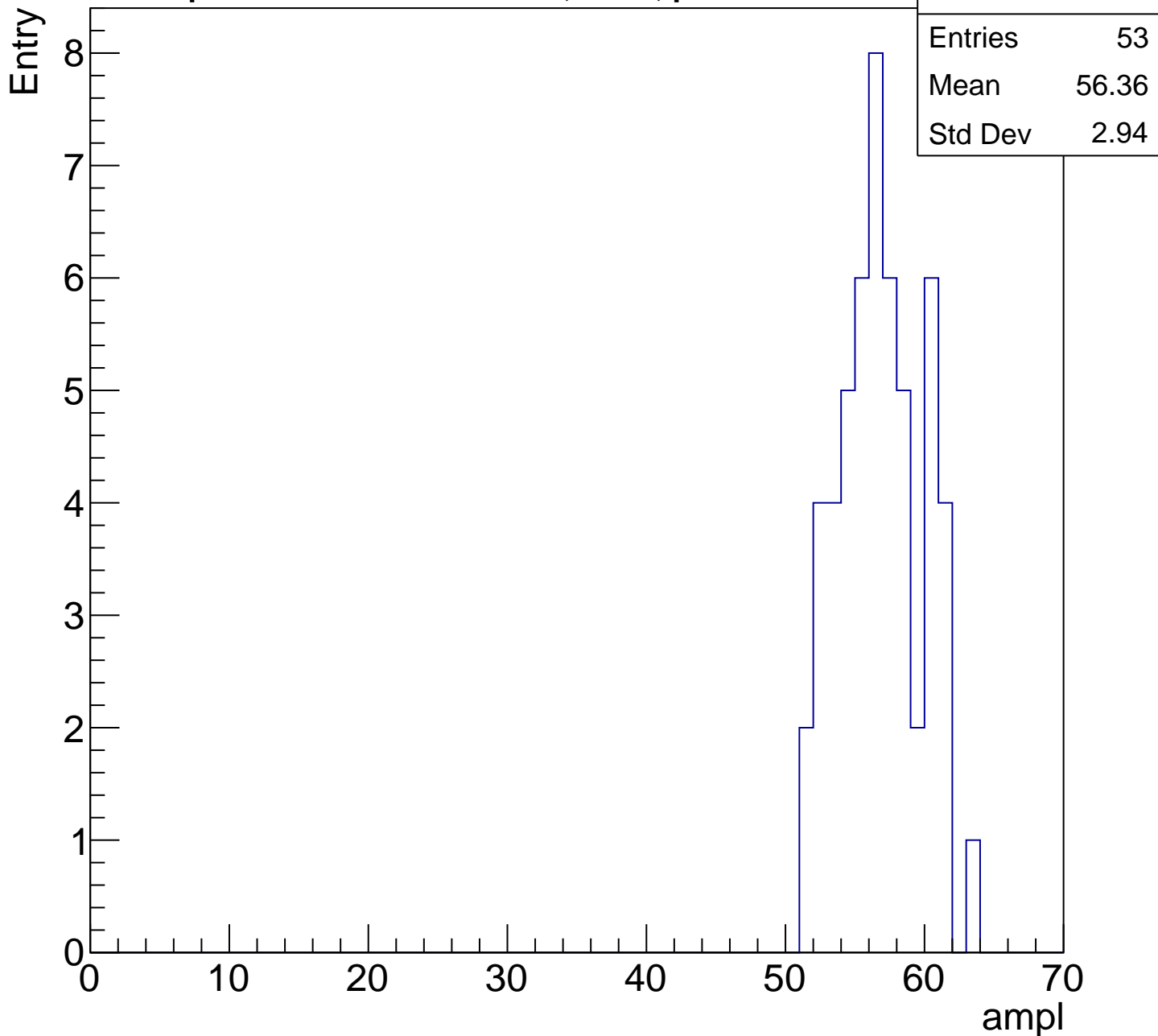
Entry

Entries	65
Mean	50.15
Std Dev	3.301



# B1L101S, U9-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

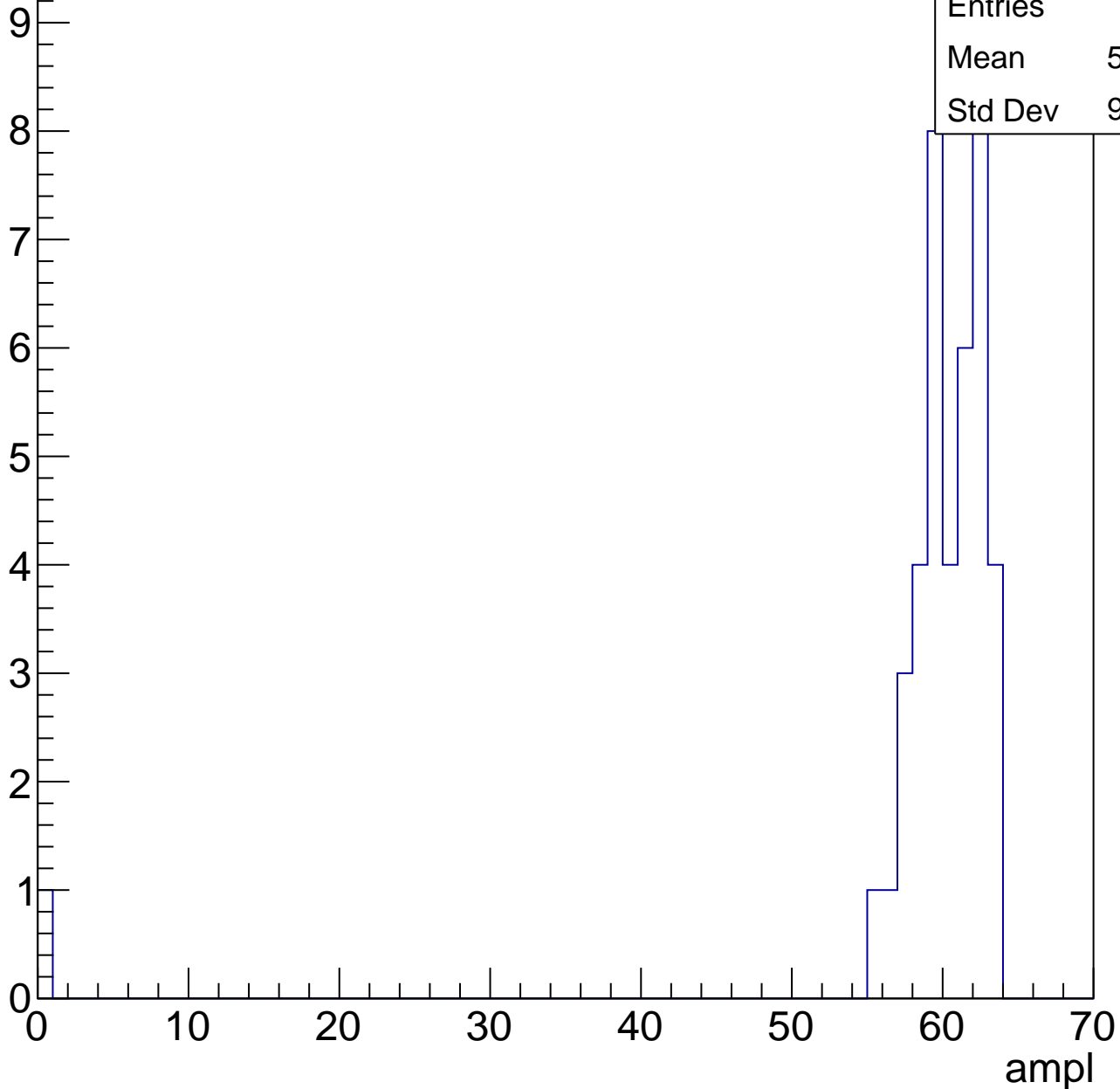


# B1L101S, U9-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	41
Mean	58.59
Std Dev	9.484

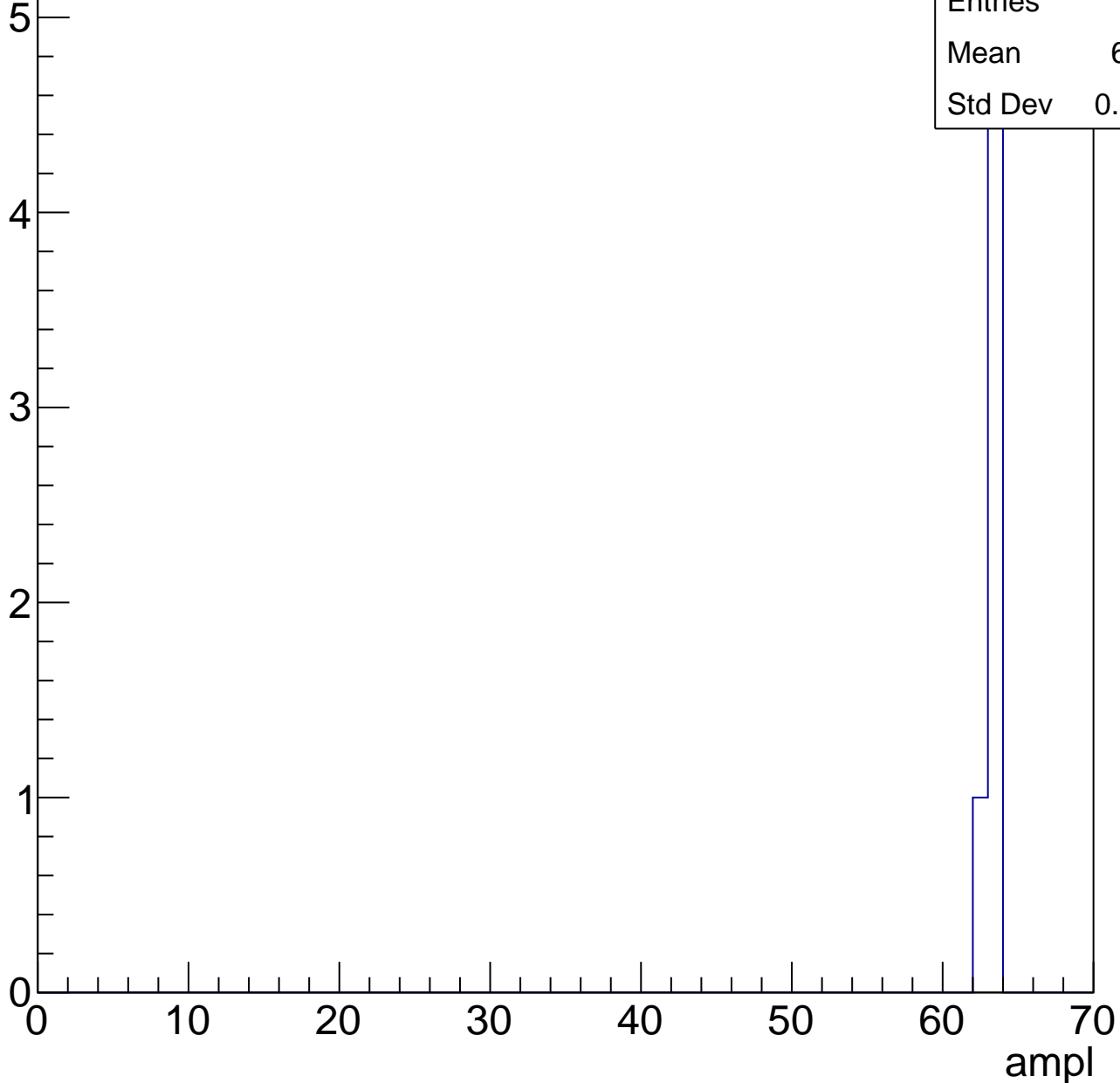


# B1L101S, U9-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	6
Mean	62.83
Std Dev	0.3727

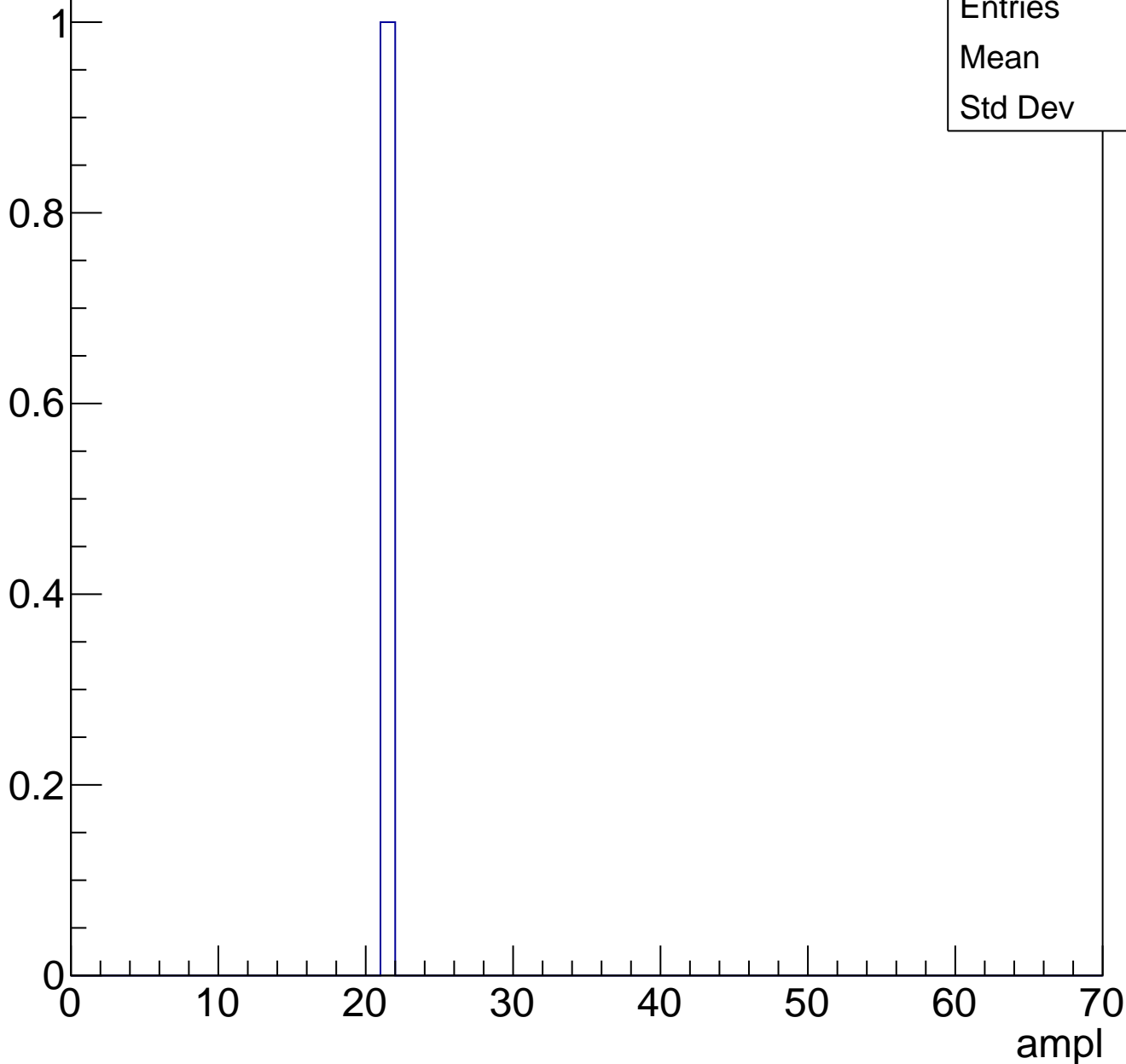




# B1L101S, U9-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch15, adc0

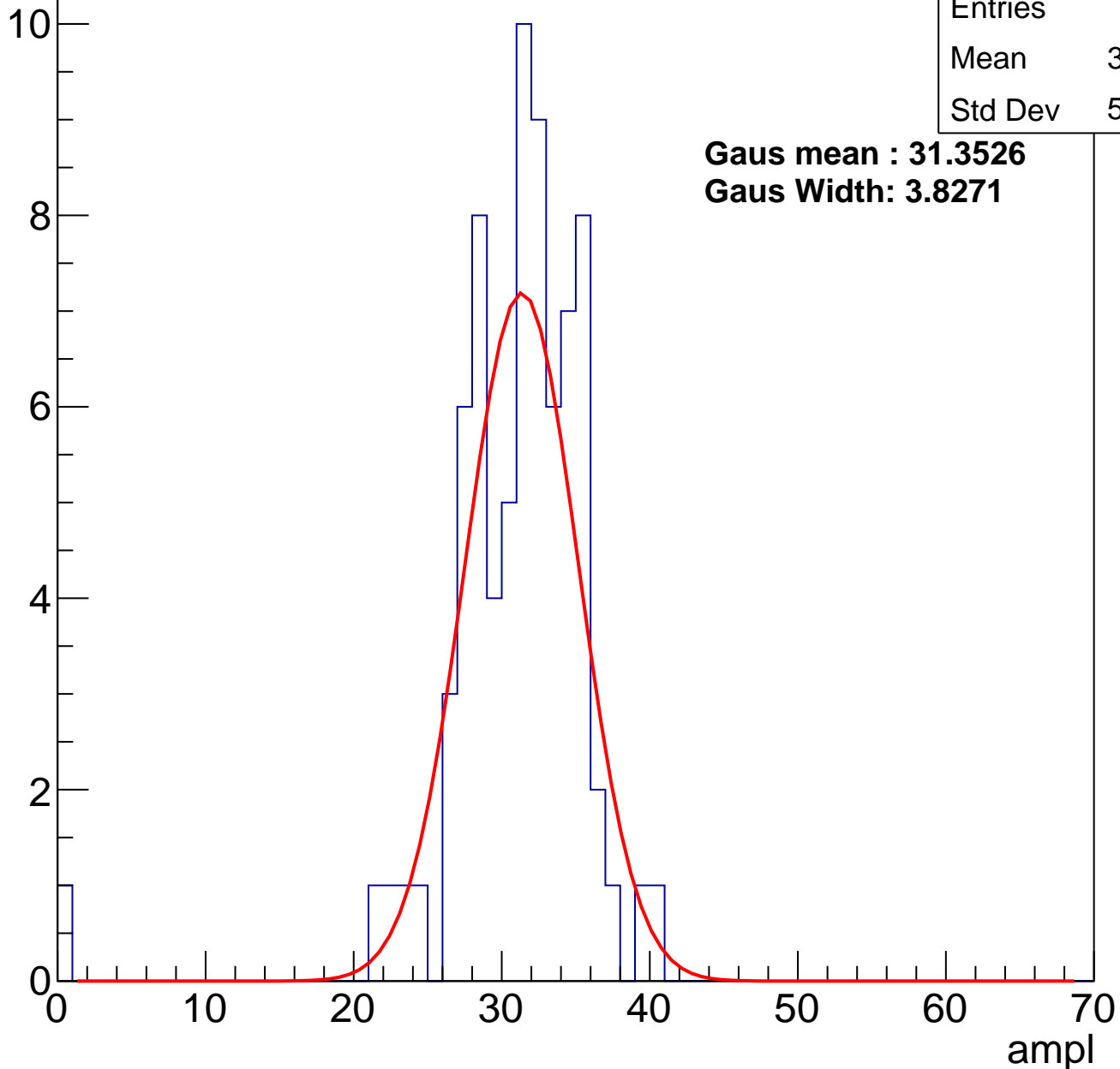
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	76
Mean	30.55
Std Dev	5.077

**Gaus mean : 31.3526**

**Gaus Width: 3.8271**

Entry



# B1L101S, U9-ch15, adc1

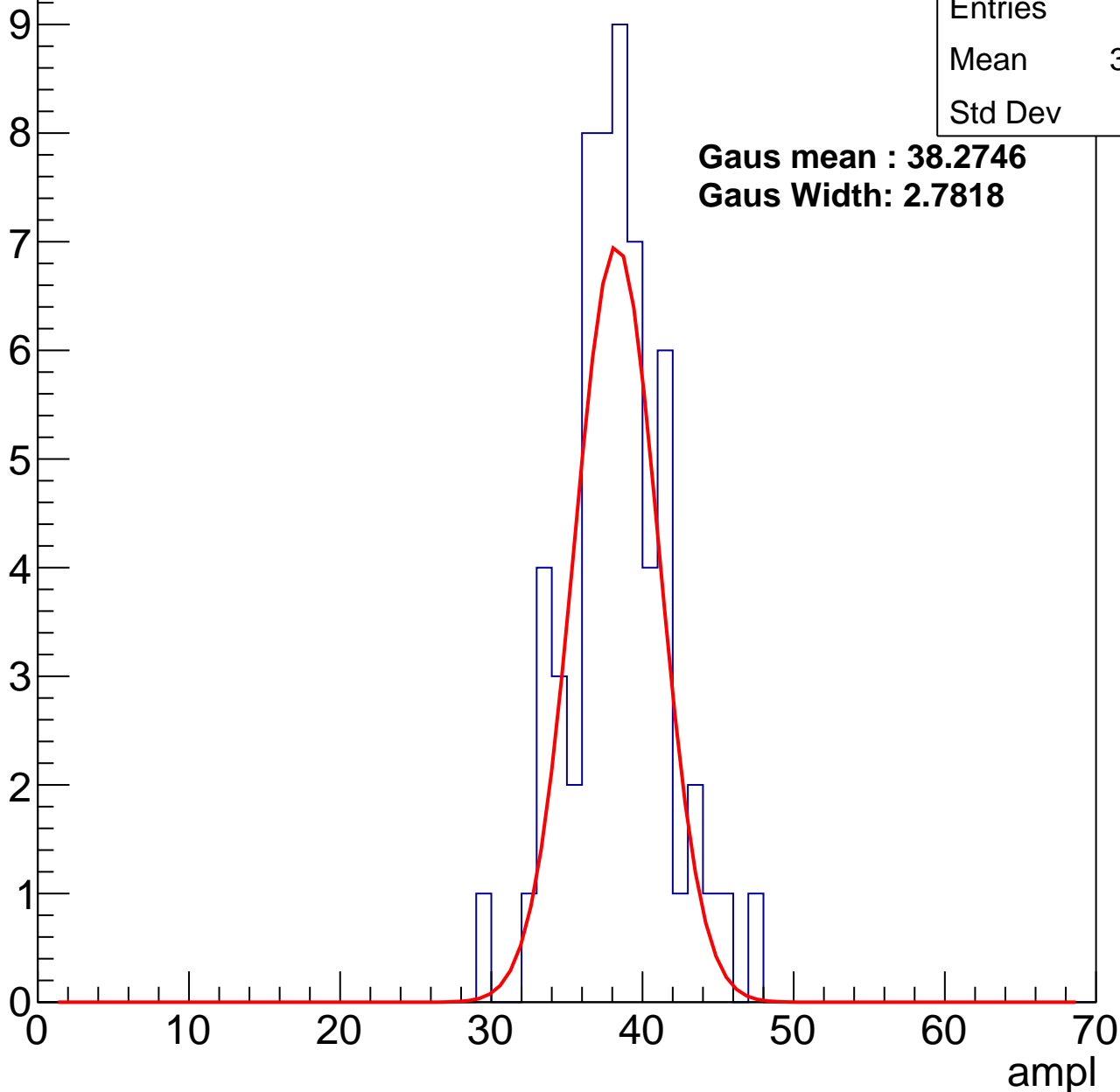
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	37.86
Std Dev	3.27

**Gaus mean : 38.2746**

**Gaus Width: 2.7818**



# B1L101S, U9-ch15, adc2

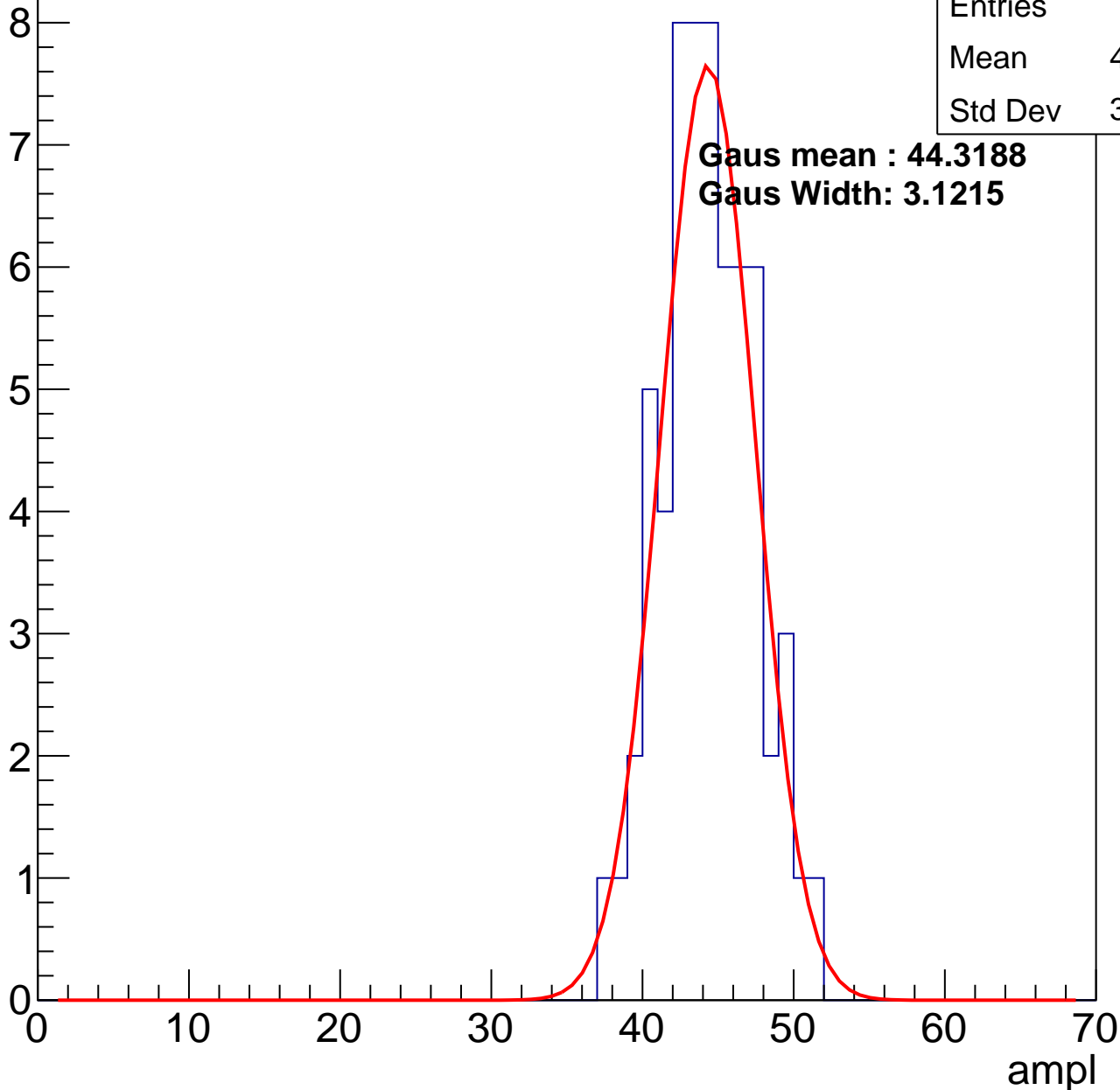
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	43.89
Std Dev	3.022

**Gaus mean : 44.3188**

**Gaus Width: 3.1215**

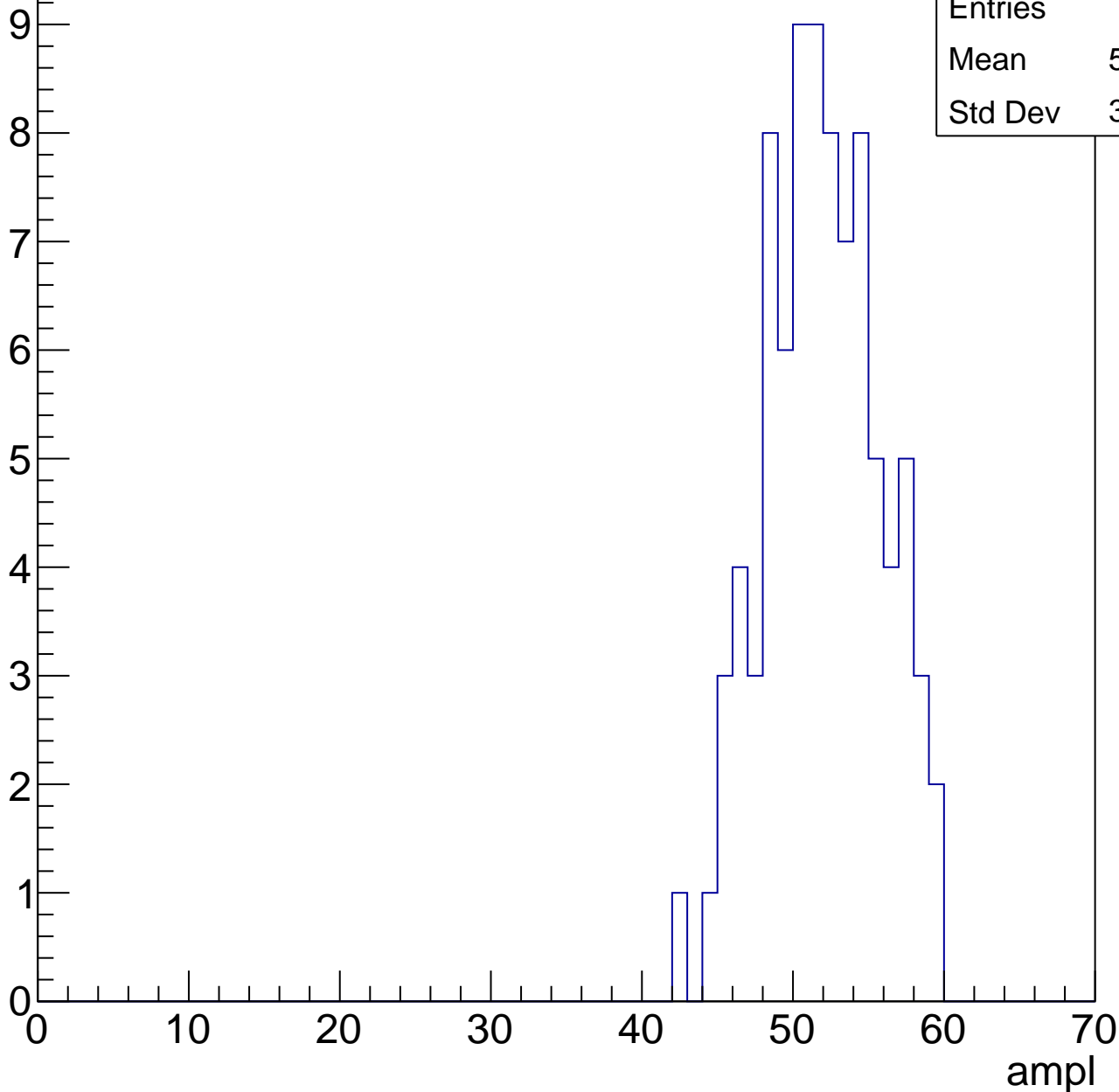


# B1L101S, U9-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	86
Mean	51.49
Std Dev	3.756

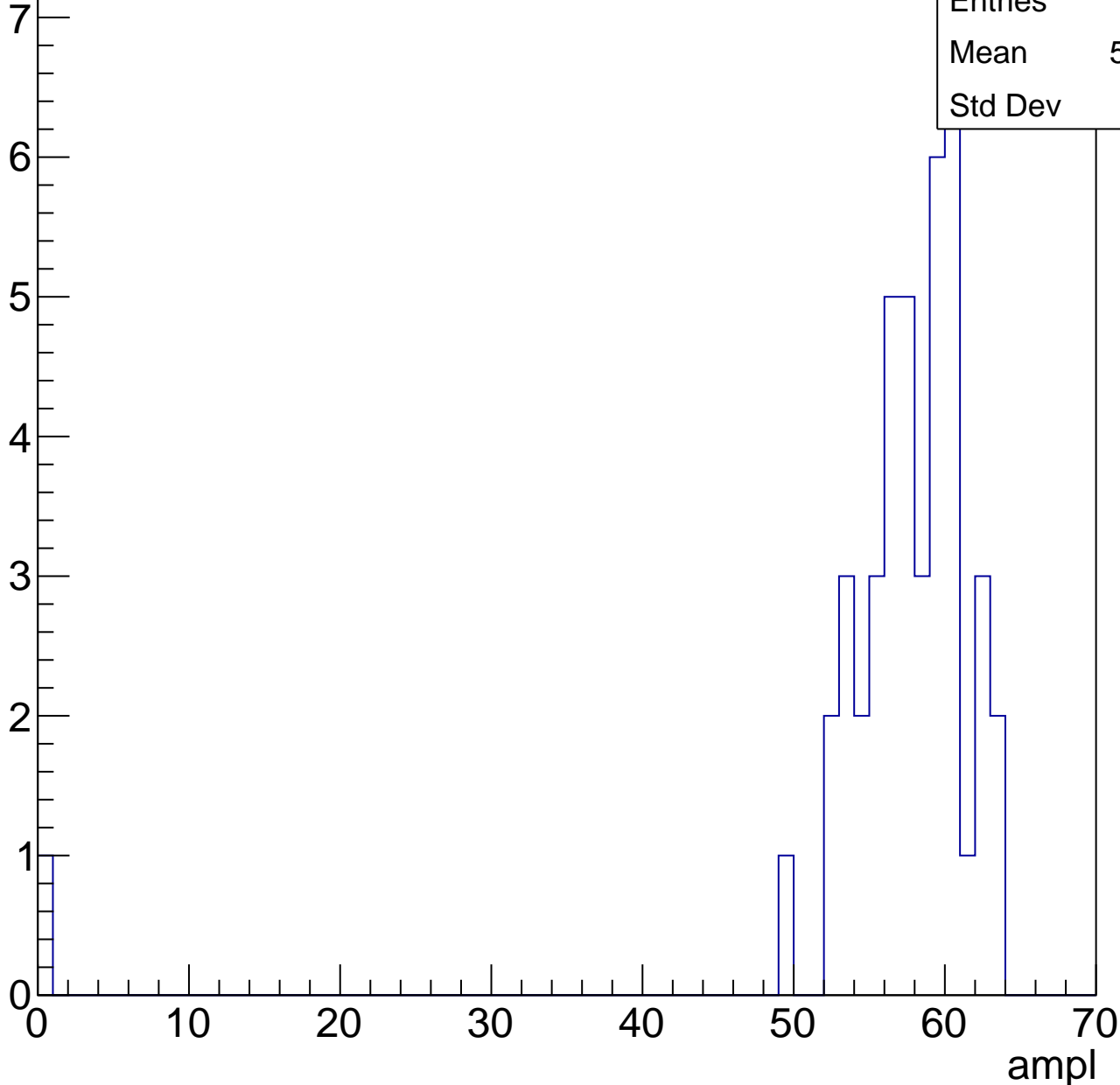


# B1L101S, U9-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	44
Mean	56.16
Std Dev	9.13

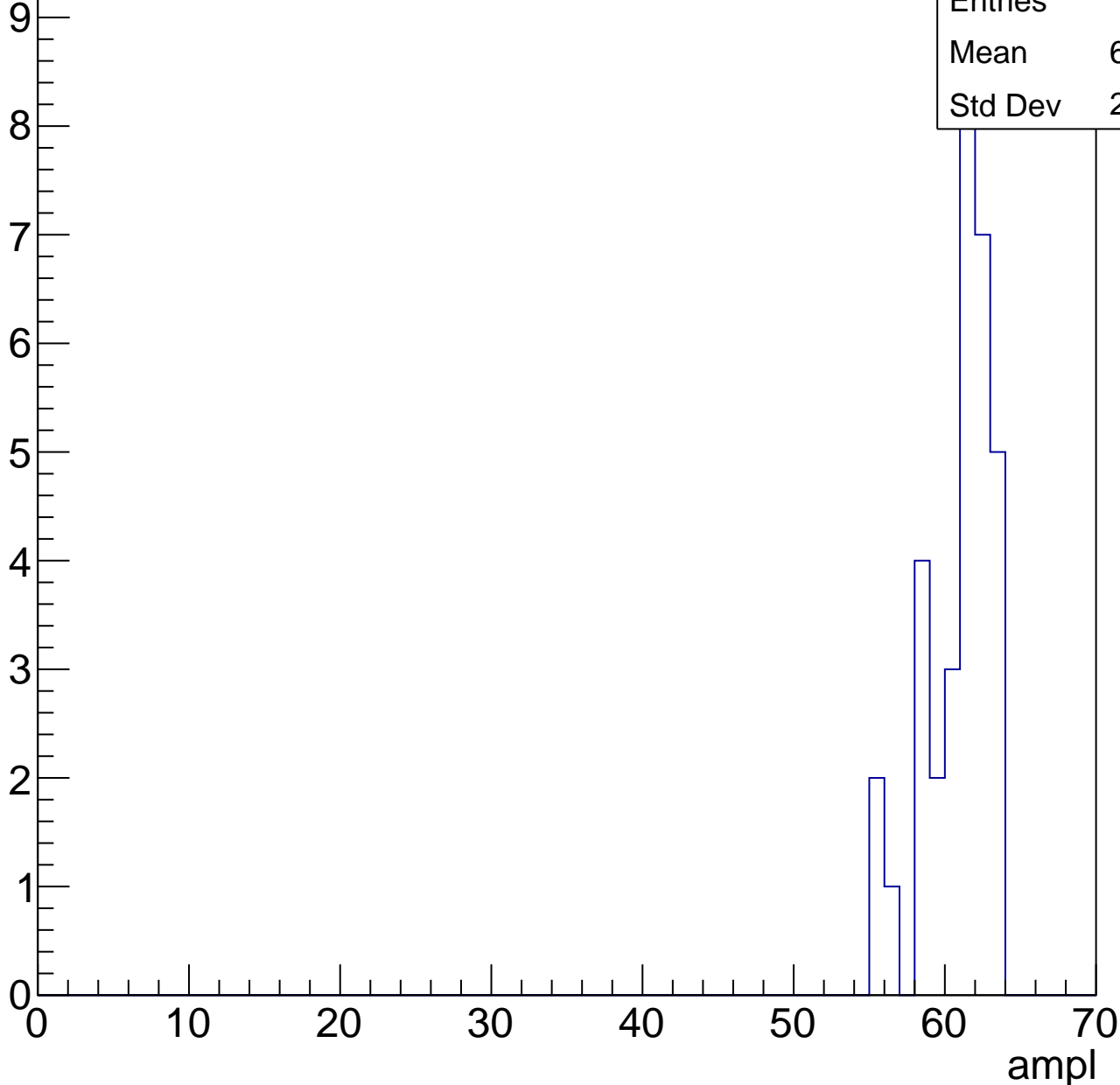


# B1L101S, U9-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	33
Mean	60.42
Std Dev	2.202



# B1L101S, U9-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U9-ch16, adc0

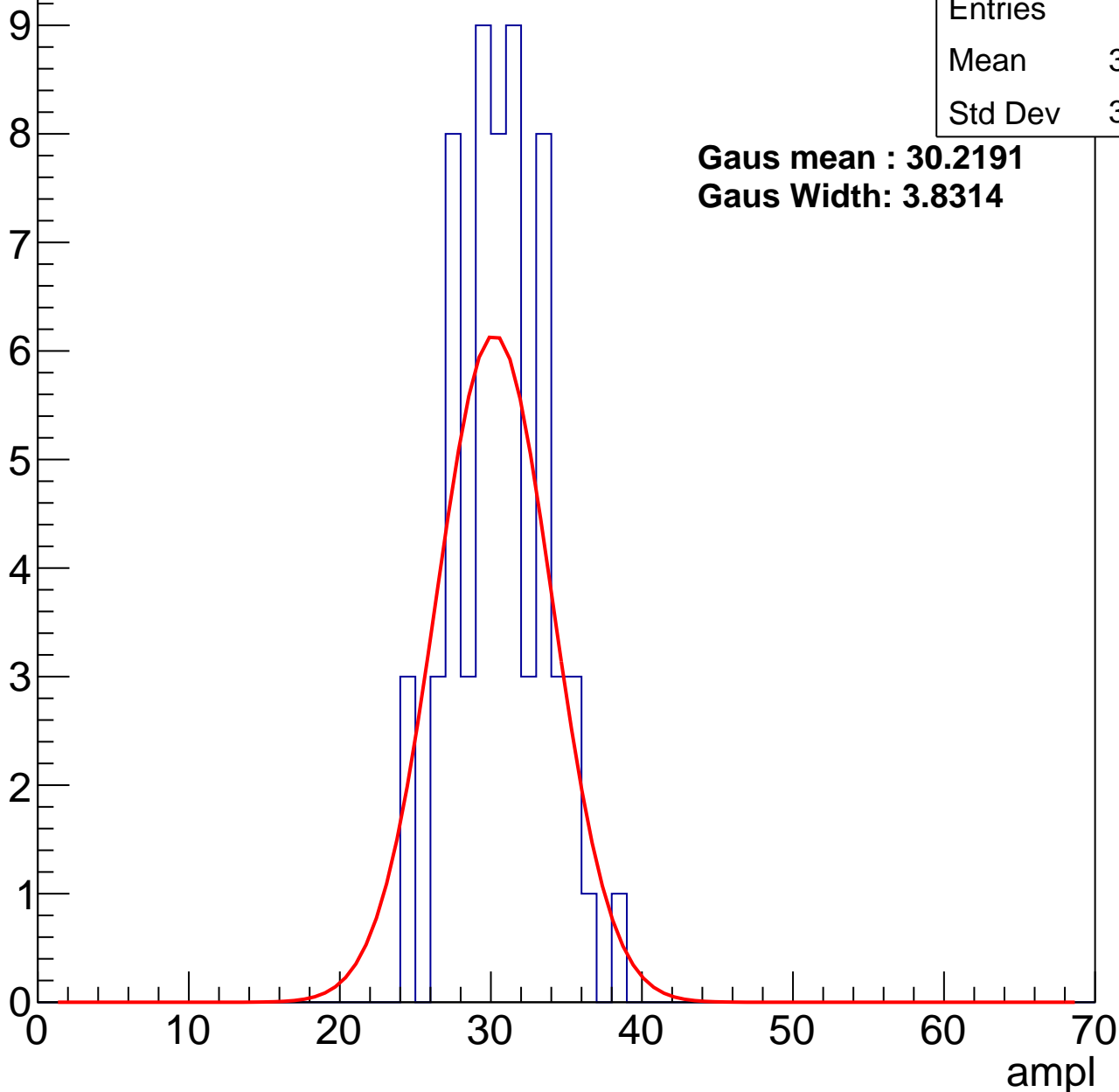
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	30.18
Std Dev	3.014

**Gaus mean : 30.2191**

**Gaus Width: 3.8314**



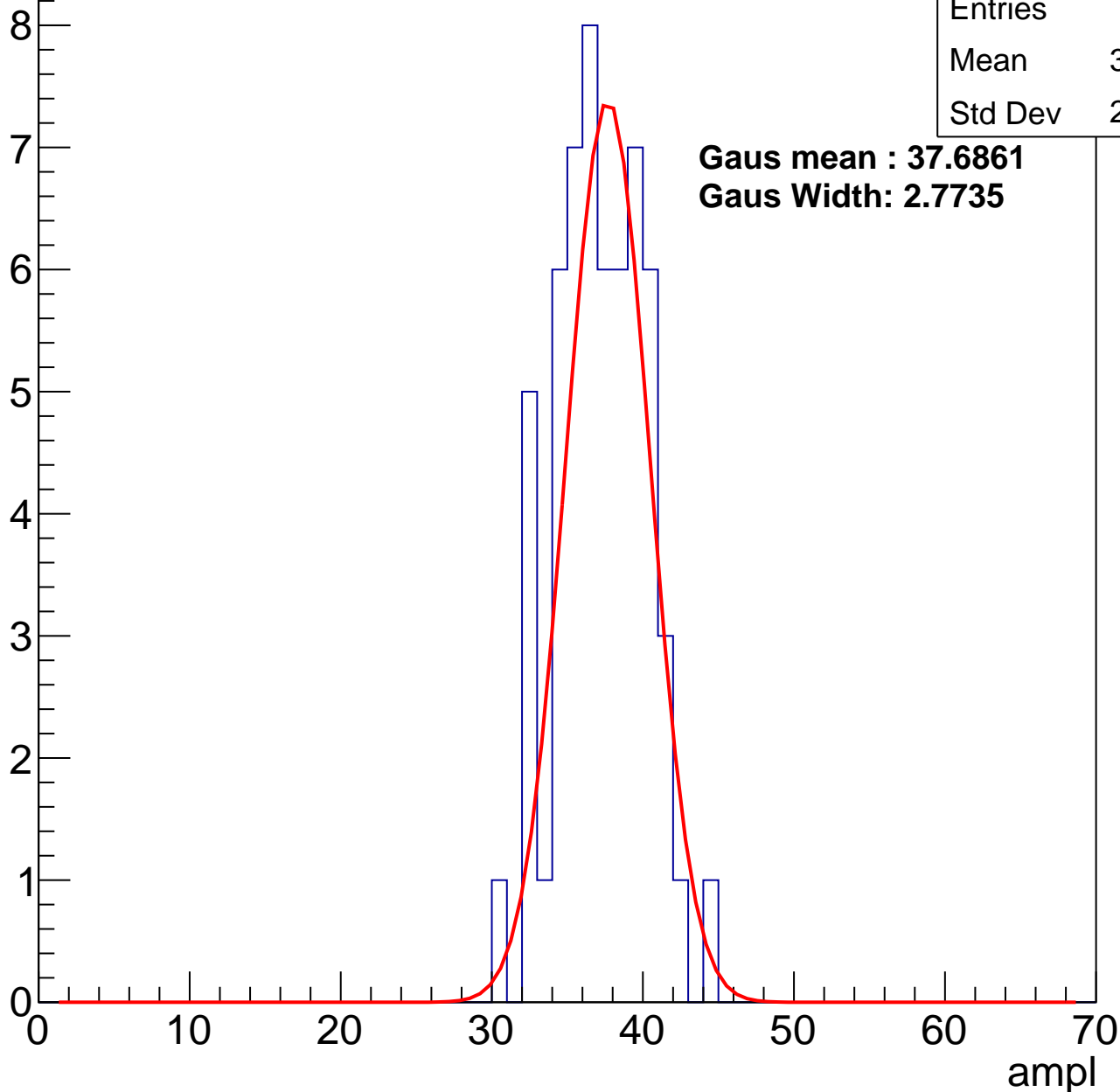
# B1L101S, U9-ch16, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	36.76
Std Dev	2.897

**Gaus mean : 37.6861**  
**Gaus Width: 2.7735**



# B1L101S, U9-ch16, adc2

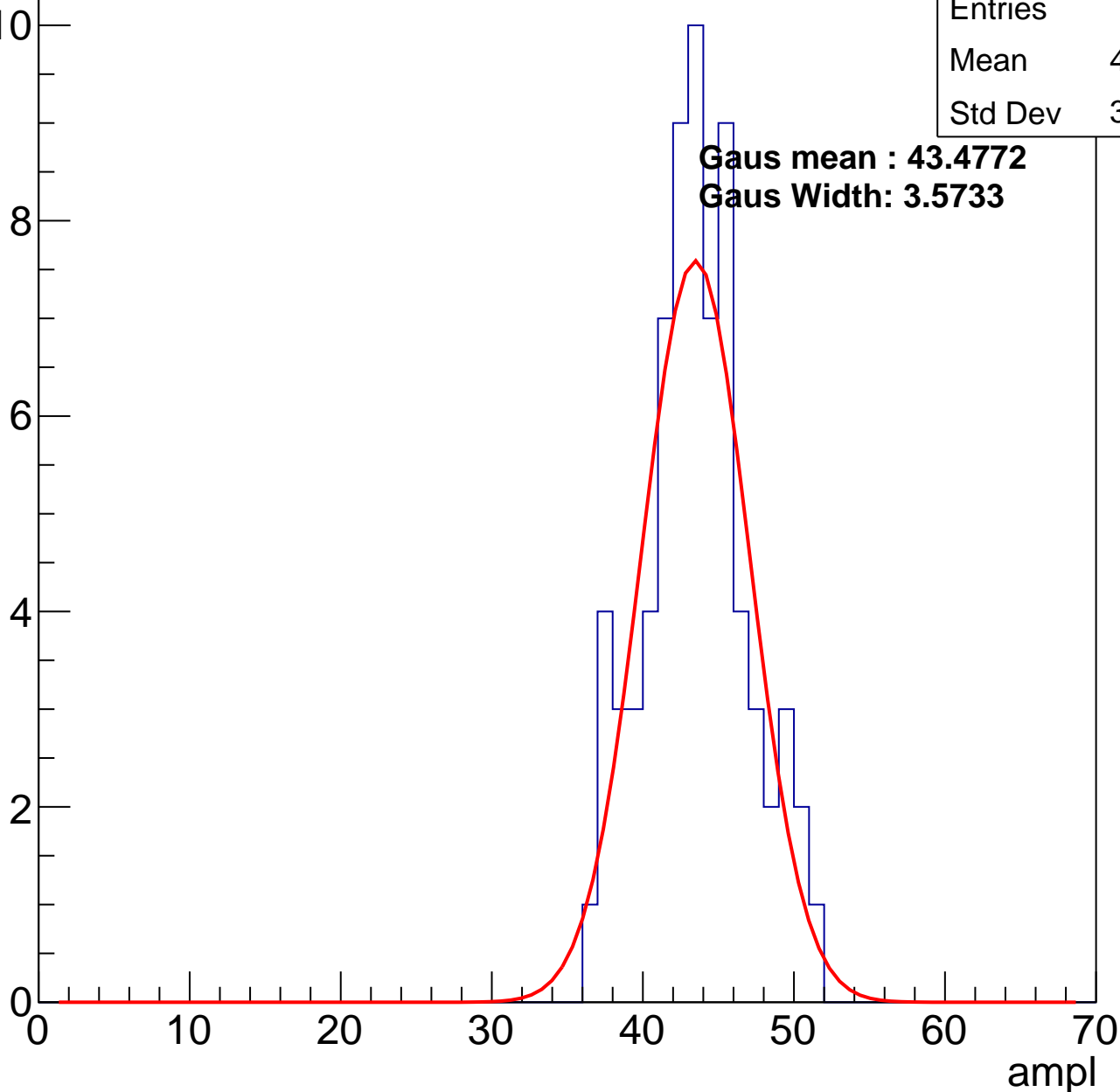
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	43.08
Std Dev	3.406

**Gaus mean : 43.4772**

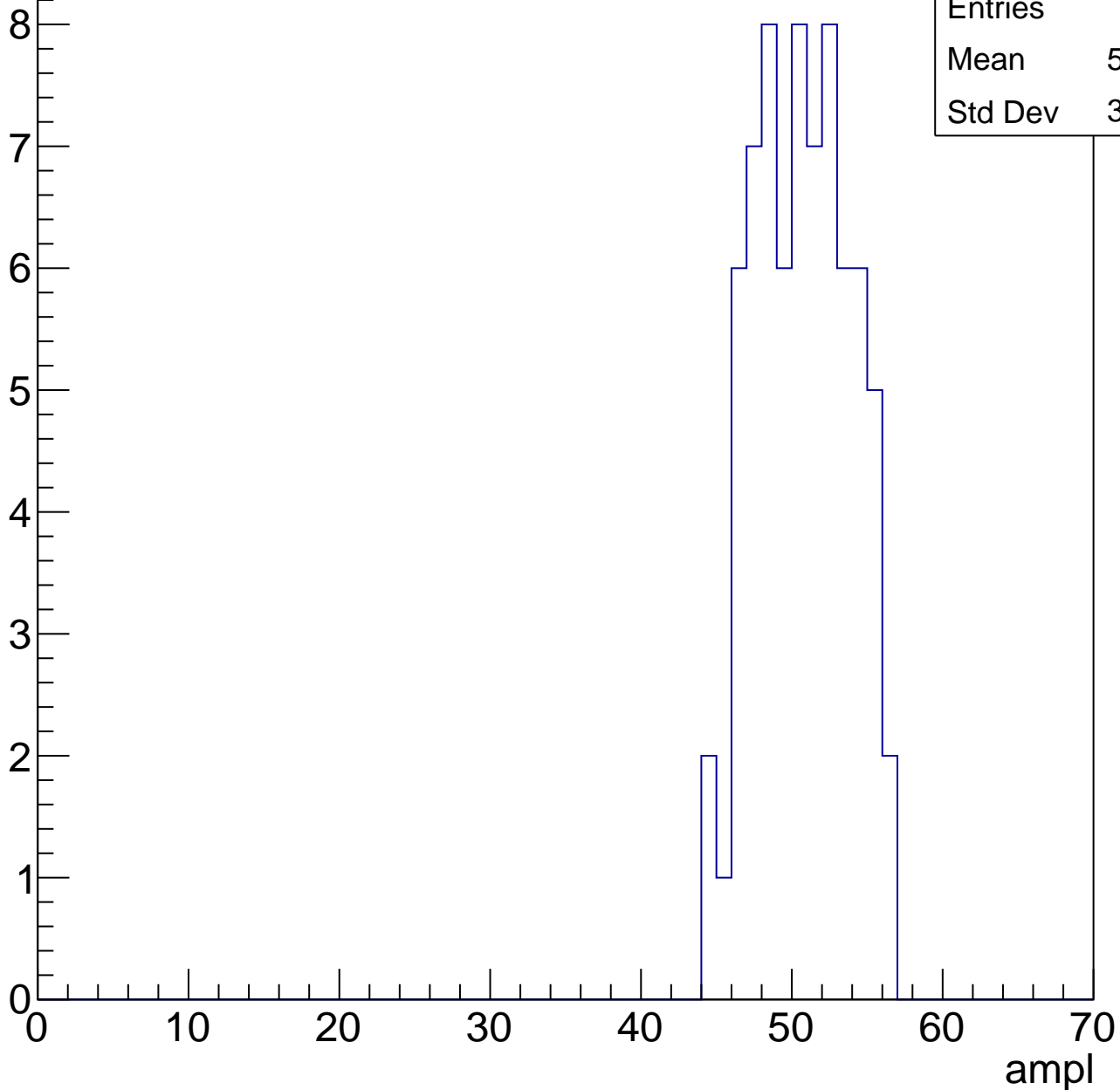
**Gaus Width: 3.5733**



# B1L101S, U9-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

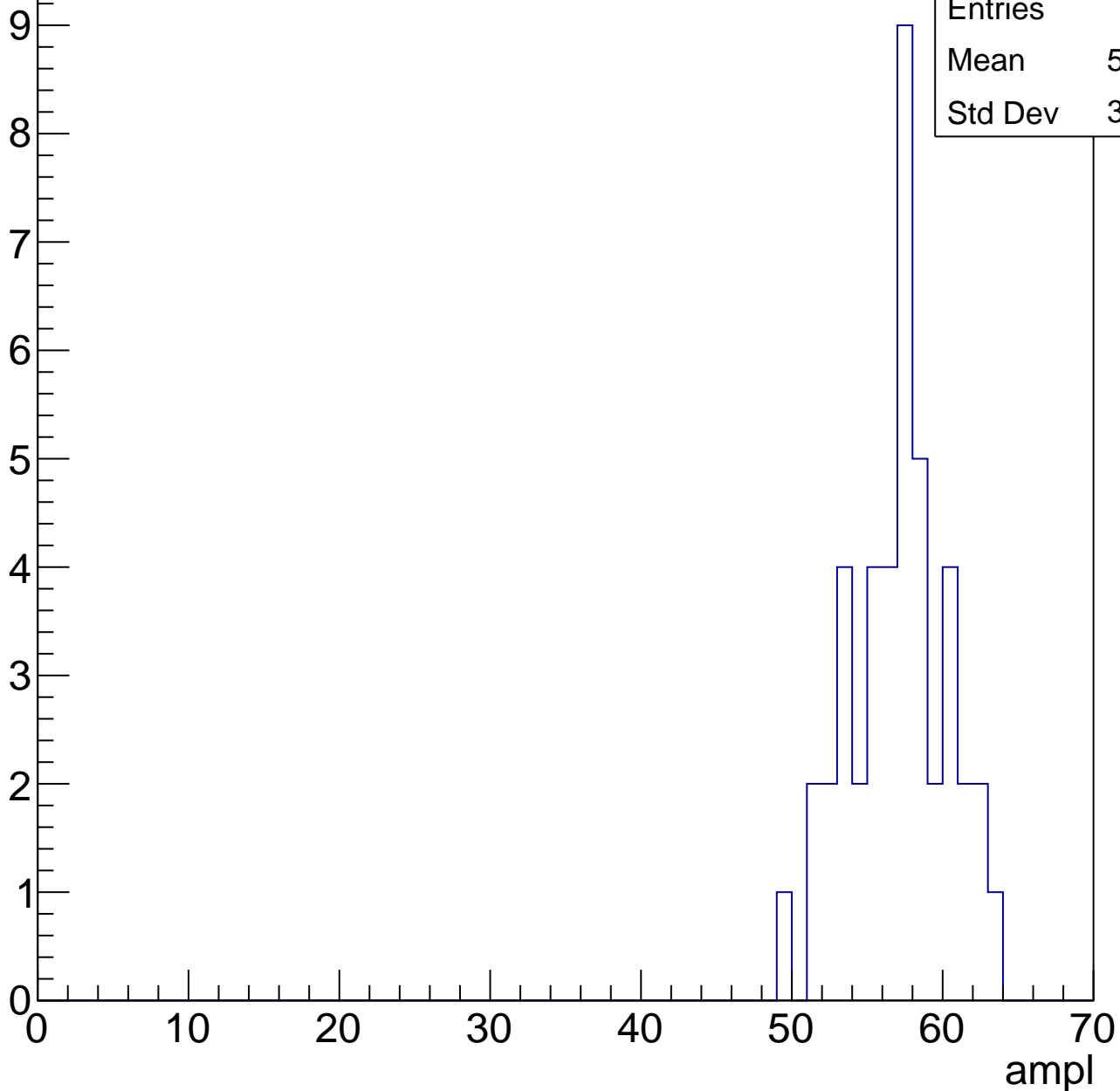


# B1L101S, U9-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

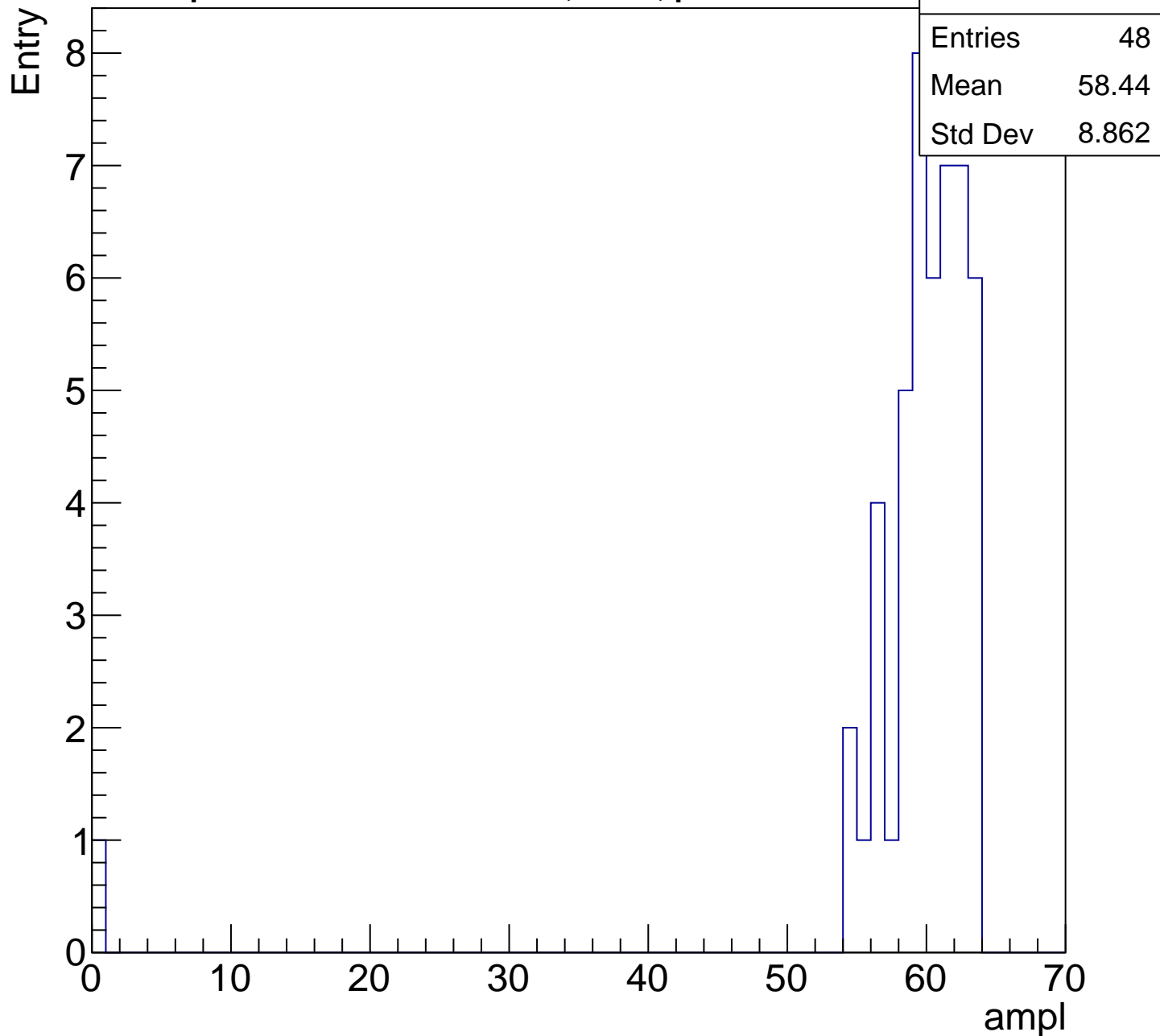
Entry

Entries	44
Mean	56.57
Std Dev	3.187



# B1L101S, U9-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U9-ch17, adc0

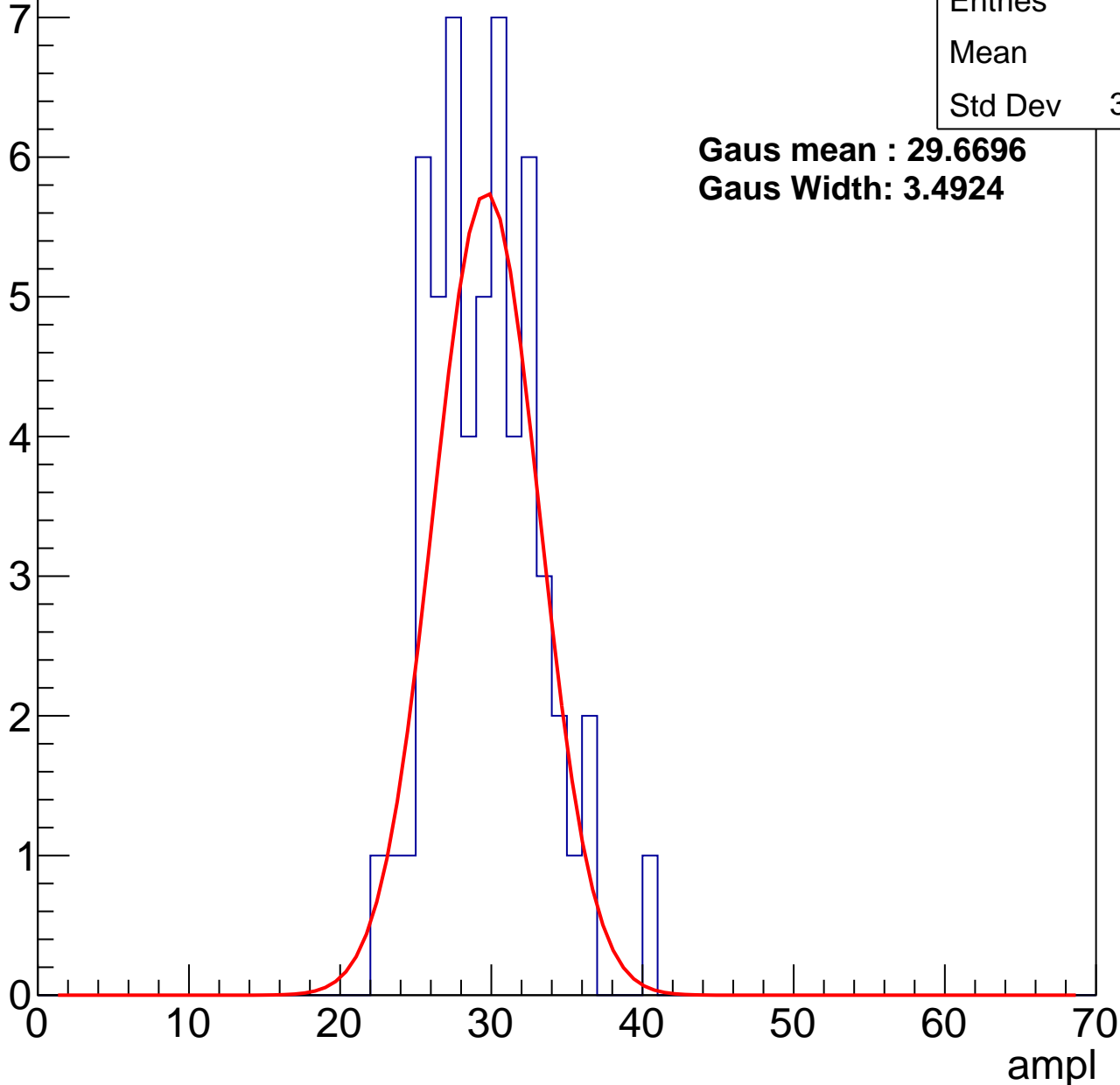
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	29.2
Std Dev	3.563

**Gaus mean : 29.6696**

**Gaus Width: 3.4924**



# B1L101S, U9-ch17, adc1

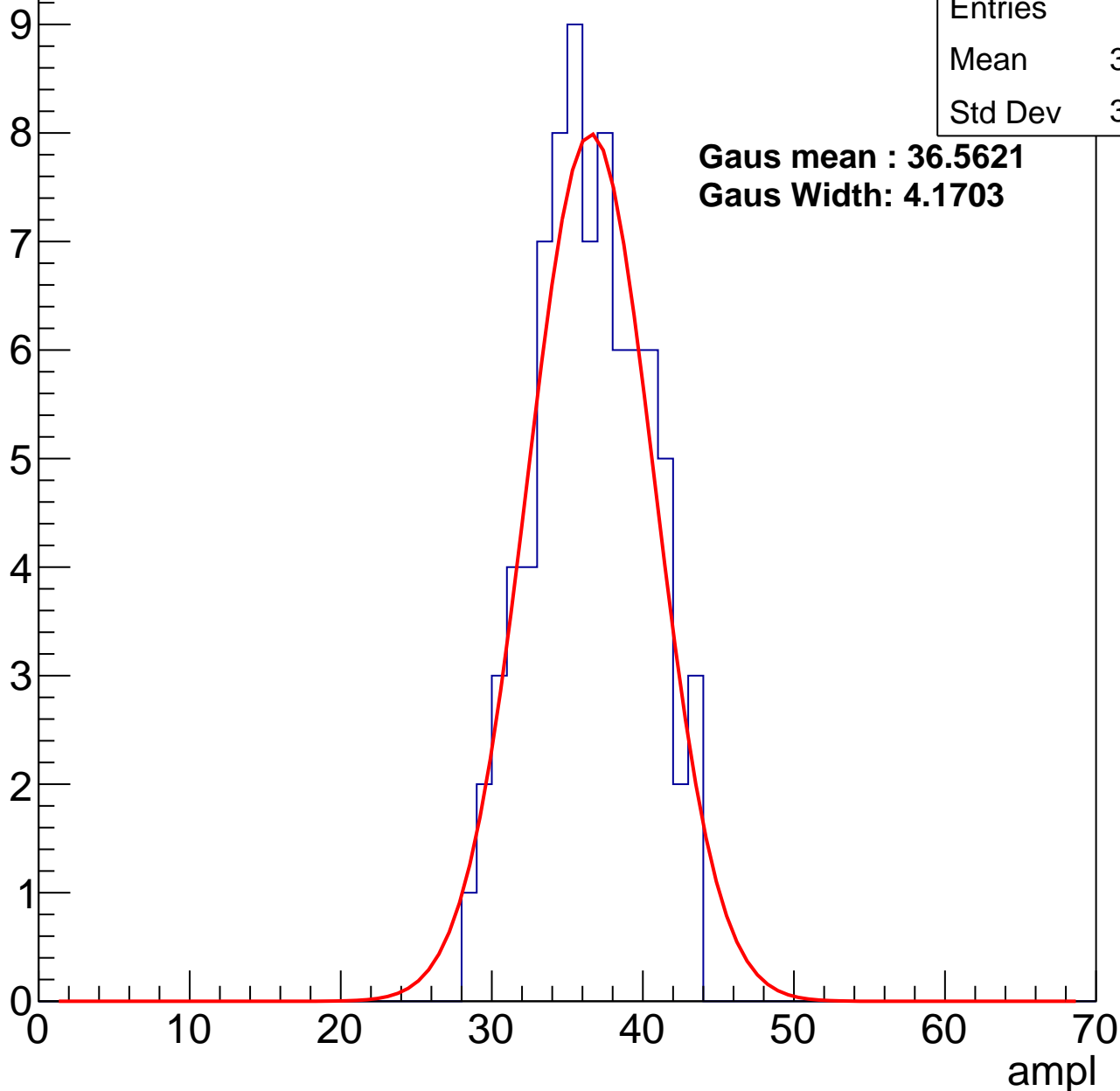
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	35.98
Std Dev	3.624

**Gaus mean : 36.5621**

**Gaus Width: 4.1703**



# B1L101S, U9-ch17, adc2

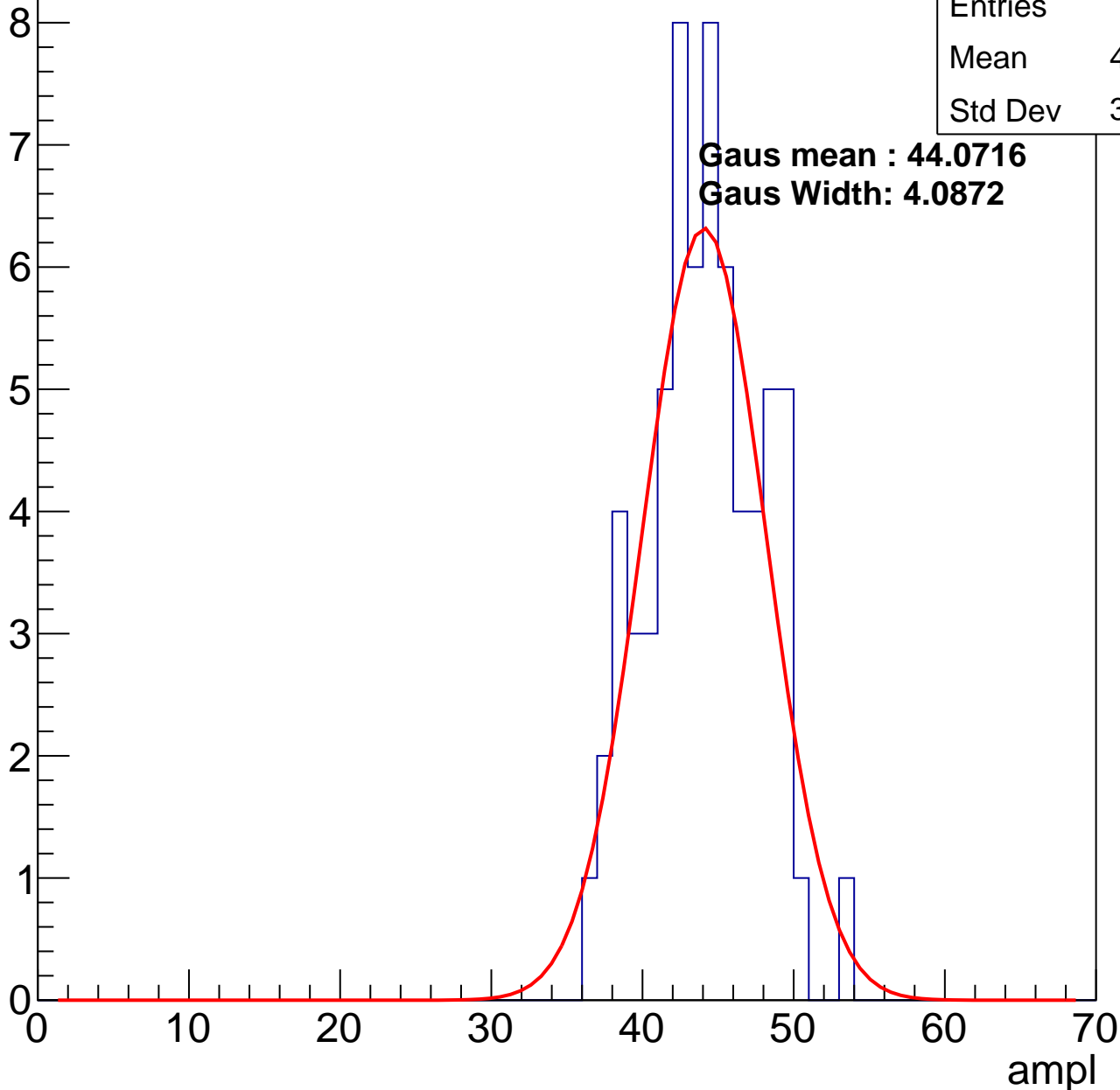
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	43.64
Std Dev	3.658

**Gaus mean : 44.0716**

**Gaus Width: 4.0872**

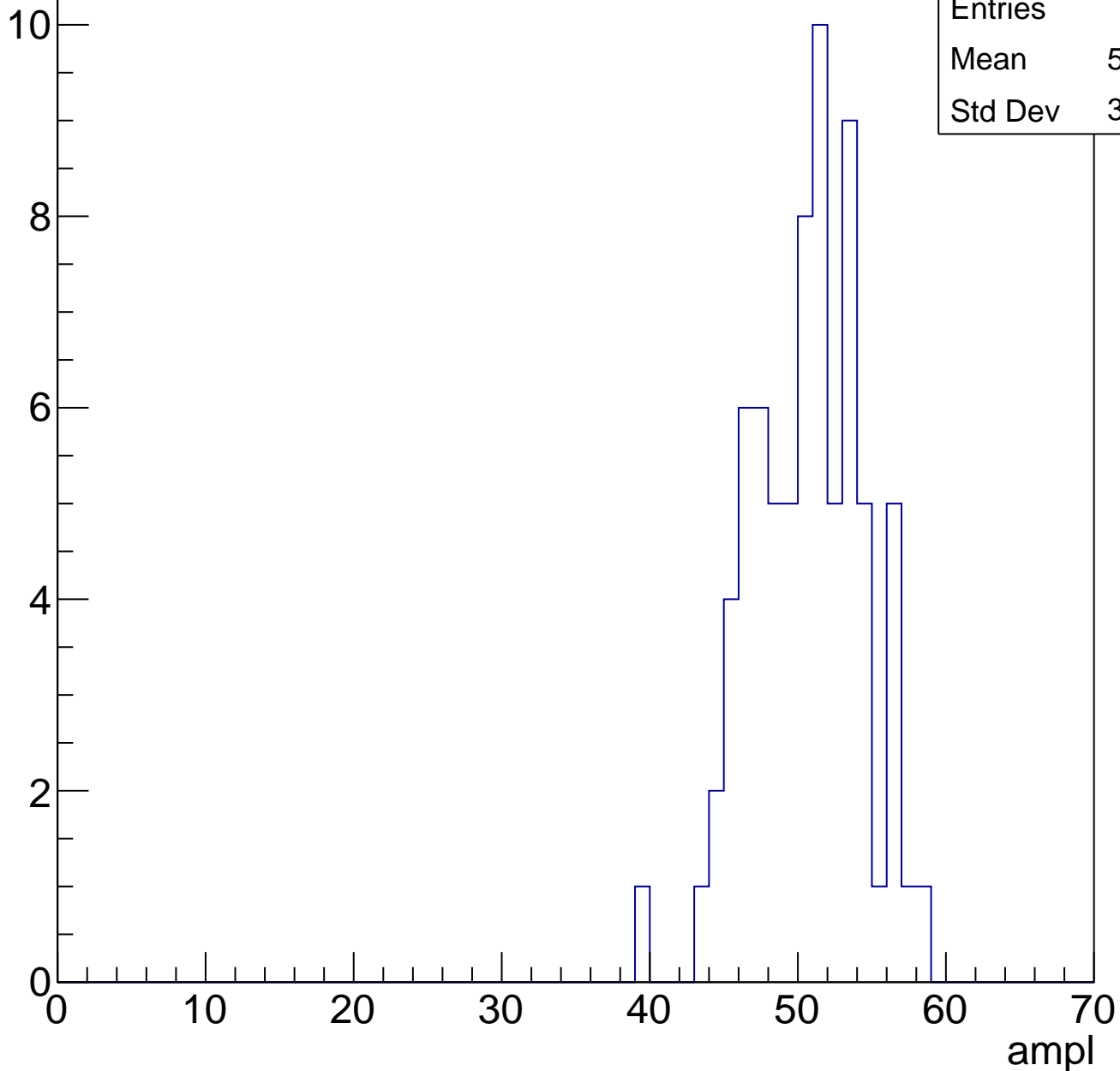


# B1L101S, U9-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	75
Mean	50.13
Std Dev	3.696

Entry

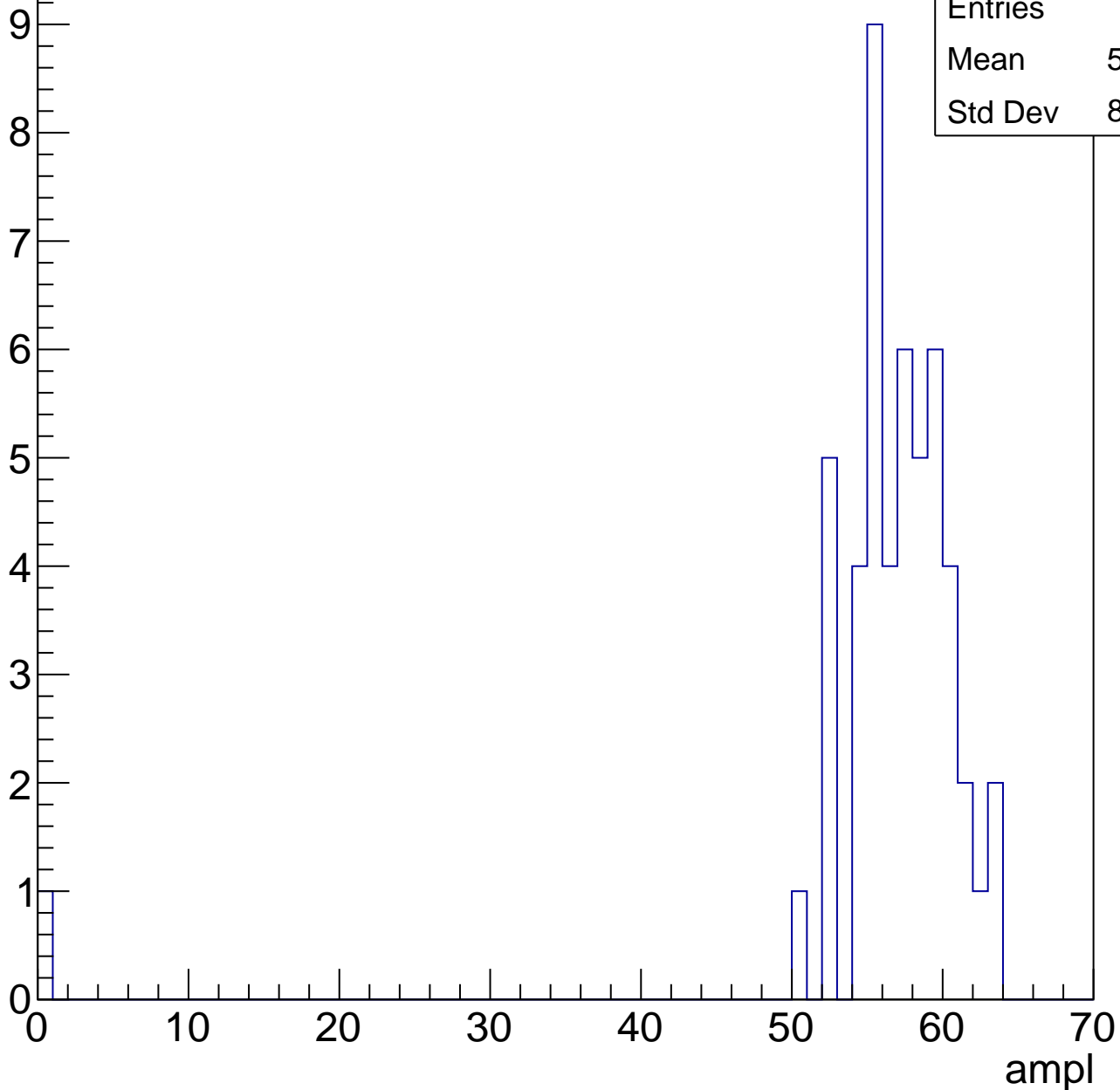


# B1L101S, U9-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	55.62
Std Dev	8.483

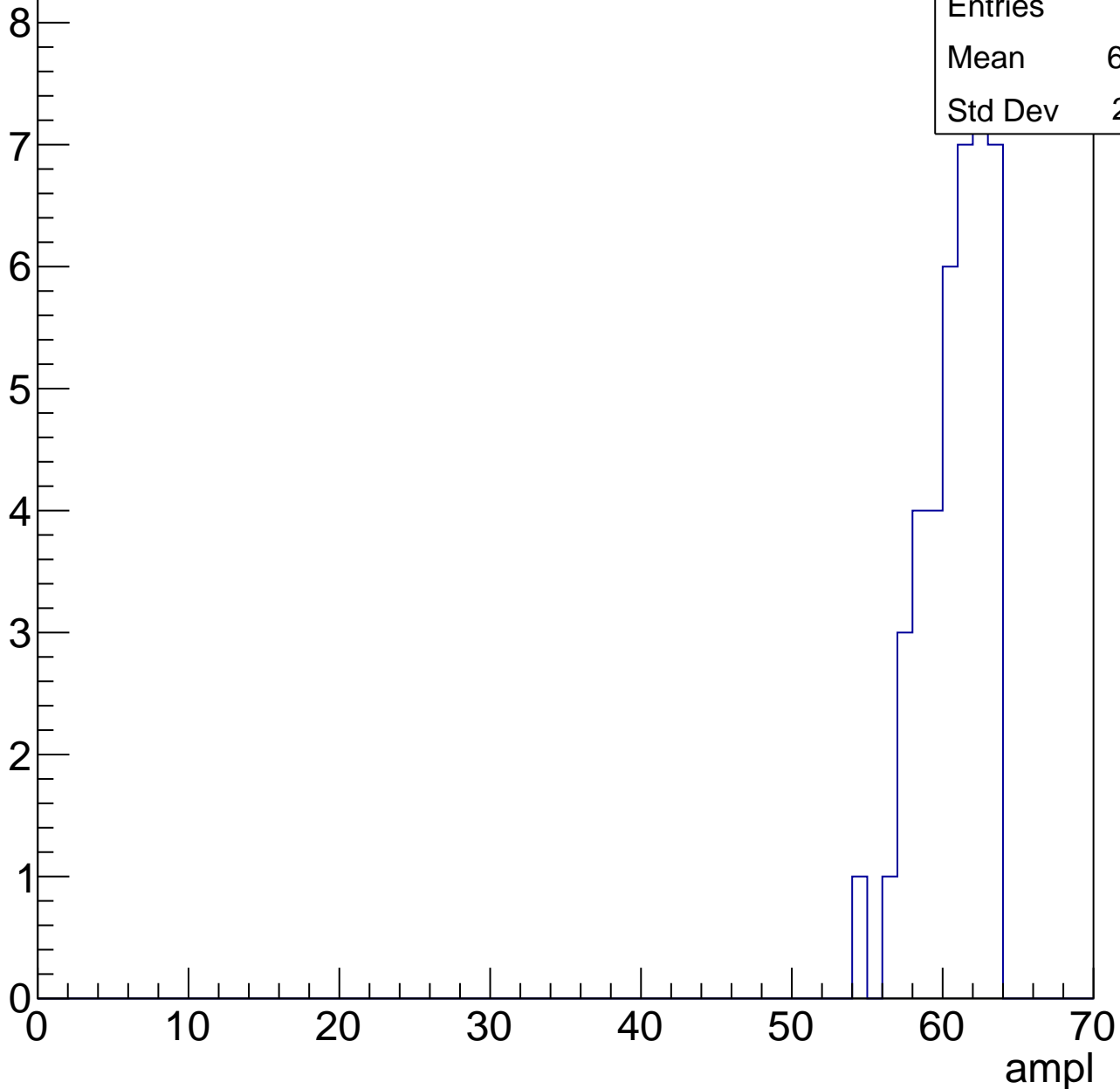


# B1L101S, U9-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	41
Mean	60.32
Std Dev	2.191



# B1L101S, U9-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U9-ch18, adc0

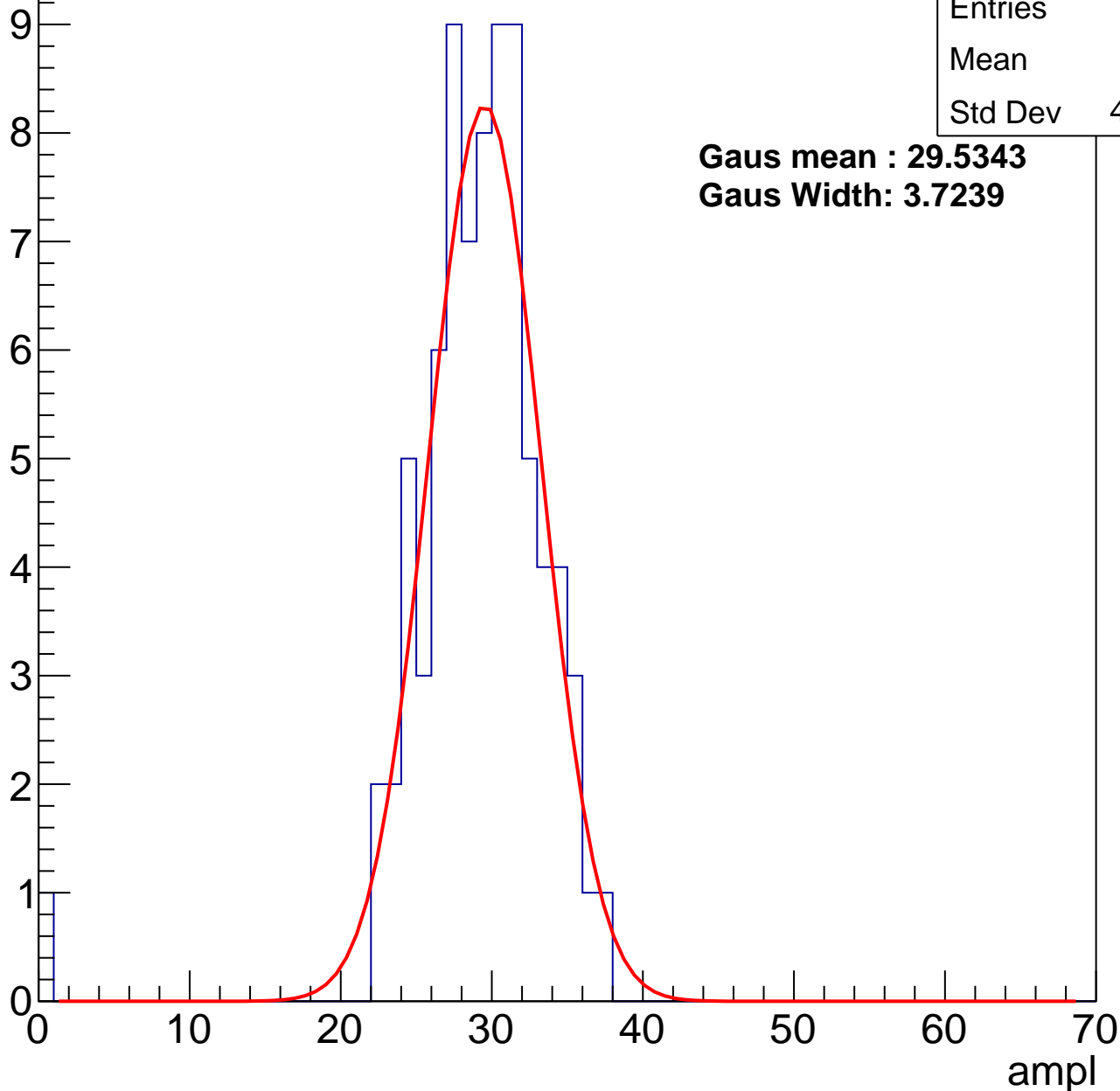
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	28.7
Std Dev	4.705

**Gaus mean : 29.5343**

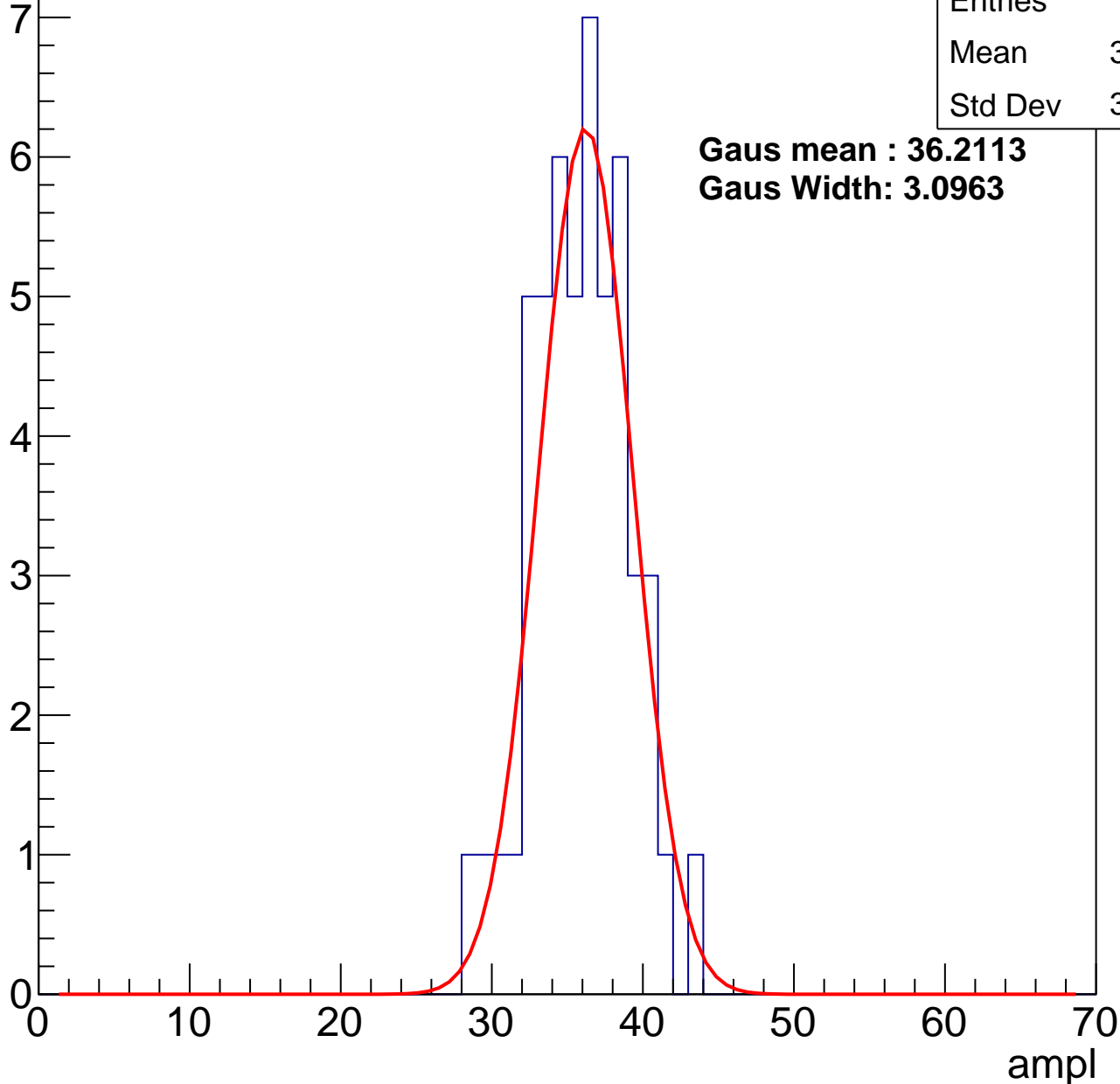
**Gaus Width: 3.7239**



# B1L101S, U9-ch18, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch18, adc2

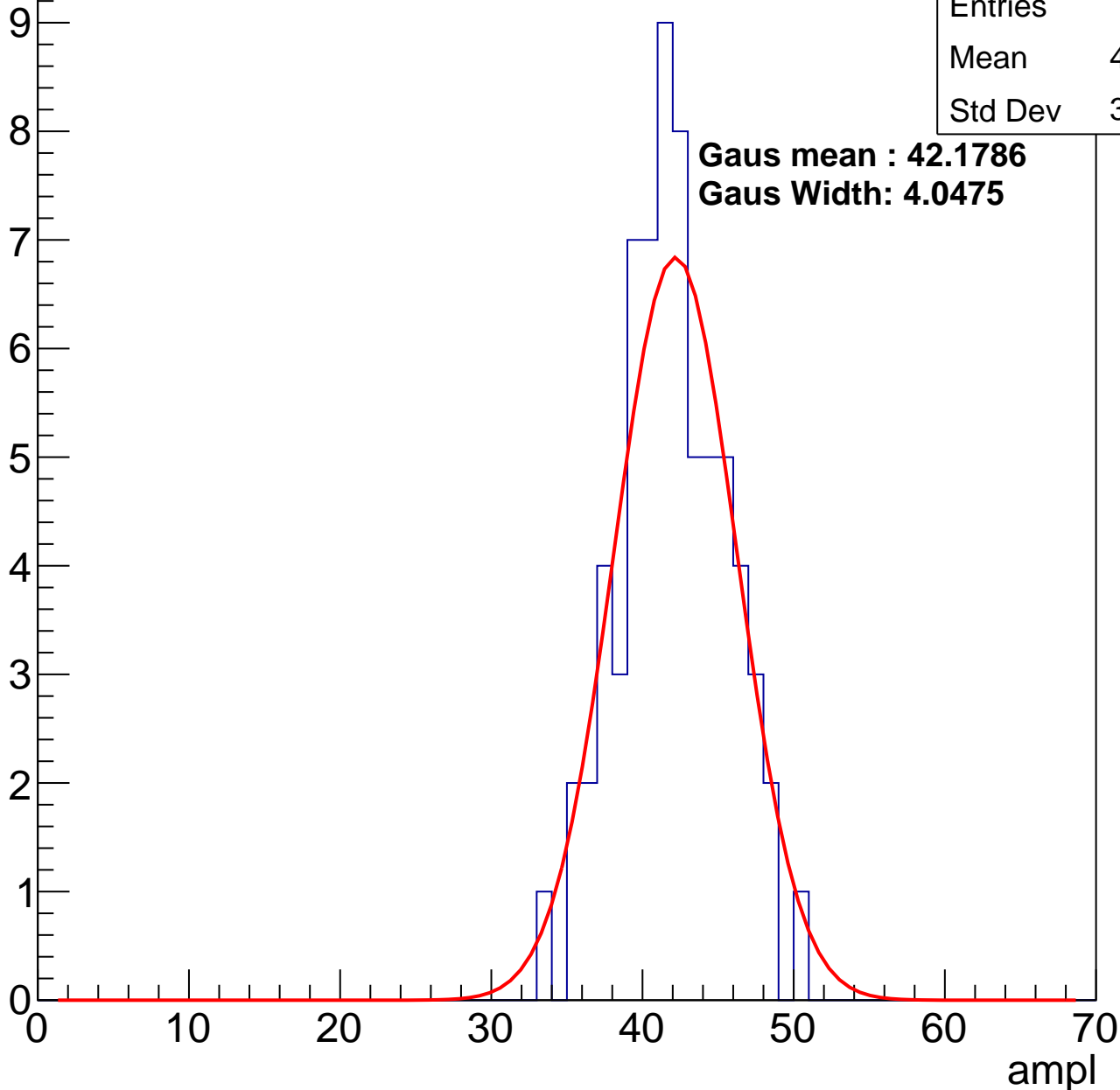
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	41.56
Std Dev	3.495

**Gaus mean : 42.1786**

**Gaus Width: 4.0475**

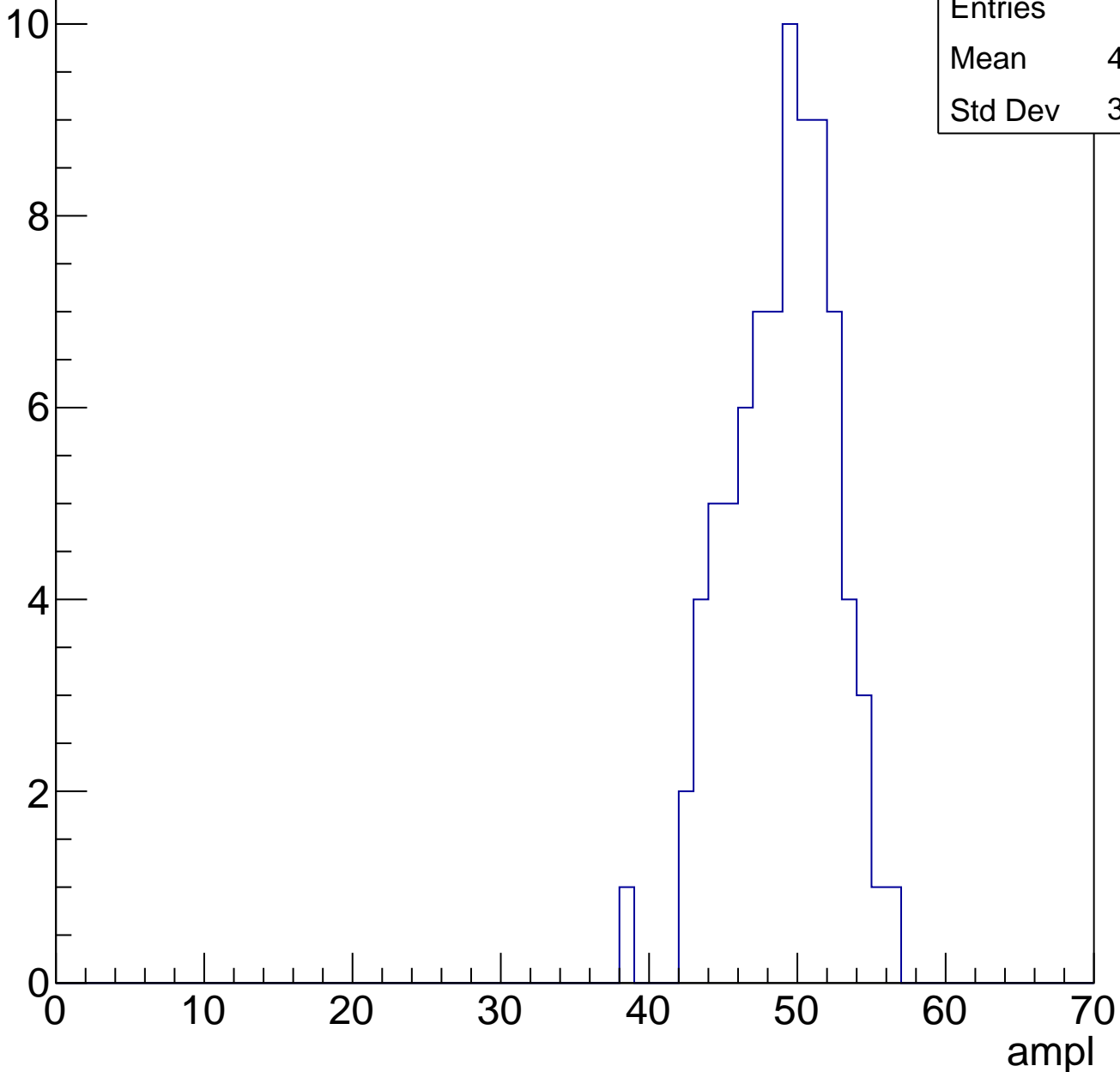


# B1L101S, U9-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	81
Mean	48.49
Std Dev	3.457

Entry

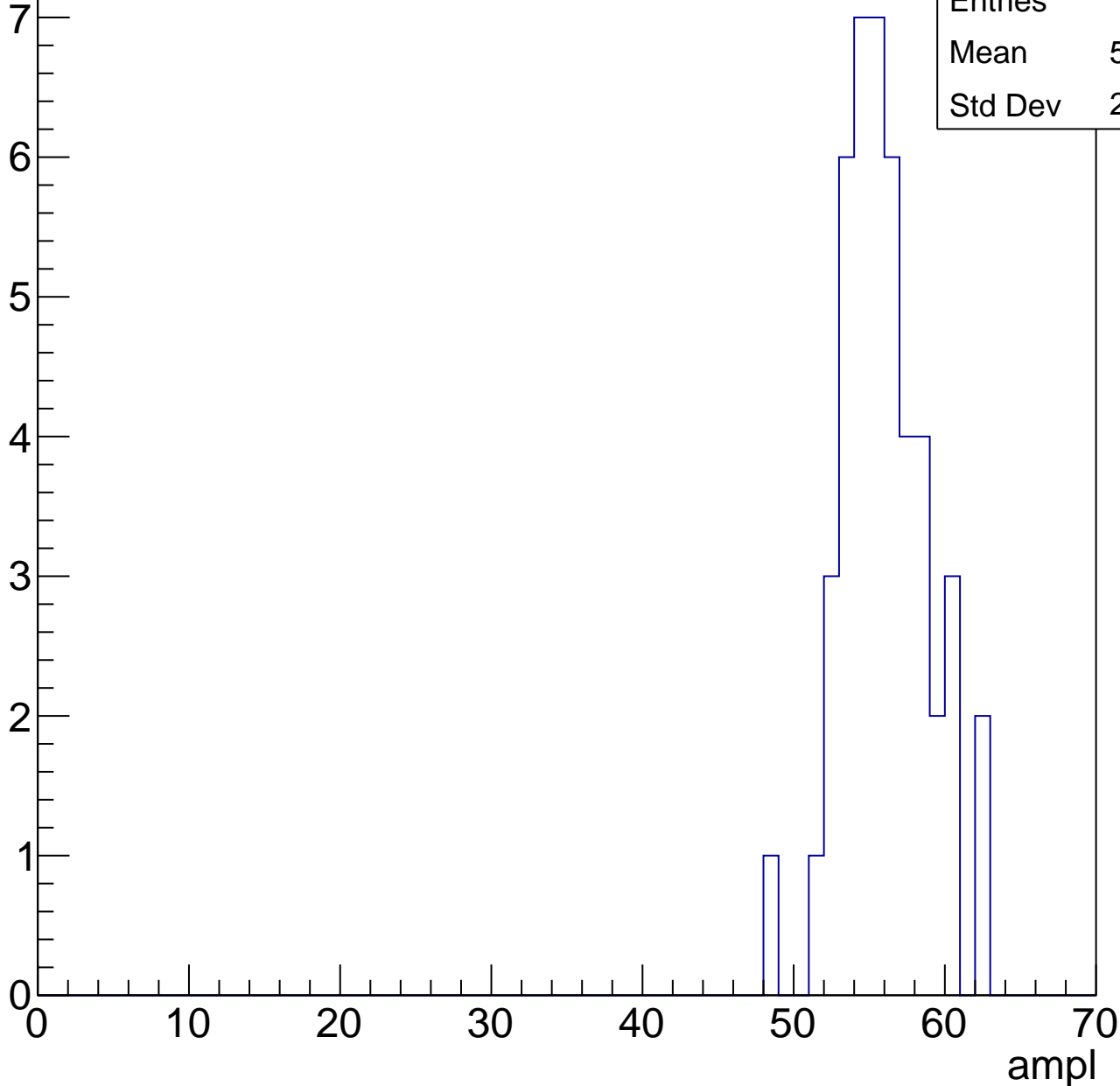


# B1L101S, U9-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	55.52
Std Dev	2.849



# B1L101S, U9-ch18, adc5

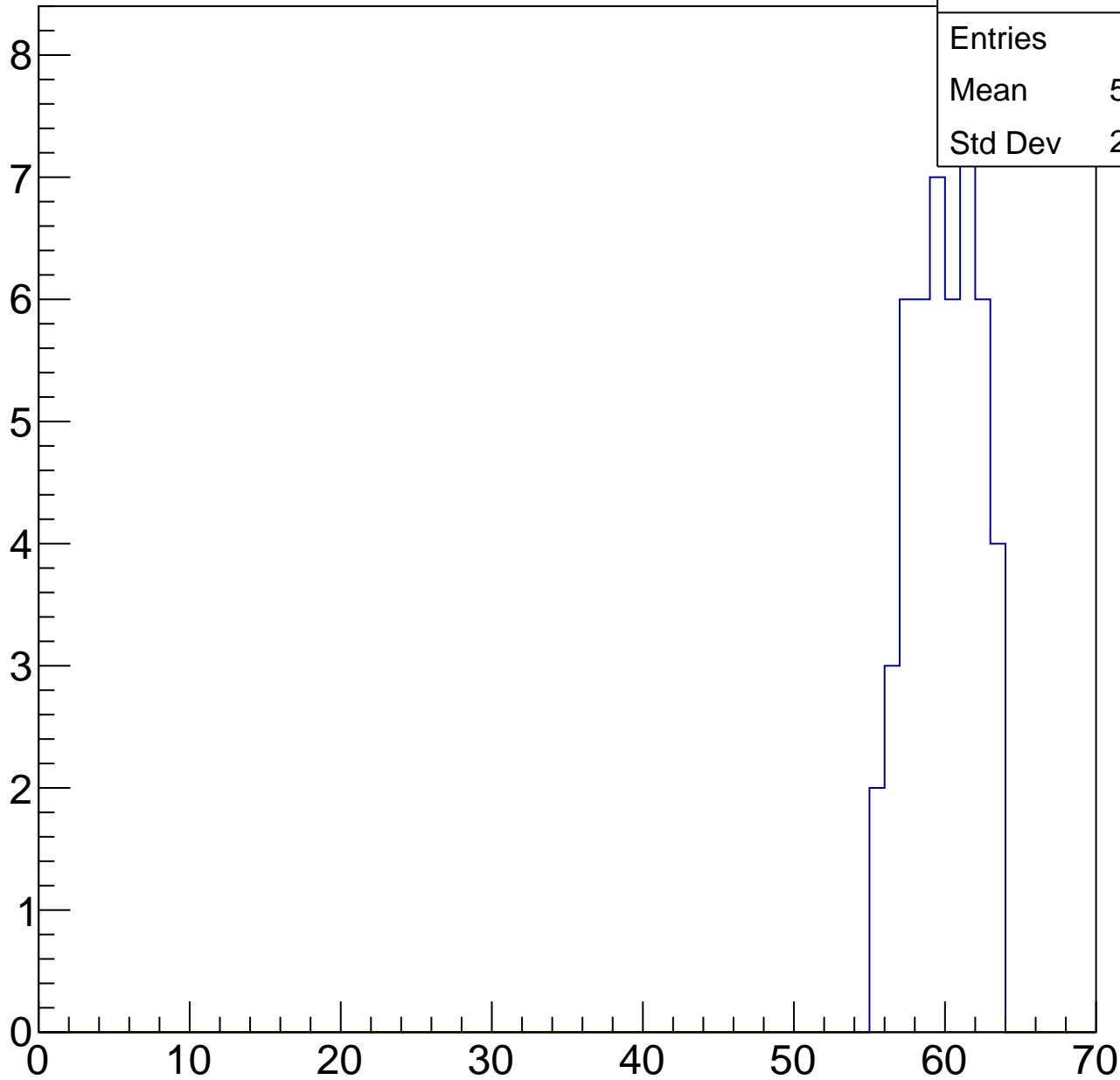
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	59.44
Std Dev	2.216

ampl

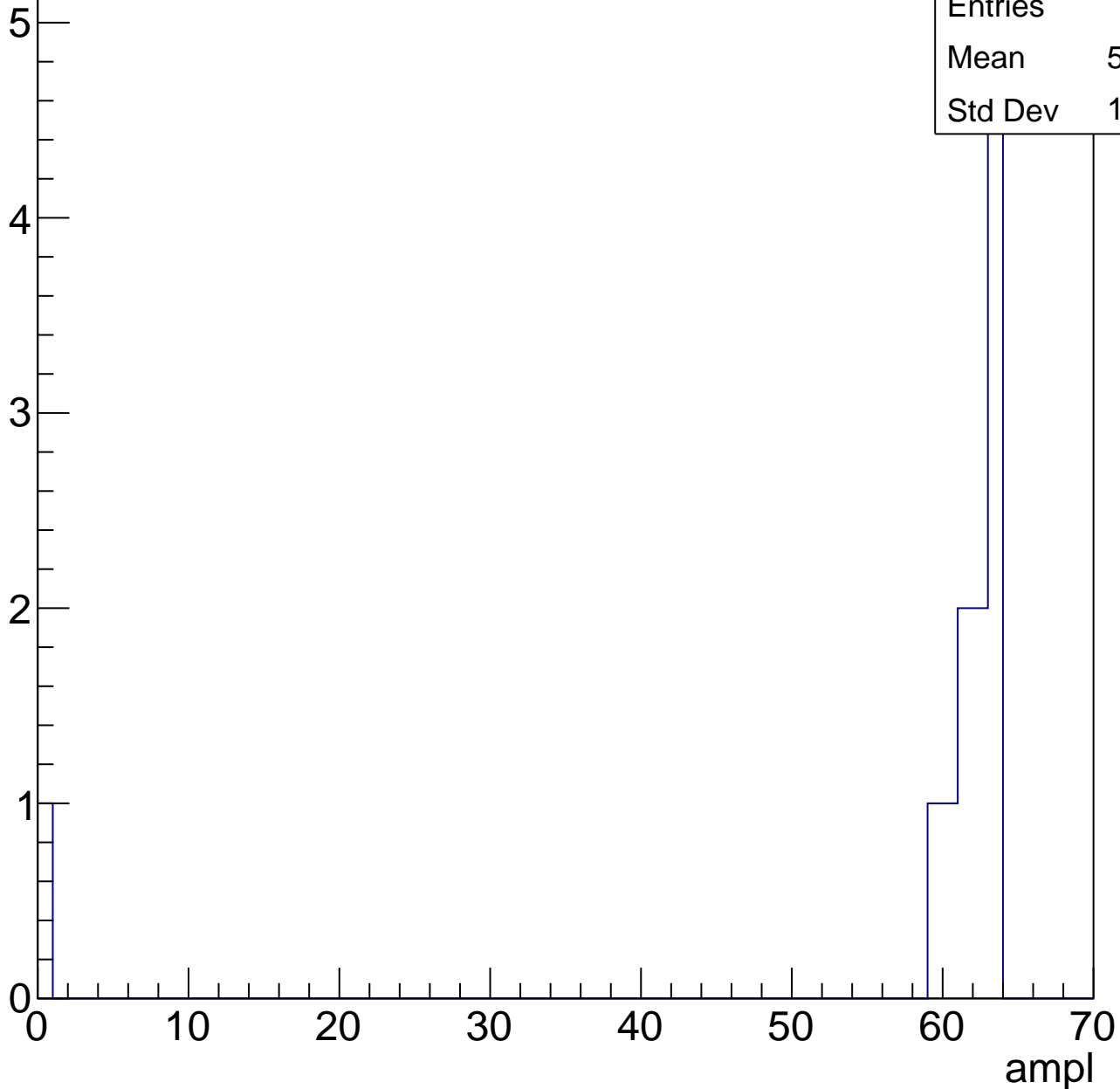


# B1L101S, U9-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	12
Mean	56.67
Std Dev	17.13

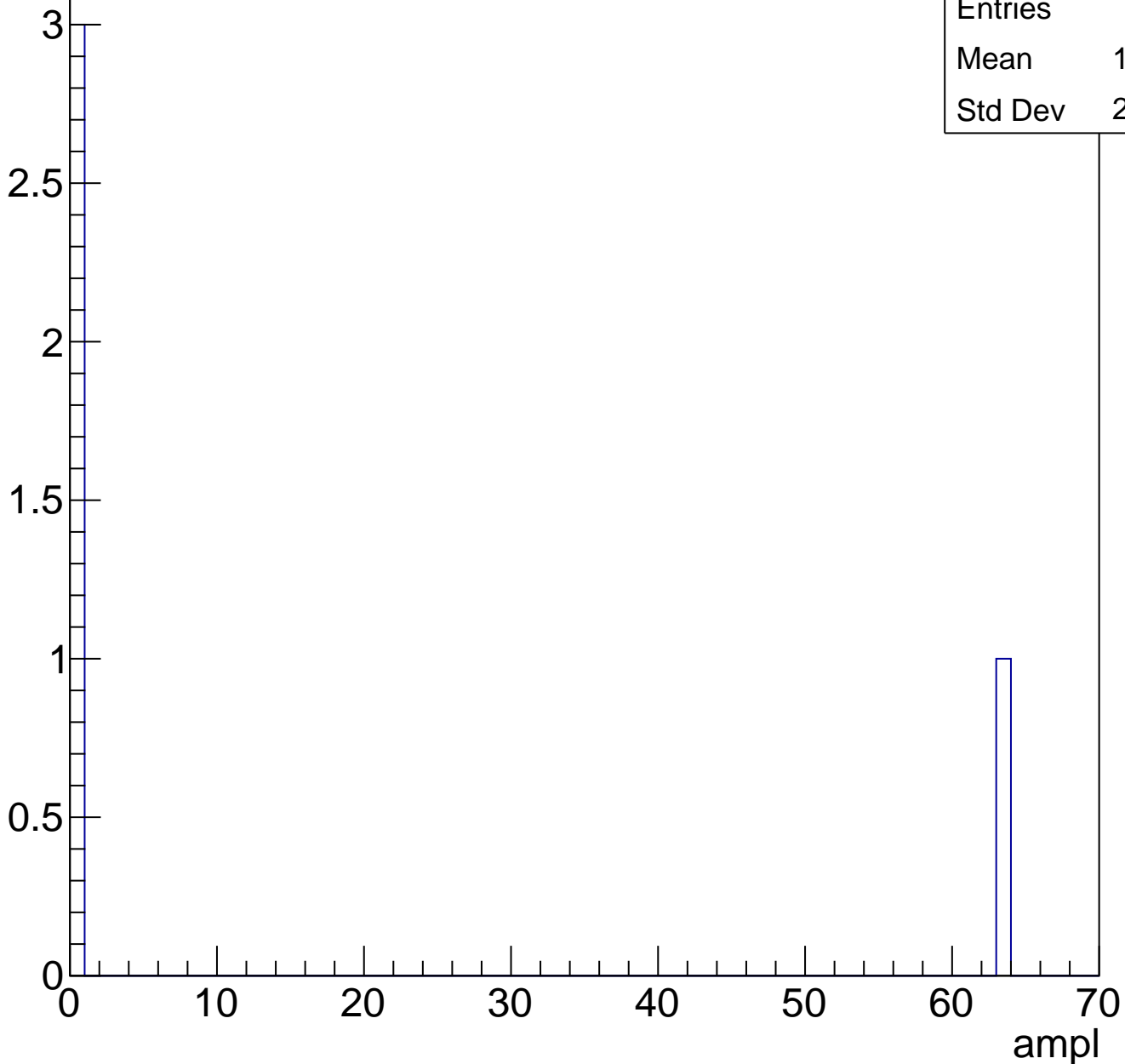




# B1L101S, U9-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch19, adc0

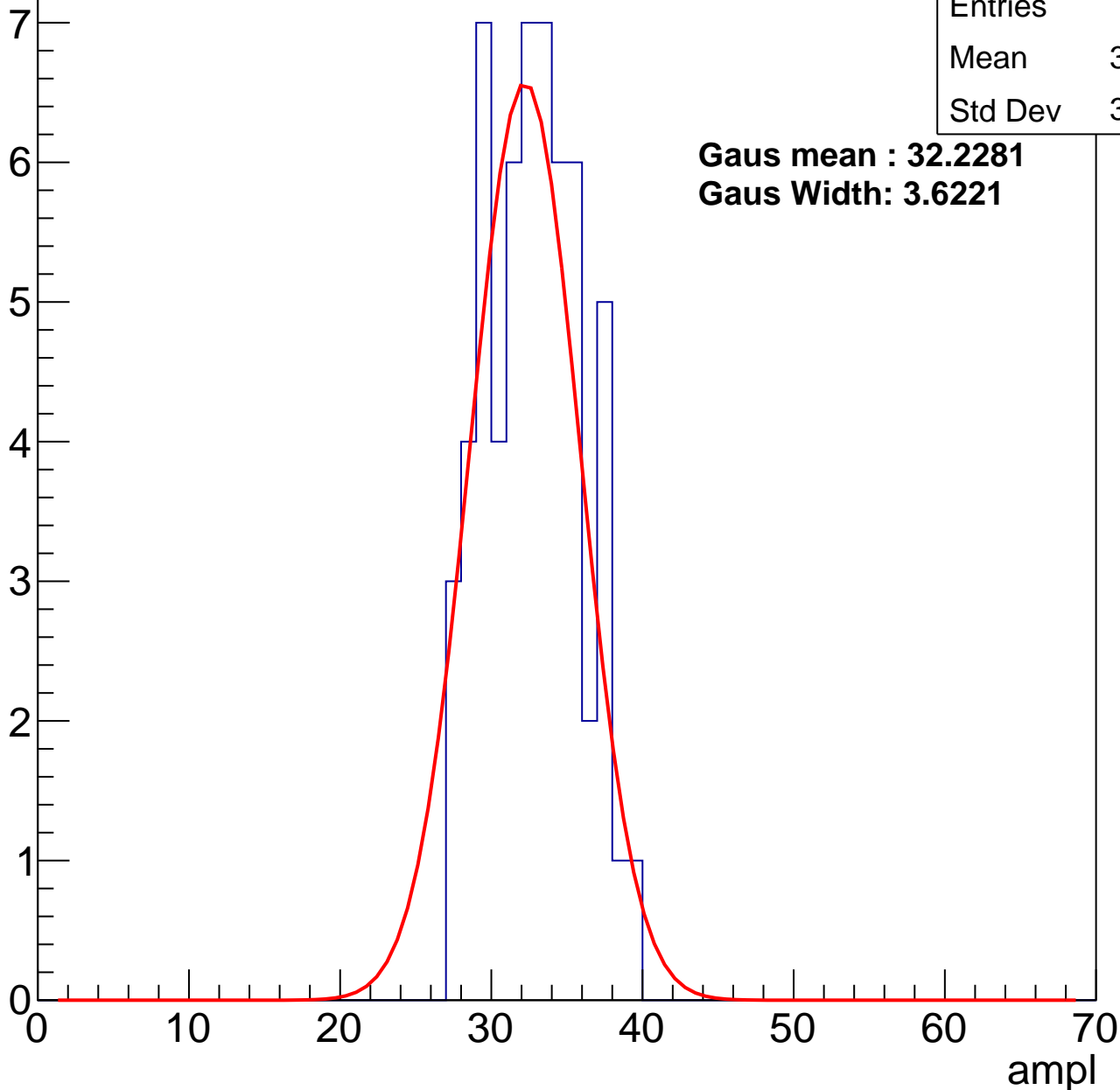
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	32.29
Std Dev	3.042

**Gaus mean : 32.2281**

**Gaus Width: 3.6221**



# B1L101S, U9-ch19, adc1

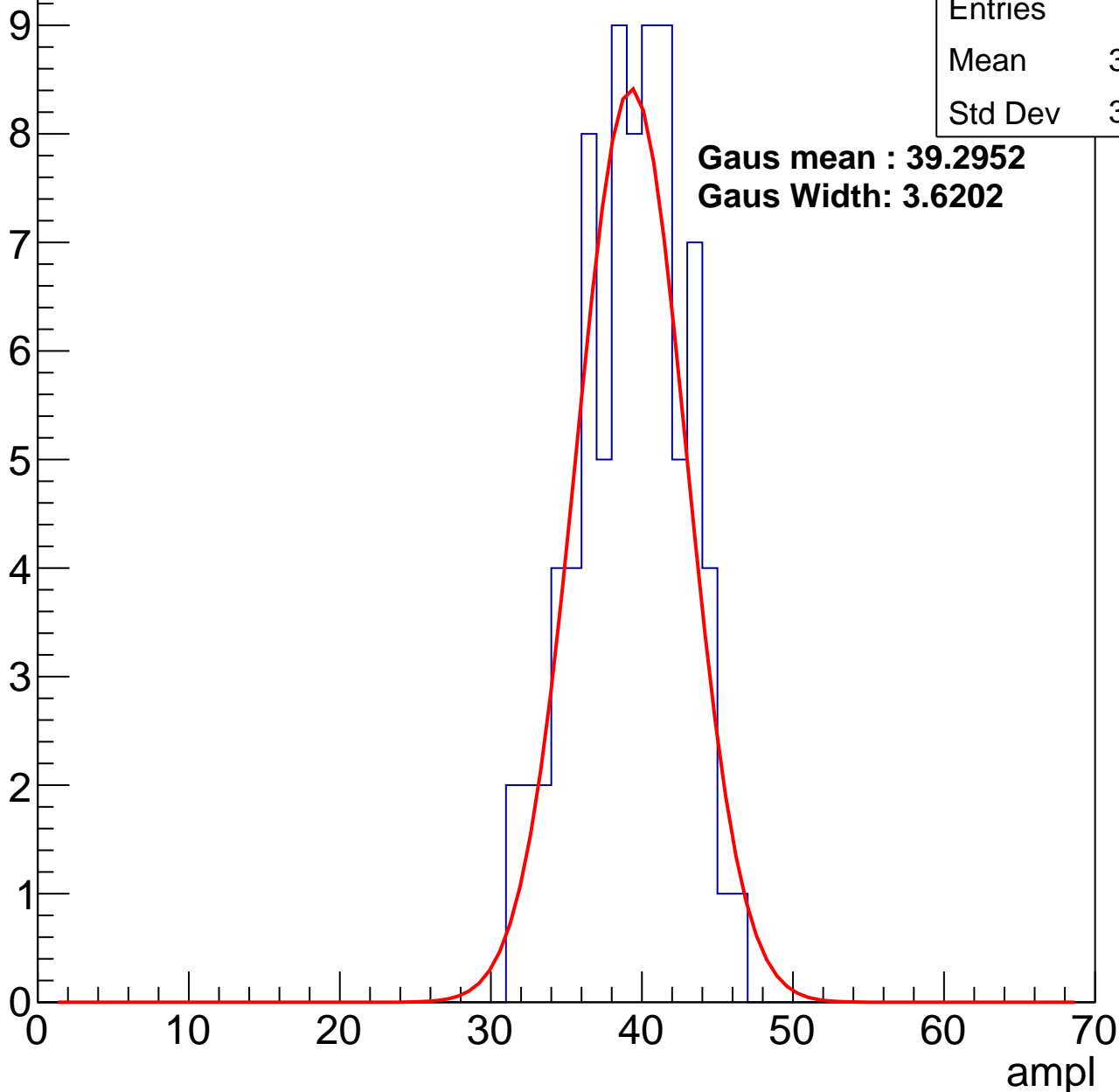
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	38.77
Std Dev	3.439

**Gaus mean : 39.2952**

**Gaus Width: 3.6202**



# B1L101S, U9-ch19, adc2

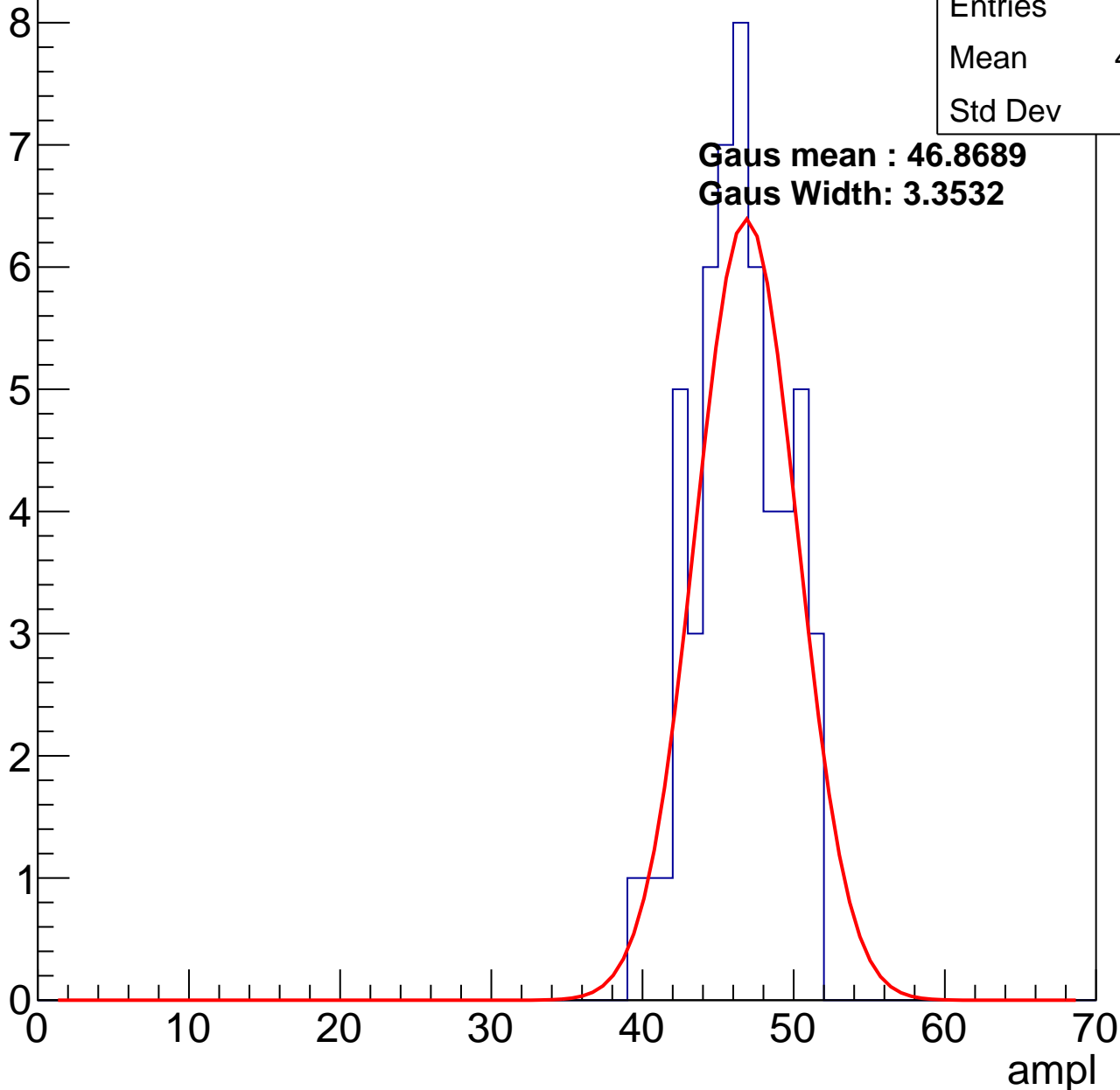
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	45.91
Std Dev	2.92

**Gaus mean : 46.8689**

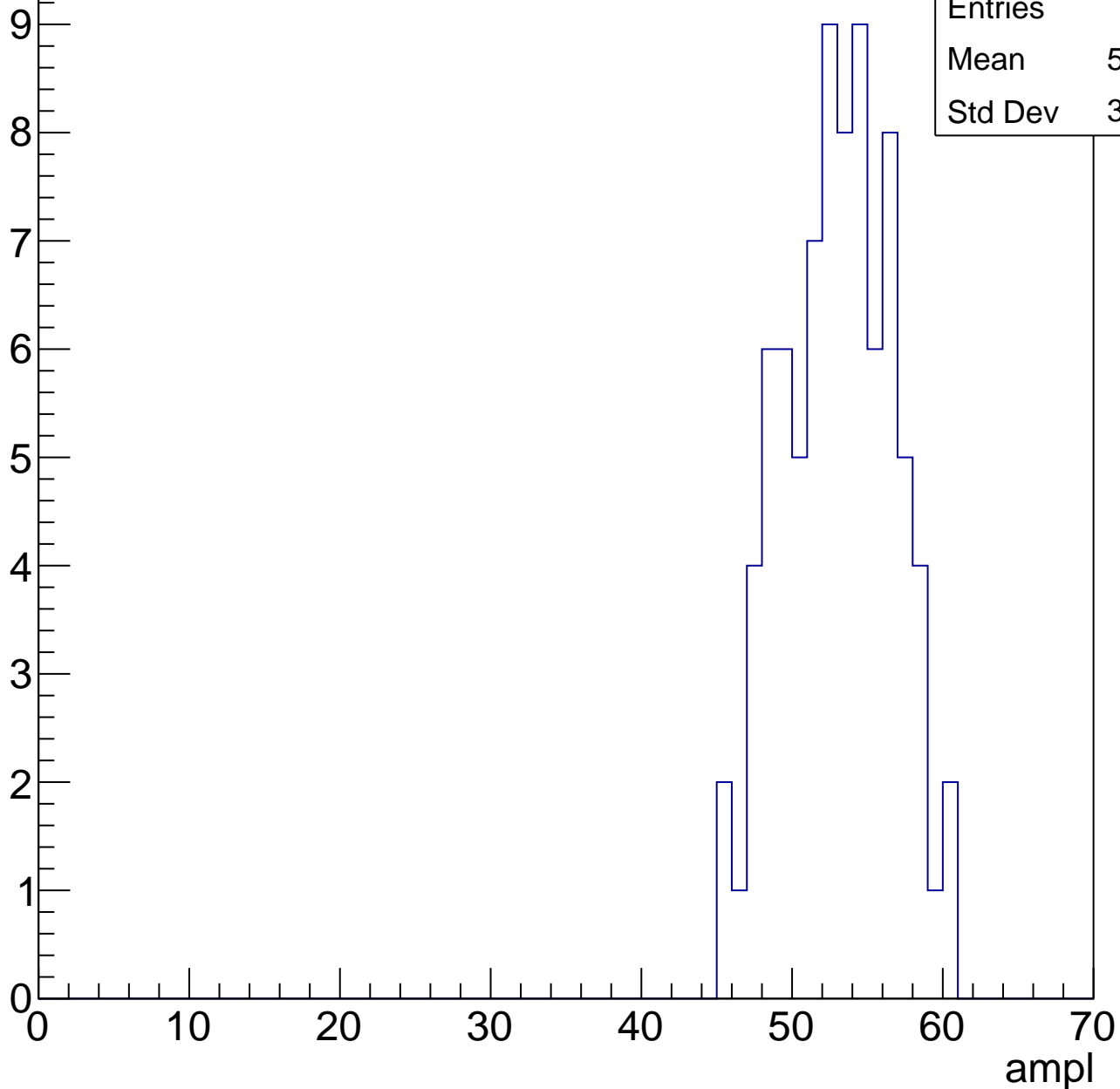
**Gaus Width: 3.3532**



# B1L101S, U9-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



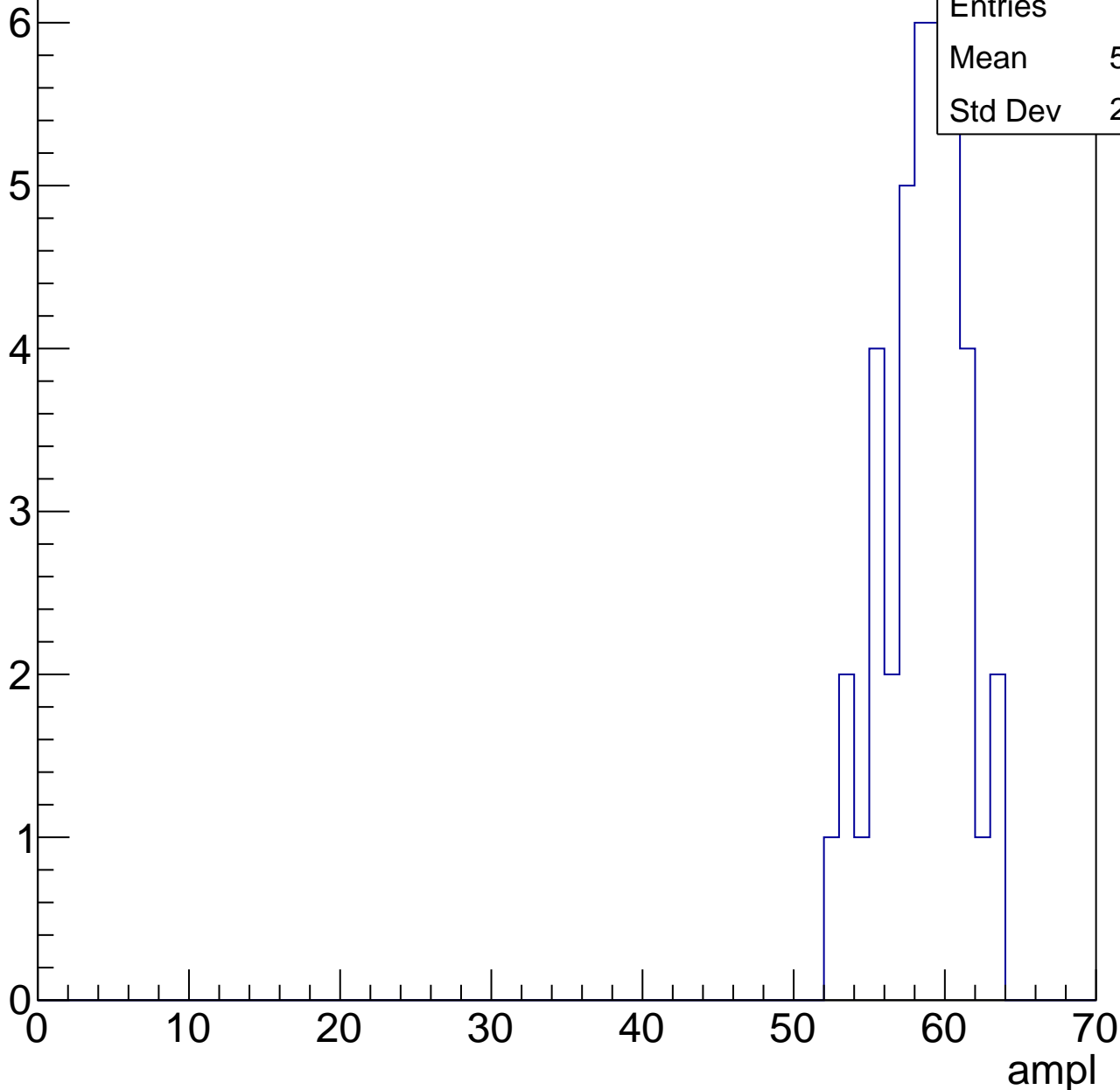
Entries	83
Mean	52.59
Std Dev	3.564

# B1L101S, U9-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	40
Mean	58.08
Std Dev	2.659

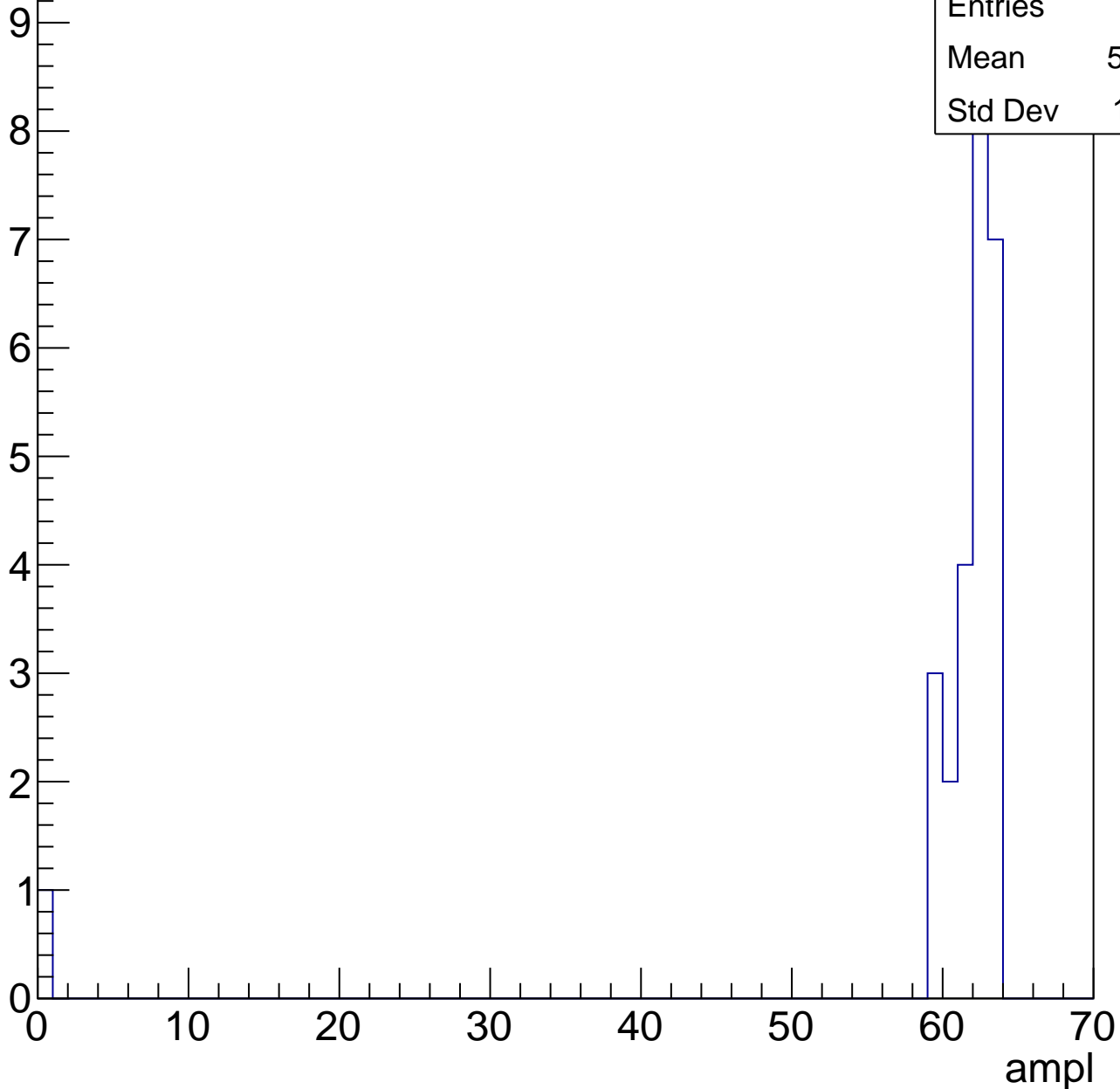


# B1L101S, U9-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	26
Mean	59.23
Std Dev	11.91



# B1L101S, U9-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U9-ch20, adc0

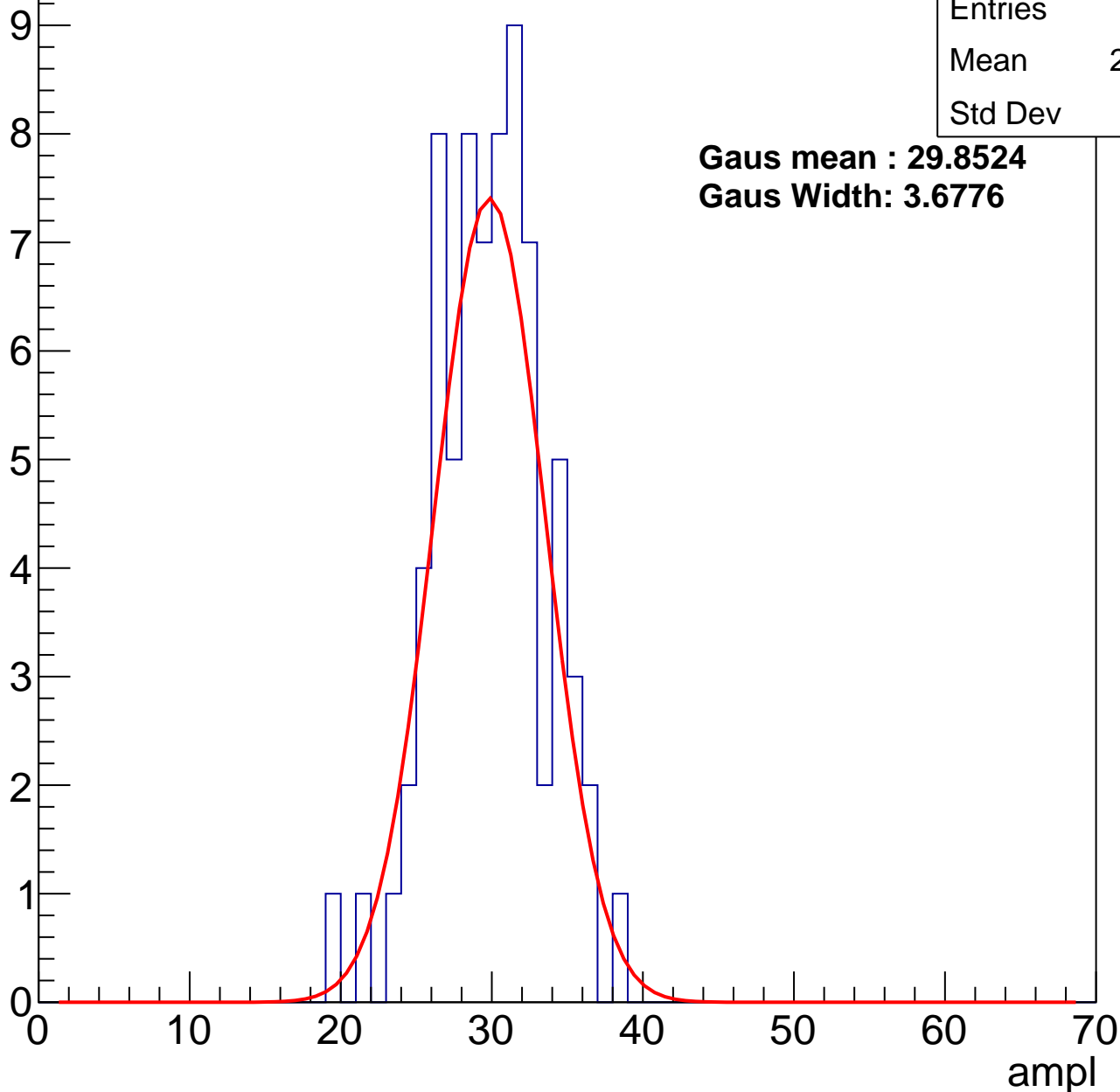
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	29.39
Std Dev	3.59

**Gaus mean : 29.8524**

**Gaus Width: 3.6776**



# B1L101S, U9-ch20, adc1

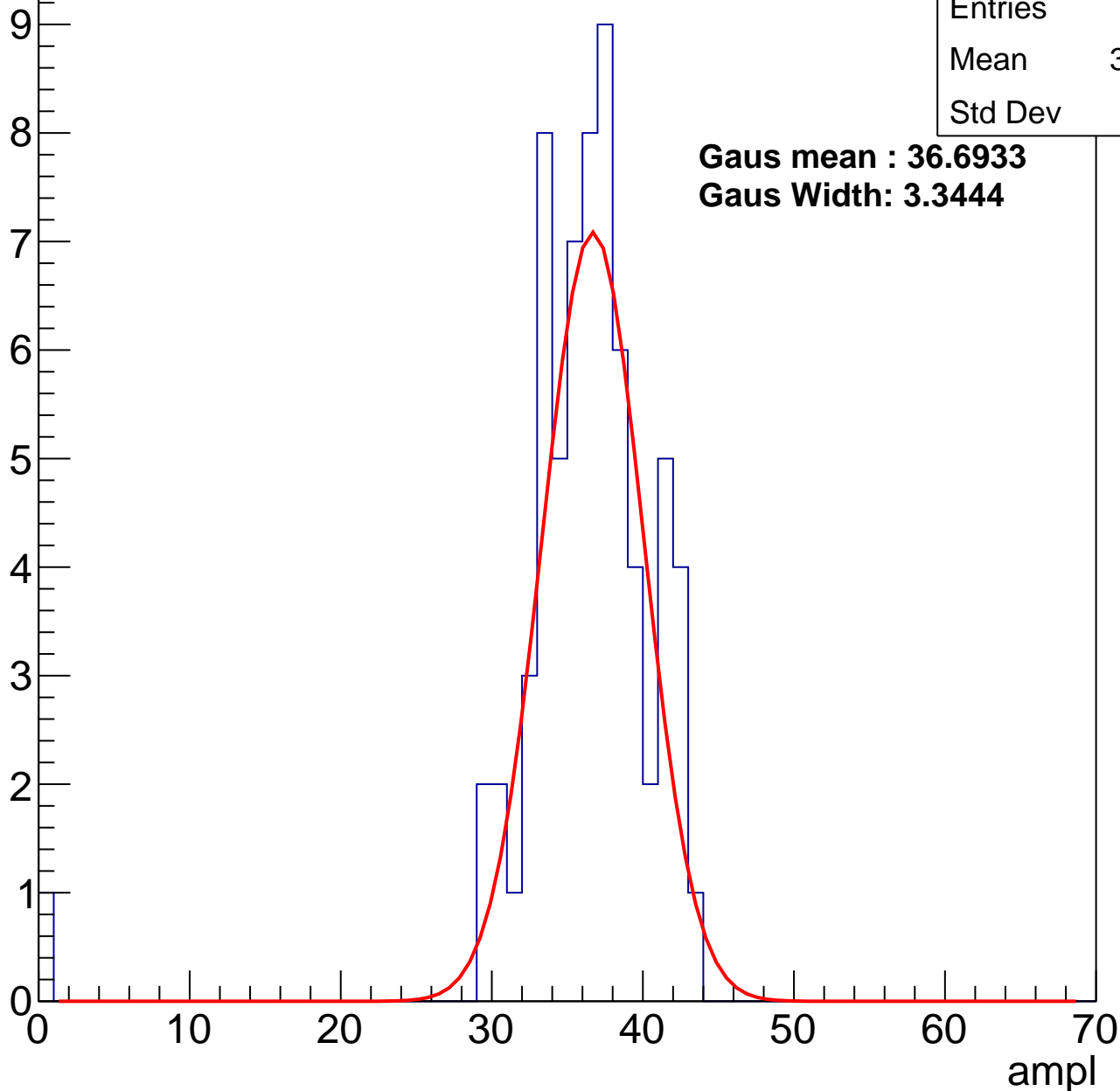
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	35.66
Std Dev	5.49

**Gaus mean : 36.6933**

**Gaus Width: 3.3444**



# B1L101S, U9-ch20, adc2

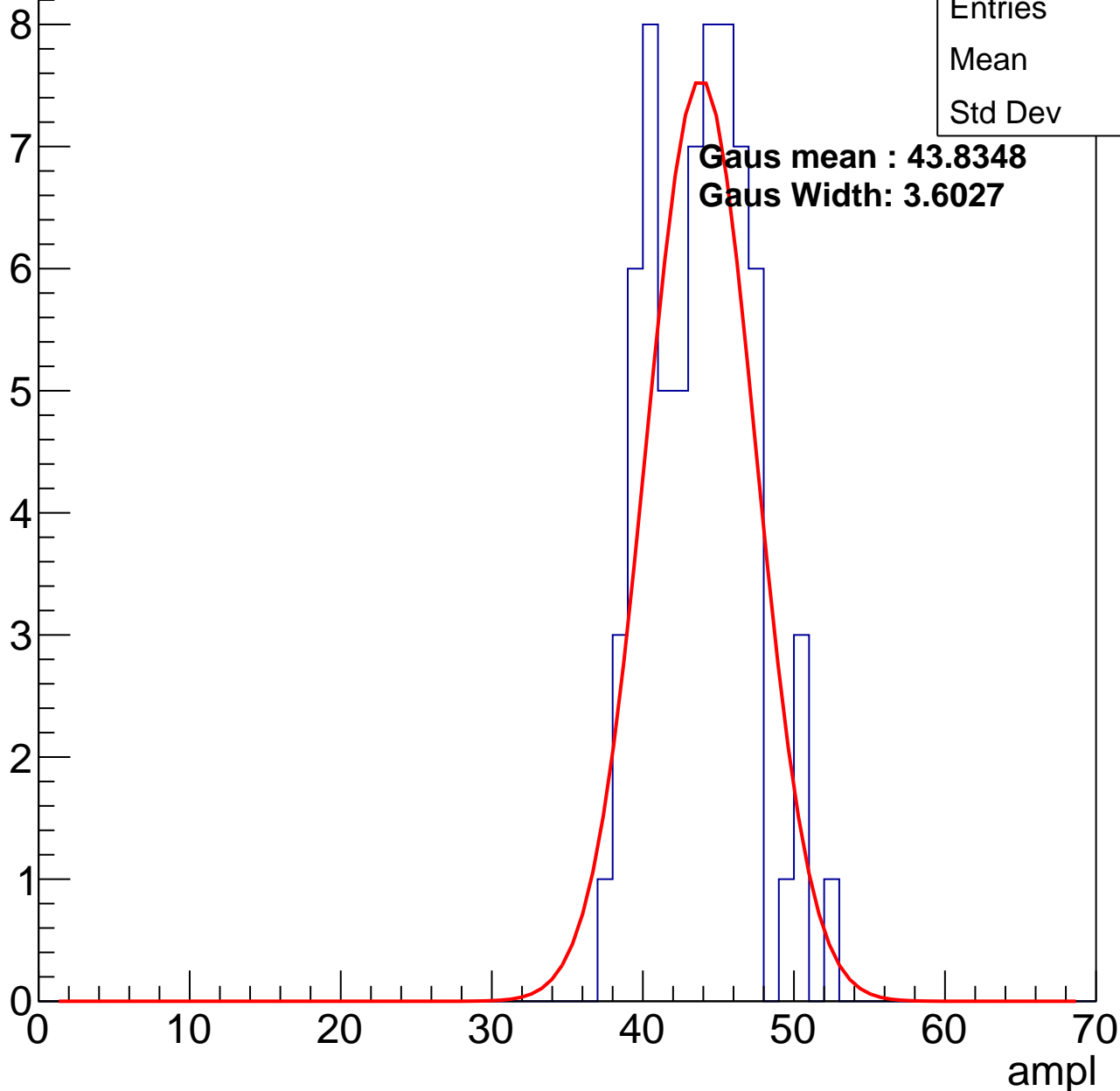
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	43.3
Std Dev	3.32

**Gaus mean : 43.8348**

**Gaus Width: 3.6027**

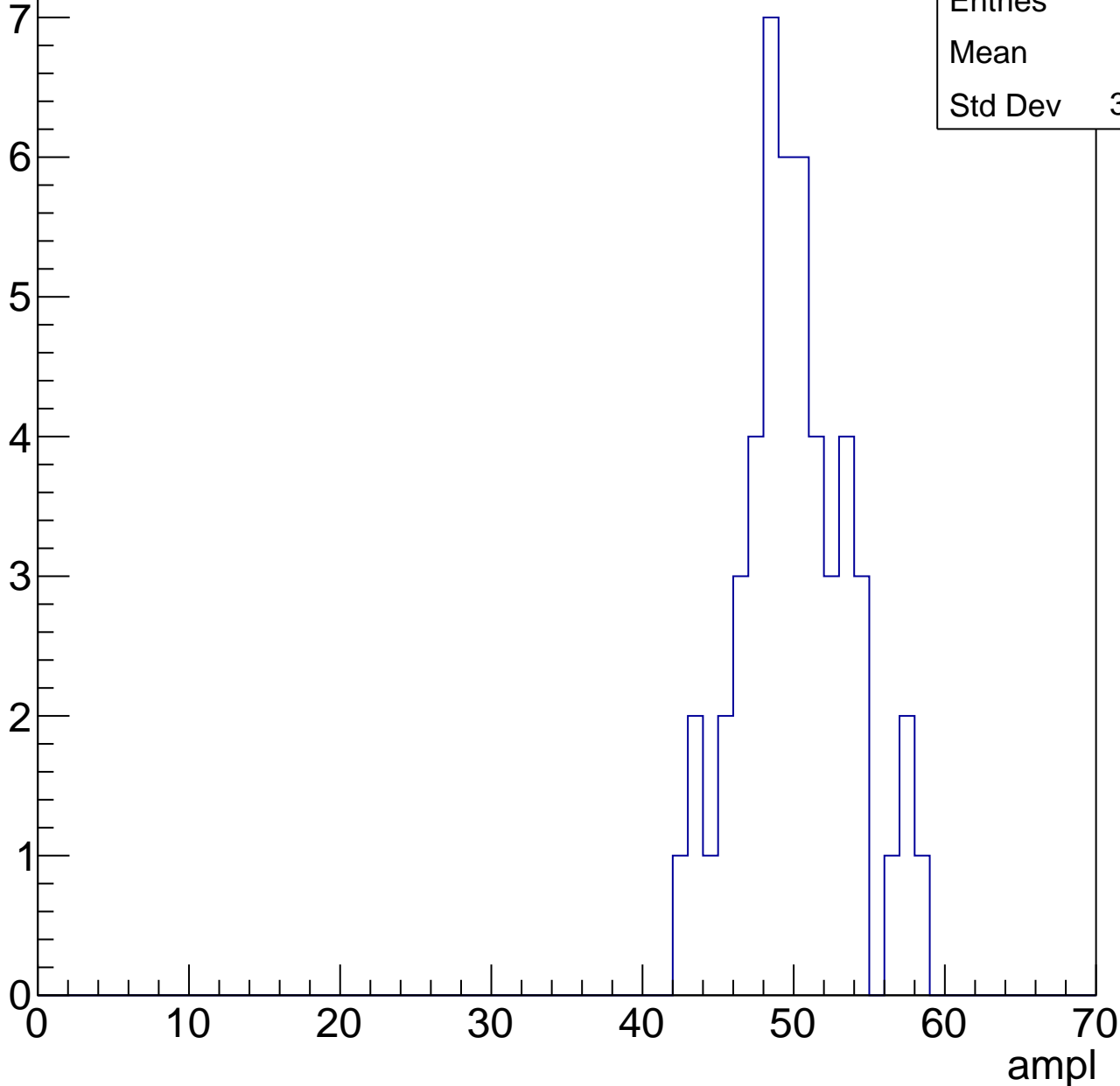


# B1L101S, U9-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

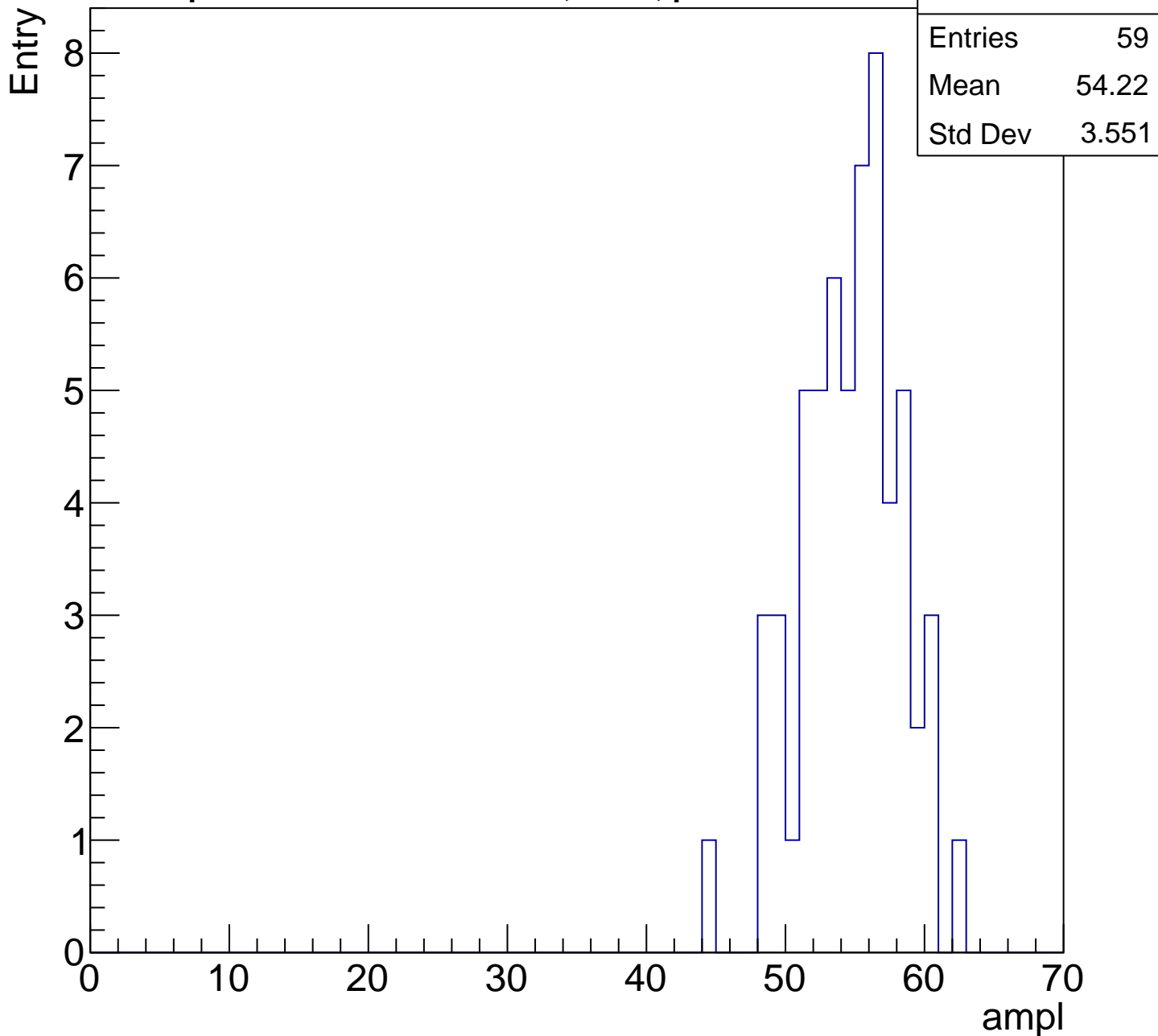
Entry

Entries	50
Mean	49.6
Std Dev	3.622



# B1L101S, U9-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

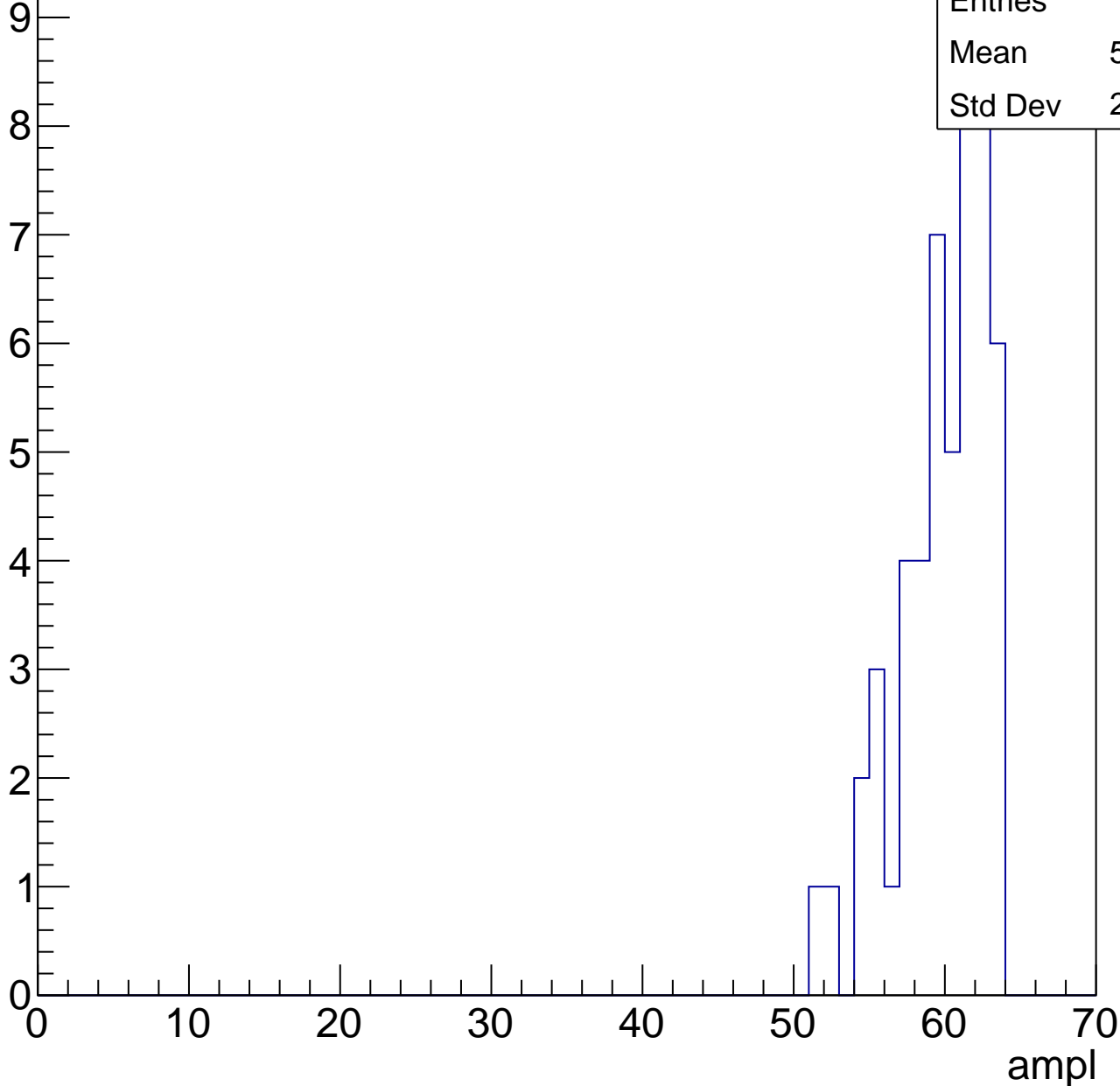


# B1L101S, U9-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

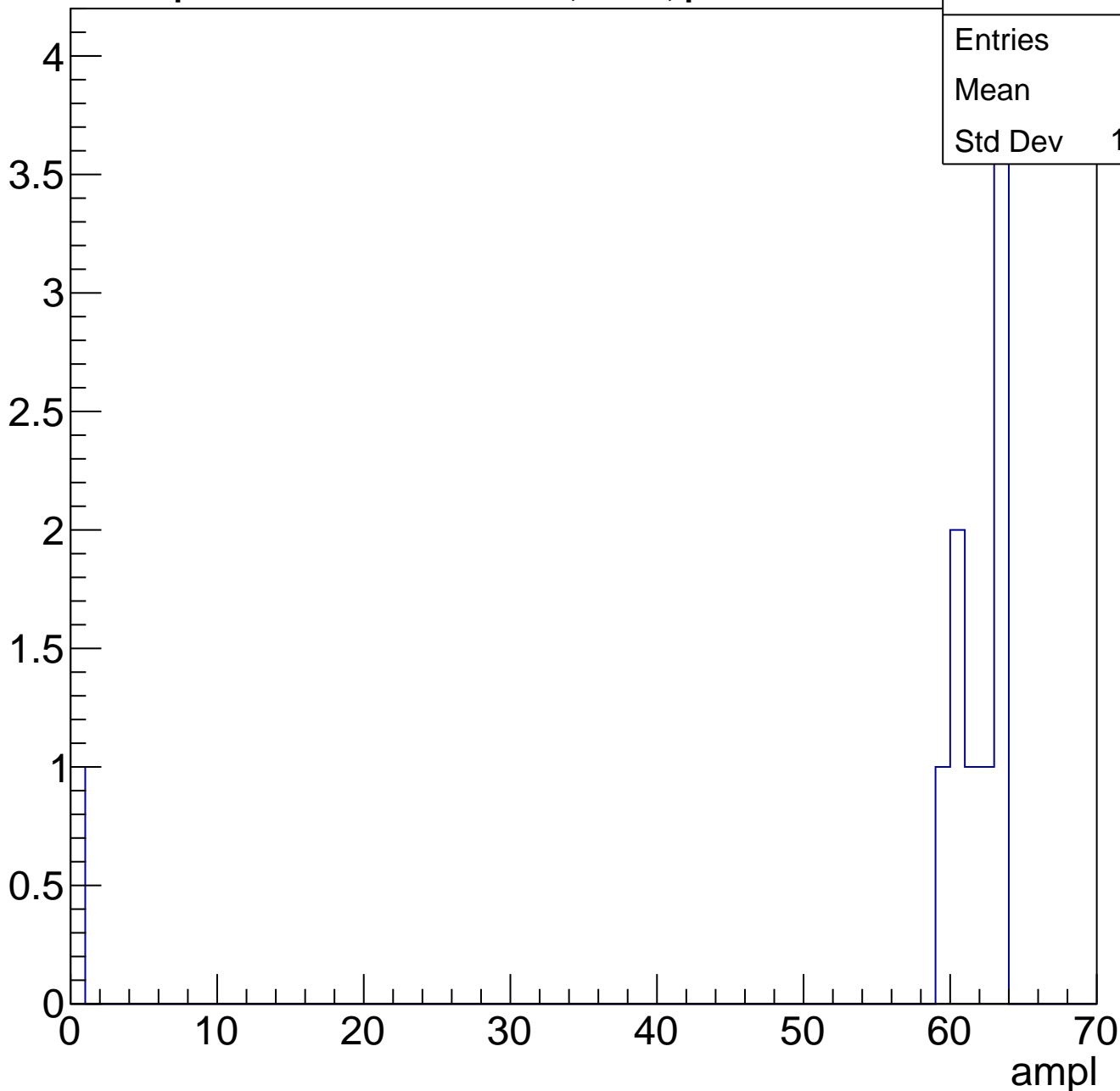
Entries	51
Mean	59.37
Std Dev	2.944



# B1L101S, U9-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U9-ch21, adc0

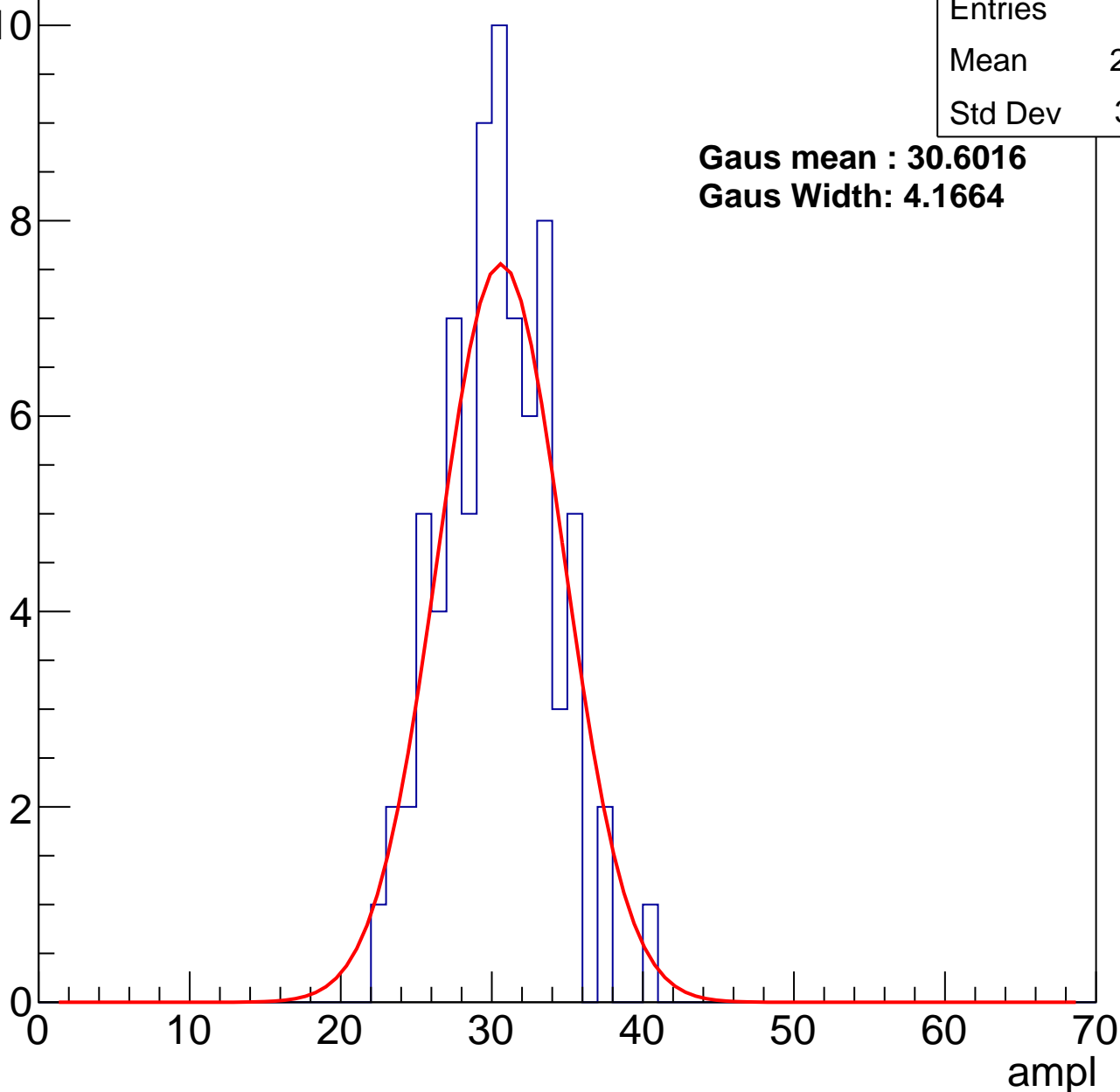
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	29.86
Std Dev	3.581

**Gaus mean : 30.6016**

**Gaus Width: 4.1664**



# B1L101S, U9-ch21, adc1

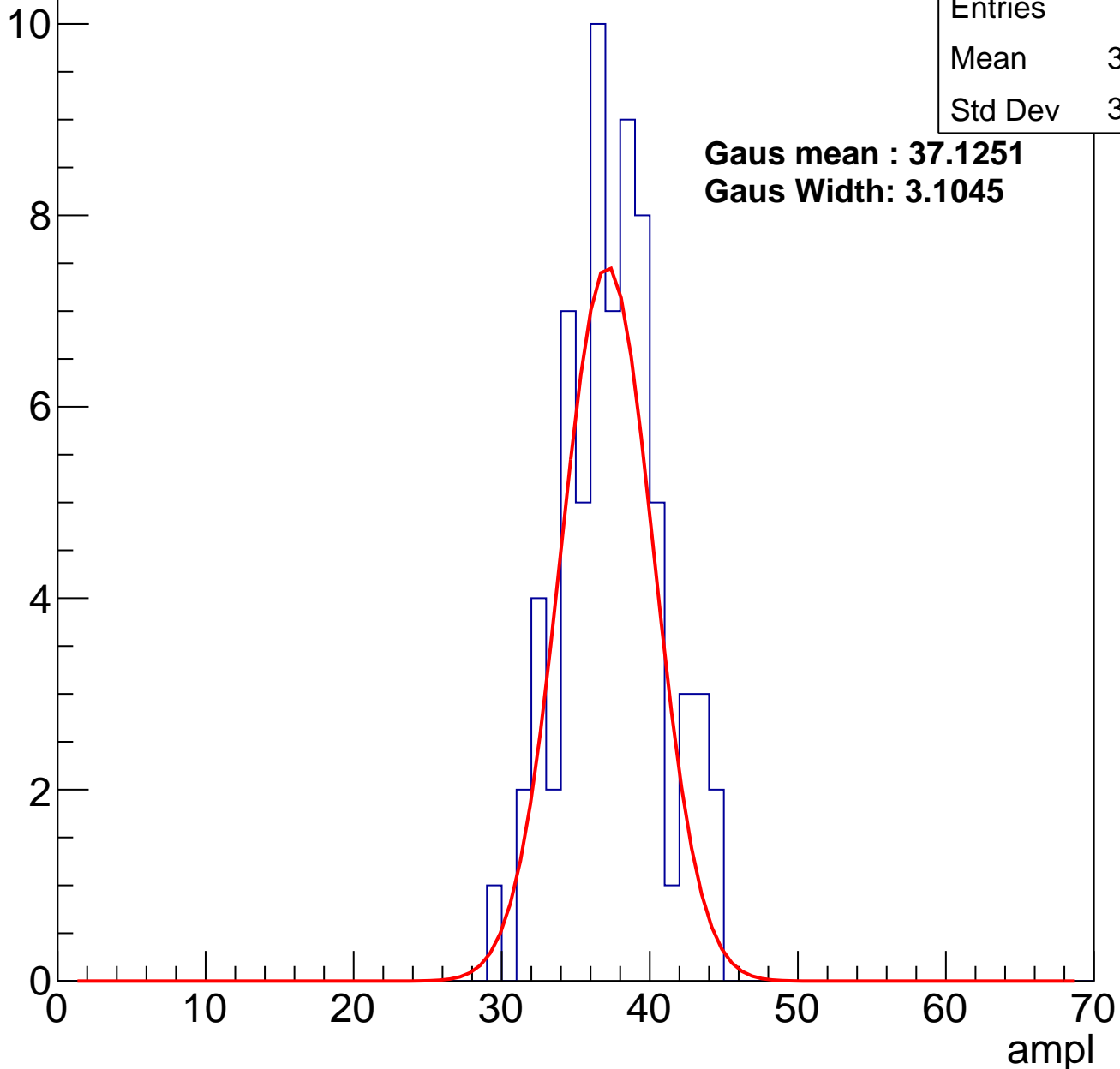
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	69
Mean	37.03
Std Dev	3.284

**Gaus mean : 37.1251**

**Gaus Width: 3.1045**

Entry



# B1L101S, U9-ch21, adc2

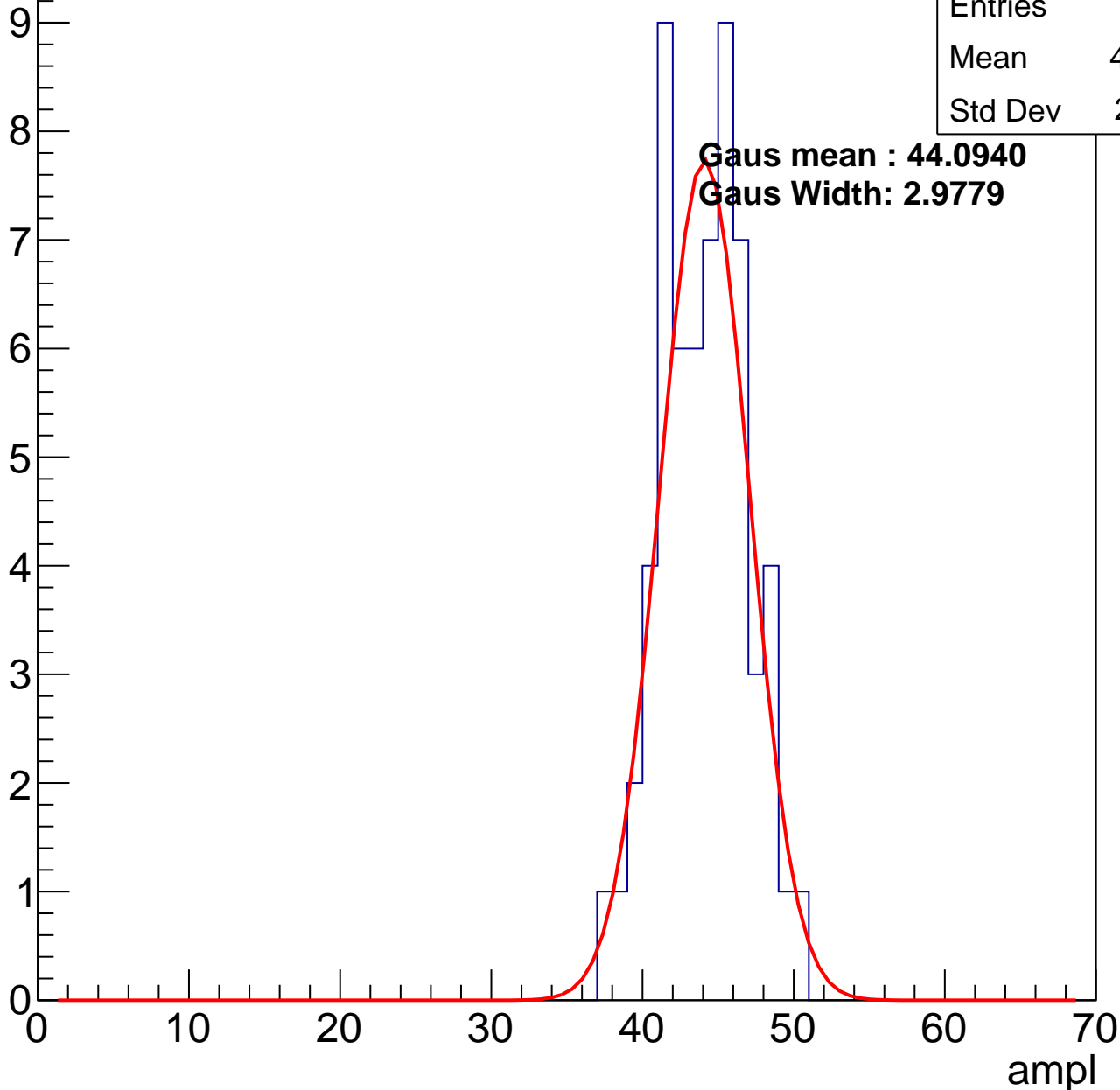
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	43.59
Std Dev	2.831

**Gaus mean : 44.0940**

**Gaus Width: 2.9779**

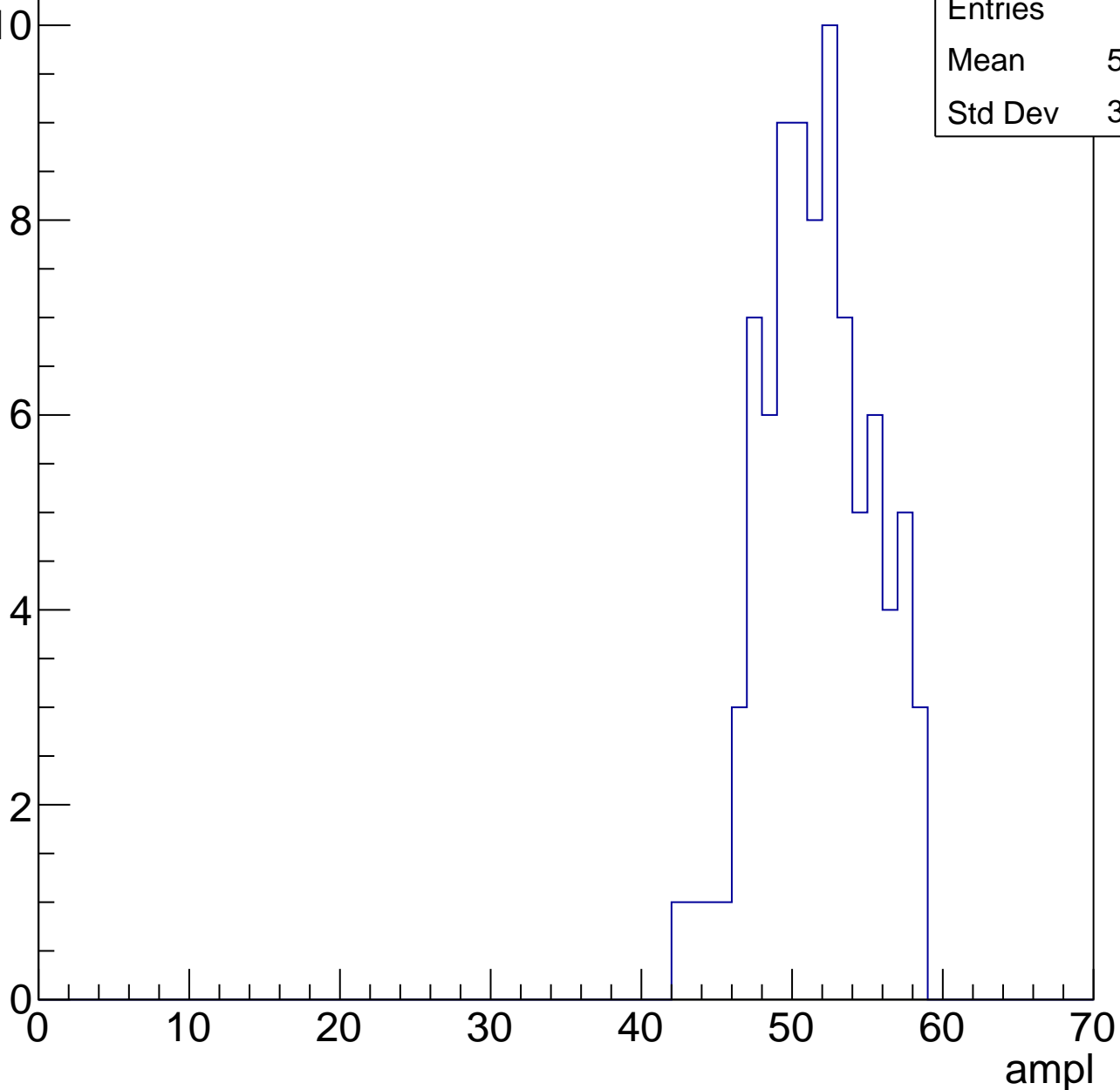


# B1L101S, U9-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

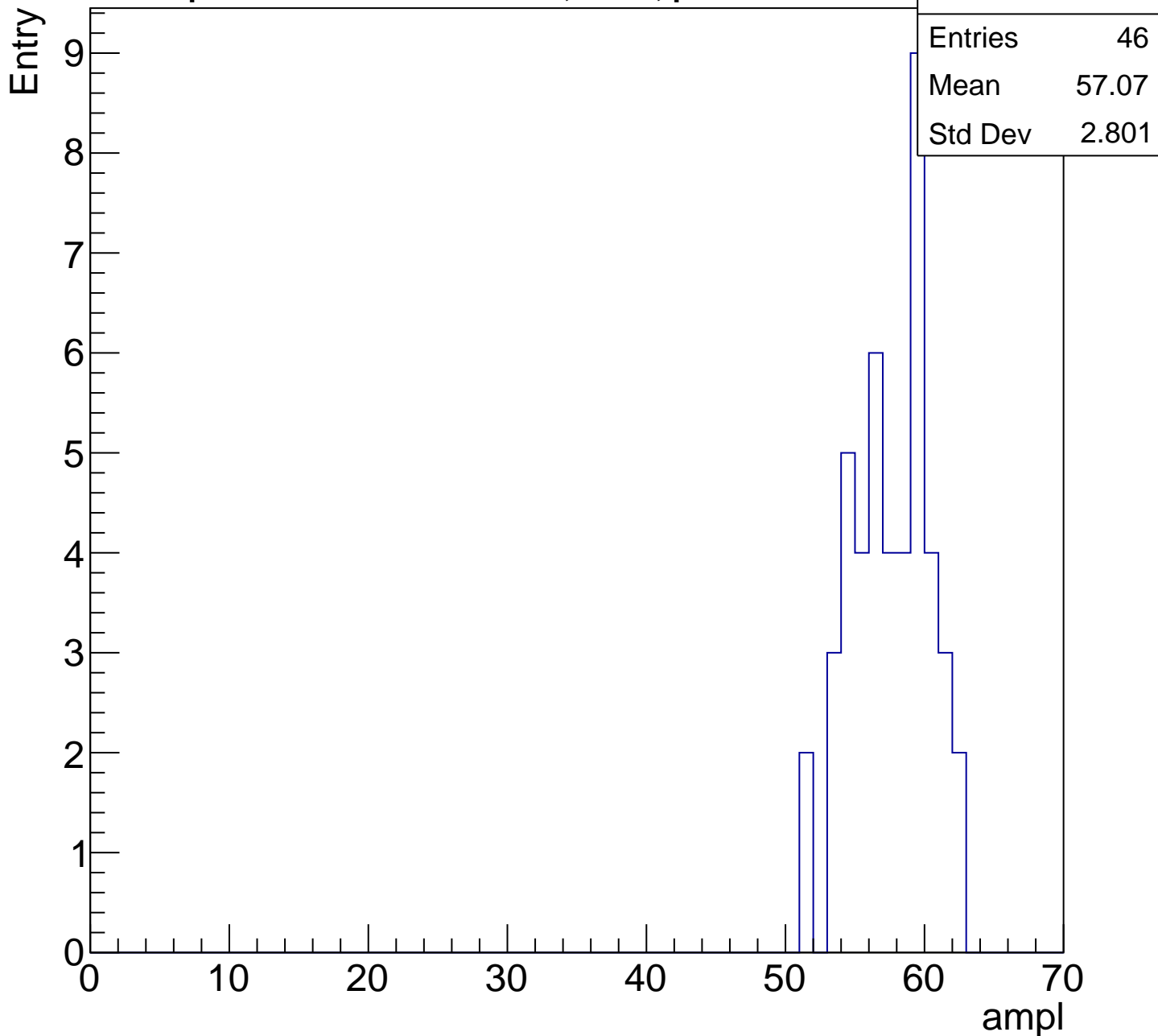
Entry

Entries	86
Mean	51.19
Std Dev	3.607



# B1L101S, U9-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

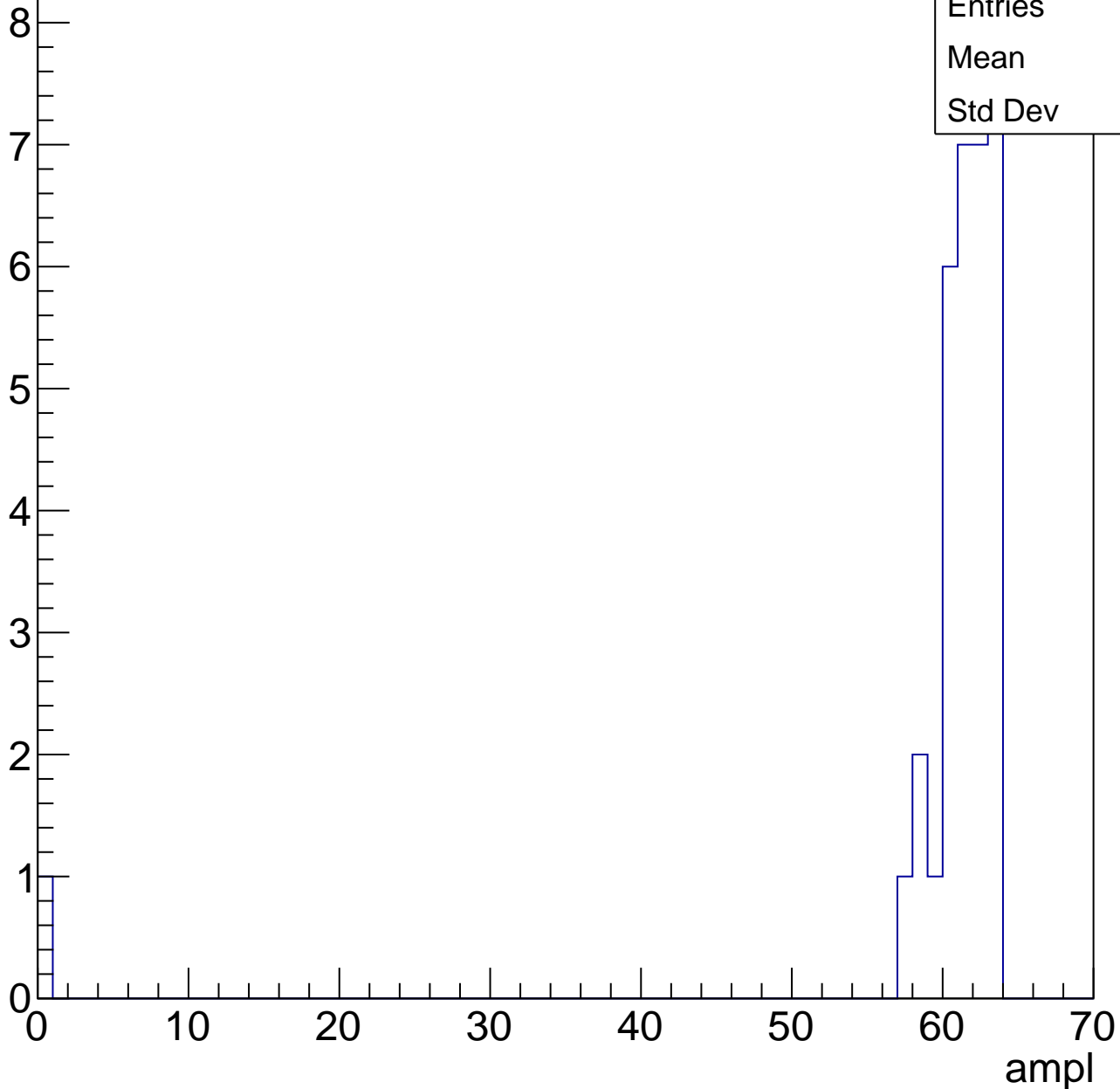


# B1L101S, U9-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	33
Mean	59.3
Std Dev	10.6



# B1L101S, U9-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U9-ch22, adc0

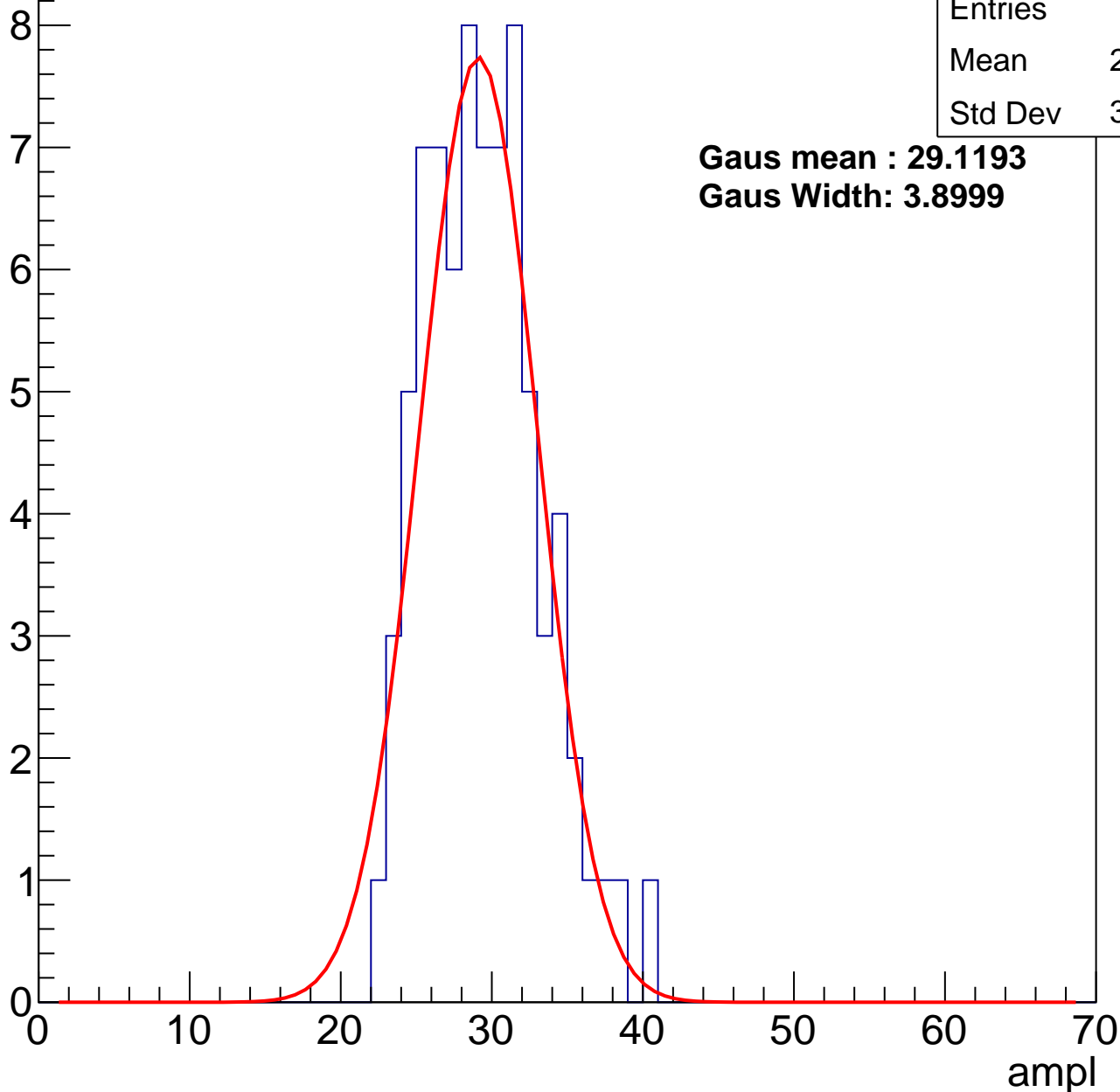
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	28.97
Std Dev	3.793

**Gaus mean : 29.1193**

**Gaus Width: 3.8999**



# B1L101S, U9-ch22, adc1

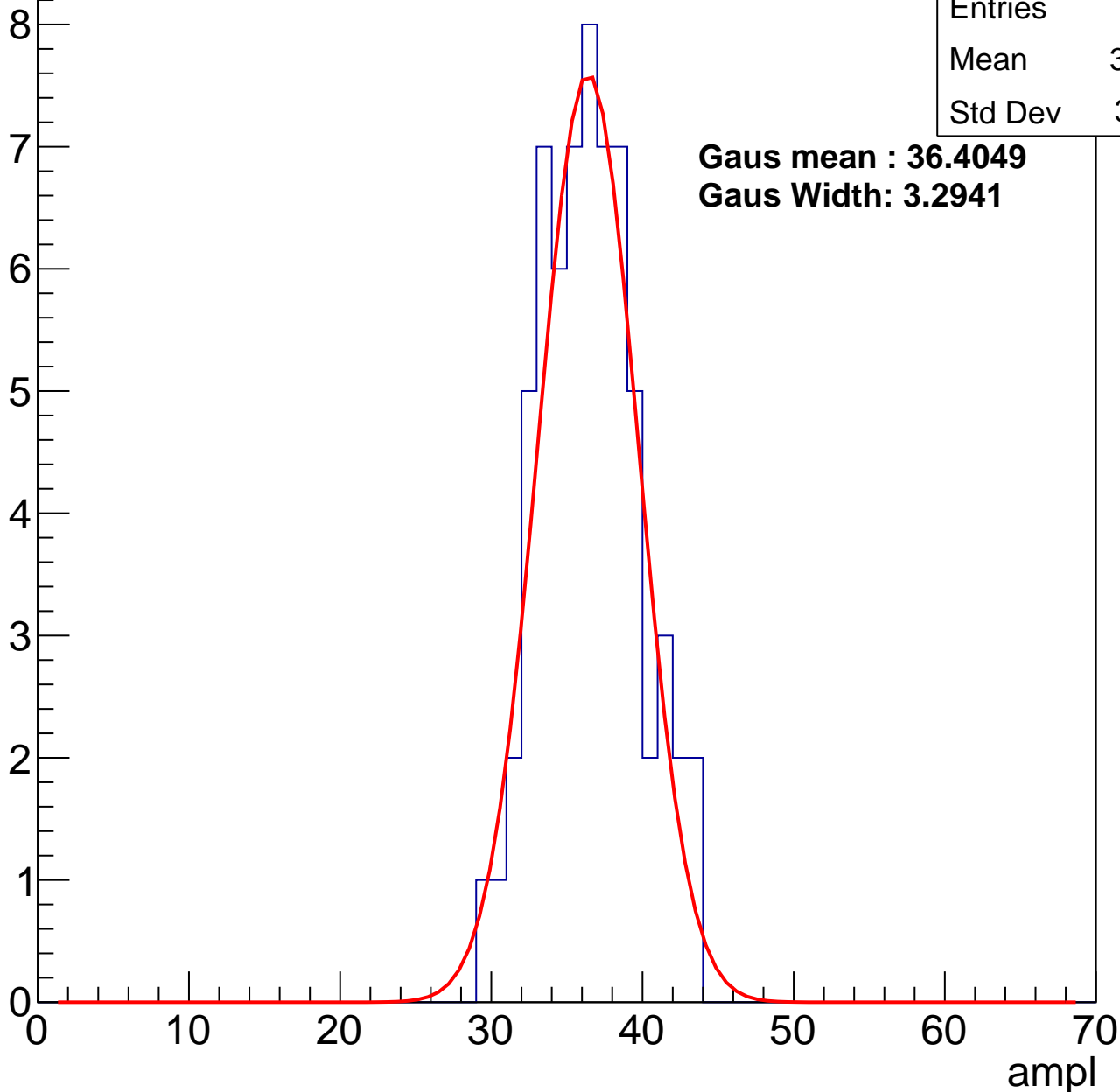
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	36.03
Std Dev	3.201

**Gaus mean : 36.4049**

**Gaus Width: 3.2941**



# B1L101S, U9-ch22, adc2

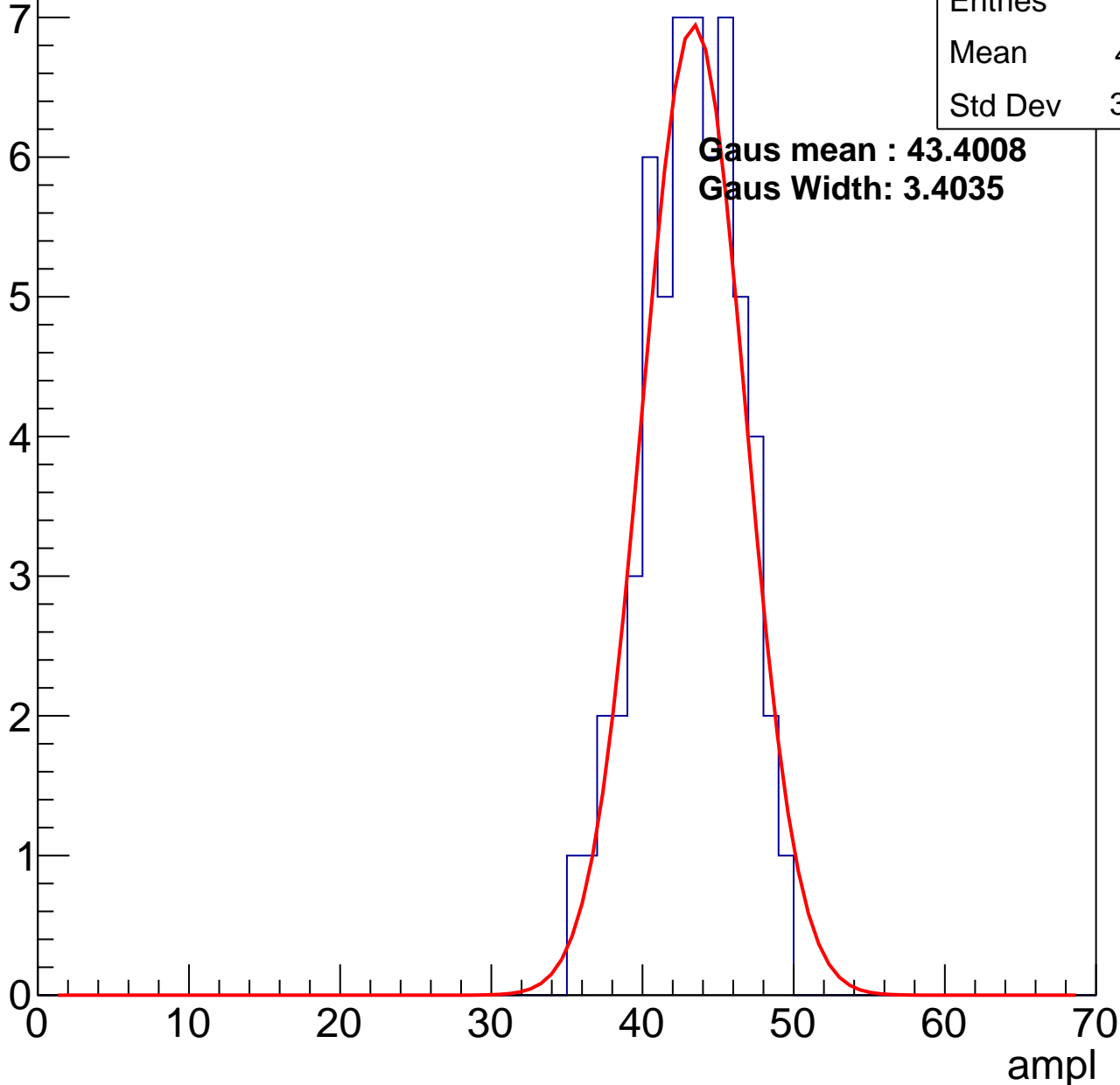
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	42.71
Std Dev	3.157

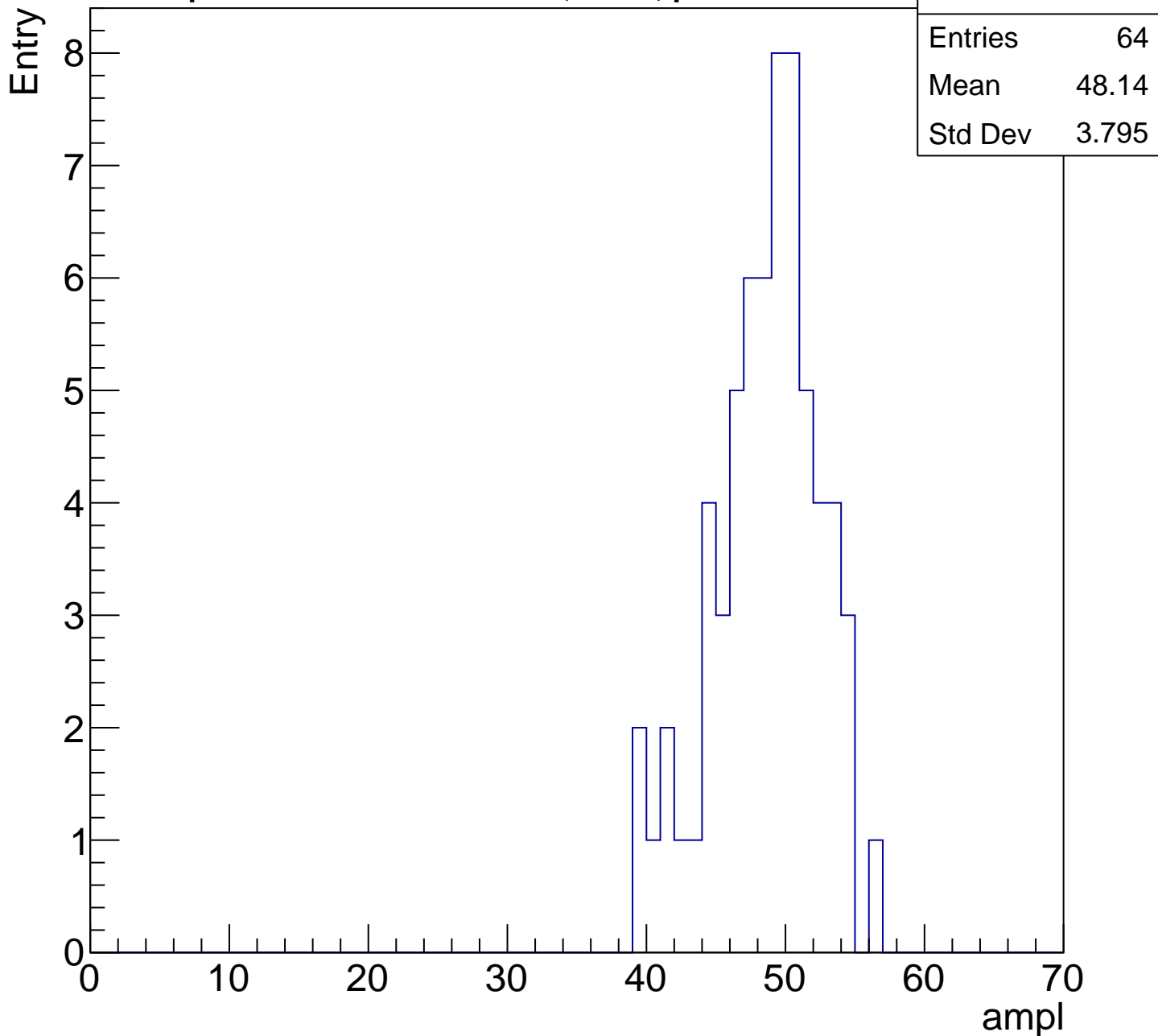
**Gaus mean : 43.4008**

**Gaus Width: 3.4035**



# B1L101S, U9-ch22, adc3

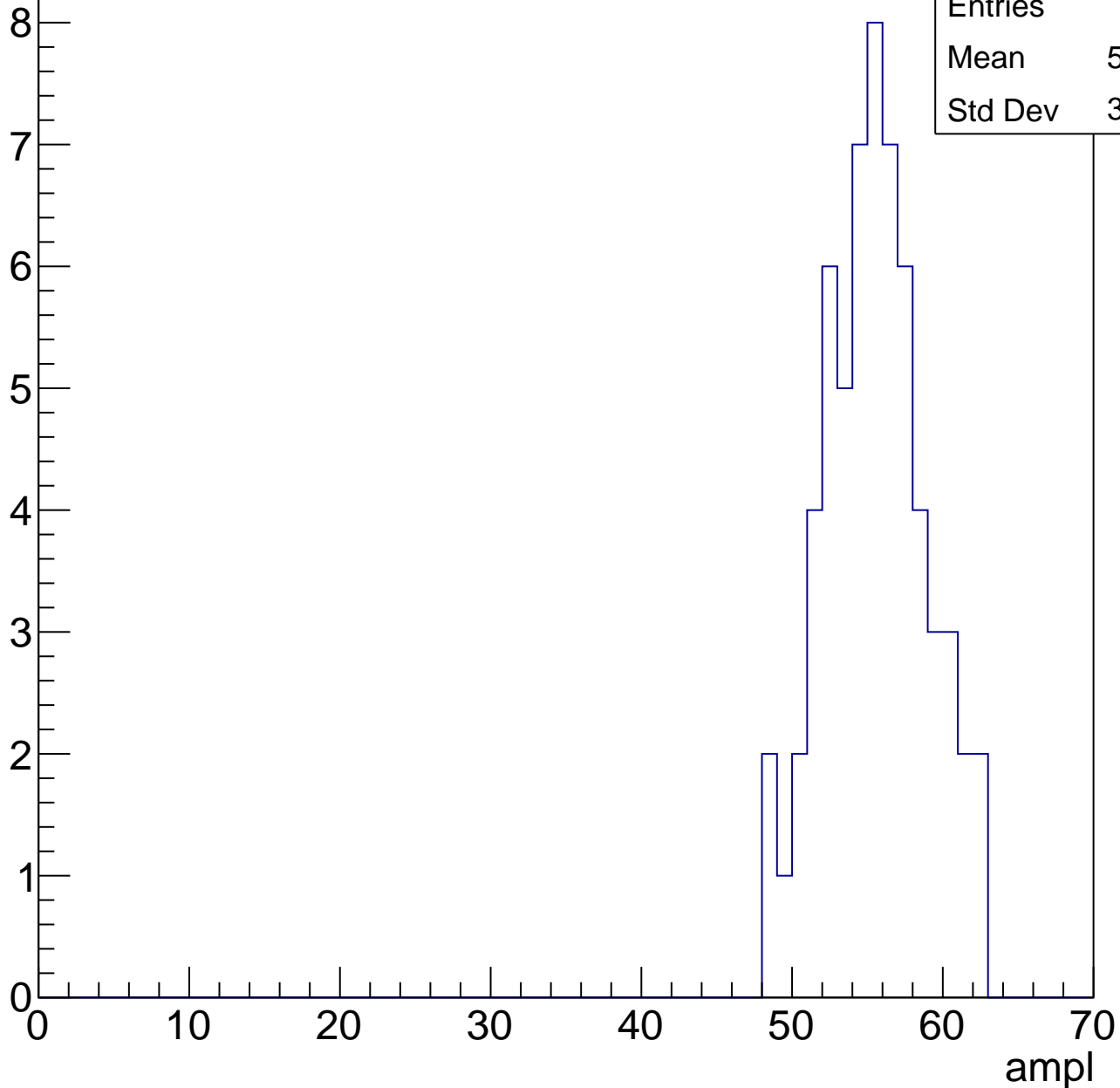
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



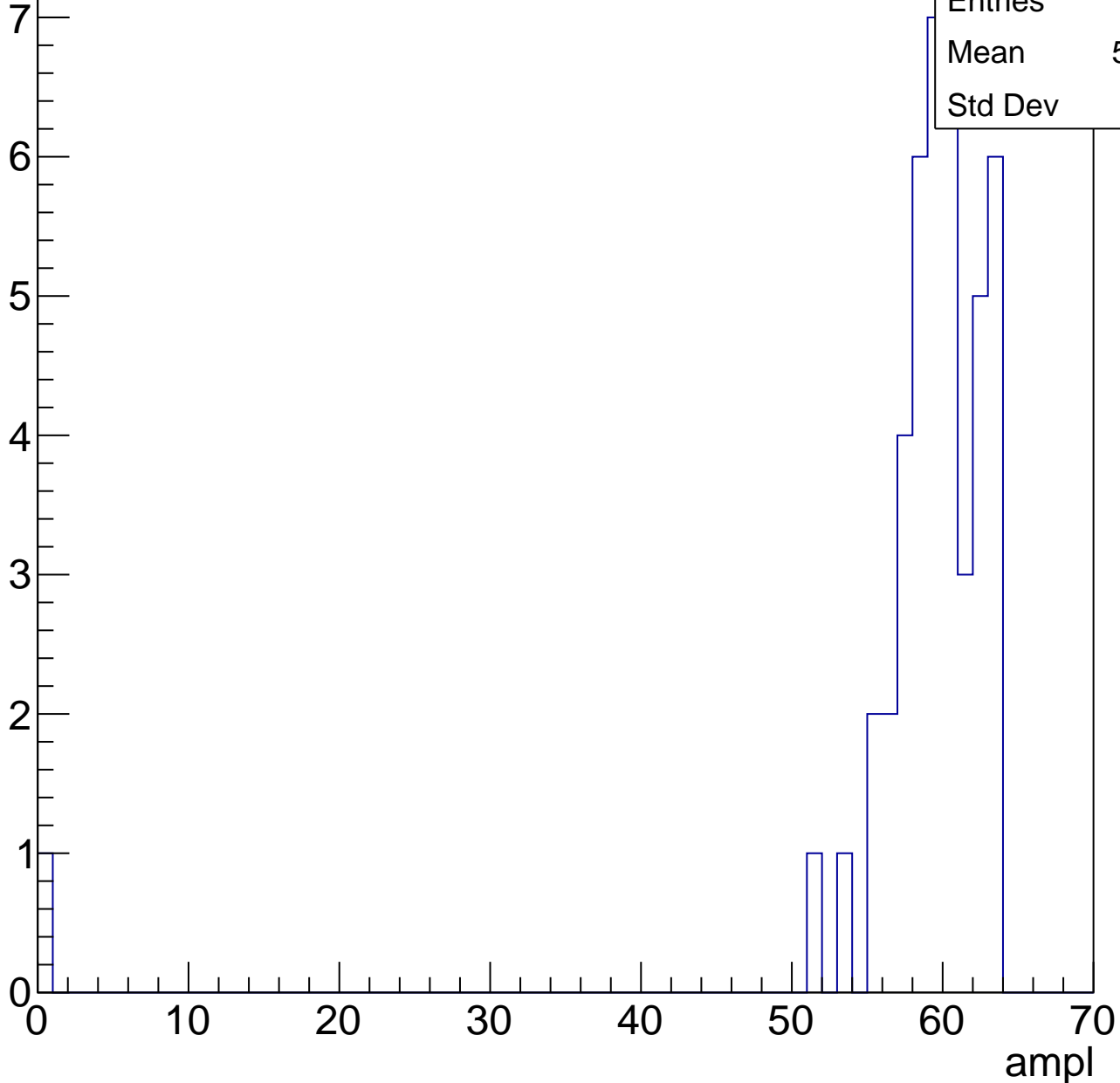
Entries	62
Mean	55.05
Std Dev	3.333

# B1L101S, U9-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	57.91
Std Dev	9.14

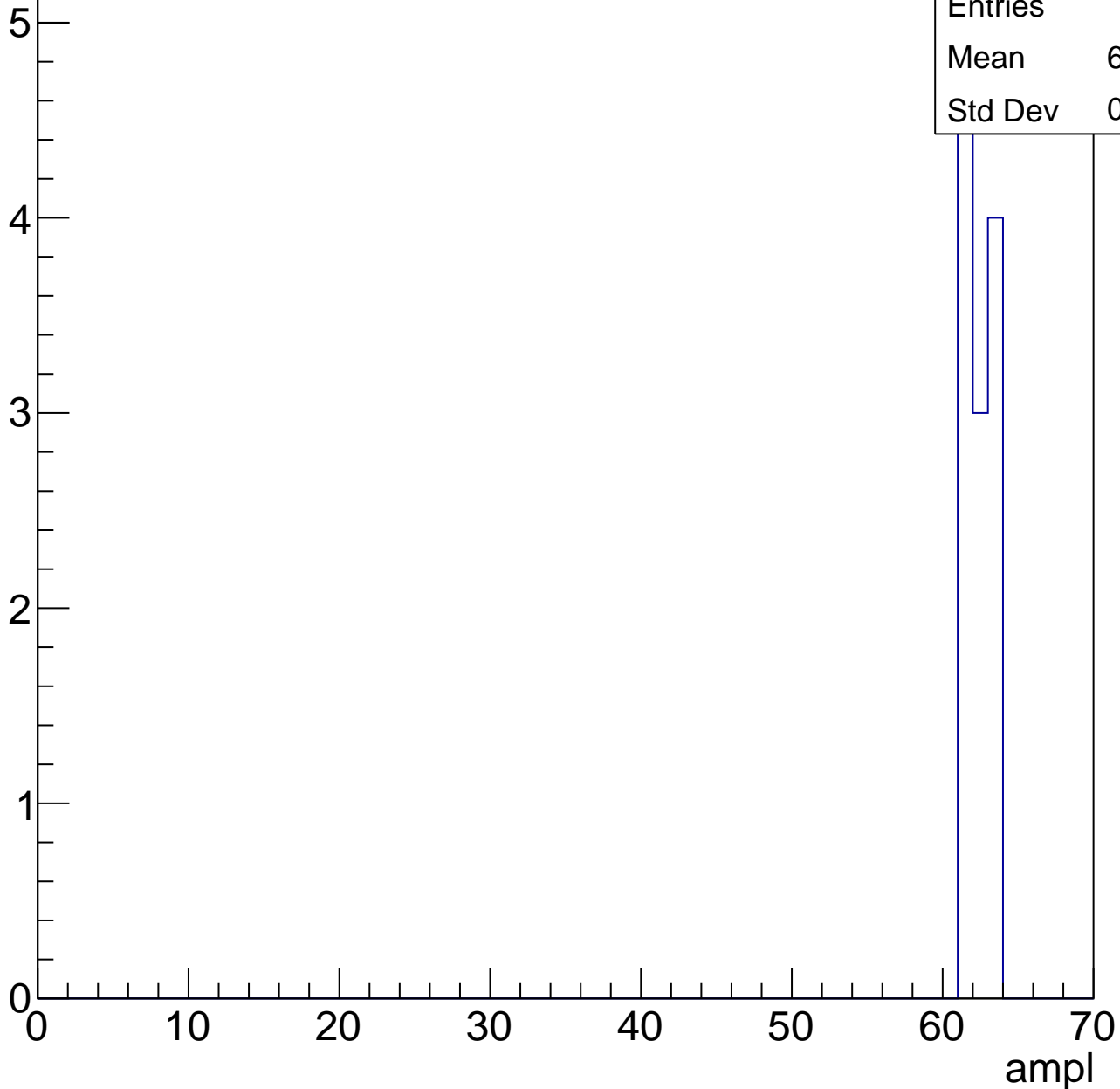


# B1L101S, U9-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	12
Mean	61.92
Std Dev	0.862





# B1L101S, U9-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U9-ch23, adc0

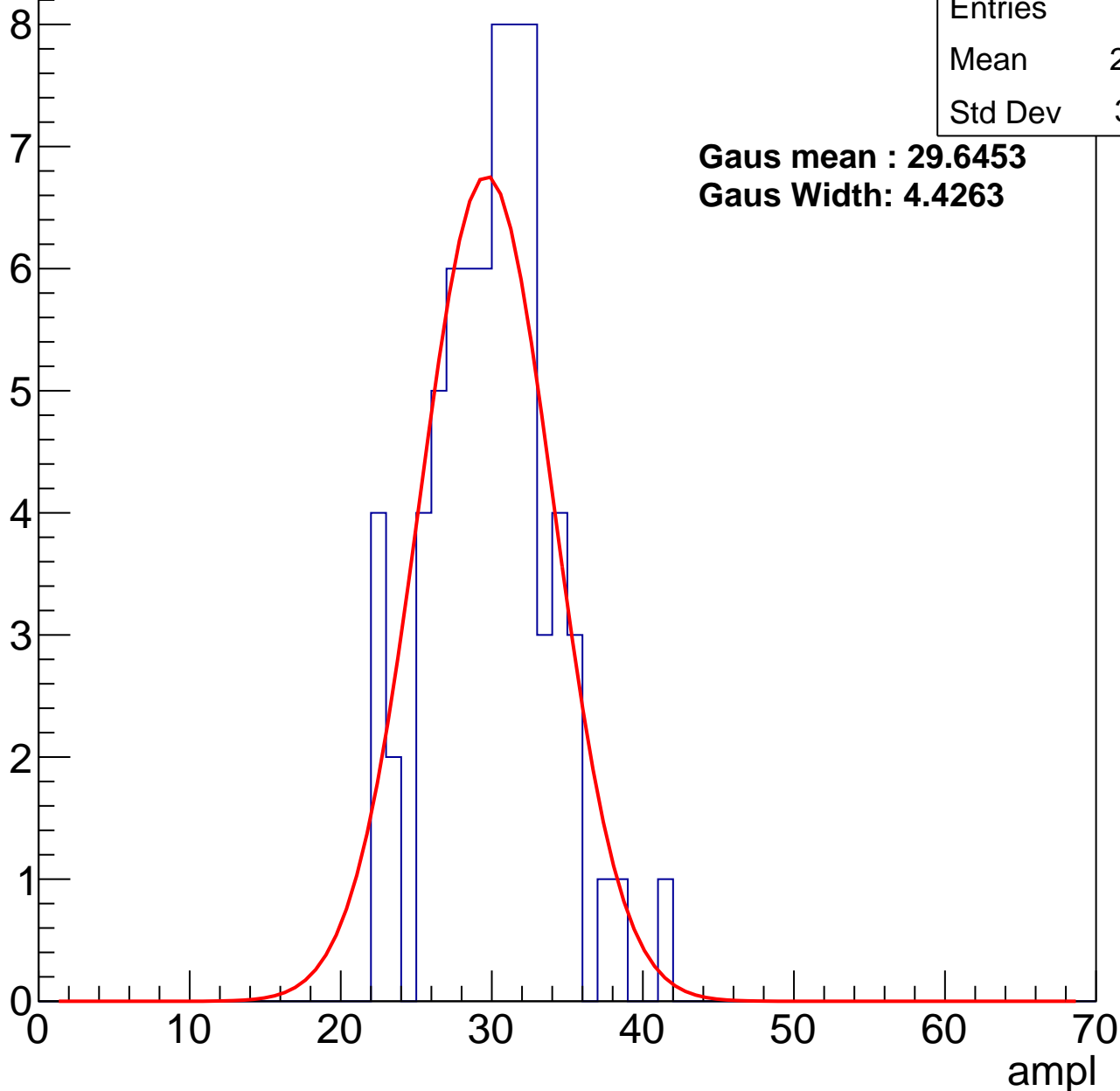
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	29.54
Std Dev	3.861

**Gaus mean : 29.6453**

**Gaus Width: 4.4263**



# B1L101S, U9-ch23, adc1

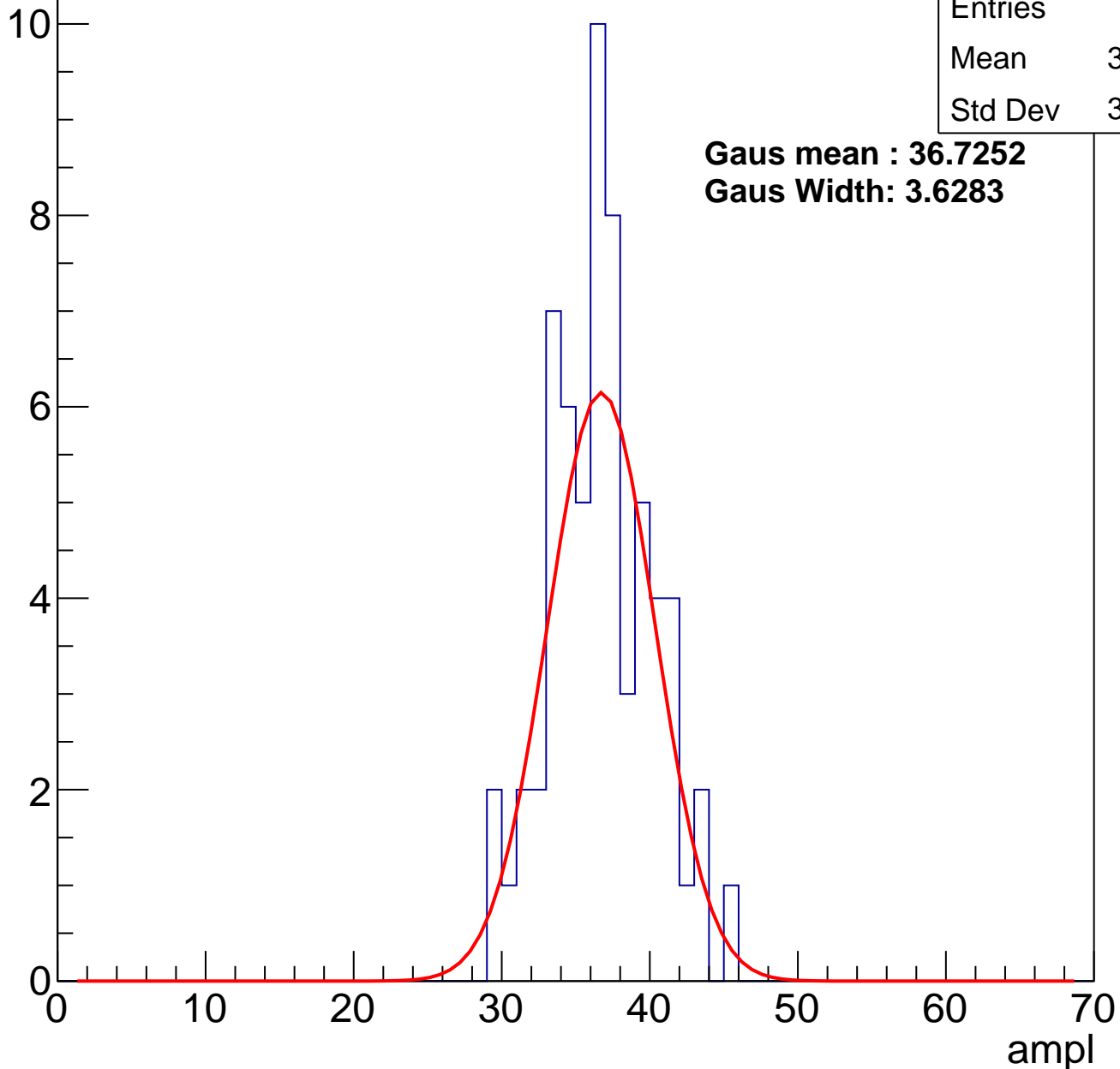
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	63
Mean	36.29
Std Dev	3.443

**Gaus mean : 36.7252**

**Gaus Width: 3.6283**

Entry



# B1L101S, U9-ch23, adc2

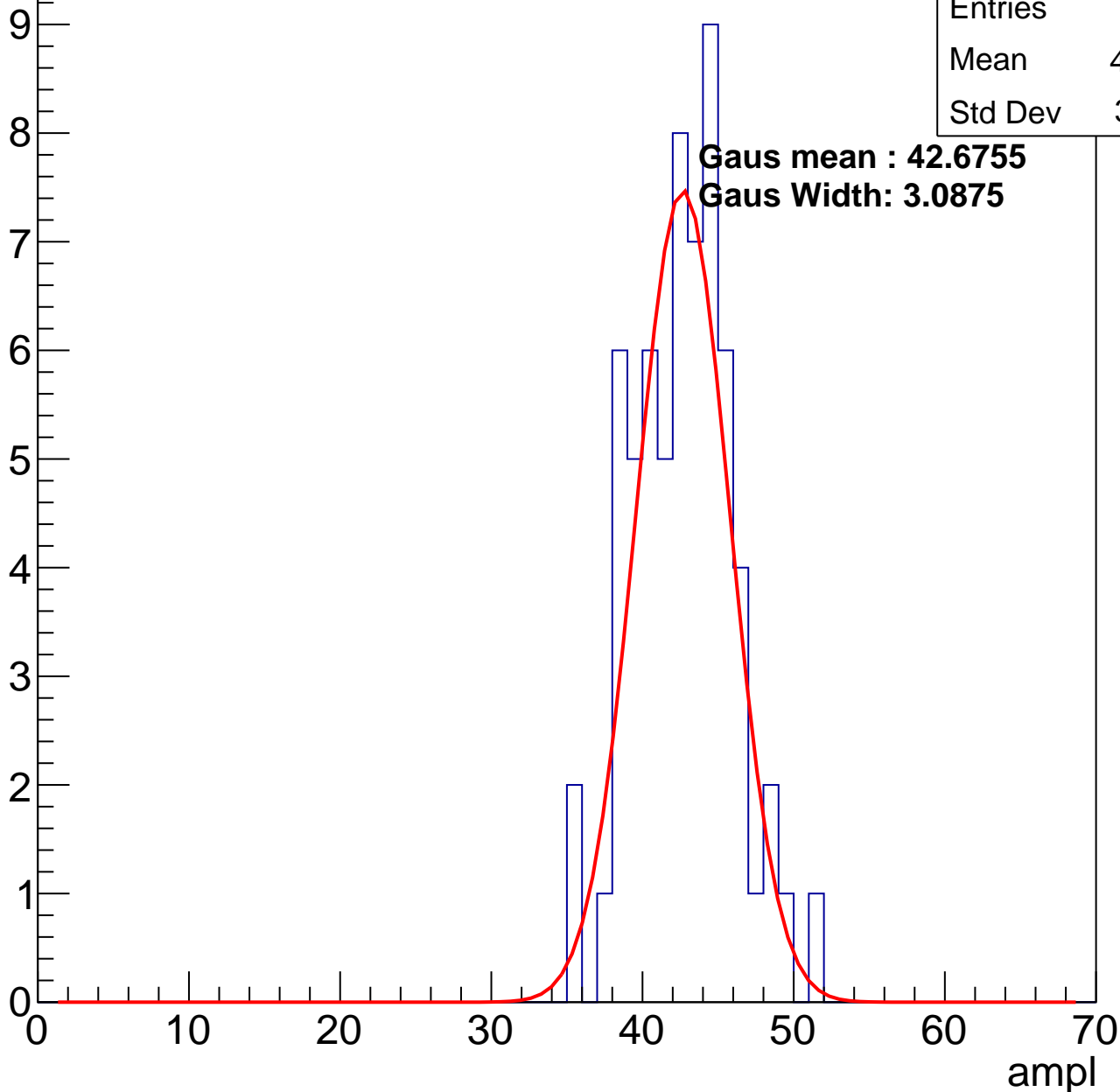
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	42.27
Std Dev	3.251

**Gaus mean : 42.6755**

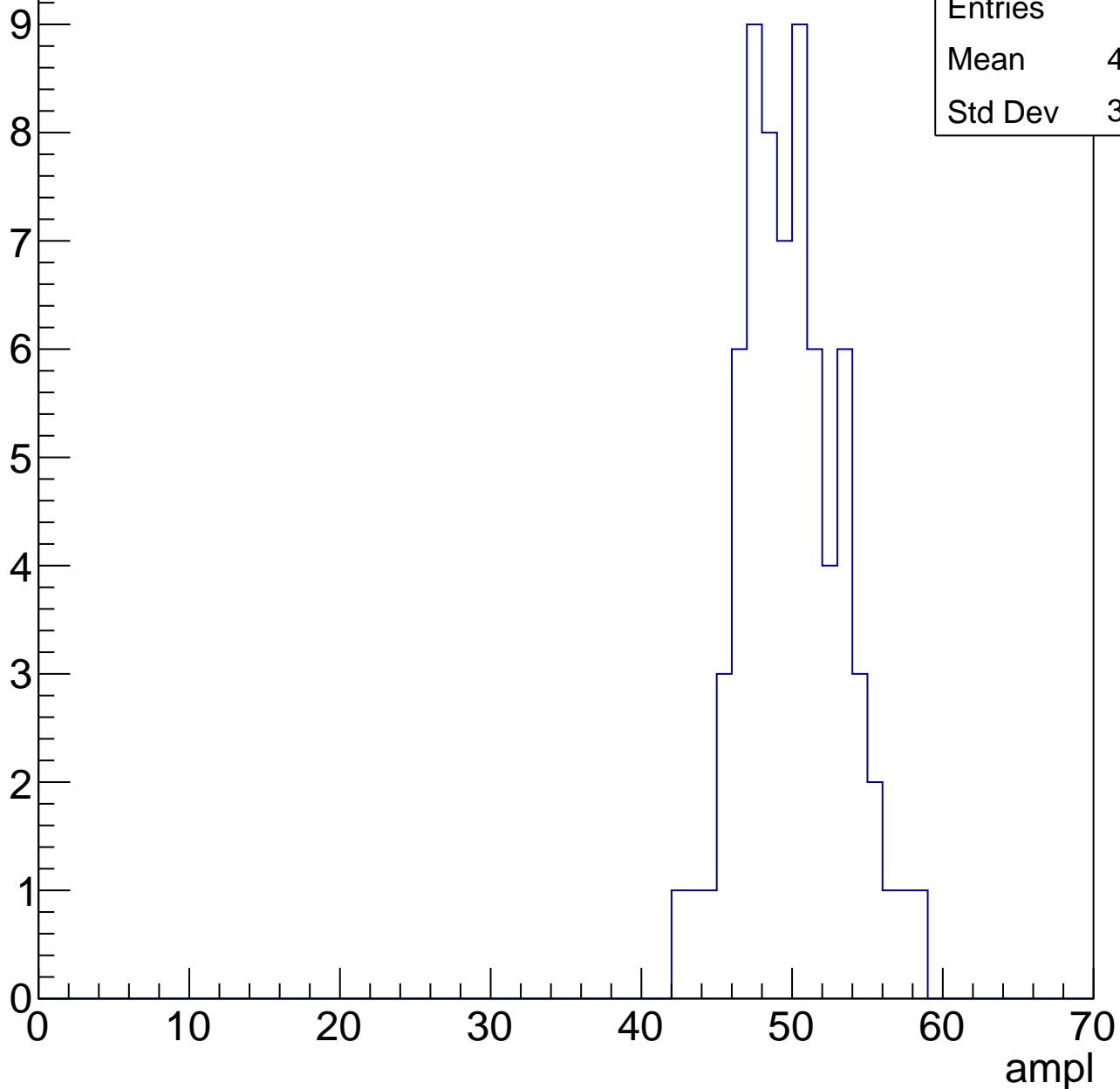
**Gaus Width: 3.0875**



# B1L101S, U9-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

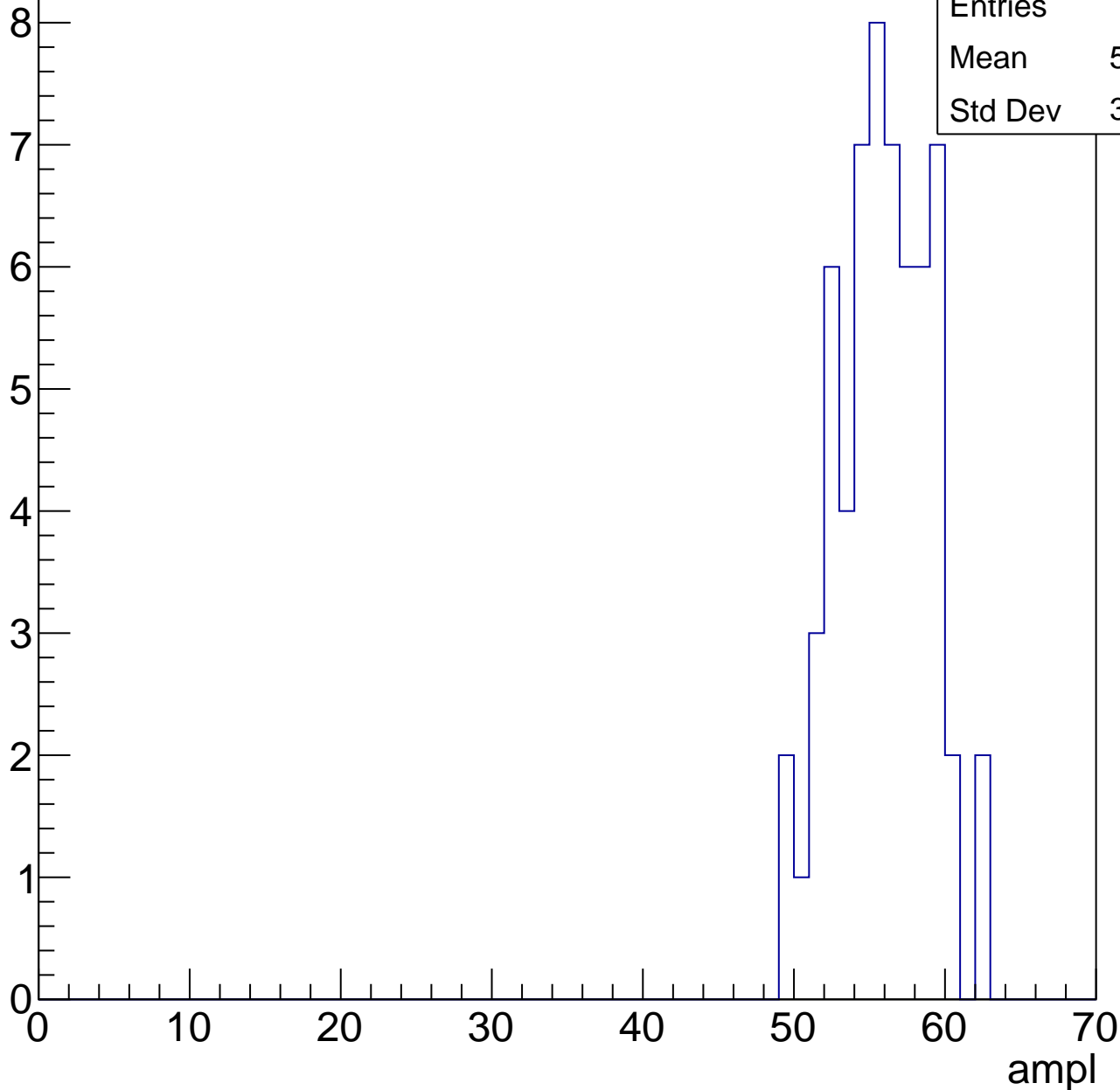


Entries	69
Mean	49.49
Std Dev	3.286

# B1L101S, U9-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



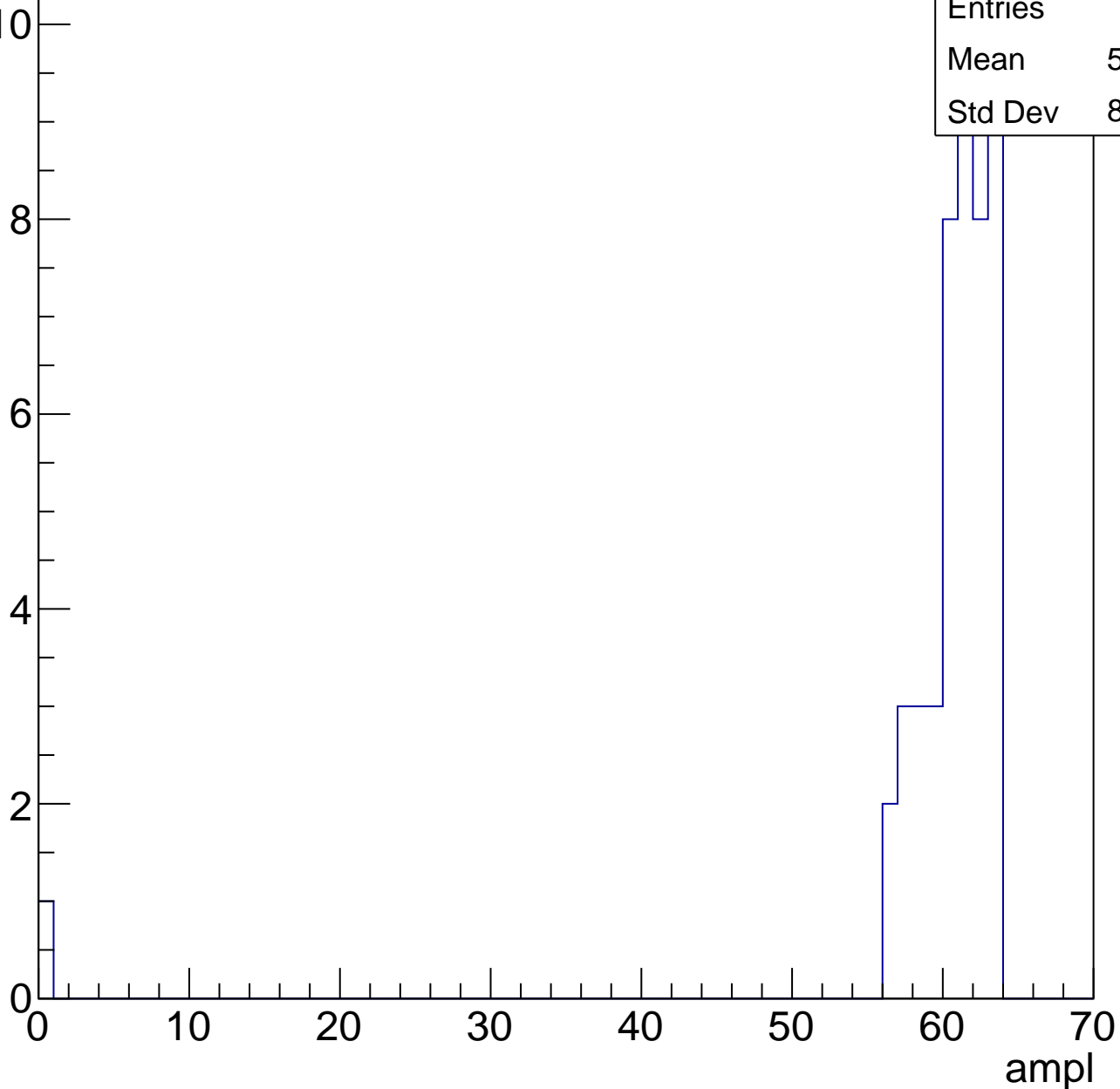
Entries	61
Mean	55.44
Std Dev	3.016

# B1L101S, U9-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	59.34
Std Dev	8.973



# B1L101S, U9-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch24, adc0

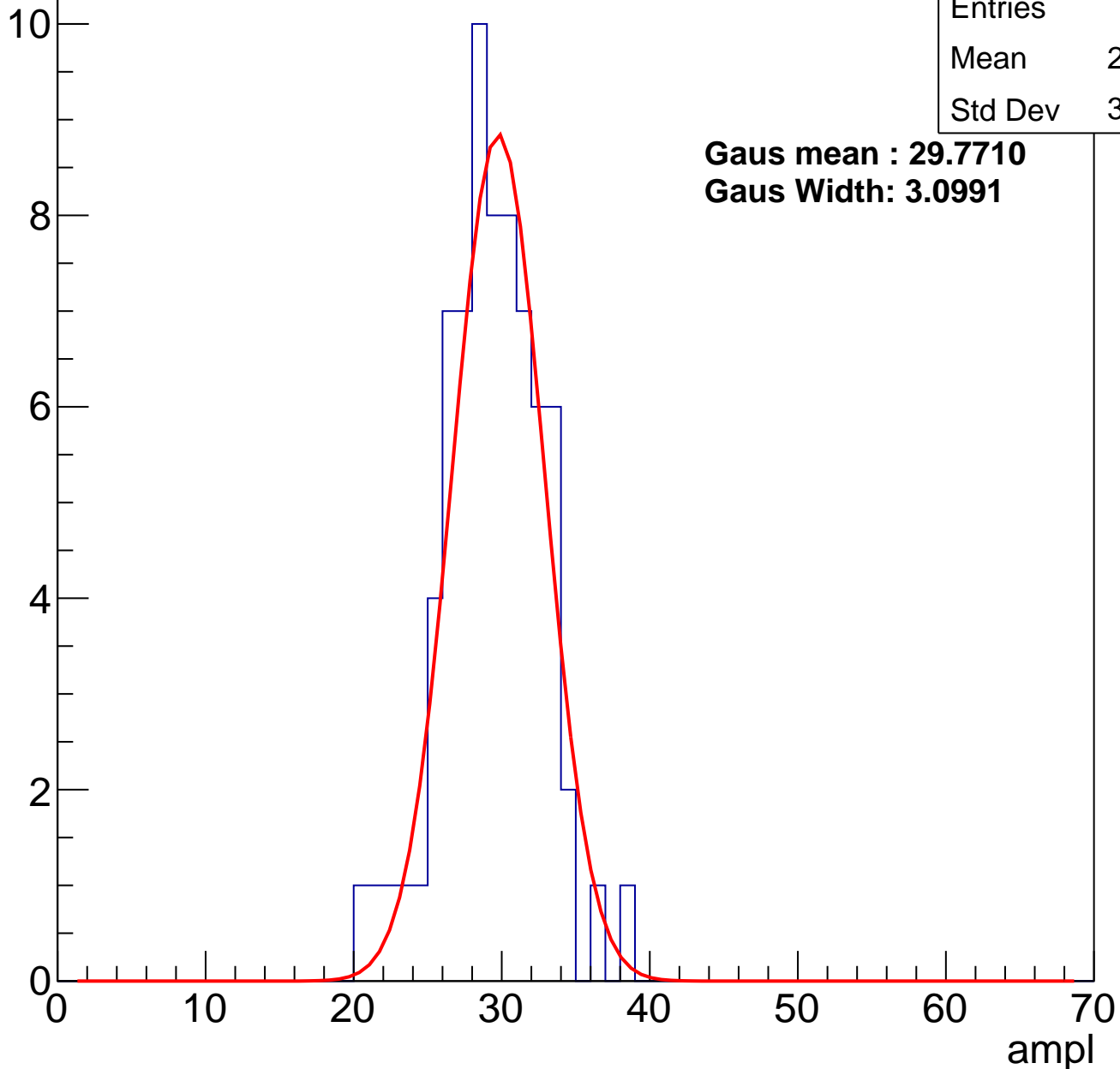
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	72
Mean	28.92
Std Dev	3.303

**Gaus mean : 29.7710**

**Gaus Width: 3.0991**

Entry



# B1L101S, U9-ch24, adc1

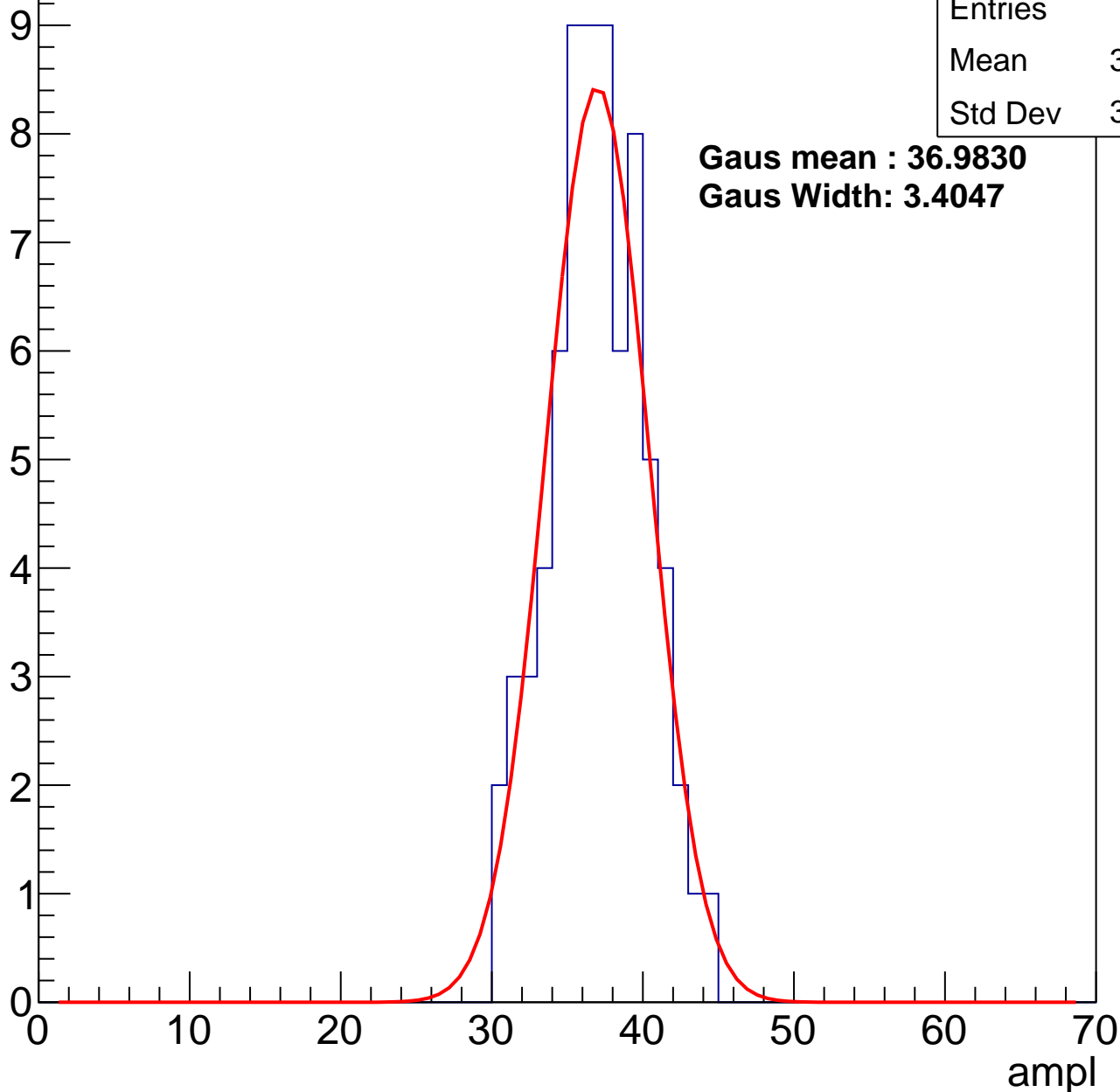
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	36.56
Std Dev	3.144

**Gaus mean : 36.9830**

**Gaus Width: 3.4047**



# B1L101S, U9-ch24, adc2

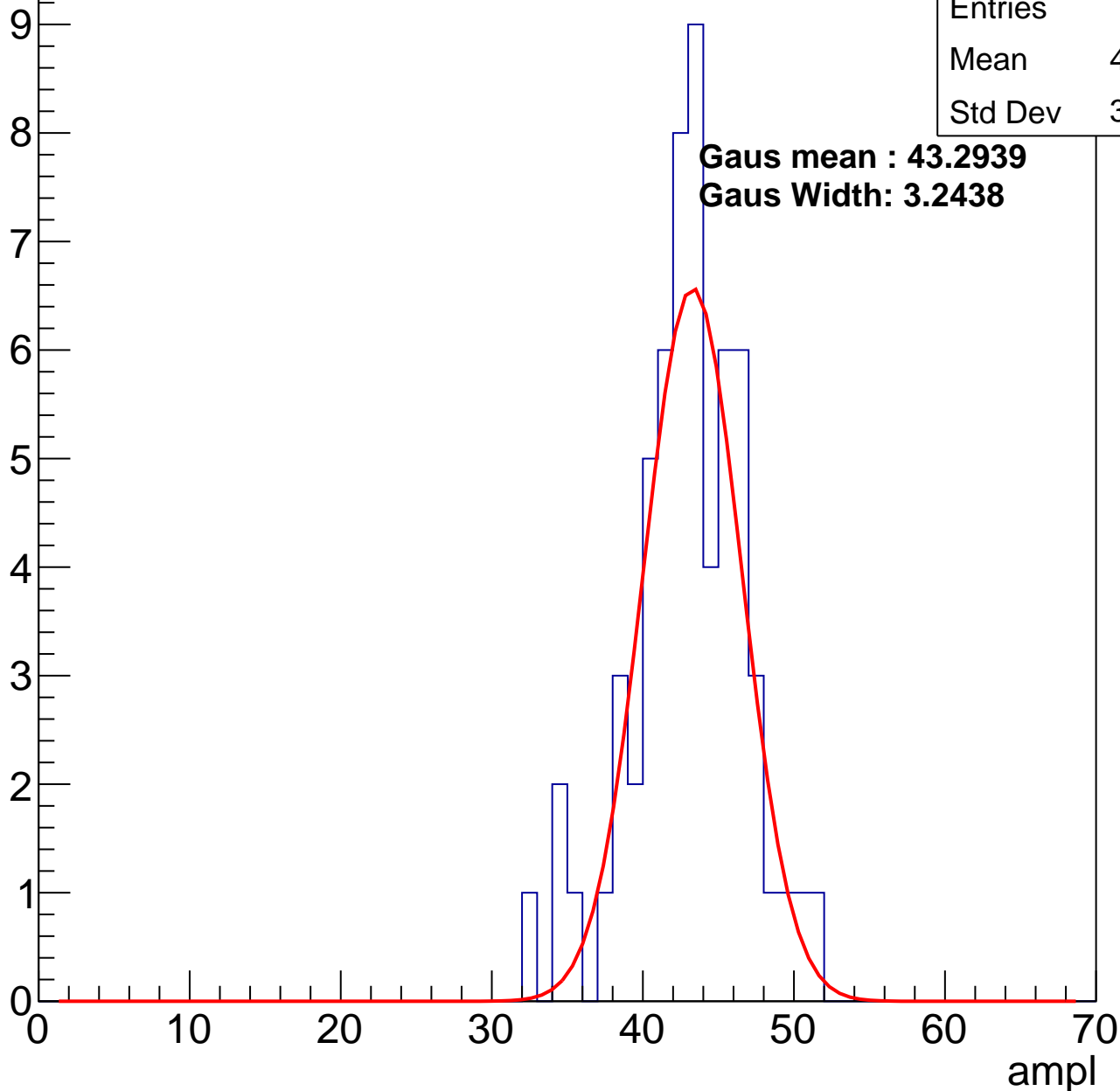
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	42.52
Std Dev	3.749

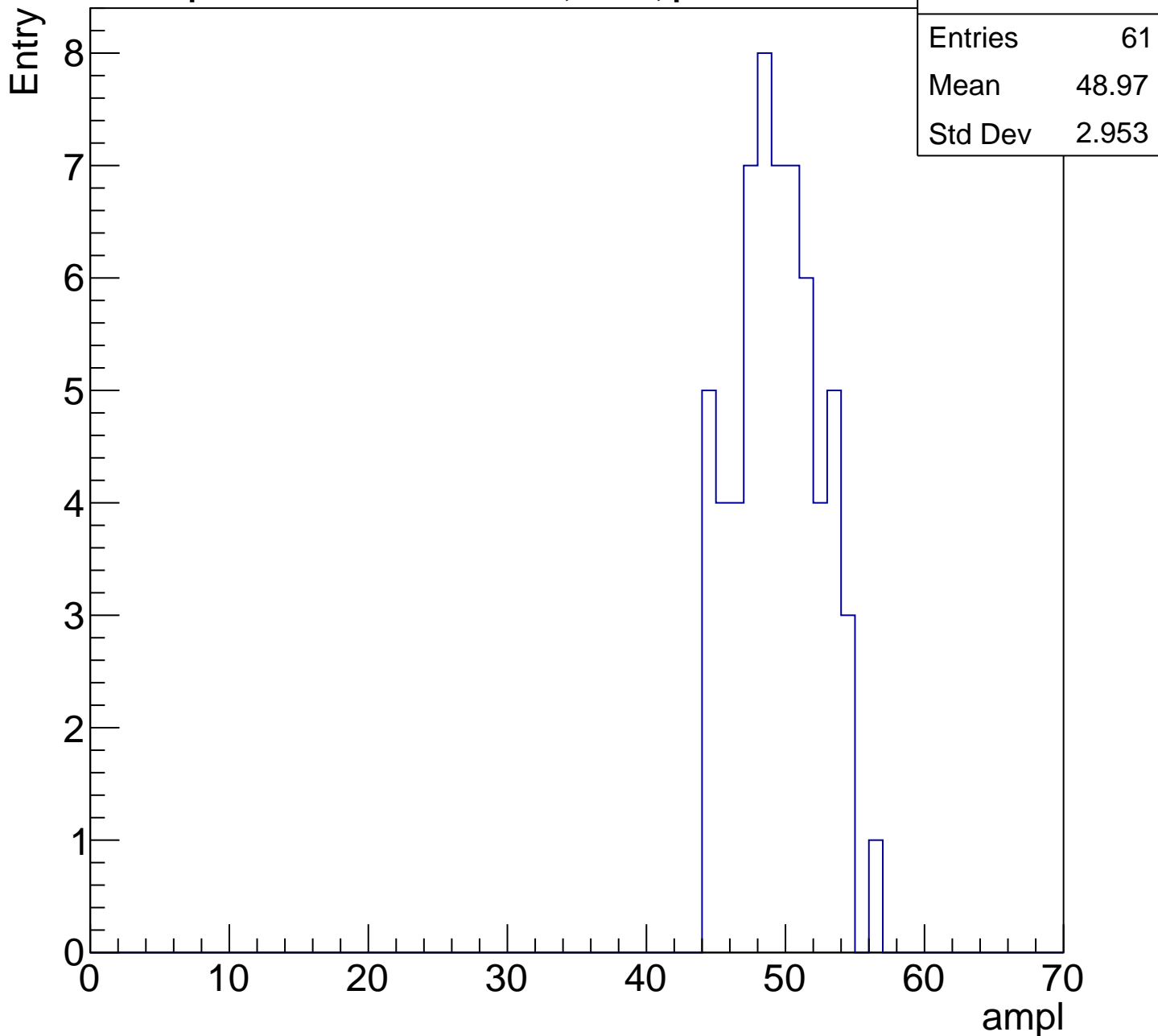
**Gaus mean : 43.2939**

**Gaus Width: 3.2438**



# B1L101S, U9-ch24, adc3

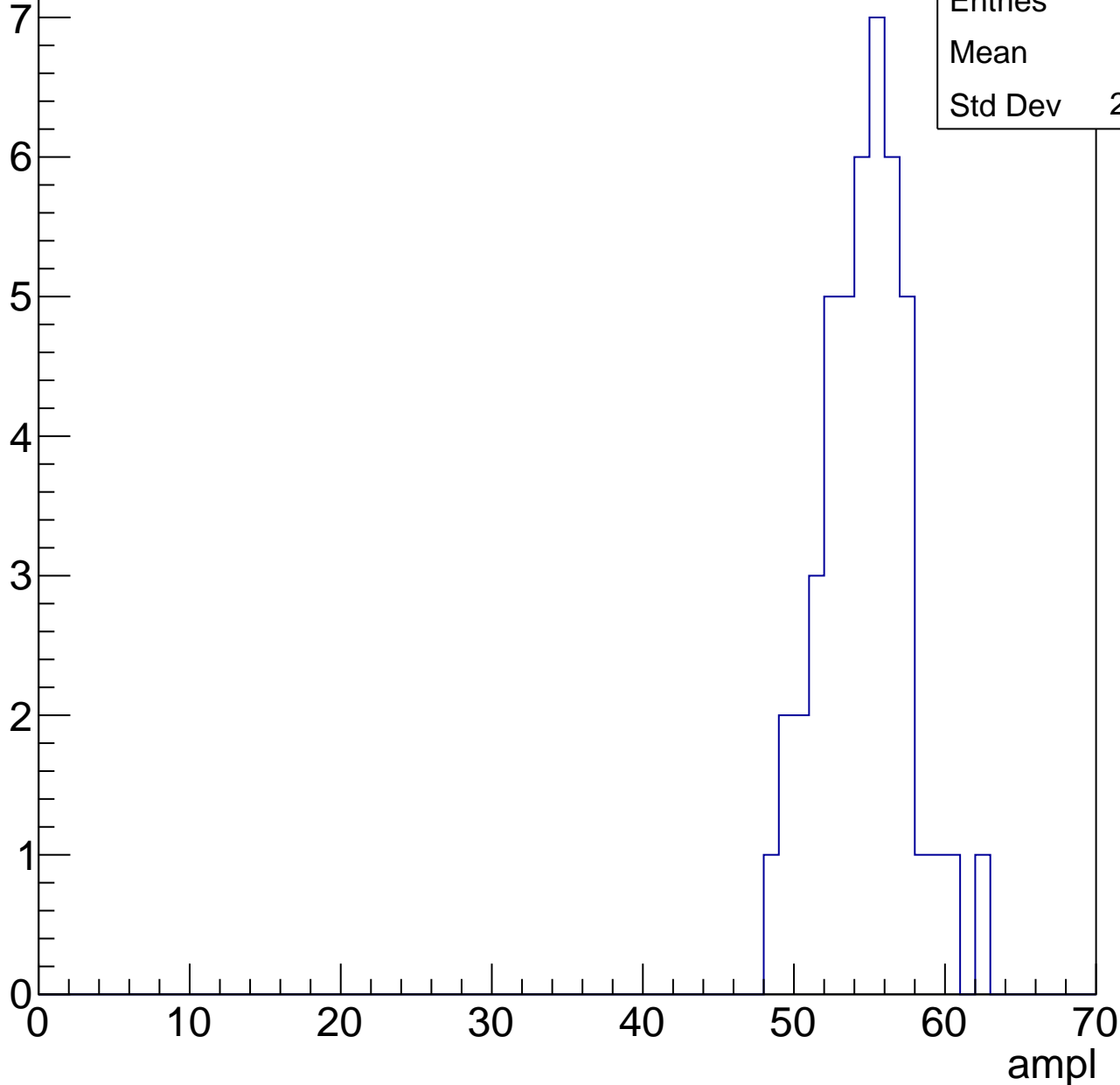
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



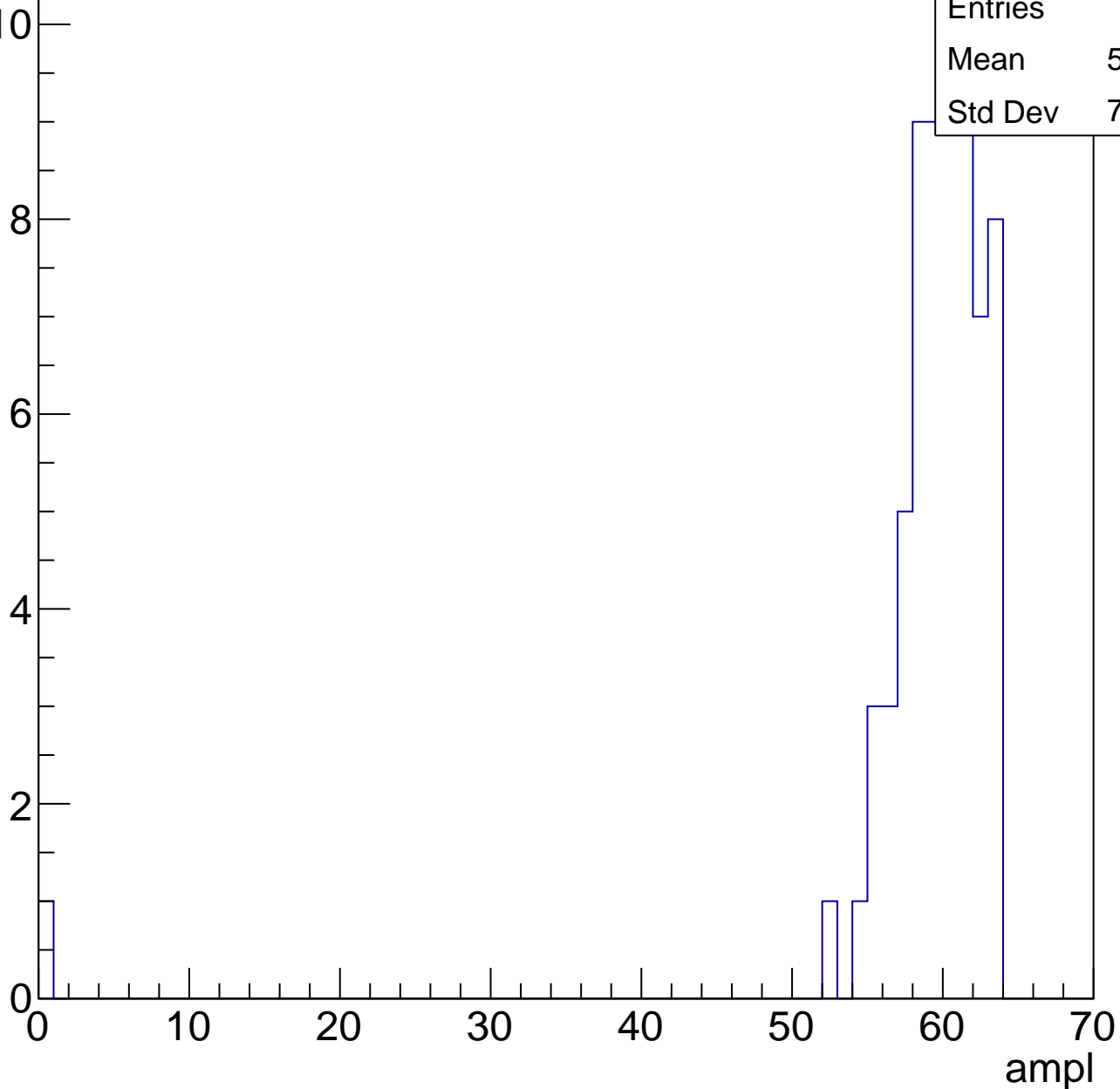
Entries	46
Mean	54.2
Std Dev	2.894

# B1L101S, U9-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	58.56
Std Dev	7.674



# B1L101S, U9-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch25, adc0

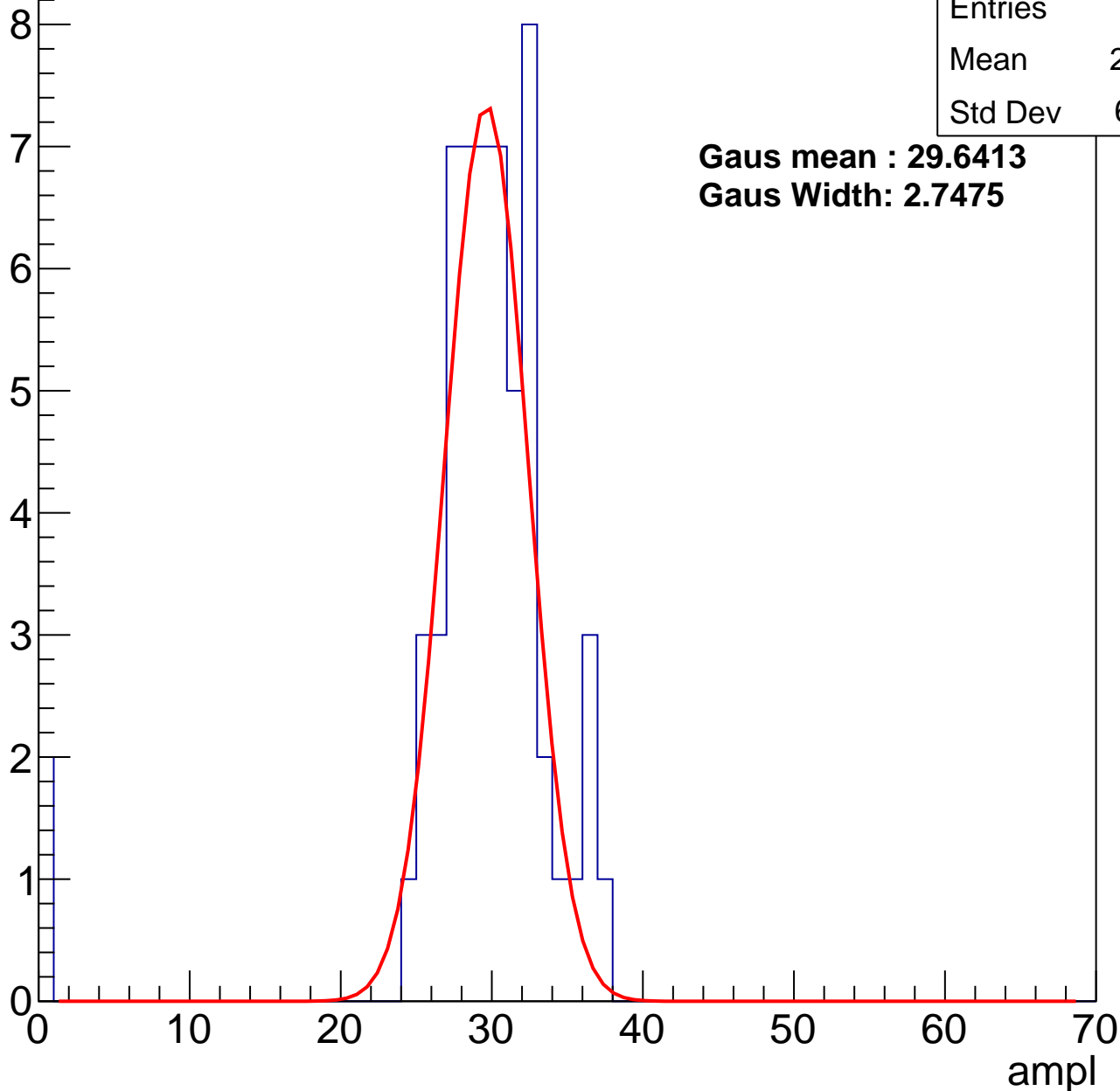
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	28.72
Std Dev	6.181

**Gaus mean : 29.6413**

**Gaus Width: 2.7475**



# B1L101S, U9-ch25, adc1

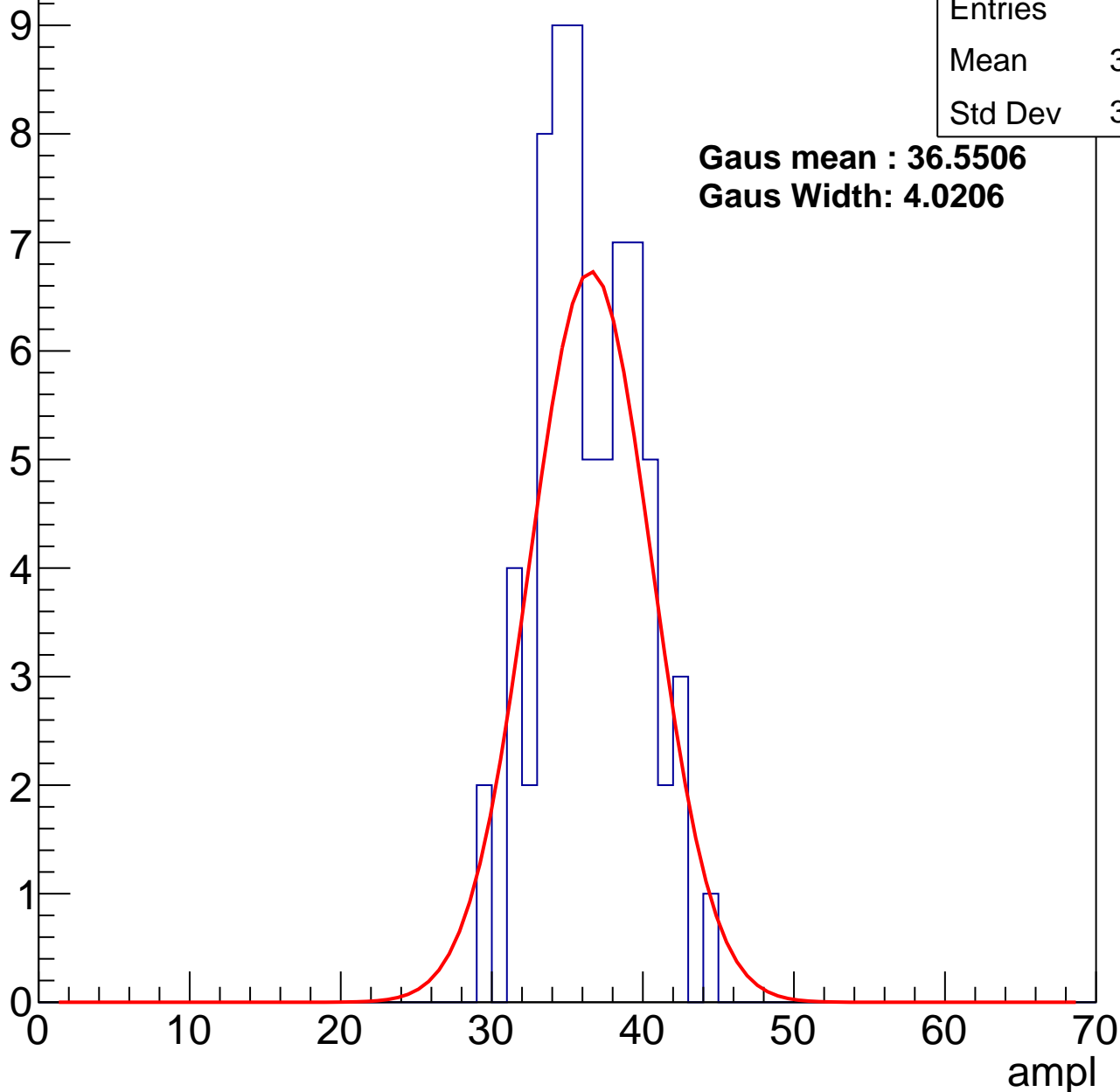
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	36.04
Std Dev	3.286

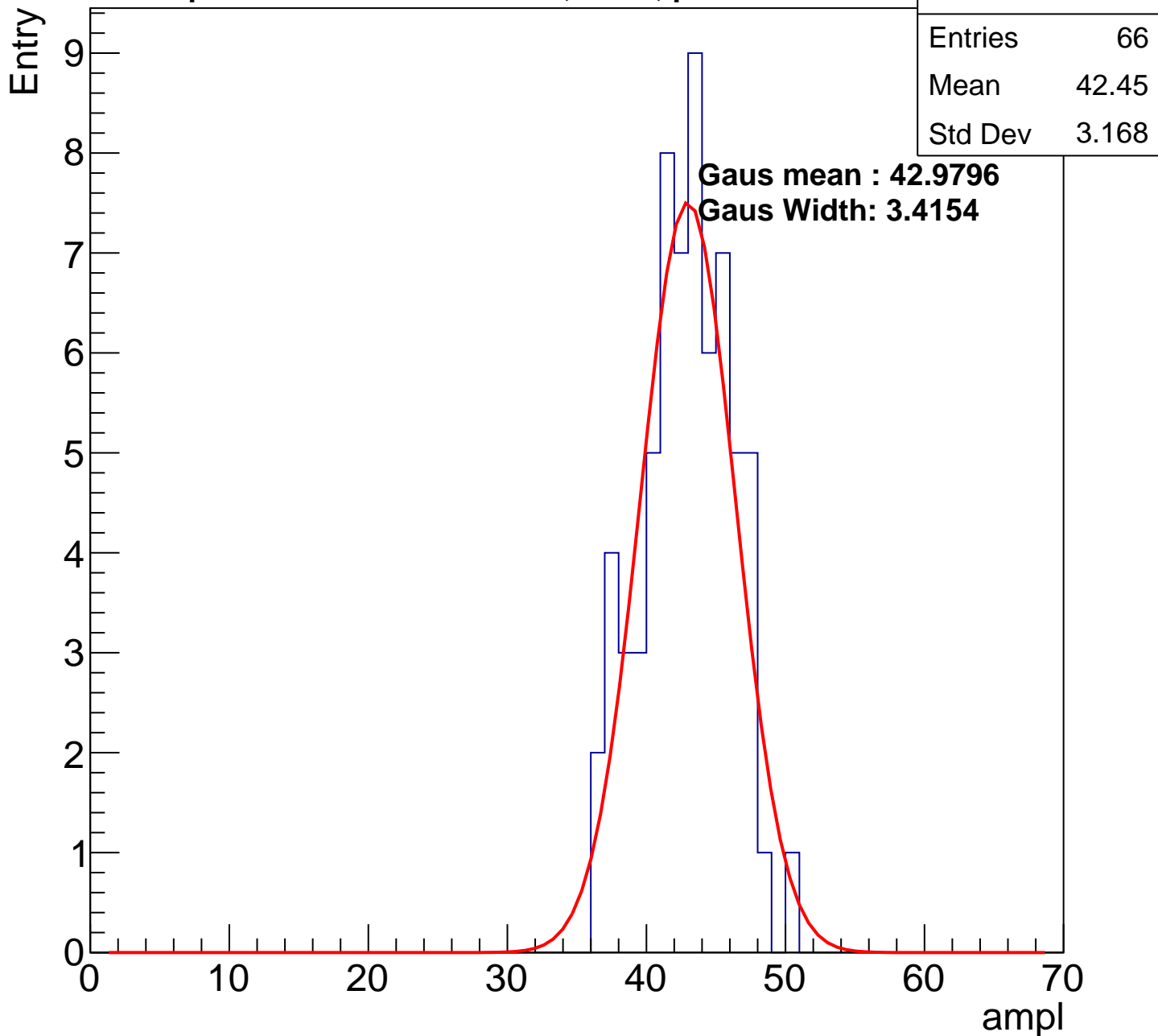
**Gaus mean : 36.5506**

**Gaus Width: 4.0206**



# B1L101S, U9-ch25, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

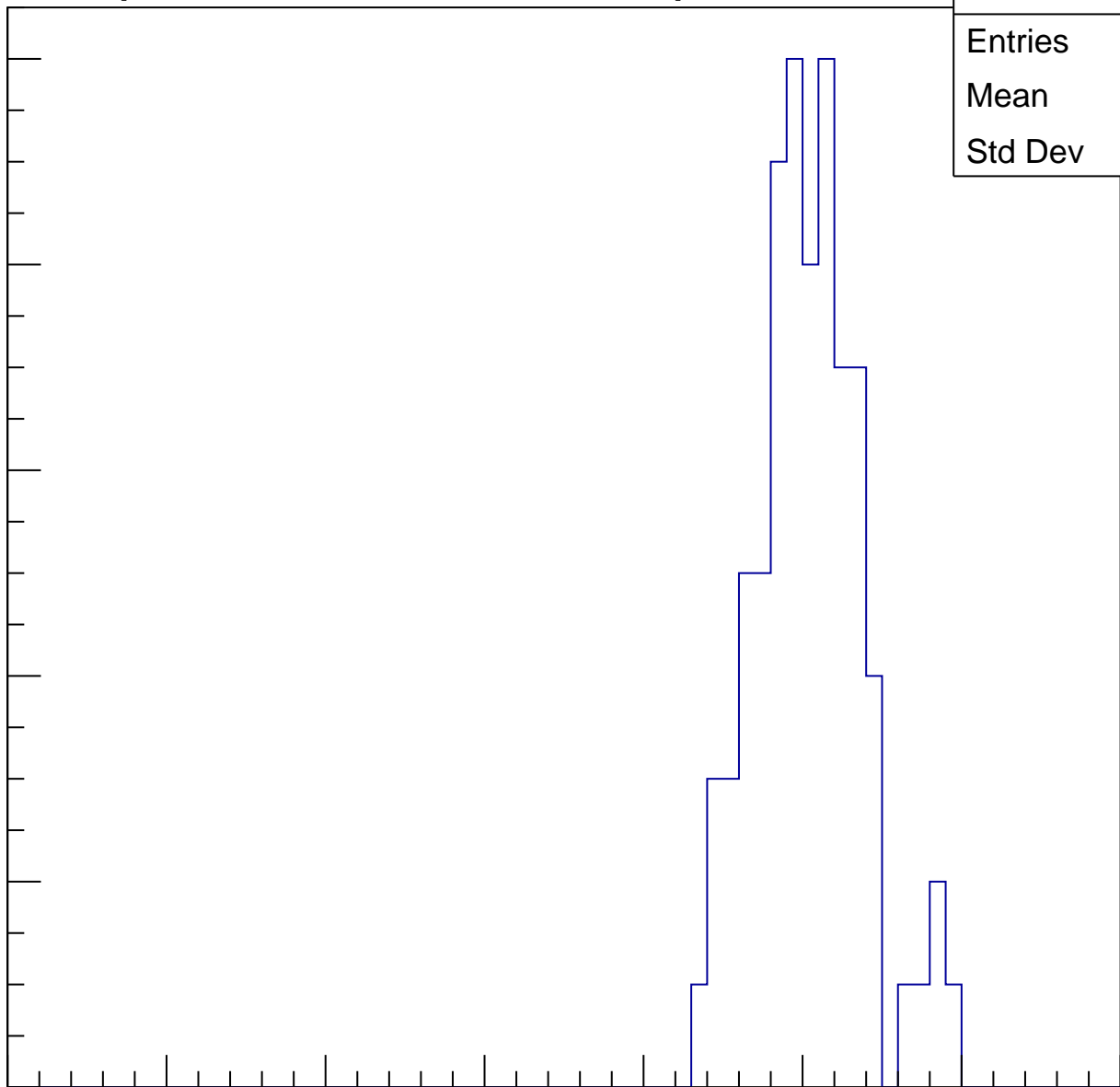
Entries	77
Mean	49.95
Std Dev	3.345

Entry

10  
8  
6  
4  
2  
0

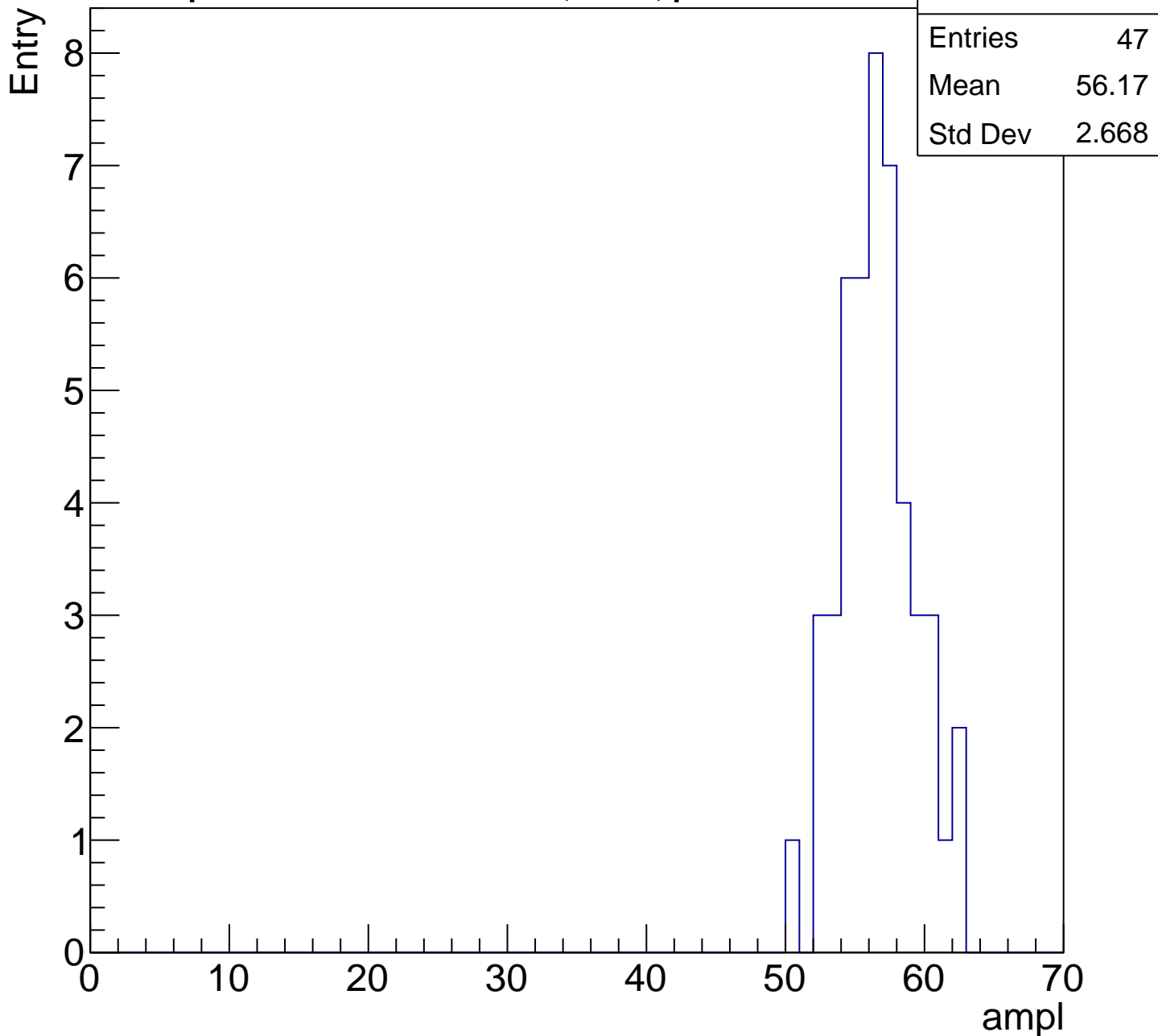
0 10 20 30 40 50 60 70

ampl



# B1L101S, U9-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

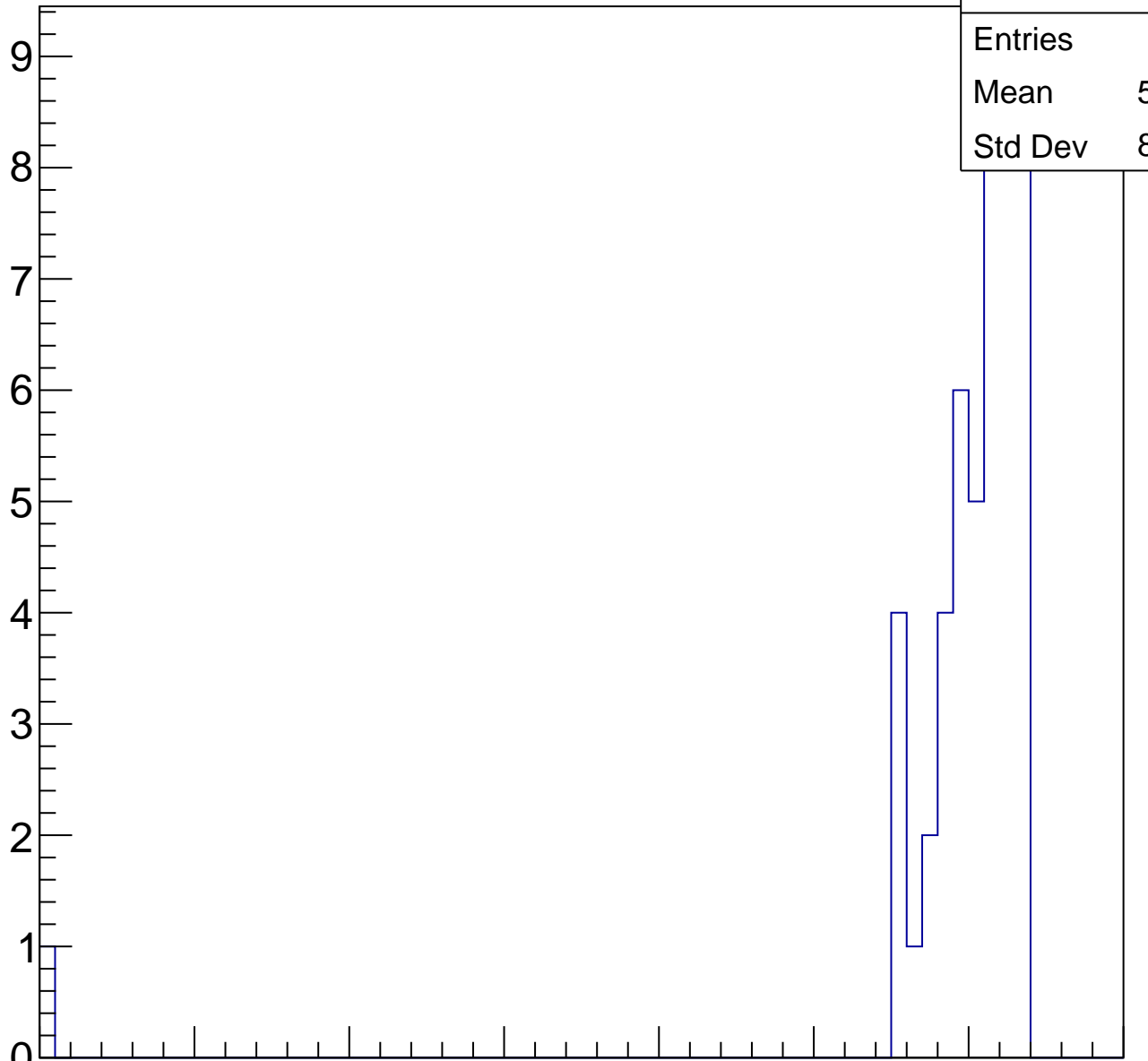
Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	58.94
Std Dev	8.833

ampl

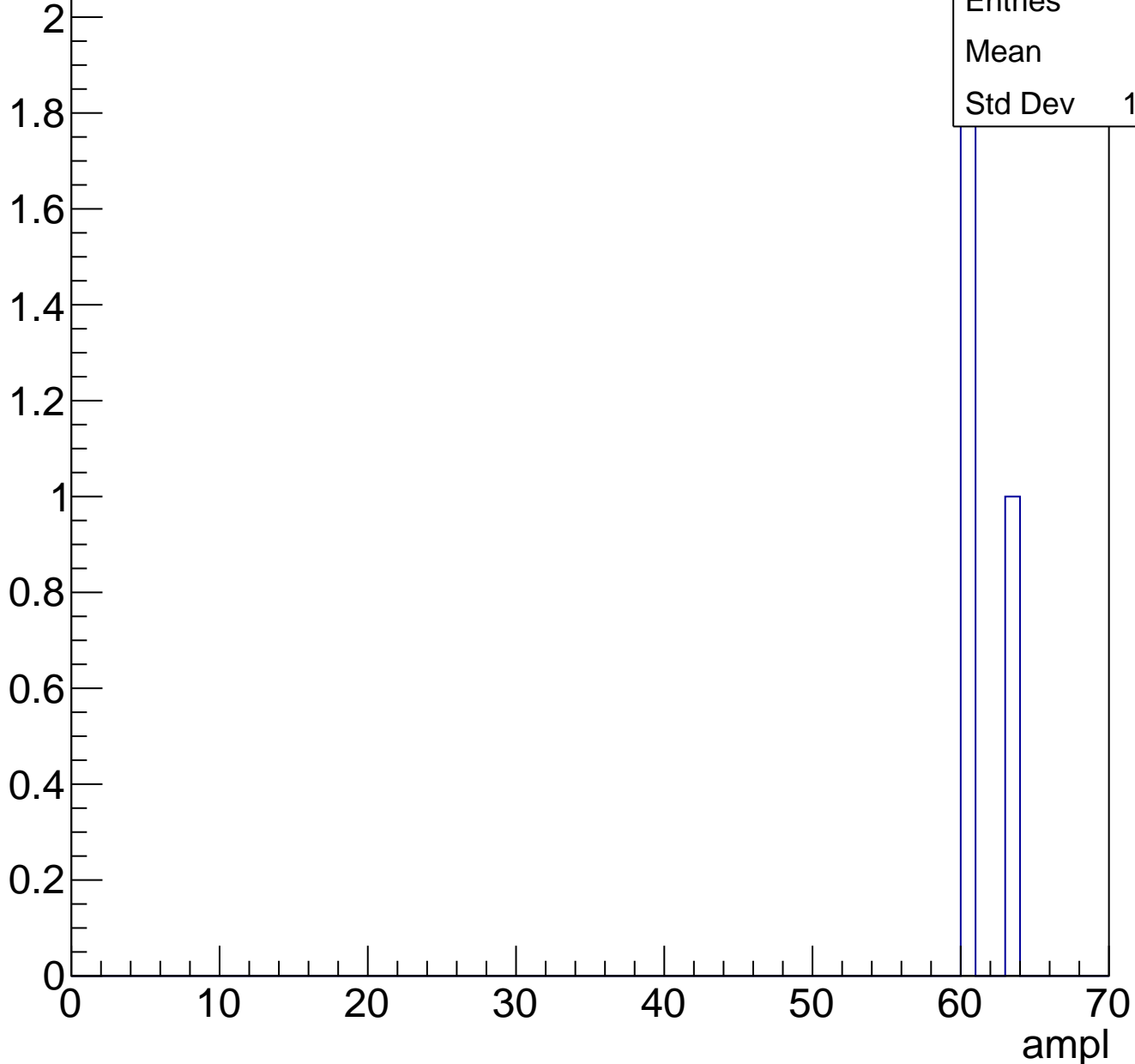
0 10 20 30 40 50 60 70



# B1L101S, U9-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch26, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	67
Mean	28.85
Std Dev	4.854

**Gaus mean : 29.8367**

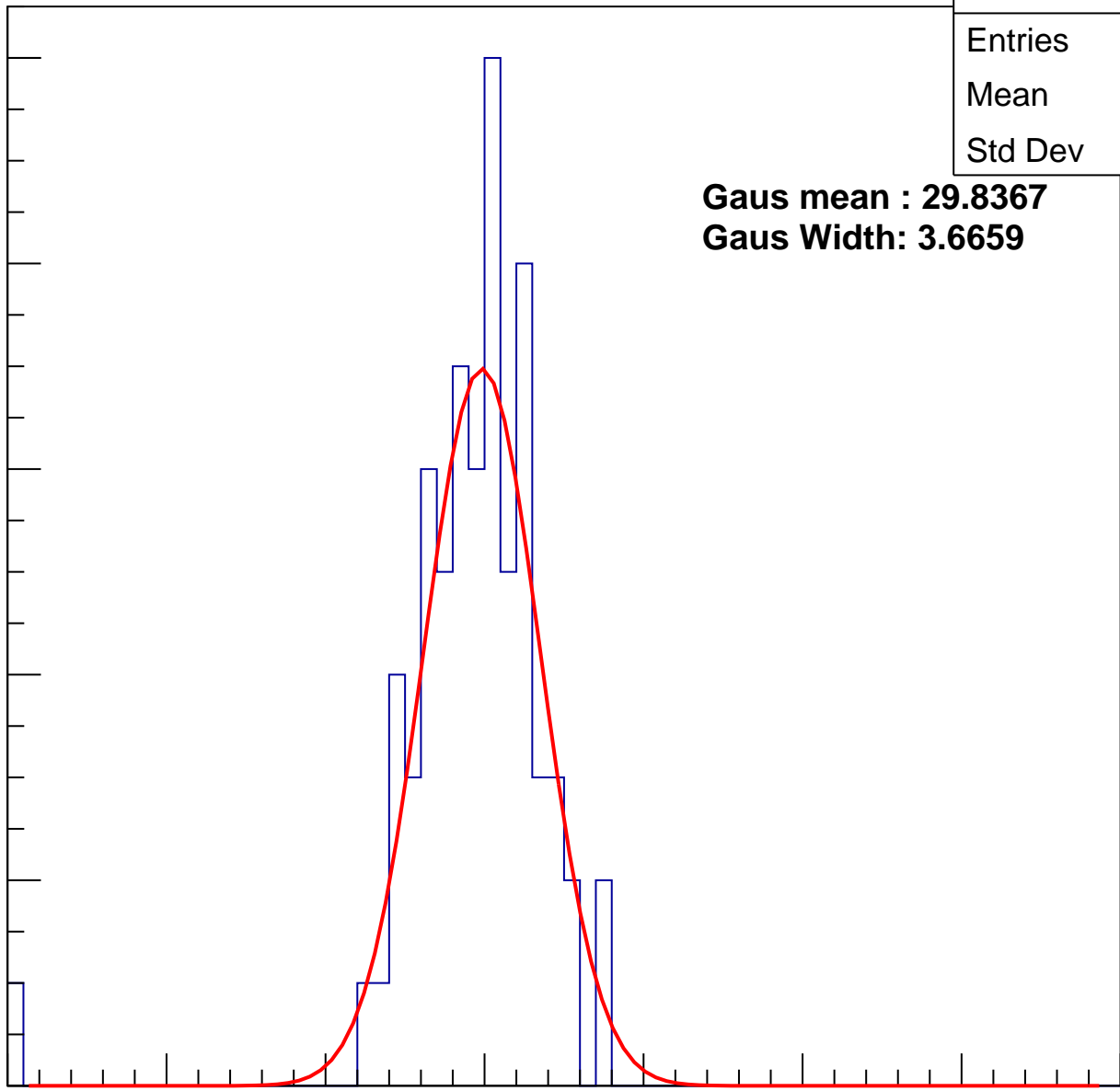
**Gaus Width: 3.6659**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U9-ch26, adc1

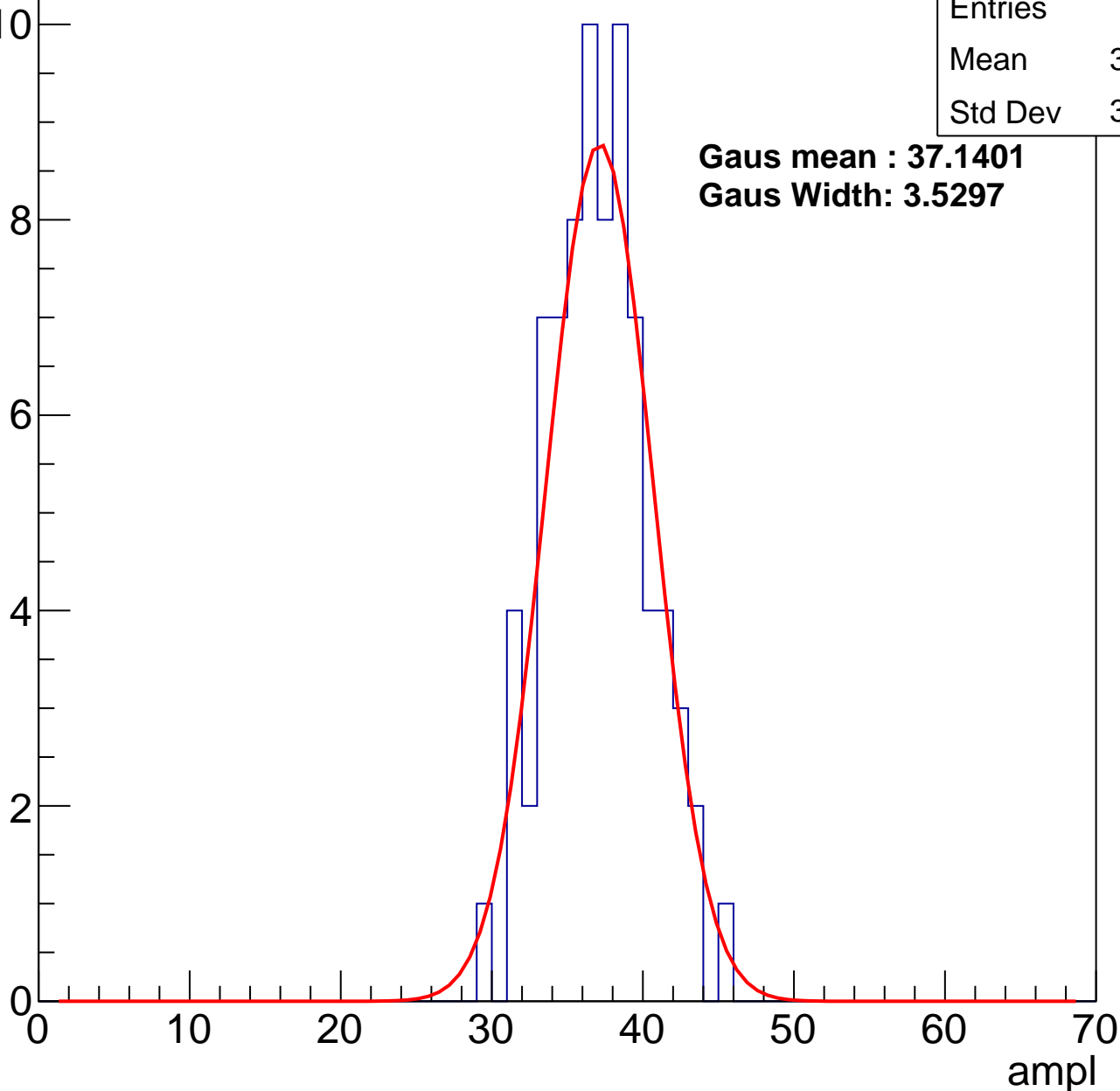
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	36.62
Std Dev	3.227

**Gaus mean : 37.1401**

**Gaus Width: 3.5297**



# B1L101S, U9-ch26, adc2

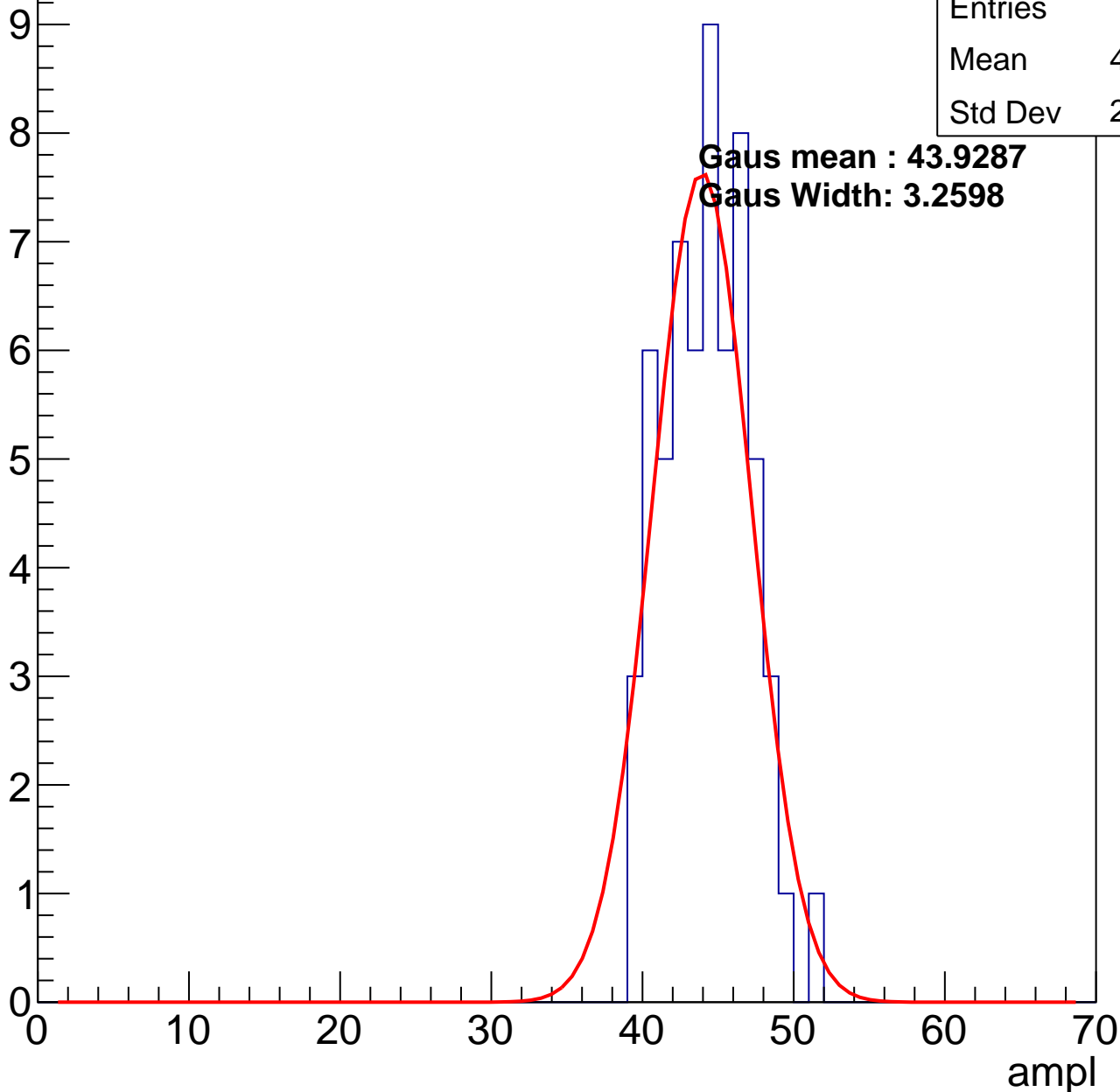
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	43.78
Std Dev	2.745

**Gaus mean : 43.9287**

**Gaus Width: 3.2598**

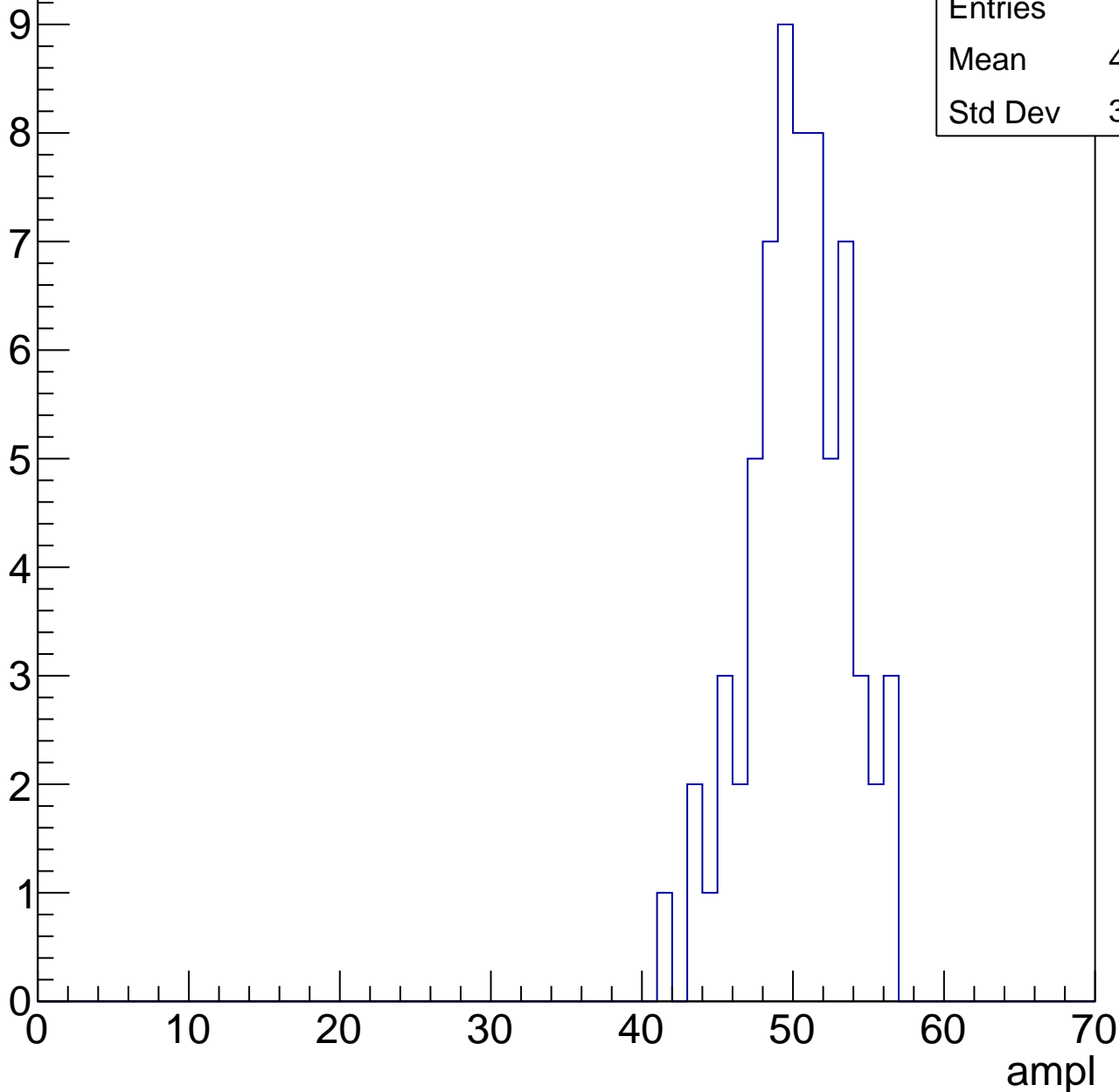


# B1L101S, U9-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

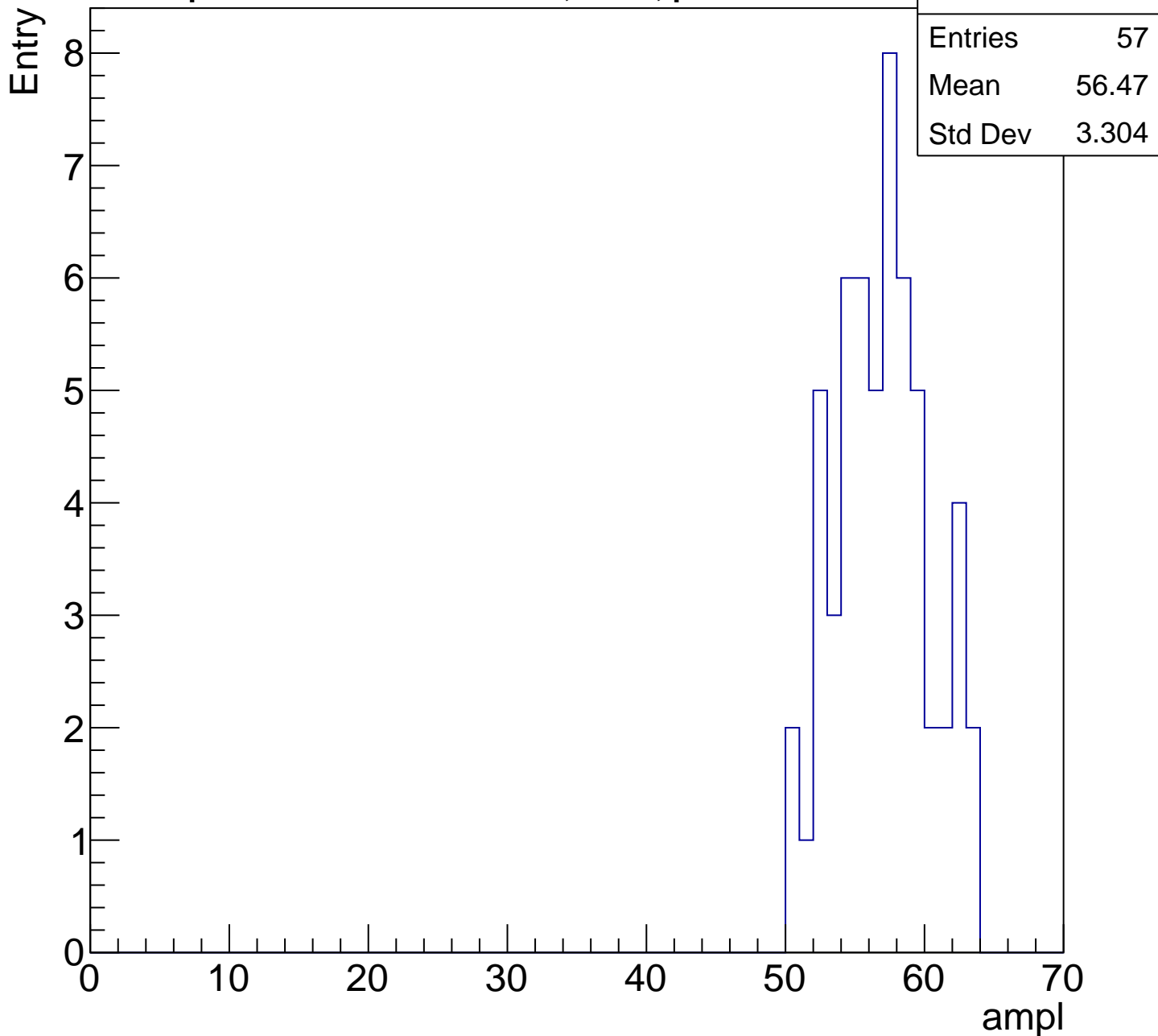
Entry

Entries	66
Mean	49.83
Std Dev	3.255



# B1L101S, U9-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

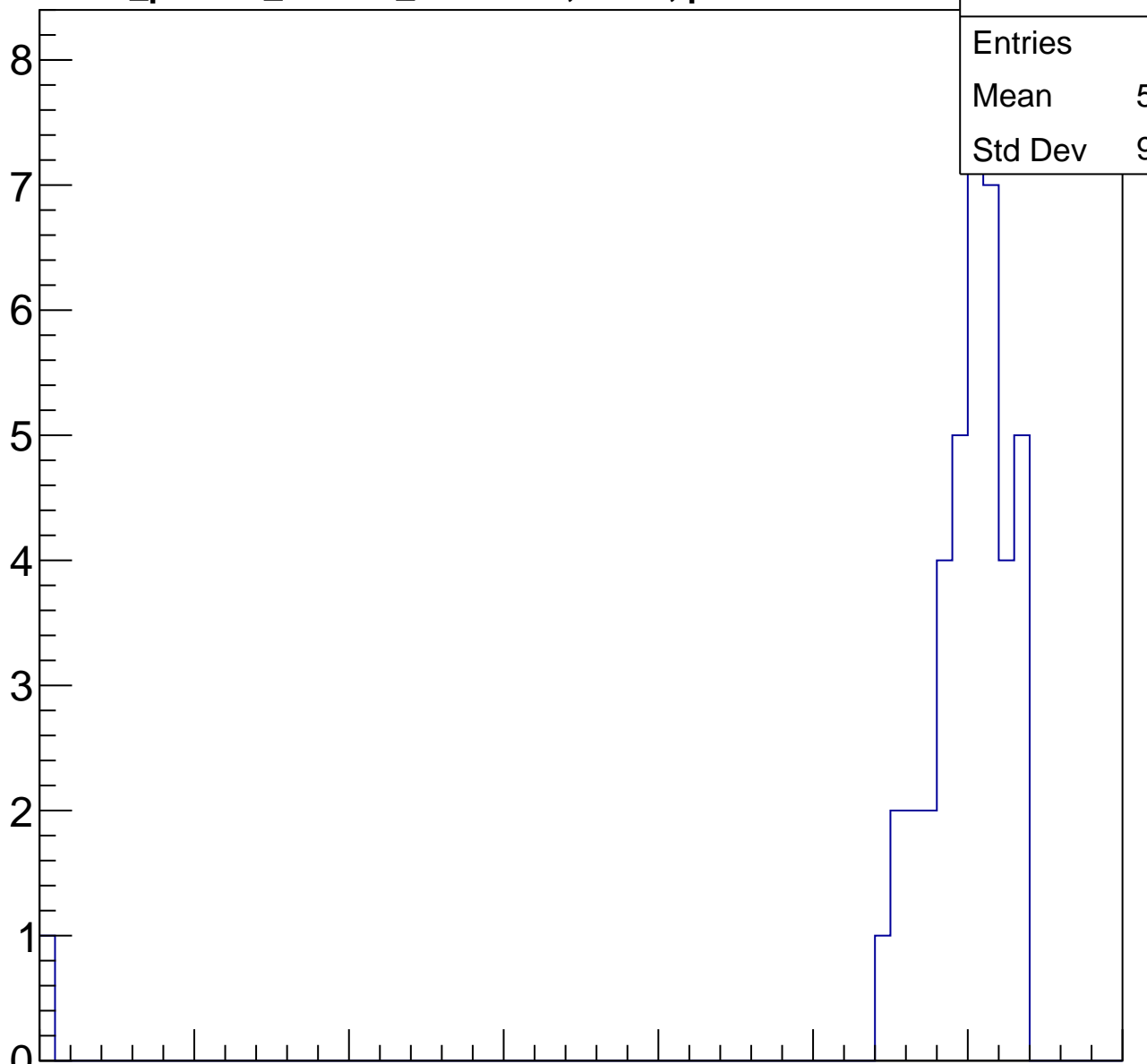
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	41
Mean	58.22
Std Dev	9.493

ampl

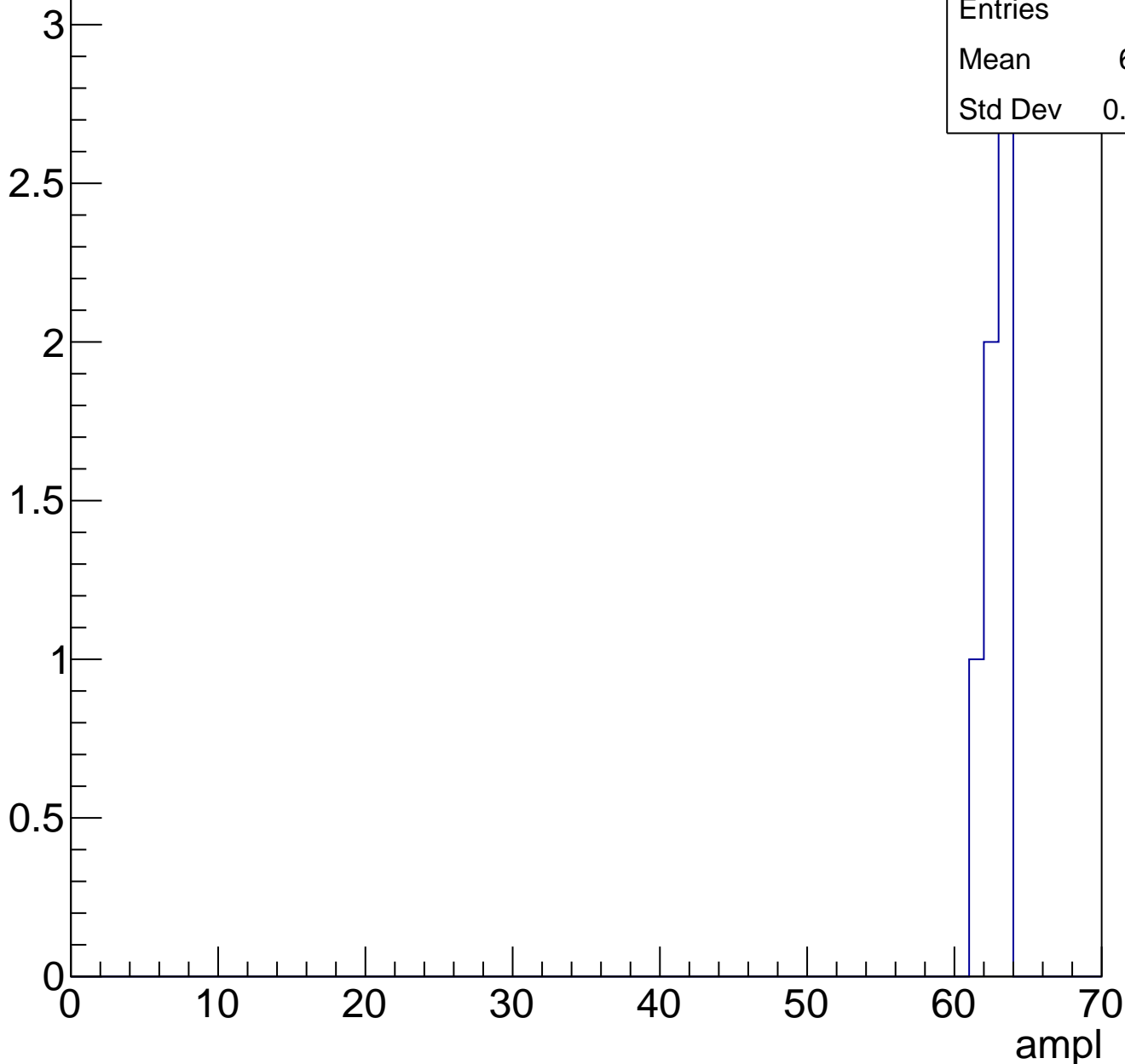
0 10 20 30 40 50 60 70



# B1L101S, U9-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U9-ch27, adc0

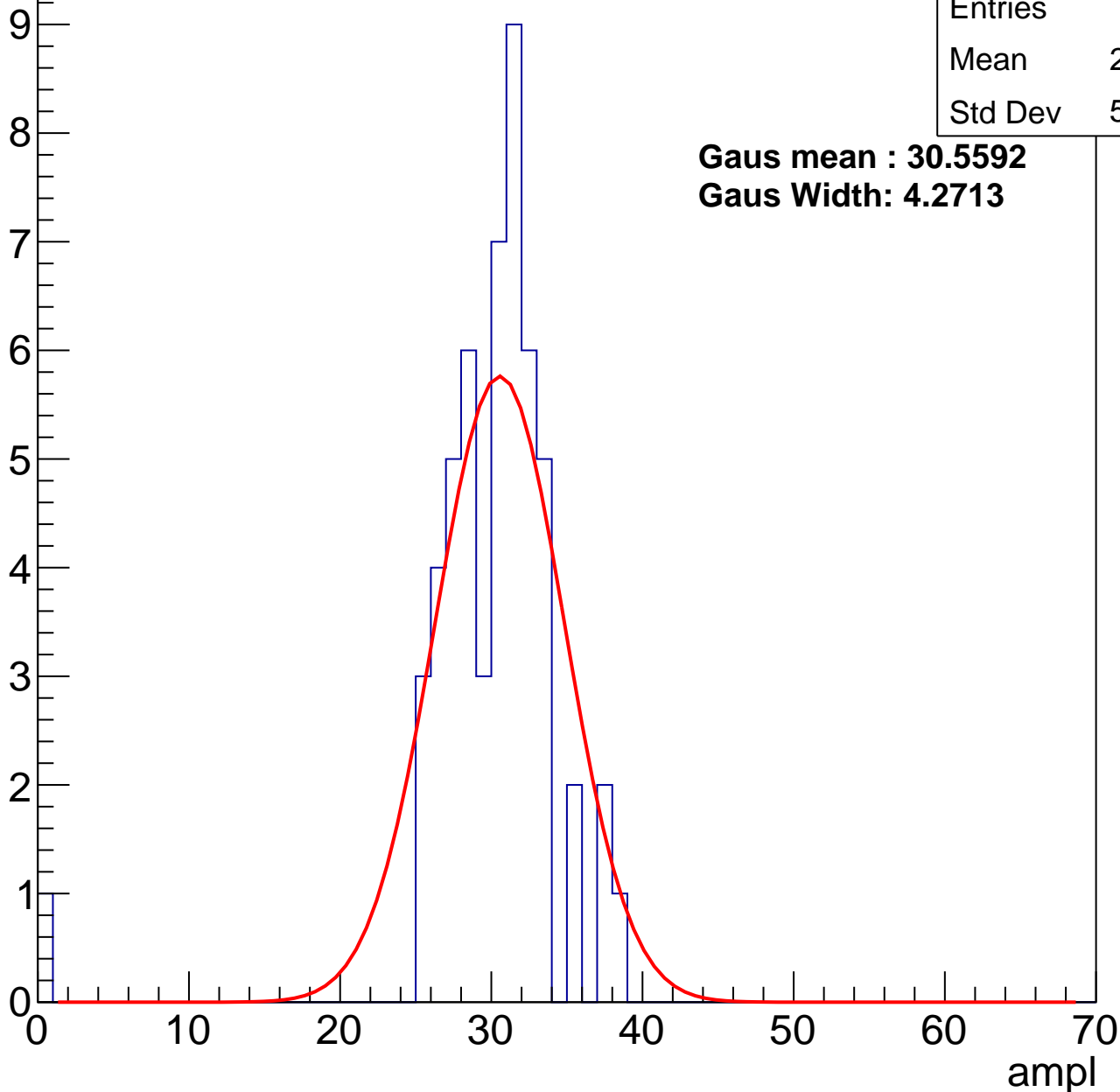
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	29.57
Std Dev	5.076

**Gaus mean : 30.5592**

**Gaus Width: 4.2713**



# B1L101S, U9-ch27, adc1

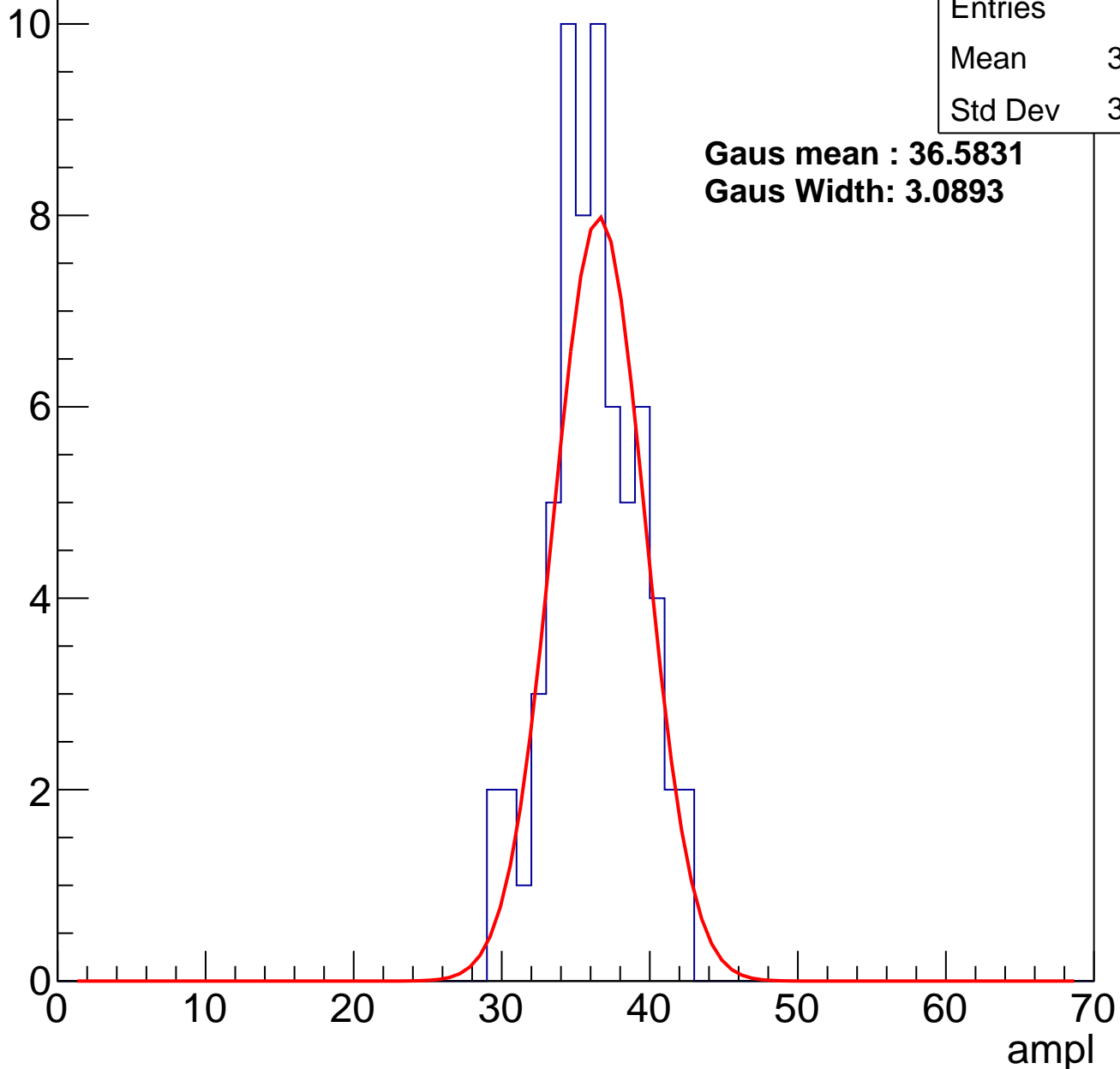
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	66
Mean	35.79
Std Dev	3.013

**Gaus mean : 36.5831**

**Gaus Width: 3.0893**

Entry



# B1L101S, U9-ch27, adc2

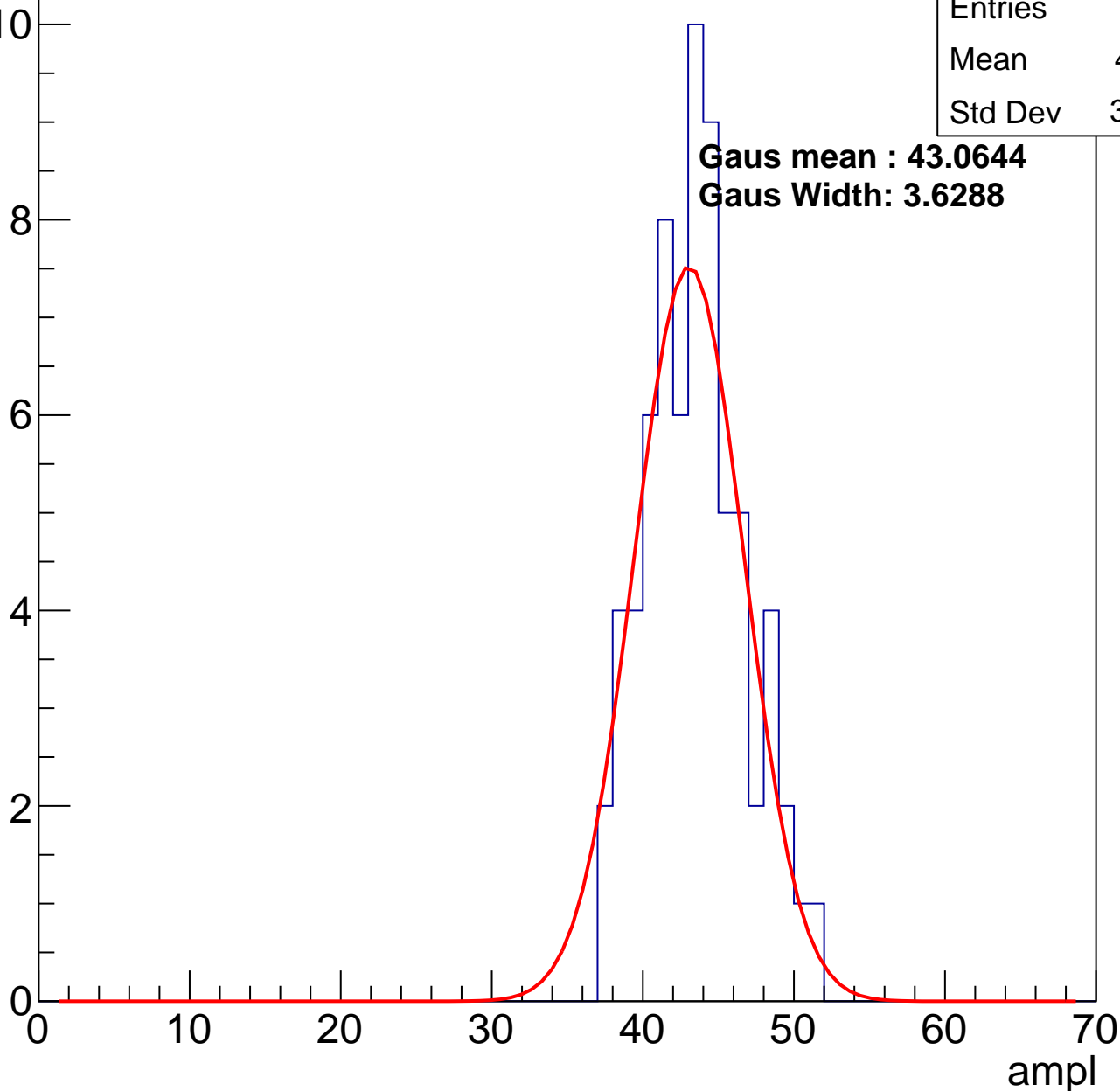
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	43.01
Std Dev	3.228

**Gaus mean : 43.0644**

**Gaus Width: 3.6288**

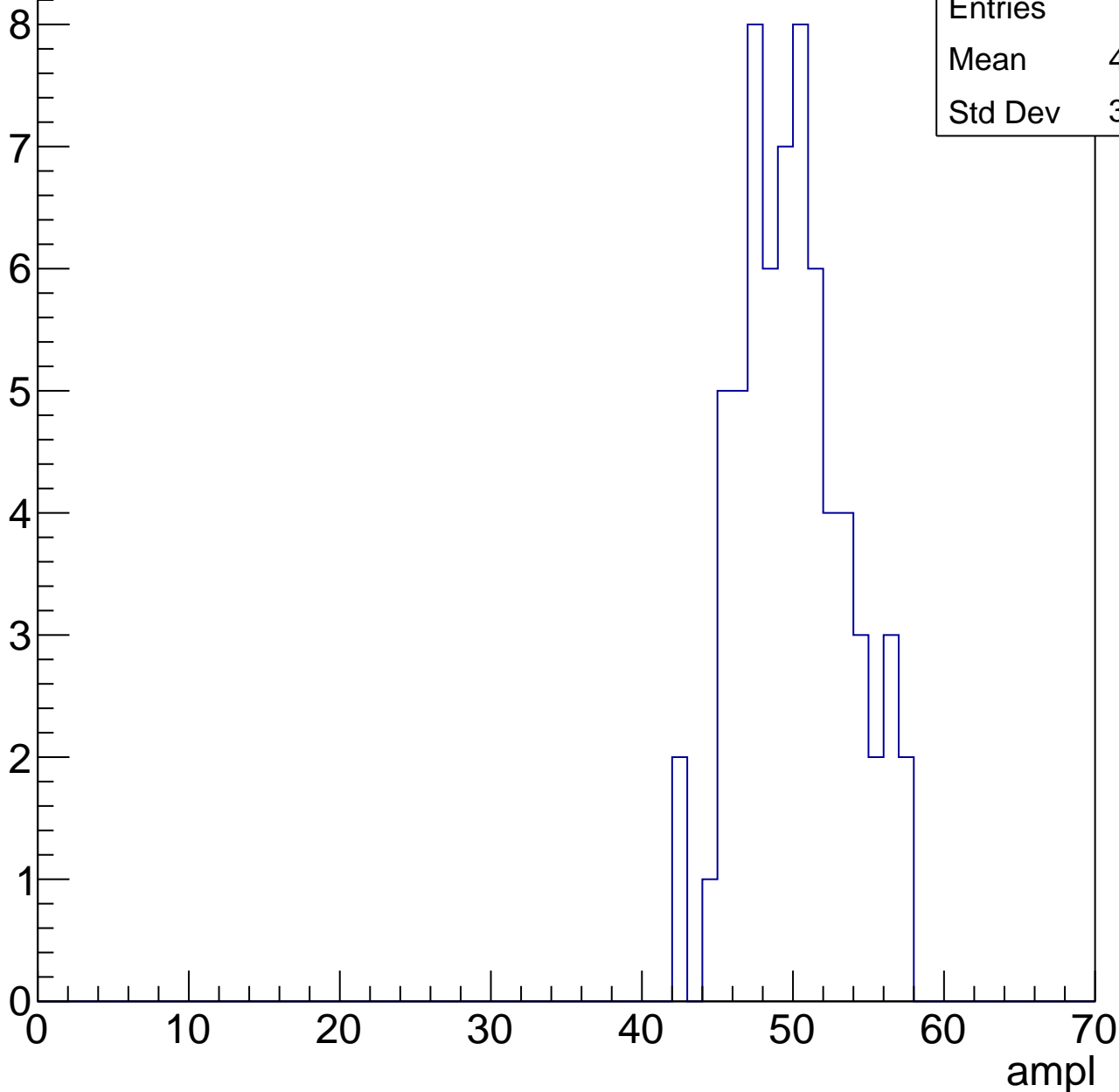


# B1L101S, U9-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

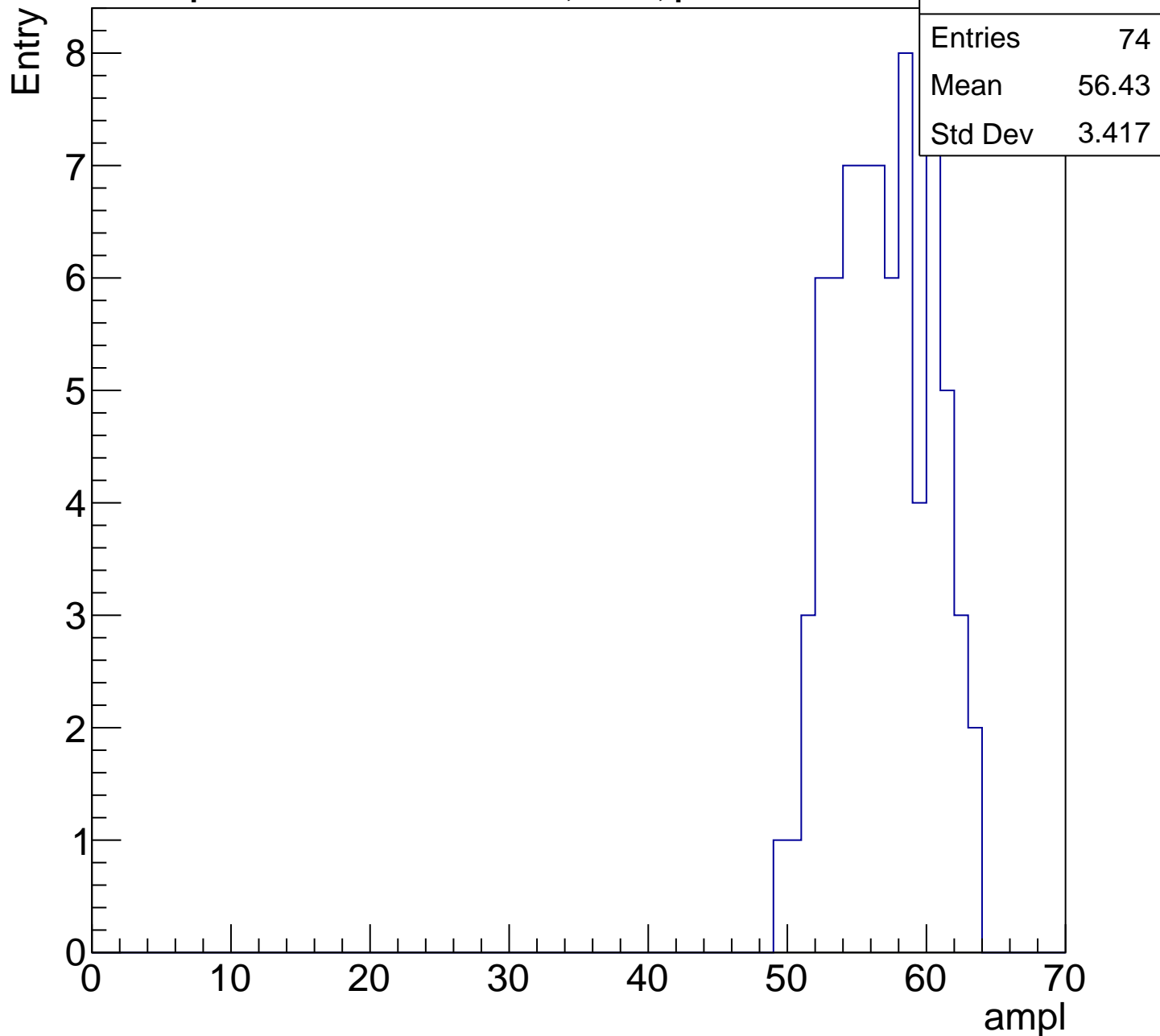
Entry

Entries	66
Mean	49.55
Std Dev	3.526



# B1L101S, U9-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

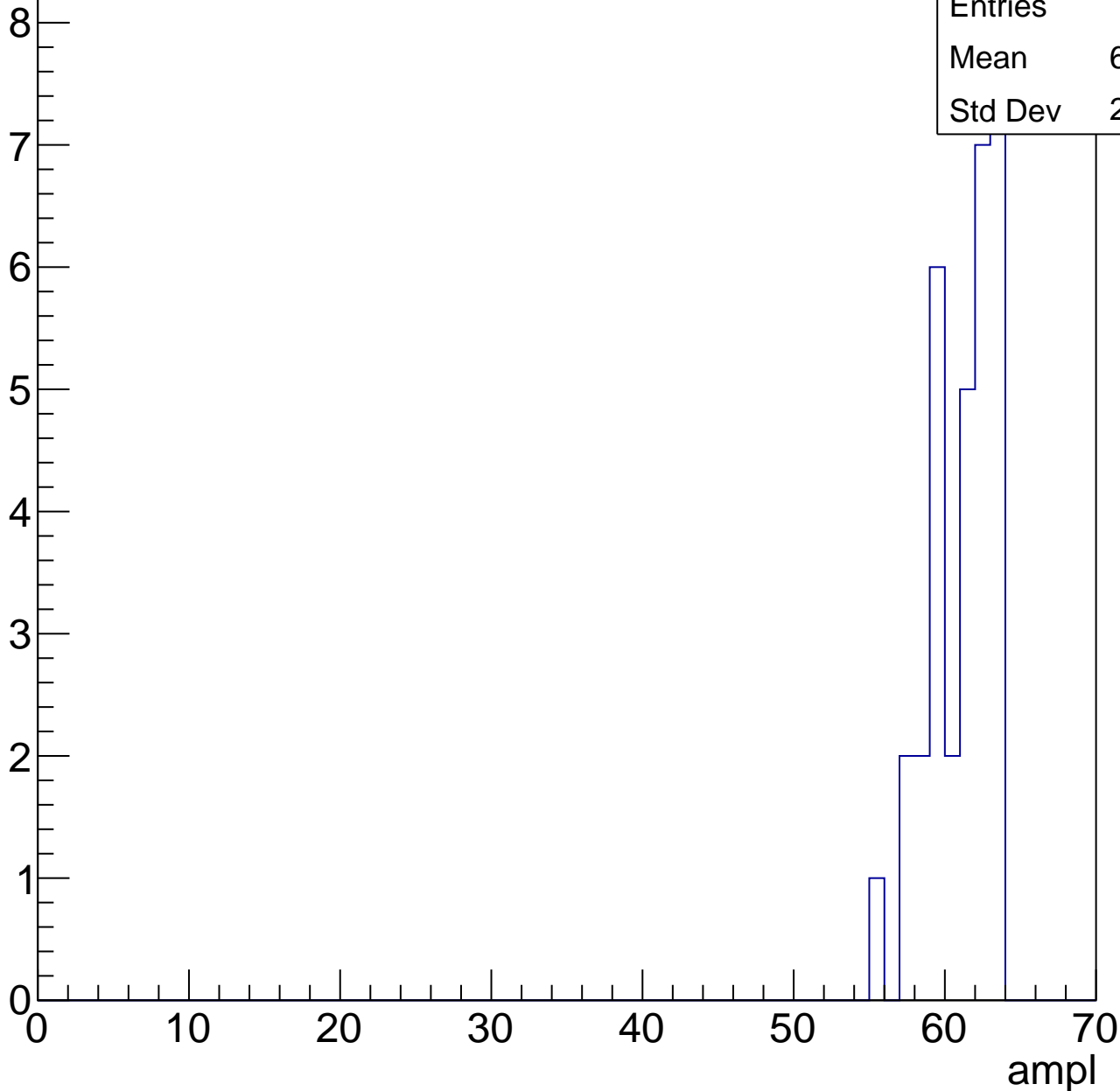


# B1L101S, U9-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

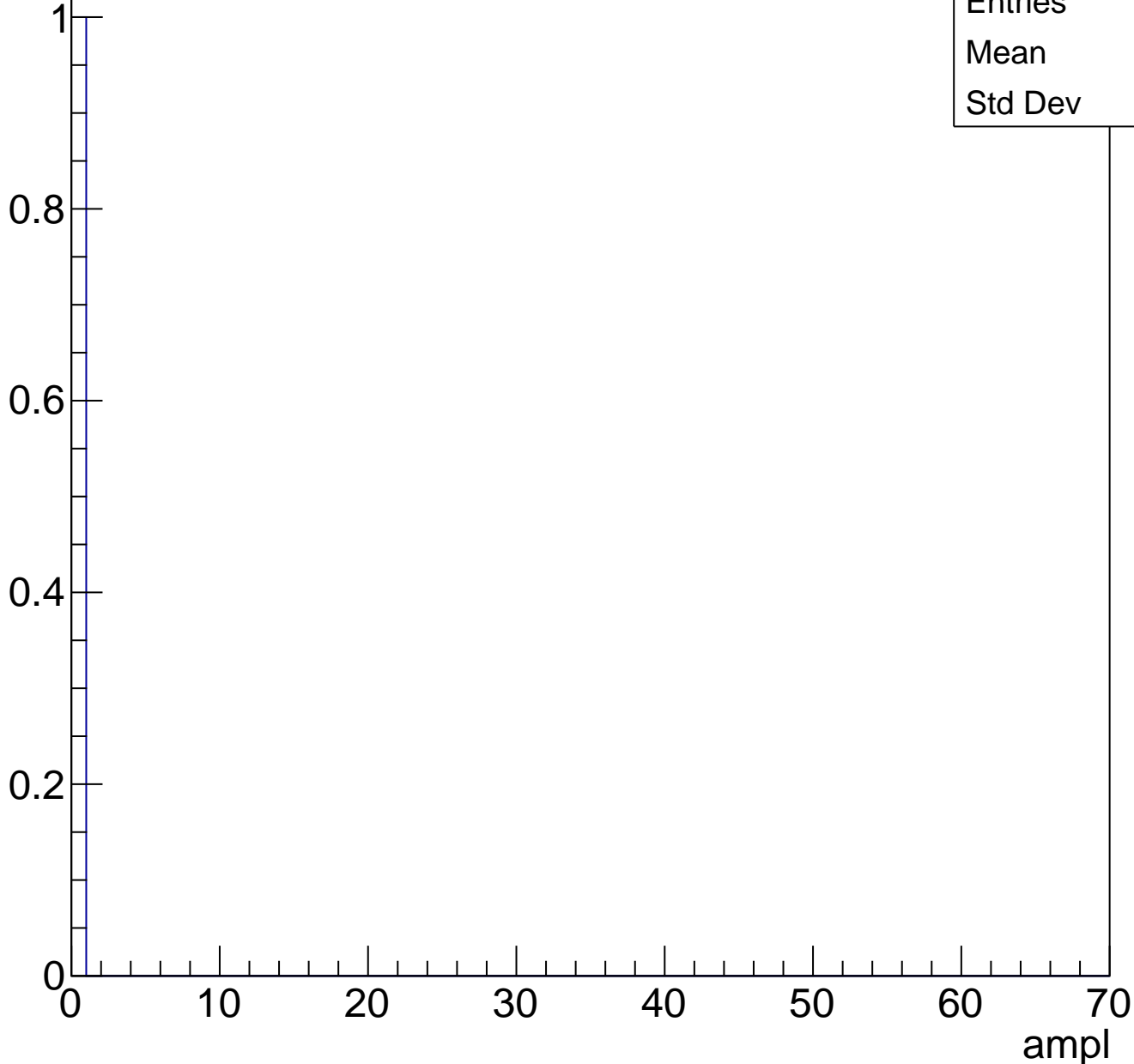
Entries	33
Mean	60.67
Std Dev	2.113



# B1L101S, U9-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	12.5
Std Dev	12.5

# B1L101S, U9-ch28, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	69
Mean	29.36
Std Dev	3.707

**Gaus mean : 29.9873**

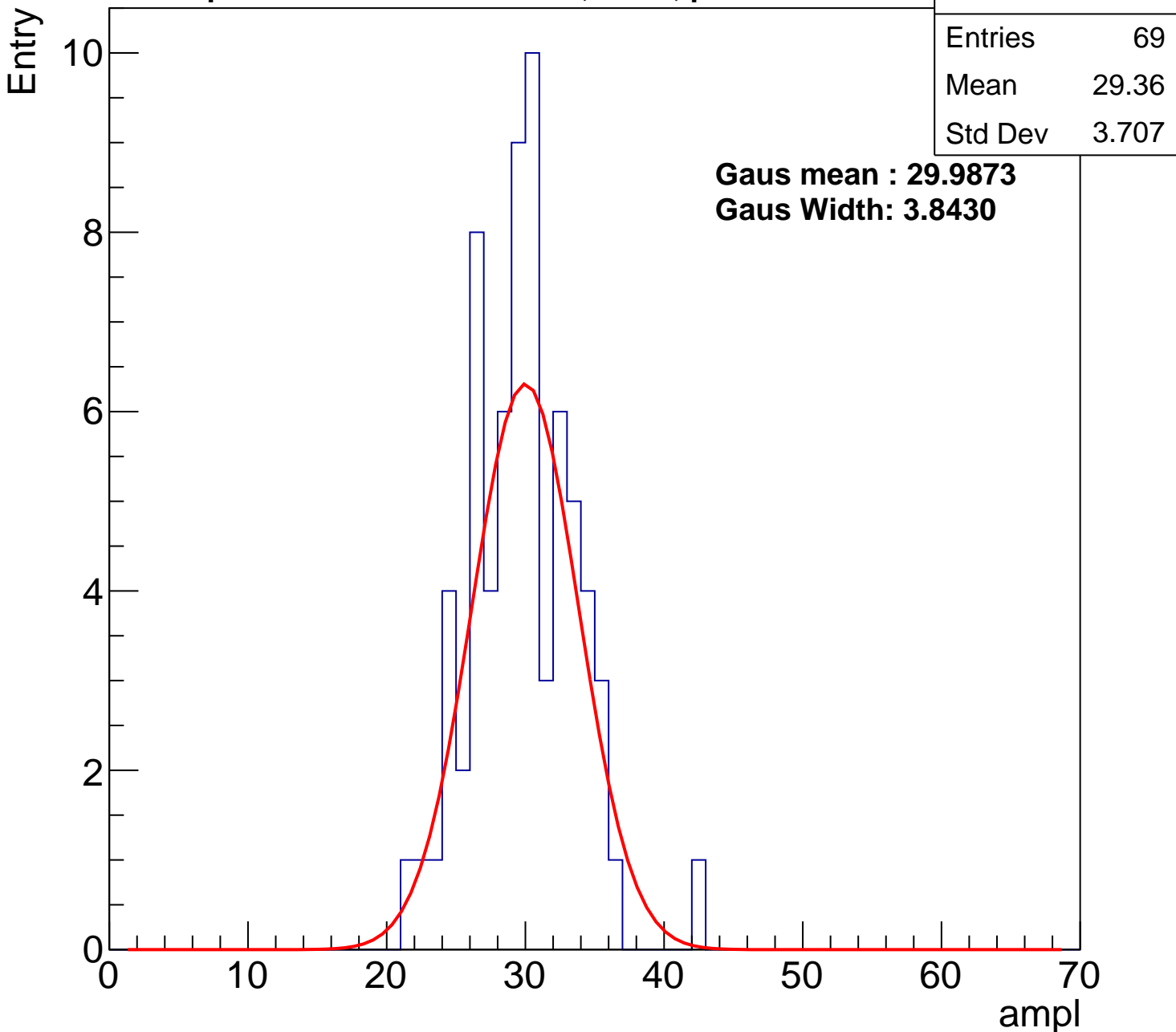
**Gaus Width: 3.8430**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U9-ch28, adc1

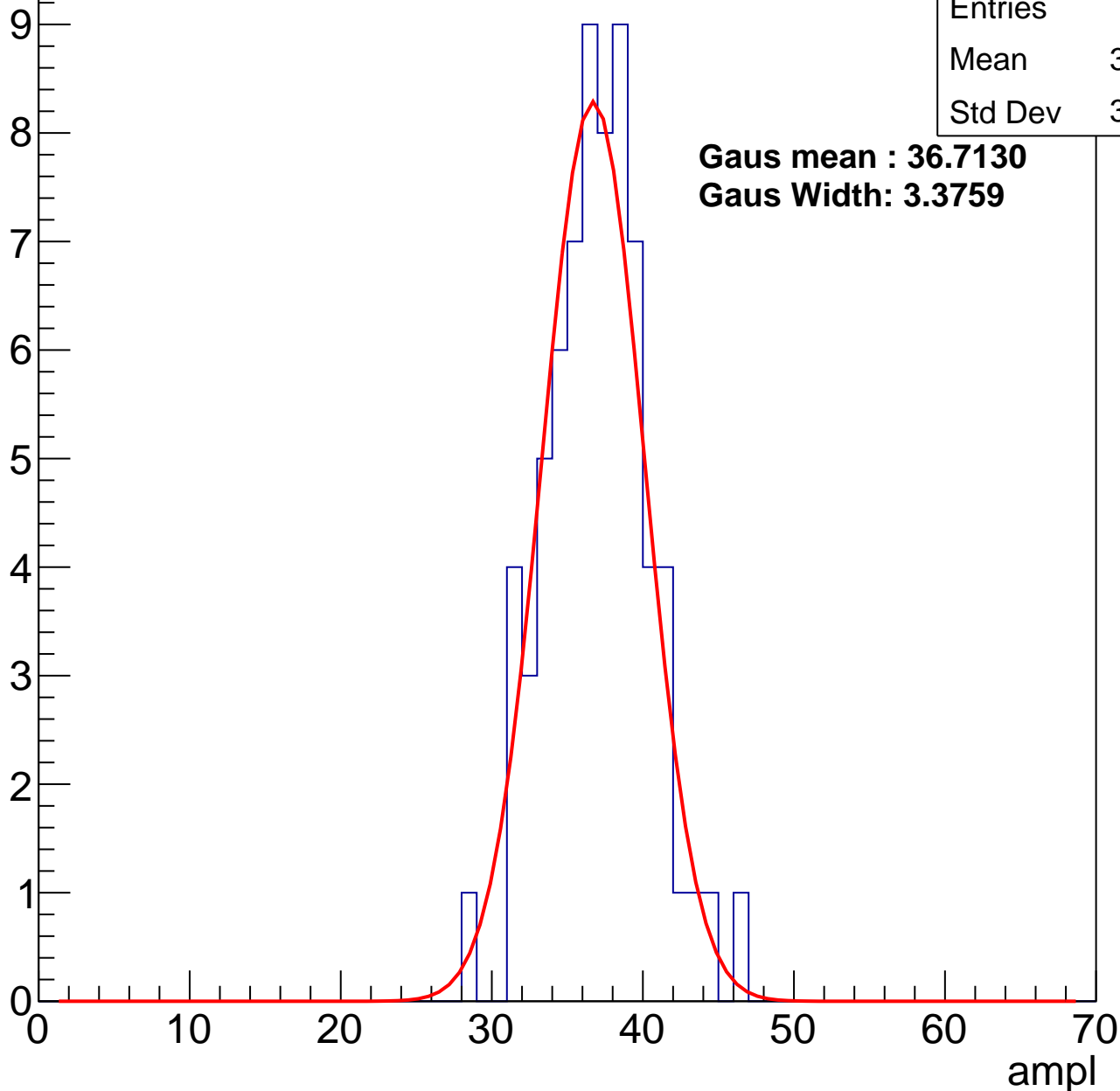
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	36.56
Std Dev	3.326

**Gaus mean : 36.7130**

**Gaus Width: 3.3759**



# B1L101S, U9-ch28, adc2

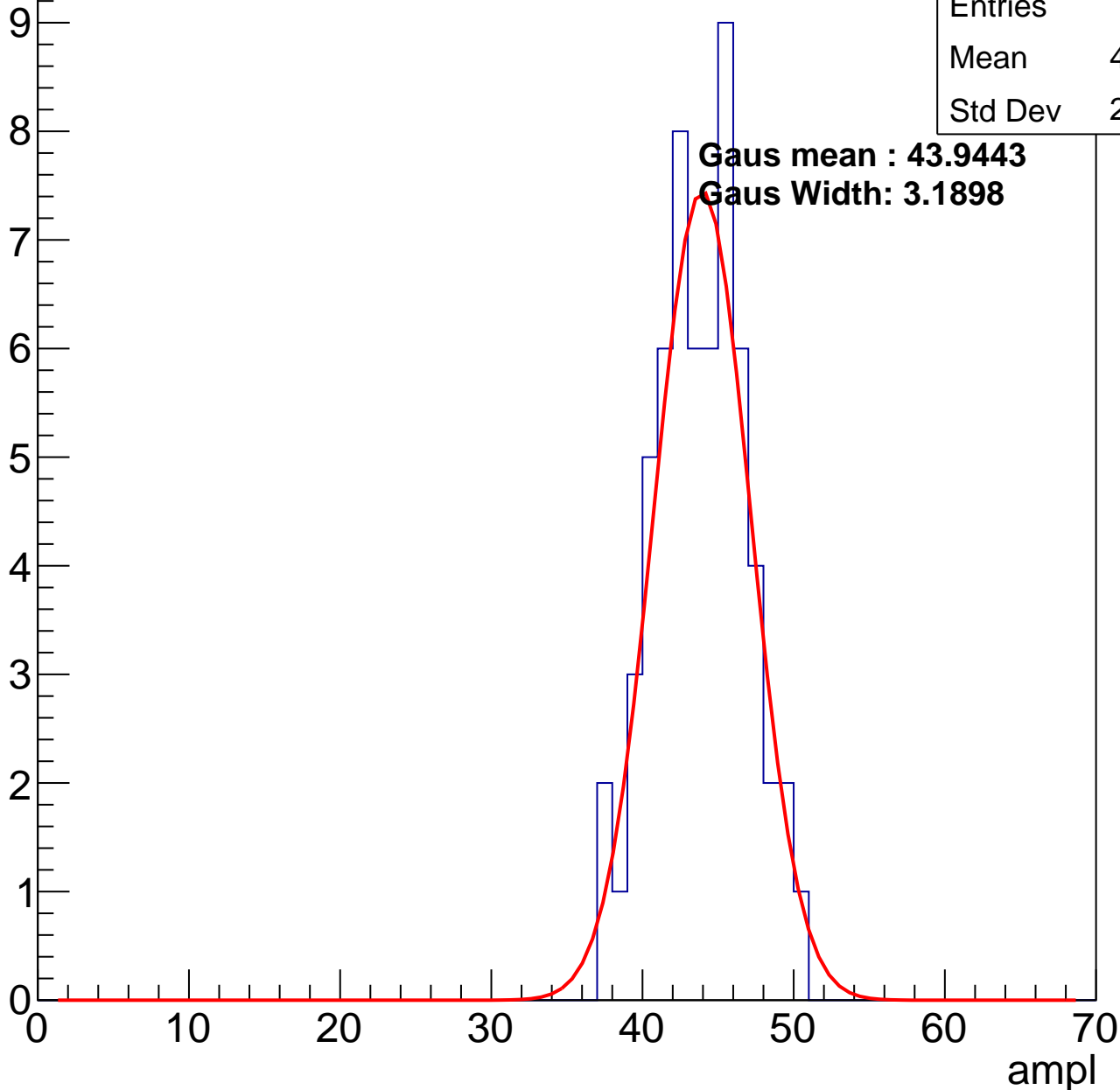
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	43.38
Std Dev	2.987

**Gaus mean : 43.9443**

**Gaus Width: 3.1898**

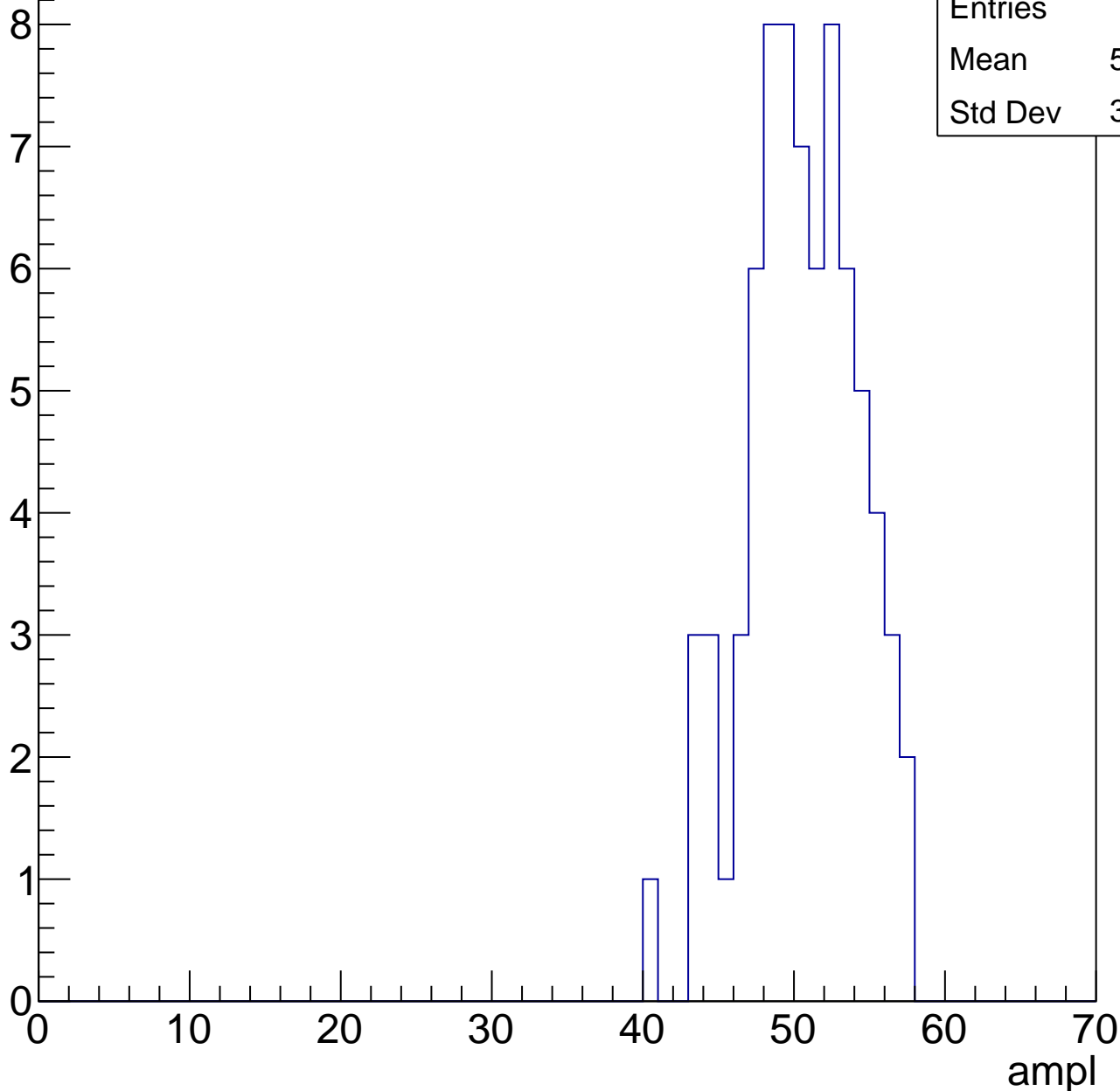


# B1L101S, U9-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	50.05
Std Dev	3.676

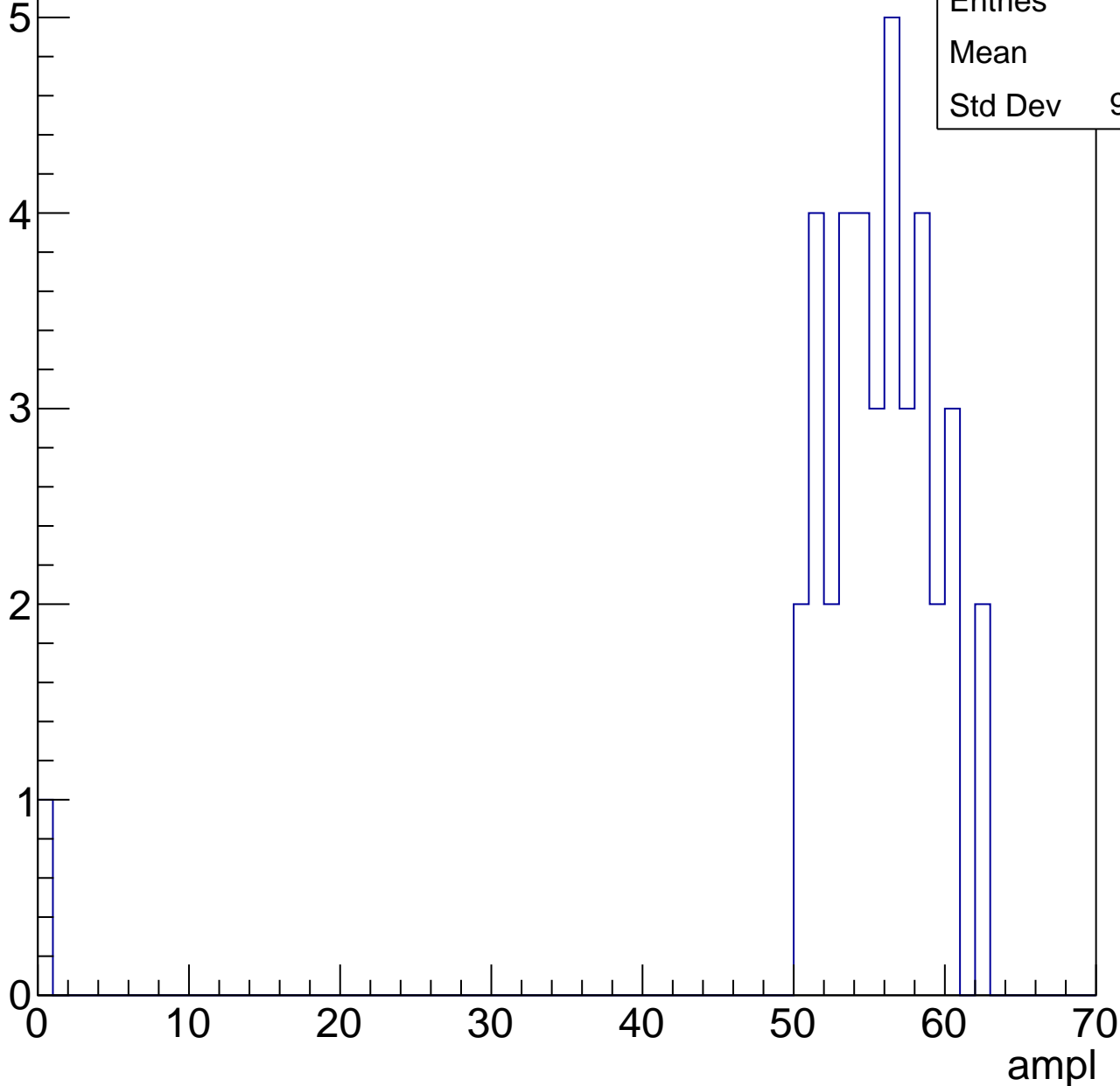


# B1L101S, U9-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

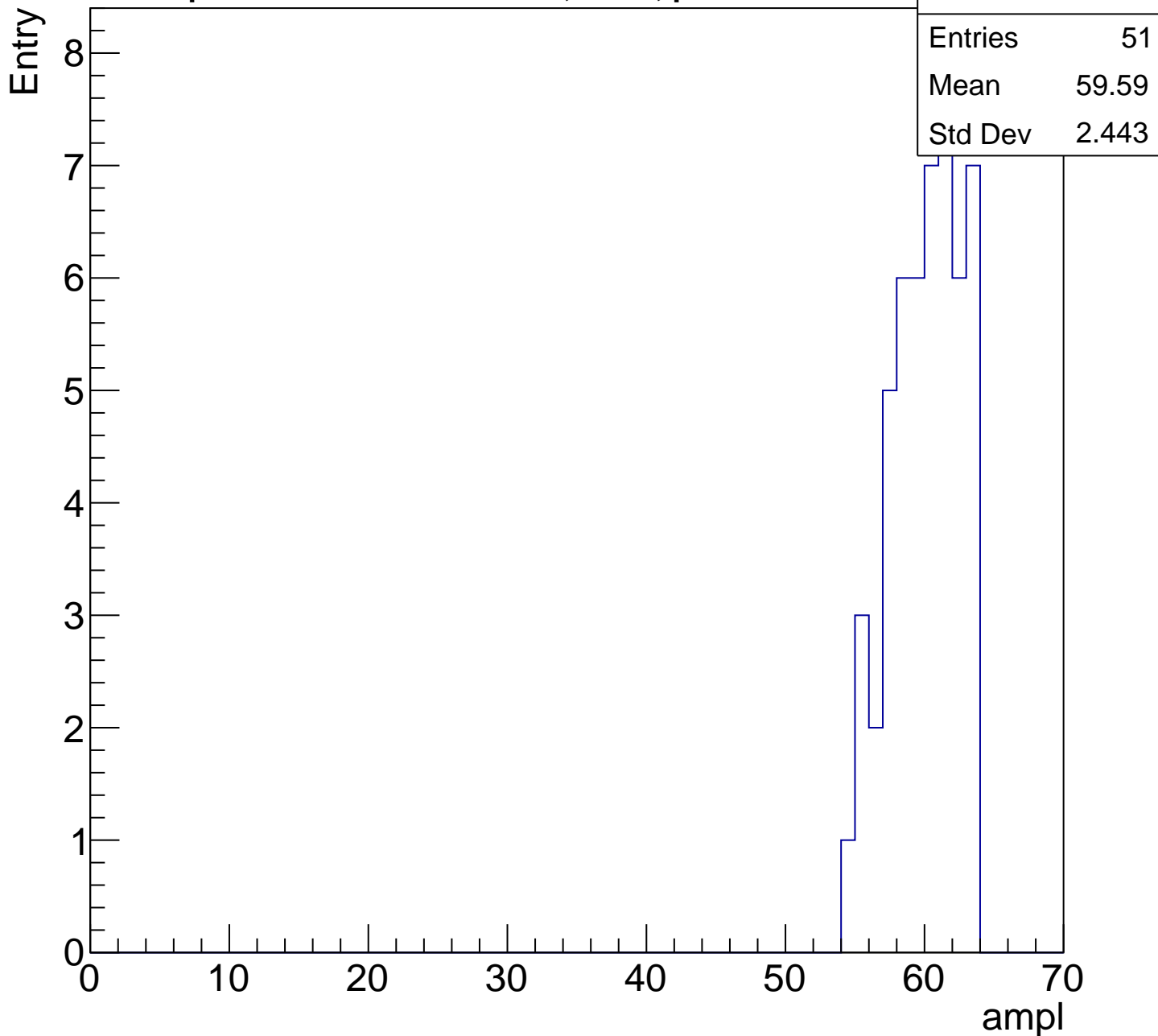
Entry

Entries	39
Mean	54
Std Dev	9.332



# B1L101S, U9-ch28, adc5

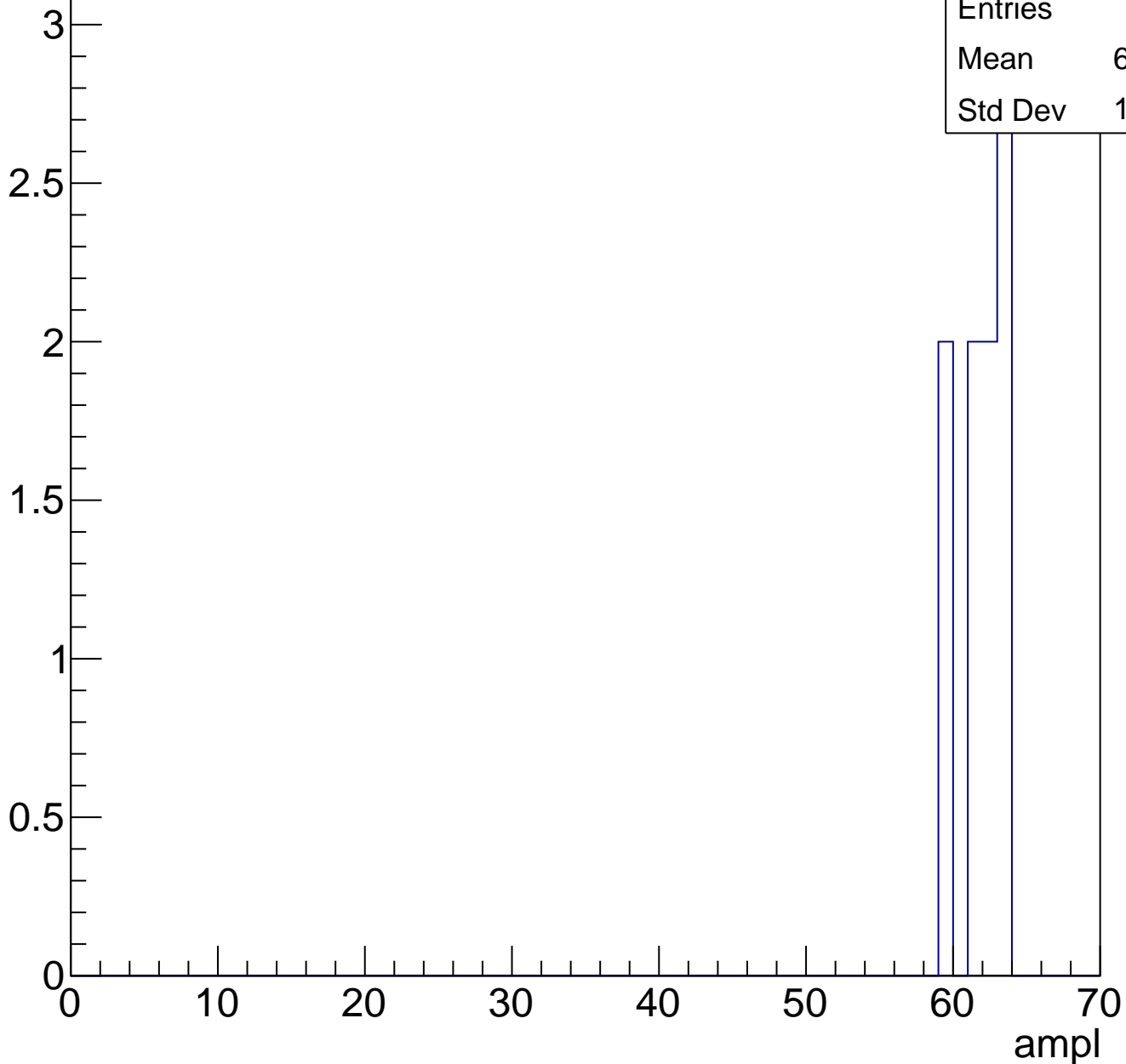
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	8.5
Std Dev	8.5

# B1L101S, U9-ch29, adc0

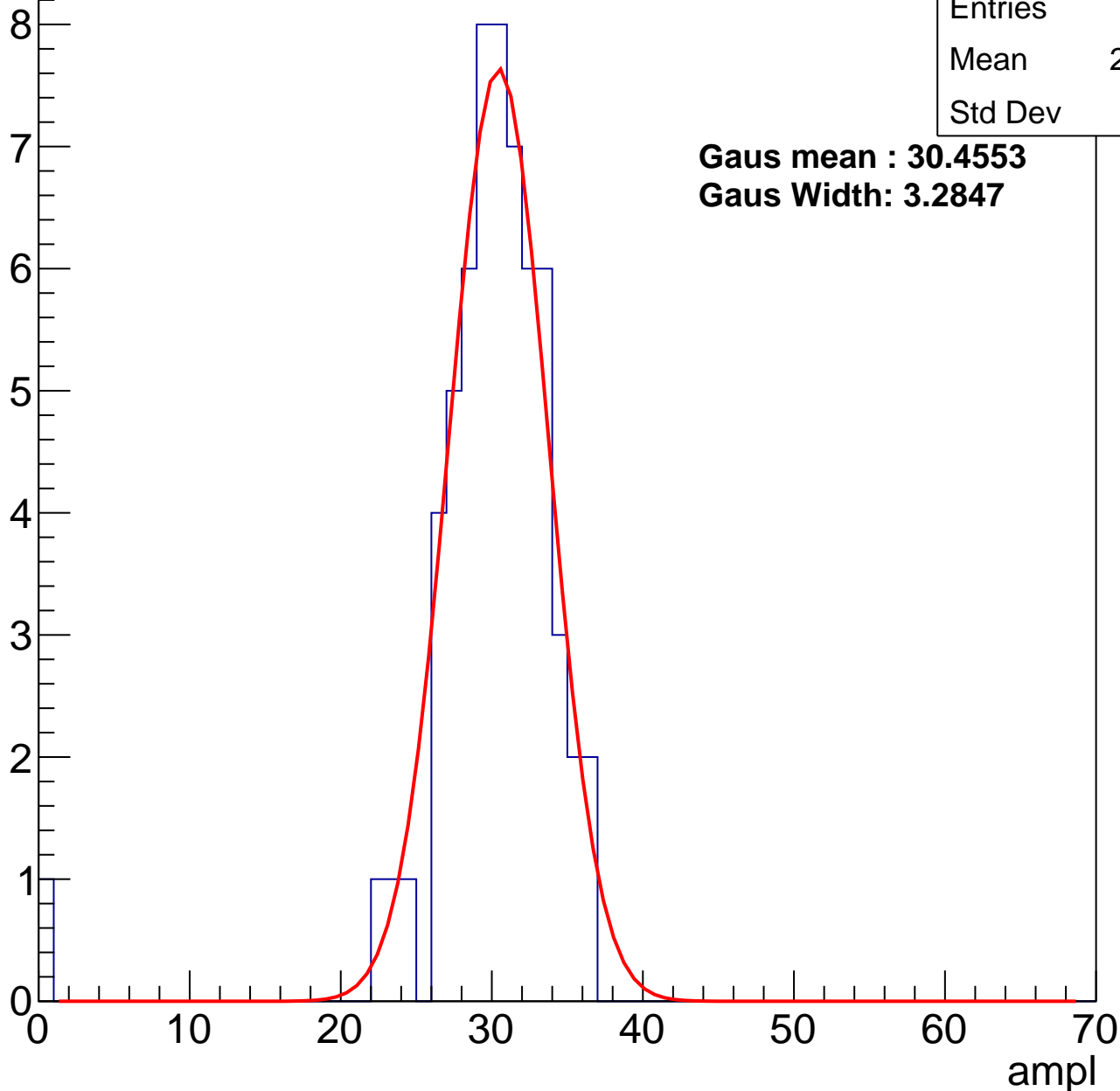
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	29.49
Std Dev	4.84

**Gaus mean : 30.4553**

**Gaus Width: 3.2847**



# B1L101S, U9-ch29, adc1

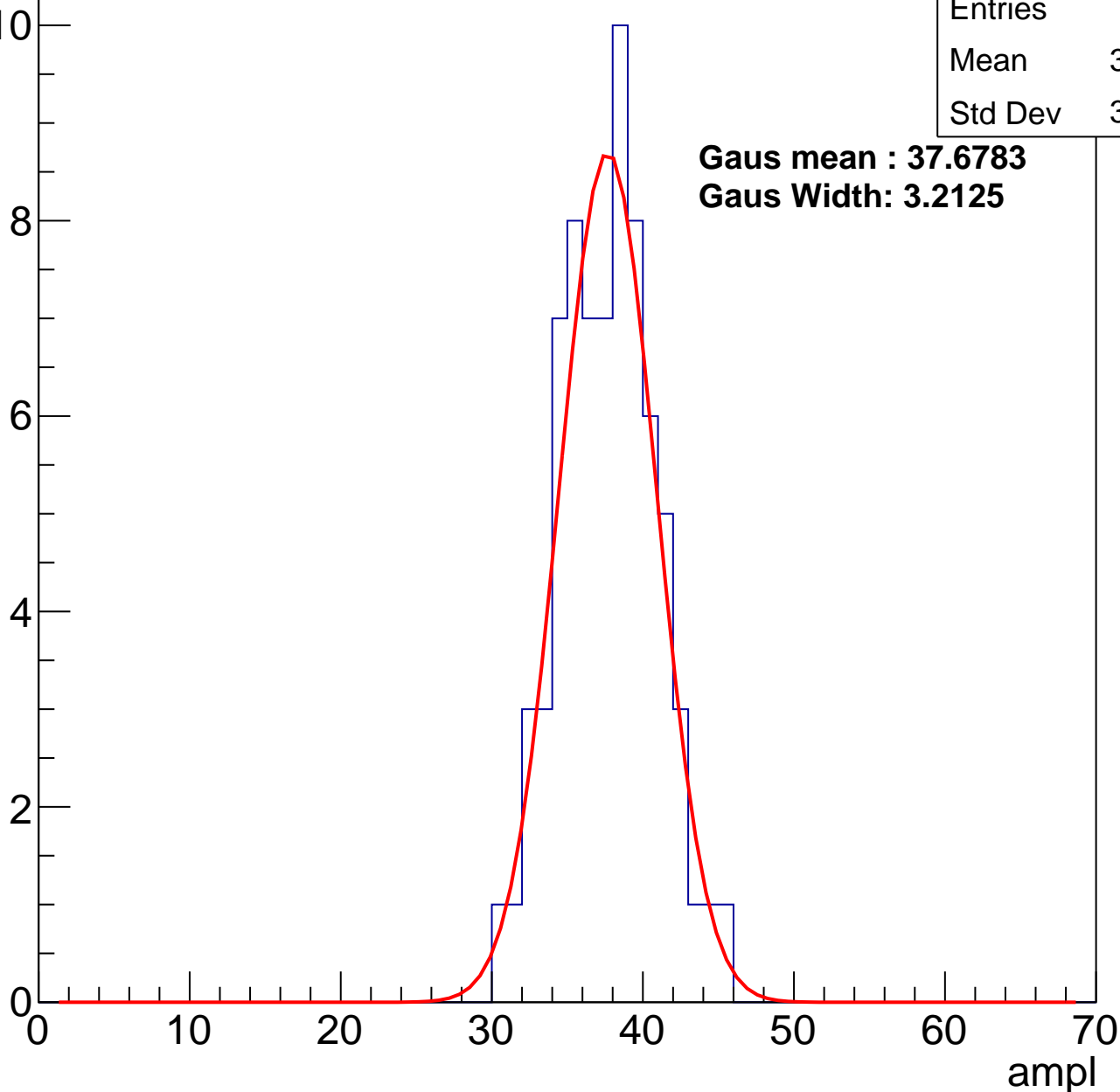
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	37.22
Std Dev	3.132

**Gaus mean : 37.6783**

**Gaus Width: 3.2125**



# B1L101S, U9-ch29, adc2

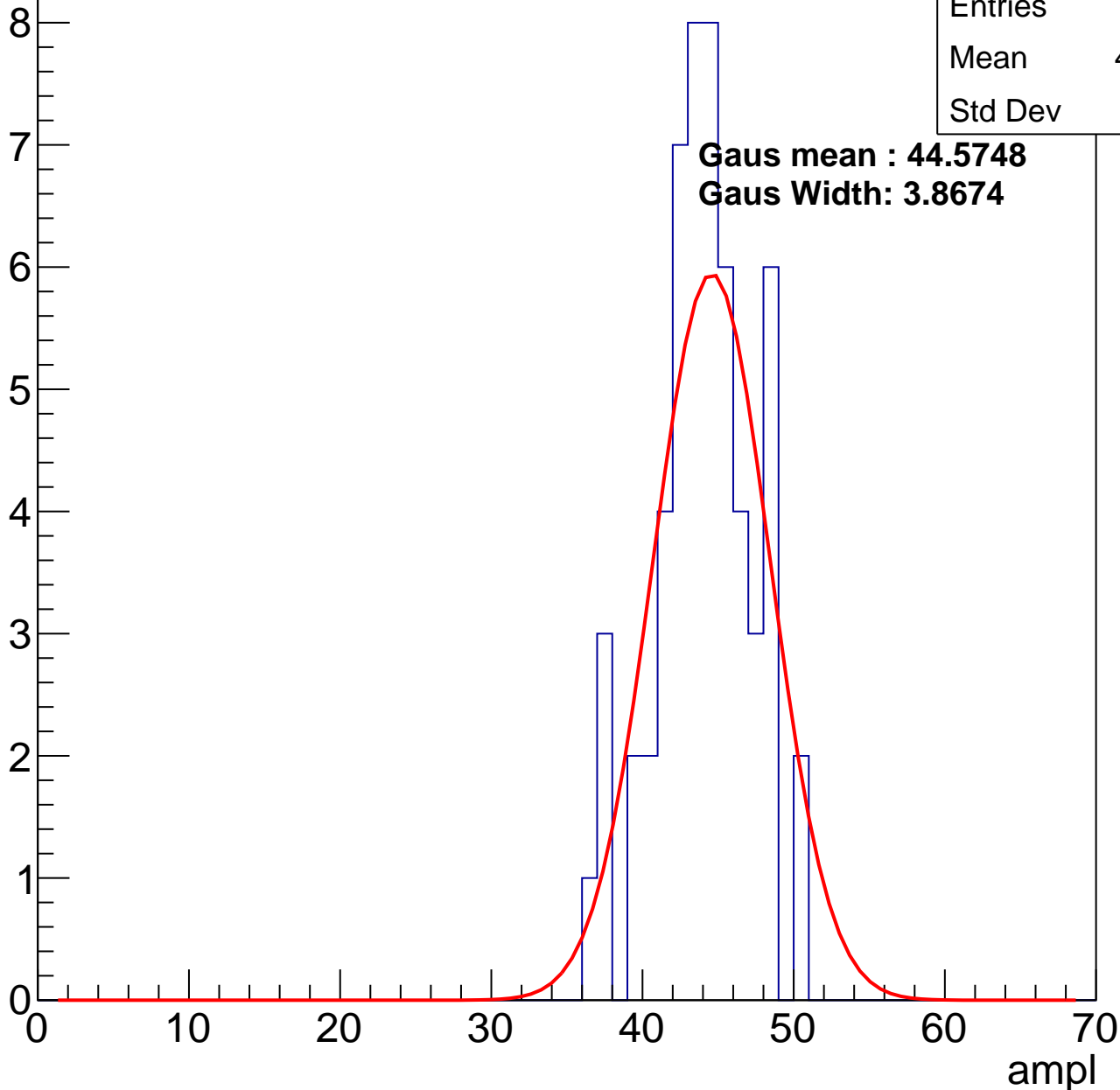
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	43.61
Std Dev	3.2

**Gaus mean : 44.5748**

**Gaus Width: 3.8674**



# B1L101S, U9-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

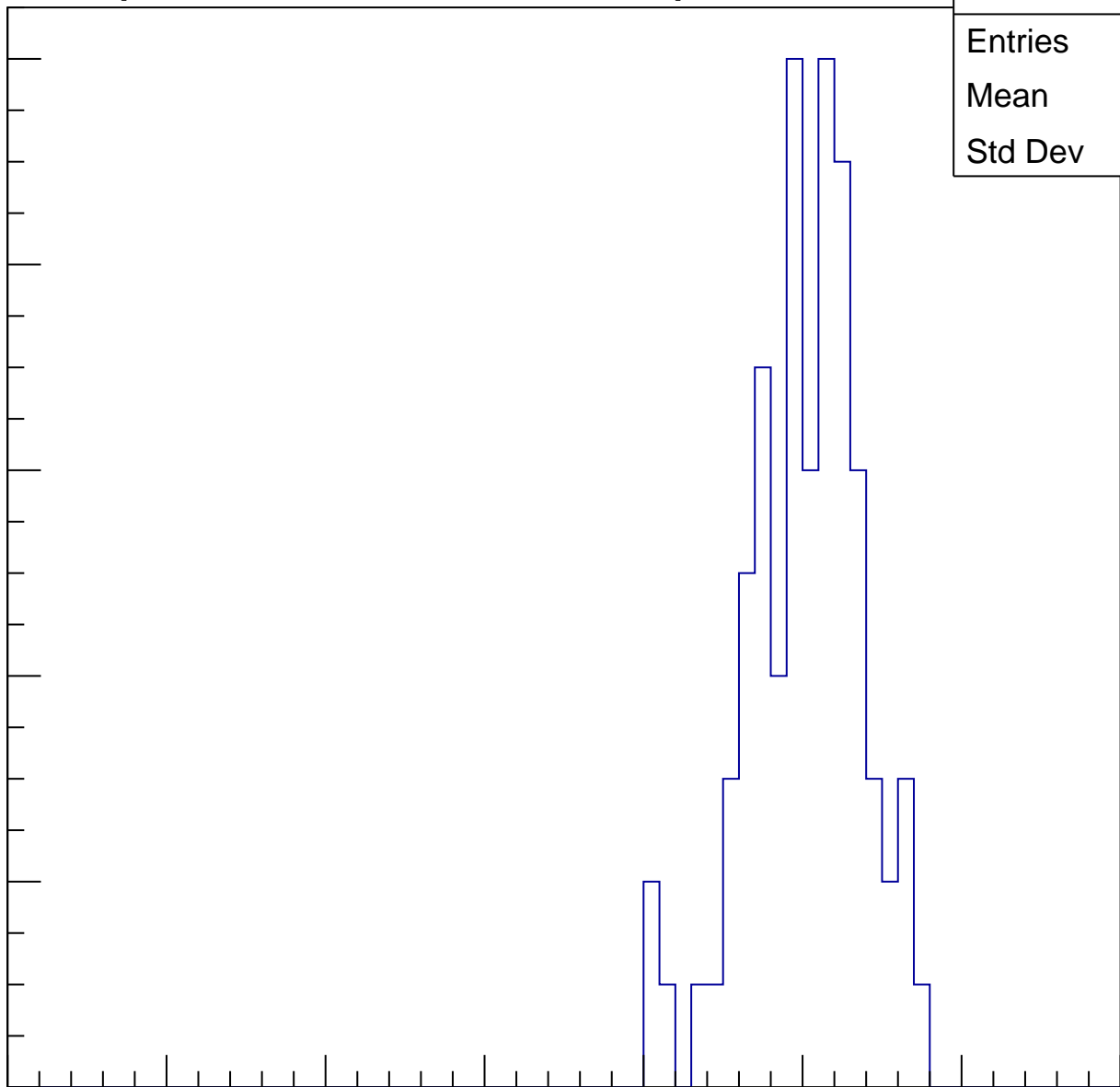
Entries	74
Mean	49.69
Std Dev	3.598

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

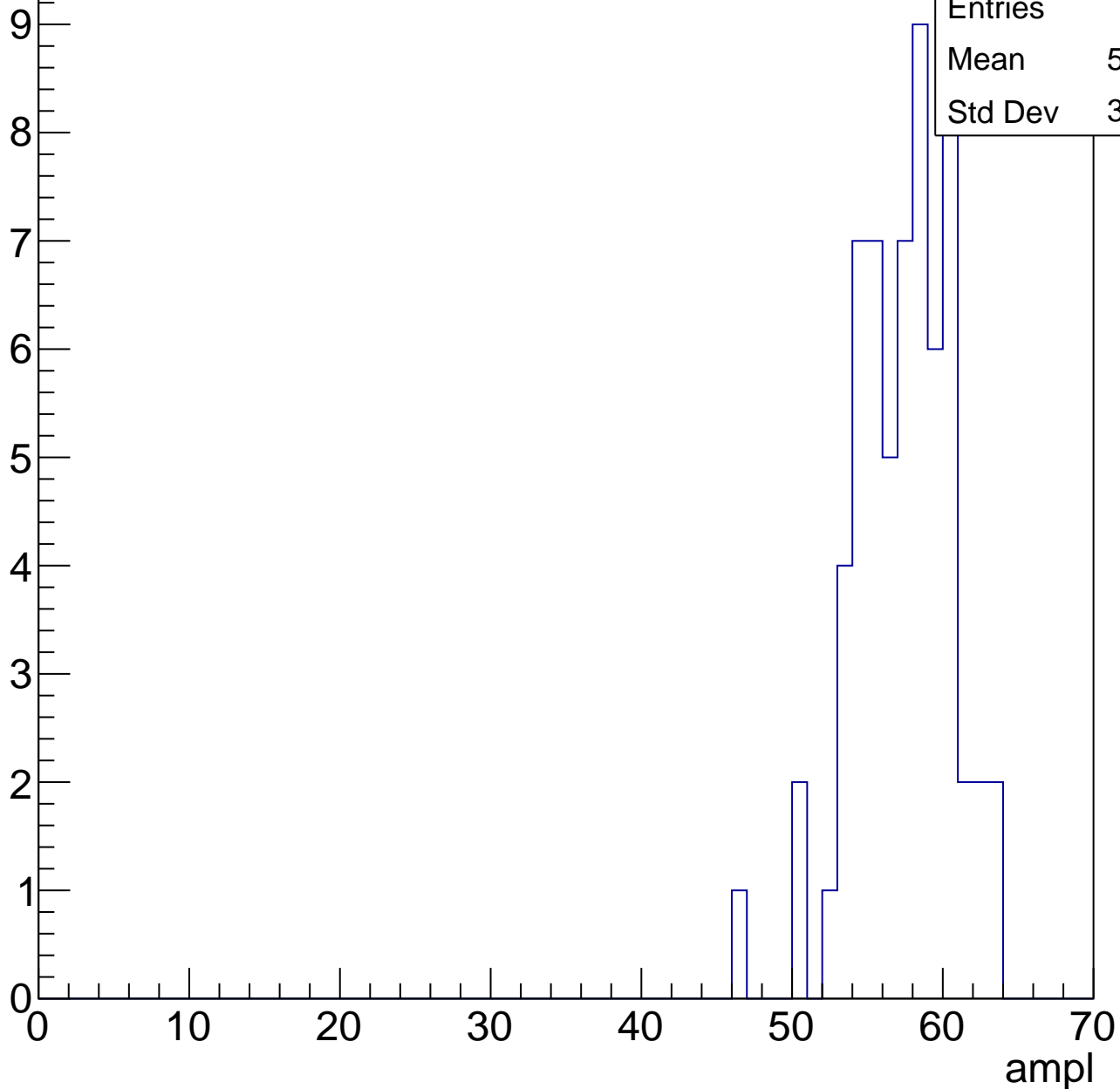
ampl



# B1L101S, U9-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

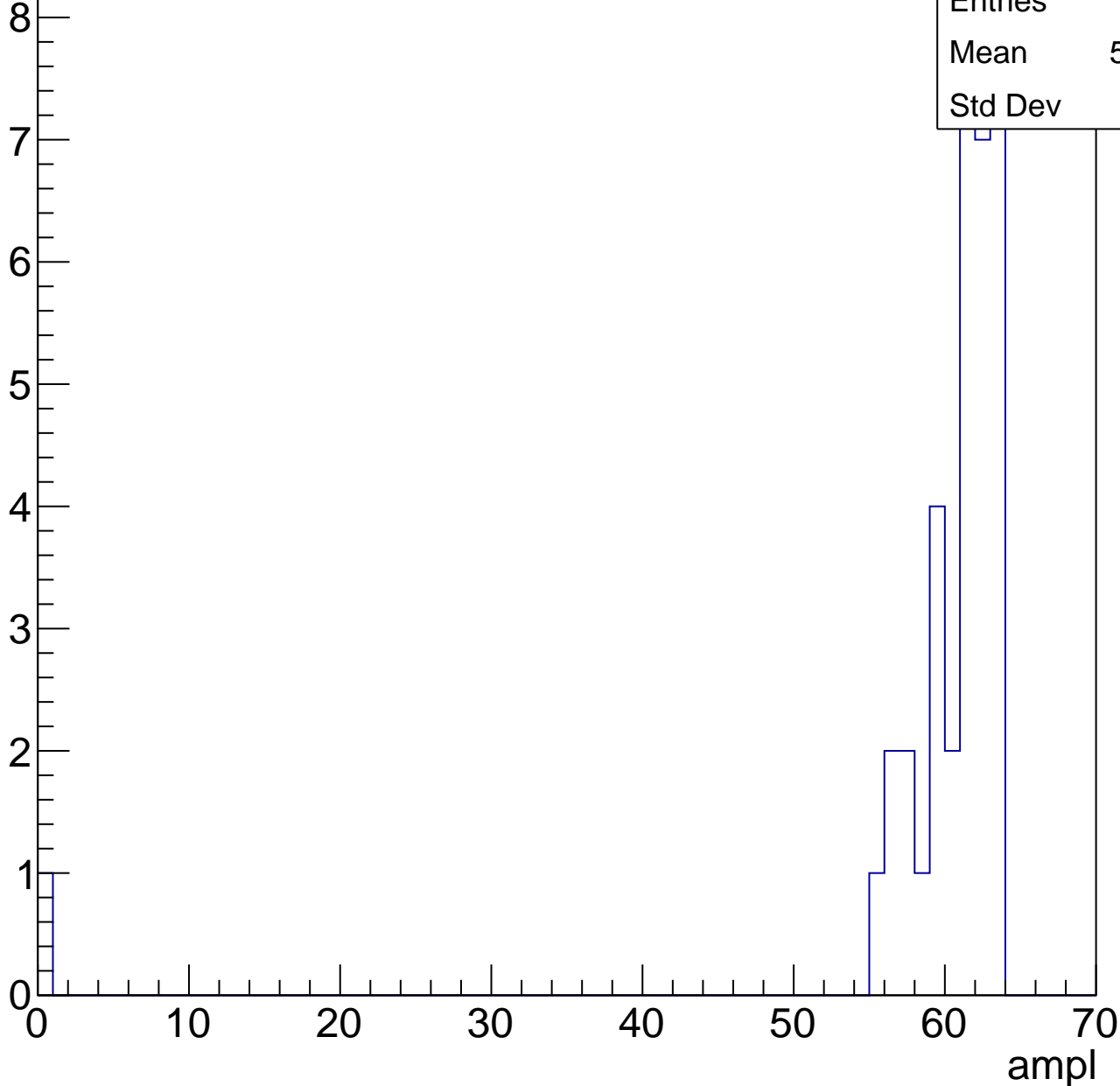


# B1L101S, U9-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

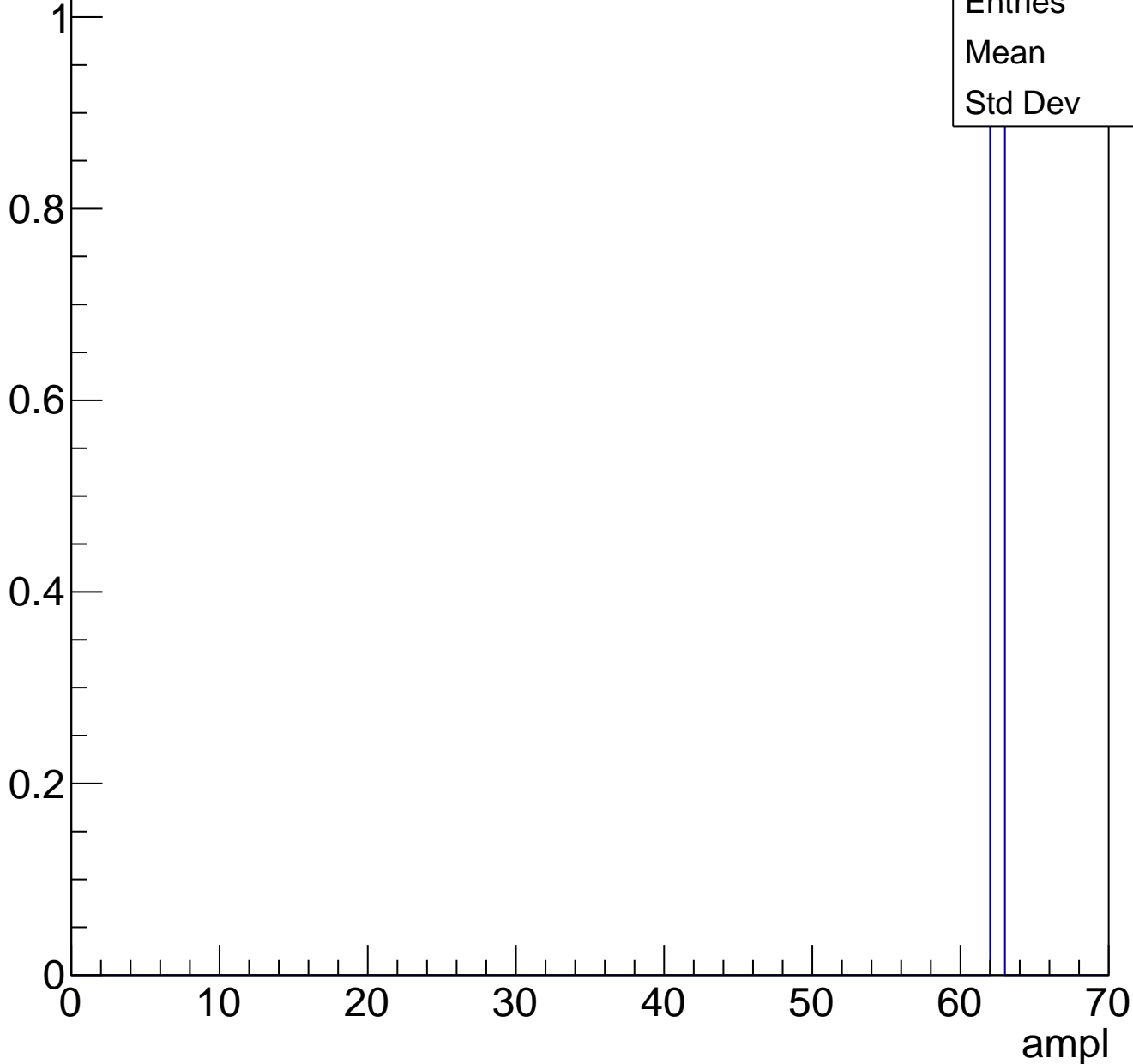
Entries	36
Mean	58.92
Std Dev	10.2



# B1L101S, U9-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U9-ch30, adc0

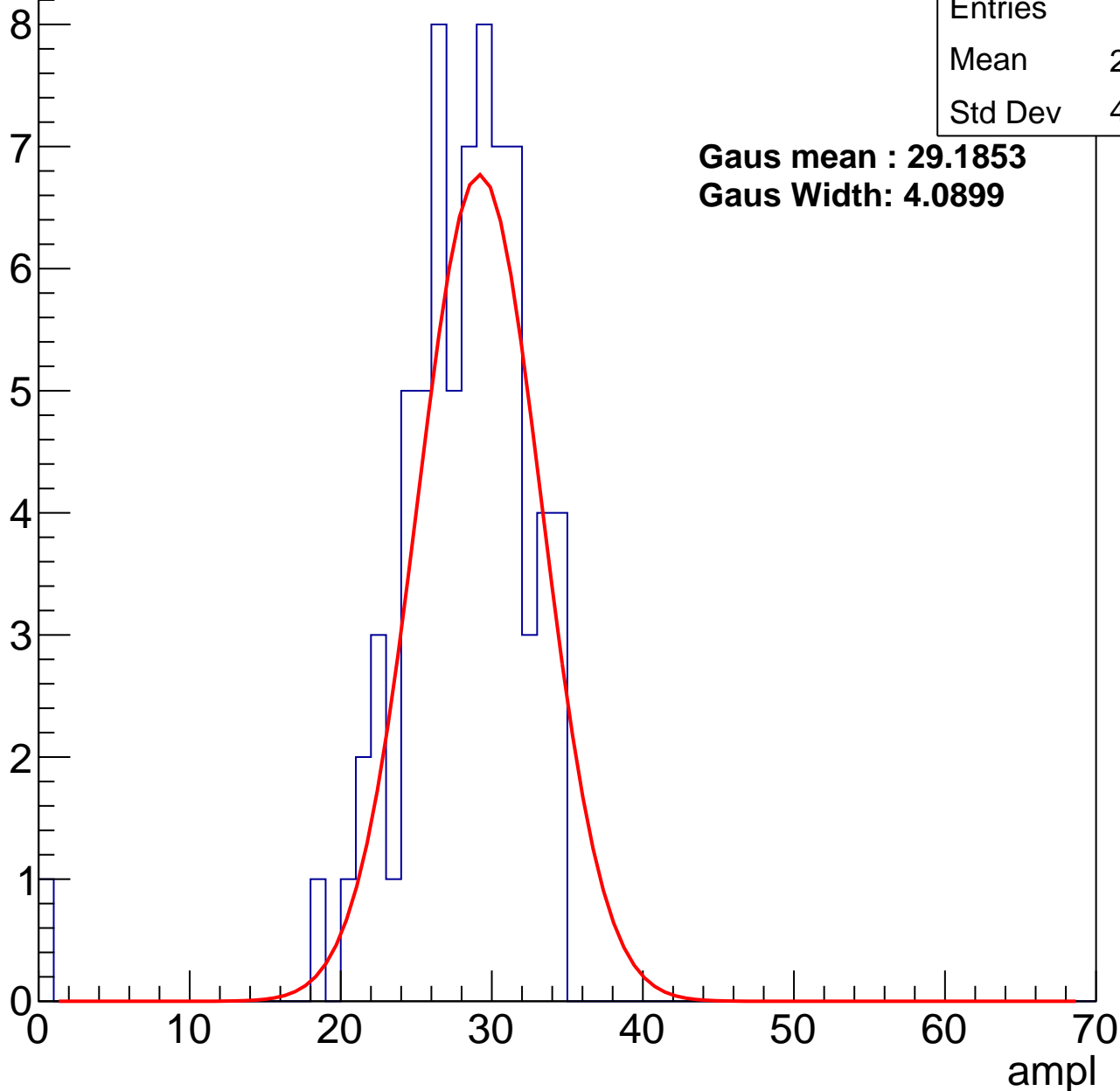
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	27.44
Std Dev	4.873

**Gaus mean : 29.1853**

**Gaus Width: 4.0899**



# B1L101S, U9-ch30, adc1

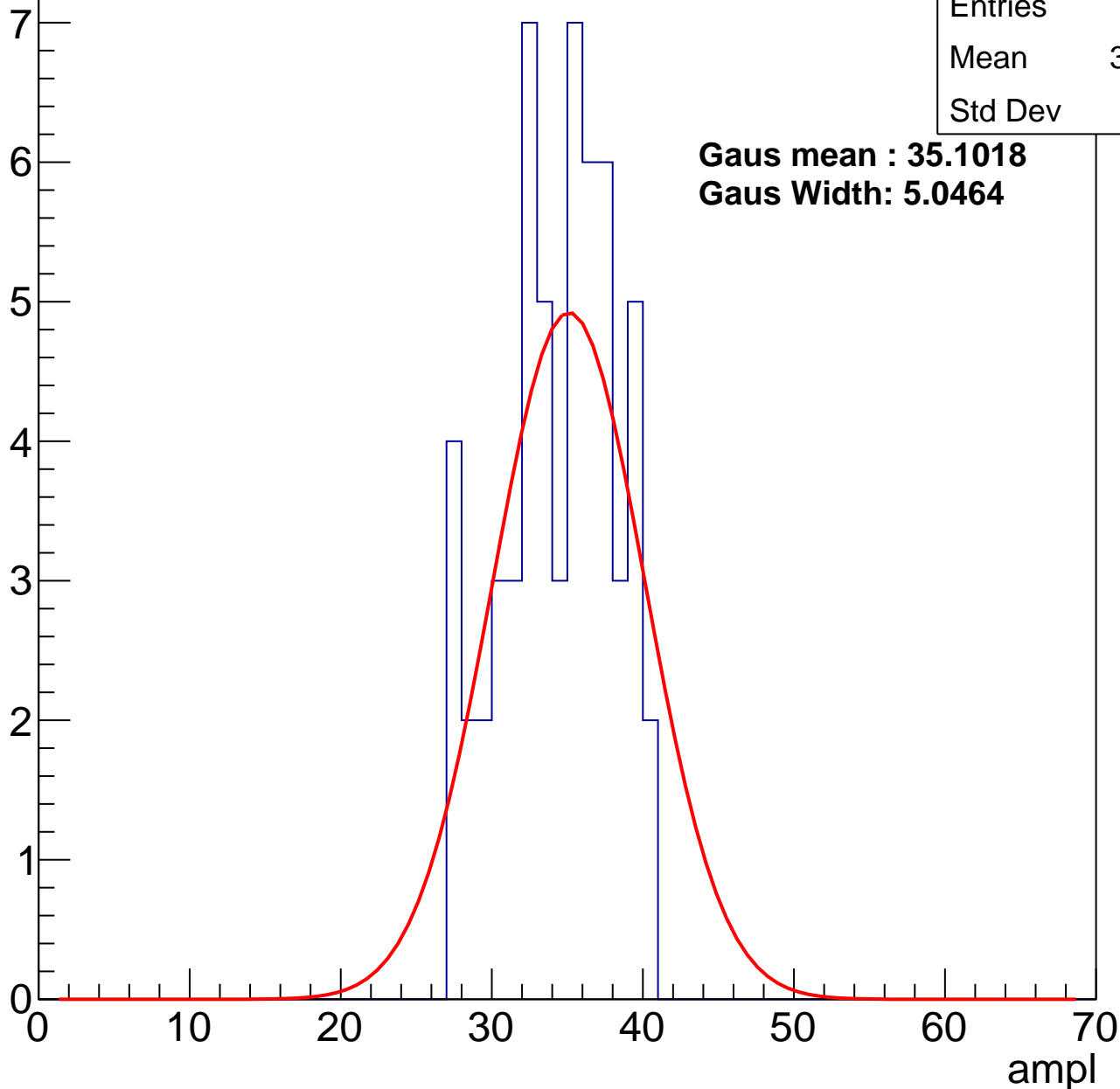
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	33.93
Std Dev	3.61

**Gaus mean : 35.1018**

**Gaus Width: 5.0464**



# B1L101S, U9-ch30, adc2

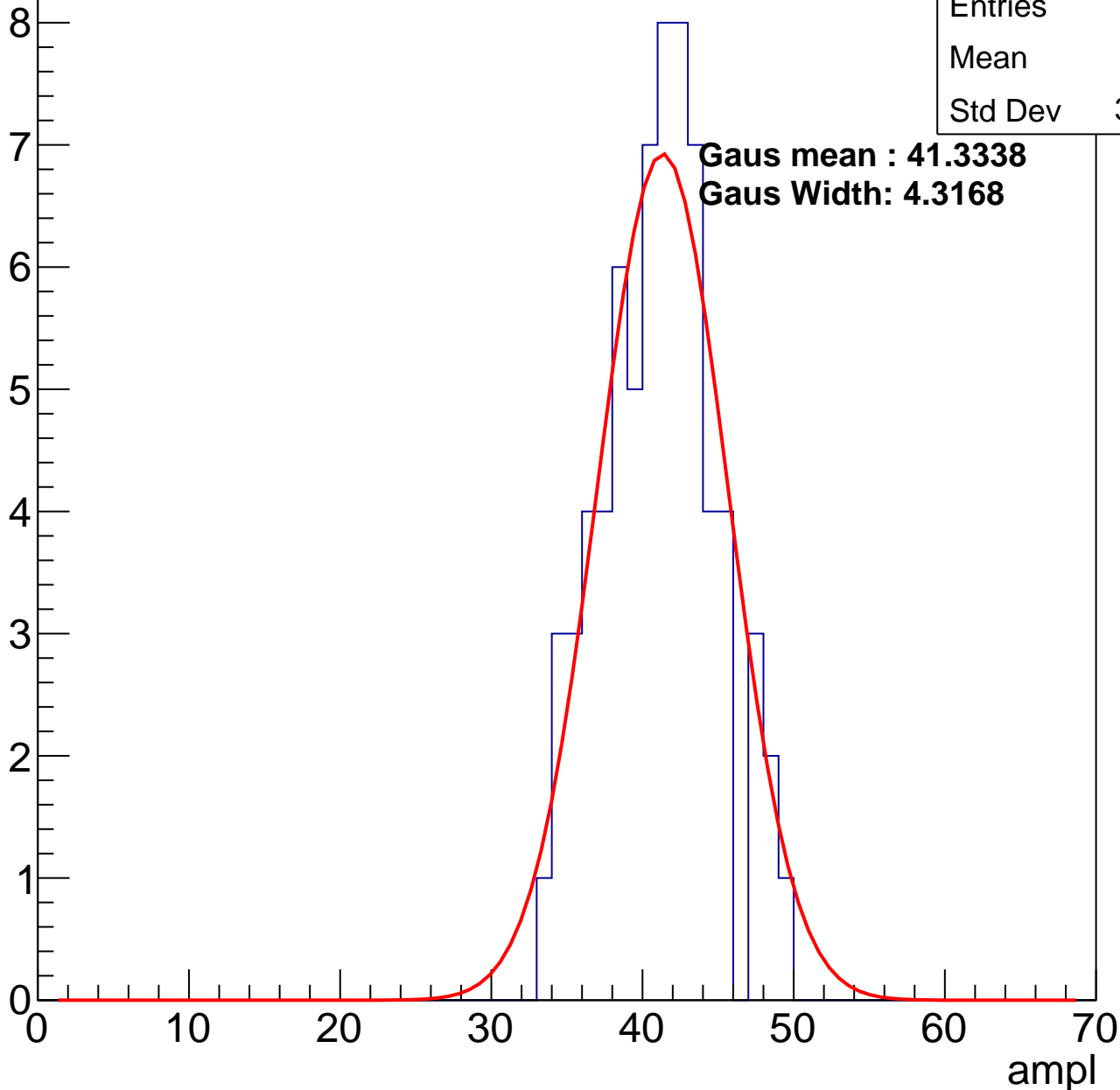
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	40.6
Std Dev	3.701

**Gaus mean : 41.3338**

**Gaus Width: 4.3168**

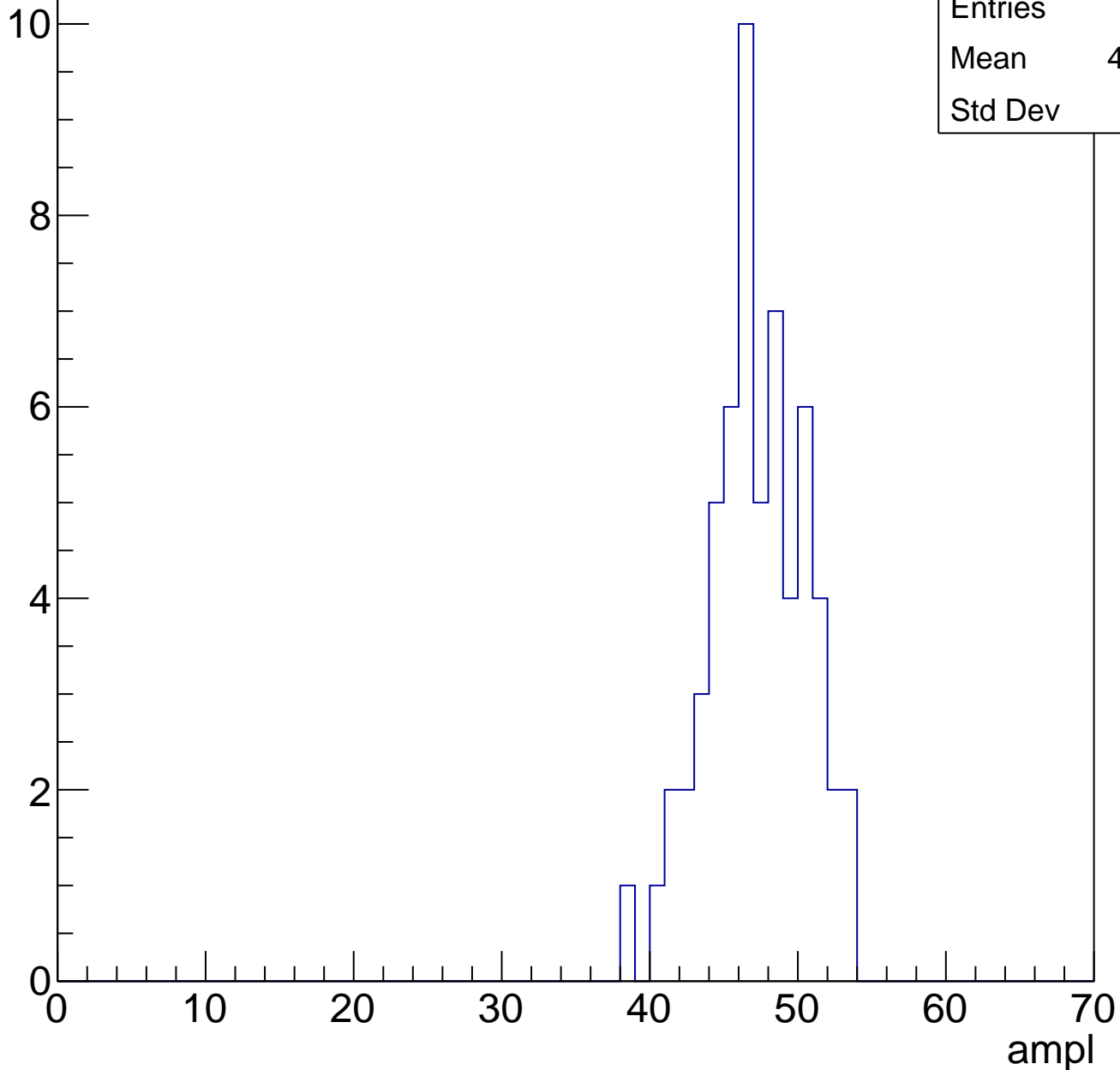


# B1L101S, U9-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	60
Mean	46.73
Std Dev	3.26

Entry

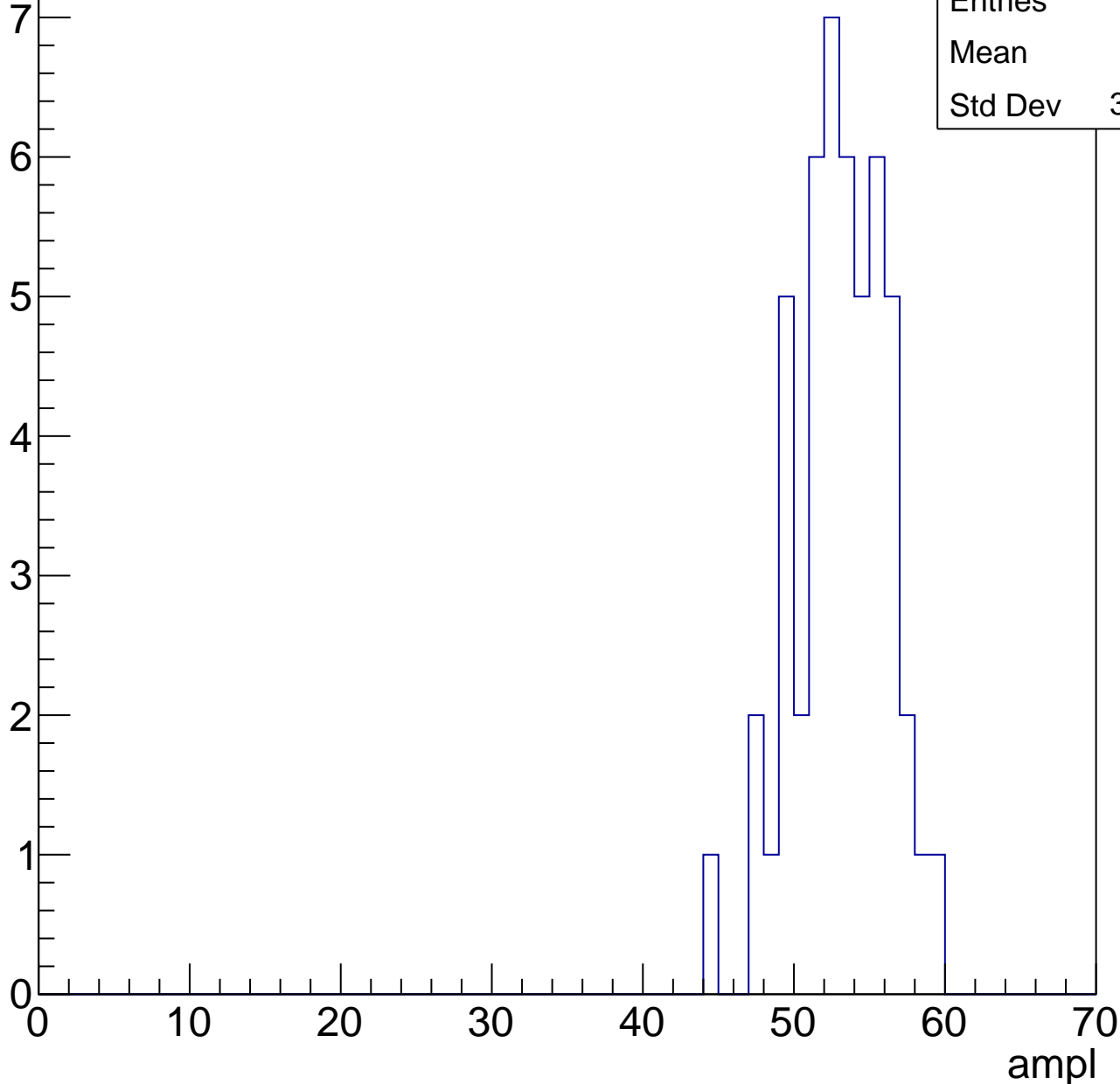


# B1L101S, U9-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	52.6
Std Dev	3.053



# B1L101S, U9-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

10

Entries 68

Mean 57.1

Std Dev 7.589

8

6

4

2

0

0

10

20

30

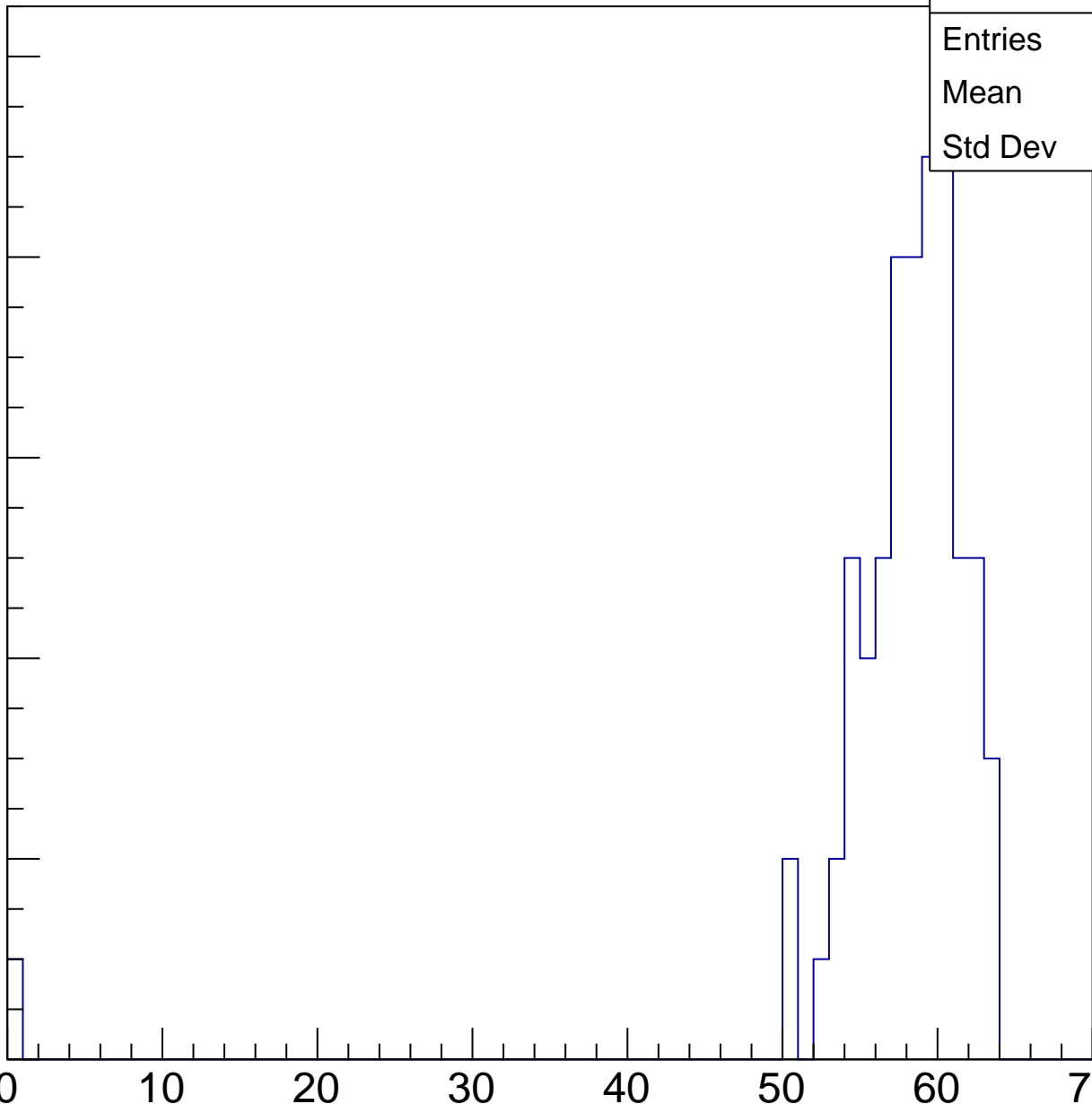
40

50

60

70

ampl

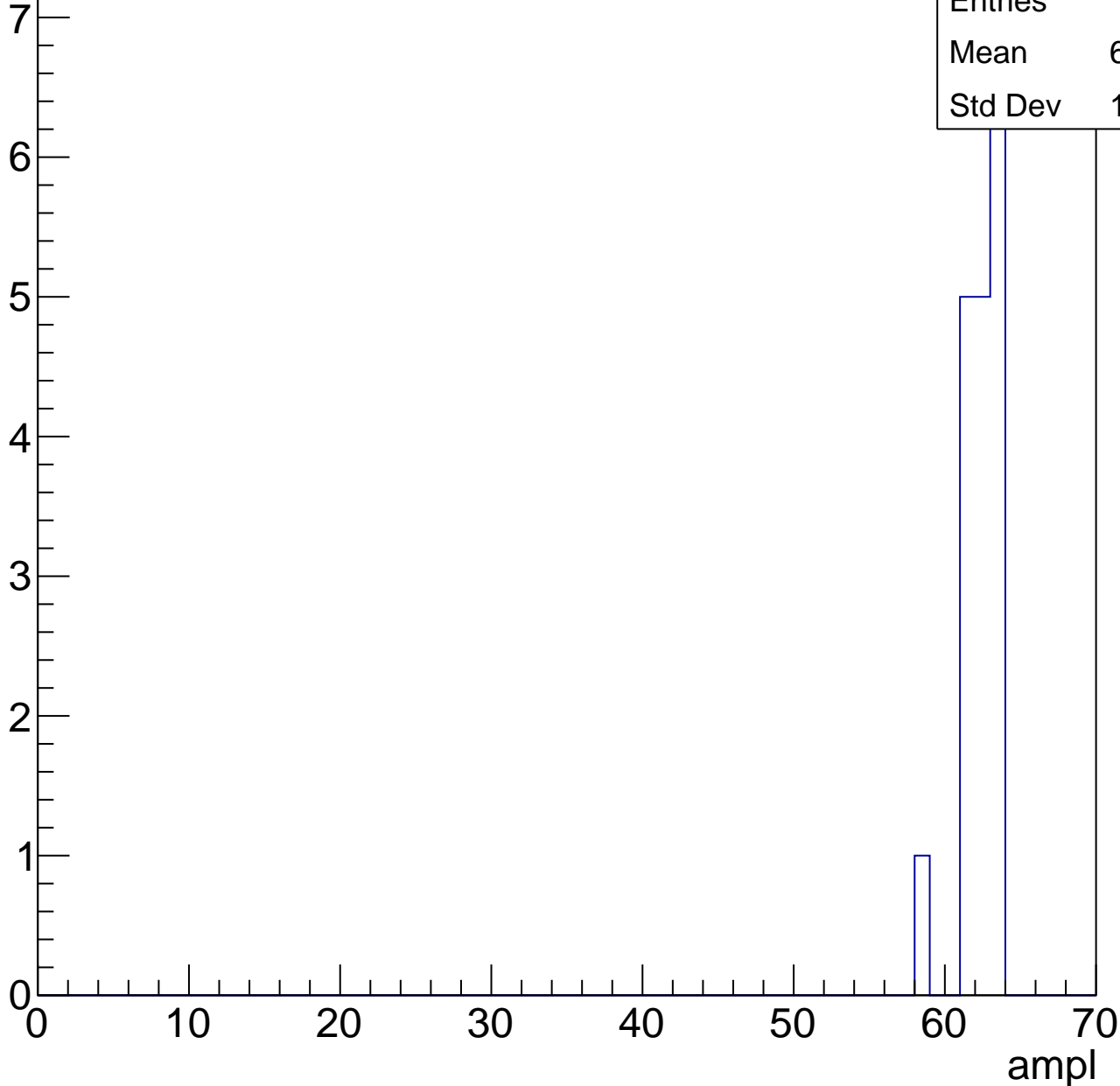


# B1L101S, U9-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	18
Mean	61.89
Std Dev	1.242





# B1L101S, U9-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch31, adc0

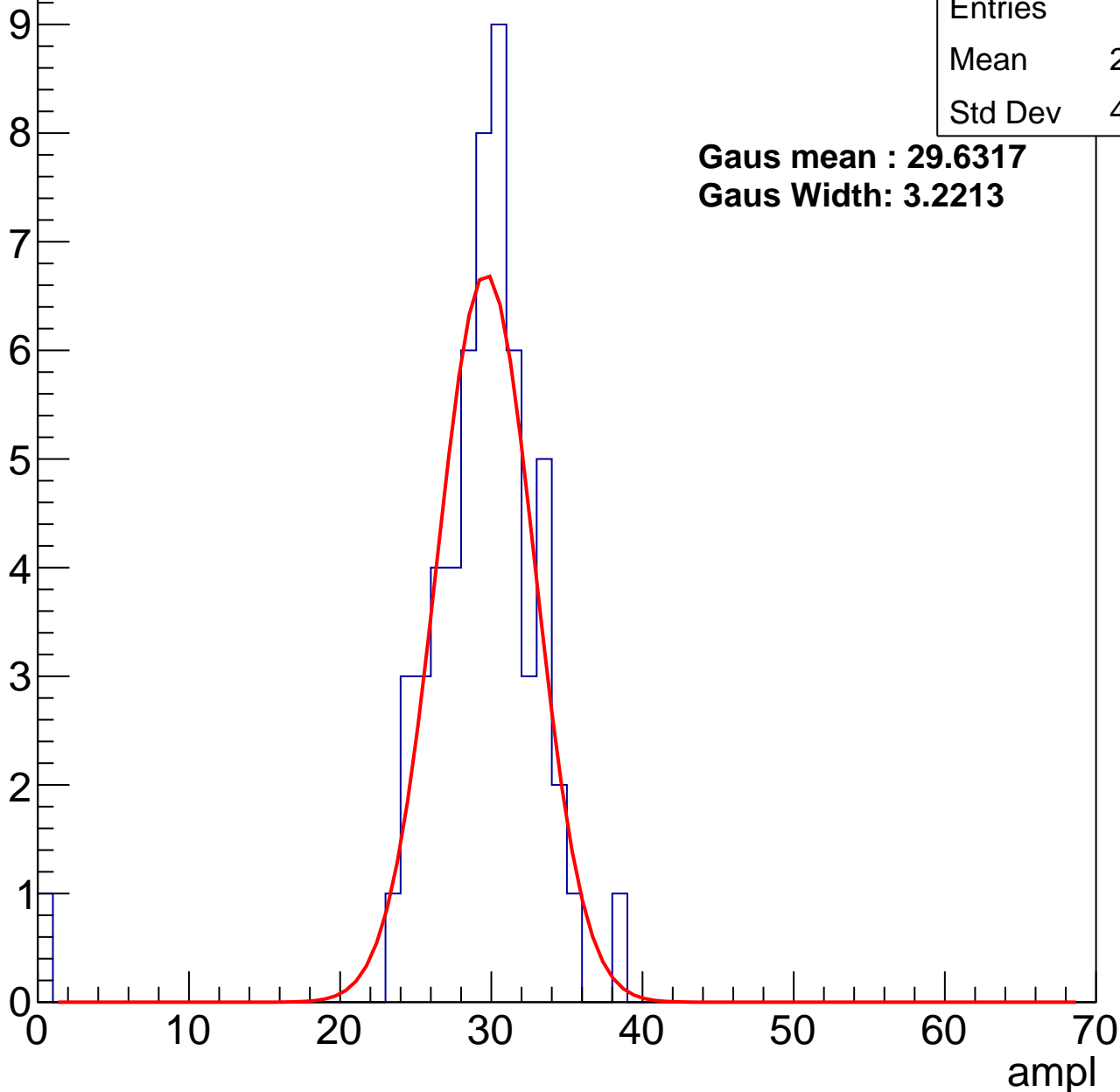
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	28.77
Std Dev	4.888

**Gaus mean : 29.6317**

**Gaus Width: 3.2213**



# B1L101S, U9-ch31, adc1

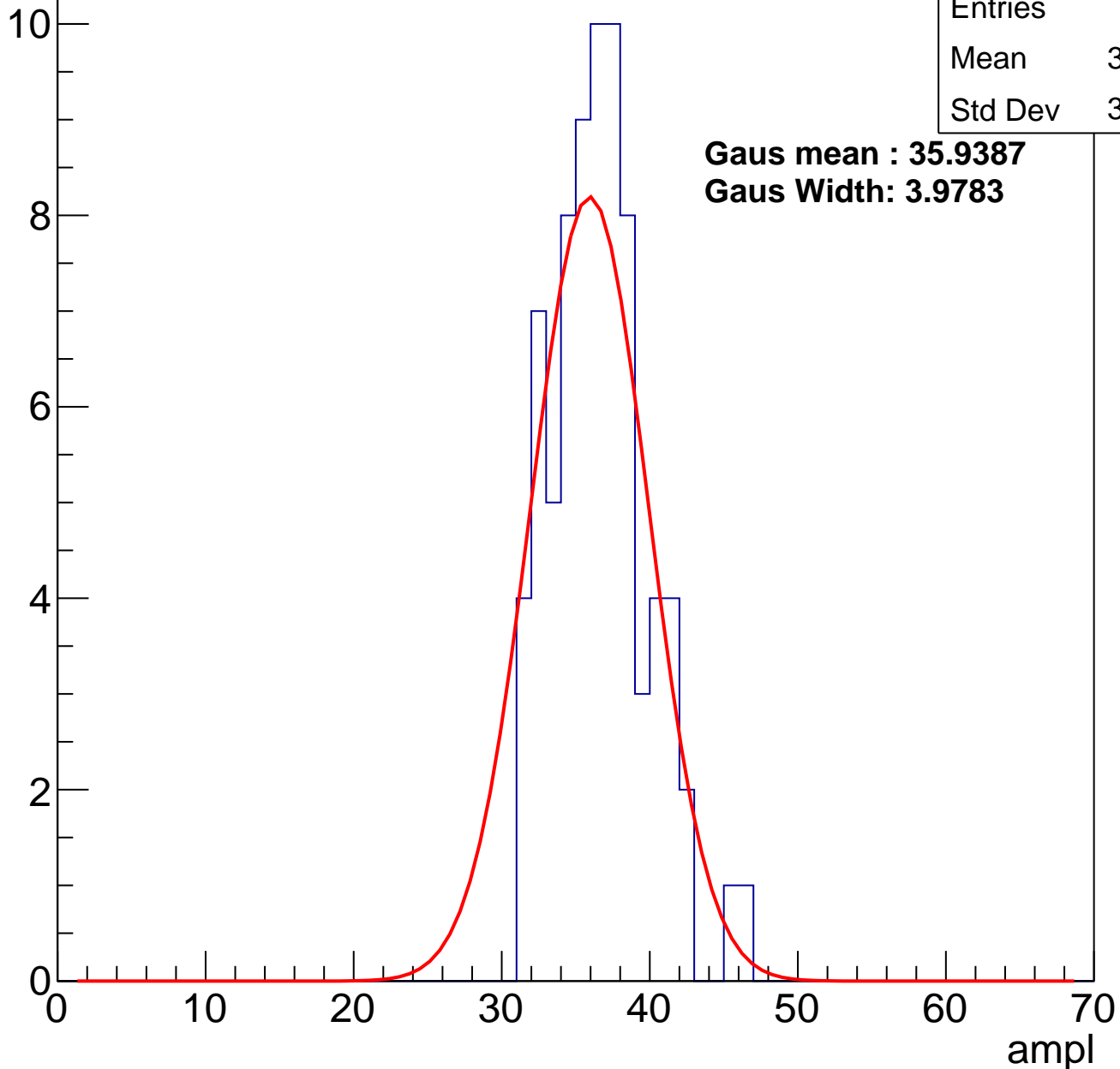
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	76
Mean	36.18
Std Dev	3.207

**Gaus mean : 35.9387**

**Gaus Width: 3.9783**

Entry



# B1L101S, U9-ch31, adc2

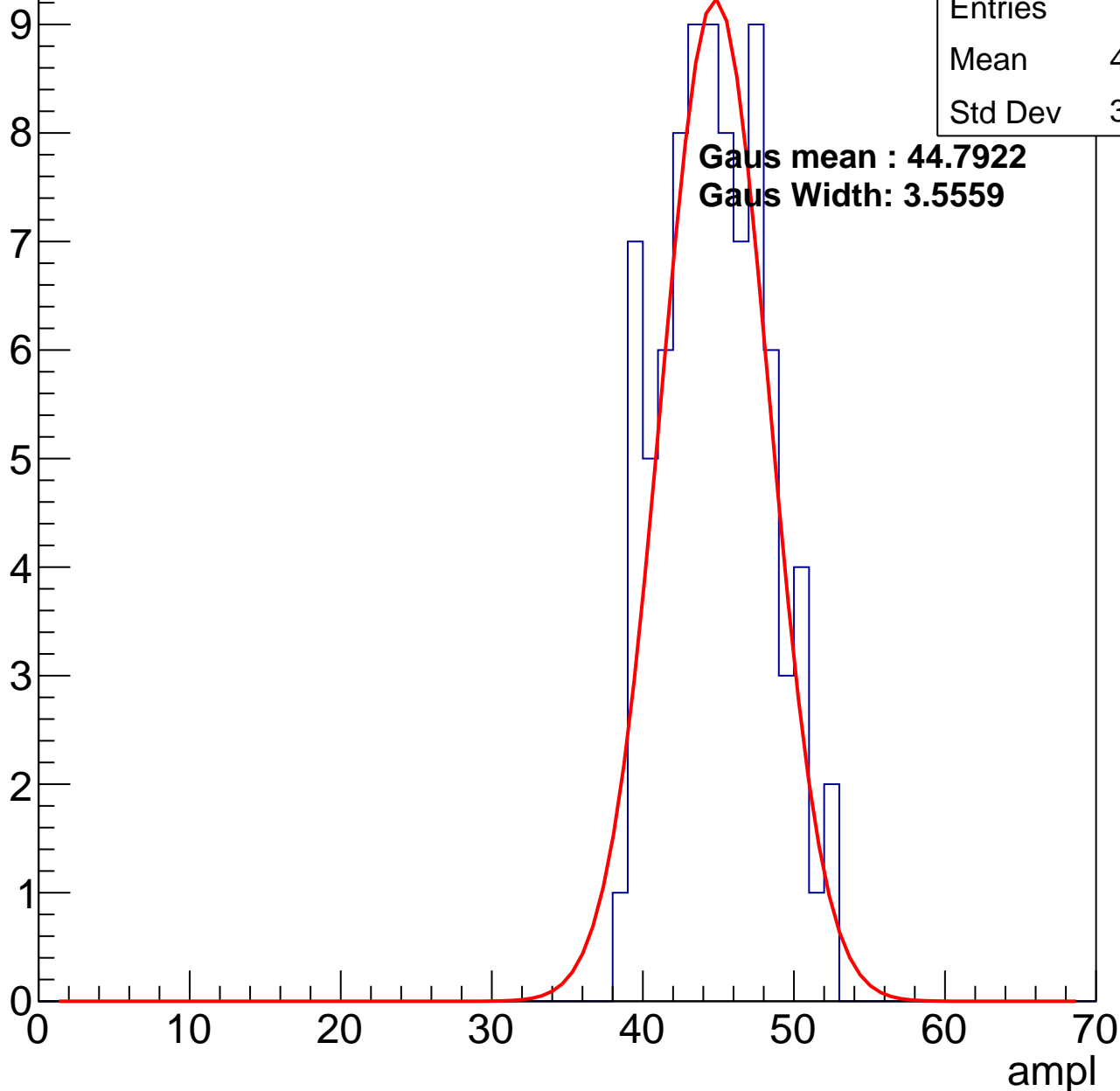
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	85
Mean	44.36
Std Dev	3.402

**Gaus mean : 44.7922**

**Gaus Width: 3.5559**

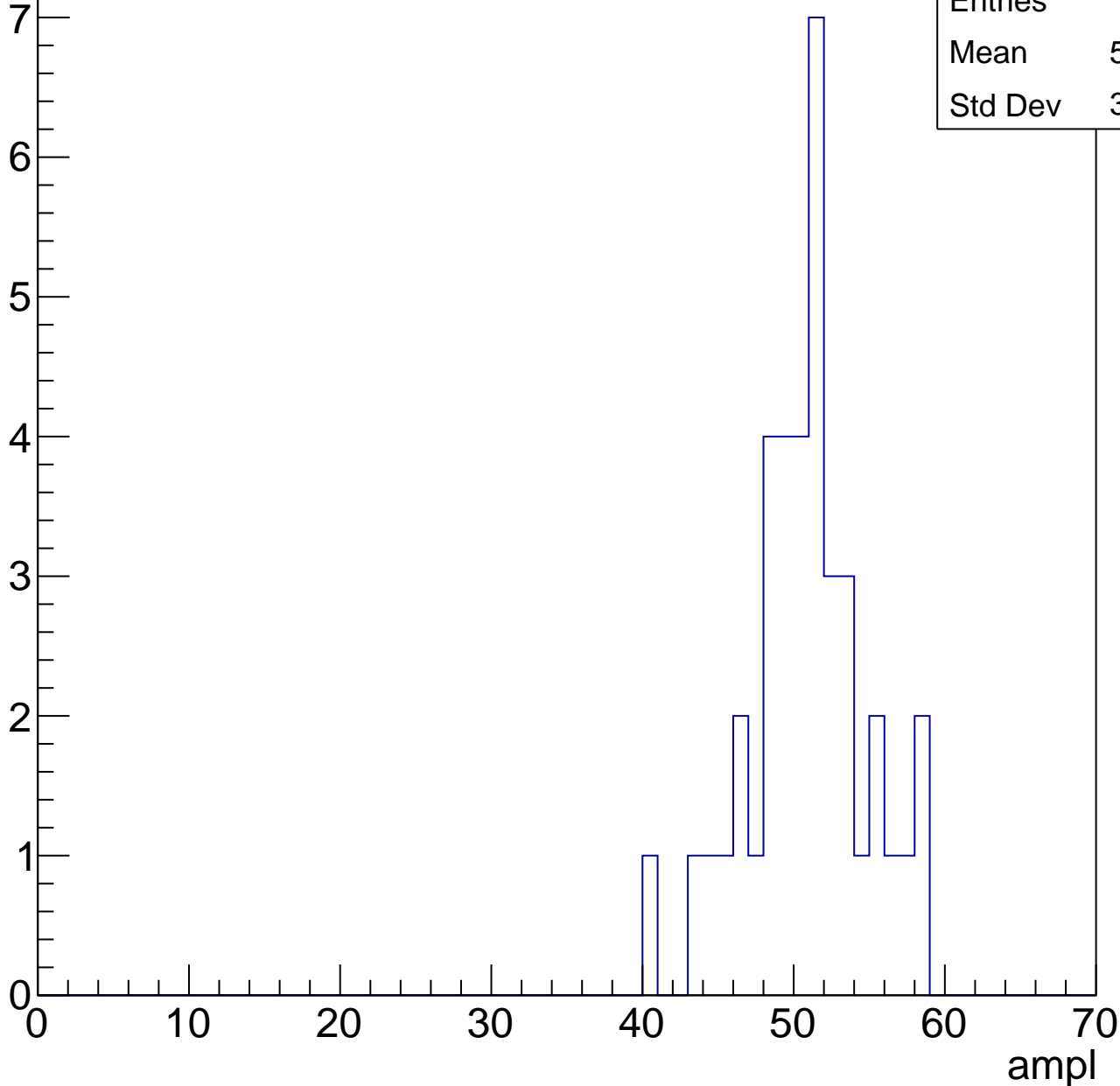


# B1L101S, U9-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

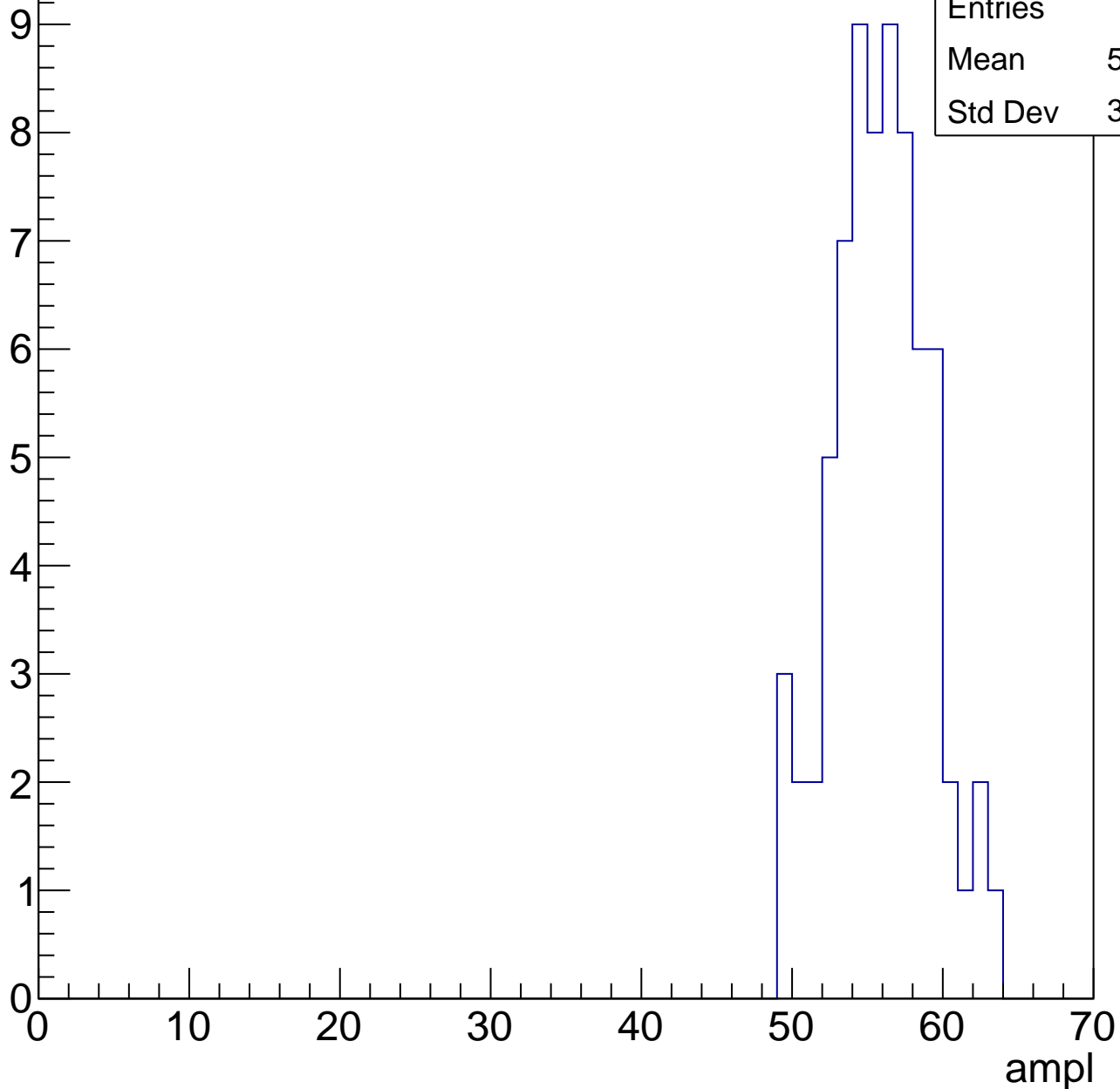
Entries	39
Mean	50.36
Std Dev	3.893



# B1L101S, U9-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

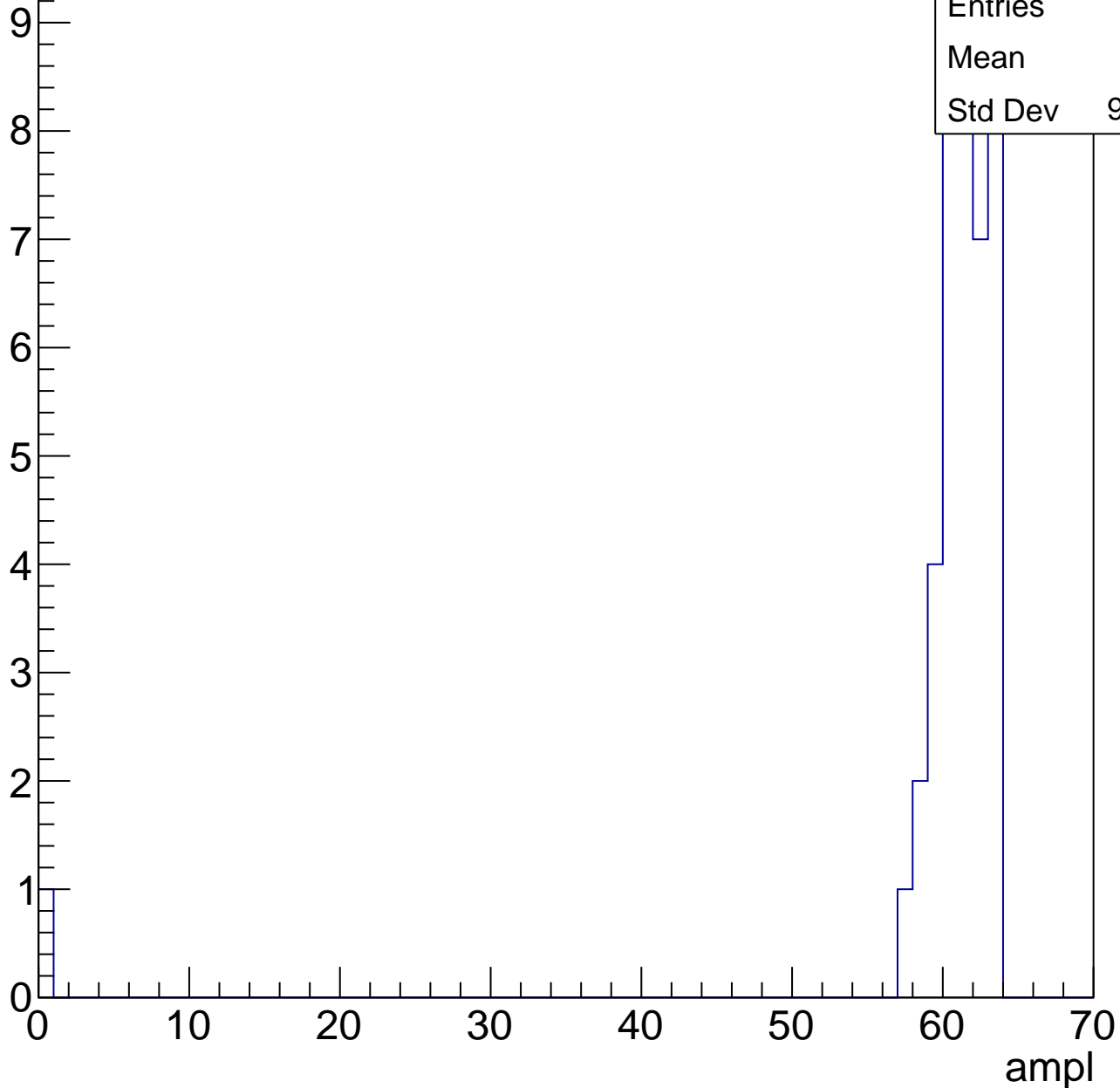


Entries	71
Mean	55.44
Std Dev	3.134

# B1L101S, U9-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U9-ch32, adc0

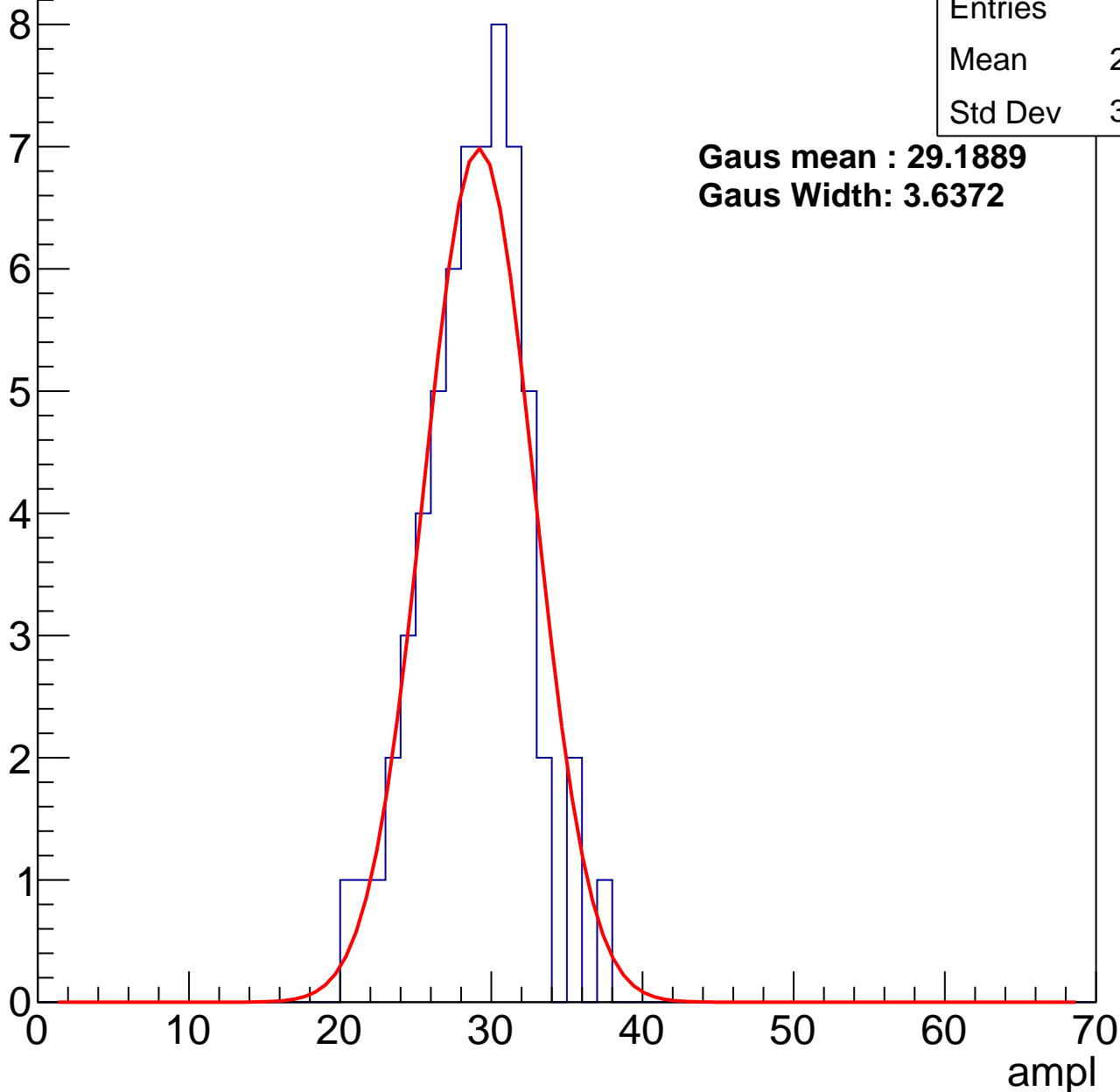
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	28.42
Std Dev	3.382

**Gaus mean : 29.1889**

**Gaus Width: 3.6372**



# B1L101S, U9-ch32, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	75
Mean	35.55
Std Dev	3.5

**Gaus mean : 36.0589**

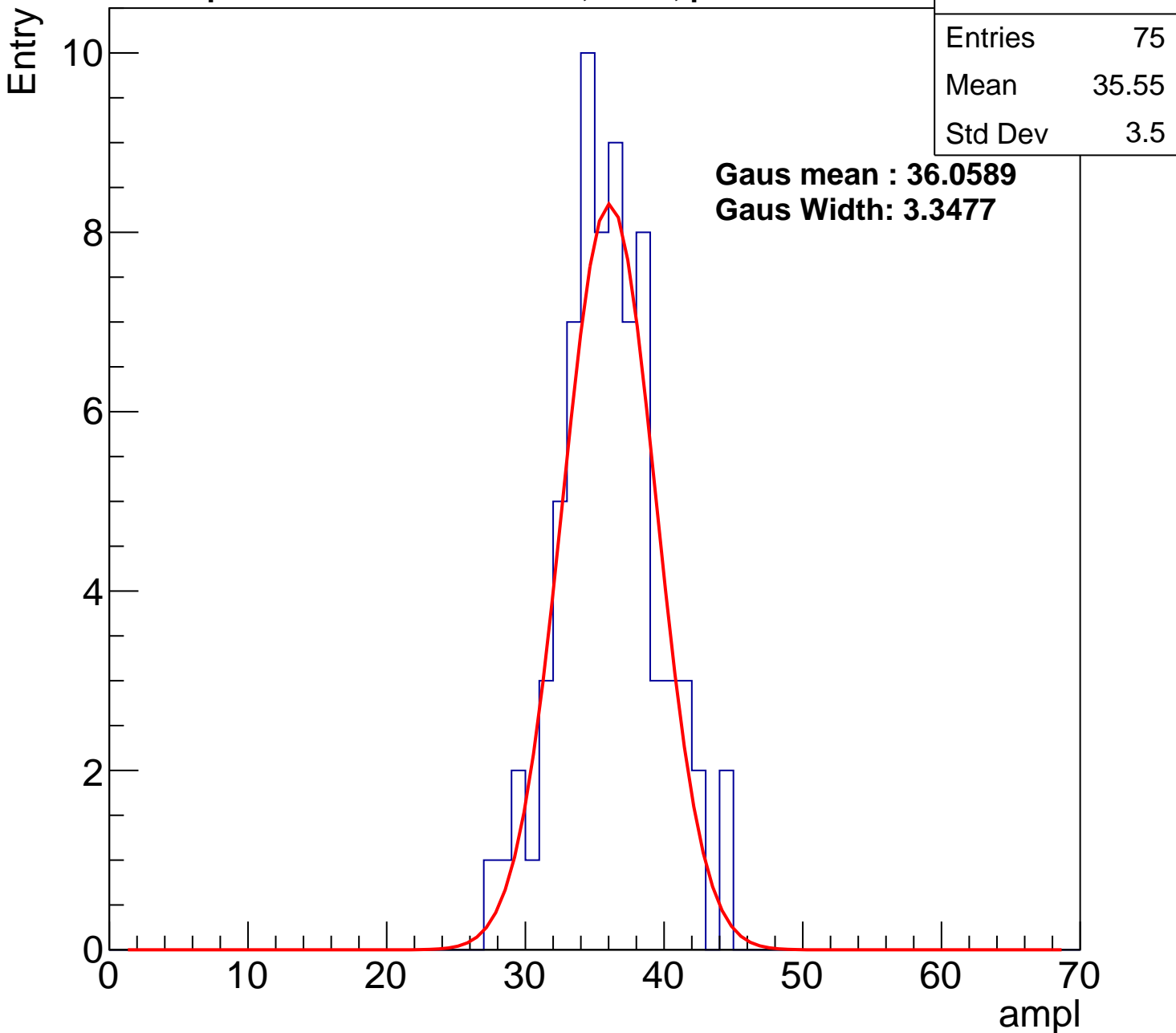
**Gaus Width: 3.3477**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U9-ch32, adc2

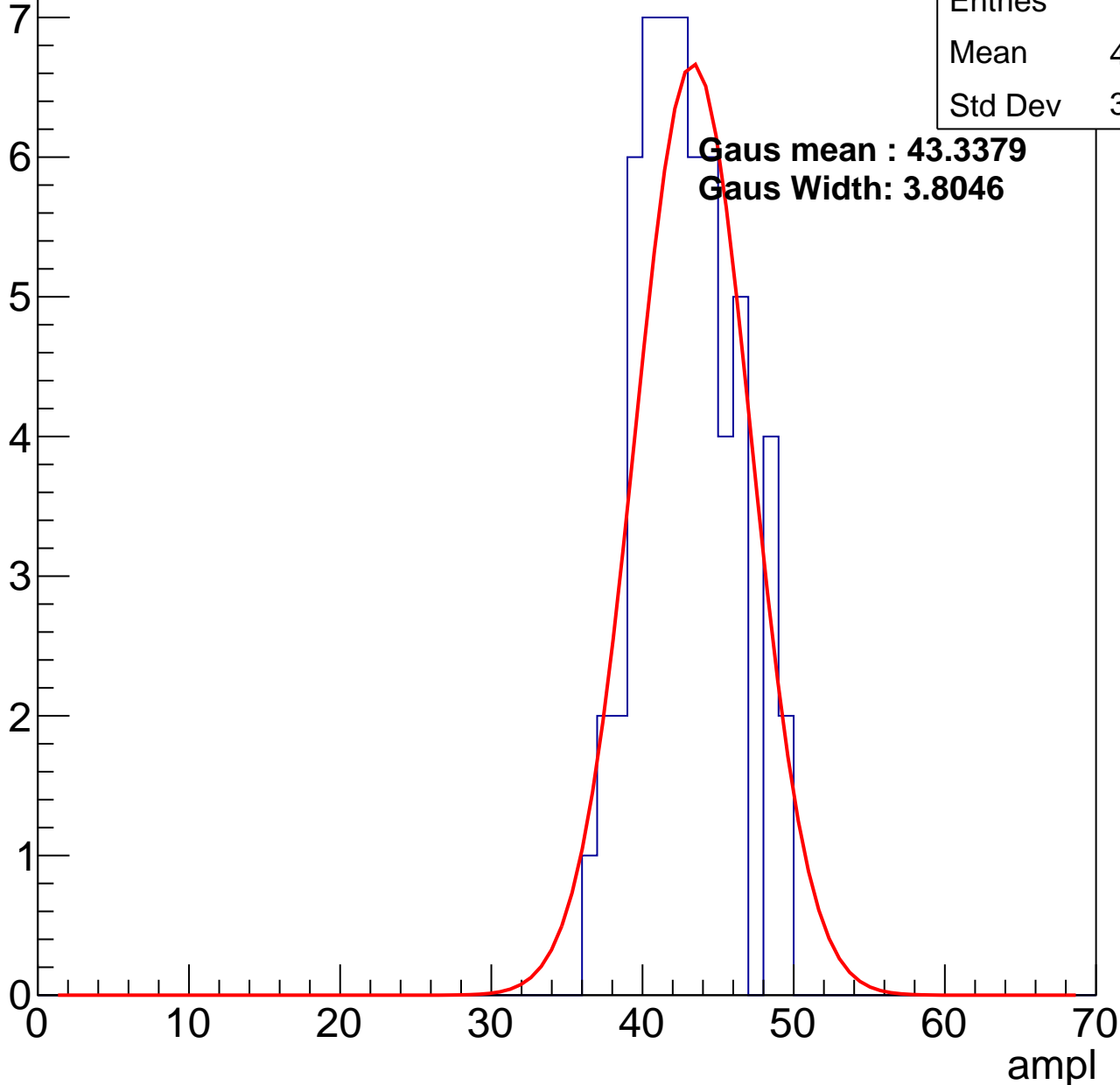
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	42.42
Std Dev	3.147

**Gaus mean : 43.3379**

**Gaus Width: 3.8046**



# B1L101S, U9-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

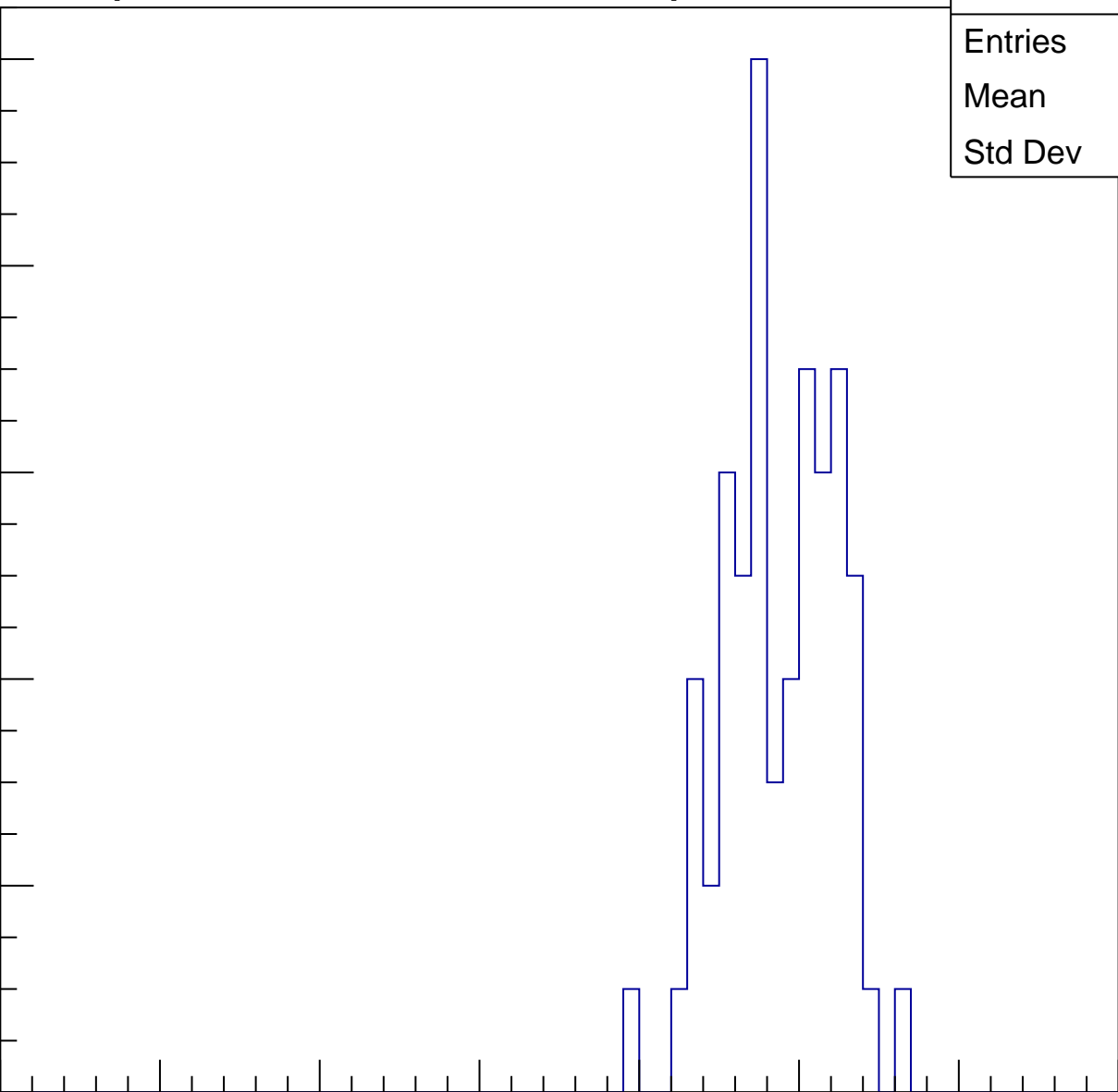
Entries	63
Mean	48.35
Std Dev	3.446

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

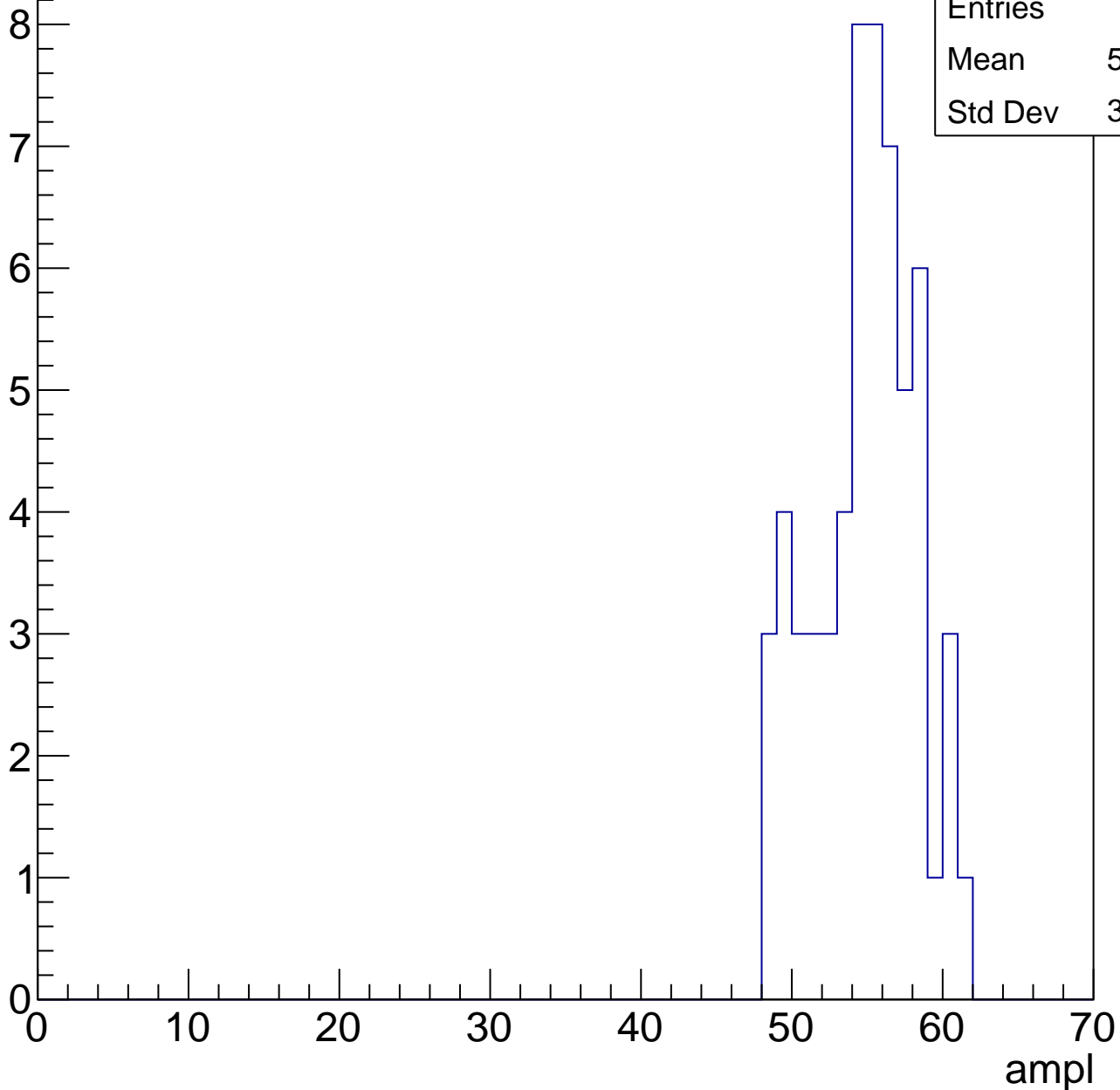


# B1L101S, U9-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

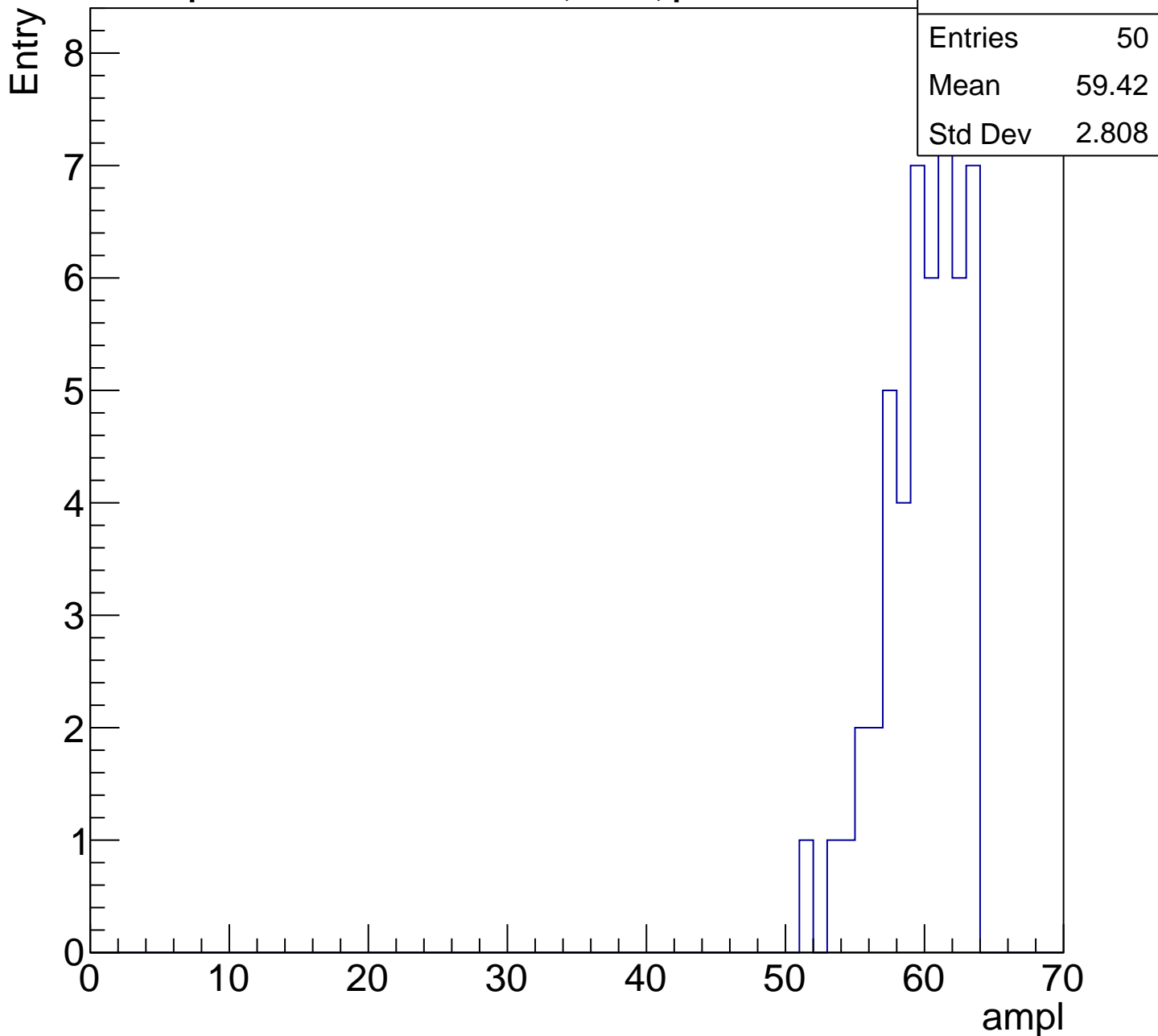
Entry

Entries	59
Mean	54.37
Std Dev	3.319



# B1L101S, U9-ch32, adc5

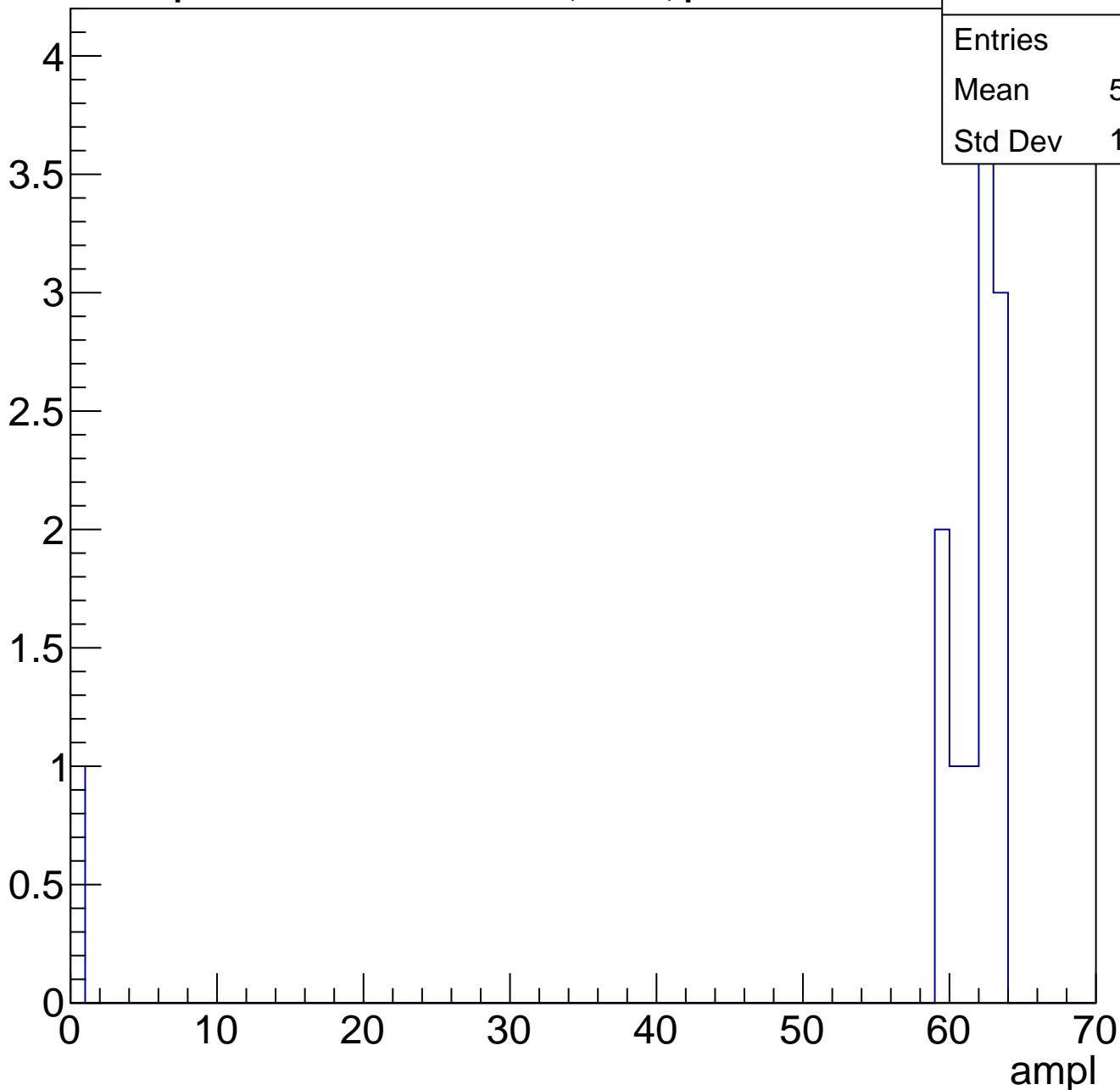
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

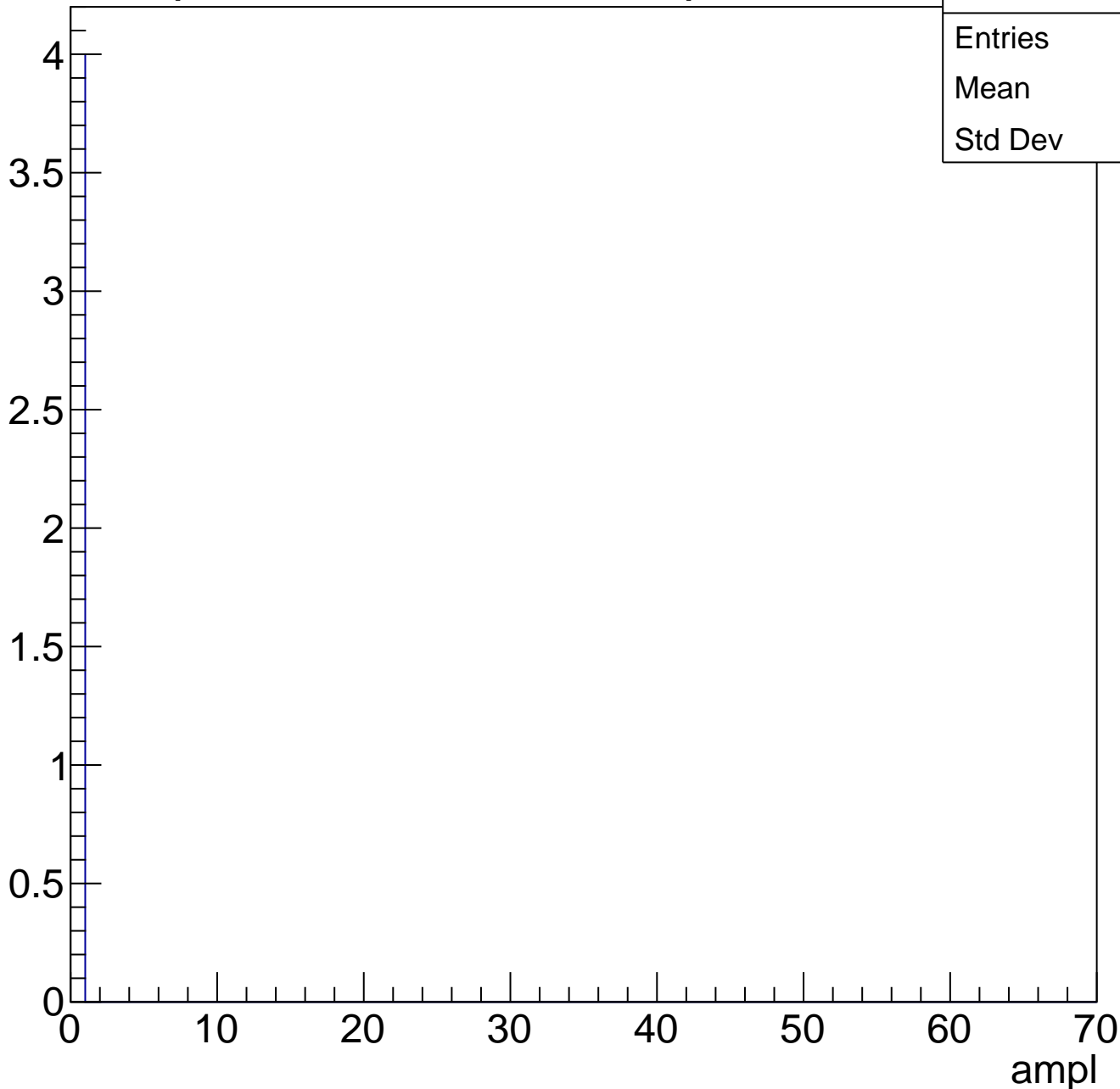




# B1L101S, U9-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	4
Mean	0
Std Dev	0

# B1L101S, U9-ch33, adc0

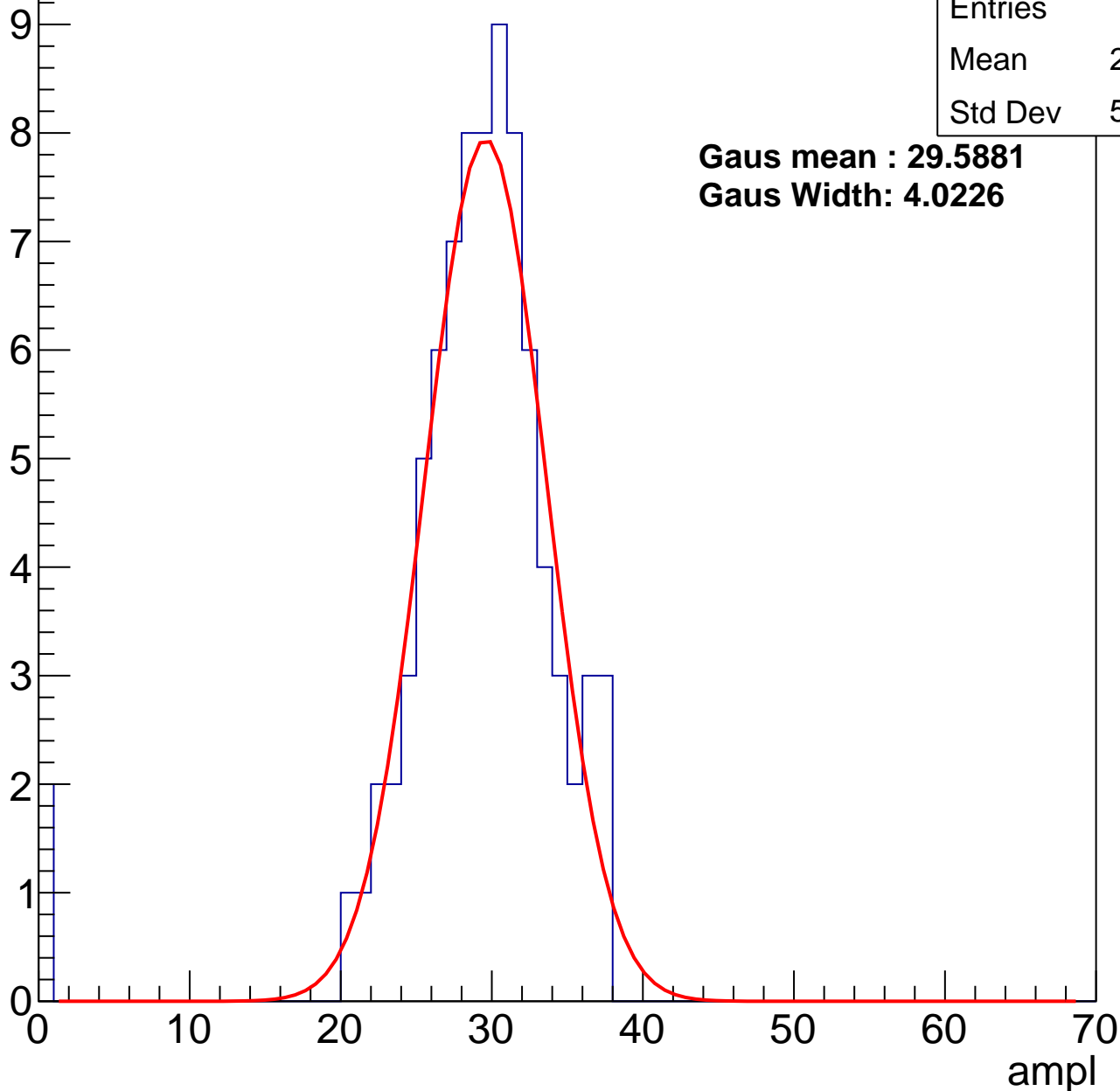
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	83
Mean	28.46
Std Dev	5.873

**Gaus mean : 29.5881**

**Gaus Width: 4.0226**



# B1L101S, U9-ch33, adc1

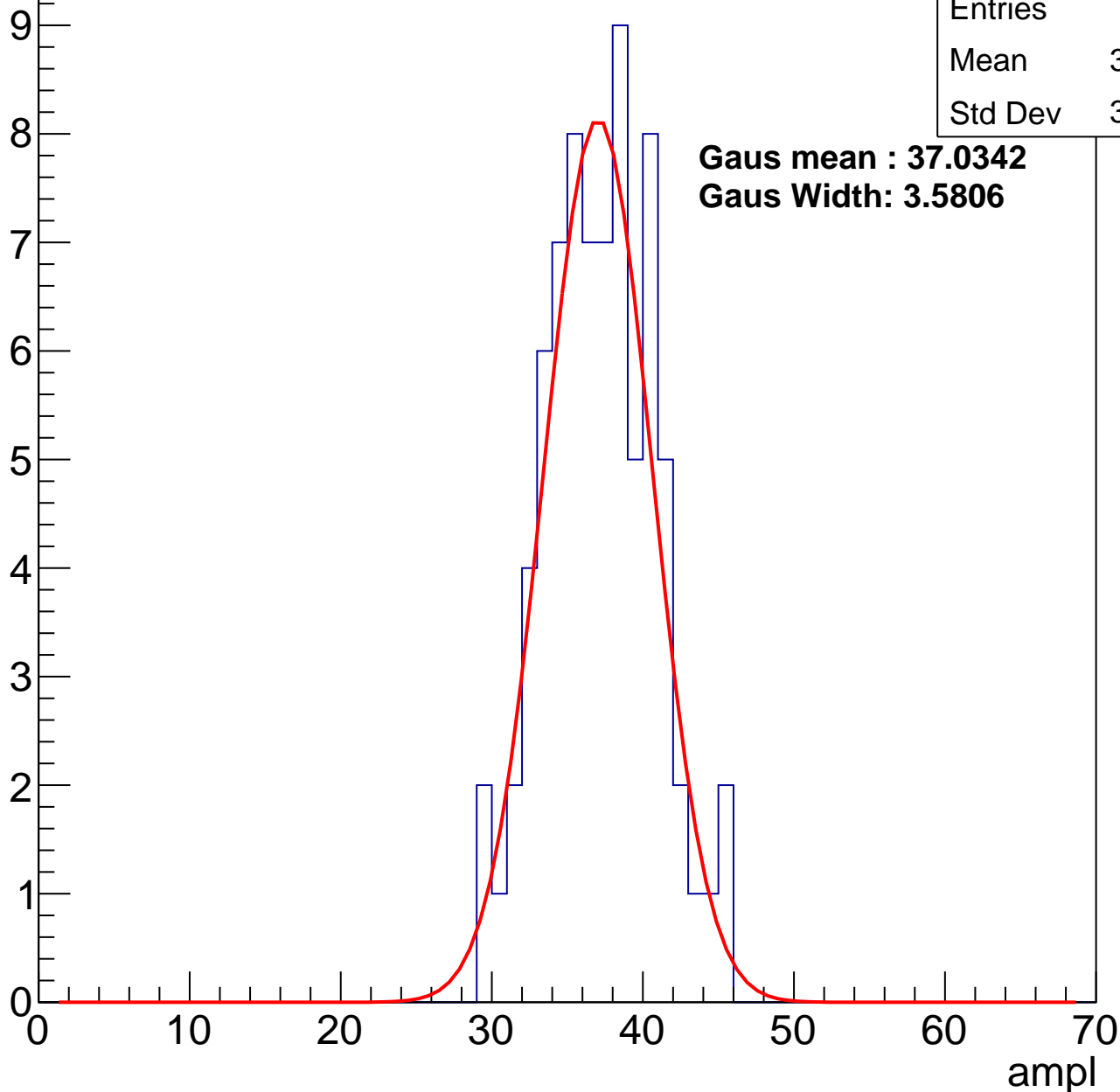
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	36.73
Std Dev	3.577

**Gaus mean : 37.0342**

**Gaus Width: 3.5806**



# B1L101S, U9-ch33, adc2

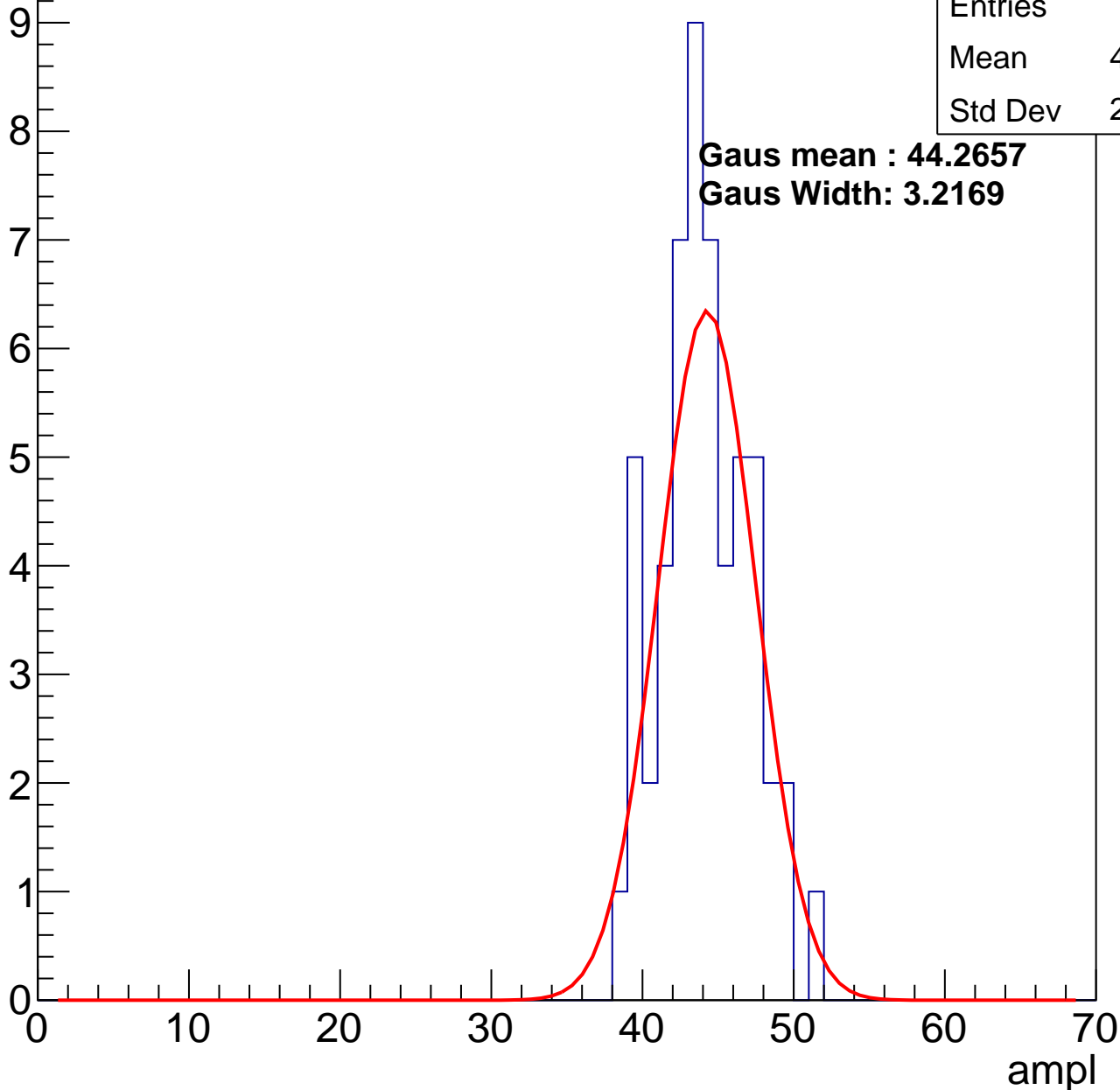
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	43.63
Std Dev	2.914

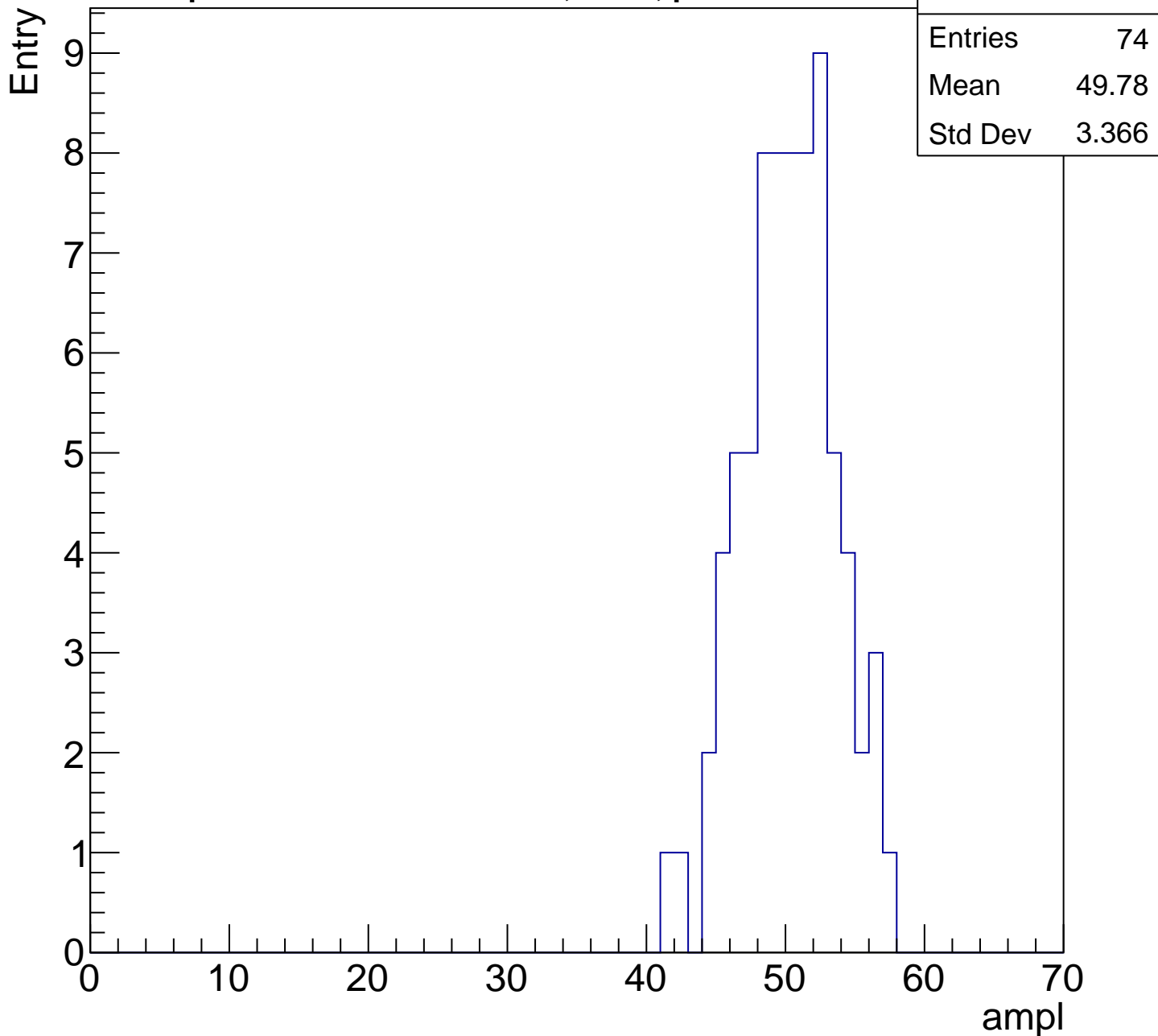
**Gaus mean : 44.2657**

**Gaus Width: 3.2169**



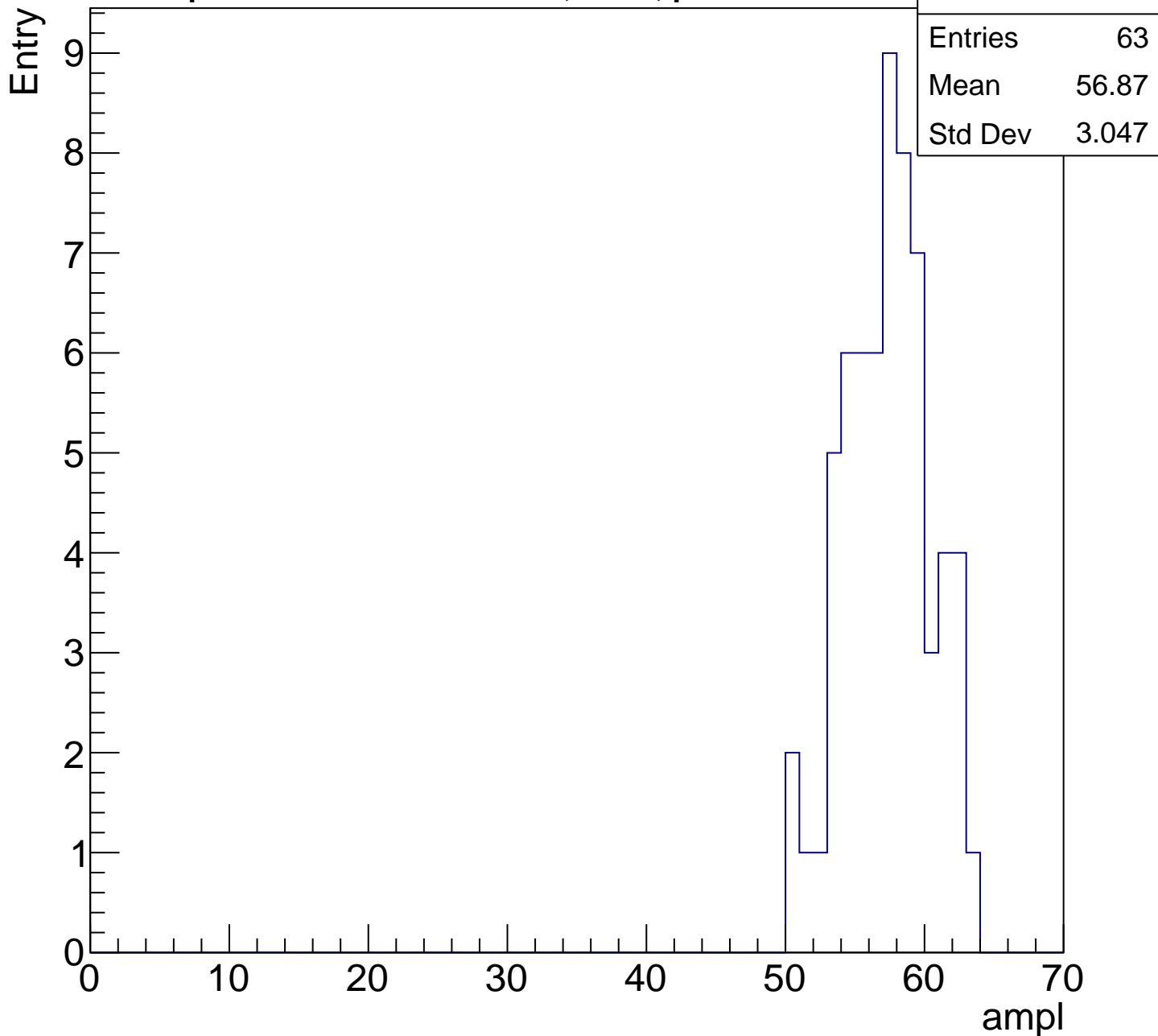
# B1L101S, U9-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

0

10

20

30

40

50

60

70

ampl

Entries	34
Mean	58.68
Std Dev	10.43

0

1

2

3

4

5

6

7

# B1L101S, U9-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch34, adc0

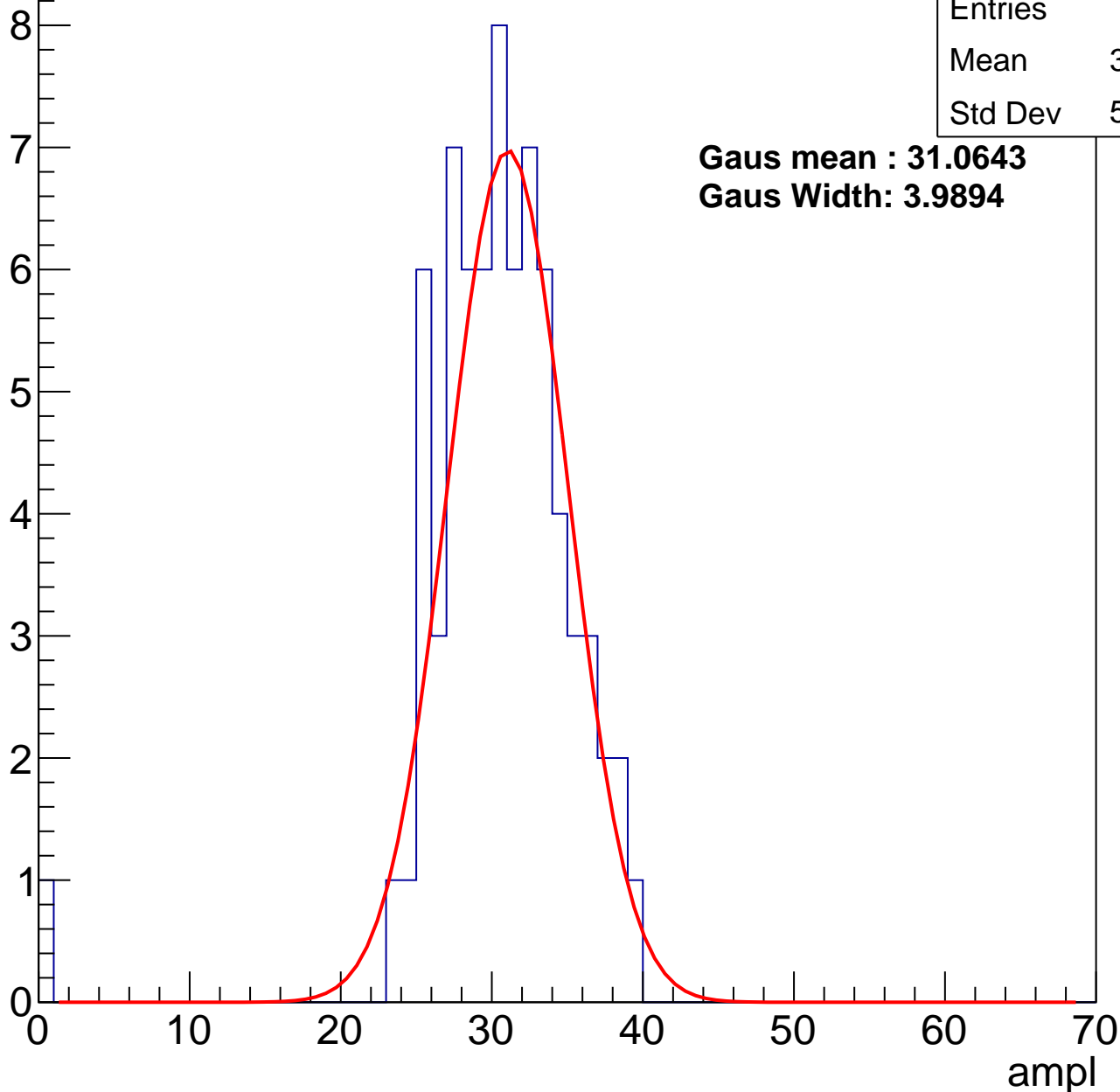
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	30.03
Std Dev	5.126

**Gaus mean : 31.0643**

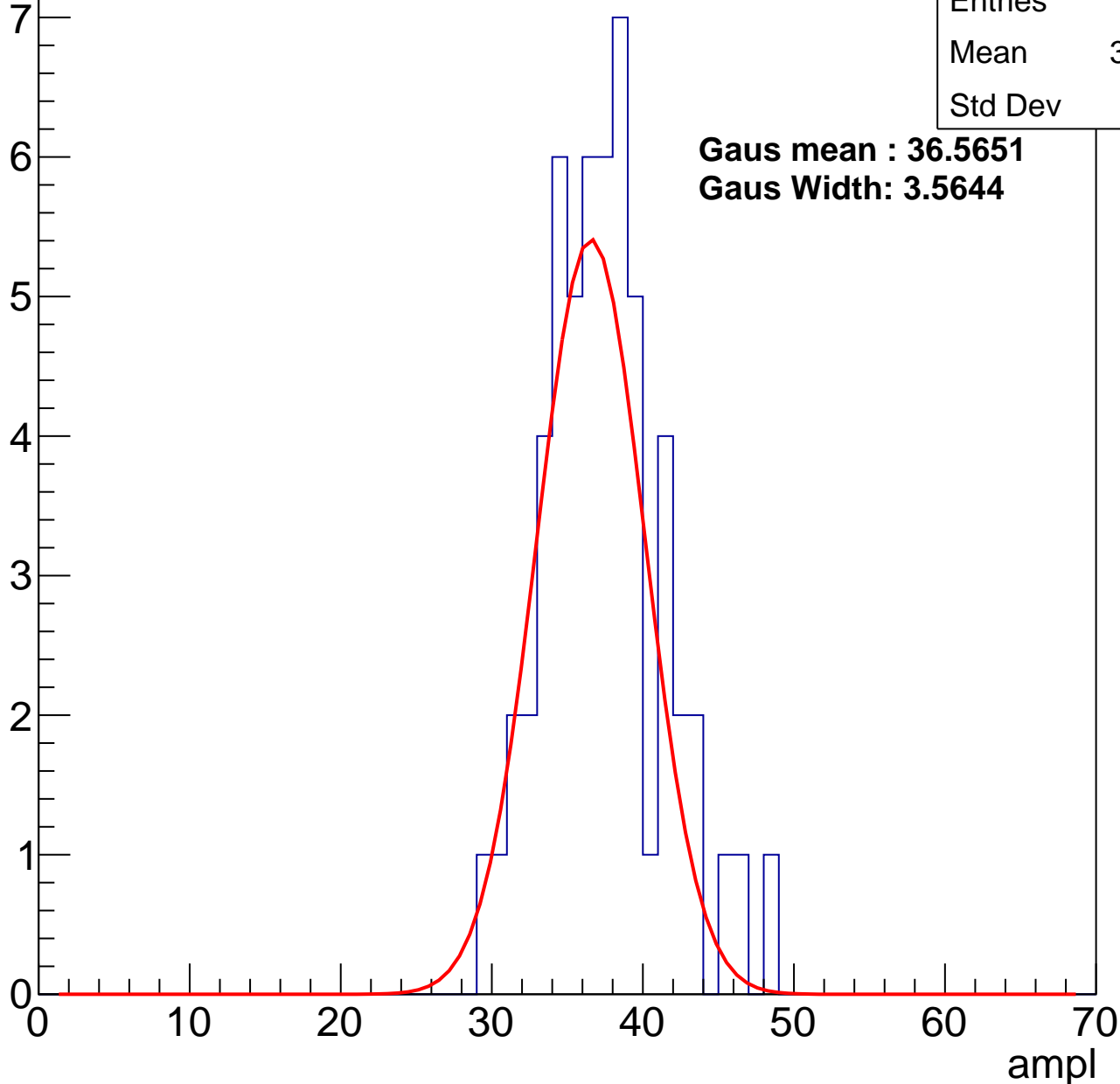
**Gaus Width: 3.9894**



# B1L101S, U9-ch34, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch34, adc2

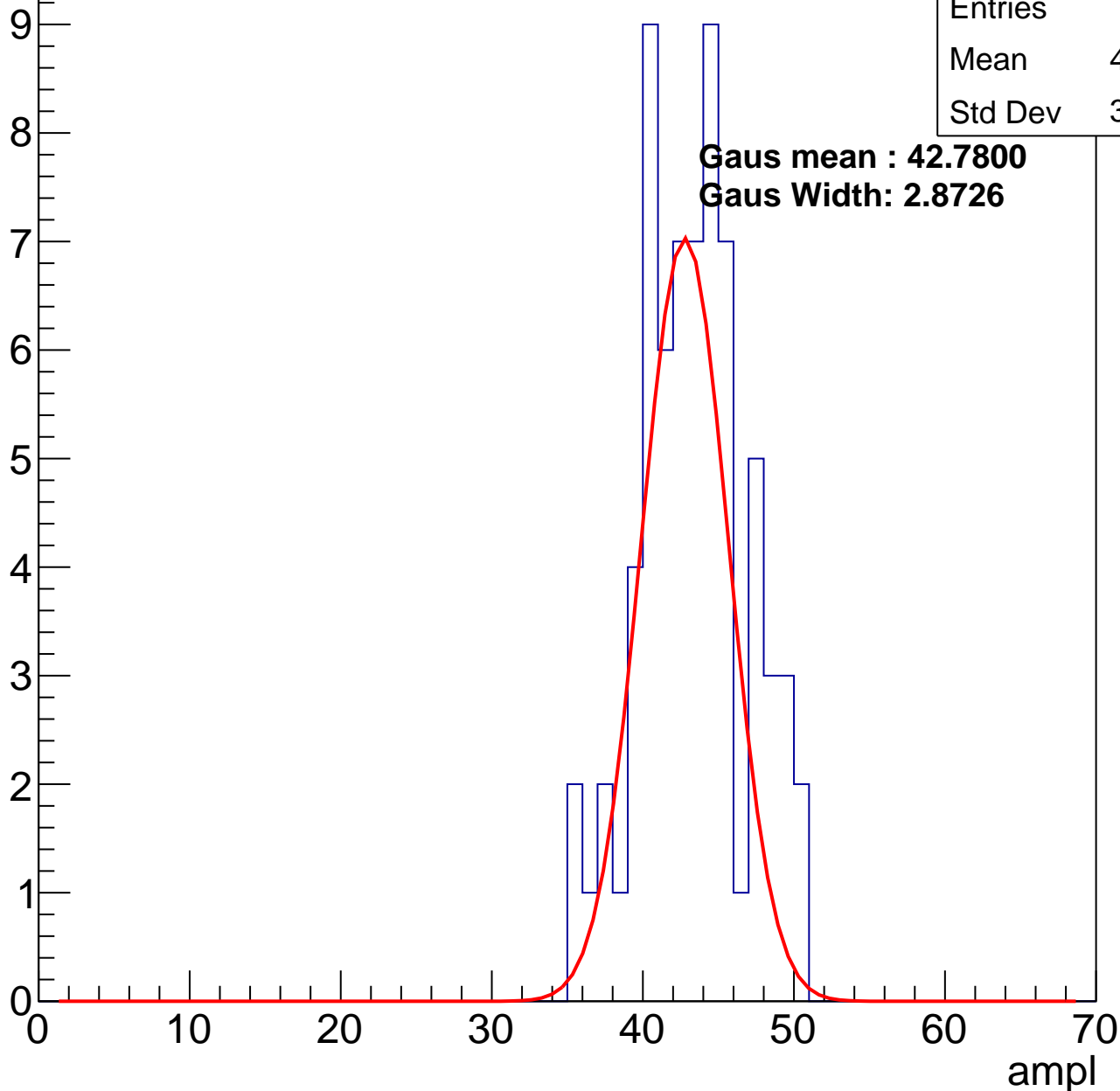
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	42.87
Std Dev	3.522

**Gaus mean : 42.7800**

**Gaus Width: 2.8726**

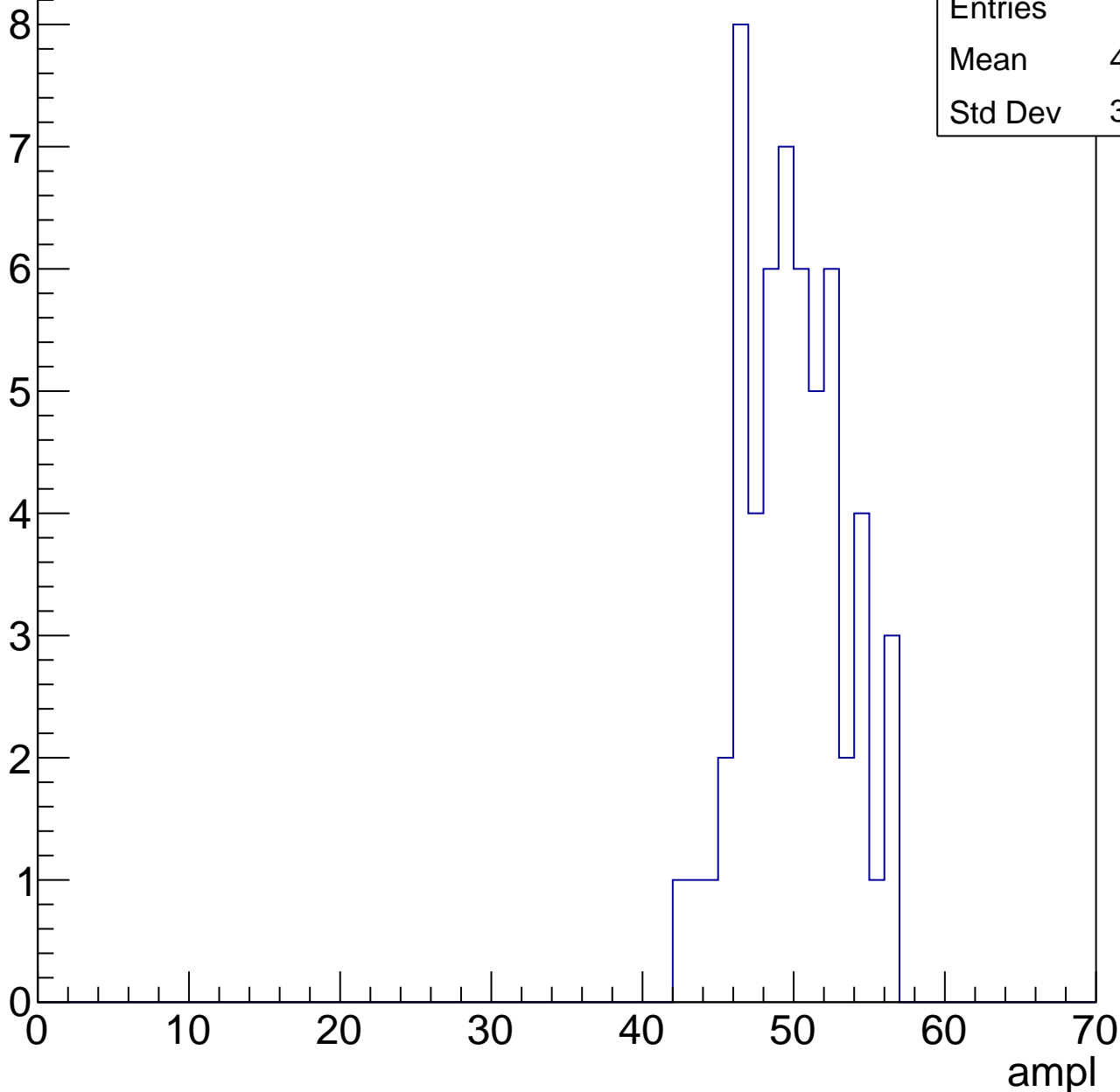


# B1L101S, U9-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	49.44
Std Dev	3.298

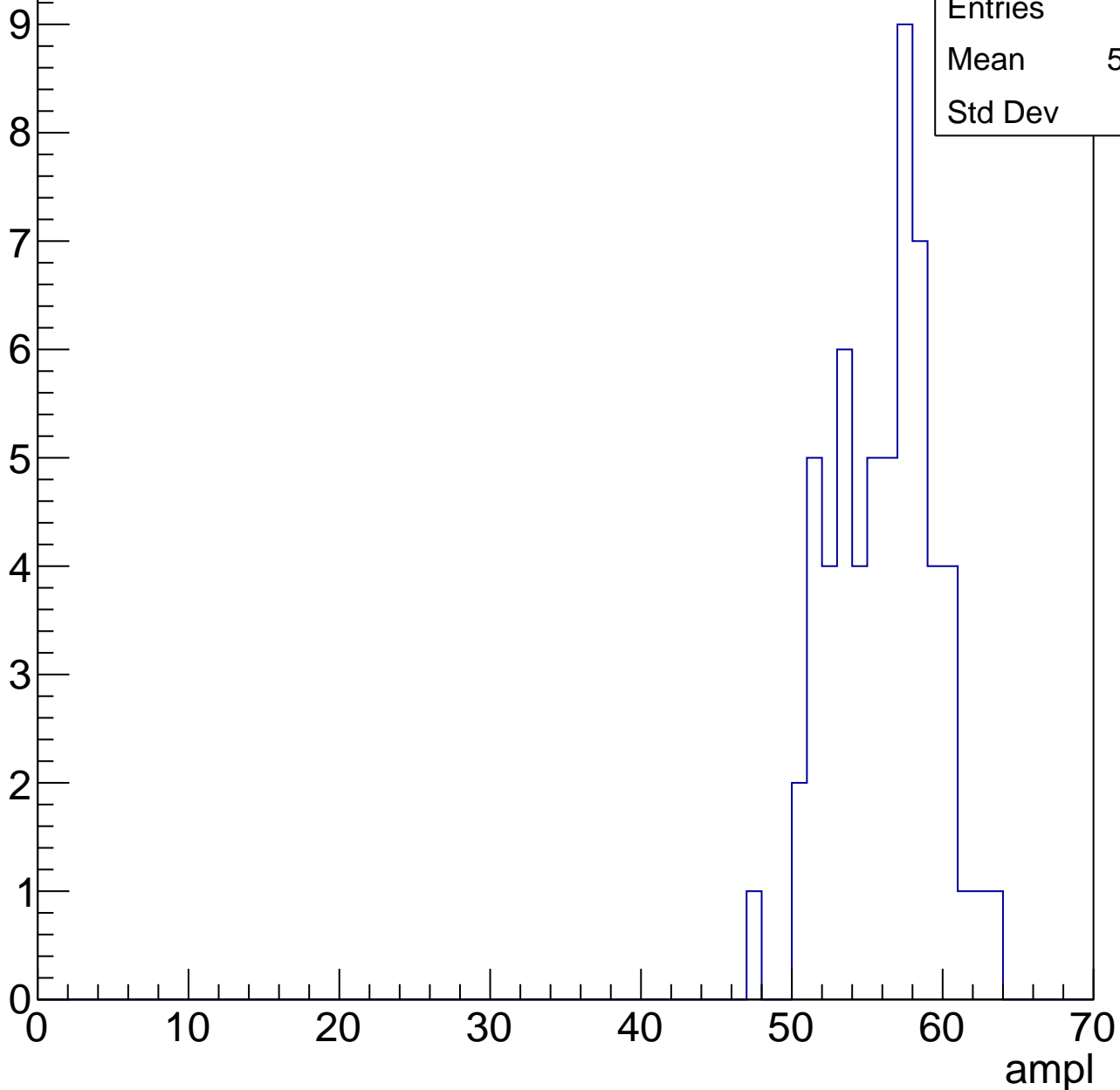


# B1L101S, U9-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	55.59
Std Dev	3.33

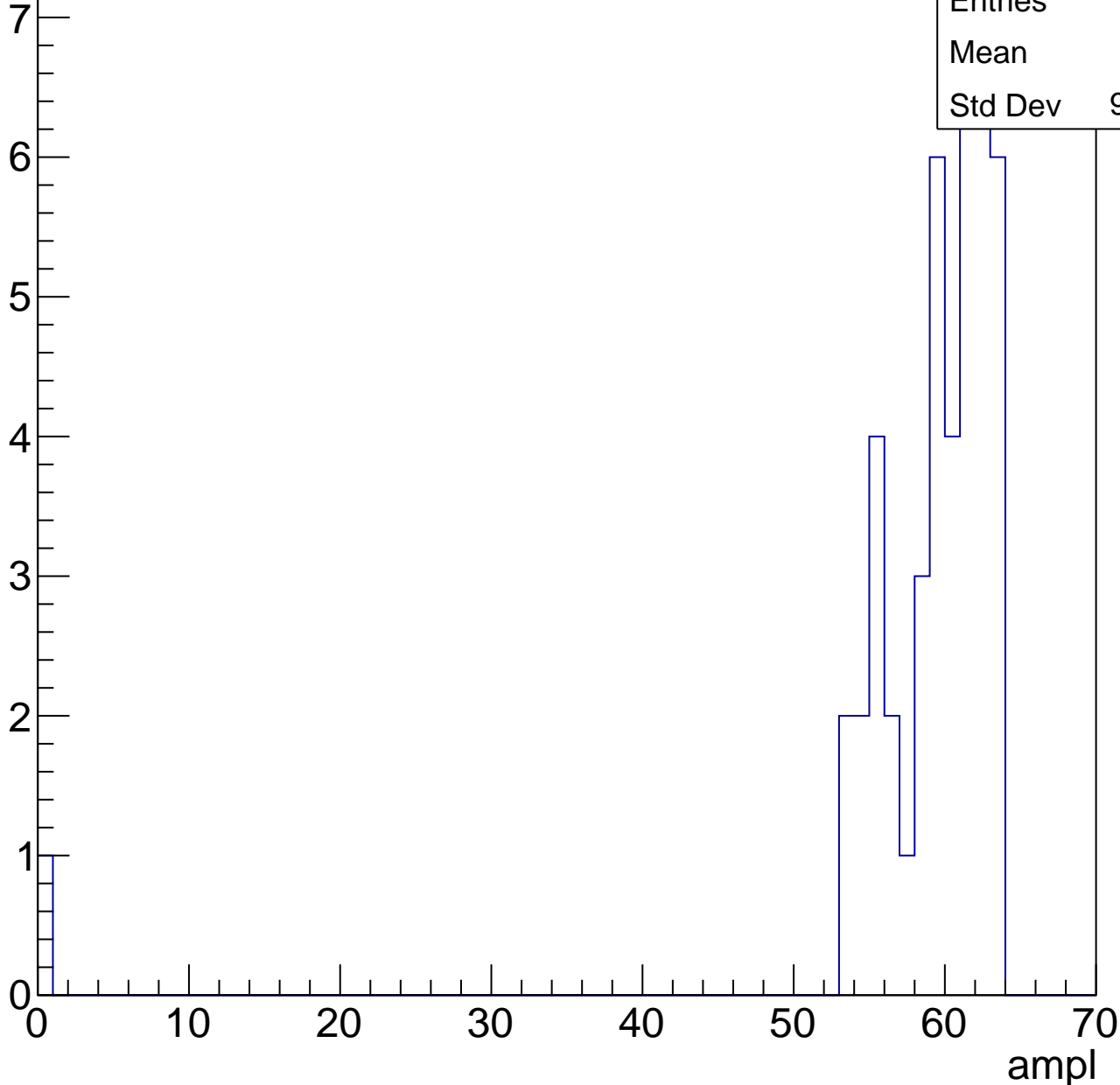


# B1L101S, U9-ch34, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

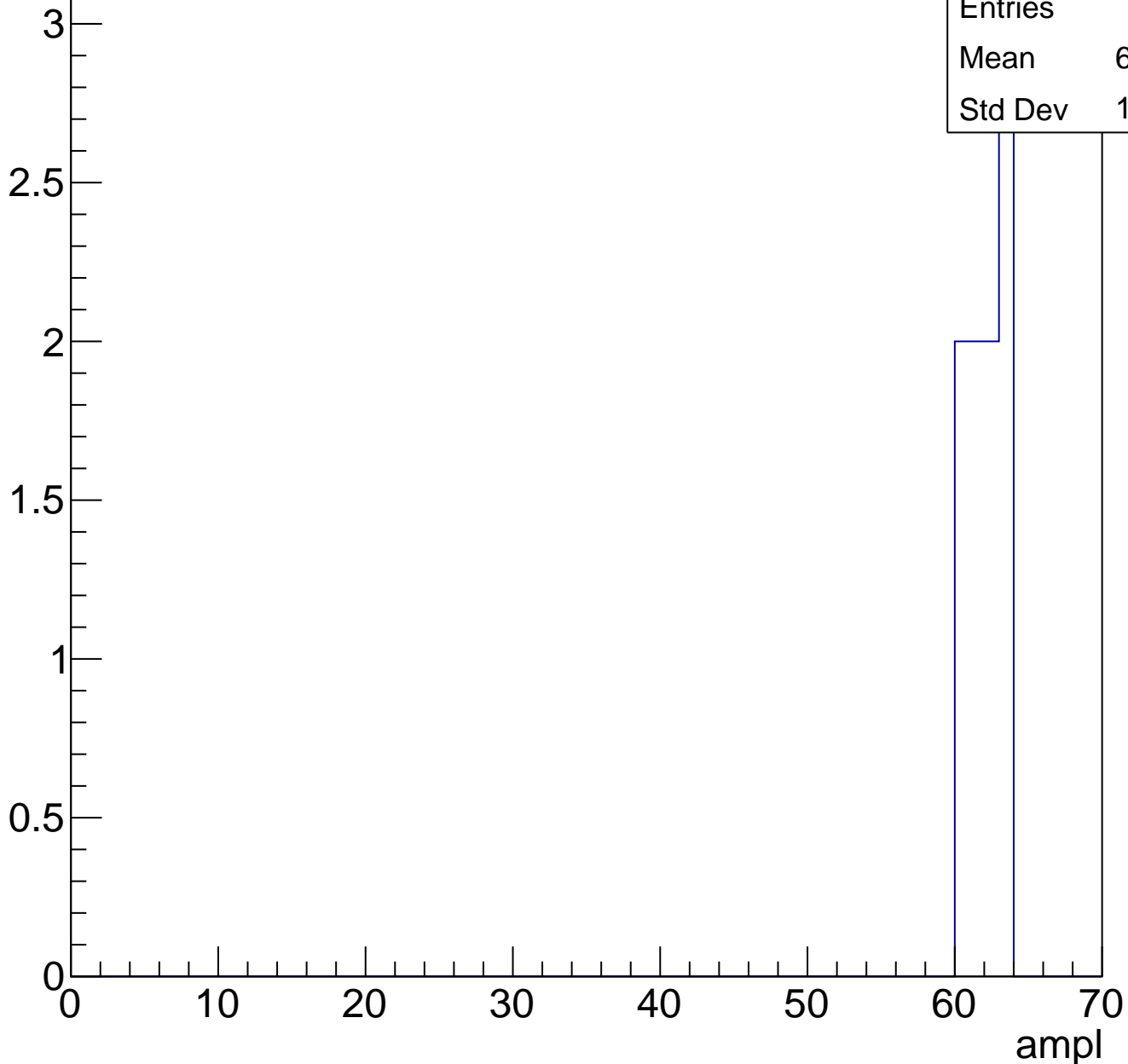
Entries	45
Mean	58
Std Dev	9.235



# B1L101S, U9-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch35, adc0

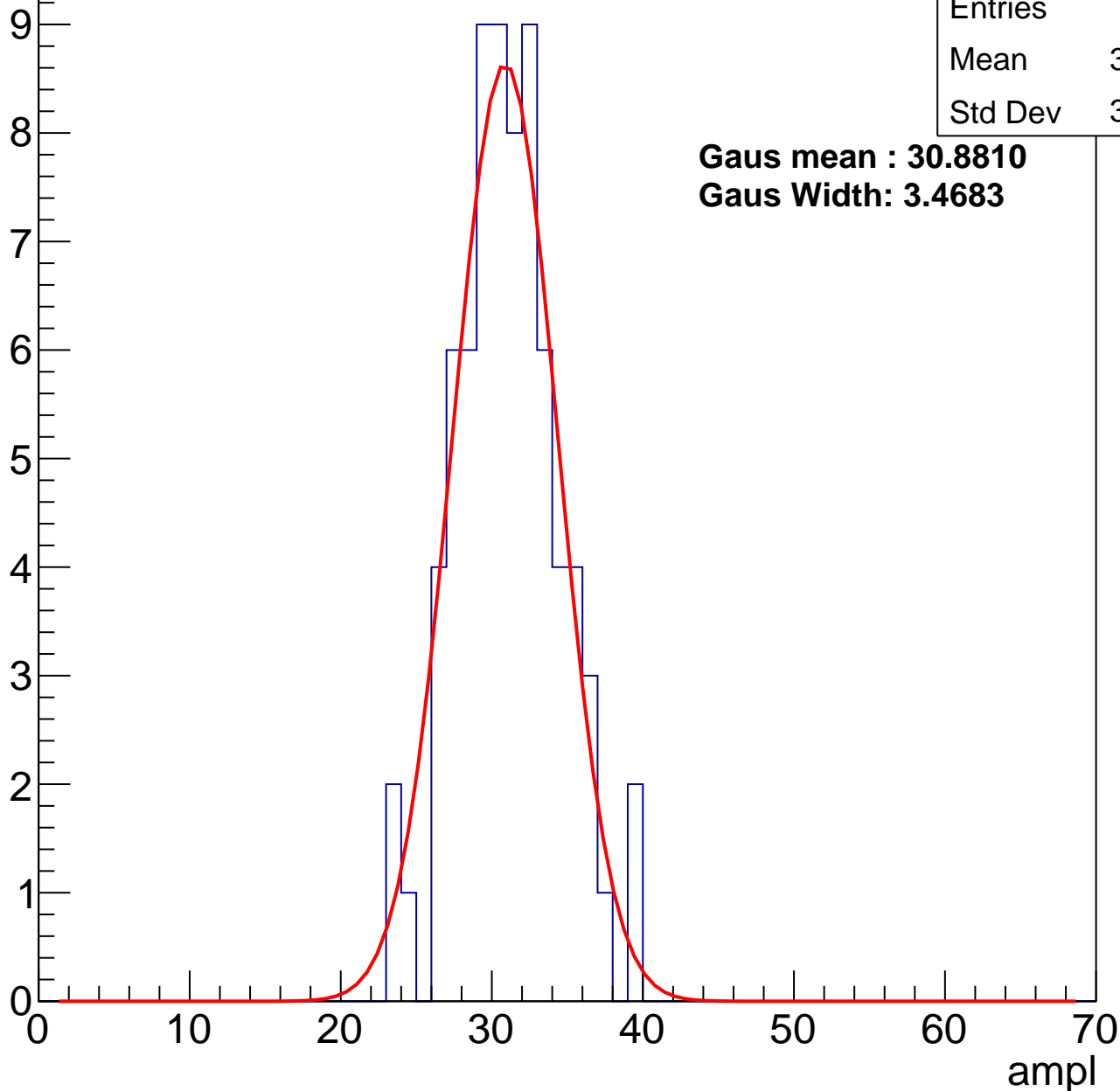
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	30.65
Std Dev	3.359

**Gaus mean : 30.8810**

**Gaus Width: 3.4683**



# B1L101S, U9-ch35, adc1

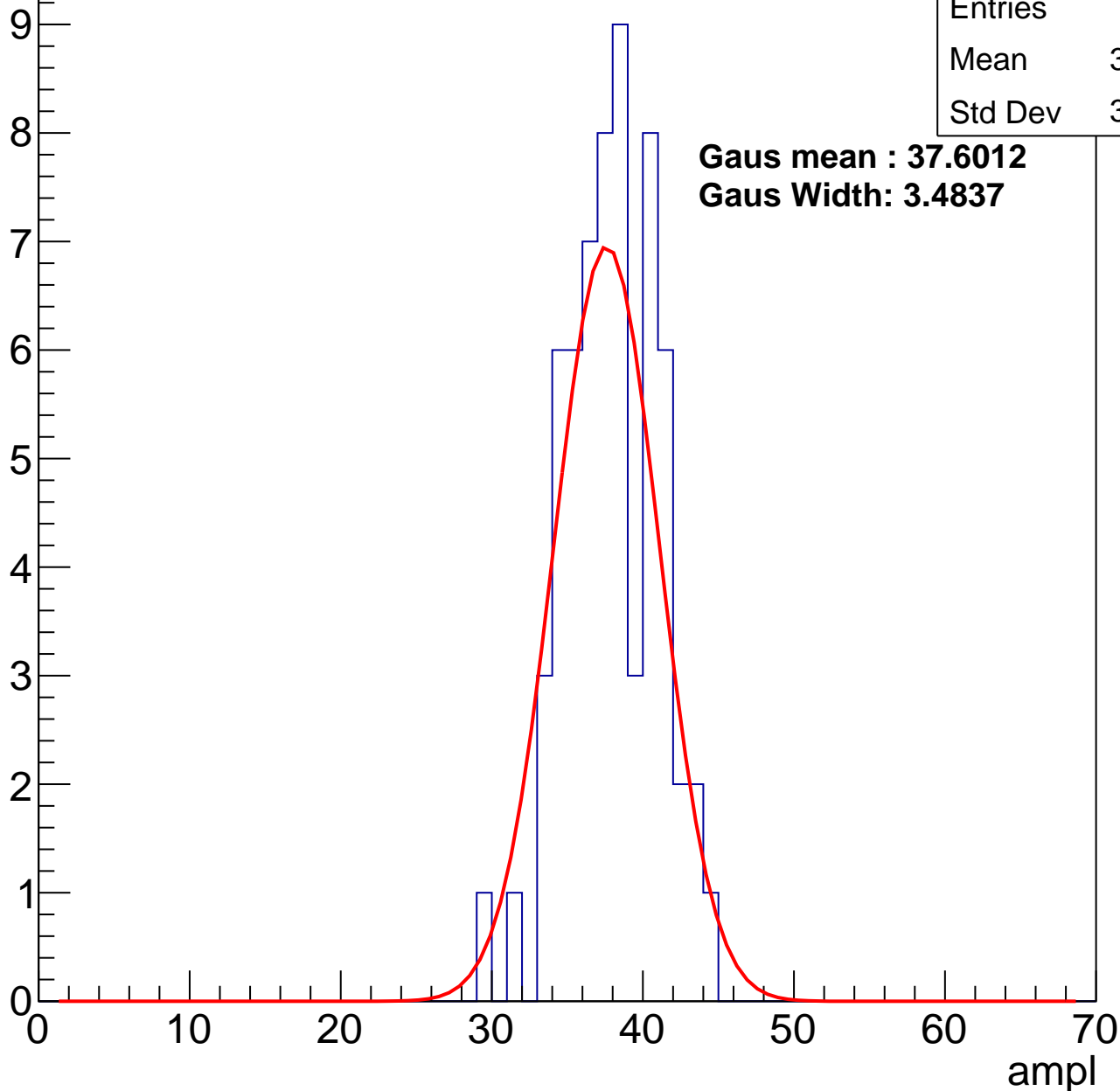
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	37.46
Std Dev	3.033

**Gaus mean : 37.6012**

**Gaus Width: 3.4837**



# B1L101S, U9-ch35, adc2

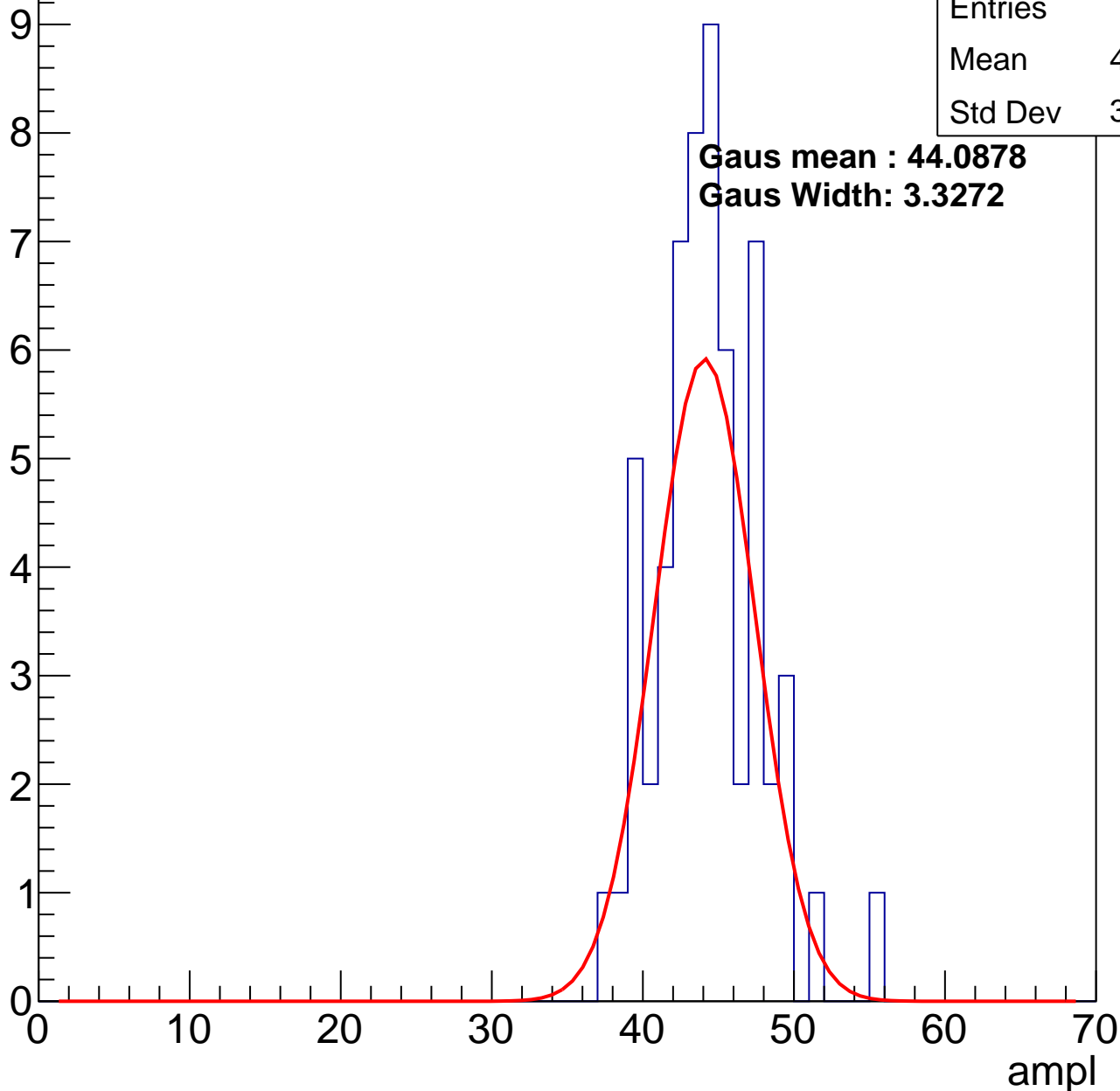
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	43.86
Std Dev	3.362

**Gaus mean : 44.0878**

**Gaus Width: 3.3272**

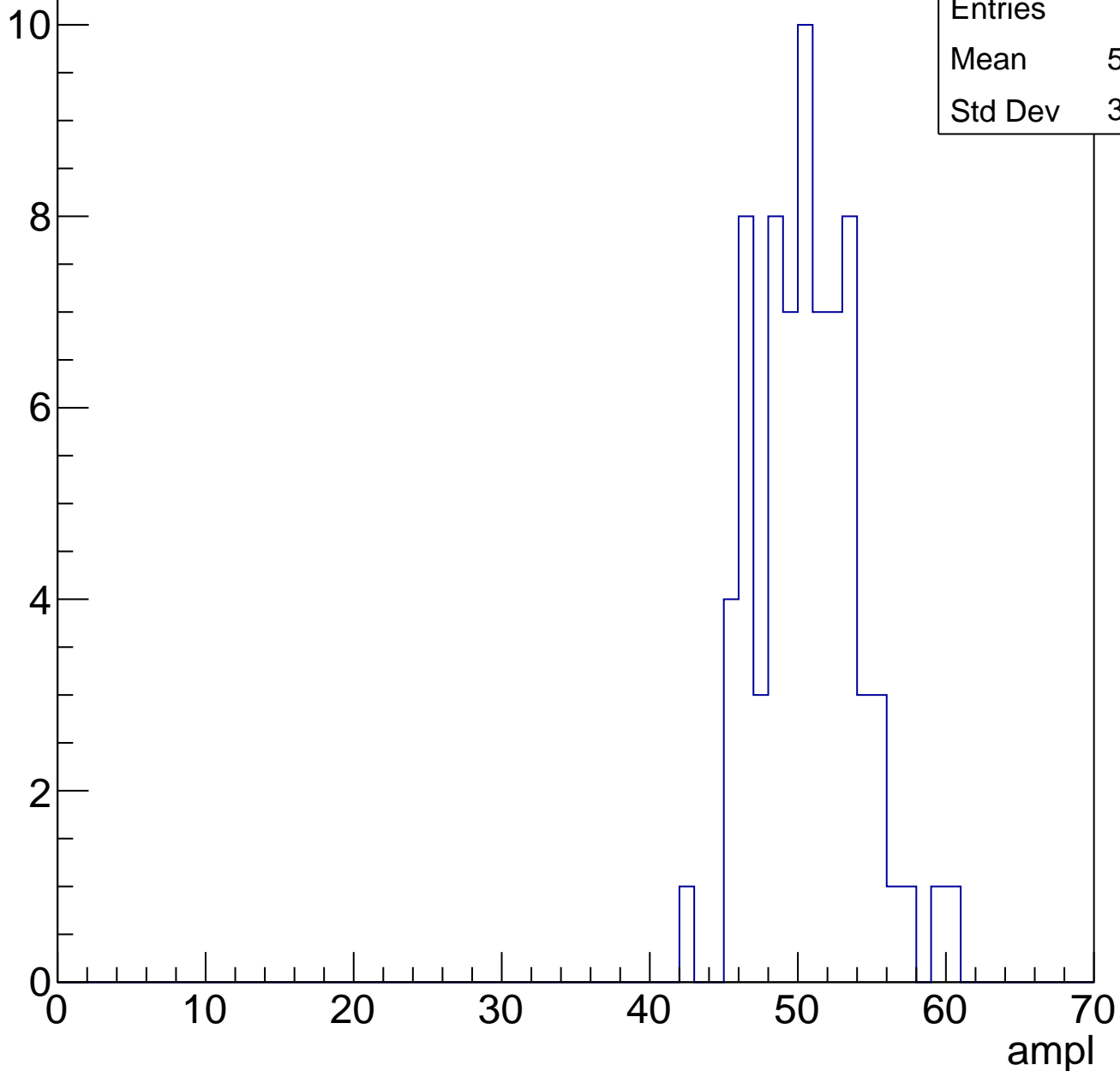


# B1L101S, U9-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	73
Mean	50.16
Std Dev	3.416

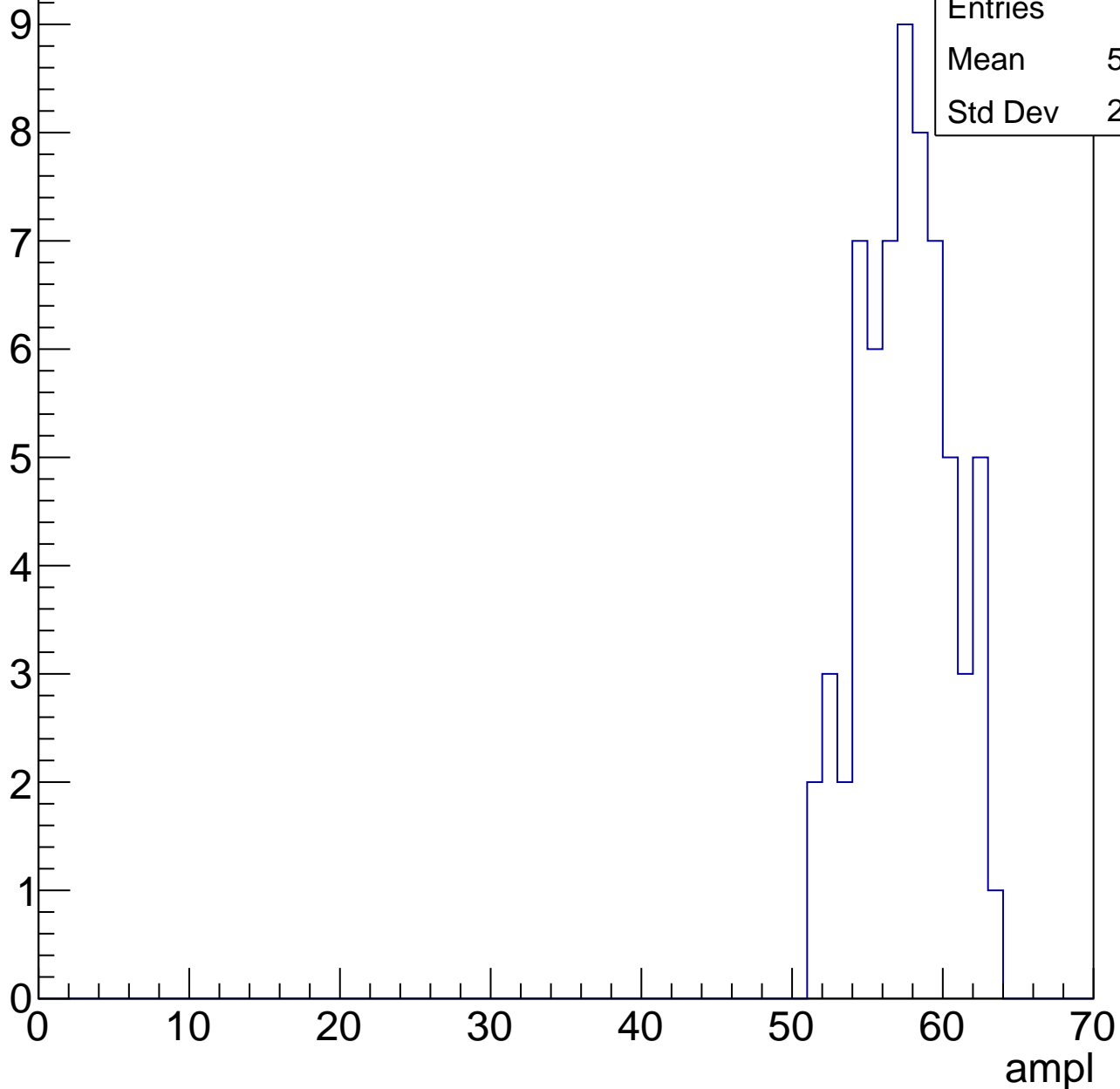
Entry



# B1L101S, U9-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



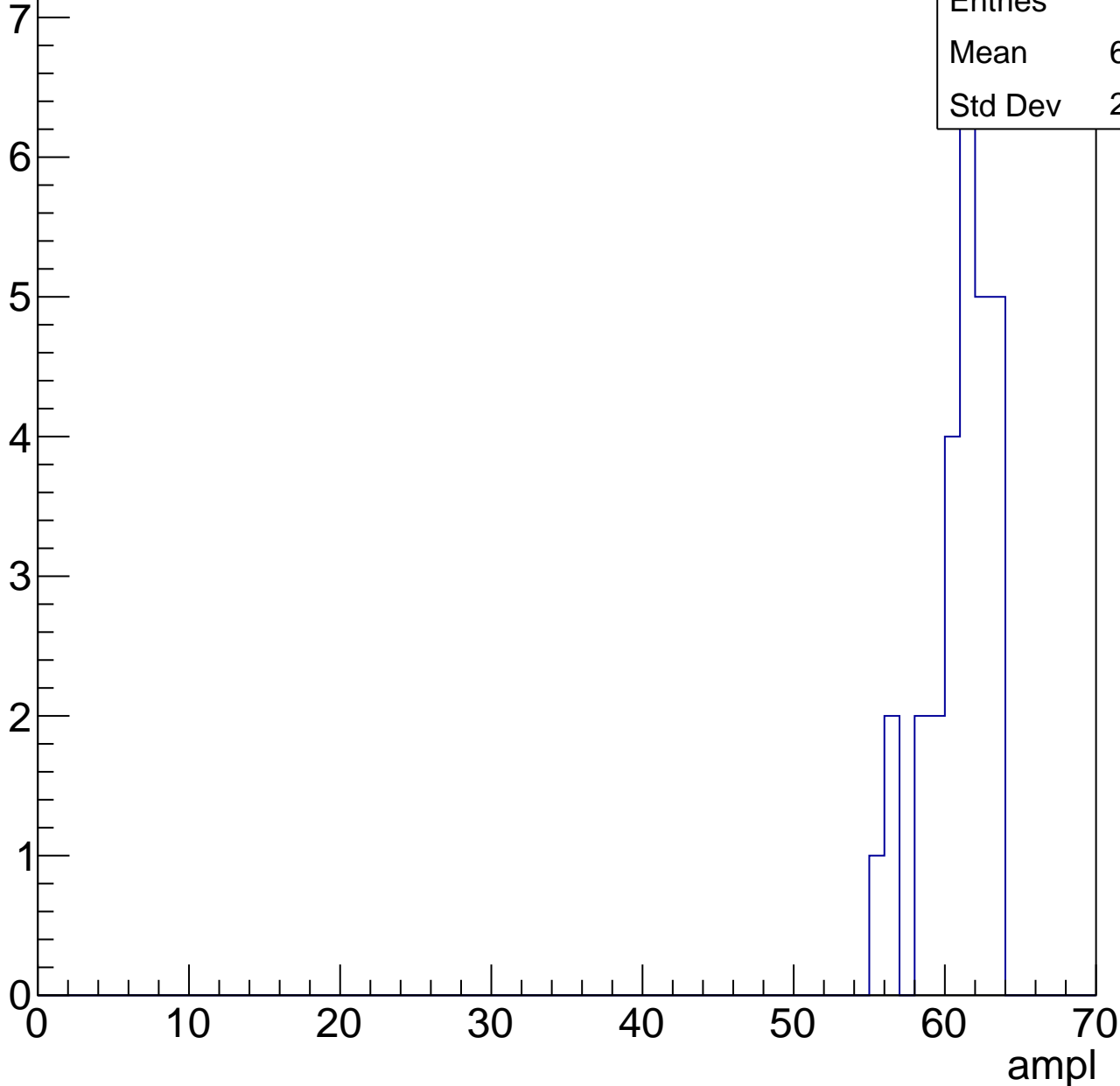
Entries	65
Mean	57.08
Std Dev	2.942

# B1L101S, U9-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

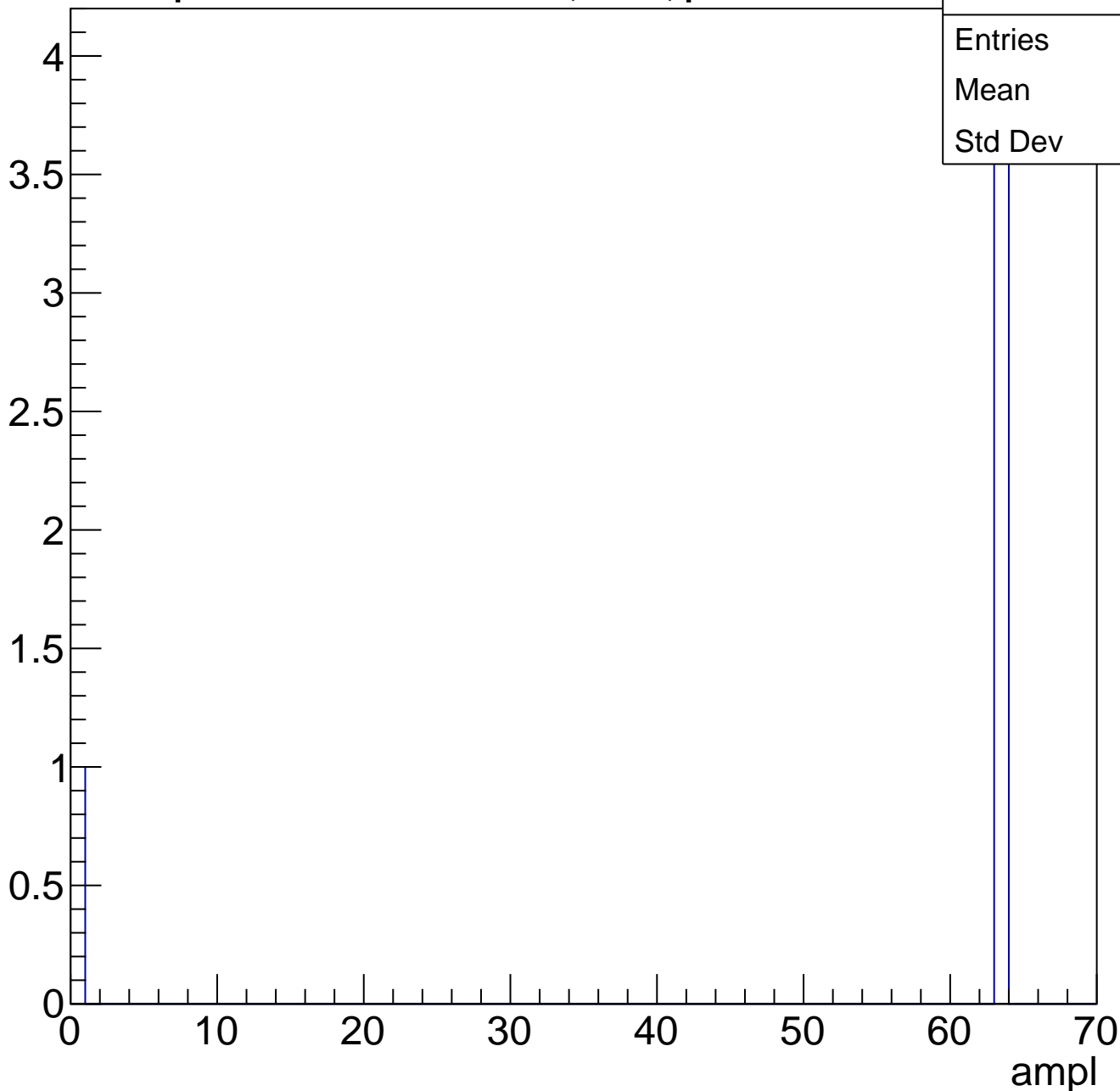
Entries	28
Mean	60.46
Std Dev	2.179



# B1L101S, U9-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U9-ch36, adc0

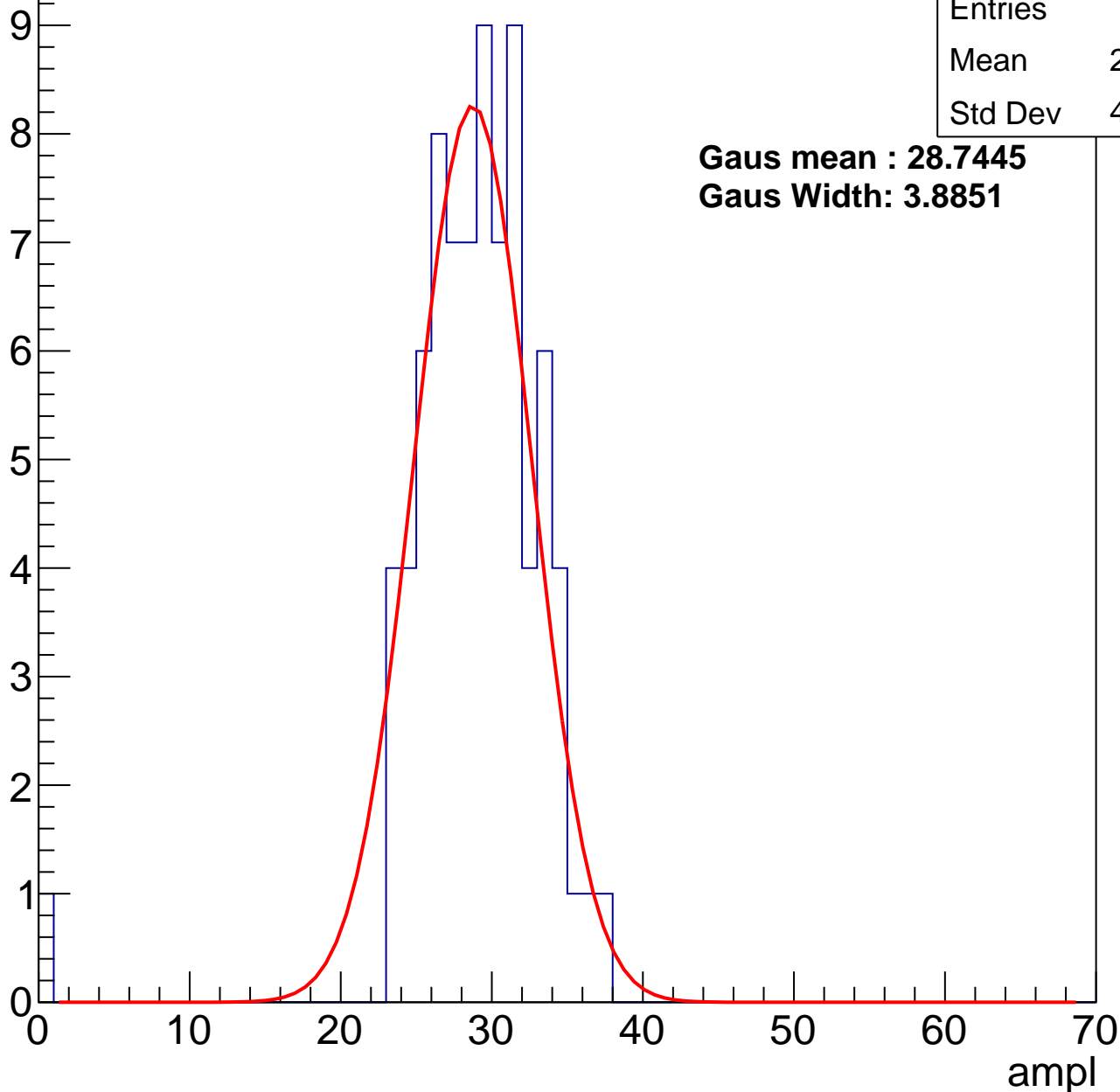
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	28.49
Std Dev	4.628

**Gaus mean : 28.7445**

**Gaus Width: 3.8851**



# B1L101S, U9-ch36, adc1

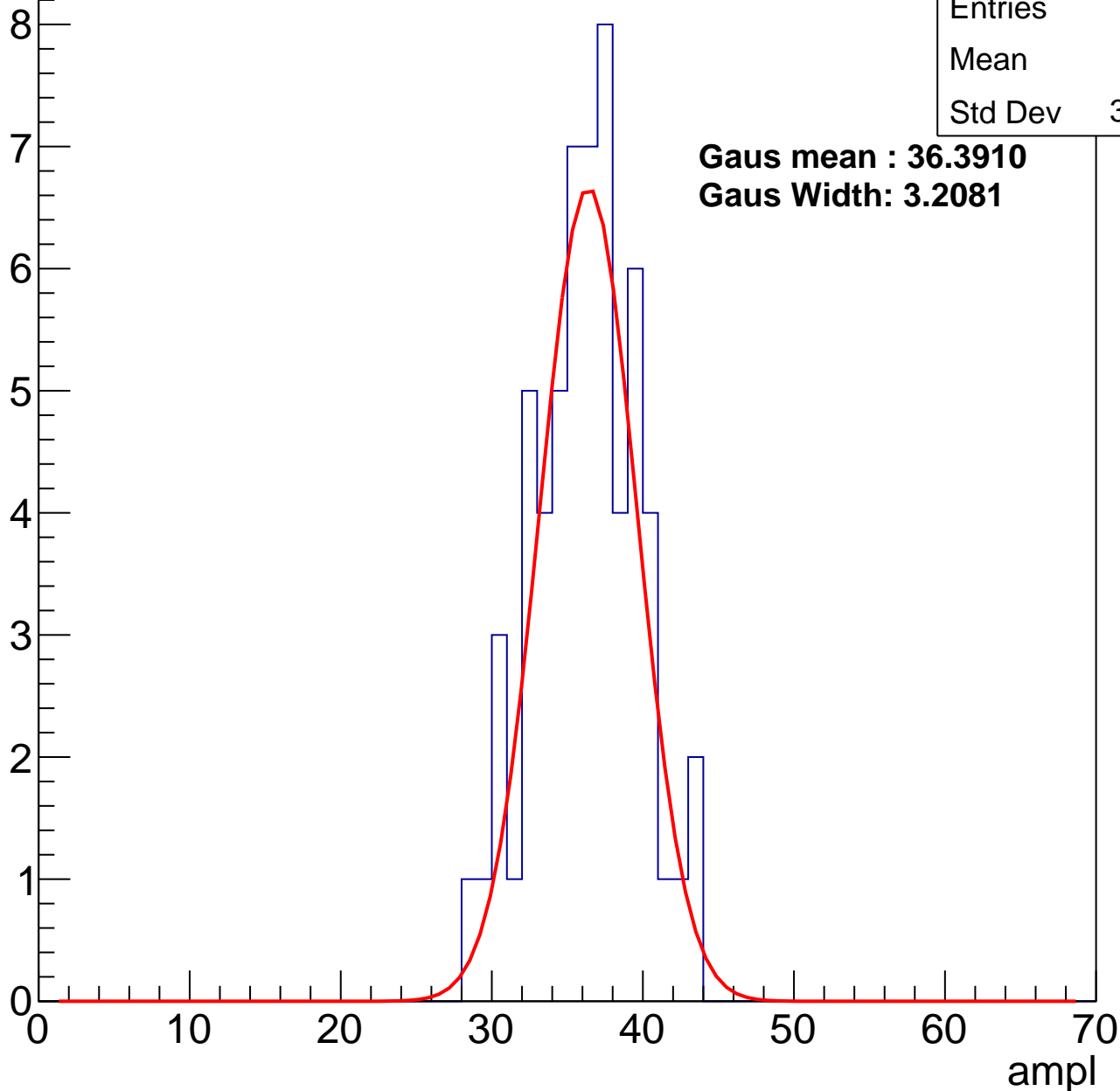
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	35.8
Std Dev	3.385

**Gaus mean : 36.3910**

**Gaus Width: 3.2081**



# B1L101S, U9-ch36, adc2

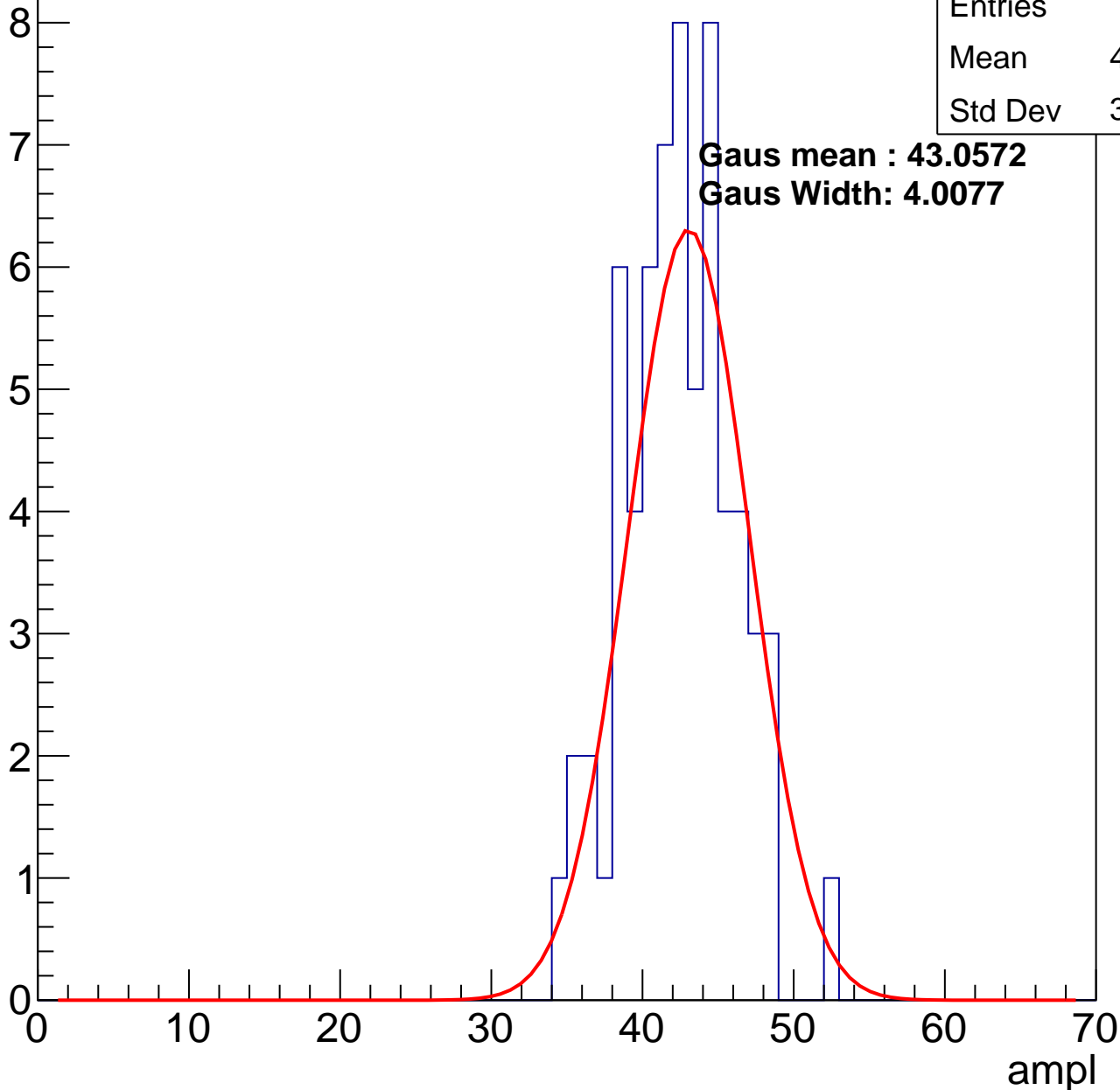
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	41.97
Std Dev	3.599

**Gaus mean : 43.0572**

**Gaus Width: 4.0077**

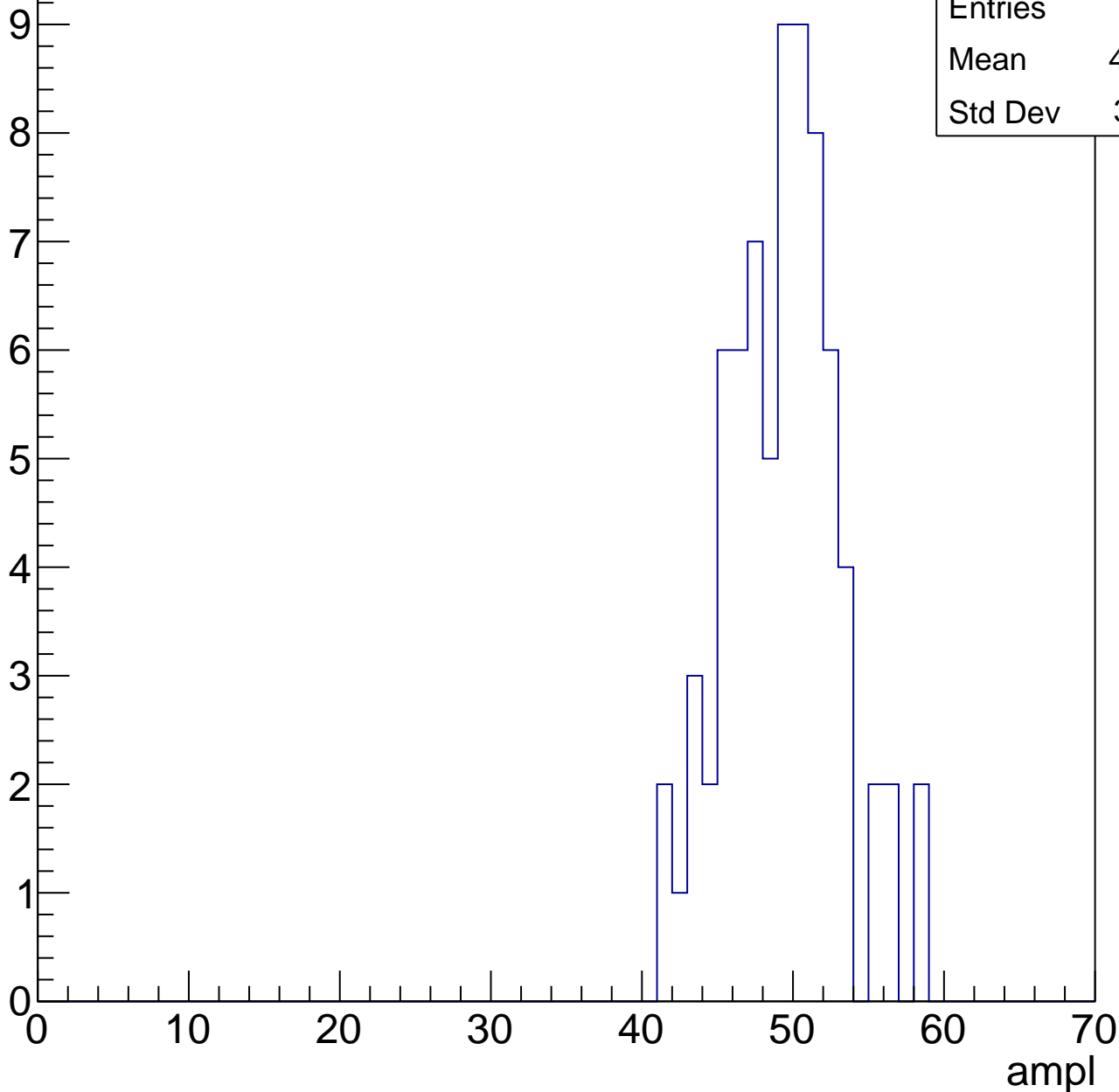


# B1L101S, U9-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	48.88
Std Dev	3.691

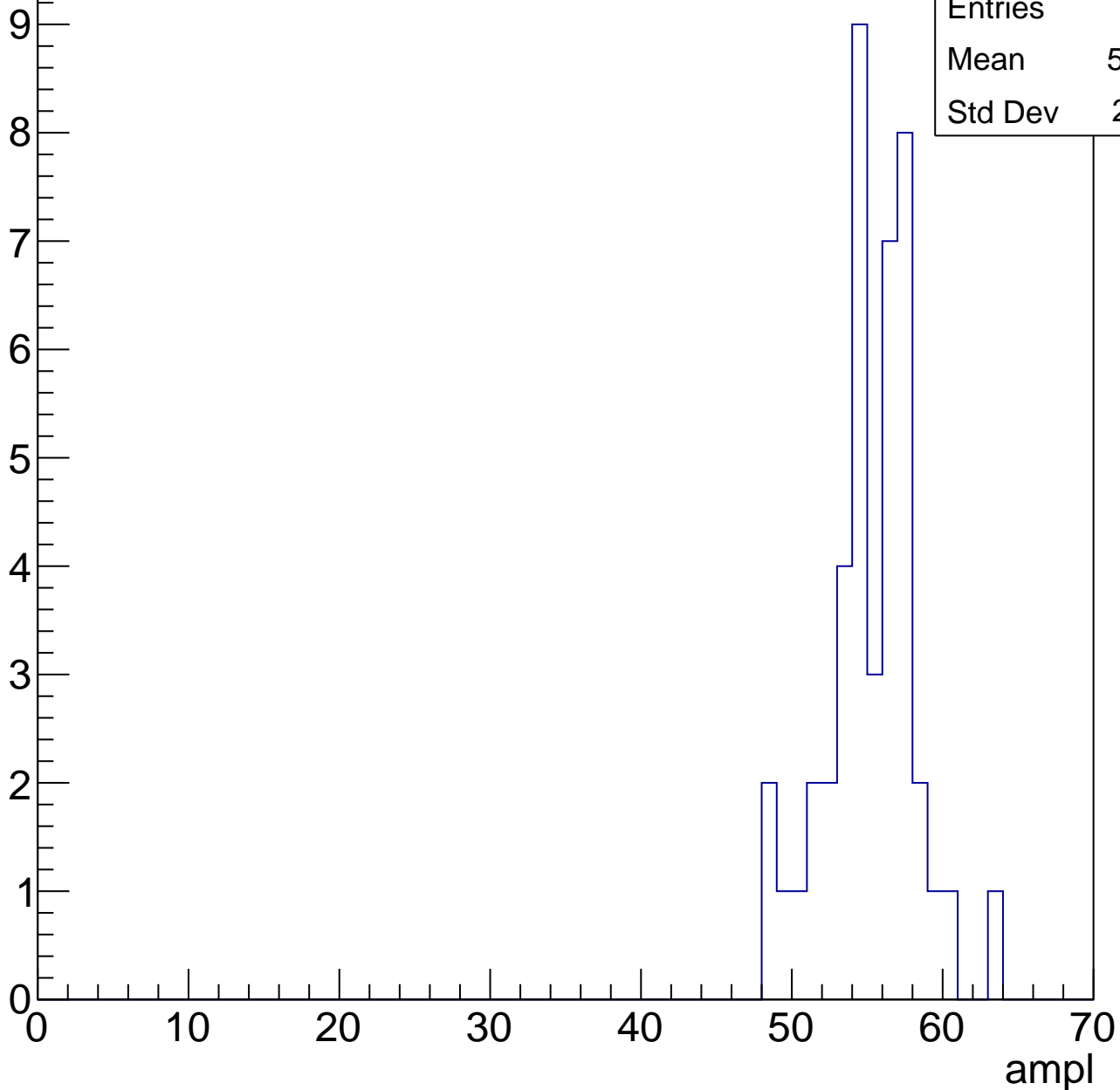


# B1L101S, U9-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	44
Mean	54.77
Std Dev	2.991

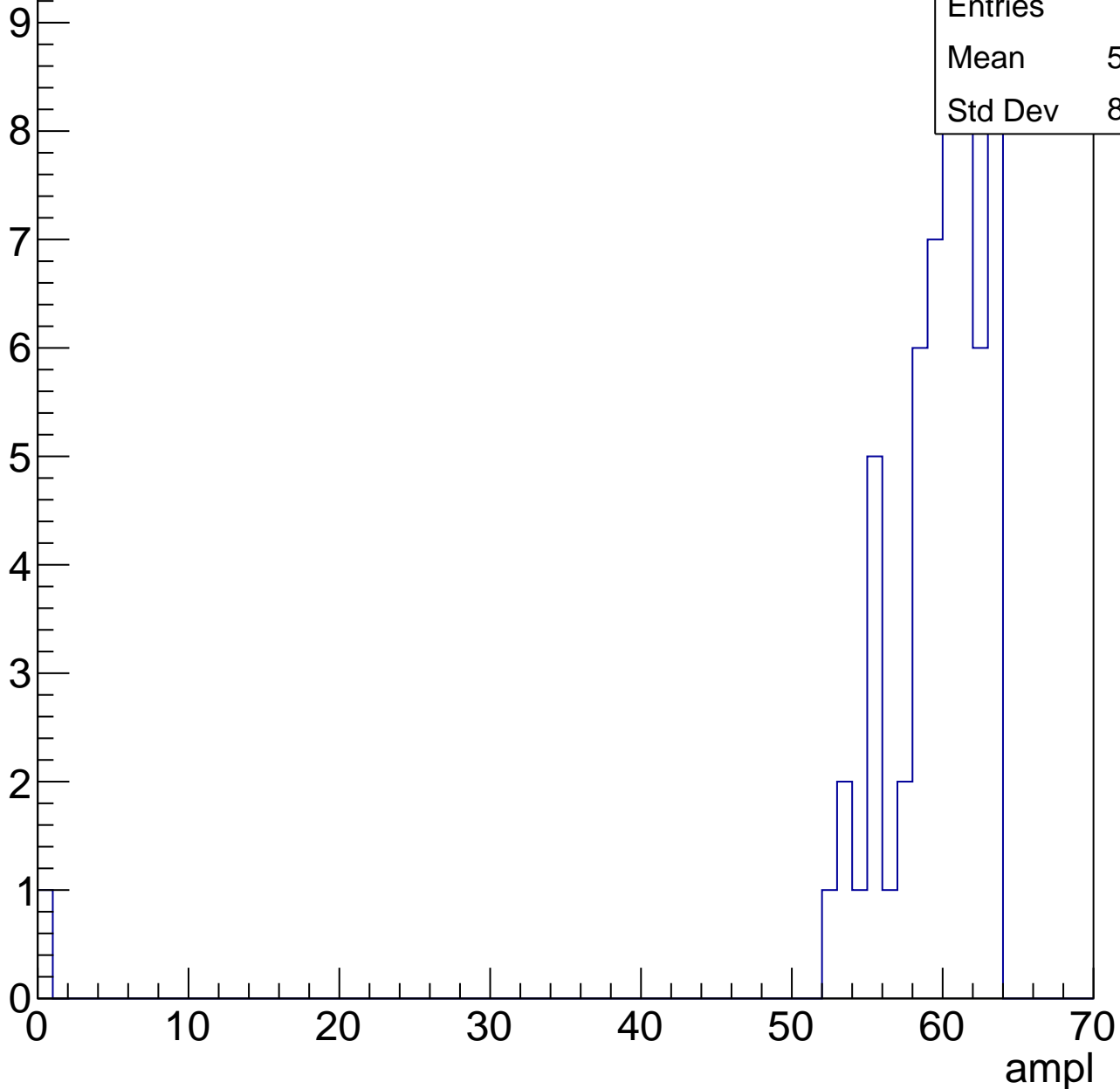


# B1L101S, U9-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

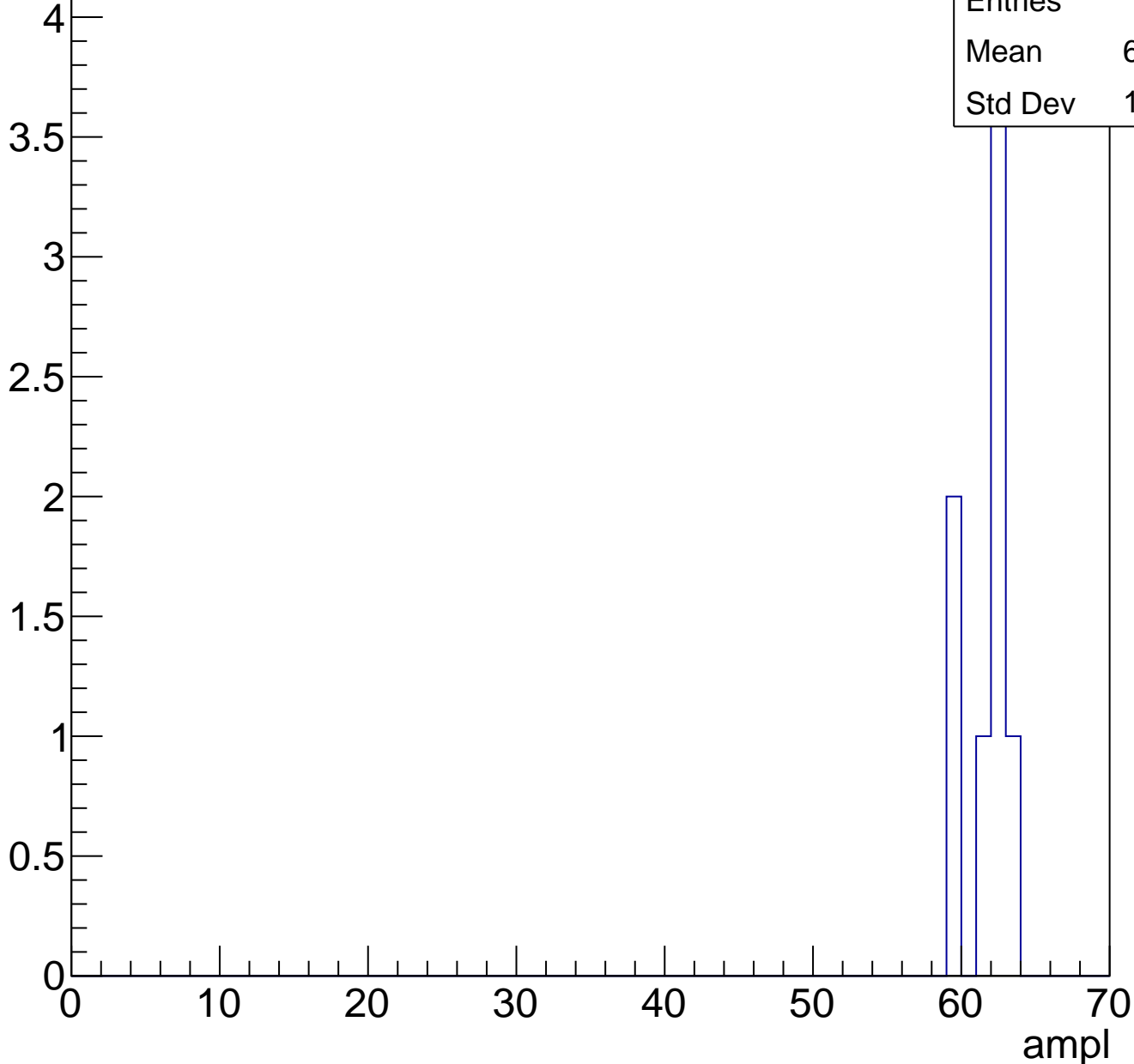
Entries	58
Mean	58.33
Std Dev	8.232



# B1L101S, U9-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U9-ch37, adc0

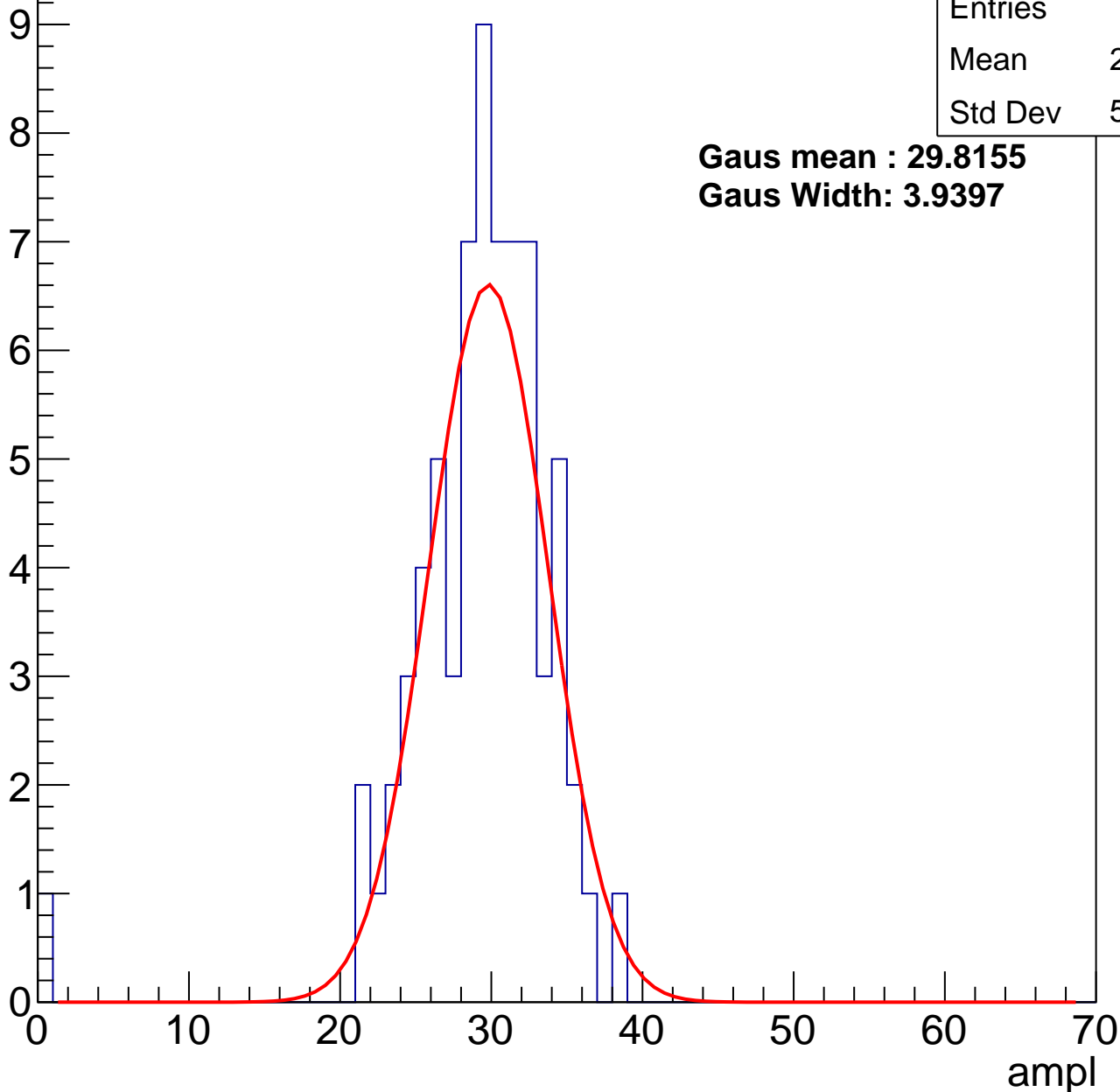
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	28.77
Std Dev	5.018

**Gaus mean : 29.8155**

**Gaus Width: 3.9397**



# B1L101S, U9-ch37, adc1

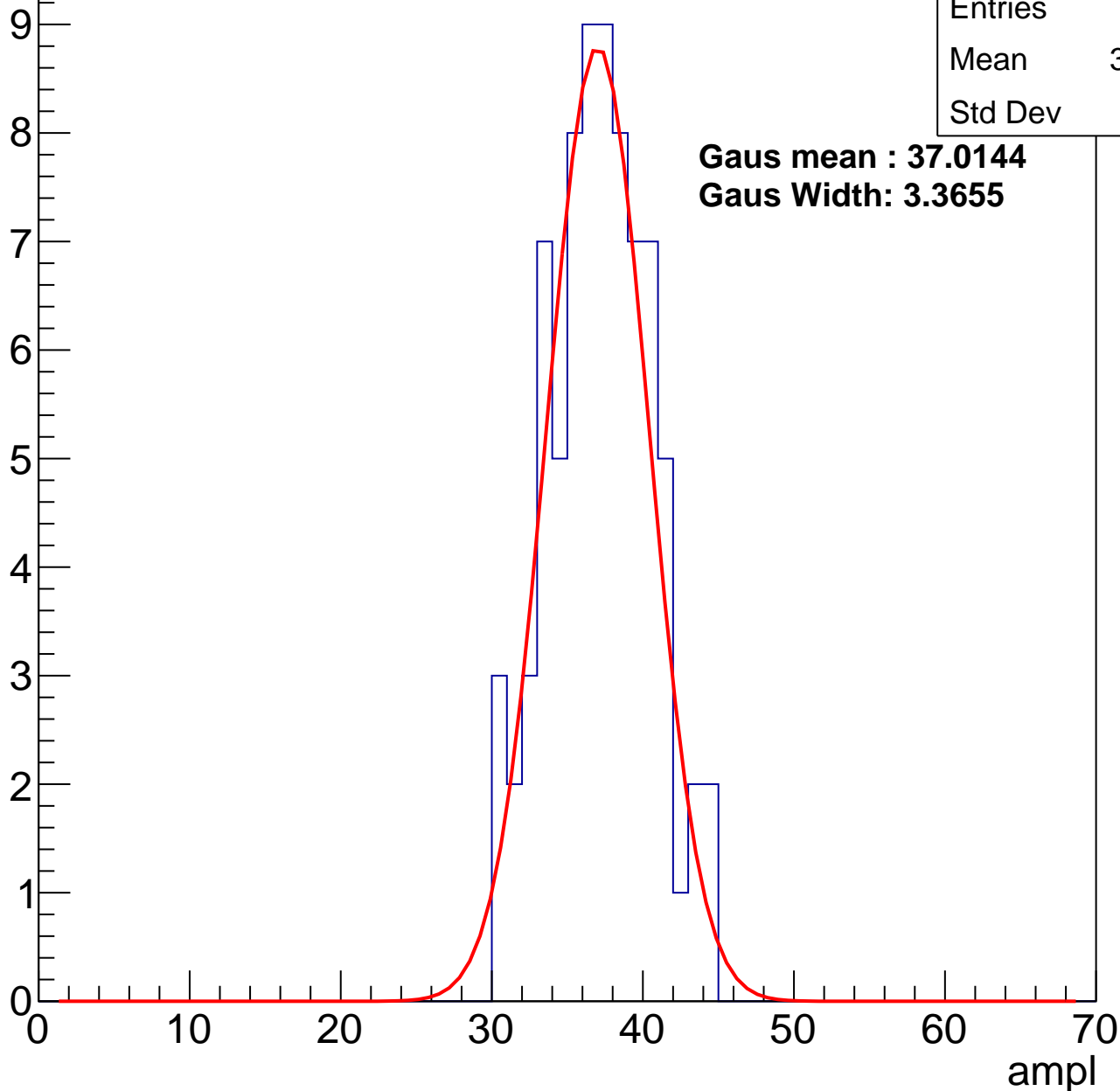
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	36.72
Std Dev	3.32

**Gaus mean : 37.0144**

**Gaus Width: 3.3655**



# B1L101S, U9-ch37, adc2

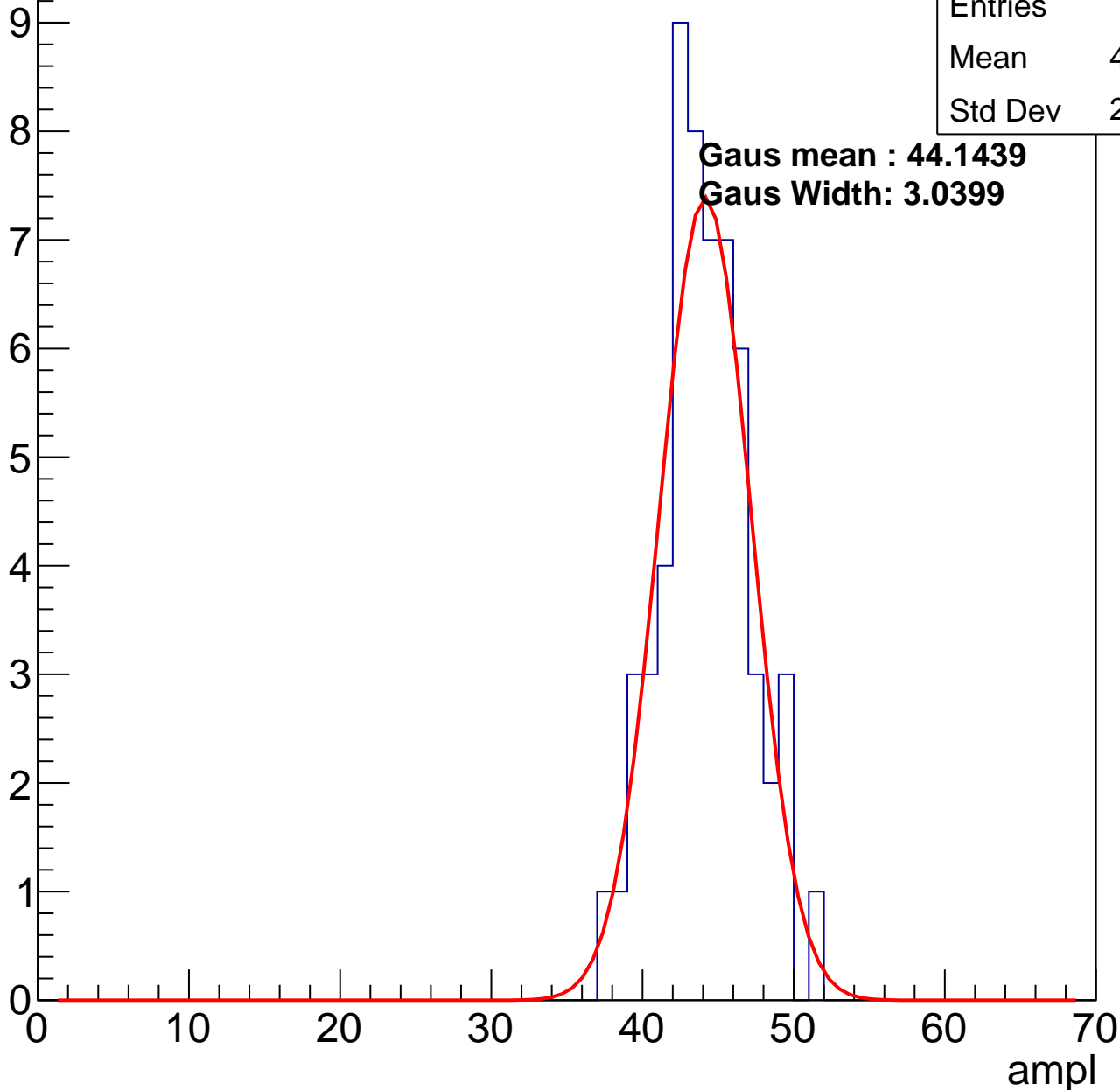
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	43.66
Std Dev	2.922

**Gaus mean : 44.1439**

**Gaus Width: 3.0399**



# B1L101S, U9-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	70
Mean	49.91
Std Dev	3.093

Entry

10

8

6

4

2

0

0

10

20

30

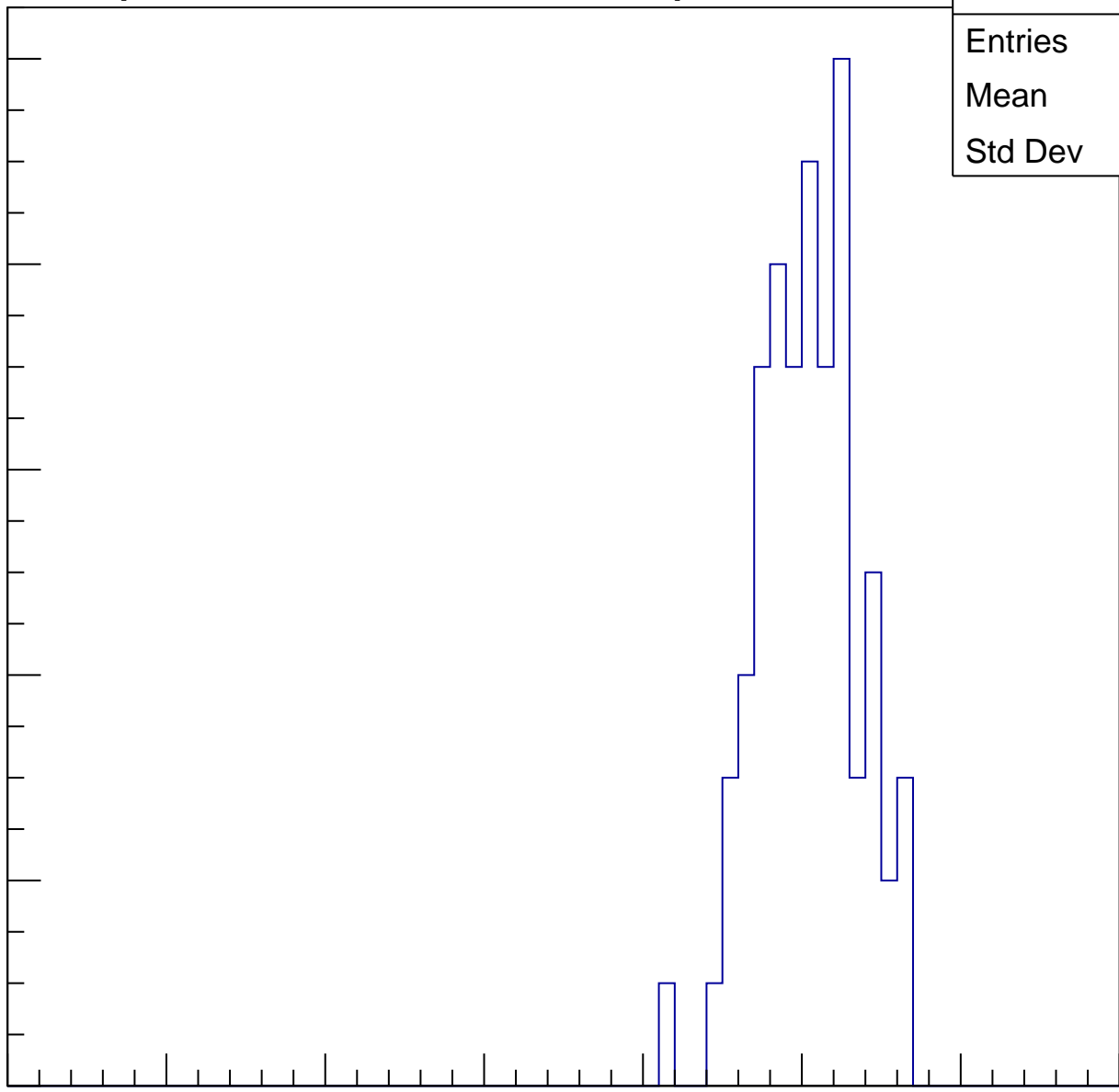
40

50

60

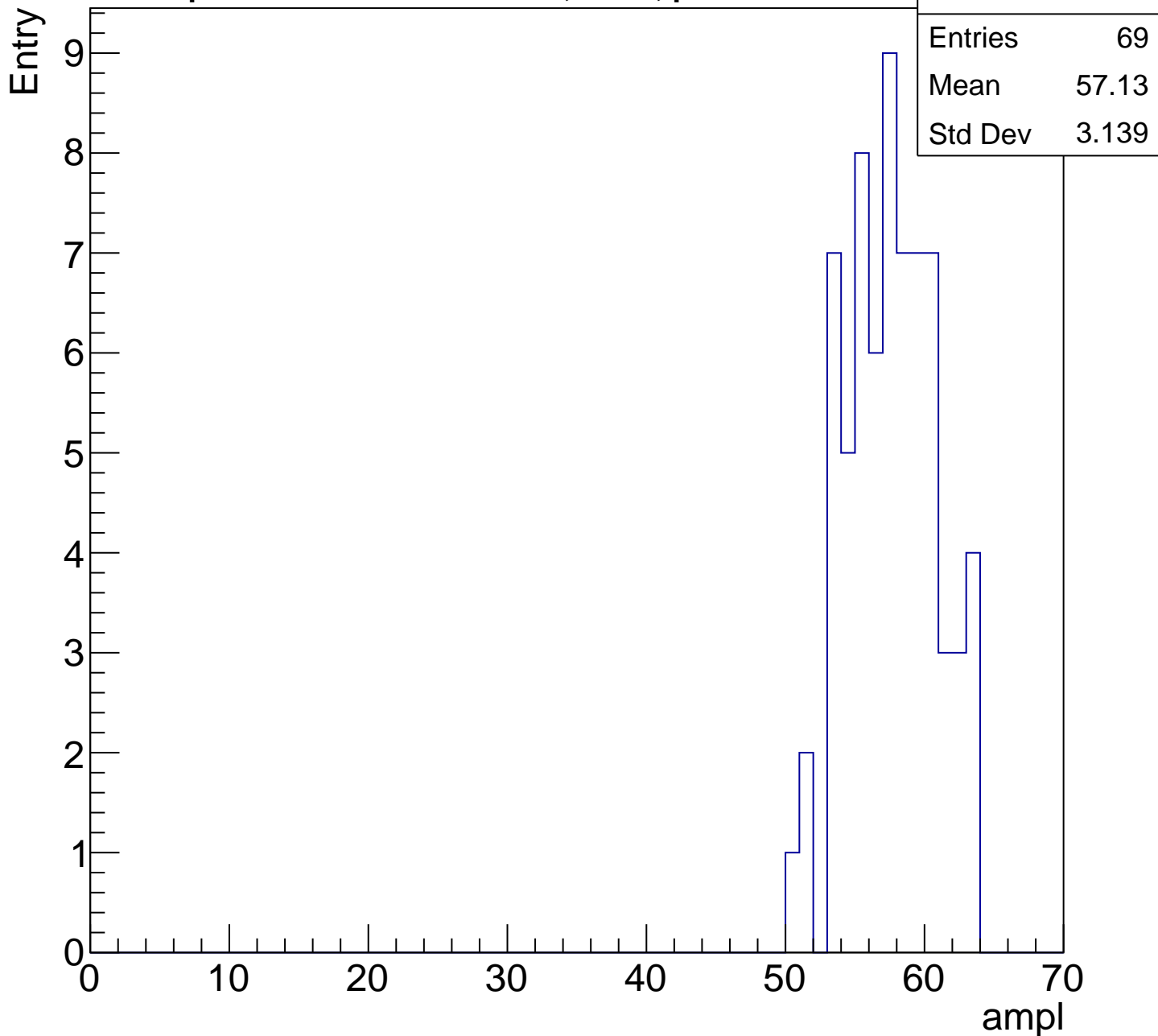
70

ampl



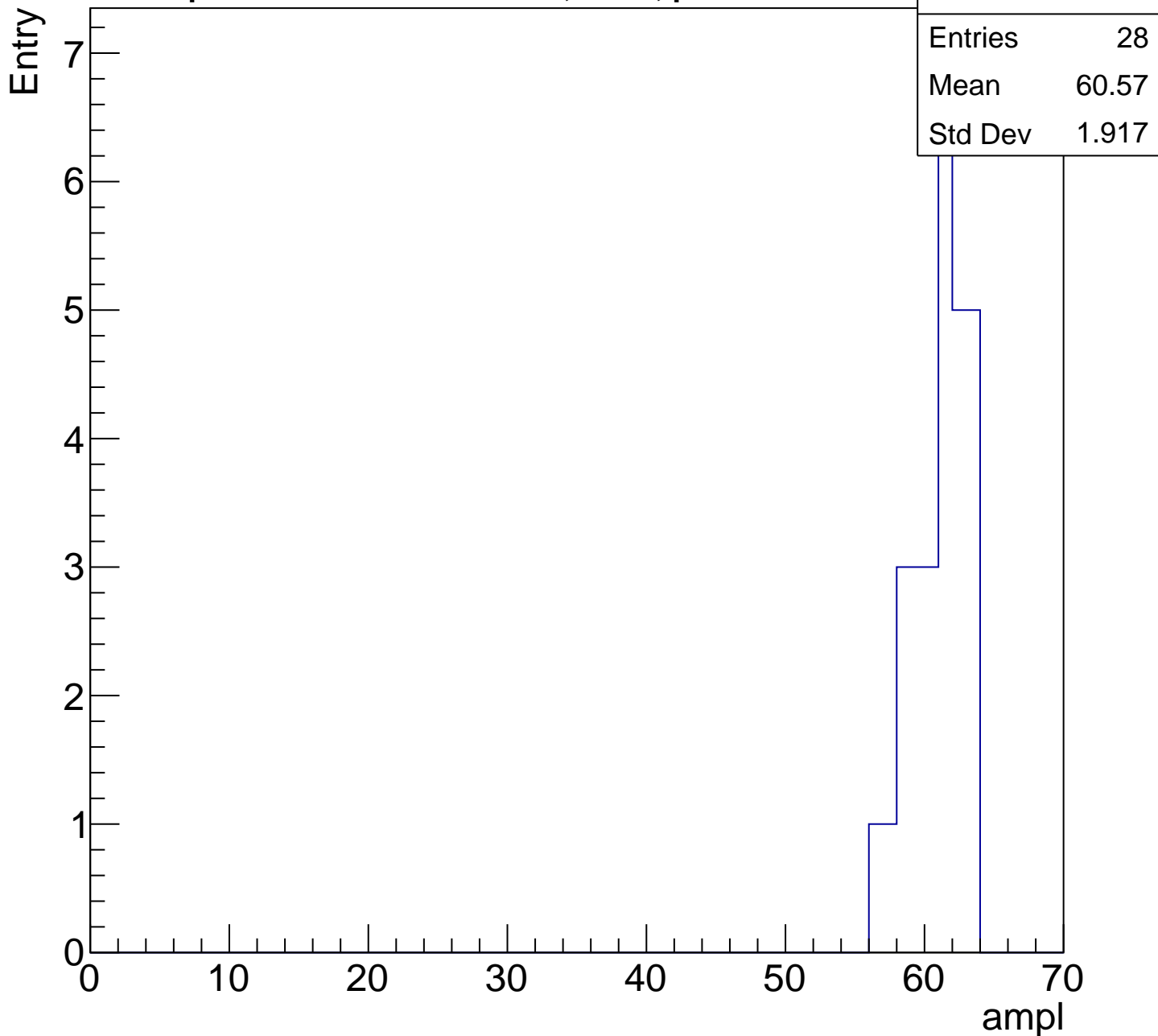
# B1L101S, U9-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U9-ch38, adc0

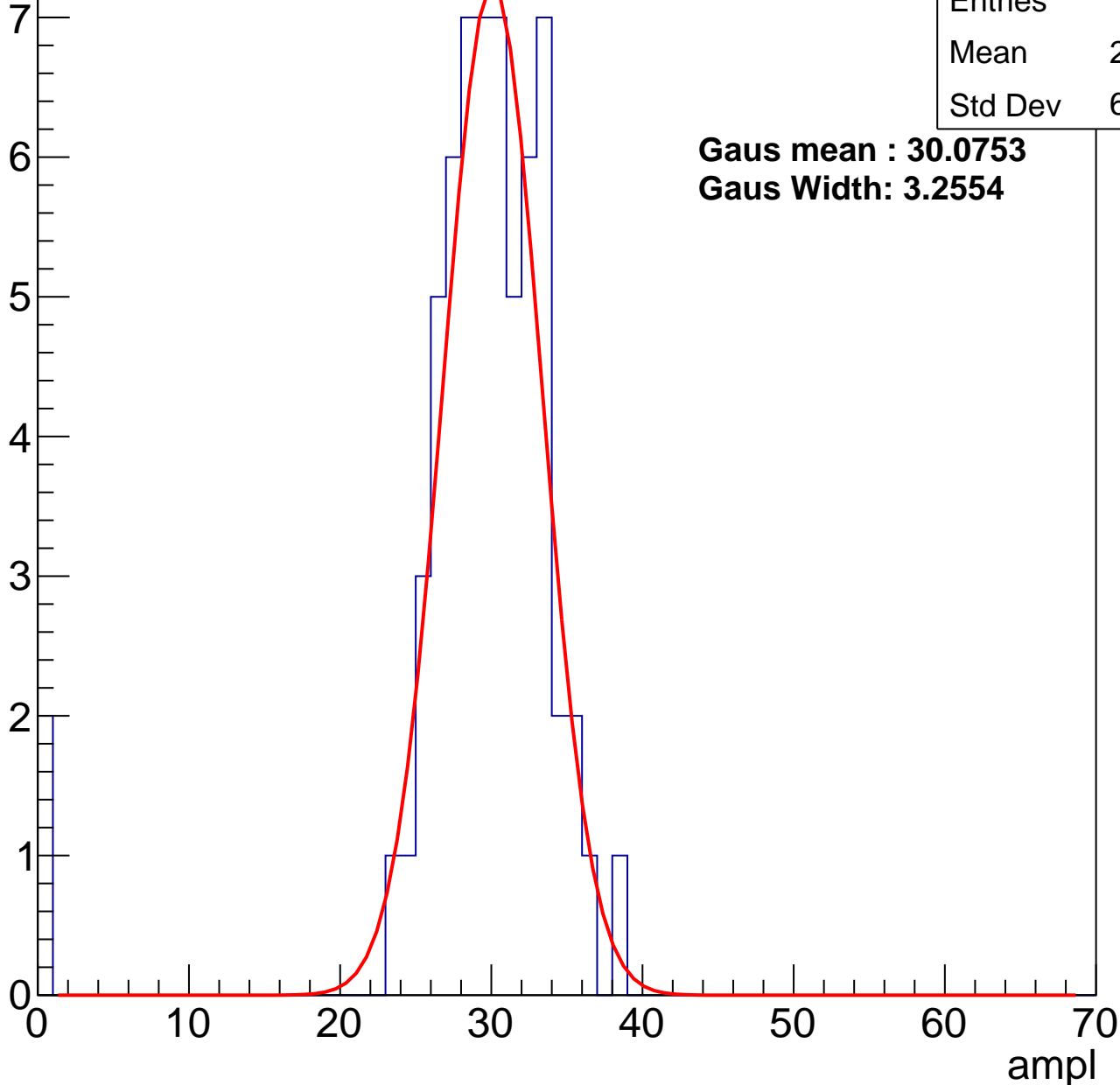
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	28.78
Std Dev	6.054

**Gaus mean : 30.0753**

**Gaus Width: 3.2554**



# B1L101S, U9-ch38, adc1

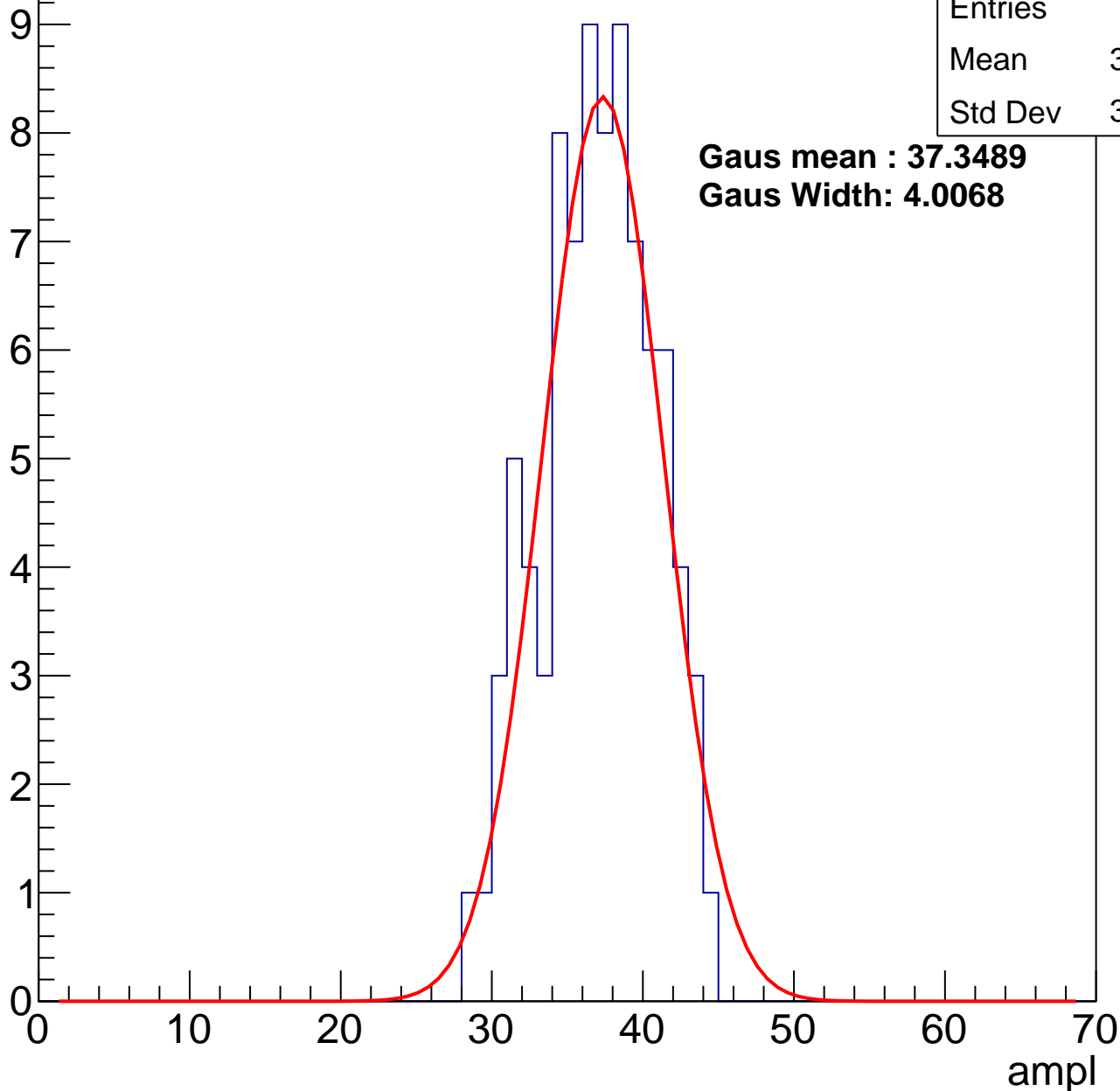
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	85
Mean	36.56
Std Dev	3.689

**Gaus mean : 37.3489**

**Gaus Width: 4.0068**



# B1L101S, U9-ch38, adc2

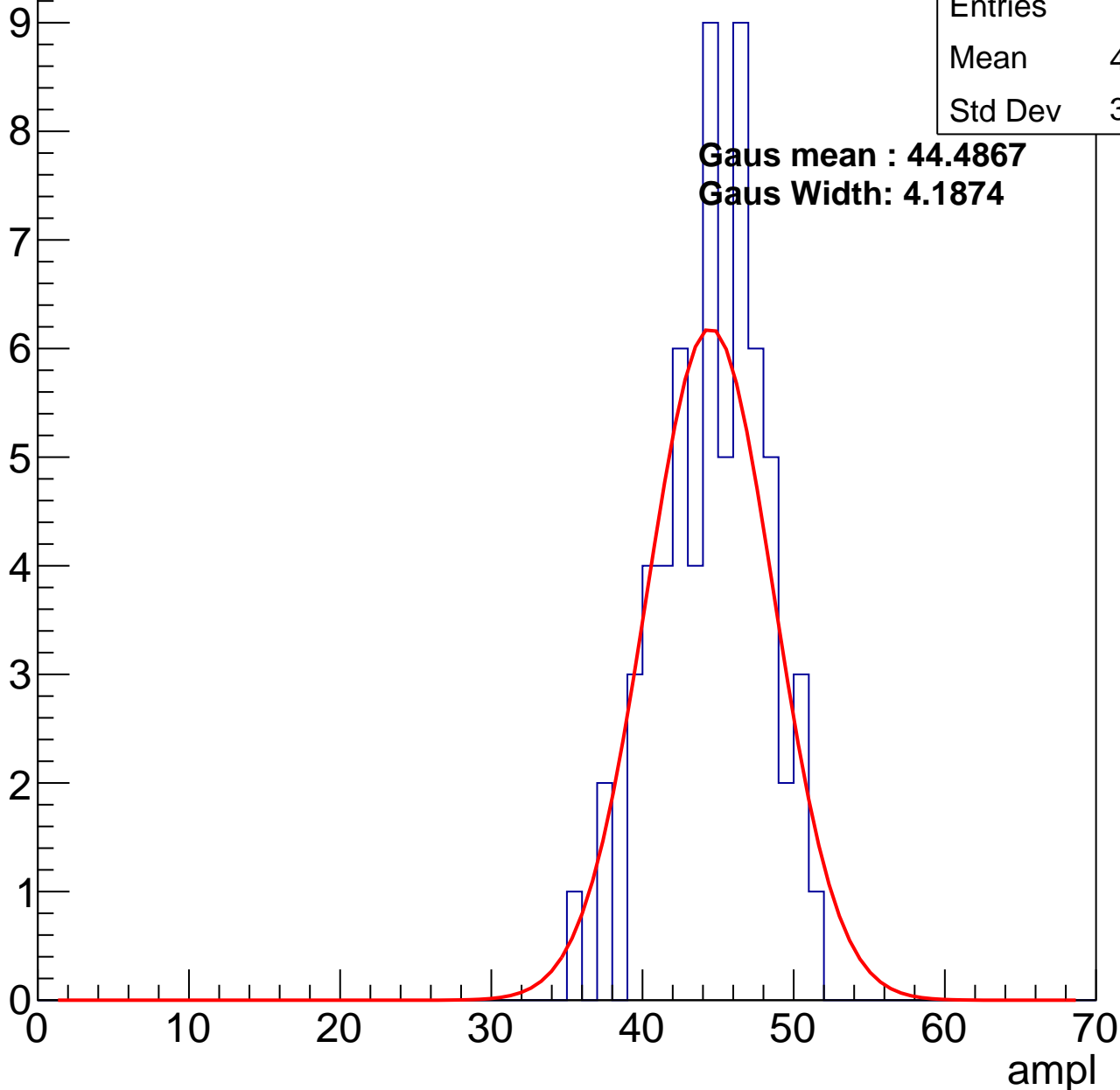
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	44.22
Std Dev	3.448

**Gaus mean : 44.4867**

**Gaus Width: 4.1874**

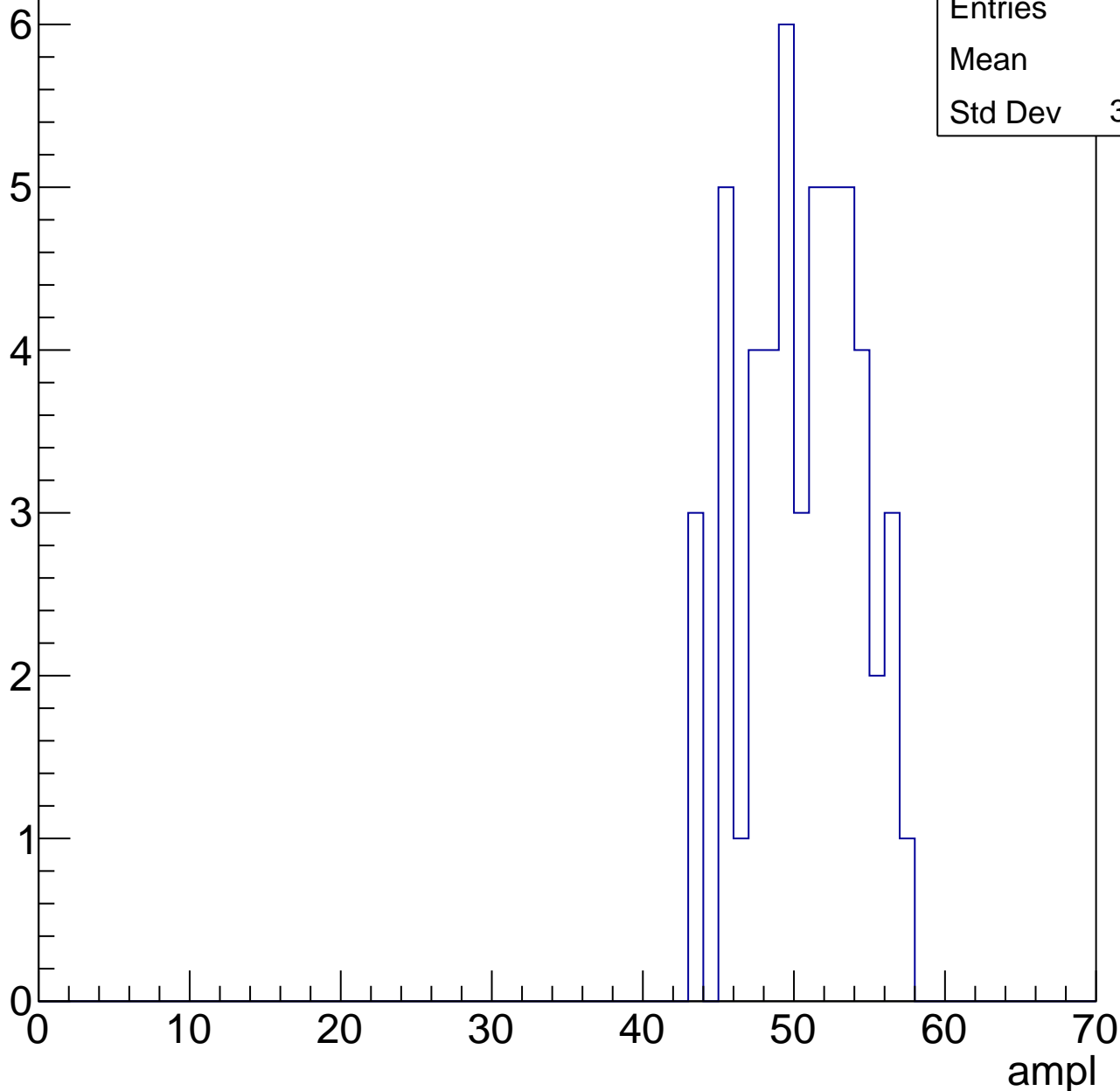


# B1L101S, U9-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	50.1
Std Dev	3.669

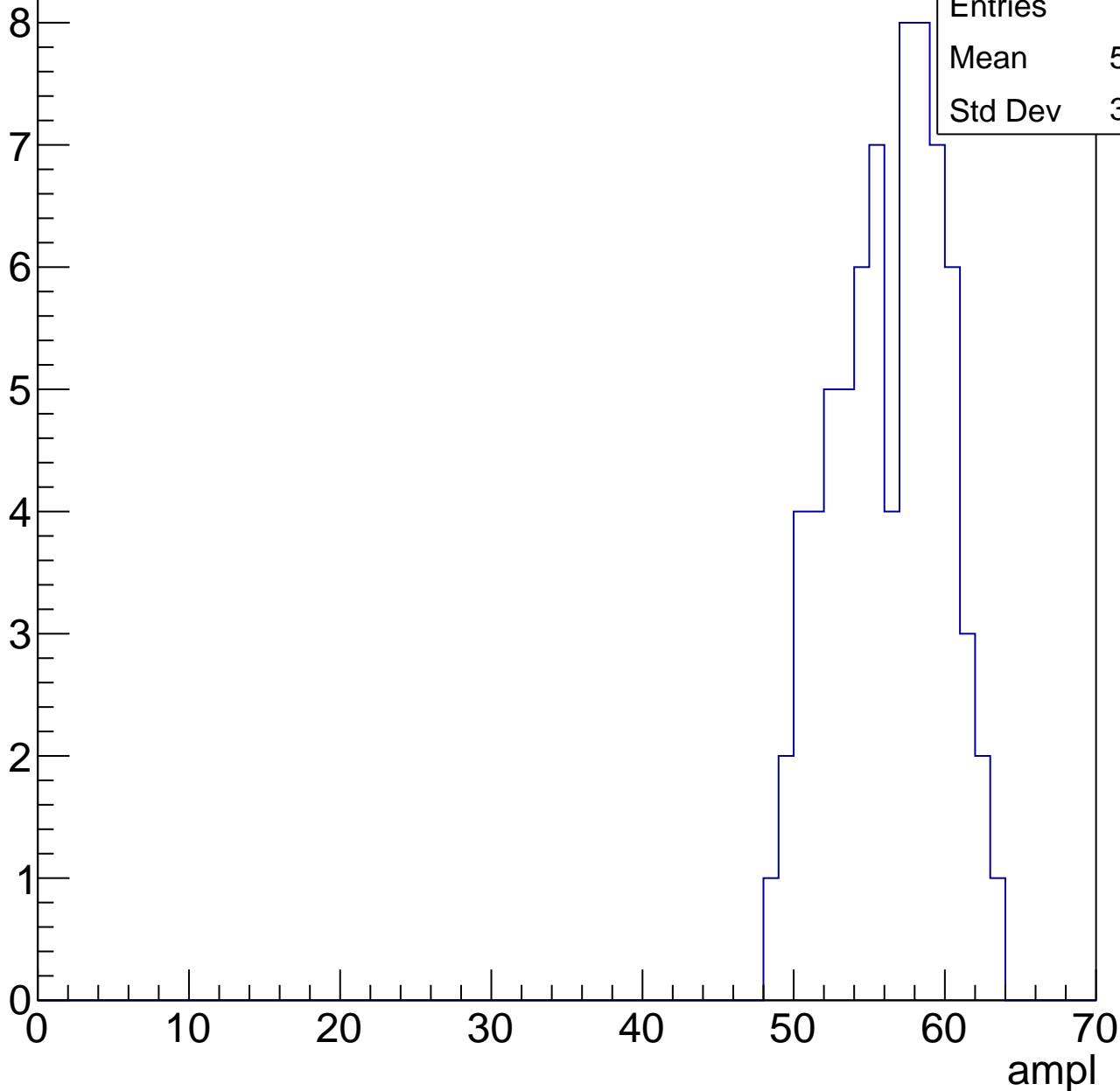


# B1L101S, U9-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	55.77
Std Dev	3.613

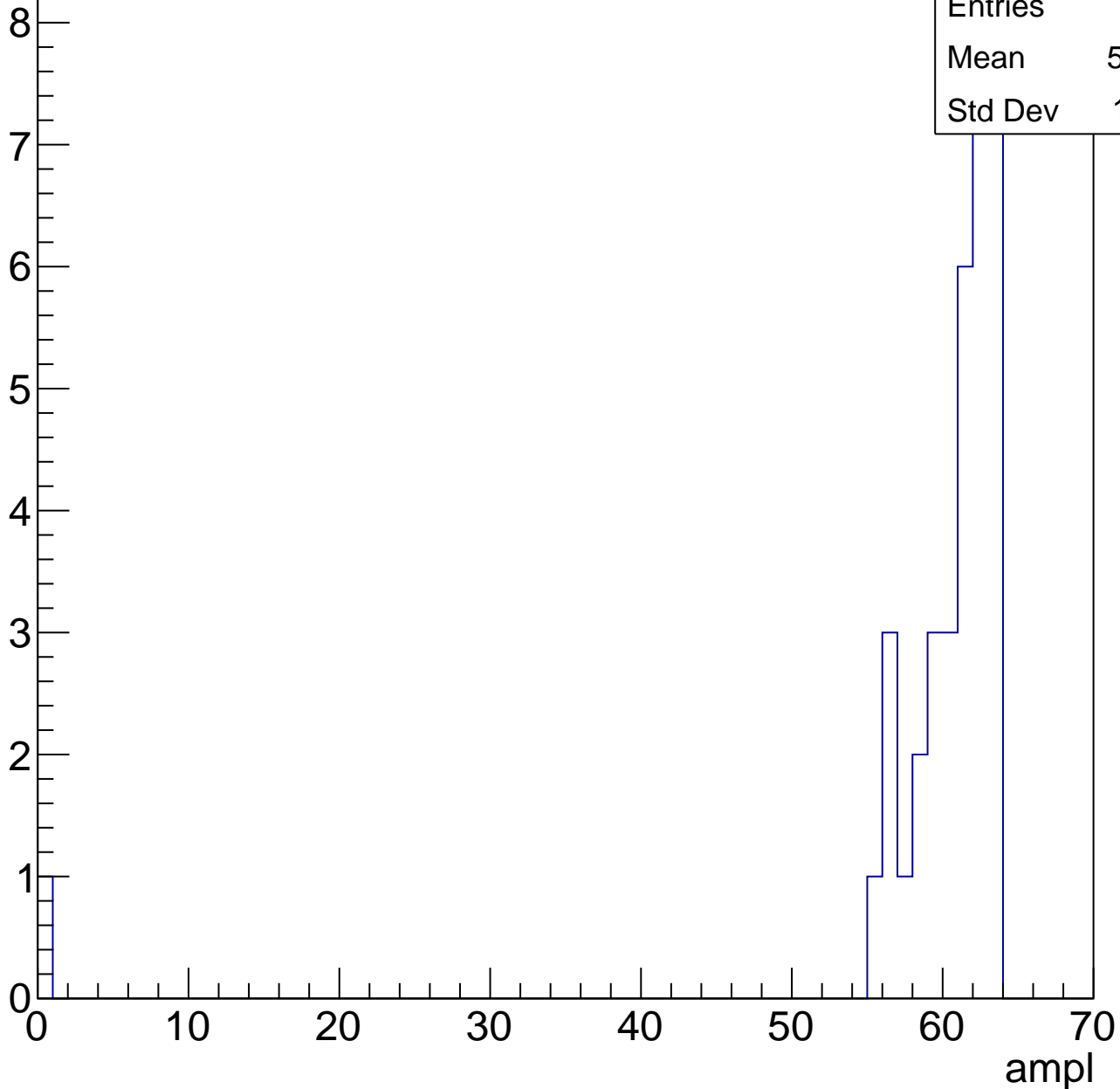


# B1L101S, U9-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	36
Mean	58.86
Std Dev	10.21



# B1L101S, U9-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch39, adc0

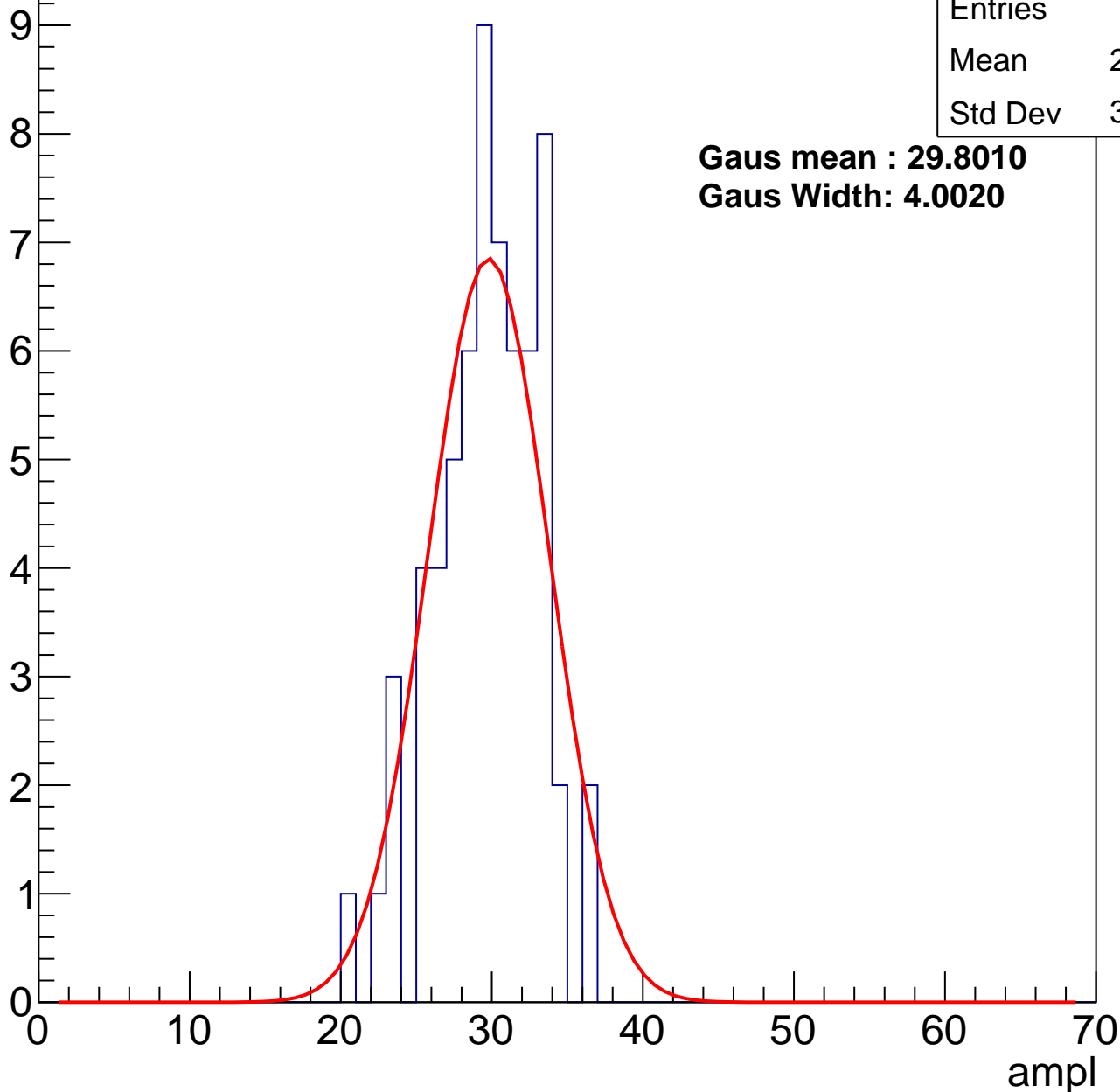
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	29.23
Std Dev	3.358

**Gaus mean : 29.8010**

**Gaus Width: 4.0020**



# B1L101S, U9-ch39, adc1

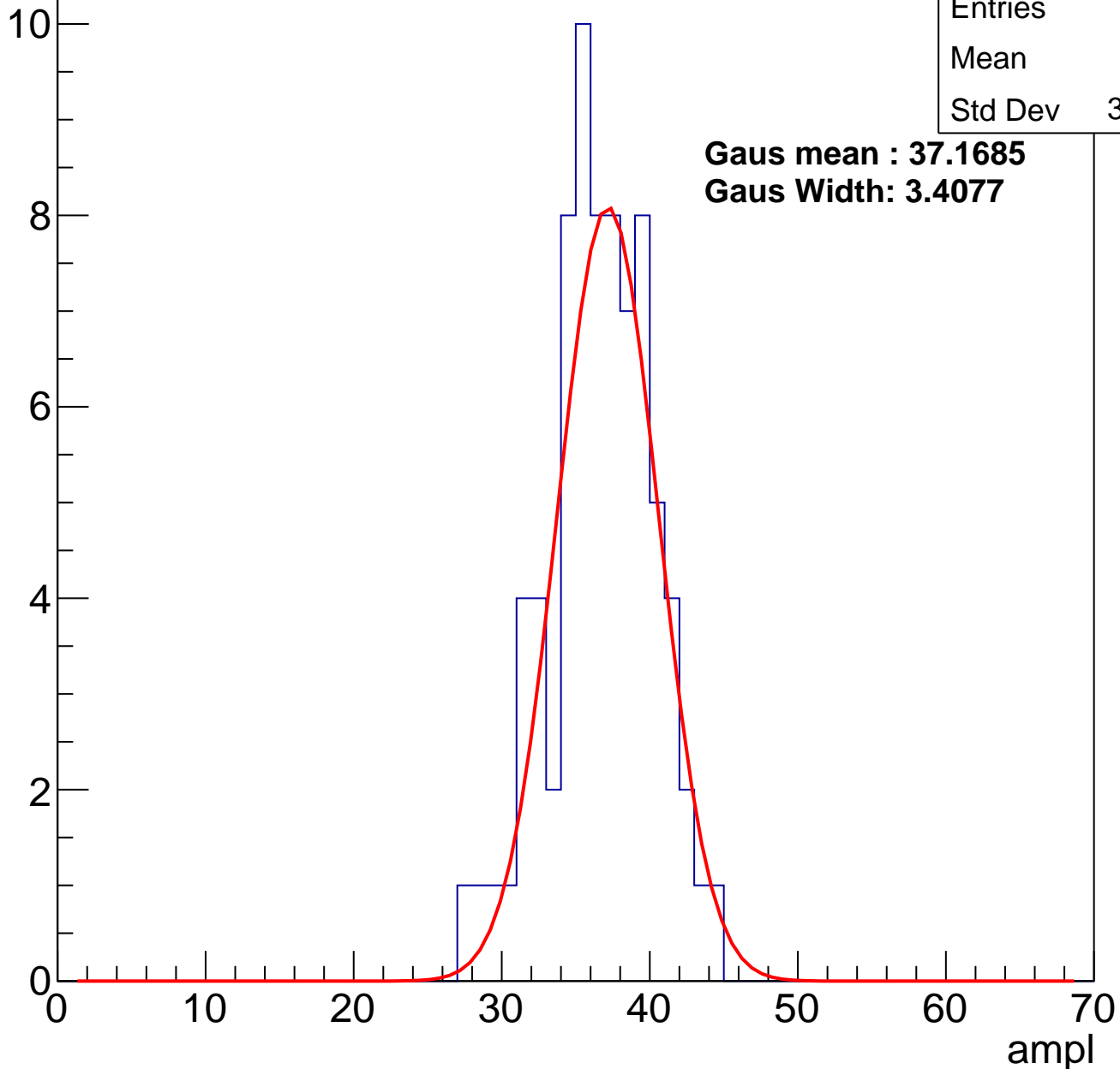
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	76
Mean	36.2
Std Dev	3.487

**Gaus mean : 37.1685**

**Gaus Width: 3.4077**

Entry



# B1L101S, U9-ch39, adc2

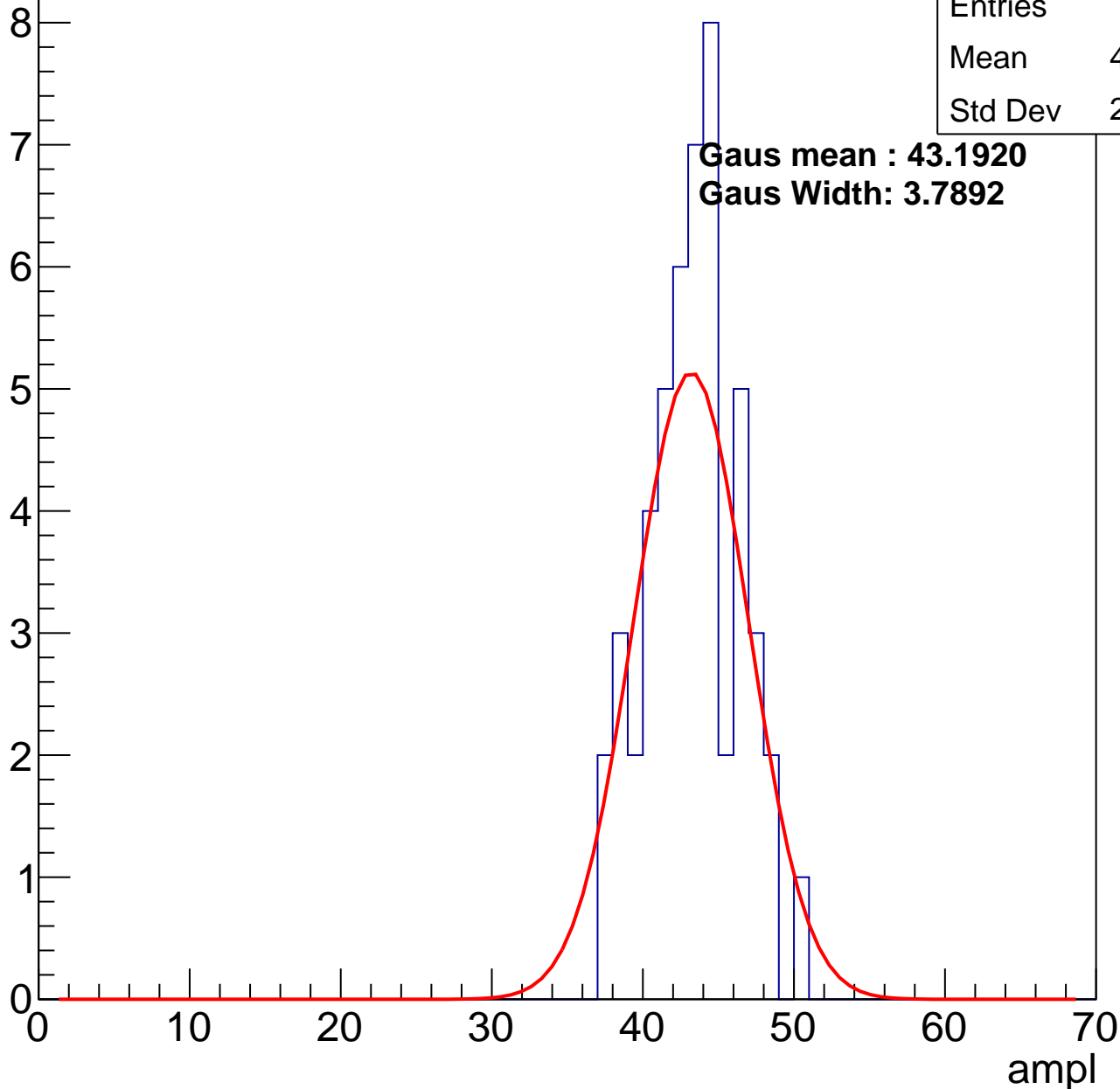
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	42.86
Std Dev	2.993

**Gaus mean : 43.1920**

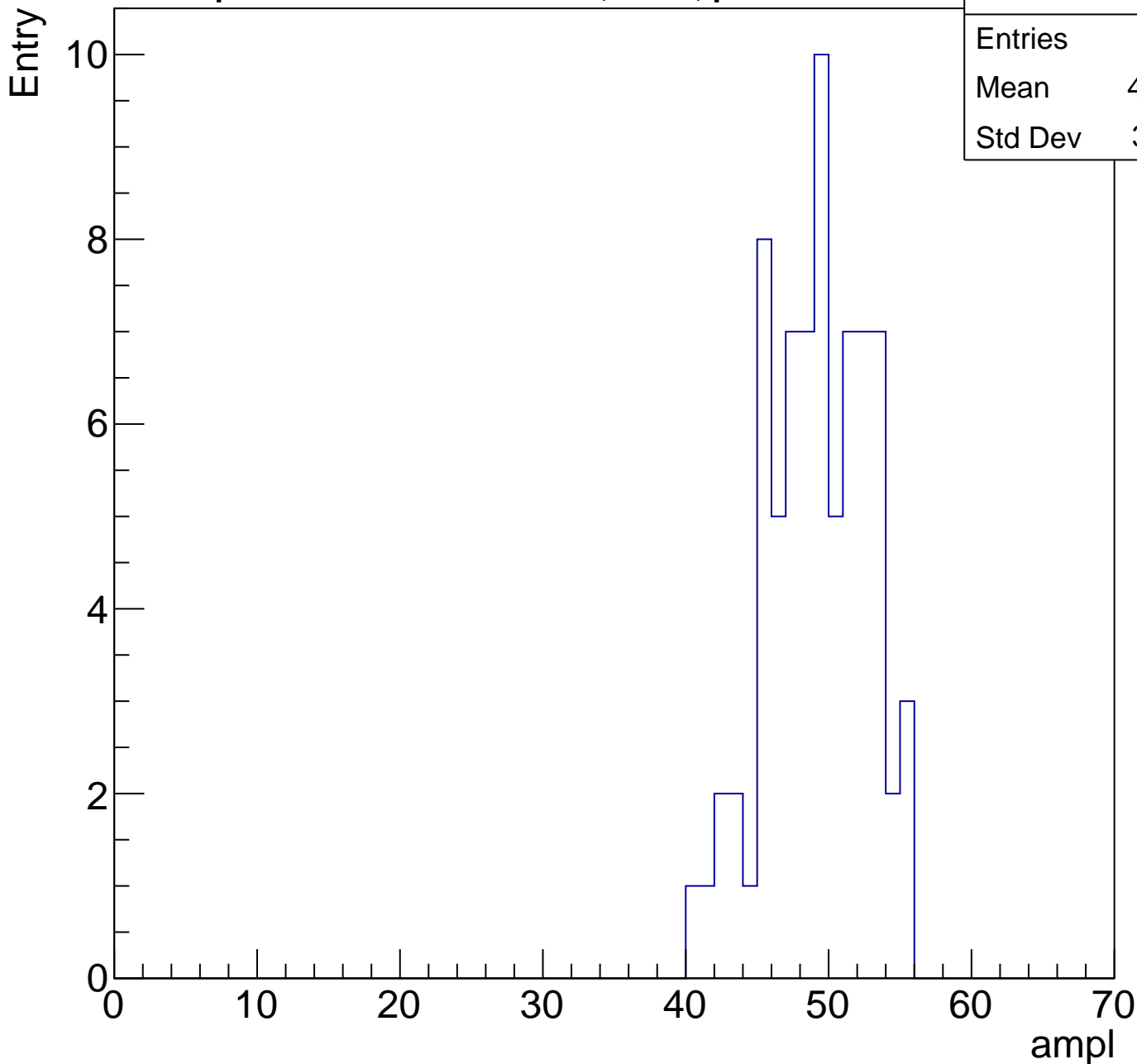
**Gaus Width: 3.7892**



# B1L101S, U9-ch39, adc3

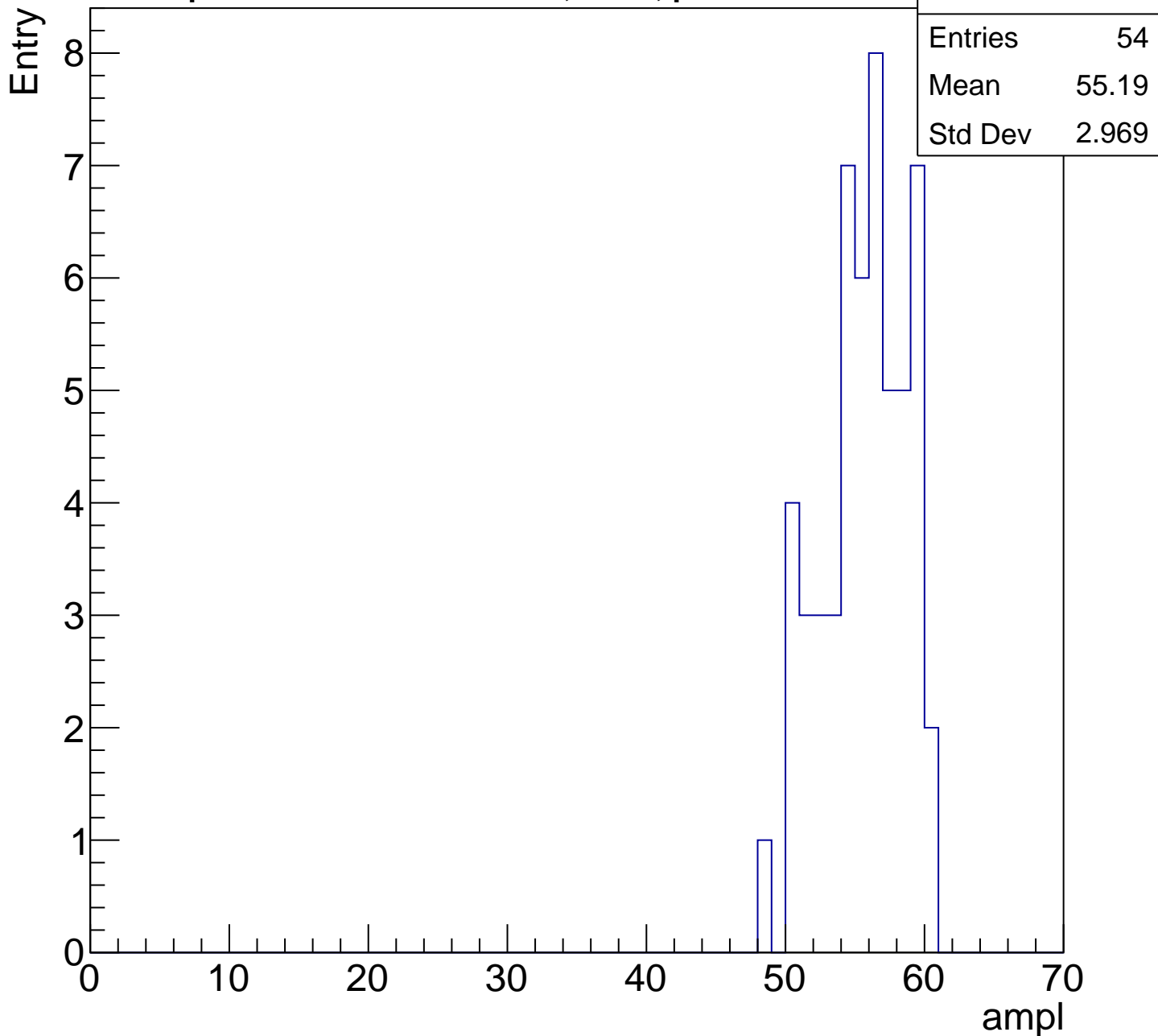
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	75
Mean	48.73
Std Dev	3.481



# B1L101S, U9-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

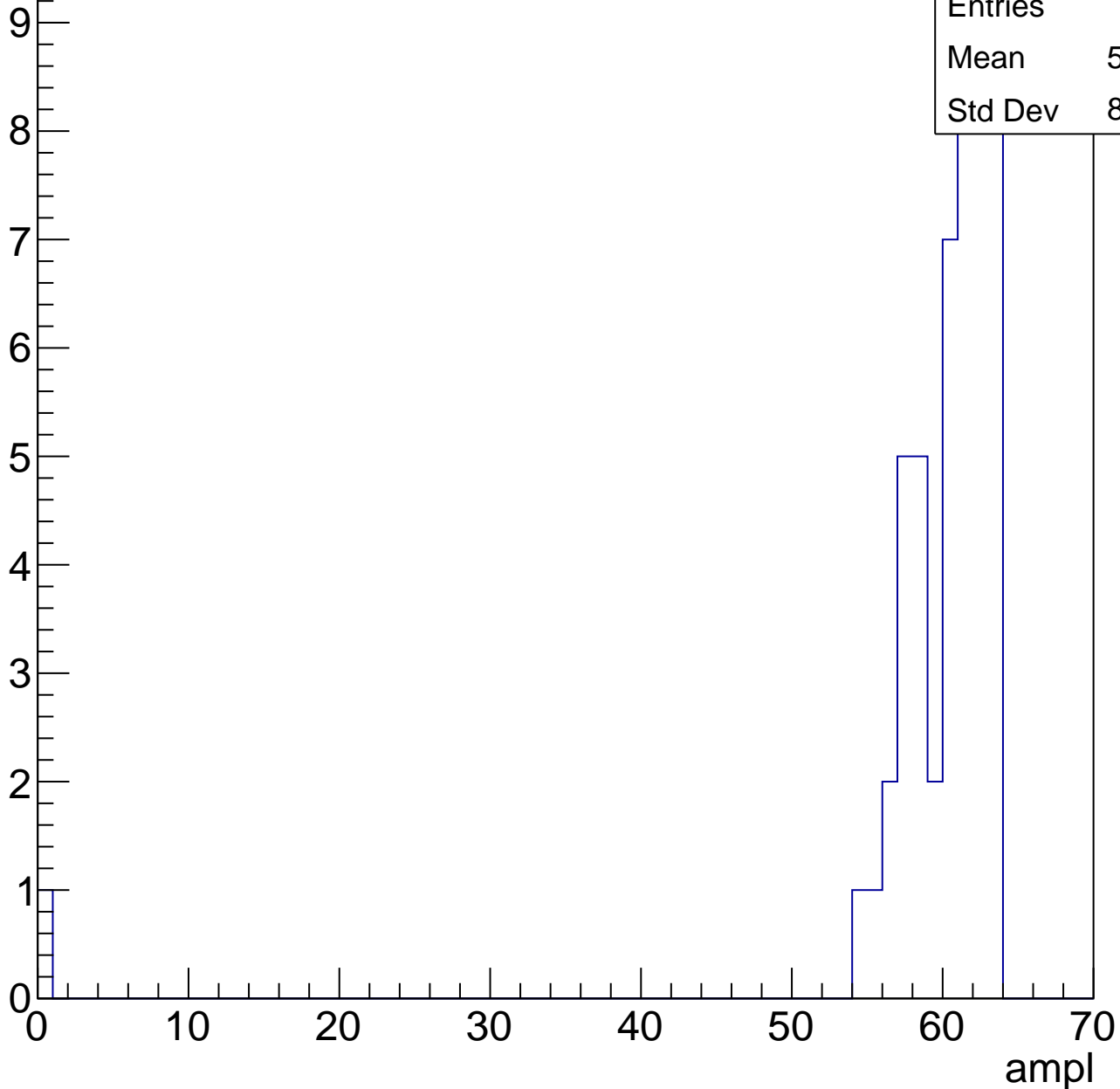


# B1L101S, U9-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	58.98
Std Dev	8.669



# B1L101S, U9-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

5

Mean

61

Std Dev

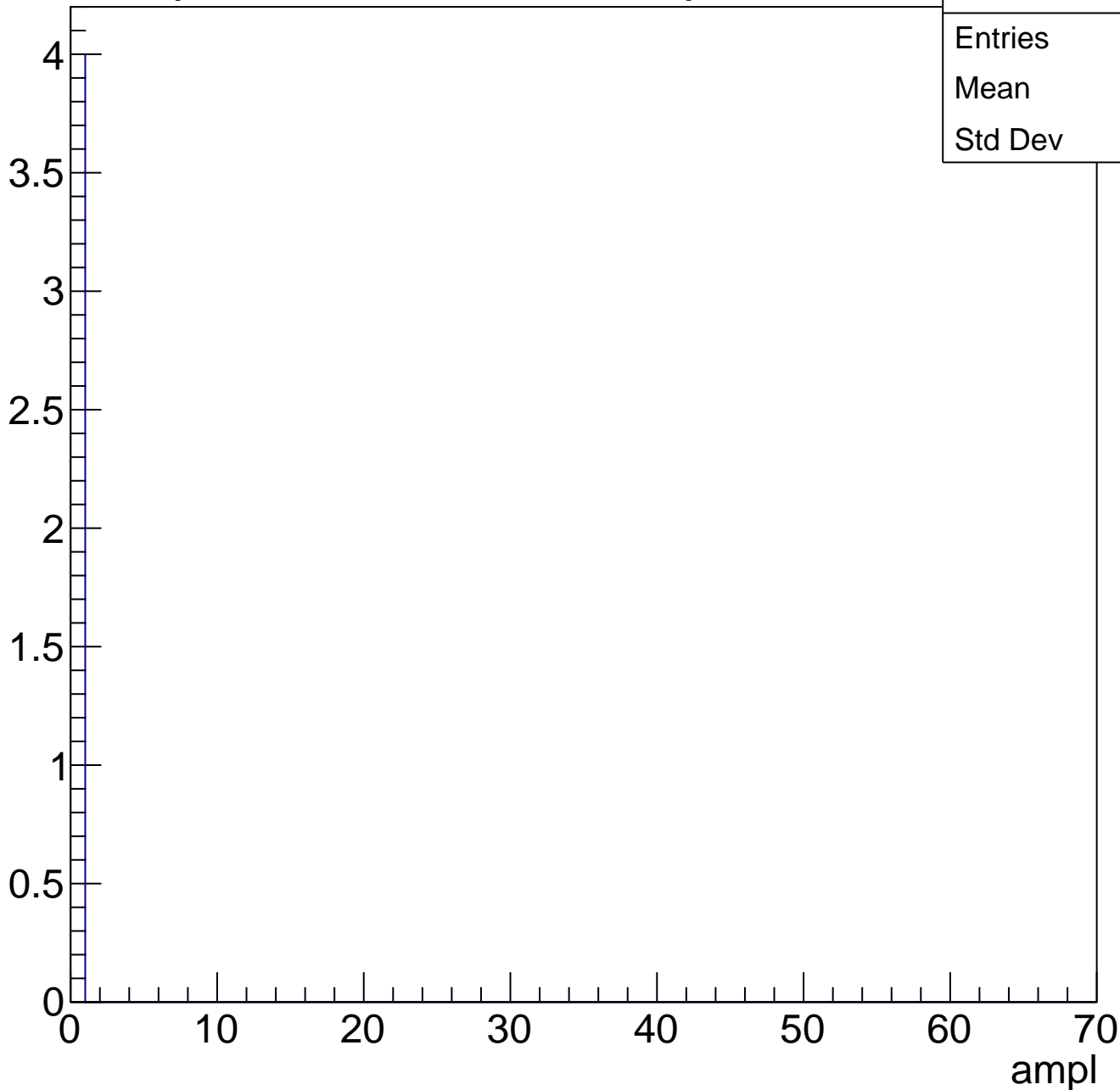
1.414



# B1L101S, U9-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	4
Mean	0
Std Dev	0

# B1L101S, U9-ch40, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	68
Mean	27.26
Std Dev	4.85

**Gaus mean : 28.2997**

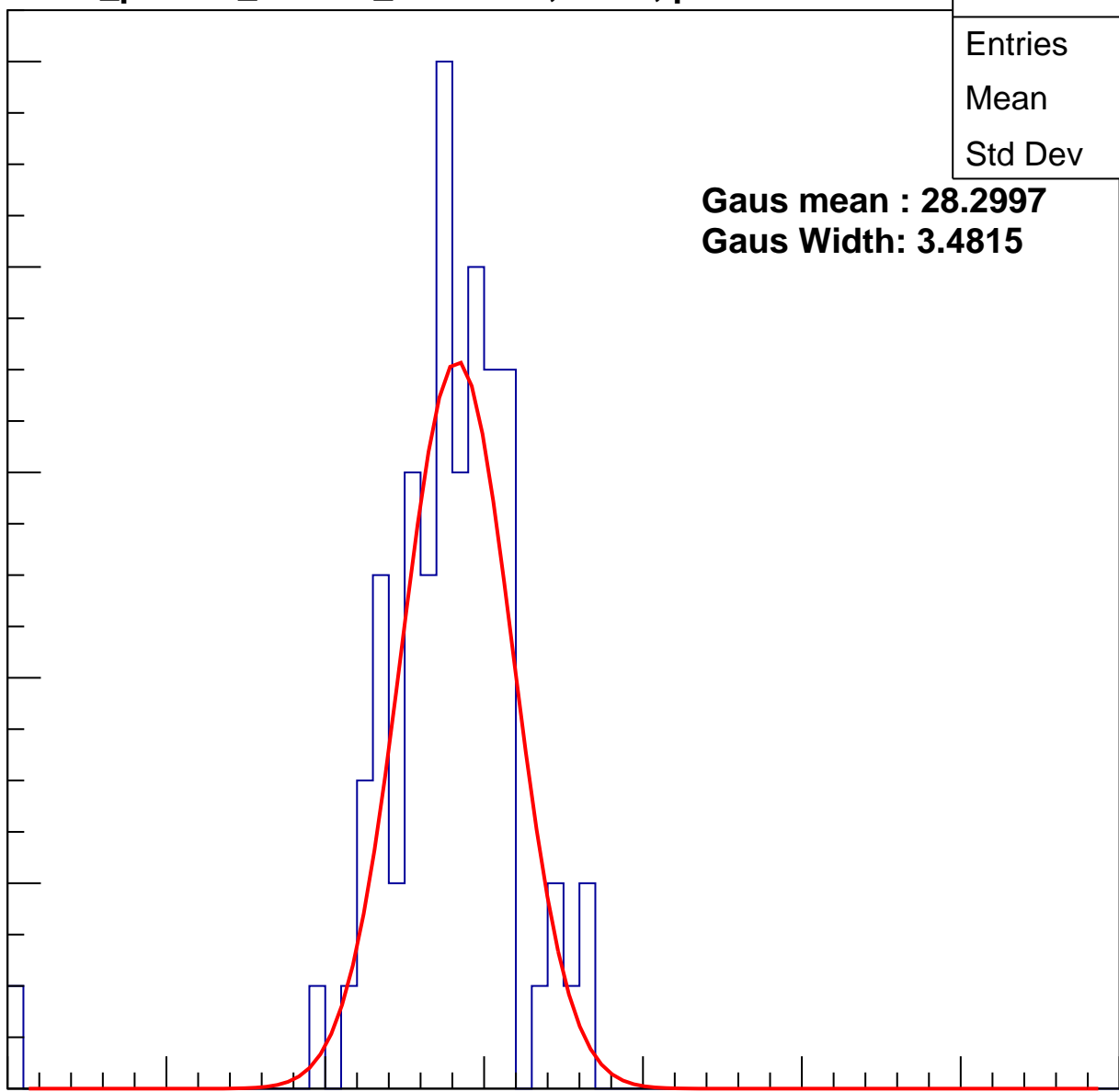
**Gaus Width: 3.4815**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U9-ch40, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	76
Mean	35.07
Std Dev	3.306

**Gaus mean : 35.4587**

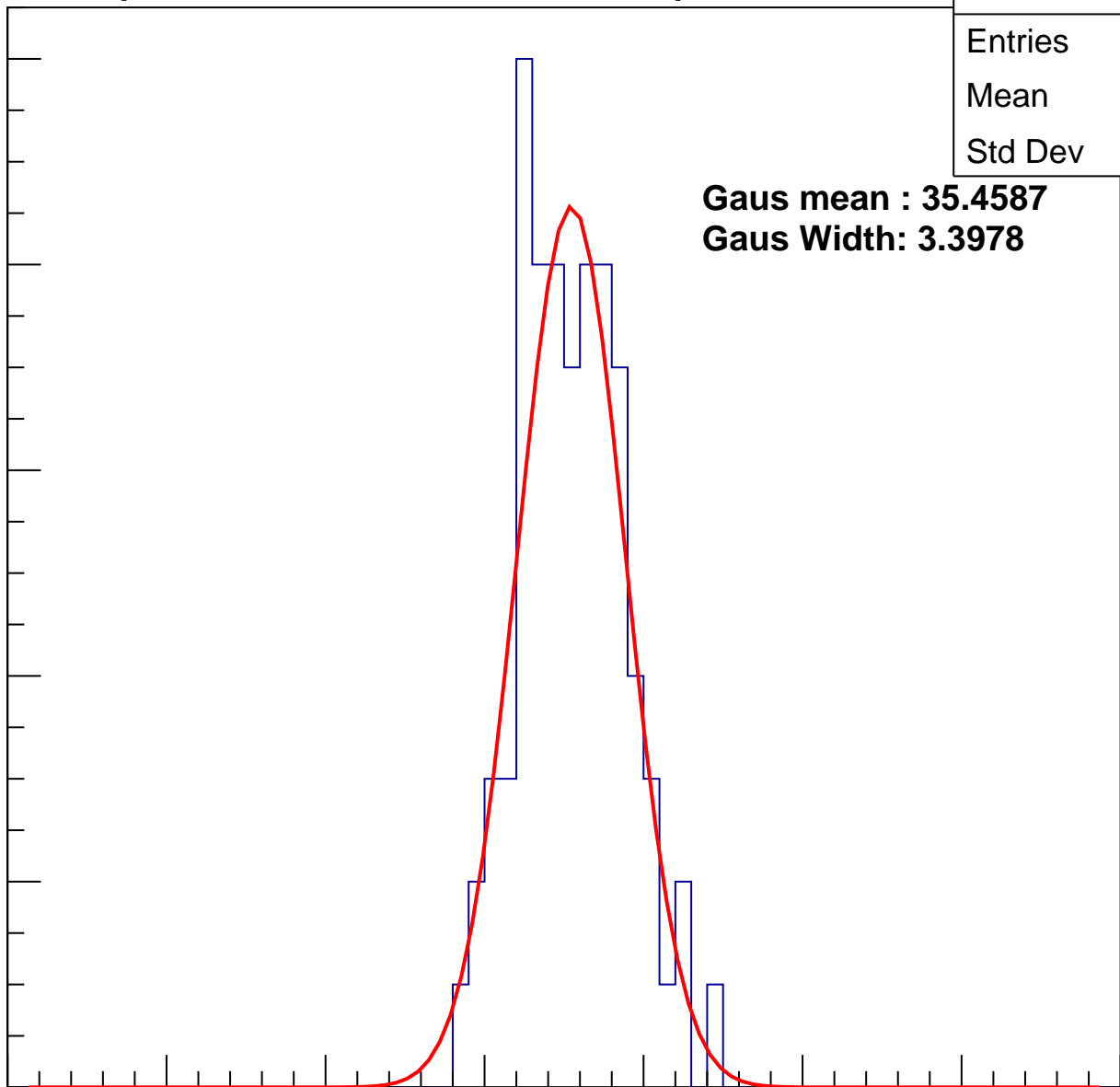
**Gaus Width: 3.3978**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U9-ch40, adc2

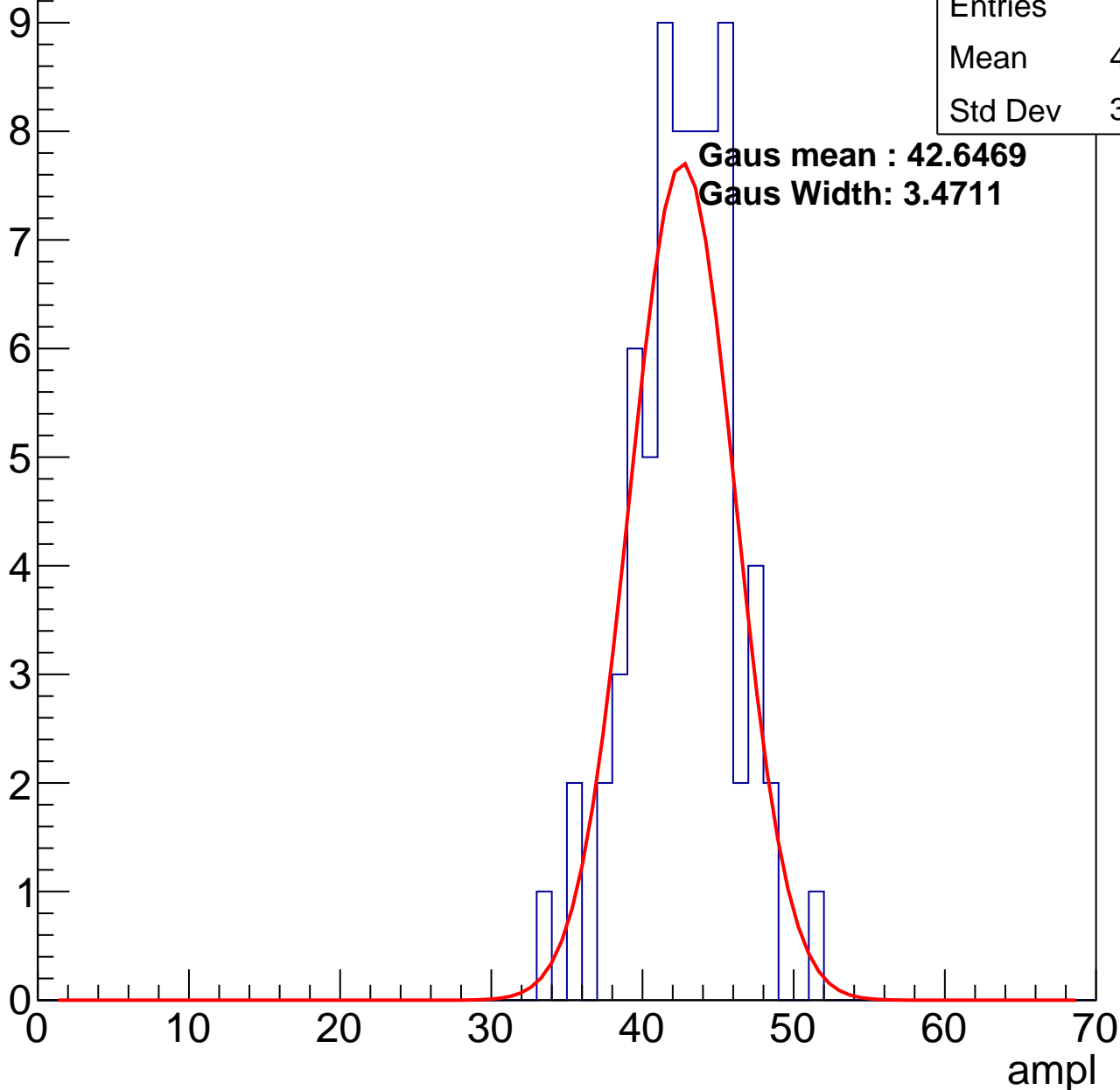
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	42.26
Std Dev	3.298

**Gaus mean : 42.6469**

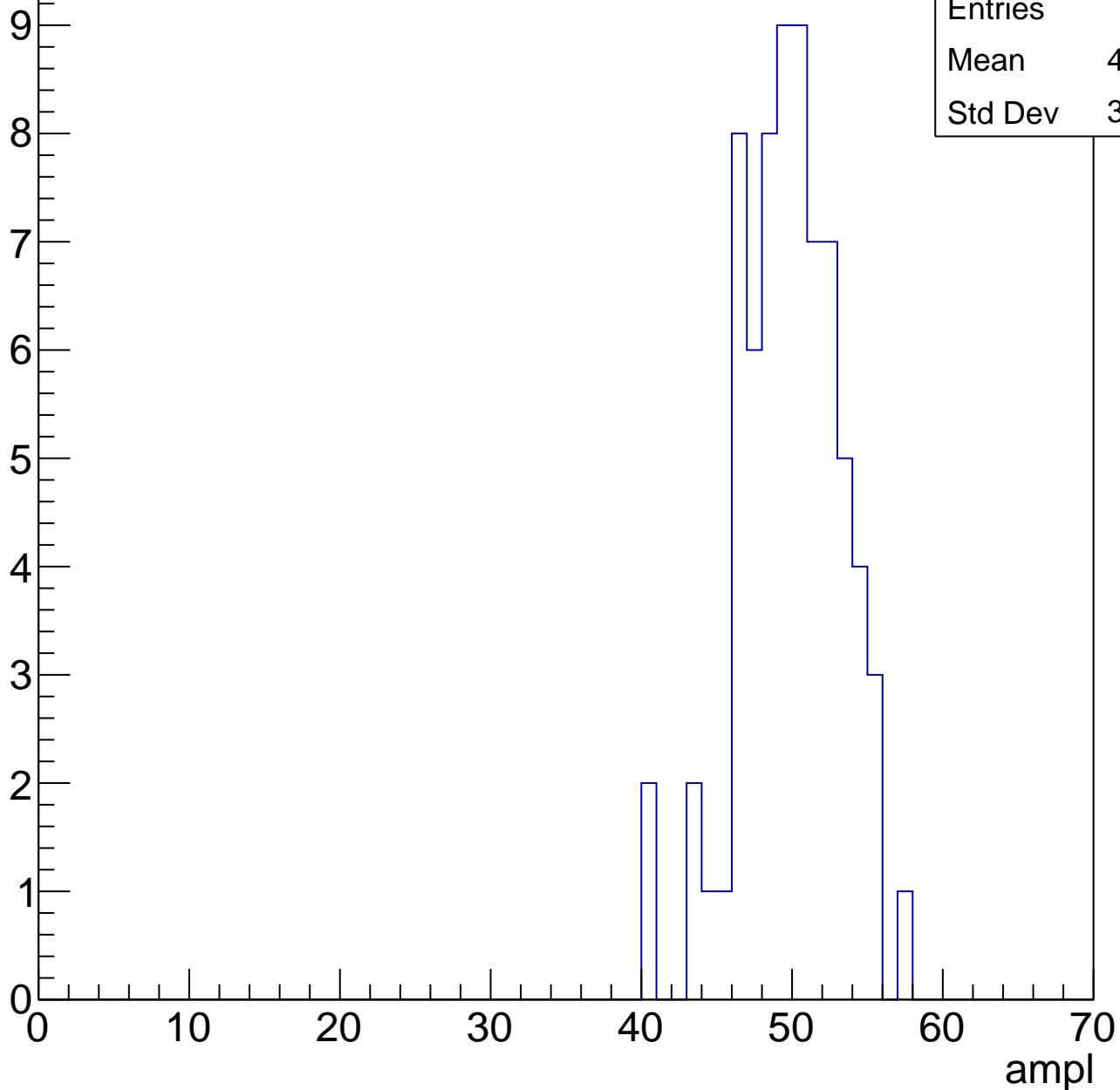
**Gaus Width: 3.4711**



# B1L101S, U9-ch40, adc3

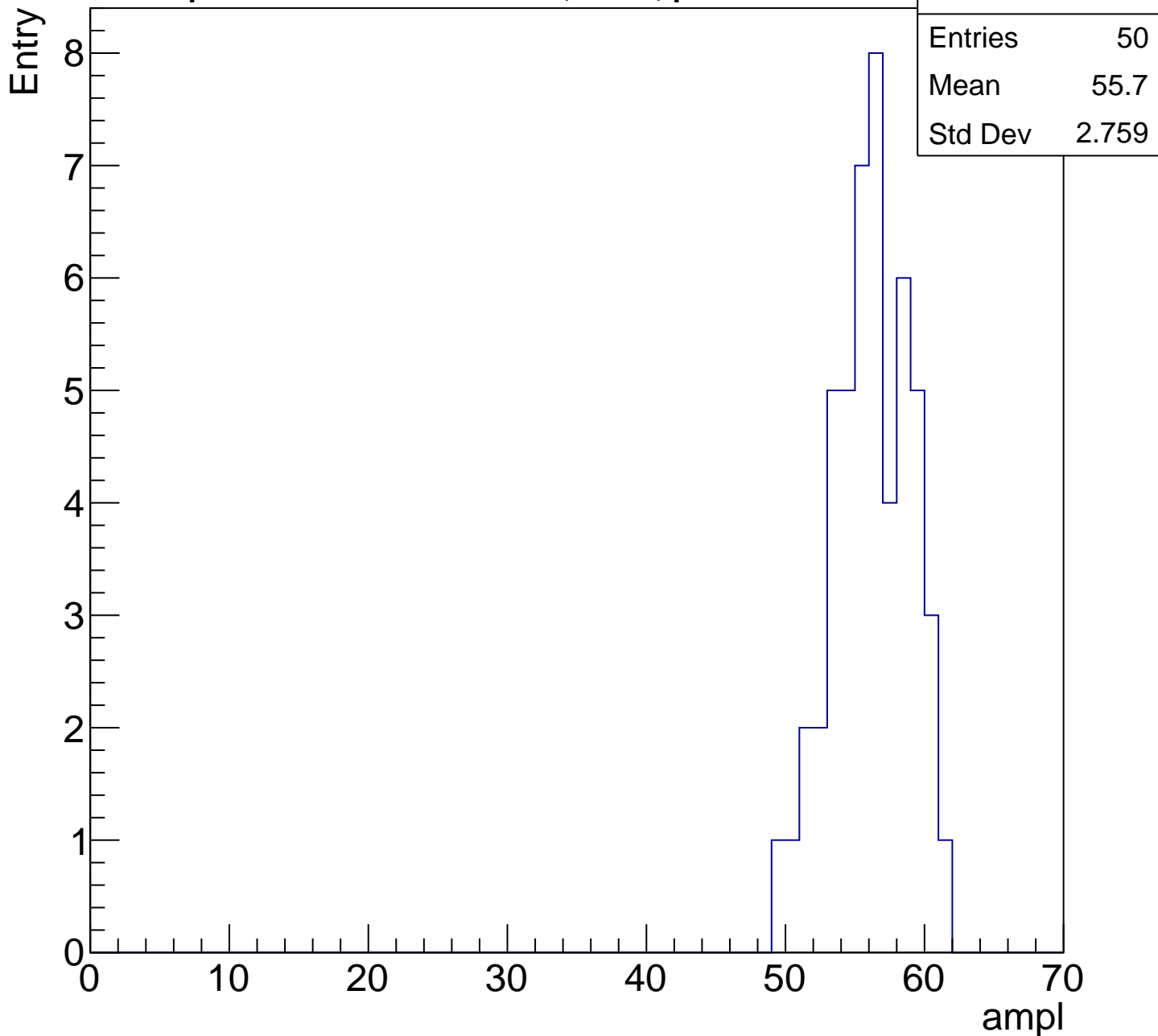
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

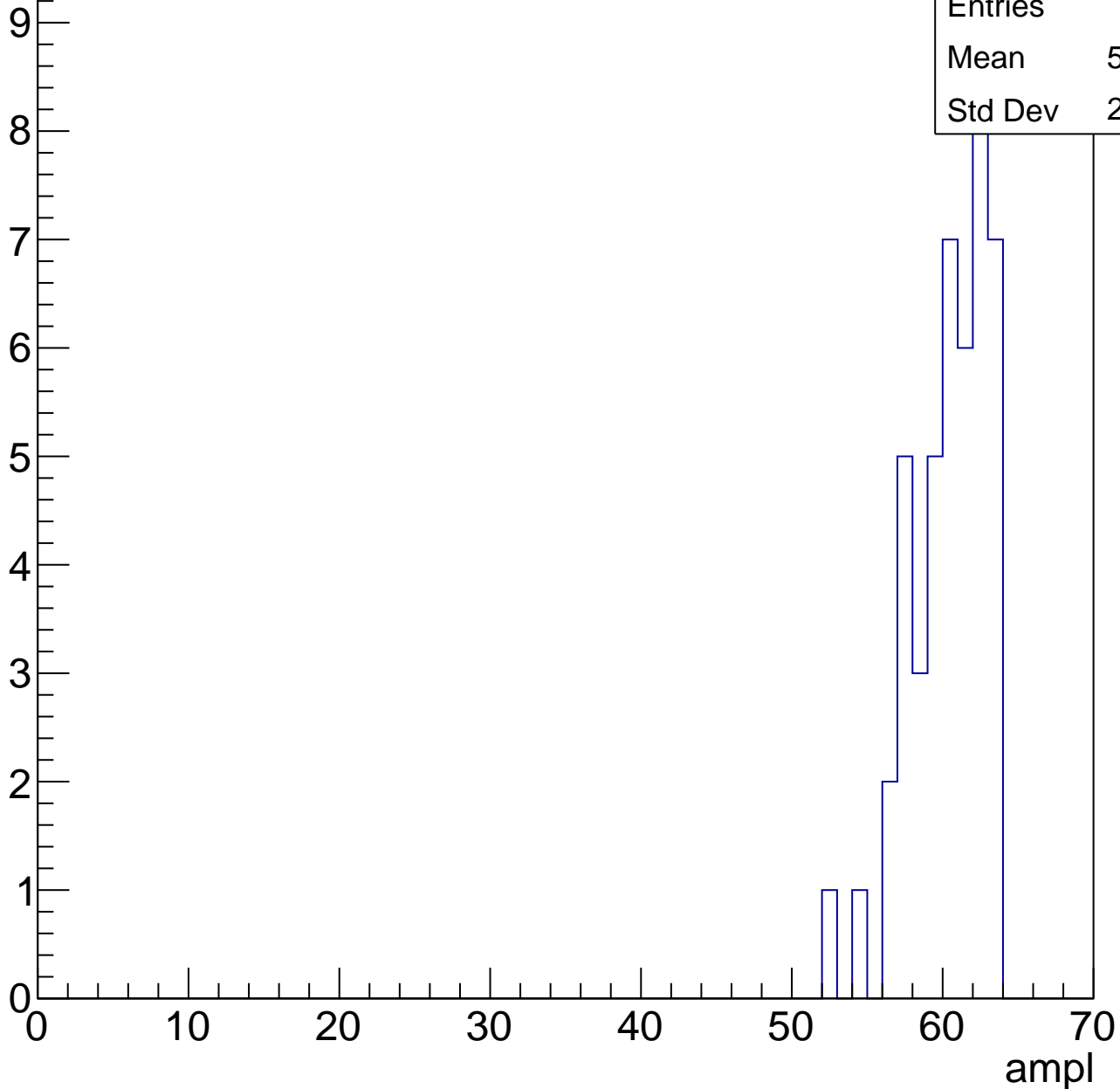


# B1L101S, U9-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	59.93
Std Dev	2.549



# B1L101S, U9-ch40, adc6

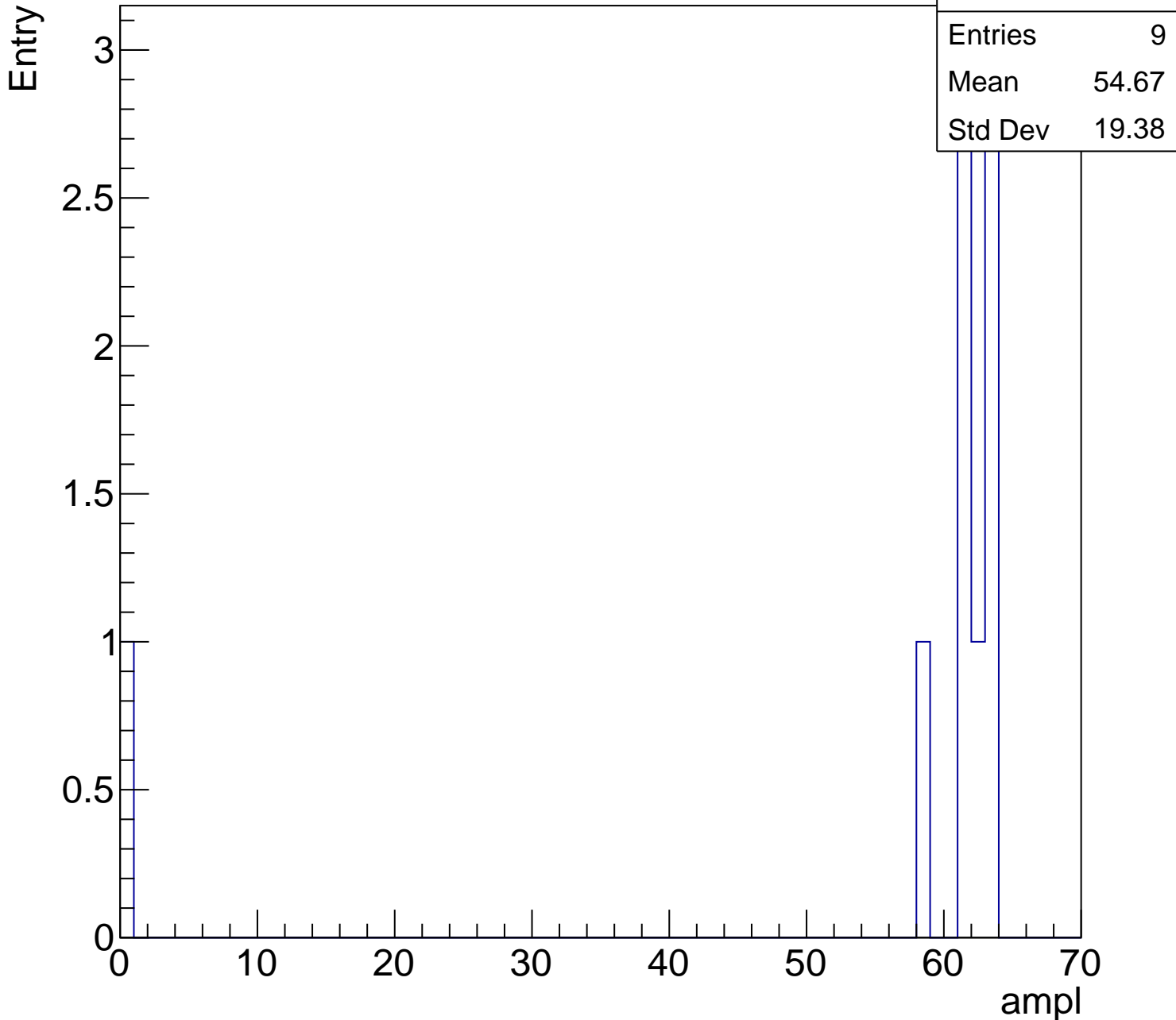
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	9
Mean	54.67
Std Dev	19.38

ampl





# B1L101S, U9-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U9-ch41, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	80
Mean	29.29
Std Dev	3.589

**Gaus mean : 29.6398**

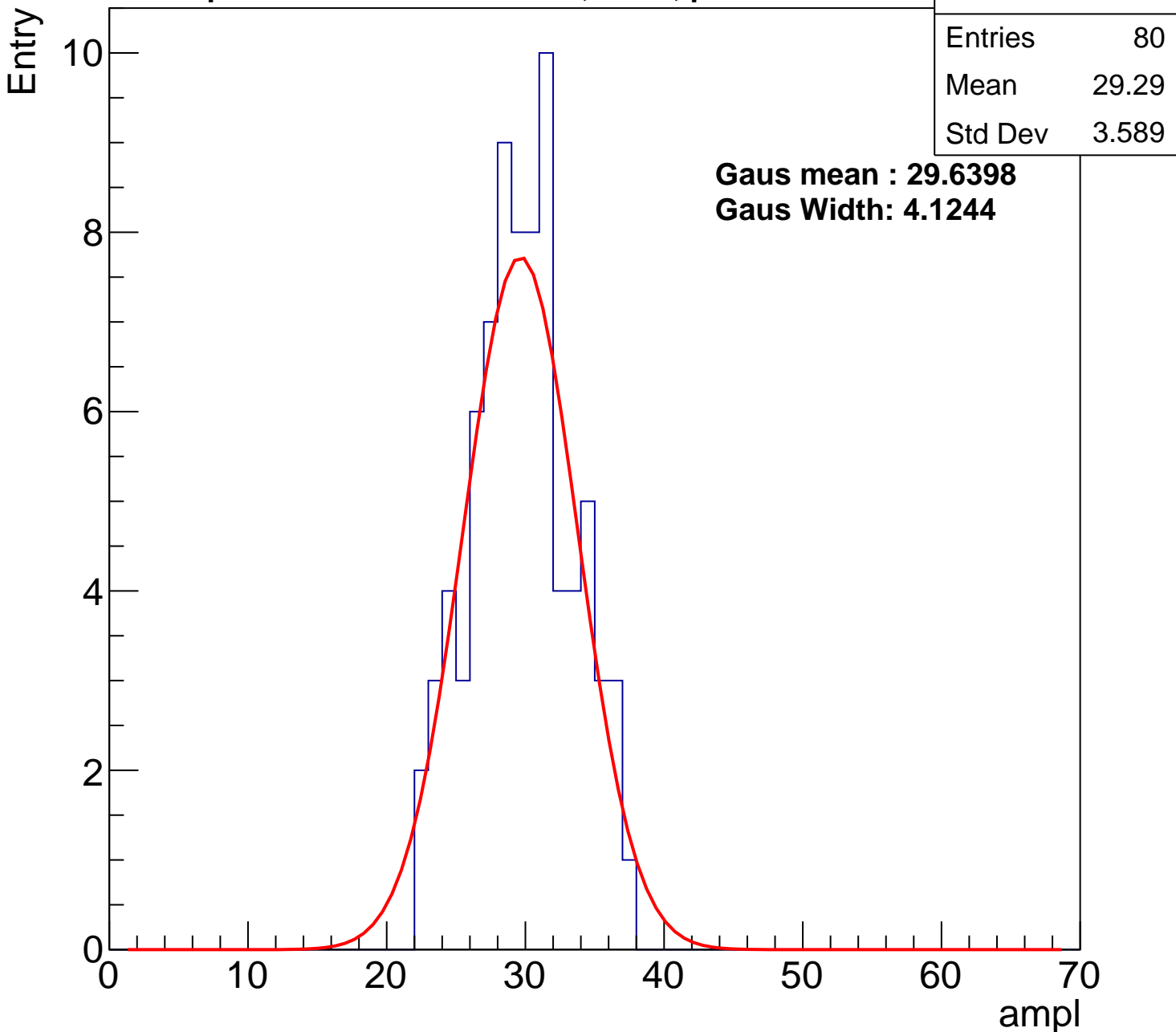
**Gaus Width: 4.1244**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U9-ch41, adc1

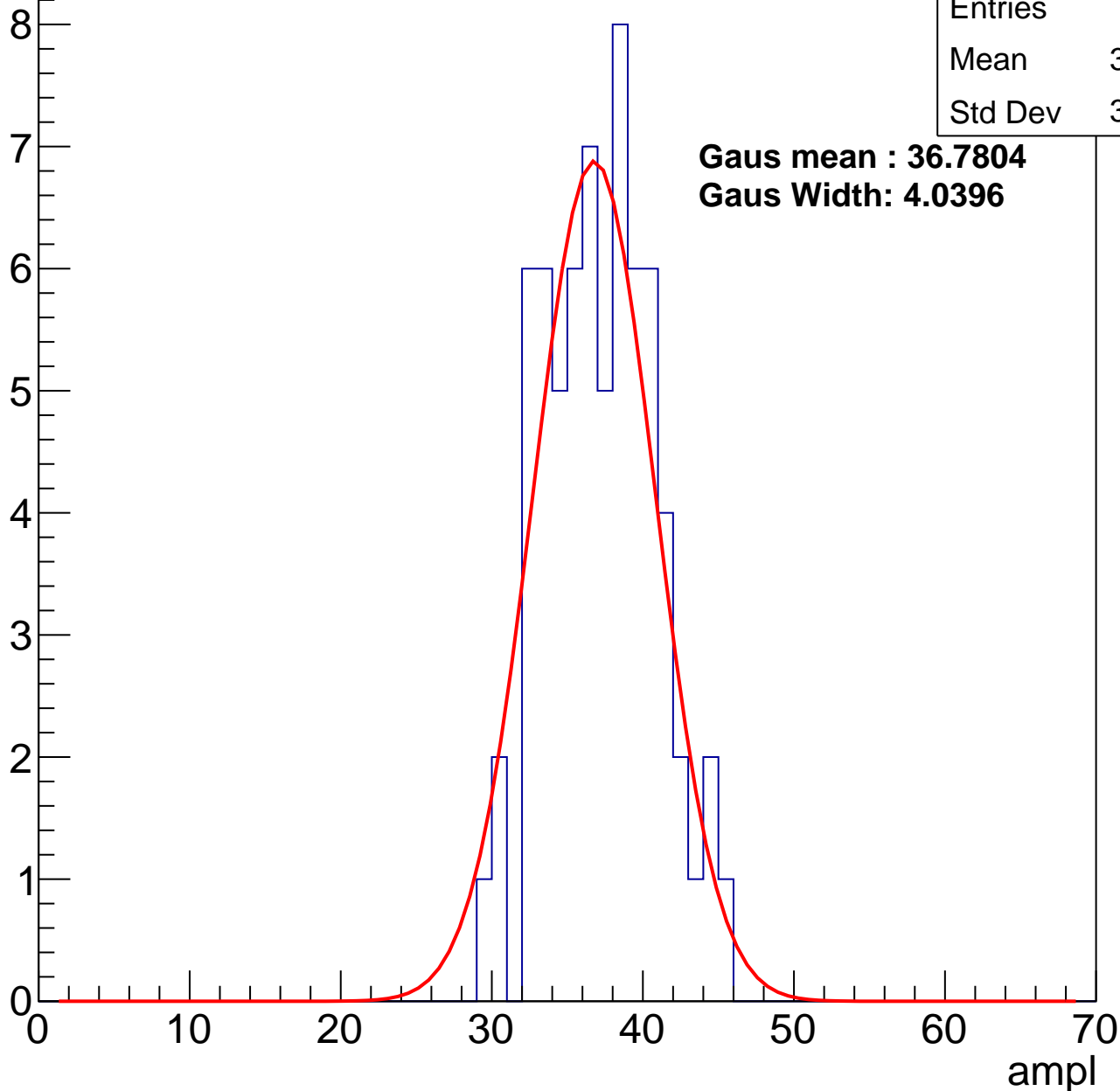
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	36.74
Std Dev	3.592

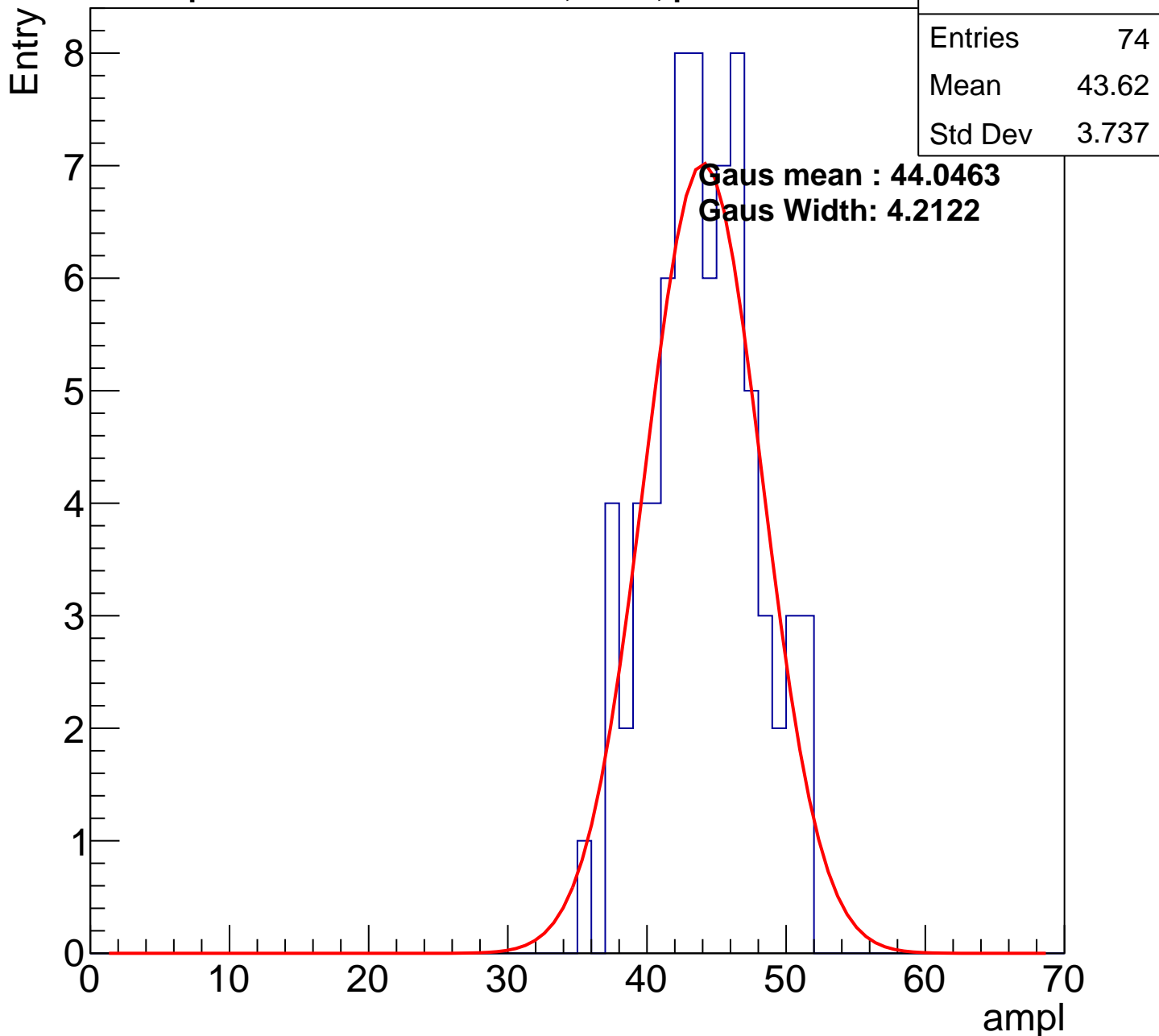
**Gaus mean : 36.7804**

**Gaus Width: 4.0396**



# B1L101S, U9-ch41, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

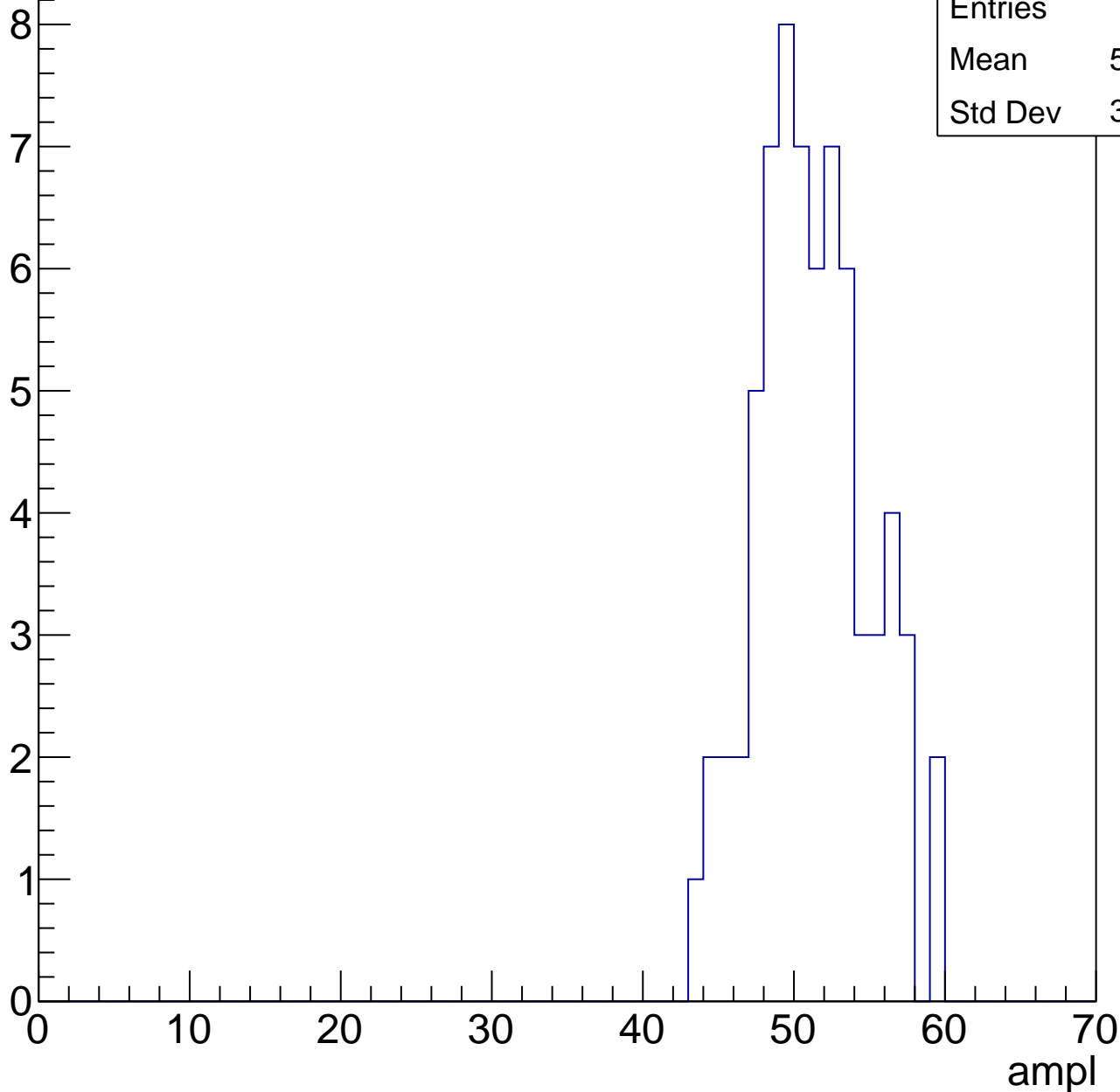


# B1L101S, U9-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	50.79
Std Dev	3.648

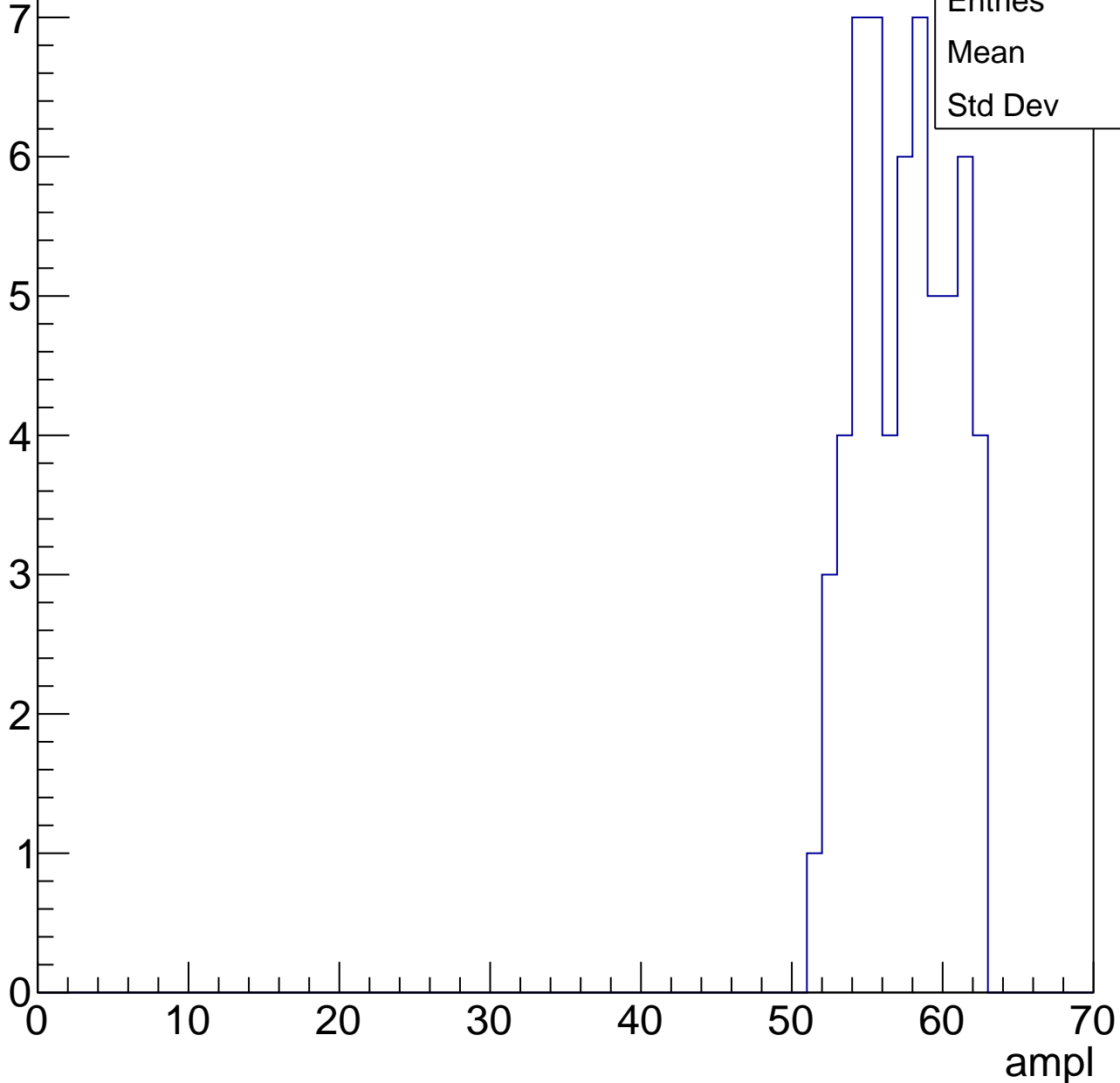


# B1L101S, U9-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	57
Std Dev	3.02

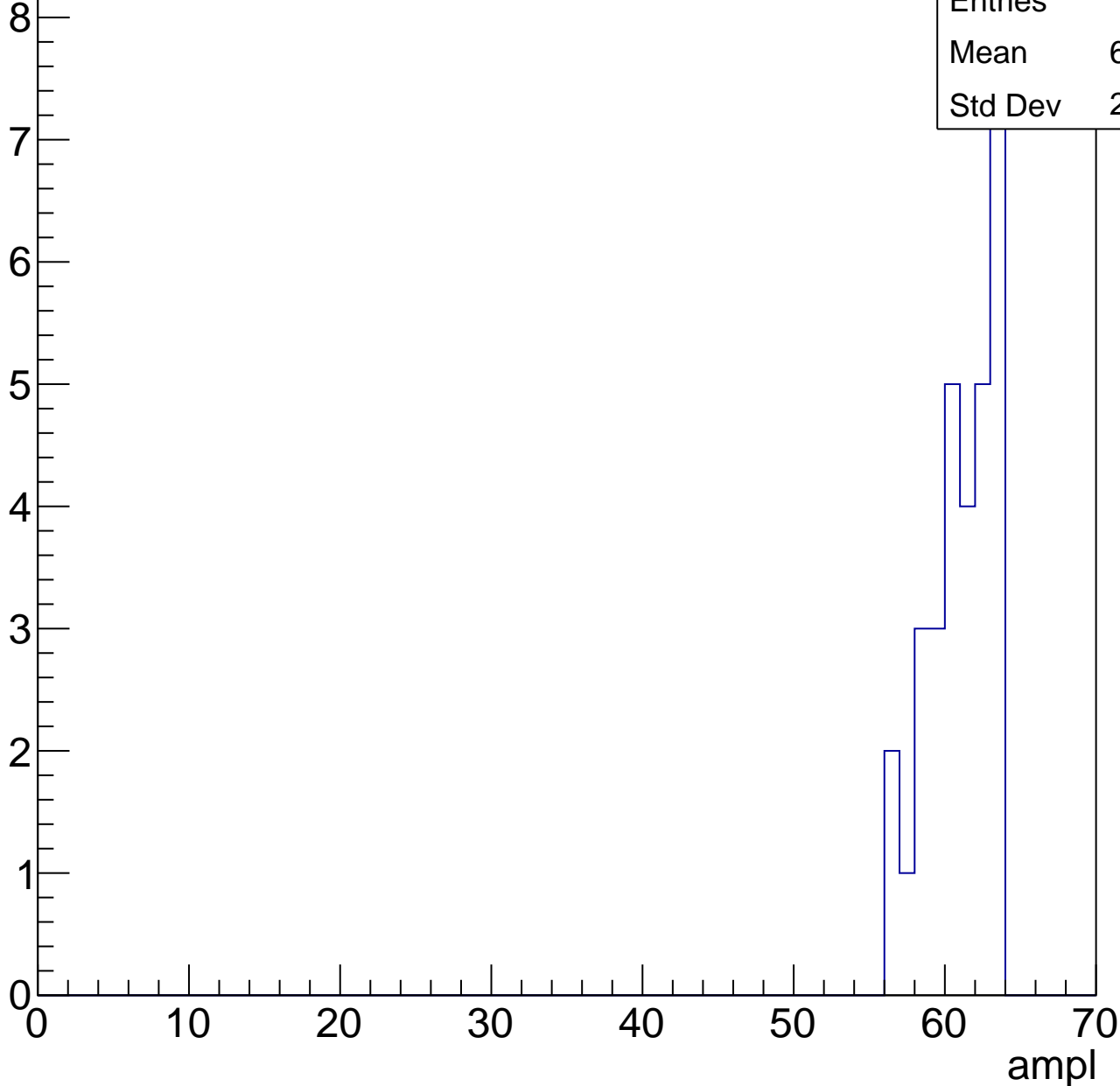


# B1L101S, U9-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	31
Mean	60.58
Std Dev	2.137



# B1L101S, U9-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

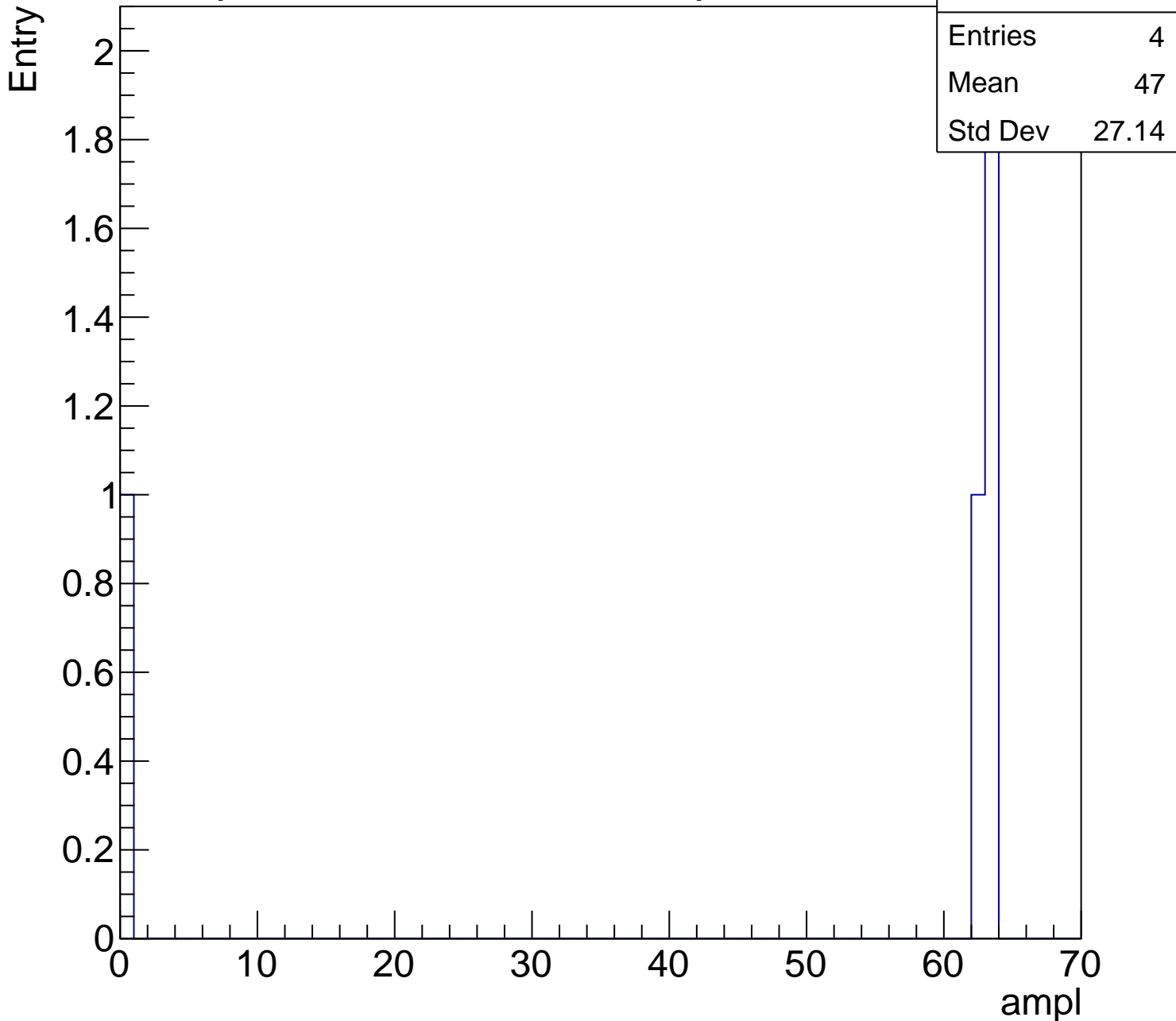
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	47
Std Dev	27.14

0 10 20 30 40 50 60 70

ampl





# B1L101S, U9-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	11
Std Dev	11

# B1L101S, U9-ch42, adc0

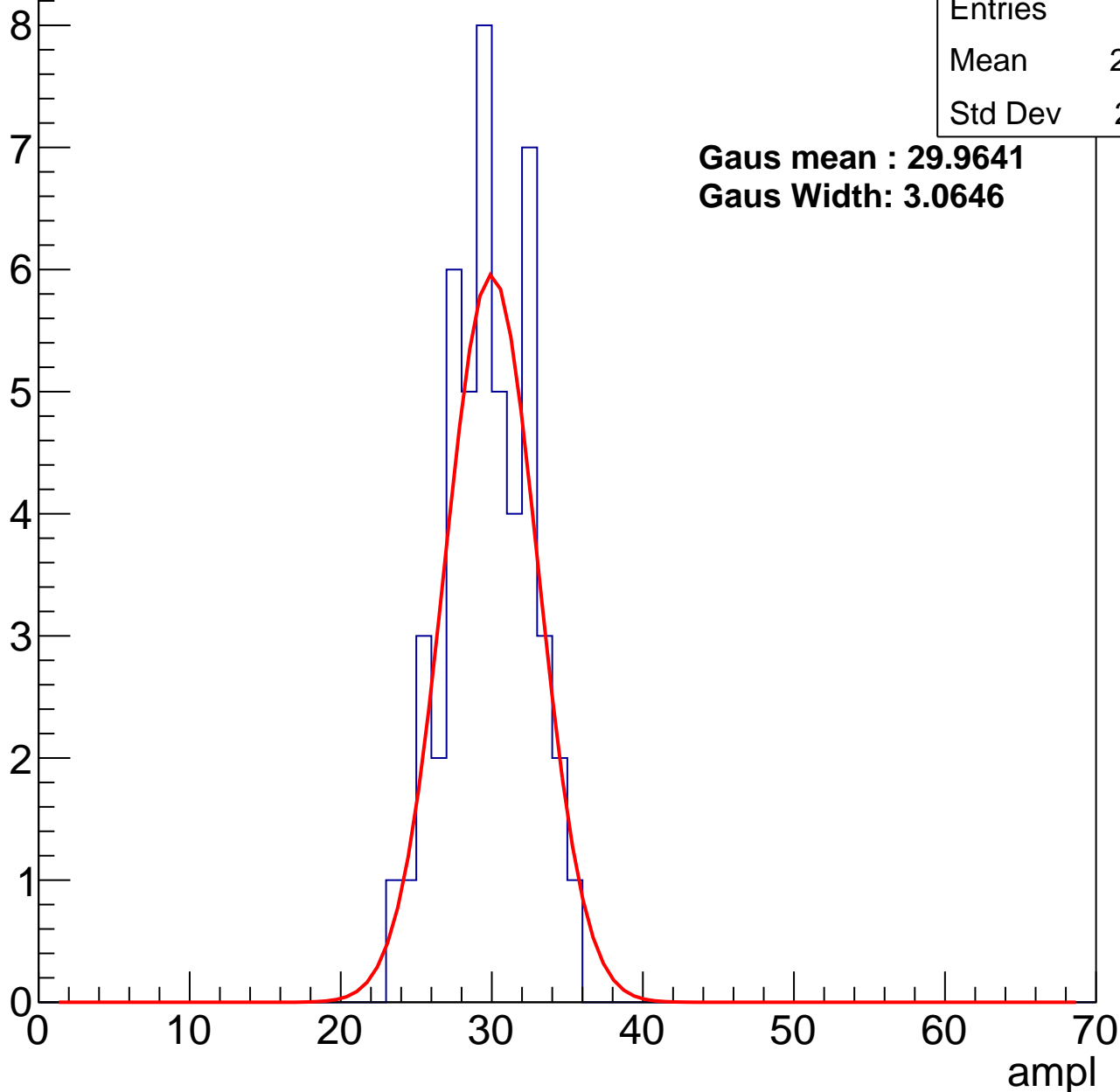
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	29.33
Std Dev	2.771

**Gaus mean : 29.9641**

**Gaus Width: 3.0646**



# B1L101S, U9-ch42, adc1

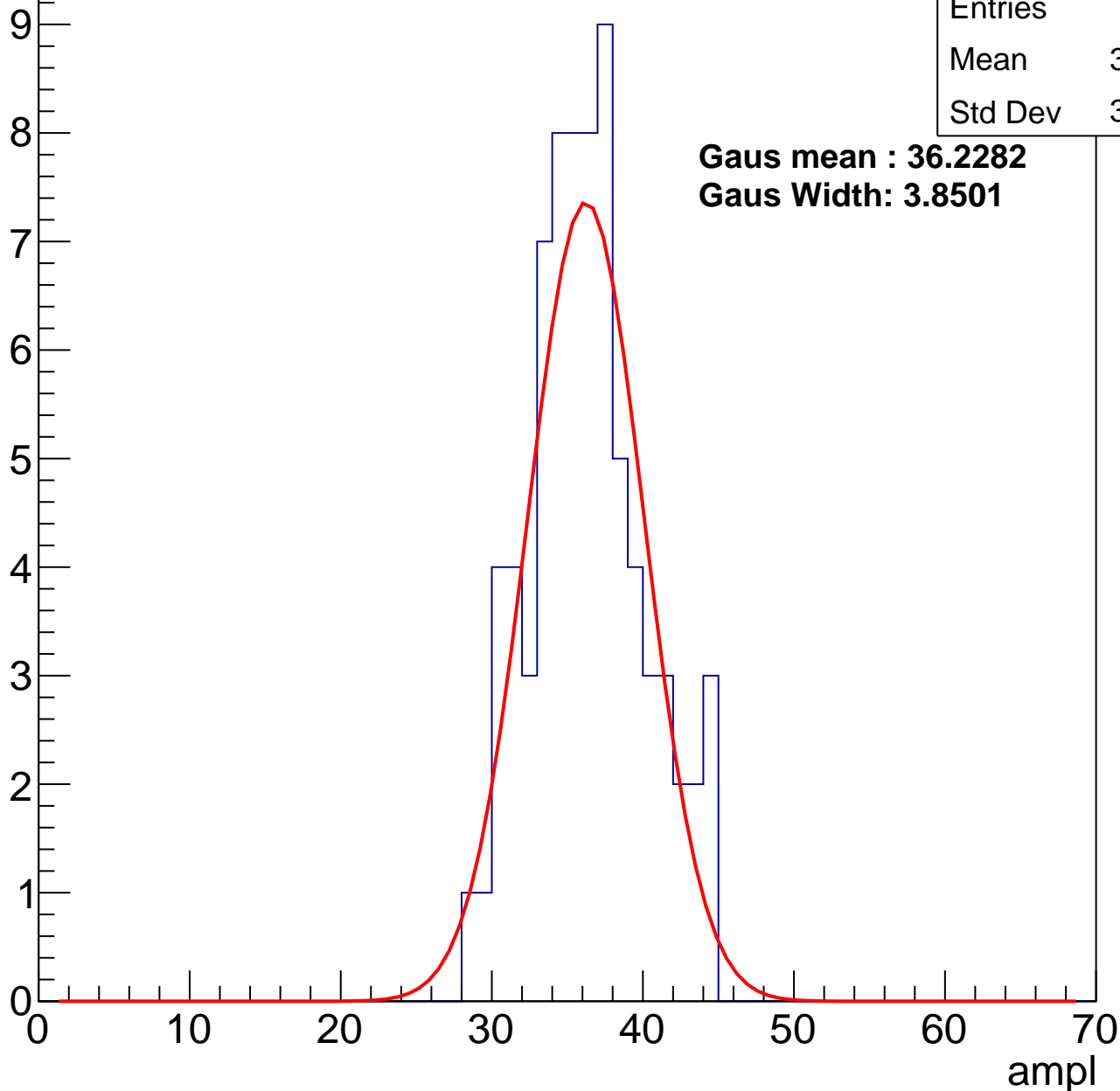
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	35.89
Std Dev	3.754

**Gaus mean : 36.2282**

**Gaus Width: 3.8501**



# B1L101S, U9-ch42, adc2

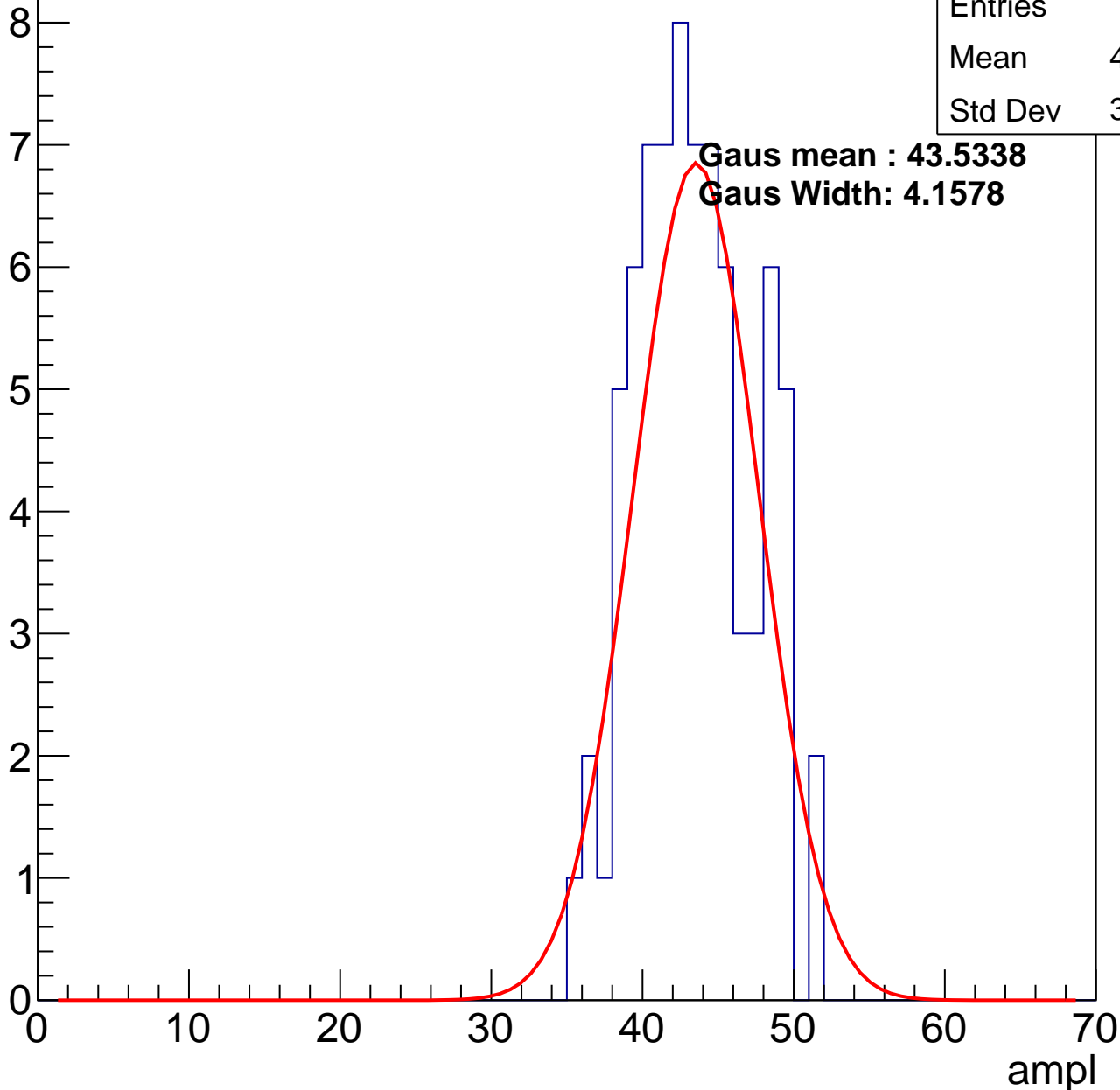
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	42.95
Std Dev	3.773

**Gaus mean : 43.5338**

**Gaus Width: 4.1578**

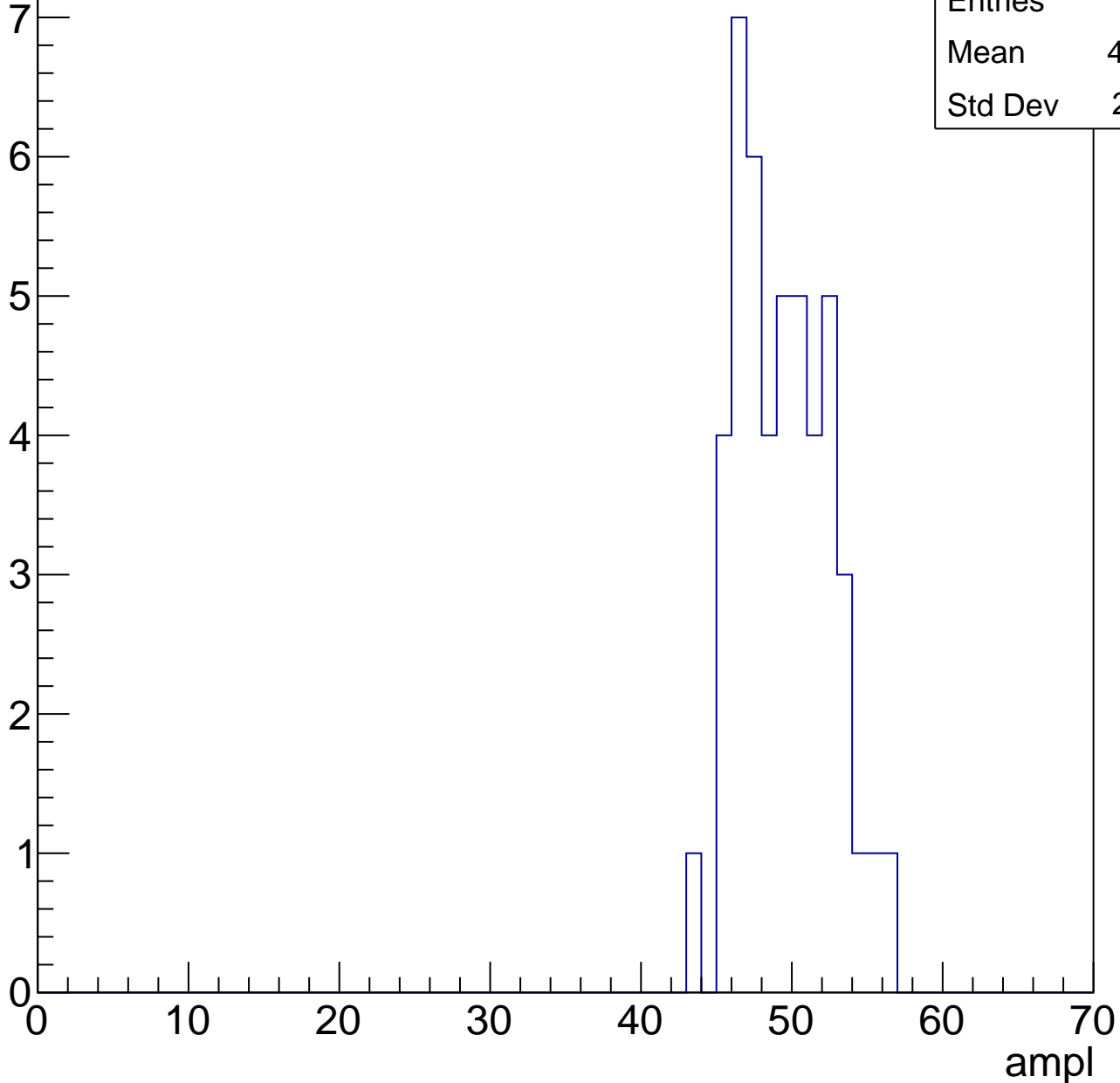


# B1L101S, U9-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	48.98
Std Dev	2.971

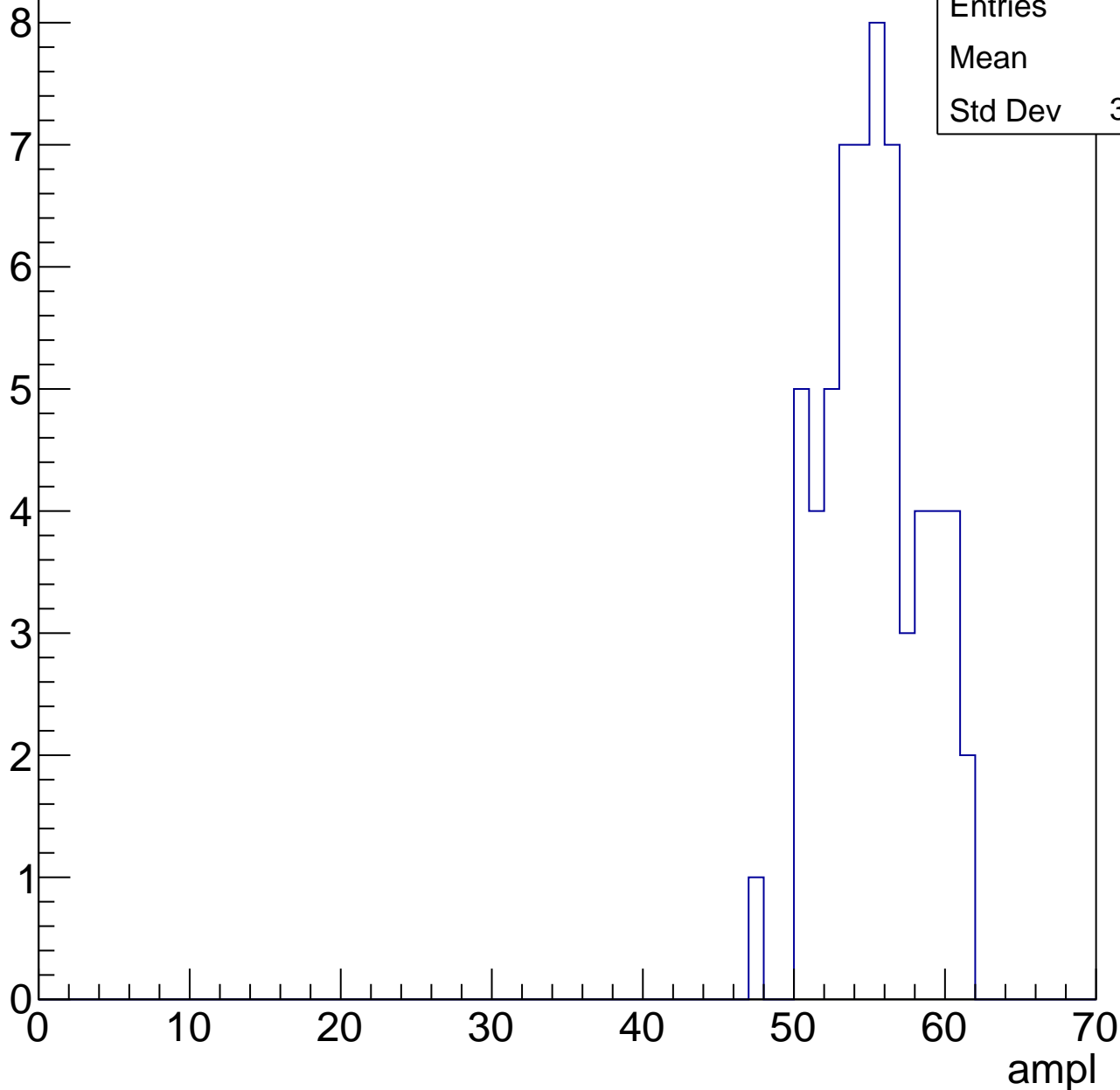


# B1L101S, U9-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	54.8
Std Dev	3.192

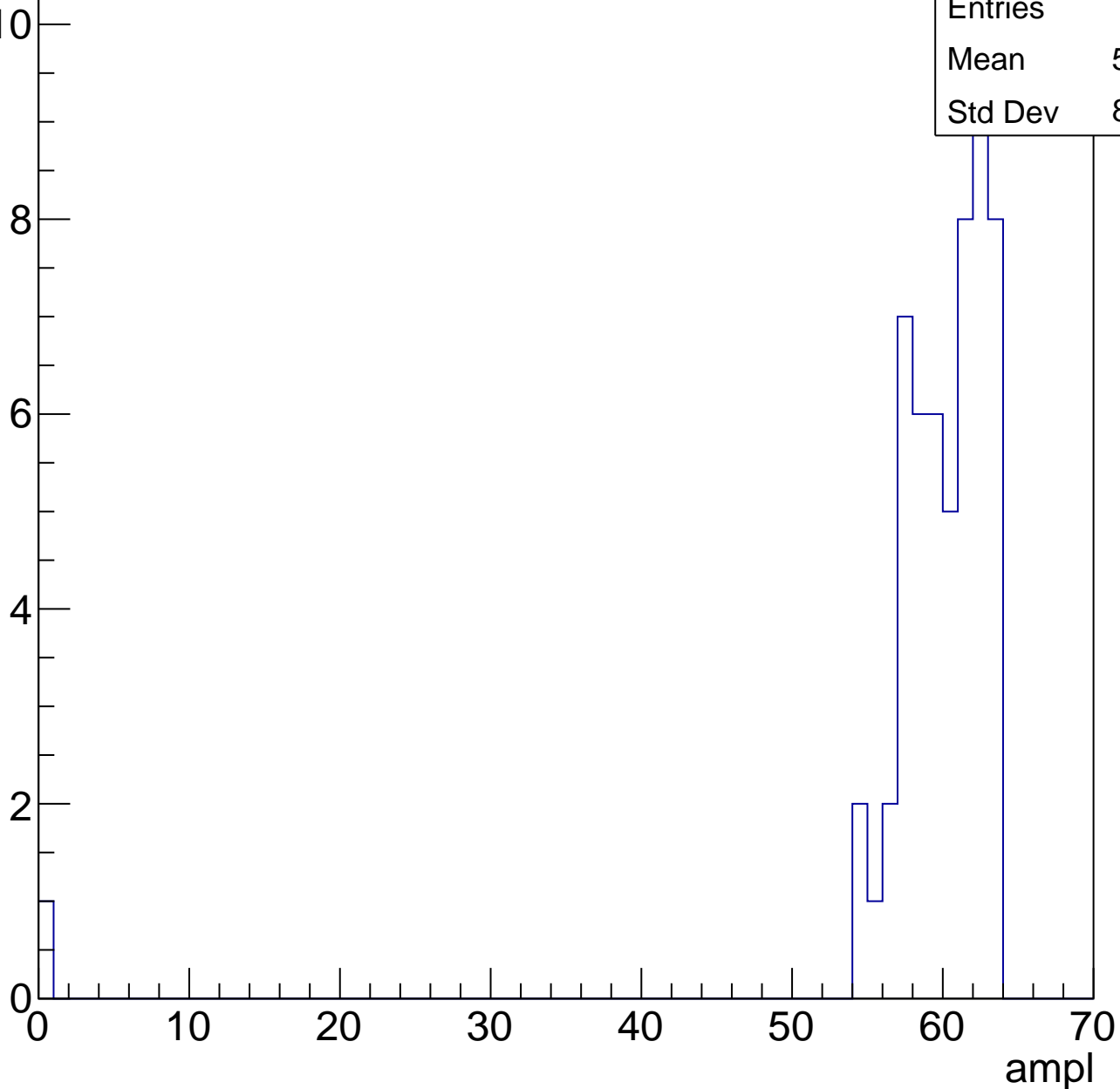


# B1L101S, U9-ch42, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	58.71
Std Dev	8.291



# B1L101S, U9-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	62
Std Dev	1.414



# B1L101S, U9-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U9-ch43, adc0

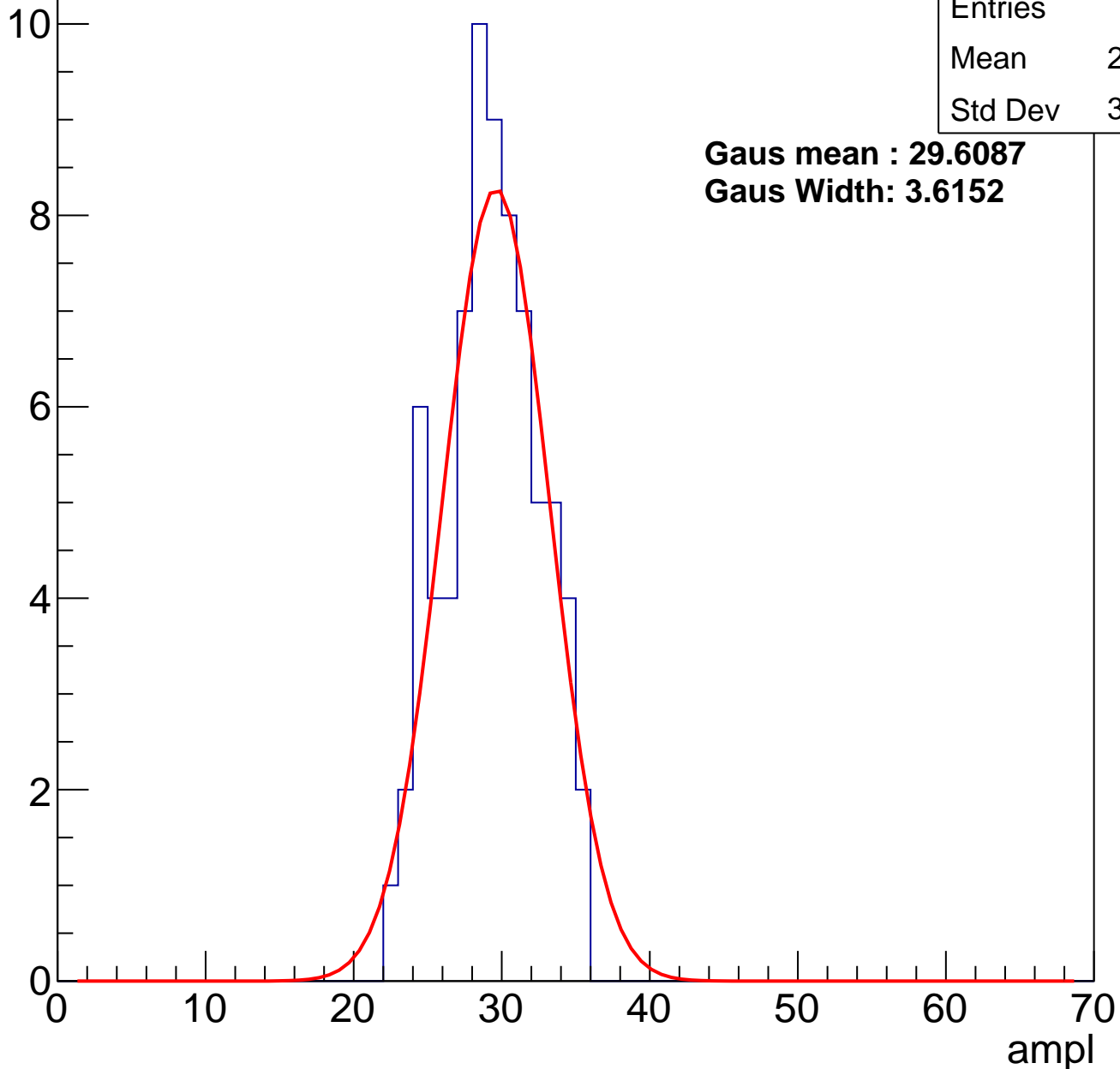
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	74
Mean	28.84
Std Dev	3.162

**Gaus mean : 29.6087**

**Gaus Width: 3.6152**

Entry



# B1L101S, U9-ch43, adc1

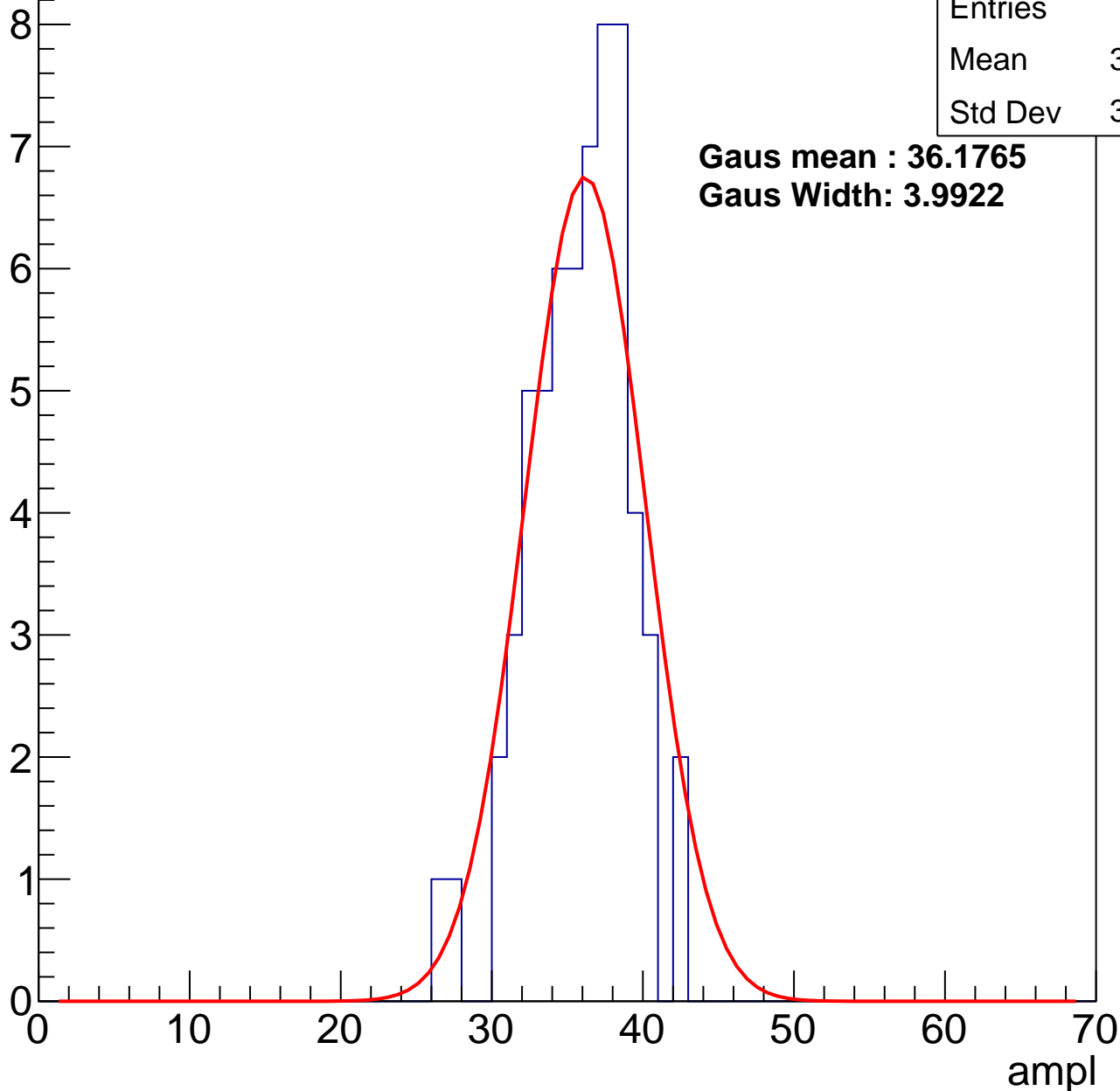
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	35.36
Std Dev	3.275

**Gaus mean : 36.1765**

**Gaus Width: 3.9922**



# B1L101S, U9-ch43, adc2

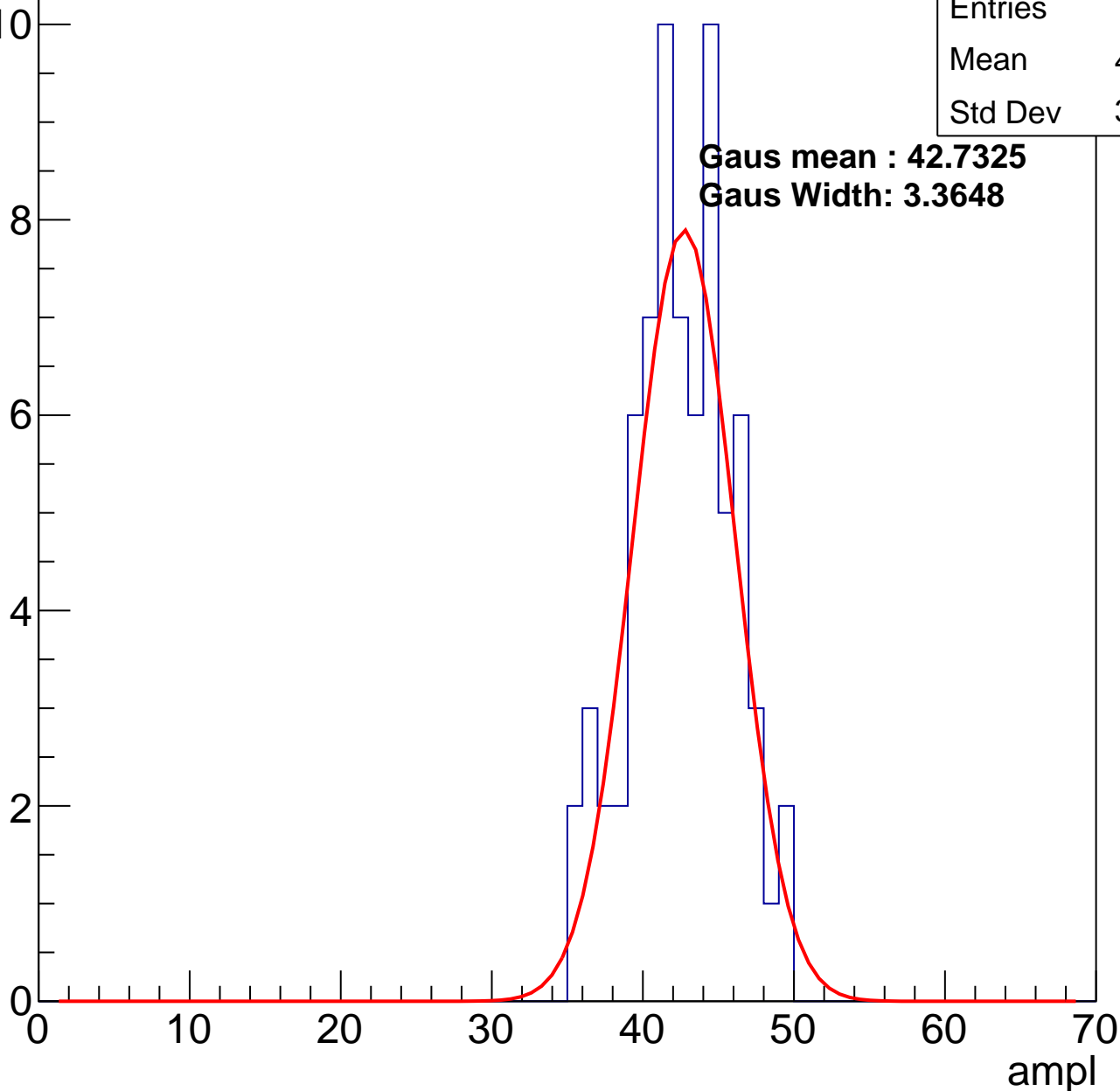
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	42.11
Std Dev	3.281

**Gaus mean : 42.7325**

**Gaus Width: 3.3648**

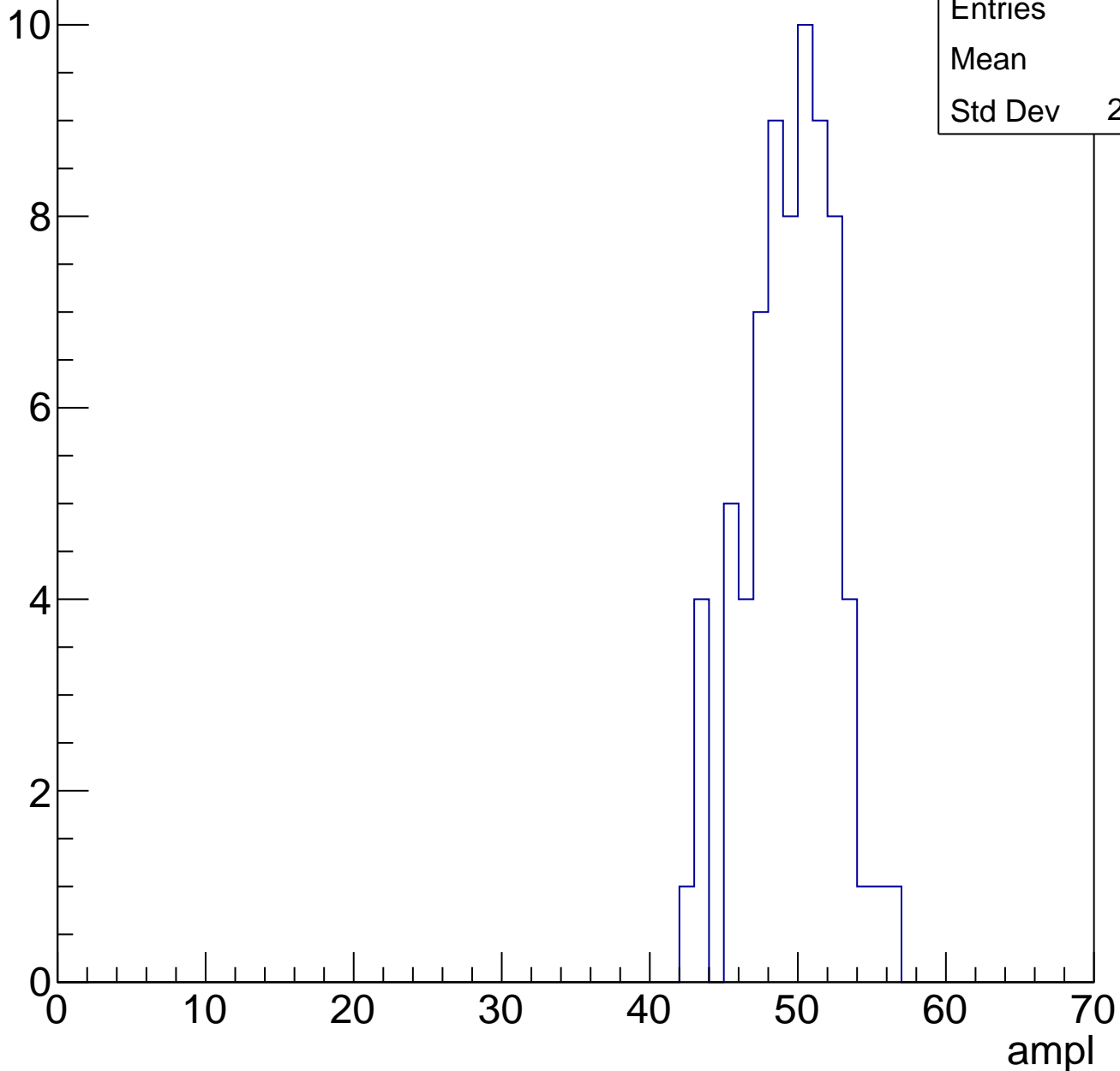


# B1L101S, U9-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

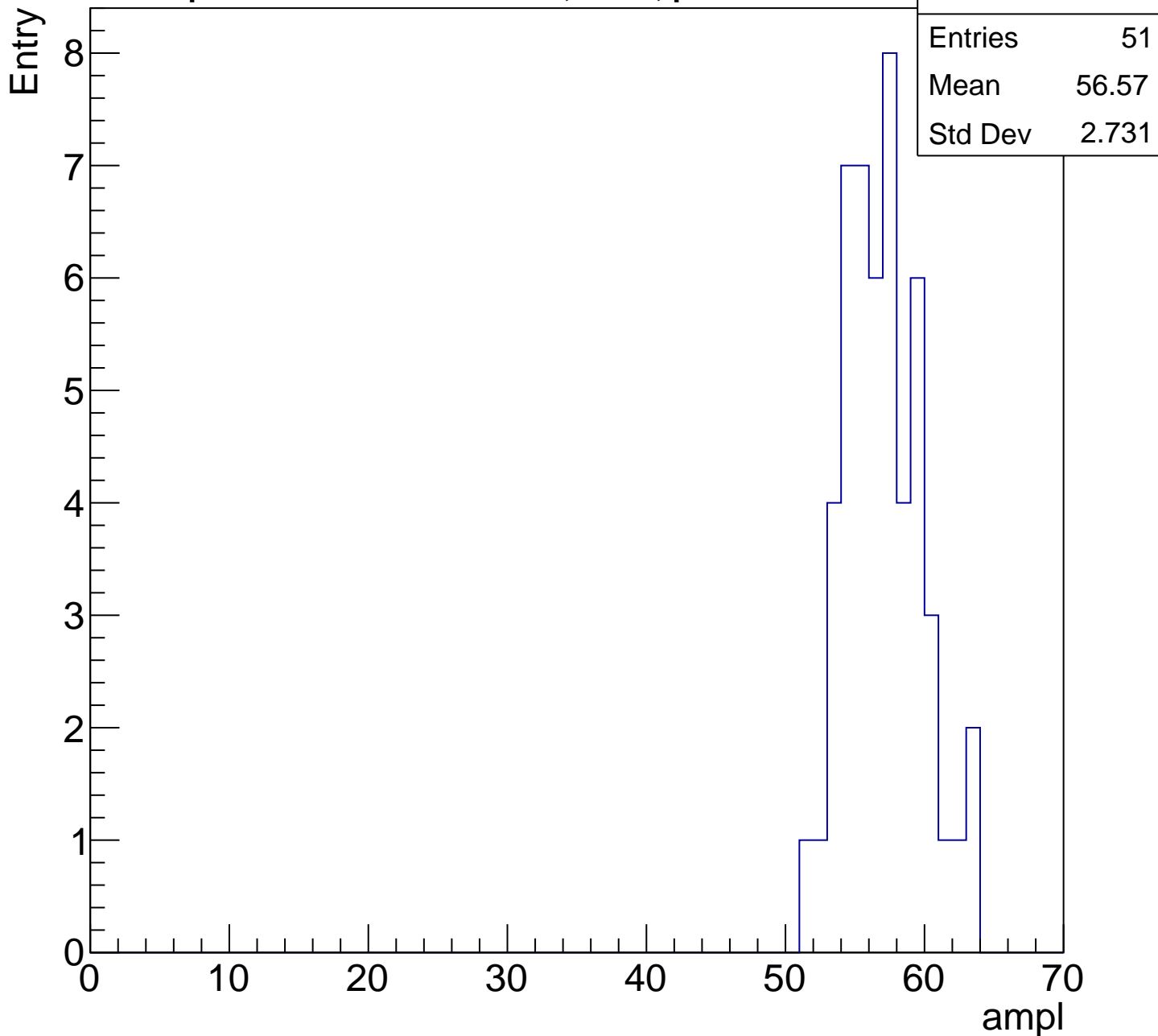
Entry

Entries	72
Mean	49
Std Dev	2.977



# B1L101S, U9-ch43, adc4

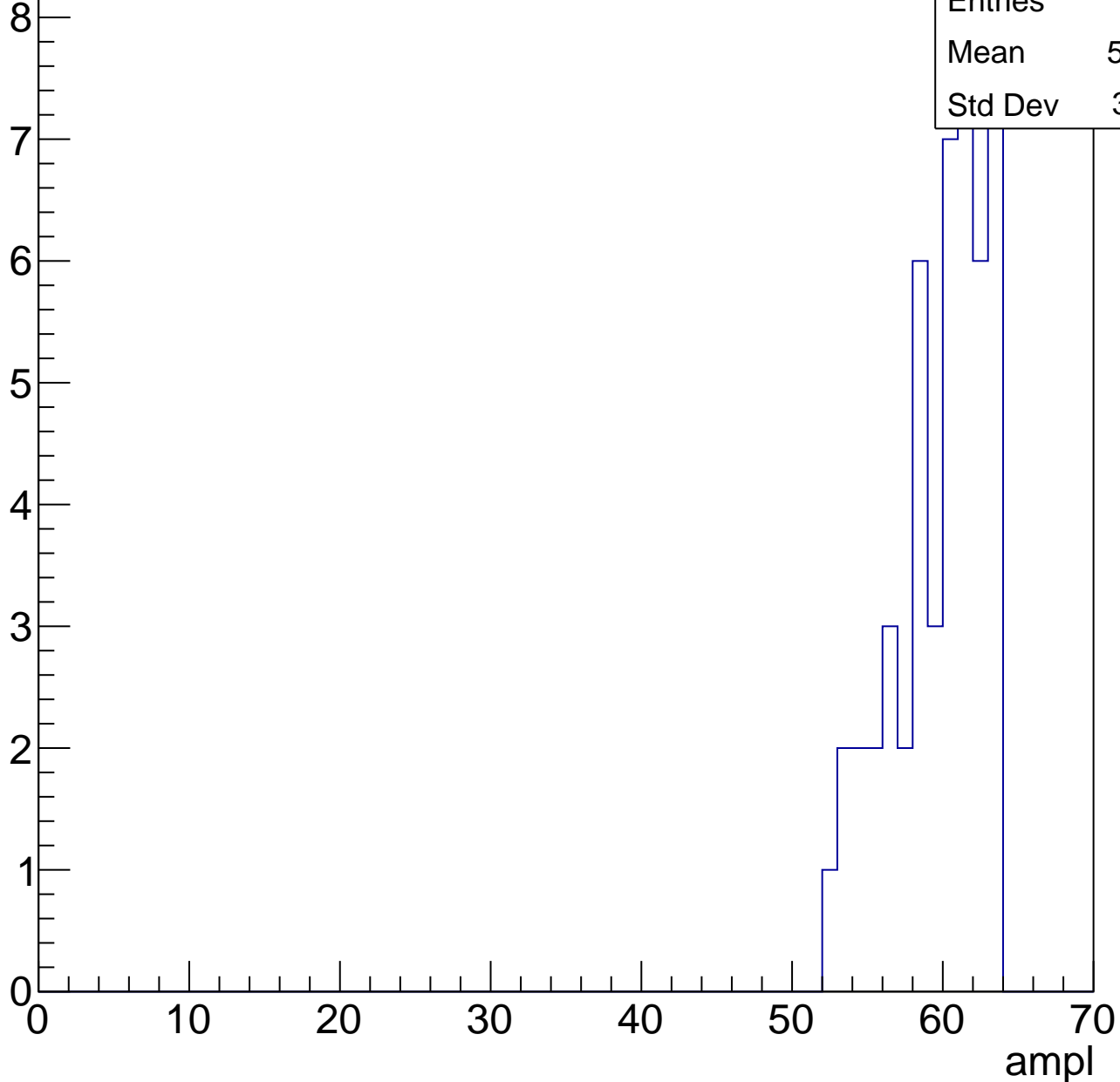
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

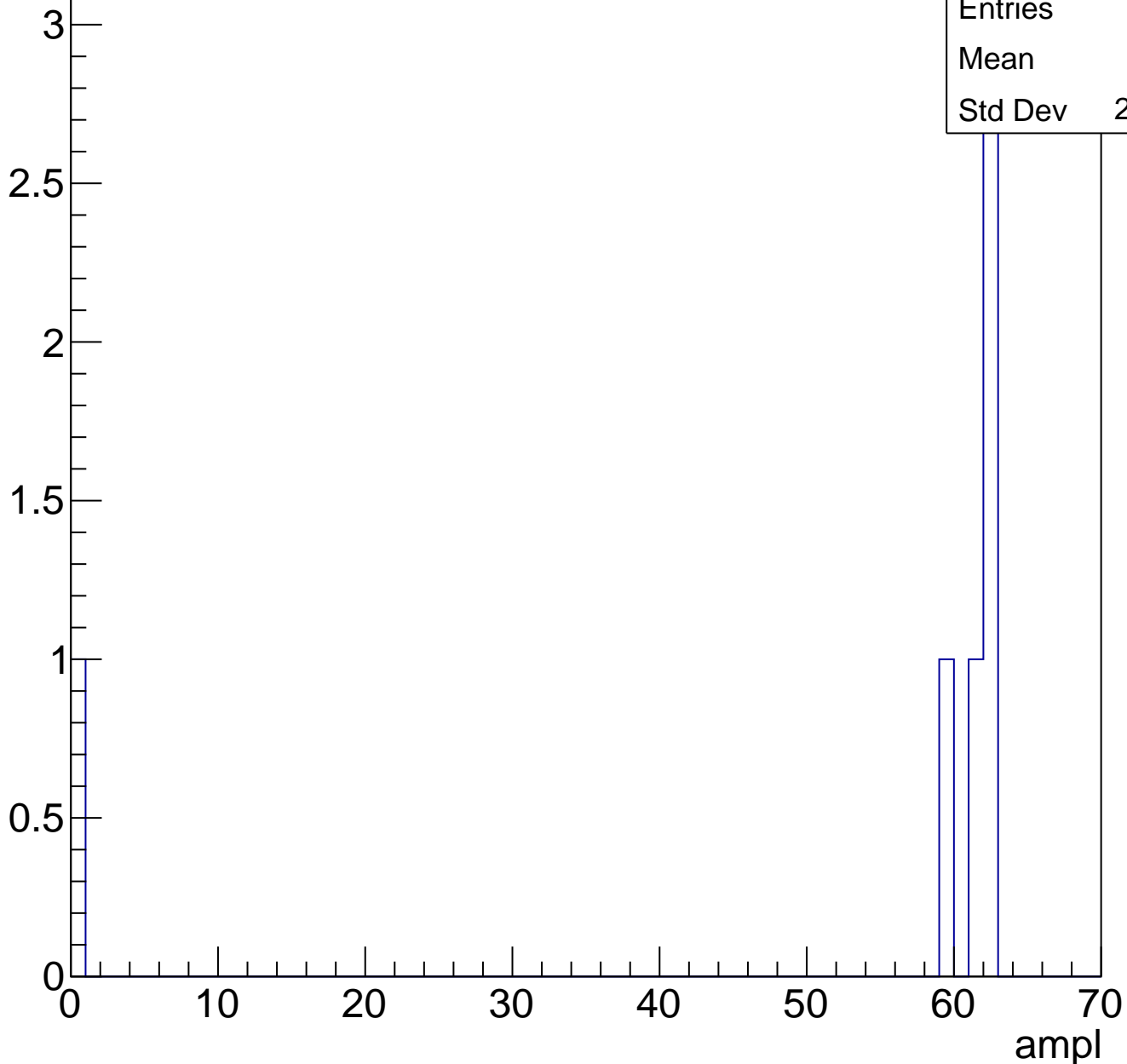
Entry



# B1L101S, U9-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U9-ch44, adc0

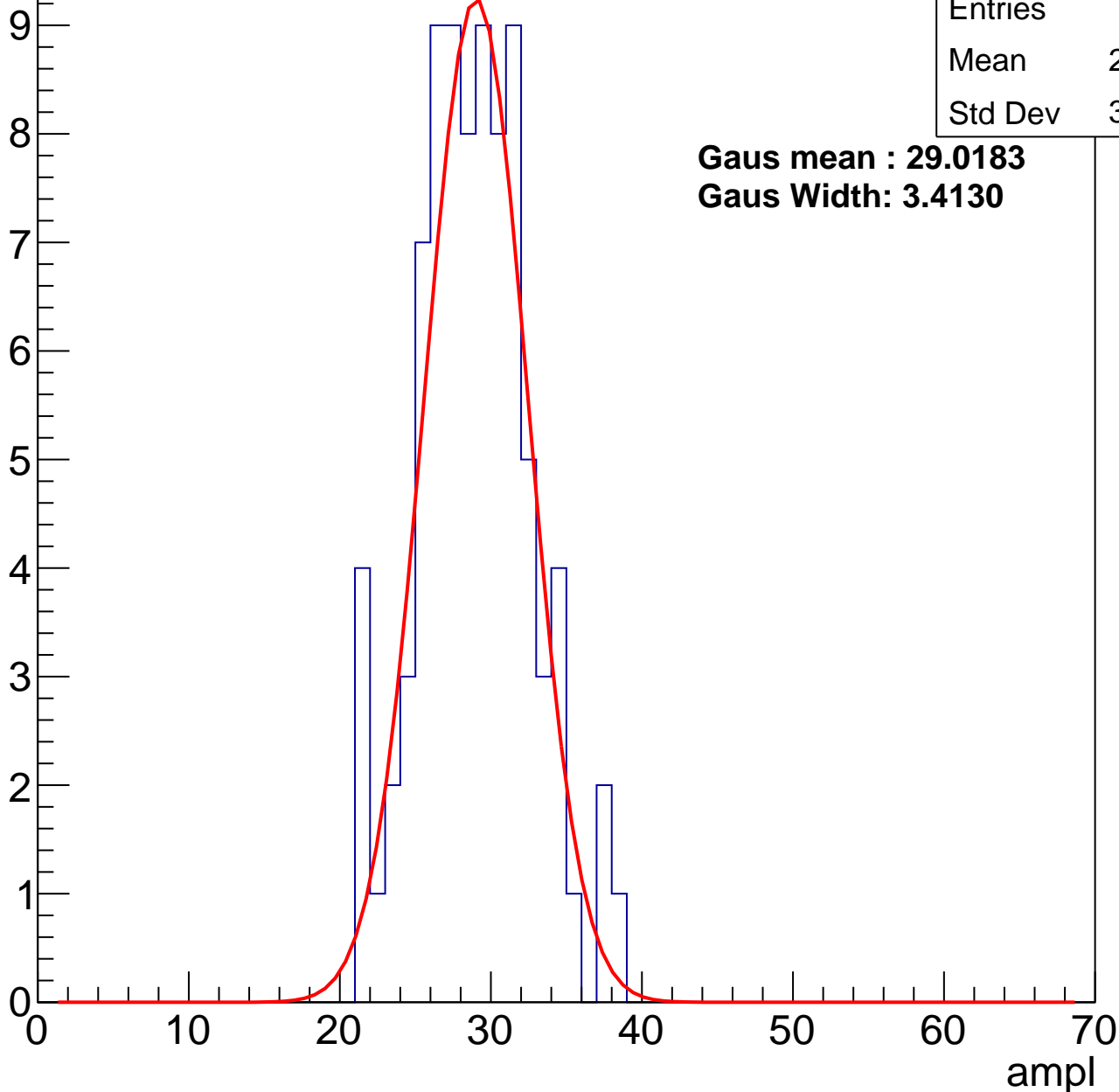
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	85
Mean	28.49
Std Dev	3.677

**Gaus mean : 29.0183**

**Gaus Width: 3.4130**



# B1L101S, U9-ch44, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	59
Mean	35.59
Std Dev	3.026

**Gaus mean : 36.0131**

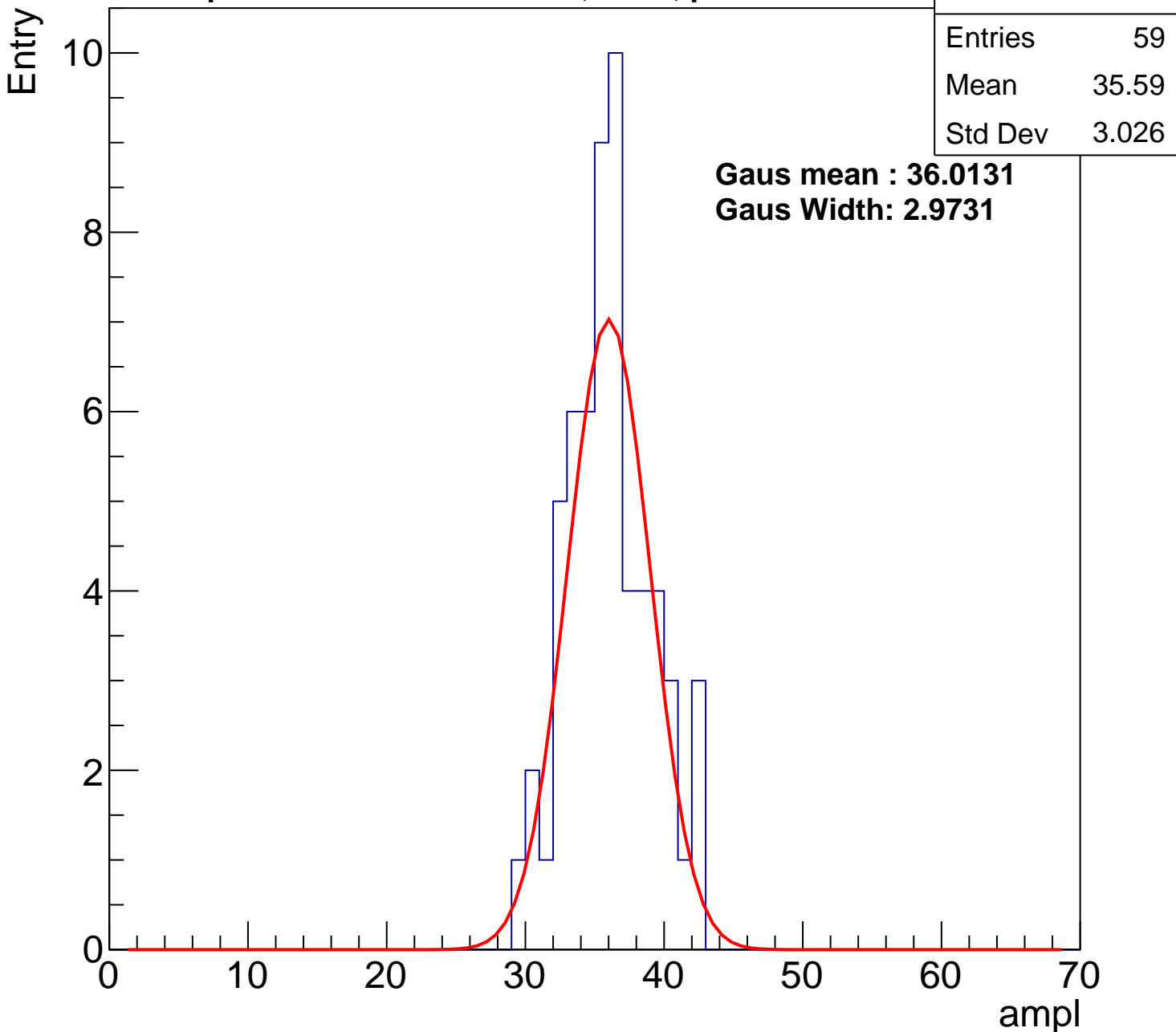
**Gaus Width: 2.9731**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U9-ch44, adc2

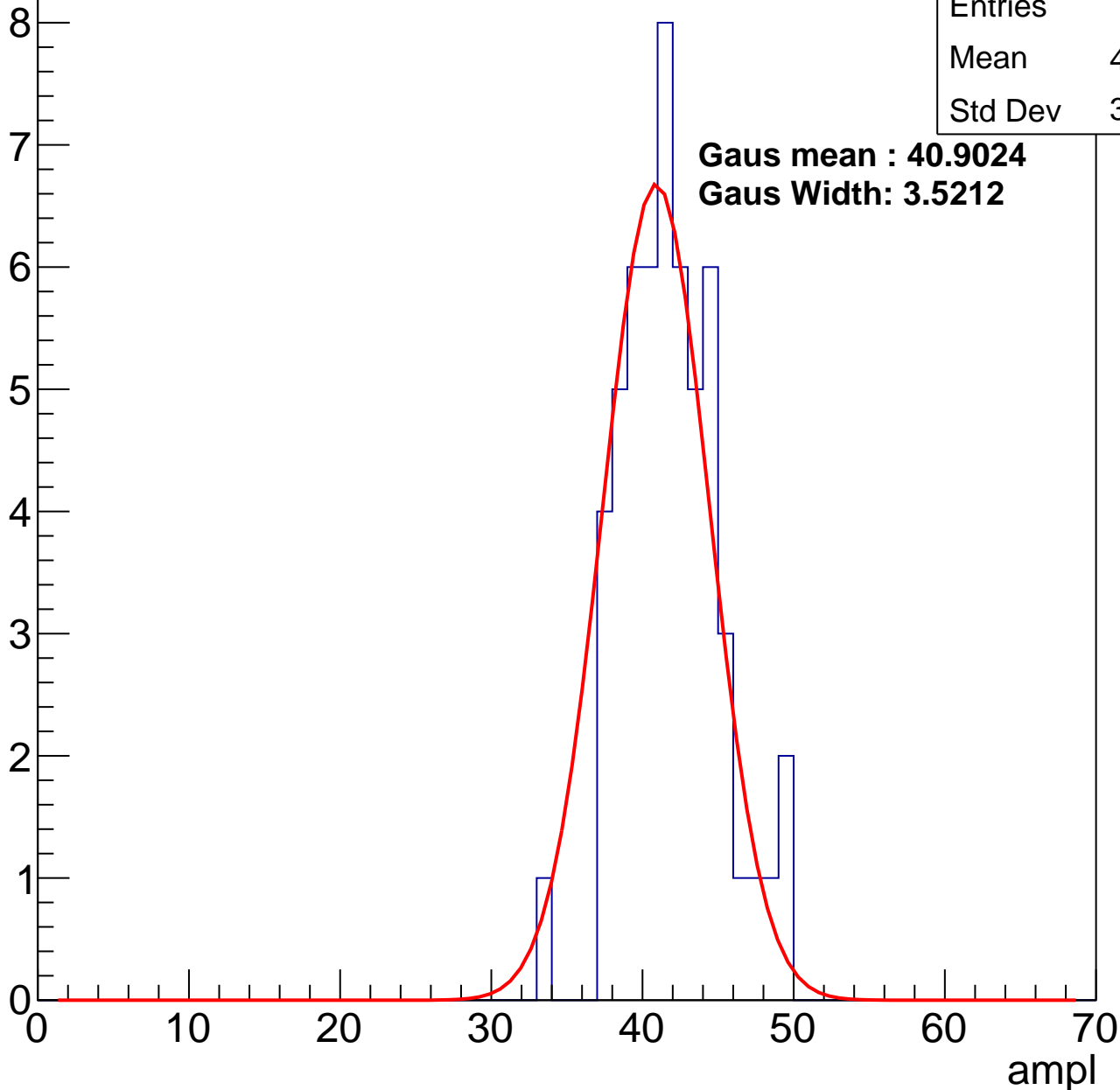
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	41.42
Std Dev	3.189

**Gaus mean : 40.9024**

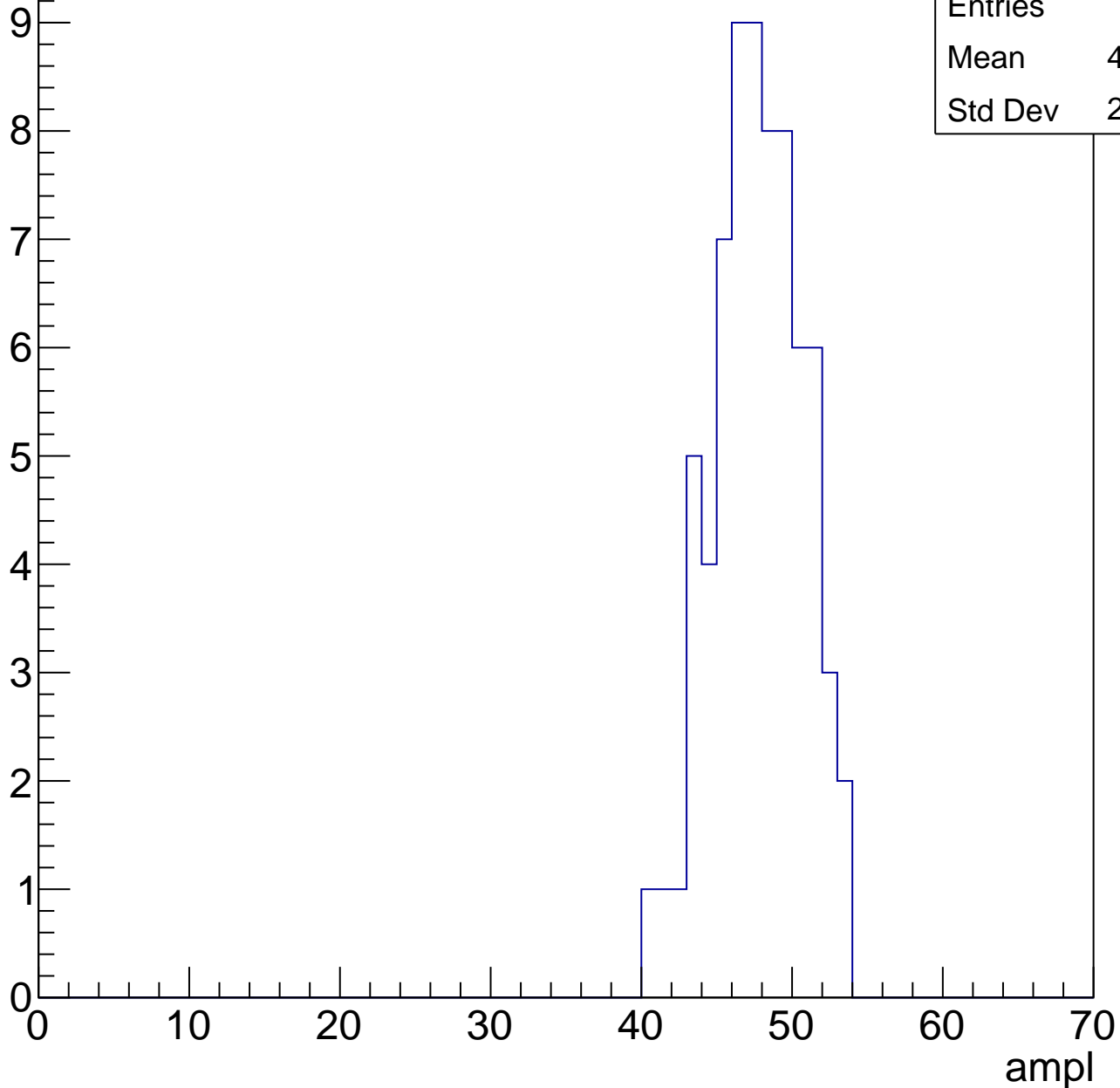
**Gaus Width: 3.5212**



# B1L101S, U9-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



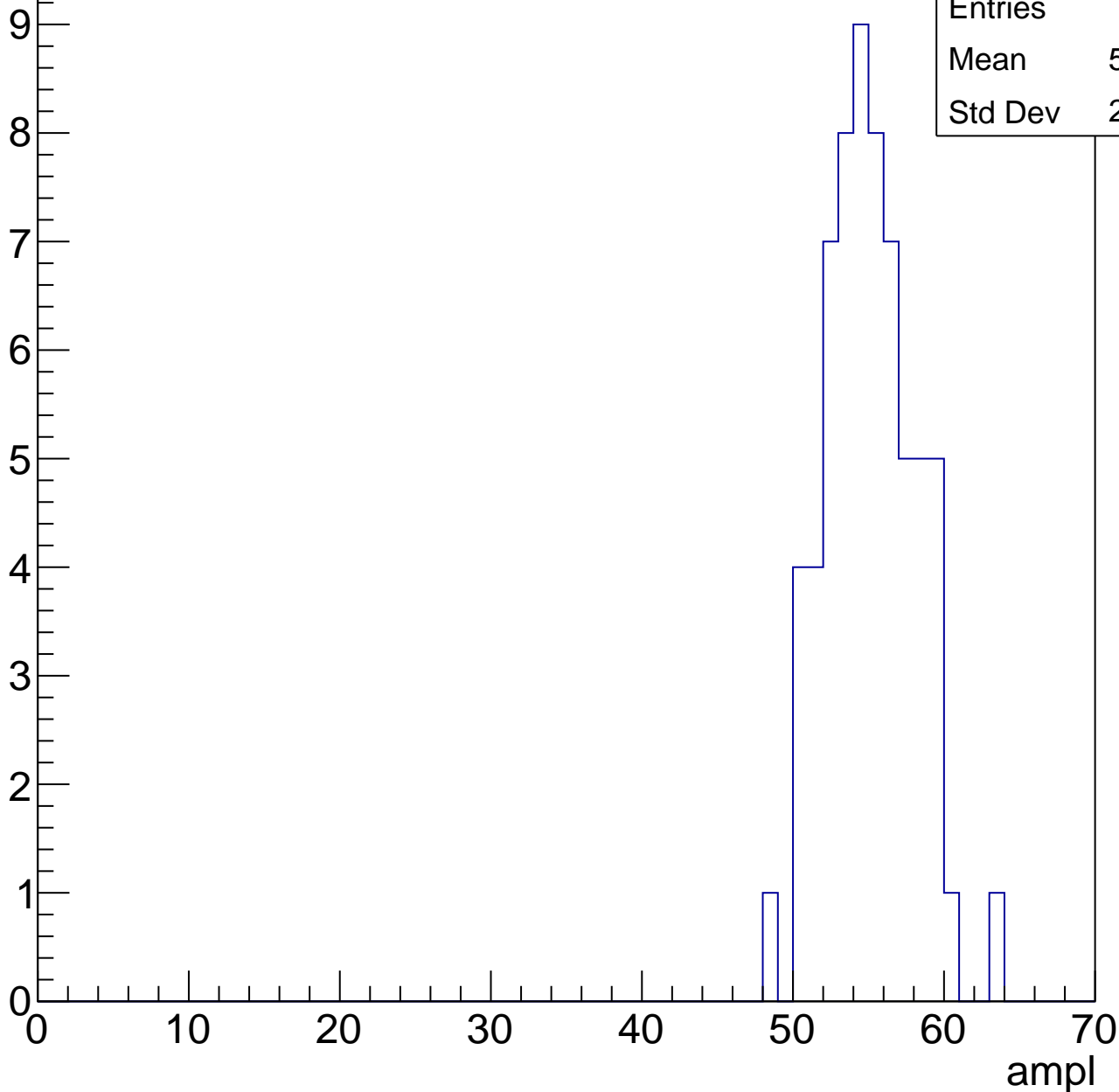
Entries	70
Mean	47.29
Std Dev	2.914

# B1L101S, U9-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	54.63
Std Dev	2.907



# B1L101S, U9-ch44, adc5

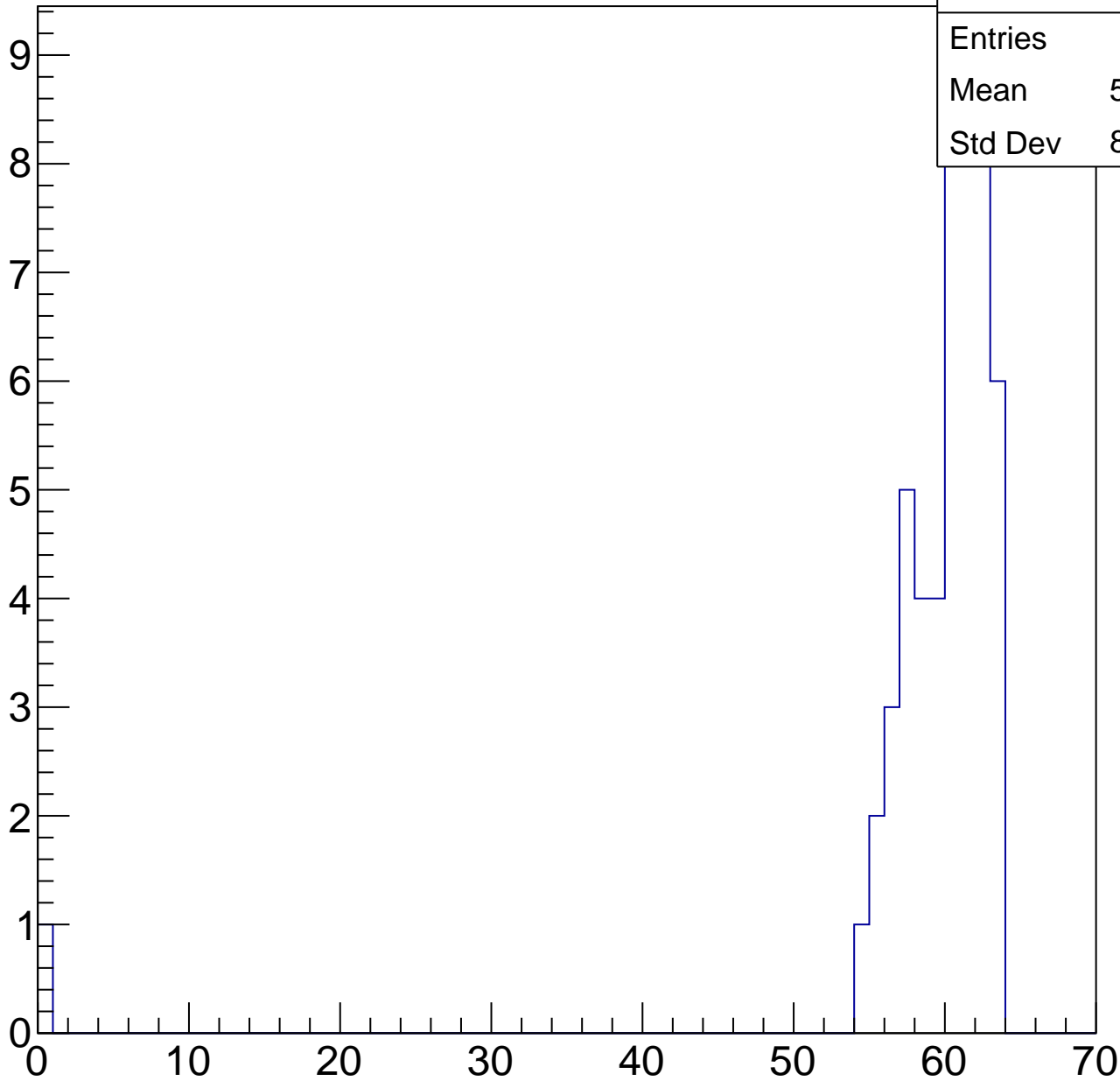
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	58.59
Std Dev	8.623

ampl



# B1L101S, U9-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

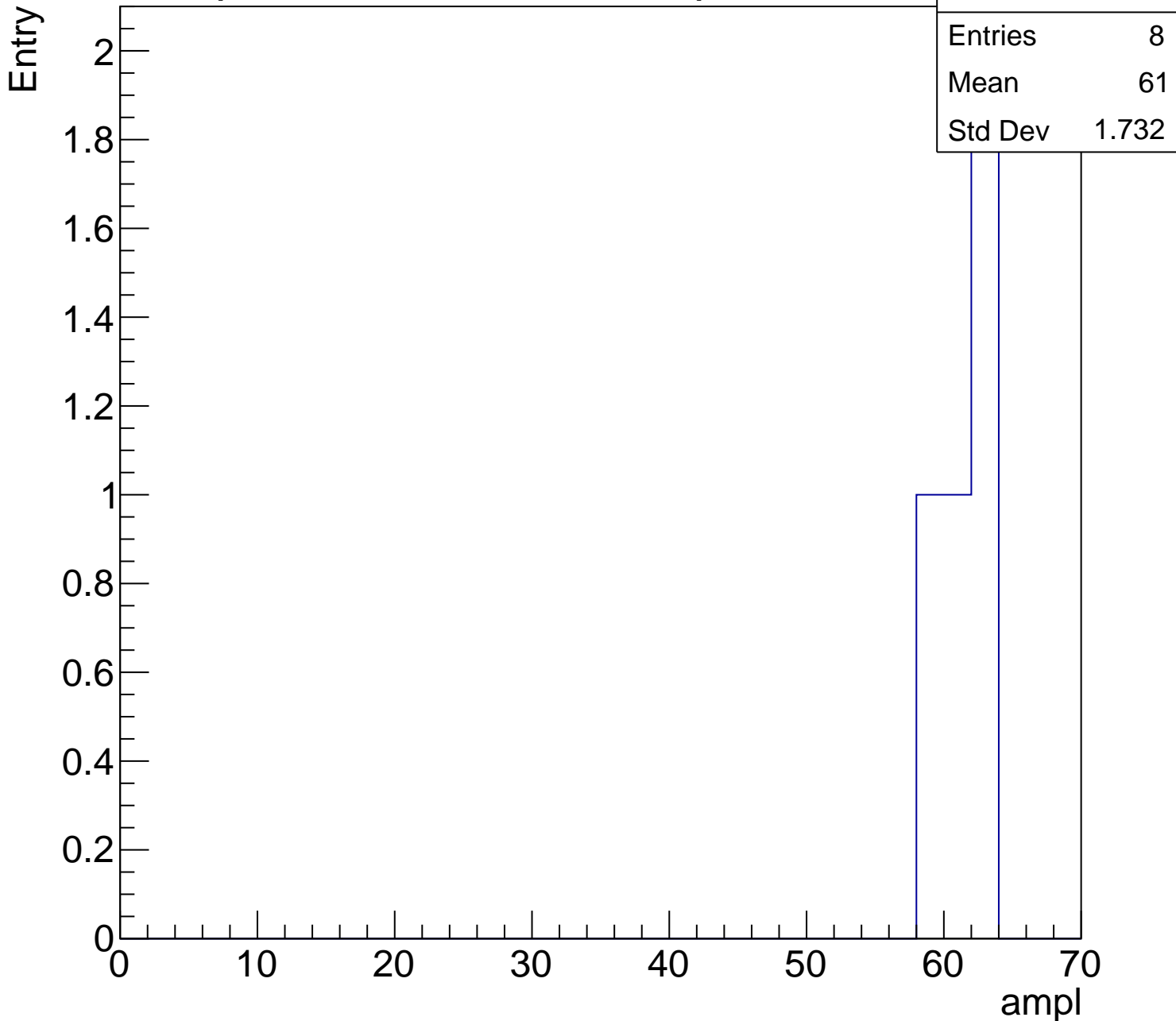
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	8
Mean	61
Std Dev	1.732

ampl

0 10 20 30 40 50 60 70





# B1L101S, U9-ch44, adc7

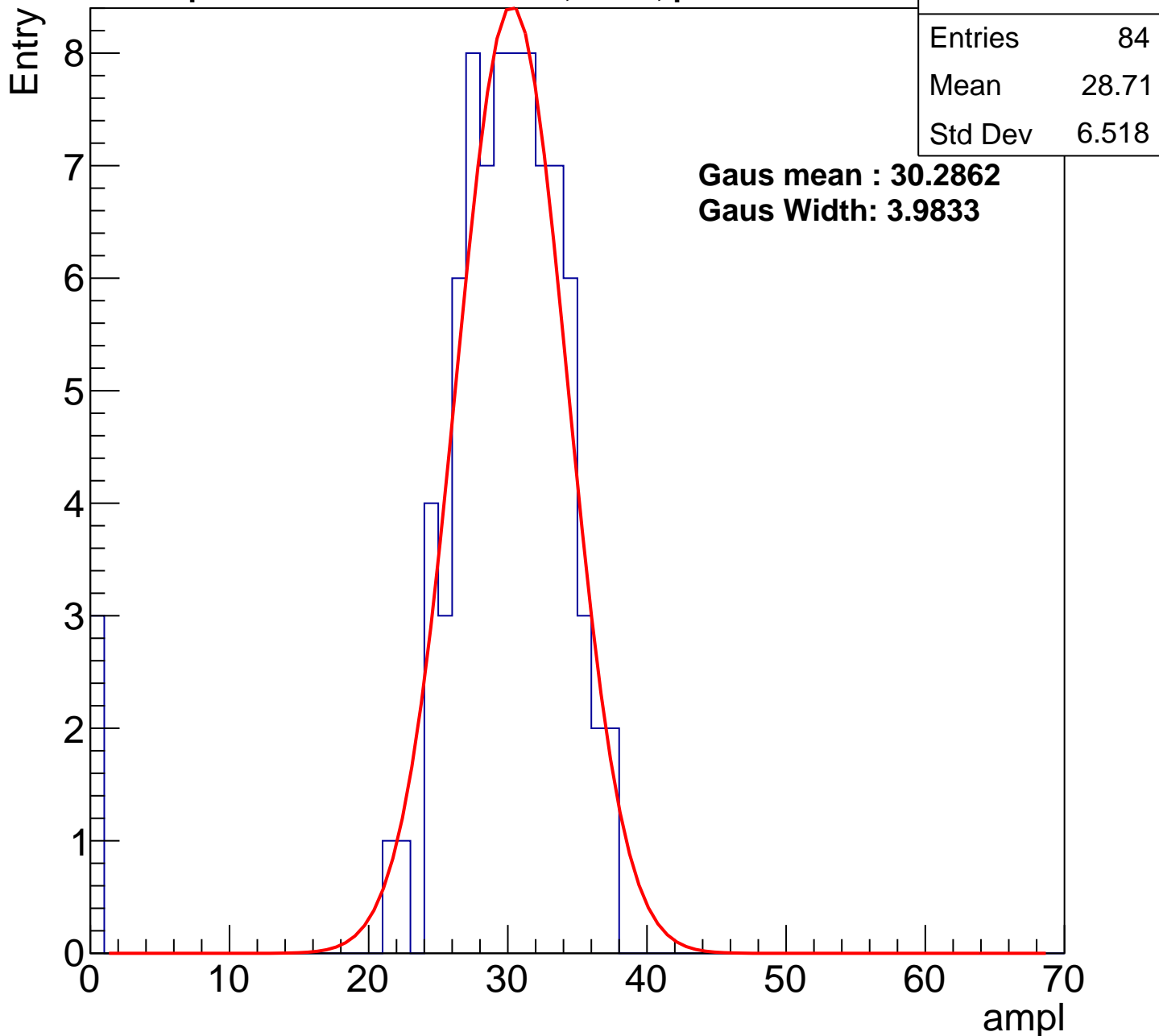
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch45, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch45, adc1

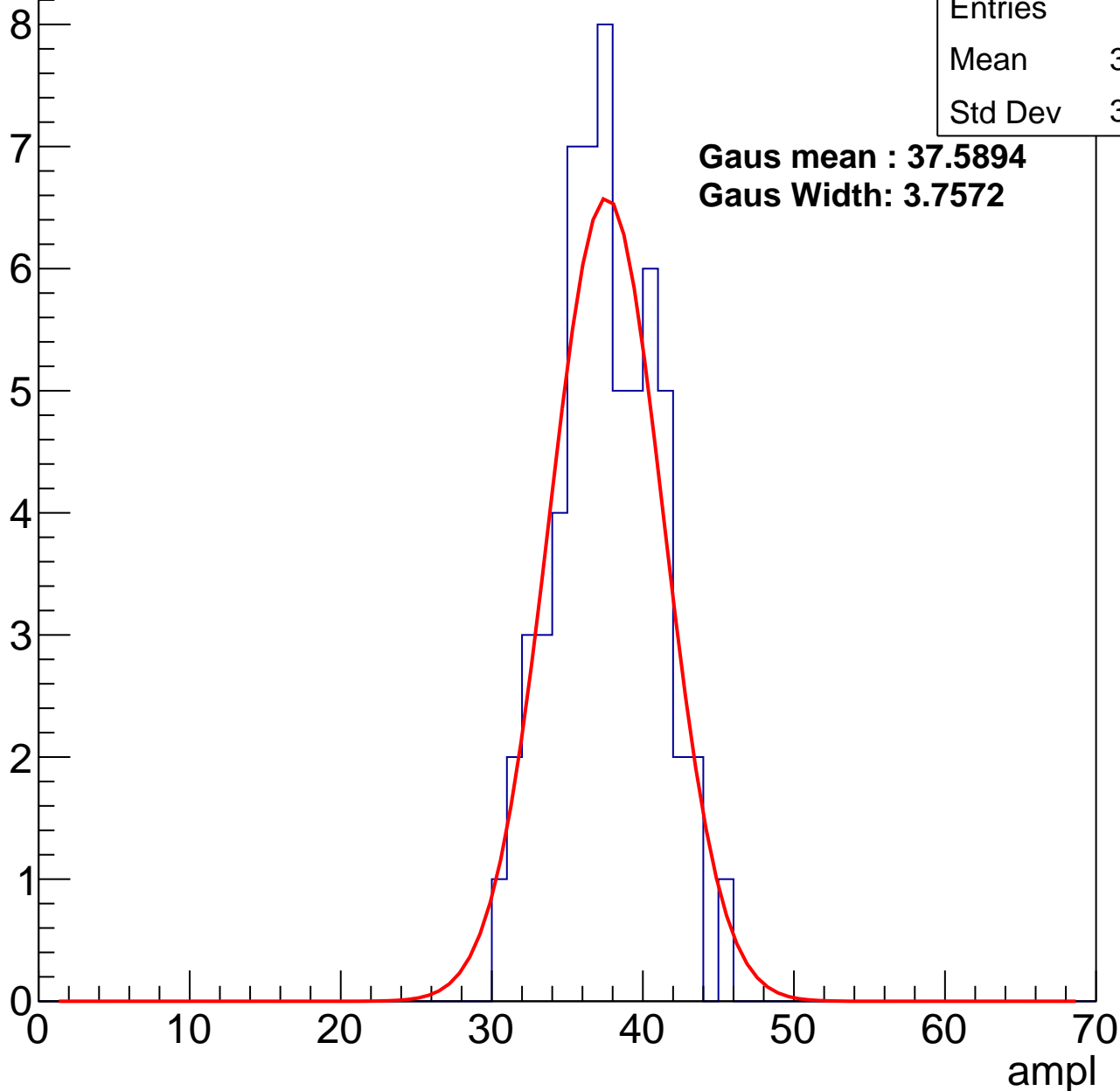
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	37.07
Std Dev	3.289

**Gaus mean : 37.5894**

**Gaus Width: 3.7572**



# B1L101S, U9-ch45, adc2

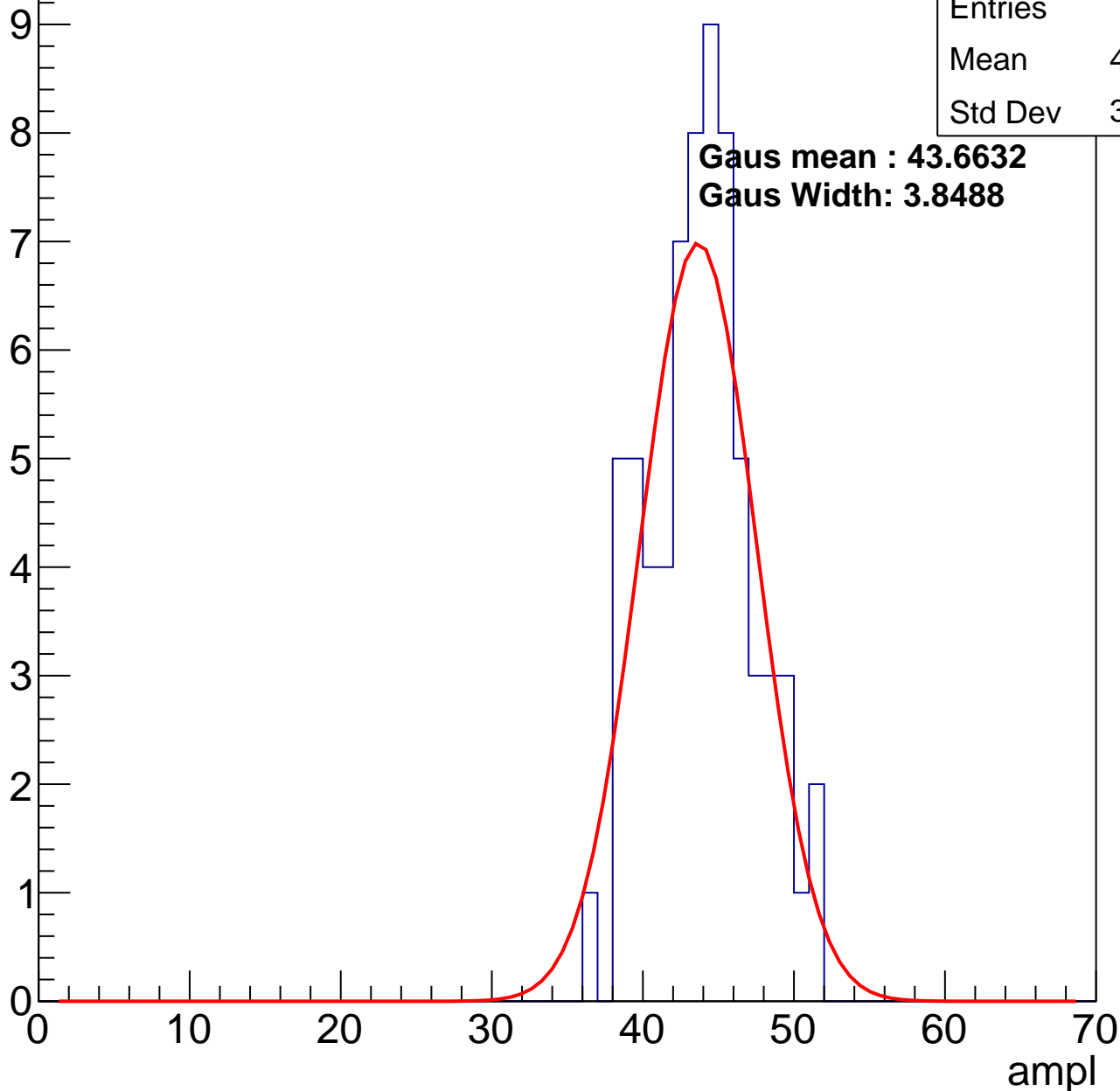
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	43.43
Std Dev	3.418

**Gaus mean : 43.6632**

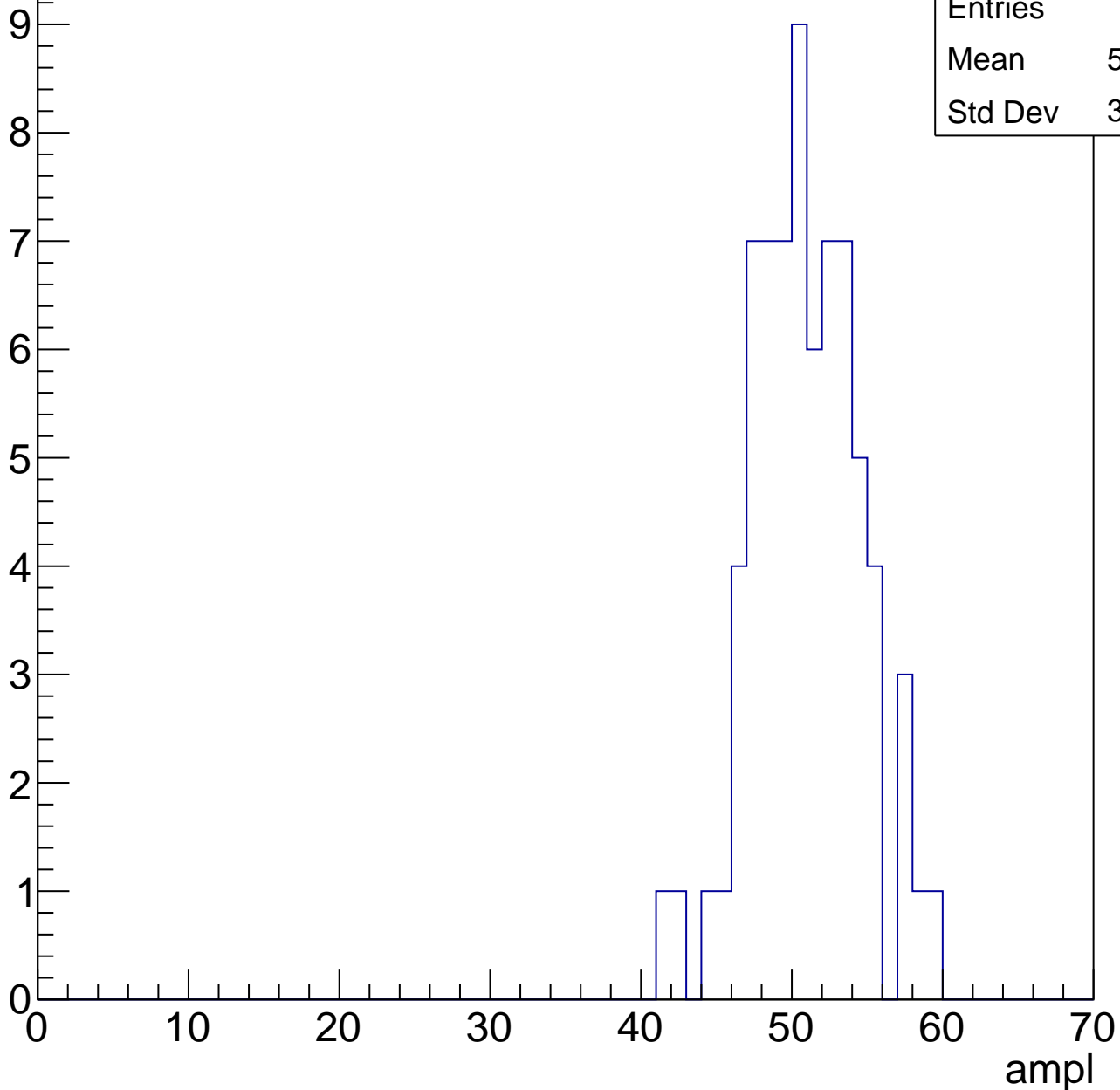
**Gaus Width: 3.8488**



# B1L101S, U9-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

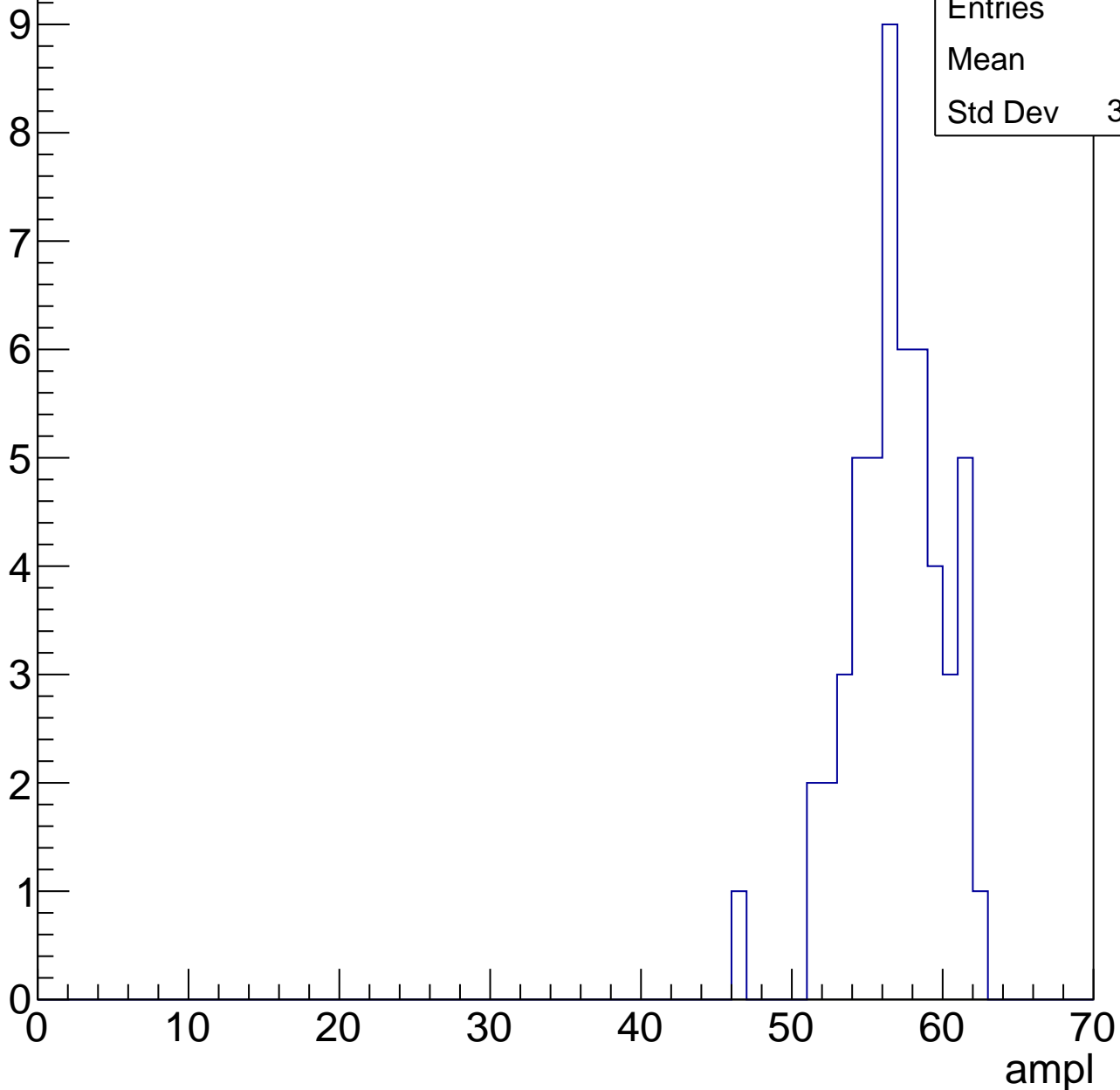


# B1L101S, U9-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	56.4
Std Dev	3.102



# B1L101S, U9-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

Entries 38

Mean 58.63

Std Dev 9.94

ampl

0

10

20

30

40

50

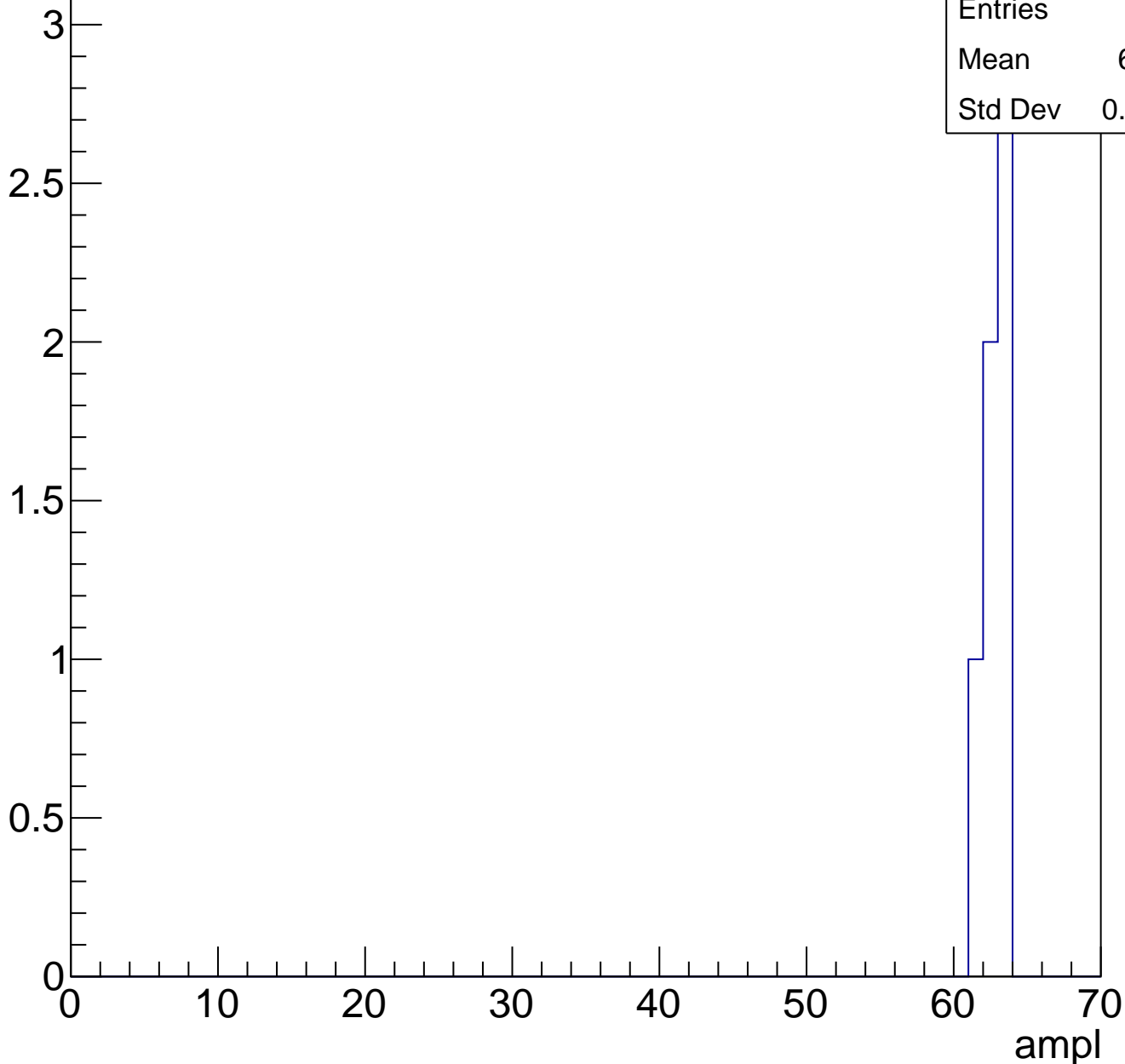
60

70

# B1L101S, U9-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

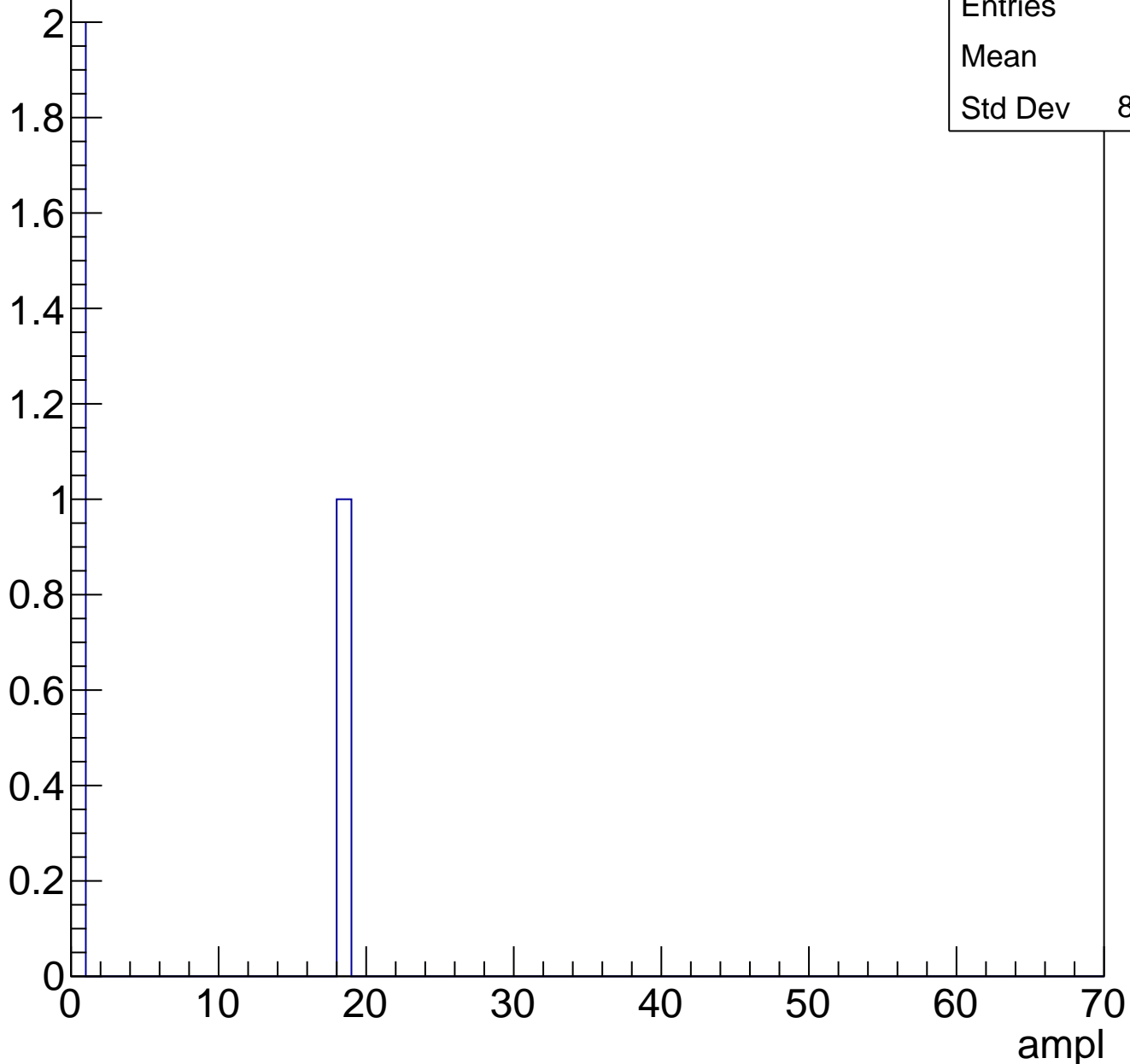




# B1L101S, U9-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	6
Std Dev	8.485

# B1L101S, U9-ch46, adc0

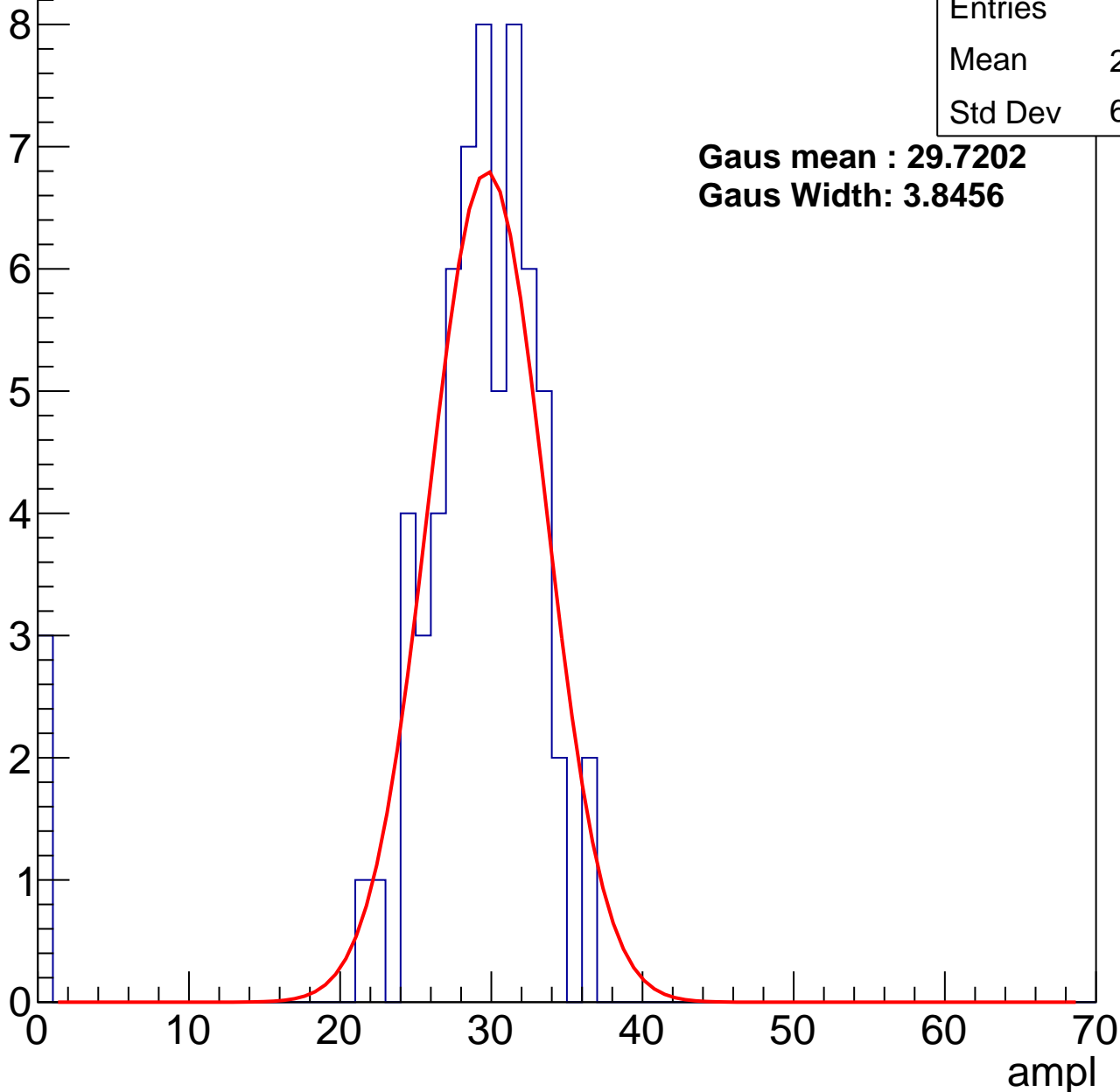
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	27.74
Std Dev	6.869

**Gaus mean : 29.7202**

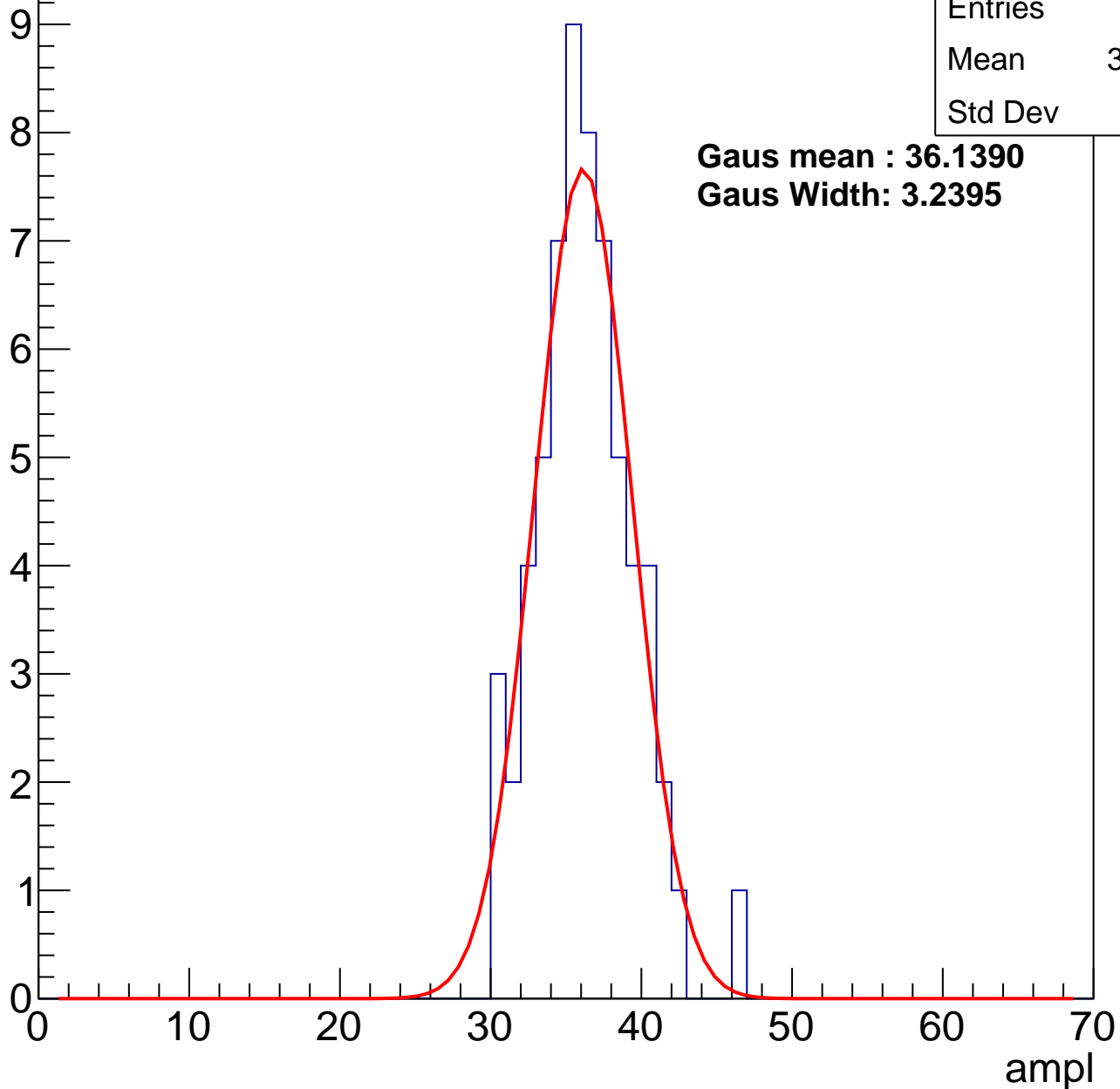
**Gaus Width: 3.8456**



# B1L101S, U9-ch46, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch46, adc2

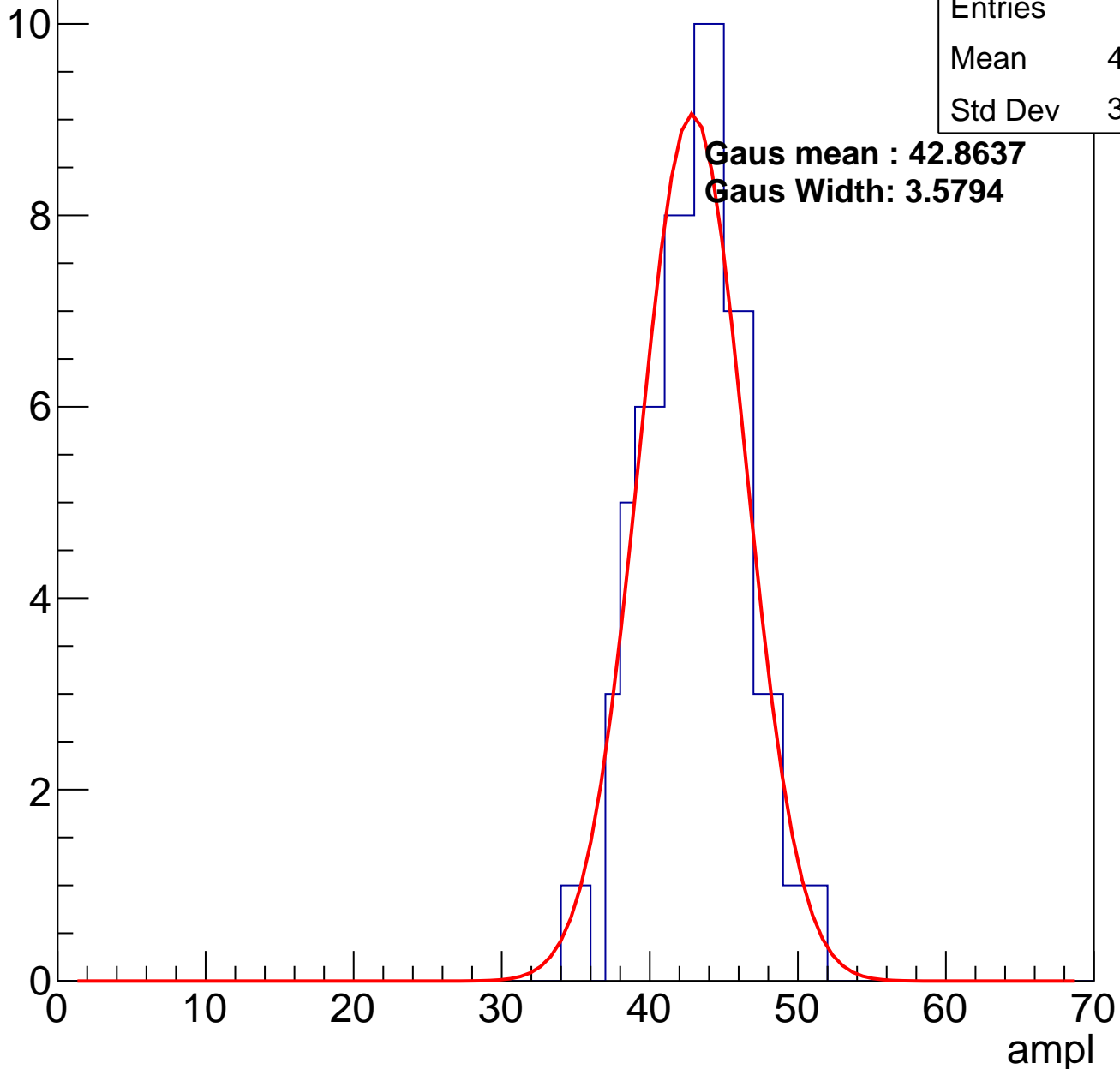
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	81
Mean	42.59
Std Dev	3.384

**Gaus mean : 42.8637**

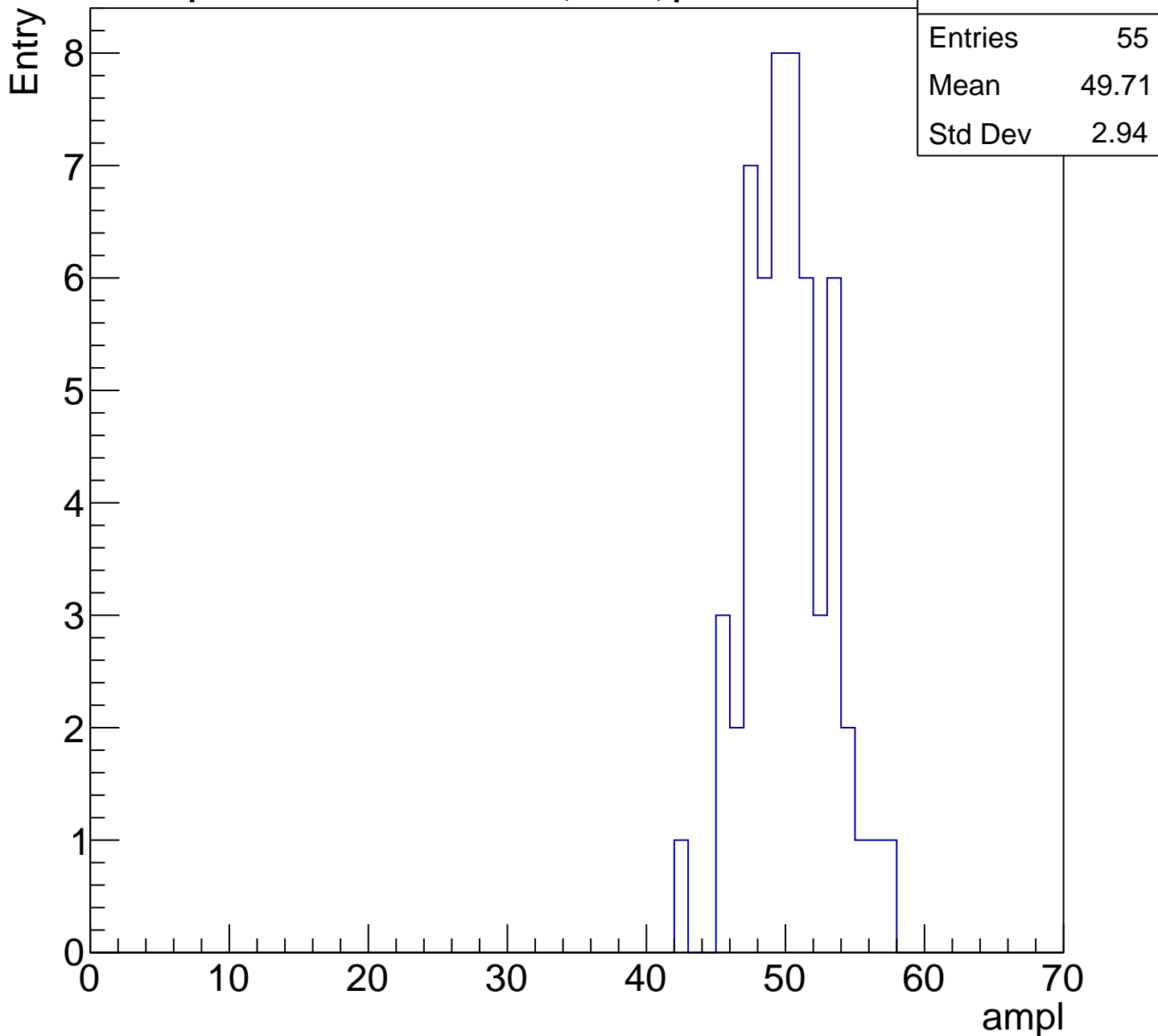
**Gaus Width: 3.5794**

Entry



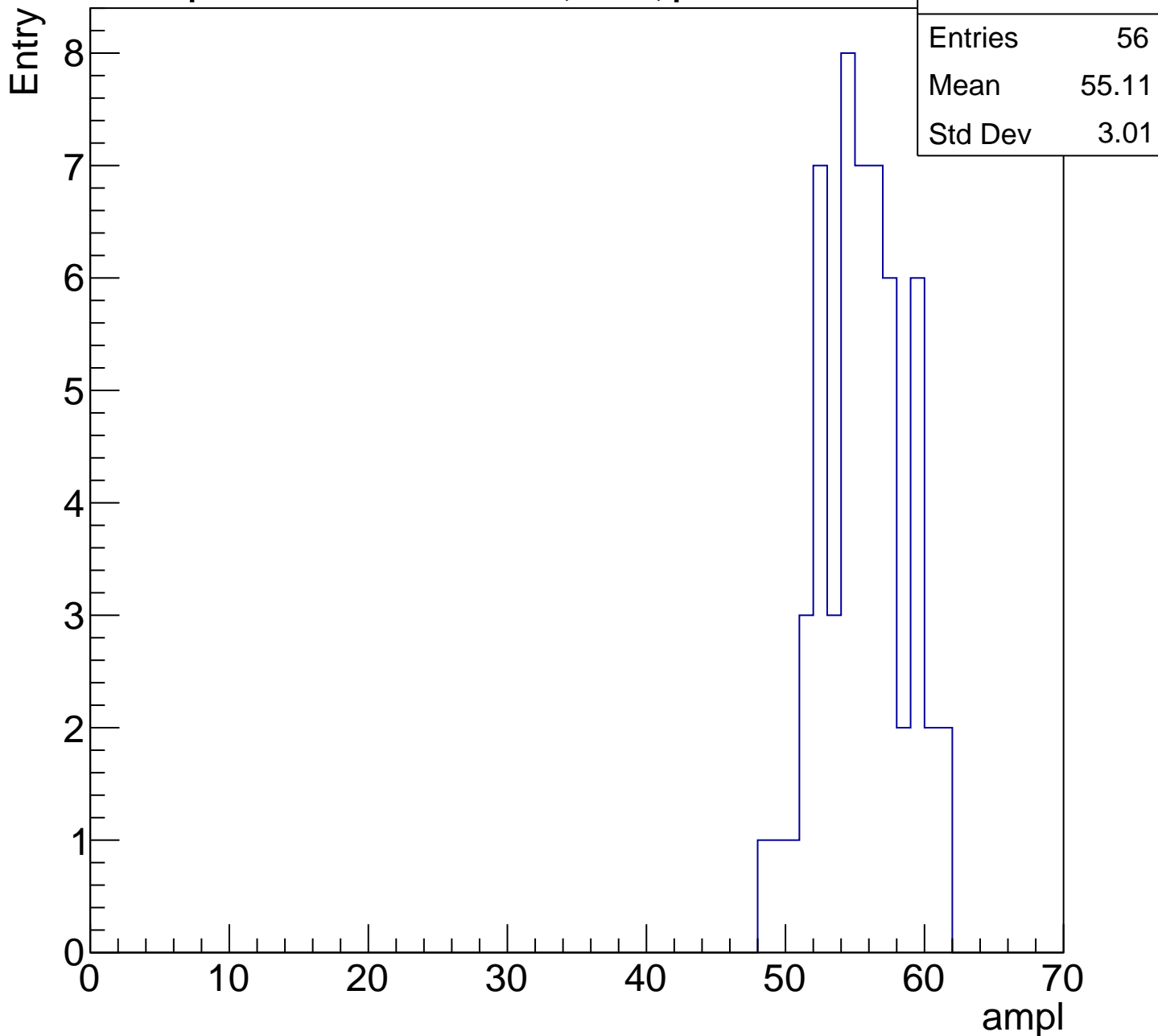
# B1L101S, U9-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

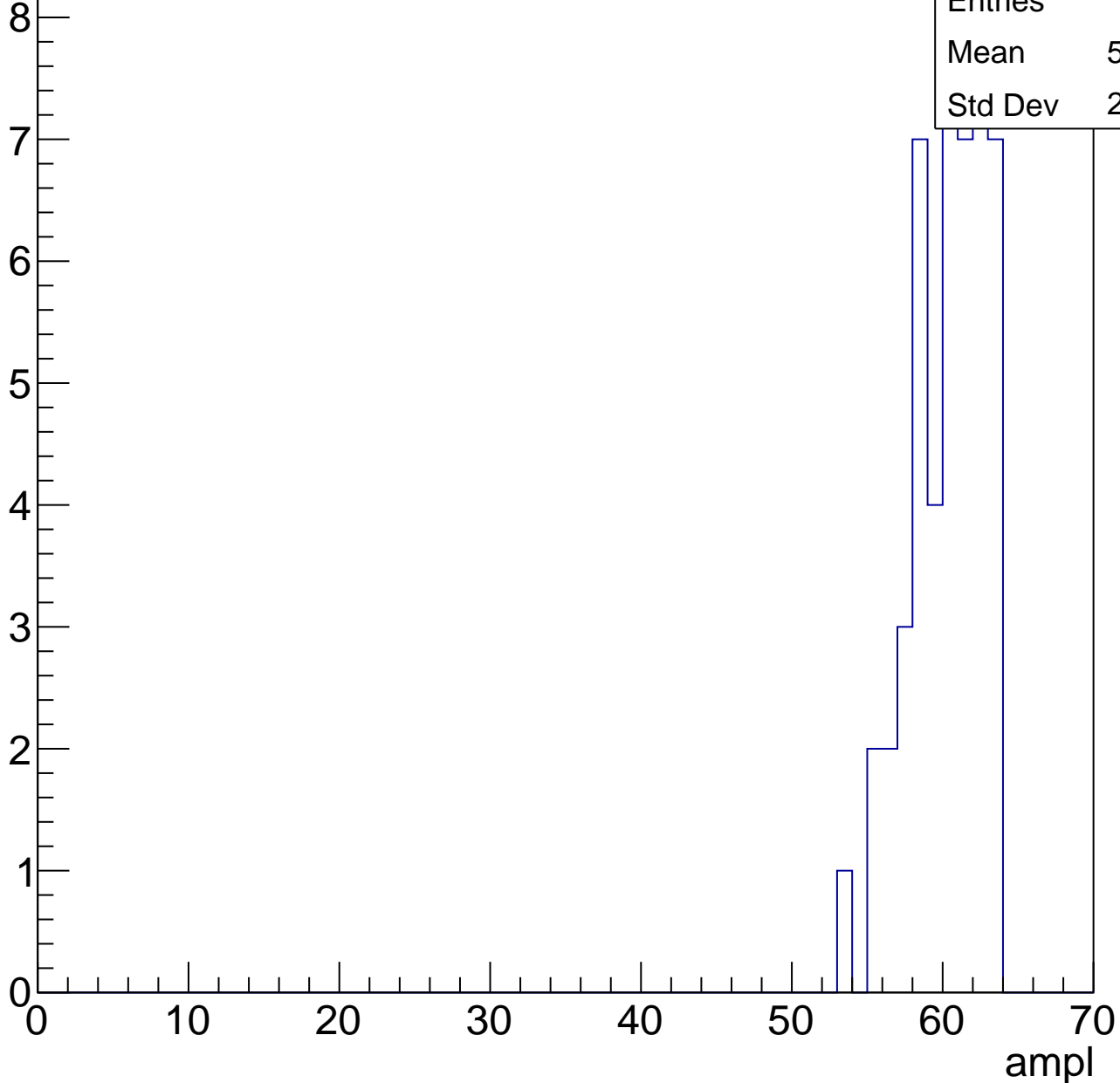


# B1L101S, U9-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

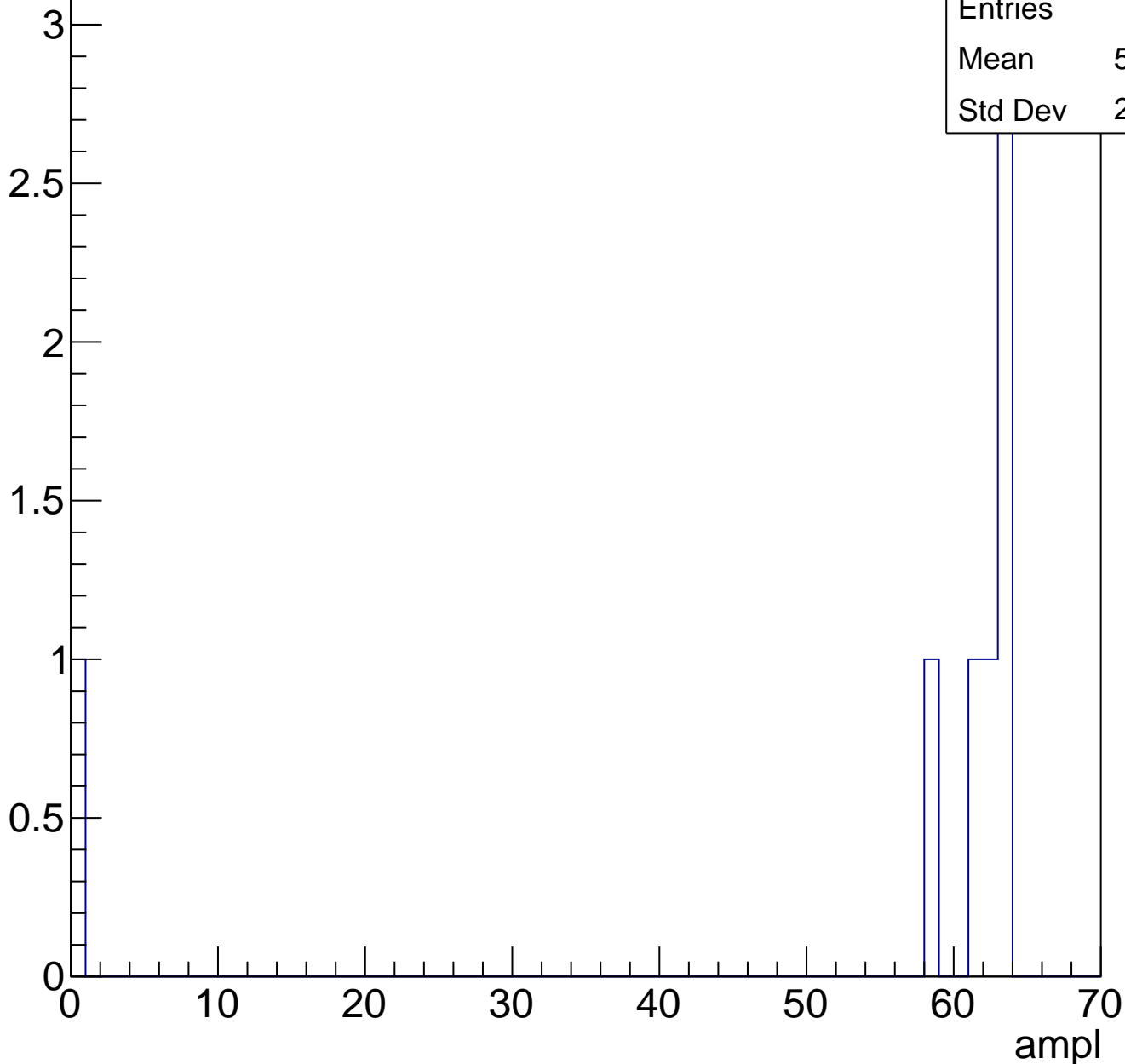
Entries	49
Mean	59.84
Std Dev	2.436



# B1L101S, U9-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch47, adc0

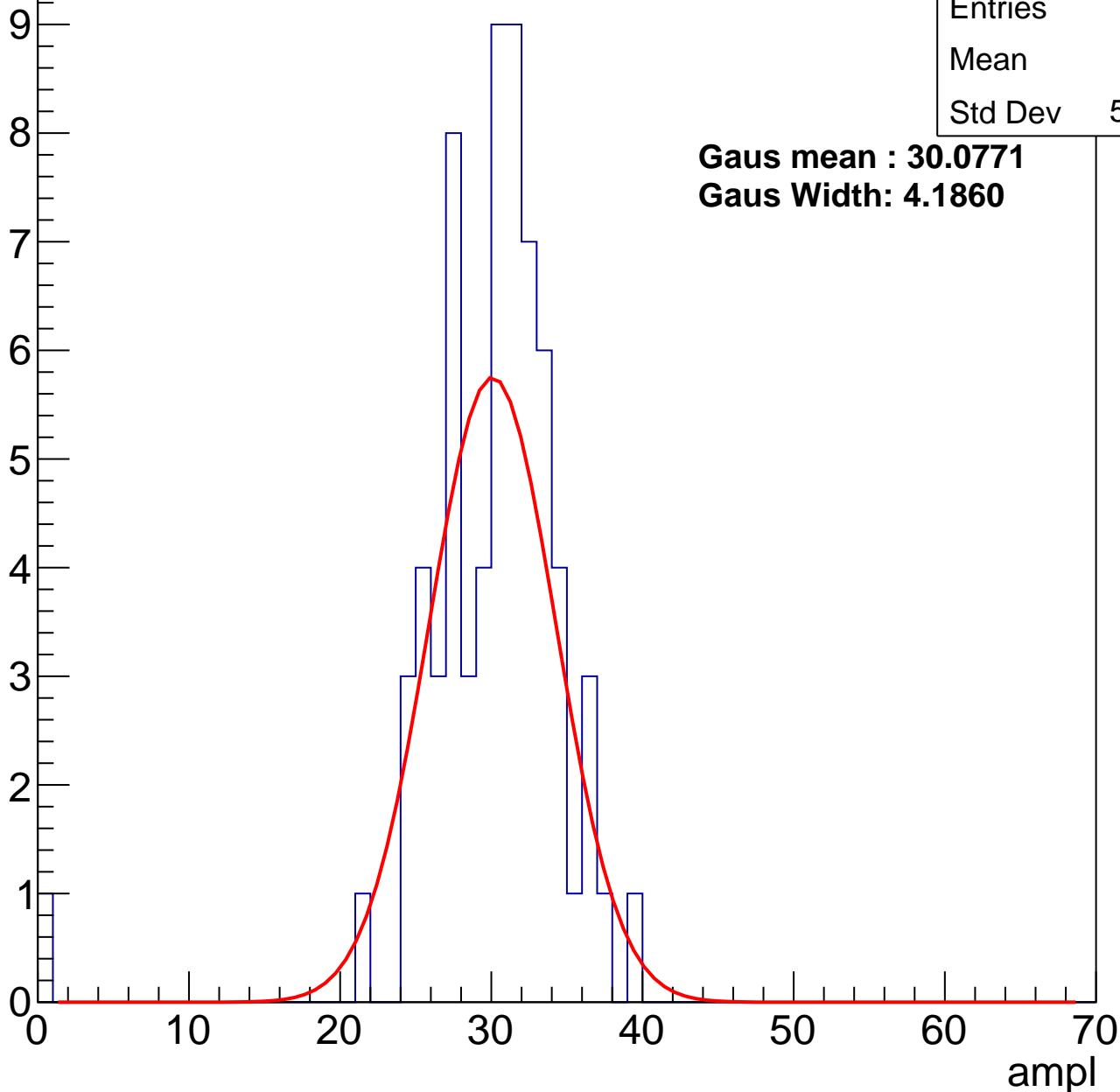
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	29.6
Std Dev	5.047

**Gaus mean : 30.0771**

**Gaus Width: 4.1860**



# B1L101S, U9-ch47, adc1

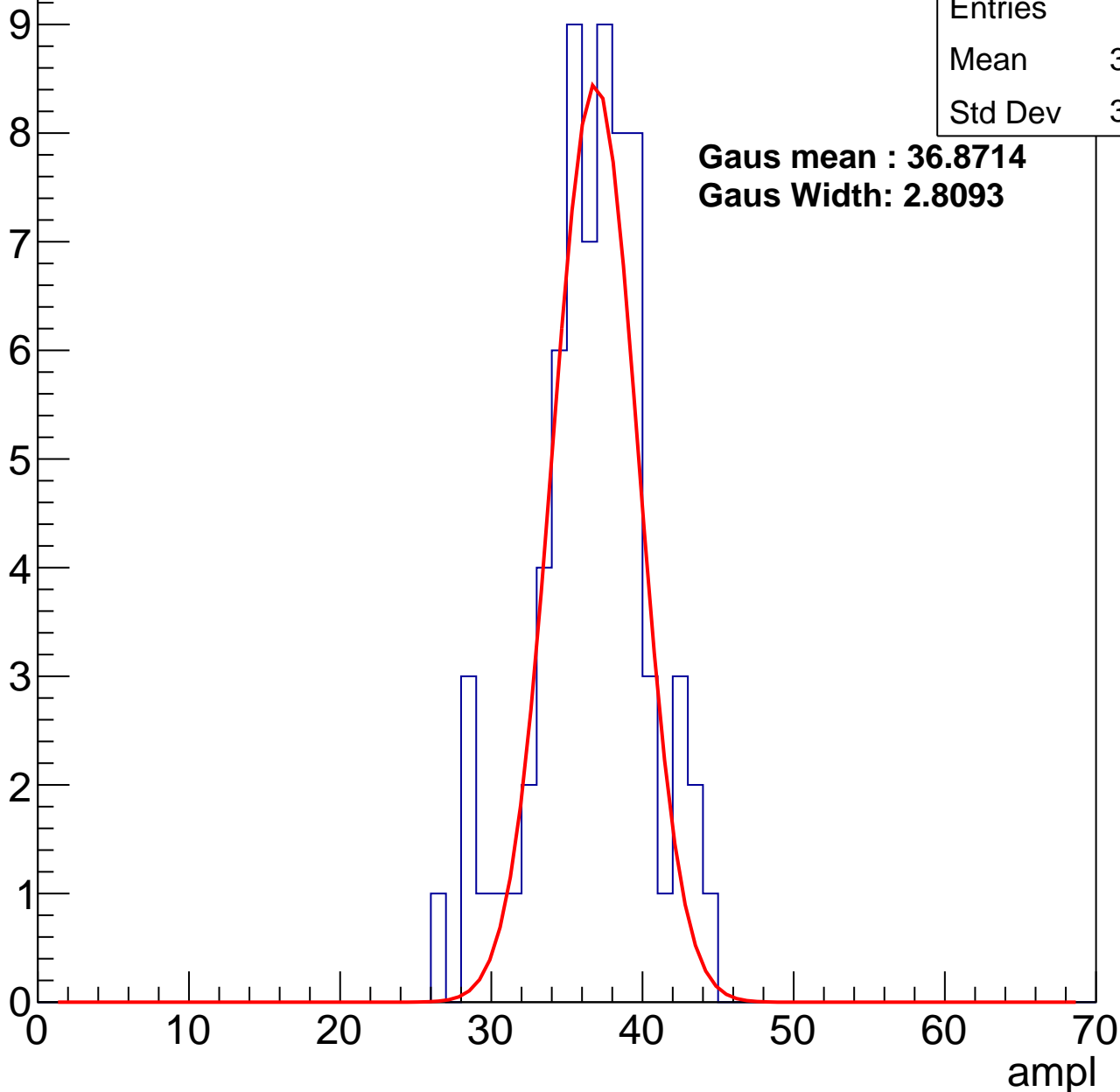
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	36.19
Std Dev	3.697

**Gaus mean : 36.8714**

**Gaus Width: 2.8093**



# B1L101S, U9-ch47, adc2

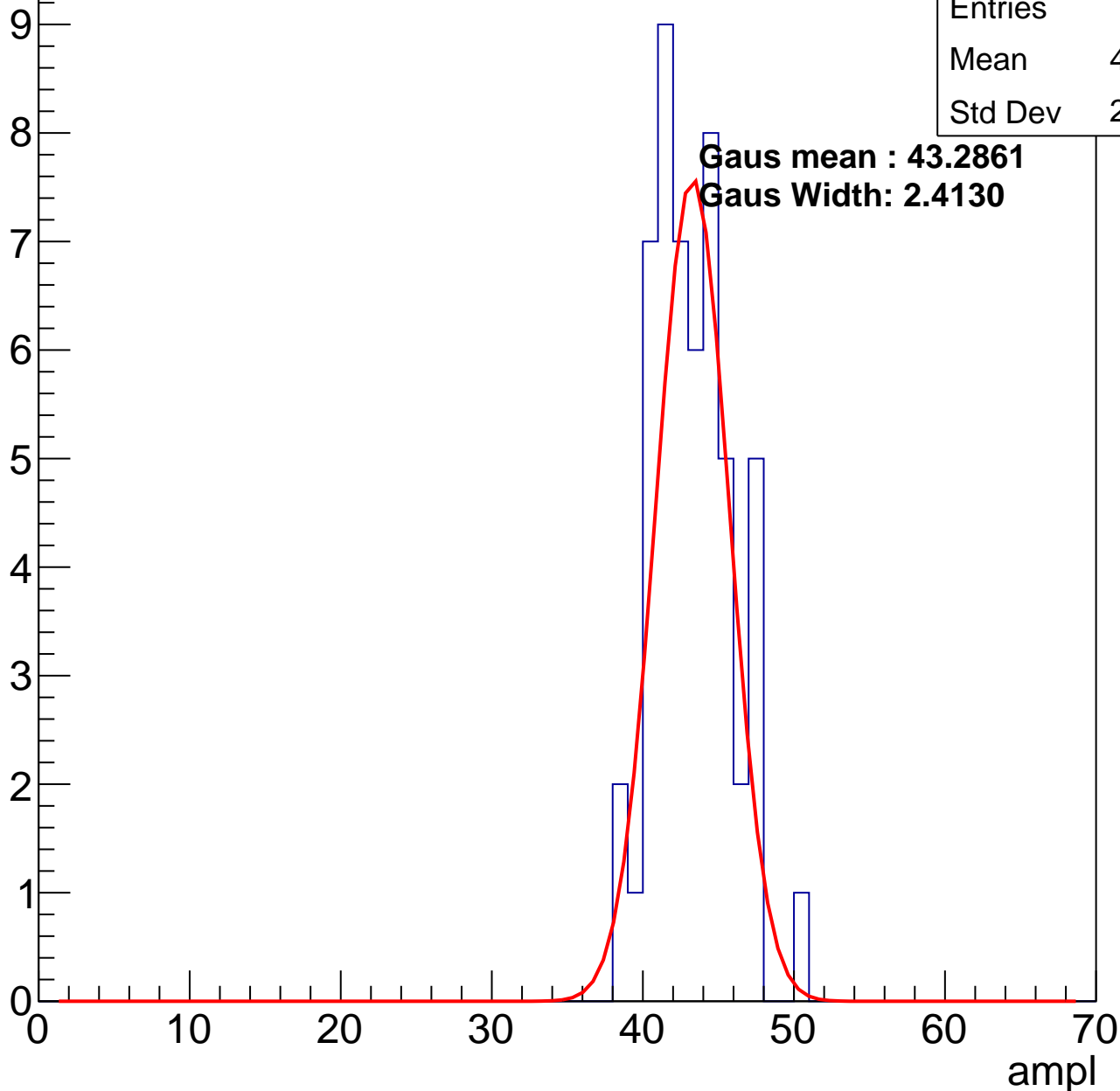
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	42.83
Std Dev	2.553

**Gaus mean : 43.2861**

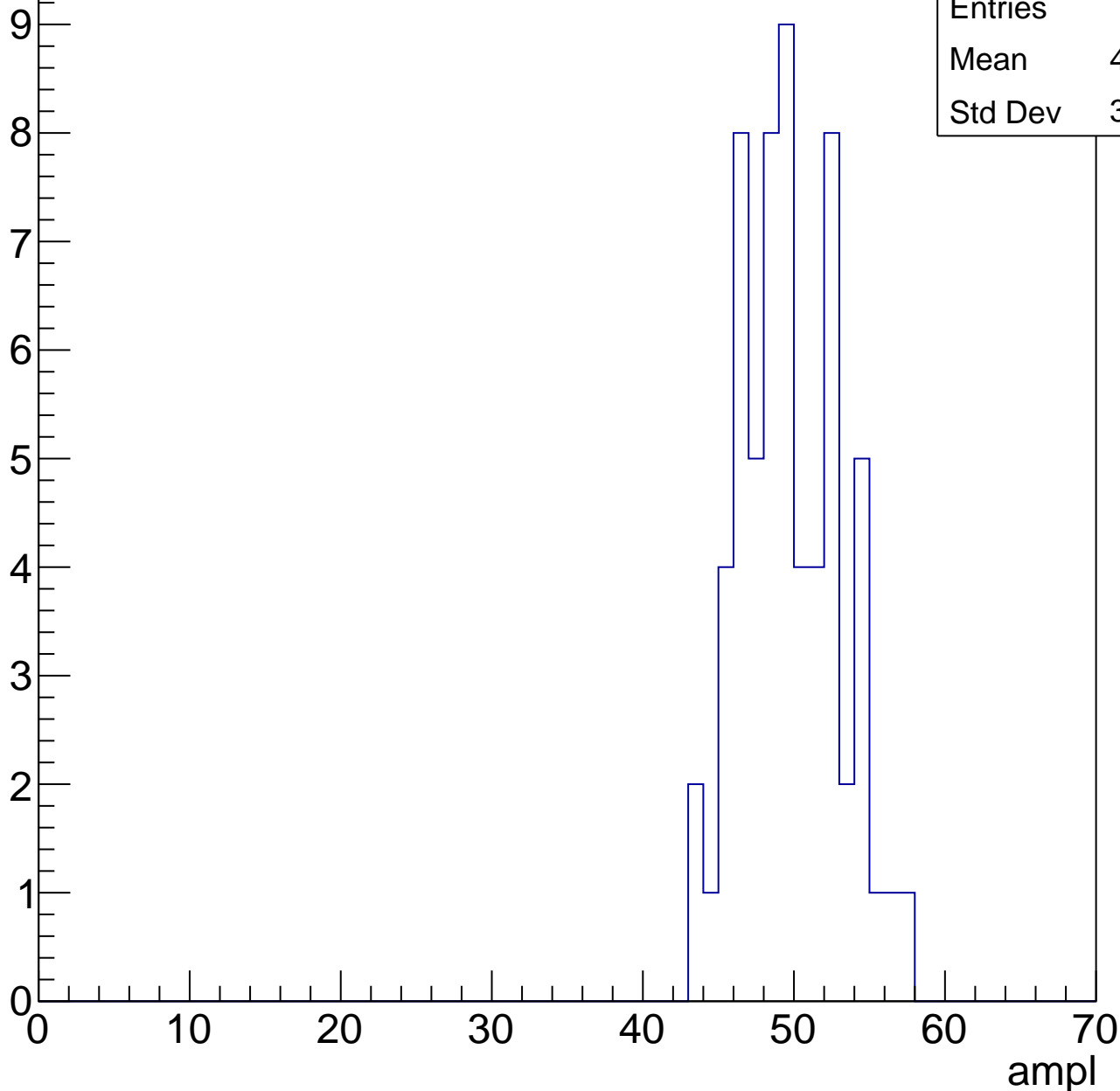
**Gaus Width: 2.4130**



# B1L101S, U9-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

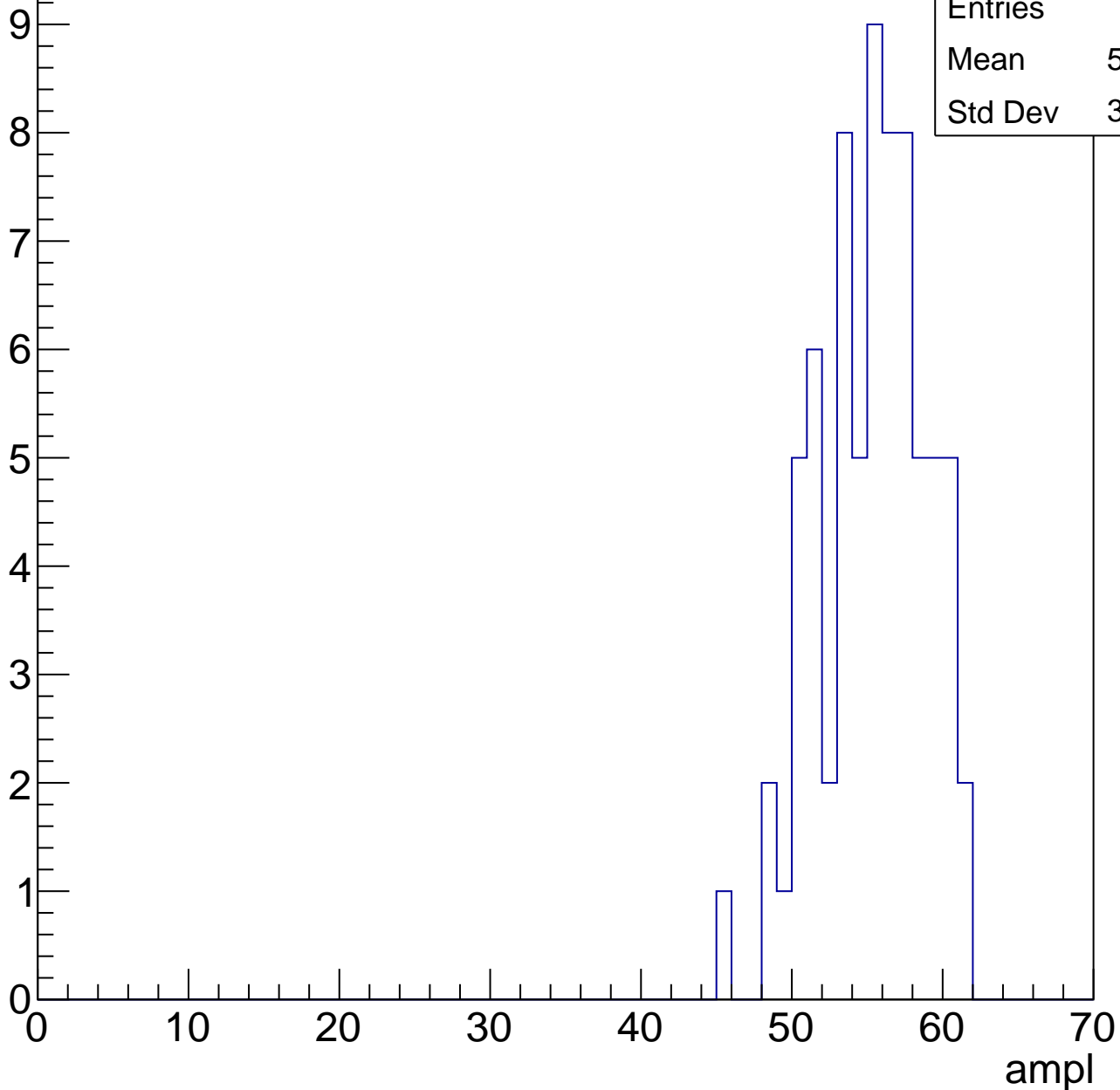


Entries	63
Mean	49.24
Std Dev	3.225

# B1L101S, U9-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	40
Mean	60.62
Std Dev	1.906

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

7

8

# B1L101S, U9-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

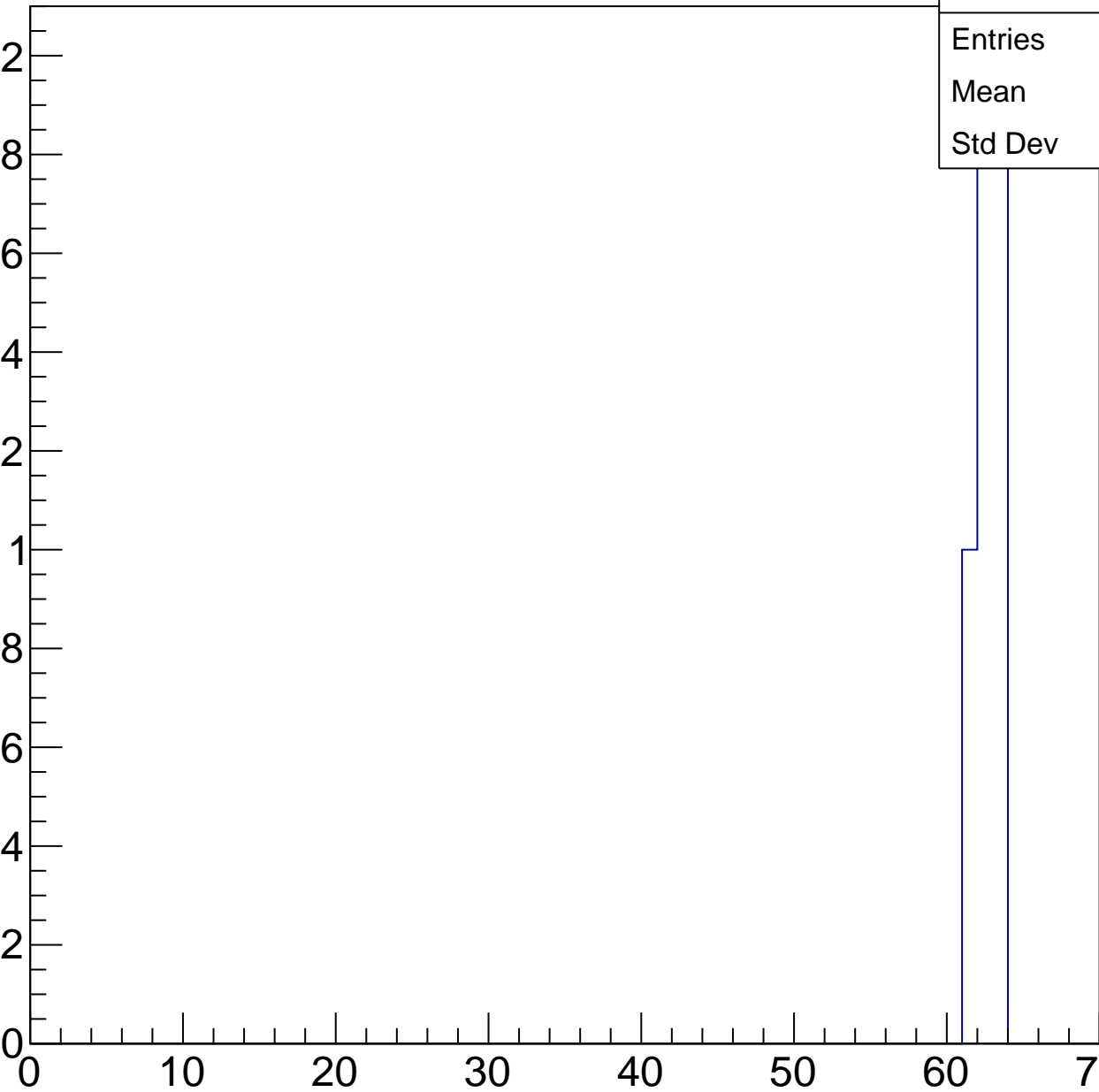
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	62.2
Std Dev	0.7483

0 10 20 30 40 50 60 70

ampl





# B1L101S, U9-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch48, adc0

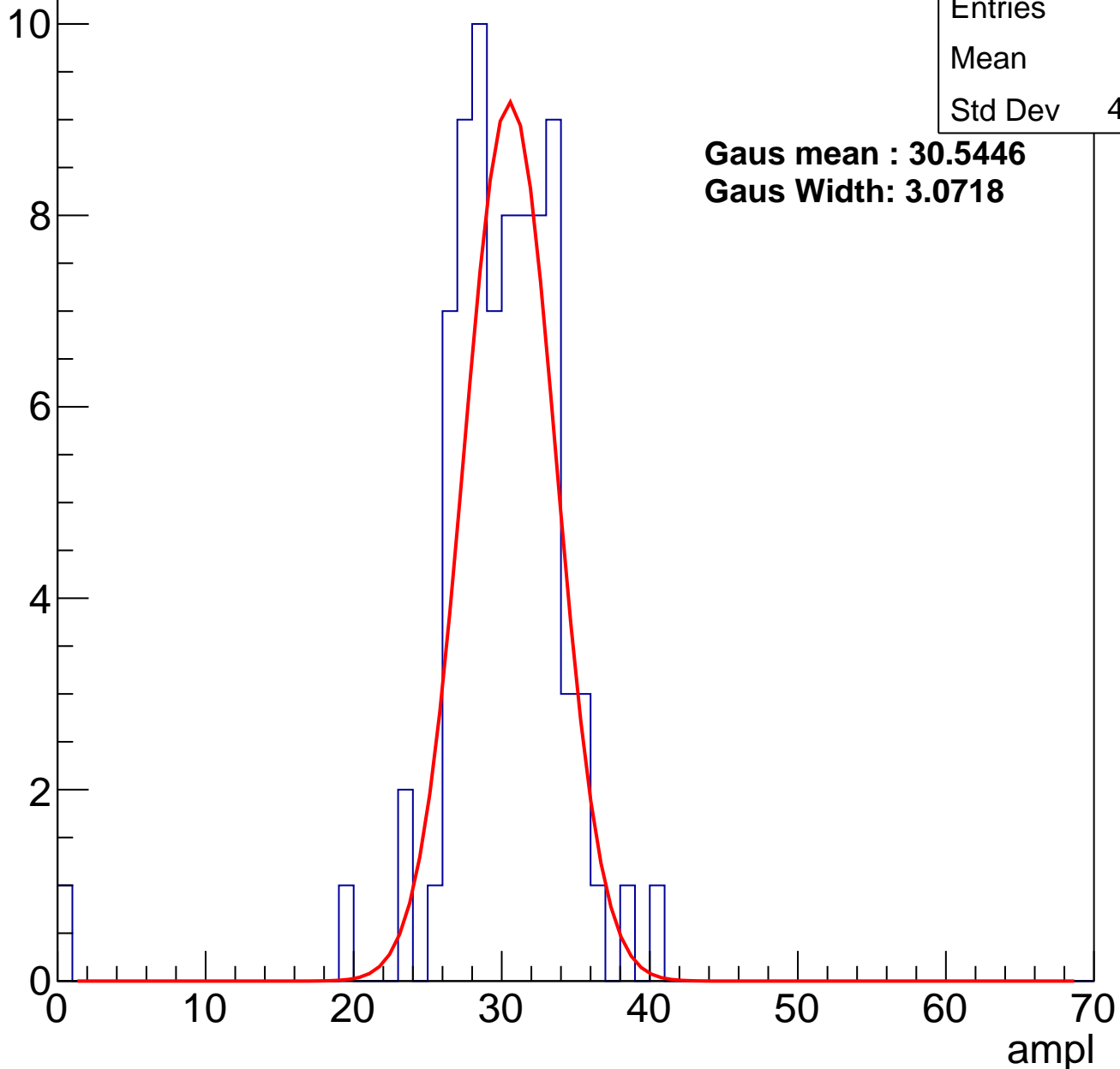
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	80
Mean	29.5
Std Dev	4.754

**Gaus mean : 30.5446**

**Gaus Width: 3.0718**

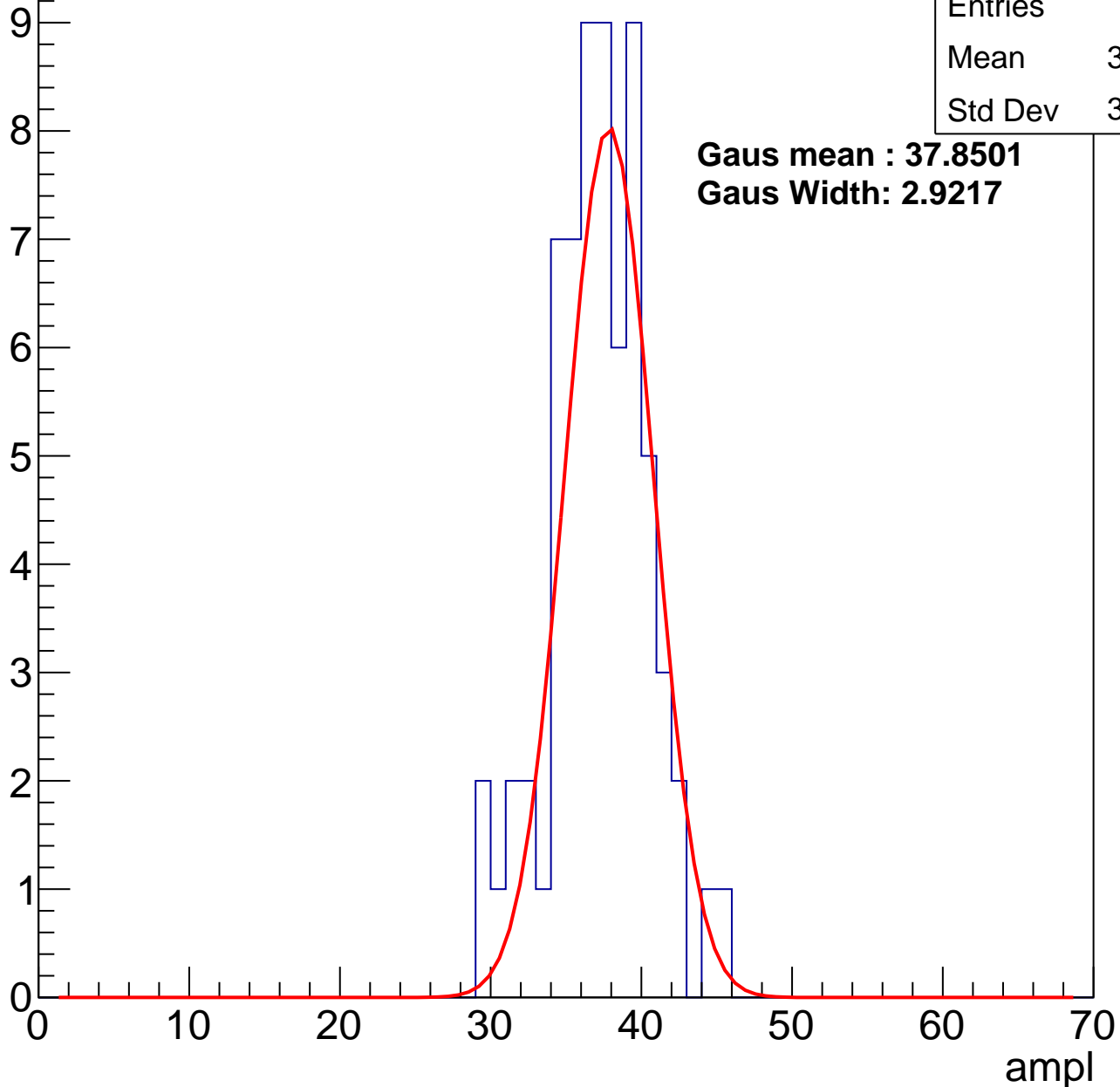
Entry



# B1L101S, U9-ch48, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch48, adc2

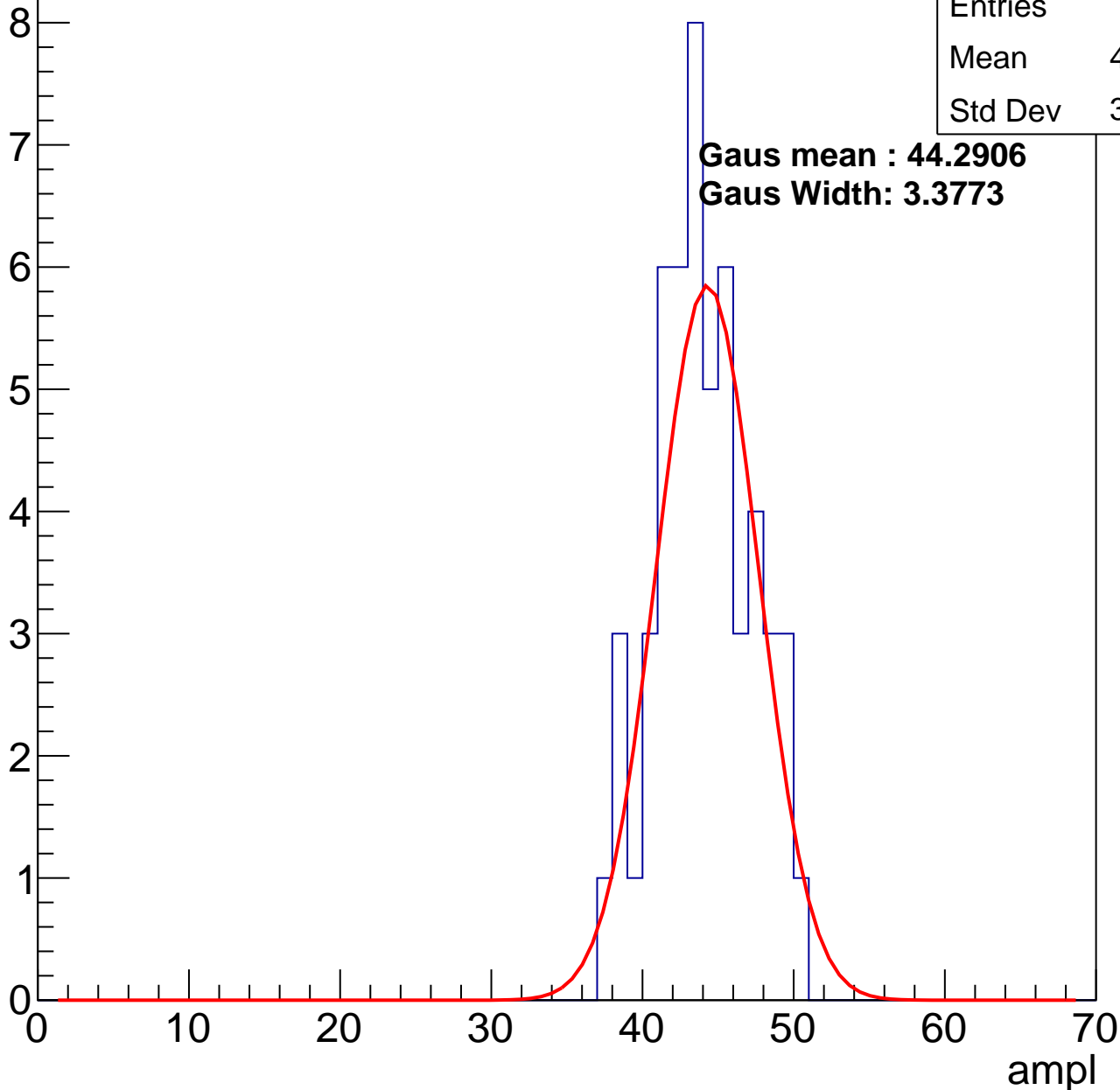
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	43.57
Std Dev	3.129

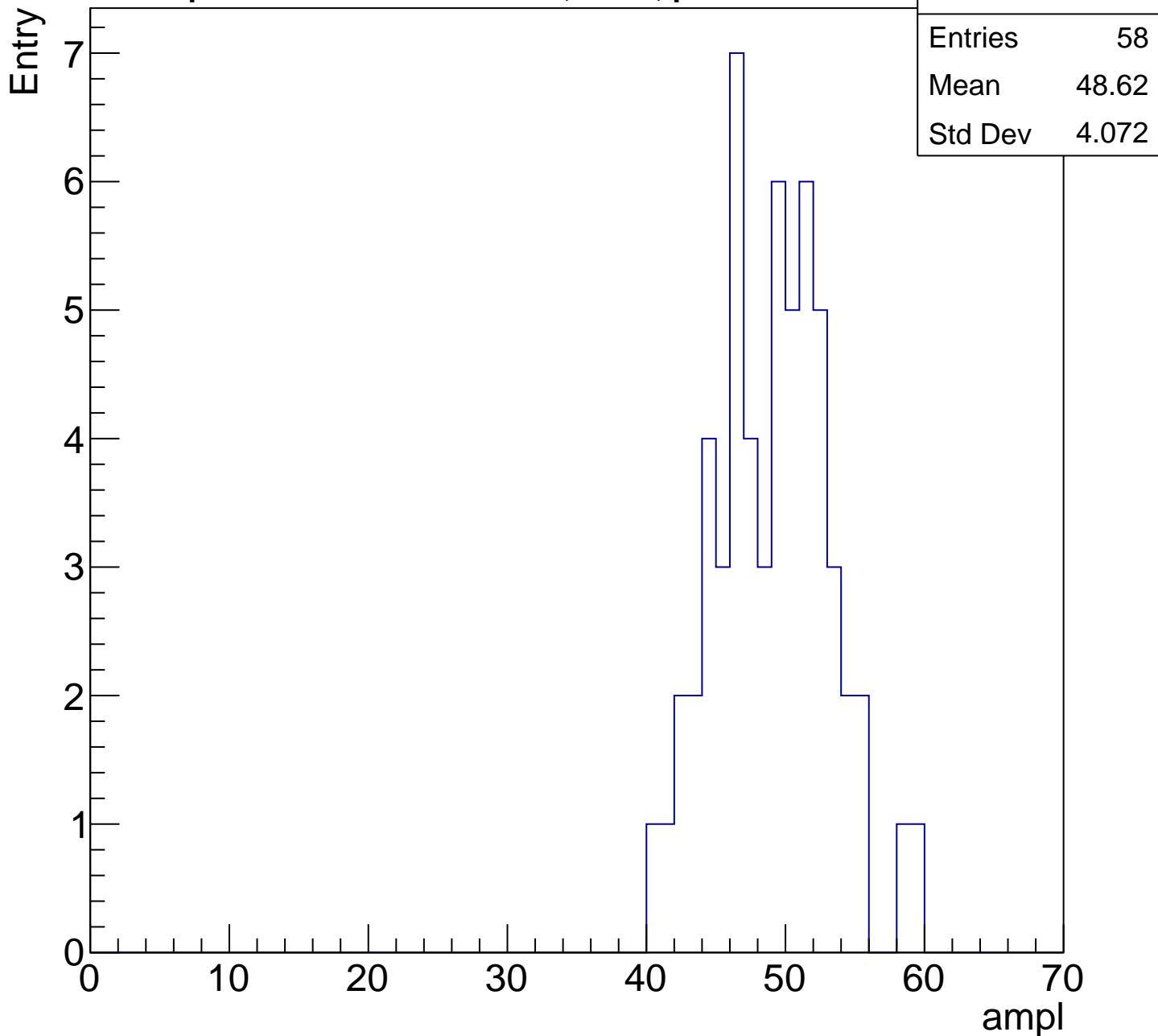
**Gaus mean : 44.2906**

**Gaus Width: 3.3773**



# B1L101S, U9-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

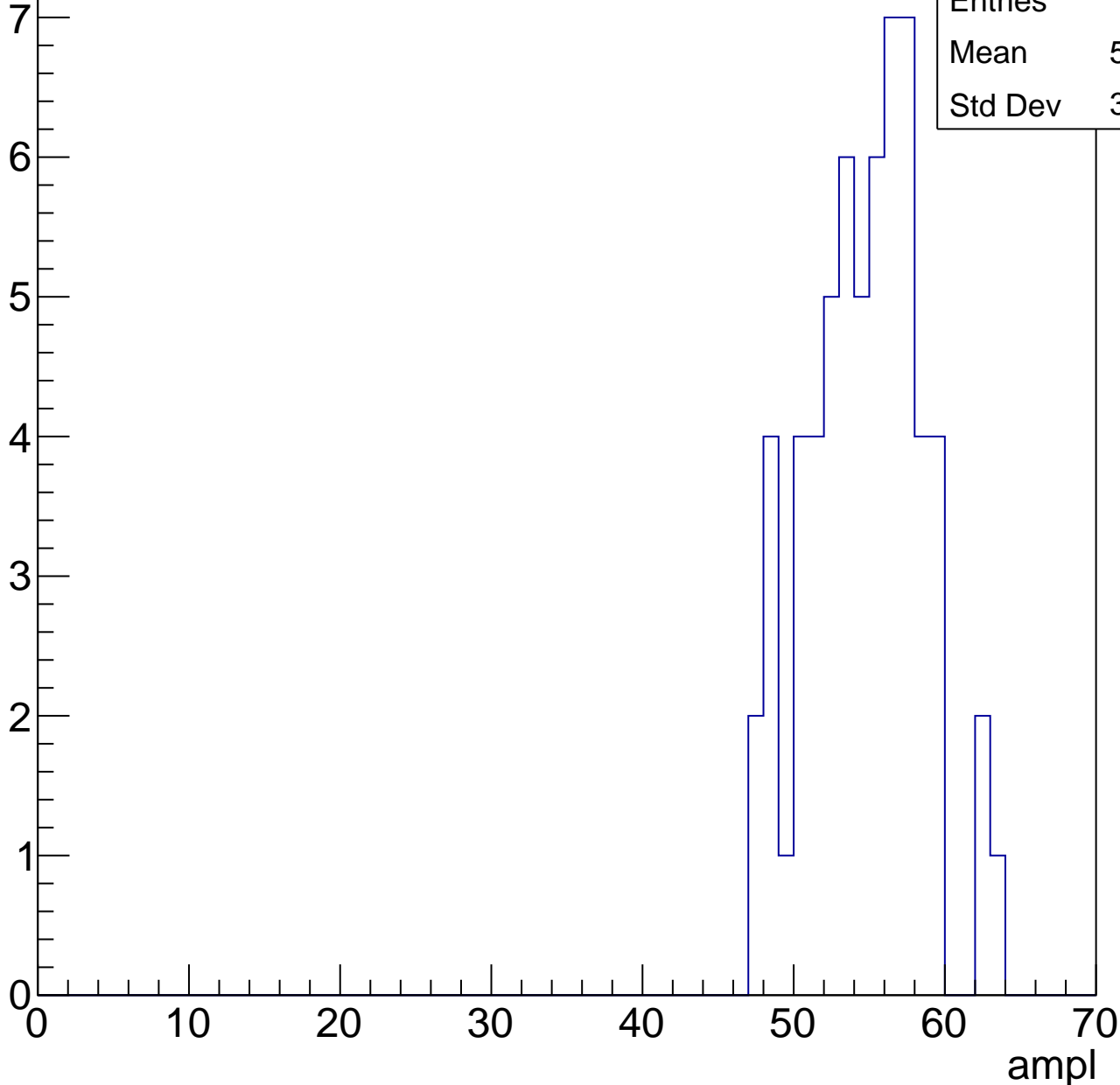


# B1L101S, U9-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

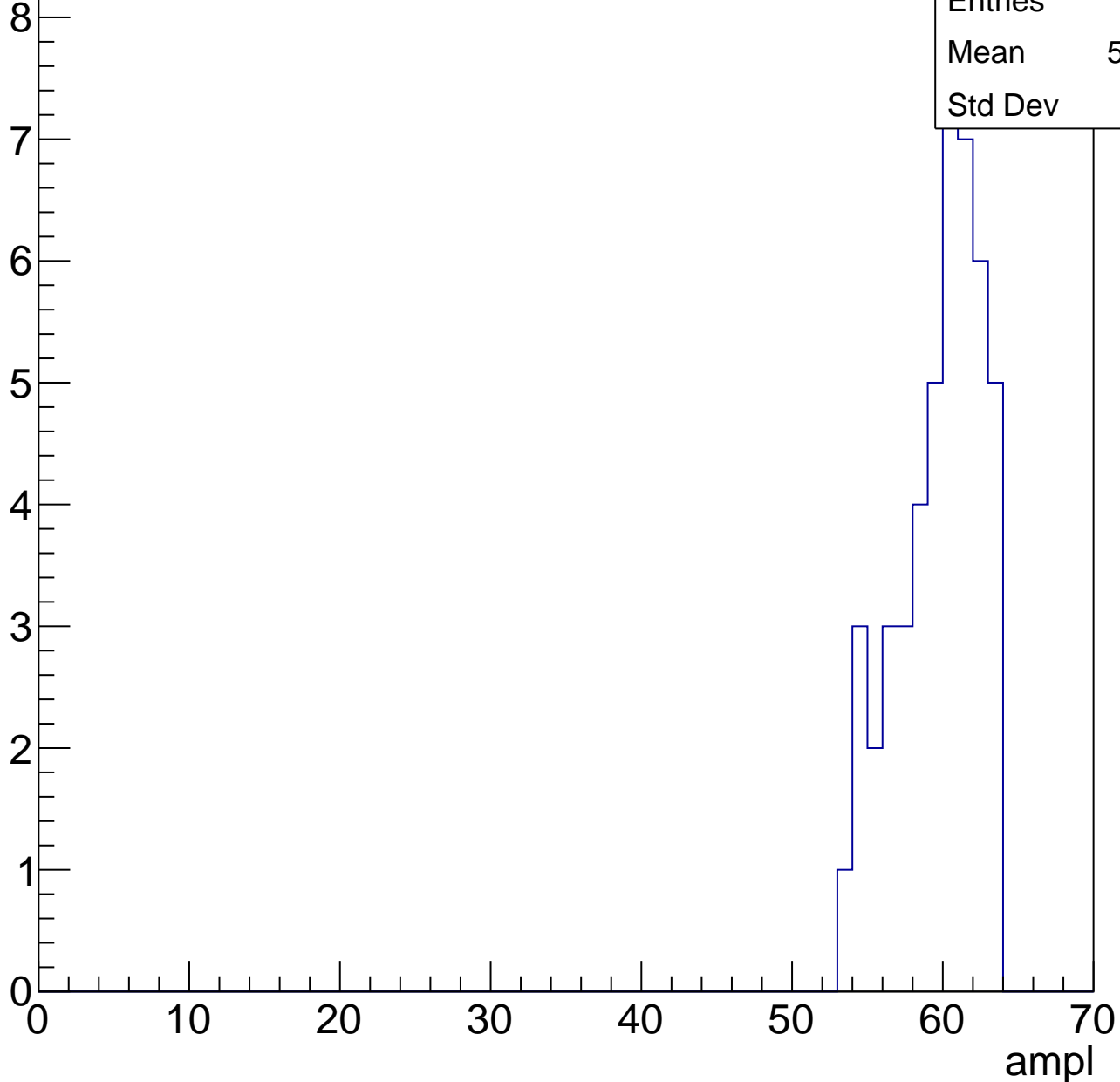
Entries	62
Mean	54.24
Std Dev	3.723



# B1L101S, U9-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

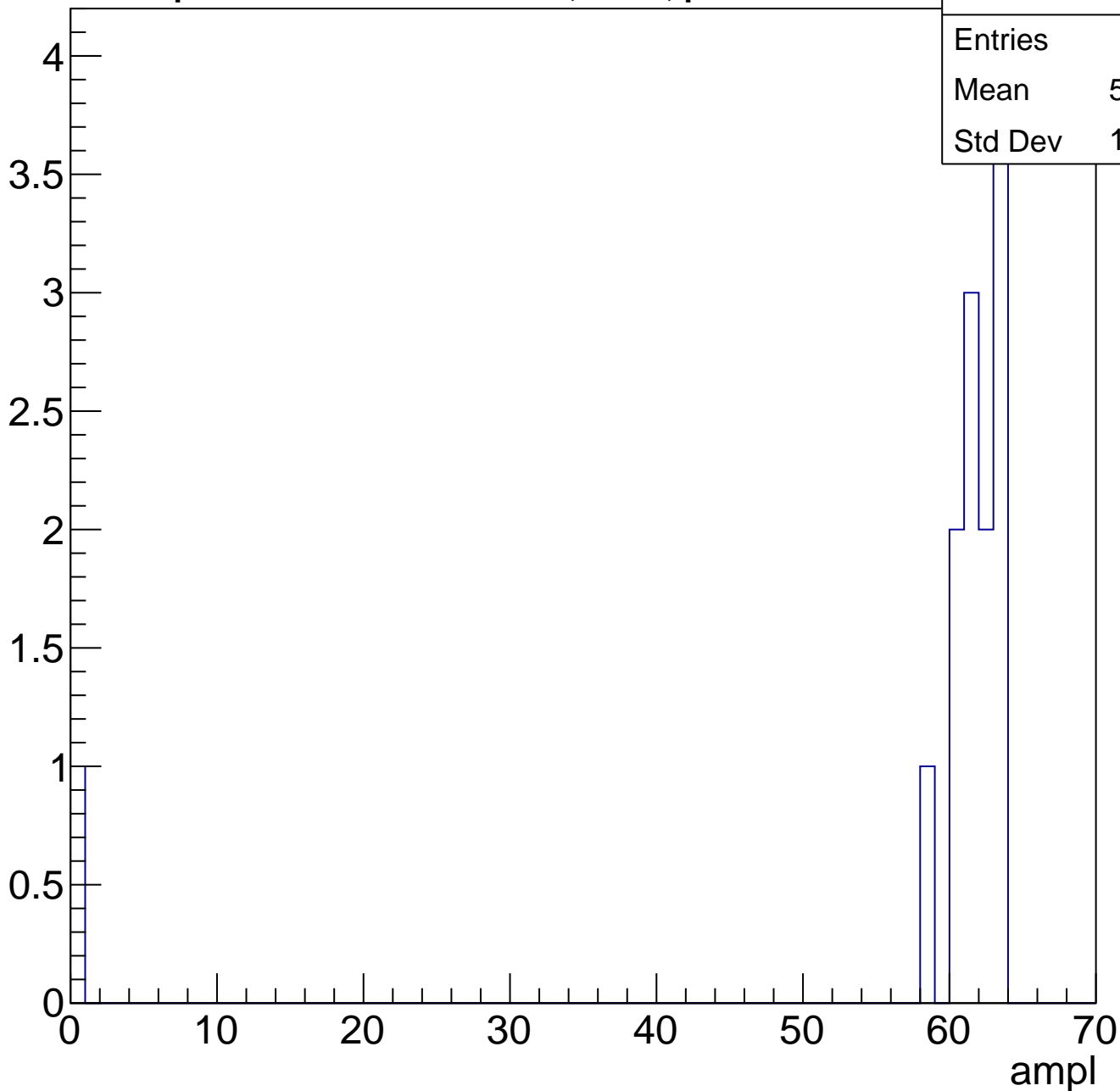
Entry



# B1L101S, U9-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U9-ch49, adc0

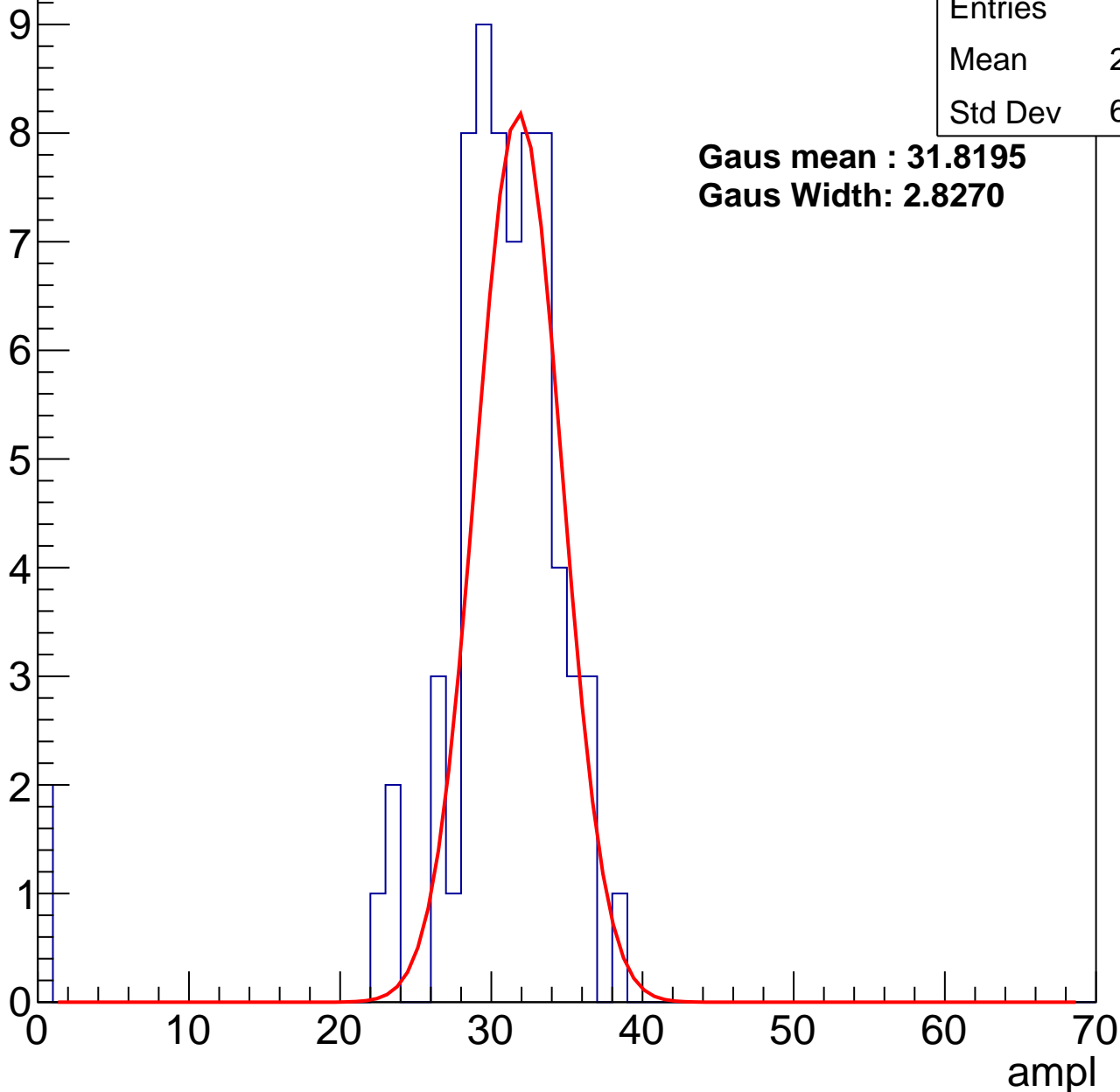
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	29.74
Std Dev	6.036

**Gaus mean : 31.8195**

**Gaus Width: 2.8270**



# B1L101S, U9-ch49, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	79
Mean	37.63
Std Dev	3.053

**Gaus mean : 38.4764**

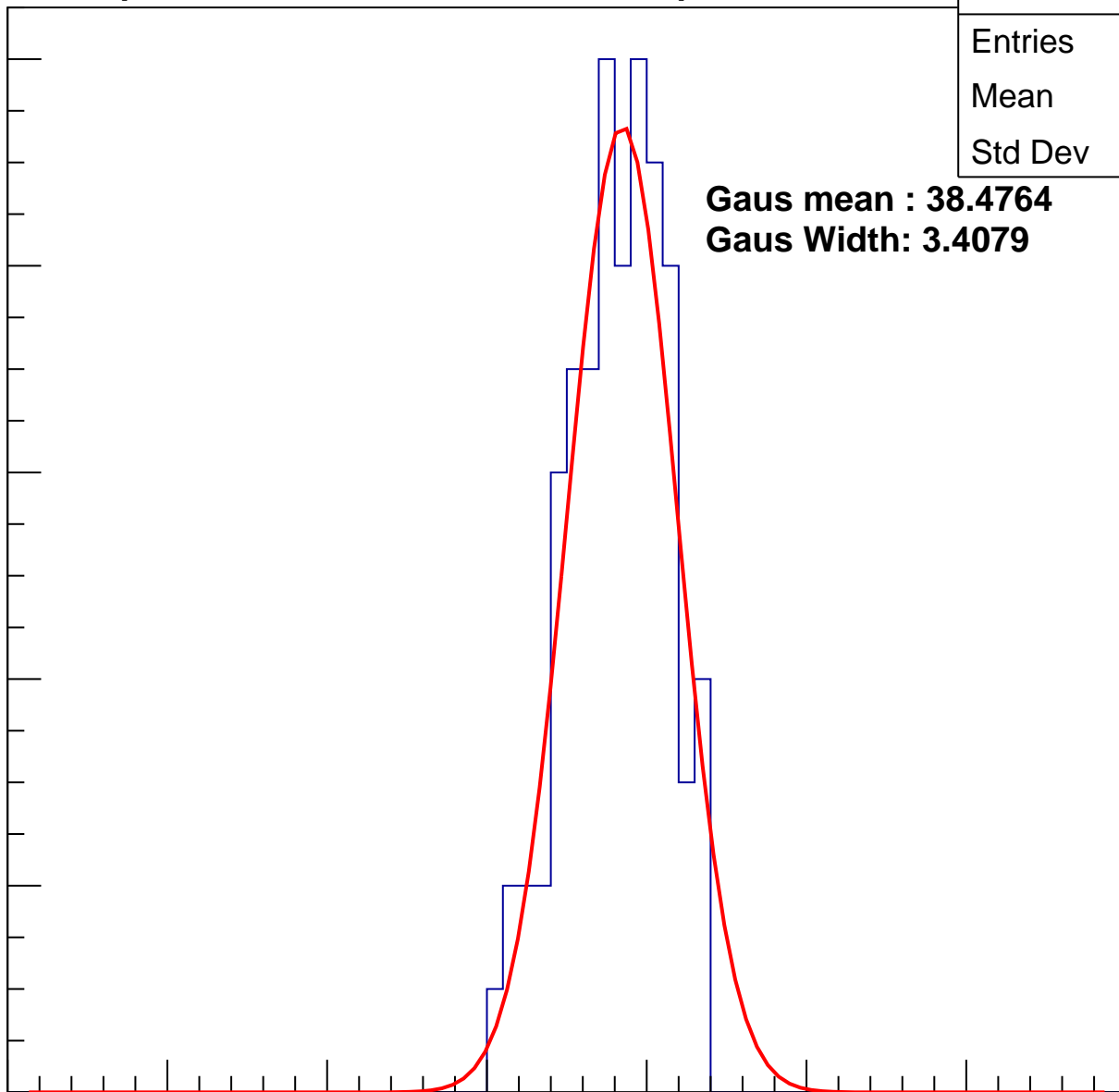
**Gaus Width: 3.4079**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U9-ch49, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	59
Mean	45.14
Std Dev	2.783

**Gaus mean : 45.3125**

**Gaus Width: 2.5050**

Entry

10  
8  
6  
4  
2  
0

ampl

0

10

20

30

40

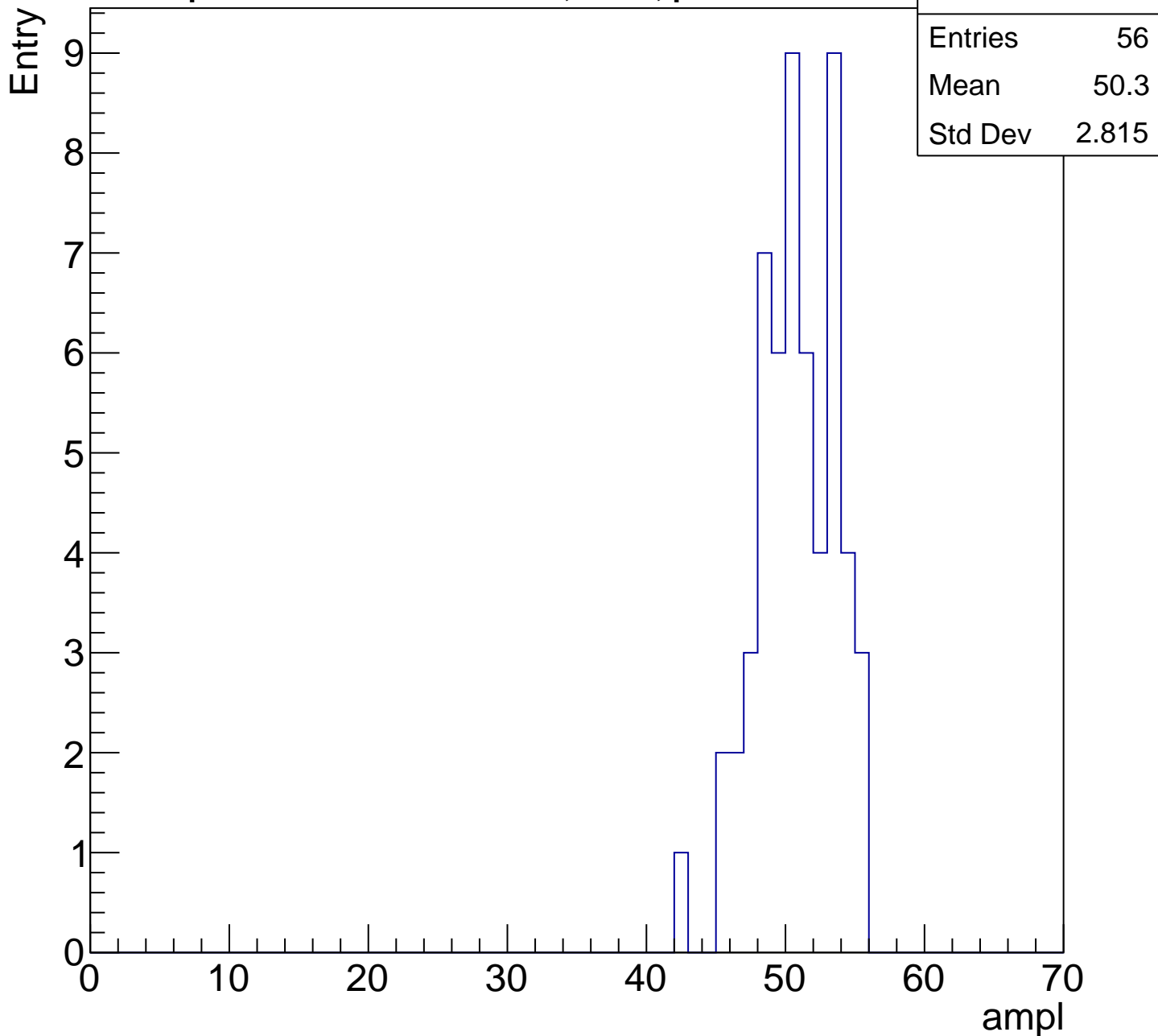
50

60

70

# B1L101S, U9-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch49, adc4

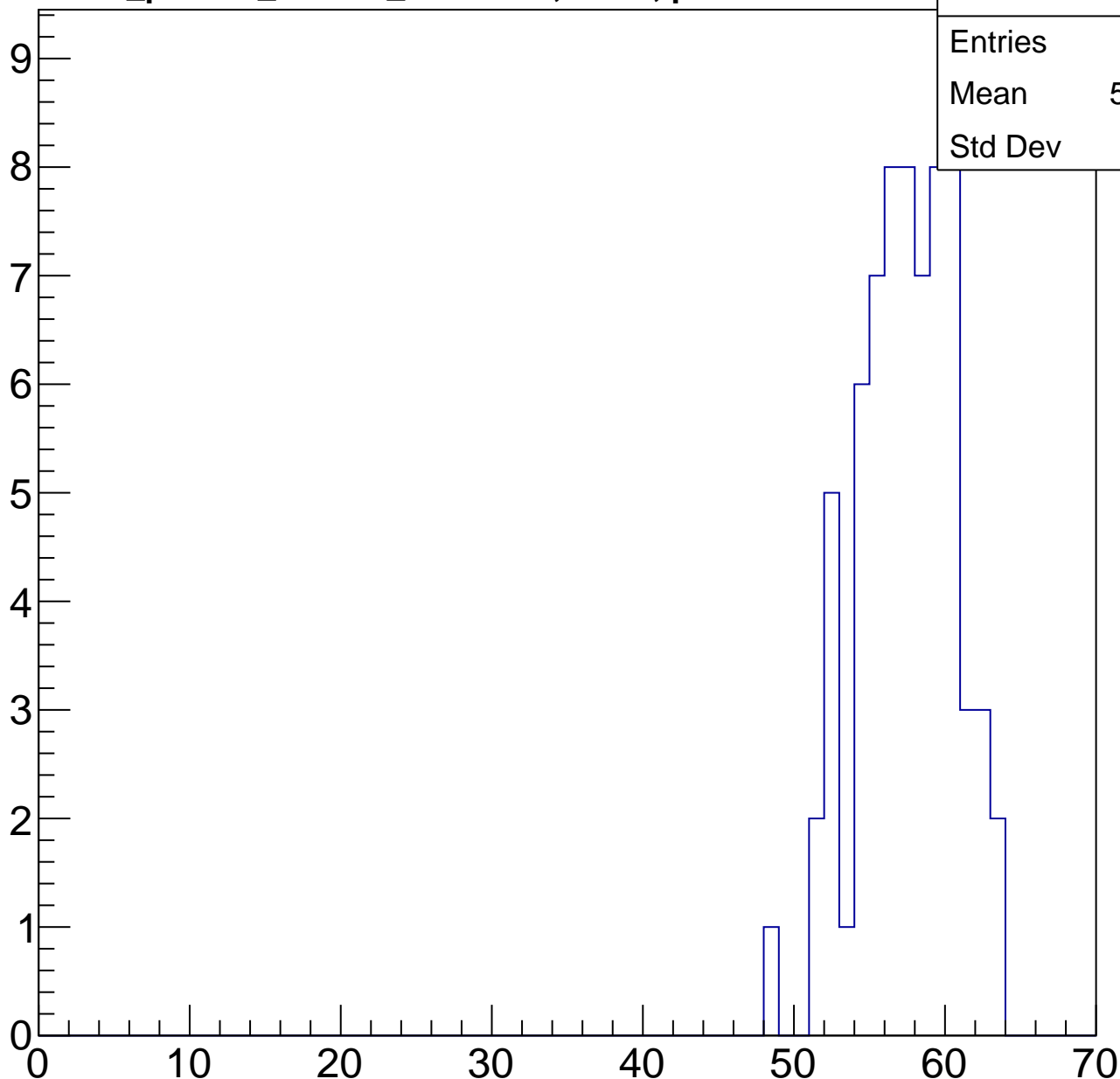
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	70
Mean	56.99
Std Dev	3.16

ampl

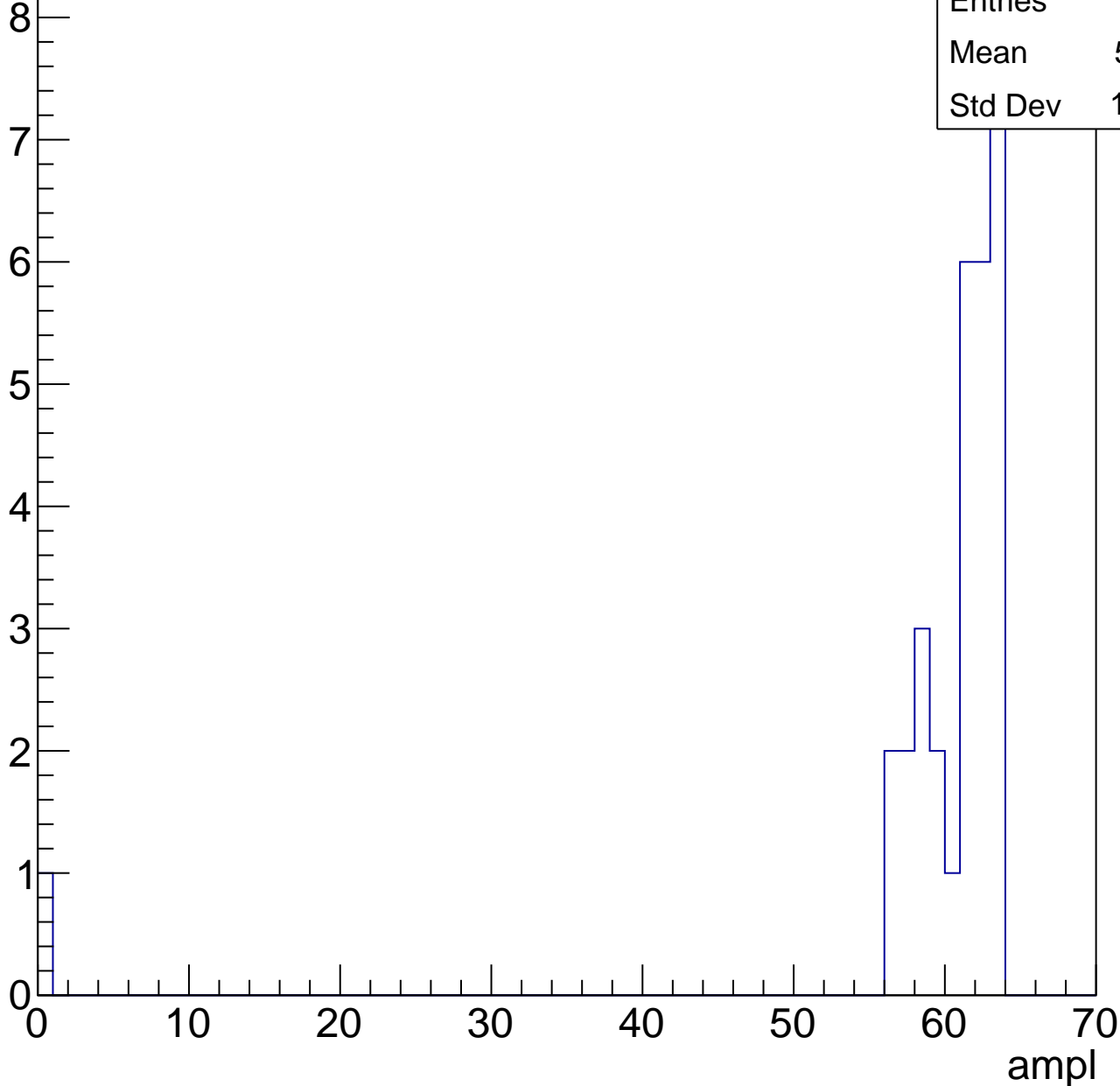


# B1L101S, U9-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	31
Mean	58.71
Std Dev	10.95



# B1L101S, U9-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U9-ch50, adc0

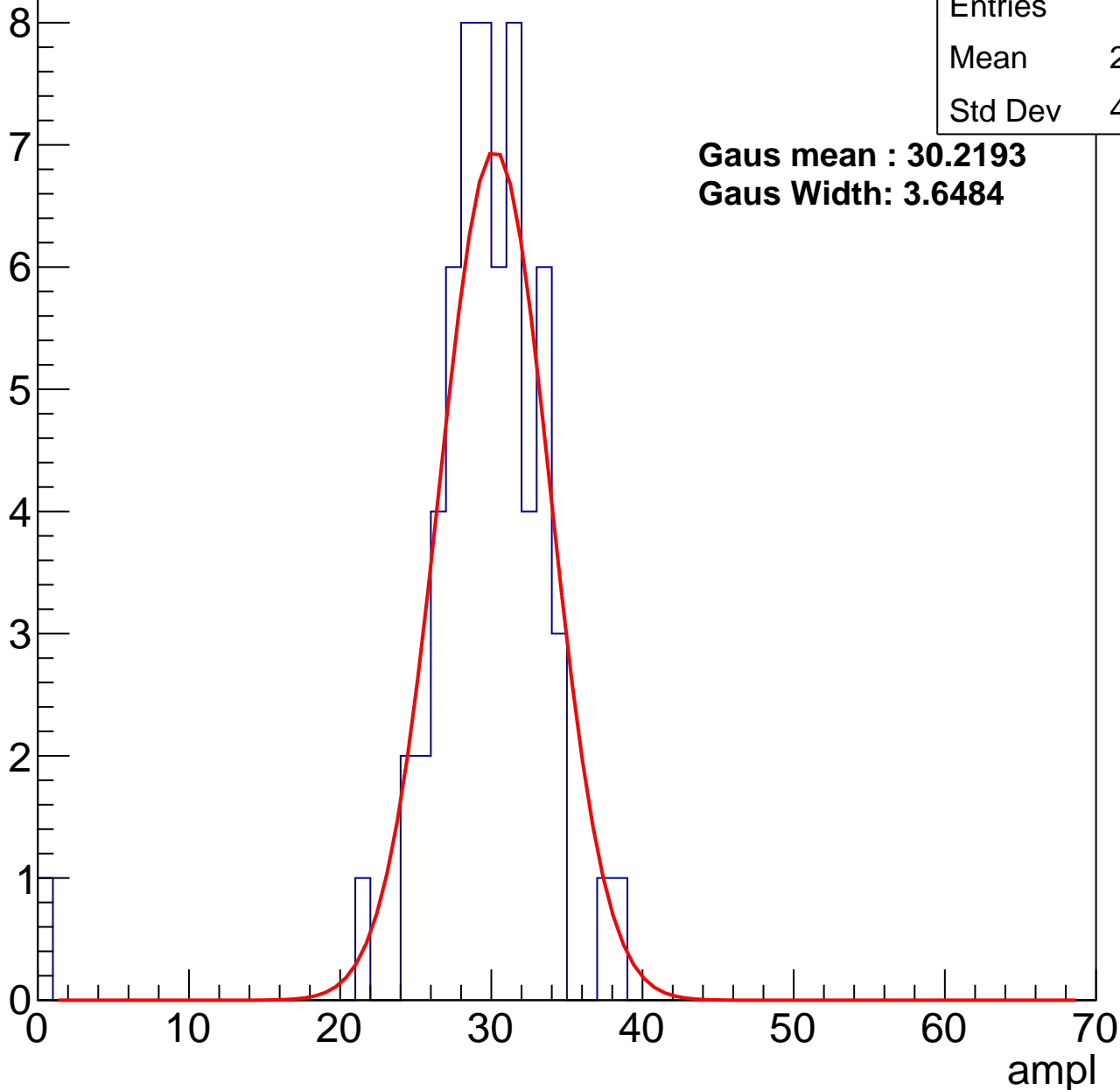
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	29.05
Std Dev	4.867

**Gaus mean : 30.2193**

**Gaus Width: 3.6484**



# B1L101S, U9-ch50, adc1

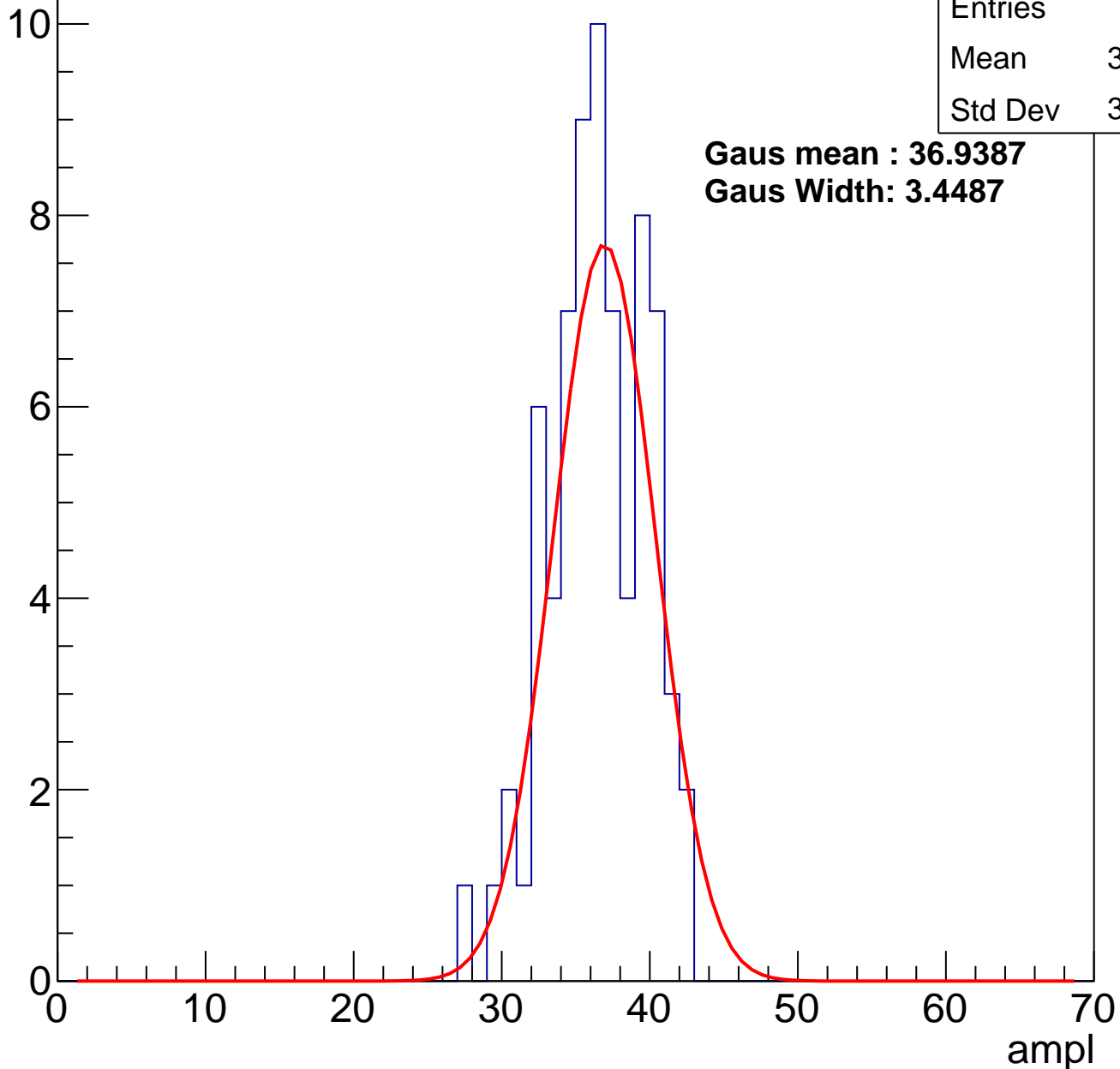
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	72
Mean	36.03
Std Dev	3.227

**Gaus mean : 36.9387**

**Gaus Width: 3.4487**

Entry



# B1L101S, U9-ch50, adc2

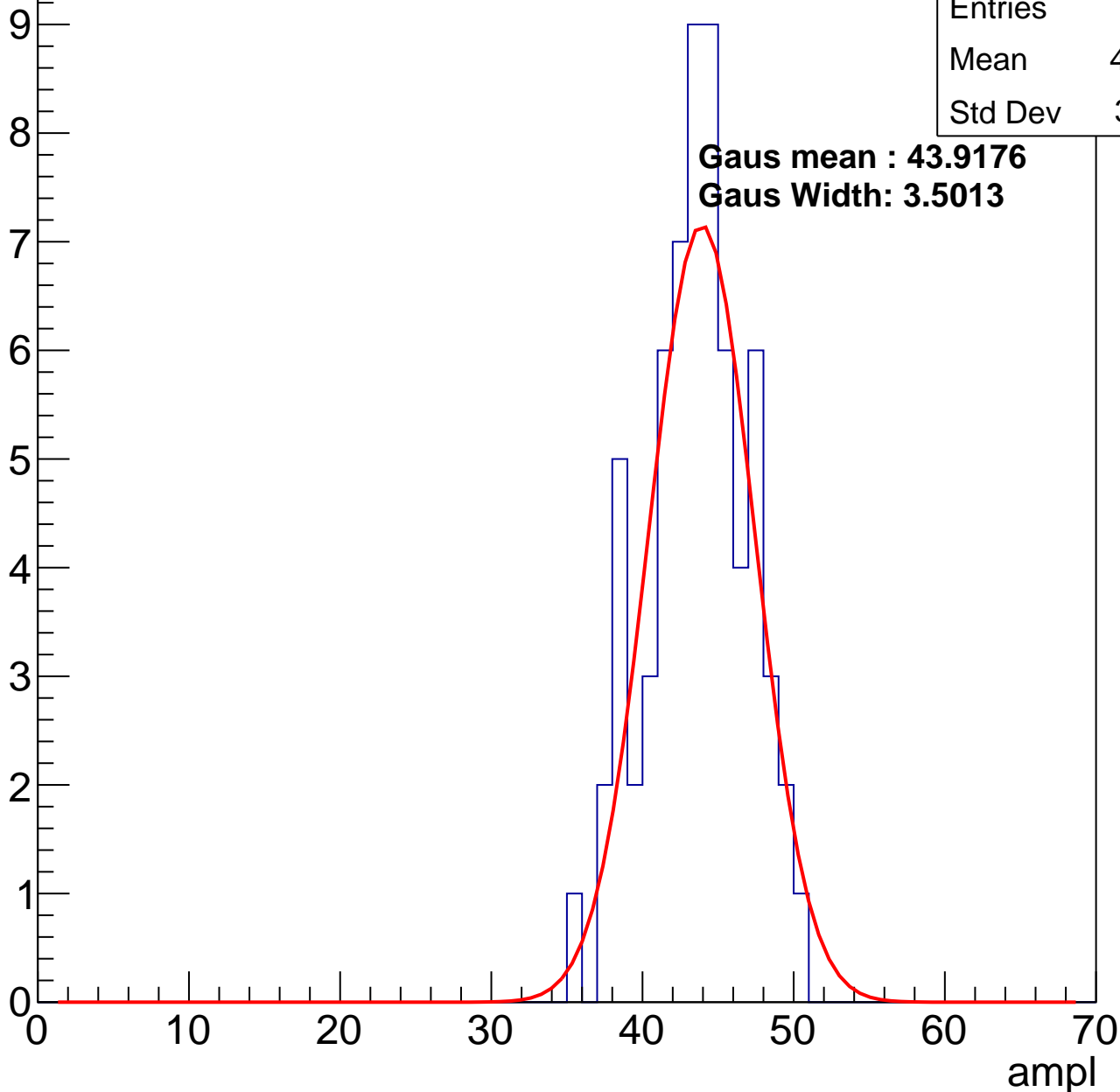
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	43.15
Std Dev	3.281

**Gaus mean : 43.9176**

**Gaus Width: 3.5013**

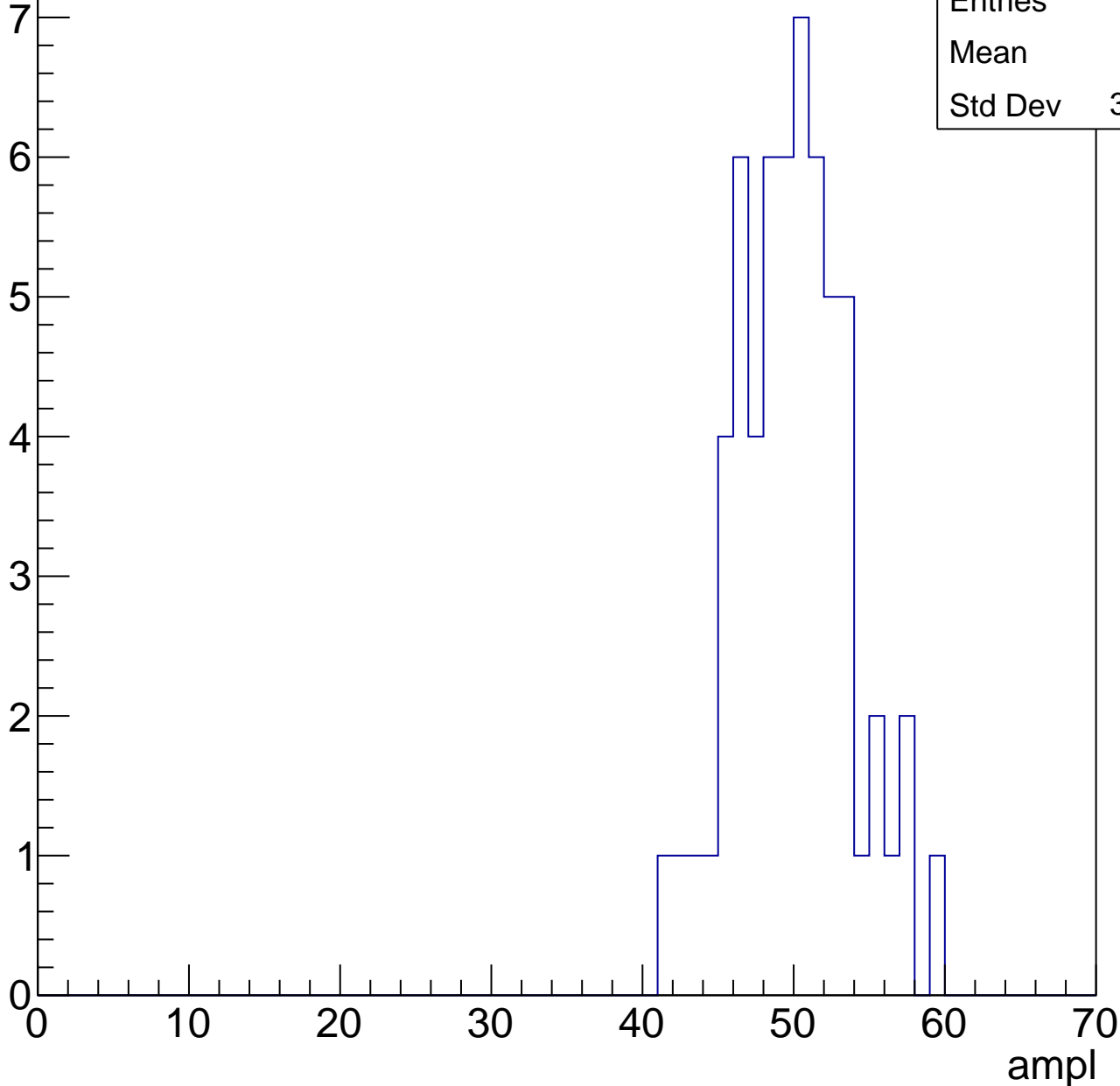


# B1L101S, U9-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

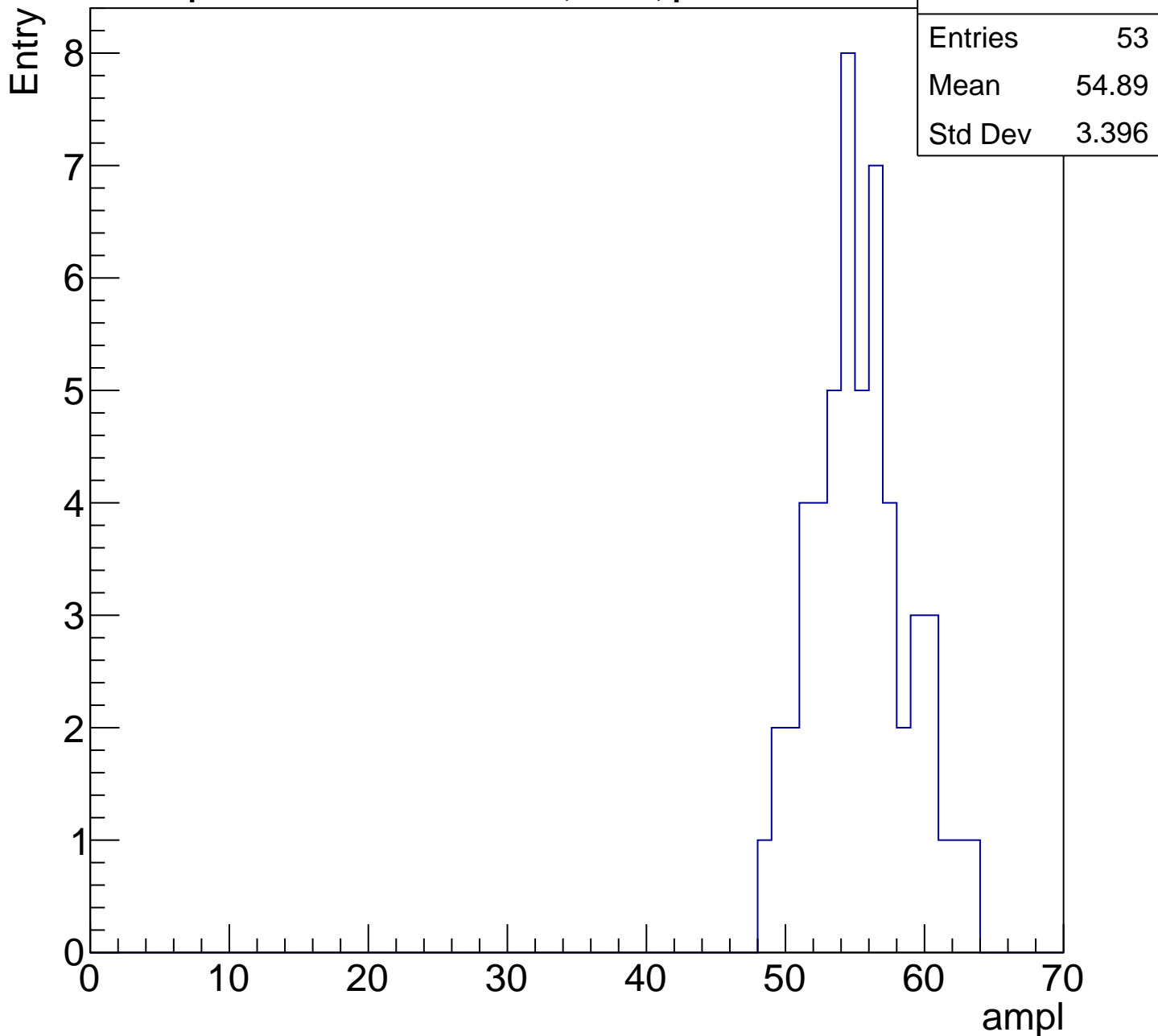
Entry

Entries	60
Mean	49.5
Std Dev	3.717



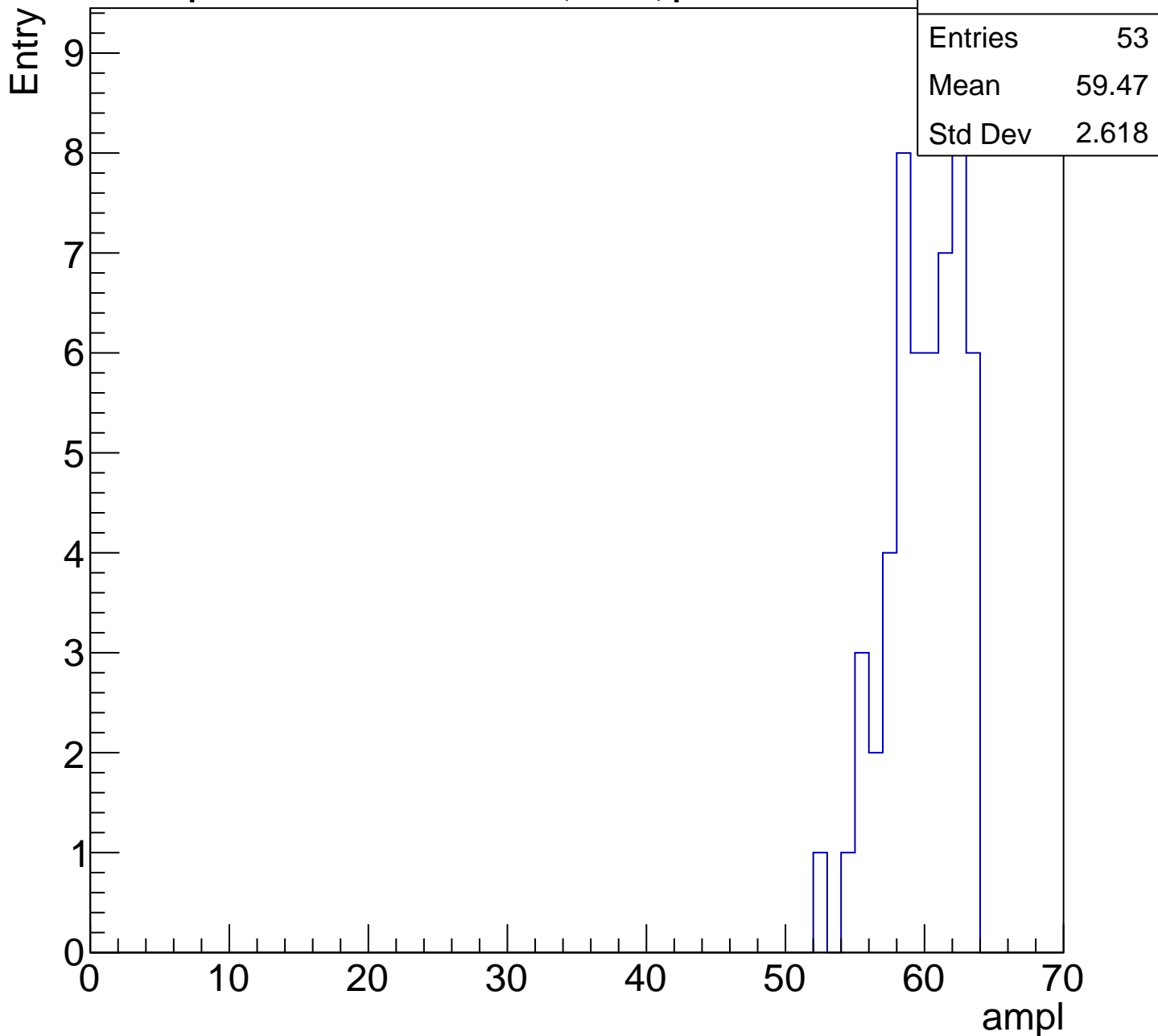
# B1L101S, U9-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch50, adc5

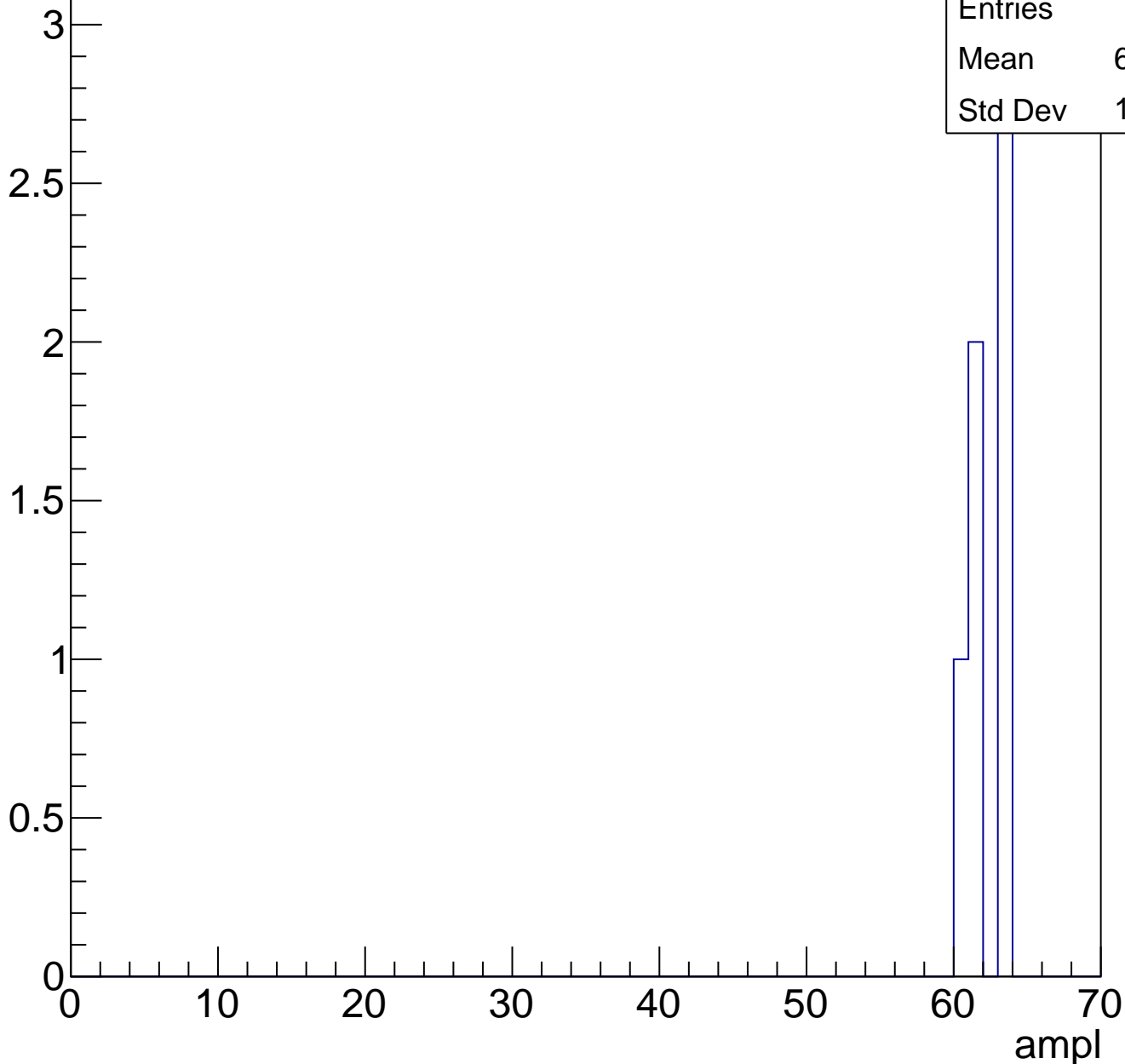
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch51, adc0

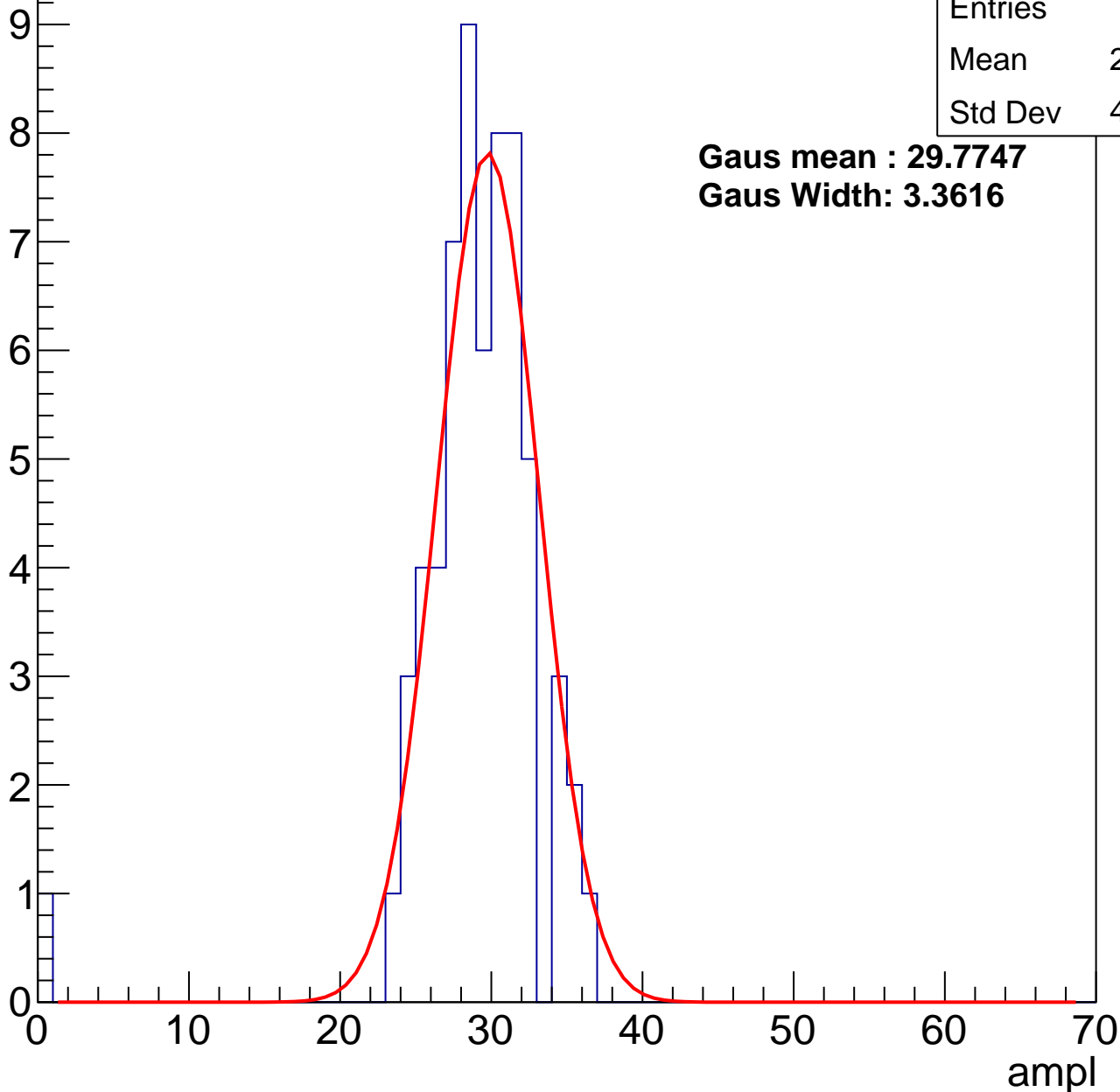
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	28.55
Std Dev	4.679

**Gaus mean : 29.7747**

**Gaus Width: 3.3616**



# B1L101S, U9-ch51, adc1

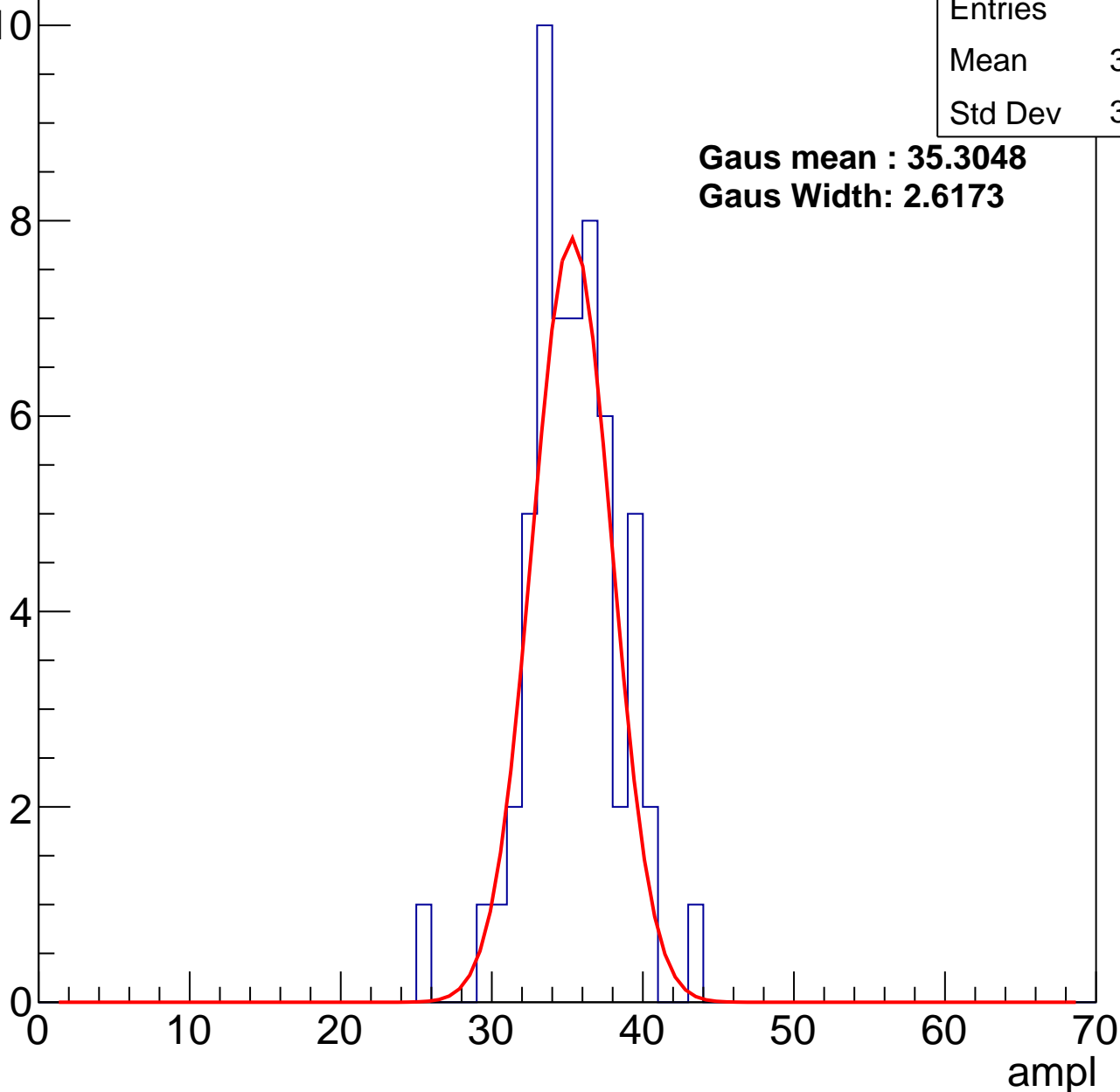
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	34.88
Std Dev	3.018

**Gaus mean : 35.3048**

**Gaus Width: 2.6173**



# B1L101S, U9-ch51, adc2

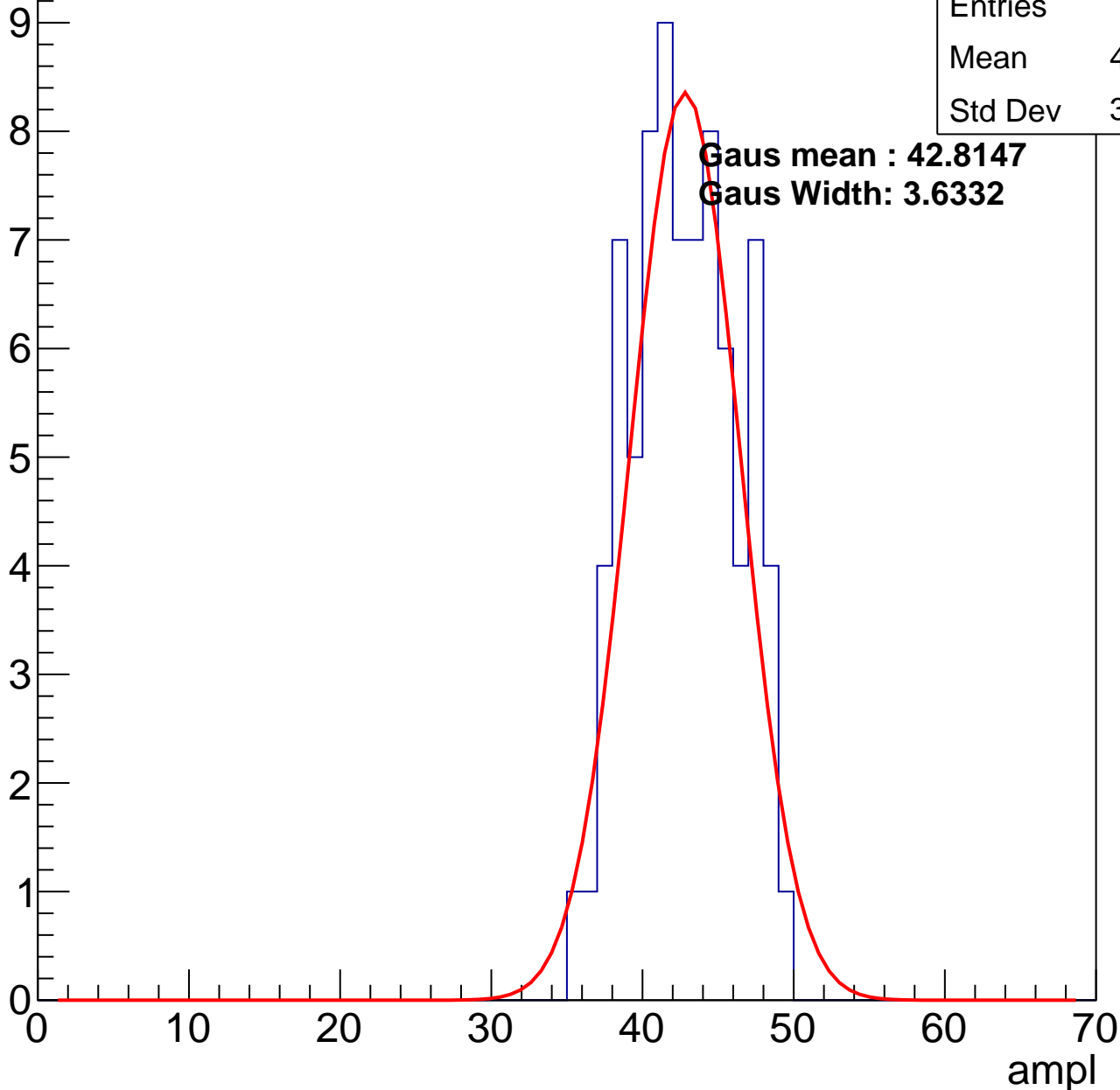
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	42.28
Std Dev	3.379

**Gaus mean : 42.8147**

**Gaus Width: 3.6332**

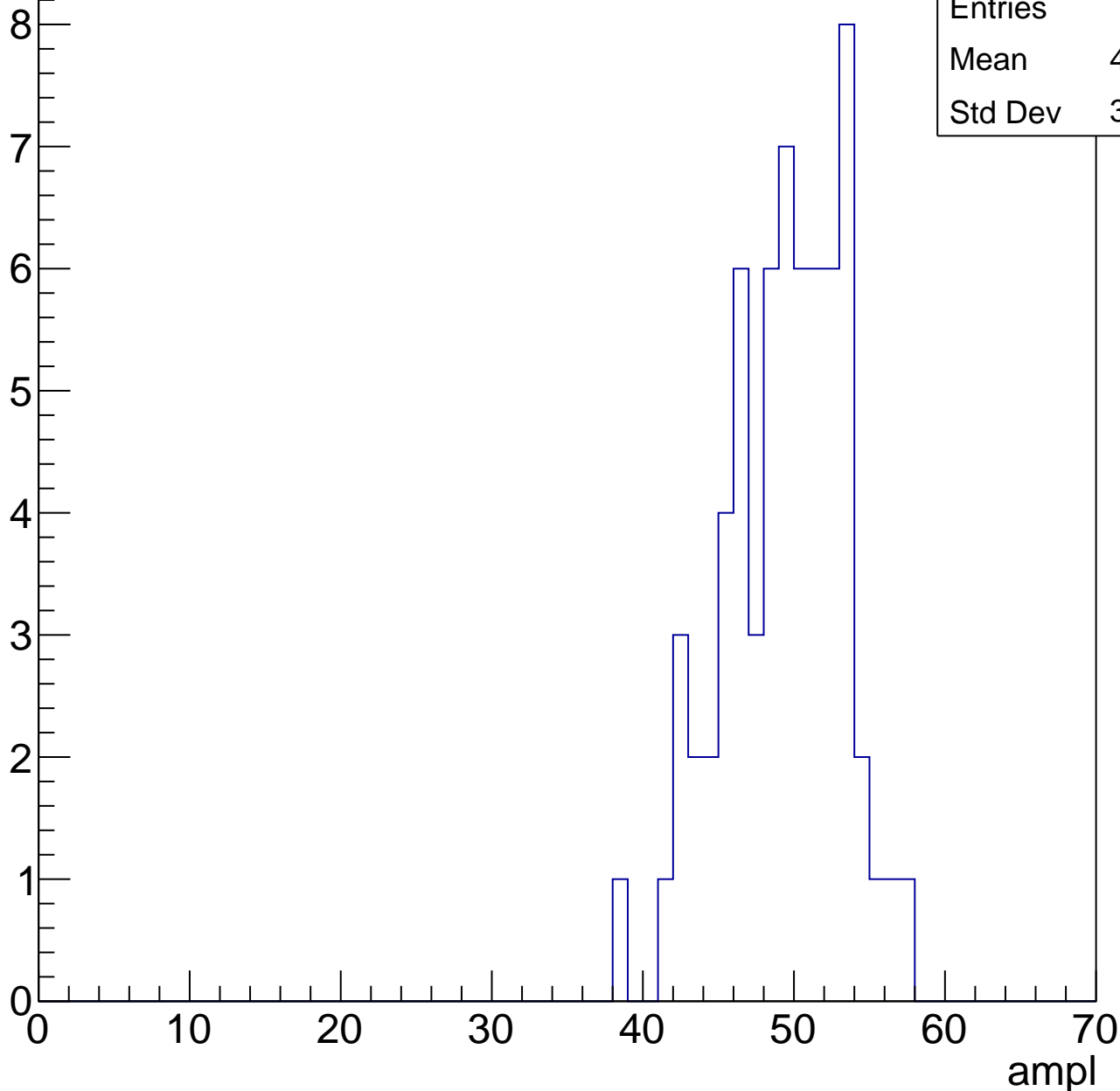


# B1L101S, U9-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

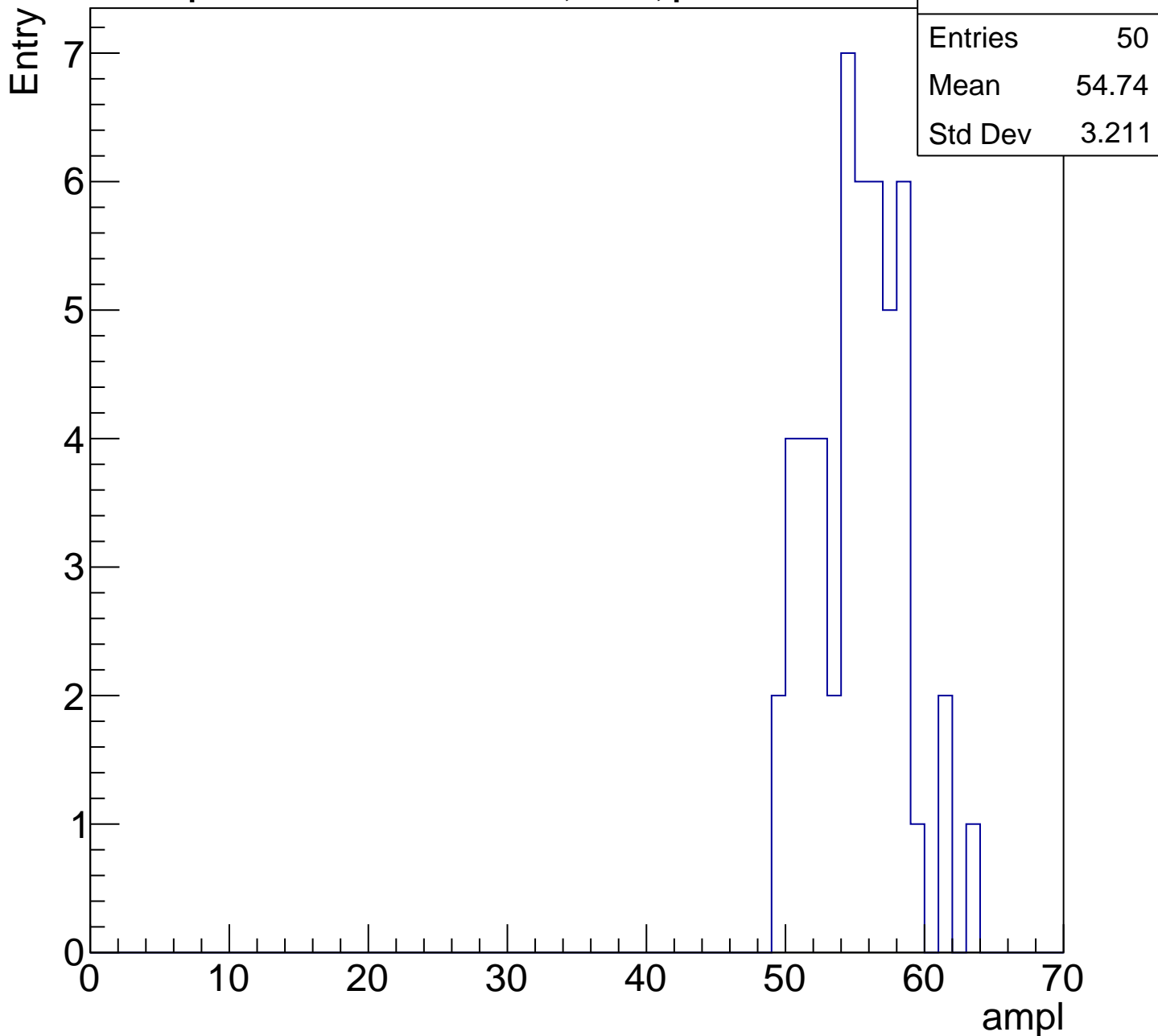
Entry

Entries	66
Mean	48.86
Std Dev	3.892



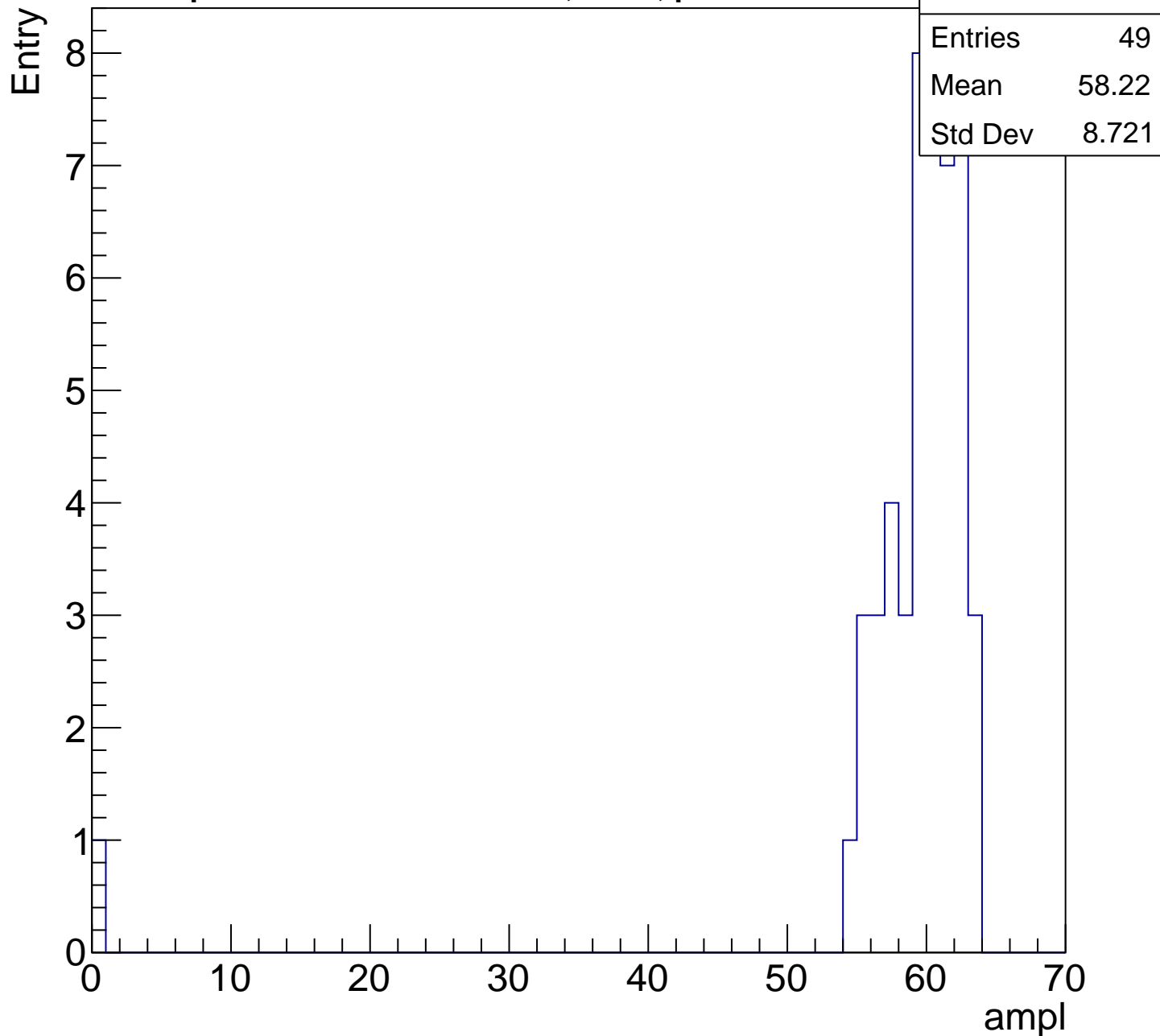
# B1L101S, U9-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

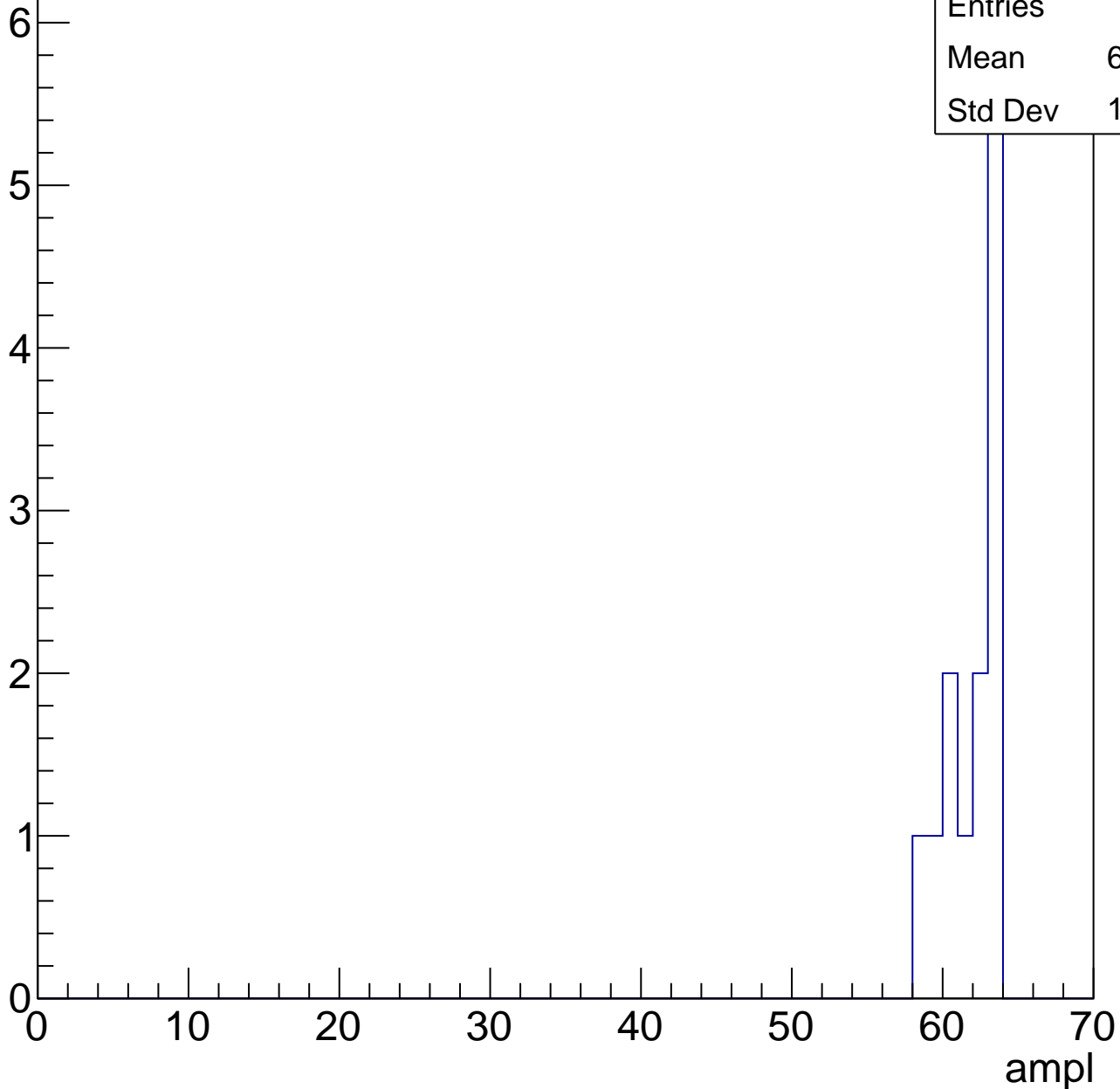


# B1L101S, U9-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	13
Mean	61.54
Std Dev	1.692





# B1L101S, U9-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U9-ch52, adc0

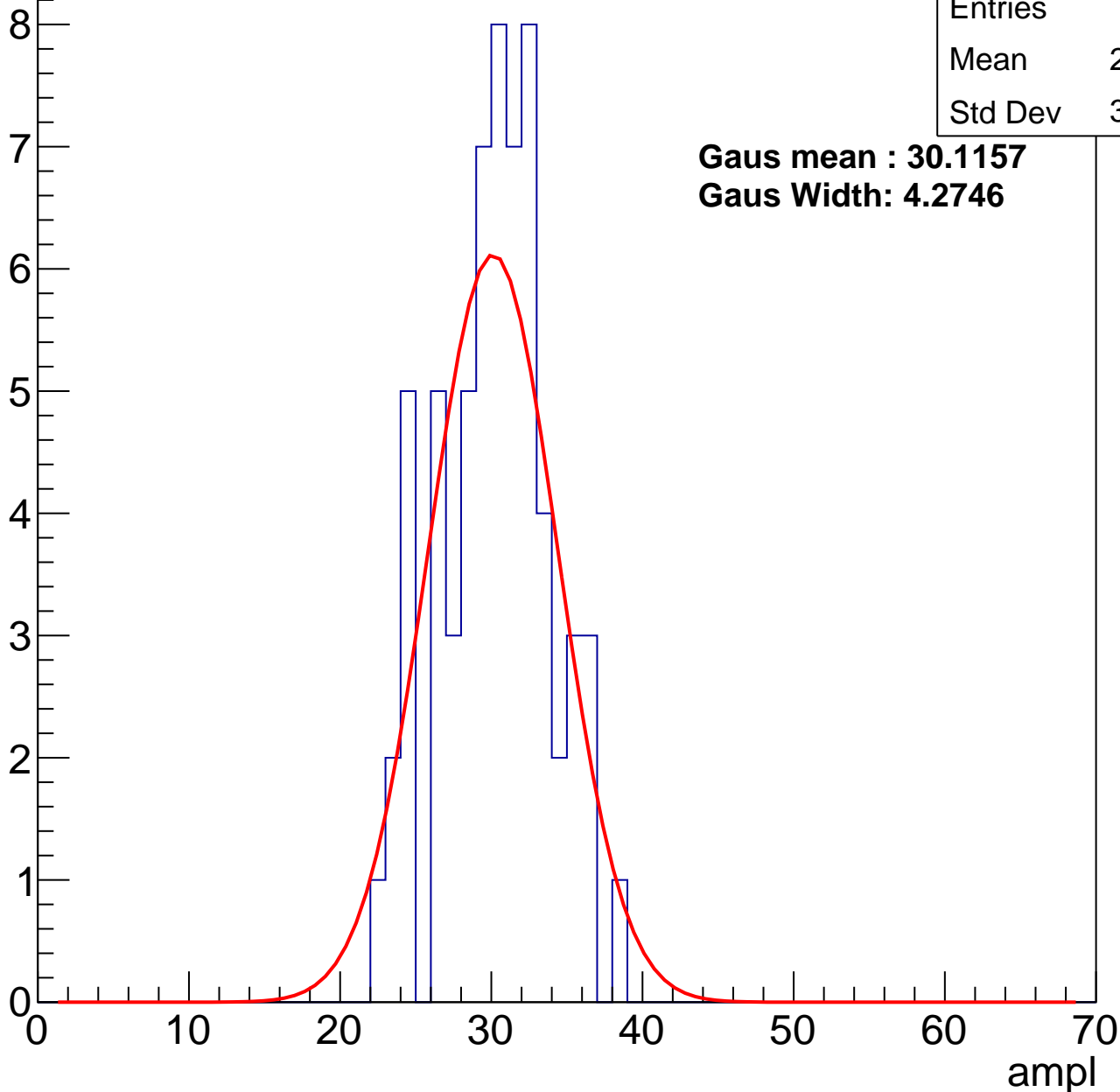
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	29.78
Std Dev	3.595

**Gaus mean : 30.1157**

**Gaus Width: 4.2746**



# B1L101S, U9-ch52, adc1

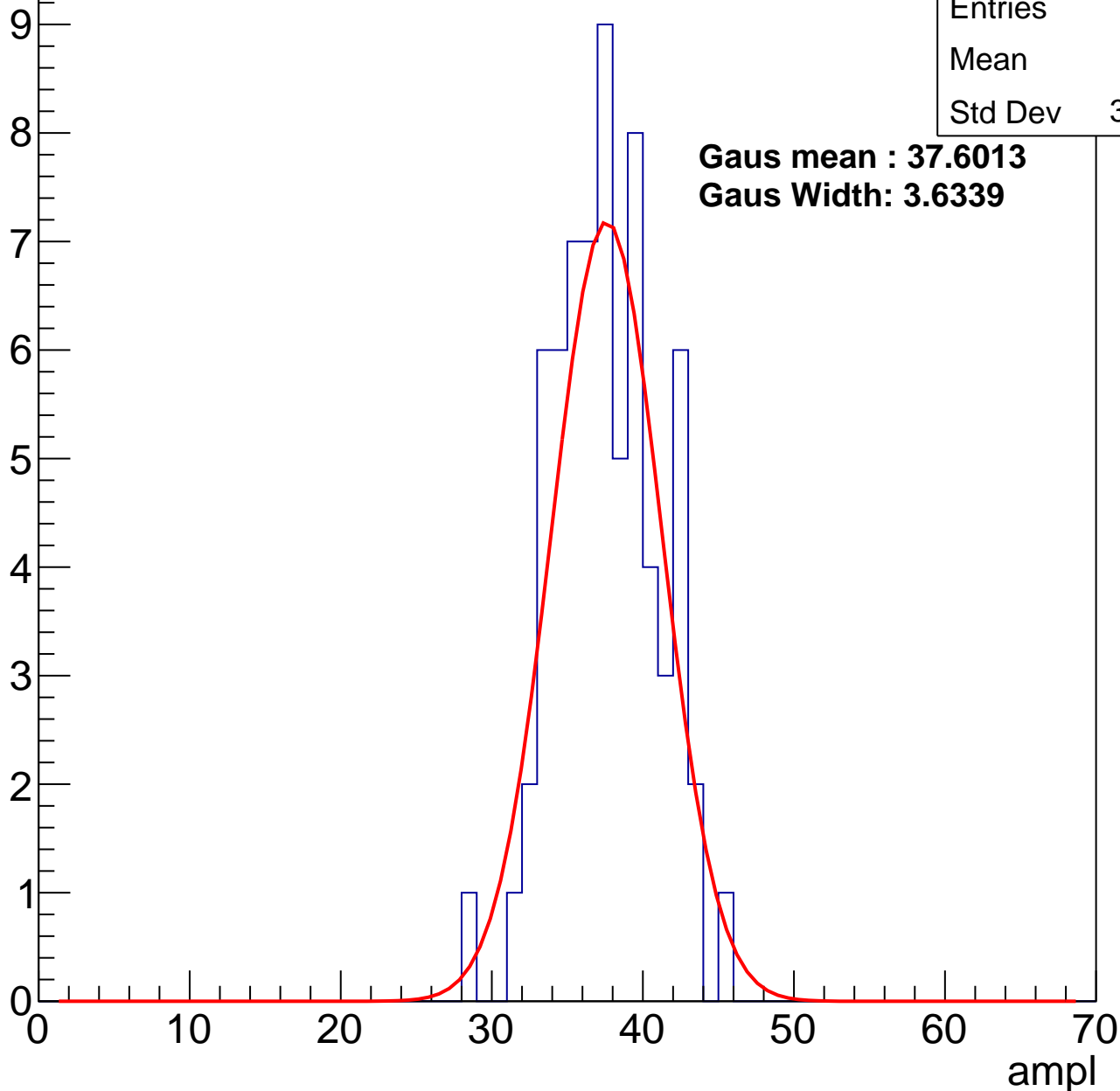
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	37.1
Std Dev	3.339

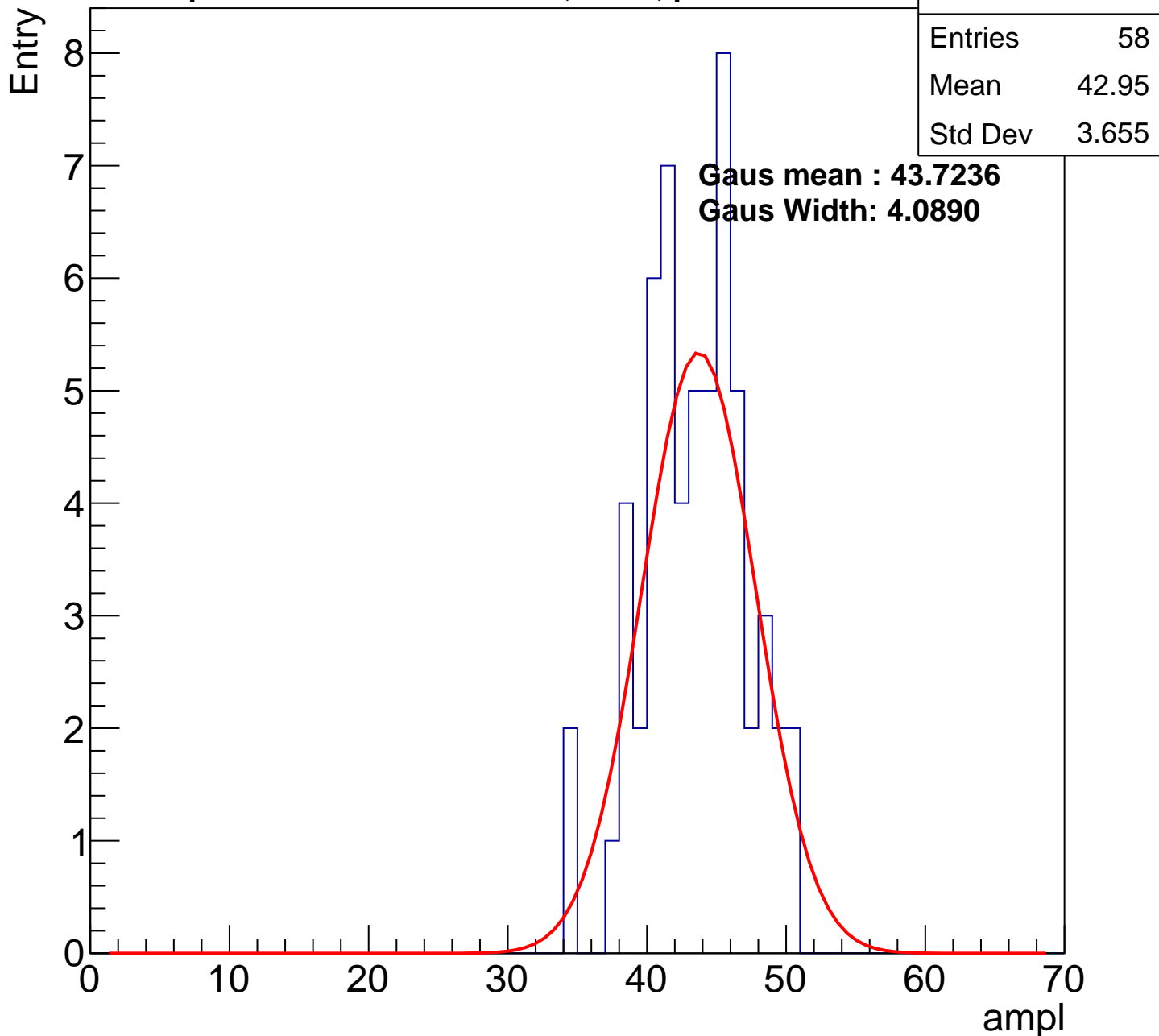
**Gaus mean : 37.6013**

**Gaus Width: 3.6339**



# B1L101S, U9-ch52, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

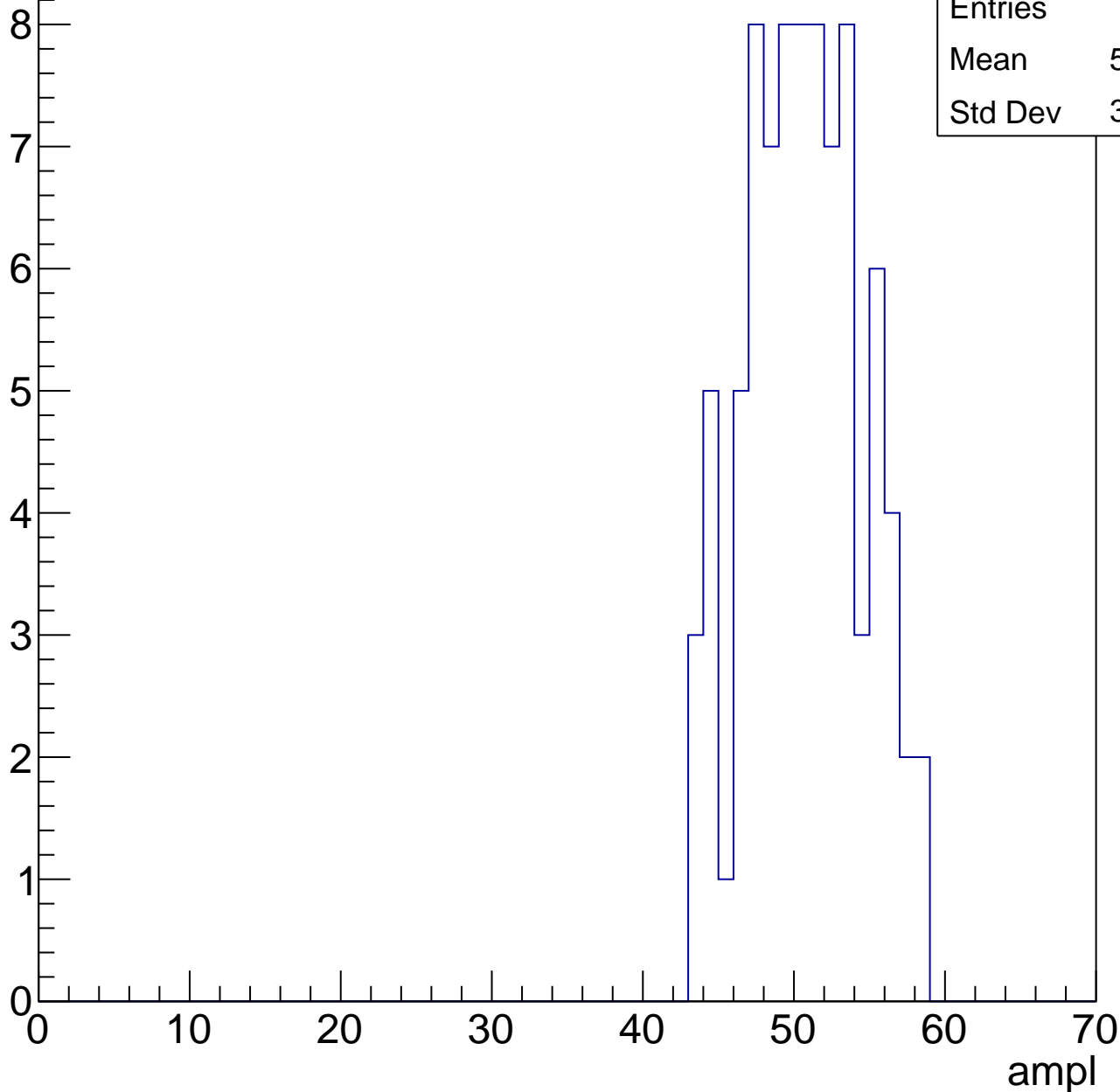


# B1L101S, U9-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

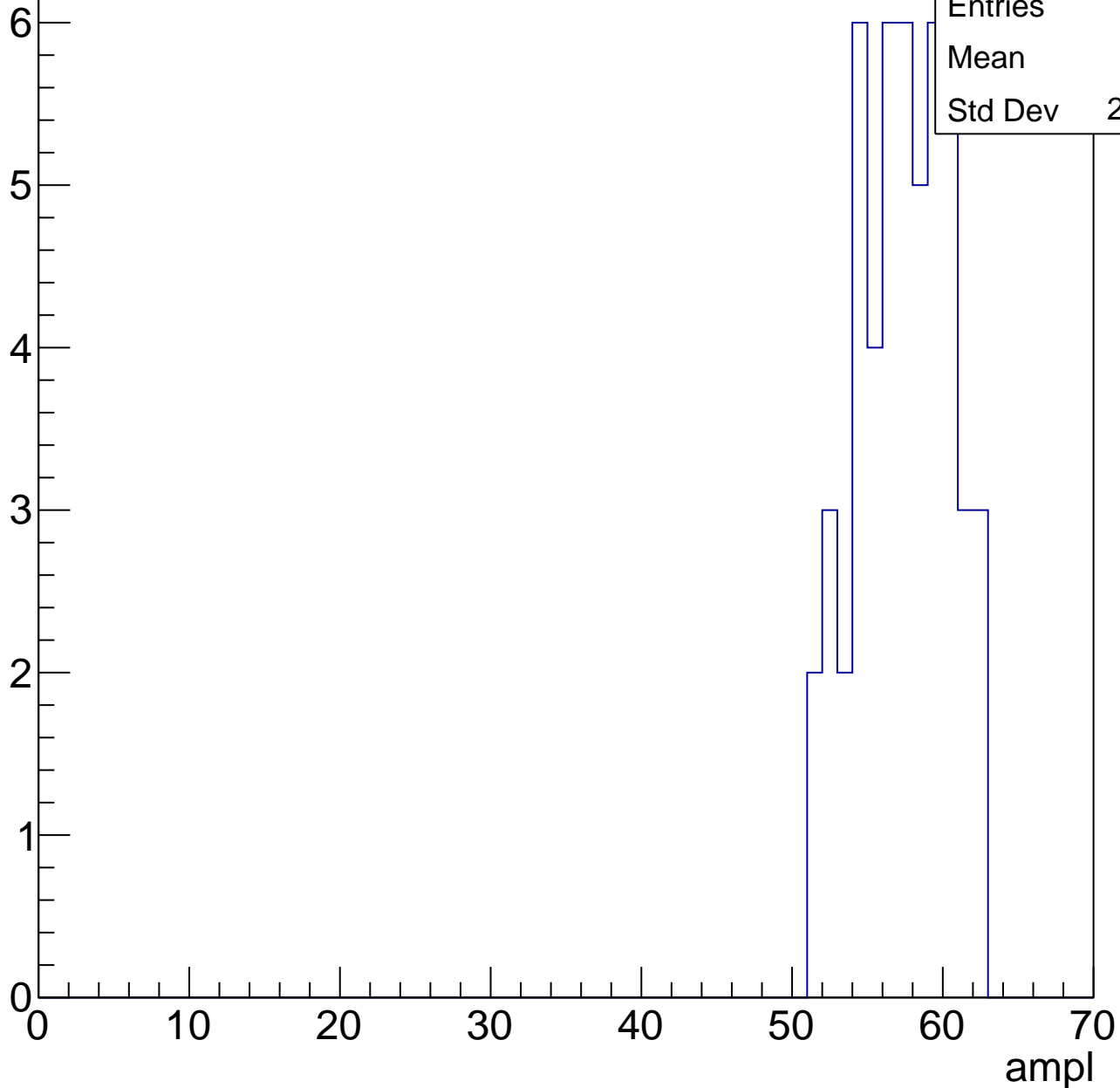
Entries	85
Mean	50.24
Std Dev	3.775



# B1L101S, U9-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



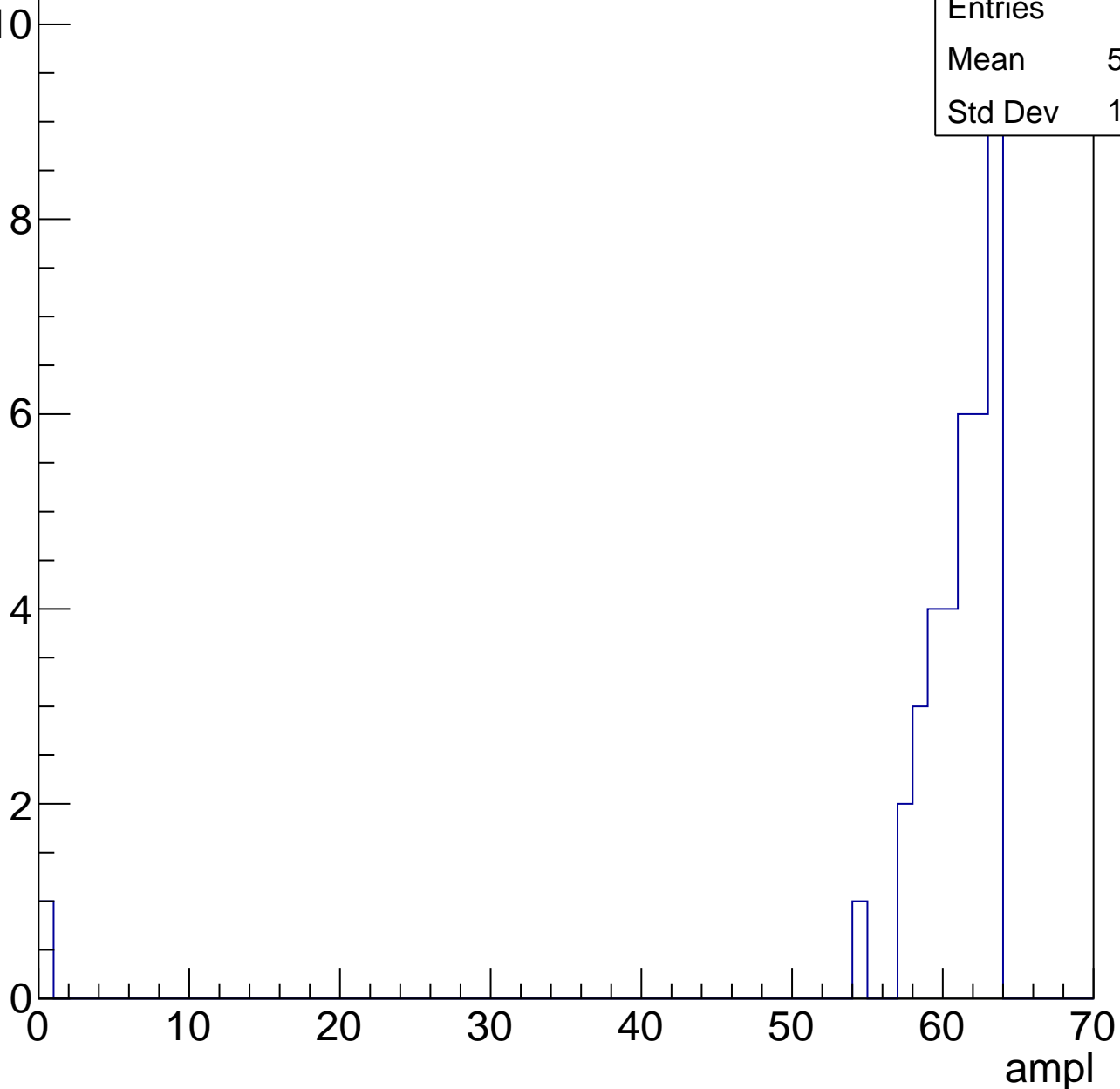
Entries	52
Mean	56.9
Std Dev	2.976

# B1L101S, U9-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

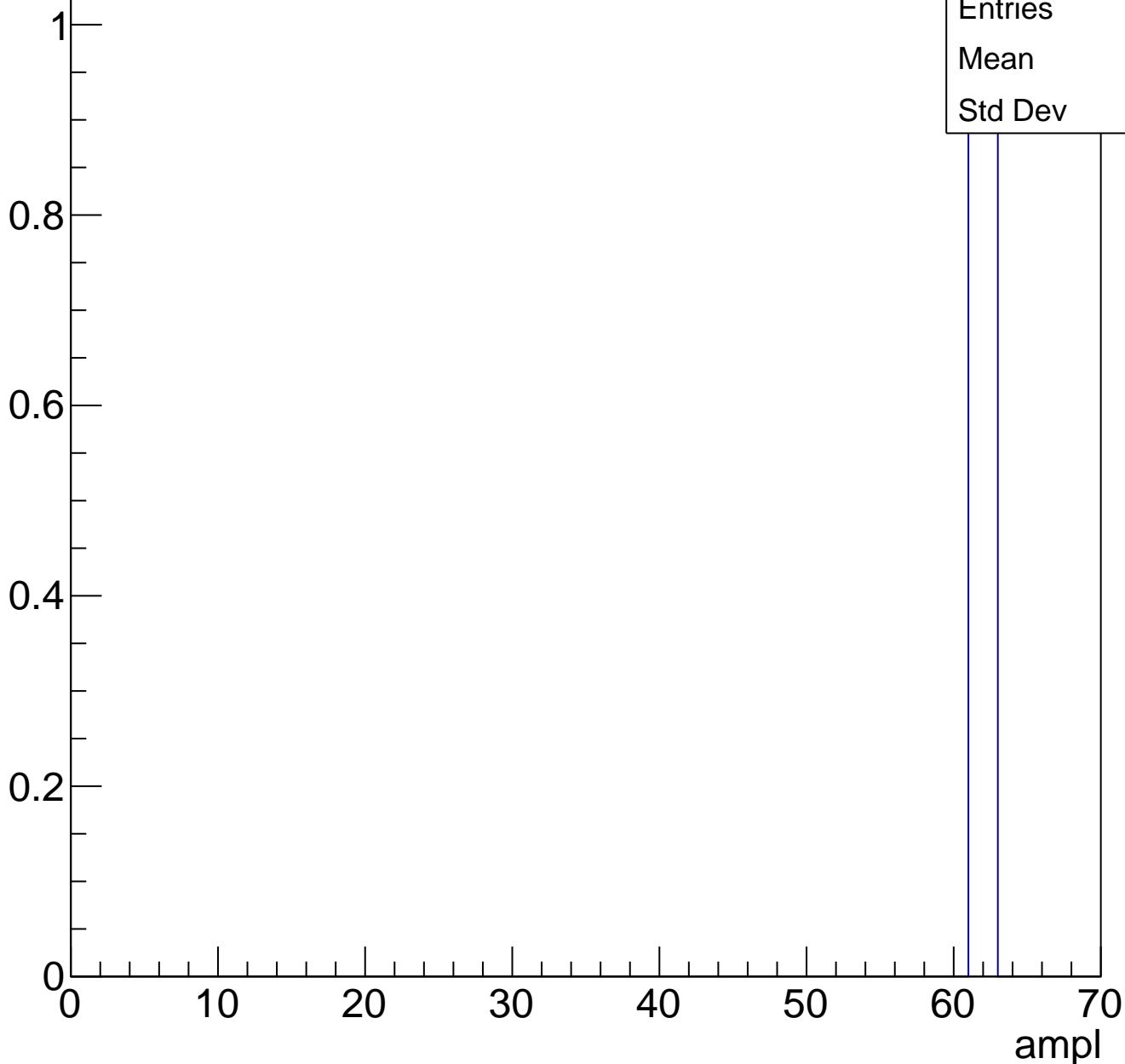
Entries	37
Mean	59.08
Std Dev	10.08



# B1L101S, U9-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U9-ch53, adc0

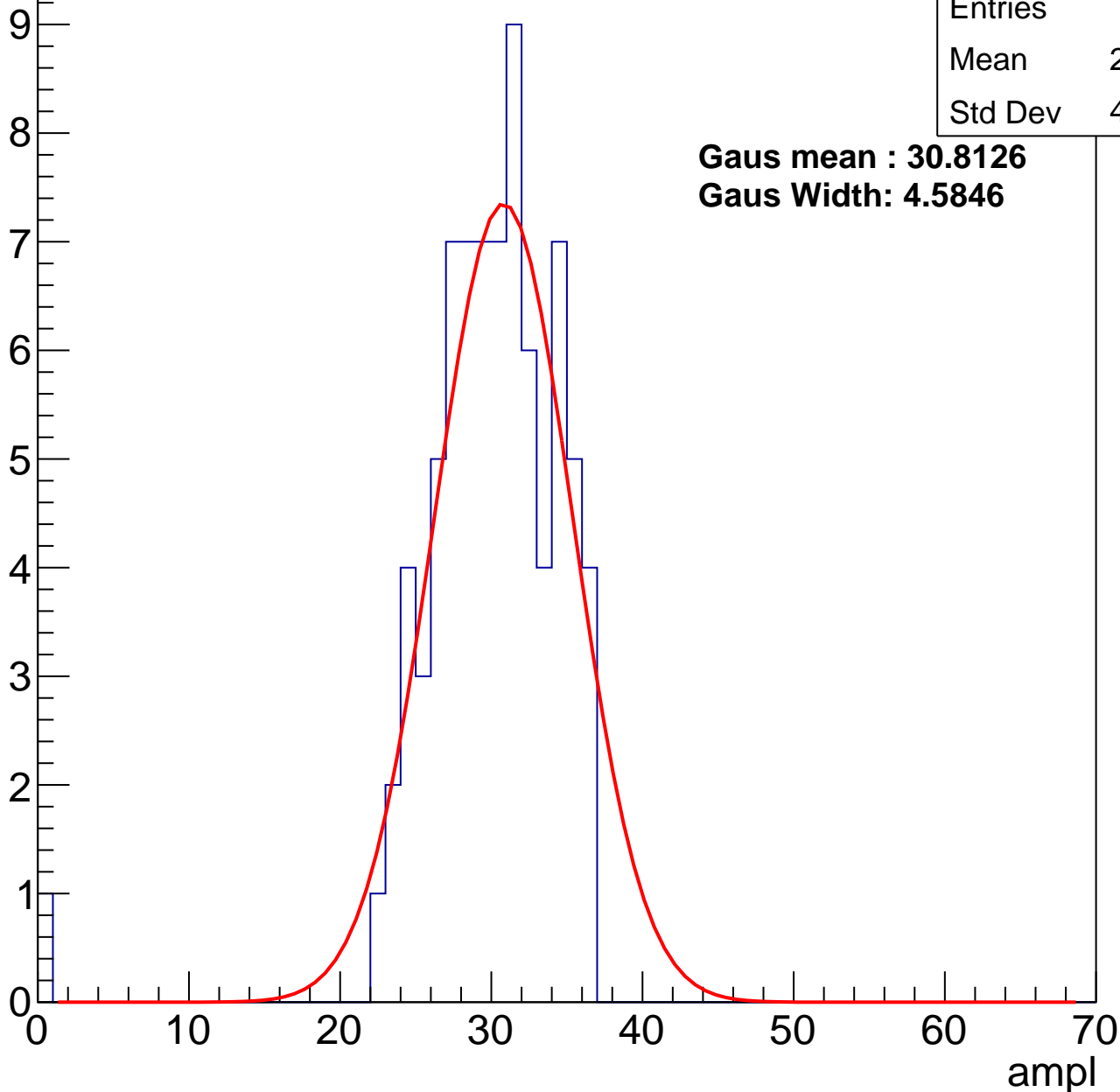
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	29.46
Std Dev	4.886

**Gaus mean : 30.8126**

**Gaus Width: 4.5846**



# B1L101S, U9-ch53, adc1

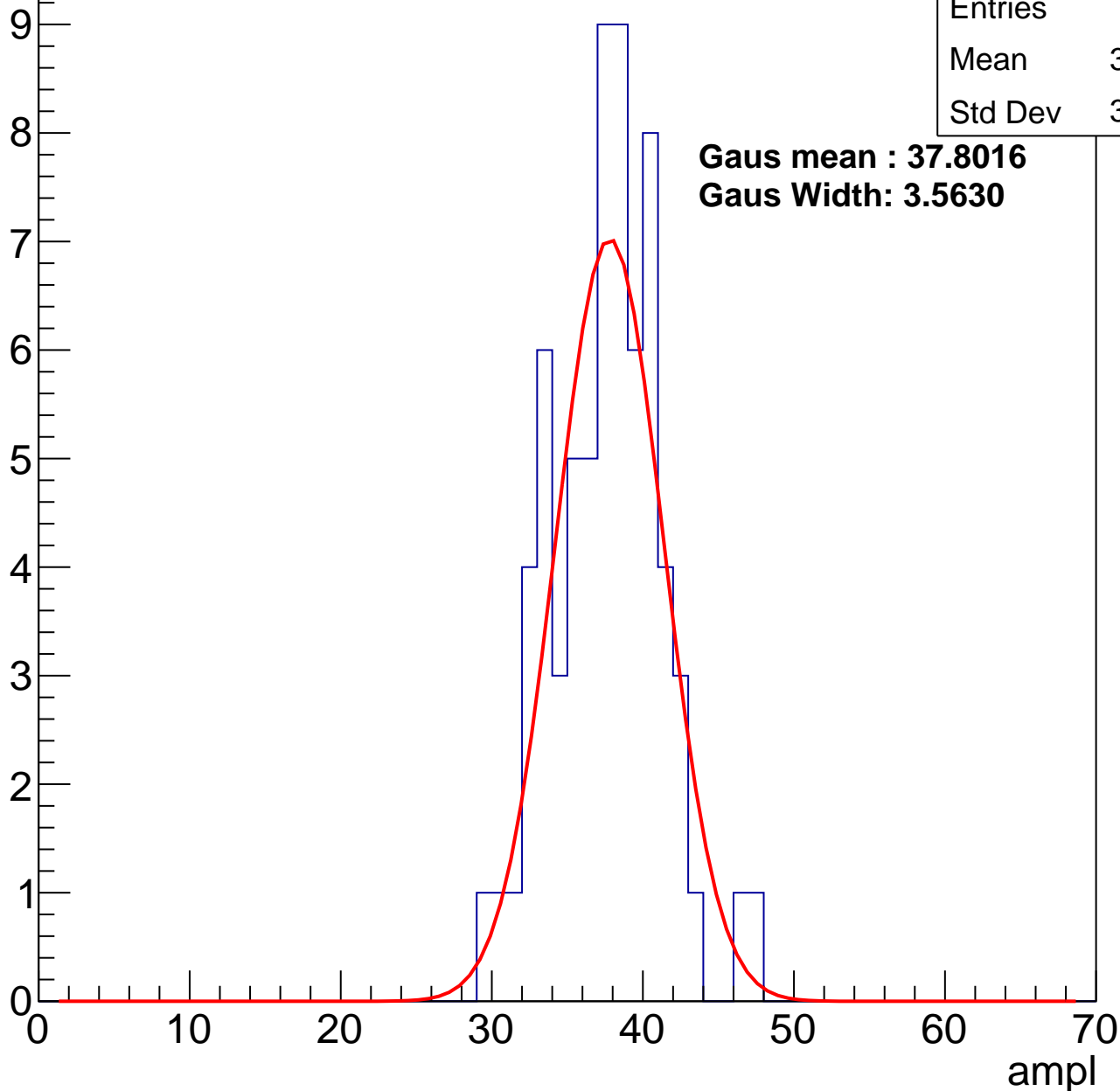
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	37.18
Std Dev	3.548

**Gaus mean : 37.8016**

**Gaus Width: 3.5630**



# B1L101S, U9-ch53, adc2

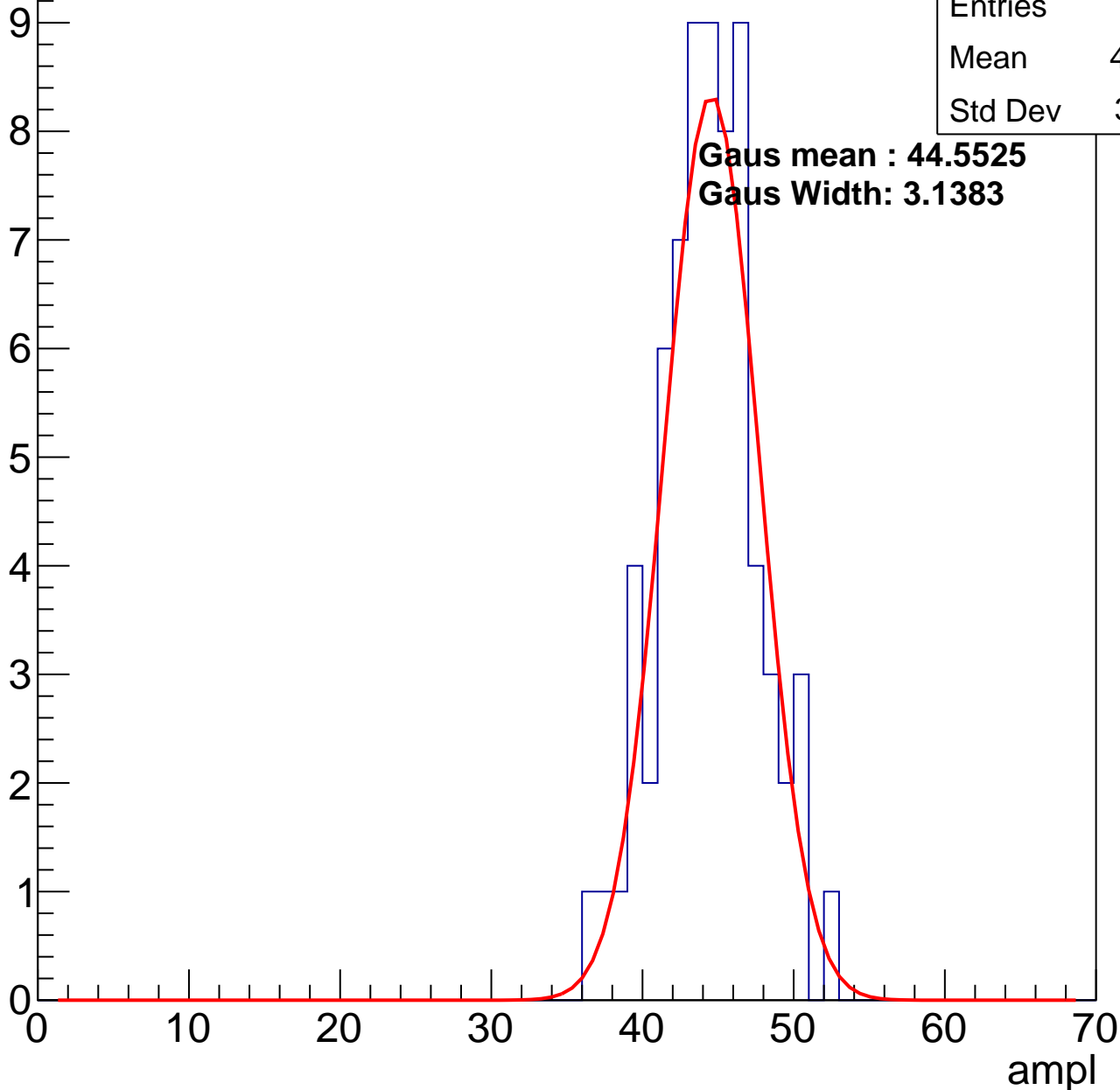
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	43.94
Std Dev	3.211

**Gaus mean : 44.5525**

**Gaus Width: 3.1383**

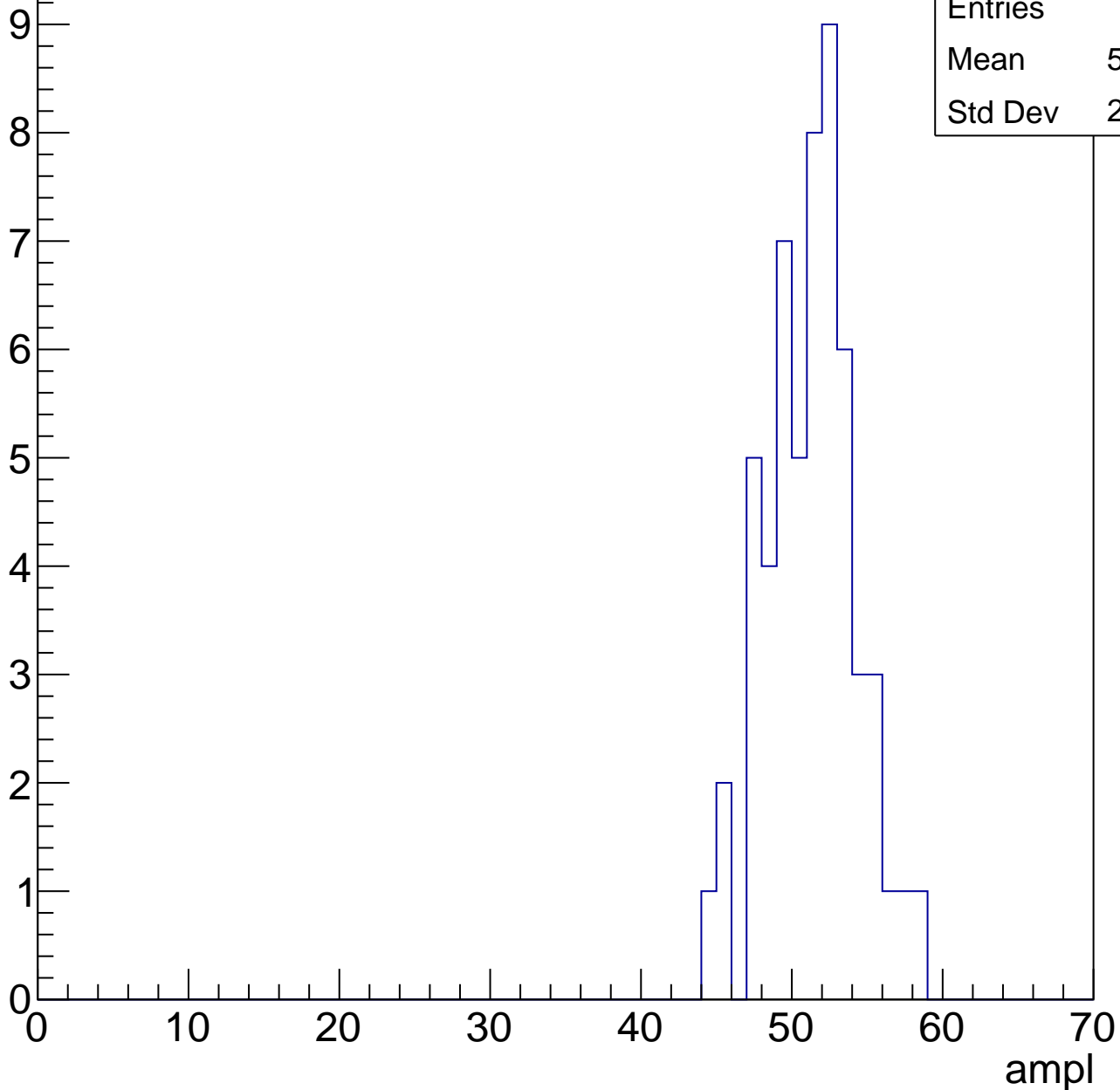


# B1L101S, U9-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	50.82
Std Dev	2.947

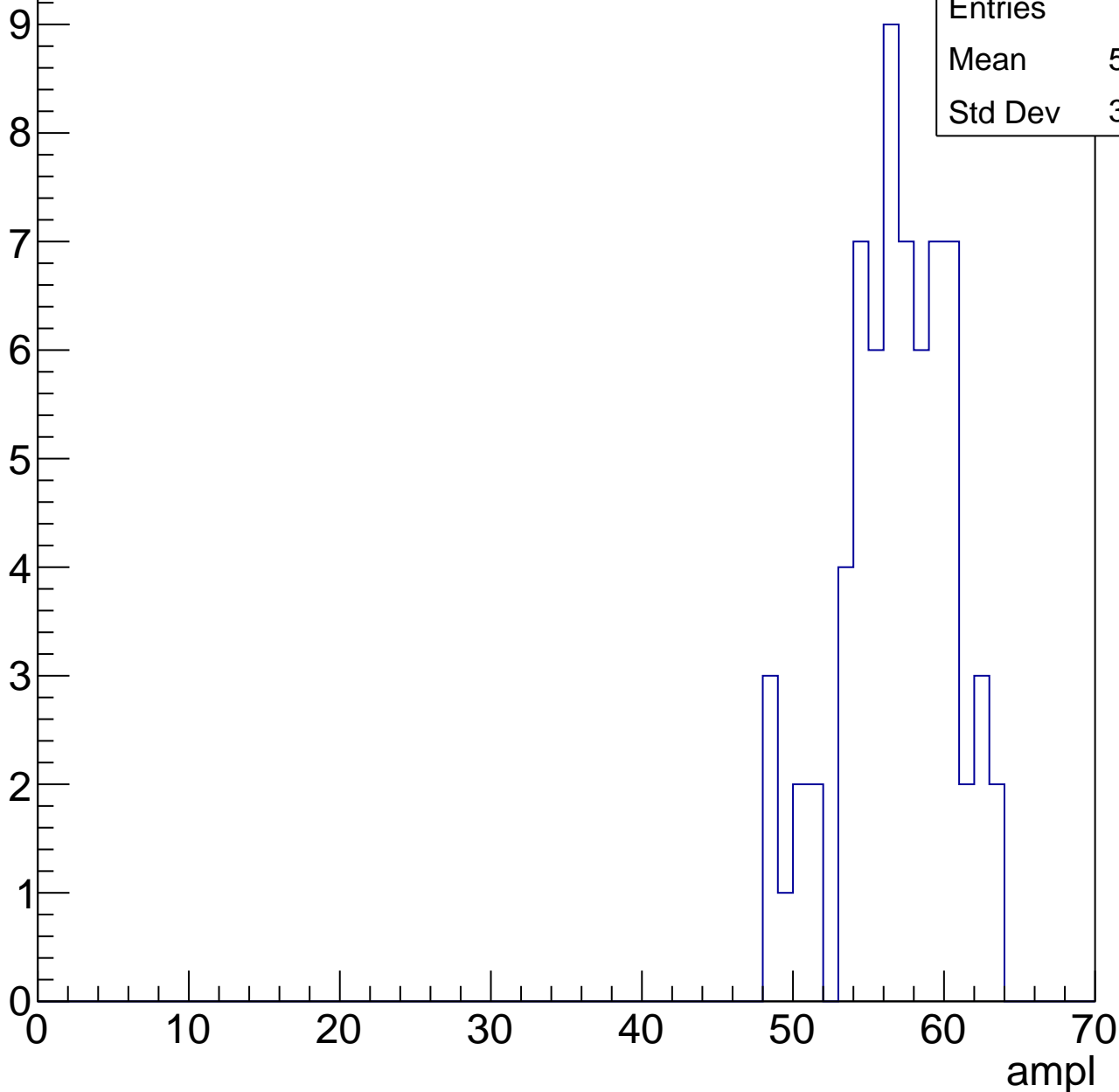


# B1L101S, U9-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	56.37
Std Dev	3.609

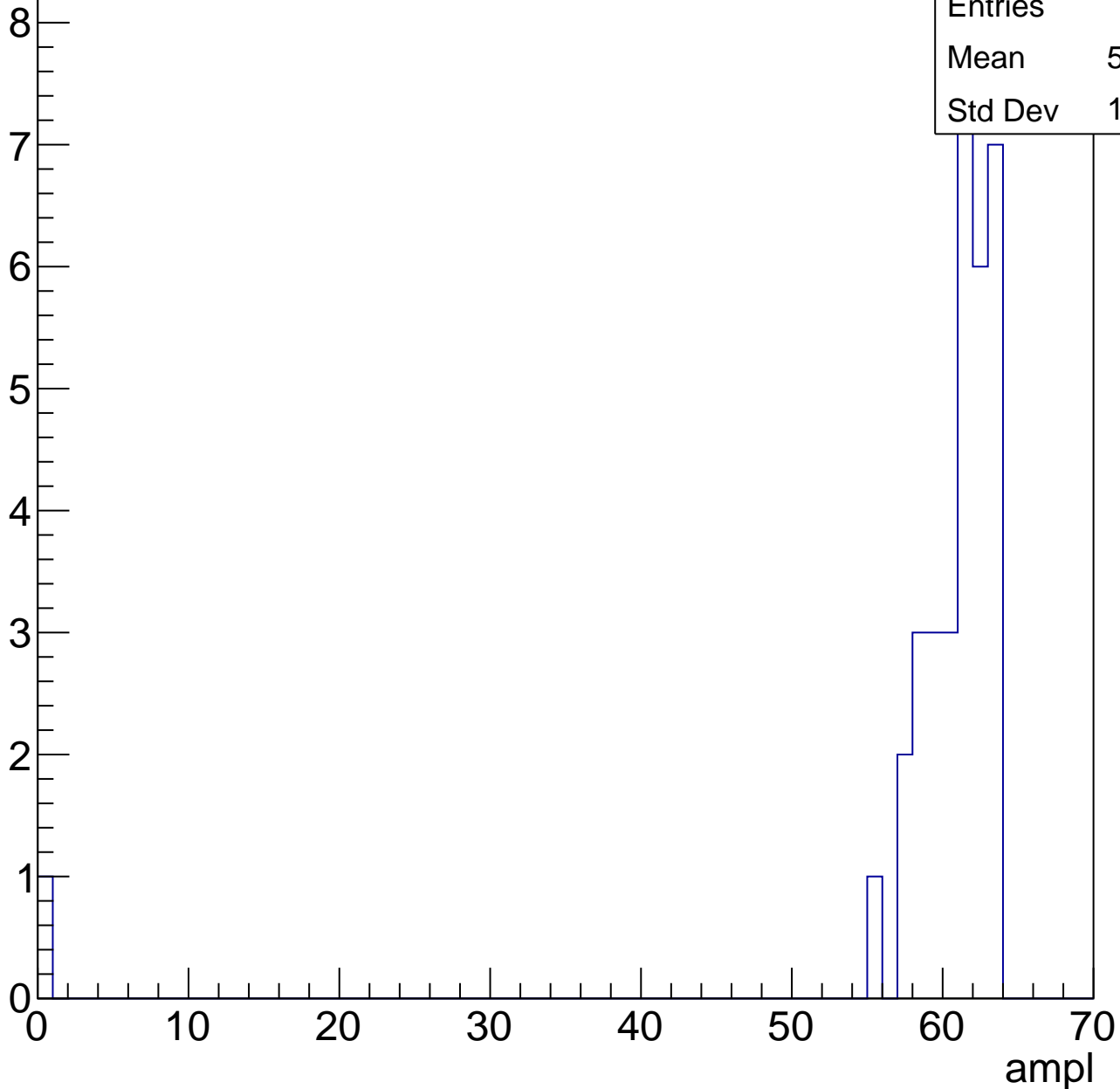


# B1L101S, U9-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	34
Mean	58.85
Std Dev	10.44



# B1L101S, U9-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

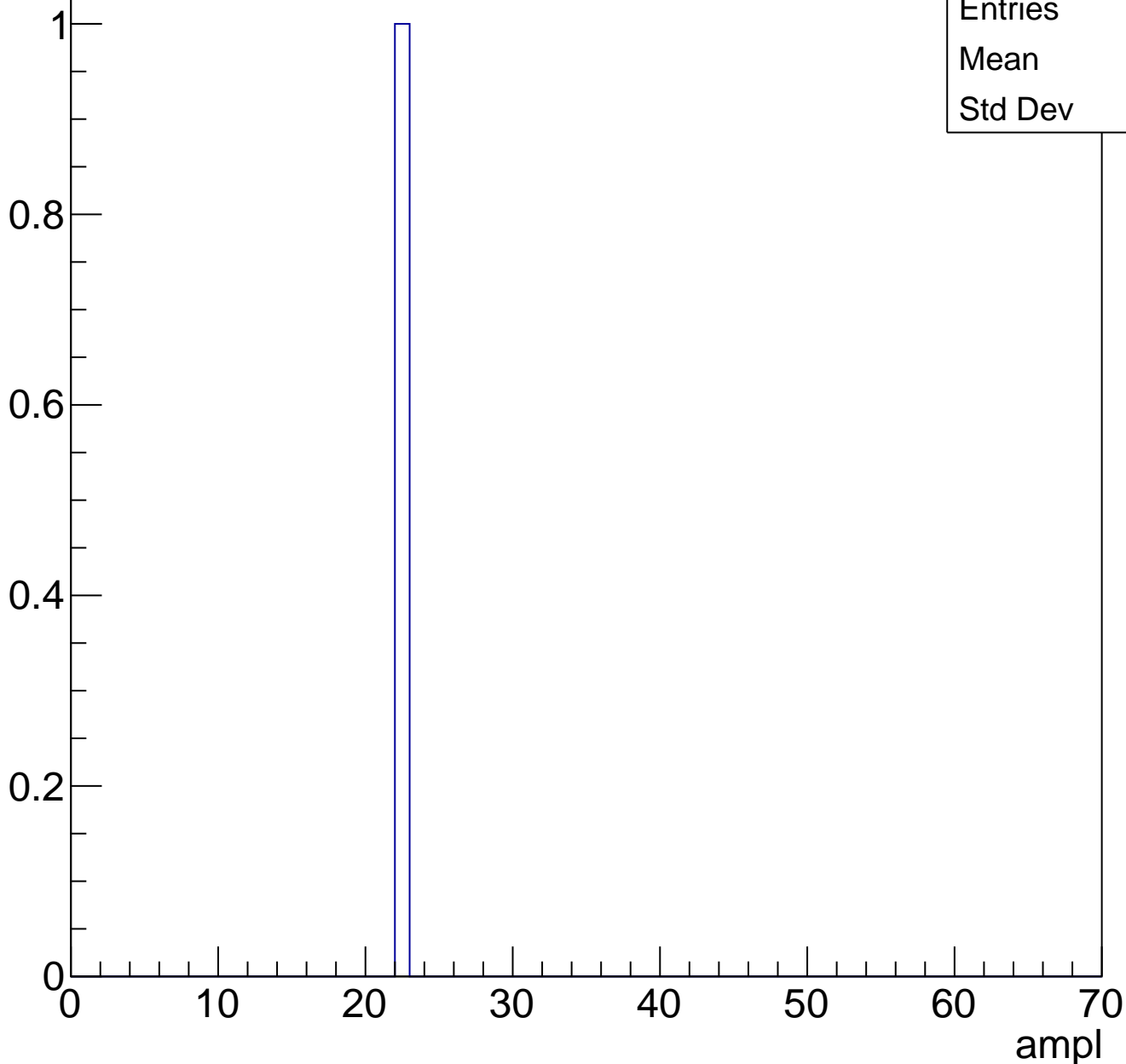




# B1L101S, U9-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

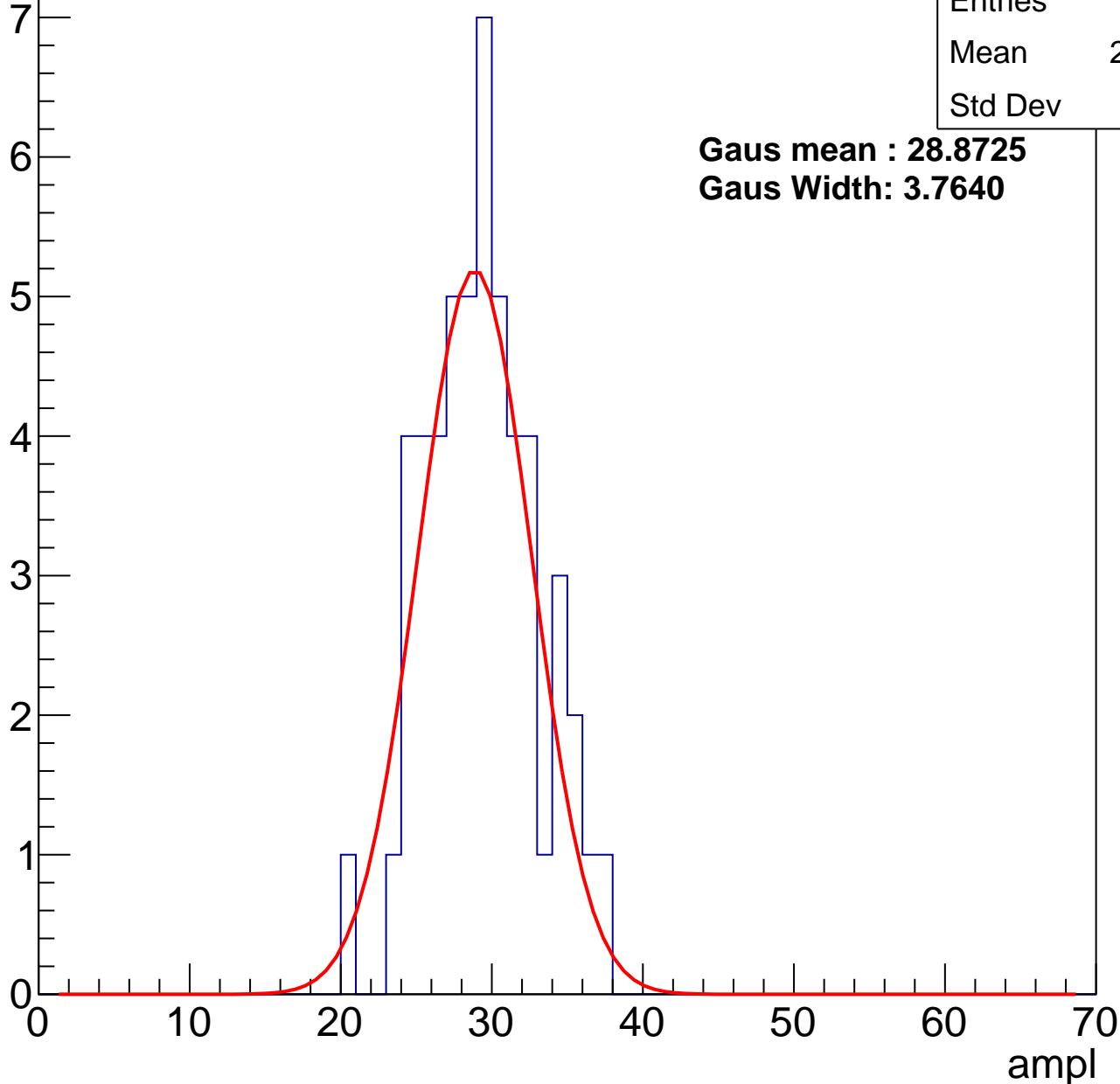
Entry



# B1L101S, U9-ch54, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch54, adc1

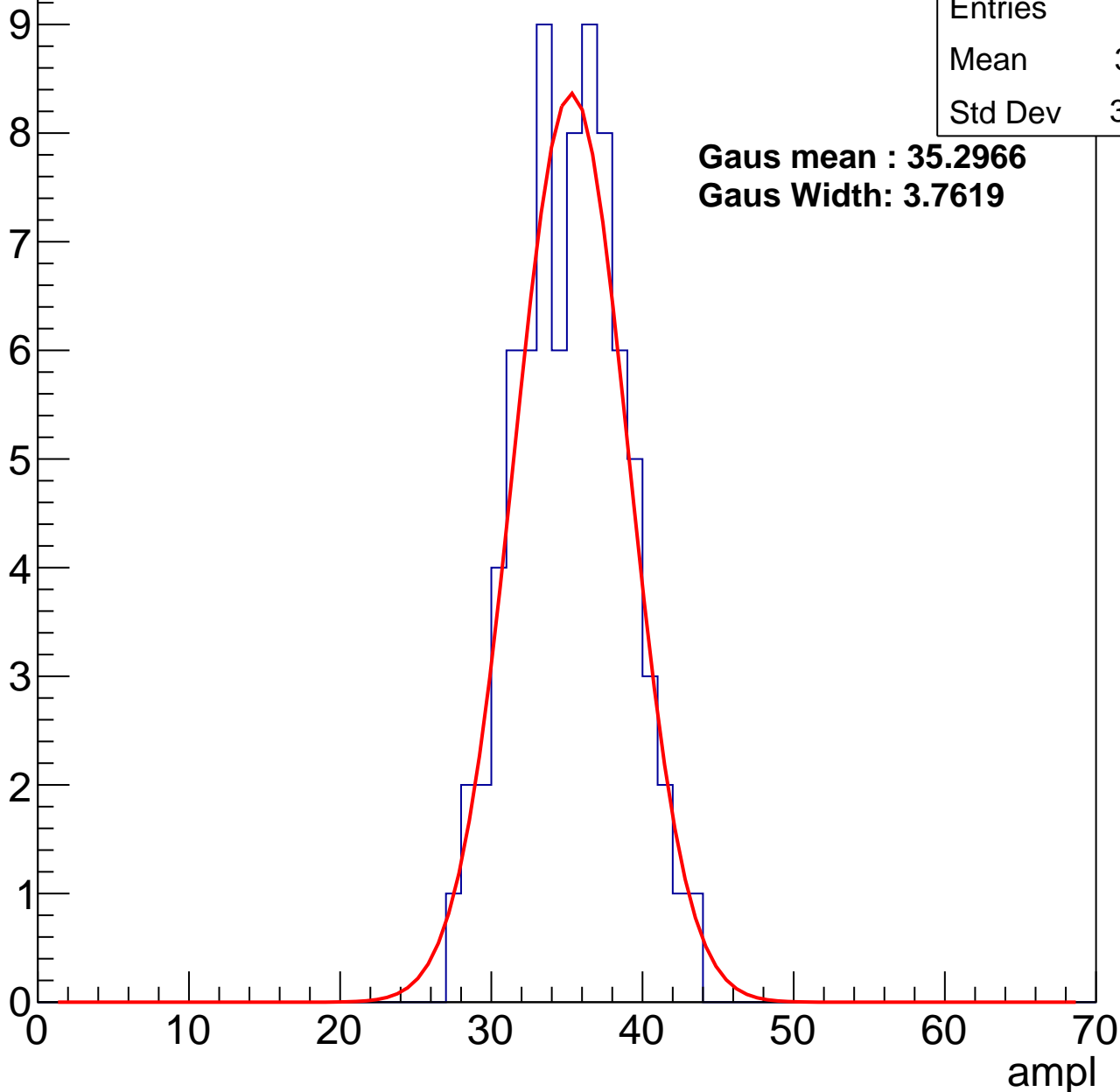
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	34.81
Std Dev	3.483

**Gaus mean : 35.2966**

**Gaus Width: 3.7619**



# B1L101S, U9-ch54, adc2

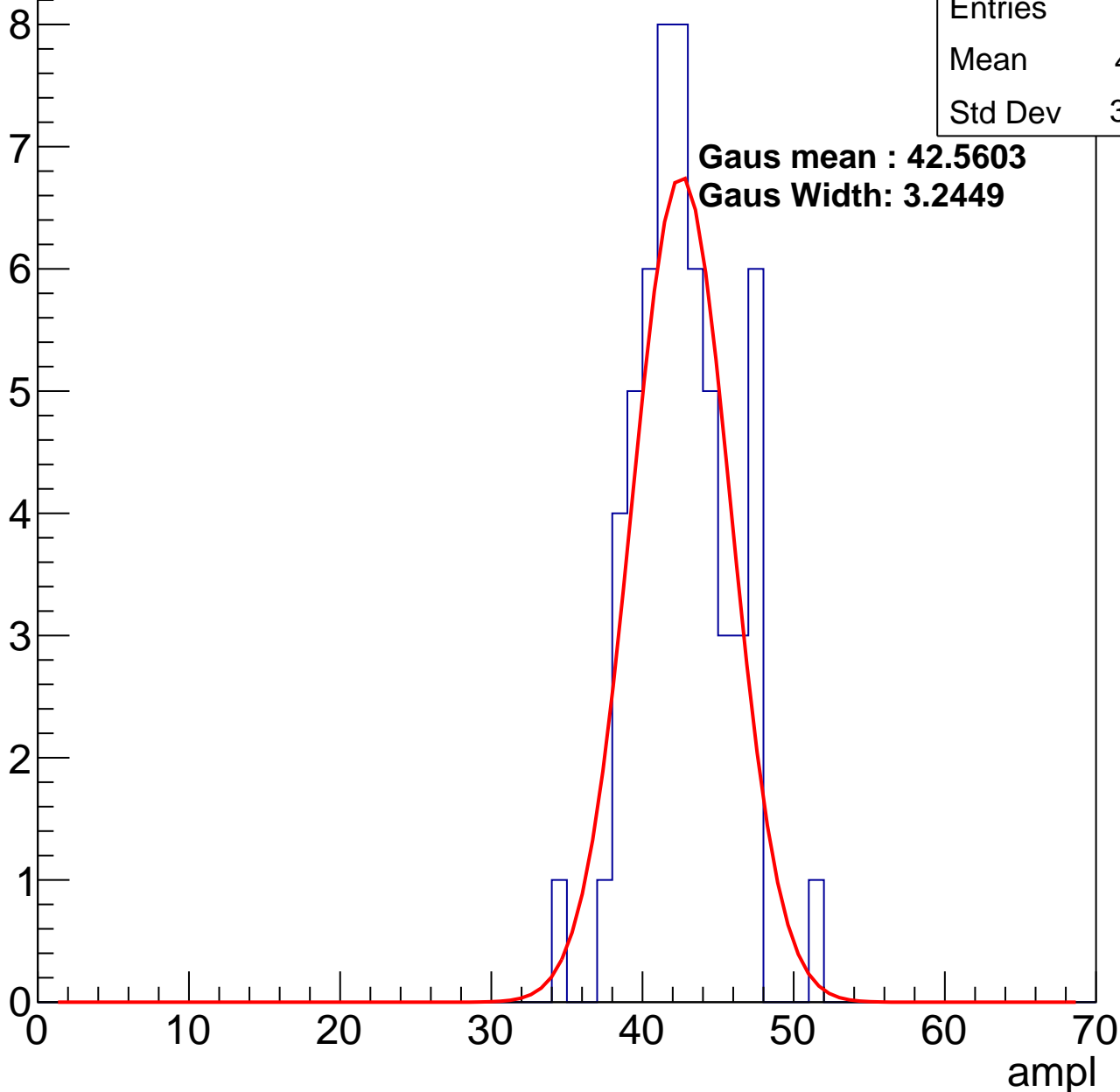
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	42.21
Std Dev	3.133

**Gaus mean : 42.5603**

**Gaus Width: 3.2449**



# B1L101S, U9-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

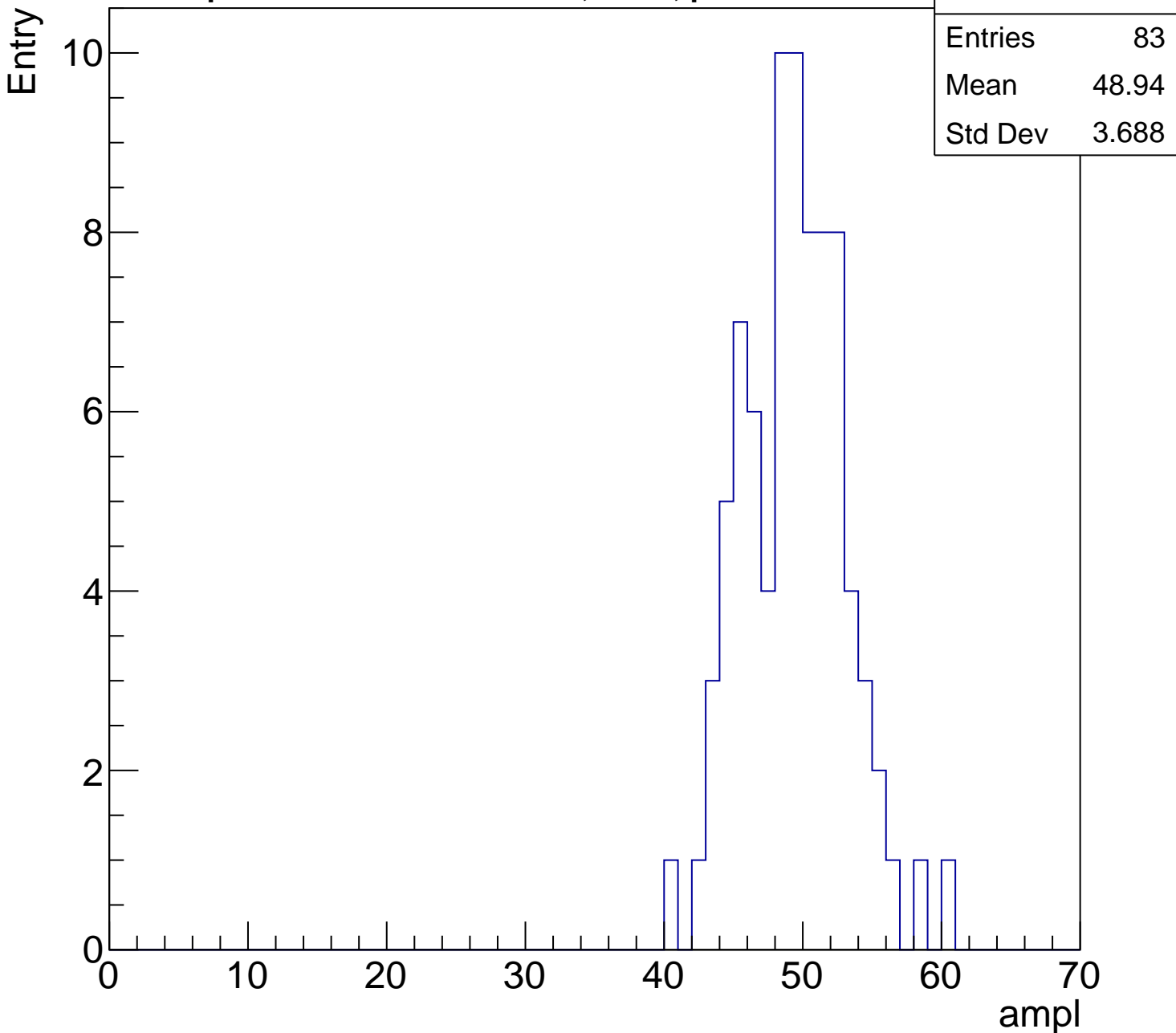
Entries	83
Mean	48.94
Std Dev	3.688

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

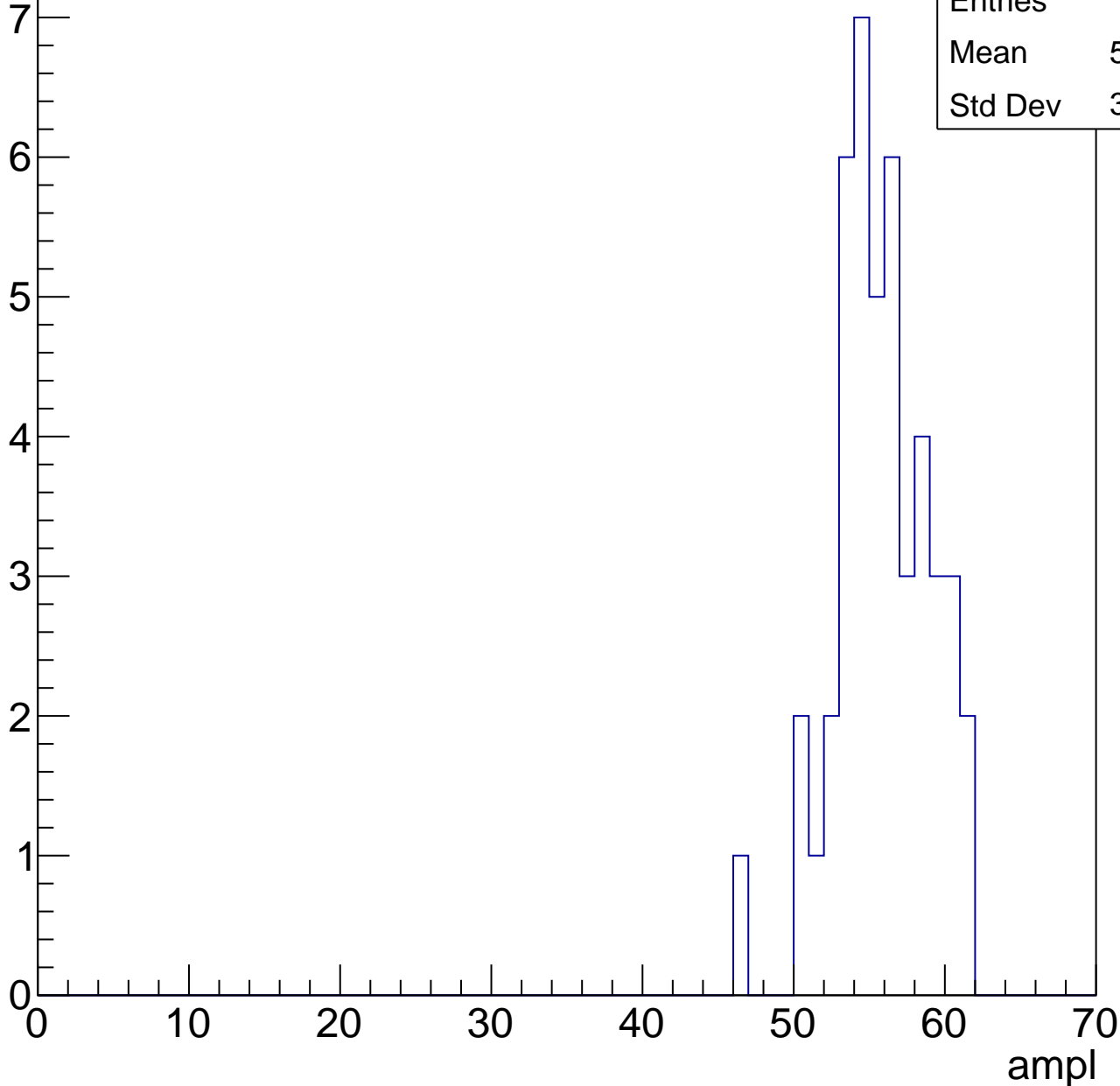


# B1L101S, U9-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	55.33
Std Dev	3.127



# B1L101S, U9-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

0

10

20

30

40

50

60

70

ampl

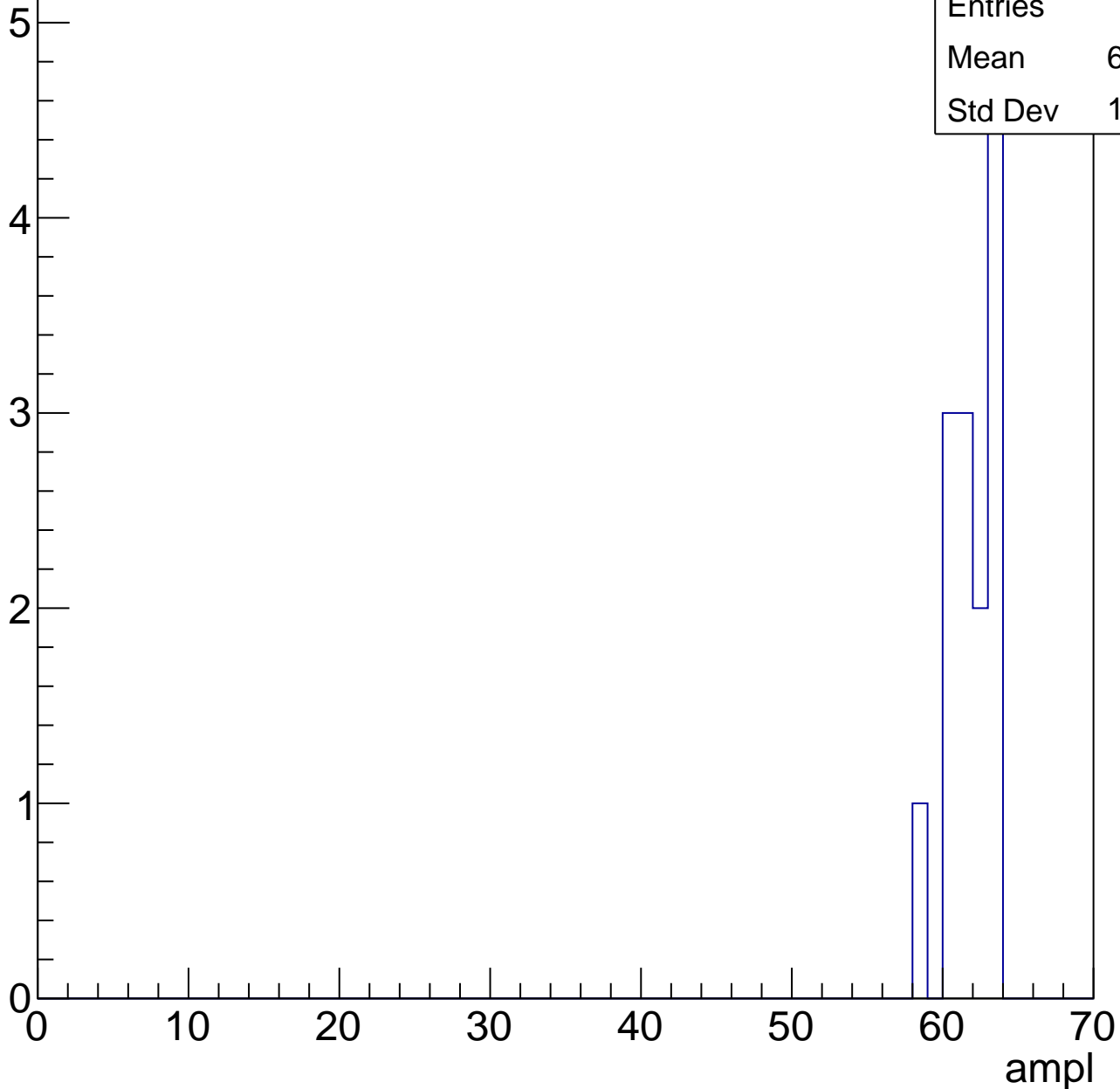
Entries	44
Mean	59.34
Std Dev	2.467

# B1L101S, U9-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	14
Mean	61.43
Std Dev	1.498





# B1L101S, U9-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch55, adc0

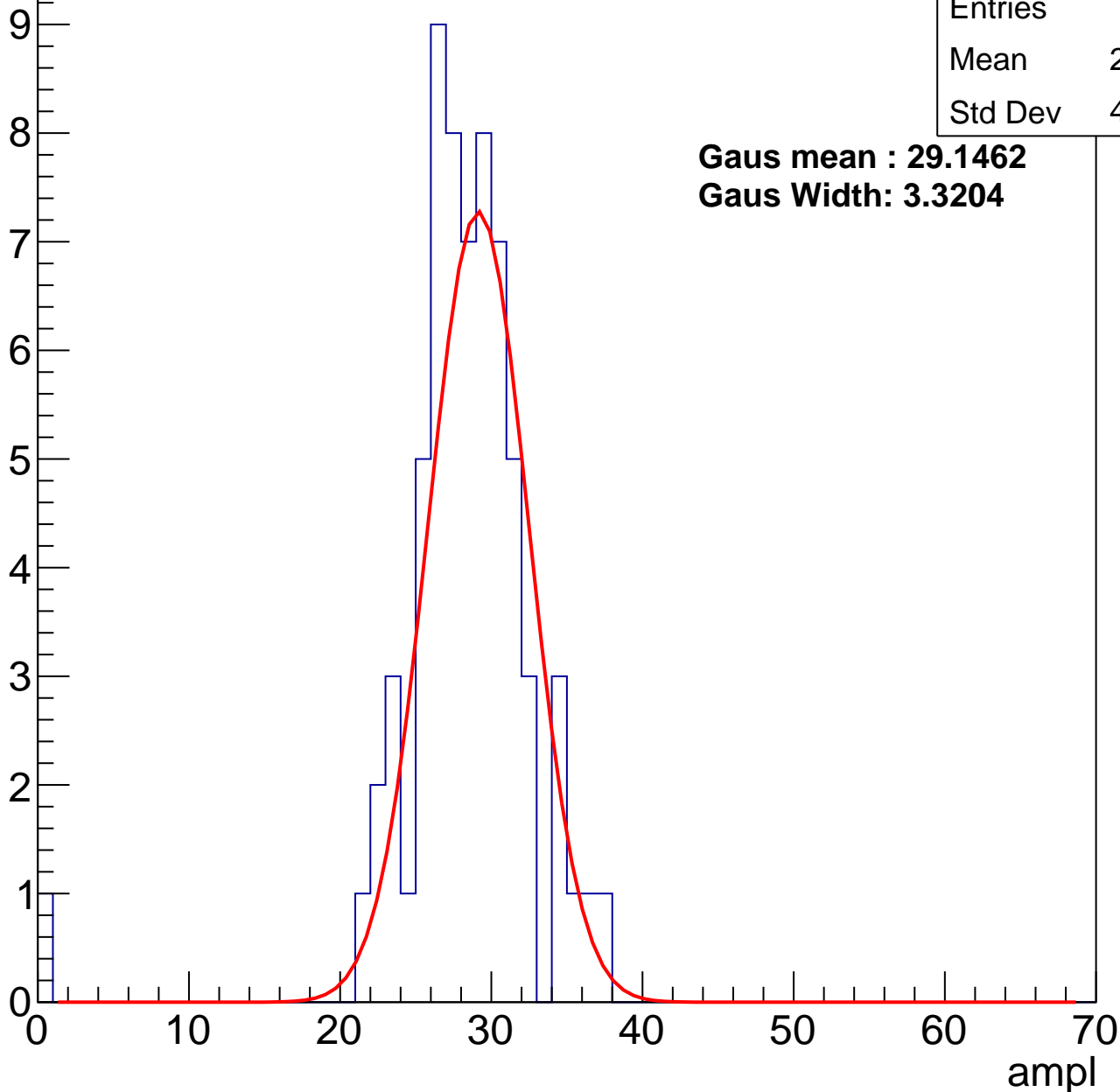
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	27.76
Std Dev	4.787

**Gaus mean : 29.1462**

**Gaus Width: 3.3204**



# B1L101S, U9-ch55, adc1

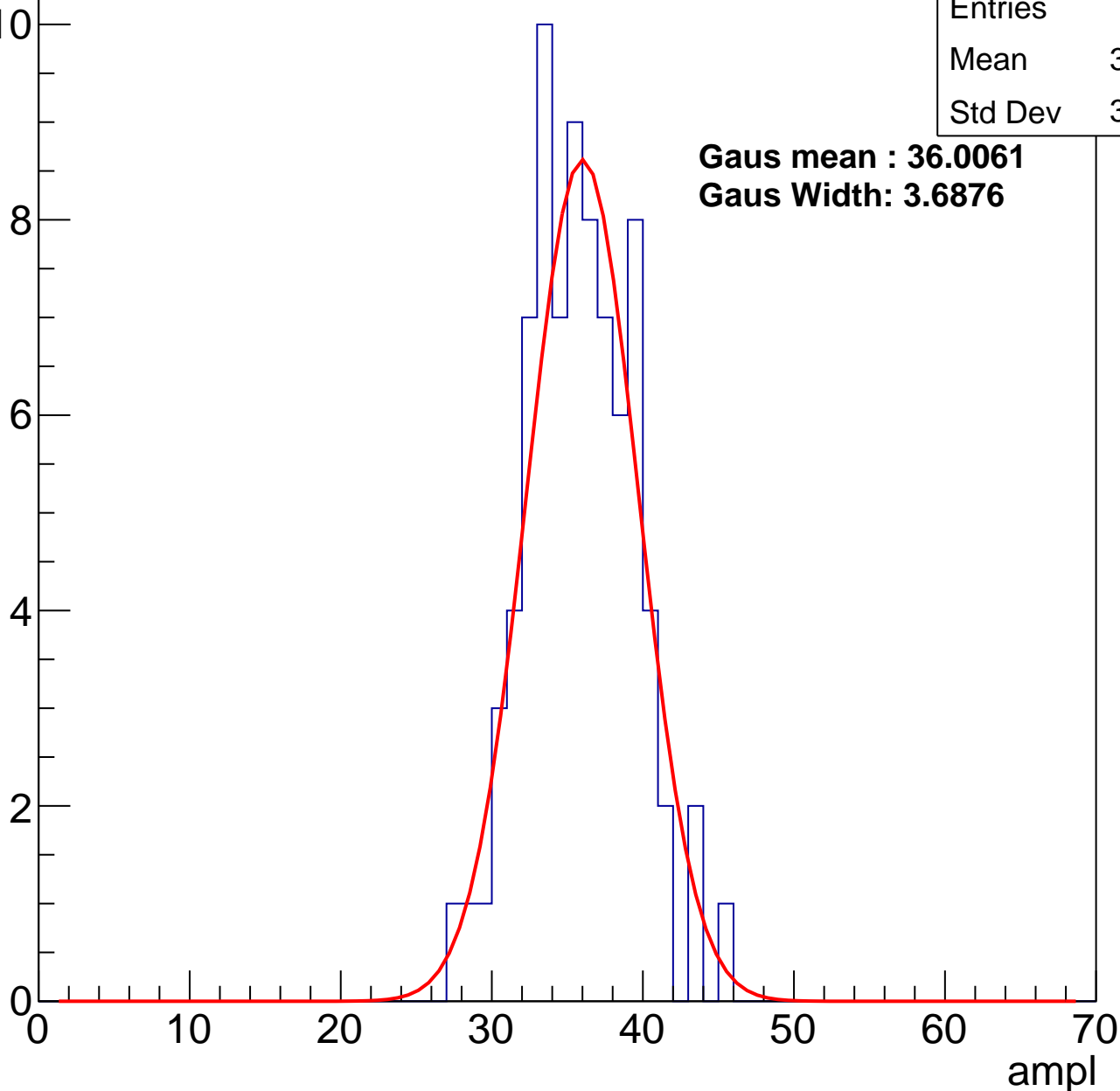
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	35.37
Std Dev	3.522

**Gaus mean : 36.0061**

**Gaus Width: 3.6876**



# B1L101S, U9-ch55, adc2

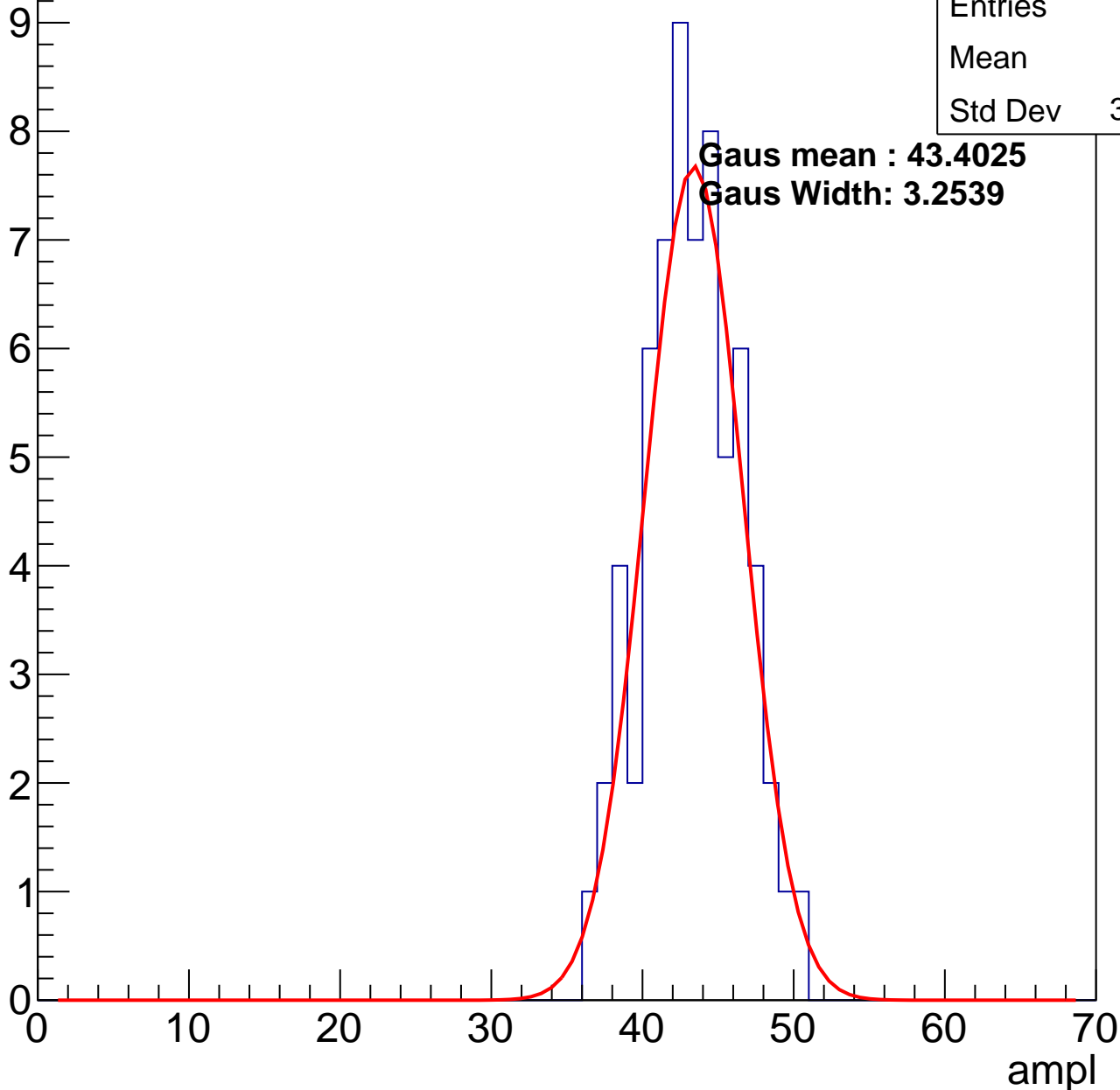
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	42.8
Std Dev	3.094

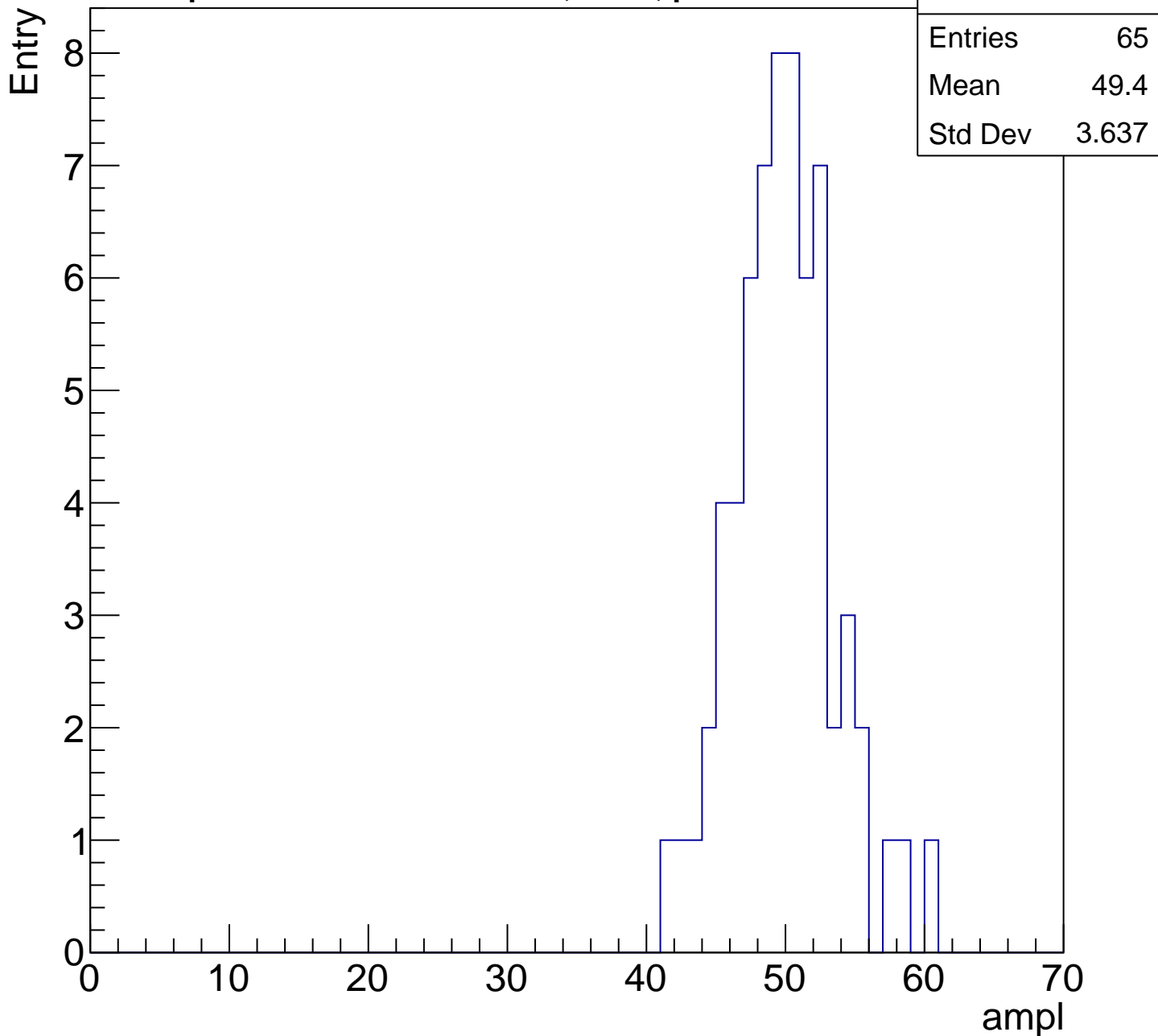
**Gaus mean : 43.4025**

**Gaus Width: 3.2539**



# B1L101S, U9-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

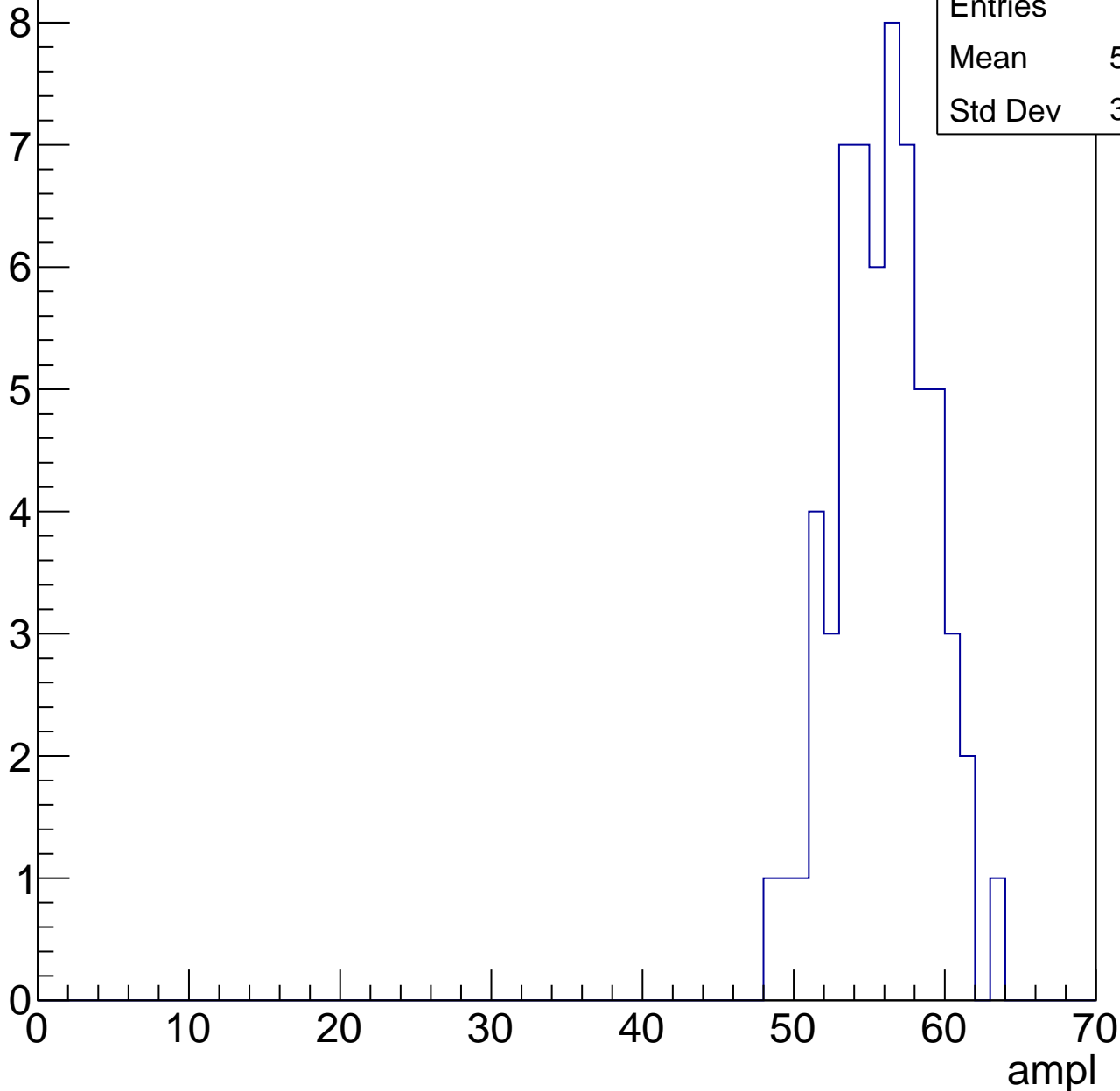


# B1L101S, U9-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	55.46
Std Dev	3.124

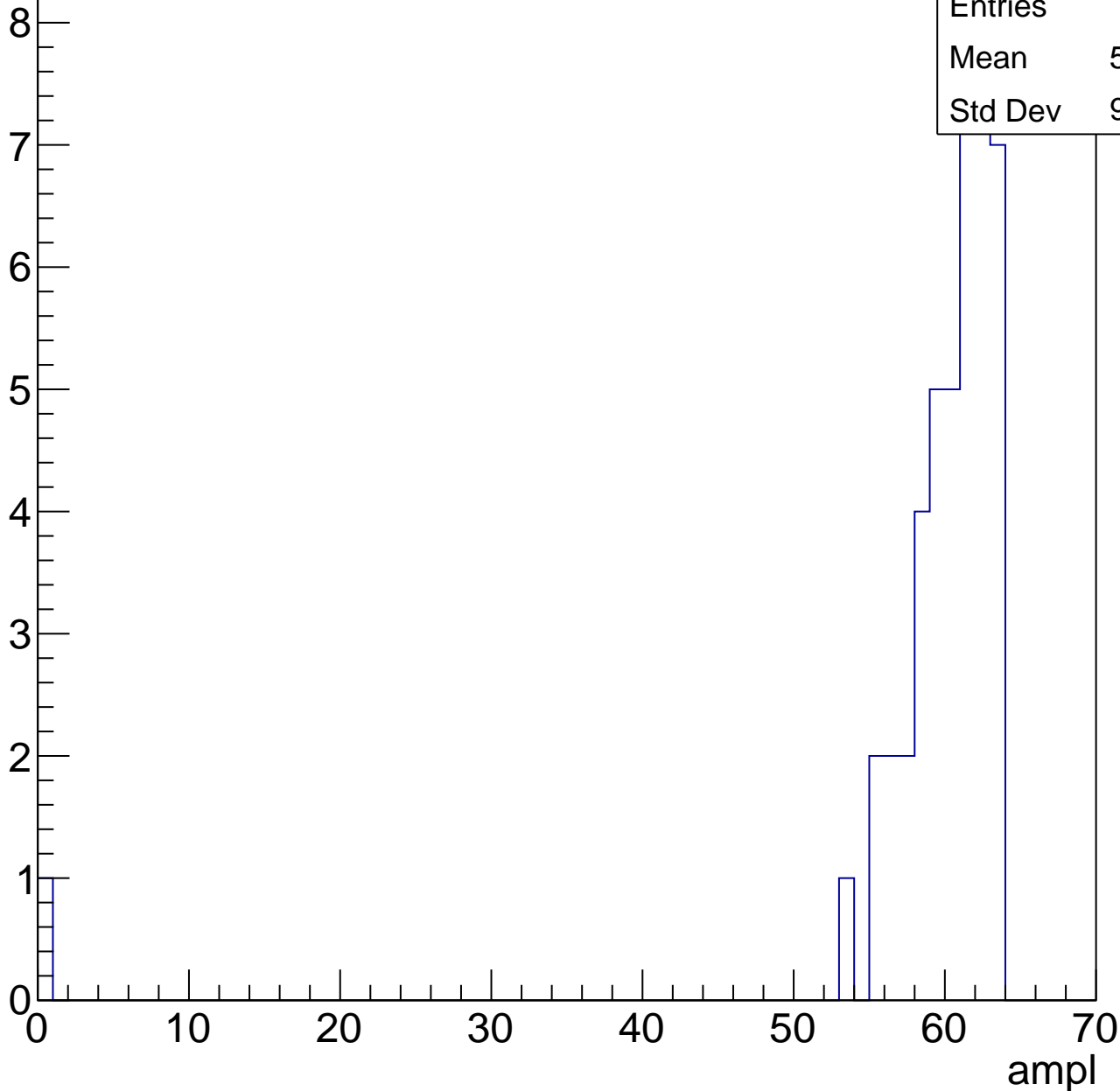


# B1L101S, U9-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	58.69
Std Dev	9.184



# B1L101S, U9-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U9-ch56, adc0

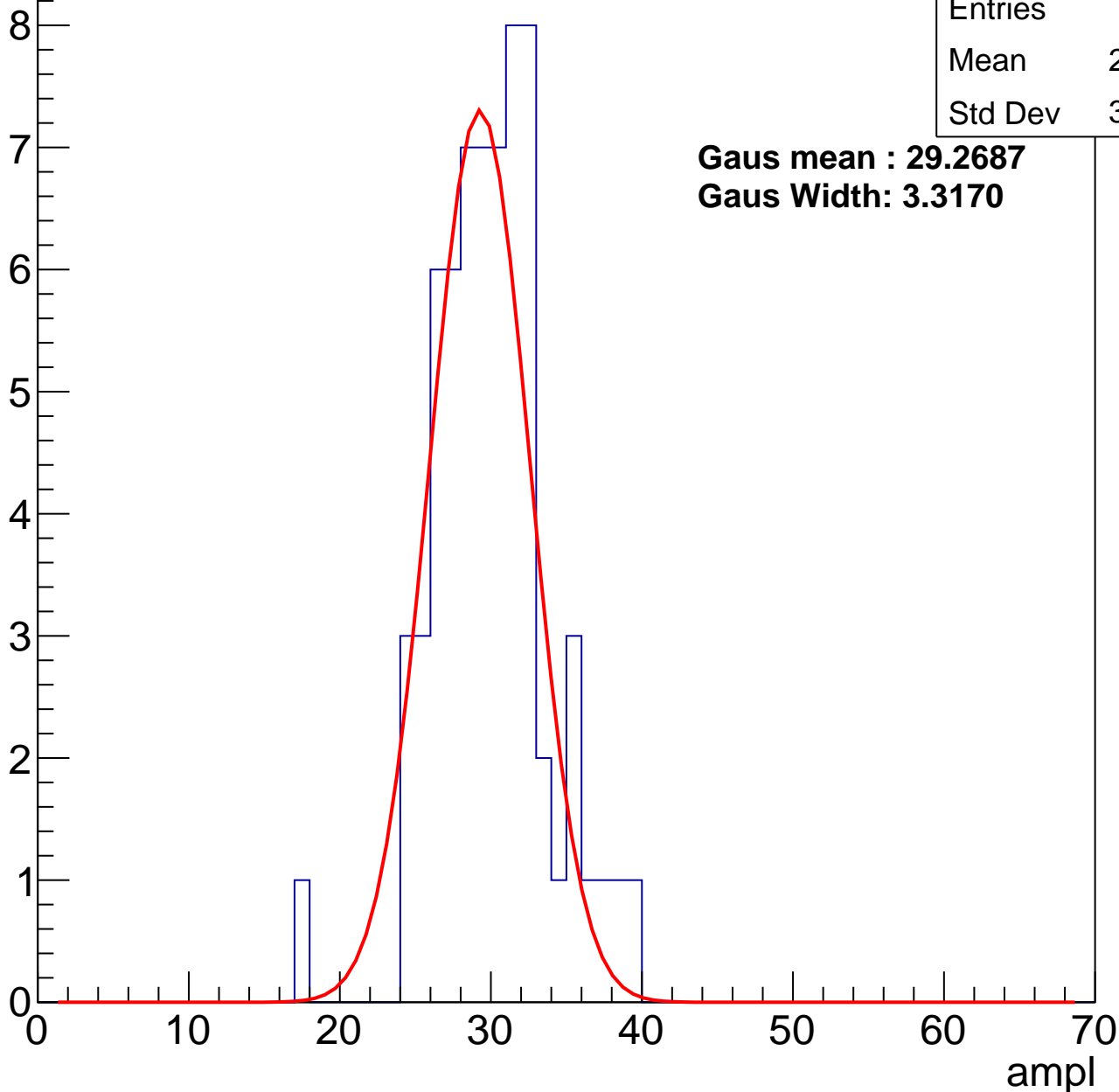
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	29.55
Std Dev	3.698

**Gaus mean : 29.2687**

**Gaus Width: 3.3170**



# B1L101S, U9-ch56, adc1

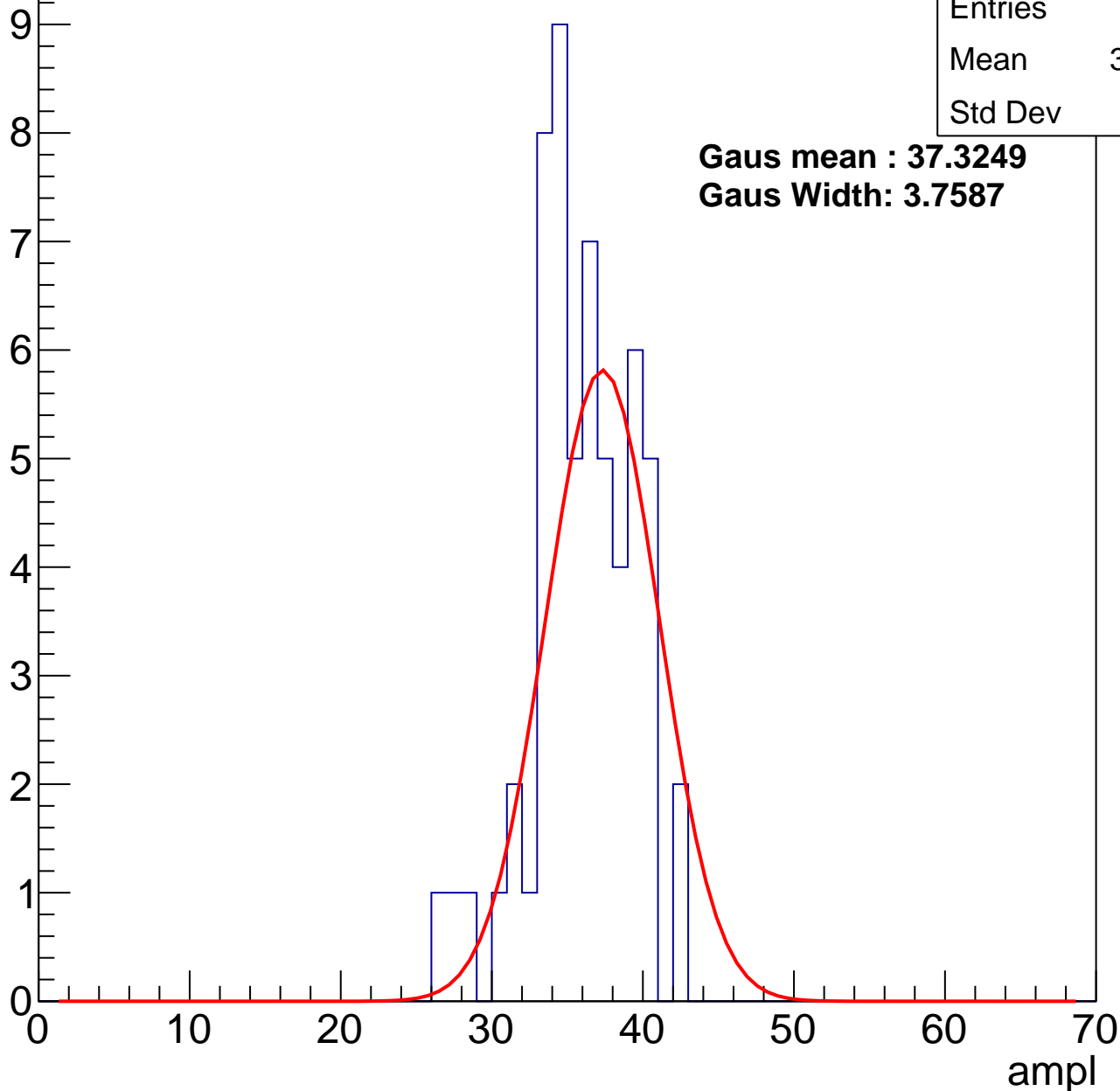
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	35.47
Std Dev	3.4

**Gaus mean : 37.3249**

**Gaus Width: 3.7587**



# B1L101S, U9-ch56, adc2

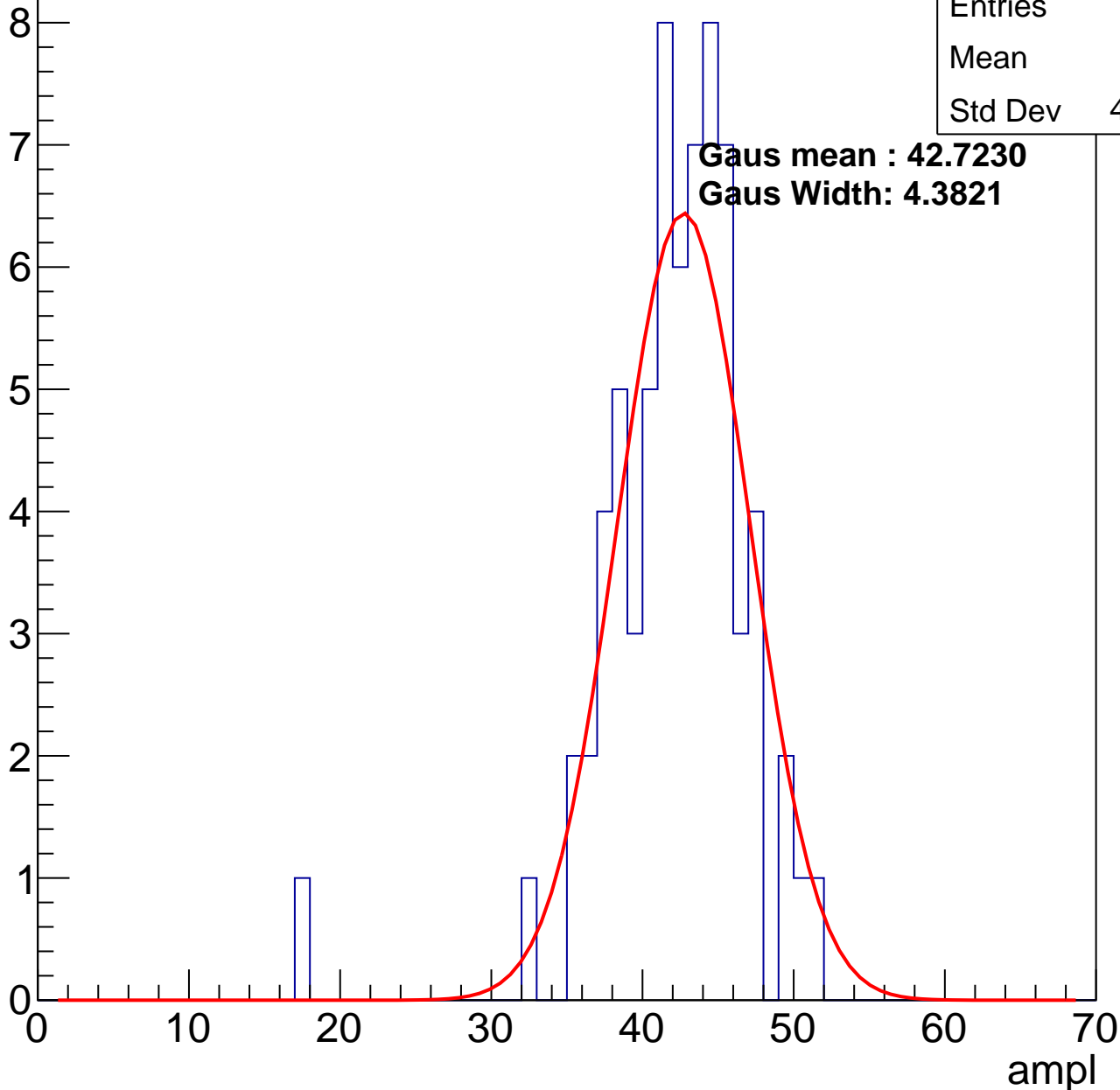
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	41.7
Std Dev	4.806

**Gaus mean : 42.7230**

**Gaus Width: 4.3821**



# B1L101S, U9-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

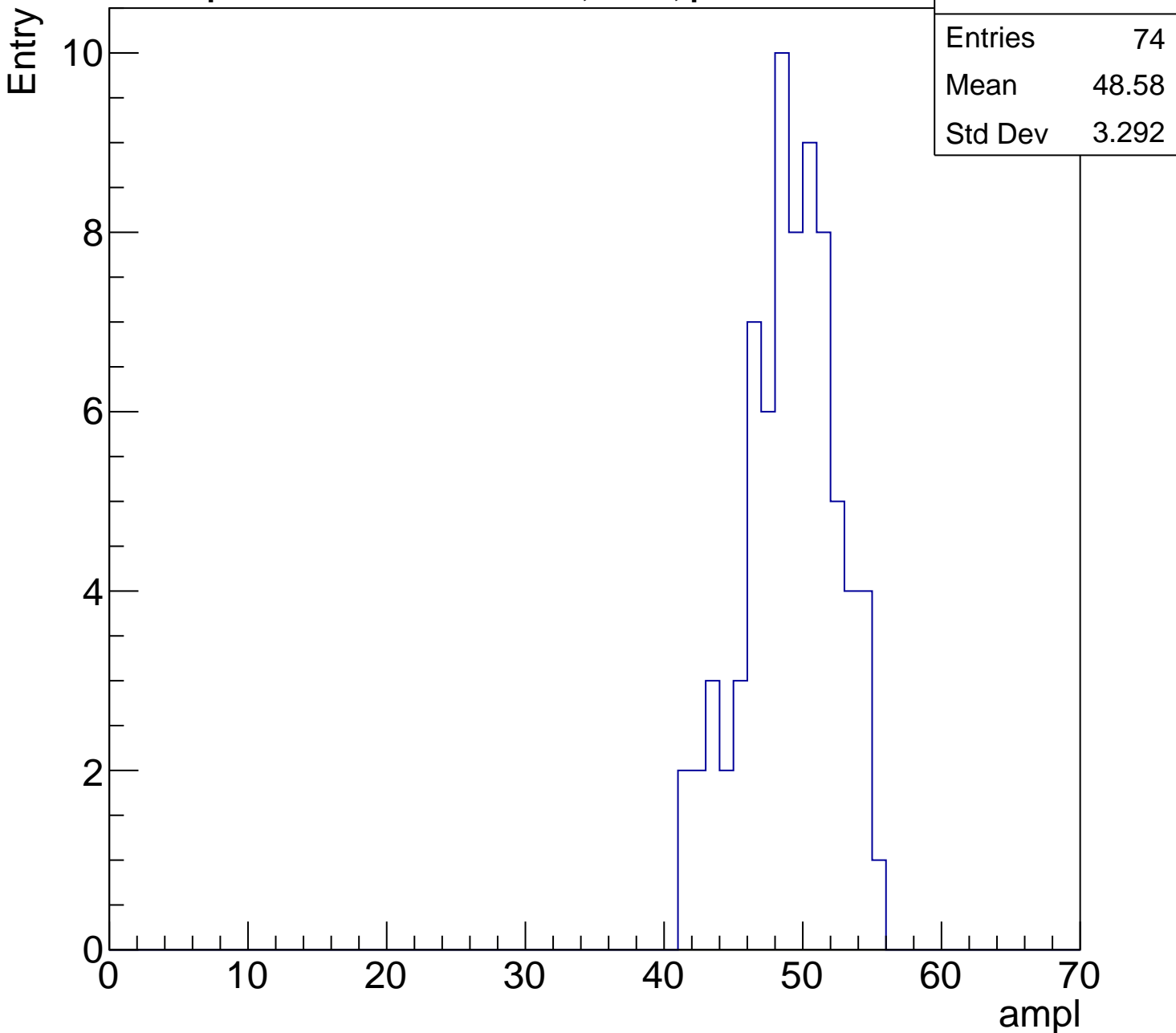
Entries	74
Mean	48.58
Std Dev	3.292

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

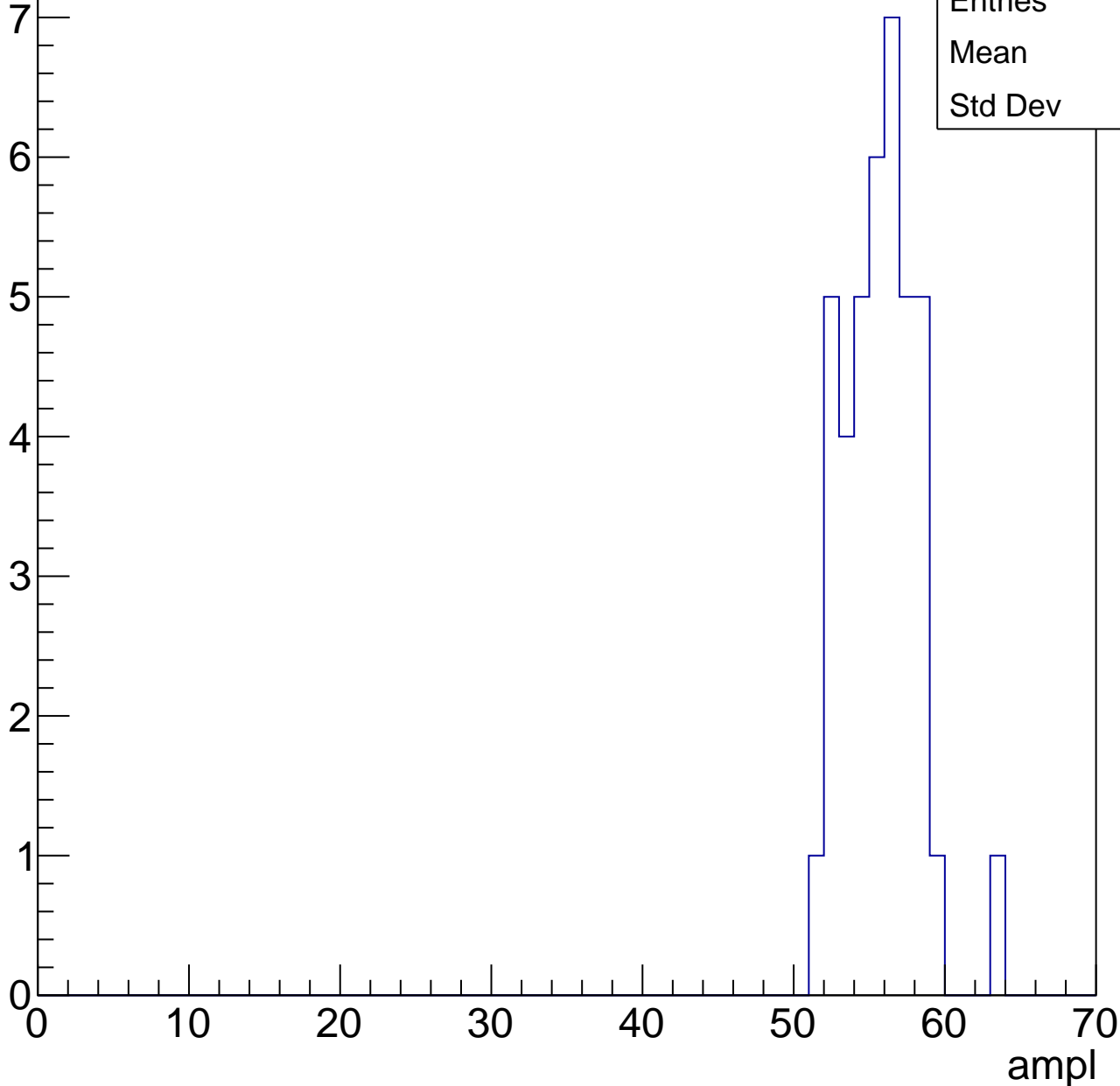


# B1L101S, U9-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	40
Mean	55.3
Std Dev	2.4

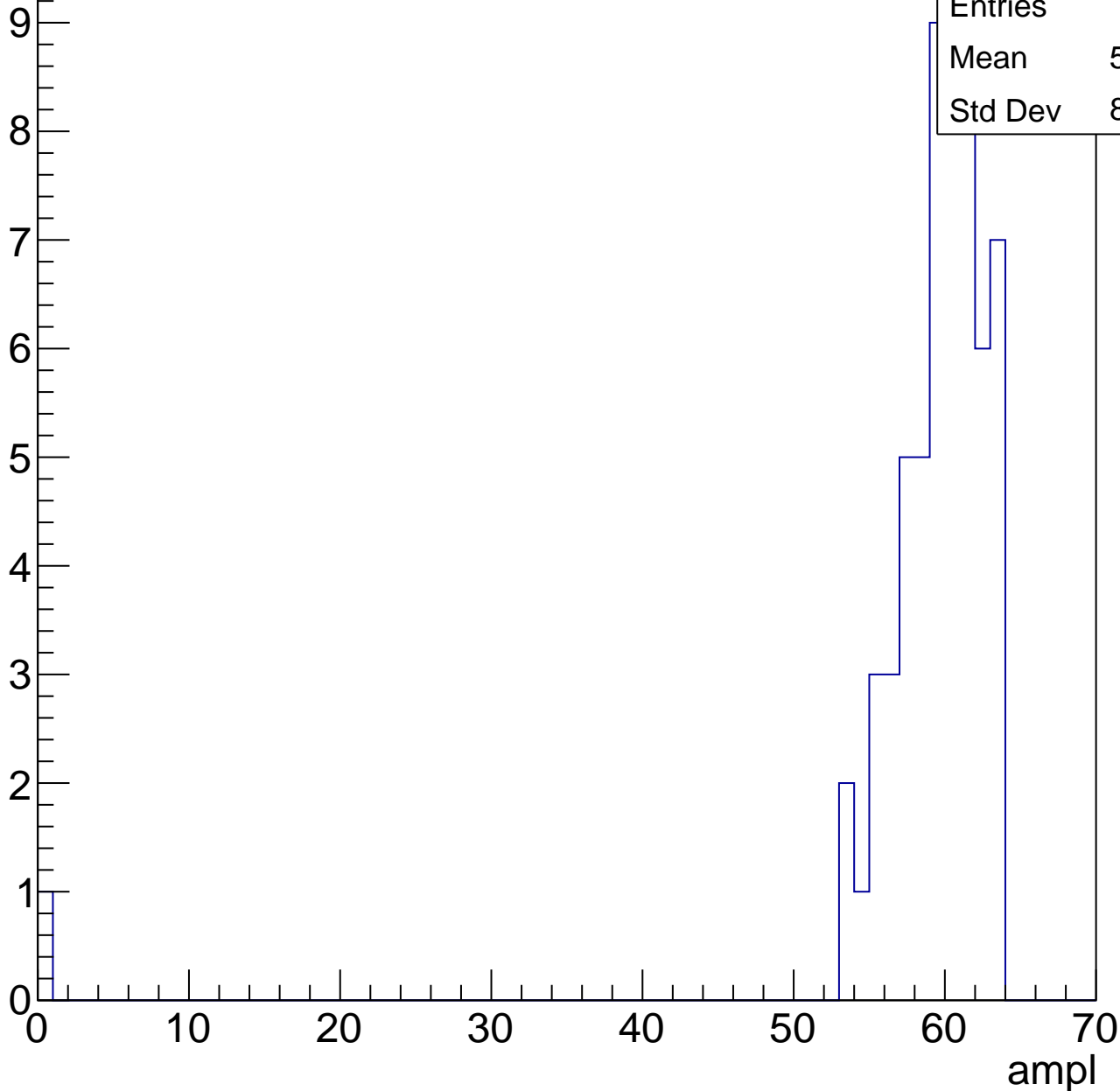


# B1L101S, U9-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

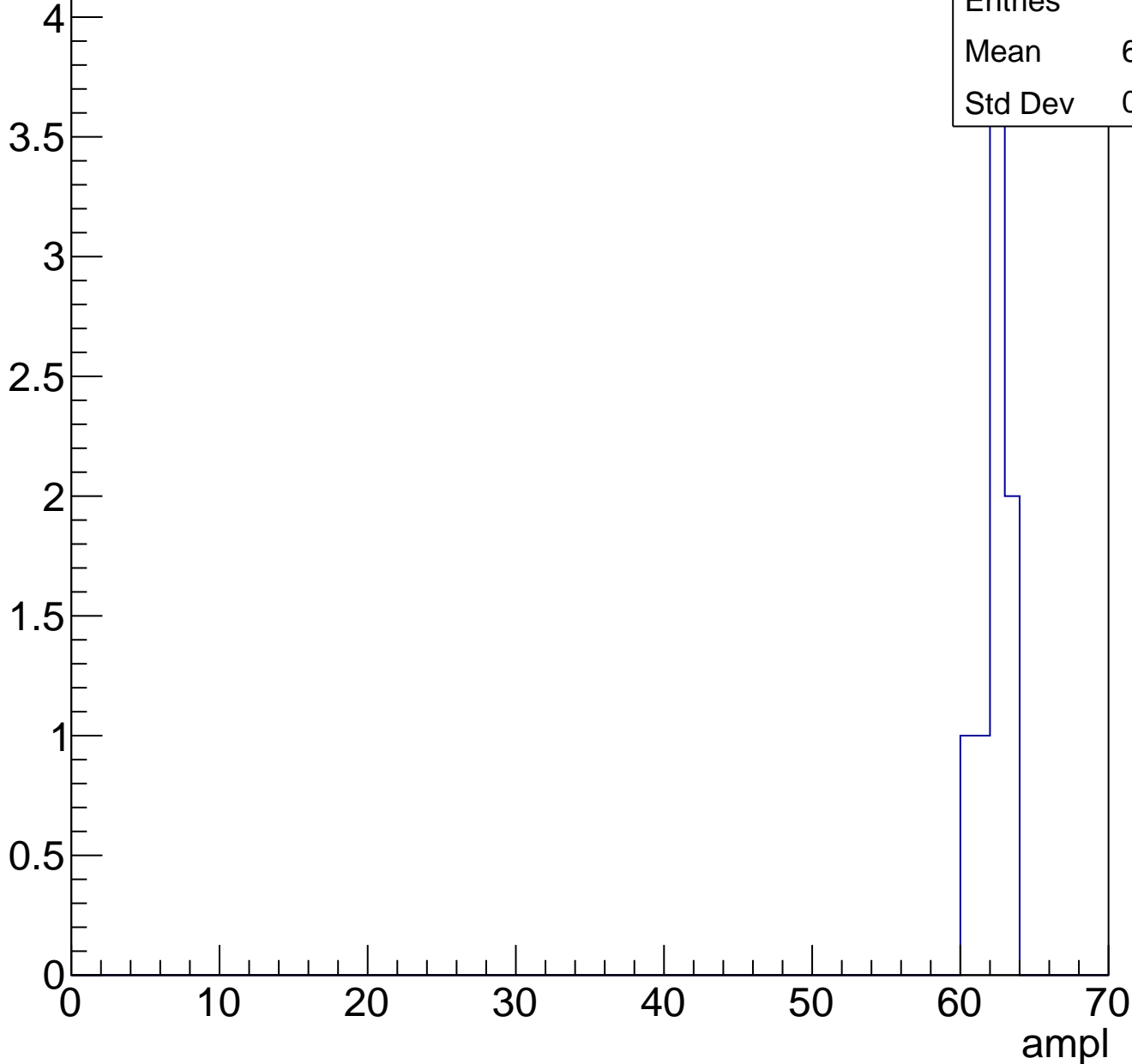
Entries	60
Mean	58.35
Std Dev	8.025



# B1L101S, U9-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	20
Std Dev	0

# B1L101S, U9-ch57, adc0

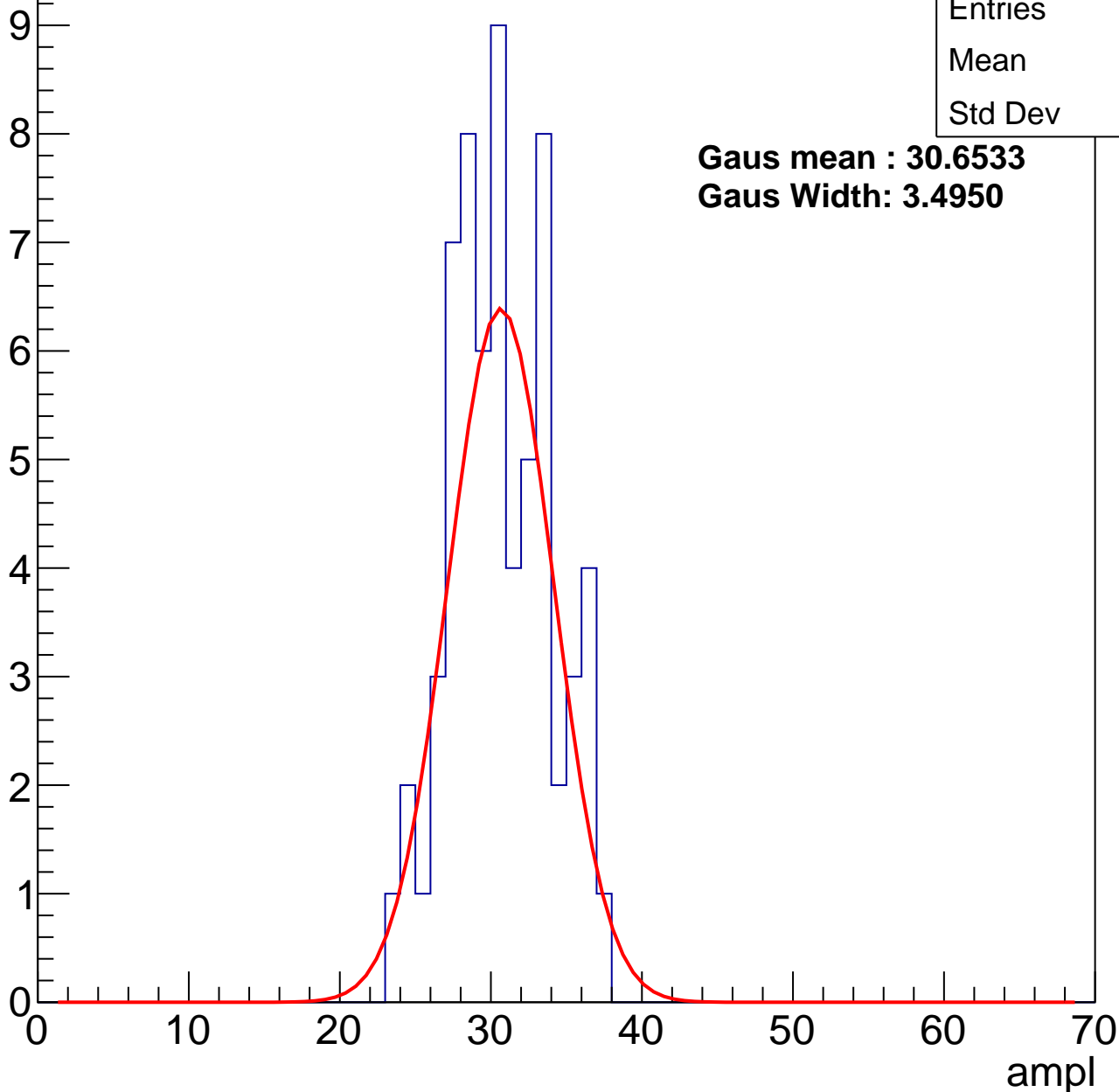
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	30.2
Std Dev	3.28

**Gaus mean : 30.6533**

**Gaus Width: 3.4950**



# B1L101S, U9-ch57, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	84
Mean	37.58
Std Dev	3.837

**Gaus mean : 38.0989**

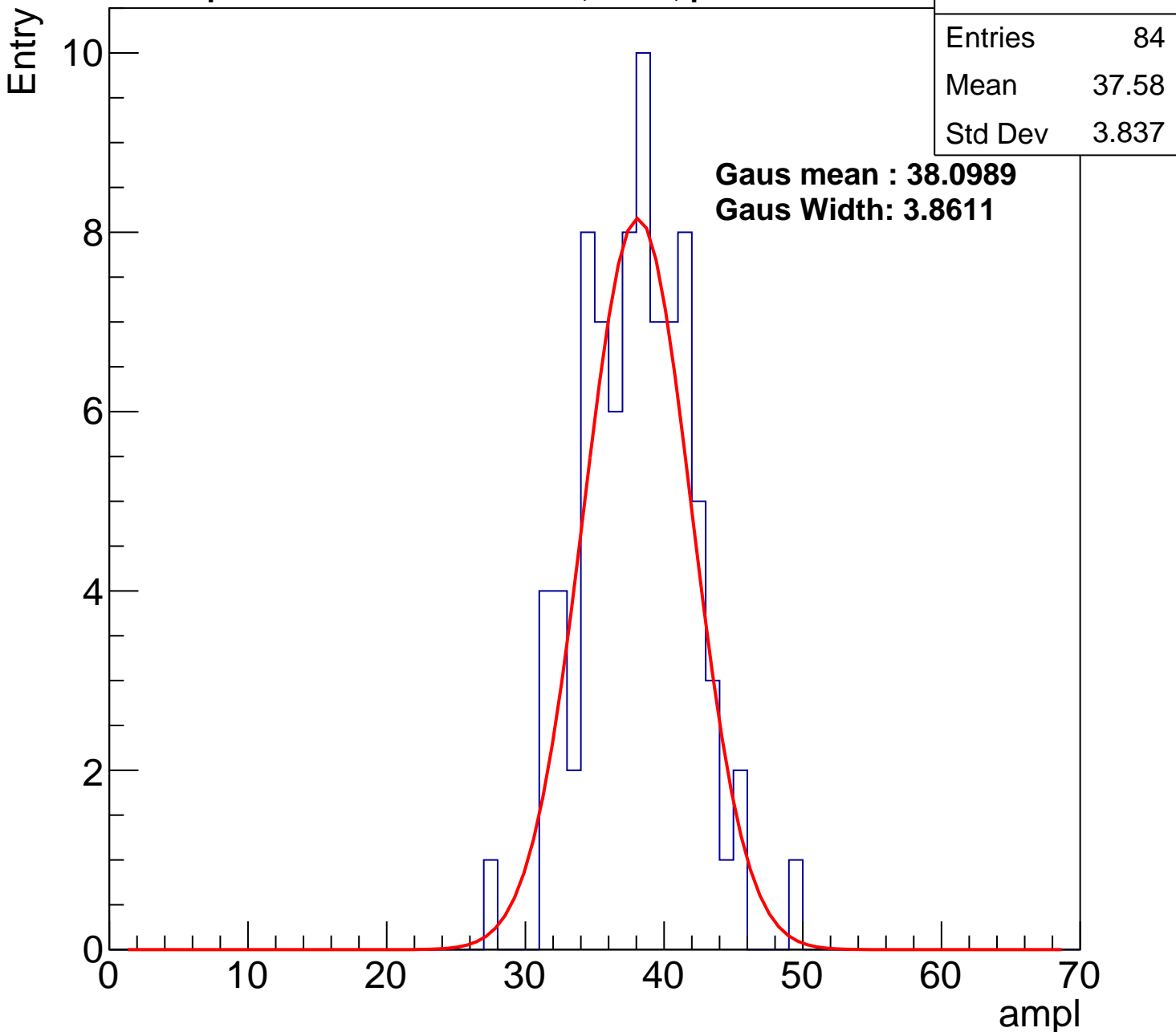
**Gaus Width: 3.8611**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U9-ch57, adc2

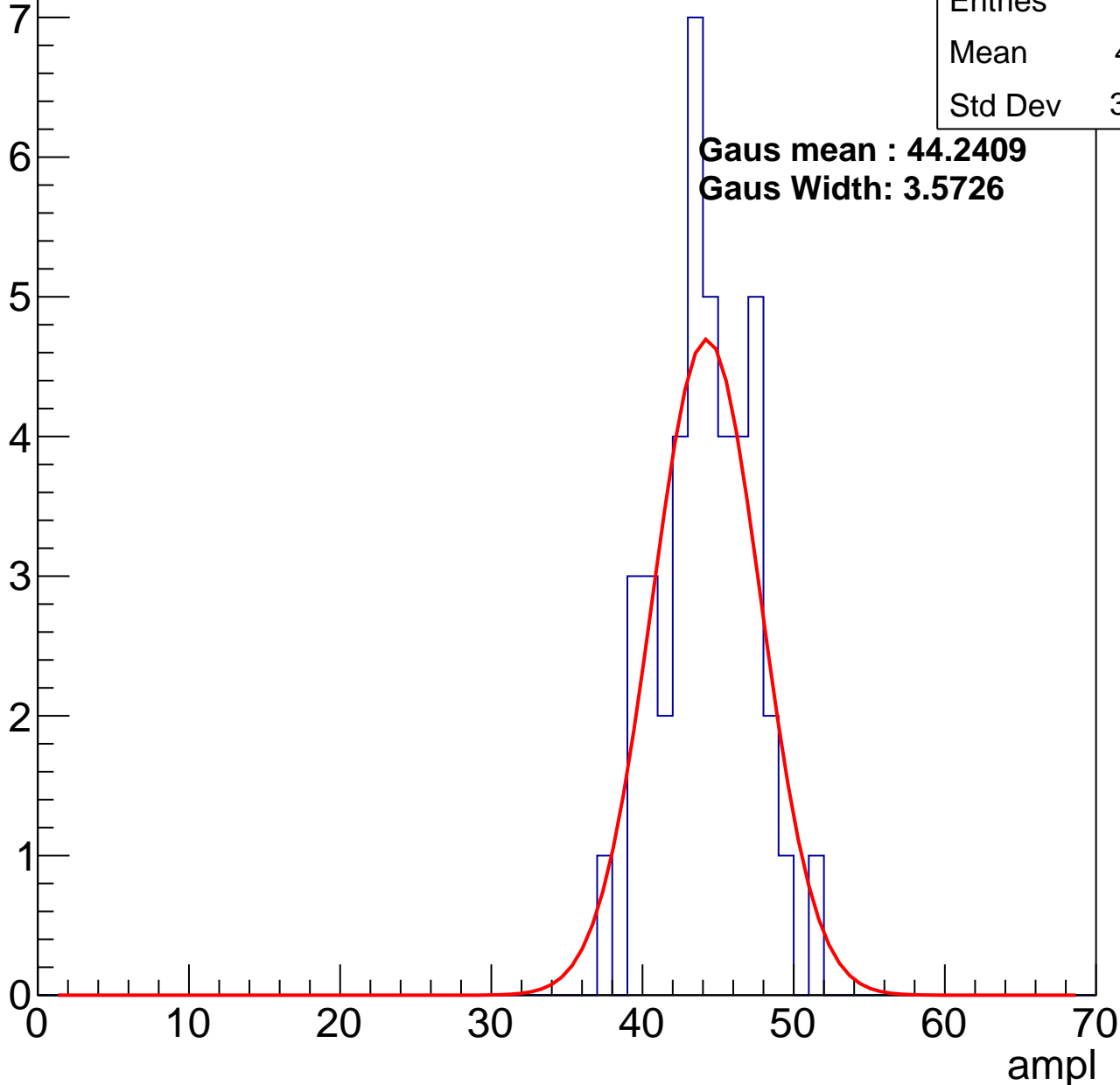
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	43.81
Std Dev	3.018

**Gaus mean : 44.2409**

**Gaus Width: 3.5726**



# B1L101S, U9-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

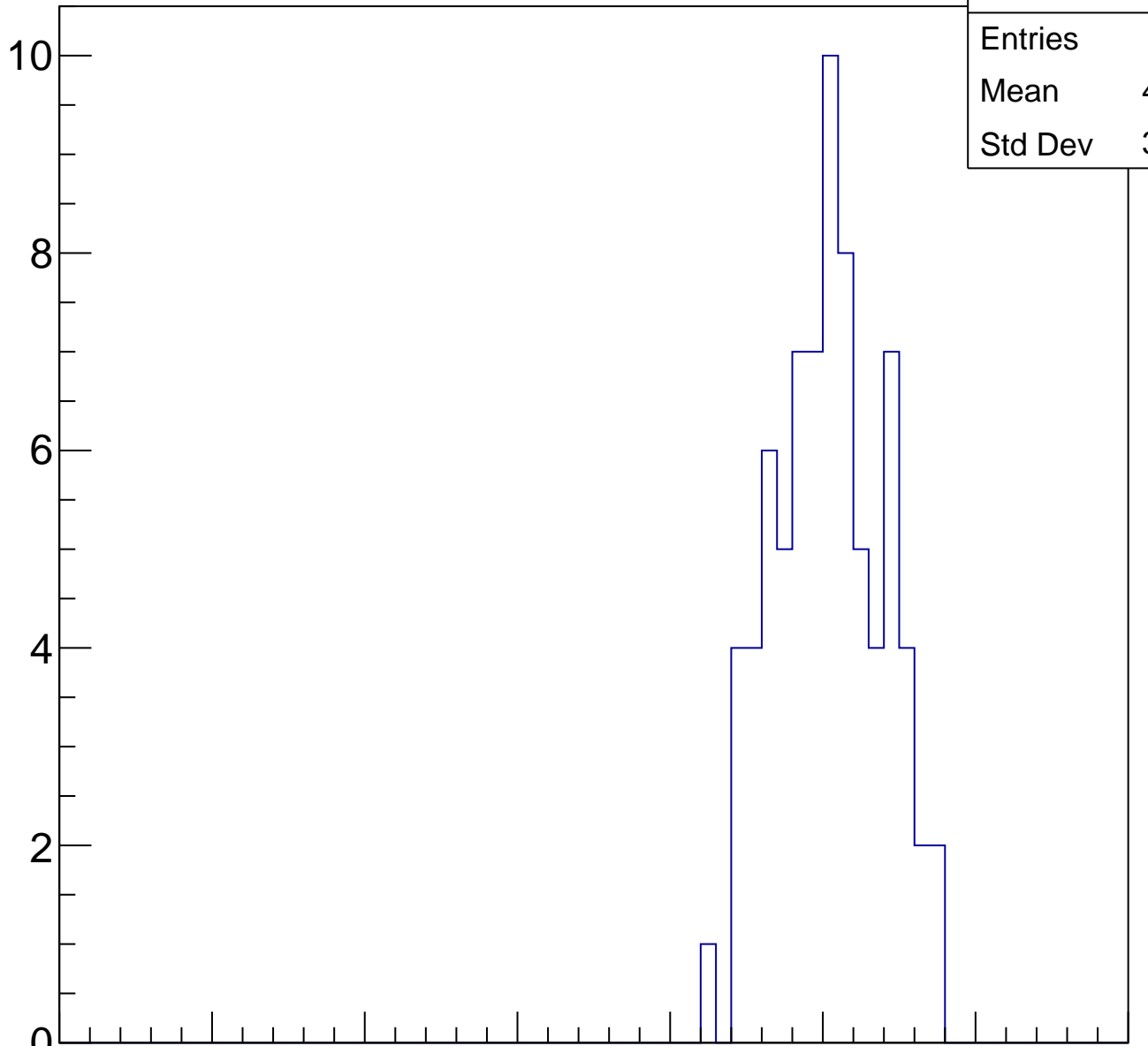
Entries	76
Mean	49.89
Std Dev	3.497

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

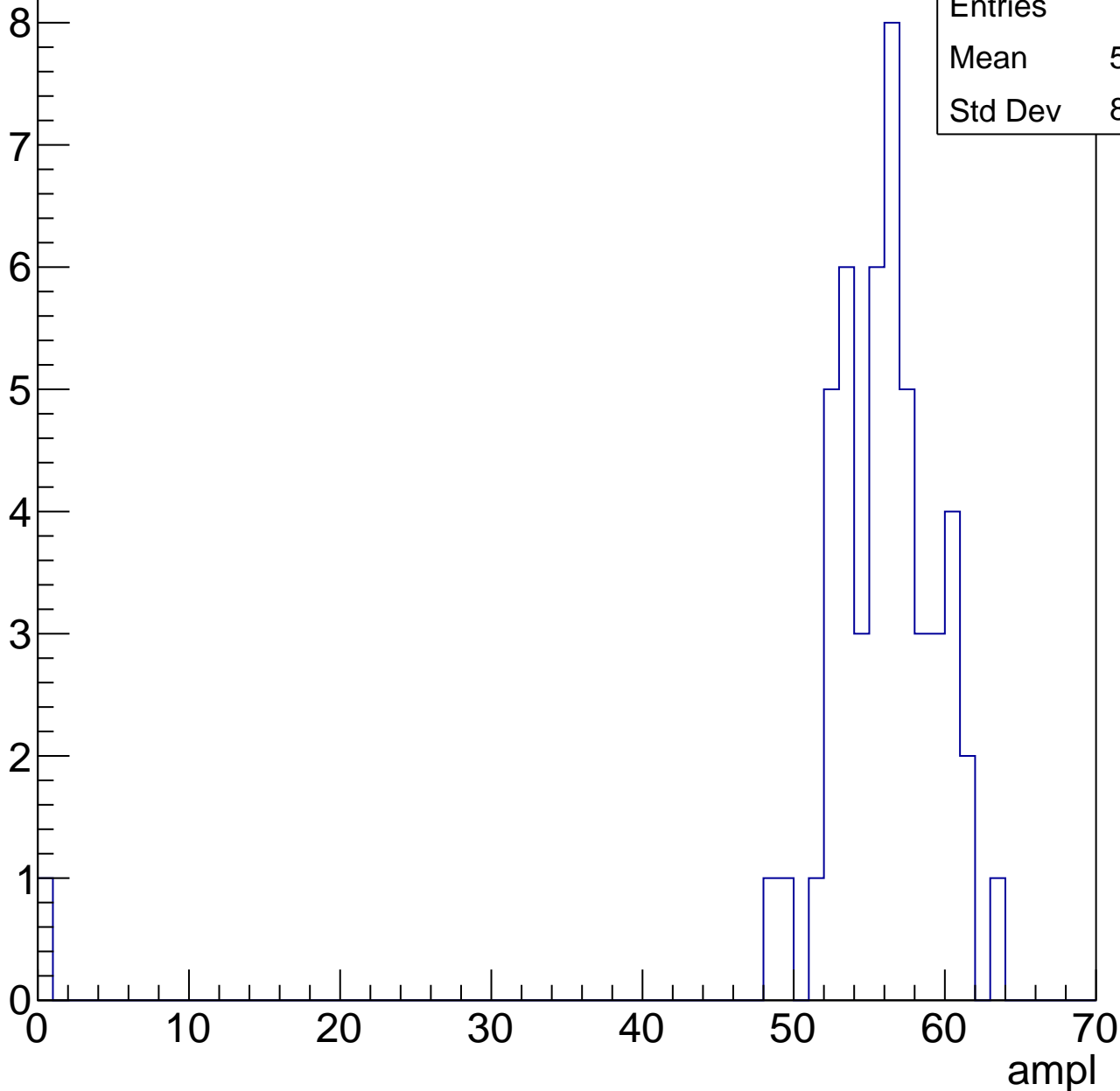


# B1L101S, U9-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

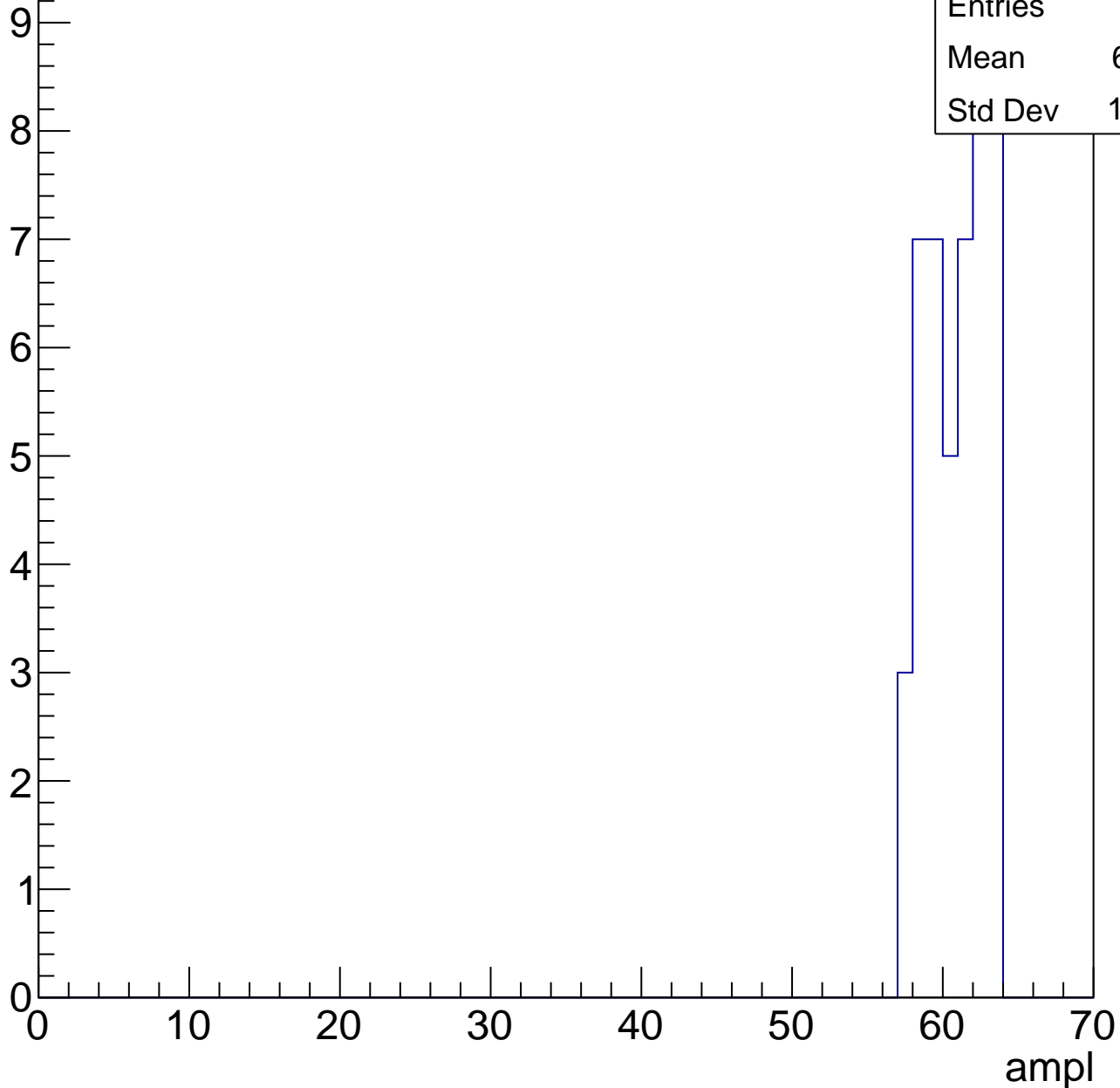
Entries	50
Mean	54.54
Std Dev	8.398



# B1L101S, U9-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	46
Mean	60.41
Std Dev	1.918

# B1L101S, U9-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U9-ch58, adc0

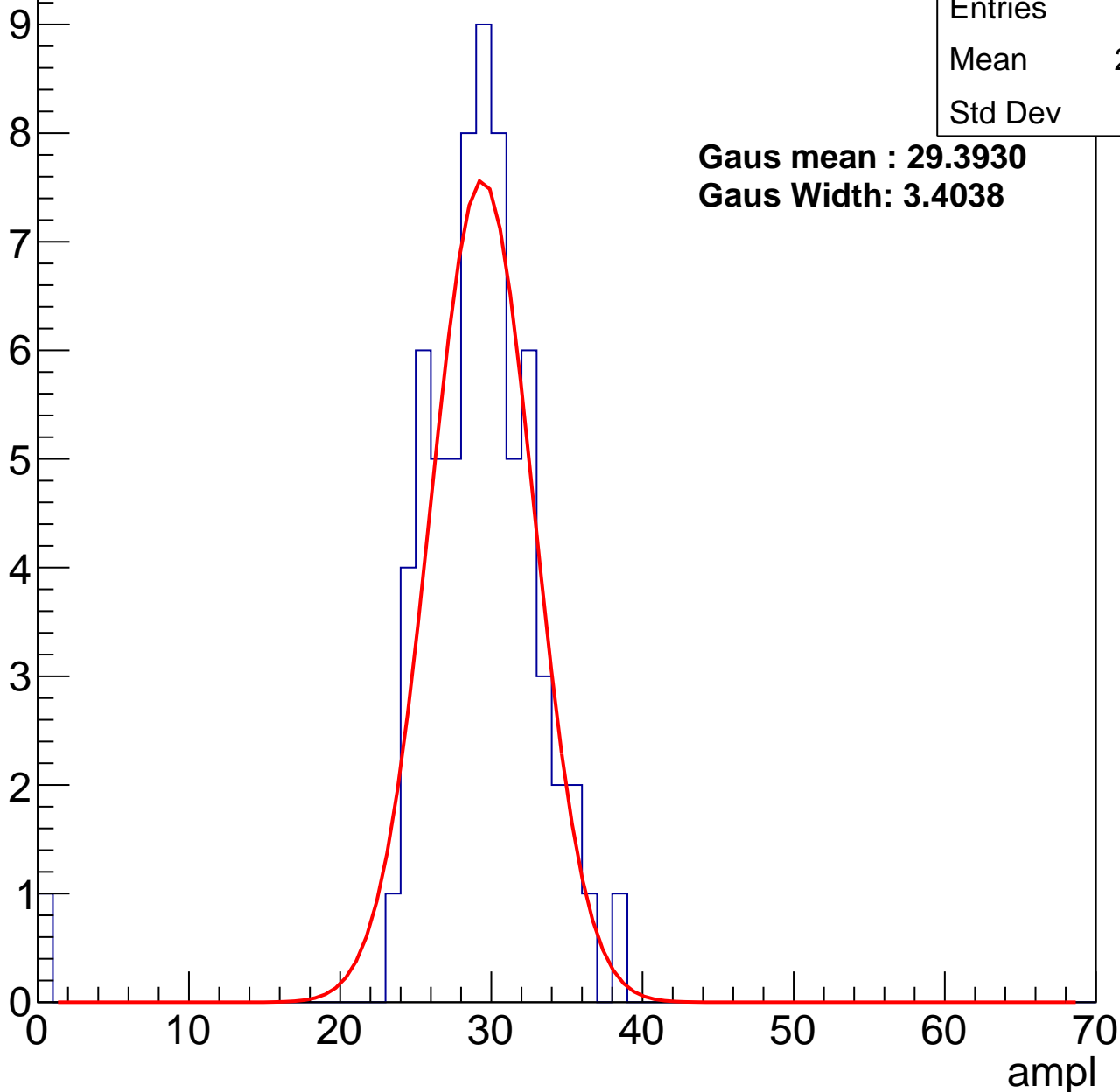
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	28.61
Std Dev	4.76

**Gaus mean : 29.3930**

**Gaus Width: 3.4038**



# B1L101S, U9-ch58, adc1

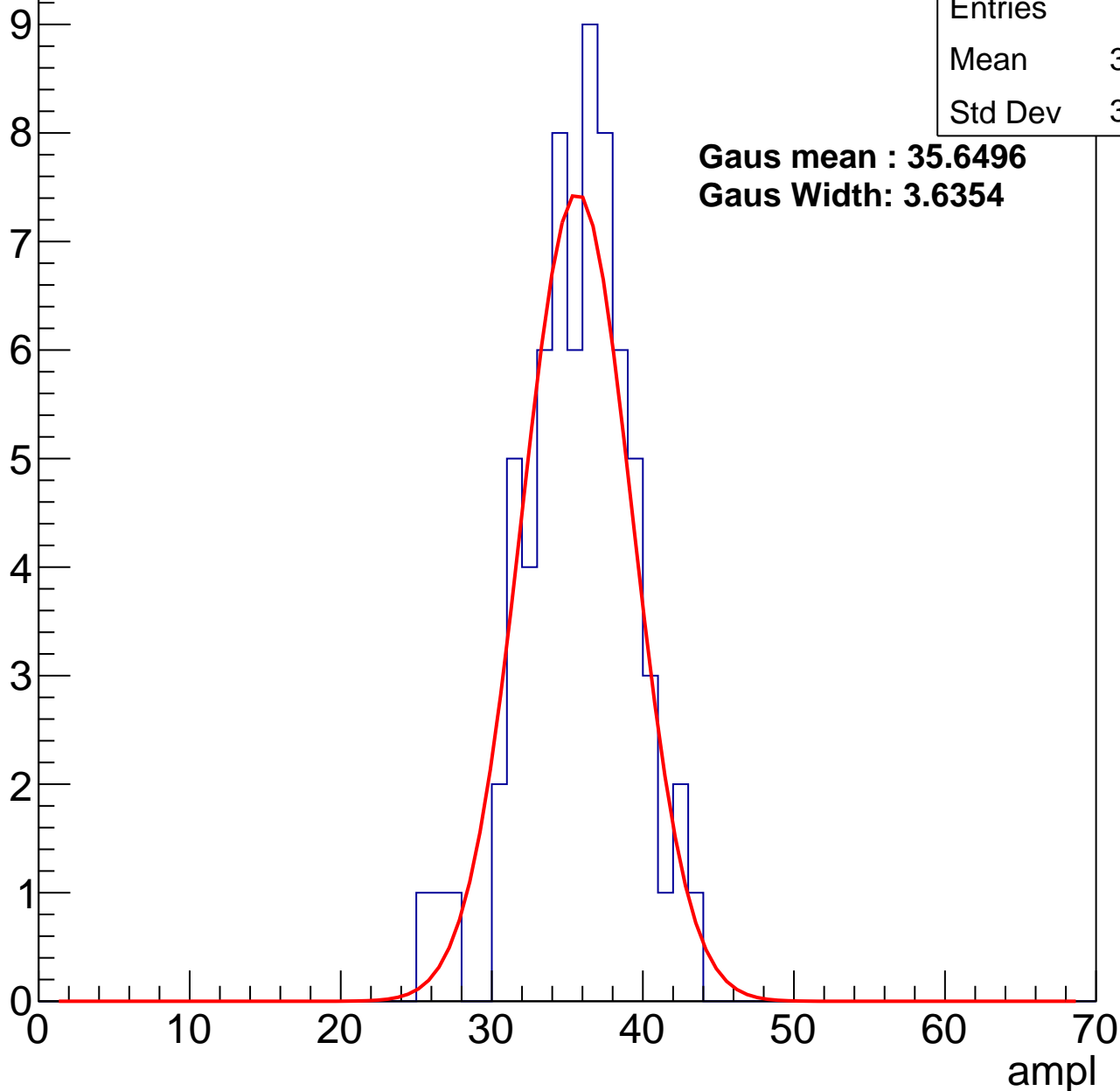
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	35.25
Std Dev	3.585

**Gaus mean : 35.6496**

**Gaus Width: 3.6354**



# B1L101S, U9-ch58, adc2

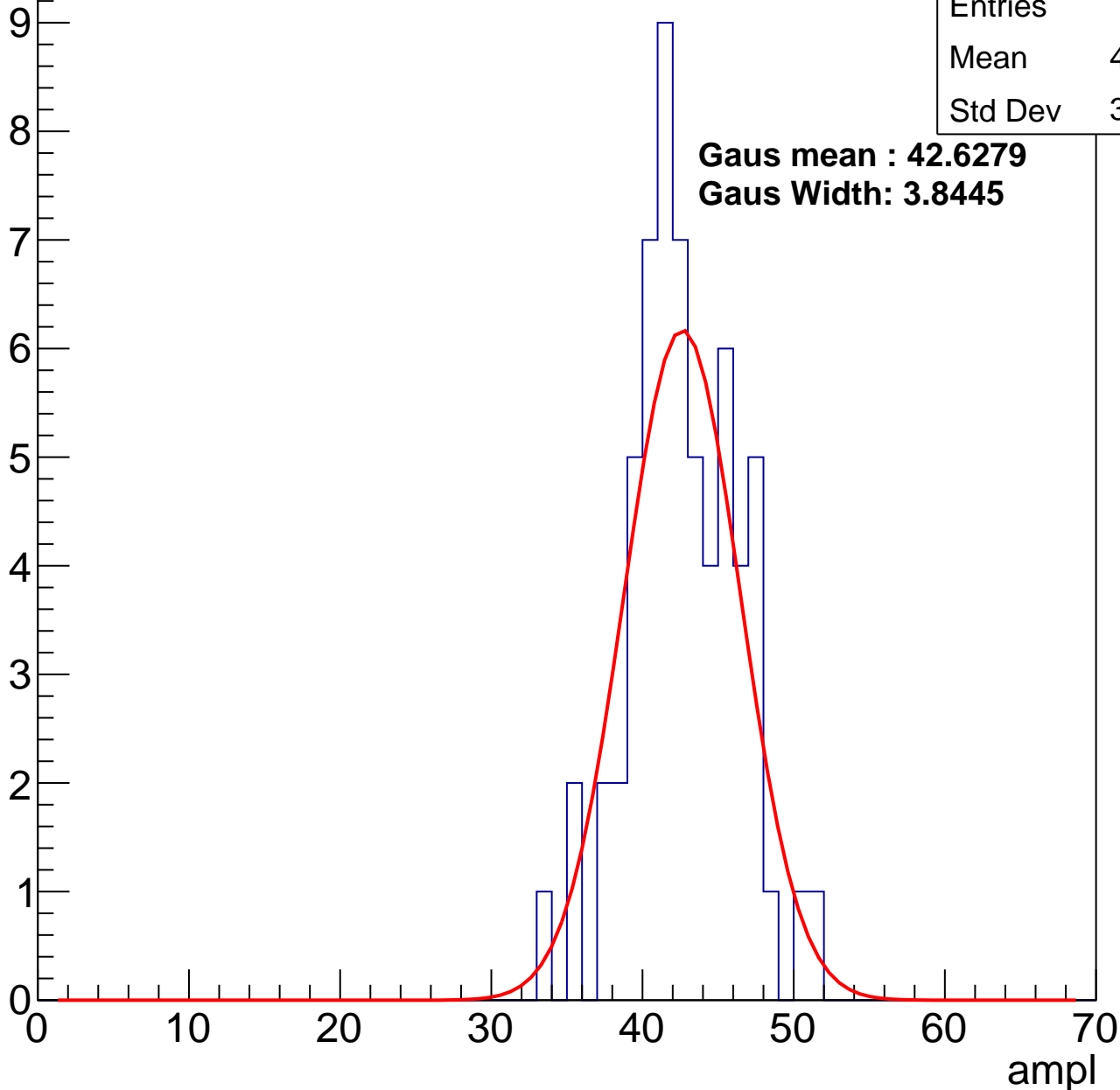
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	42.26
Std Dev	3.556

**Gaus mean : 42.6279**

**Gaus Width: 3.8445**

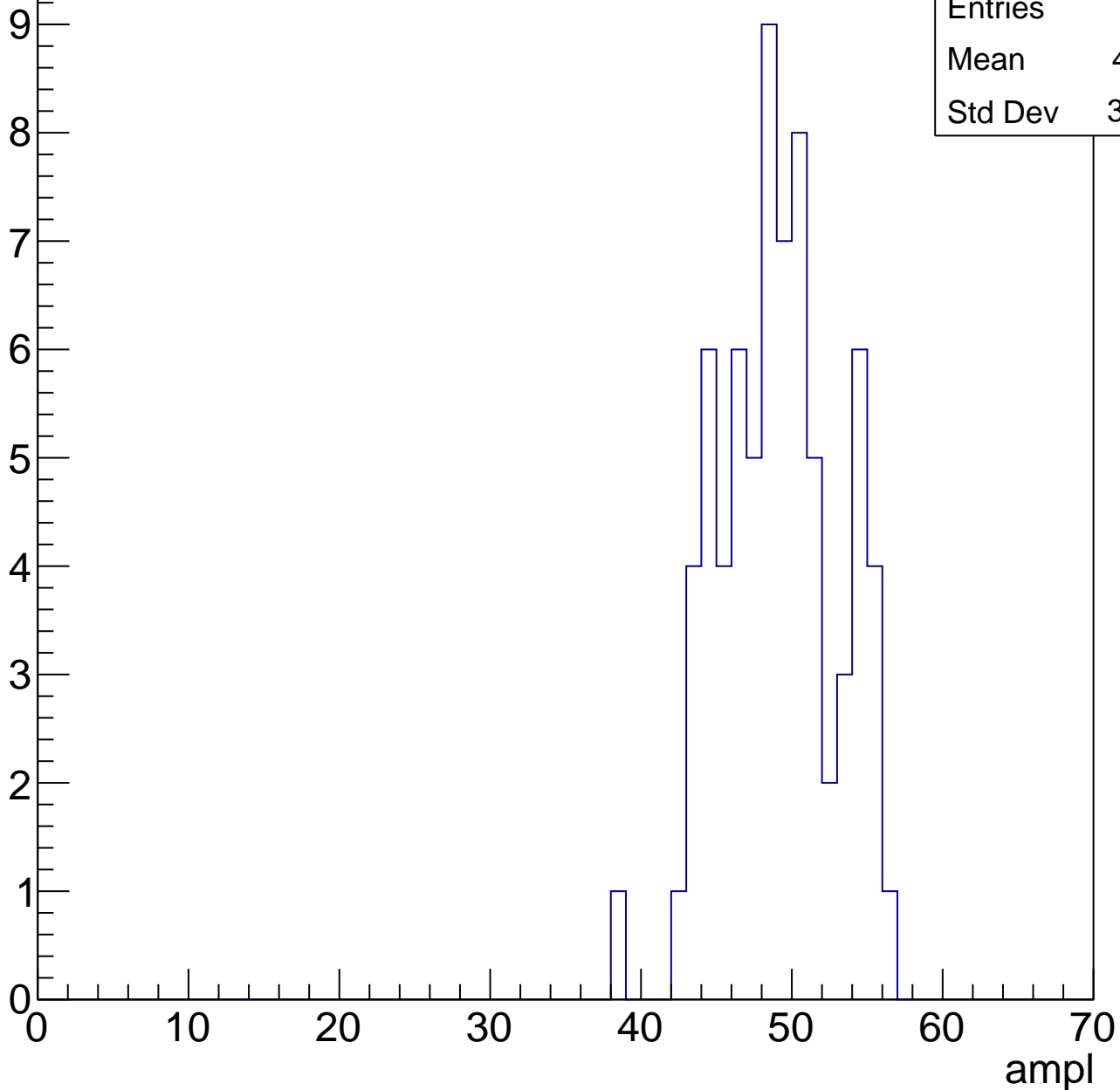


# B1L101S, U9-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	48.61
Std Dev	3.795

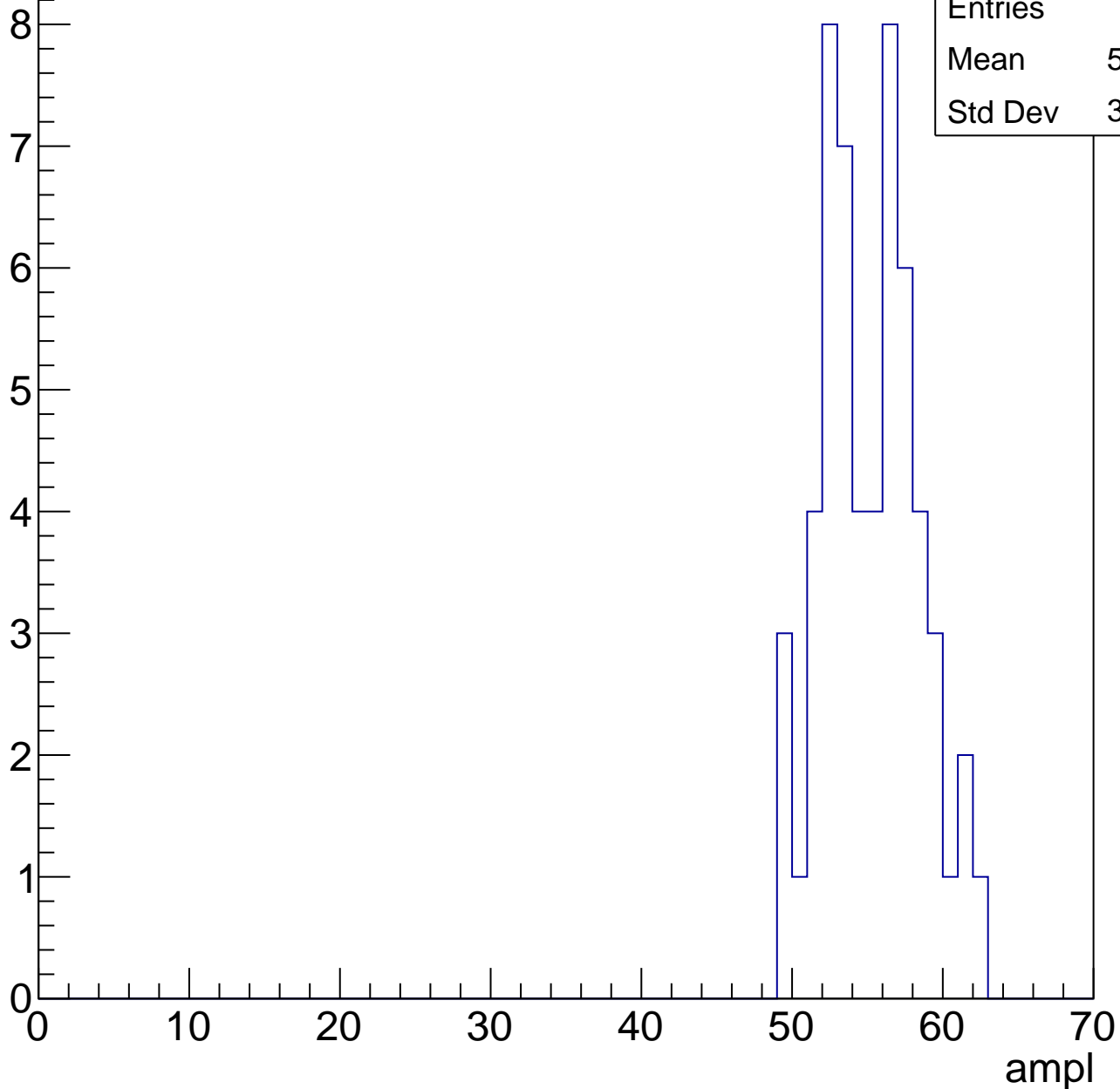


# B1L101S, U9-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	54.77
Std Dev	3.162



# B1L101S, U9-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

Entries 43

Mean 58.4

Std Dev 9.274

ampl

0

10

20

30

40

50

60

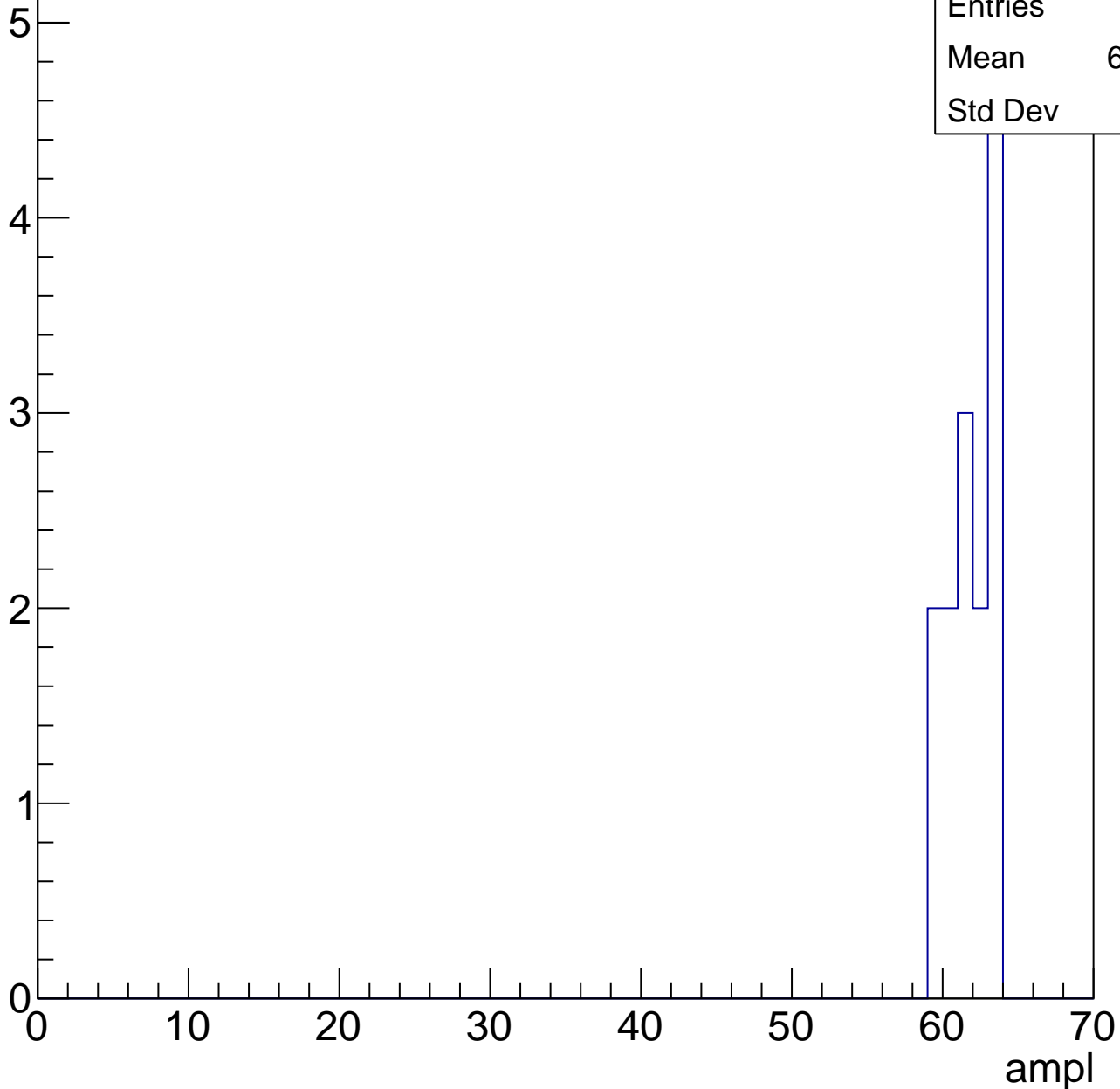
70

# B1L101S, U9-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	14
Mean	61.43
Std Dev	1.45





# B1L101S, U9-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch59, adc0

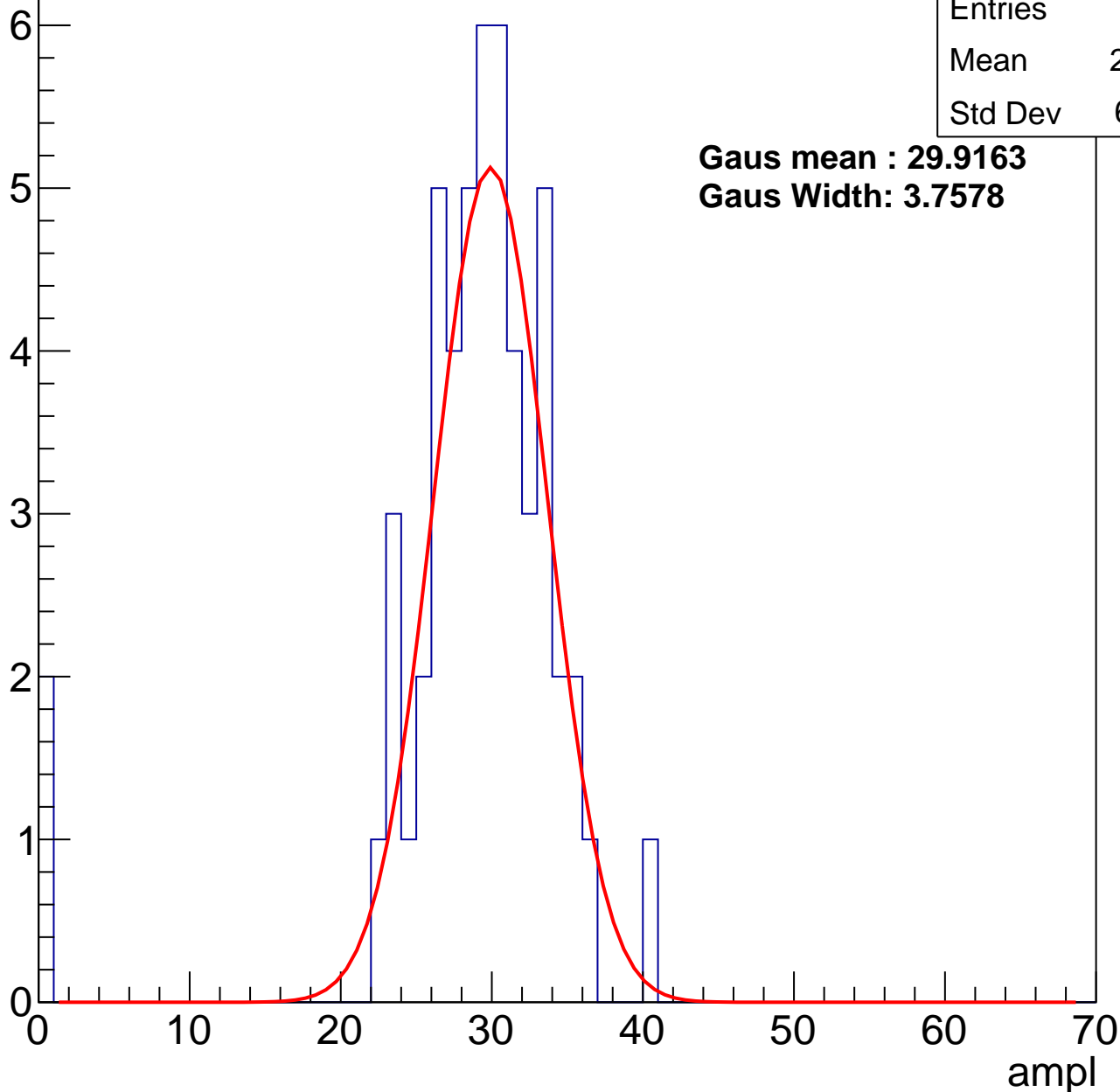
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	28.23
Std Dev	6.661

**Gaus mean : 29.9163**

**Gaus Width: 3.7578**



# B1L101S, U9-ch59, adc1

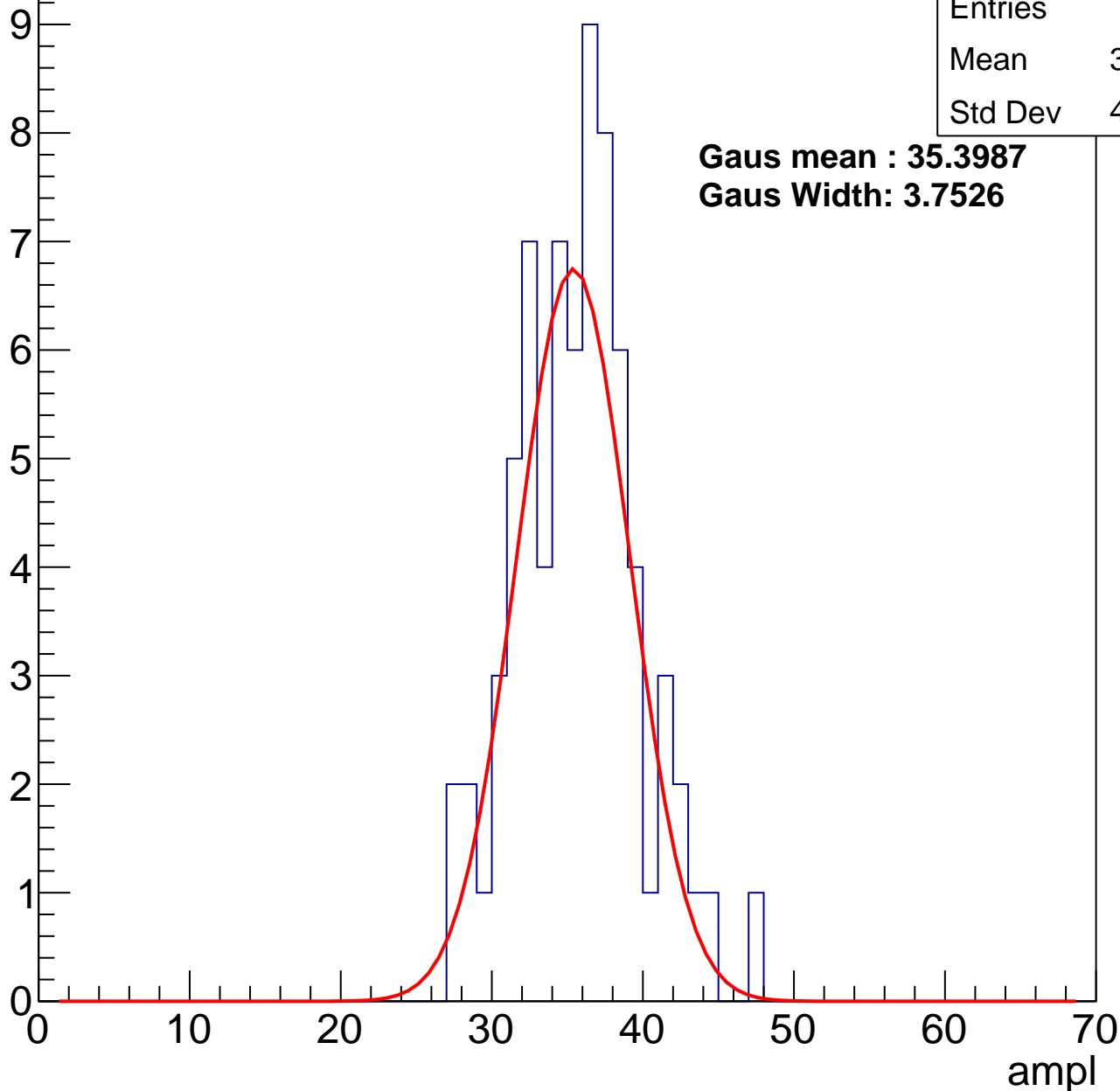
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	35.25
Std Dev	4.016

**Gaus mean : 35.3987**

**Gaus Width: 3.7526**



# B1L101S, U9-ch59, adc2

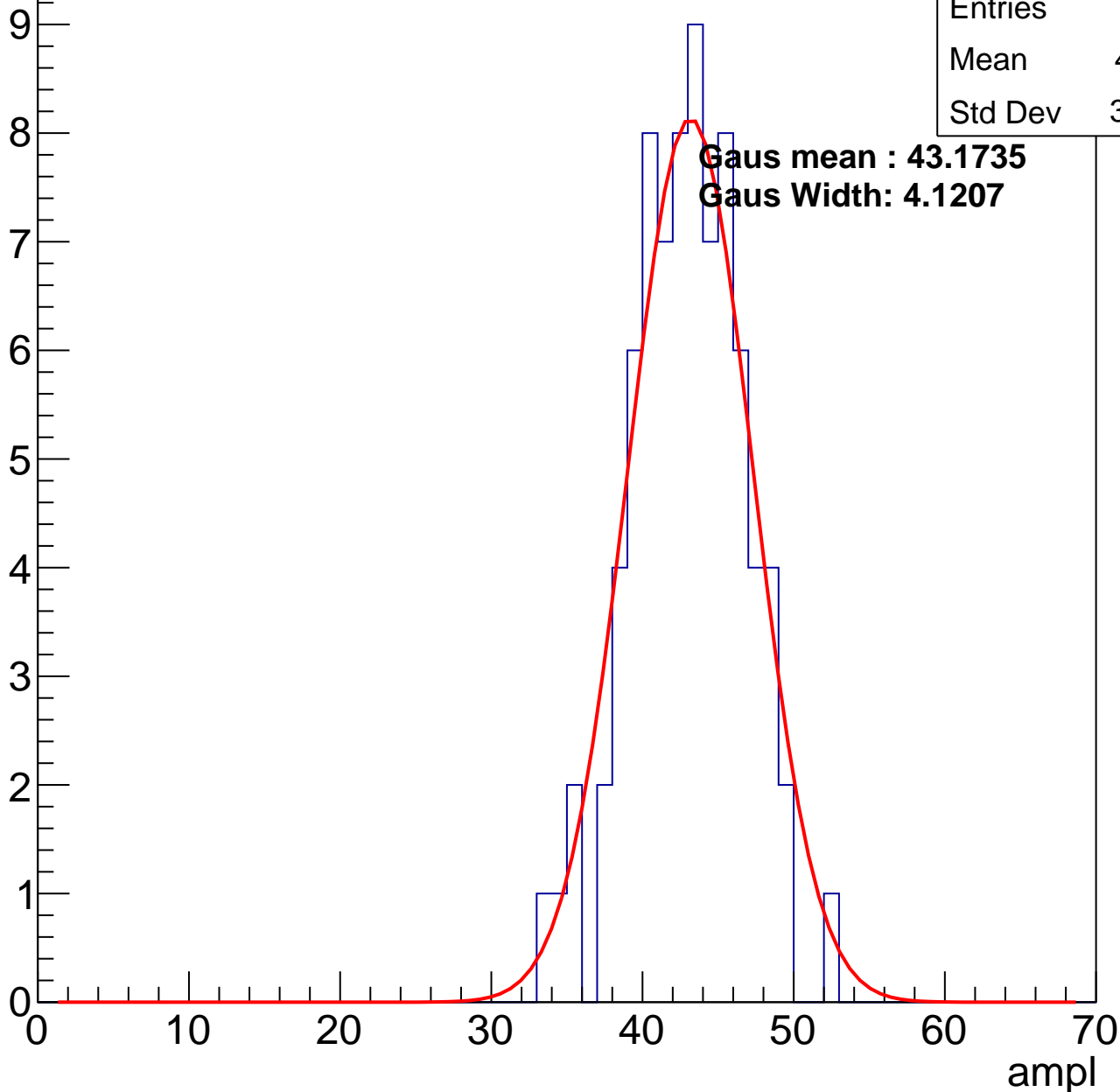
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	42.51
Std Dev	3.667

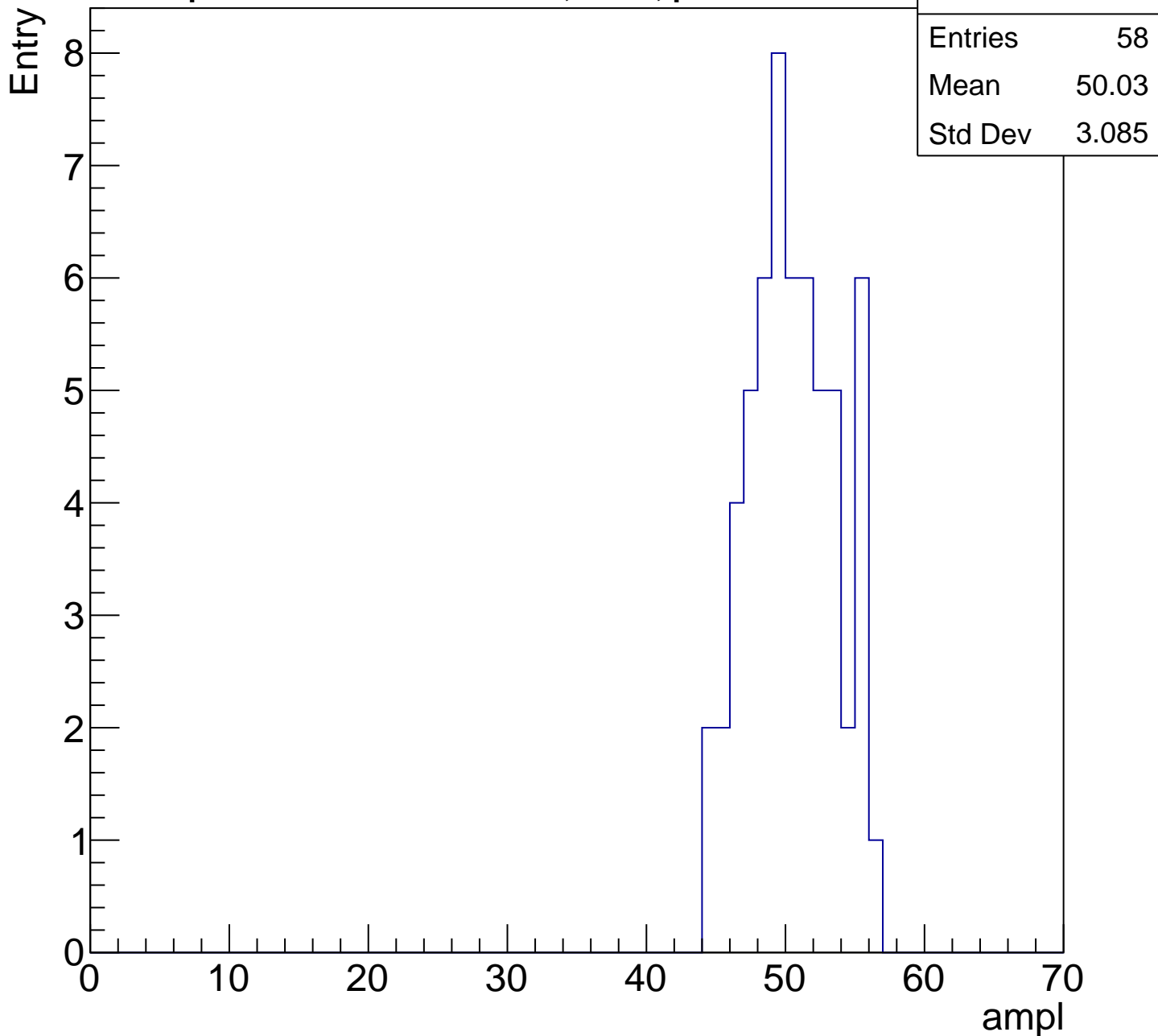
**Gaus mean : 43.1735**

**Gaus Width: 4.1207**



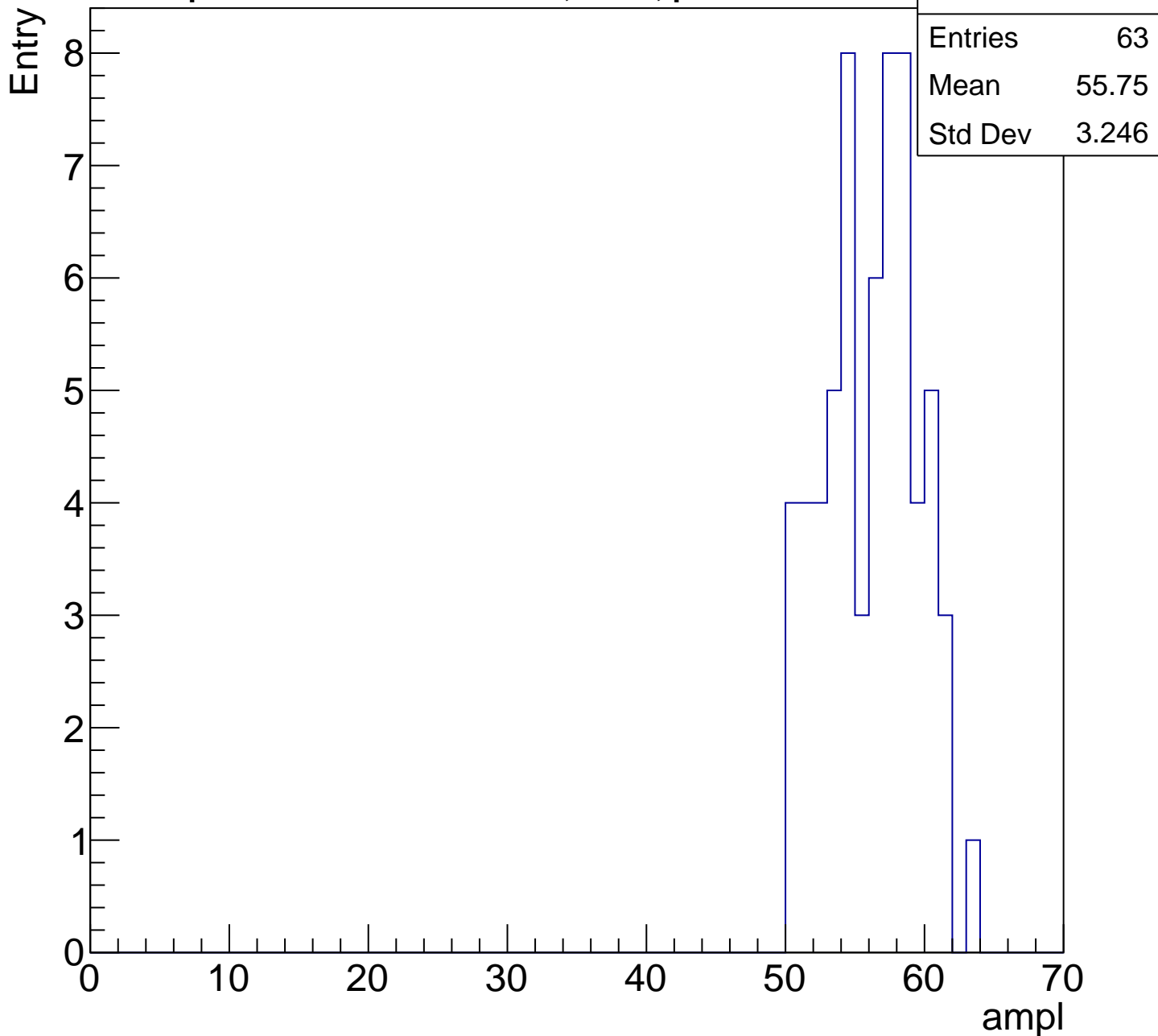
# B1L101S, U9-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

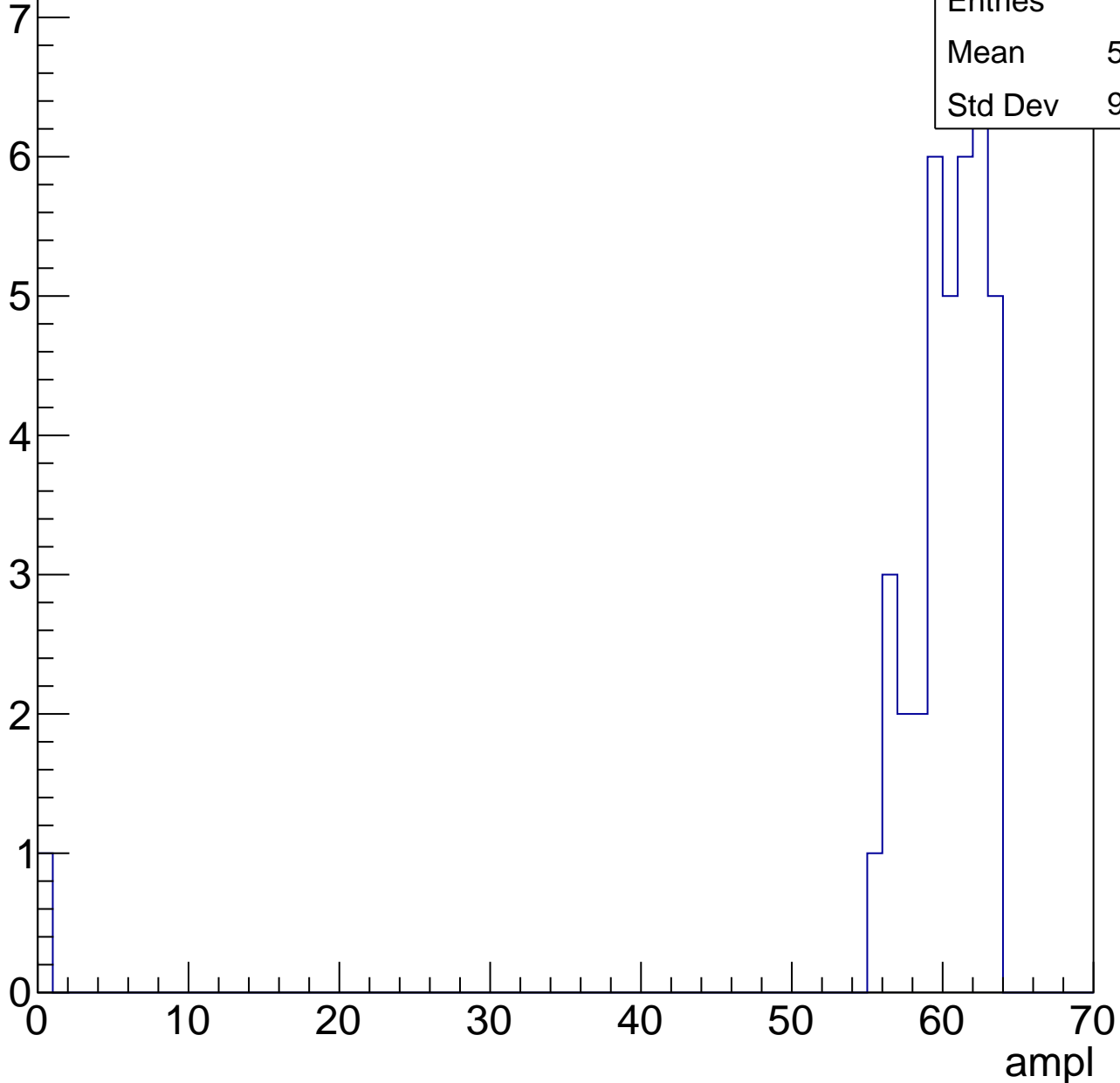


# B1L101S, U9-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

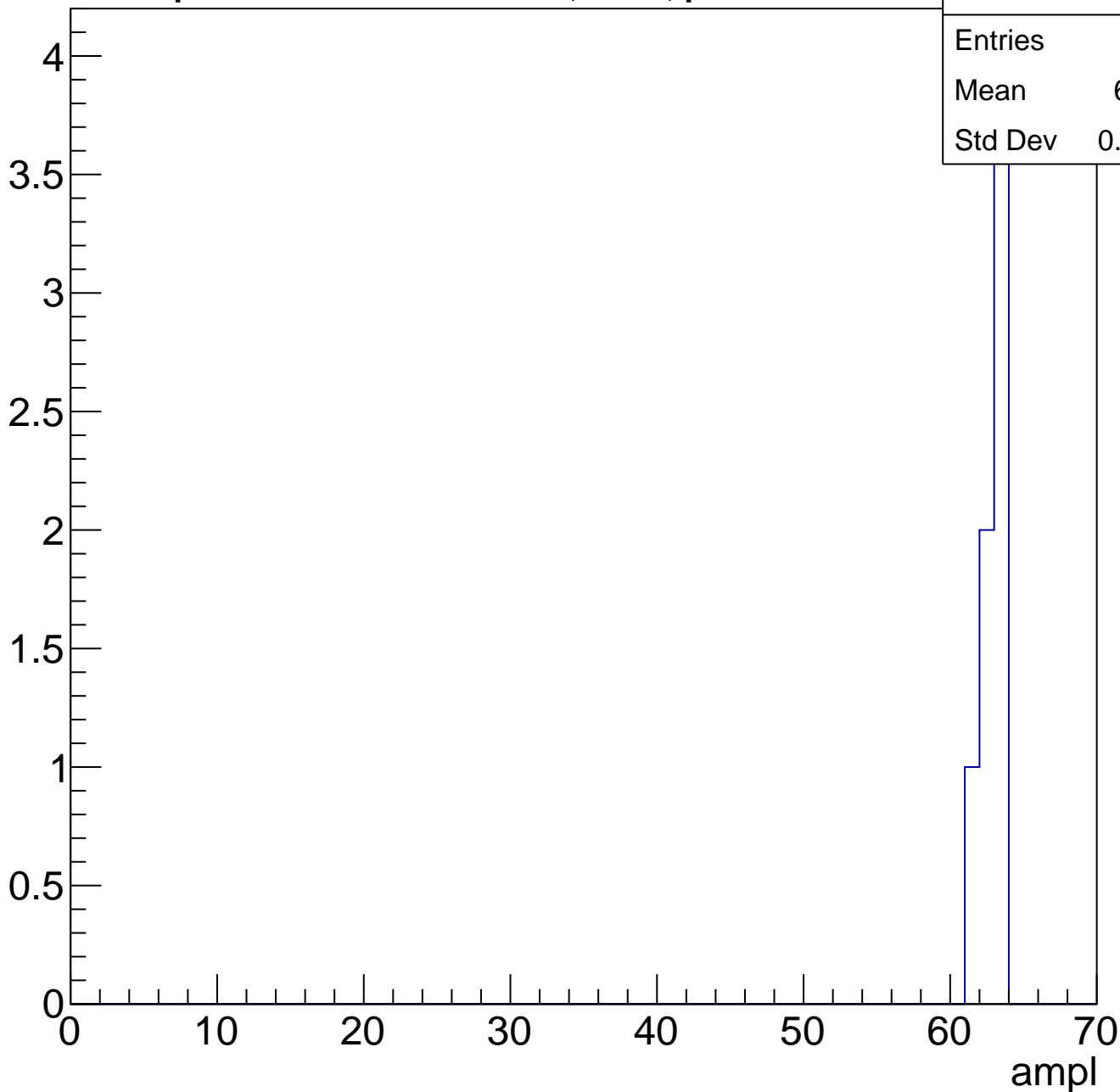
Entries	38
Mean	58.47
Std Dev	9.862



# B1L101S, U9-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	62
Std Dev	0

ampl

# B1L101S, U9-ch60, adc0

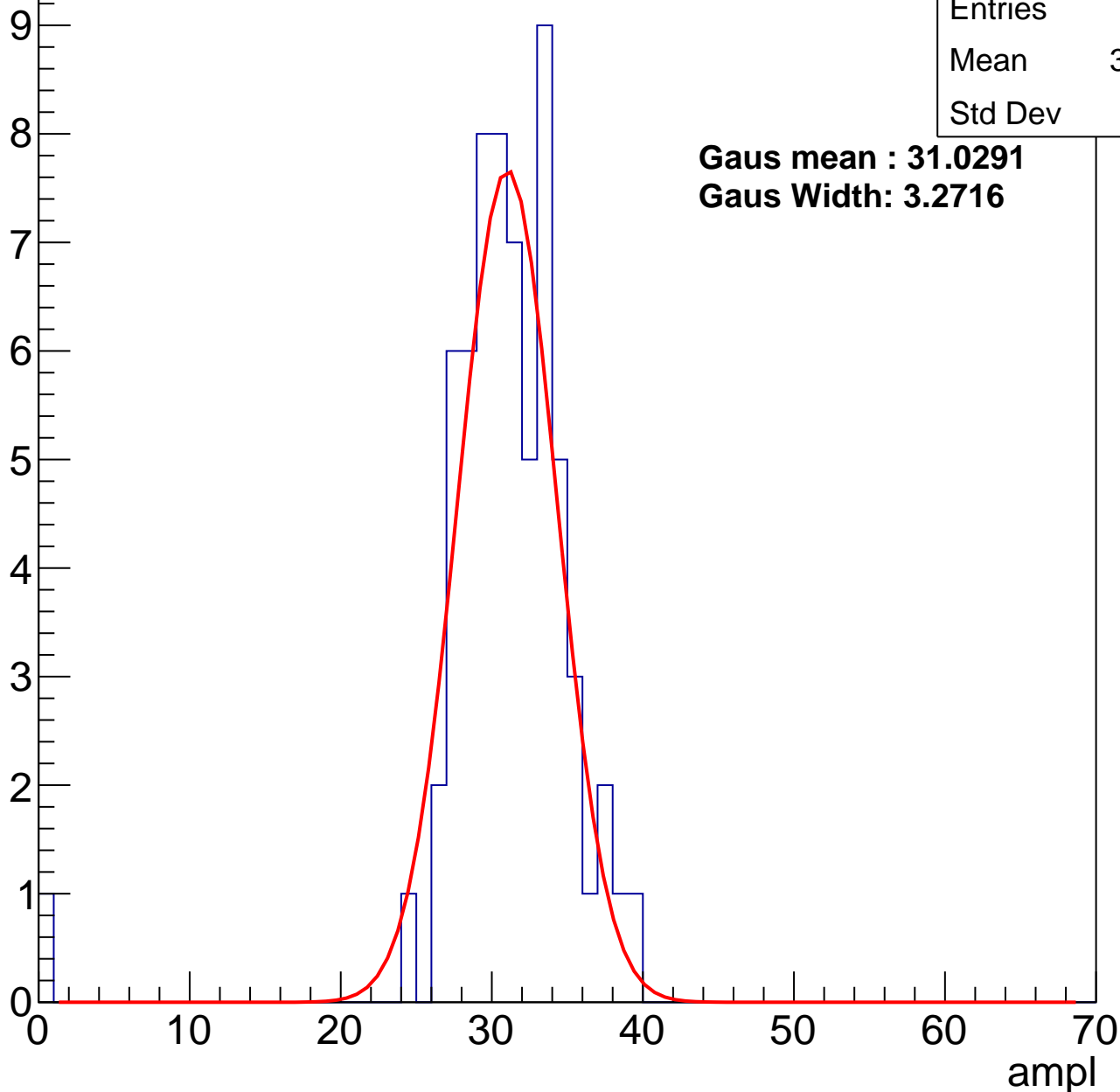
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	30.52
Std Dev	4.89

**Gaus mean : 31.0291**

**Gaus Width: 3.2716**



# B1L101S, U9-ch60, adc1

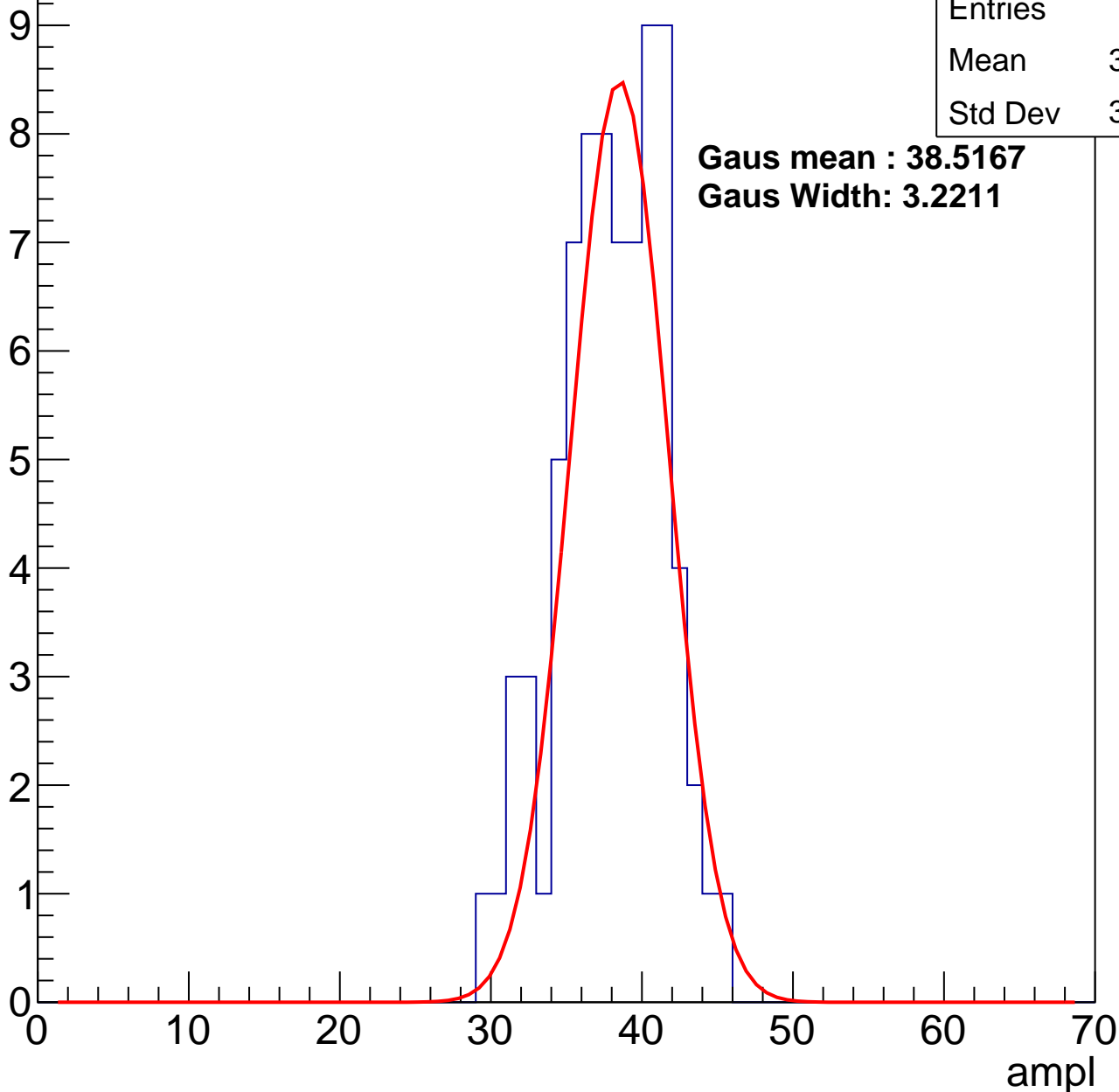
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	37.55
Std Dev	3.447

**Gaus mean : 38.5167**

**Gaus Width: 3.2211**



# B1L101S, U9-ch60, adc2

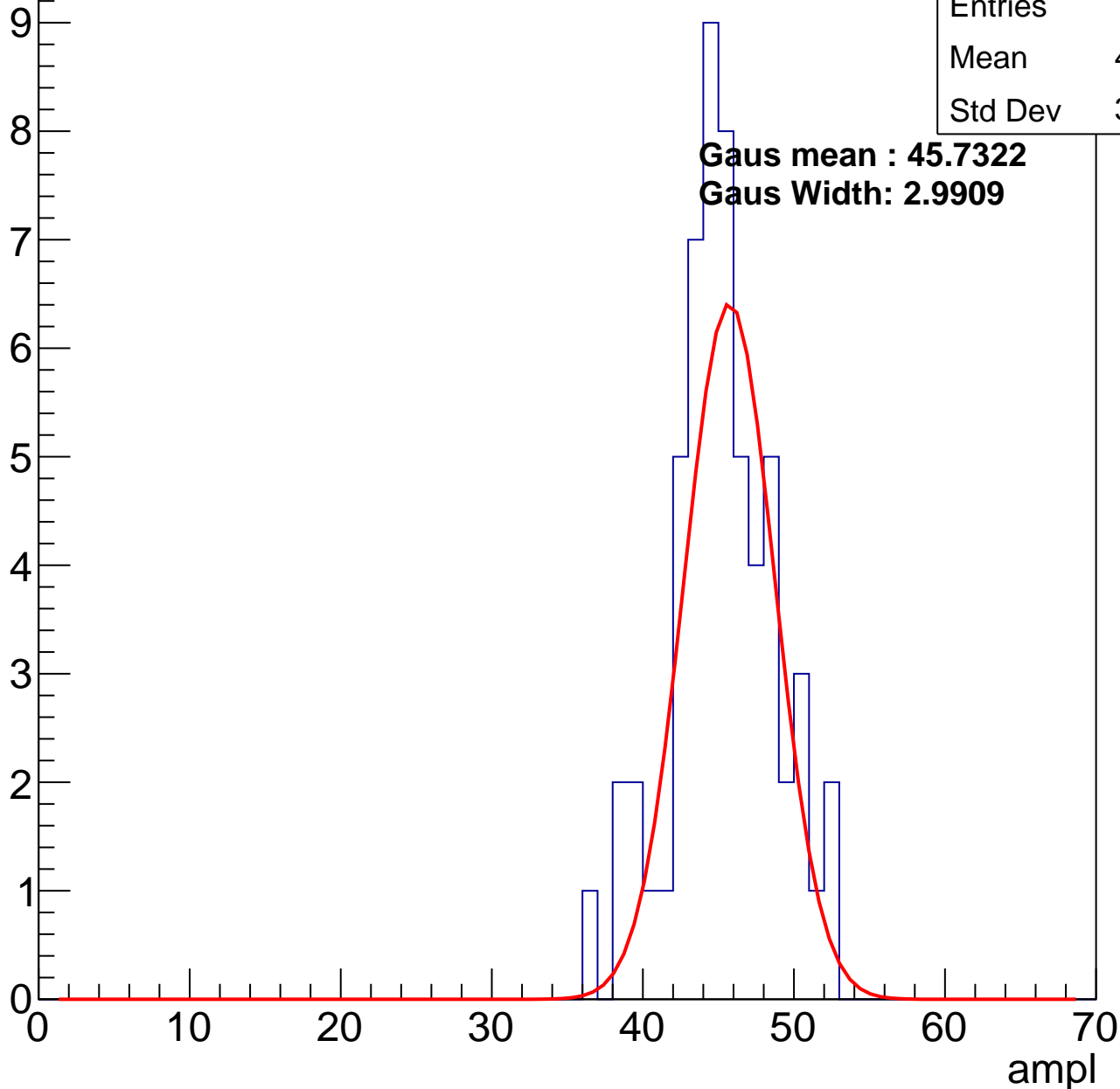
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	44.81
Std Dev	3.421

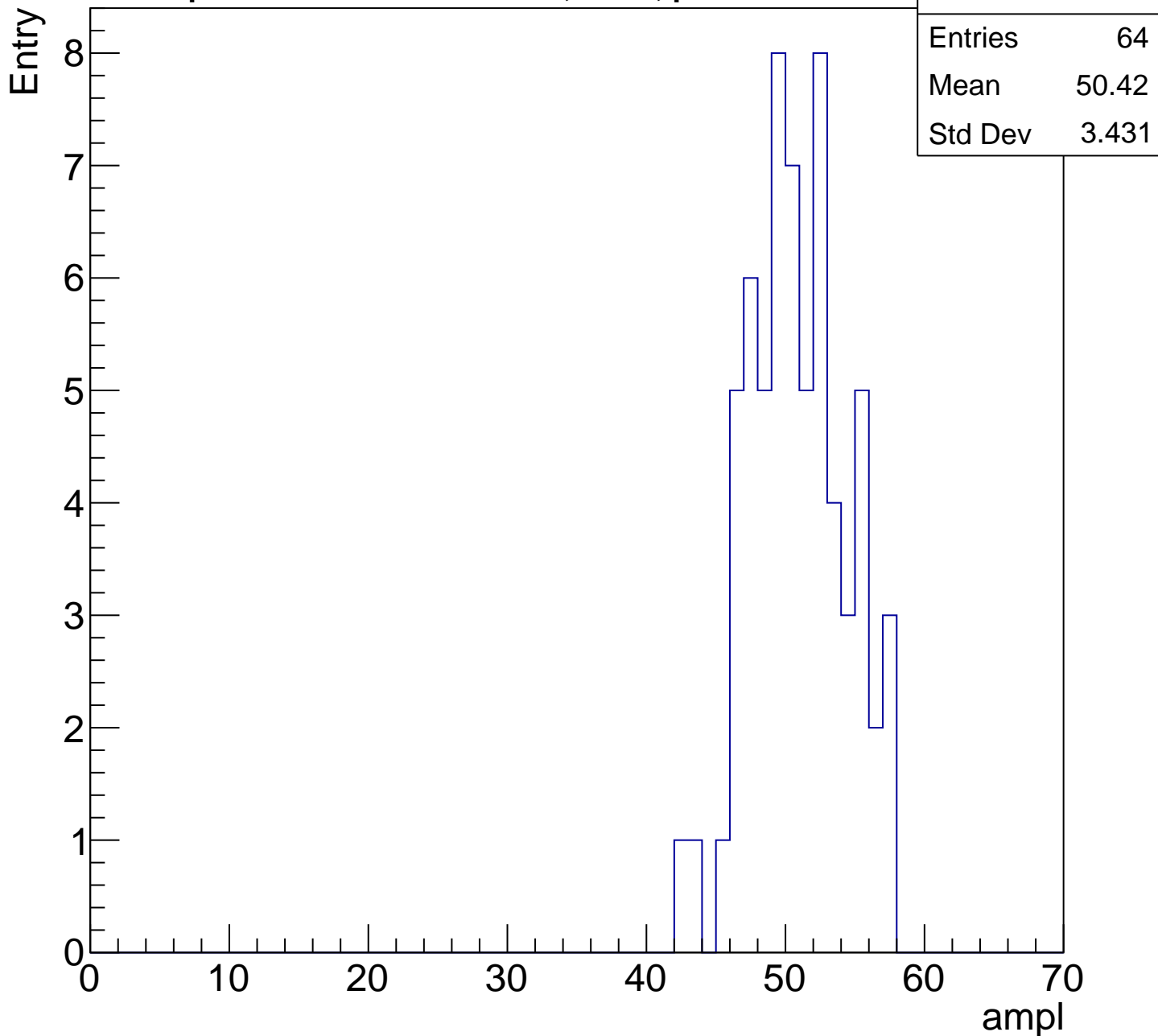
**Gaus mean : 45.7322**

**Gaus Width: 2.9909**



# B1L101S, U9-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

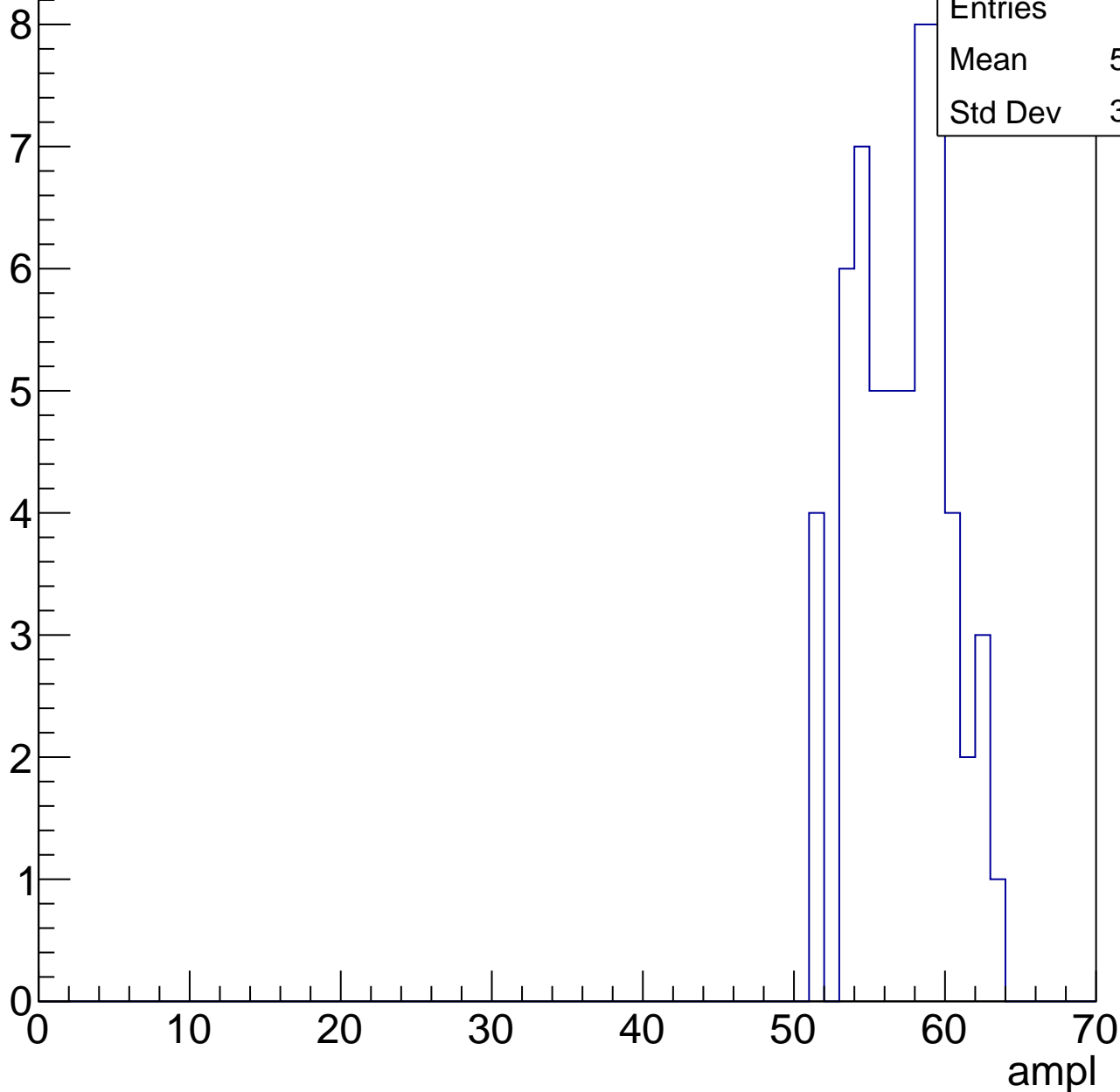


# B1L101S, U9-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	56.67
Std Dev	3.053

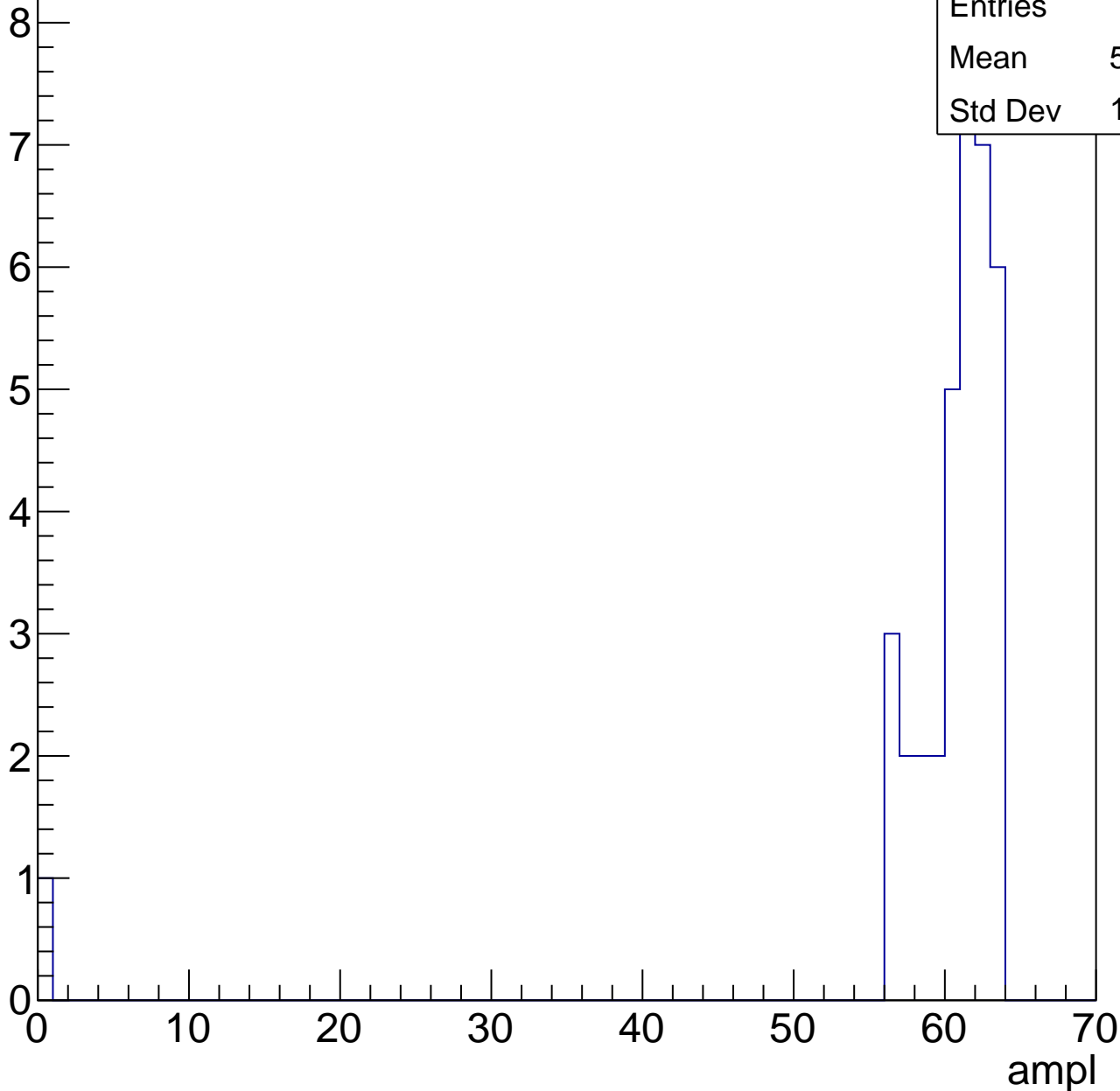


# B1L101S, U9-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

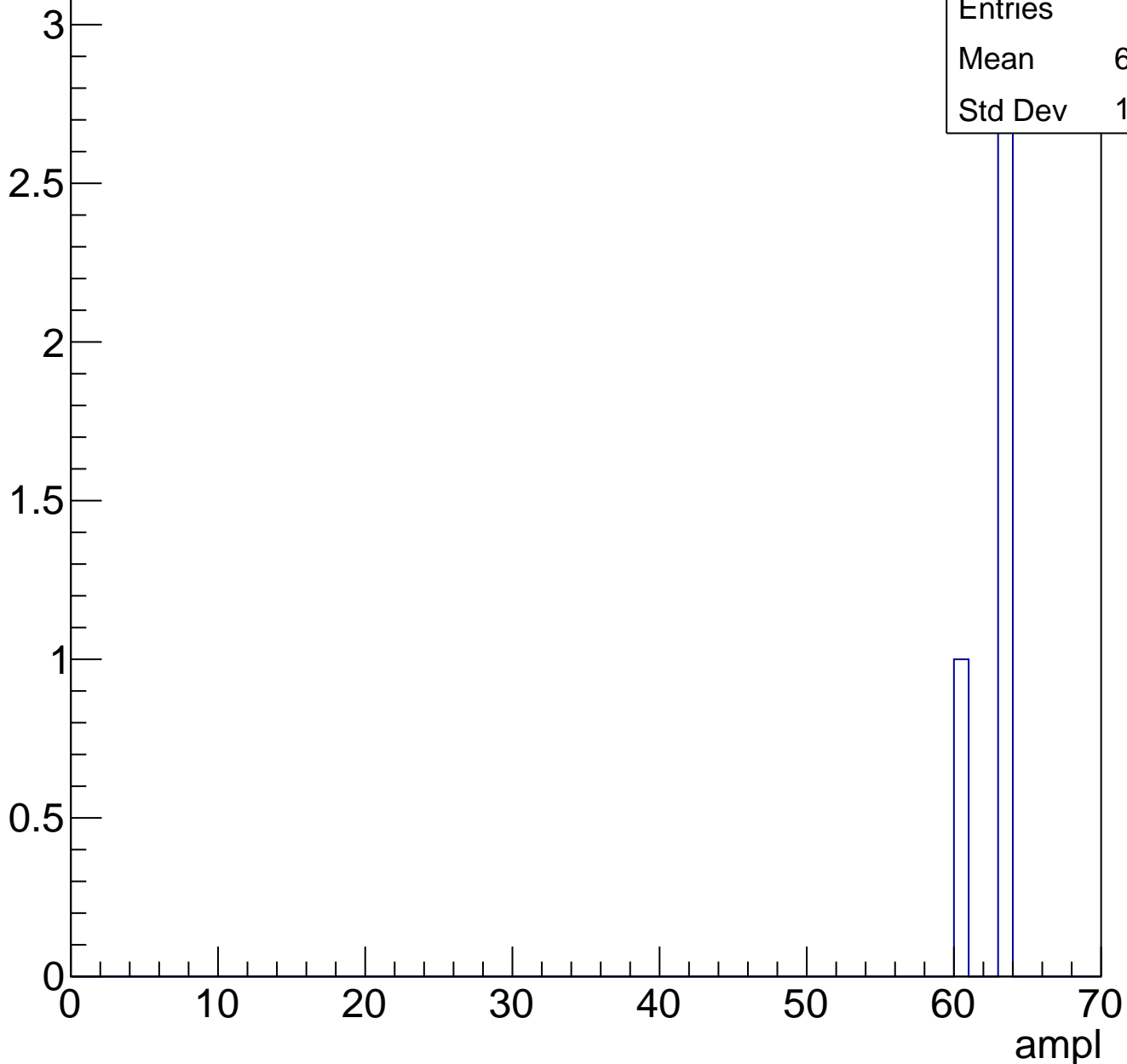
Entries	36
Mean	58.78
Std Dev	10.15



# B1L101S, U9-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U9-ch61, adc0

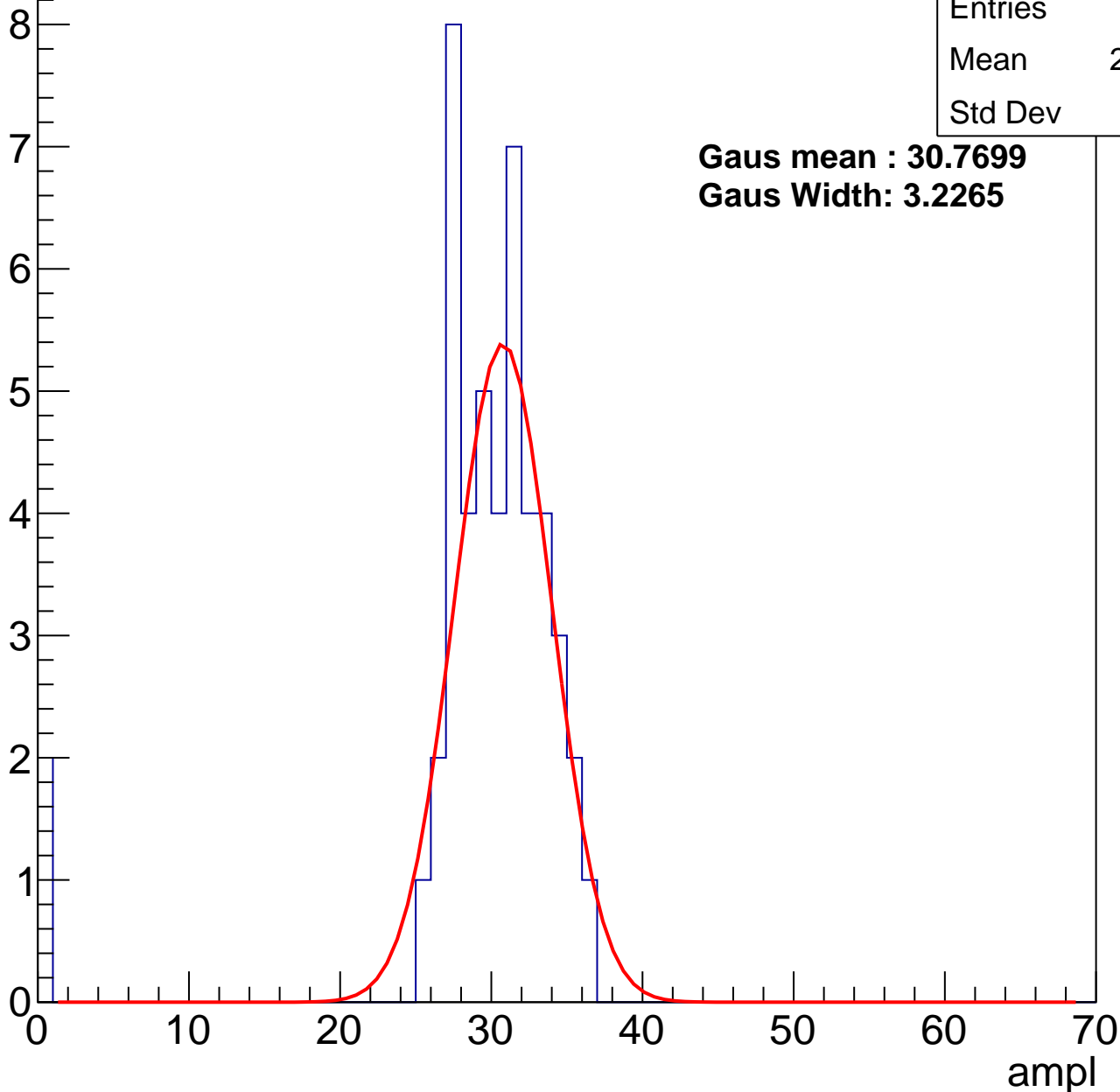
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	28.83
Std Dev	6.65

**Gaus mean : 30.7699**

**Gaus Width: 3.2265**



# B1L101S, U9-ch61, adc1

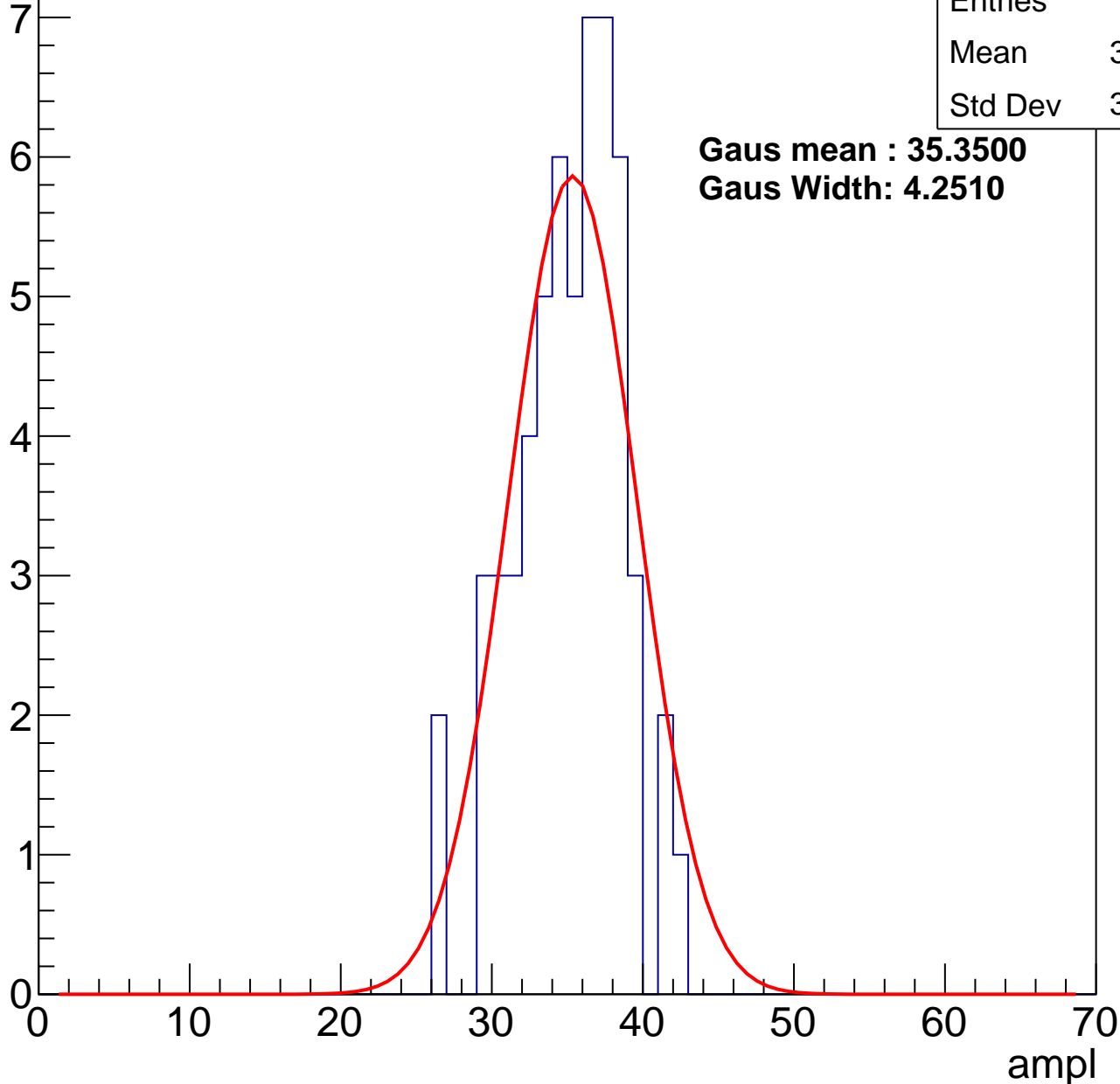
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	34.63
Std Dev	3.518

**Gaus mean : 35.3500**

**Gaus Width: 4.2510**



# B1L101S, U9-ch61, adc2

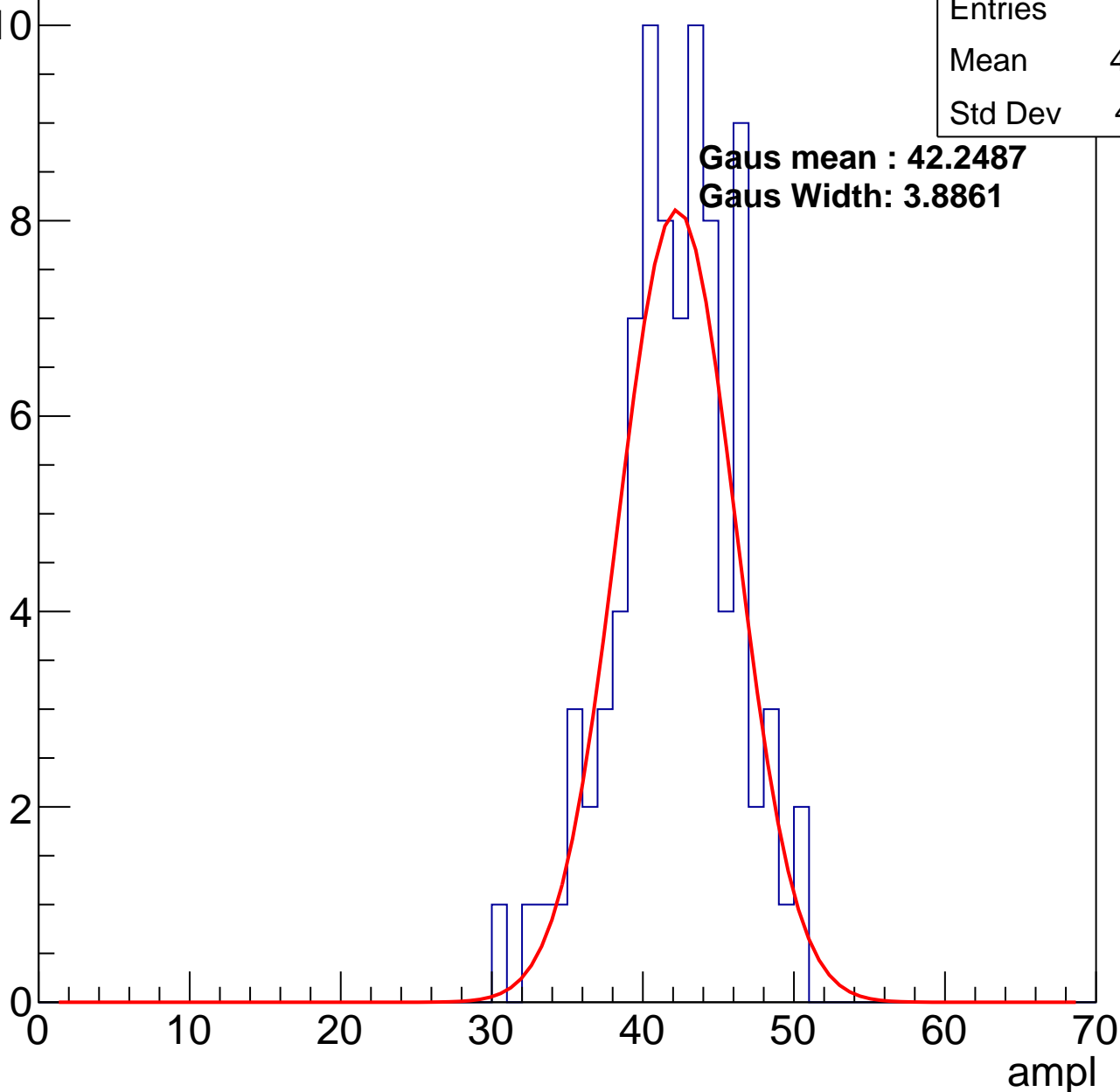
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	87
Mean	41.69
Std Dev	4.021

**Gaus mean : 42.2487**

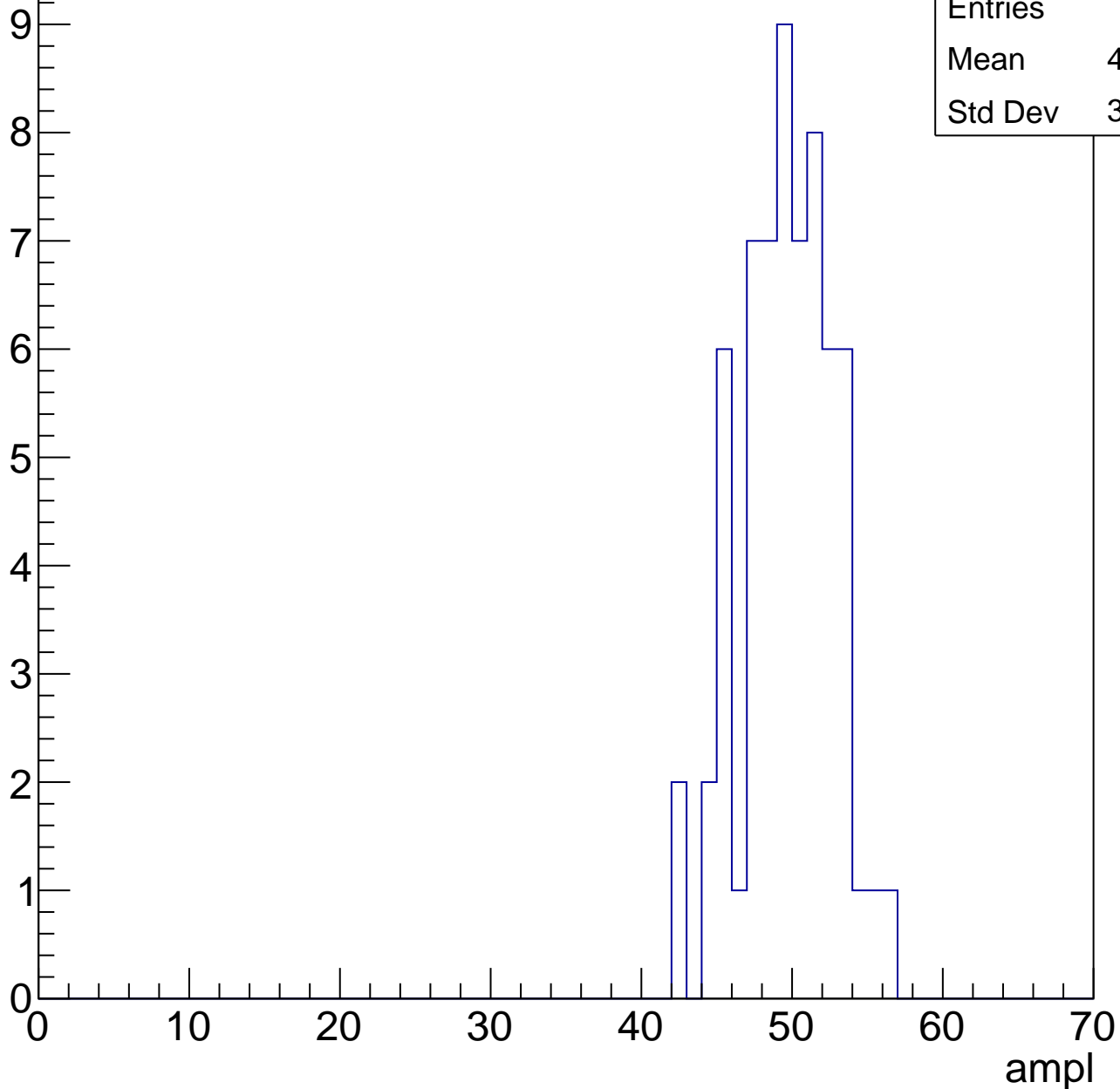
**Gaus Width: 3.8861**



# B1L101S, U9-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

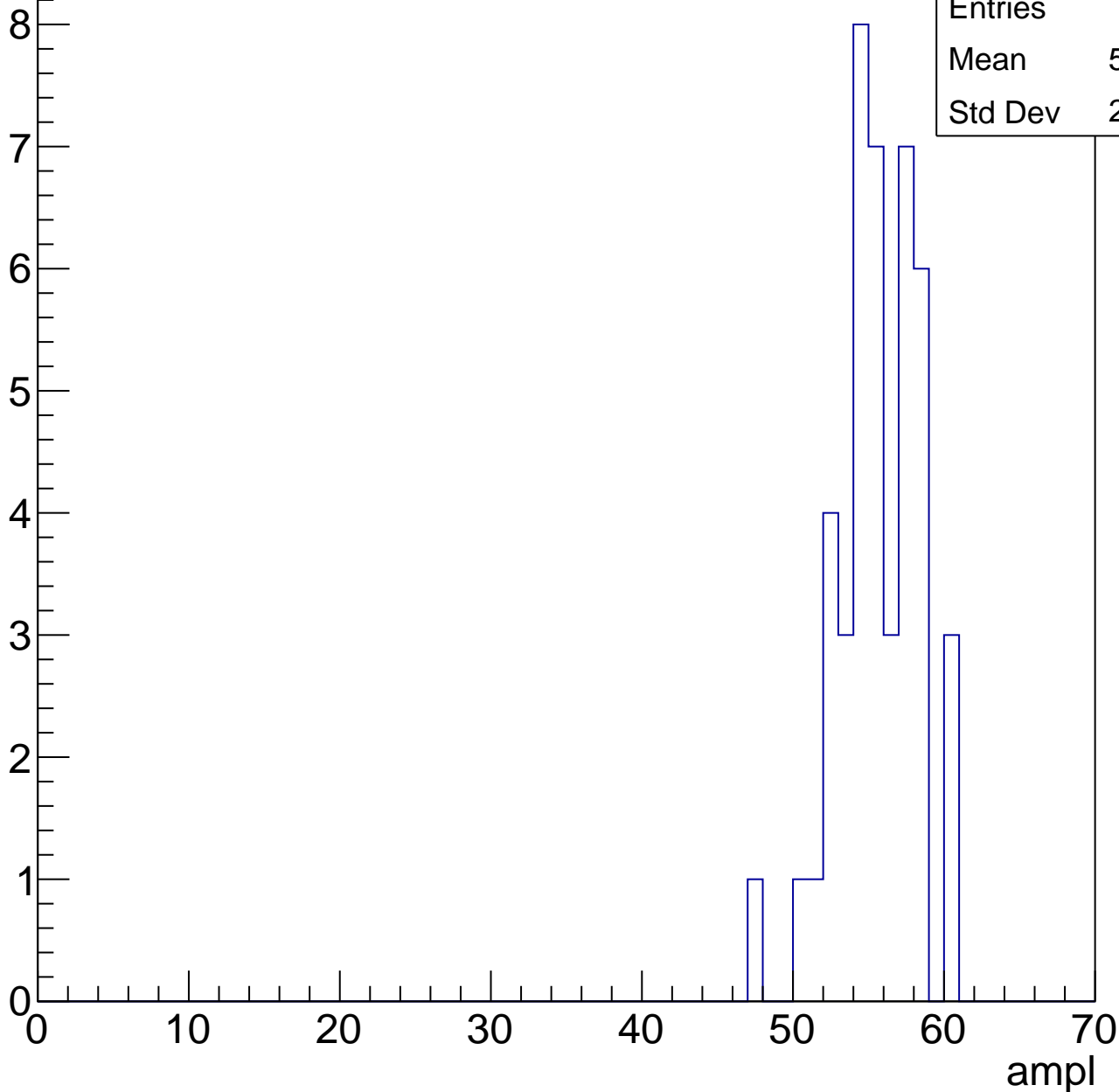


# B1L101S, U9-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	44
Mean	55.16
Std Dev	2.696

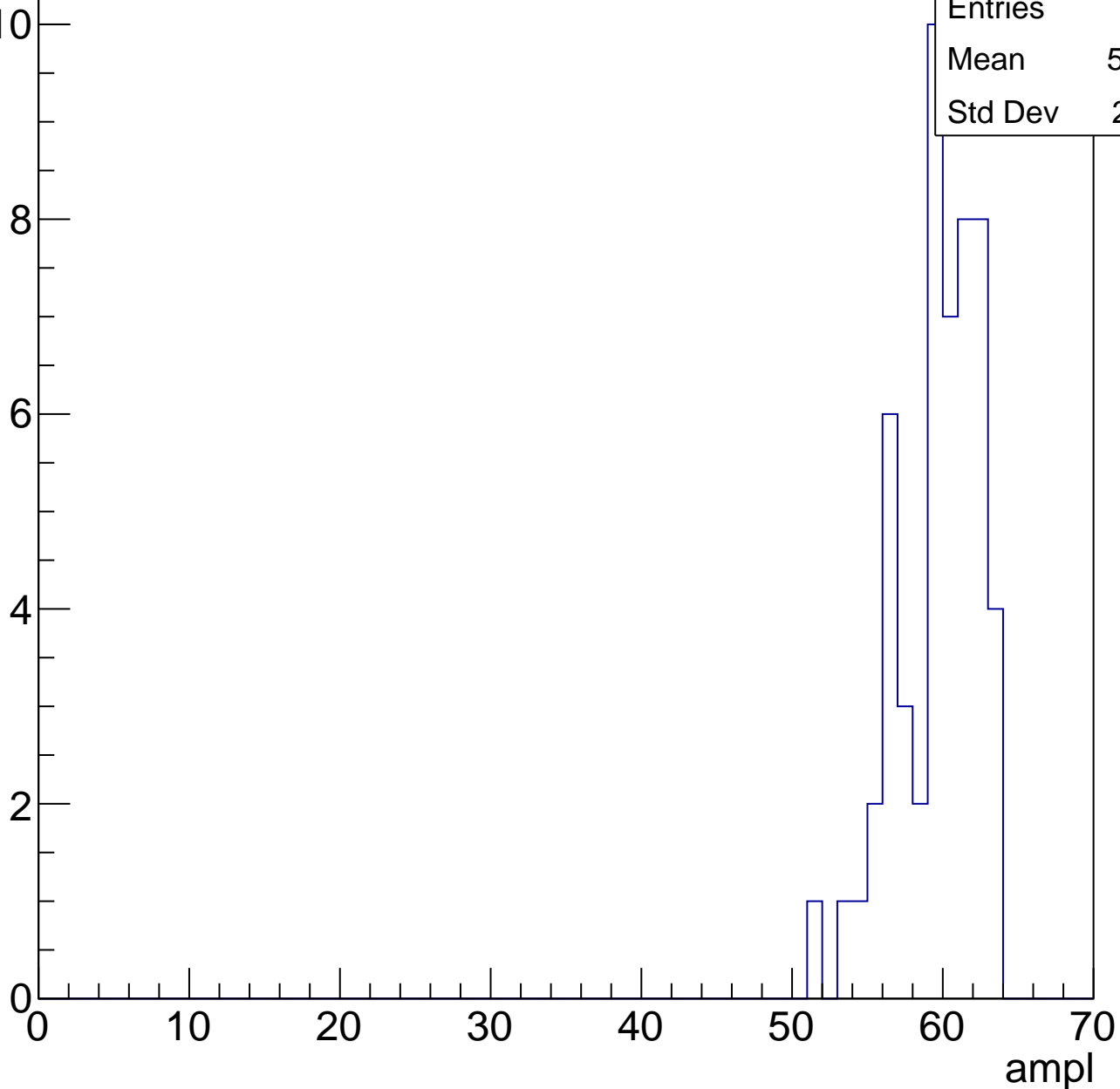


# B1L101S, U9-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	59.19
Std Dev	2.741

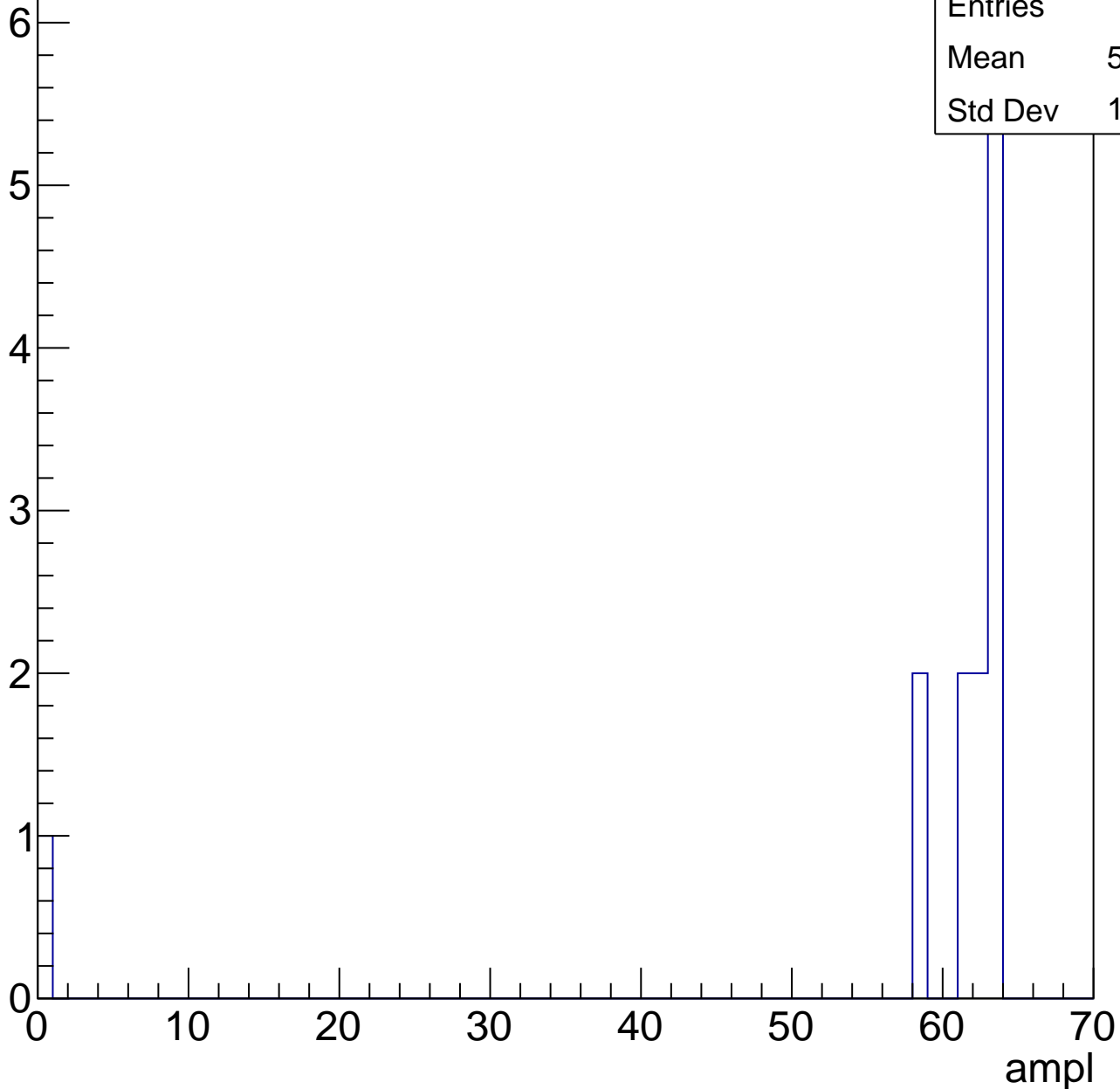


# B1L101S, U9-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	13
Mean	56.92
Std Dev	16.52





# B1L101S, U9-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	25
Std Dev	0

ampl

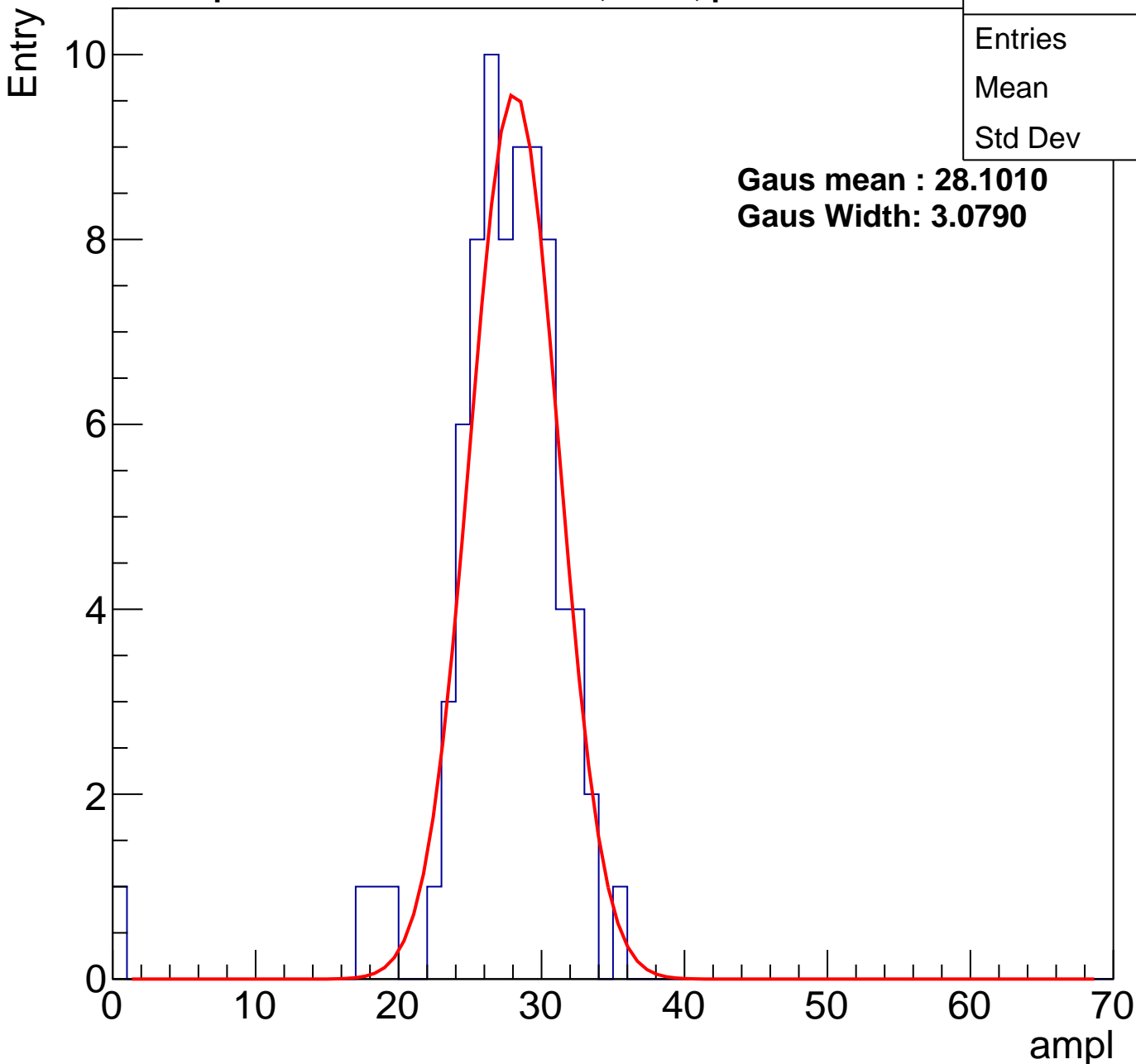
# B1L101S, U9-ch62, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	77
Mean	26.9
Std Dev	4.5

**Gaus mean : 28.1010**

**Gaus Width: 3.0790**



# B1L101S, U9-ch62, adc1

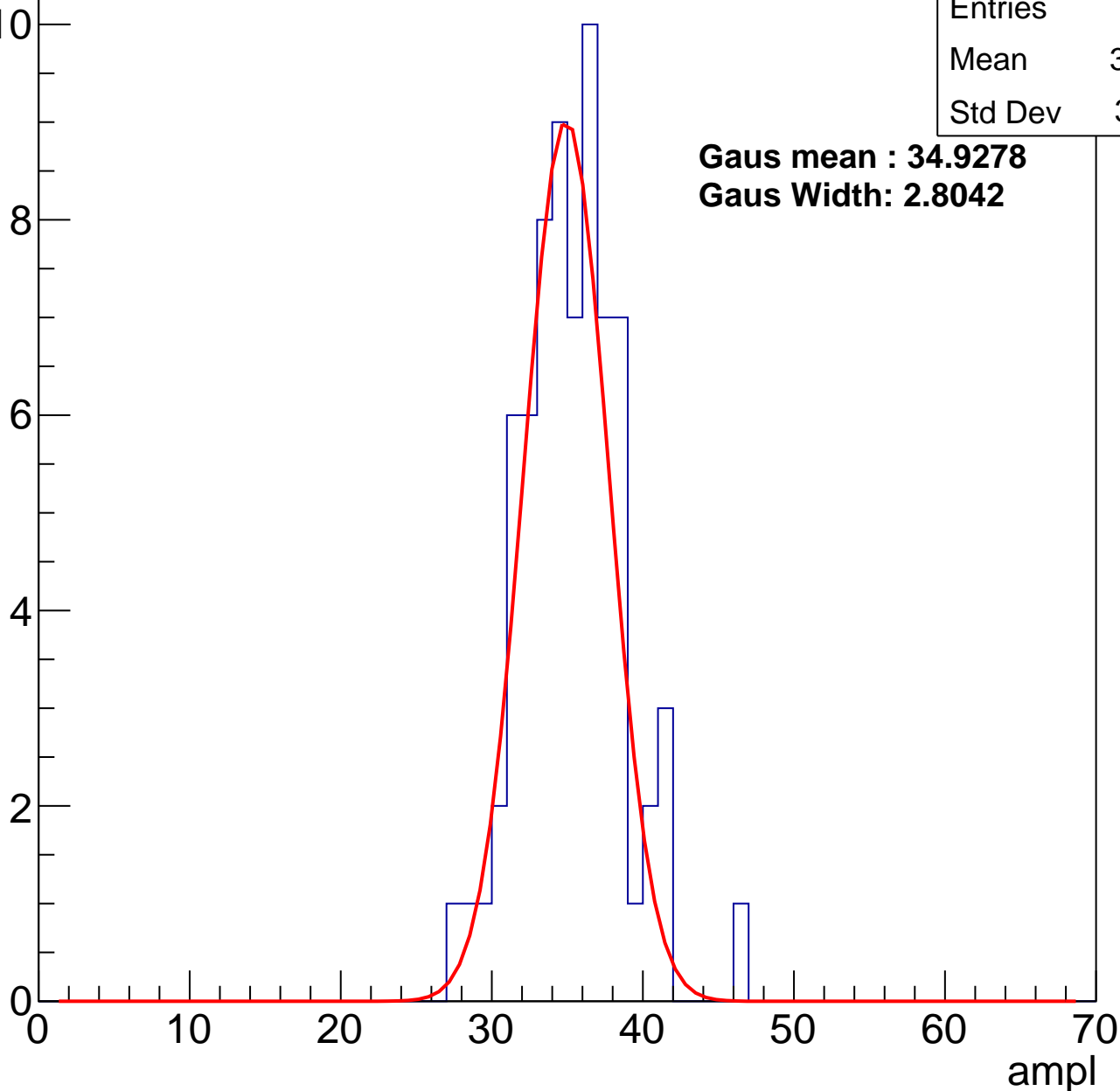
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	34.86
Std Dev	3.301

**Gaus mean : 34.9278**

**Gaus Width: 2.8042**



# B1L101S, U9-ch62, adc2

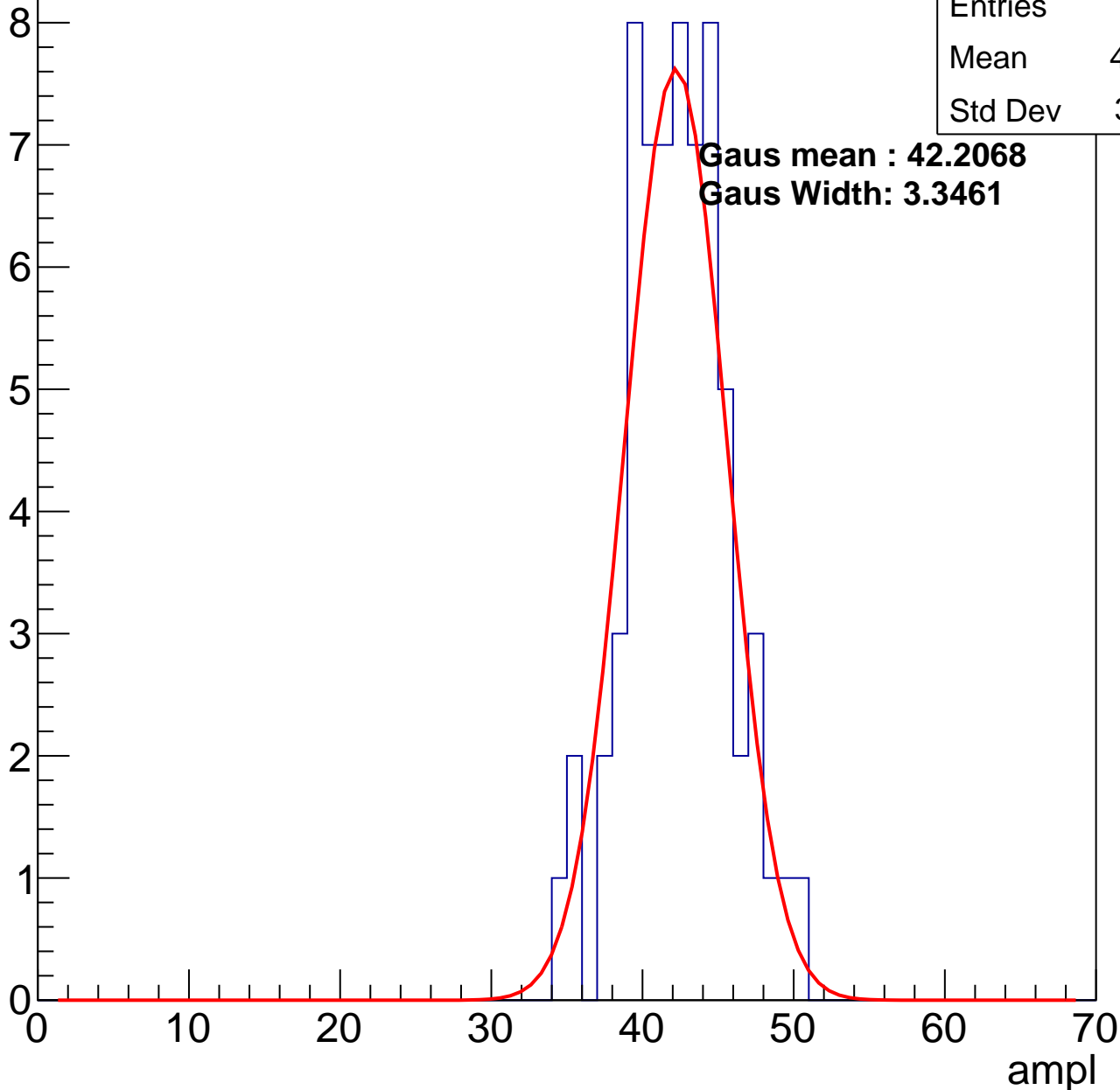
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	41.89
Std Dev	3.271

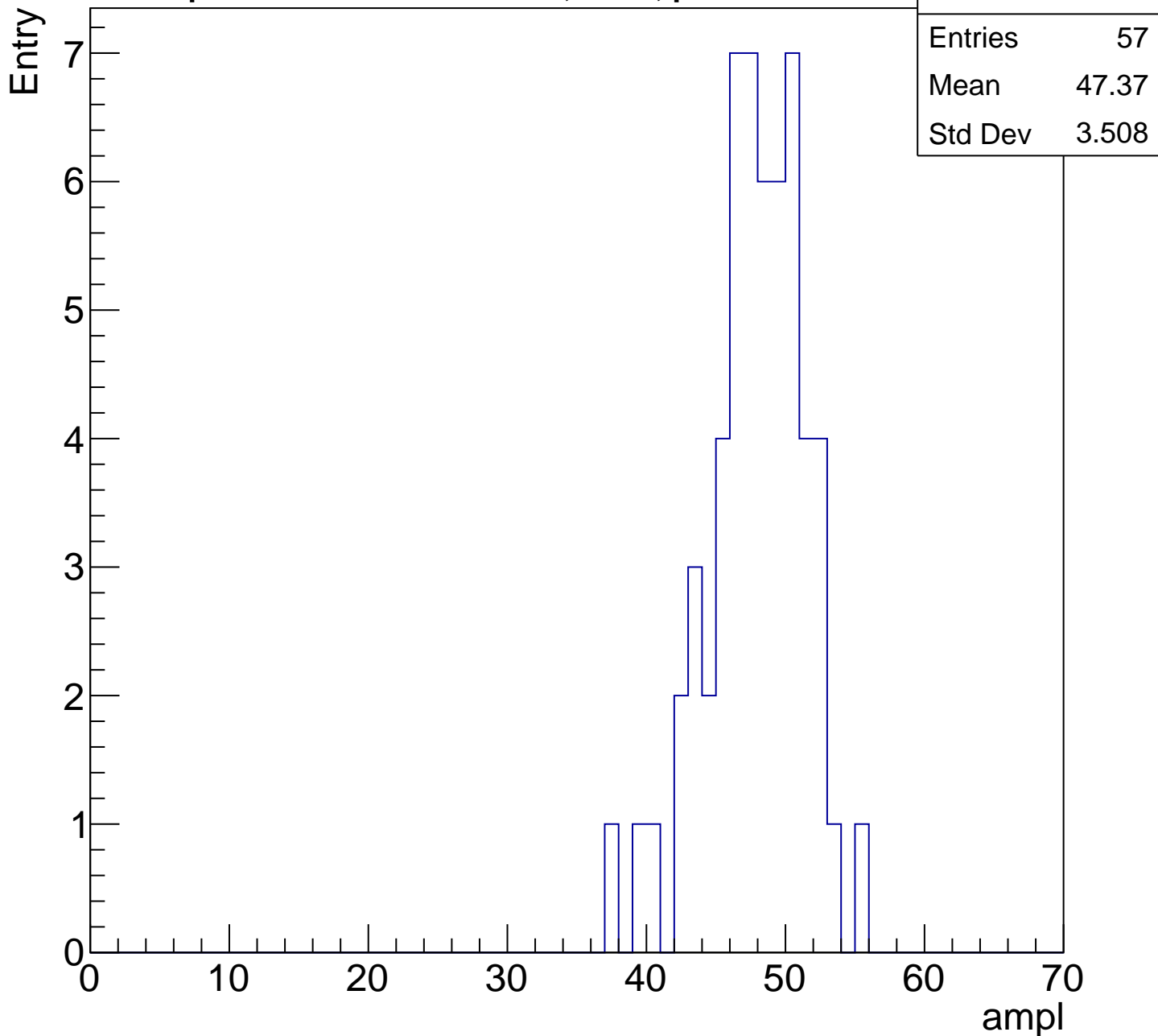
**Gaus mean : 42.2068**

**Gaus Width: 3.3461**



# B1L101S, U9-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

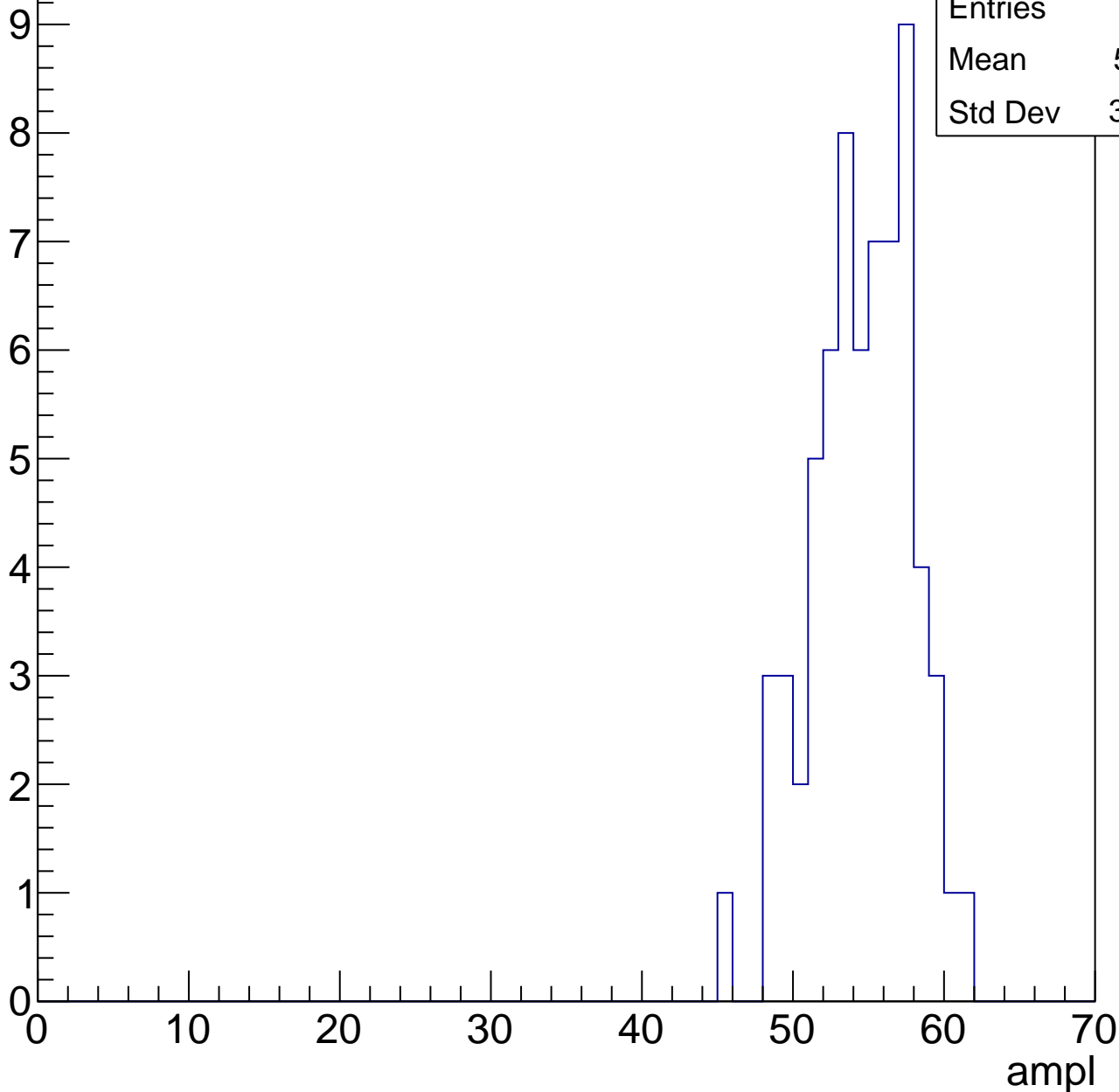


# B1L101S, U9-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	54.11
Std Dev	3.285

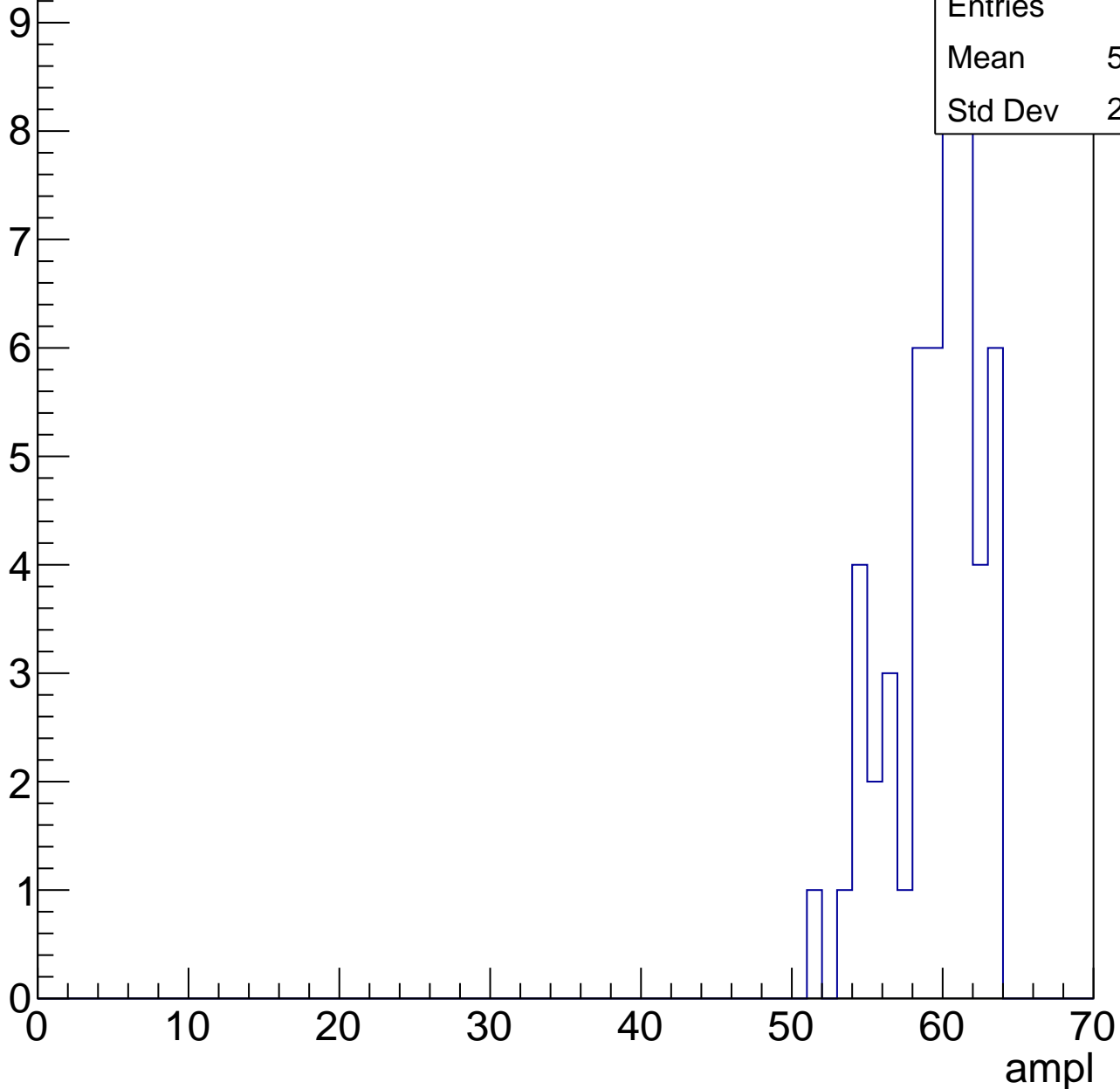


# B1L101S, U9-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	59.04
Std Dev	2.944

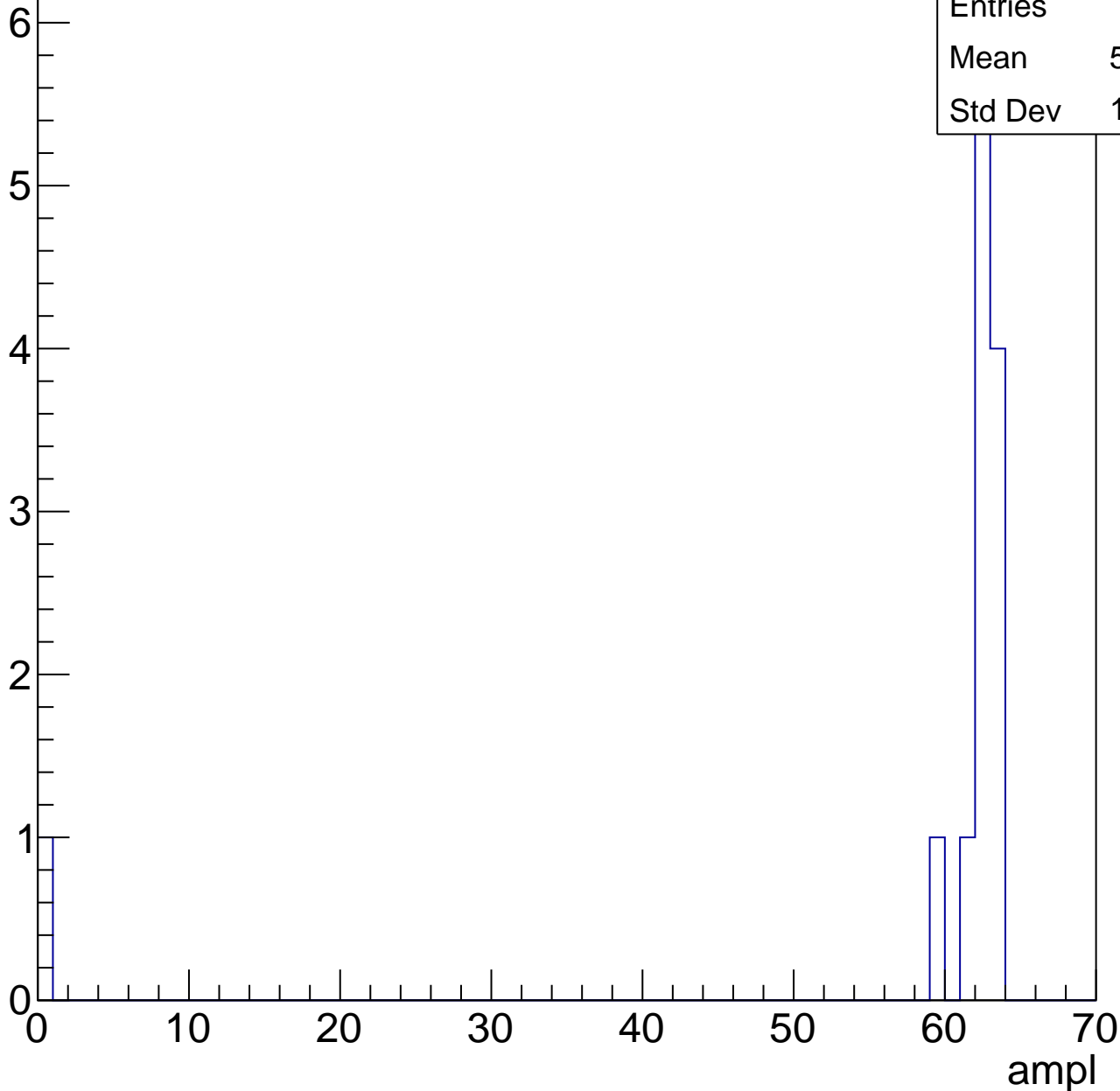


# B1L101S, U9-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	13
Mean	57.23
Std Dev	16.55





# B1L101S, U9-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch63, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

Entries 63

Mean 28.63

Std Dev 3.344

**Gaus mean : 28.5535**

**Gaus Width: 4.2831**

0

10

20

30

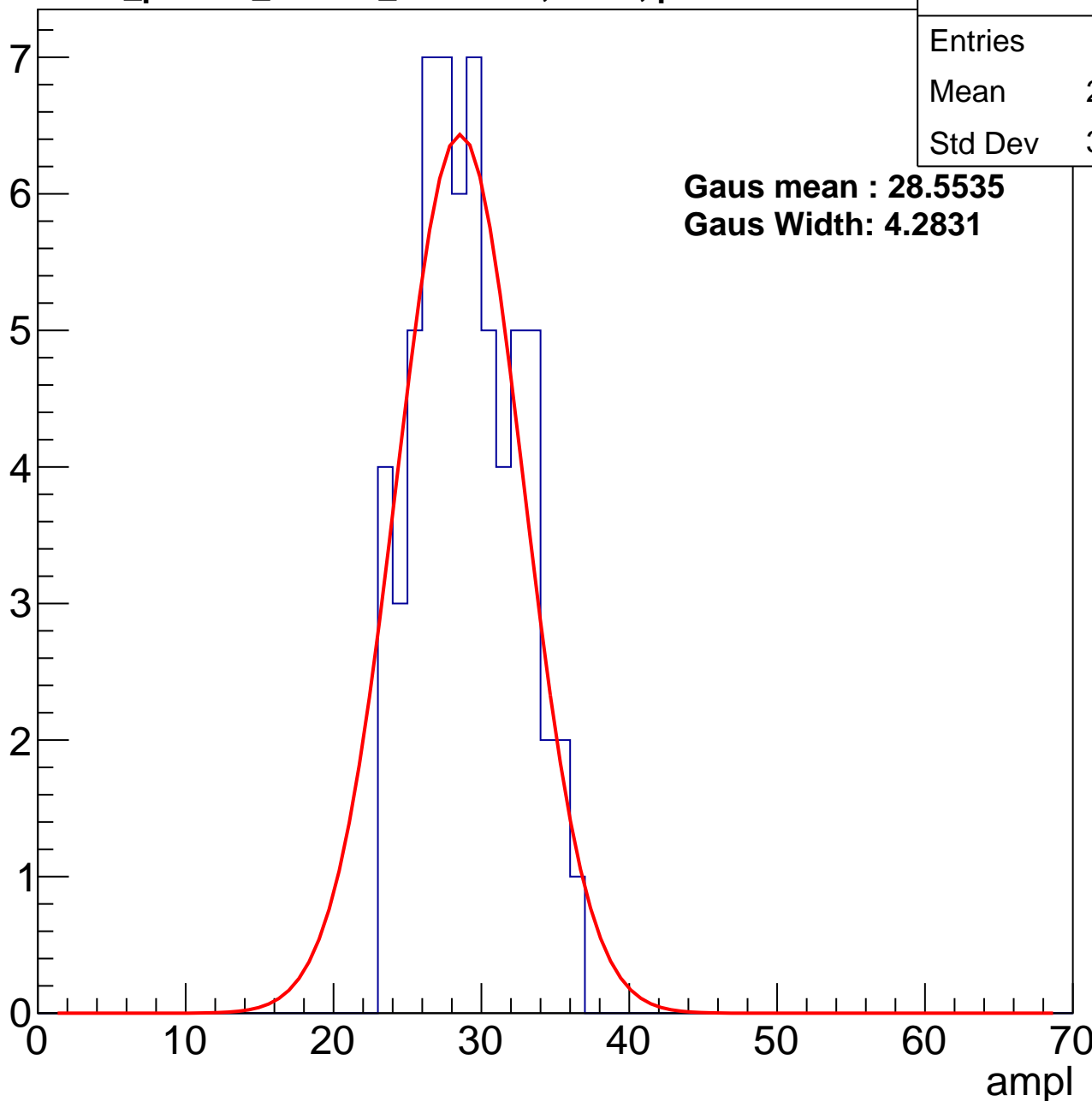
40

50

60

70

ampl



# B1L101S, U9-ch63, adc1

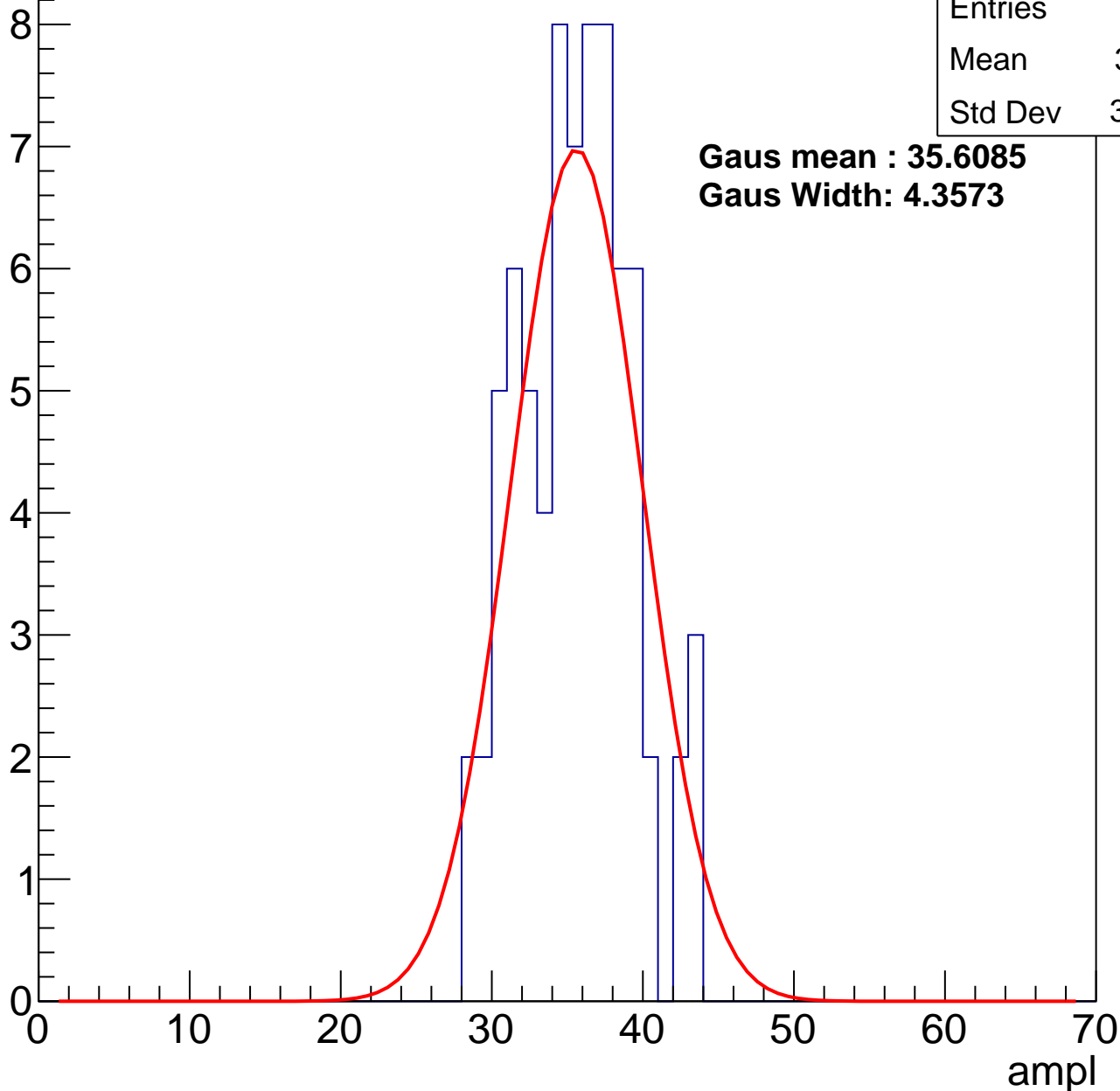
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	35.11
Std Dev	3.656

**Gaus mean : 35.6085**

**Gaus Width: 4.3573**



# B1L101S, U9-ch63, adc2

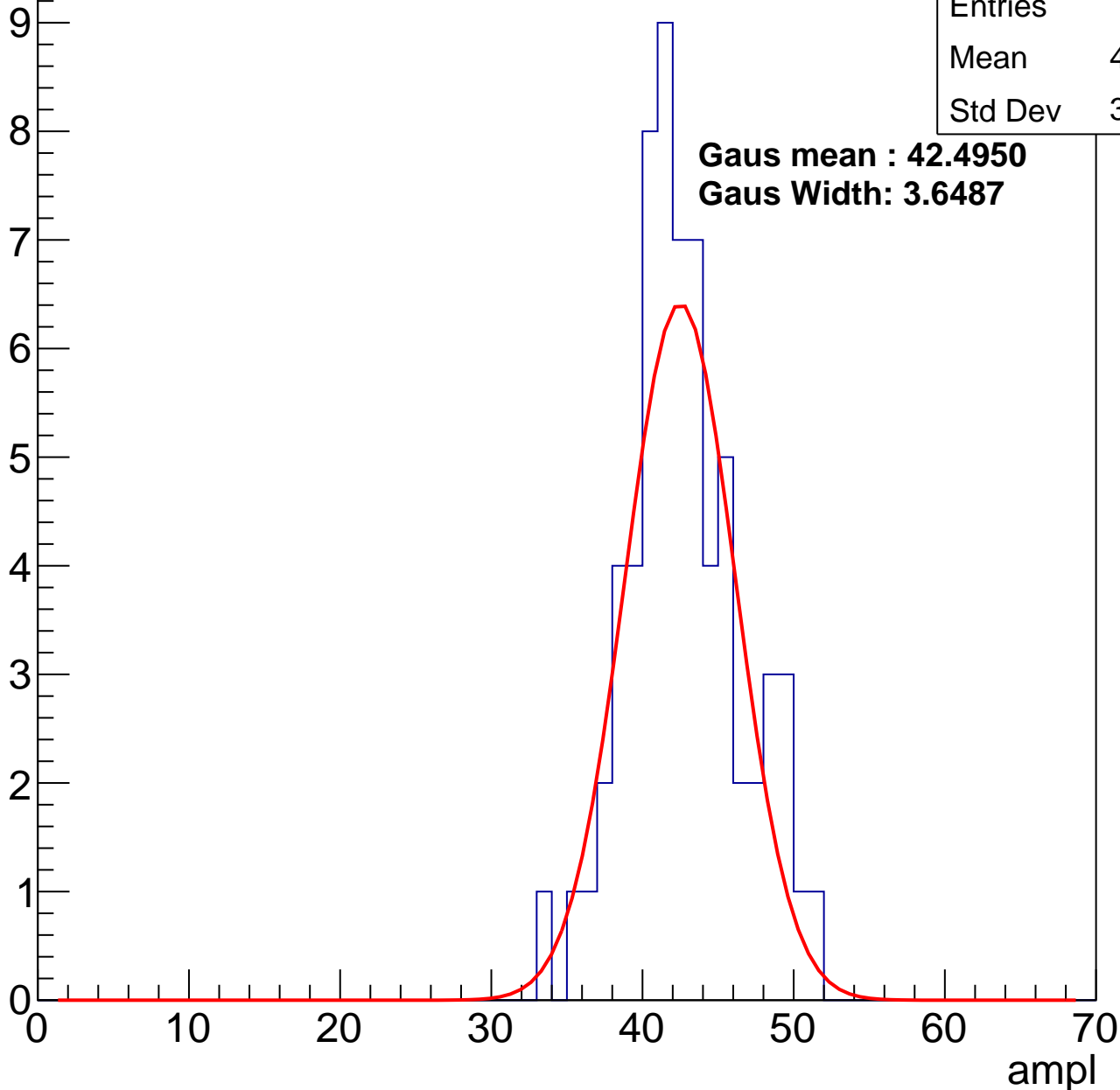
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	42.29
Std Dev	3.724

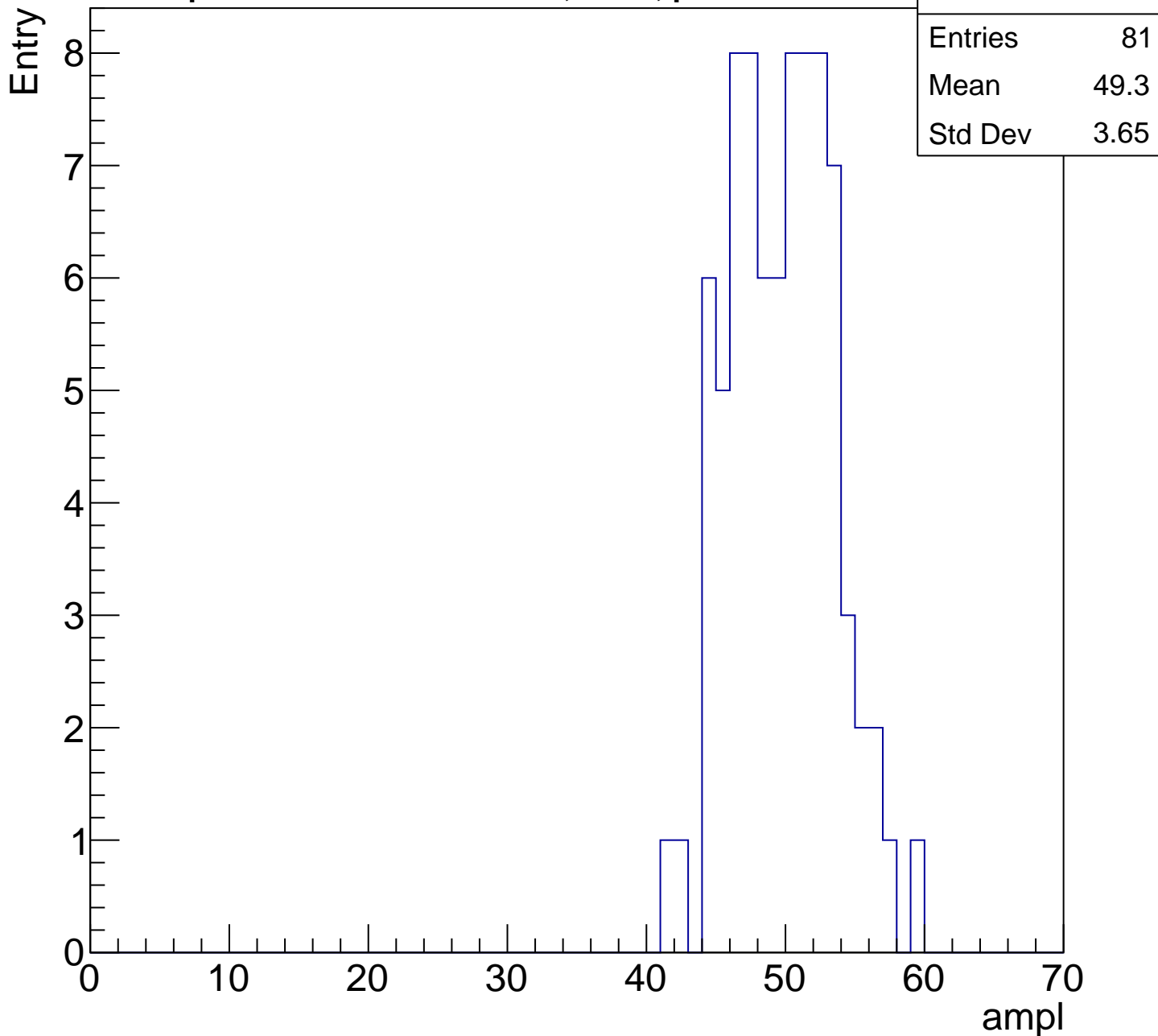
**Gaus mean : 42.4950**

**Gaus Width: 3.6487**



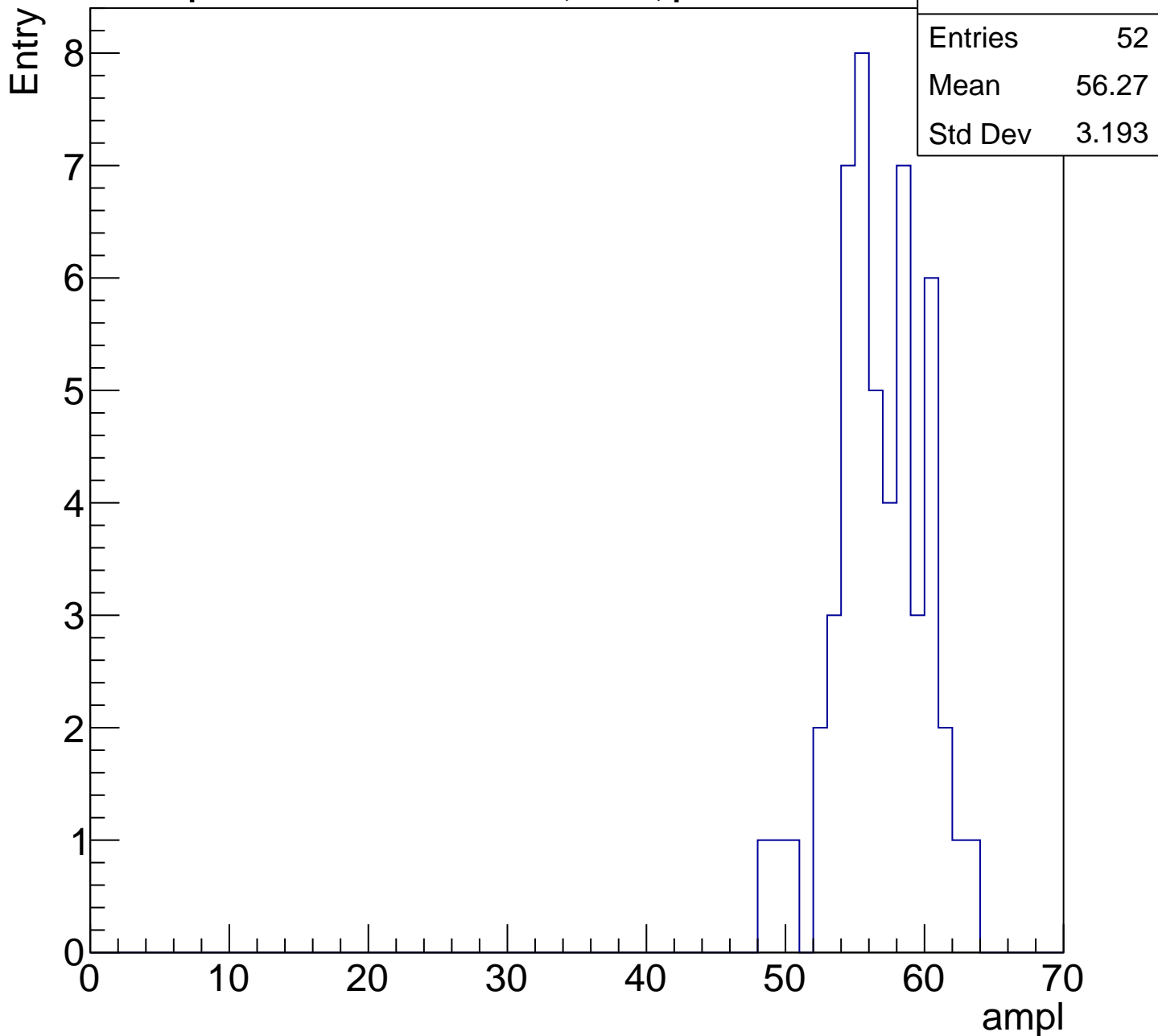
# B1L101S, U9-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2



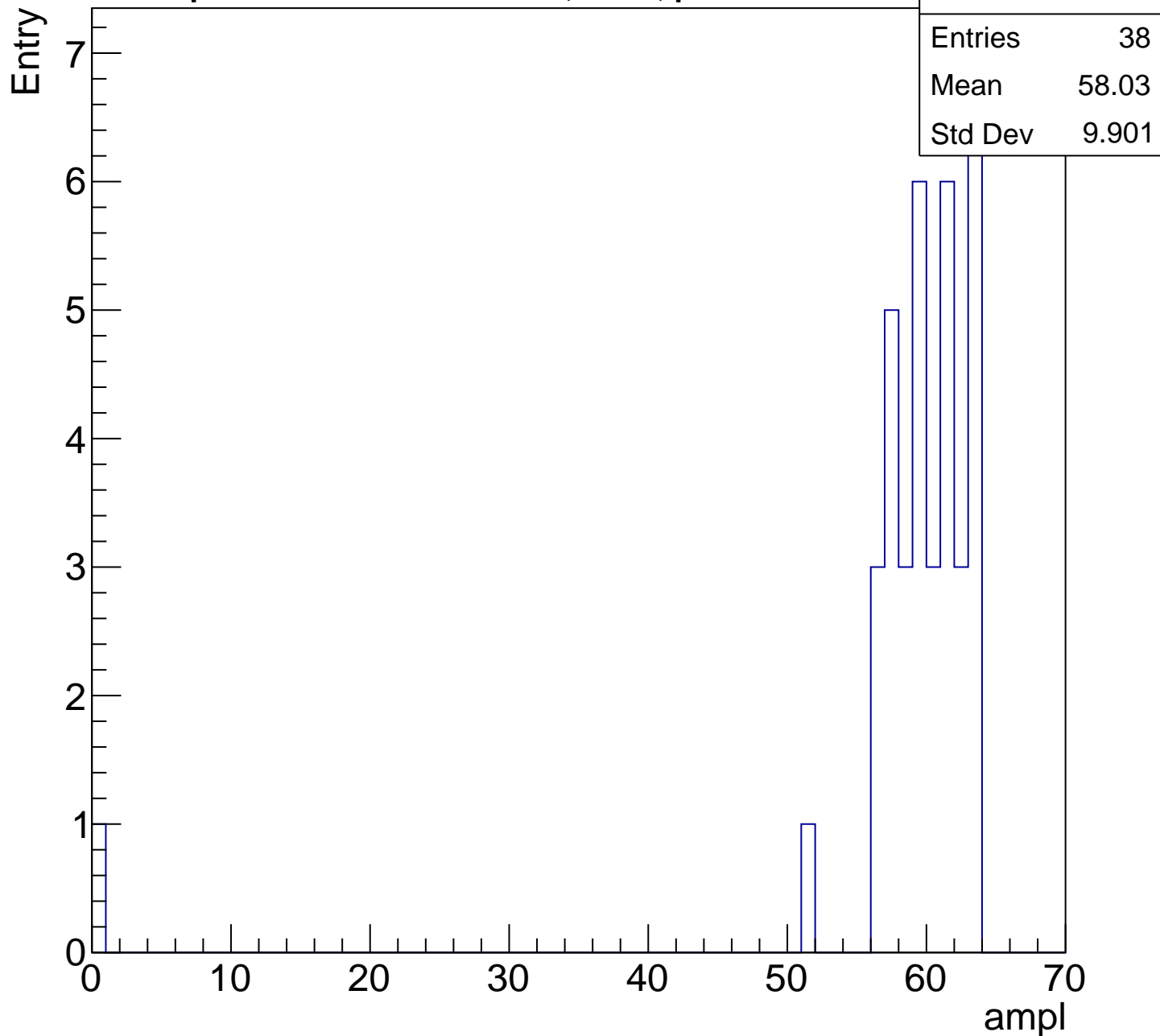
# B1L101S, U9-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

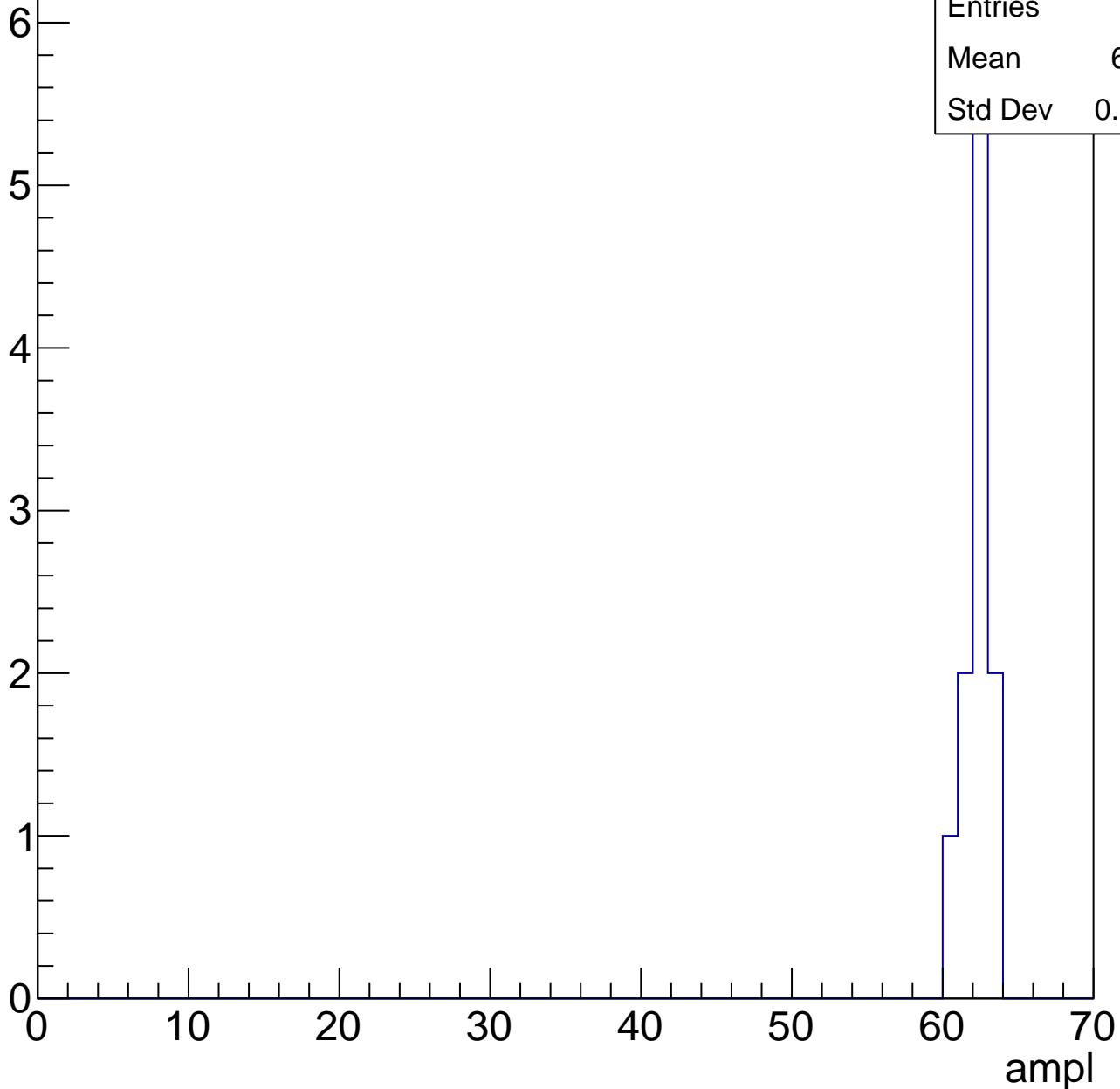


# B1L101S, U9-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	11
Mean	61.82
Std Dev	0.8332





# B1L101S, U9-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U9-ch64, adc0

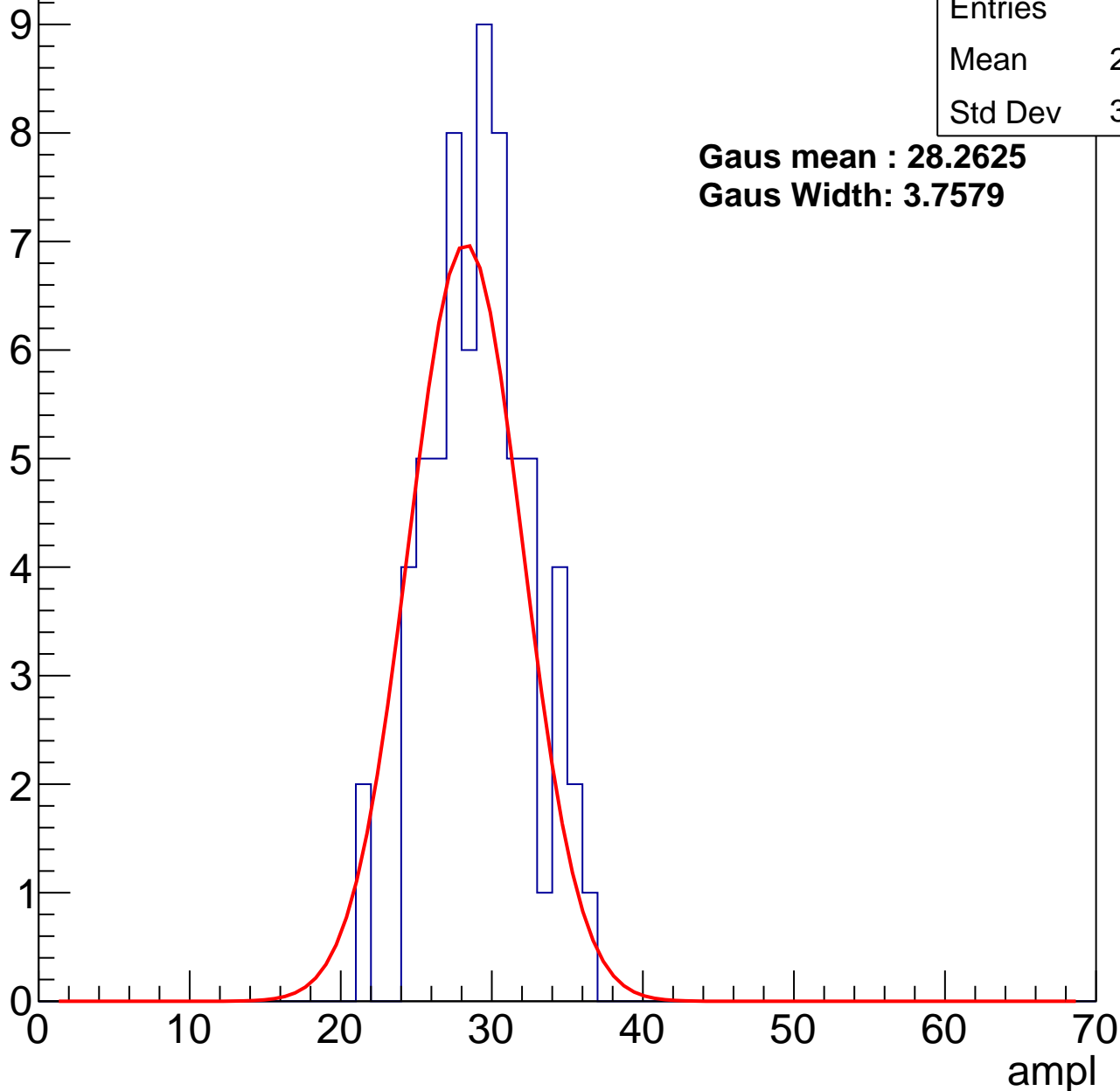
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	28.74
Std Dev	3.274

**Gaus mean : 28.2625**

**Gaus Width: 3.7579**



# B1L101S, U9-ch64, adc1

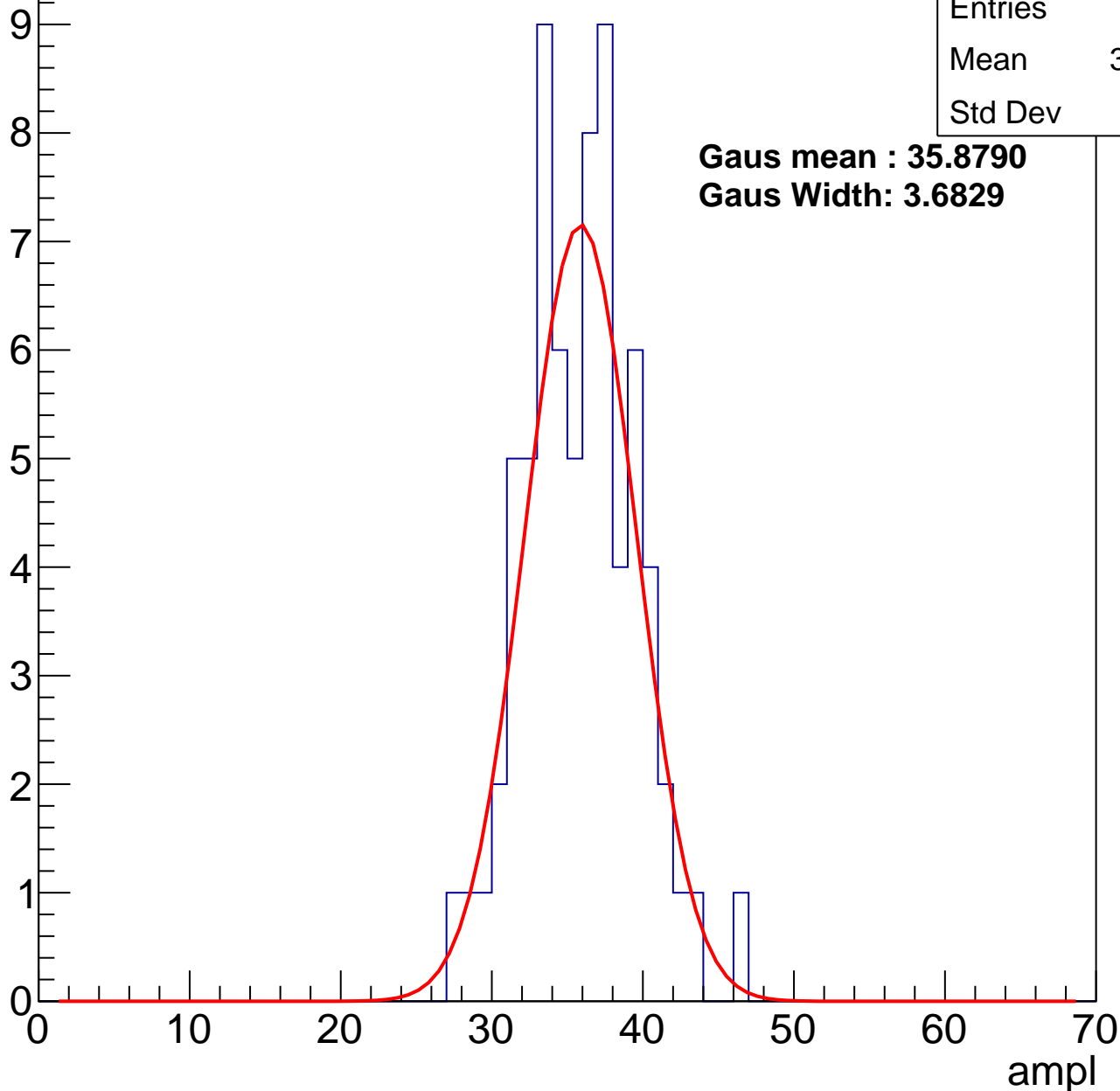
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	35.42
Std Dev	3.63

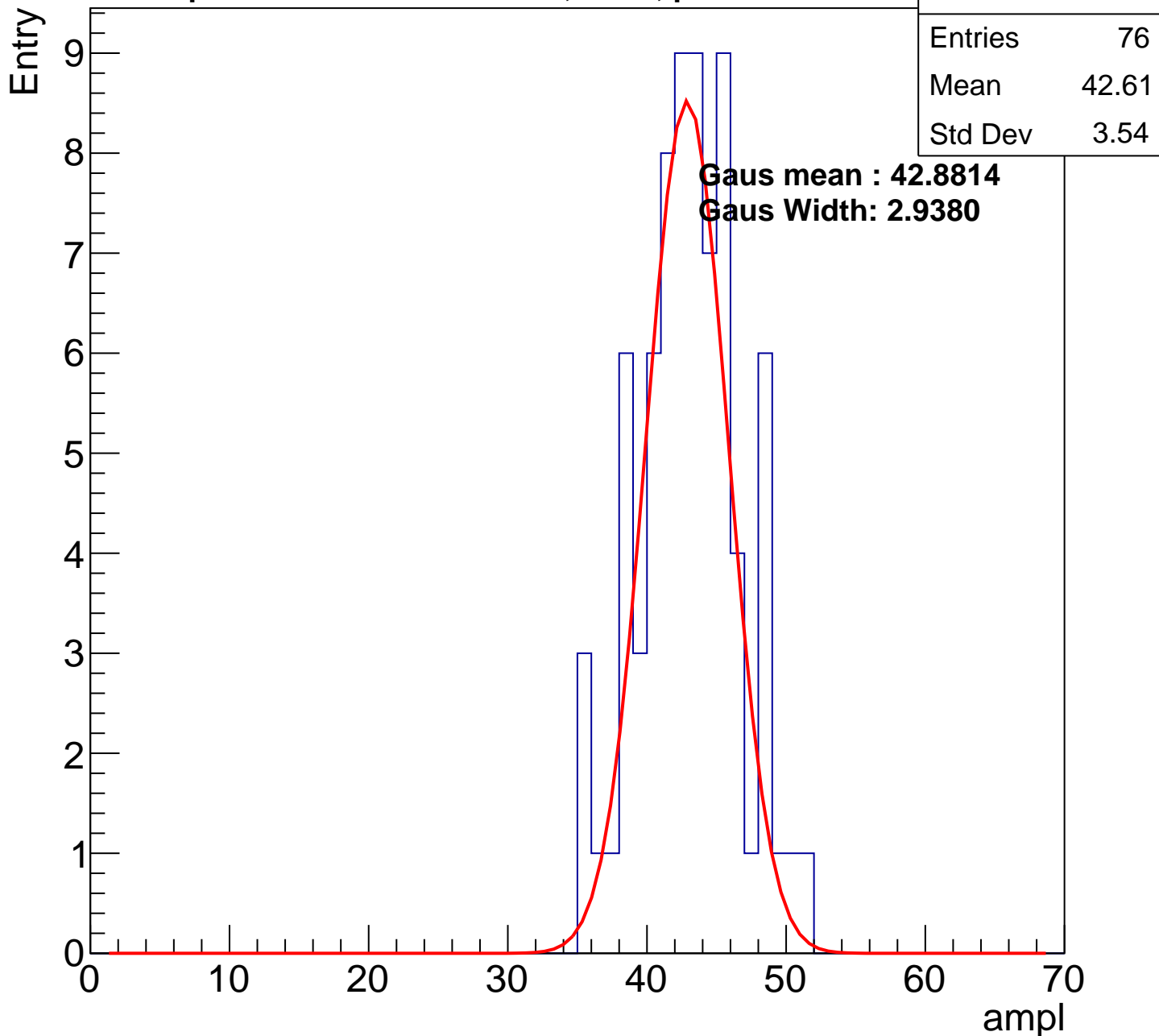
**Gaus mean : 35.8790**

**Gaus Width: 3.6829**



# B1L101S, U9-ch64, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

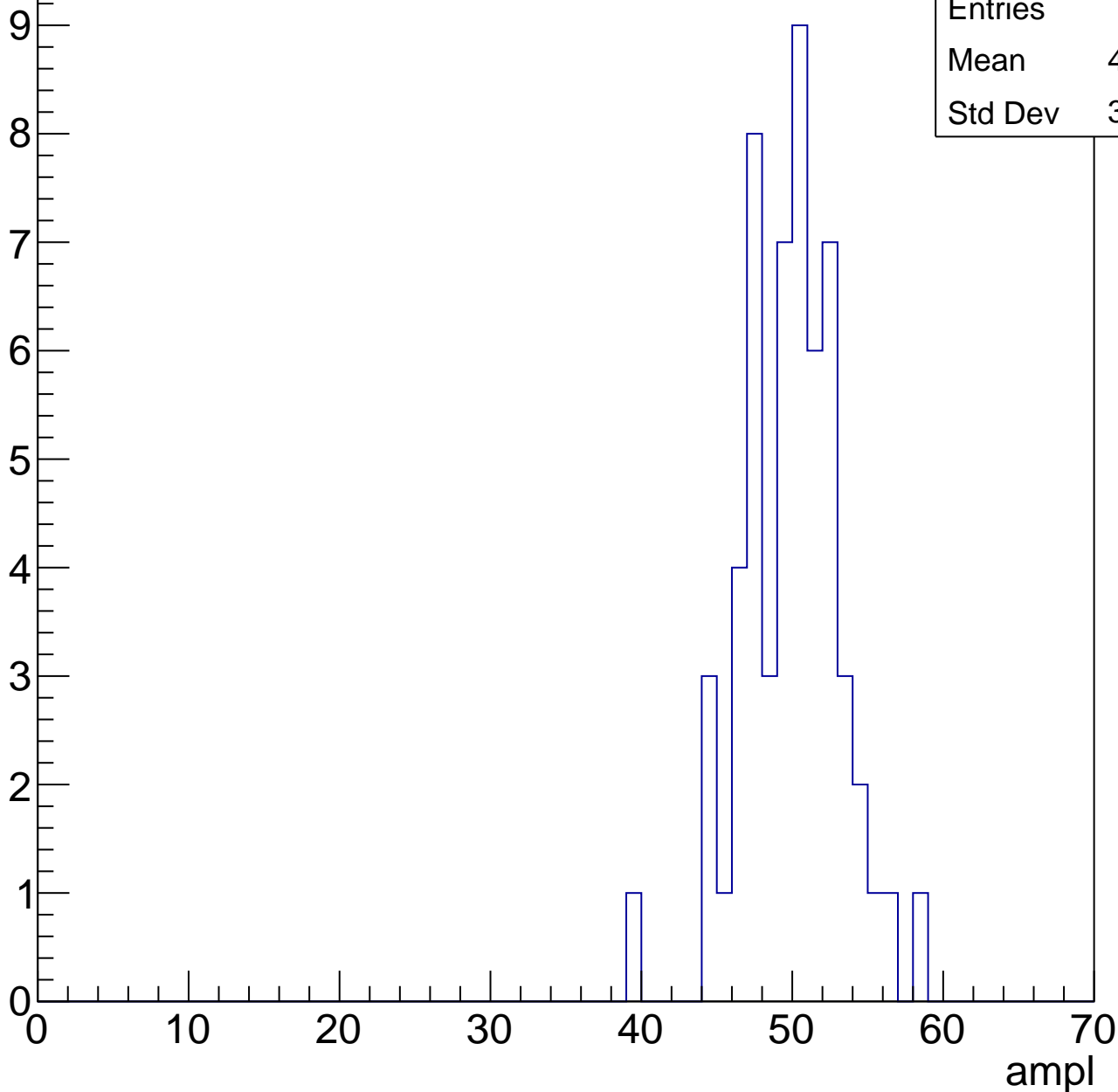


# B1L101S, U9-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

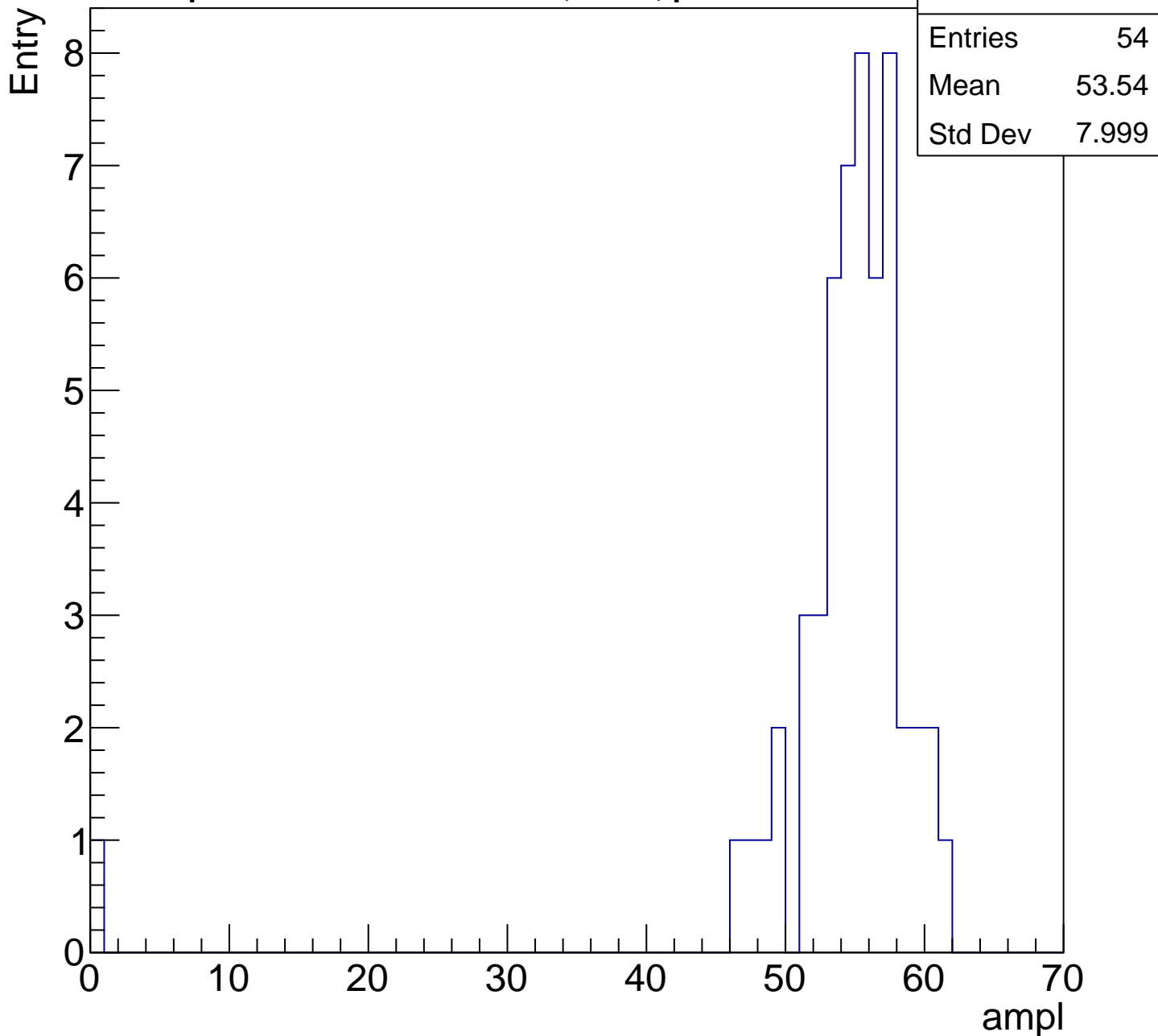
Entry

Entries	57
Mean	49.46
Std Dev	3.272



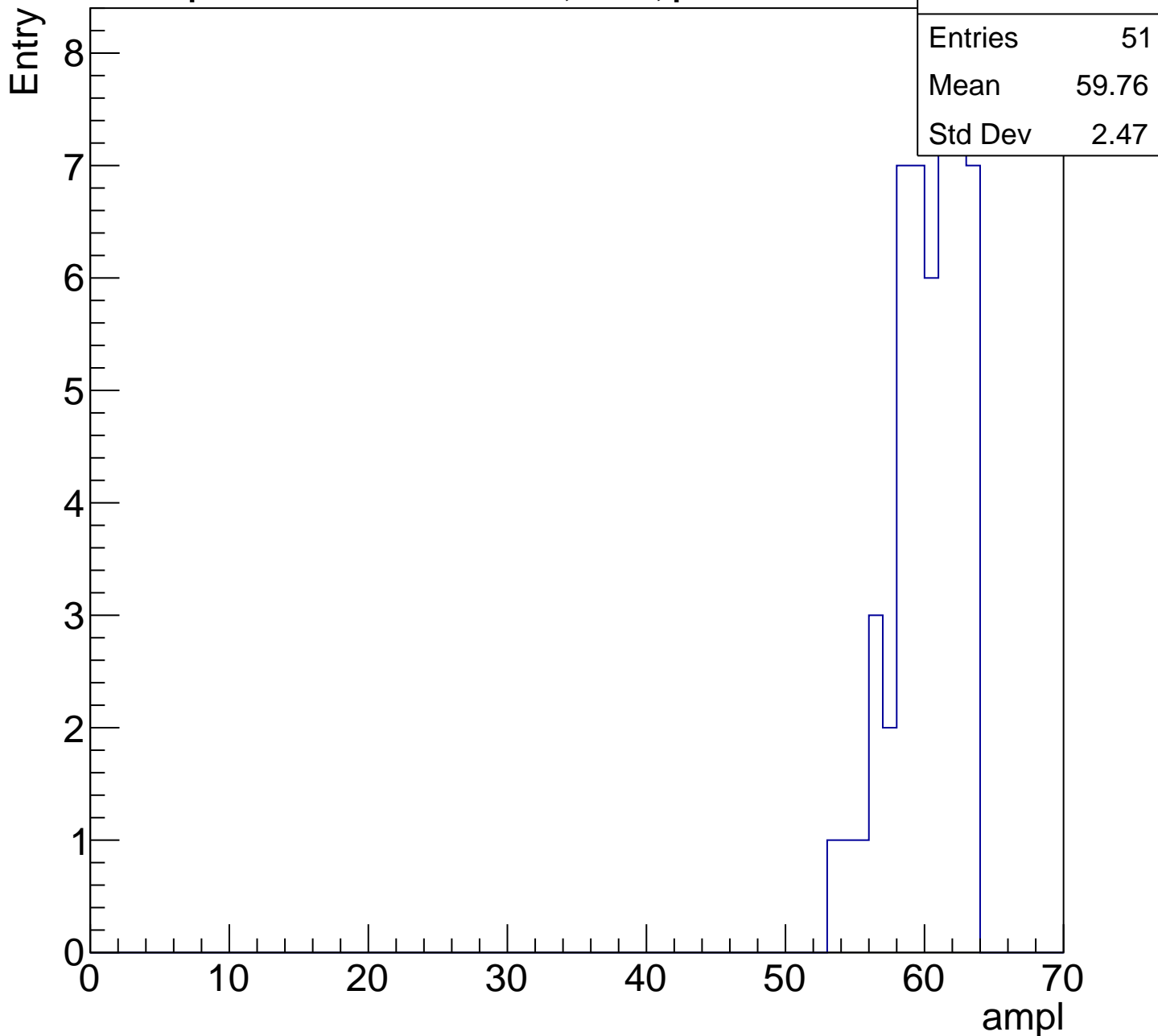
# B1L101S, U9-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch64, adc5

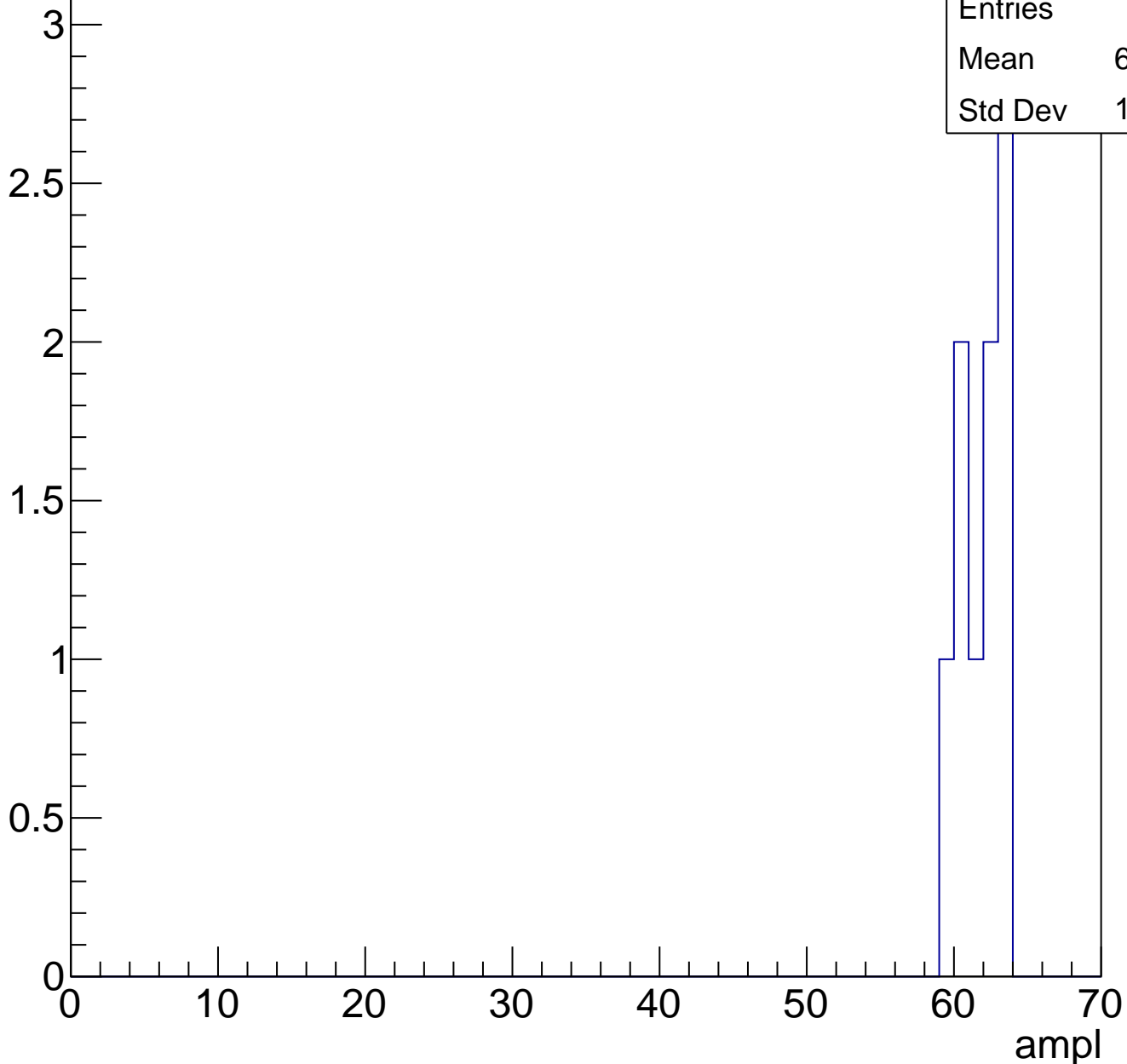
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U9-ch65, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	83
Mean	29.22
Std Dev	5.779

**Gaus mean : 30.4080**

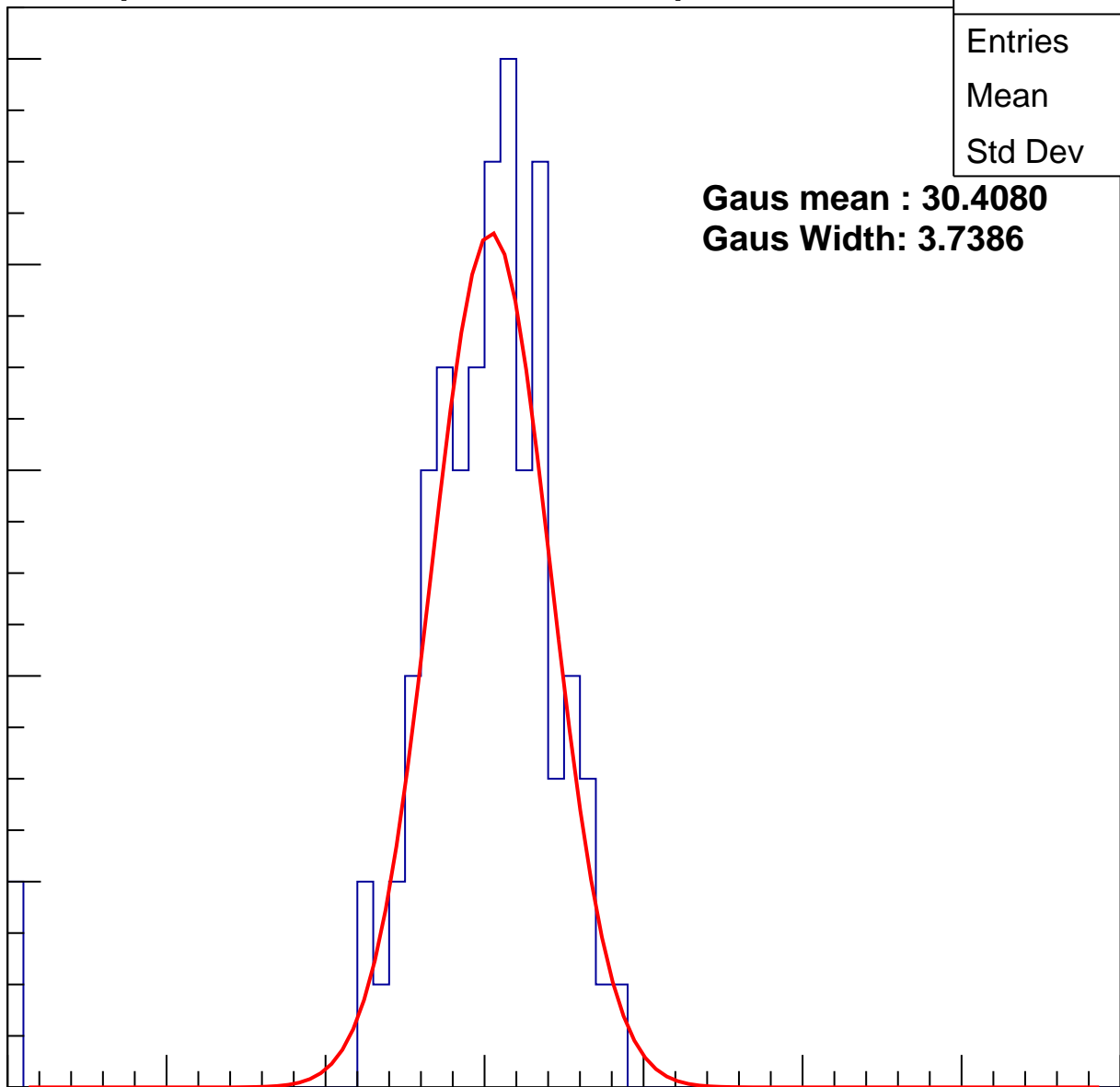
**Gaus Width: 3.7386**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U9-ch65, adc1

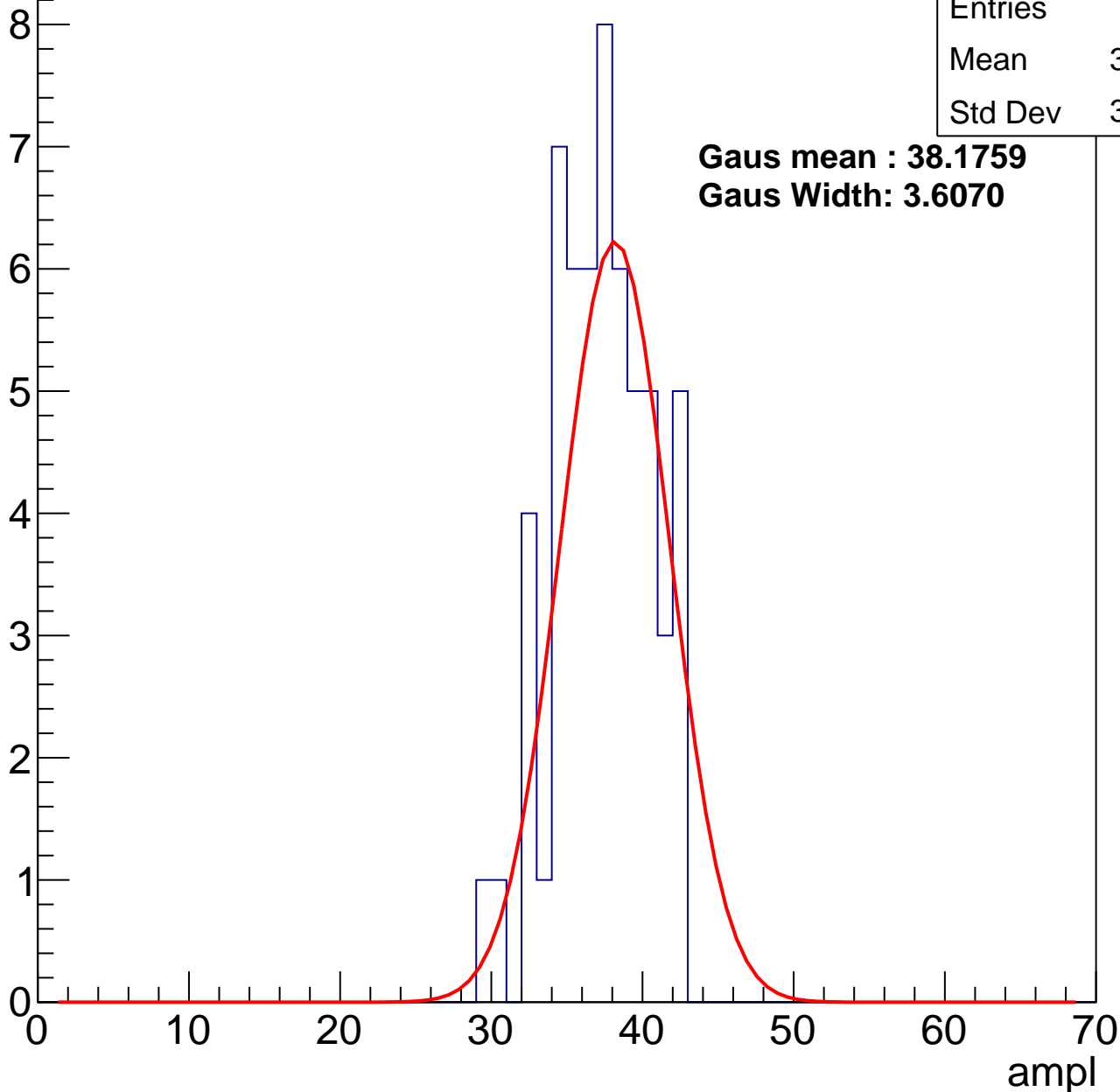
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	36.83
Std Dev	3.119

**Gaus mean : 38.1759**

**Gaus Width: 3.6070**



# B1L101S, U9-ch65, adc2

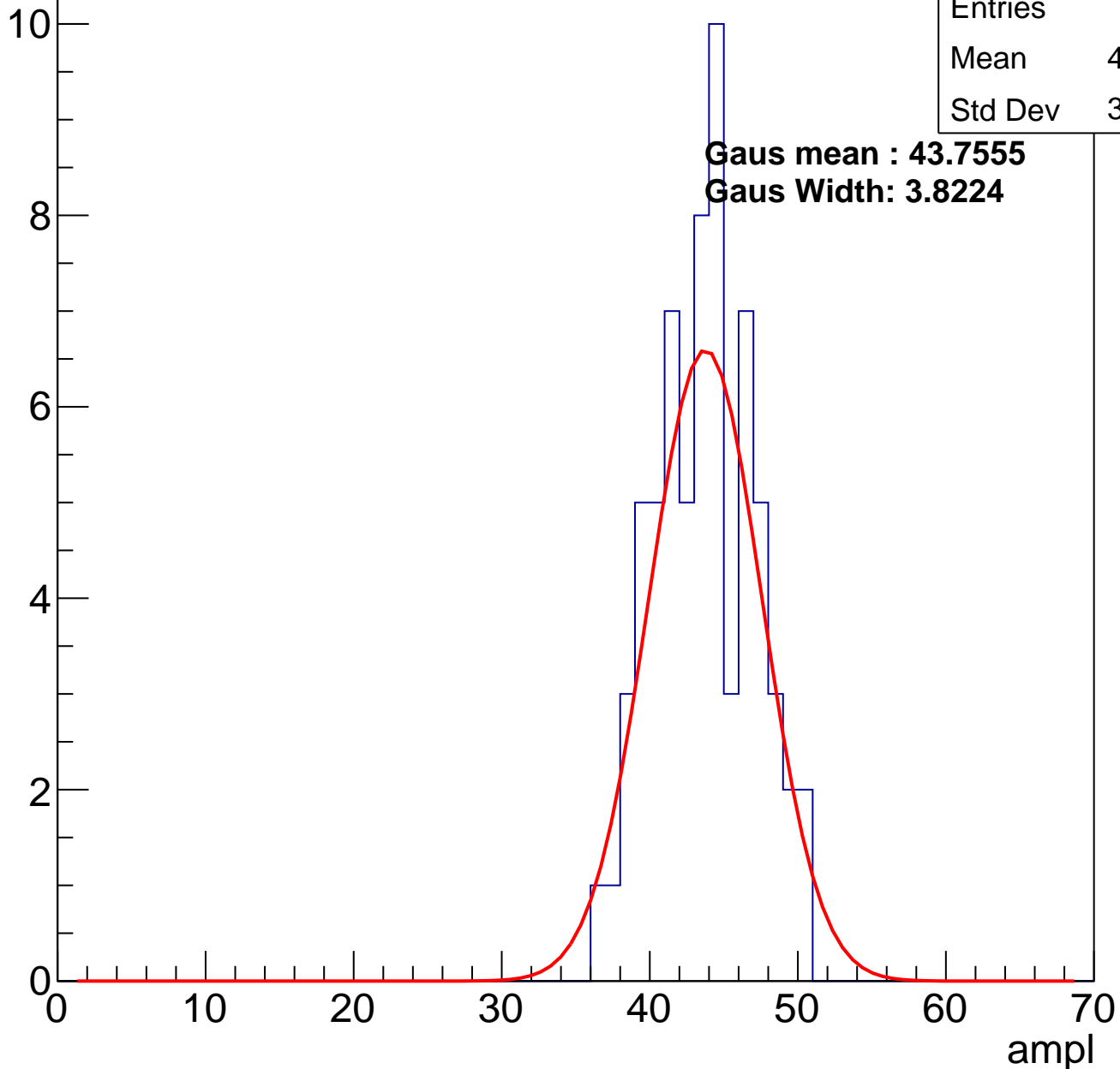
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	67
Mean	43.24
Std Dev	3.288

**Gaus mean : 43.7555**

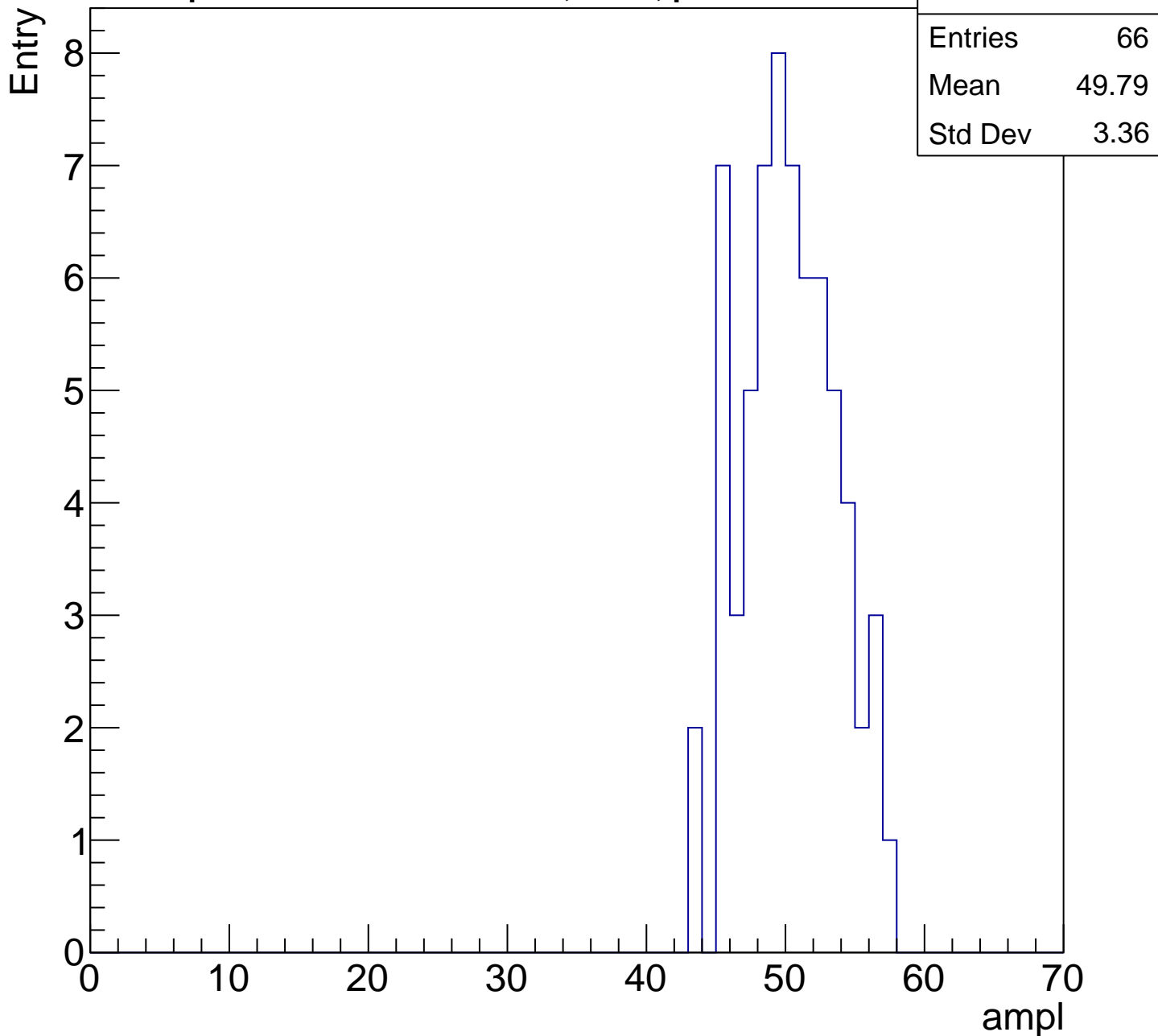
**Gaus Width: 3.8224**

Entry



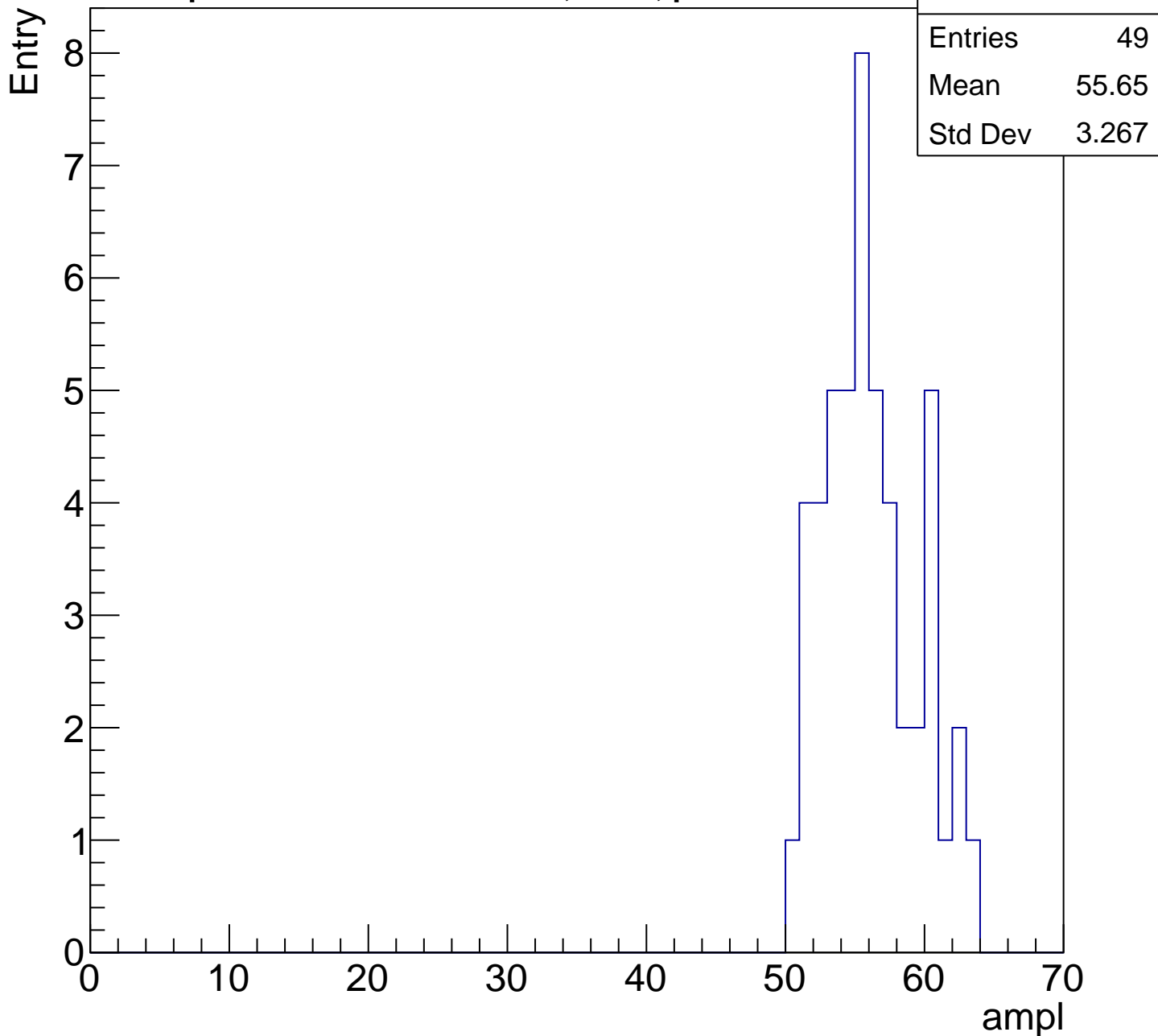
# B1L101S, U9-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch65, adc4

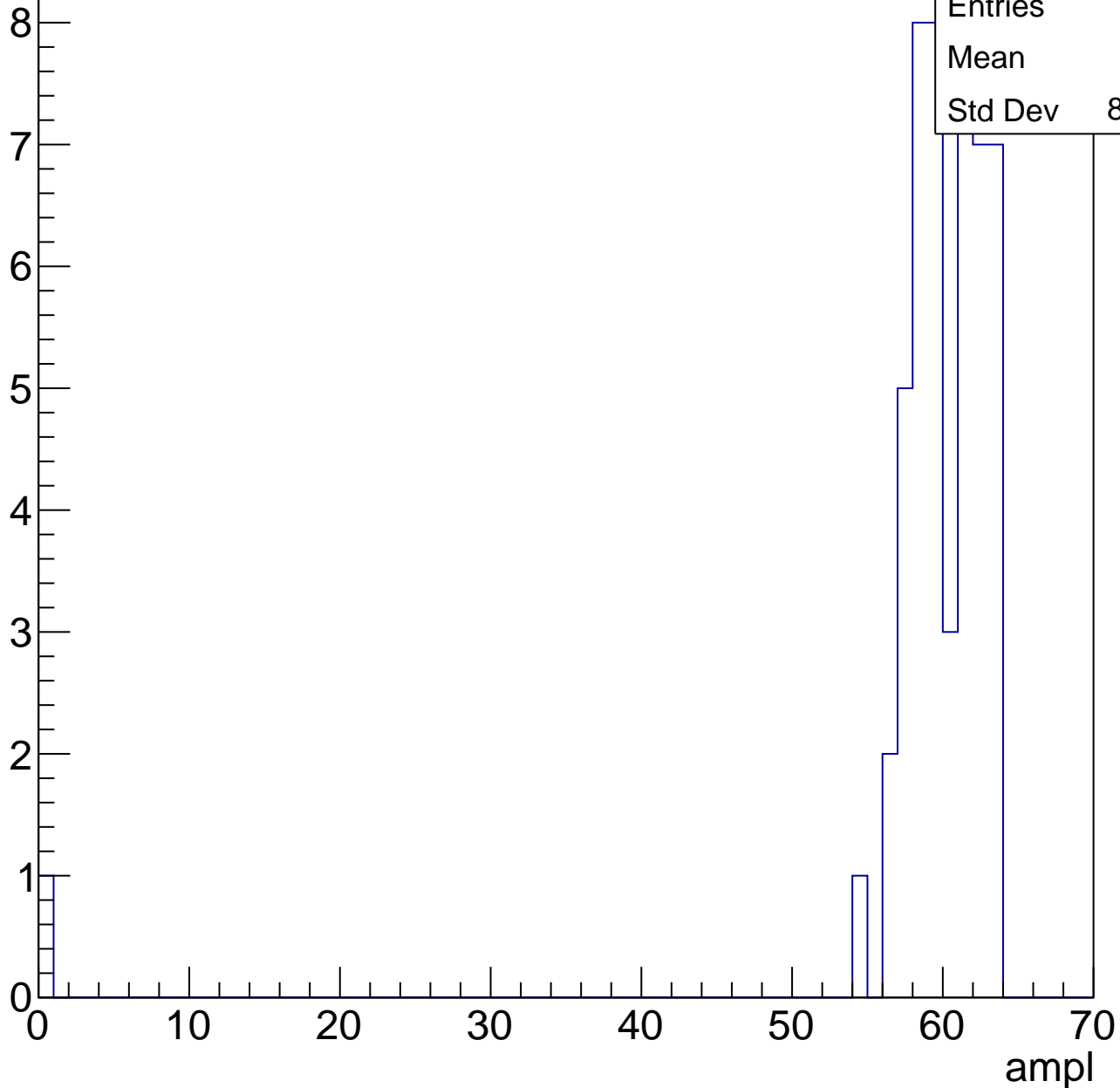
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.5
Std Dev	1.258

ampl



# B1L101S, U9-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch66, adc0

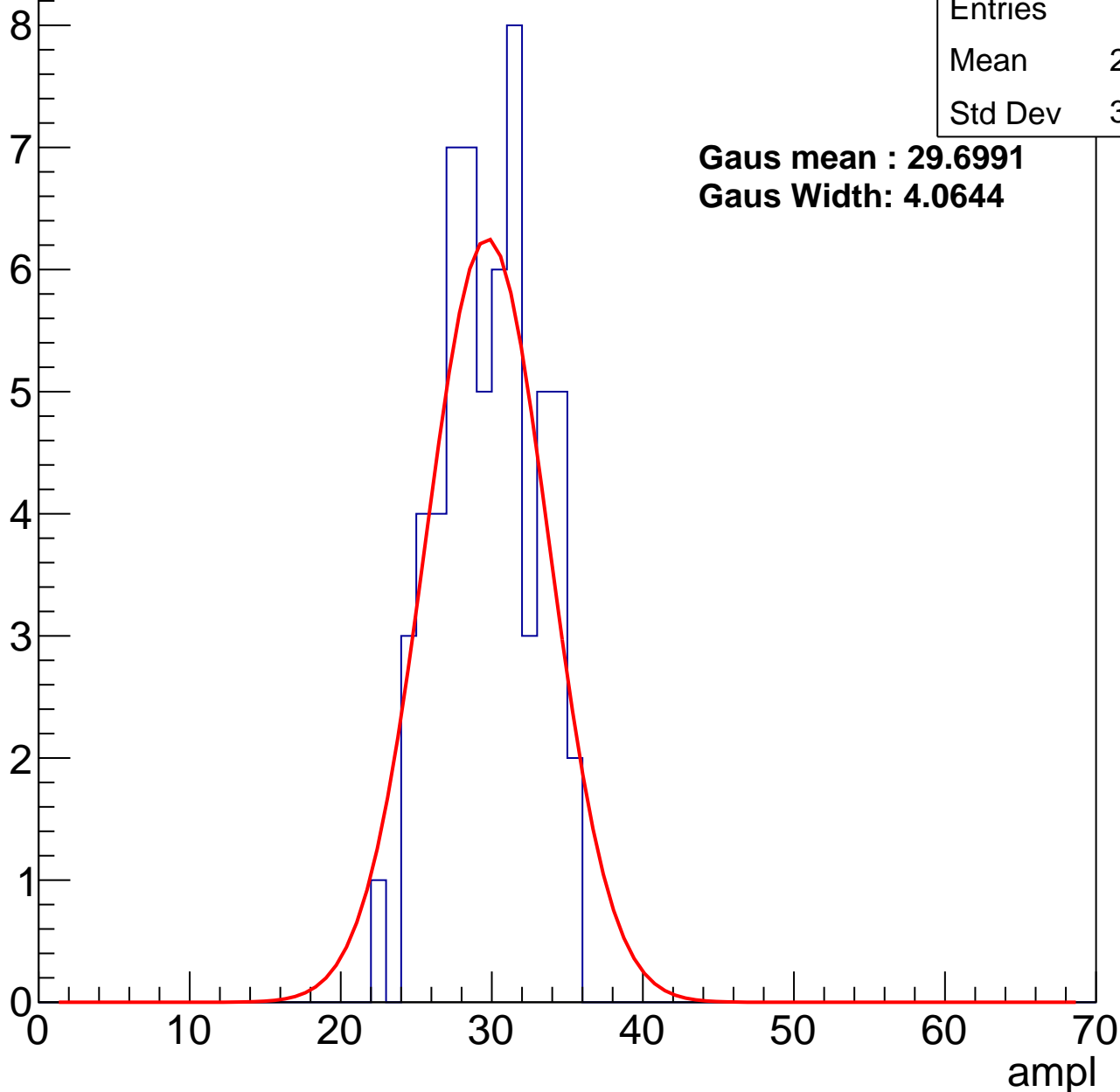
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	29.28
Std Dev	3.152

**Gaus mean : 29.6991**

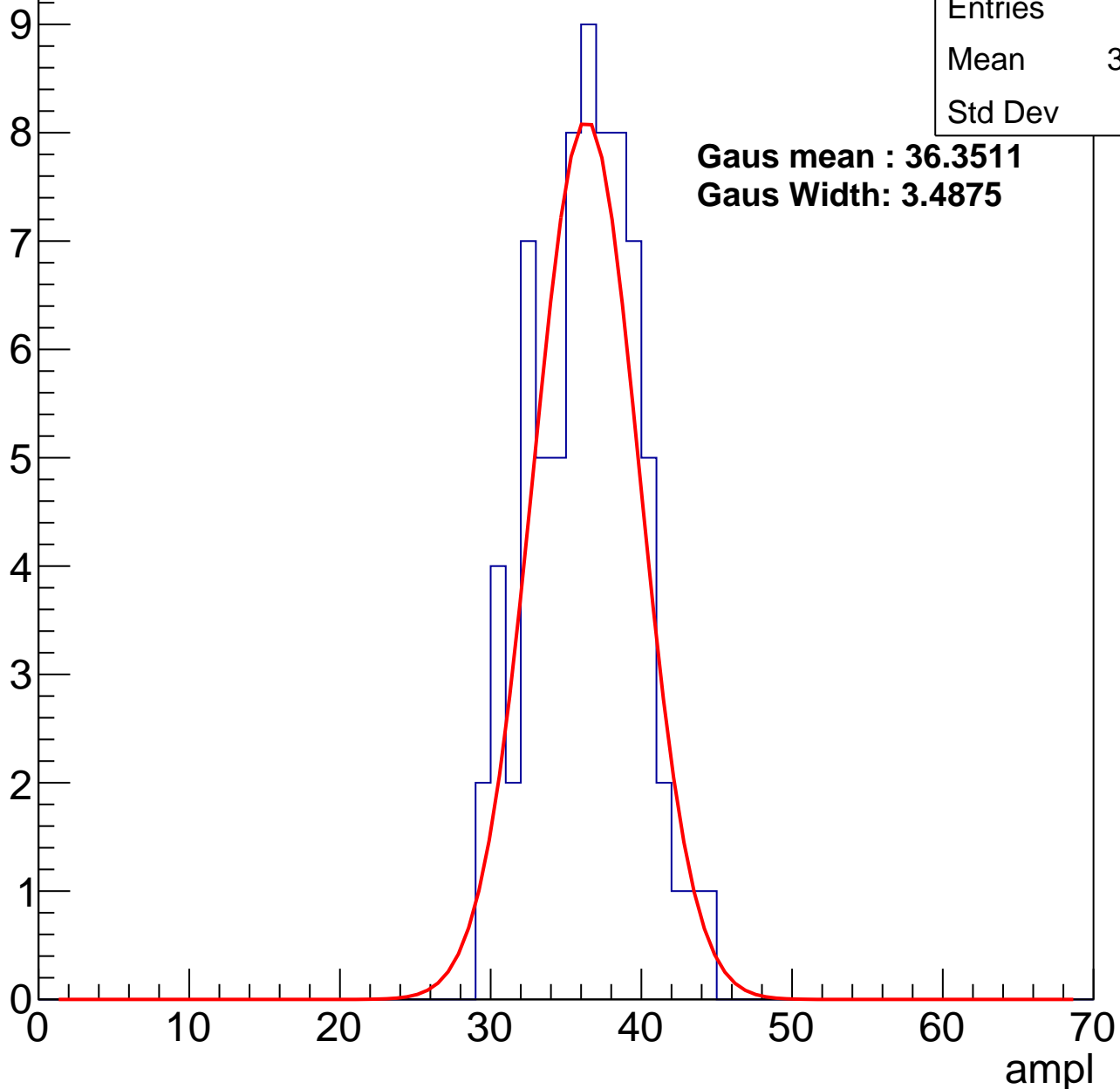
**Gaus Width: 4.0644**



# B1L101S, U9-ch66, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	75
Mean	35.83
Std Dev	3.38

# B1L101S, U9-ch66, adc2

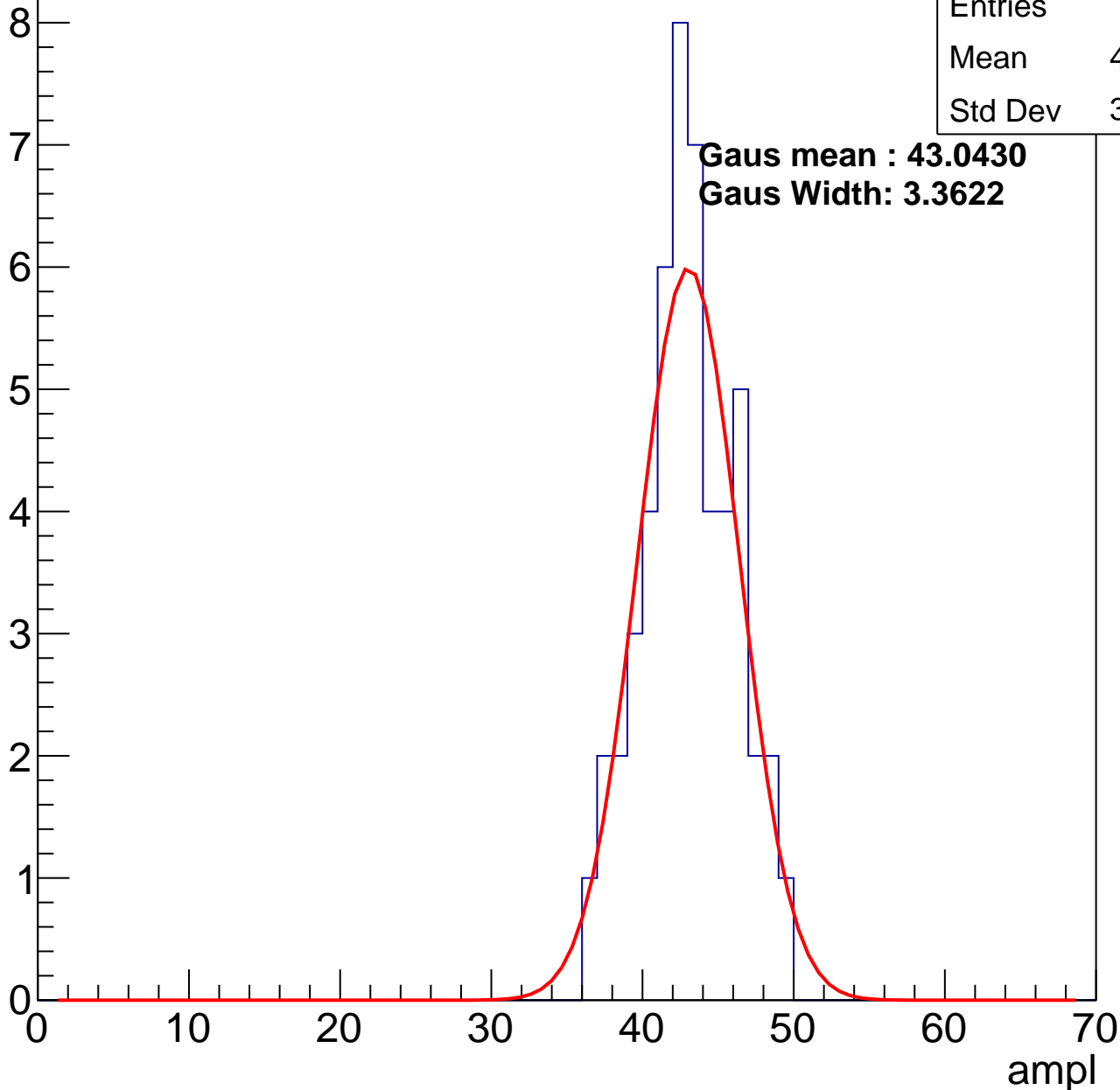
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	42.57
Std Dev	3.005

**Gaus mean : 43.0430**

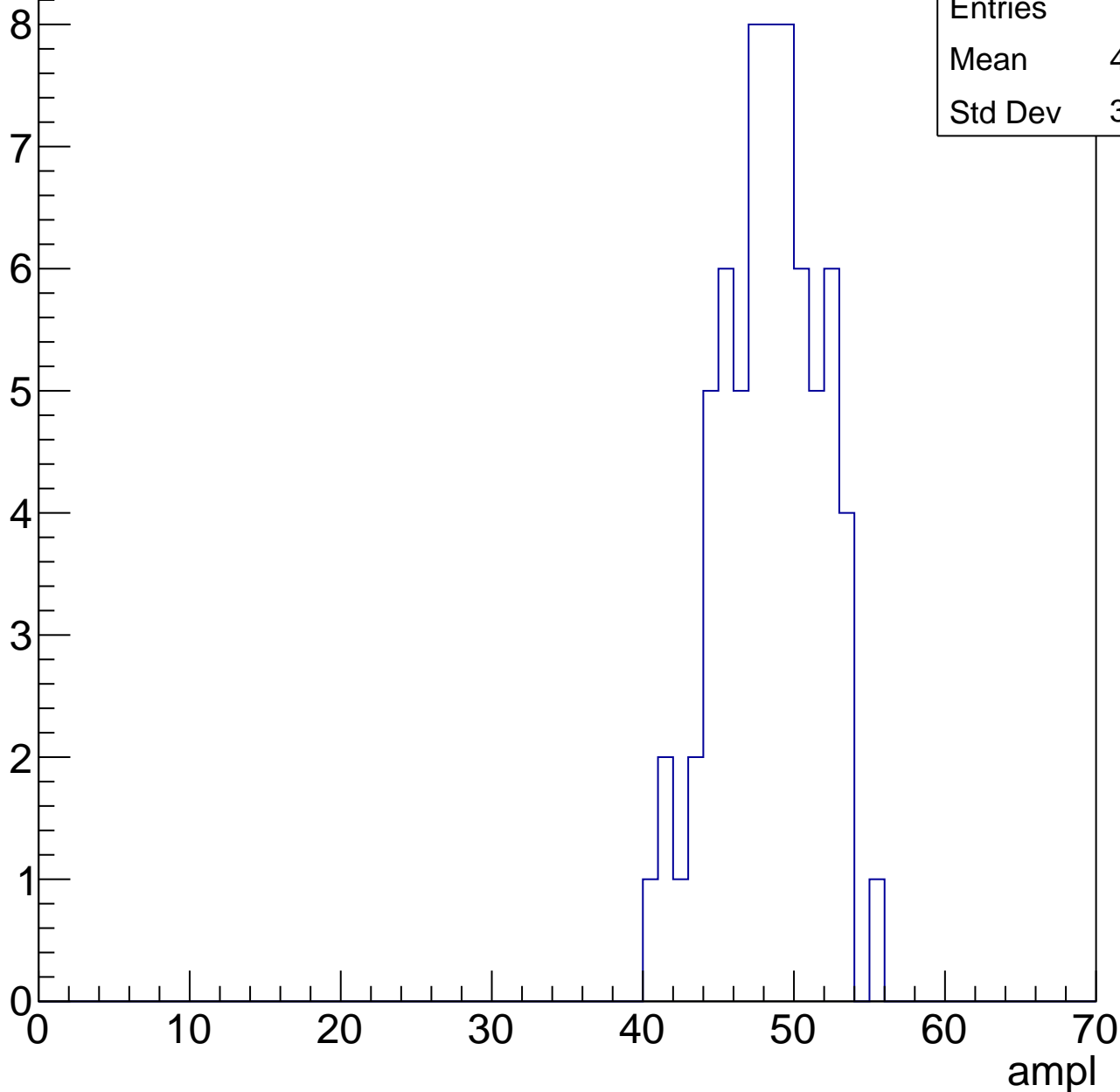
**Gaus Width: 3.3622**



# B1L101S, U9-ch66, adc3

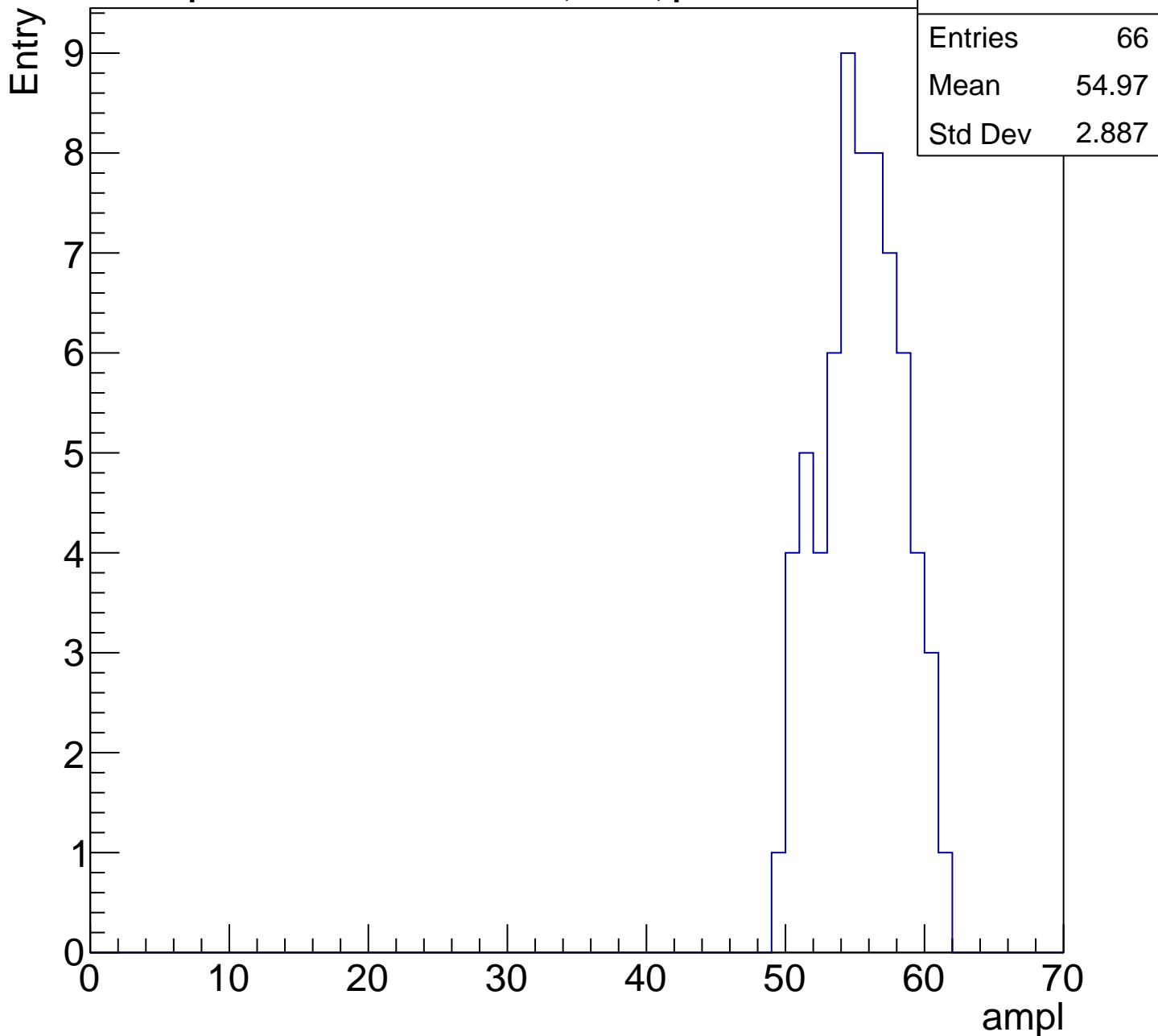
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch66, adc4

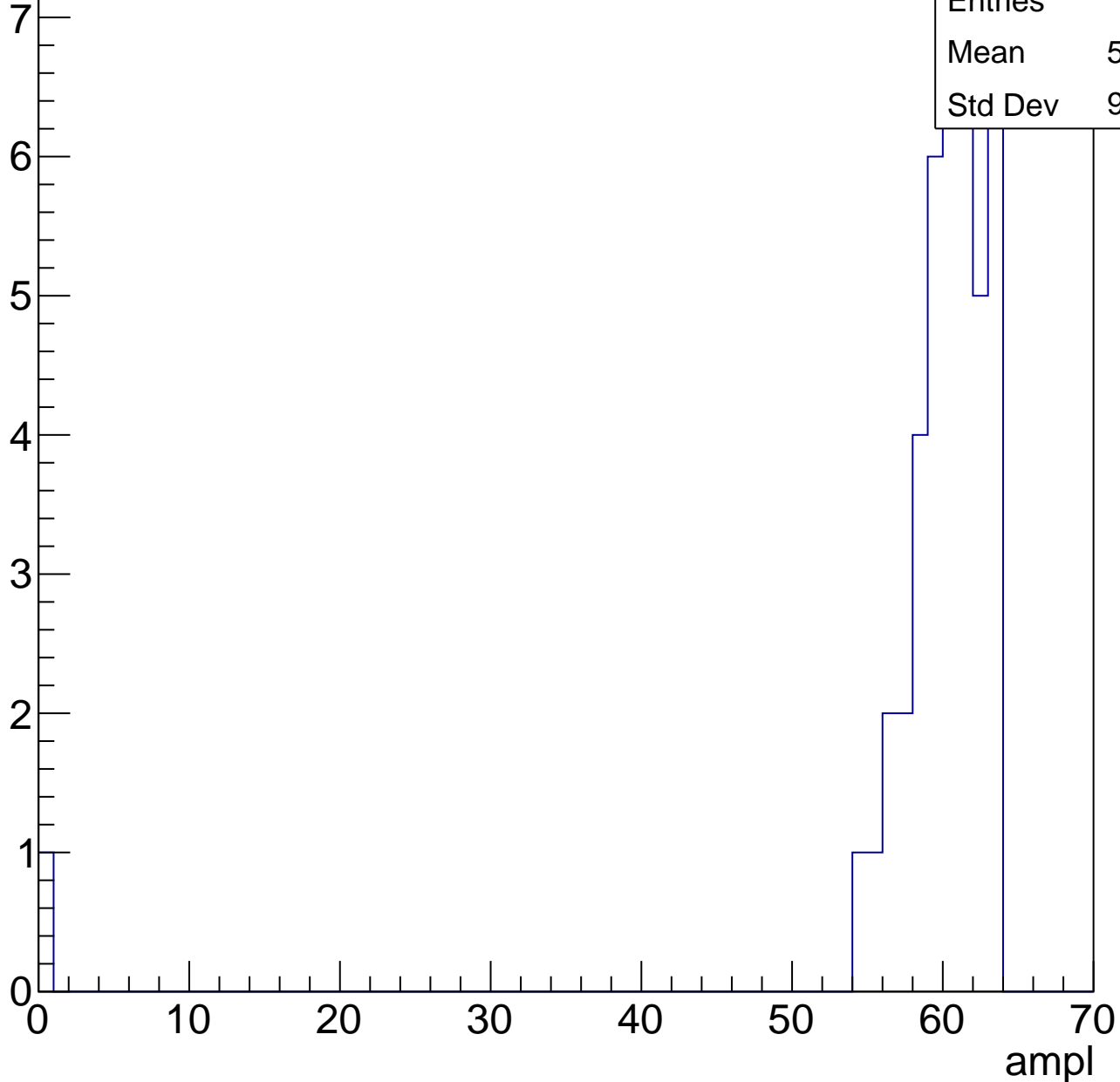
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

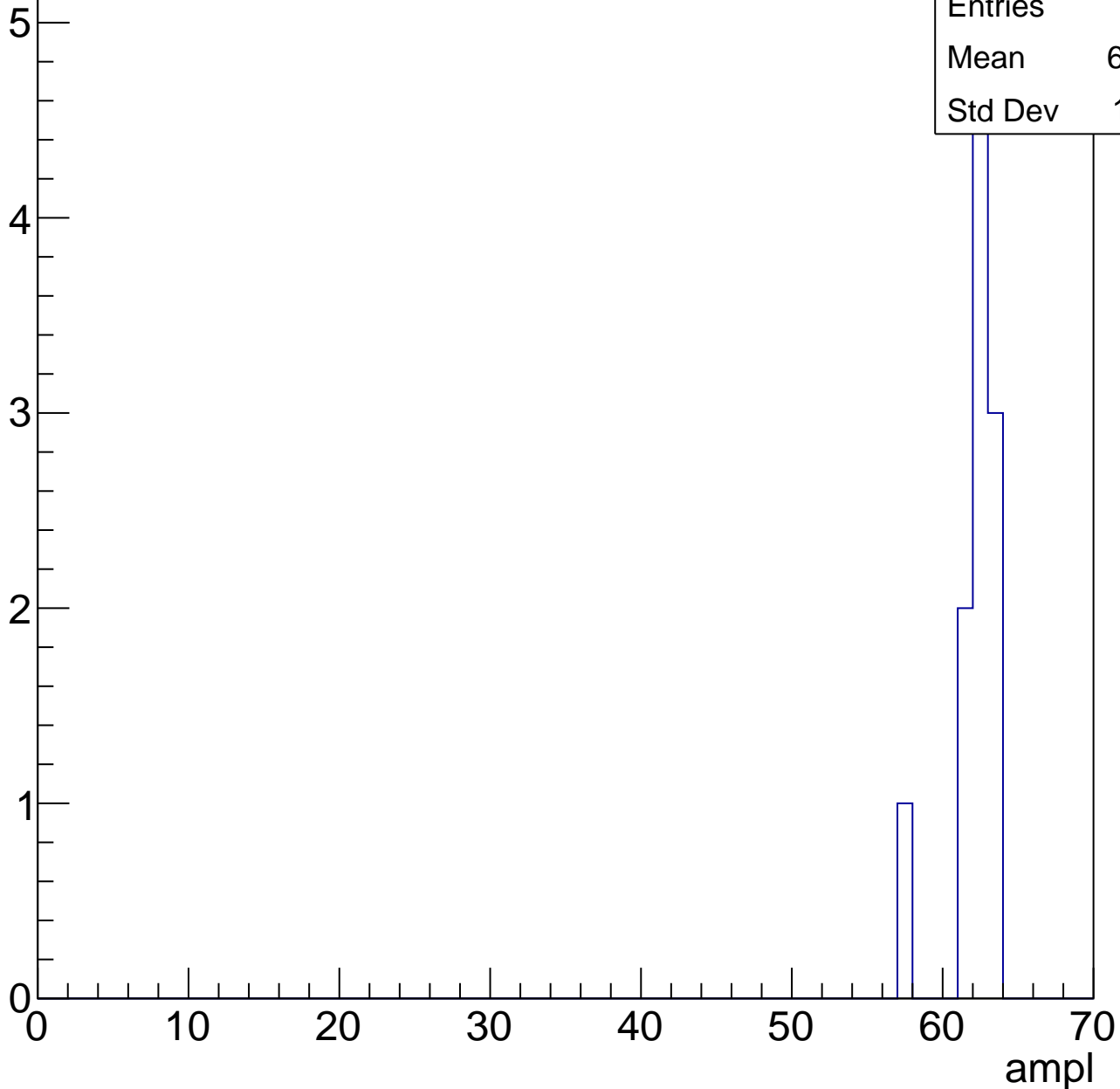


# B1L101S, U9-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	11
Mean	61.64
Std Dev	1.611





# B1L101S, U9-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	7
Std Dev	9.899

# B1L101S, U9-ch67, adc0

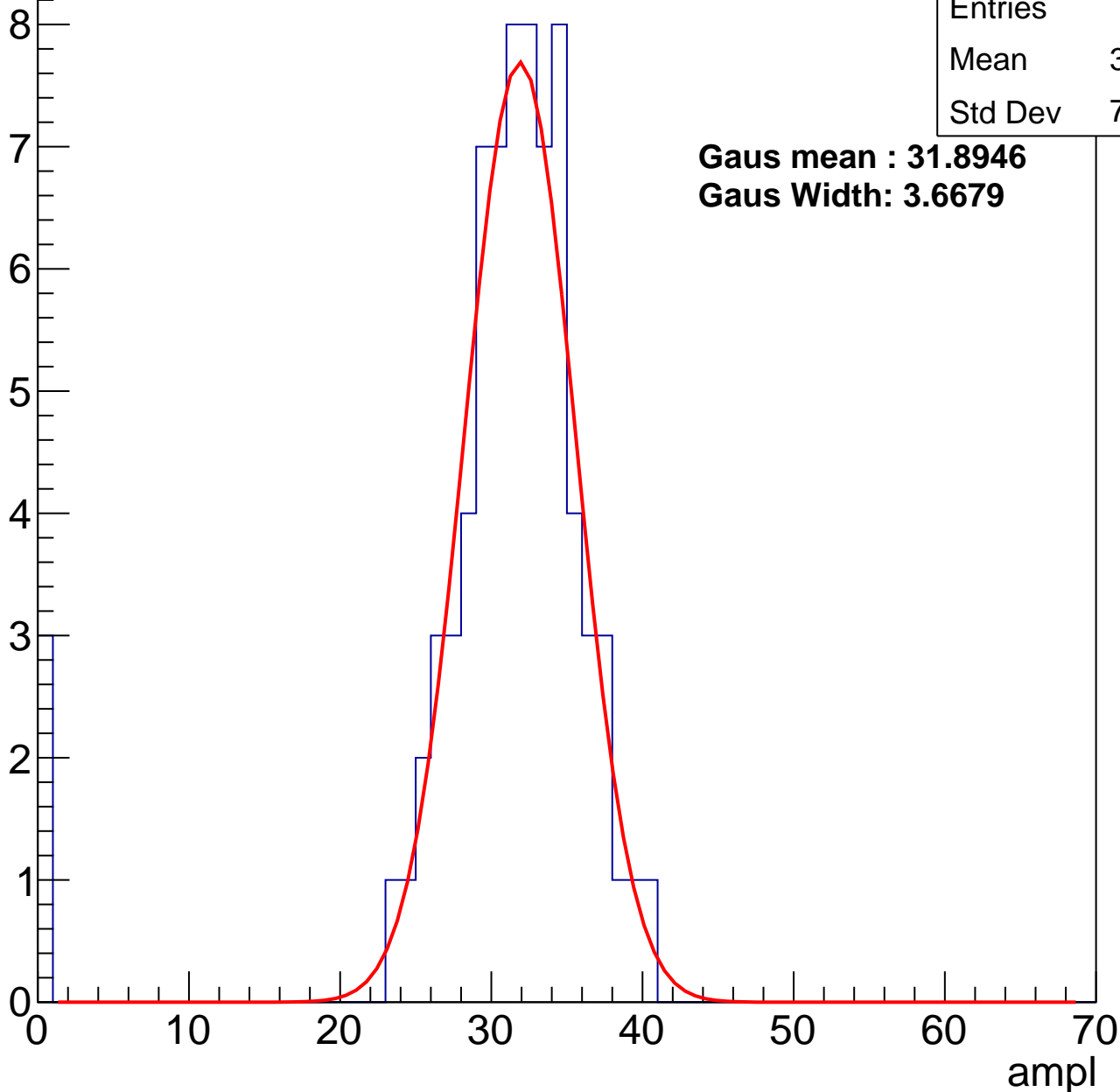
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	30.19
Std Dev	7.082

**Gaus mean : 31.8946**

**Gaus Width: 3.6679**



# B1L101S, U9-ch67, adc1

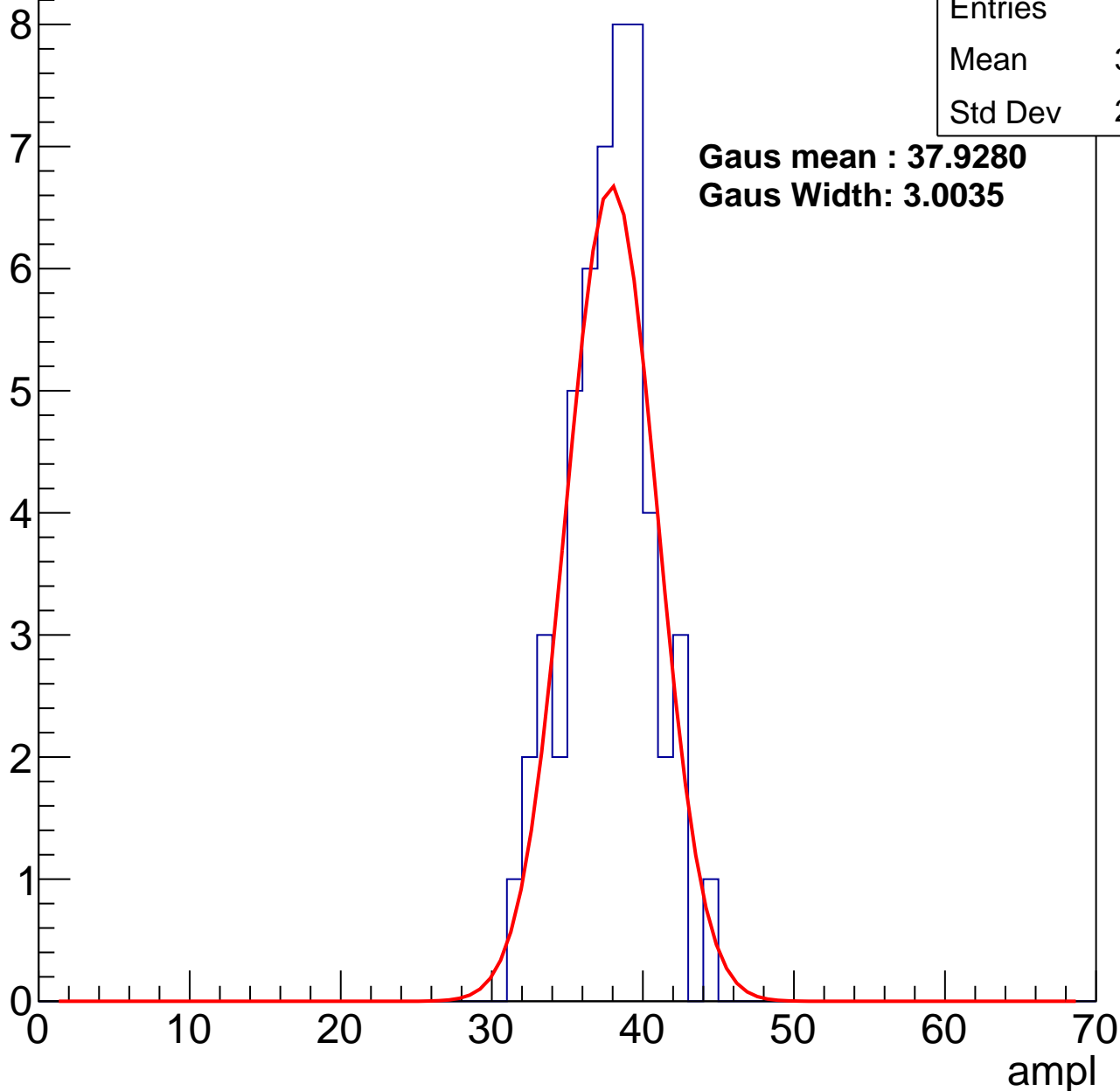
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	37.31
Std Dev	2.791

**Gaus mean : 37.9280**

**Gaus Width: 3.0035**



# B1L101S, U9-ch67, adc2

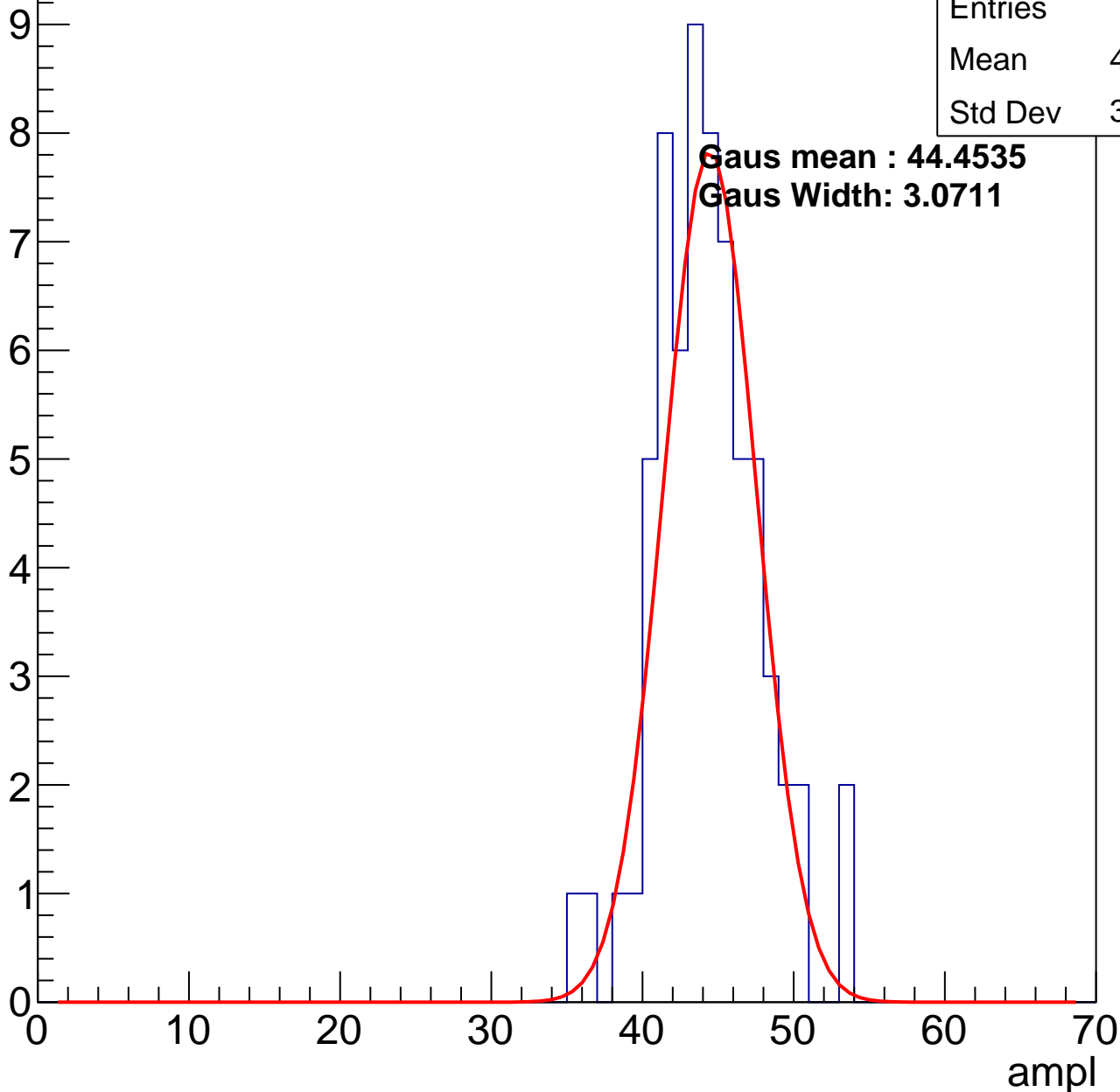
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	43.86
Std Dev	3.468

**Gaus mean : 44.4535**

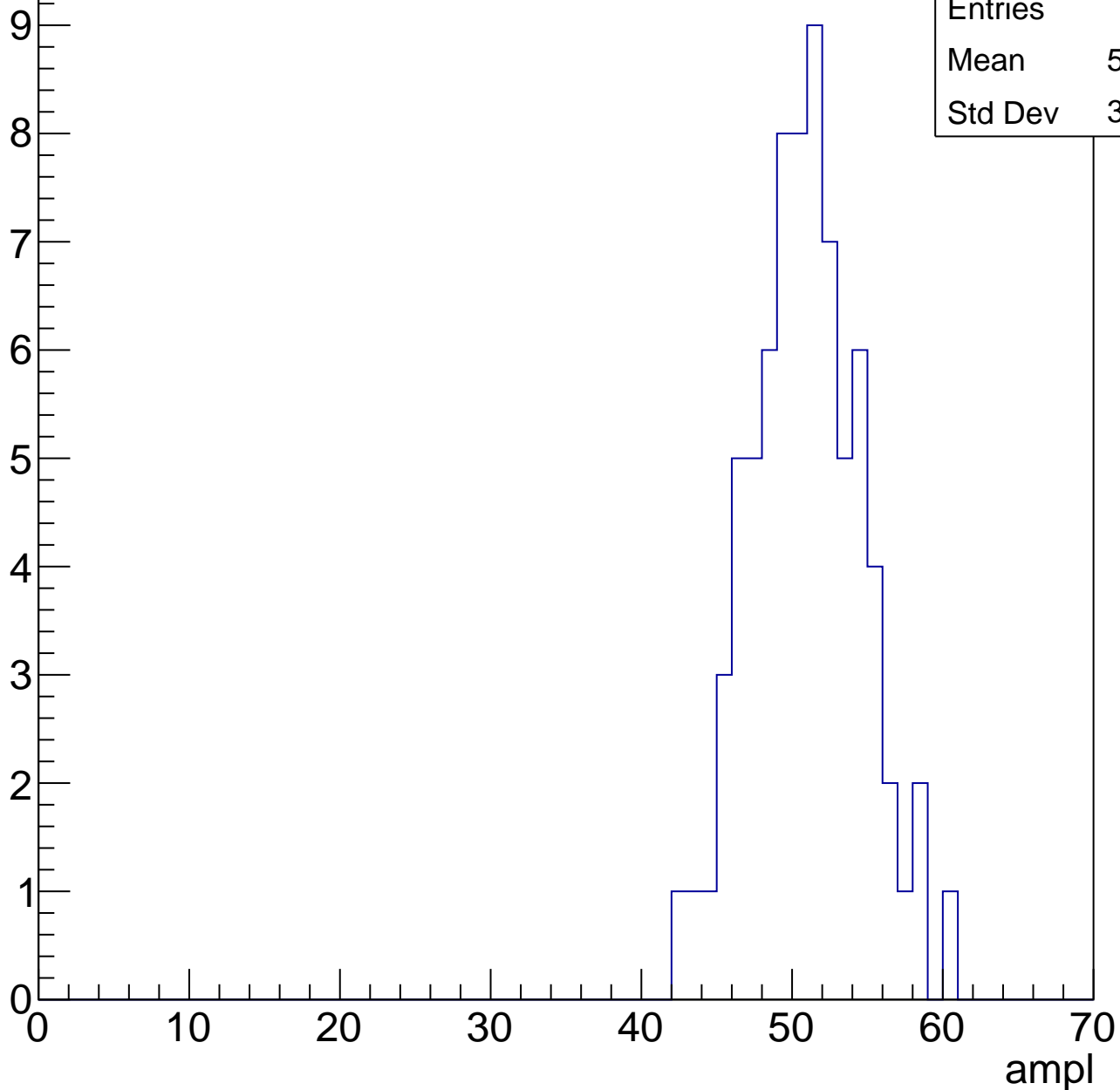
**Gaus Width: 3.0711**



# B1L101S, U9-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



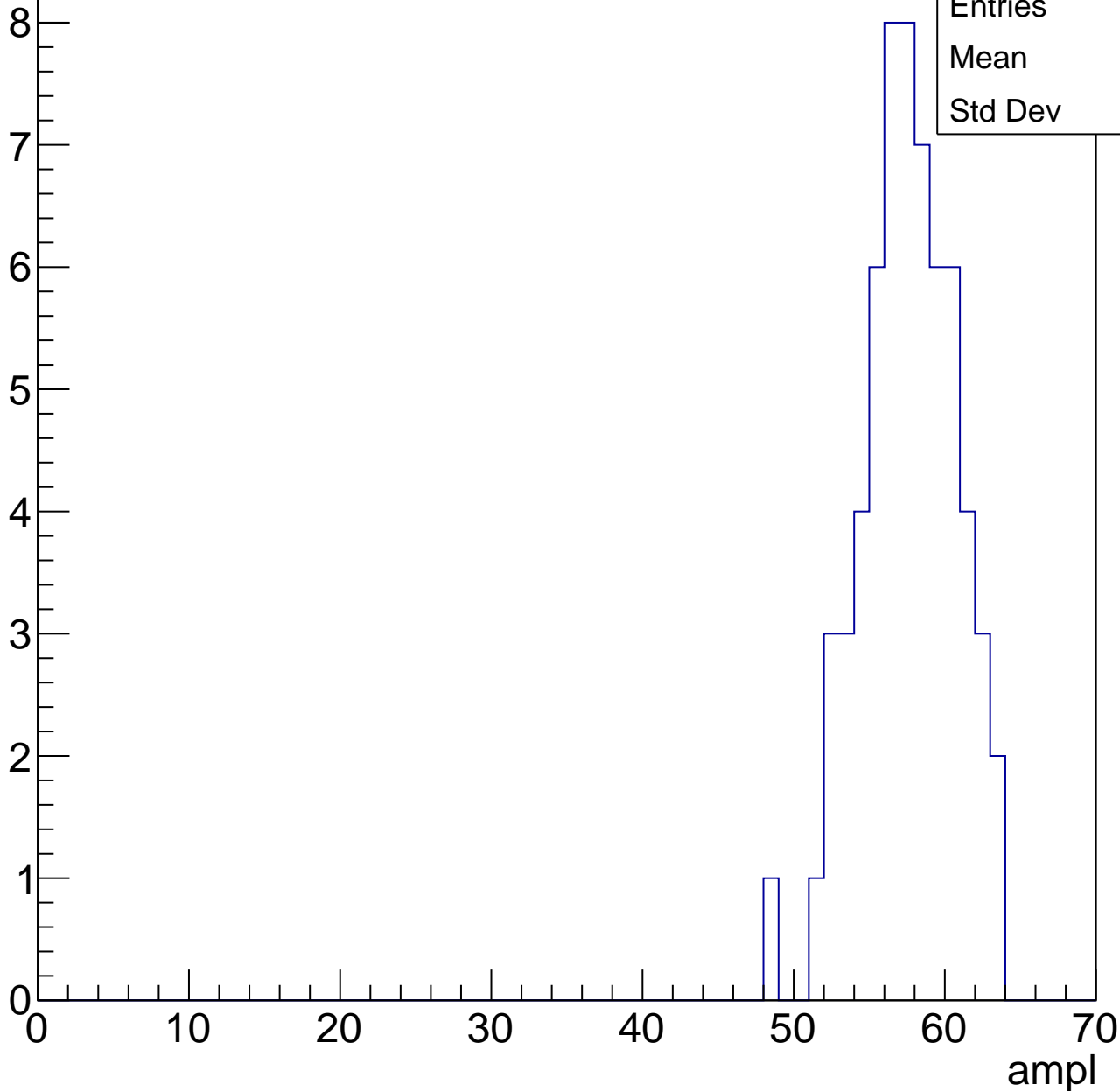
Entries	75
Mean	50.48
Std Dev	3.635

# B1L101S, U9-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	57.1
Std Dev	3.12



# B1L101S, U9-ch67, adc5

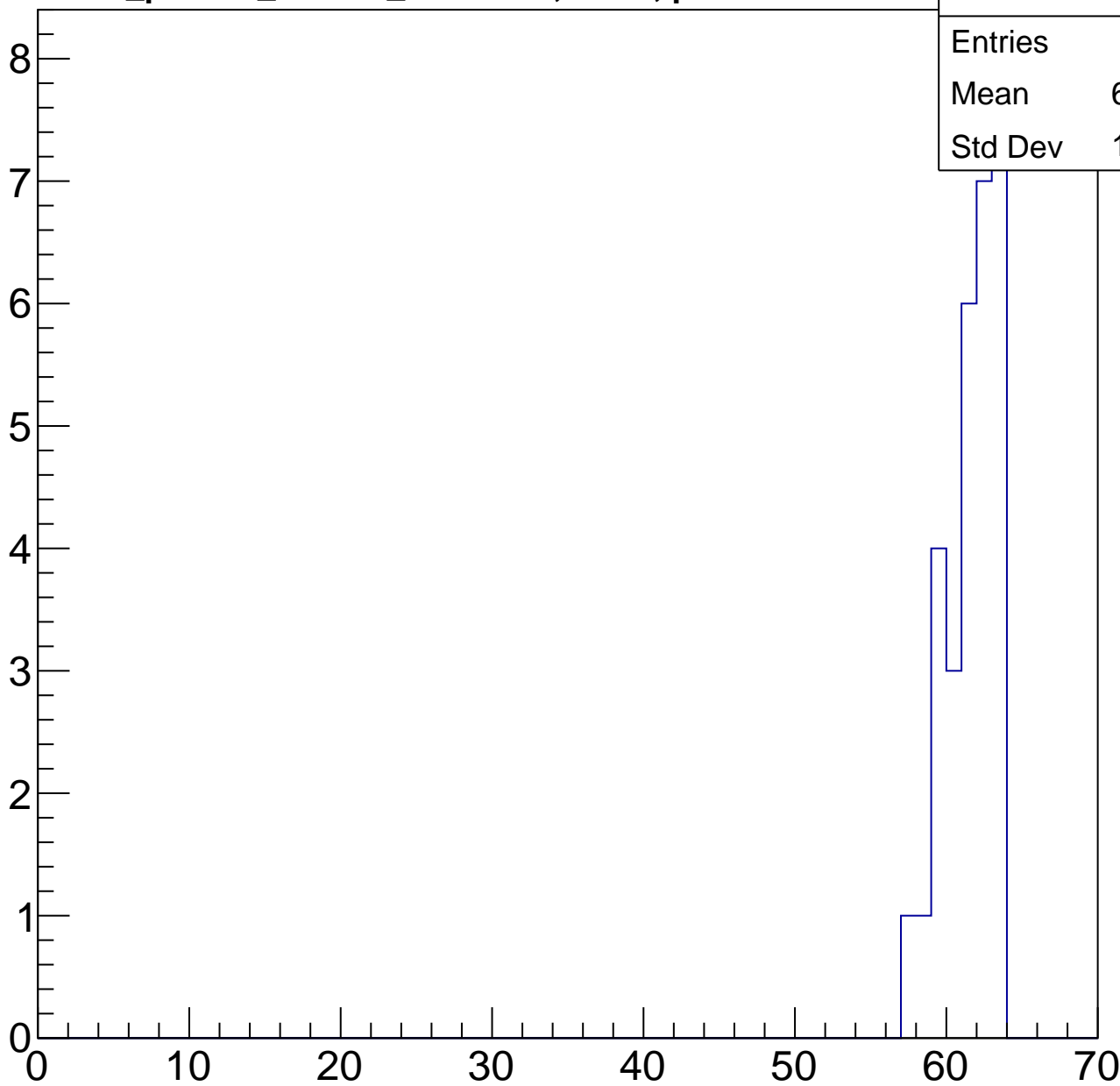
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	30
Mean	61.17
Std Dev	1.655

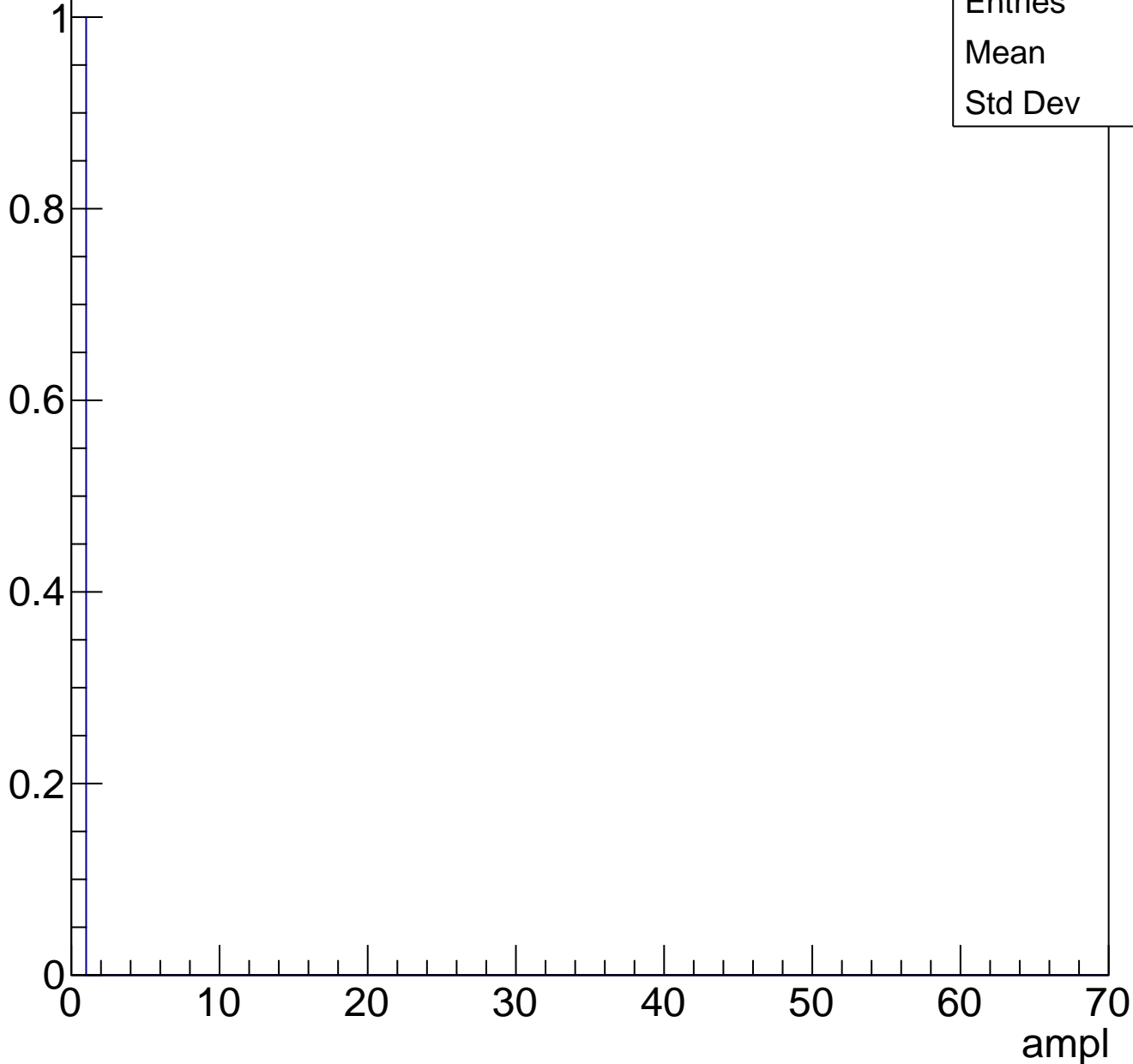
ampl



# B1L101S, U9-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	6.333
Std Dev	8.957

# B1L101S, U9-ch68, adc0

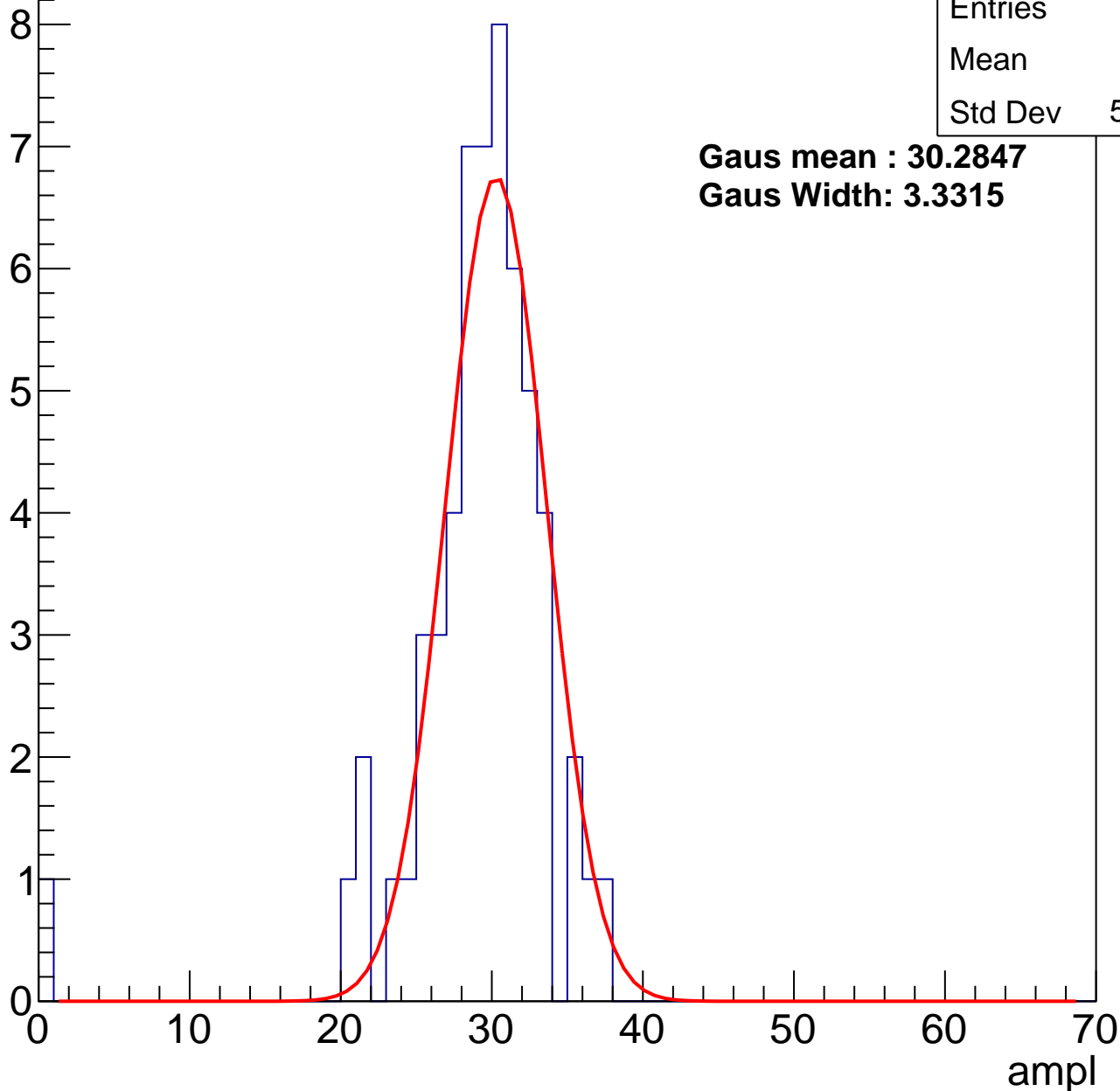
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	28.6
Std Dev	5.174

**Gaus mean : 30.2847**

**Gaus Width: 3.3315**



# B1L101S, U9-ch68, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	88
Mean	36.1
Std Dev	4.208

**Gaus mean : 36.7589**

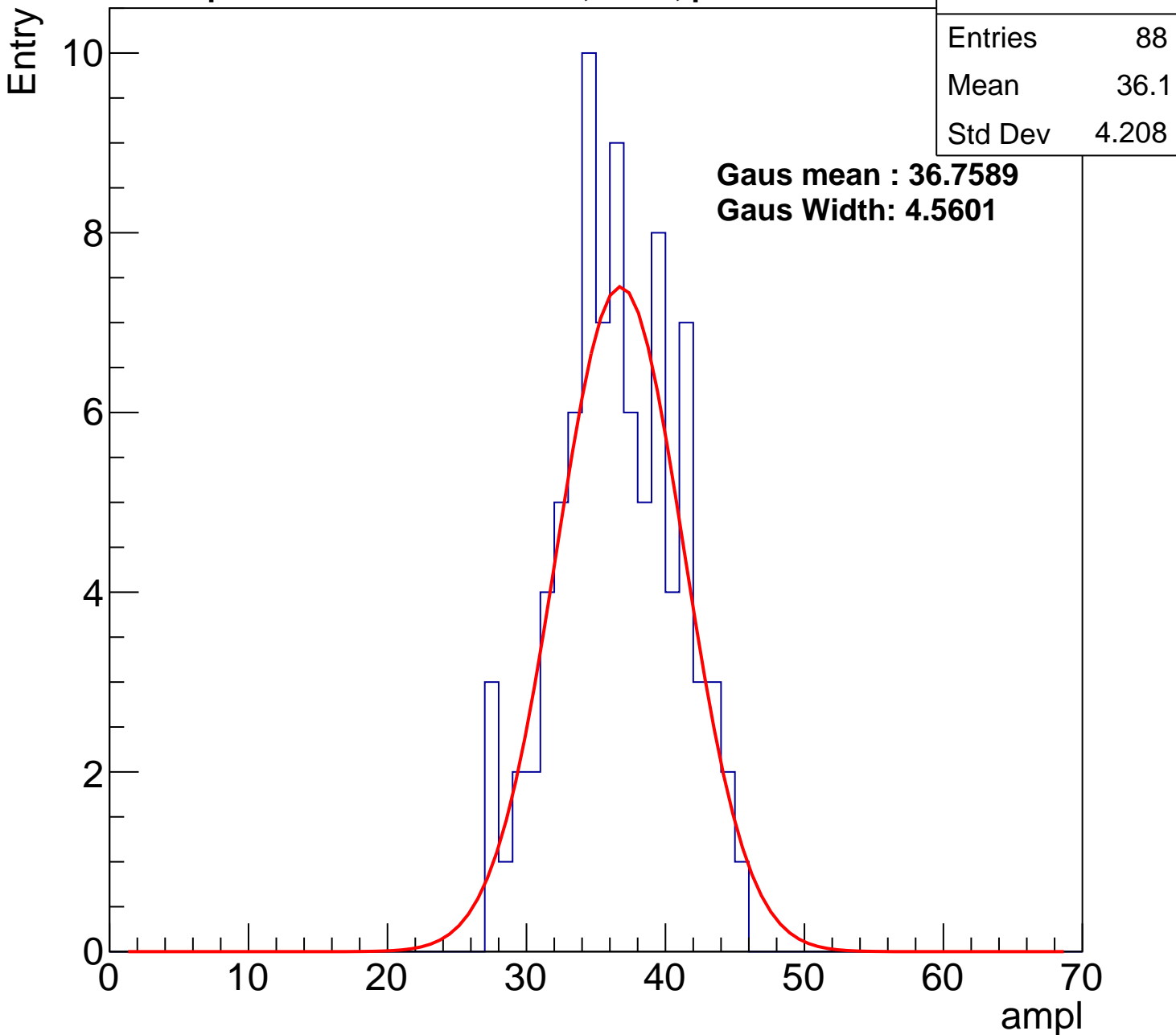
**Gaus Width: 4.5601**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U9-ch68, adc2

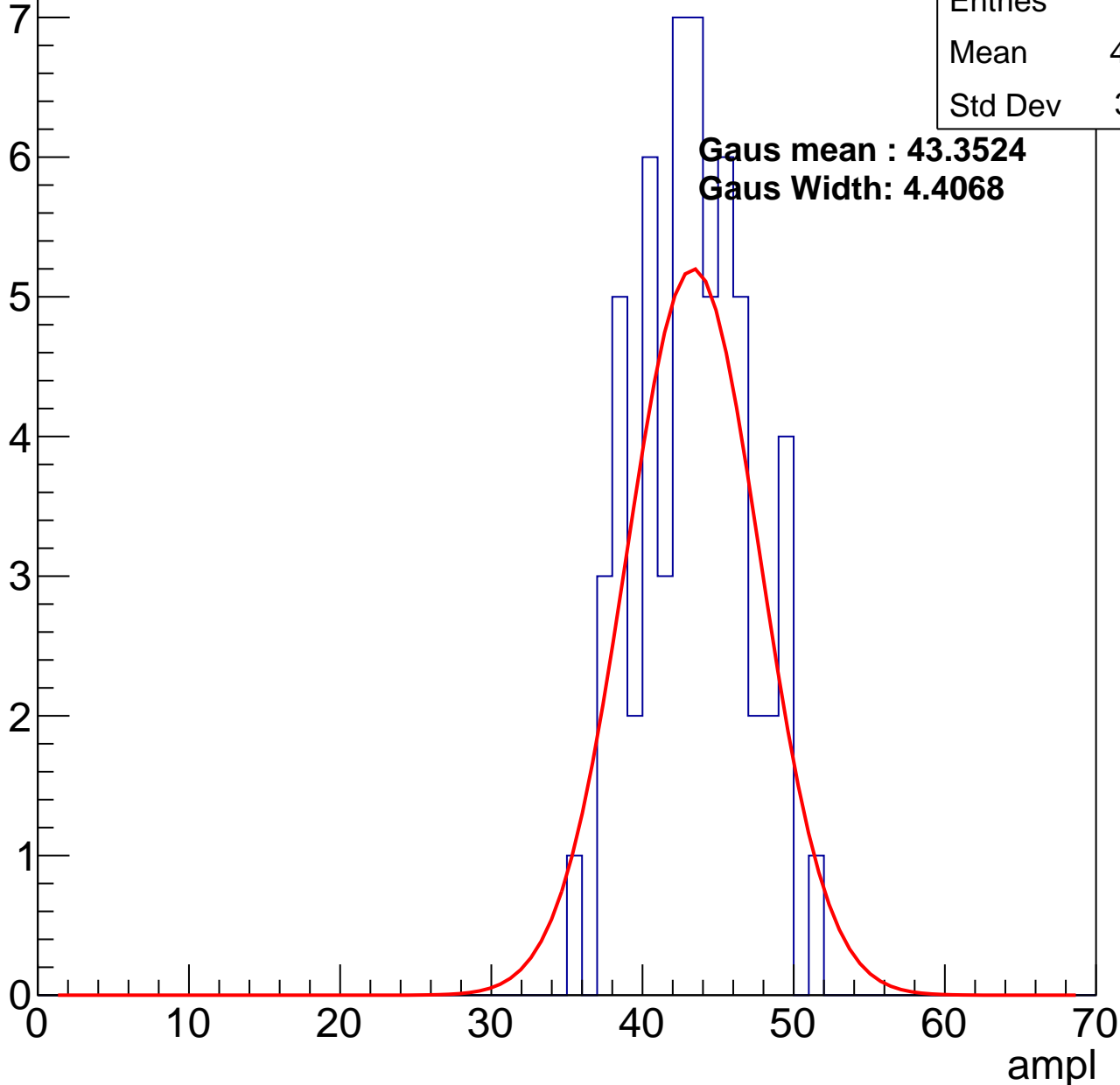
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	42.86
Std Dev	3.601

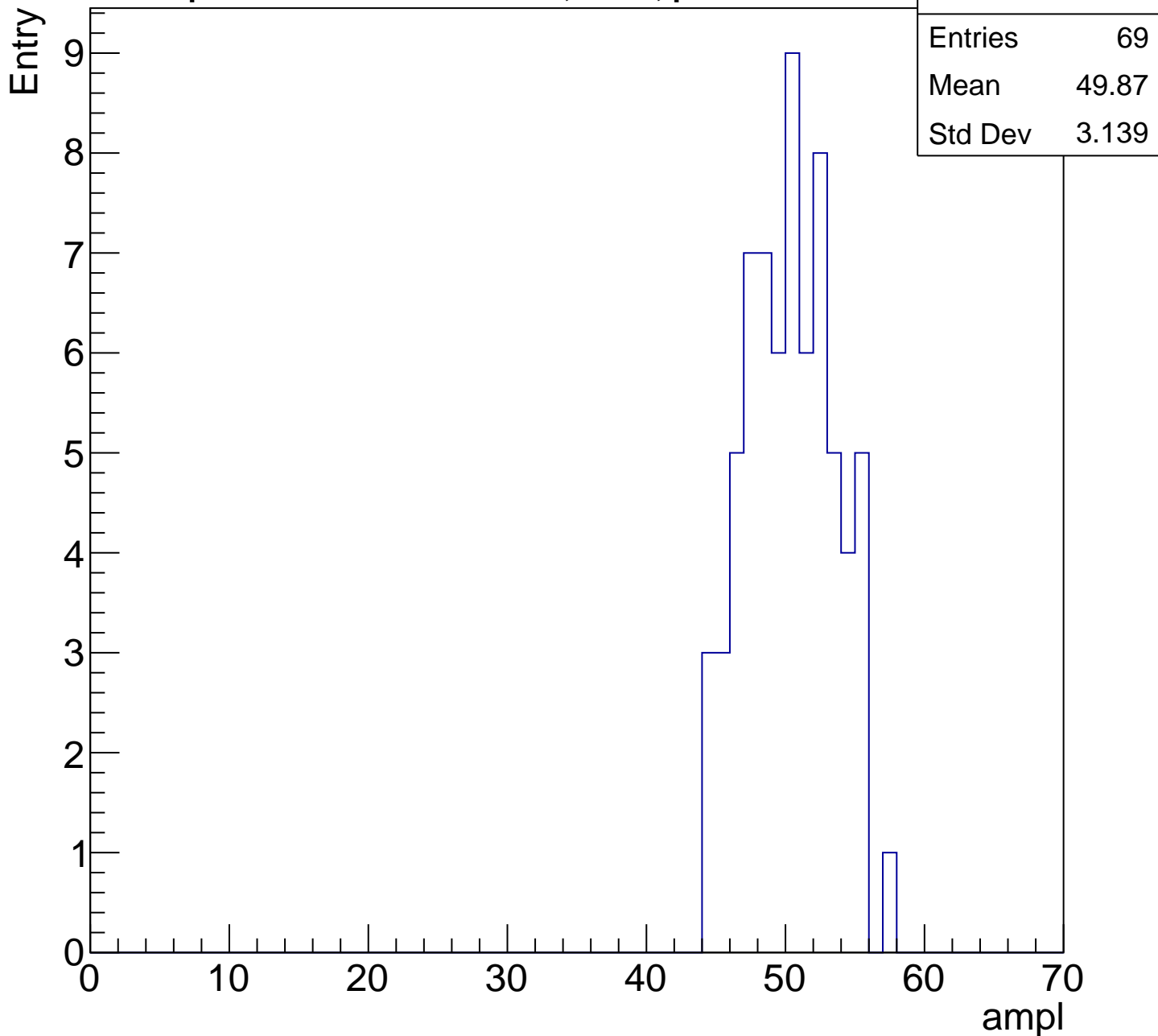
**Gaus mean : 43.3524**

**Gaus Width: 4.4068**



# B1L101S, U9-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

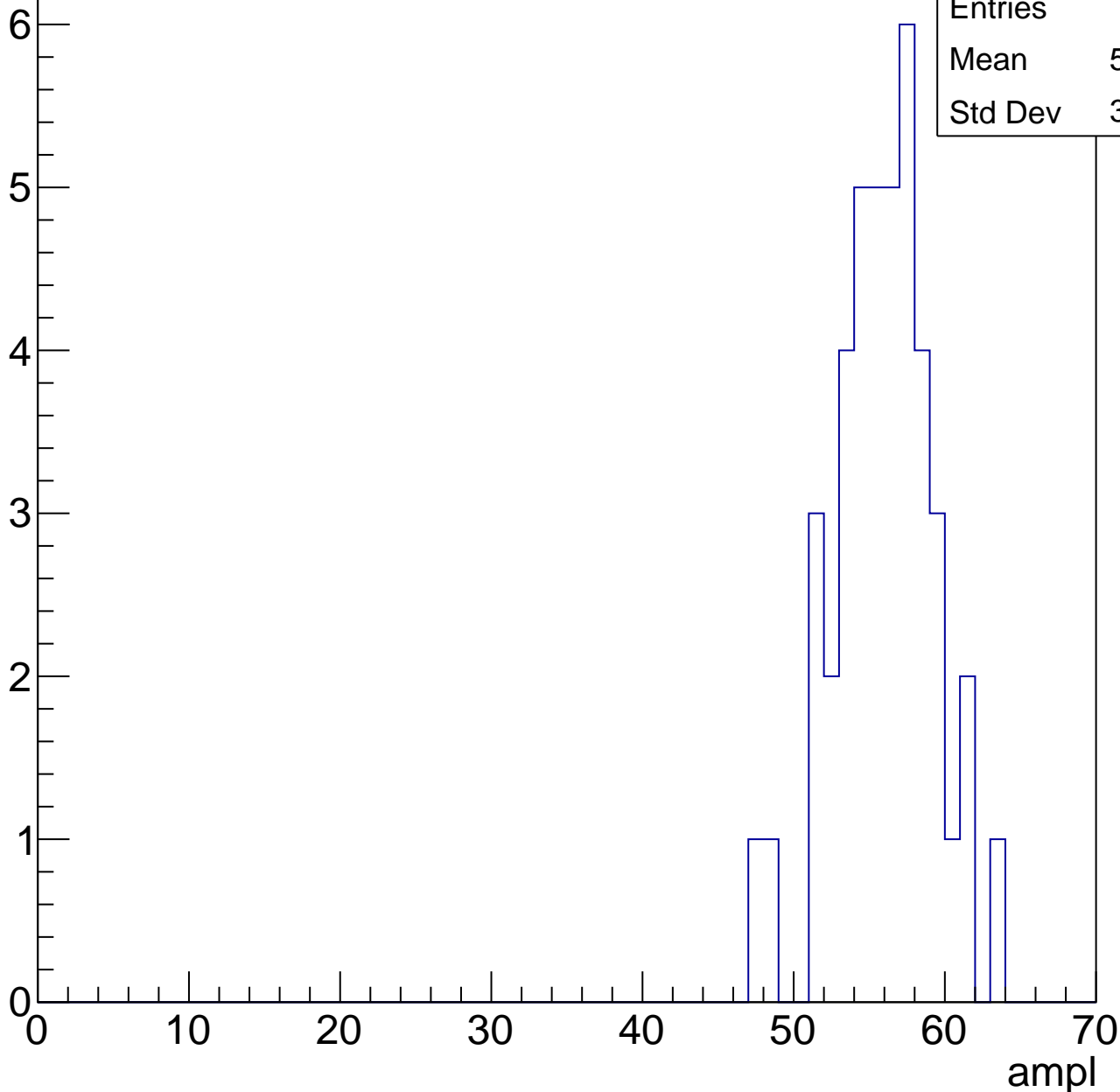


# B1L101S, U9-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

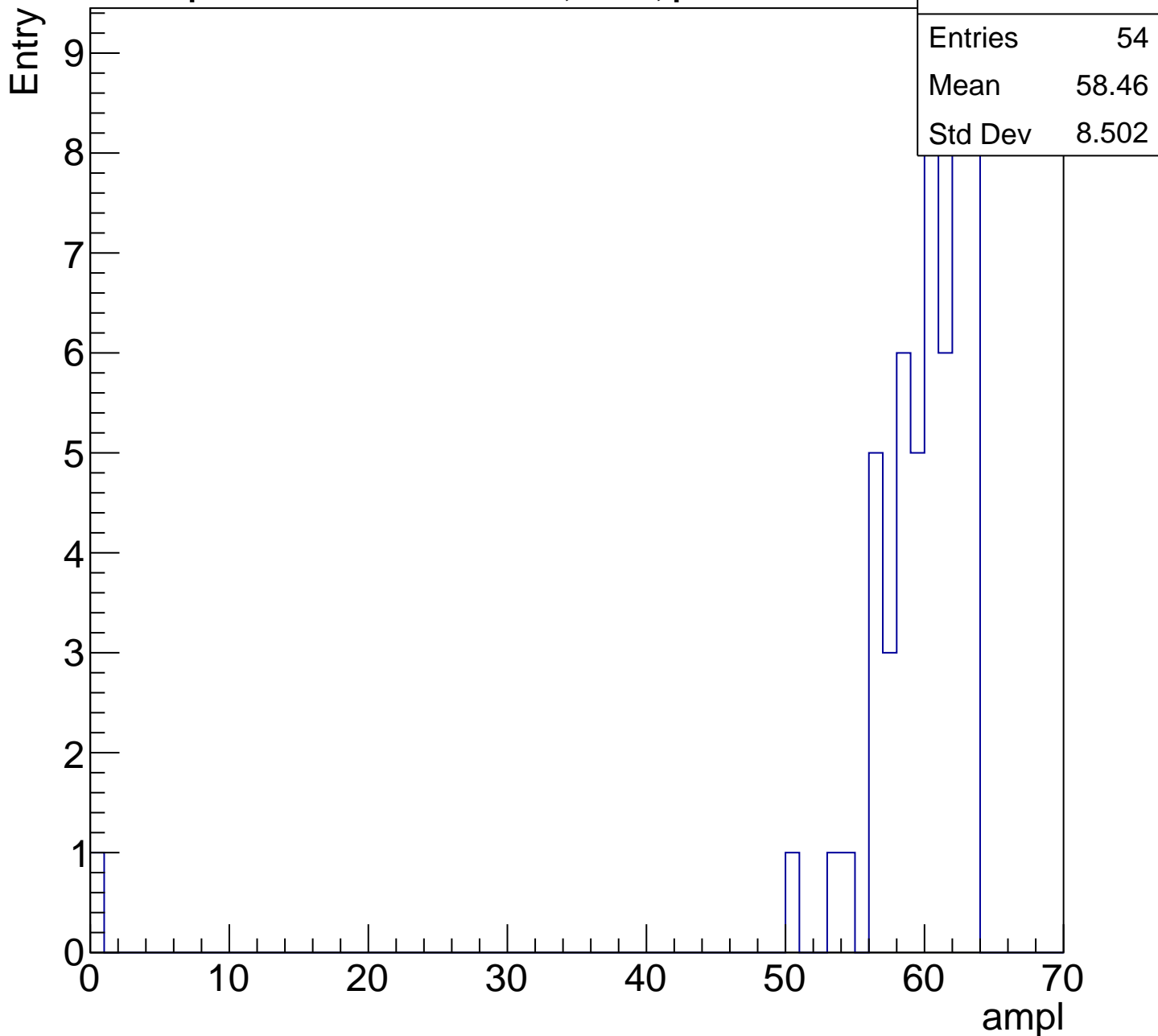
Entry

Entries	43
Mean	55.47
Std Dev	3.287



# B1L101S, U9-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

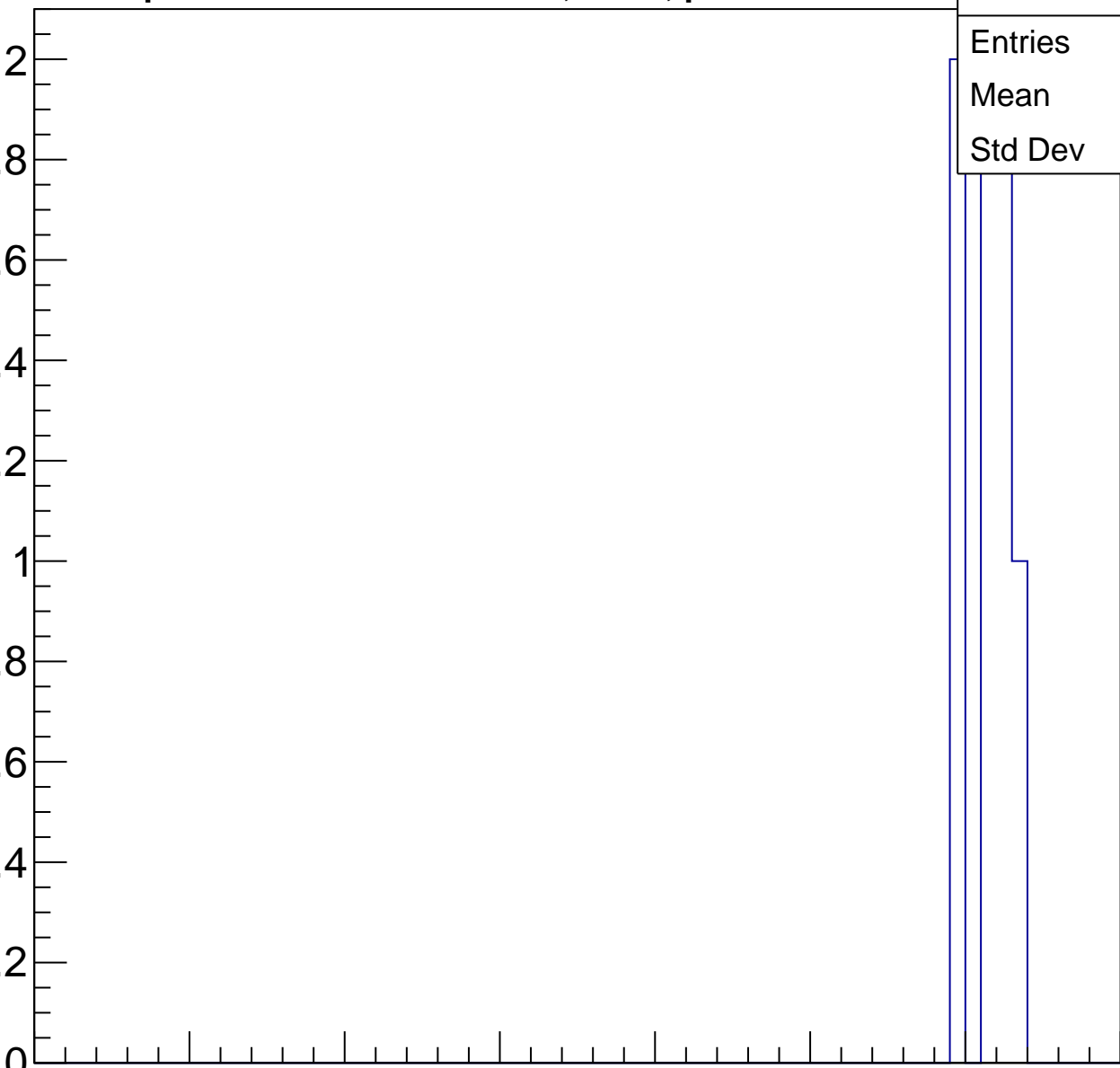
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	61
Std Dev	1.414

0 10 20 30 40 50 60 70

ampl





# B1L101S, U9-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U9-ch69, adc0

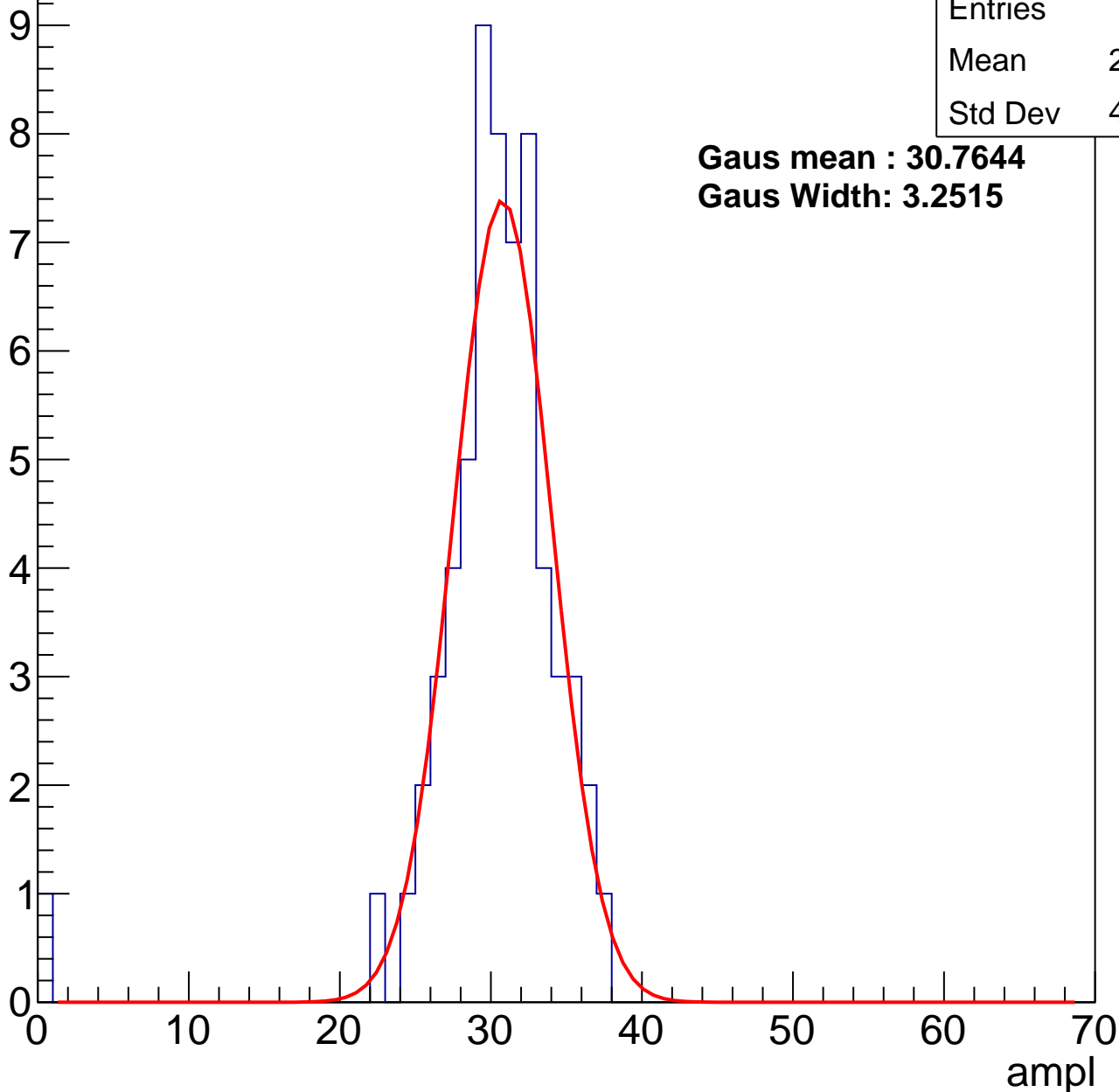
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	29.74
Std Dev	4.882

**Gaus mean : 30.7644**

**Gaus Width: 3.2515**



# B1L101S, U9-ch69, adc1

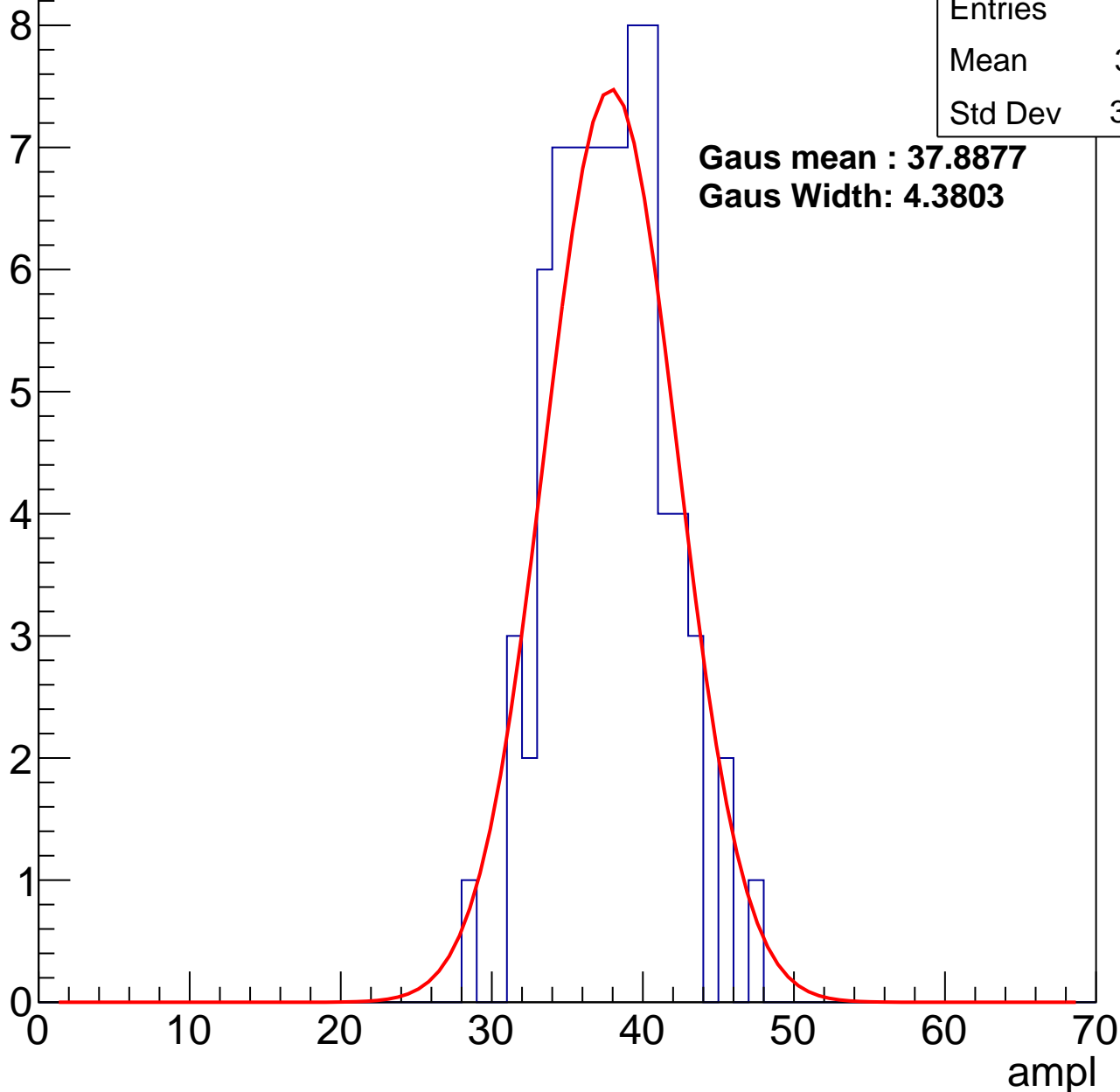
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	37.31
Std Dev	3.669

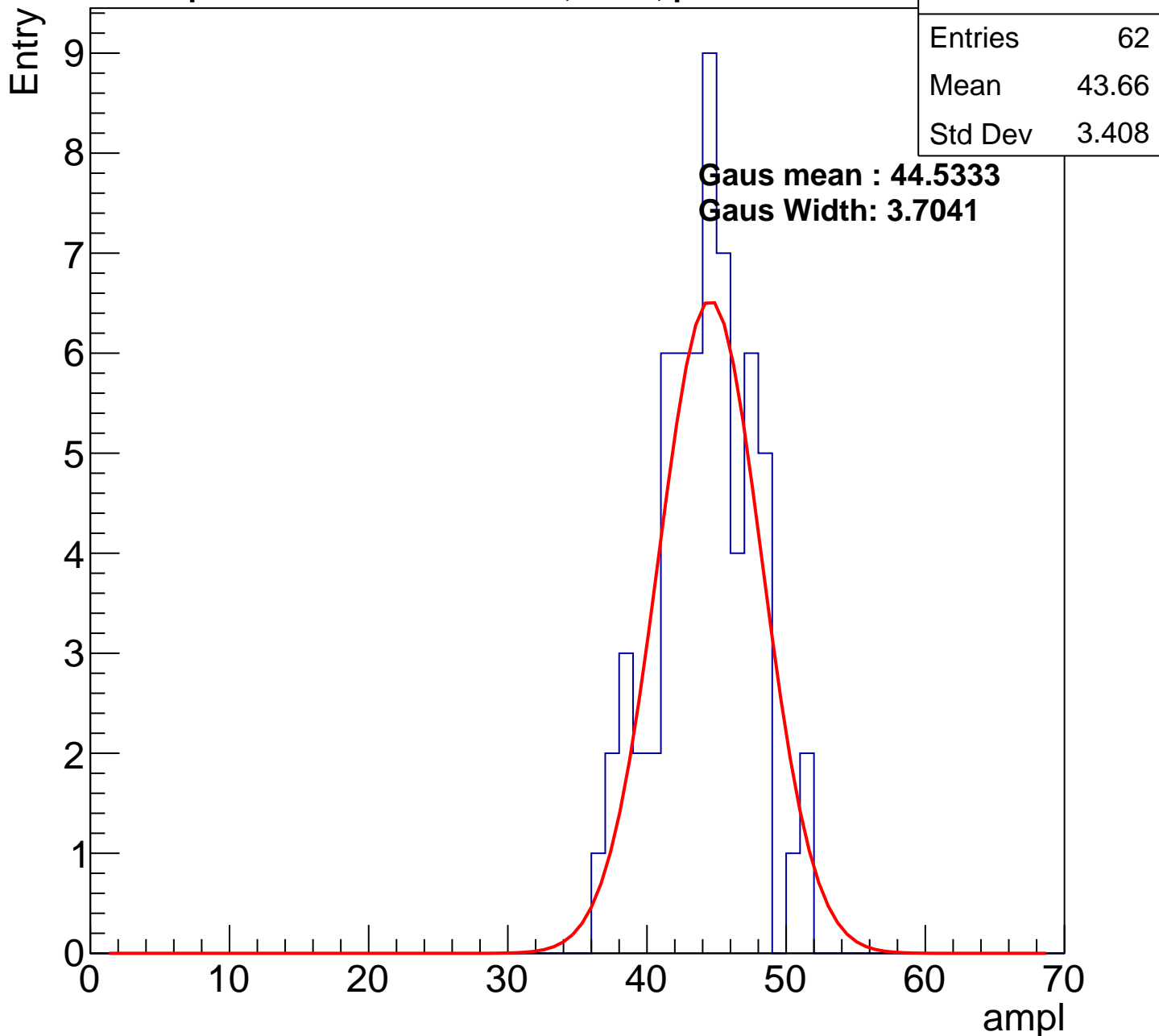
**Gaus mean : 37.8877**

**Gaus Width: 4.3803**



# B1L101S, U9-ch69, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

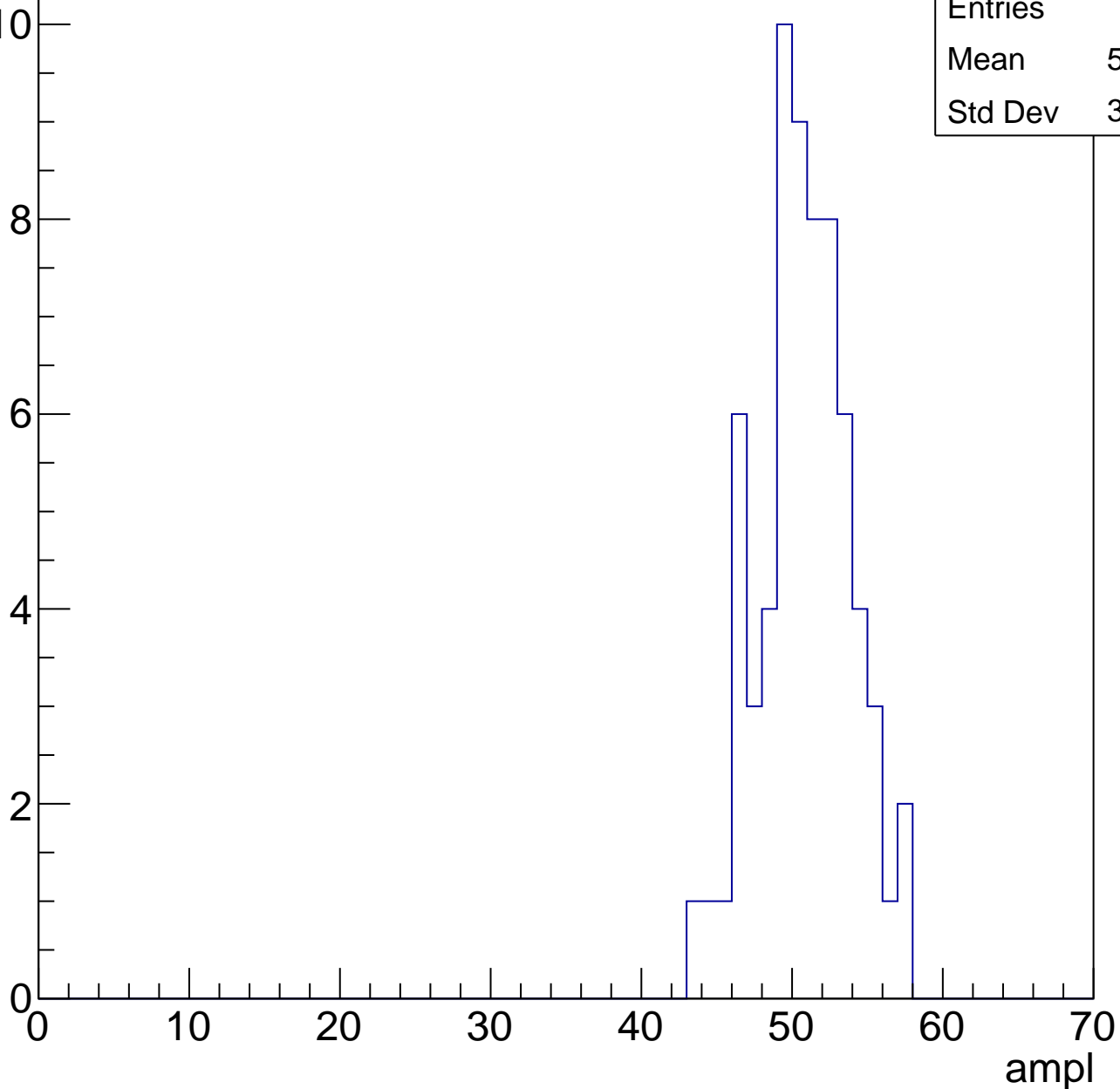


# B1L101S, U9-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

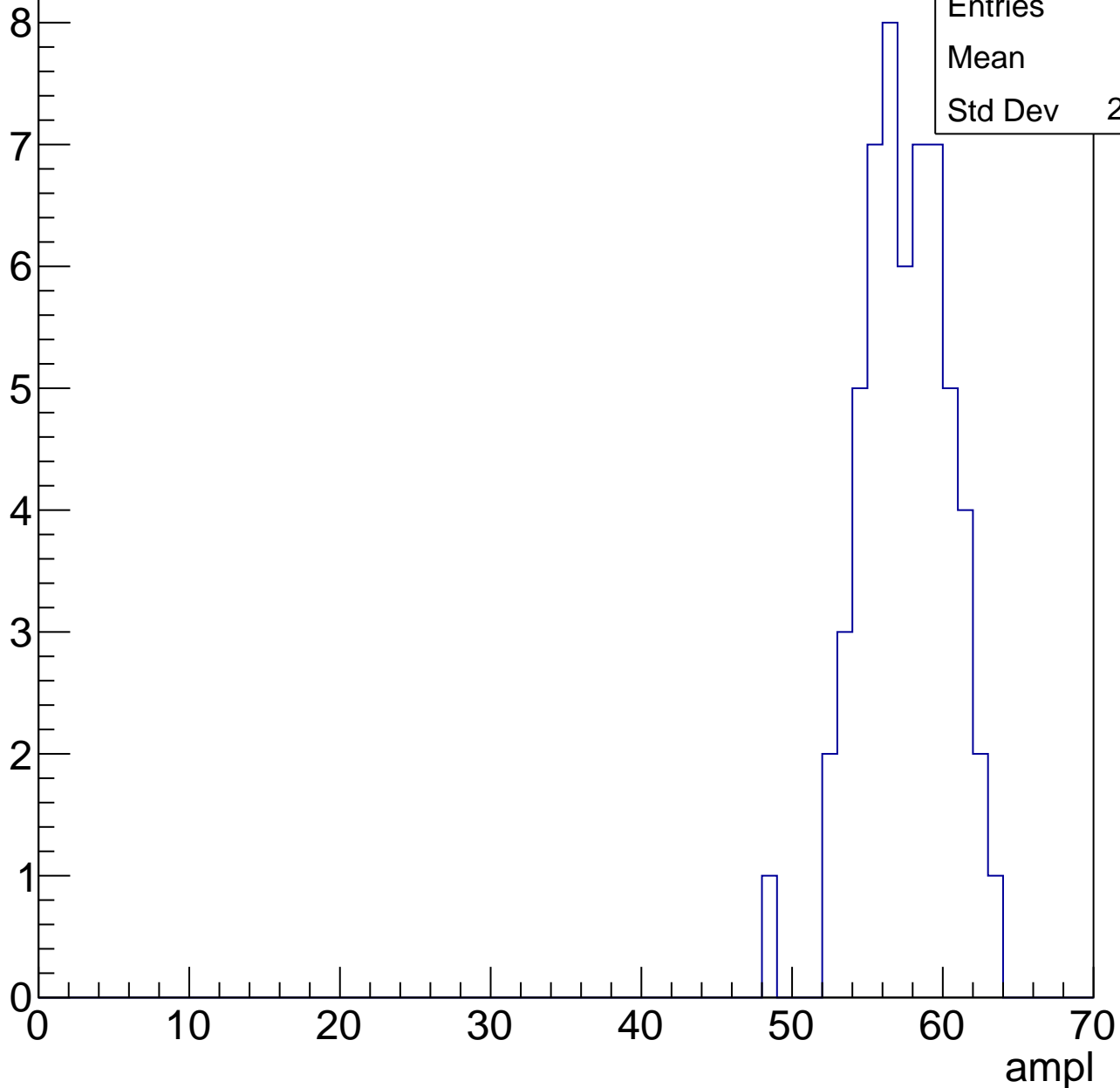
Entries	67
Mean	50.36
Std Dev	3.036



# B1L101S, U9-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

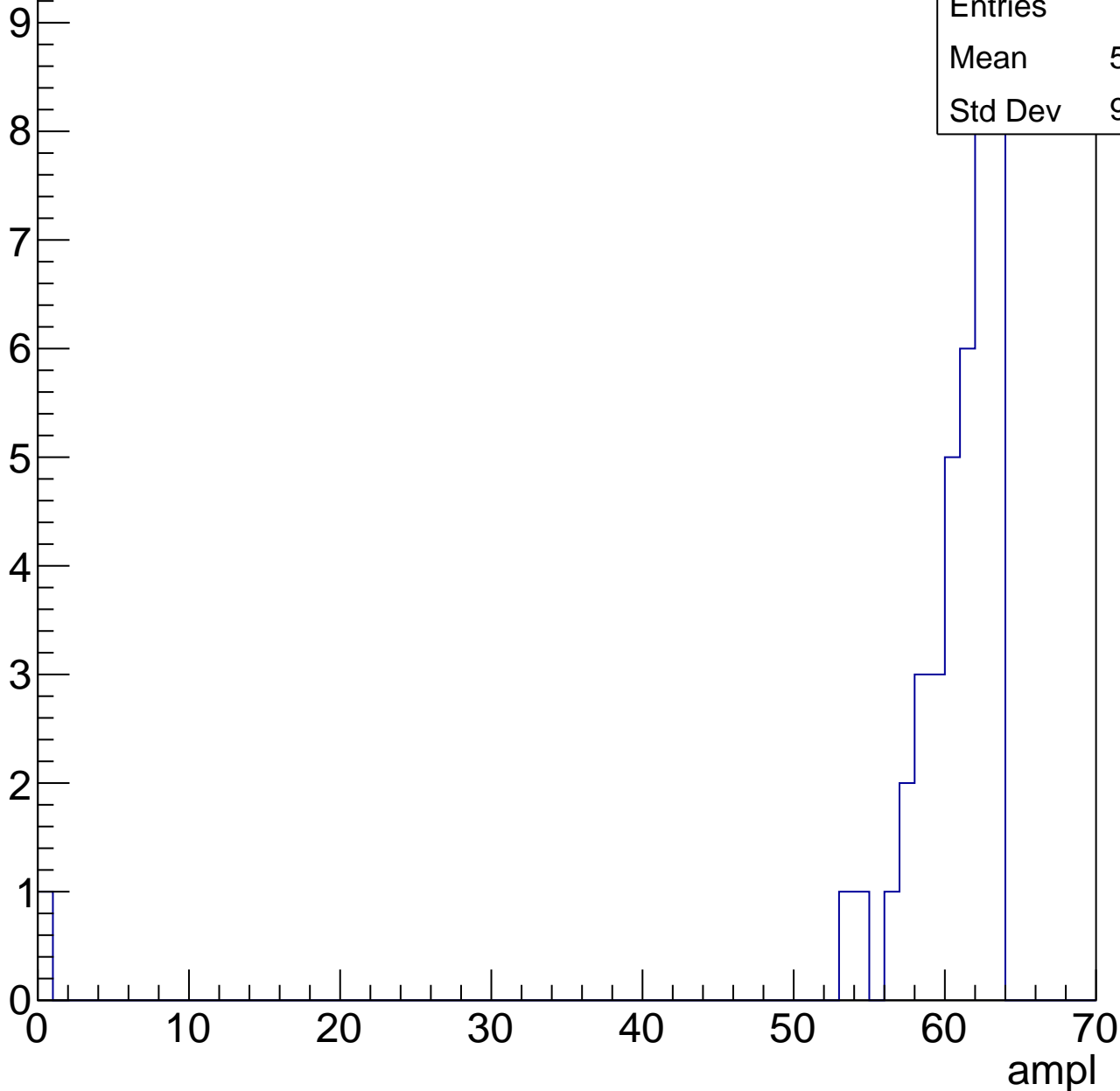


# B1L101S, U9-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	40
Mean	58.92
Std Dev	9.755



# B1L101S, U9-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L101S, U9-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch70, adc0

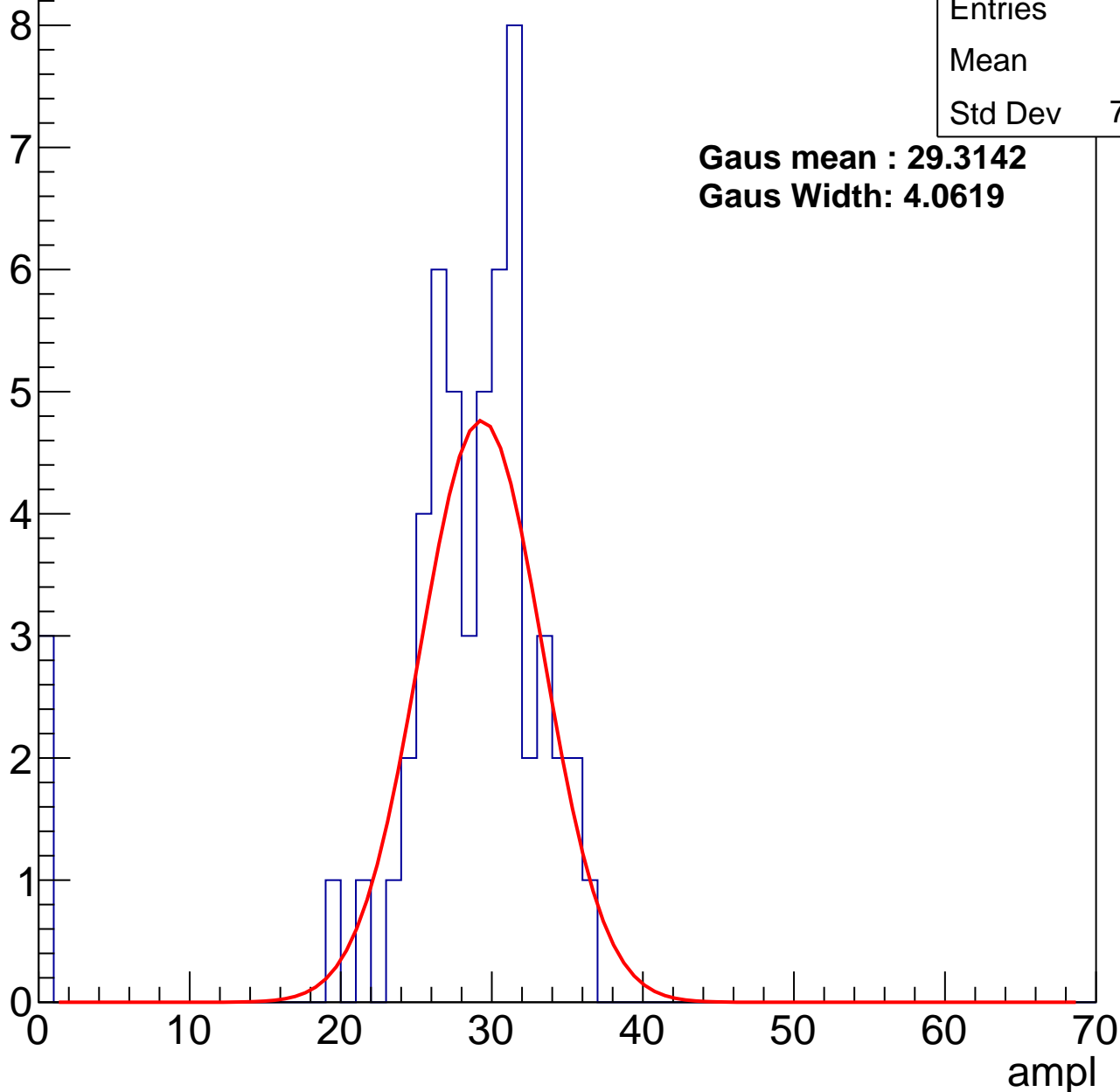
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	27.2
Std Dev	7.399

**Gaus mean : 29.3142**

**Gaus Width: 4.0619**



# B1L101S, U9-ch70, adc1

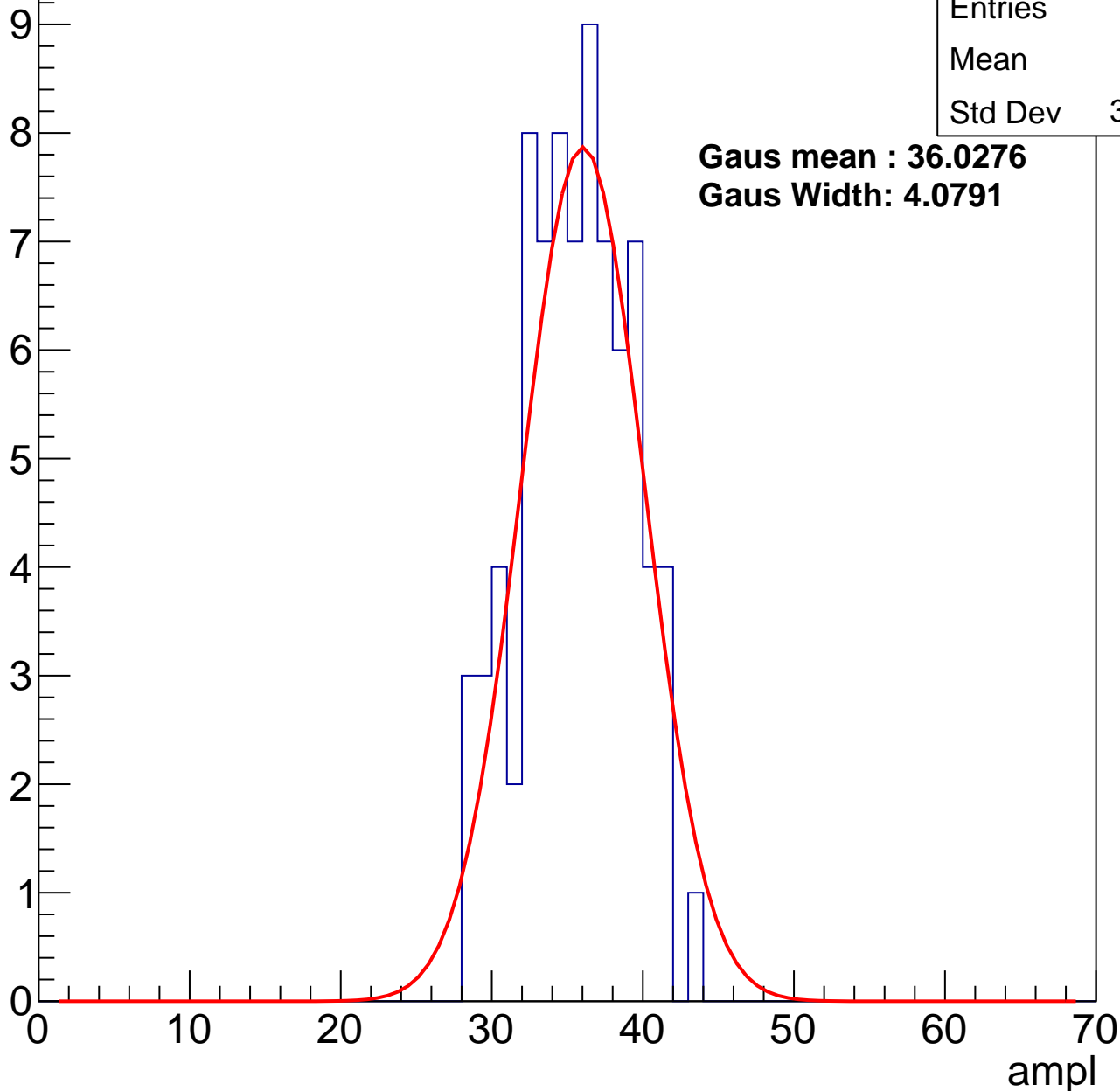
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	35.1
Std Dev	3.545

**Gaus mean : 36.0276**

**Gaus Width: 4.0791**



# B1L101S, U9-ch70, adc2

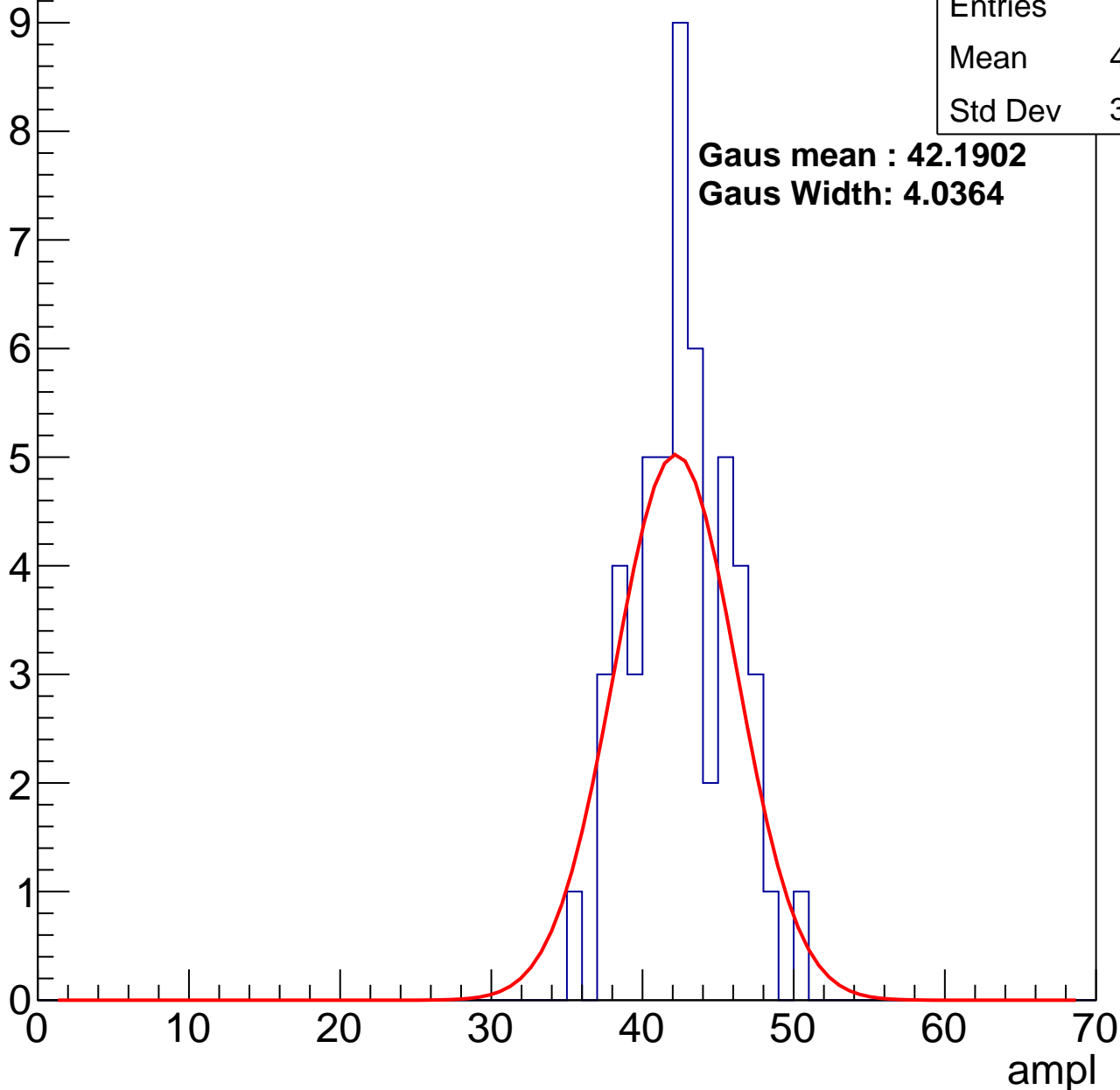
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	42.15
Std Dev	3.213

**Gaus mean : 42.1902**

**Gaus Width: 4.0364**

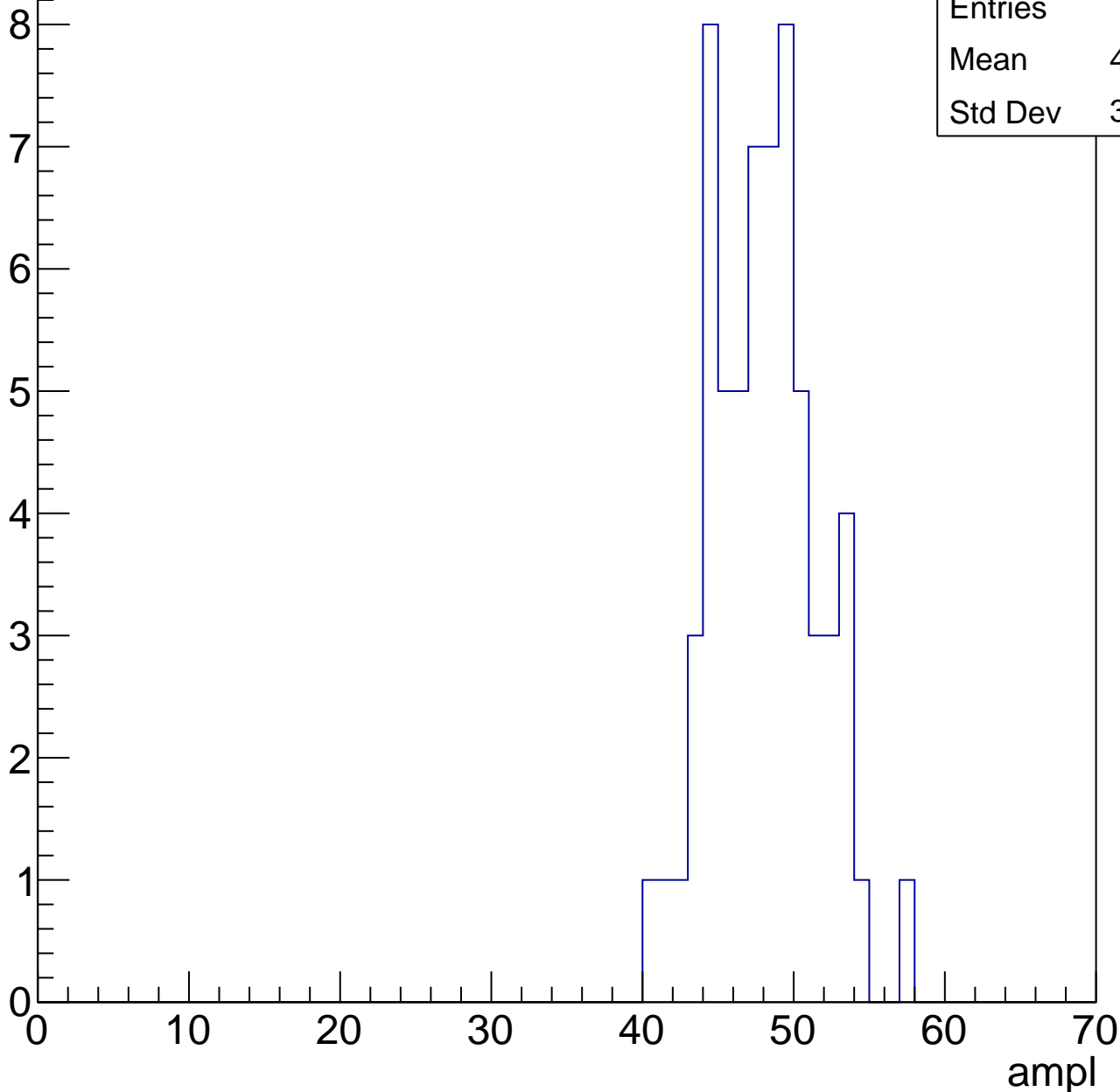


# B1L101S, U9-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

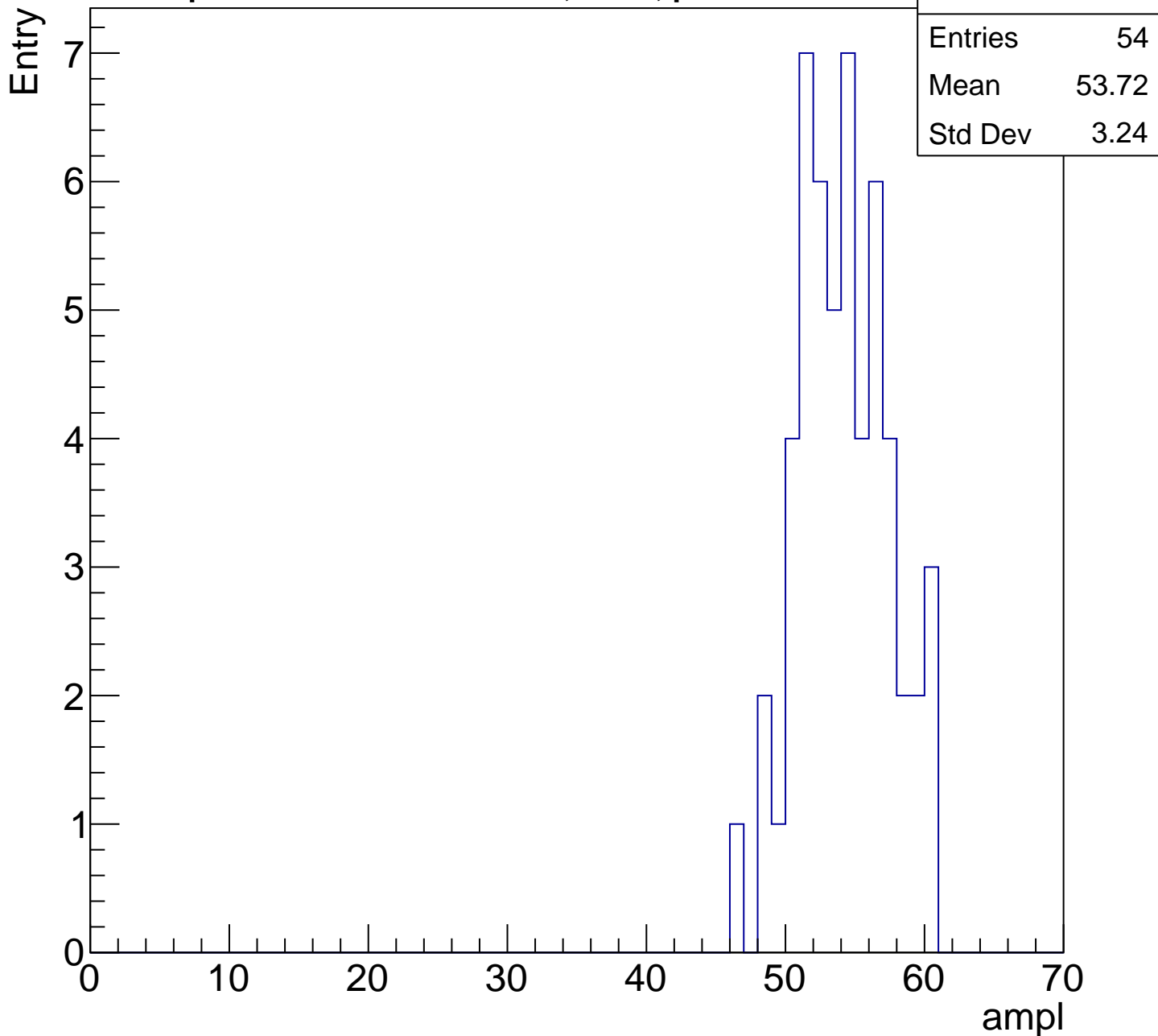
Entry

Entries	63
Mean	47.59
Std Dev	3.412



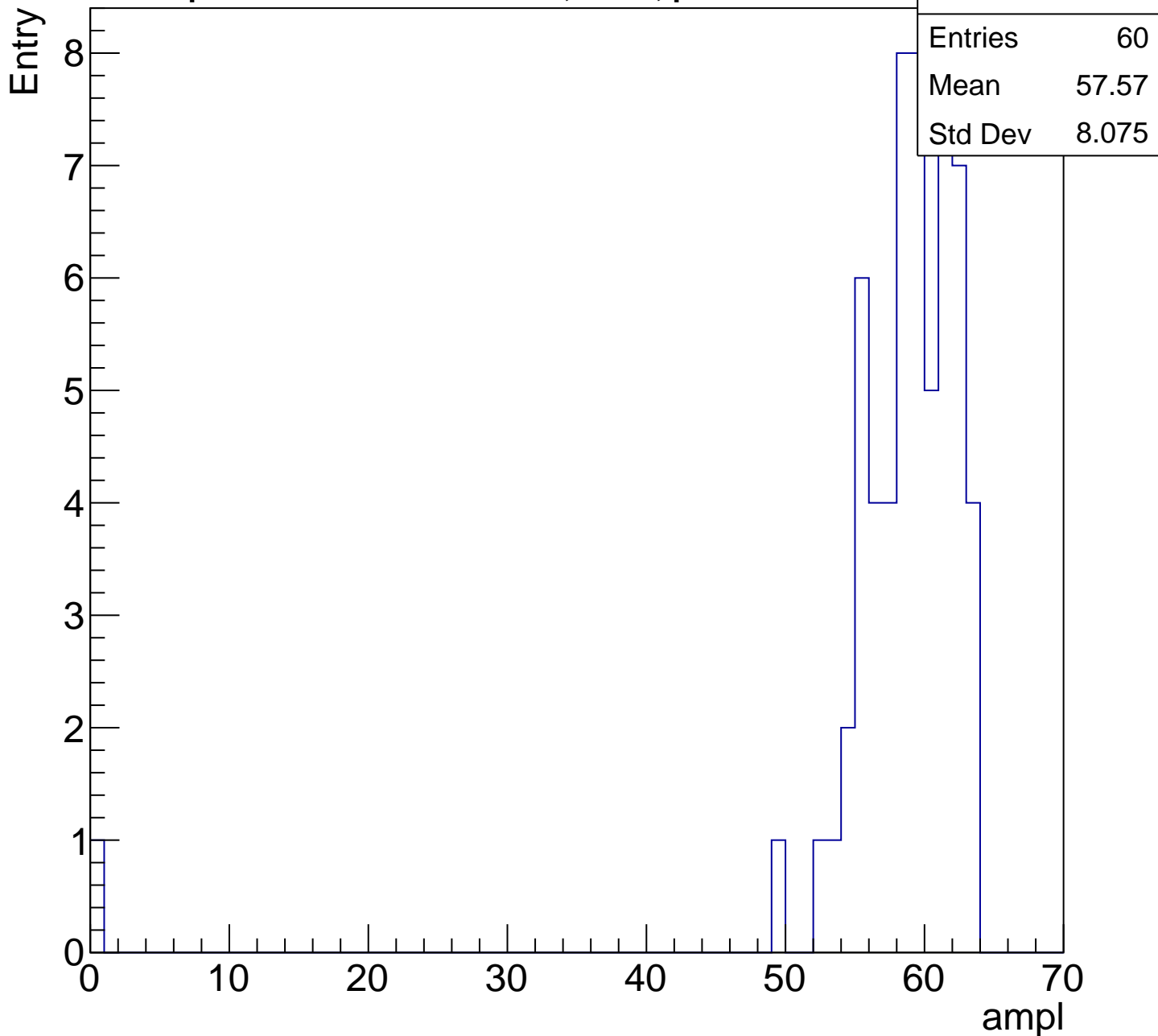
# B1L101S, U9-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

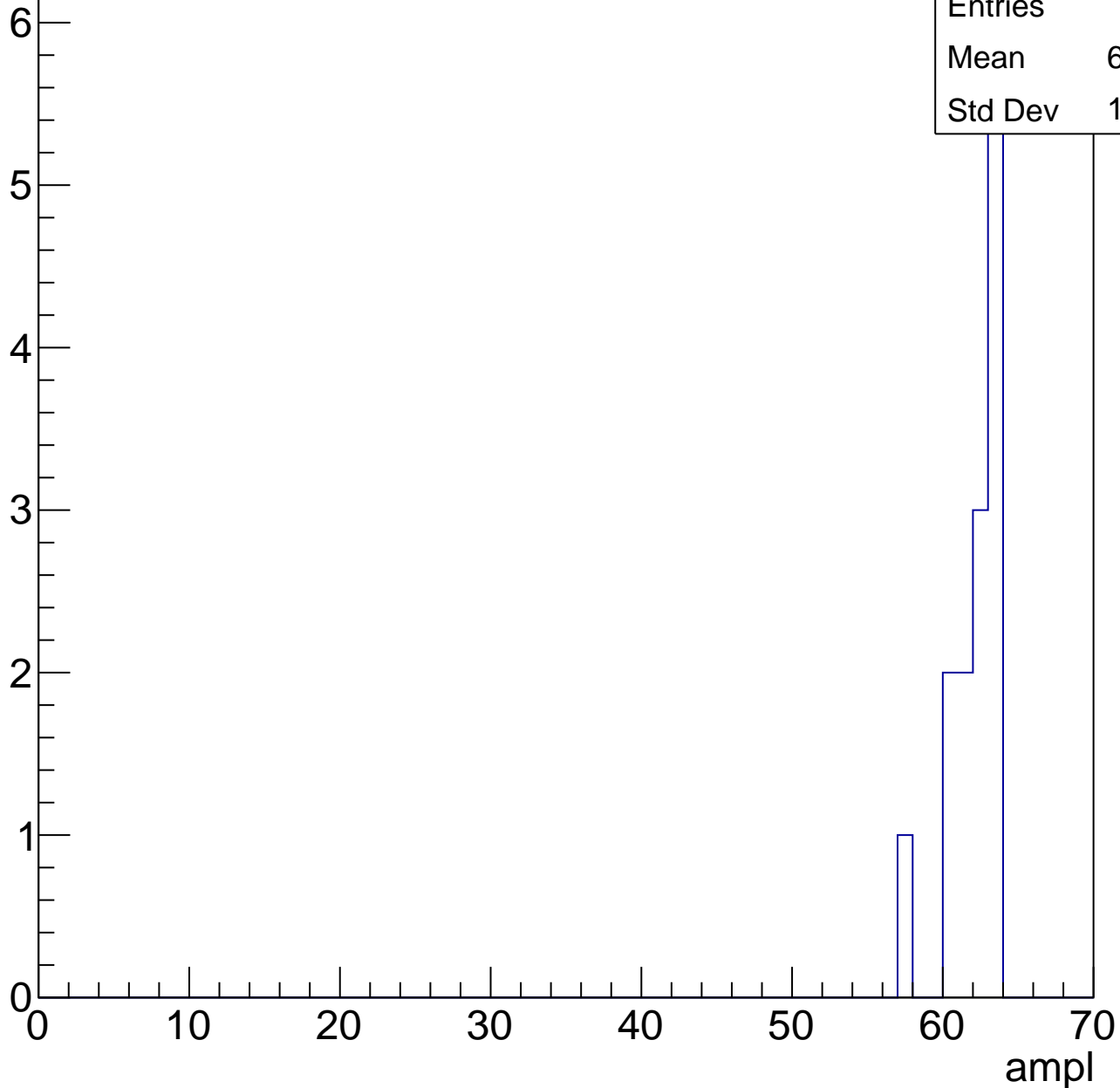


# B1L101S, U9-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	14
Mean	61.64
Std Dev	1.674





# B1L101S, U9-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U9-ch71, adc0

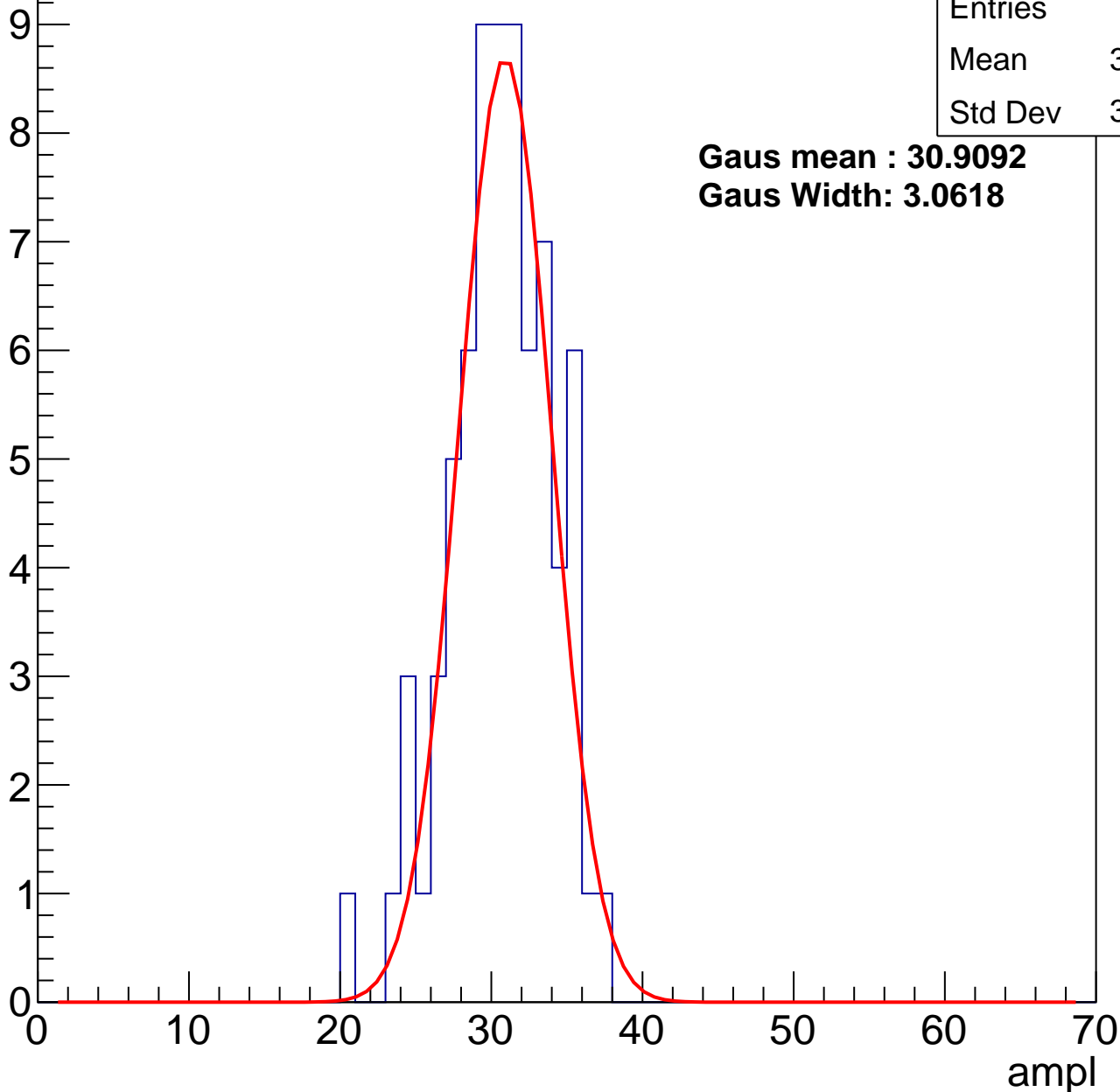
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	30.18
Std Dev	3.335

**Gaus mean : 30.9092**

**Gaus Width: 3.0618**



# B1L101S, U9-ch71, adc1

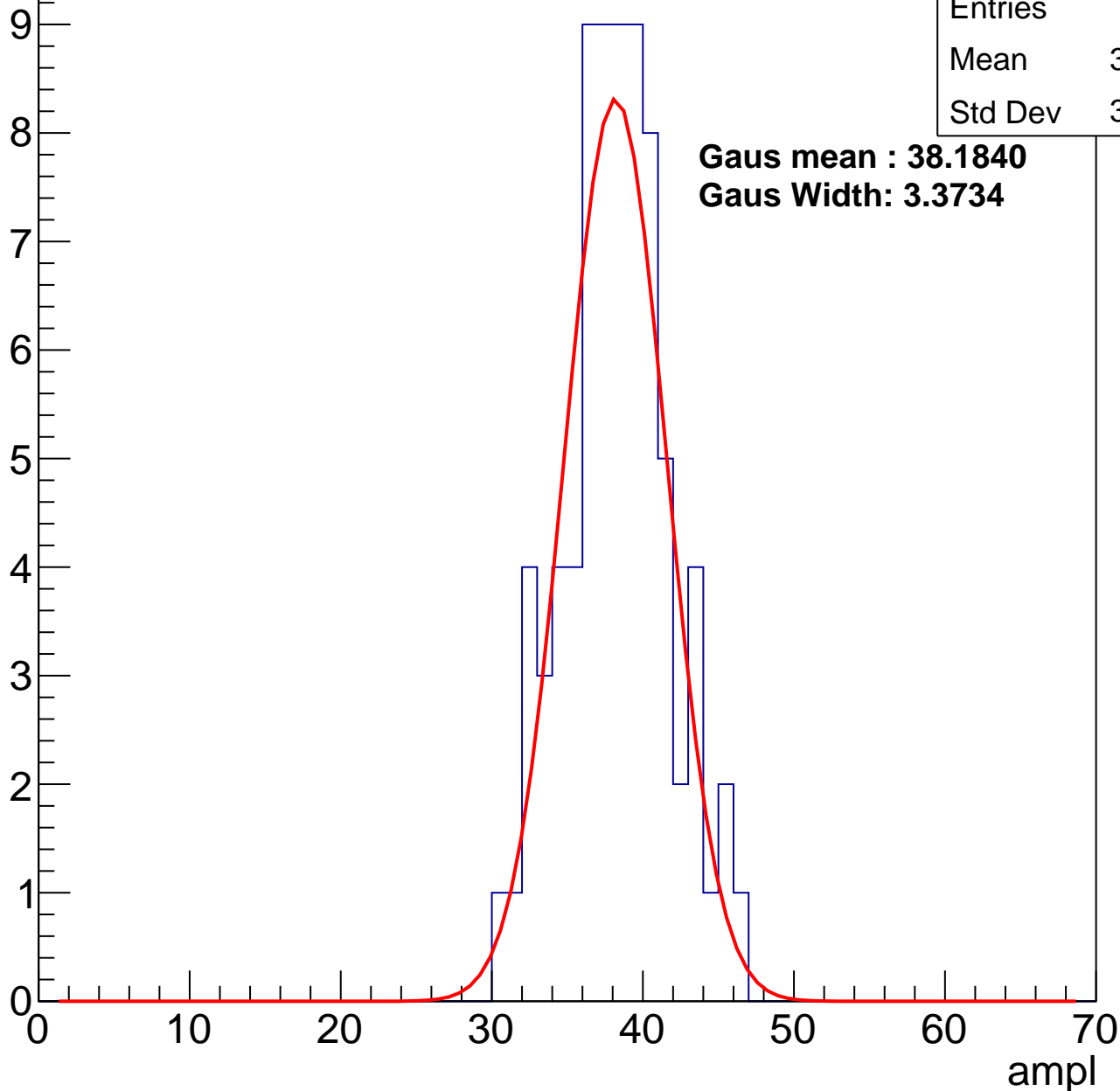
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	37.83
Std Dev	3.424

**Gaus mean : 38.1840**

**Gaus Width: 3.3734**



# B1L101S, U9-ch71, adc2

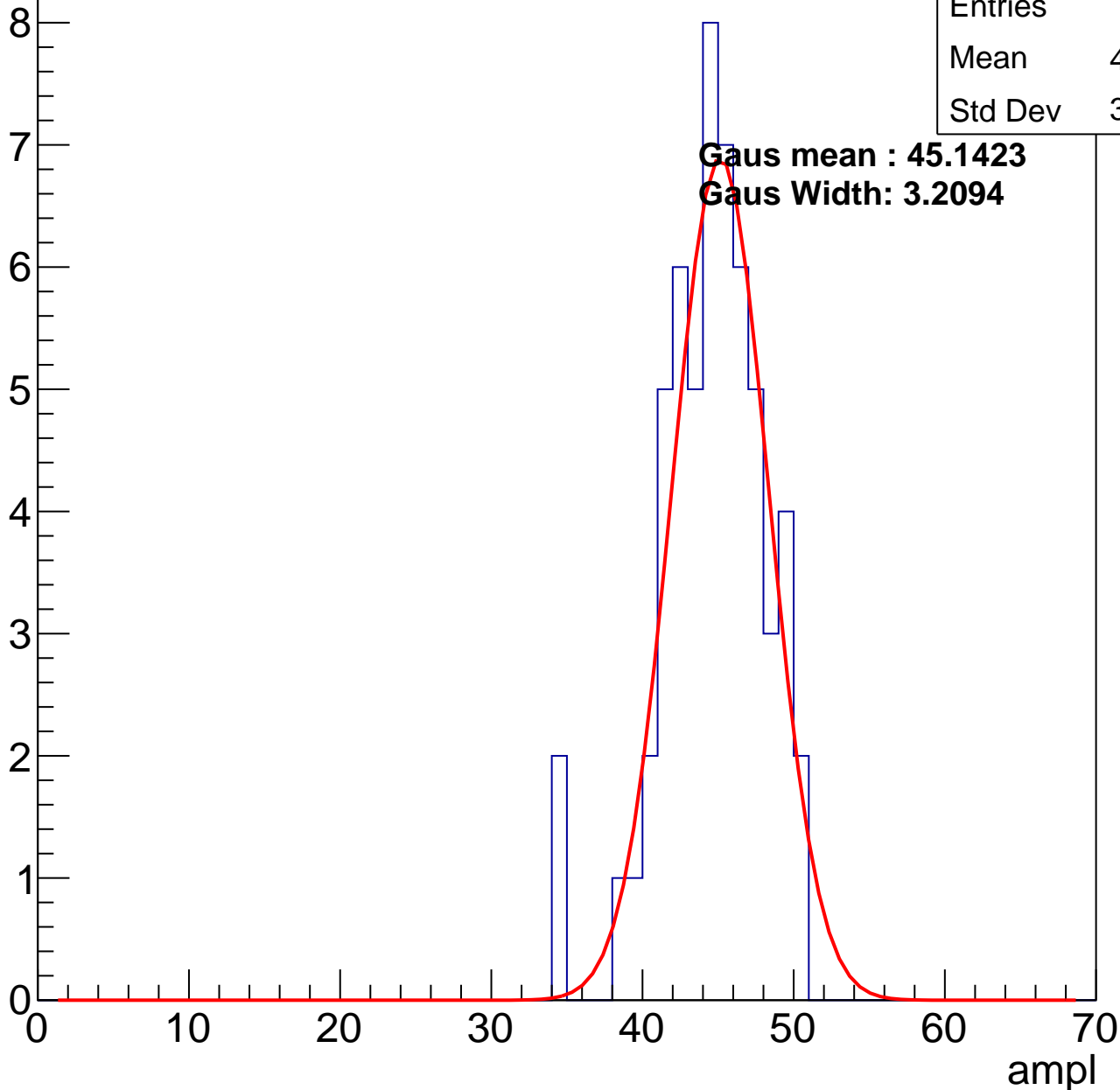
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	44.12
Std Dev	3.408

**Gaus mean : 45.1423**

**Gaus Width: 3.2094**

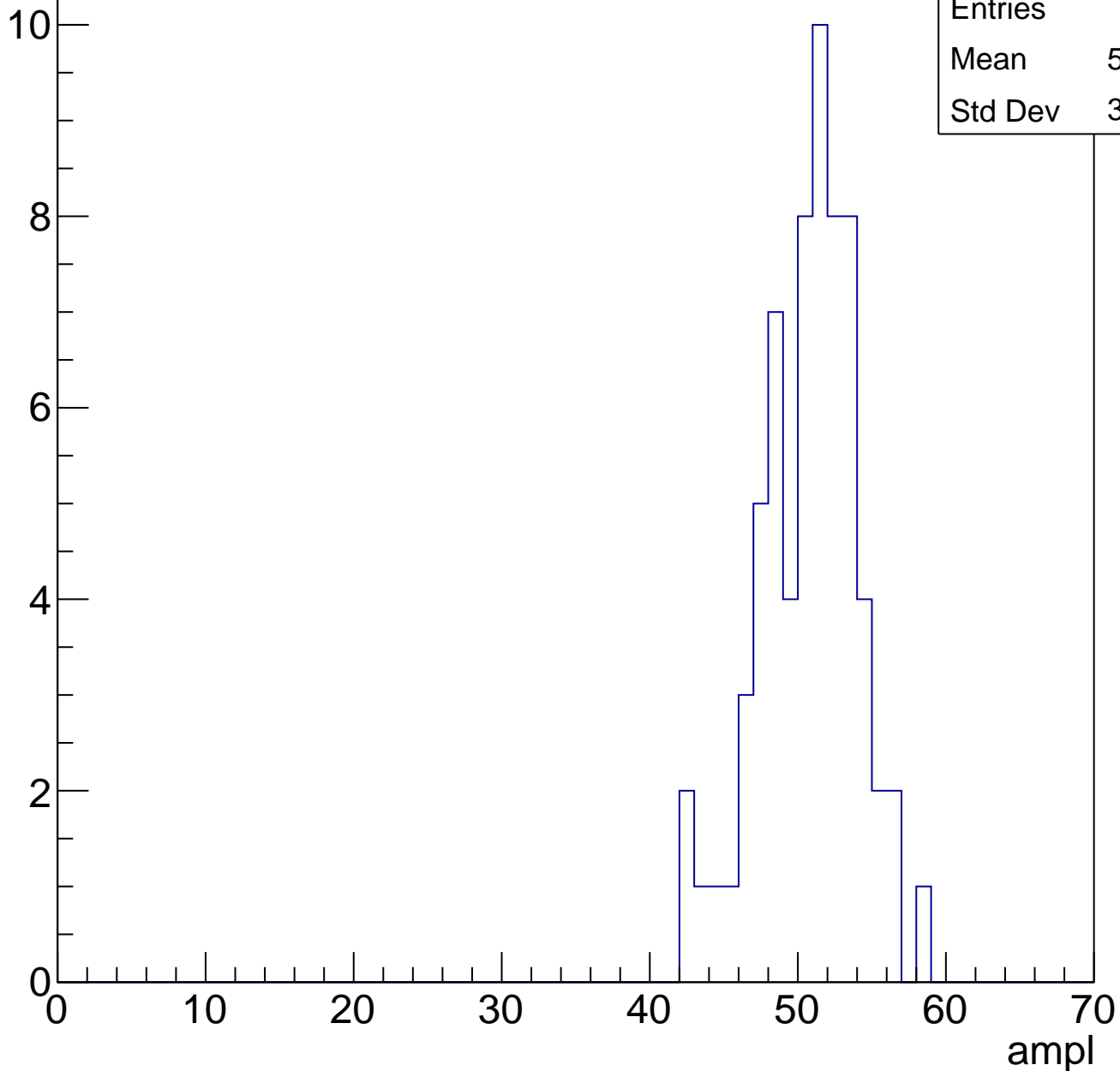


# B1L101S, U9-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

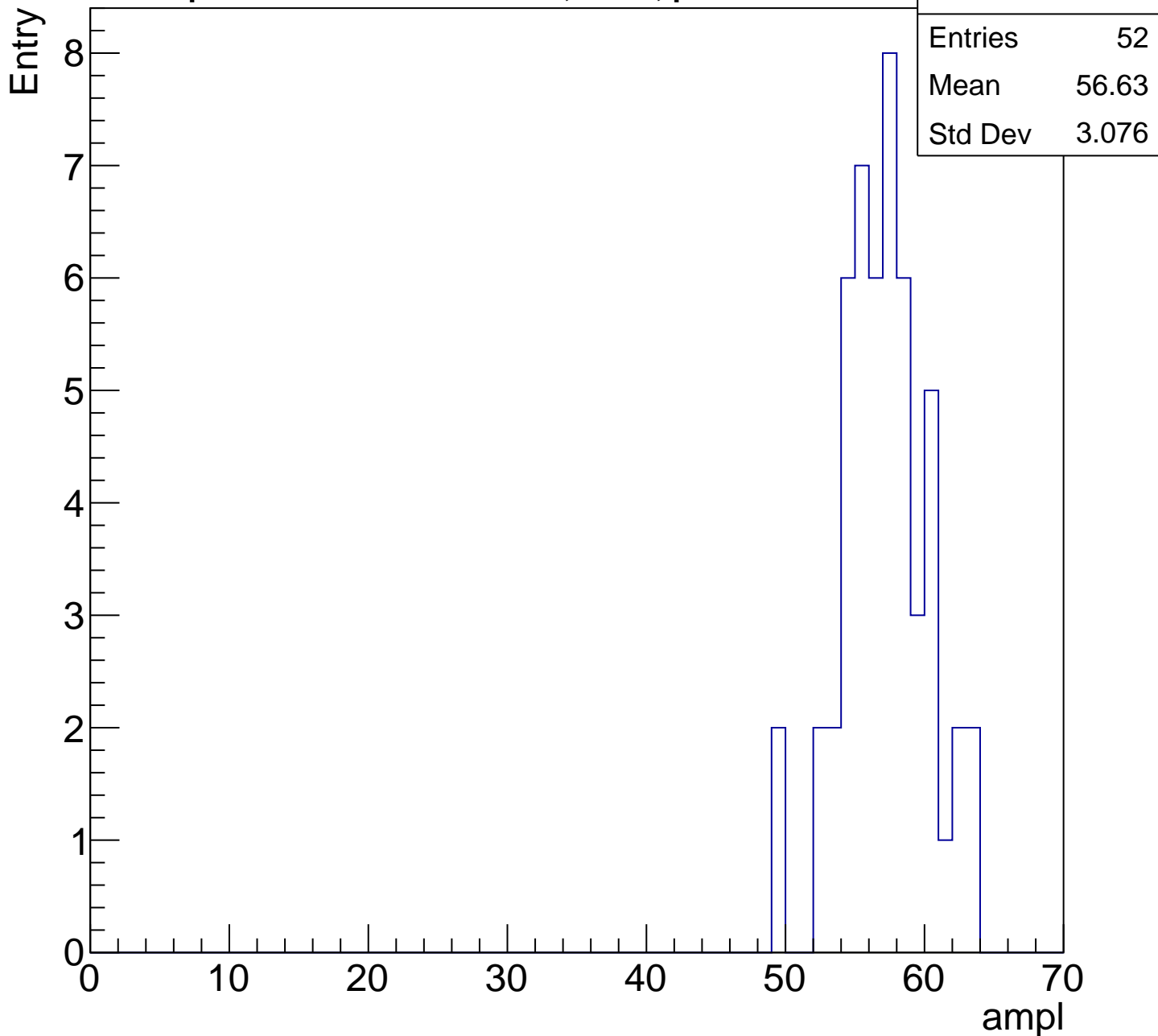
Entries	67
Mean	50.25
Std Dev	3.284

Entry



# B1L101S, U9-ch71, adc4

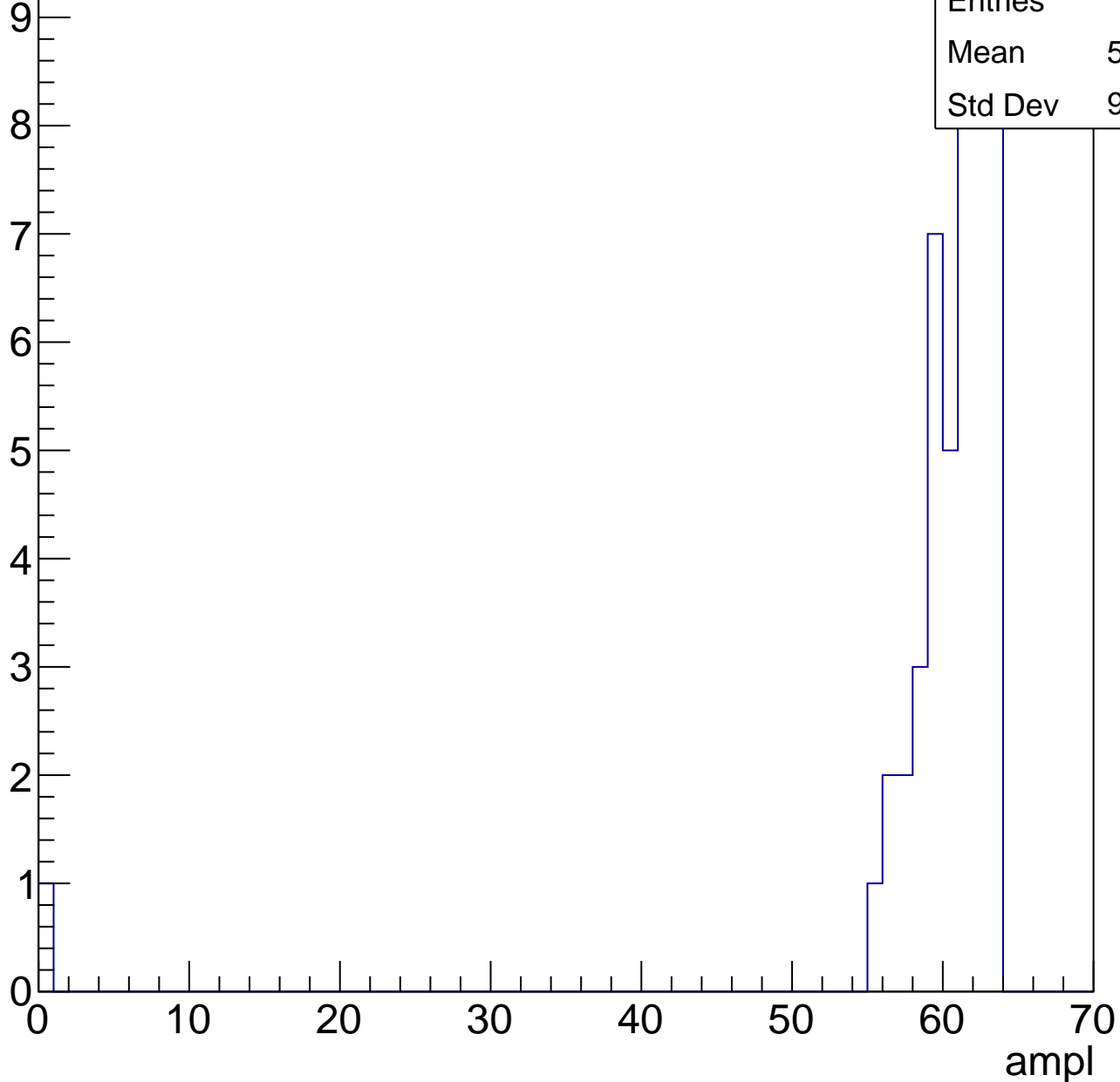
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L101S, U9-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch72, adc0

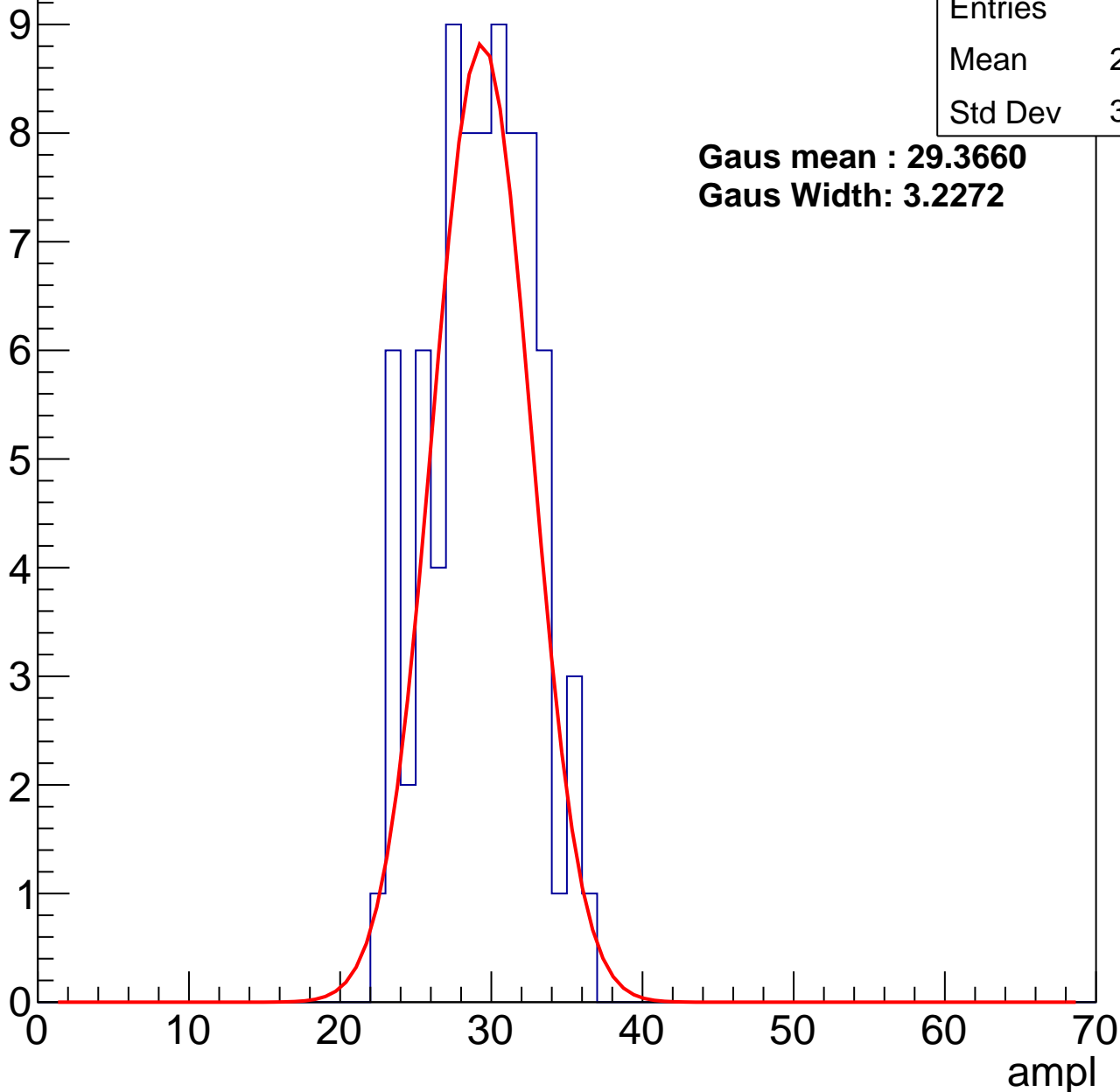
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	28.85
Std Dev	3.317

**Gaus mean : 29.3660**

**Gaus Width: 3.2272**



# B1L101S, U9-ch72, adc1

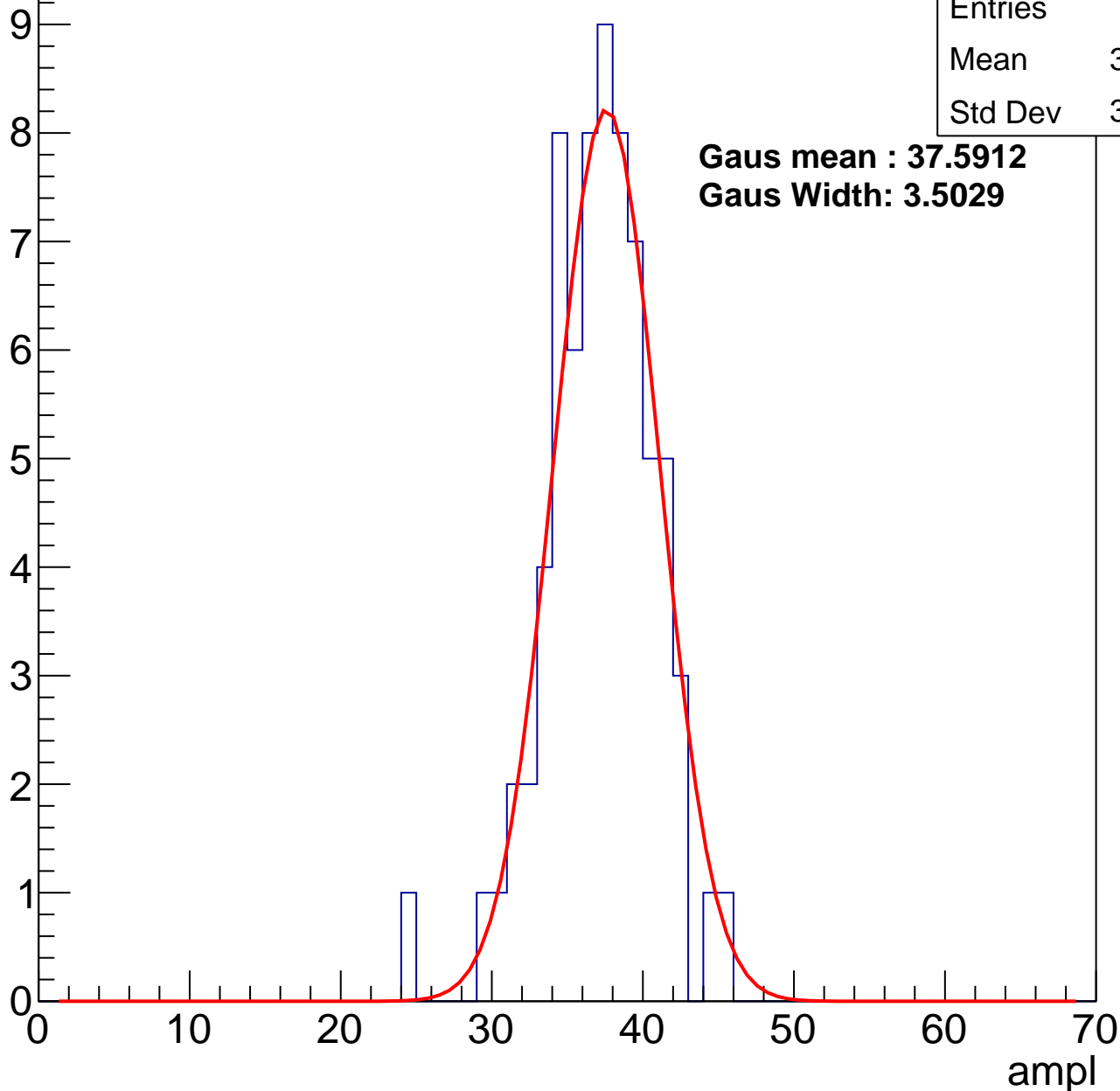
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	36.68
Std Dev	3.562

**Gaus mean : 37.5912**

**Gaus Width: 3.5029**



# B1L101S, U9-ch72, adc2

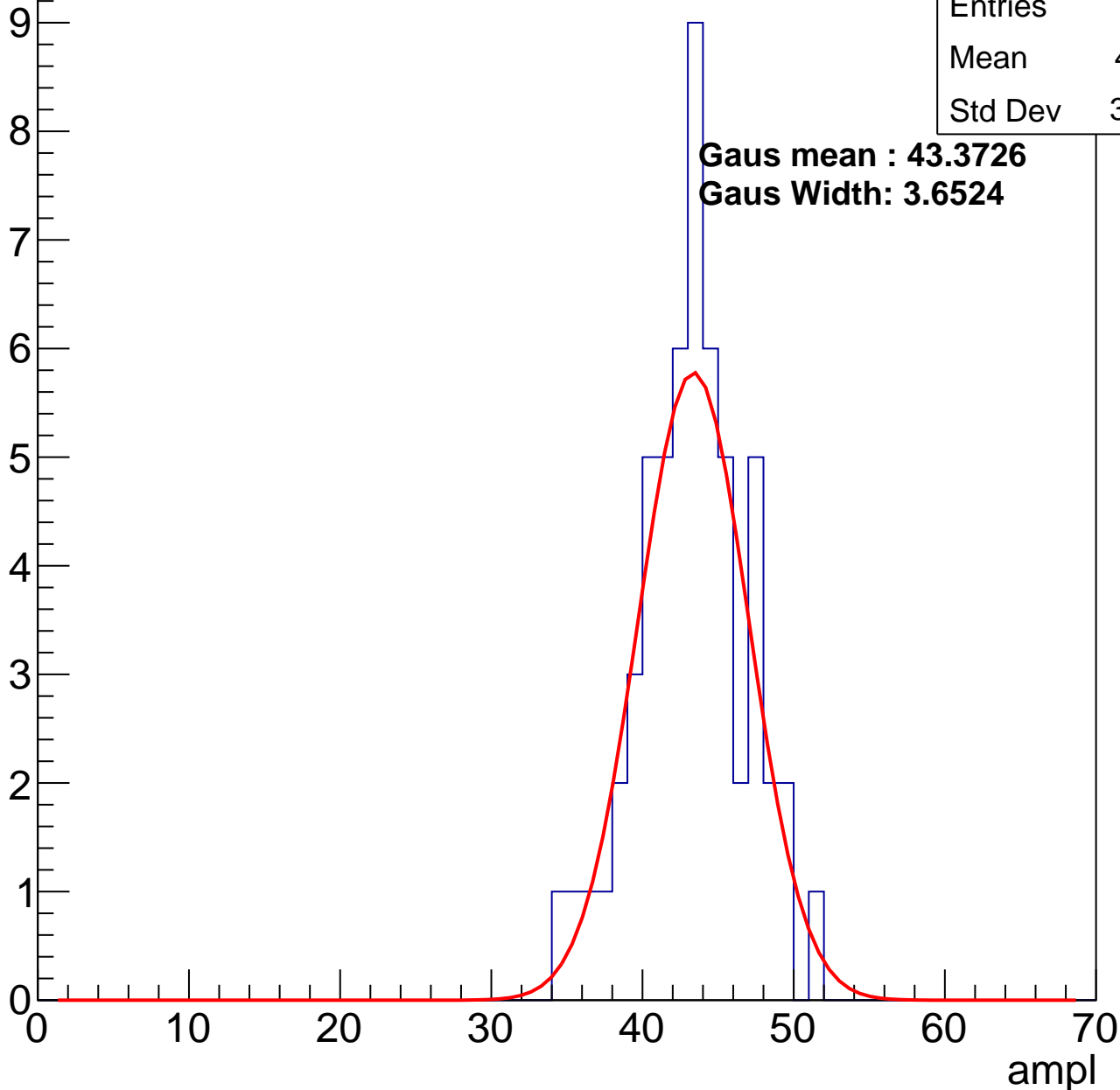
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	42.81
Std Dev	3.522

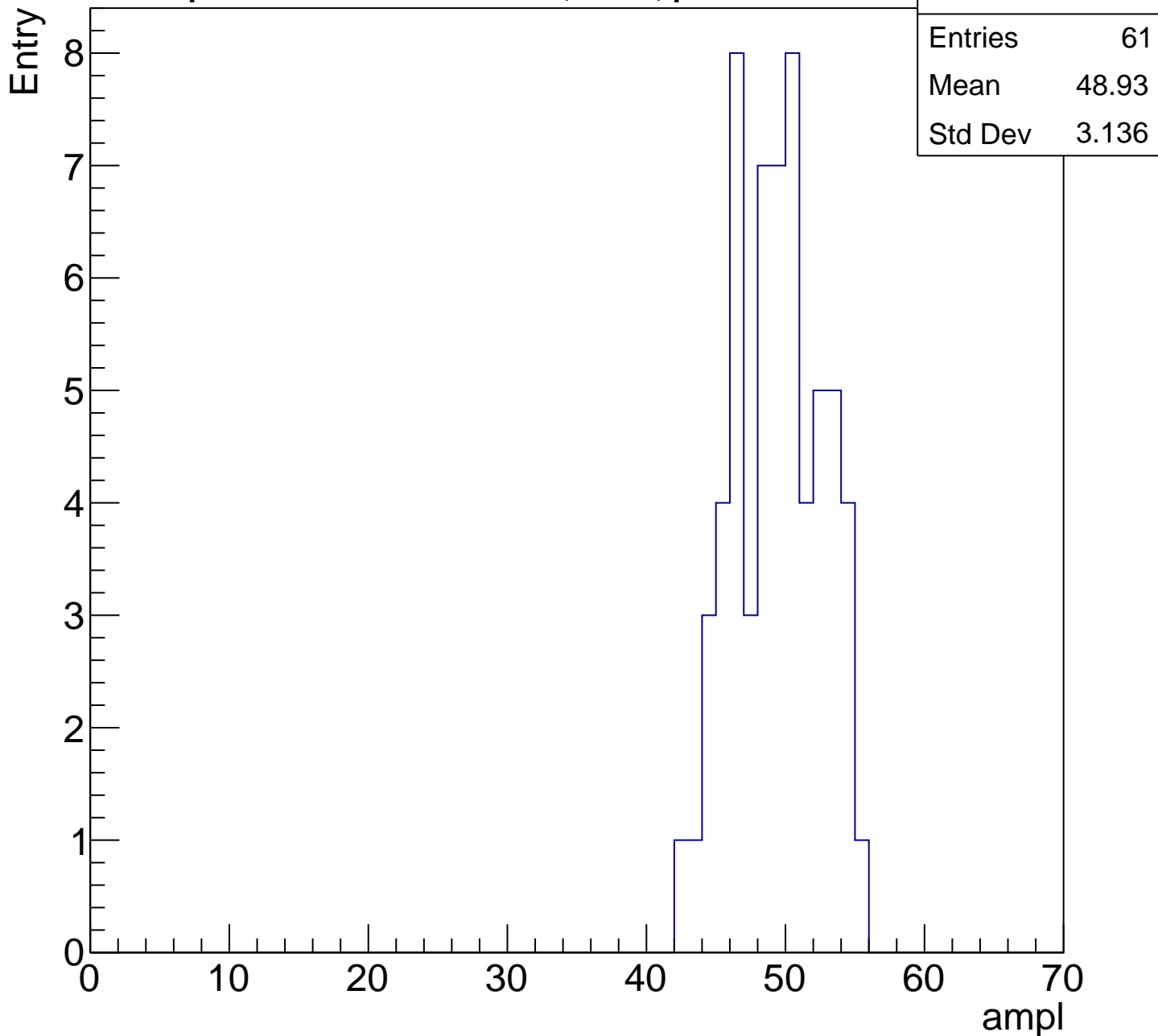
**Gaus mean : 43.3726**

**Gaus Width: 3.6524**



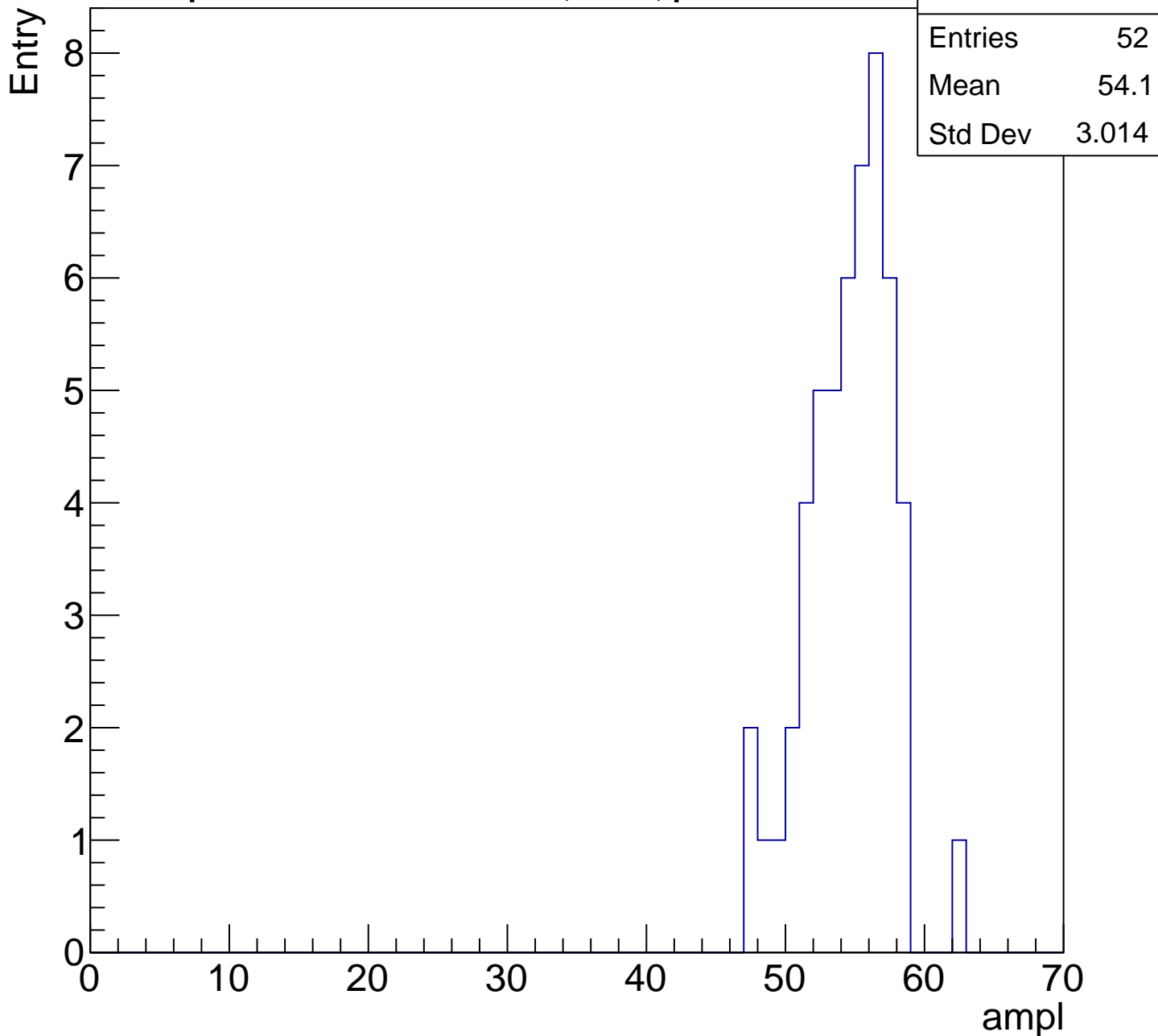
# B1L101S, U9-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

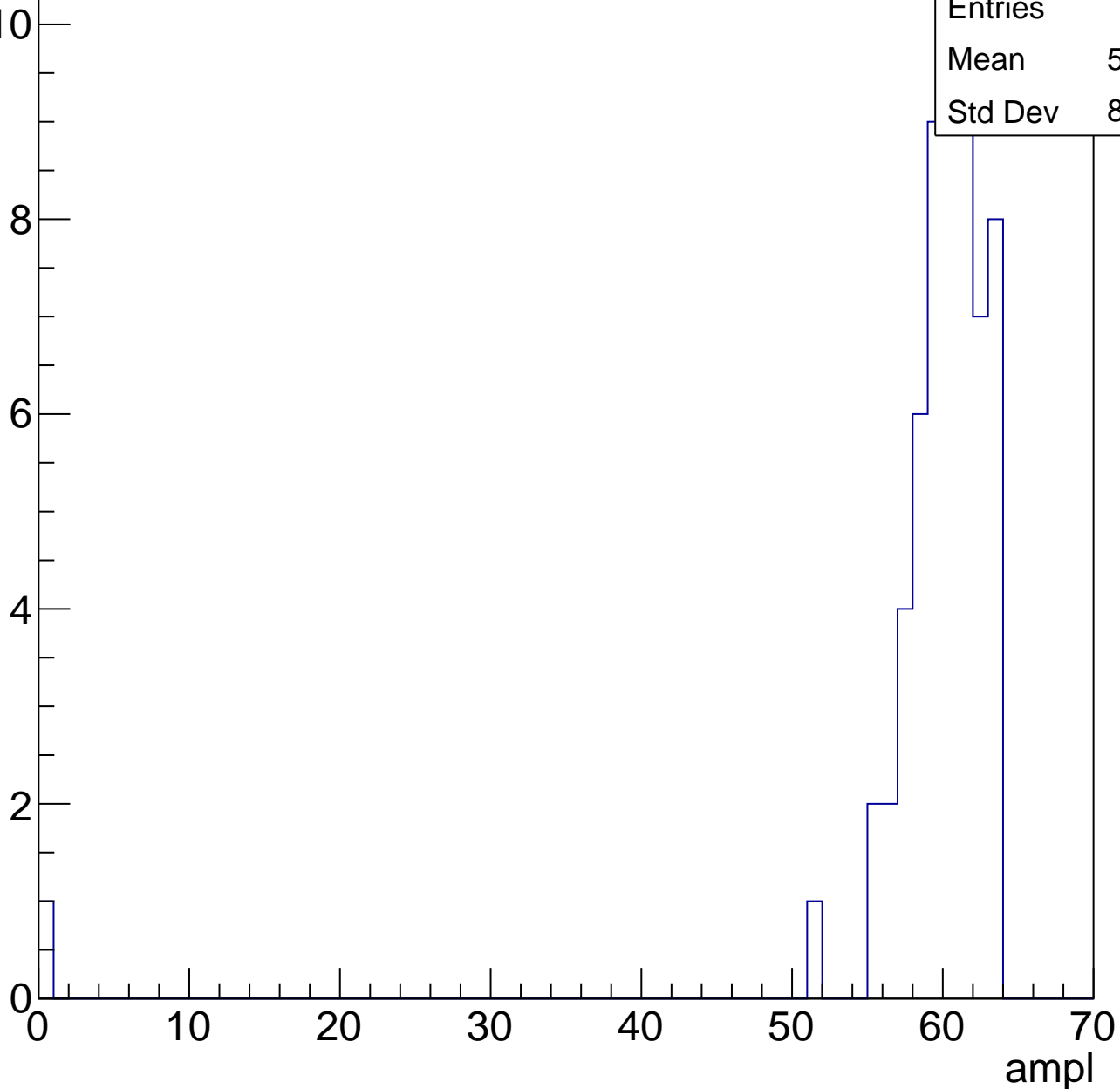


# B1L101S, U9-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

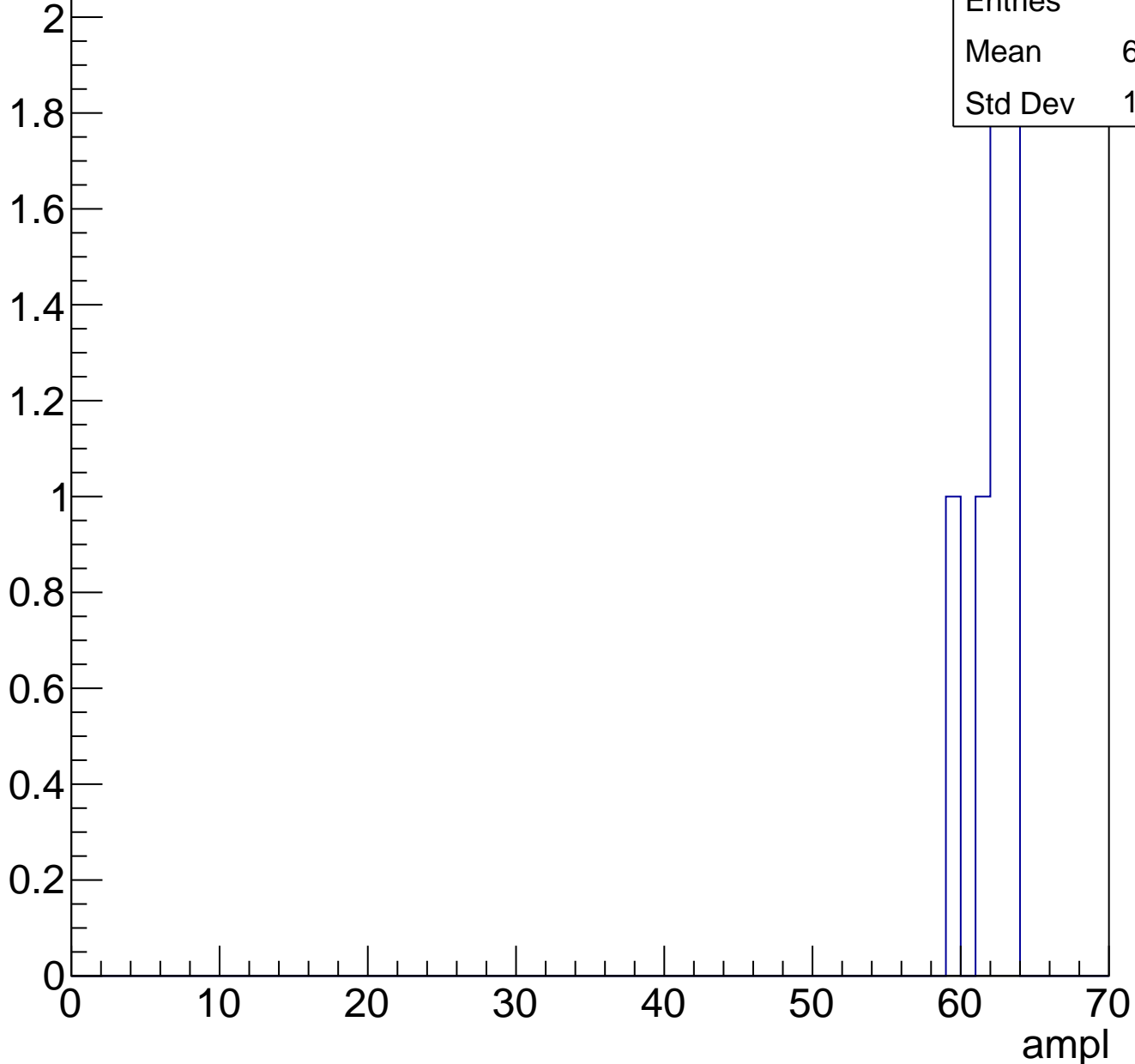
Entries	59
Mean	58.76
Std Dev	8.079



# B1L101S, U9-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U9-ch73, adc0

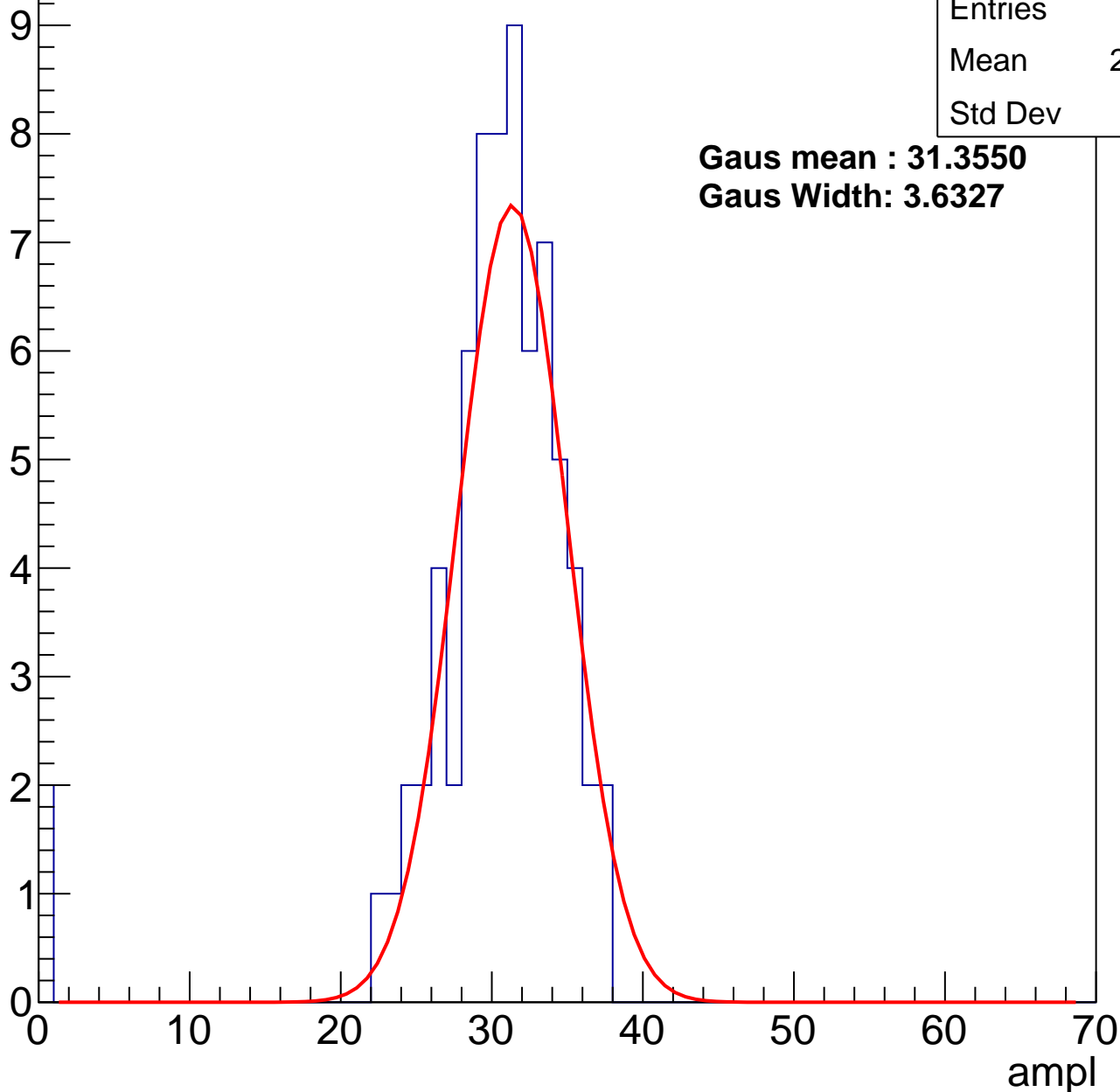
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	29.56
Std Dev	6.03

**Gaus mean : 31.3550**

**Gaus Width: 3.6327**



# B1L101S, U9-ch73, adc1

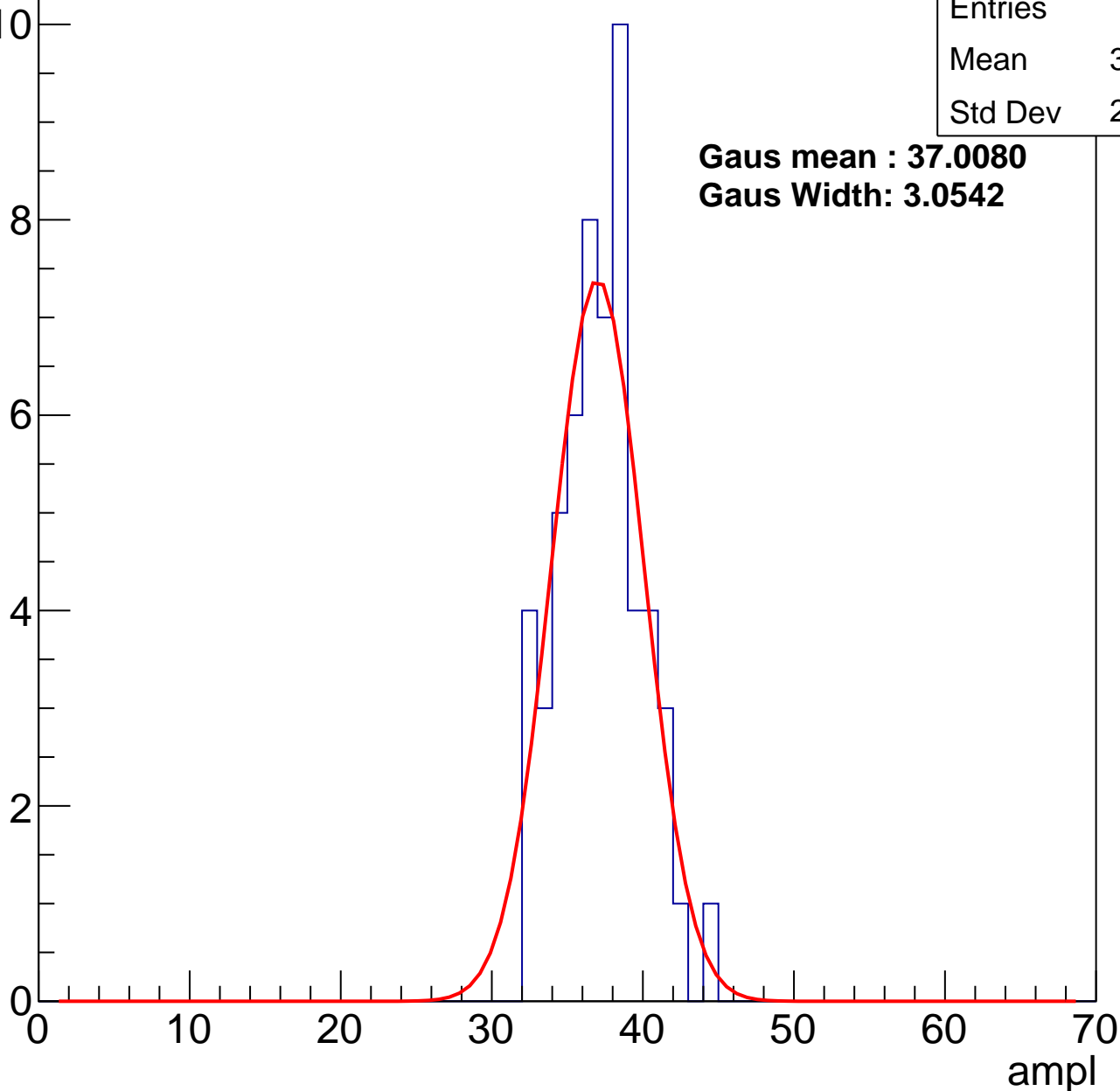
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	36.77
Std Dev	2.693

**Gaus mean : 37.0080**

**Gaus Width: 3.0542**



# B1L101S, U9-ch73, adc2

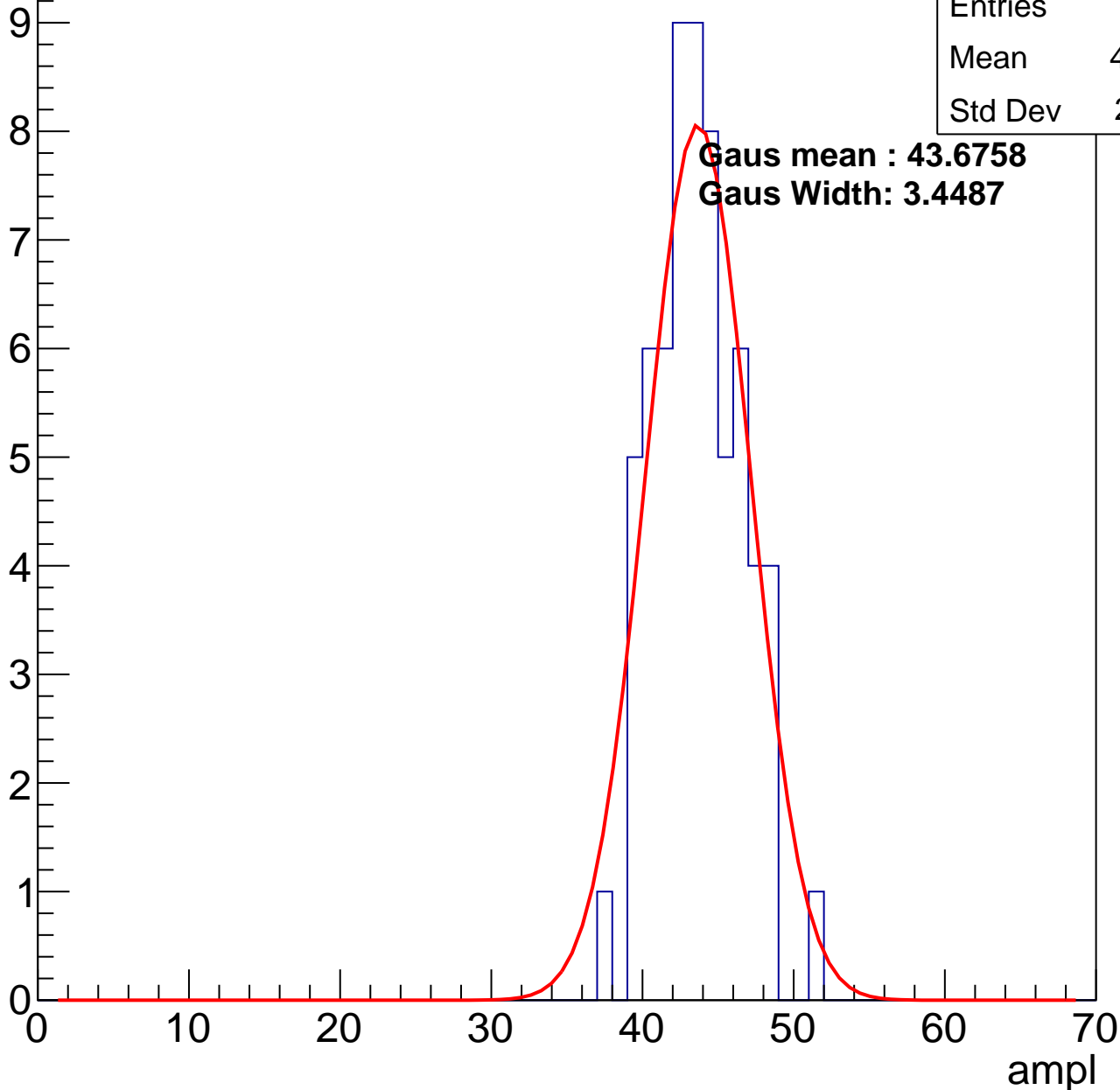
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	43.23
Std Dev	2.821

**Gaus mean : 43.6758**

**Gaus Width: 3.4487**

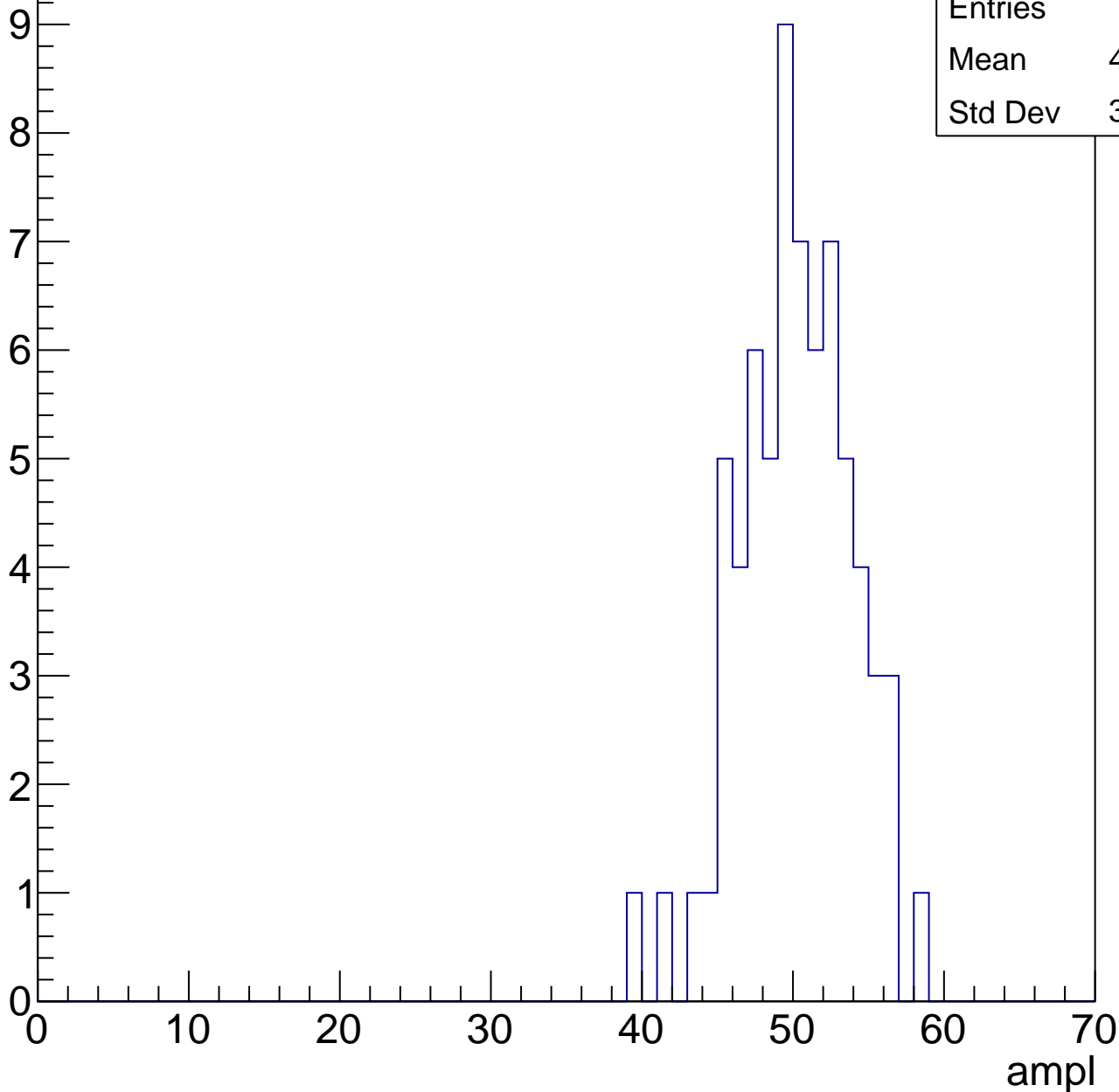


# B1L101S, U9-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	49.72
Std Dev	3.698

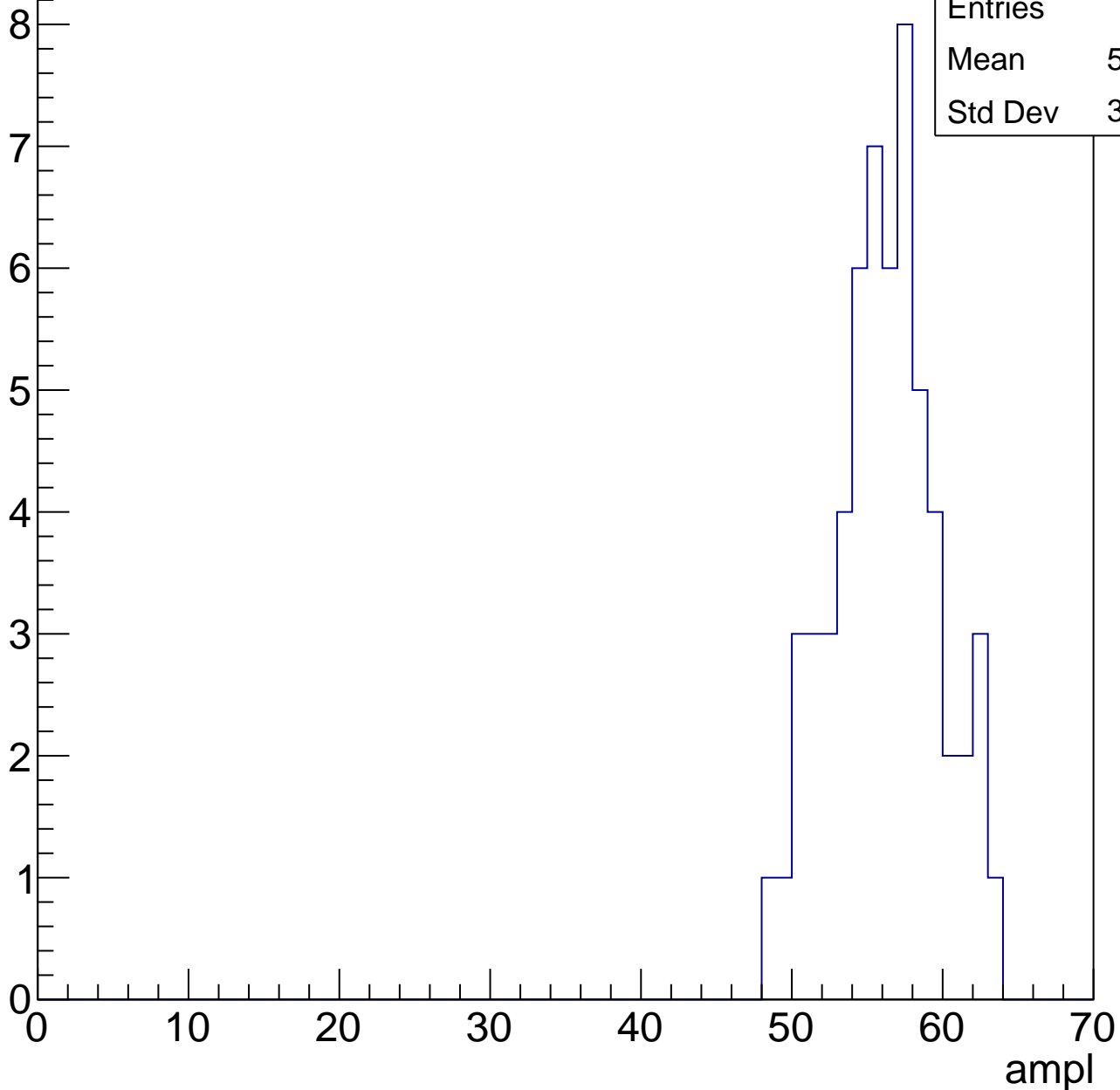


# B1L101S, U9-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

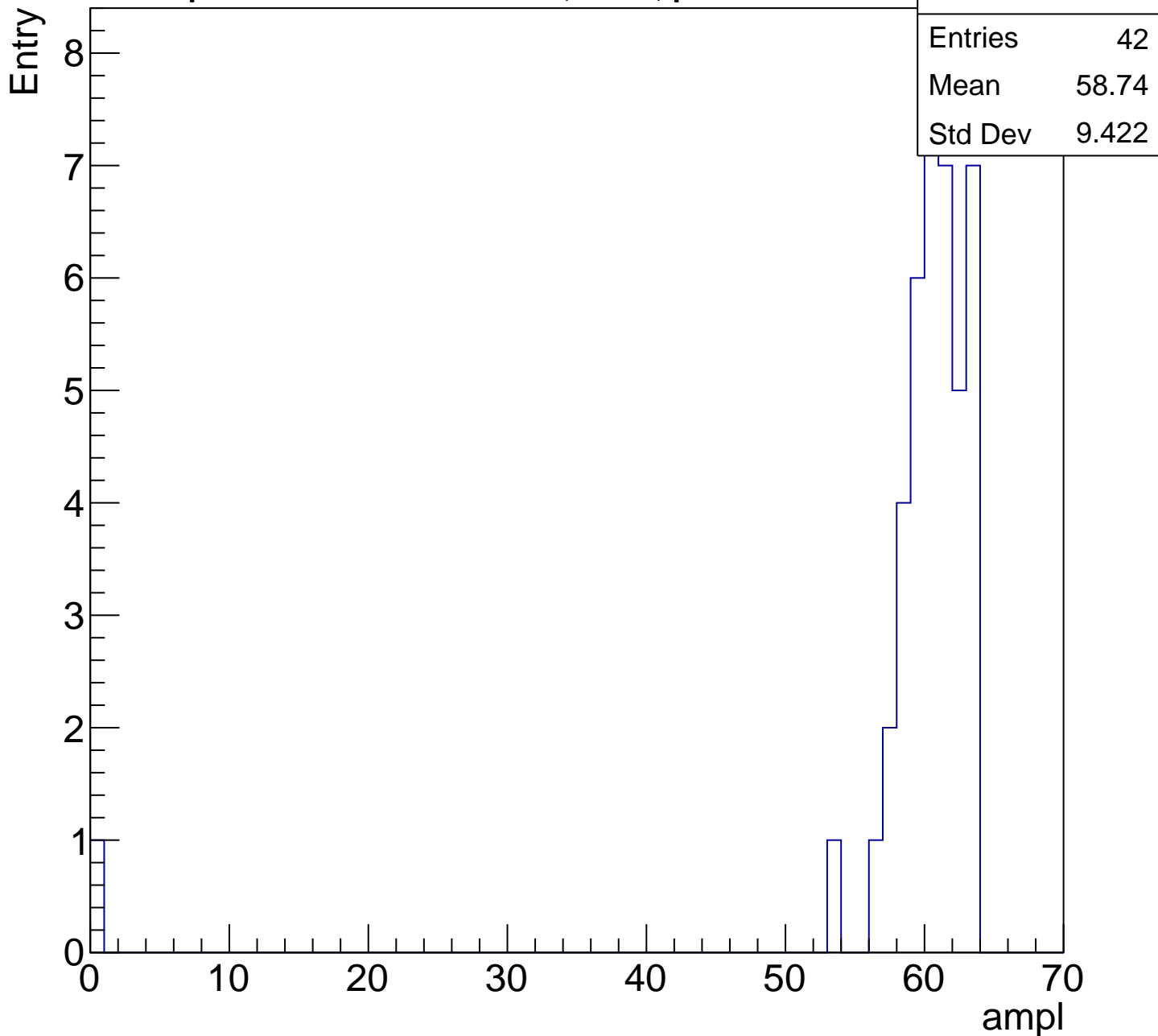
Entry

Entries	59
Mean	55.69
Std Dev	3.465



# B1L101S, U9-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	10.5
Std Dev	10.5

# B1L101S, U9-ch74, adc0

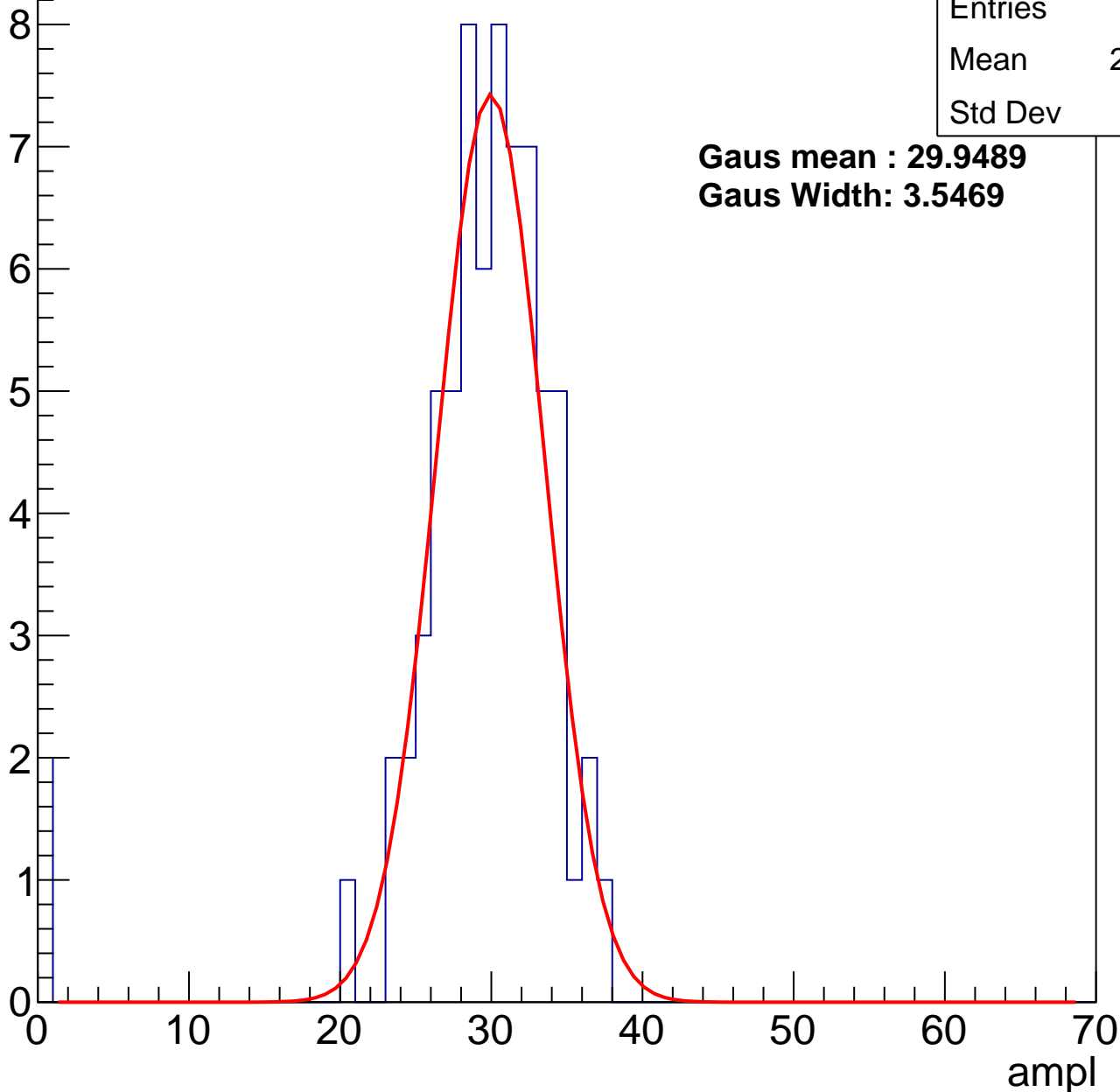
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	28.74
Std Dev	5.98

**Gaus mean : 29.9489**

**Gaus Width: 3.5469**



# B1L101S, U9-ch74, adc1

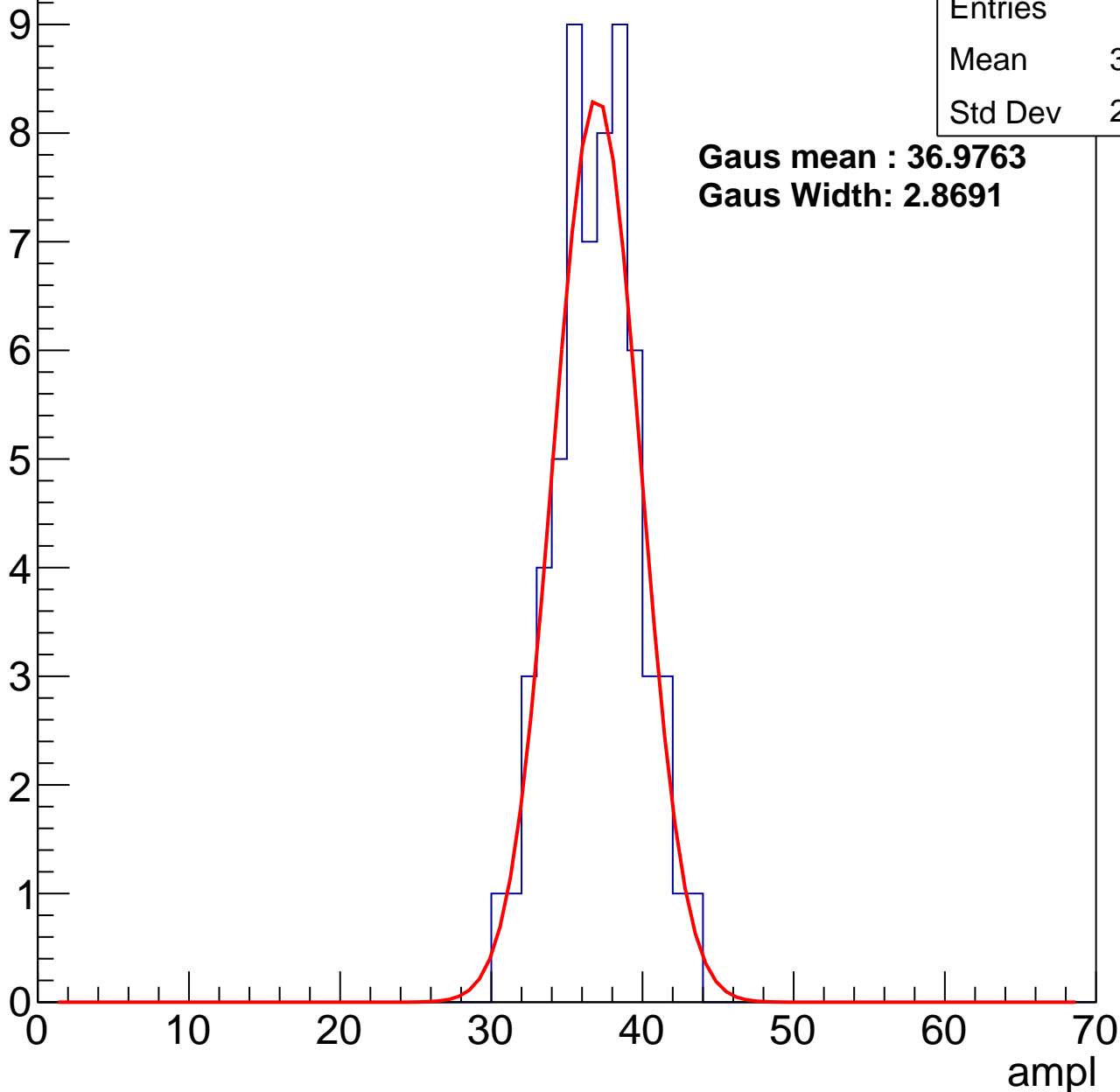
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	36.49
Std Dev	2.762

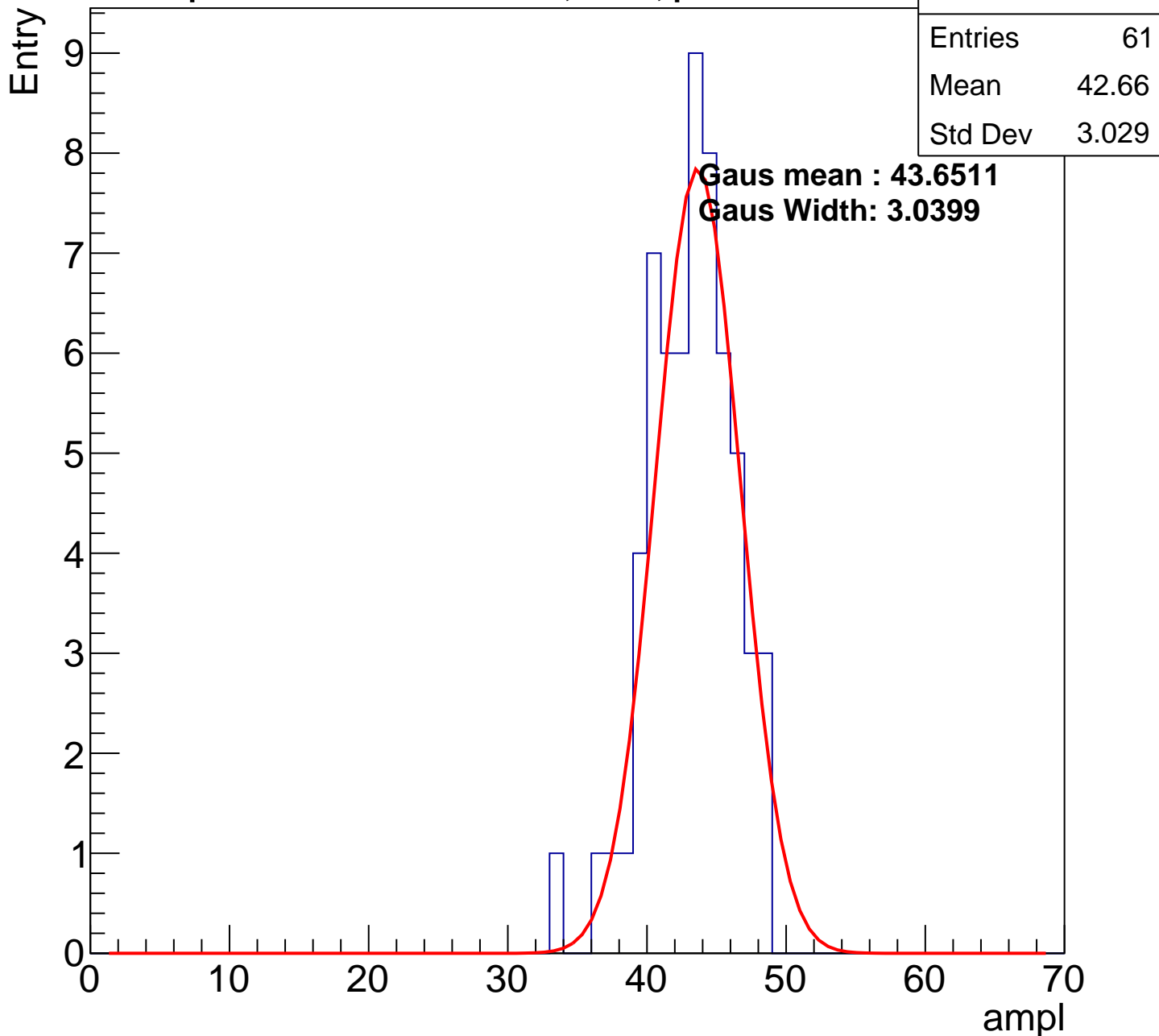
**Gaus mean : 36.9763**

**Gaus Width: 2.8691**



# B1L101S, U9-ch74, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

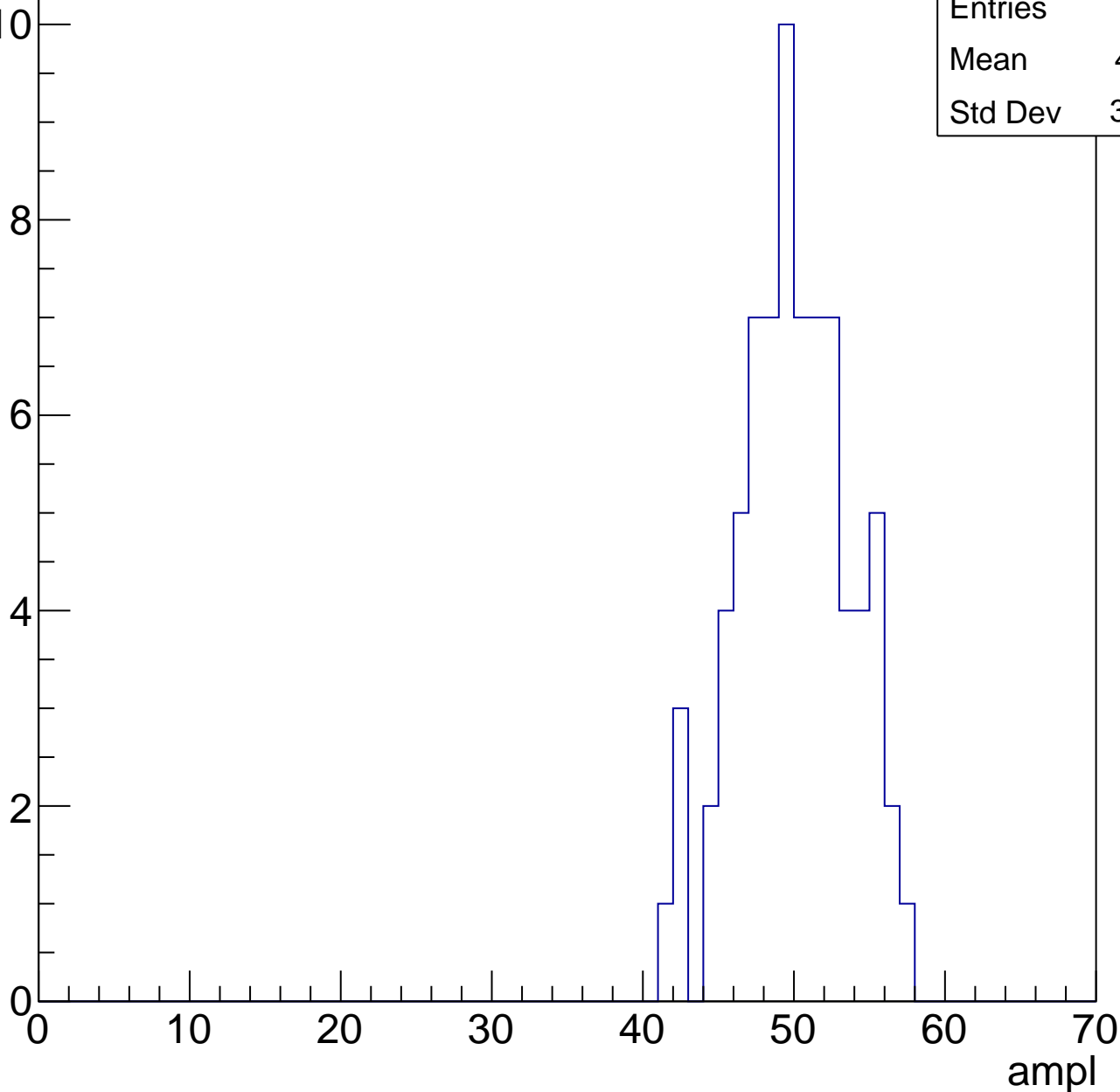


# B1L101S, U9-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

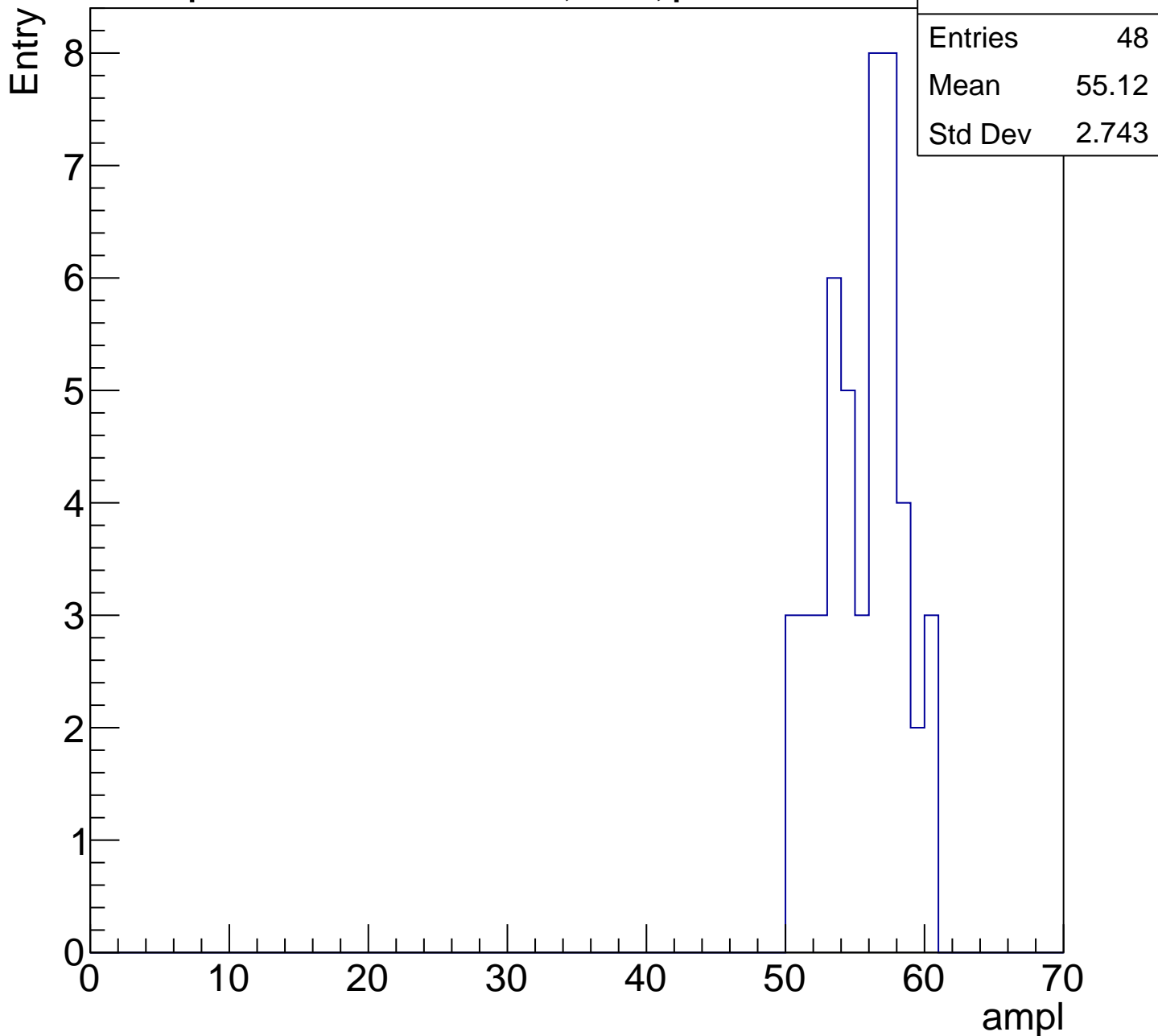
Entry

Entries	76
Mean	49.51
Std Dev	3.607



# B1L101S, U9-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

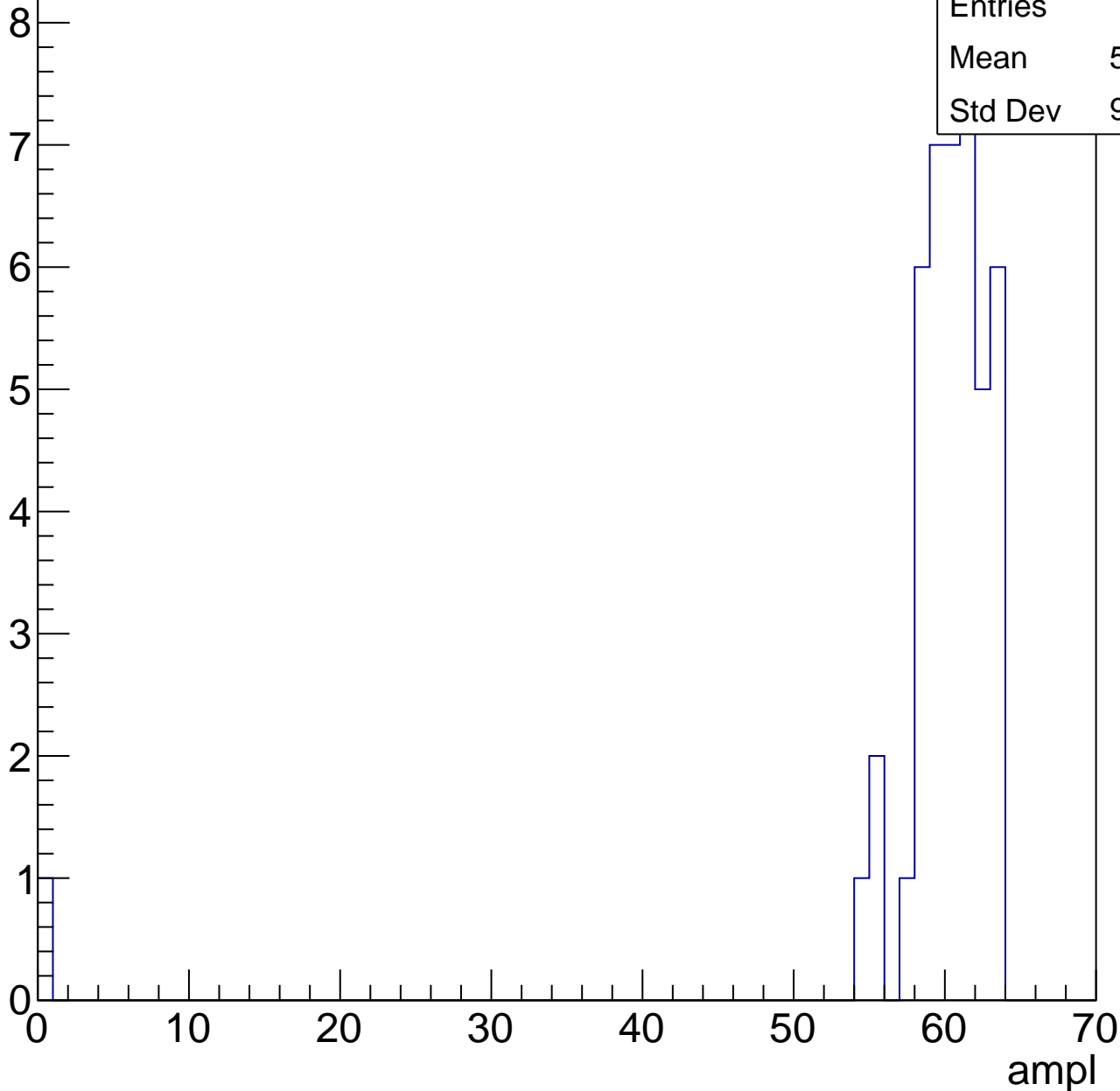


# B1L101S, U9-ch74, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	44
Mean	58.59
Std Dev	9.196

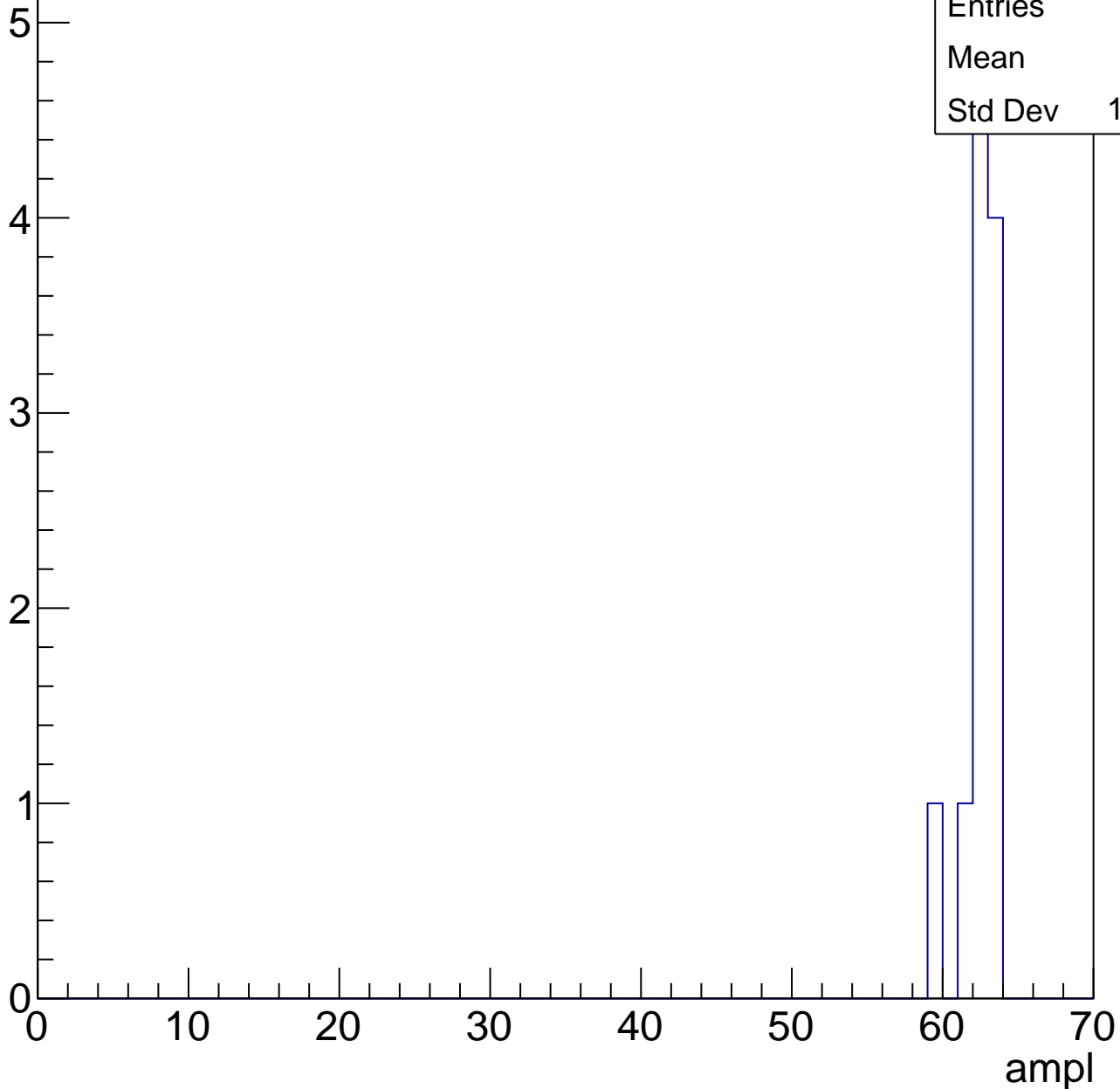


# B1L101S, U9-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	11
Mean	62
Std Dev	1.128

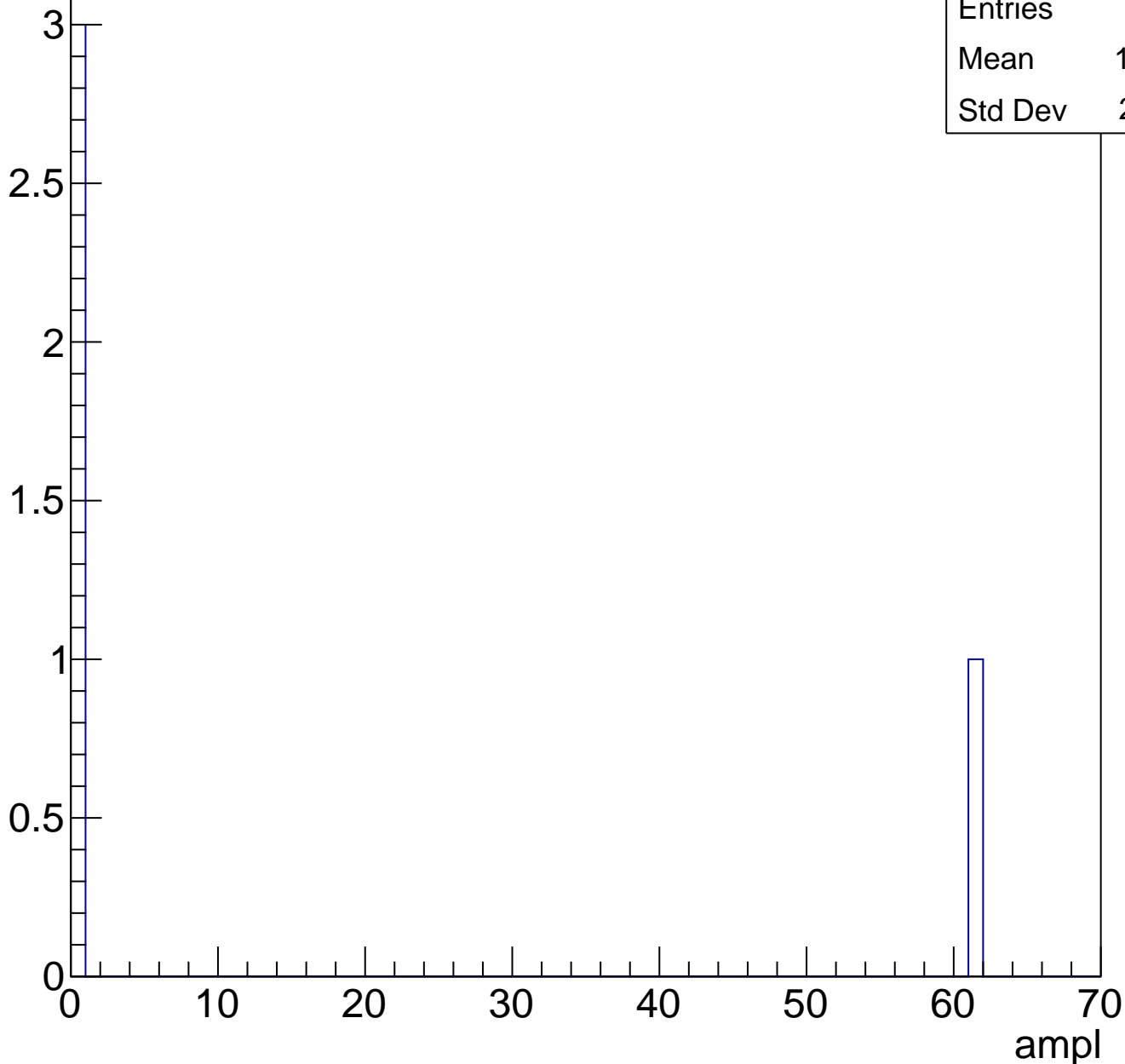




# B1L101S, U9-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch75, adc0

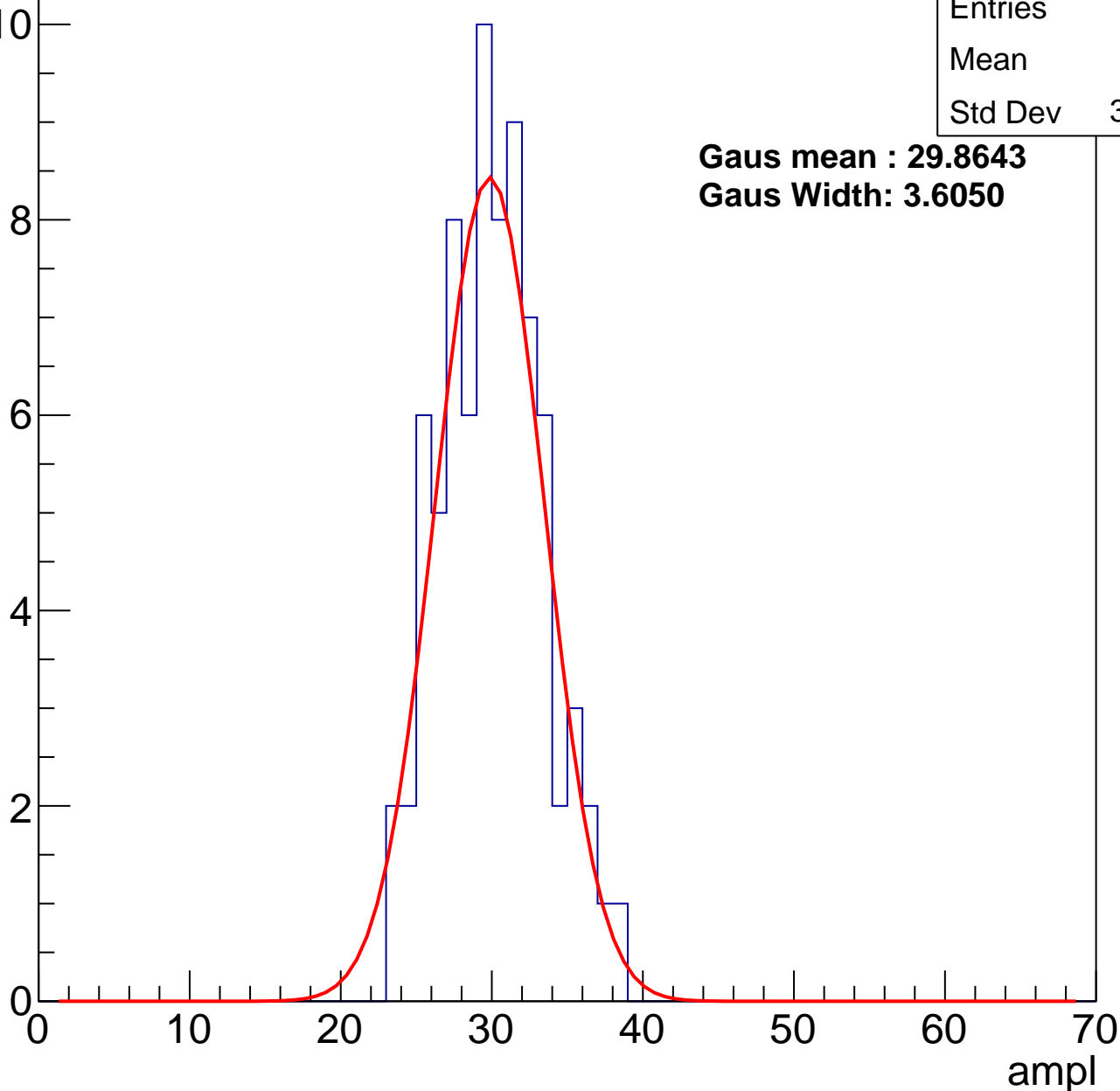
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	29.6
Std Dev	3.353

**Gaus mean : 29.8643**

**Gaus Width: 3.6050**



# B1L101S, U9-ch75, adc1

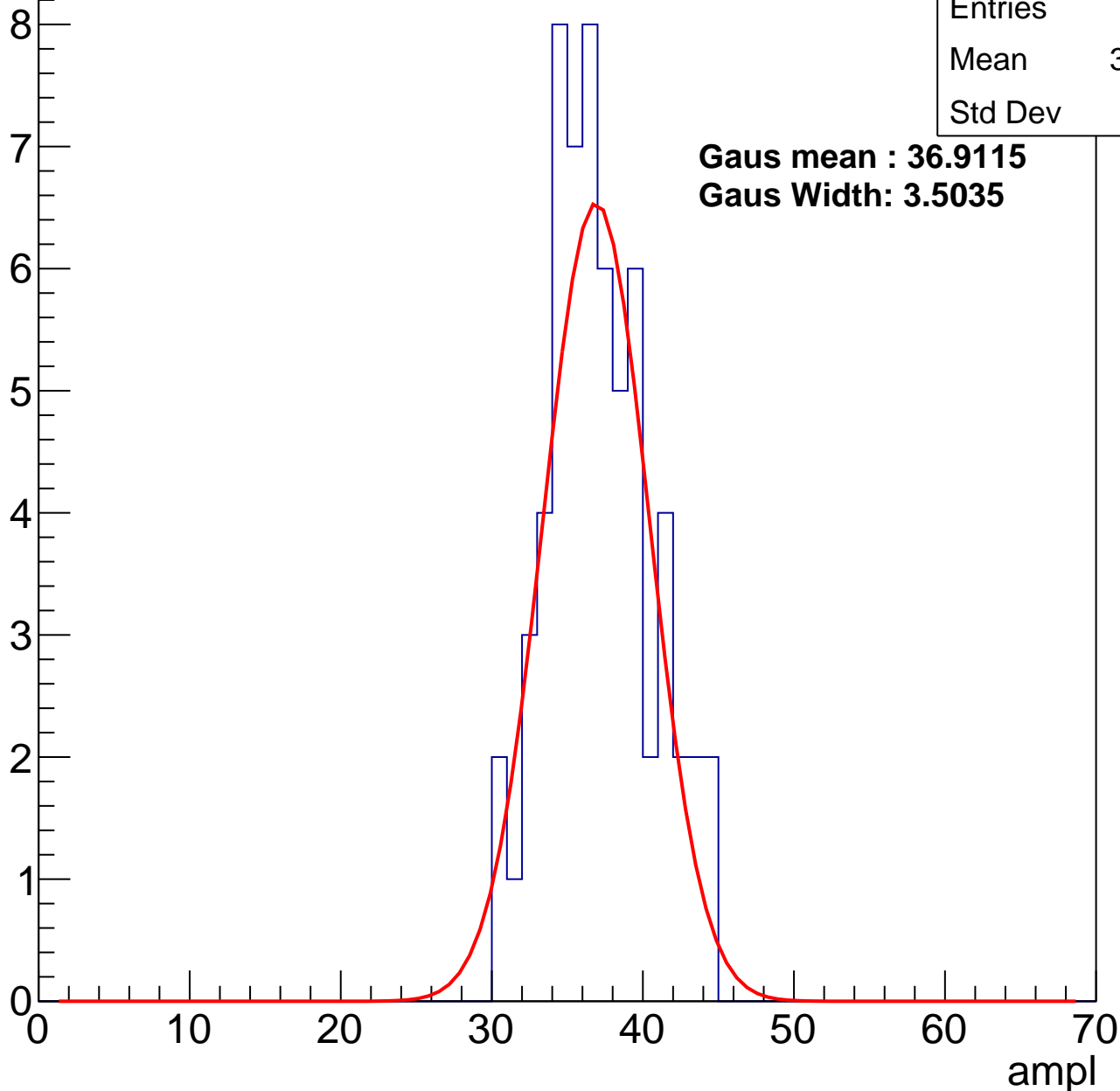
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	36.65
Std Dev	3.37

**Gaus mean : 36.9115**

**Gaus Width: 3.5035**



# B1L101S, U9-ch75, adc2

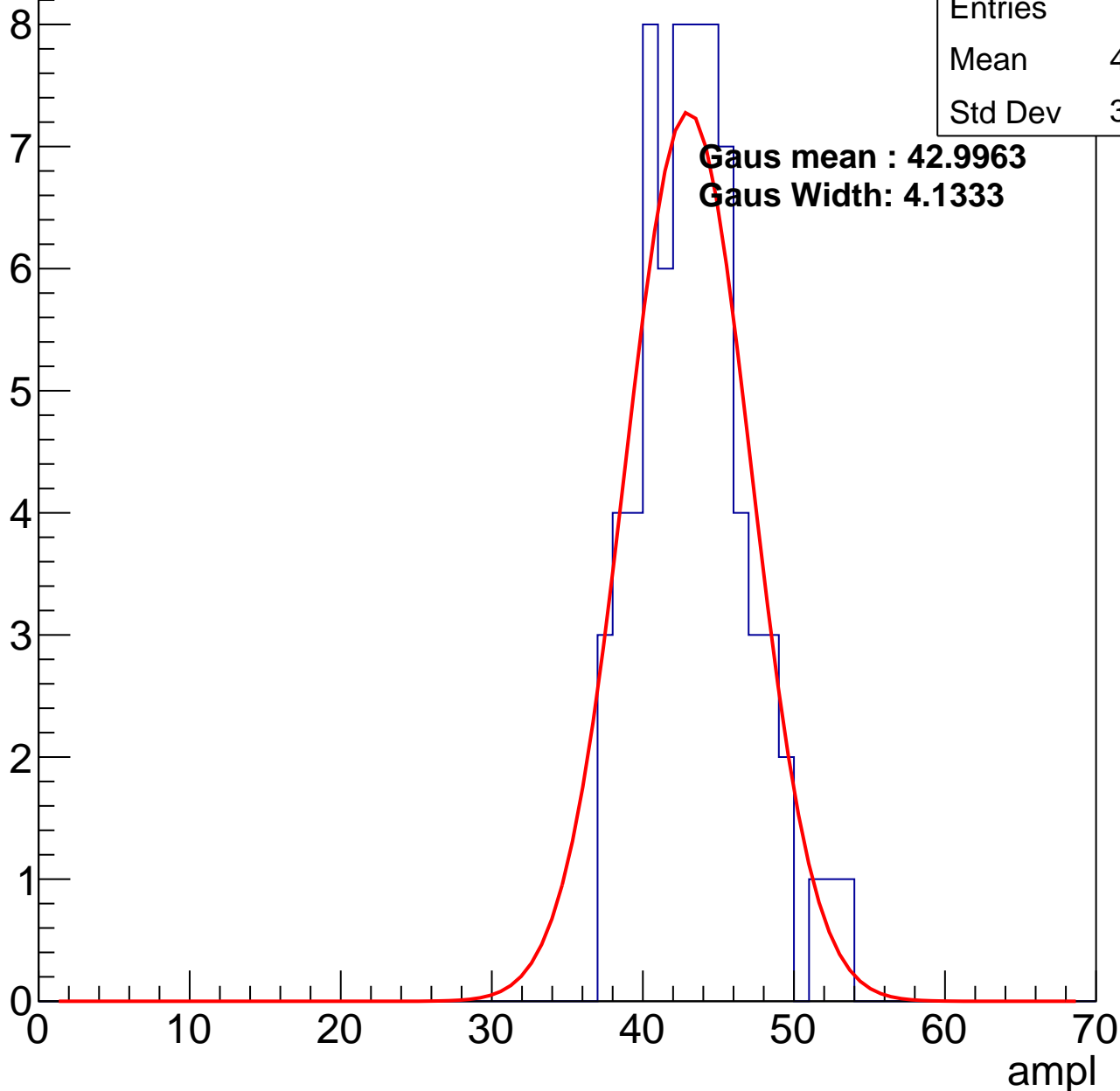
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	43.03
Std Dev	3.536

**Gaus mean : 42.9963**

**Gaus Width: 4.1333**



# B1L101S, U9-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

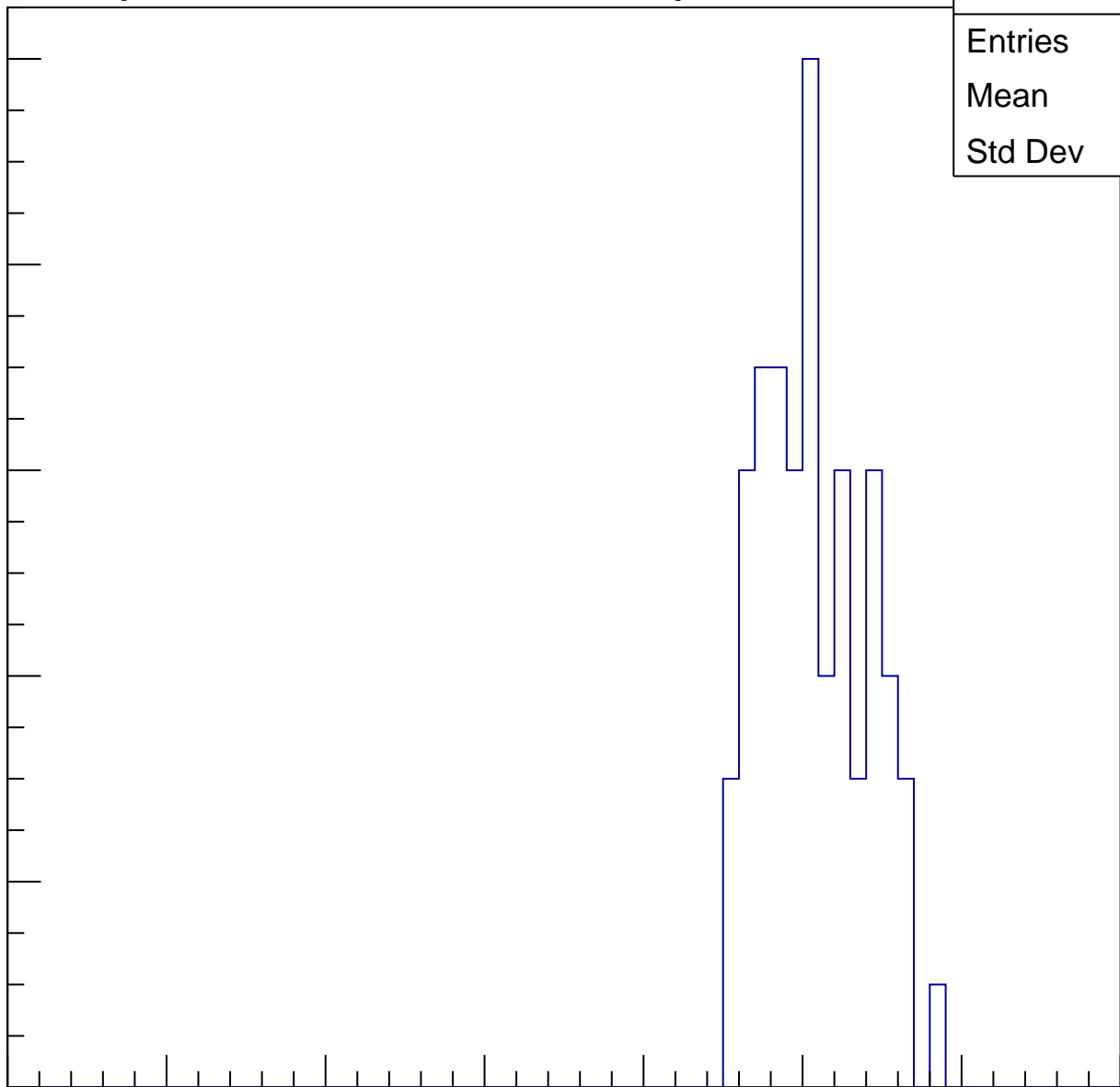
Entries	66
Mean	50.23
Std Dev	3.228

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

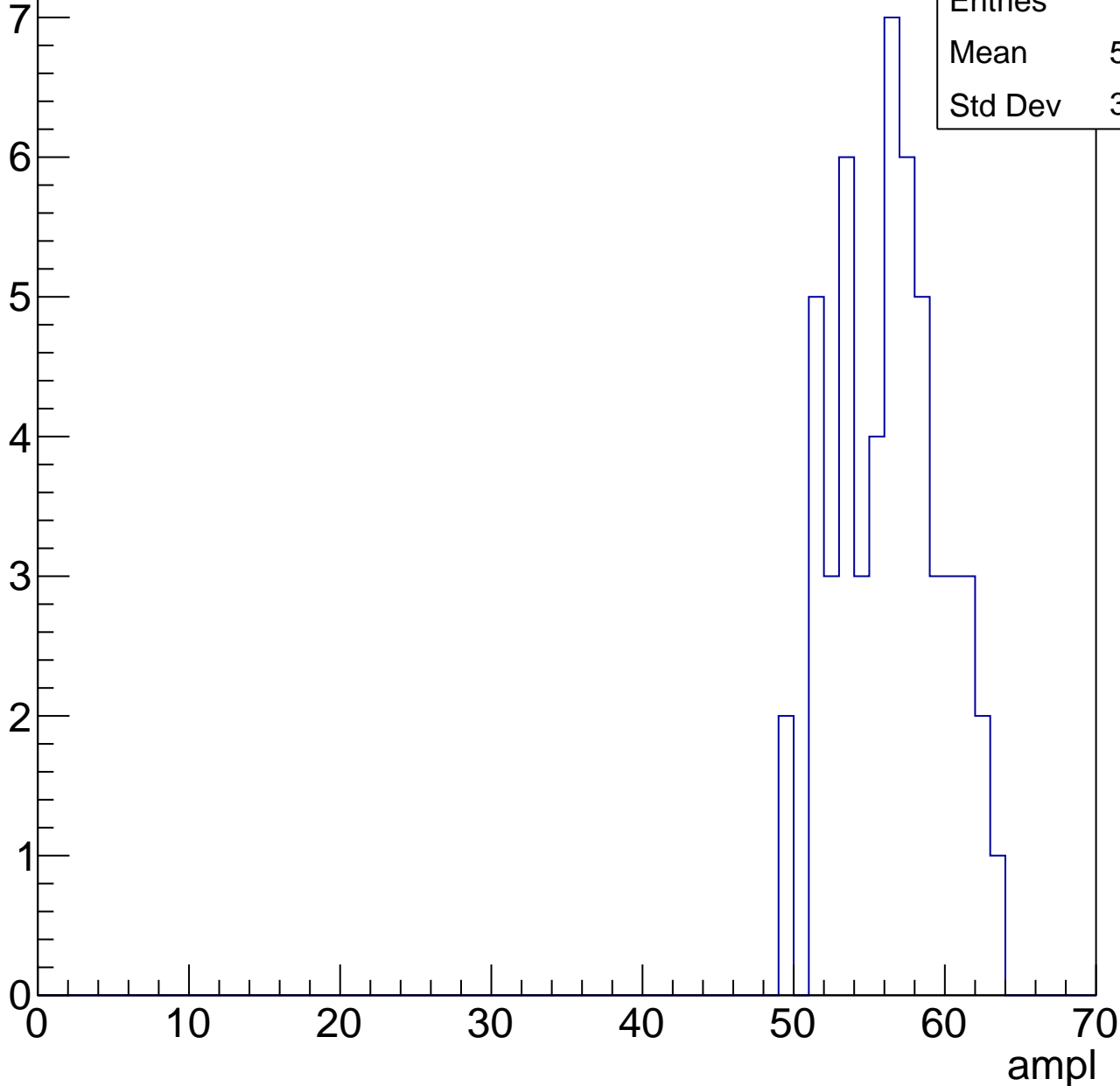


# B1L101S, U9-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

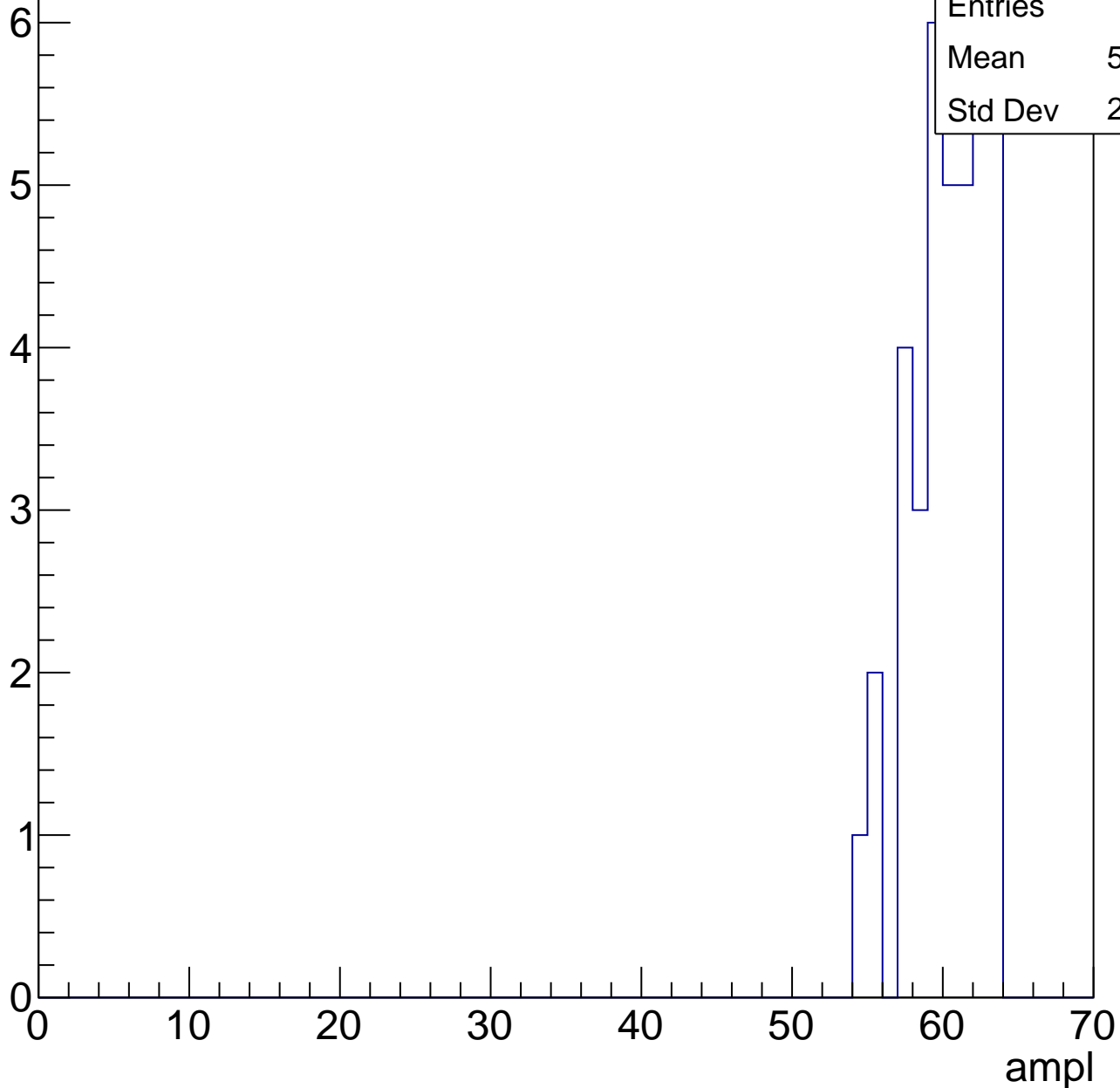
Entries	53
Mean	55.85
Std Dev	3.466



# B1L101S, U9-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

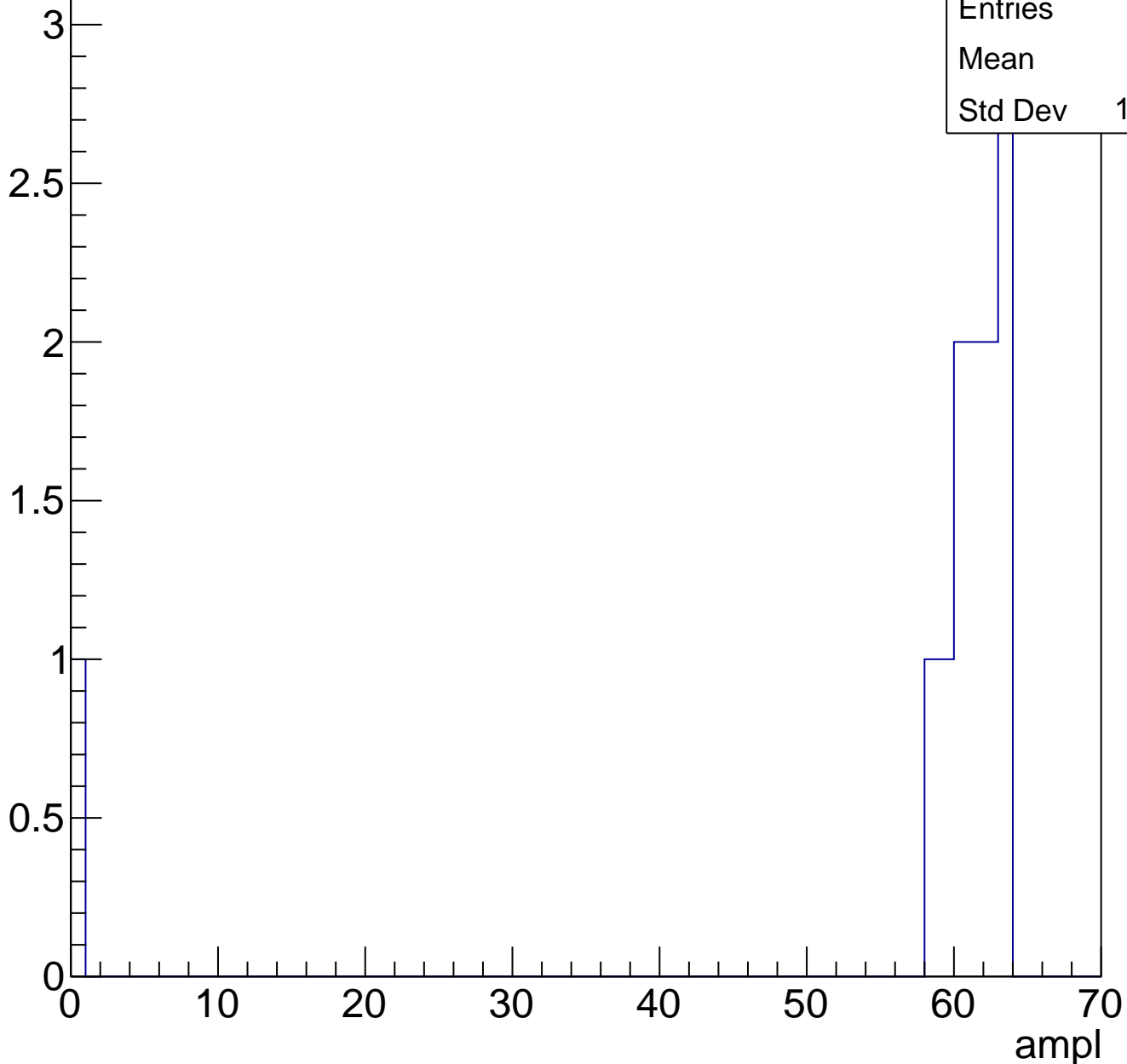
Entry



# B1L101S, U9-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

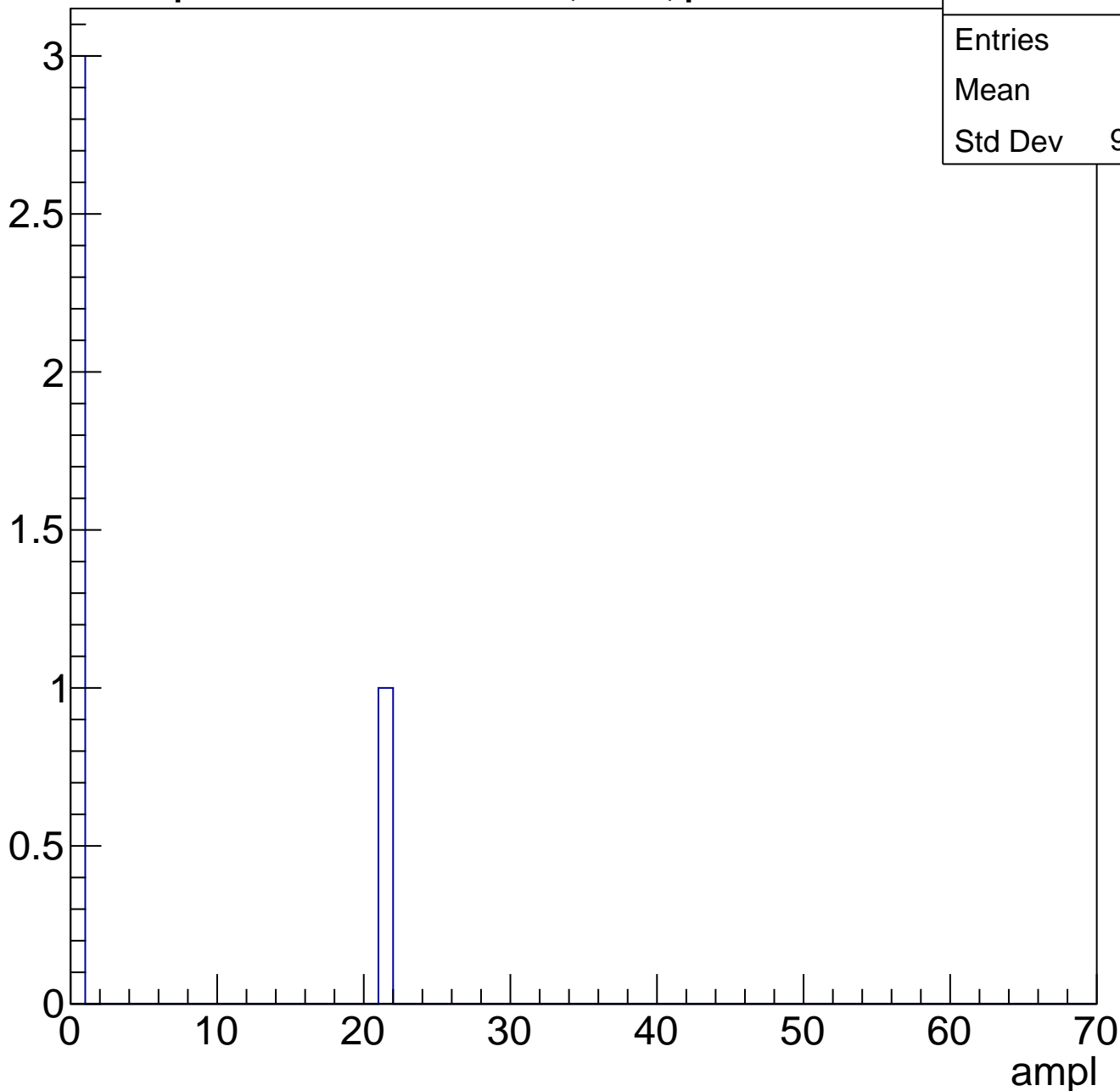




# B1L101S, U9-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	4
Mean	5.25
Std Dev	9.093

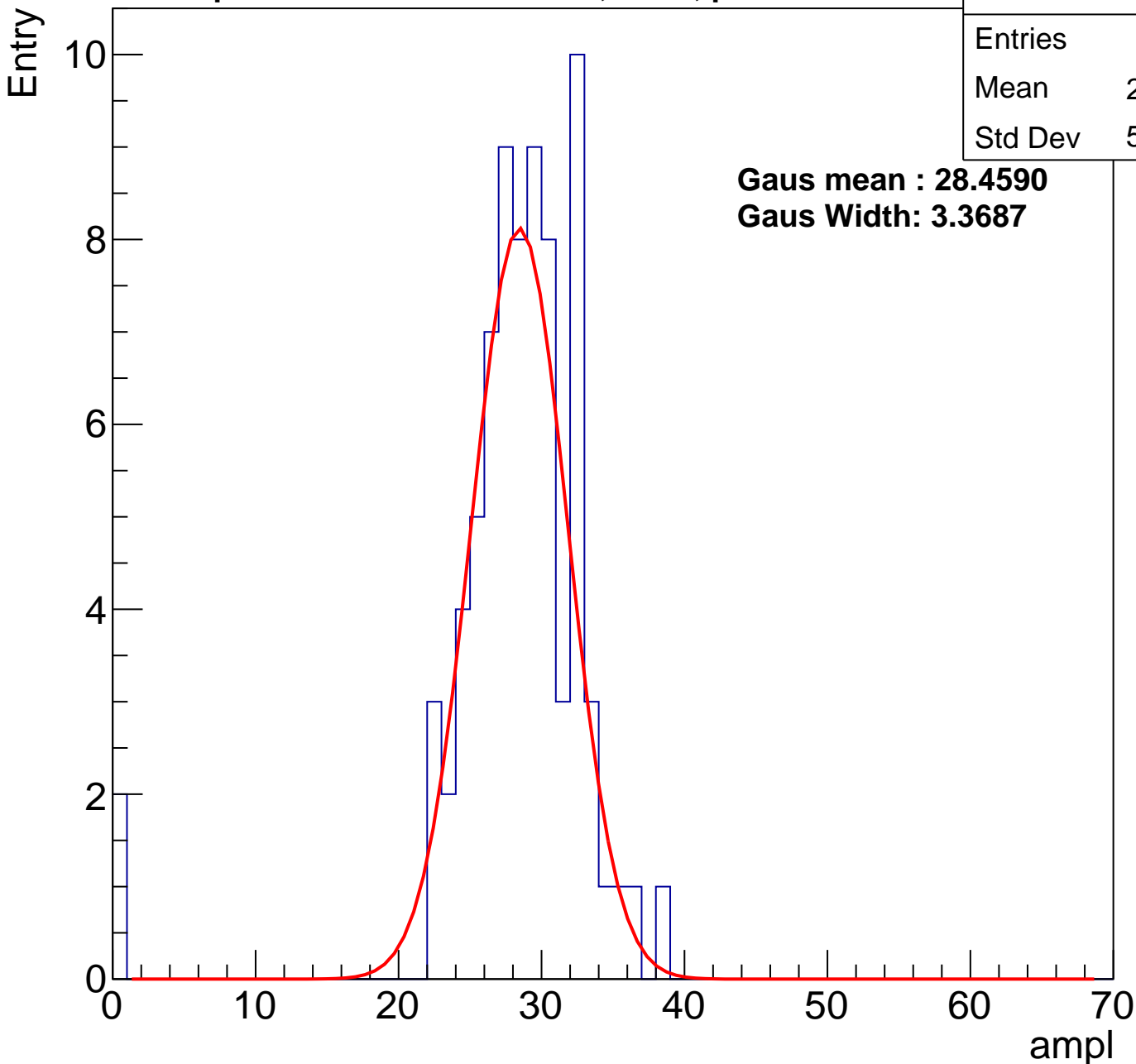
# B1L101S, U9-ch76, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	77
Mean	27.77
Std Dev	5.606

**Gaus mean : 28.4590**

**Gaus Width: 3.3687**



# B1L101S, U9-ch76, adc1

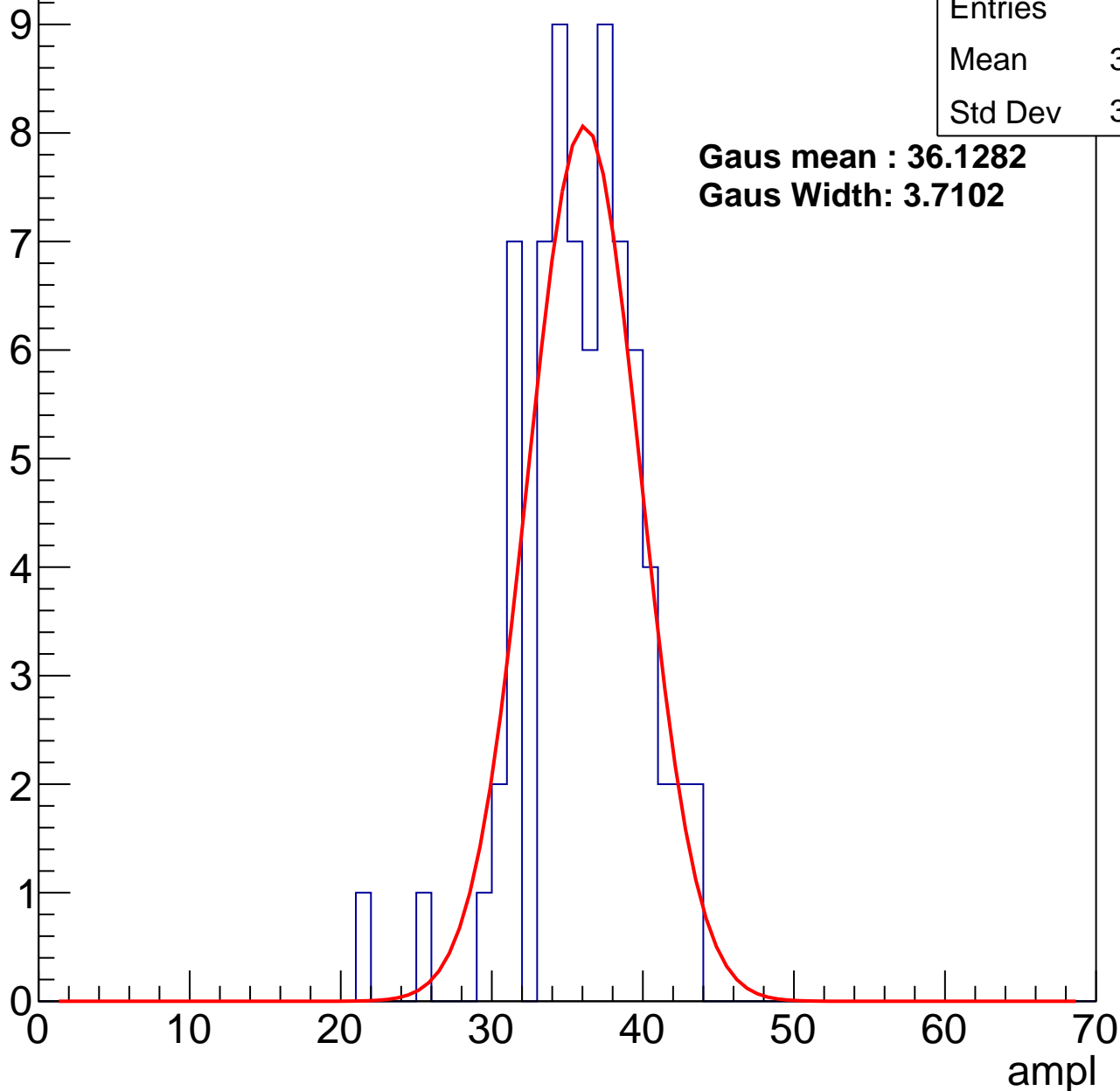
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	35.55
Std Dev	3.896

**Gaus mean : 36.1282**

**Gaus Width: 3.7102**



# B1L101S, U9-ch76, adc2

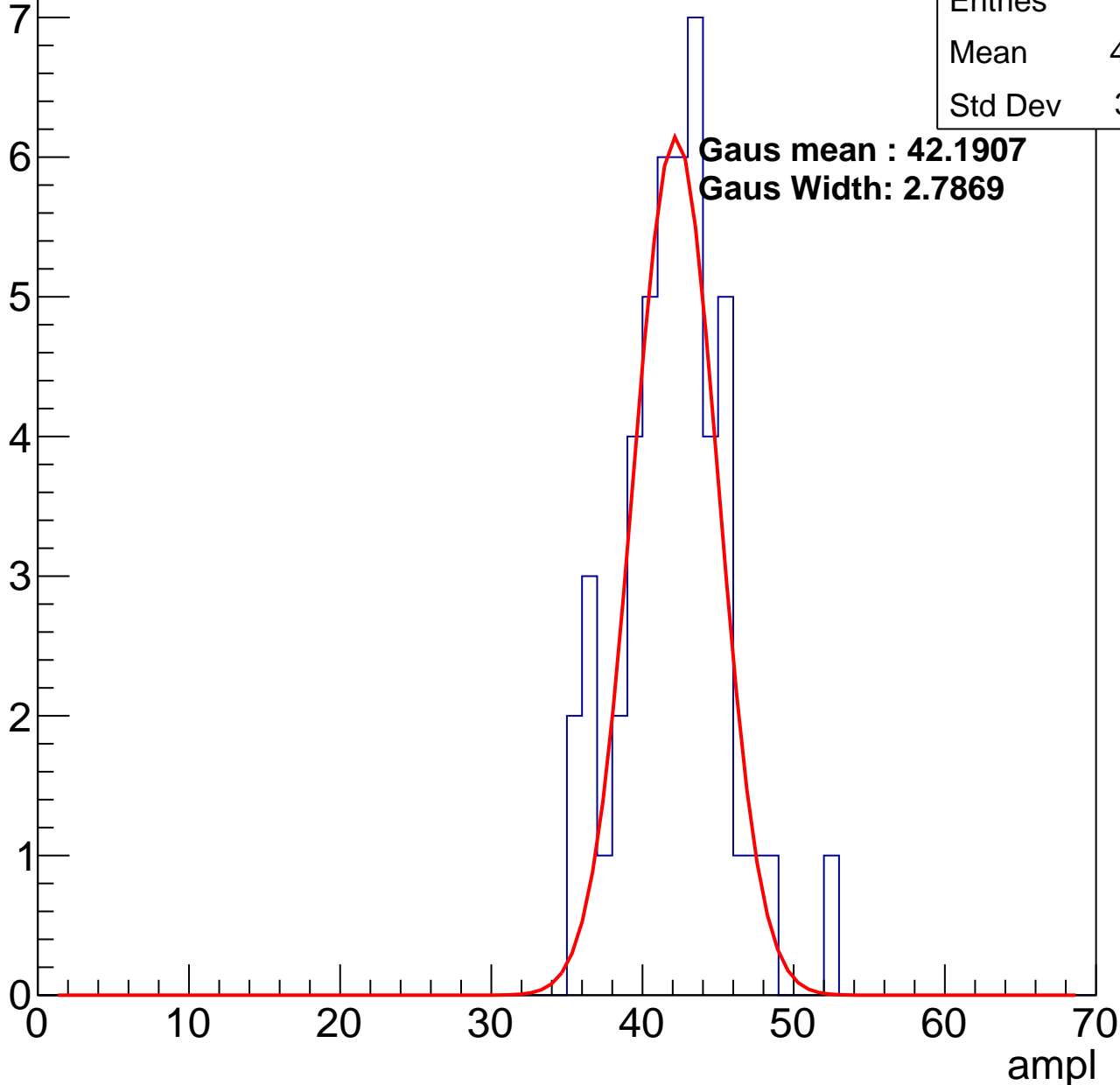
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	41.63
Std Dev	3.391

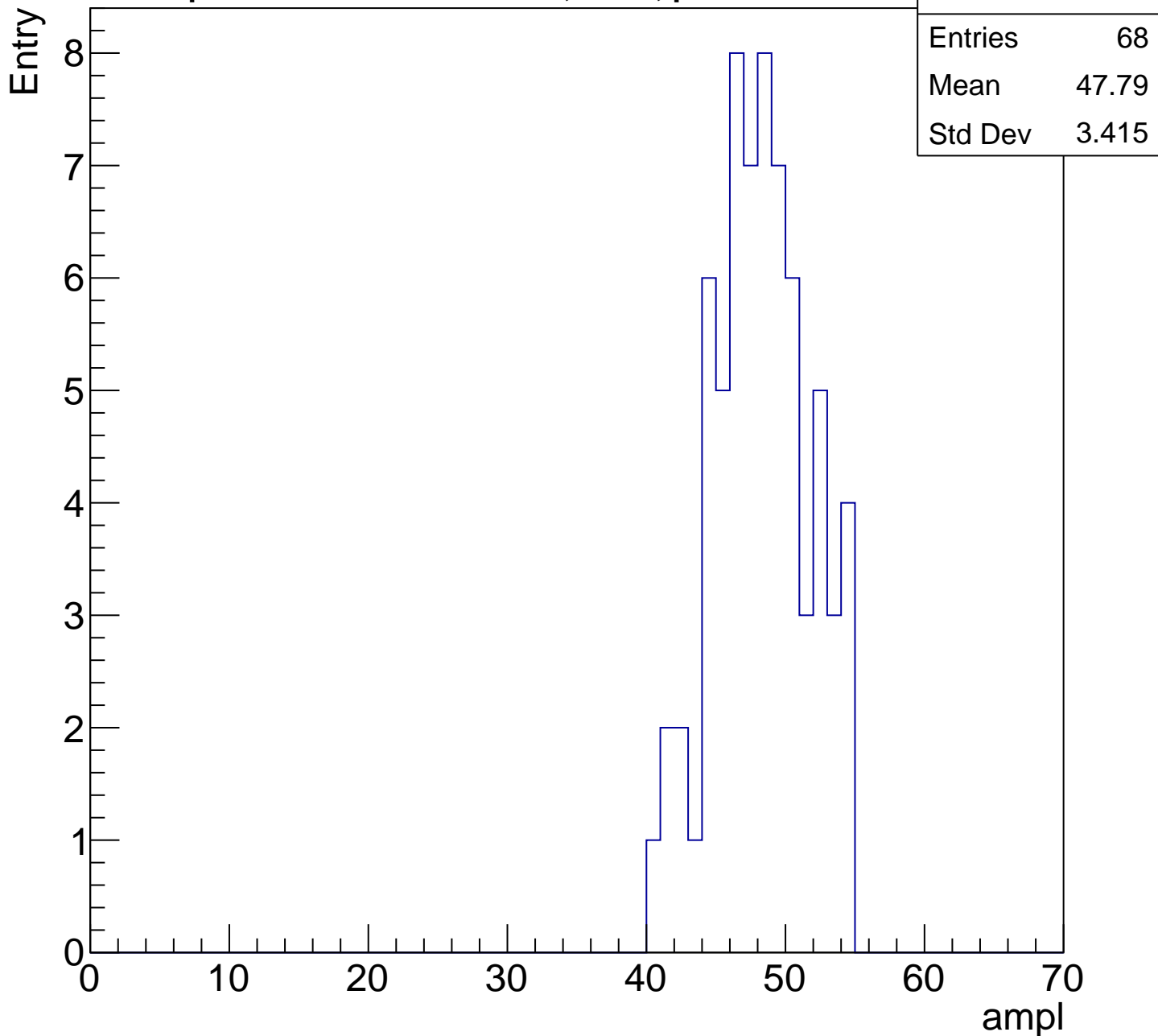
**Gaus mean : 42.1907**

**Gaus Width: 2.7869**



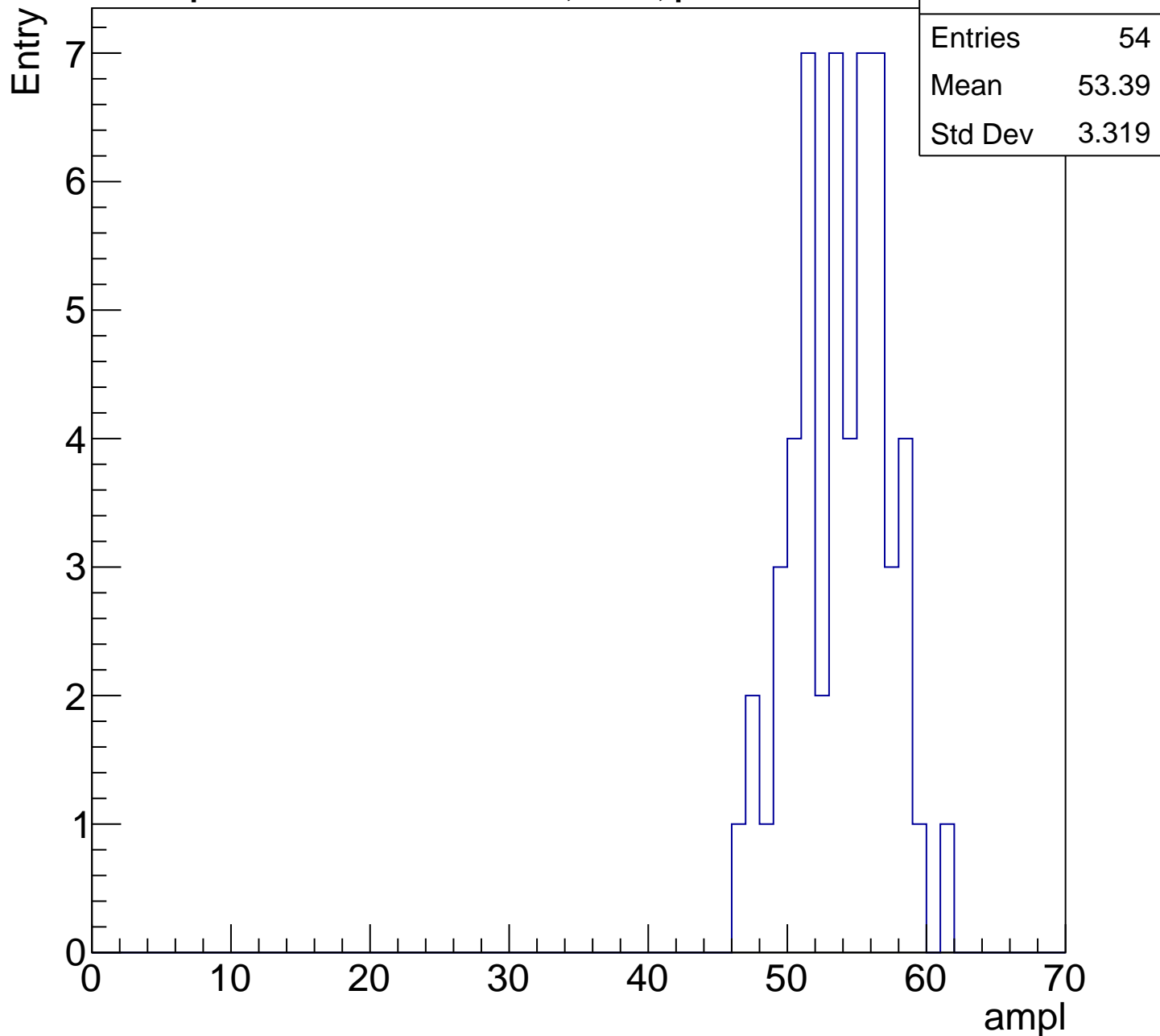
# B1L101S, U9-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

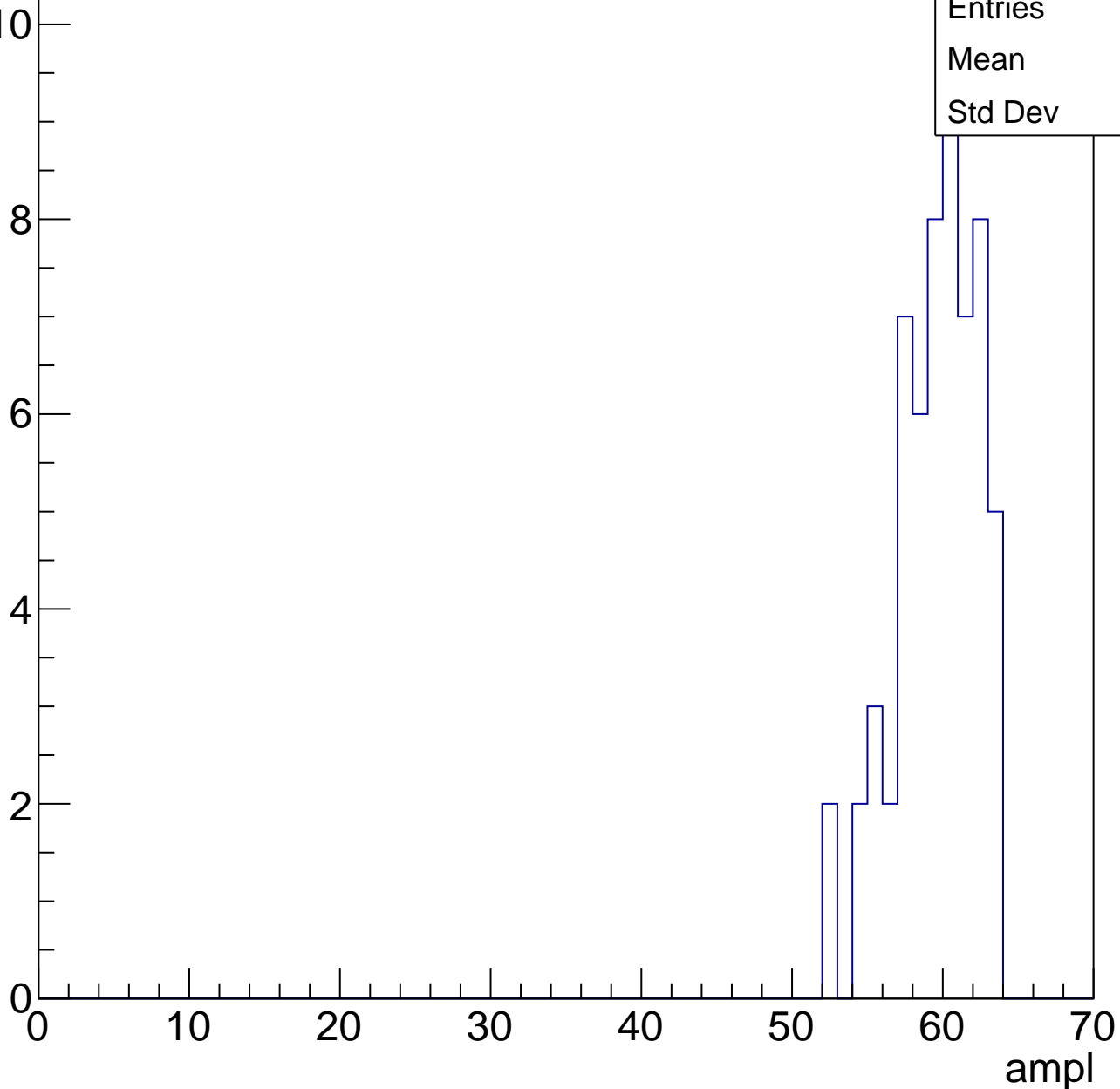


# B1L101S, U9-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	59.1
Std Dev	2.7

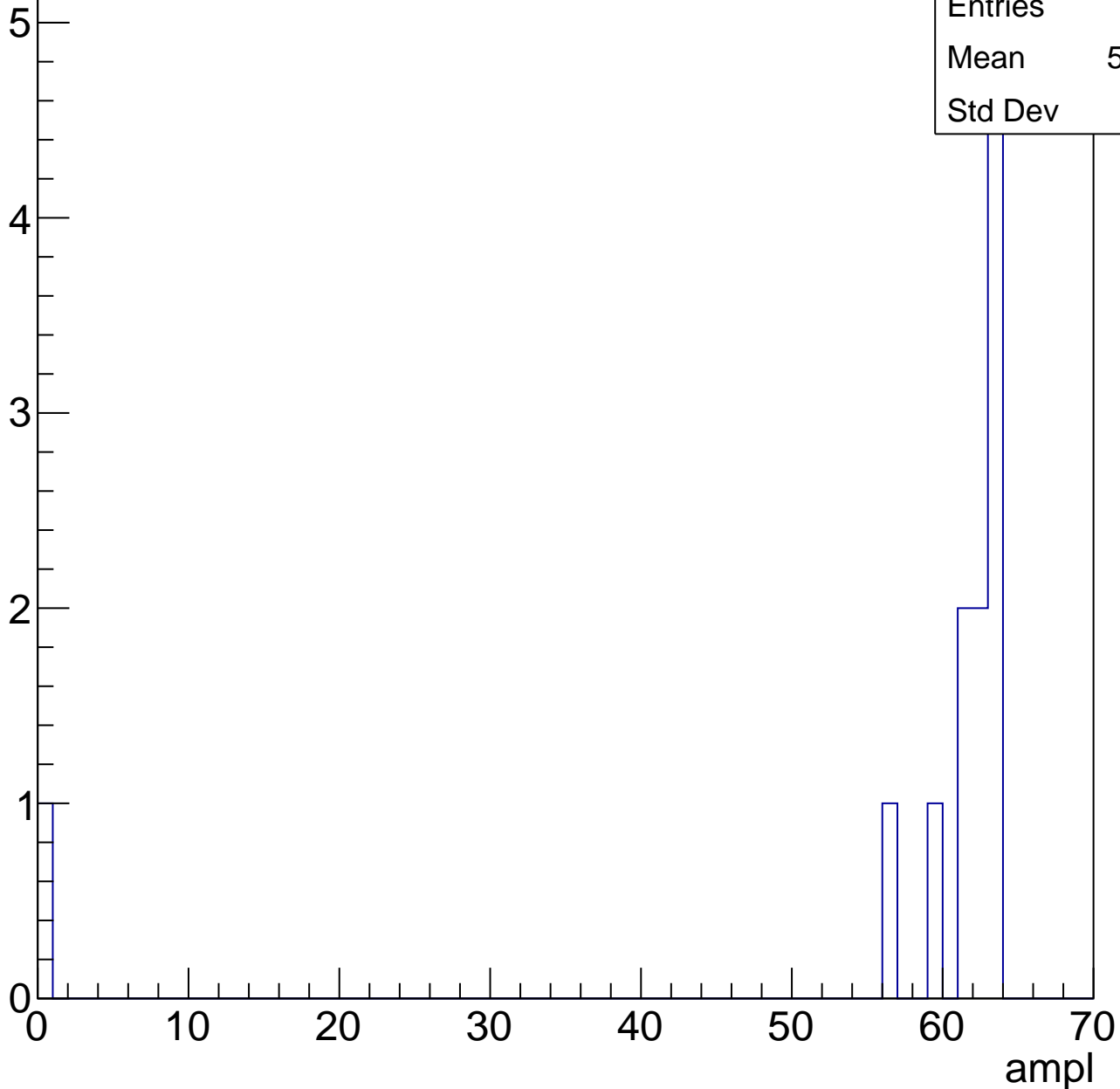


# B1L101S, U9-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	12
Mean	56.33
Std Dev	17.1





# B1L101S, U9-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U9-ch77, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	84
Mean	28.63
Std Dev	5.654

**Gaus mean : 31.2126**

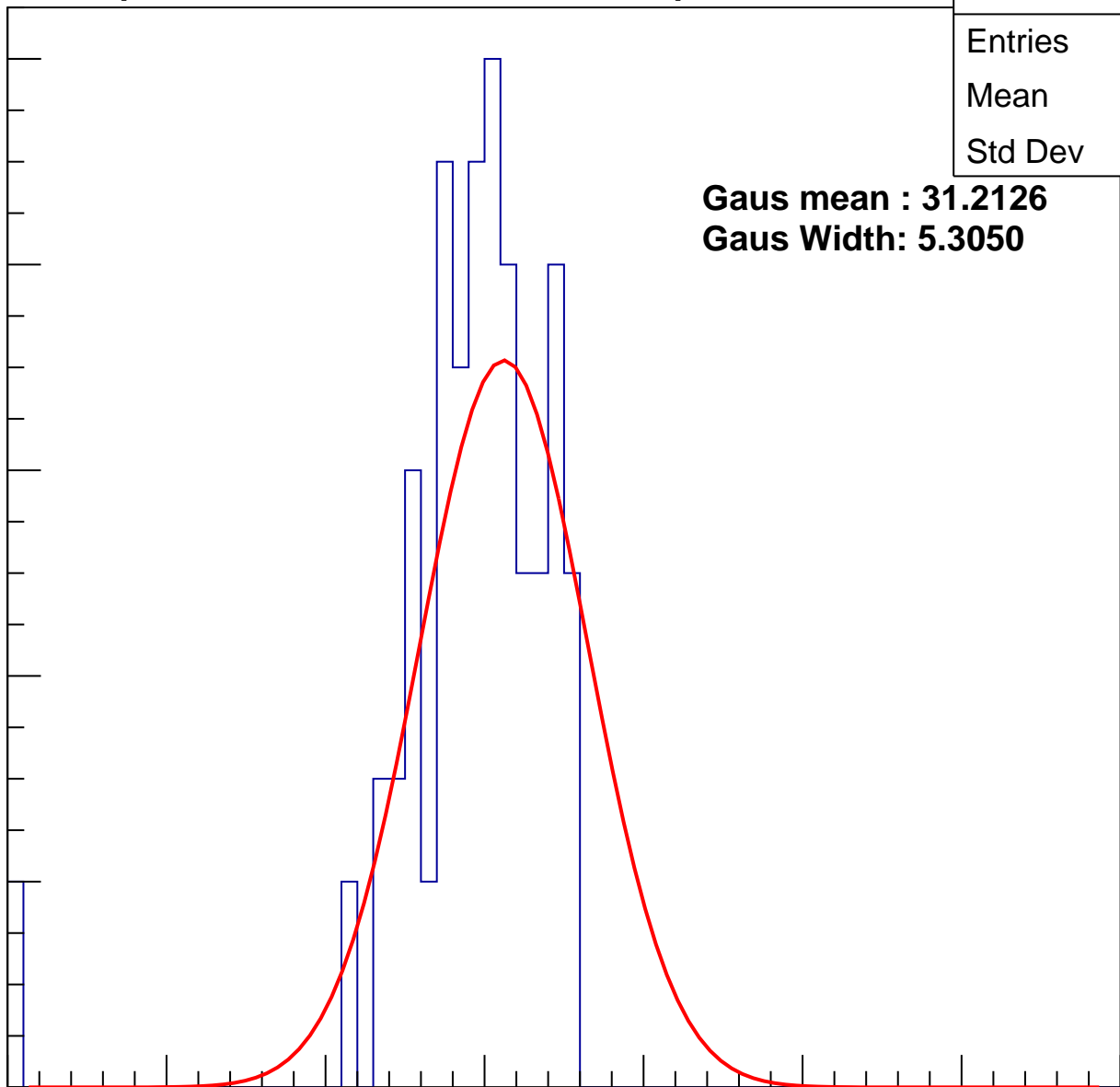
**Gaus Width: 5.3050**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U9-ch77, adc1

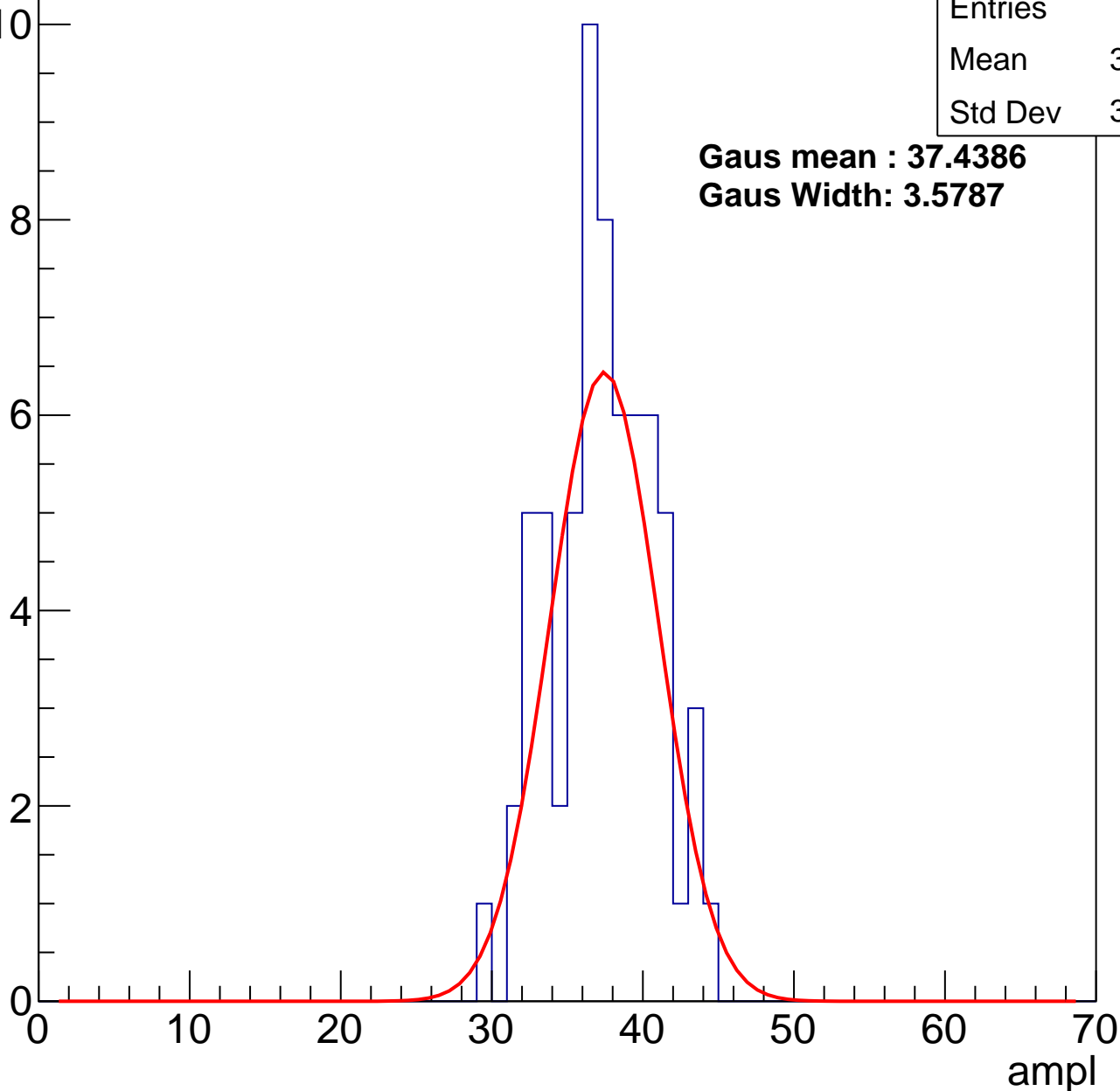
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	36.92
Std Dev	3.336

**Gaus mean : 37.4386**

**Gaus Width: 3.5787**



# B1L101S, U9-ch77, adc2

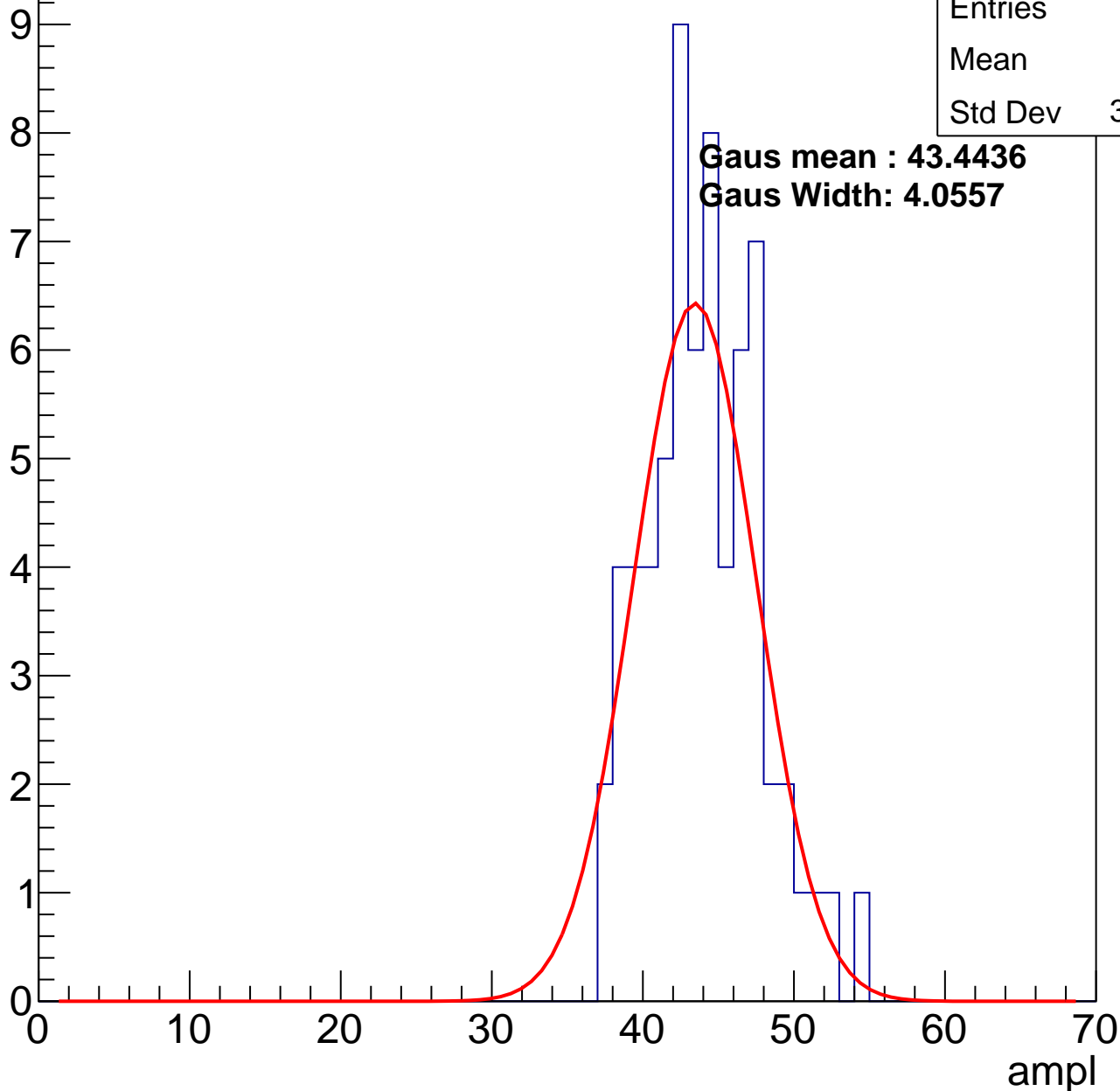
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	43.6
Std Dev	3.673

**Gaus mean : 43.4436**

**Gaus Width: 4.0557**

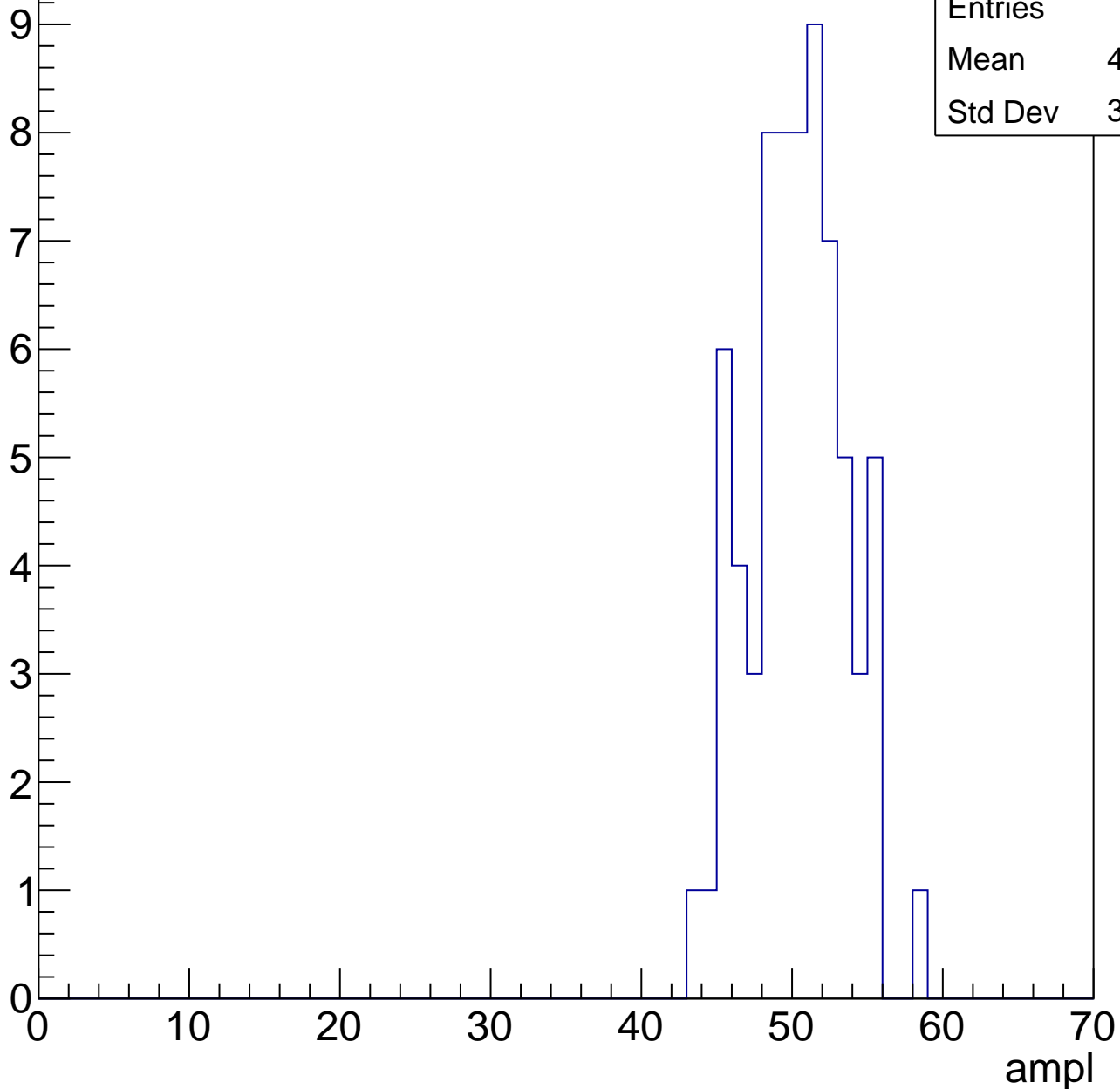


# B1L101S, U9-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	49.87
Std Dev	3.148

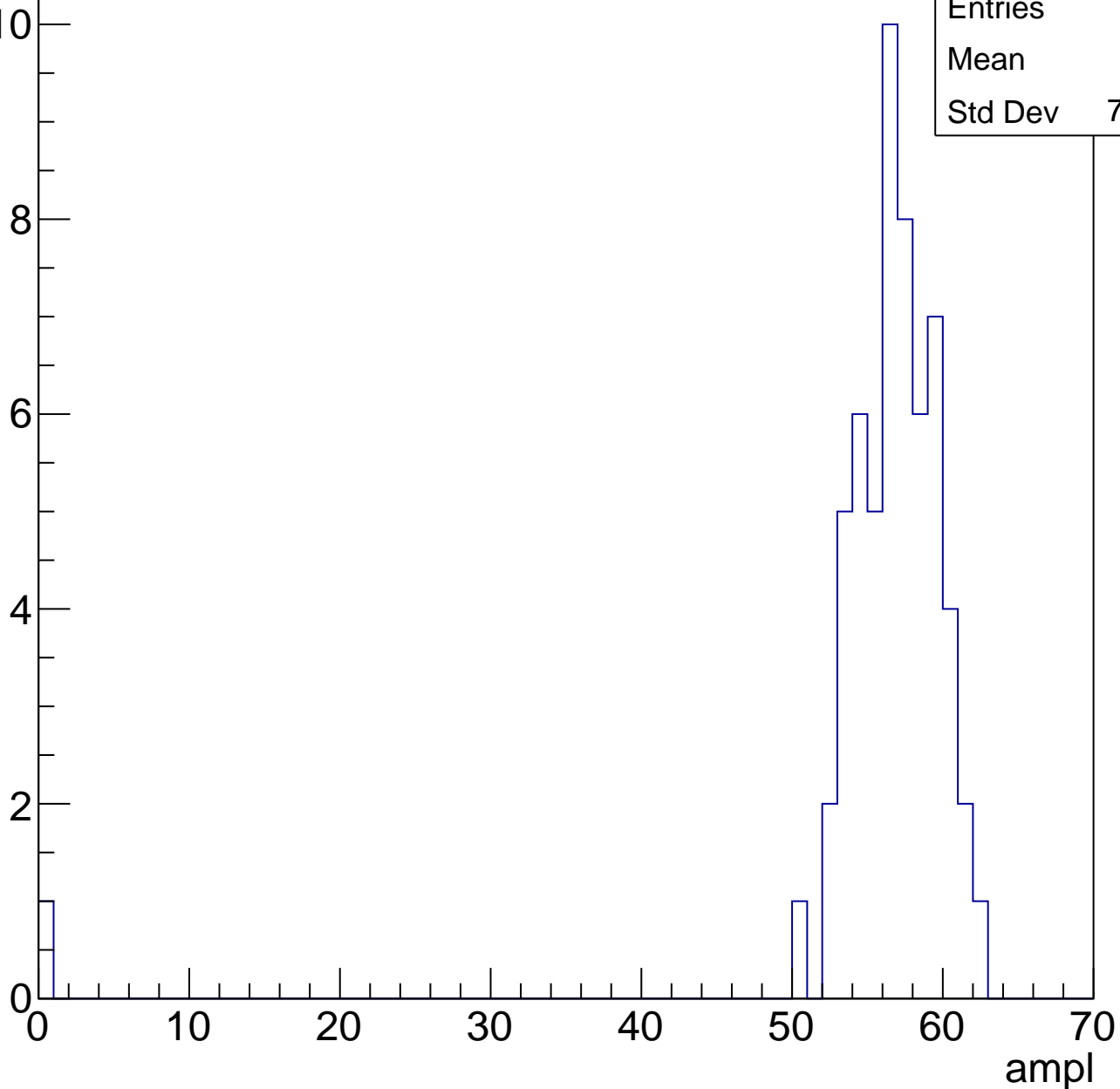


# B1L101S, U9-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	55.5
Std Dev	7.778



# B1L101S, U9-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

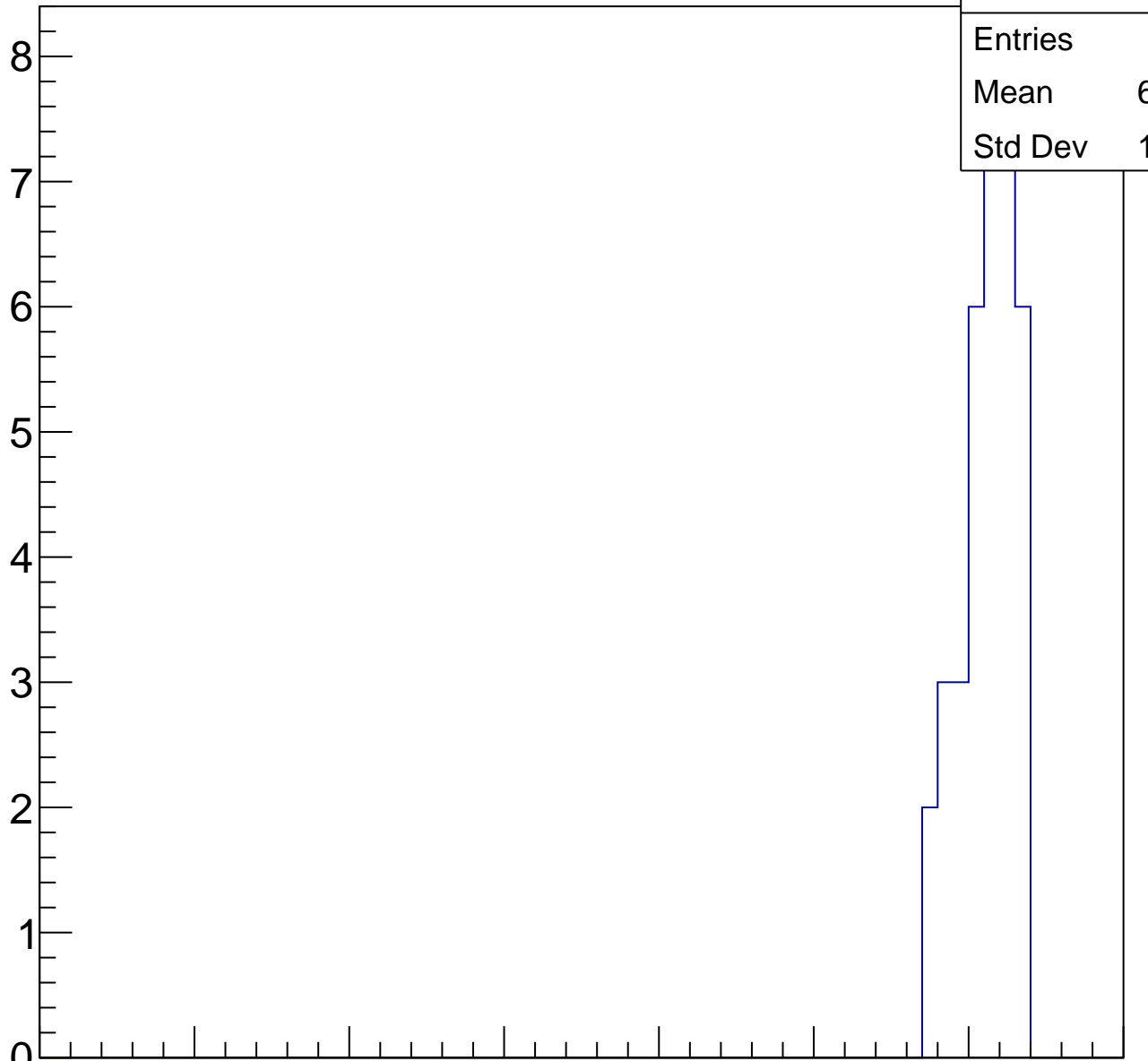
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	36
Mean	60.75
Std Dev	1.722

ampl

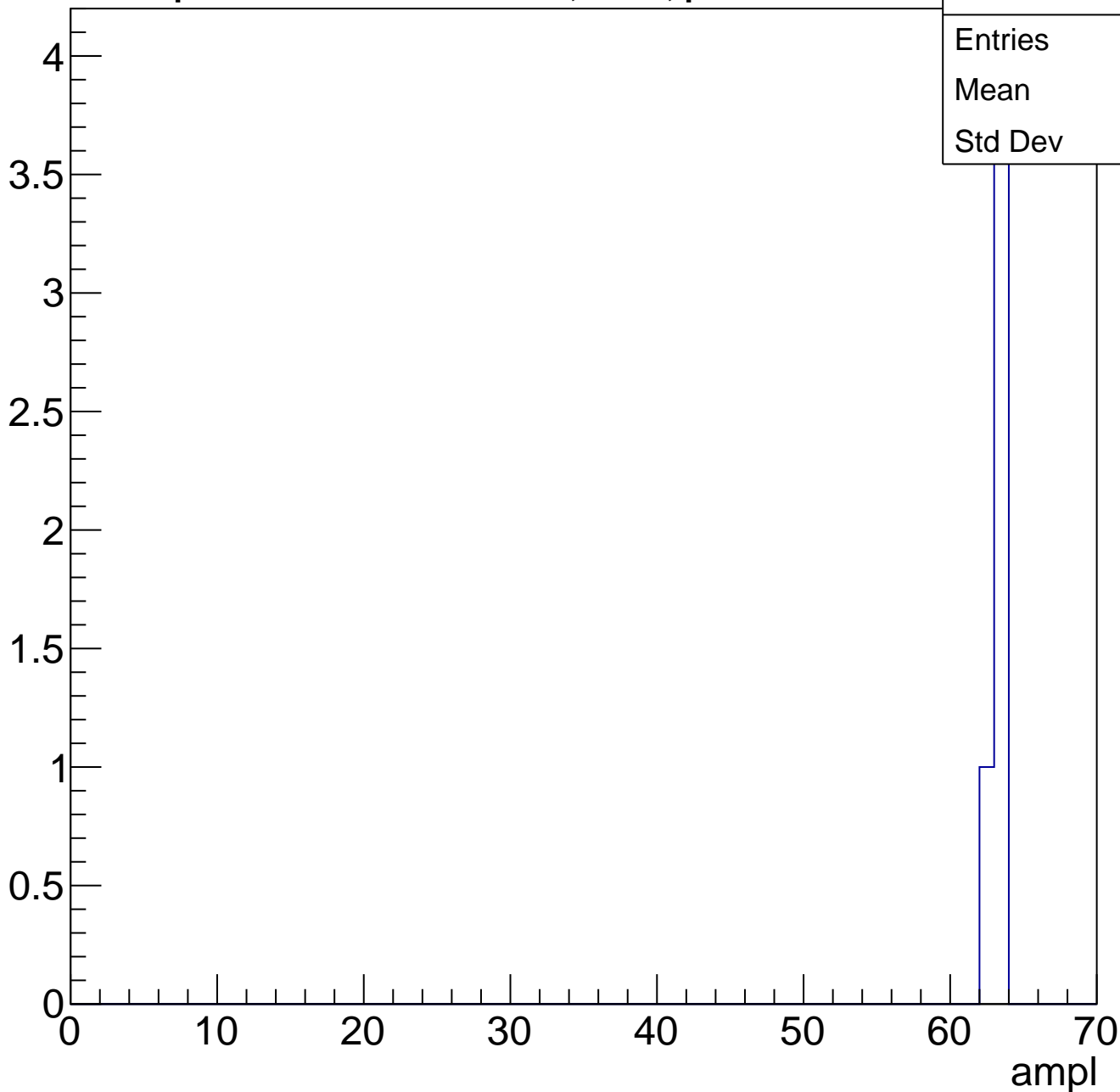
0 10 20 30 40 50 60 70



# B1L101S, U9-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch78, adc0

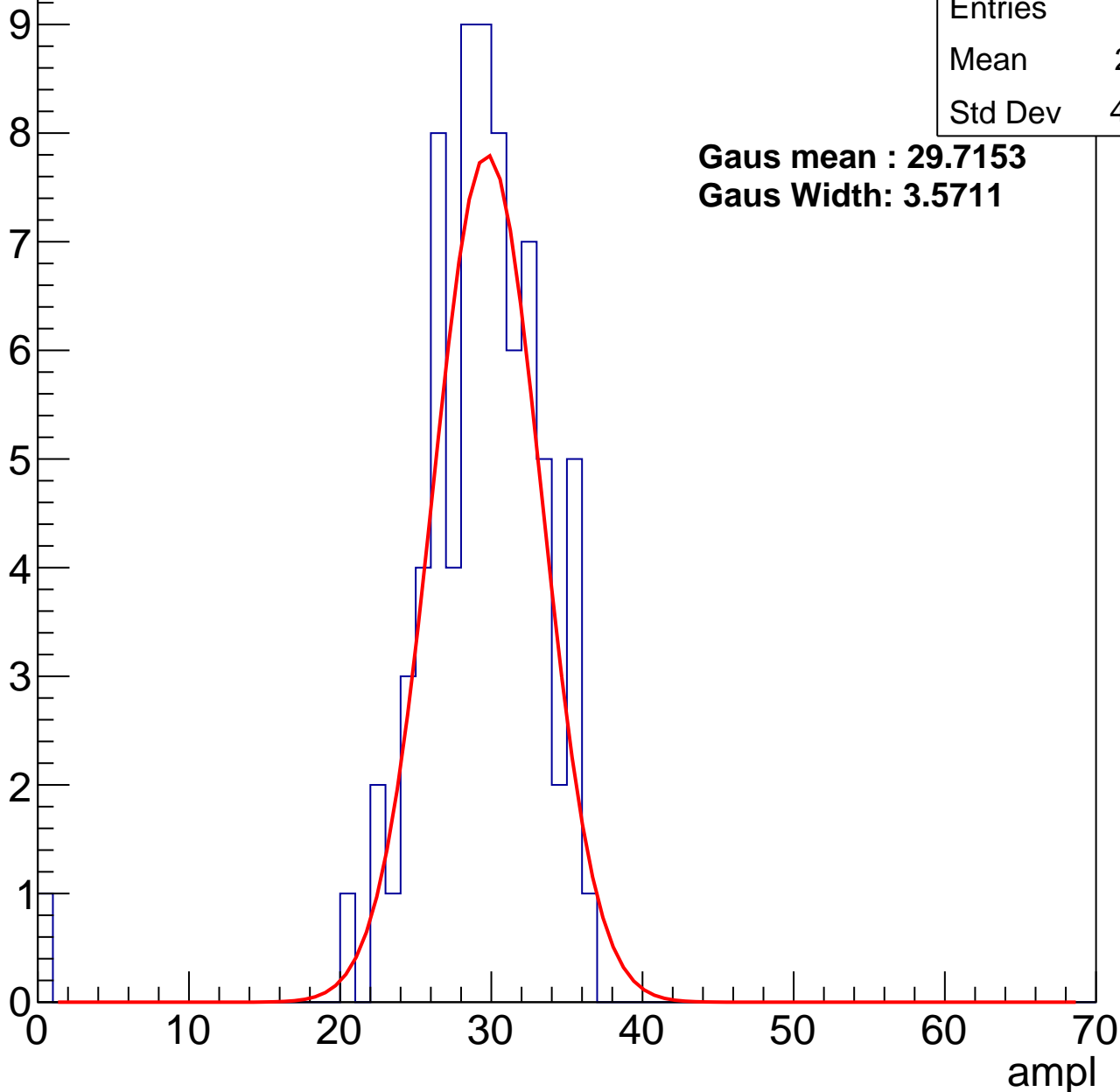
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	28.71
Std Dev	4.784

**Gaus mean : 29.7153**

**Gaus Width: 3.5711**



# B1L101S, U9-ch78, adc1

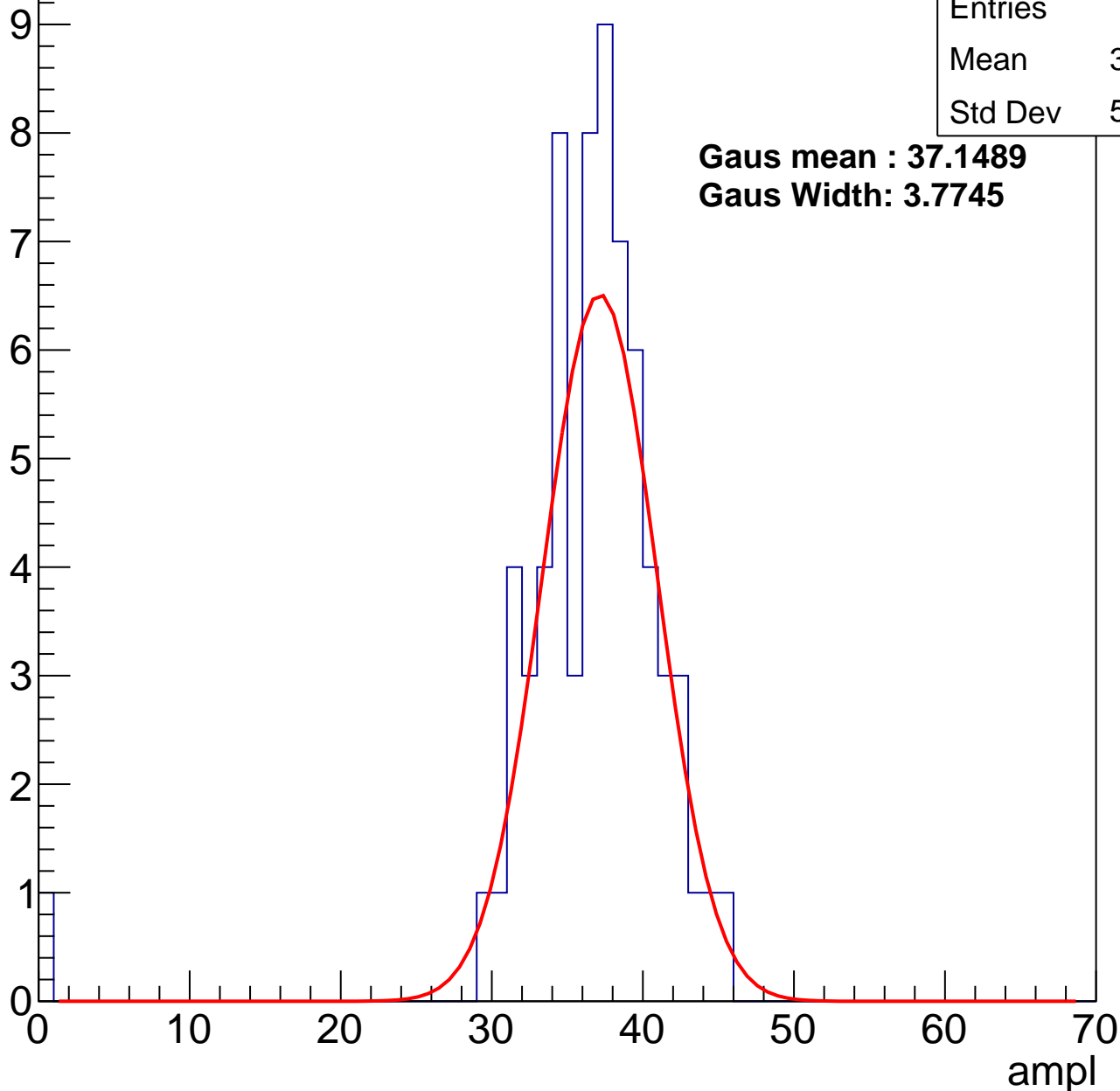
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	36.03
Std Dev	5.599

**Gaus mean : 37.1489**

**Gaus Width: 3.7745**



# B1L101S, U9-ch78, adc2

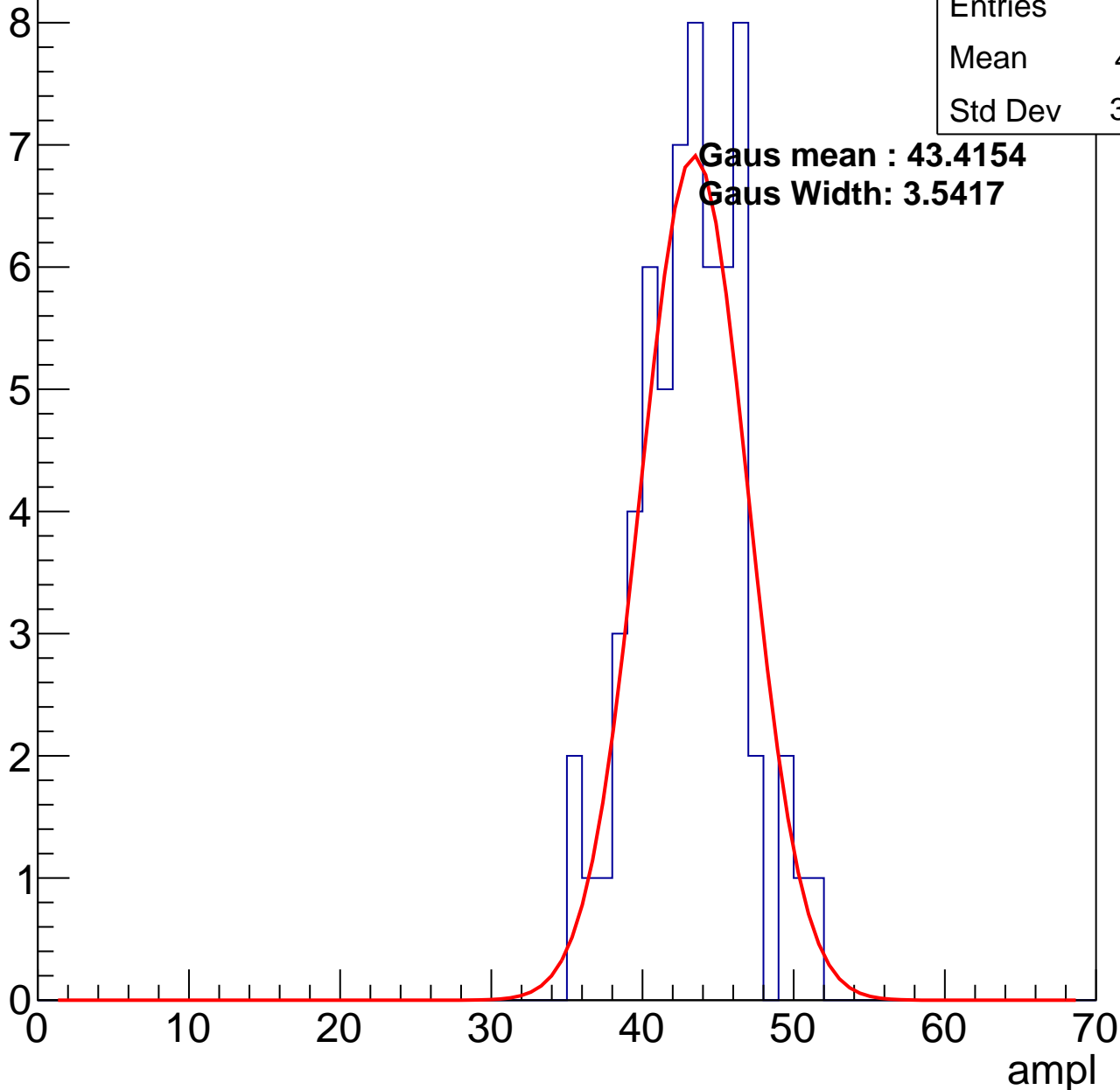
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	42.71
Std Dev	3.443

**Gaus mean : 43.4154**

**Gaus Width: 3.5417**

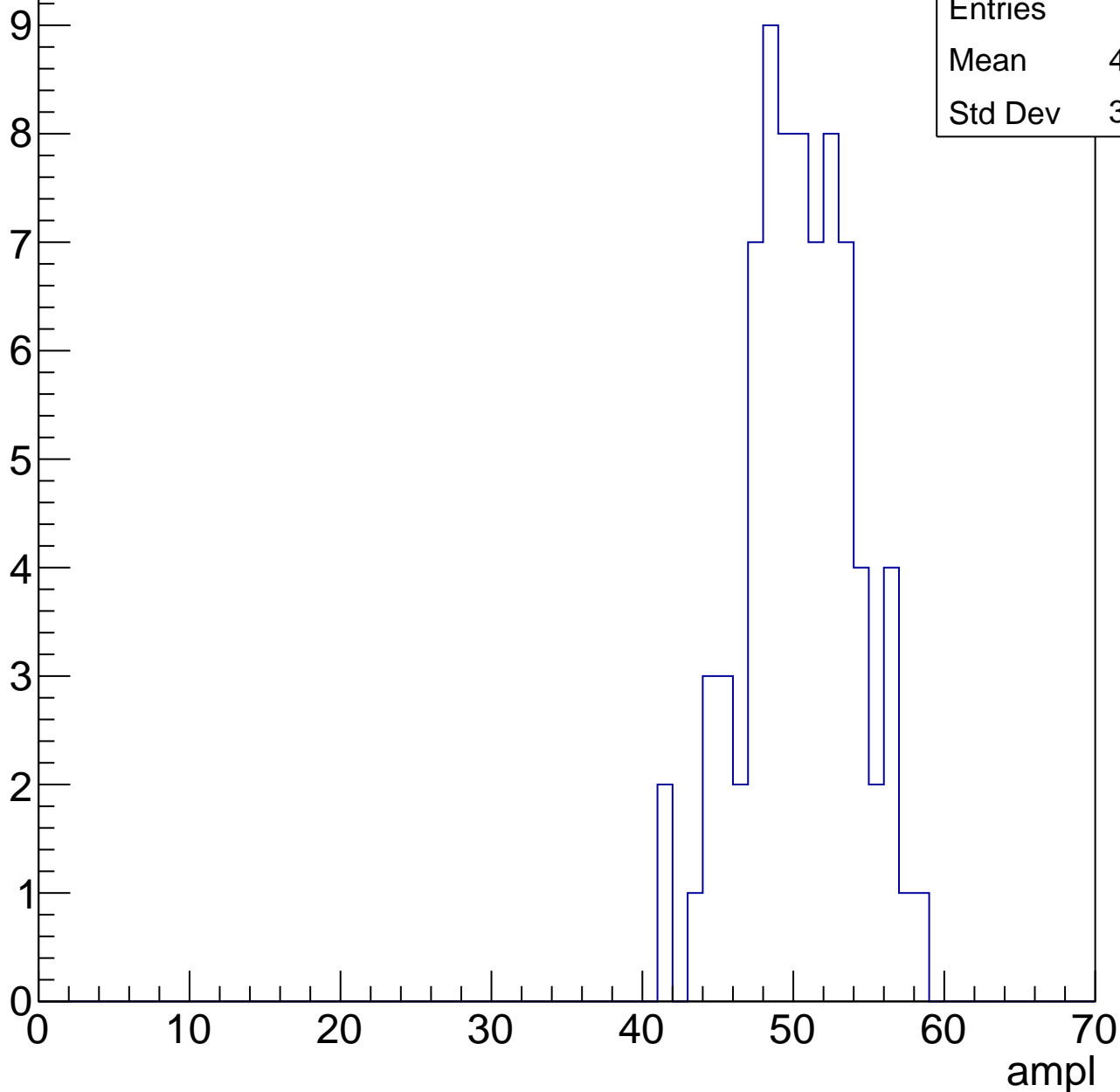


# B1L101S, U9-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	49.95
Std Dev	3.614

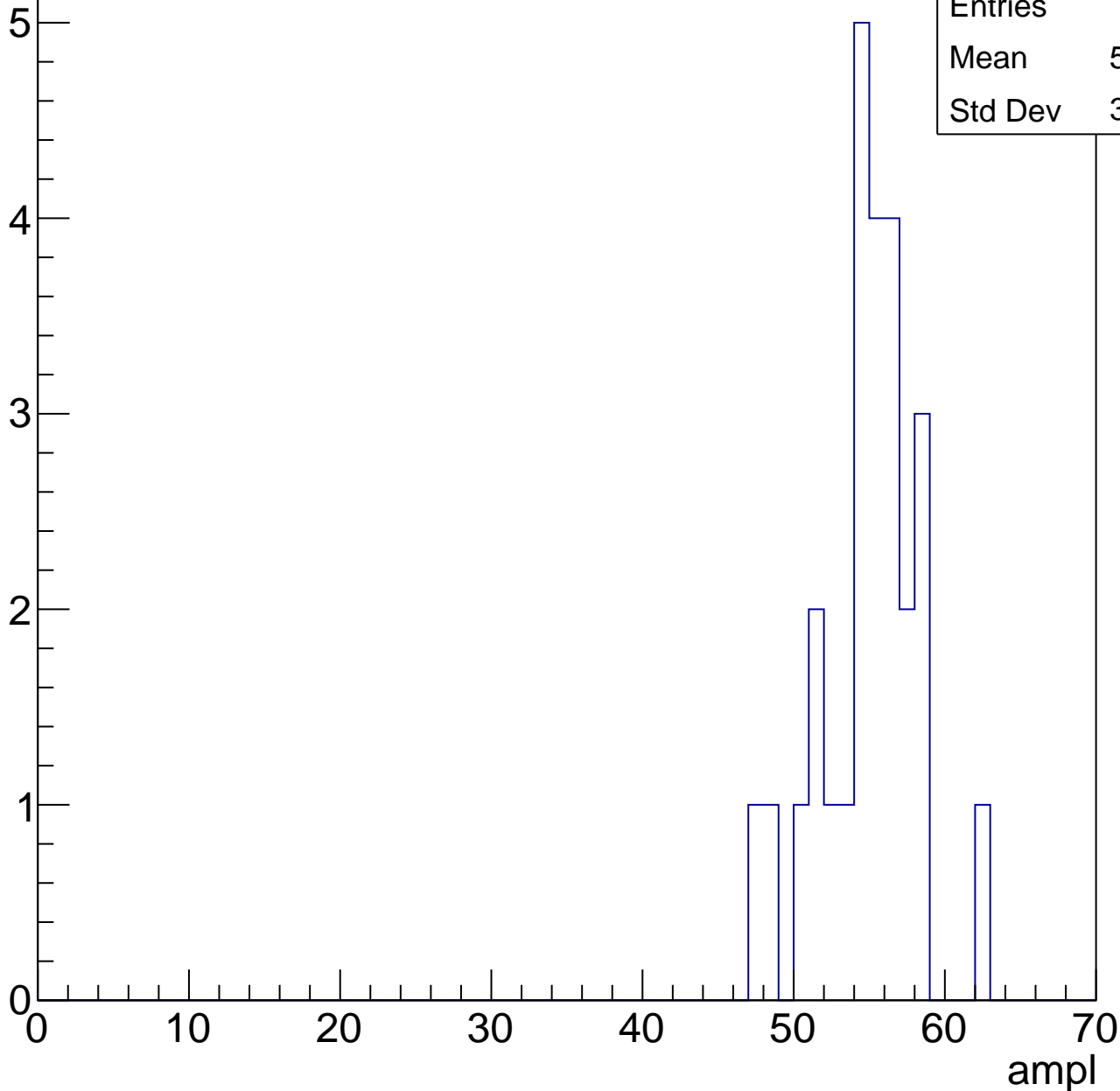


# B1L101S, U9-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

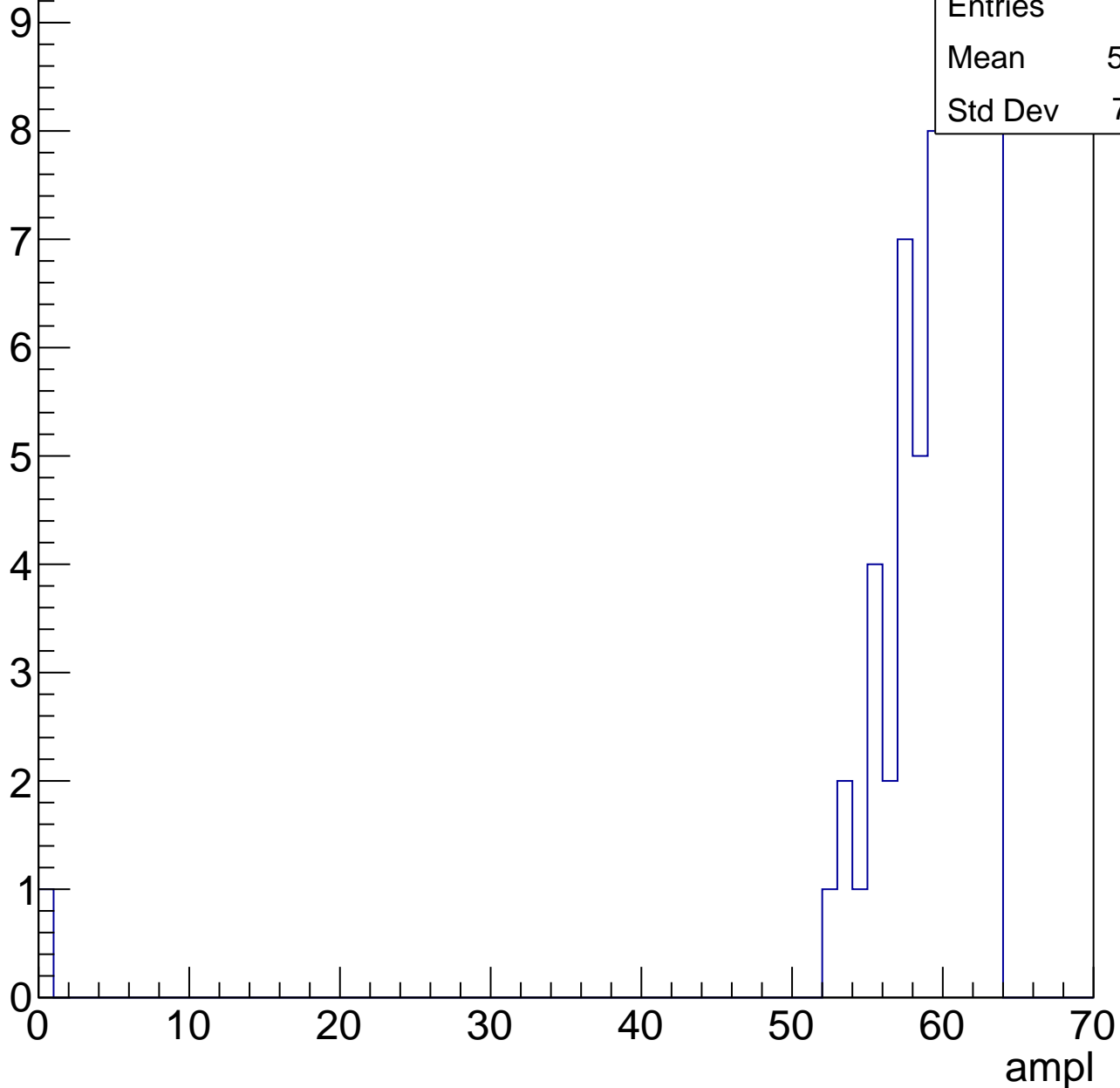
Entries	26
Mean	54.46
Std Dev	3.213



# B1L101S, U9-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

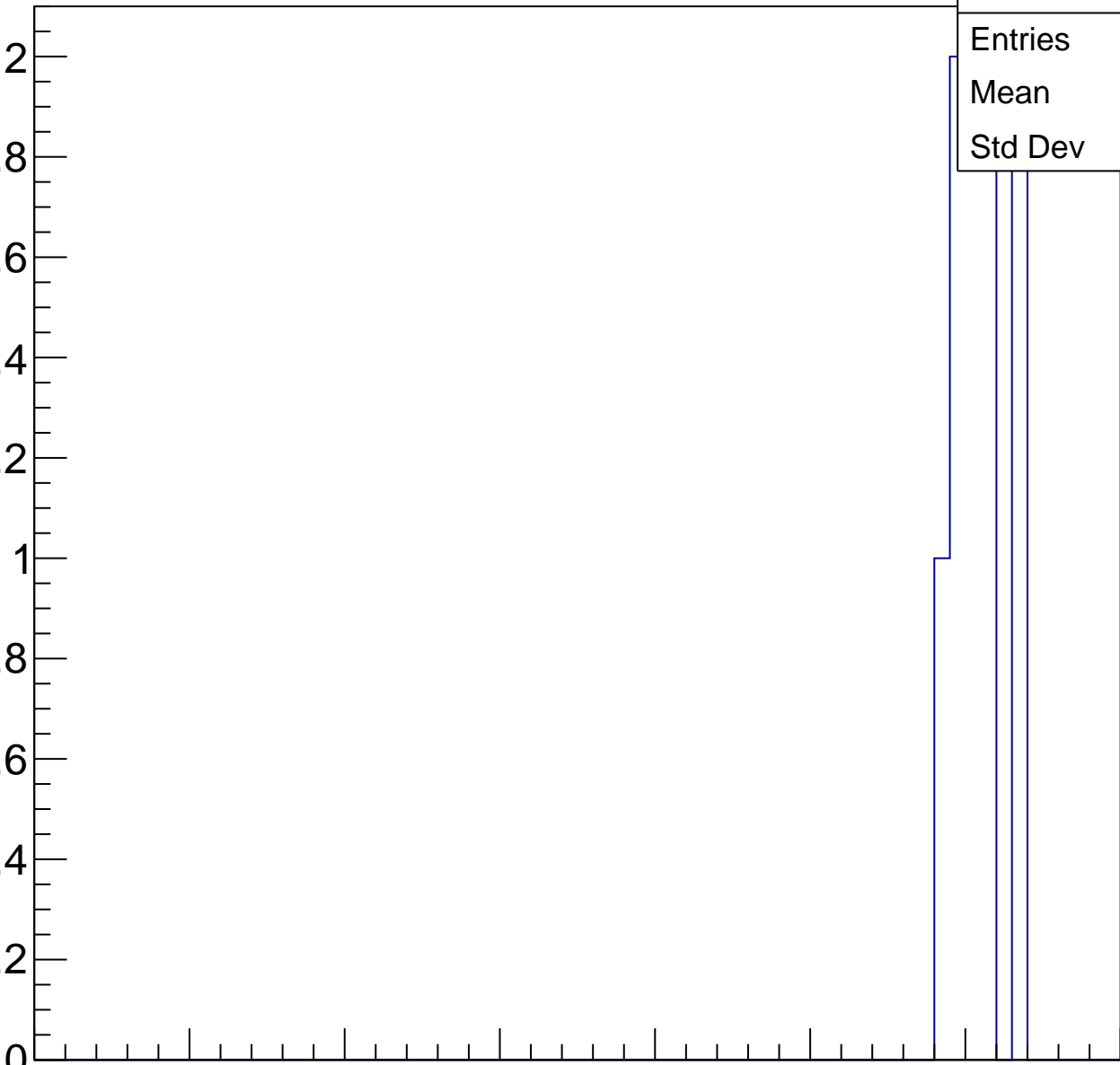
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	9
Mean	60.44
Std Dev	1.641

0 10 20 30 40 50 60 70

ampl





# B1L101S, U9-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U9-ch79, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	77
Mean	29.7
Std Dev	3.264

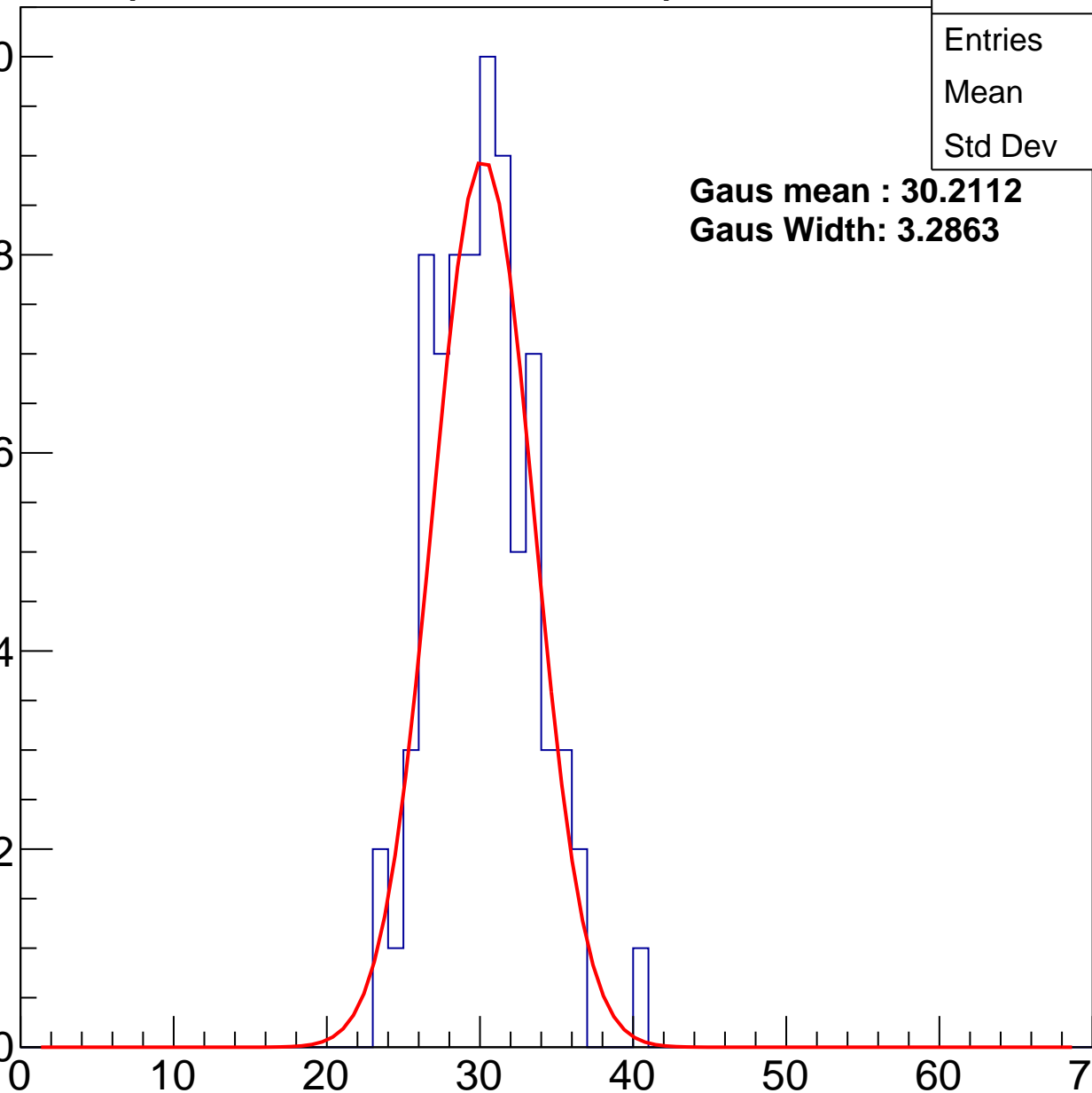
**Gaus mean : 30.2112**

**Gaus Width: 3.2863**

Entry

10  
8  
6  
4  
2  
0

ampl



# B1L101S, U9-ch79, adc1

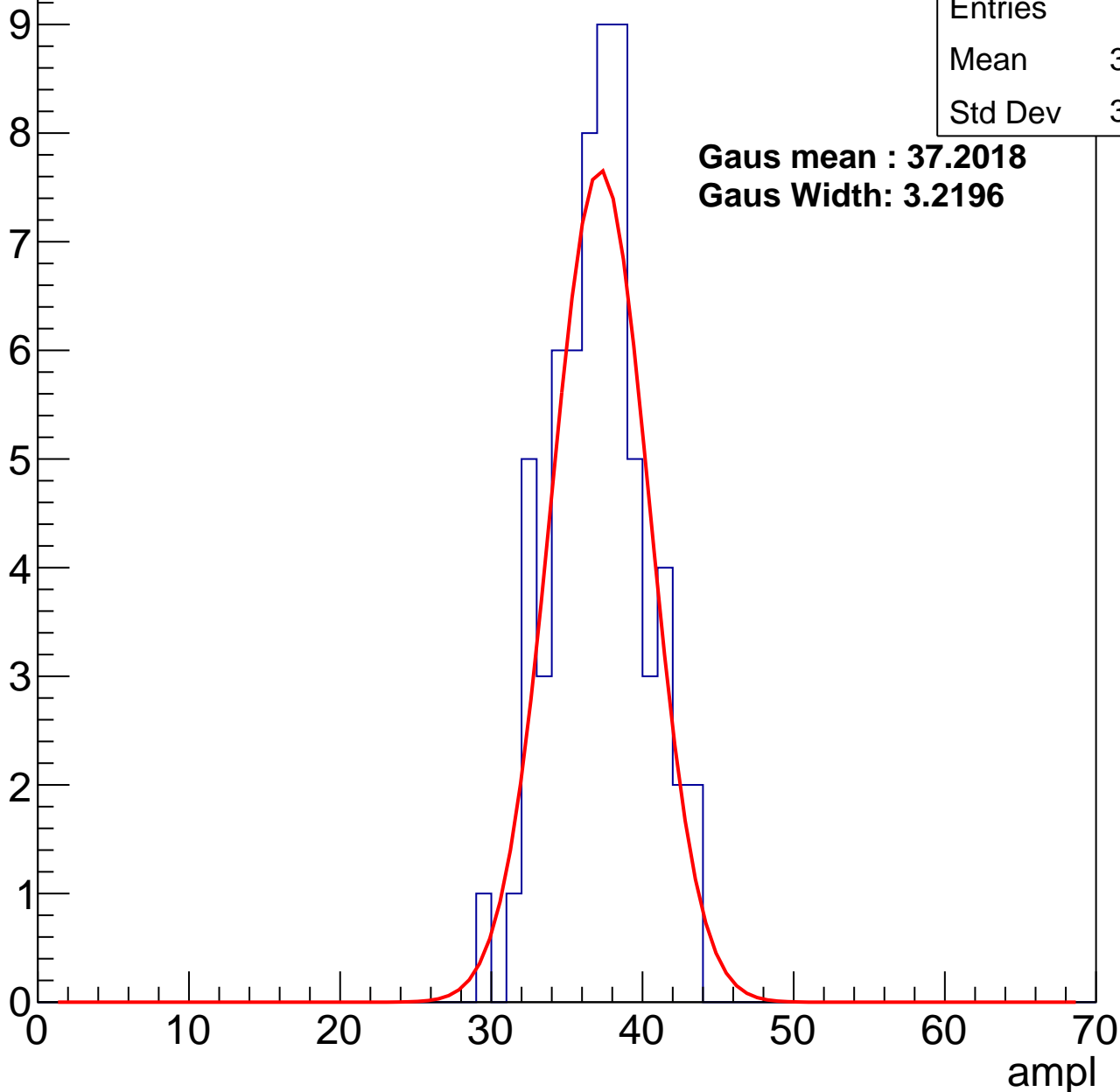
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	36.64
Std Dev	3.043

**Gaus mean : 37.2018**

**Gaus Width: 3.2196**



# B1L101S, U9-ch79, adc2

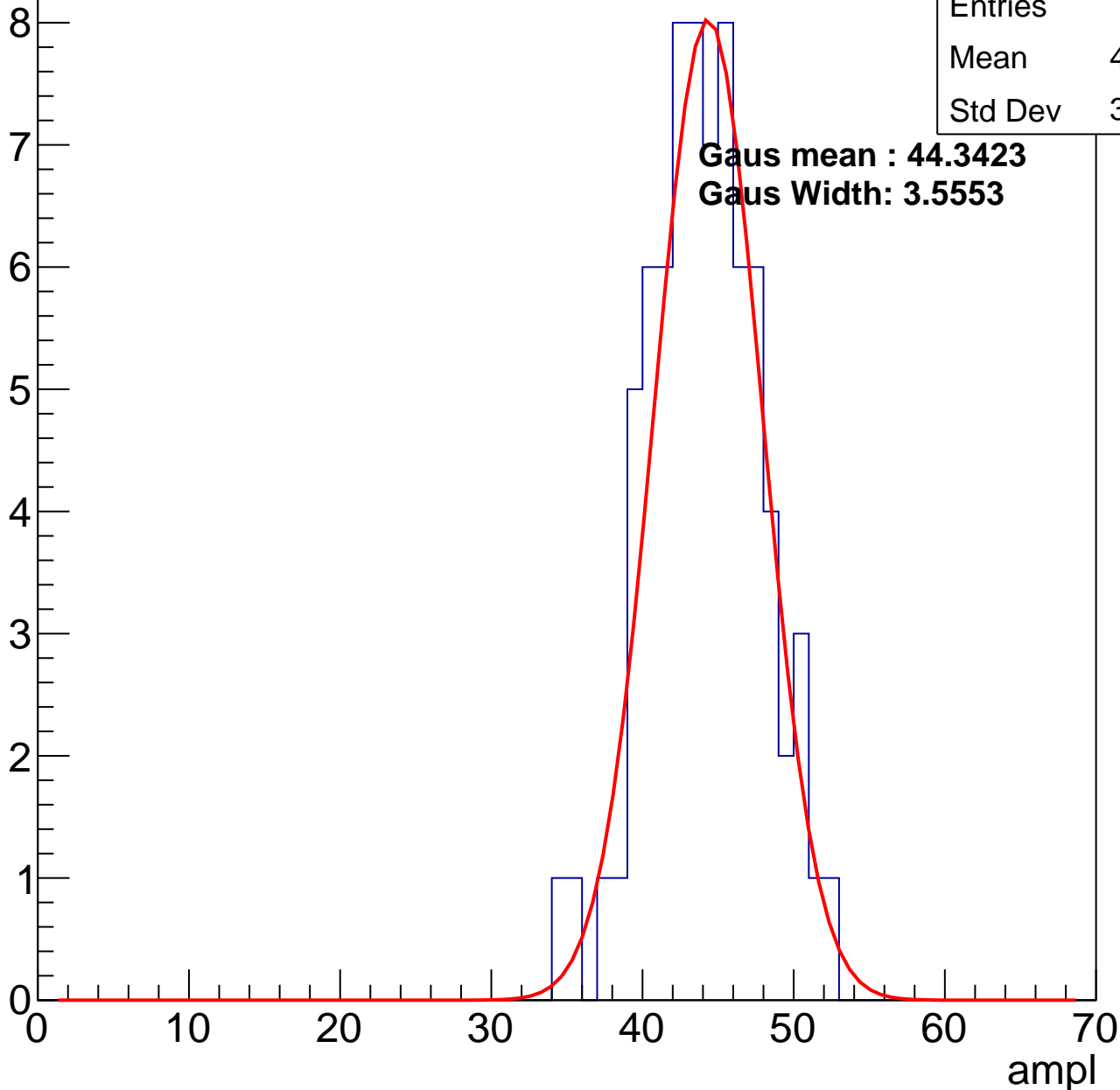
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	43.65
Std Dev	3.639

**Gaus mean : 44.3423**

**Gaus Width: 3.5553**

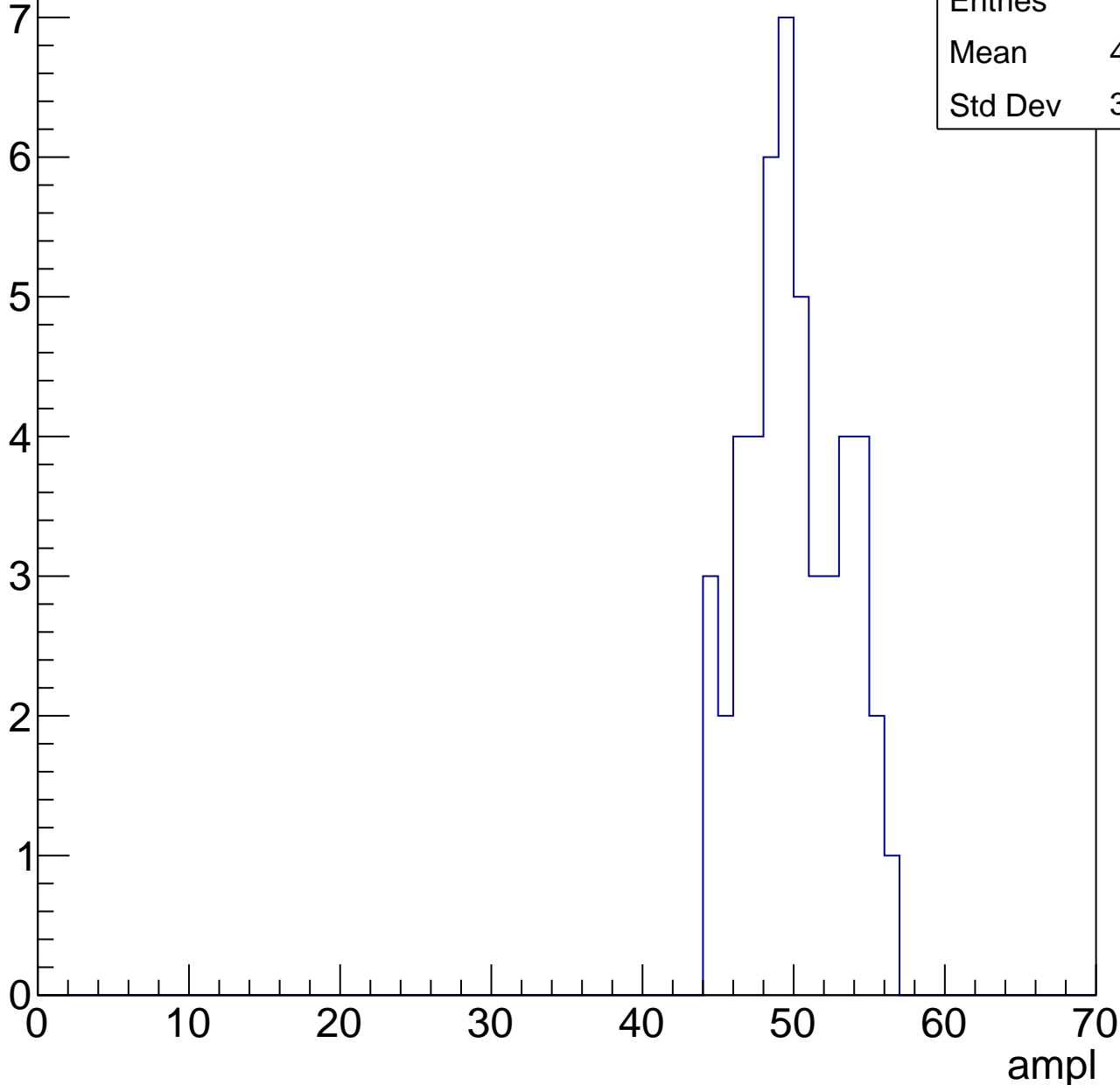


# B1L101S, U9-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

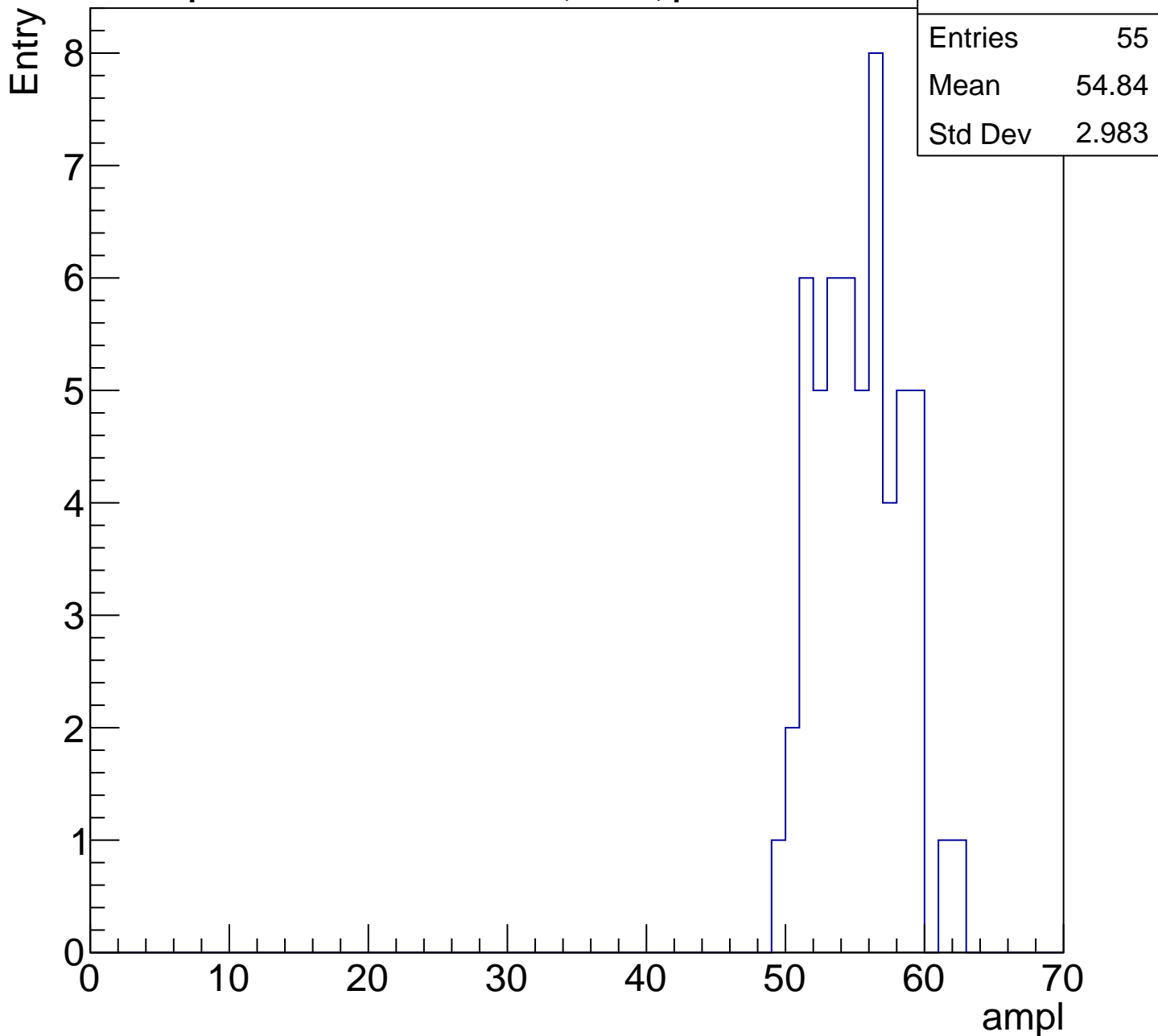
Entry

Entries	48
Mean	49.54
Std Dev	3.162



# B1L101S, U9-ch79, adc4

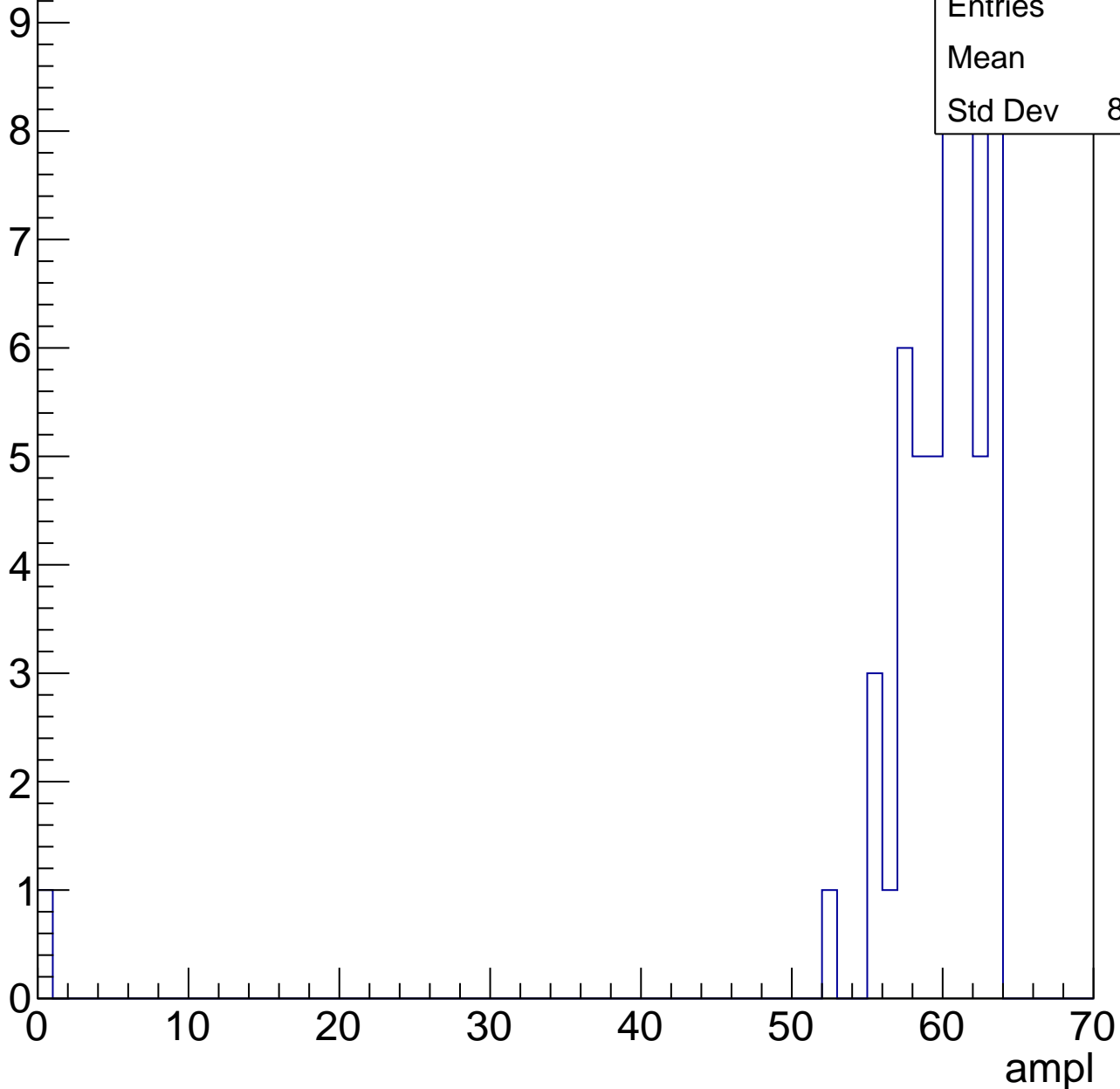
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

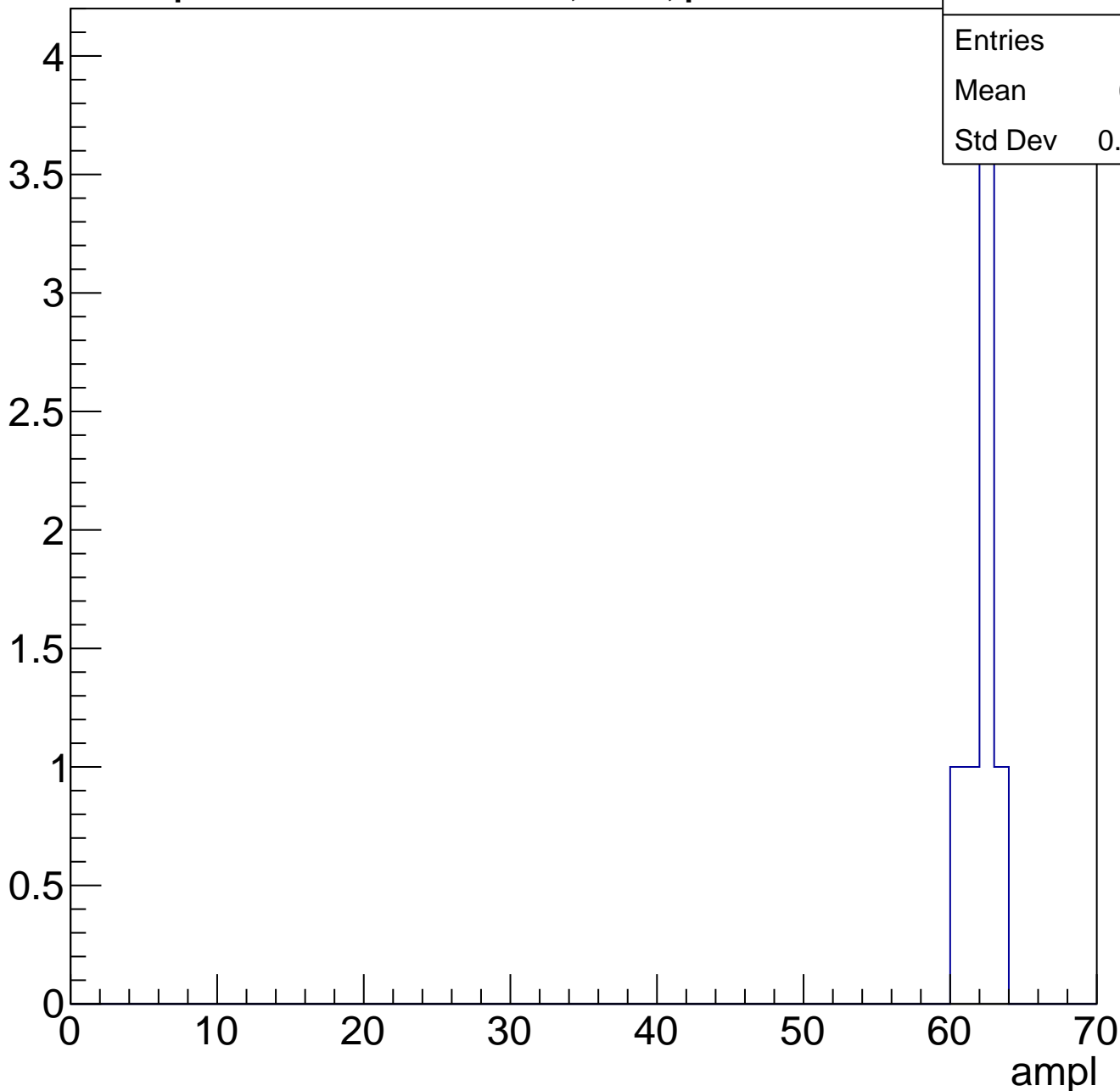


Entries	52
Mean	58.5
Std Dev	8.568

# B1L101S, U9-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	43
Std Dev	20

ampl

# B1L101S, U9-ch80, adc0

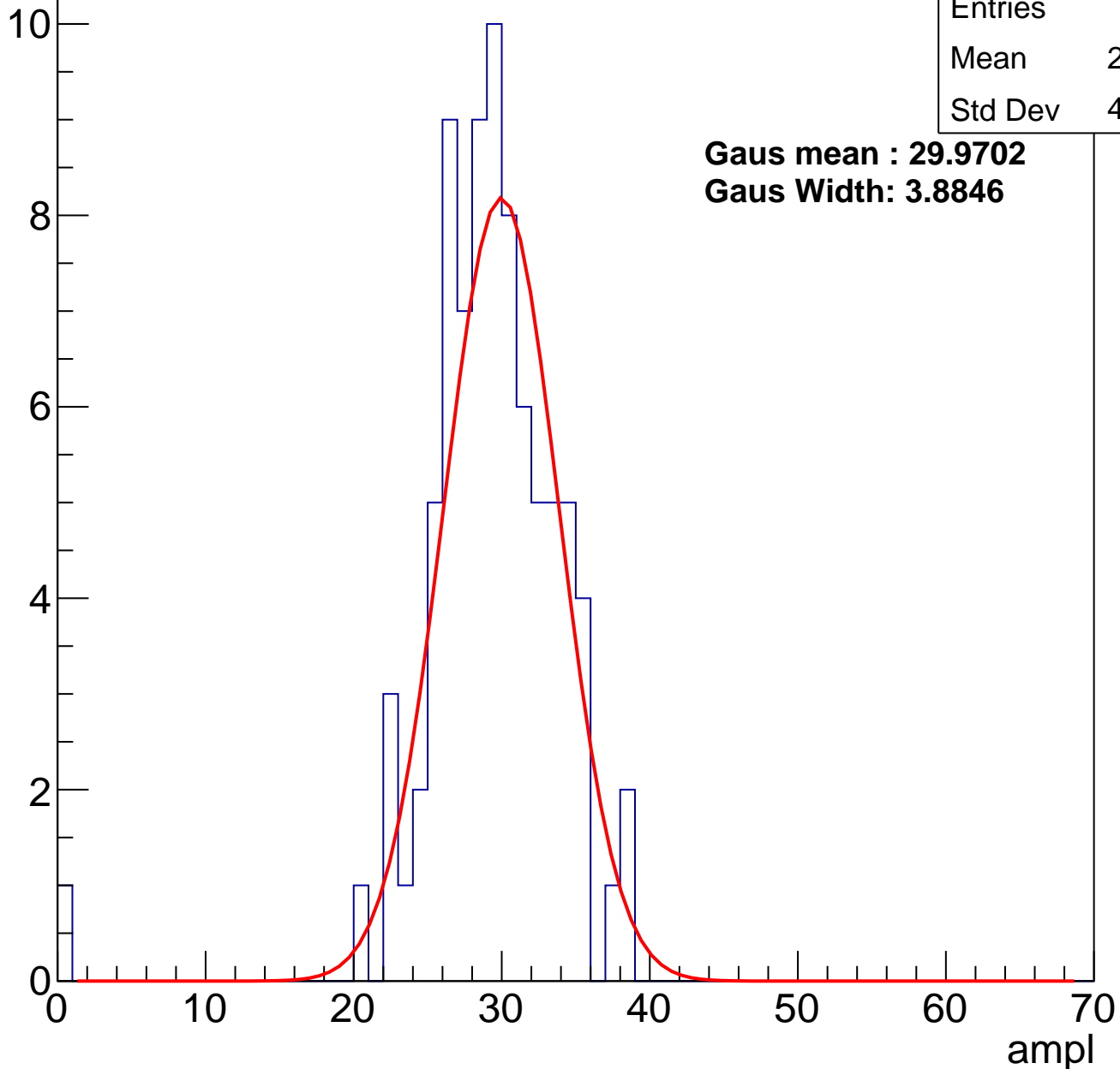
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	84
Mean	28.82
Std Dev	4.882

**Gaus mean : 29.9702**

**Gaus Width: 3.8846**

Entry



# B1L101S, U9-ch80, adc1

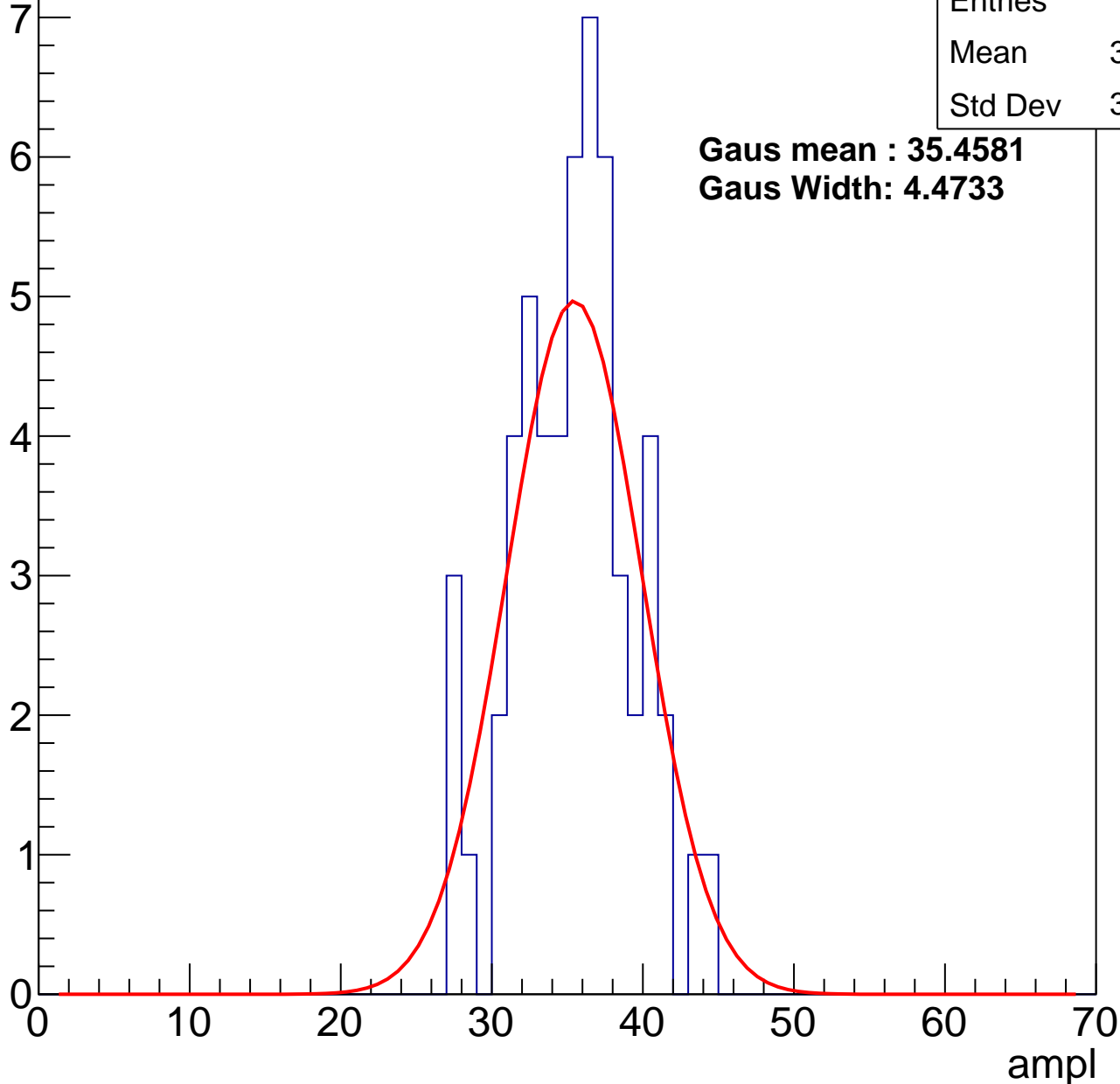
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	35.02
Std Dev	3.878

**Gaus mean : 35.4581**

**Gaus Width: 4.4733**



# B1L101S, U9-ch80, adc2

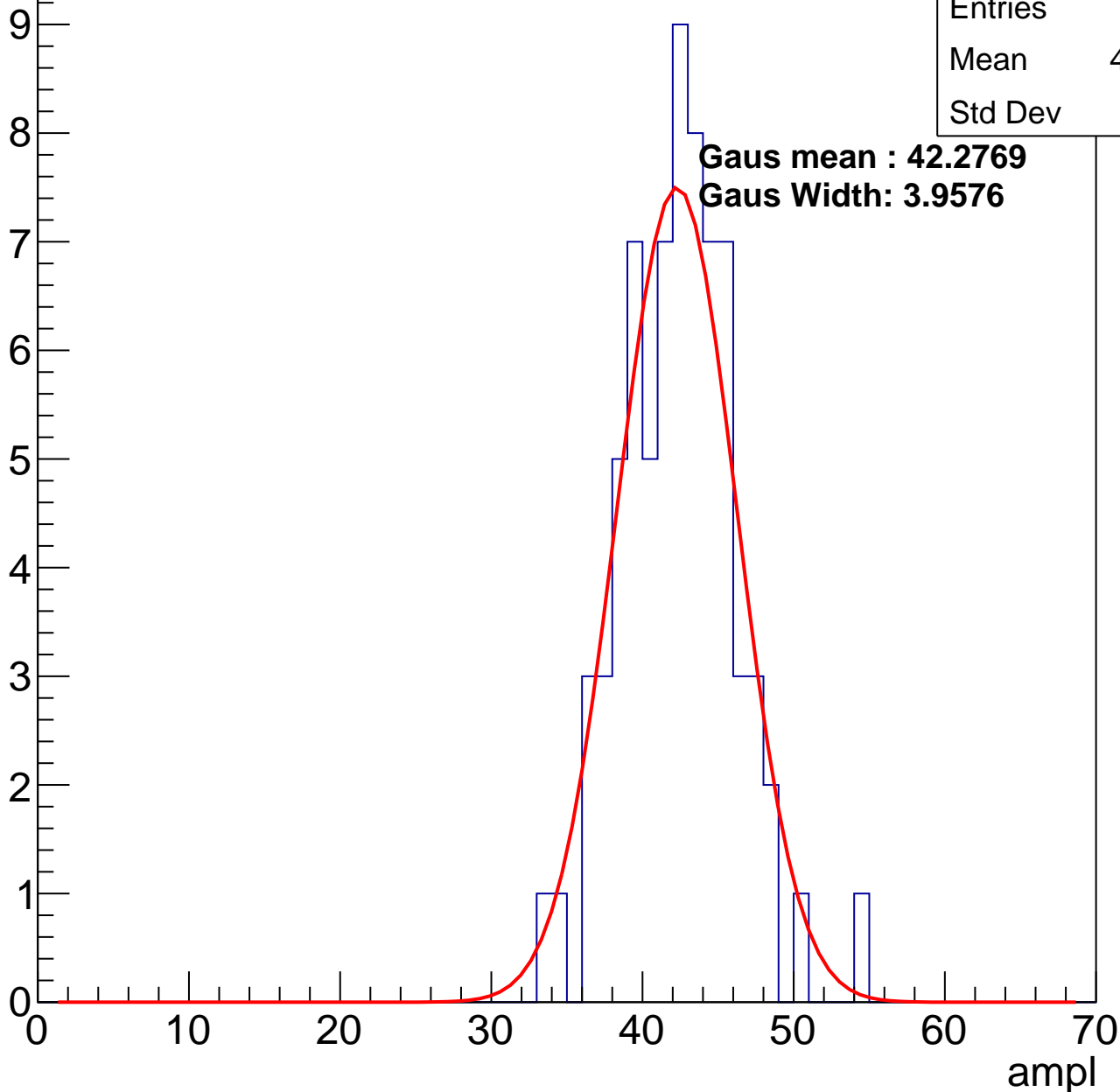
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	41.92
Std Dev	3.7

**Gaus mean : 42.2769**

**Gaus Width: 3.9576**



# B1L101S, U9-ch80, adc3

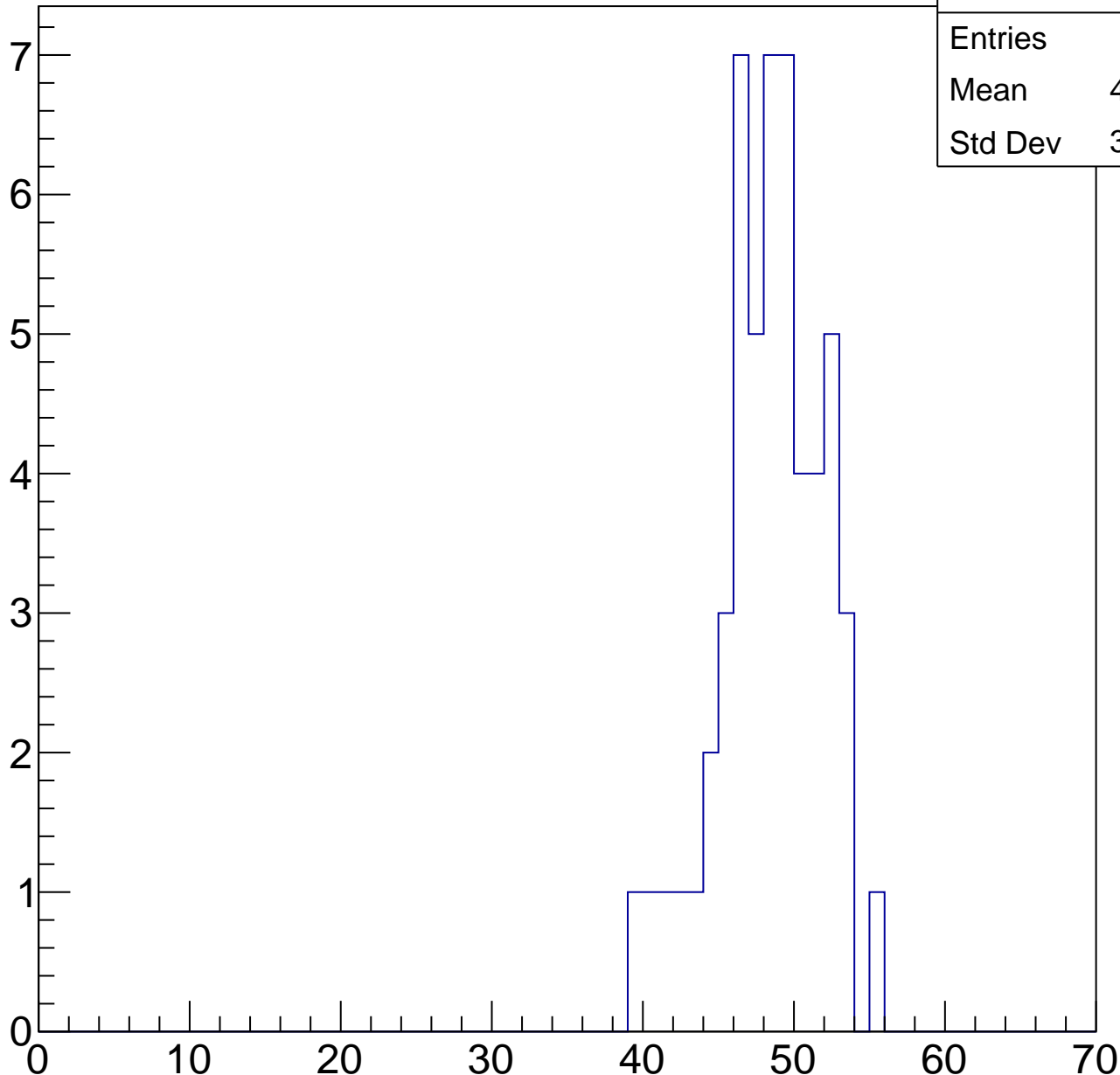
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	53
Mean	47.96
Std Dev	3.392

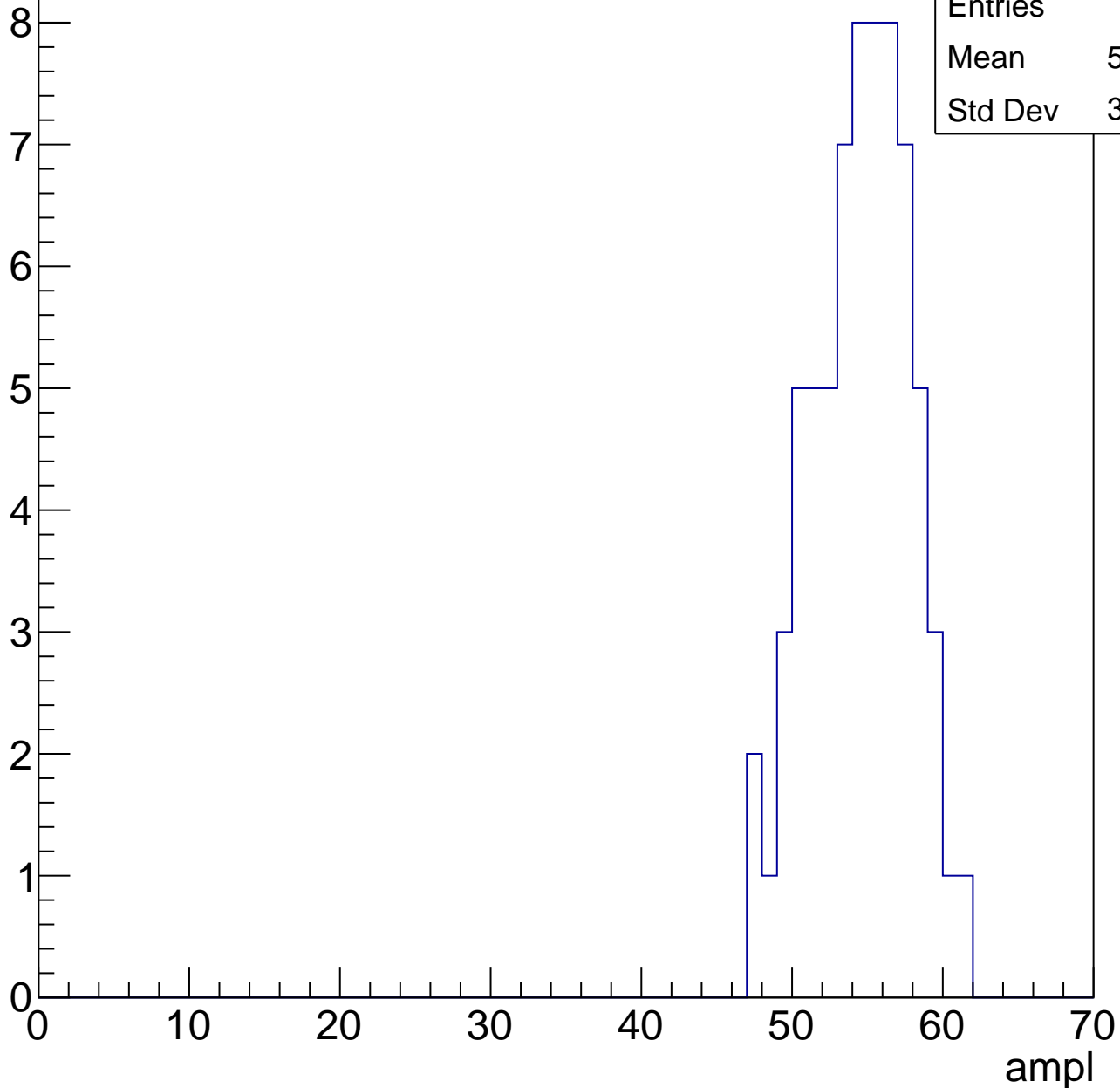
ampl



# B1L101S, U9-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	69
Mean	54.09
Std Dev	3.193

# B1L101S, U9-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

Entries

36

Mean

59.69

Std Dev

2.767

0

10

20

30

40

50

60

70

ampl

0

1

2

3

4

5

6

7

8

9

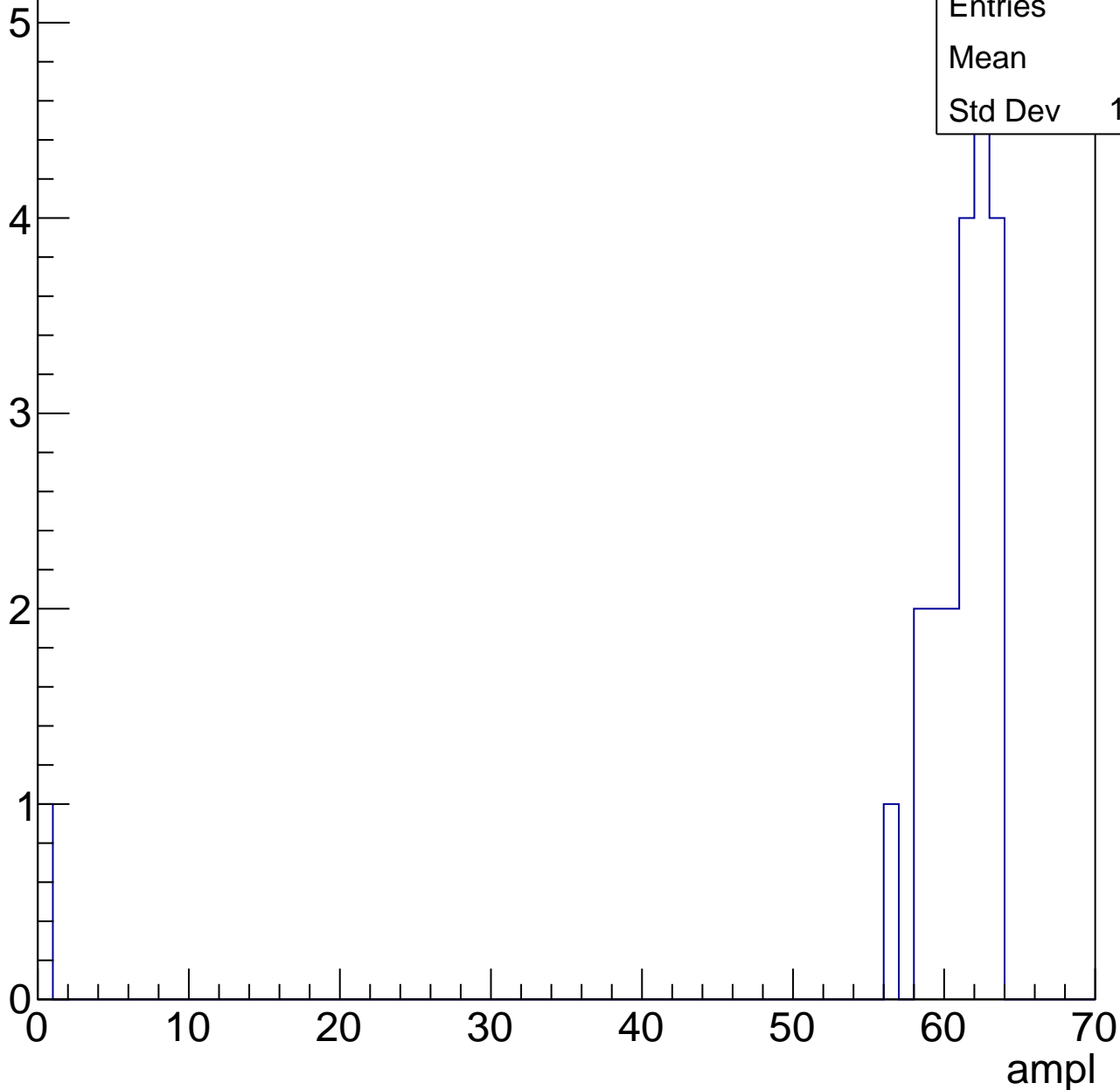
10

# B1L101S, U9-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	21
Mean	57.9
Std Dev	13.08

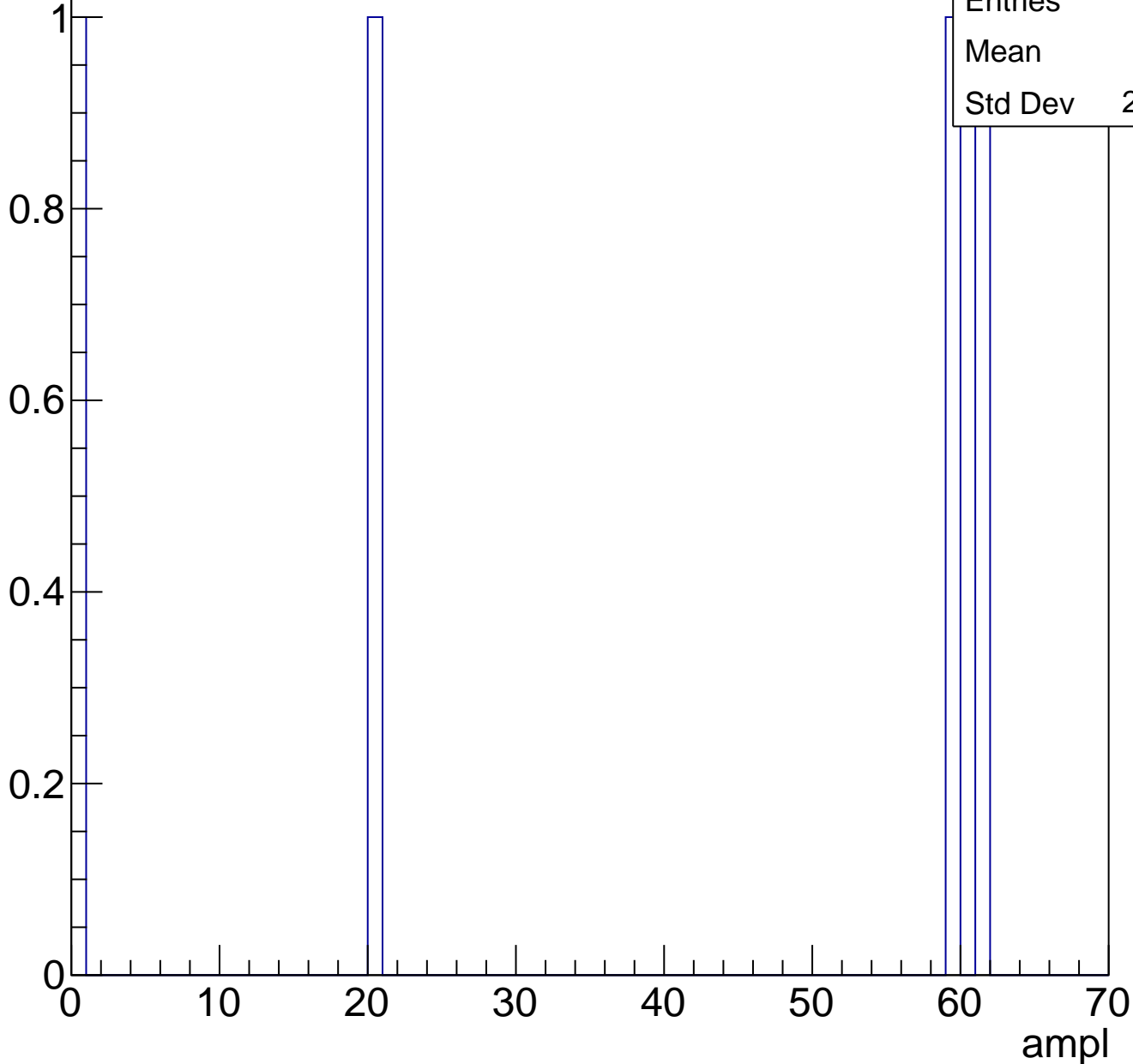




# B1L101S, U9-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch81, adc0

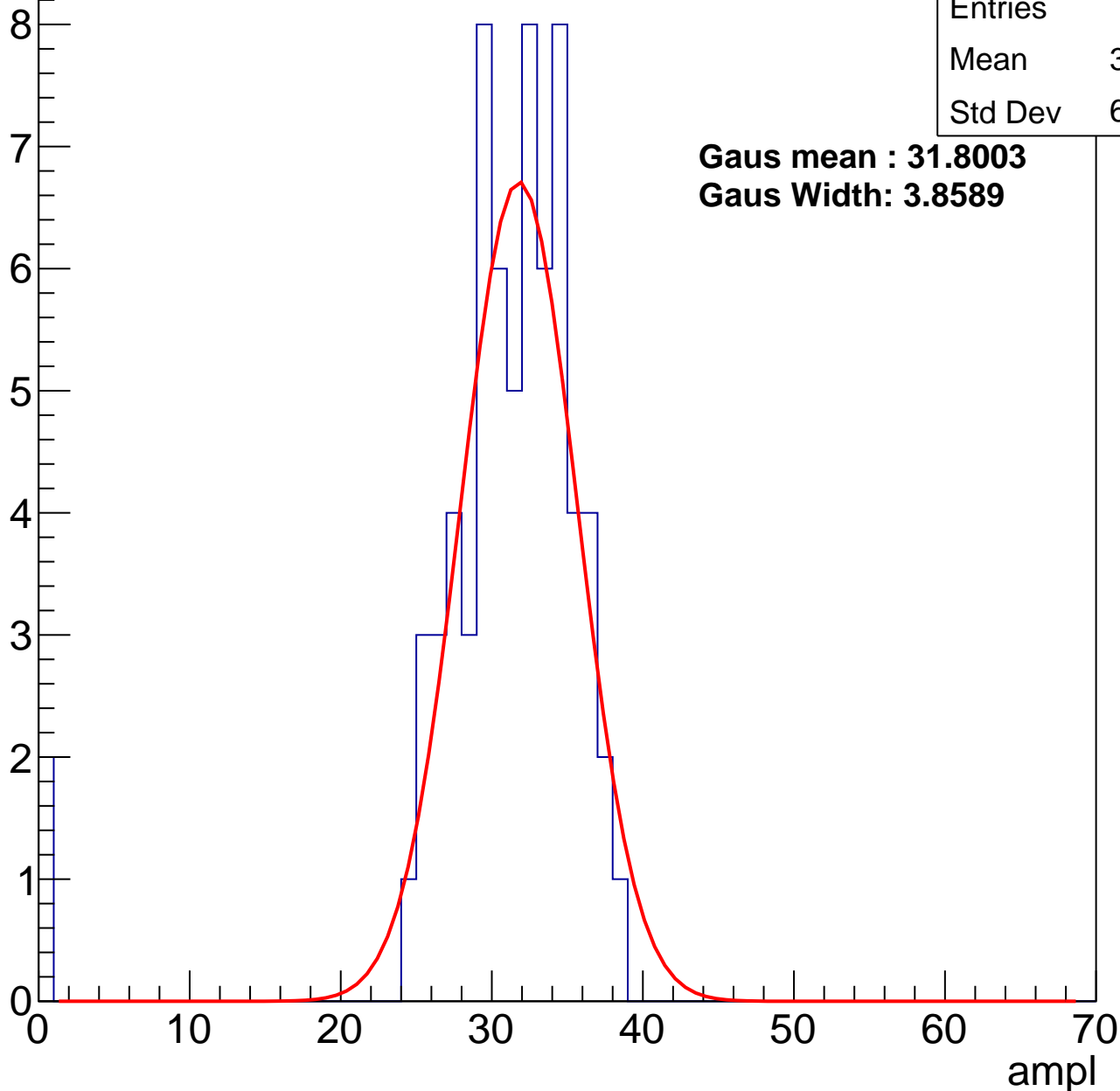
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	30.26
Std Dev	6.225

**Gaus mean : 31.8003**

**Gaus Width: 3.8589**



# B1L101S, U9-ch81, adc1

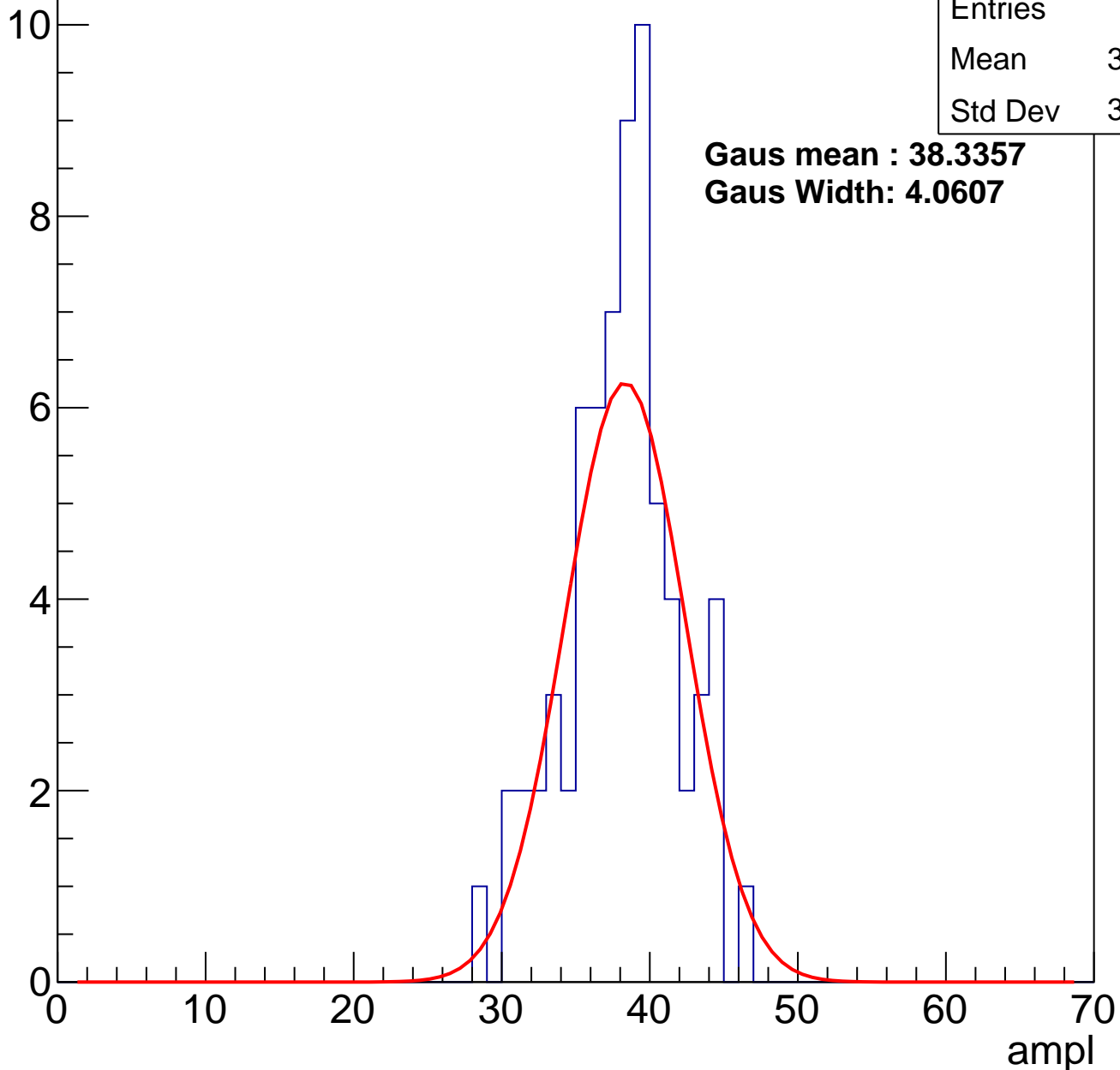
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	69
Mean	37.64
Std Dev	3.734

**Gaus mean : 38.3357**

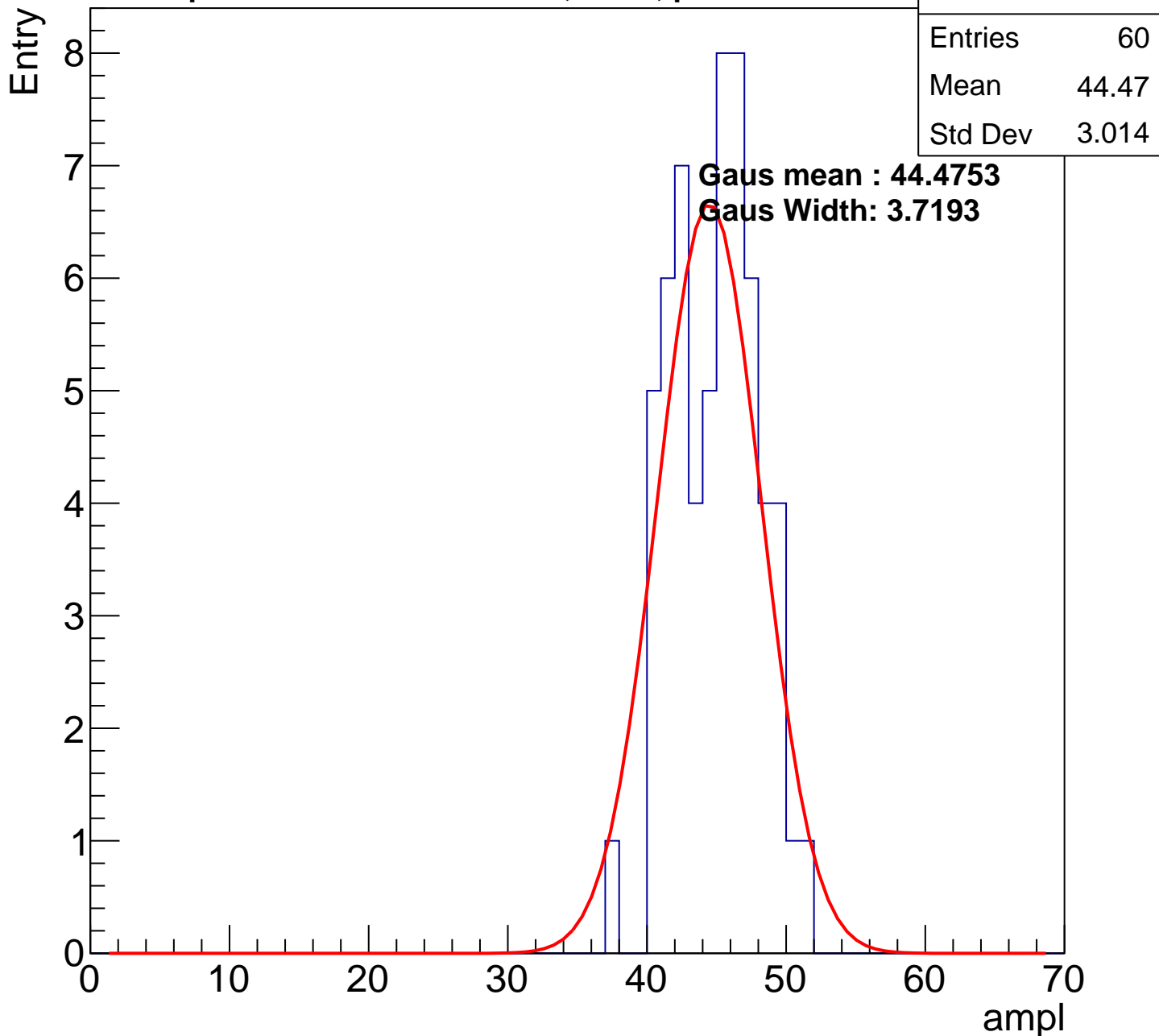
**Gaus Width: 4.0607**

Entry



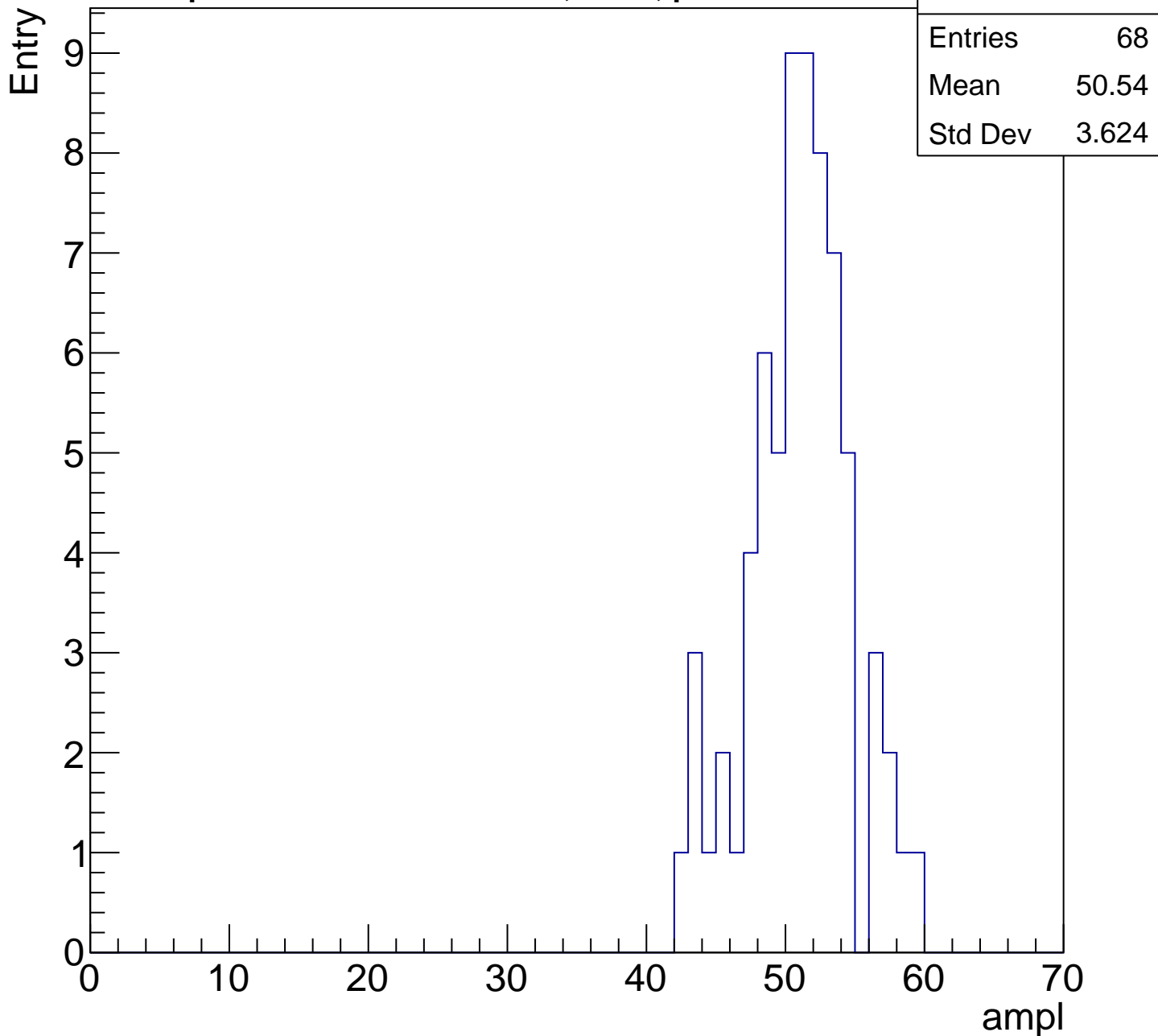
# B1L101S, U9-ch81, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

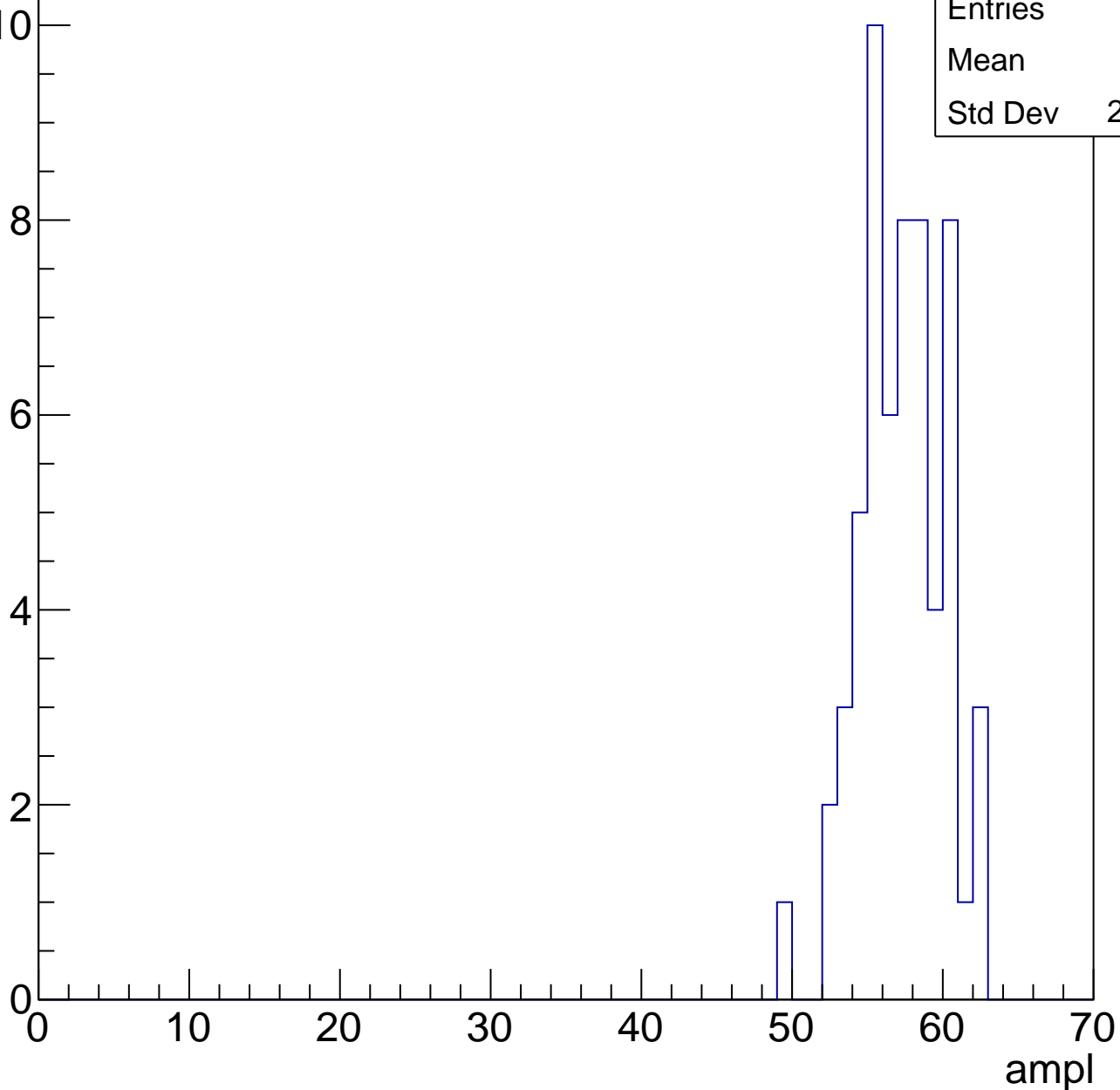


# B1L101S, U9-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	56.8
Std Dev	2.723

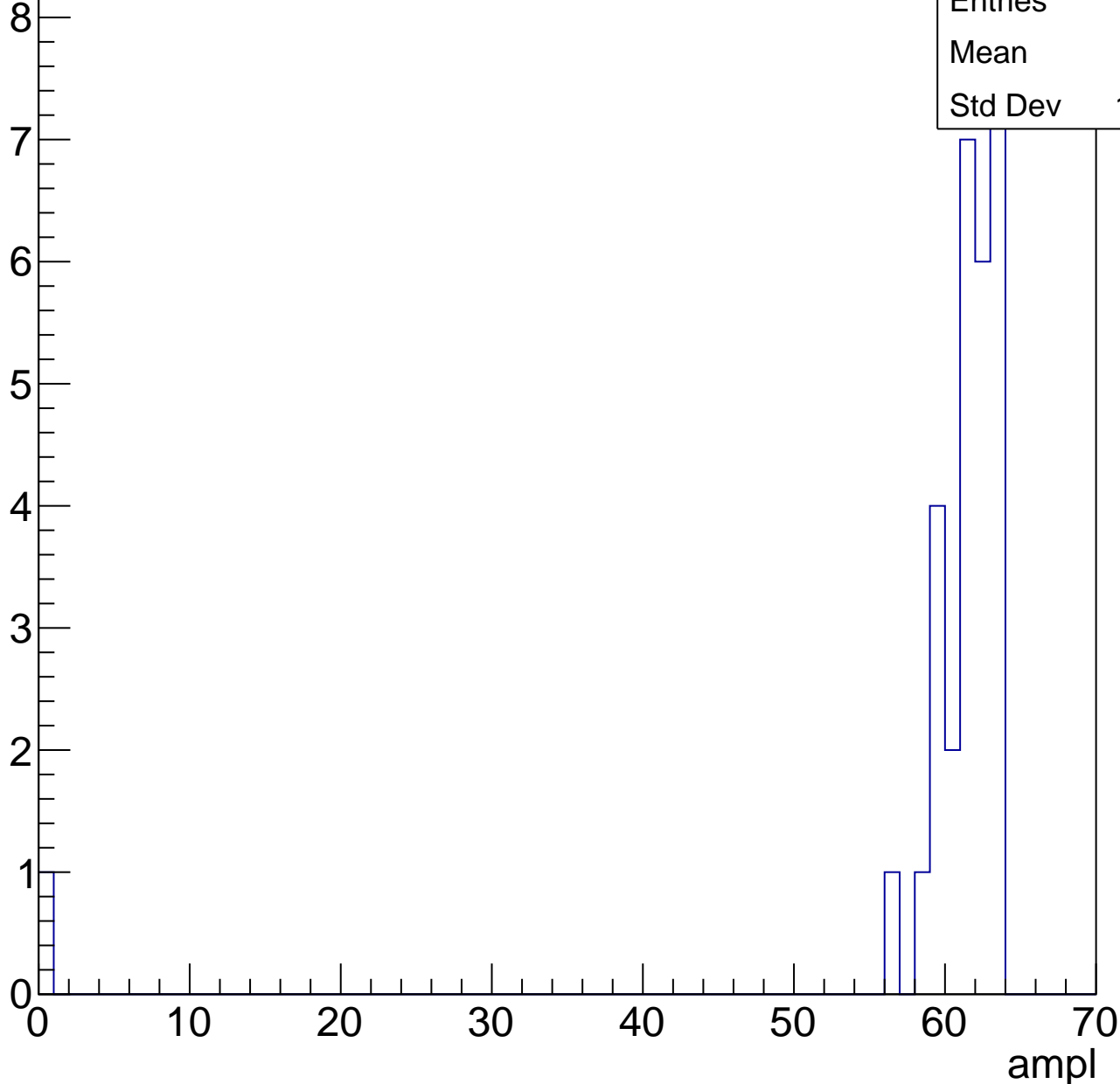


# B1L101S, U9-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

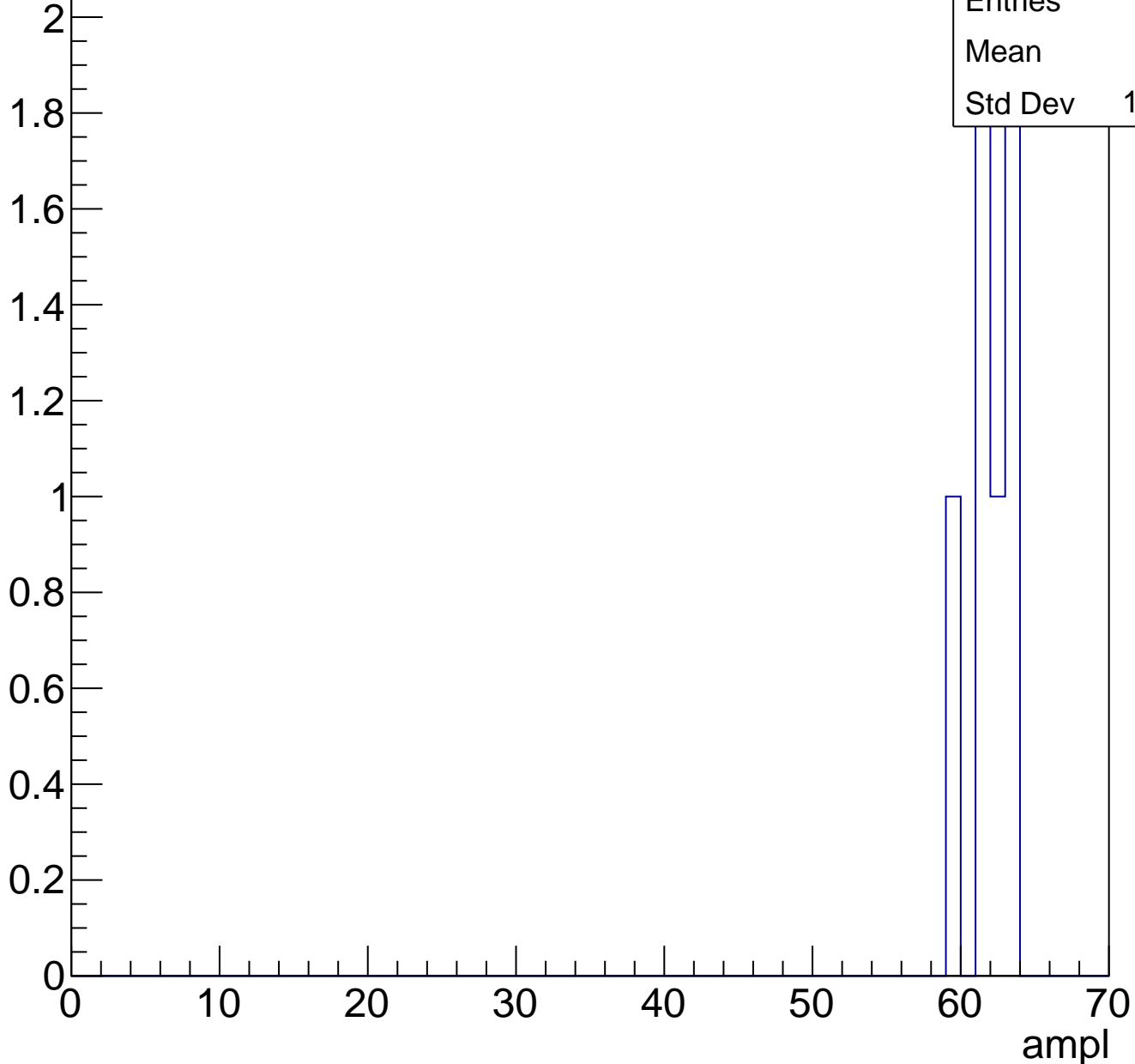
Entries	30
Mean	59.1
Std Dev	11.11



# B1L101S, U9-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch82, adc0

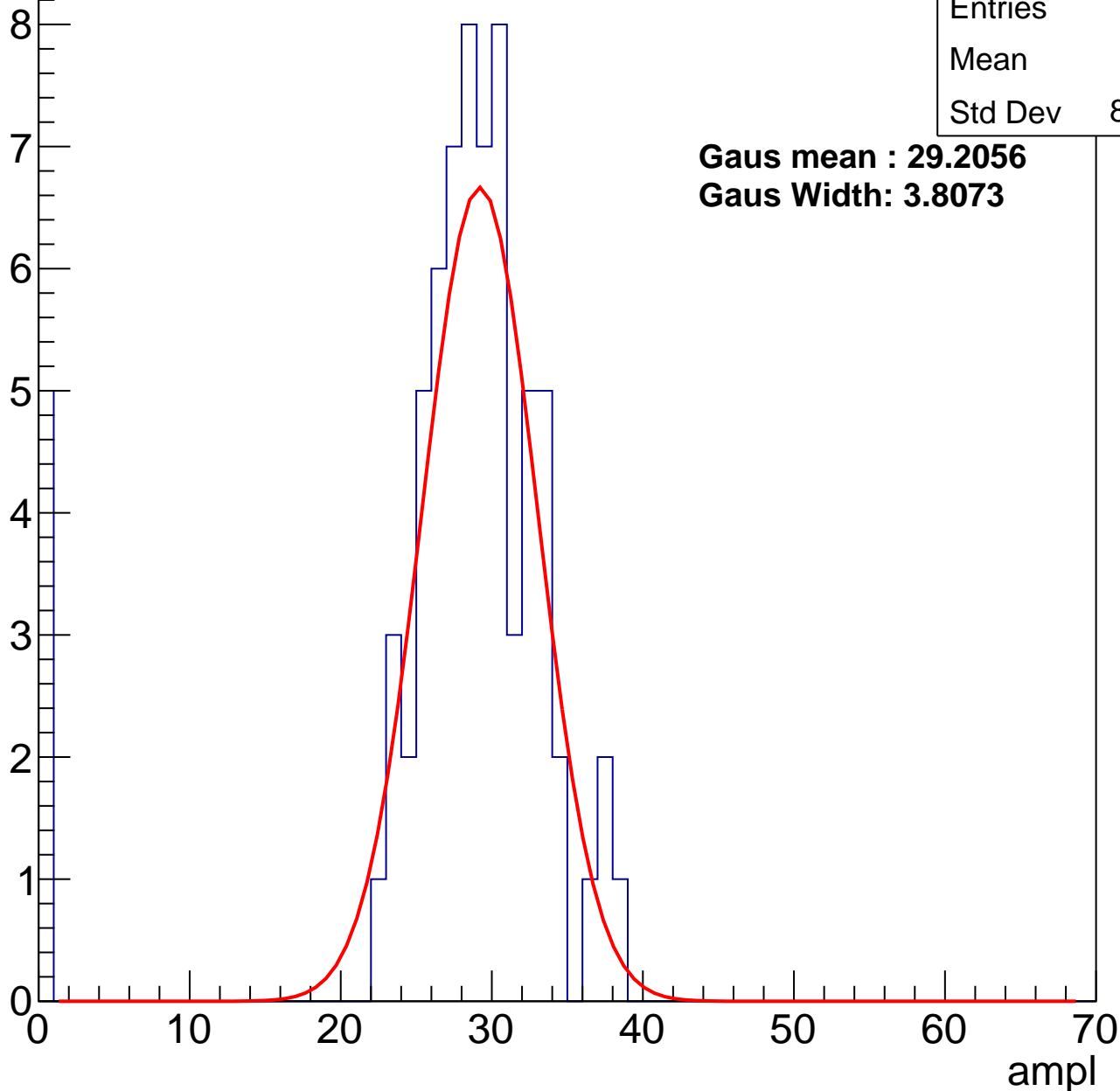
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	26.9
Std Dev	8.155

**Gaus mean : 29.2056**

**Gaus Width: 3.8073**



# B1L101S, U9-ch82, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	81
Mean	35.58
Std Dev	3.741

**Gaus mean : 35.9726**

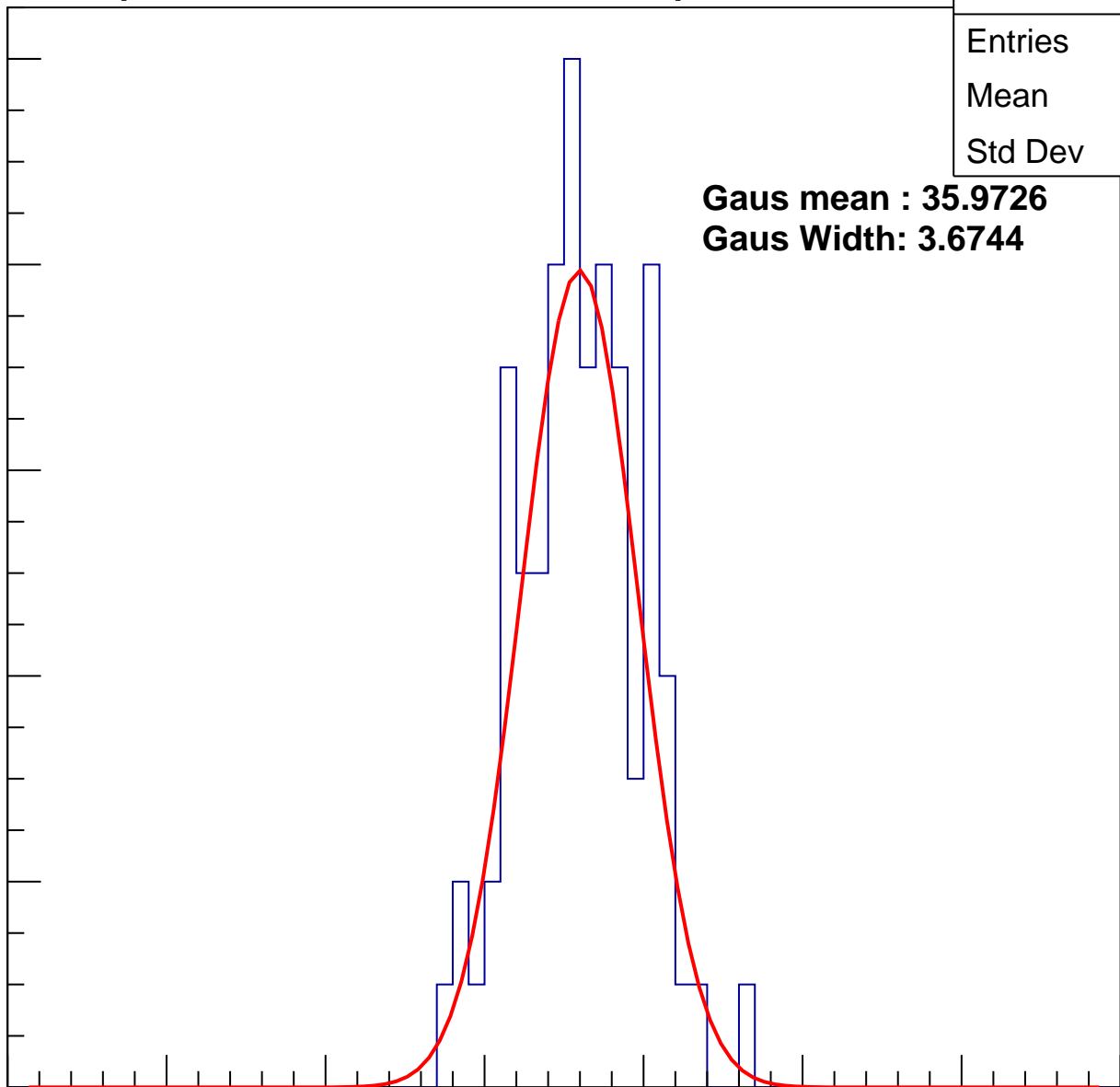
**Gaus Width: 3.6744**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

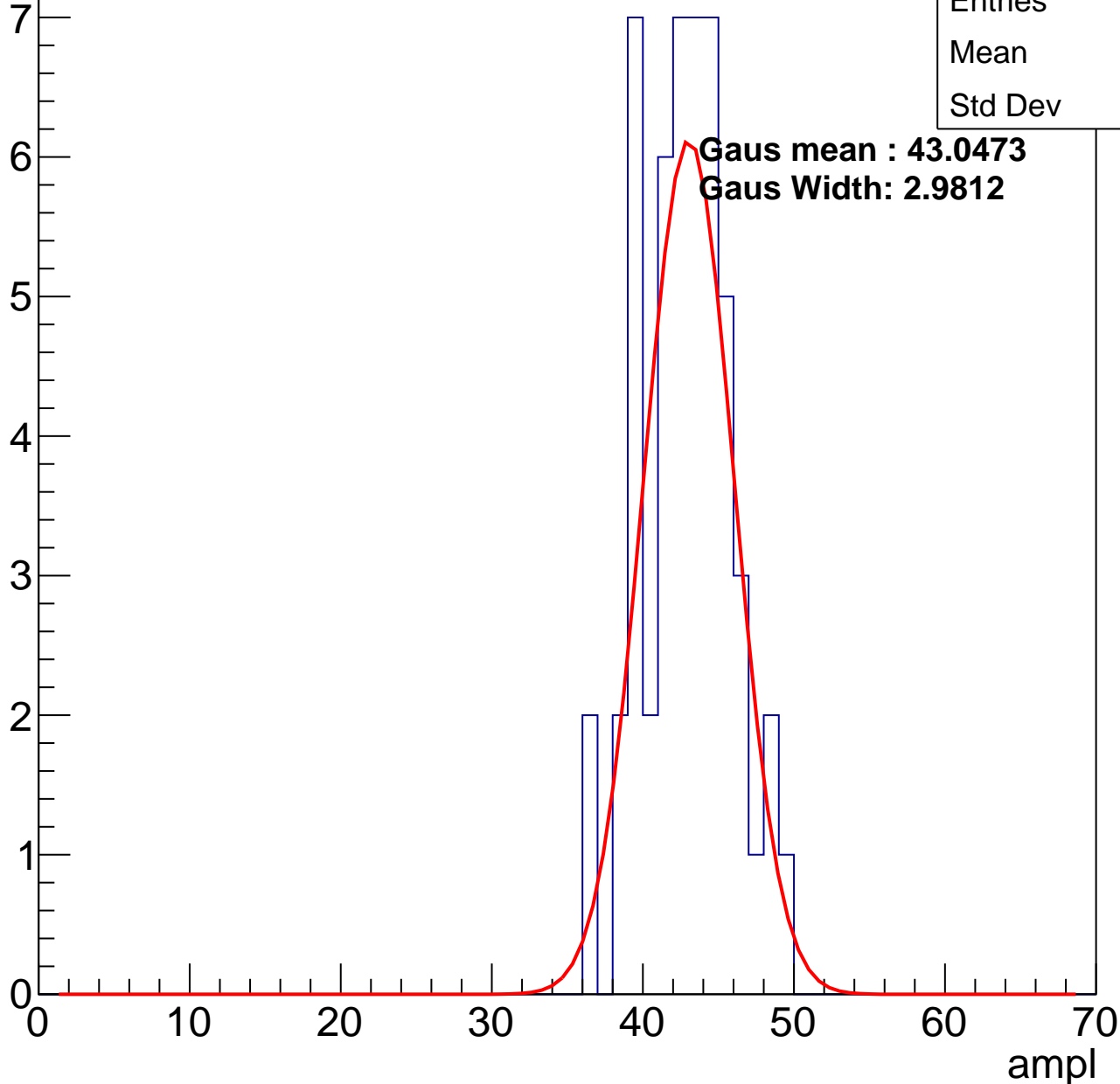


# B1L101S, U9-ch82, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

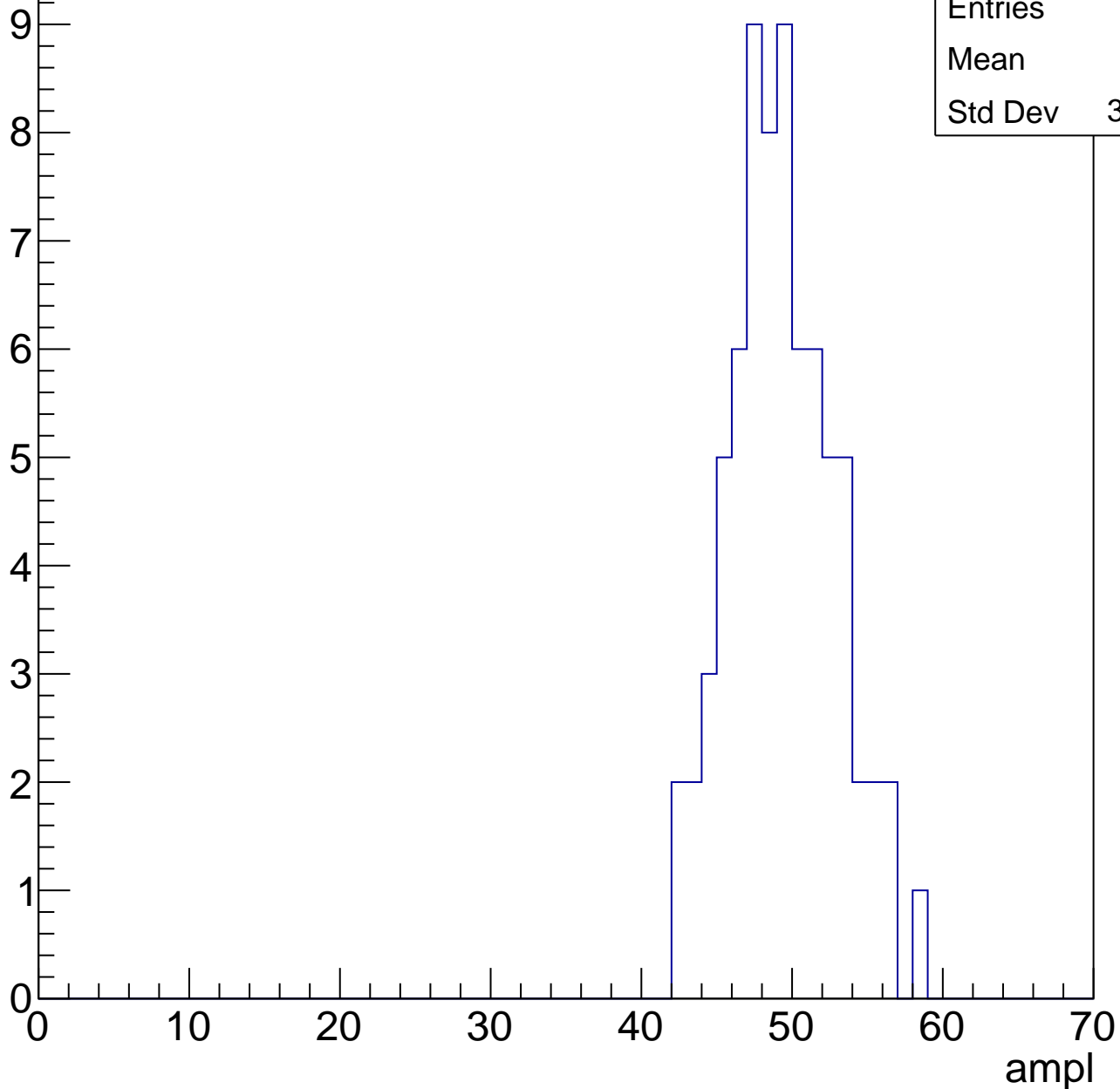
Entries	52
Mean	42.4
Std Dev	2.93



# B1L101S, U9-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

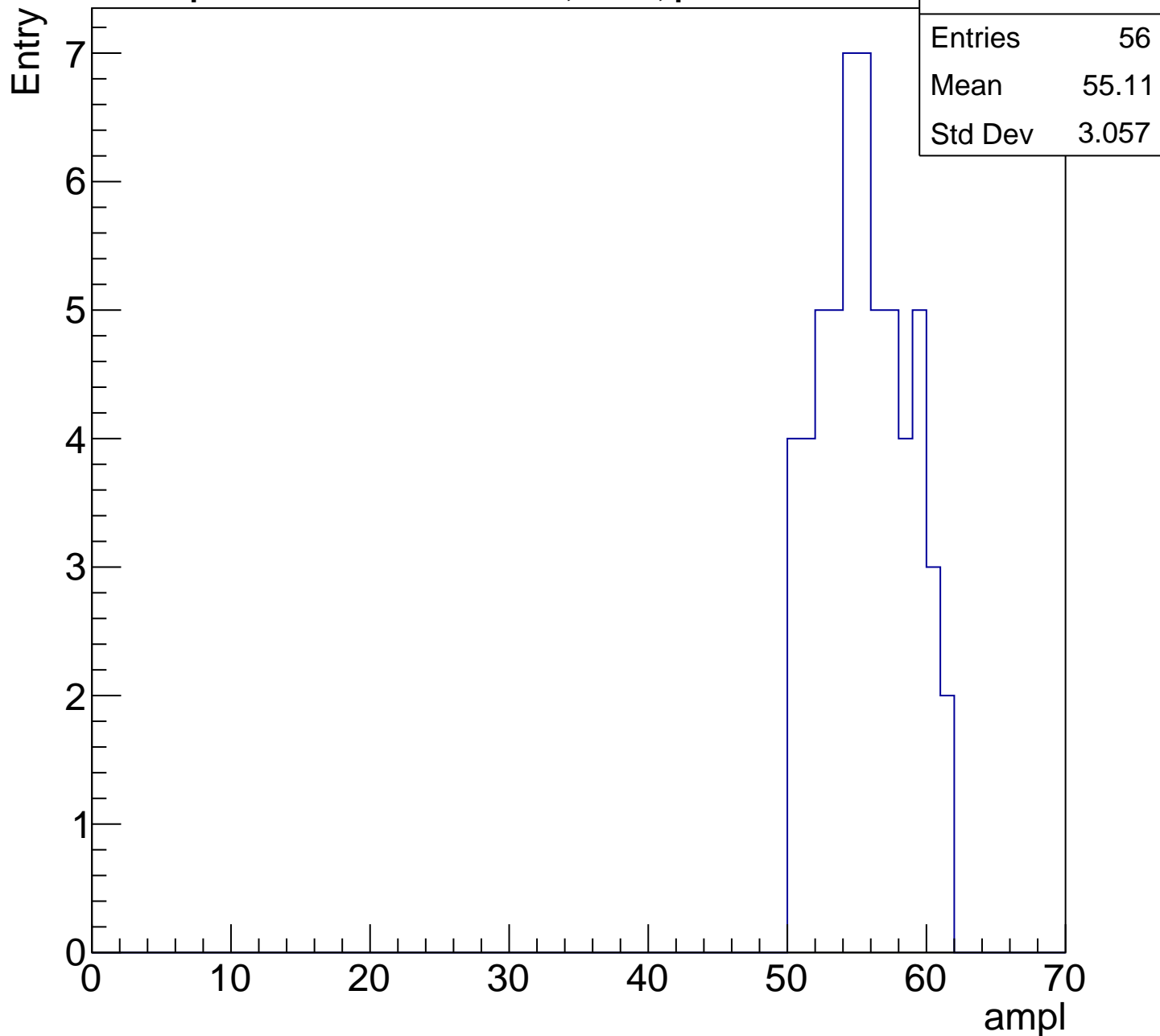
Entry



Entries	73
Mean	48.9
Std Dev	3.469

# B1L101S, U9-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

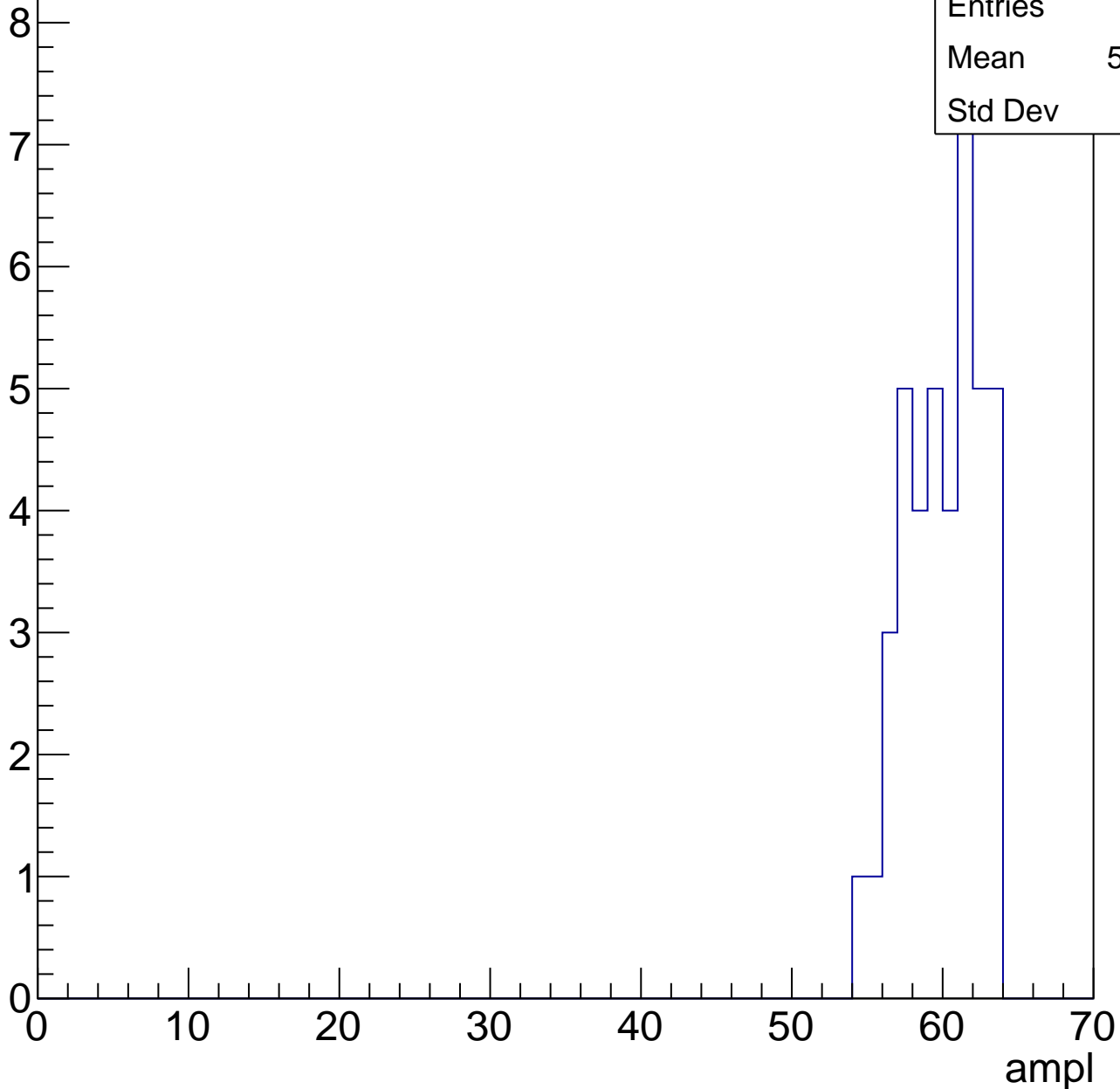


# B1L101S, U9-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	41
Mean	59.56
Std Dev	2.42

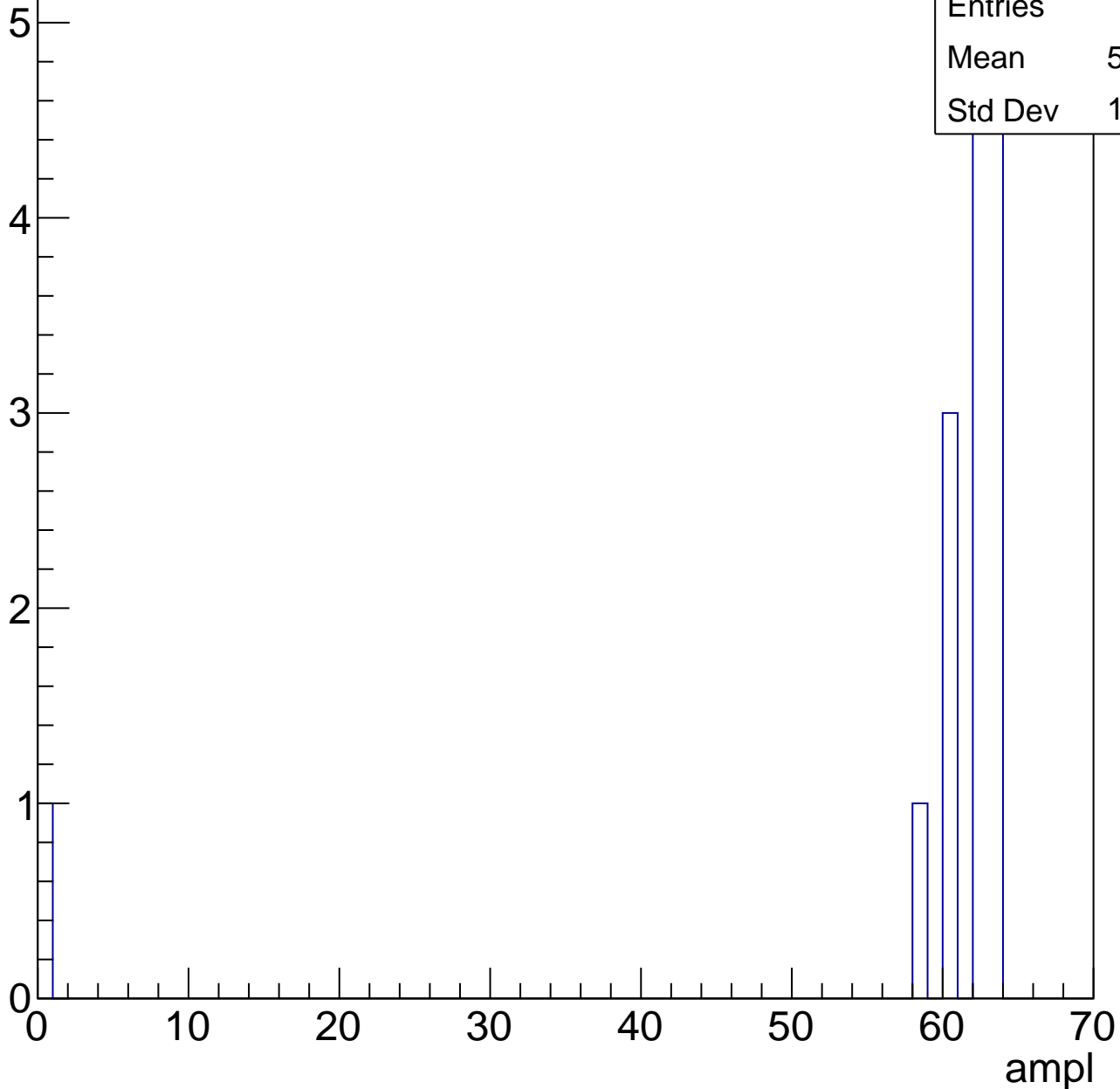


# B1L101S, U9-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	15
Mean	57.53
Std Dev	15.44





# B1L101S, U9-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch83, adc0

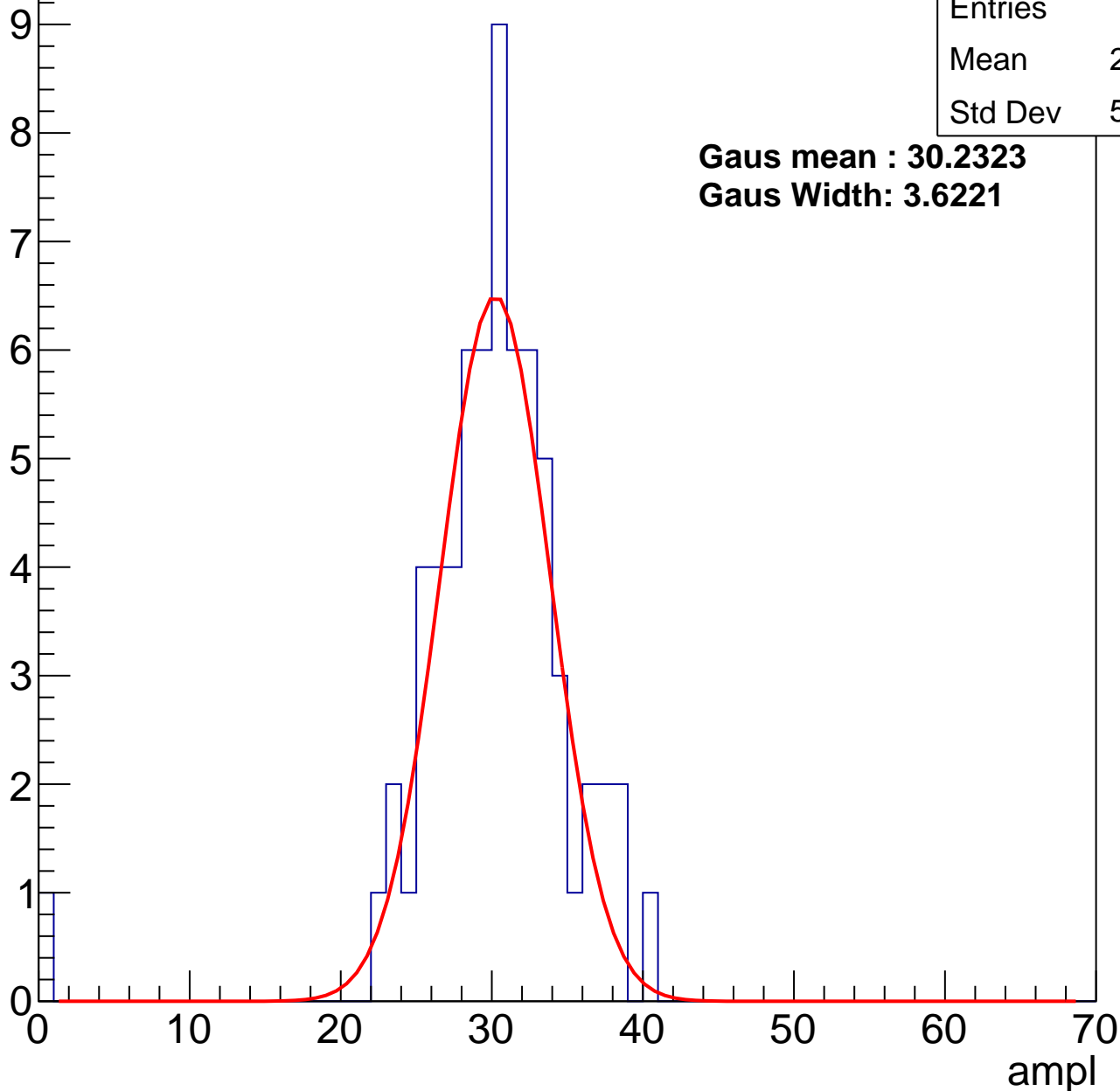
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	29.67
Std Dev	5.318

**Gaus mean : 30.2323**

**Gaus Width: 3.6221**



# B1L101S, U9-ch83, adc1

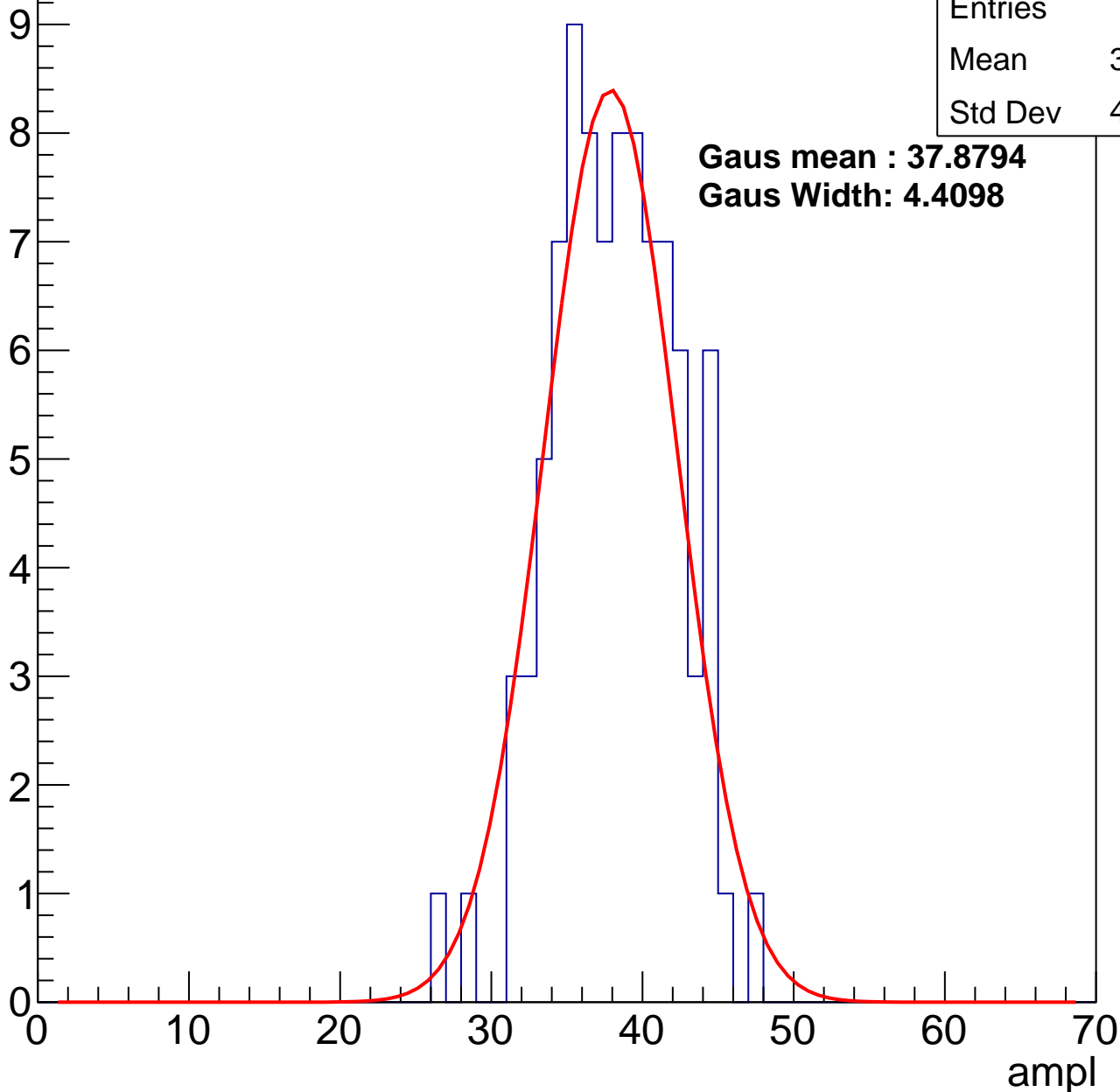
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	91
Mean	37.67
Std Dev	4.008

**Gaus mean : 37.8794**

**Gaus Width: 4.4098**



# B1L101S, U9-ch83, adc2

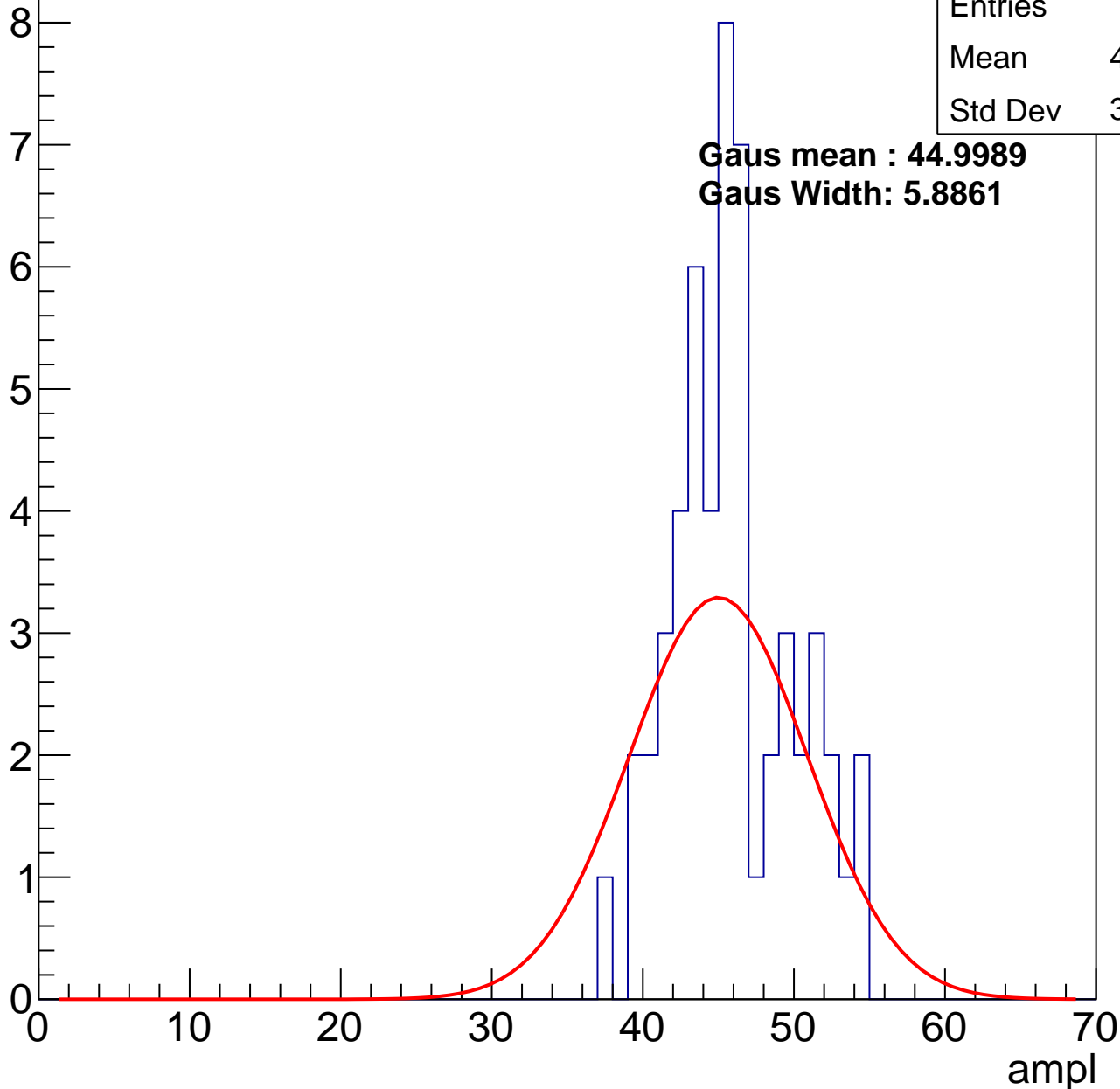
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	45.47
Std Dev	3.993

**Gaus mean : 44.9989**

**Gaus Width: 5.8861**

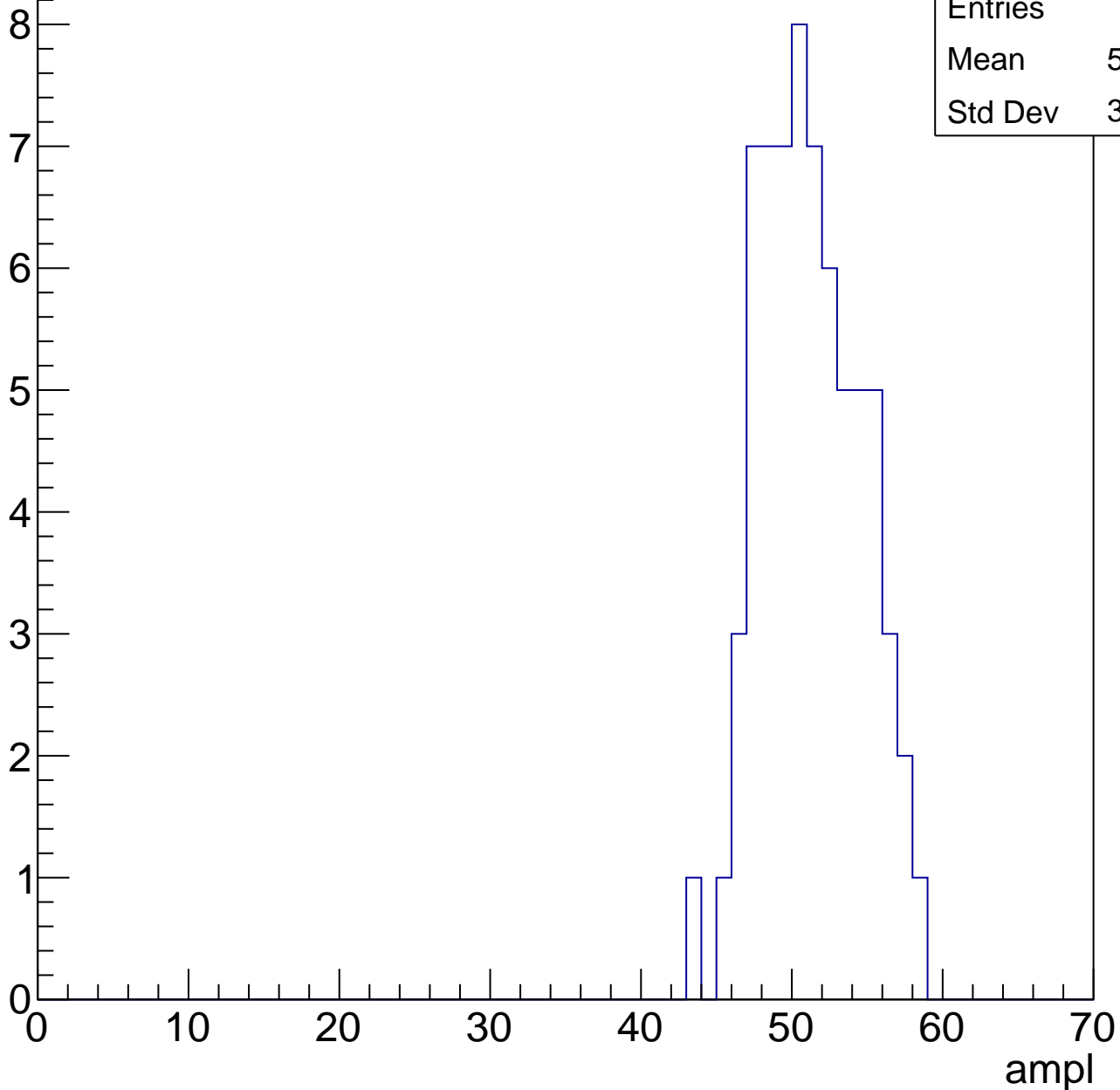


# B1L101S, U9-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

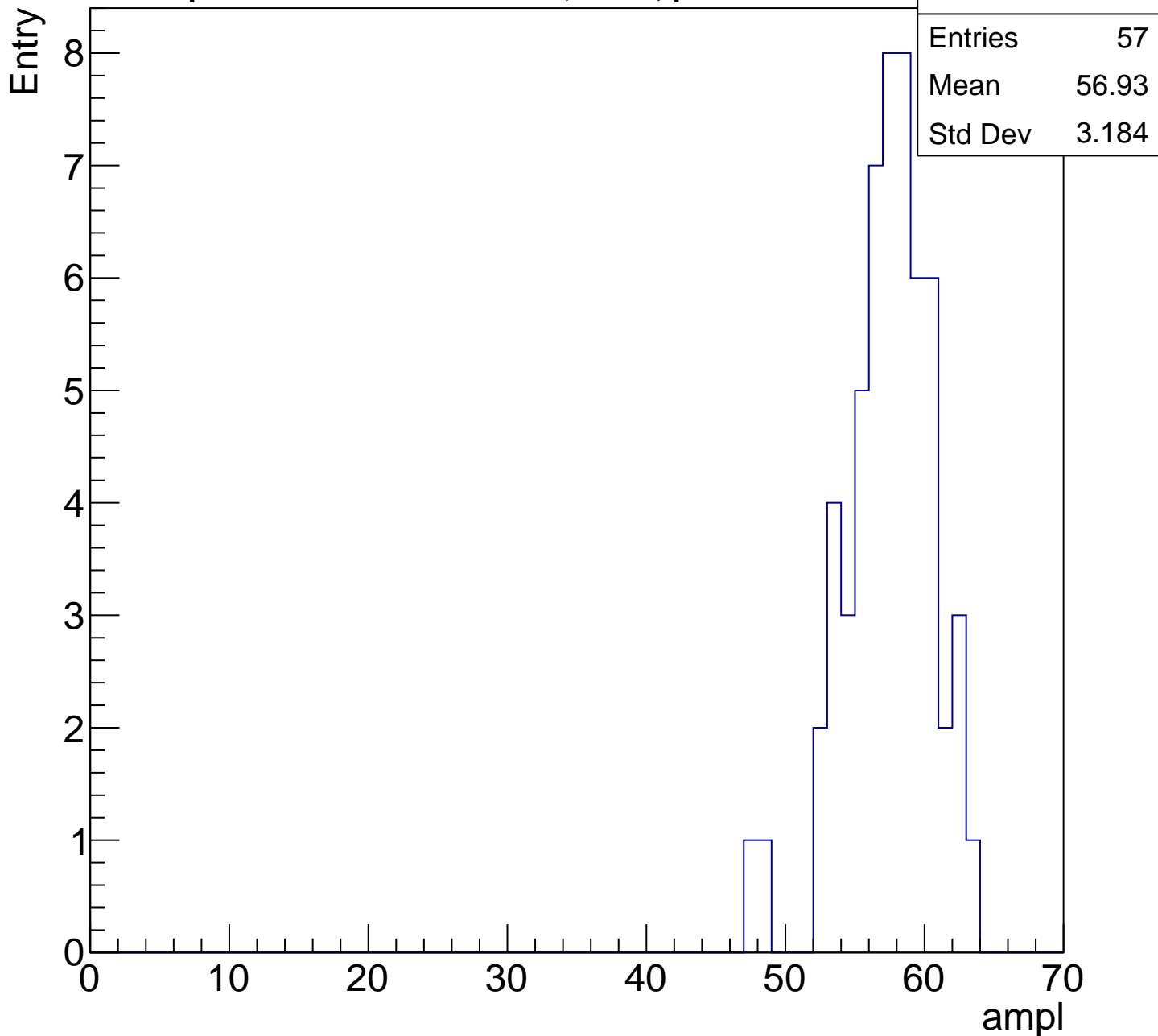
Entry

Entries	68
Mean	50.78
Std Dev	3.276



# B1L101S, U9-ch83, adc4

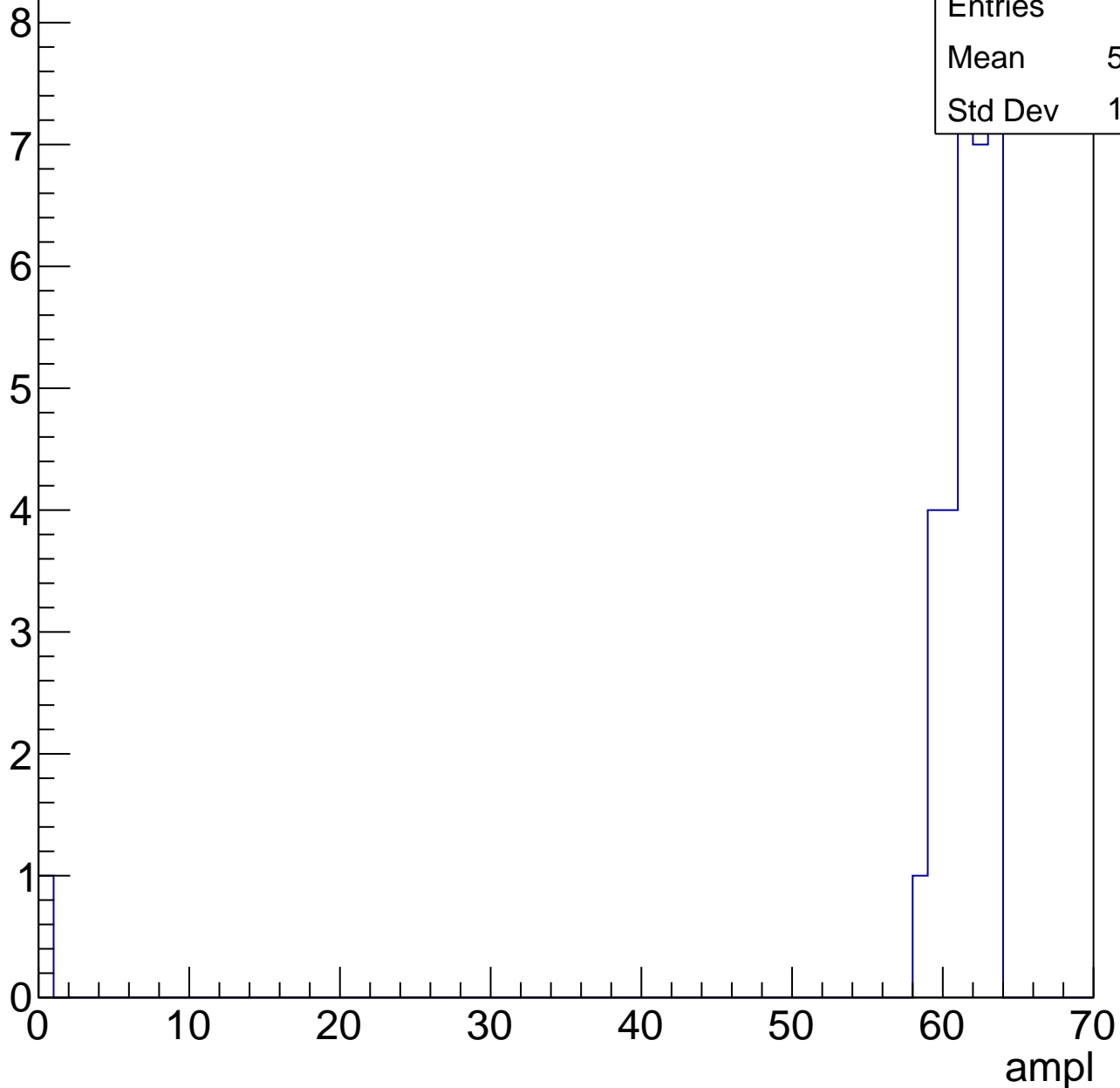
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	63
Std Dev	0

ampl



# B1L101S, U9-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U9-ch84, adc0

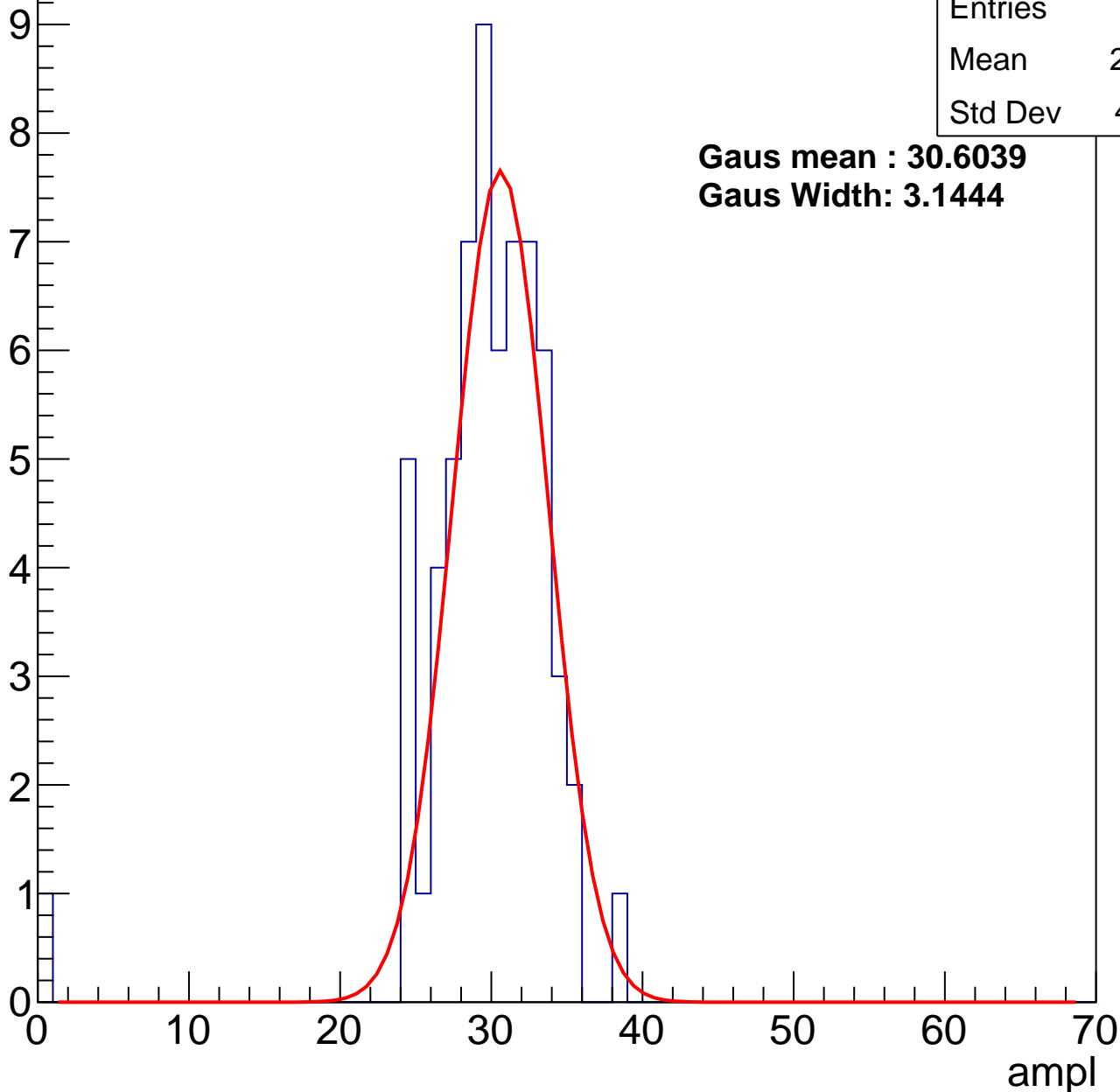
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	29.22
Std Dev	4.781

**Gaus mean : 30.6039**

**Gaus Width: 3.1444**



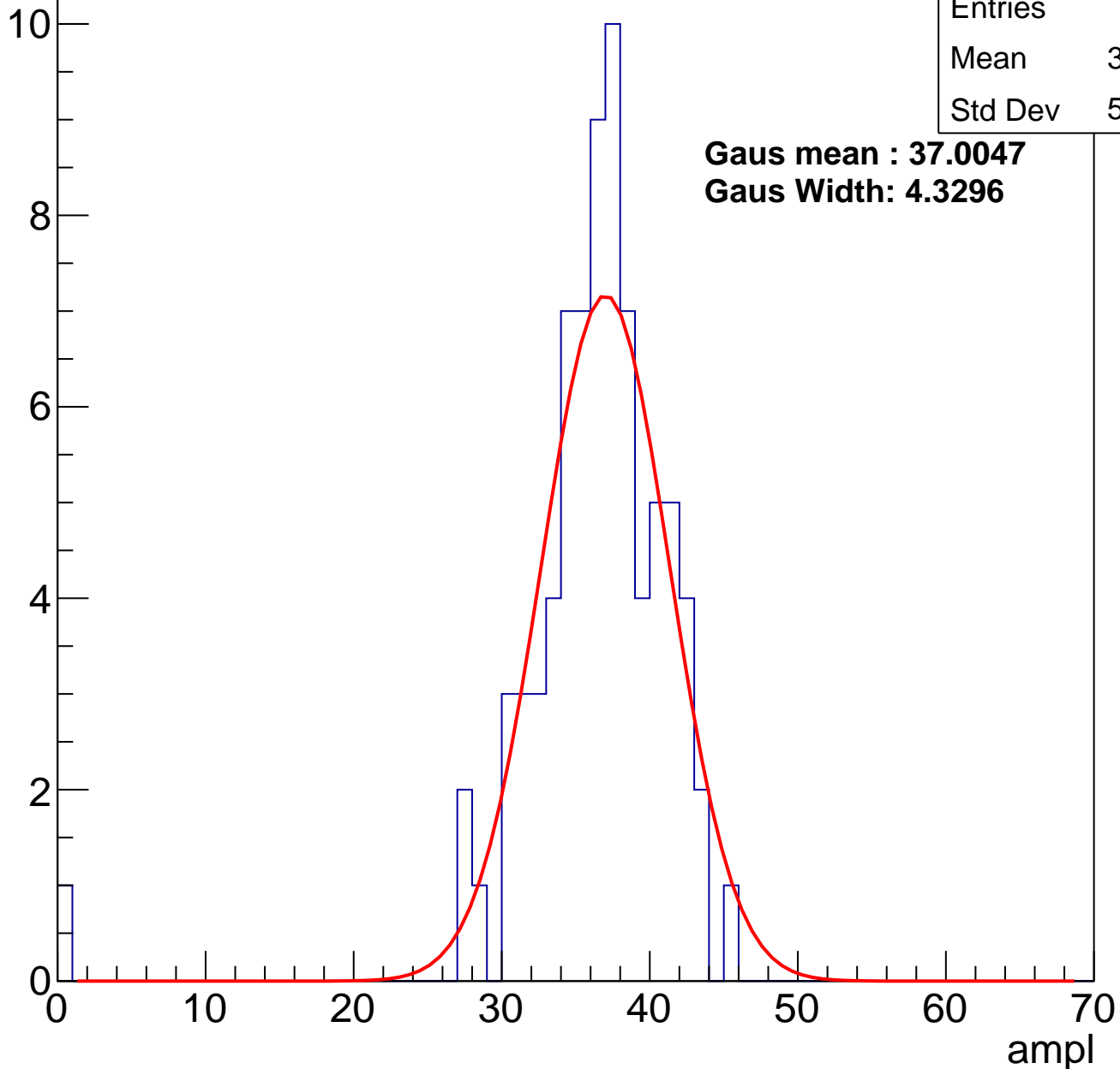
# B1L101S, U9-ch84, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	78
Mean	35.85
Std Dev	5.575

**Gaus mean : 37.0047**  
**Gaus Width: 4.3296**

Entry



# B1L101S, U9-ch84, adc2

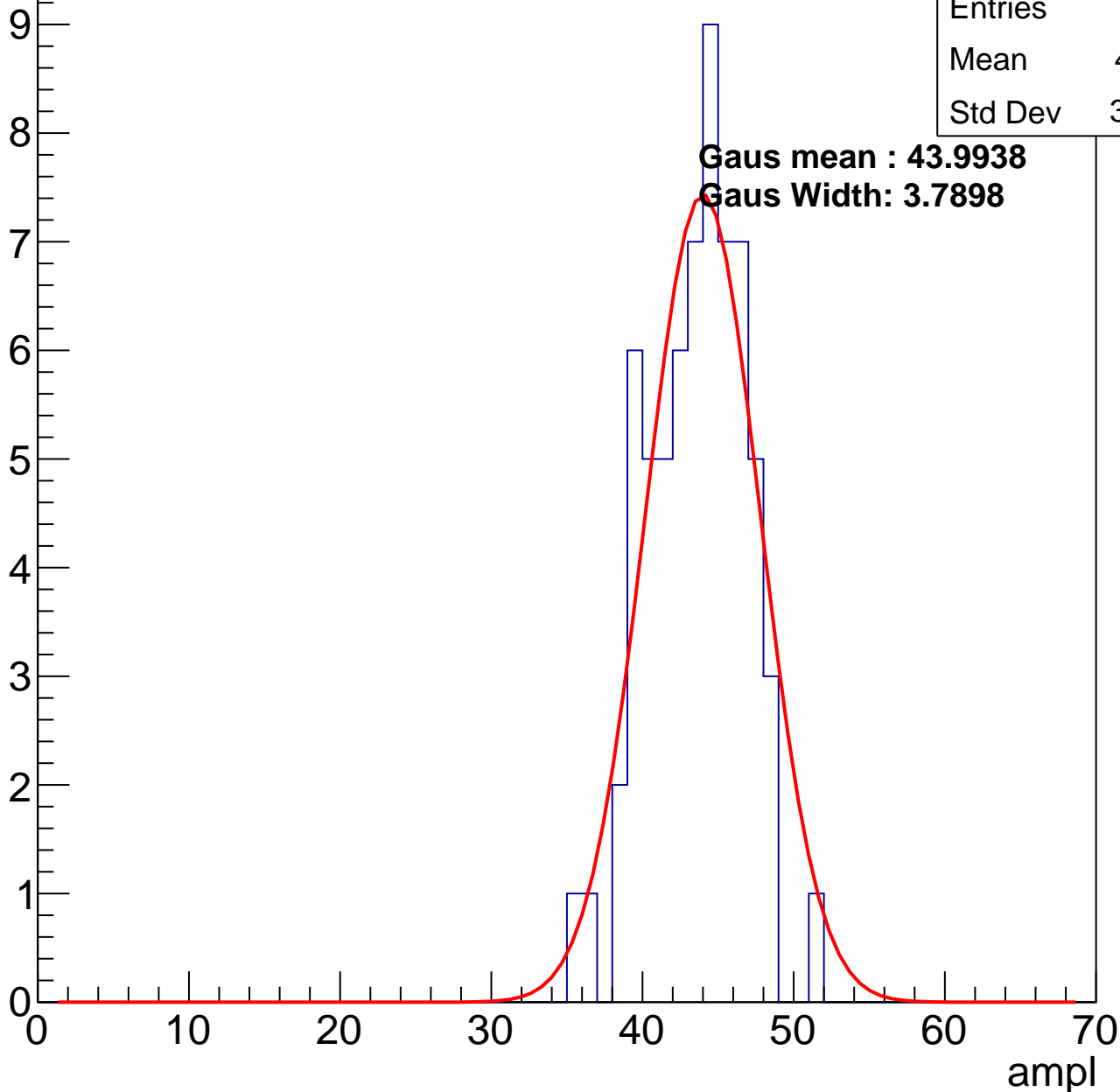
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	43.11
Std Dev	3.158

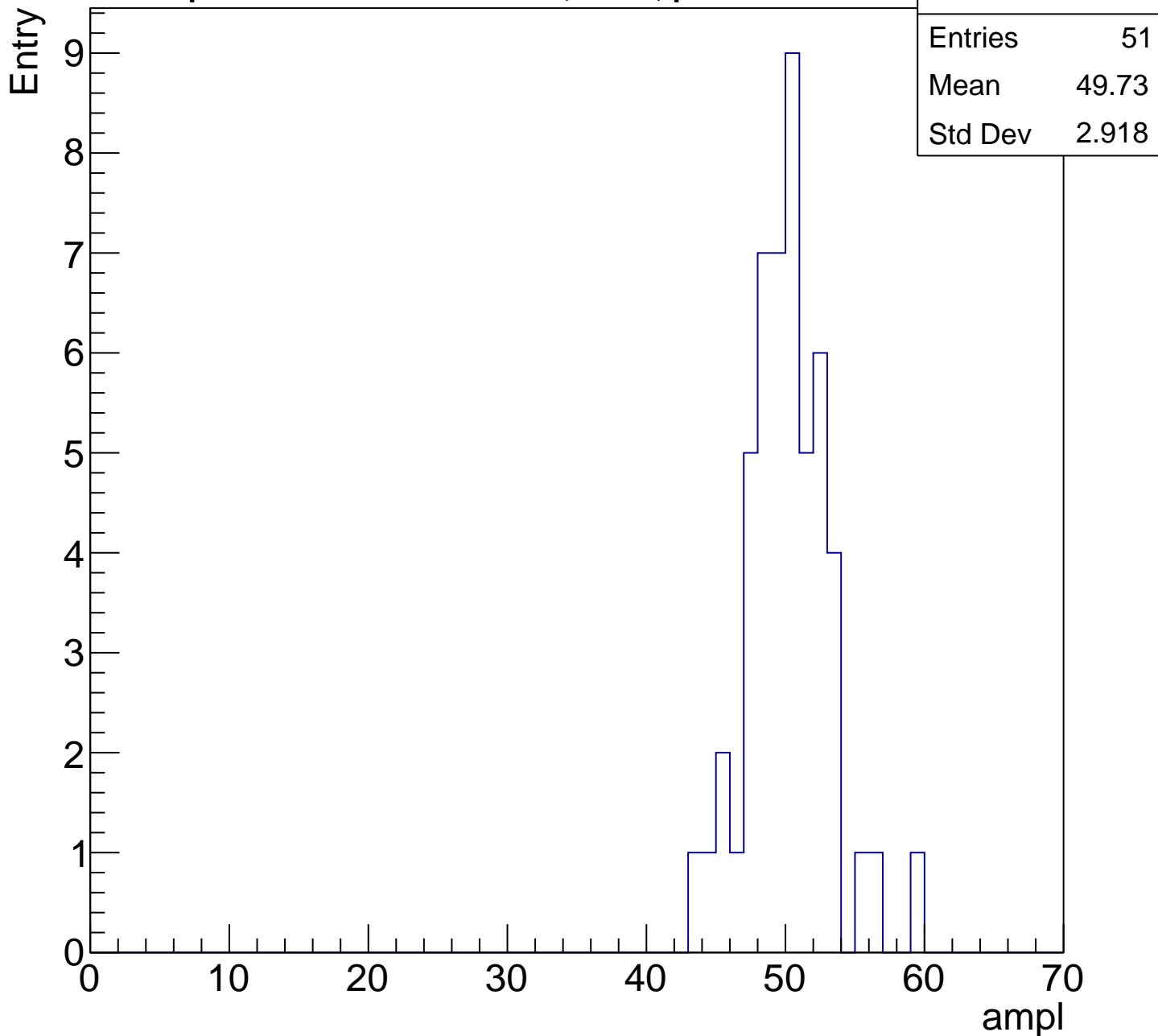
**Gaus mean : 43.9938**

**Gaus Width: 3.7898**



# B1L101S, U9-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

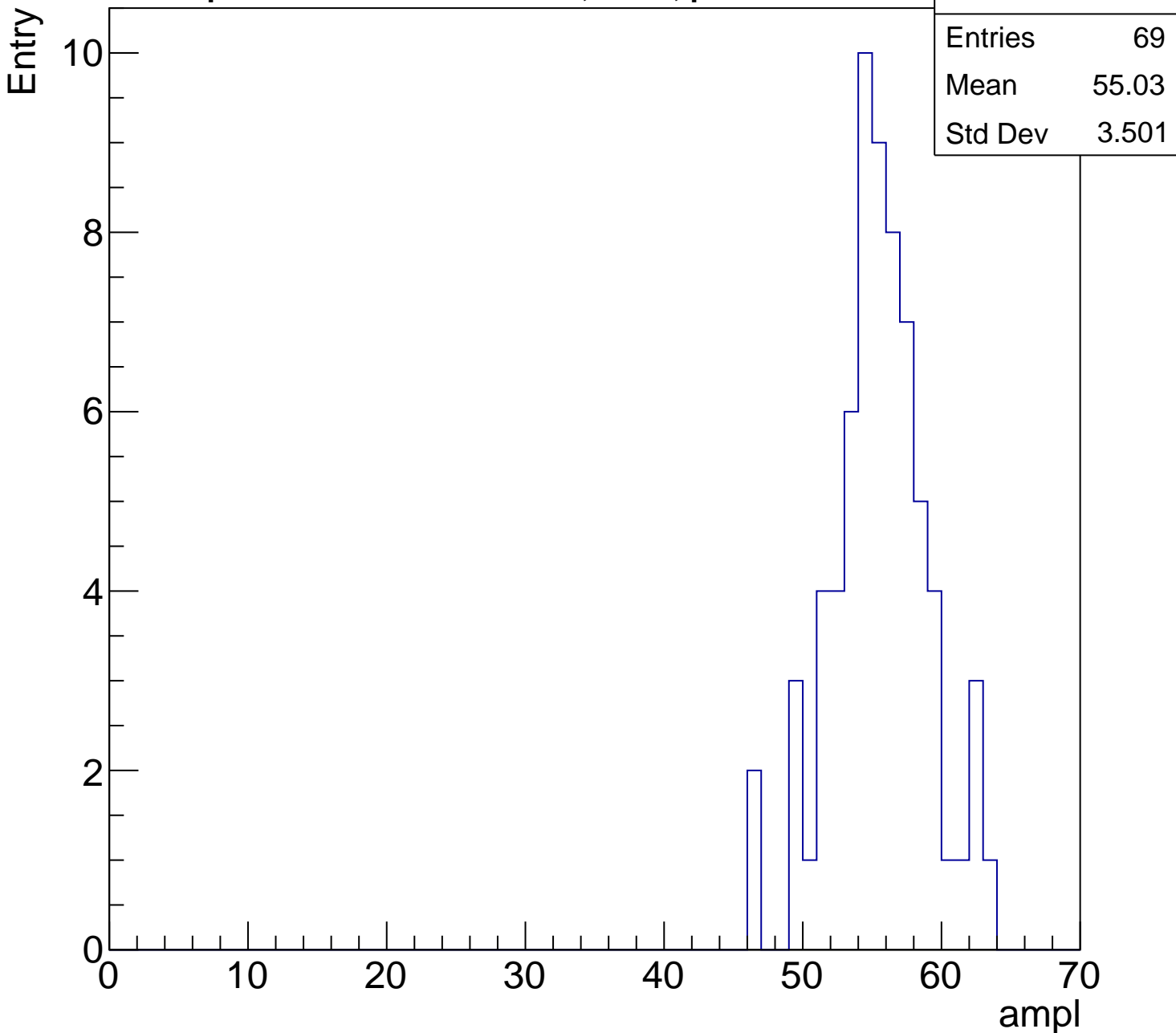
Entries	69
Mean	55.03
Std Dev	3.501

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U9-ch84, adc5

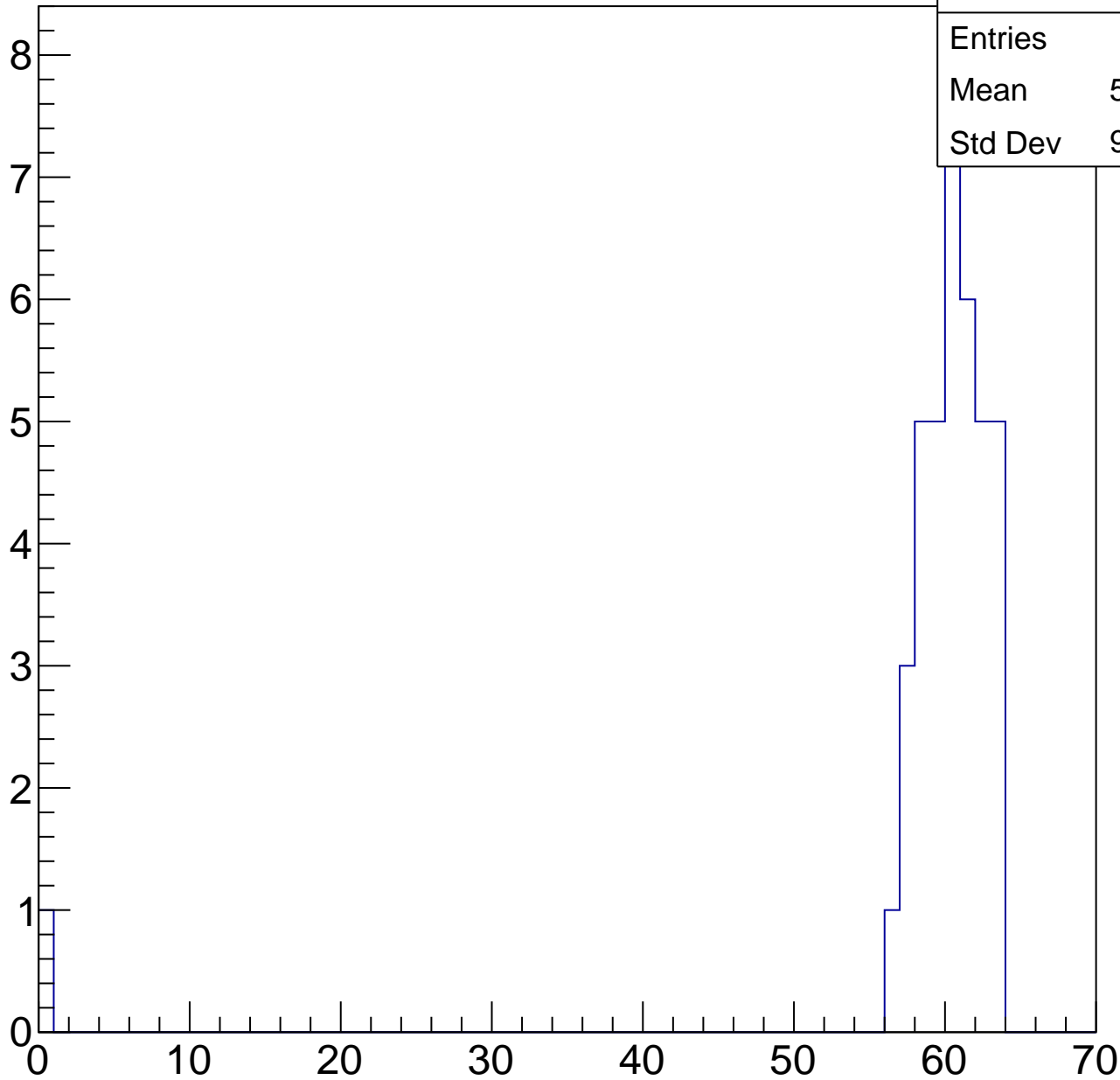
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	39
Mean	58.54
Std Dev	9.682

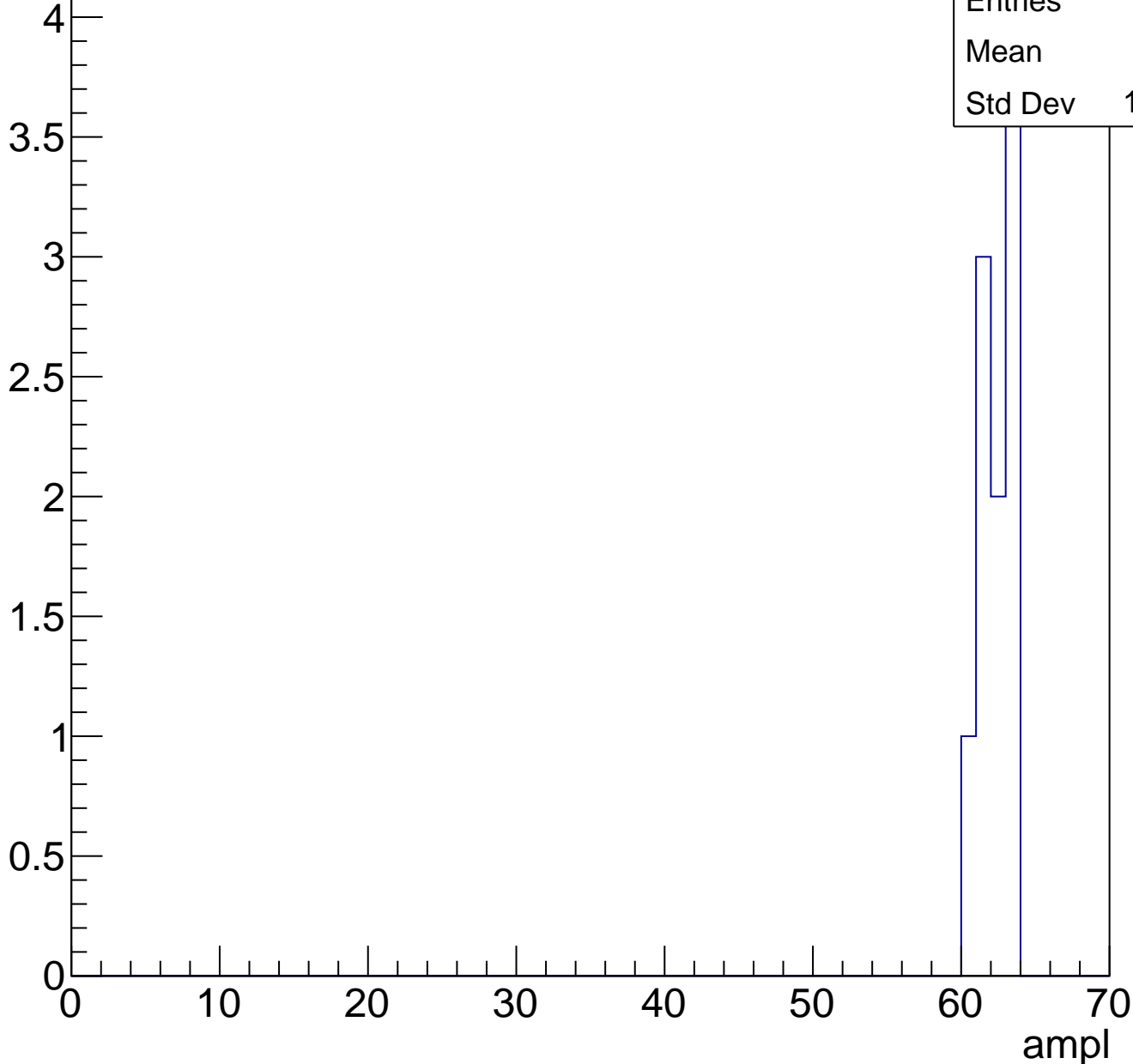
ampl



# B1L101S, U9-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	10
Mean	61.9
Std Dev	1.044



# B1L101S, U9-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch85, adc0

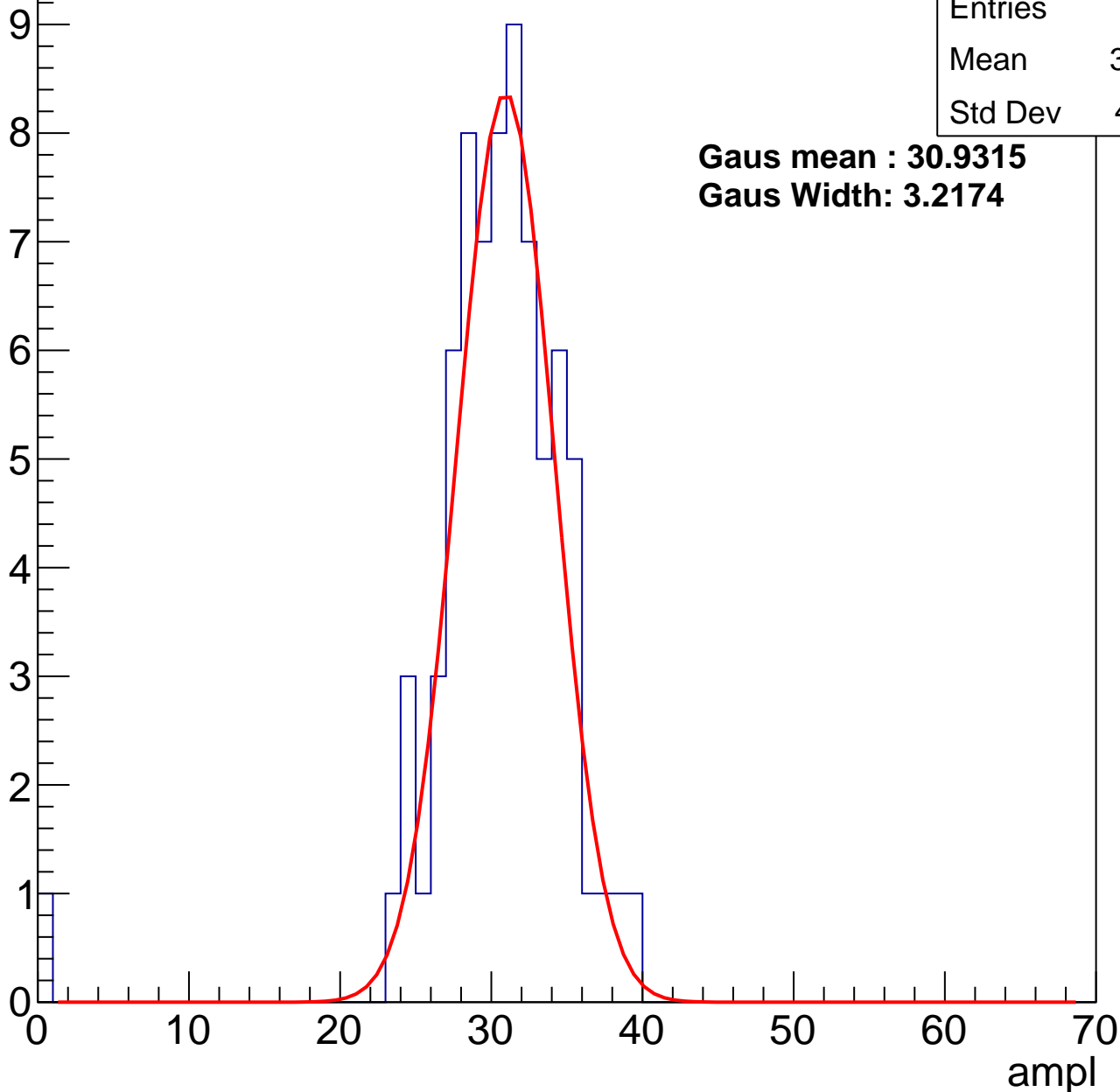
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	30.05
Std Dev	4.871

**Gaus mean : 30.9315**

**Gaus Width: 3.2174**



# B1L101S, U9-ch85, adc1

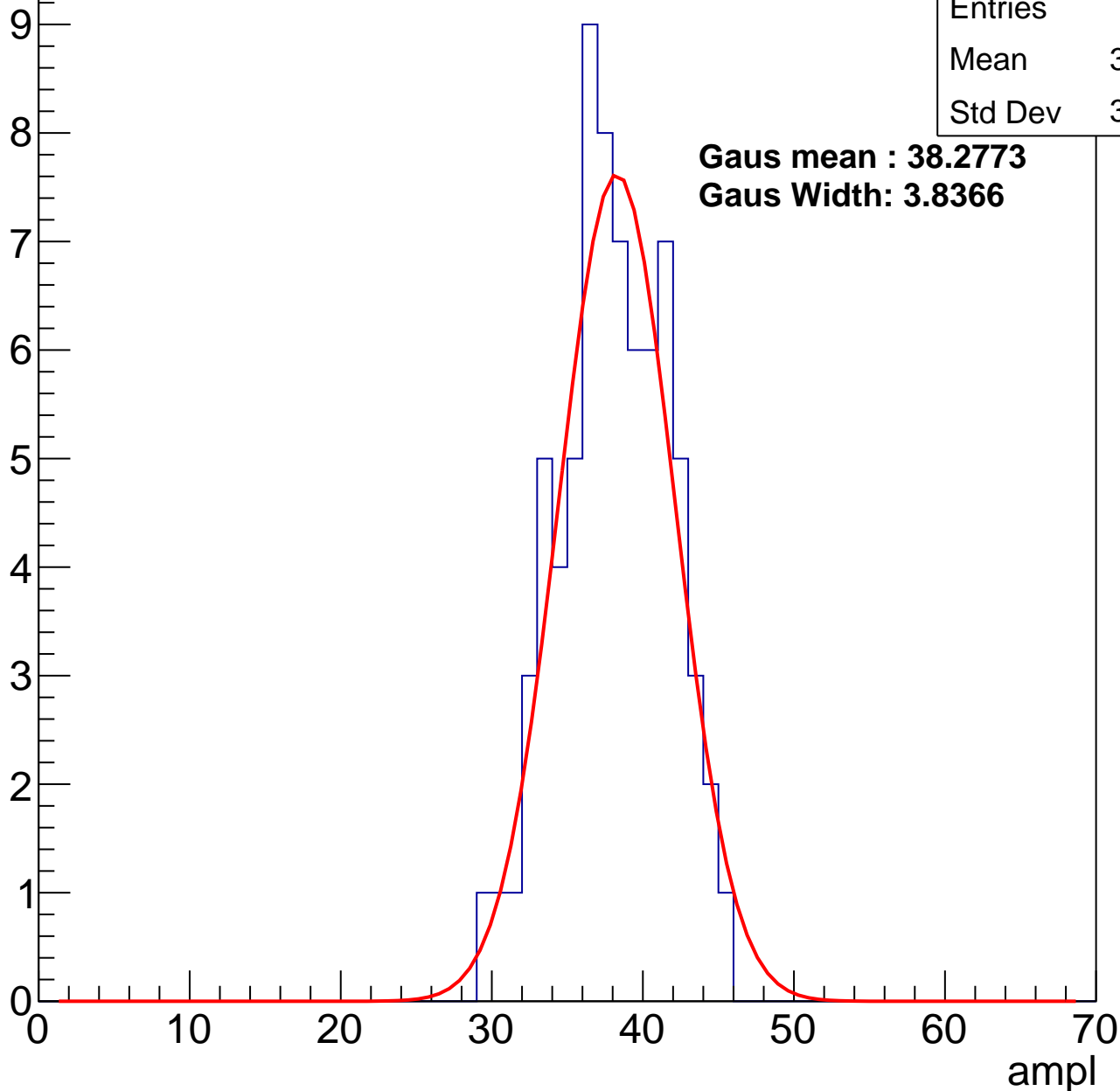
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	37.58
Std Dev	3.557

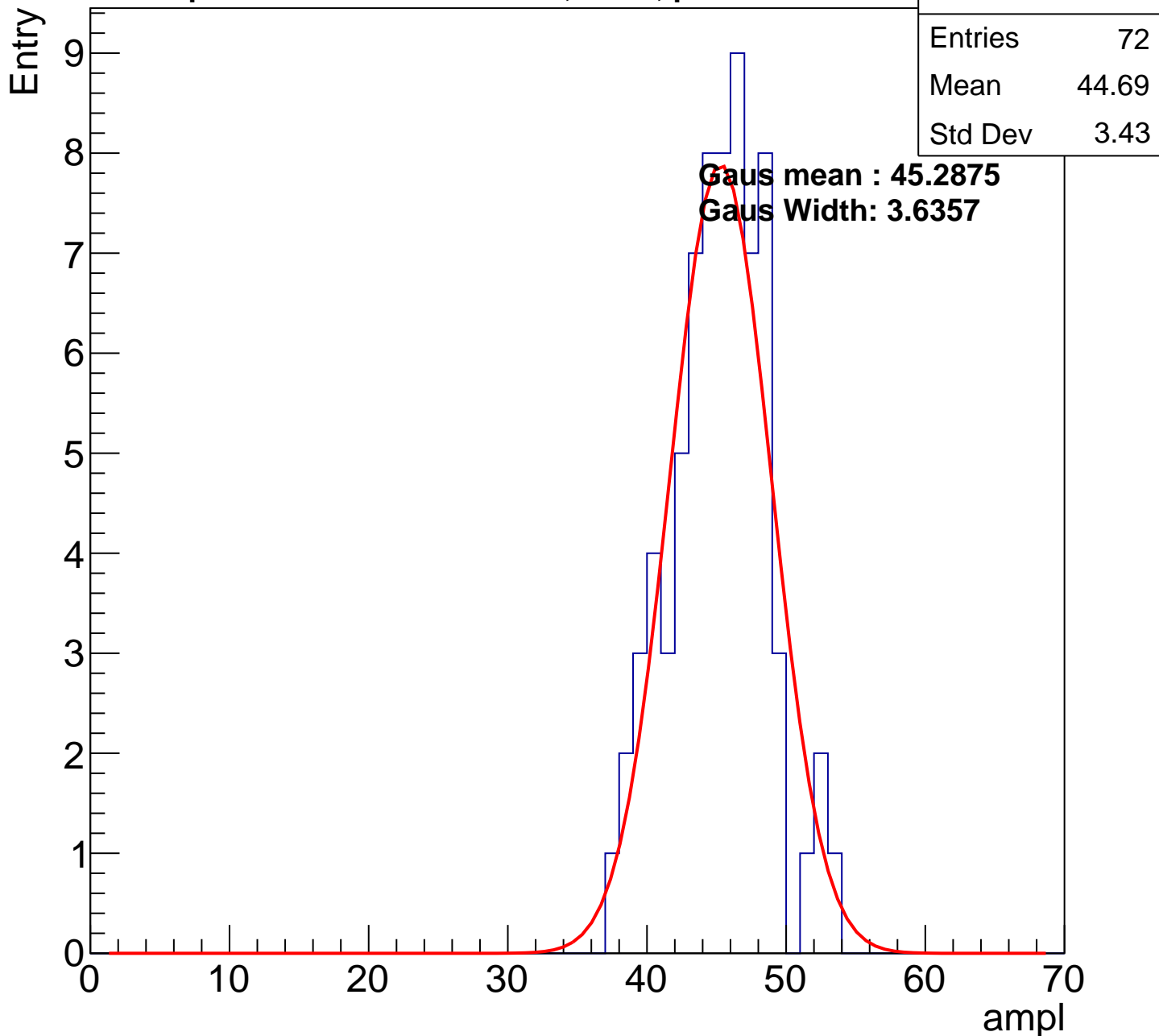
**Gaus mean : 38.2773**

**Gaus Width: 3.8366**



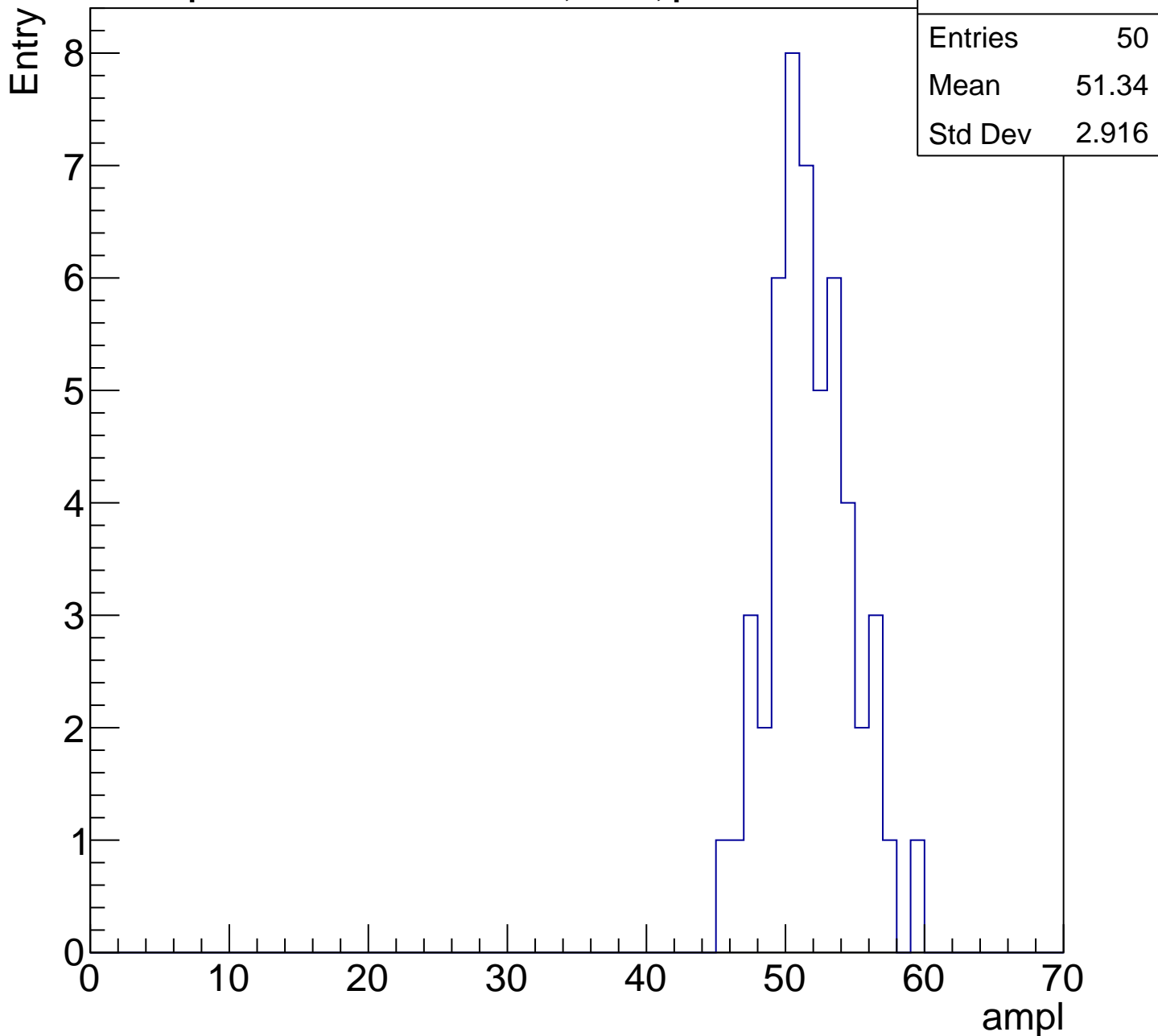
# B1L101S, U9-ch85, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

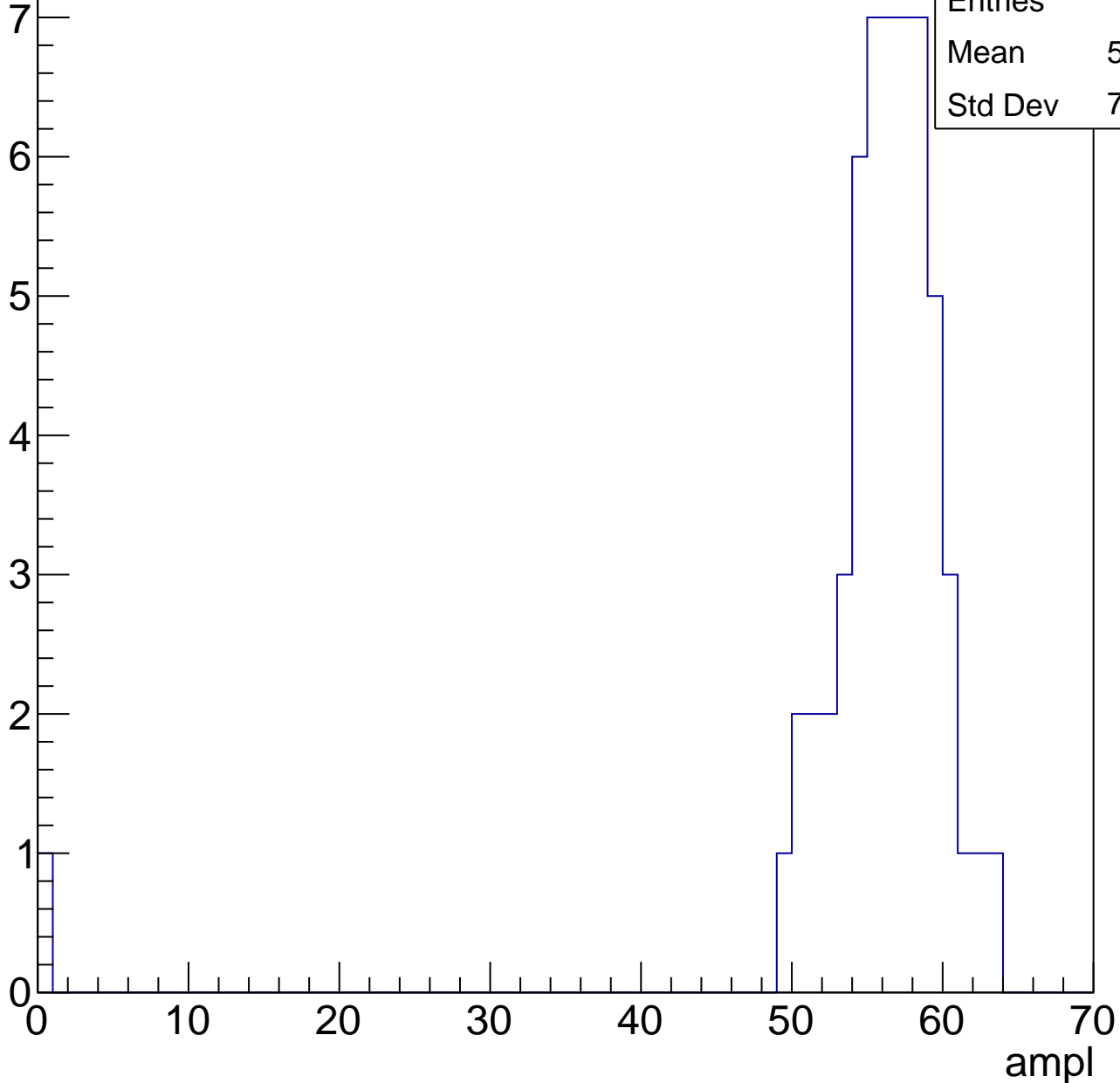


# B1L101S, U9-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	55.02
Std Dev	7.997

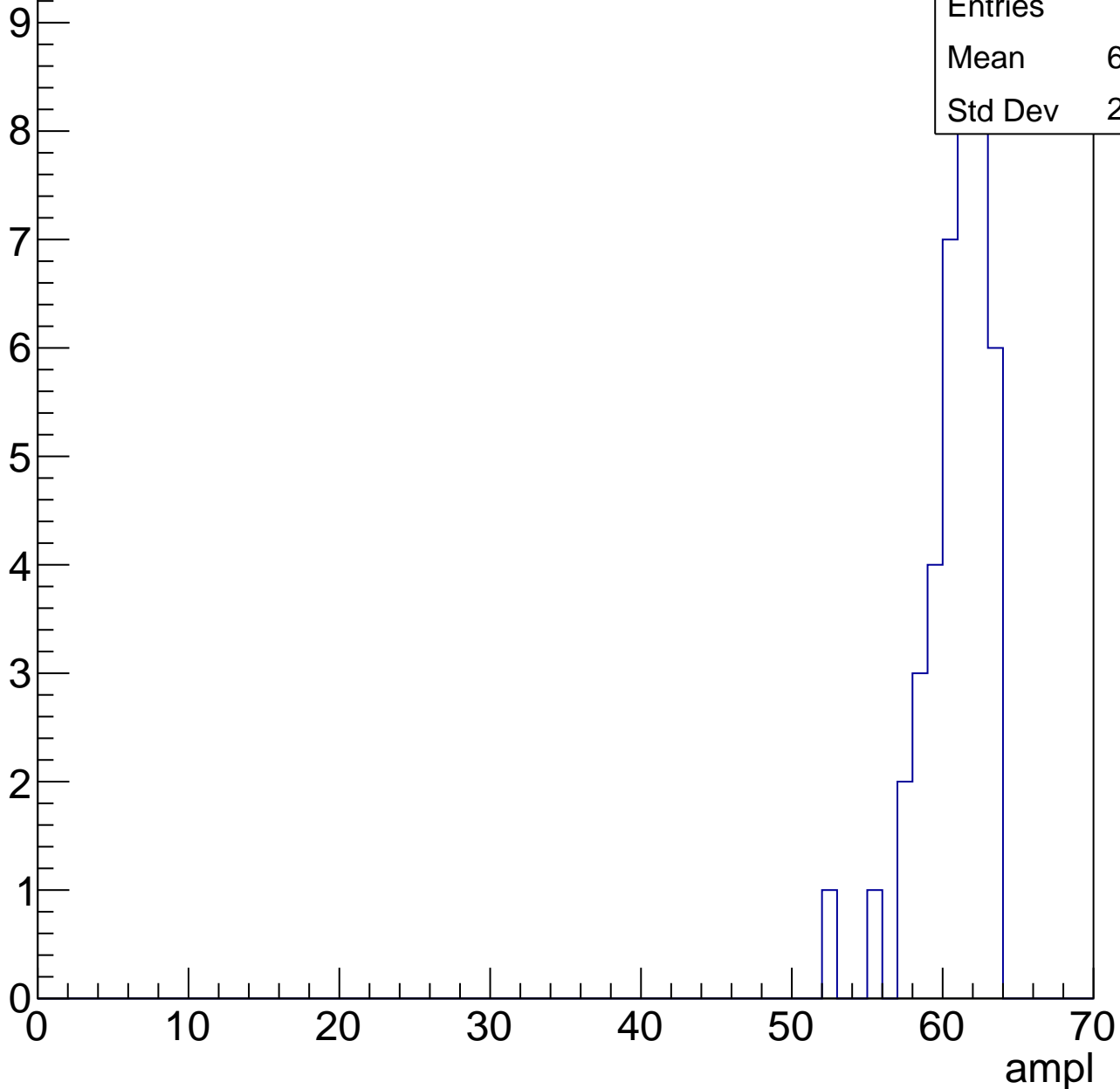


# B1L101S, U9-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	60.38
Std Dev	2.267



# B1L101S, U9-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U9-ch86, adc0

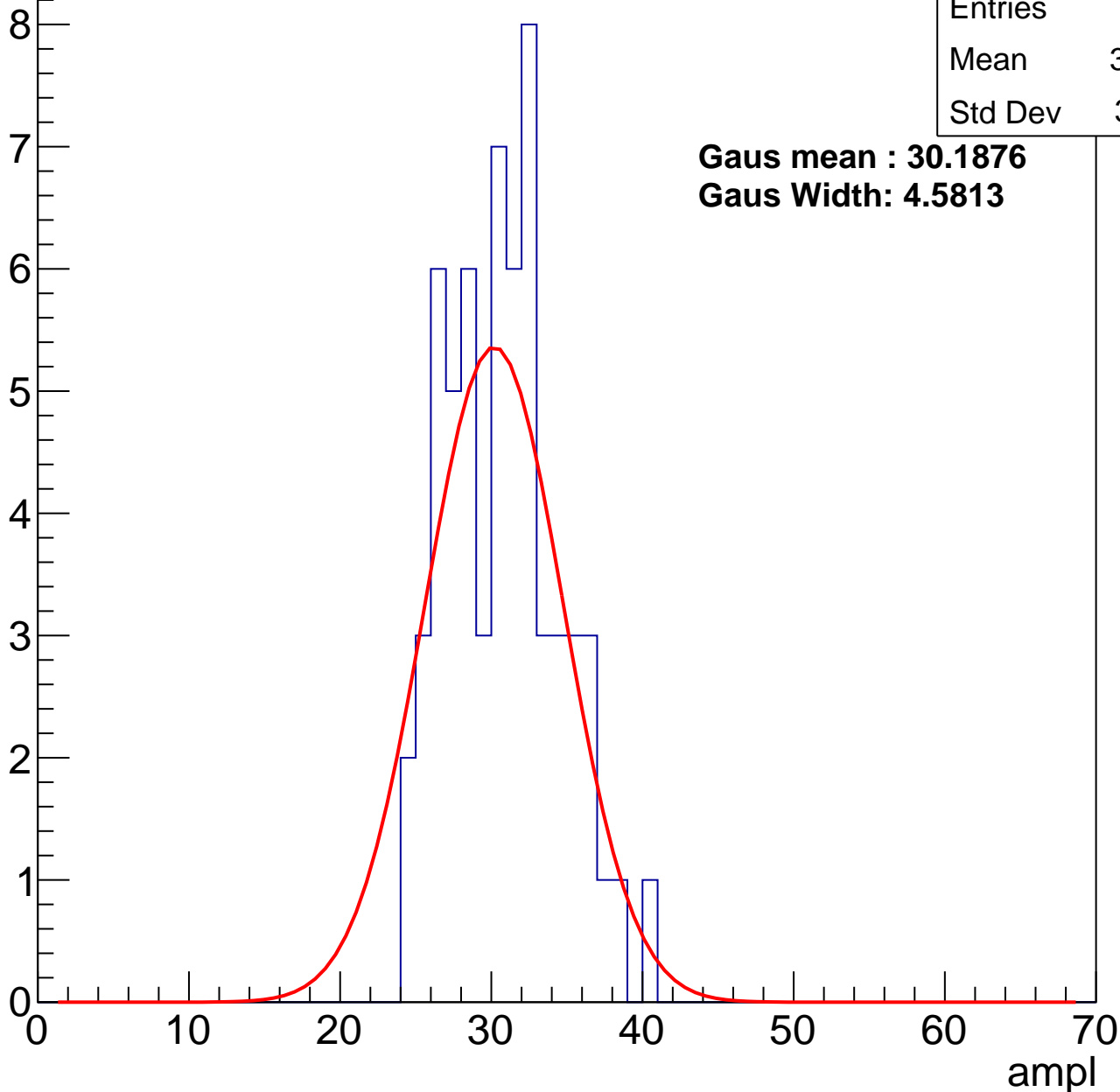
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	30.33
Std Dev	3.661

**Gaus mean : 30.1876**

**Gaus Width: 4.5813**



# B1L101S, U9-ch86, adc1

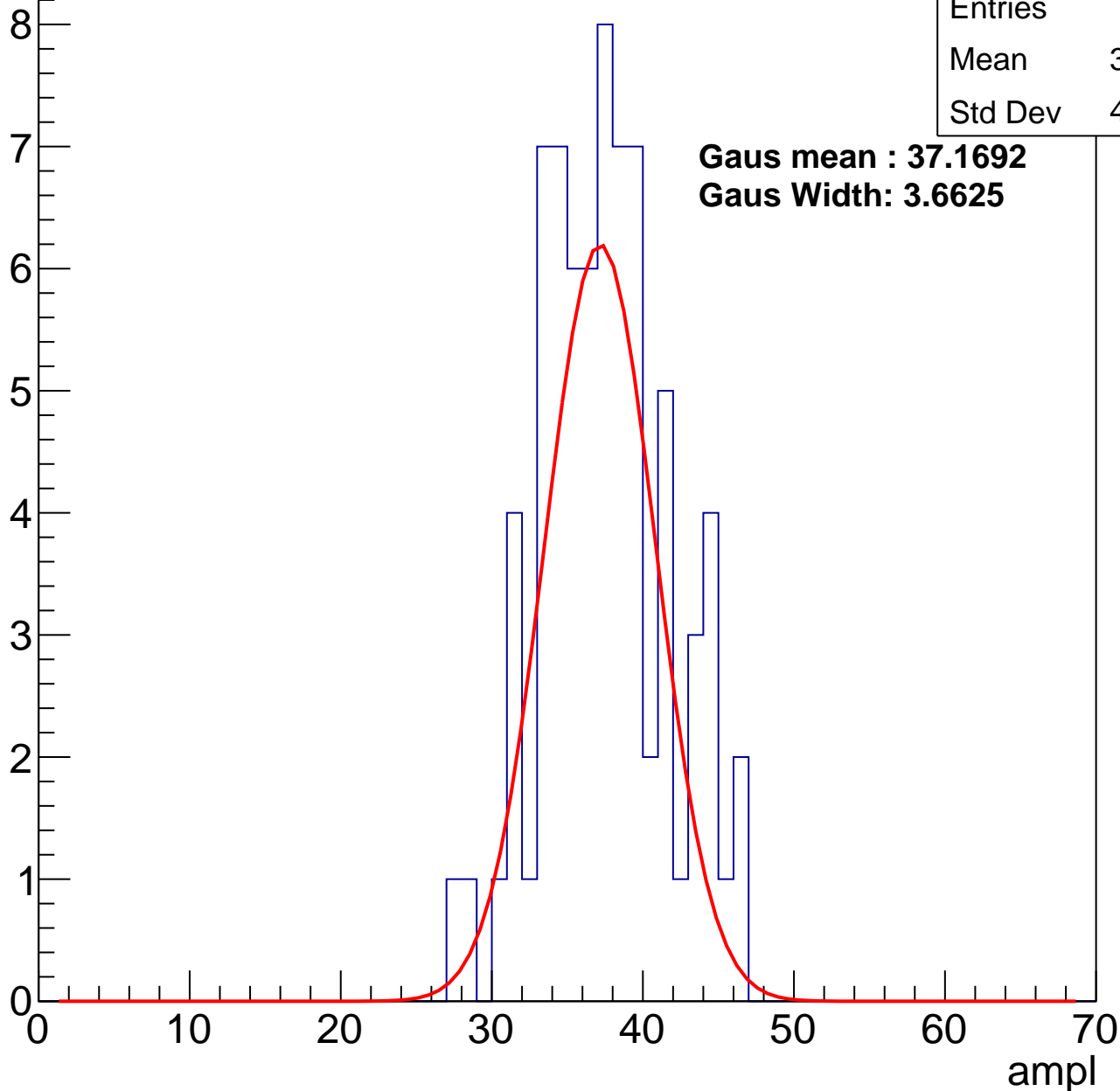
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	37.03
Std Dev	4.178

**Gaus mean : 37.1692**

**Gaus Width: 3.6625**



# B1L101S, U9-ch86, adc2

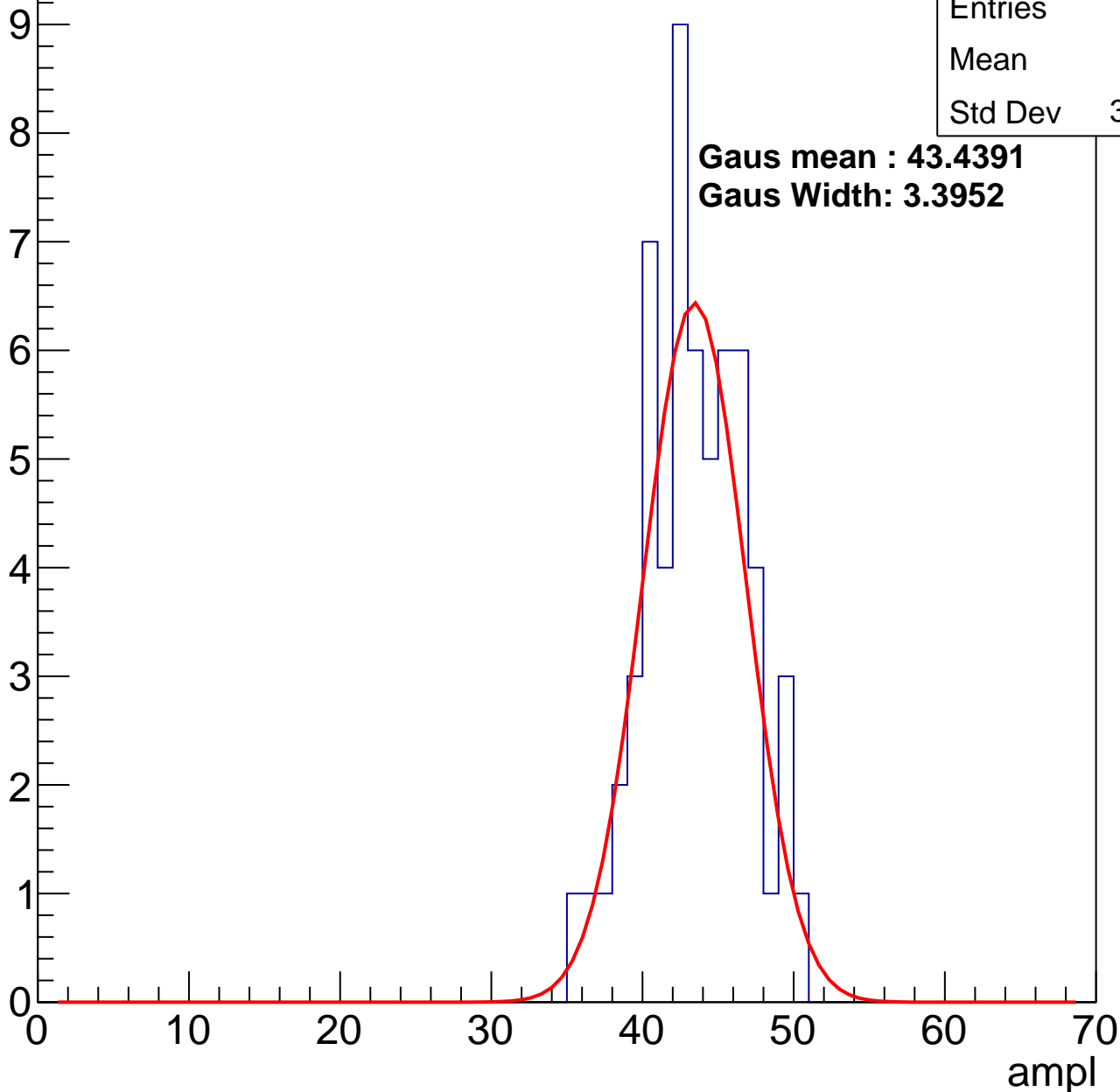
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	43
Std Dev	3.327

**Gaus mean : 43.4391**

**Gaus Width: 3.3952**

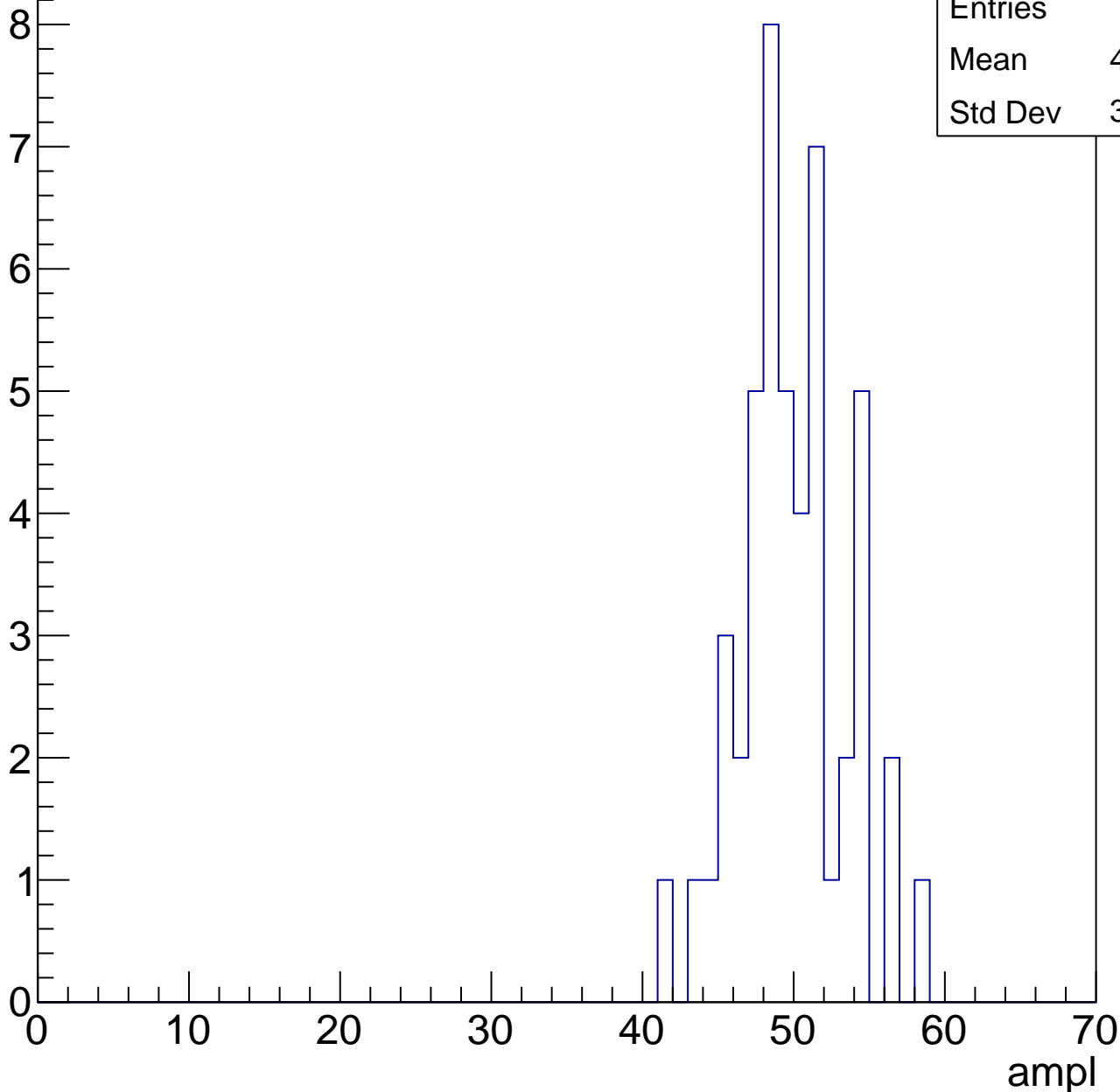


# B1L101S, U9-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

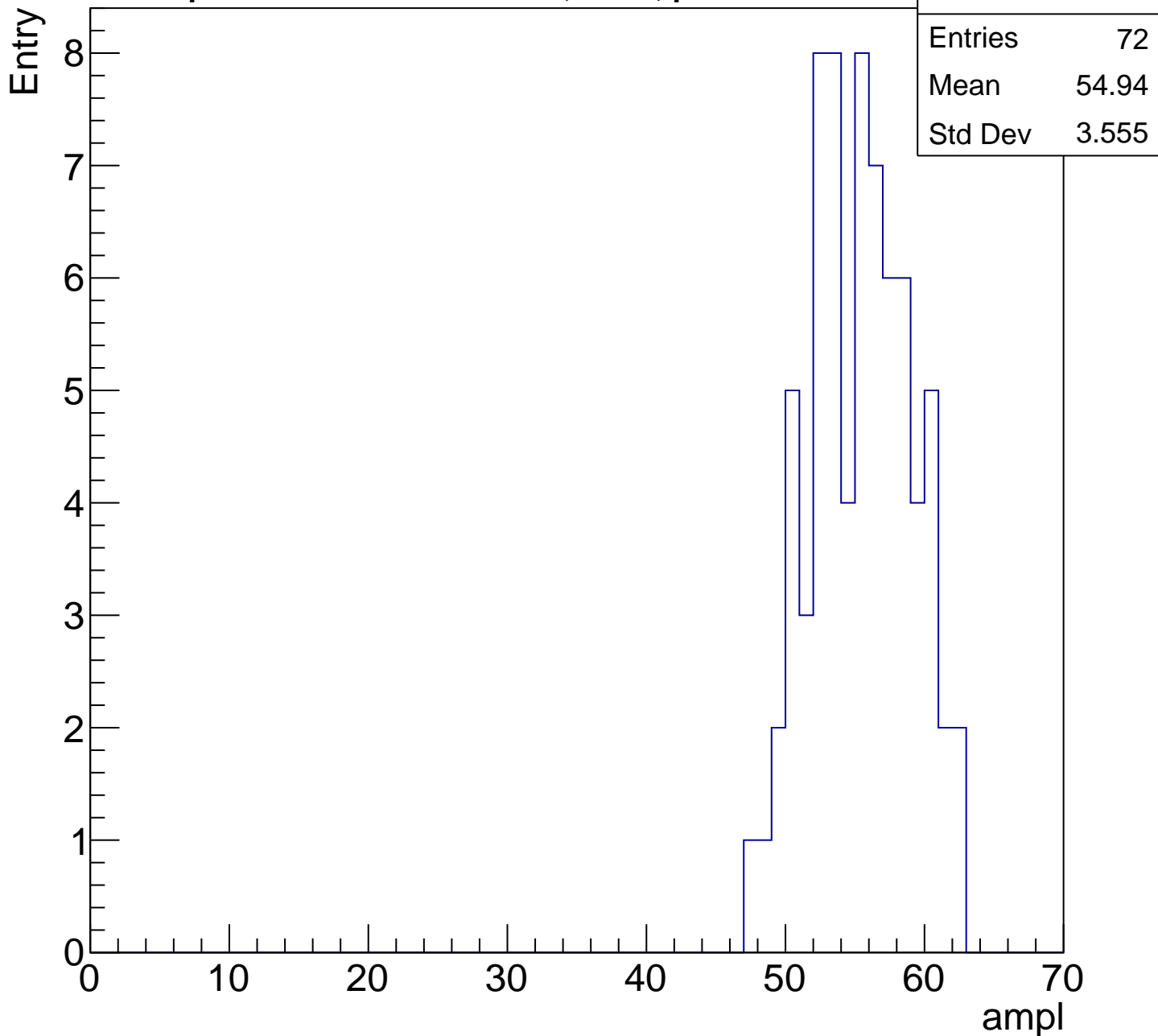
Entry

Entries	48
Mean	49.46
Std Dev	3.494



# B1L101S, U9-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

Entries	41
Mean	59.68
Std Dev	2.691

ampl

0

10

20

30

40

50

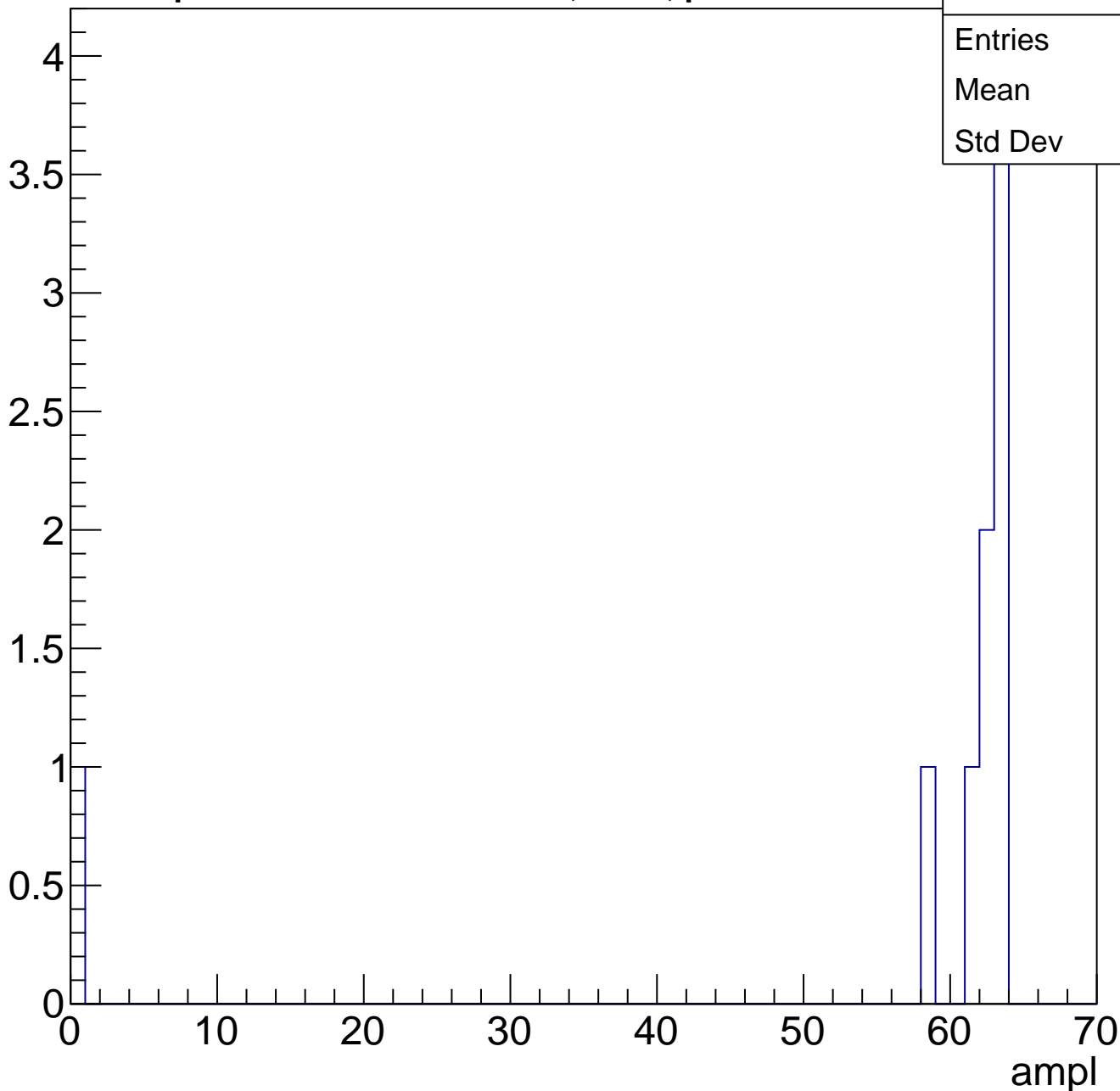
60

70

# B1L101S, U9-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	23
Std Dev	0

ampl

# B1L101S, U9-ch87, adc0

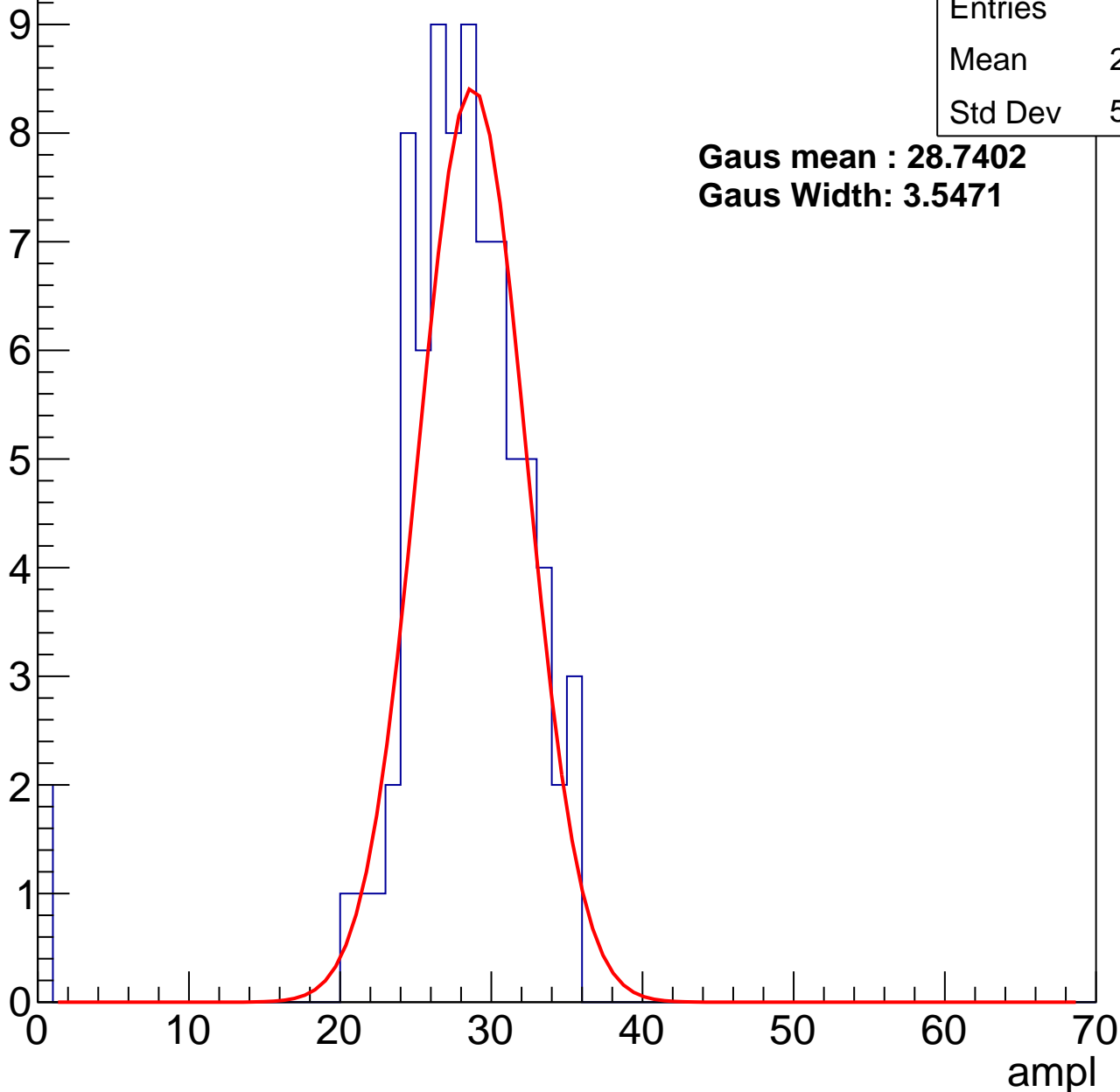
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	27.32
Std Dev	5.518

**Gaus mean : 28.7402**

**Gaus Width: 3.5471**



# B1L101S, U9-ch87, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

Entries	60
Mean	35.23
Std Dev	3.328

**Gaus mean : 35.3862**

**Gaus Width: 3.8603**

0

0

10

20

30

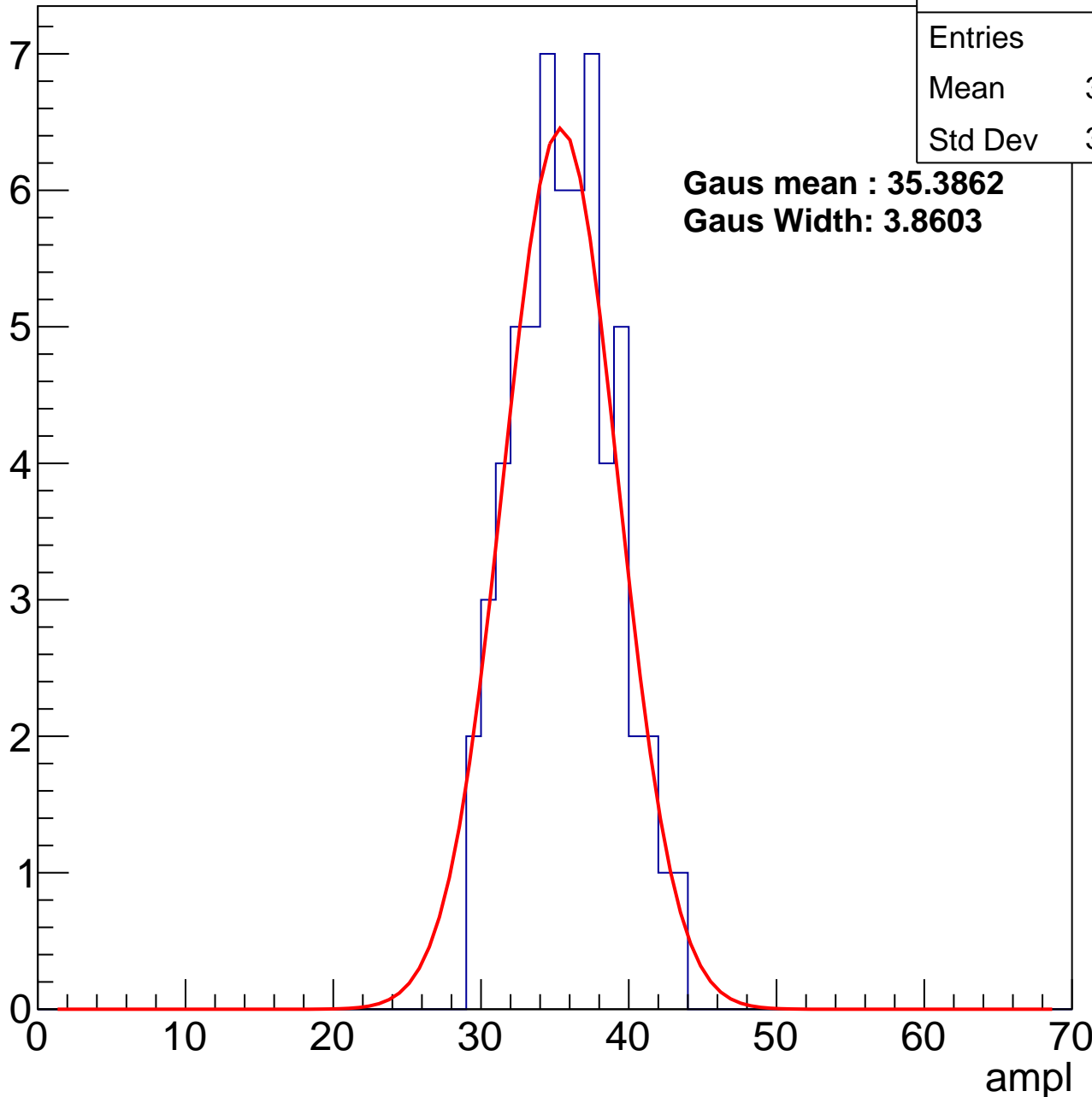
40

50

60

70

ampl



# B1L101S, U9-ch87, adc2

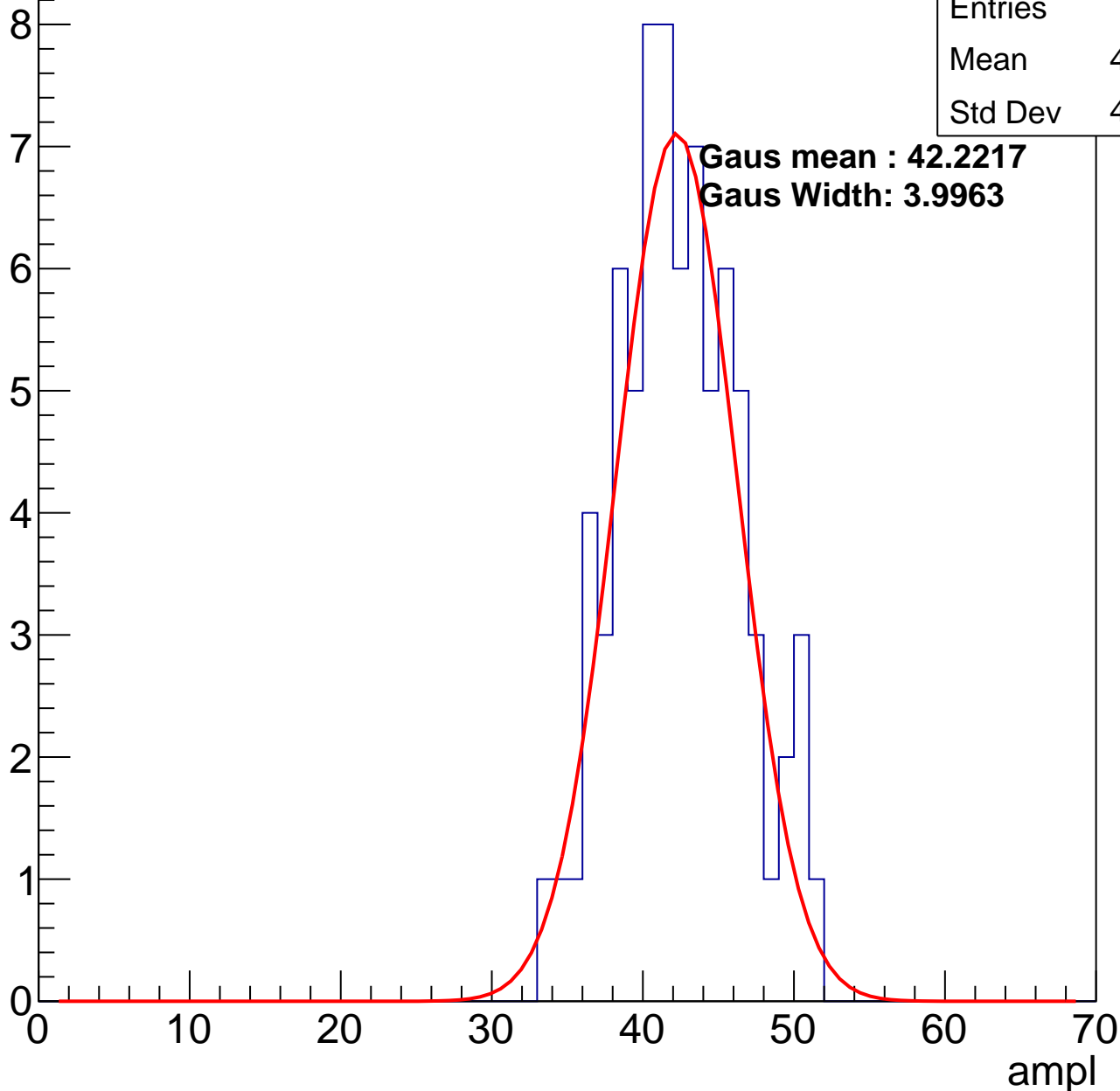
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	41.96
Std Dev	4.034

**Gaus mean : 42.2217**

**Gaus Width: 3.9963**

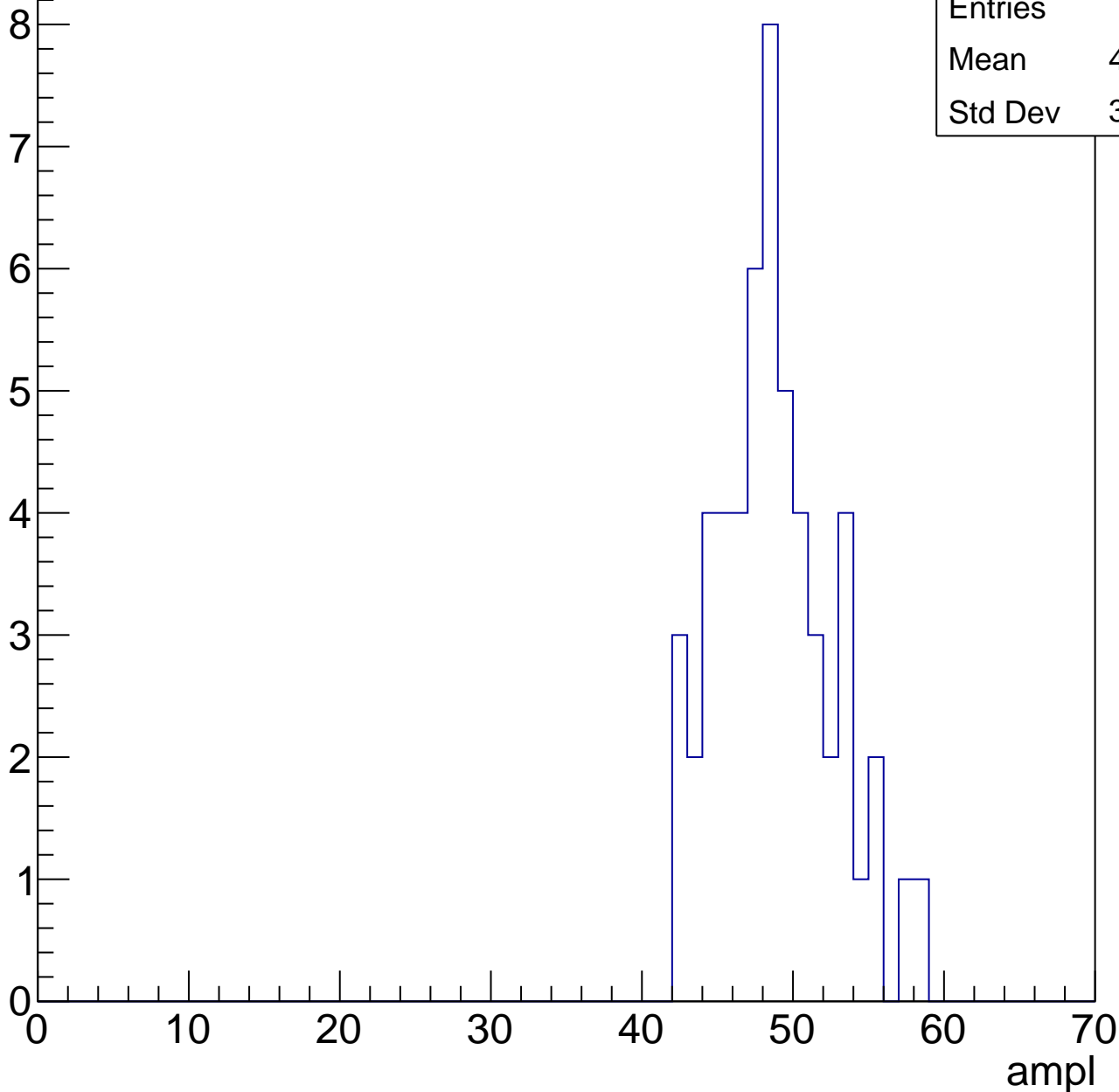


# B1L101S, U9-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	48.35
Std Dev	3.772

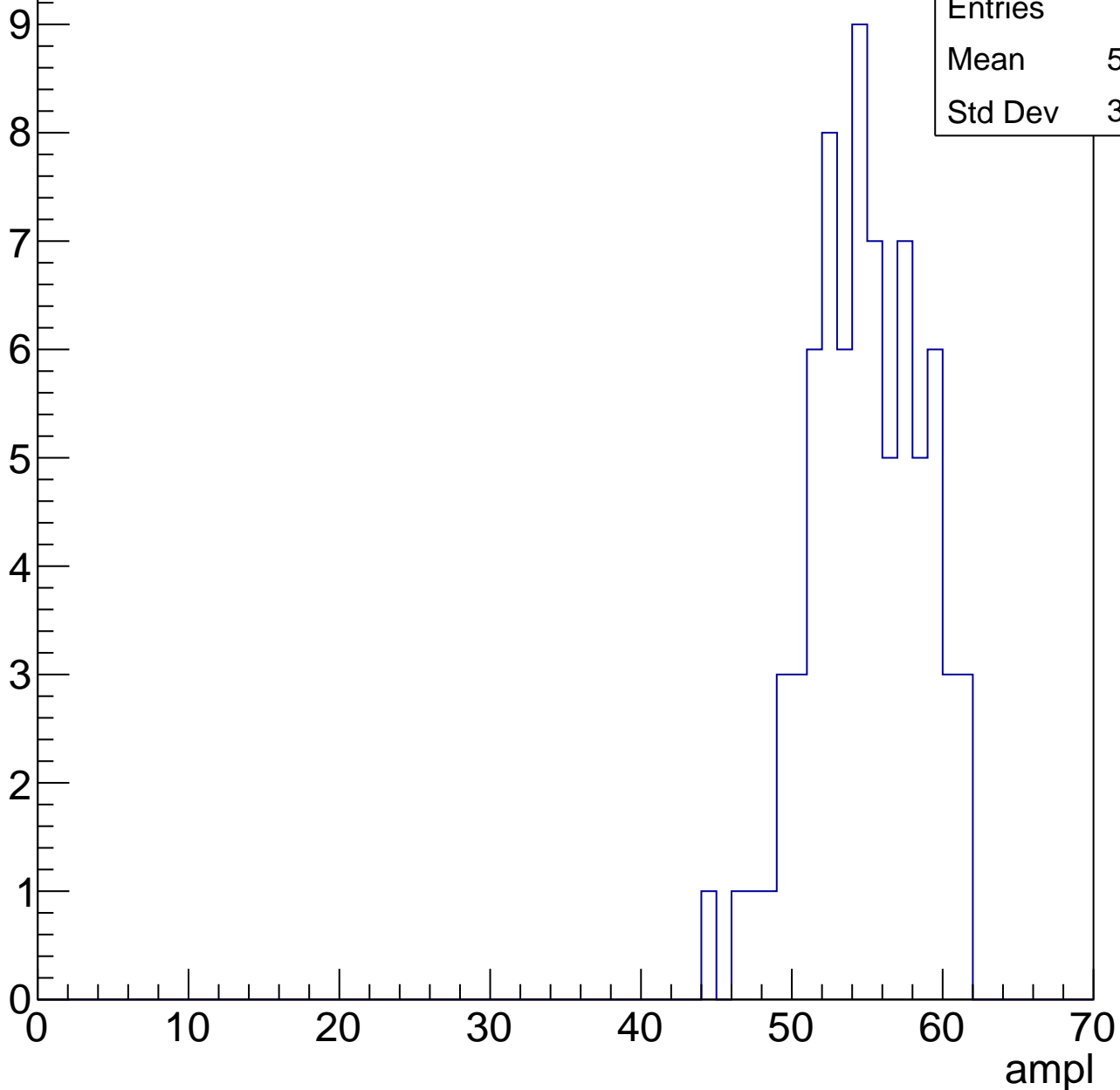


# B1L101S, U9-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	54.39
Std Dev	3.702

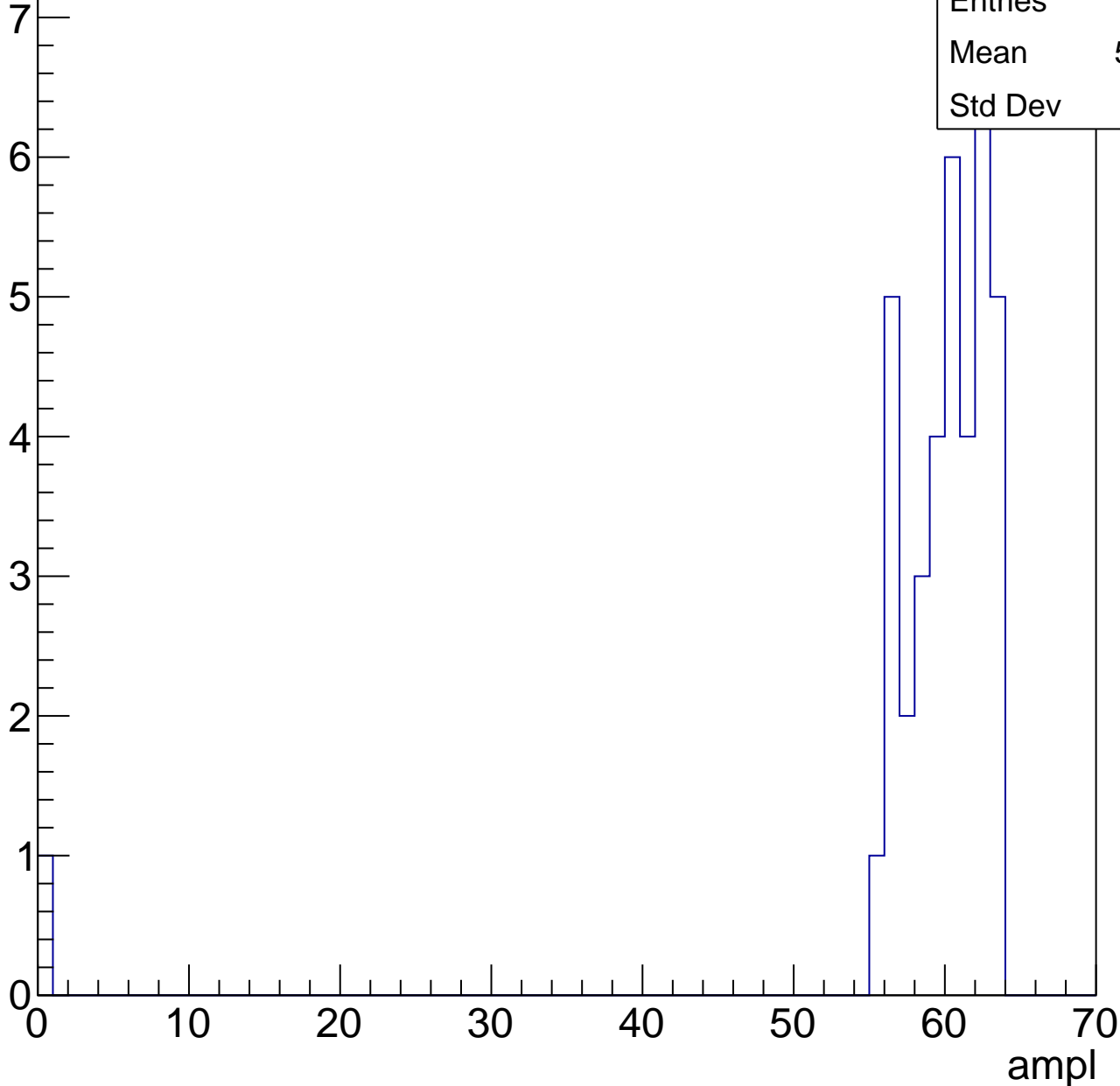


# B1L101S, U9-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	38
Mean	58.21
Std Dev	9.86

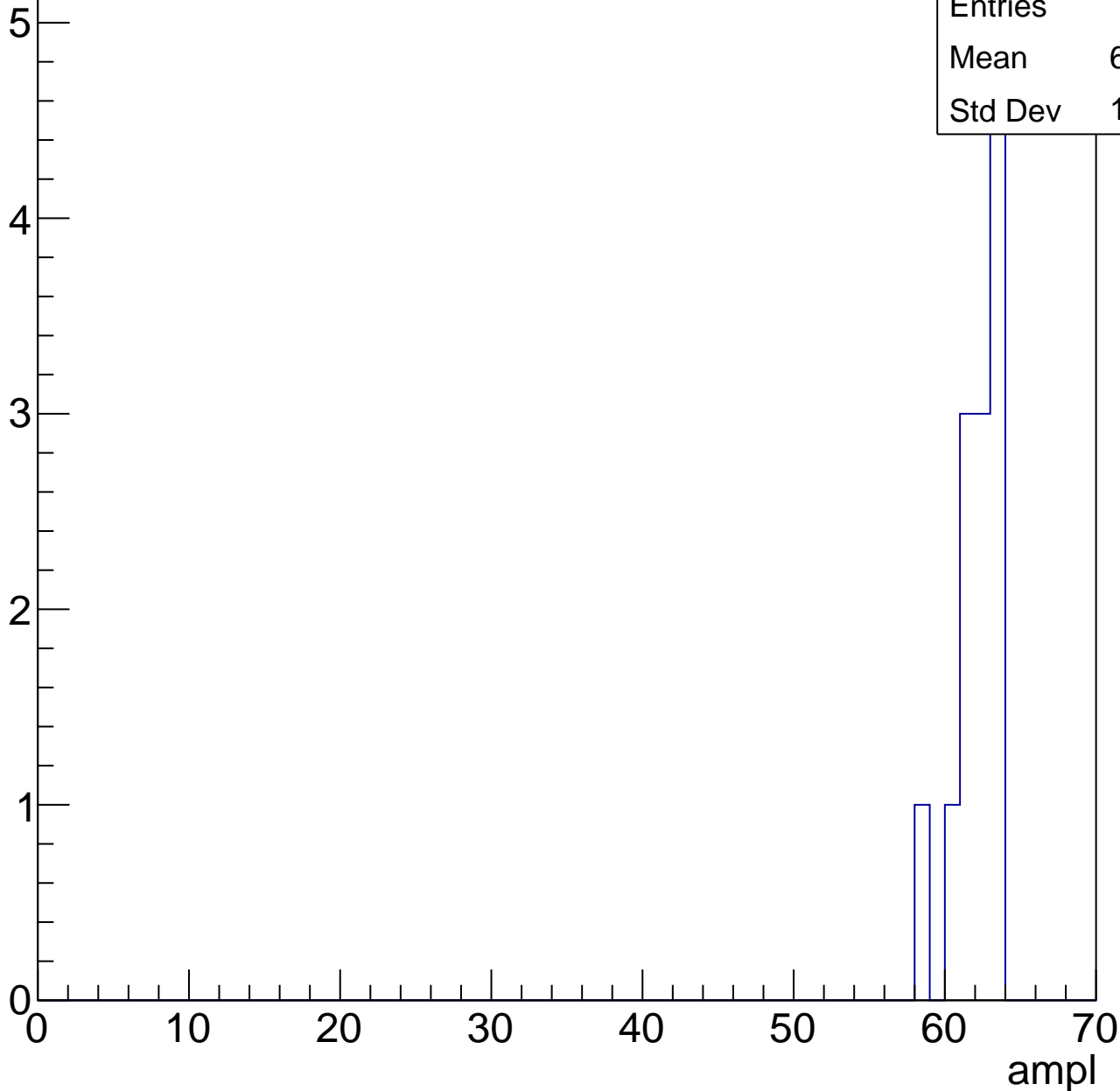


# B1L101S, U9-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	13
Mean	61.69
Std Dev	1.435





# B1L101S, U9-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

5

4

3

2

1

0

0

10

20

30

40

50

60

70

ampl

Entries

5

Mean

0

Std Dev

0

# B1L101S, U9-ch88, adc0

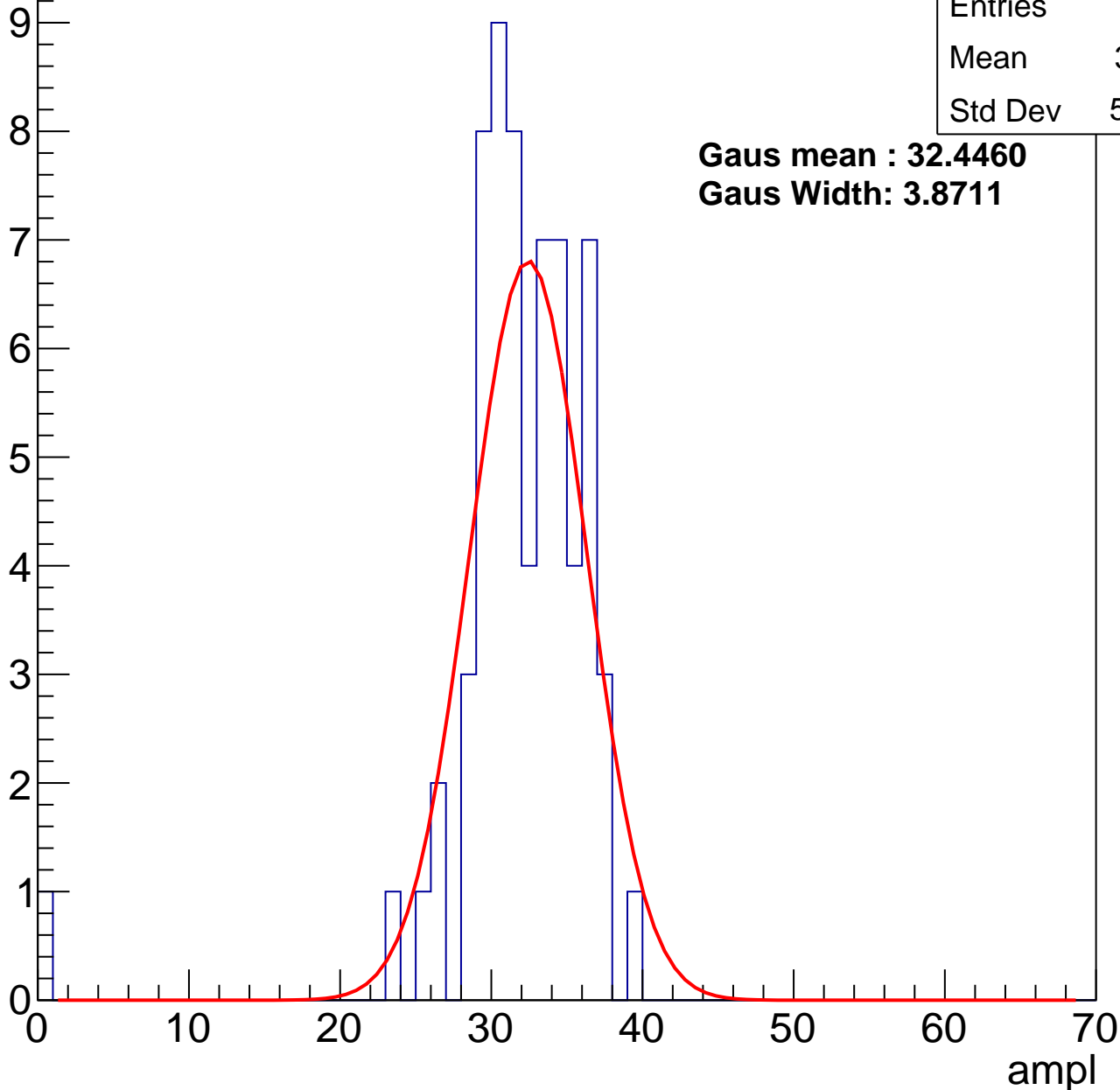
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	31.41
Std Dev	5.036

**Gaus mean : 32.4460**

**Gaus Width: 3.8711**



# B1L101S, U9-ch88, adc1

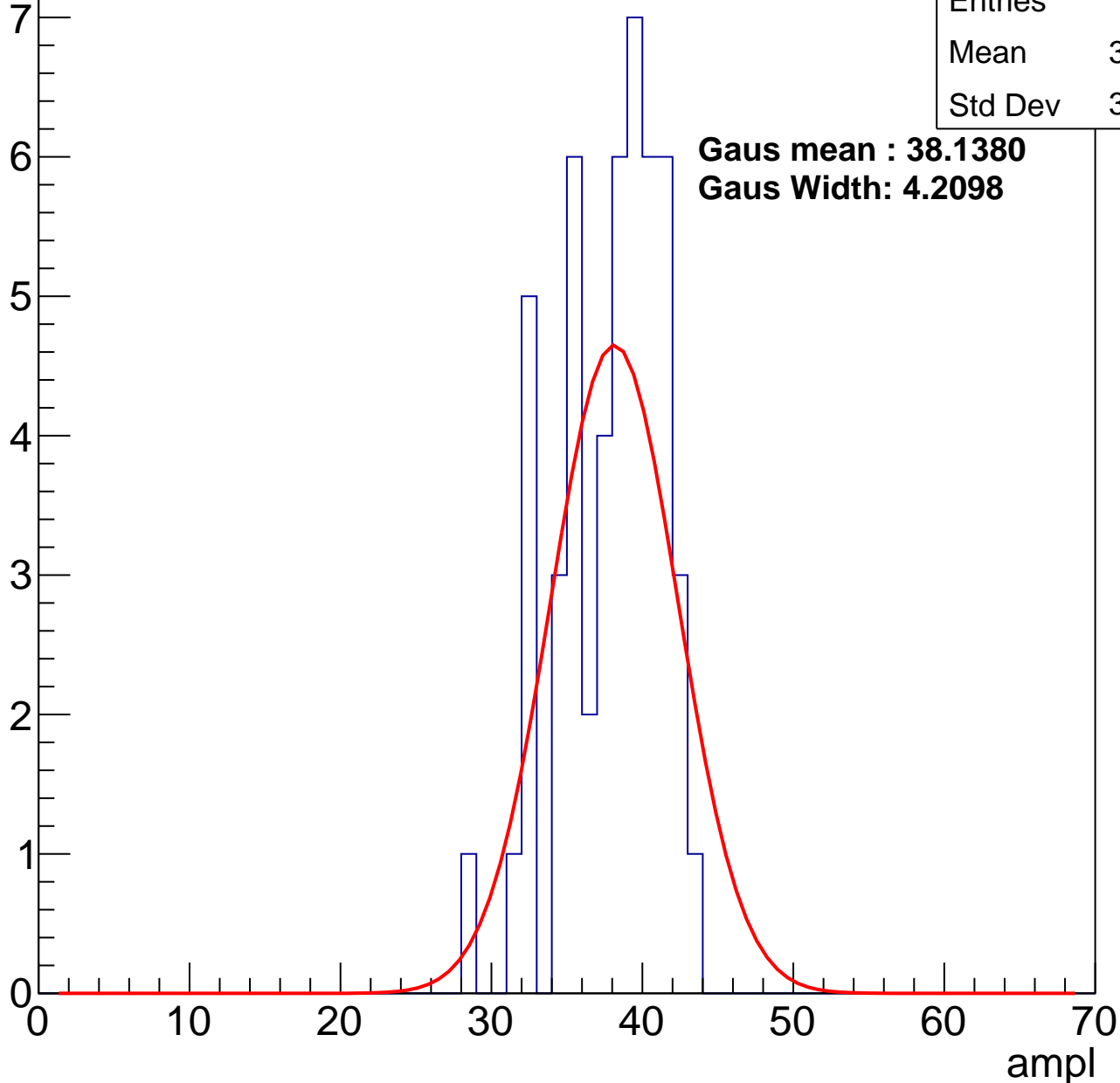
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	37.39
Std Dev	3.379

**Gaus mean : 38.1380**

**Gaus Width: 4.2098**



# B1L101S, U9-ch88, adc2

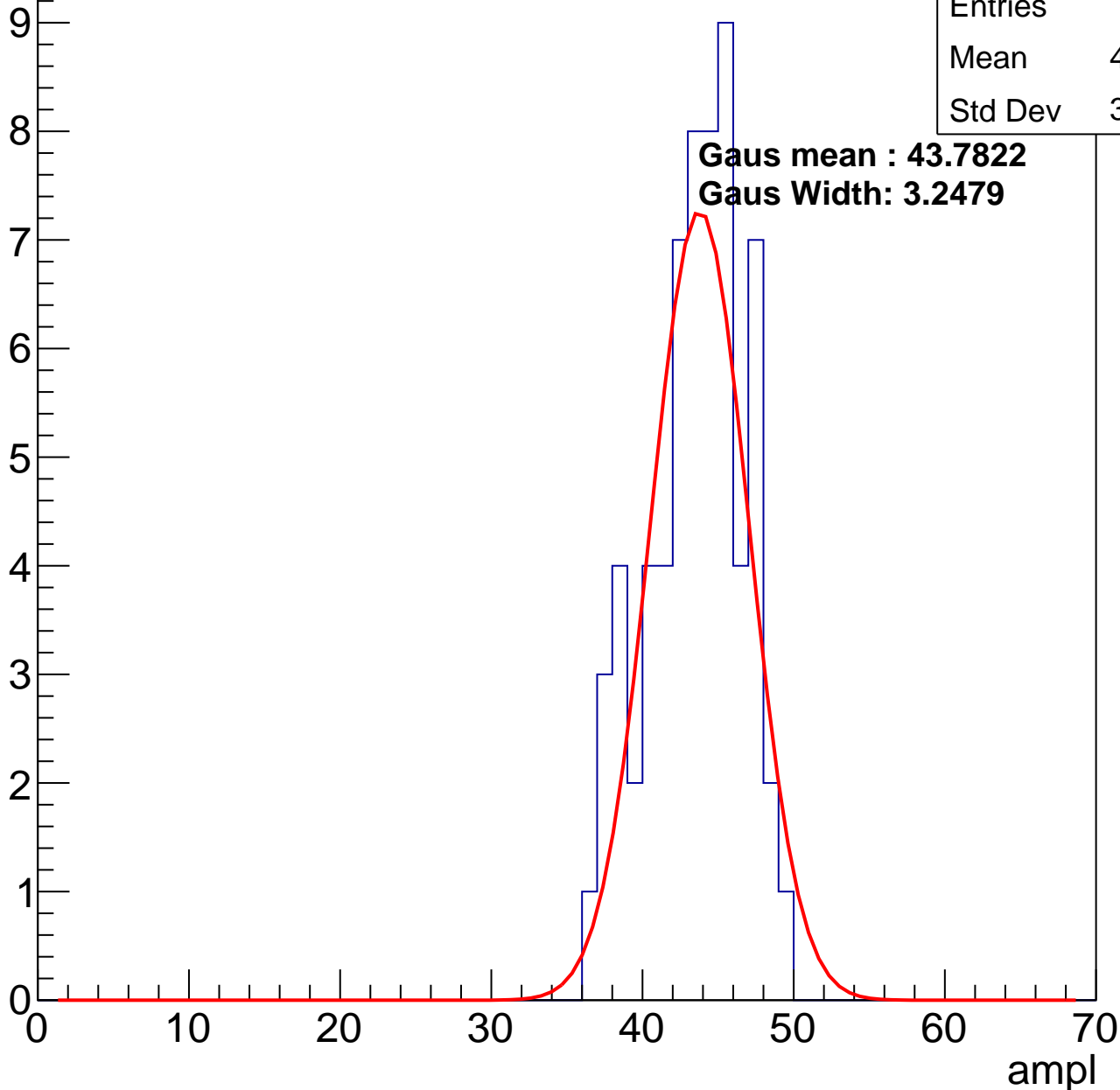
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	43.03
Std Dev	3.127

**Gaus mean : 43.7822**

**Gaus Width: 3.2479**

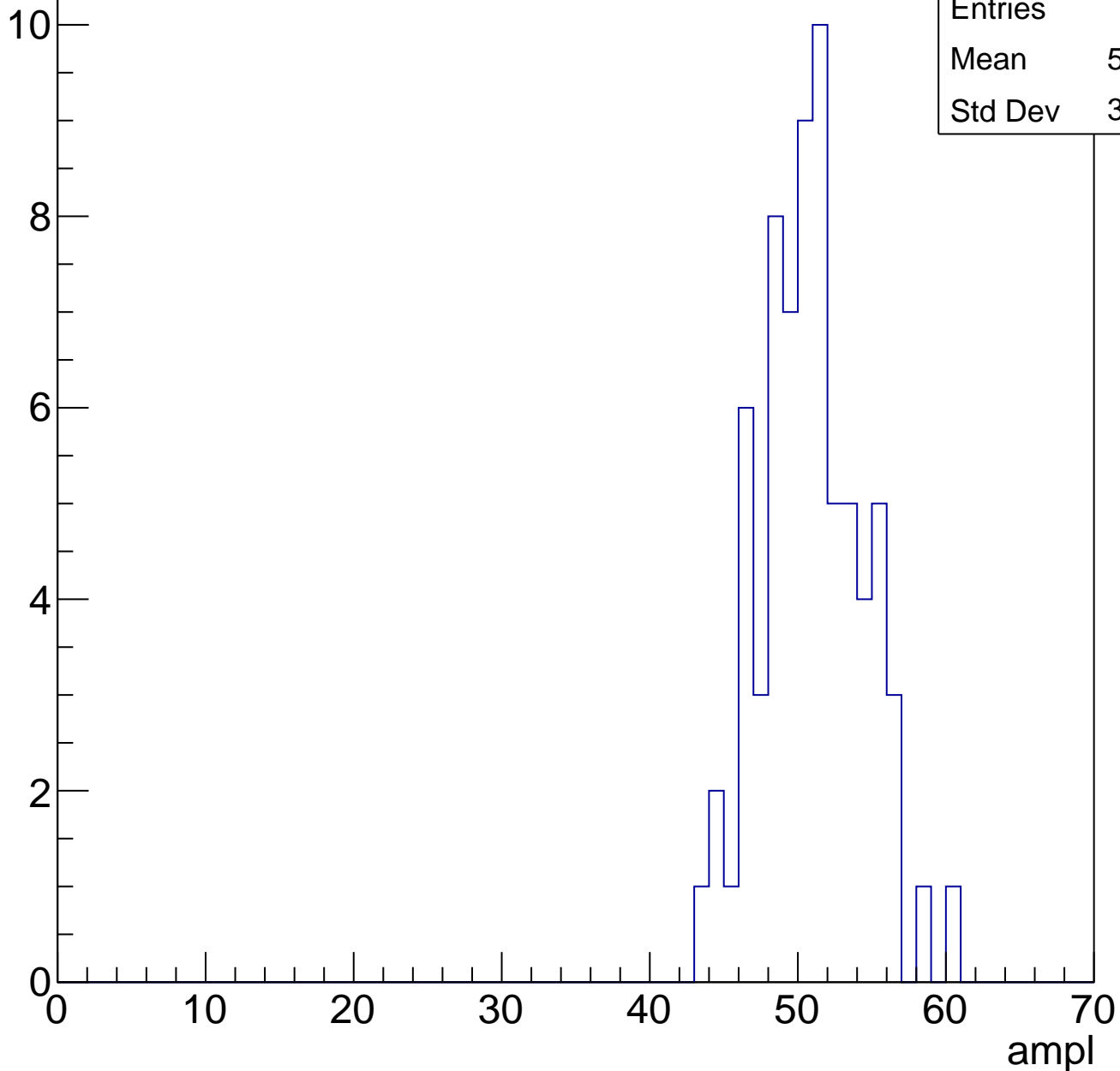


# B1L101S, U9-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	71
Mean	50.45
Std Dev	3.418

Entry

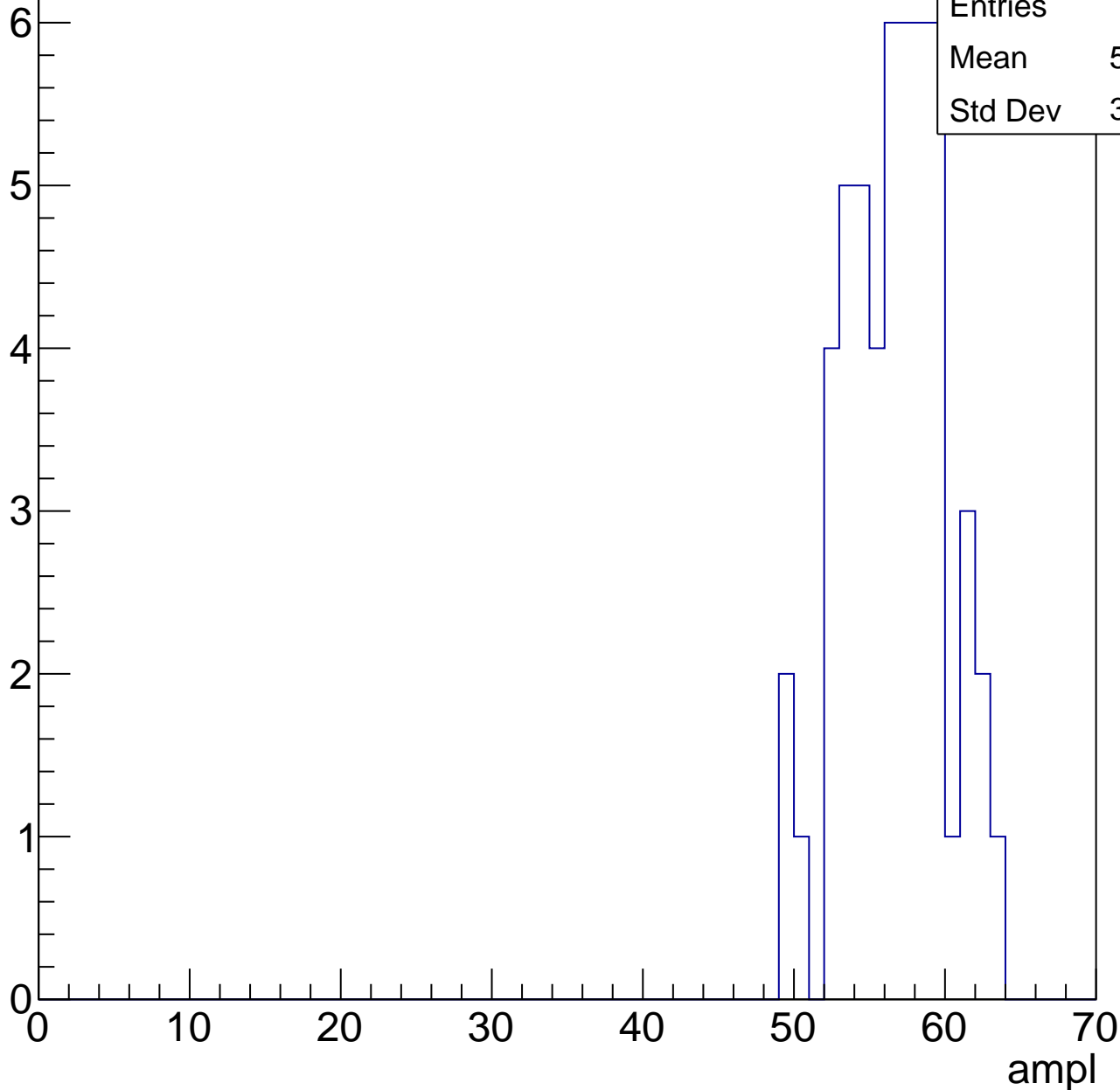


# B1L101S, U9-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

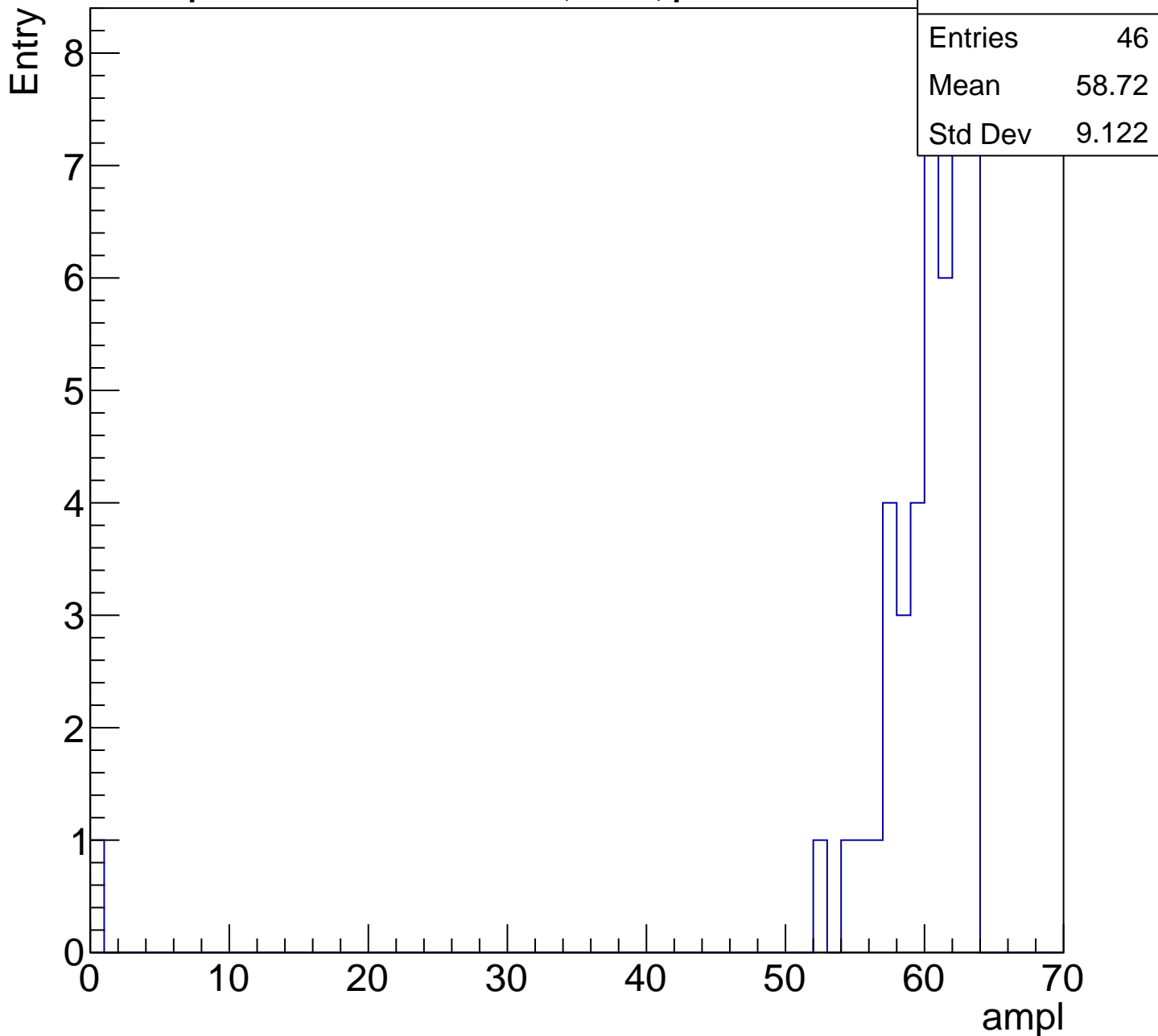
Entry

Entries	52
Mean	56.17
Std Dev	3.286



# B1L101S, U9-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch89, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	77
Mean	30.16
Std Dev	3.647

**Gaus mean : 30.2169**

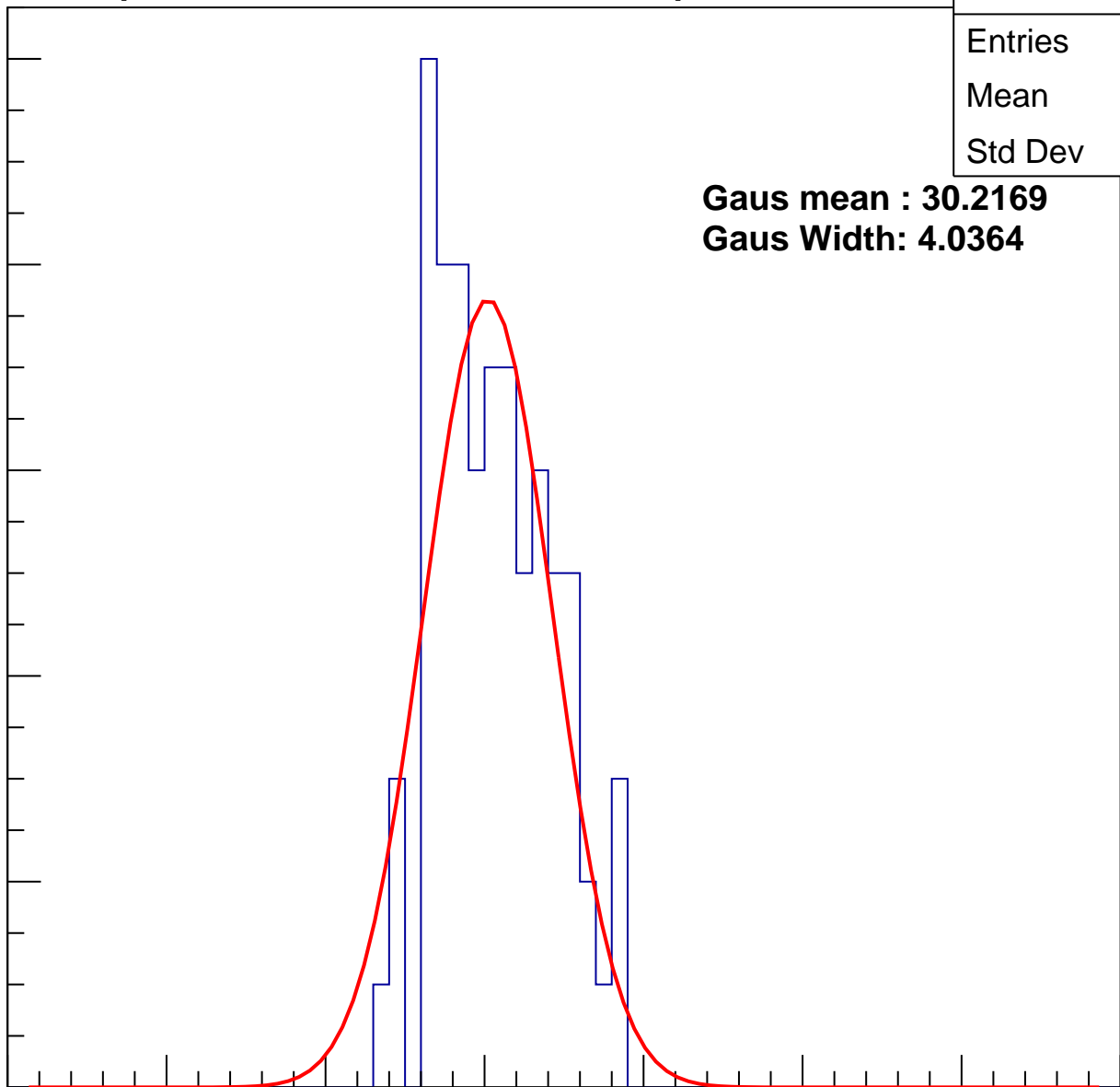
**Gaus Width: 4.0364**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U9-ch89, adc1

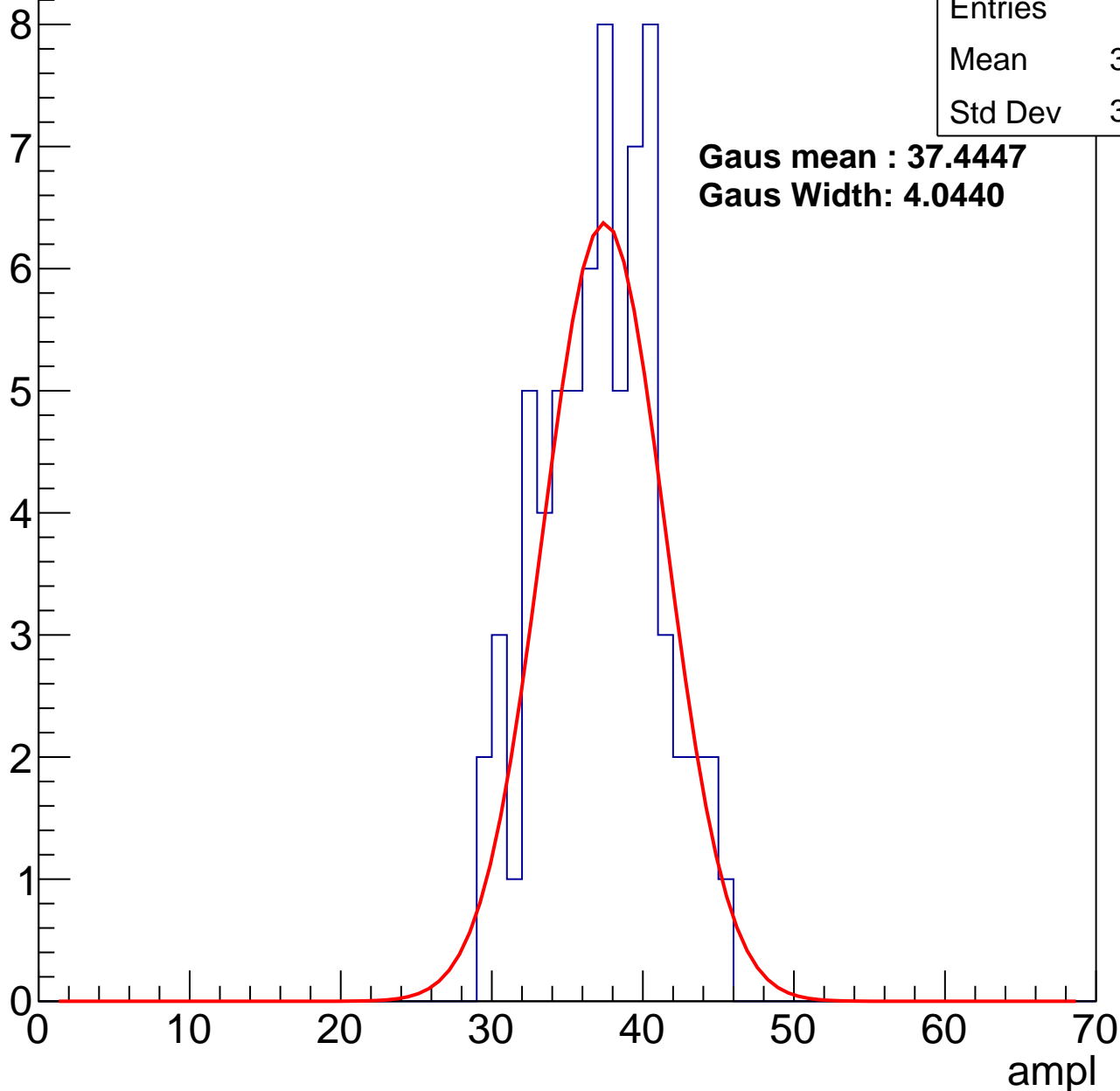
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	36.77
Std Dev	3.815

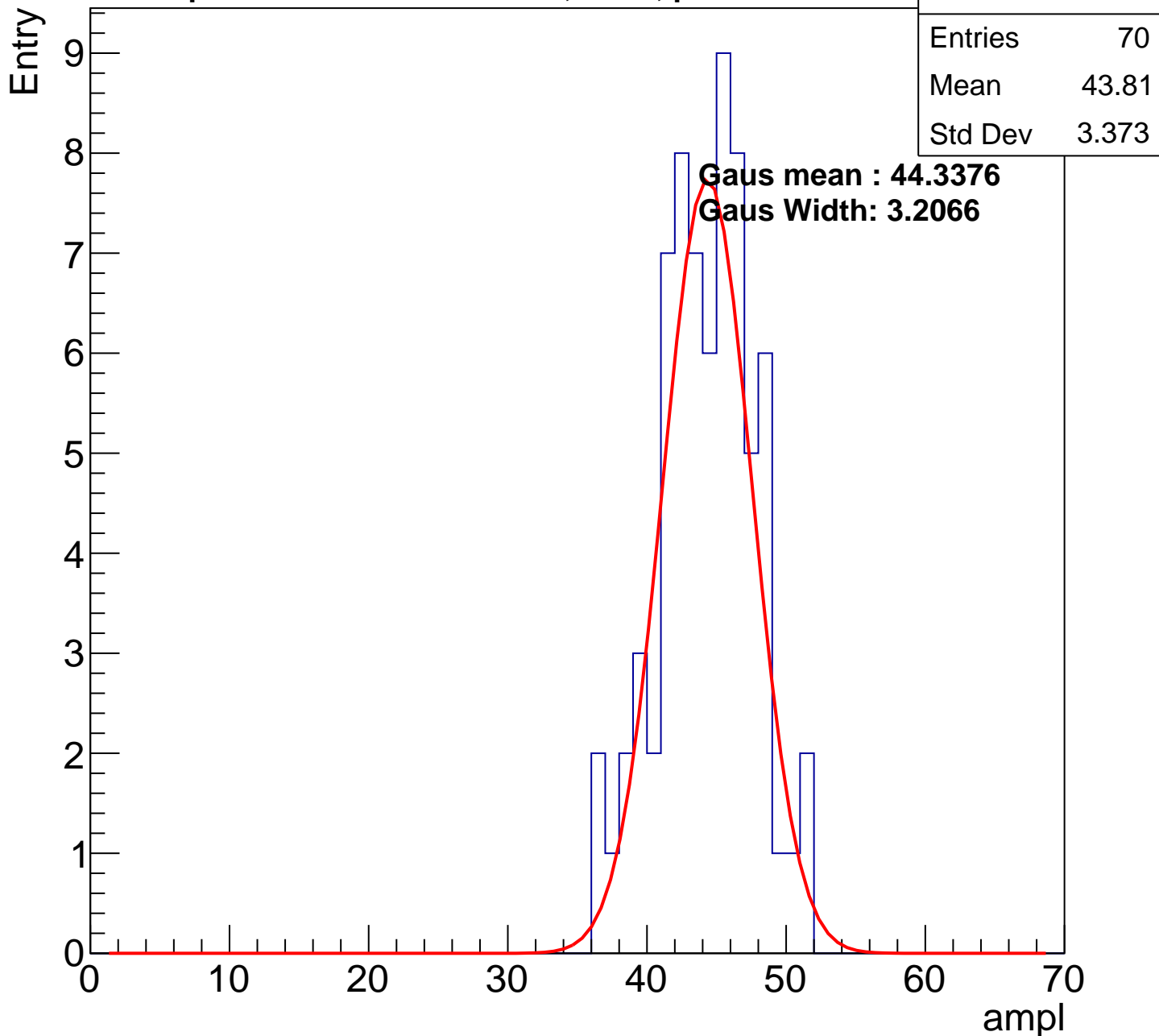
**Gaus mean : 37.4447**

**Gaus Width: 4.0440**



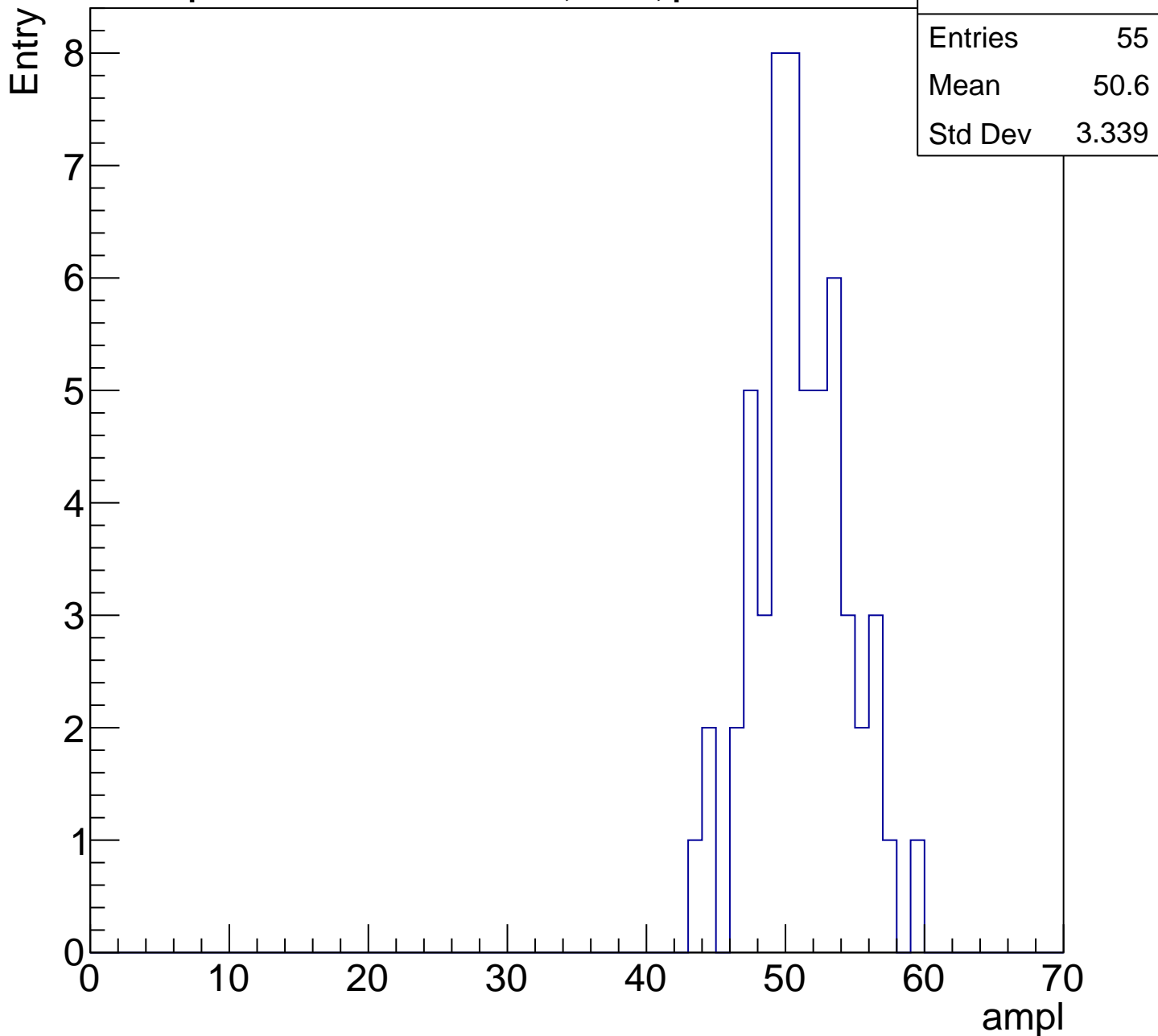
# B1L101S, U9-ch89, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

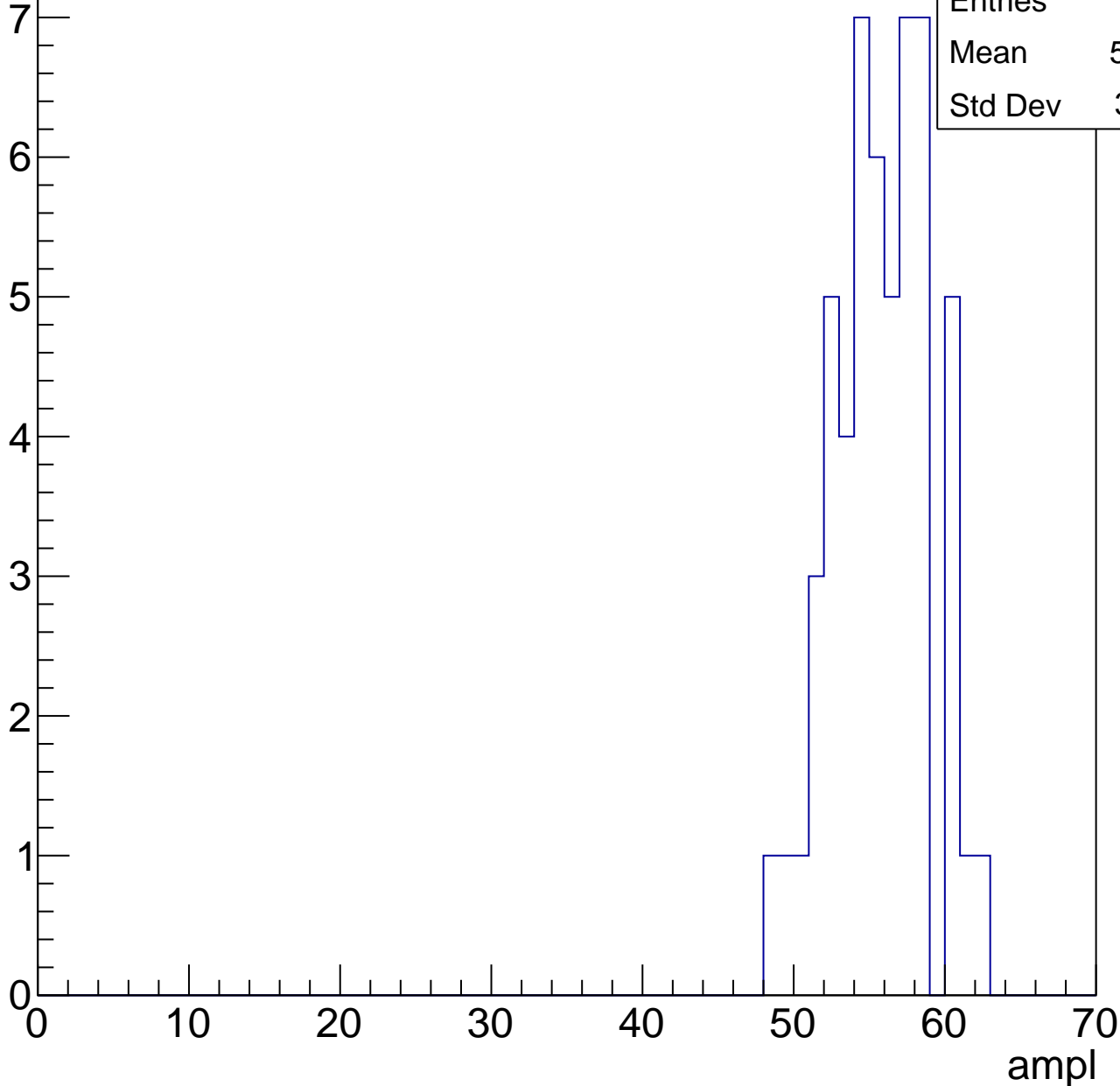


# B1L101S, U9-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

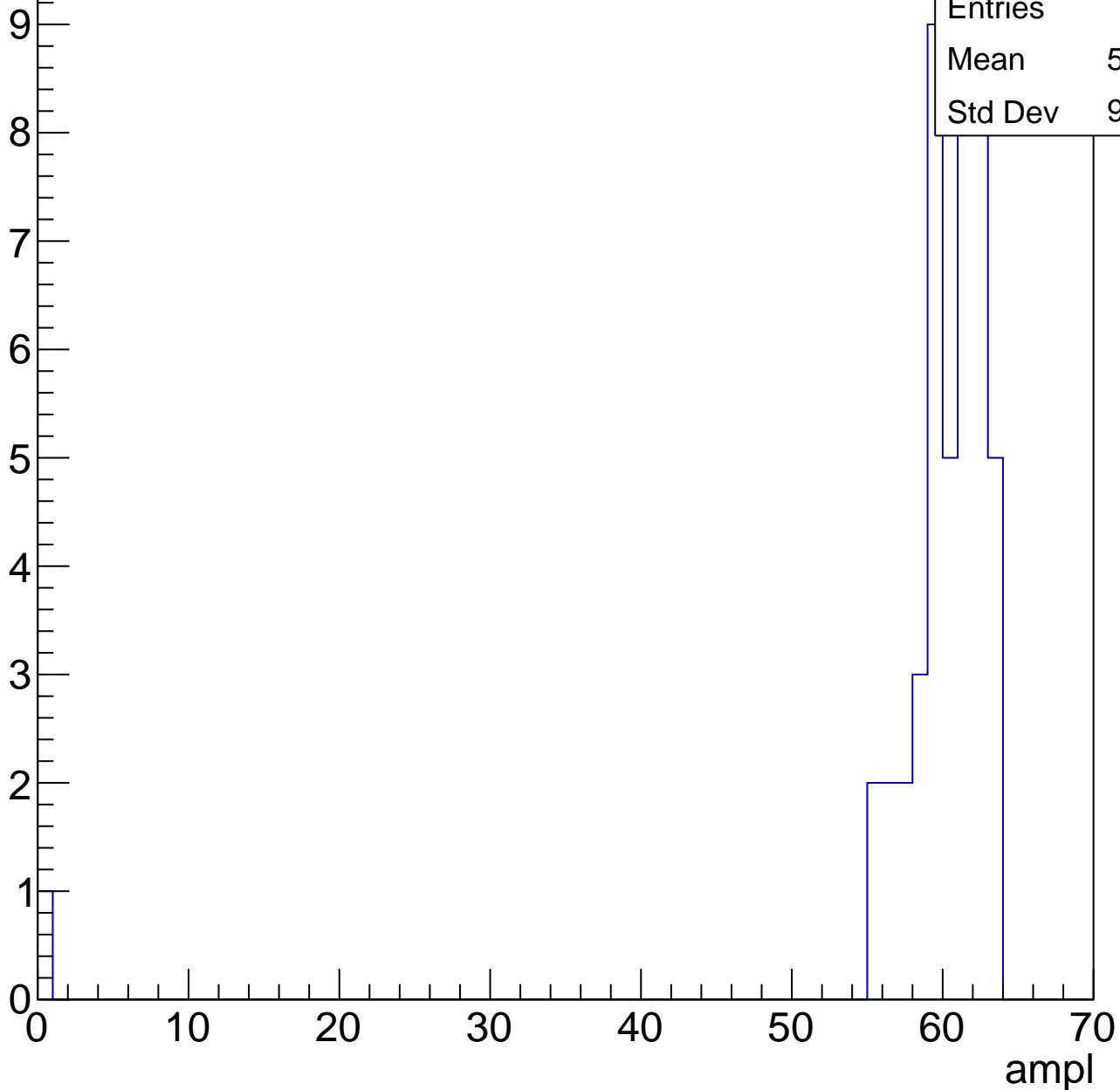
Entries	54
Mean	55.33
Std Dev	3.121



# B1L101S, U9-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

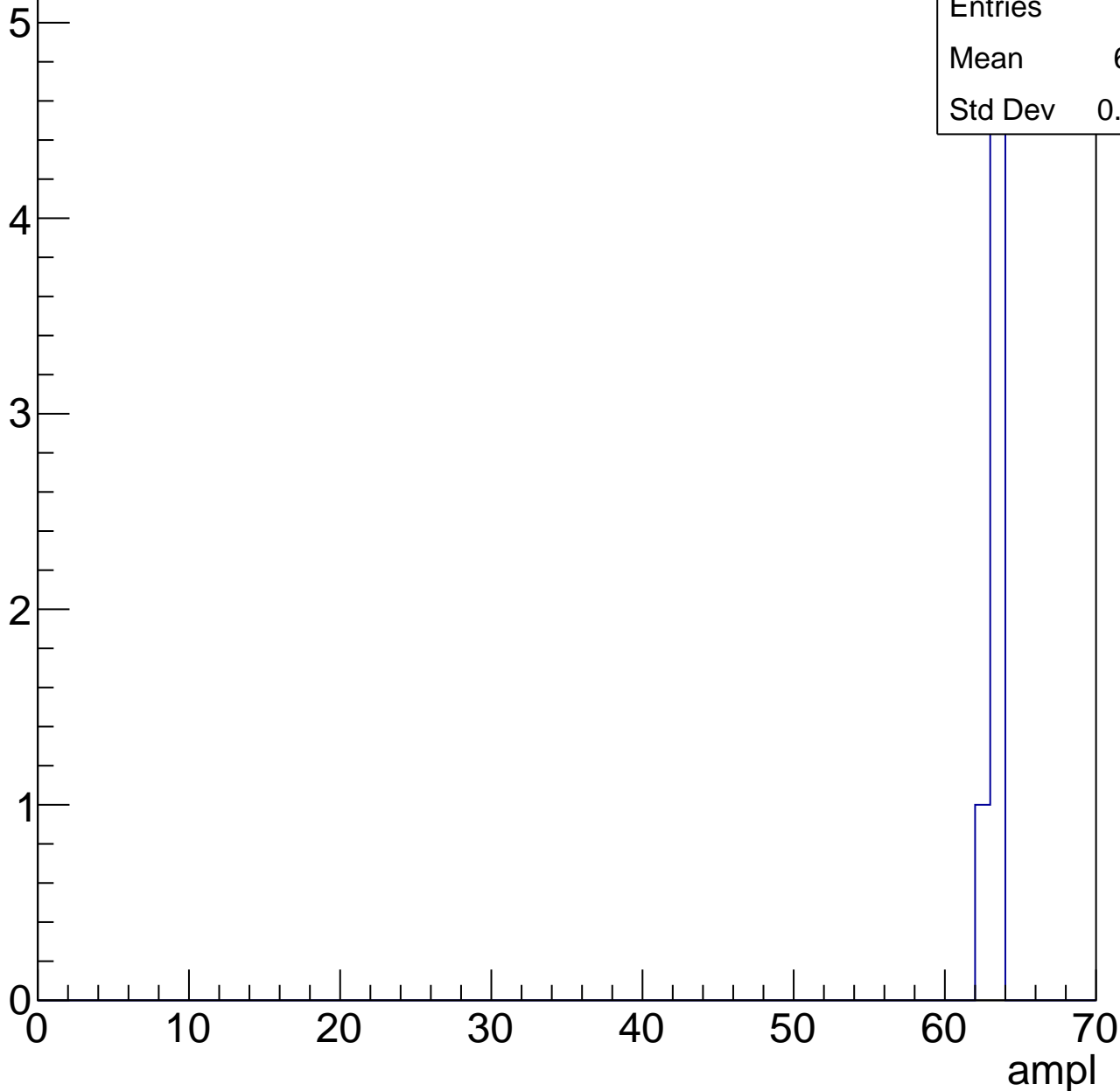


# B1L101S, U9-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	6
Mean	62.83
Std Dev	0.3727





# B1L101S, U9-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch90, adc0

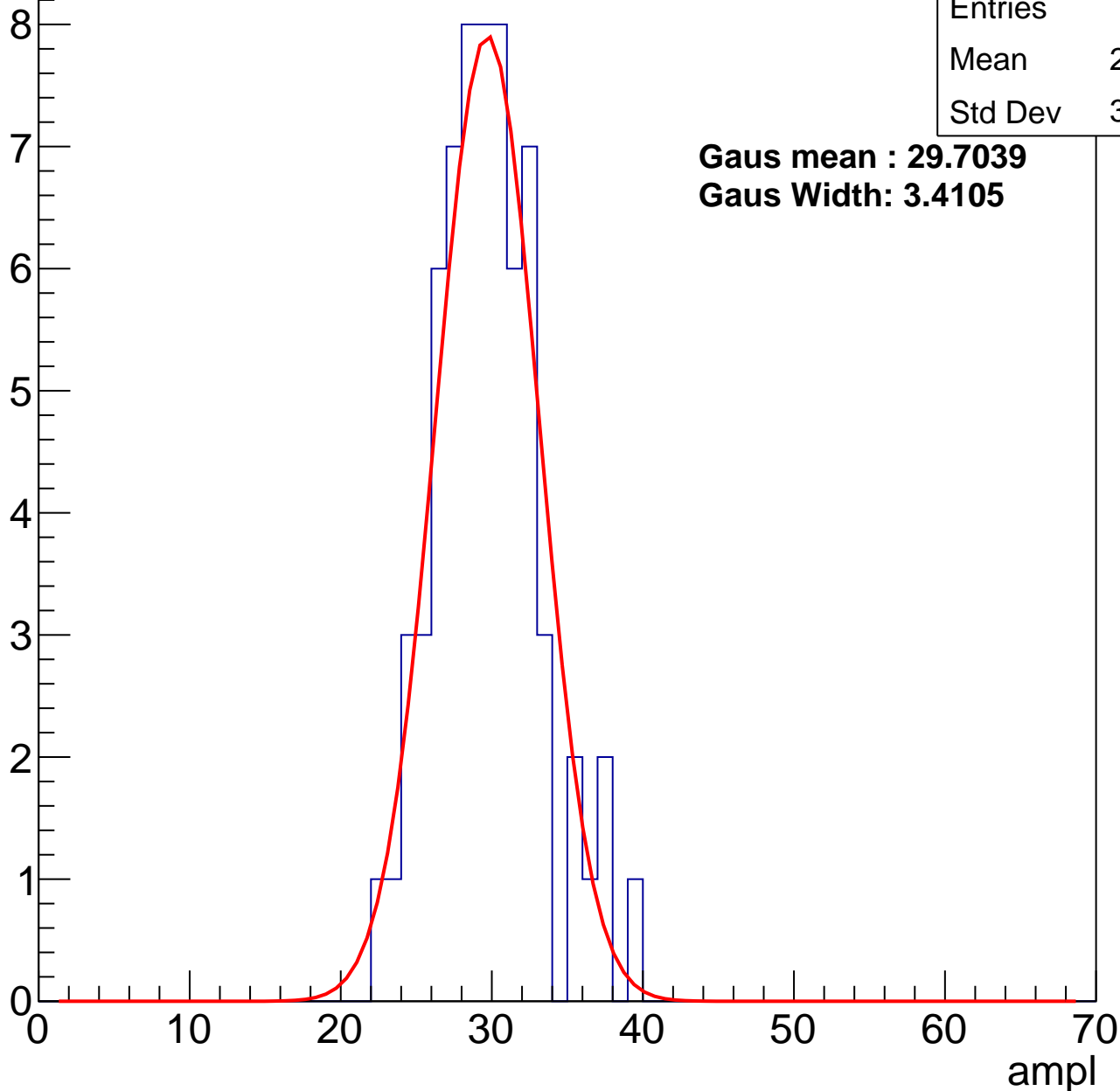
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	29.27
Std Dev	3.423

**Gaus mean : 29.7039**

**Gaus Width: 3.4105**



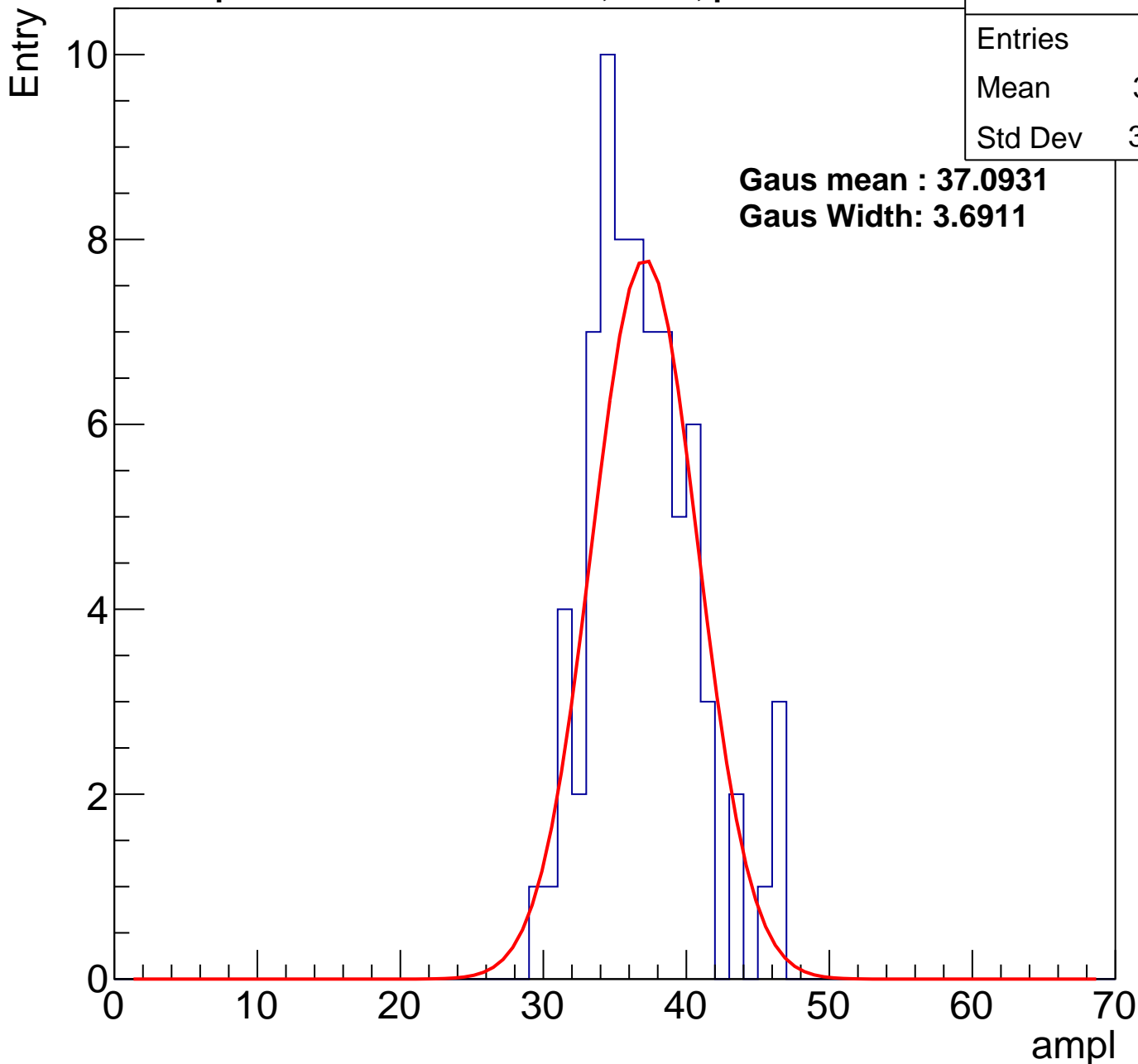
# B1L101S, U9-ch90, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	75
Mean	36.51
Std Dev	3.722

**Gaus mean : 37.0931**

**Gaus Width: 3.6911**



# B1L101S, U9-ch90, adc2

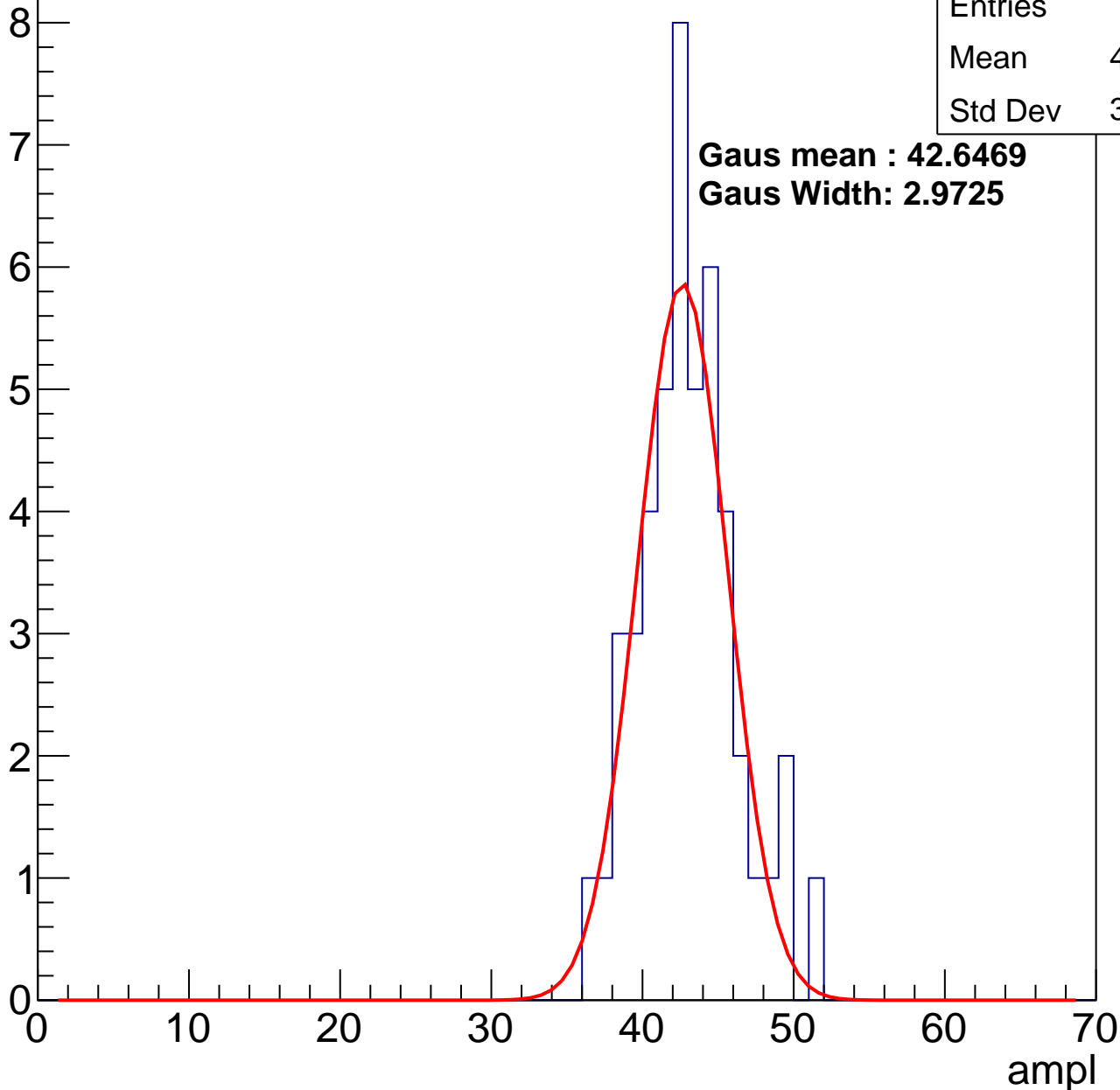
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	42.55
Std Dev	3.194

**Gaus mean : 42.6469**

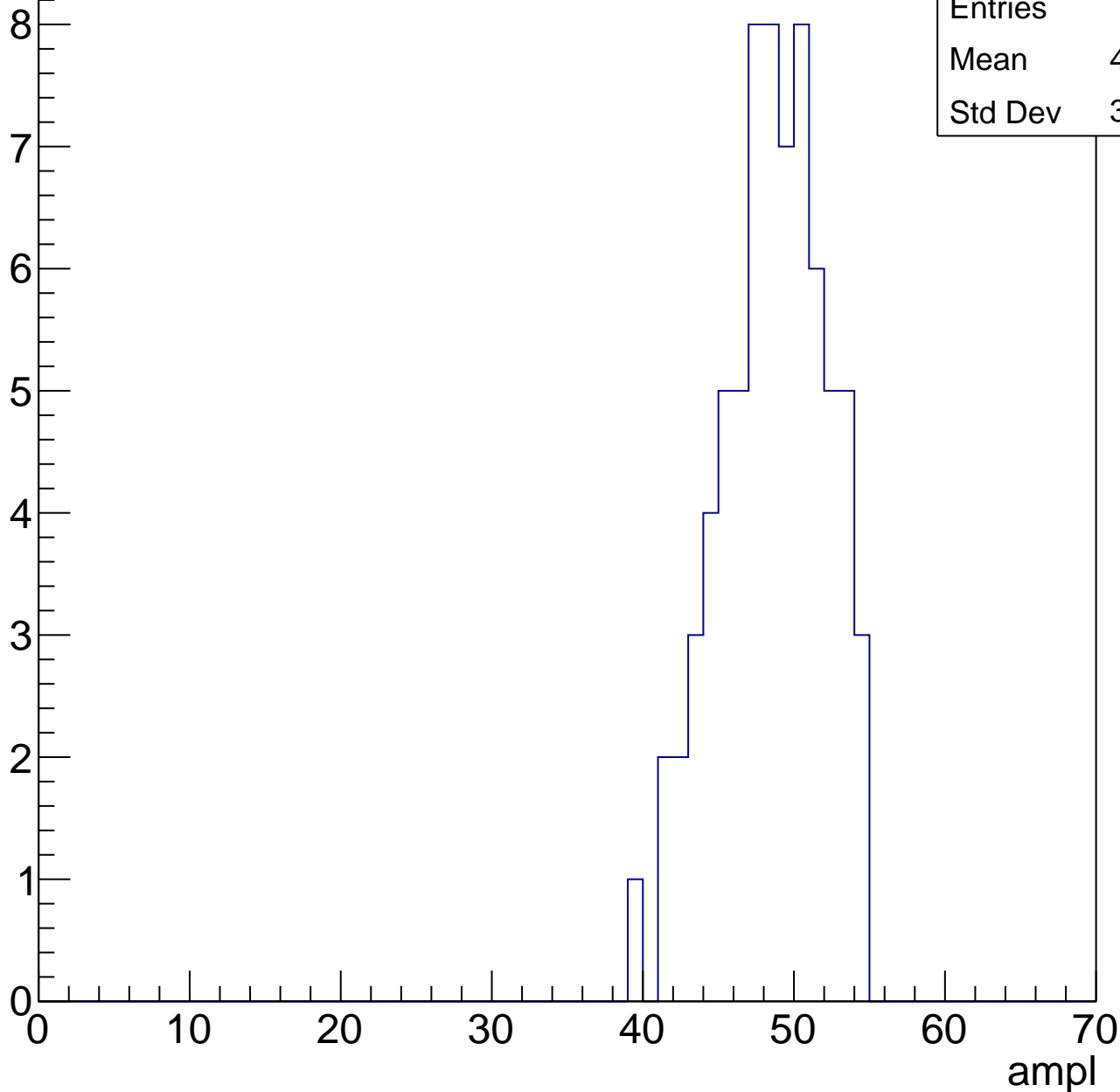
**Gaus Width: 2.9725**



# B1L101S, U9-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

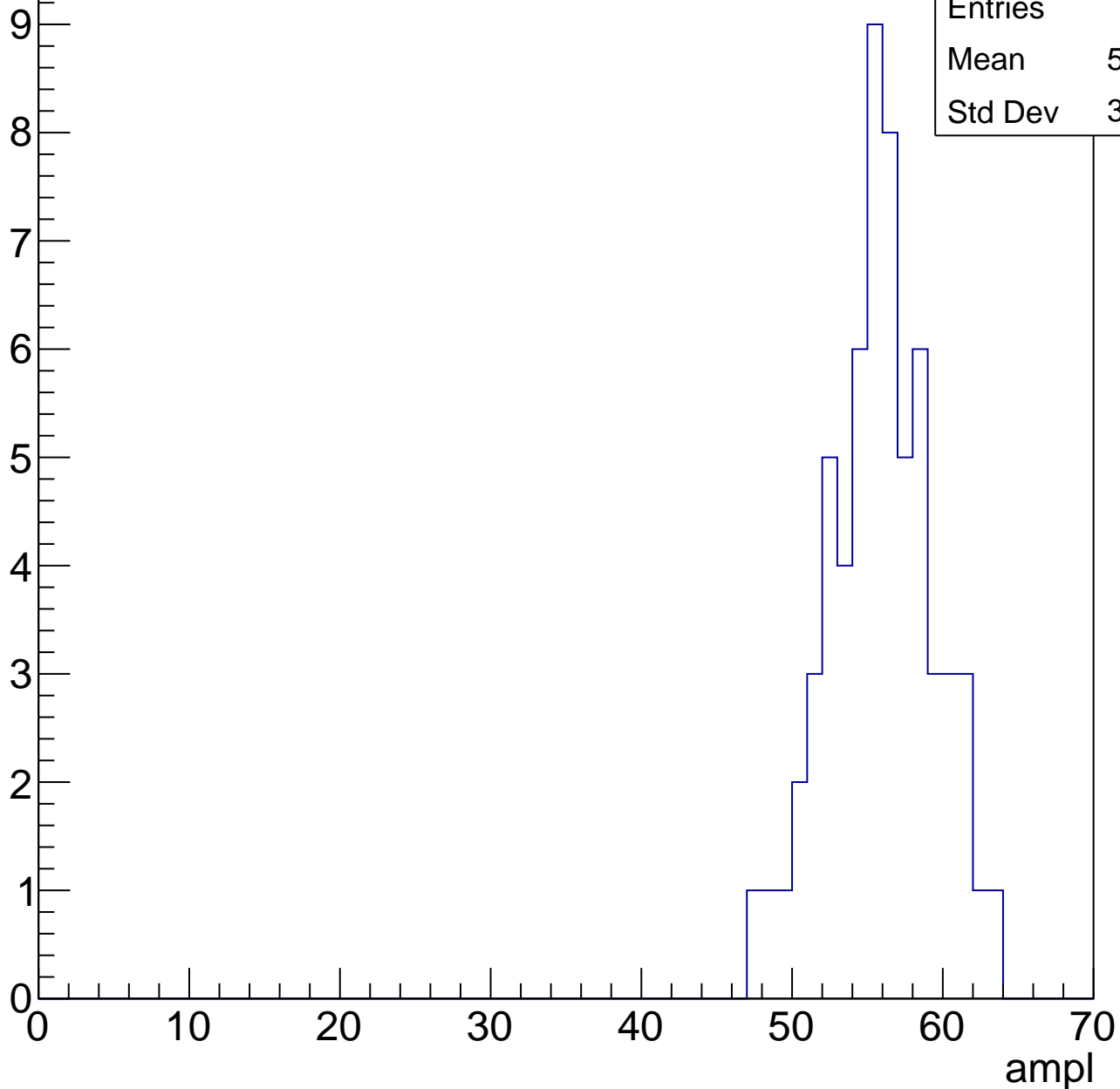


Entries	72
Mean	48.07
Std Dev	3.473

# B1L101S, U9-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

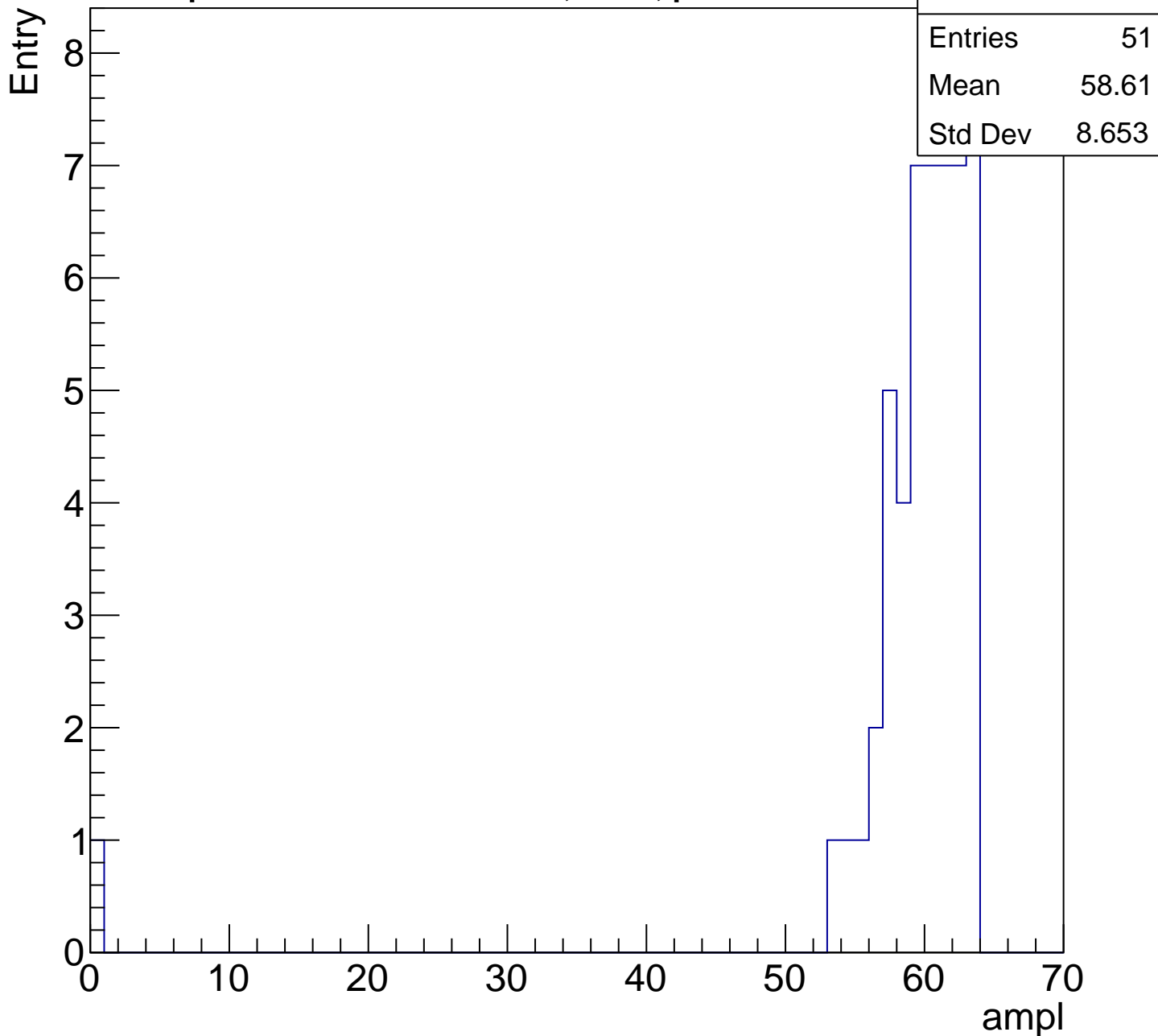
Entry



Entries	62
Mean	55.39
Std Dev	3.433

# B1L101S, U9-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U9-ch91, adc0

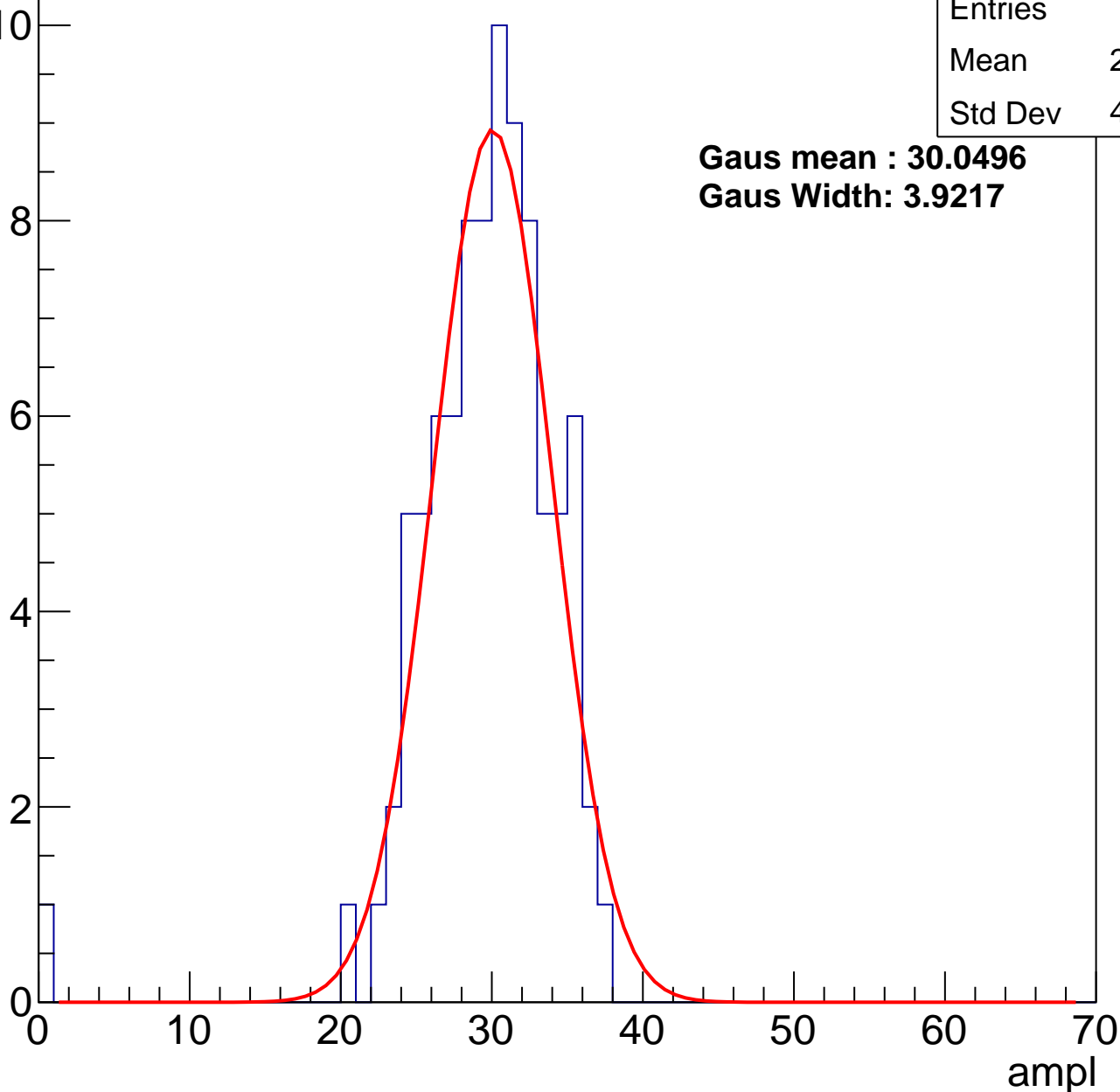
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	89
Mean	29.17
Std Dev	4.779

**Gaus mean : 30.0496**

**Gaus Width: 3.9217**



# B1L101S, U9-ch91, adc1

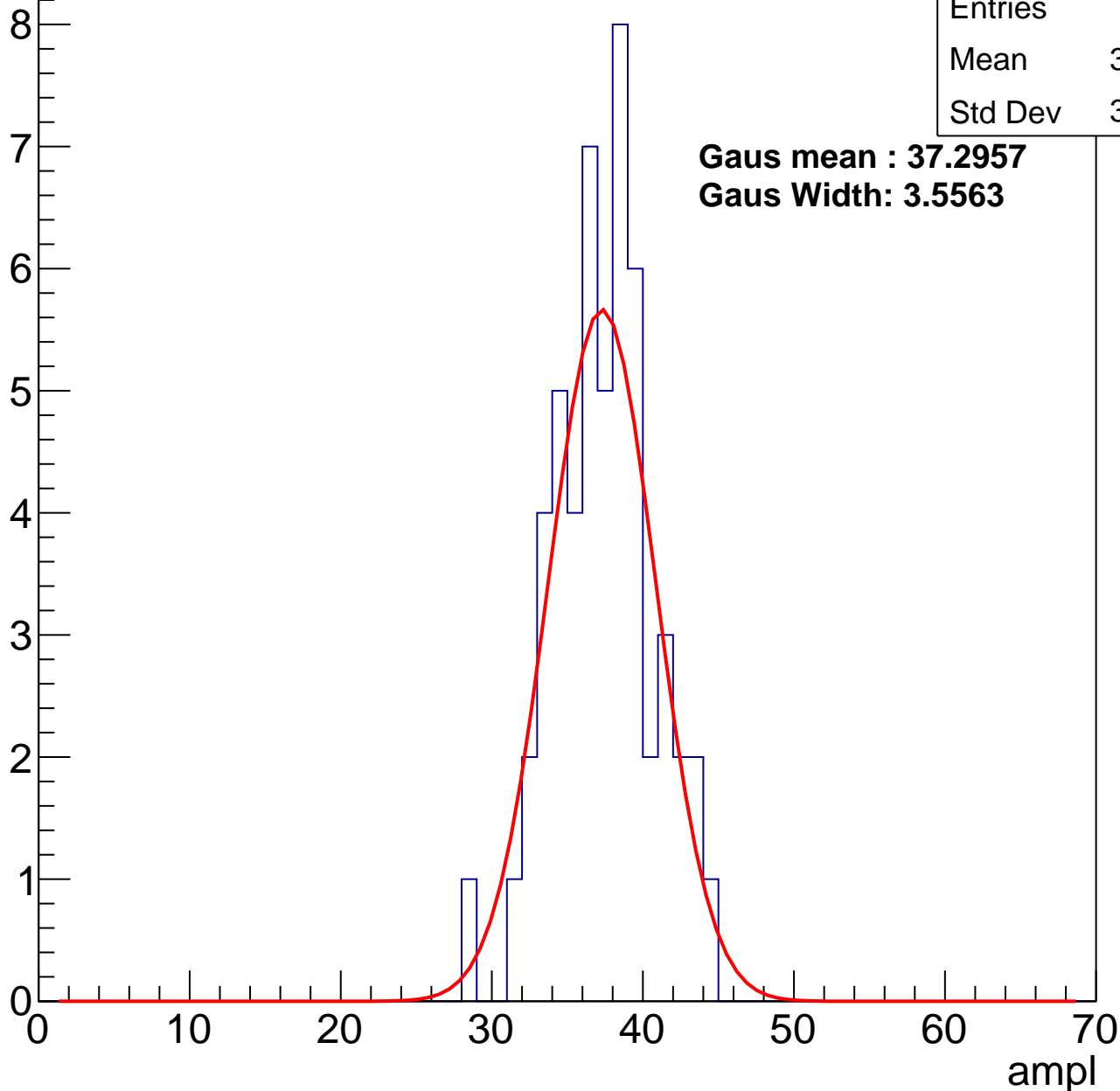
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	36.92
Std Dev	3.273

**Gaus mean : 37.2957**

**Gaus Width: 3.5563**



# B1L101S, U9-ch91, adc2

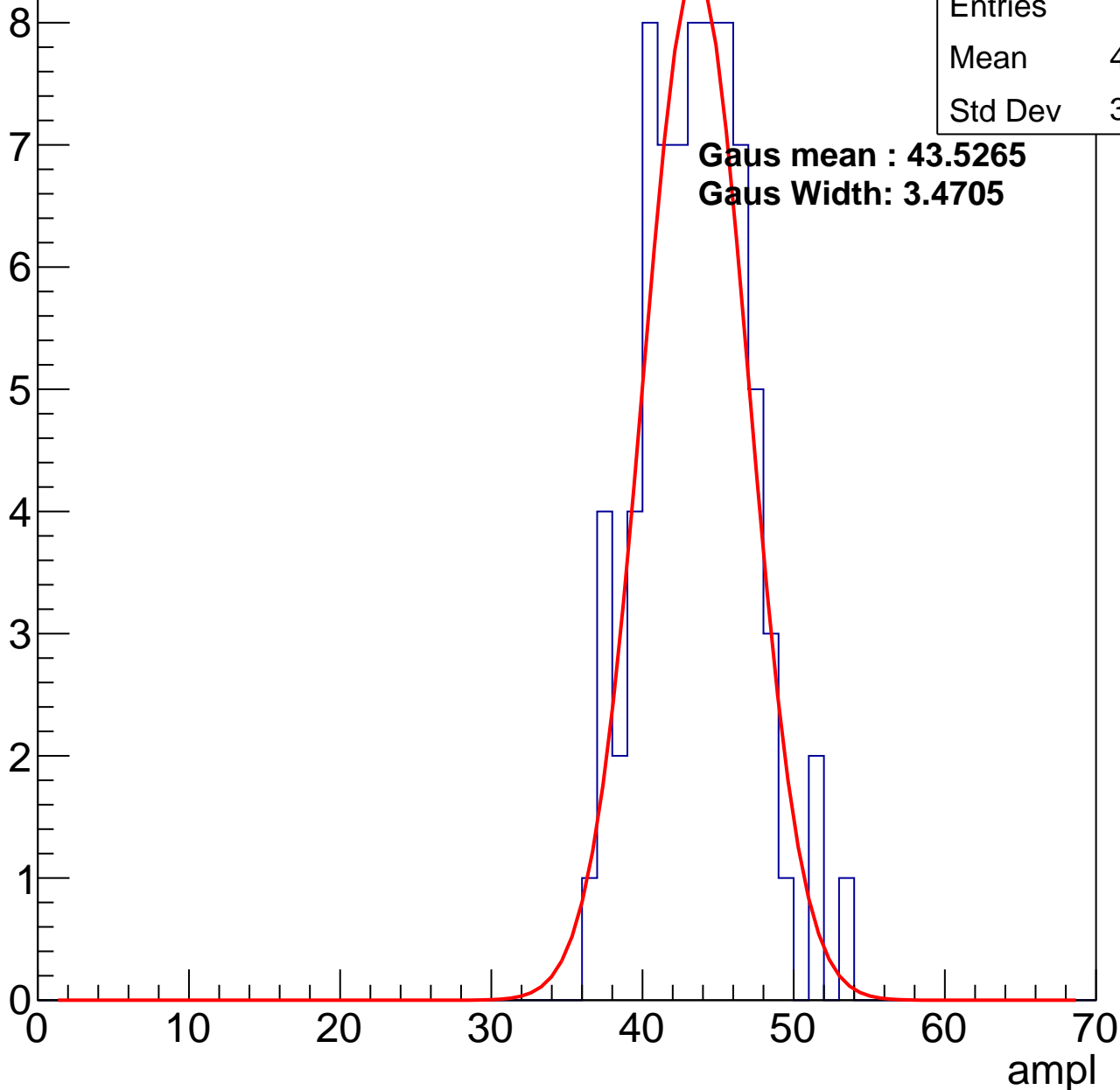
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	43.13
Std Dev	3.507

**Gaus mean : 43.5265**

**Gaus Width: 3.4705**

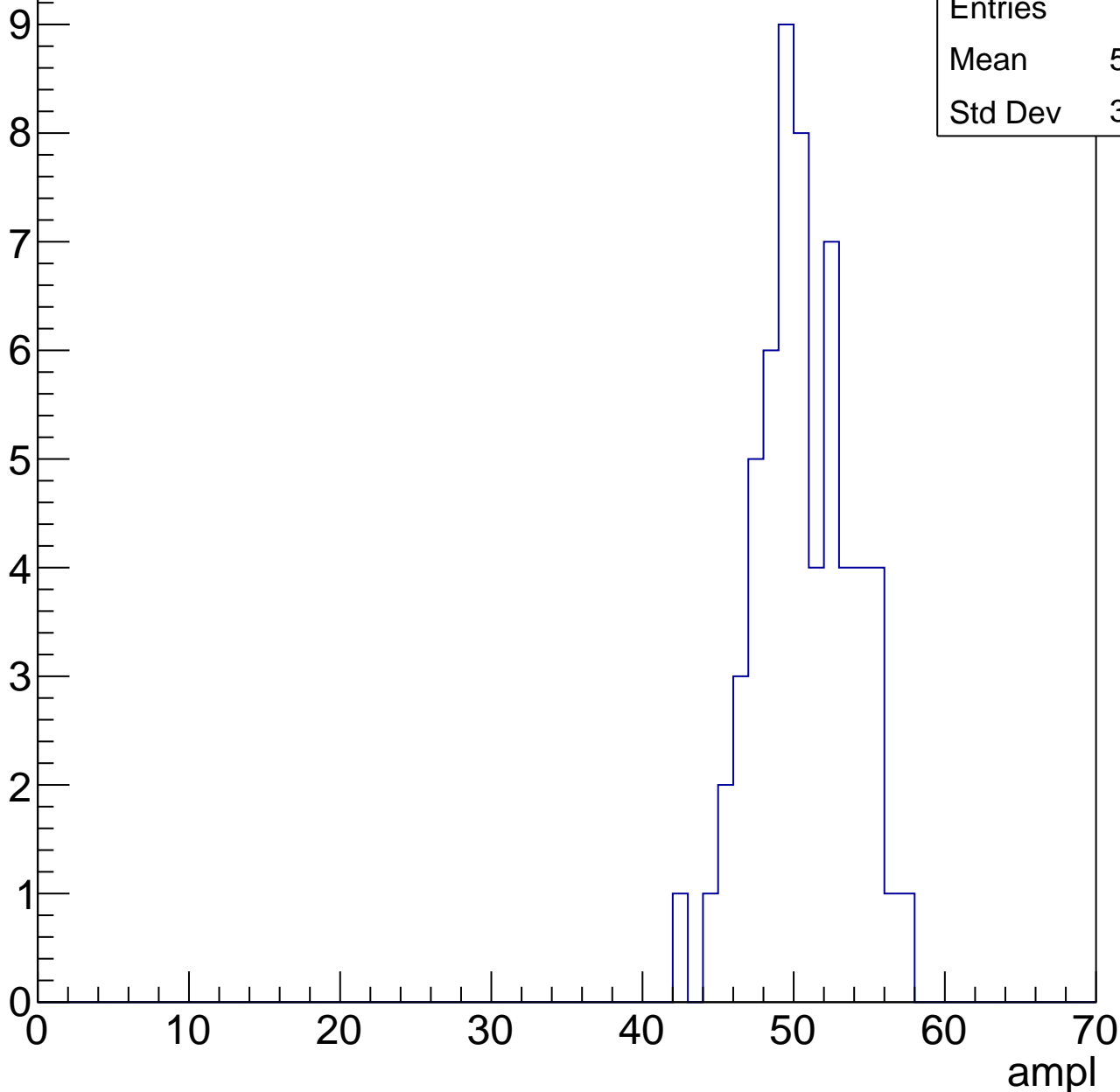


# B1L101S, U9-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	50.12
Std Dev	3.142

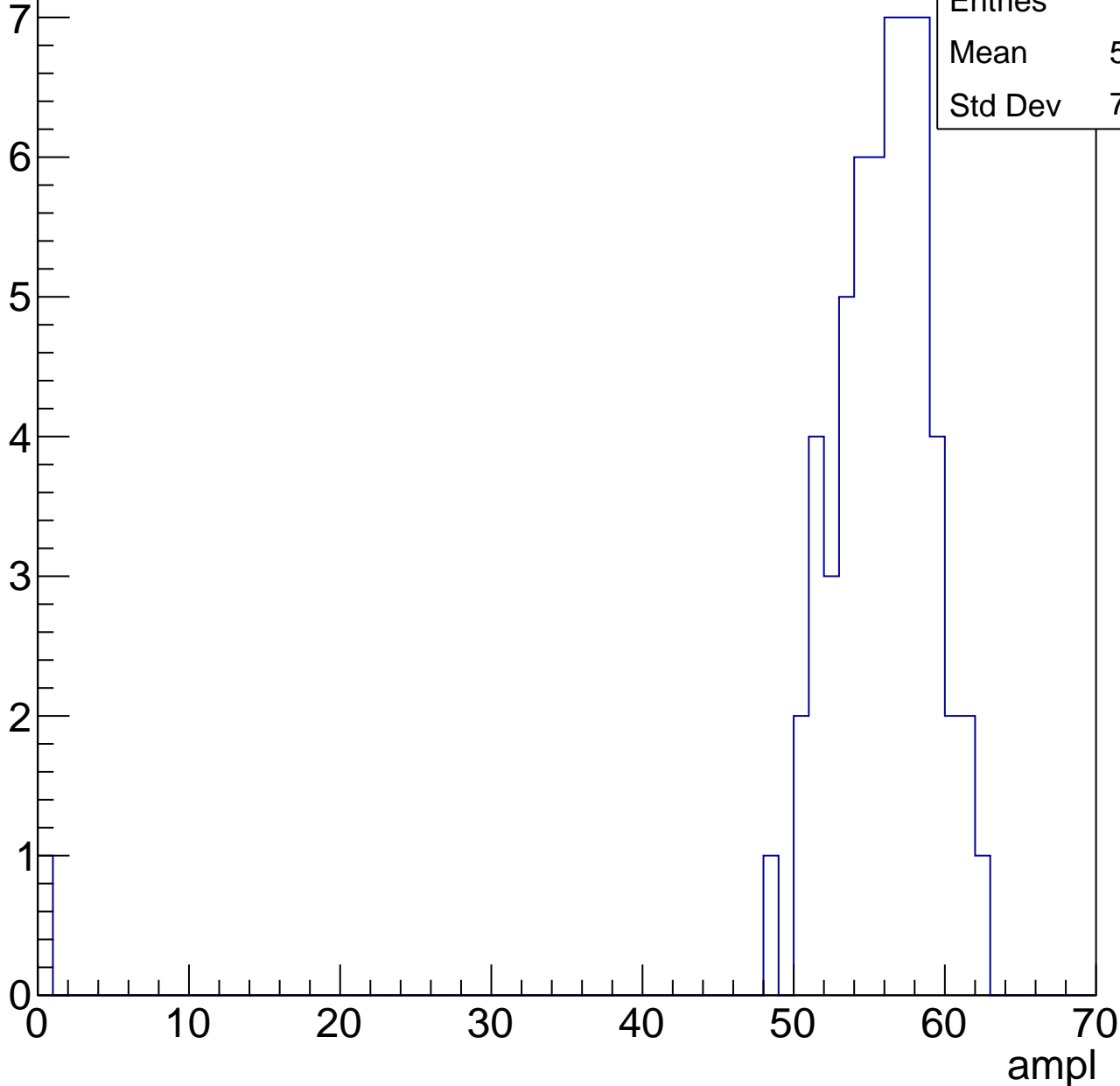


# B1L101S, U9-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	54.55
Std Dev	7.837



# B1L101S, U9-ch91, adc5

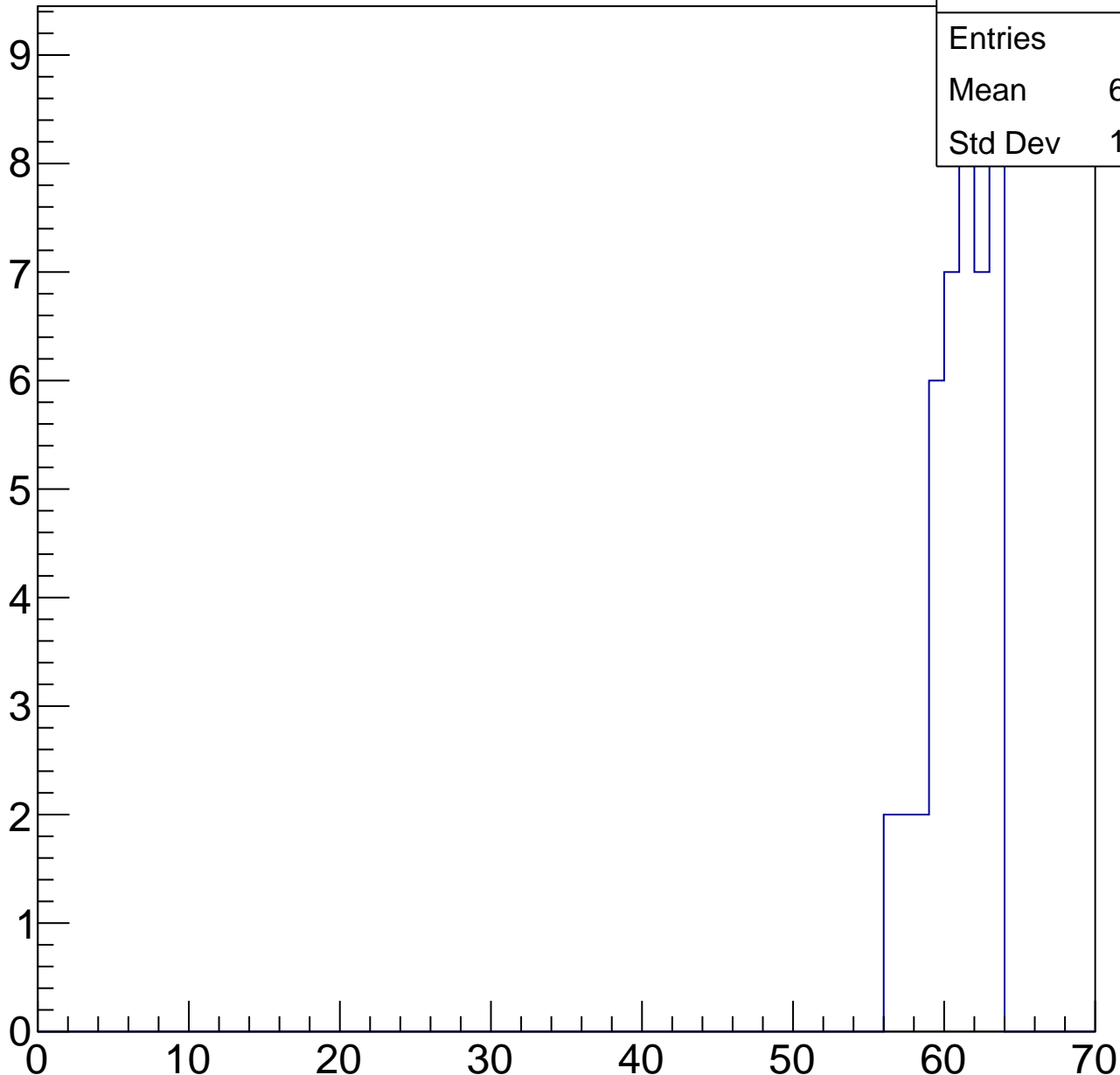
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	43
Mean	60.58
Std Dev	1.968

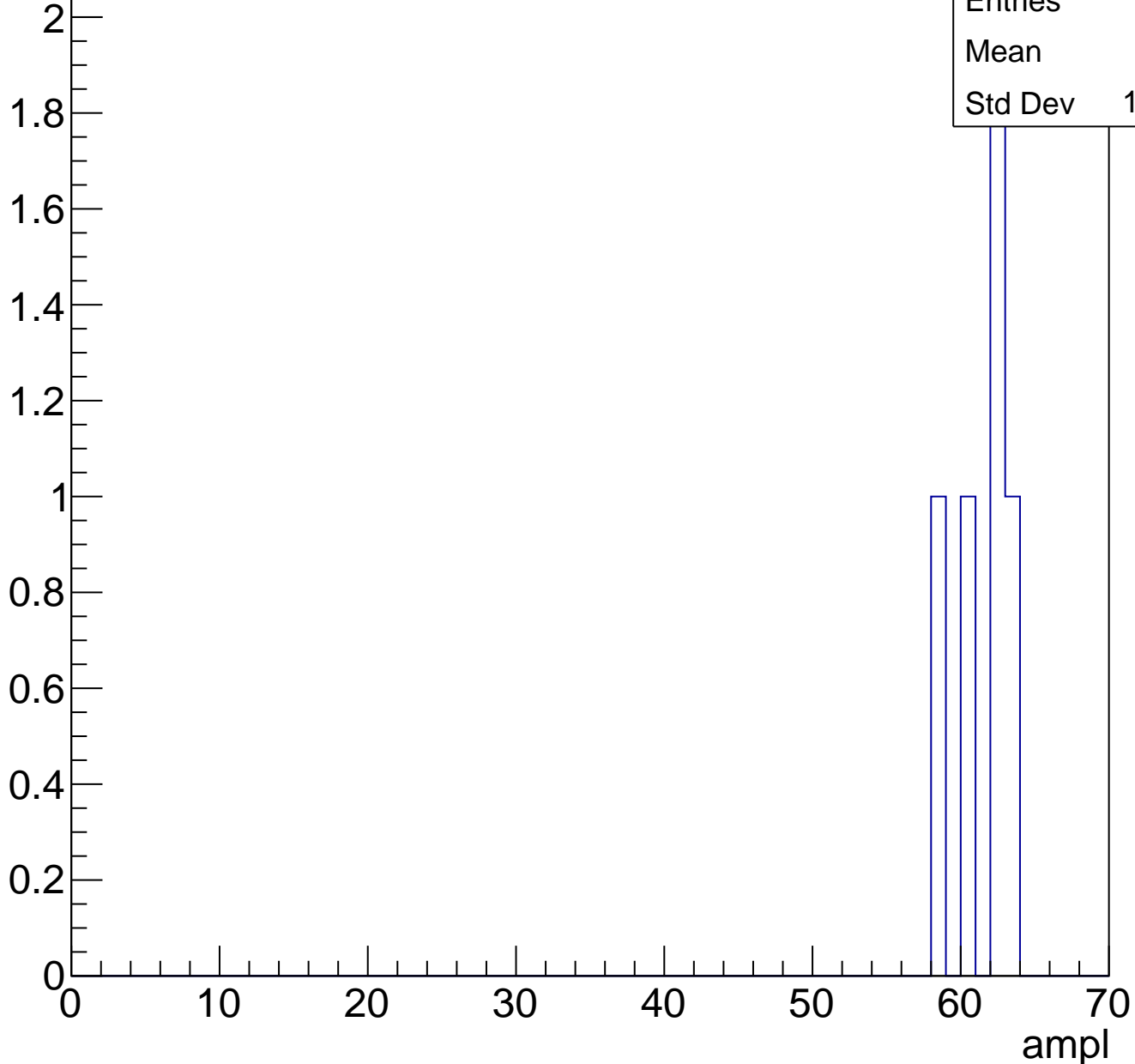
ampl



# B1L101S, U9-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch92, adc0

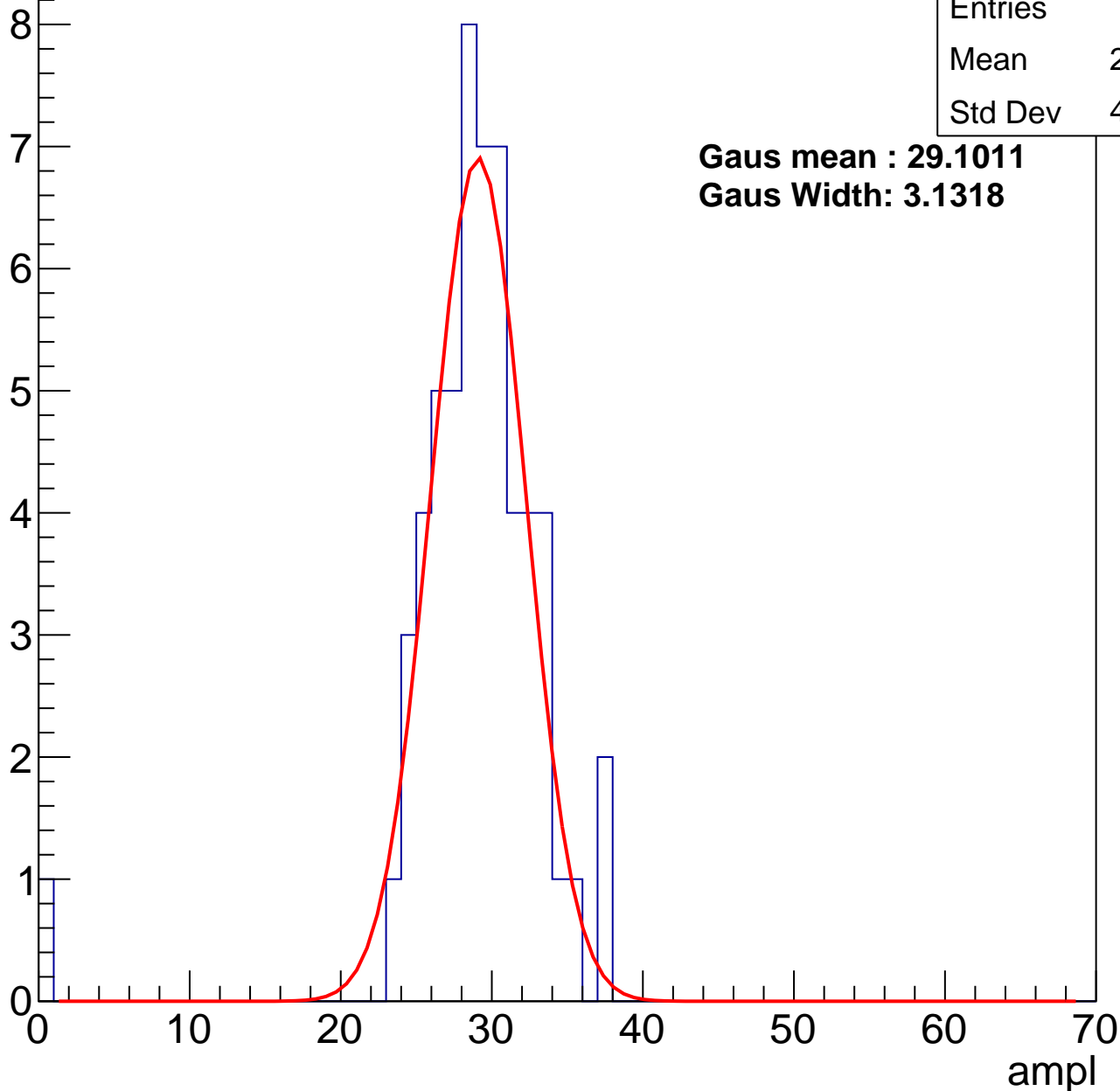
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	28.49
Std Dev	4.932

**Gaus mean : 29.1011**

**Gaus Width: 3.1318**



# B1L101S, U9-ch92, adc1

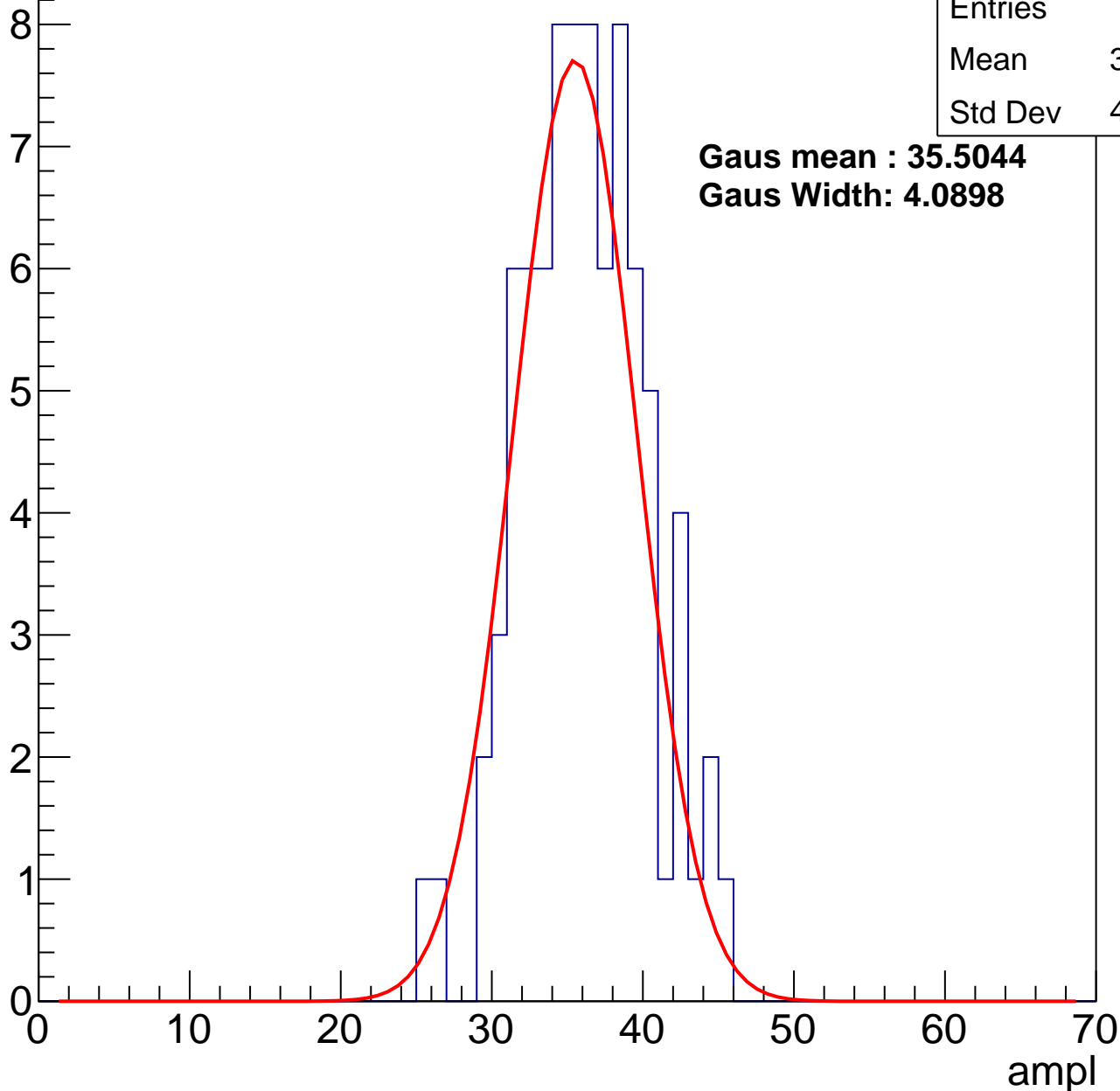
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	83
Mean	35.66
Std Dev	4.043

**Gaus mean : 35.5044**

**Gaus Width: 4.0898**



# B1L101S, U9-ch92, adc2

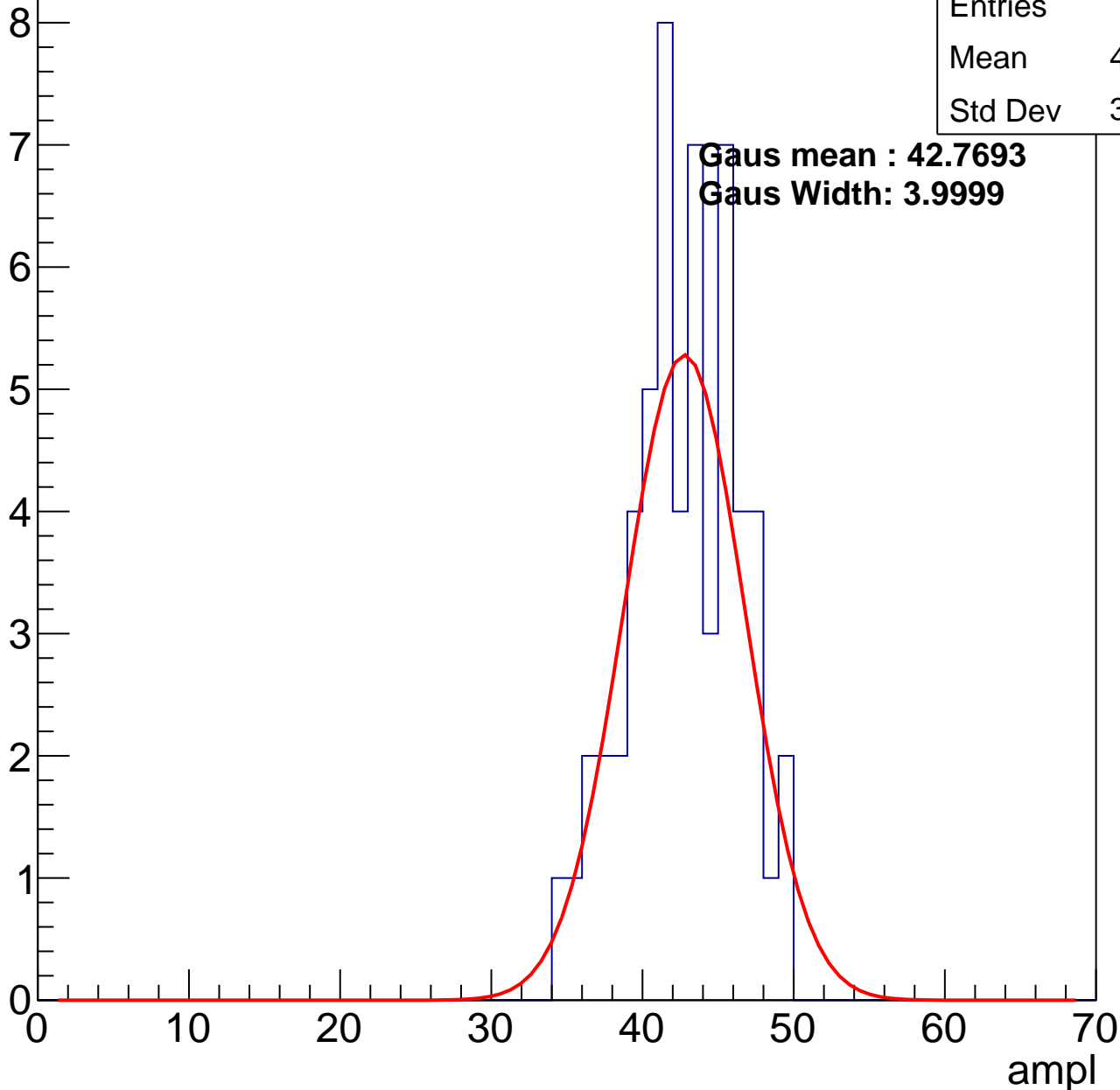
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	42.26
Std Dev	3.522

**Gaus mean : 42.7693**

**Gaus Width: 3.9999**

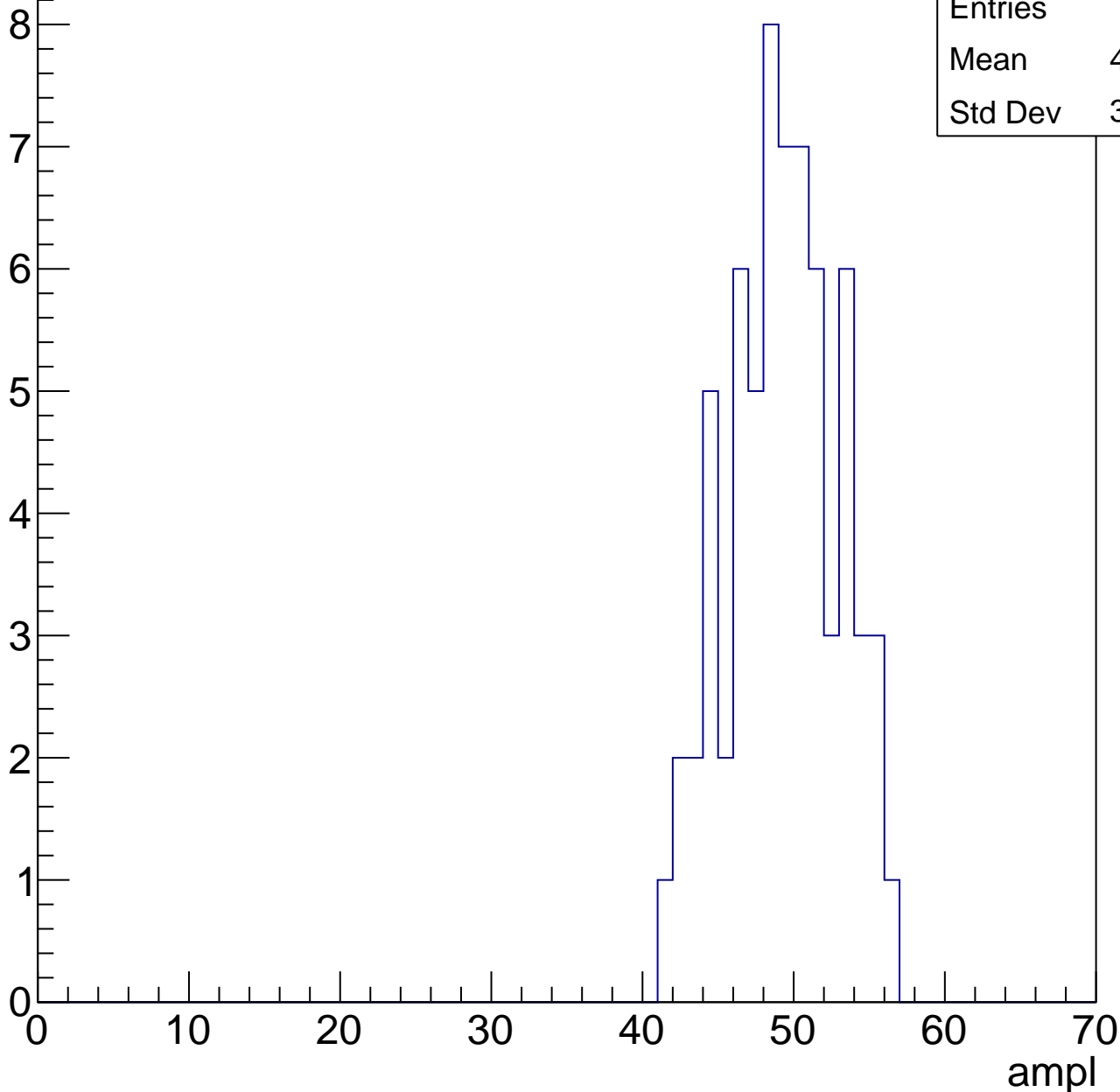


# B1L101S, U9-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

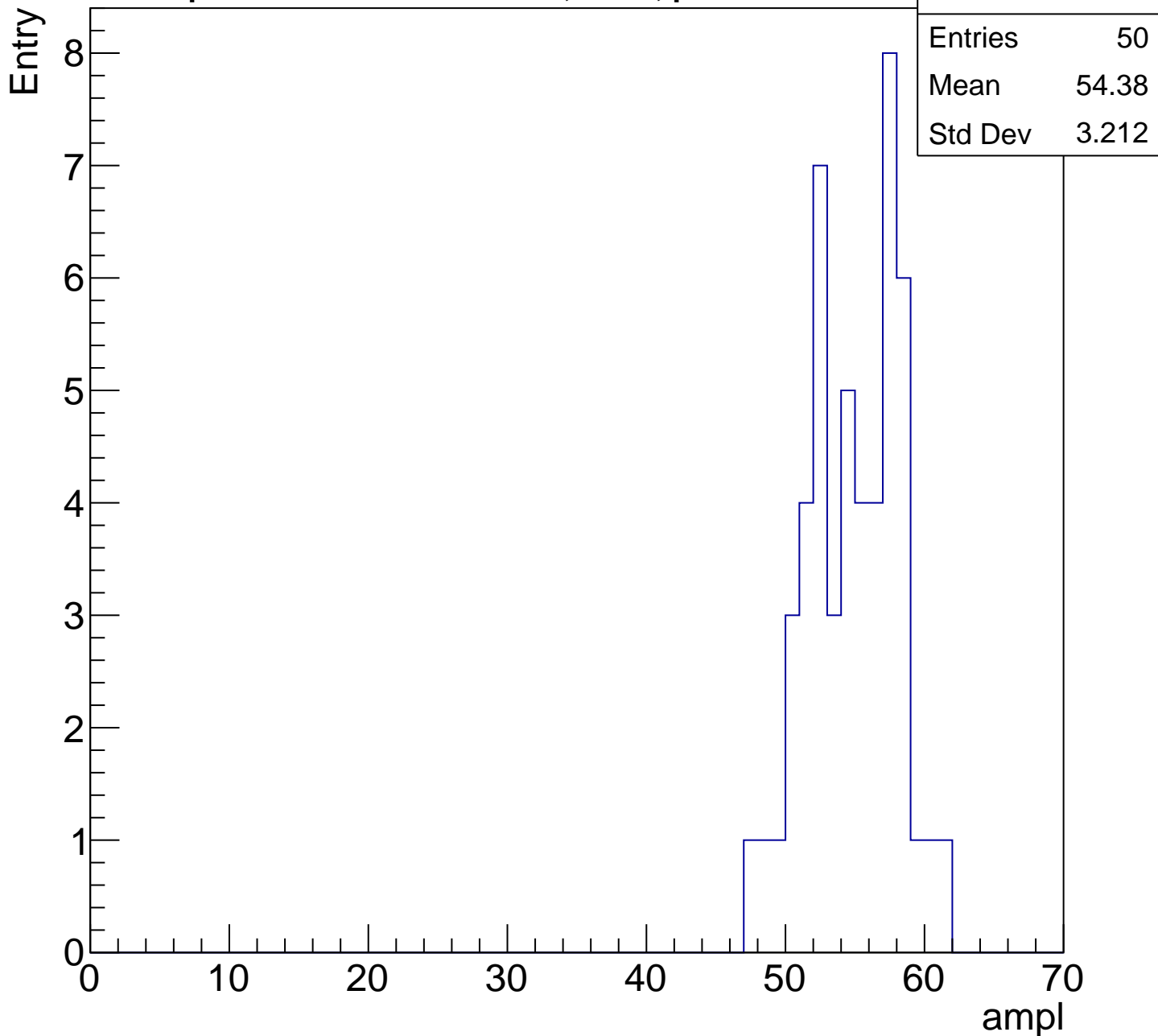
Entry

Entries	67
Mean	48.84
Std Dev	3.577



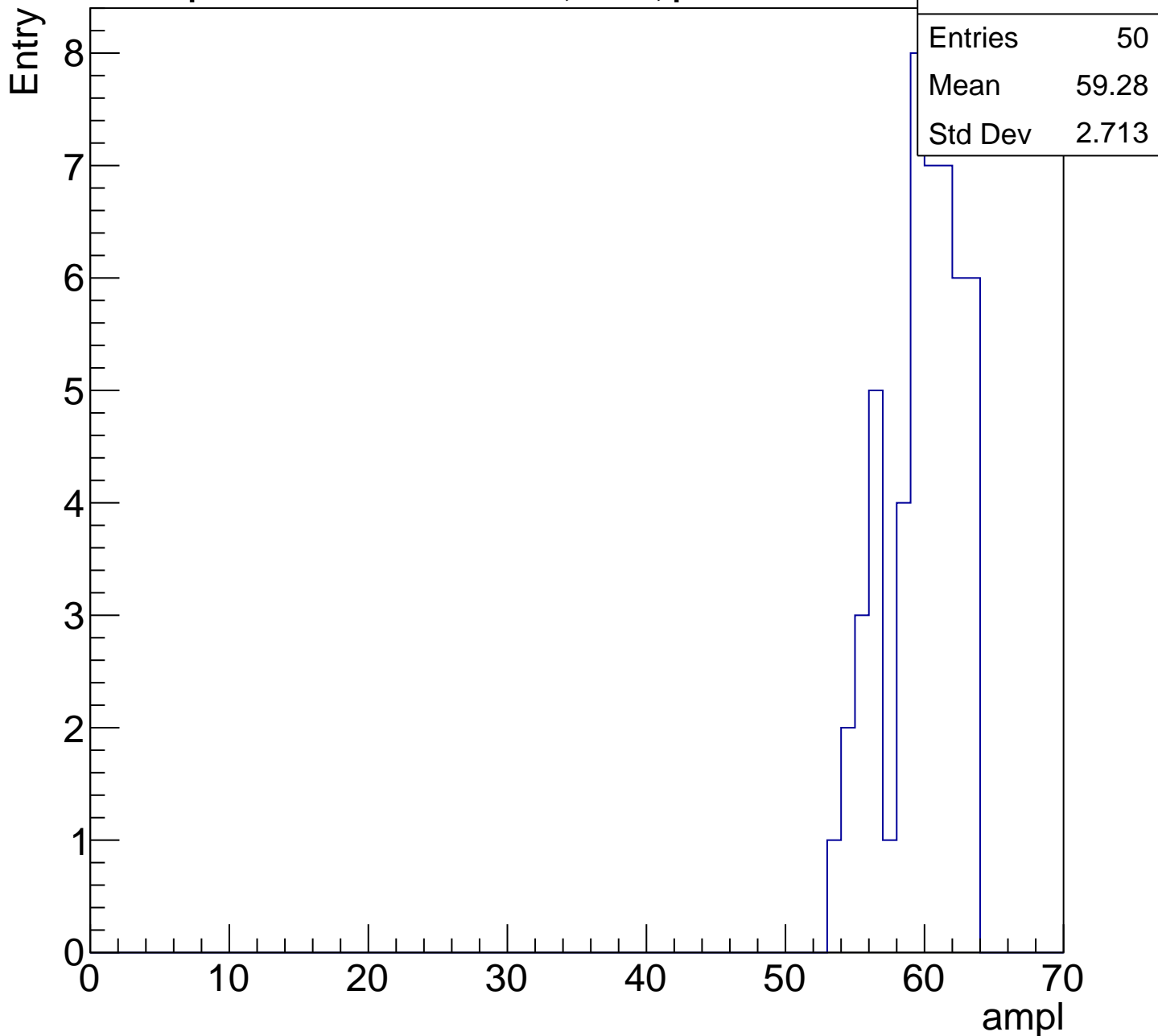
# B1L101S, U9-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch92, adc5

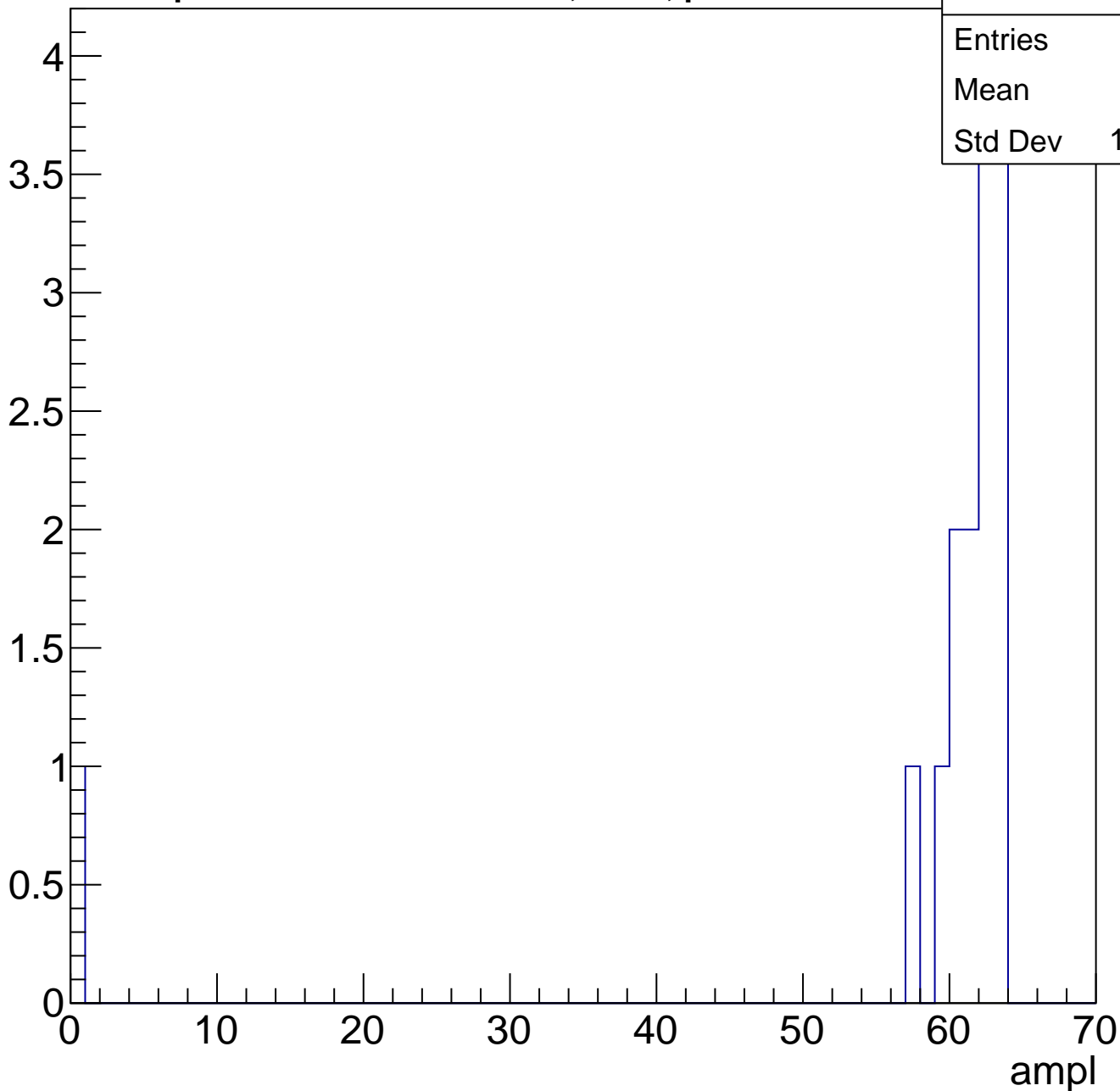
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch93, adc0

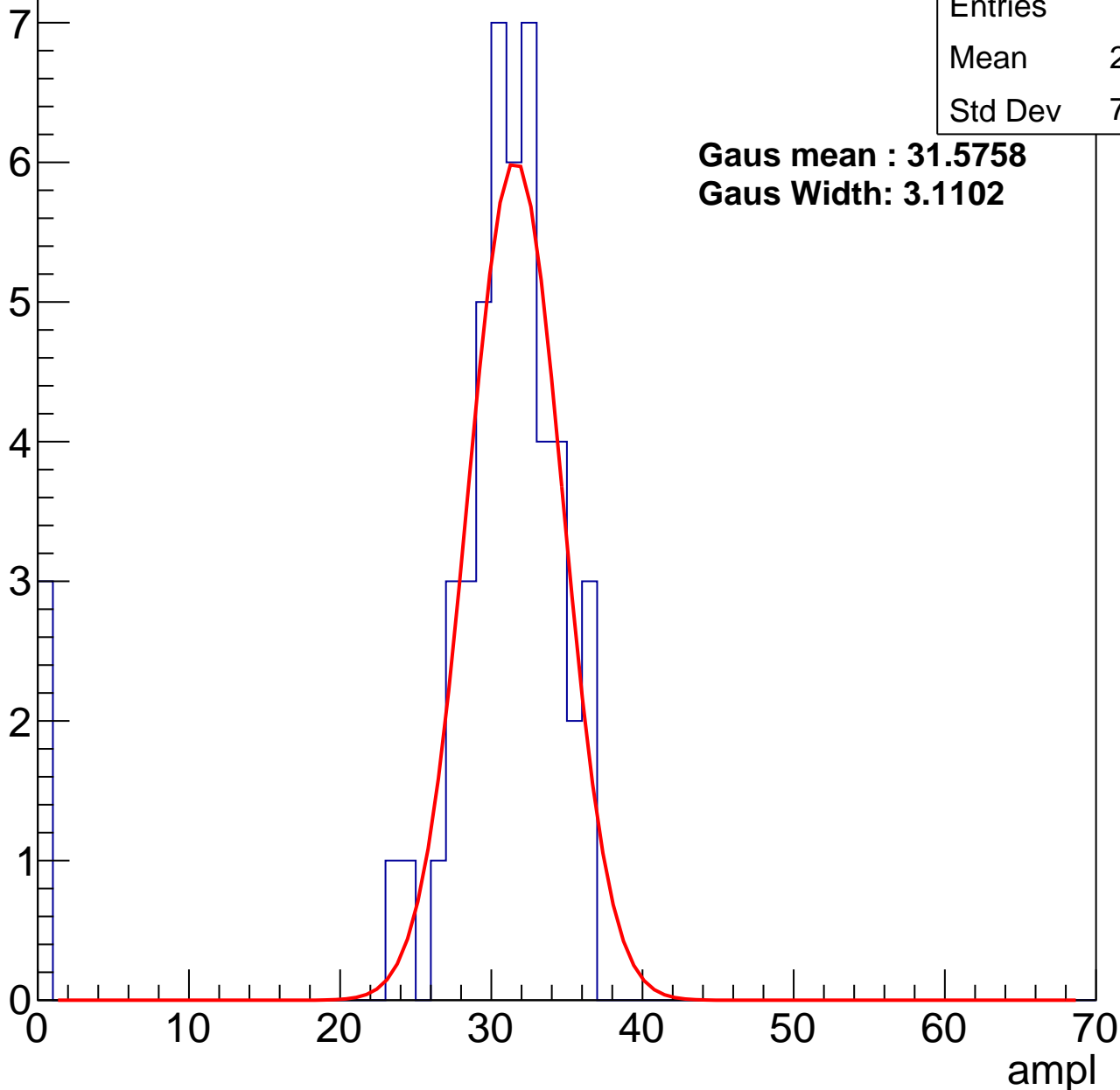
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	28.98
Std Dev	7.855

**Gaus mean : 31.5758**

**Gaus Width: 3.1102**



# B1L101S, U9-ch93, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	83
Mean	37.53
Std Dev	3.618

**Gaus mean : 37.7931**

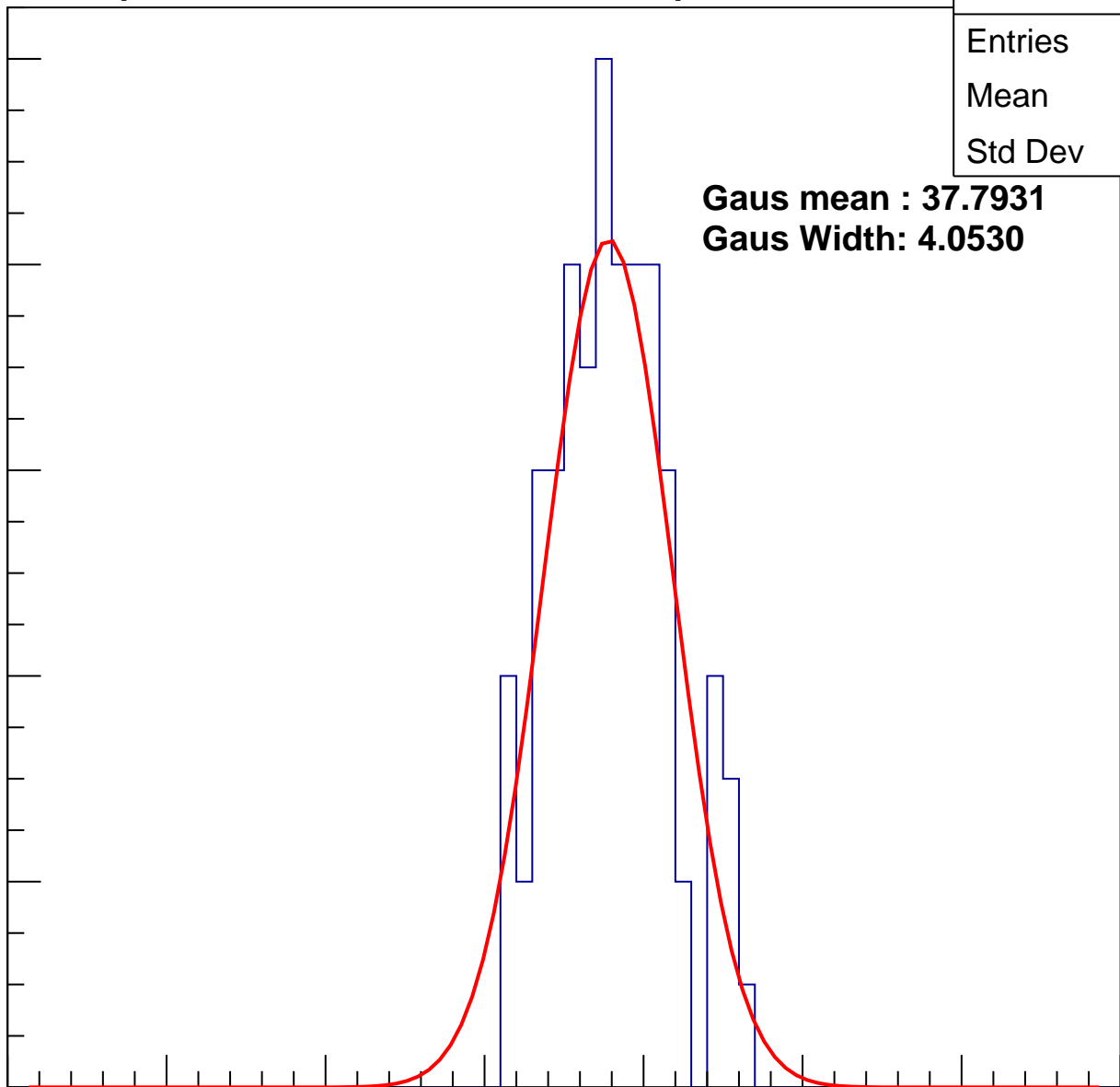
**Gaus Width: 4.0530**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U9-ch93, adc2

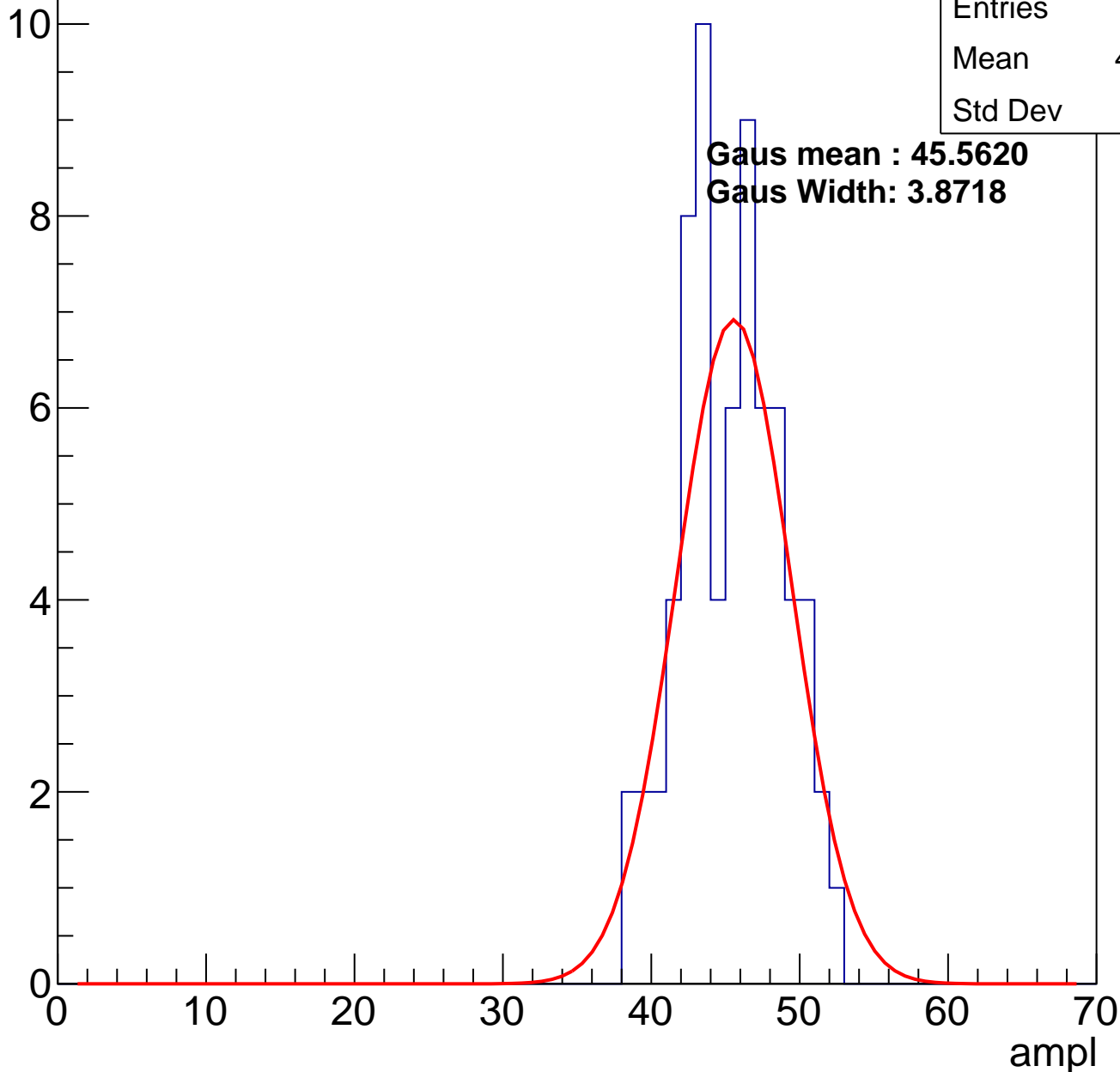
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	70
Mean	44.91
Std Dev	3.32

**Gaus mean : 45.5620**

**Gaus Width: 3.8718**

Entry

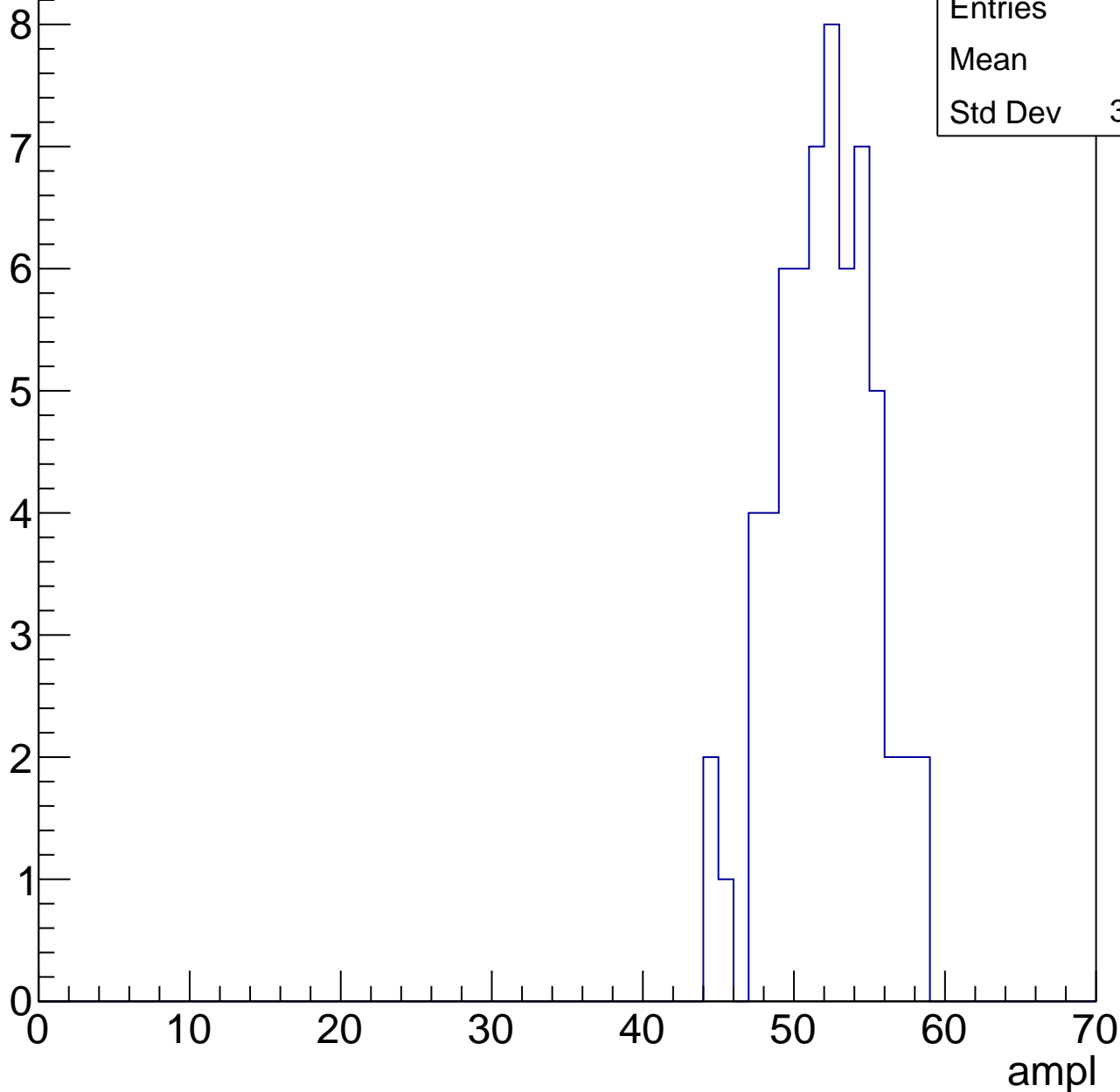


# B1L101S, U9-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

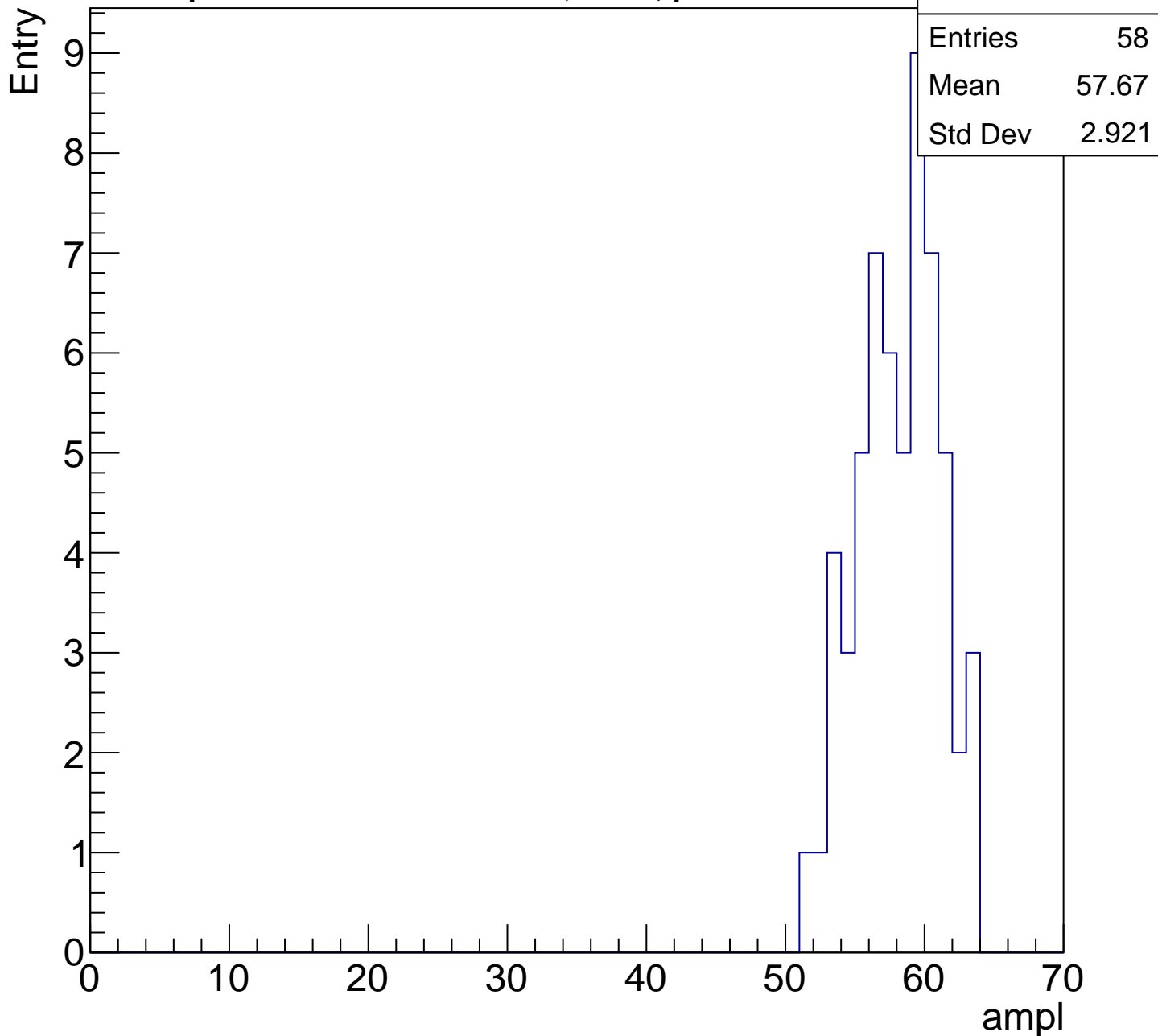
Entry

Entries	62
Mean	51.5
Std Dev	3.222



# B1L101S, U9-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

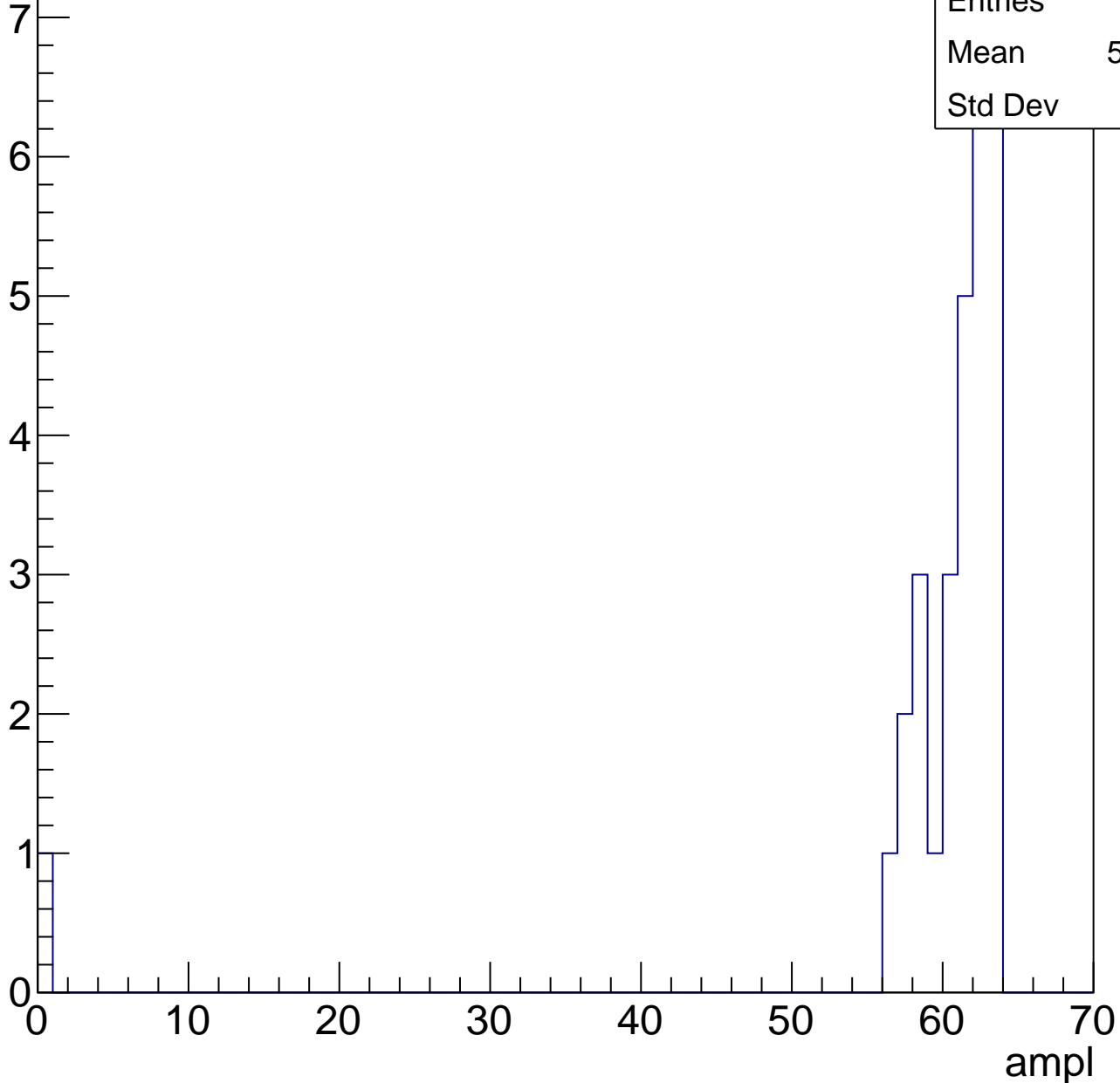


# B1L101S, U9-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	30
Mean	58.77
Std Dev	11.1



# B1L101S, U9-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U9-ch94, adc0

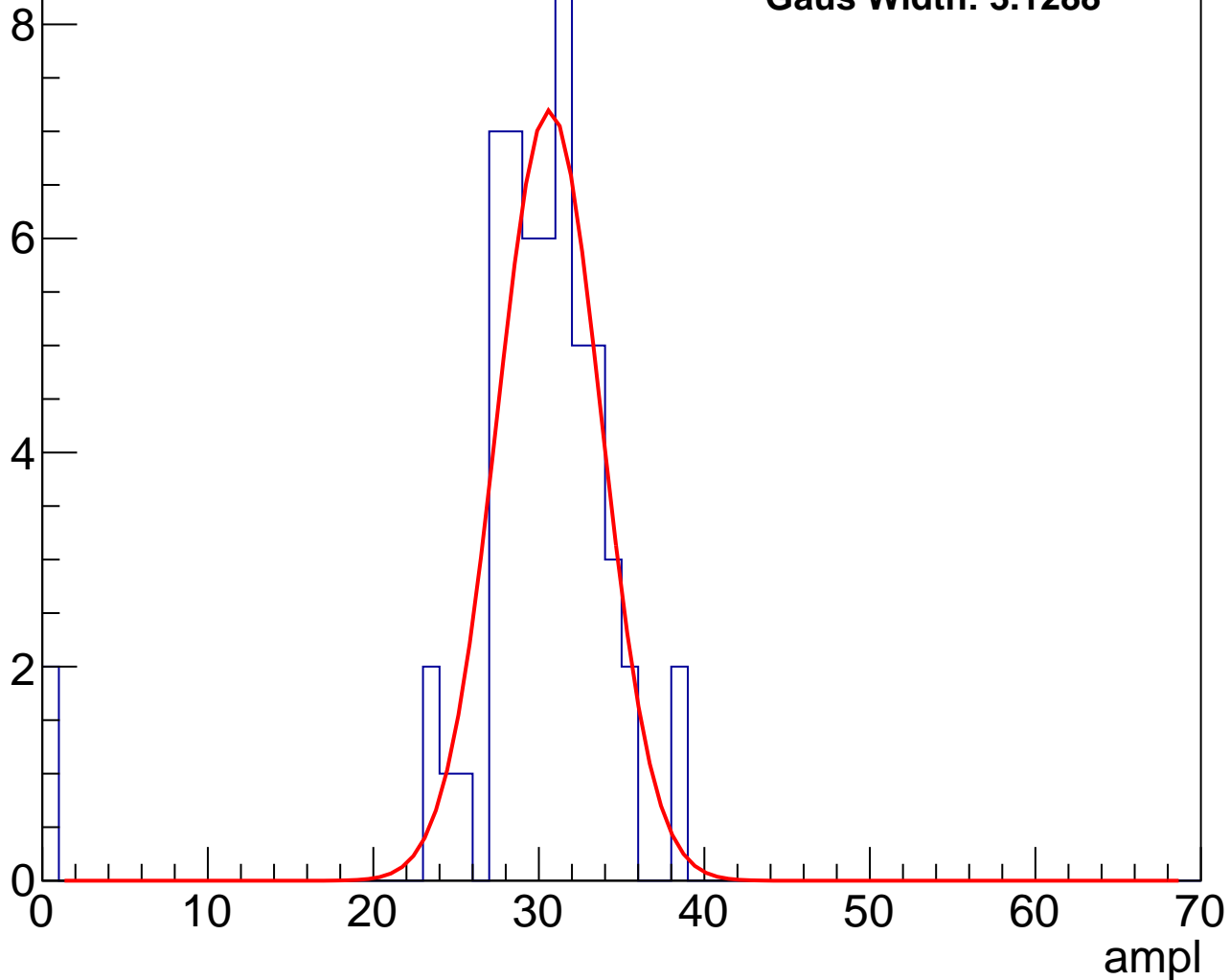
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	29.1
Std Dev	6.256

**Gaus mean : 30.6253**

**Gaus Width: 3.1288**



# B1L101S, U9-ch94, adc1

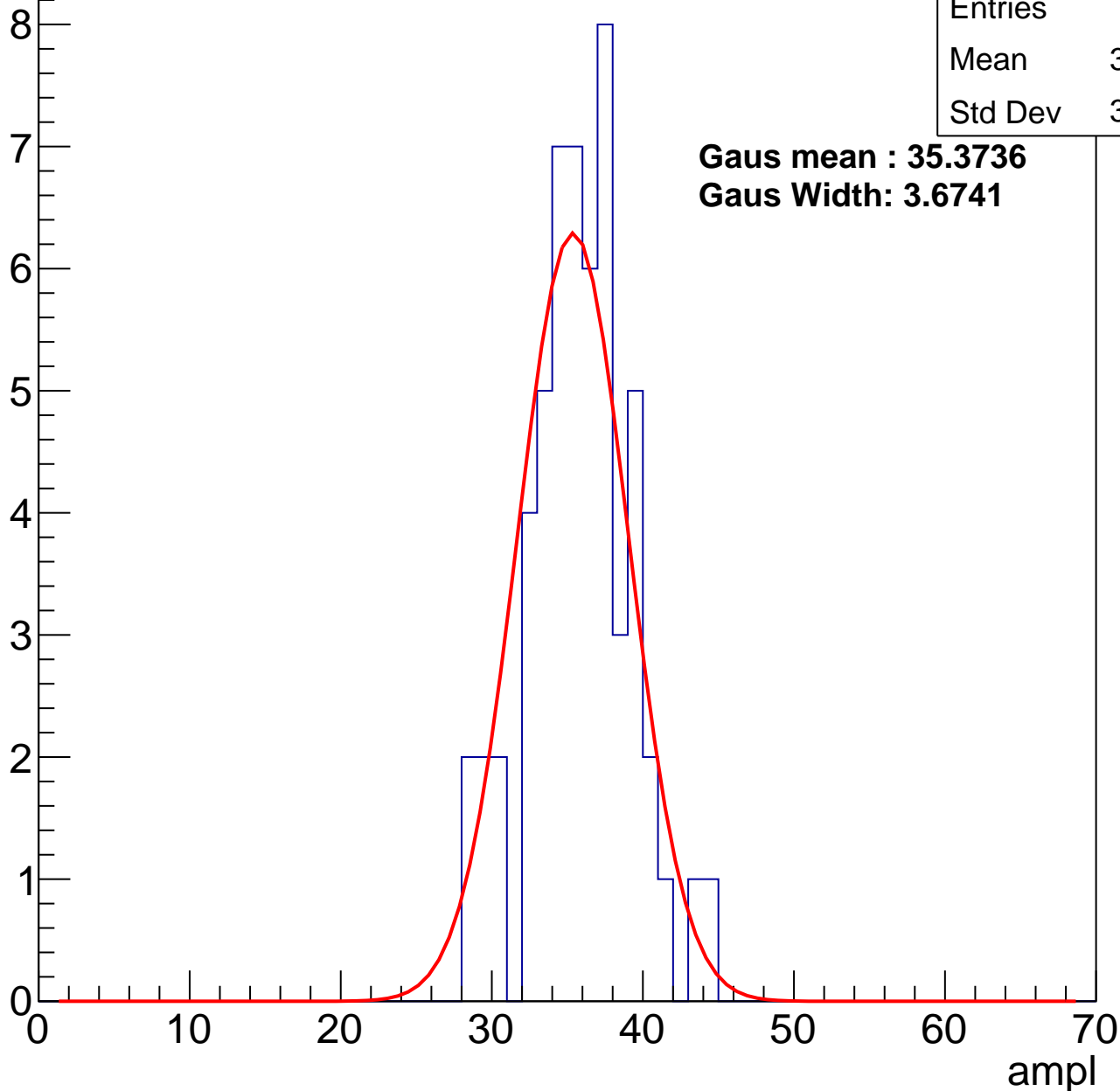
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	35.34
Std Dev	3.414

**Gaus mean : 35.3736**

**Gaus Width: 3.6741**



# B1L101S, U9-ch94, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	92
Mean	42.91
Std Dev	3.833

**Gaus mean : 43.1910**

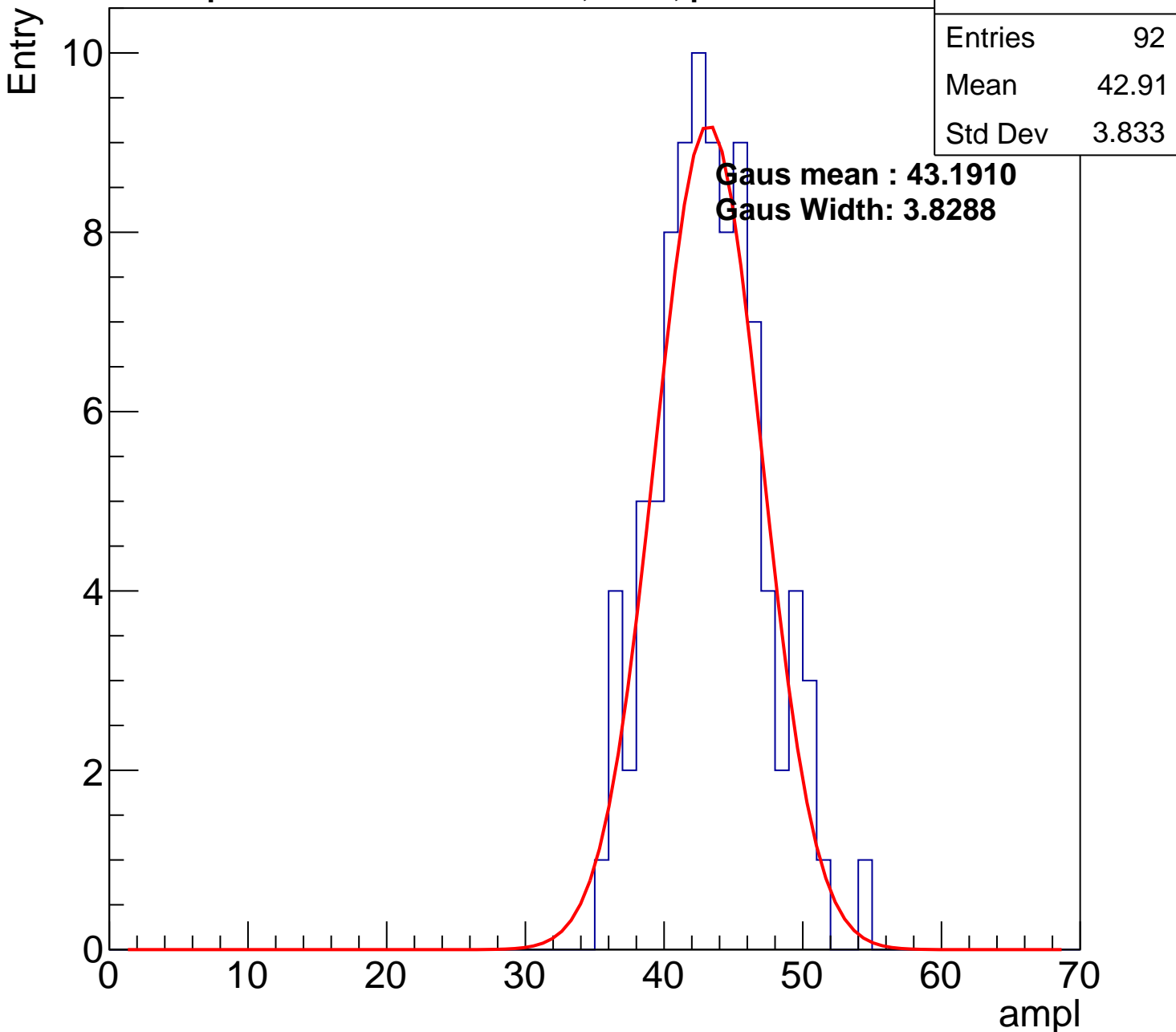
**Gaus Width: 3.8288**

Entry

10  
8  
6  
4  
2  
0

ampl

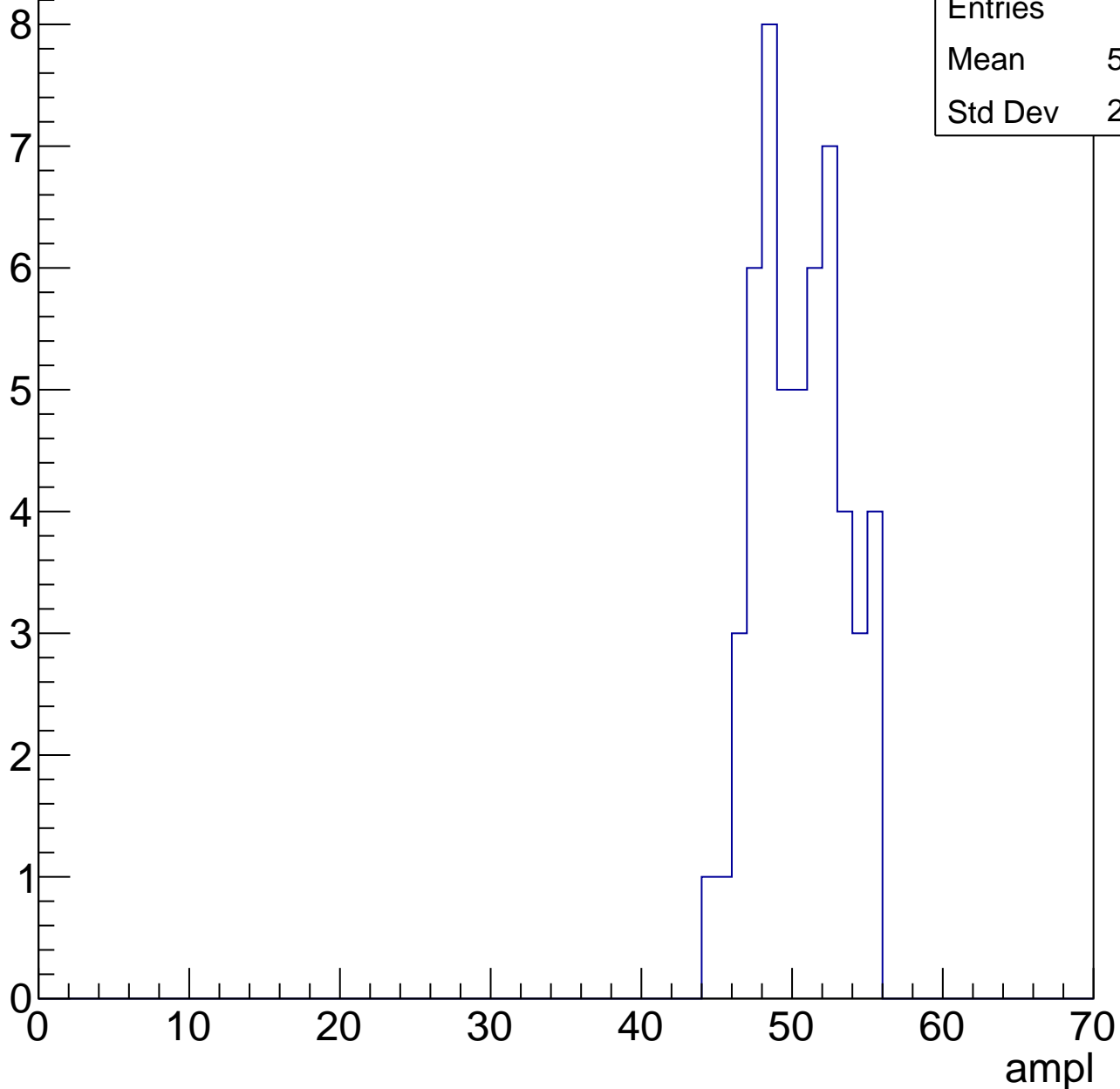
0 10 20 30 40 50 60 70



# B1L101S, U9-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

Entries 48

Mean 55.35

Std Dev 3.152

ampl

0

10

20

30

40

50

60

70

0

1

2

3

4

5

6

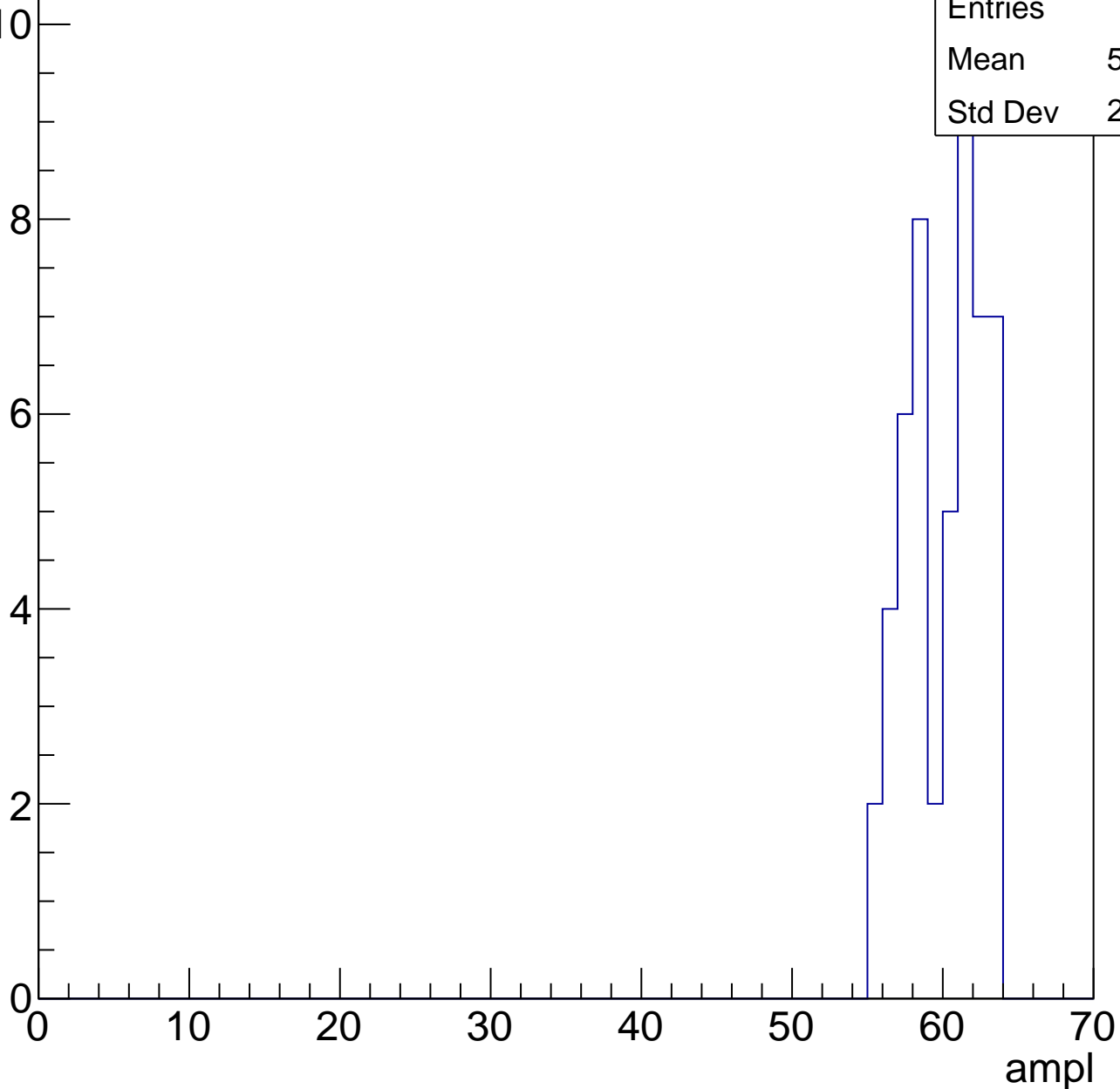
7

# B1L101S, U9-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

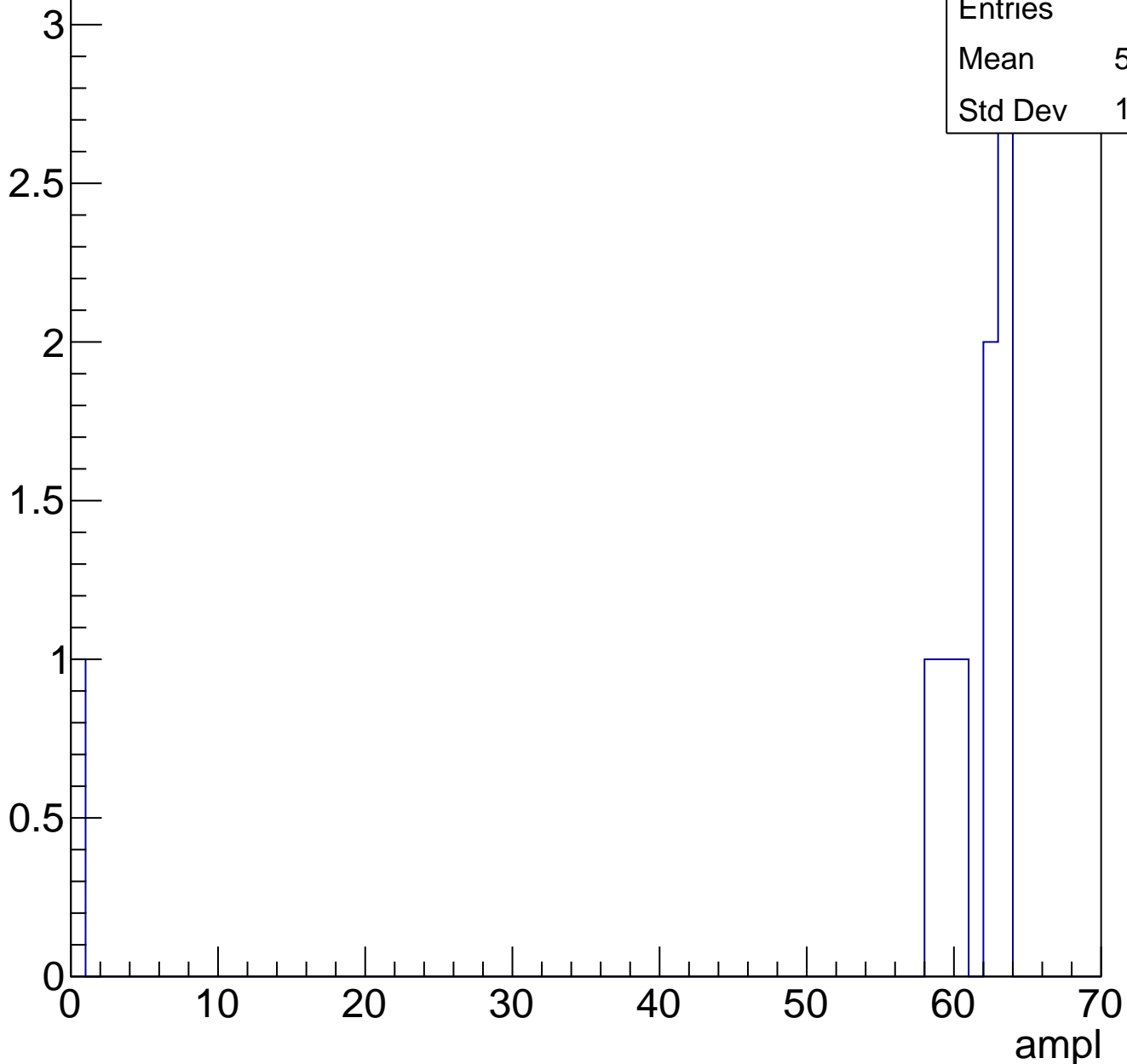
Entries	51
Mean	59.67
Std Dev	2.415



# B1L101S, U9-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U9-ch95, adc0

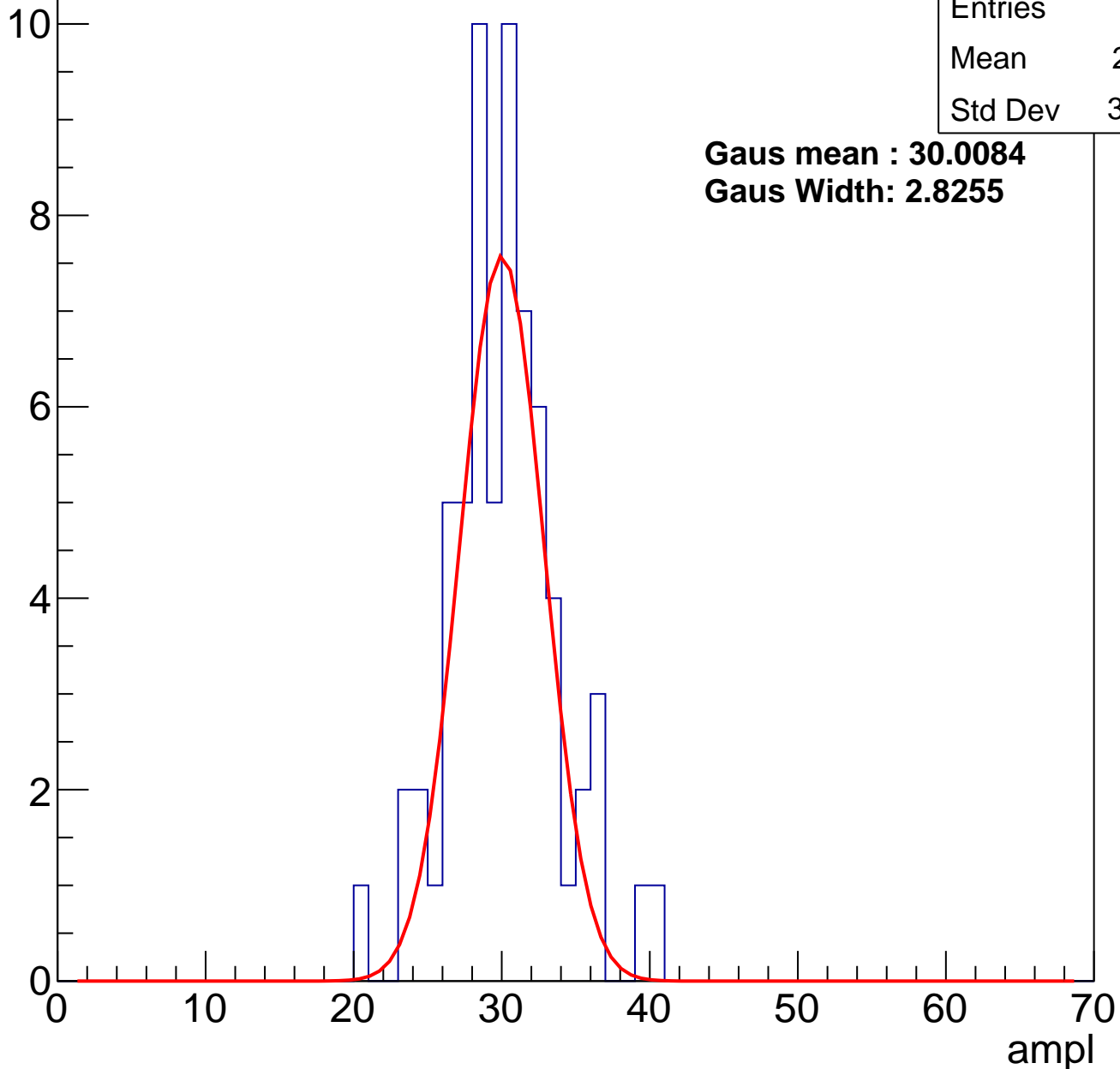
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	66
Mean	29.71
Std Dev	3.655

**Gaus mean : 30.0084**

**Gaus Width: 2.8255**

Entry



# B1L101S, U9-ch95, adc1

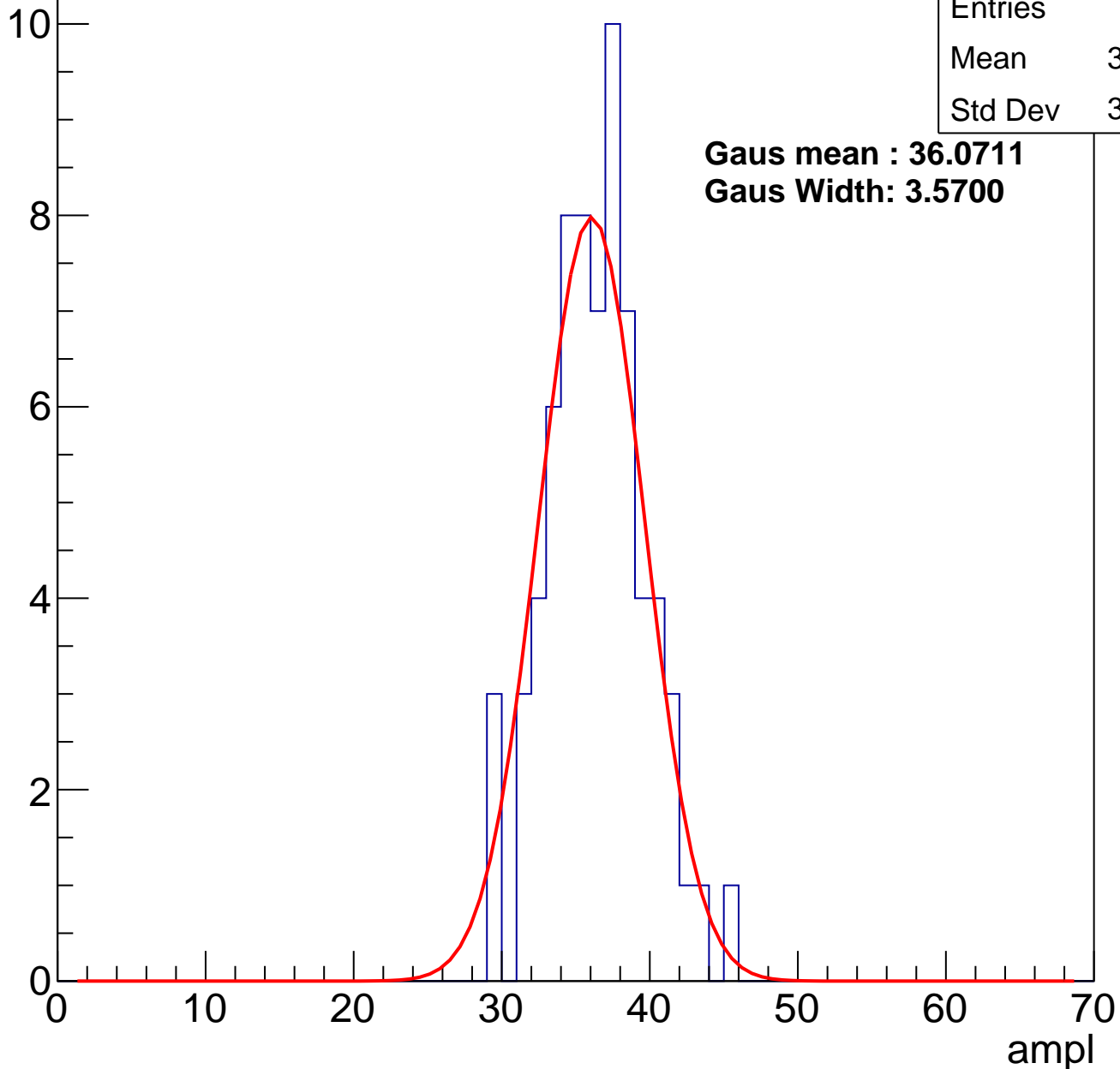
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	70
Mean	35.93
Std Dev	3.292

**Gaus mean : 36.0711**

**Gaus Width: 3.5700**

Entry



# B1L101S, U9-ch95, adc2

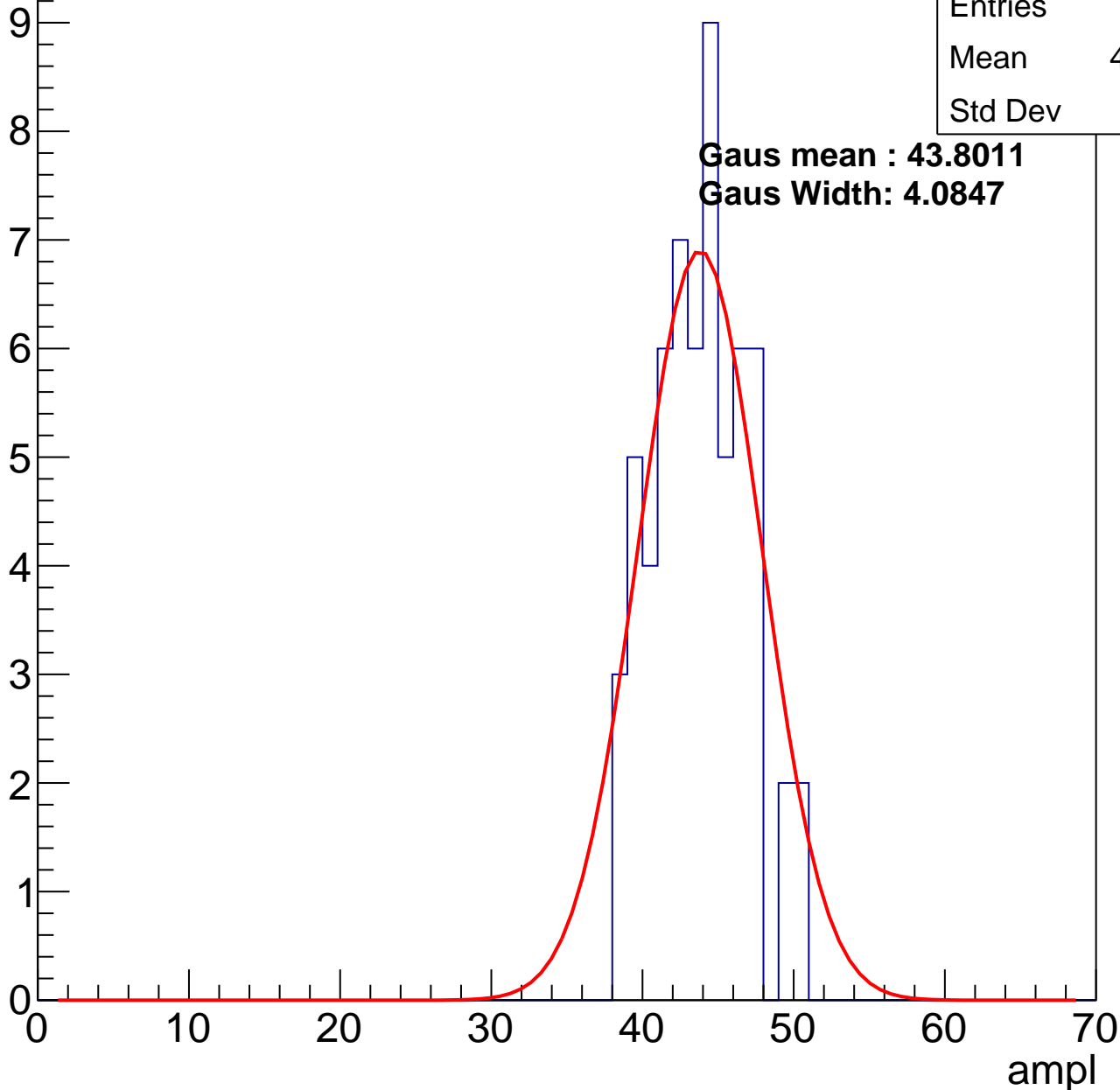
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	43.34
Std Dev	3.04

**Gaus mean : 43.8011**

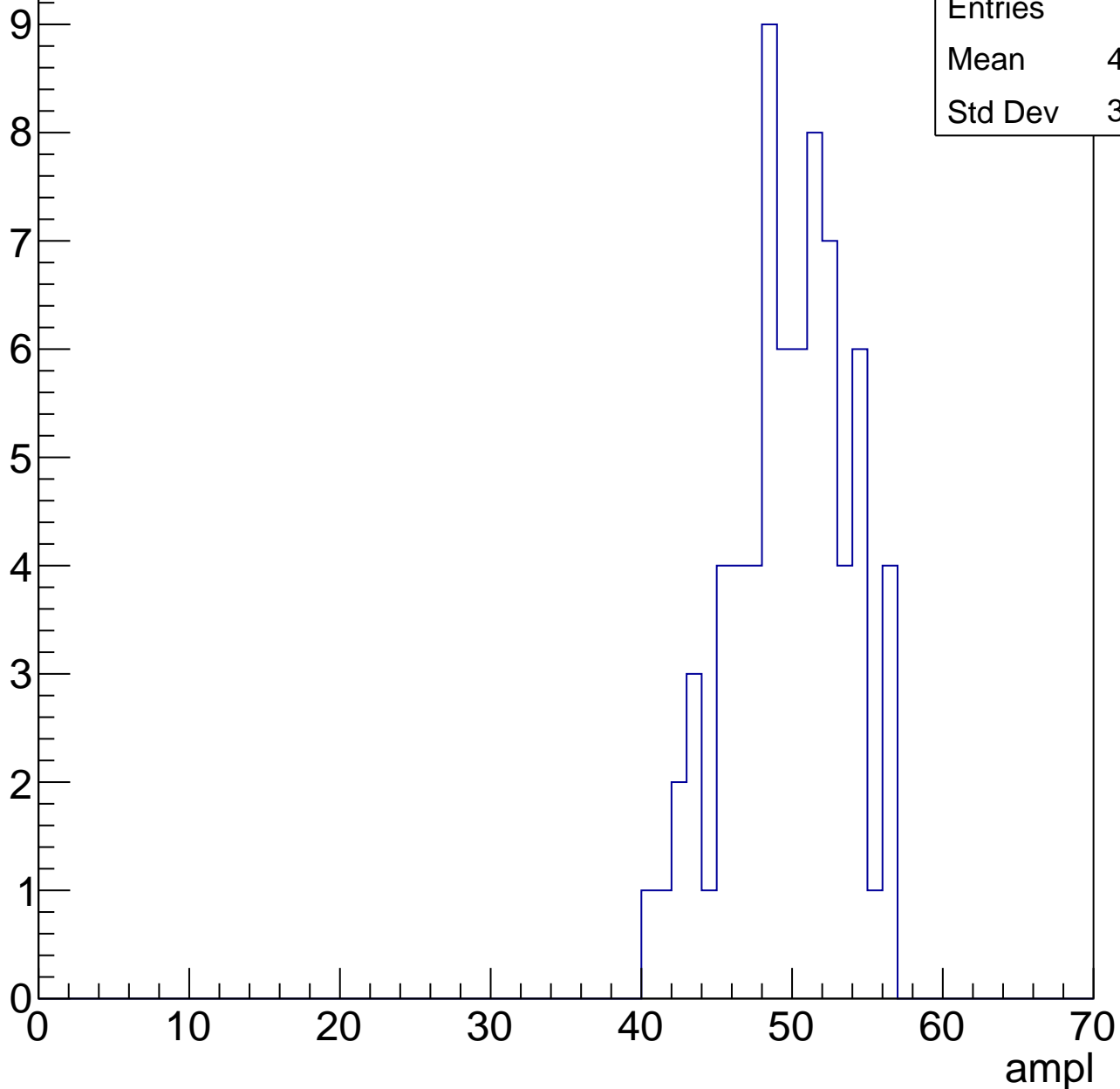
**Gaus Width: 4.0847**



# B1L101S, U9-ch95, adc3

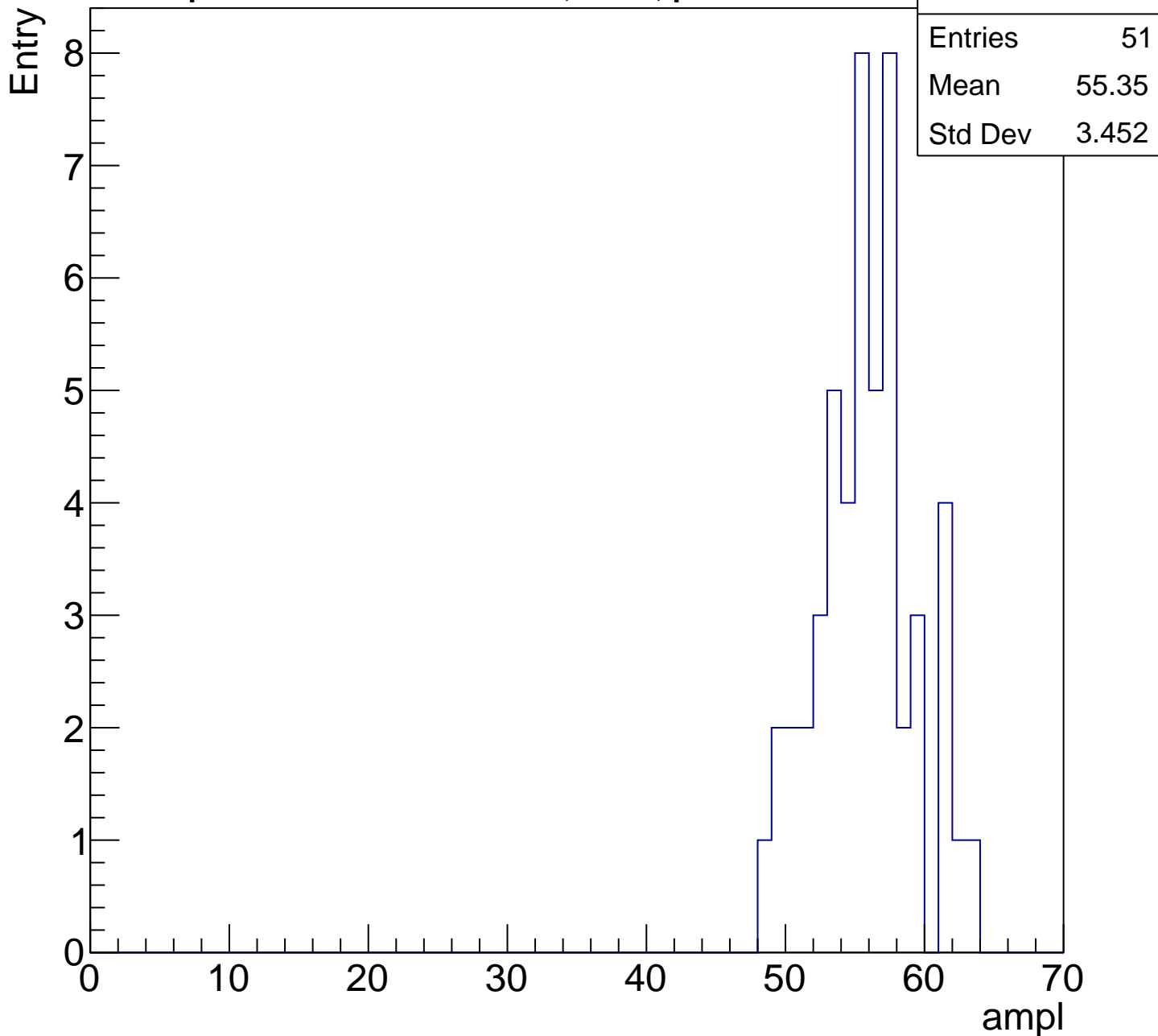
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

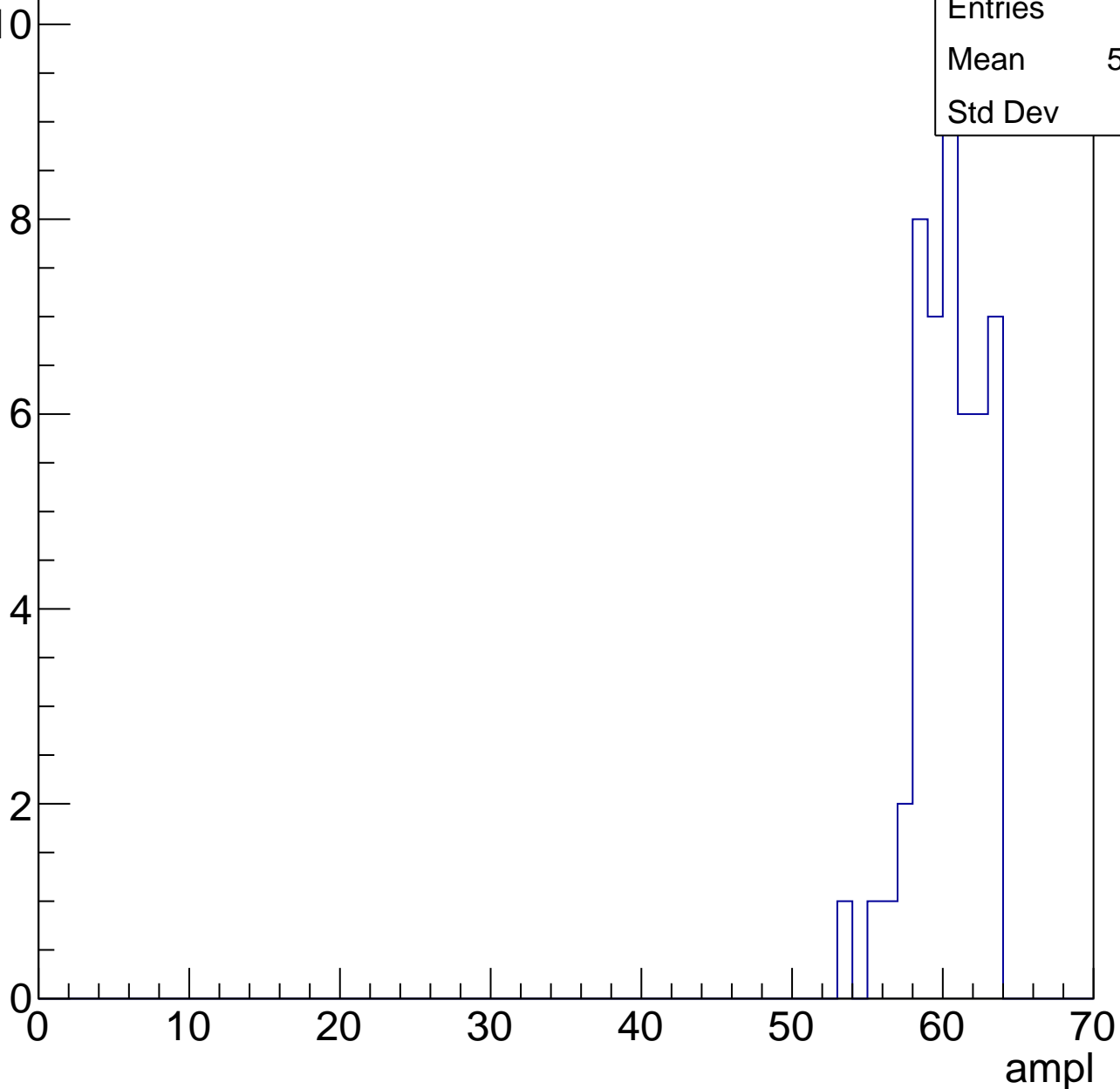


# B1L101S, U9-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

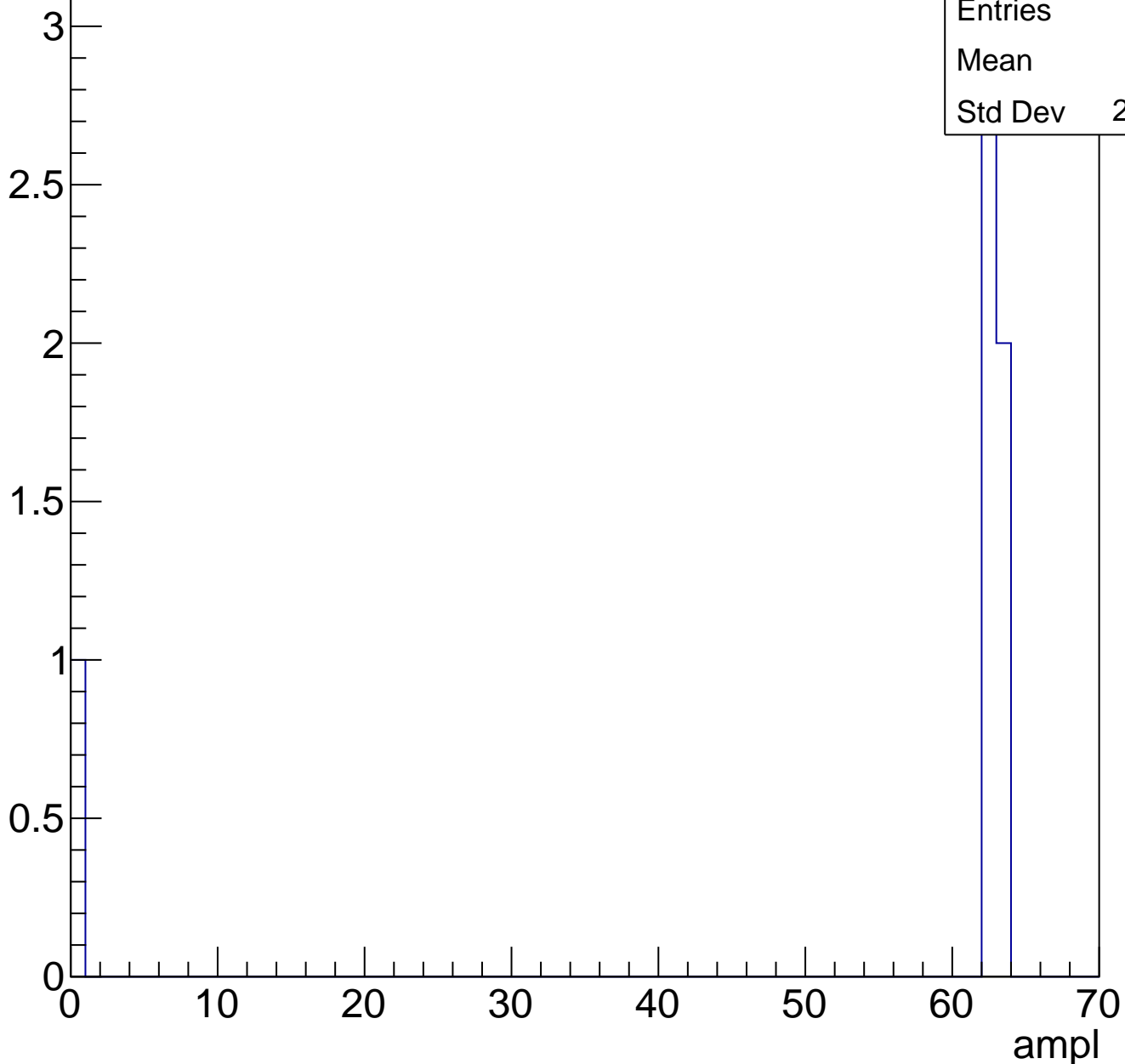
Entries	49
Mean	59.88
Std Dev	2.21



# B1L101S, U9-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U9-ch96, adc0

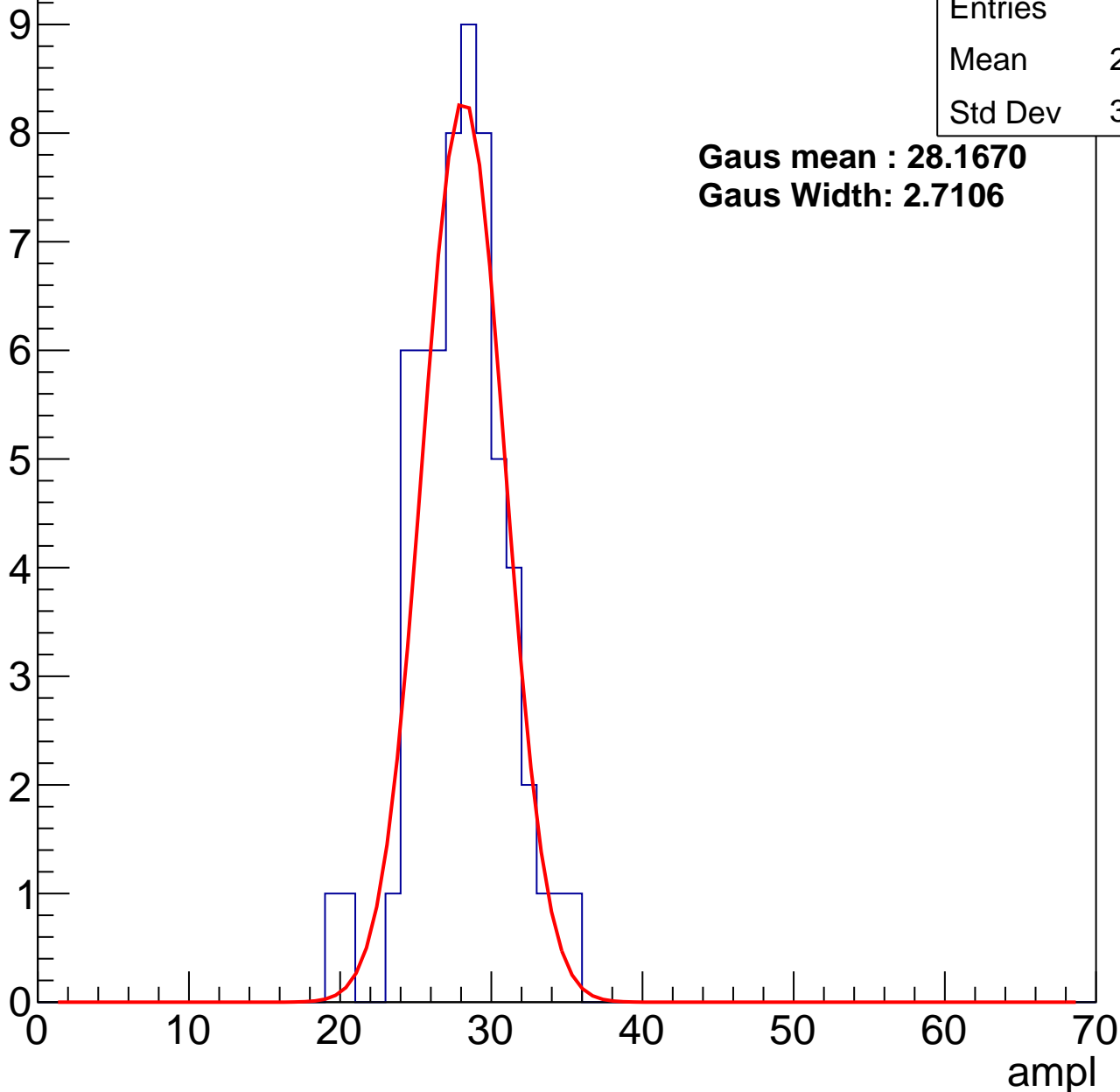
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	27.53
Std Dev	3.014

**Gaus mean : 28.1670**

**Gaus Width: 2.7106**



# B1L101S, U9-ch96, adc1

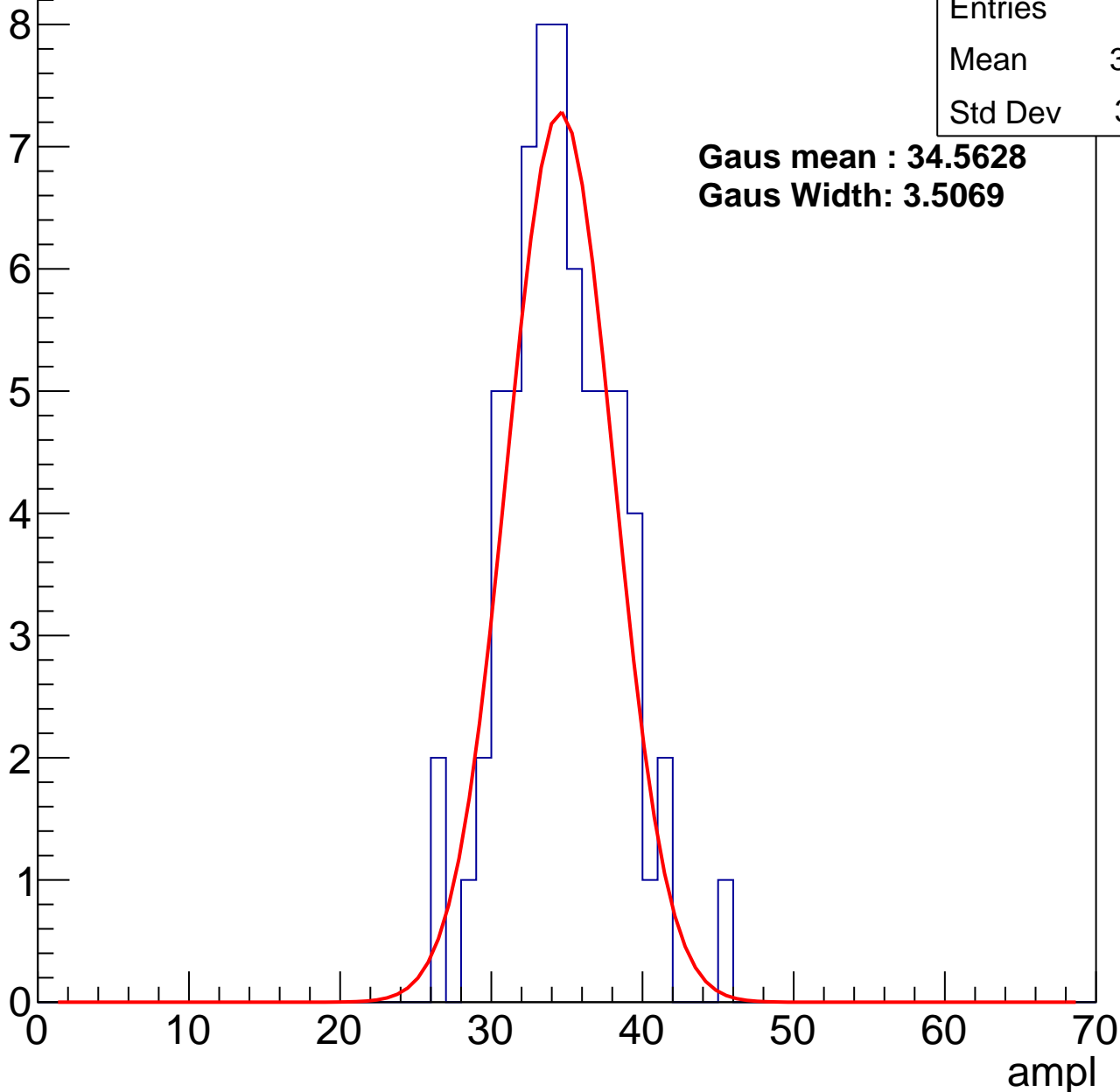
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	34.19
Std Dev	3.621

**Gaus mean : 34.5628**

**Gaus Width: 3.5069**



# B1L101S, U9-ch96, adc2

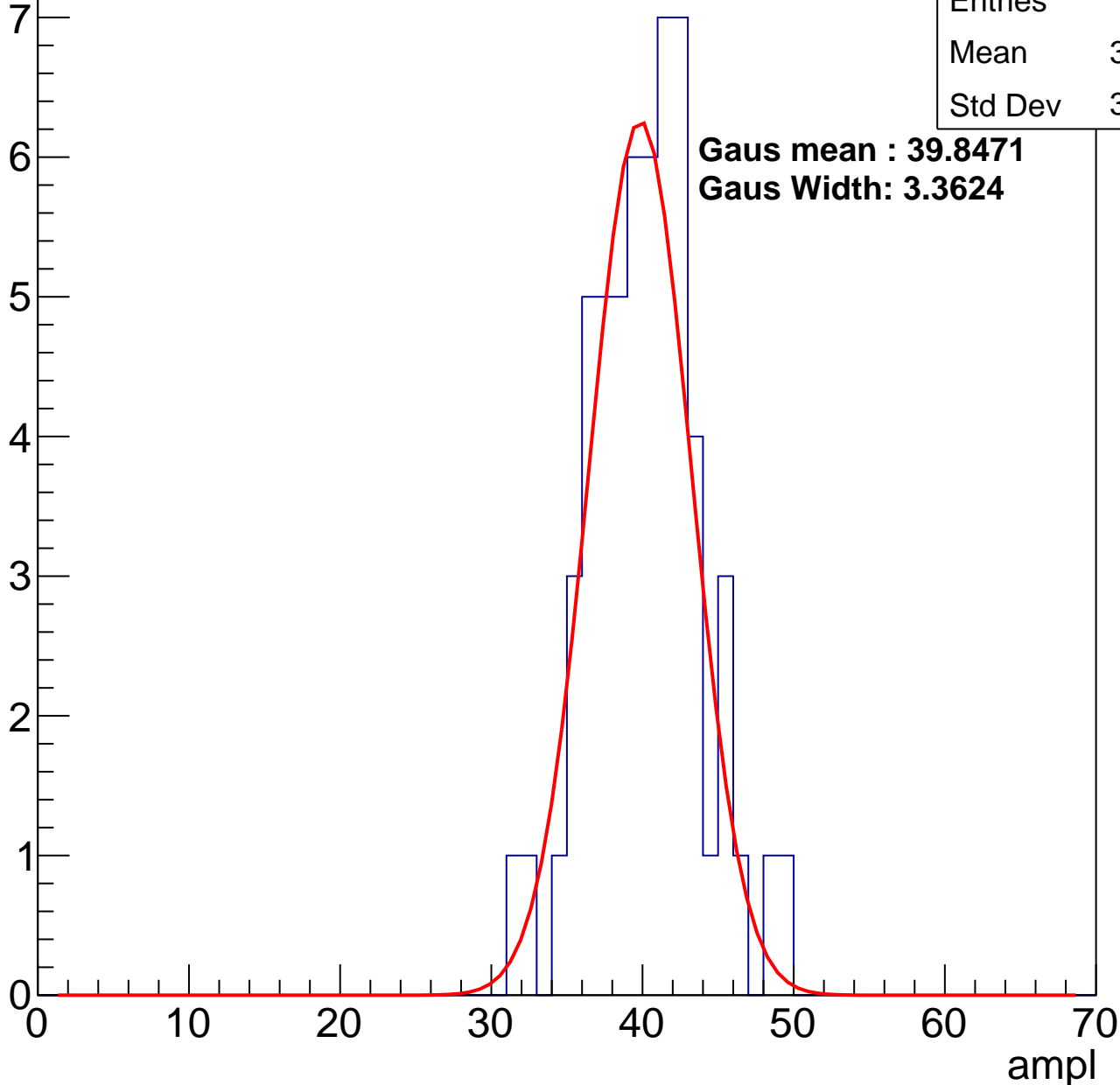
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	39.76
Std Dev	3.588

**Gaus mean : 39.8471**

**Gaus Width: 3.3624**

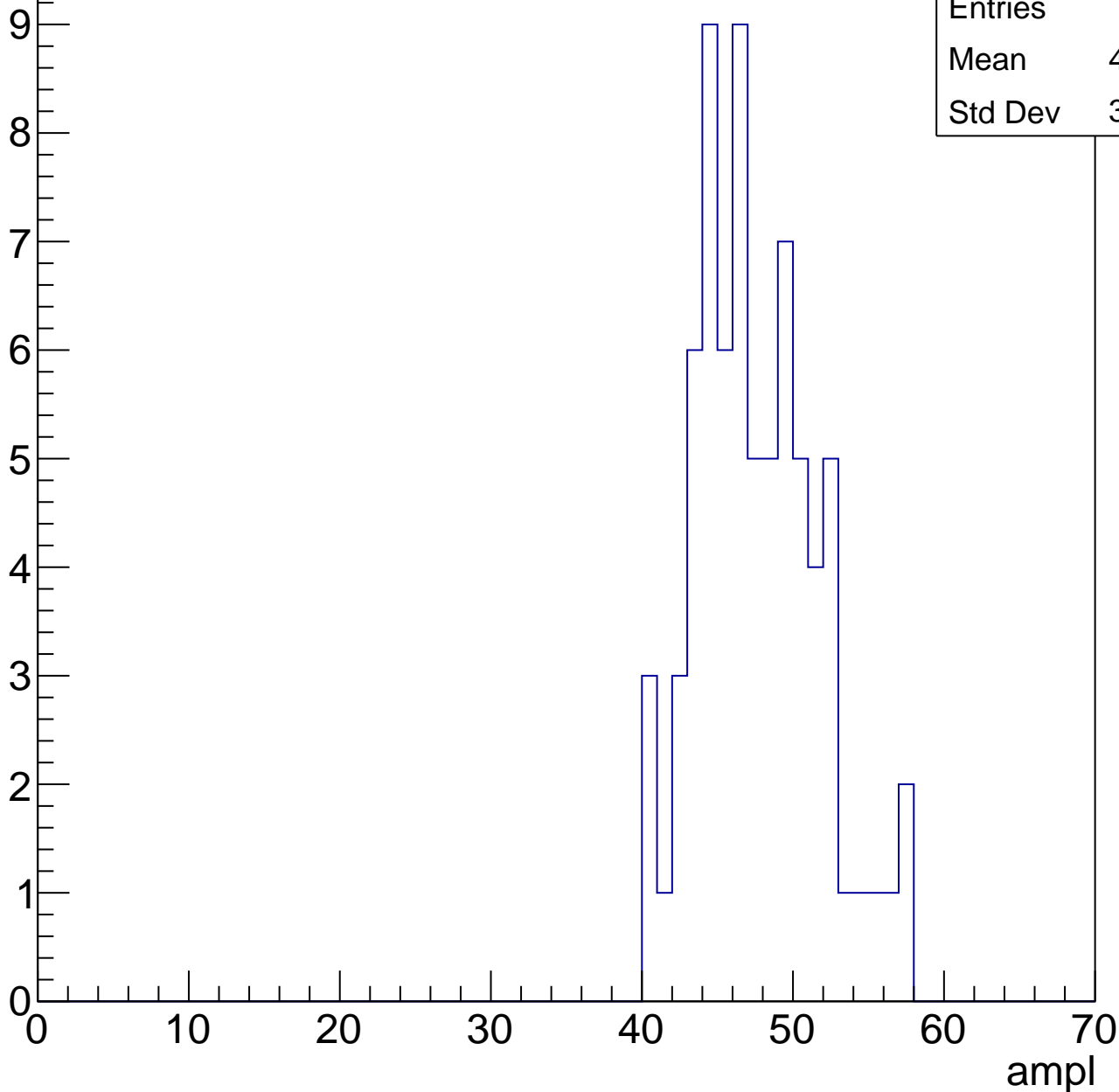


# B1L101S, U9-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	47.15
Std Dev	3.965

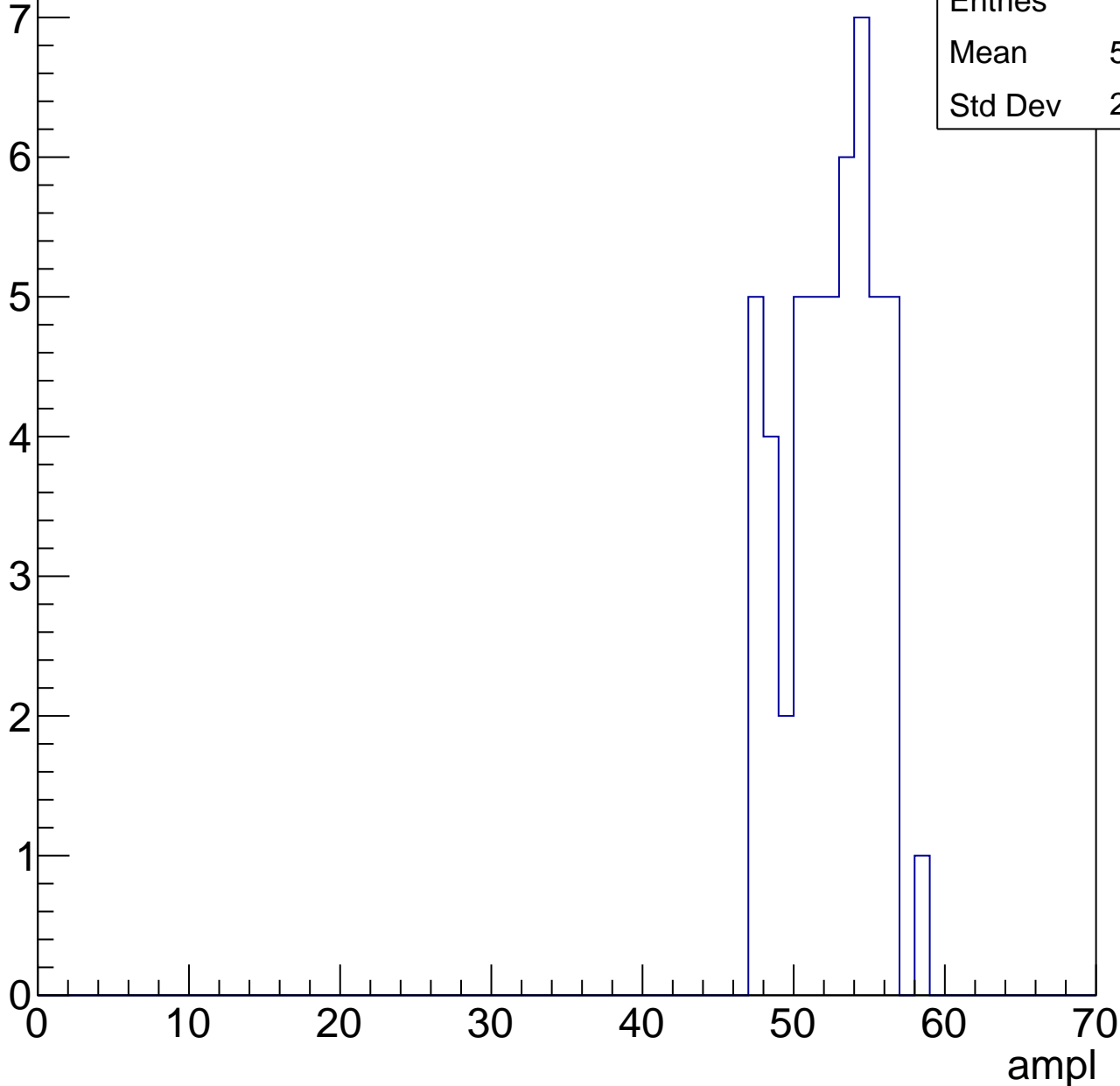


# B1L101S, U9-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	51.98
Std Dev	2.922

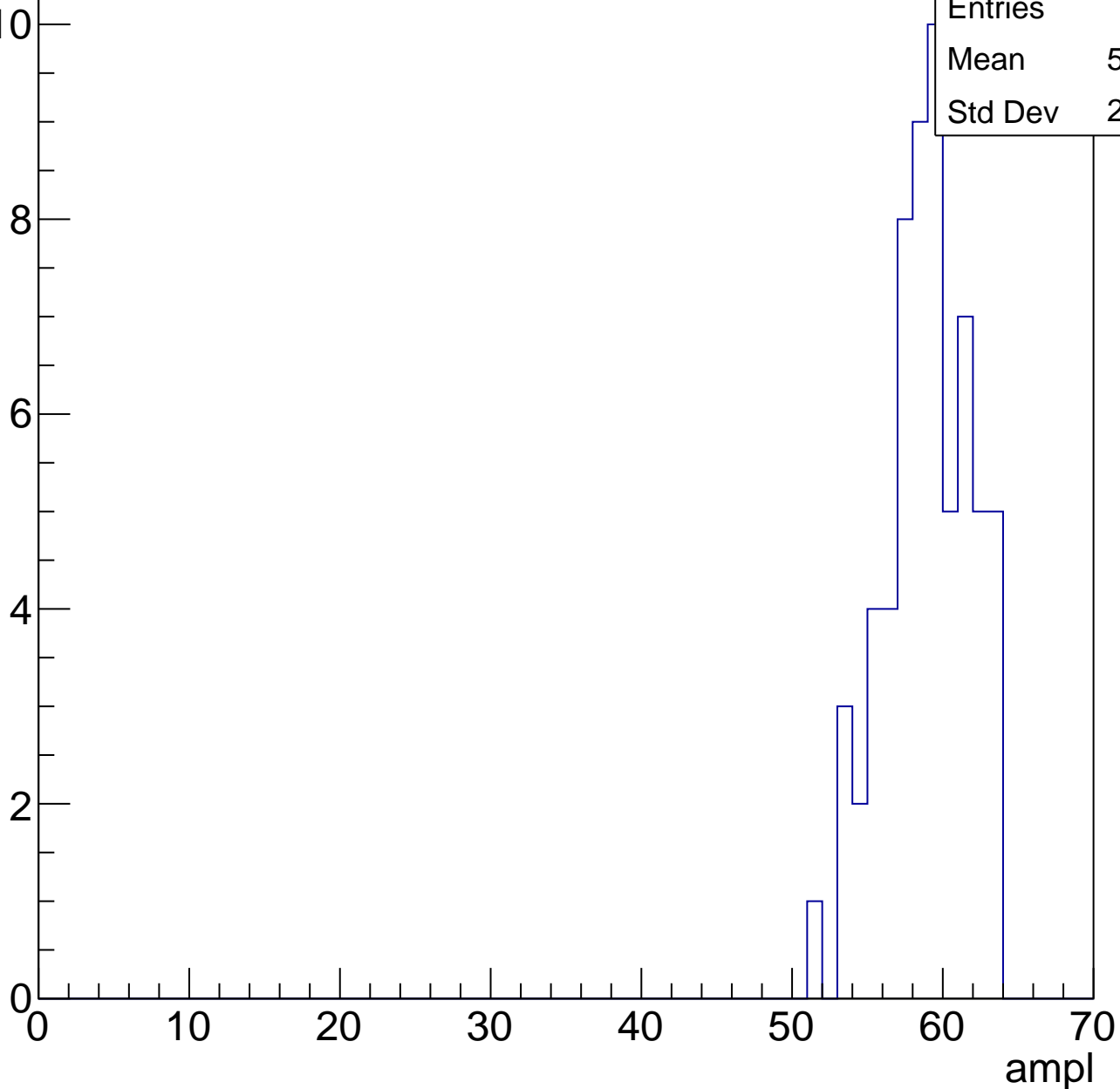


# B1L101S, U9-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	58.44
Std Dev	2.822

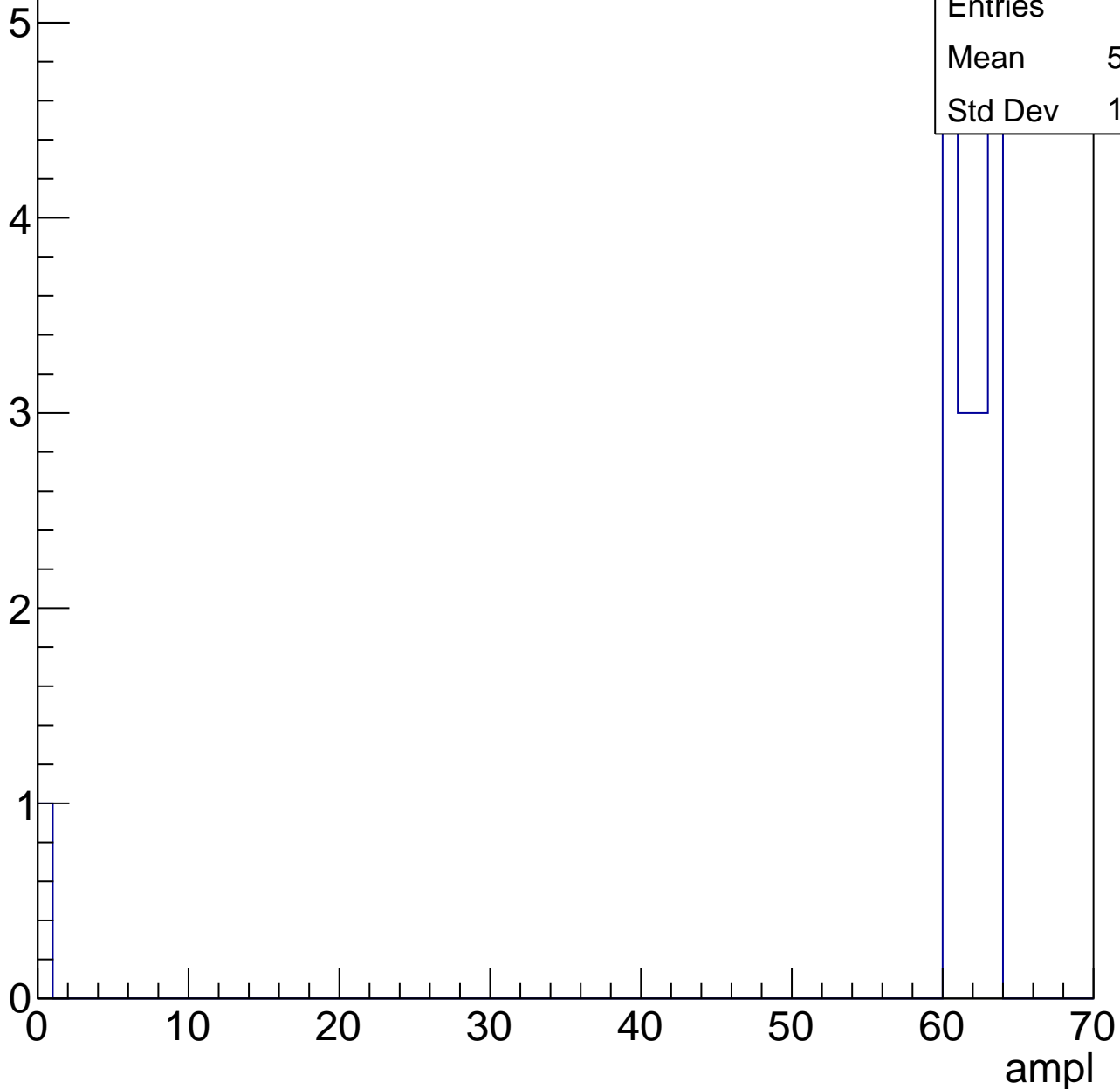


# B1L101S, U9-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	17
Mean	57.88
Std Dev	14.52





# B1L101S, U9-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	62
Std Dev	0

0 10 20 30 40 50 60 70

ampl

# B1L101S, U9-ch97, adc0

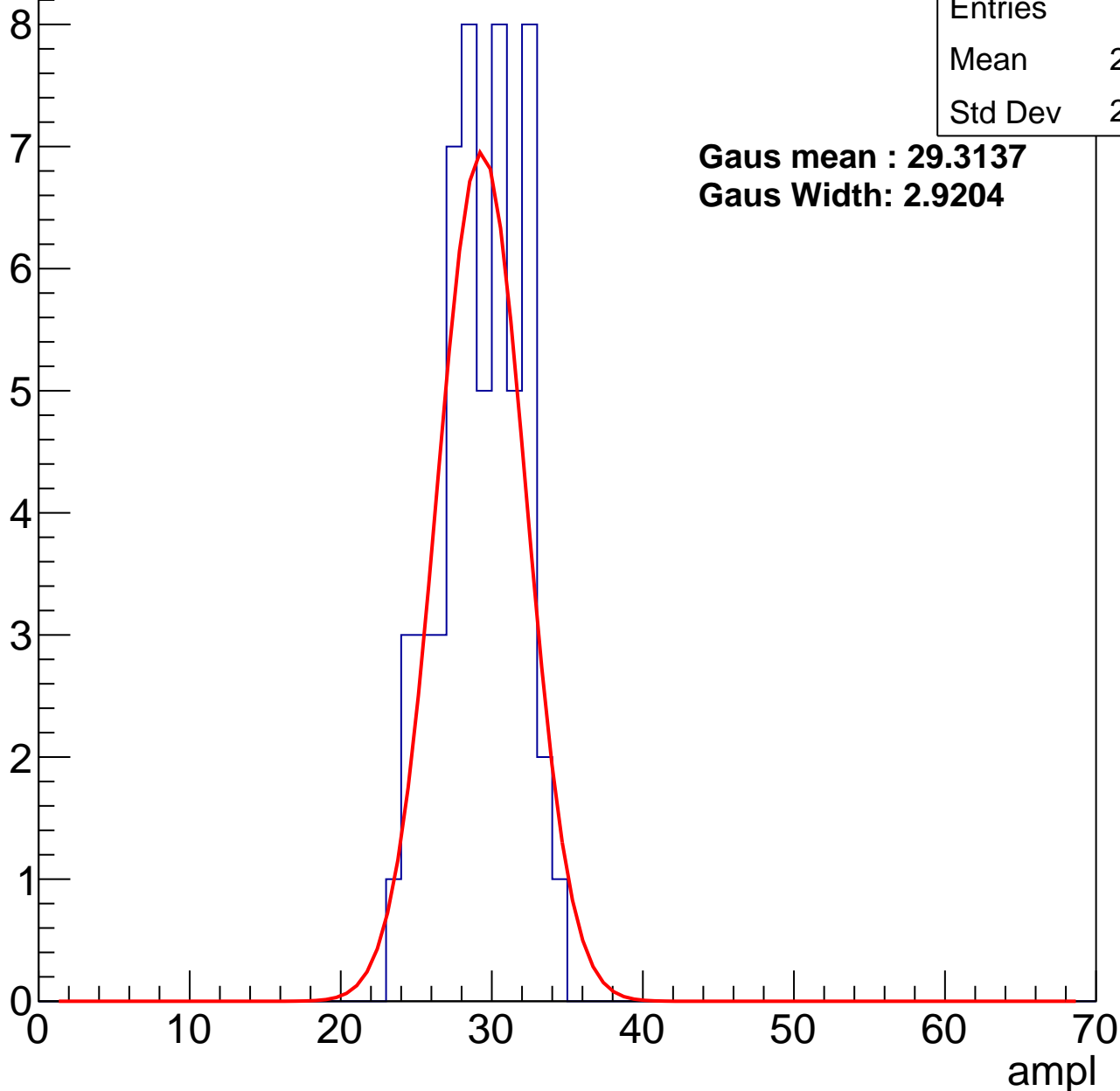
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	28.83
Std Dev	2.644

**Gaus mean : 29.3137**

**Gaus Width: 2.9204**



# B1L101S, U9-ch97, adc1

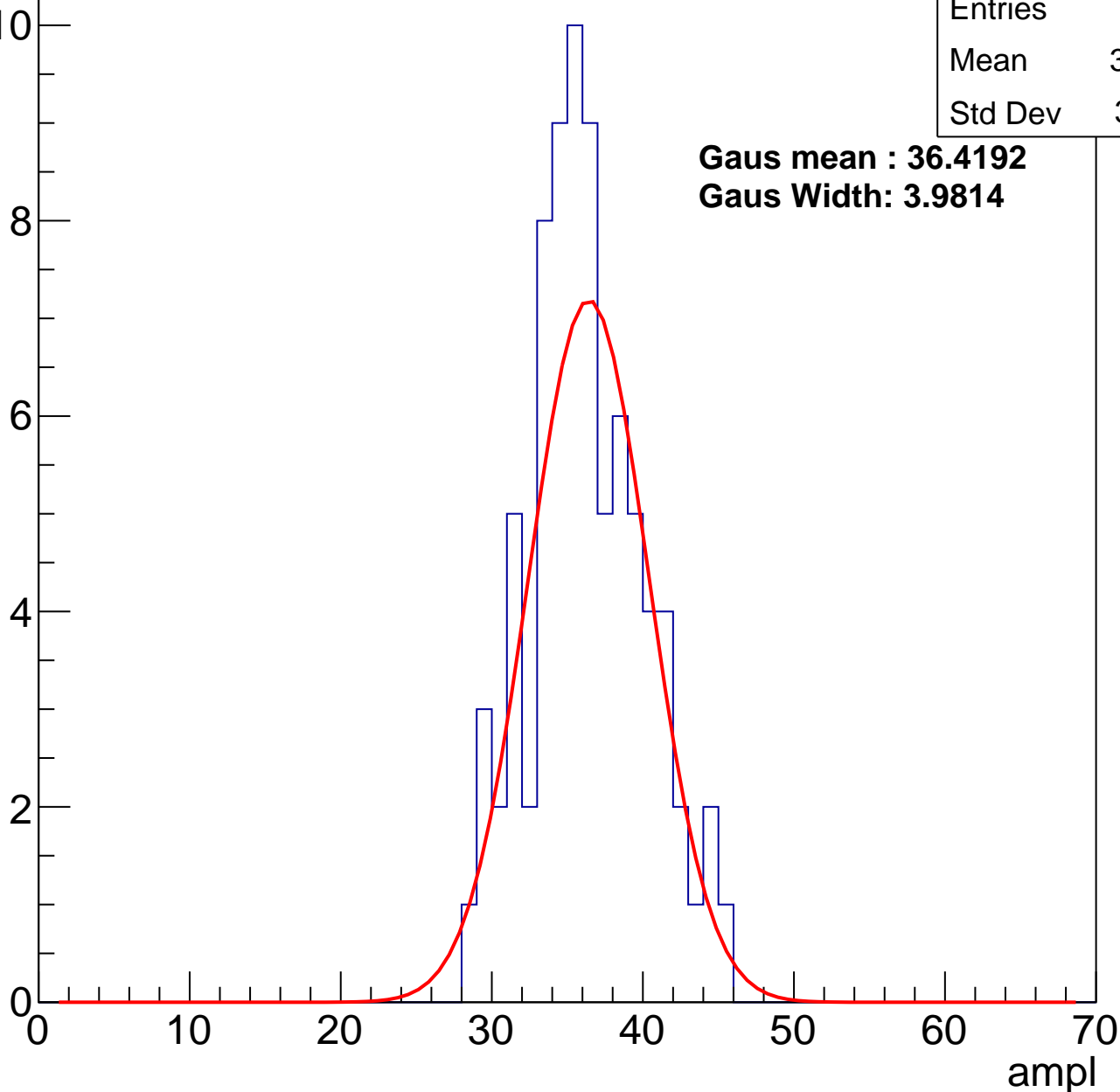
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	35.82
Std Dev	3.771

**Gaus mean : 36.4192**

**Gaus Width: 3.9814**

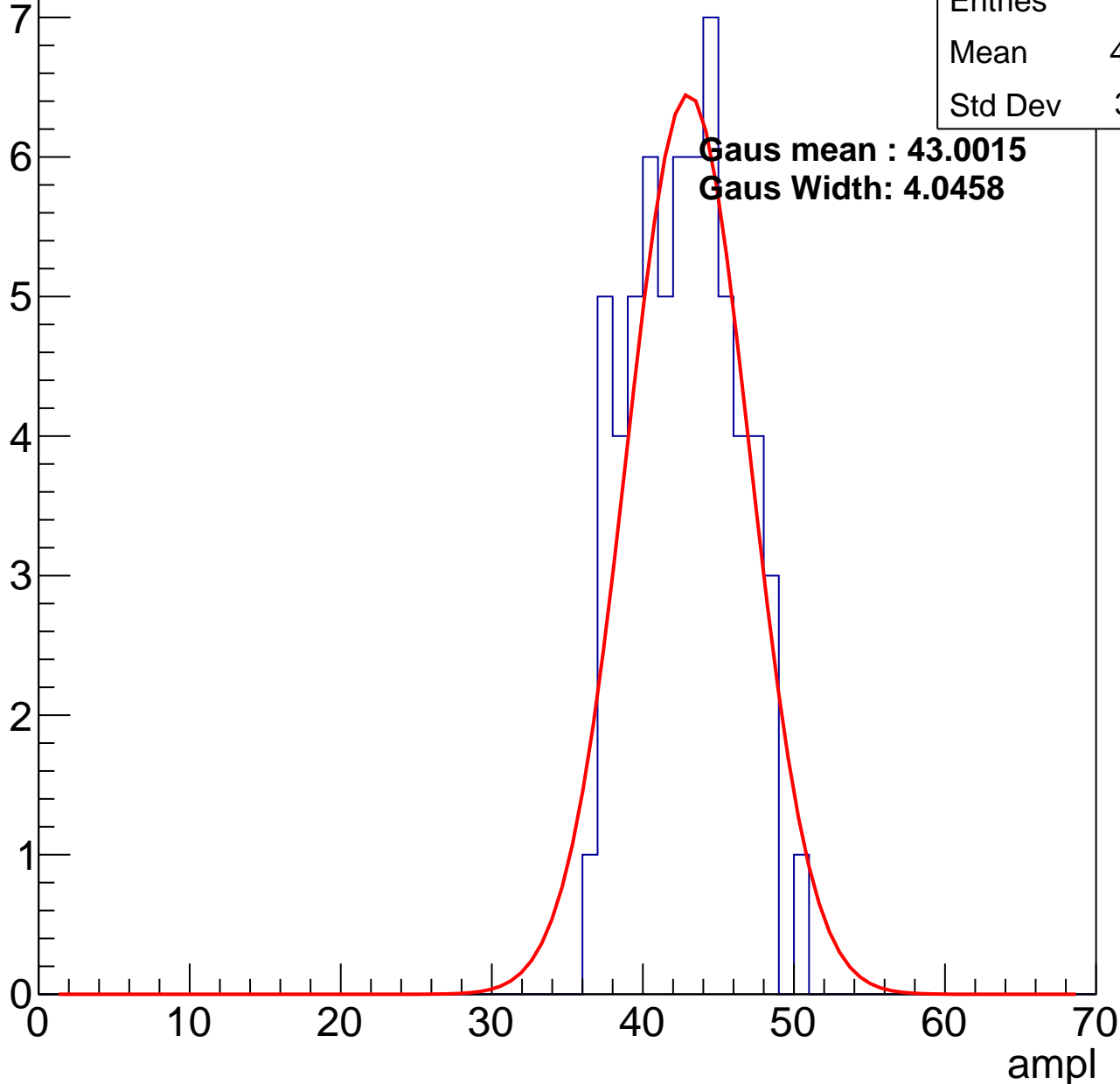


# B1L101S, U9-ch97, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	42.29
Std Dev	3.381

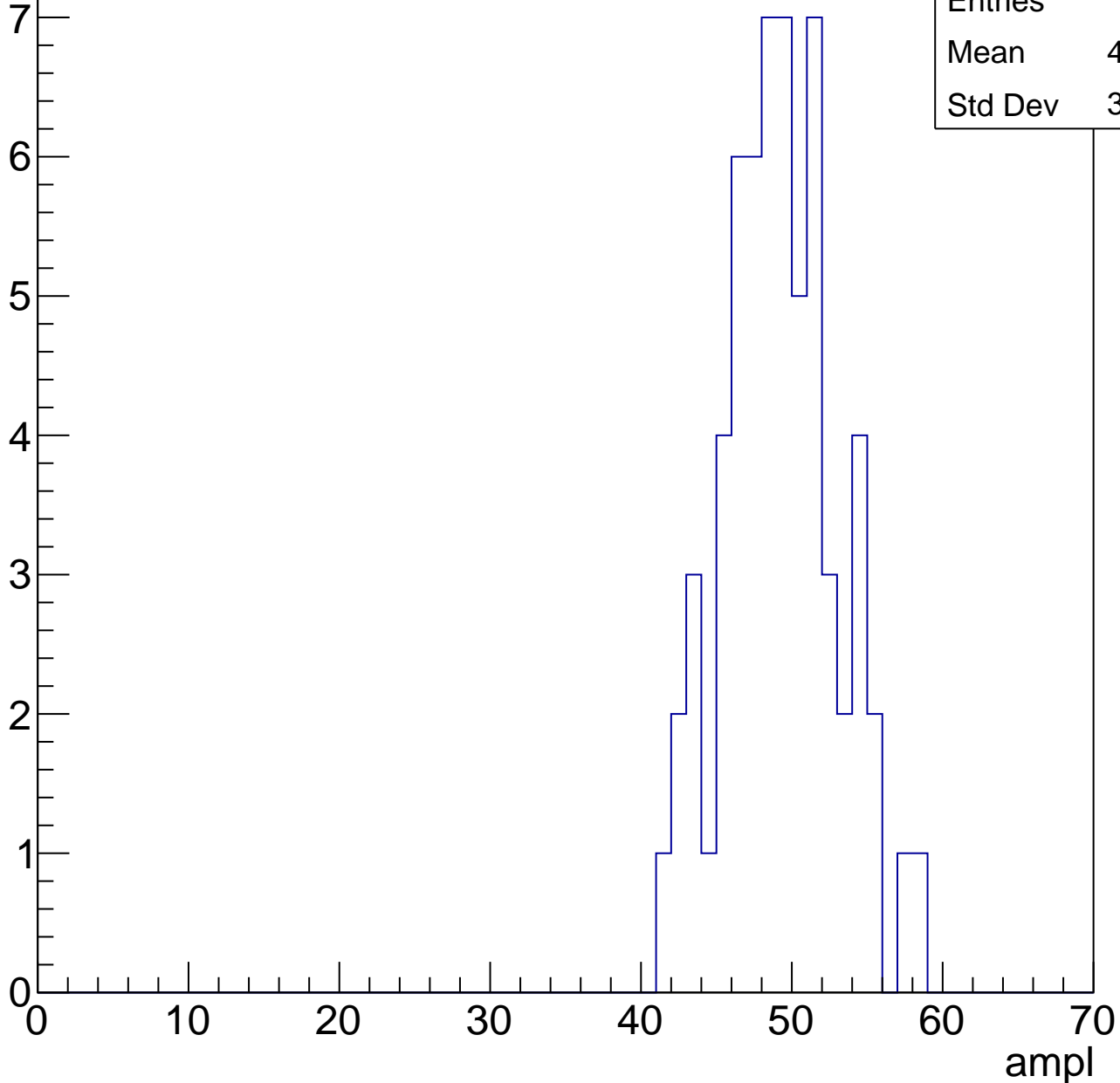


# B1L101S, U9-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	48.79
Std Dev	3.703

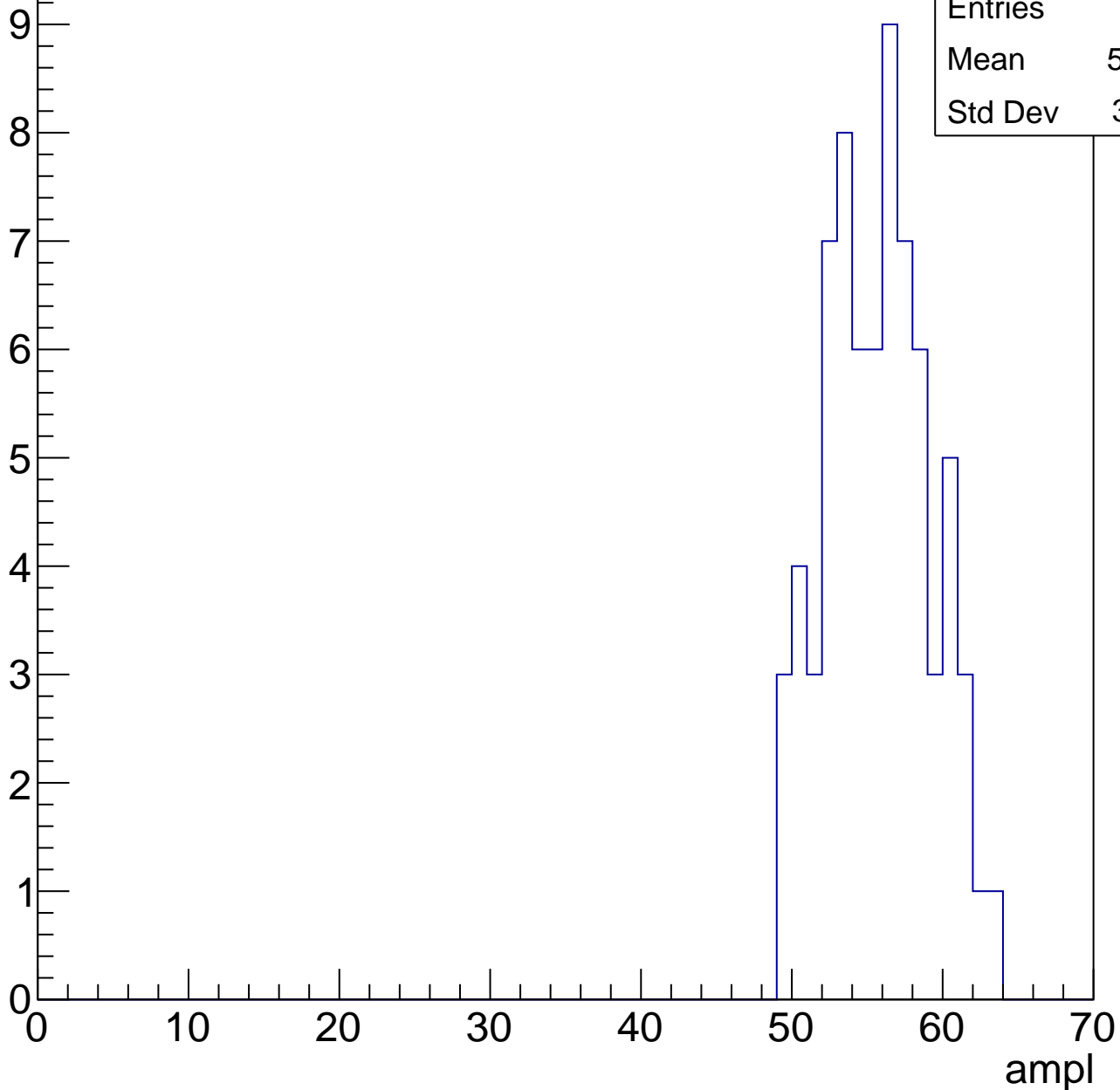


# B1L101S, U9-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	55.25
Std Dev	3.411

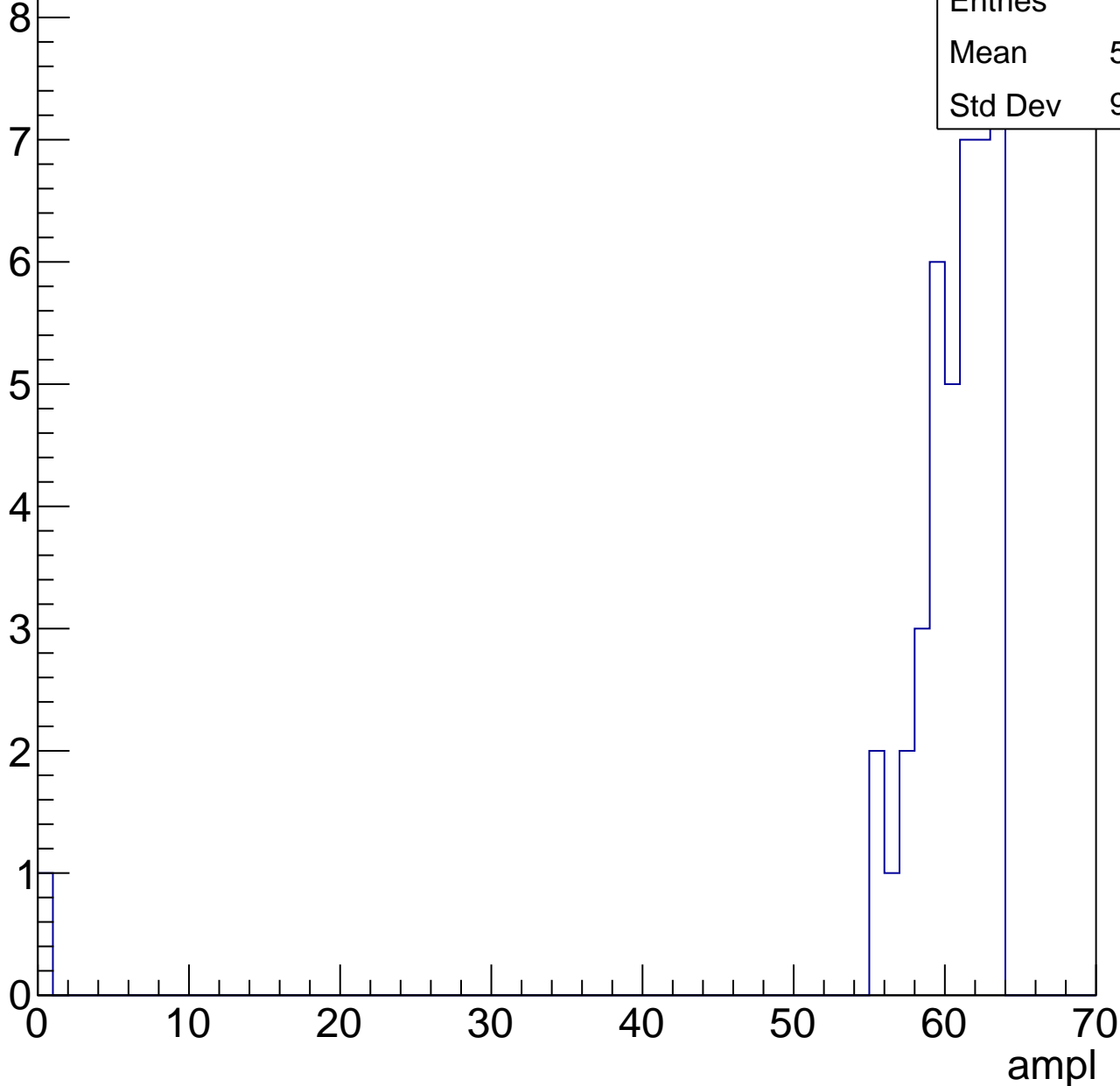


# B1L101S, U9-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	58.88
Std Dev	9.457



# B1L101S, U9-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

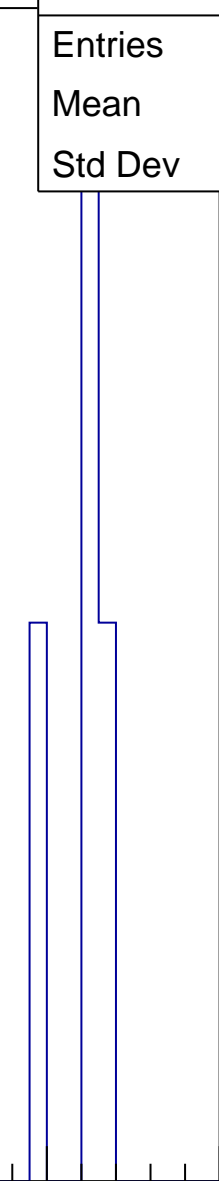
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	61.5
Std Dev	1.5

0 10 20 30 40 50 60 70

ampl





# B1L101S, U9-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch98, adc0

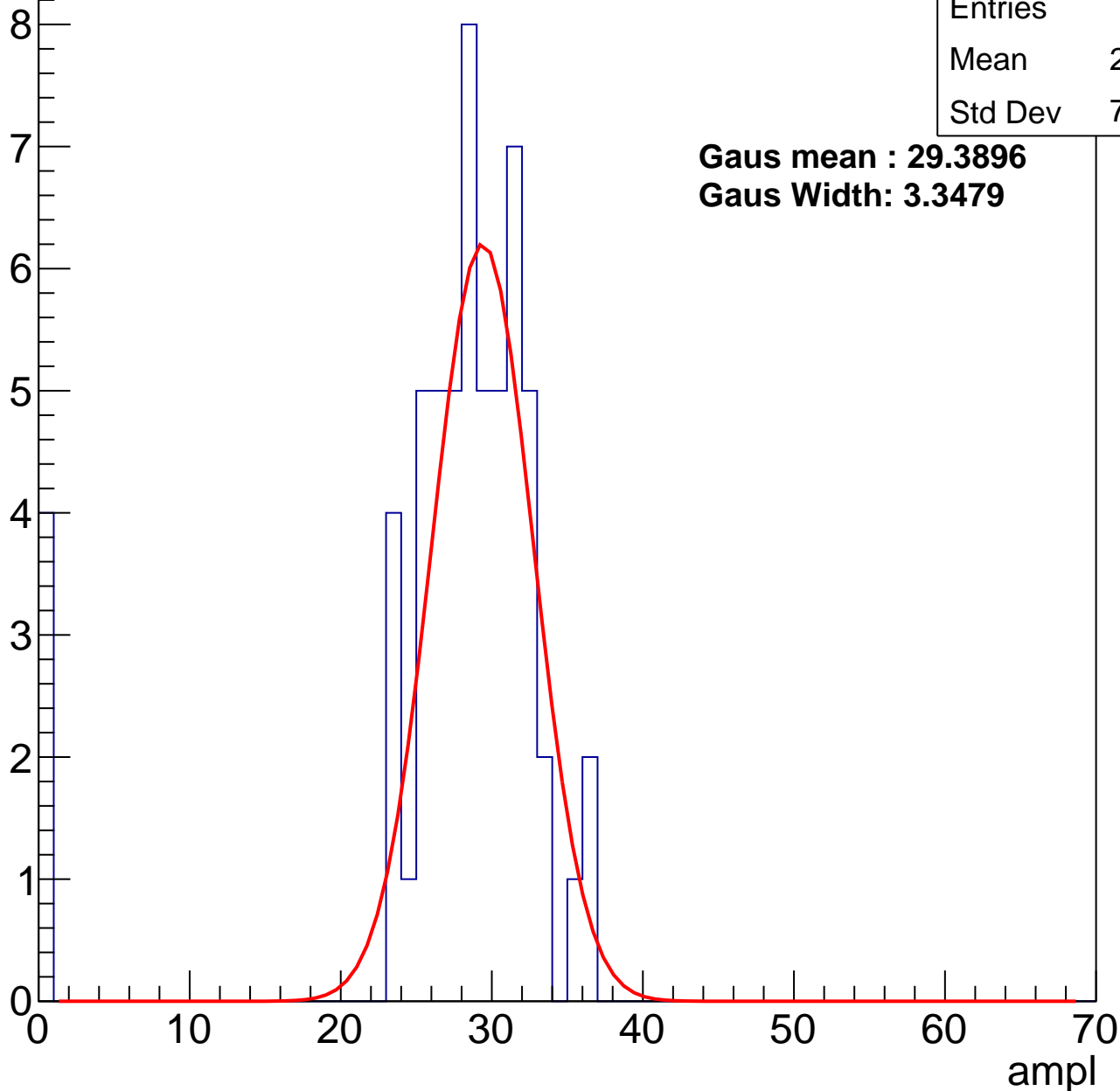
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	26.69
Std Dev	7.829

**Gaus mean : 29.3896**

**Gaus Width: 3.3479**



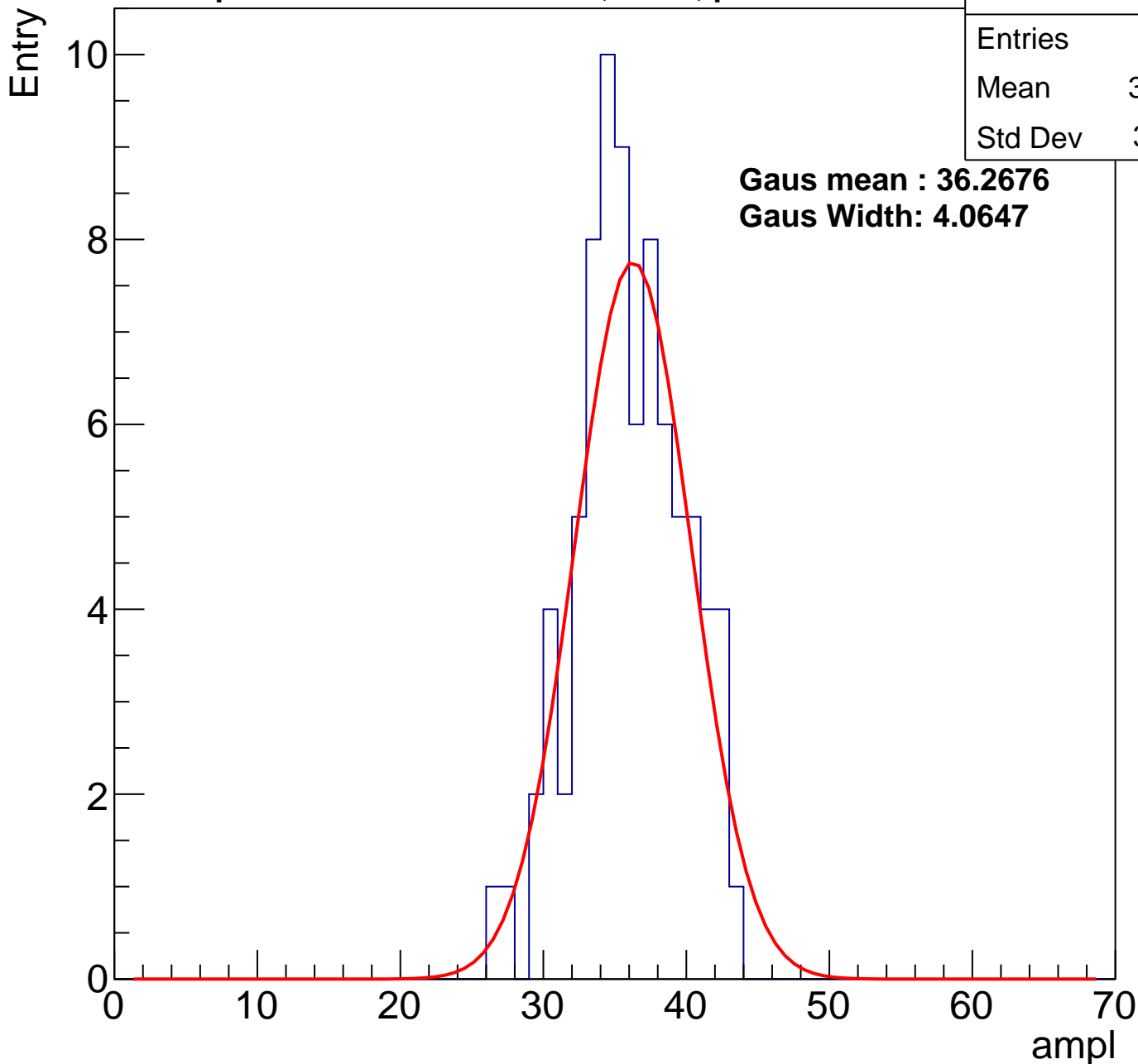
# B1L101S, U9-ch98, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	81
Mean	35.58
Std Dev	3.701

**Gaus mean : 36.2676**

**Gaus Width: 4.0647**



# B1L101S, U9-ch98, adc2

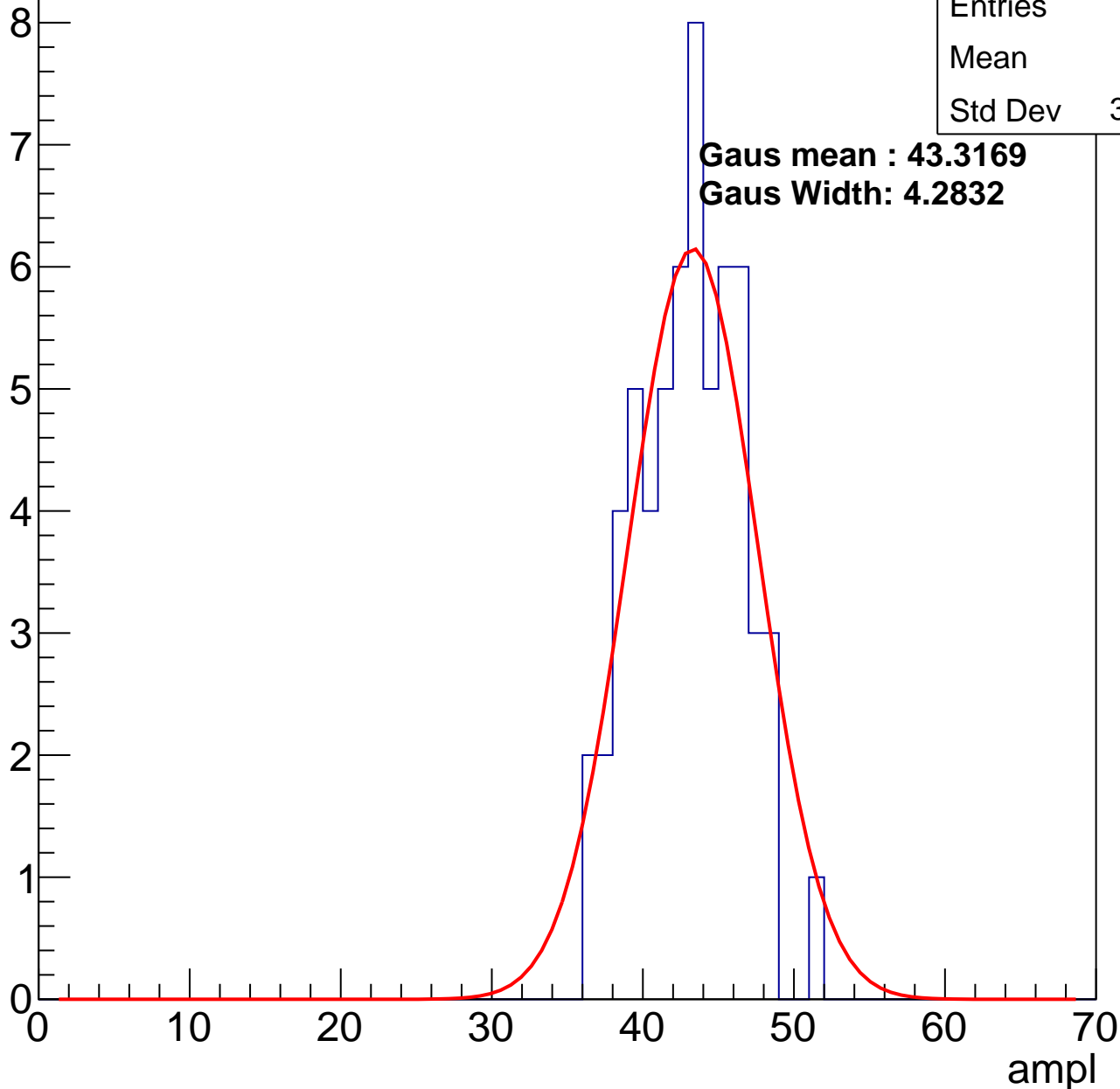
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	42.6
Std Dev	3.348

**Gaus mean : 43.3169**

**Gaus Width: 4.2832**

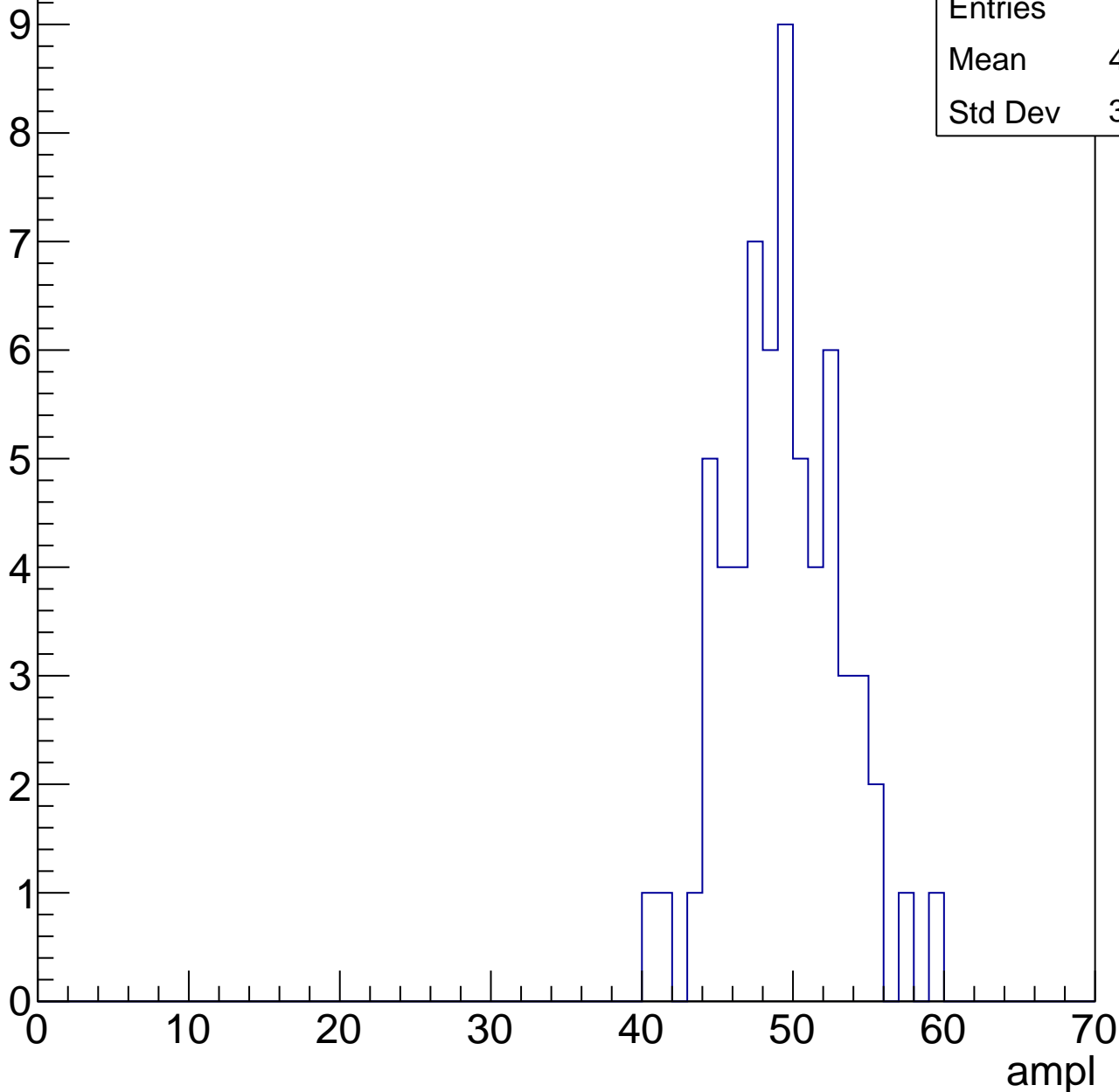


# B1L101S, U9-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	48.87
Std Dev	3.722

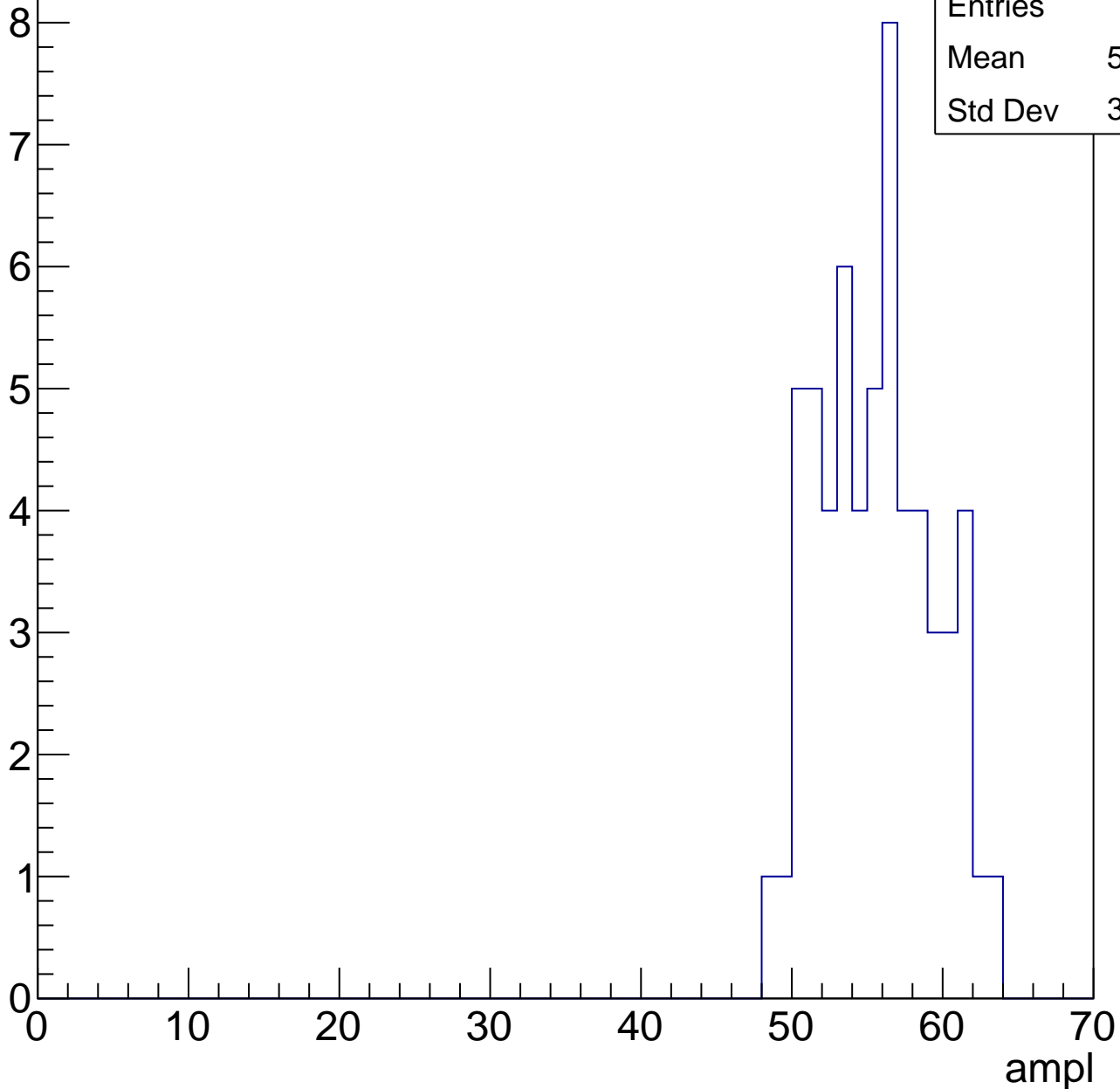


# B1L101S, U9-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	55.14
Std Dev	3.666

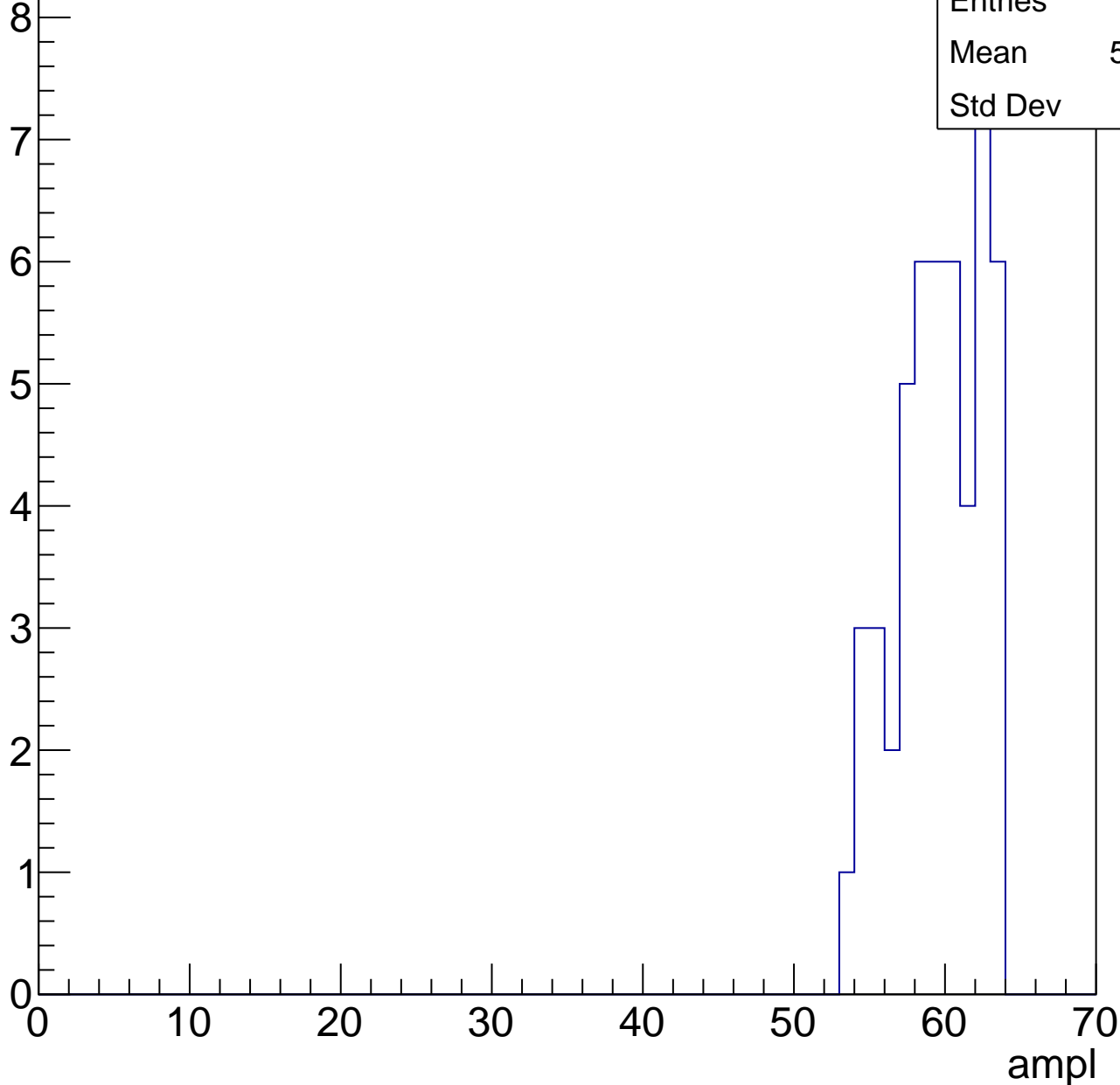


# B1L101S, U9-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

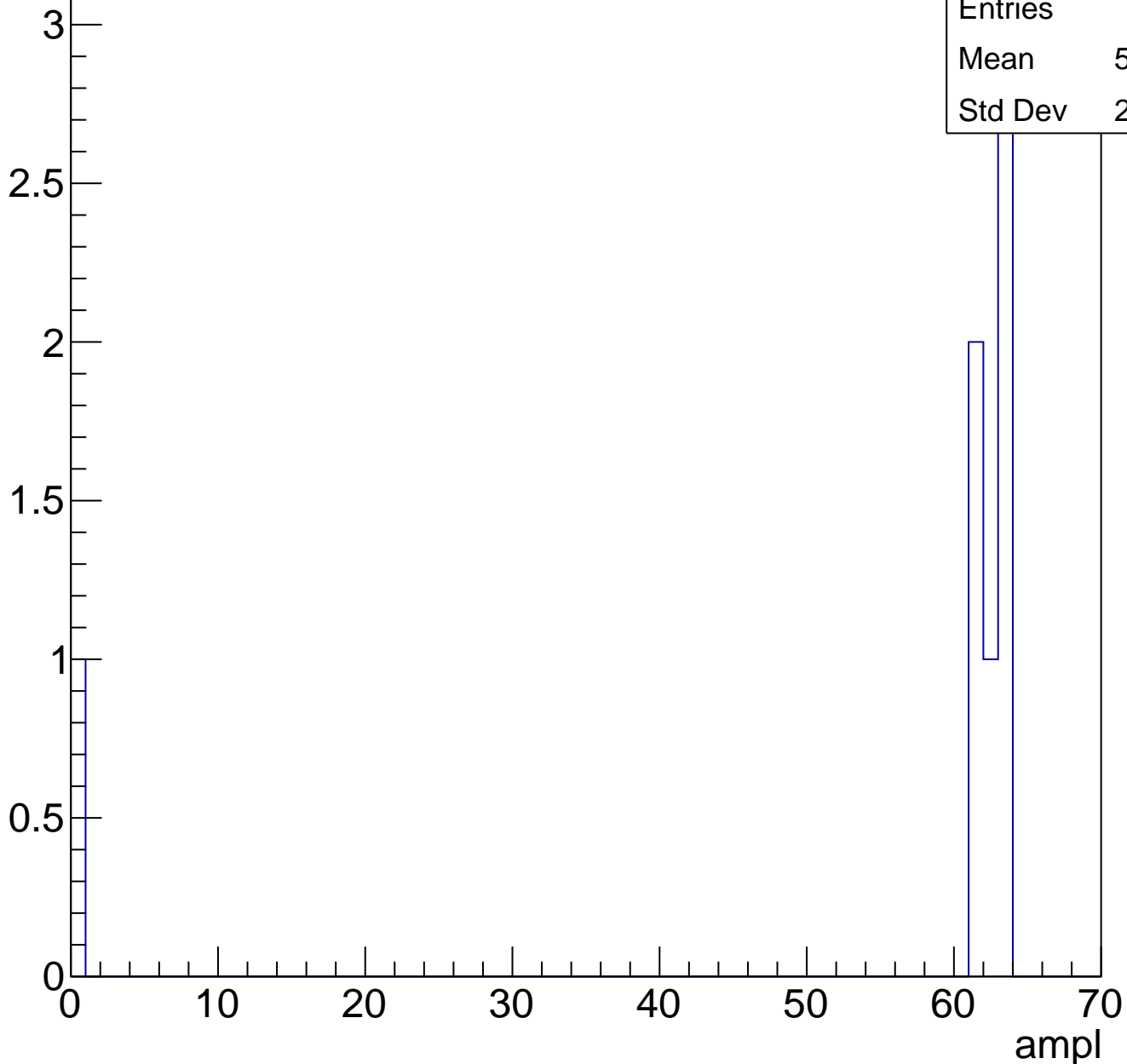
Entries	50
Mean	59.14
Std Dev	2.8



# B1L101S, U9-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



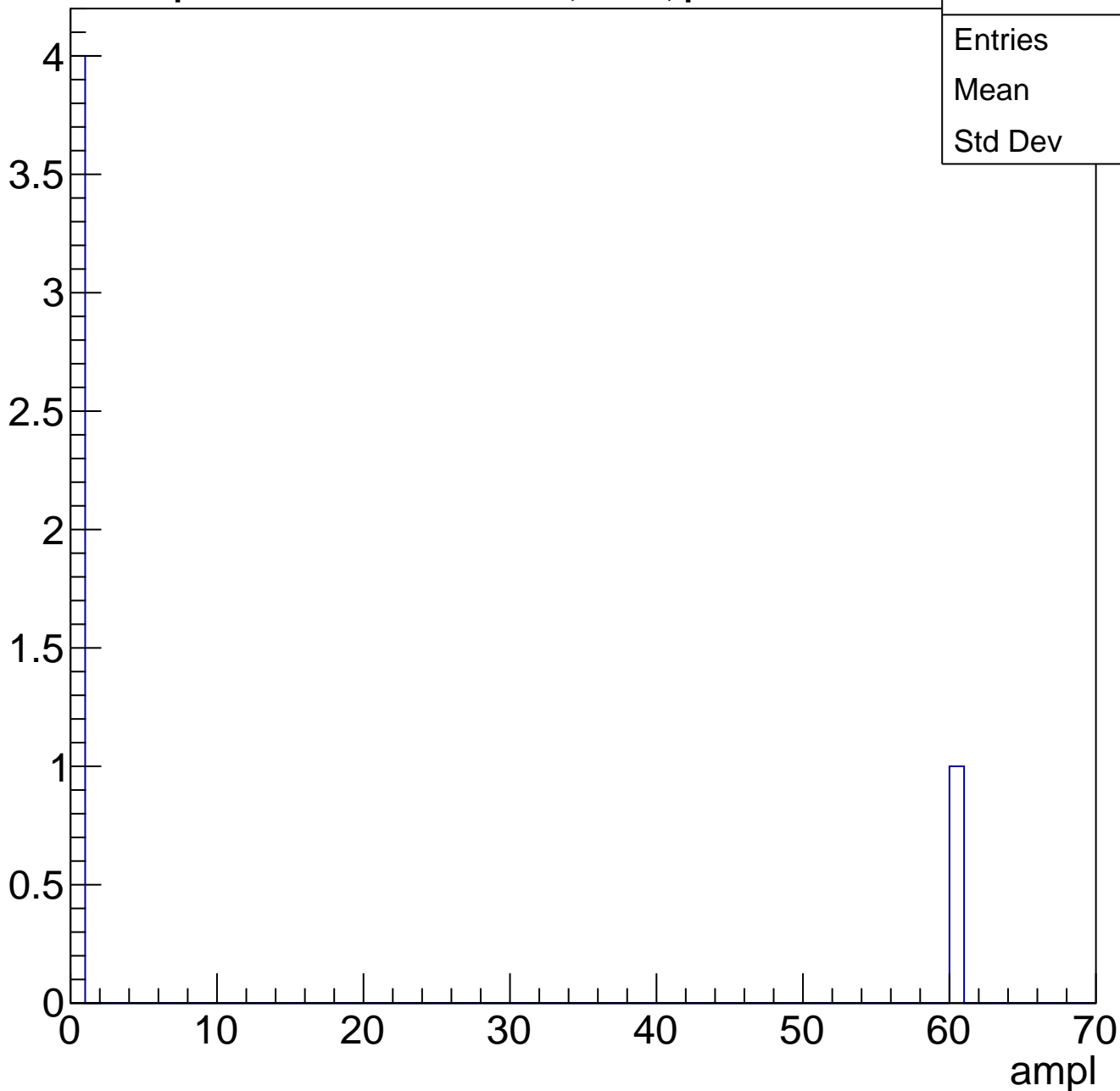
Entries	7
Mean	53.29
Std Dev	21.77



# B1L101S, U9-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch99, adc0

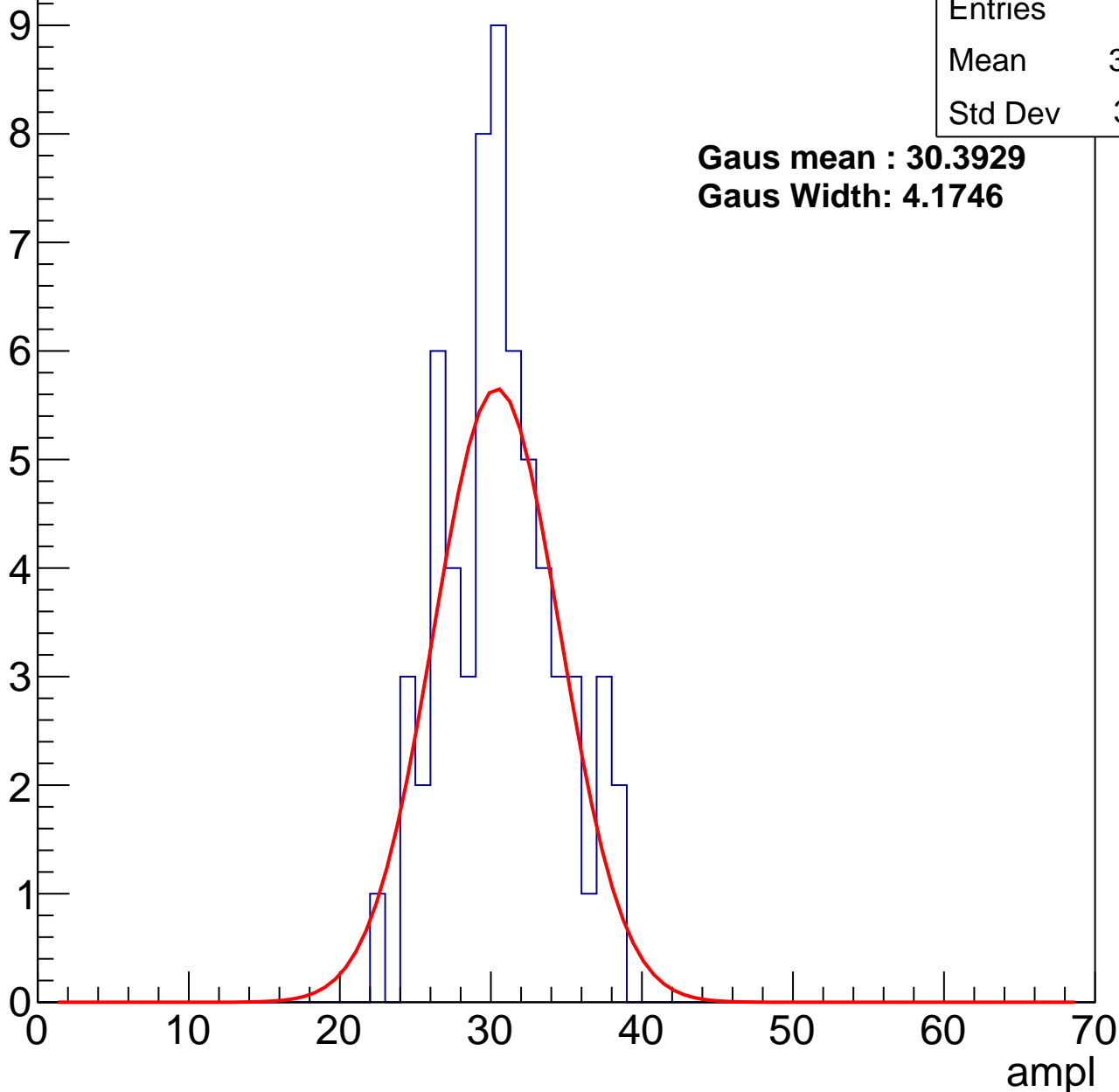
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	30.19
Std Dev	3.711

**Gaus mean : 30.3929**

**Gaus Width: 4.1746**



# B1L101S, U9-ch99, adc1

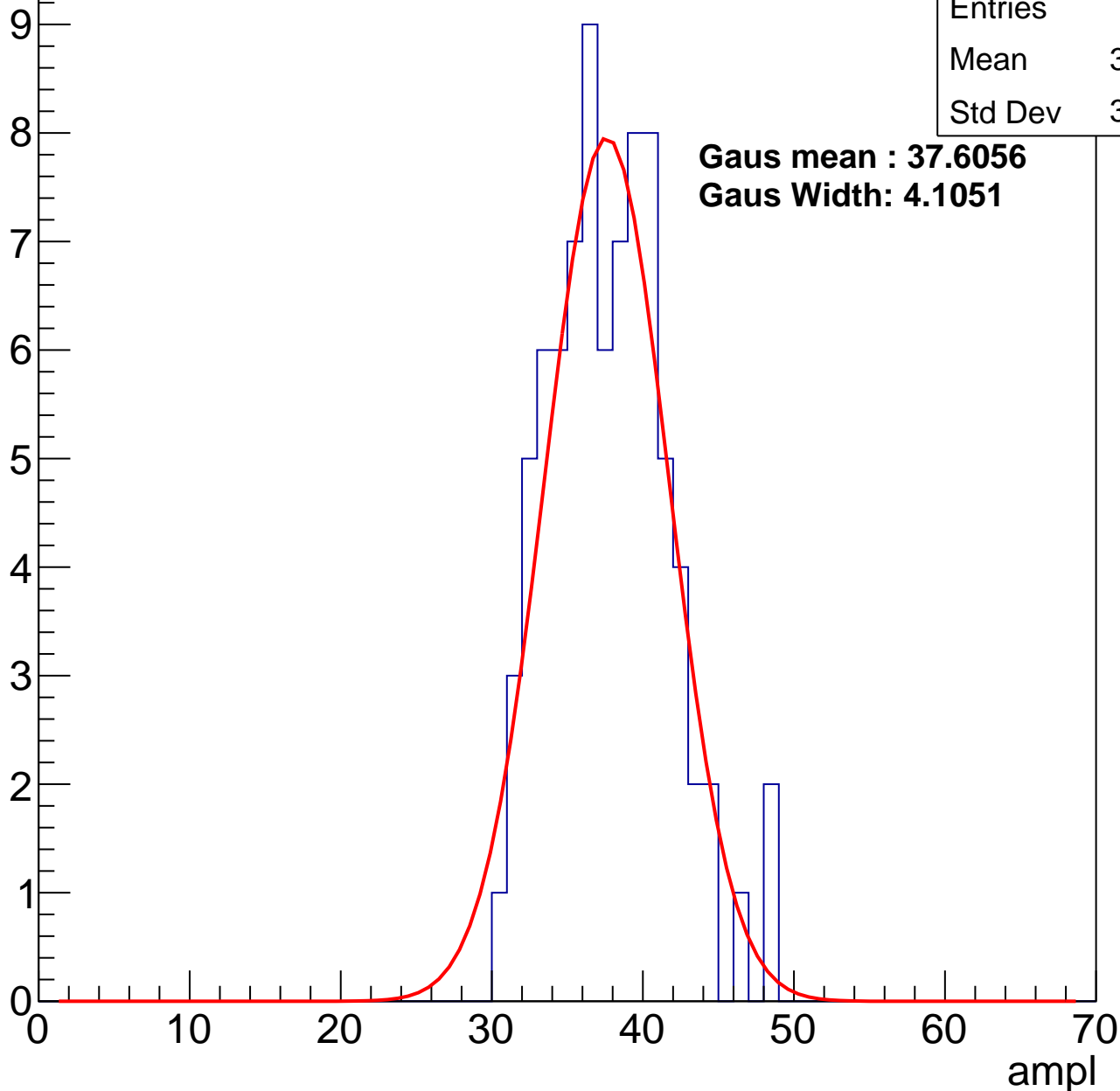
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	37.35
Std Dev	3.893

**Gaus mean : 37.6056**

**Gaus Width: 4.1051**



# B1L101S, U9-ch99, adc2

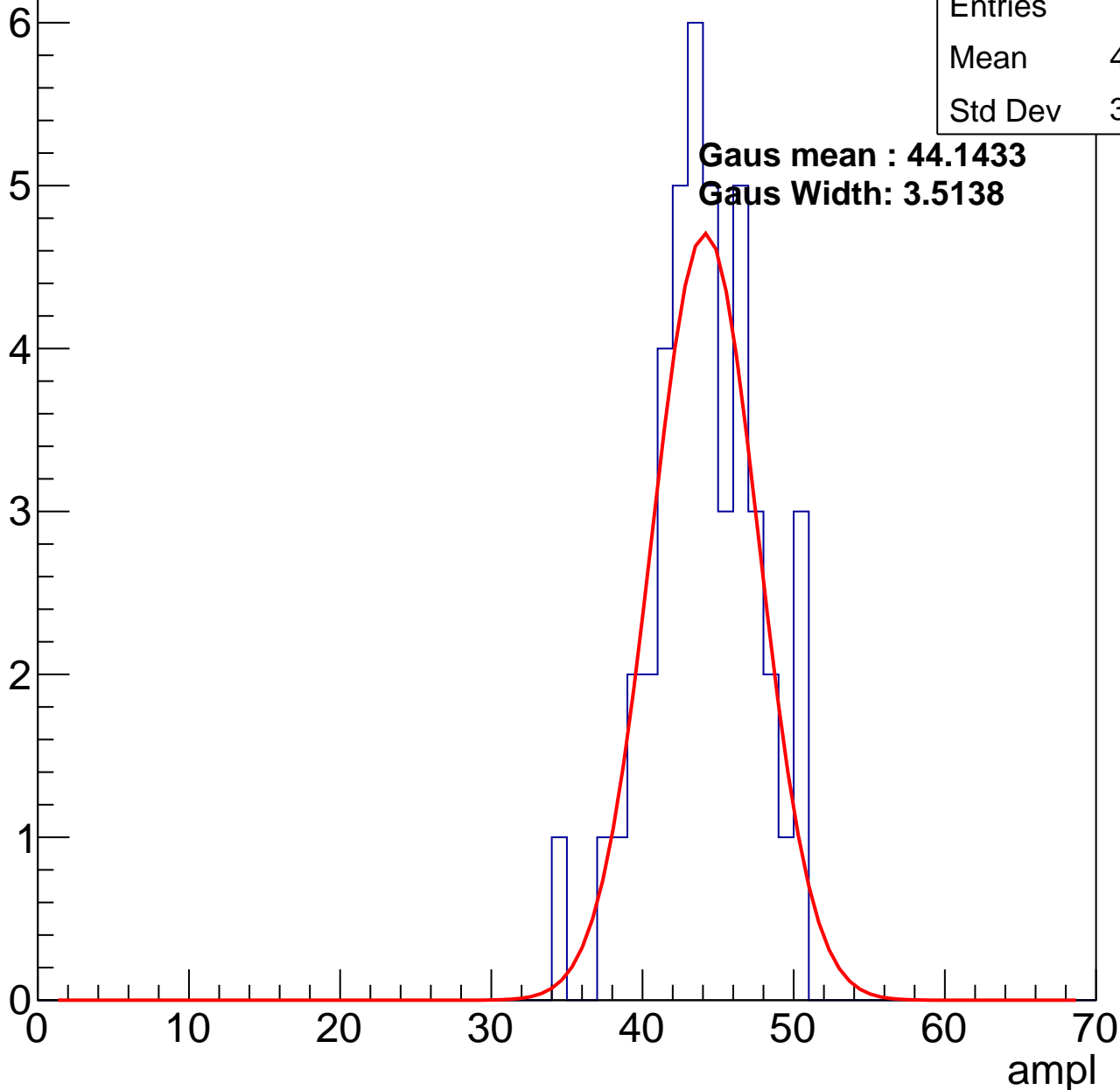
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	44
Mean	43.64
Std Dev	3.497

**Gaus mean : 44.1433**

**Gaus Width: 3.5138**



# B1L101S, U9-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

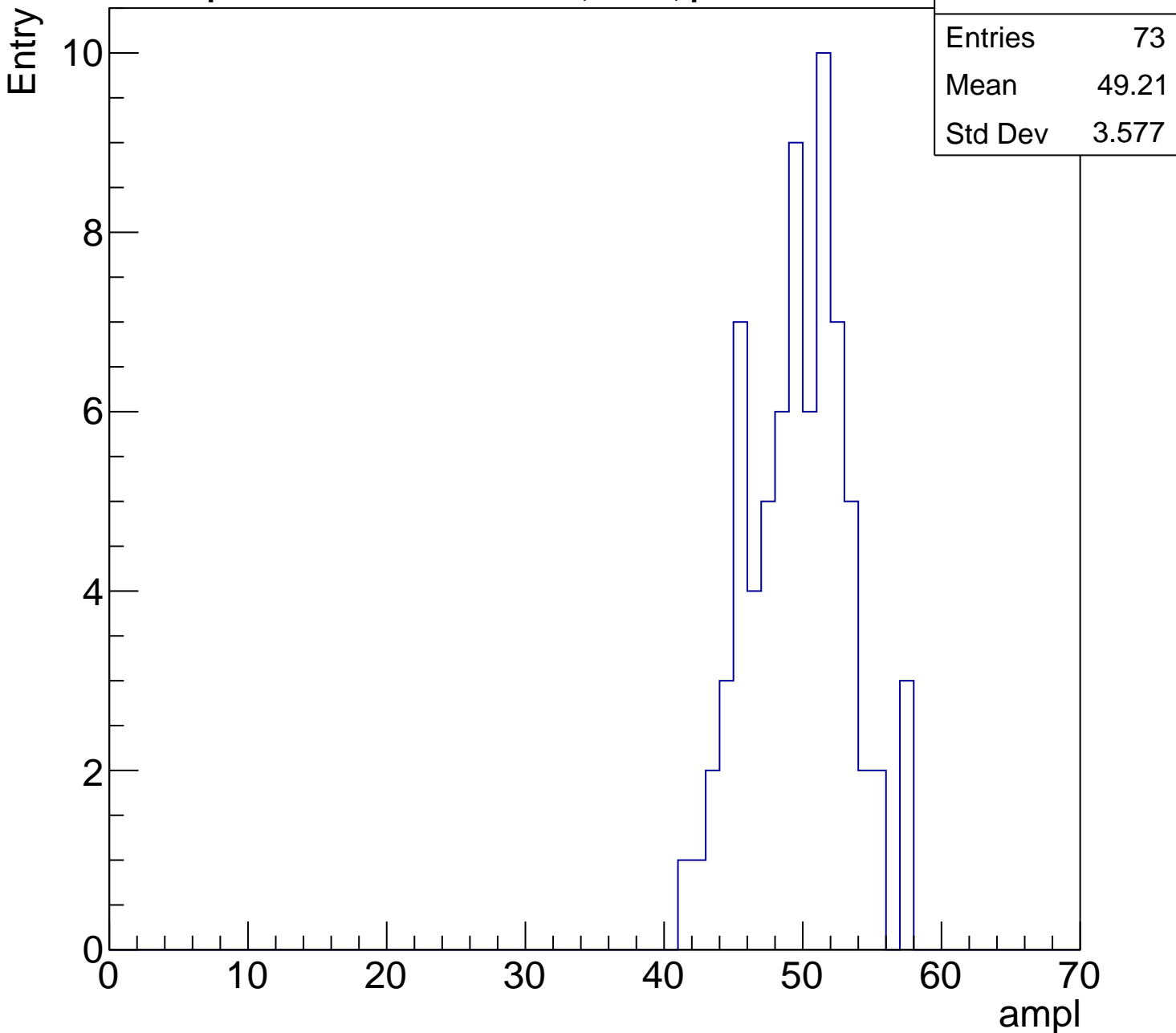
Entries	73
Mean	49.21
Std Dev	3.577

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

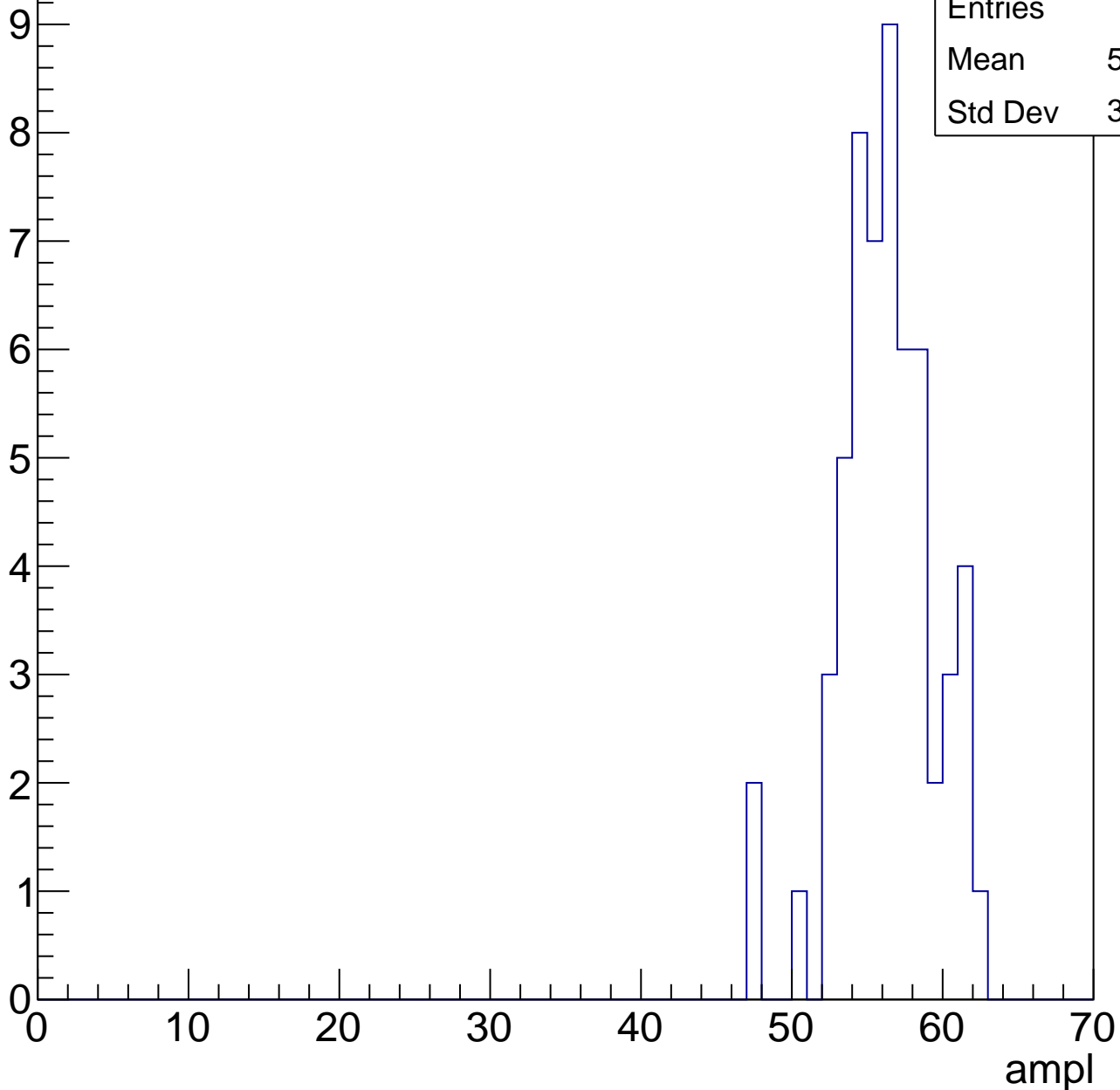


# B1L101S, U9-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	55.79
Std Dev	3.133



# B1L101S, U9-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

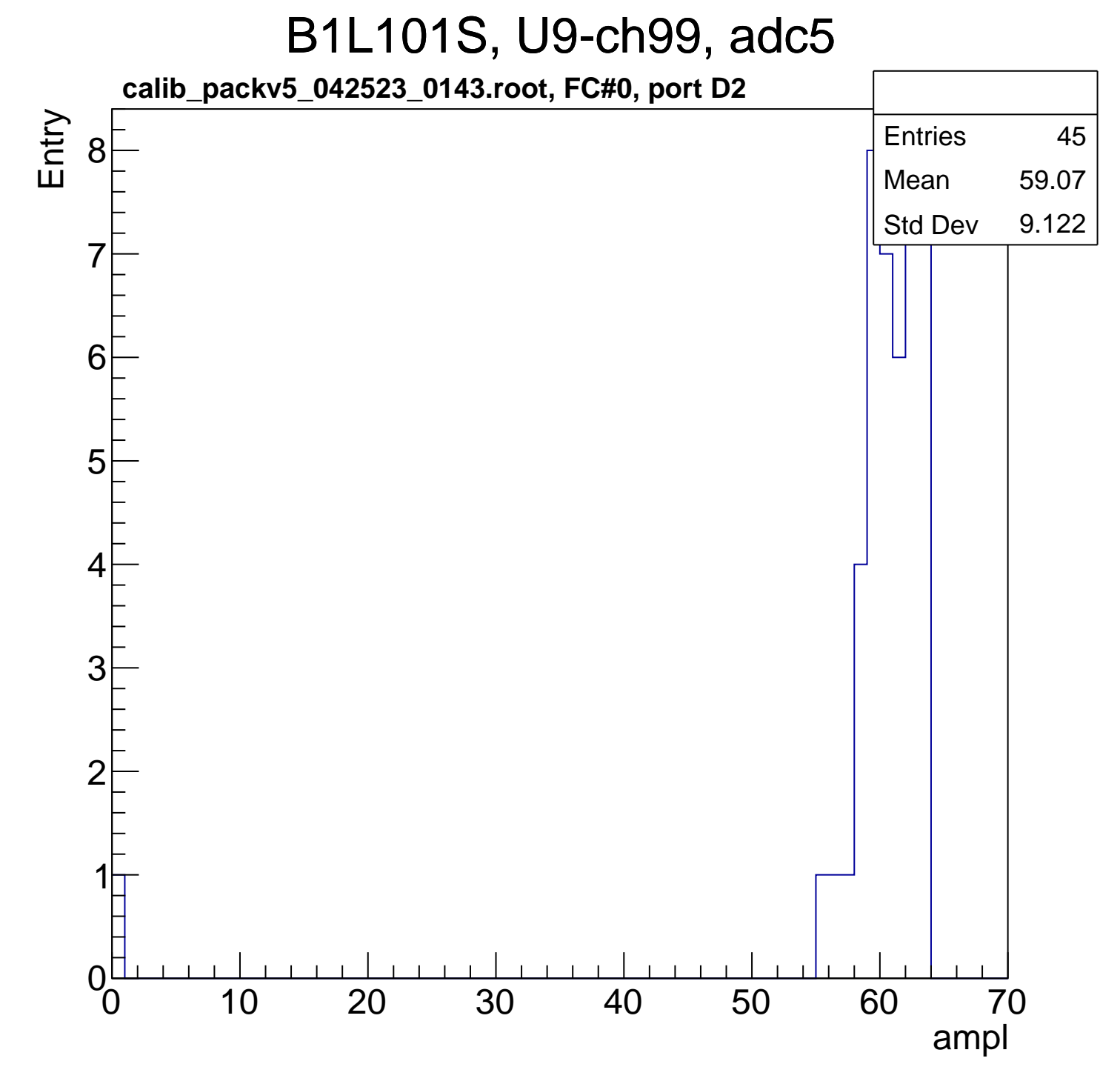
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	45
Mean	59.07
Std Dev	9.122

ampl

0 10 20 30 40 50 60 70



# B1L101S, U9-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	62.67
Std Dev	0.4714



# B1L101S, U9-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch100, adc0

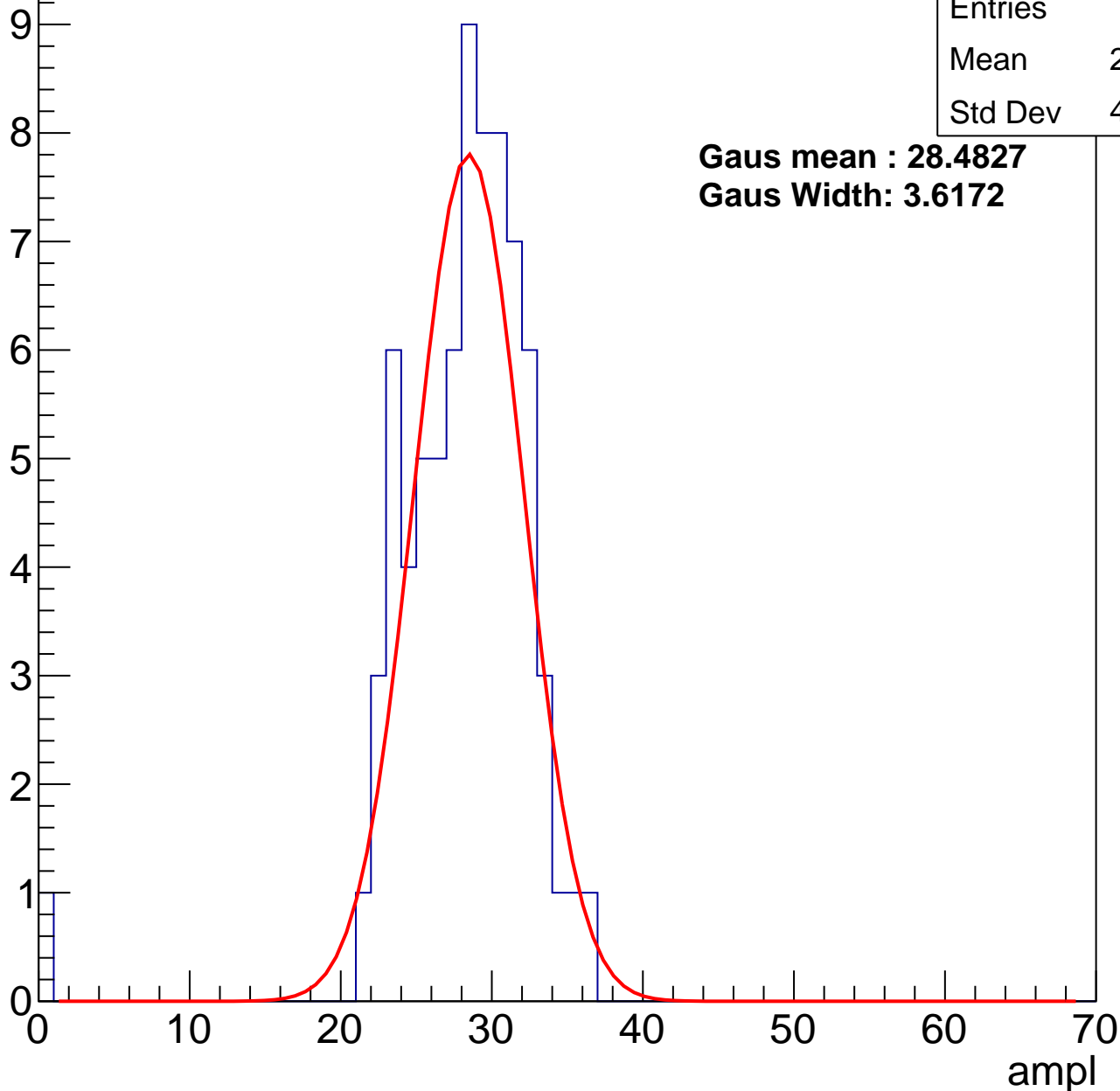
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	27.67
Std Dev	4.677

**Gaus mean : 28.4827**

**Gaus Width: 3.6172**



# B1L101S, U9-ch100, adc1

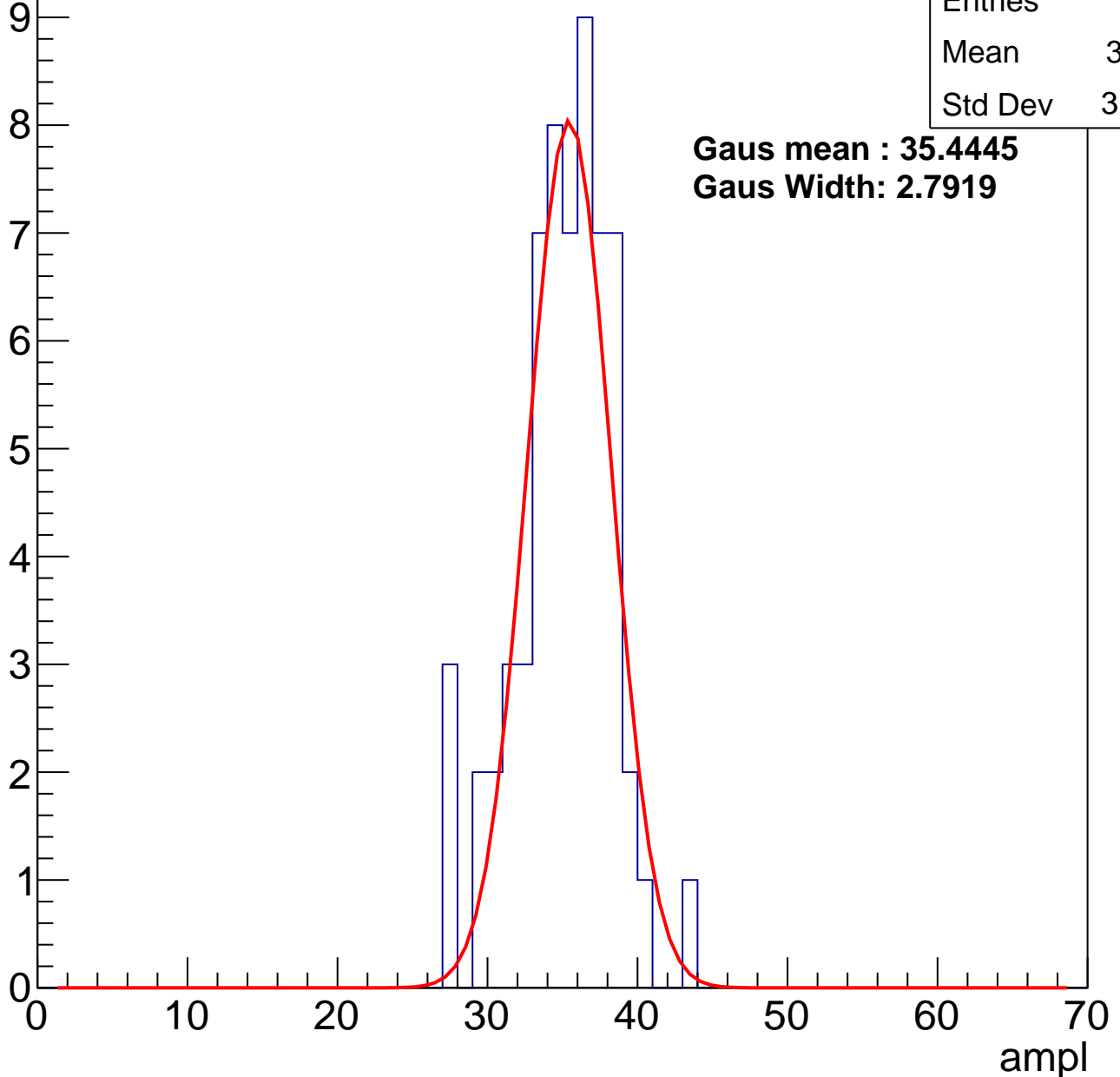
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	34.61
Std Dev	3.205

**Gaus mean : 35.4445**

**Gaus Width: 2.7919**



# B1L101S, U9-ch100, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	65
Mean	41.17
Std Dev	3.204

**Gaus mean : 41.6739**

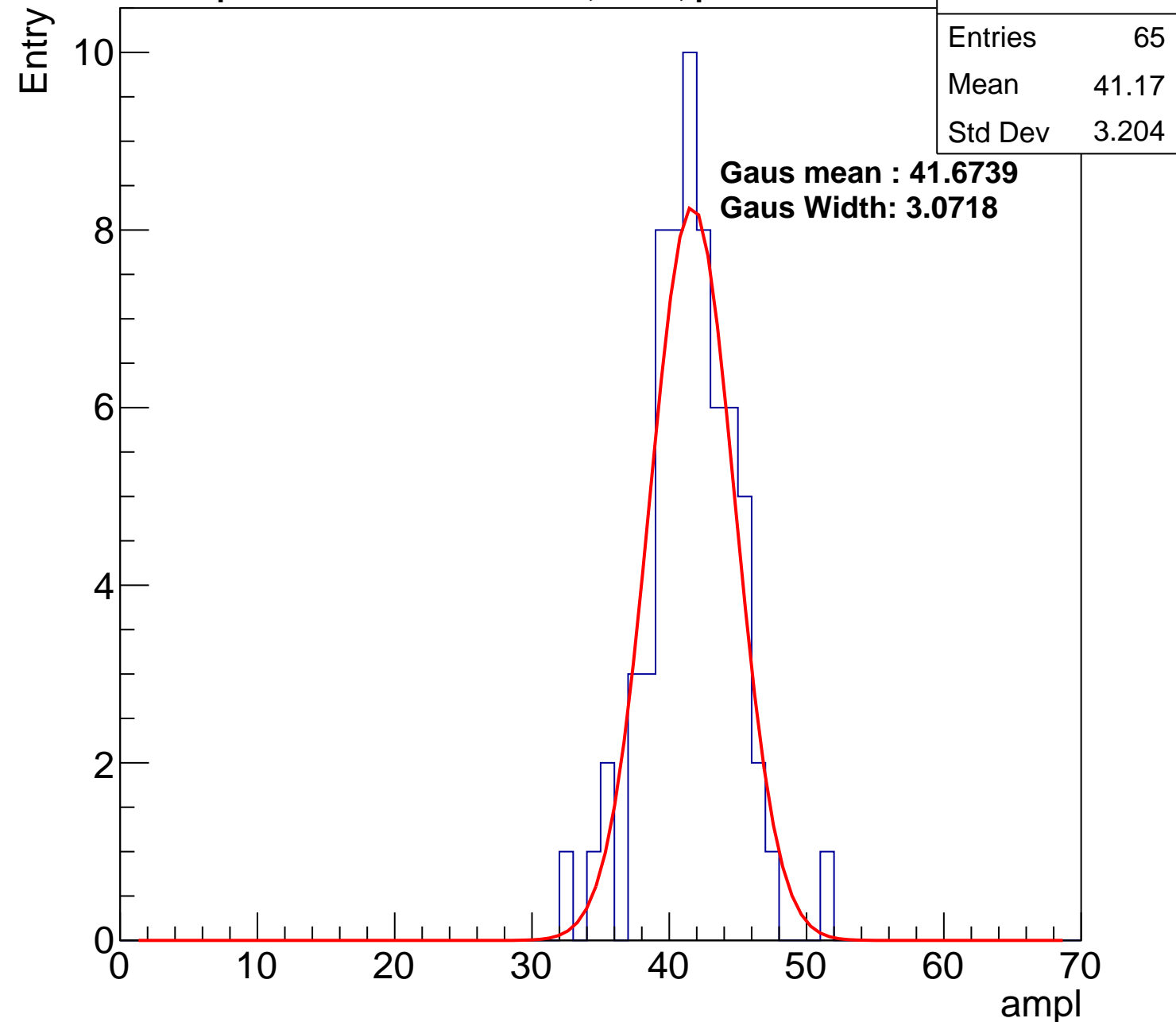
**Gaus Width: 3.0718**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

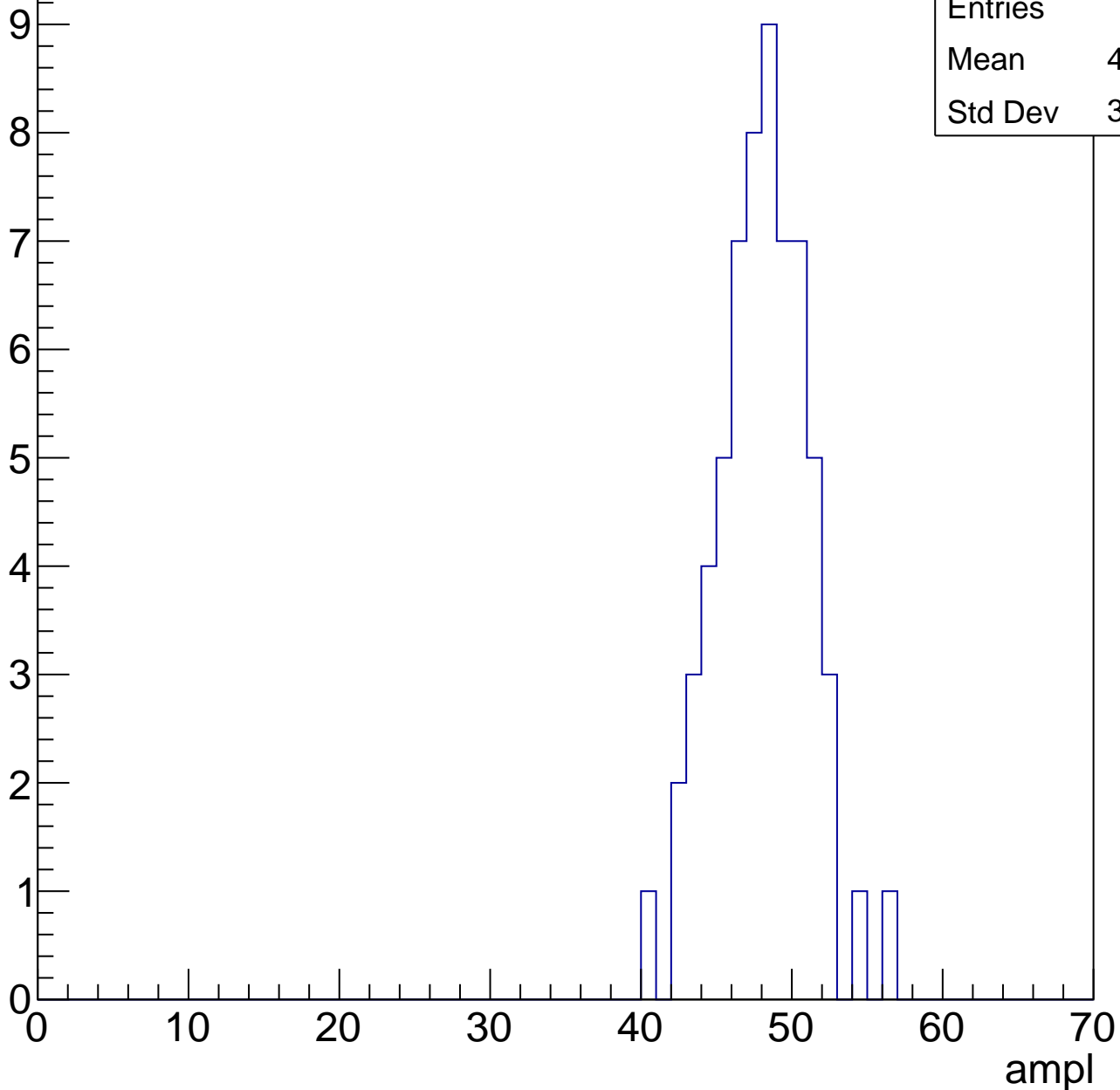


# B1L101S, U9-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

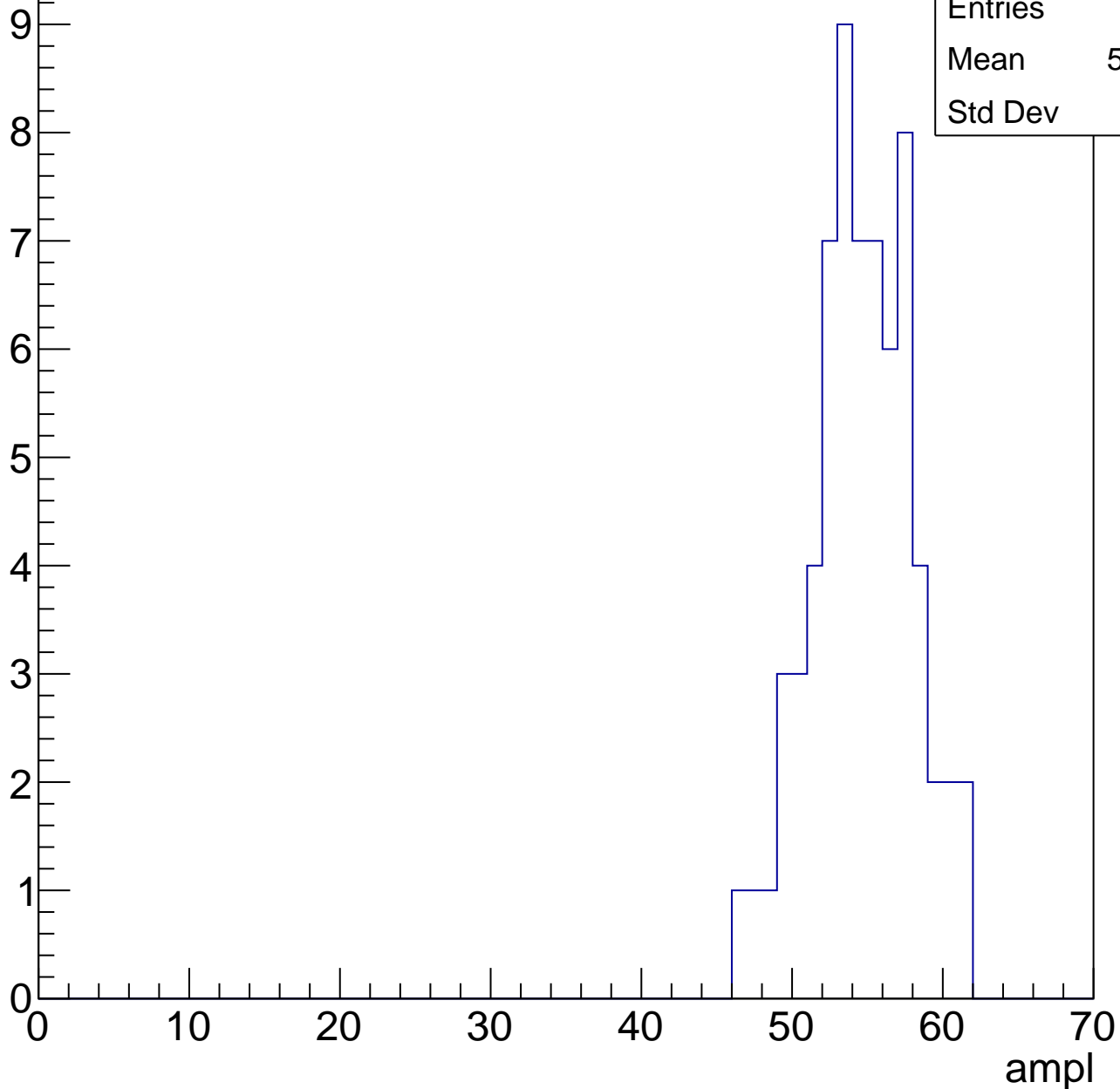
Entries	63
Mean	47.59
Std Dev	3.017



# B1L101S, U9-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



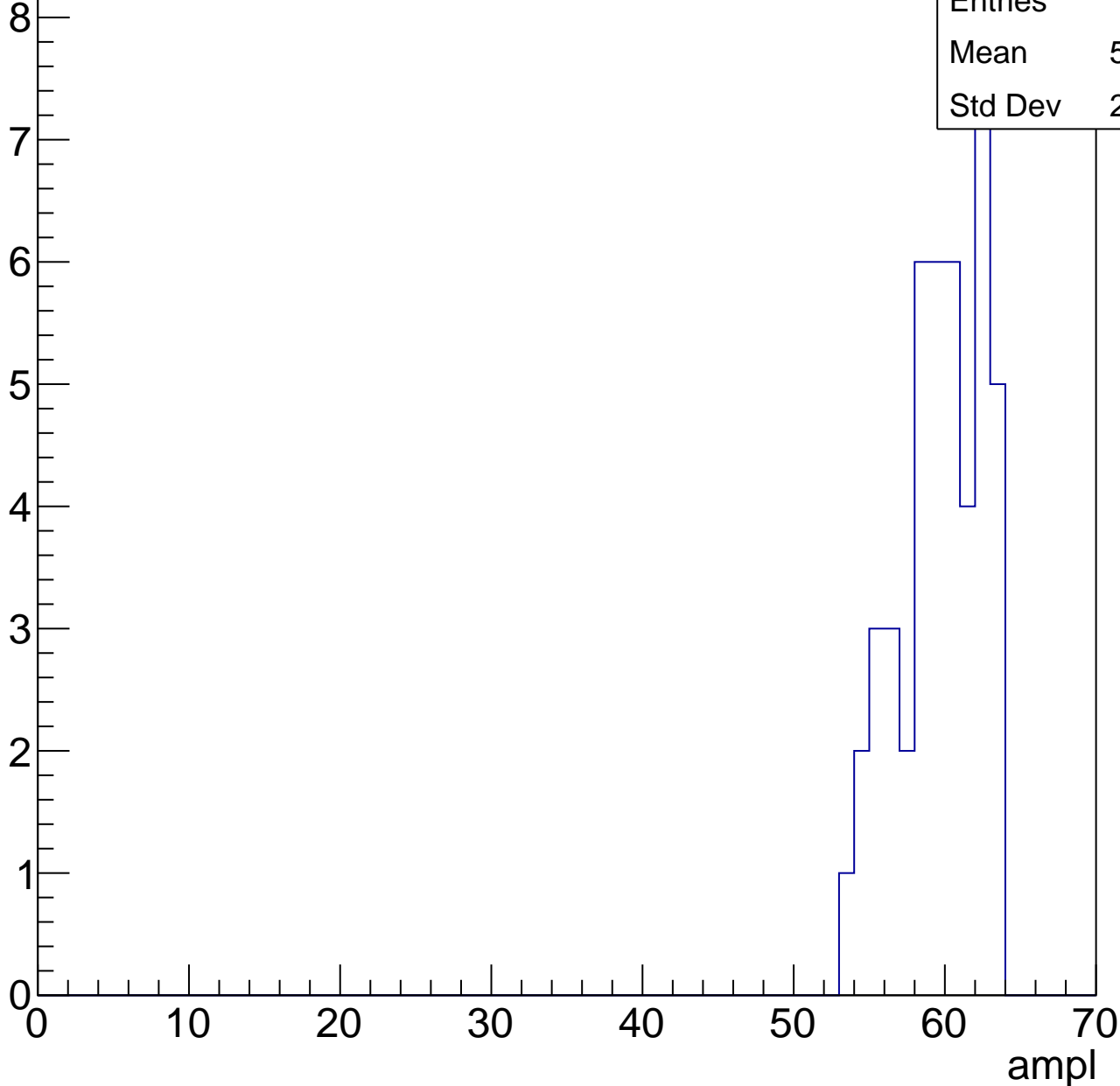
Entries	67
Mean	54.18
Std Dev	3.3

# B1L101S, U9-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

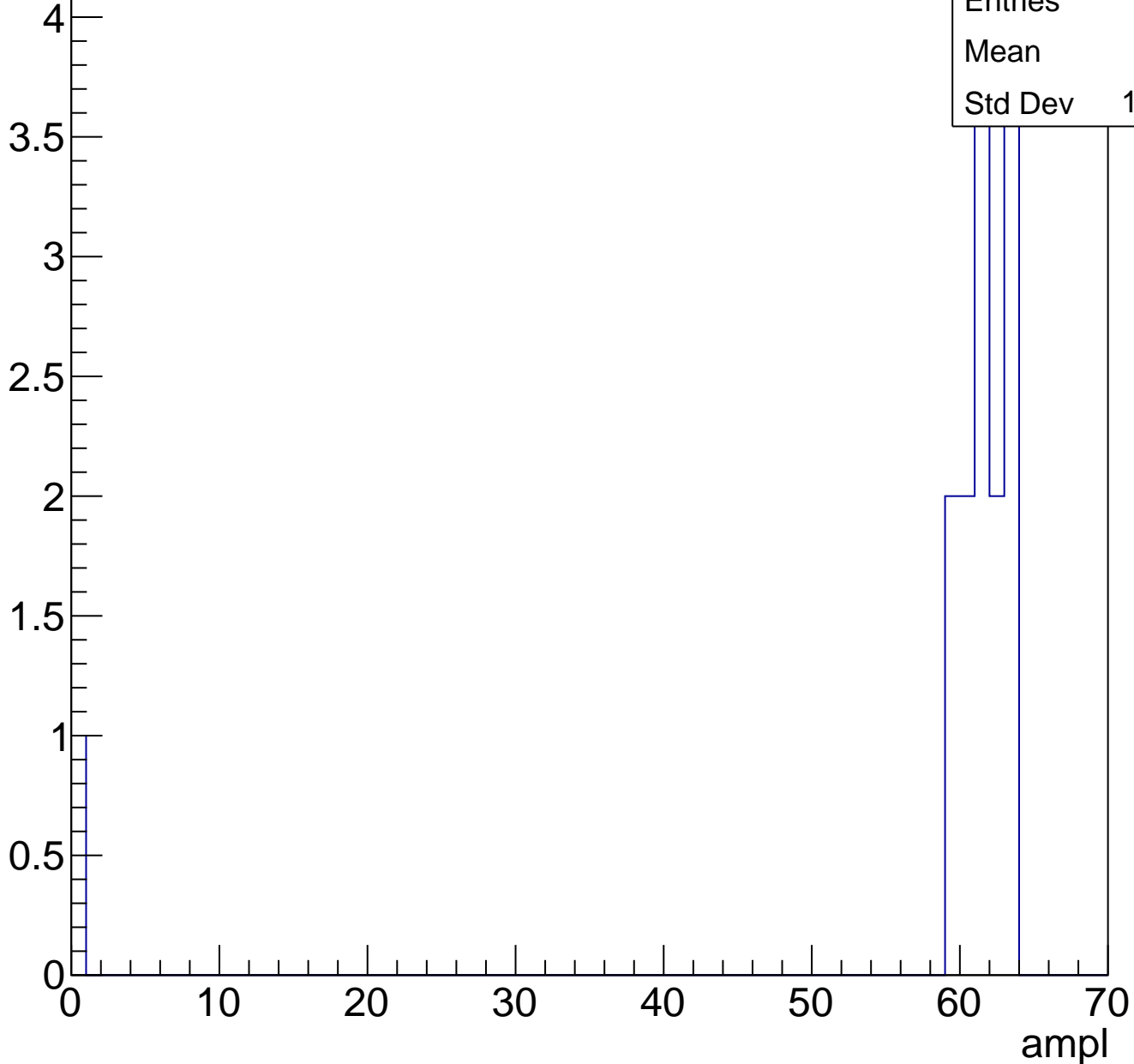
Entries	46
Mean	59.24
Std Dev	2.744



# B1L101S, U9-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

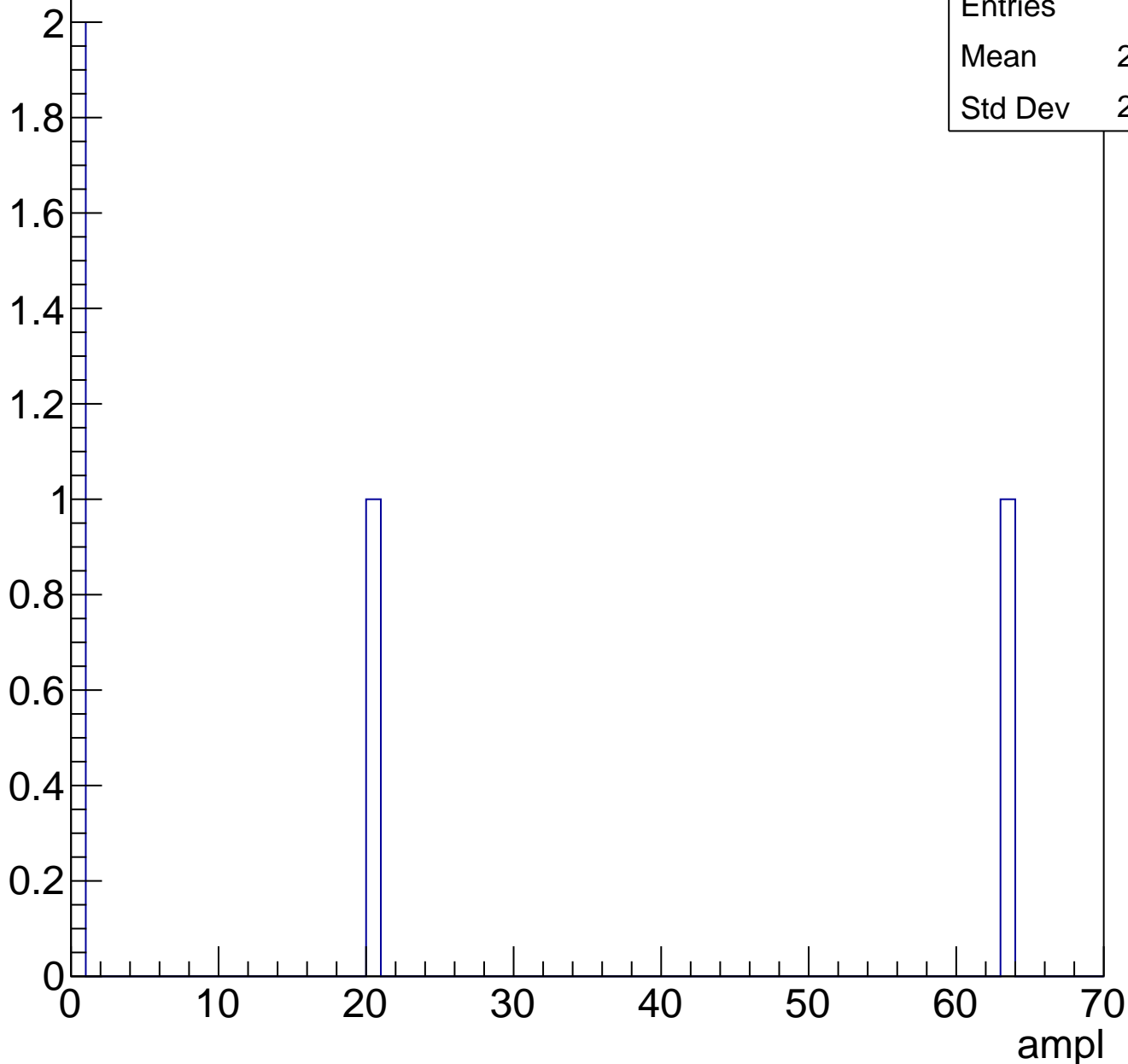




# B1L101S, U9-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	4
Mean	20.75
Std Dev	25.72

# B1L101S, U9-ch101, adc0

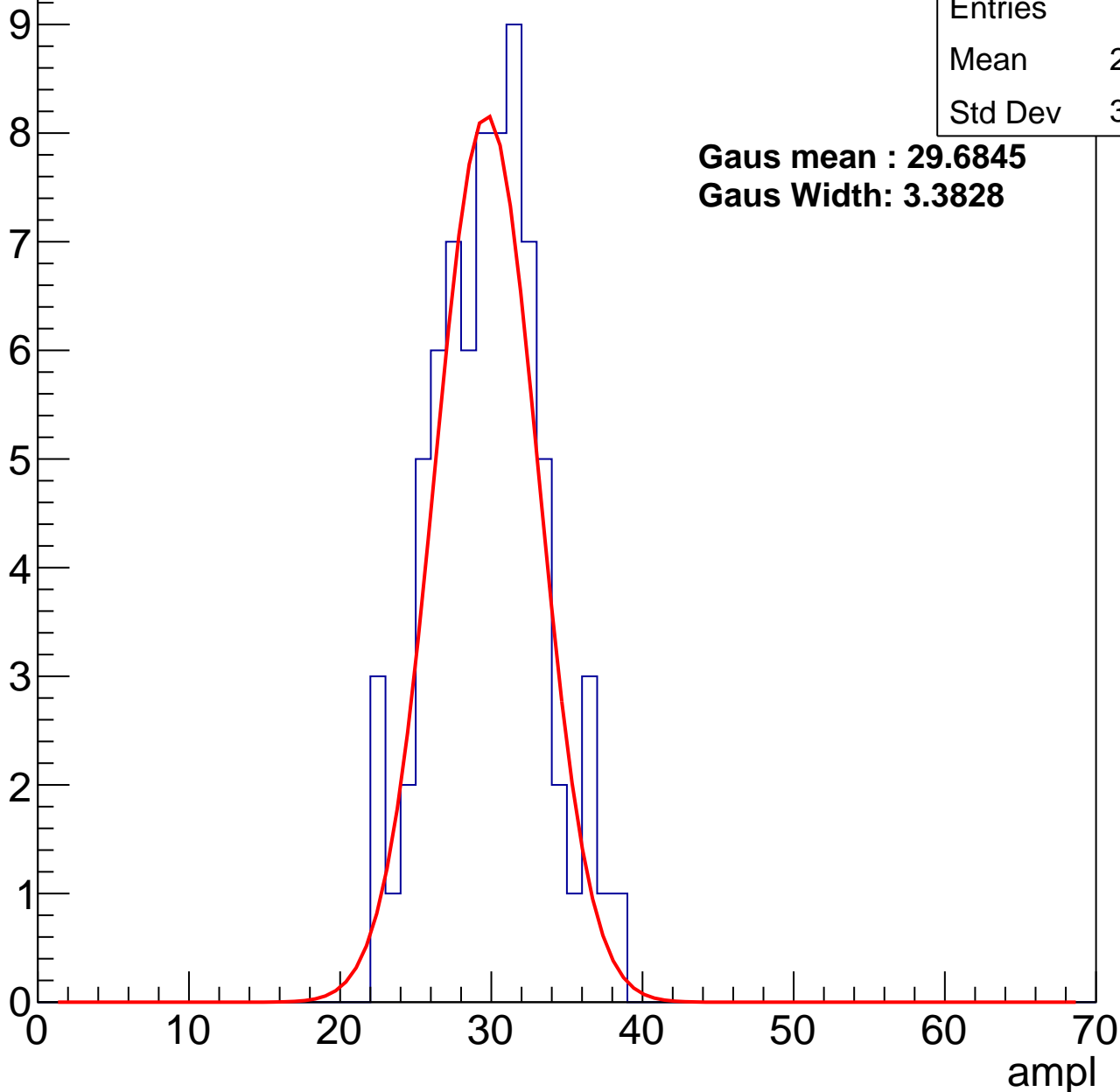
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	29.35
Std Dev	3.572

**Gaus mean : 29.6845**

**Gaus Width: 3.3828**



# B1L101S, U9-ch101, adc1

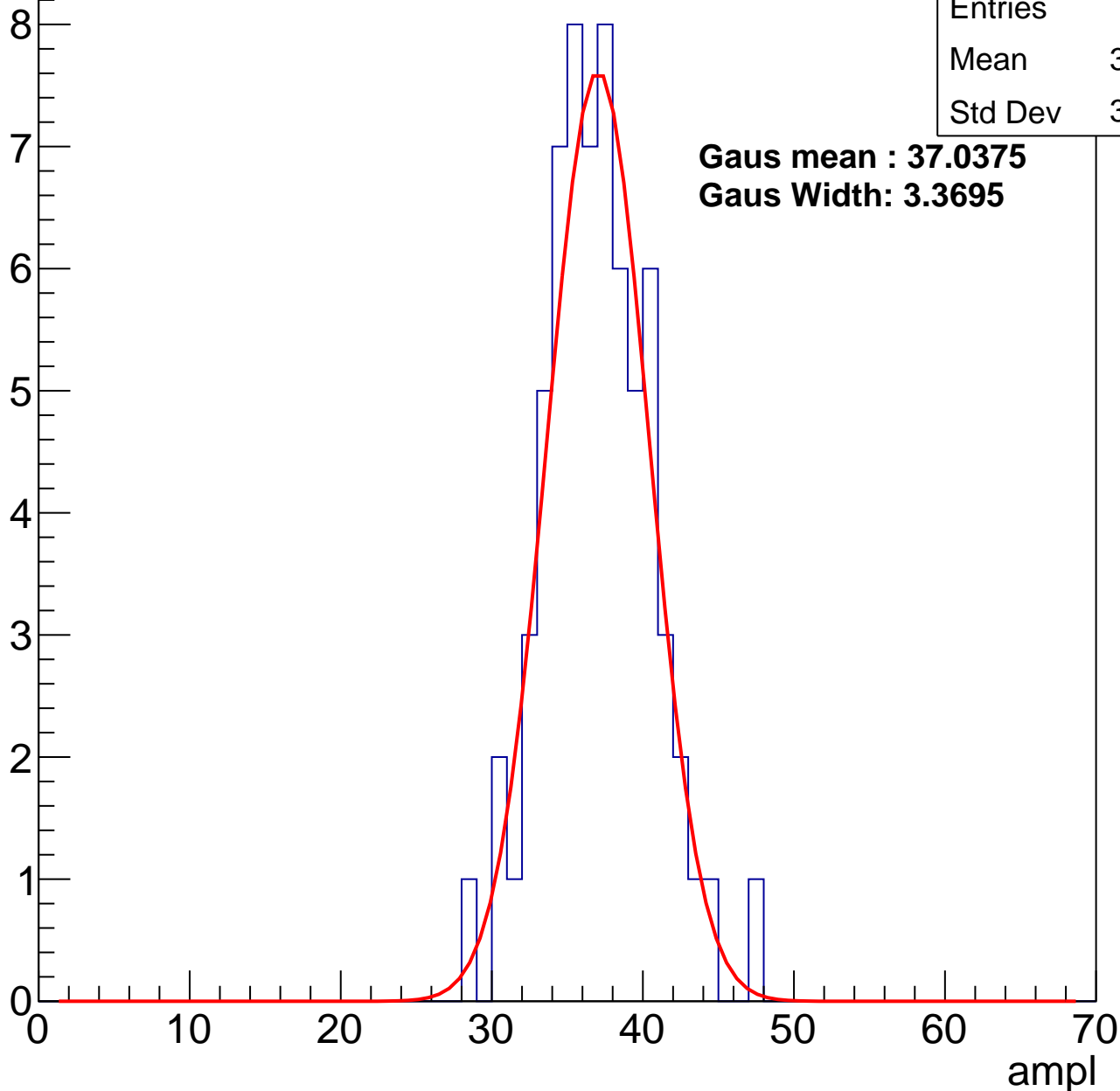
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	36.57
Std Dev	3.504

**Gaus mean : 37.0375**

**Gaus Width: 3.3695**



# B1L101S, U9-ch101, adc2

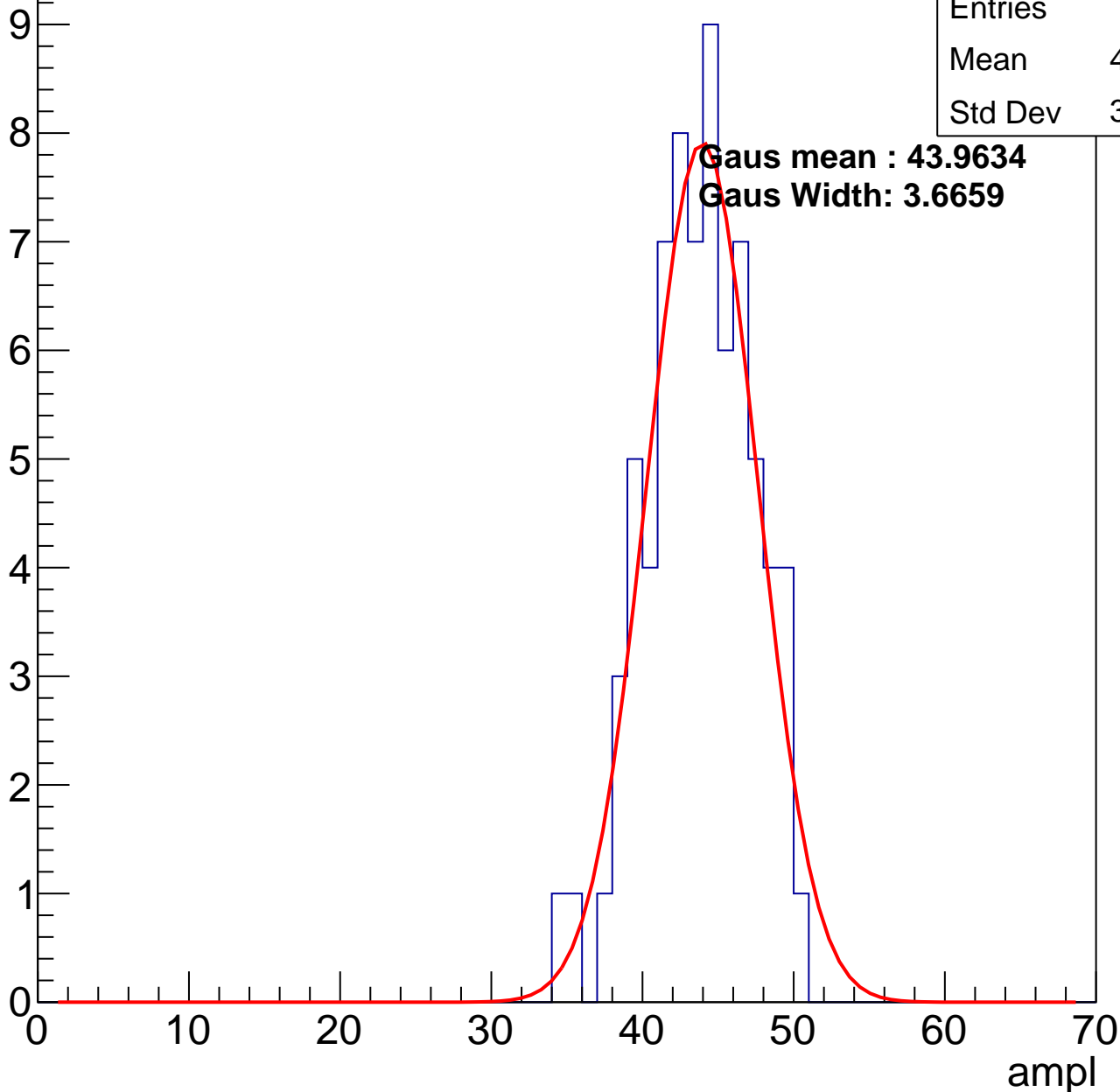
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	43.29
Std Dev	3.454

**Gaus mean : 43.9634**

**Gaus Width: 3.6659**

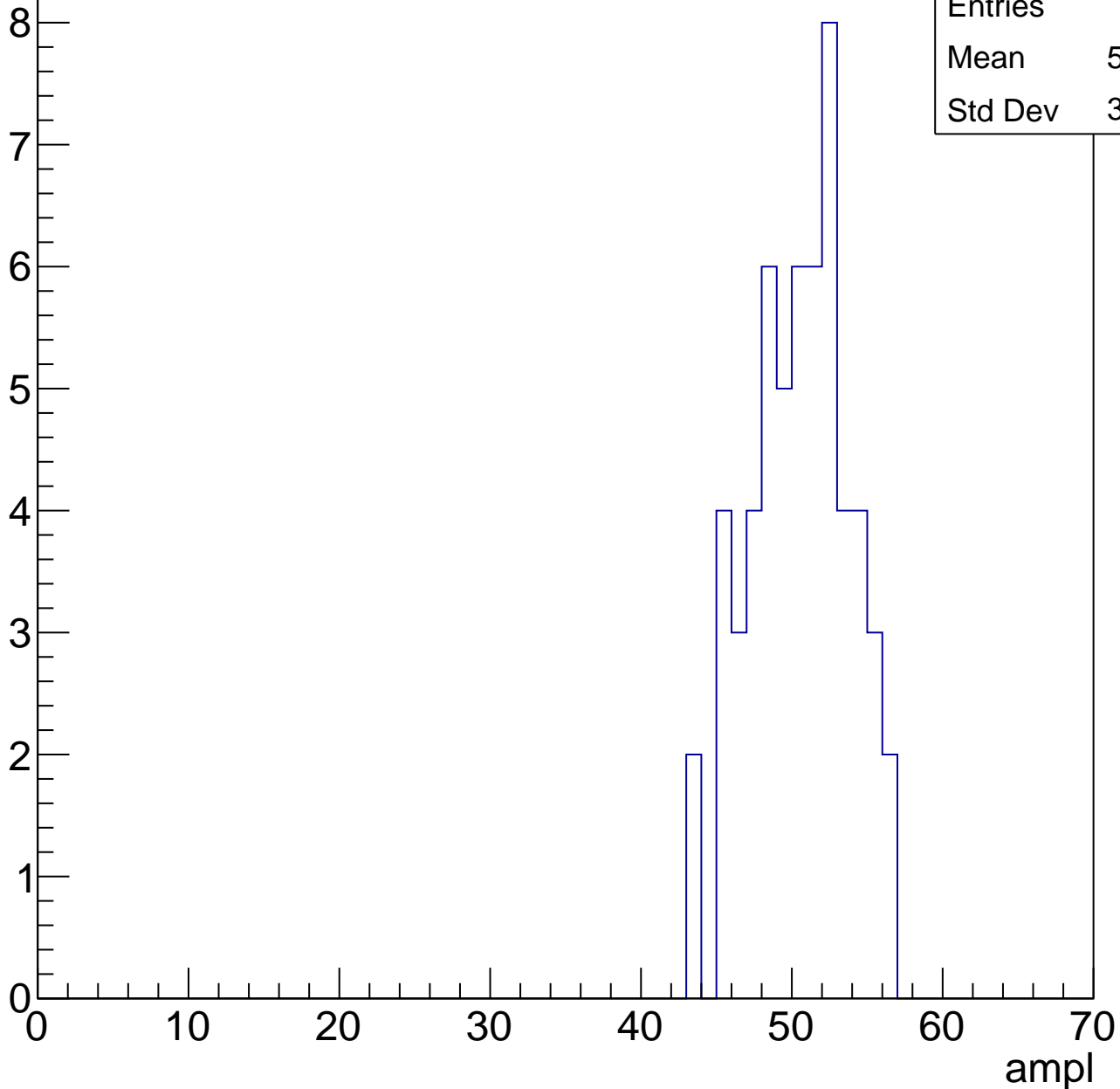


# B1L101S, U9-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	50.04
Std Dev	3.233

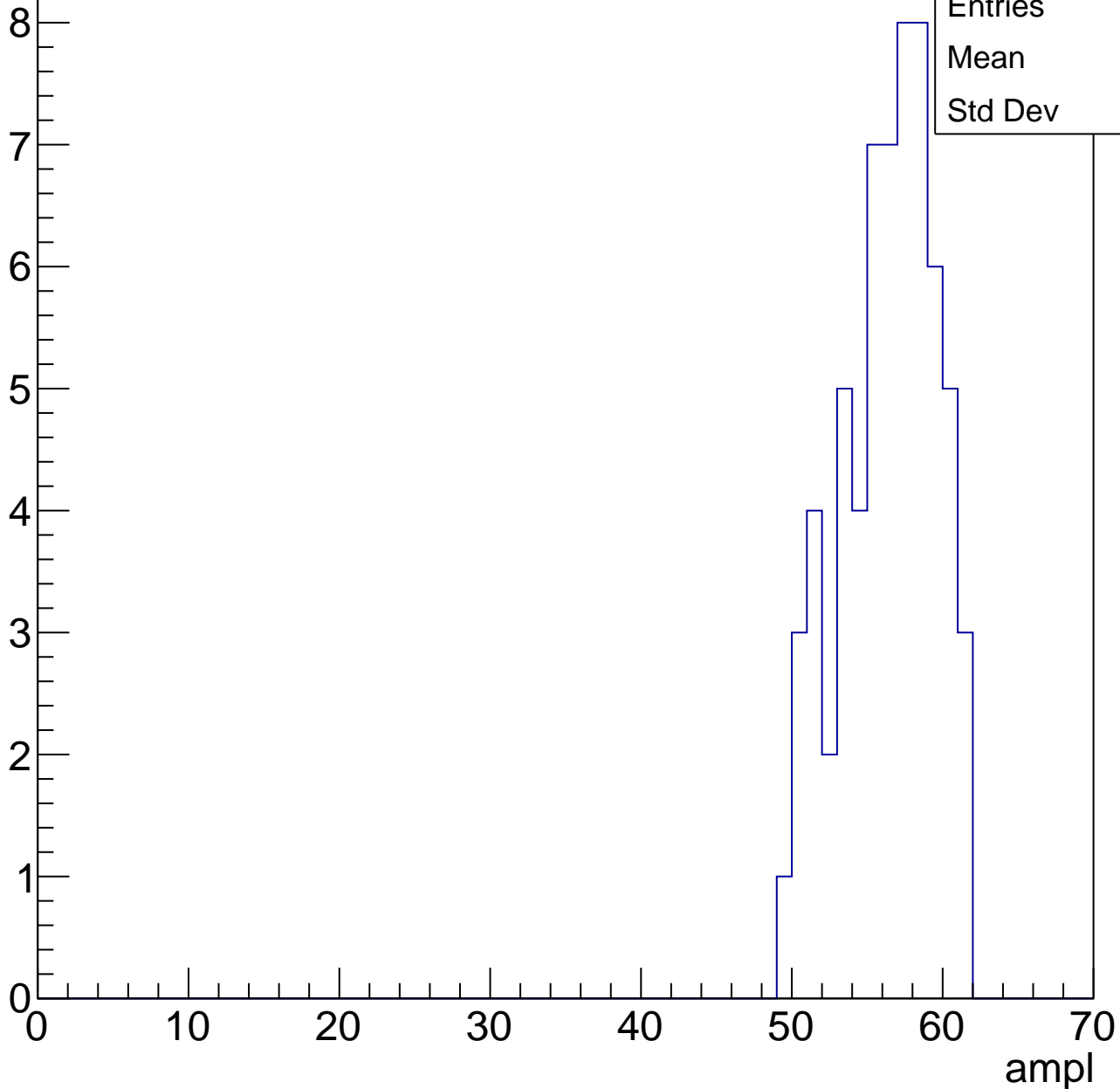


# B1L101S, U9-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	55.9
Std Dev	3.1

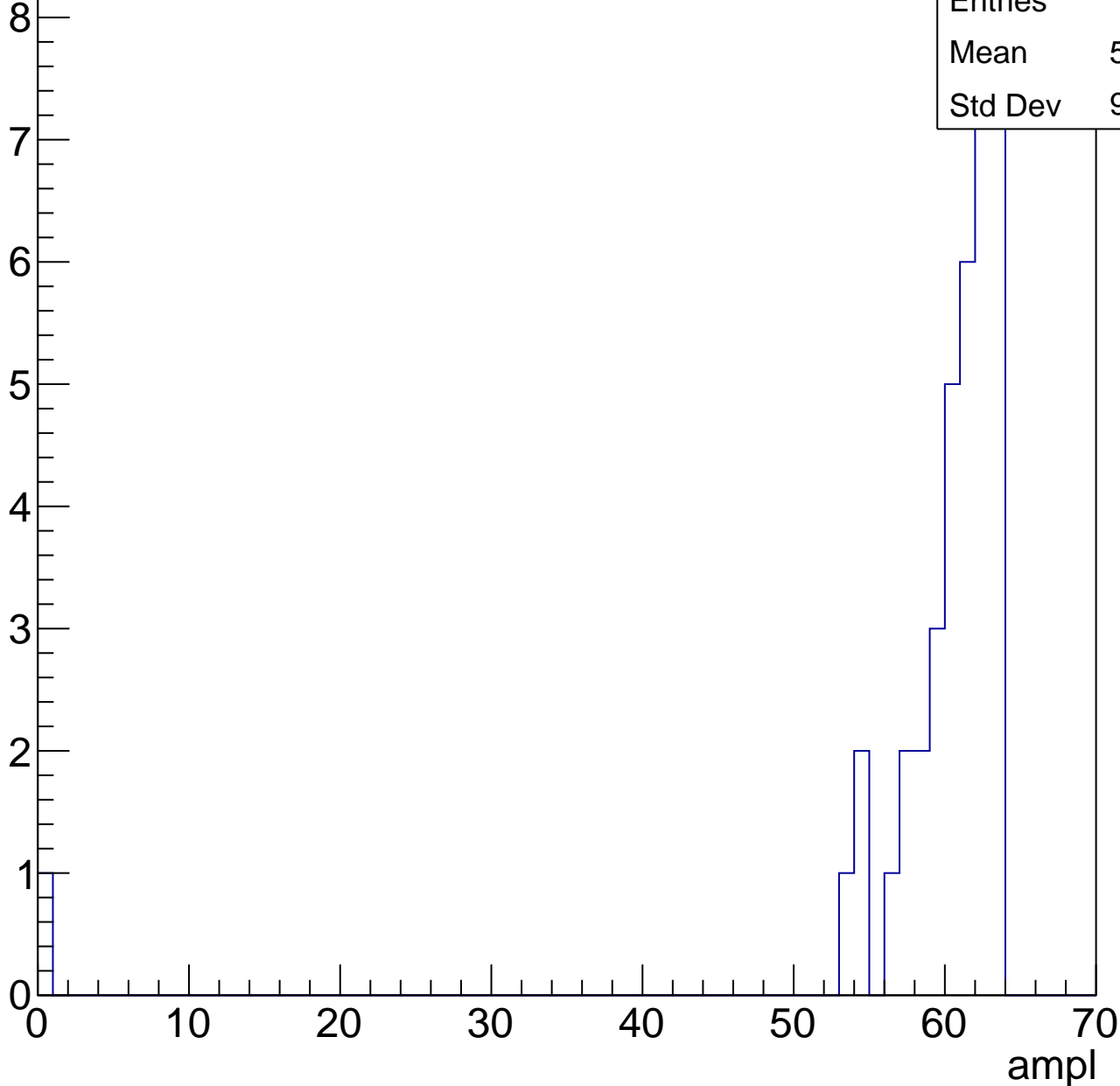


# B1L101S, U9-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	39
Mean	58.72
Std Dev	9.886



# B1L101S, U9-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

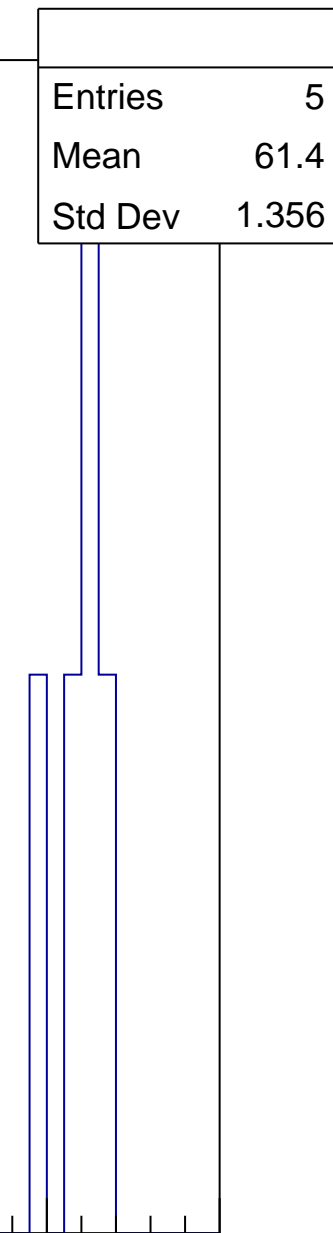
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.4
Std Dev	1.356

ampl

0 10 20 30 40 50 60 70





# B1L101S, U9-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch102, adc0

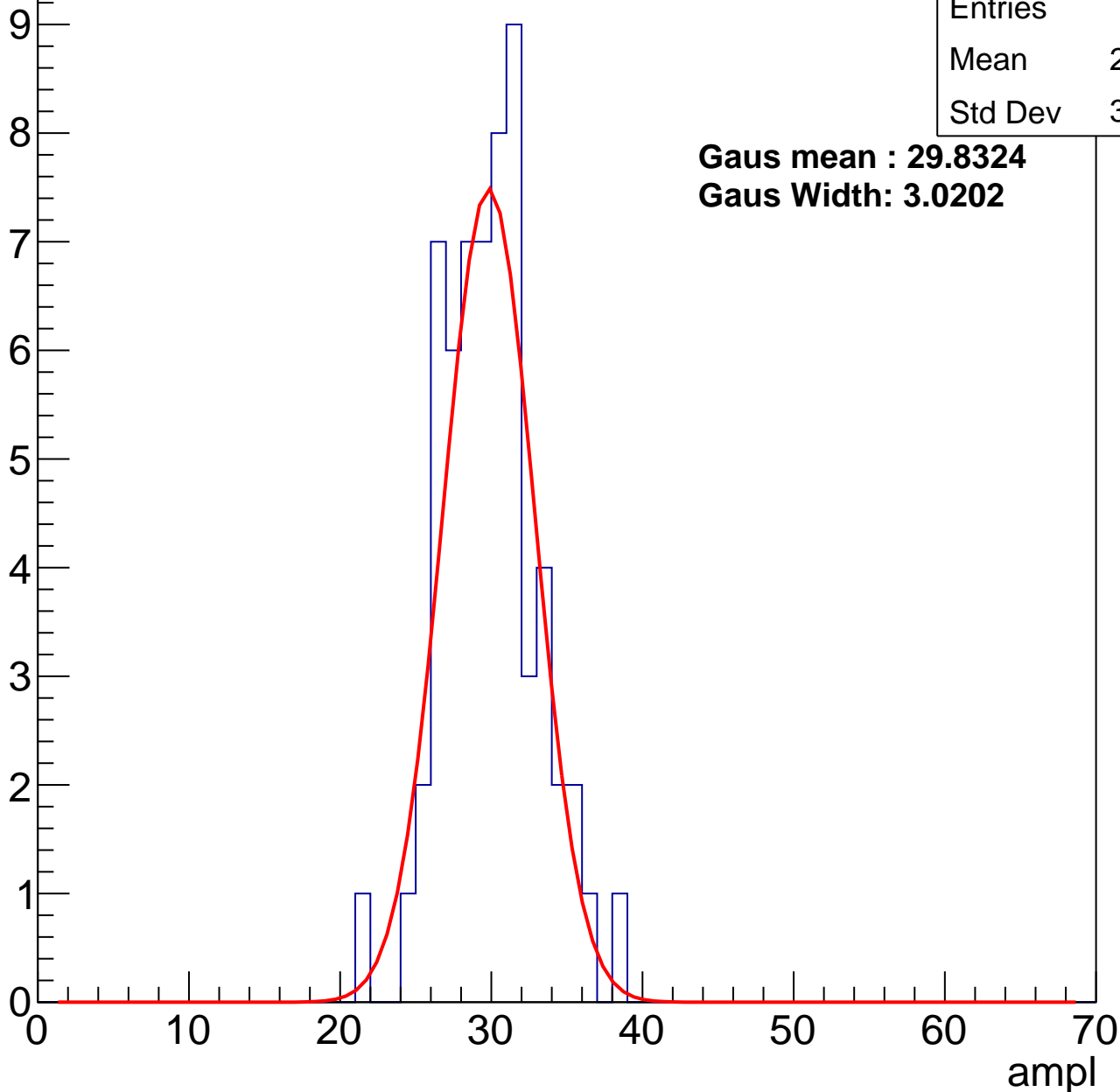
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	29.46
Std Dev	3.108

**Gaus mean : 29.8324**

**Gaus Width: 3.0202**



# B1L101S, U9-ch102, adc1

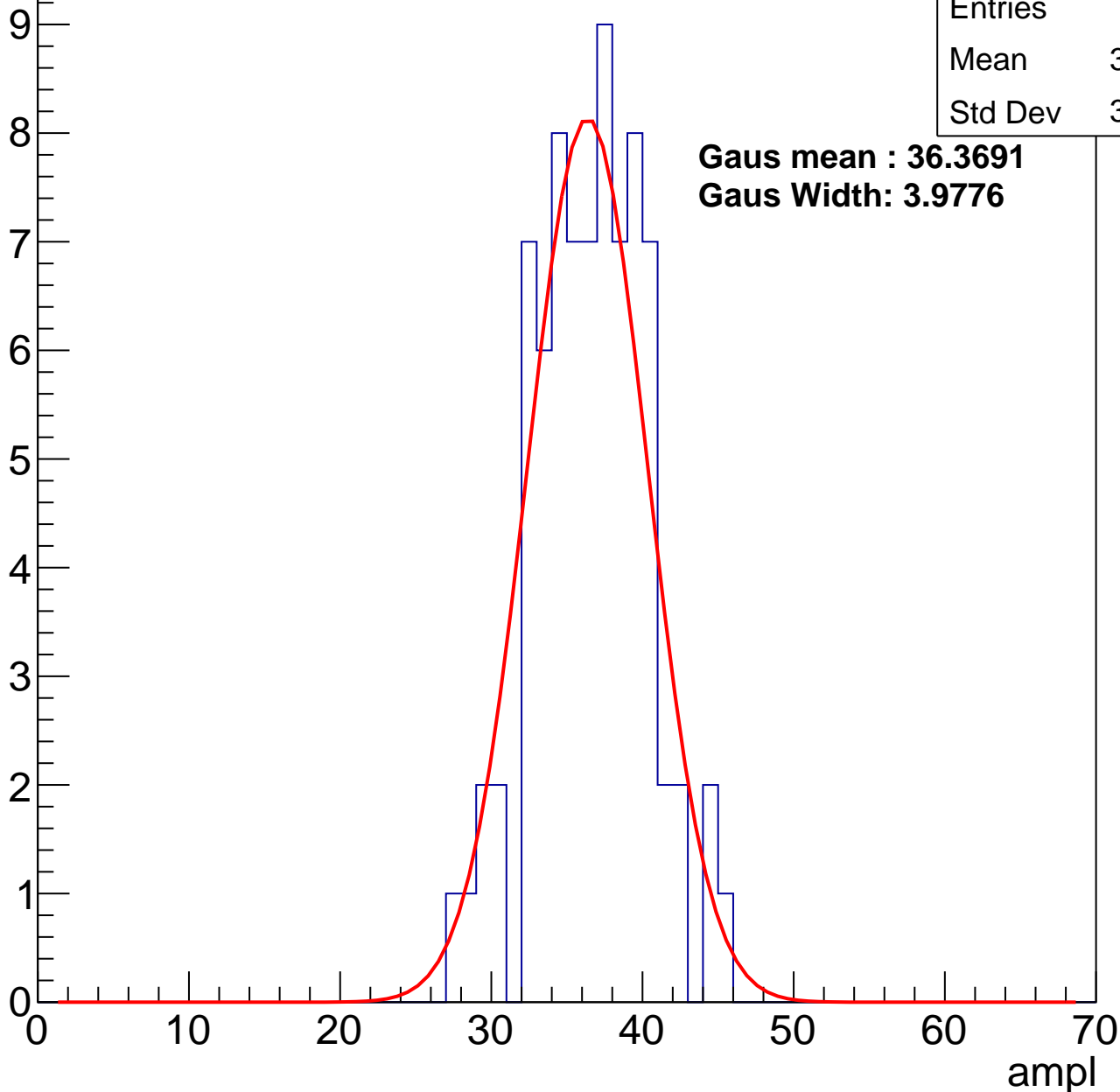
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	36.13
Std Dev	3.682

**Gaus mean : 36.3691**

**Gaus Width: 3.9776**



# B1L101S, U9-ch102, adc2

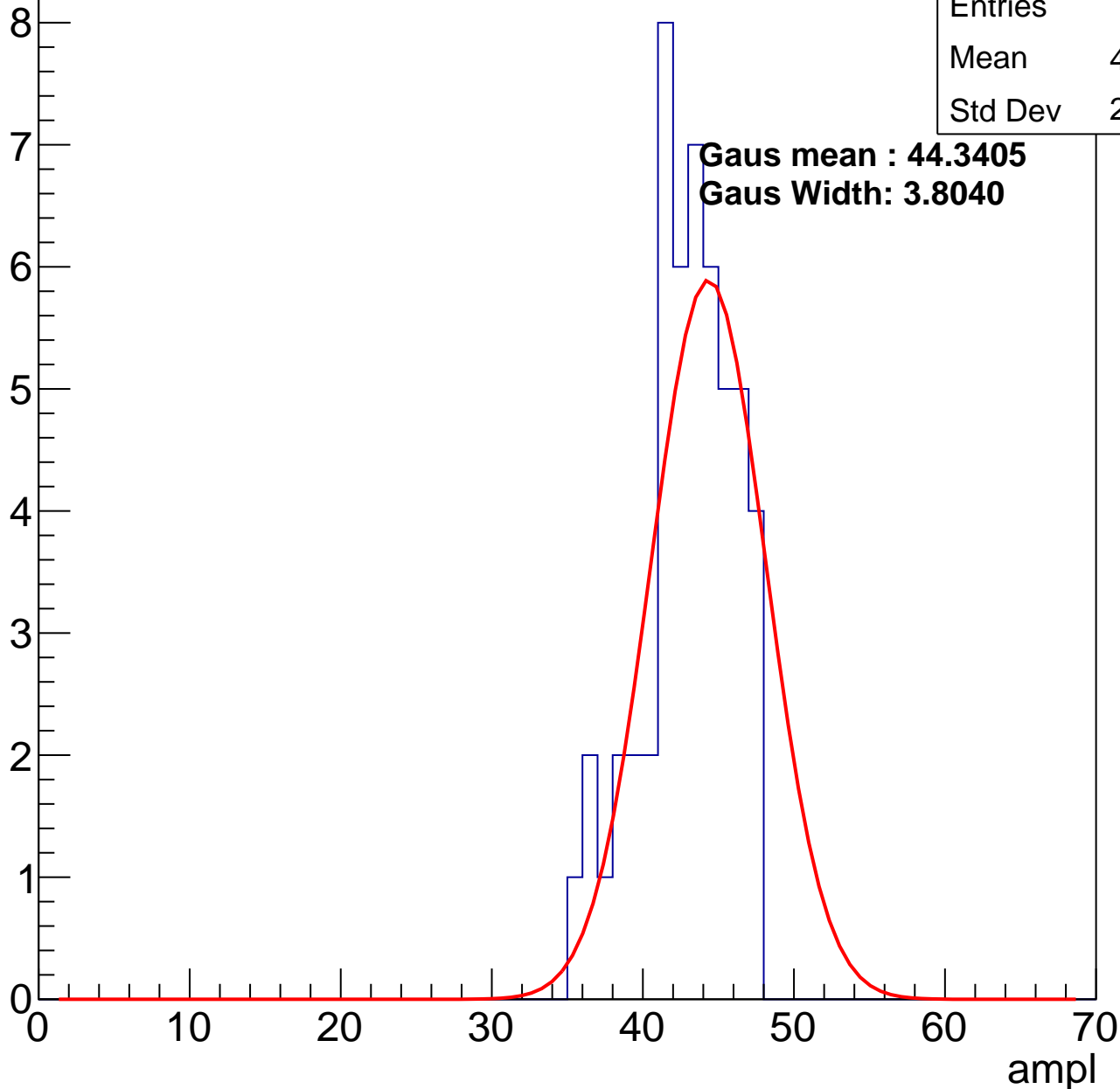
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	42.47
Std Dev	2.992

**Gaus mean : 44.3405**

**Gaus Width: 3.8040**

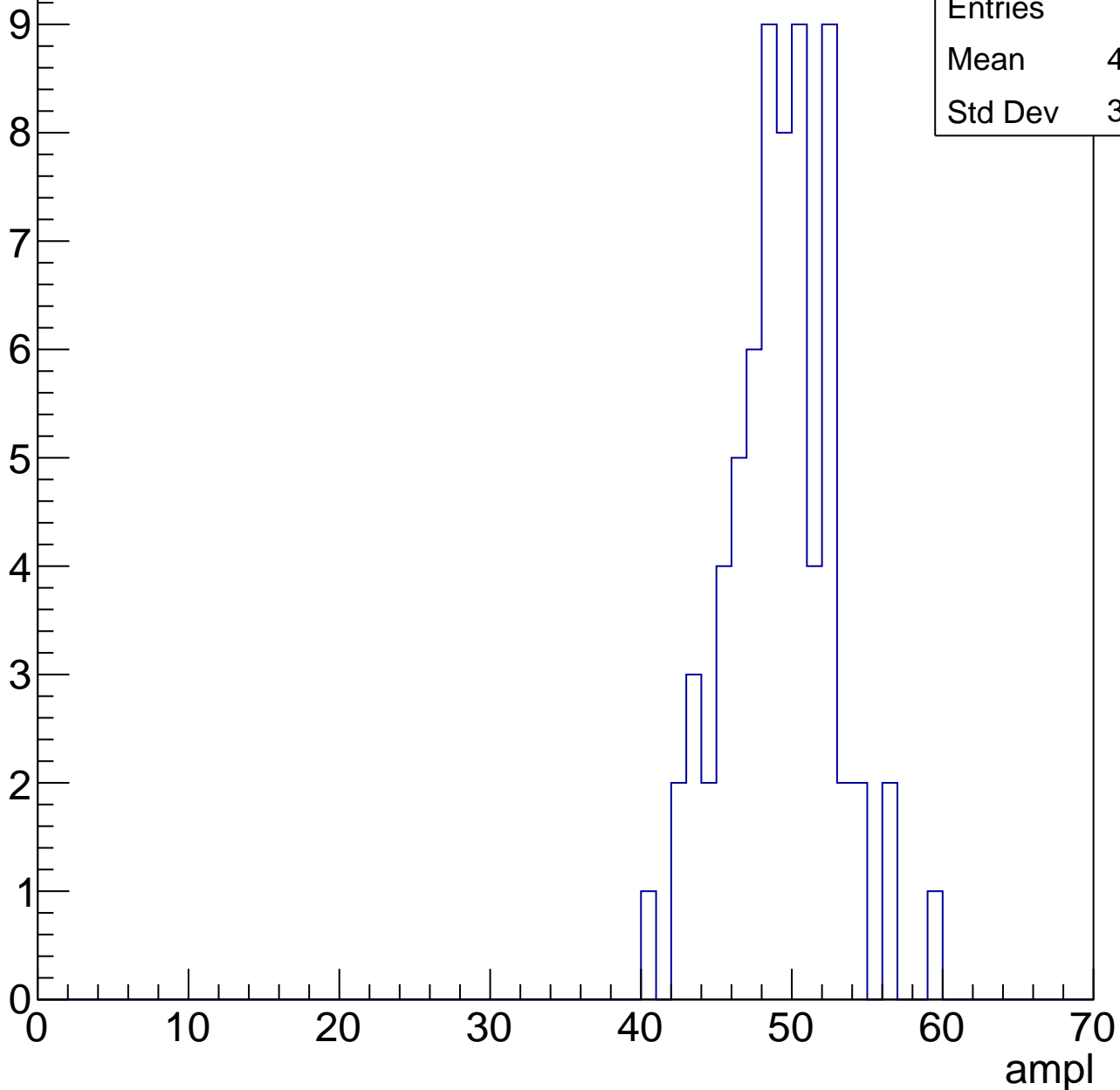


# B1L101S, U9-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

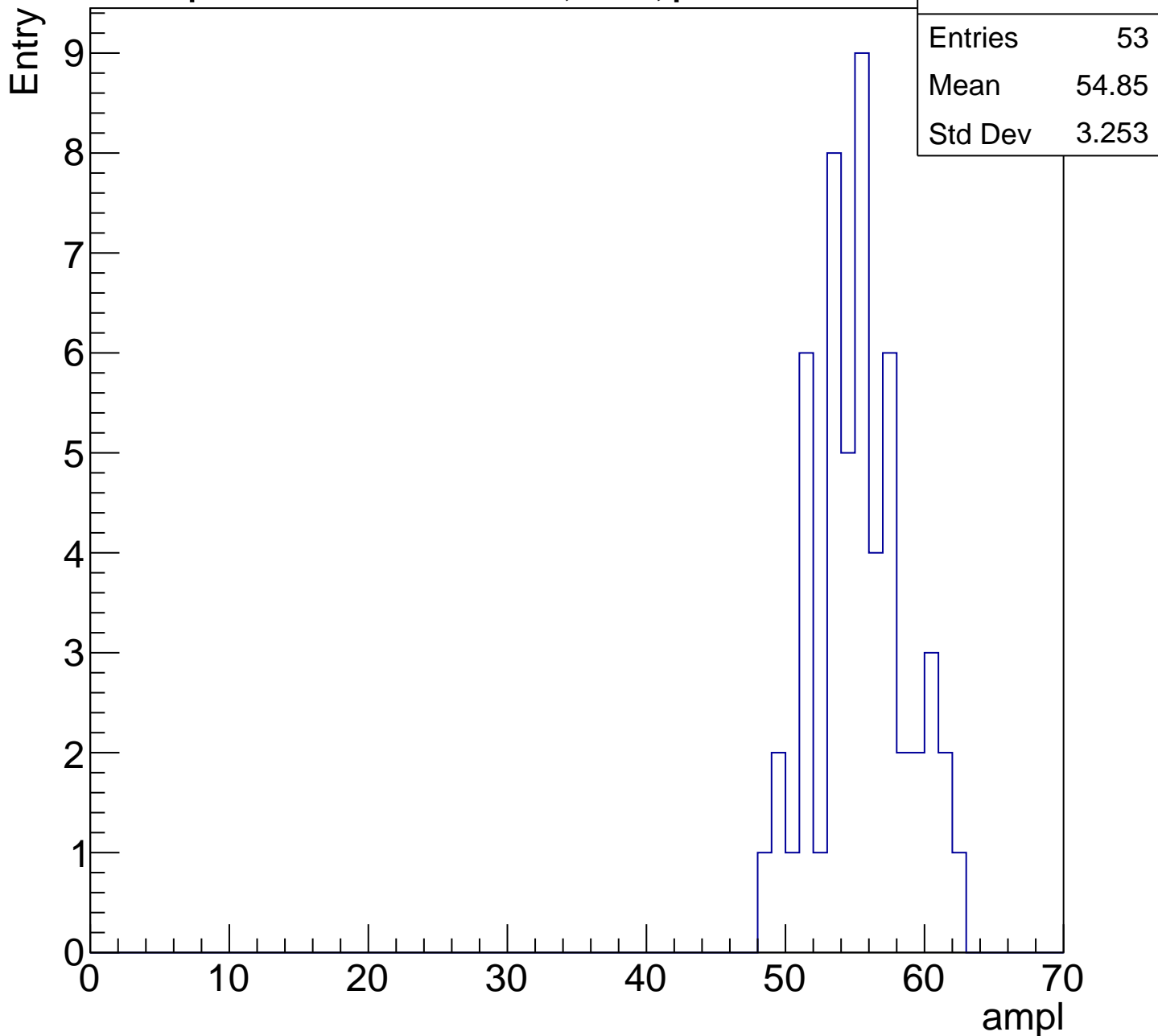
Entry

Entries	69
Mean	48.75
Std Dev	3.532



# B1L101S, U9-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U9-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	55
Mean	59.4
Std Dev	2.513

ampl

0

10

20

30

40

50

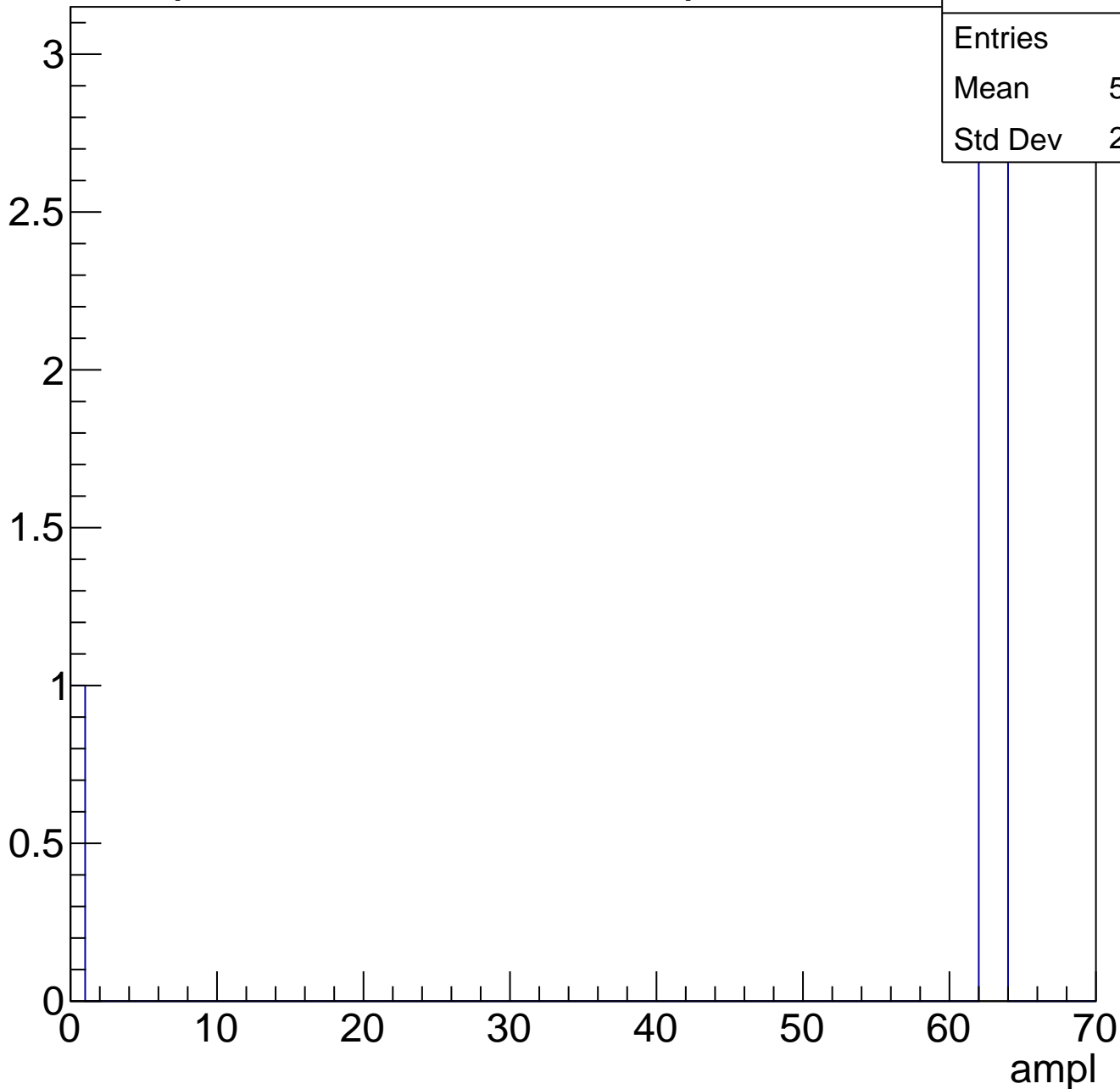
60

70

# B1L101S, U9-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	7
Mean	53.57
Std Dev	21.88



# B1L101S, U9-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U9-ch103, adc0

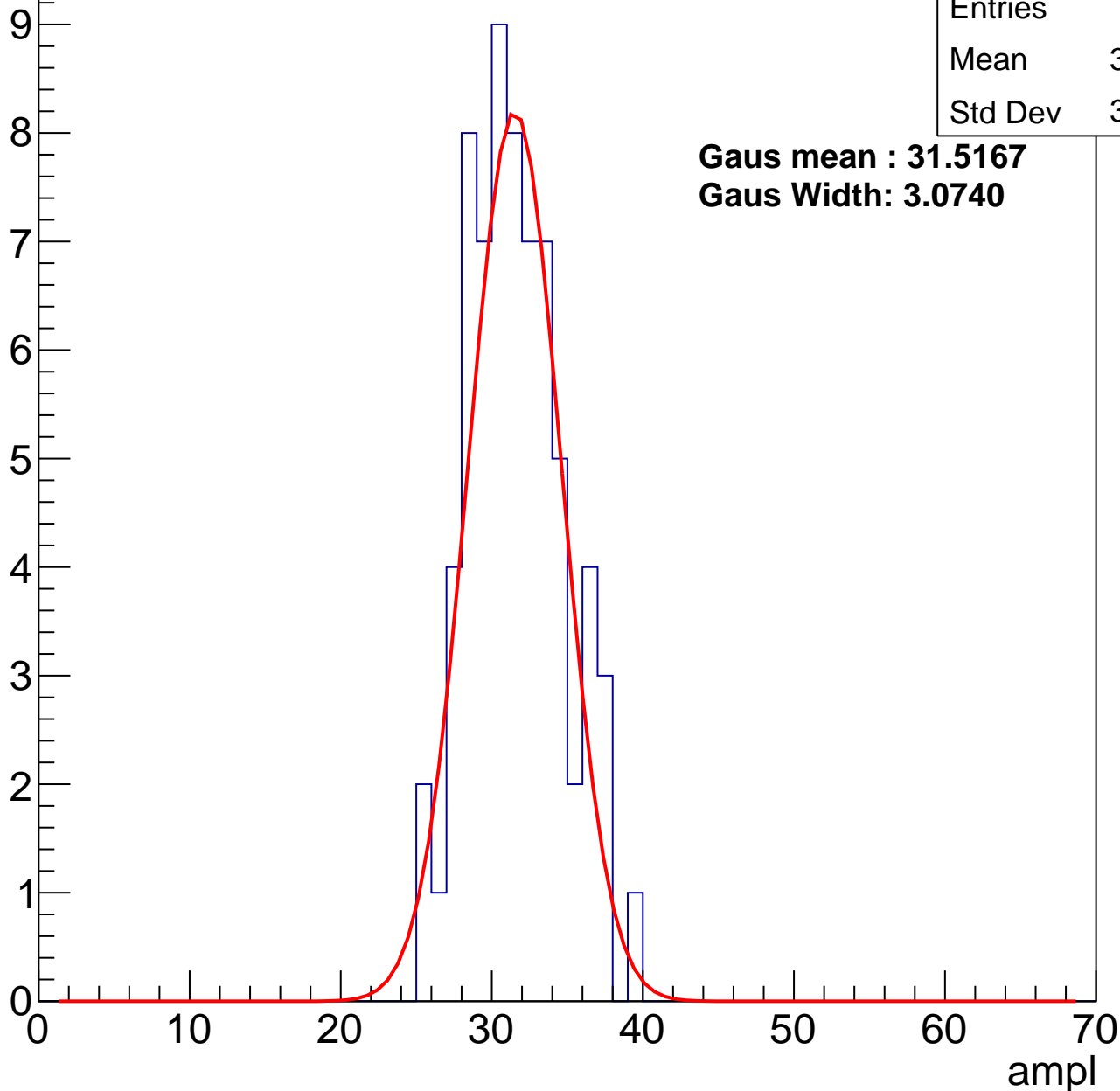
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	31.15
Std Dev	3.098

**Gaus mean : 31.5167**

**Gaus Width: 3.0740**



# B1L101S, U9-ch103, adc1

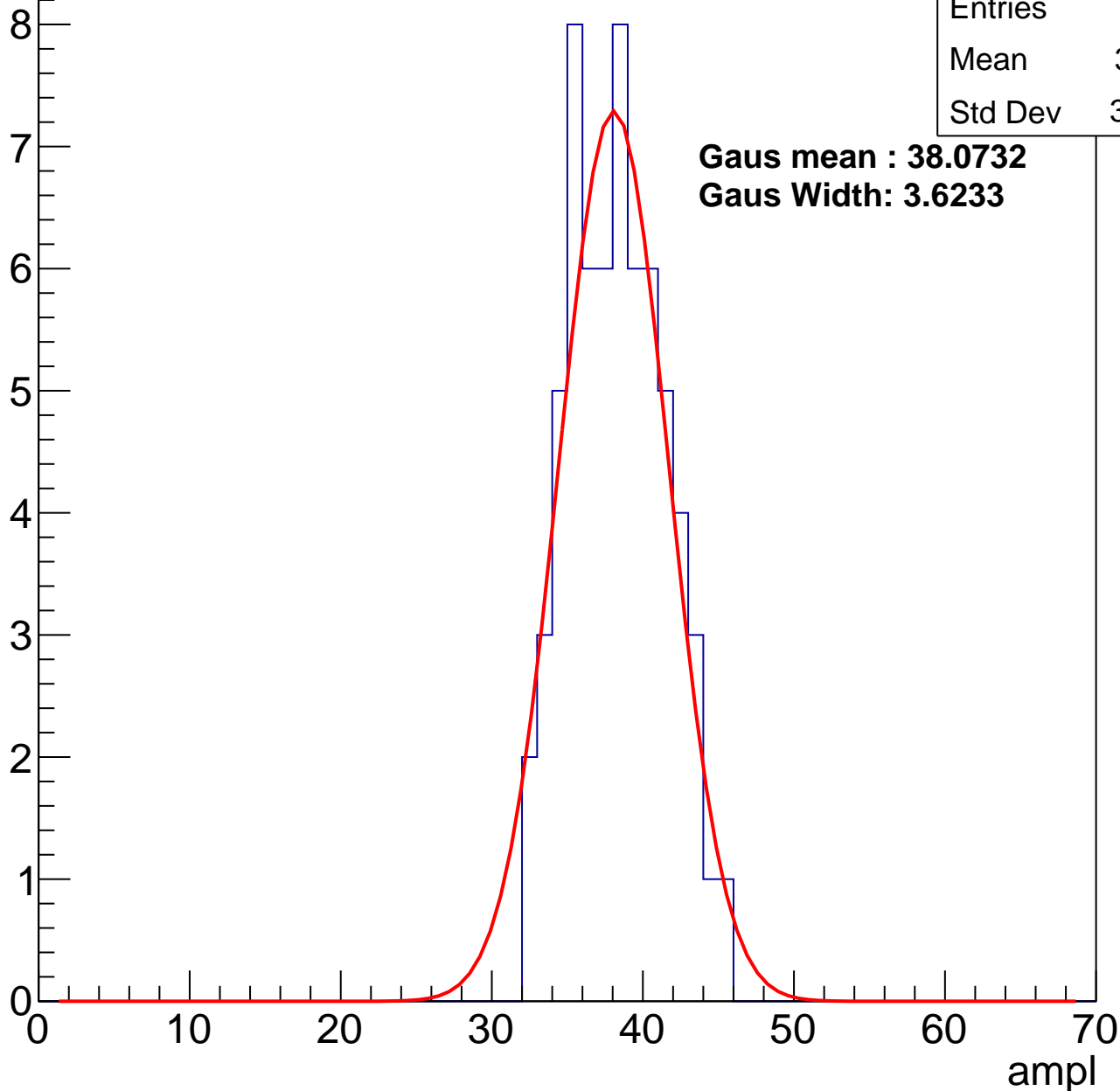
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	37.81
Std Dev	3.127

**Gaus mean : 38.0732**

**Gaus Width: 3.6233**



# B1L101S, U9-ch103, adc2

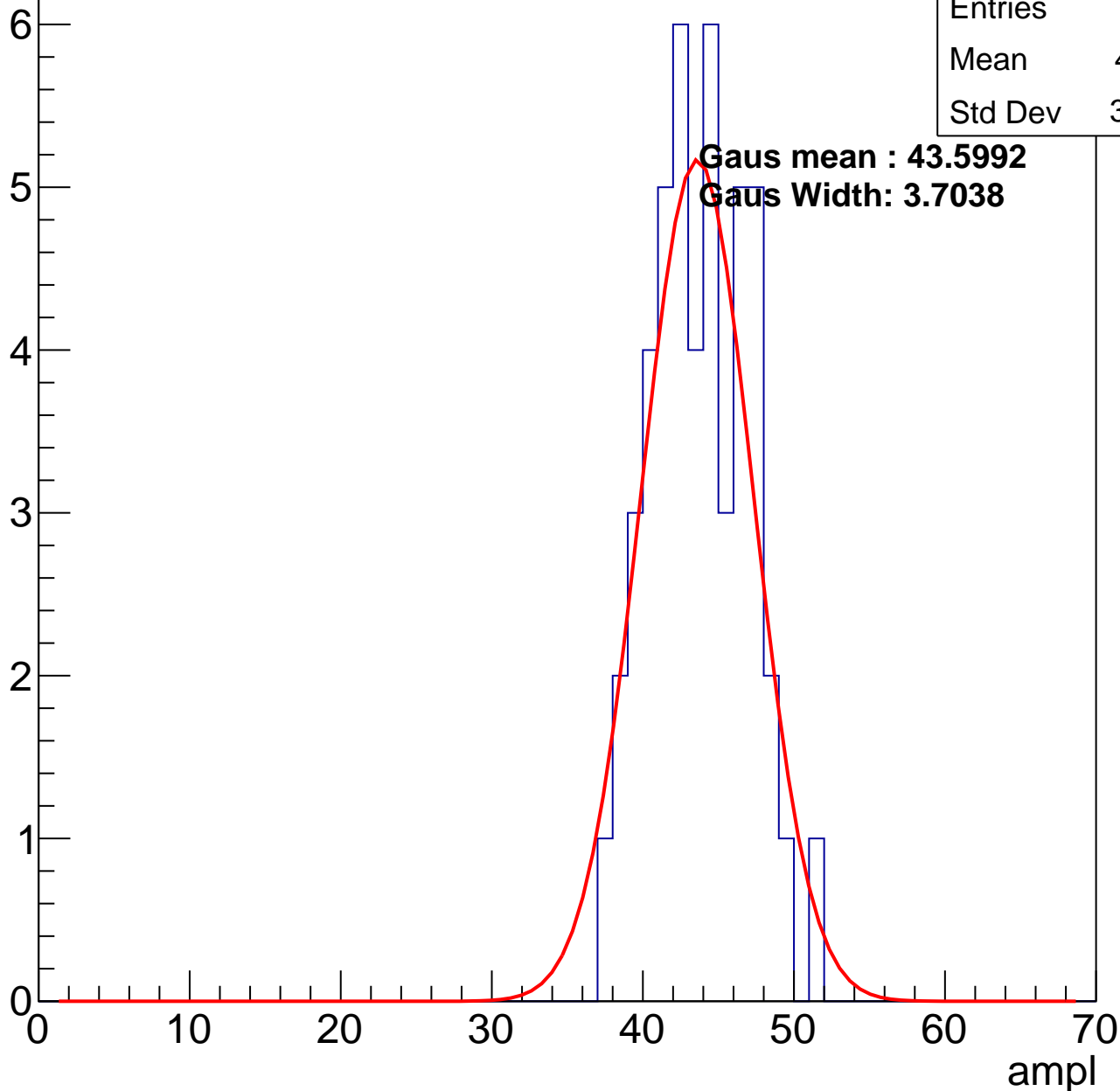
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	43.31
Std Dev	3.176

**Gaus mean : 43.5992**

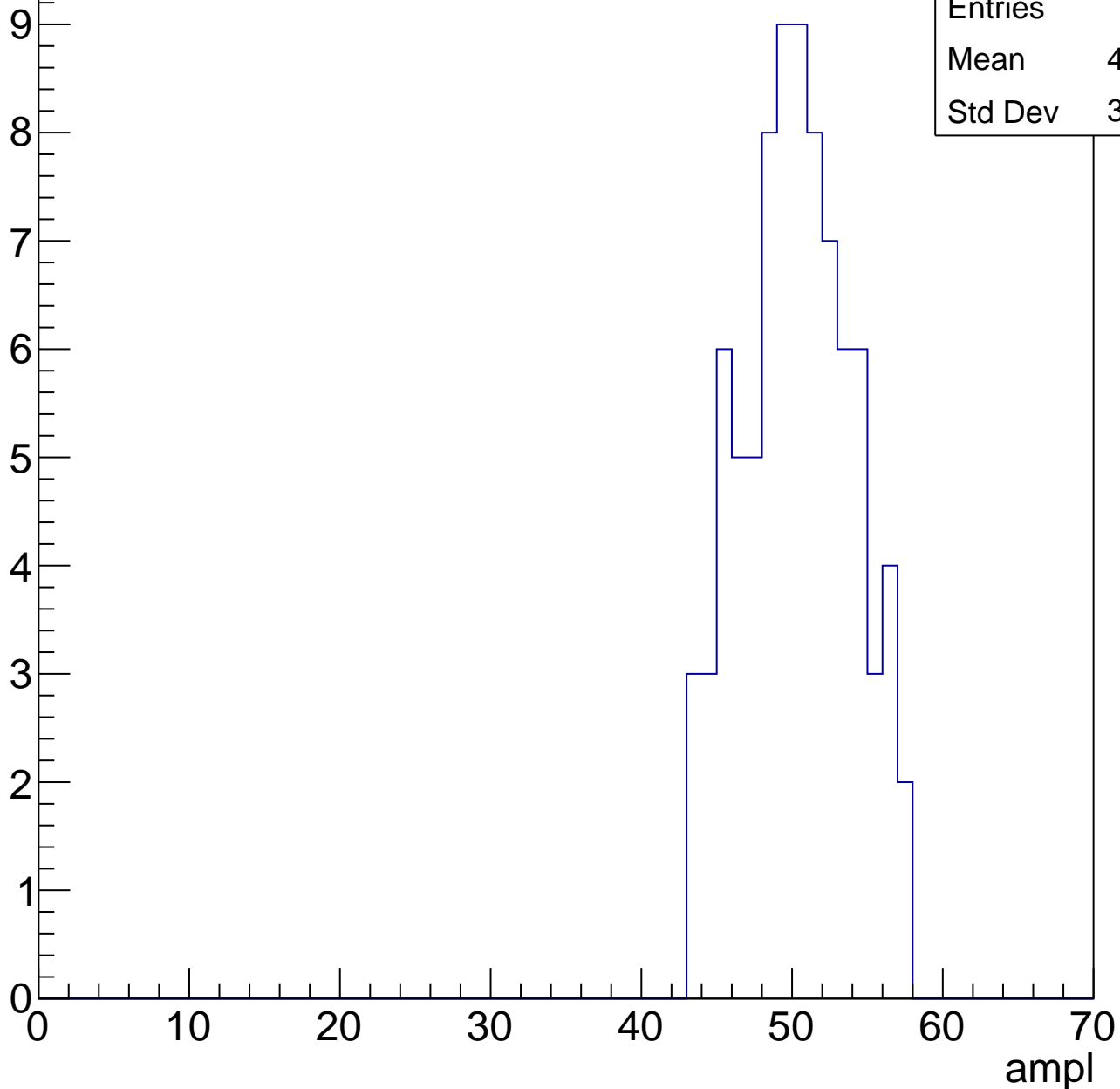
**Gaus Width: 3.7038**



# B1L101S, U9-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



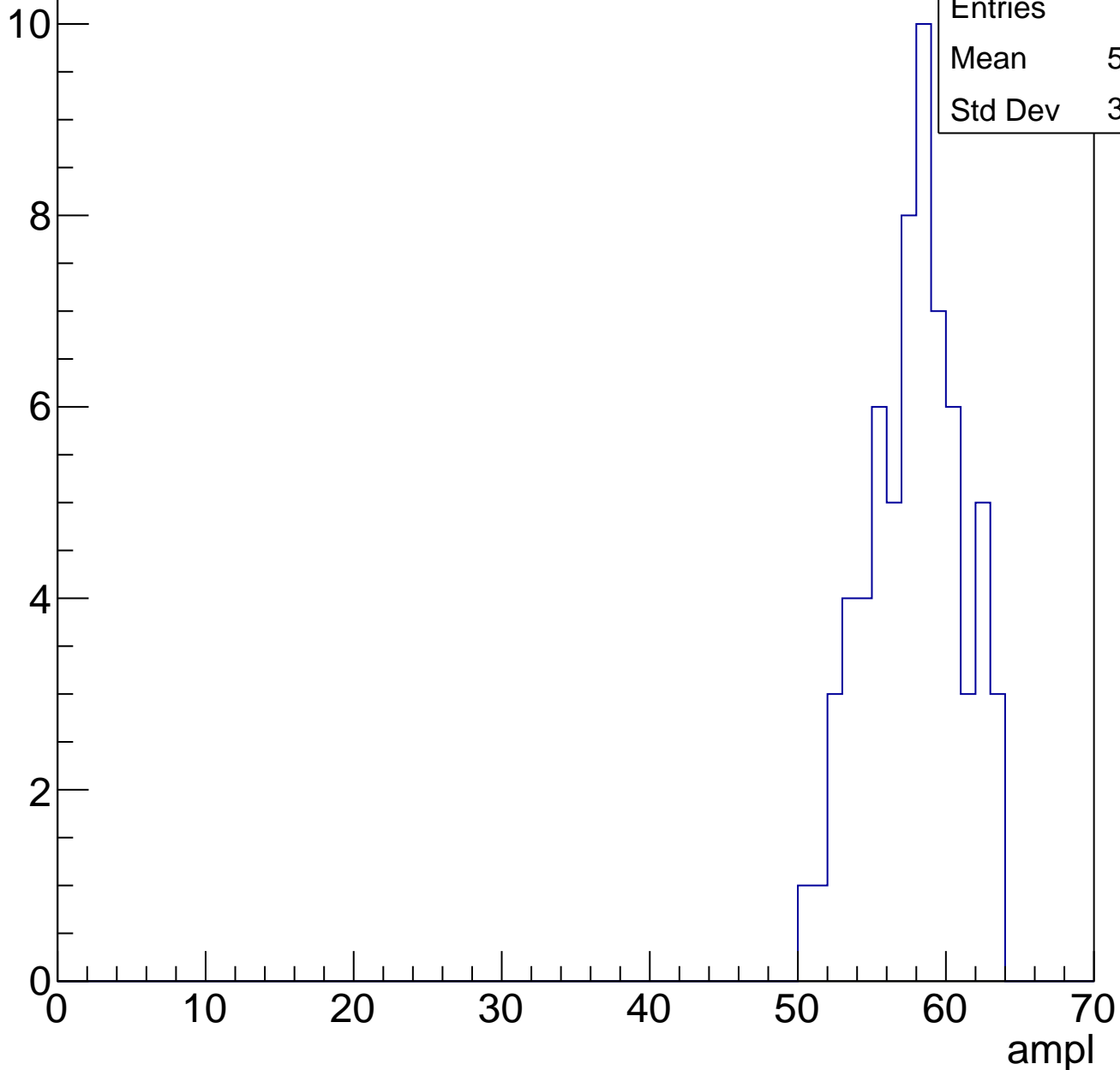
Entries	84
Mean	49.86
Std Dev	3.573

# B1L101S, U9-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	66
Mean	57.36
Std Dev	3.146

Entry

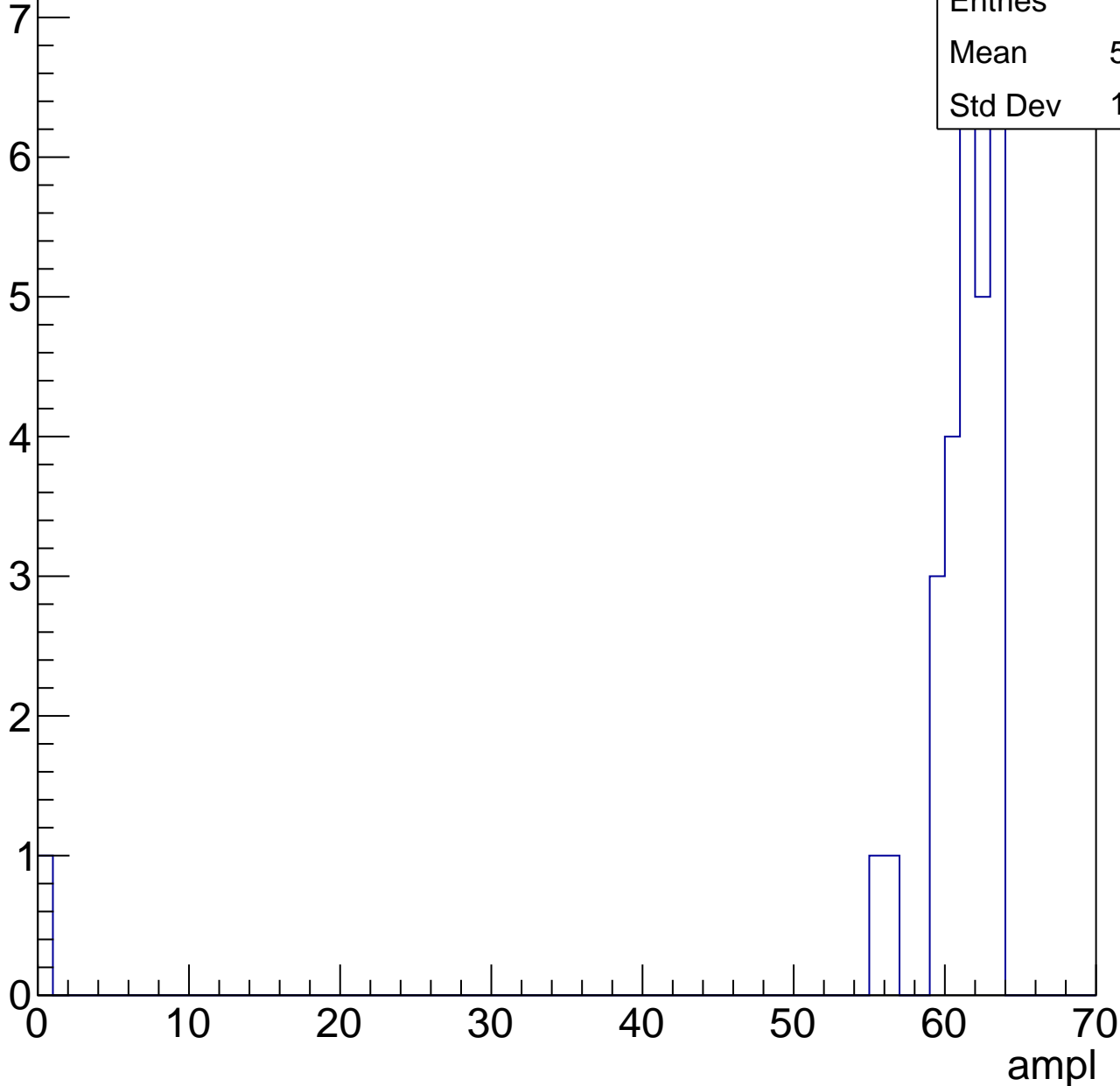


# B1L101S, U9-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	29
Mean	58.83
Std Dev	11.29



# B1L101S, U9-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L101S, U9-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U9-ch104, adc0

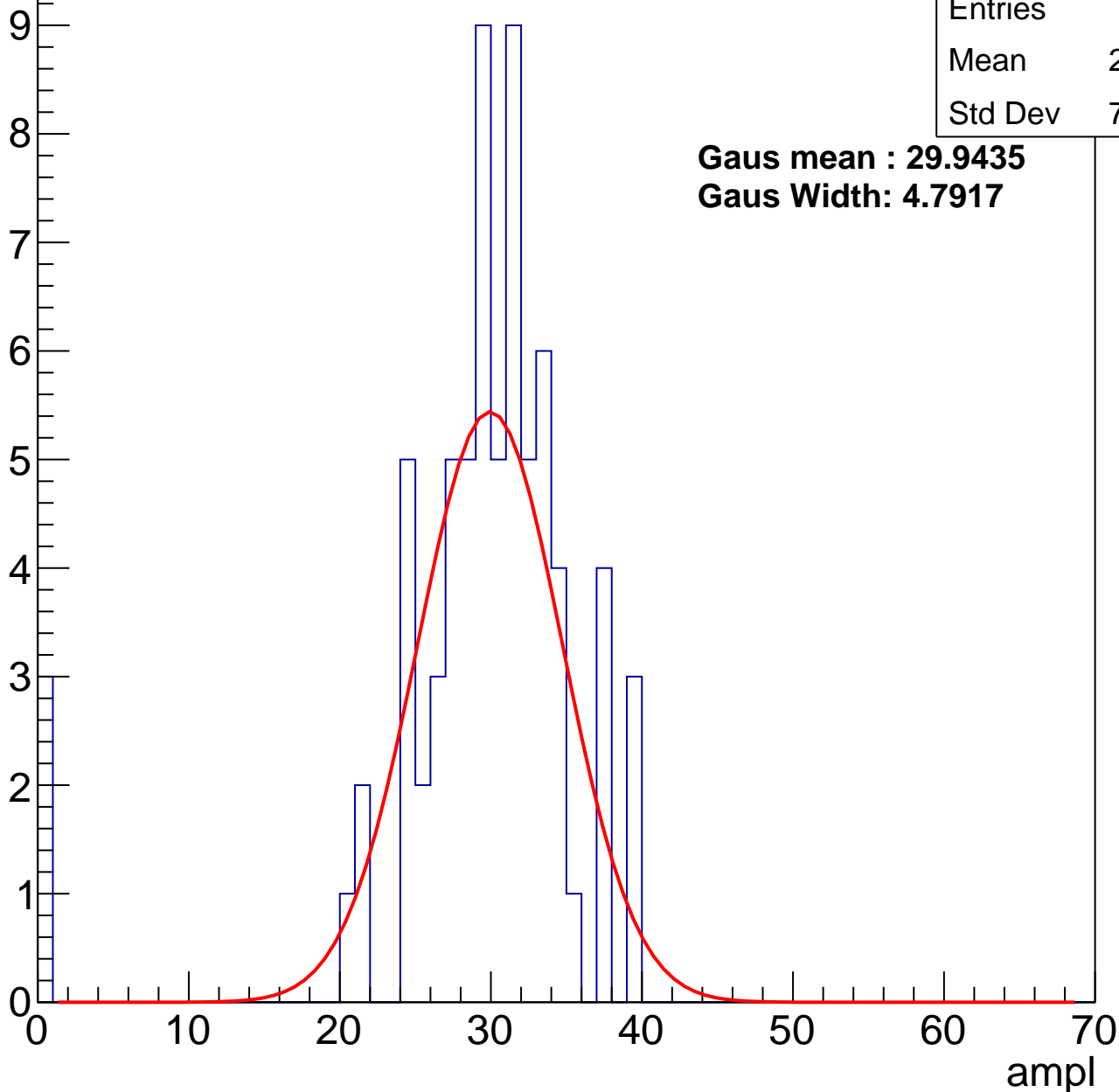
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	28.74
Std Dev	7.274

**Gaus mean : 29.9435**

**Gaus Width: 4.7917**



# B1L101S, U9-ch104, adc1

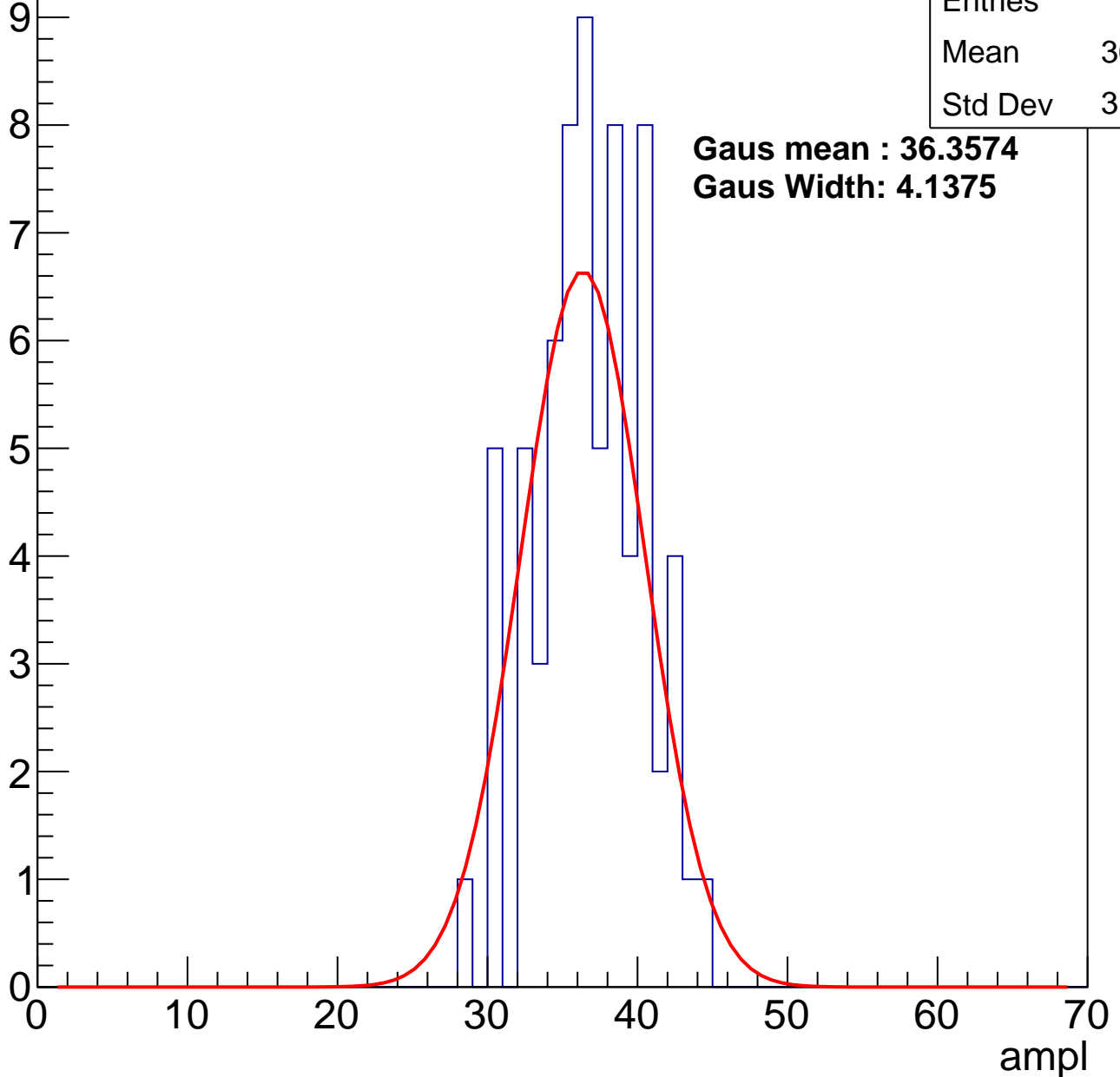
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	36.39
Std Dev	3.547

**Gaus mean : 36.3574**

**Gaus Width: 4.1375**



# B1L101S, U9-ch104, adc2

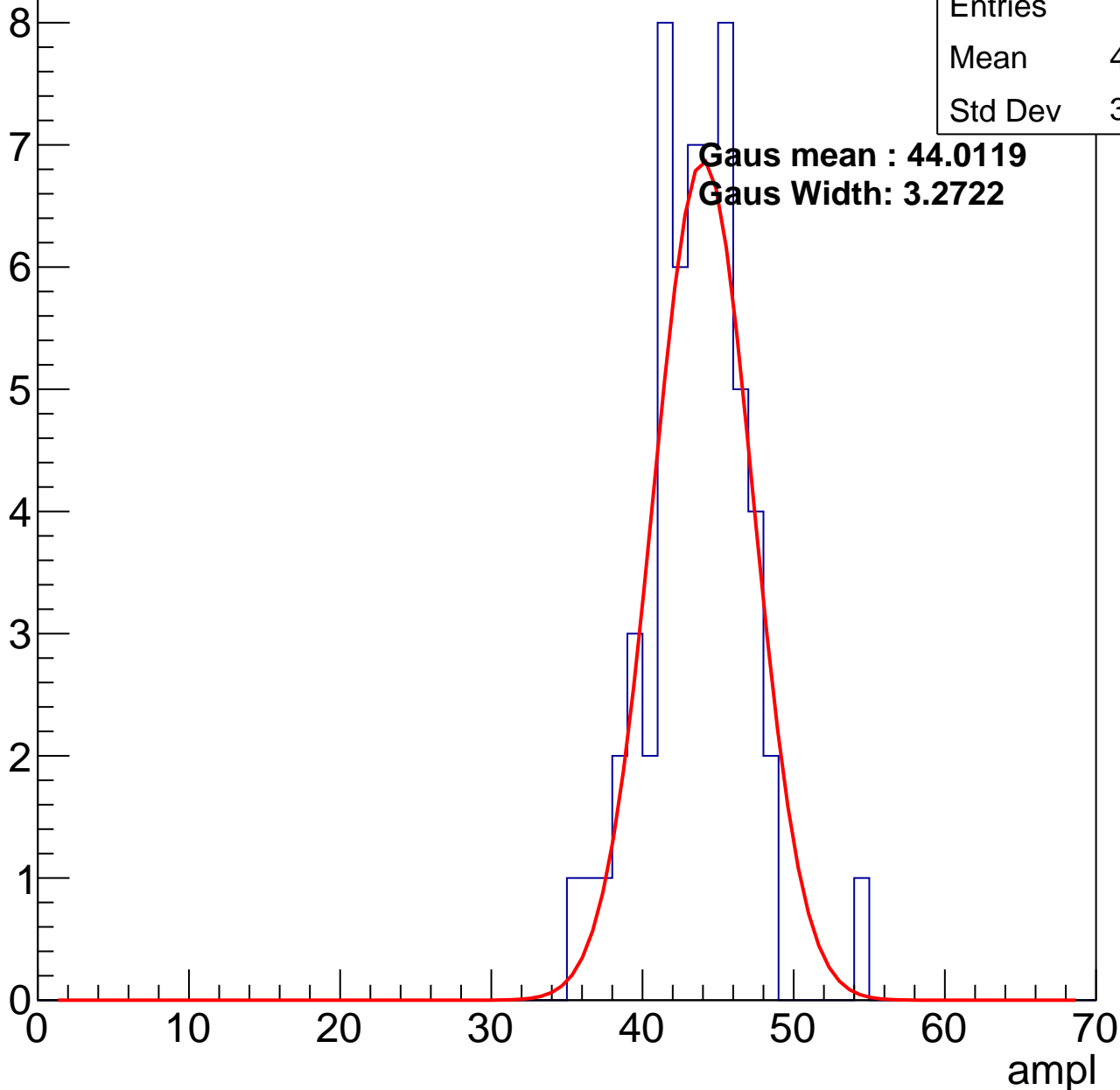
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	43.07
Std Dev	3.274

**Gaus mean : 44.0119**

**Gaus Width: 3.2722**



# B1L101S, U9-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	67
Mean	49.67
Std Dev	3.197

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

70

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

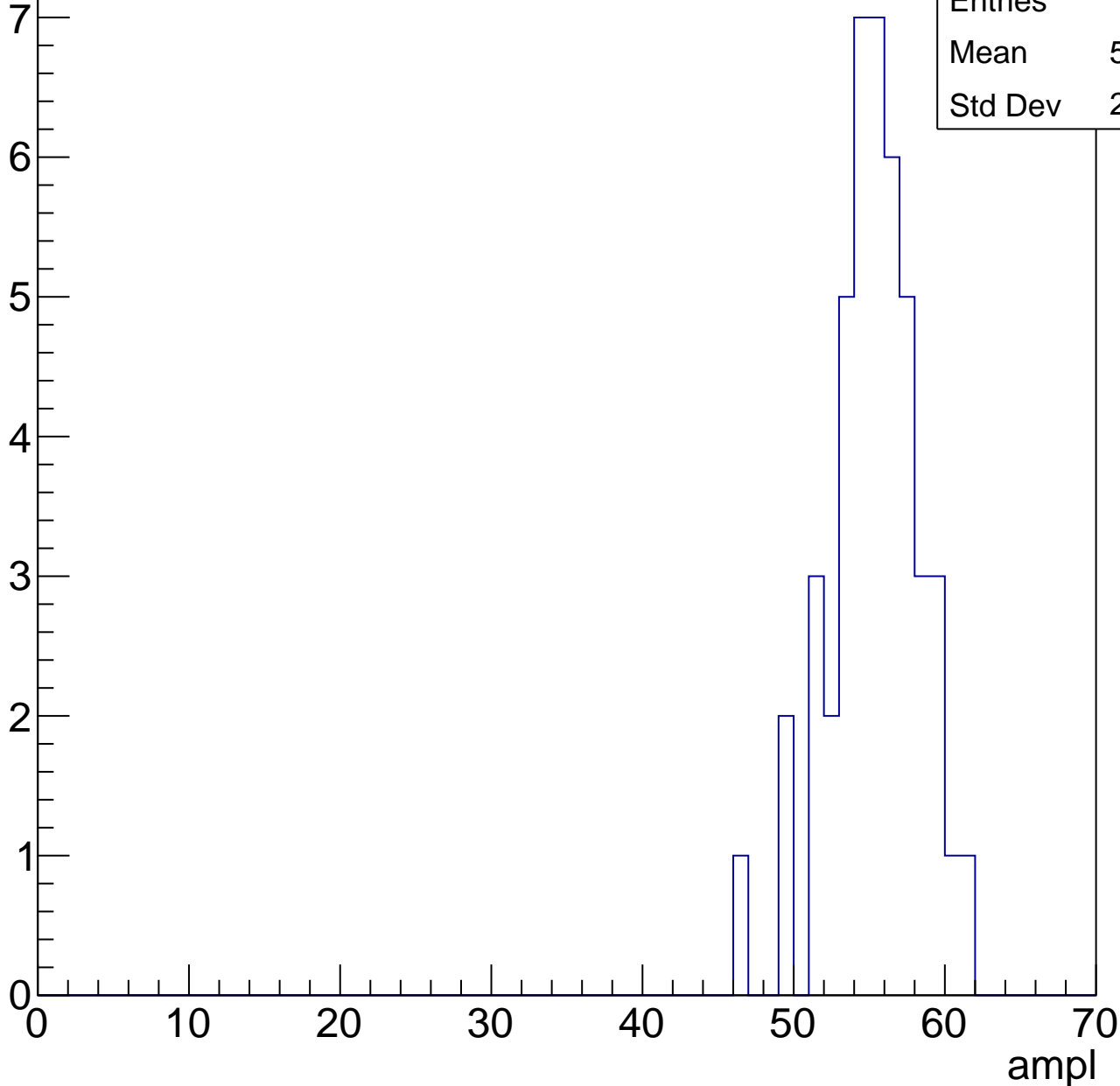
70

# B1L101S, U9-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	54.83
Std Dev	2.973

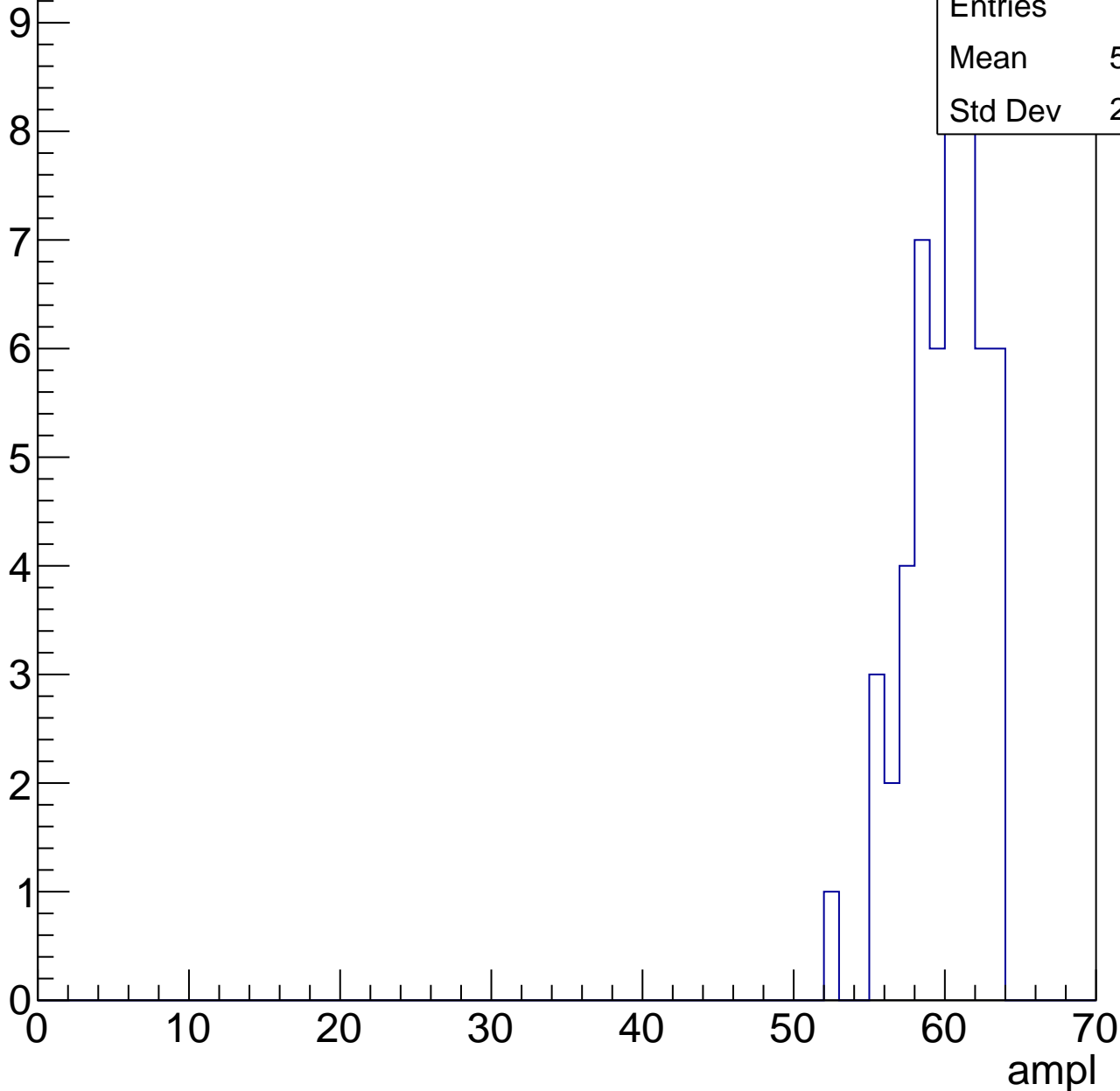


# B1L101S, U9-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

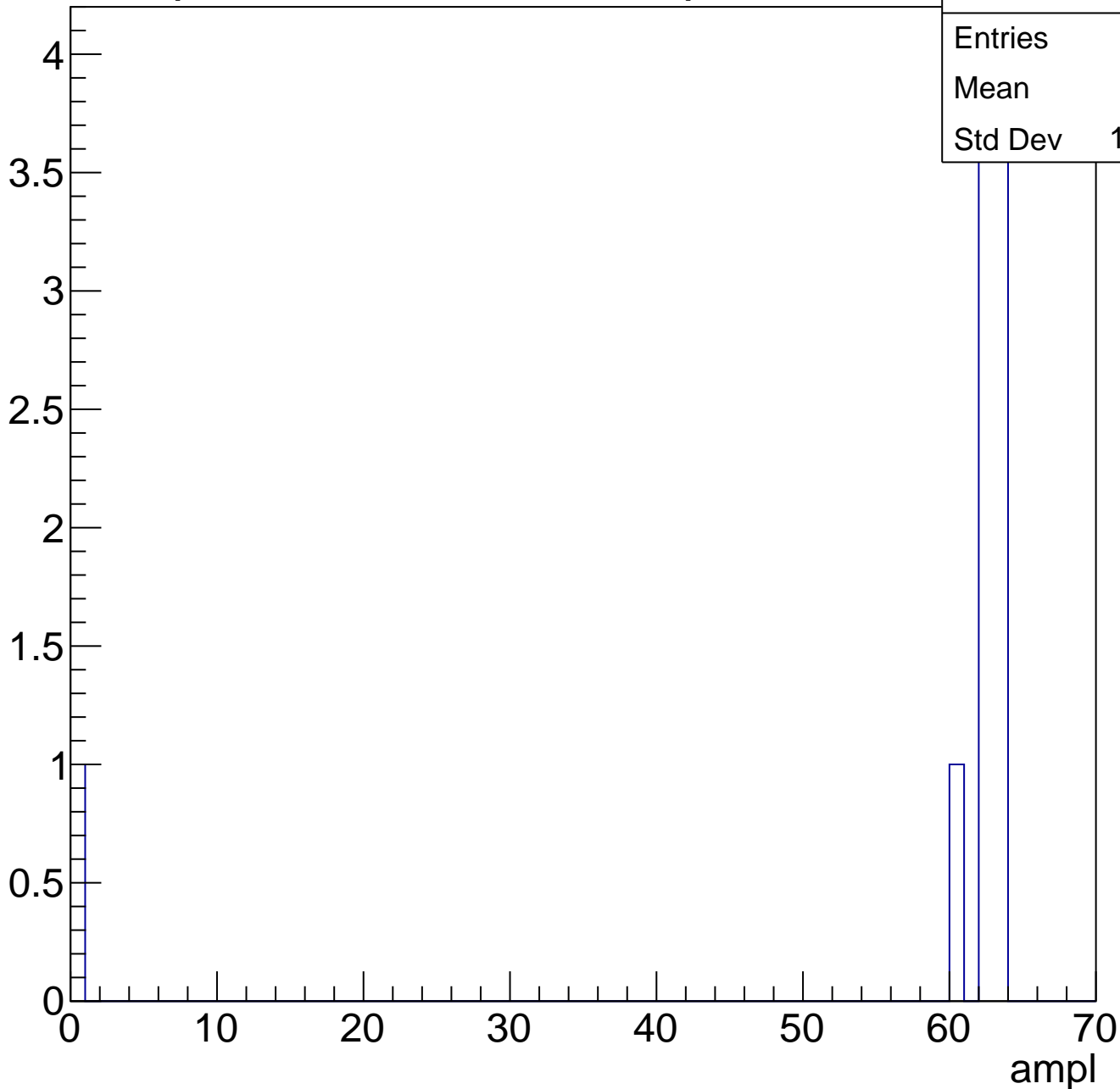
Entries	52
Mean	59.54
Std Dev	2.469



# B1L101S, U9-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U9-ch105, adc0

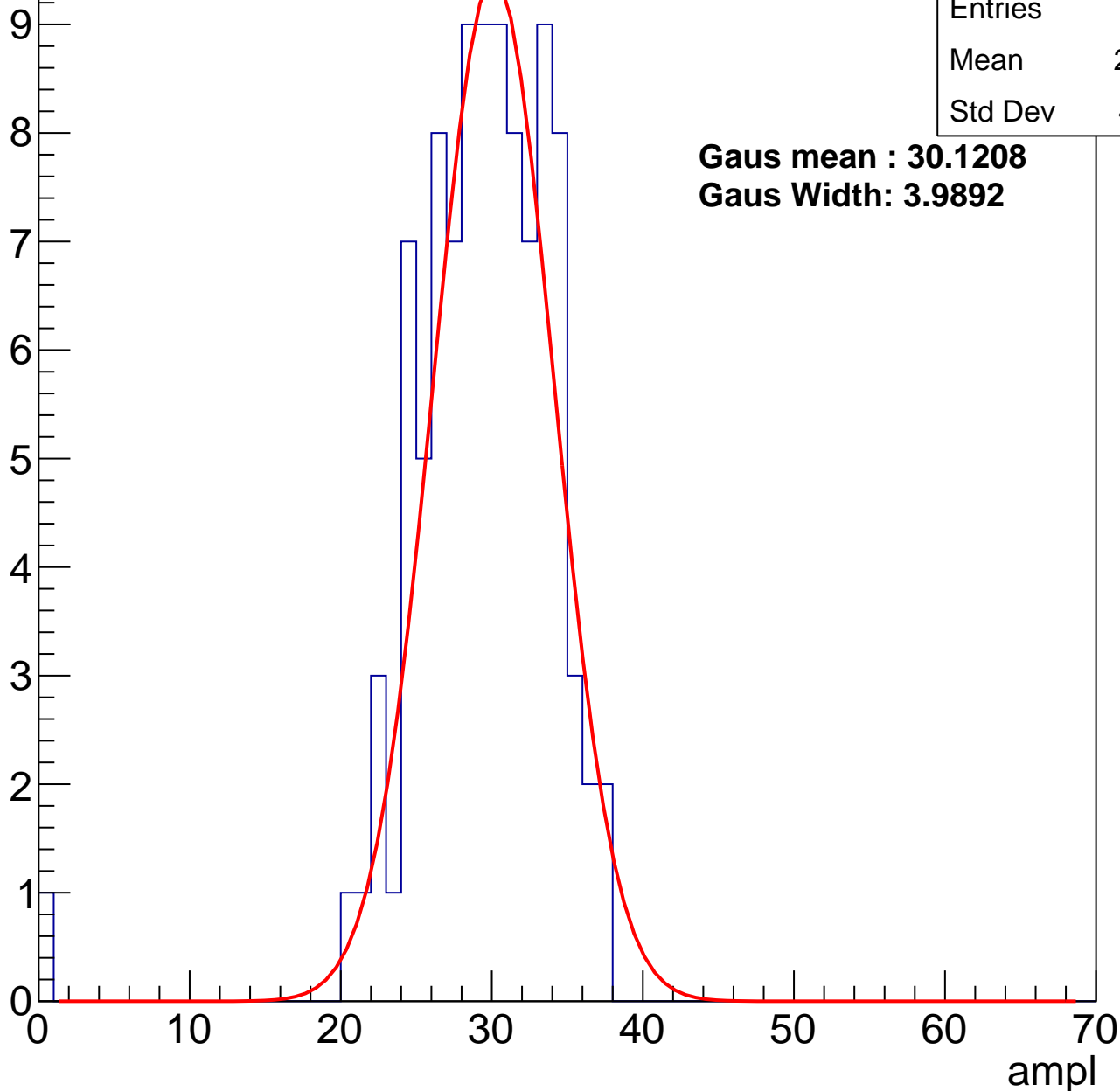
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	100
Mean	28.95
Std Dev	4.811

**Gaus mean : 30.1208**

**Gaus Width: 3.9892**



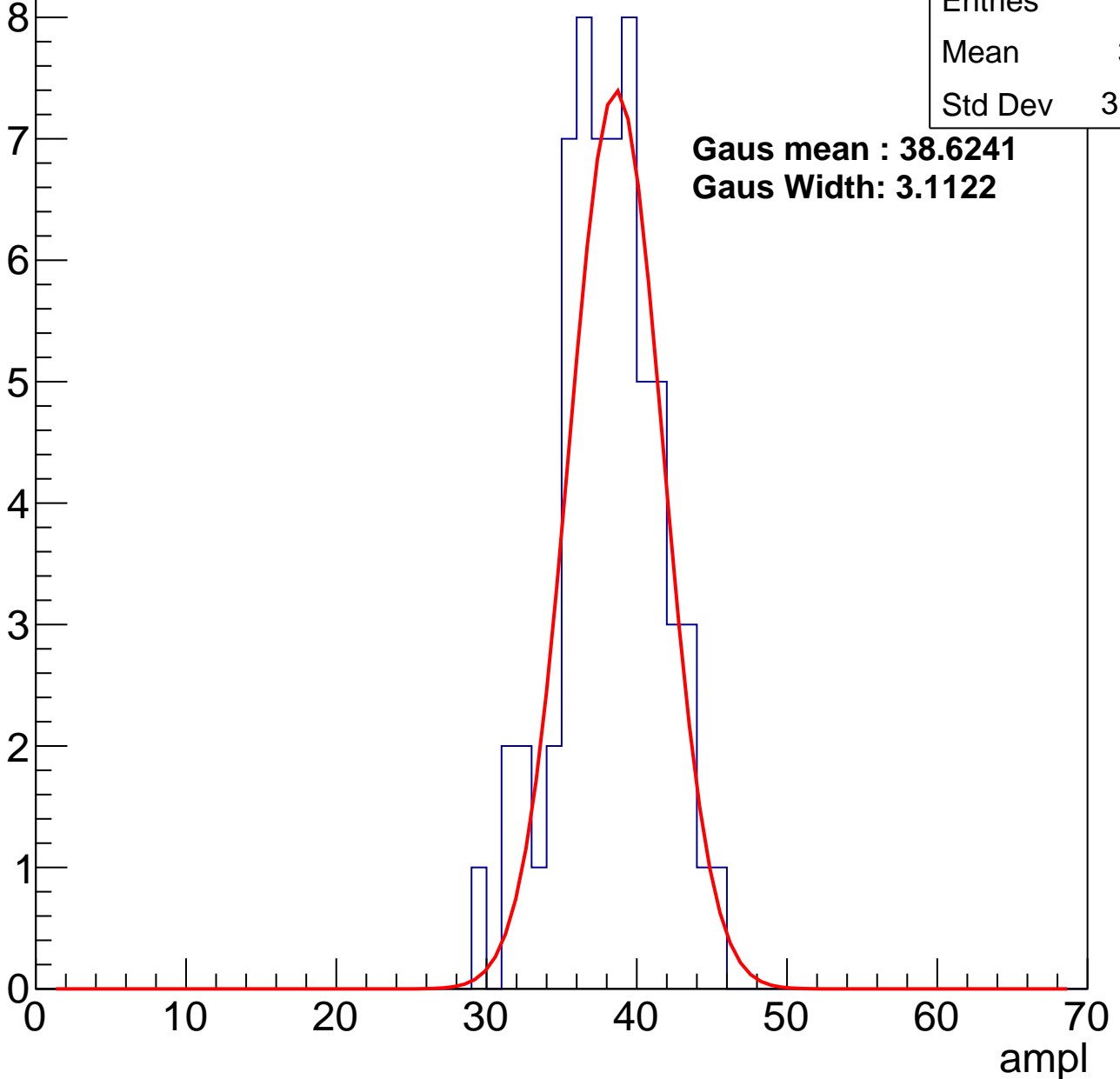
# B1L101S, U9-ch105, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	37.7
Std Dev	3.298

**Gaus mean : 38.6241**  
**Gaus Width: 3.1122**



# B1L101S, U9-ch105, adc2

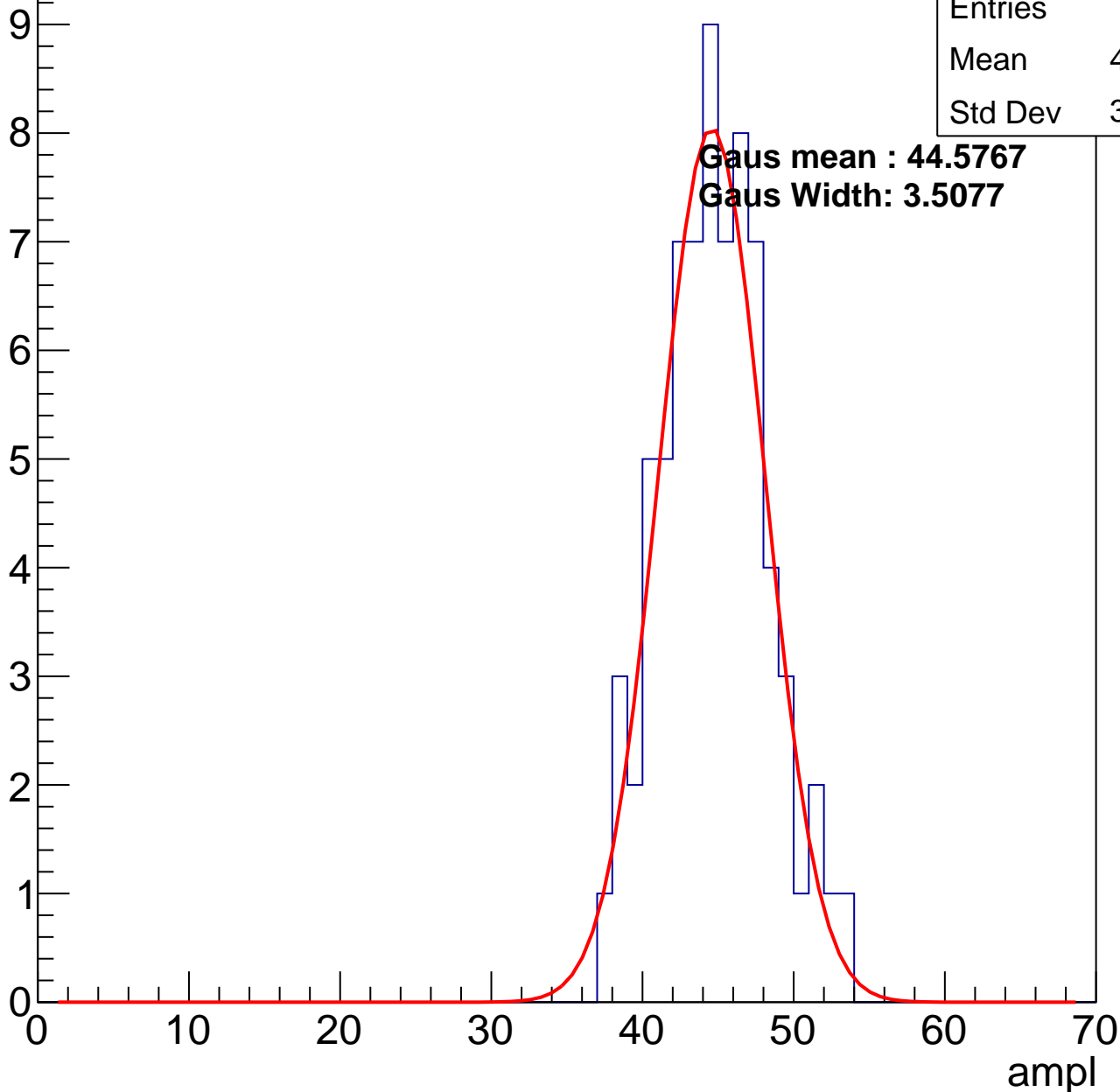
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	44.29
Std Dev	3.474

**Gaus mean : 44.5767**

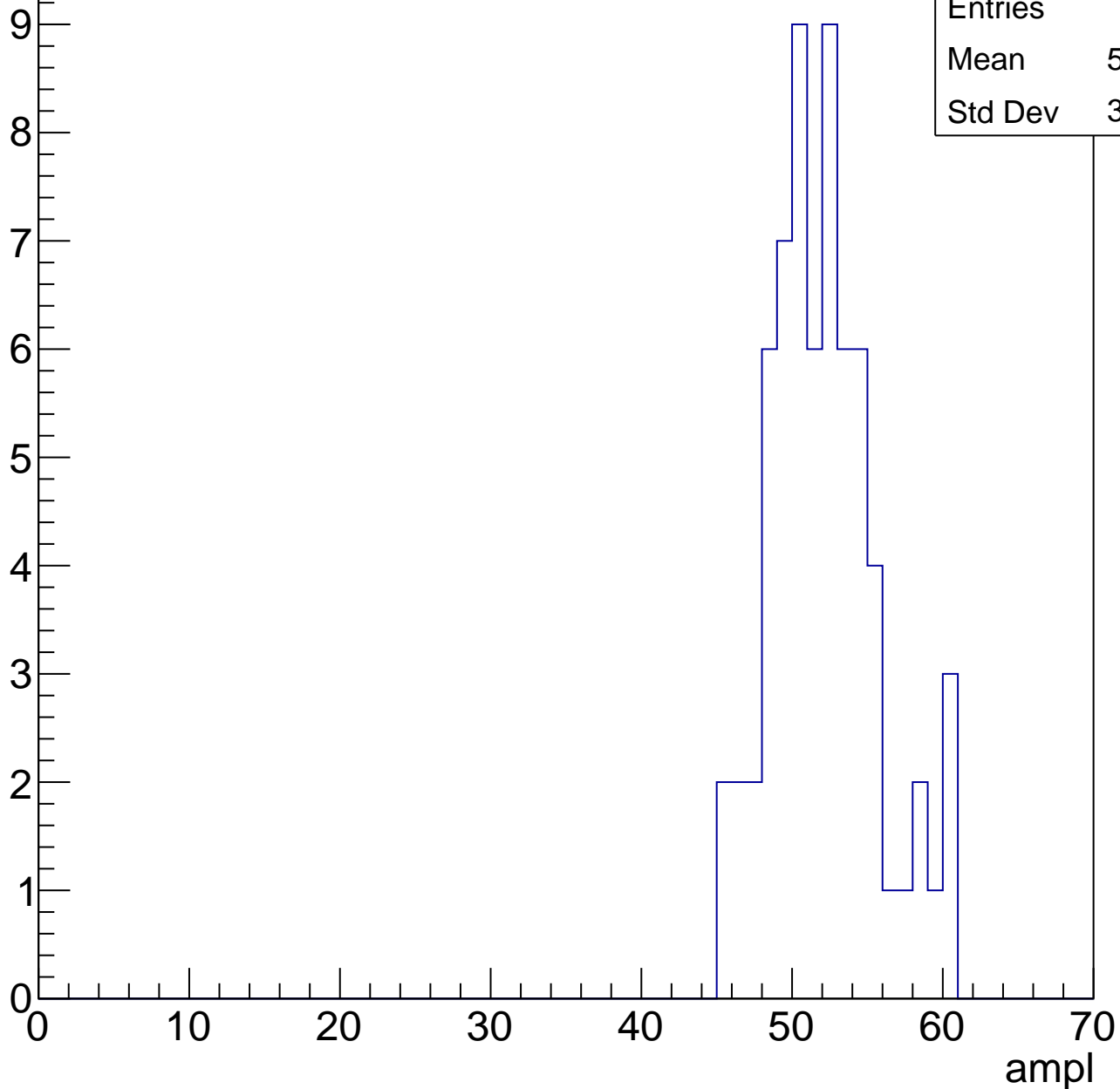
**Gaus Width: 3.5077**



# B1L101S, U9-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

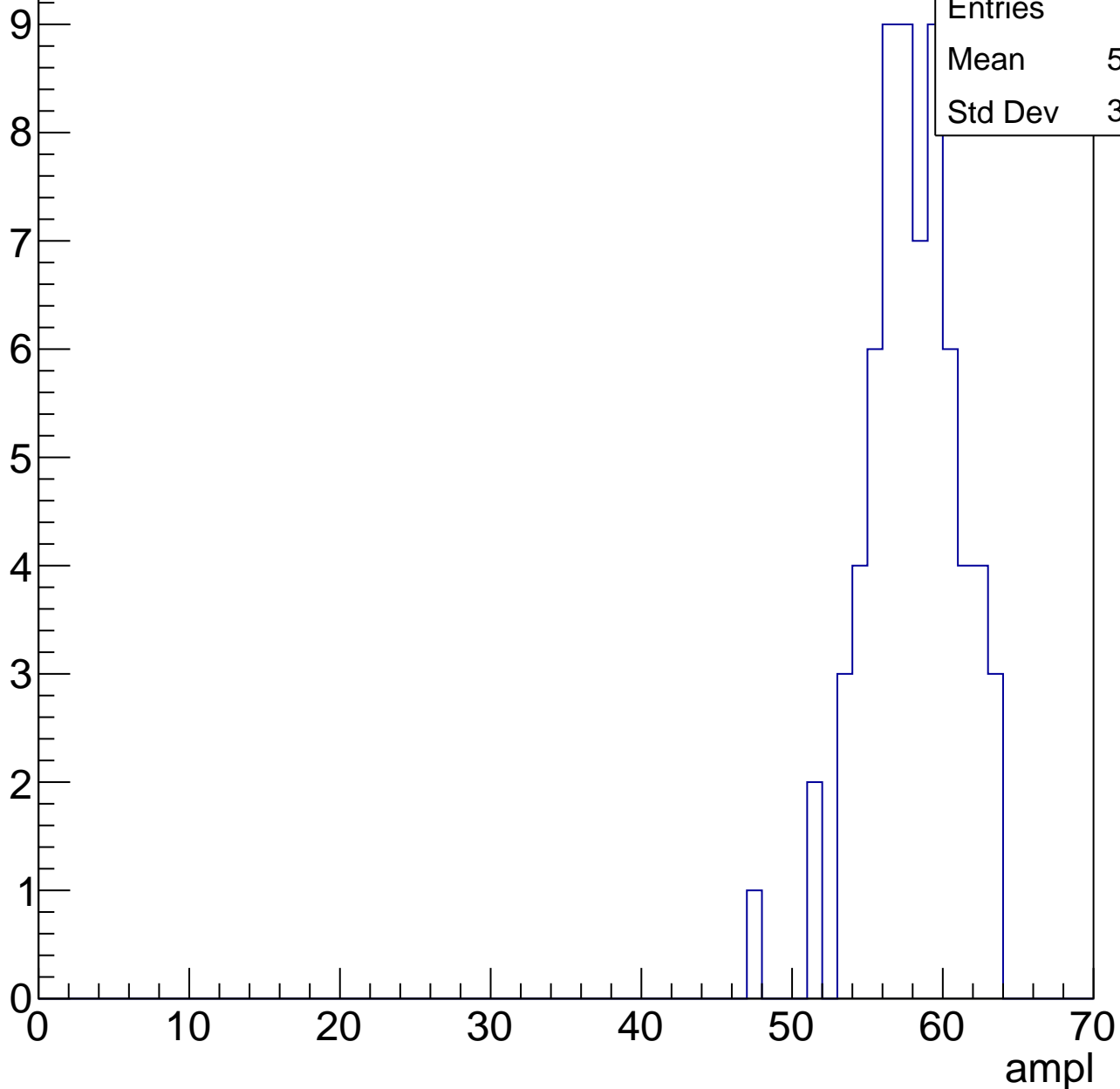
Entry



# B1L101S, U9-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

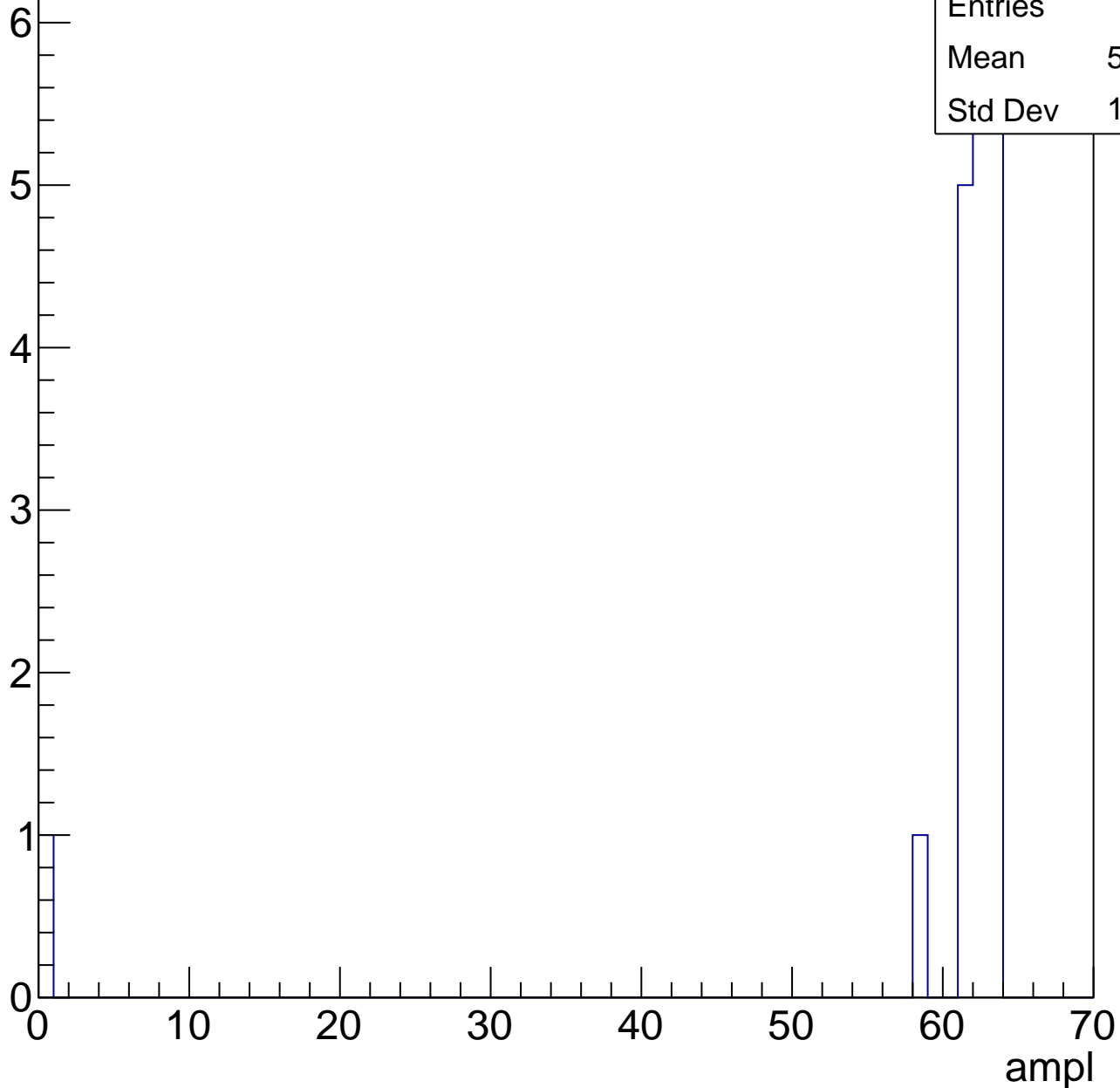
Entry



# B1L101S, U9-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U9-ch106, adc0

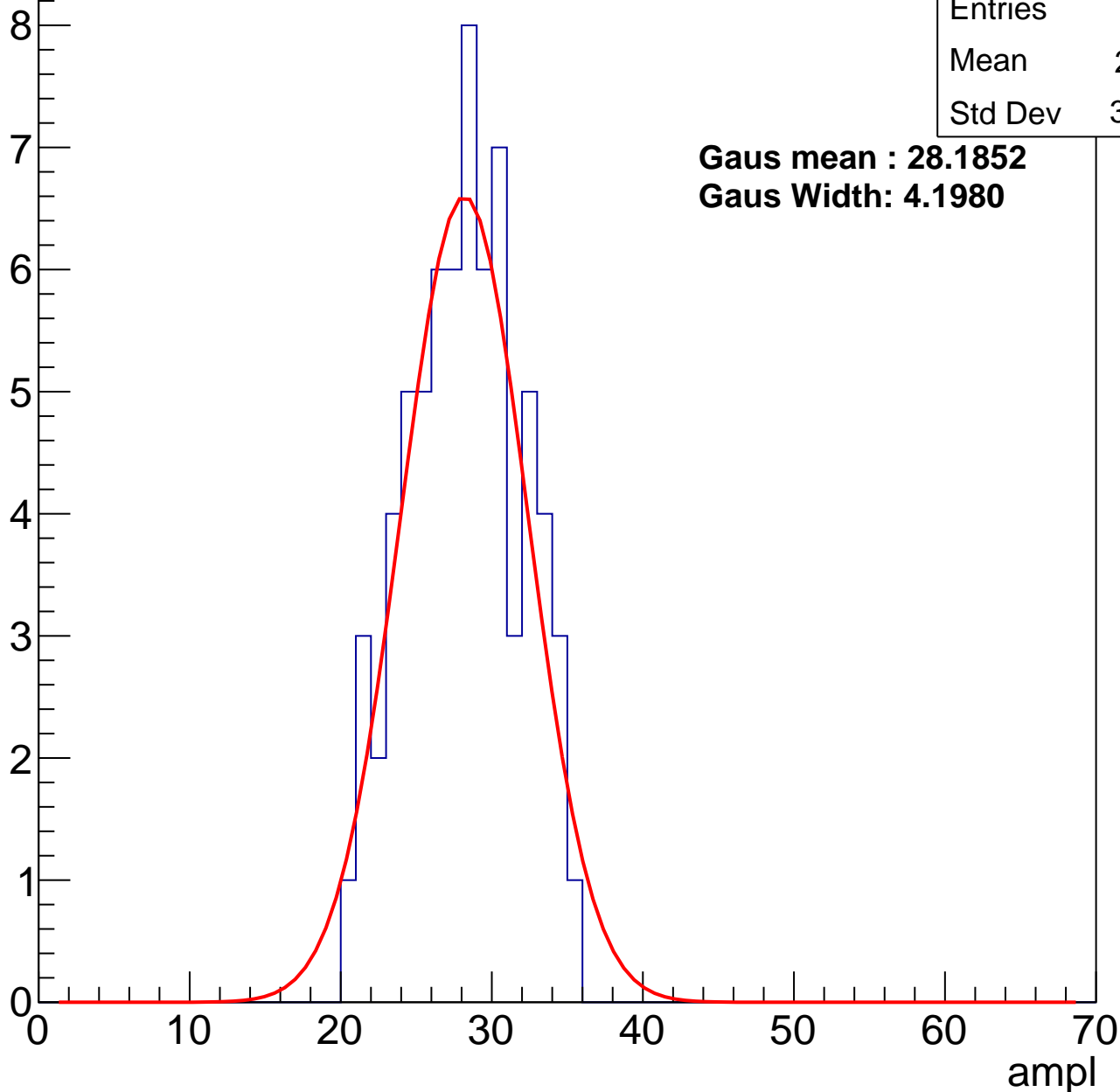
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	27.71
Std Dev	3.672

**Gaus mean : 28.1852**

**Gaus Width: 4.1980**



# B1L101S, U9-ch106, adc1

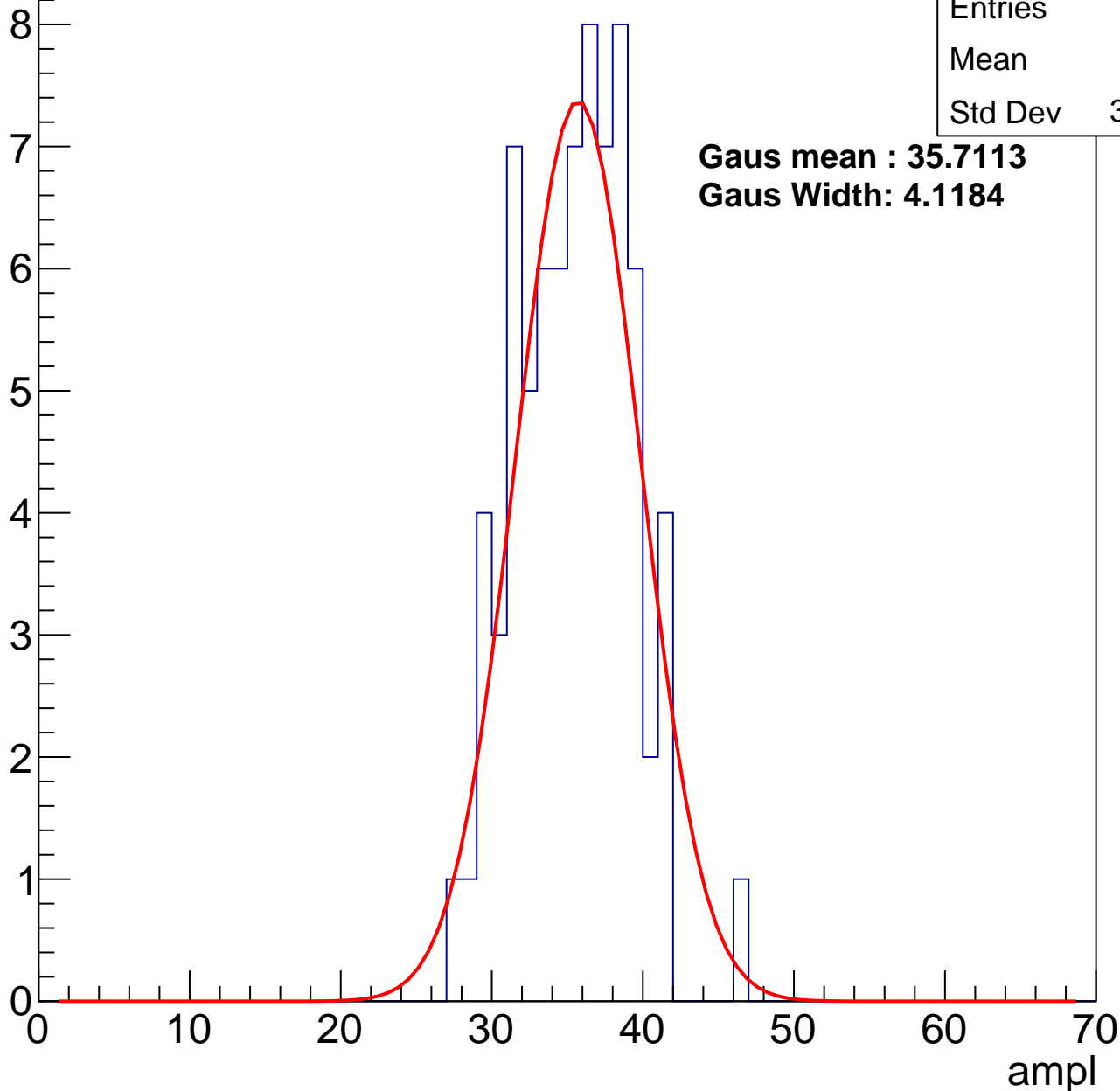
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	35
Std Dev	3.696

**Gaus mean : 35.7113**

**Gaus Width: 4.1184**



# B1L101S, U9-ch106, adc2

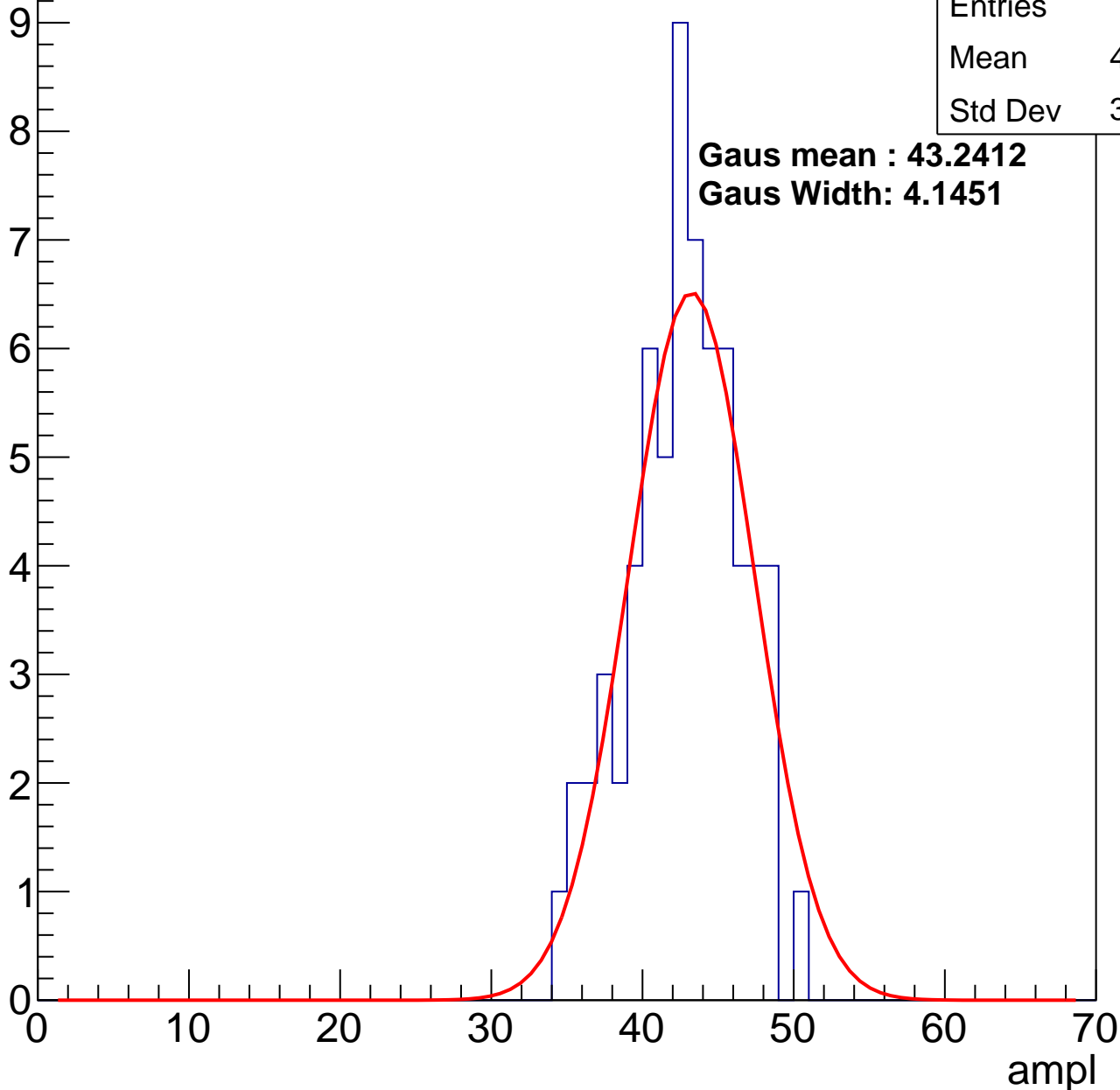
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	42.29
Std Dev	3.605

**Gaus mean : 43.2412**

**Gaus Width: 4.1451**

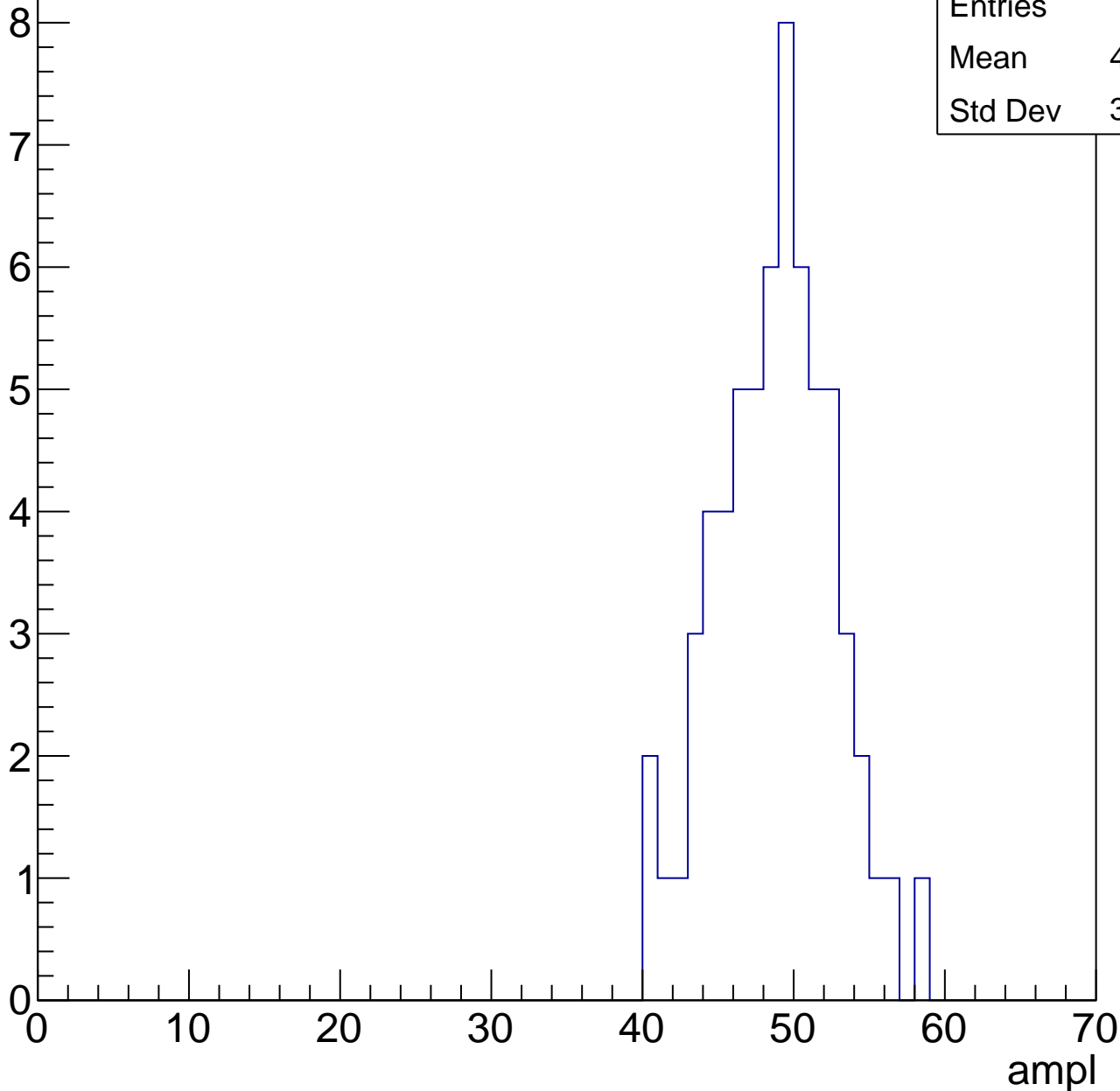


# B1L101S, U9-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

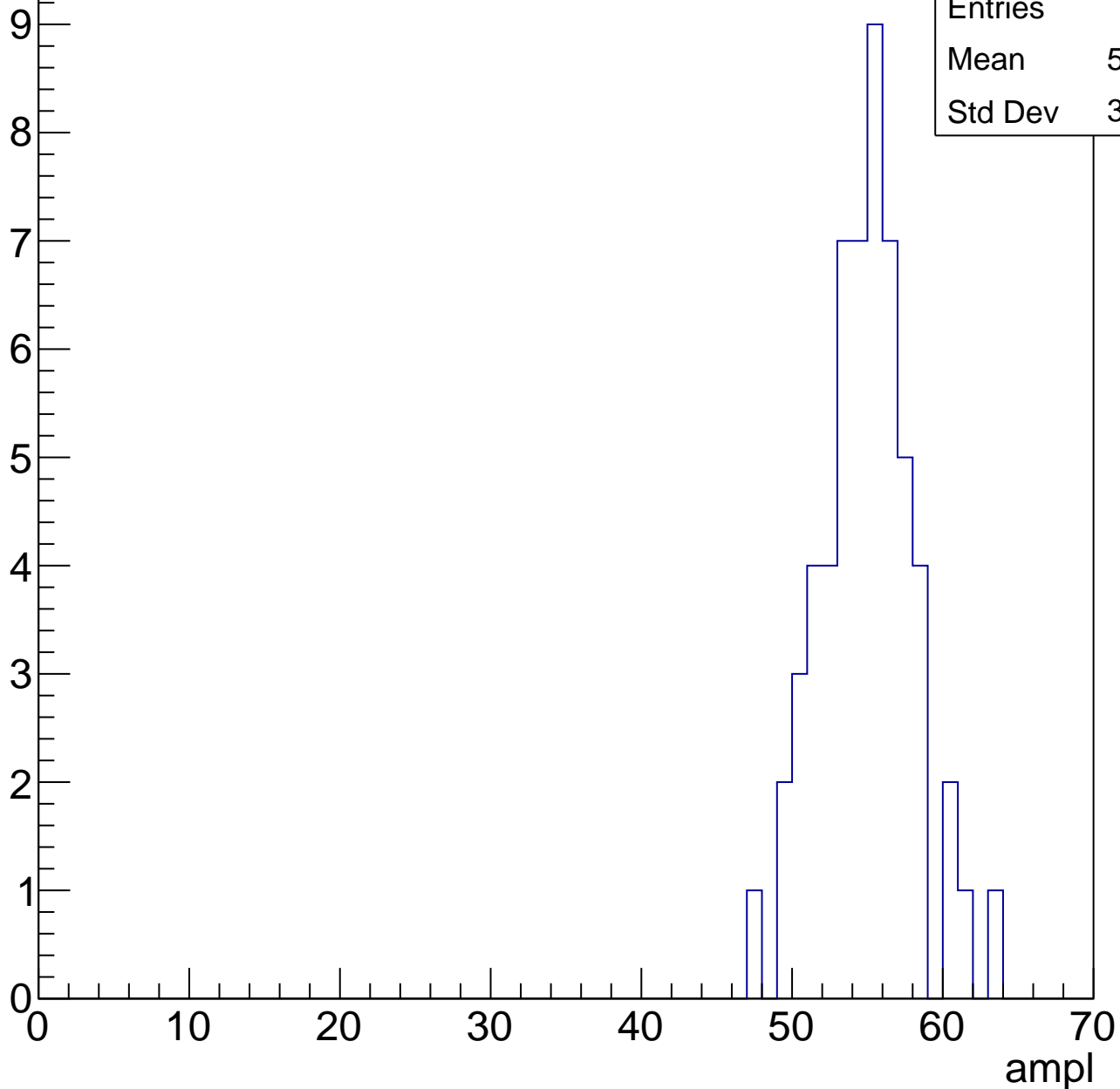
Entries	63
Mean	48.32
Std Dev	3.829



# B1L101S, U9-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

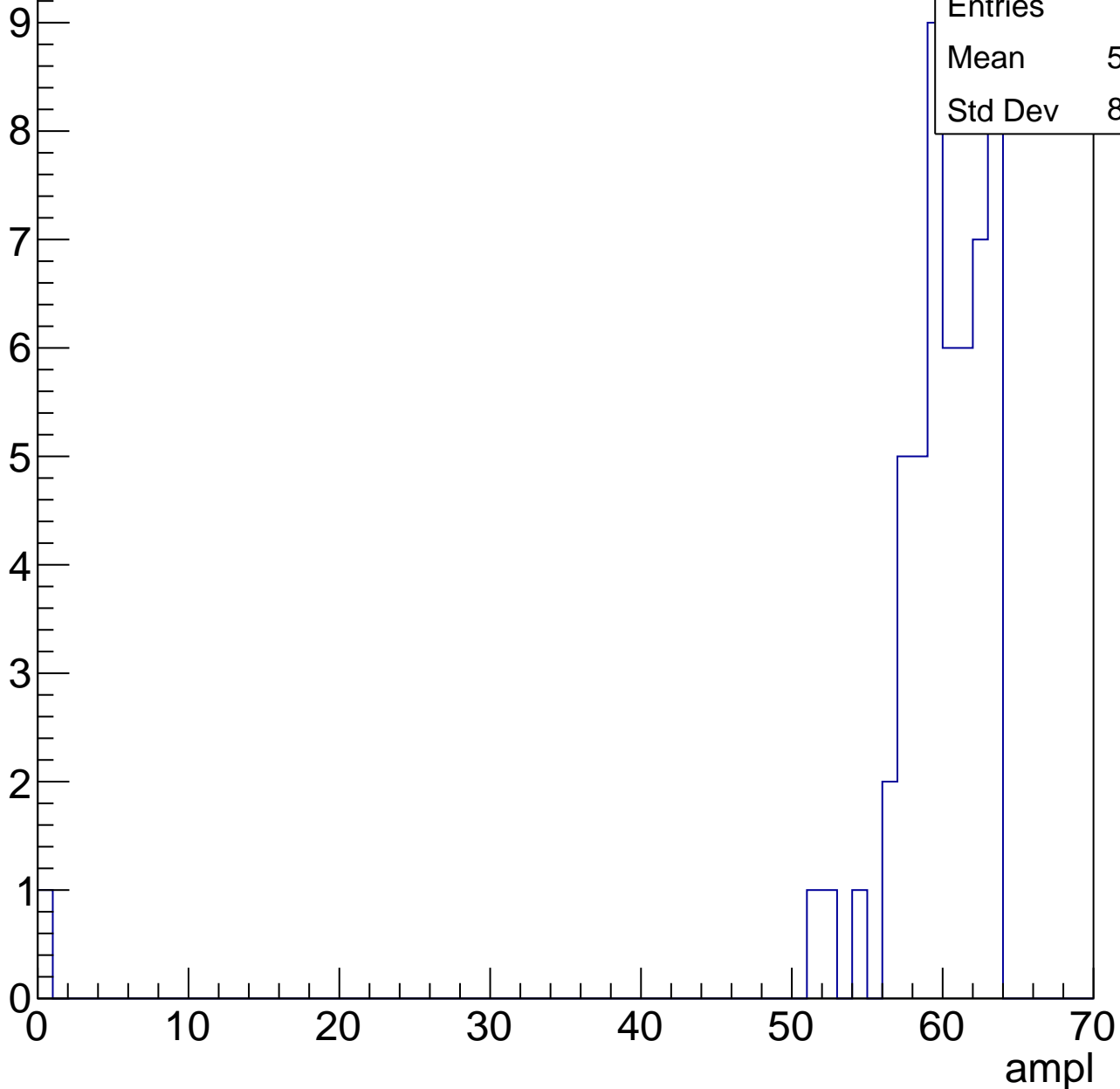
Entry



# B1L101S, U9-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

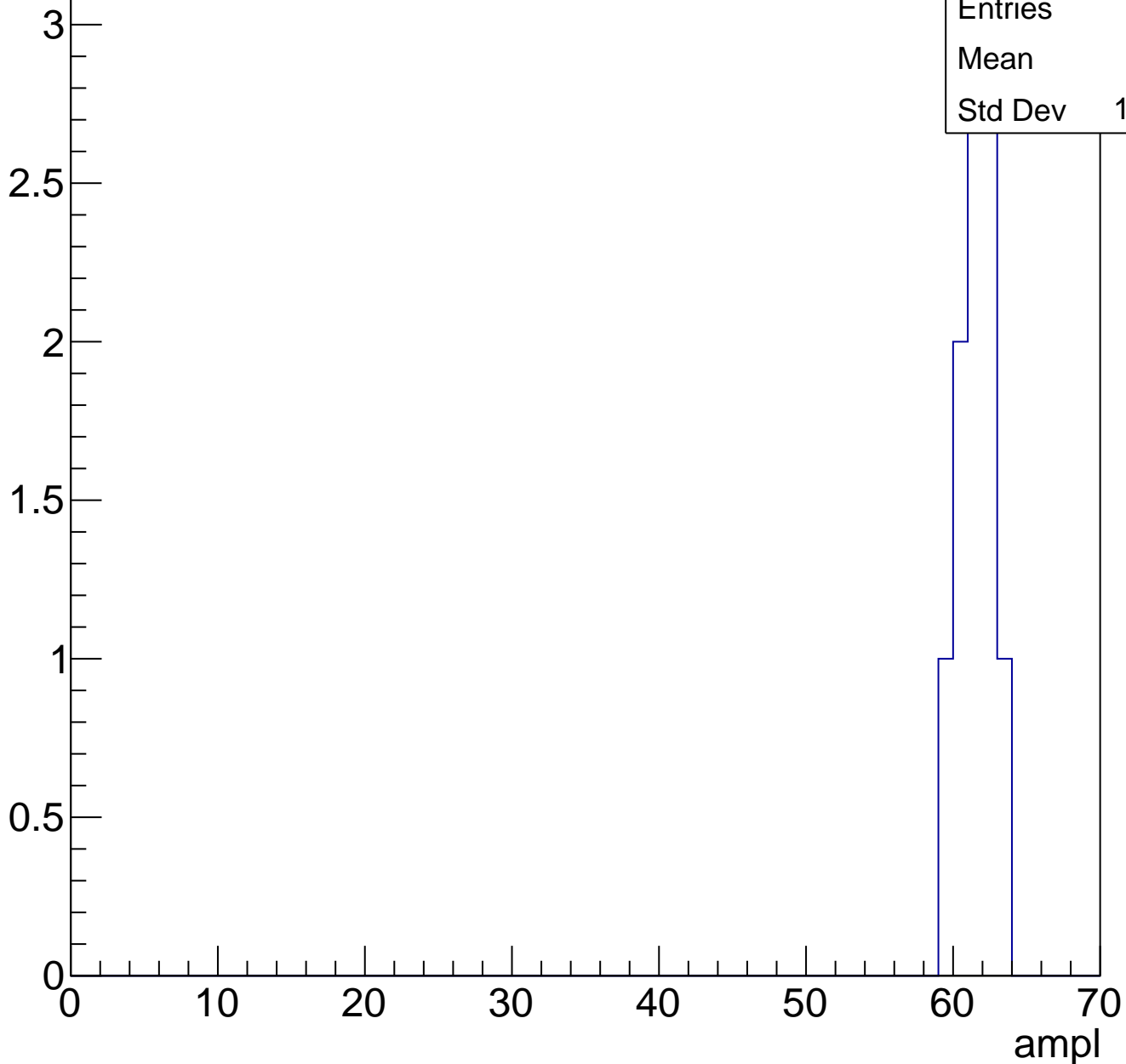
Entry



# B1L101S, U9-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch107, adc0

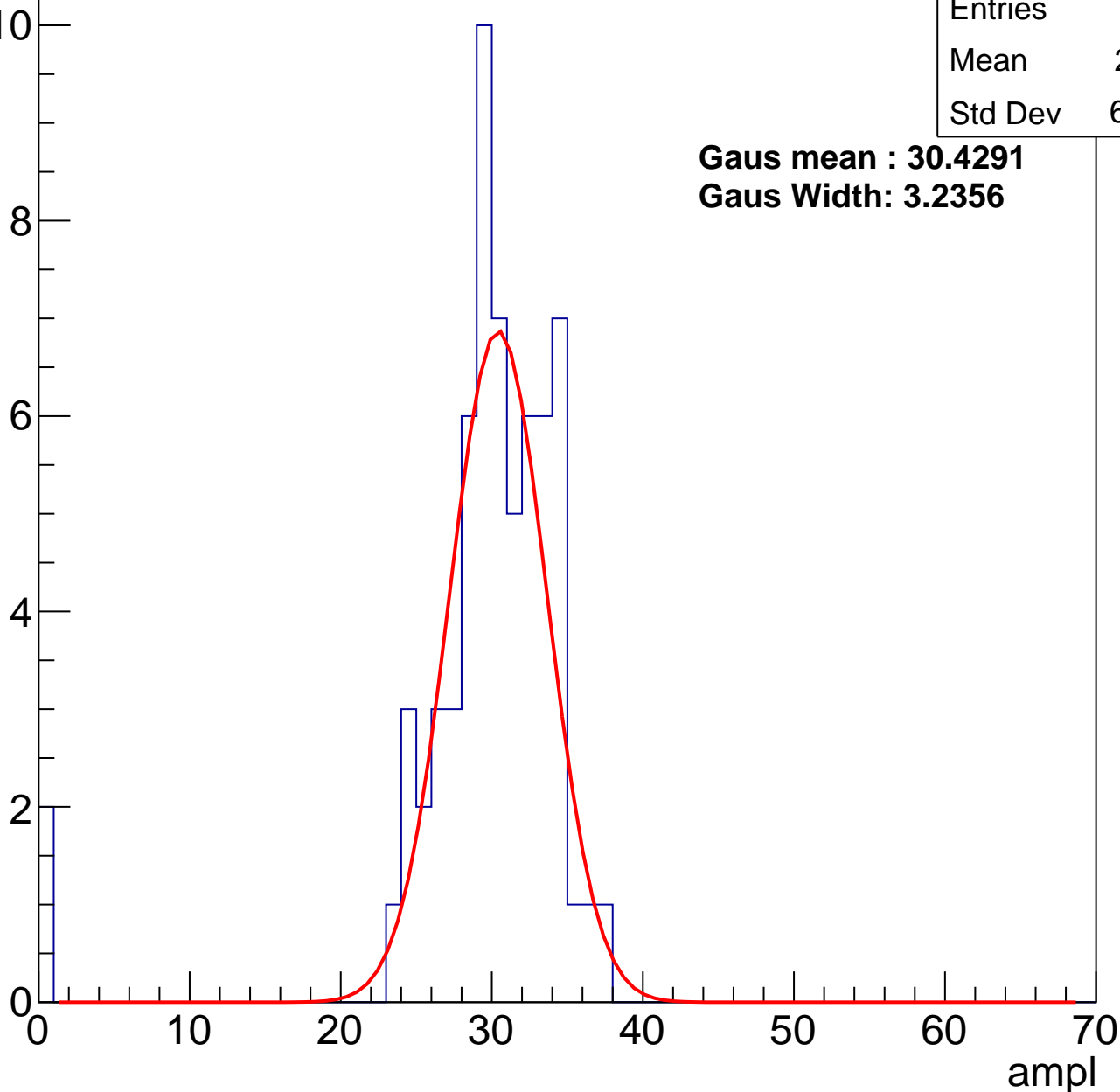
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	29.11
Std Dev	6.086

**Gaus mean : 30.4291**

**Gaus Width: 3.2356**



# B1L101S, U9-ch107, adc1

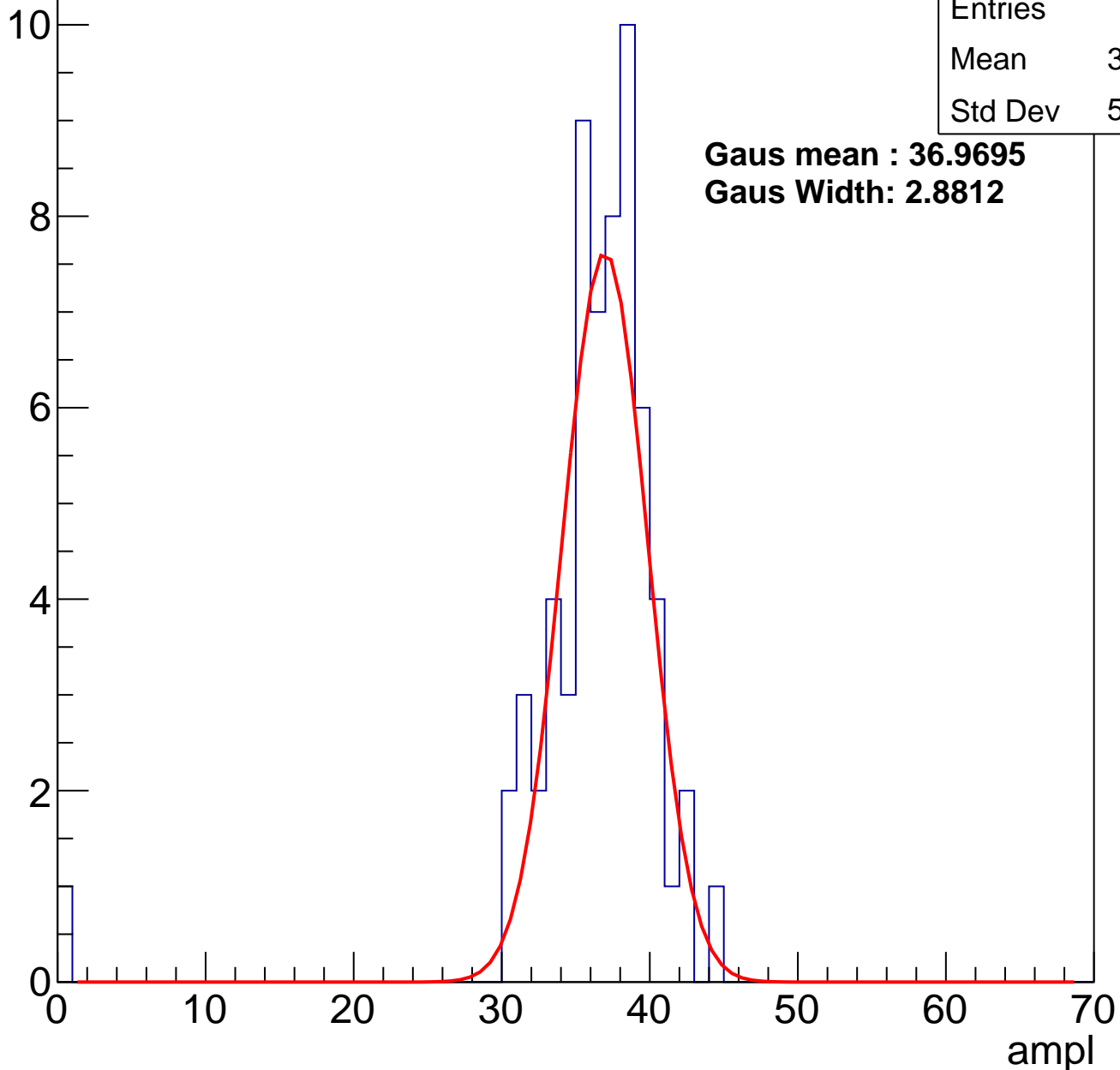
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	63
Mean	35.83
Std Dev	5.429

**Gaus mean : 36.9695**

**Gaus Width: 2.8812**

Entry



# B1L101S, U9-ch107, adc2

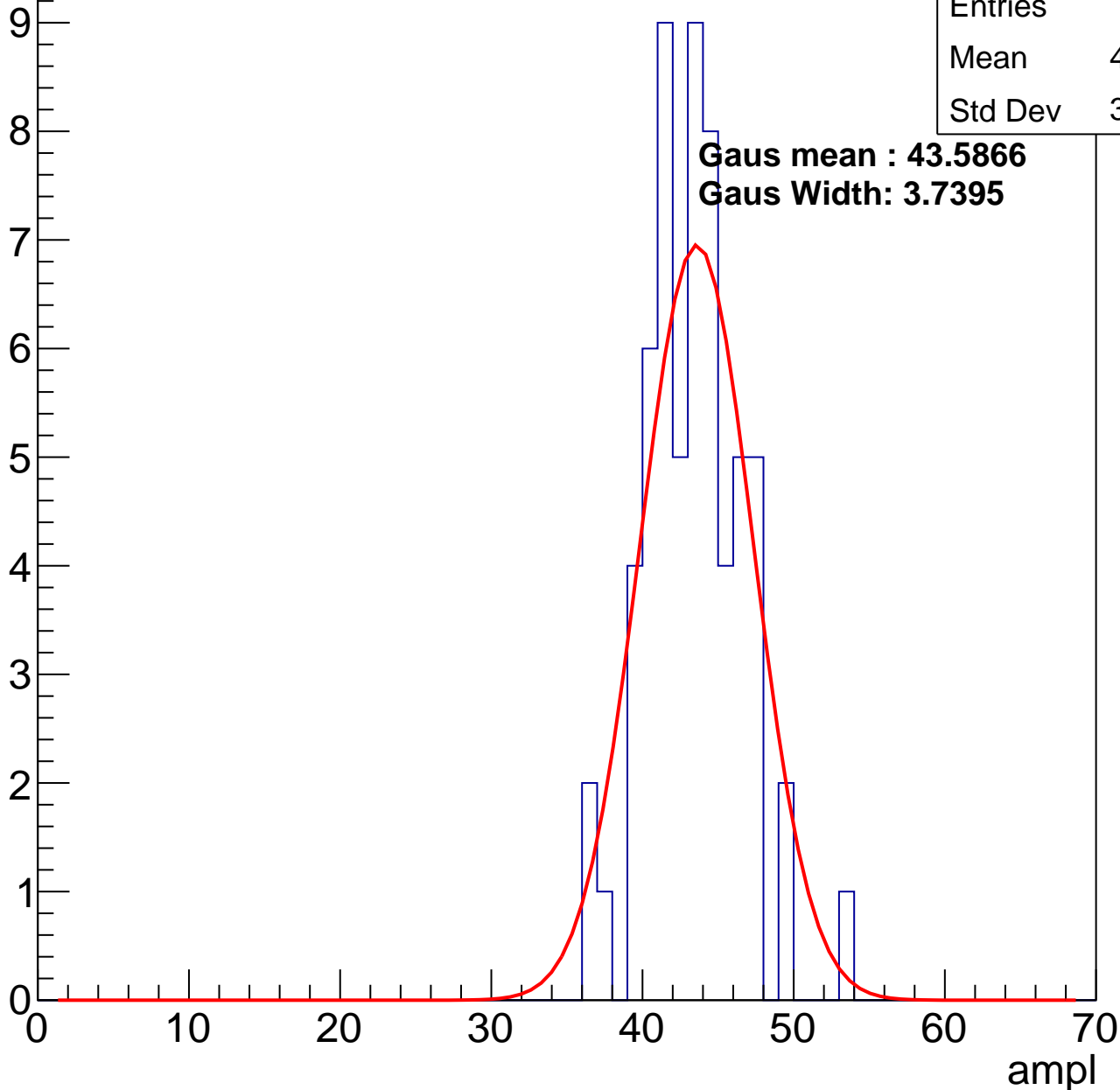
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	42.93
Std Dev	3.172

**Gaus mean : 43.5866**

**Gaus Width: 3.7395**



# B1L101S, U9-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	102
Mean	50.68
Std Dev	3.954

Entry

10

8

6

4

2

0

0

10

20

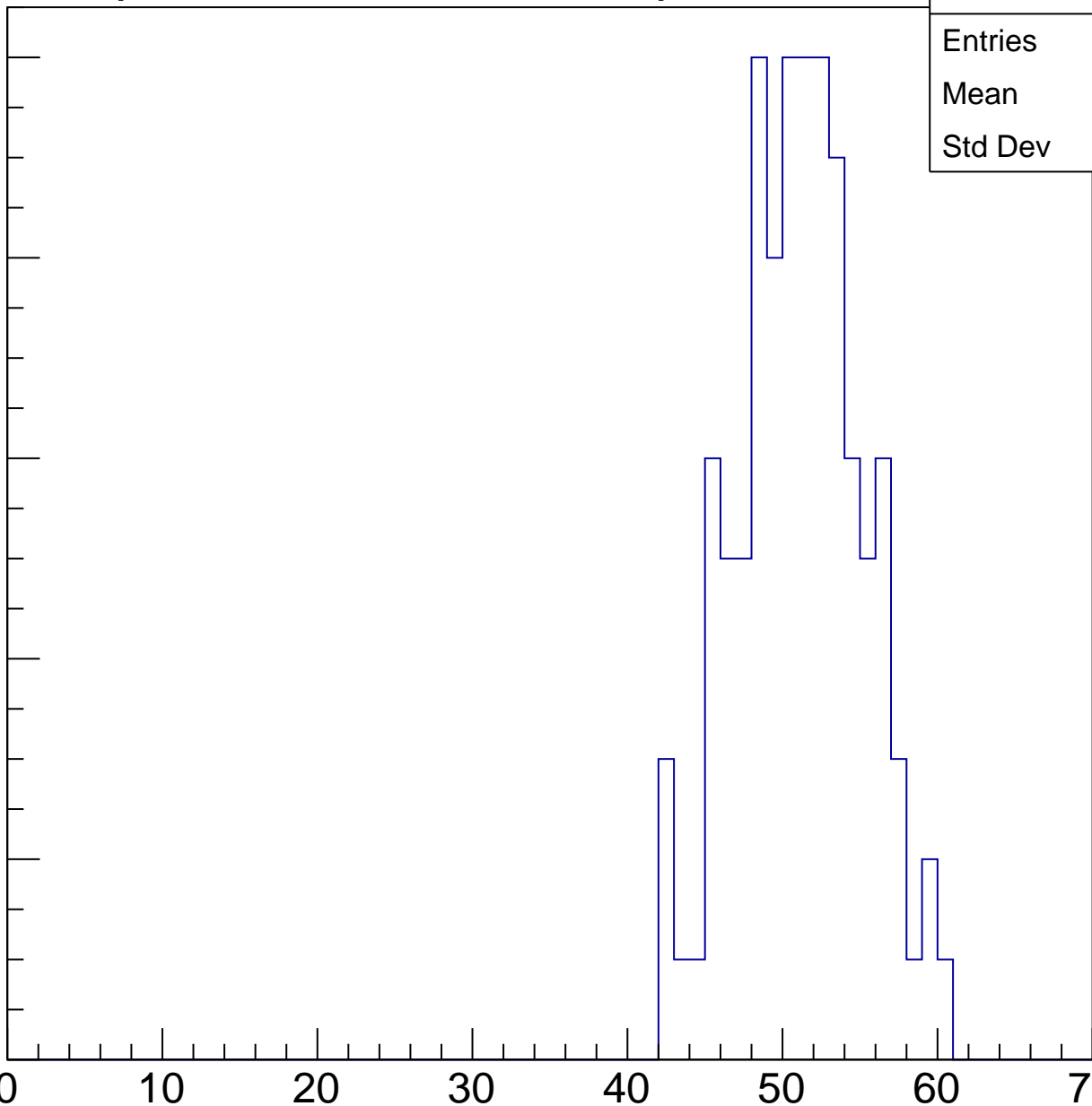
30

40

50

60

ampl



# B1L101S, U9-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

6

5

4

3

2

1

0

Entries

35

Mean

57.86

Std Dev

2.598

ampl

0

10

20

30

40

50

60

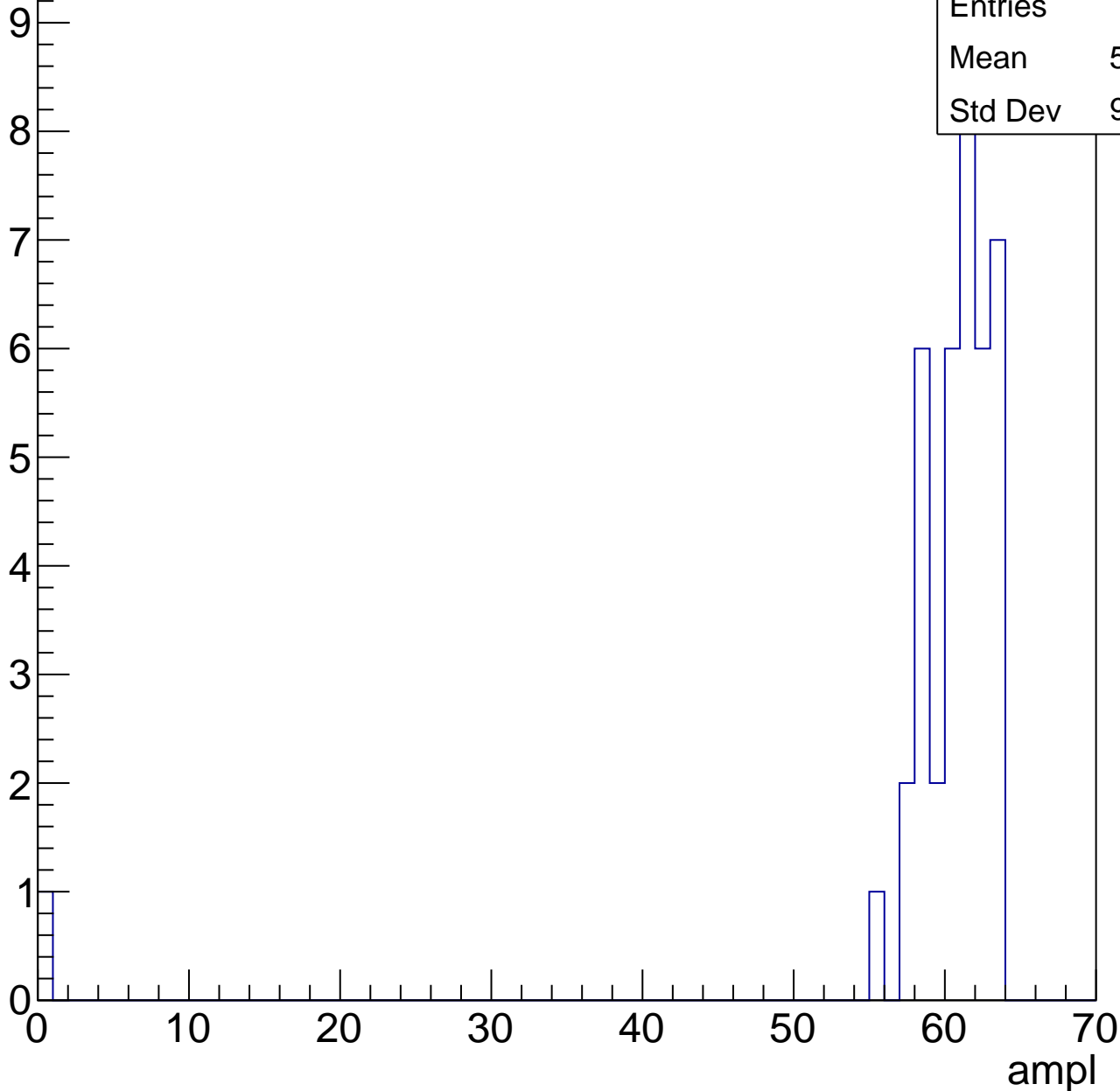
70

# B1L101S, U9-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	40
Mean	58.92
Std Dev	9.642



# B1L101S, U9-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U9-ch108, adc0

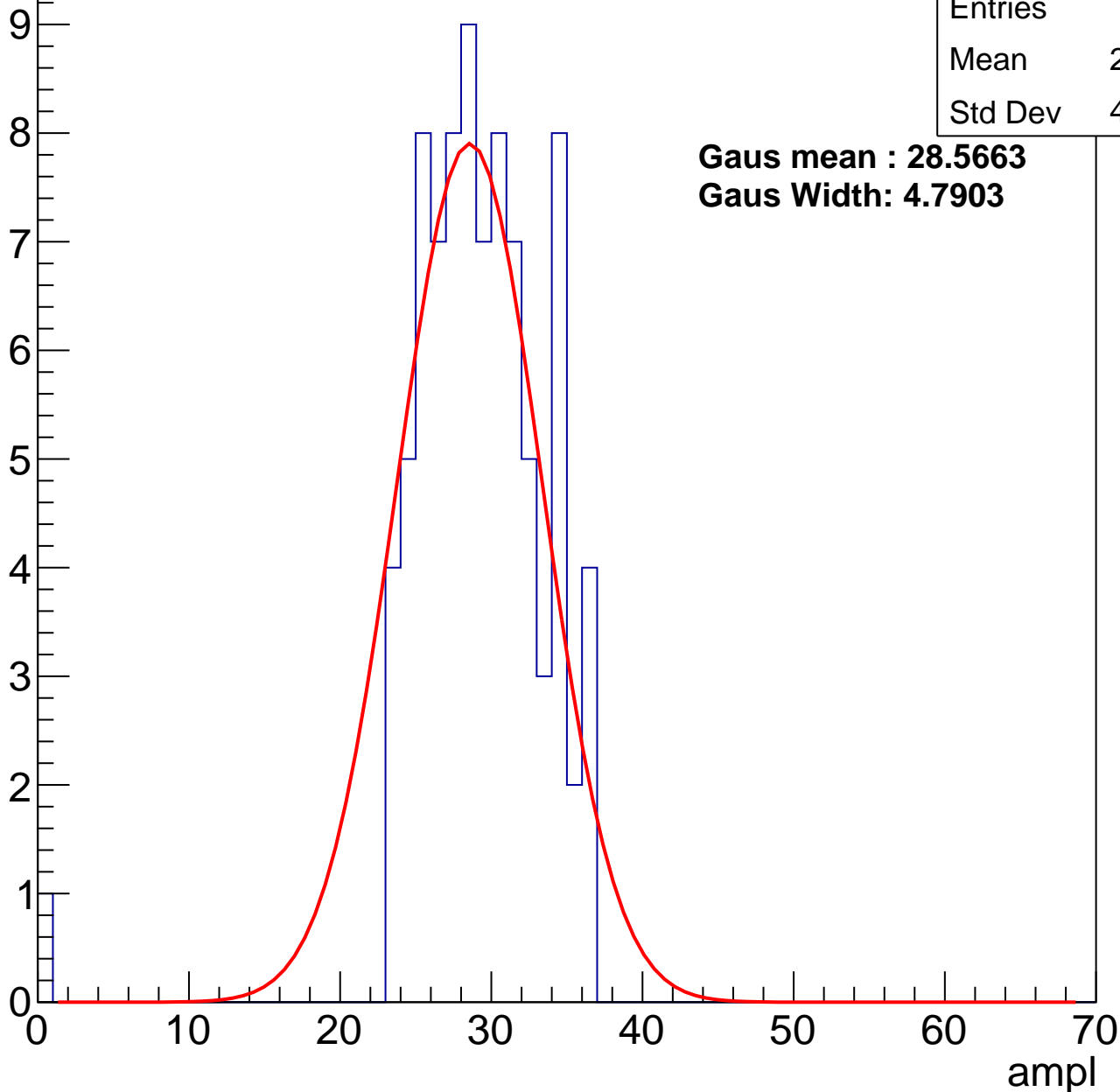
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	86
Mean	28.69
Std Dev	4.738

**Gaus mean : 28.5663**

**Gaus Width: 4.7903**



# B1L101S, U9-ch108, adc1

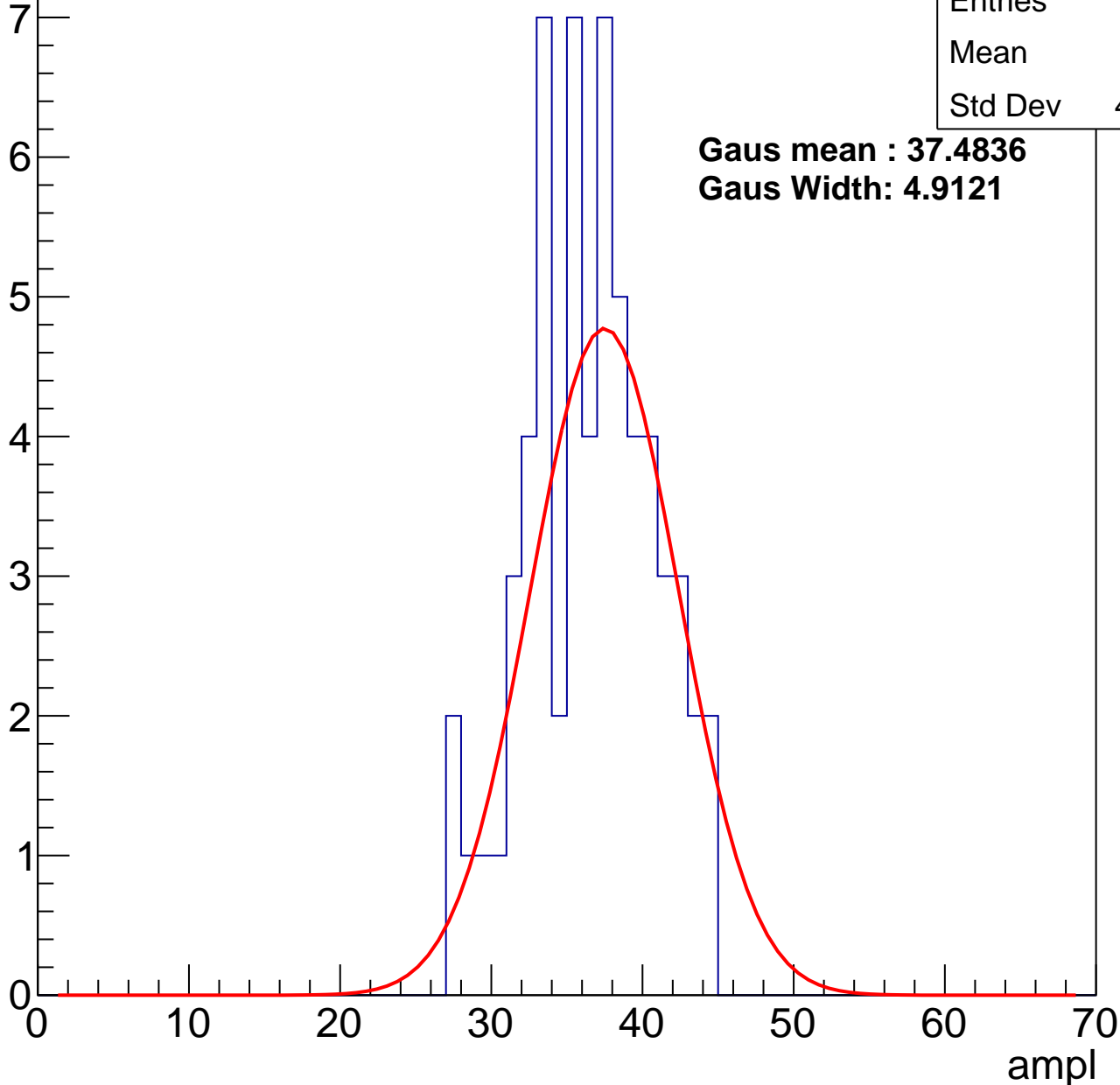
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	36.1
Std Dev	4.141

**Gaus mean : 37.4836**

**Gaus Width: 4.9121**



# B1L101S, U9-ch108, adc2

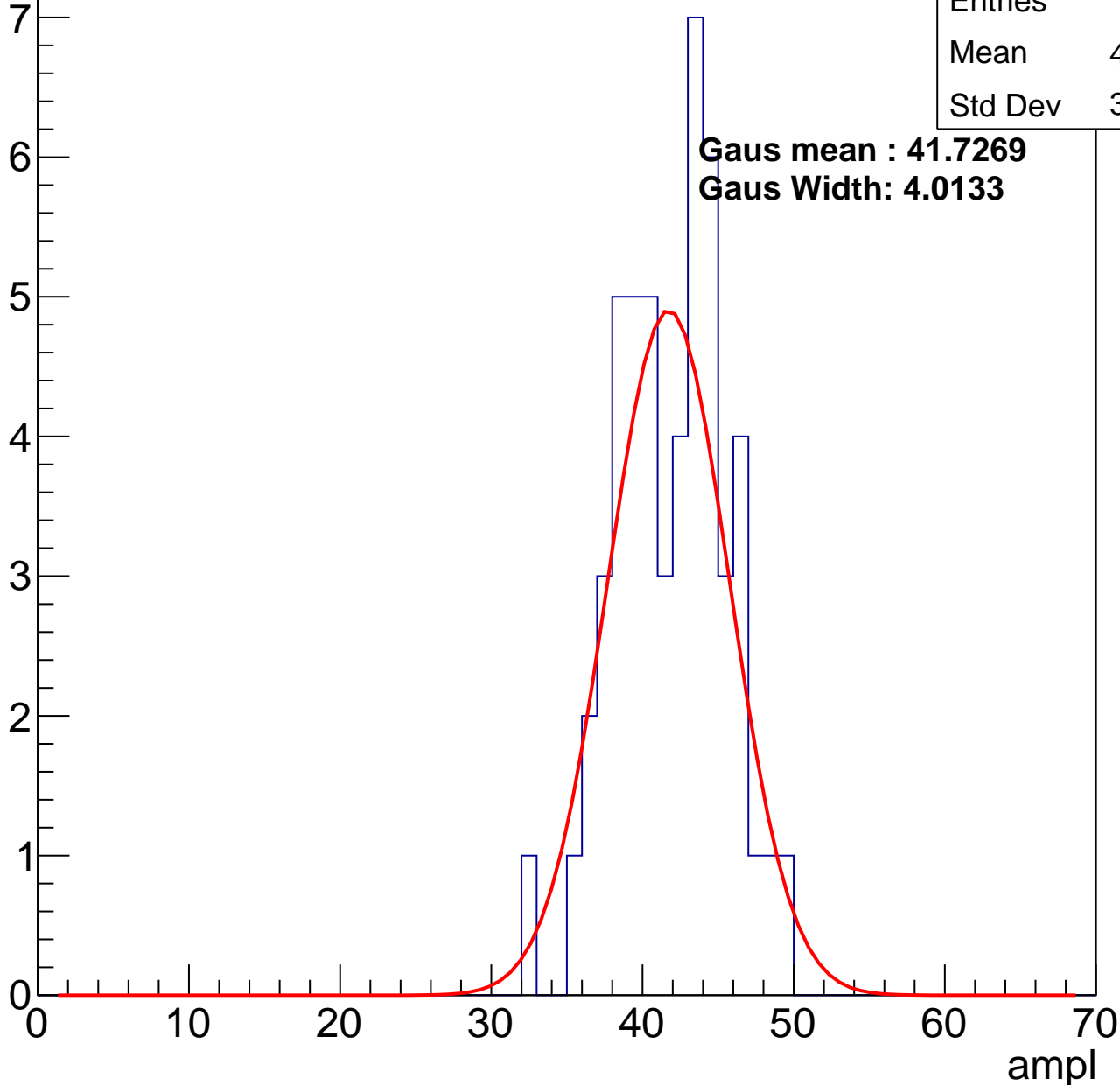
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	41.42
Std Dev	3.559

**Gaus mean : 41.7269**

**Gaus Width: 4.0133**

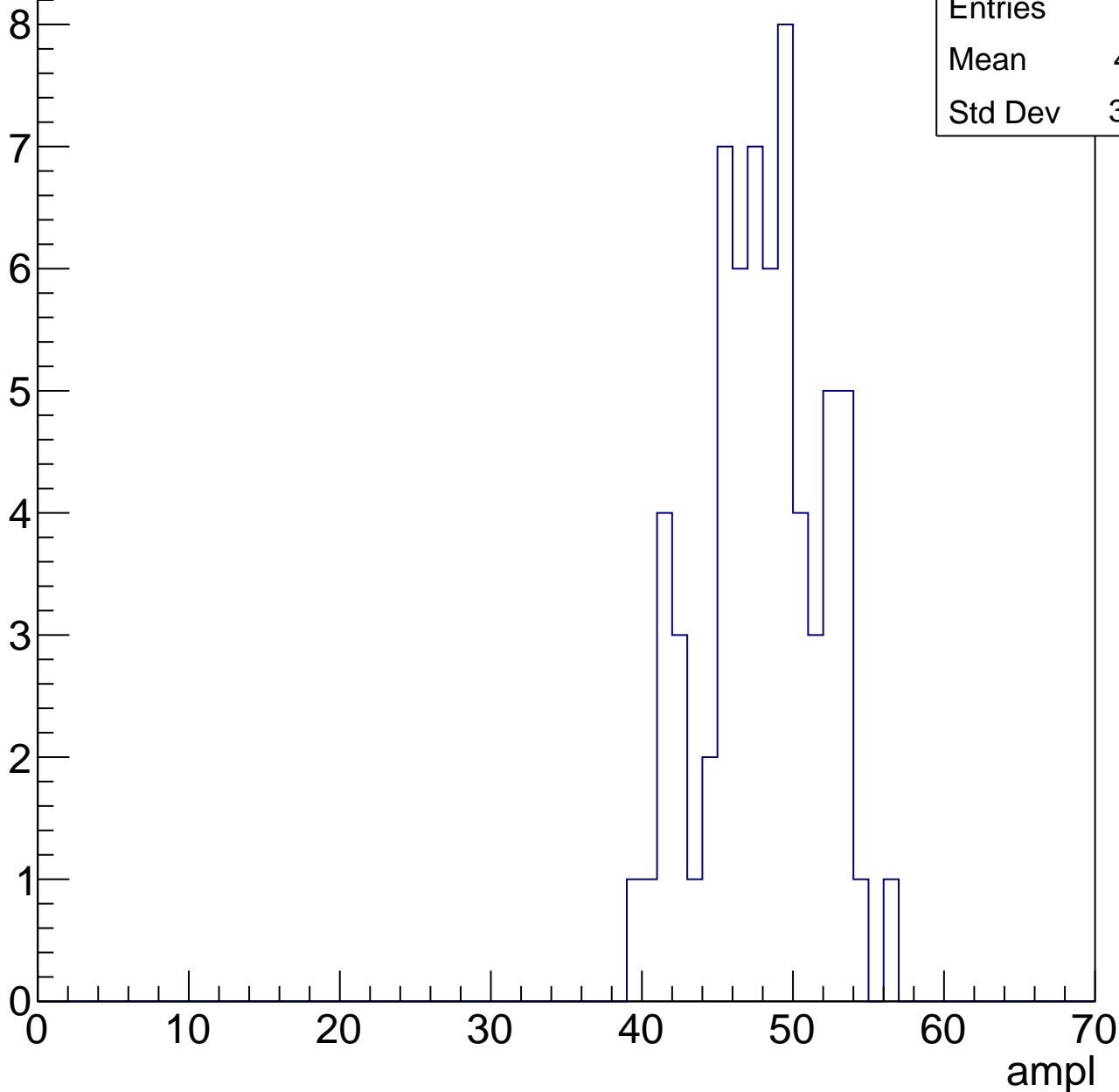


# B1L101S, U9-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

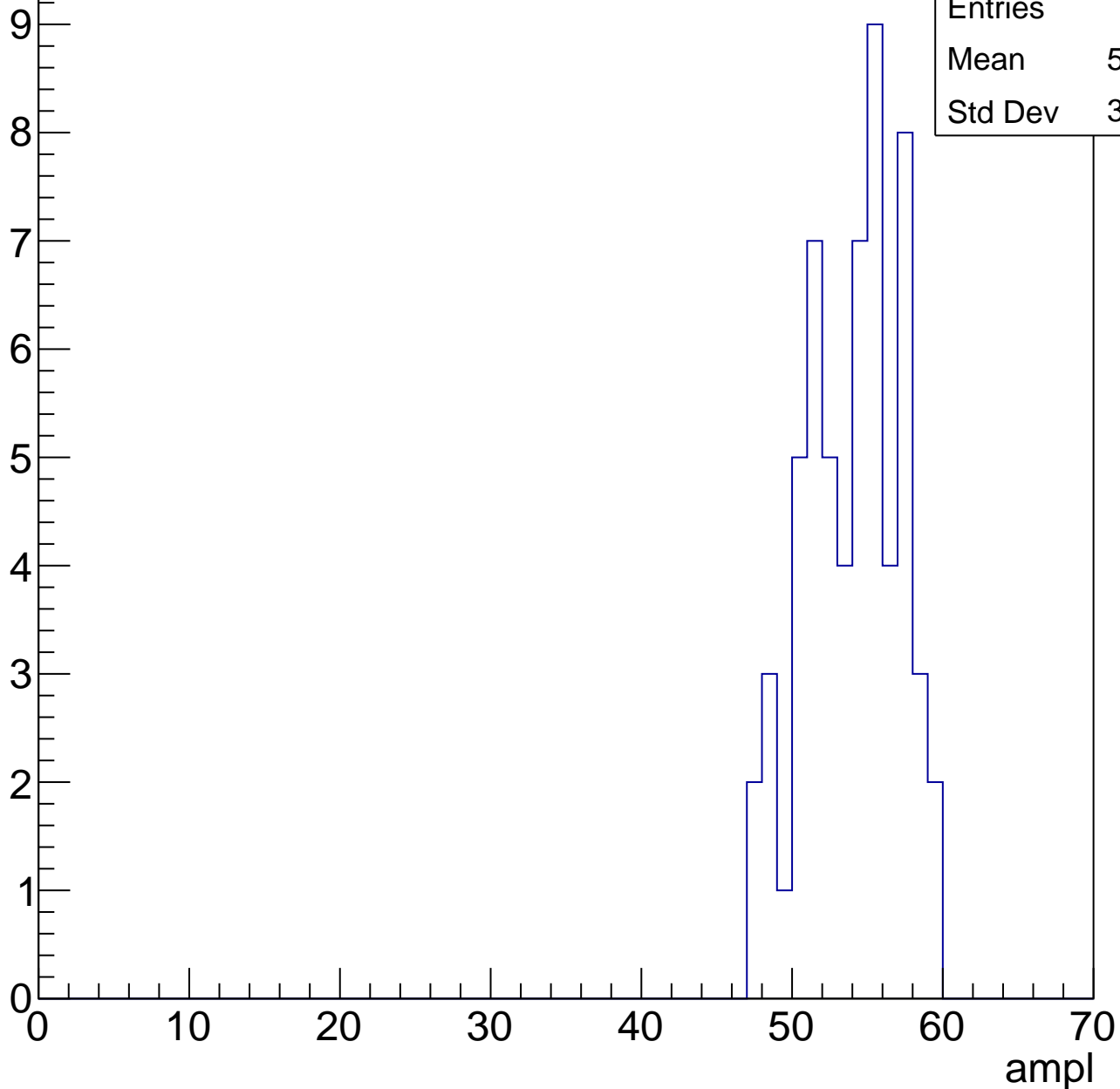
Entries	65
Mean	47.51
Std Dev	3.803



# B1L101S, U9-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

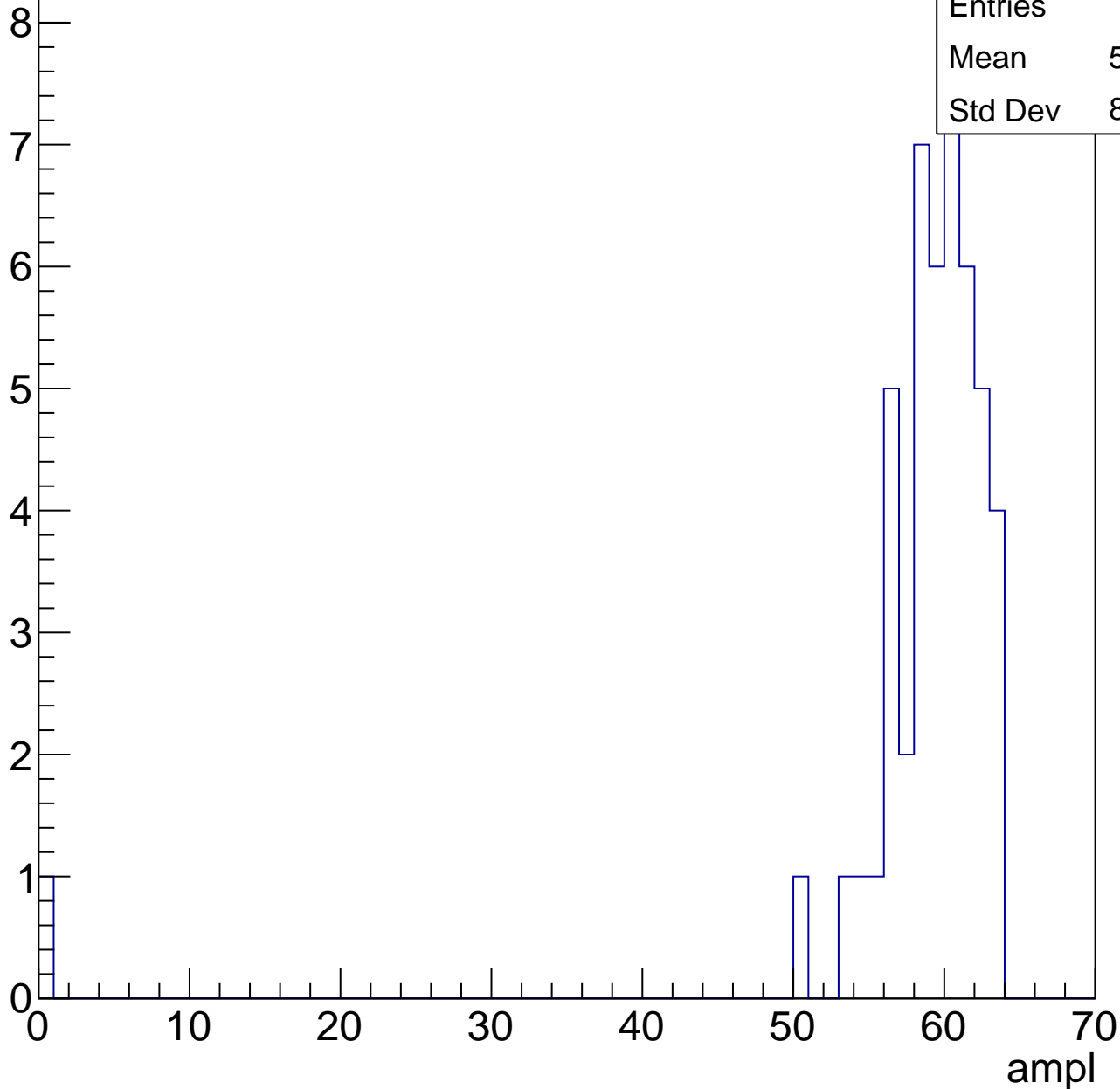


# B1L101S, U9-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	57.79
Std Dev	8.862

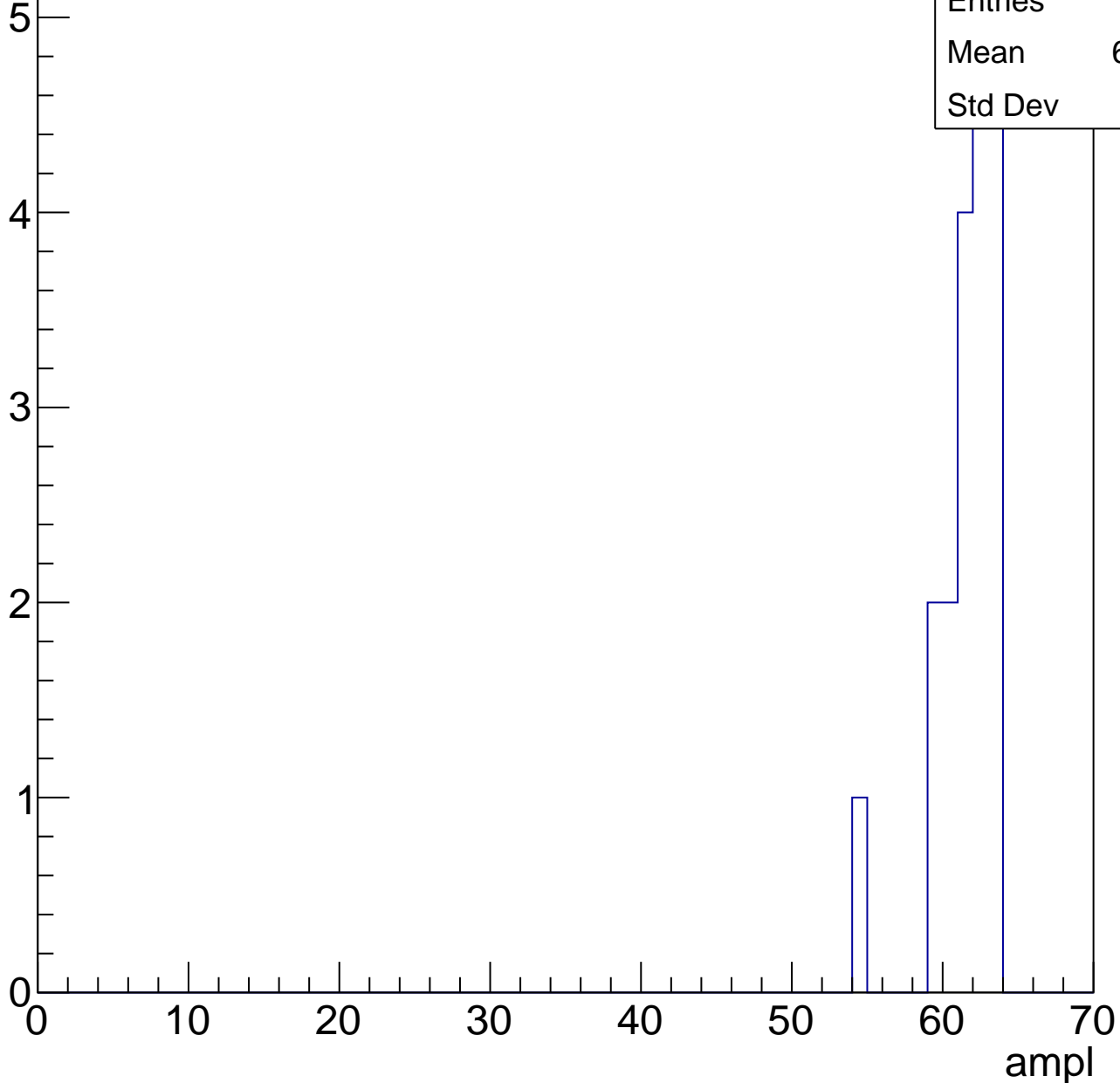


# B1L101S, U9-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	19
Mean	61.11
Std Dev	2.1

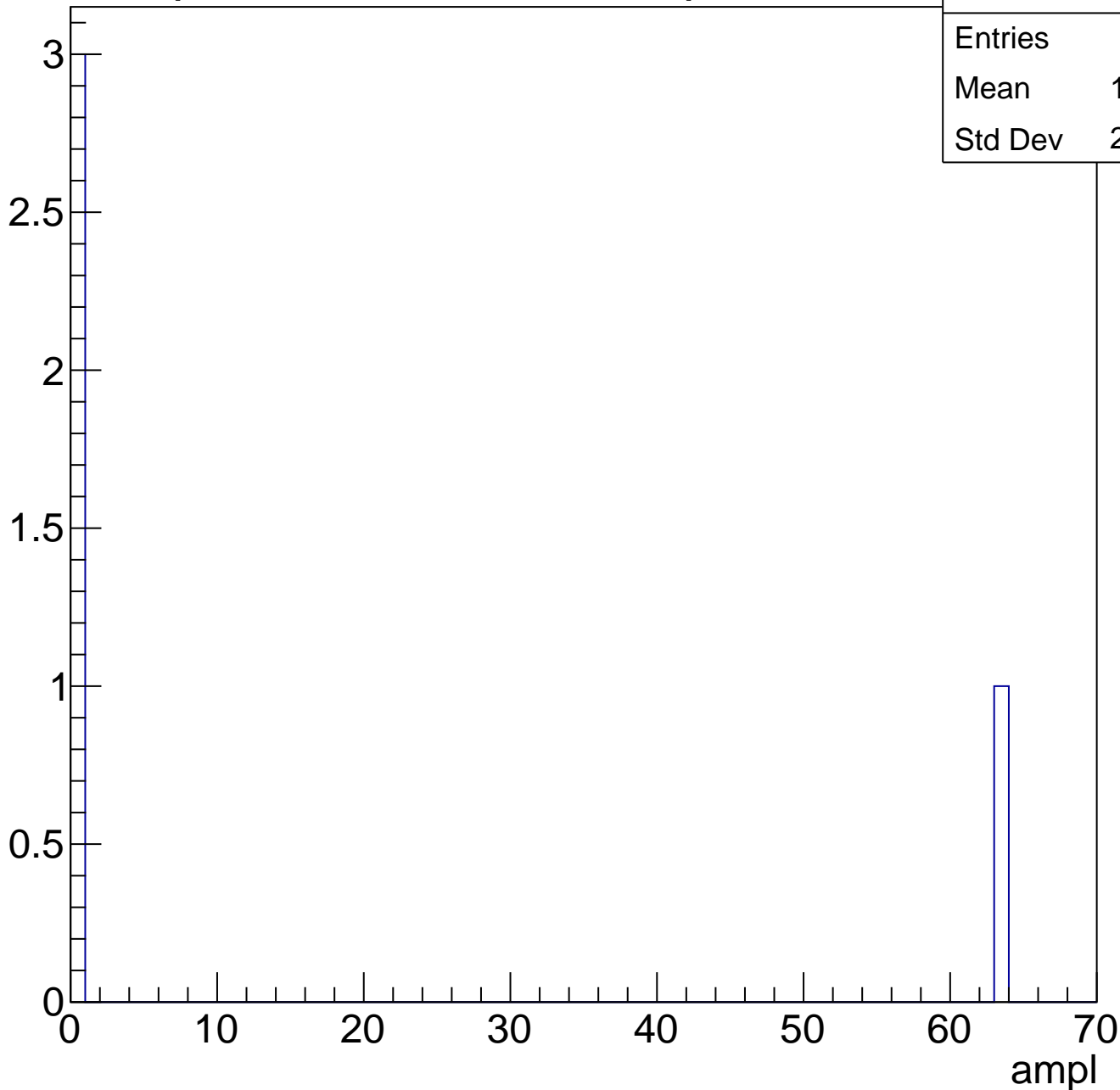




# B1L101S, U9-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	4
Mean	15.75
Std Dev	27.28

# B1L101S, U9-ch109, adc0

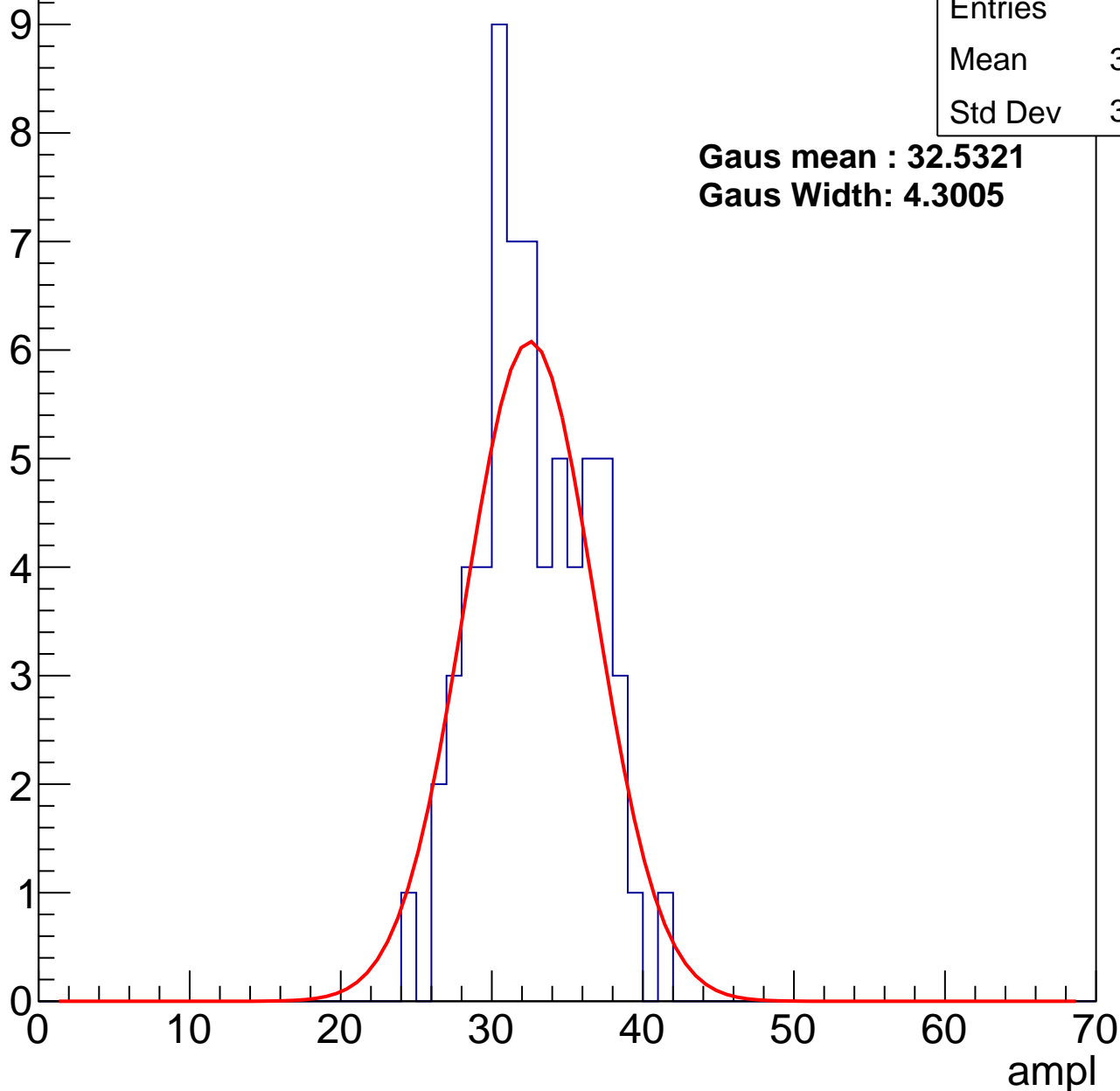
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	32.26
Std Dev	3.622

**Gaus mean : 32.5321**

**Gaus Width: 4.3005**



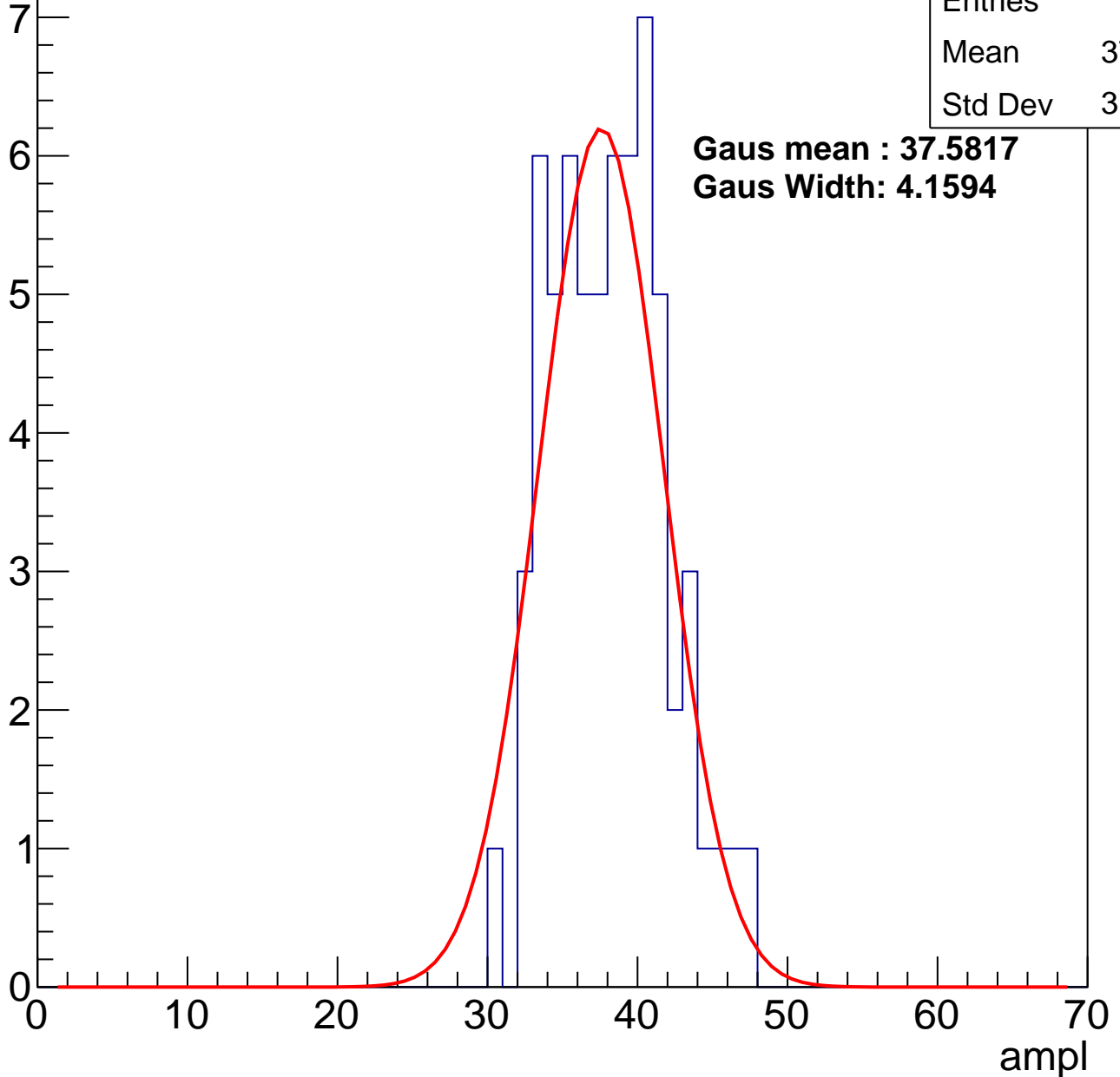
# B1L101S, U9-ch109, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	37.67
Std Dev	3.729

**Gaus mean : 37.5817**  
**Gaus Width: 4.1594**



# B1L101S, U9-ch109, adc2

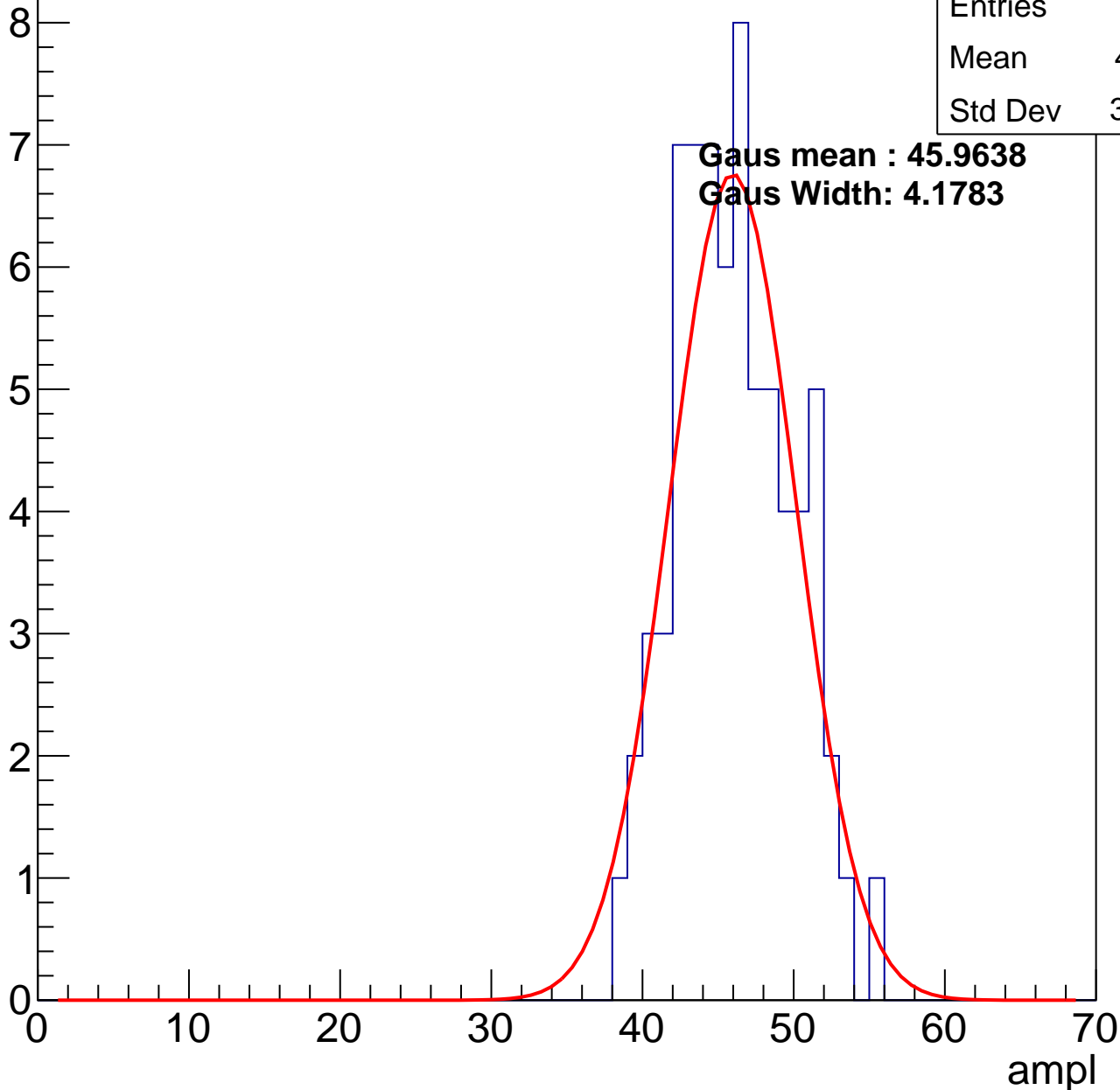
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	45.61
Std Dev	3.743

**Gaus mean : 45.9638**

**Gaus Width: 4.1783**

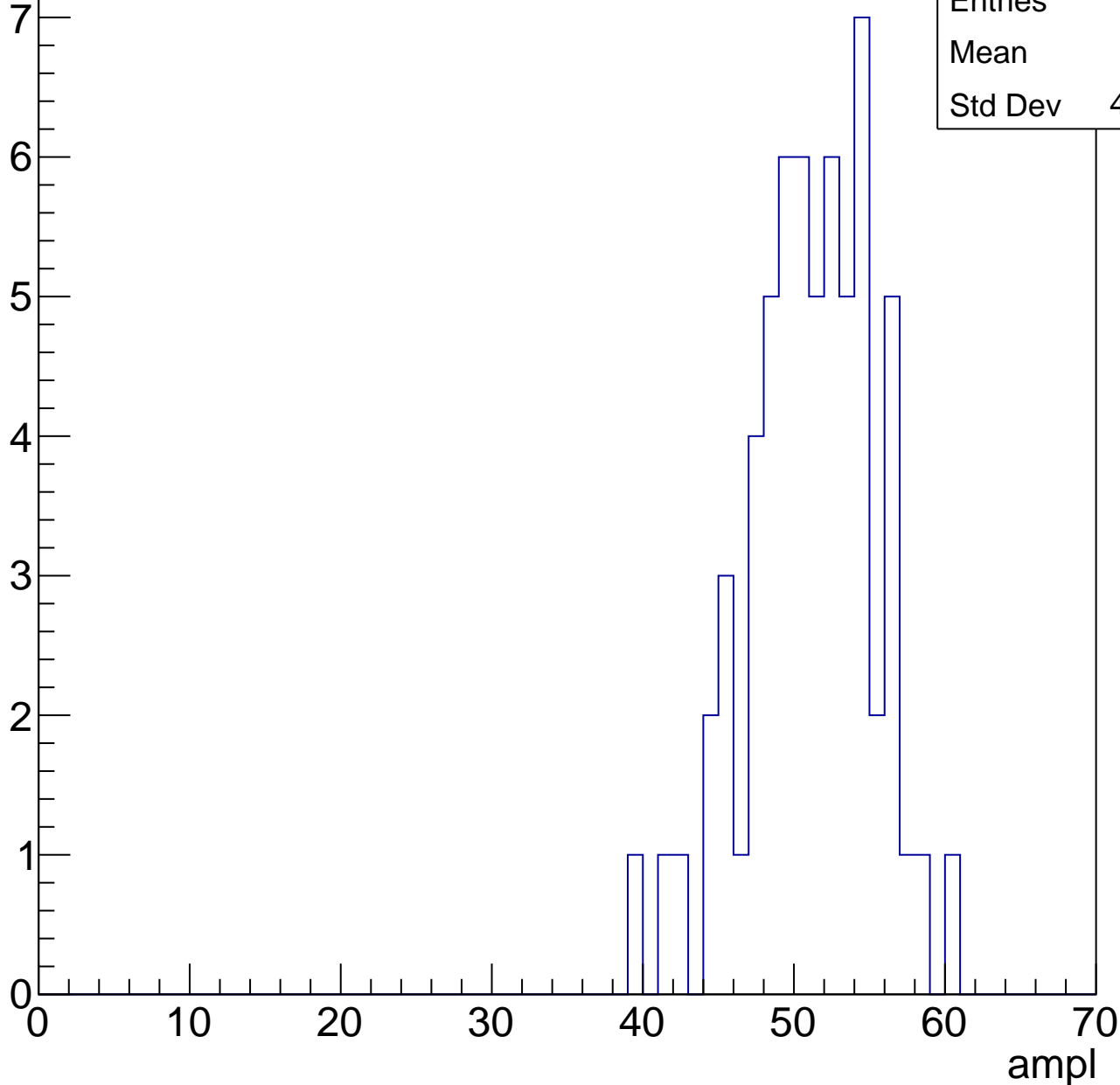


# B1L101S, U9-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	50.6
Std Dev	4.173

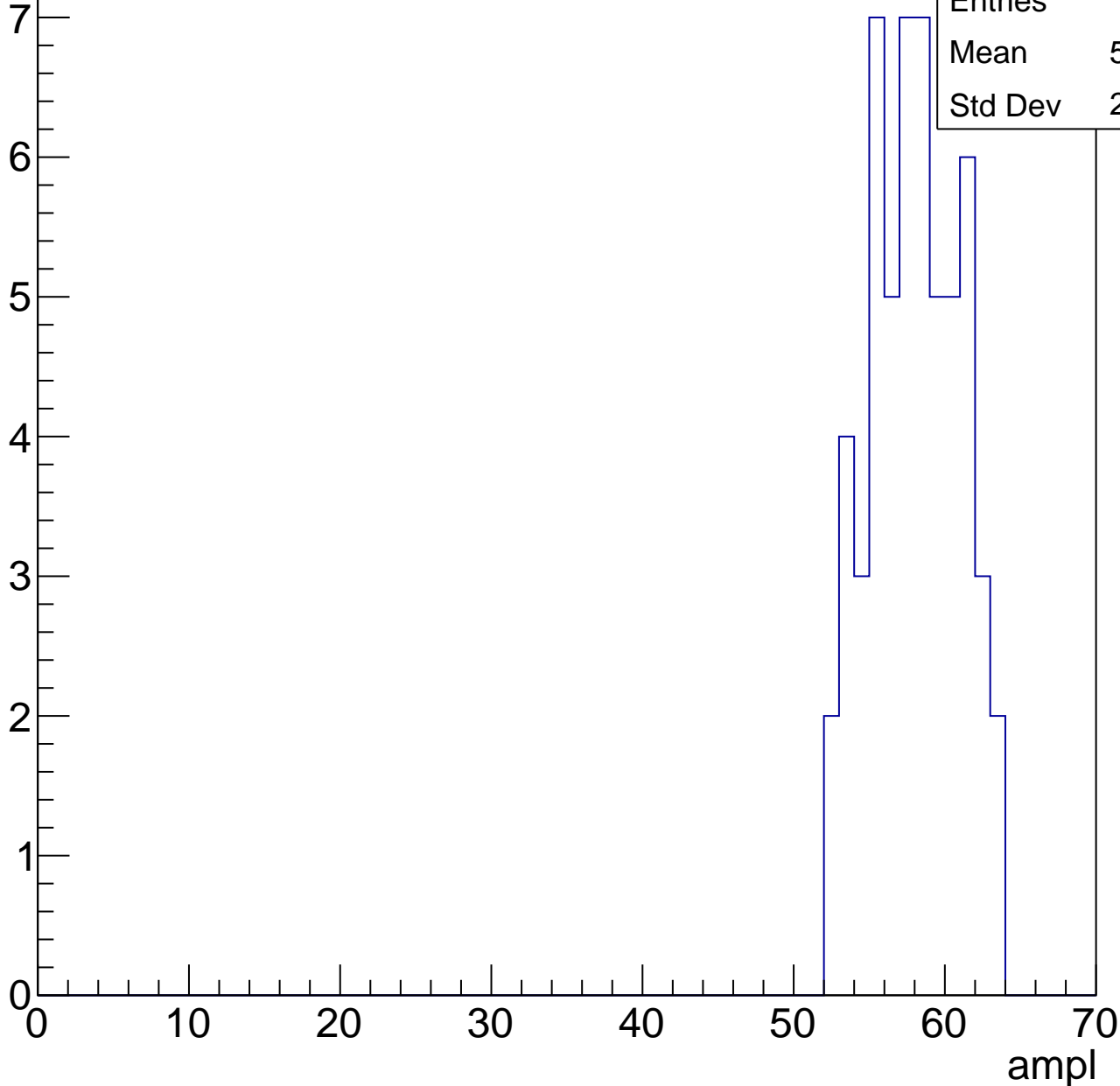


# B1L101S, U9-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	57.52
Std Dev	2.909

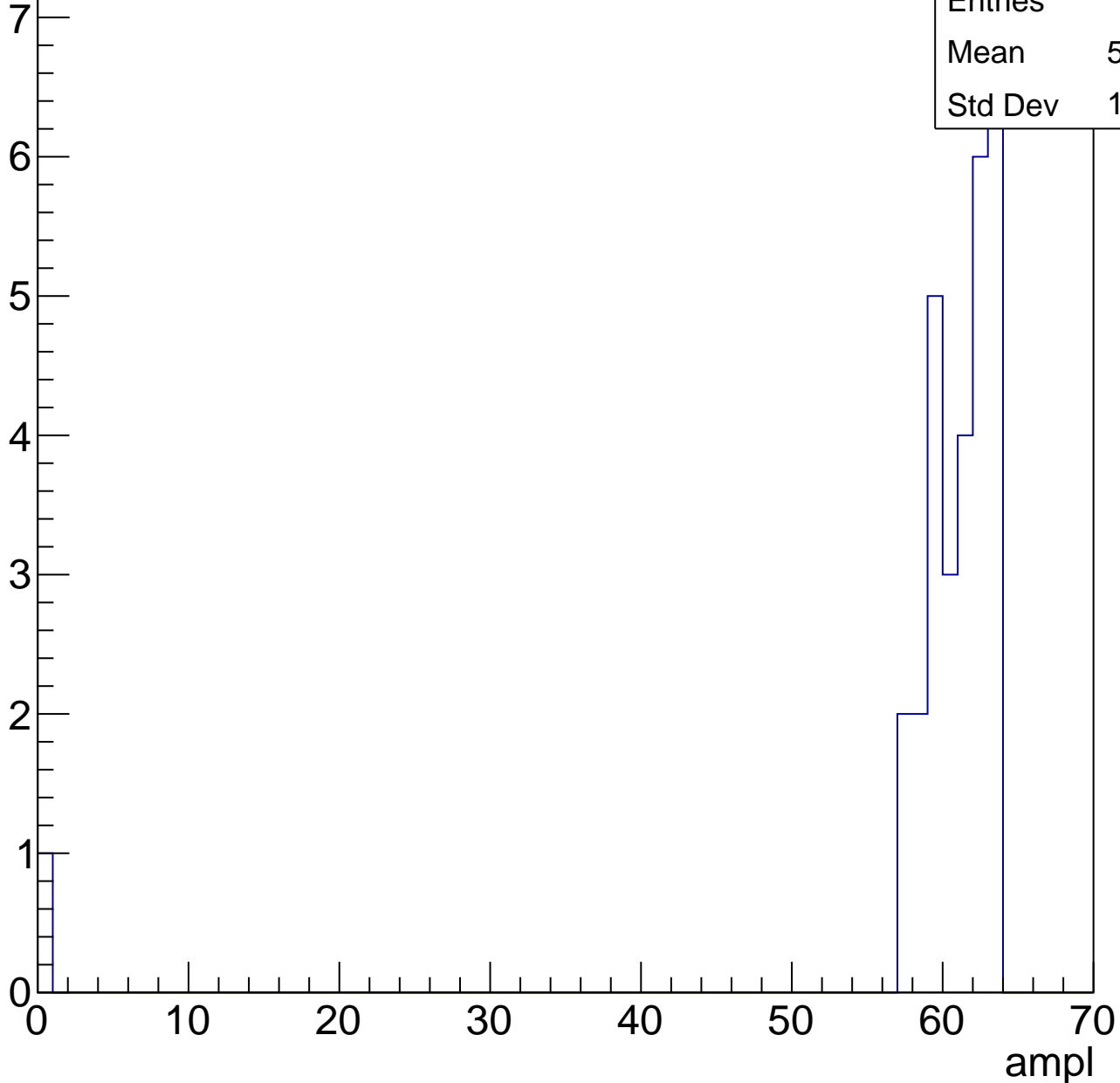


# B1L101S, U9-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	30
Mean	58.73
Std Dev	11.07



# B1L101S, U9-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U9-ch110, adc0

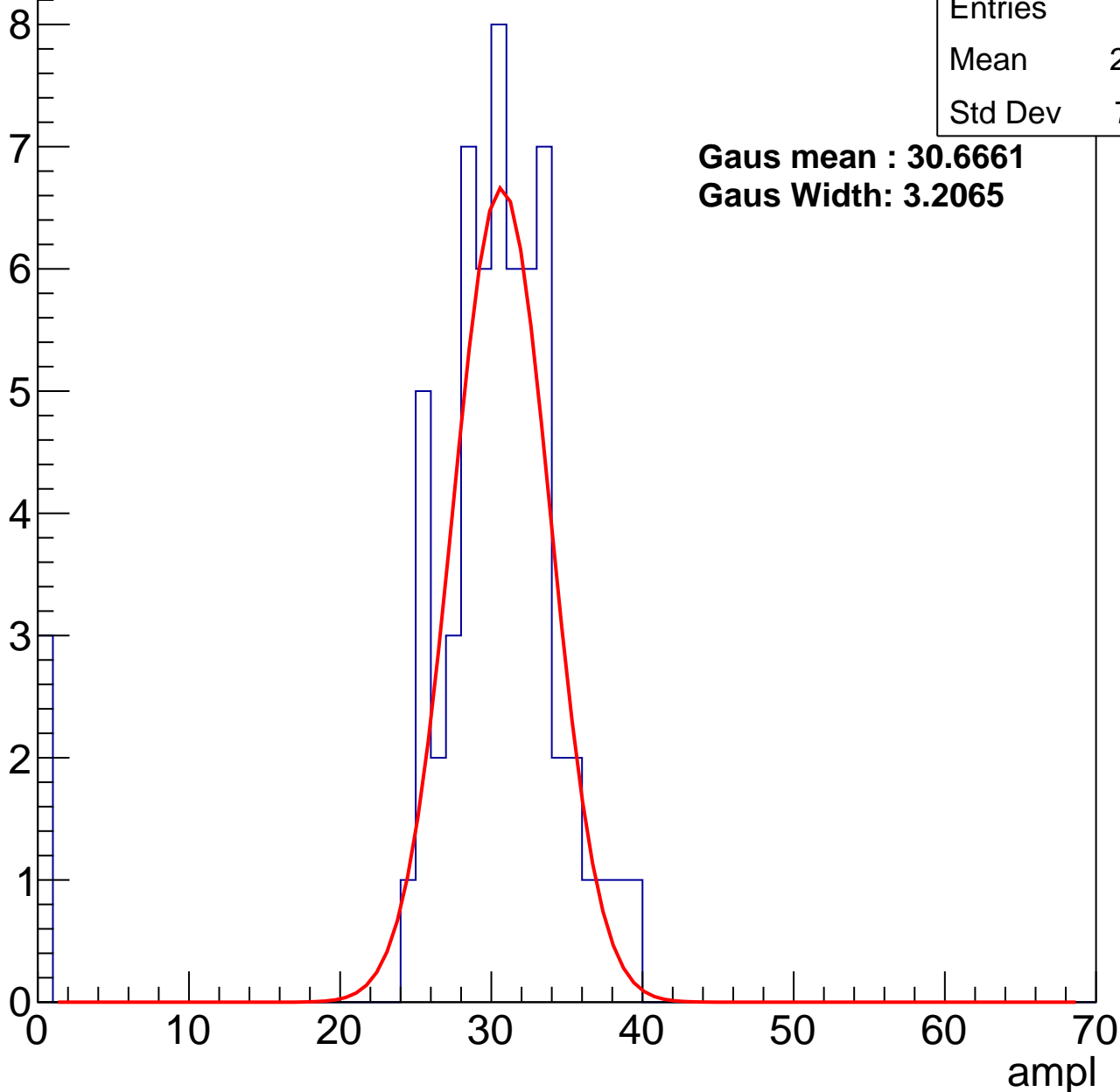
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	28.85
Std Dev	7.271

**Gaus mean : 30.6661**

**Gaus Width: 3.2065**



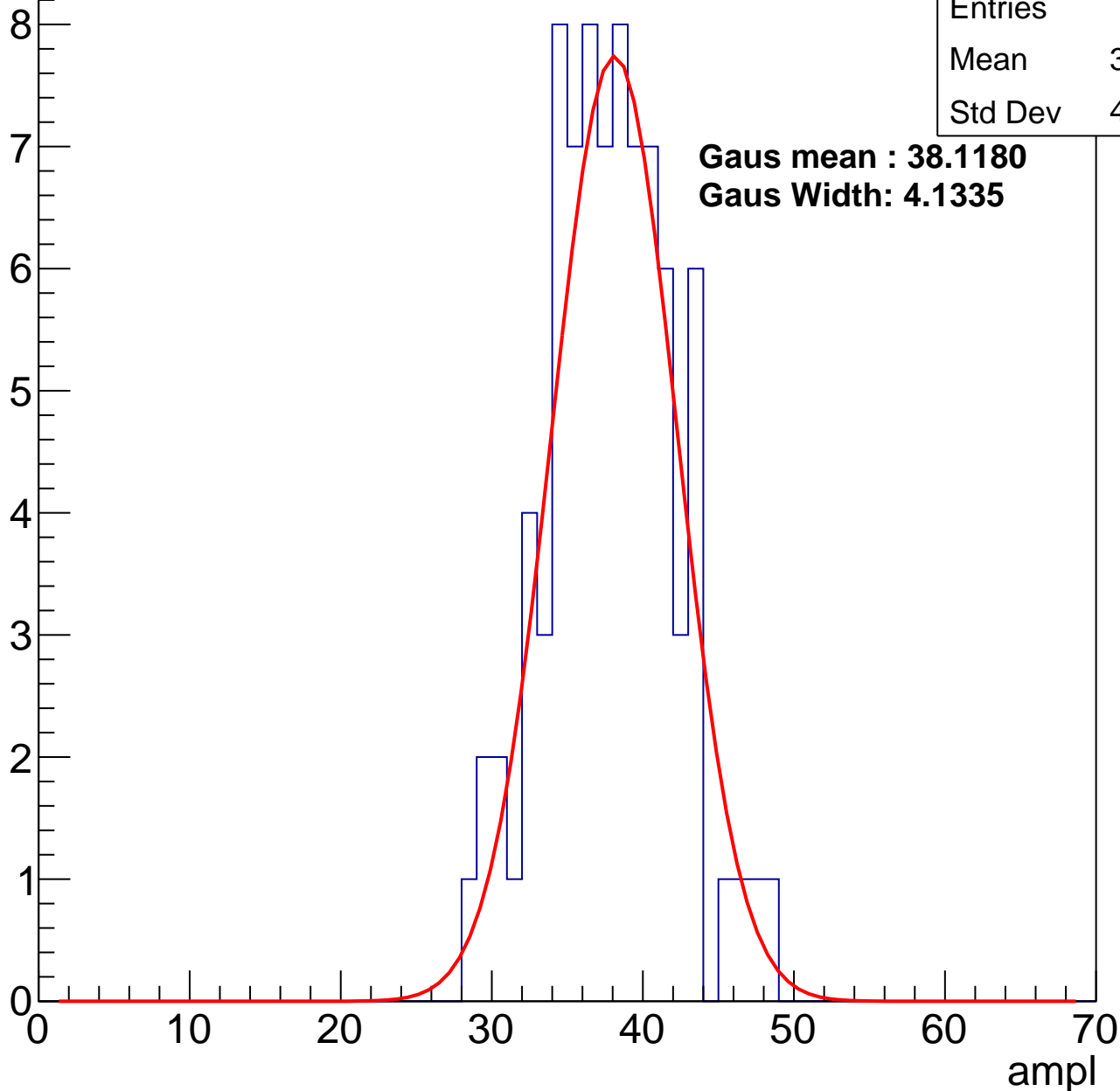
# B1L101S, U9-ch110, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	84
Mean	37.39
Std Dev	4.138

**Gaus mean : 38.1180**  
**Gaus Width: 4.1335**



# B1L101S, U9-ch110, adc2

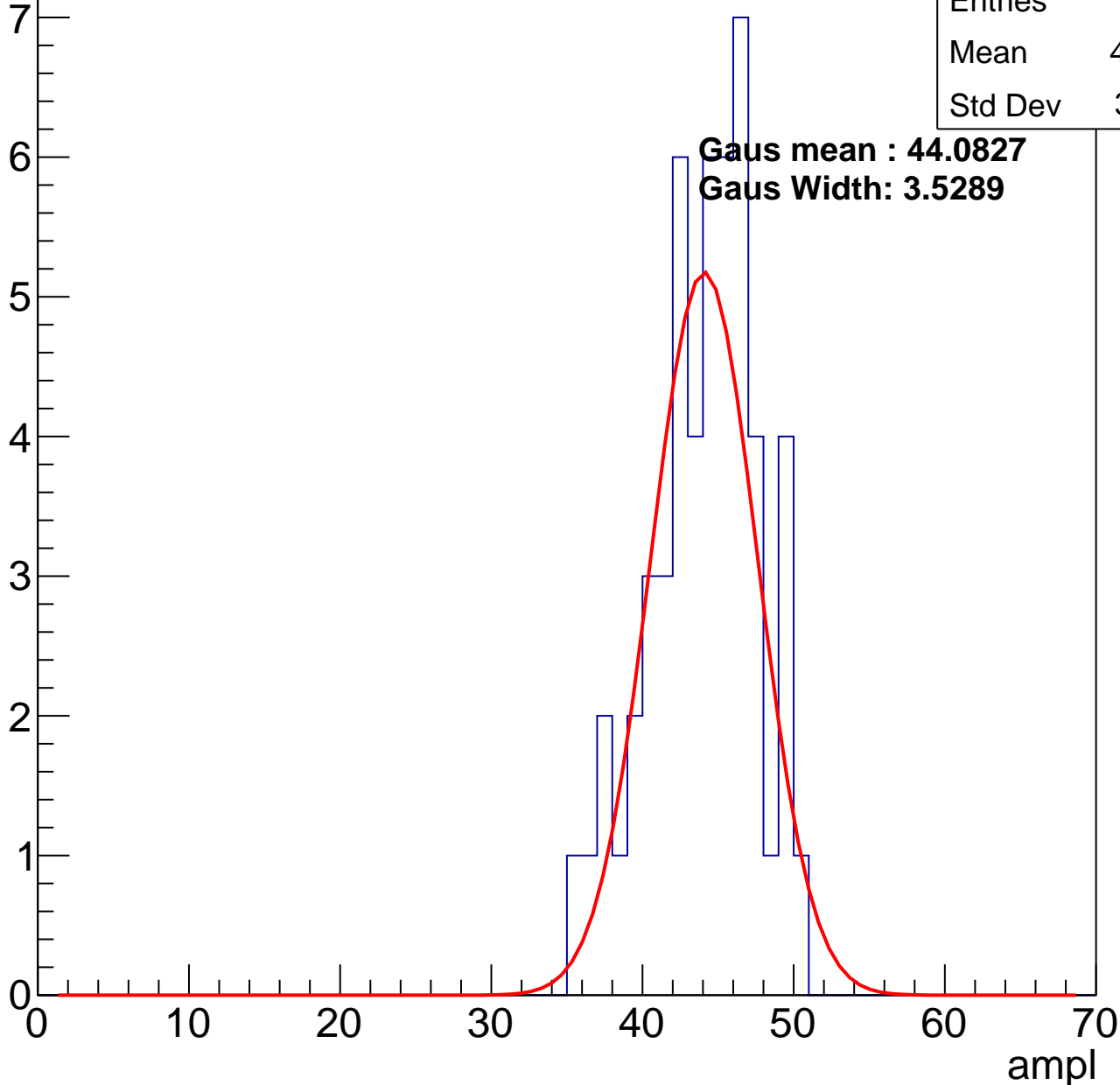
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	43.58
Std Dev	3.521

**Gaus mean : 44.0827**

**Gaus Width: 3.5289**



# B1L101S, U9-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

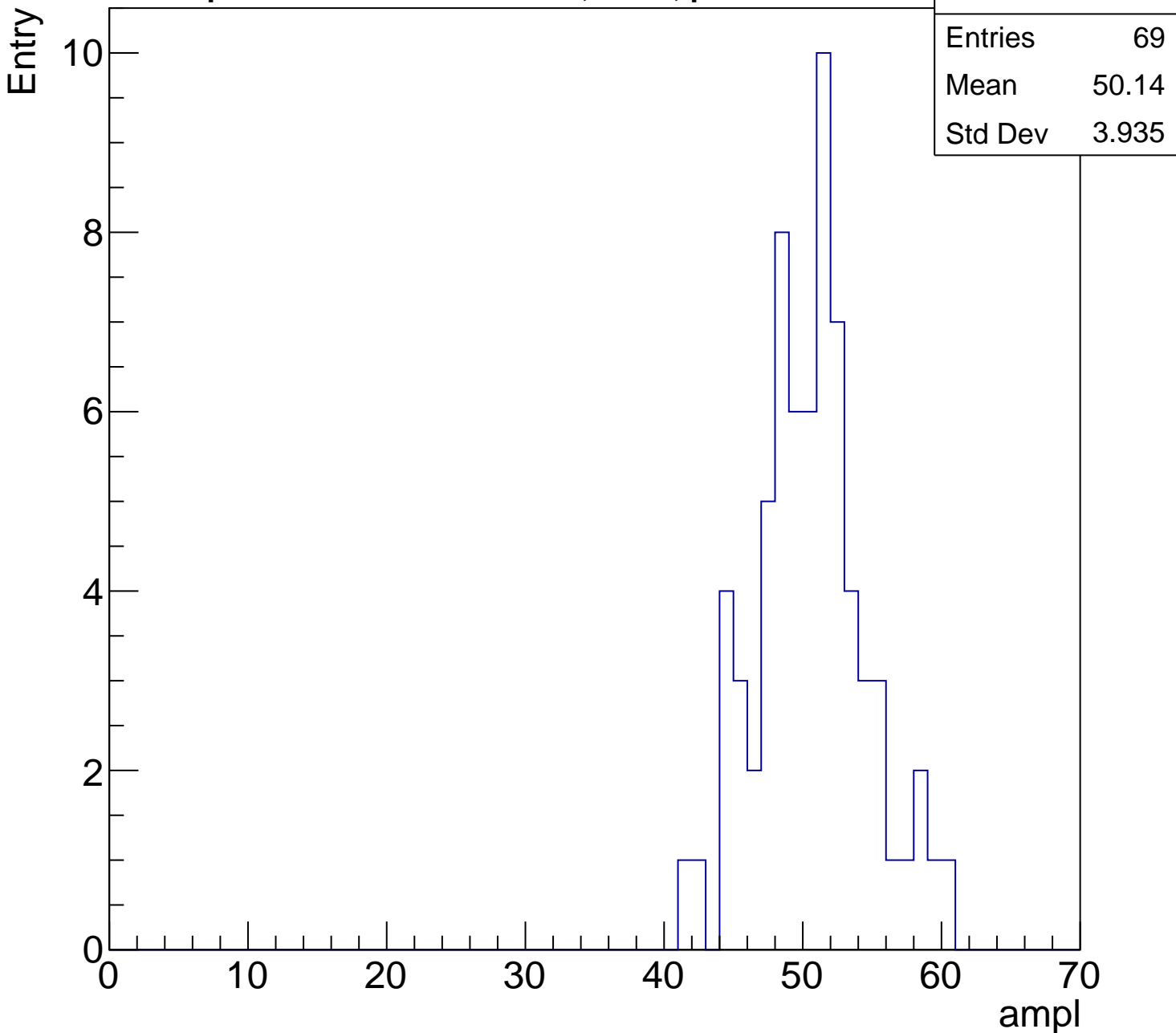
Entries	69
Mean	50.14
Std Dev	3.935

Entry

10  
8  
6  
4  
2  
0

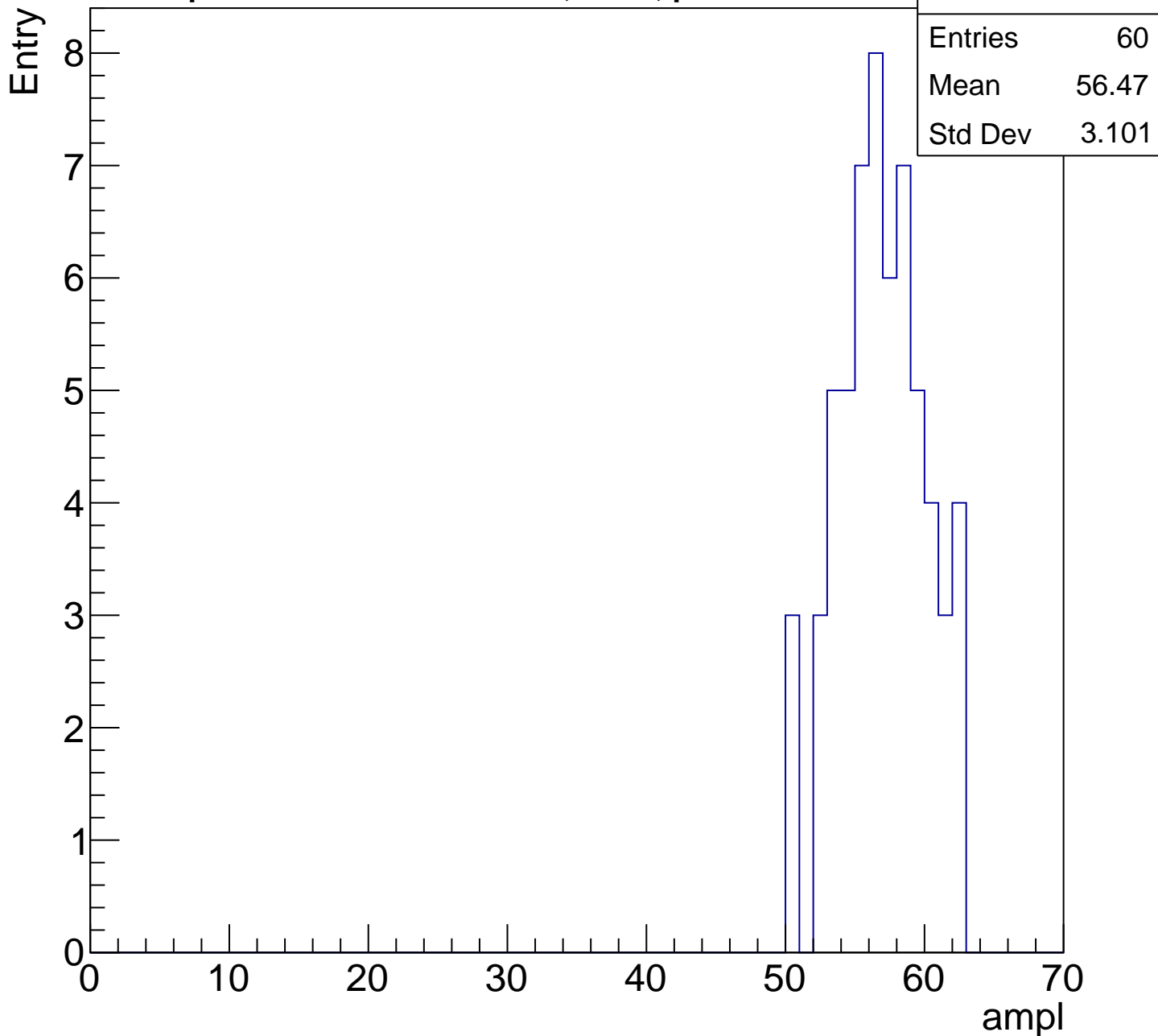
0 10 20 30 40 50 60 70

ampl



# B1L101S, U9-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

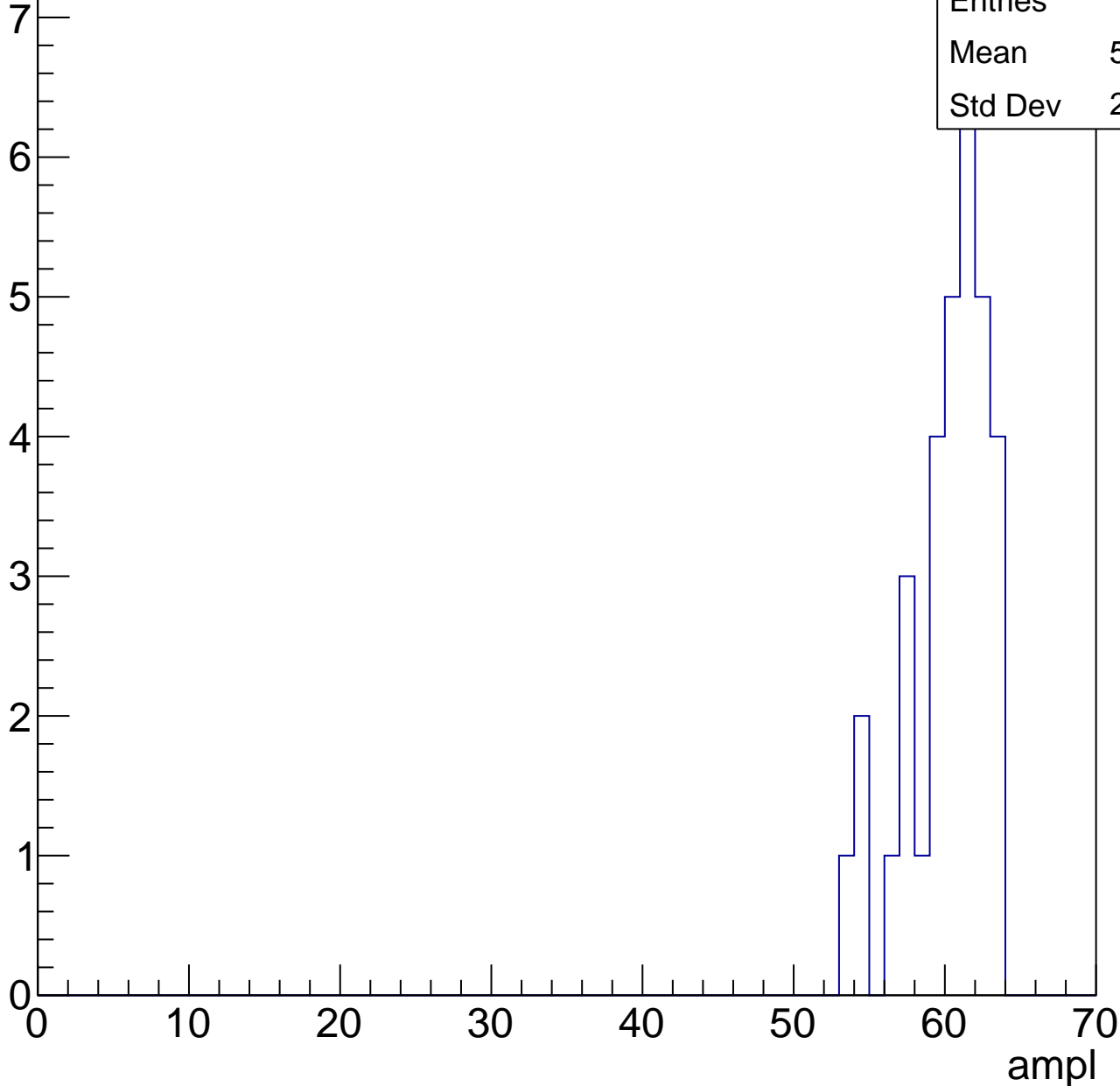


# B1L101S, U9-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	33
Mean	59.73
Std Dev	2.655

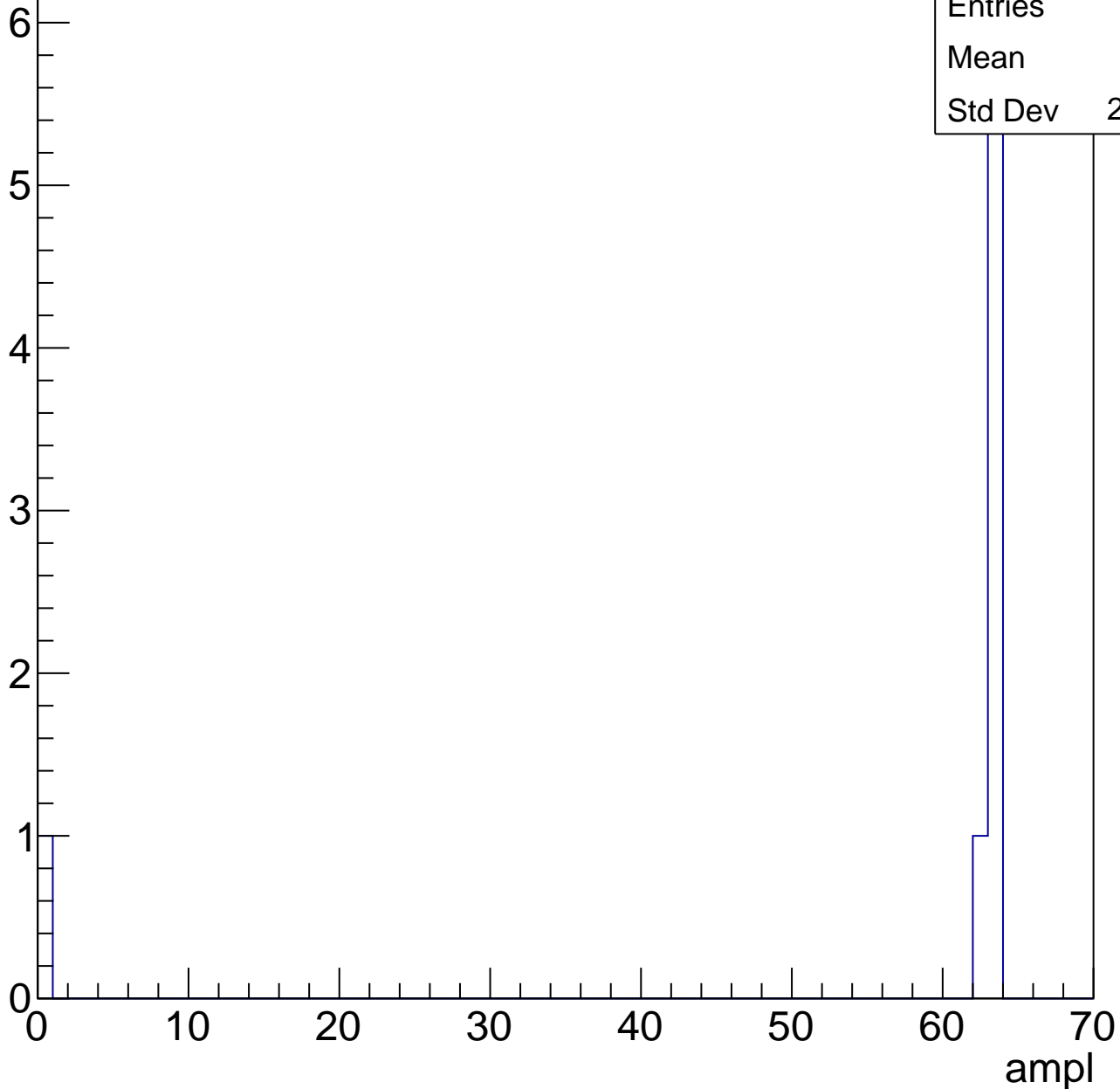


# B1L101S, U9-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	8
Mean	55
Std Dev	20.79





# B1L101S, U9-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U9-ch111, adc0

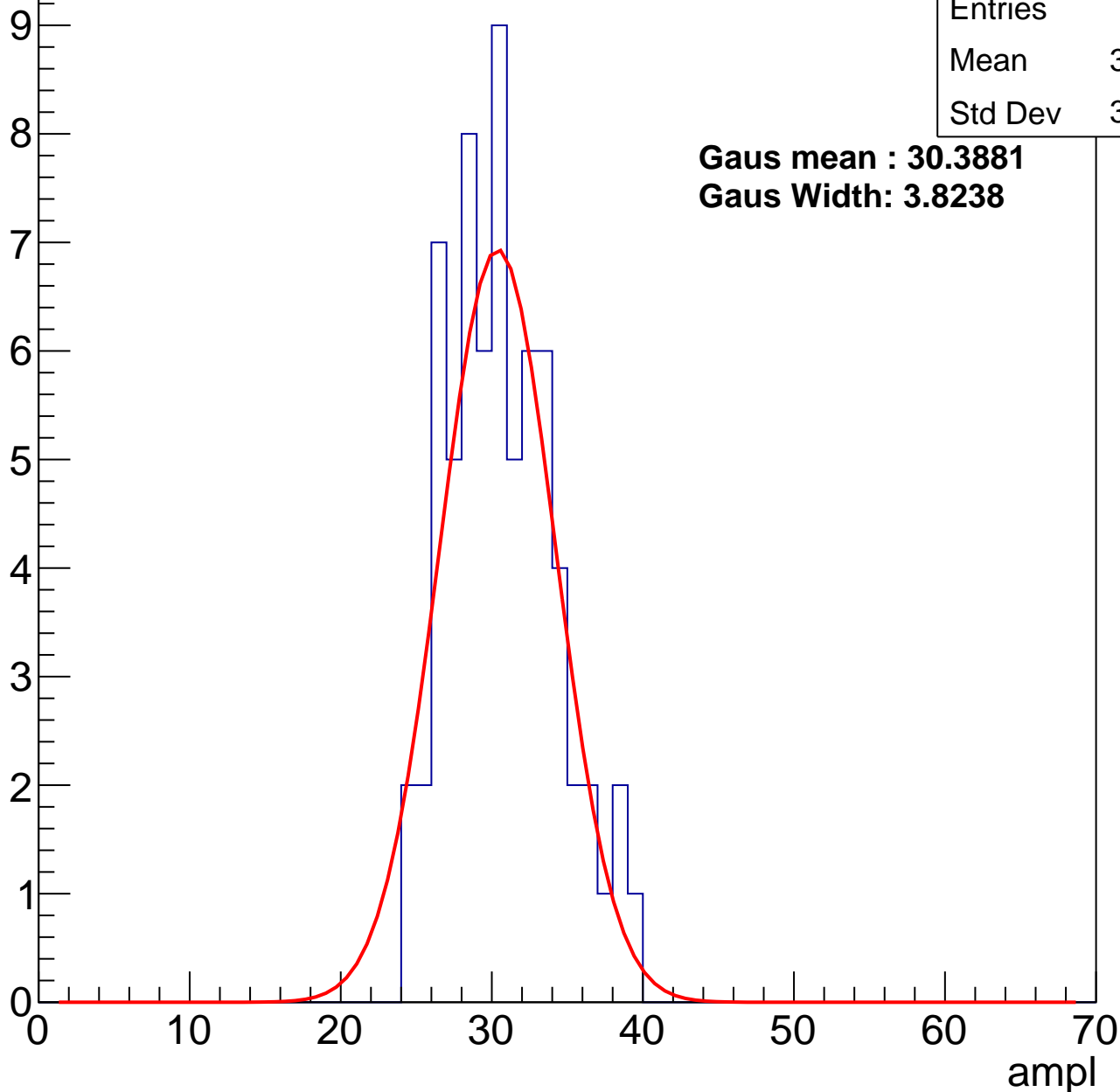
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	30.26
Std Dev	3.513

**Gaus mean : 30.3881**

**Gaus Width: 3.8238**



# B1L101S, U9-ch111, adc1

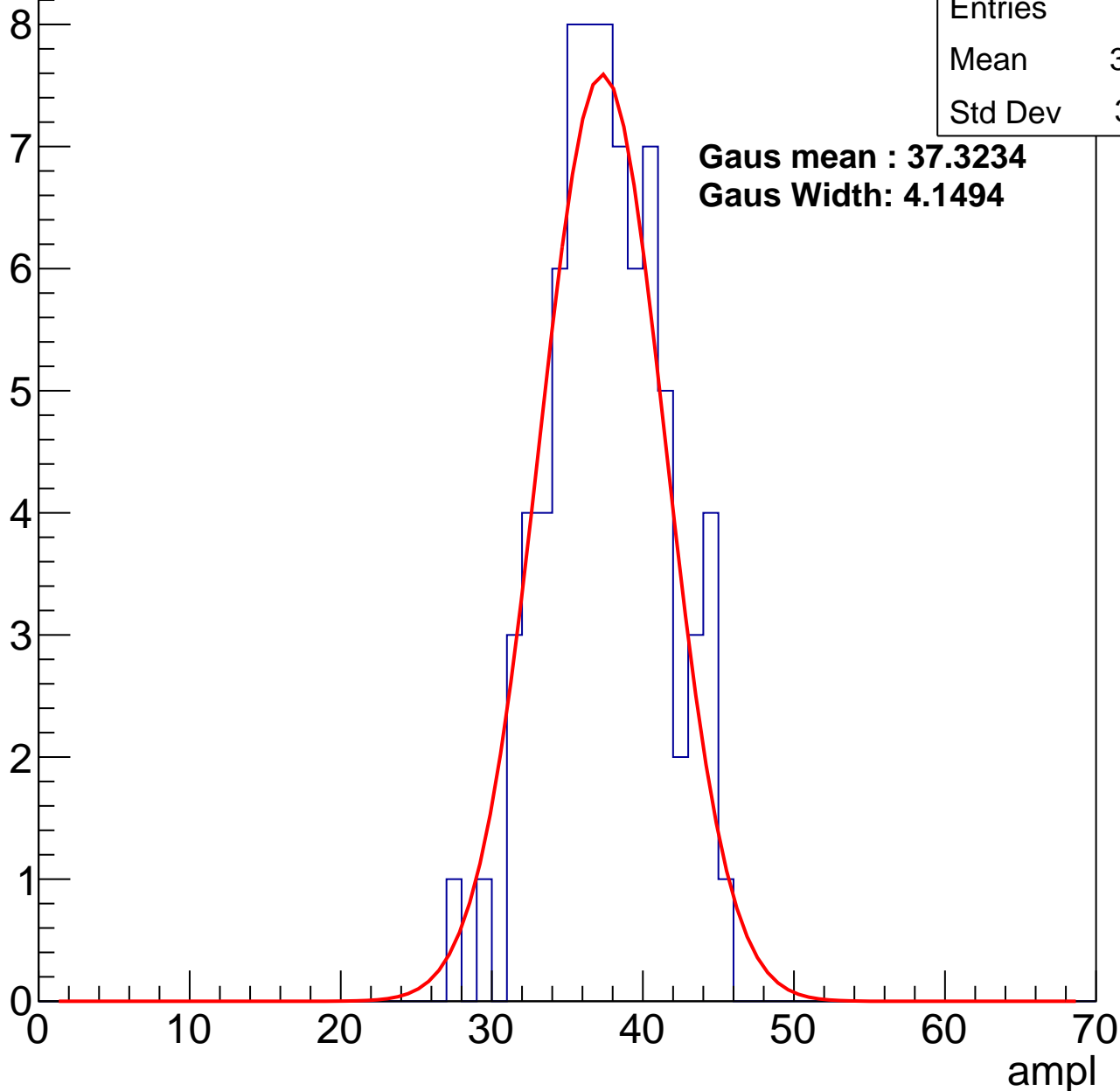
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	37.13
Std Dev	3.791

**Gaus mean : 37.3234**

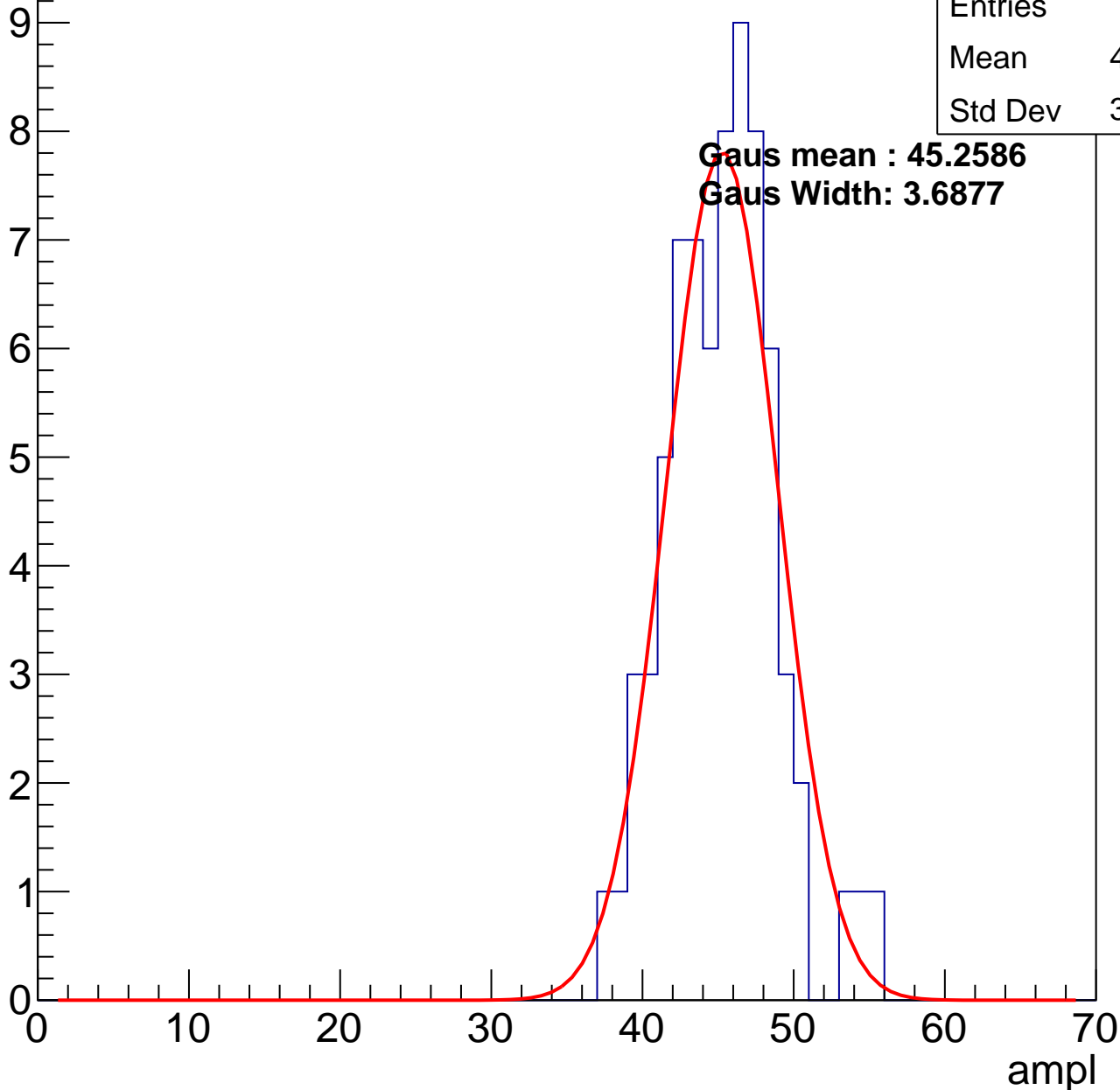
**Gaus Width: 4.1494**



# B1L101S, U9-ch111, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

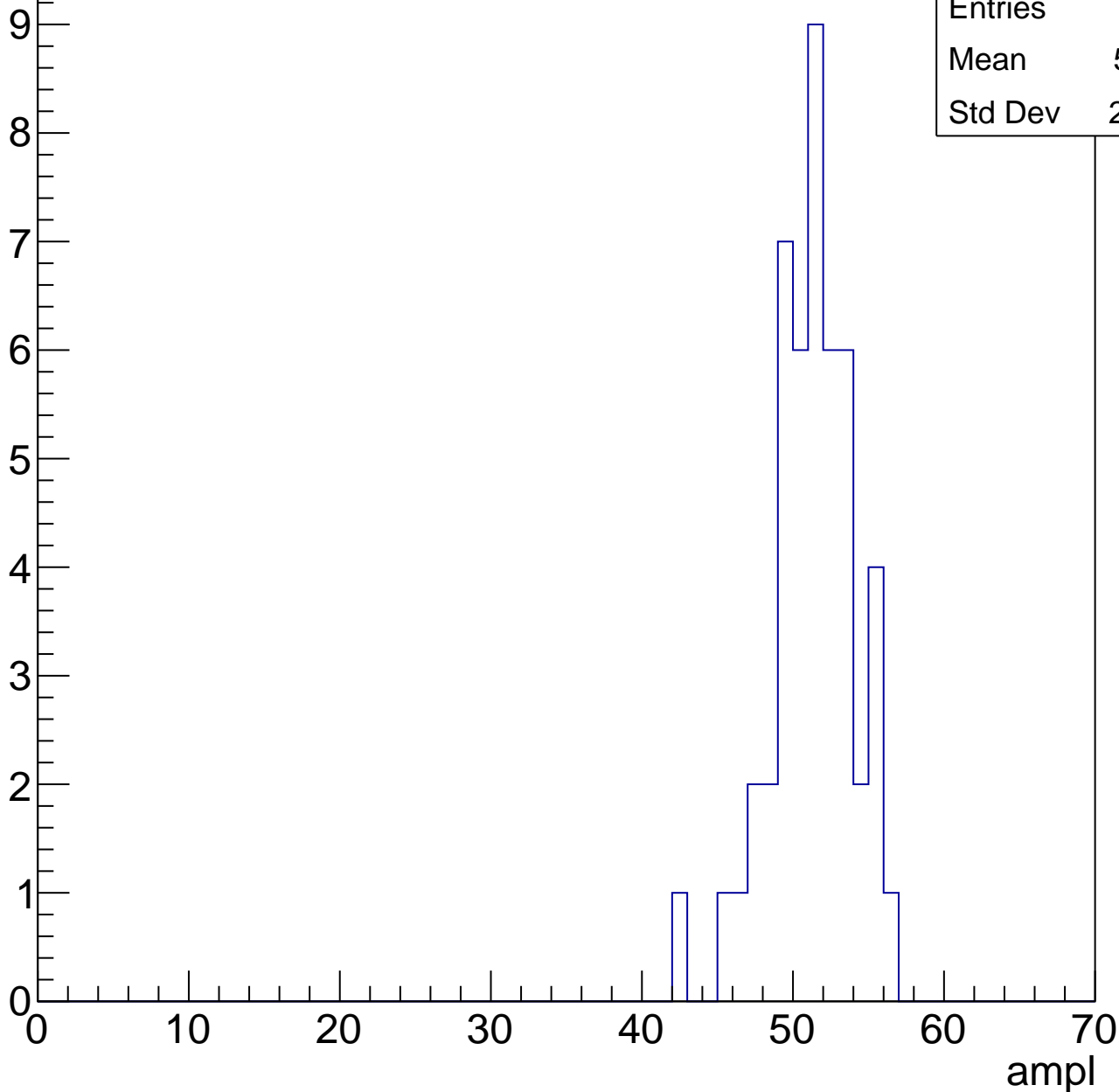


# B1L101S, U9-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	50.81
Std Dev	2.744

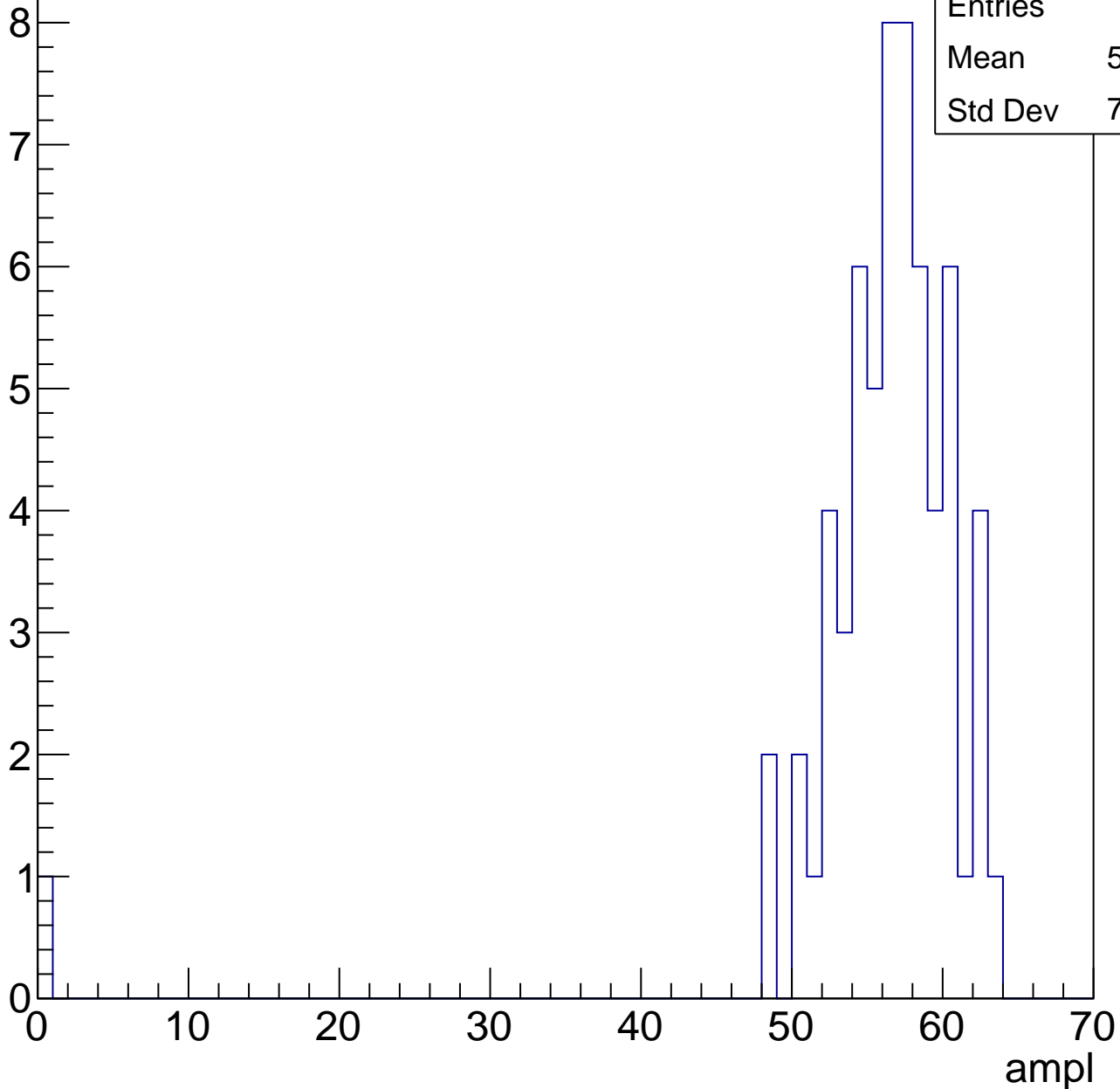


# B1L101S, U9-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	55.37
Std Dev	7.868

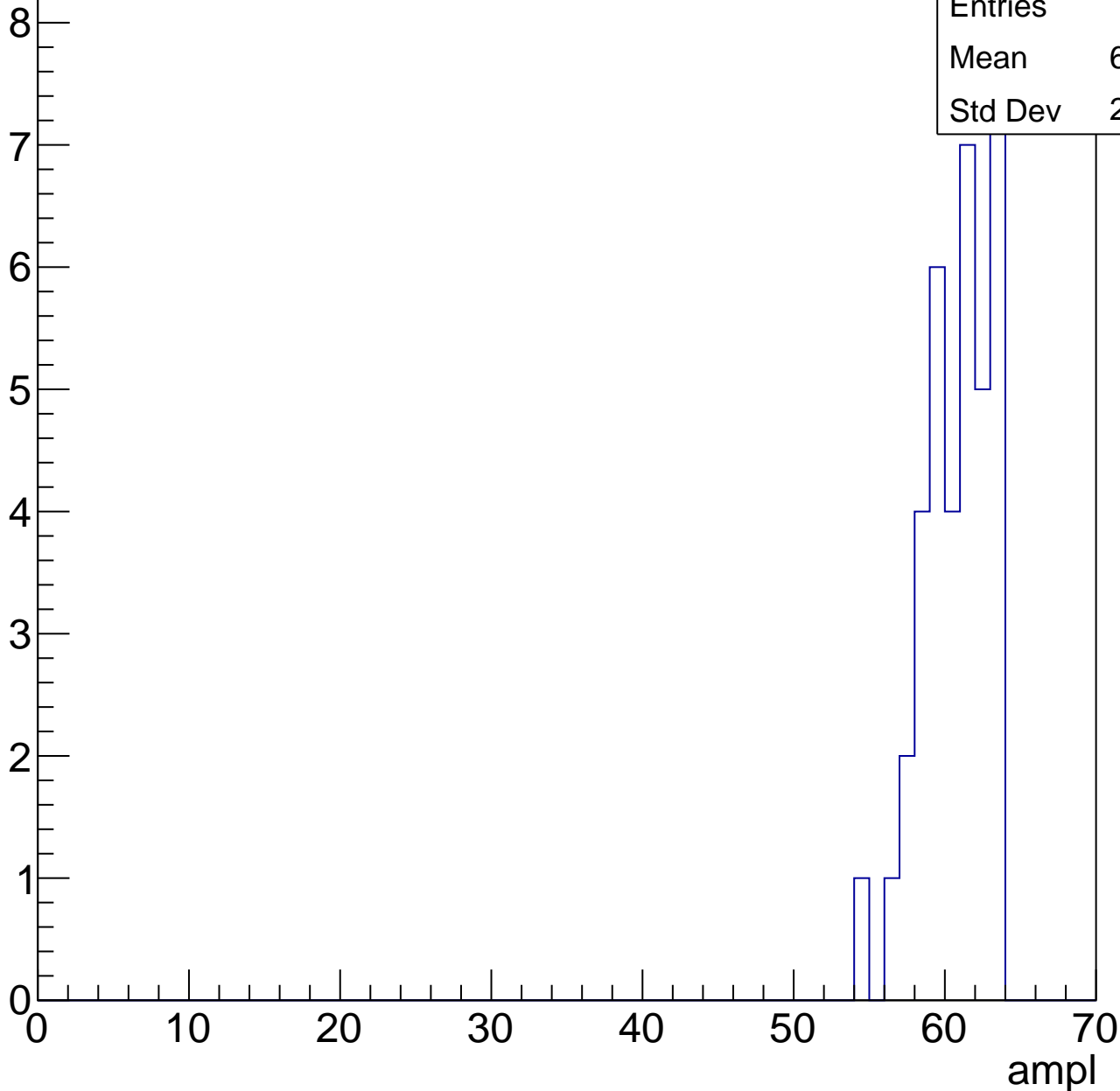


# B1L101S, U9-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

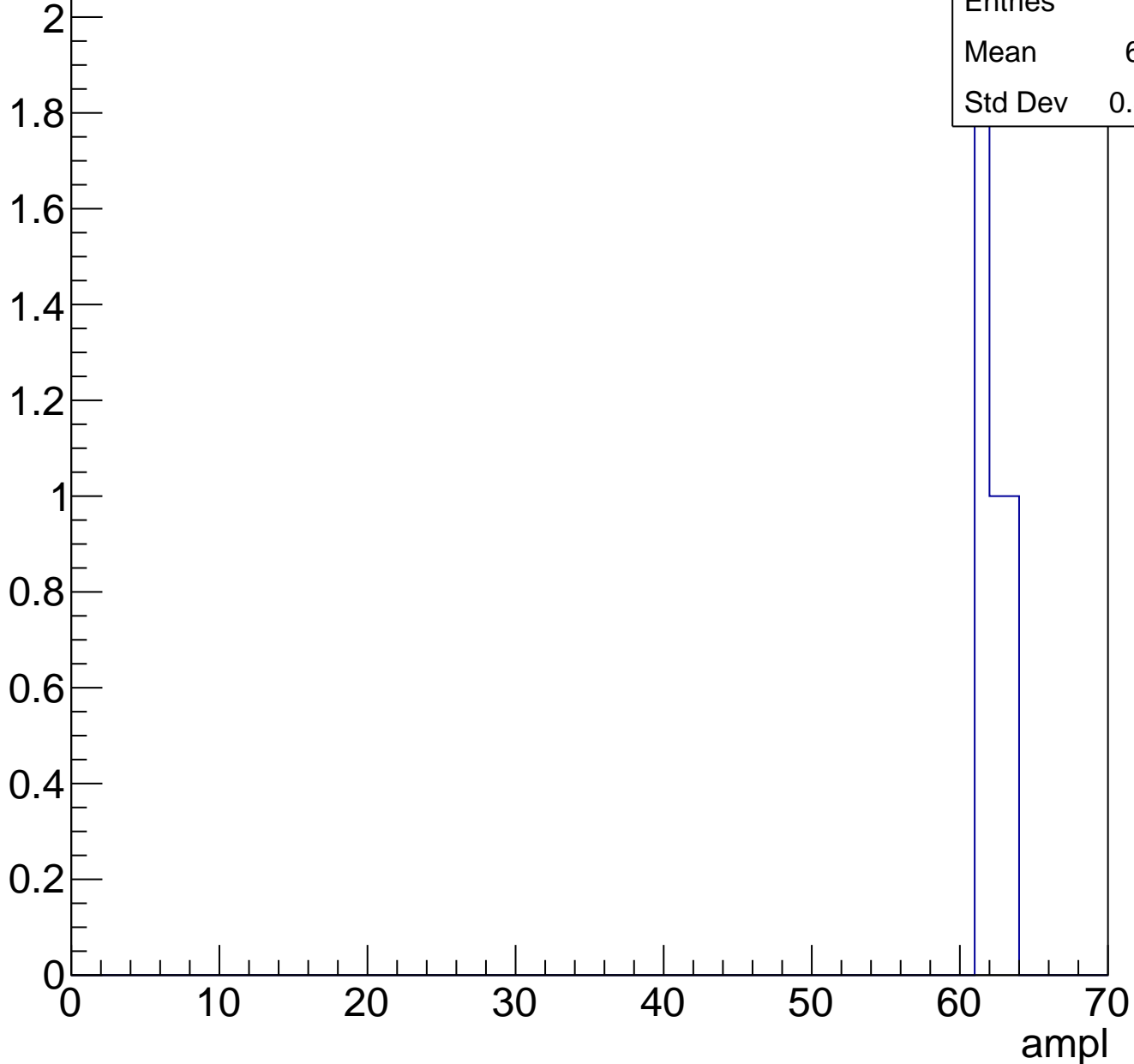
Entries	38
Mean	60.29
Std Dev	2.223



# B1L101S, U9-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

0

10

20

30

40

50

60

70

ampl

Entries	1
Mean	21
Std Dev	0

# B1L101S, U9-ch112, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	80
Mean	29.23
Std Dev	6.629

**Gaus mean : 30.9087**

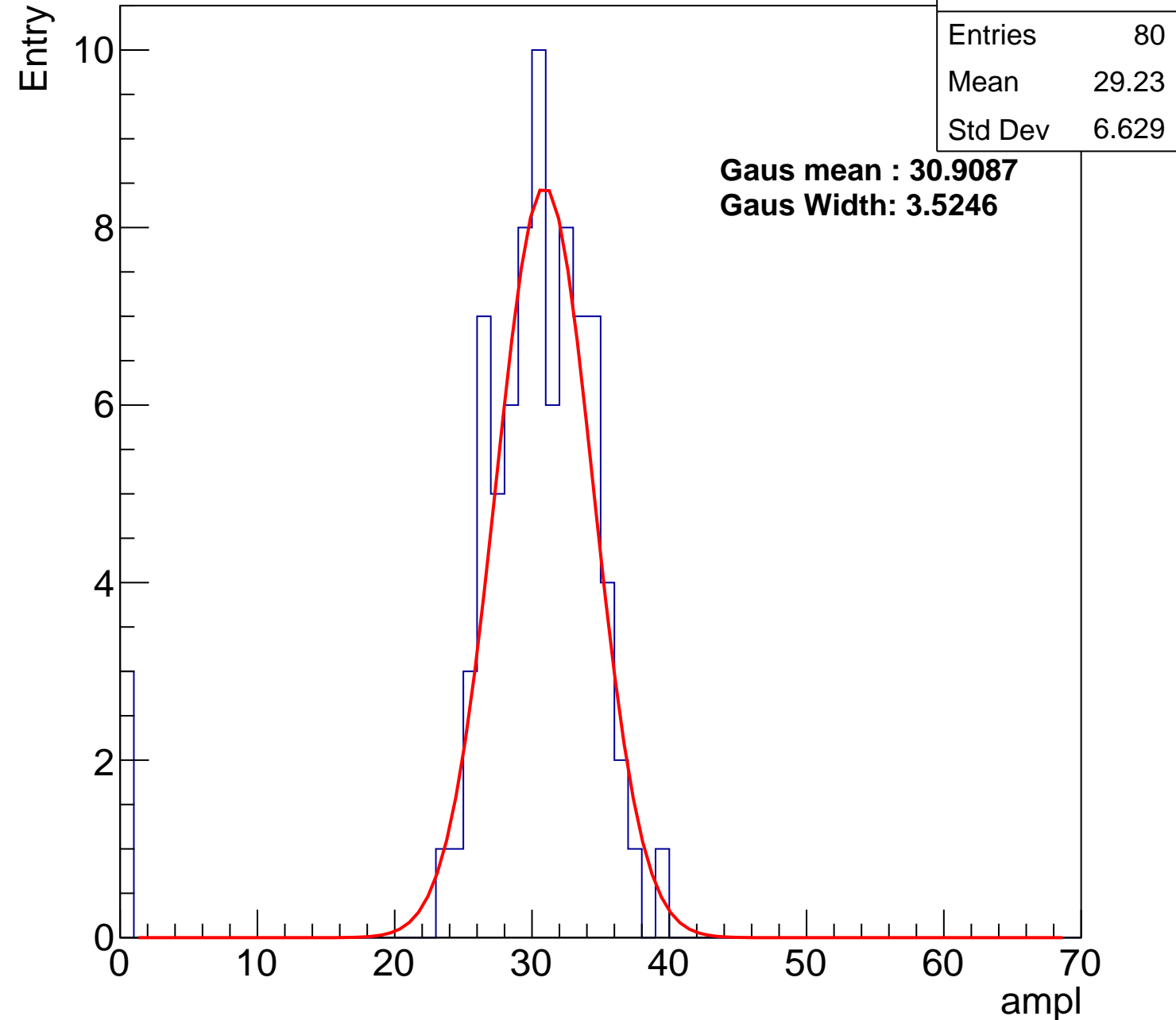
**Gaus Width: 3.5246**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U9-ch112, adc1

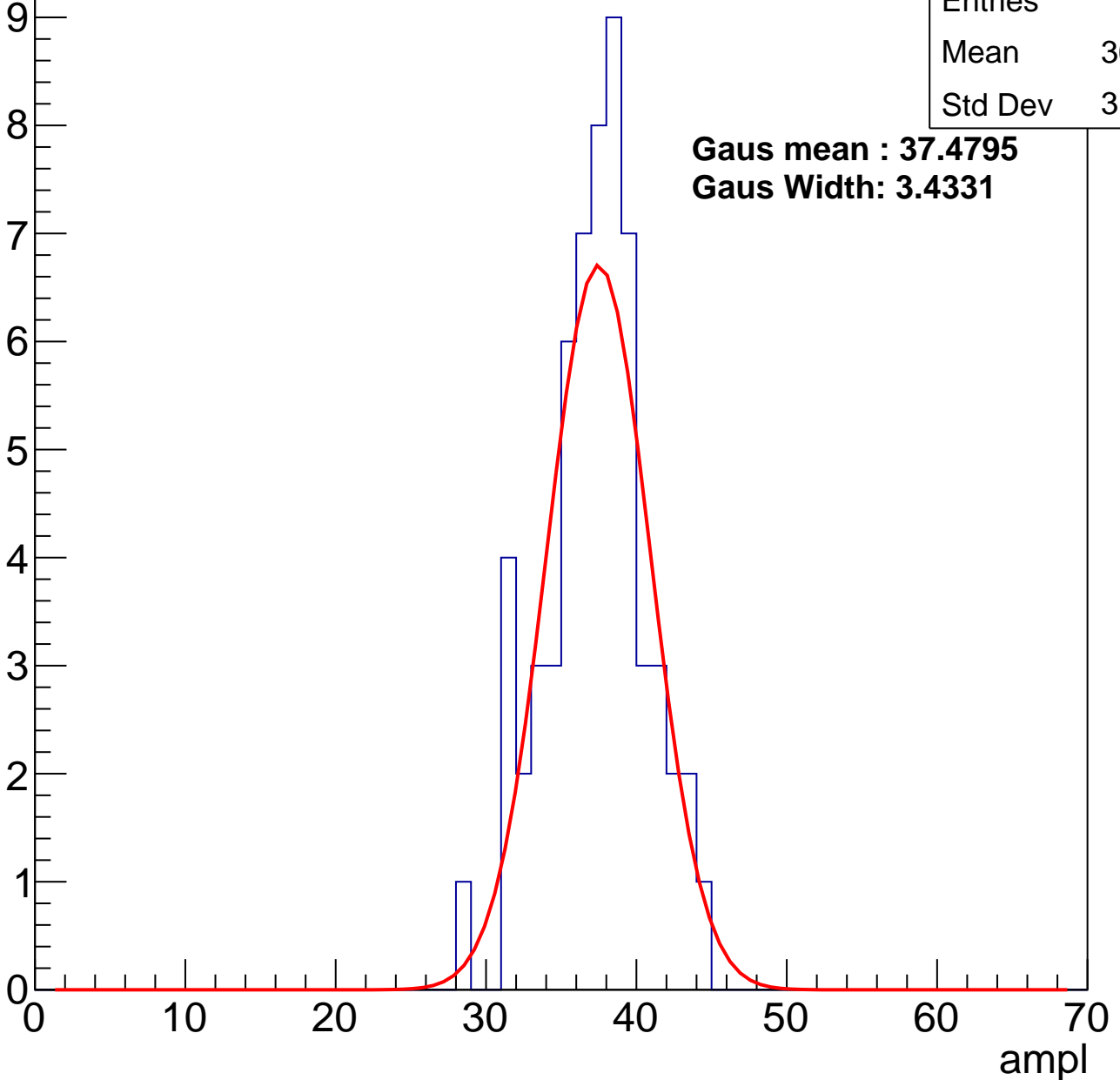
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	36.84
Std Dev	3.295

**Gaus mean : 37.4795**

**Gaus Width: 3.4331**



# B1L101S, U9-ch112, adc2

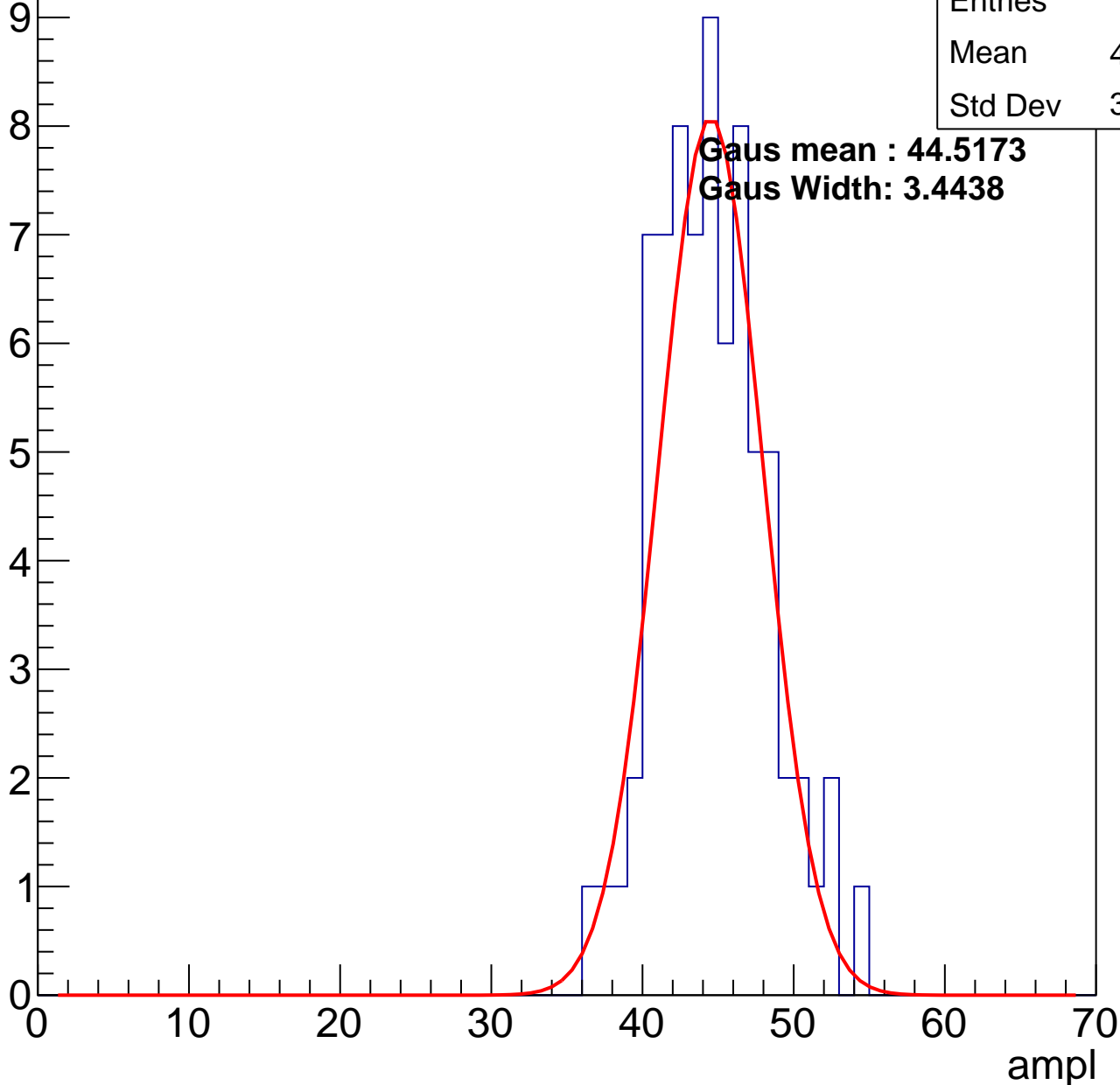
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	44.12
Std Dev	3.604

**Gaus mean : 44.5173**

**Gaus Width: 3.4438**

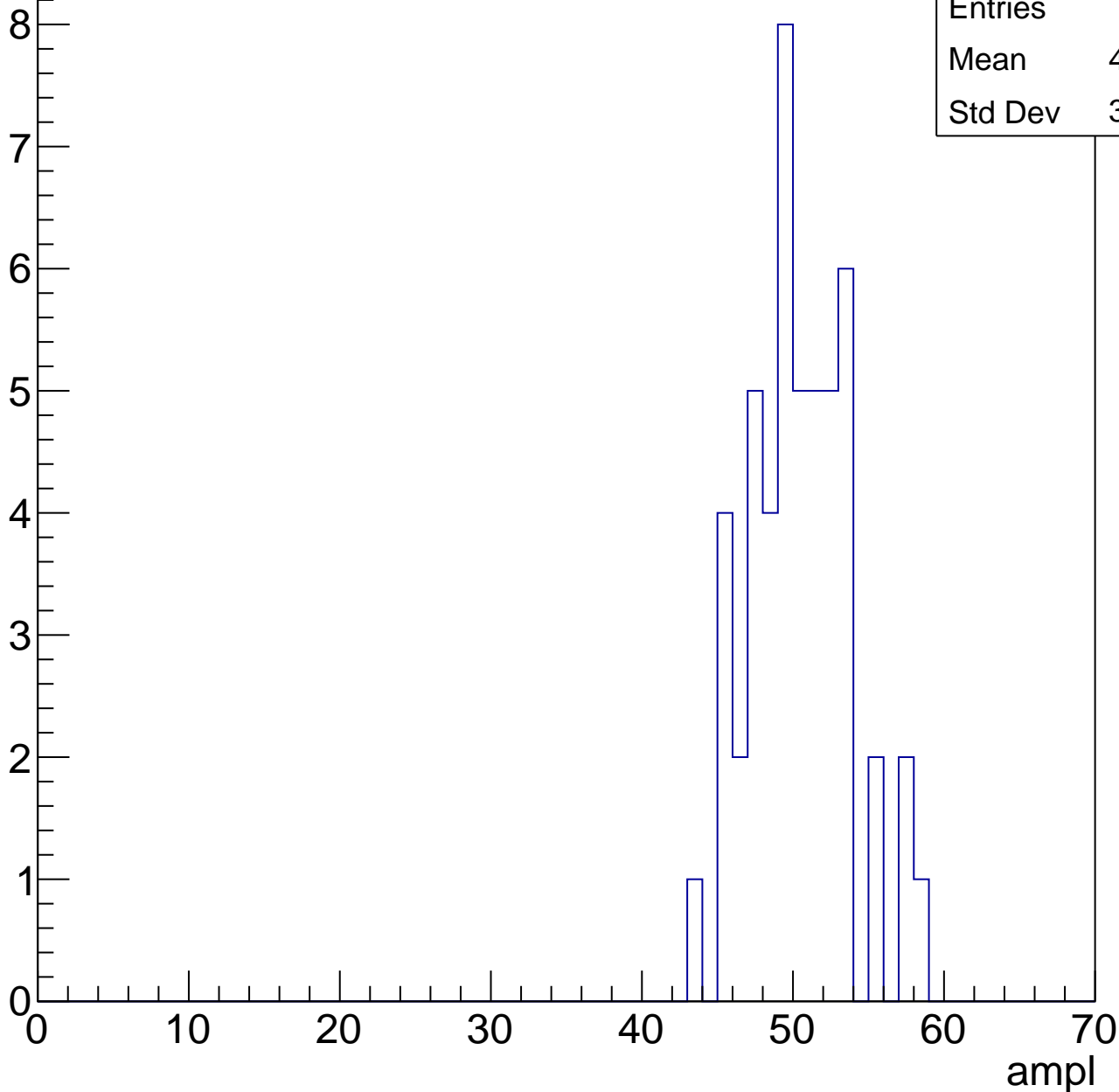


# B1L101S, U9-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	49.98
Std Dev	3.289

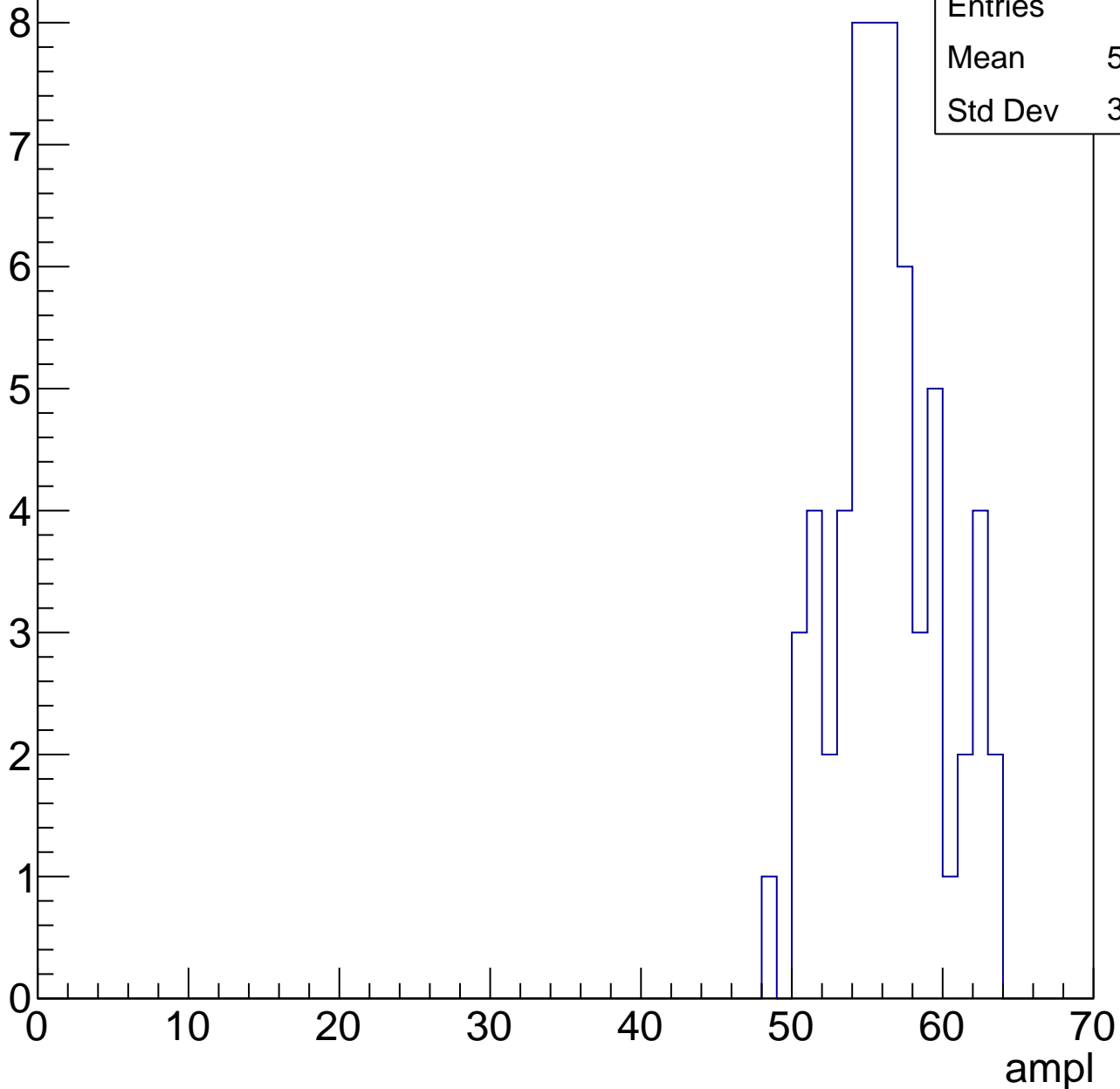


# B1L101S, U9-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	55.82
Std Dev	3.504



# B1L101S, U9-ch112, adc5

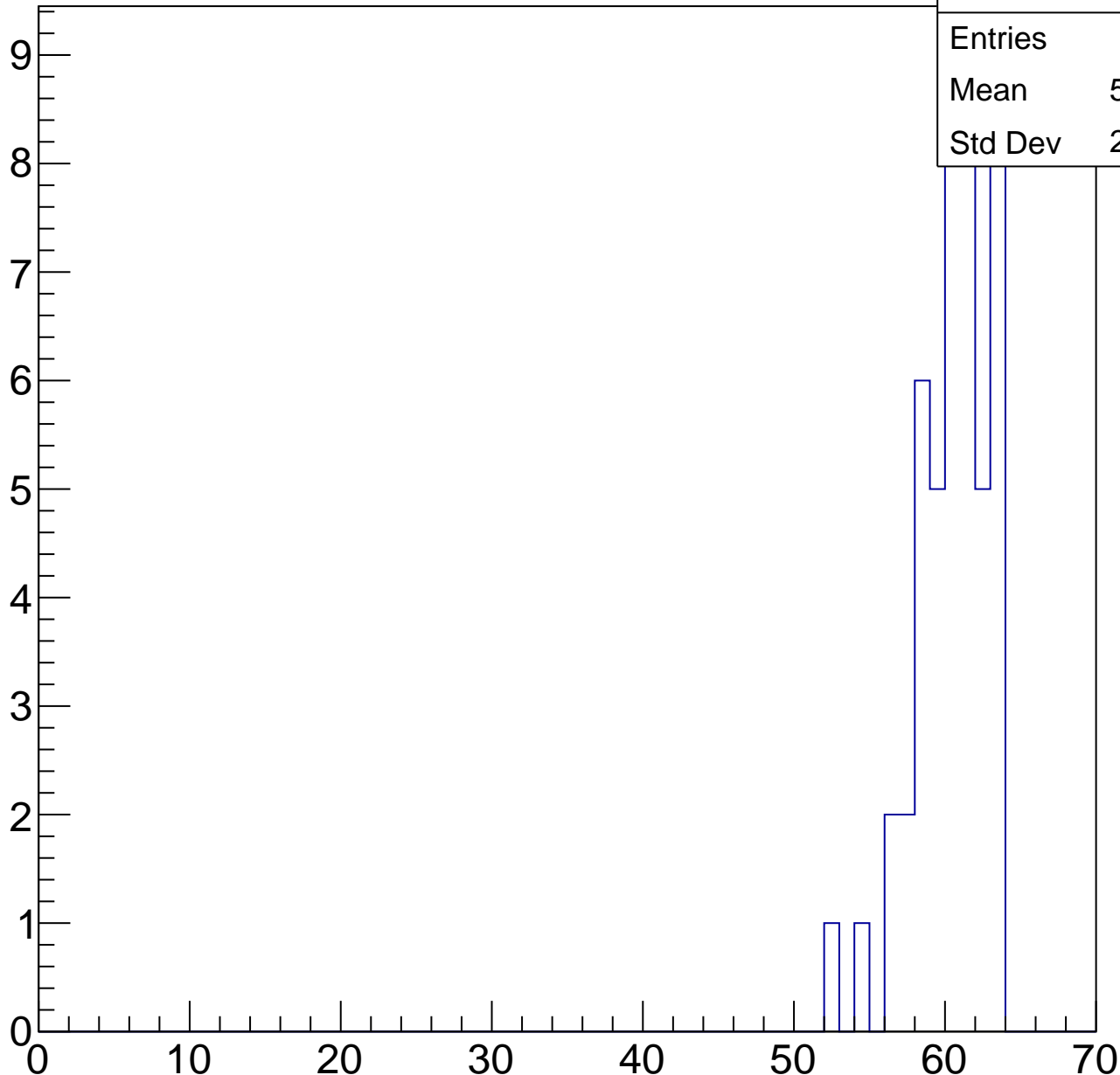
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	47
Mean	59.94
Std Dev	2.436

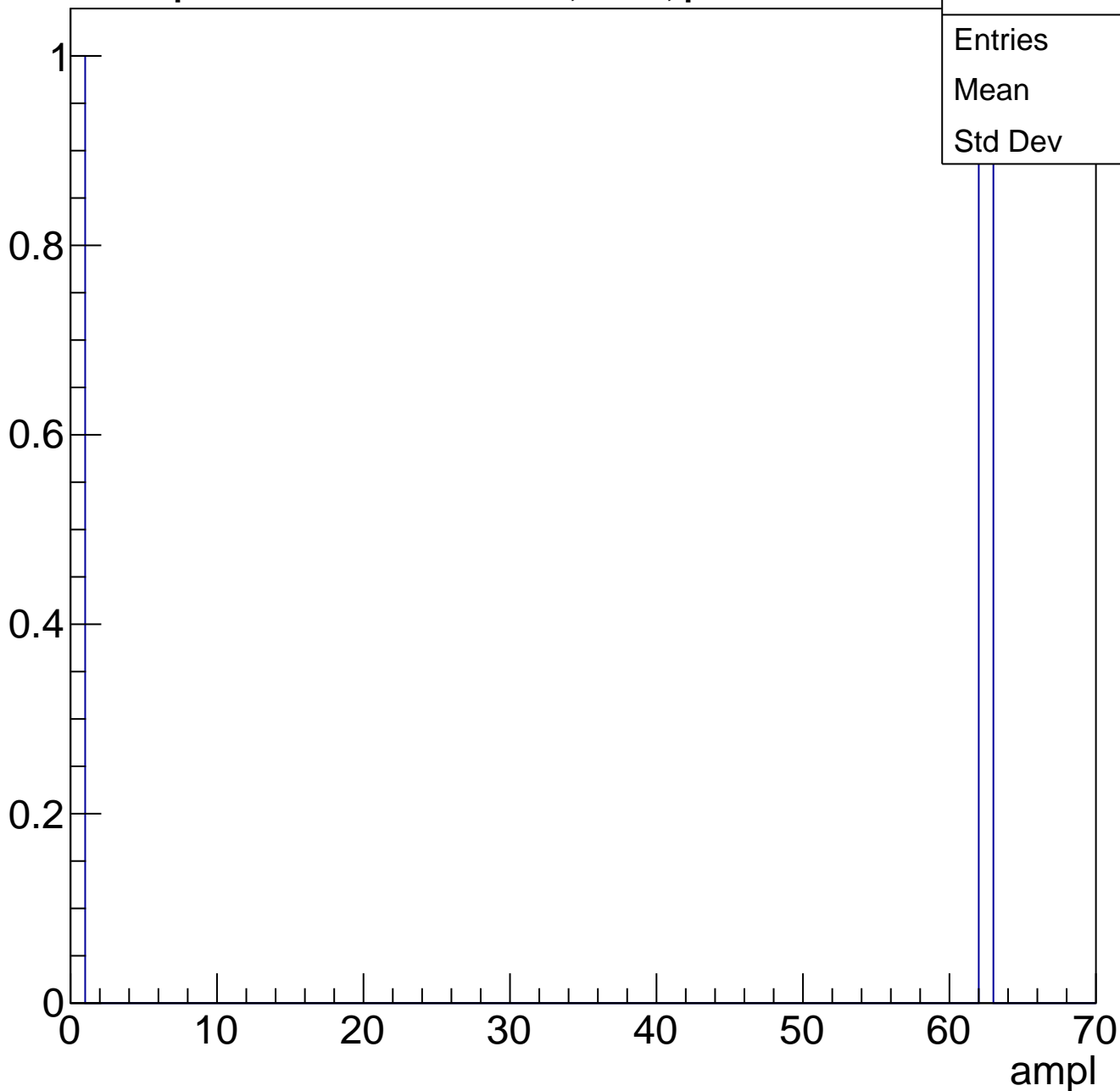
ampl



# B1L101S, U9-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch113, adc0

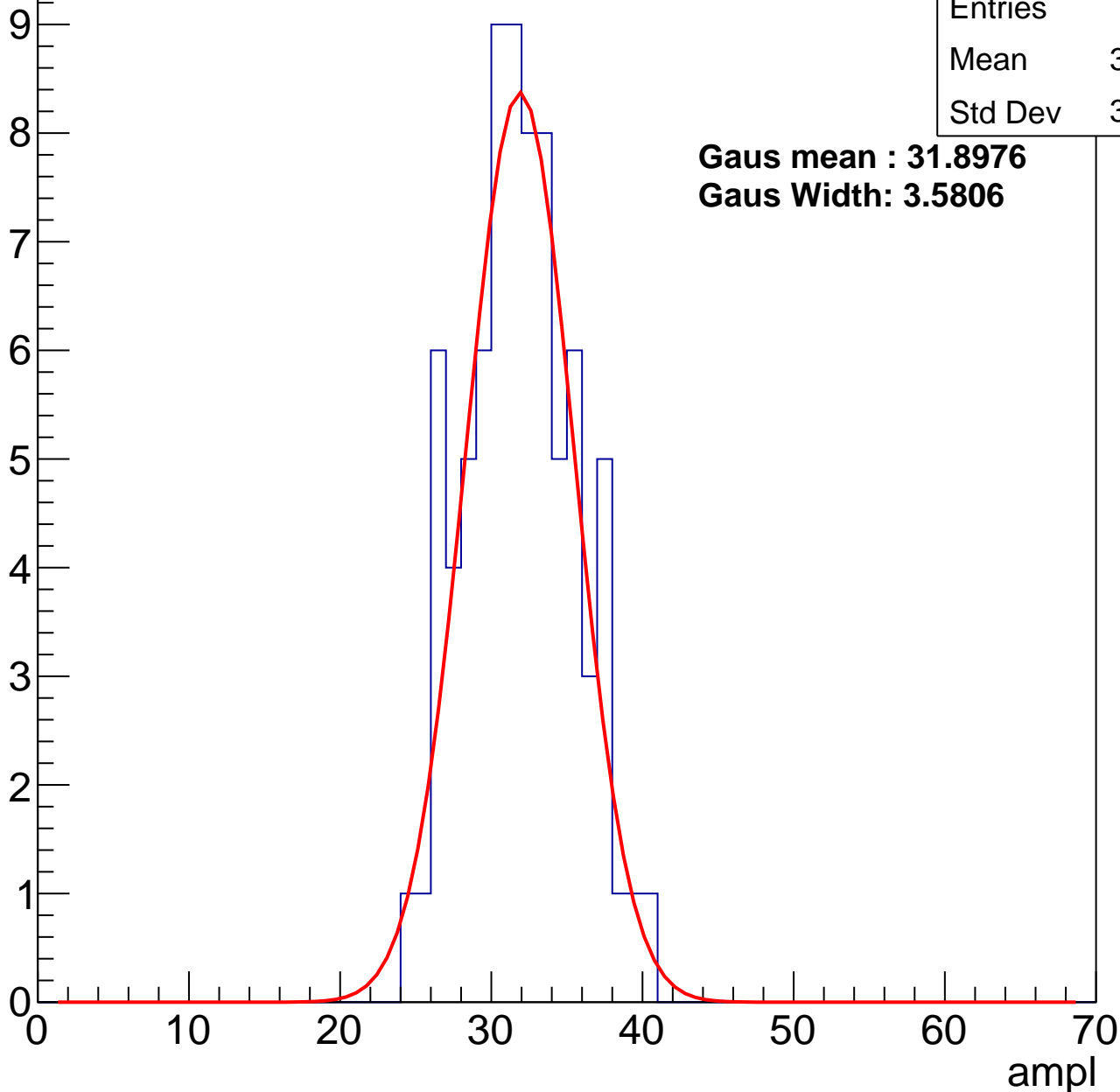
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	31.47
Std Dev	3.539

**Gaus mean : 31.8976**

**Gaus Width: 3.5806**



# B1L101S, U9-ch113, adc1

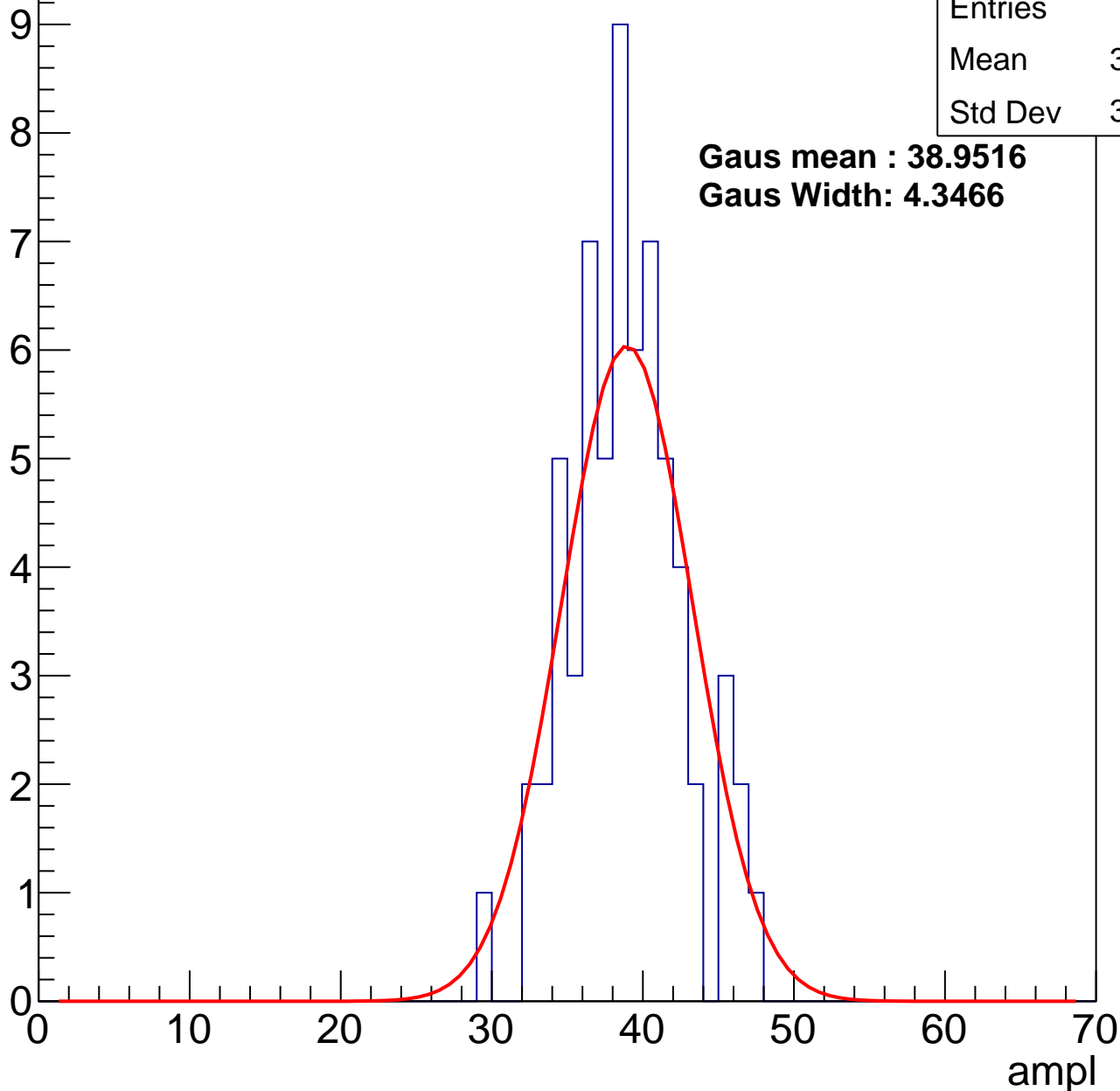
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	38.44
Std Dev	3.708

**Gaus mean : 38.9516**

**Gaus Width: 4.3466**



# B1L101S, U9-ch113, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	74
Mean	45.07
Std Dev	3.554

**Gaus mean : 45.8274**

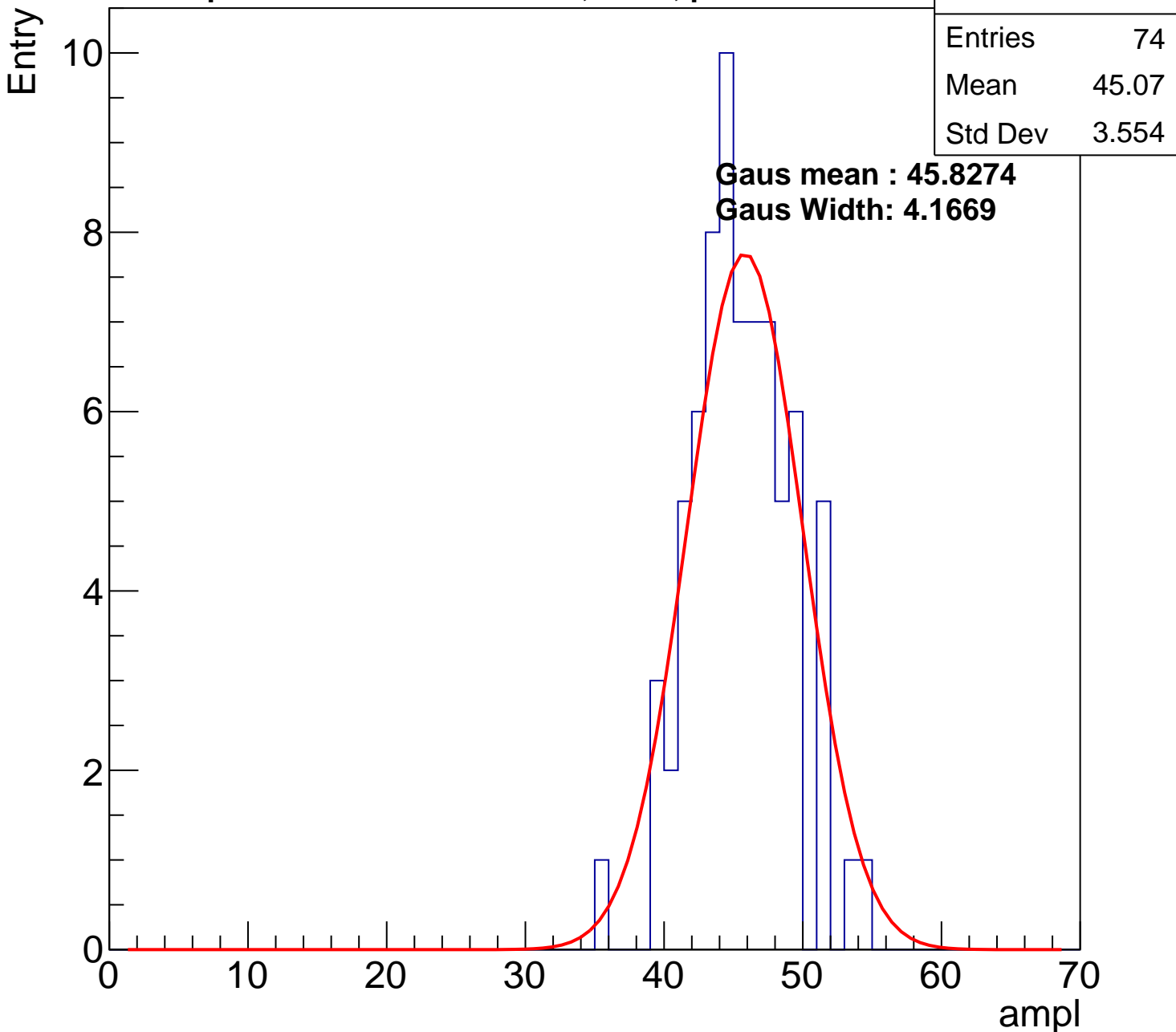
**Gaus Width: 4.1669**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

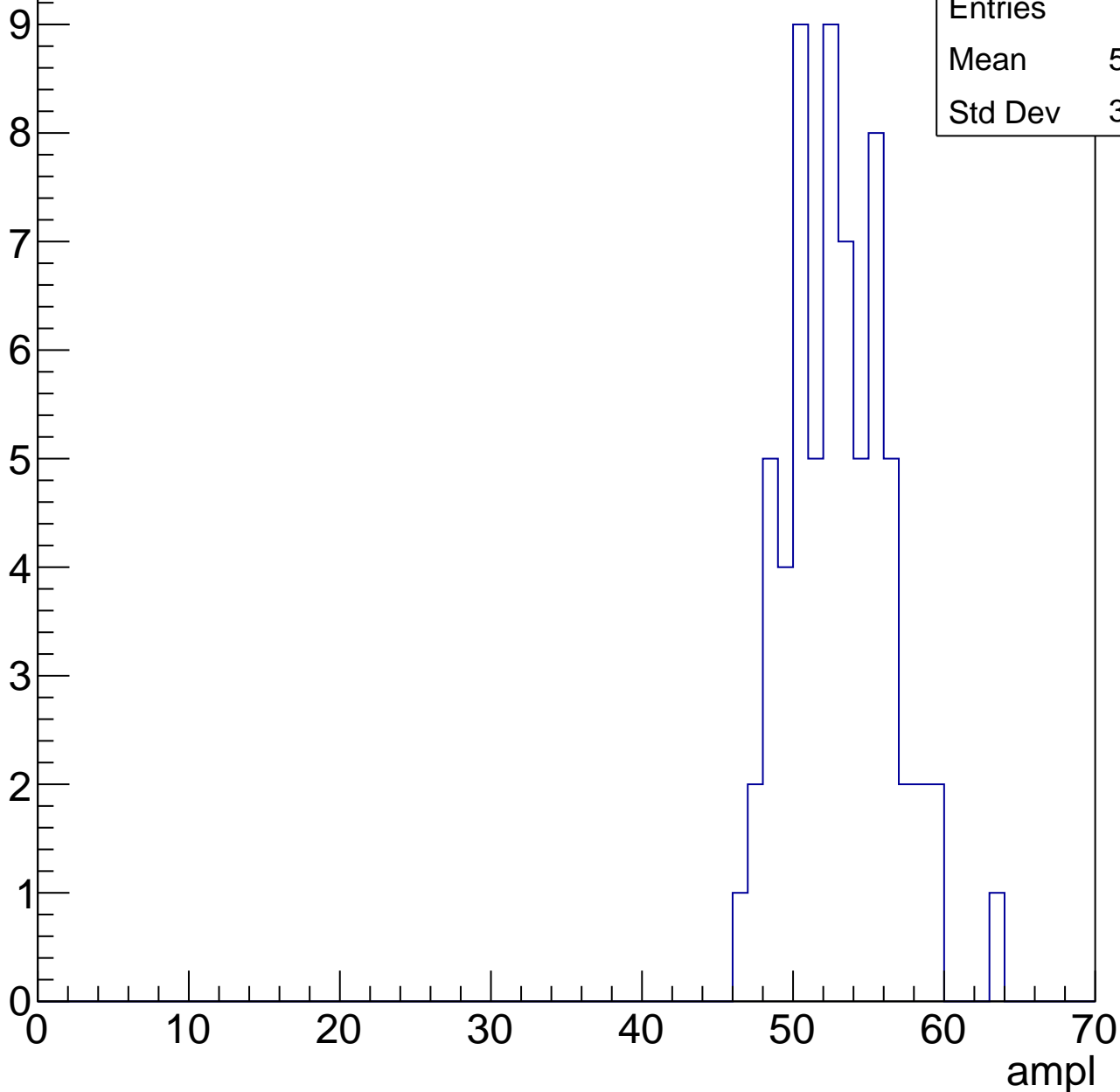


# B1L101S, U9-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	52.55
Std Dev	3.329

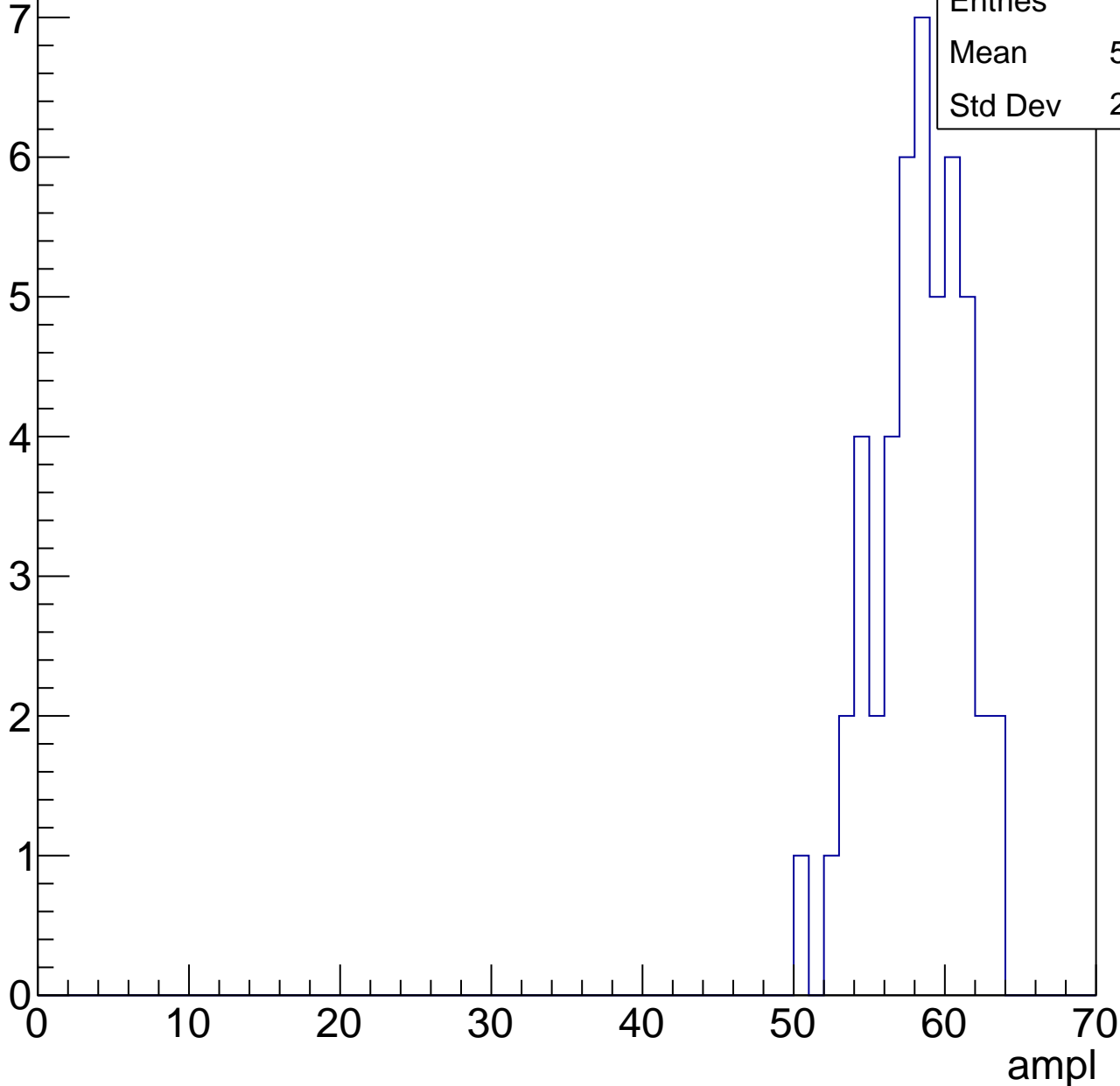


# B1L101S, U9-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	57.79
Std Dev	2.946

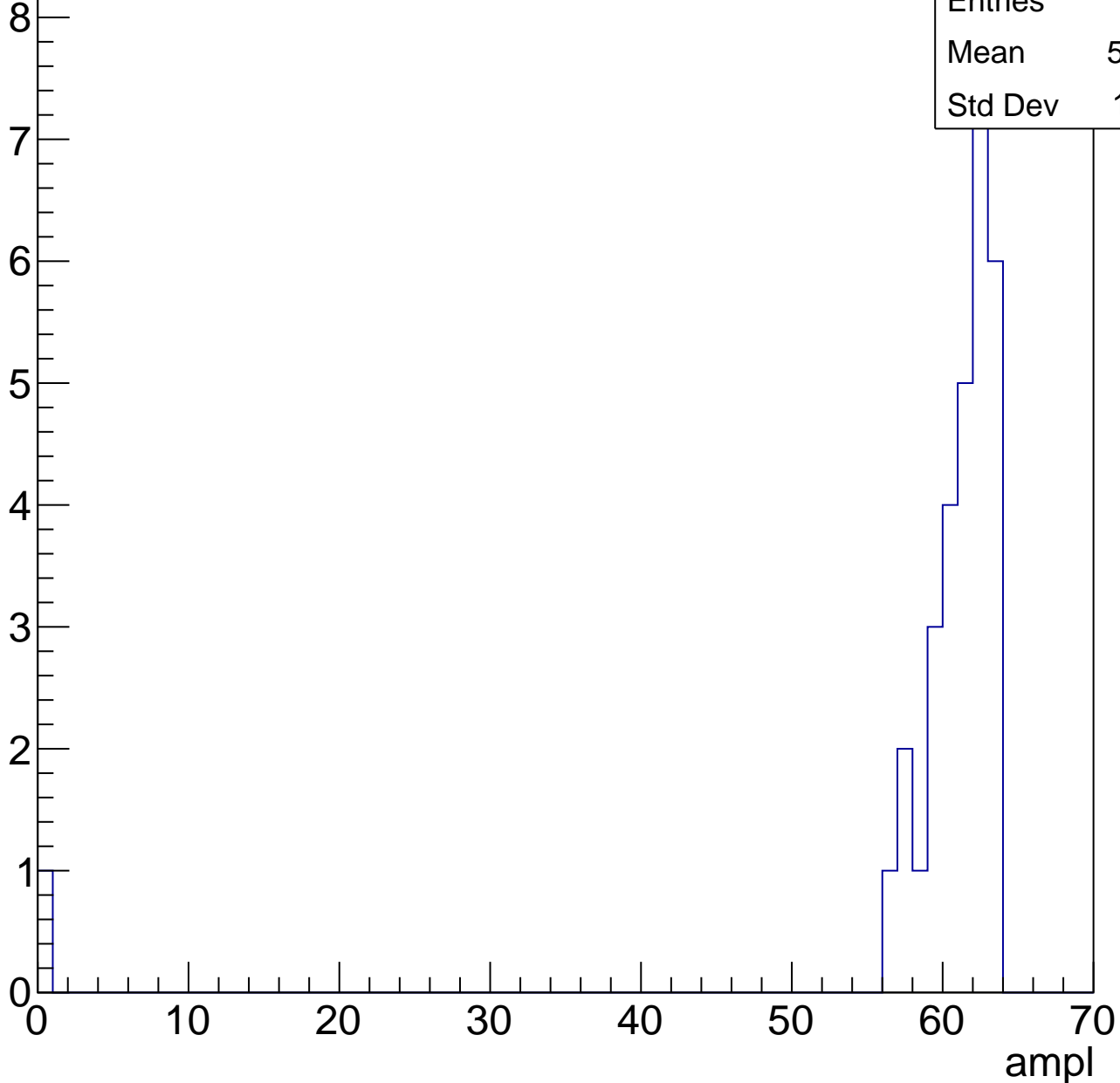


# B1L101S, U9-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	31
Mean	58.84
Std Dev	10.91



# B1L101S, U9-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



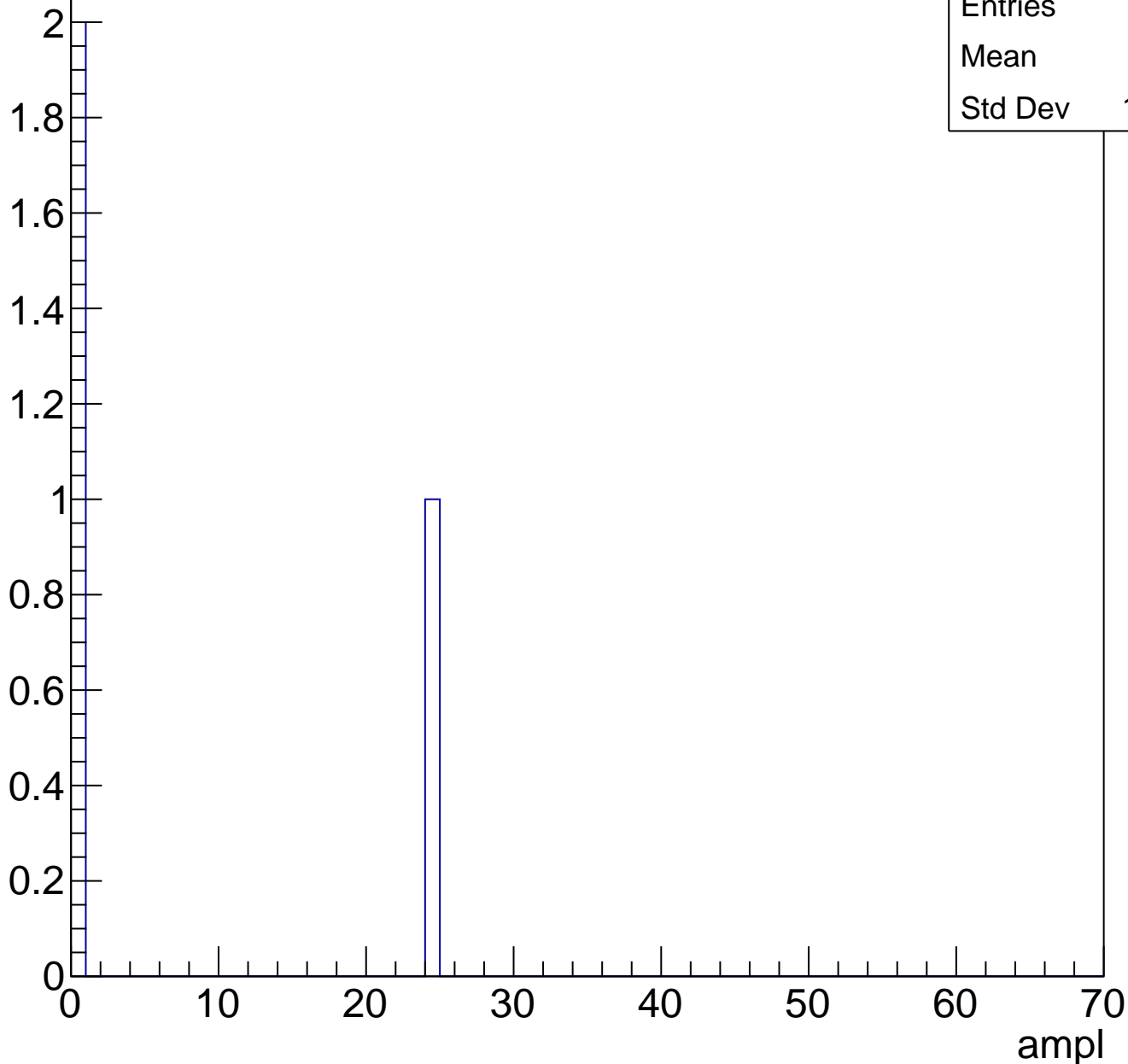
Entries	1
Mean	63
Std Dev	0



# B1L101S, U9-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch114, adc0

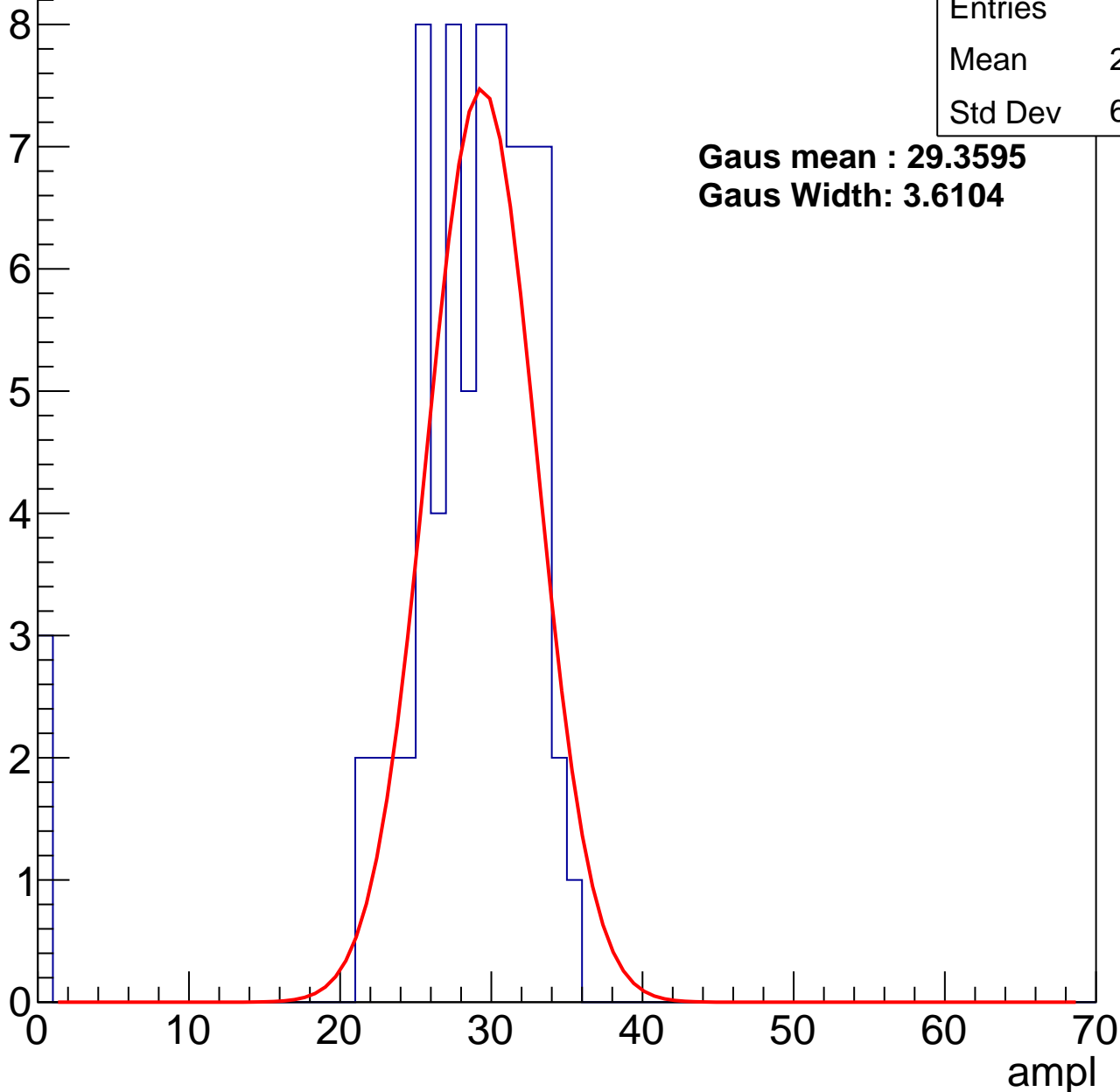
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	27.46
Std Dev	6.478

**Gaus mean : 29.3595**

**Gaus Width: 3.6104**



# B1L101S, U9-ch114, adc1

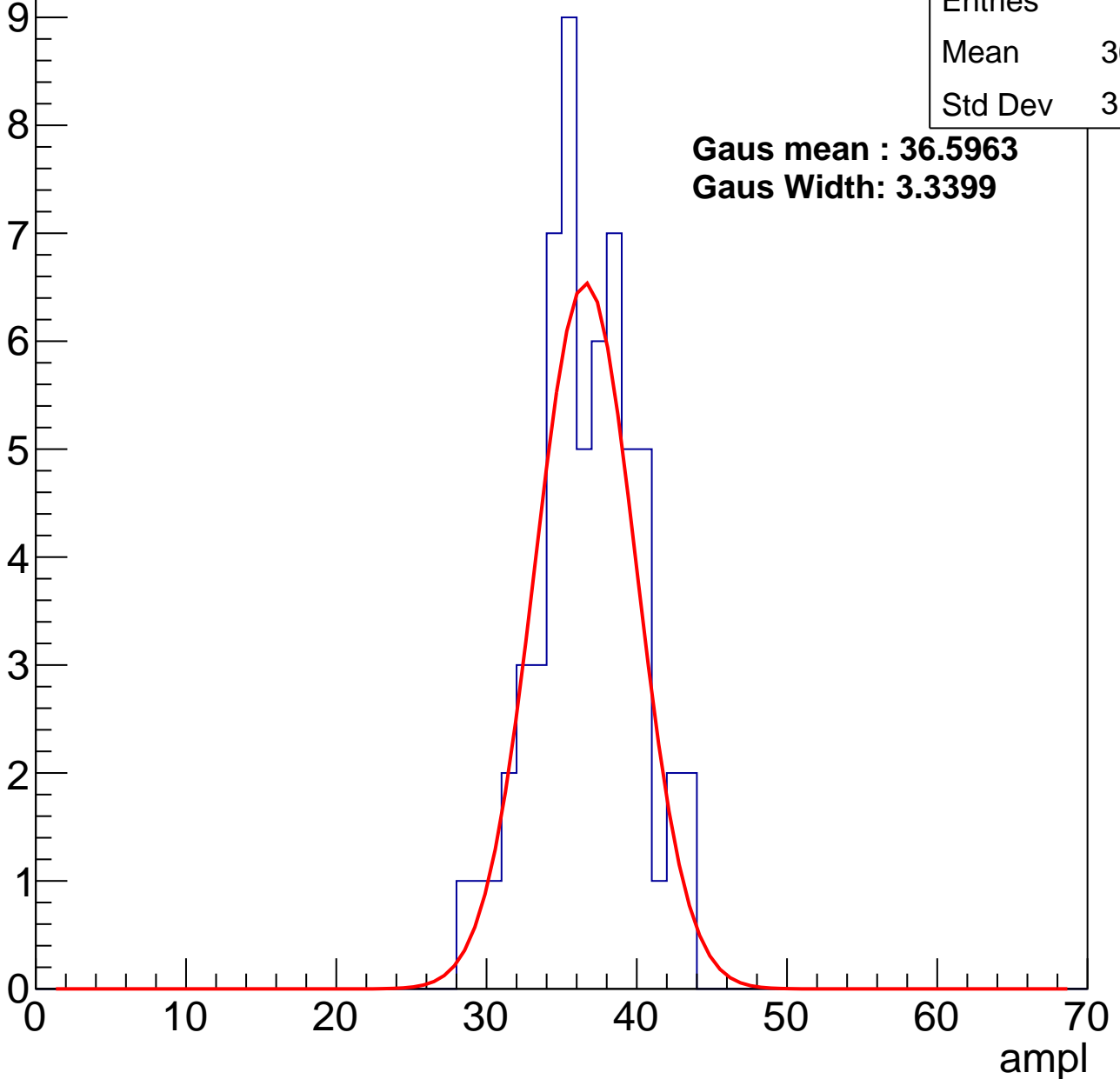
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	36.18
Std Dev	3.324

**Gaus mean : 36.5963**

**Gaus Width: 3.3399**



# B1L101S, U9-ch114, adc2

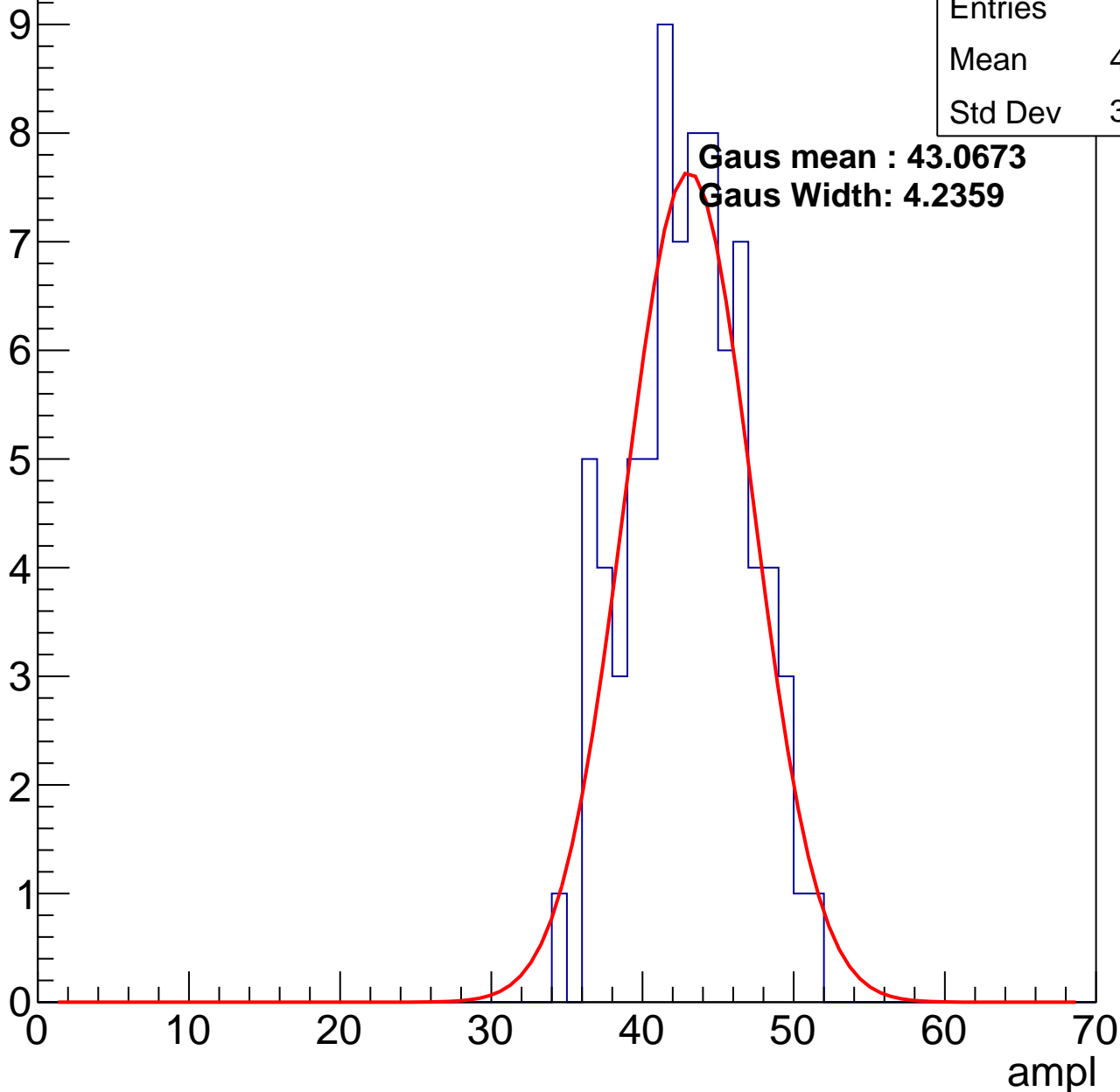
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	42.59
Std Dev	3.816

**Gaus mean : 43.0673**

**Gaus Width: 4.2359**

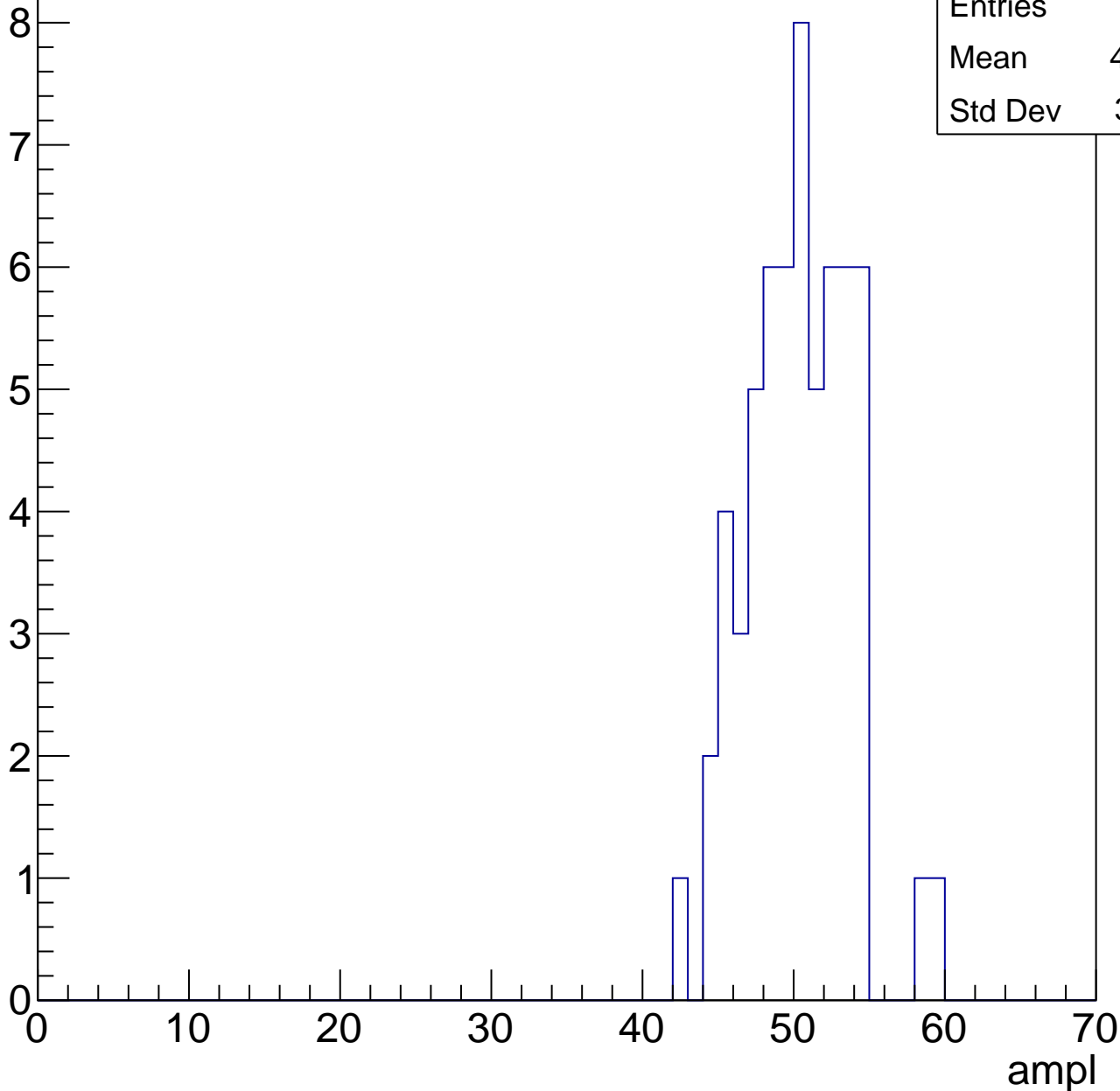


# B1L101S, U9-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	49.85
Std Dev	3.371

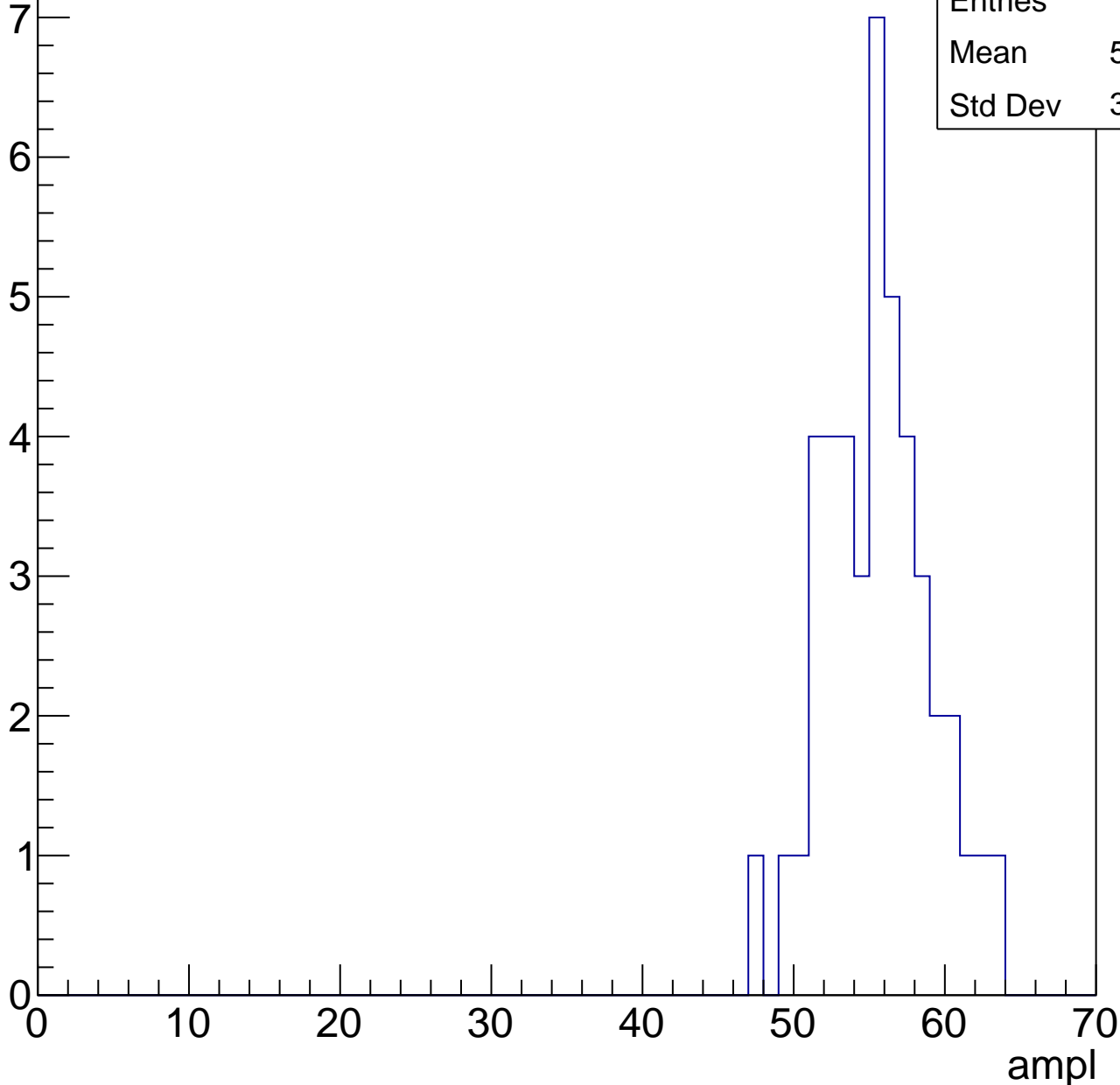


# B1L101S, U9-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	44
Mean	55.07
Std Dev	3.447

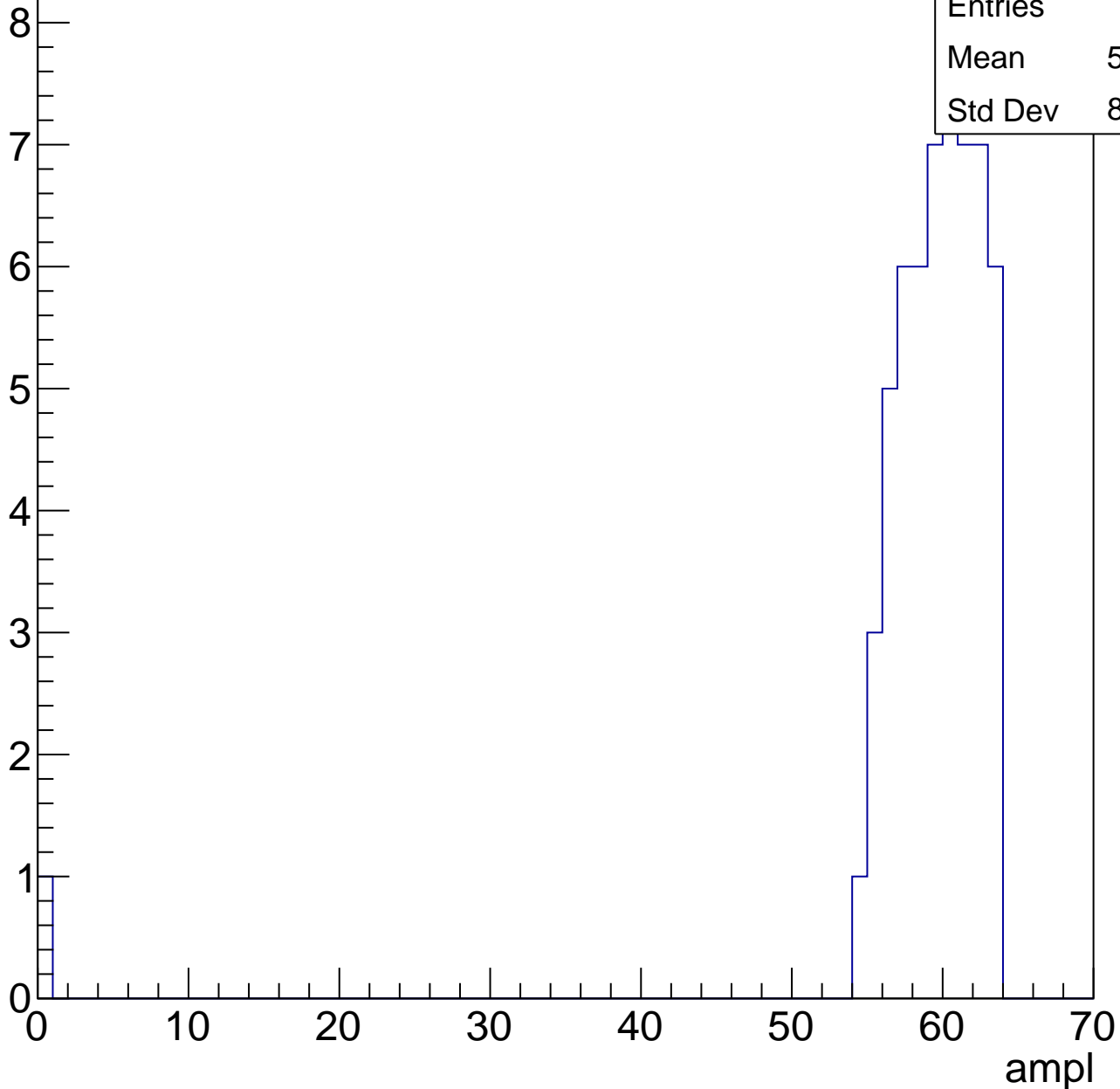


# B1L101S, U9-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	58.26
Std Dev	8.157



# B1L101S, U9-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	62
Std Dev	0.8165

0 10 20 30 40 50 60 70

ampl



# B1L101S, U9-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	63
Std Dev	0

# B1L101S, U9-ch115, adc0

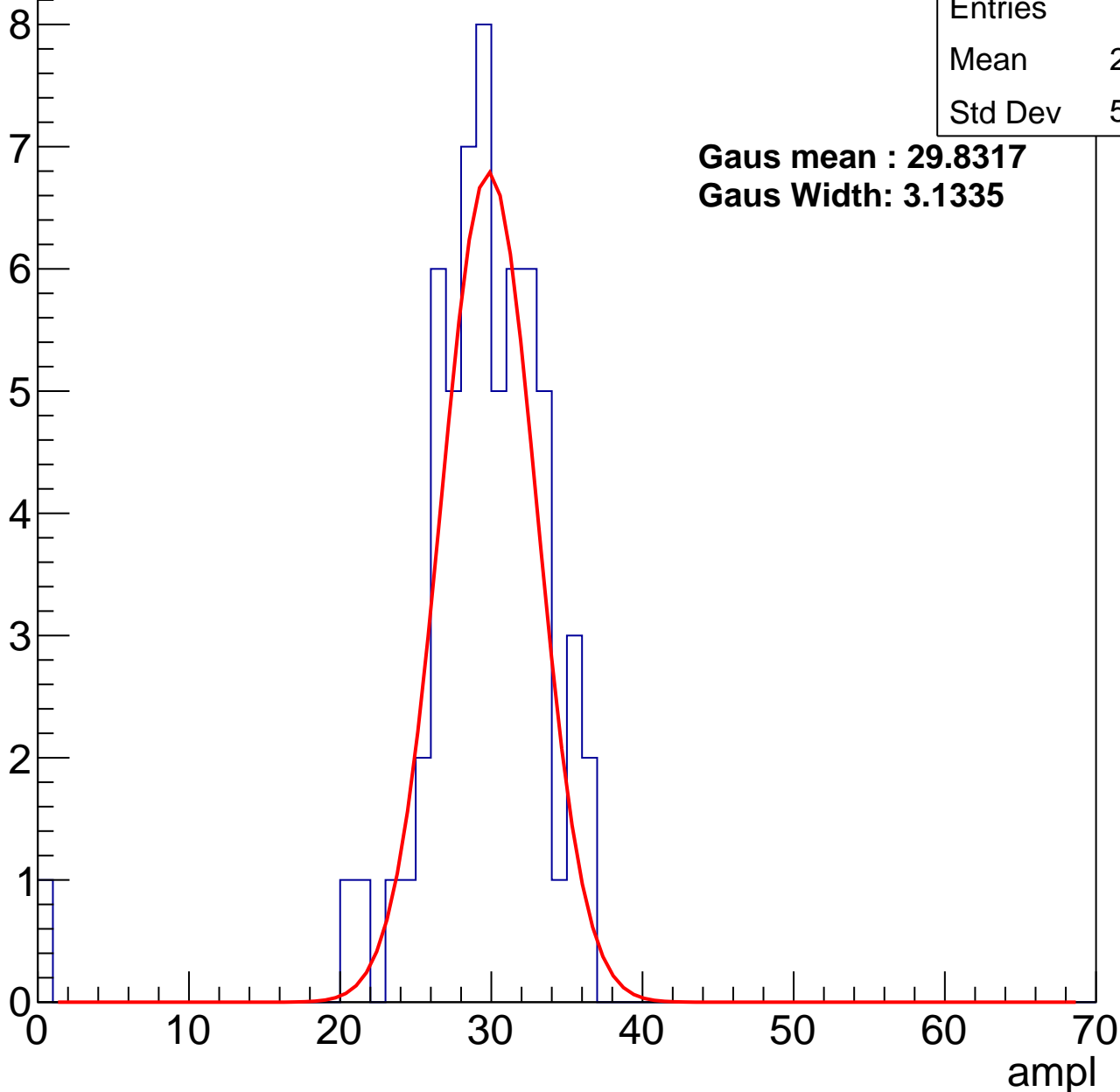
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	28.87
Std Dev	5.046

**Gaus mean : 29.8317**

**Gaus Width: 3.1335**



# B1L101S, U9-ch115, adc1

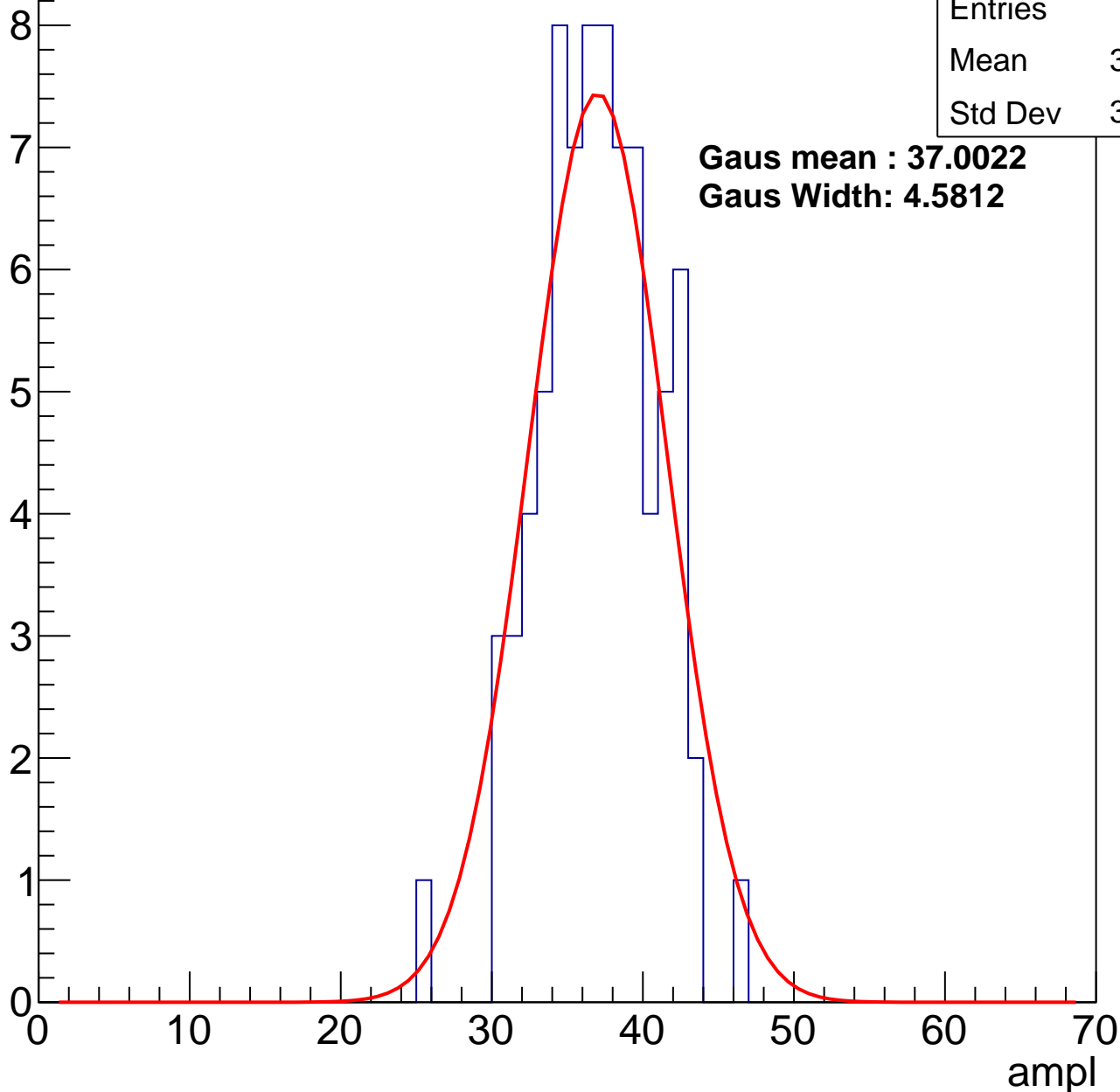
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	36.58
Std Dev	3.777

**Gaus mean : 37.0022**

**Gaus Width: 4.5812**



# B1L101S, U9-ch115, adc2

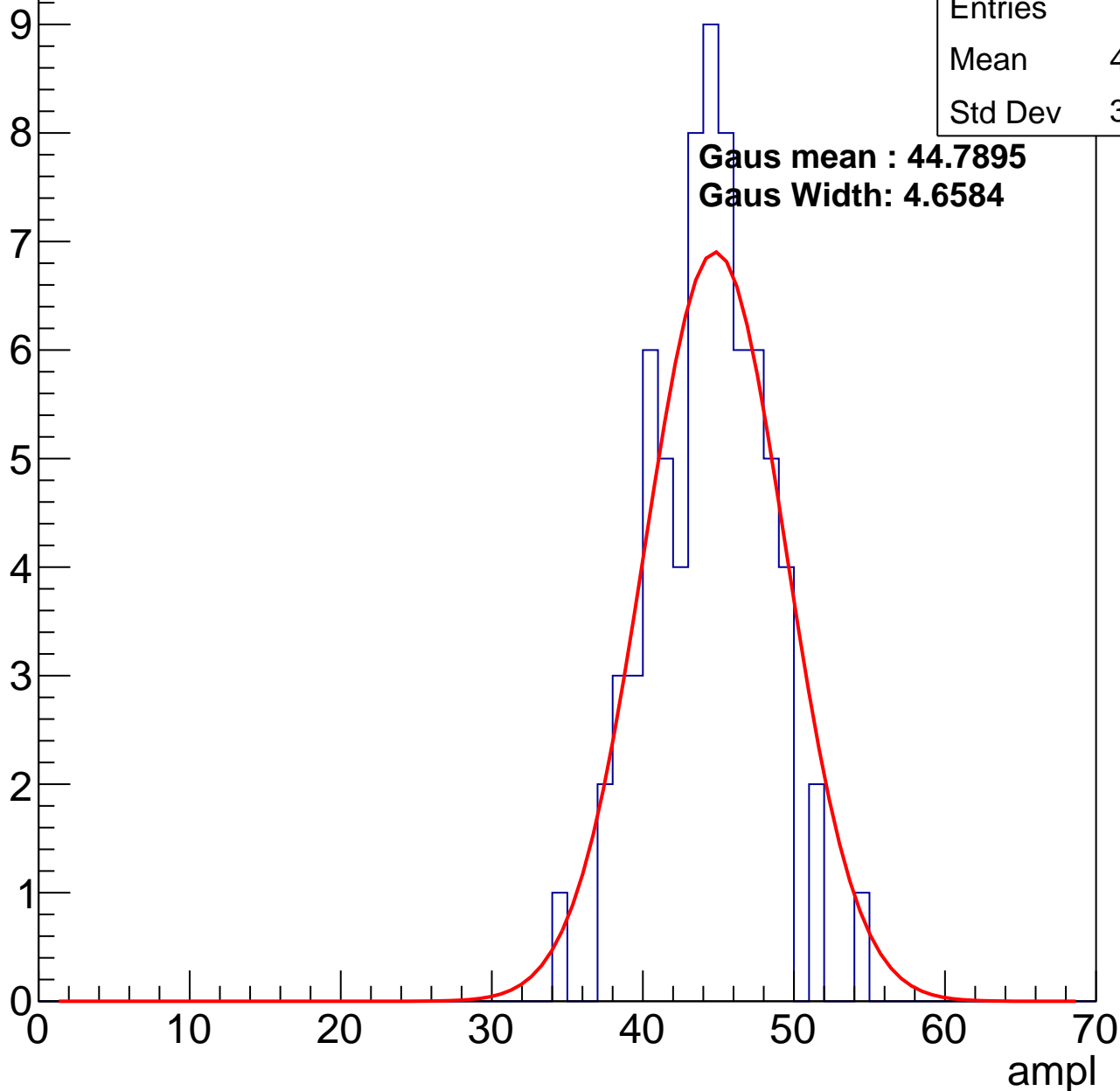
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	43.86
Std Dev	3.717

**Gaus mean : 44.7895**

**Gaus Width: 4.6584**

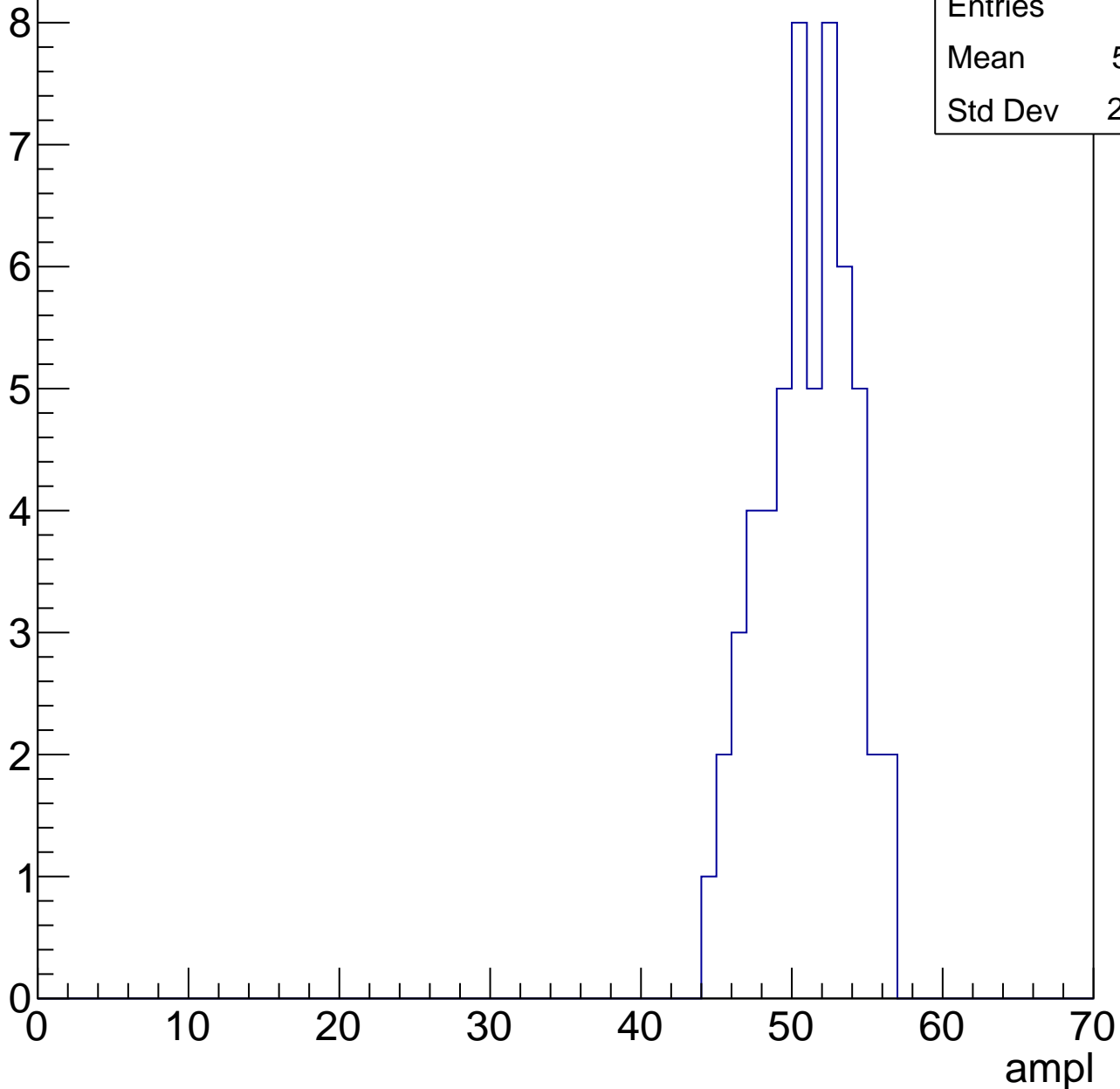


# B1L101S, U9-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

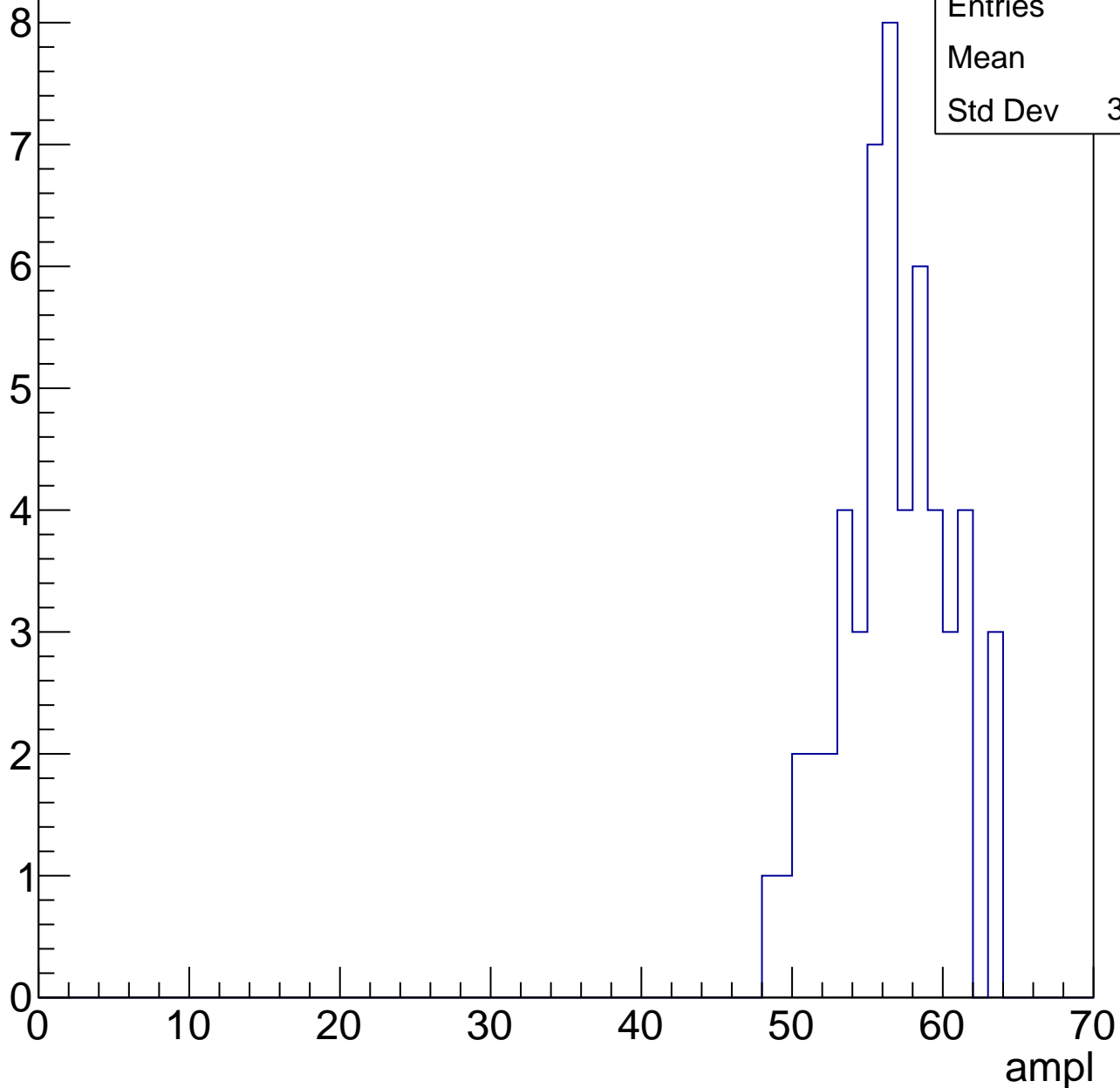
Entries	55
Mean	50.51
Std Dev	2.922



# B1L101S, U9-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



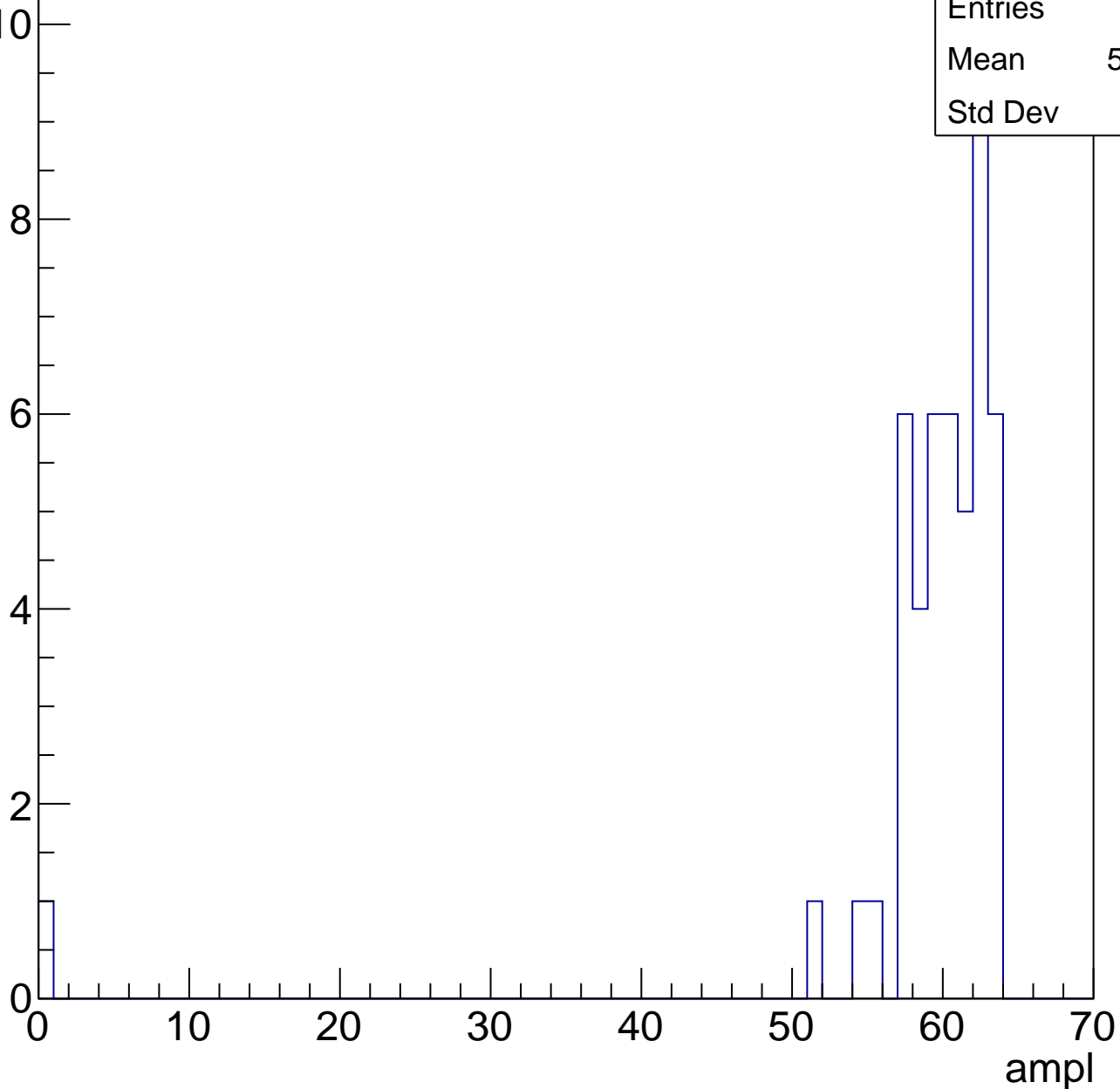
Entries	54
Mean	56.2
Std Dev	3.545

# B1L101S, U9-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

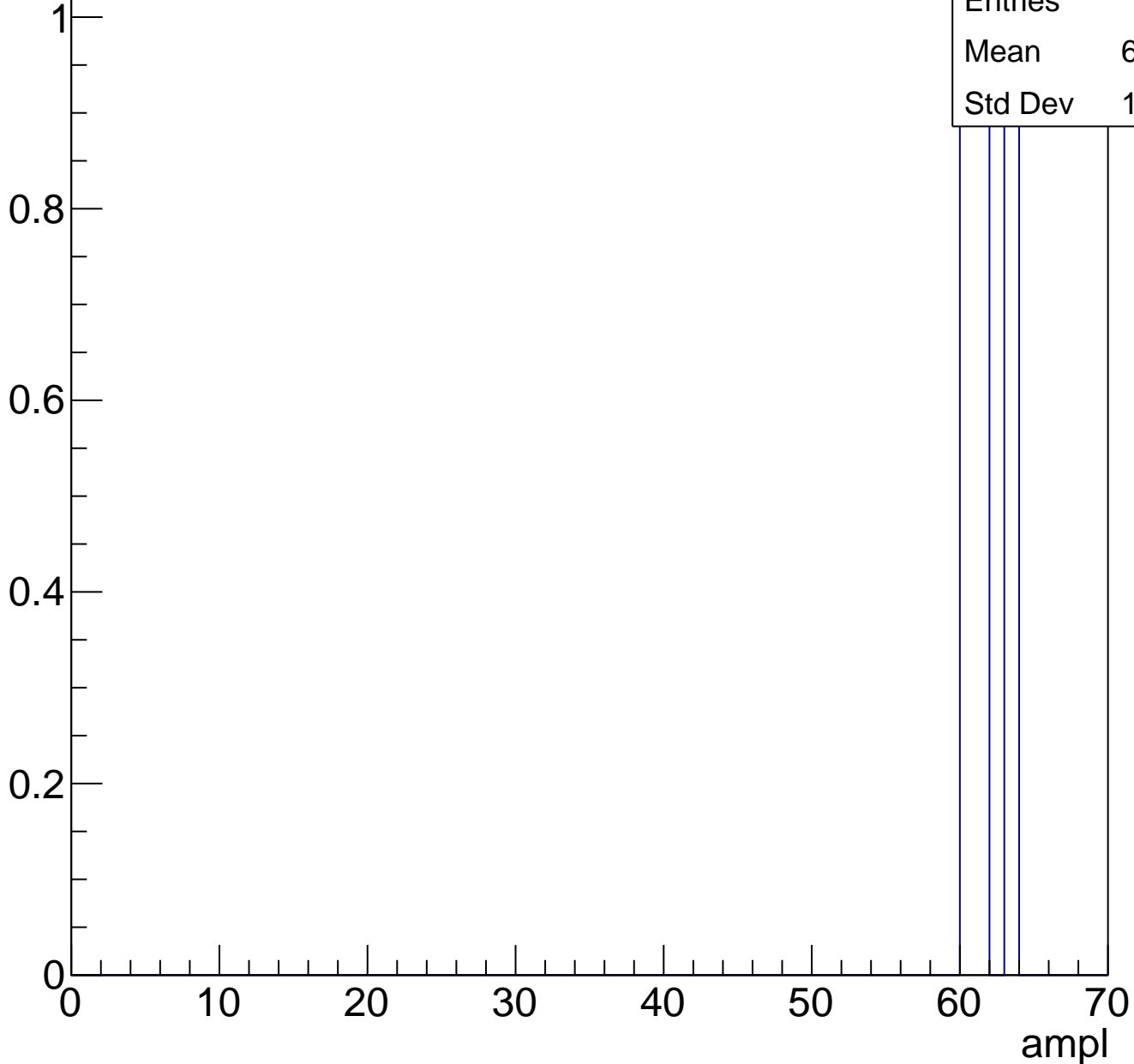
Entries	47
Mean	58.53
Std Dev	9.01



# B1L101S, U9-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch116, adc0

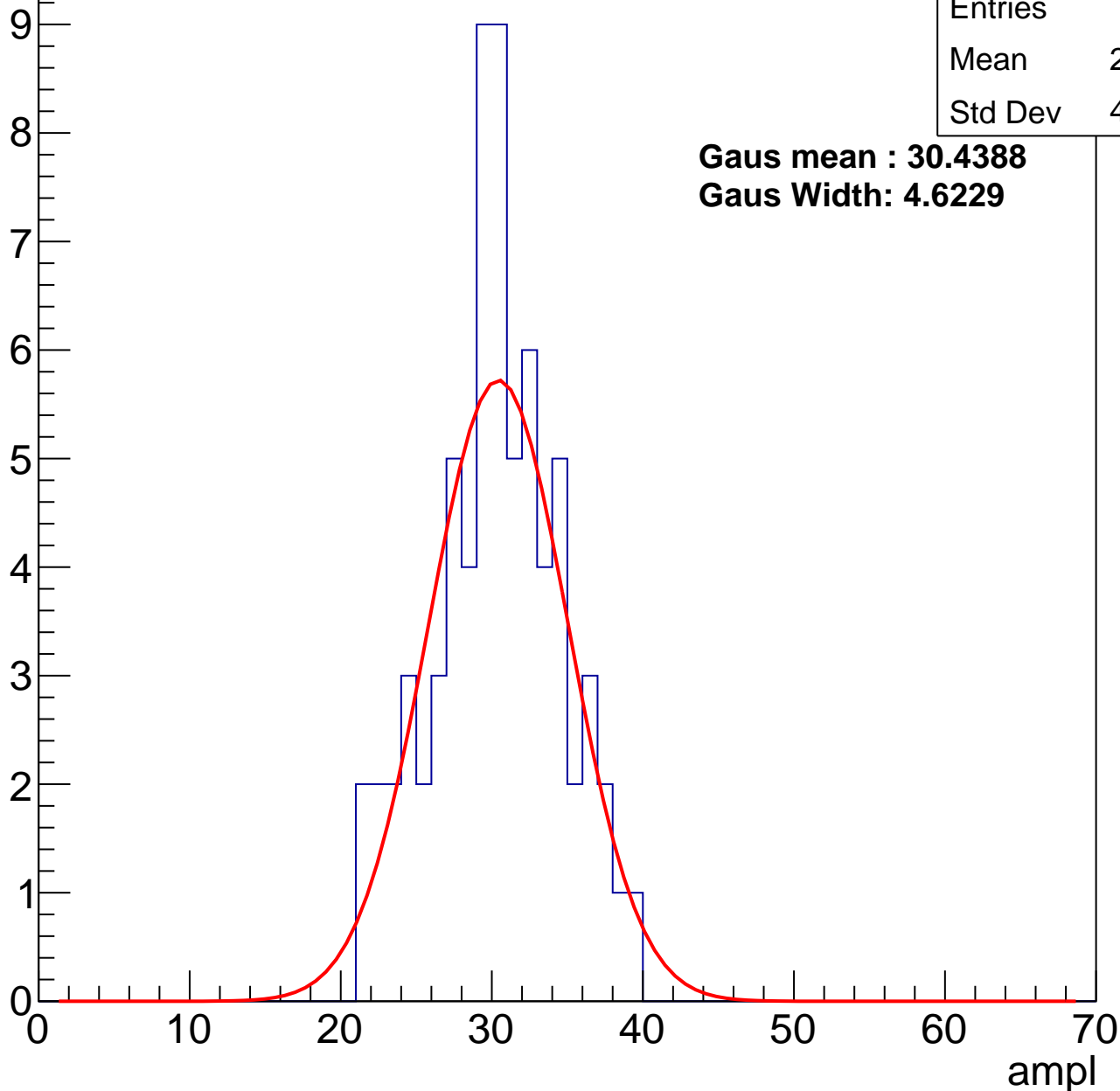
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	29.83
Std Dev	4.154

**Gaus mean : 30.4388**

**Gaus Width: 4.6229**



# B1L101S, U9-ch116, adc1

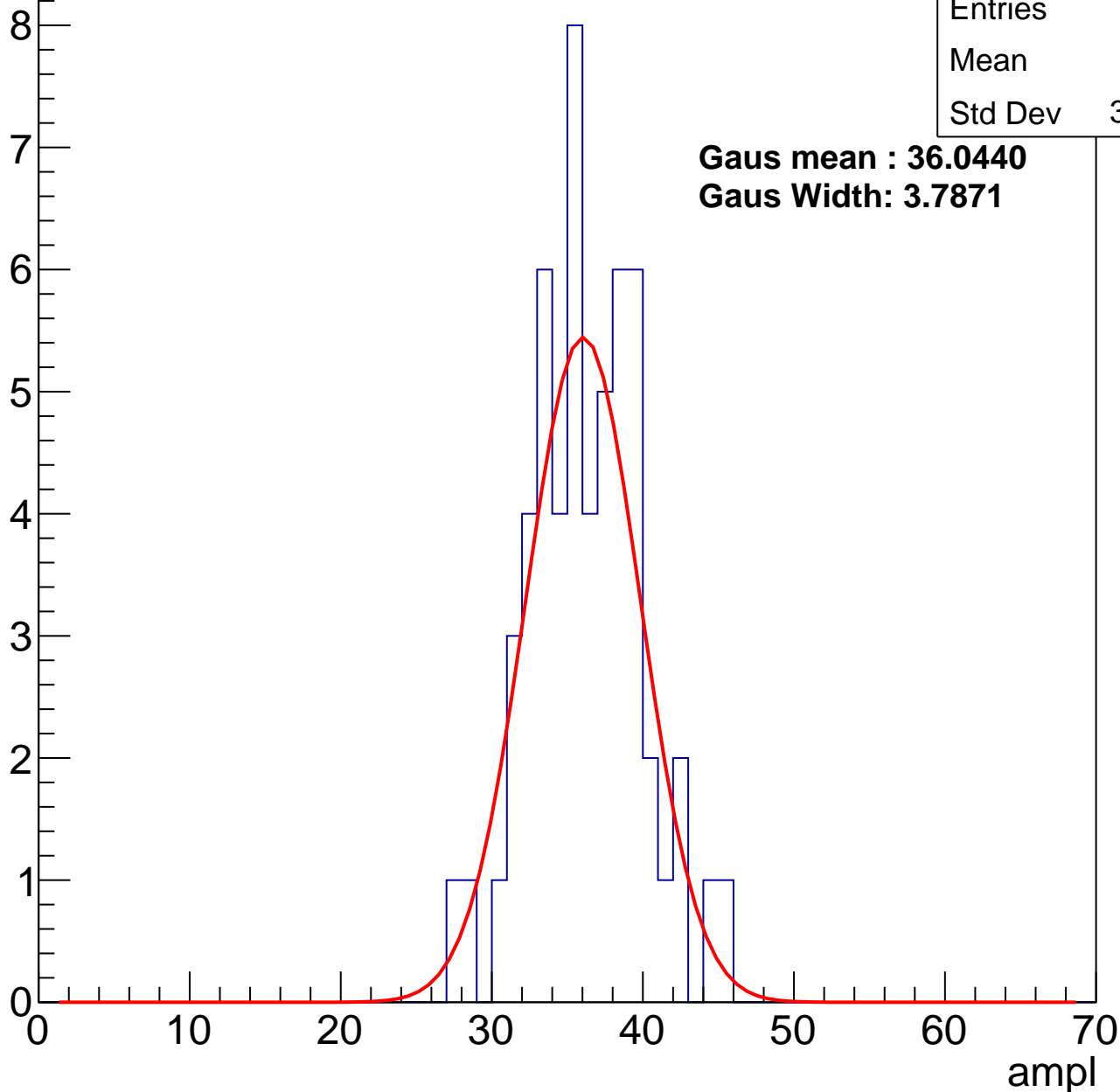
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	35.8
Std Dev	3.667

**Gaus mean : 36.0440**

**Gaus Width: 3.7871**



# B1L101S, U9-ch116, adc2

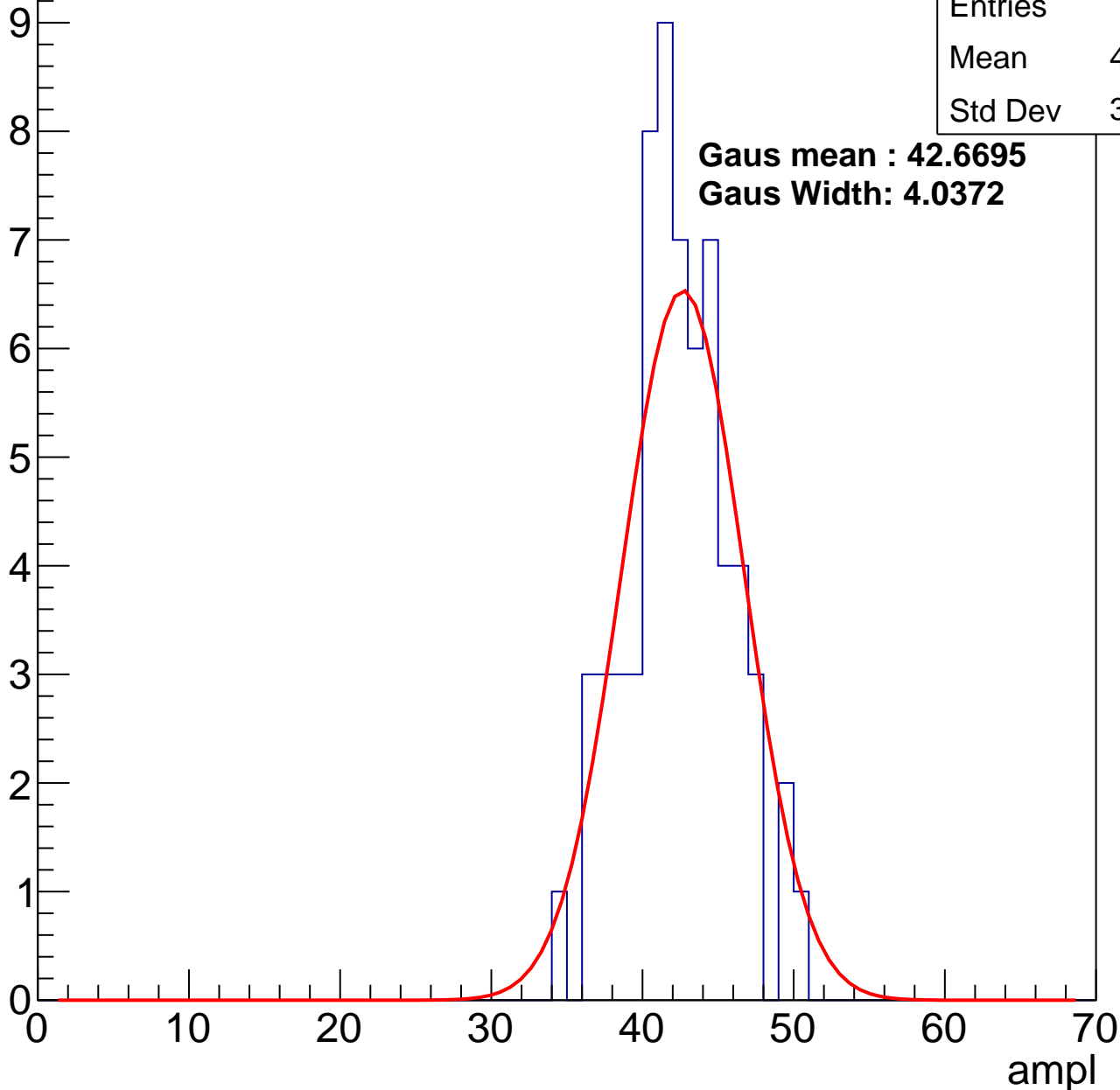
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	41.97
Std Dev	3.386

**Gaus mean : 42.6695**

**Gaus Width: 4.0372**



# B1L101S, U9-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

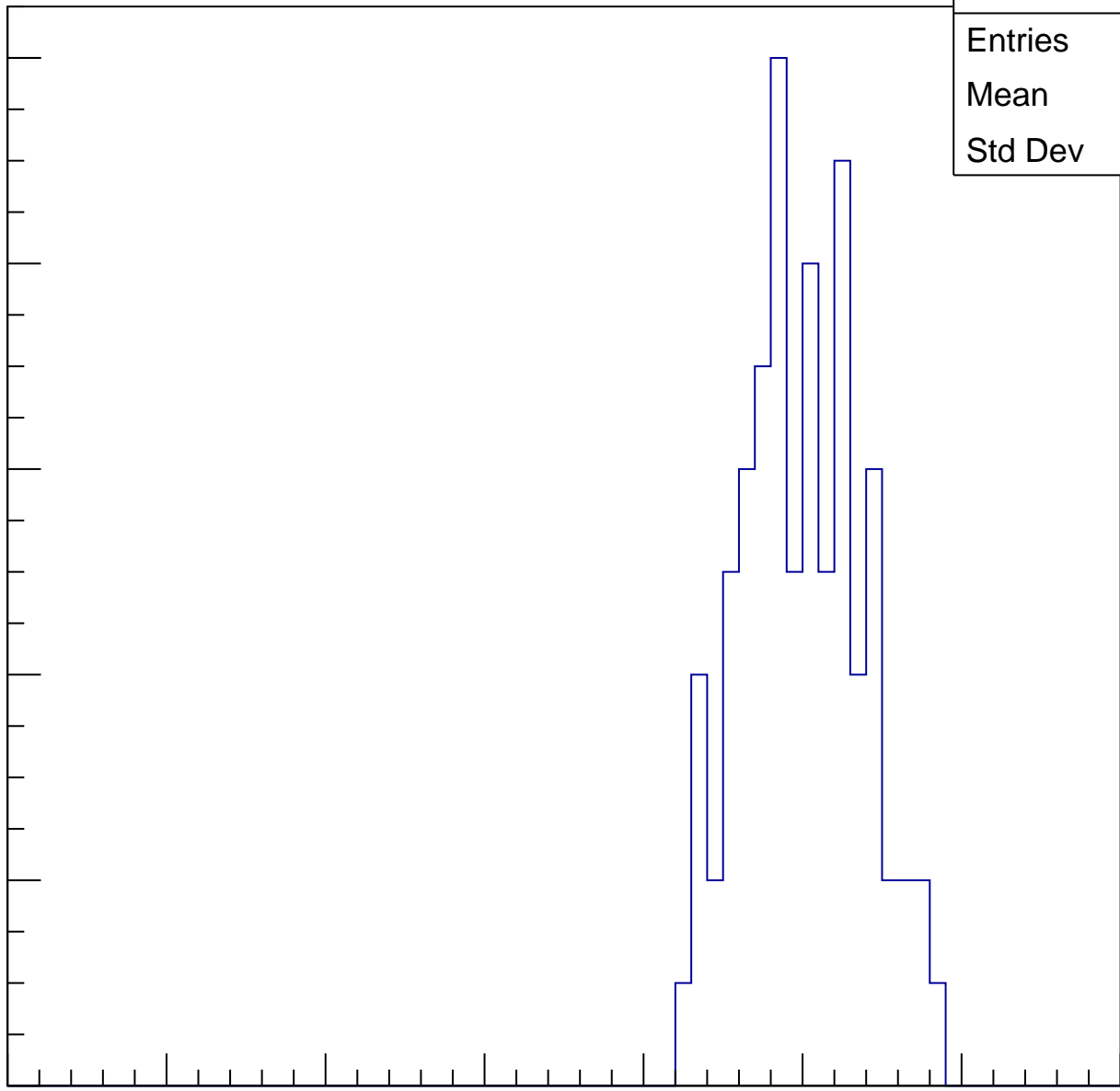
Entries	79
Mean	49.49
Std Dev	3.728

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

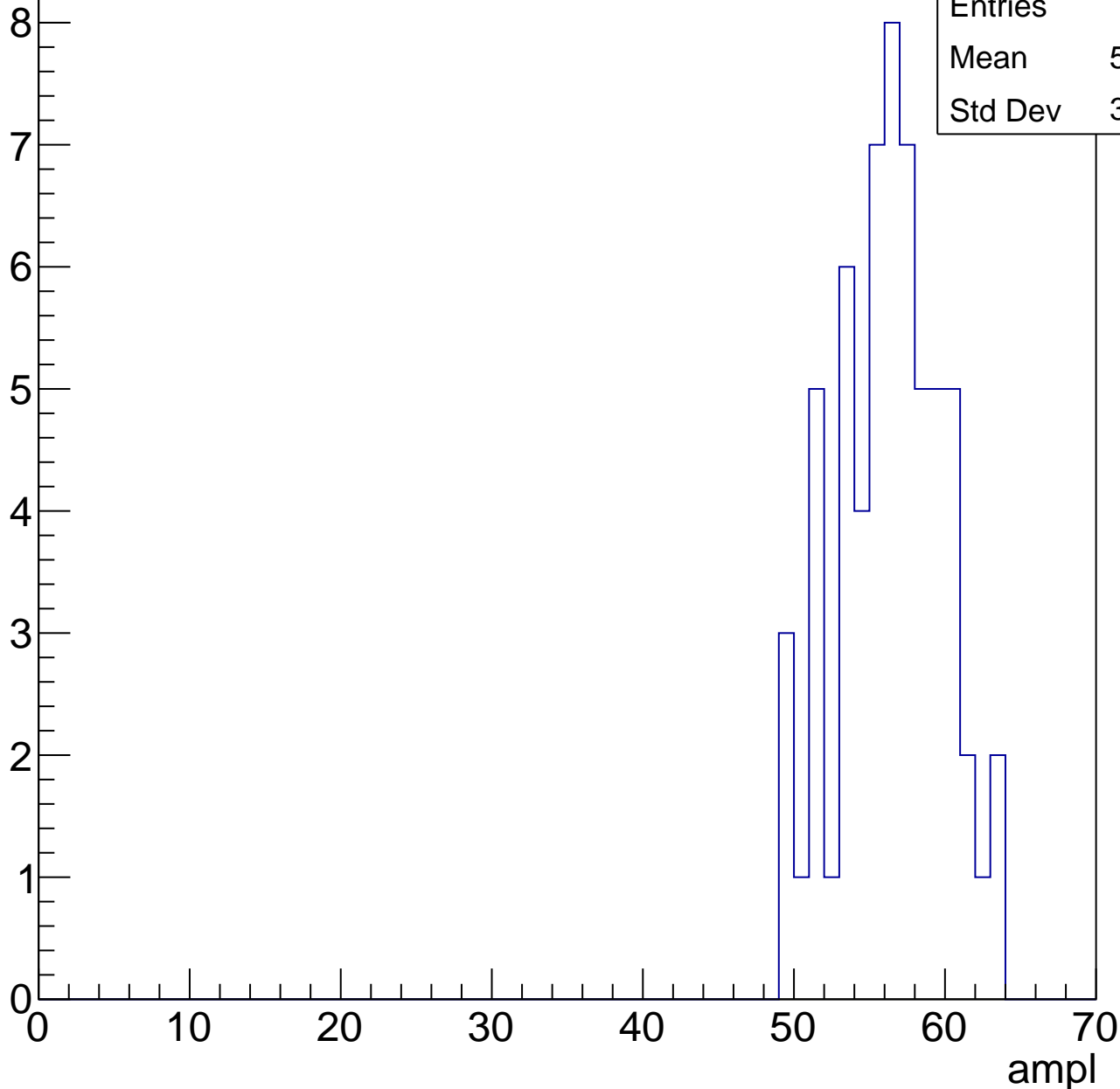


# B1L101S, U9-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	55.89
Std Dev	3.446

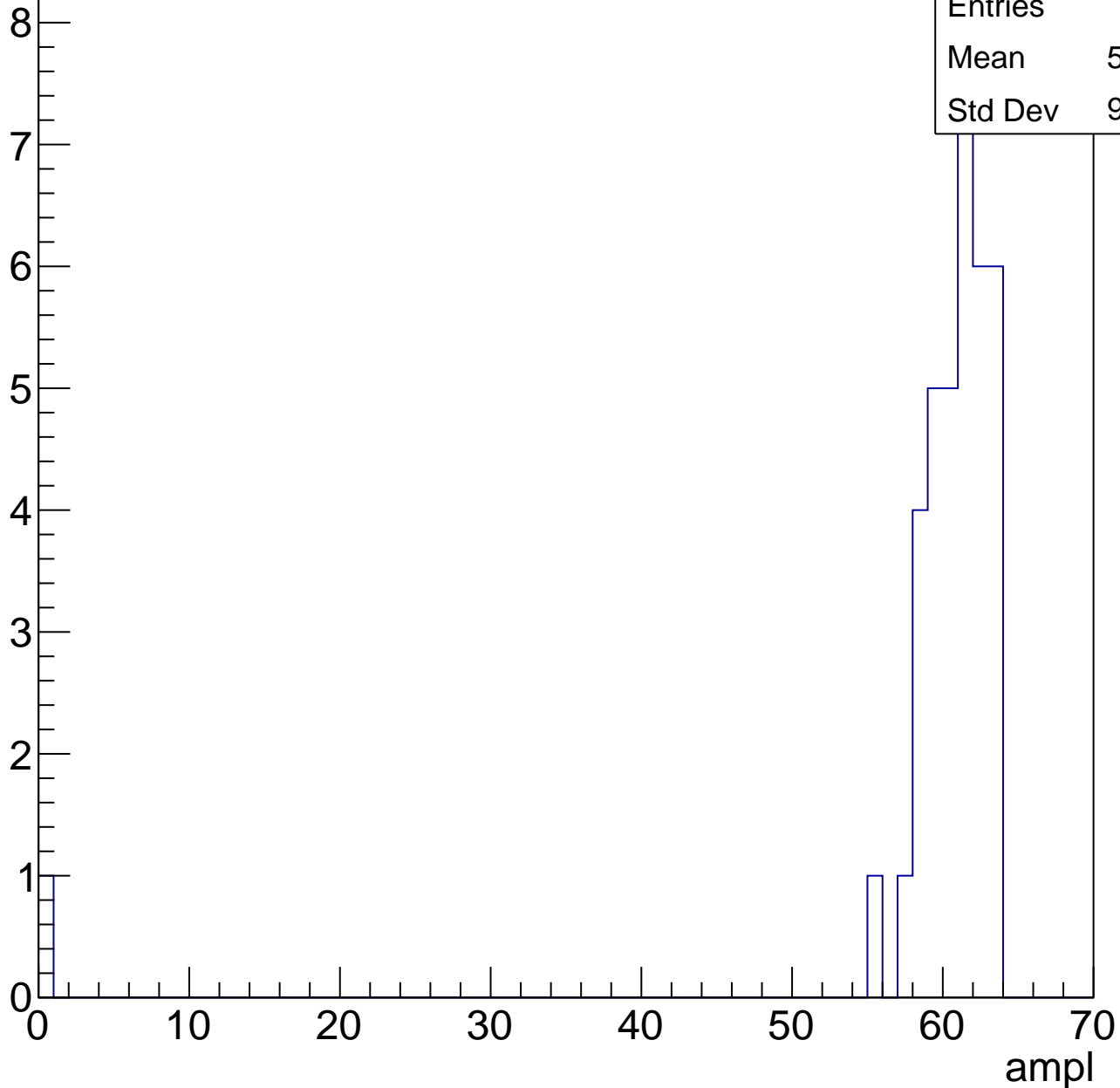


# B1L101S, U9-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	37
Mean	58.84
Std Dev	9.988



# B1L101S, U9-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U9-ch117, adc0

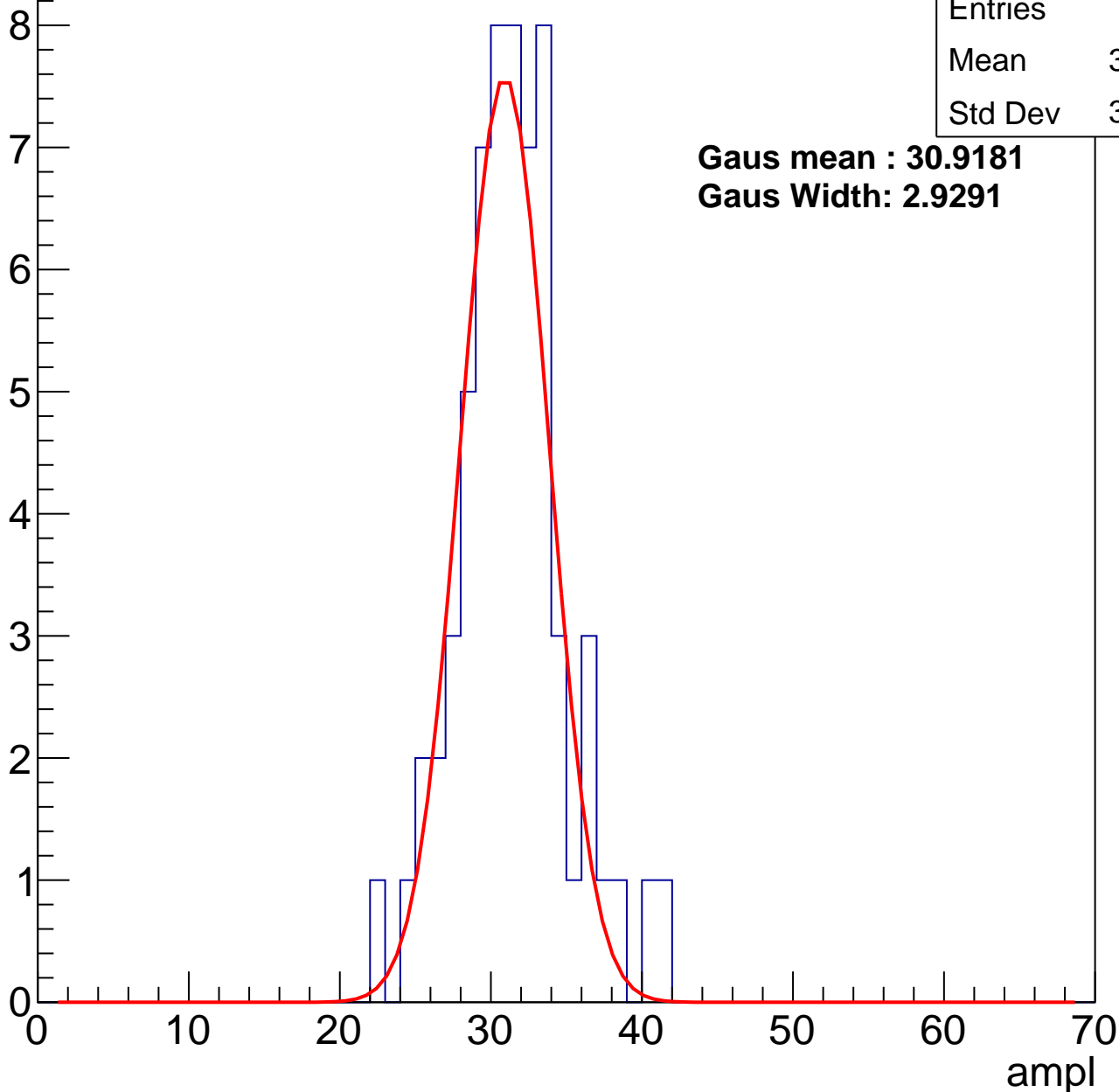
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	30.94
Std Dev	3.572

**Gaus mean : 30.9181**

**Gaus Width: 2.9291**



# B1L101S, U9-ch117, adc1

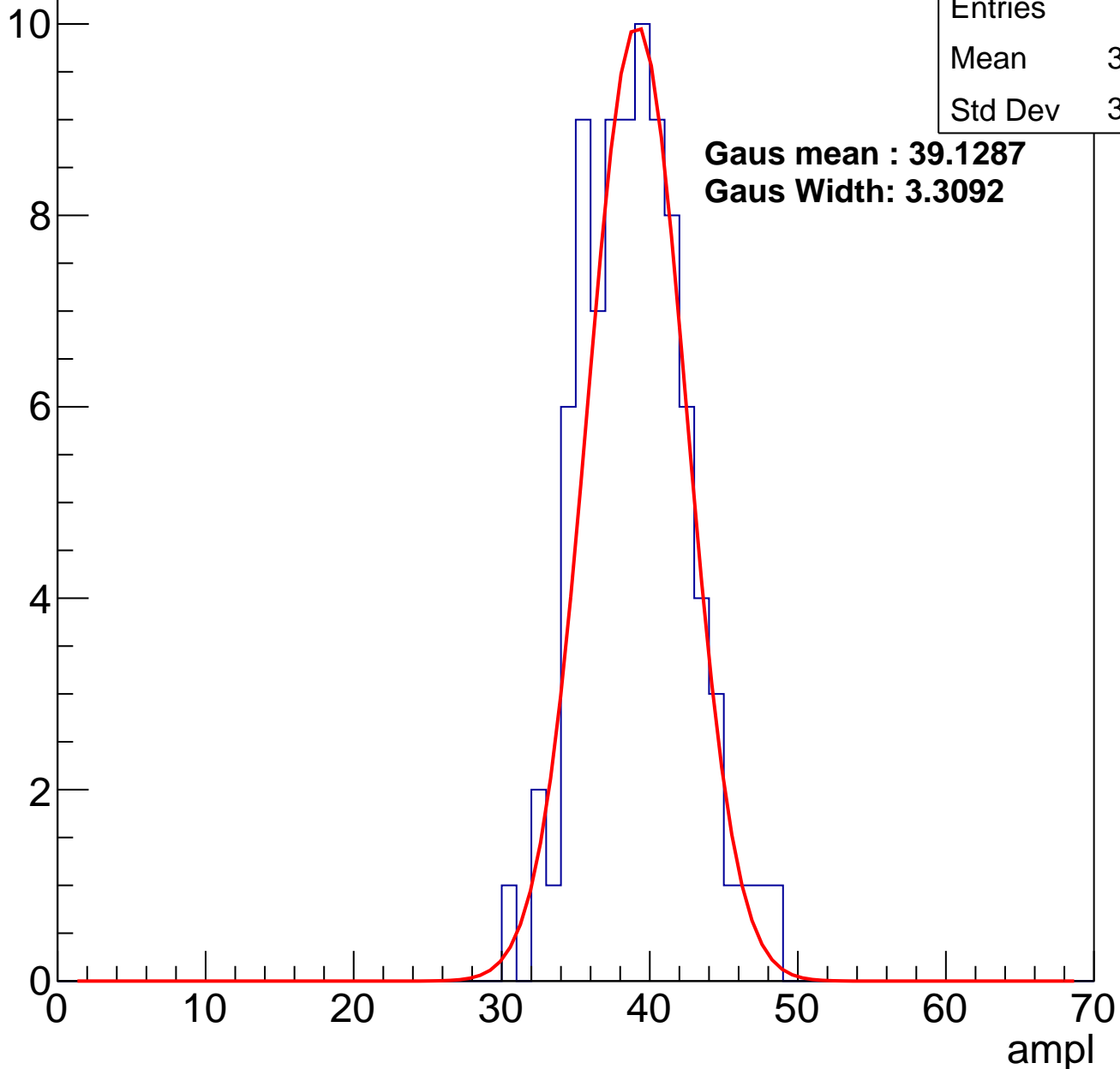
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	88
Mean	38.56
Std Dev	3.477

**Gaus mean : 39.1287**

**Gaus Width: 3.3092**

Entry



# B1L101S, U9-ch117, adc2

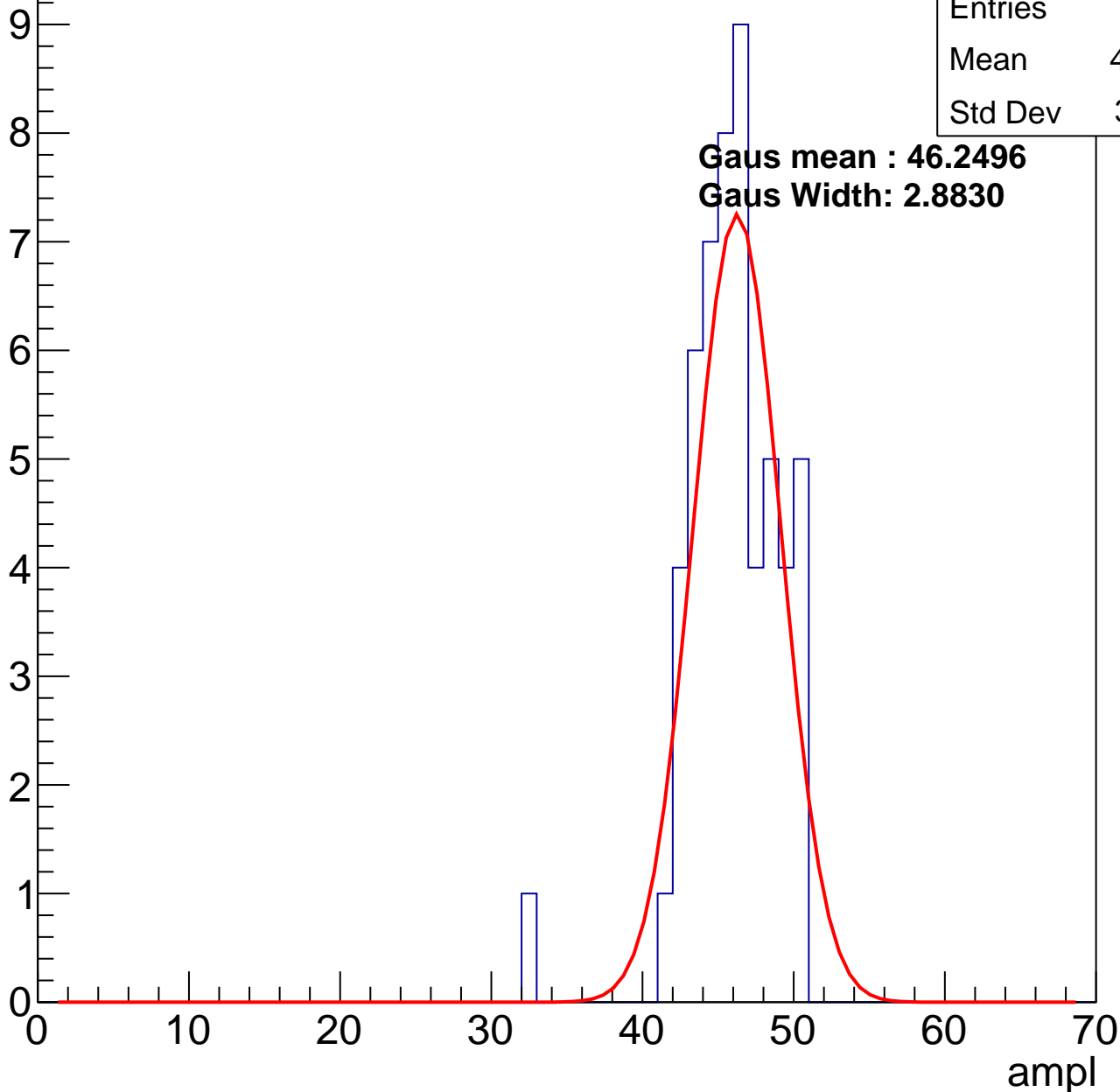
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	45.46
Std Dev	3.041

**Gaus mean : 46.2496**

**Gaus Width: 2.8830**

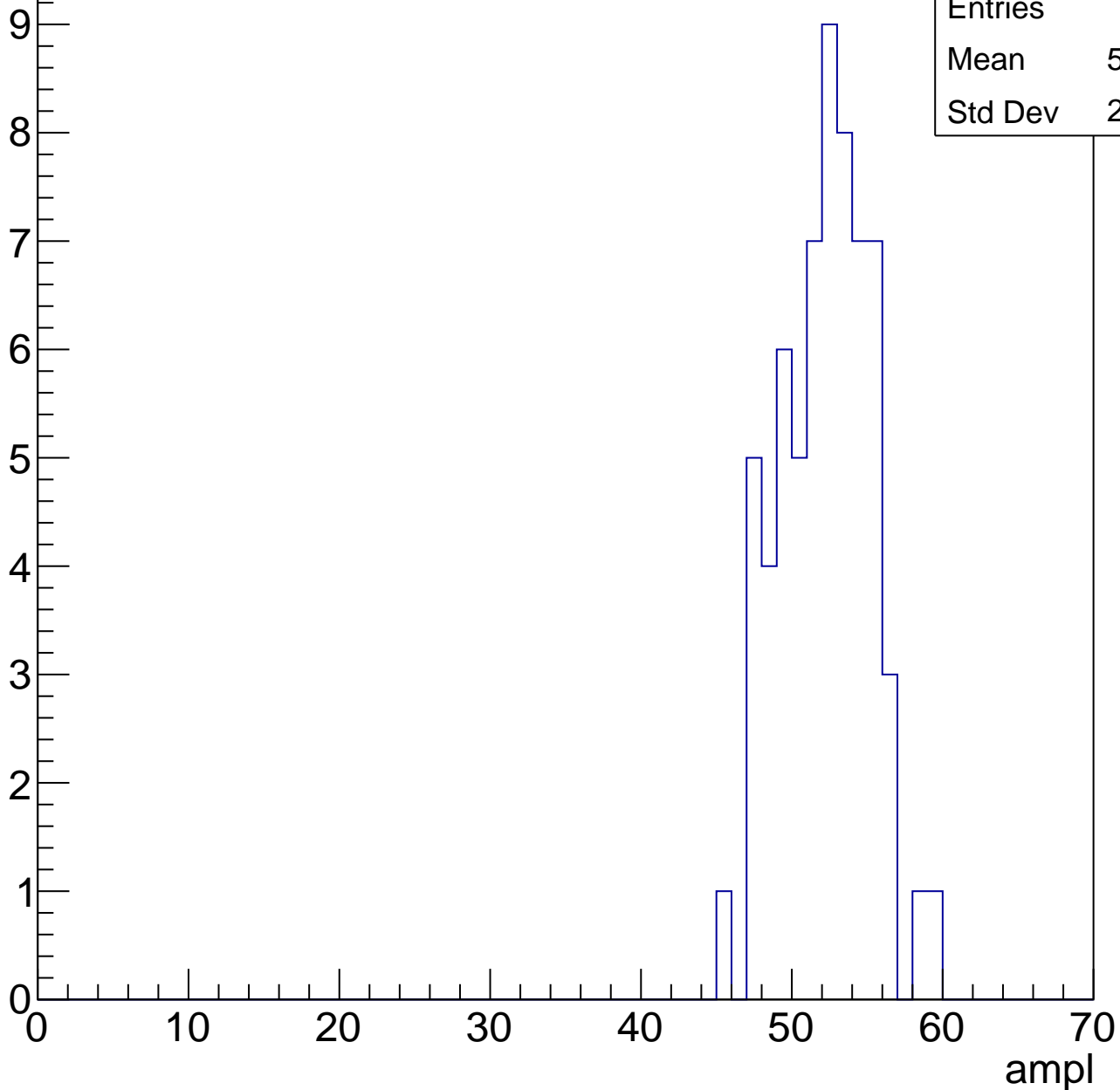


# B1L101S, U9-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	51.77
Std Dev	2.925

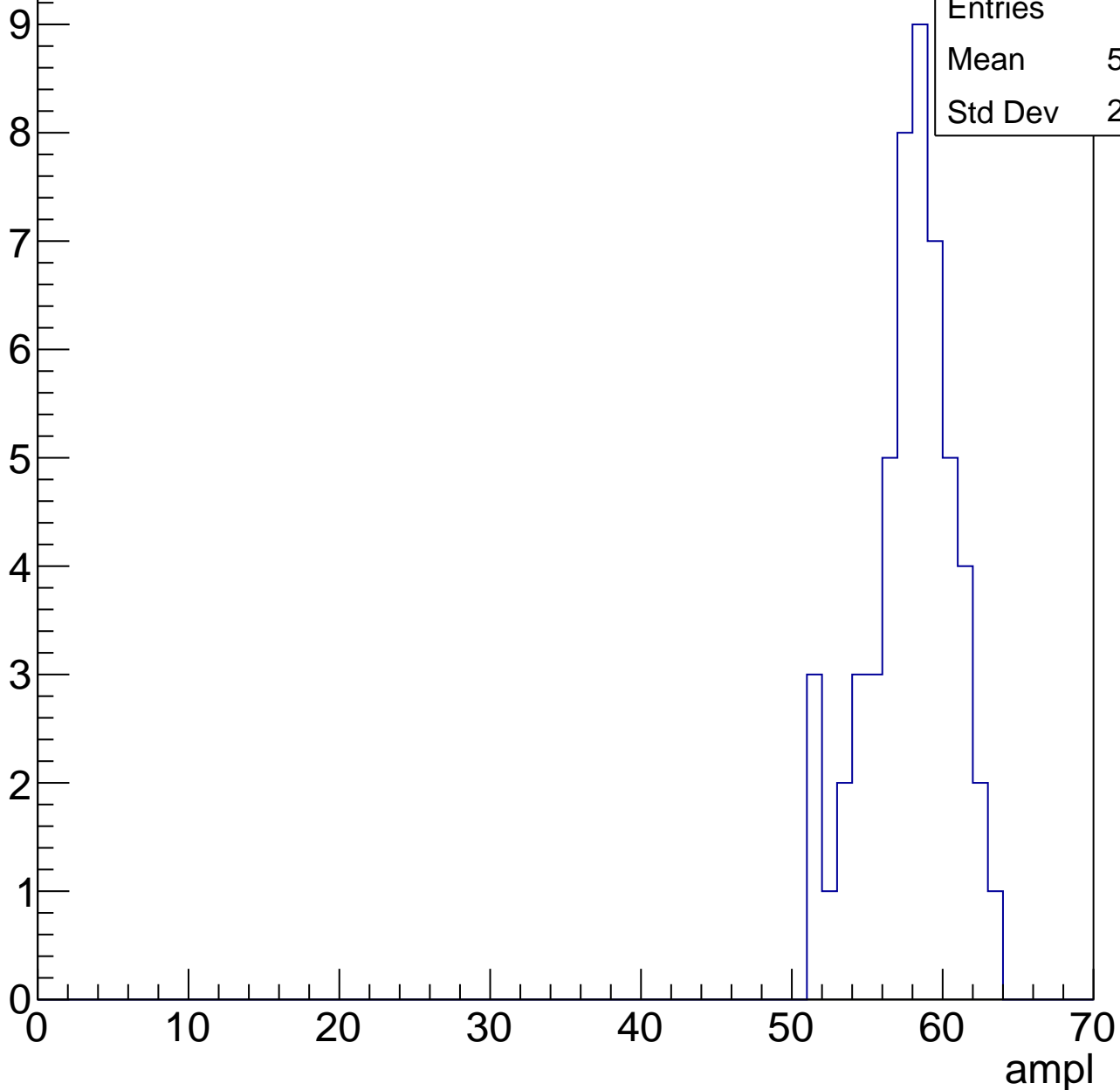


# B1L101S, U9-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	57.36
Std Dev	2.862

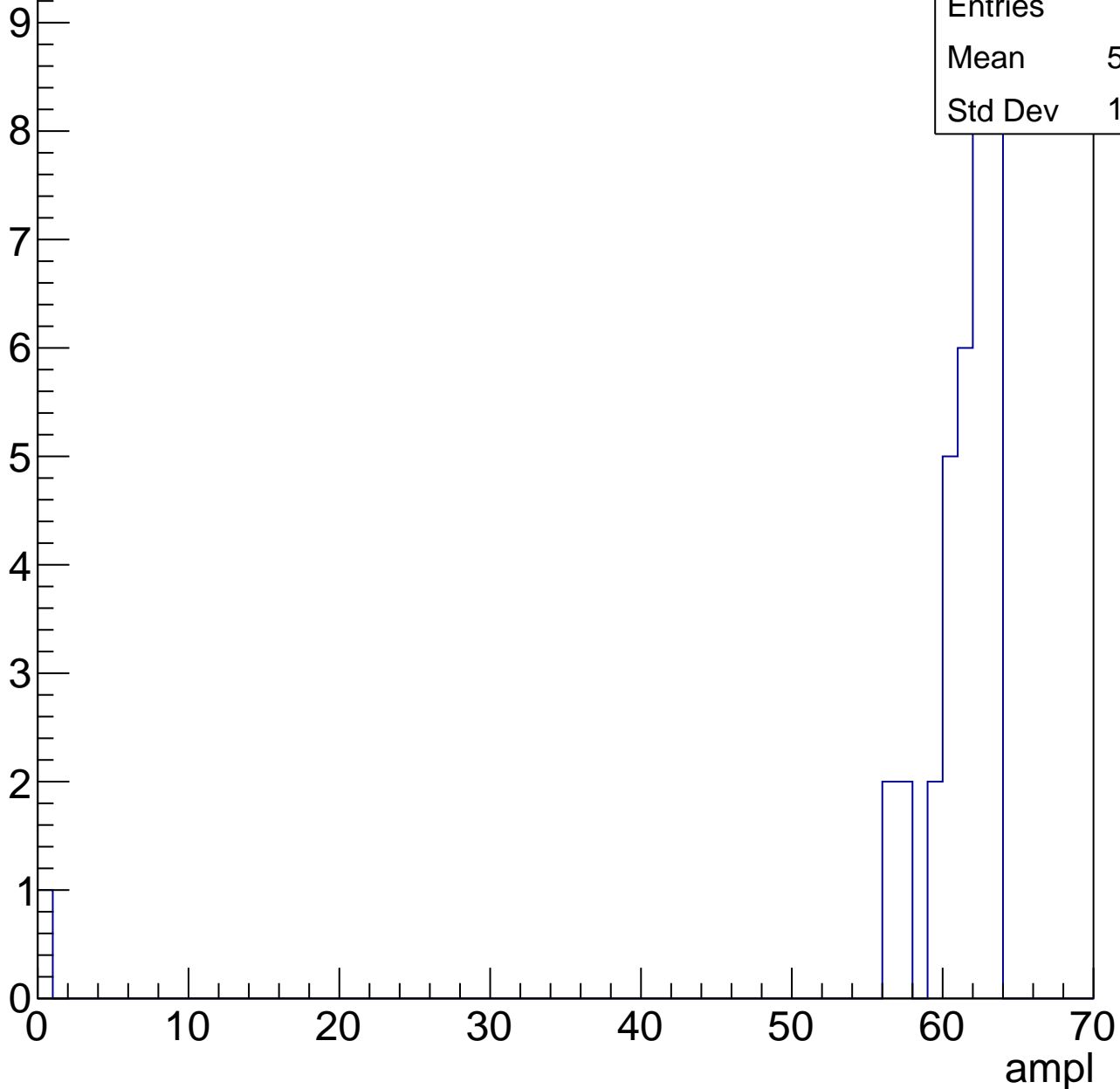


# B1L101S, U9-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

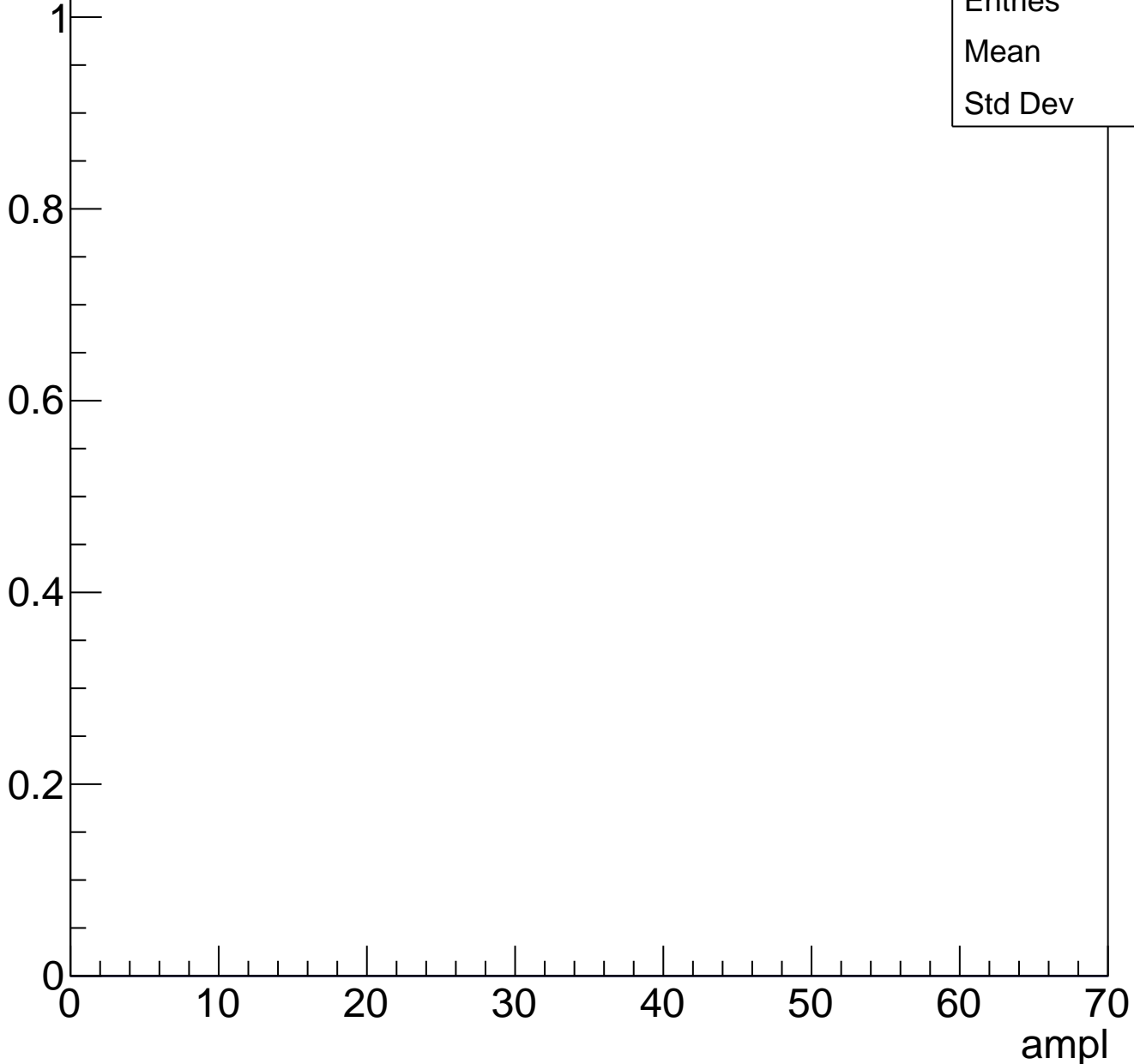
Entries	35
Mean	59.23
Std Dev	10.35



# B1L101S, U9-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L101S, U9-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch118, adc0

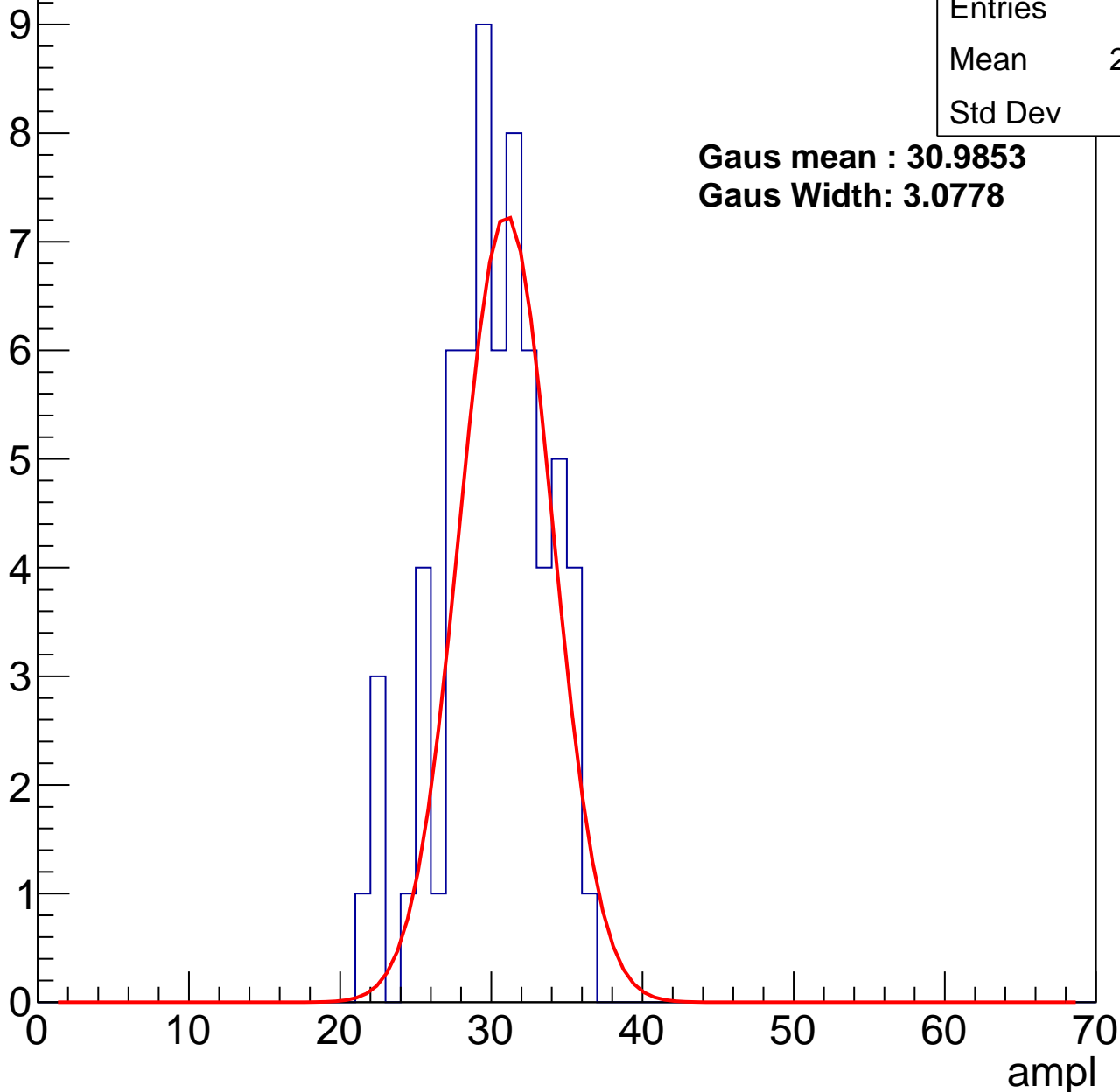
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	29.63
Std Dev	3.48

**Gaus mean : 30.9853**

**Gaus Width: 3.0778**



# B1L101S, U9-ch118, adc1

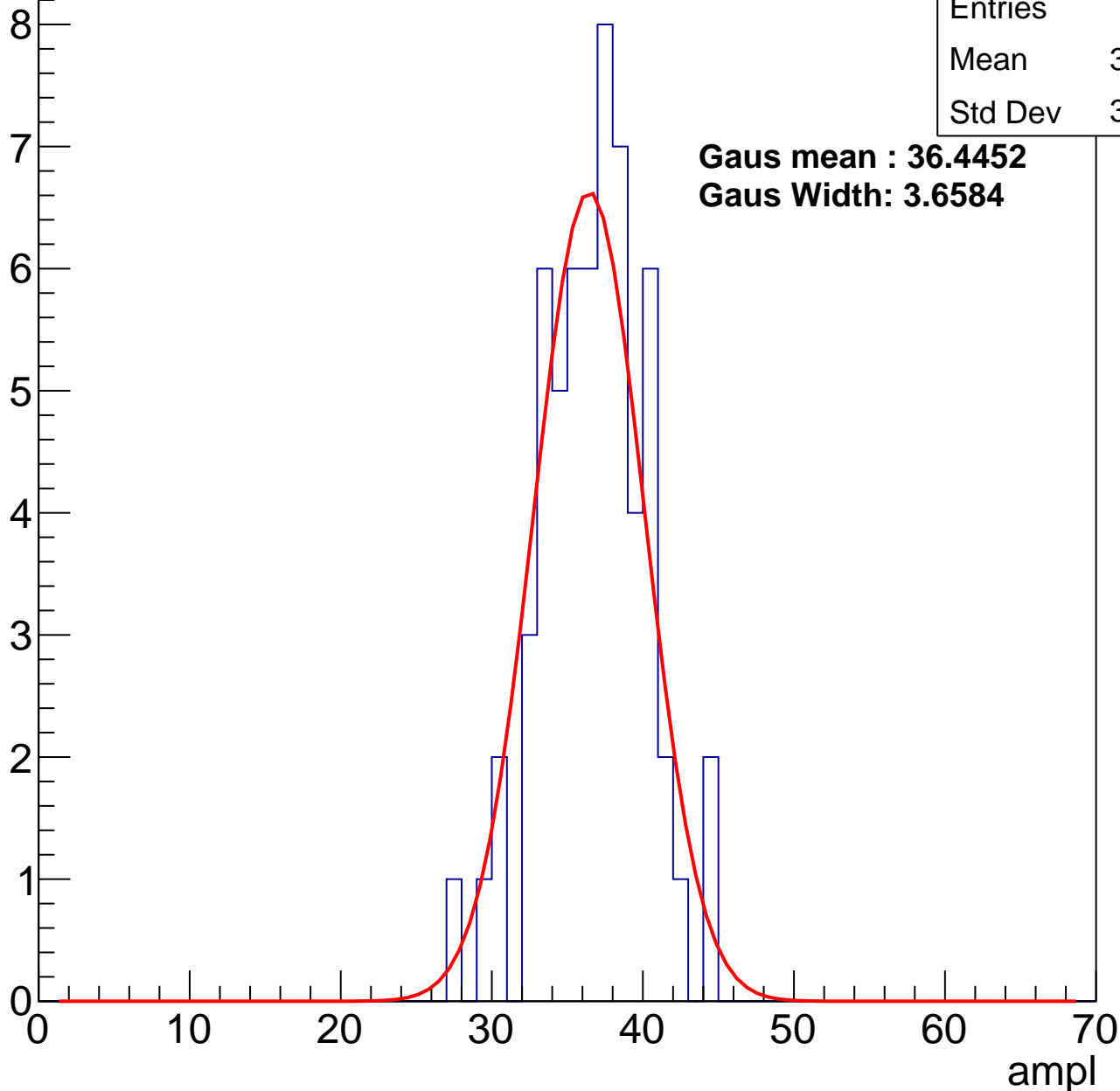
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	36.27
Std Dev	3.434

**Gaus mean : 36.4452**

**Gaus Width: 3.6584**



# B1L101S, U9-ch118, adc2

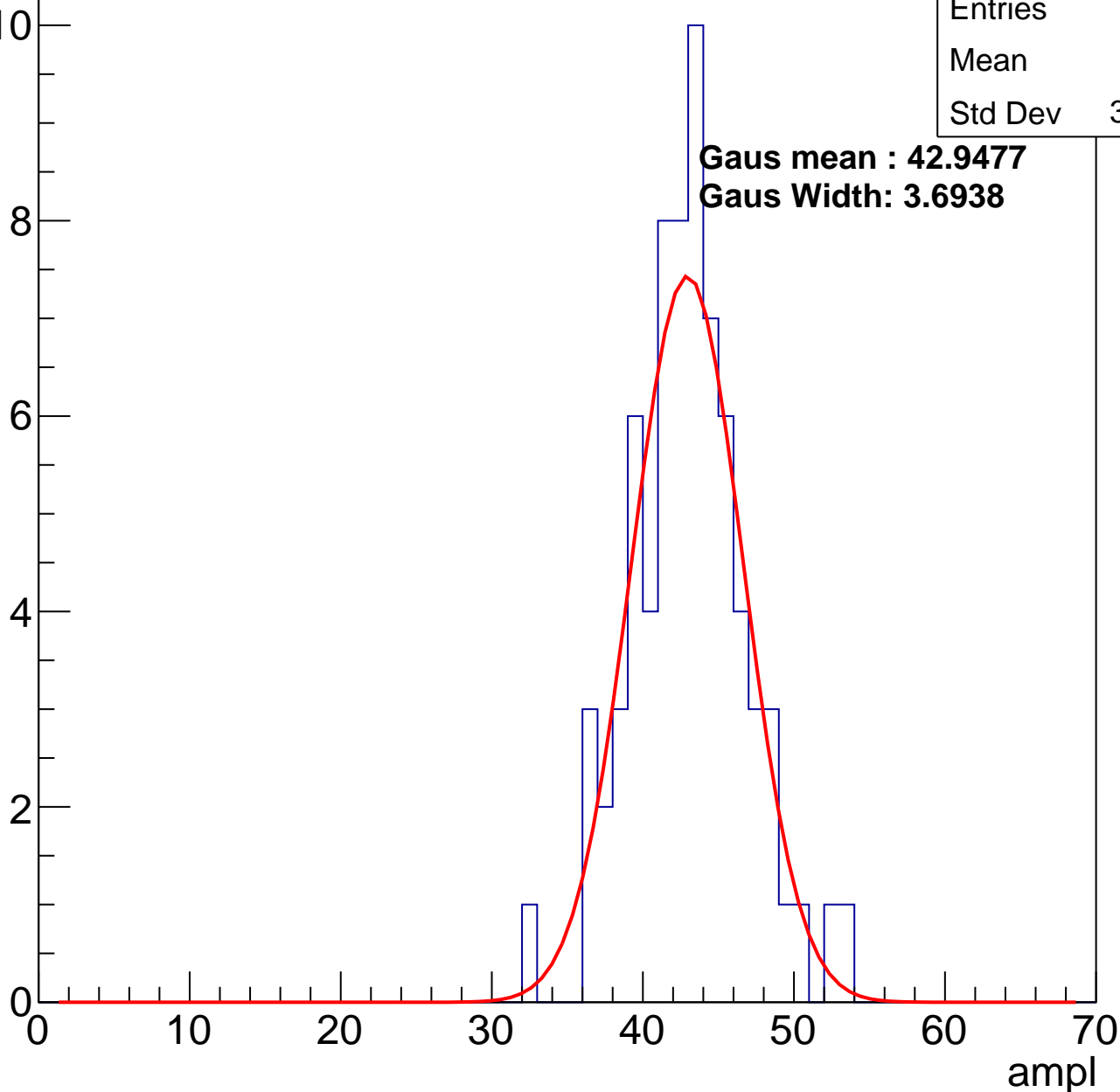
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	42.6
Std Dev	3.785

**Gaus mean : 42.9477**

**Gaus Width: 3.6938**

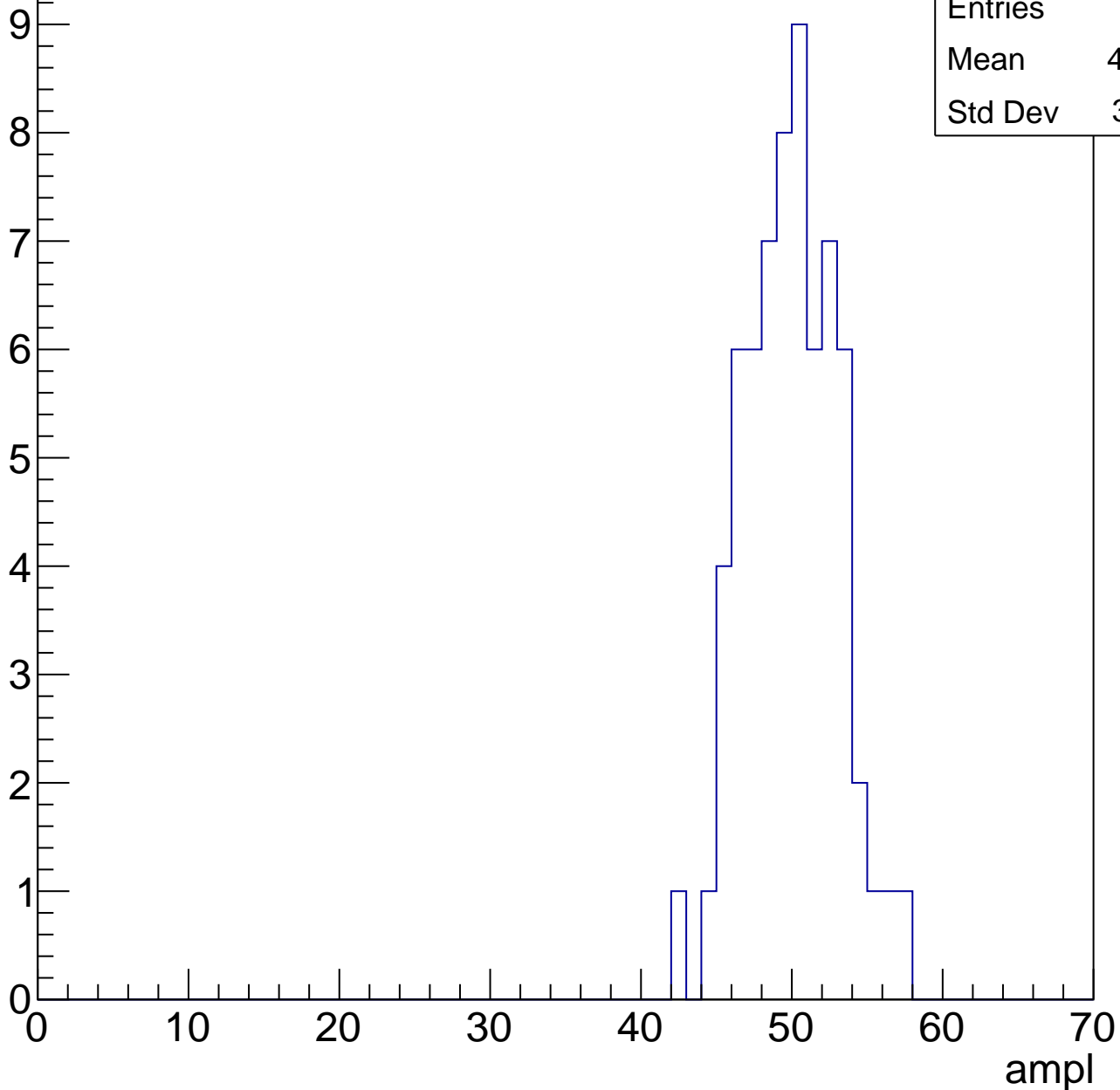


# B1L101S, U9-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	49.48
Std Dev	3.011

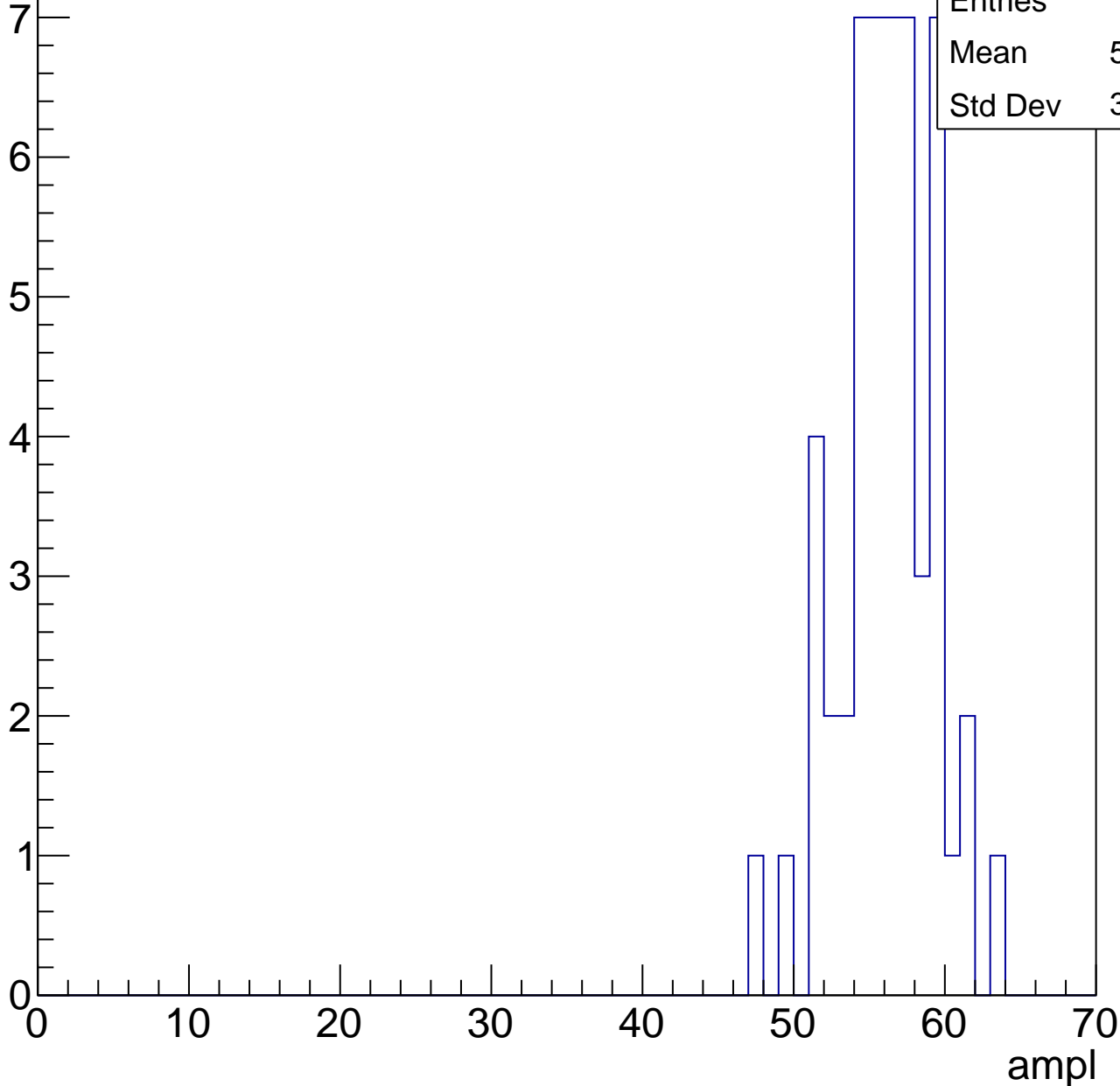


# B1L101S, U9-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

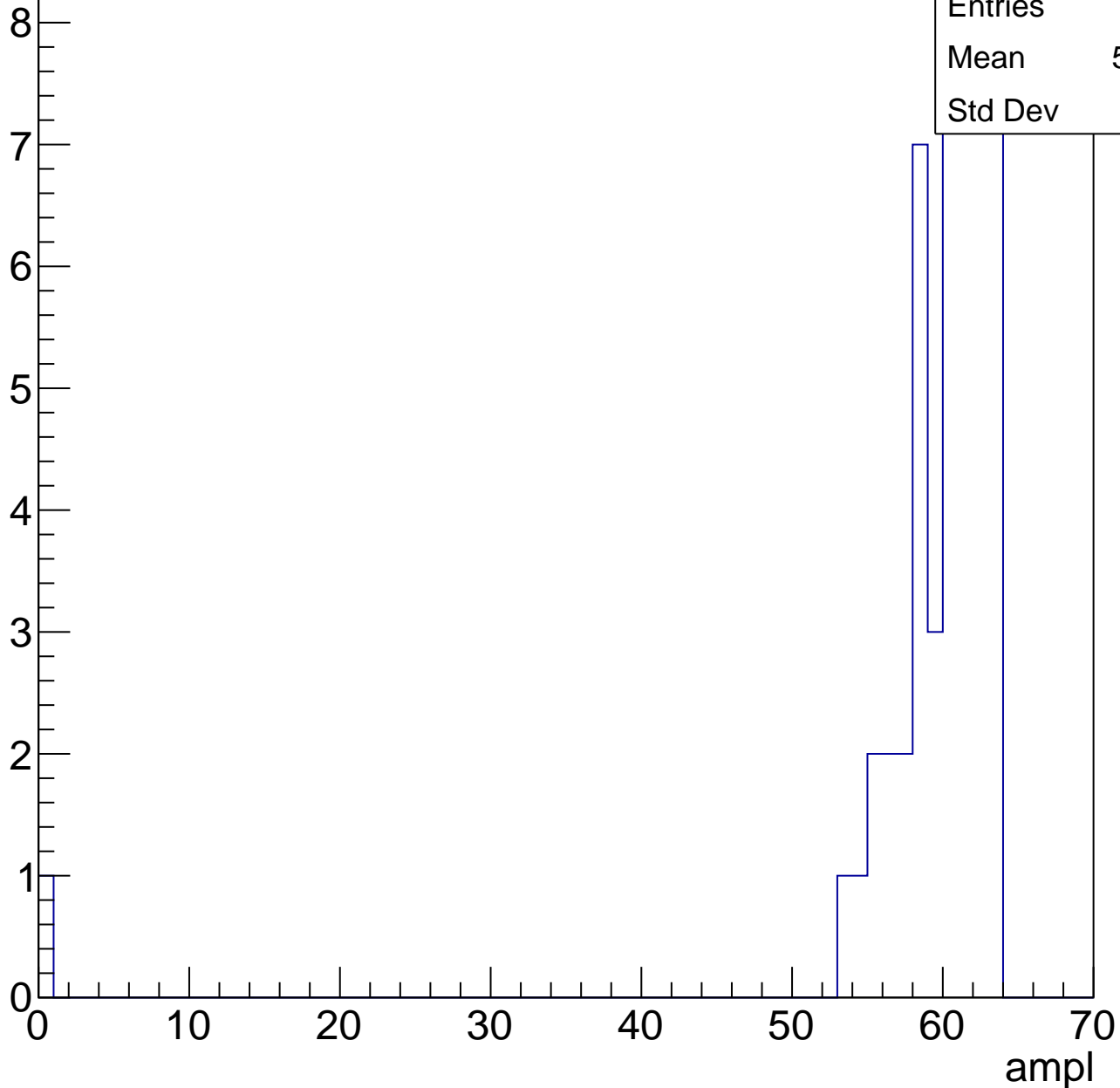
Entries	52
Mean	55.69
Std Dev	3.123



# B1L101S, U9-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	61.75
Std Dev	1.09

ampl

0 10 20 30 40 50 60 70



# B1L101S, U9-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	10.5
Std Dev	10.5

# B1L101S, U9-ch119, adc0

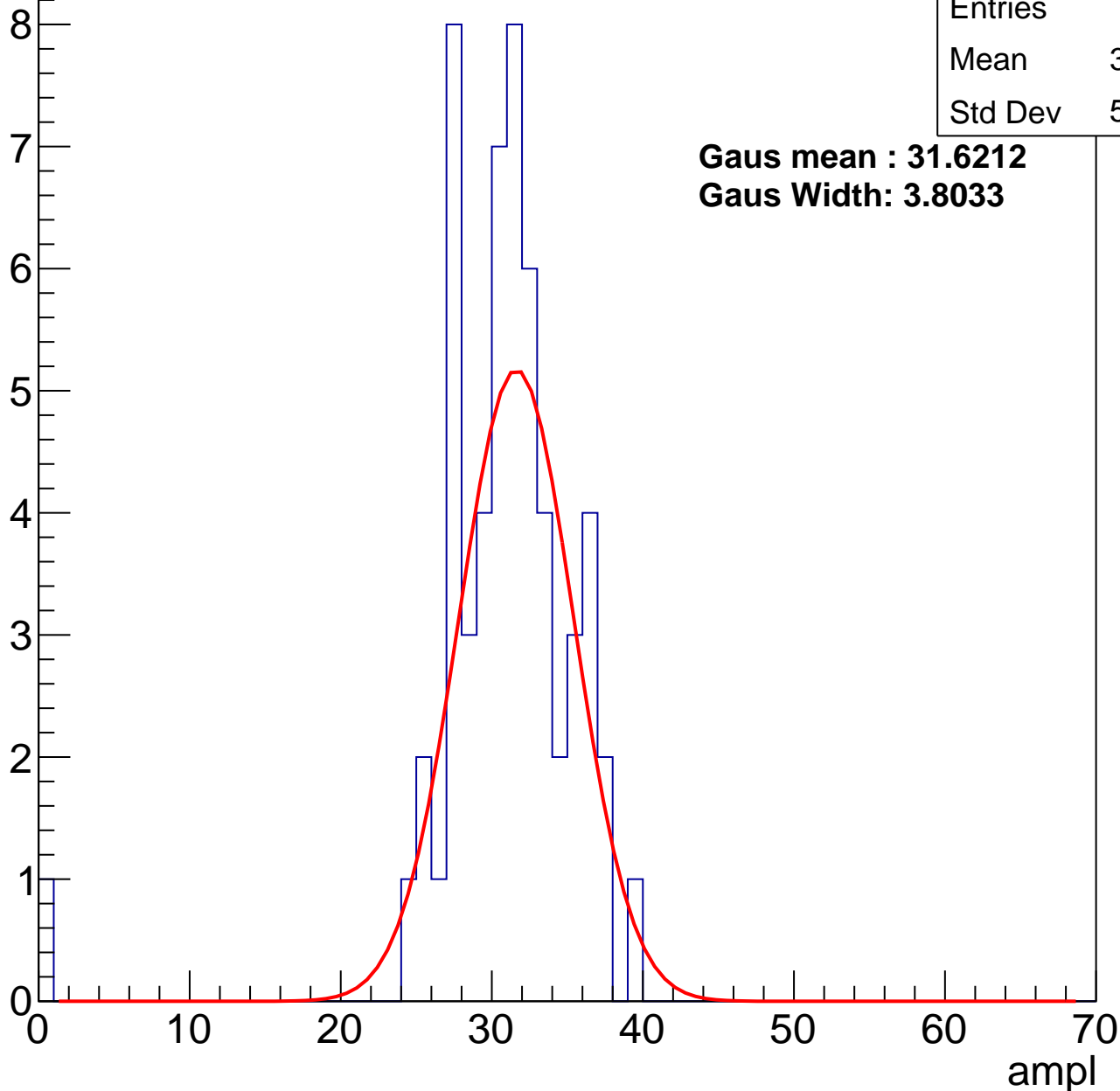
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	30.32
Std Dev	5.269

**Gaus mean : 31.6212**

**Gaus Width: 3.8033**



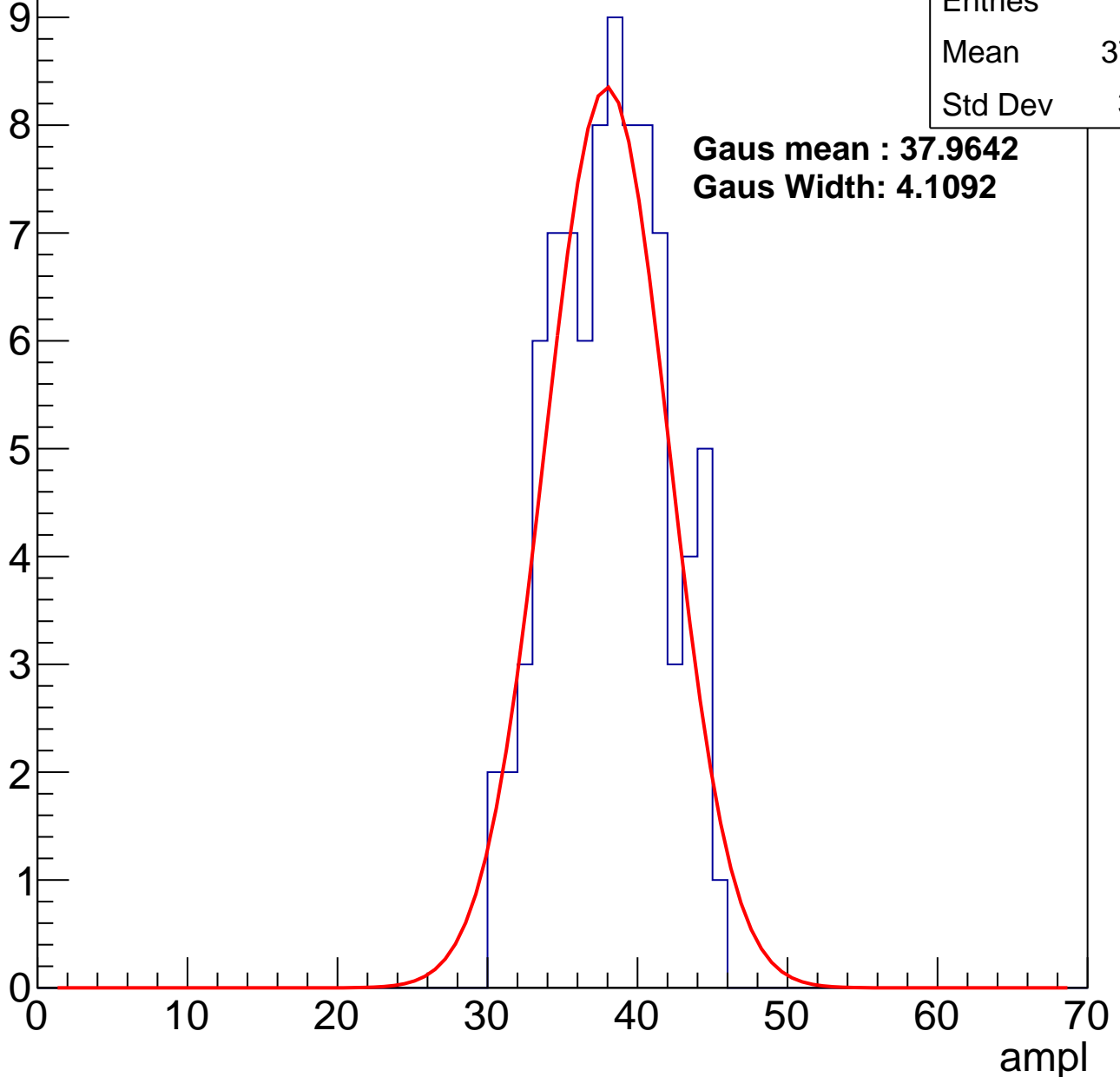
# B1L101S, U9-ch119, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	86
Mean	37.62
Std Dev	3.67

**Gaus mean : 37.9642**  
**Gaus Width: 4.1092**



# B1L101S, U9-ch119, adc2

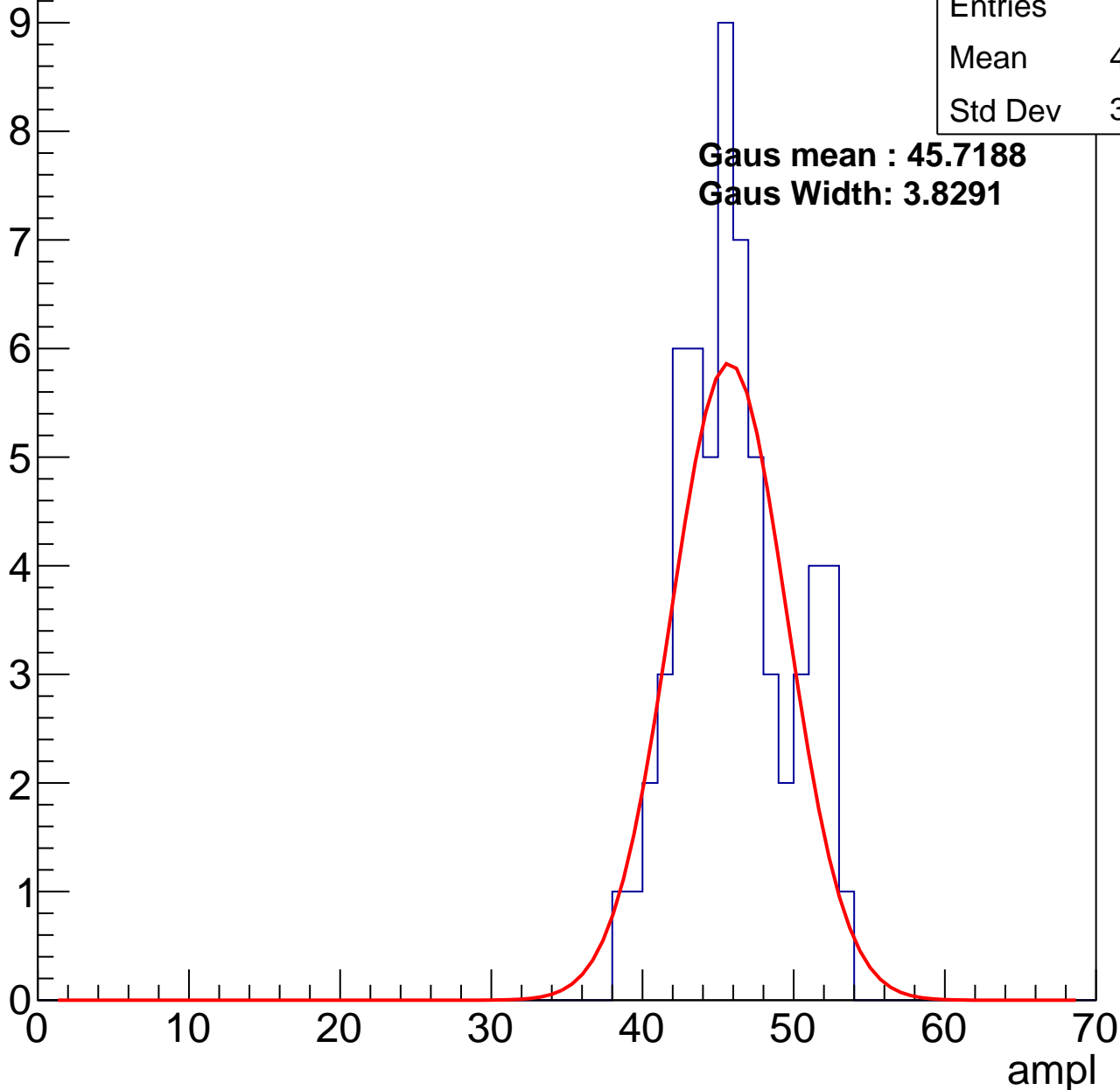
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	45.63
Std Dev	3.607

**Gaus mean : 45.7188**

**Gaus Width: 3.8291**

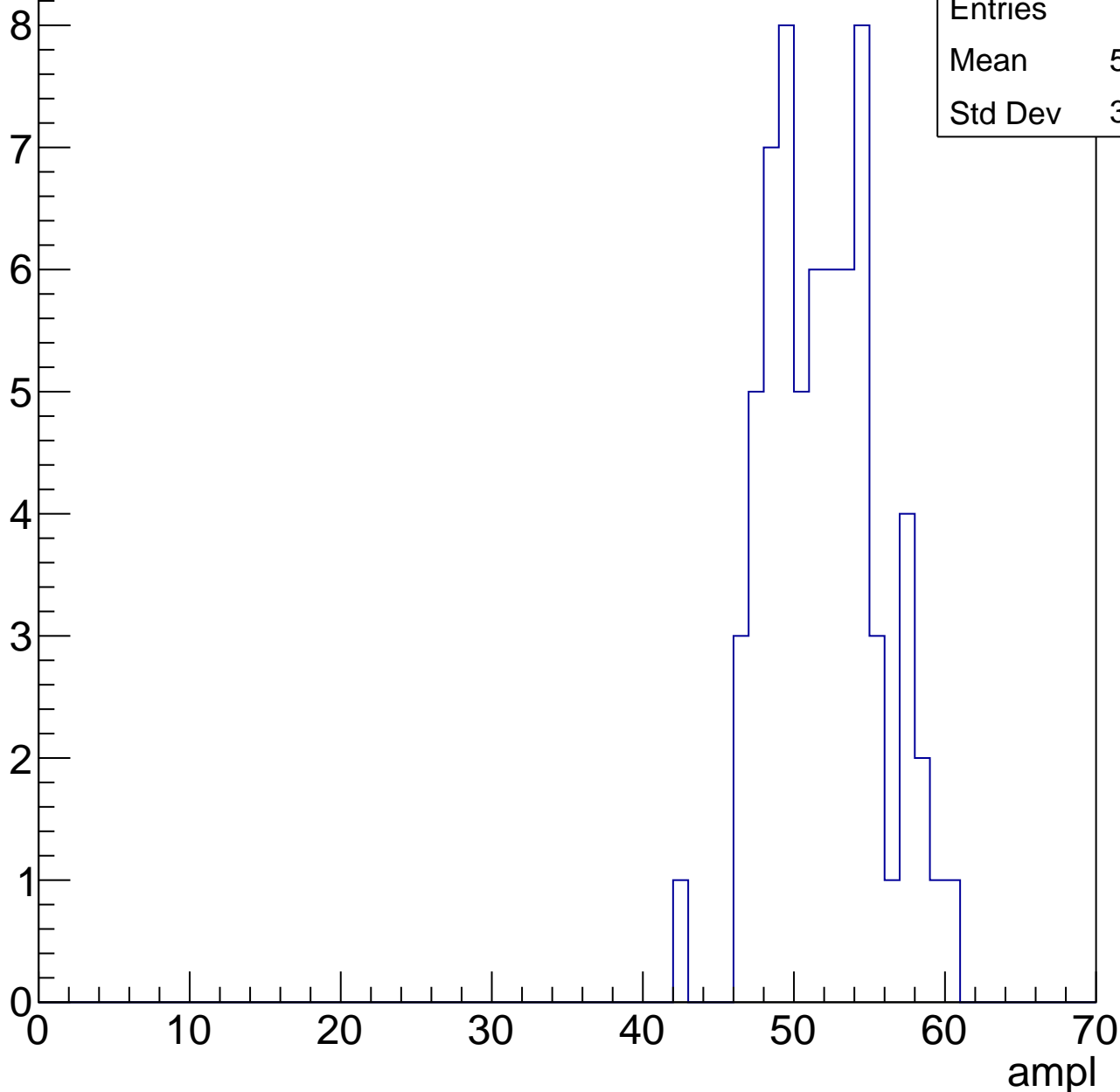


# B1L101S, U9-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

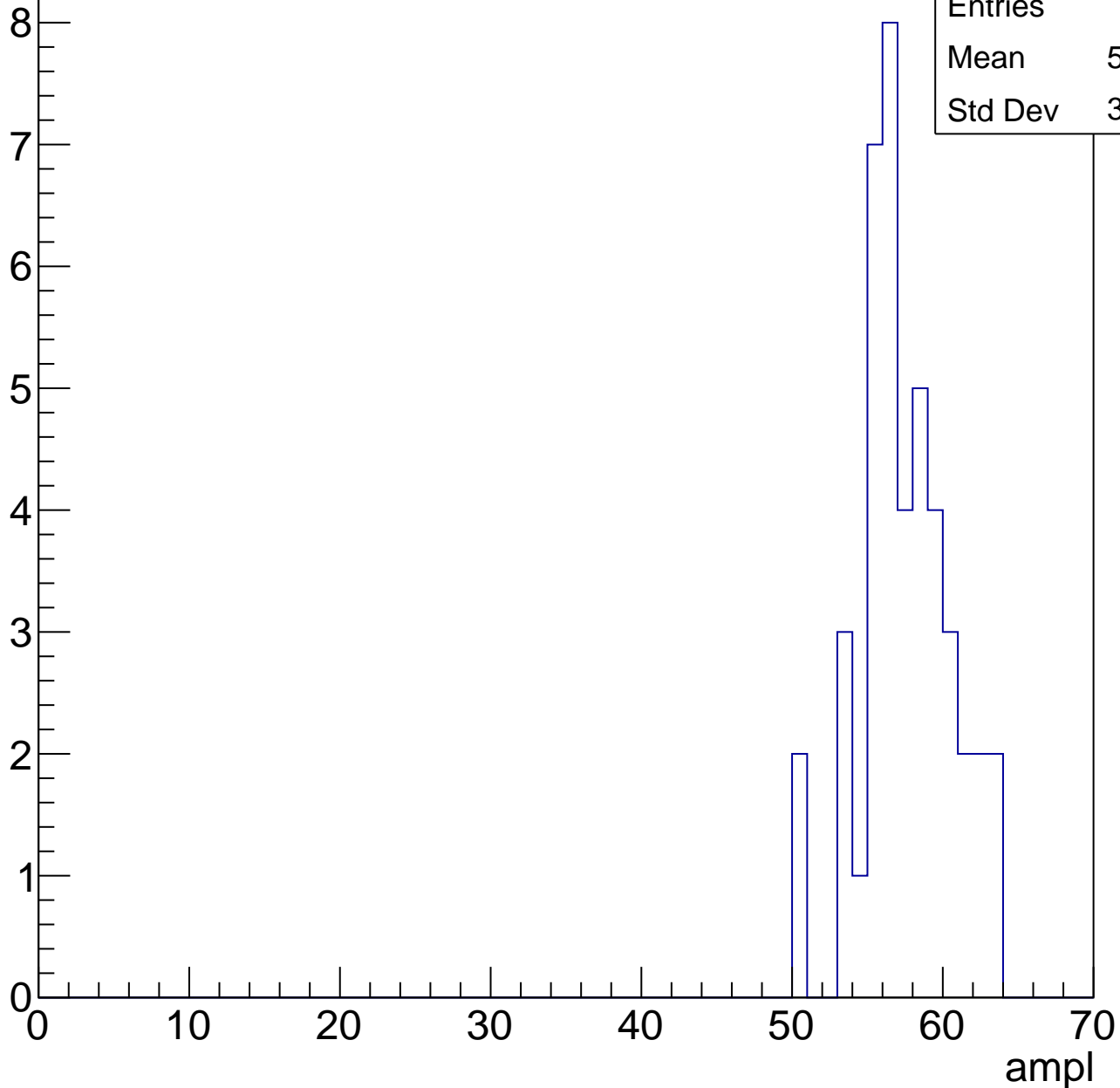
Entries	67
Mean	51.42
Std Dev	3.637



# B1L101S, U9-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



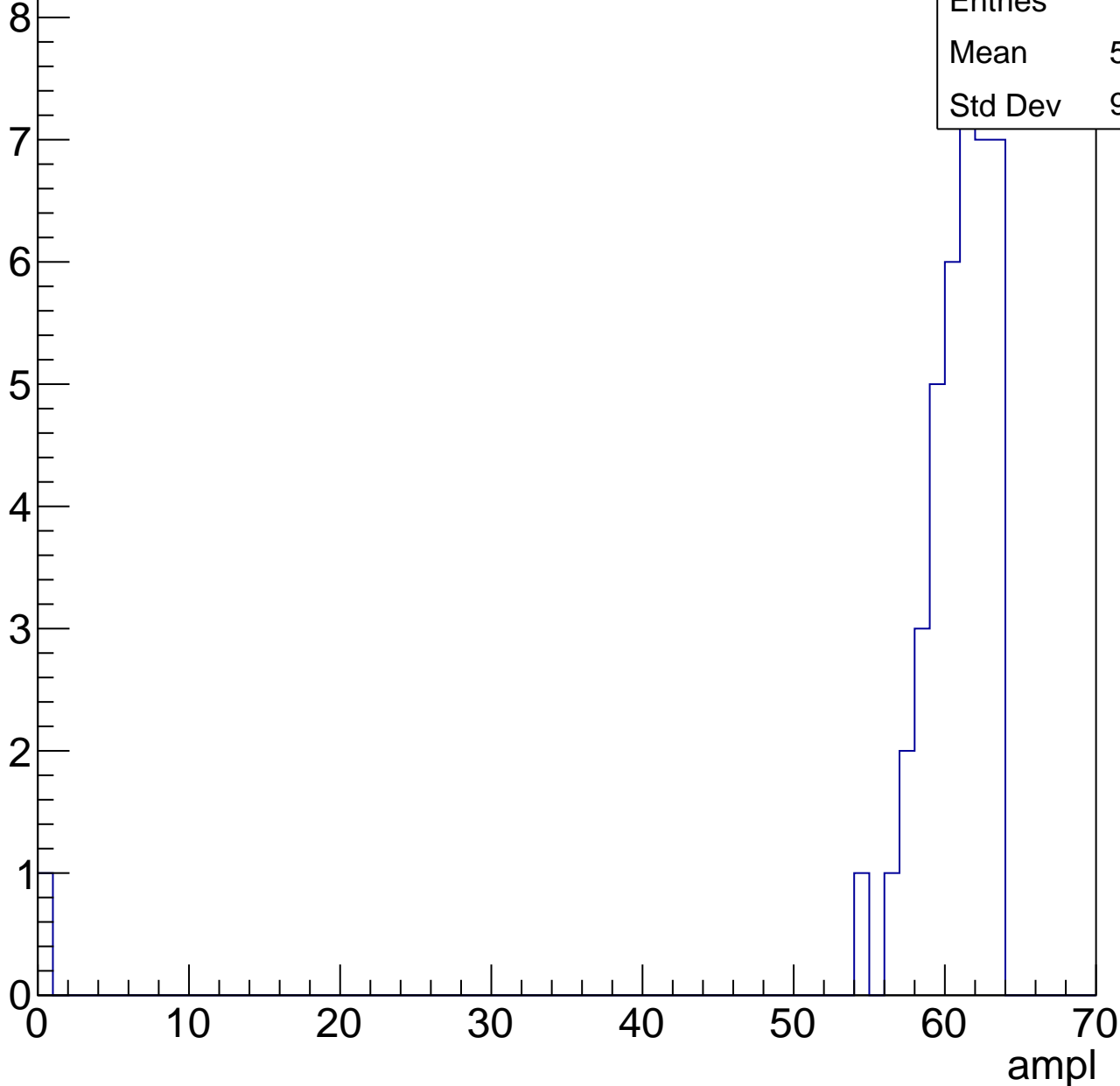
Entries	43
Mean	57.02
Std Dev	3.023

# B1L101S, U9-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	41
Mean	58.93
Std Dev	9.549



# B1L101S, U9-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U9-ch120, adc0

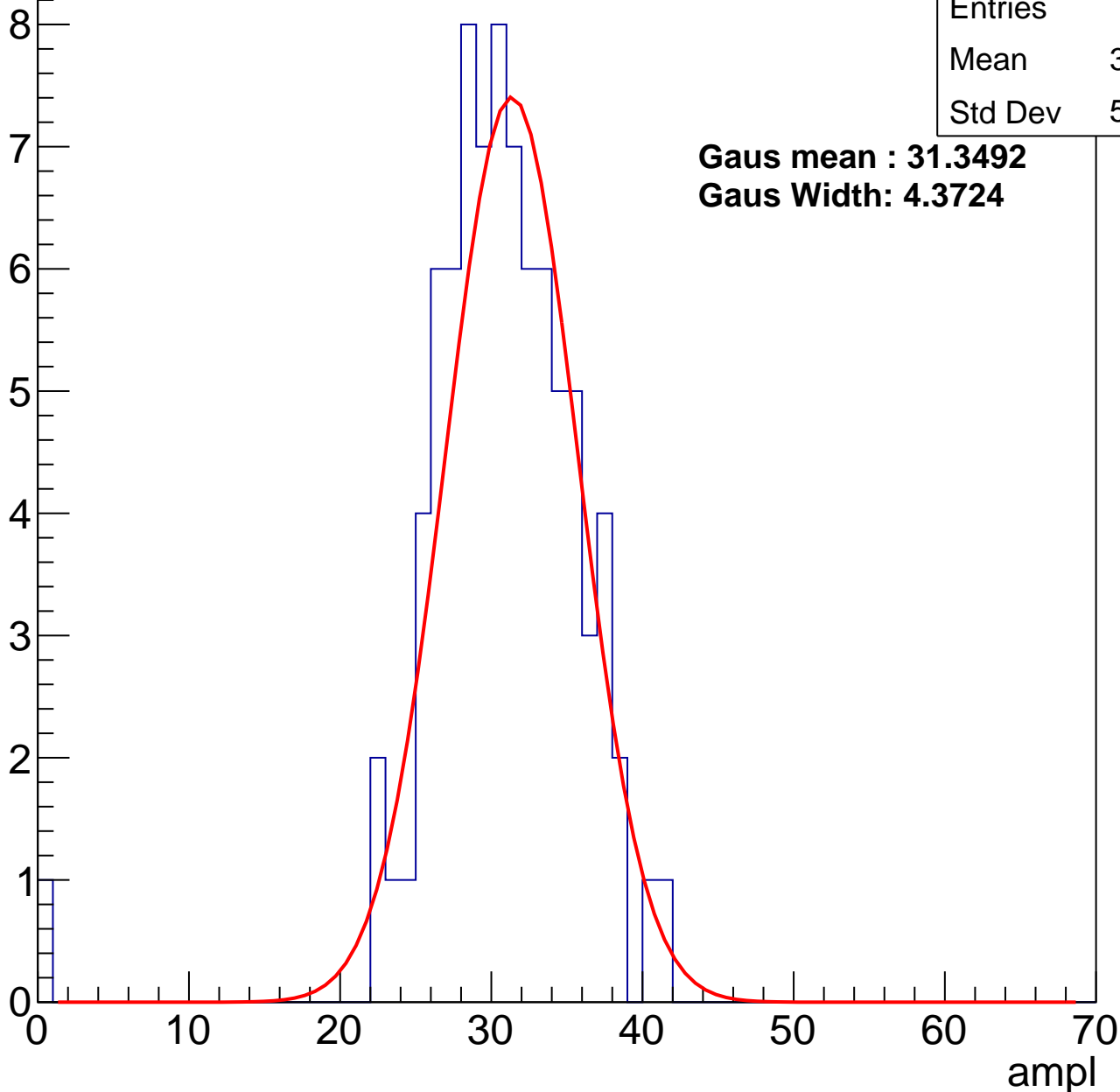
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	84
Mean	30.25
Std Dev	5.278

**Gaus mean : 31.3492**

**Gaus Width: 4.3724**



# B1L101S, U9-ch120, adc1

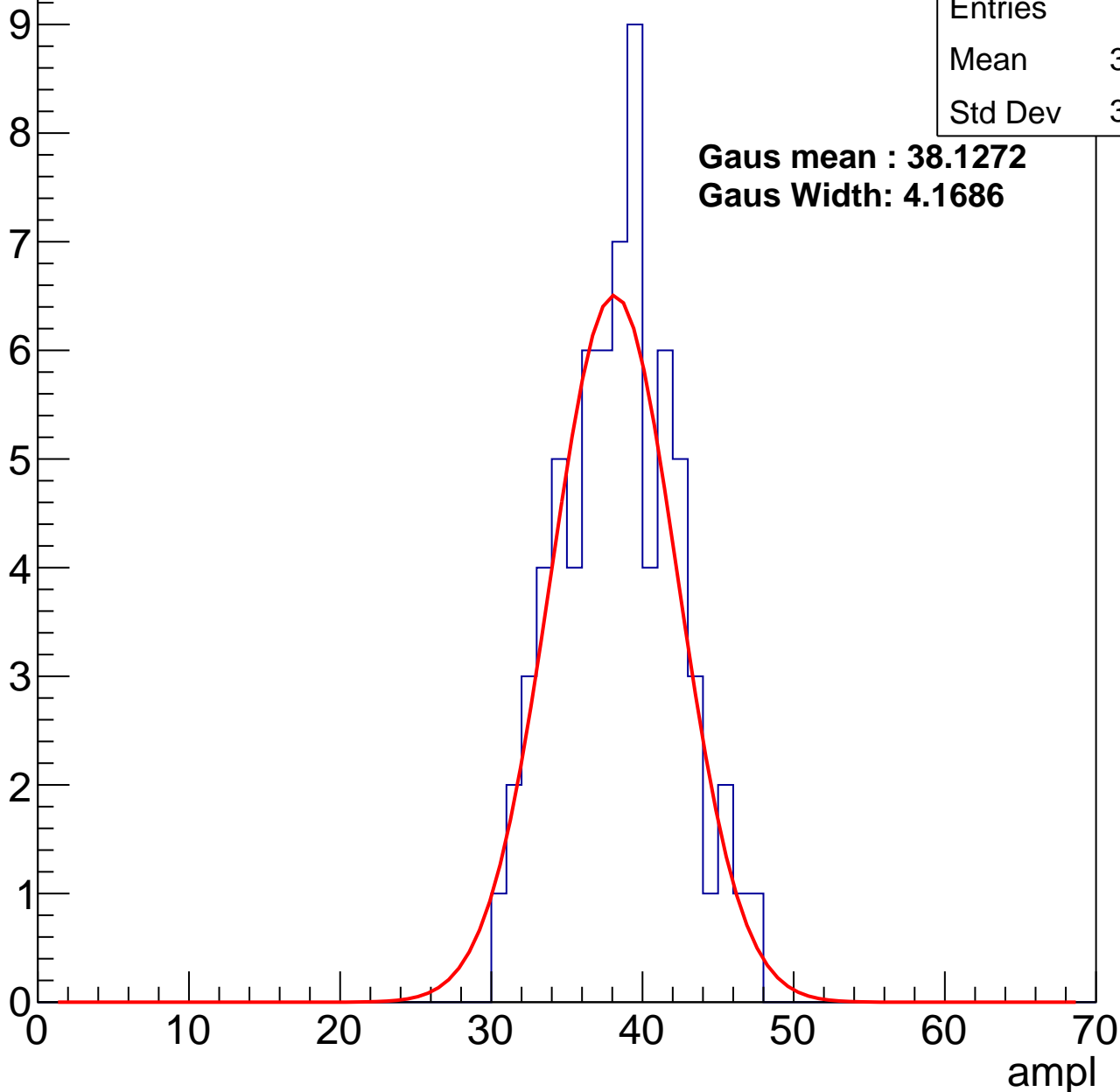
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	37.96
Std Dev	3.834

**Gaus mean : 38.1272**

**Gaus Width: 4.1686**



# B1L101S, U9-ch120, adc2

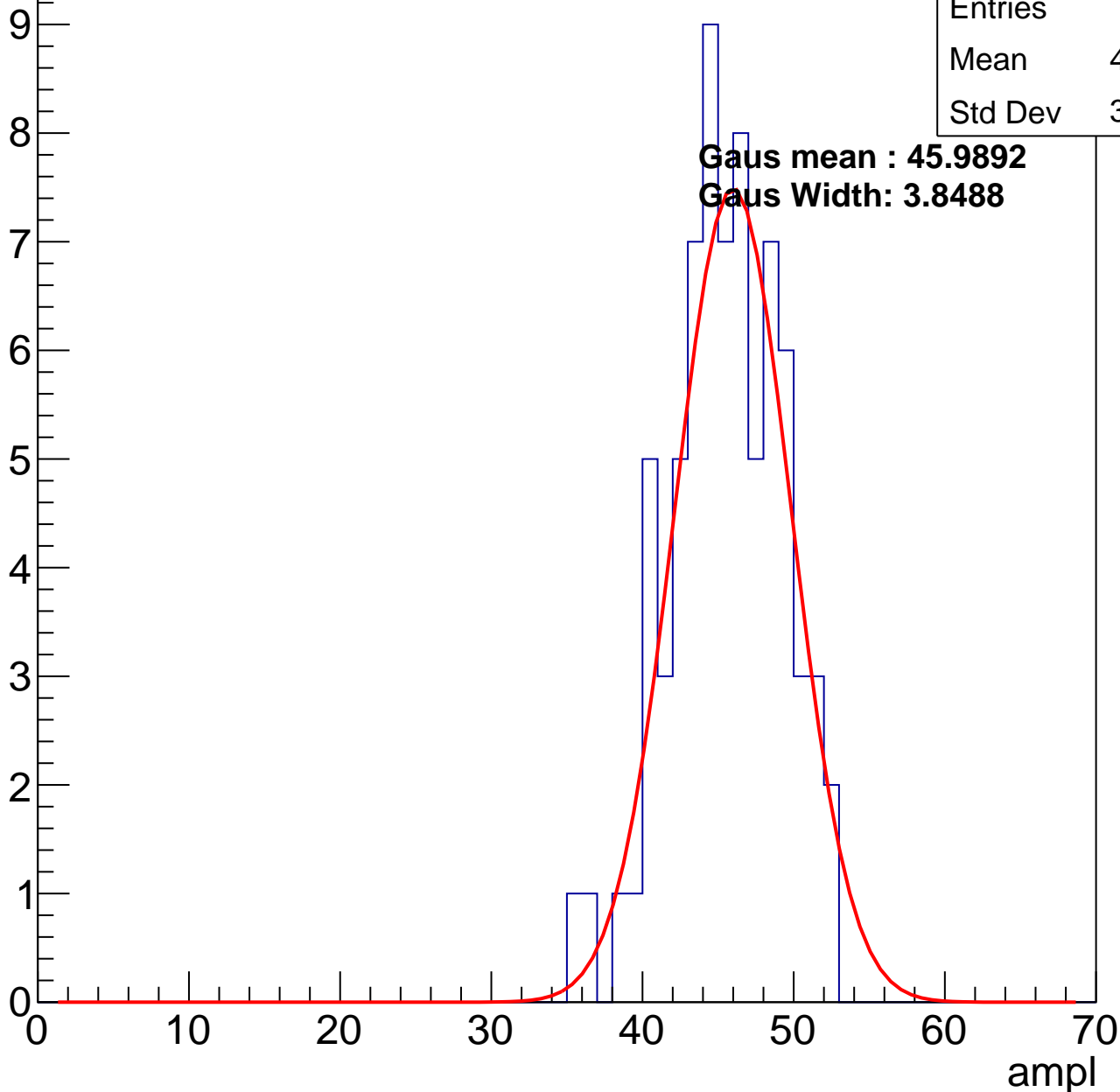
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	45.04
Std Dev	3.656

**Gaus mean : 45.9892**

**Gaus Width: 3.8488**

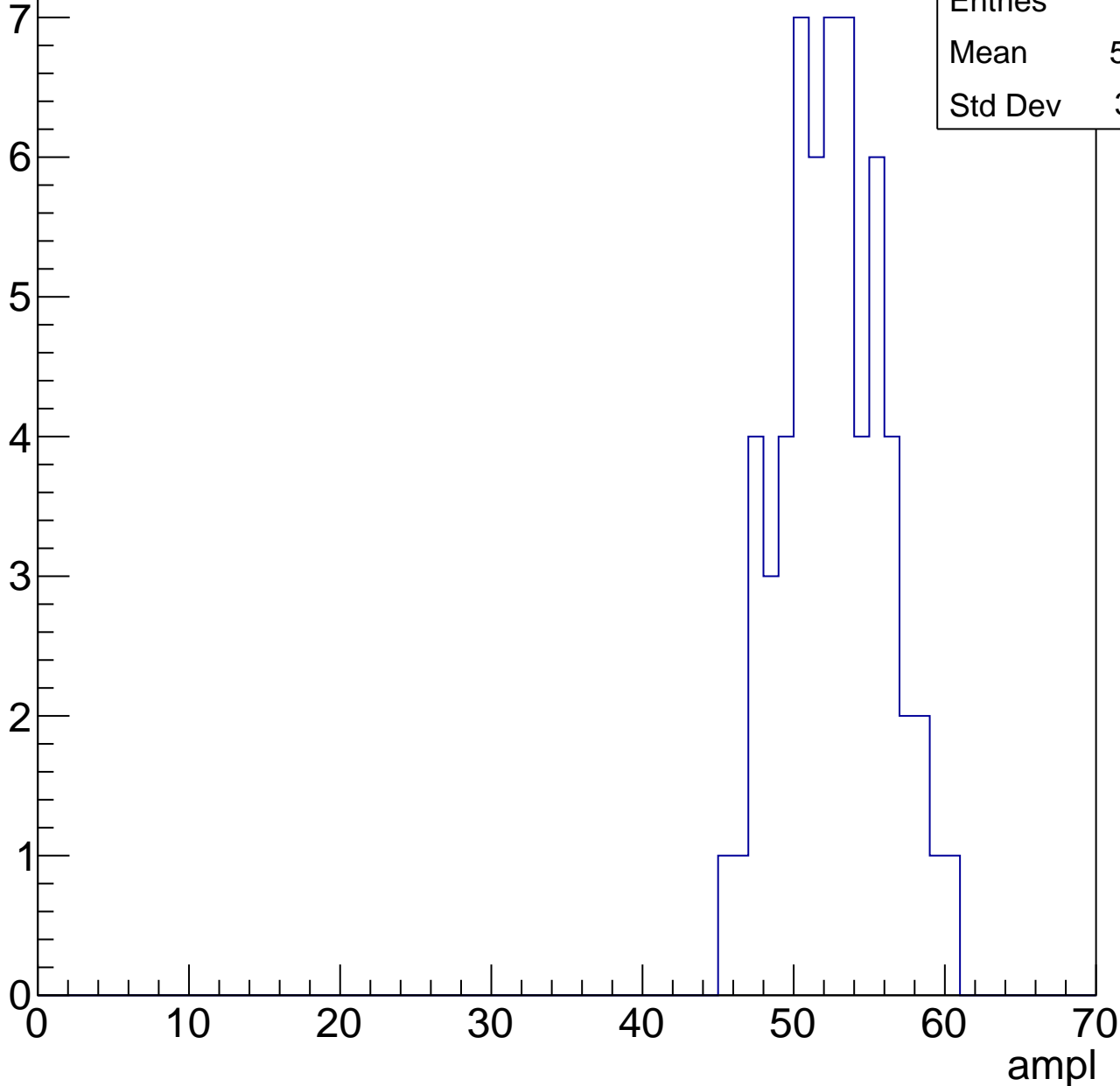


# B1L101S, U9-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

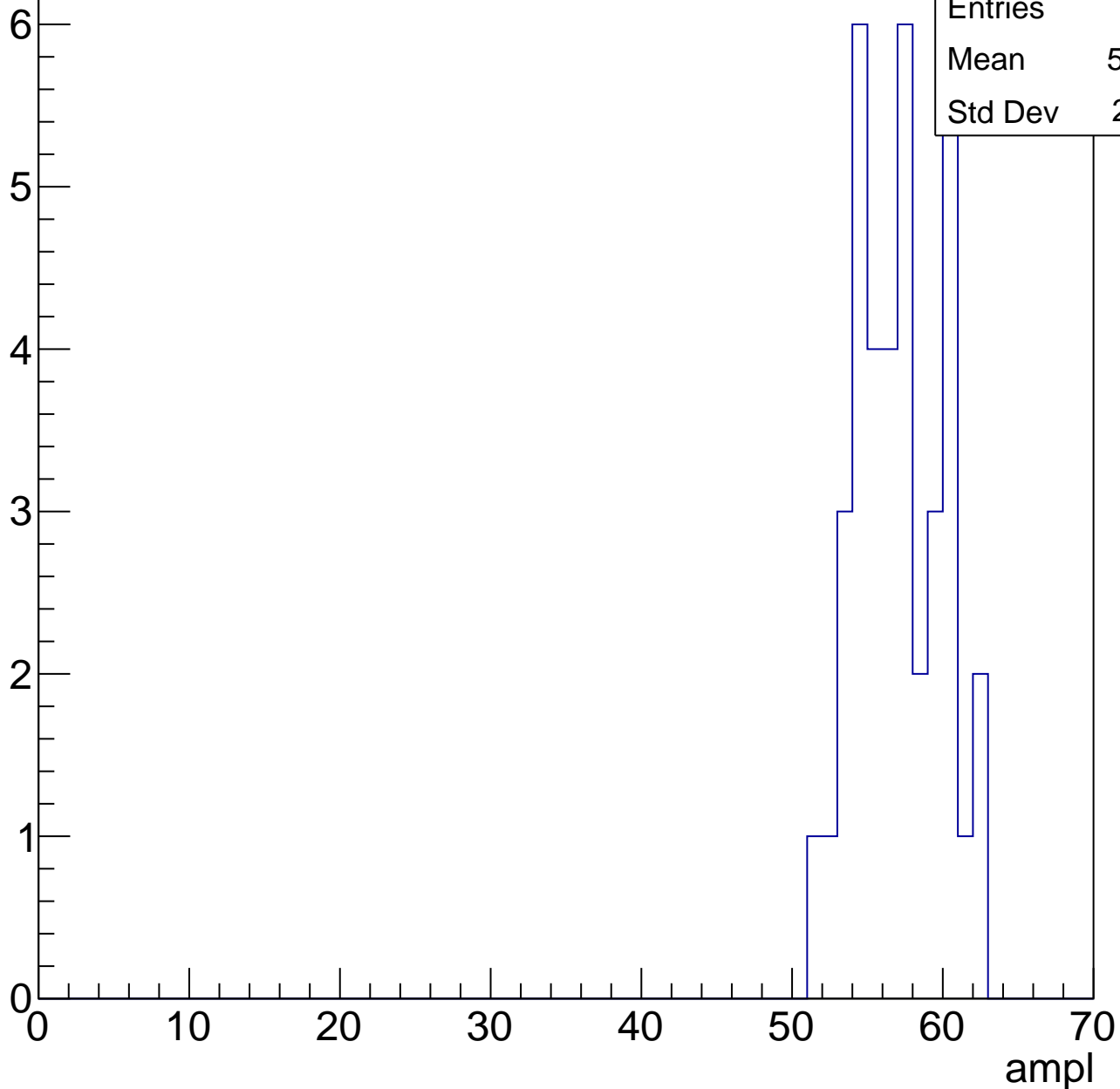
Entries	60
Mean	52.15
Std Dev	3.361



# B1L101S, U9-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



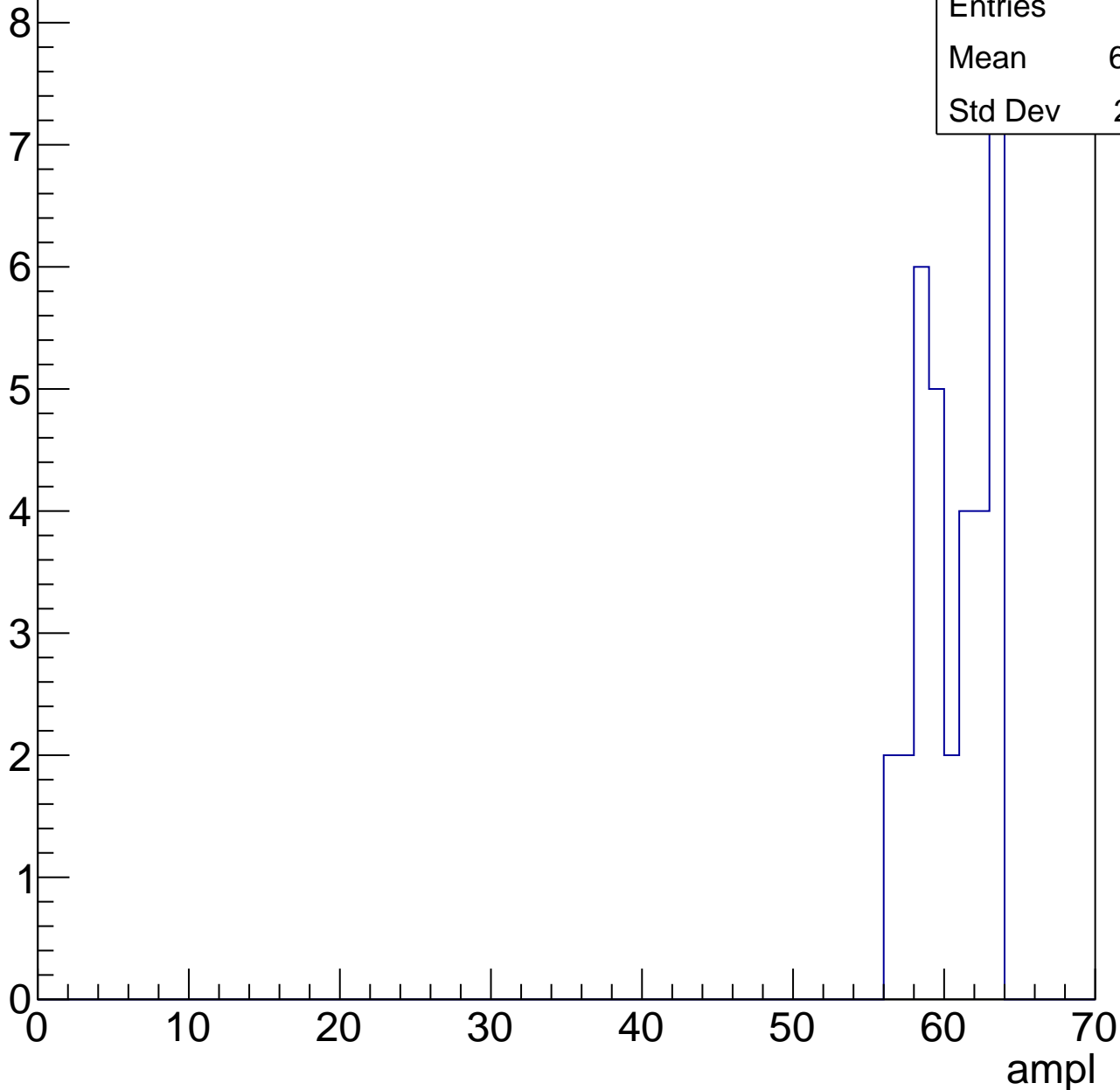
Entries	39
Mean	56.67
Std Dev	2.831

# B1L101S, U9-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	33
Mean	60.15
Std Dev	2.271

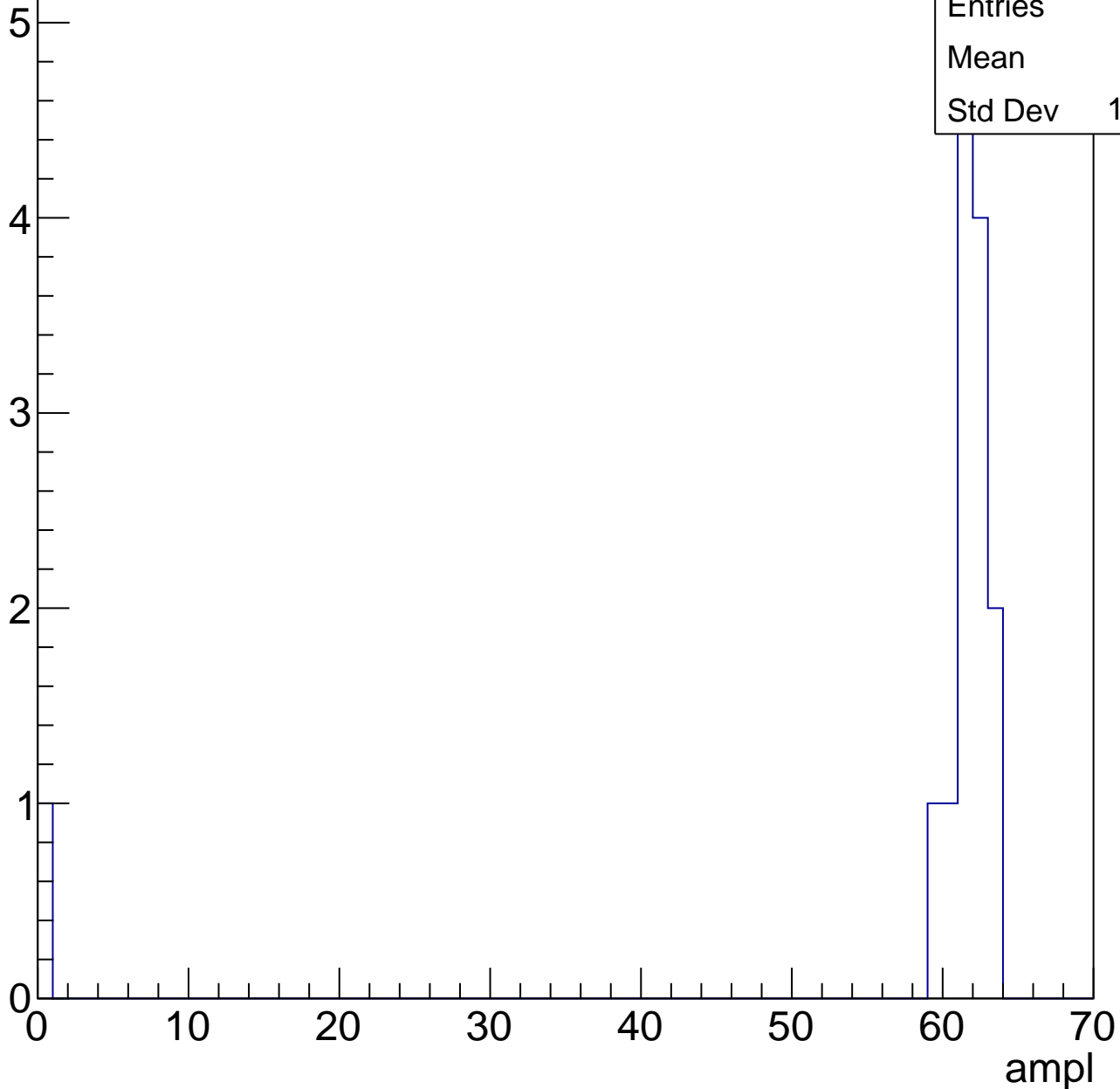


# B1L101S, U9-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	14
Mean	57
Std Dev	15.84





# B1L101S, U9-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch121, adc0

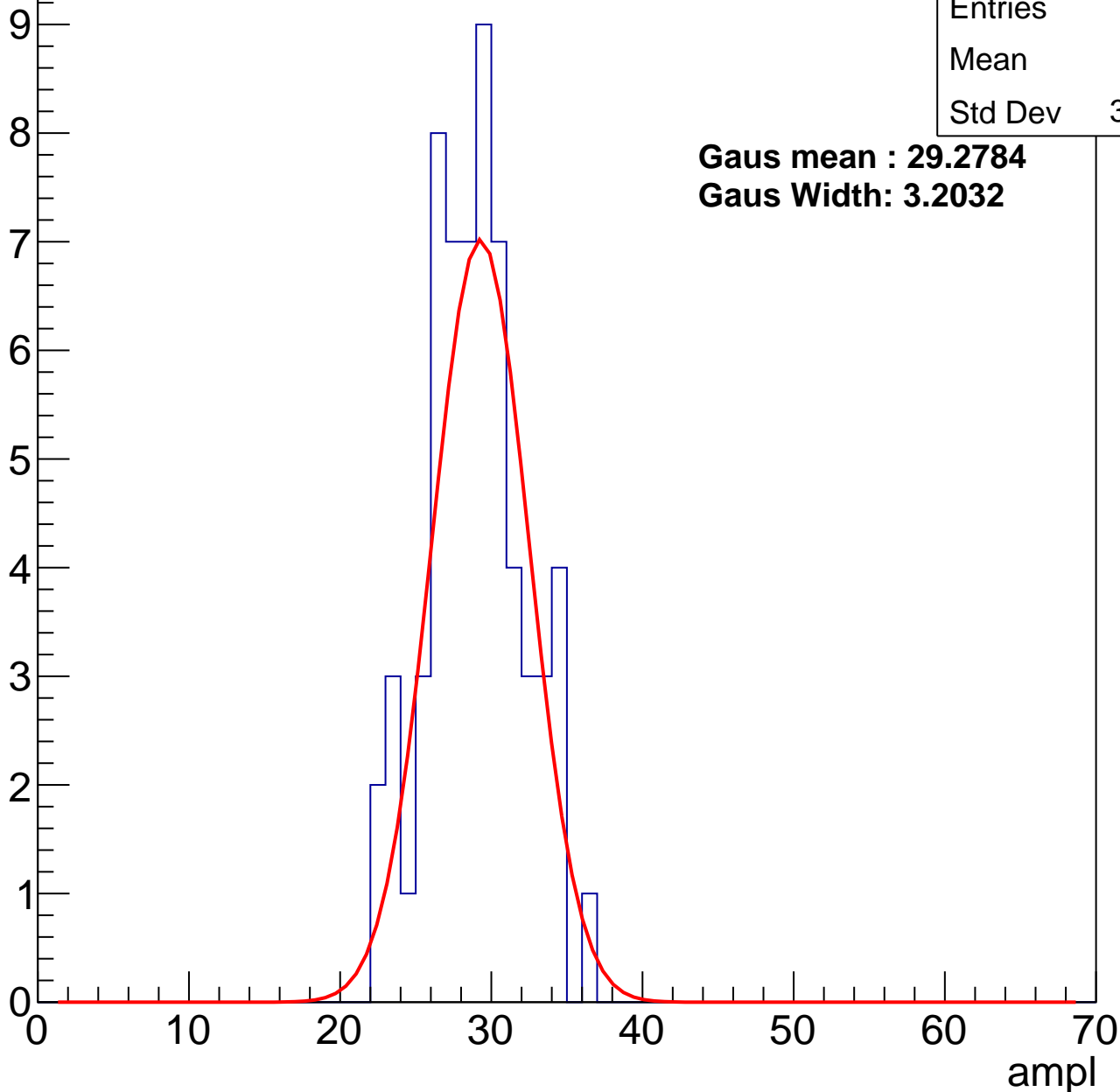
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	28.5
Std Dev	3.156

**Gaus mean : 29.2784**

**Gaus Width: 3.2032**



# B1L101S, U9-ch121, adc1

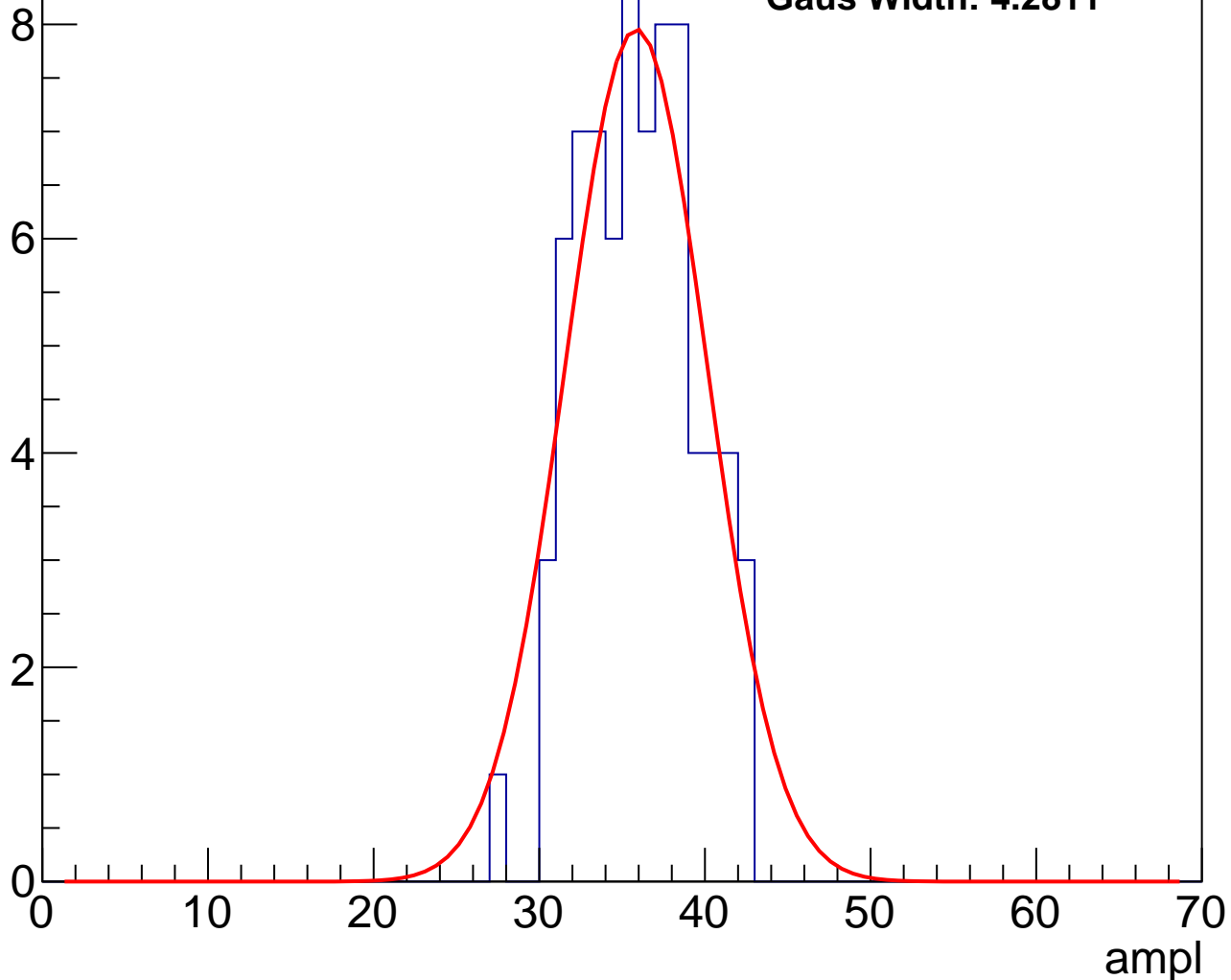
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	35.51
Std Dev	3.354

**Gaus mean : 35.8559**

**Gaus Width: 4.2811**



# B1L101S, U9-ch121, adc2

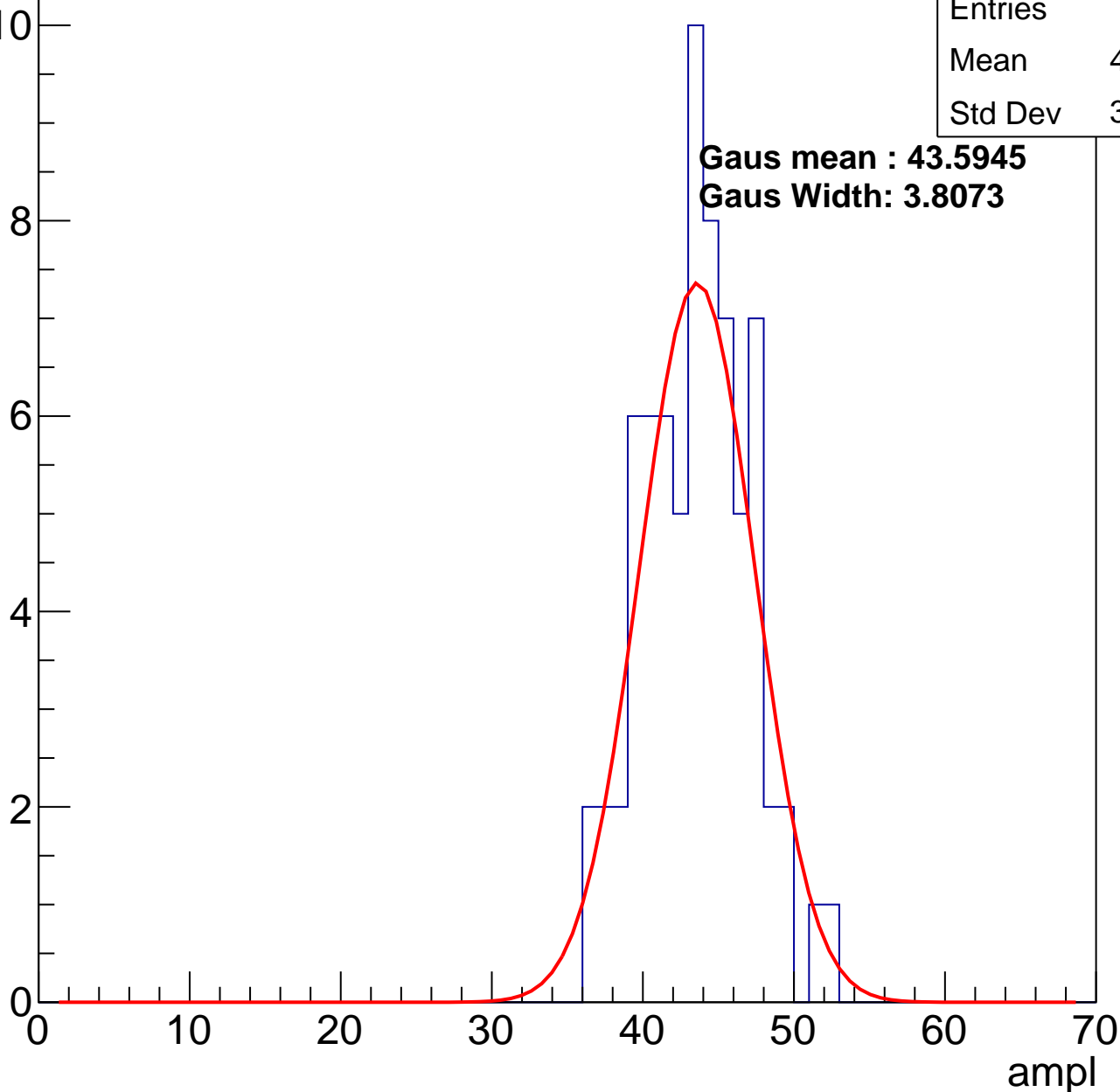
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	43.12
Std Dev	3.452

**Gaus mean : 43.5945**

**Gaus Width: 3.8073**

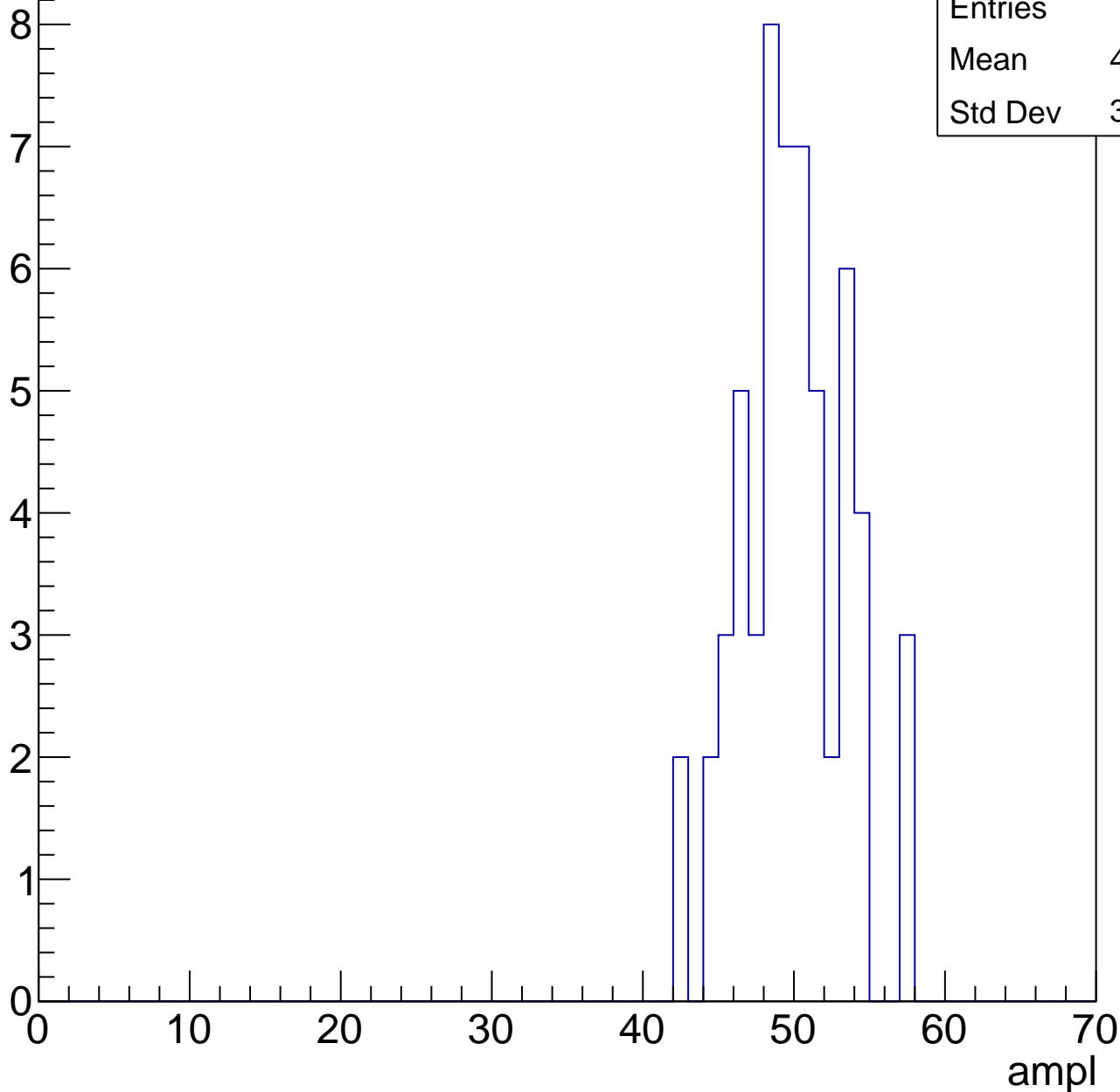


# B1L101S, U9-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

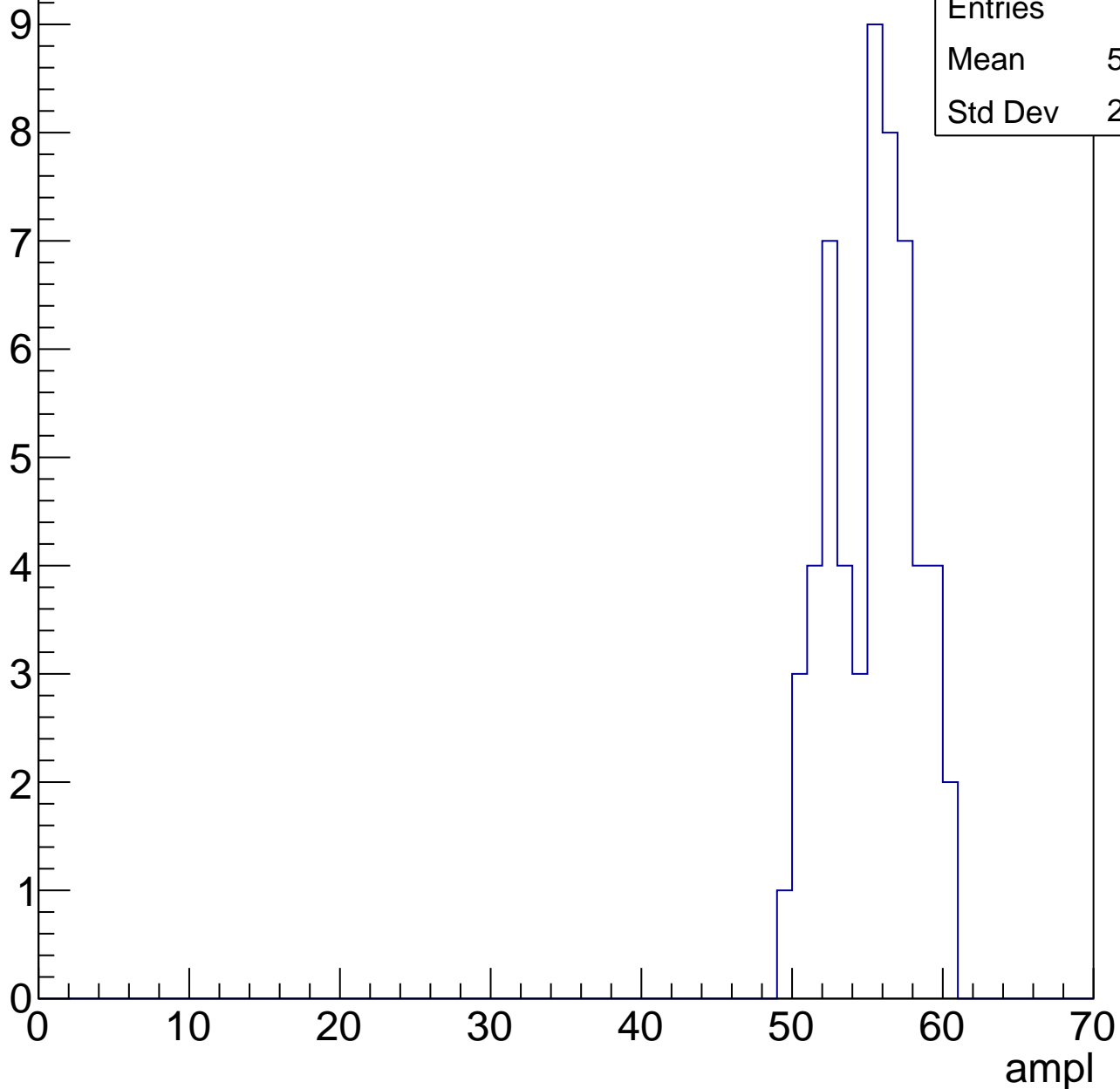
Entries	57
Mean	49.46
Std Dev	3.459



# B1L101S, U9-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	56
Mean	54.84
Std Dev	2.808

# B1L101S, U9-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	50
Mean	60.22
Std Dev	2.54

Entry

10

8

6

4

2

0

0

10

20

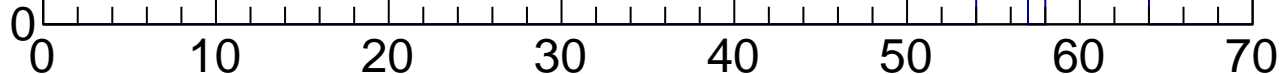
30

40

50

60

ampl



# B1L101S, U9-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

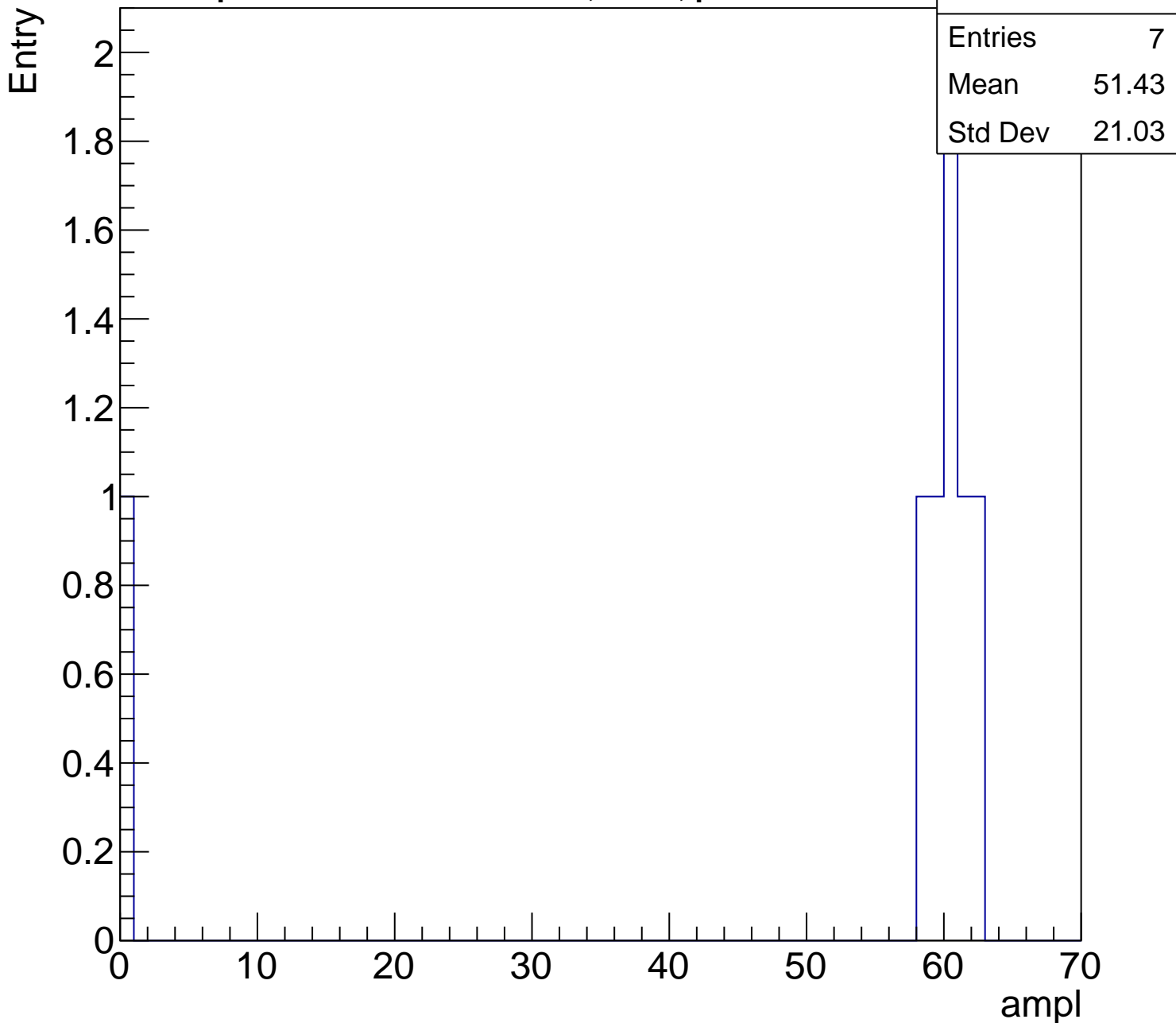
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	51.43
Std Dev	21.03

0 10 20 30 40 50 60 70

ampl





# B1L101S, U9-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch122, adc0

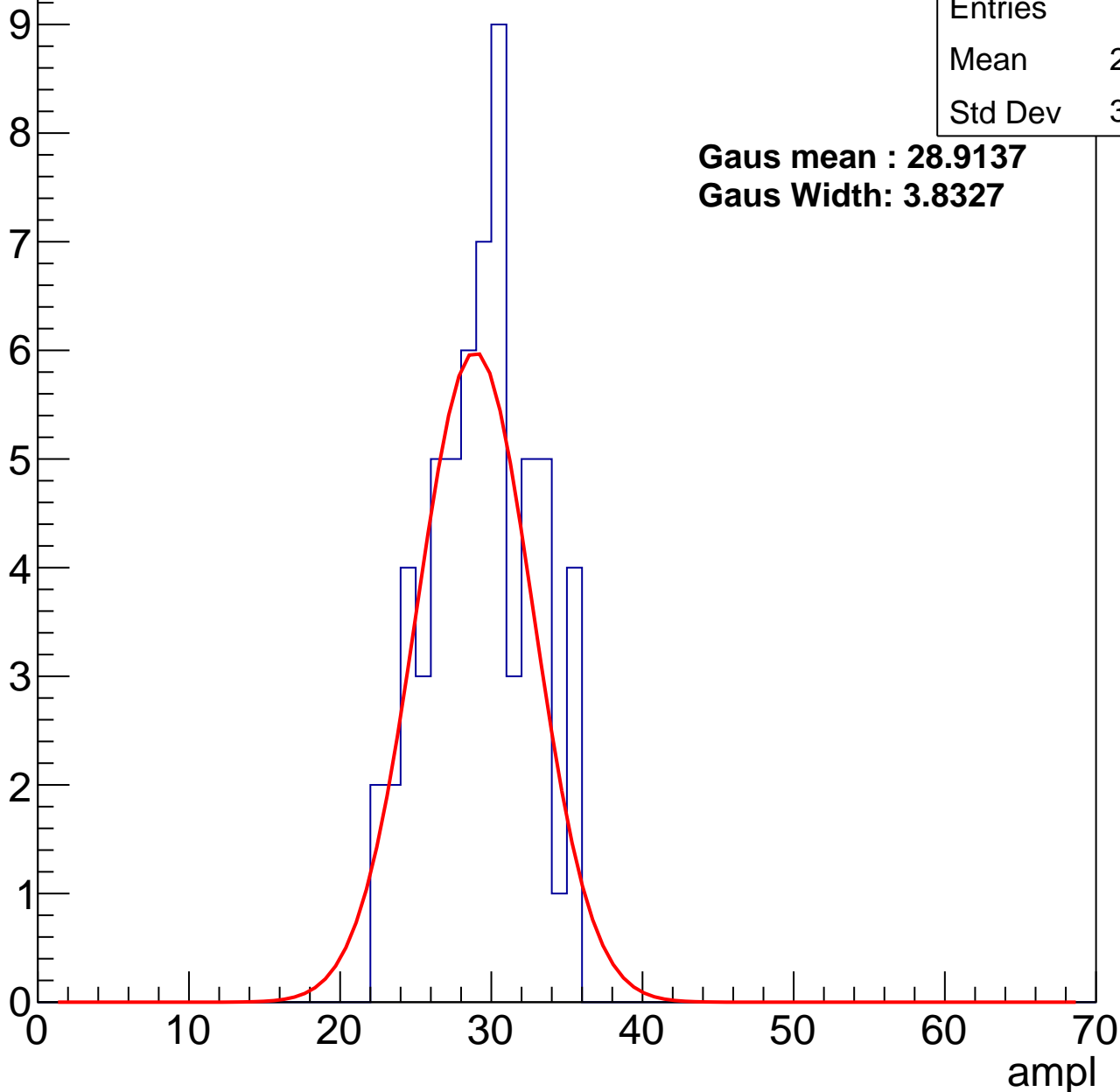
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	28.84
Std Dev	3.393

**Gaus mean : 28.9137**

**Gaus Width: 3.8327**



# B1L101S, U9-ch122, adc1

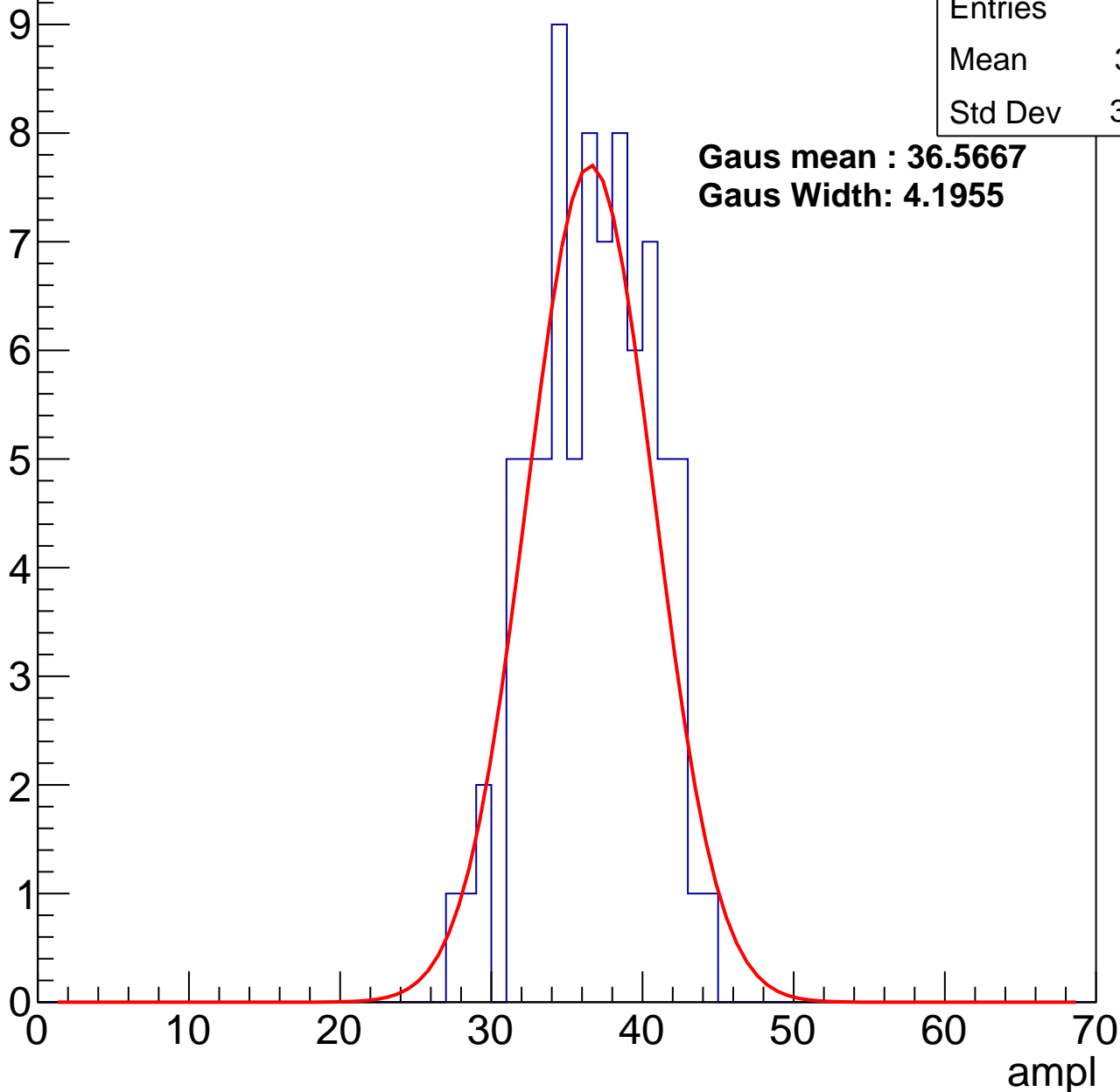
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	36.31
Std Dev	3.767

**Gaus mean : 36.5667**

**Gaus Width: 4.1955**



# B1L101S, U9-ch122, adc2

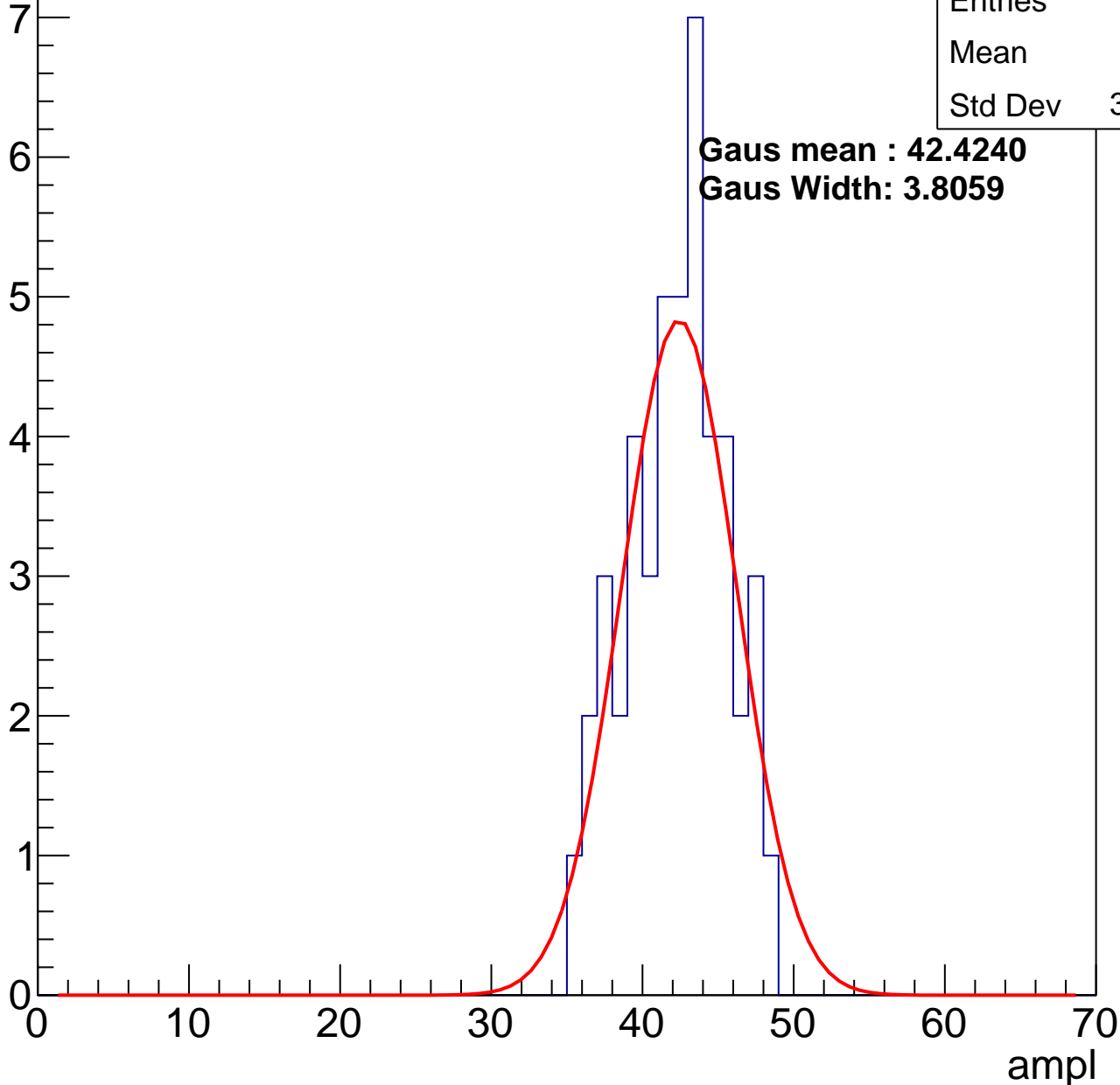
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	41.8
Std Dev	3.234

**Gaus mean : 42.4240**

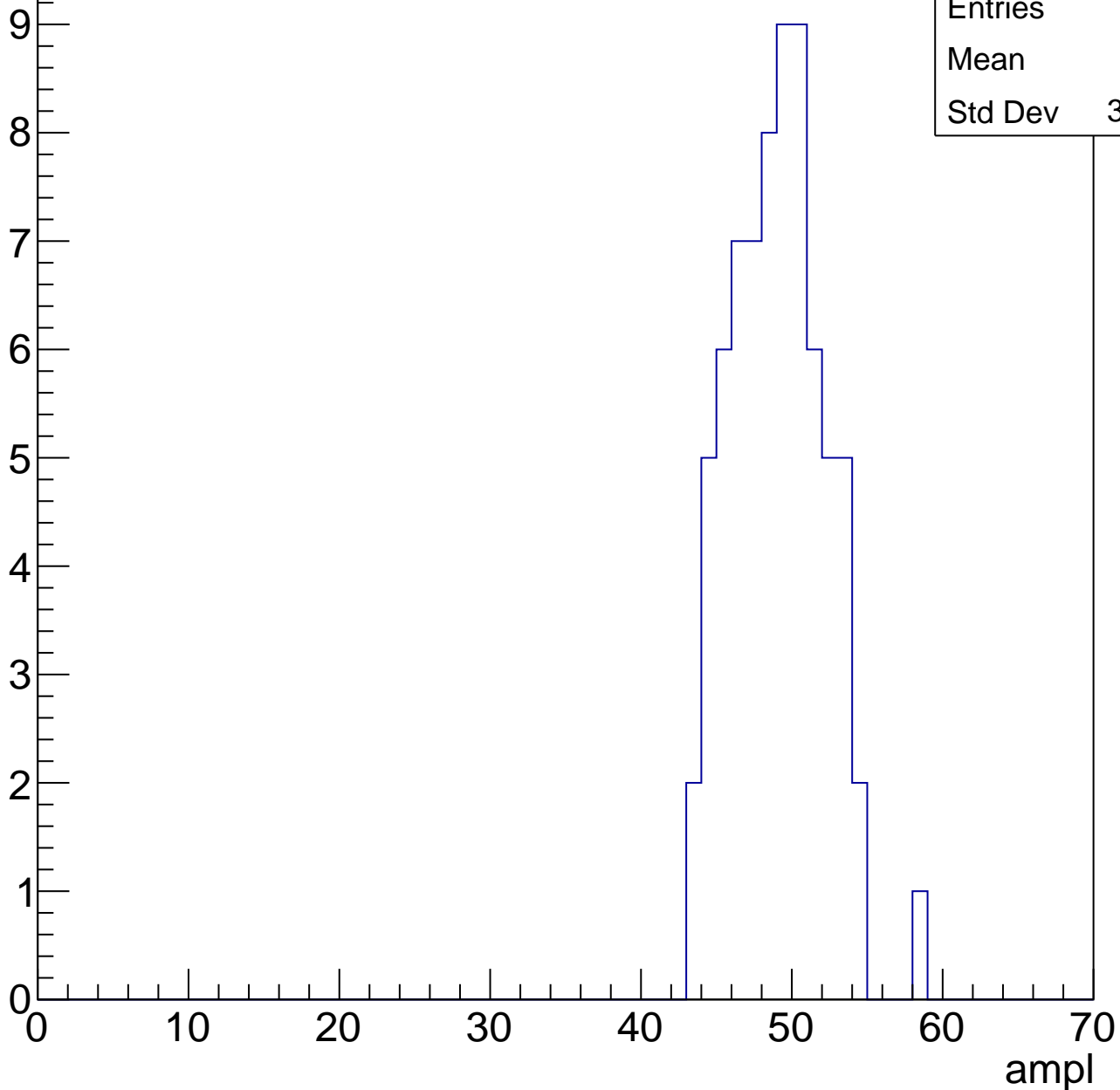
**Gaus Width: 3.8059**



# B1L101S, U9-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



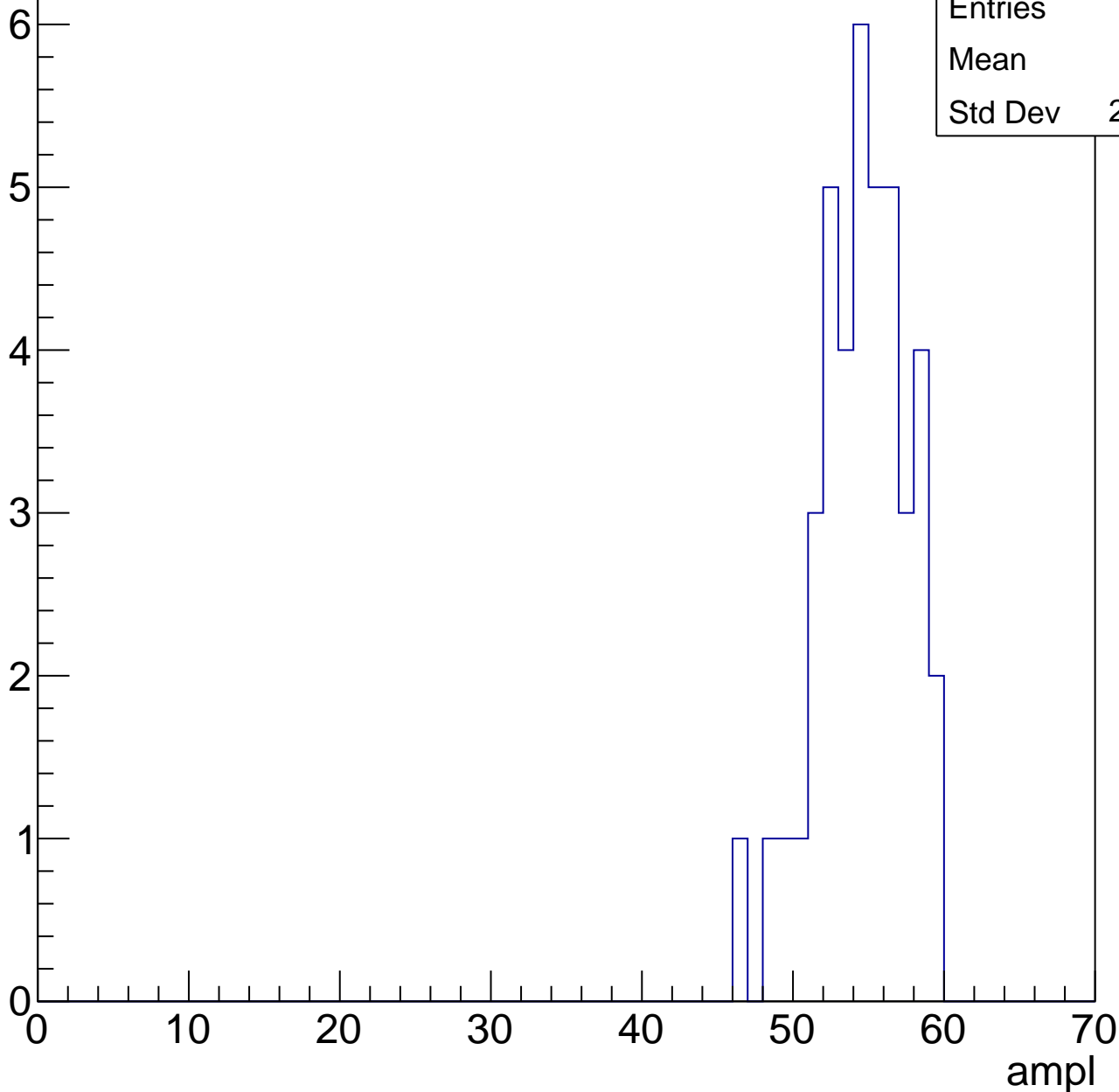
Entries	72
Mean	48.6
Std Dev	3.049

# B1L101S, U9-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	41
Mean	54.1
Std Dev	2.953

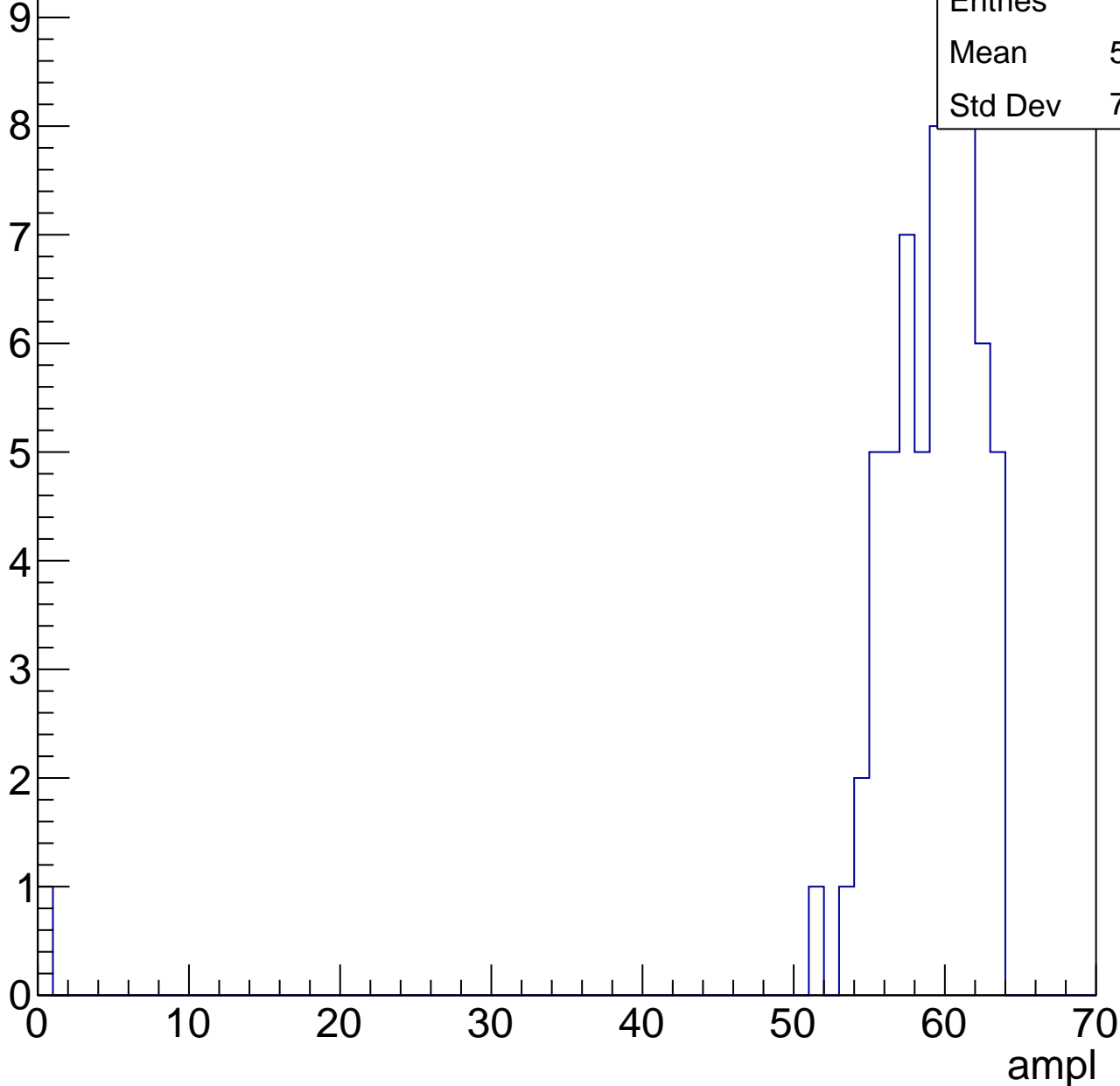


# B1L101S, U9-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	57.88
Std Dev	7.793

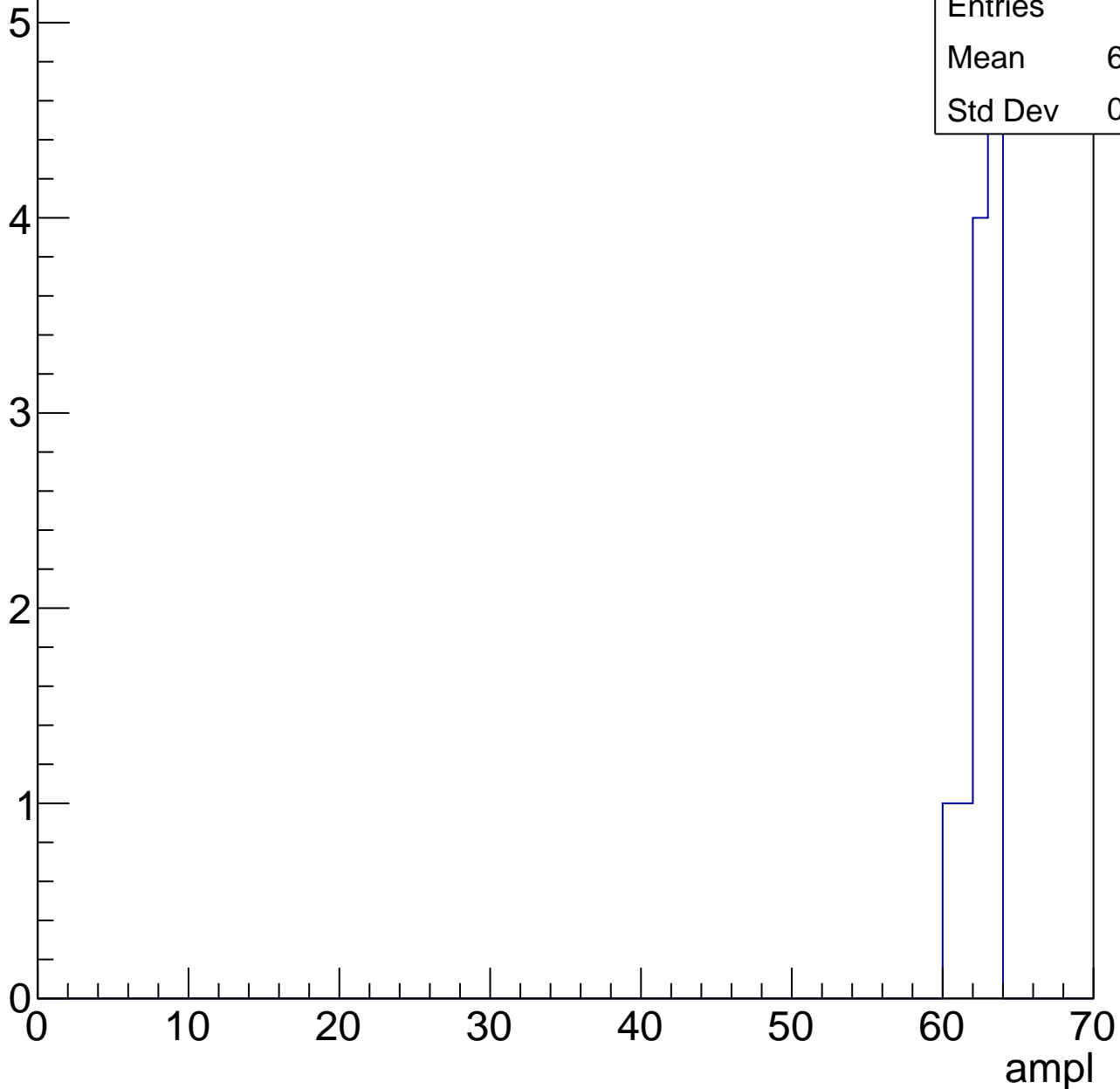


# B1L101S, U9-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	11
Mean	62.18
Std Dev	0.936





# B1L101S, U9-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch123, adc0

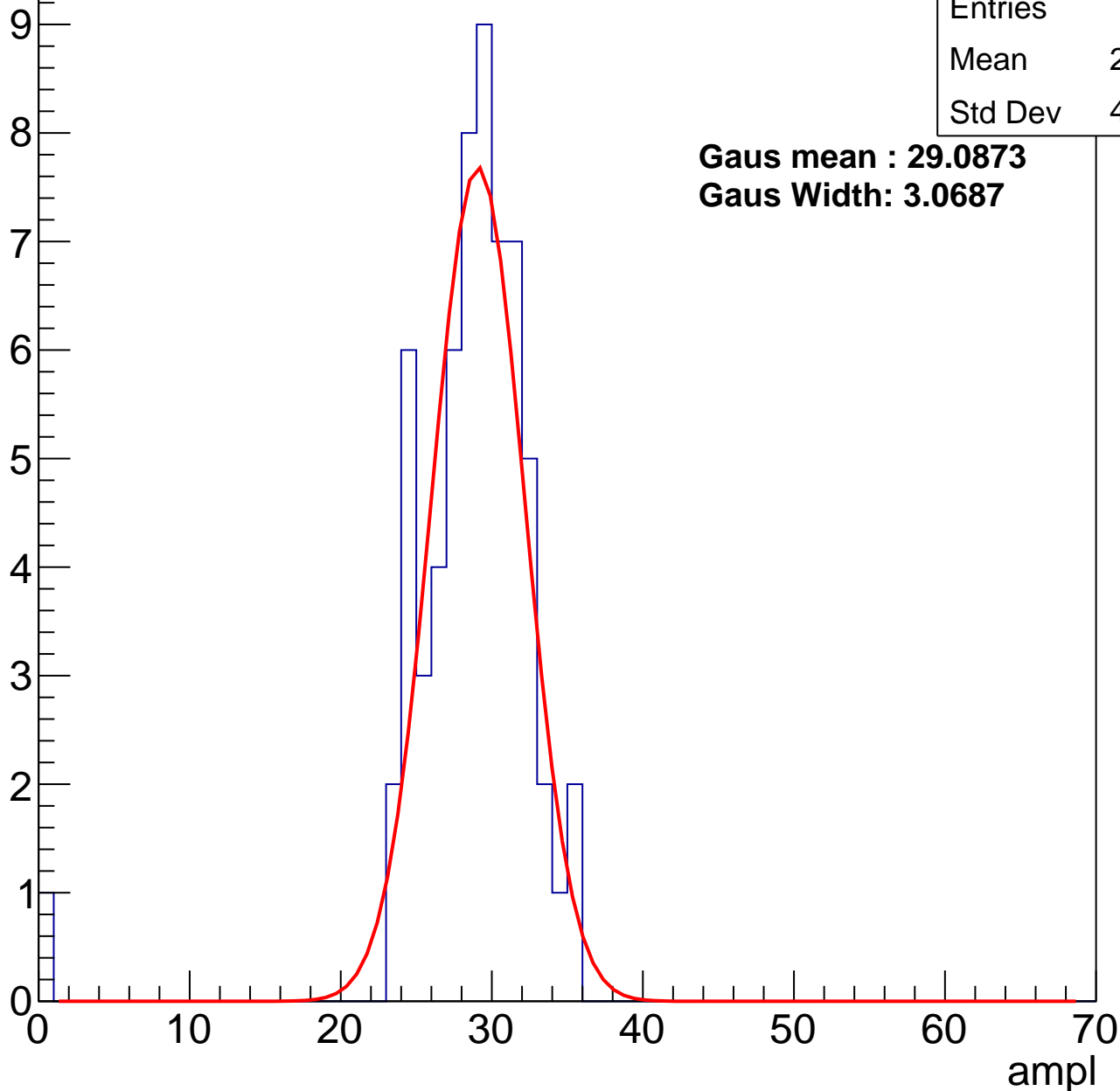
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	28.14
Std Dev	4.615

**Gaus mean : 29.0873**

**Gaus Width: 3.0687**



# B1L101S, U9-ch123, adc1

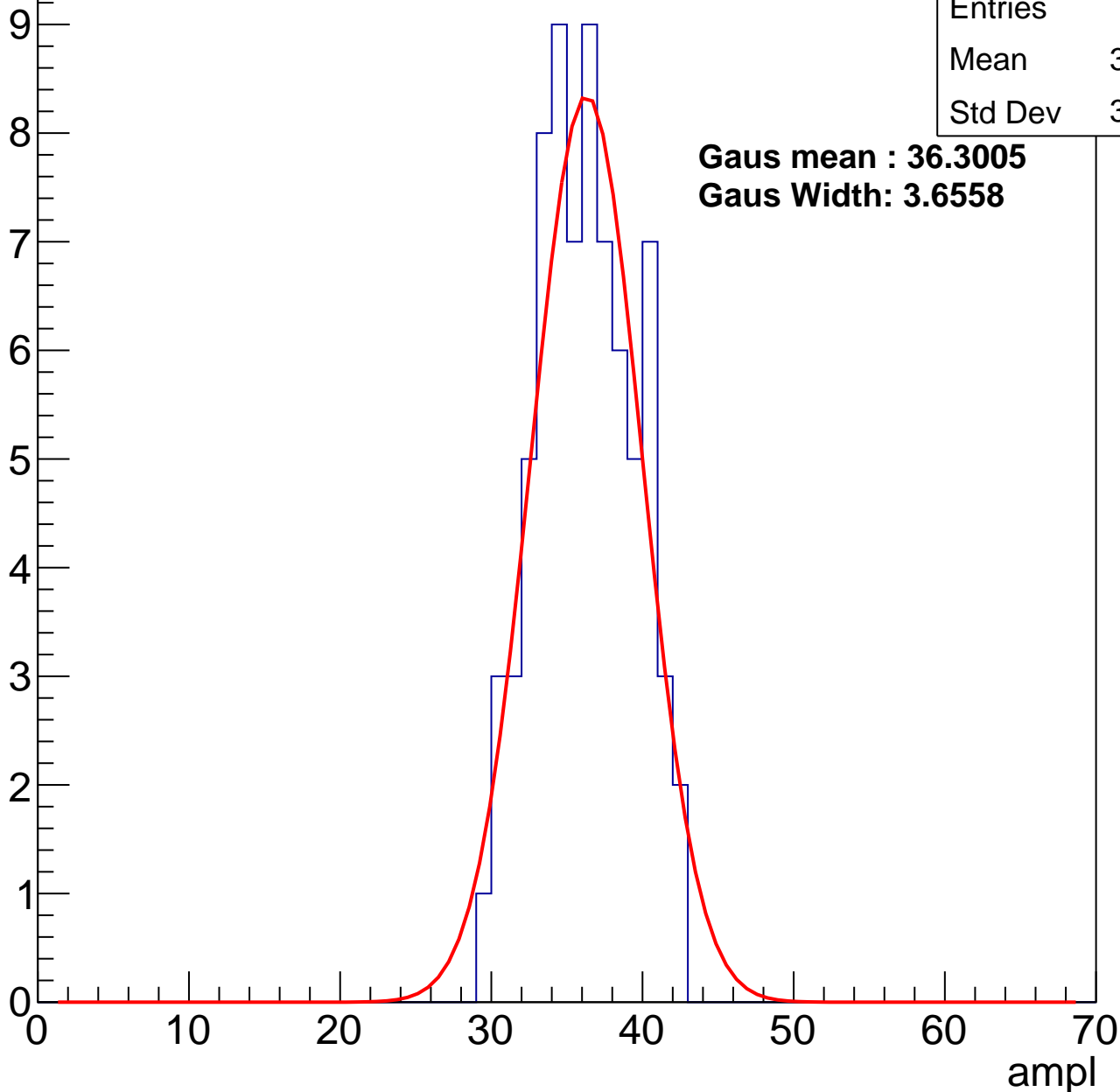
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	35.73
Std Dev	3.176

**Gaus mean : 36.3005**

**Gaus Width: 3.6558**



# B1L101S, U9-ch123, adc2

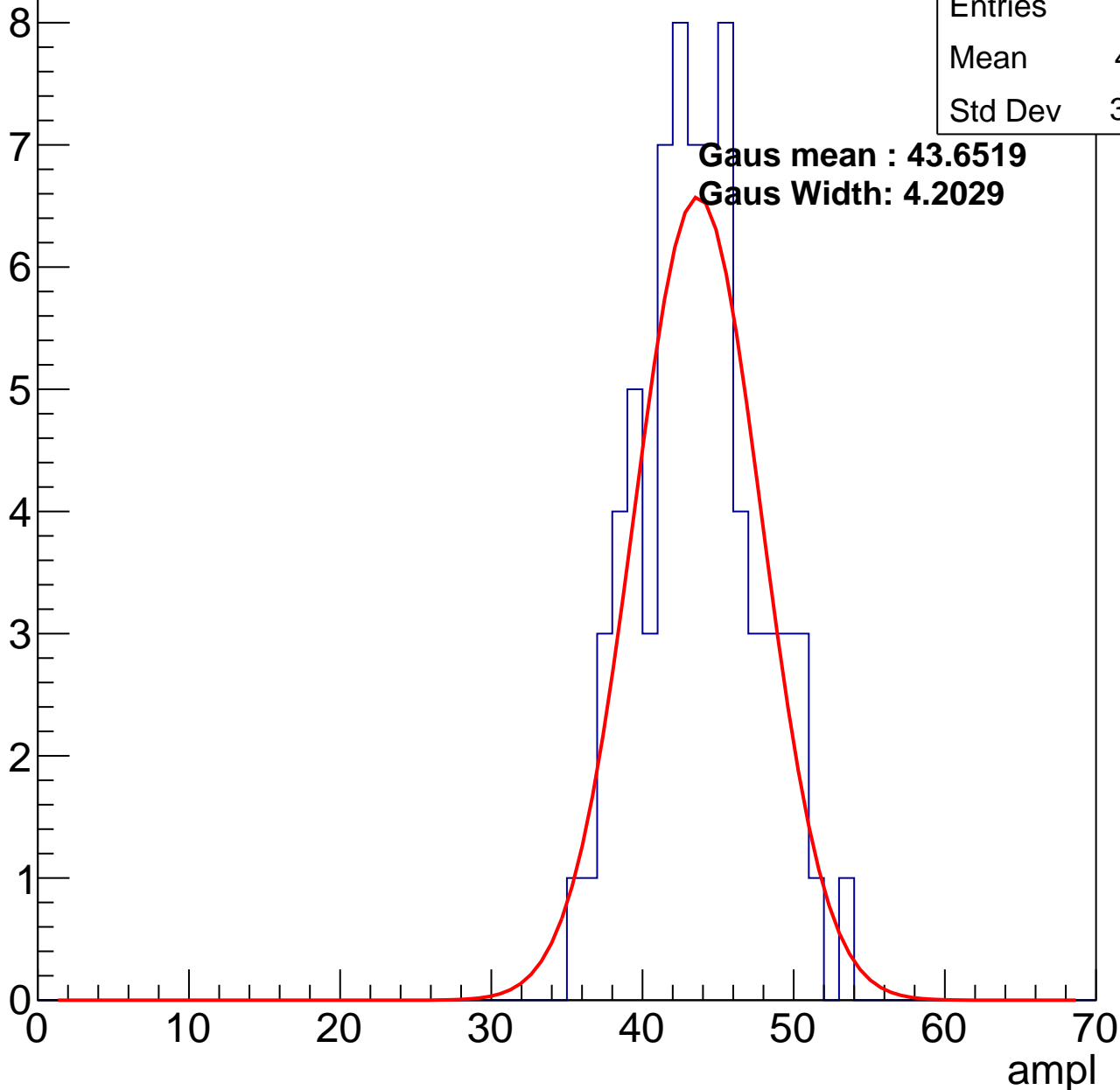
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	43.21
Std Dev	3.869

**Gaus mean : 43.6519**

**Gaus Width: 4.2029**

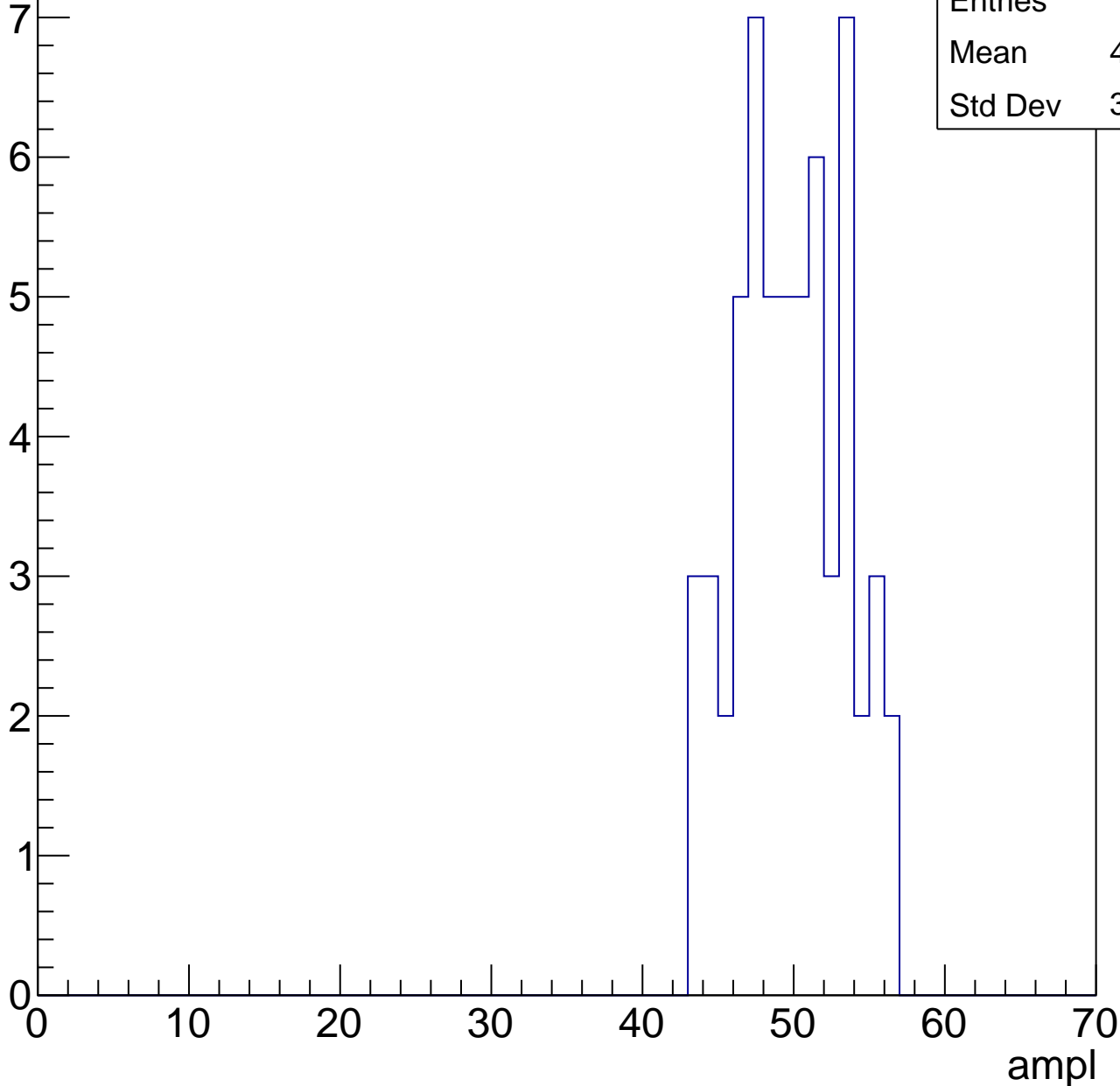


# B1L101S, U9-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	49.36
Std Dev	3.497

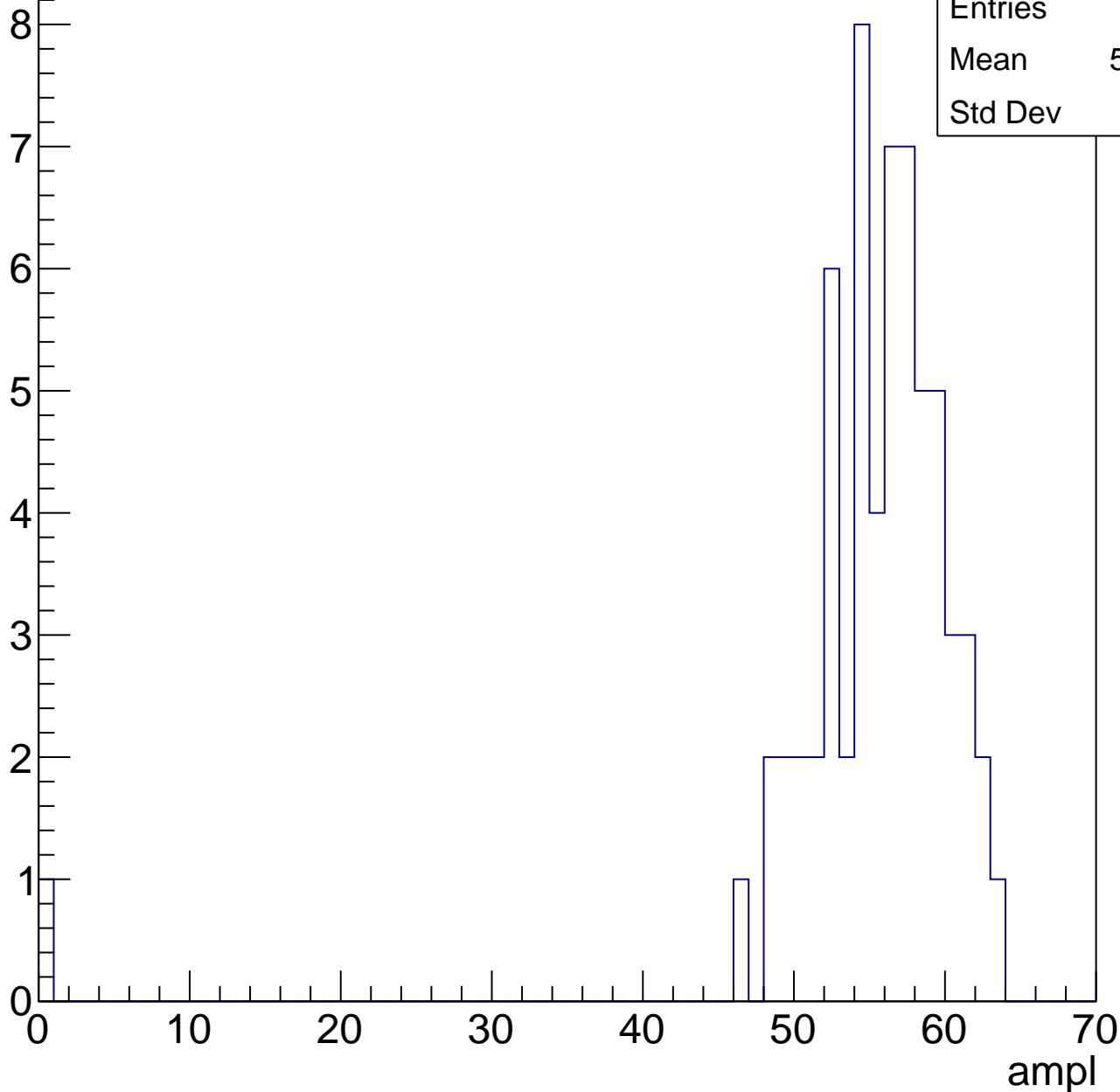


# B1L101S, U9-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

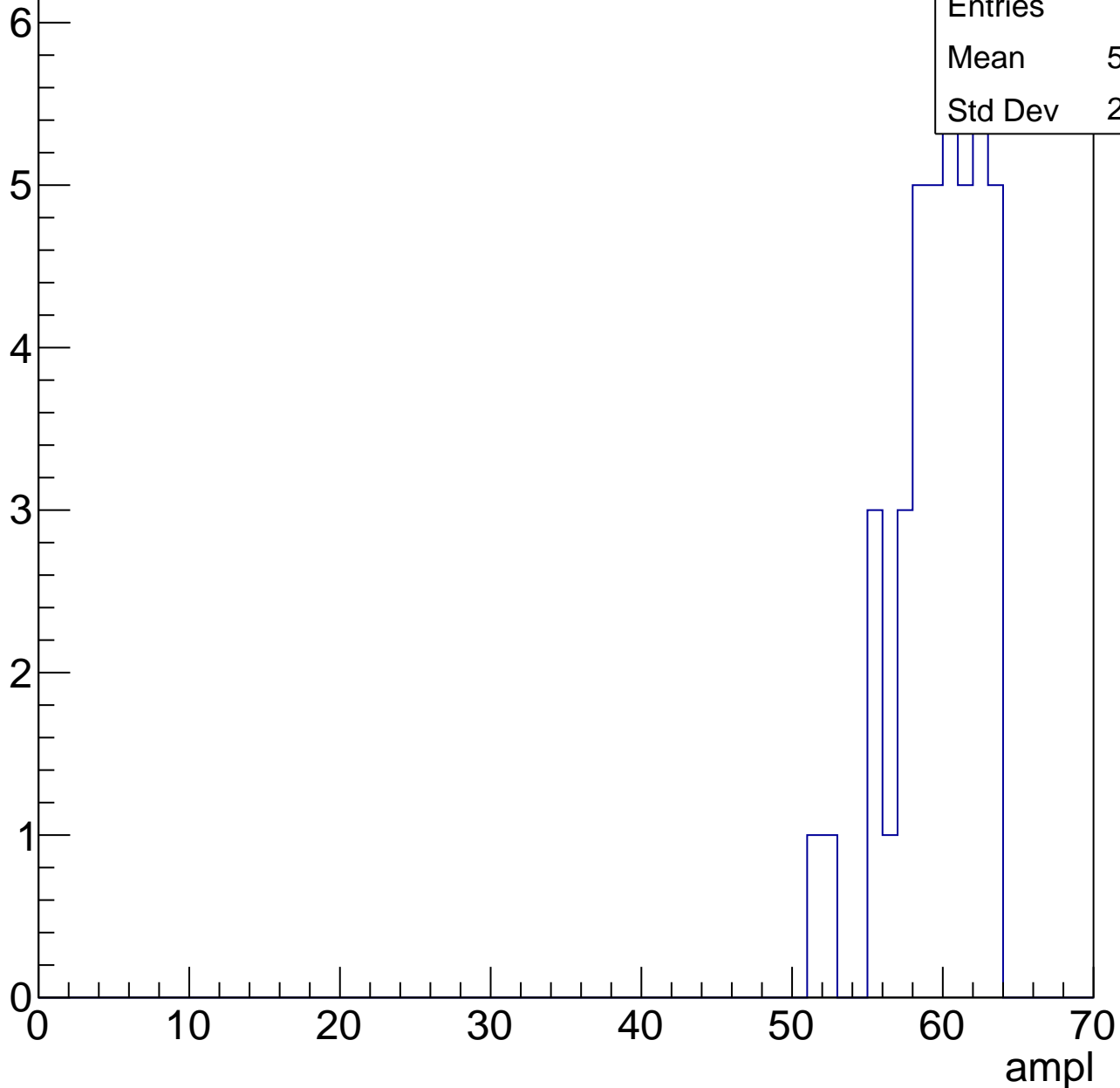
Entries	63
Mean	54.57
Std Dev	7.89



# B1L101S, U9-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

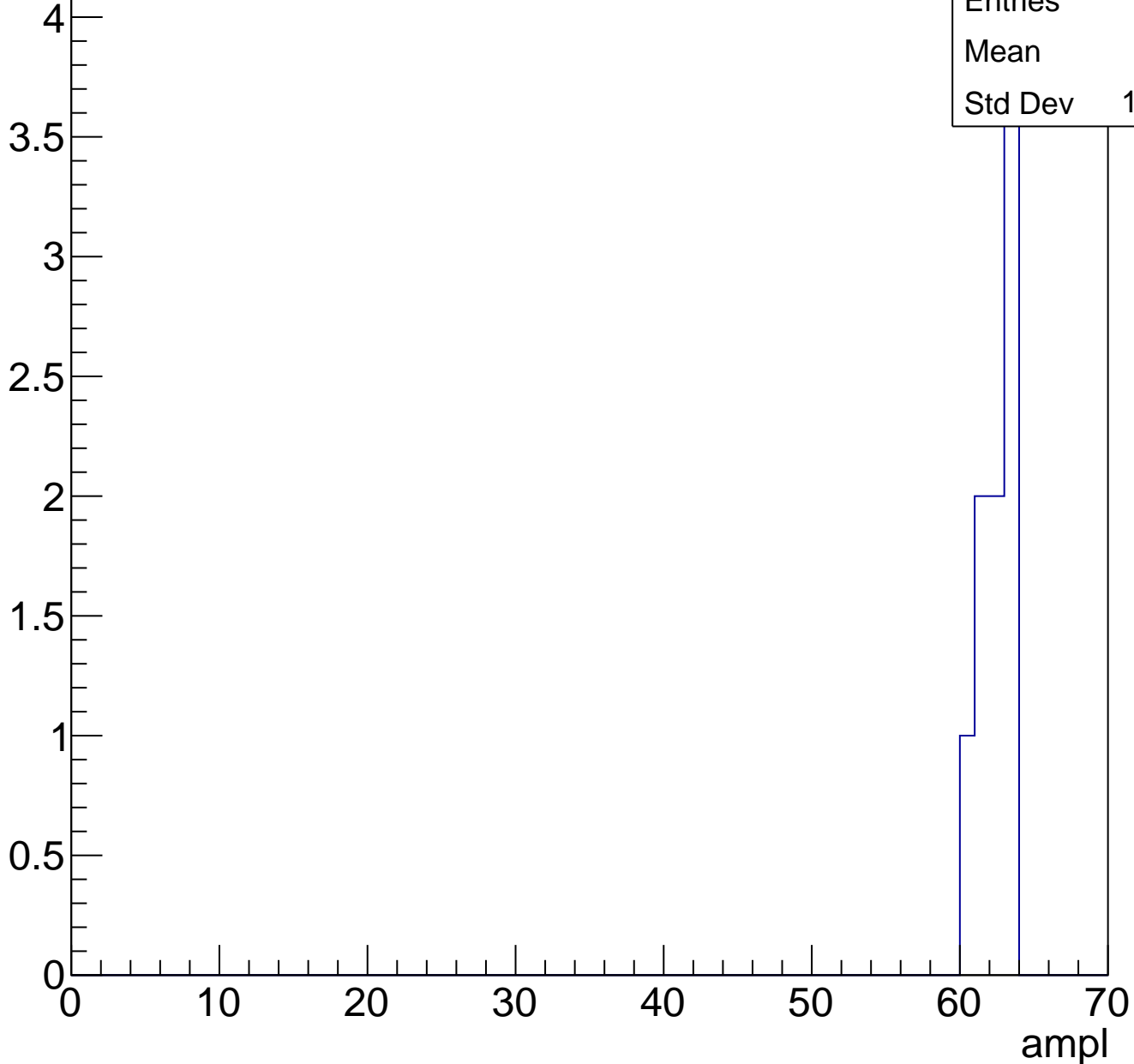
Entry



# B1L101S, U9-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



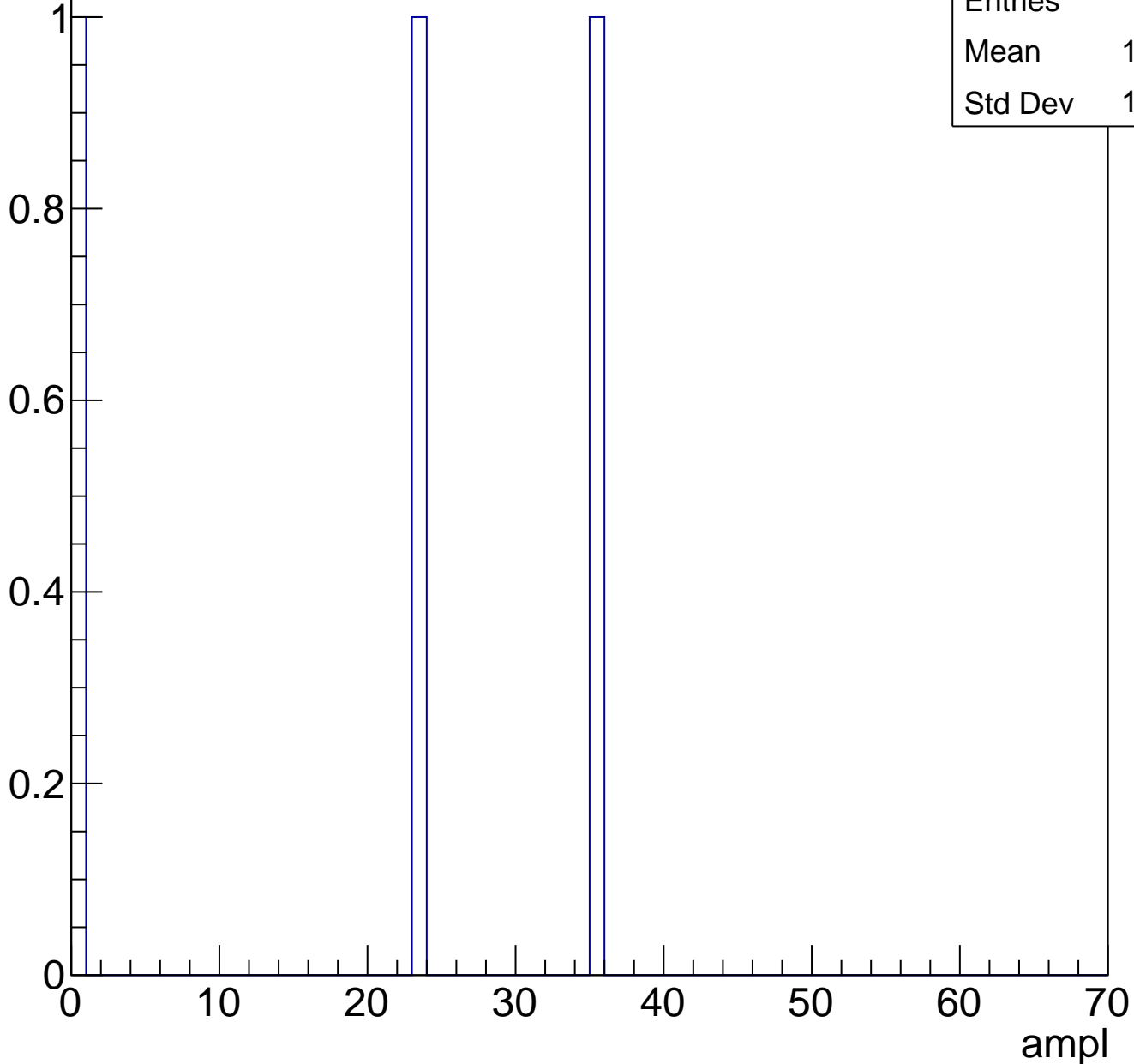
Entries	9
Mean	62
Std Dev	1.054



# B1L101S, U9-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U9-ch124, adc0

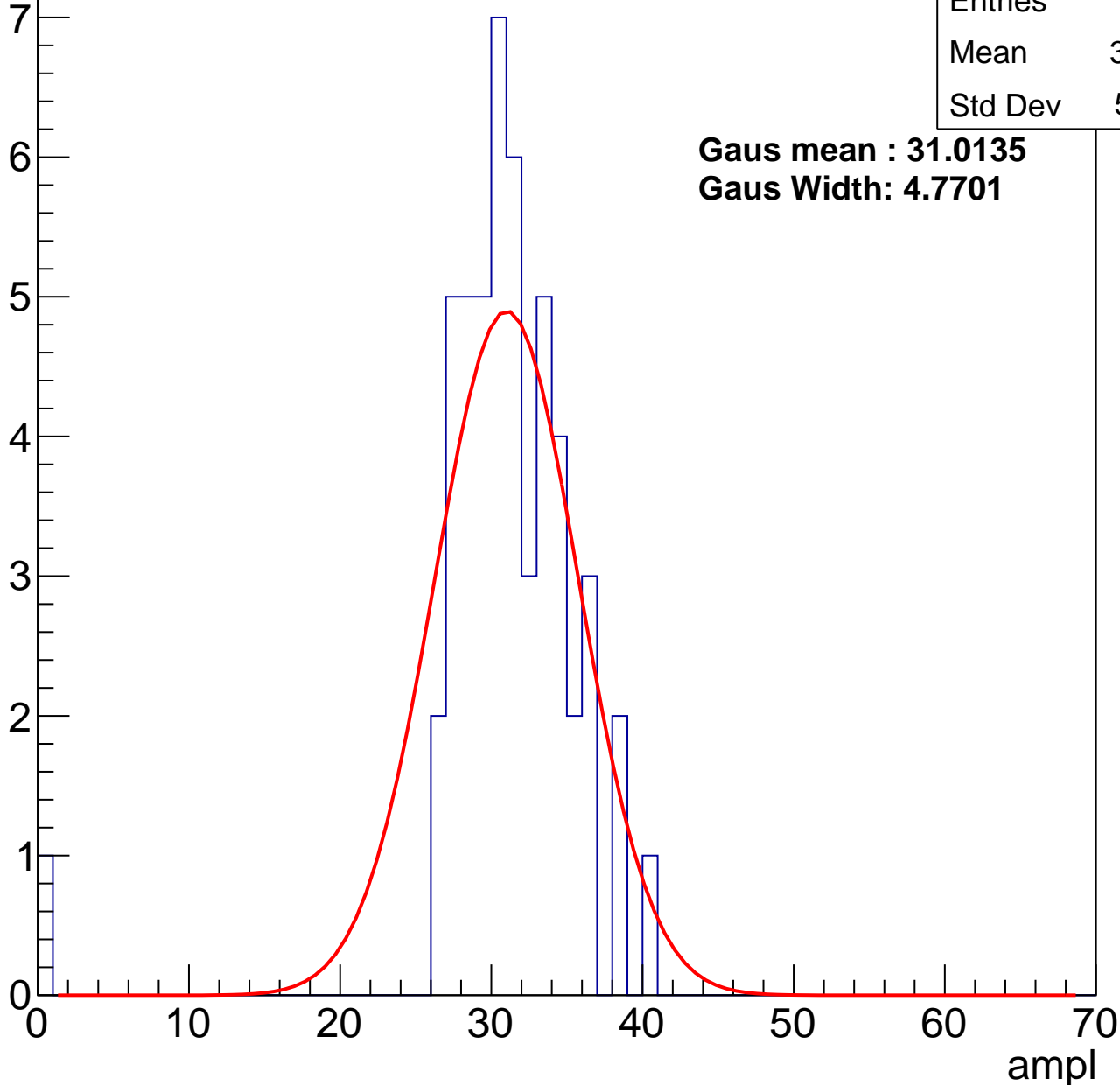
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	30.57
Std Dev	5.421

**Gaus mean : 31.0135**

**Gaus Width: 4.7701**



# B1L101S, U9-ch124, adc1

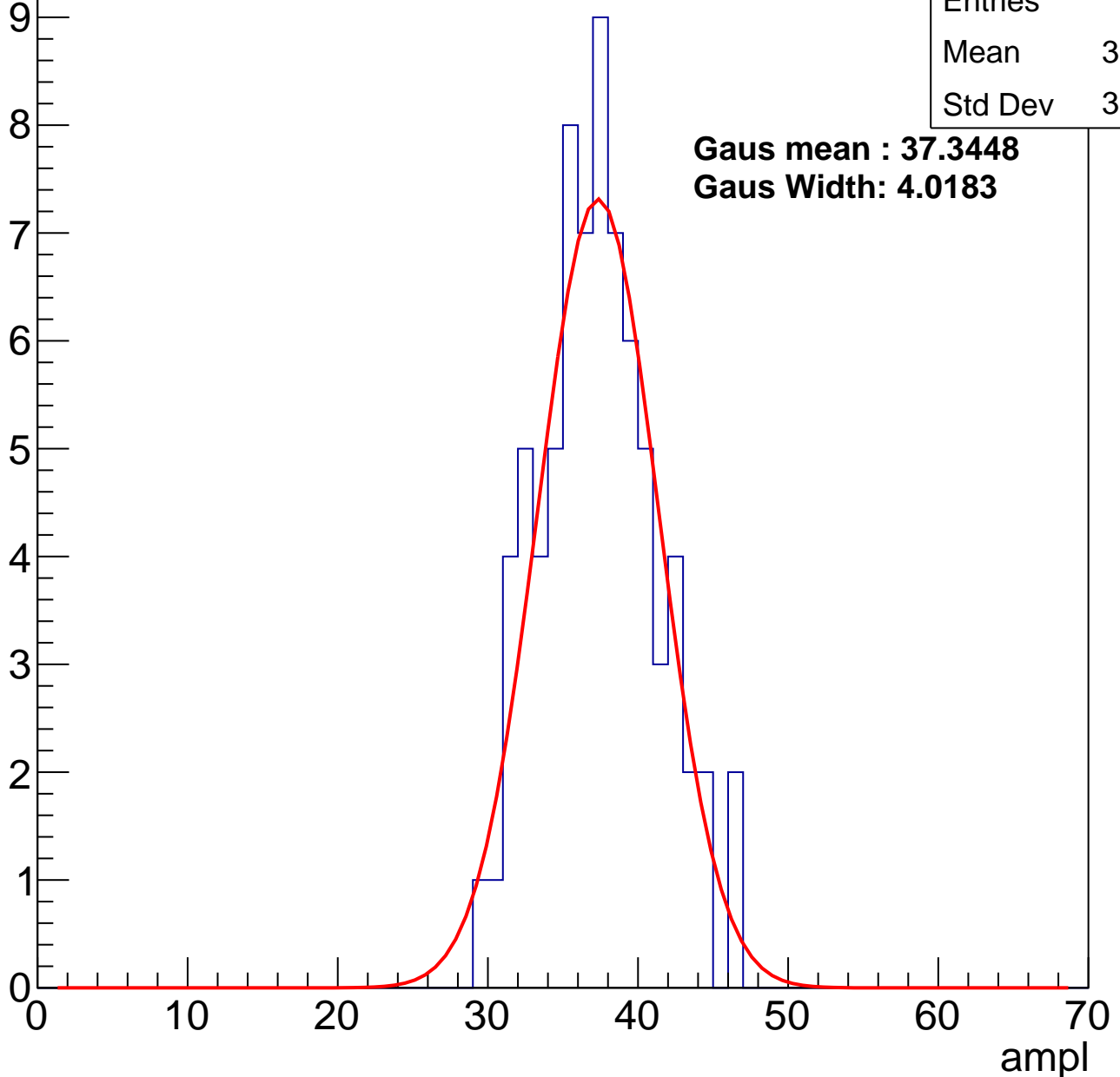
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	36.89
Std Dev	3.804

**Gaus mean : 37.3448**

**Gaus Width: 4.0183**



# B1L101S, U9-ch124, adc2

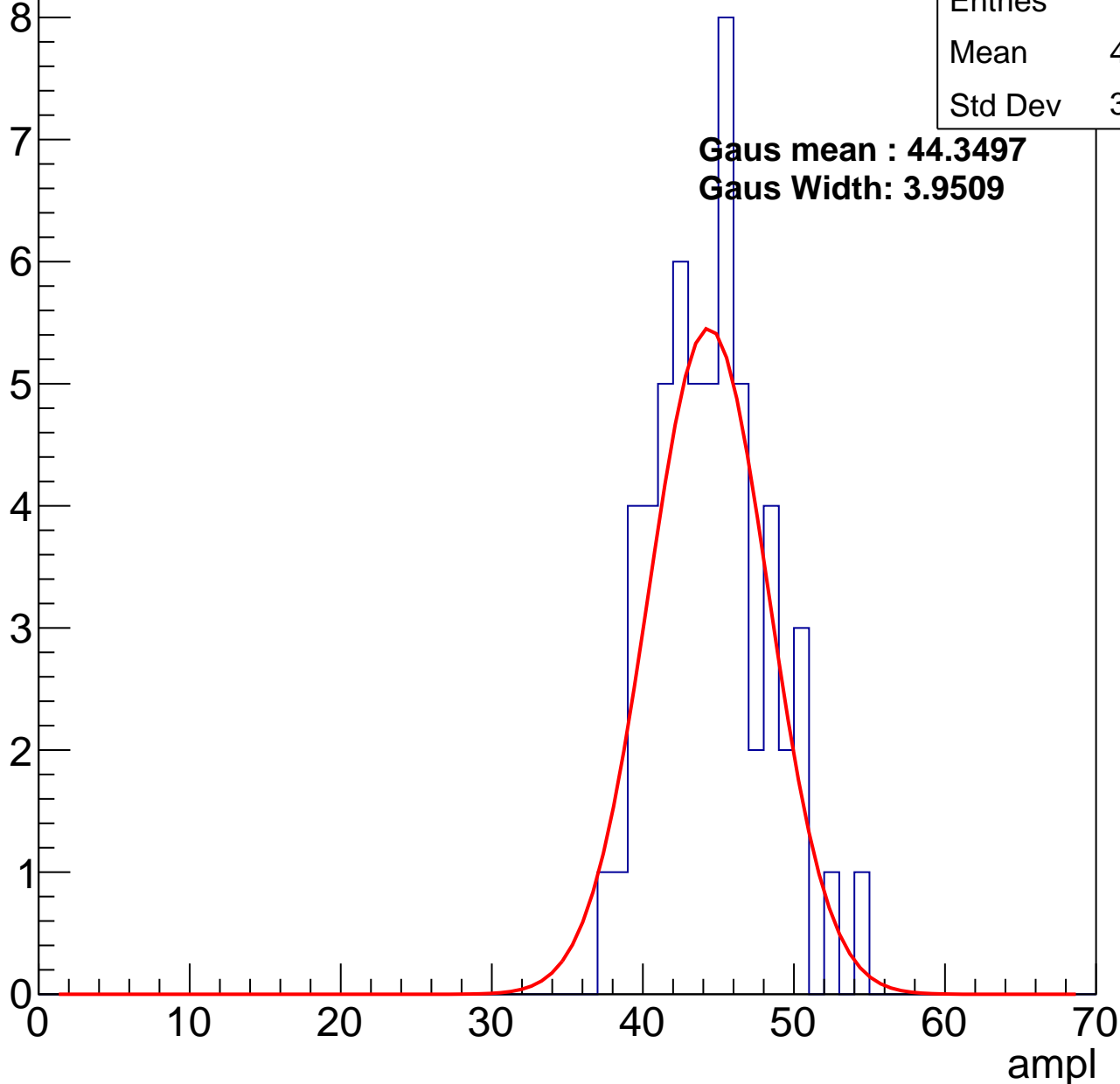
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	44.09
Std Dev	3.638

**Gaus mean : 44.3497**

**Gaus Width: 3.9509**

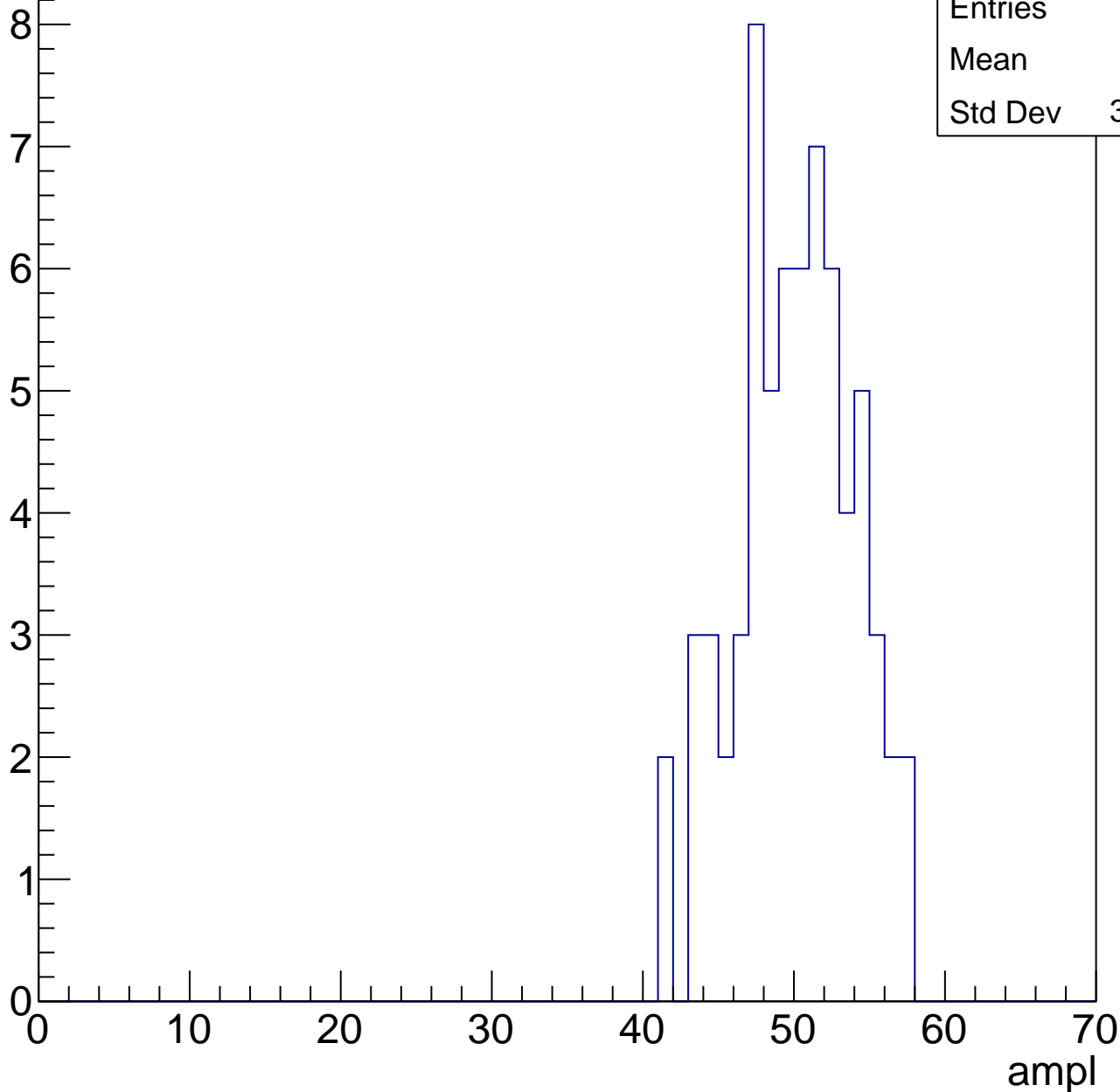


# B1L101S, U9-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	49.6
Std Dev	3.852

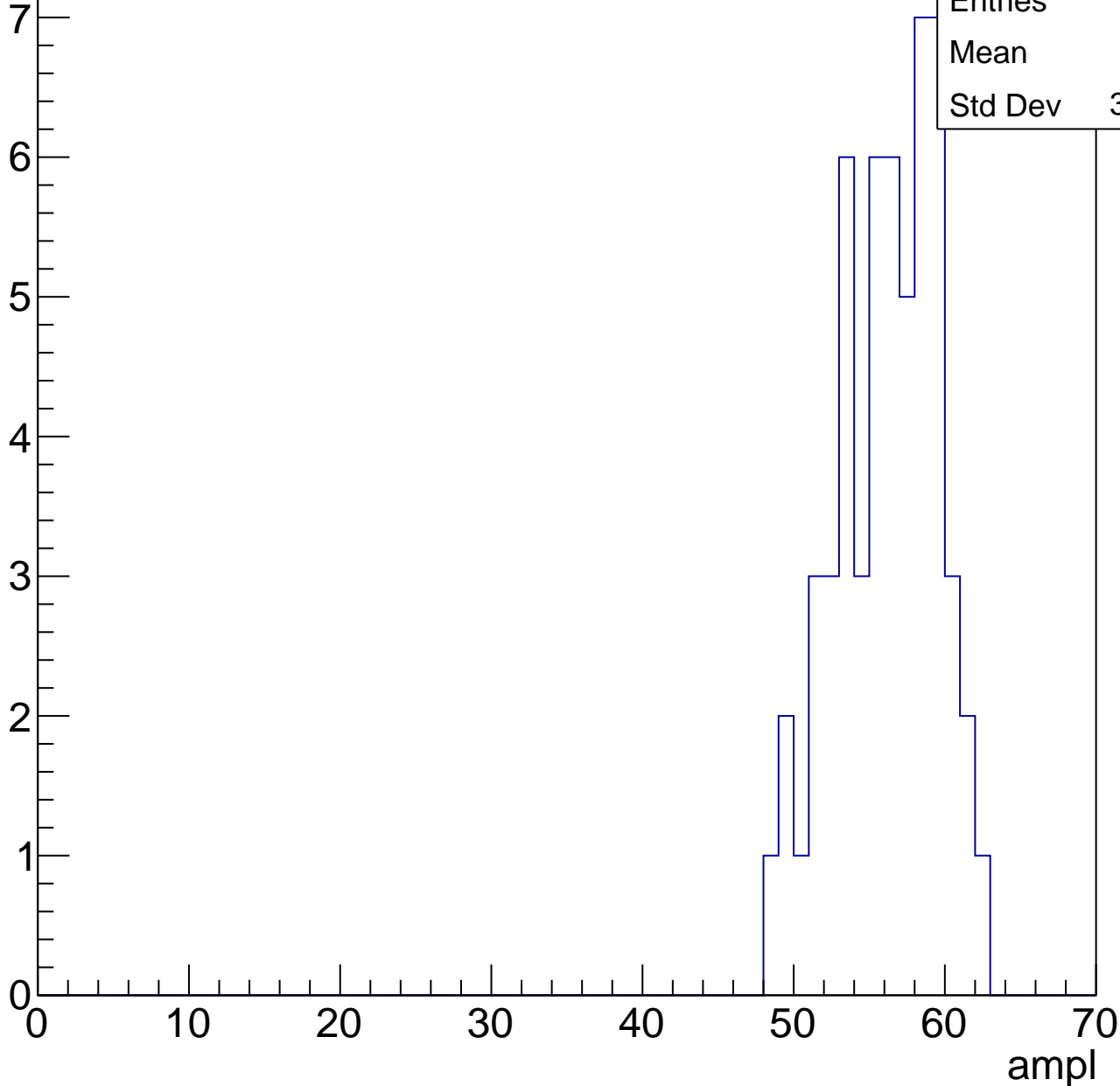


# B1L101S, U9-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	55.7
Std Dev	3.322



# B1L101S, U9-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

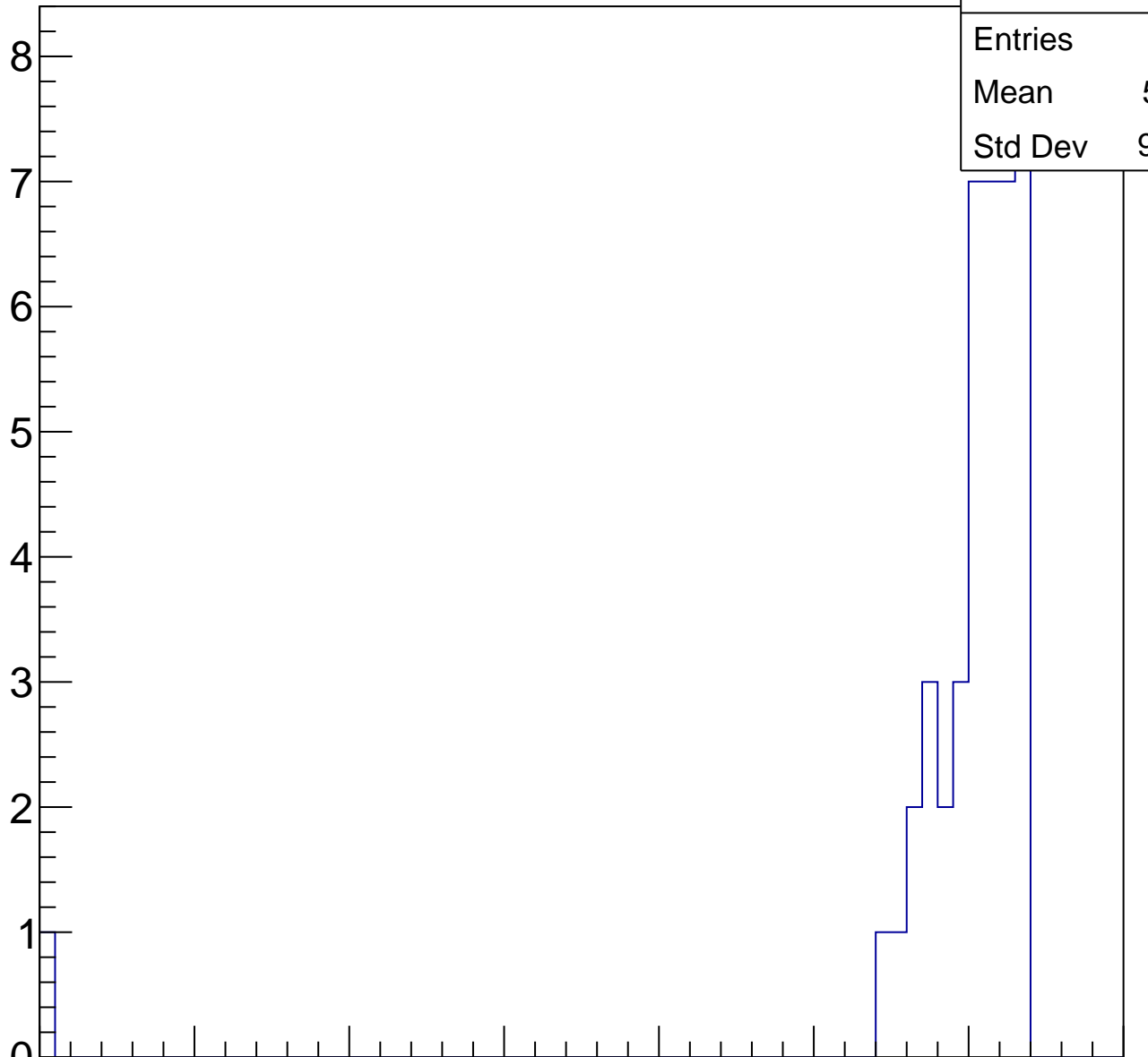
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	42
Mean	58.81
Std Dev	9.485

ampl

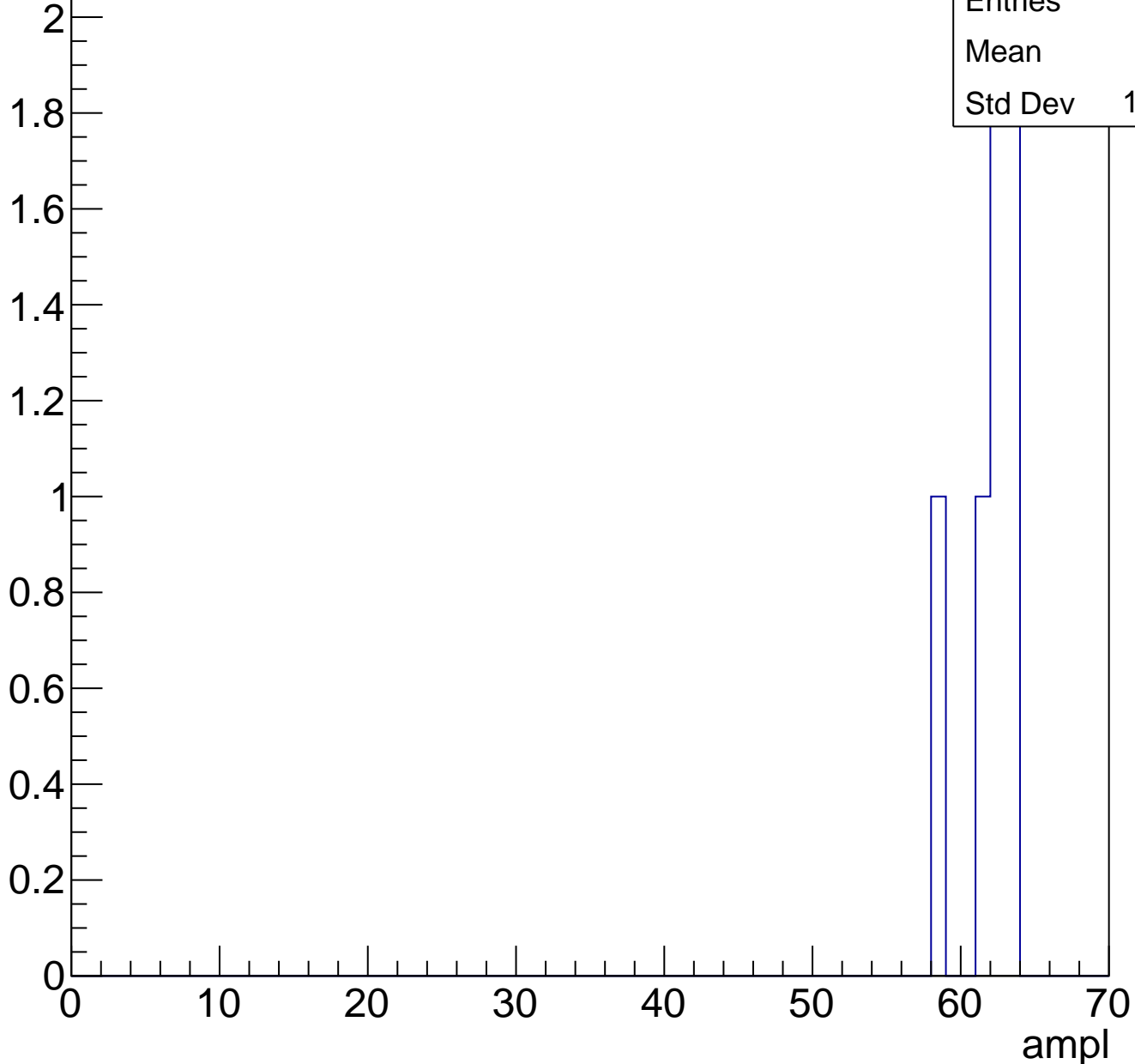
0 10 20 30 40 50 60 70



# B1L101S, U9-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

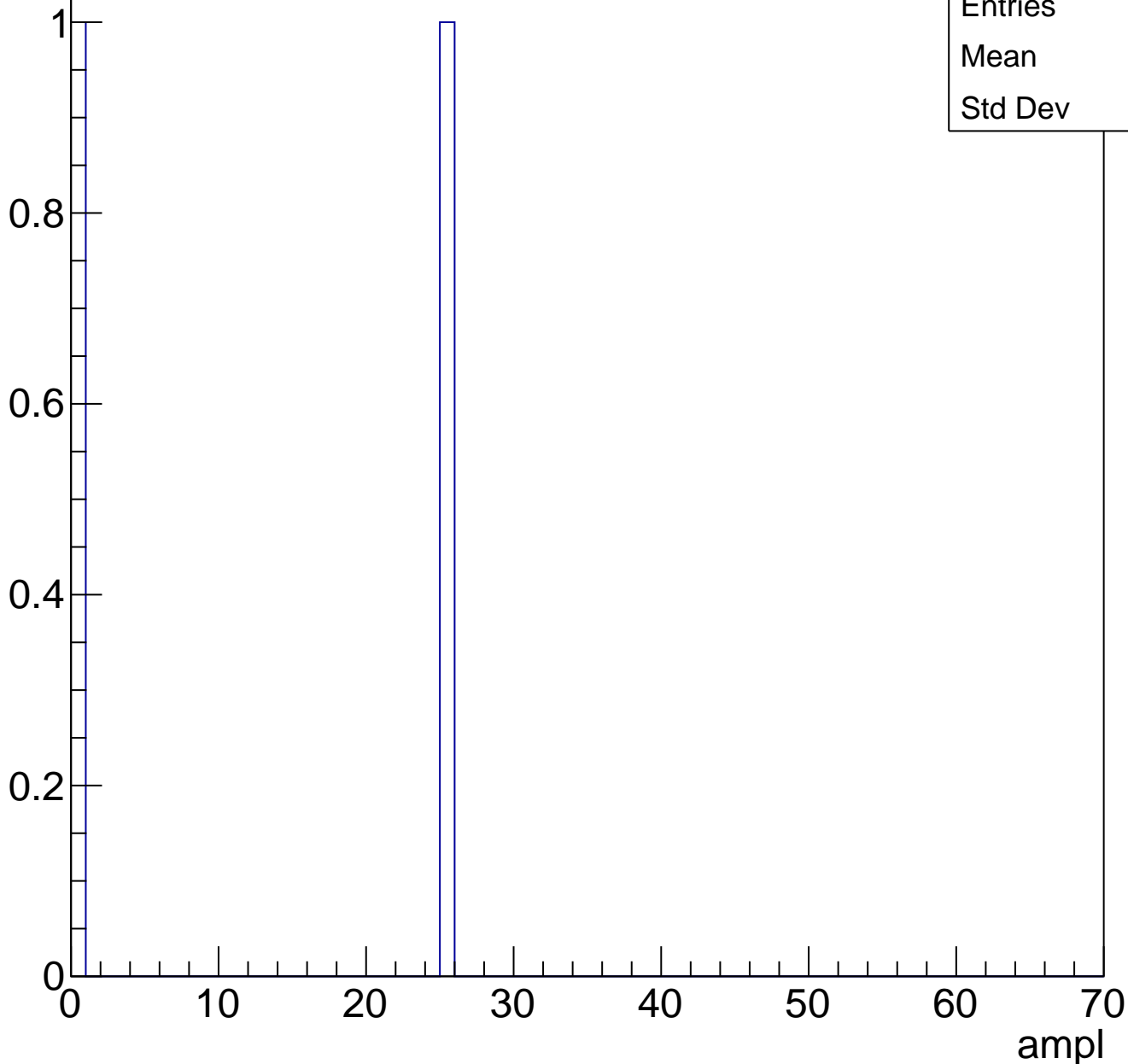




# B1L101S, U9-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	12.5
Std Dev	12.5

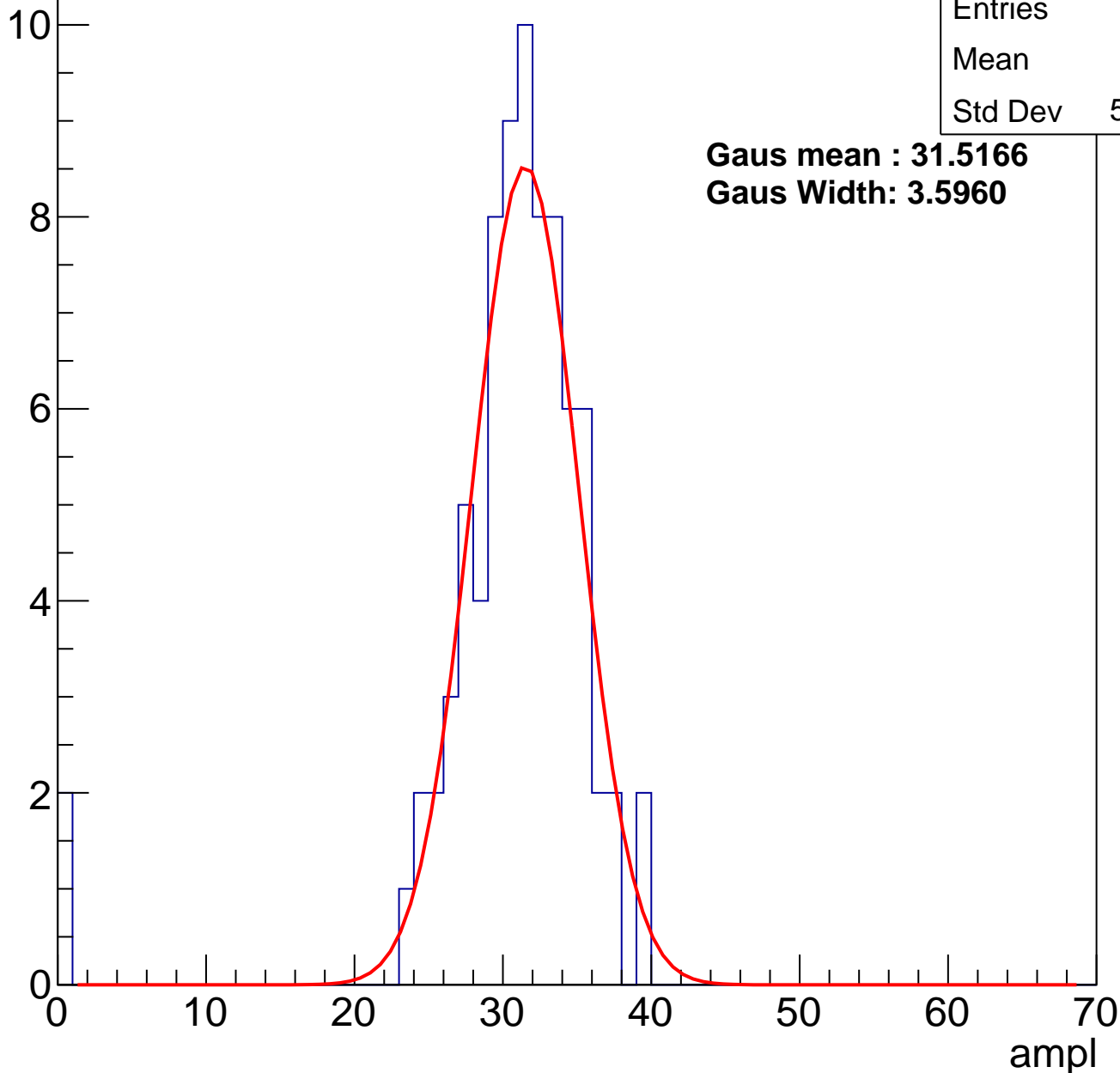
# B1L101S, U9-ch125, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	80
Mean	30.2
Std Dev	5.892

**Gaus mean : 31.5166**  
**Gaus Width: 3.5960**

Entry



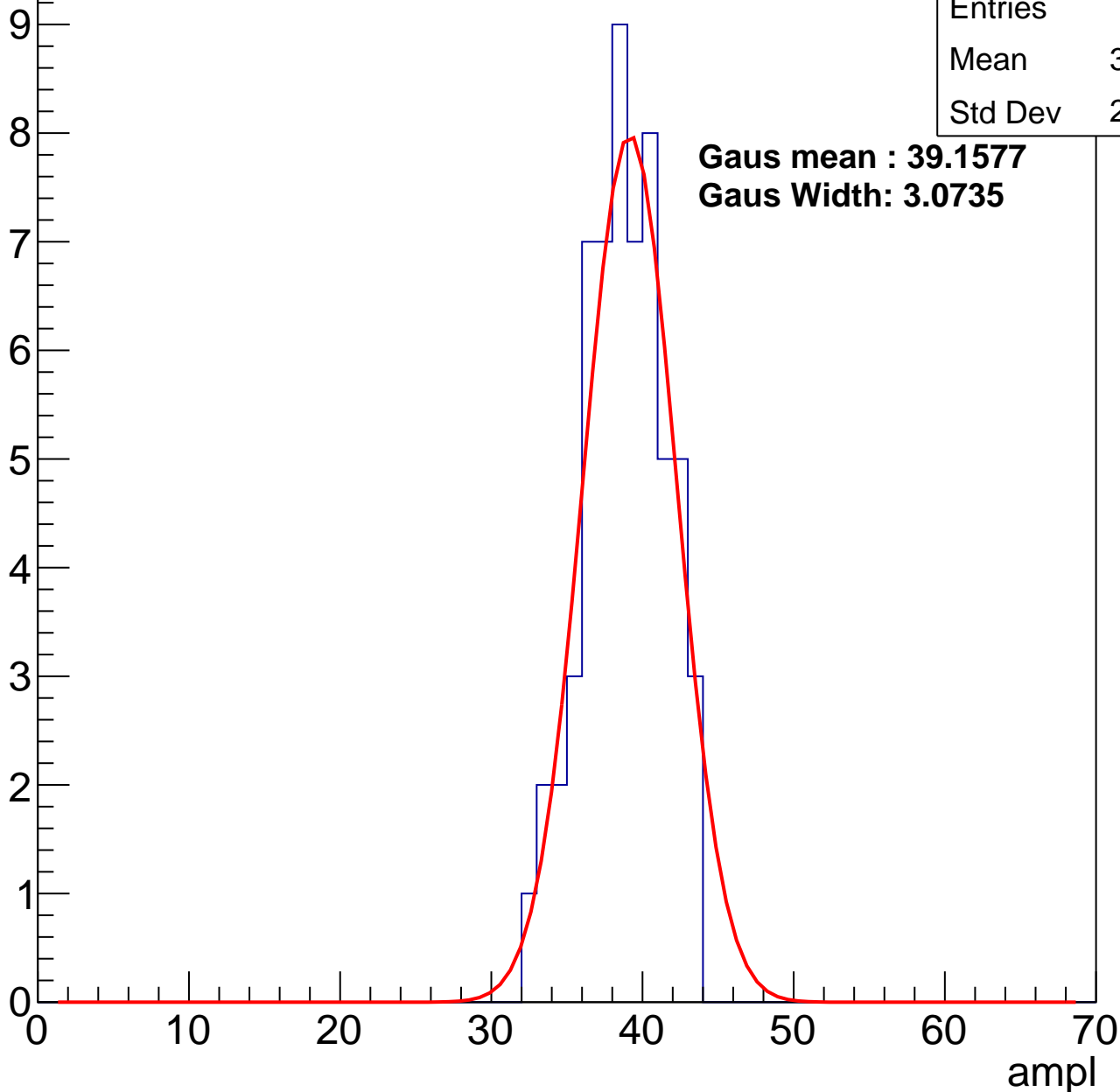
# B1L101S, U9-ch125, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	38.32
Std Dev	2.645

**Gaus mean : 39.1577**  
**Gaus Width: 3.0735**



# B1L101S, U9-ch125, adc2

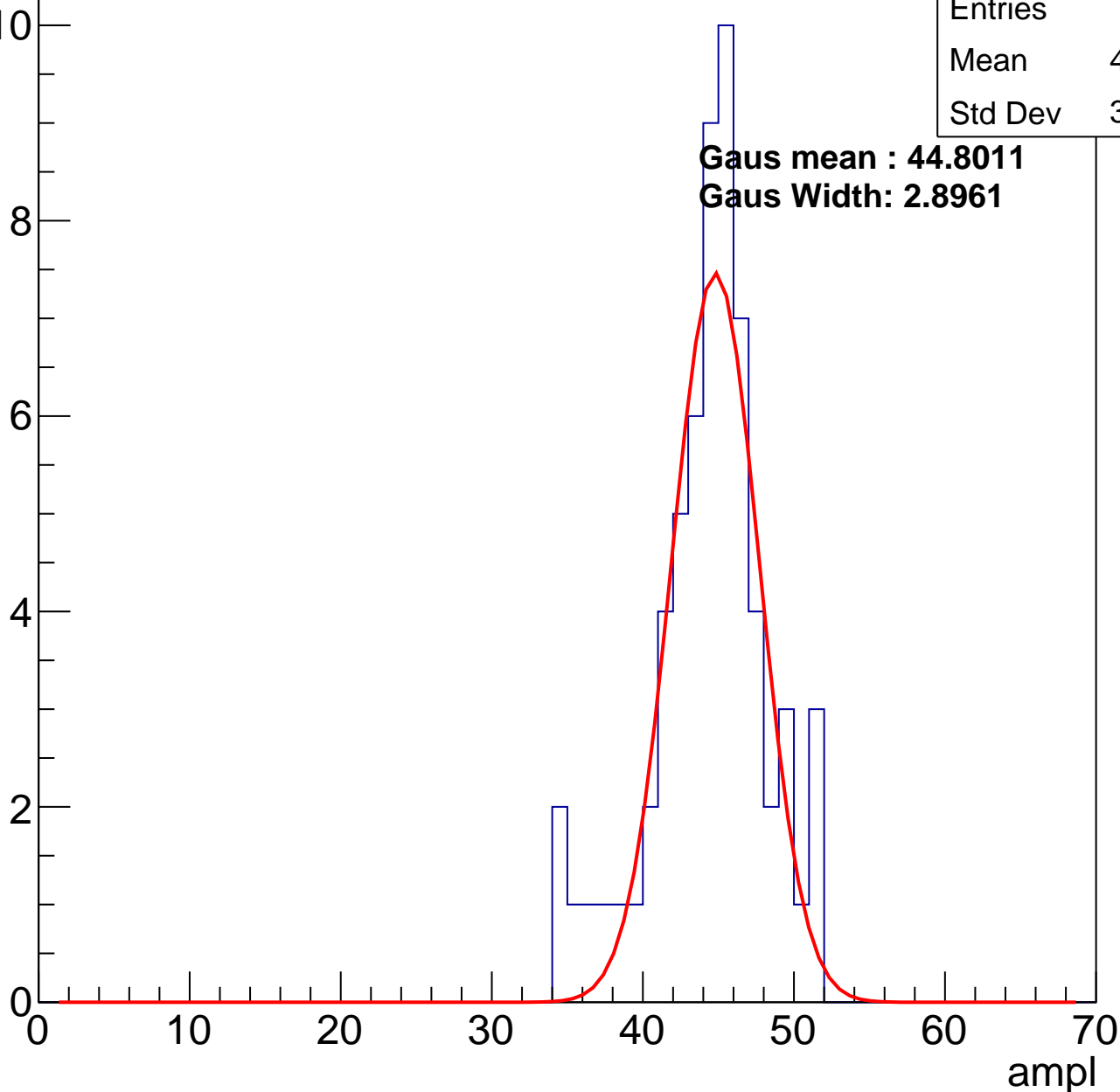
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	43.92
Std Dev	3.806

**Gaus mean : 44.8011**

**Gaus Width: 2.8961**

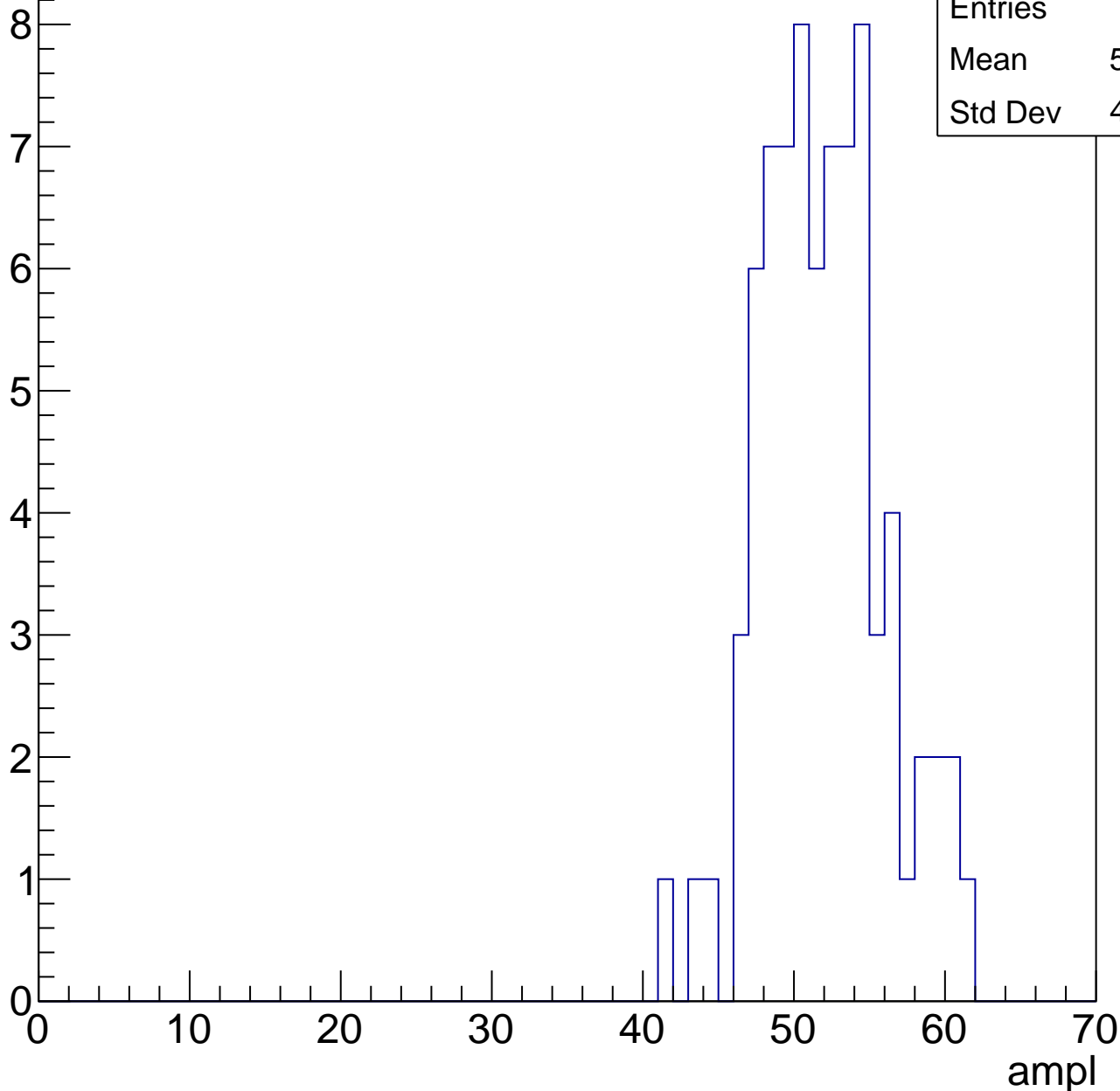


# B1L101S, U9-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	51.44
Std Dev	4.024

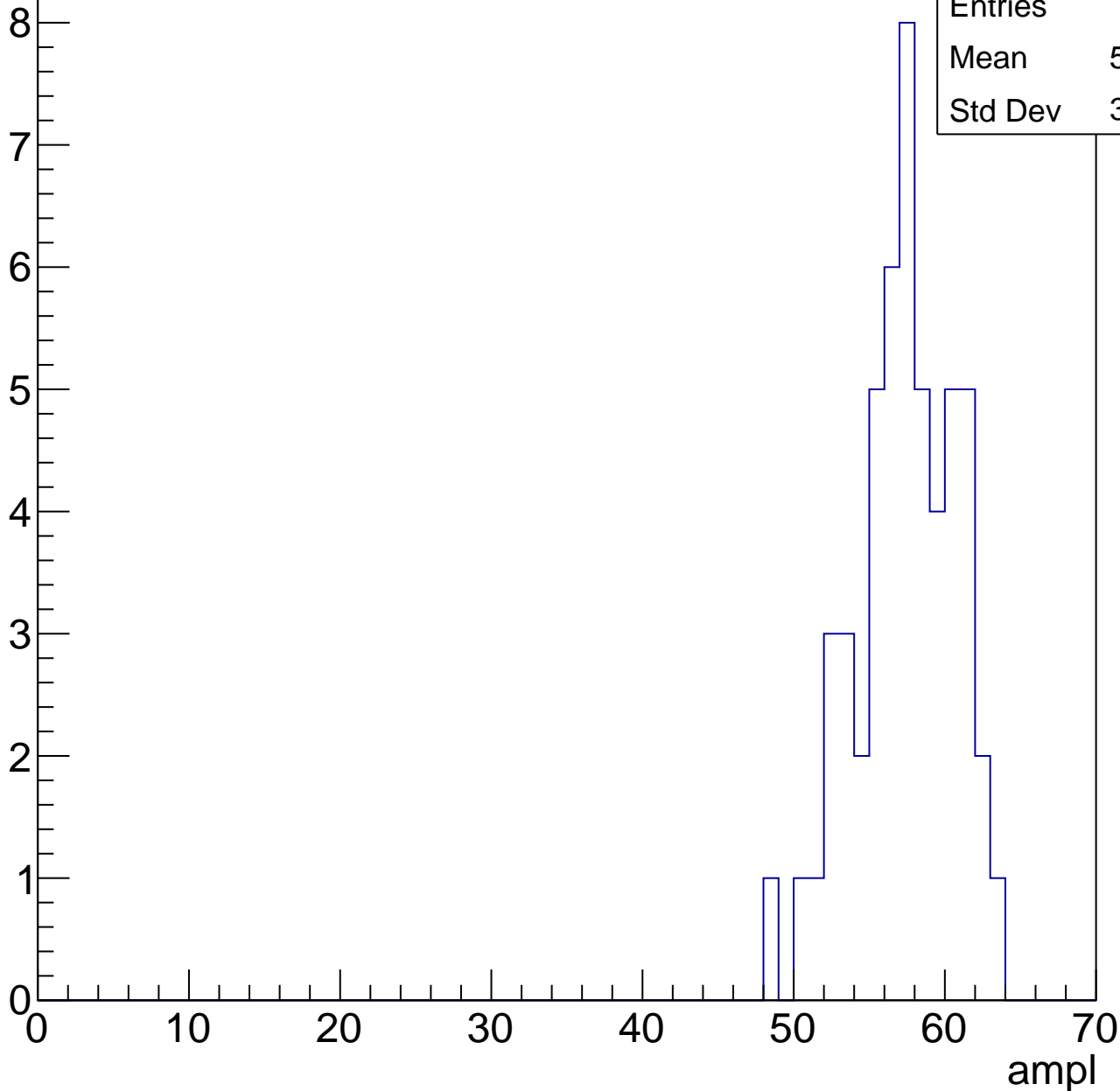


# B1L101S, U9-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	56.87
Std Dev	3.294

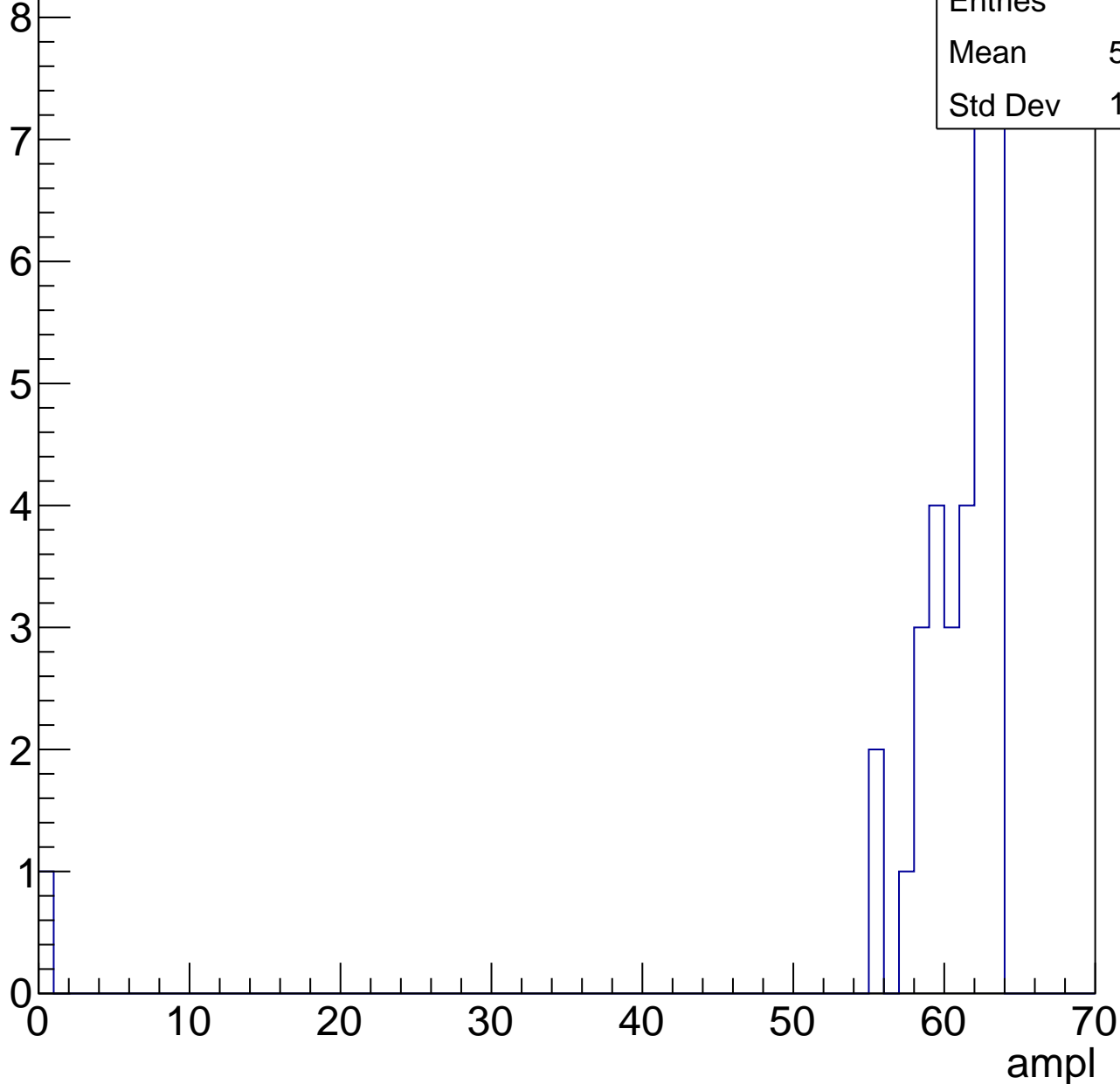


# B1L101S, U9-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	34
Mean	58.85
Std Dev	10.49



# B1L101S, U9-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U9-ch126, adc0

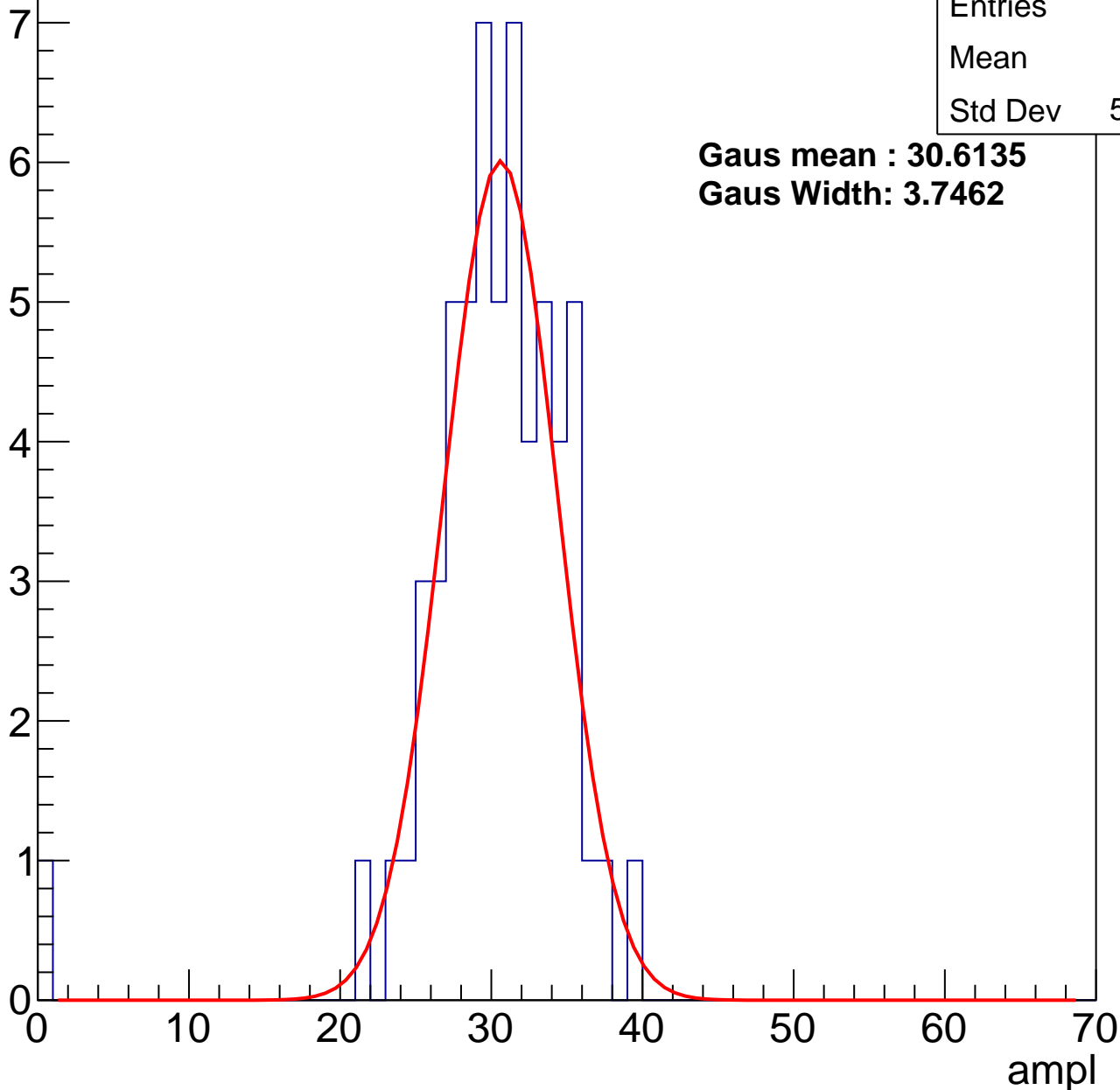
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	29.7
Std Dev	5.289

**Gaus mean : 30.6135**

**Gaus Width: 3.7462**



# B1L101S, U9-ch126, adc1

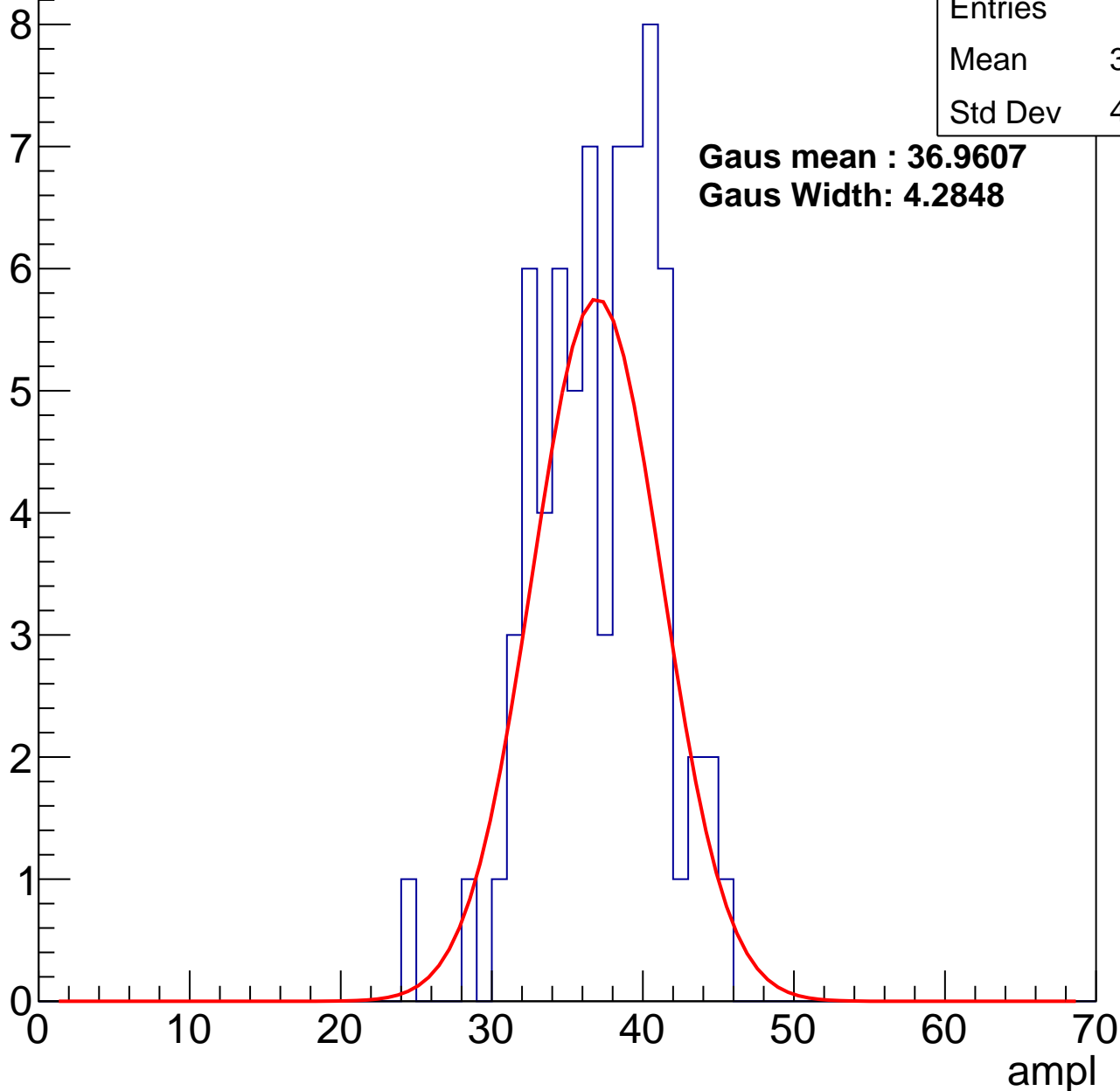
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	36.72
Std Dev	4.039

**Gaus mean : 36.9607**

**Gaus Width: 4.2848**



# B1L101S, U9-ch126, adc2

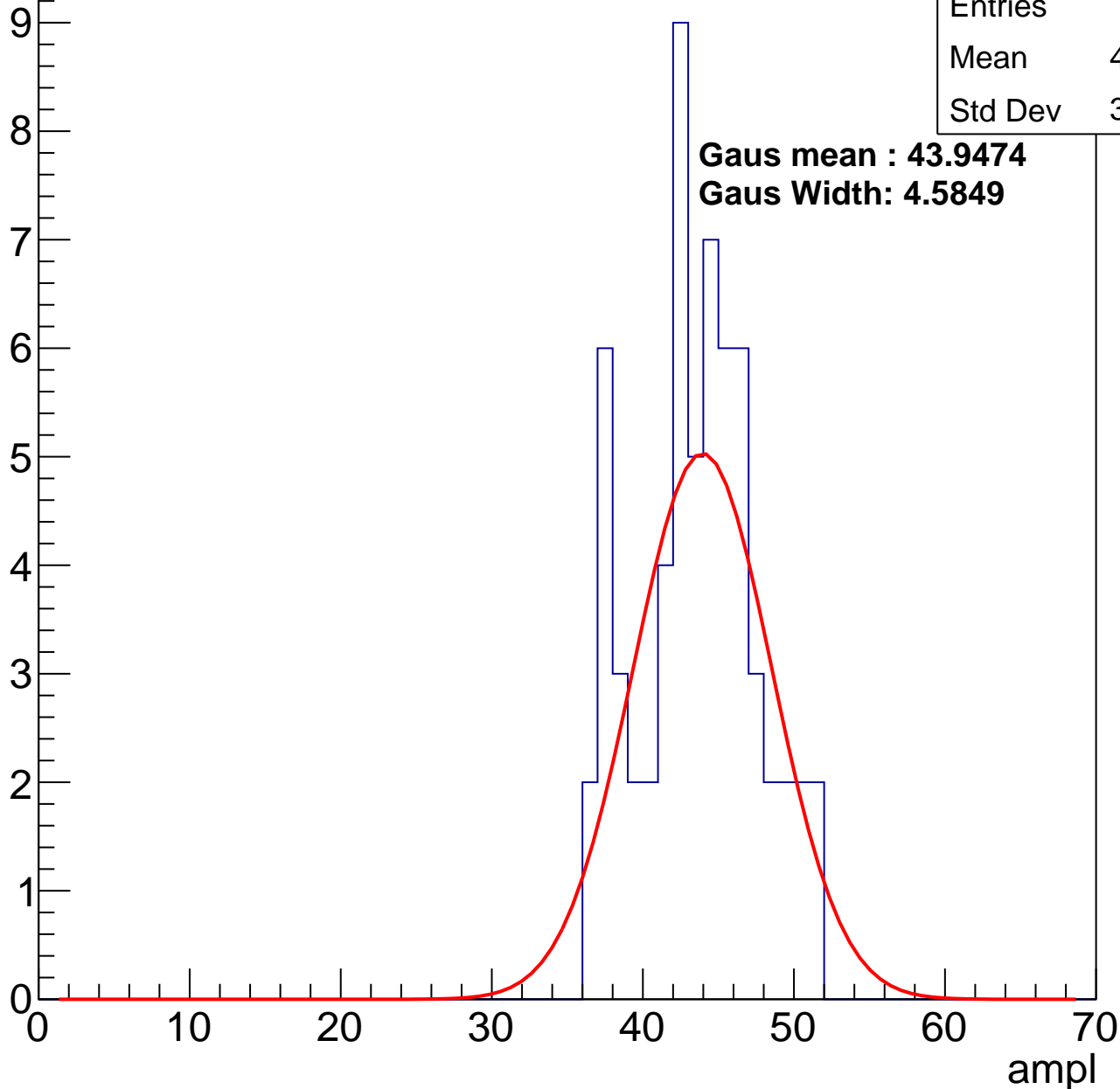
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	43.08
Std Dev	3.872

**Gaus mean : 43.9474**

**Gaus Width: 4.5849**

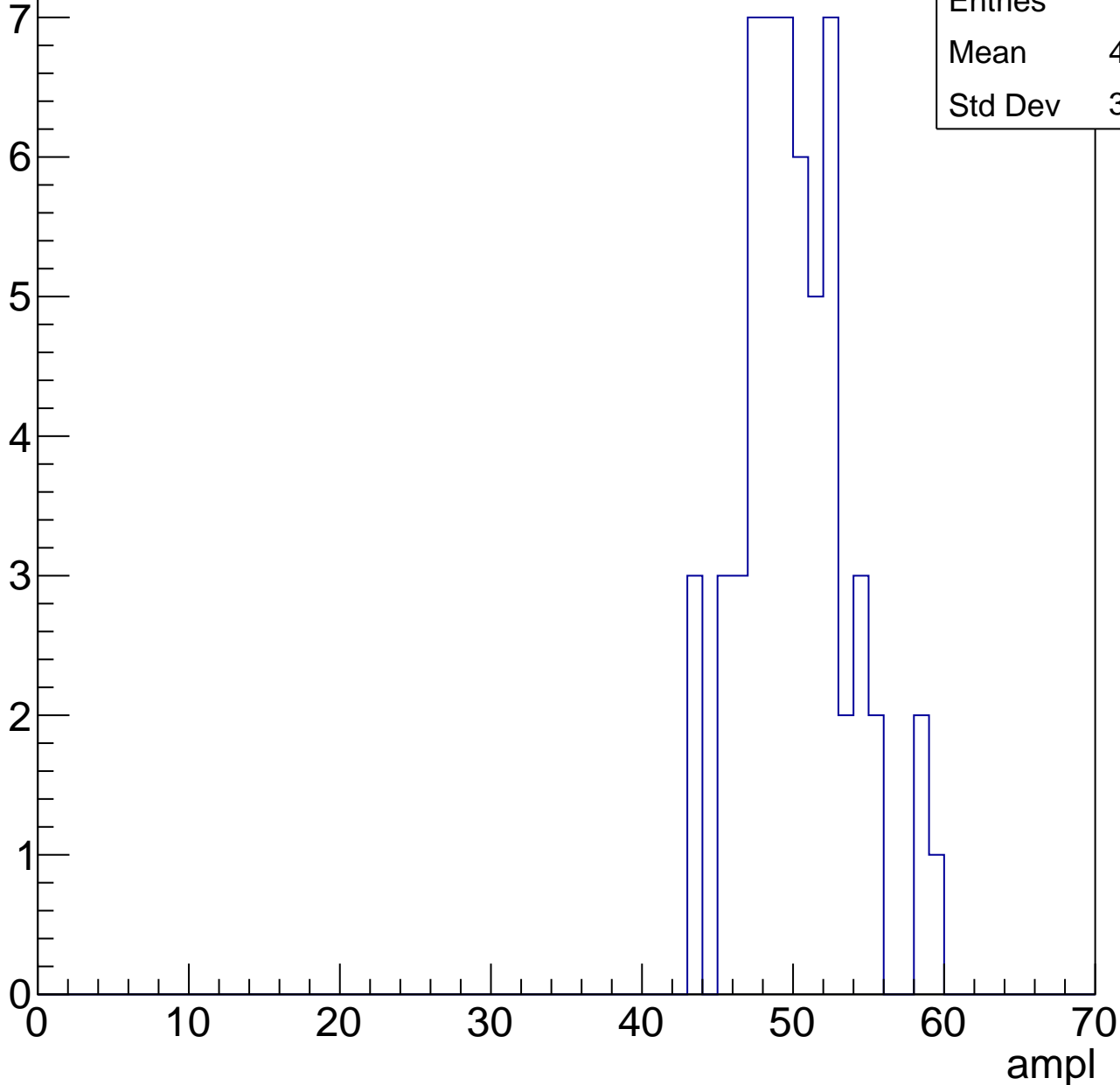


# B1L101S, U9-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	49.69
Std Dev	3.524

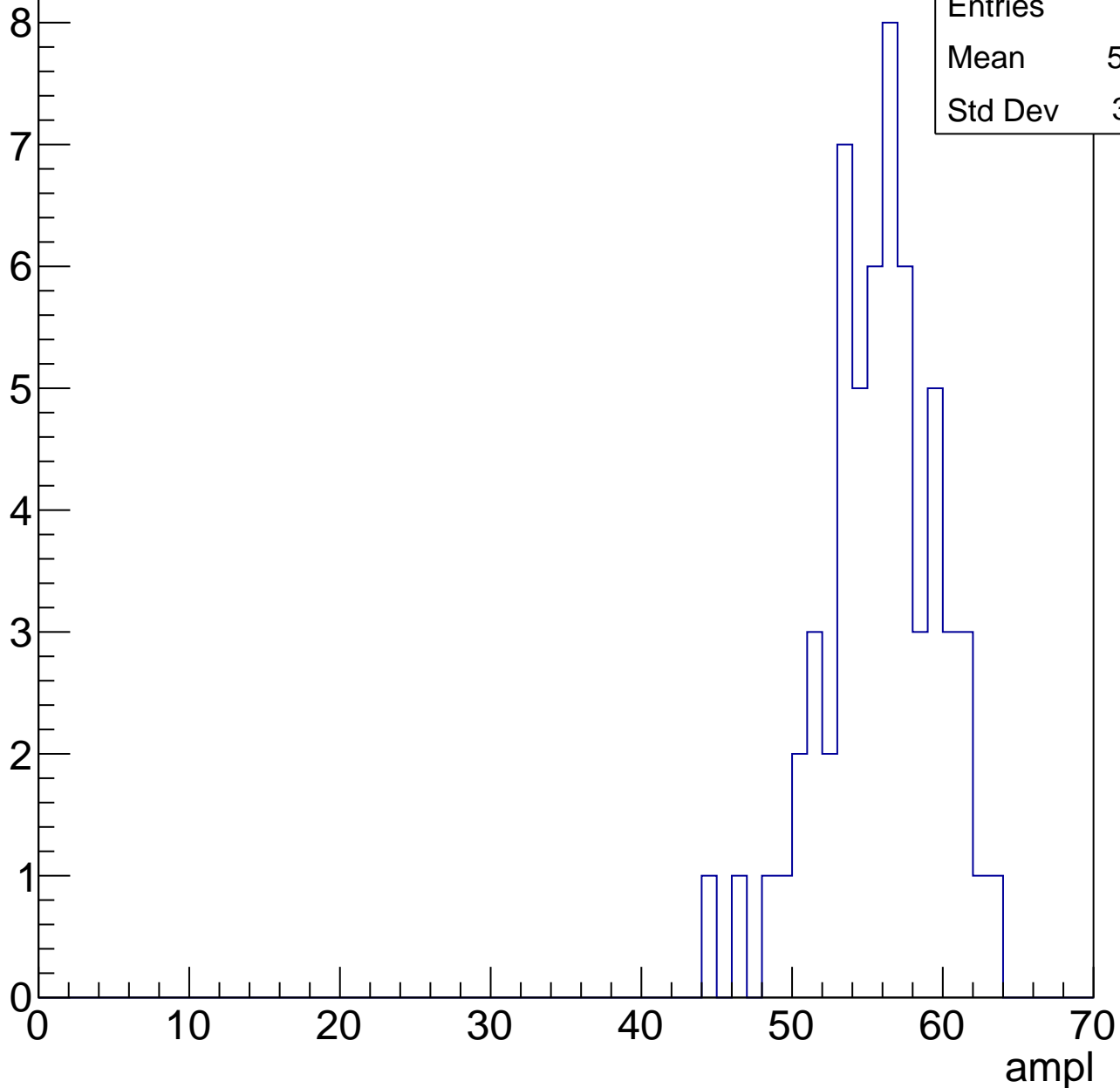


# B1L101S, U9-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	55.29
Std Dev	3.831



# B1L101S, U9-ch126, adc5

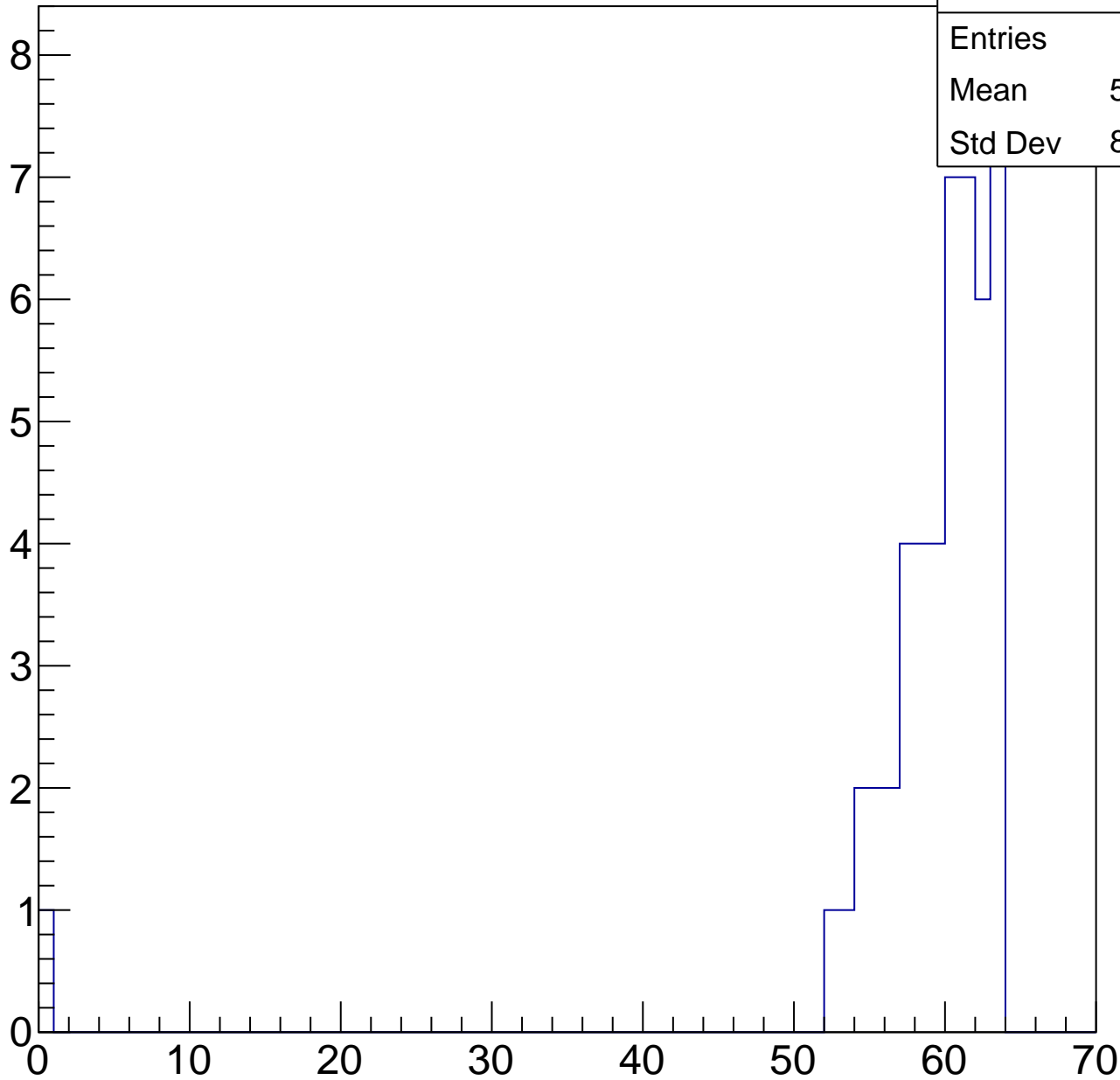
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	58.24
Std Dev	8.893

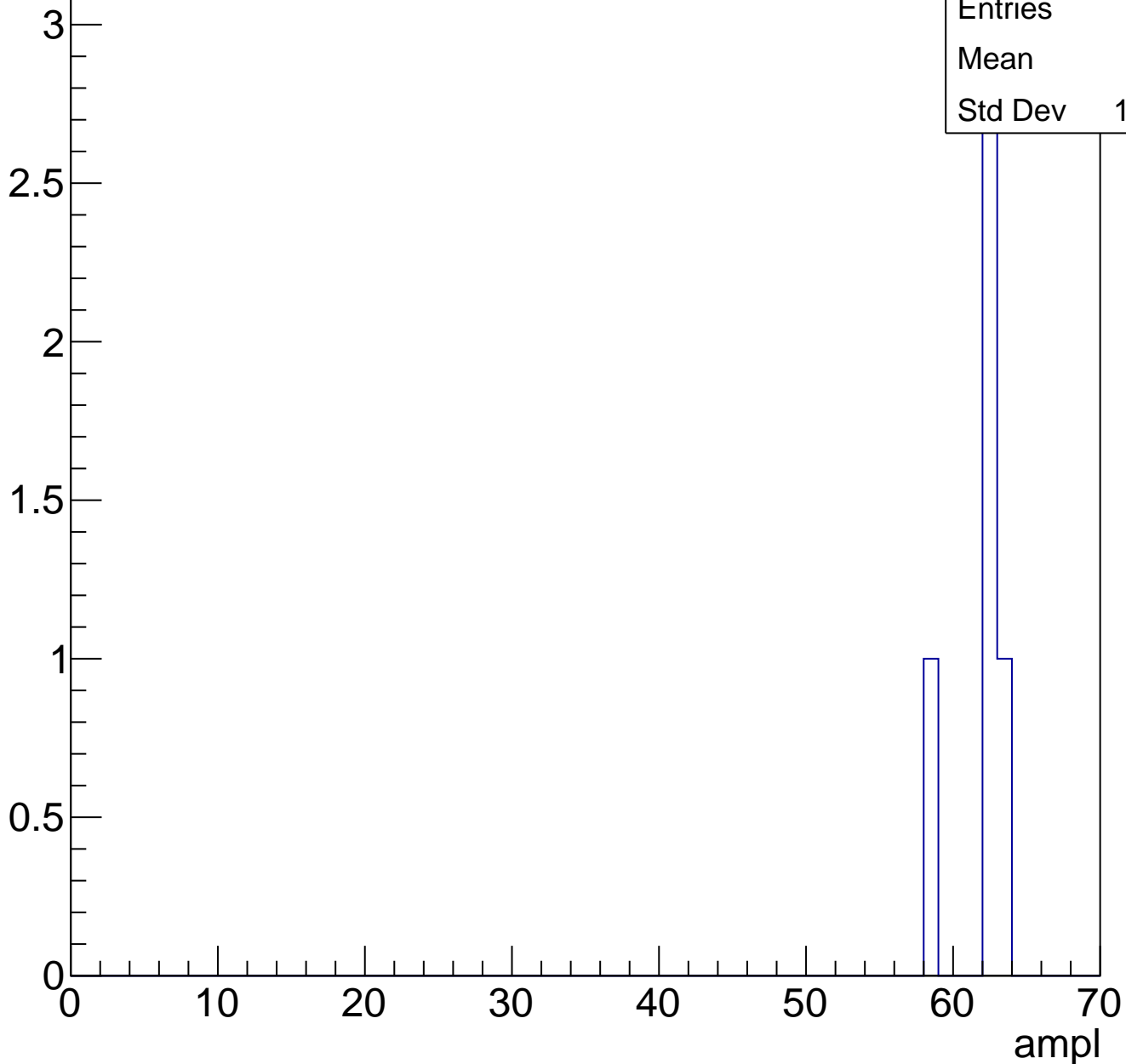
ampl



# B1L101S, U9-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U9-ch127, adc0

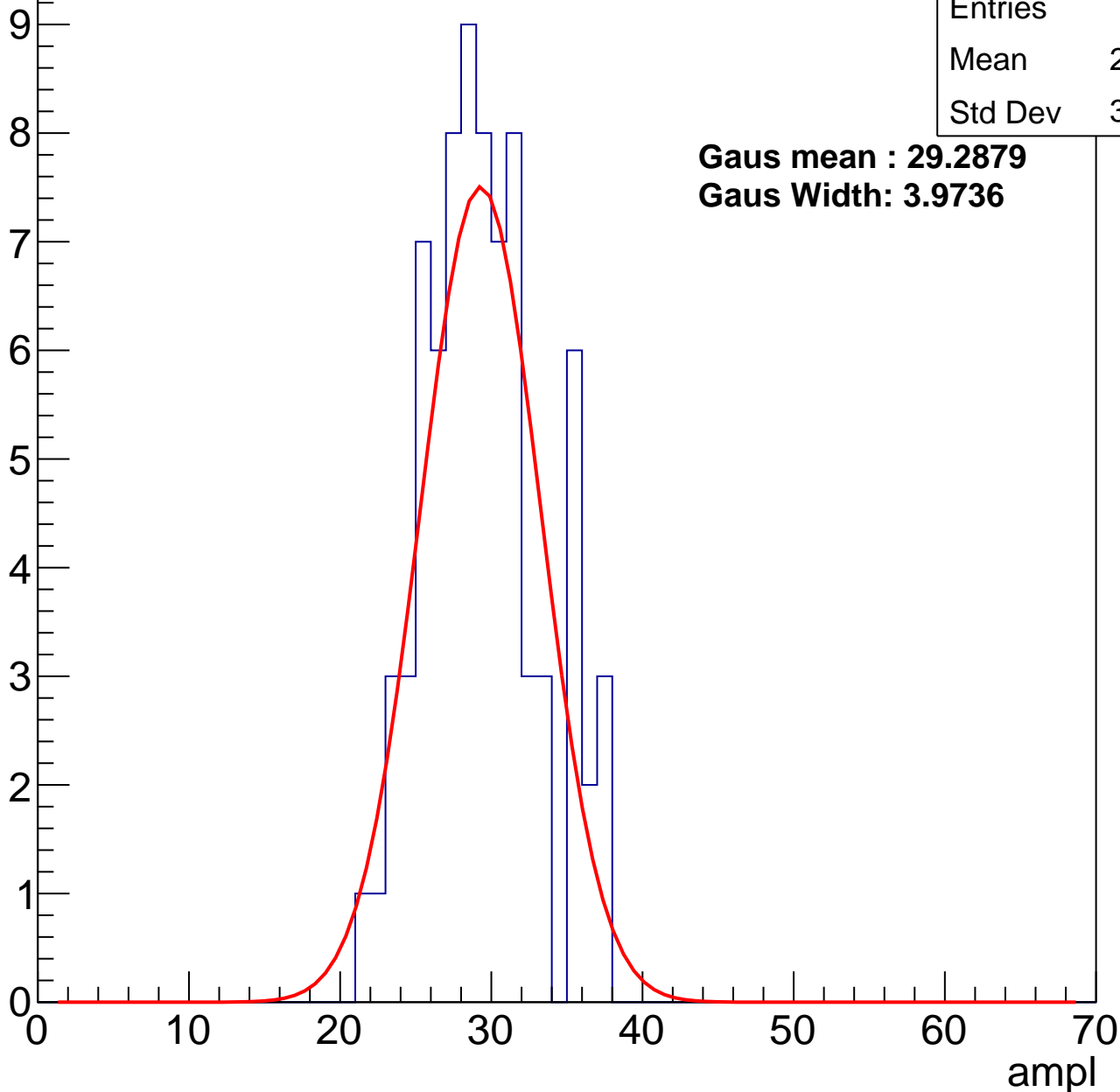
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	28.99
Std Dev	3.794

**Gaus mean : 29.2879**

**Gaus Width: 3.9736**



# B1L101S, U9-ch127, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	70
Mean	36.39
Std Dev	3.591

**Gaus mean : 36.8175**

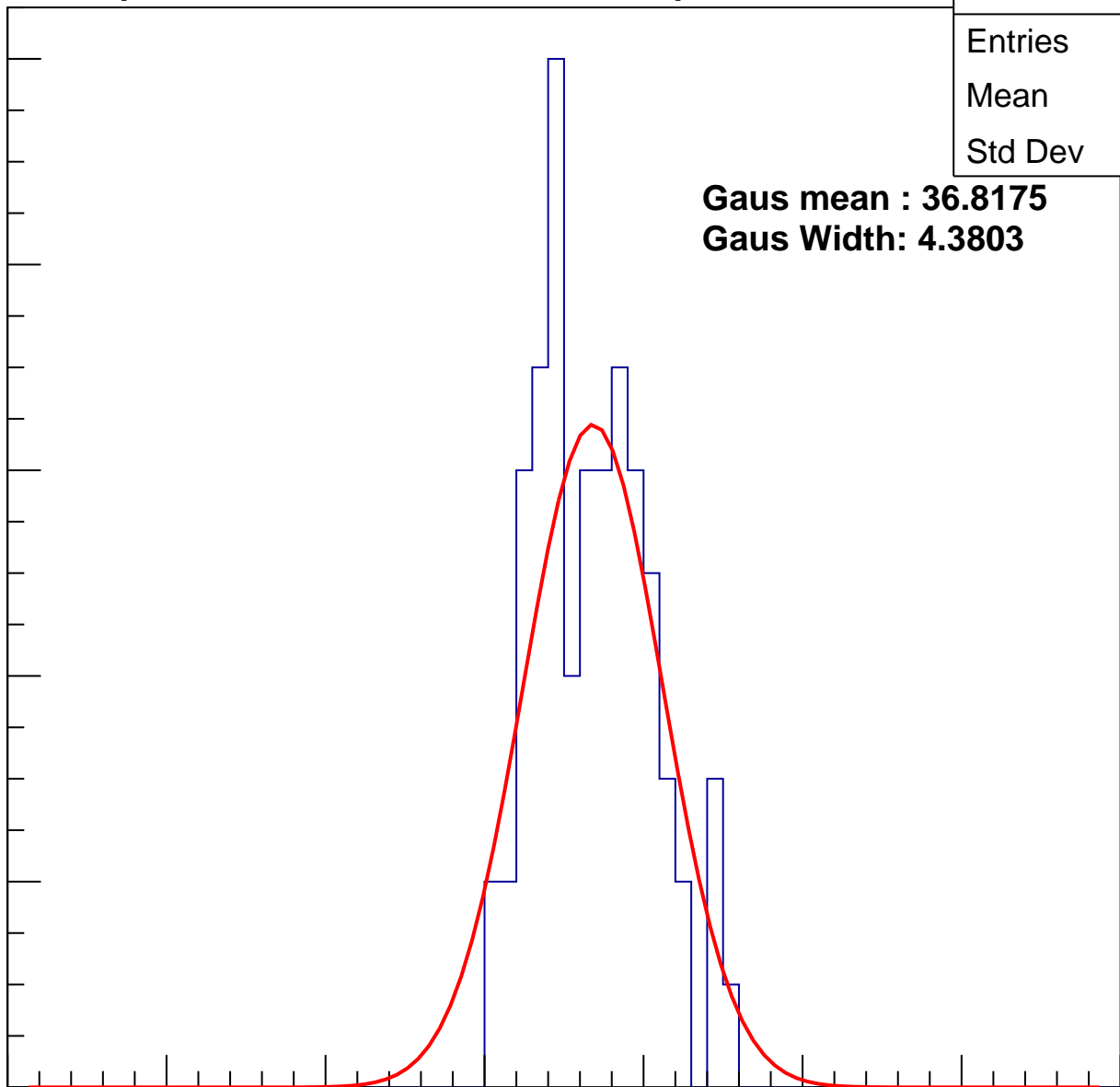
**Gaus Width: 4.3803**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U9-ch127, adc2

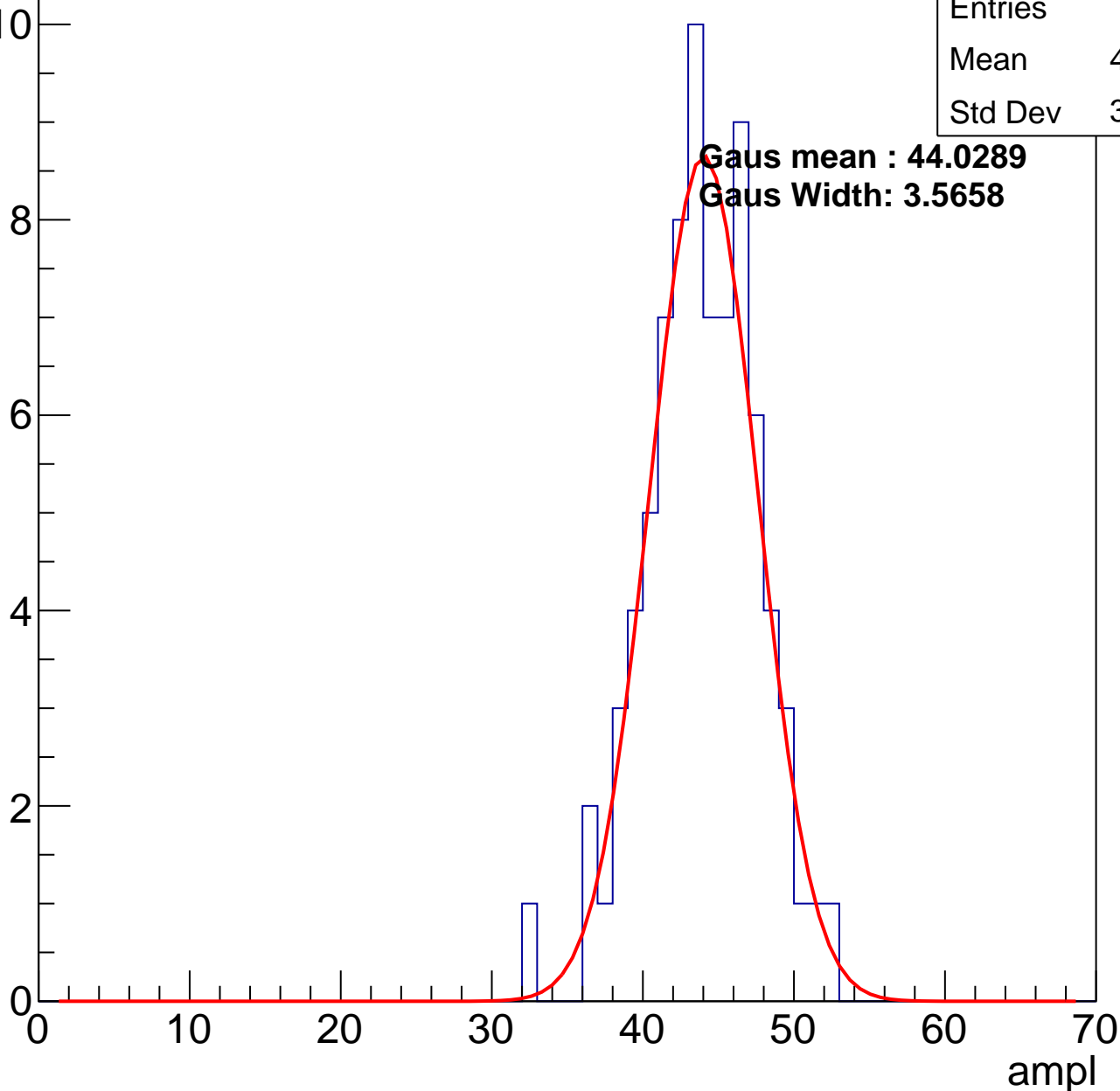
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	43.44
Std Dev	3.663

**Gaus mean : 44.0289**

**Gaus Width: 3.5658**

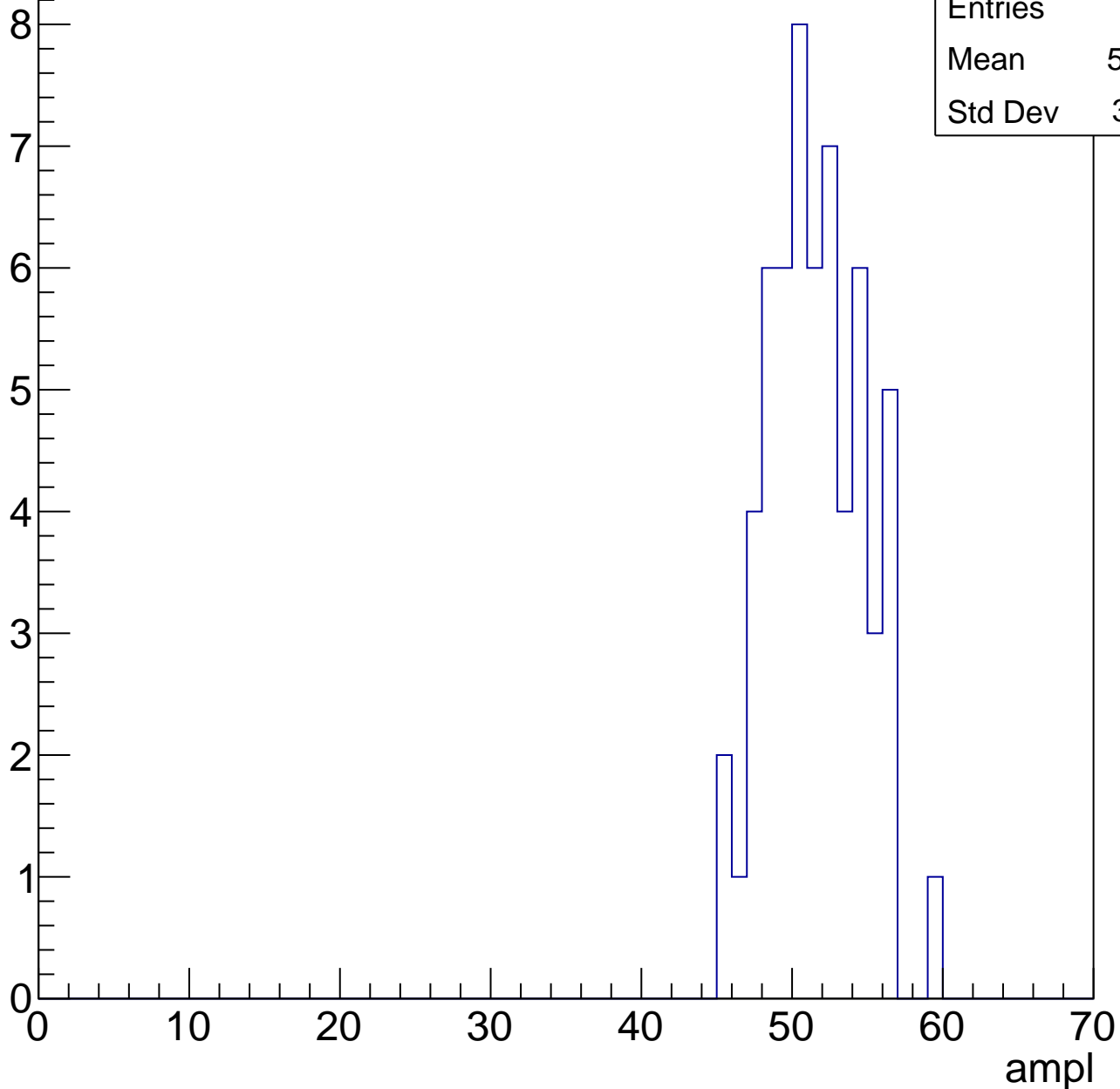


# B1L101S, U9-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	51.12
Std Dev	3.081

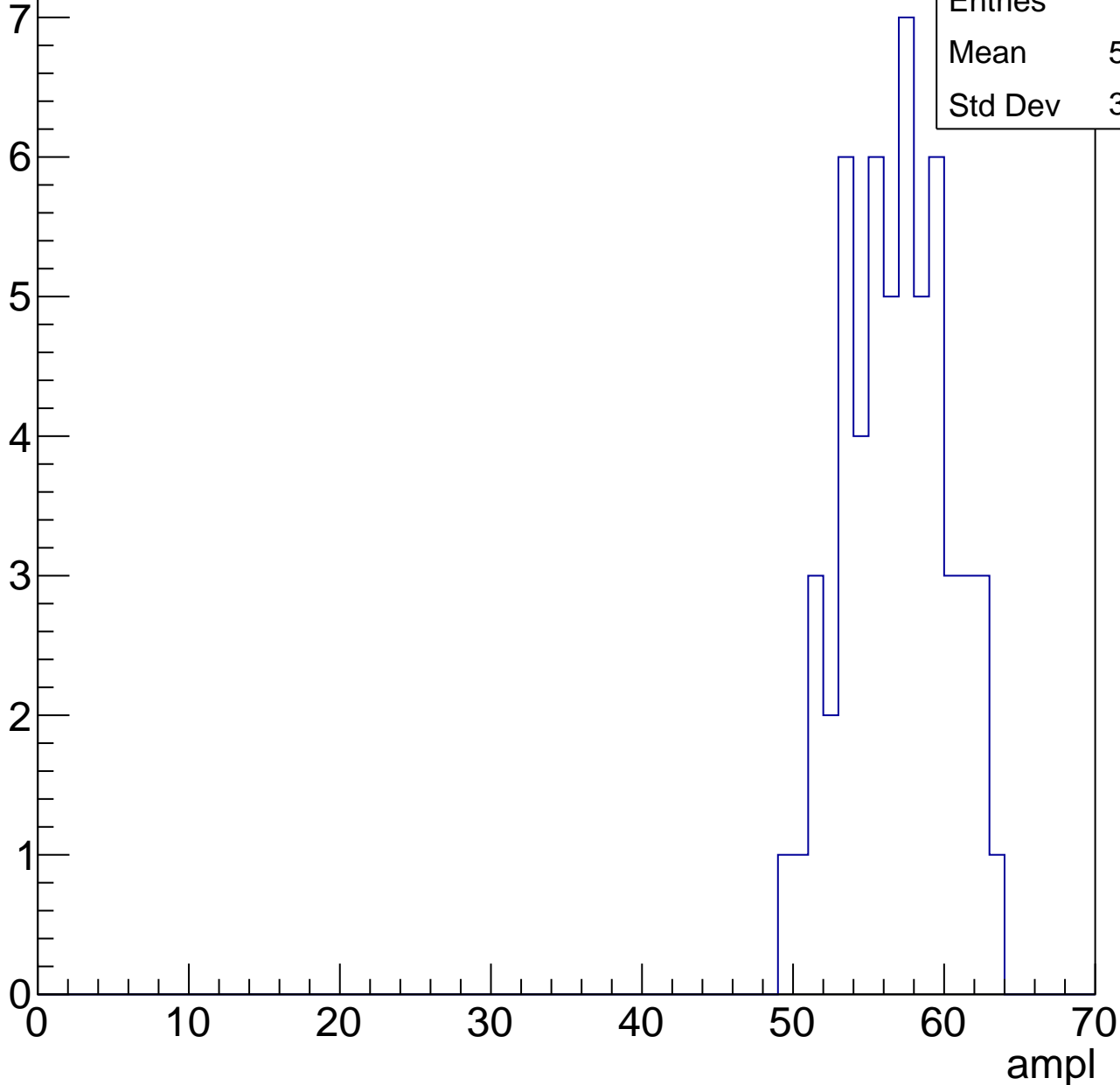


# B1L101S, U9-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

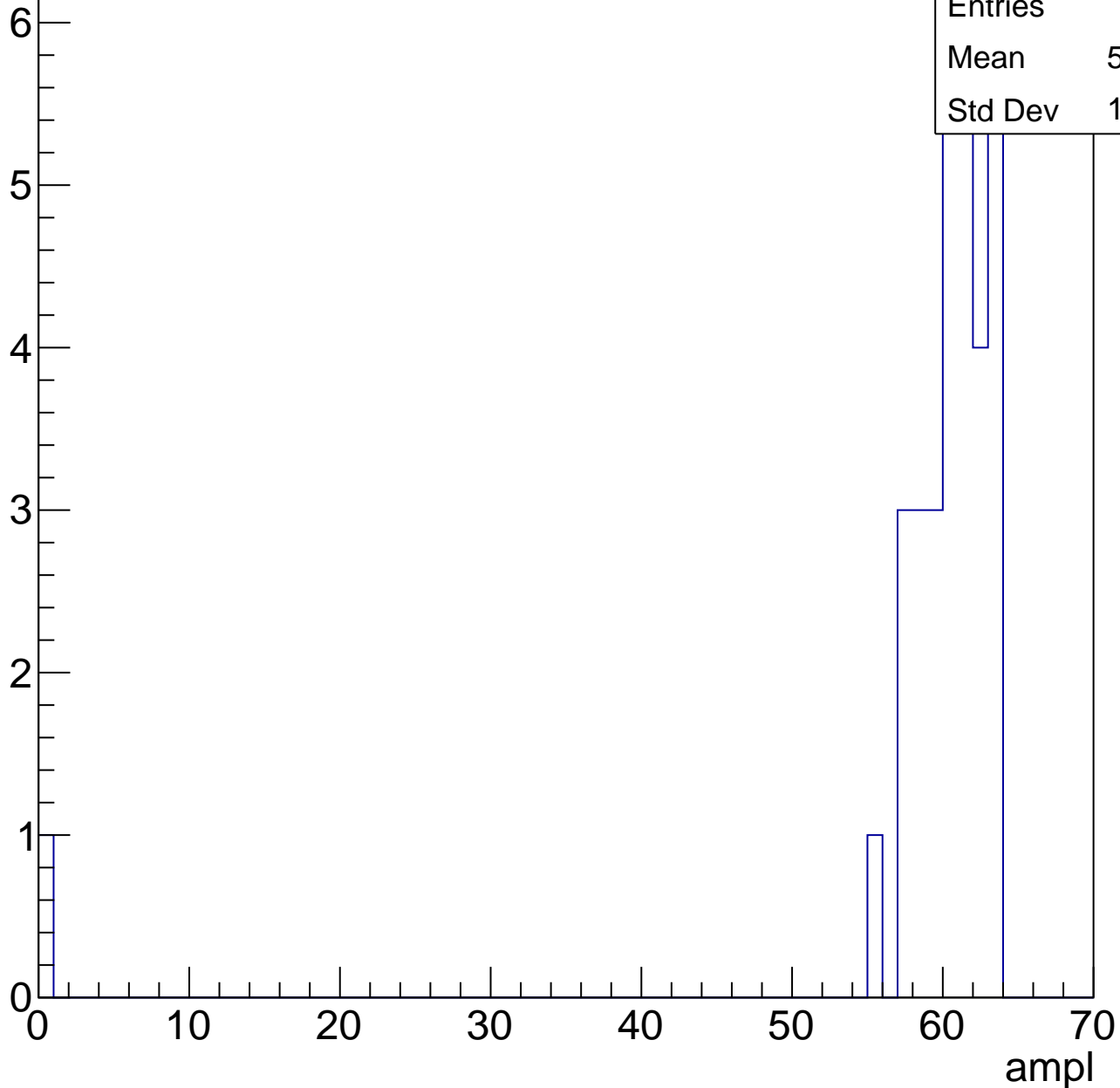
Entries	56
Mean	56.34
Std Dev	3.334



# B1L101S, U9-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

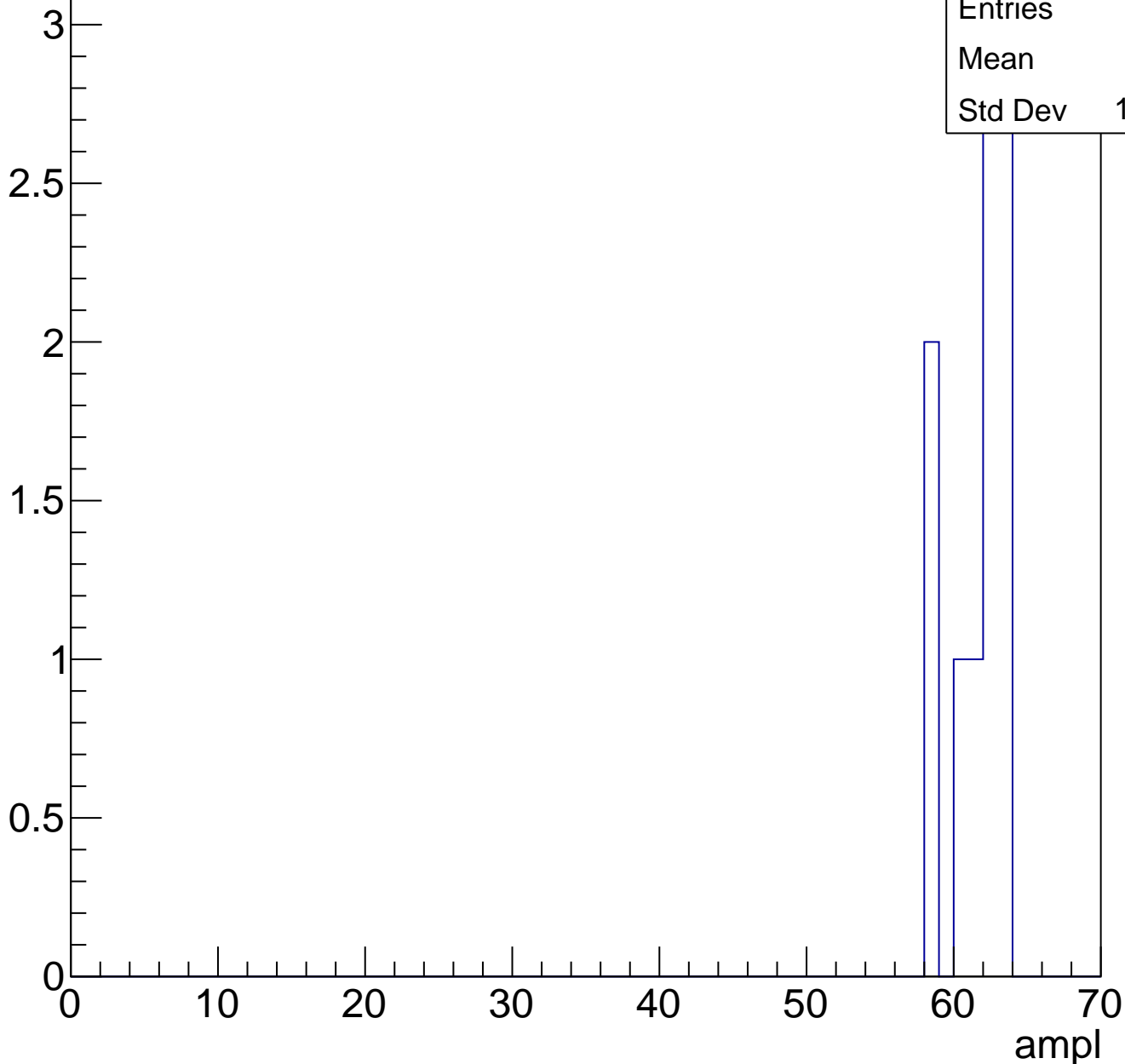
Entry



# B1L101S, U9-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U9-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U9-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

