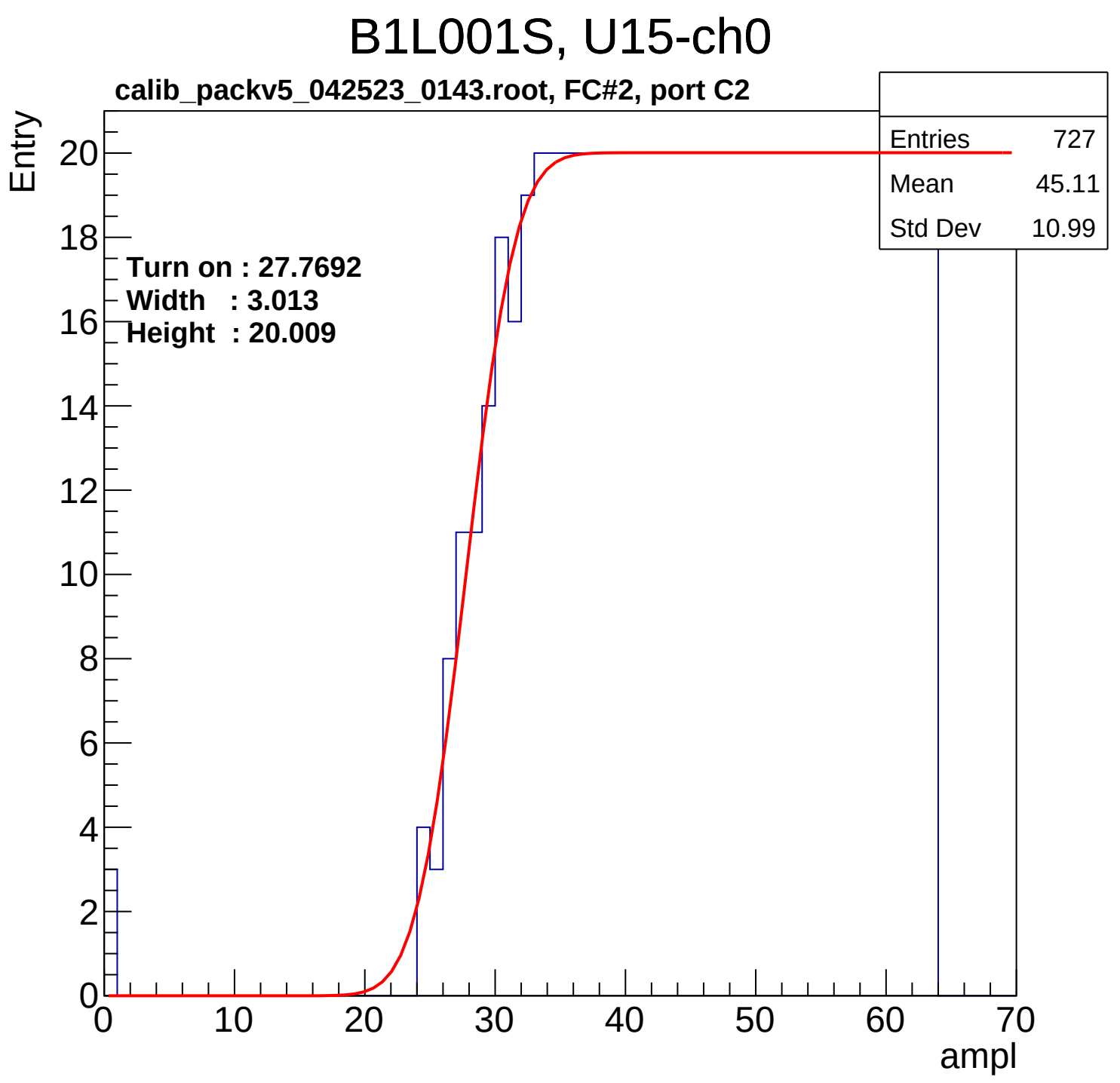
B1L001S, U15-ch0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 727
Mean 45.11
Std Dev 10.99
Turn on : 27.7692
Width : 3.013
Height : 20.009
Entry
ampl
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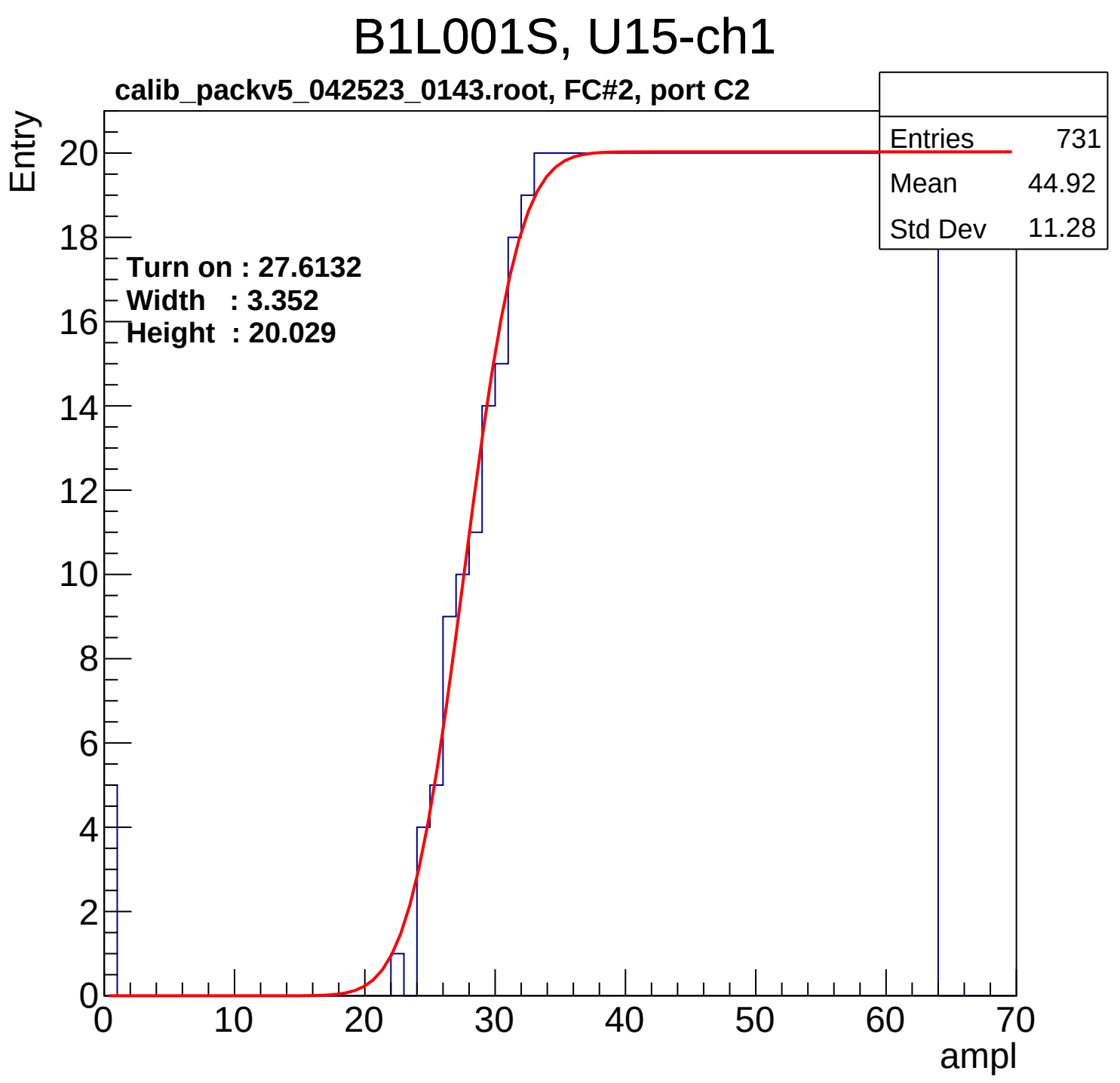
B1L001S, U15-ch1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 731
Mean 44.92
Std Dev 11.28
Turn on : 27.6132
Width : 3.352
Height : 20.029
Entry
ampl
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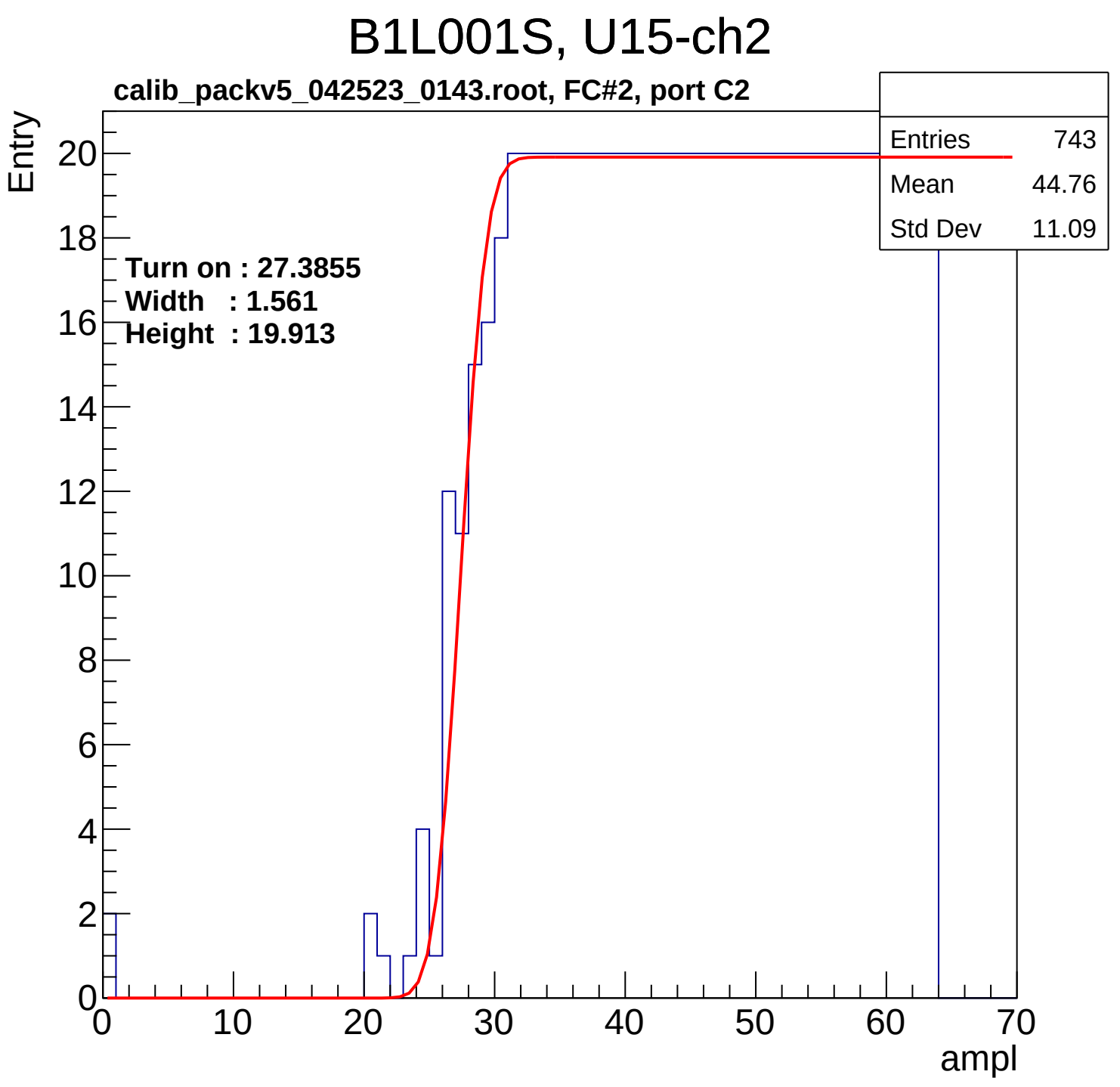
B1L001S, U15-ch2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.76
Std Dev 11.09
Turn on : 27.3855
Width : 1.561
Height : 19.913
Entry
ampl
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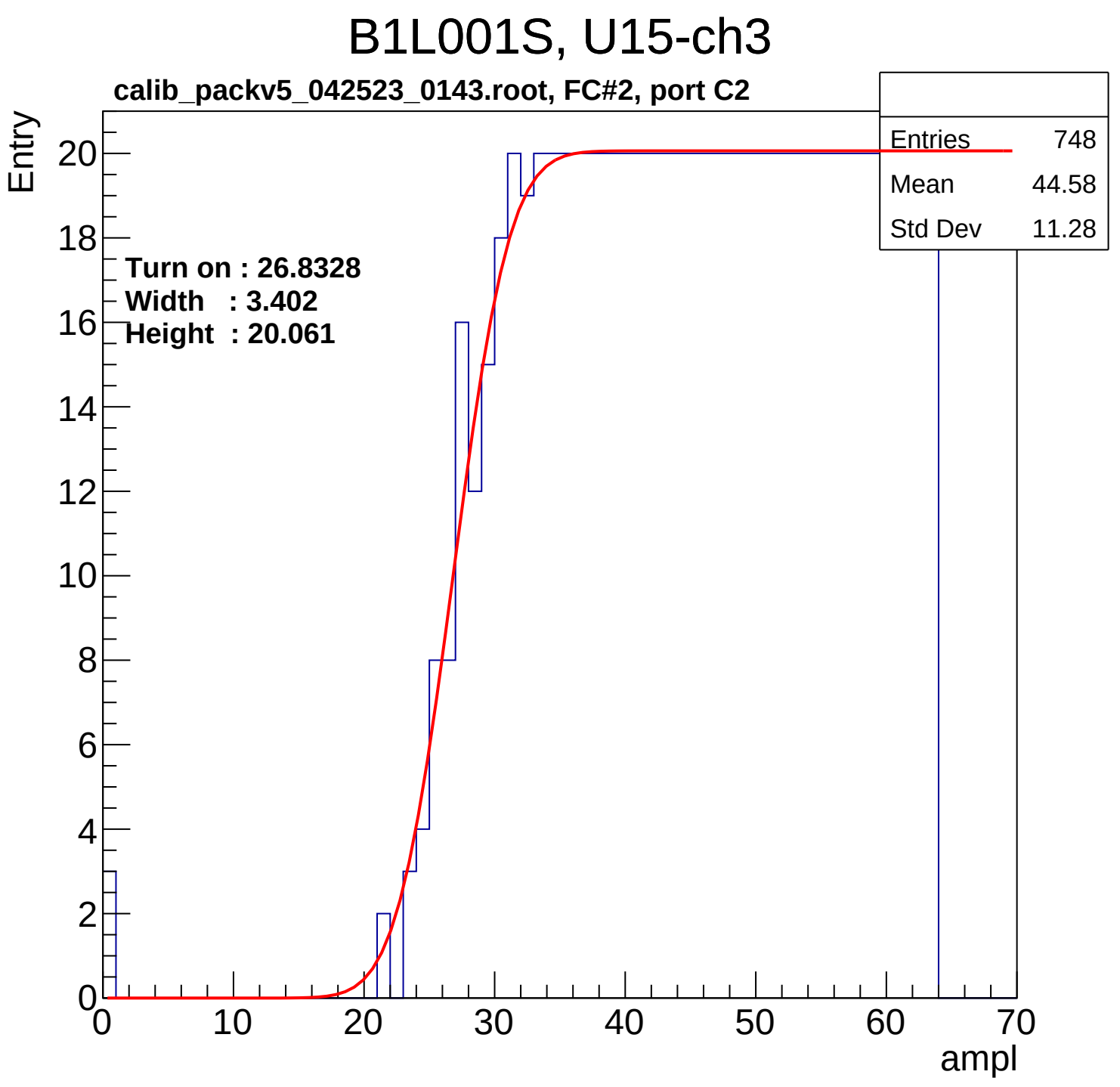
B1L001S, U15-ch3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 748
Mean 44.58
Std Dev 11.28
Turn on : 26.8328
Width : 3.402
Height : 20.061
Entry
ampl
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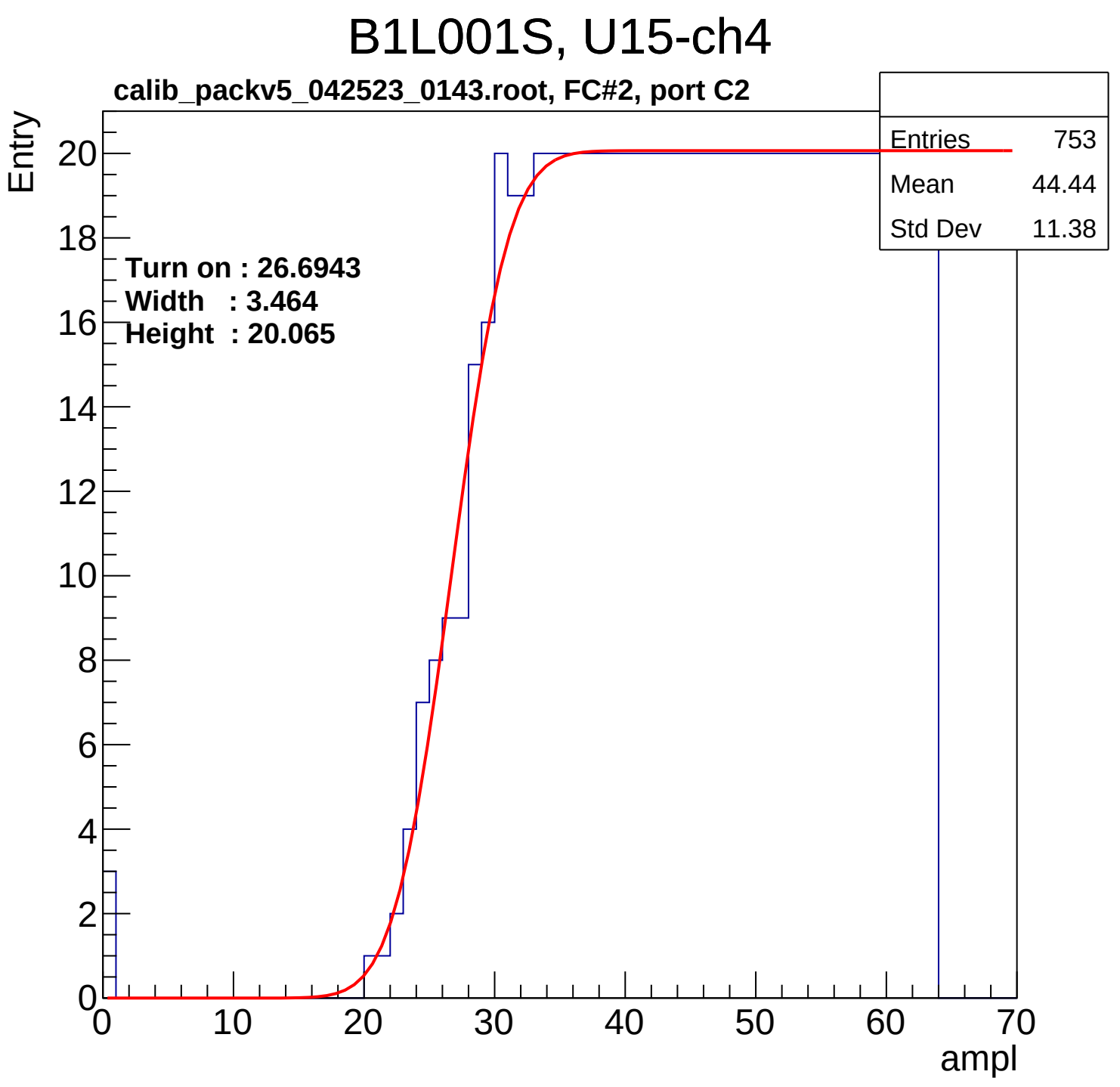
B1L001S, U15-ch4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 753
Mean 44.44
Std Dev 11.38
Turn on : 26.6943
Width : 3.464
Height : 20.065
Entry
ampl
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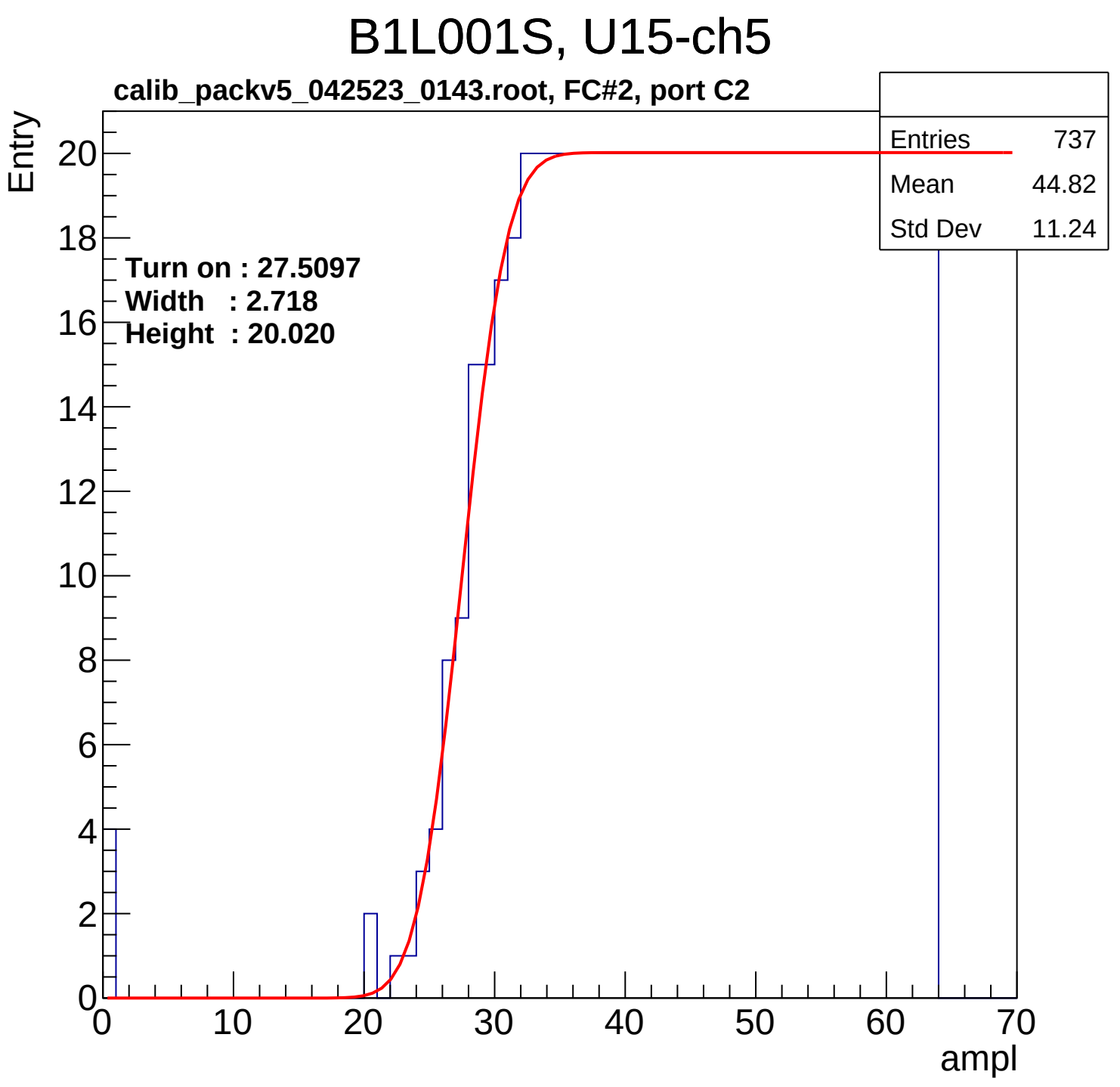
B1L001S, U15-ch5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 737
Mean 44.82
Std Dev 11.24
Turn on : 27.5097
Width : 2.718
Height : 20.020
Entry
ampl
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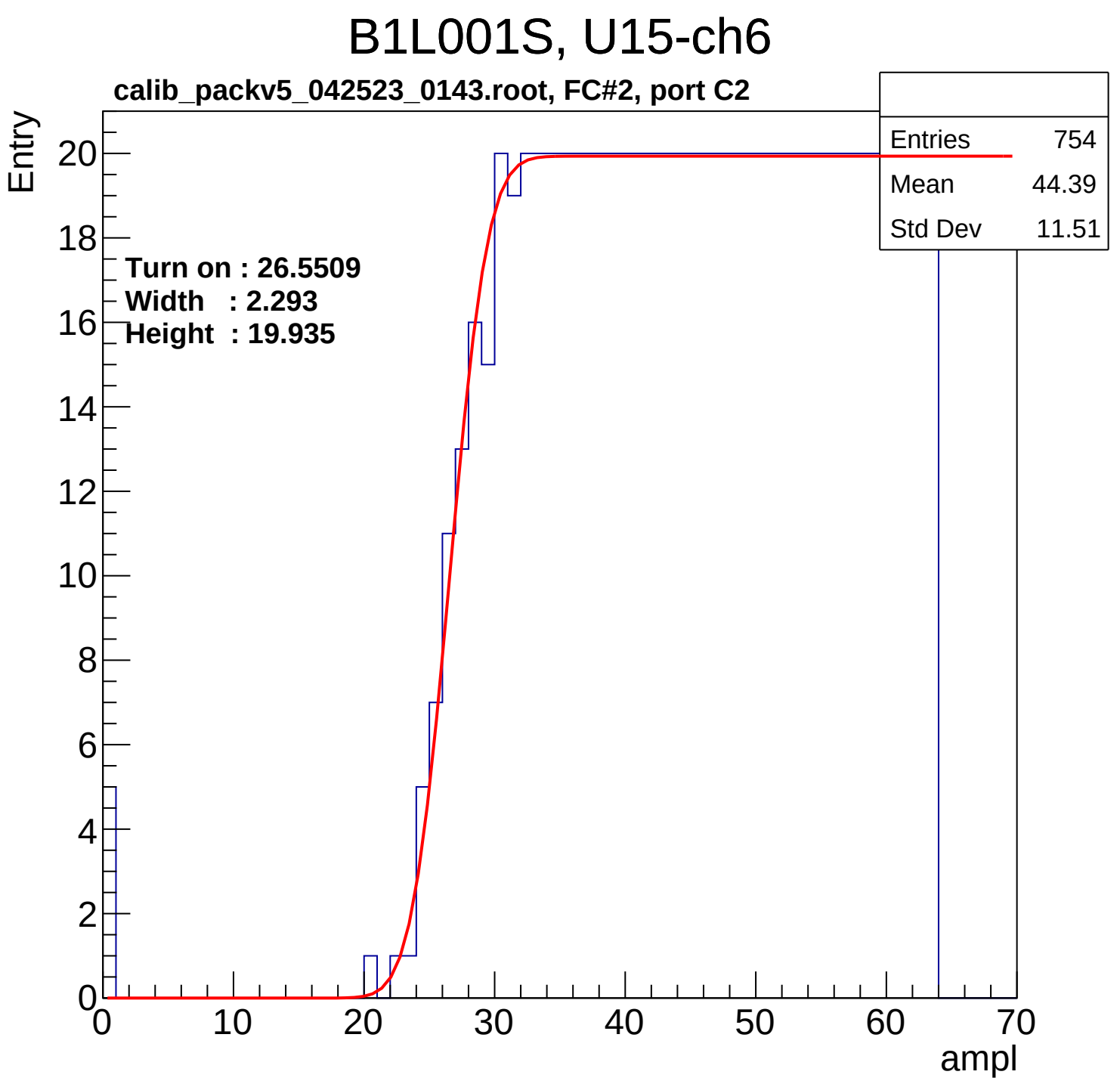
B1L001S, U15-ch6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 754
Mean 44.39
Std Dev 11.51
Turn on : 26.5509
Width : 2.293
Height : 19.935
Entry
ampl
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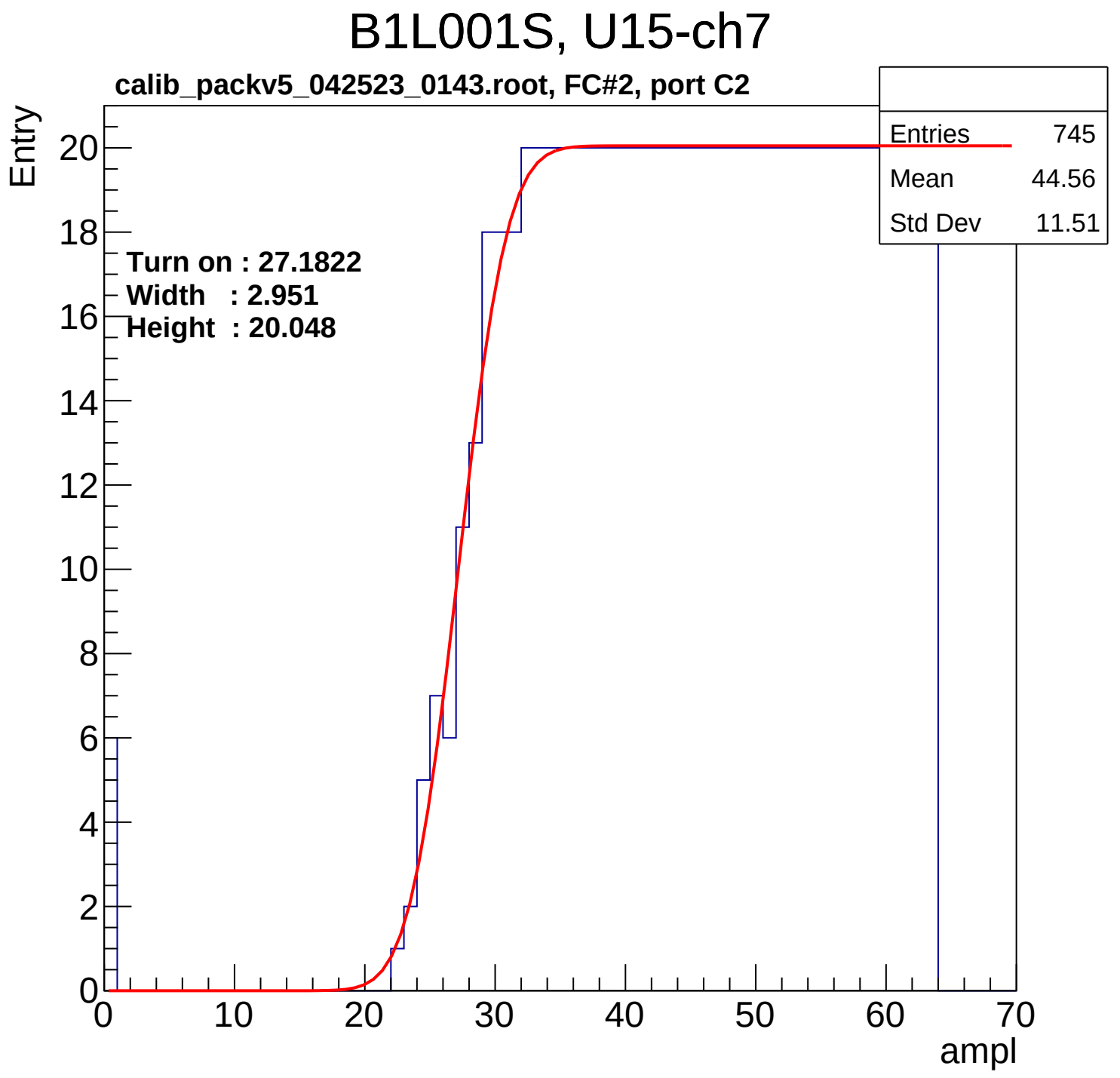
B1L001S, U15-ch7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 745
Mean 44.56
Std Dev 11.51
Turn on : 27.1822
Width : 2.951
Height : 20.048
Entry
ampl
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6
8
10
12
14
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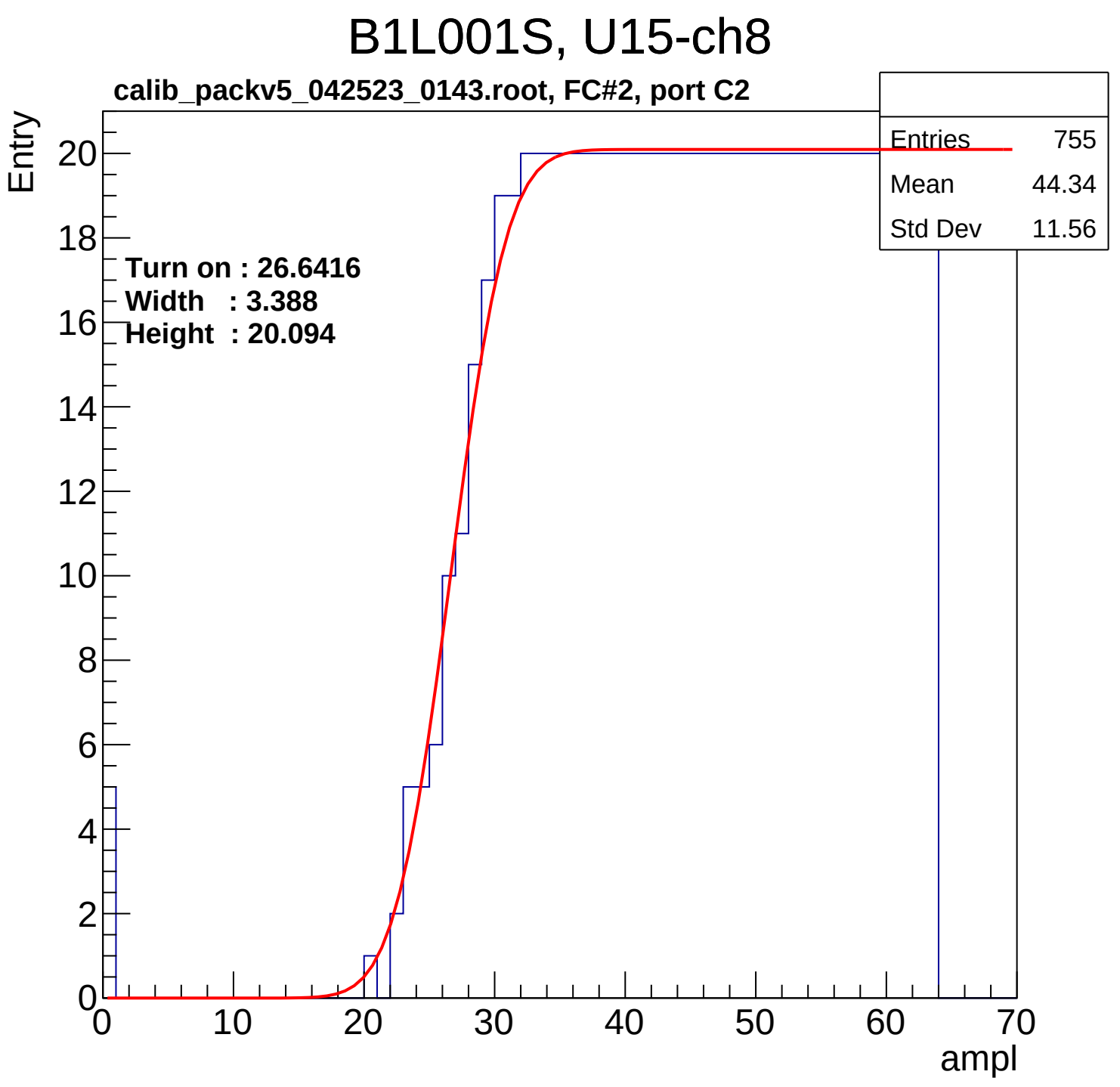
B1L001S, U15-ch8
calib_packv5_042523_0143.root, FC#2, port C2
Entries 755
Mean 44.34
Std Dev 11.56
Turn on : 26.6416
Width : 3.388
Height : 20.094
Entry
ampl
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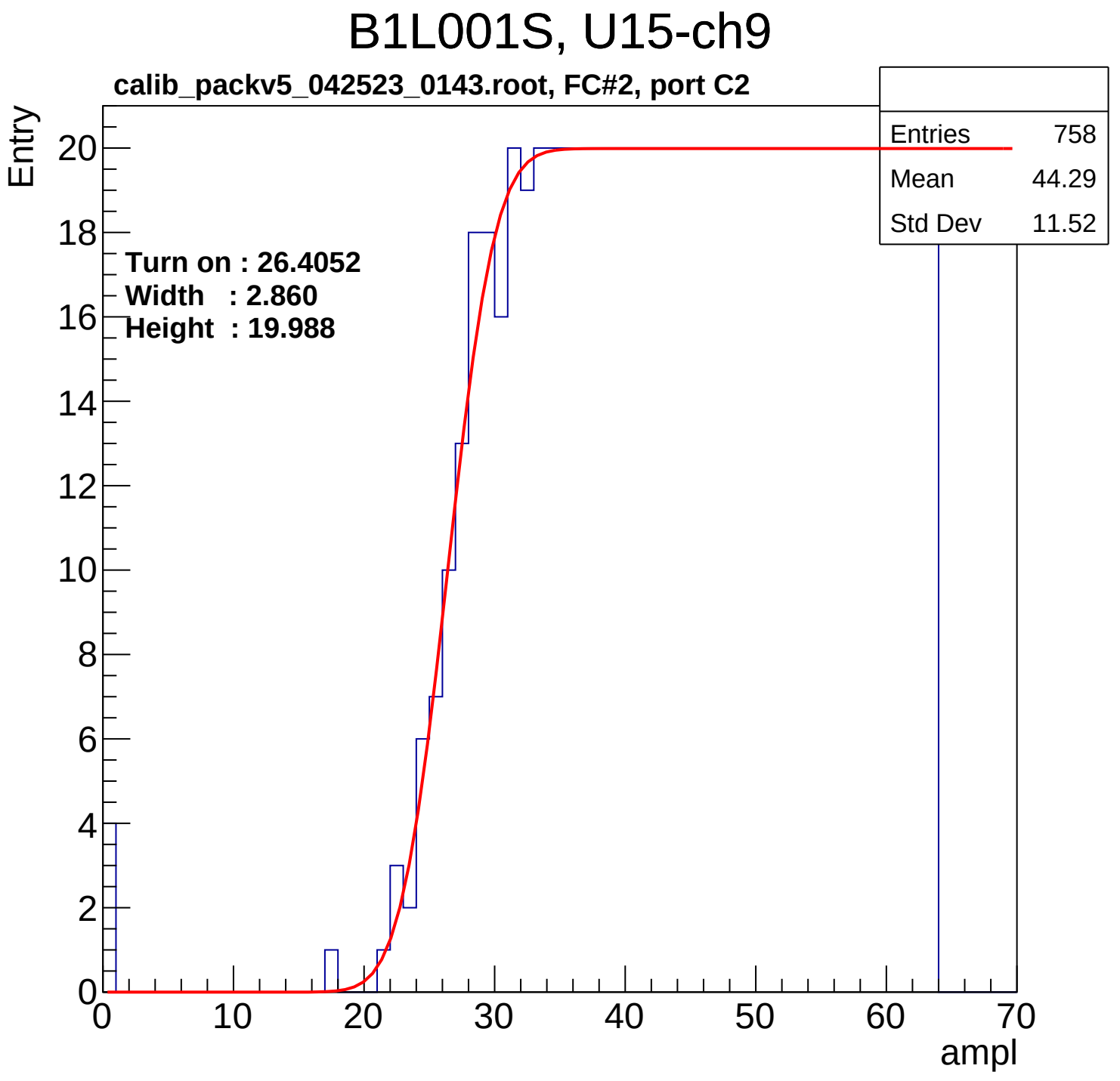
B1L001S, U15-ch9
calib_packv5_042523_0143.root, FC#2, port C2
Entries 758
Mean 44.29
Std Dev 11.52
Turn on : 26.4052
Width : 2.860
Height : 19.988
Entry
ampl
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6
8
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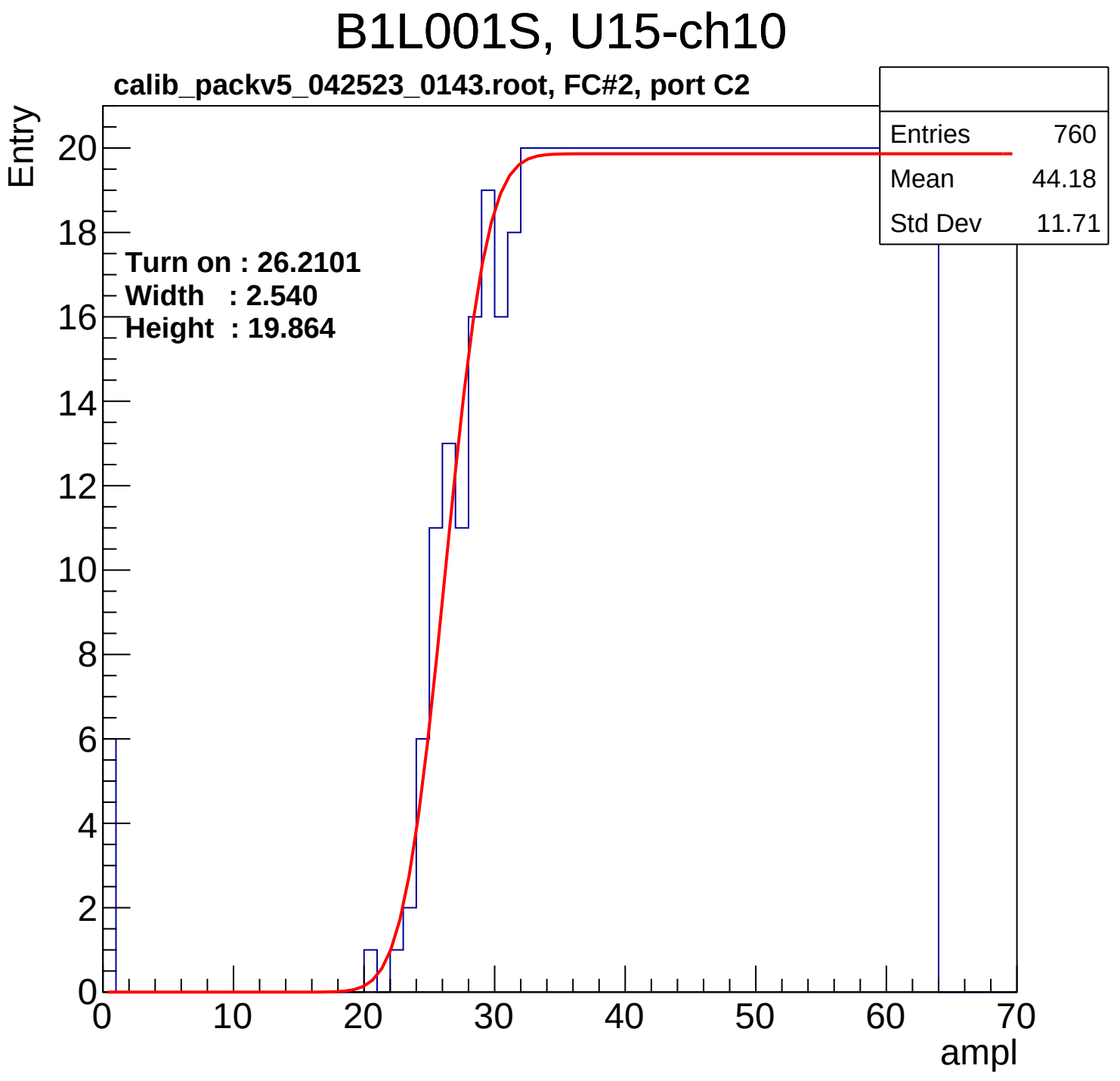
B1L001S, U15-ch10
calib_packv5_042523_0143.root, FC#2, port C2
Entries 760
Mean 44.18
Std Dev 11.71
Turn on : 26.2101
Width : 2.540
Height : 19.864
Entry
ampl
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6
8
10
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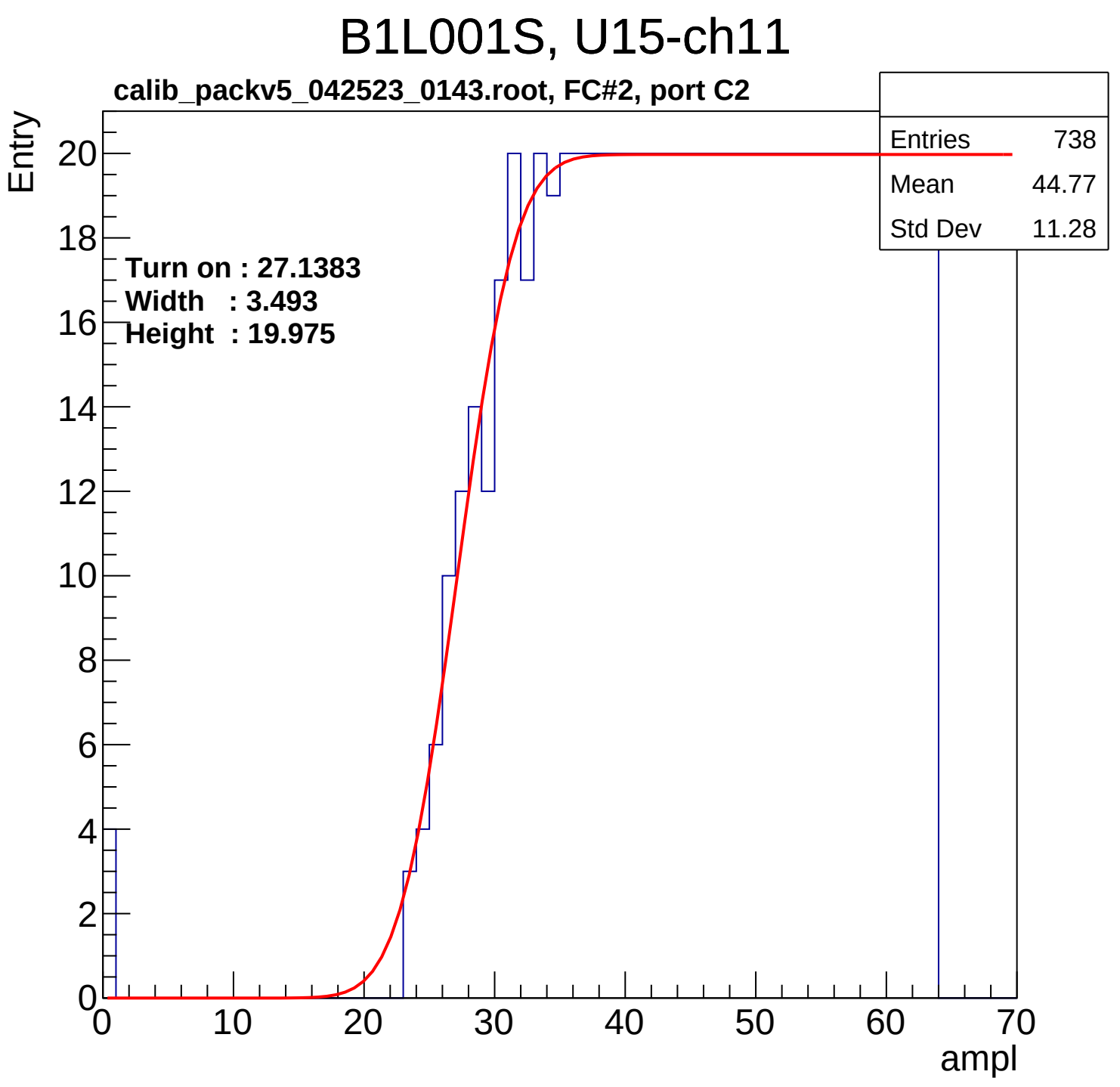
B1L001S, U15-ch11
calib_packv5_042523_0143.root, FC#2, port C2
Entries 738
Mean 44.77
Std Dev 11.28
Turn on : 27.1383
Width : 3.493
Height : 19.975
Entry
ampl
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6
8
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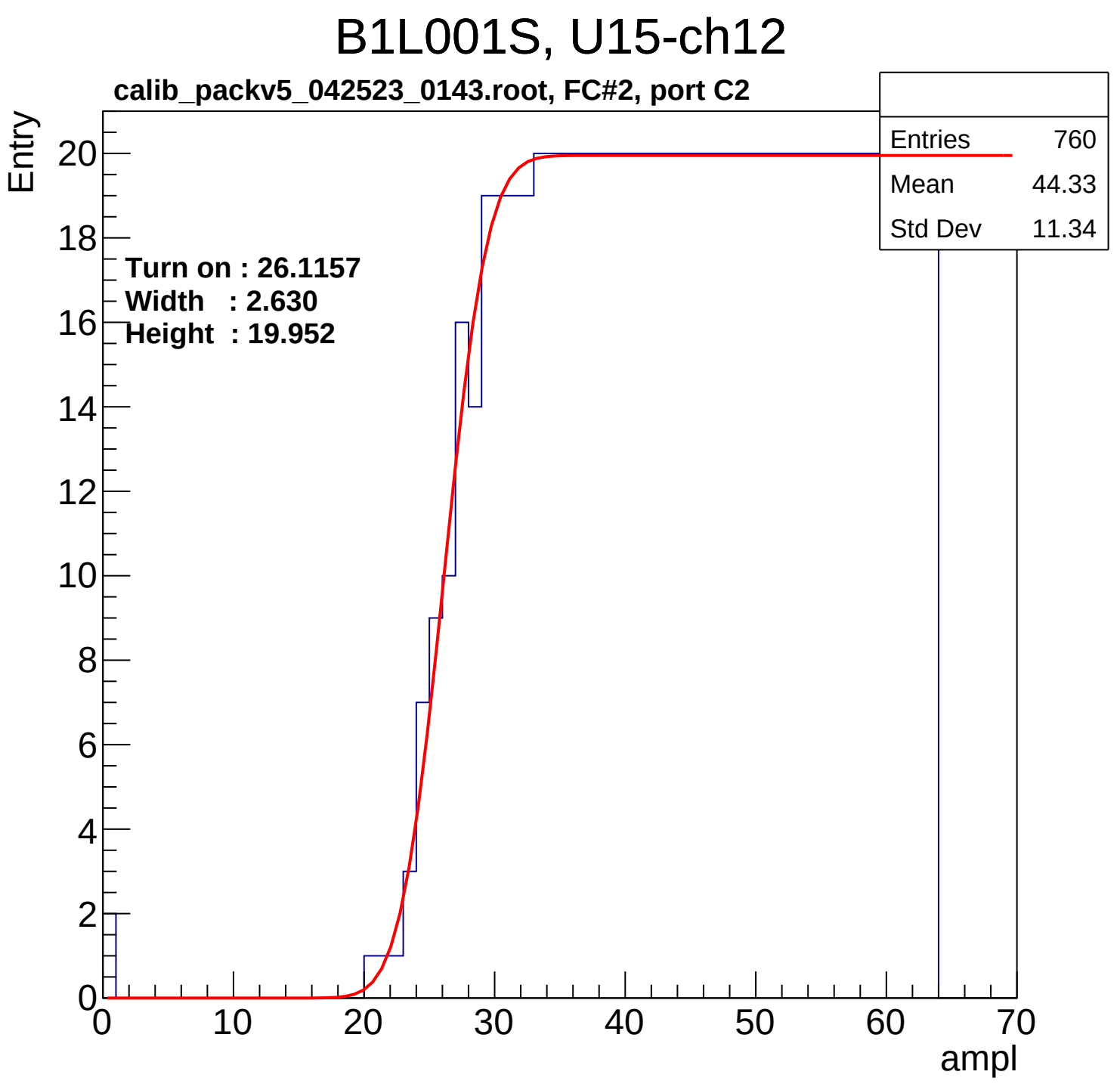
B1L001S, U15-ch12
calib_packv5_042523_0143.root, FC#2, port C2
Entries 760
Mean 44.33
Std Dev 11.34
Turn on : 26.1157
Width : 2.630
Height : 19.952
Entry
ampl
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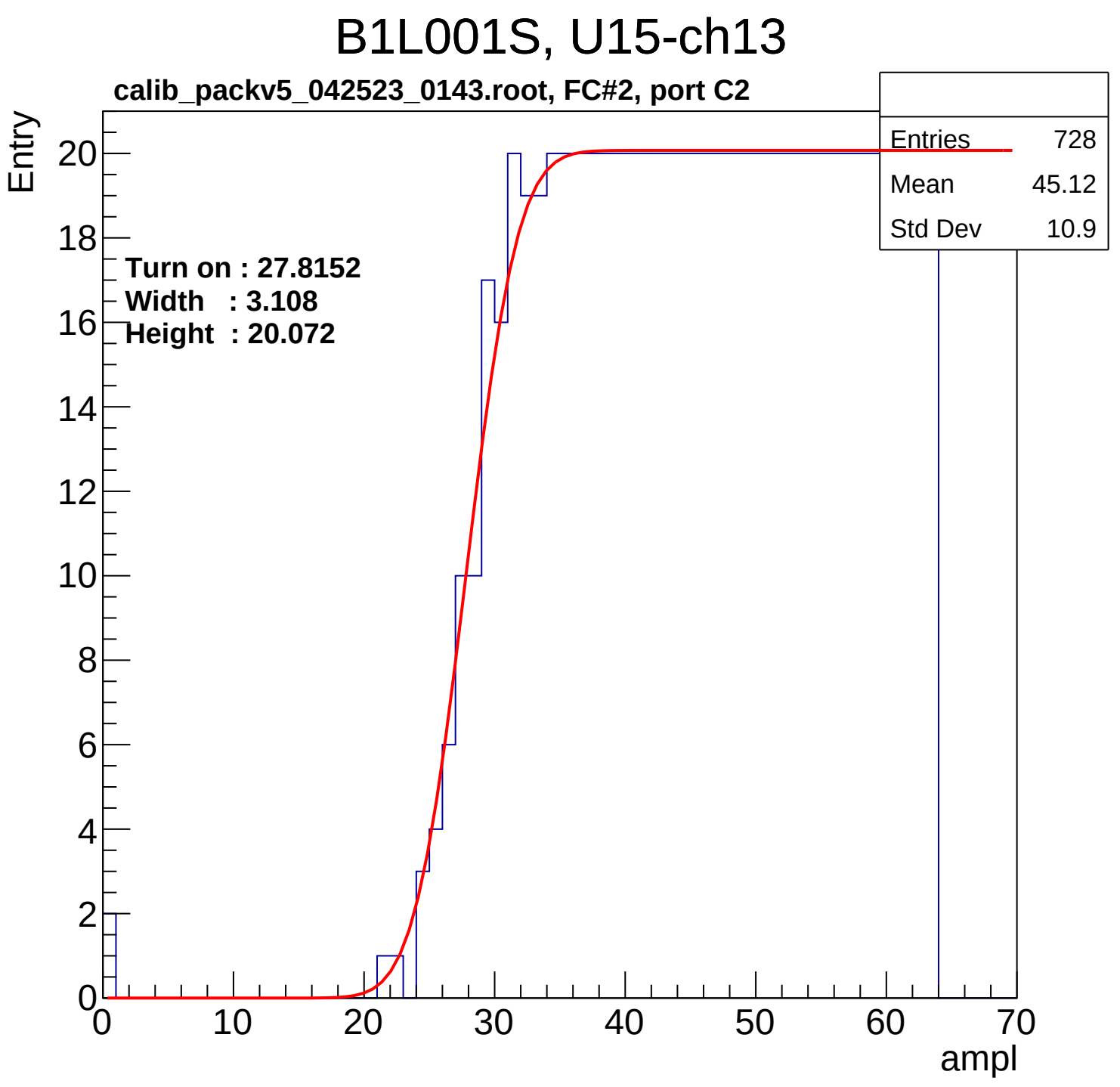
B1L001S, U15-ch13
calib_packv5_042523_0143.root, FC#2, port C2
Entries 728
Mean 45.12
Std Dev 10.9
Turn on : 27.8152
Width : 3.108
Height : 20.072
Entry
ampl
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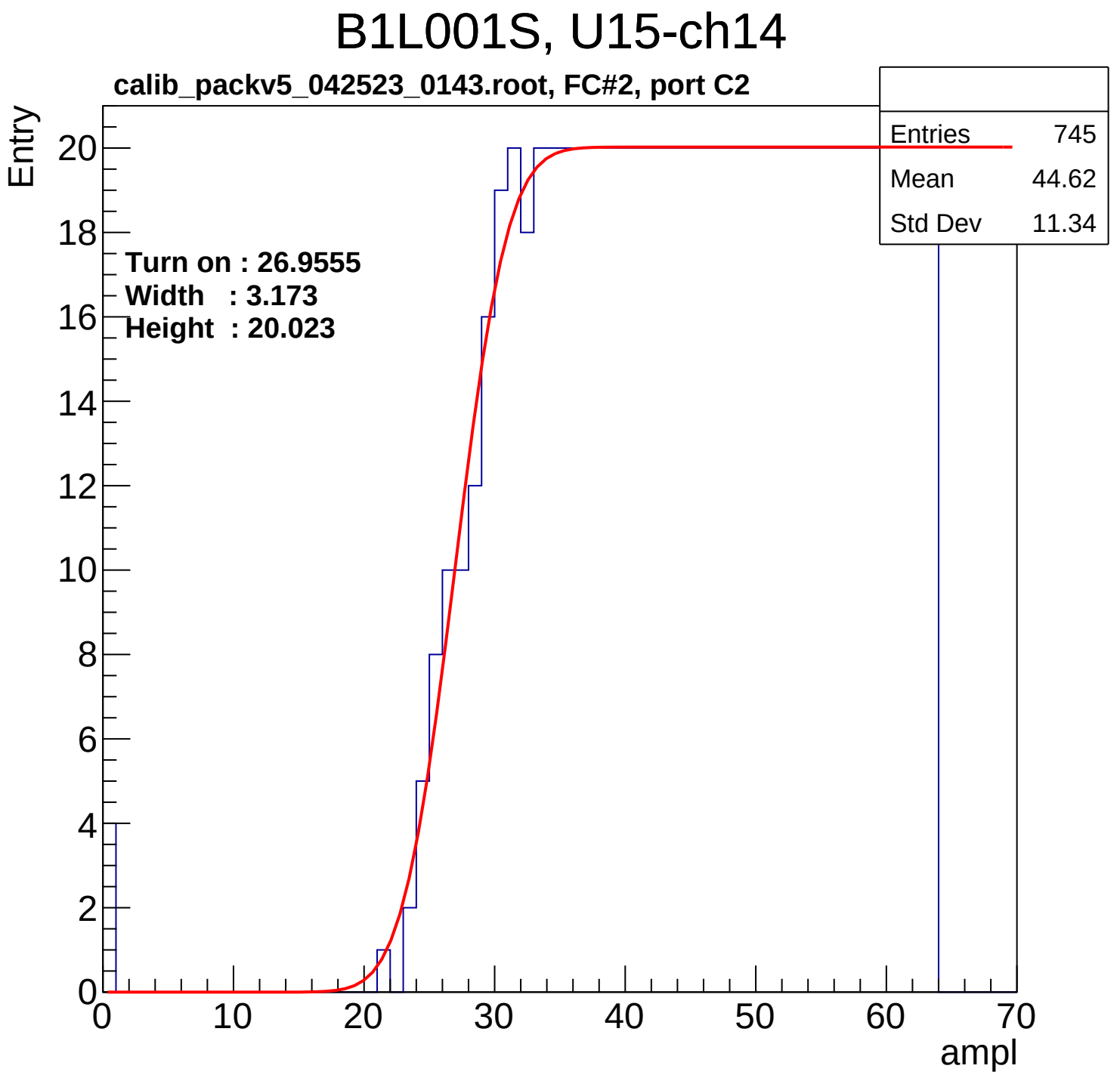
B1L001S, U15-ch14
calib_packv5_042523_0143.root, FC#2, port C2
Entries 745
Mean 44.62
Std Dev 11.34
Turn on : 26.9555
Width : 3.173
Height : 20.023
Entry
ampl
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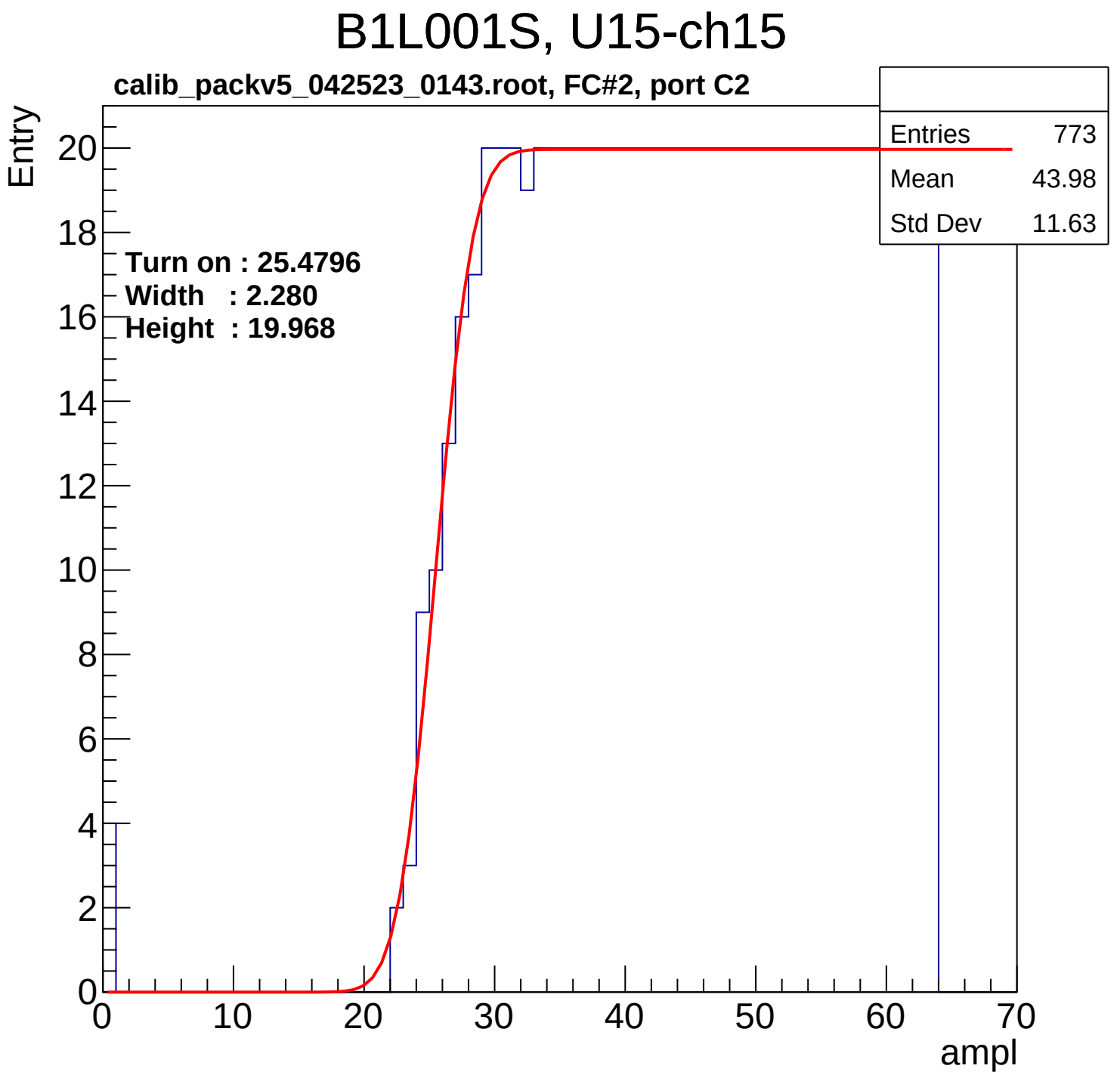
B1L001S, U15-ch15
calib_packv5_042523_0143.root, FC#2, port C2
Entries 773
Mean 43.98
Std Dev 11.63
Turn on : 25.4796
Width : 2.280
Height : 19.968
Entry
ampl
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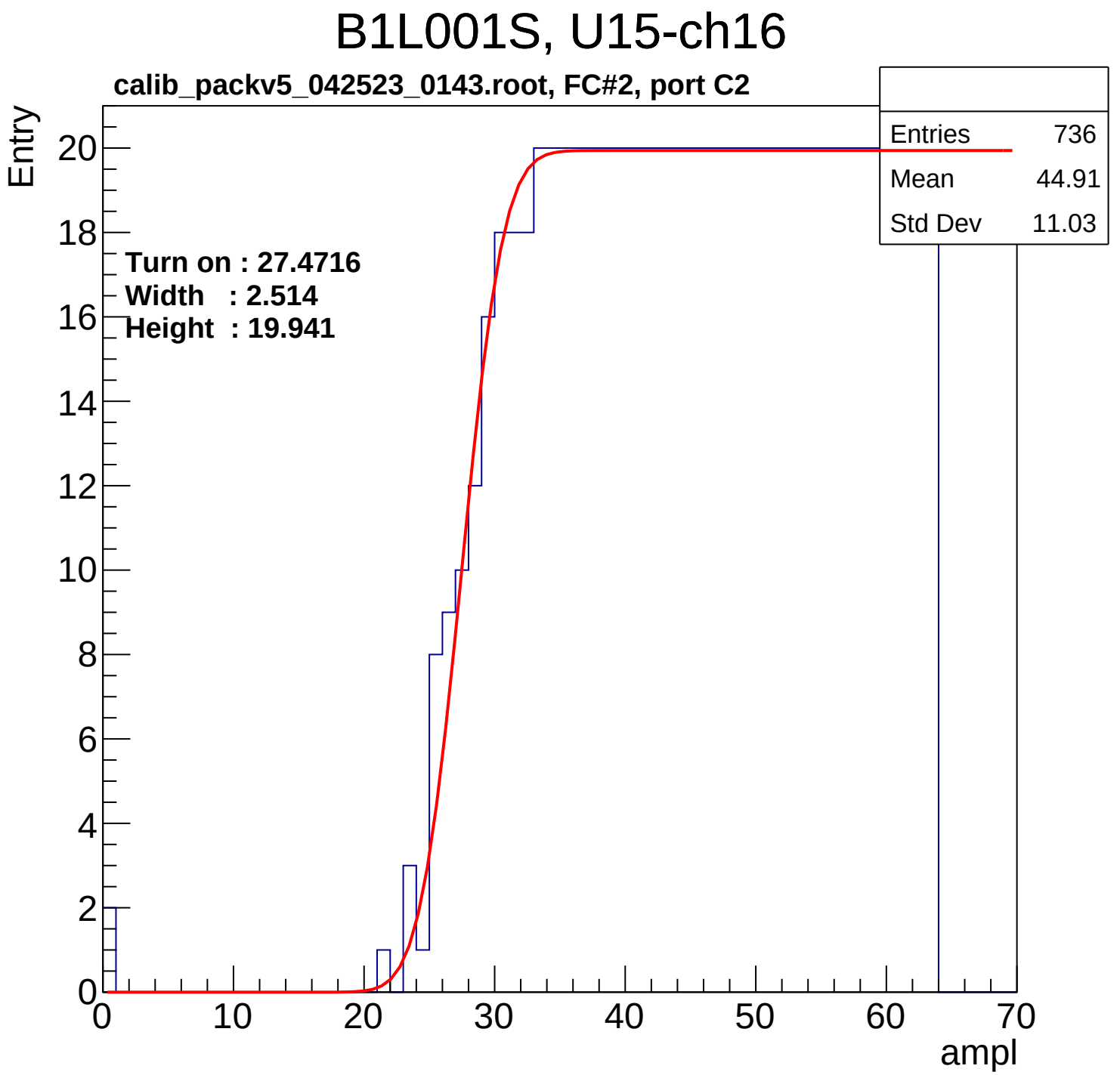
B1L001S, U15-ch16
calib_packv5_042523_0143.root, FC#2, port C2
Entries 736
Mean 44.91
Std Dev 11.03
Turn on : 27.4716
Width : 2.514
Height : 19.941
Entry
ampl
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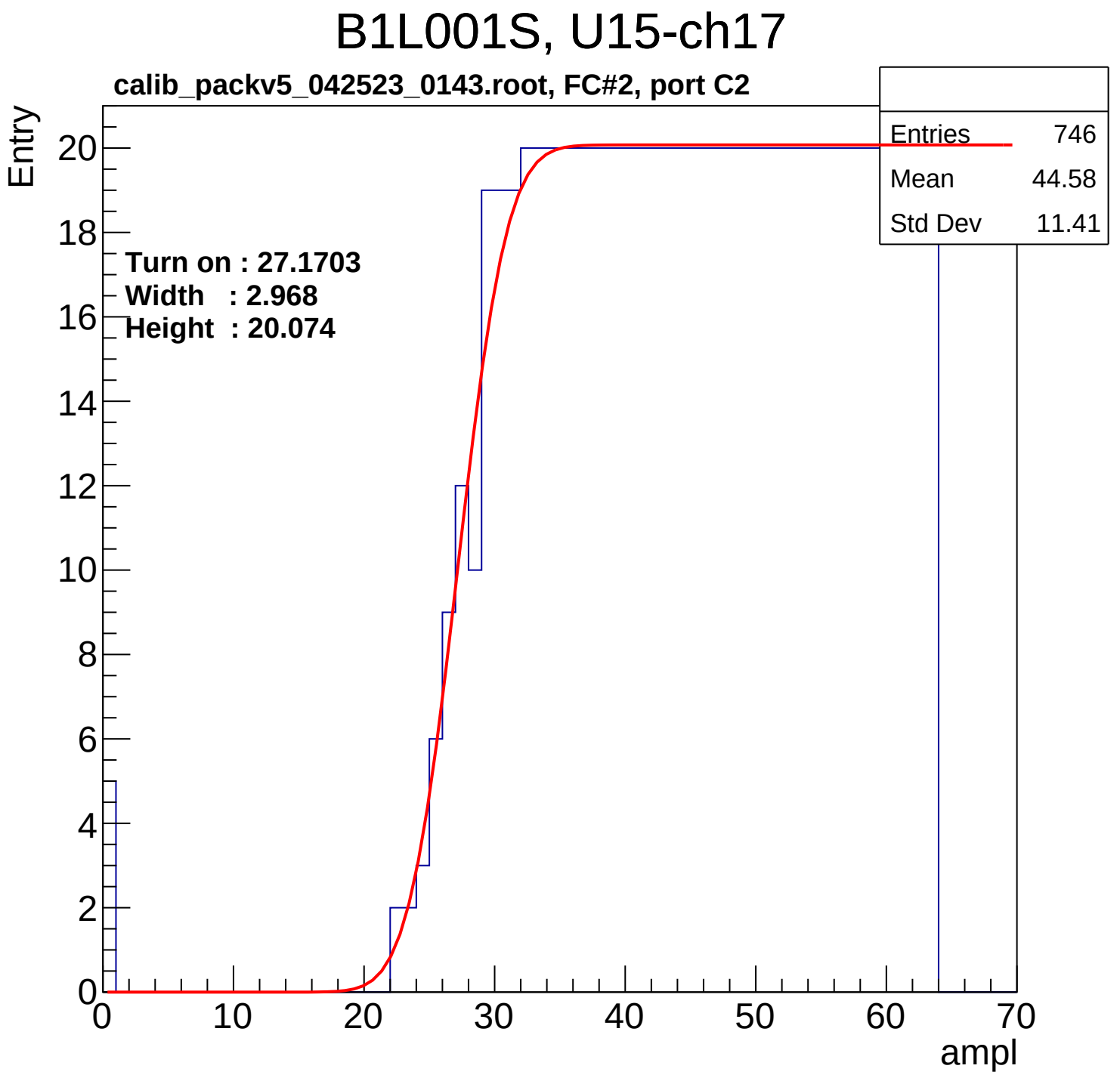
B1L001S, U15-ch17
calib_packv5_042523_0143.root, FC#2, port C2
Entries 746
Mean 44.58
Std Dev 11.41
Turn on : 27.1703
Width : 2.968
Height : 20.074
Entry
ampl
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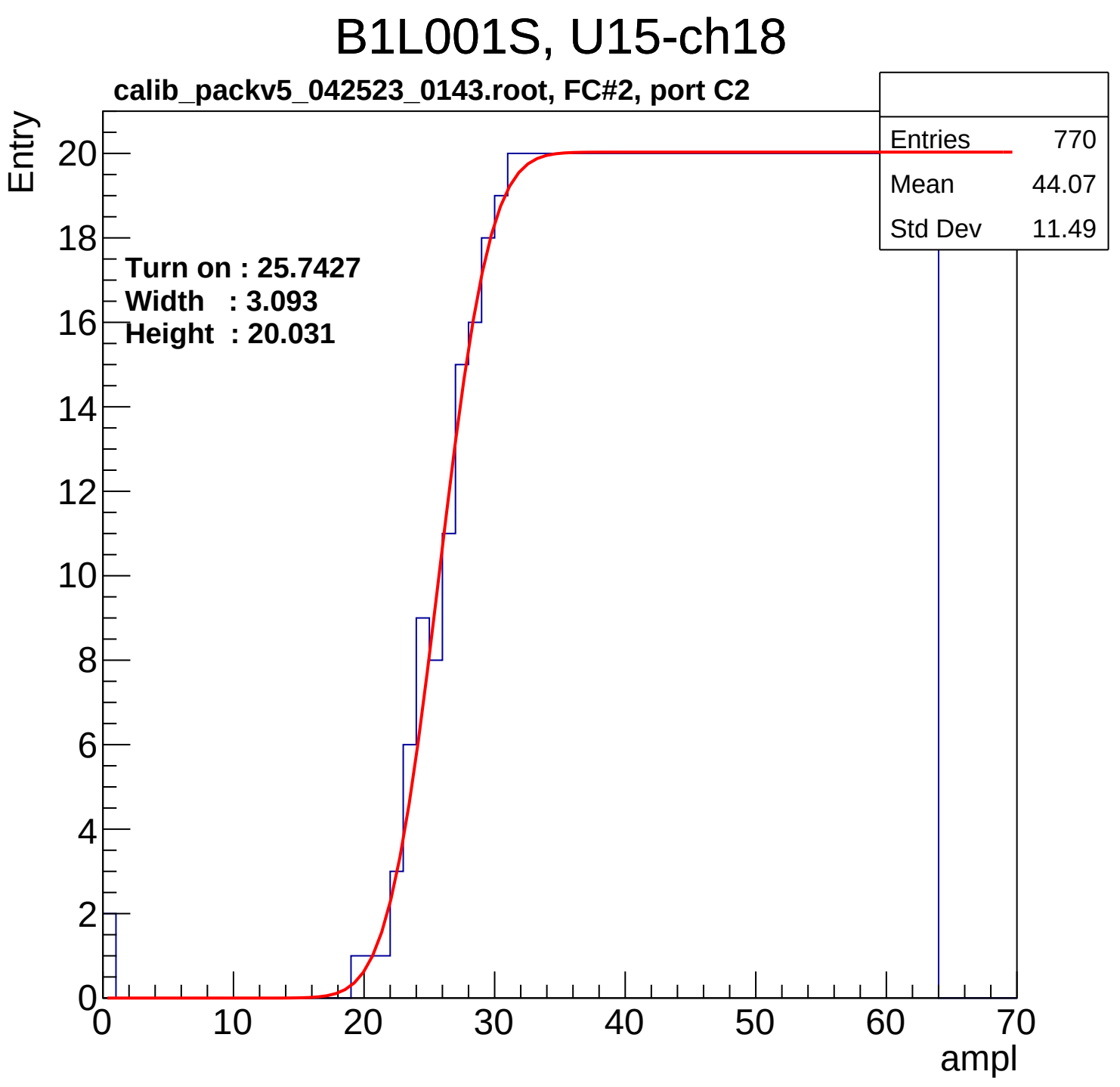
B1L001S, U15-ch18
calib_packv5_042523_0143.root, FC#2, port C2
Entries 770
Mean 44.07
Std Dev 11.49
Turn on : 25.7427
Width : 3.093
Height : 20.031
Entry
ampl
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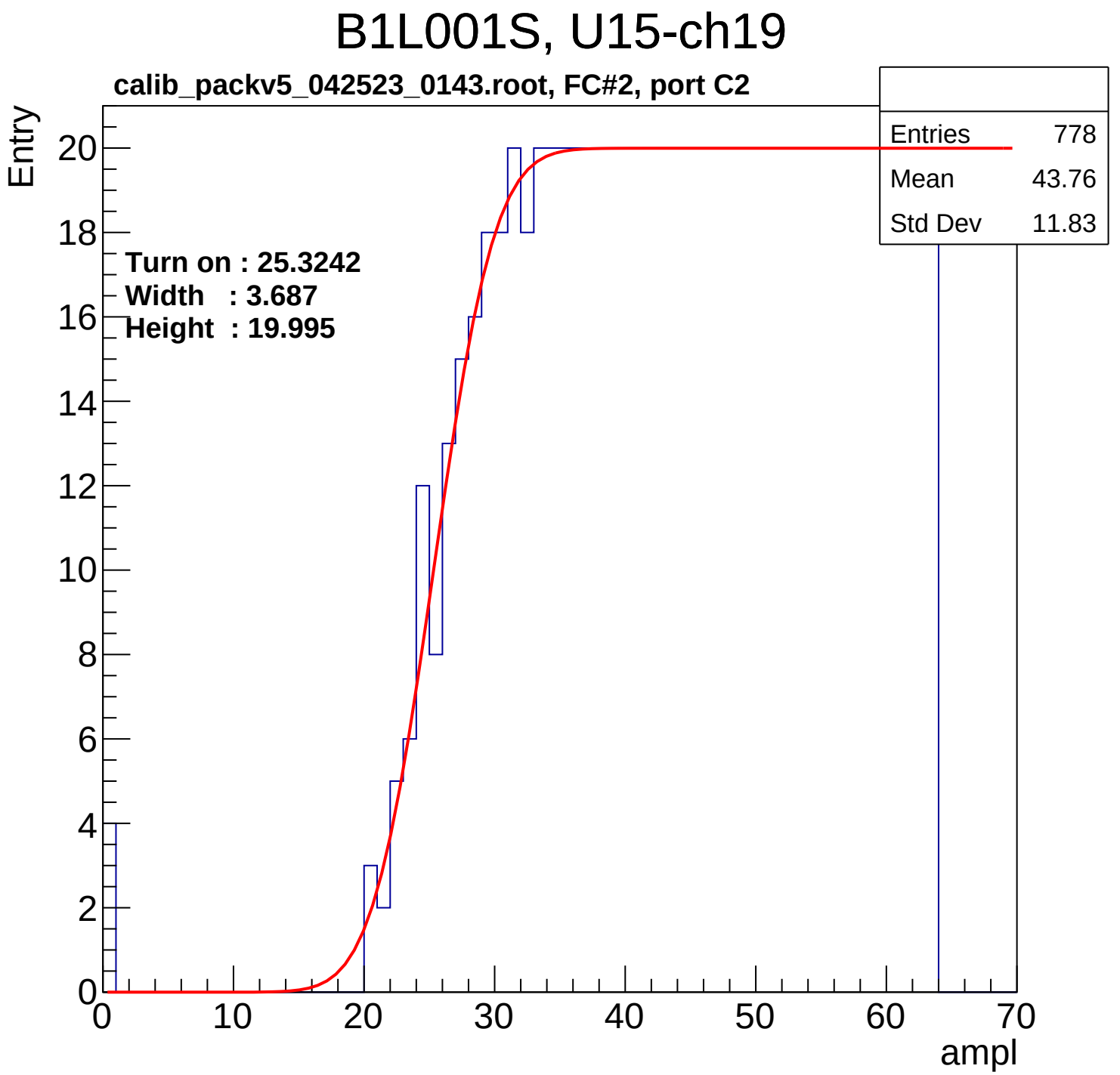
B1L001S, U15-ch19
calib_packv5_042523_0143.root, FC#2, port C2
Entries 778
Mean 43.76
Std Dev 11.83
Turn on : 25.3242
Width : 3.687
Height : 19.995
Entry
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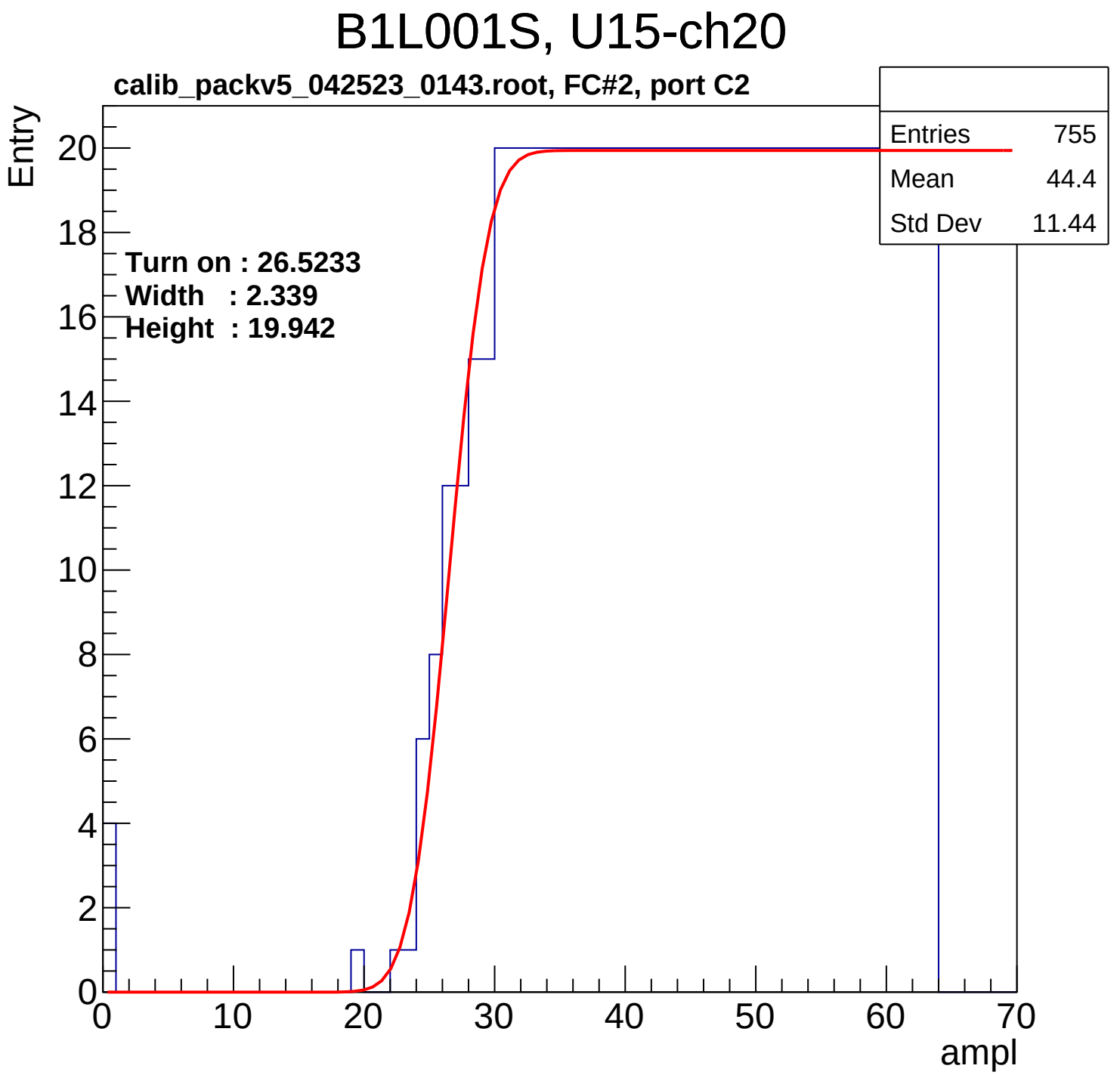
B1L001S, U15-ch20
calib_packv5_042523_0143.root, FC#2, port C2
Entries 755
Mean 44.4
Std Dev 11.44
Turn on : 26.5233
Width : 2.339
Height : 19.942
Entry
ampl
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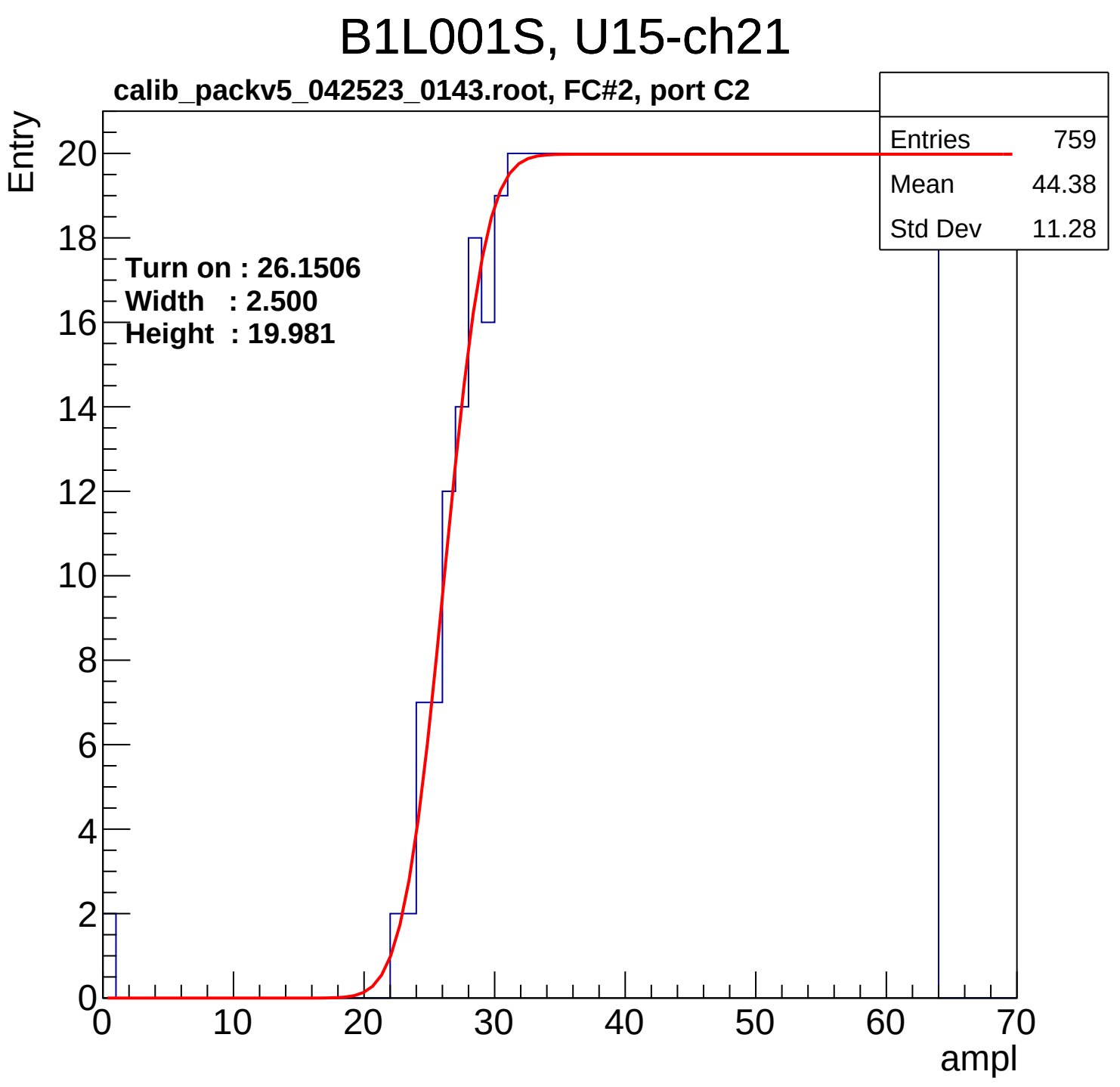
B1L001S, U15-ch21
calib_packv5_042523_0143.root, FC#2, port C2
Entries 759
Mean 44.38
Std Dev 11.28
Turn on : 26.1506
Width : 2.500
Height : 19.981
Entry
ampl
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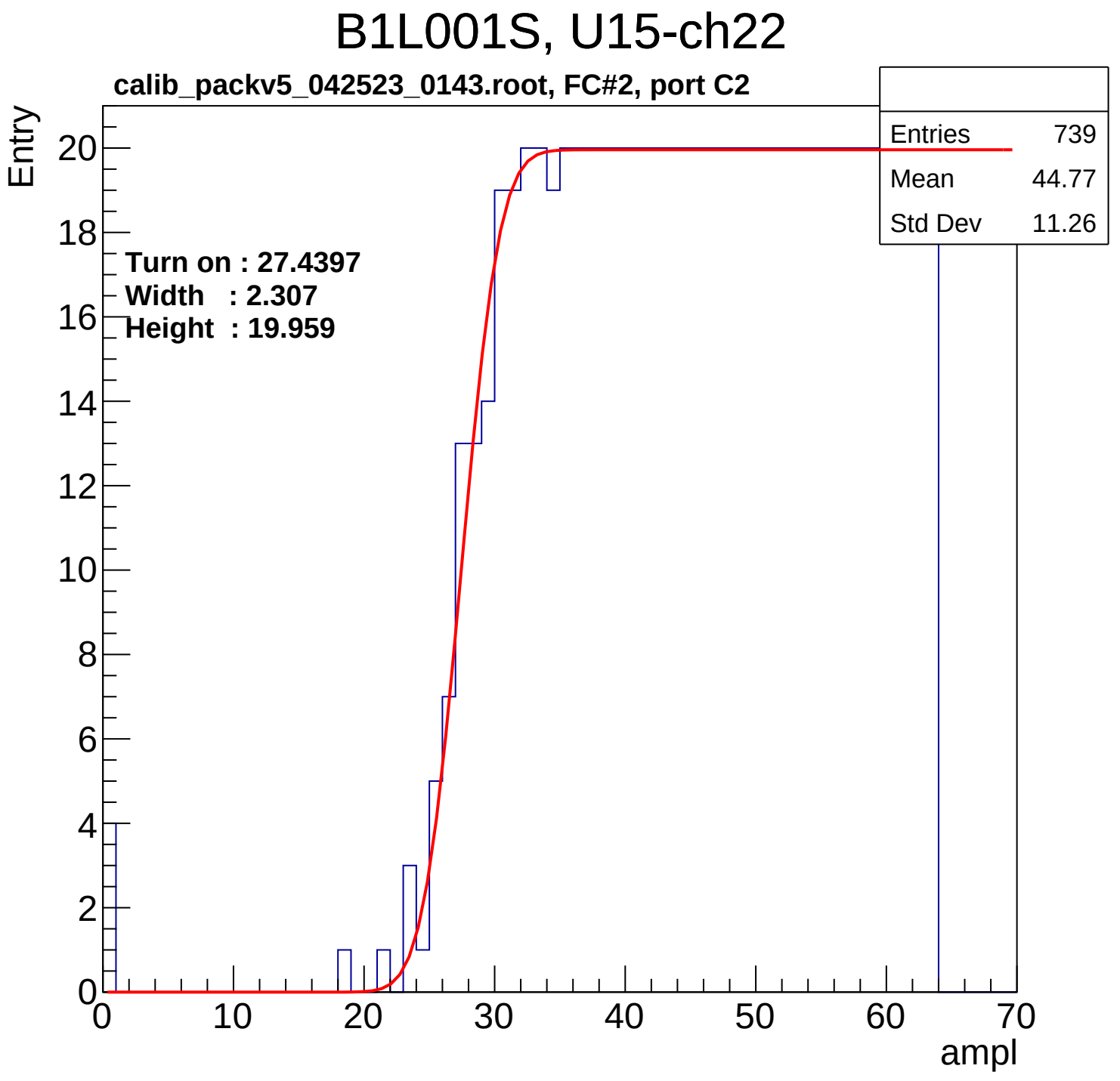
B1L001S, U15-ch22
calib_packv5_042523_0143.root, FC#2, port C2
Entries 739
Mean 44.77
Std Dev 11.26
Turn on : 27.4397
Width : 2.307
Height : 19.959
Entry
ampl
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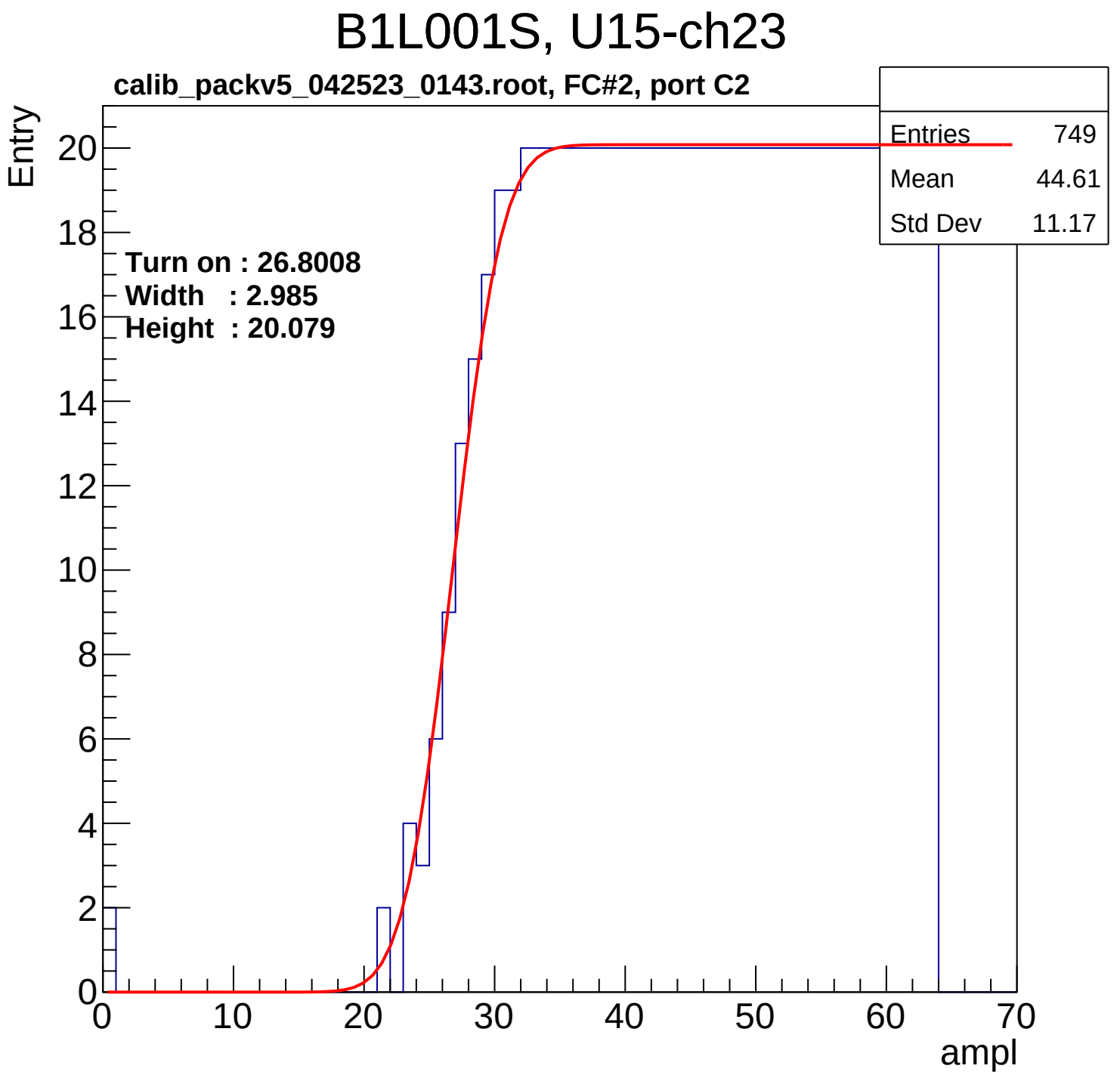
B1L001S, U15-ch23
calib_packv5_042523_0143.root, FC#2, port C2
Entries 749
Mean 44.61
Std Dev 11.17
Turn on : 26.8008
Width : 2.985
Height : 20.079
Entry
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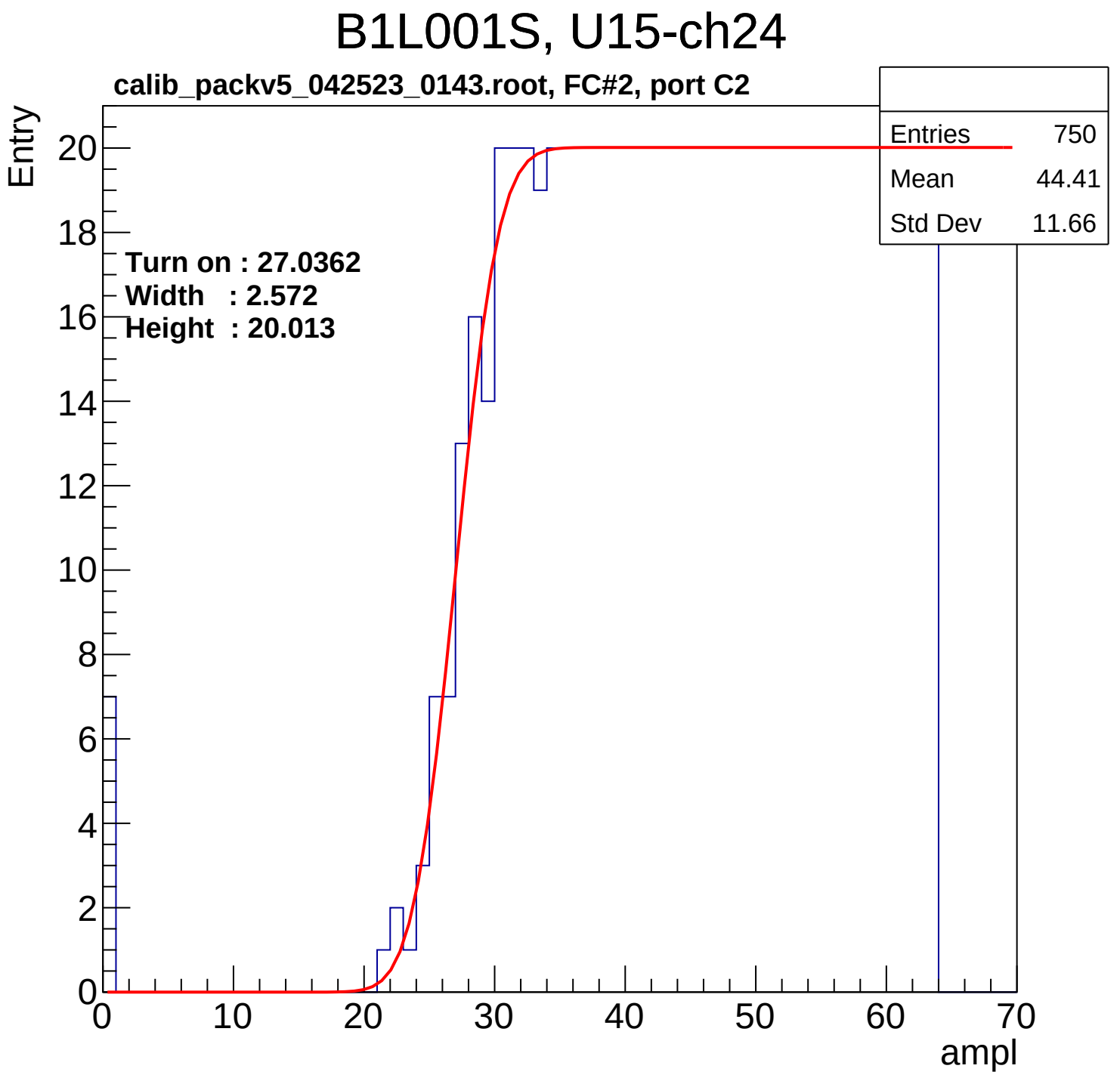
B1L001S, U15-ch24
calib_packv5_042523_0143.root, FC#2, port C2
Entries 750
Mean 44.41
Std Dev 11.66
Turn on : 27.0362
Width : 2.572
Height : 20.013
Entry
ampl
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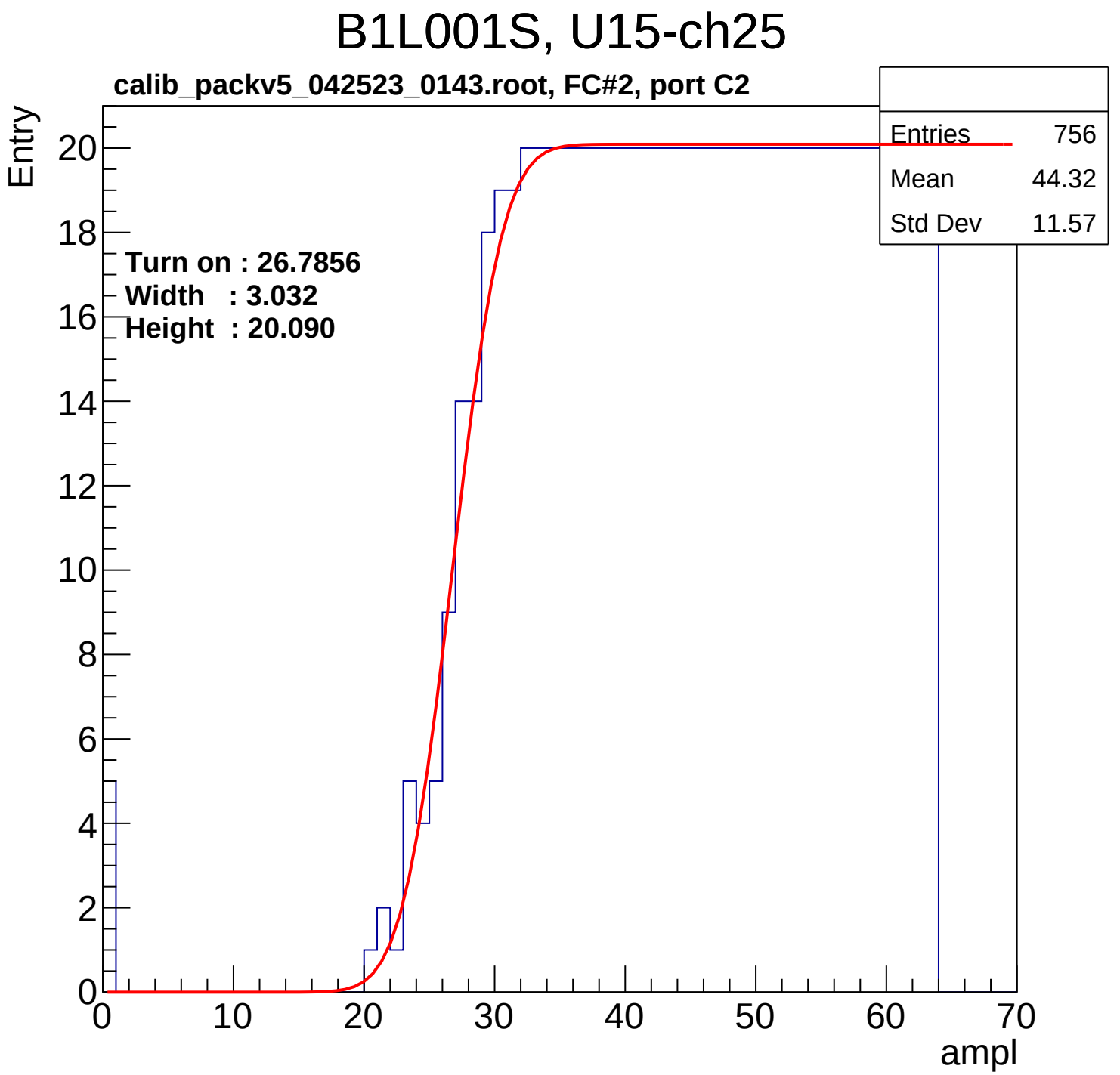
B1L001S, U15-ch25
calib_packv5_042523_0143.root, FC#2, port C2
Entries 756
Mean 44.32
Std Dev 11.57
Turn on : 26.7856
Width : 3.032
Height : 20.090
Entry
ampl
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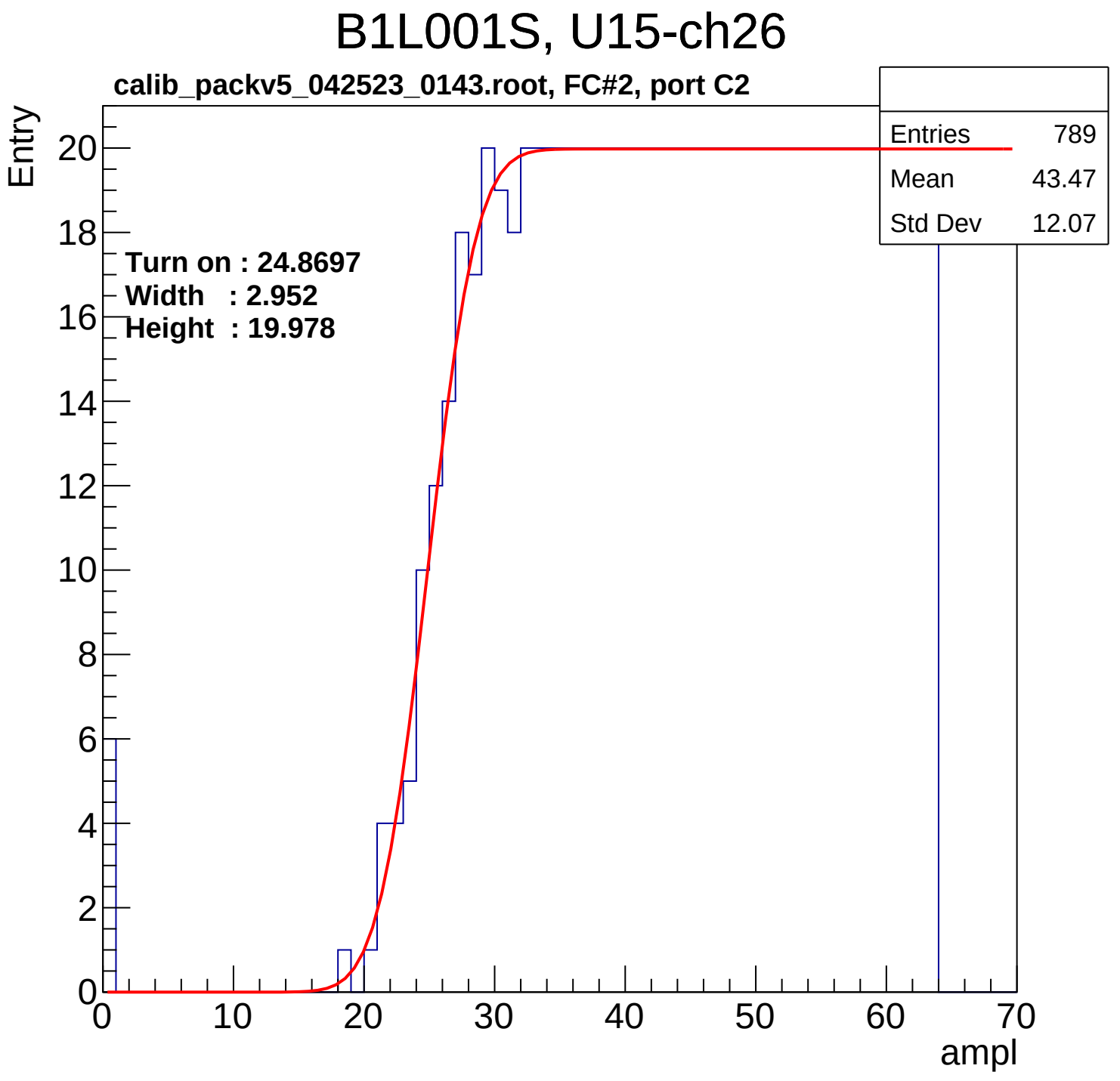
B1L001S, U15-ch26
calib_packv5_042523_0143.root, FC#2, port C2
Entries 789
Mean 43.47
Std Dev 12.07
Turn on : 24.8697
Width : 2.952
Height : 19.978
Entry
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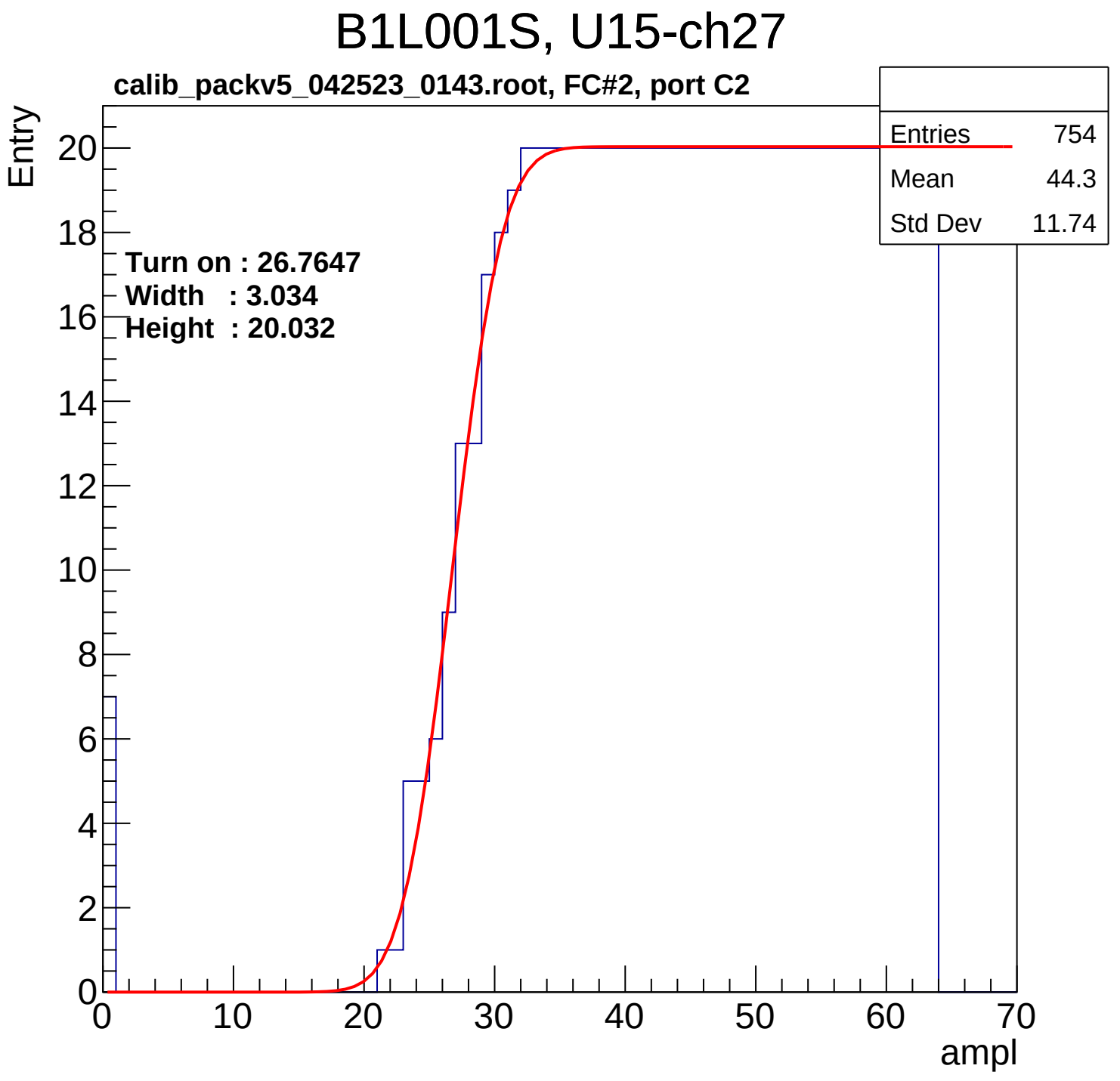
B1L001S, U15-ch27
calib_packv5_042523_0143.root, FC#2, port C2
Entries 754
Mean 44.3
Std Dev 11.74
Turn on : 26.7647
Width : 3.034
Height : 20.032
Entry
ampl
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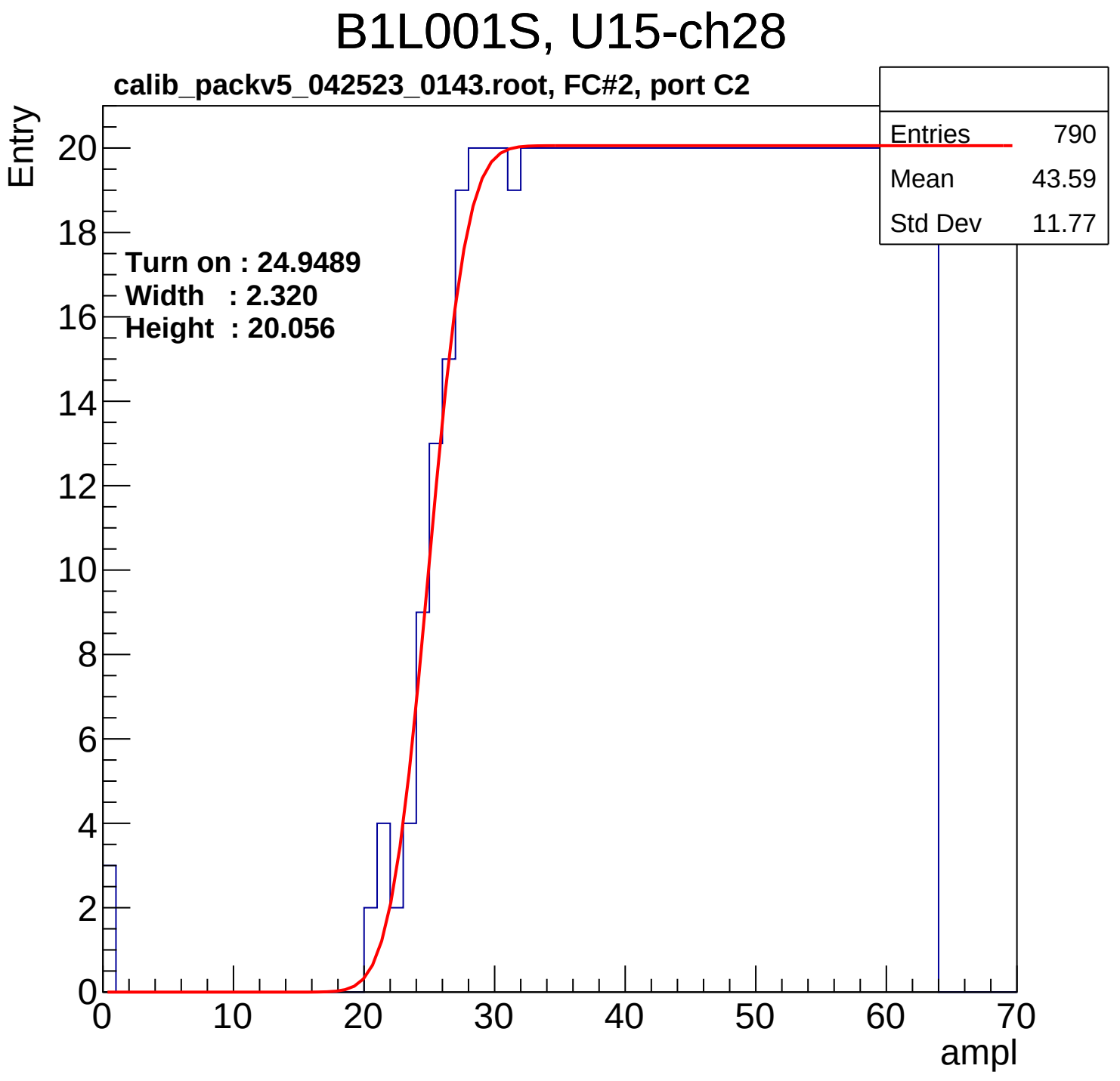
B1L001S, U15-ch28
calib_packv5_042523_0143.root, FC#2, port C2
Entries 790
Mean 43.59
Std Dev 11.77
Turn on : 24.9489
Width : 2.320
Height : 20.056
Entry
ampl
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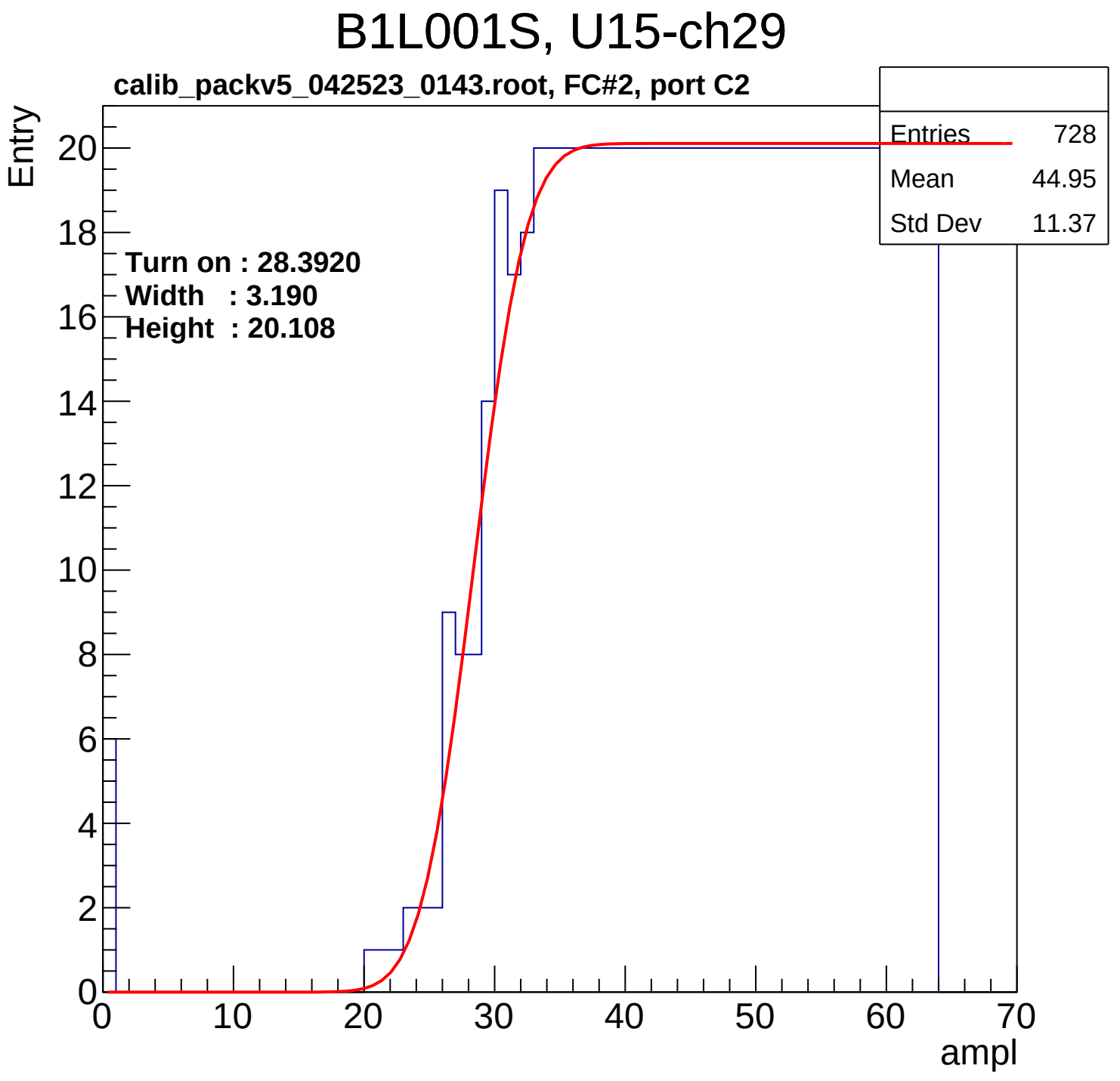
B1L001S, U15-ch29
calib_packv5_042523_0143.root, FC#2, port C2
Entries 728
Mean 44.95
Std Dev 11.37
Turn on : 28.3920
Width : 3.190
Height : 20.108
Entry
ampl
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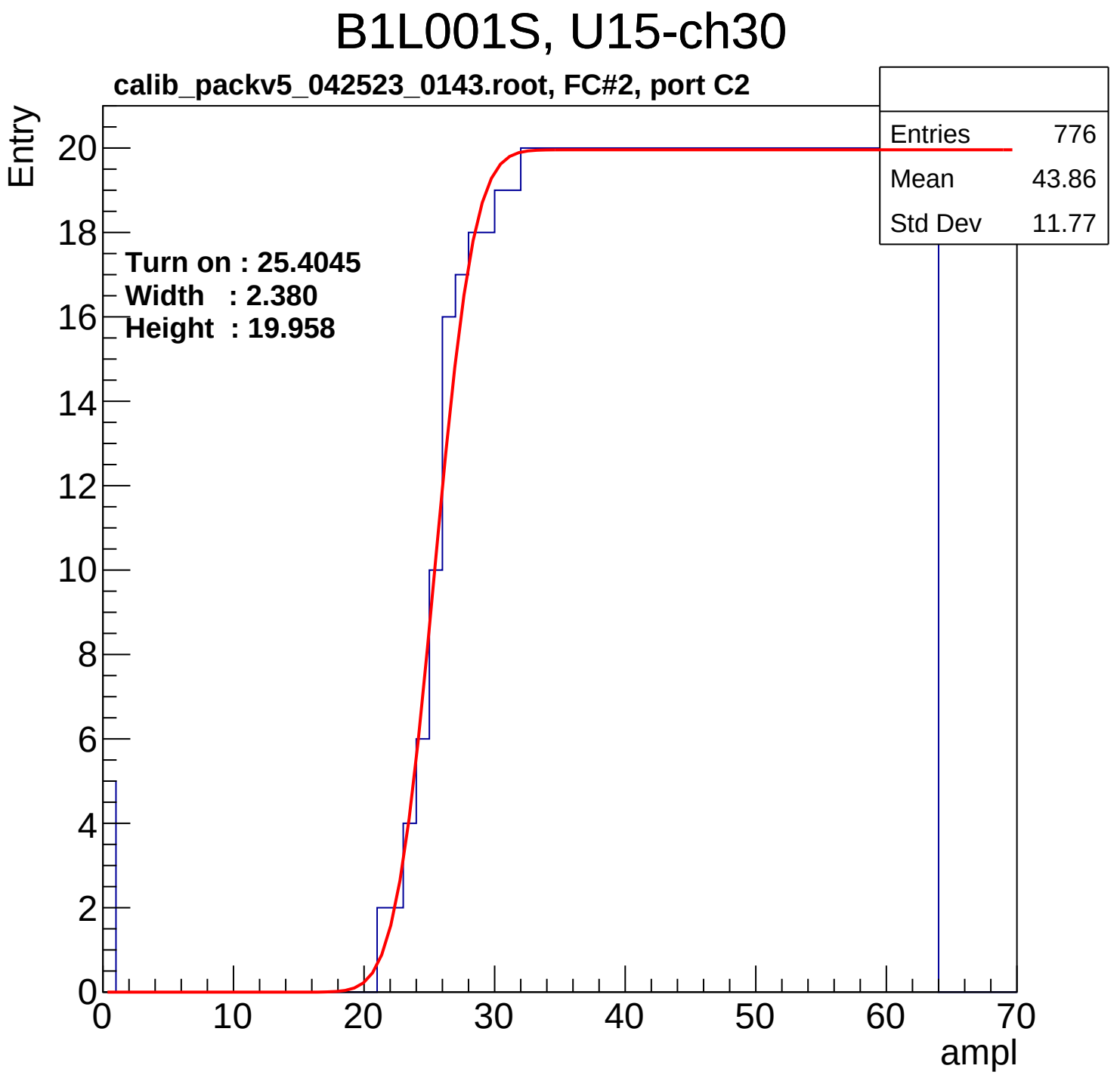
B1L001S, U15-ch30
calib_packv5_042523_0143.root, FC#2, port C2
Entries 776
Mean 43.86
Std Dev 11.77
Turn on : 25.4045
Width : 2.380
Height : 19.958
Entry
ampl
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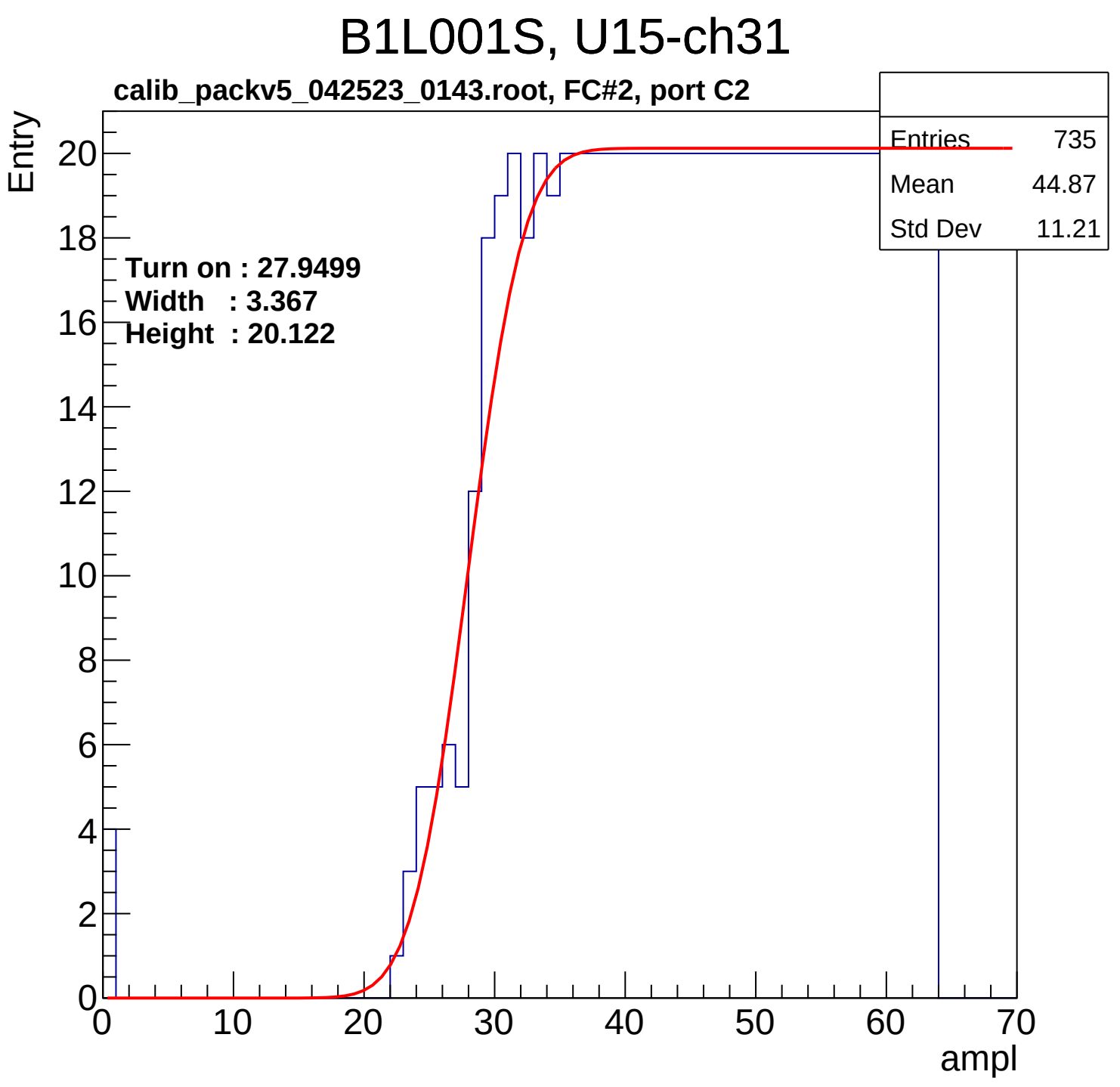
B1L001S, U15-ch31
calib_packv5_042523_0143.root, FC#2, port C2
Entries 735
Mean 44.87
Std Dev 11.21
Turn on : 27.9499
Width : 3.367
Height : 20.122
Entry
ampl
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6
8
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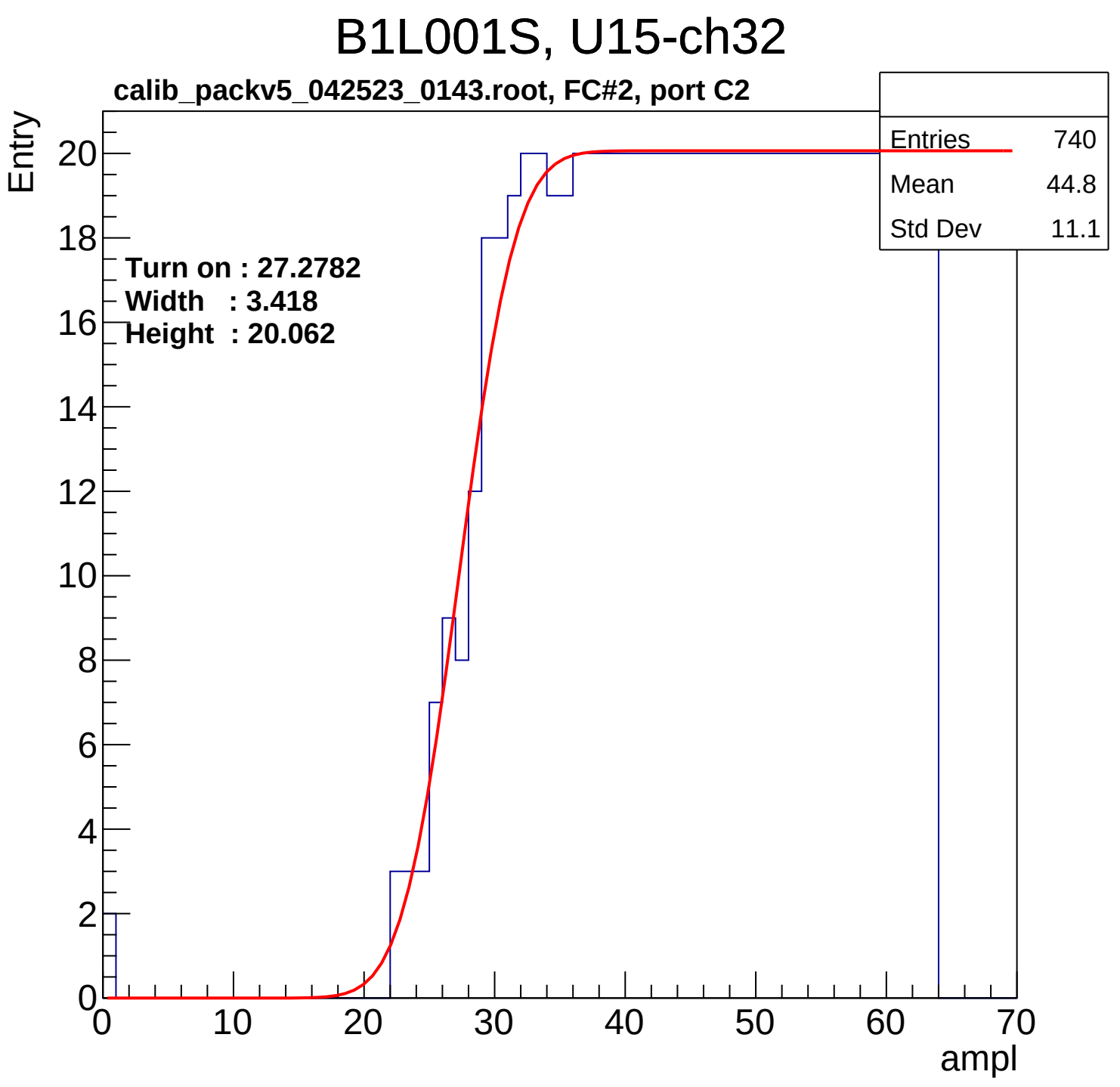
B1L001S, U15-ch32
calib_packv5_042523_0143.root, FC#2, port C2
Entries 740
Mean 44.8
Std Dev 11.1
Turn on : 27.2782
Width : 3.418
Height : 20.062
Entry
ampl
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6
8
10
12
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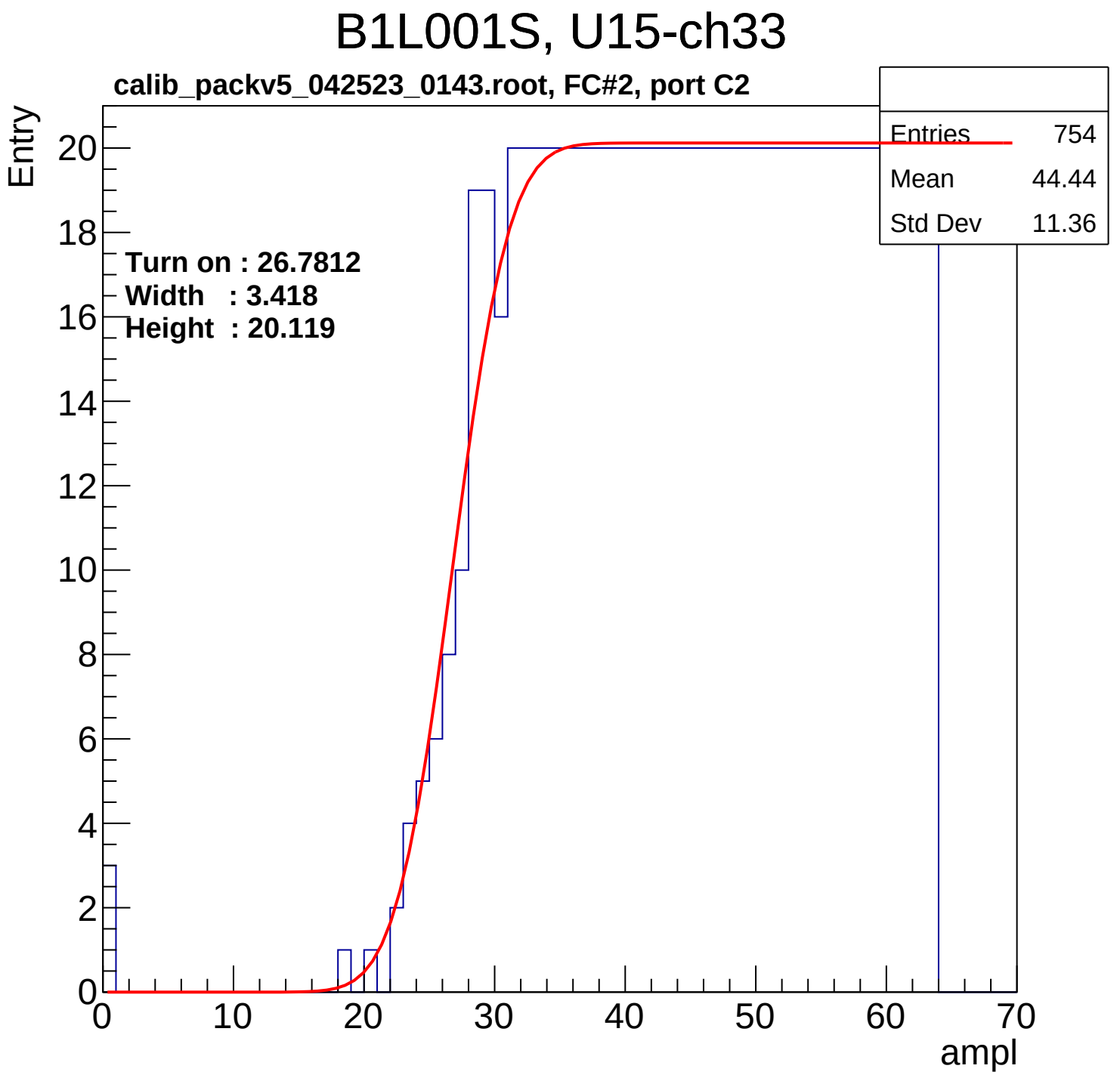
B1L001S, U15-ch33
calib_packv5_042523_0143.root, FC#2, port C2
Entries 754
Mean 44.44
Std Dev 11.36
Turn on : 26.7812
Width : 3.418
Height : 20.119
Entry
ampl
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6
8
10
12
14
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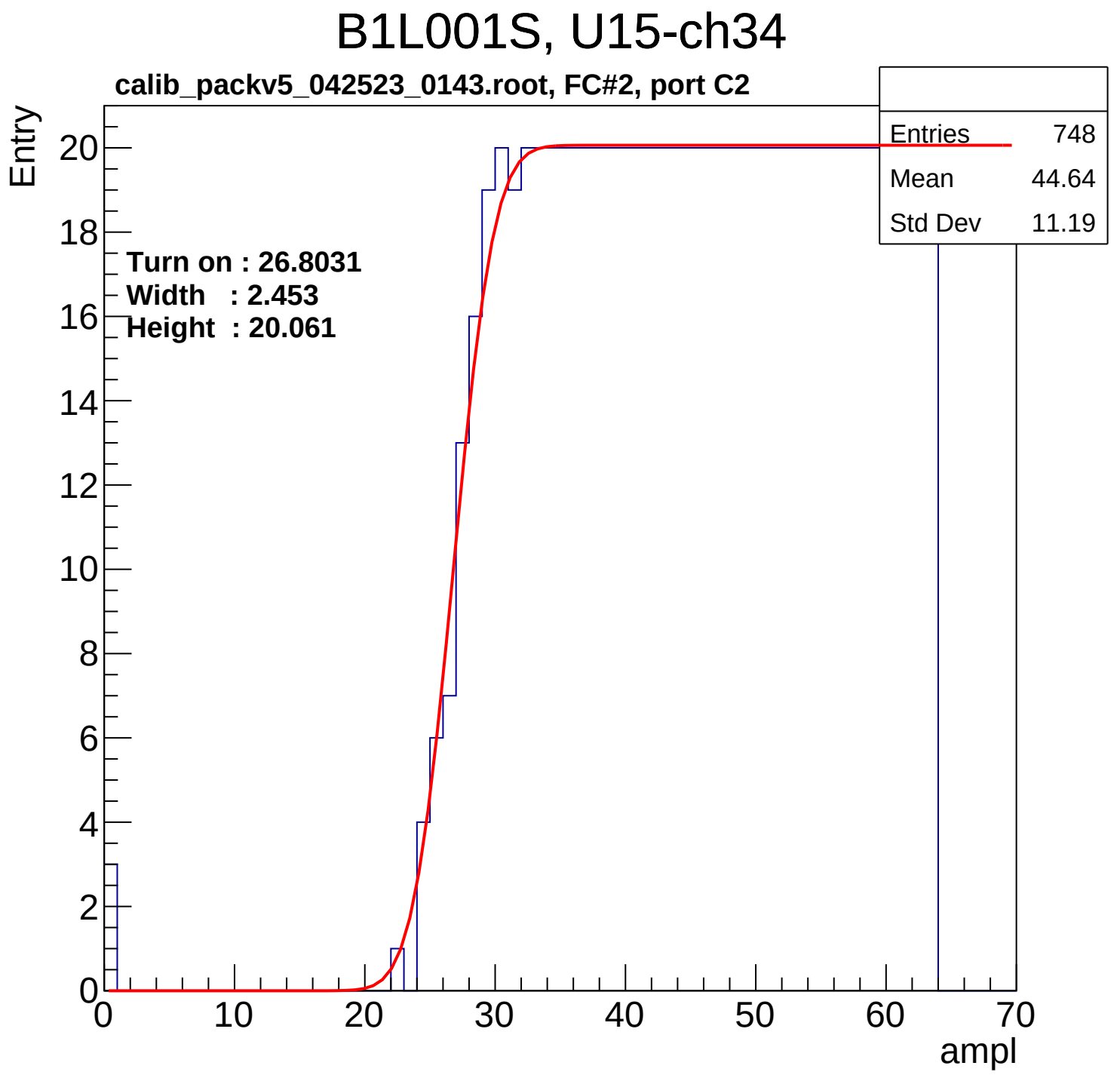
B1L001S, U15-ch34
calib_packv5_042523_0143.root, FC#2, port C2
Entries 748
Mean 44.64
Std Dev 11.19
Turn on : 26.8031
Width : 2.453
Height : 20.061
Entry
ampl
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6
8
10
12
14
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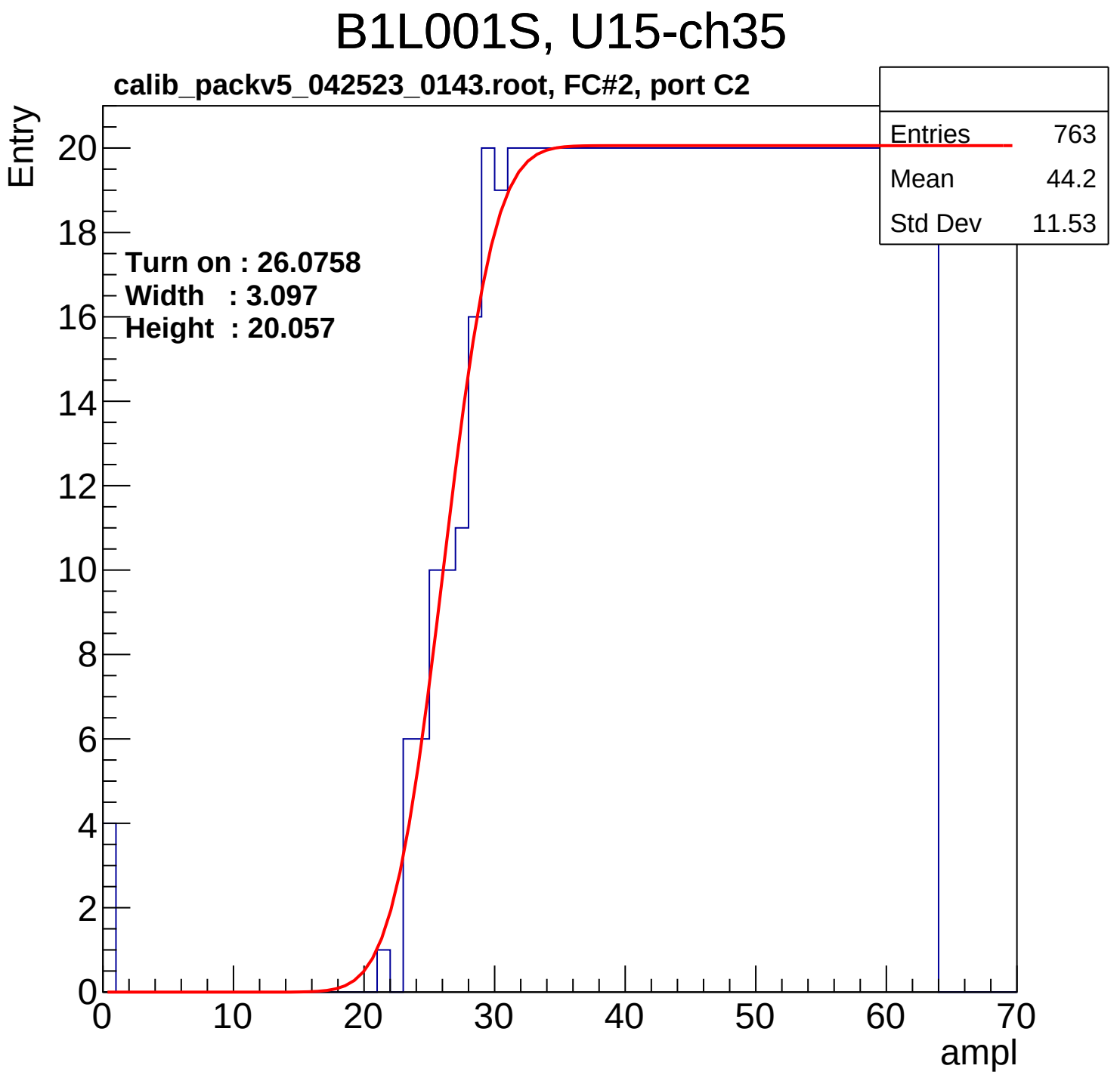
B1L001S, U15-ch35
calib_packv5_042523_0143.root, FC#2, port C2
Entries 763
Mean 44.2
Std Dev 11.53
Turn on : 26.0758
Width : 3.097
Height : 20.057
Entry
ampl
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6
8
10
12
14
16
18
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0
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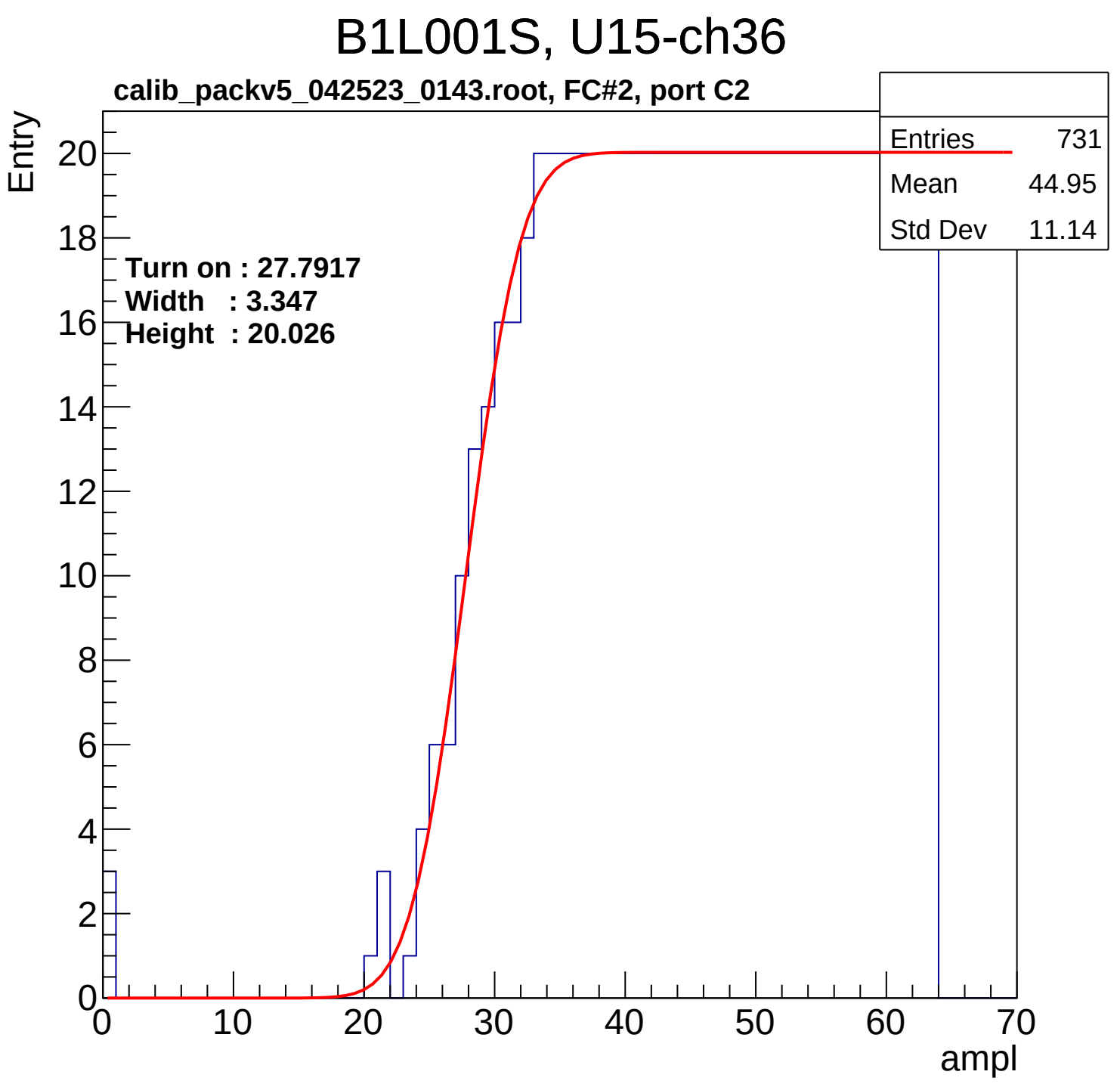
B1L001S, U15-ch36
calib_packv5_042523_0143.root, FC#2, port C2
Entries 731
Mean 44.95
Std Dev 11.14
Turn on : 27.7917
Width : 3.347
Height : 20.026
Entry
ampl
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6
8
10
12
14
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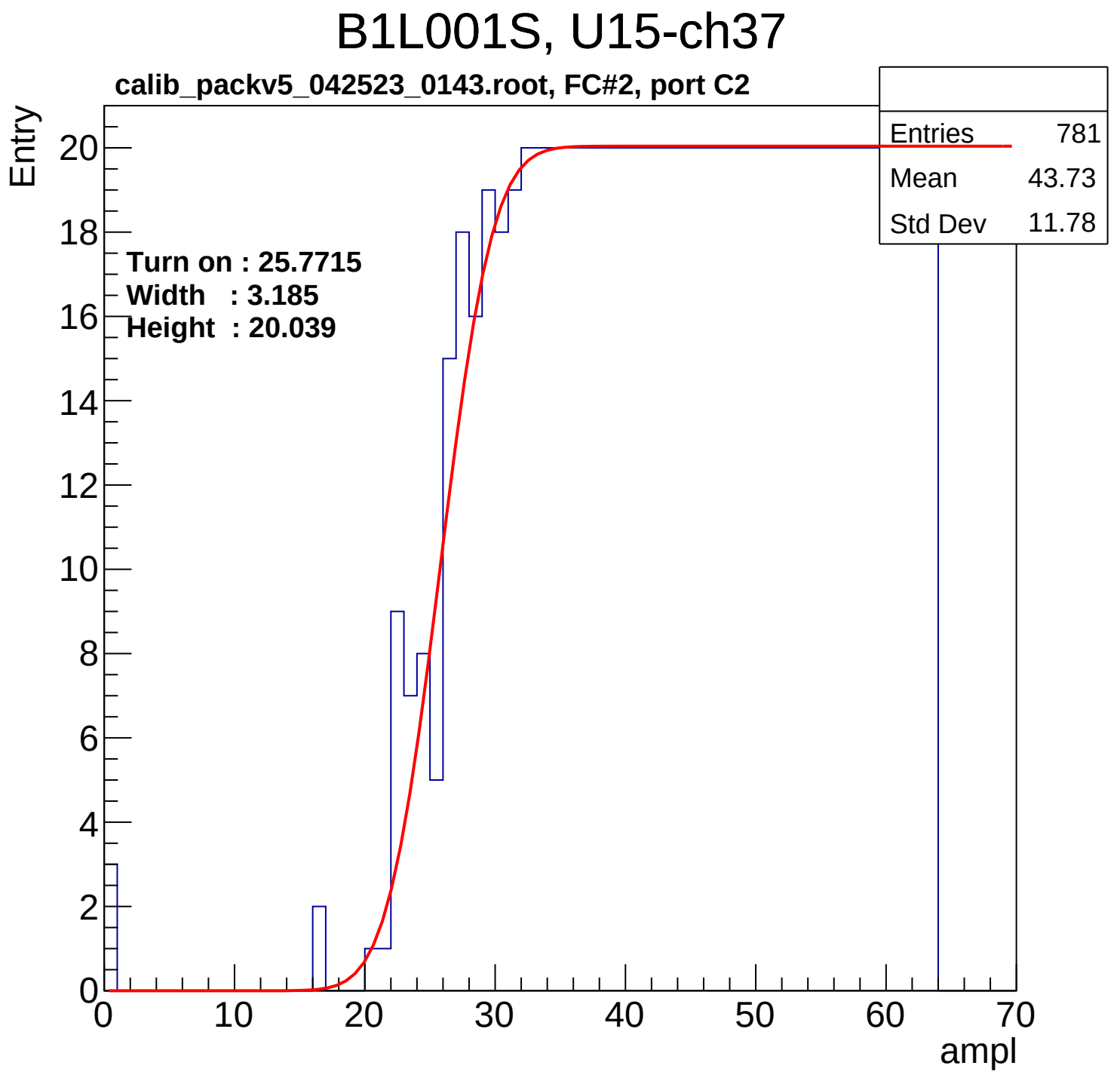
B1L001S, U15-ch37
calib_packv5_042523_0143.root, FC#2, port C2
Entries 781
Mean 43.73
Std Dev 11.78
Turn on : 25.7715
Width : 3.185
Height : 20.039
Entry
ampl
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8
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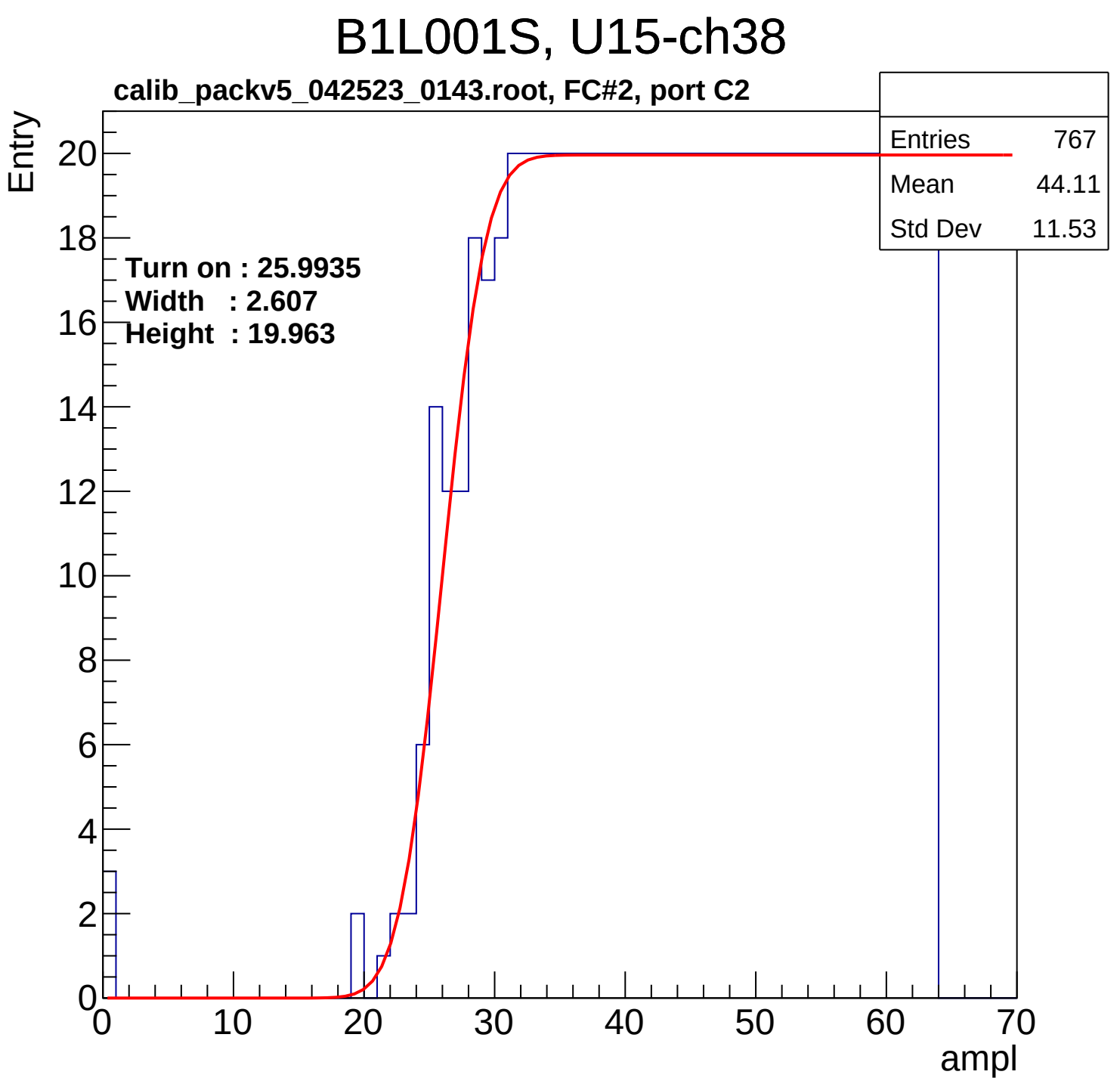
B1L001S, U15-ch38
calib_packv5_042523_0143.root, FC#2, port C2
Entries 767
Mean 44.11
Std Dev 11.53
Turn on : 25.9935
Width : 2.607
Height : 19.963
Entry
ampl
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6
8
10
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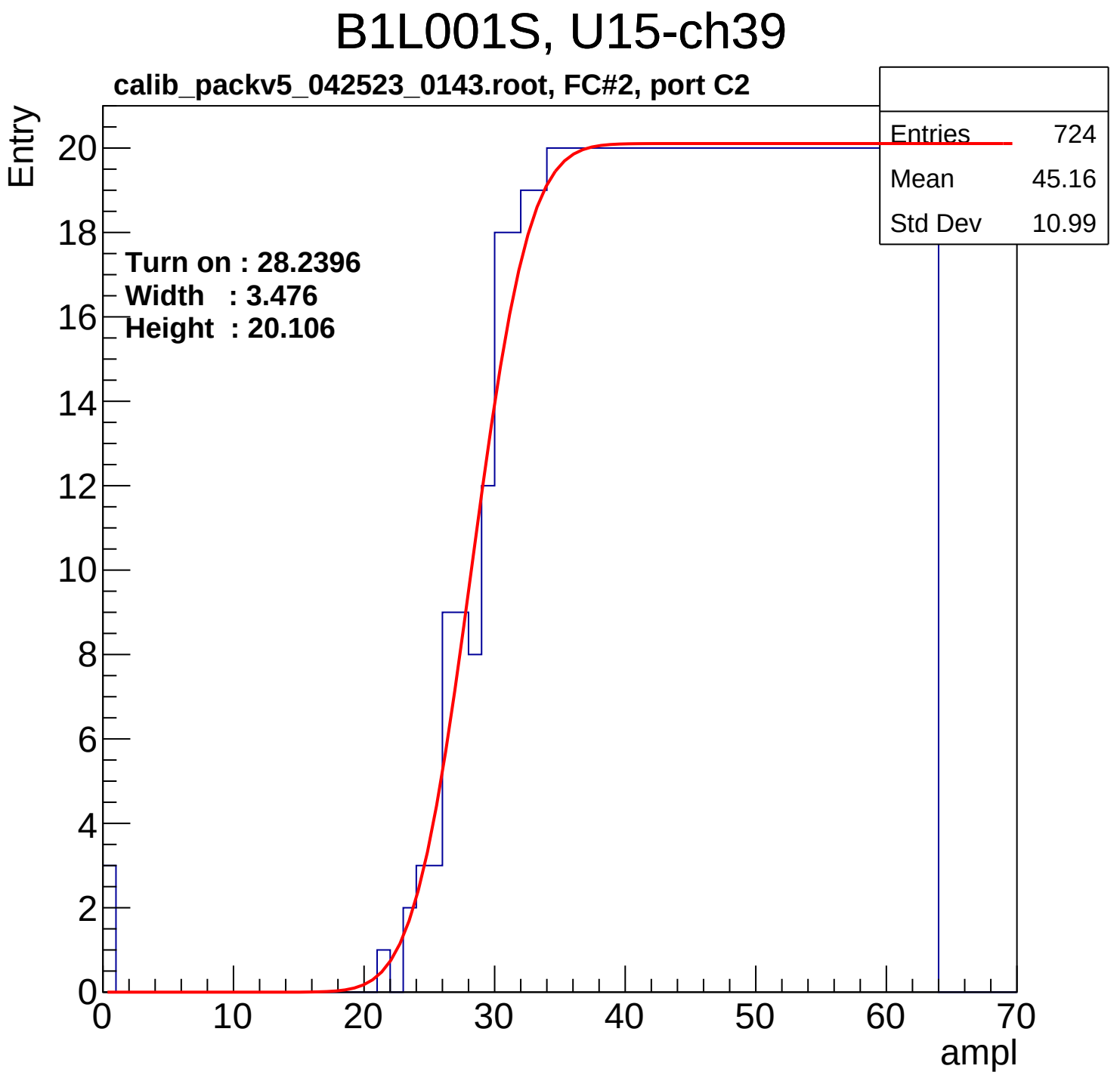
B1L001S, U15-ch39
calib_packv5_042523_0143.root, FC#2, port C2
Entries 724
Mean 45.16
Std Dev 10.99
Turn on : 28.2396
Width : 3.476
Height : 20.106
Entry
ampl
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8
10
12
14
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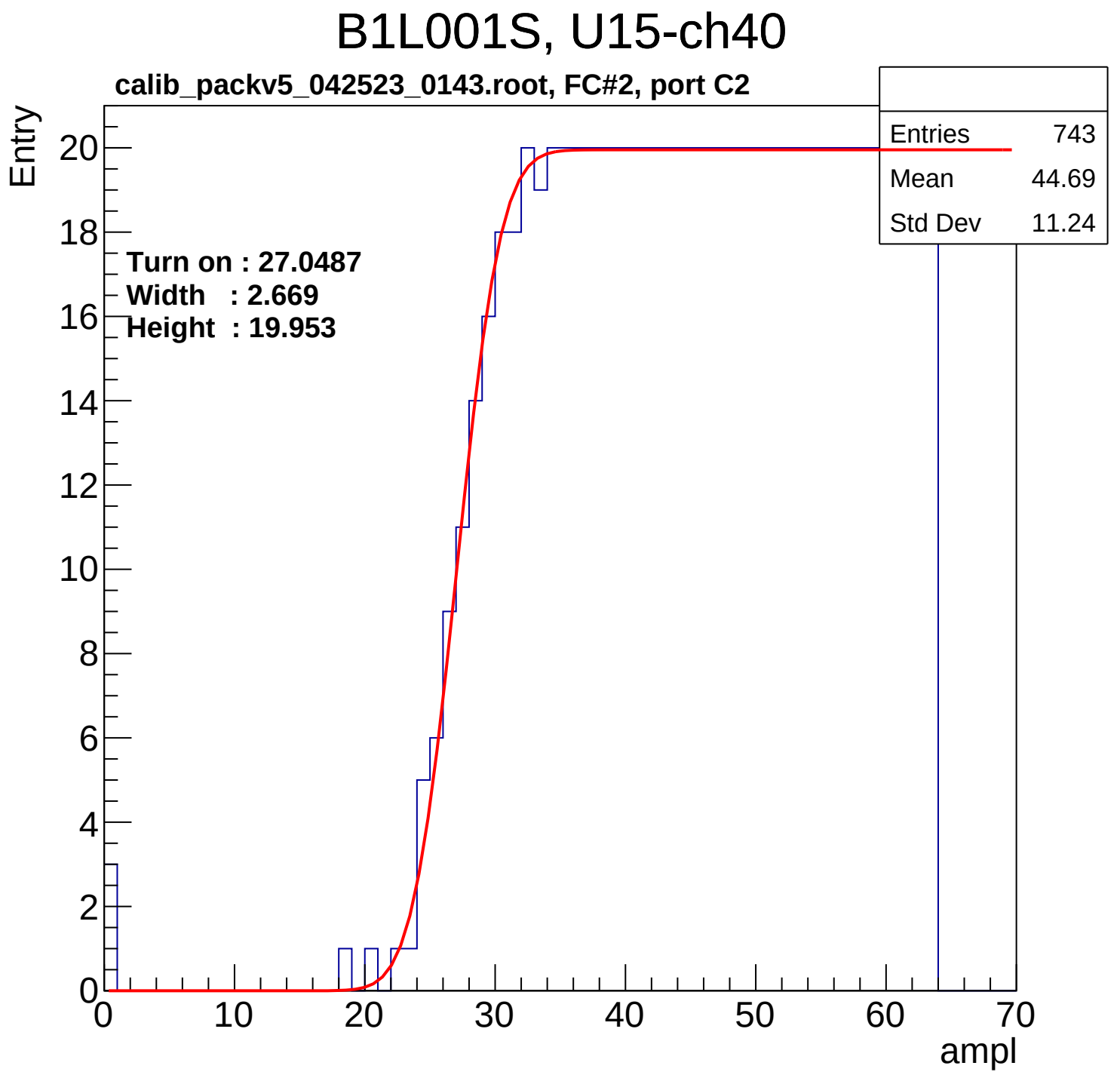
B1L001S, U15-ch40
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.69
Std Dev 11.24
Turn on : 27.0487
Width : 2.669
Height : 19.953
Entry
ampl
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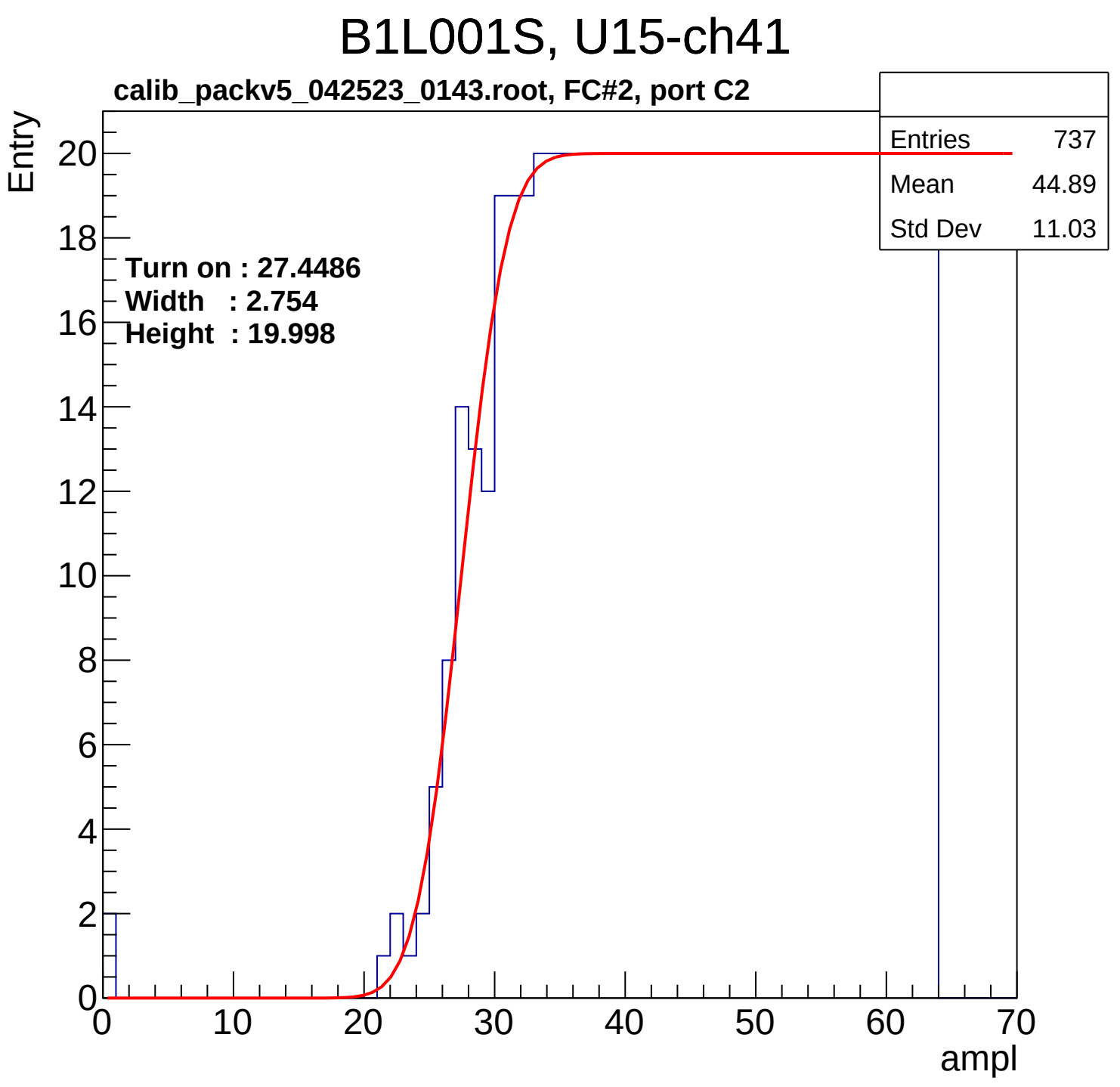
B1L001S, U15-ch41
calib_packv5_042523_0143.root, FC#2, port C2
Entries 737
Mean 44.89
Std Dev 11.03
Turn on : 27.4486
Width : 2.754
Height : 19.998
Entry
ampl
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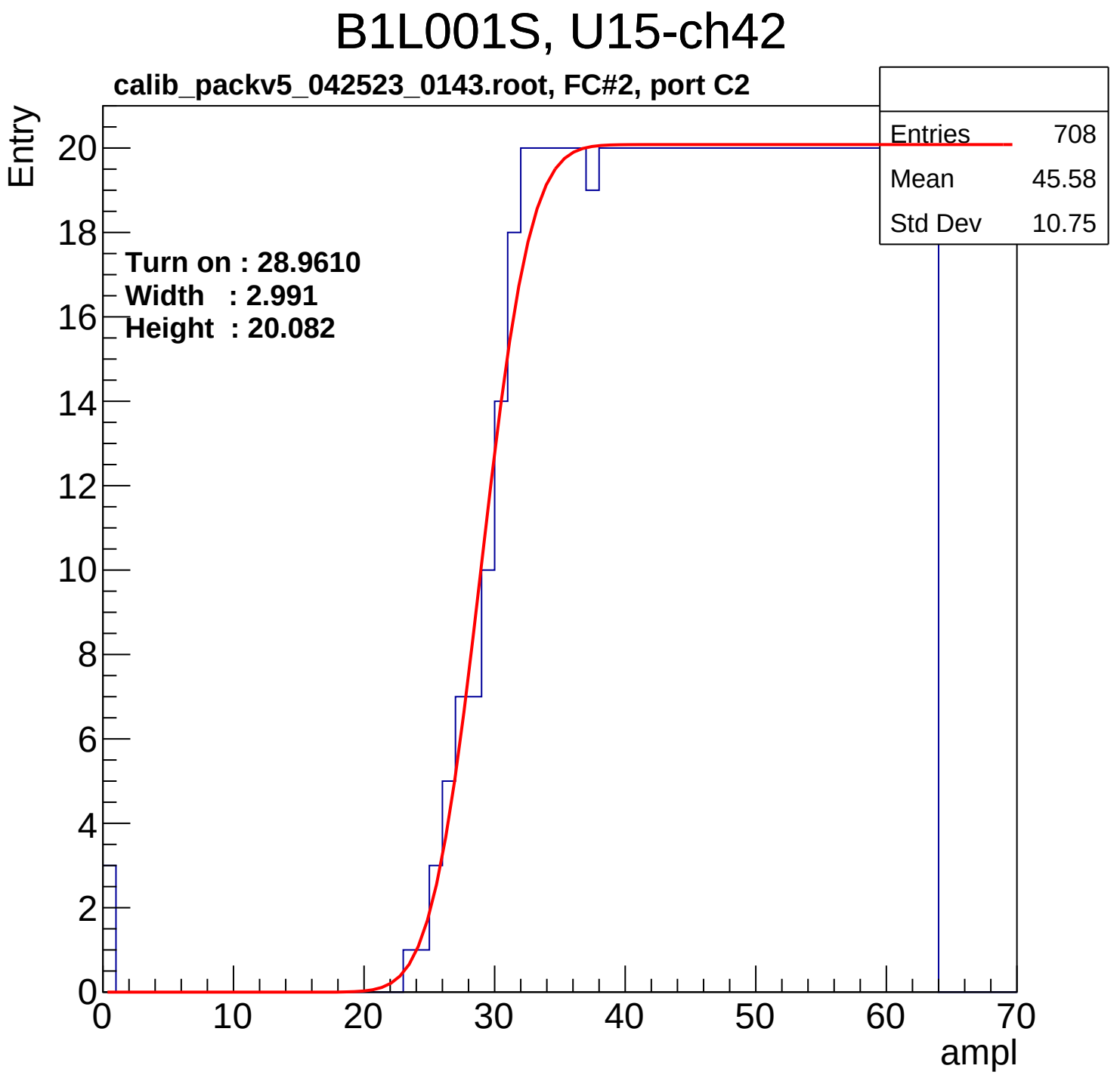
B1L001S, U15-ch42
calib_packv5_042523_0143.root, FC#2, port C2
Entries 708
Mean 45.58
Std Dev 10.75
Turn on : 28.9610
Width : 2.991
Height : 20.082
Entry
ampl
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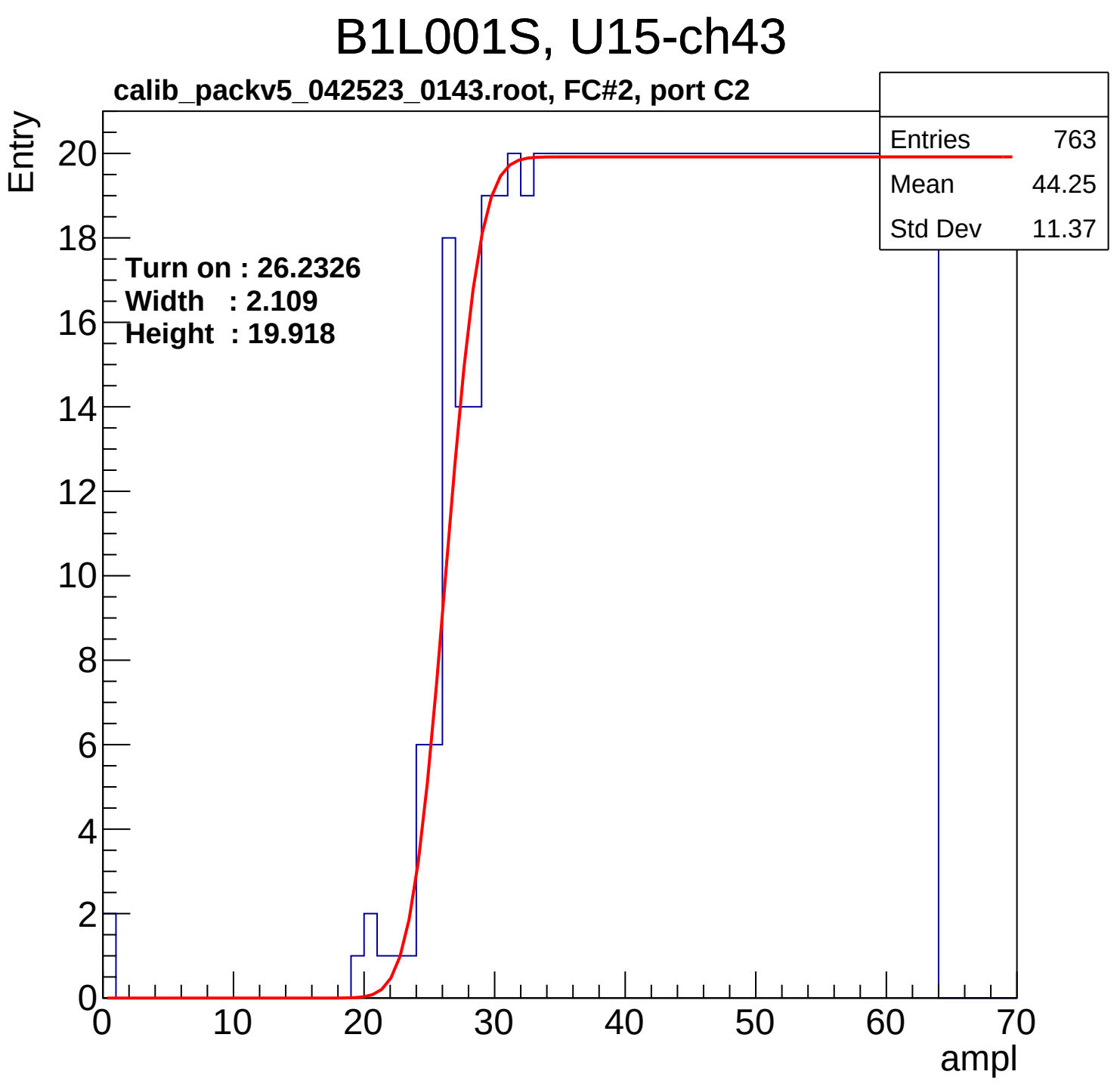
B1L001S, U15-ch43
calib_packv5_042523_0143.root, FC#2, port C2
Entries 763
Mean 44.25
Std Dev 11.37
Turn on : 26.2326
Width : 2.109
Height : 19.918
Entry
ampl
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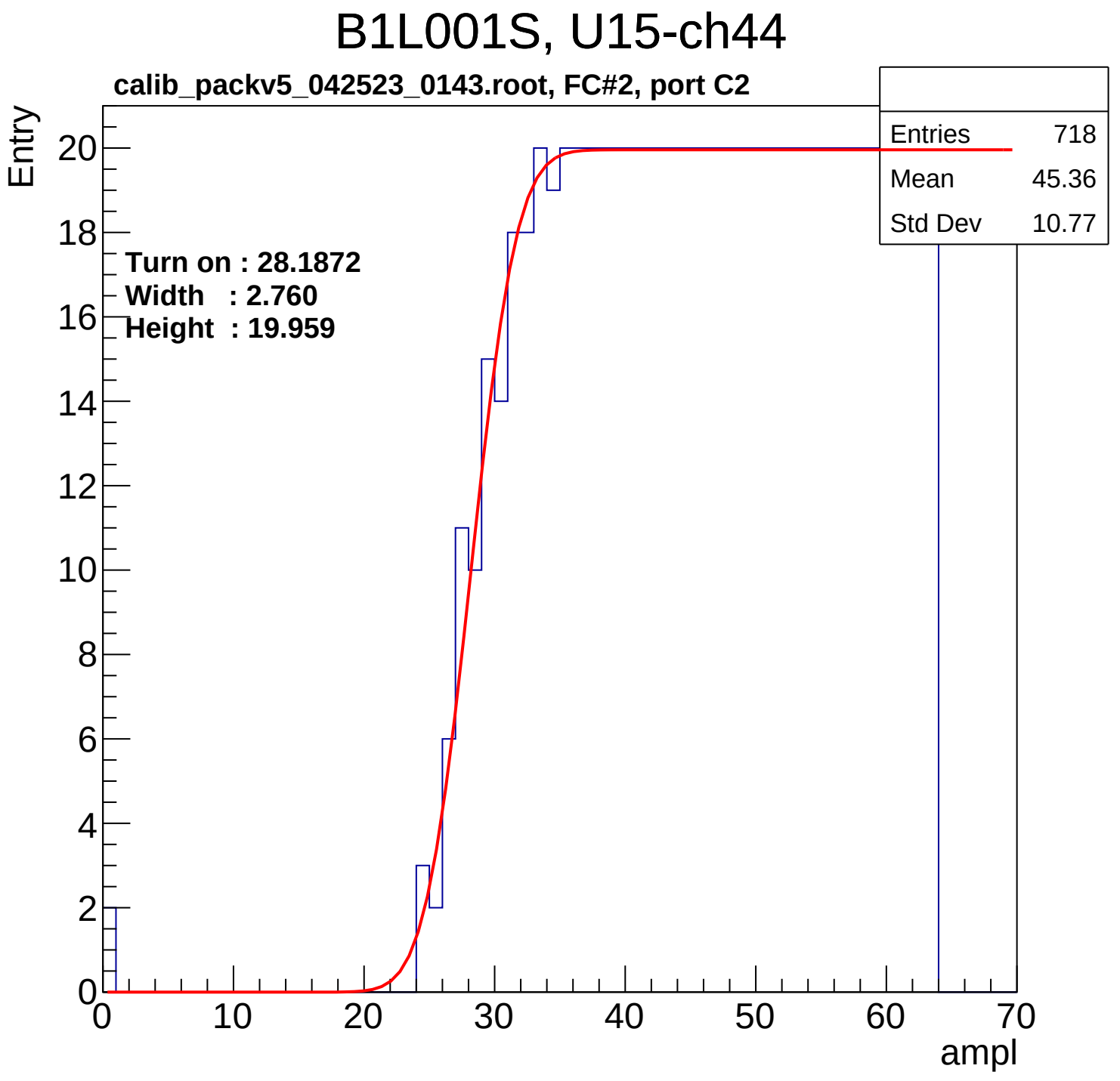
B1L001S, U15-ch44
calib_packv5_042523_0143.root, FC#2, port C2
Entries 718
Mean 45.36
Std Dev 10.77
Turn on : 28.1872
Width : 2.760
Height : 19.959
Entry
ampl
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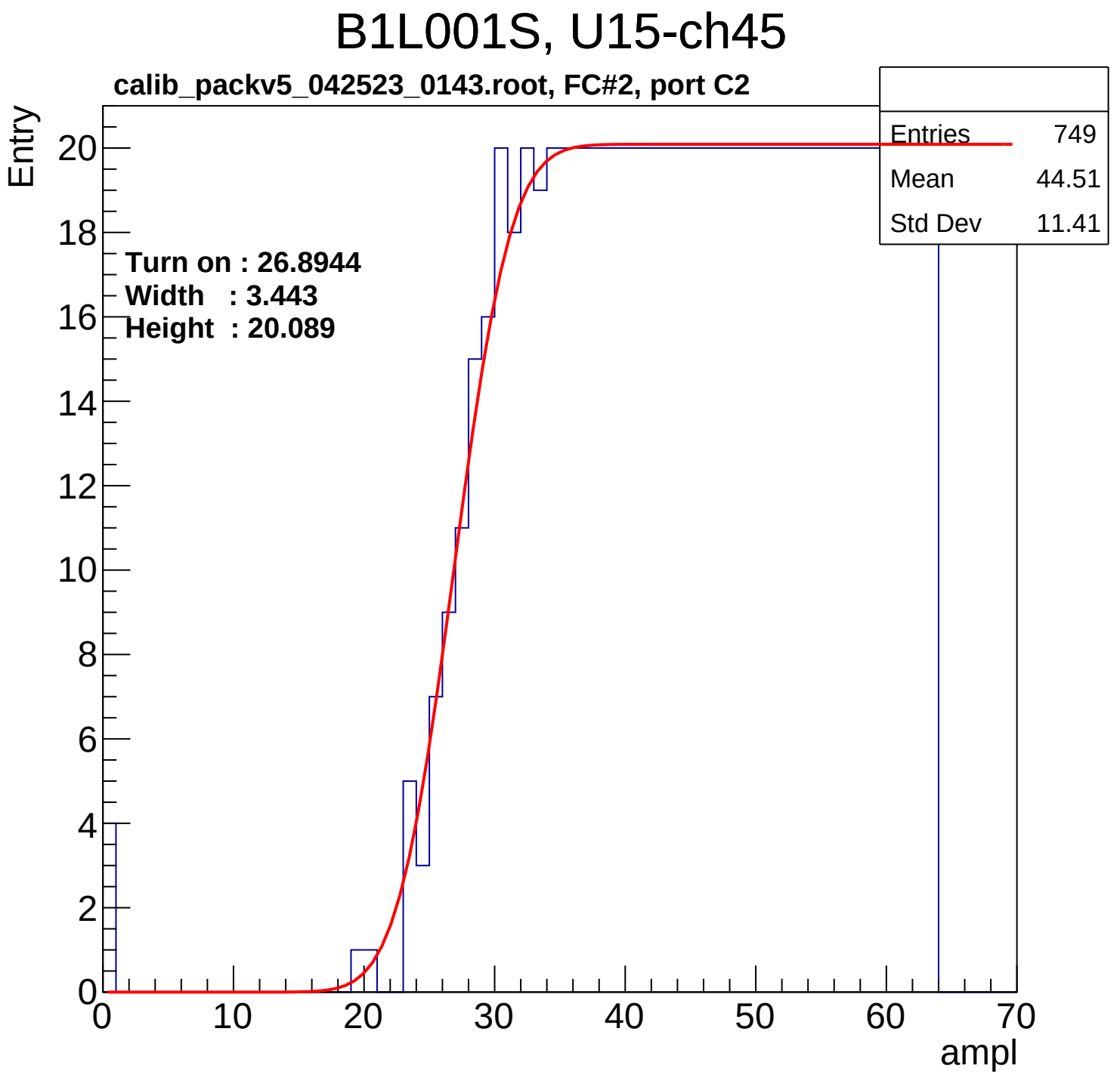
B1L001S, U15-ch45
calib_packv5_042523_0143.root, FC#2, port C2
Entries 749
Mean 44.51
Std Dev 11.41
Turn on : 26.8944
Width : 3.443
Height : 20.089
Entry
ampl
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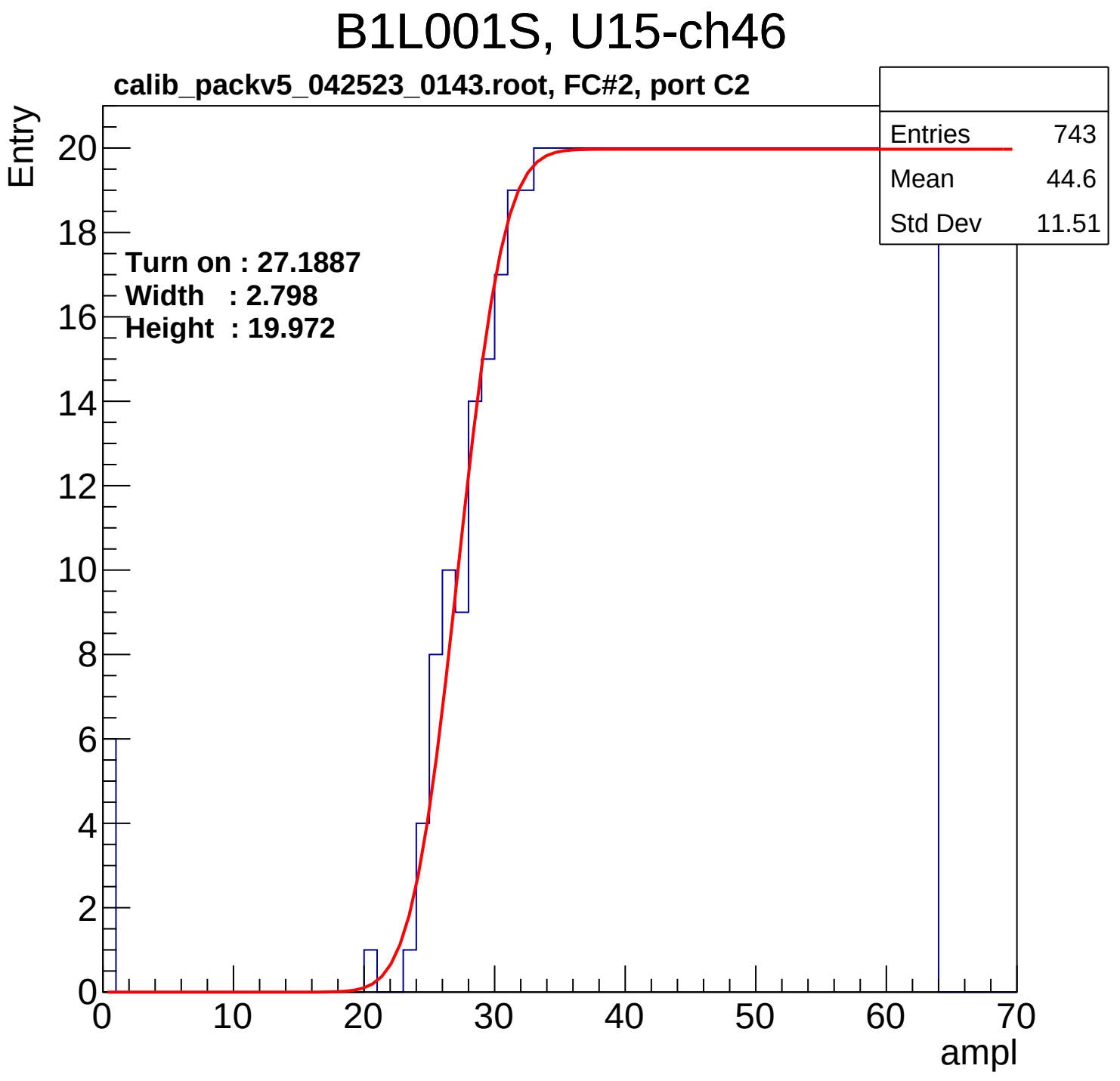
B1L001S, U15-ch46
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.6
Std Dev 11.51
Turn on : 27.1887
Width : 2.798
Height : 19.972
Entry
ampl
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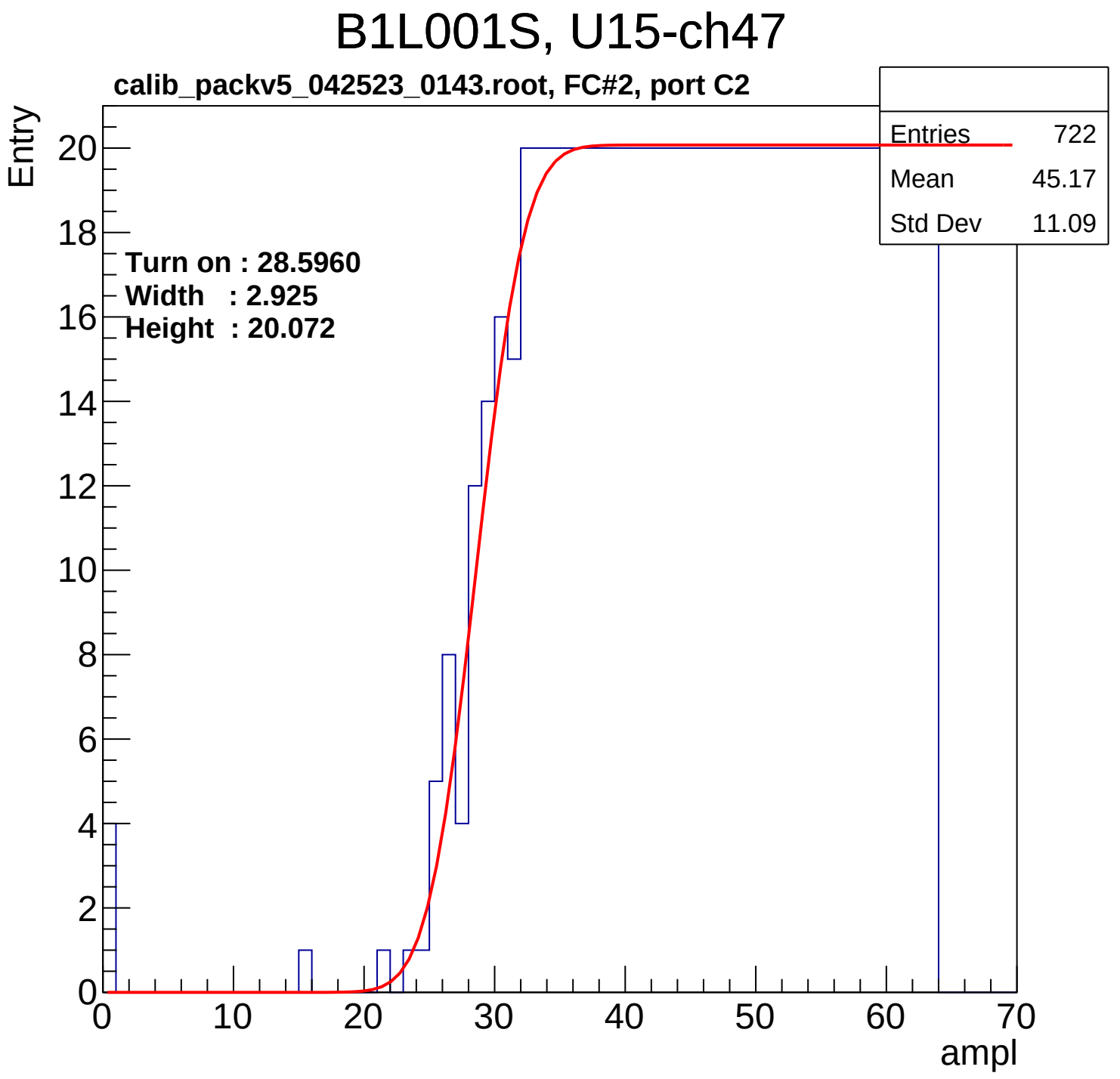
B1L001S, U15-ch47
calib_packv5_042523_0143.root, FC#2, port C2
Entries 722
Mean 45.17
Std Dev 11.09
Turn on : 28.5960
Width : 2.925
Height : 20.072
Entry
ampl
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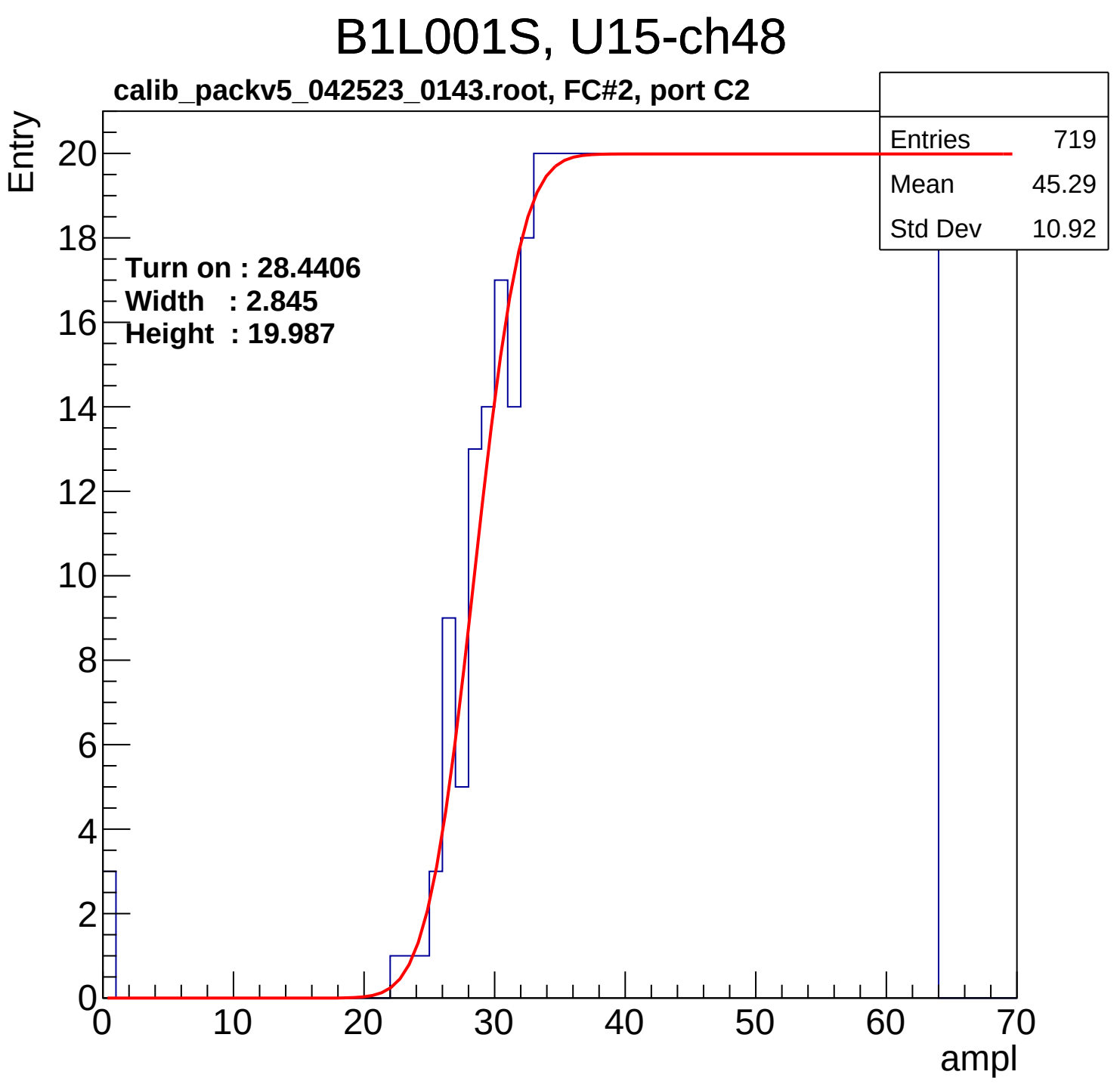
B1L001S, U15-ch48
calib_packv5_042523_0143.root, FC#2, port C2
Entries 719
Mean 45.29
Std Dev 10.92
Turn on : 28.4406
Width : 2.845
Height : 19.987
Entry
ampl
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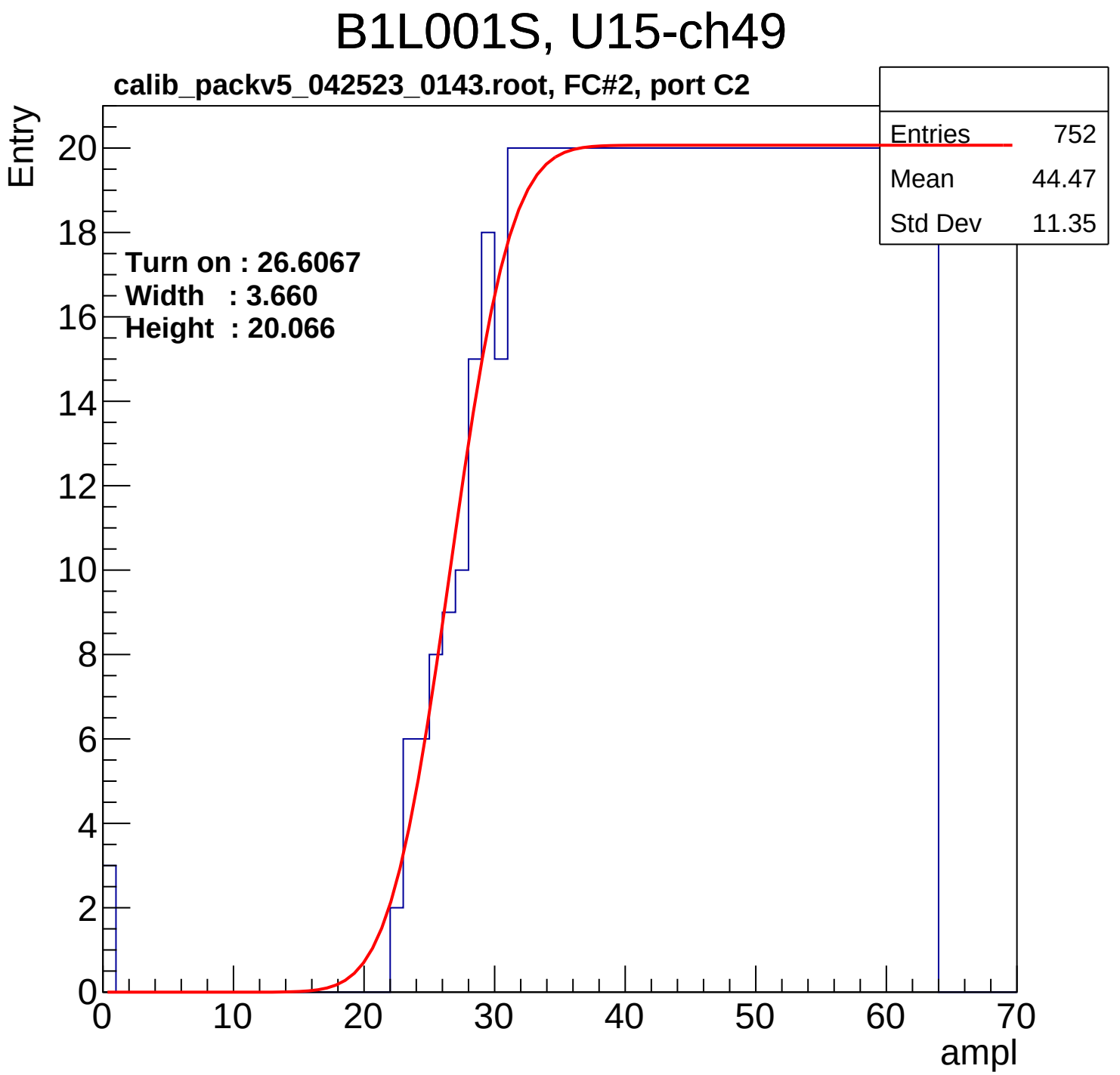
B1L001S, U15-ch49
calib_packv5_042523_0143.root, FC#2, port C2
Entries 752
Mean 44.47
Std Dev 11.35
Turn on : 26.6067
Width : 3.660
Height : 20.066
Entry
ampl
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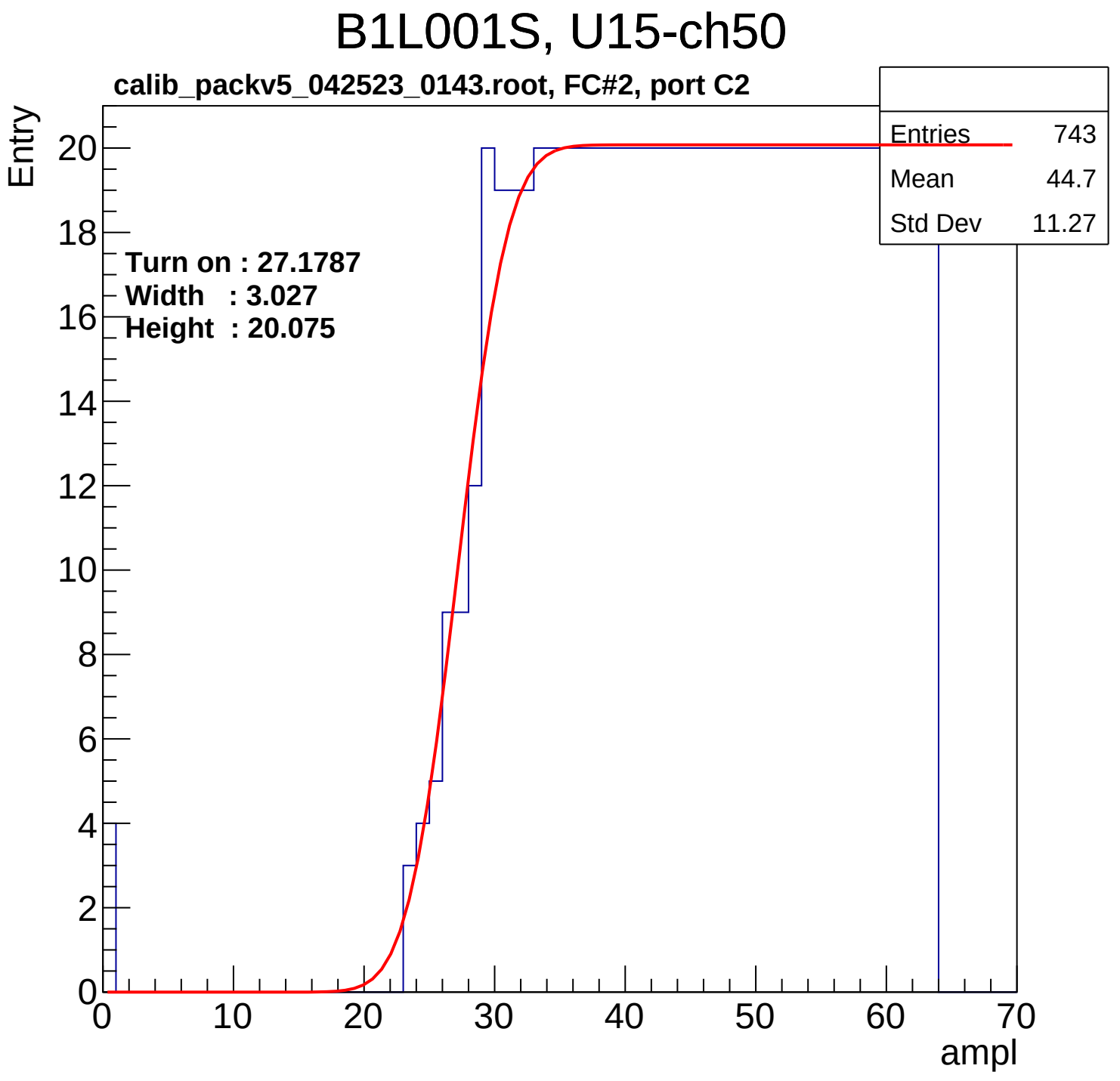
B1L001S, U15-ch50
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.7
Std Dev 11.27
Turn on : 27.1787
Width : 3.027
Height : 20.075
Entry
ampl
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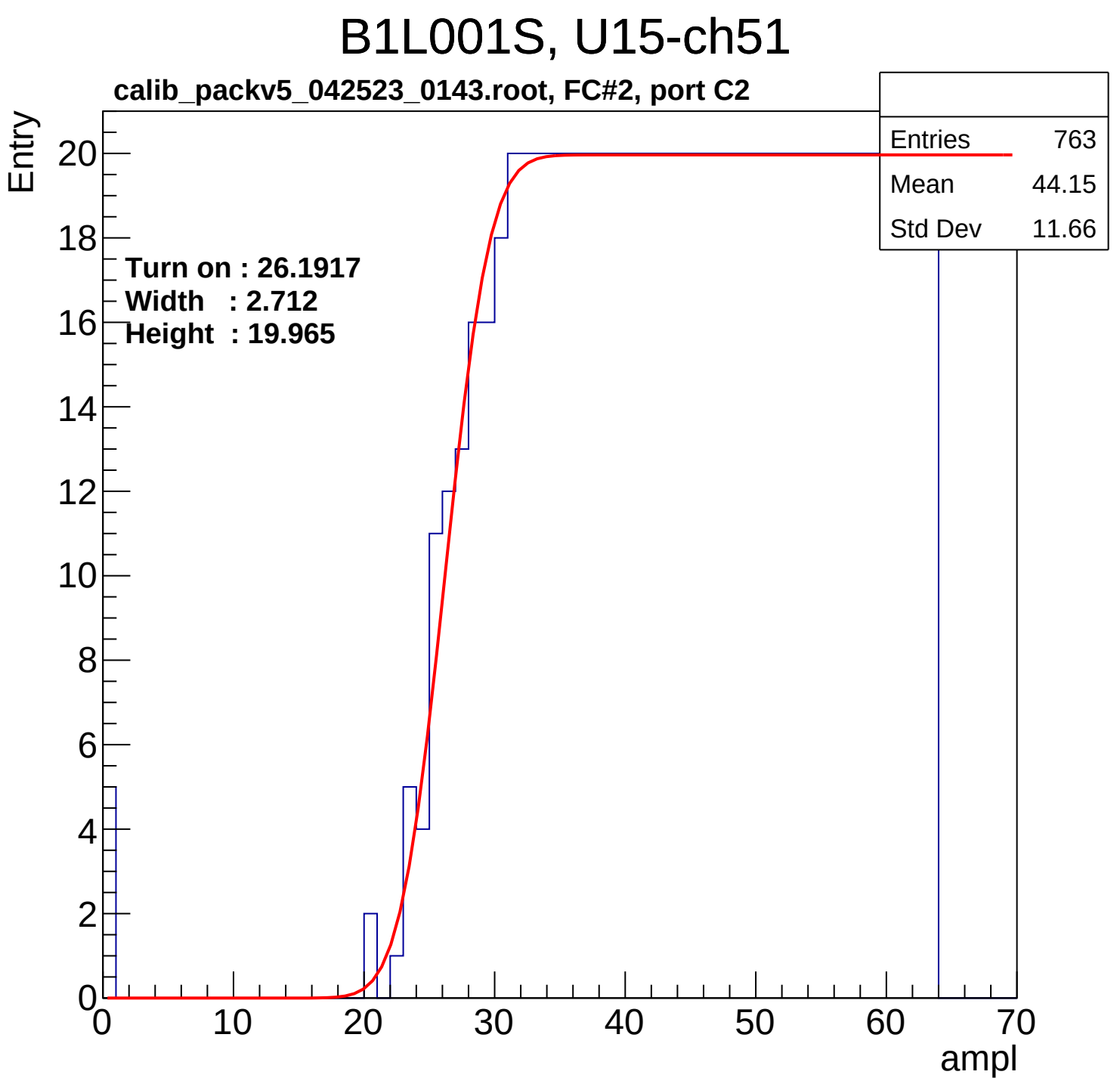
B1L001S, U15-ch51
calib_packv5_042523_0143.root, FC#2, port C2
Entries 763
Mean 44.15
Std Dev 11.66
Turn on : 26.1917
Width : 2.712
Height : 19.965
Entry
ampl
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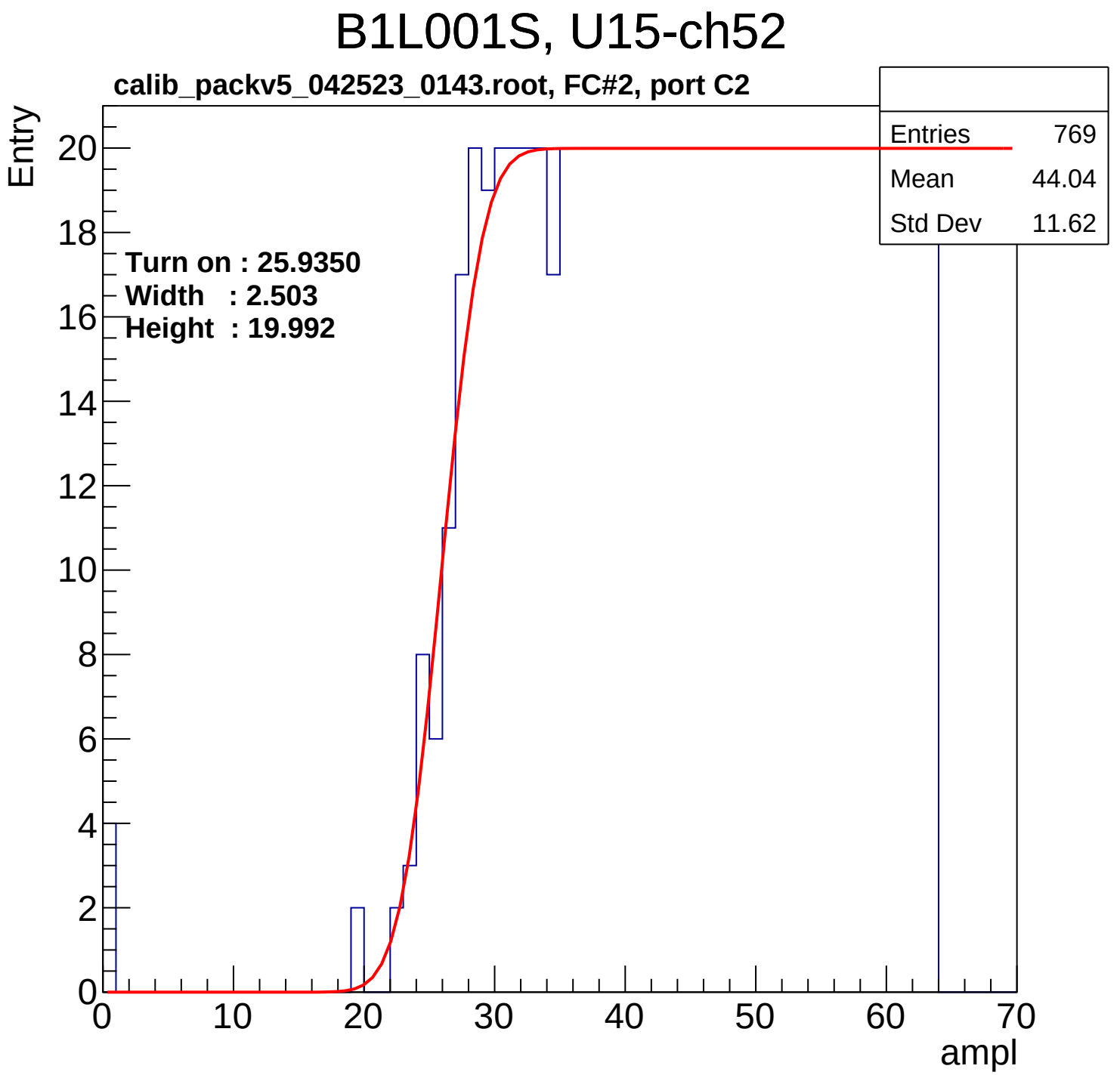
B1L001S, U15-ch52
calib_packv5_042523_0143.root, FC#2, port C2
Entries 769
Mean 44.04
Std Dev 11.62
Turn on : 25.9350
Width : 2.503
Height : 19.992
Entry
ampl
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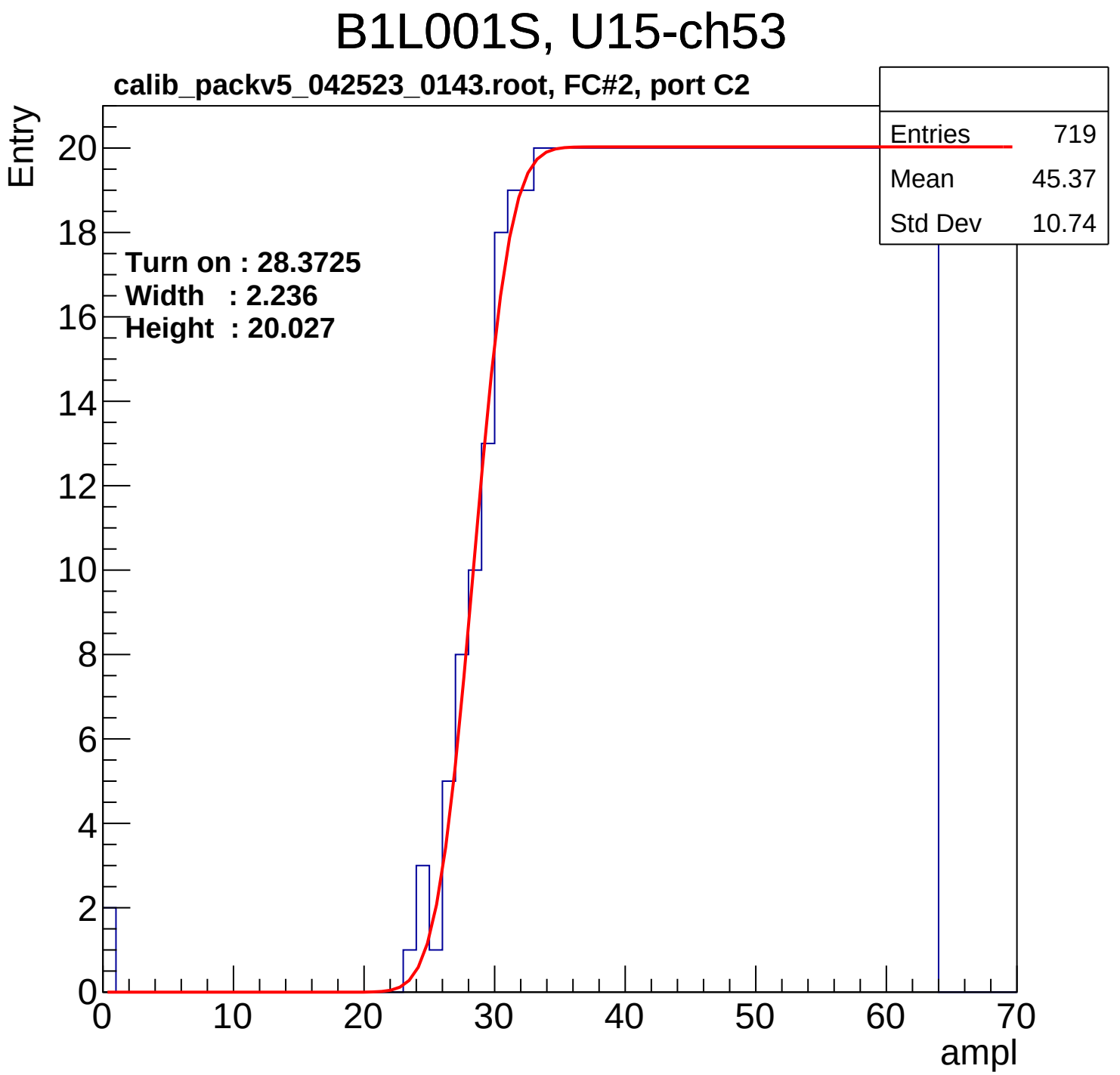
B1L001S, U15-ch53
calib_packv5_042523_0143.root, FC#2, port C2
Entries 719
Mean 45.37
Std Dev 10.74
Turn on : 28.3725
Width : 2.236
Height : 20.027
Entry
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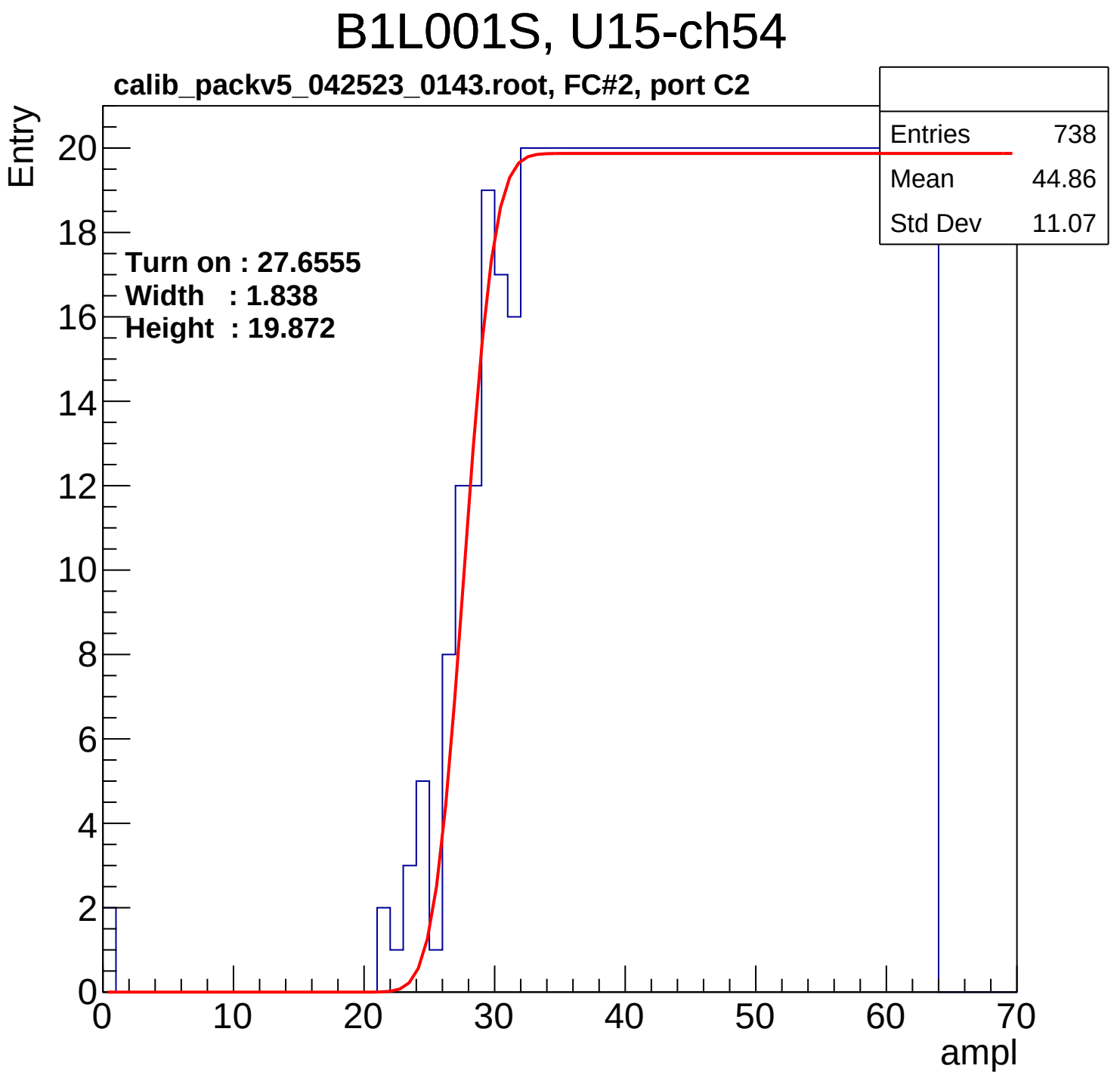
B1L001S, U15-ch54
calib_packv5_042523_0143.root, FC#2, port C2
Entries 738
Mean 44.86
Std Dev 11.07
Turn on : 27.6555
Width : 1.838
Height : 19.872
Entry
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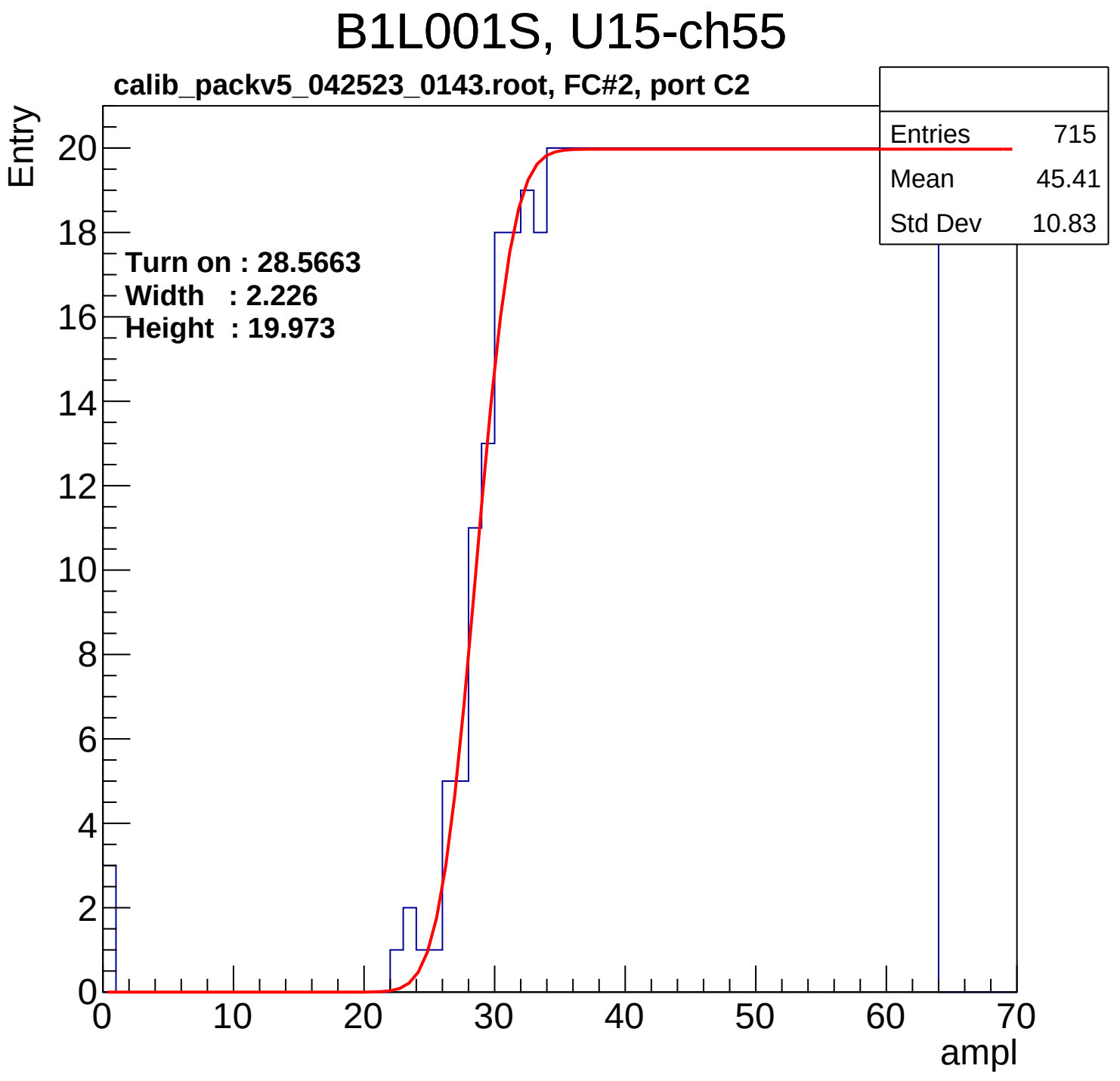
B1L001S, U15-ch55
calib_packv5_042523_0143.root, FC#2, port C2
Entries 715
Mean 45.41
Std Dev 10.83
Turn on : 28.5663
Width : 2.226
Height : 19.973
Entry
ampl
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6
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12
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18
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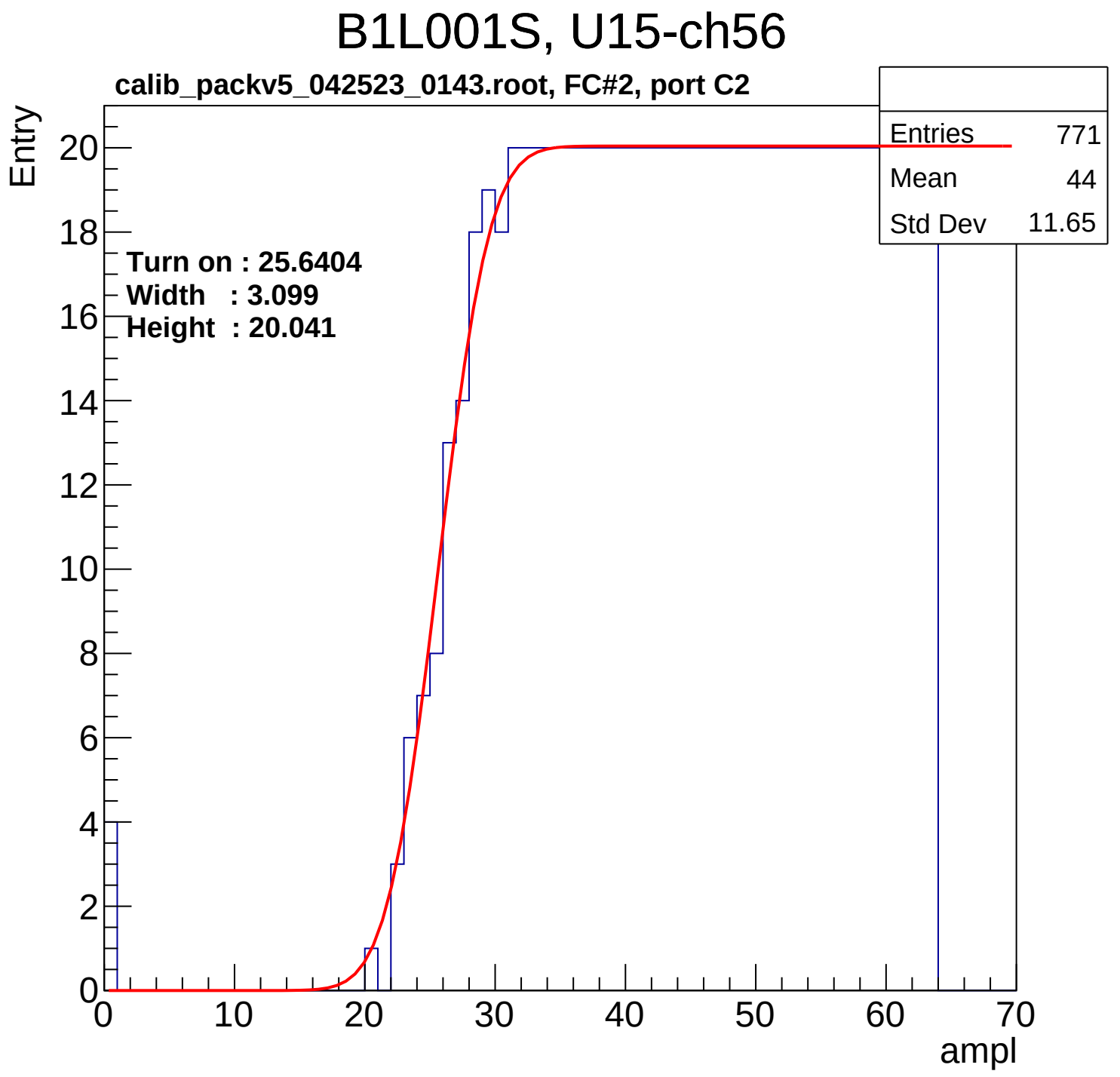
B1L001S, U15-ch56
calib_packv5_042523_0143.root, FC#2, port C2
Entries 771
Mean 44
Std Dev 11.65
Turn on : 25.6404
Width : 3.099
Height : 20.041
Entry
ampl
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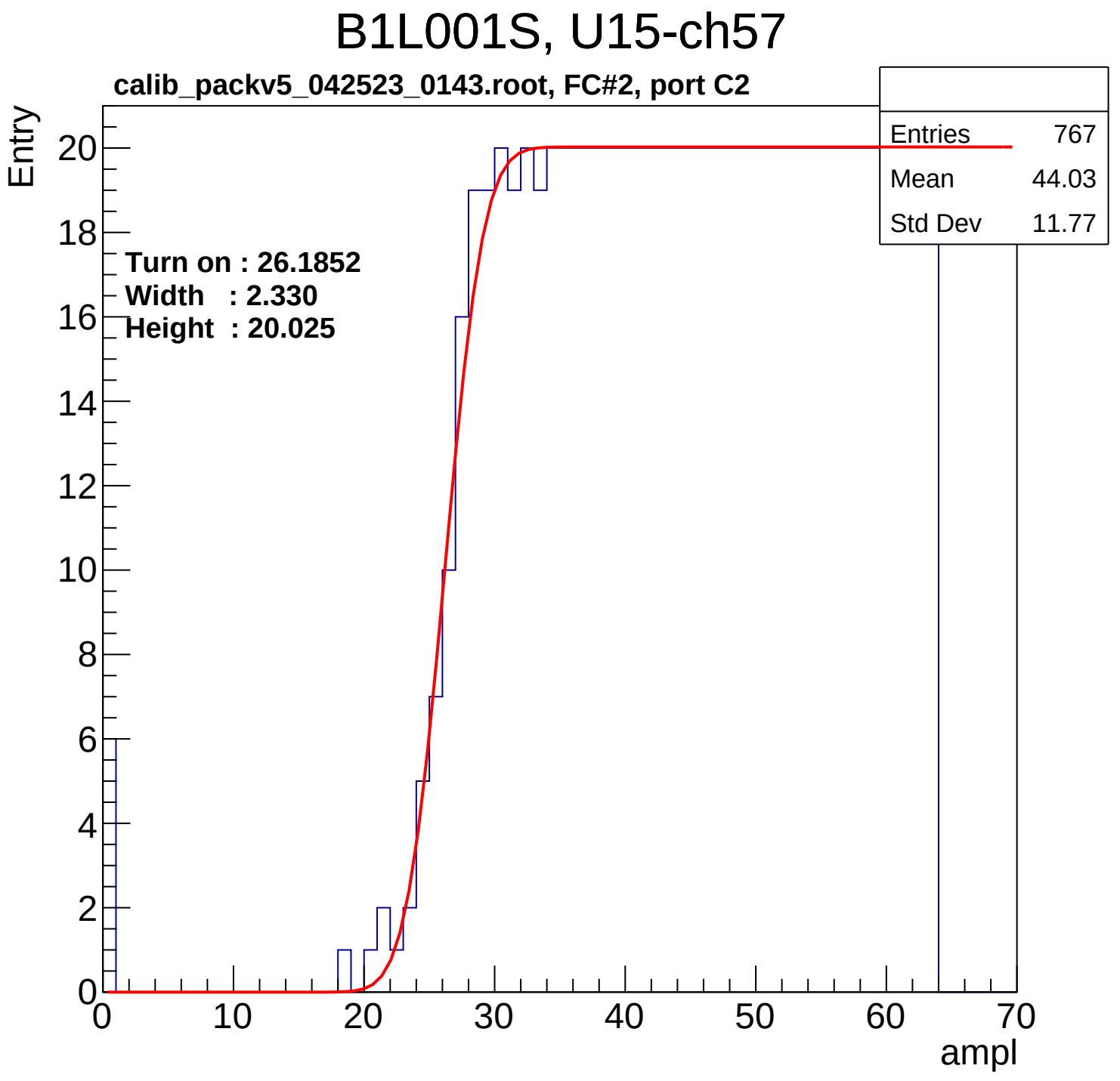
B1L001S, U15-ch57
calib_packv5_042523_0143.root, FC#2, port C2
Entries 767
Mean 44.03
Std Dev 11.77
Turn on : 26.1852
Width : 2.330
Height : 20.025
Entry
ampl
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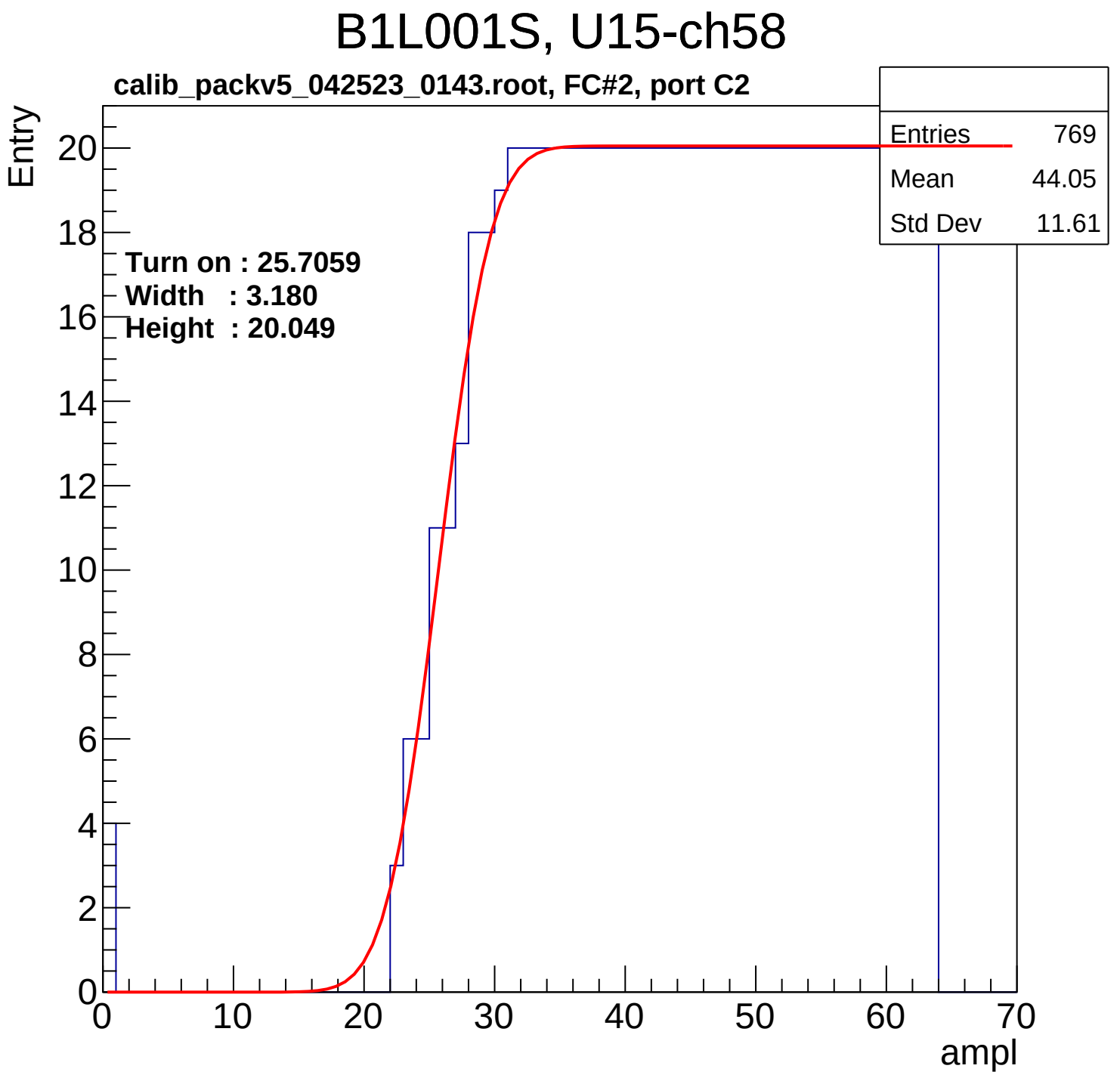
B1L001S, U15-ch58
calib_packv5_042523_0143.root, FC#2, port C2
Entries 769
Mean 44.05
Std Dev 11.61
Turn on : 25.7059
Width : 3.180
Height : 20.049
Entry
ampl
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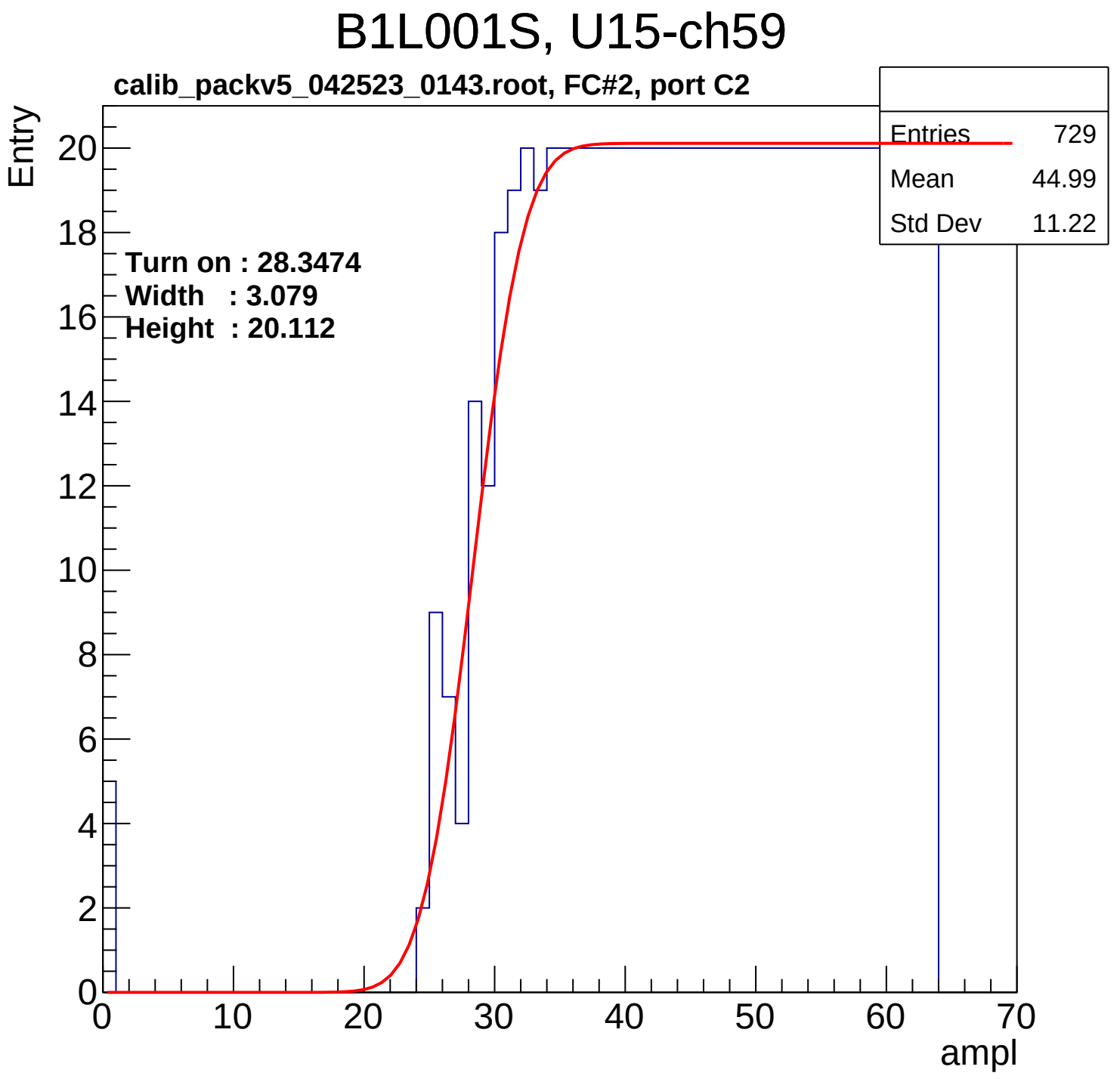
B1L001S, U15-ch59
calib_packv5_042523_0143.root, FC#2, port C2
Entries 729
Mean 44.99
Std Dev 11.22
Turn on : 28.3474
Width : 3.079
Height : 20.112
Entry
ampl
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6
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14
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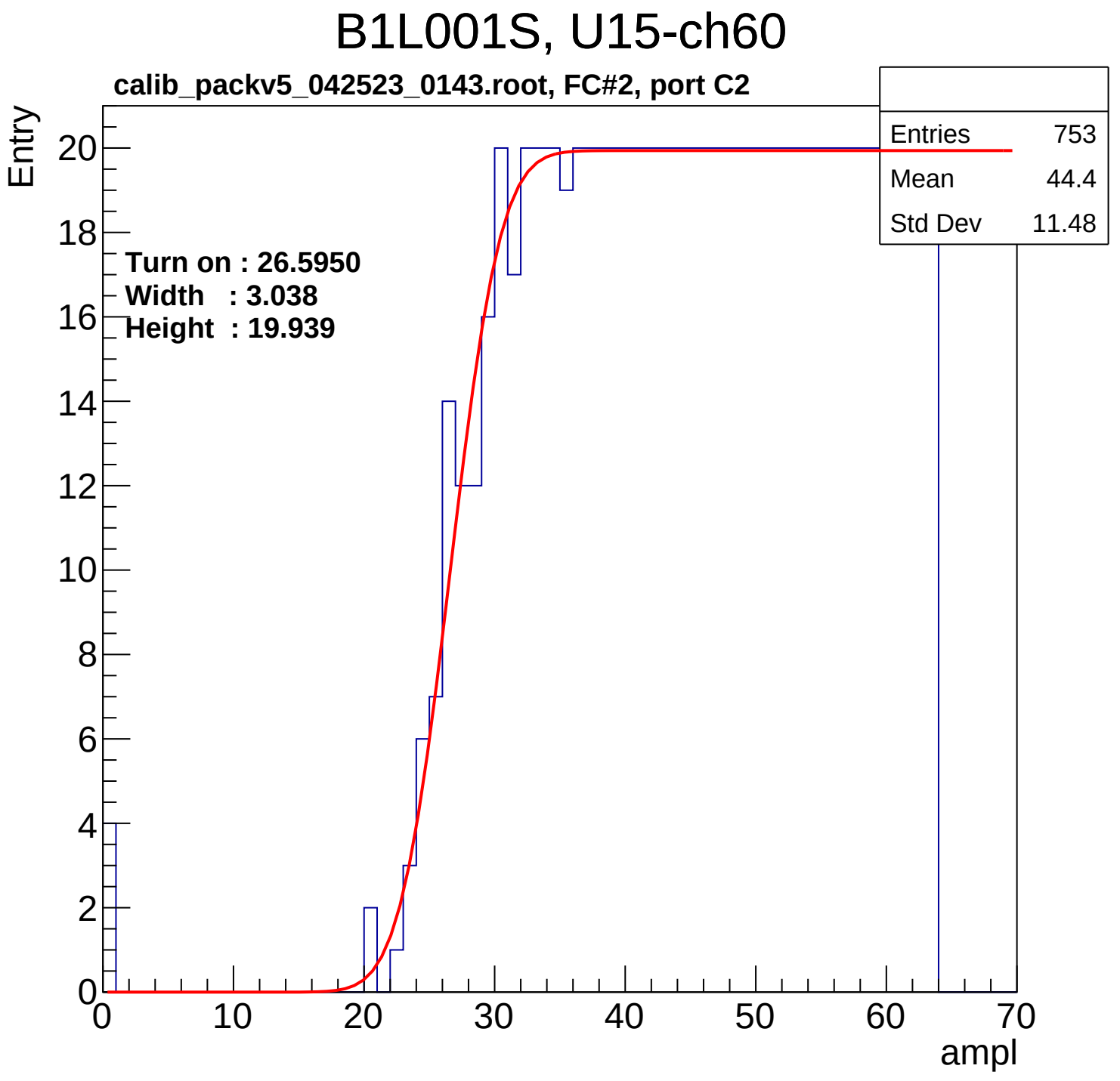
B1L001S, U15-ch60
calib_packv5_042523_0143.root, FC#2, port C2
Entries 753
Mean 44.4
Std Dev 11.48
Turn on : 26.5950
Width : 3.038
Height : 19.939
Entry
ampl
0
2
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6
8
10
12
14
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0
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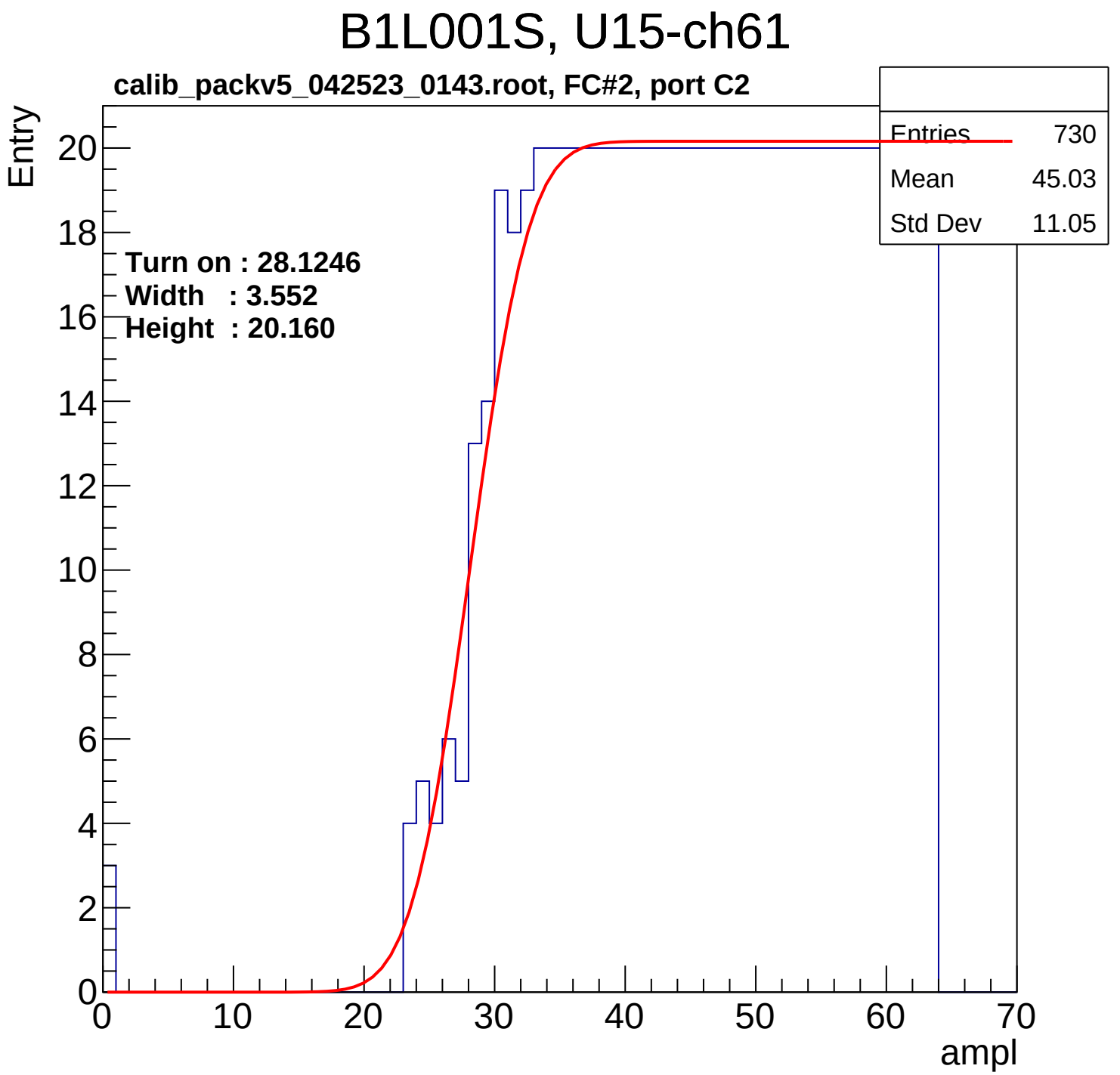
B1L001S, U15-ch61
calib_packv5_042523_0143.root, FC#2, port C2
Entry
Entries 730
Mean 45.03
Std Dev 11.05
Turn on : 28.1246
Width : 3.552
Height : 20.160
0
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10
12
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16
18
20
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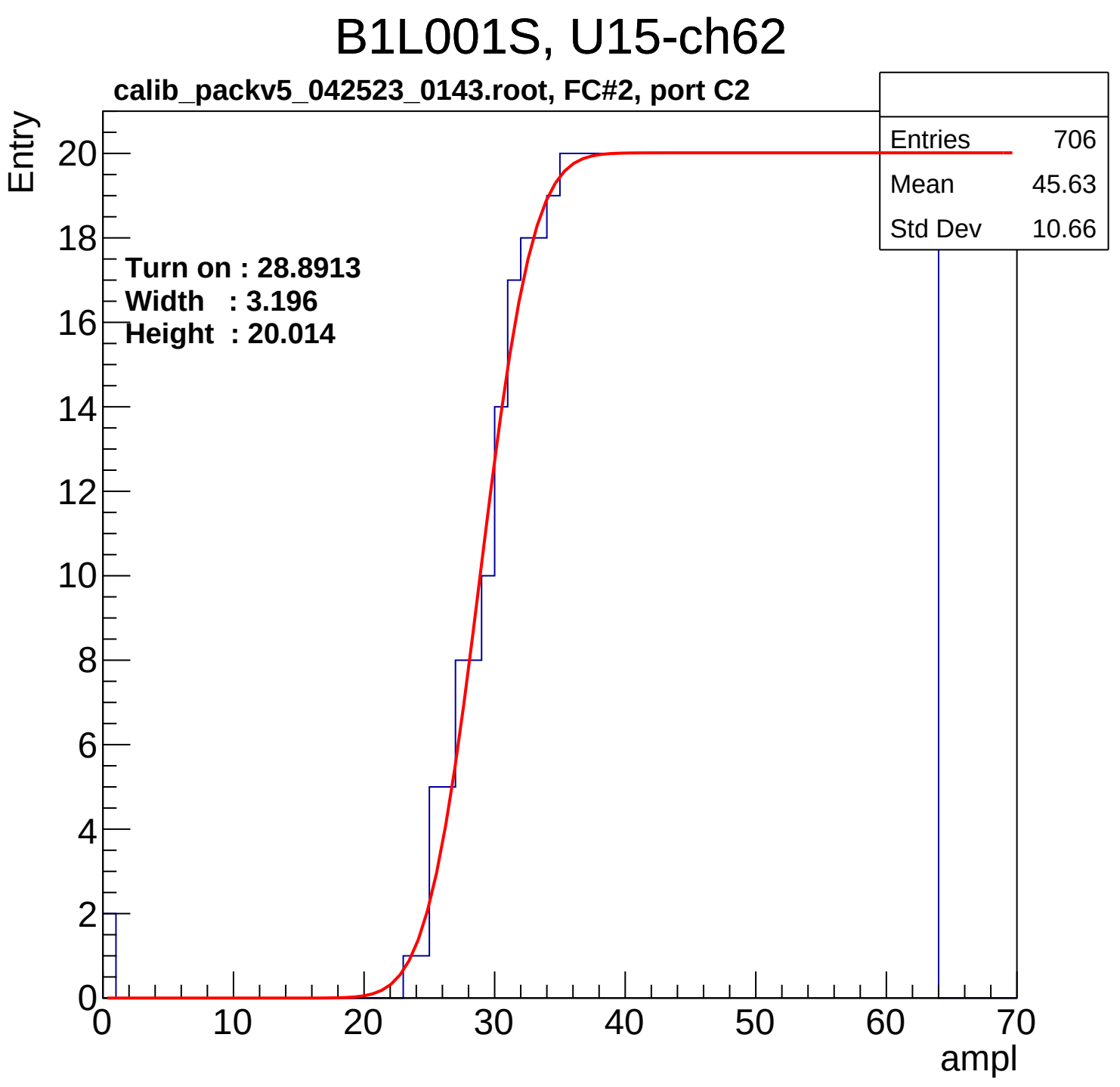
70
ampl


B1L001S, U15-ch62
calib_packv5_042523_0143.root, FC#2, port C2
Entries 706
Mean 45.63
Std Dev 10.66
Turn on : 28.8913
Width : 3.196
Height : 20.014
Entry
ampl
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8
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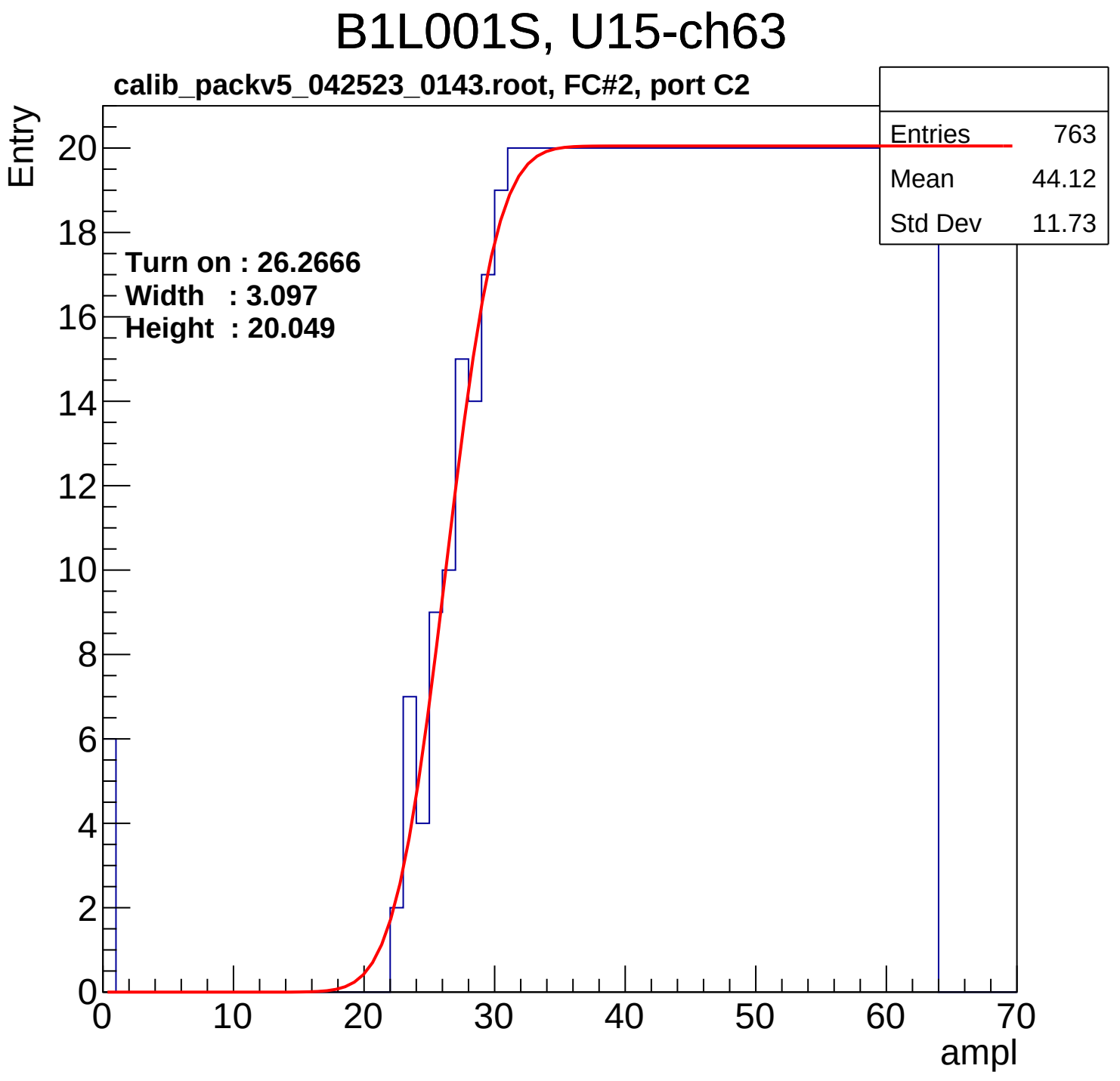
B1L001S, U15-ch63
calib_packv5_042523_0143.root, FC#2, port C2
Entries 763
Mean 44.12
Std Dev 11.73
Turn on : 26.2666
Width : 3.097
Height : 20.049
Entry
ampl
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2
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6
8
10
12
14
16
18
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0
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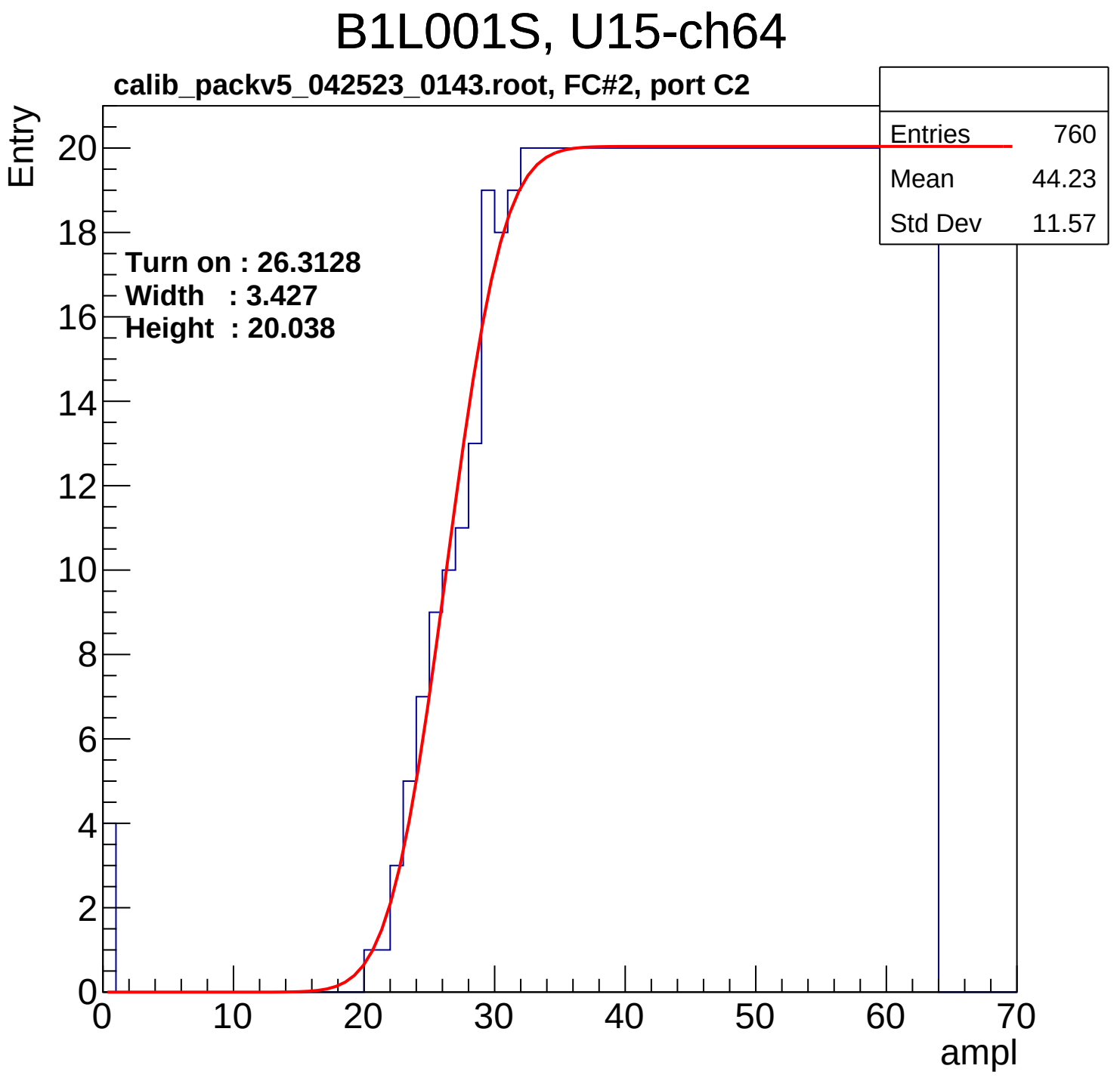
B1L001S, U15-ch64
calib_packv5_042523_0143.root, FC#2, port C2
Entries 760
Mean 44.23
Std Dev 11.57
Turn on : 26.3128
Width : 3.427
Height : 20.038
Entry
ampl
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6
8
10
12
14
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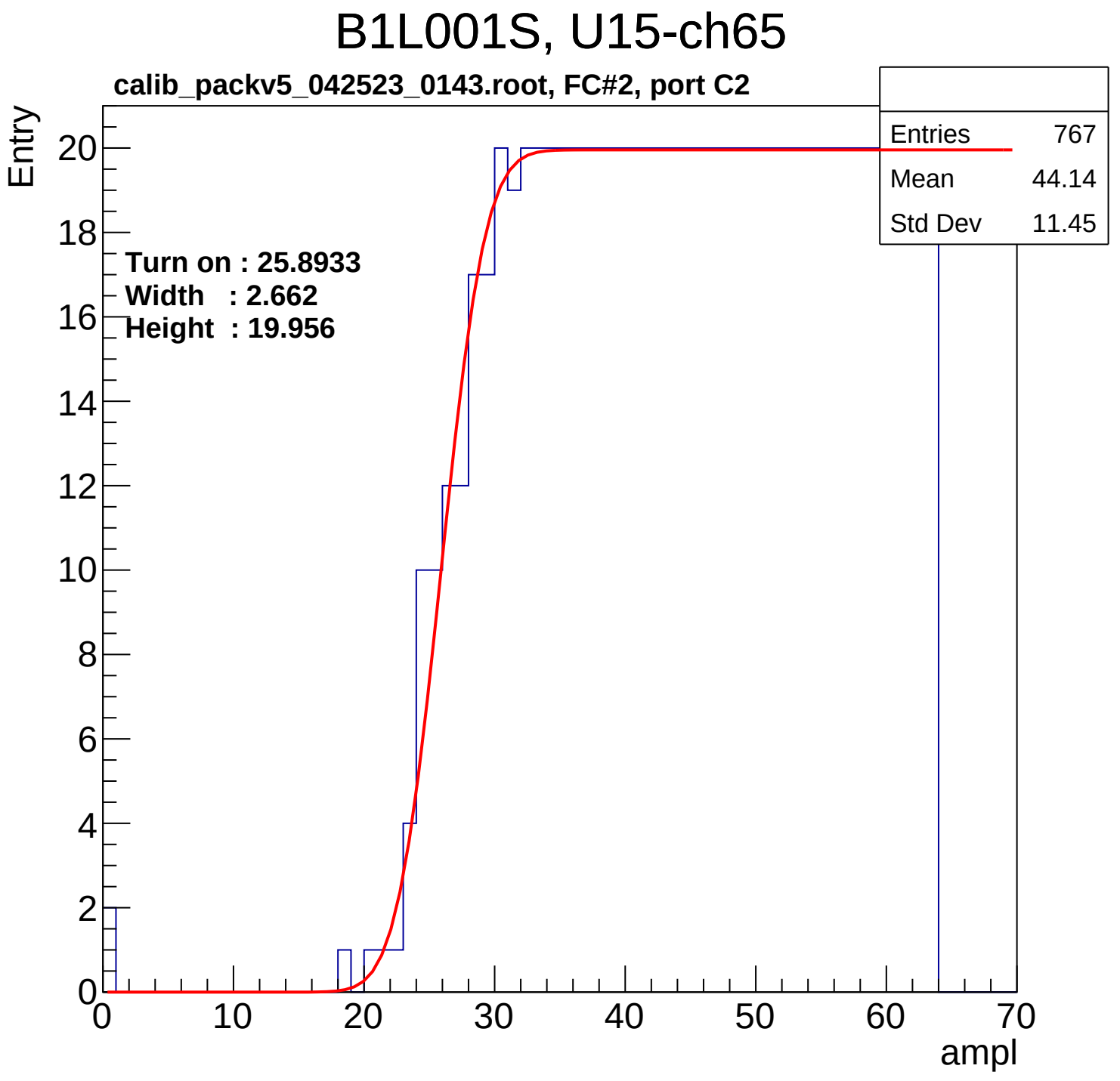
B1L001S, U15-ch65
calib_packv5_042523_0143.root, FC#2, port C2
Entries 767
Mean 44.14
Std Dev 11.45
Turn on : 25.8933
Width : 2.662
Height : 19.956
Entry
ampl
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6
8
10
12
14
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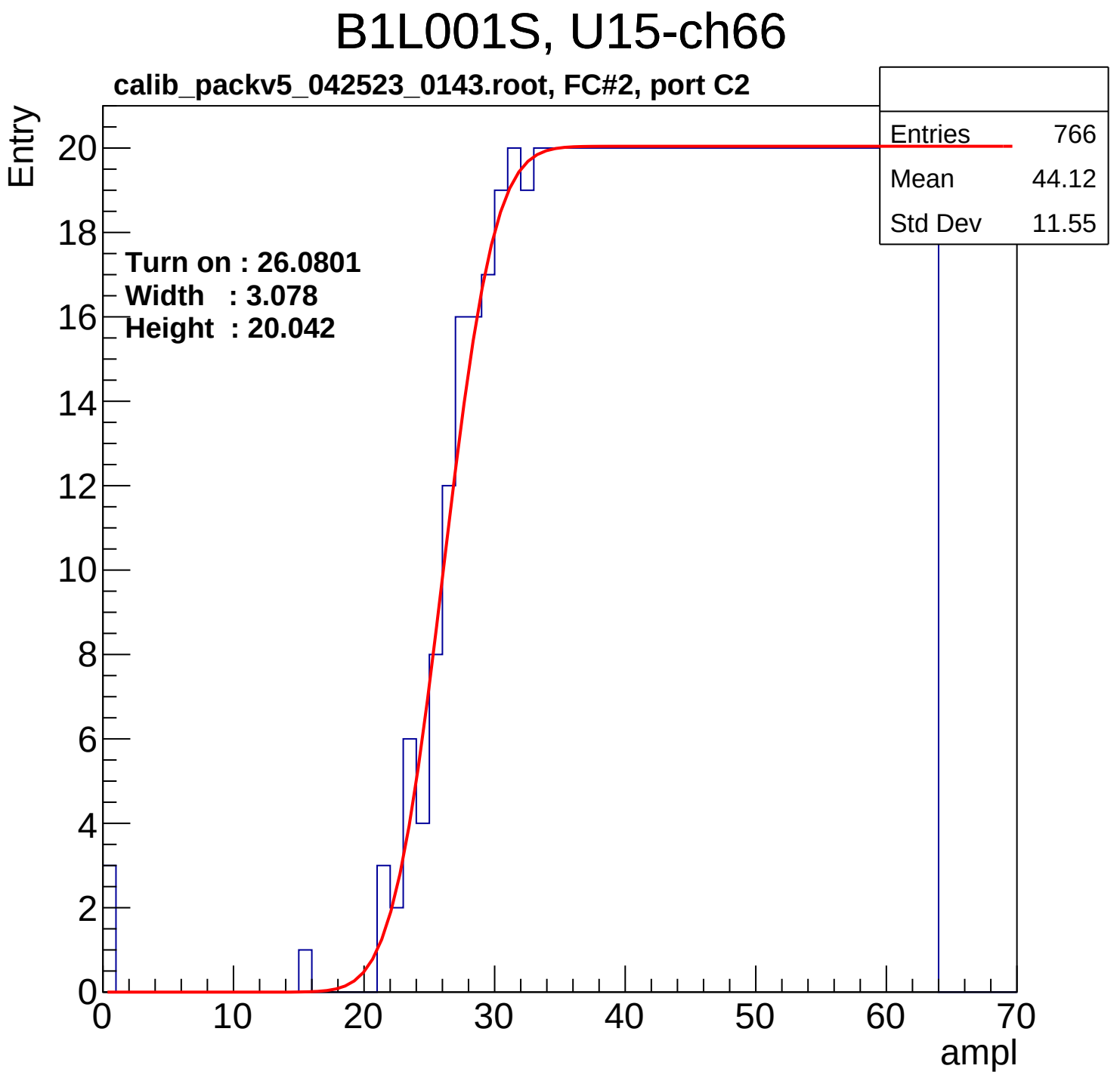
B1L001S, U15-ch66
calib_packv5_042523_0143.root, FC#2, port C2
Entries 766
Mean 44.12
Std Dev 11.55
Turn on : 26.0801
Width : 3.078
Height : 20.042
Entry
ampl
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6
8
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12
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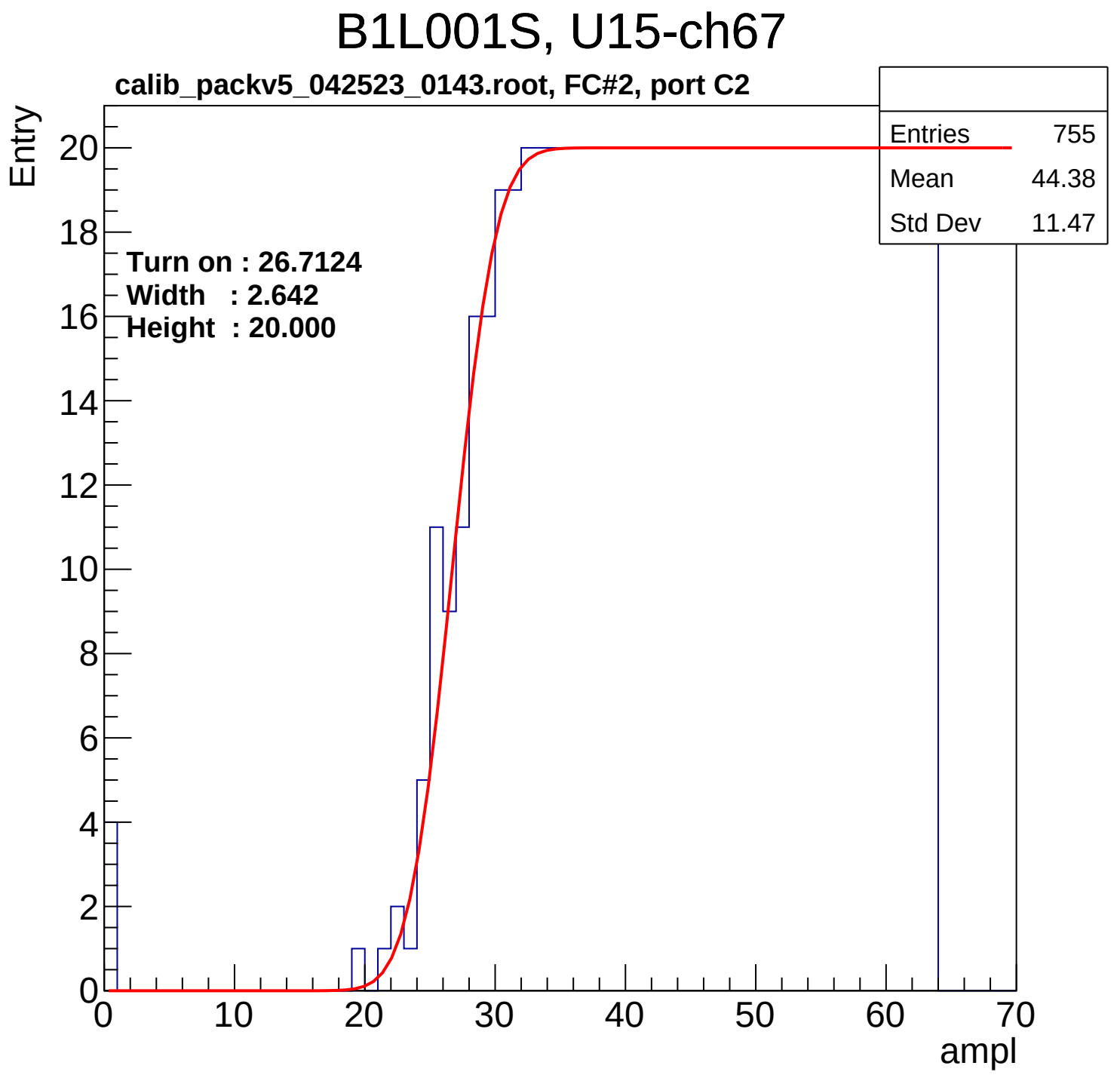
B1L001S, U15-ch67
calib_packv5_042523_0143.root, FC#2, port C2
Entries 755
Mean 44.38
Std Dev 11.47
Turn on : 26.7124
Width : 2.642
Height : 20.000
Entry
ampl
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6
8
10
12
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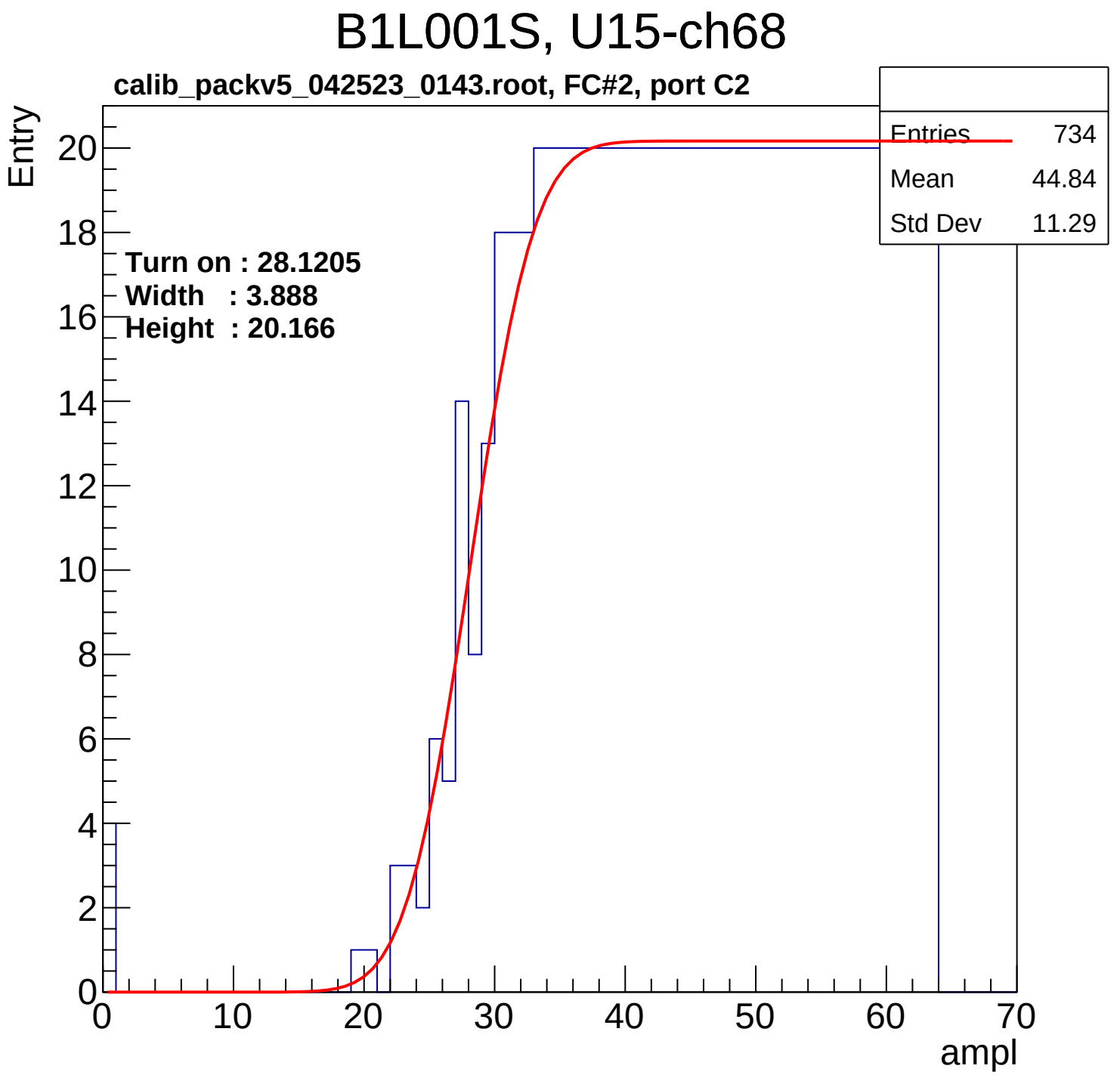
B1L001S, U15-ch68
calib_packv5_042523_0143.root, FC#2, port C2
Entries 734
Mean 44.84
Std Dev 11.29
Turn on : 28.1205
Width : 3.888
Height : 20.166
Entry
ampl
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6
8
10
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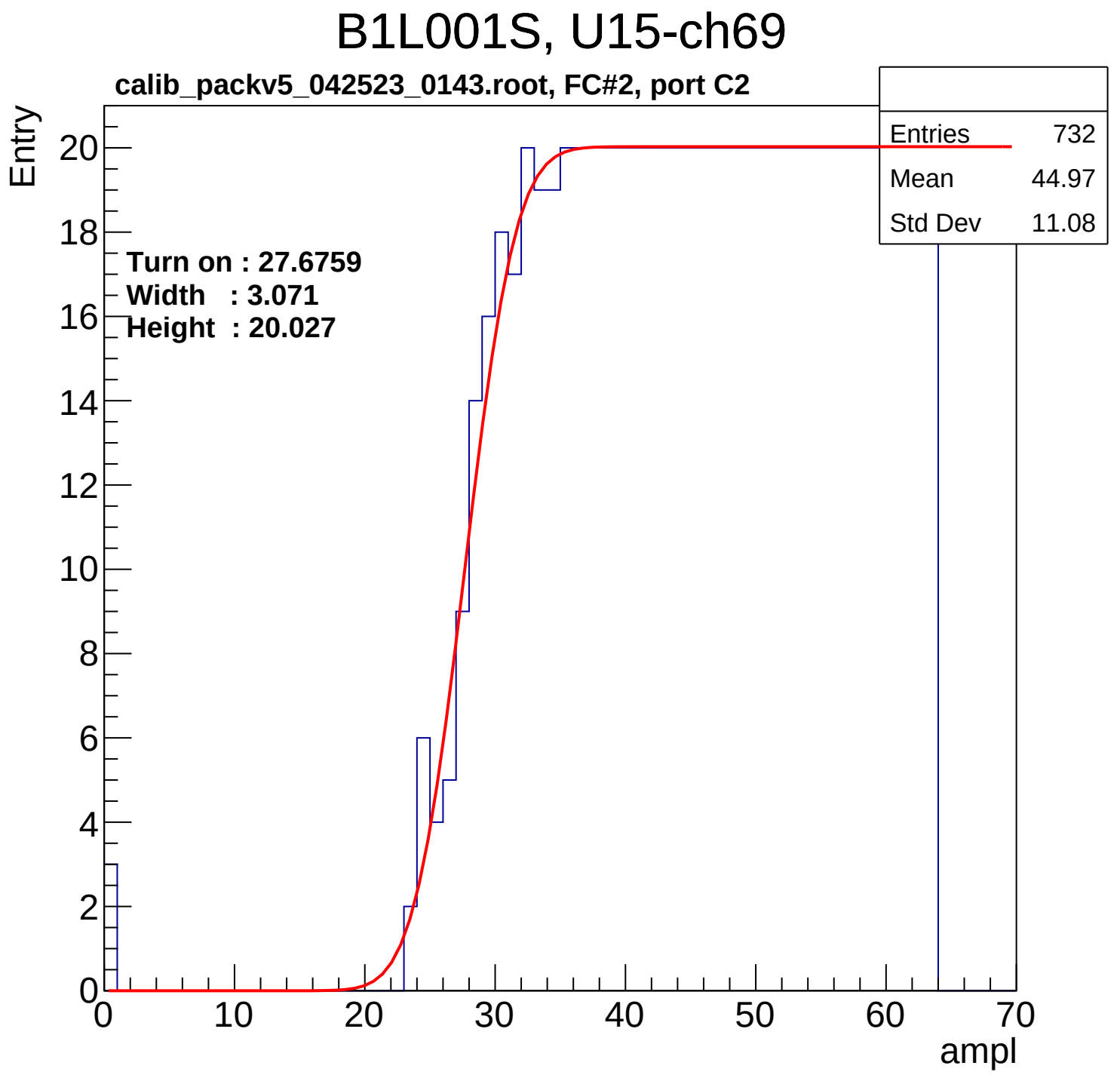
B1L001S, U15-ch69
calib_packv5_042523_0143.root, FC#2, port C2
Entries 732
Mean 44.97
Std Dev 11.08
Turn on : 27.6759
Width : 3.071
Height : 20.027
Entry
ampl
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6
8
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12
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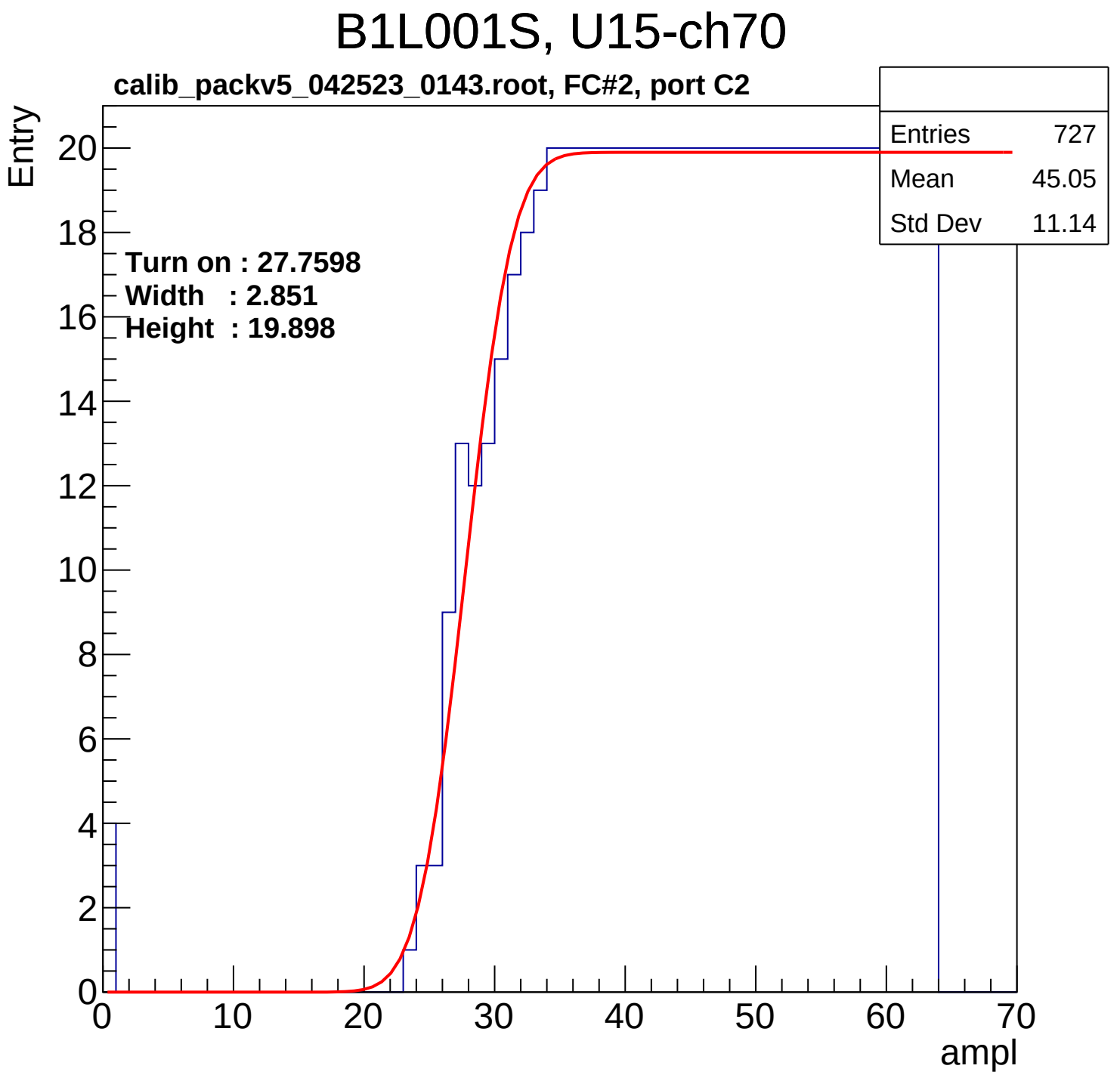
B1L001S, U15-ch70
calib_packv5_042523_0143.root, FC#2, port C2
Entries 727
Mean 45.05
Std Dev 11.14
Turn on : 27.7598
Width : 2.851
Height : 19.898
Entry
ampl
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6
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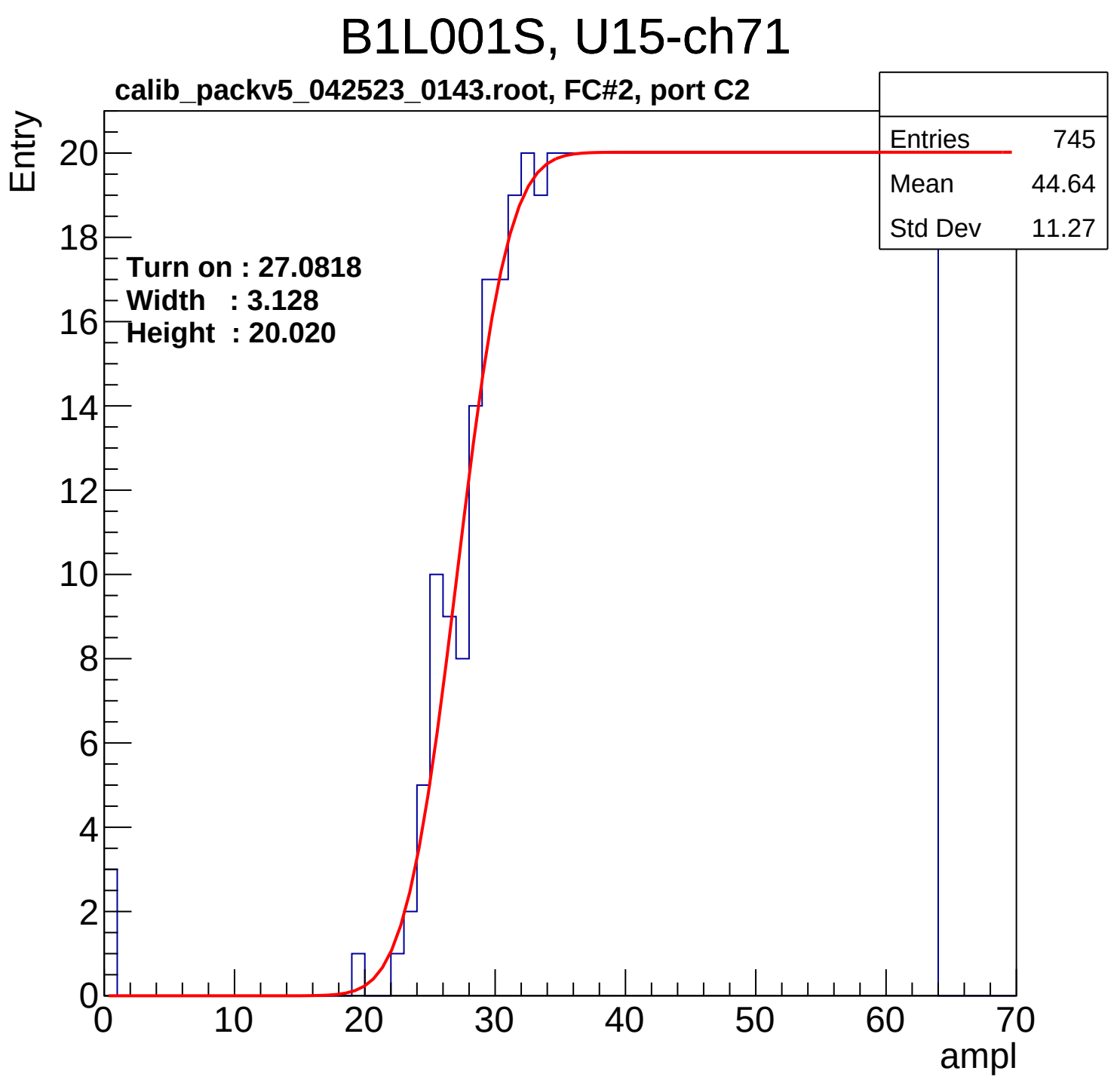
B1L001S, U15-ch71
calib_packv5_042523_0143.root, FC#2, port C2
Entries 745
Mean 44.64
Std Dev 11.27
Turn on : 27.0818
Width : 3.128
Height : 20.020
Entry
ampl
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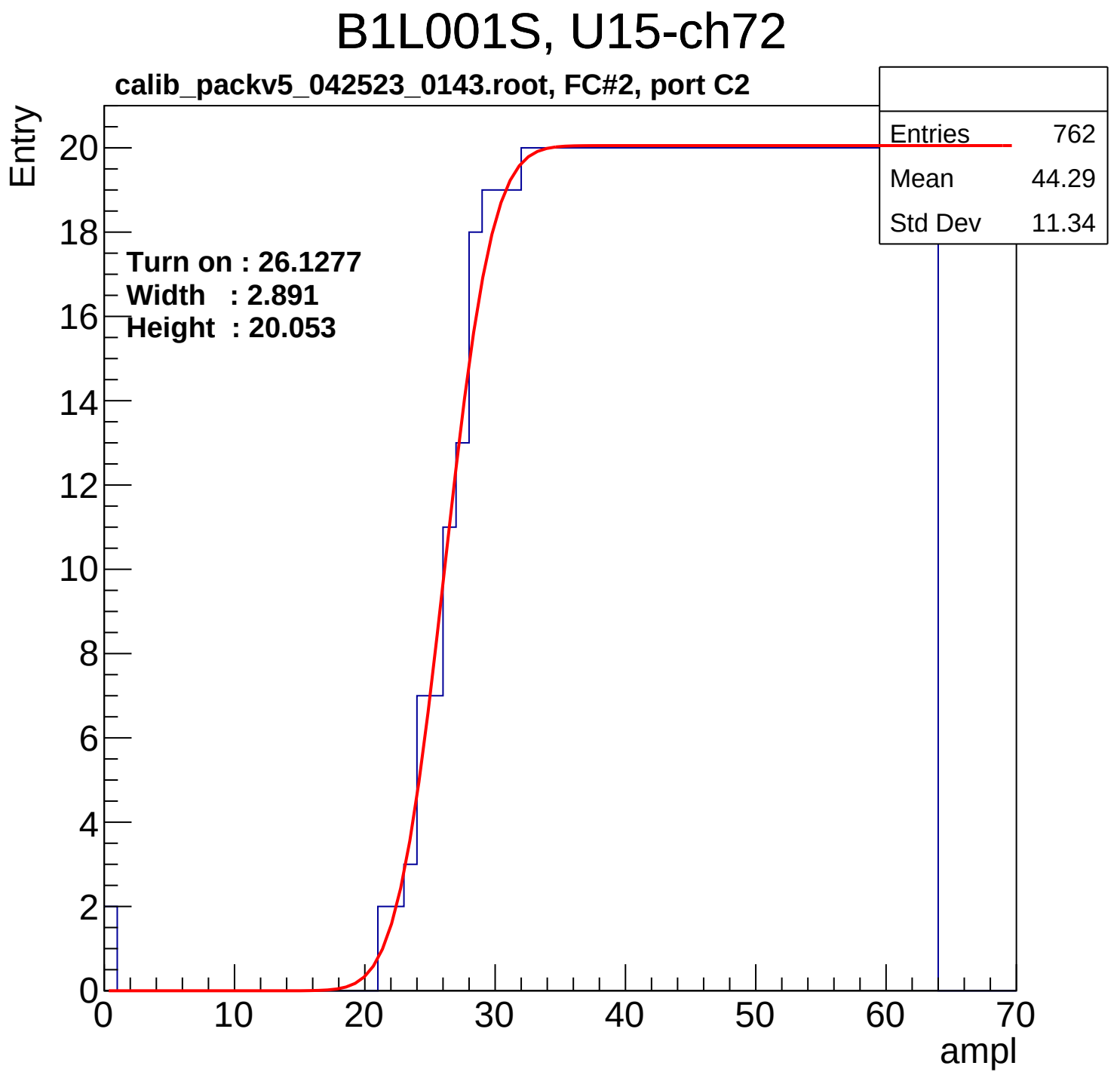
B1L001S, U15-ch72
calib_packv5_042523_0143.root, FC#2, port C2
Entries 762
Mean 44.29
Std Dev 11.34
Turn on : 26.1277
Width : 2.891
Height : 20.053
Entry
ampl
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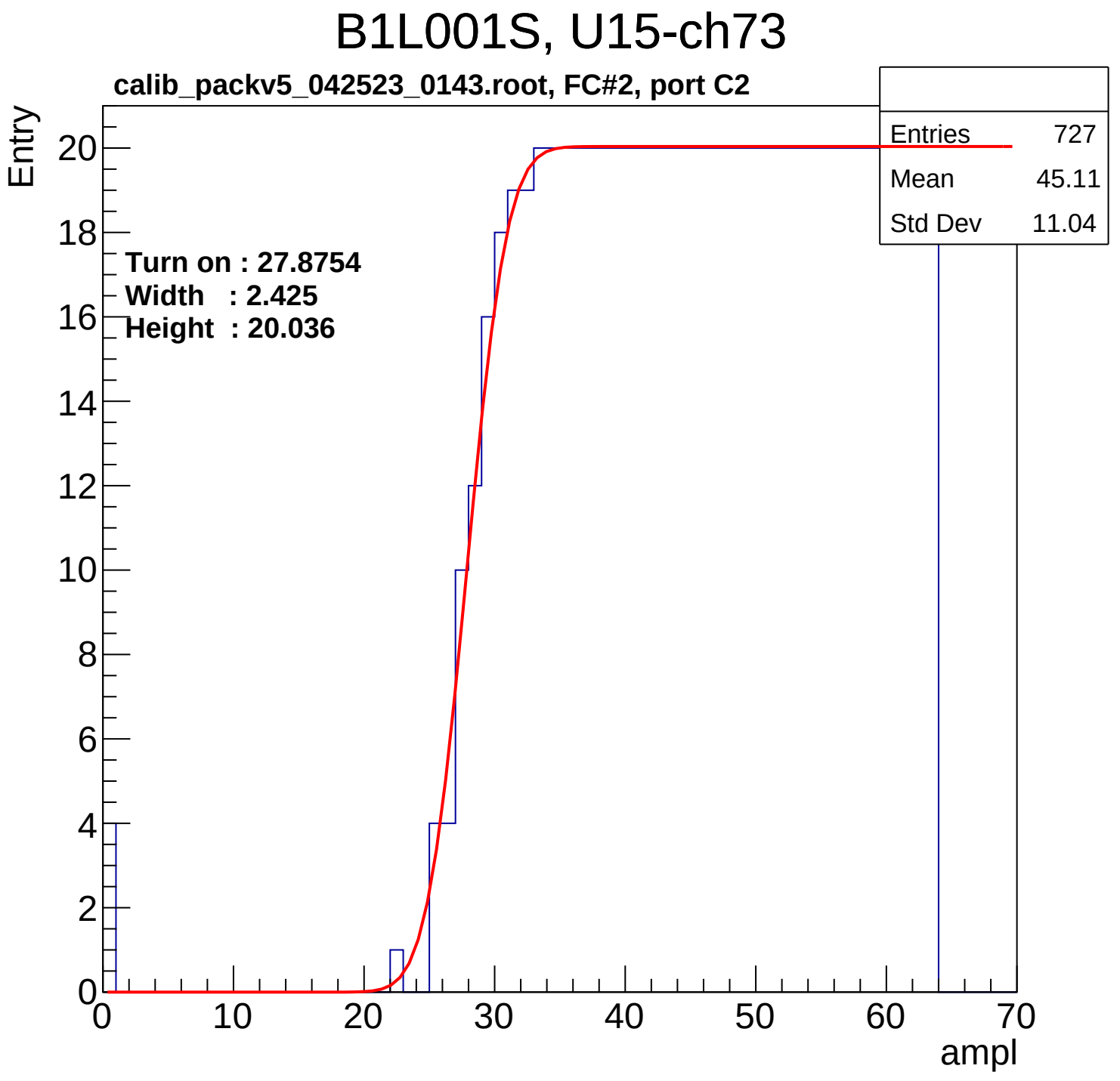
B1L001S, U15-ch73
calib_packv5_042523_0143.root, FC#2, port C2
Entries 727
Mean 45.11
Std Dev 11.04
Turn on : 27.8754
Width : 2.425
Height : 20.036
Entry
ampl
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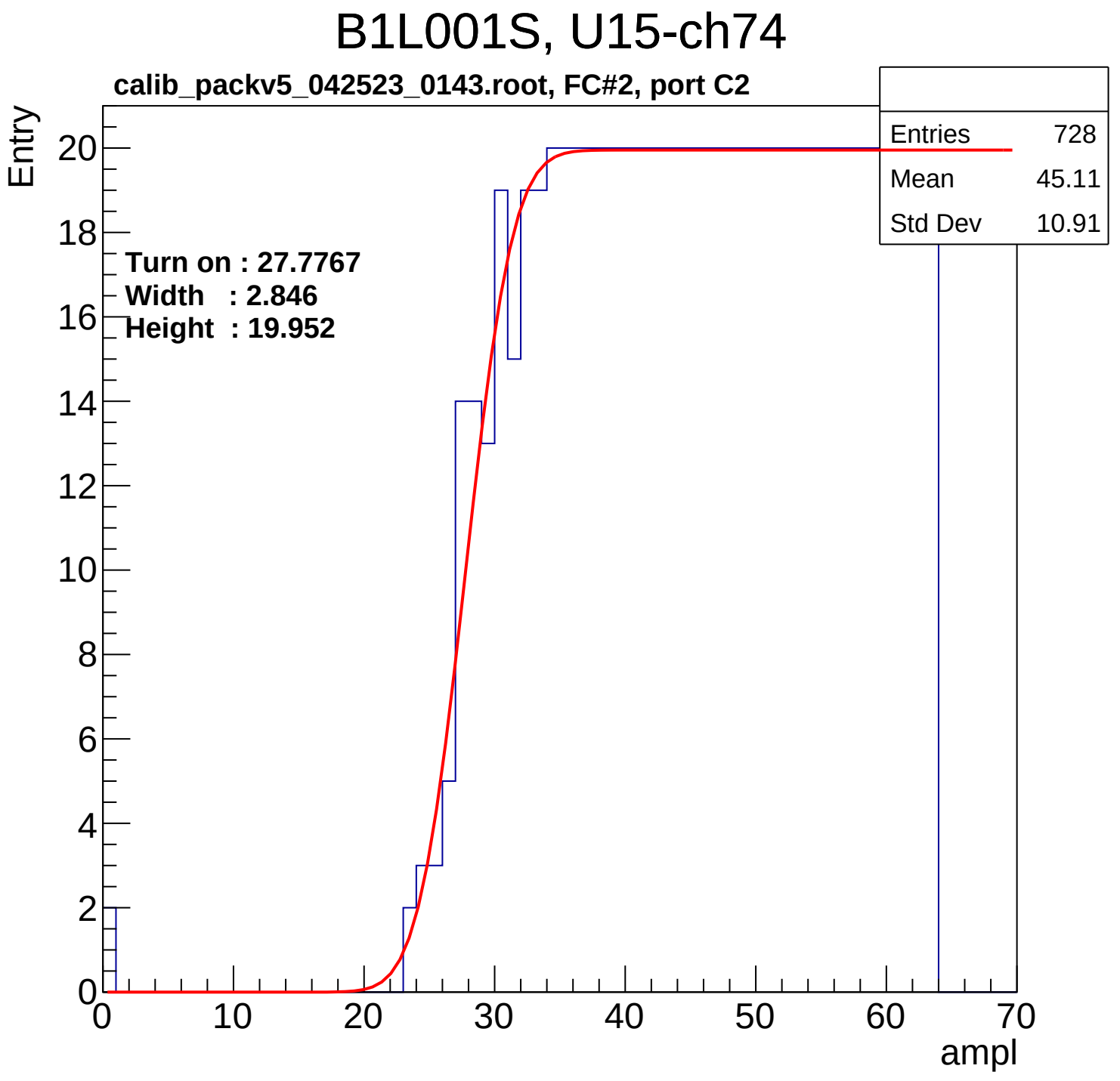
B1L001S, U15-ch74
calib_packv5_042523_0143.root, FC#2, port C2
Entries 728
Mean 45.11
Std Dev 10.91
Turn on : 27.7767
Width : 2.846
Height : 19.952
Entry
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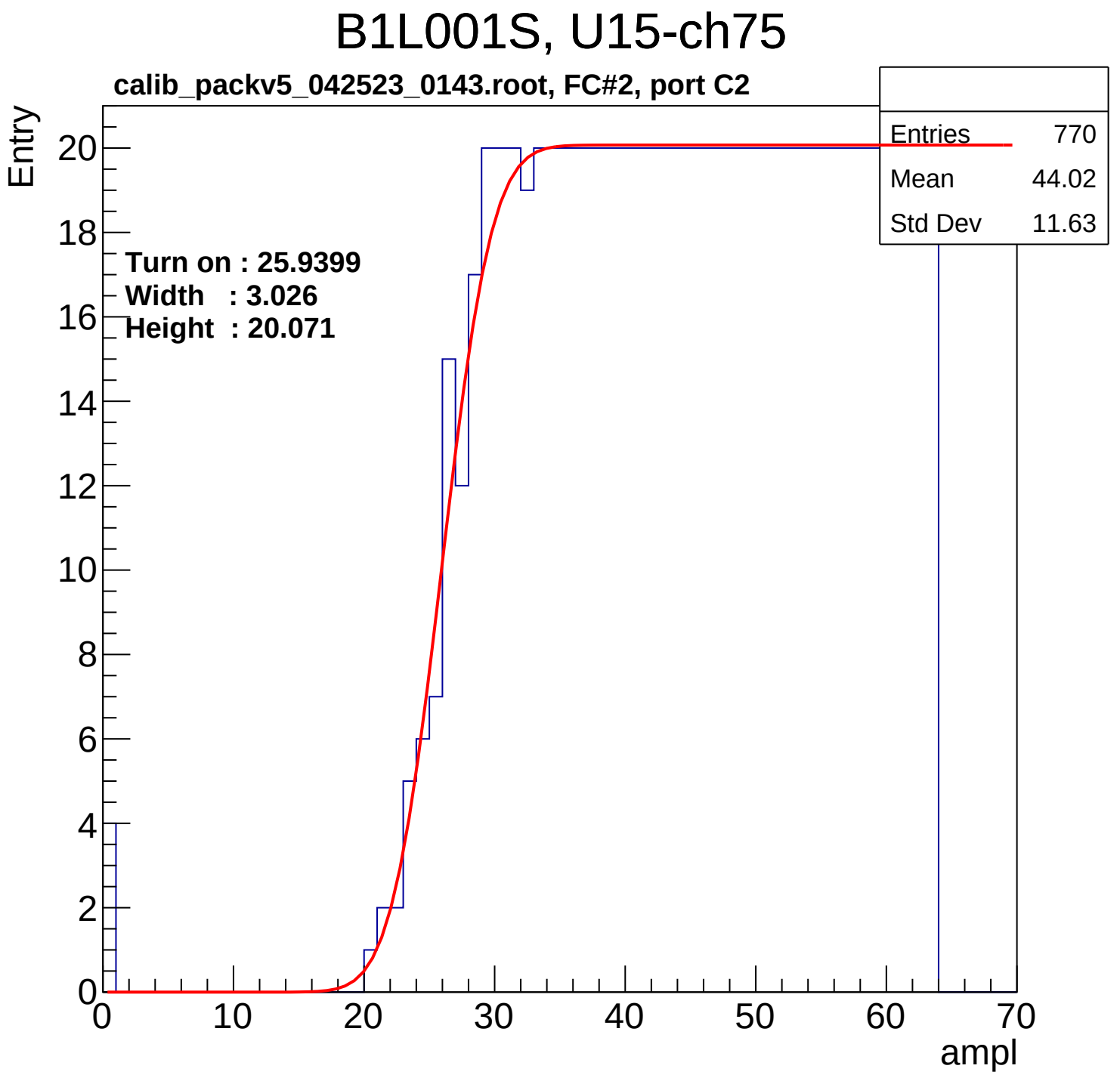
B1L001S, U15-ch75
calib_packv5_042523_0143.root, FC#2, port C2
Entries 770
Mean 44.02
Std Dev 11.63
Turn on : 25.9399
Width : 3.026
Height : 20.071
Entry
ampl
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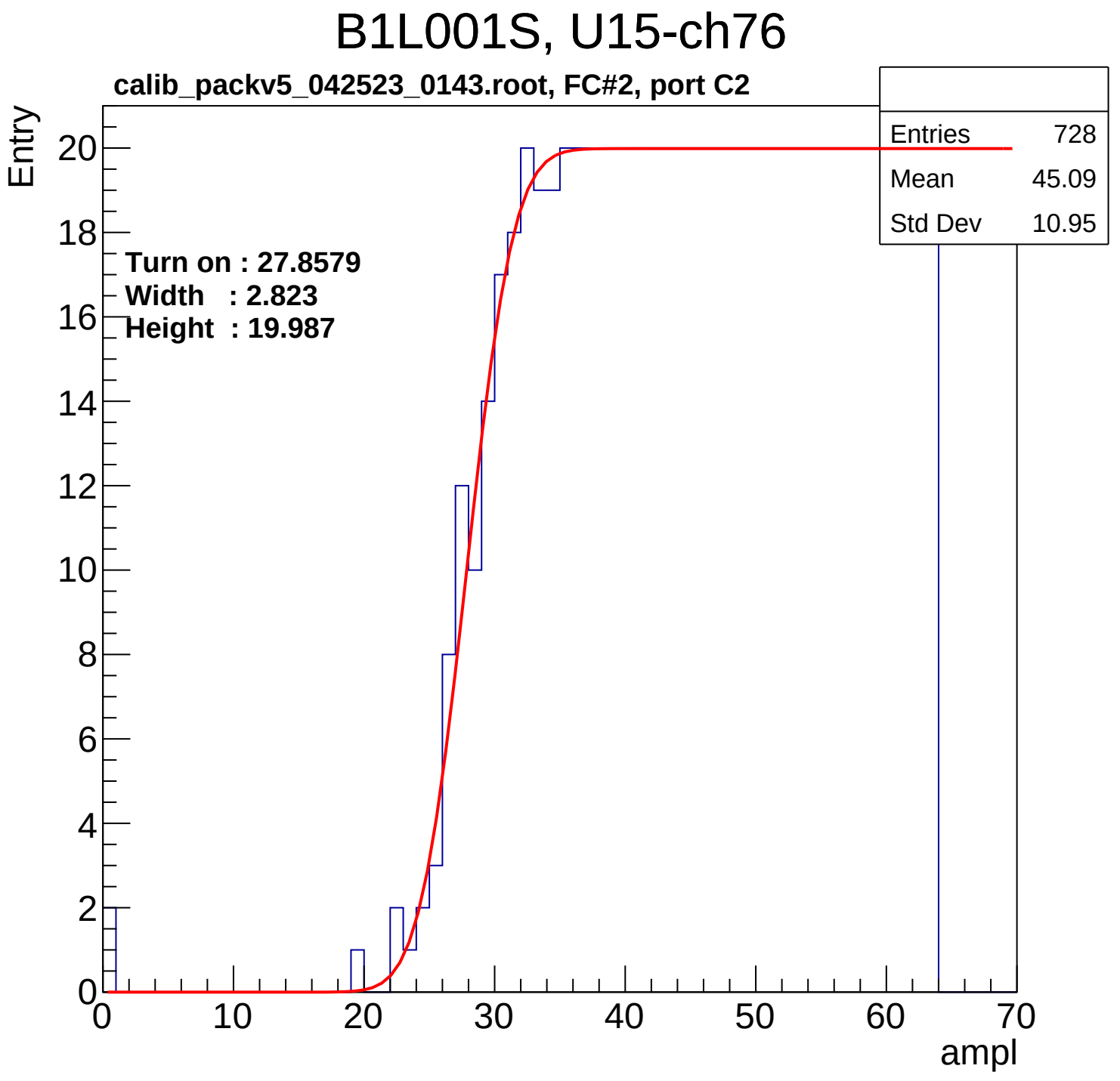
B1L001S, U15-ch76
calib_packv5_042523_0143.root, FC#2, port C2
Entries 728
Mean 45.09
Std Dev 10.95
Turn on : 27.8579
Width : 2.823
Height : 19.987
Entry
ampl
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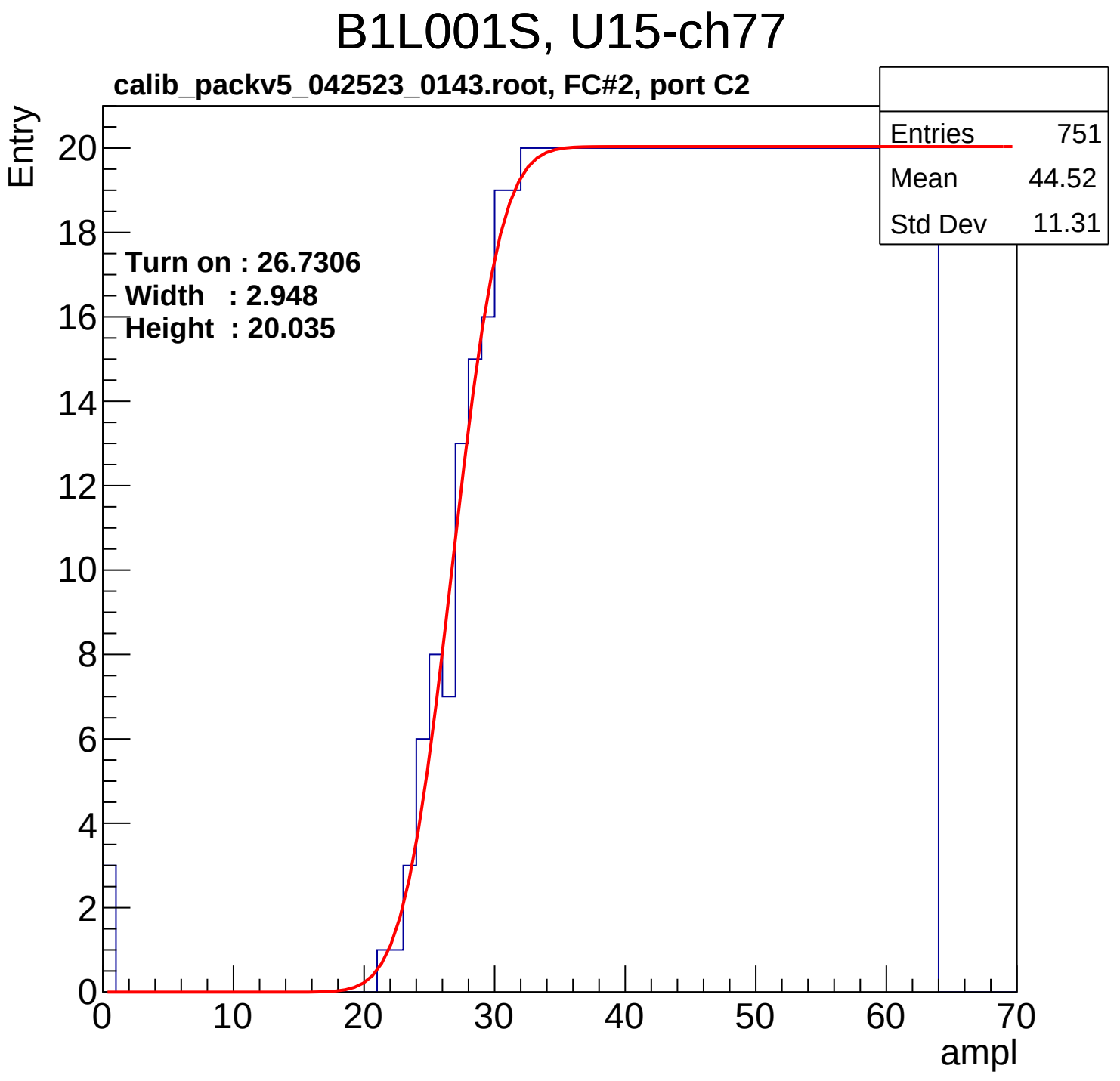
B1L001S, U15-ch77
calib_packv5_042523_0143.root, FC#2, port C2
Entries 751
Mean 44.52
Std Dev 11.31
Turn on : 26.7306
Width : 2.948
Height : 20.035
Entry
ampl
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6
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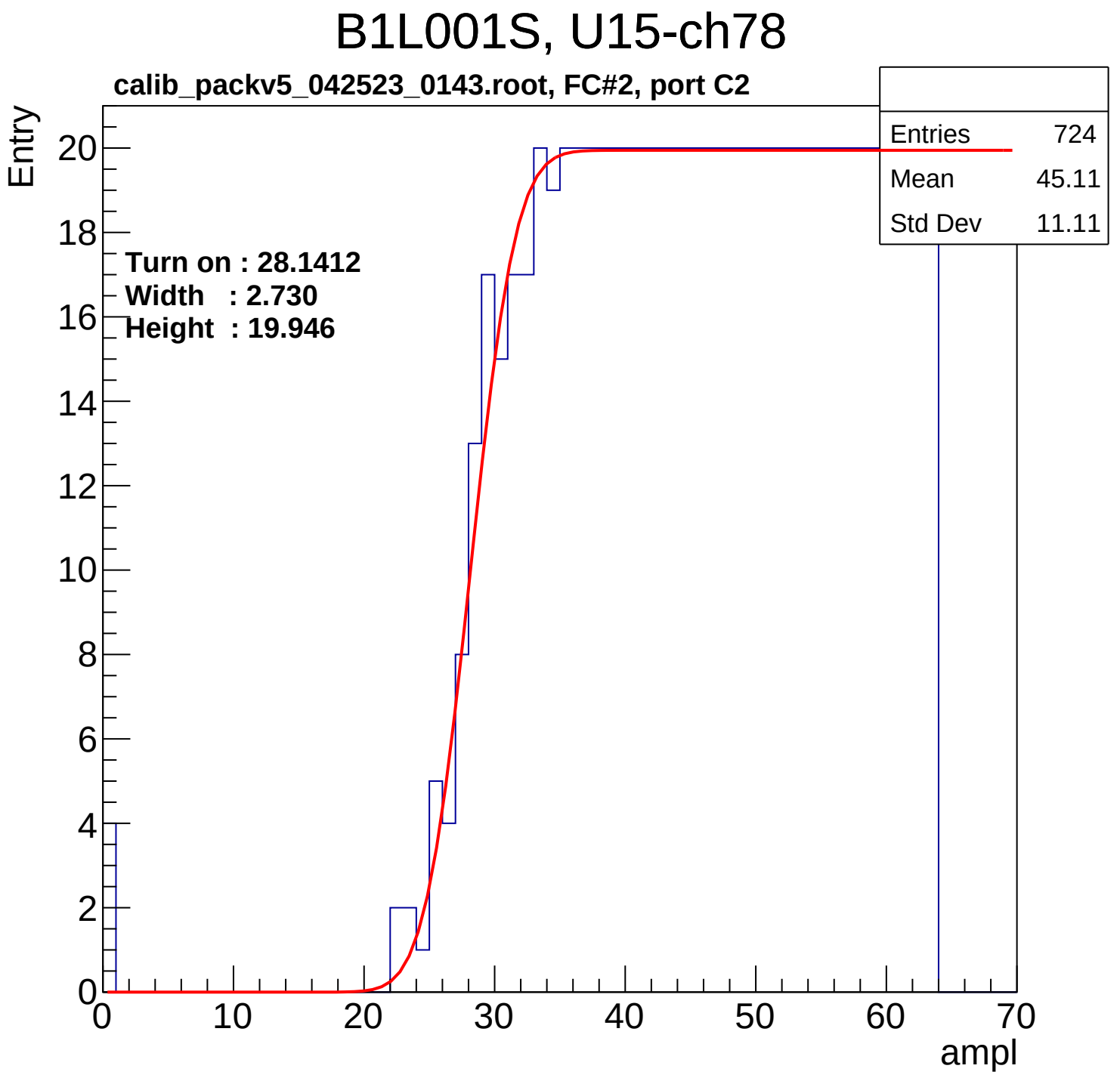
B1L001S, U15-ch78
calib_packv5_042523_0143.root, FC#2, port C2
Entries 724
Mean 45.11
Std Dev 11.11
Turn on : 28.1412
Width : 2.730
Height : 19.946
Entry
ampl
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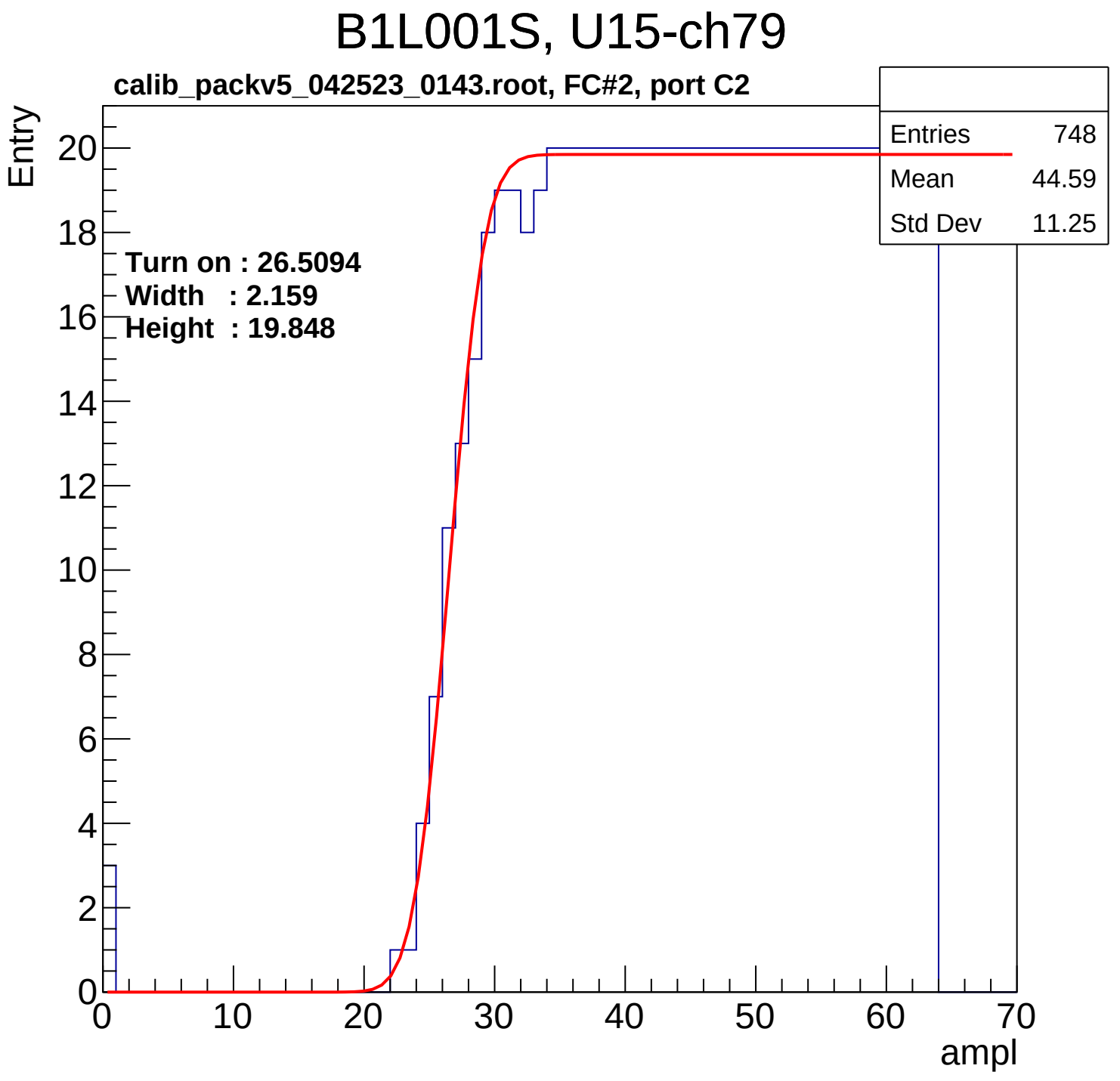
B1L001S, U15-ch79
calib_packv5_042523_0143.root, FC#2, port C2
Entries 748
Mean 44.59
Std Dev 11.25
Turn on : 26.5094
Width : 2.159
Height : 19.848
Entry
ampl
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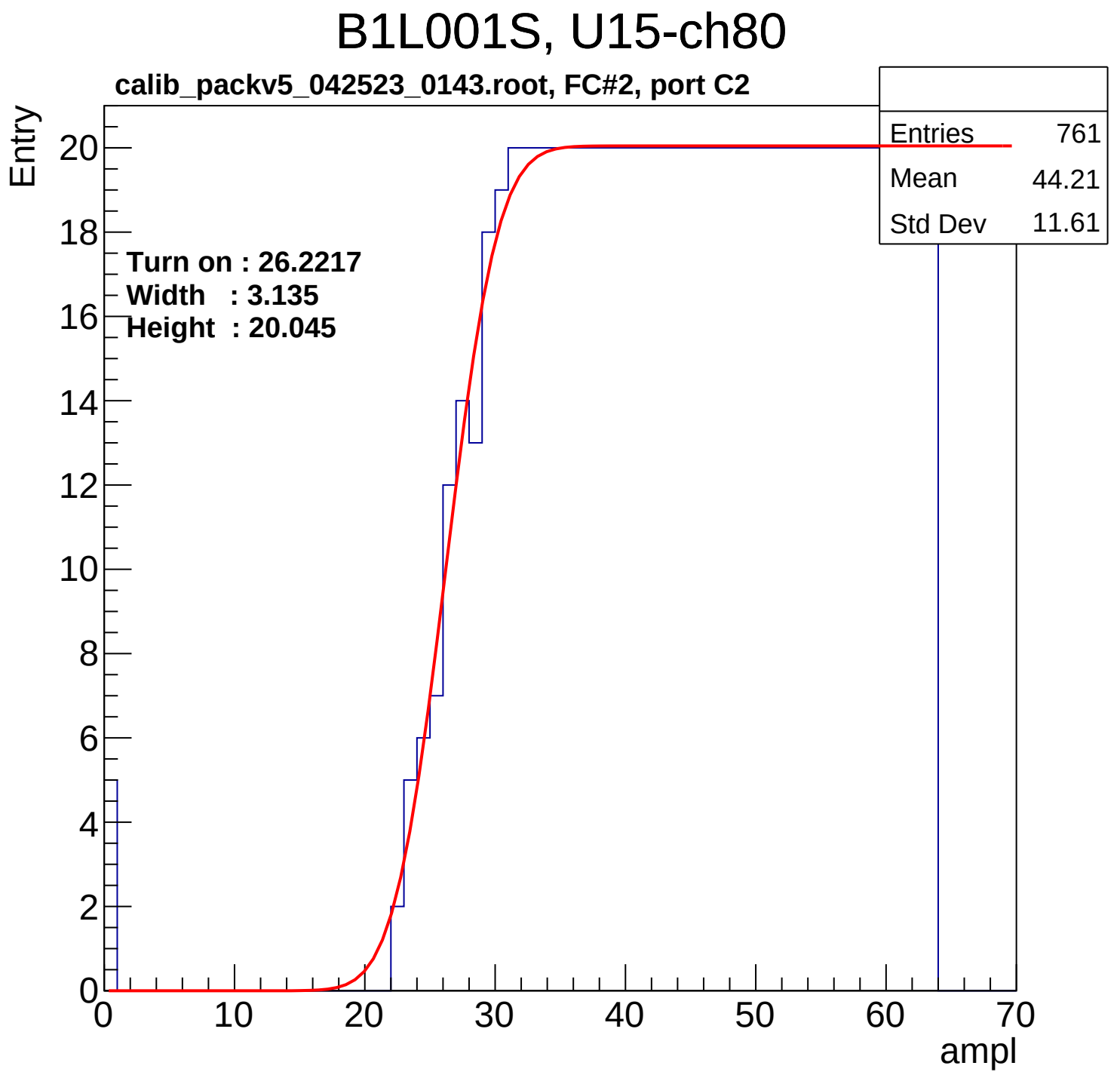
B1L001S, U15-ch80
calib_packv5_042523_0143.root, FC#2, port C2
Entries 761
Mean 44.21
Std Dev 11.61
Turn on : 26.2217
Width : 3.135
Height : 20.045
Entry
ampl
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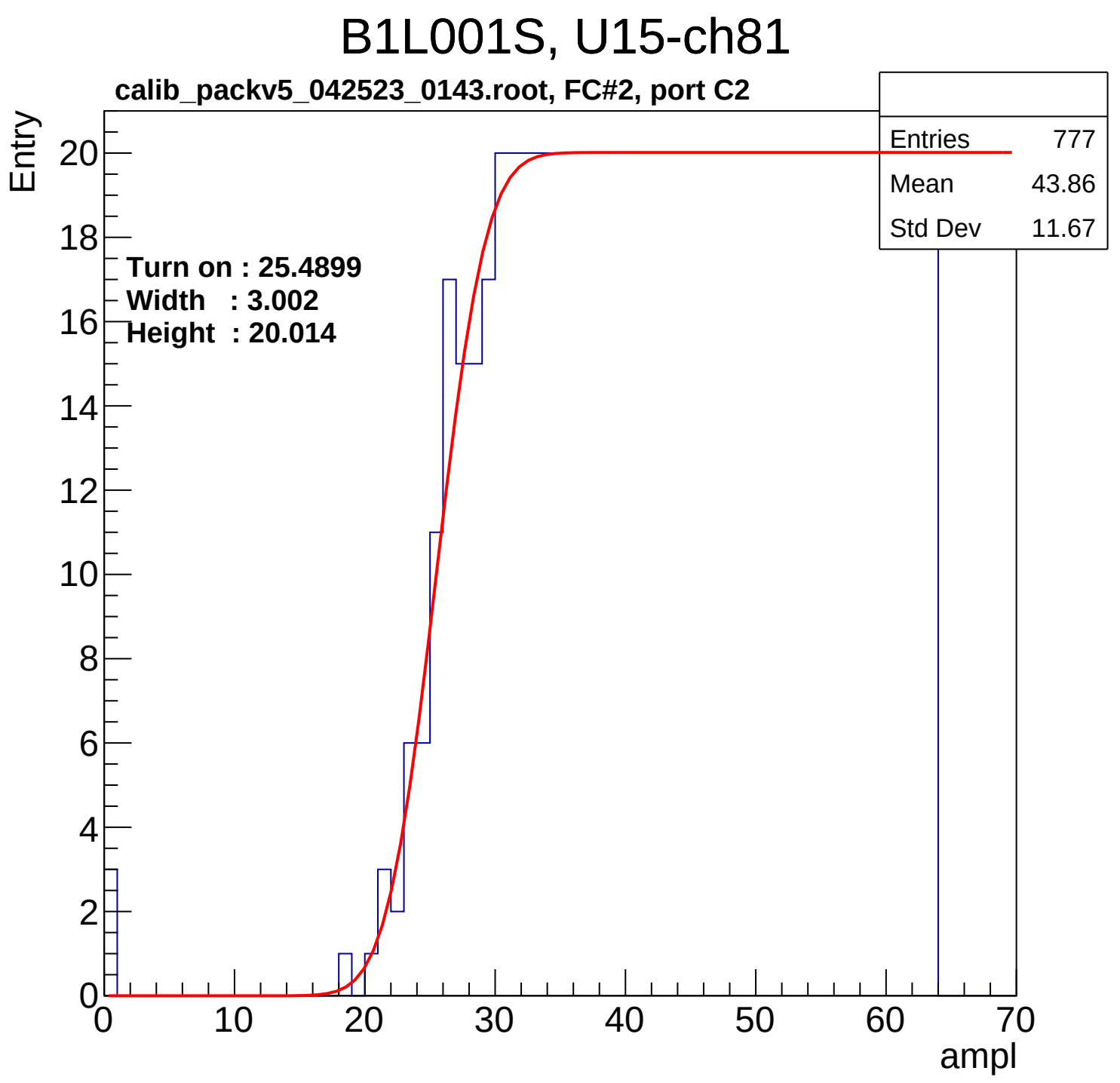
B1L001S, U15-ch81
calib_packv5_042523_0143.root, FC#2, port C2
Entries 777
Mean 43.86
Std Dev 11.67
Turn on : 25.4899
Width : 3.002
Height : 20.014
Entry
ampl
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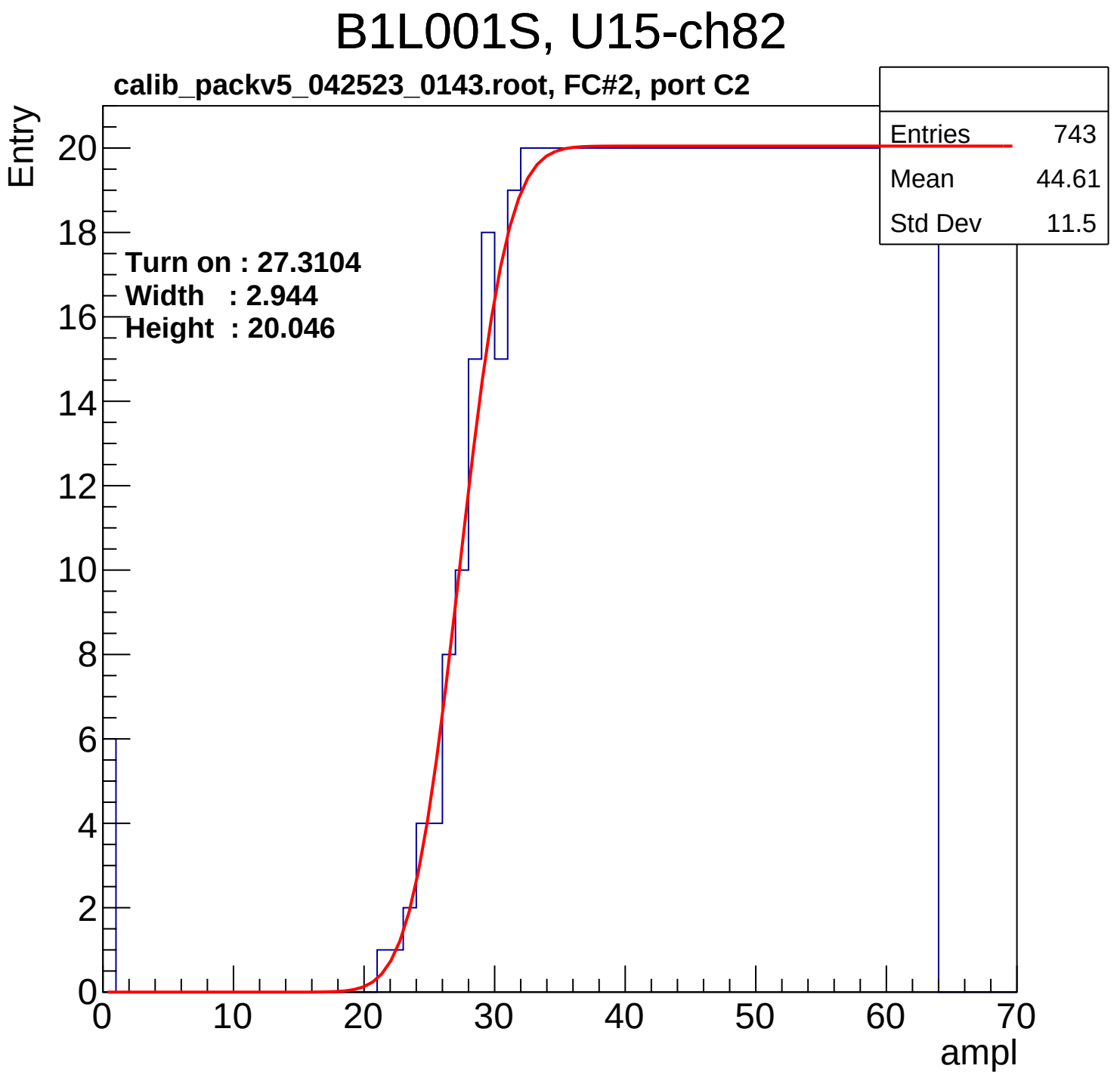
B1L001S, U15-ch82
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.61
Std Dev 11.5
Turn on : 27.3104
Width : 2.944
Height : 20.046
Entry
ampl
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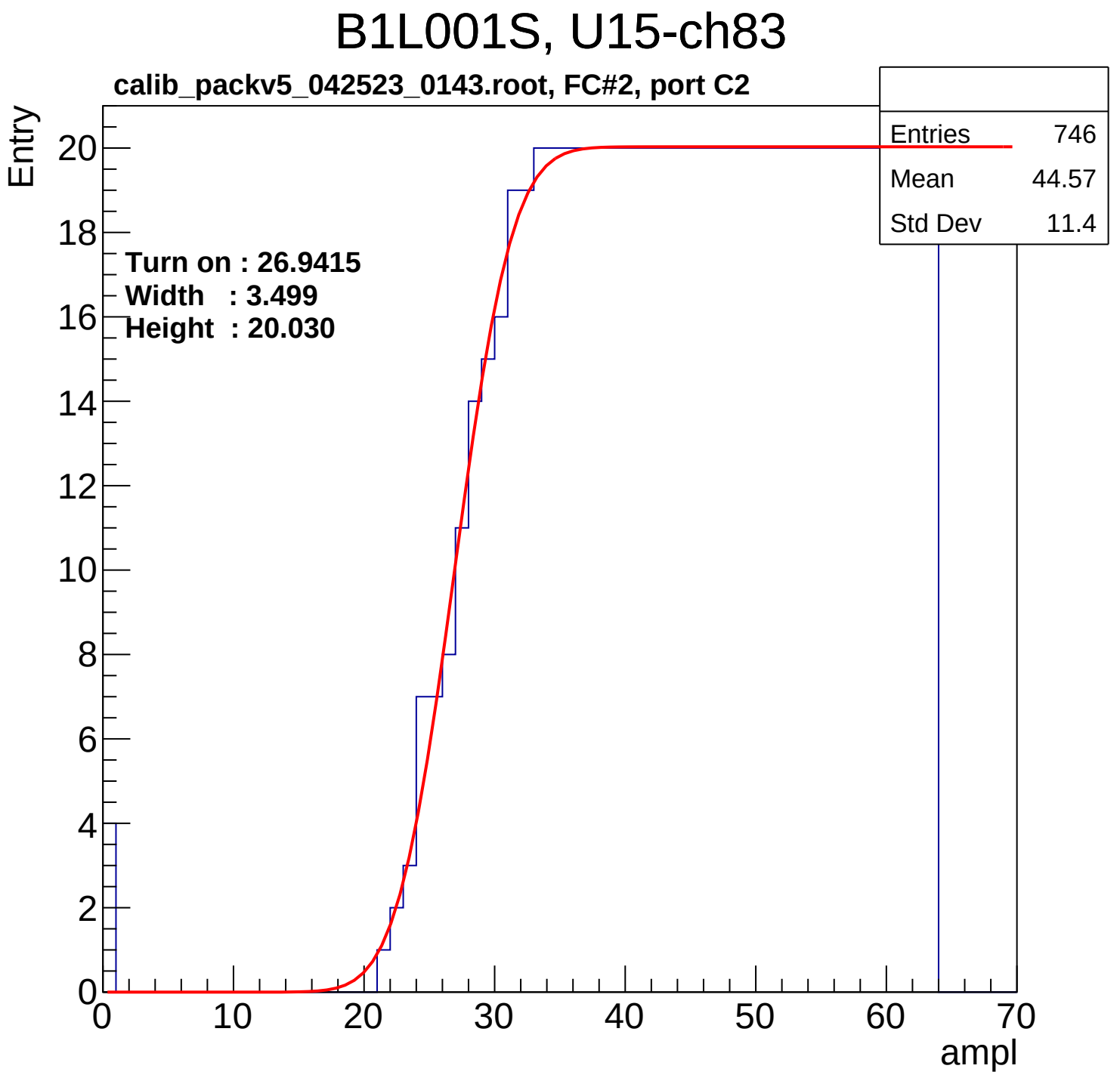
B1L001S, U15-ch83
calib_packv5_042523_0143.root, FC#2, port C2
Entries 746
Mean 44.57
Std Dev 11.4
Turn on : 26.9415
Width : 3.499
Height : 20.030
Entry
ampl
0
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6
8
10
12
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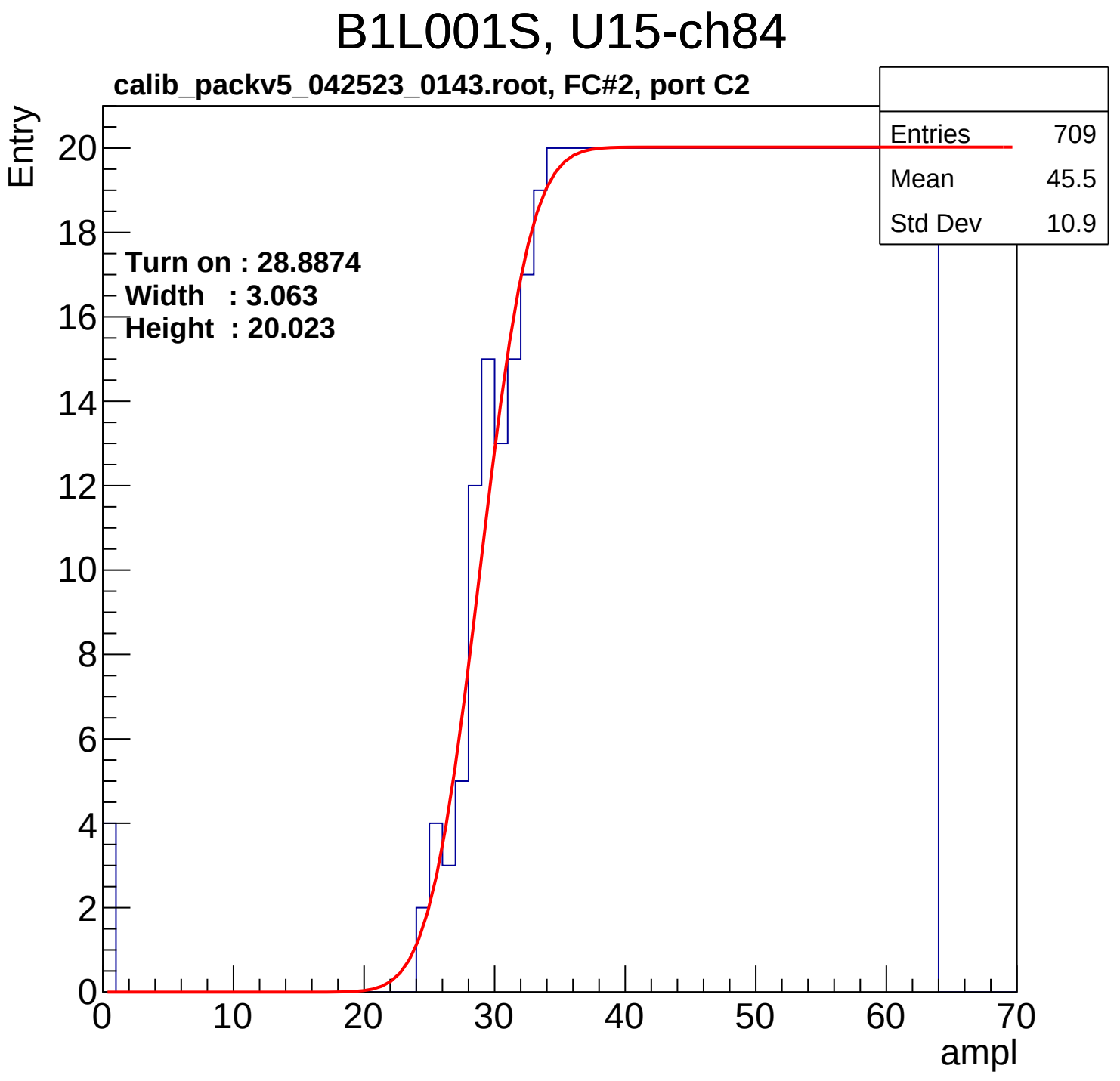
B1L001S, U15-ch84
calib_packv5_042523_0143.root, FC#2, port C2
Entries 709
Mean 45.5
Std Dev 10.9
Turn on : 28.8874
Width : 3.063
Height : 20.023
Entry
ampl
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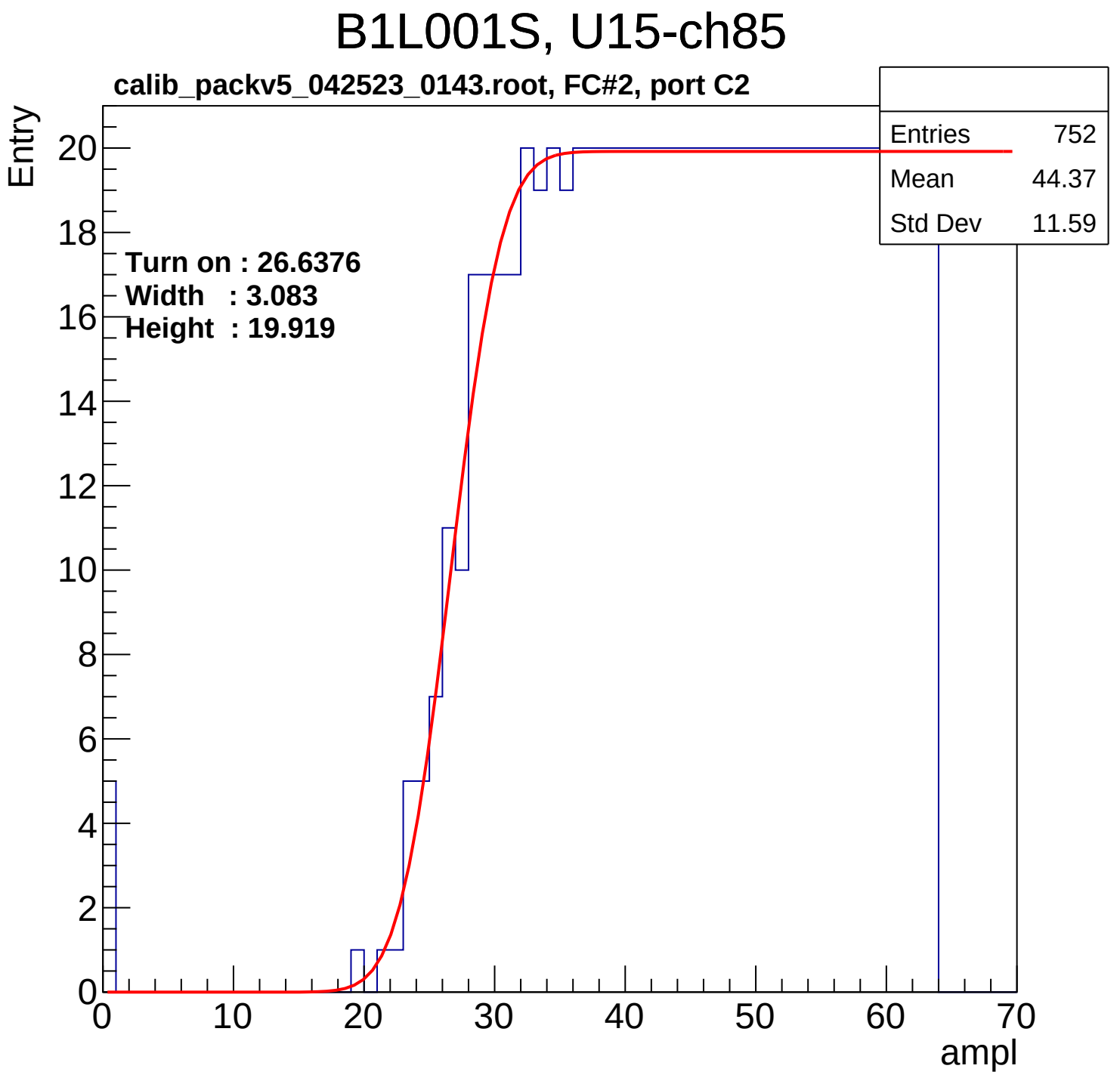
B1L001S, U15-ch85
calib_packv5_042523_0143.root, FC#2, port C2
Entries 752
Mean 44.37
Std Dev 11.59
Turn on : 26.6376
Width : 3.083
Height : 19.919
Entry
ampl
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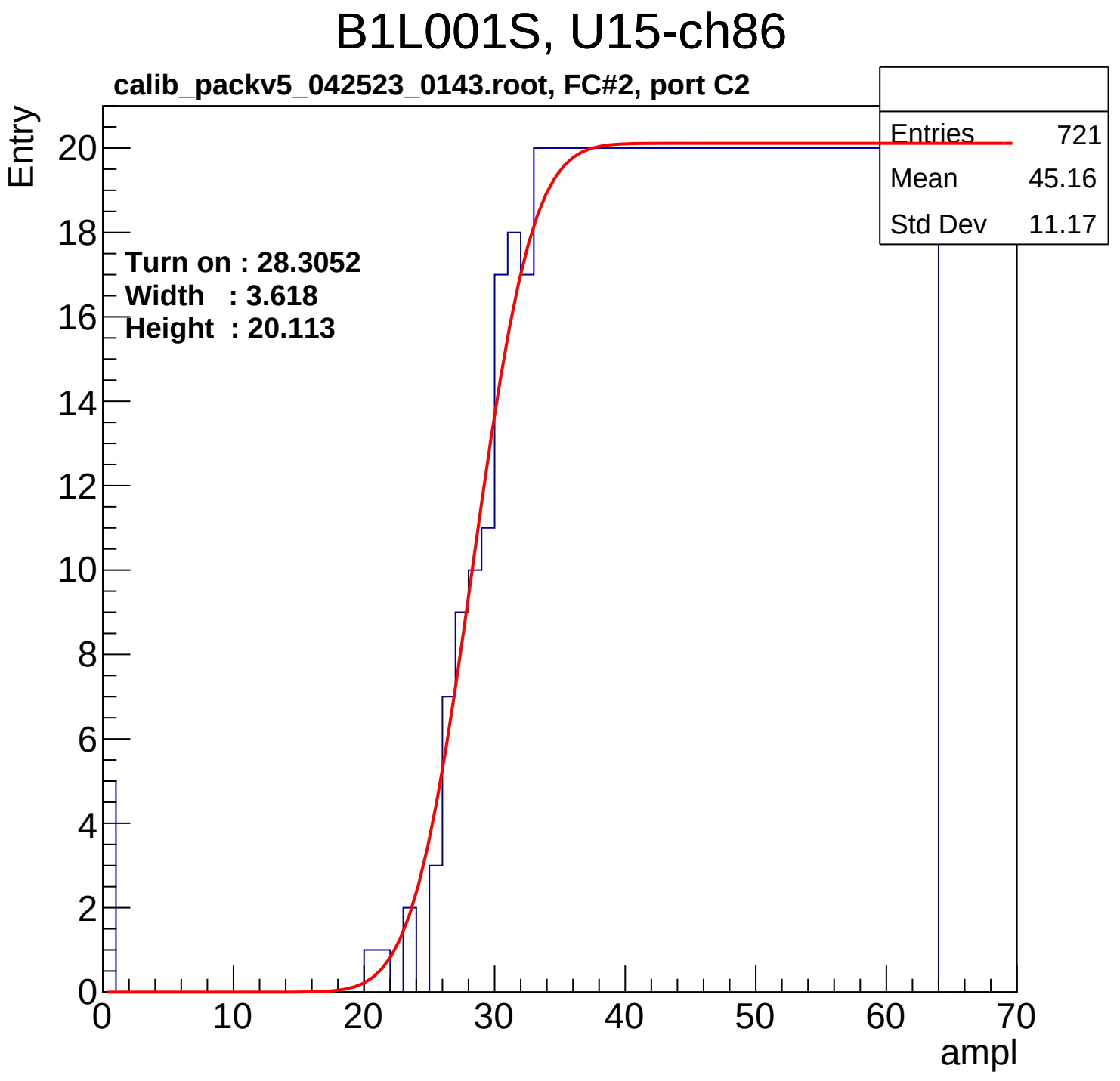
B1L001S, U15-ch86
calib_packv5_042523_0143.root, FC#2, port C2
Entries 721
Mean 45.16
Std Dev 11.17
Turn on : 28.3052
Width : 3.618
Height : 20.113
Entry
ampl
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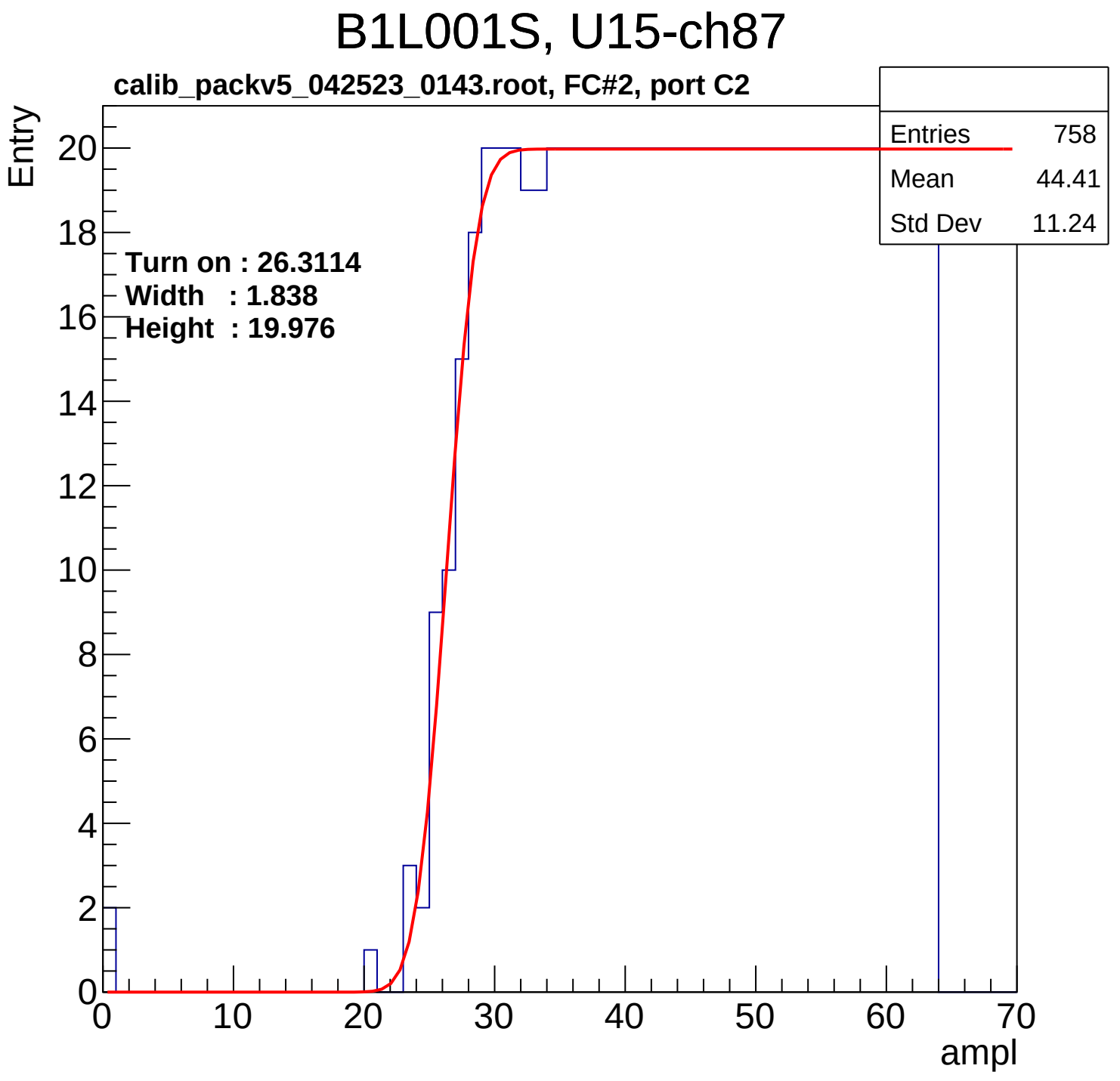
B1L001S, U15-ch87
calib_packv5_042523_0143.root, FC#2, port C2
Entries 758
Mean 44.41
Std Dev 11.24
Turn on : 26.3114
Width : 1.838
Height : 19.976
Entry
ampl
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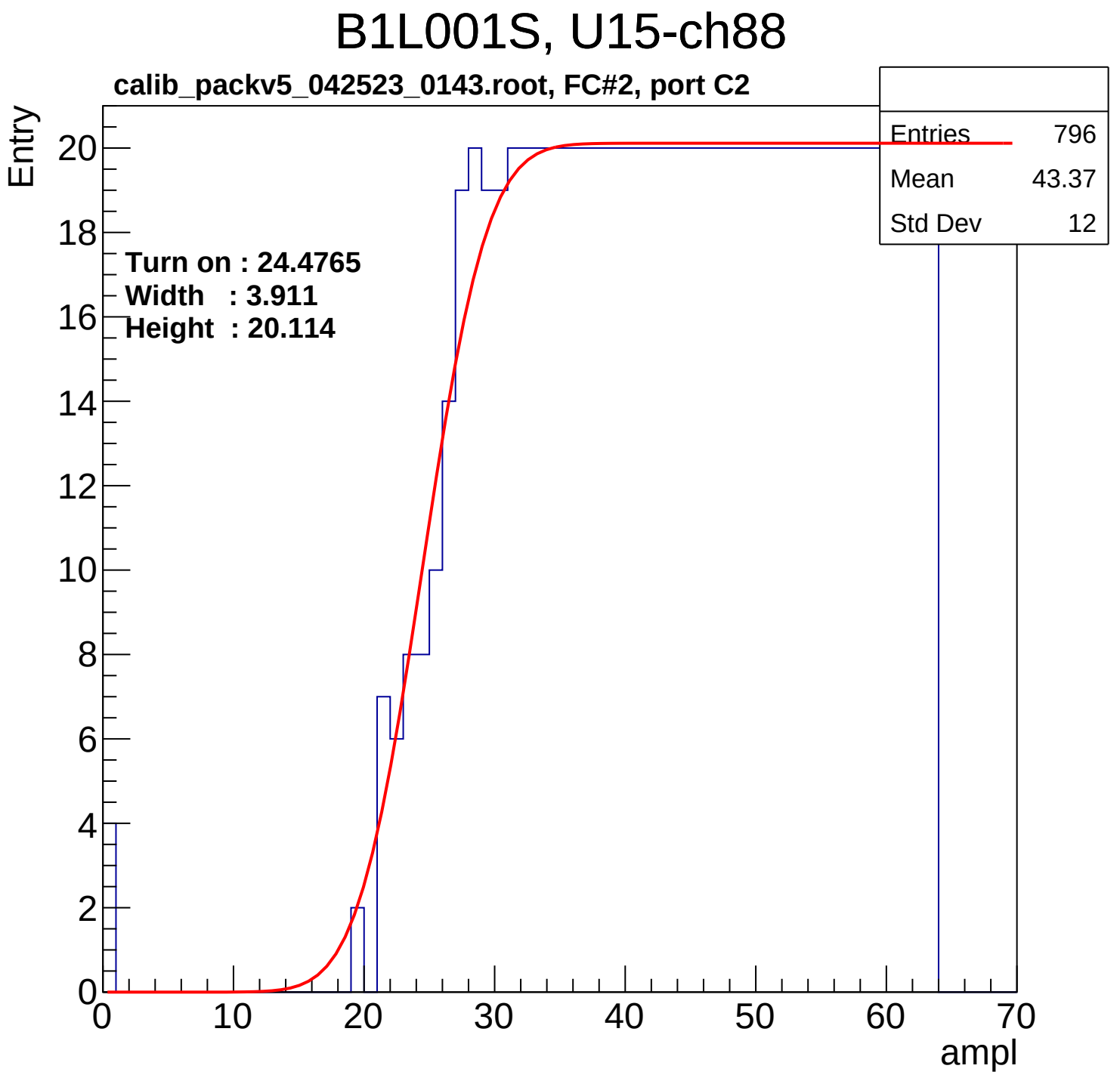
B1L001S, U15-ch88
calib_packv5_042523_0143.root, FC#2, port C2
Entries 796
Mean 43.37
Std Dev 12
Turn on : 24.4765
Width : 3.911
Height : 20.114
Entry
ampl
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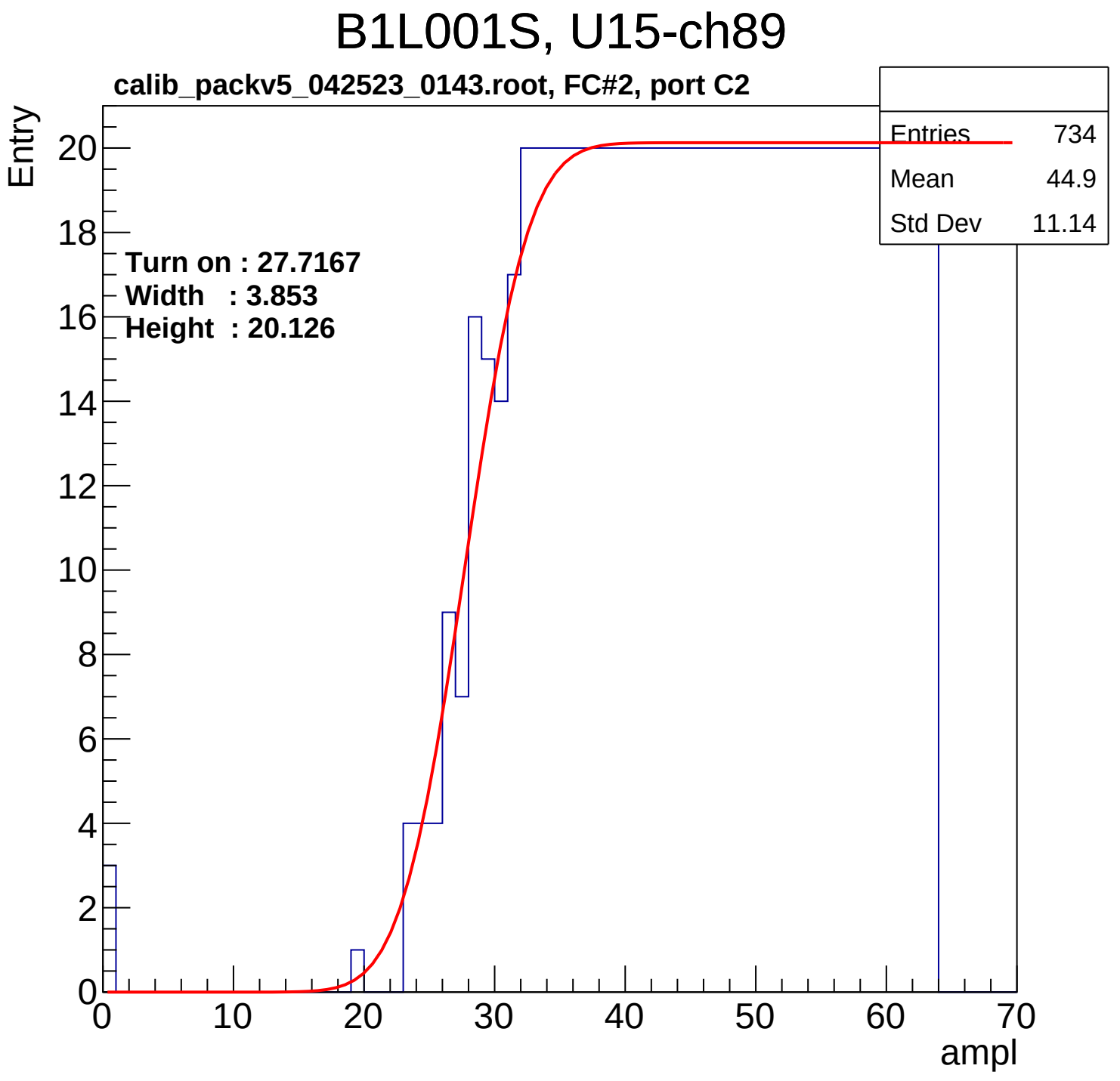
B1L001S, U15-ch89
calib_packv5_042523_0143.root, FC#2, port C2
Entries 734
Mean 44.9
Std Dev 11.14
Turn on : 27.7167
Width : 3.853
Height : 20.126
Entry
ampl
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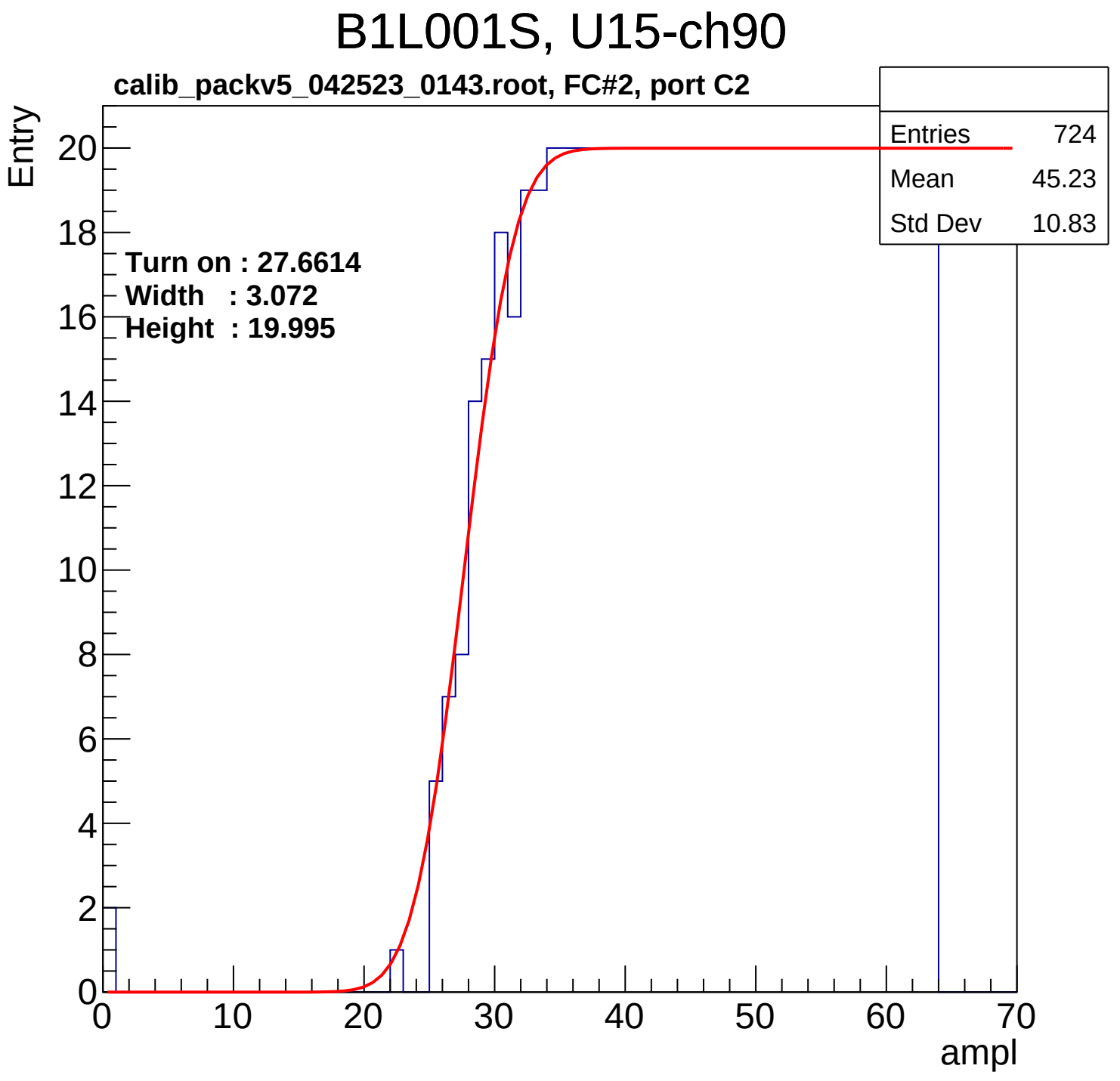
B1L001S, U15-ch90
calib_packv5_042523_0143.root, FC#2, port C2
Entries 724
Mean 45.23
Std Dev 10.83
Turn on : 27.6614
Width : 3.072
Height : 19.995
Entry
ampl
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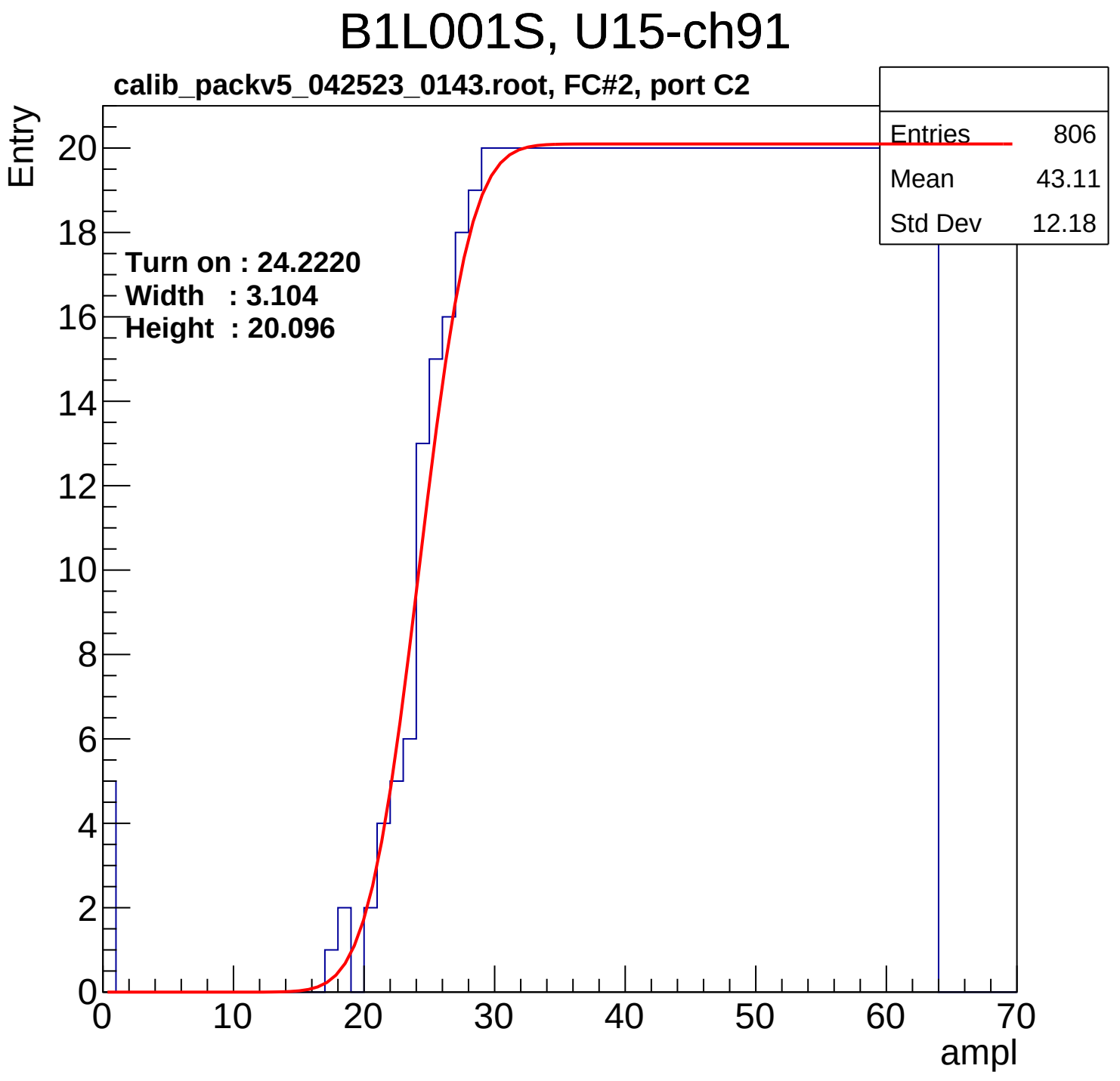
B1L001S, U15-ch91
calib_packv5_042523_0143.root, FC#2, port C2
Entries 806
Mean 43.11
Std Dev 12.18
Turn on : 24.2220
Width : 3.104
Height : 20.096
Entry
ampl
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6
8
10
12
14
16
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0
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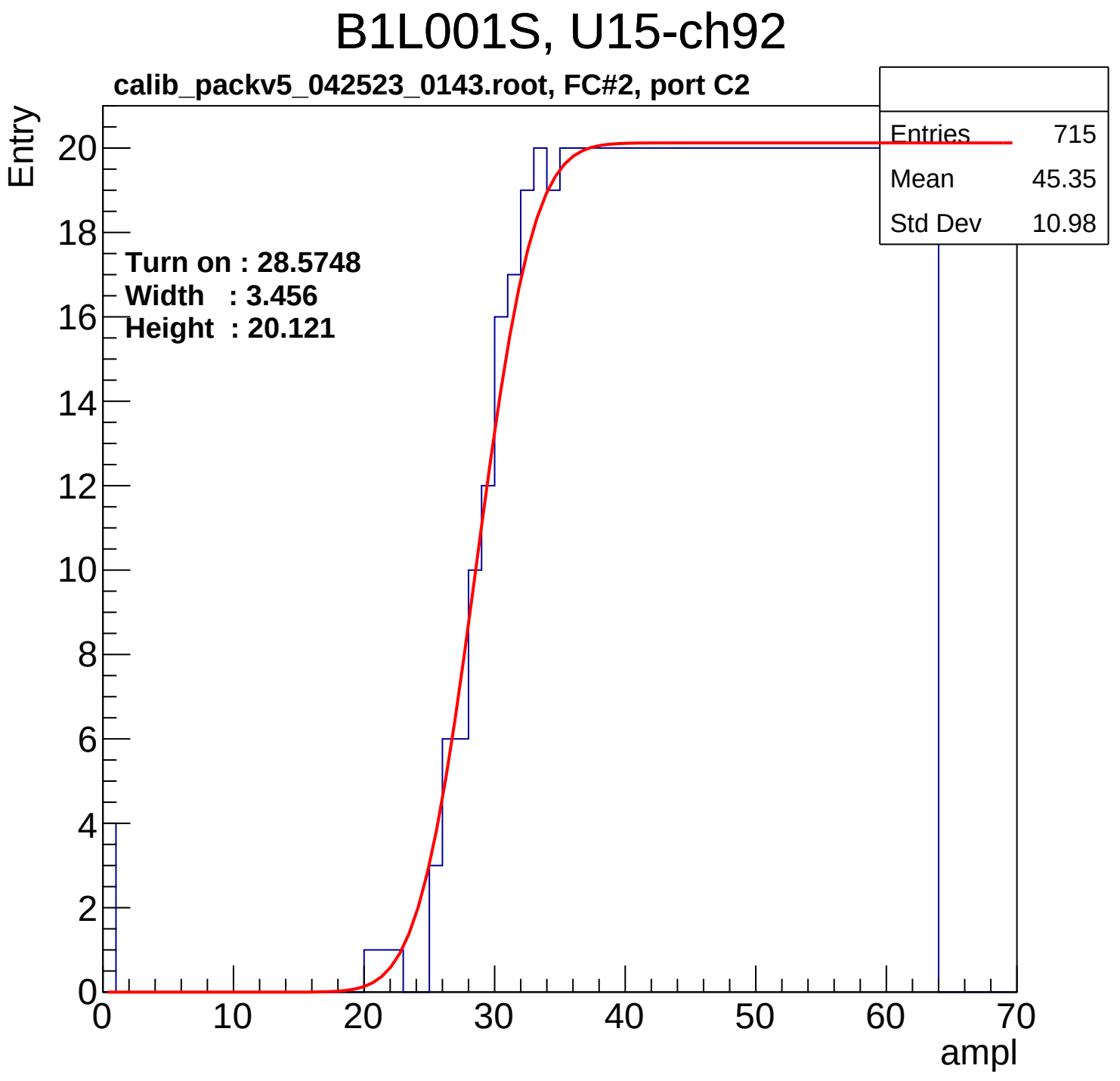
B1L001S, U15-ch92
calib_packv5_042523_0143.root, FC#2, port C2
Entries 715
Mean 45.35
Std Dev 10.98
Turn on : 28.5748
Width : 3.456
Height : 20.121
Entry
ampl
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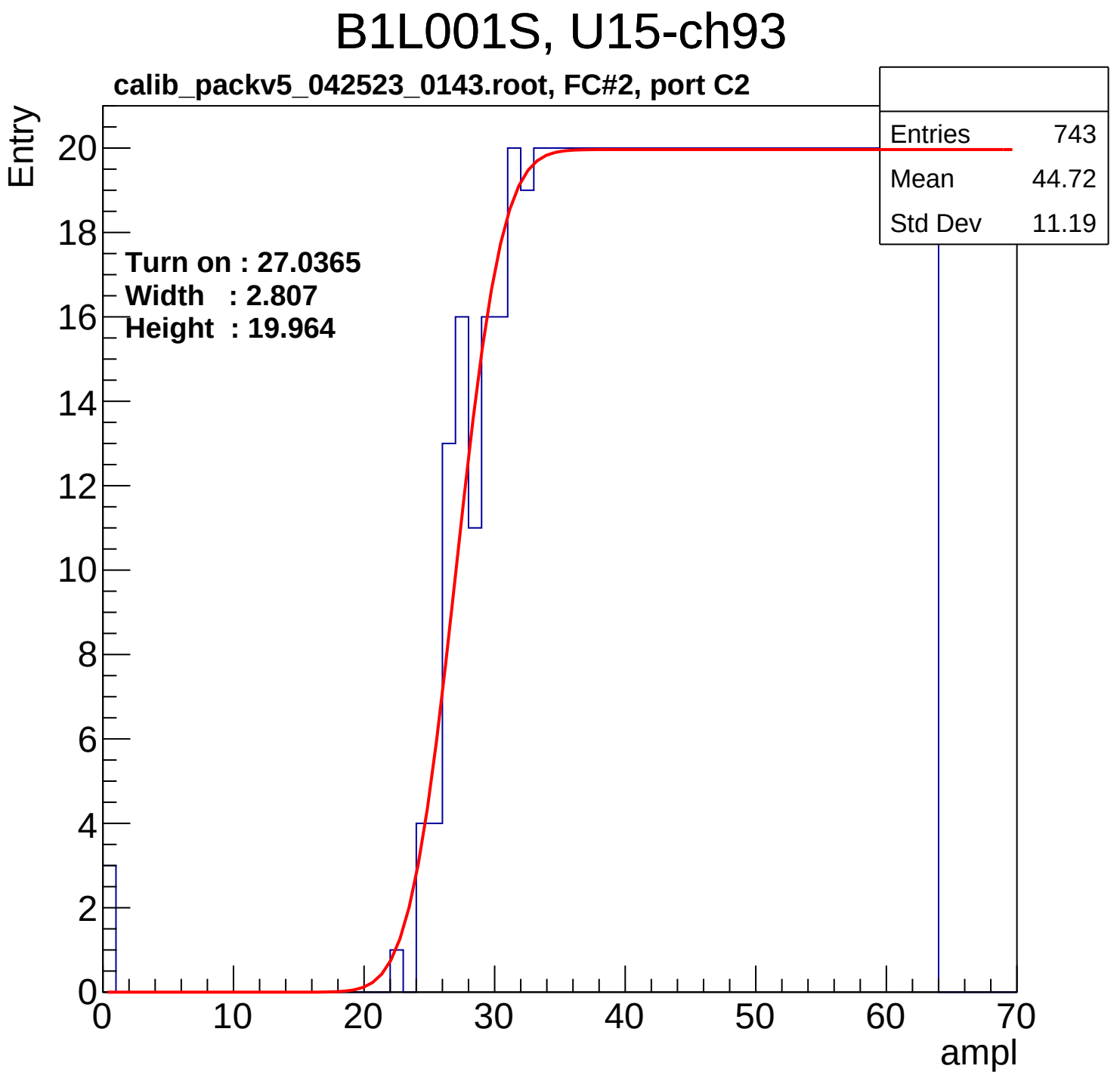
B1L001S, U15-ch93
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.72
Std Dev 11.19
Turn on : 27.0365
Width : 2.807
Height : 19.964
Entry
ampl
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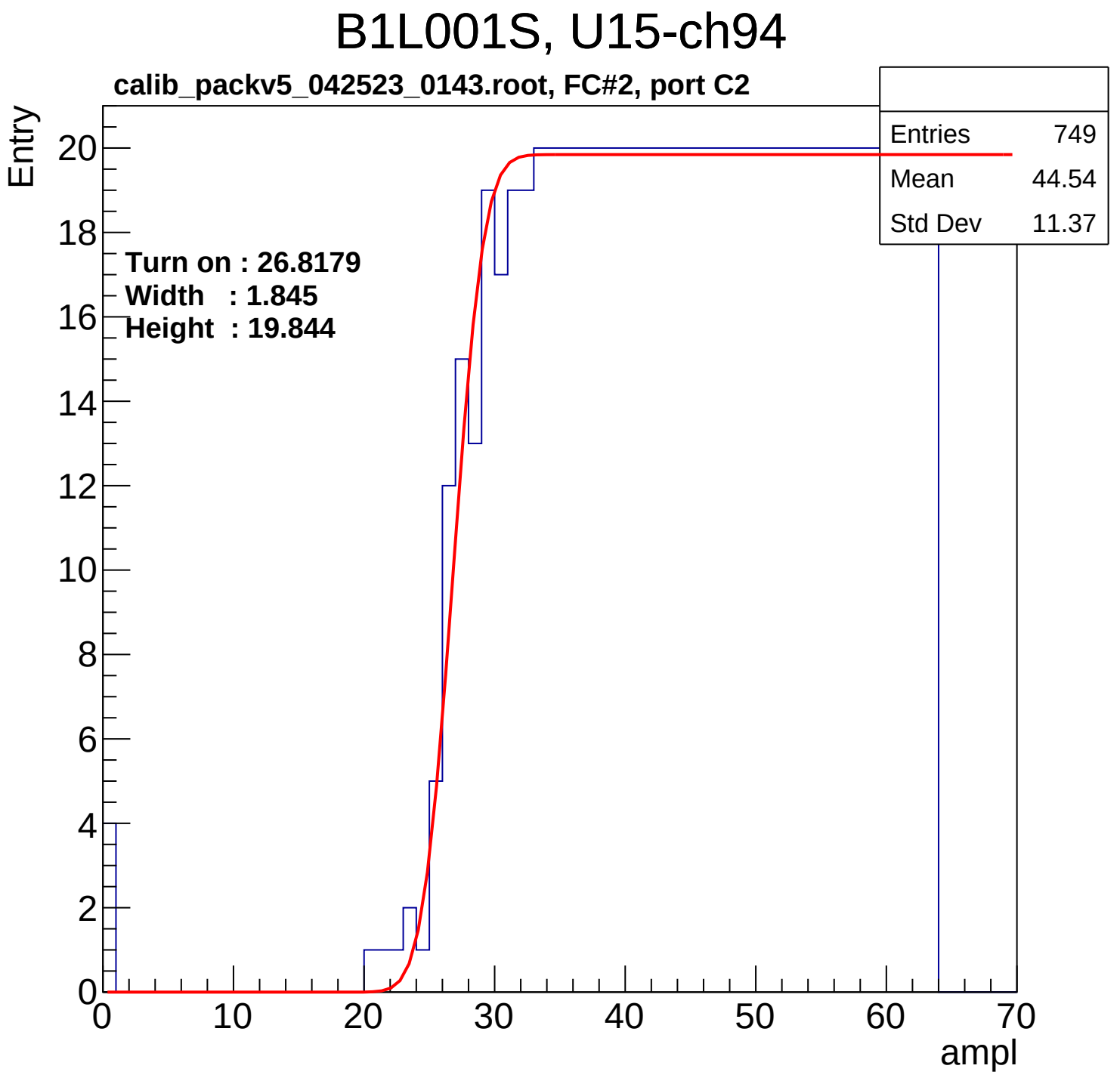
B1L001S, U15-ch94
calib_packv5_042523_0143.root, FC#2, port C2
Entries 749
Mean 44.54
Std Dev 11.37
Turn on : 26.8179
Width : 1.845
Height : 19.844
Entry
ampl
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8
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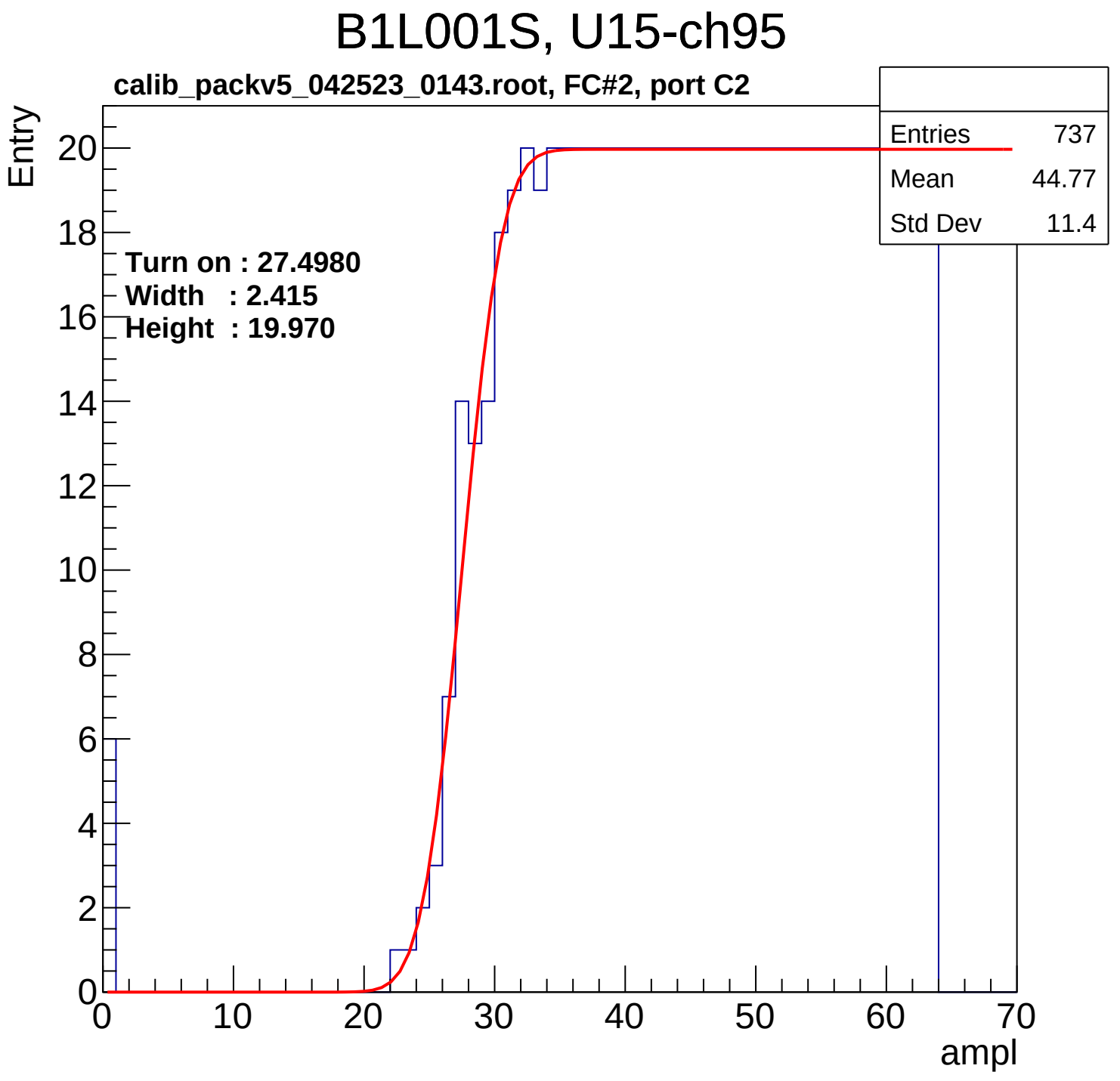
B1L001S, U15-ch95
calib_packv5_042523_0143.root, FC#2, port C2
Entries 737
Mean 44.77
Std Dev 11.4
Turn on : 27.4980
Width : 2.415
Height : 19.970
Entry
ampl
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6
8
10
12
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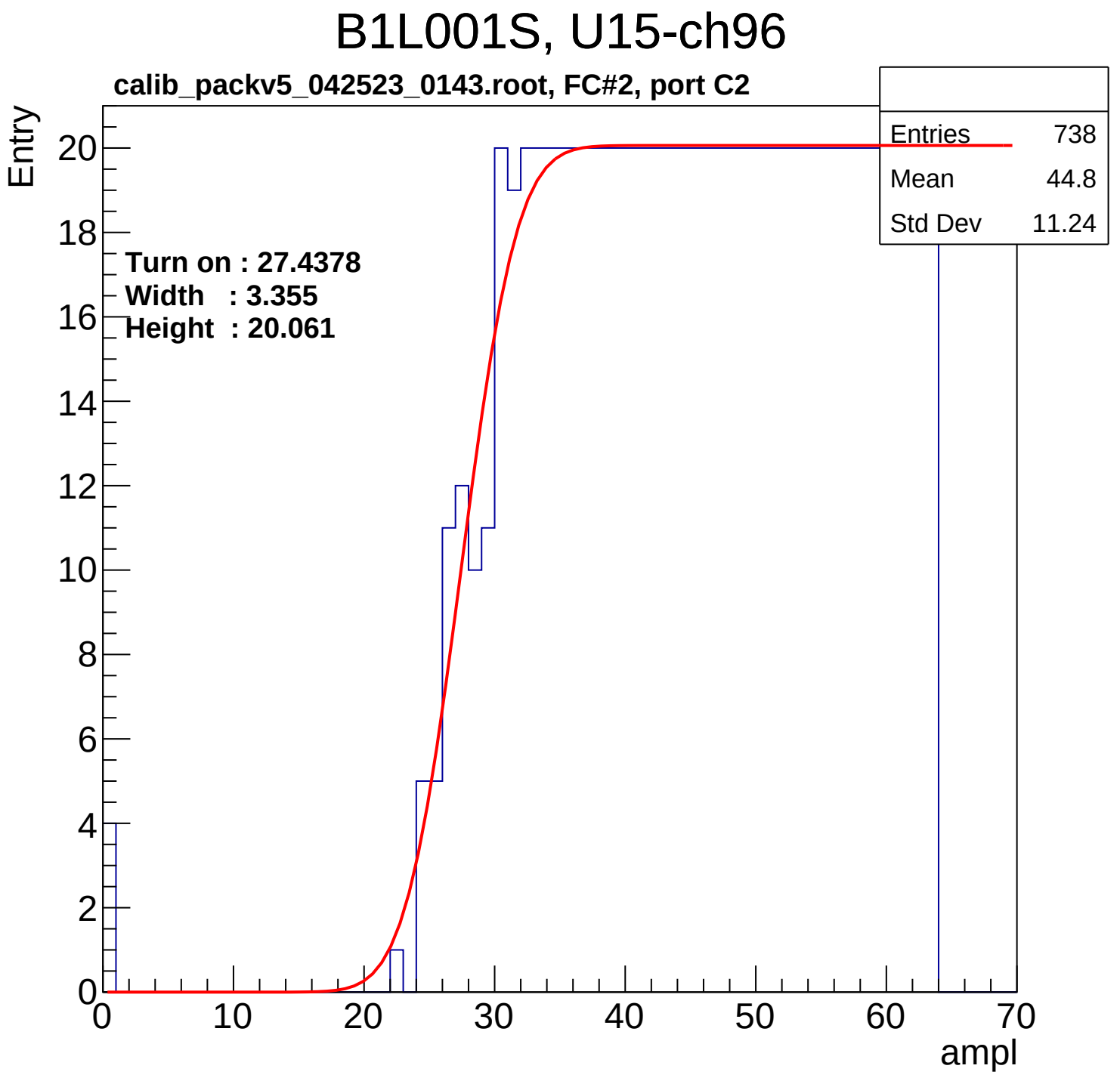
B1L001S, U15-ch96
calib_packv5_042523_0143.root, FC#2, port C2
Entries 738
Mean 44.8
Std Dev 11.24
Turn on : 27.4378
Width : 3.355
Height : 20.061
Entry
ampl
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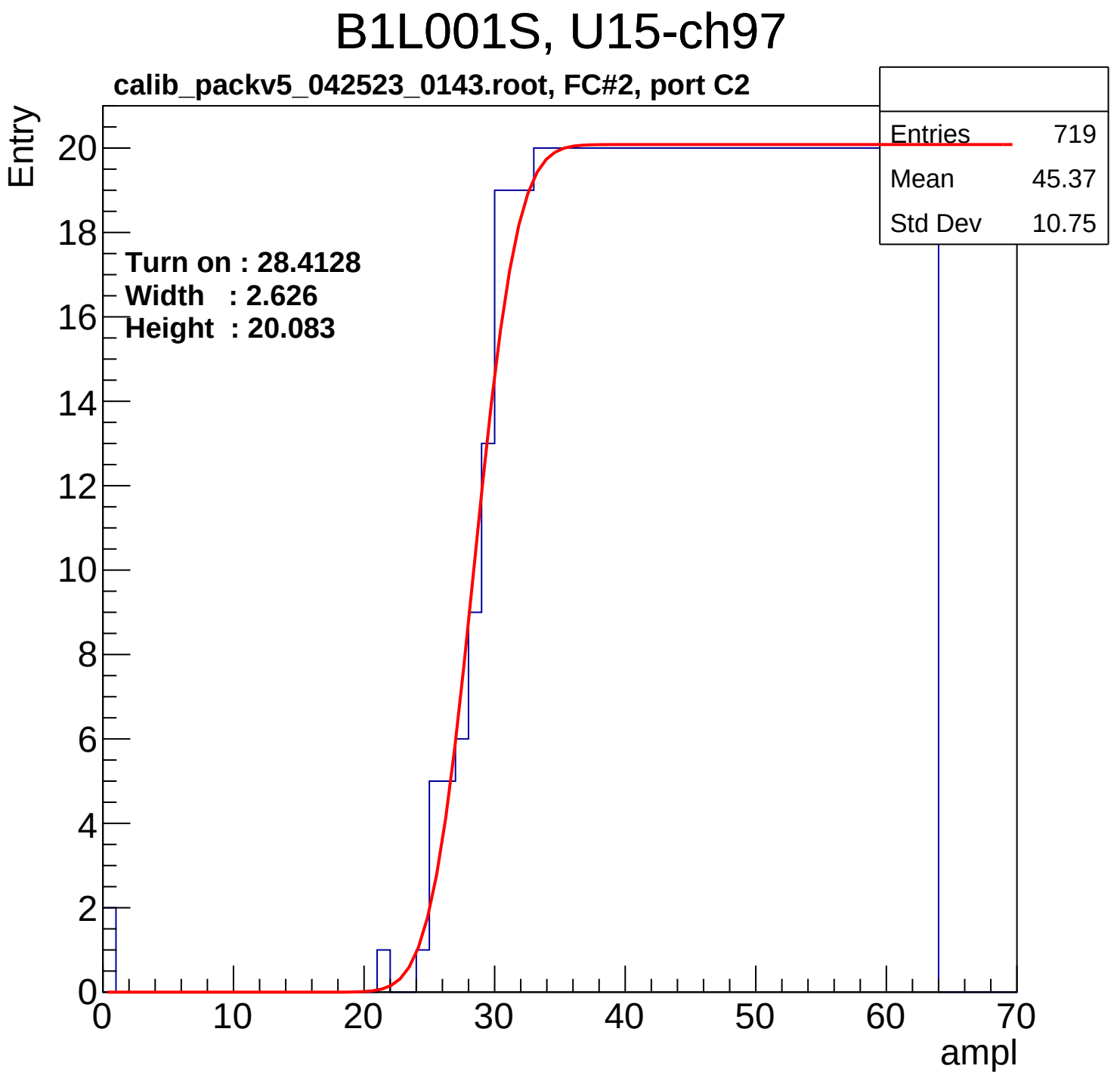
B1L001S, U15-ch97
calib_packv5_042523_0143.root, FC#2, port C2
Entries 719
Mean 45.37
Std Dev 10.75
Turn on : 28.4128
Width : 2.626
Height : 20.083
Entry
ampl
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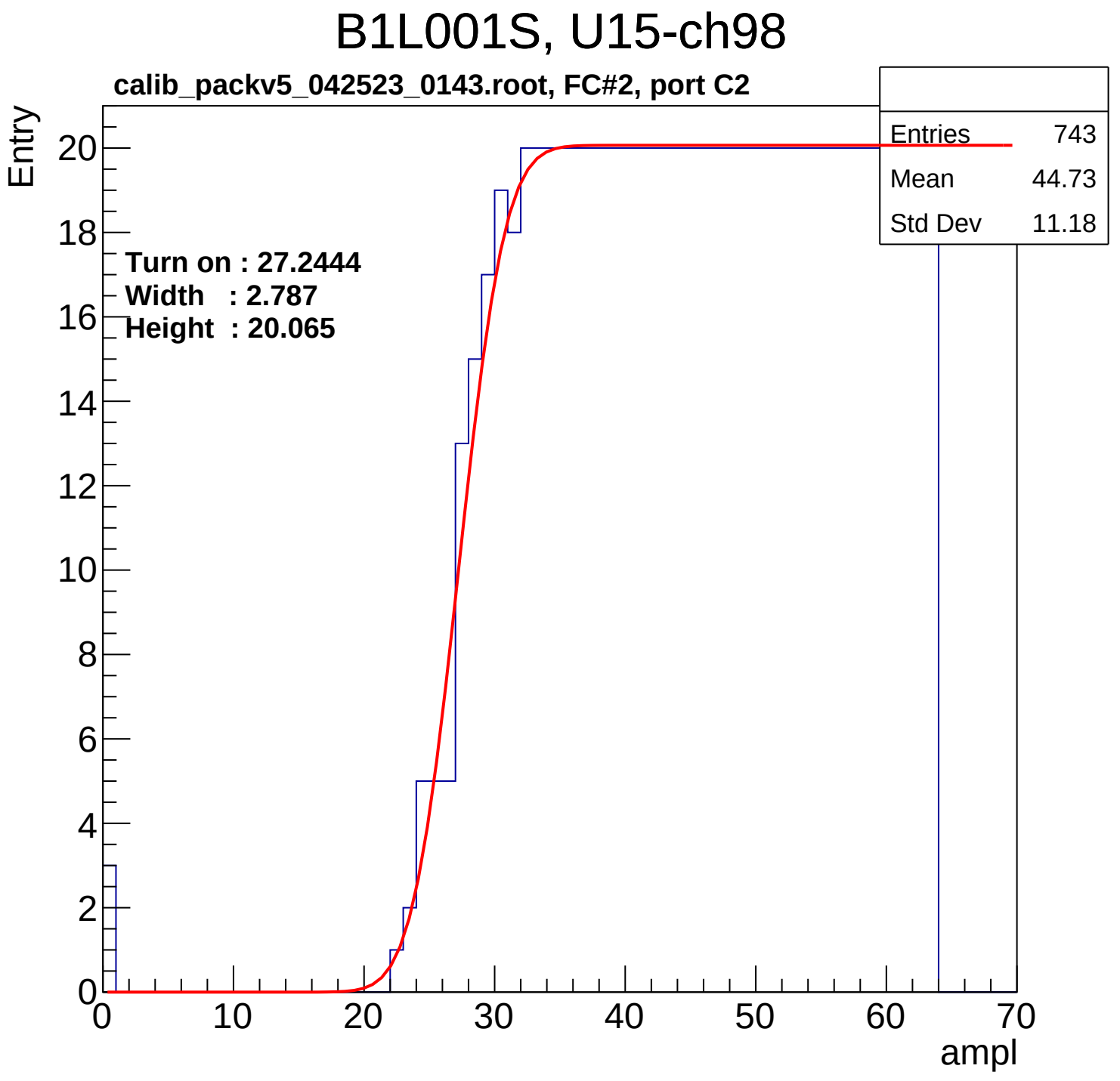
B1L001S, U15-ch98
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.73
Std Dev 11.18
Turn on : 27.2444
Width : 2.787
Height : 20.065
Entry
ampl
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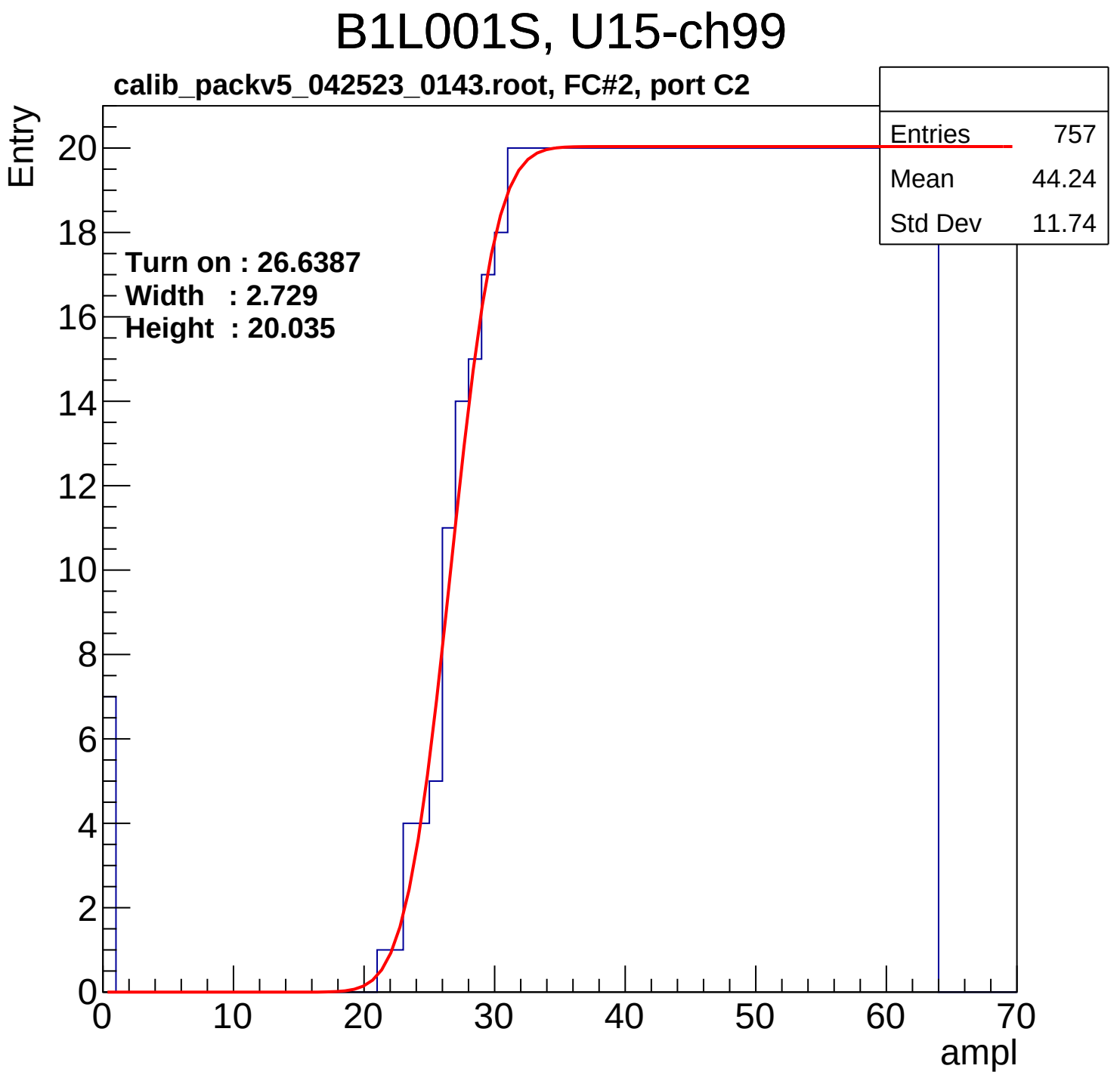
B1L001S, U15-ch99
calib_packv5_042523_0143.root, FC#2, port C2
Entries 757
Mean 44.24
Std Dev 11.74
Turn on : 26.6387
Width : 2.729
Height : 20.035
Entry
ampl
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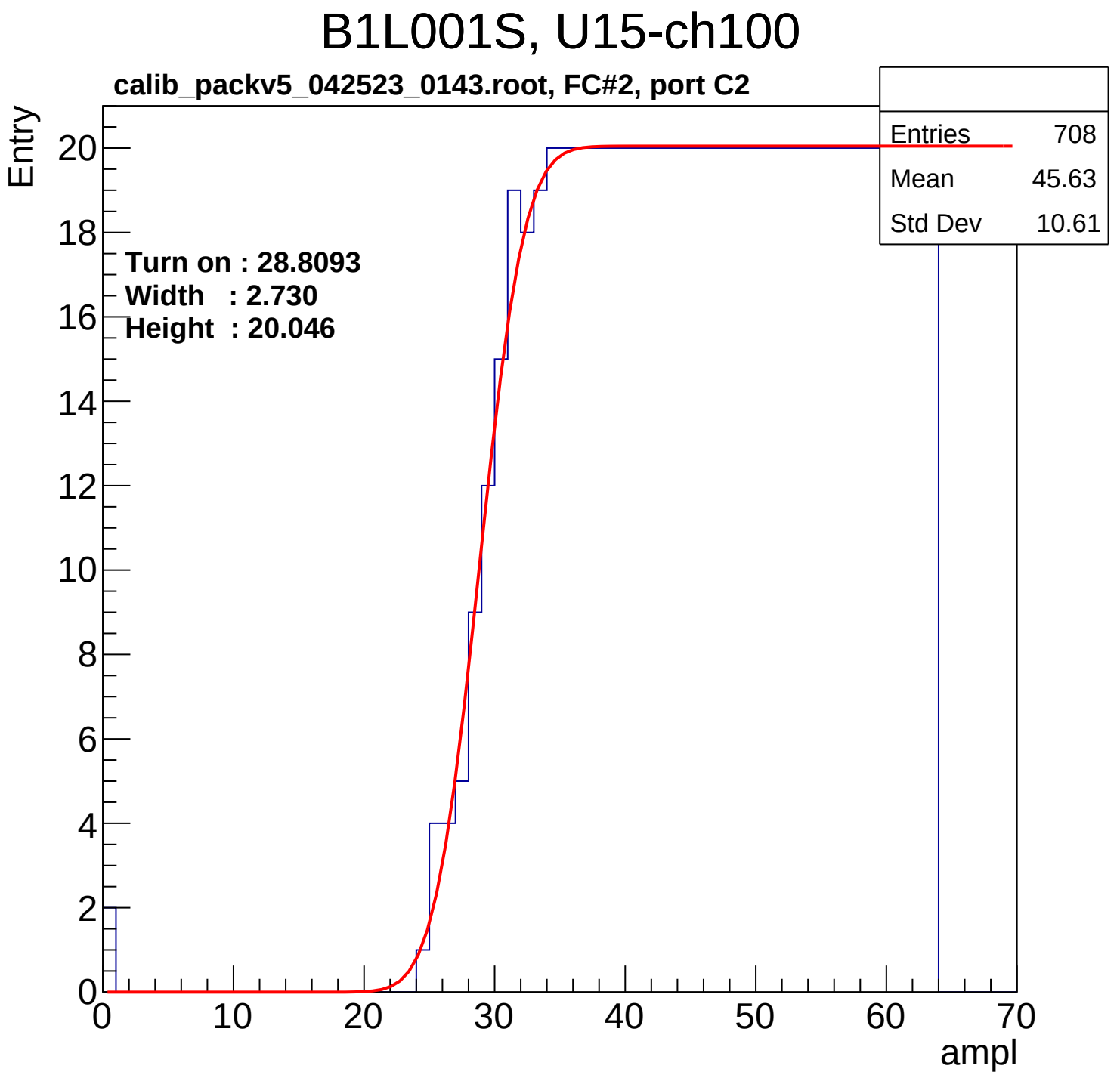
B1L001S, U15-ch100
calib_packv5_042523_0143.root, FC#2, port C2
Entries 708
Mean 45.63
Std Dev 10.61
Turn on : 28.8093
Width : 2.730
Height : 20.046
Entry
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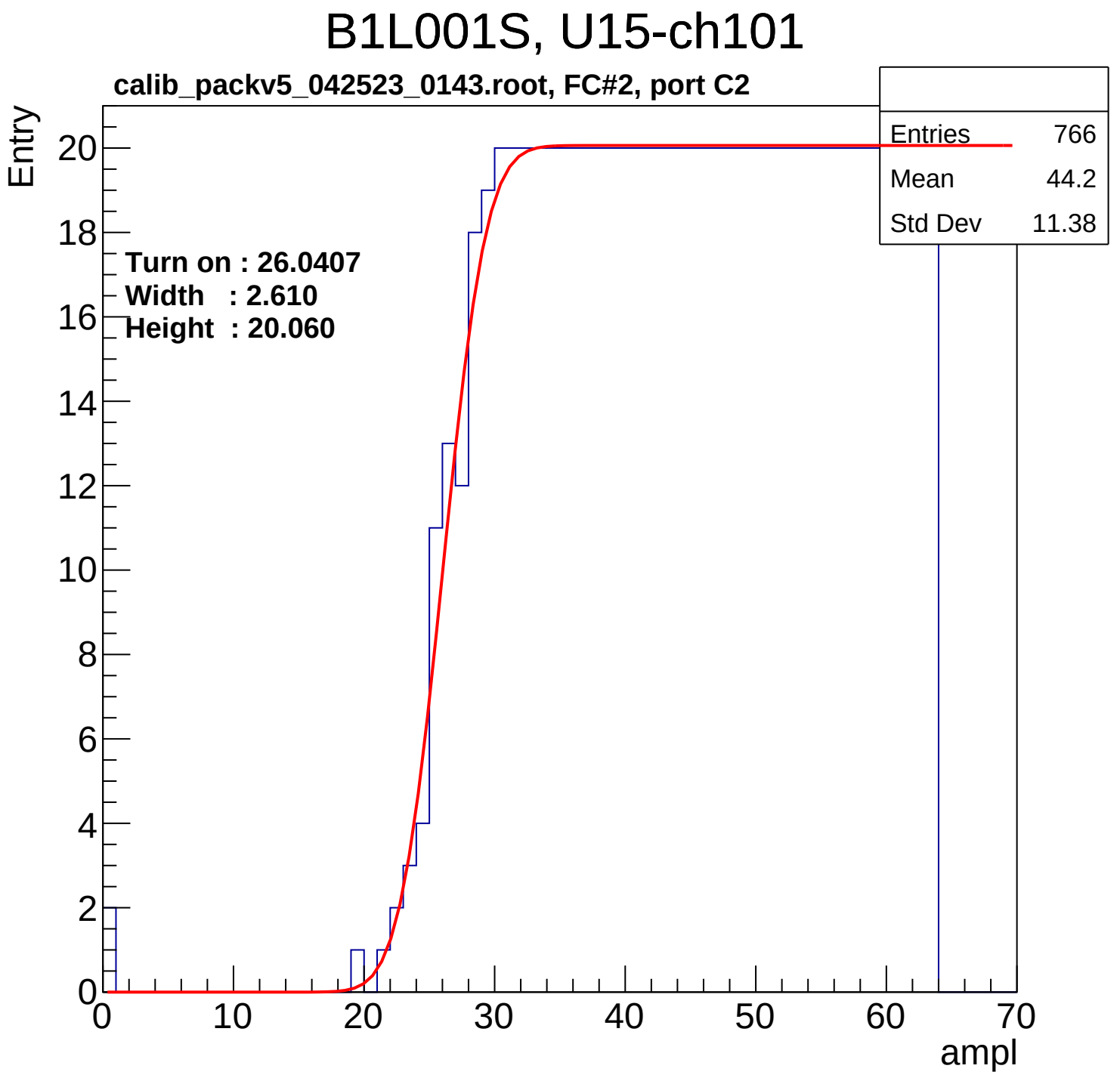
B1L001S, U15-ch101
calib_packv5_042523_0143.root, FC#2, port C2
Entries 766
Mean 44.2
Std Dev 11.38
Turn on : 26.0407
Width : 2.610
Height : 20.060
Entry
ampl
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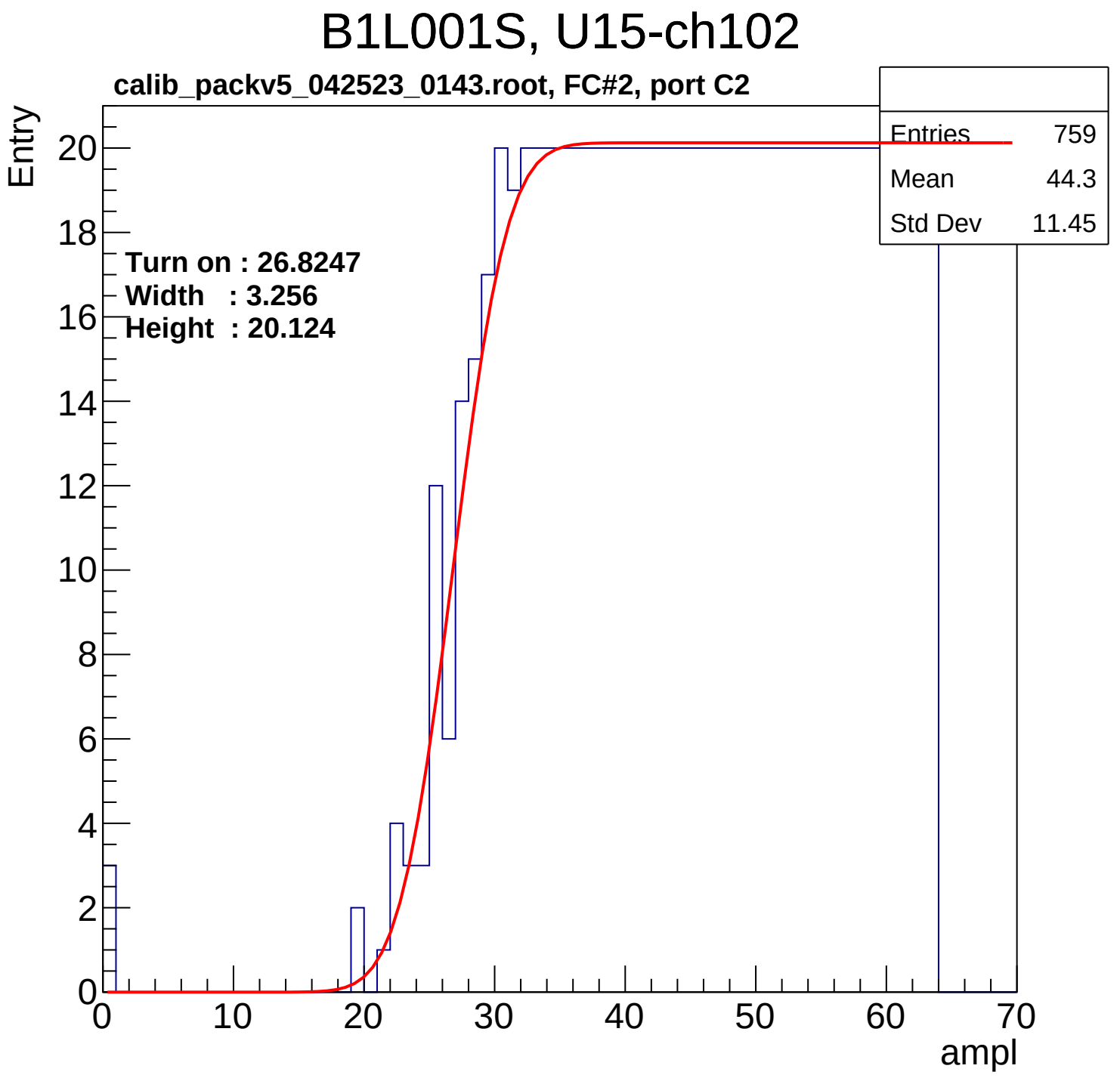
B1L001S, U15-ch102
calib_packv5_042523_0143.root, FC#2, port C2
Entries 759
Mean 44.3
Std Dev 11.45
Turn on : 26.8247
Width : 3.256
Height : 20.124
Entry
ampl
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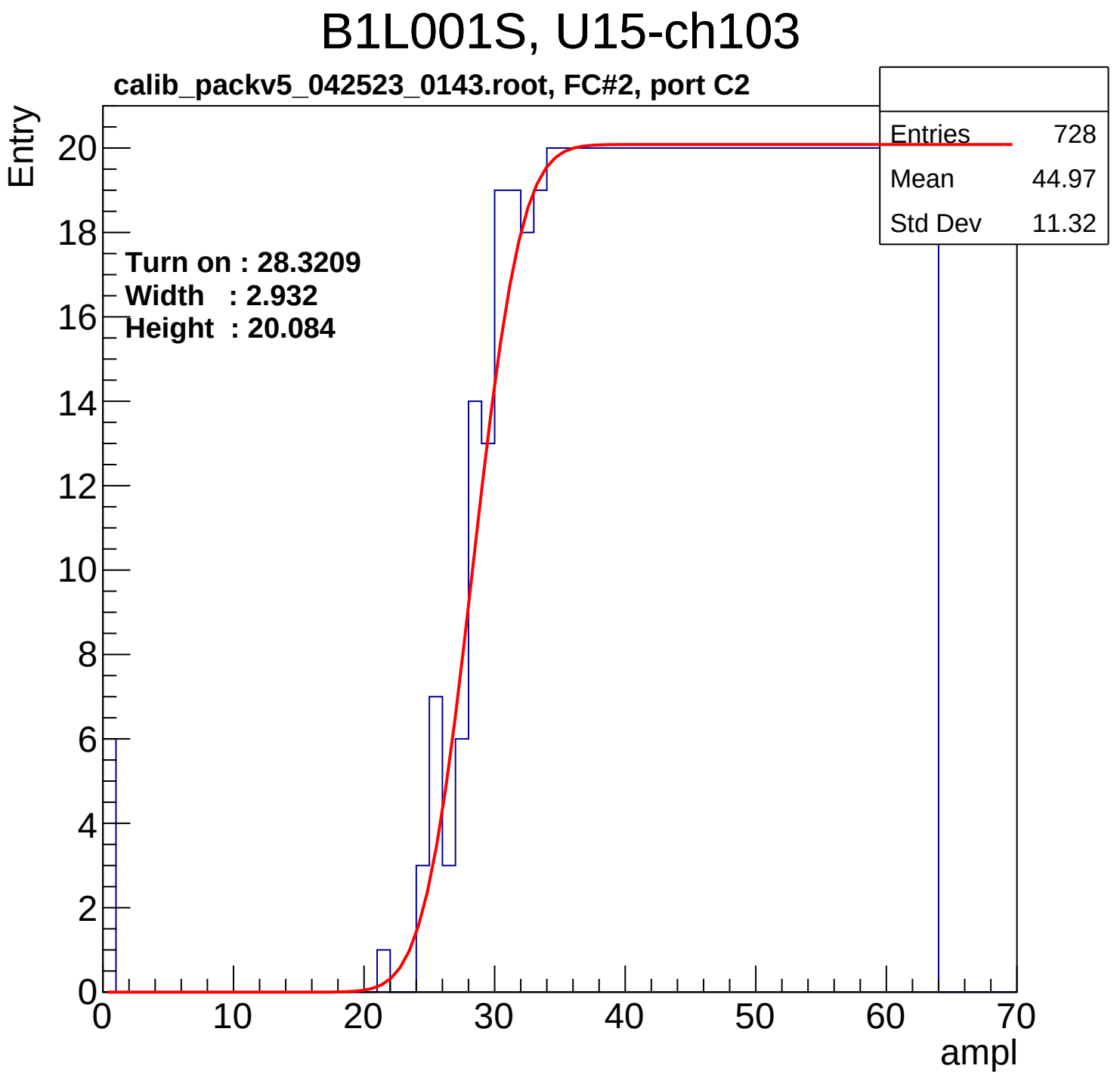
B1L001S, U15-ch103
calib_packv5_042523_0143.root, FC#2, port C2
Entries 728
Mean 44.97
Std Dev 11.32
Turn on : 28.3209
Width : 2.932
Height : 20.084
Entry
ampl
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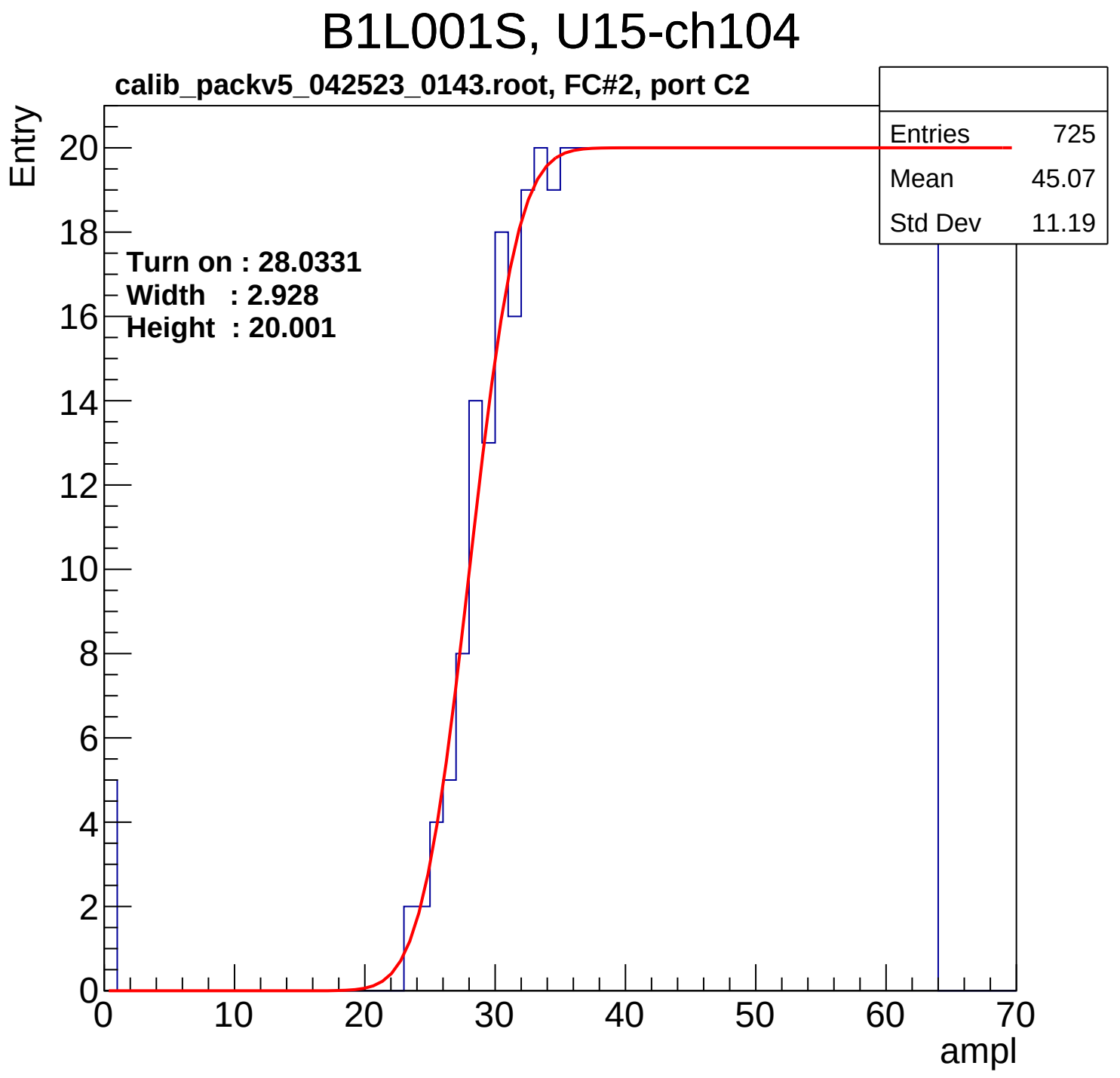
B1L001S, U15-ch104
calib_packv5_042523_0143.root, FC#2, port C2
Entries 725
Mean 45.07
Std Dev 11.19
Turn on : 28.0331
Width : 2.928
Height : 20.001
Entry
ampl
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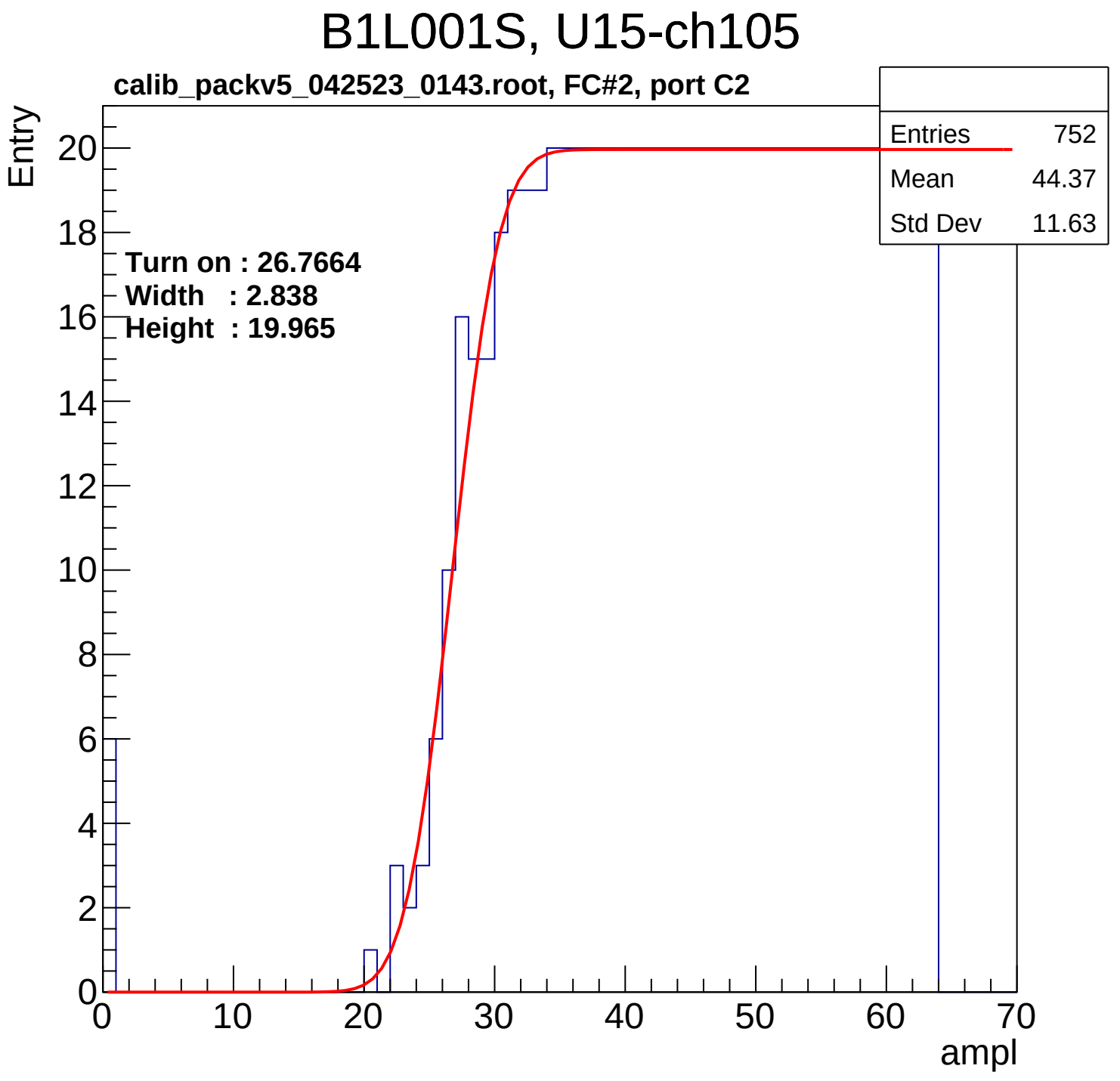
B1L001S, U15-ch105
calib_packv5_042523_0143.root, FC#2, port C2
Entries 752
Mean 44.37
Std Dev 11.63
Turn on : 26.7664
Width : 2.838
Height : 19.965
Entry
ampl
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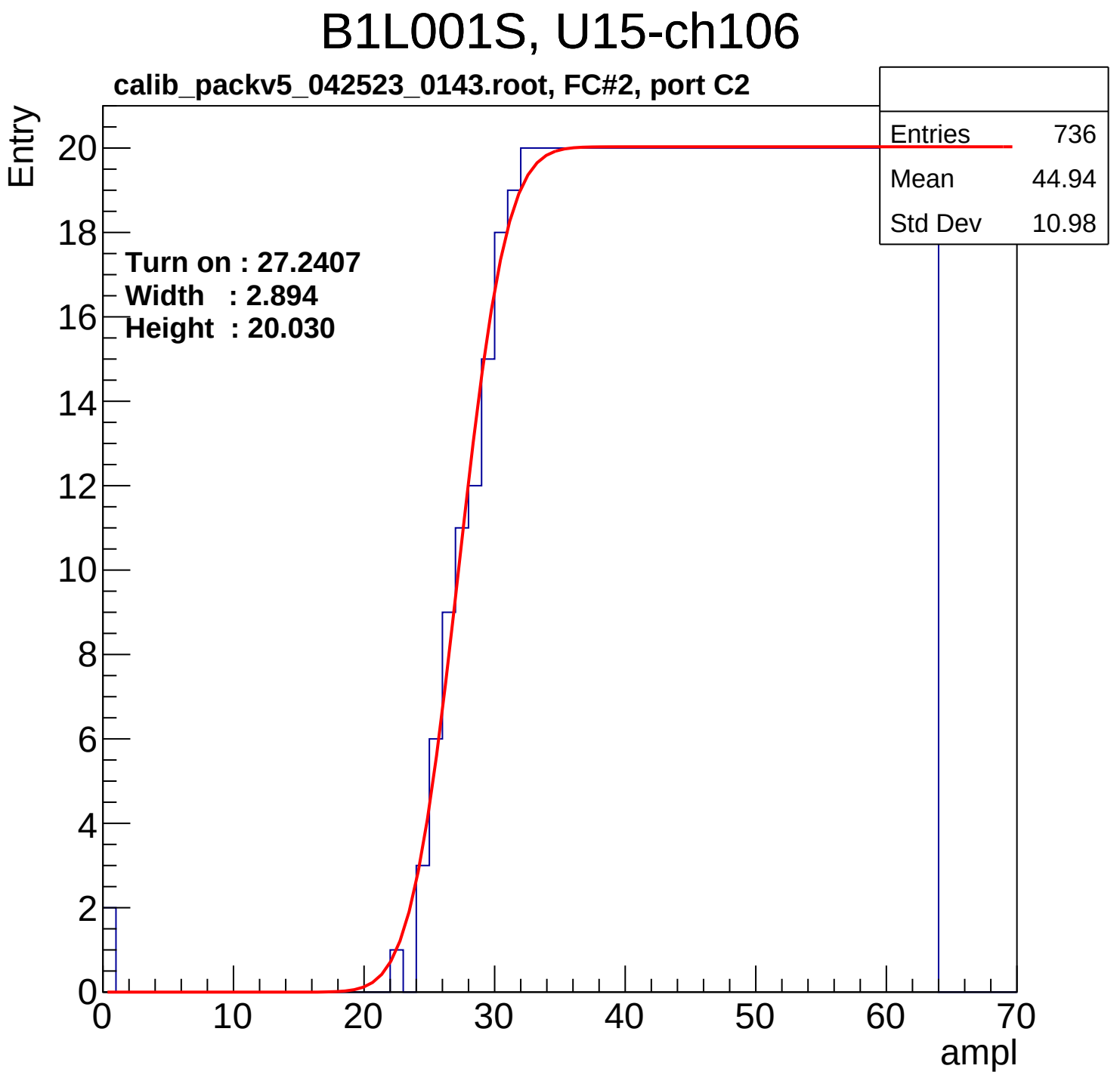
B1L001S, U15-ch106
calib_packv5_042523_0143.root, FC#2, port C2
Entries 736
Mean 44.94
Std Dev 10.98
Turn on : 27.2407
Width : 2.894
Height : 20.030
Entry
ampl
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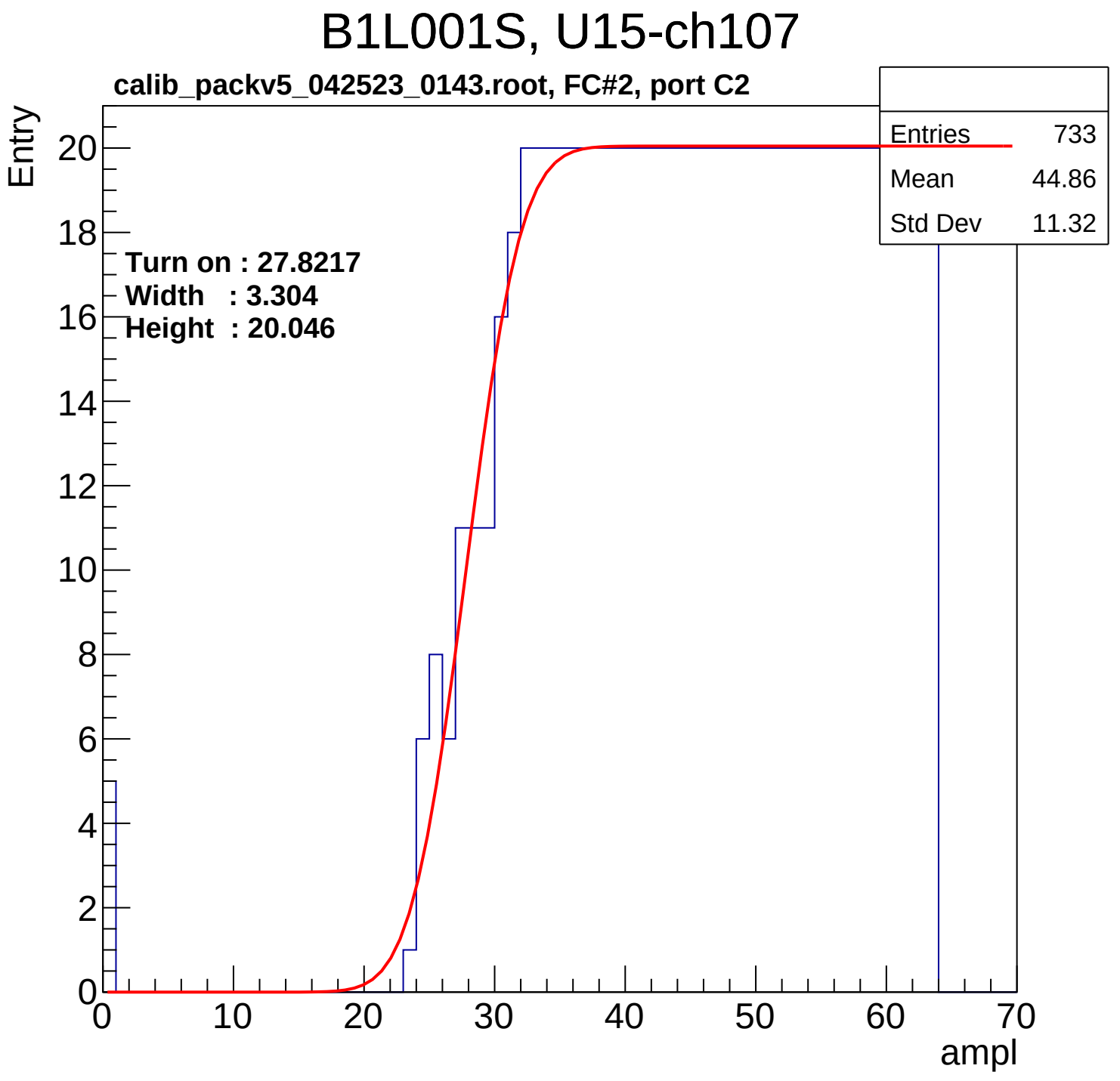
B1L001S, U15-ch107
calib_packv5_042523_0143.root, FC#2, port C2
Entries 733
Mean 44.86
Std Dev 11.32
Turn on : 27.8217
Width : 3.304
Height : 20.046
Entry
ampl
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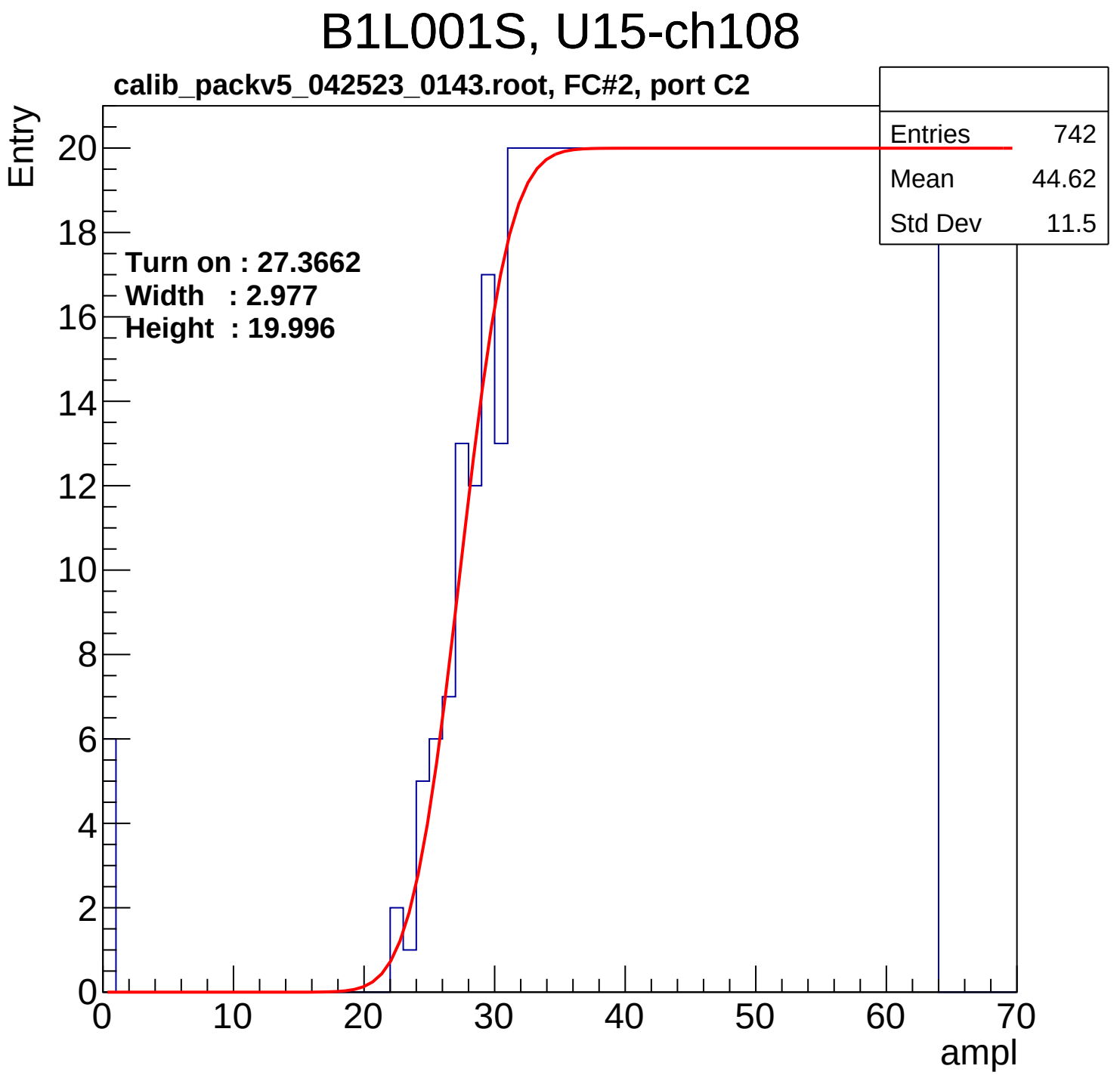
B1L001S, U15-ch108
calib_packv5_042523_0143.root, FC#2, port C2
Entries 742
Mean 44.62
Std Dev 11.5
Turn on : 27.3662
Width : 2.977
Height : 19.996
Entry
ampl
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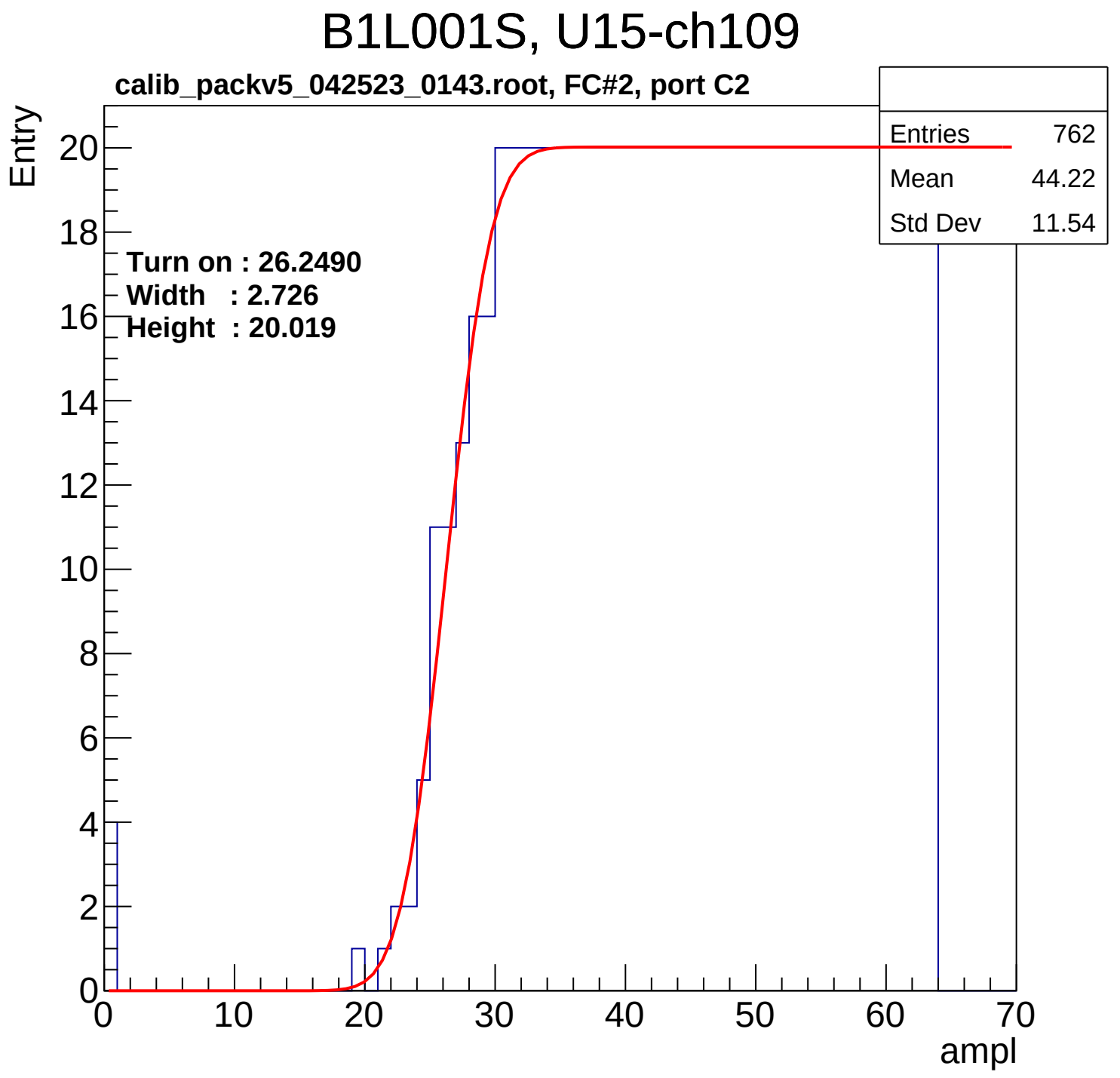
B1L001S, U15-ch109
calib_packv5_042523_0143.root, FC#2, port C2
Entries 762
Mean 44.22
Std Dev 11.54
Turn on : 26.2490
Width : 2.726
Height : 20.019
Entry
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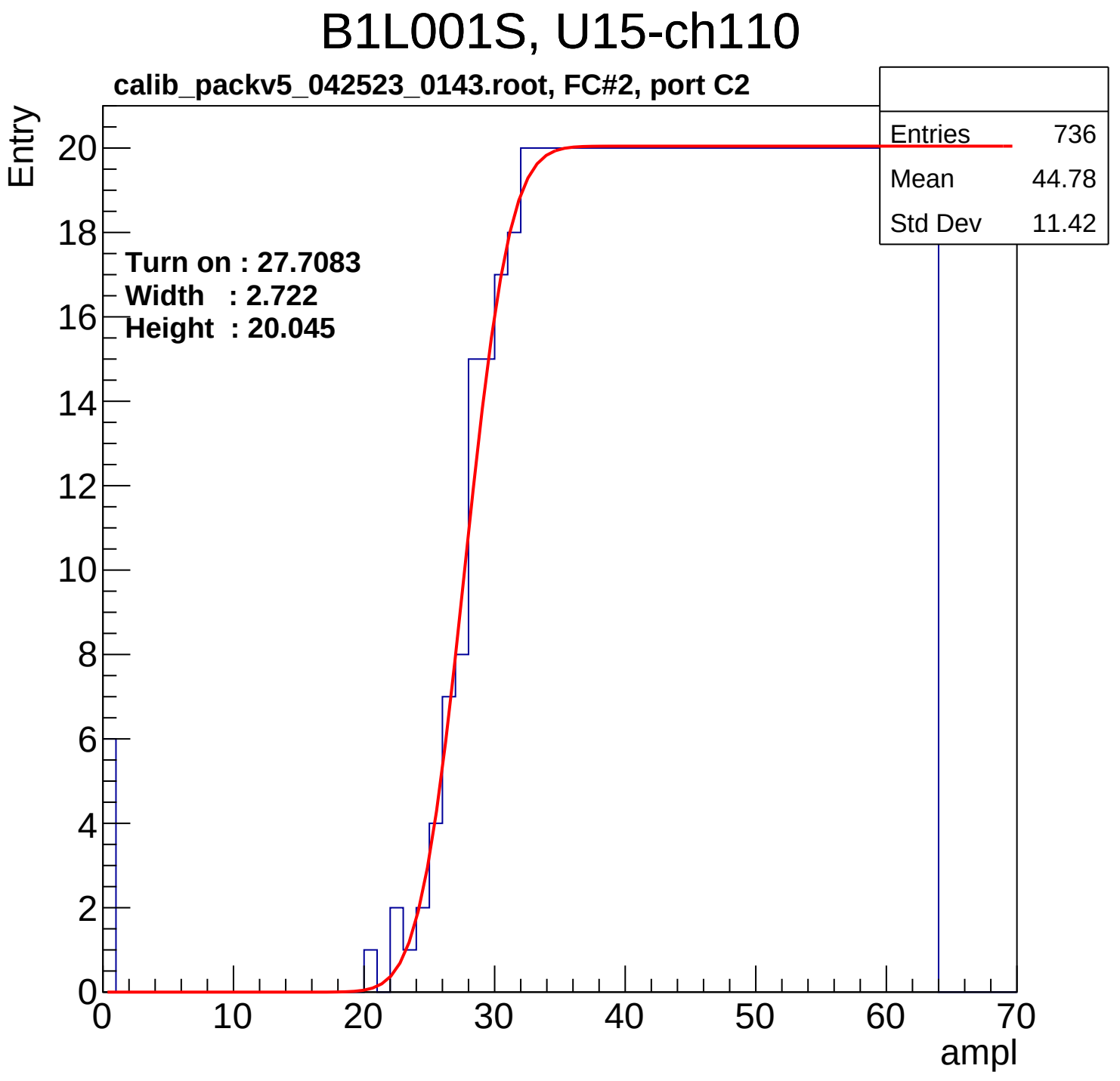
B1L001S, U15-ch110
calib_packv5_042523_0143.root, FC#2, port C2
Entries 736
Mean 44.78
Std Dev 11.42
Turn on : 27.7083
Width : 2.722
Height : 20.045
Entry
ampl
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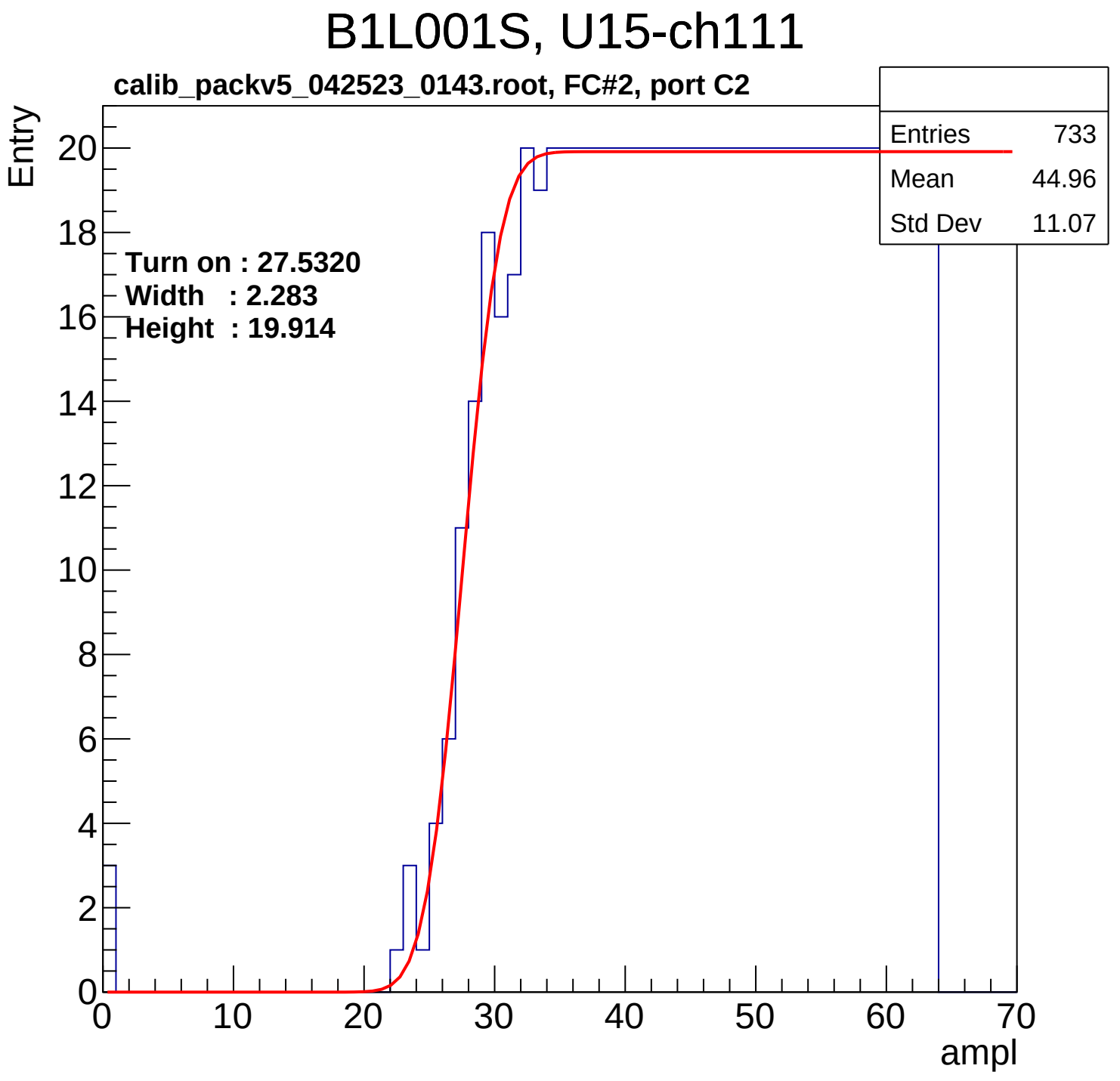
B1L001S, U15-ch111
calib_packv5_042523_0143.root, FC#2, port C2
Entries 733
Mean 44.96
Std Dev 11.07
Turn on : 27.5320
Width : 2.283
Height : 19.914
Entry
ampl
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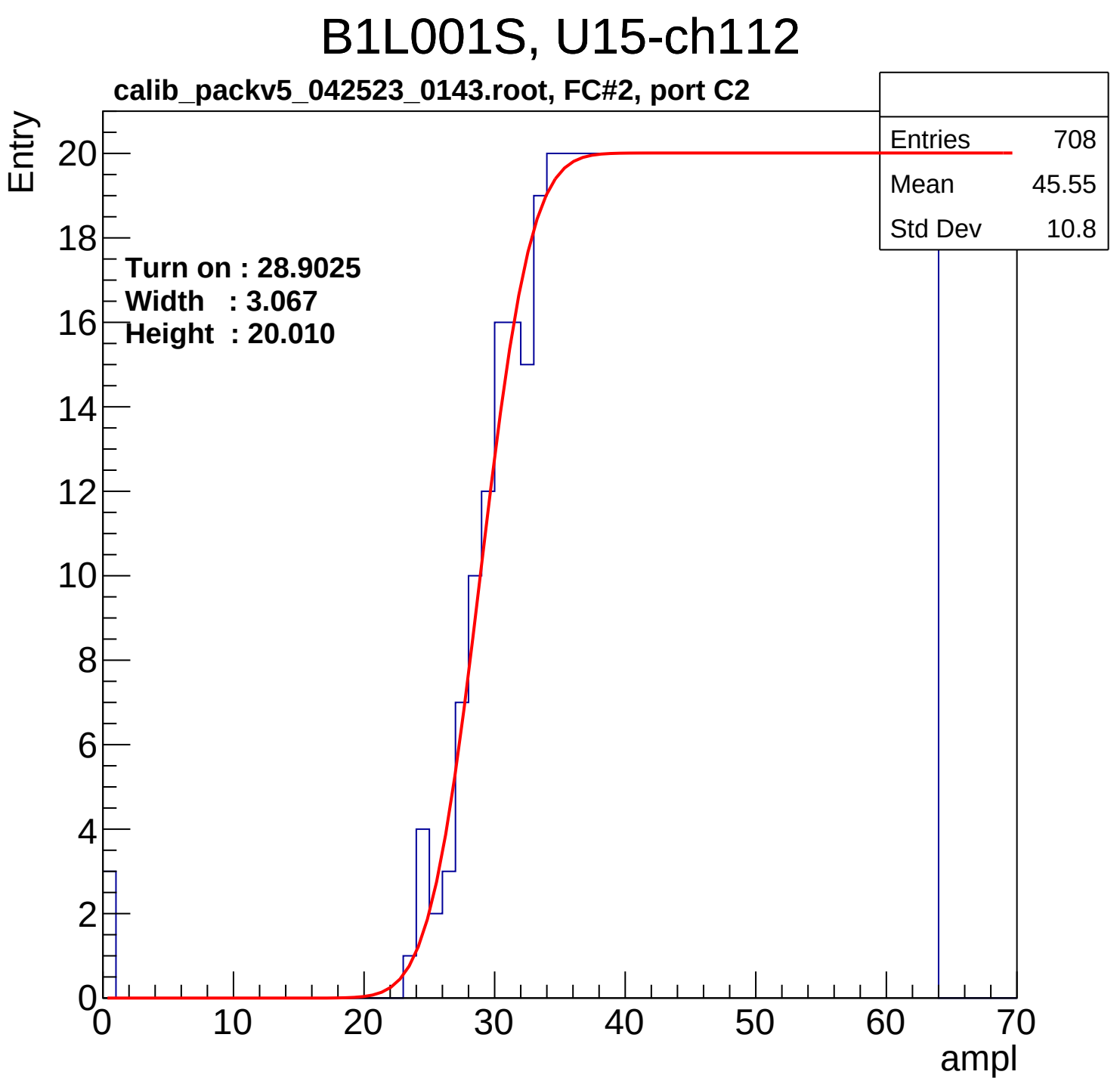
B1L001S, U15-ch112
calib_packv5_042523_0143.root, FC#2, port C2
Entries 708
Mean 45.55
Std Dev 10.8
Turn on : 28.9025
Width : 3.067
Height : 20.010
Entry
ampl
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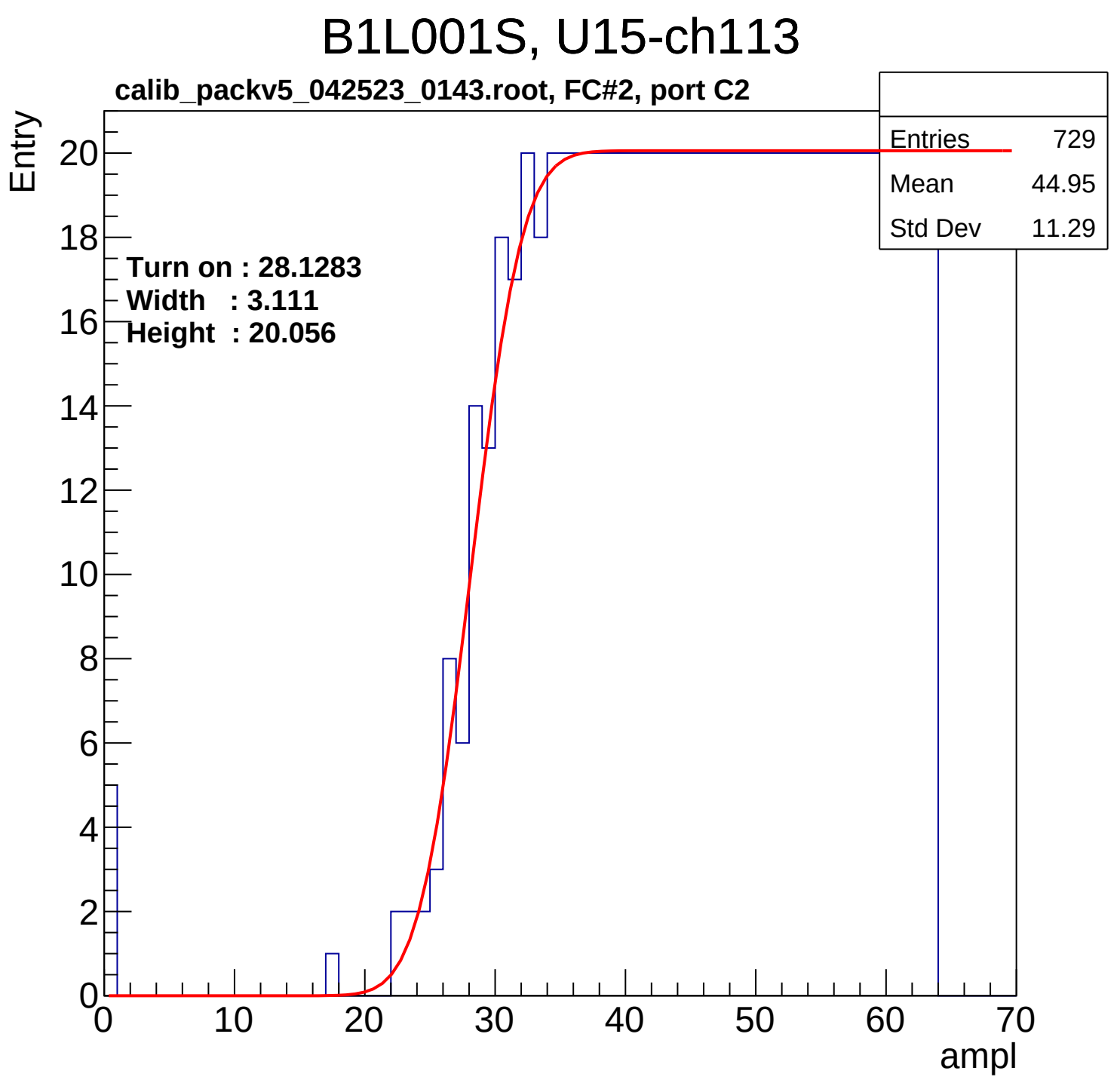
B1L001S, U15-ch113
calib_packv5_042523_0143.root, FC#2, port C2
Entries 729
Mean 44.95
Std Dev 11.29
Turn on : 28.1283
Width : 3.111
Height : 20.056
Entry
ampl
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6
8
10
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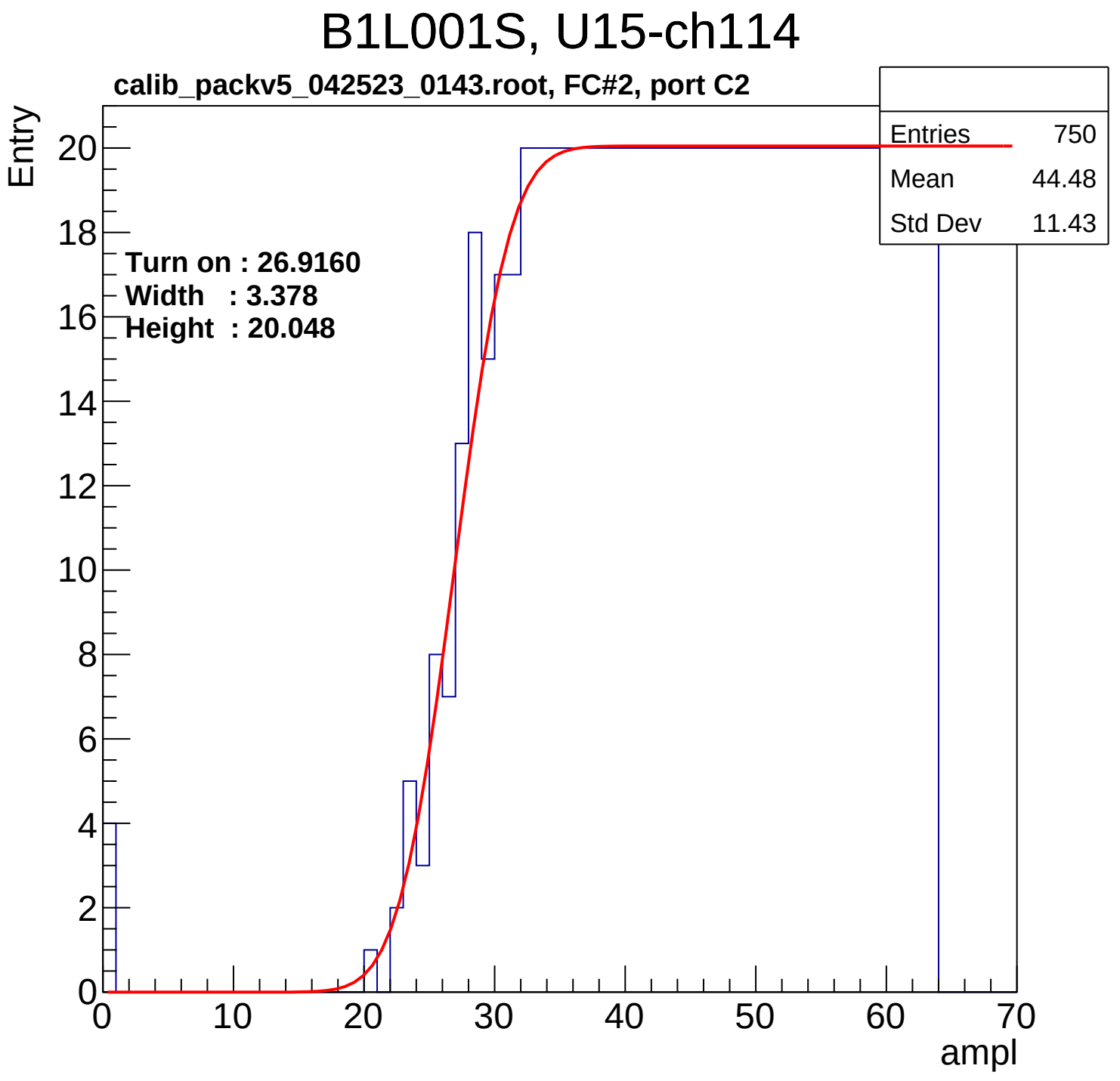
B1L001S, U15-ch114
calib_packv5_042523_0143.root, FC#2, port C2
Entries 750
Mean 44.48
Std Dev 11.43
Turn on : 26.9160
Width : 3.378
Height : 20.048
Entry
ampl
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6
8
10
12
14
16
18
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0
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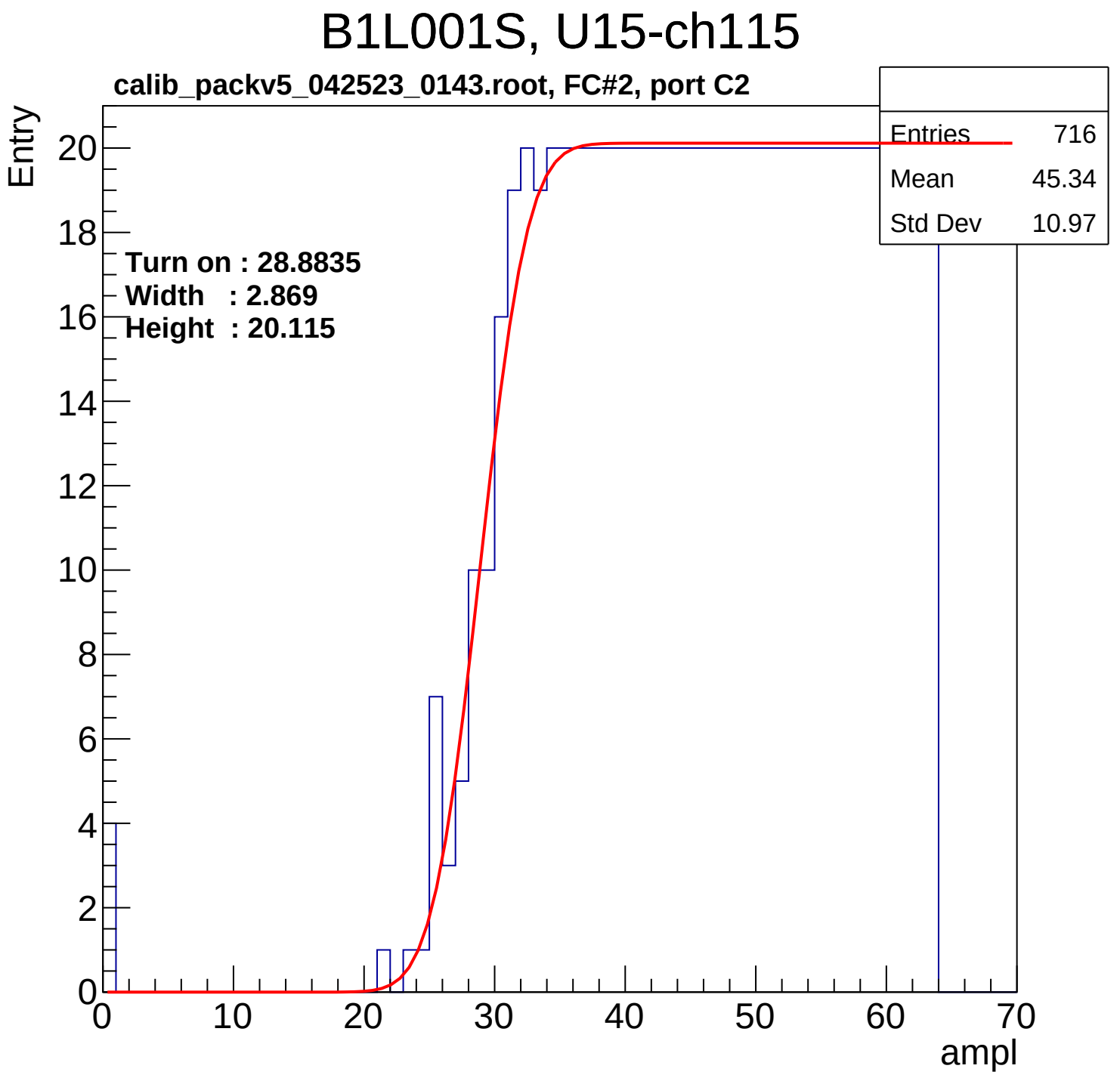
B1L001S, U15-ch115
calib_packv5_042523_0143.root, FC#2, port C2
Entries 716
Mean 45.34
Std Dev 10.97
Turn on : 28.8835
Width : 2.869
Height : 20.115
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
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20
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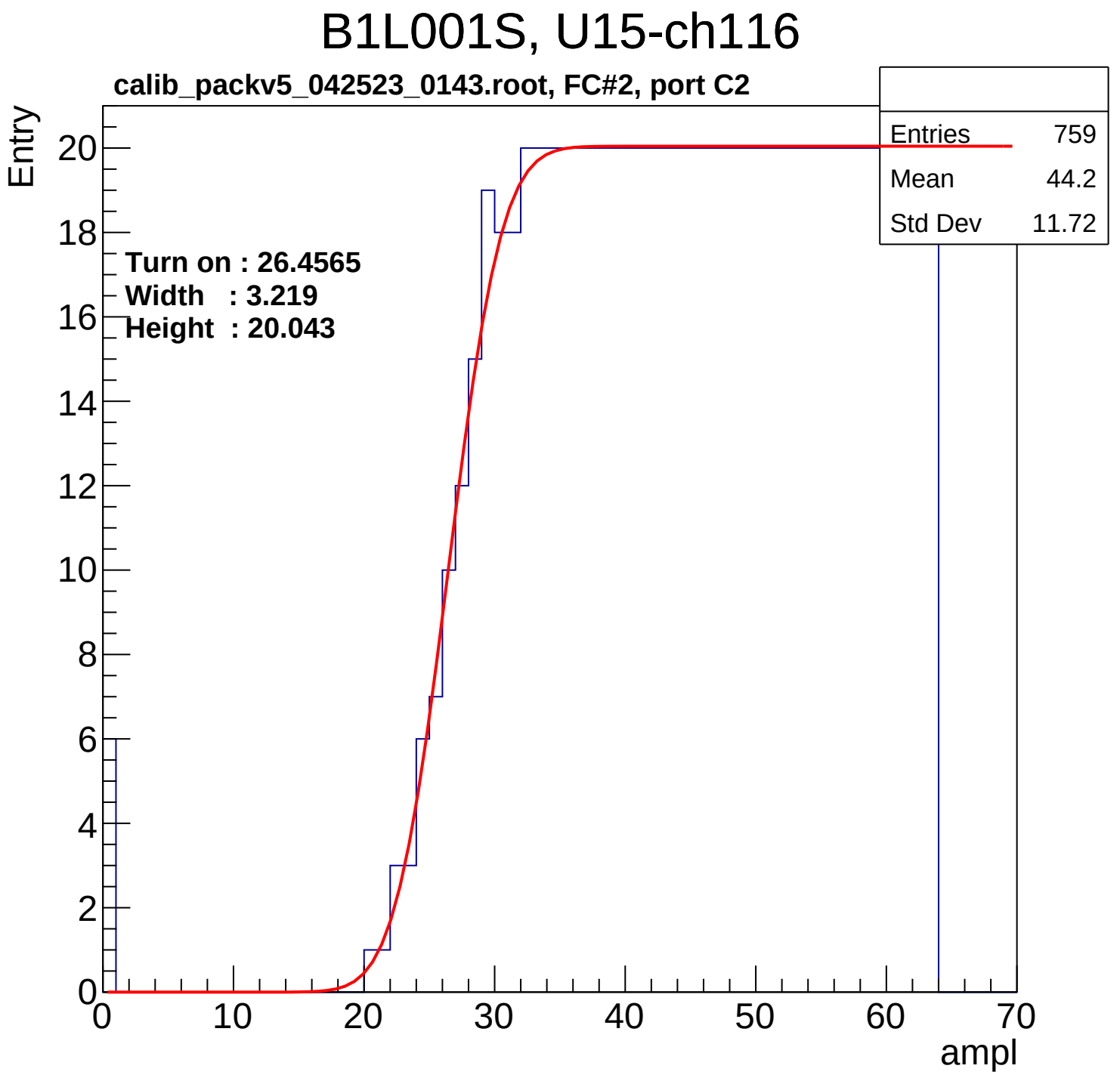
B1L001S, U15-ch116
calib_packv5_042523_0143.root, FC#2, port C2
Entries 759
Mean 44.2
Std Dev 11.72
Turn on : 26.4565
Width : 3.219
Height : 20.043
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
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40
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60
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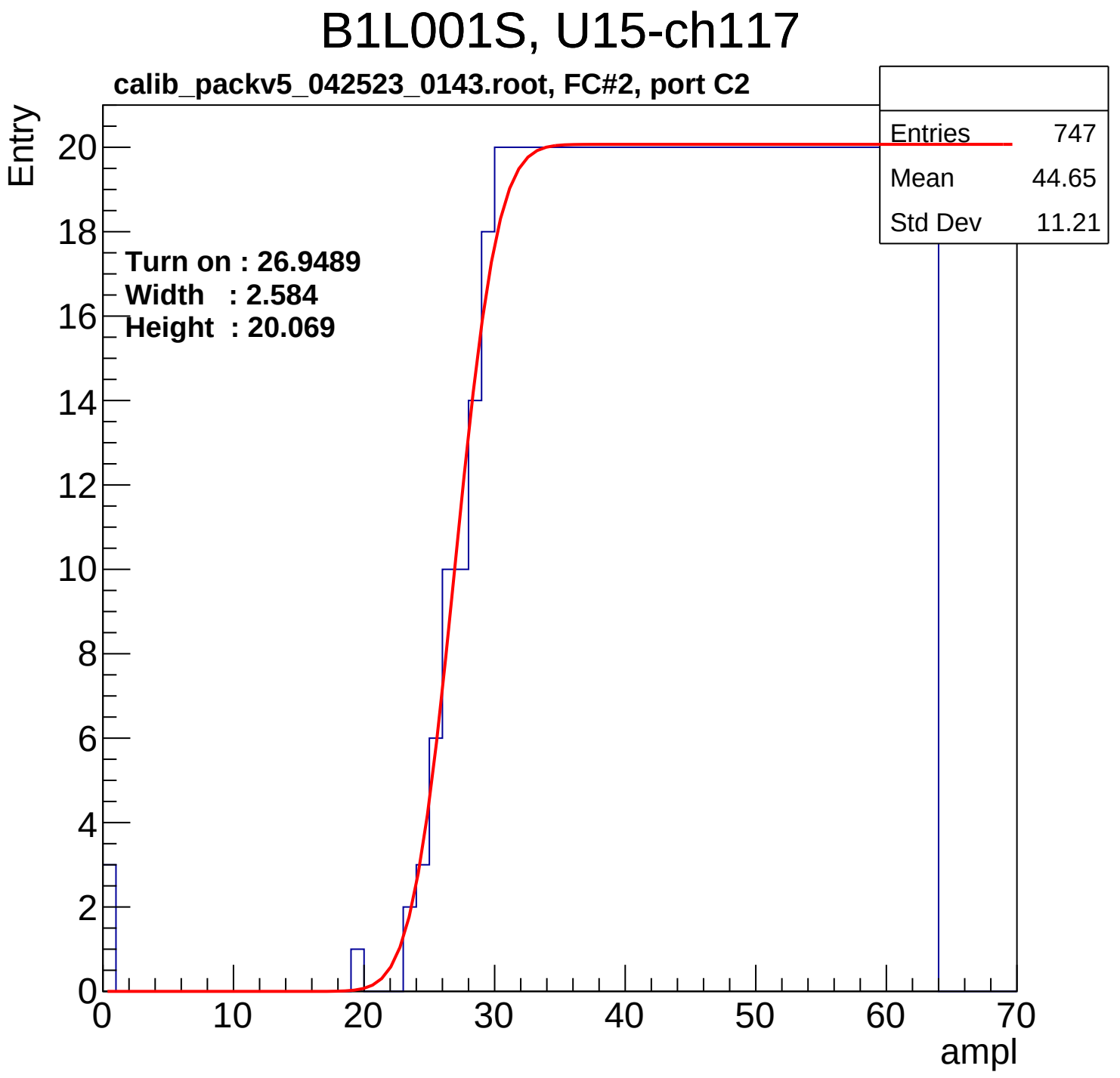
B1L001S, U15-ch117
calib_packv5_042523_0143.root, FC#2, port C2
Entries 747
Mean 44.65
Std Dev 11.21
Turn on : 26.9489
Width : 2.584
Height : 20.069
Entry
ampl
0
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6
8
10
12
14
16
18
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0
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20
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60
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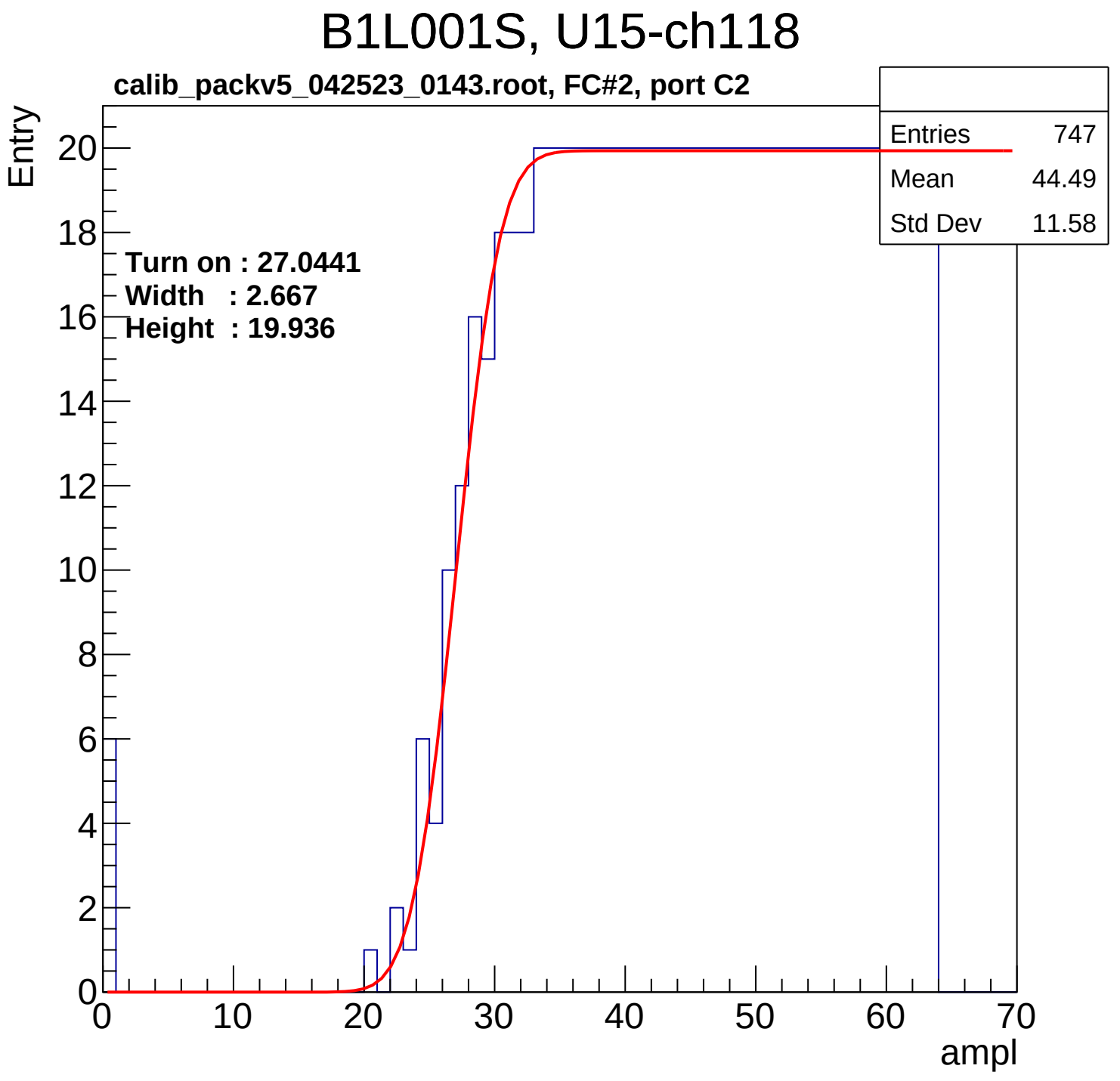
B1L001S, U15-ch118
calib_packv5_042523_0143.root, FC#2, port C2
Entries 747
Mean 44.49
Std Dev 11.58
Turn on : 27.0441
Width : 2.667
Height : 19.936
Entry
ampl
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6
8
10
12
14
16
18
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0
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20
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60
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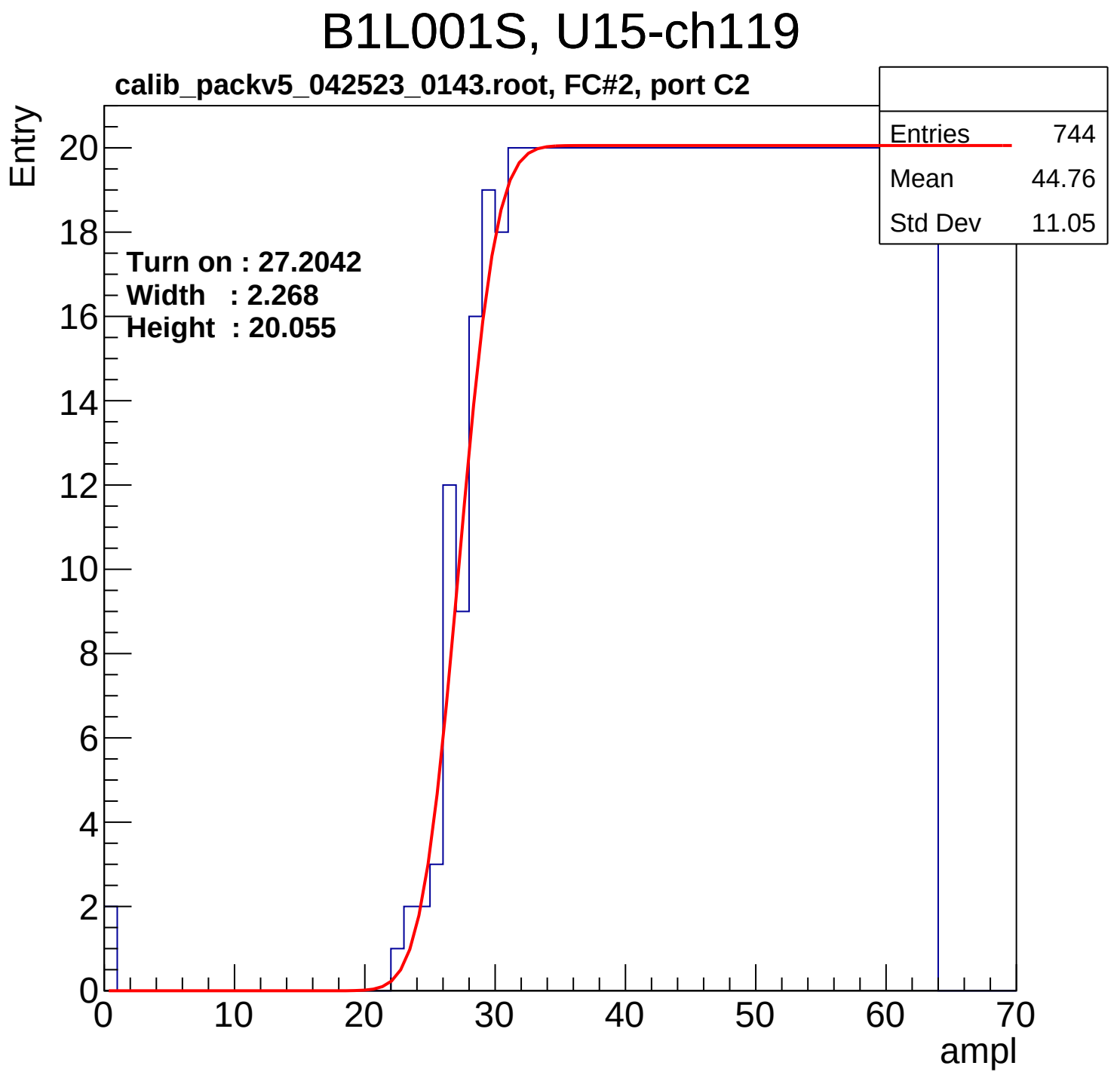
B1L001S, U15-ch119
calib_packv5_042523_0143.root, FC#2, port C2
Entries 744
Mean 44.76
Std Dev 11.05
Turn on : 27.2042
Width : 2.268
Height : 20.055
Entry
ampl
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6
8
10
12
14
16
18
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0
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20
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40
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60
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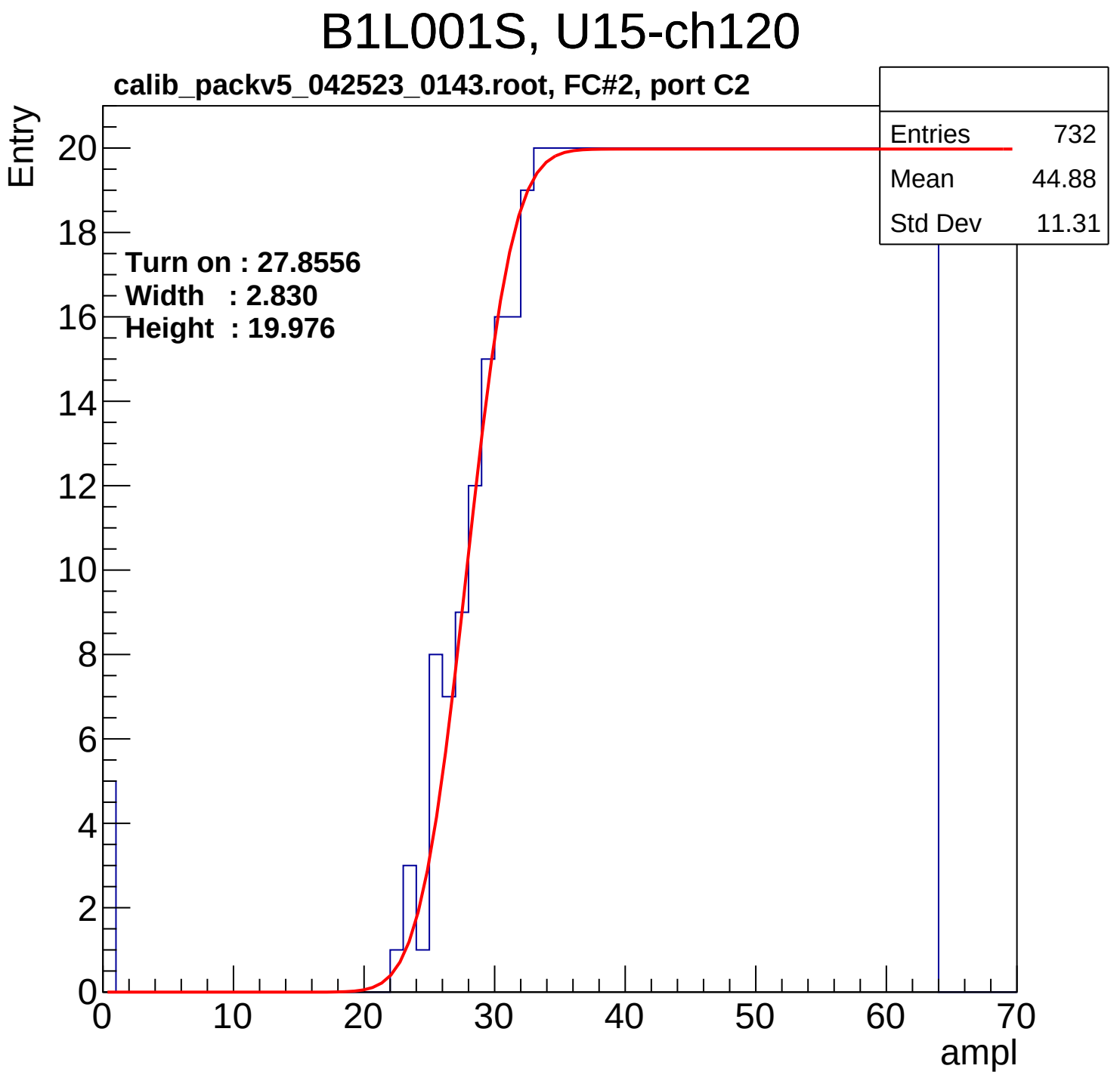
B1L001S, U15-ch120
calib_packv5_042523_0143.root, FC#2, port C2
Entries 732
Mean 44.88
Std Dev 11.31
Turn on : 27.8556
Width : 2.830
Height : 19.976
Entry
ampl
0
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4
6
8
10
12
14
16
18
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0
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20
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40
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60
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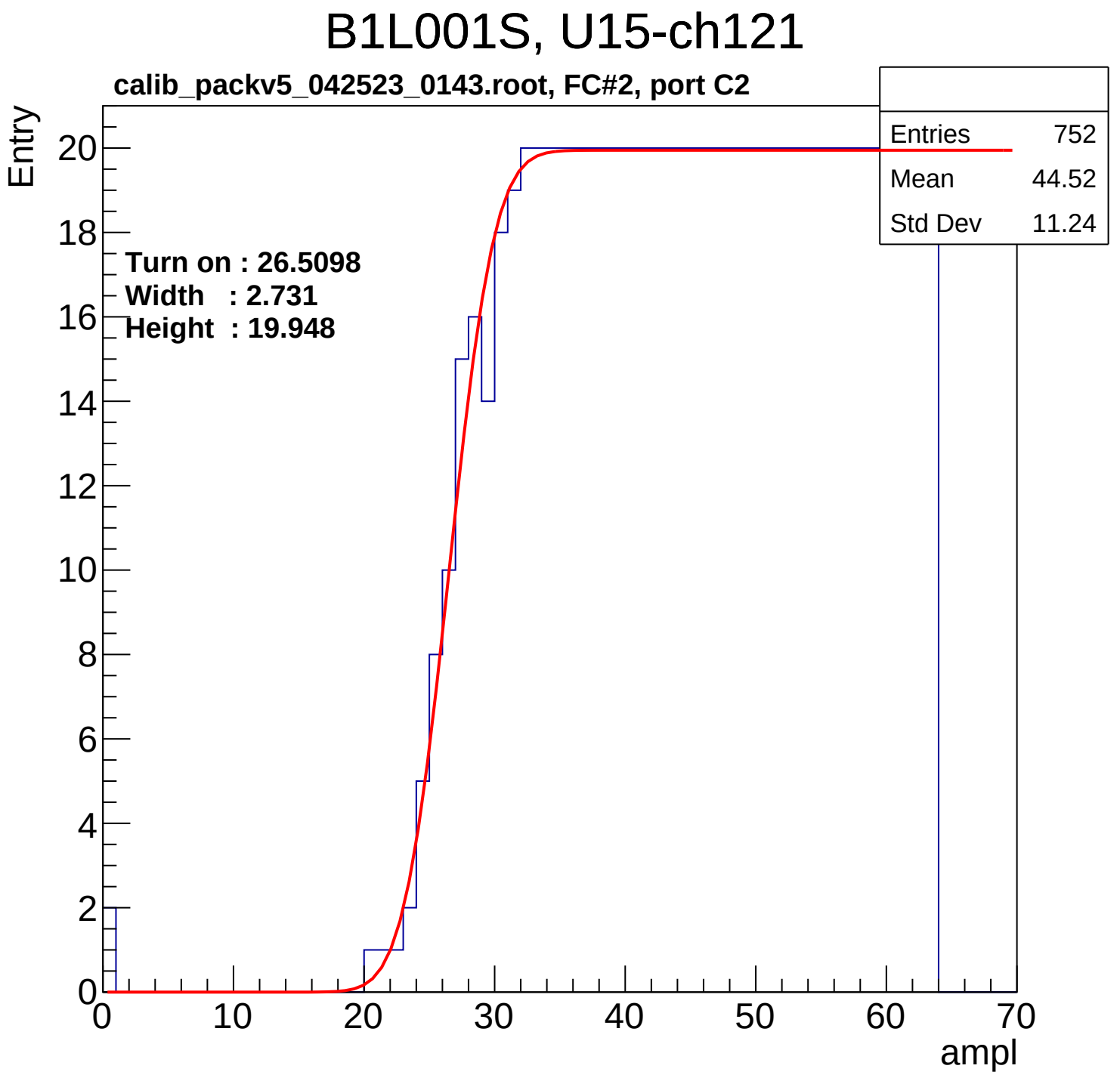
B1L001S, U15-ch121
calib_packv5_042523_0143.root, FC#2, port C2
Entries 752
Mean 44.52
Std Dev 11.24
Turn on : 26.5098
Width : 2.731
Height : 19.948
Entry
ampl
0
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4
6
8
10
12
14
16
18
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0
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20
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40
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60
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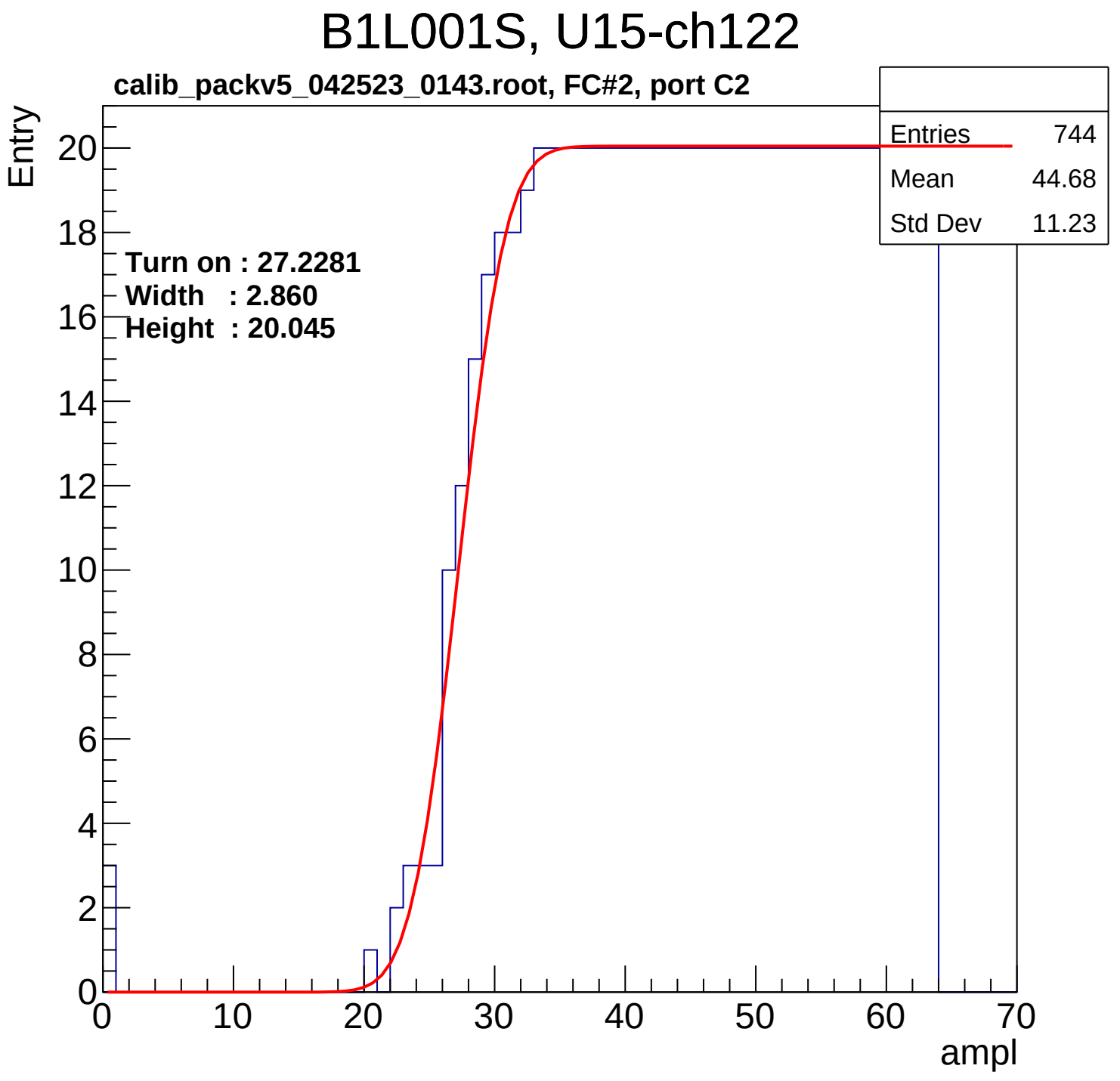
B1L001S, U15-ch122
calib_packv5_042523_0143.root, FC#2, port C2
Entries 744
Mean 44.68
Std Dev 11.23
Turn on : 27.2281
Width : 2.860
Height : 20.045
Entry
ampl
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6
8
10
12
14
16
18
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0
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20
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60
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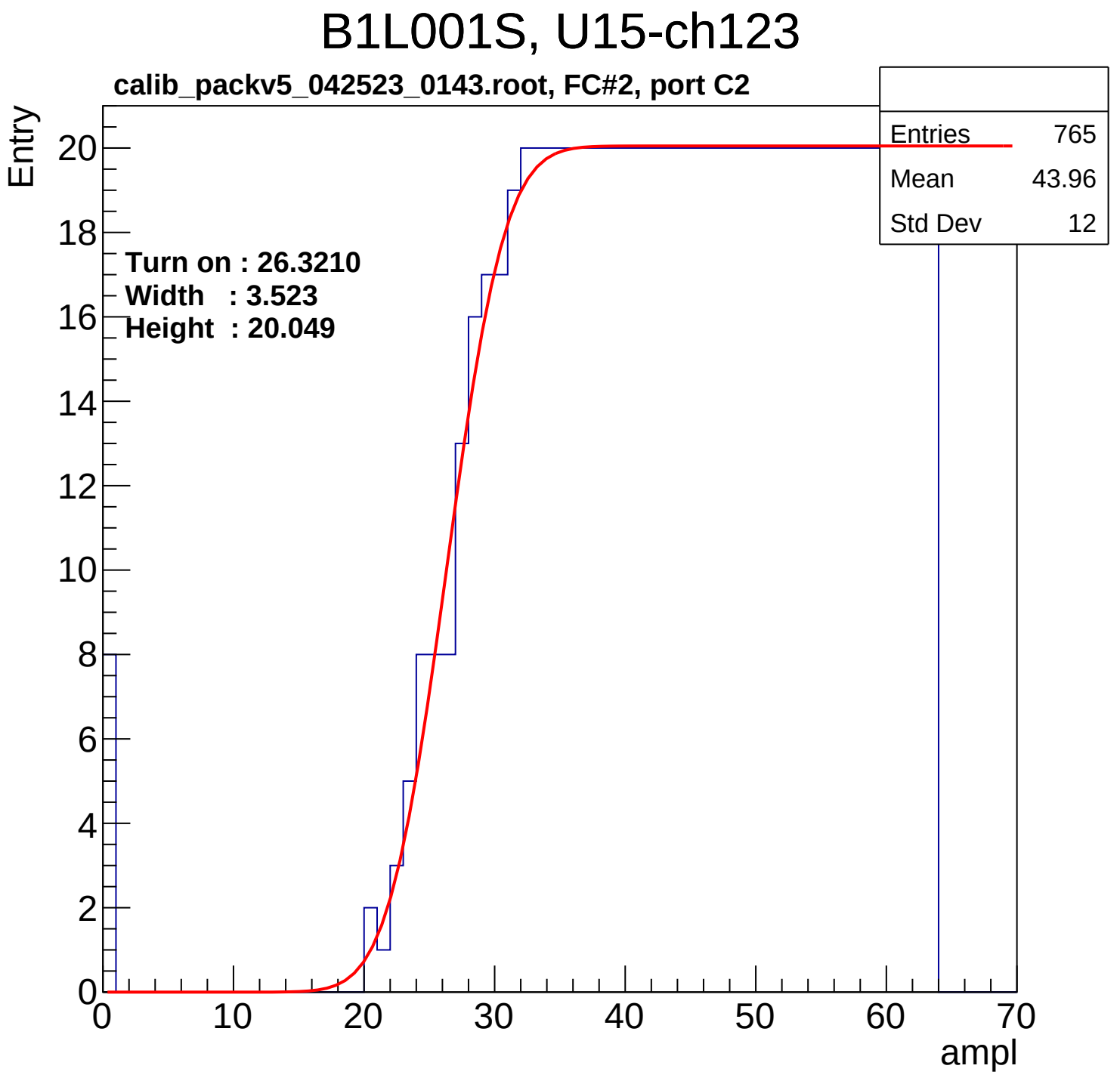
B1L001S, U15-ch123
calib_packv5_042523_0143.root, FC#2, port C2
Entries 765
Mean 43.96
Std Dev 12
Turn on : 26.3210
Width : 3.523
Height : 20.049
Entry
ampl
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6
8
10
12
14
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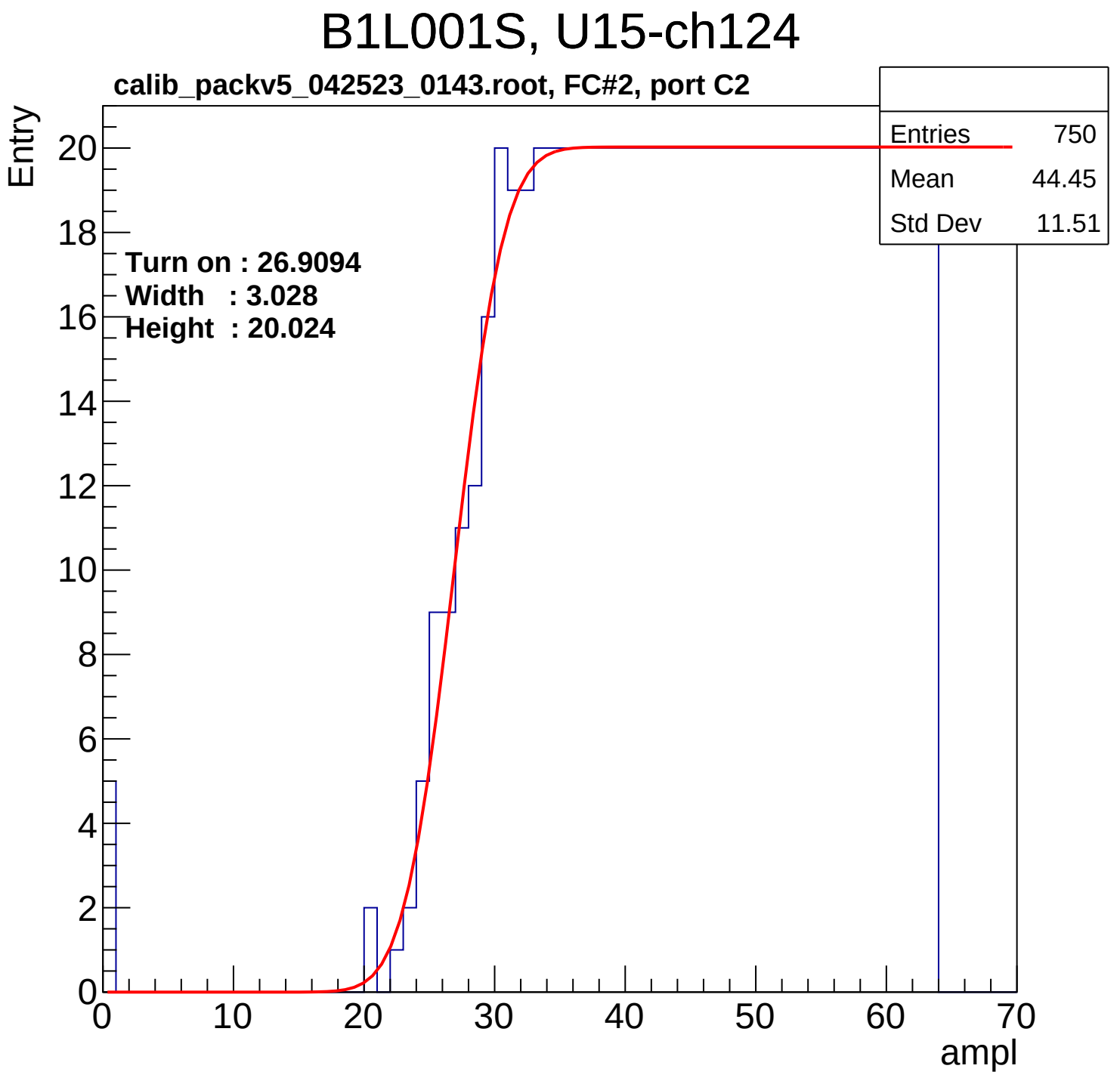
B1L001S, U15-ch124
calib_packv5_042523_0143.root, FC#2, port C2
Entries 750
Mean 44.45
Std Dev 11.51
Turn on : 26.9094
Width : 3.028
Height : 20.024
Entry
ampl
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6
8
10
12
14
16
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20
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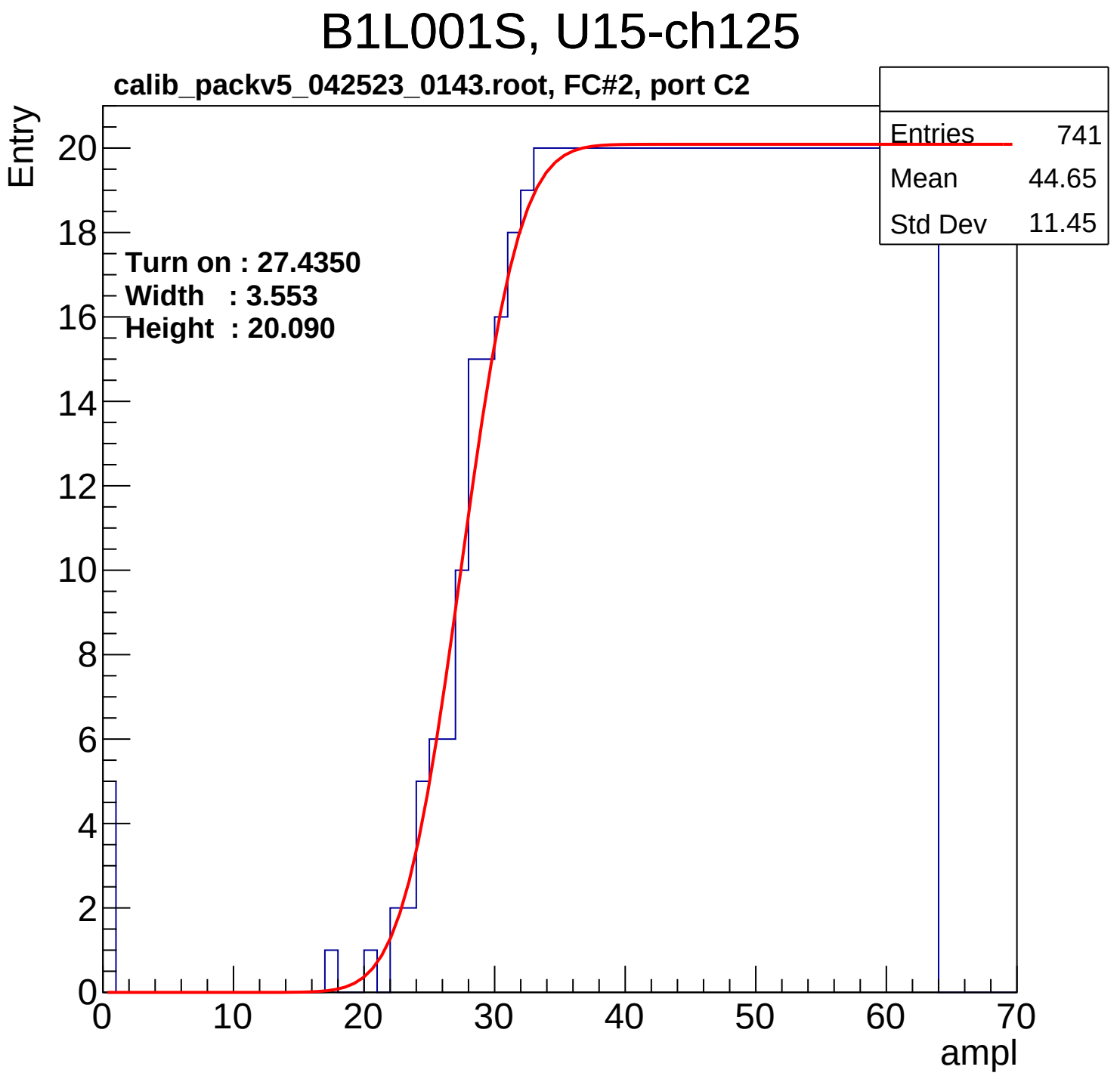
B1L001S, U15-ch125
calib_packv5_042523_0143.root, FC#2, port C2
Entries 741
Mean 44.65
Std Dev 11.45
Turn on : 27.4350
Width : 3.553
Height : 20.090
Entry
ampl
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6
8
10
12
14
16
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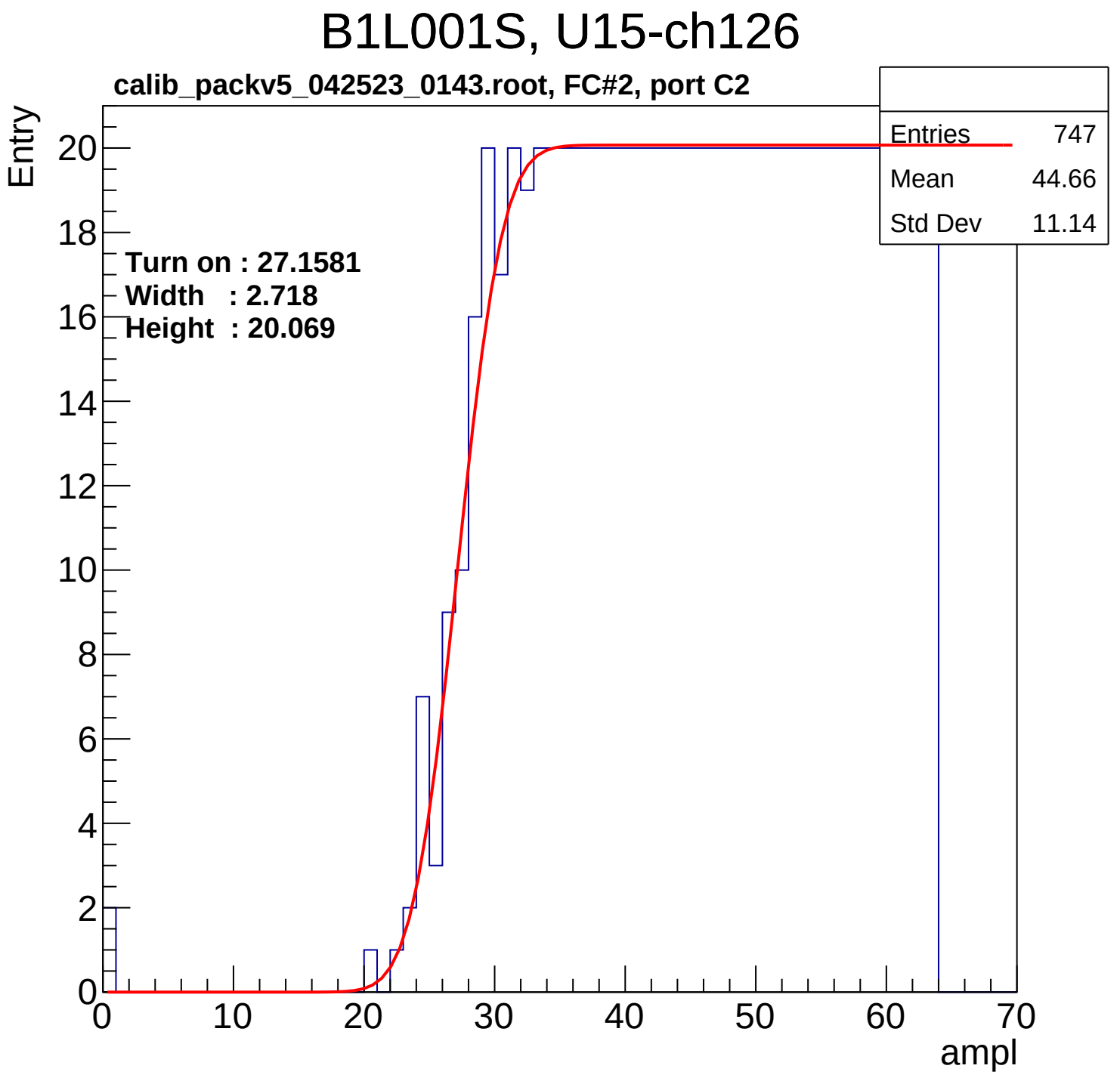
B1L001S, U15-ch126
calib_packv5_042523_0143.root, FC#2, port C2
Entries 747
Mean 44.66
Std Dev 11.14
Turn on : 27.1581
Width : 2.718
Height : 20.069
Entry
ampl
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8
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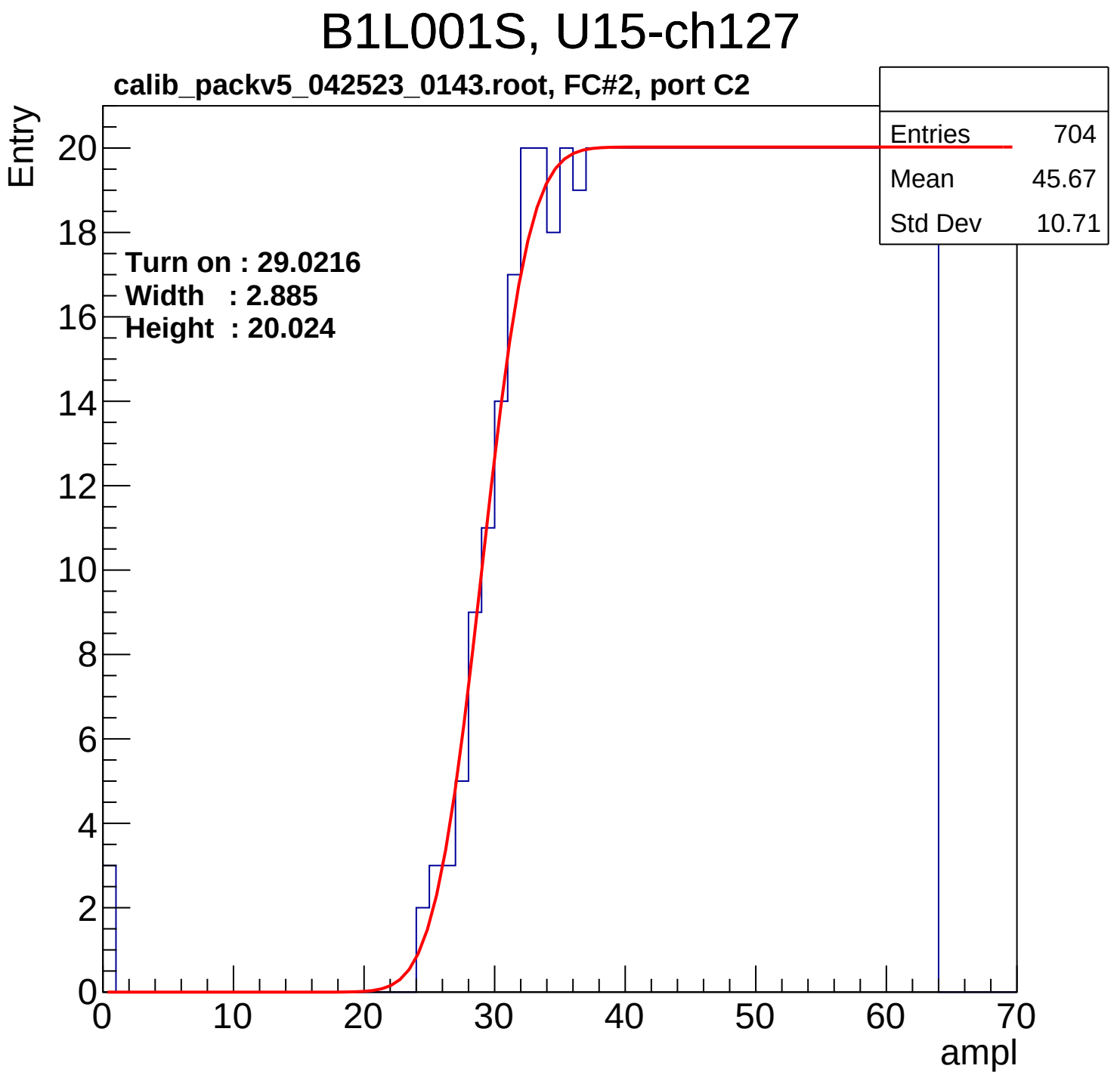
B1L001S, U15-ch127
calib_packv5_042523_0143.root, FC#2, port C2
Entries 704
Mean 45.67
Std Dev 10.71
Turn on : 29.0216
Width : 2.885
Height : 20.024
Entry
ampl
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8
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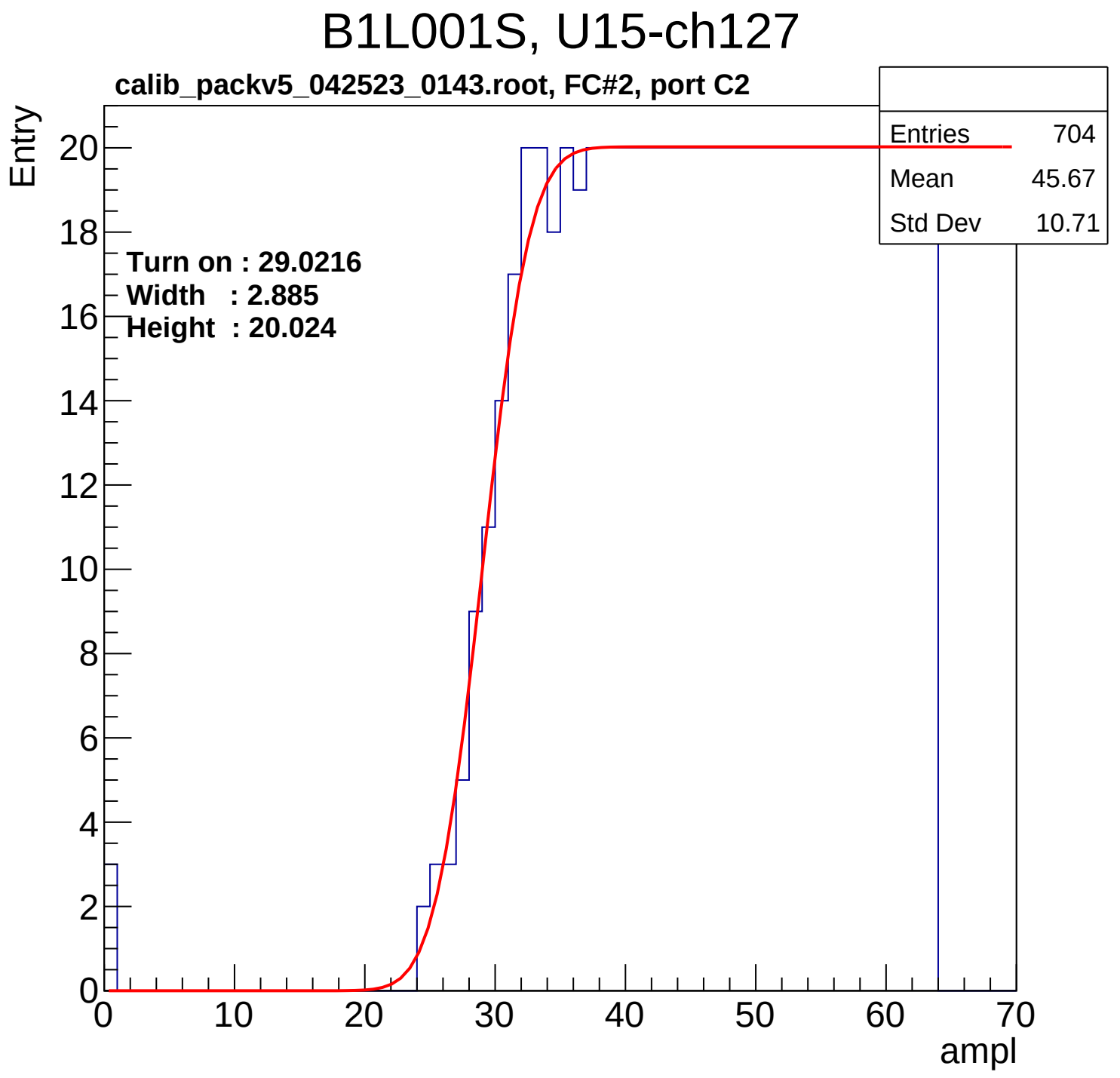
B1L001S, U15-ch127
calib_packv5_042523_0143.root, FC#2, port C2
Entries 704
Mean 45.67
Std Dev 10.71
Turn on : 29.0216
Width : 2.885
Height : 20.024
Entry
ampl
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8
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