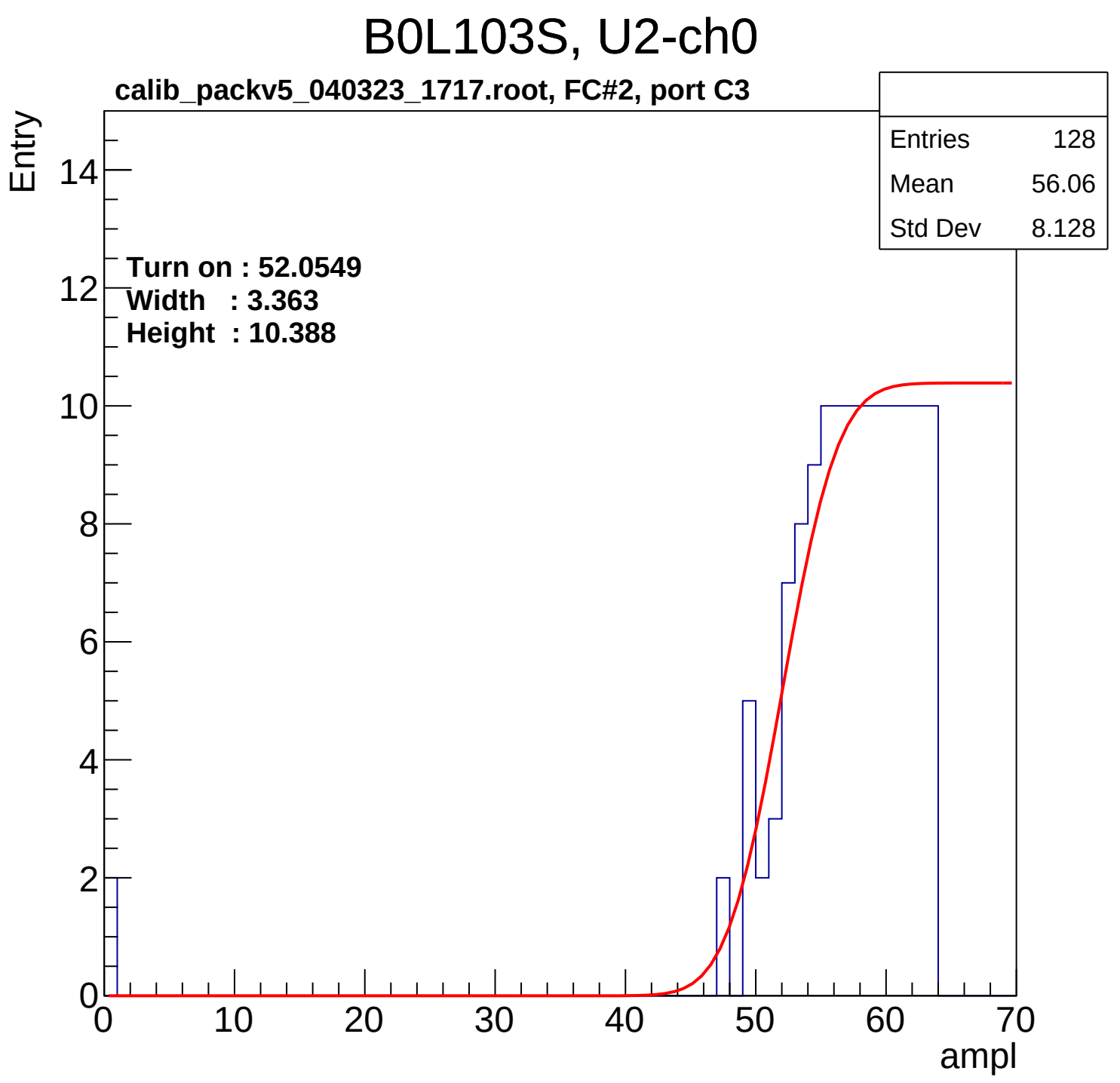
B0L103S, U2-ch0
calib_packv5_040323_1717.root, FC#2, port C3
Entries 128
Mean 56.06
Std Dev 8.128
Turn on : 52.0549
Width : 3.363
Height : 10.388
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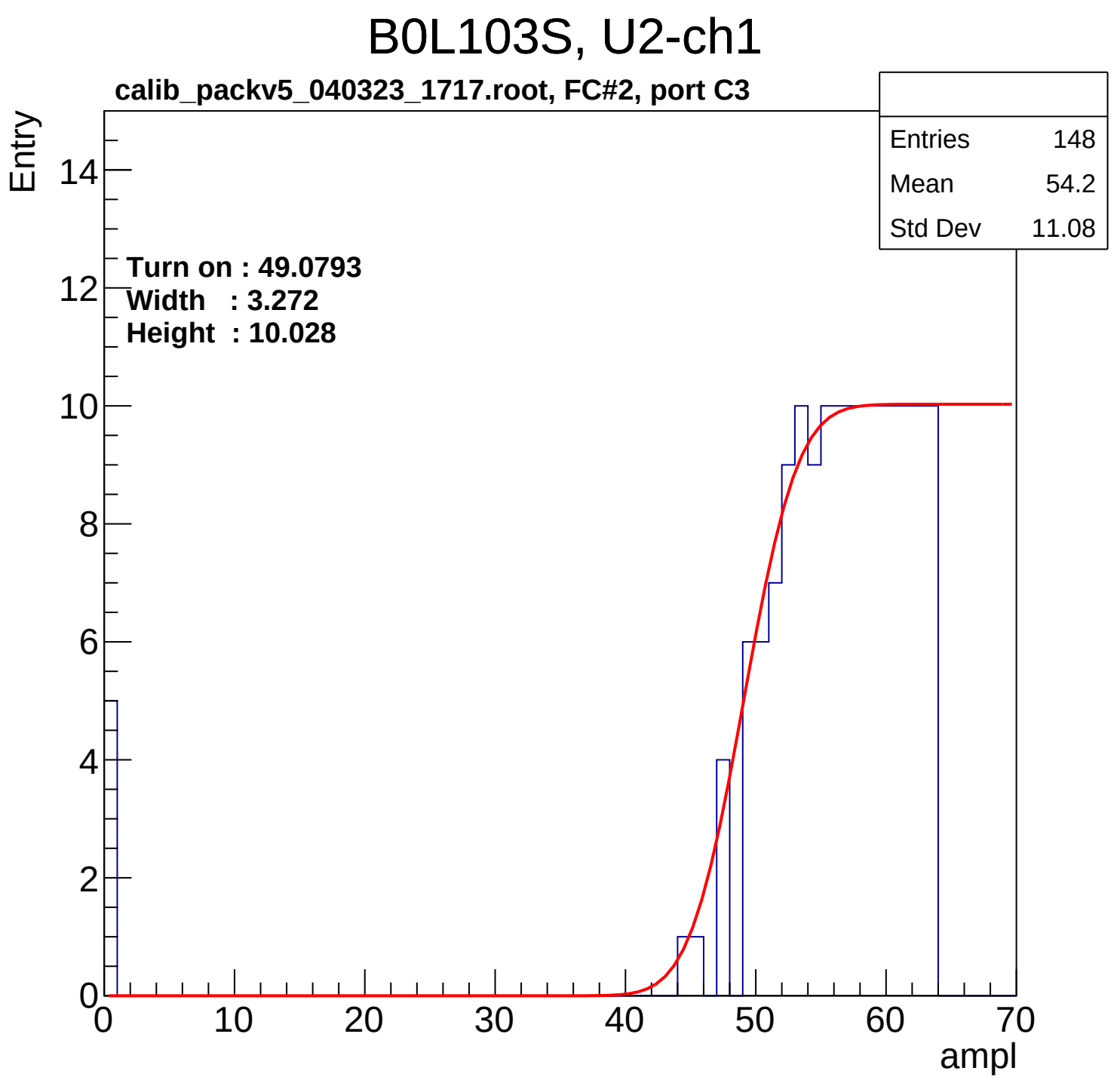
B0L103S, U2-ch1
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 54.2
Std Dev 11.08
Turn on : 49.0793
Width : 3.272
Height : 10.028
Entry
ampl
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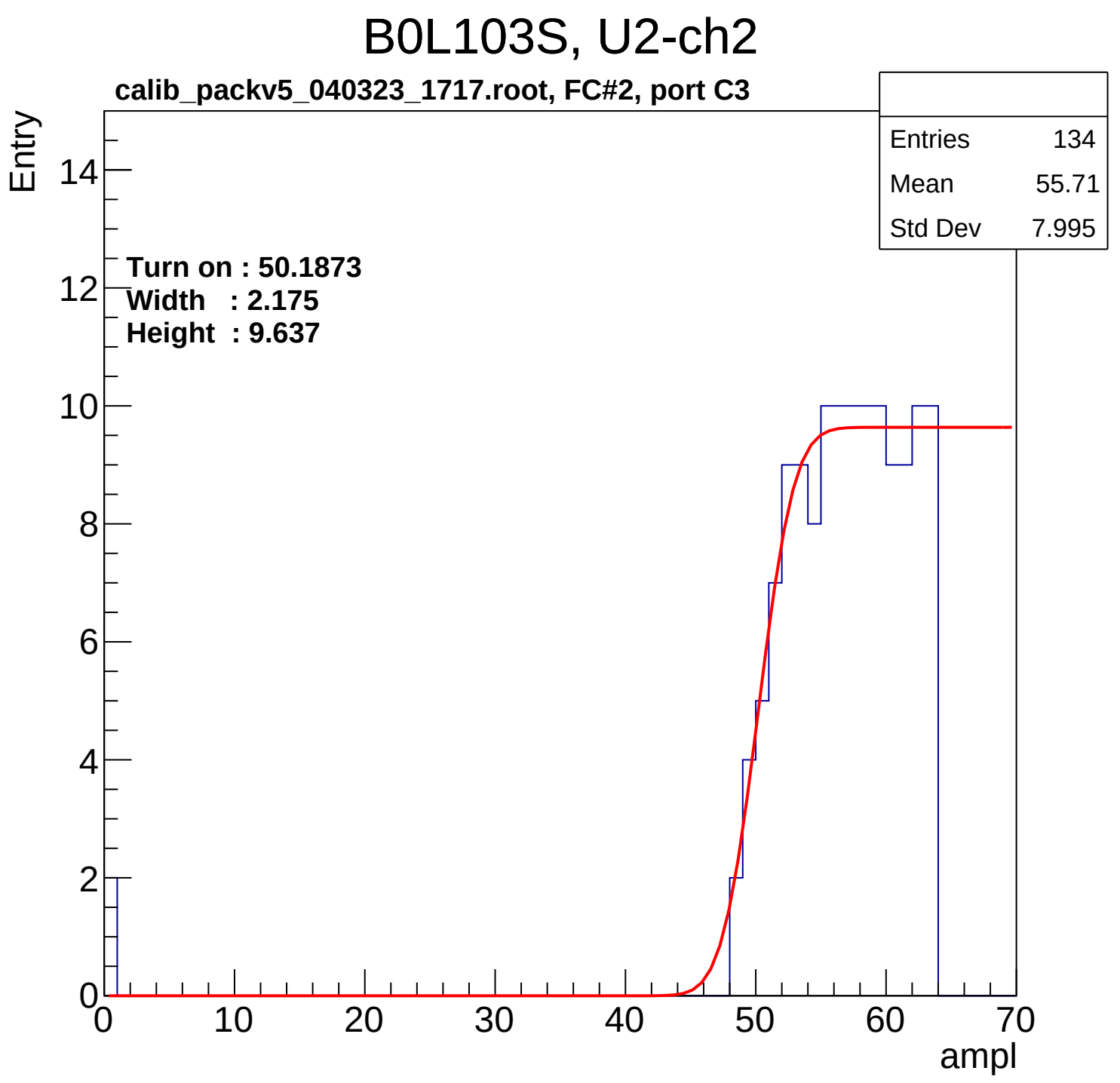
B0L103S, U2-ch2
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 55.71
Std Dev 7.995
Turn on : 50.1873
Width : 2.175
Height : 9.637
Entry
ampl
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6
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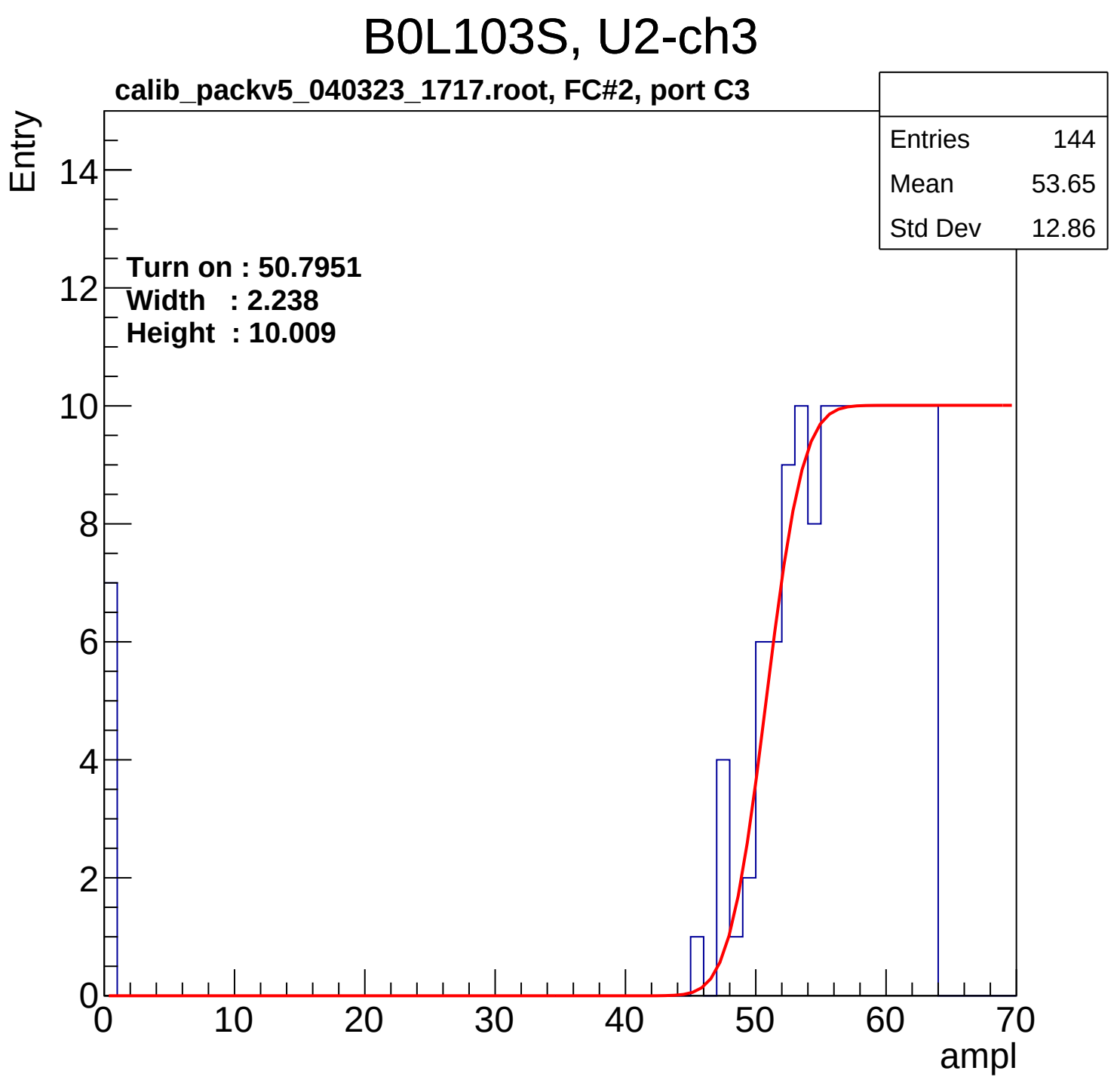
B0L103S, U2-ch3
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 53.65
Std Dev 12.86
Turn on : 50.7951
Width : 2.238
Height : 10.009
Entry
ampl
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2
4
6
8
10
12
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0
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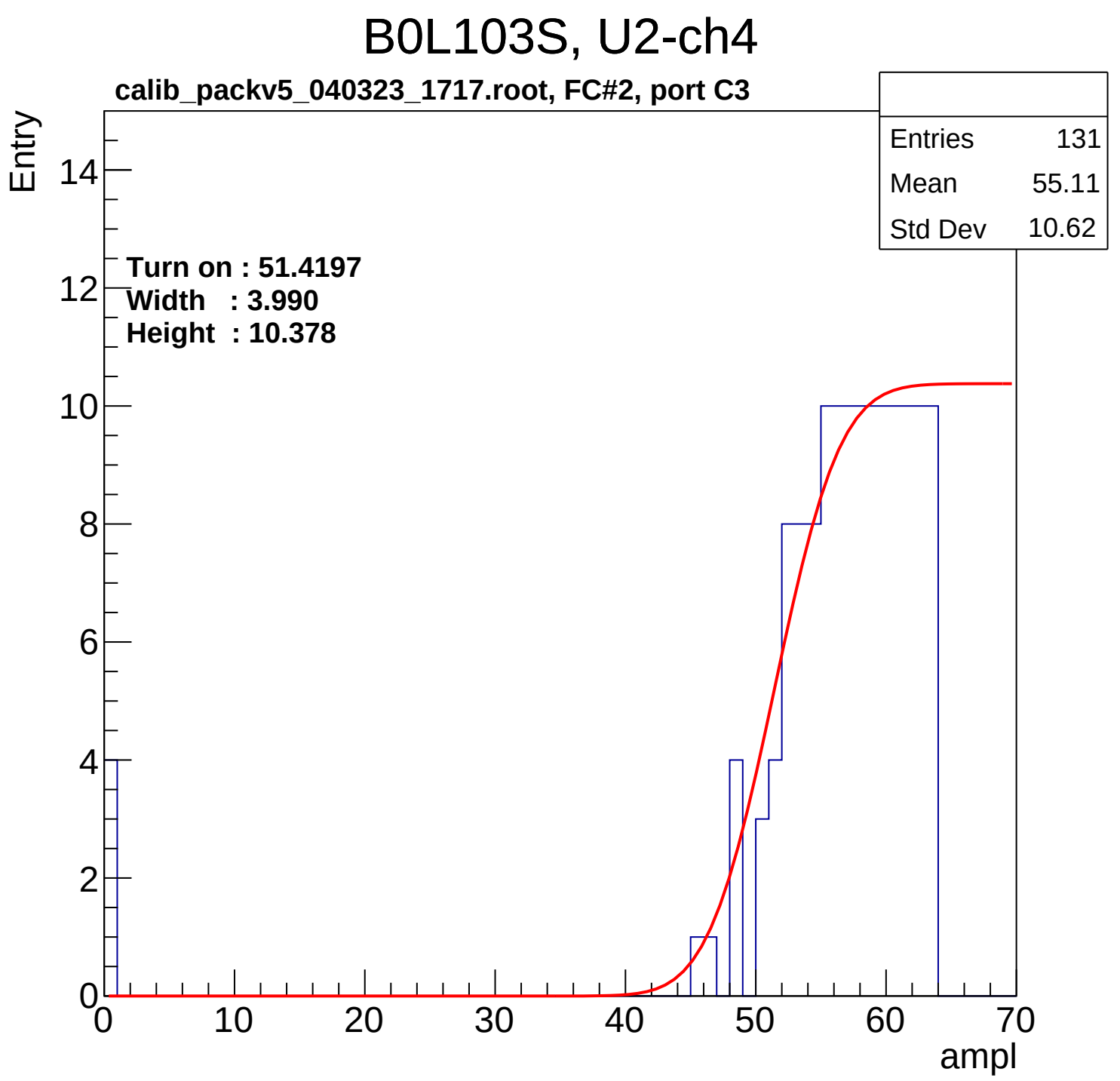
B0L103S, U2-ch4
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 55.11
Std Dev 10.62
Turn on : 51.4197
Width : 3.990
Height : 10.378
Entry
ampl
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6
8
10
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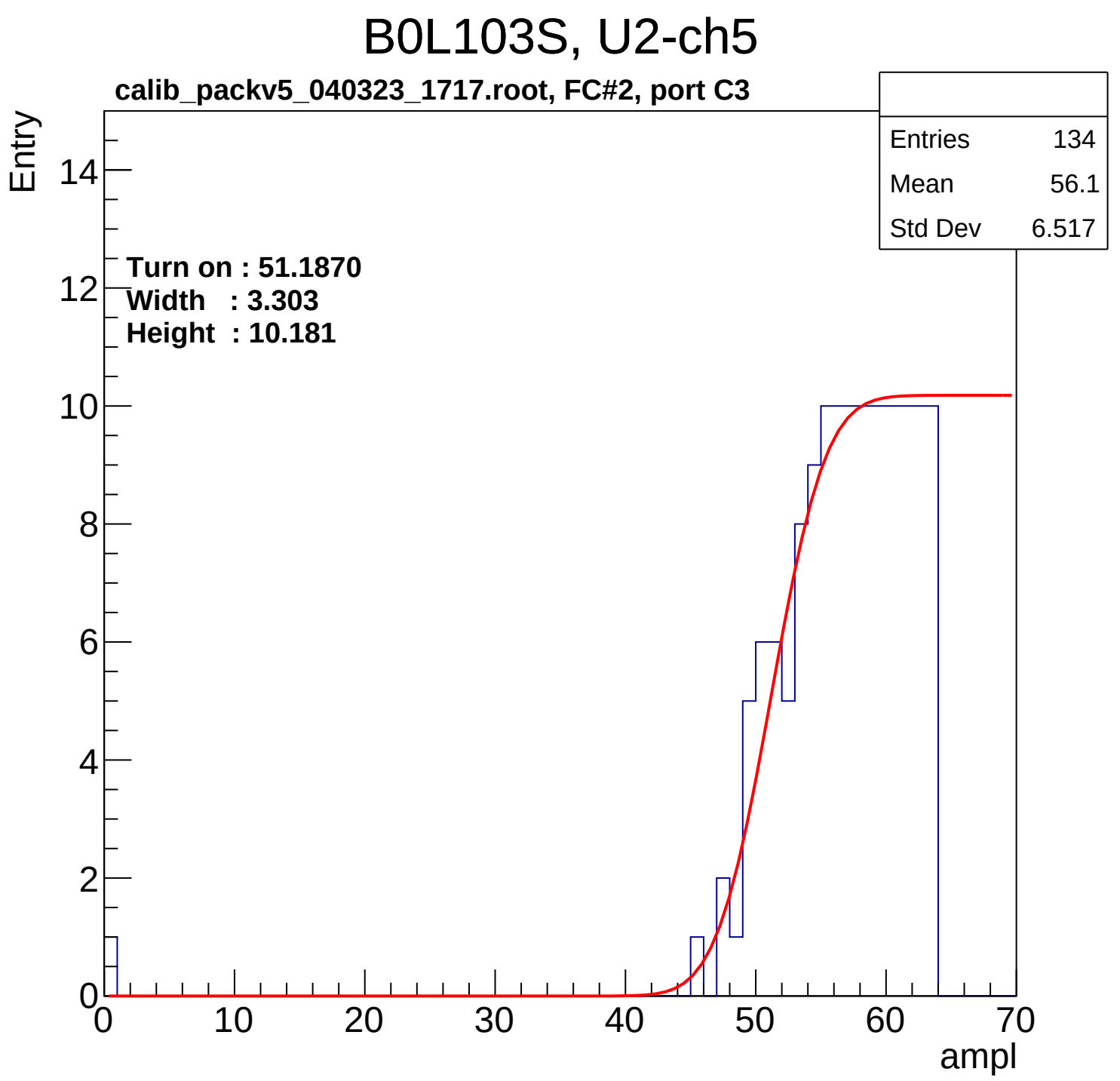
B0L103S, U2-ch5
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 56.1
Std Dev 6.517
Turn on : 51.1870
Width : 3.303
Height : 10.181
Entry
ampl
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2
4
6
8
10
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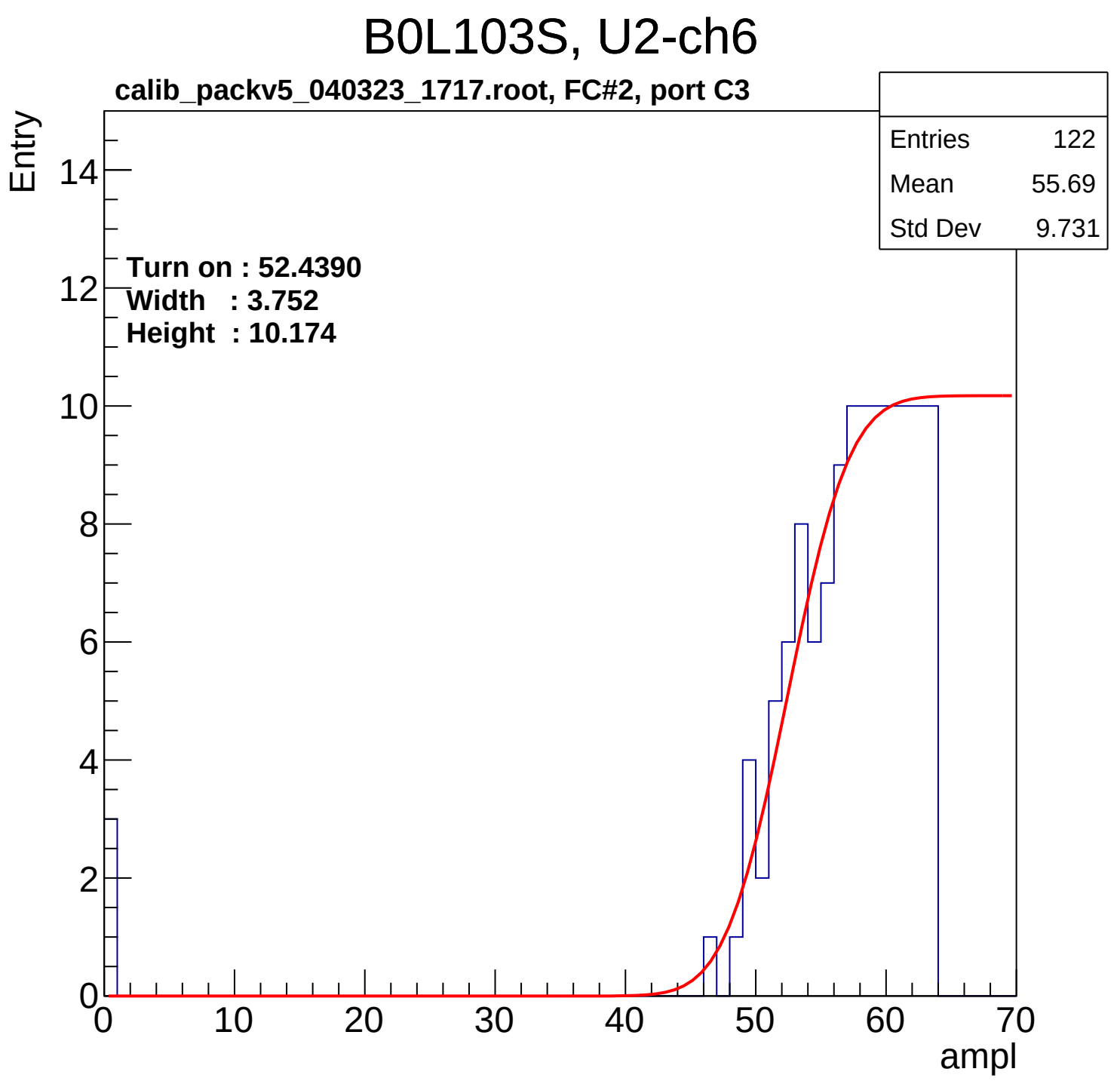
B0L103S, U2-ch6
calib_packv5_040323_1717.root, FC#2, port C3
Entries 122
Mean 55.69
Std Dev 9.731
Turn on : 52.4390
Width : 3.752
Height : 10.174
Entry
ampl
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6
8
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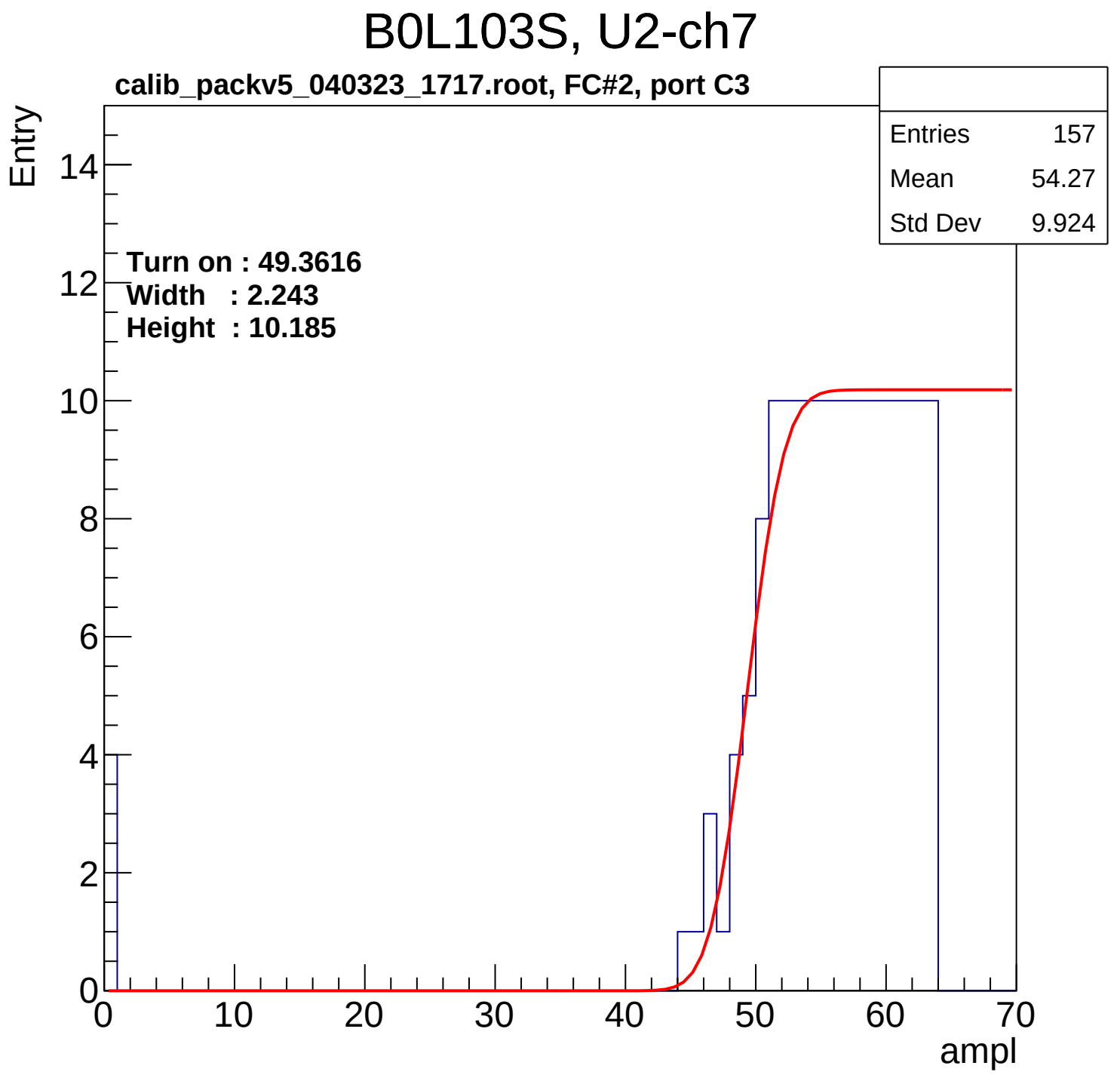
B0L103S, U2-ch7
calib_packv5_040323_1717.root, FC#2, port C3
Entries 157
Mean 54.27
Std Dev 9.924
Turn on : 49.3616
Width : 2.243
Height : 10.185
Entry
ampl
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2
4
6
8
10
12
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0
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40
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60
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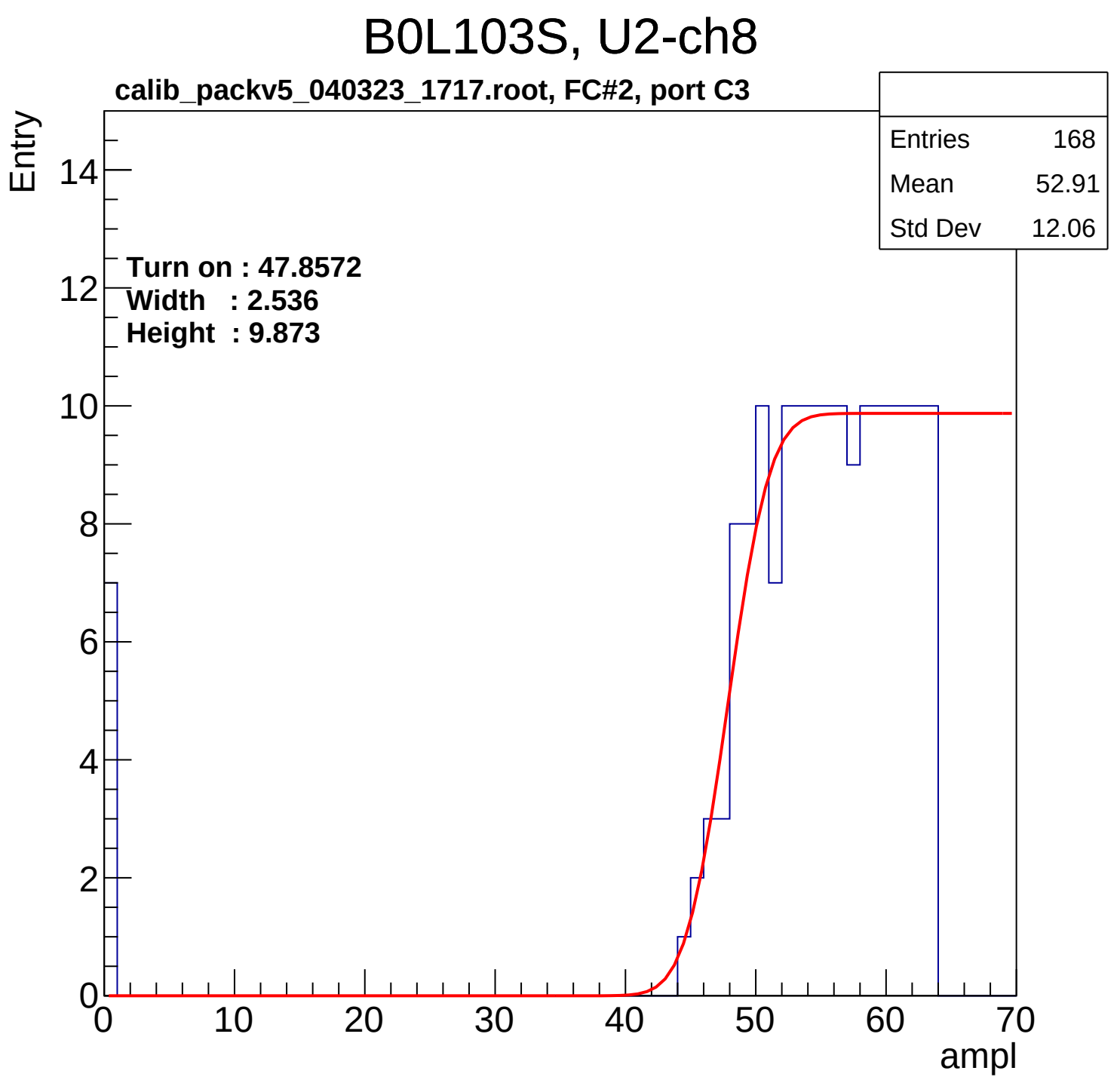
B0L103S, U2-ch8
calib_packv5_040323_1717.root, FC#2, port C3
Entries 168
Mean 52.91
Std Dev 12.06
Turn on : 47.8572
Width : 2.536
Height : 9.873
Entry
ampl
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6
8
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0
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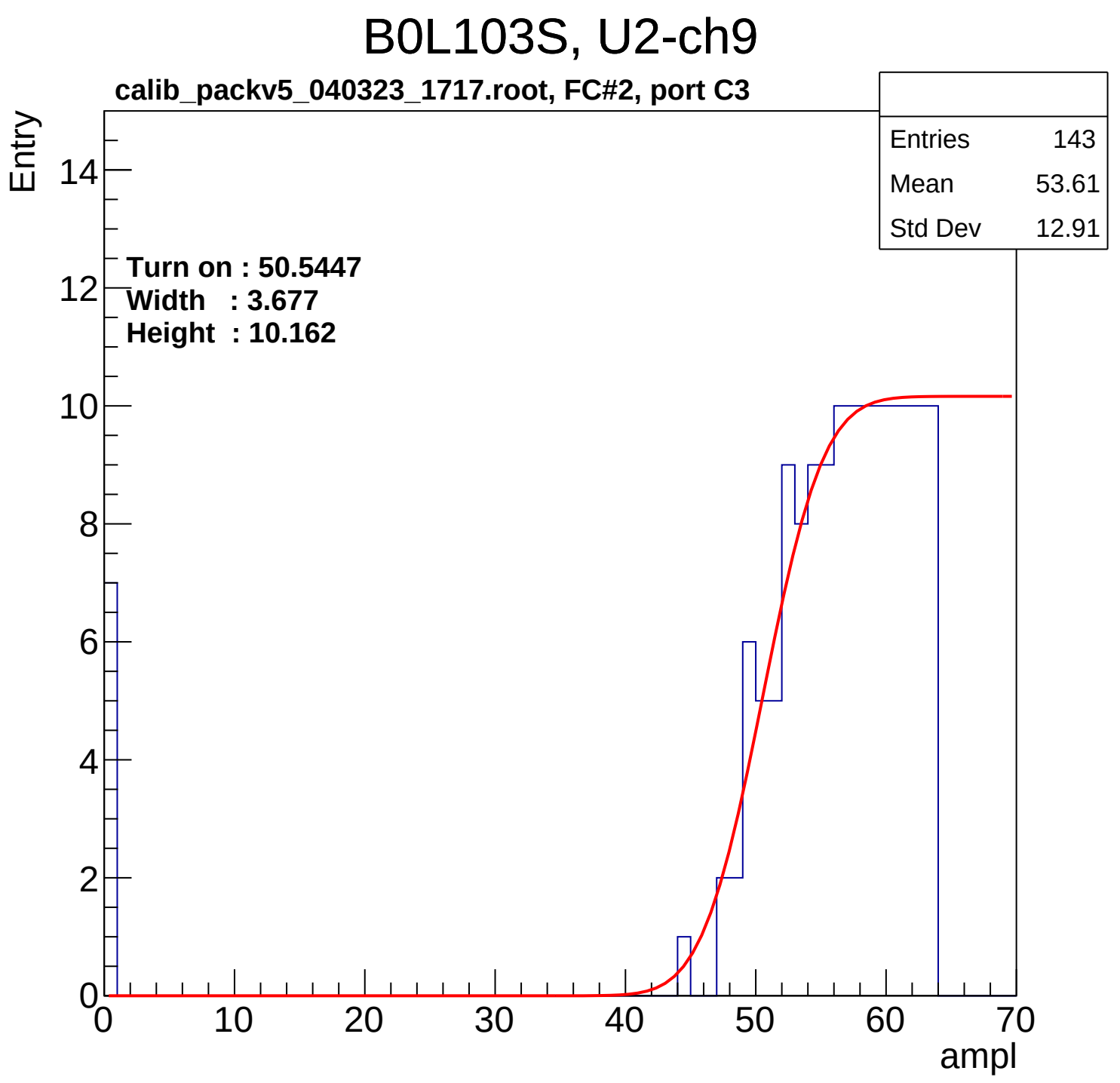
B0L103S, U2-ch9
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 53.61
Std Dev 12.91
Turn on : 50.5447
Width : 3.677
Height : 10.162
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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60
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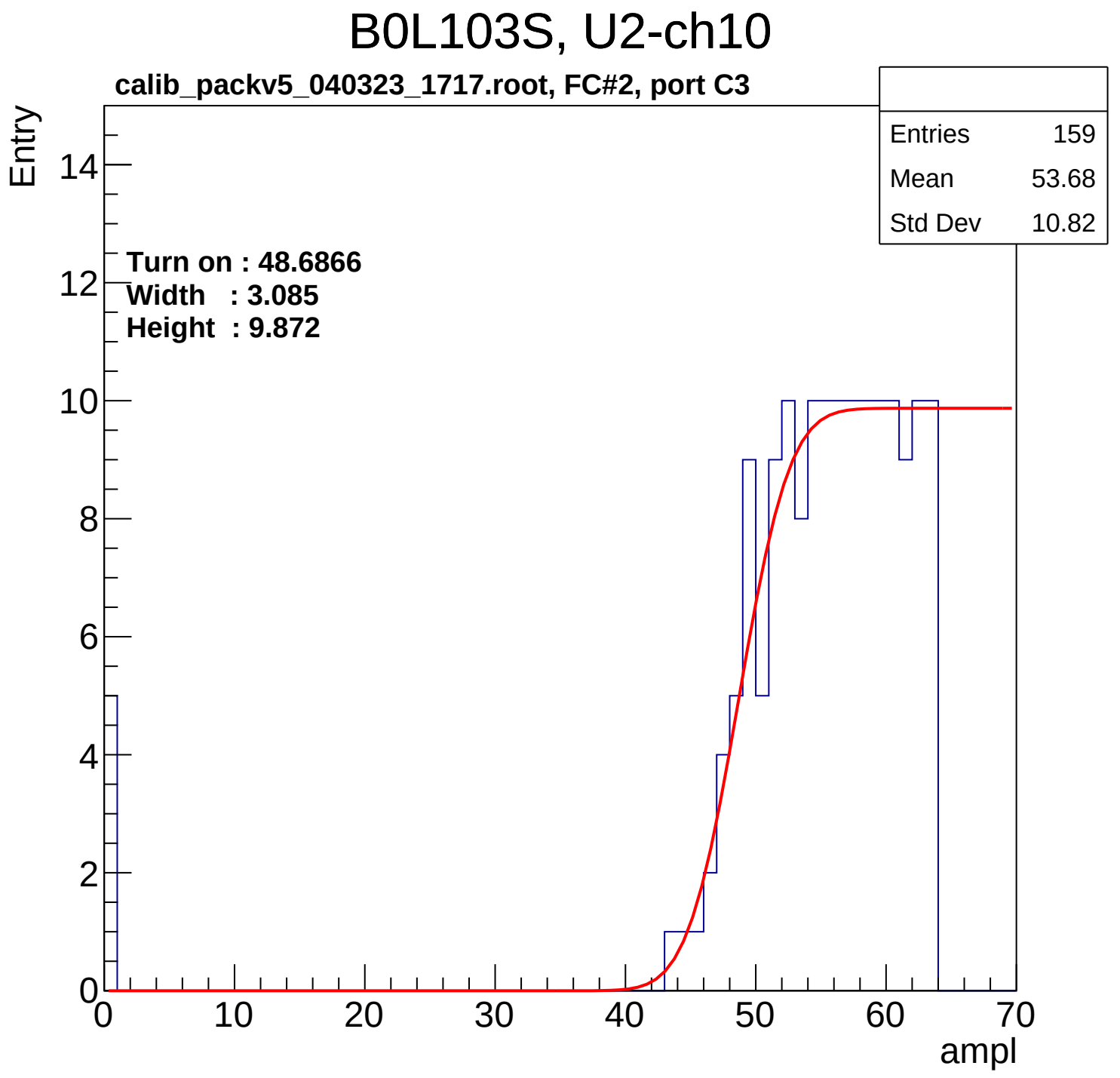
B0L103S, U2-ch10
calib_packv5_040323_1717.root, FC#2, port C3
Entries 159
Mean 53.68
Std Dev 10.82
Turn on : 48.6866
Width : 3.085
Height : 9.872
Entry
ampl
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6
8
10
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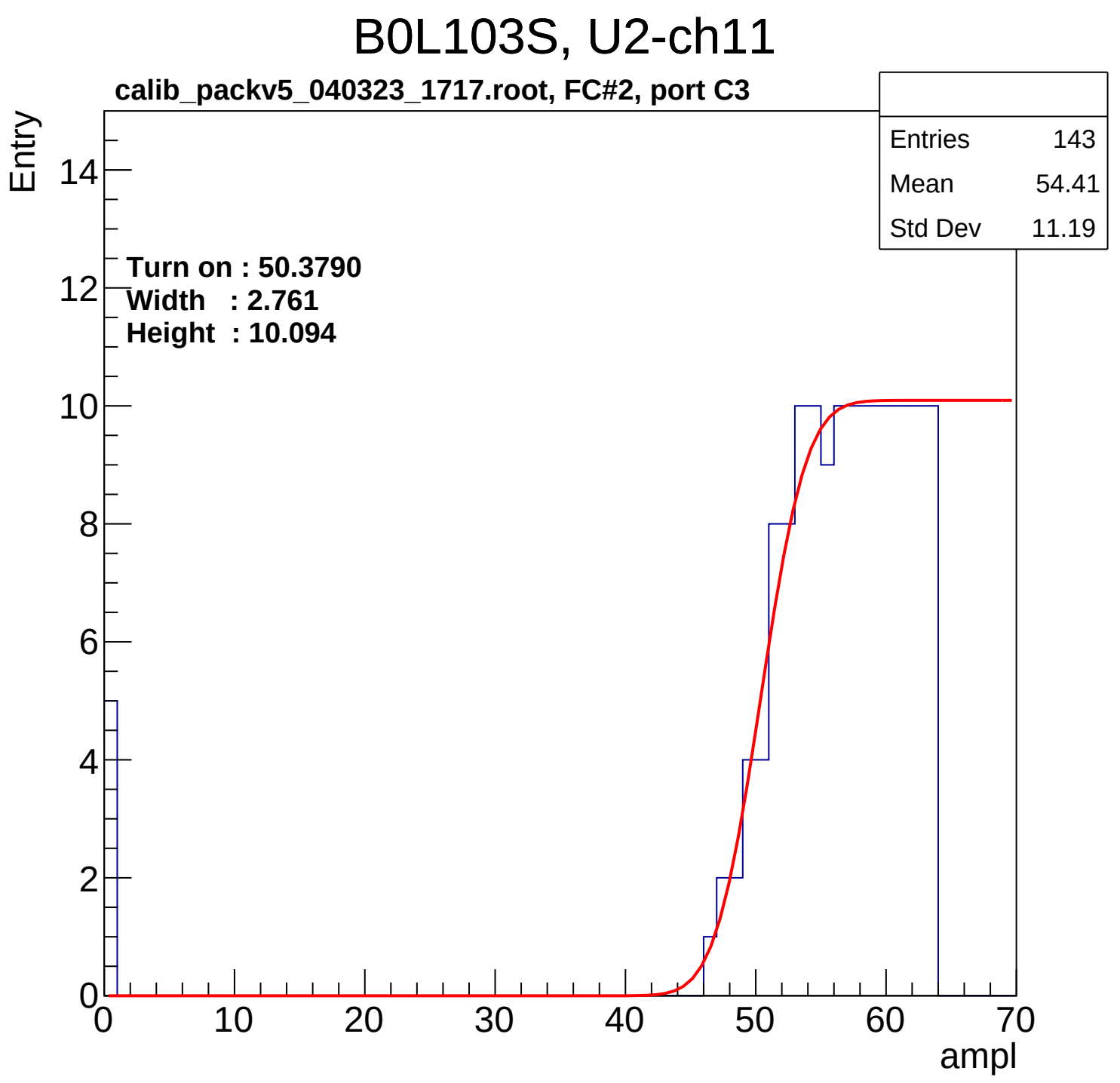
B0L103S, U2-ch11
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 54.41
Std Dev 11.19
Turn on : 50.3790
Width : 2.761
Height : 10.094
Entry
ampl
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4
6
8
10
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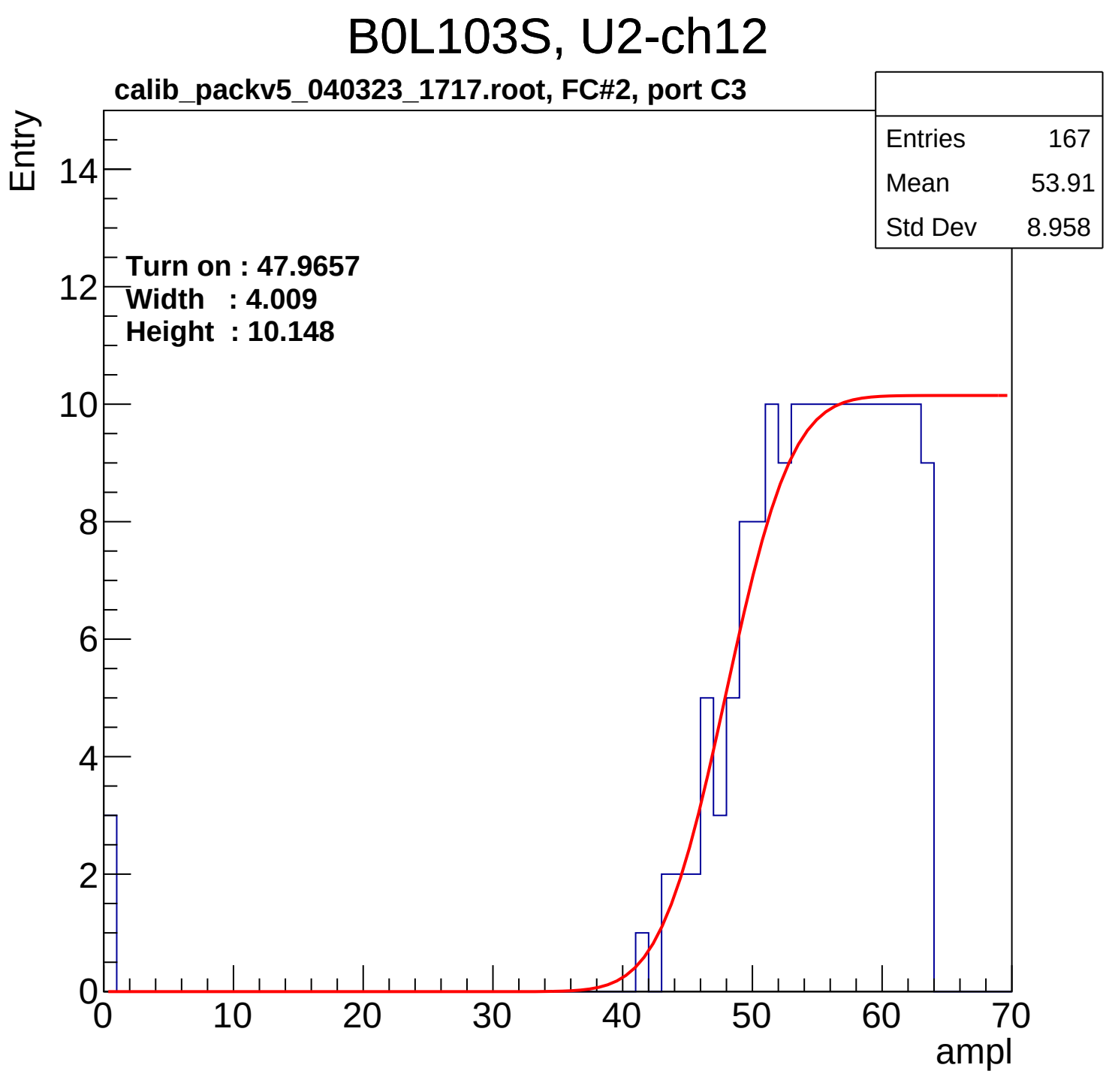
B0L103S, U2-ch12
calib_packv5_040323_1717.root, FC#2, port C3
Entries 167
Mean 53.91
Std Dev 8.958
Turn on : 47.9657
Width : 4.009
Height : 10.148
Entry
ampl
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8
10
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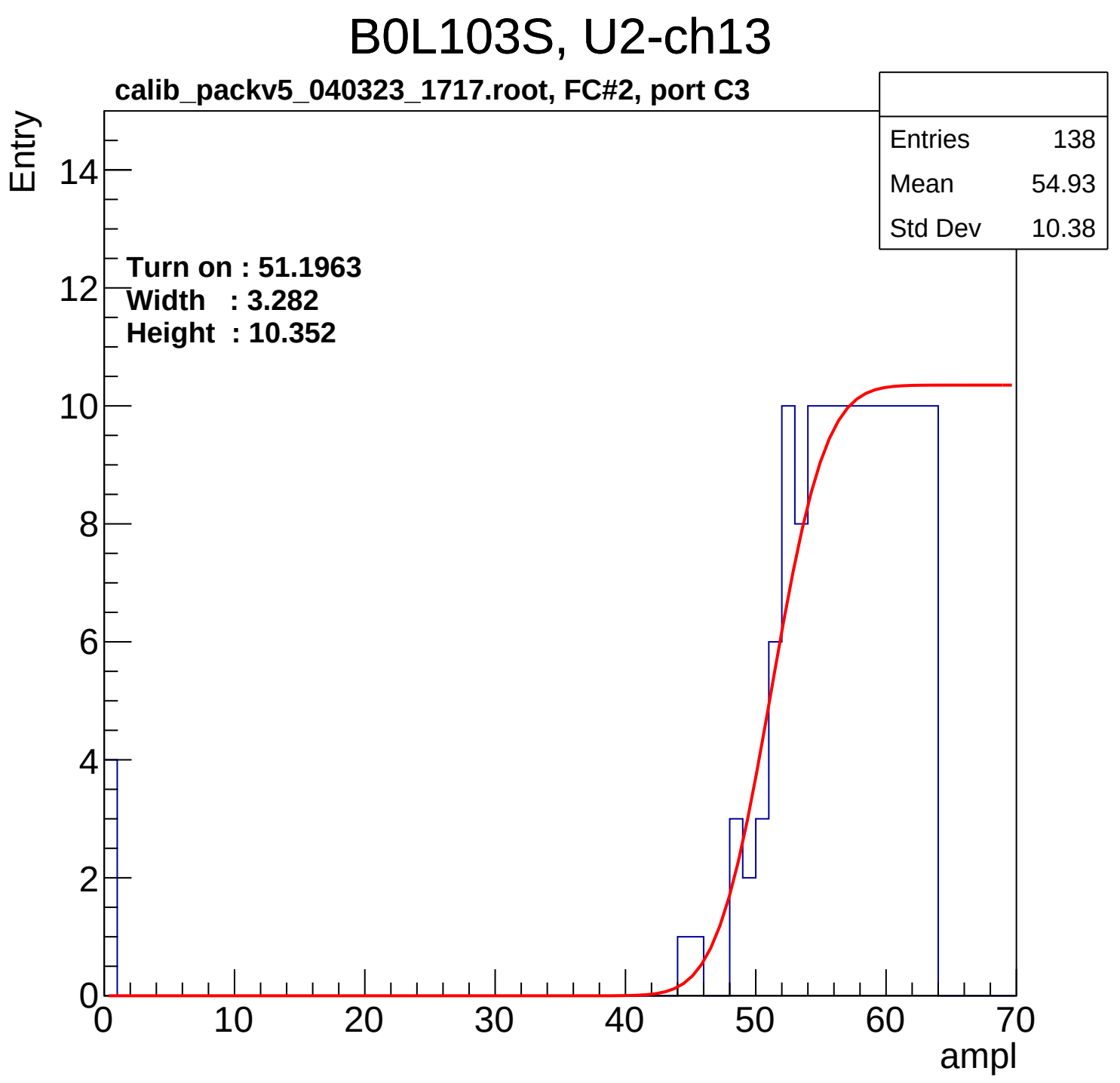
B0L103S, U2-ch13
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 54.93
Std Dev 10.38
Turn on : 51.1963
Width : 3.282
Height : 10.352
Entry
ampl
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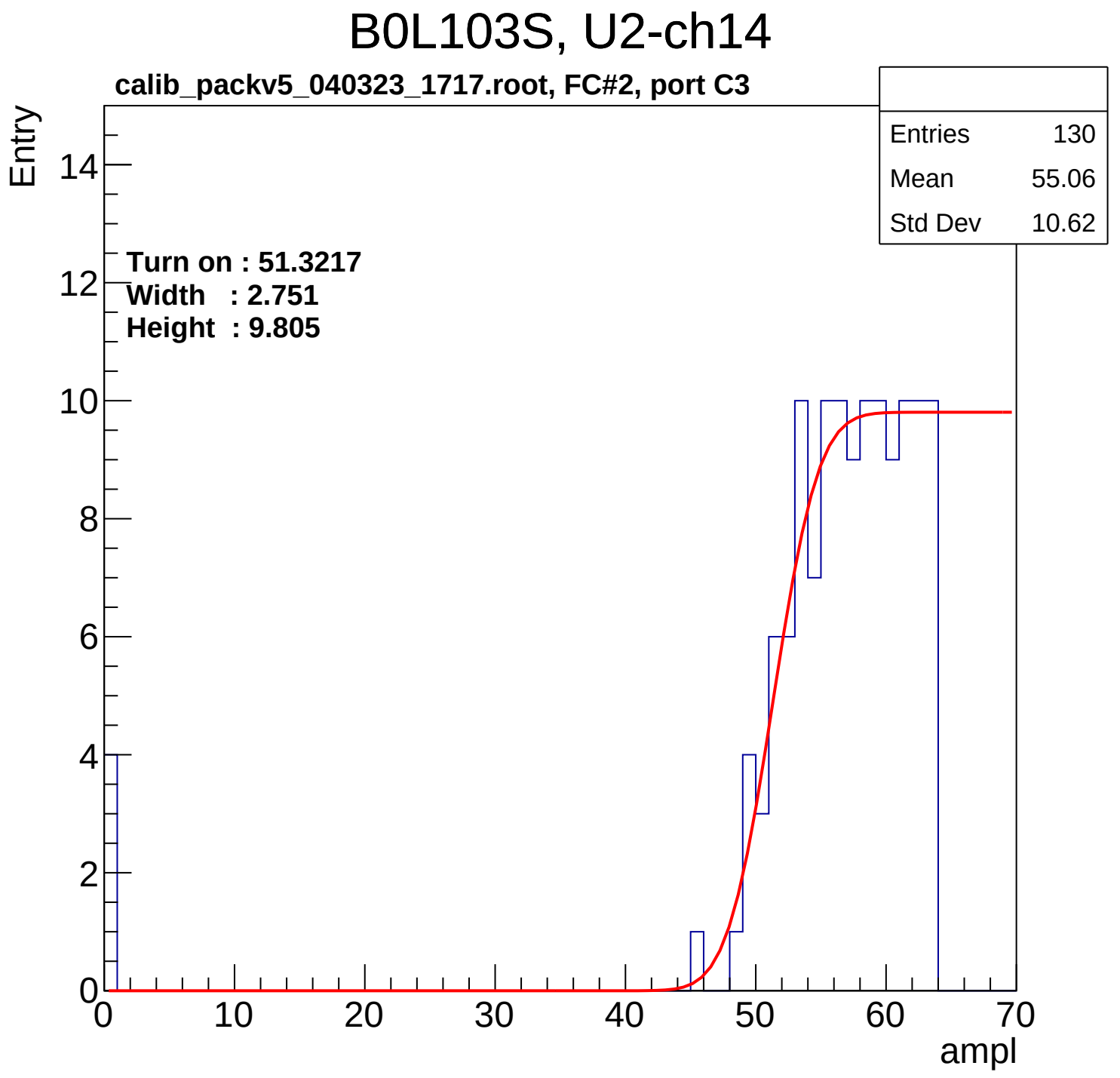
B0L103S, U2-ch14
calib_packv5_040323_1717.root, FC#2, port C3
Entries 130
Mean 55.06
Std Dev 10.62
Turn on : 51.3217
Width : 2.751
Height : 9.805
Entry
ampl
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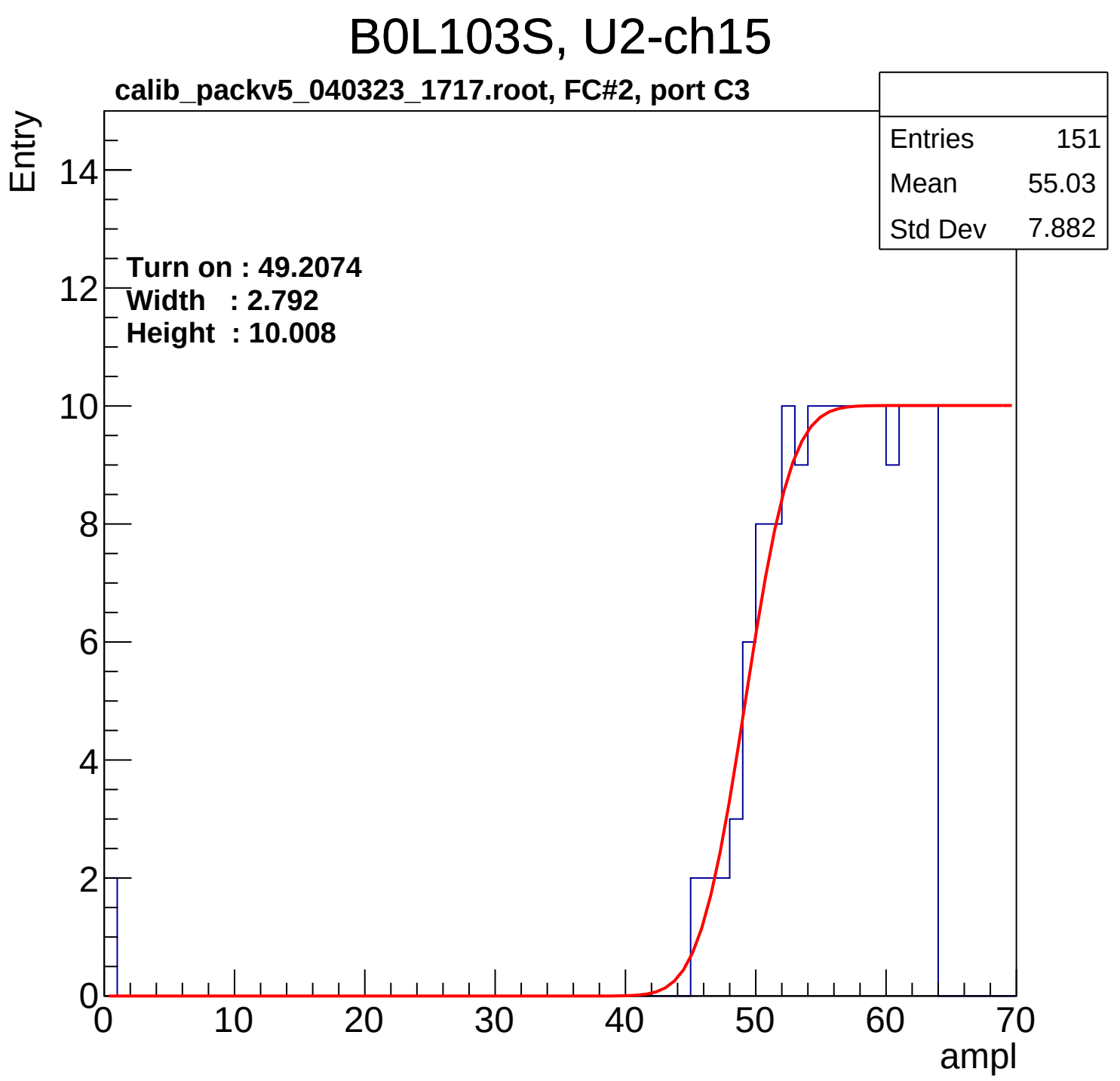
B0L103S, U2-ch15
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 55.03
Std Dev 7.882
Turn on : 49.2074
Width : 2.792
Height : 10.008
Entry
ampl
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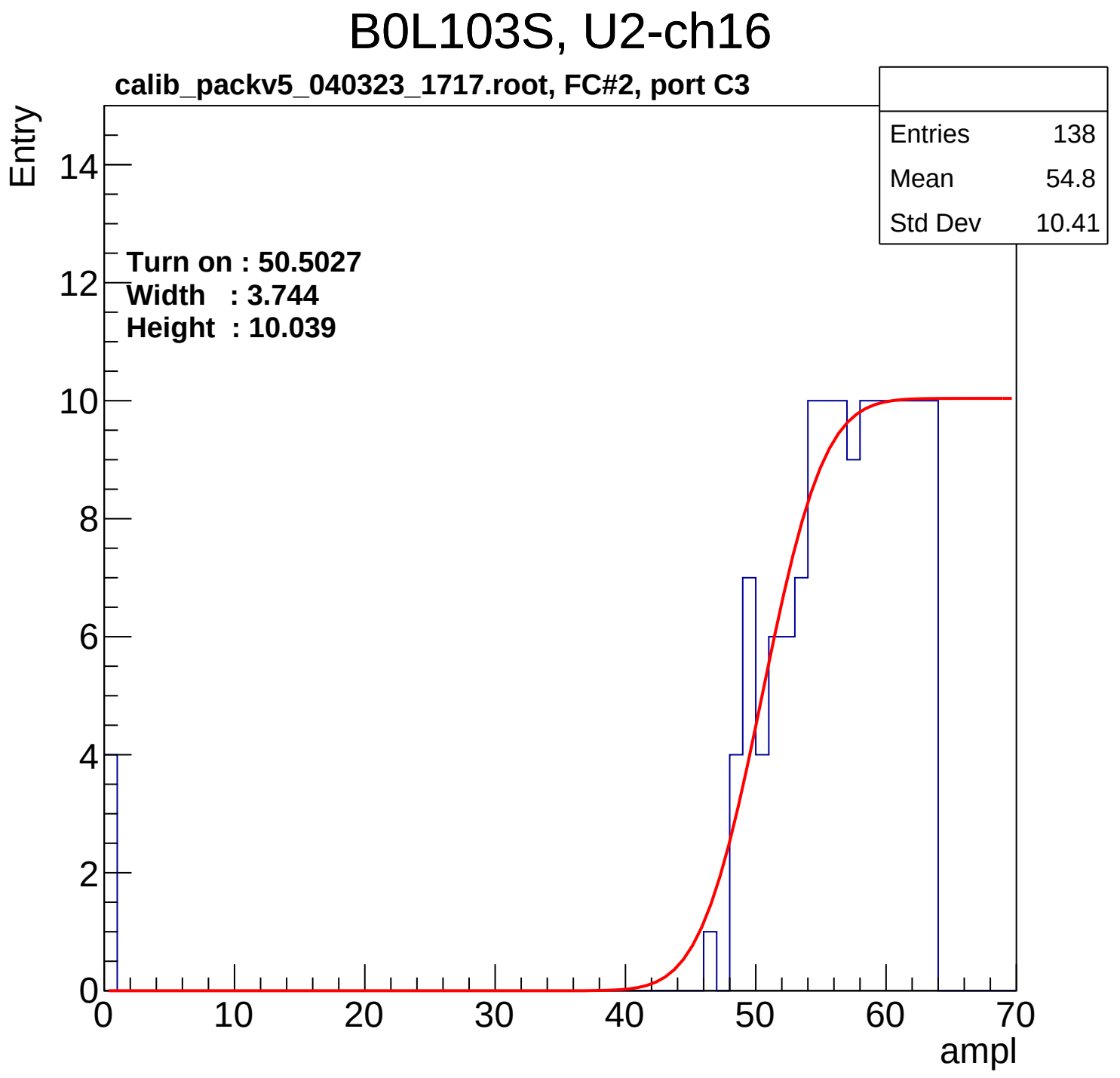
B0L103S, U2-ch16
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 54.8
Std Dev 10.41
Turn on : 50.5027
Width : 3.744
Height : 10.039
Entry
ampl
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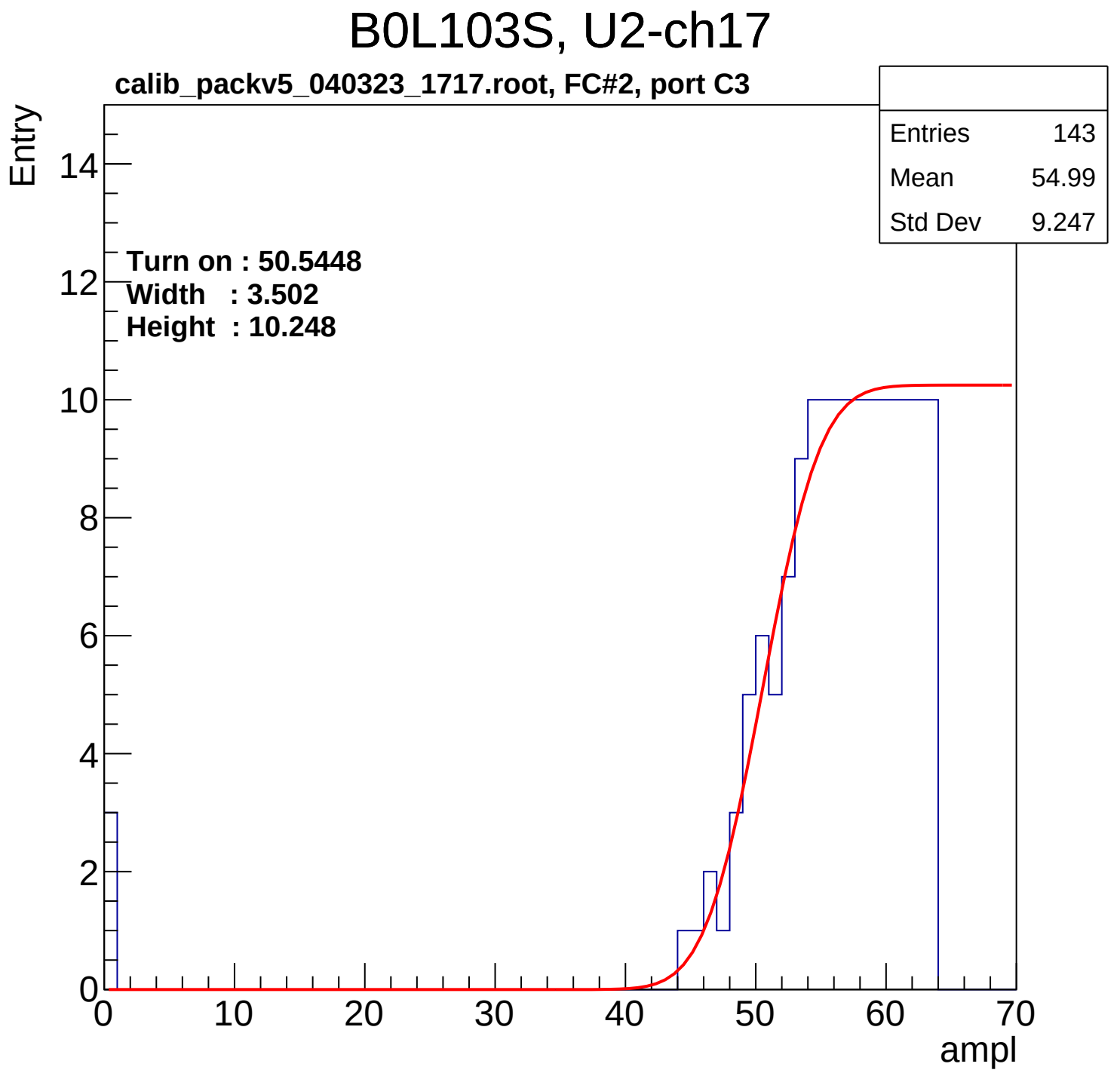
B0L103S, U2-ch17
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 54.99
Std Dev 9.247
Turn on : 50.5448
Width : 3.502
Height : 10.248
Entry
ampl
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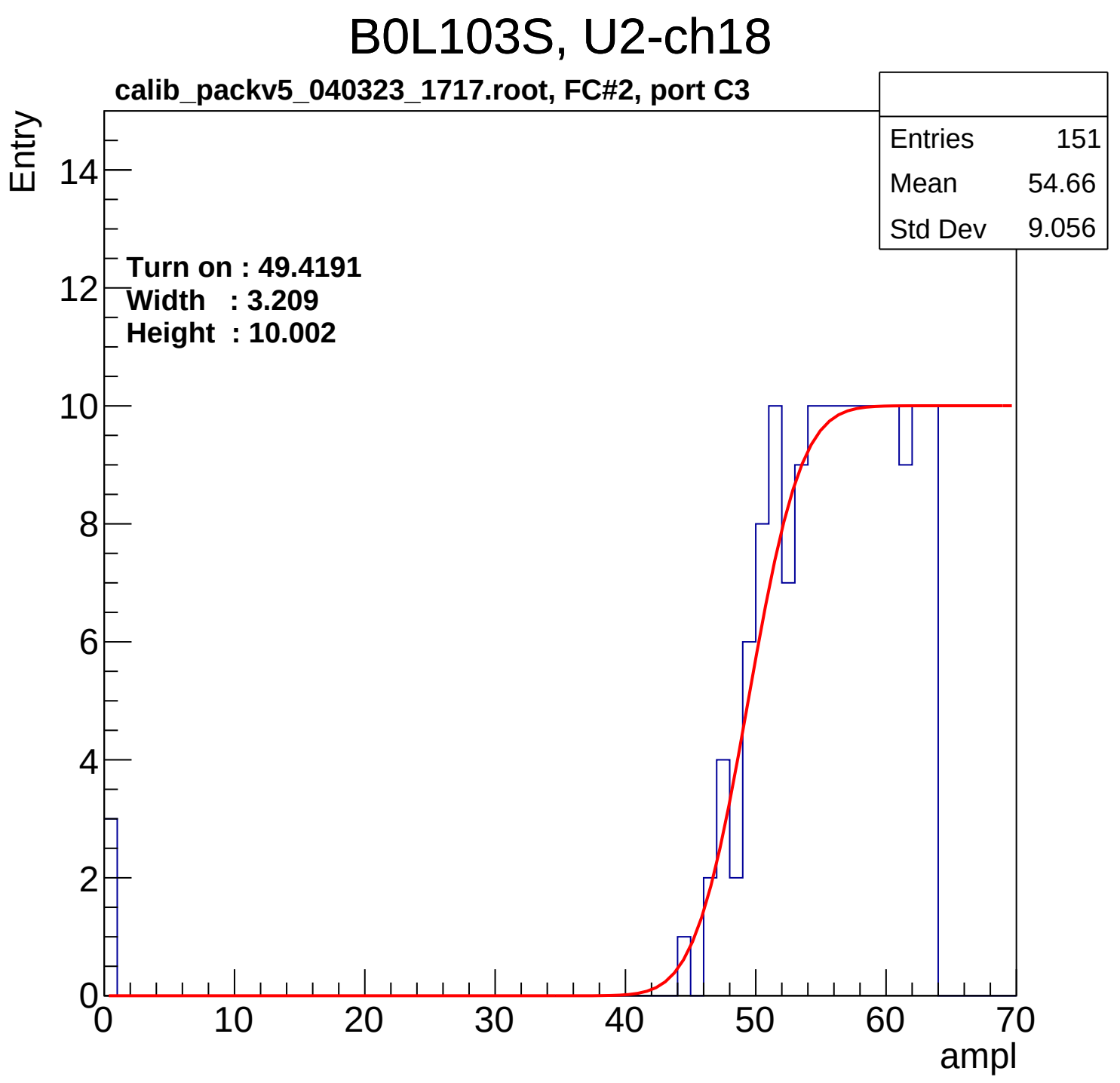
B0L103S, U2-ch18
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 54.66
Std Dev 9.056
Turn on : 49.4191
Width : 3.209
Height : 10.002
Entry
ampl
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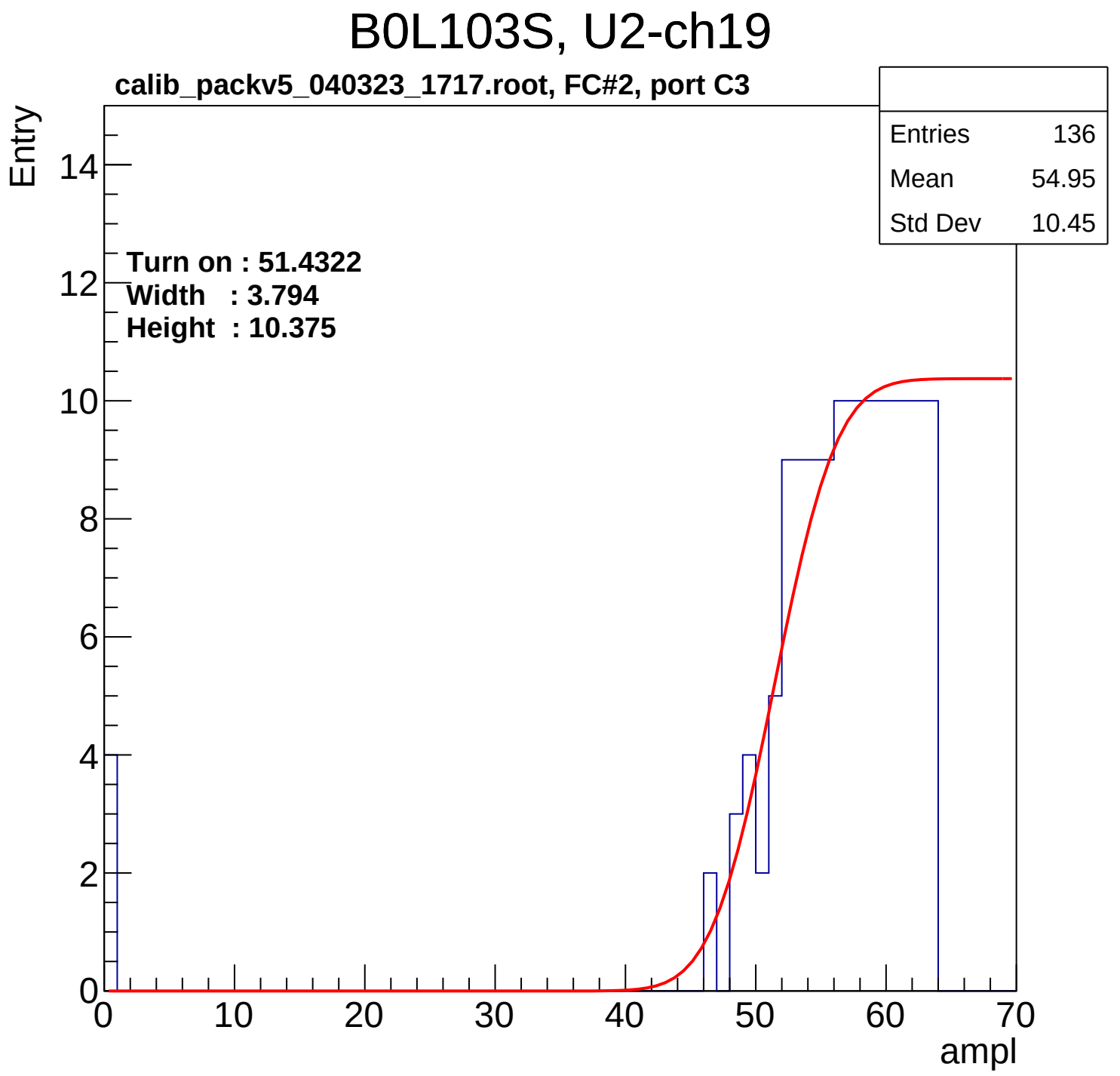
B0L103S, U2-ch19
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 54.95
Std Dev 10.45
Turn on : 51.4322
Width : 3.794
Height : 10.375
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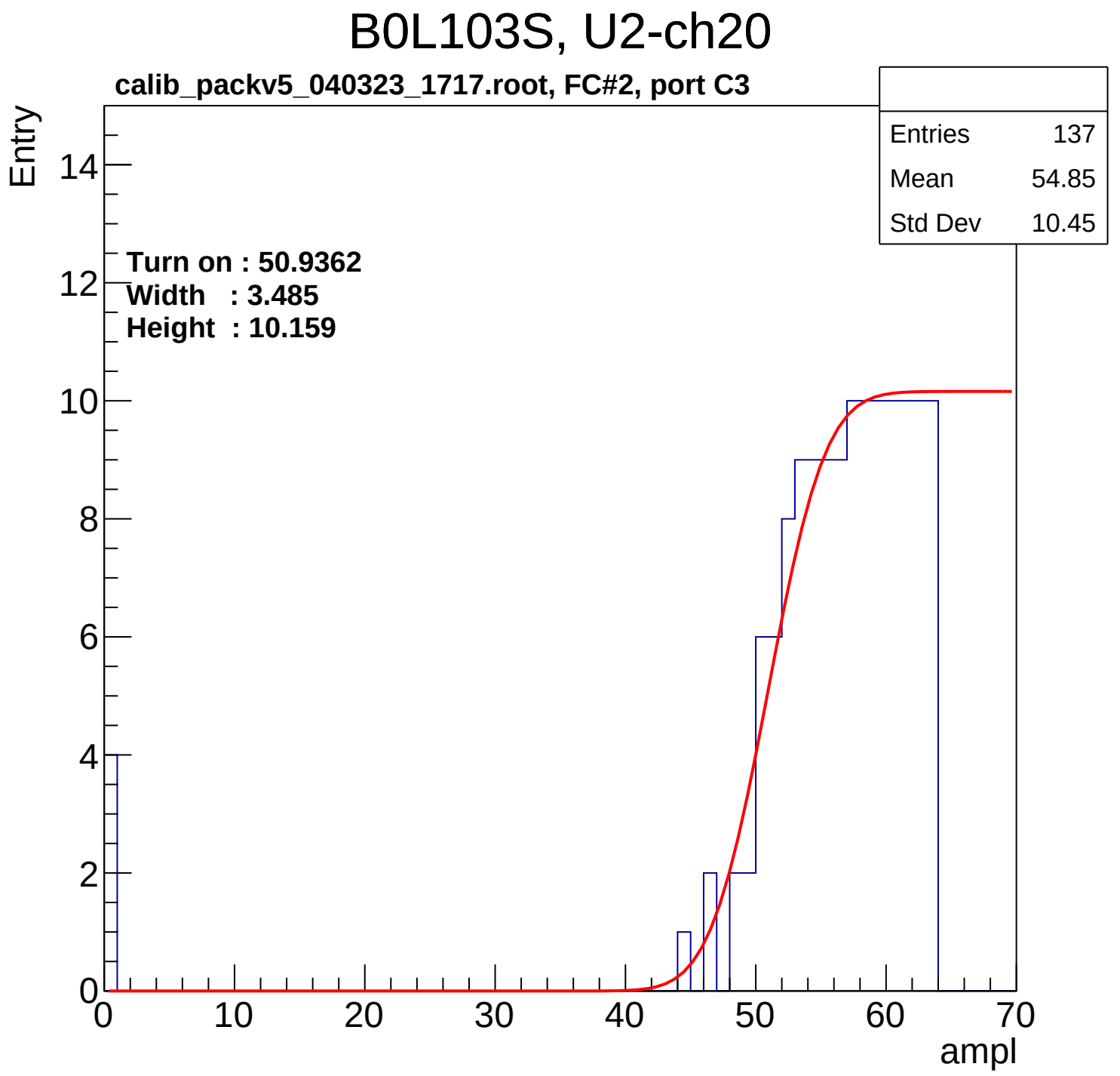
B0L103S, U2-ch20
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 54.85
Std Dev 10.45
Turn on : 50.9362
Width : 3.485
Height : 10.159
Entry
ampl
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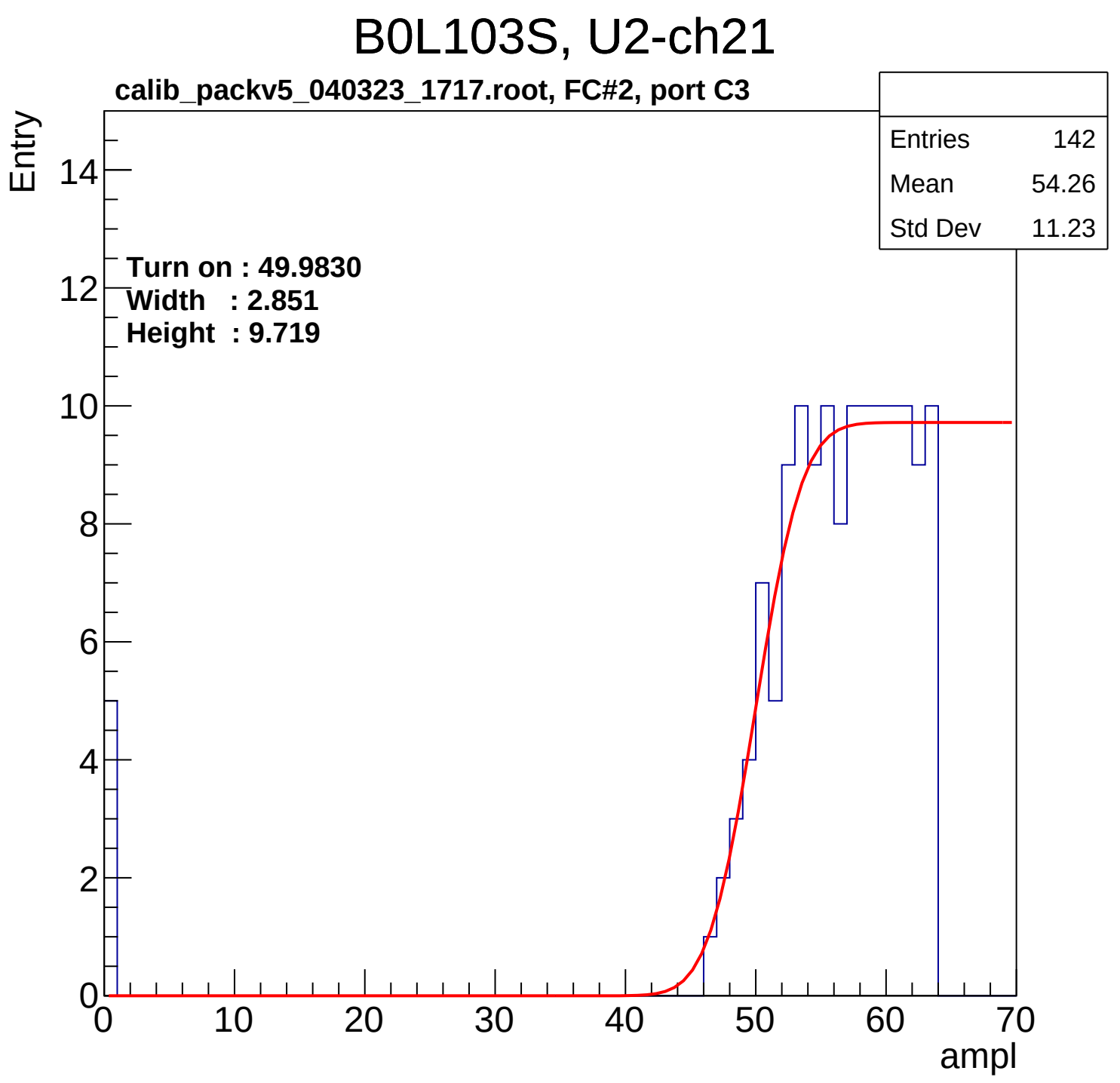
B0L103S, U2-ch21
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 54.26
Std Dev 11.23
Turn on : 49.9830
Width : 2.851
Height : 9.719
Entry
ampl
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2
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6
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10
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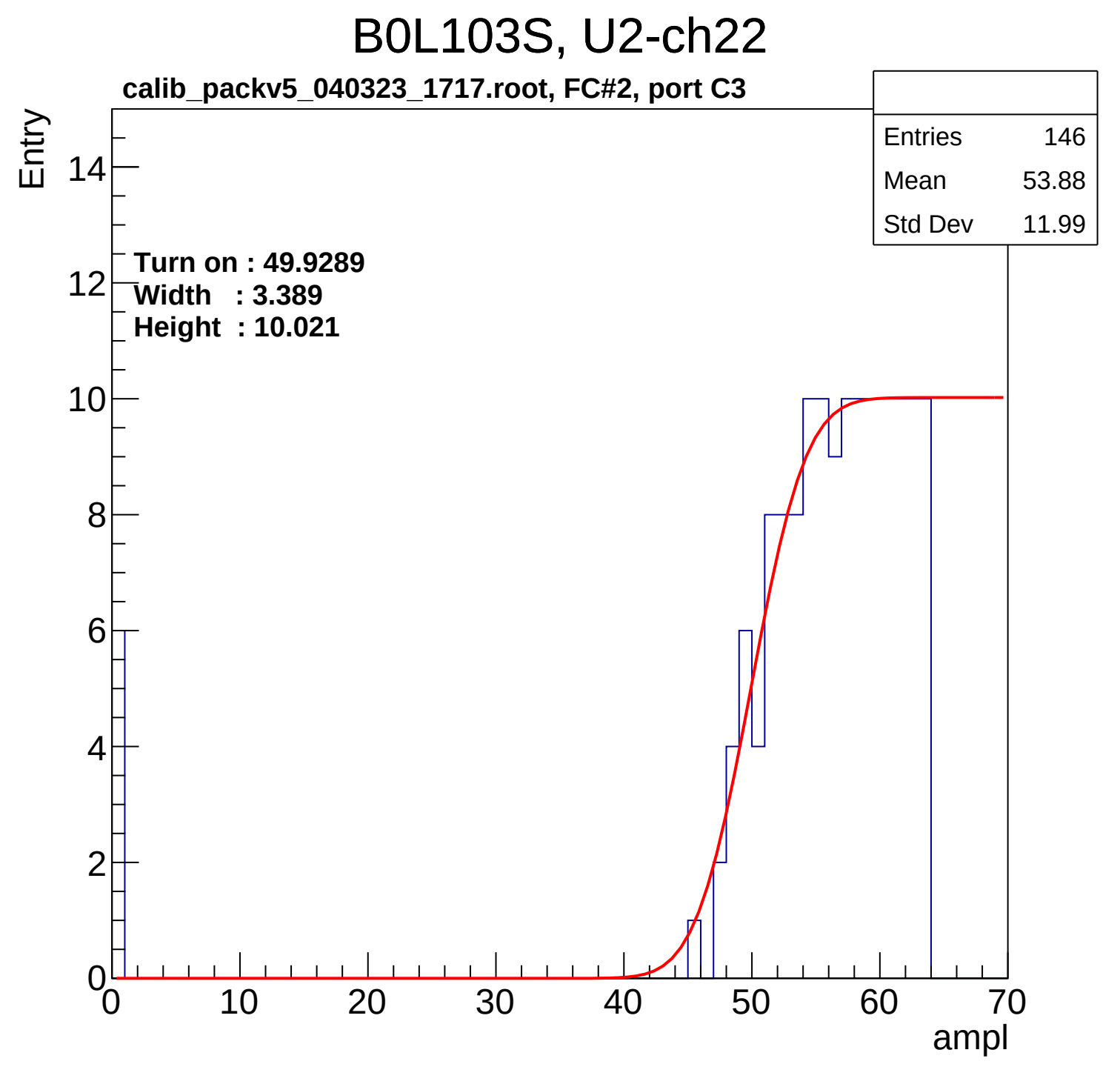
B0L103S, U2-ch22
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 53.88
Std Dev 11.99
Turn on : 49.9289
Width : 3.389
Height : 10.021
Entry
ampl
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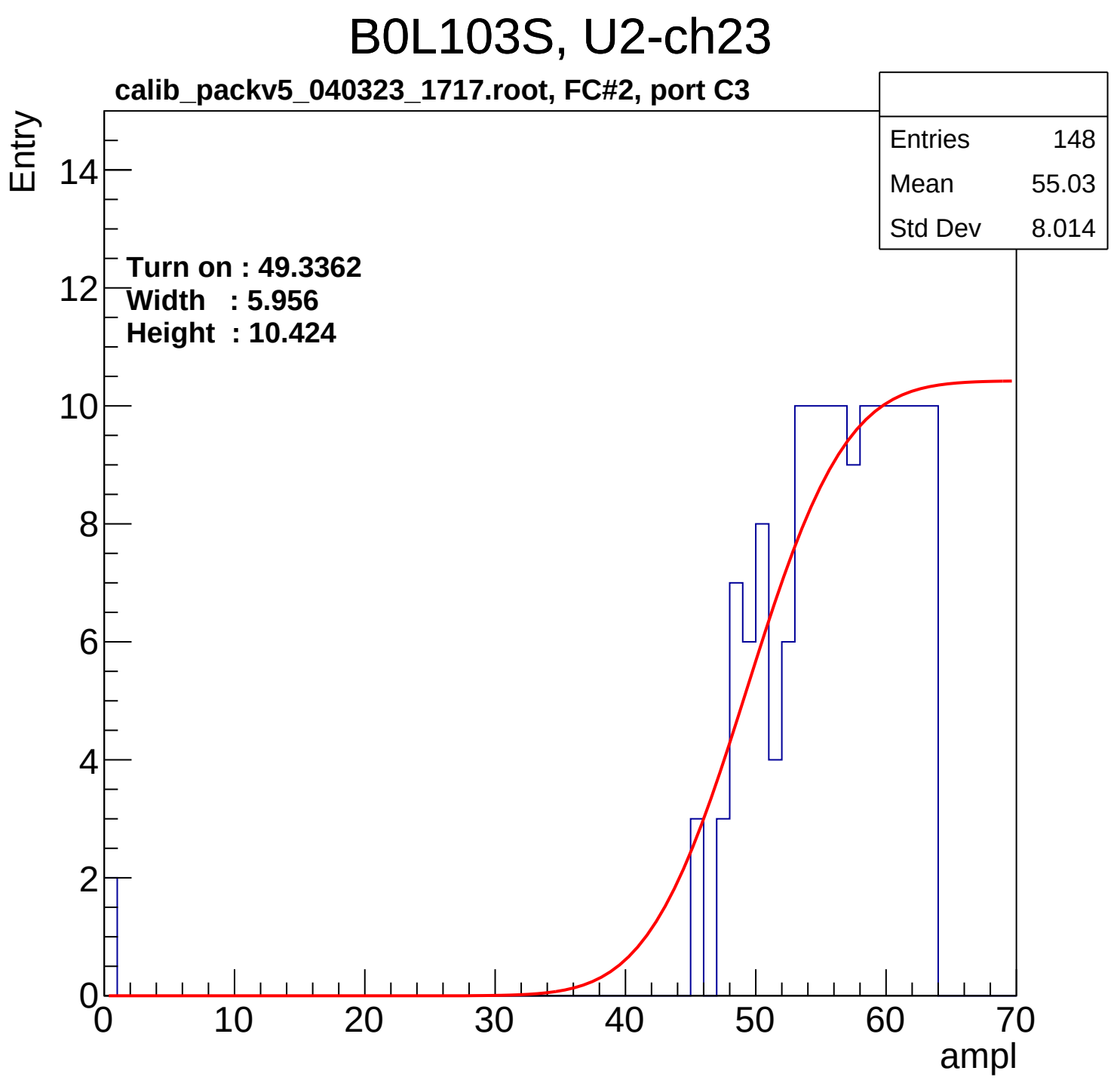
B0L103S, U2-ch23
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 55.03
Std Dev 8.014
Turn on : 49.3362
Width : 5.956
Height : 10.424
Entry
ampl
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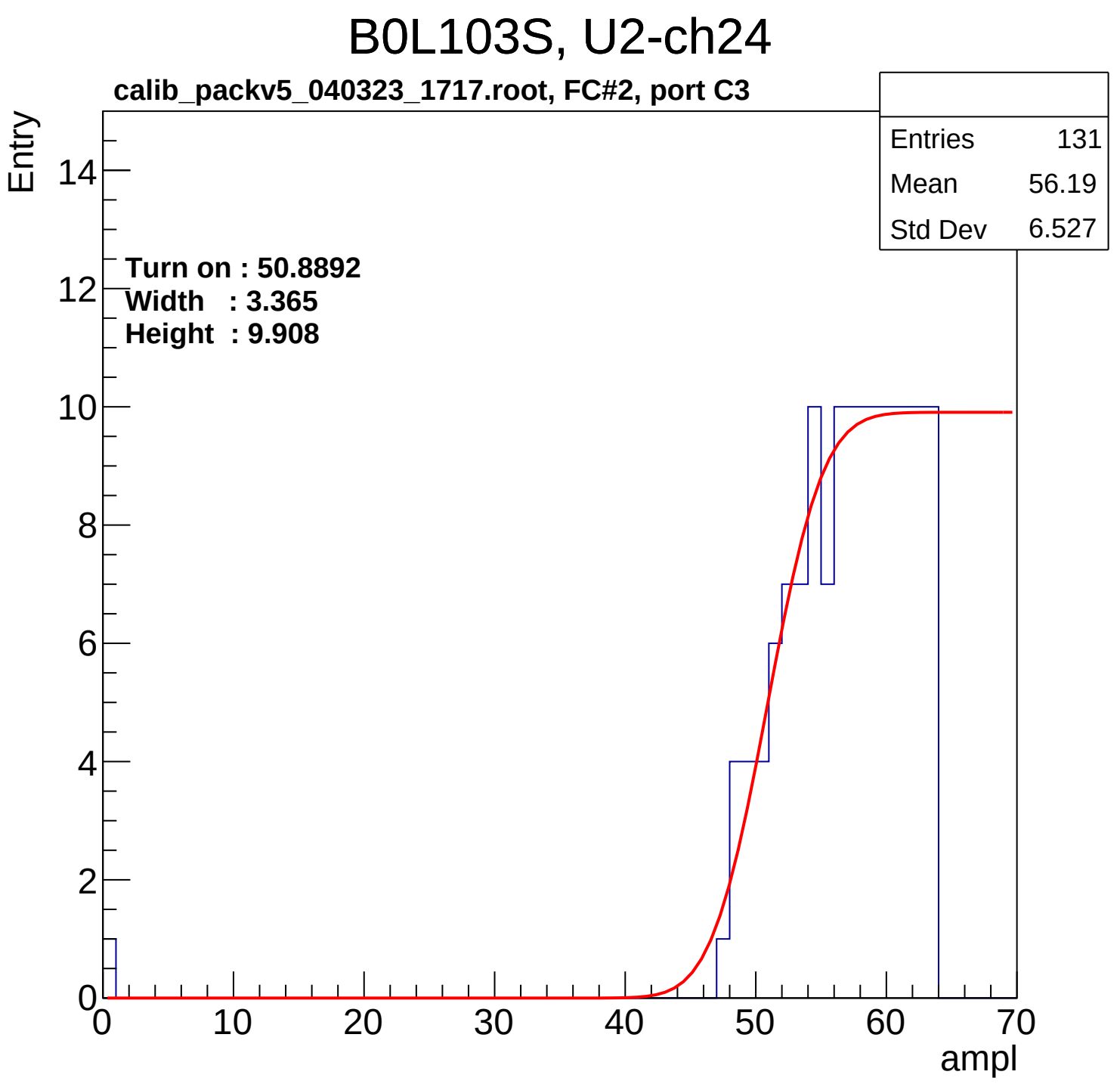
B0L103S, U2-ch24
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 56.19
Std Dev 6.527
Turn on : 50.8892
Width : 3.365
Height : 9.908
Entry
ampl
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6
8
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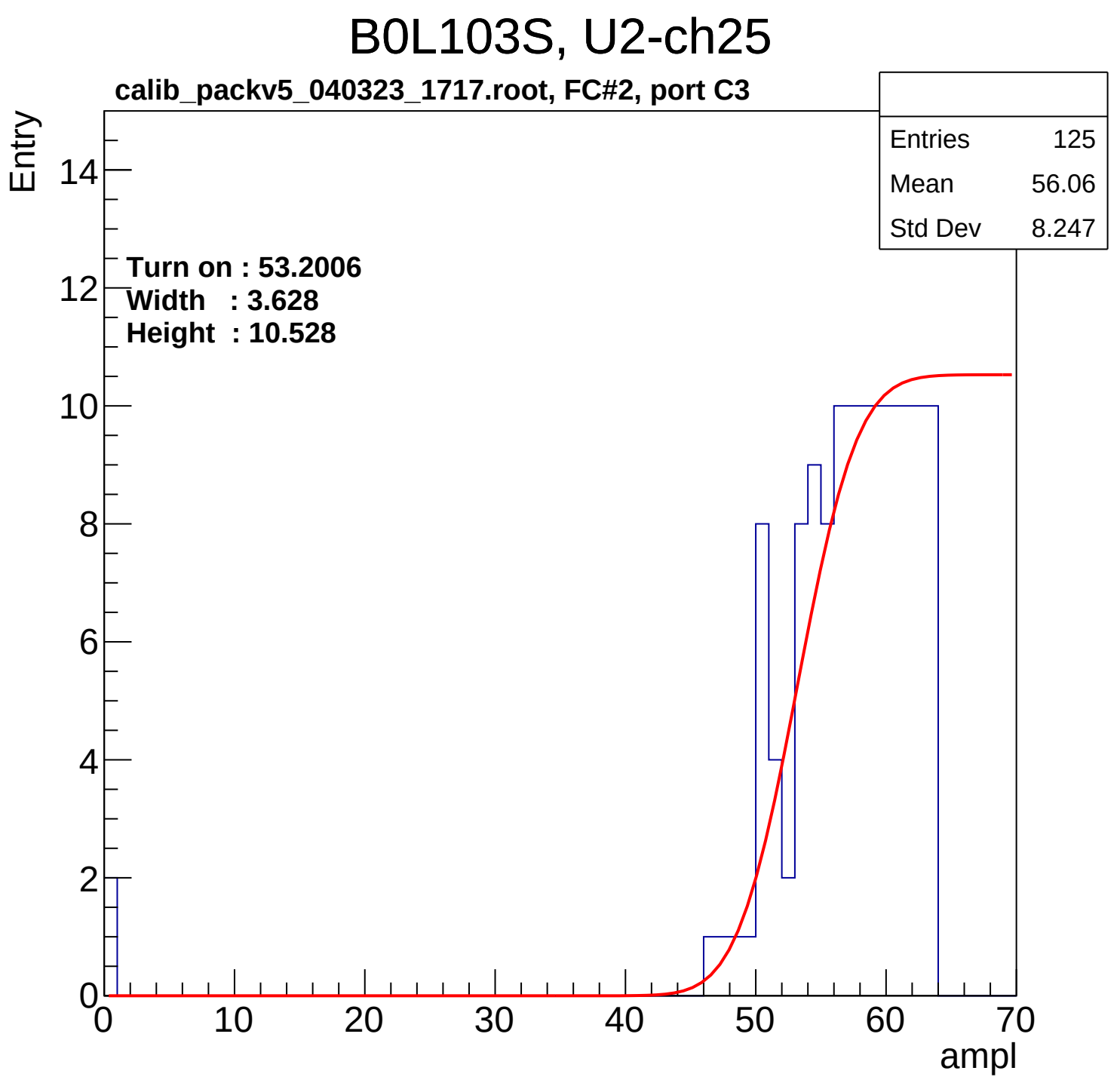
B0L103S, U2-ch25
calib_packv5_040323_1717.root, FC#2, port C3
Entries 125
Mean 56.06
Std Dev 8.247
Turn on : 53.2006
Width : 3.628
Height : 10.528
Entry
ampl
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8
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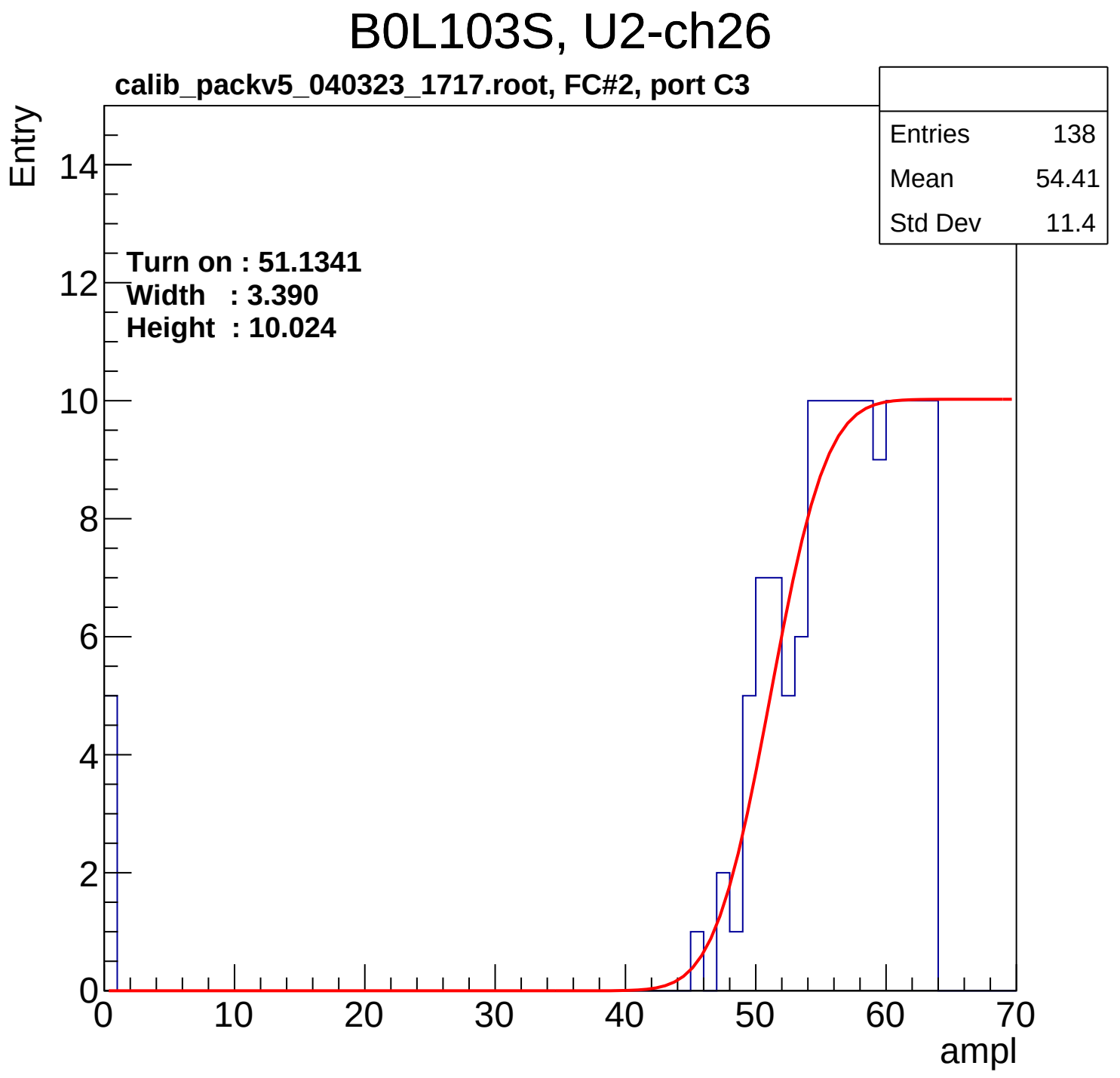
B0L103S, U2-ch26
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 54.41
Std Dev 11.4
Turn on : 51.1341
Width : 3.390
Height : 10.024
Entry
ampl
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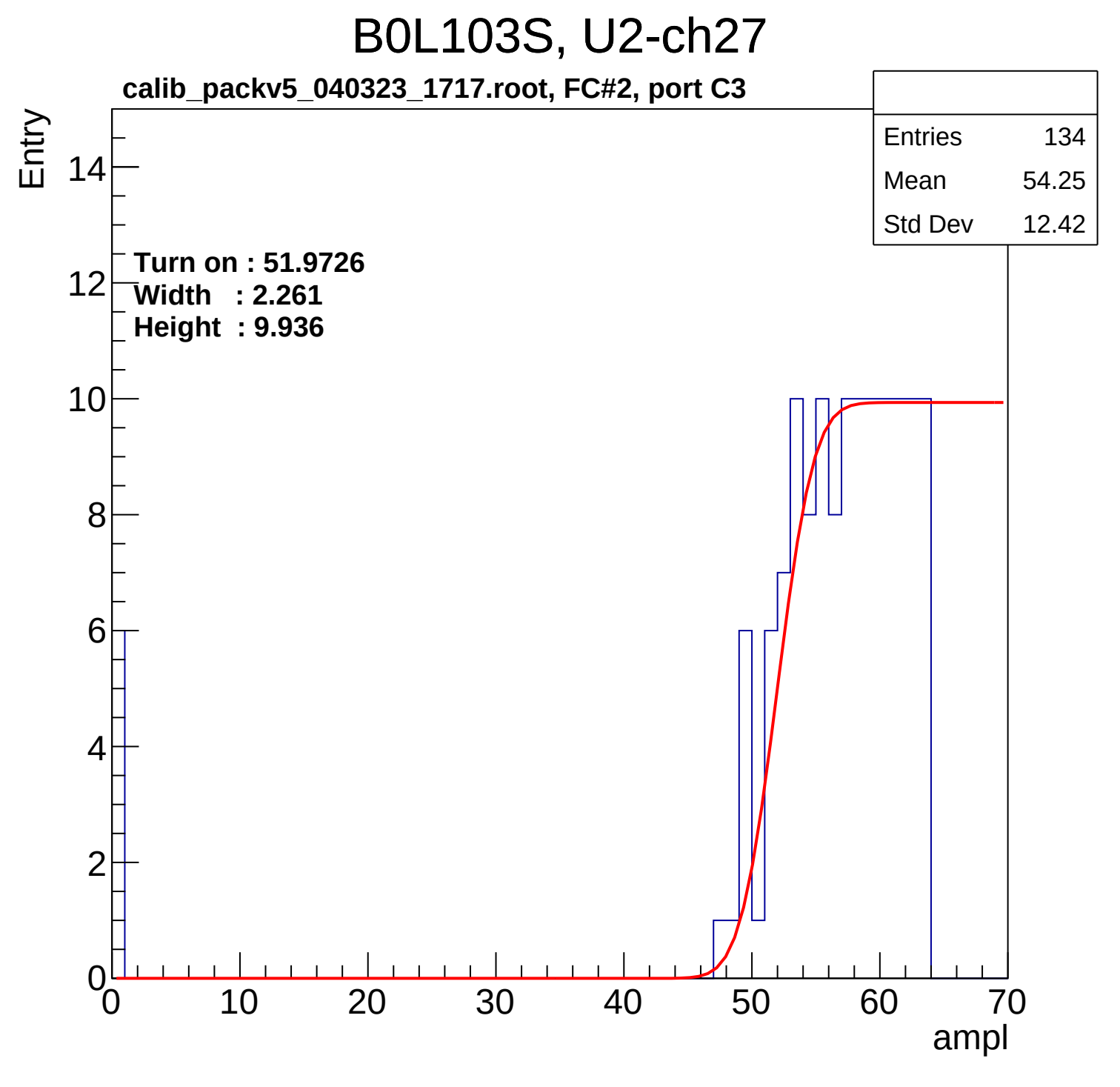
B0L103S, U2-ch27
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 54.25
Std Dev 12.42
Turn on : 51.9726
Width : 2.261
Height : 9.936
Entry
ampl
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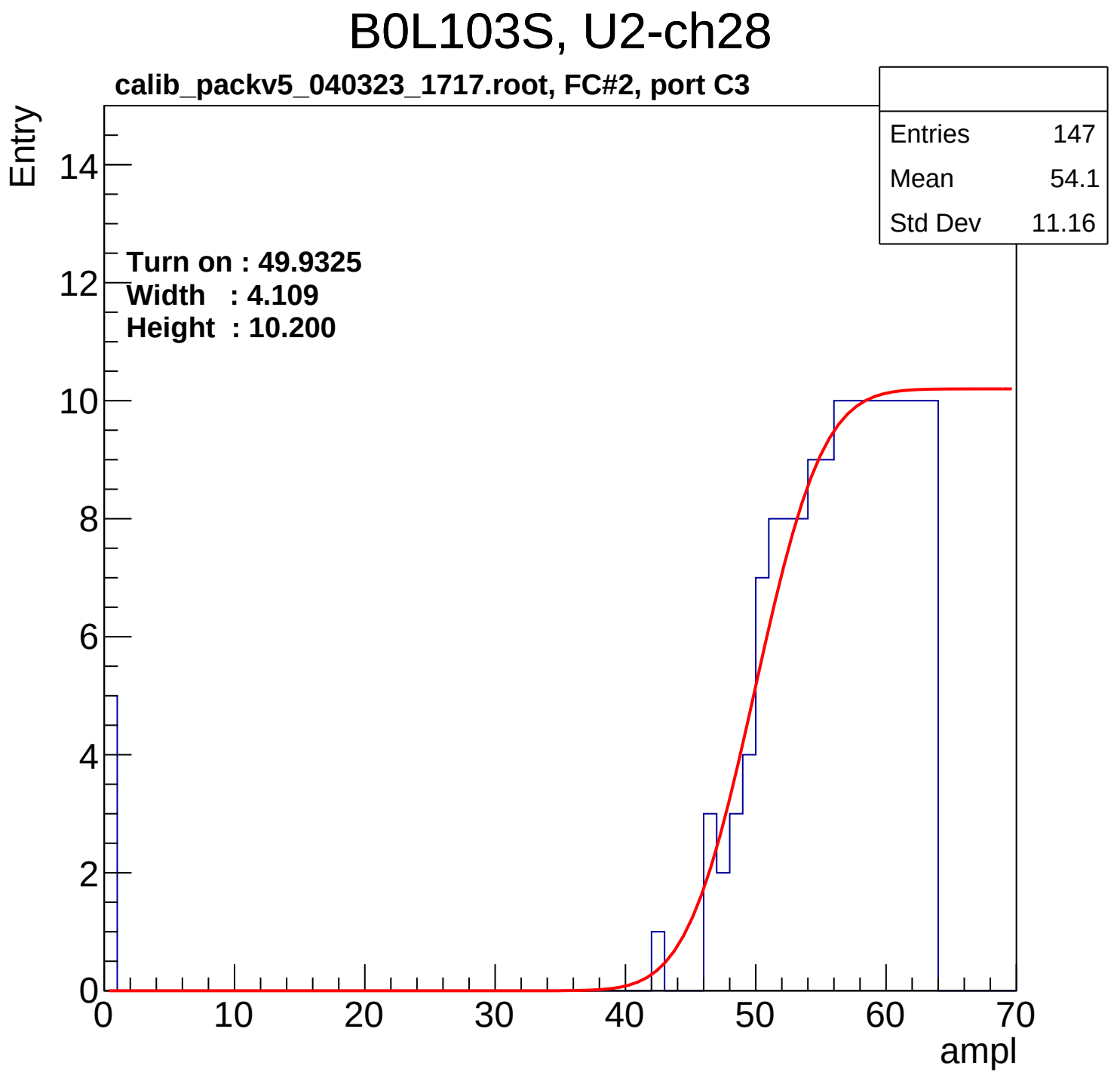
B0L103S, U2-ch28
calib_packv5_040323_1717.root, FC#2, port C3
Entries 147
Mean 54.1
Std Dev 11.16
Turn on : 49.9325
Width : 4.109
Height : 10.200
Entry
ampl
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4
6
8
10
12
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0
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20
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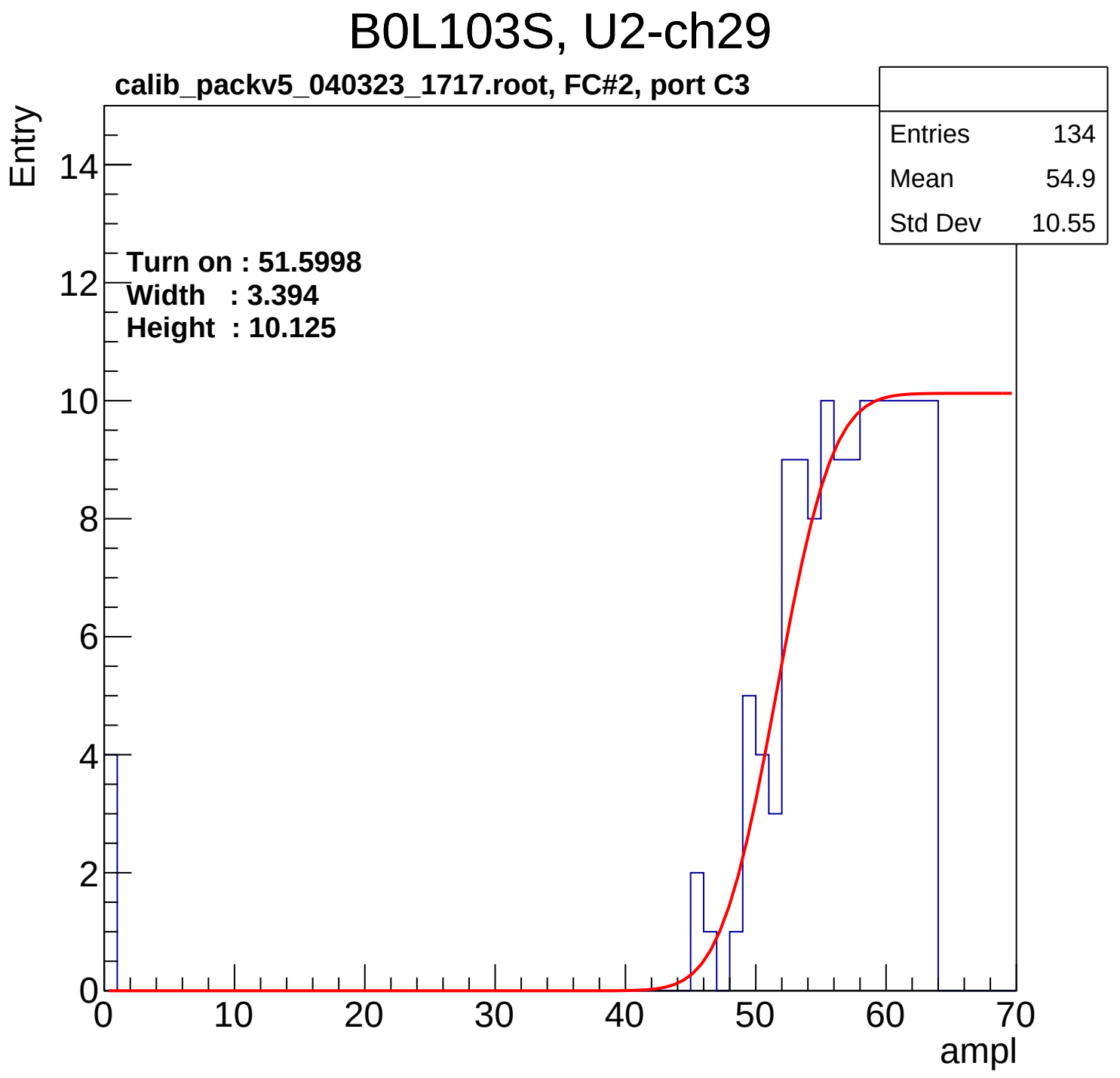
B0L103S, U2-ch29
calib_packv5_040323_1717.root, FC#2, port C3
Entries 134
Mean 54.9
Std Dev 10.55
Turn on : 51.5998
Width : 3.394
Height : 10.125
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ampl
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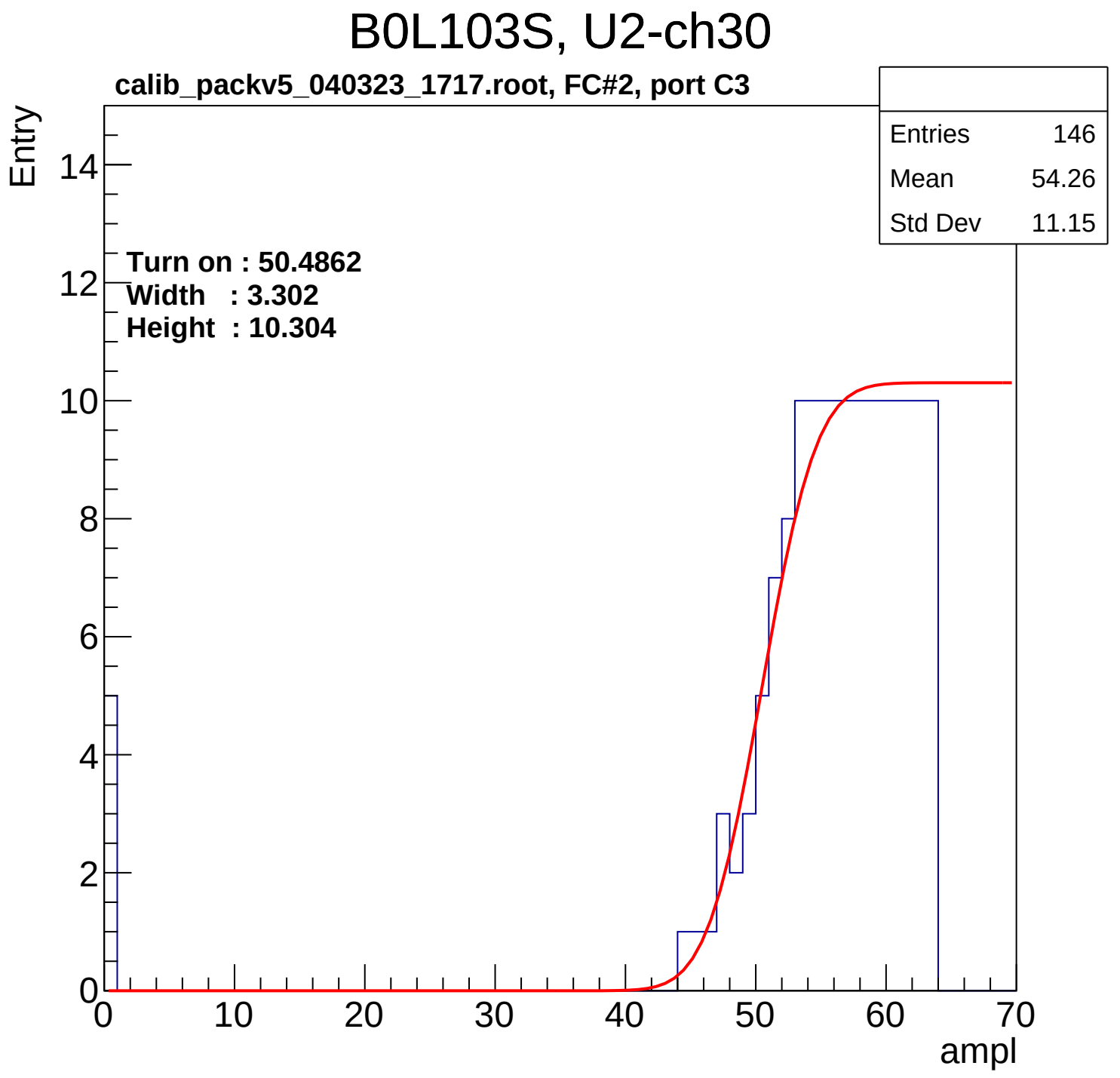
B0L103S, U2-ch30
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 54.26
Std Dev 11.15
Turn on : 50.4862
Width : 3.302
Height : 10.304
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ampl
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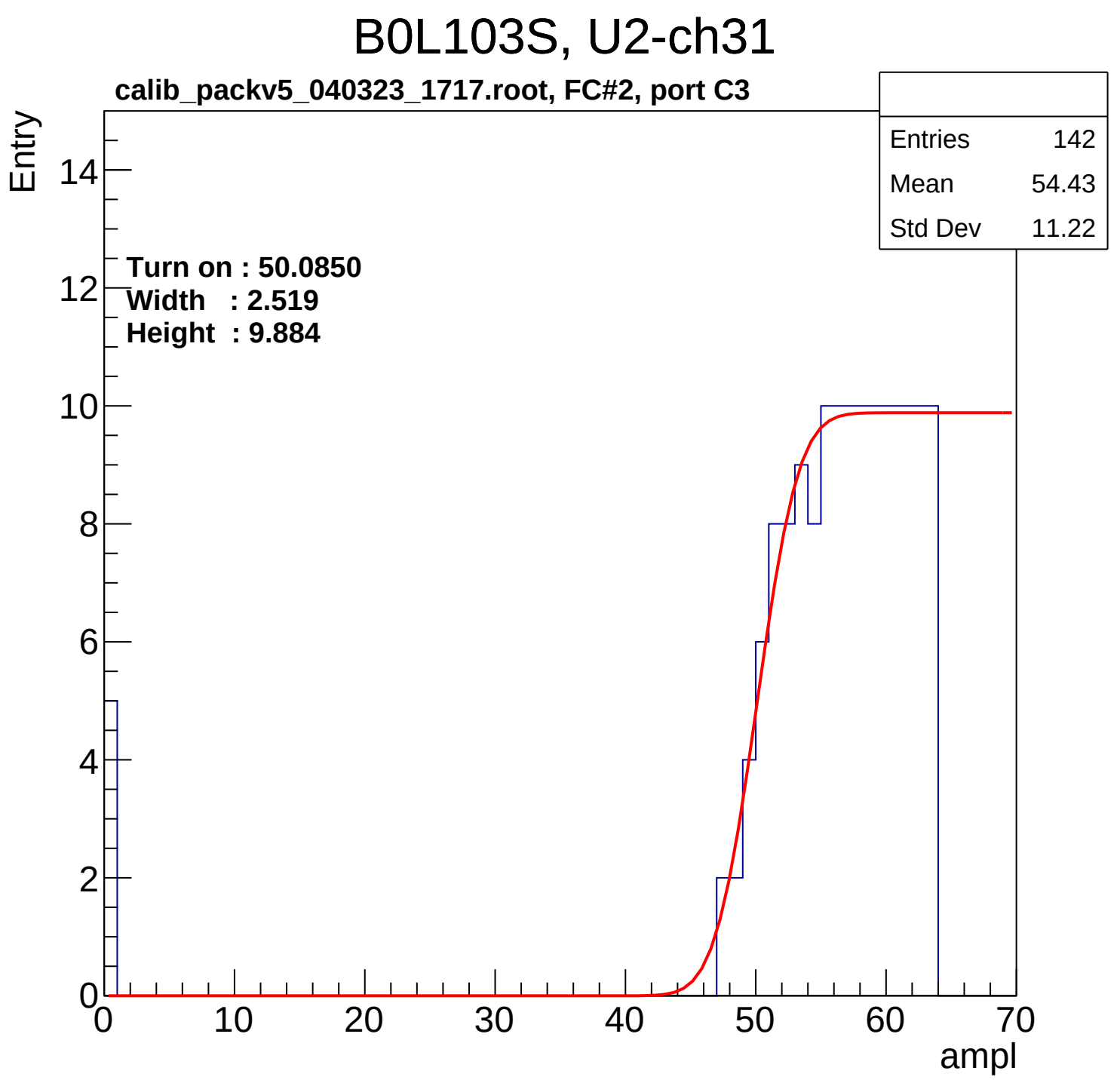
B0L103S, U2-ch31
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 54.43
Std Dev 11.22
Turn on : 50.0850
Width : 2.519
Height : 9.884
Entry
ampl
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6
8
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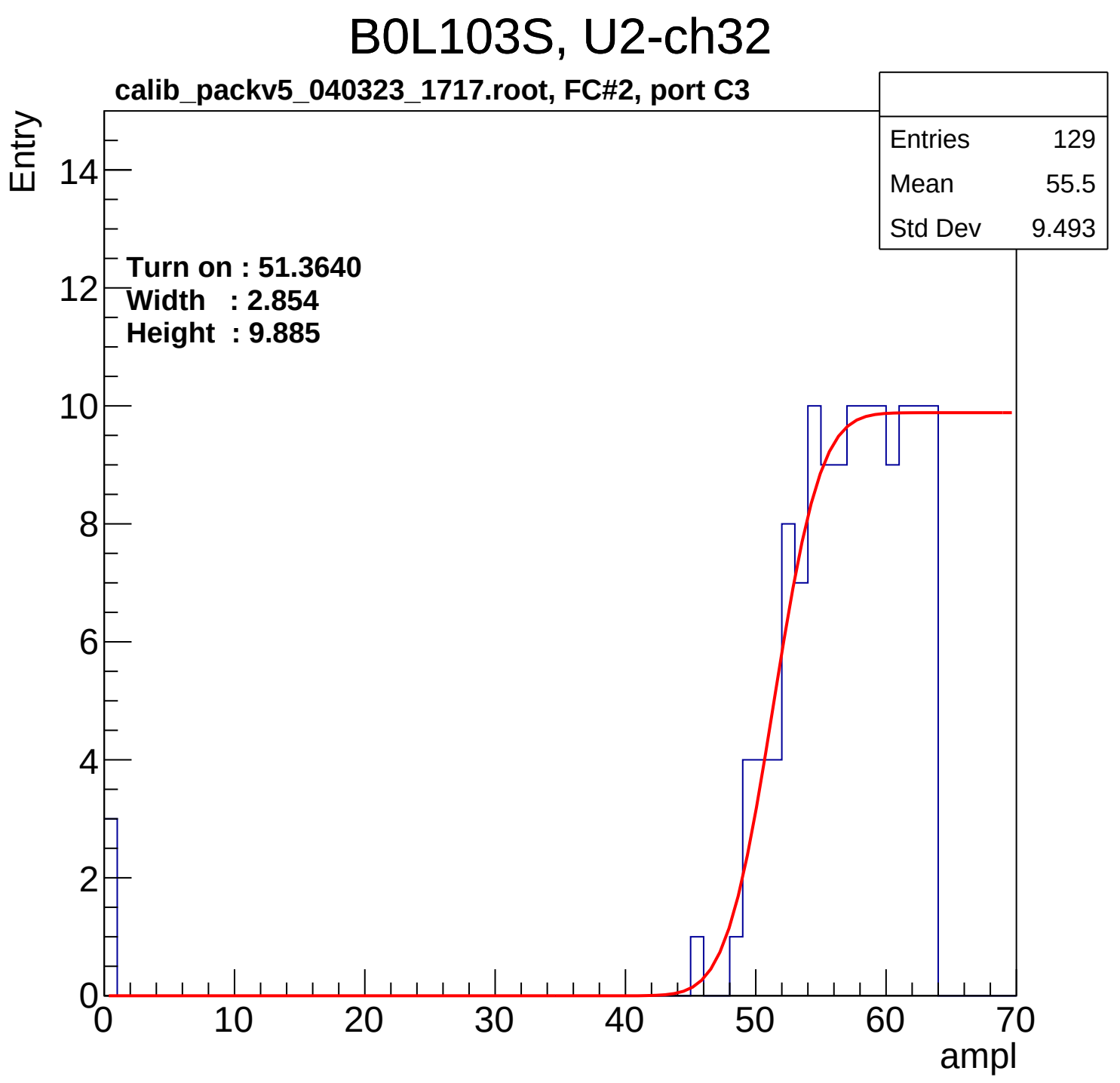
B0L103S, U2-ch32
calib_packv5_040323_1717.root, FC#2, port C3
Entries 129
Mean 55.5
Std Dev 9.493
Turn on : 51.3640
Width : 2.854
Height : 9.885
Entry
ampl
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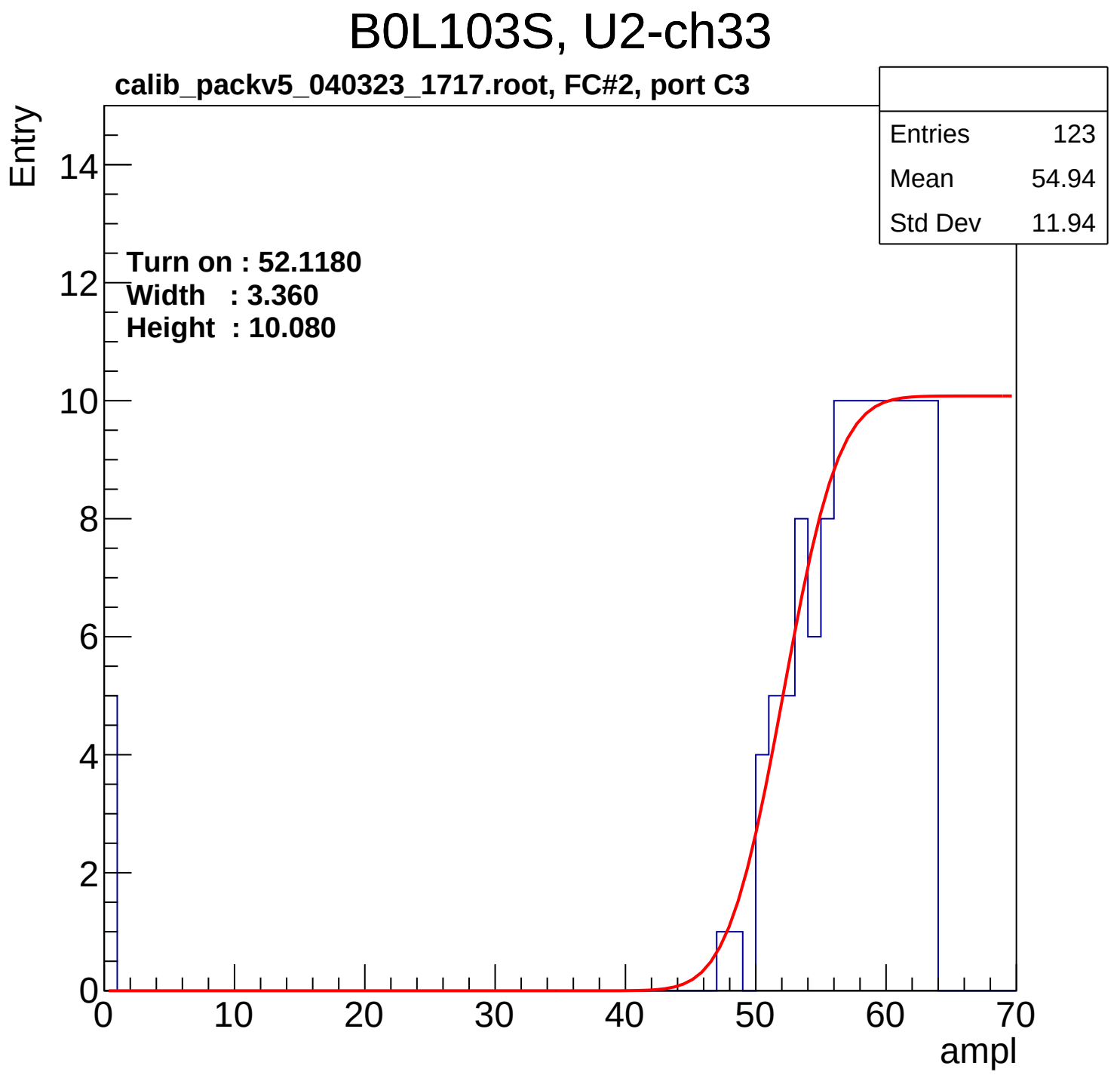
B0L103S, U2-ch33
calib_packv5_040323_1717.root, FC#2, port C3
Entries 123
Mean 54.94
Std Dev 11.94
Turn on : 52.1180
Width : 3.360
Height : 10.080
Entry
ampl
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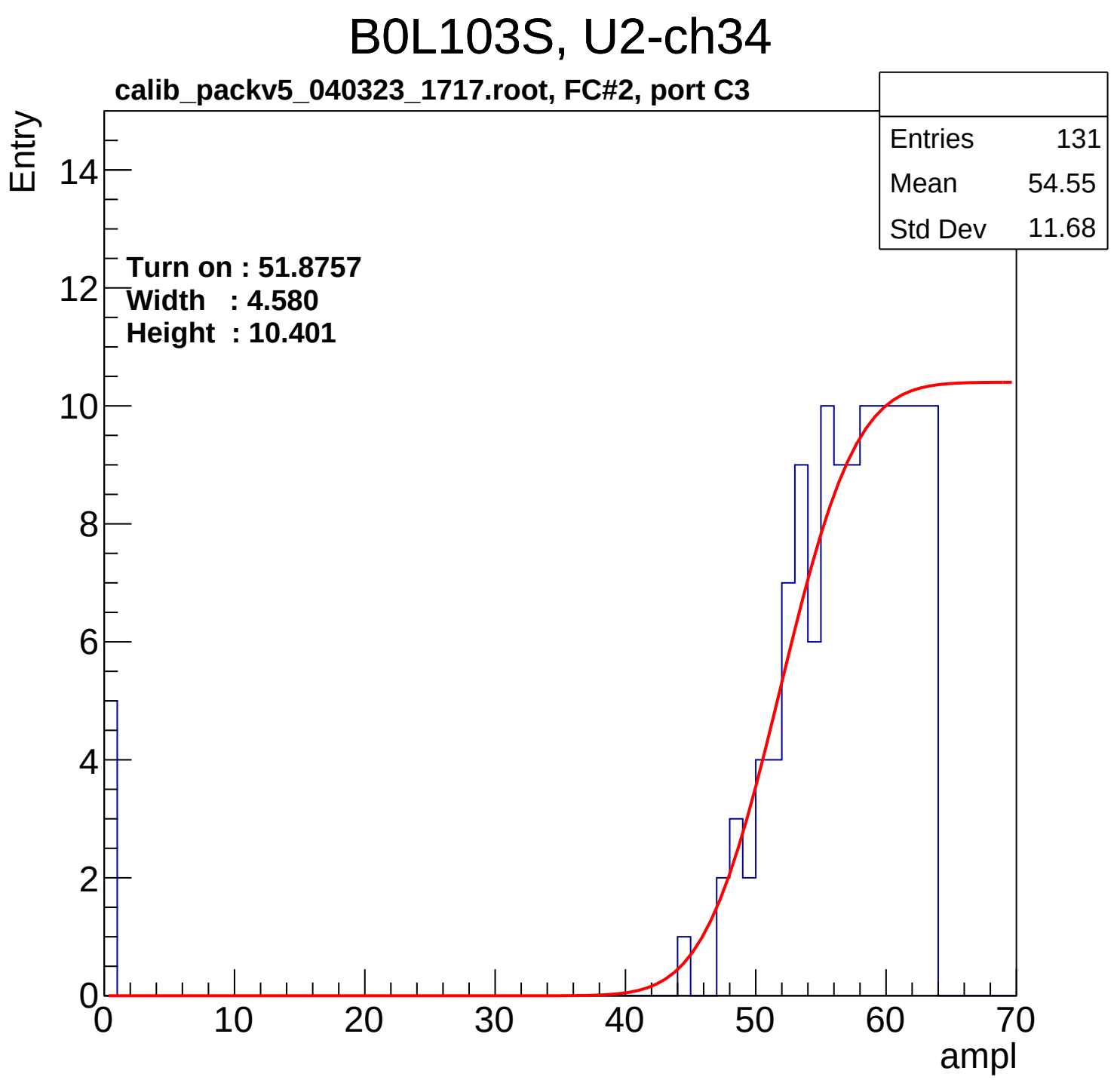
B0L103S, U2-ch34
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 54.55
Std Dev 11.68
Turn on : 51.8757
Width : 4.580
Height : 10.401
Entry
ampl
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6
8
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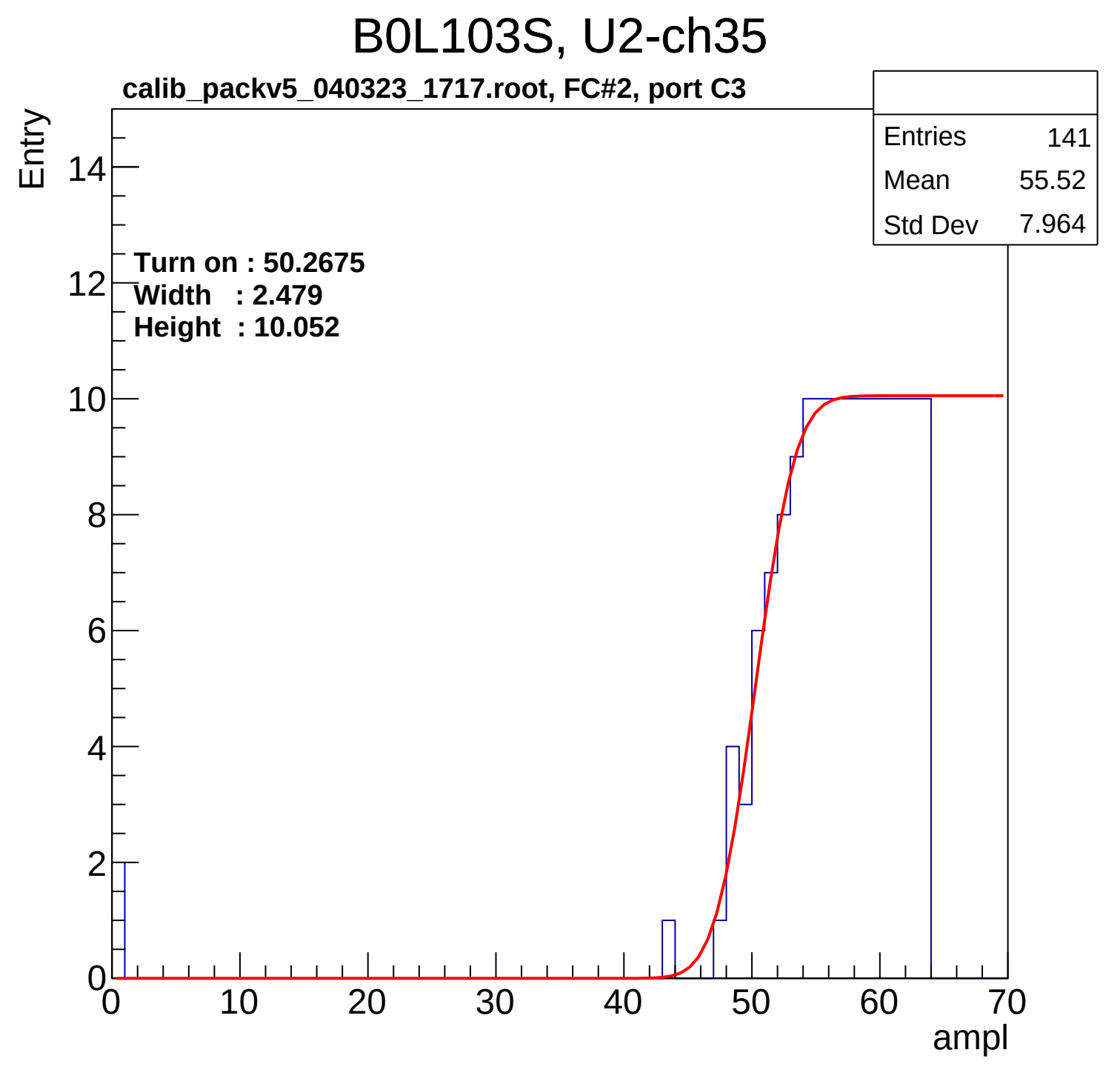
B0L103S, U2-ch35
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 55.52
Std Dev 7.964
Turn on : 50.2675
Width : 2.479
Height : 10.052
Entry
ampl
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4
6
8
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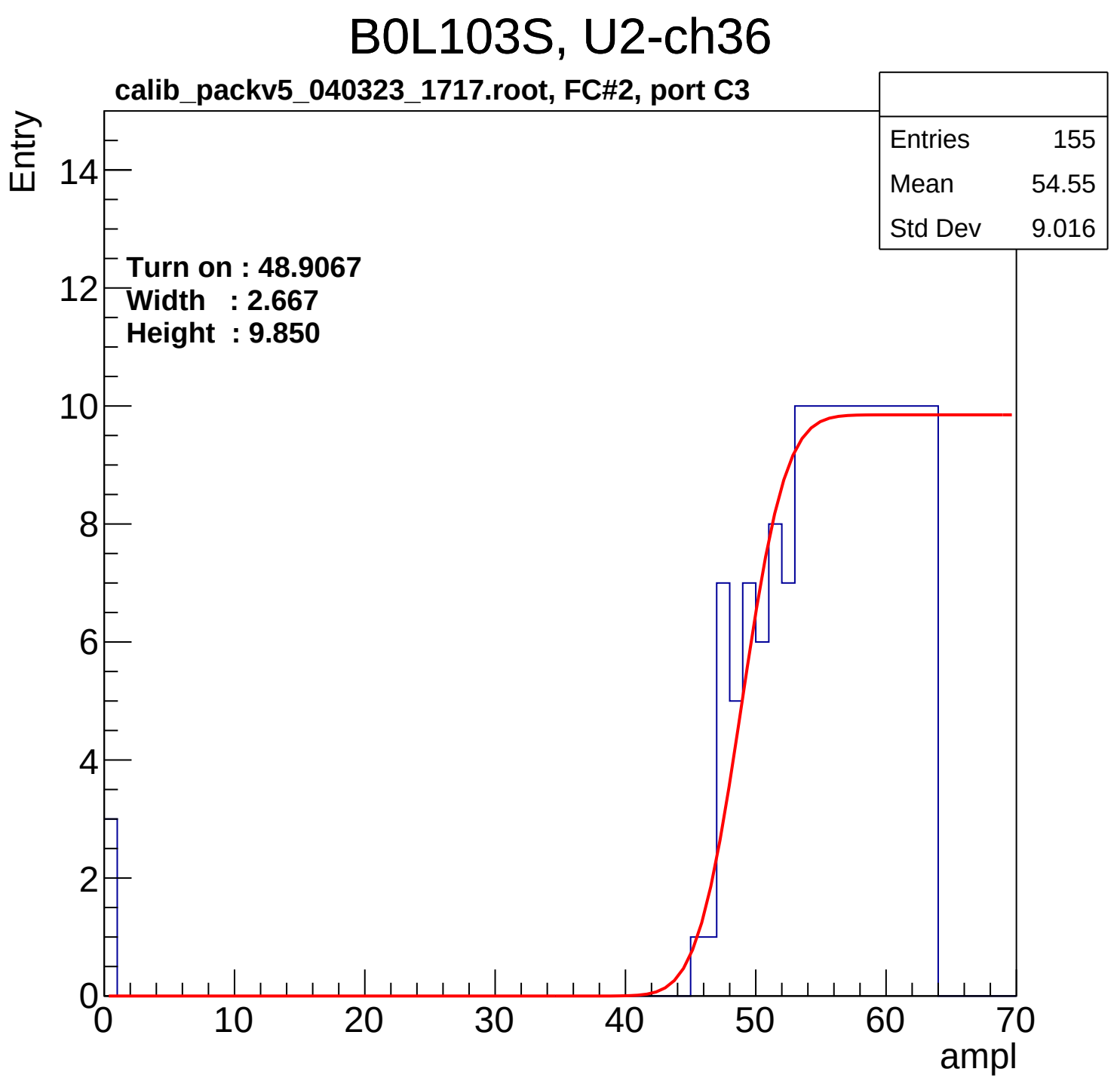
B0L103S, U2-ch36
calib_packv5_040323_1717.root, FC#2, port C3
Entries 155
Mean 54.55
Std Dev 9.016
Turn on : 48.9067
Width : 2.667
Height : 9.850
Entry
ampl
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4
6
8
10
12
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40
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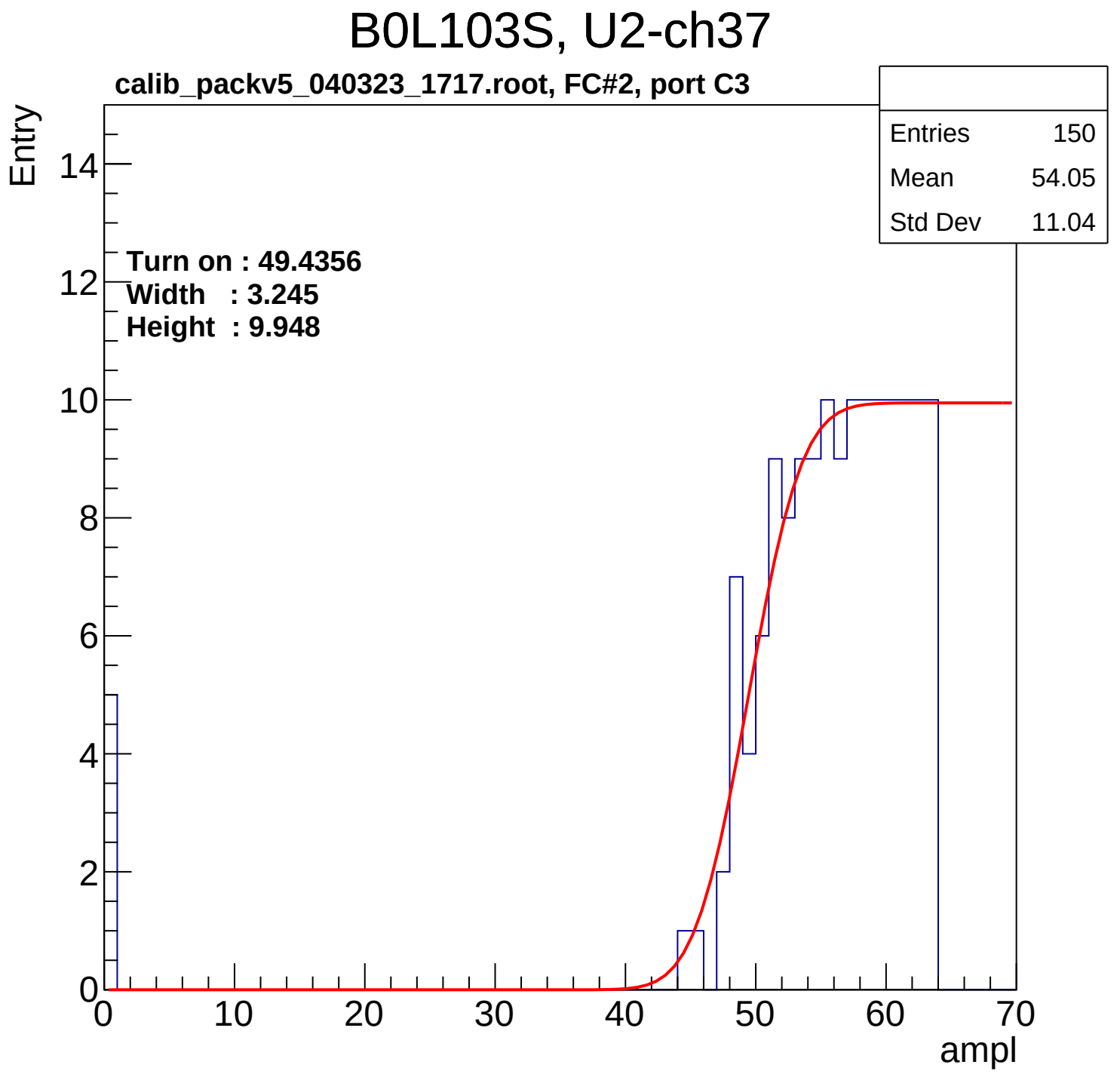
B0L103S, U2-ch37
calib_packv5_040323_1717.root, FC#2, port C3
Entries 150
Mean 54.05
Std Dev 11.04
Turn on : 49.4356
Width : 3.245
Height : 9.948
Entry
ampl
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8
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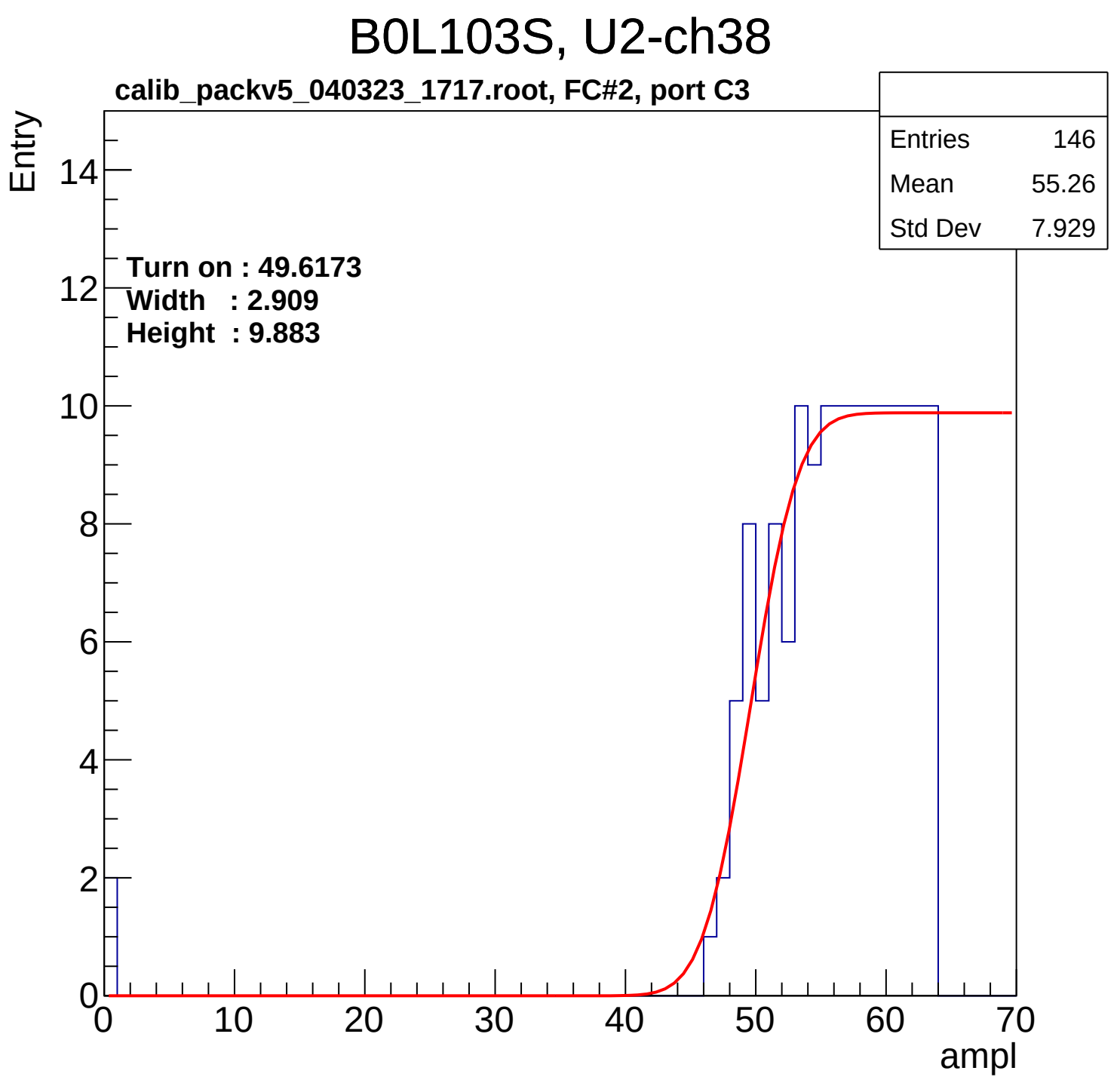
B0L103S, U2-ch38
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 55.26
Std Dev 7.929
Turn on : 49.6173
Width : 2.909
Height : 9.883
Entry
ampl
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2
4
6
8
10
12
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20
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40
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60
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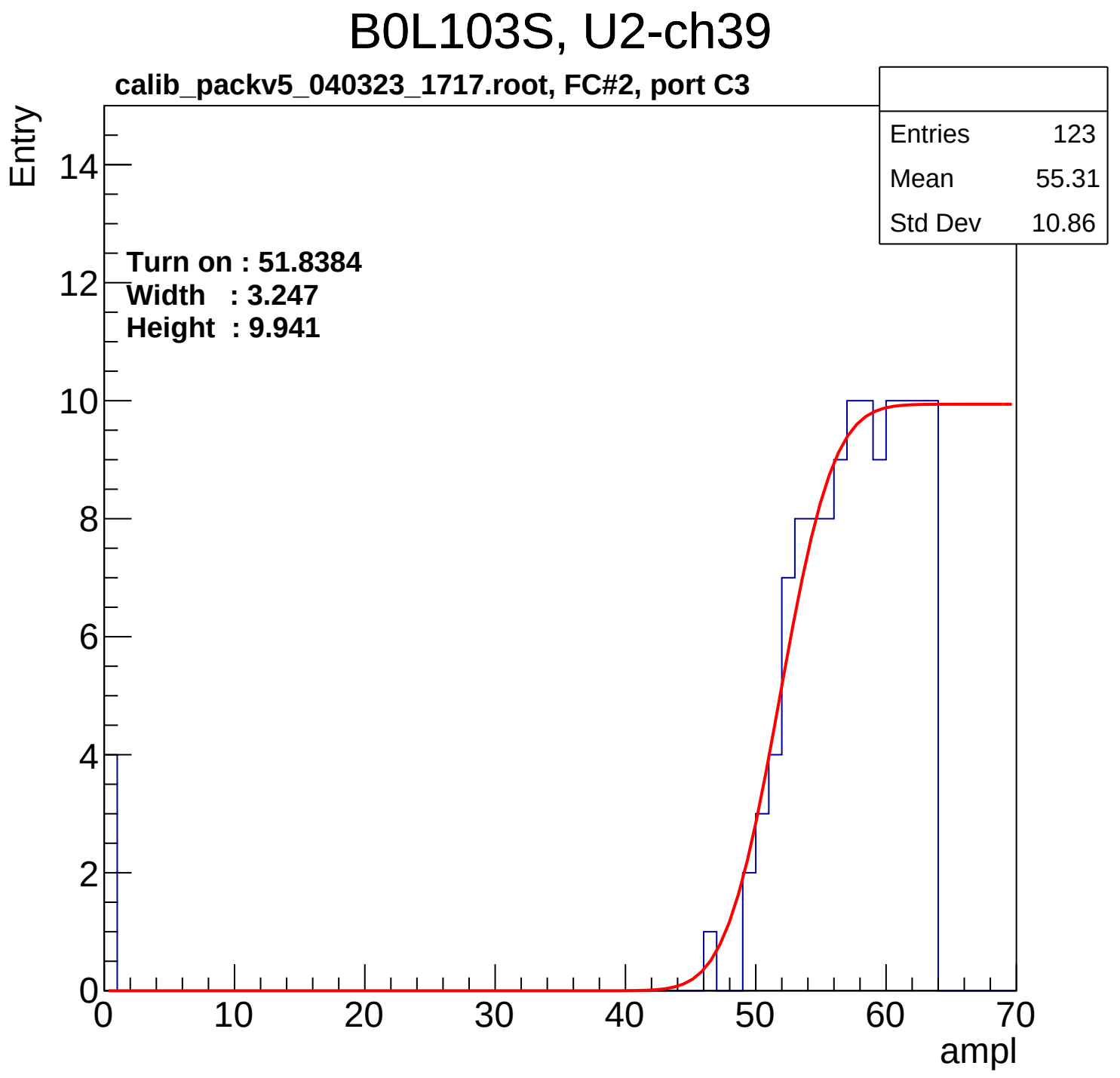
B0L103S, U2-ch39
calib_packv5_040323_1717.root, FC#2, port C3
Entries 123
Mean 55.31
Std Dev 10.86
Turn on : 51.8384
Width : 3.247
Height : 9.941
Entry
ampl
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6
8
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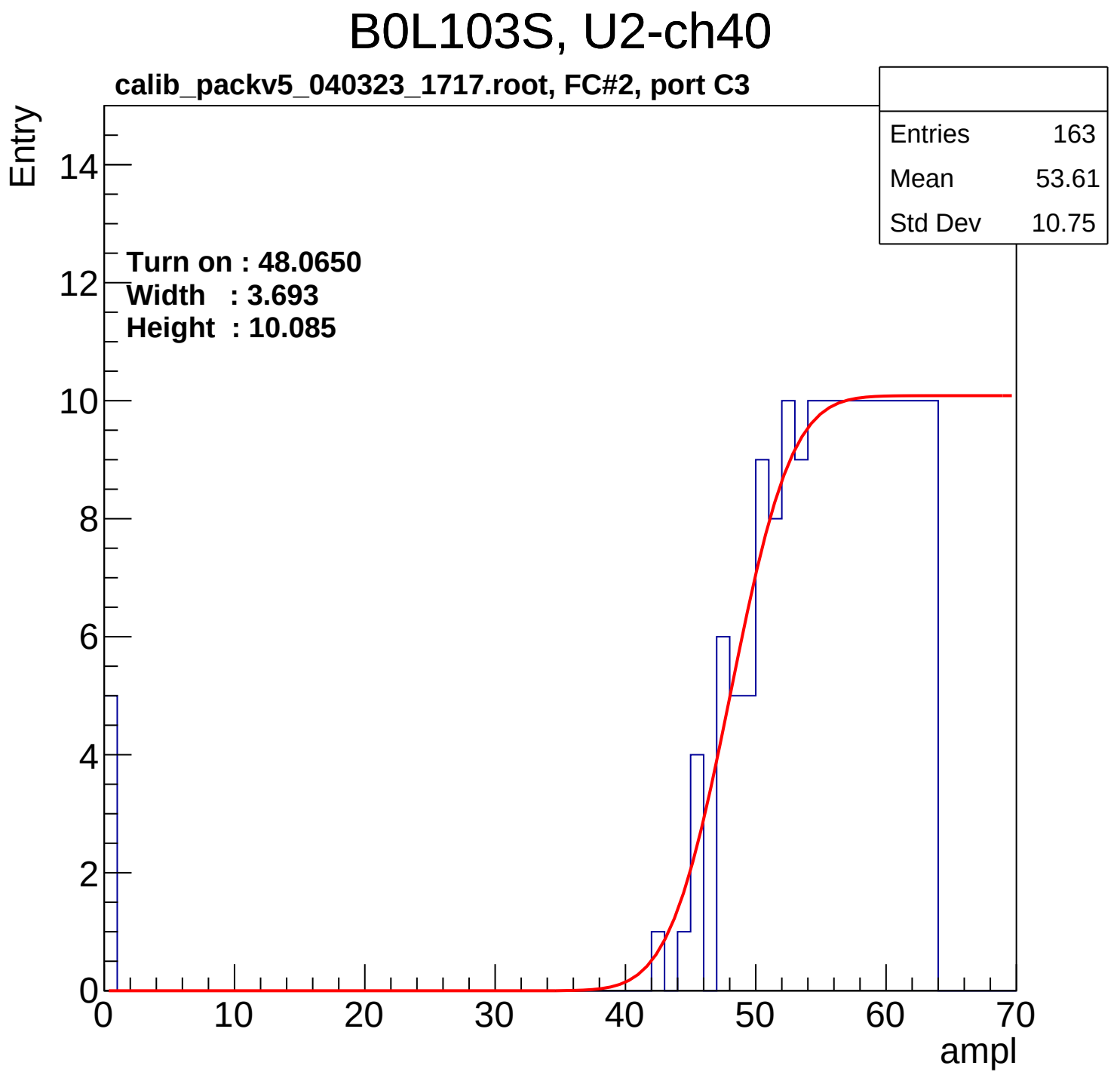
B0L103S, U2-ch40
calib_packv5_040323_1717.root, FC#2, port C3
Entries 163
Mean 53.61
Std Dev 10.75
Turn on : 48.0650
Width : 3.693
Height : 10.085
Entry
ampl
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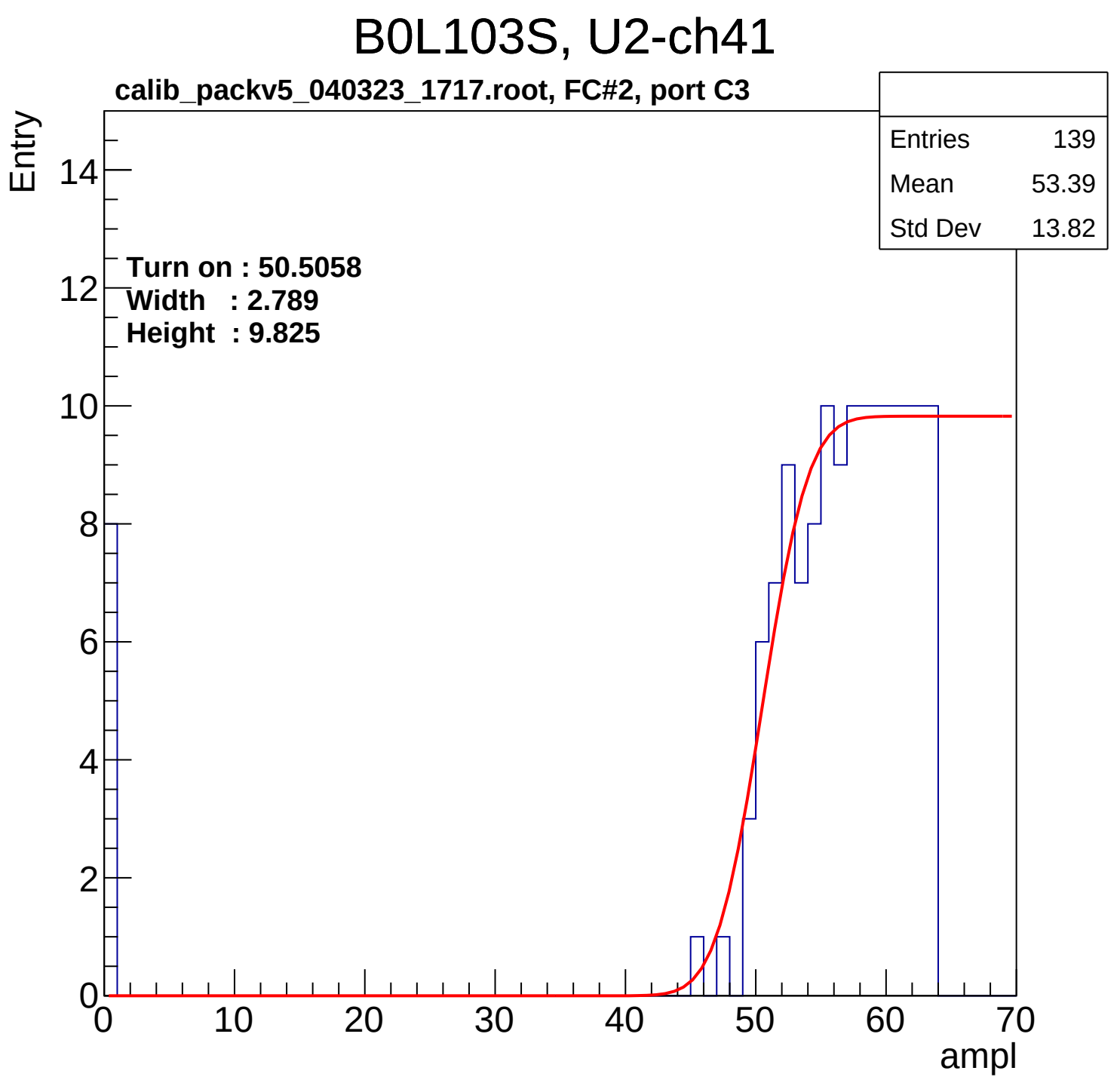
B0L103S, U2-ch41
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 53.39
Std Dev 13.82
Turn on : 50.5058
Width : 2.789
Height : 9.825
Entry
ampl
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6
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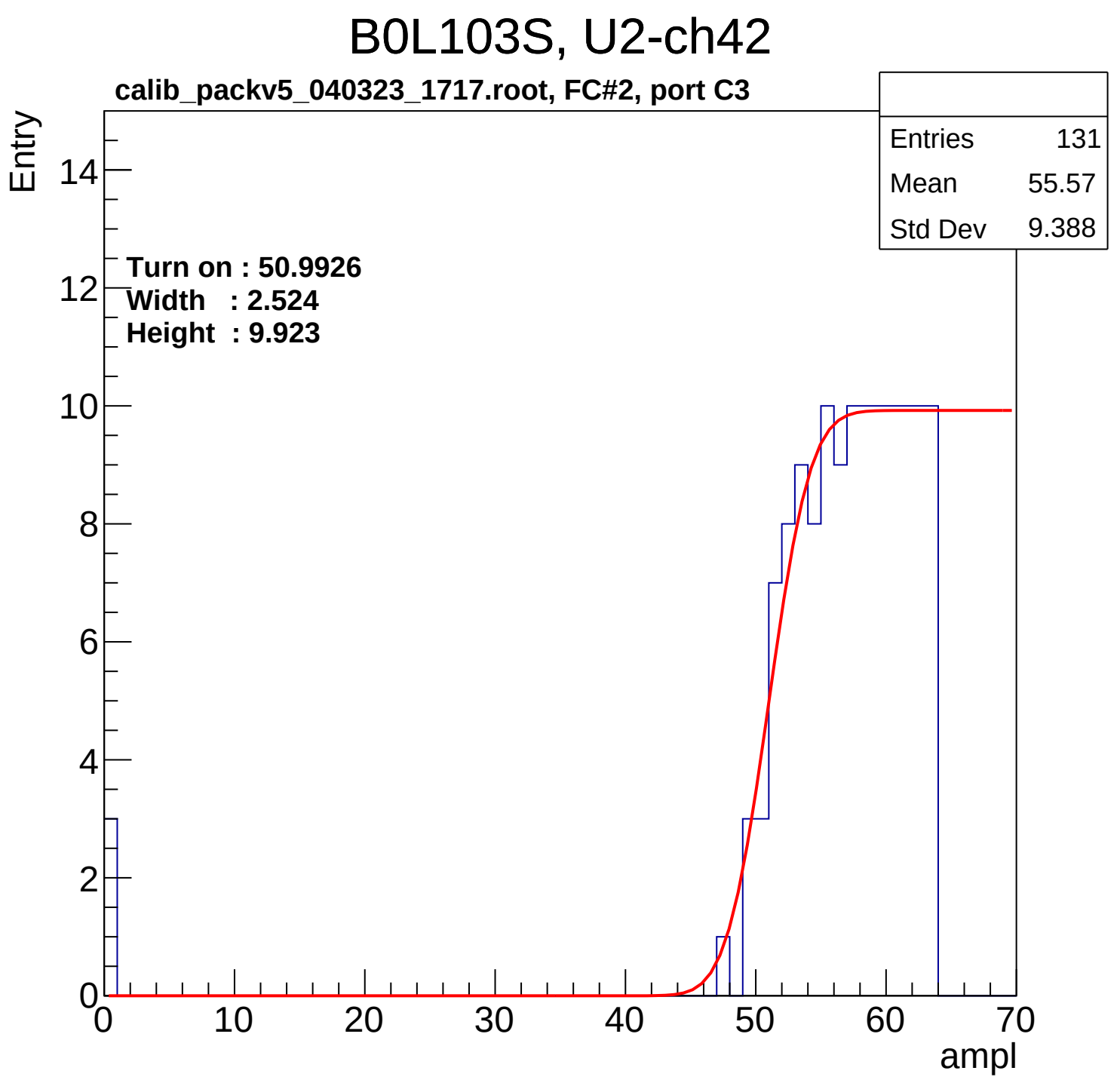
B0L103S, U2-ch42
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 55.57
Std Dev 9.388
Turn on : 50.9926
Width : 2.524
Height : 9.923
Entry
ampl
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2
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6
8
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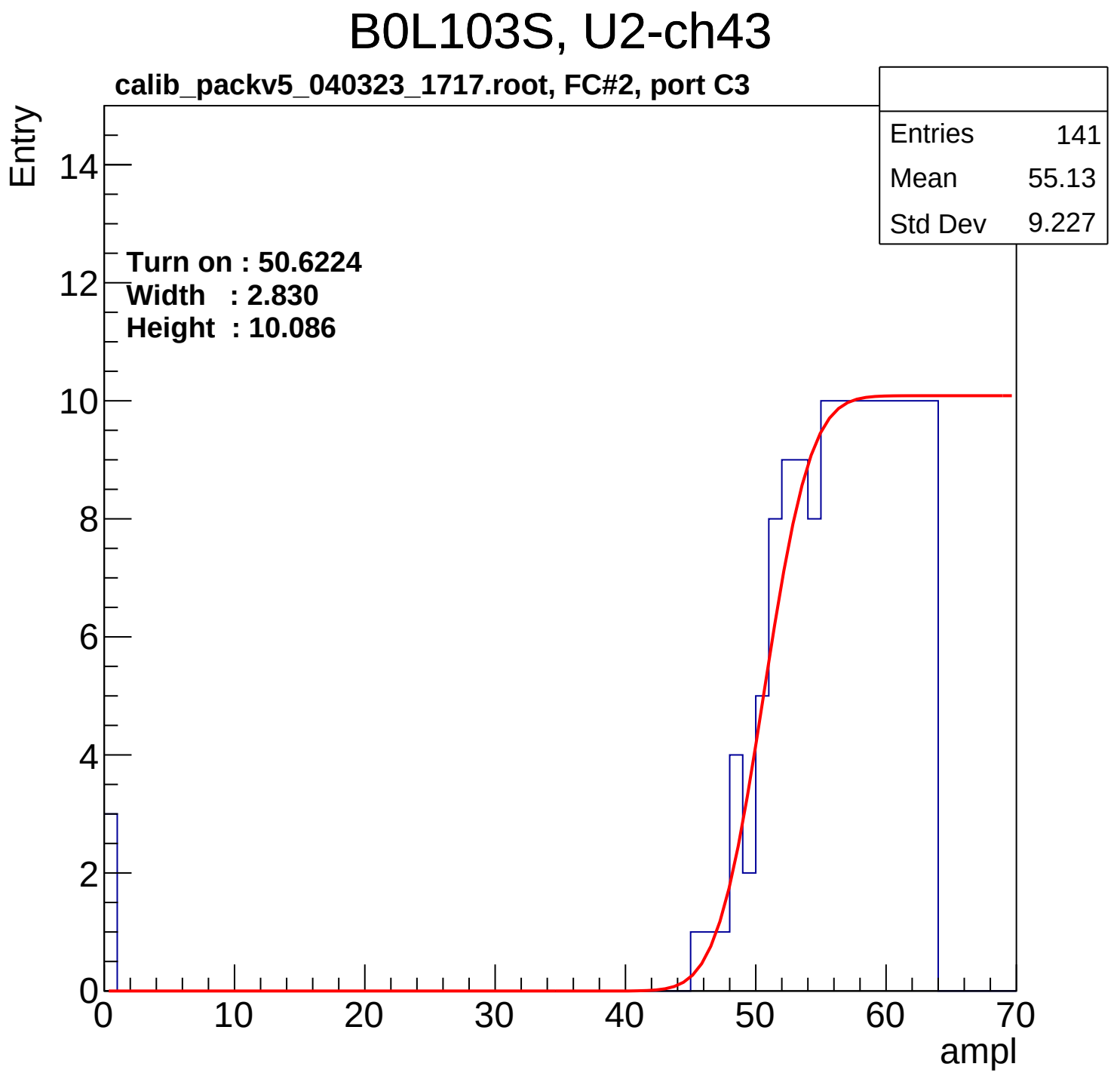
B0L103S, U2-ch43
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 55.13
Std Dev 9.227
Turn on : 50.6224
Width : 2.830
Height : 10.086
Entry
ampl
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6
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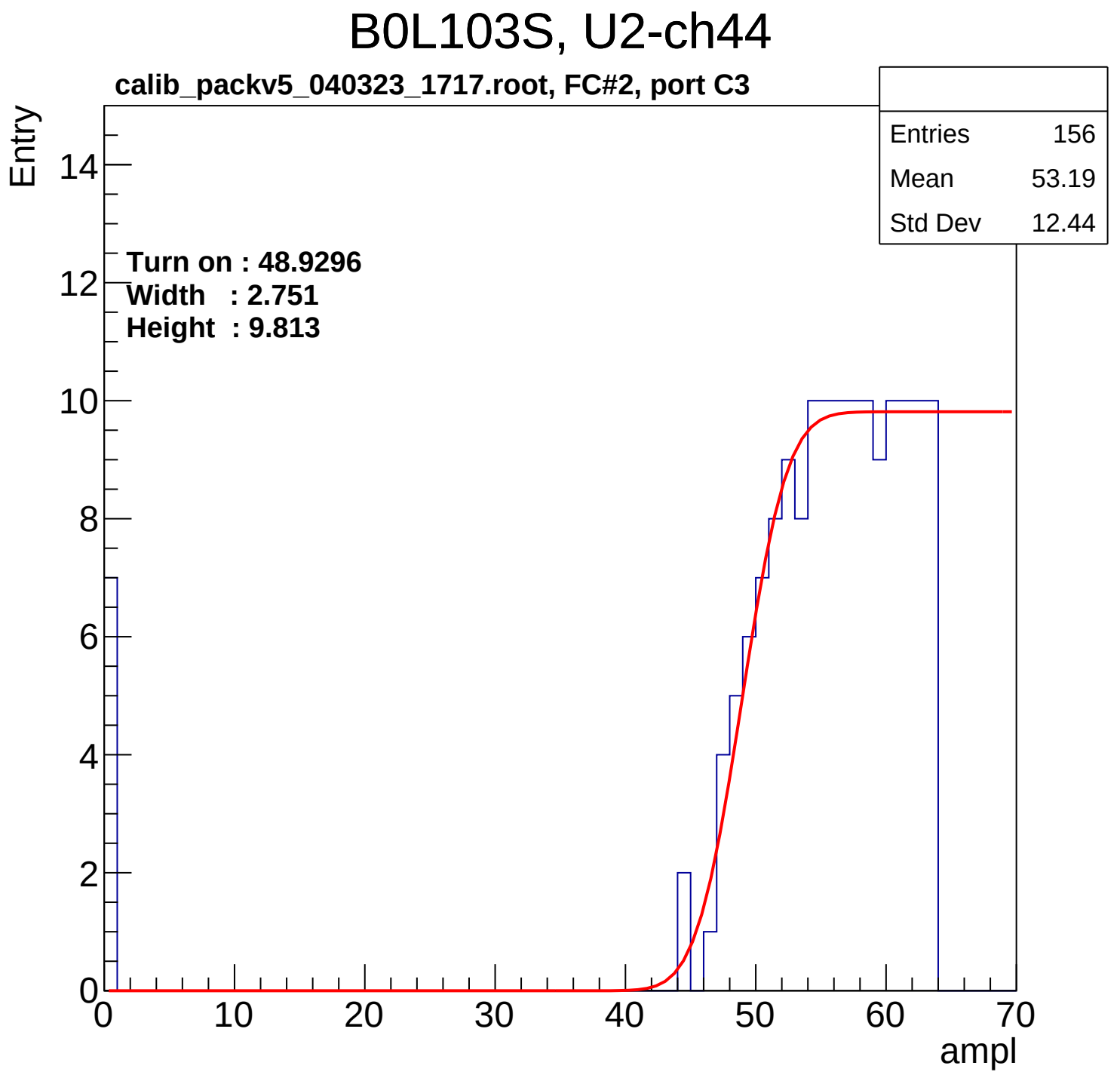
B0L103S, U2-ch44
calib_packv5_040323_1717.root, FC#2, port C3
Entries 156
Mean 53.19
Std Dev 12.44
Turn on : 48.9296
Width : 2.751
Height : 9.813
Entry
ampl
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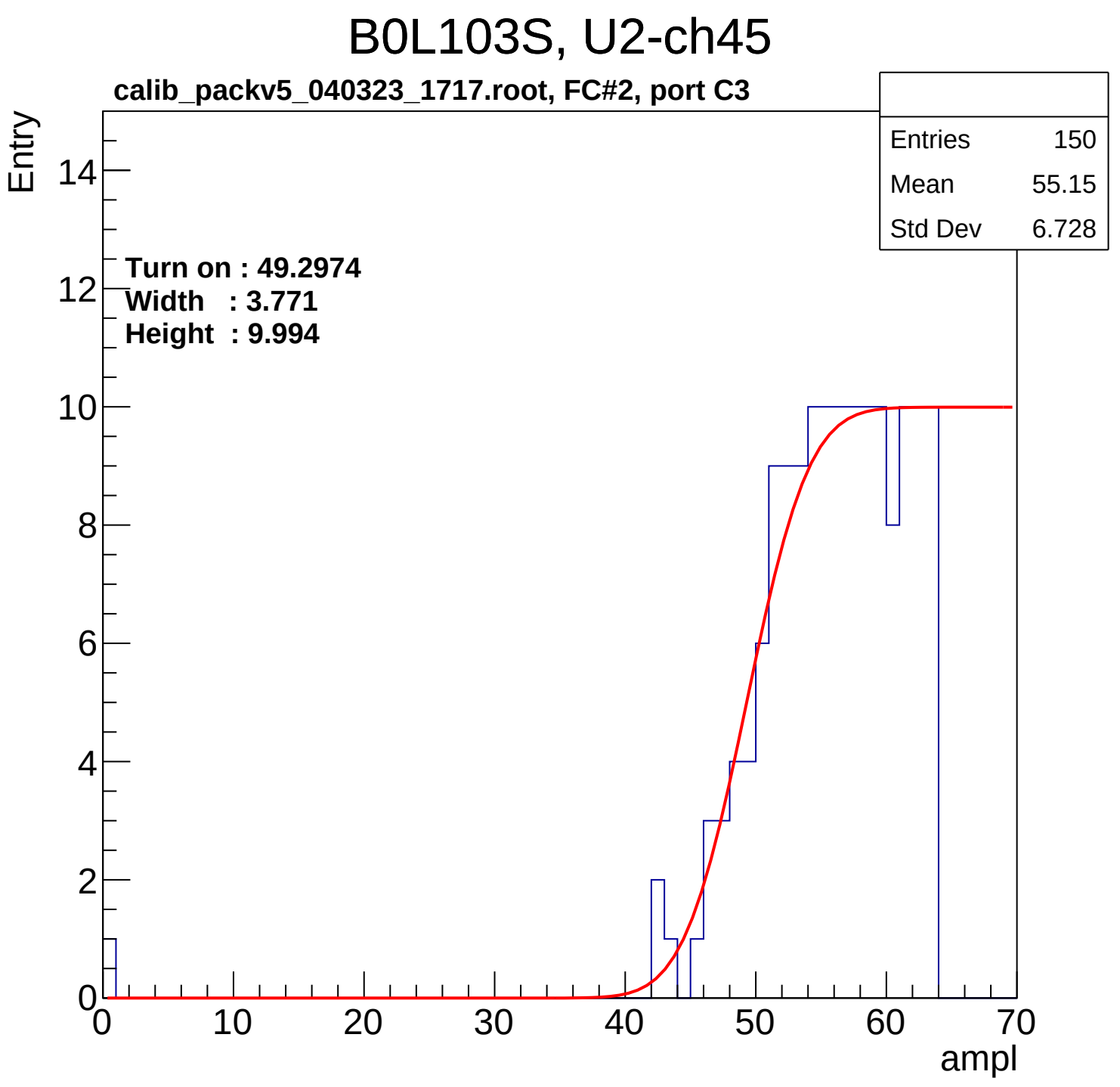
B0L103S, U2-ch45
calib_packv5_040323_1717.root, FC#2, port C3
Entries 150
Mean 55.15
Std Dev 6.728
Turn on : 49.2974
Width : 3.771
Height : 9.994
Entry
ampl
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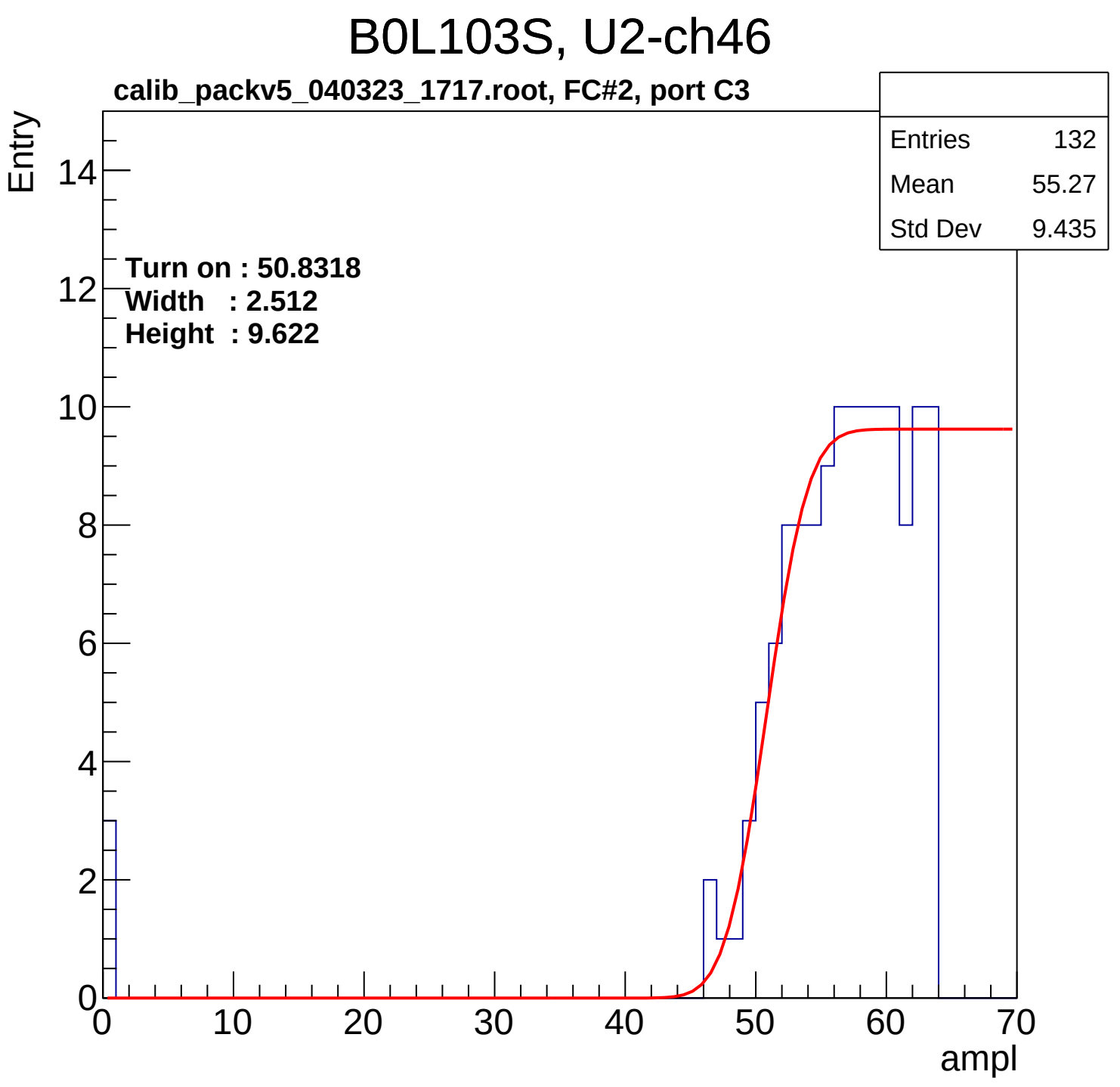
B0L103S, U2-ch46
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 55.27
Std Dev 9.435
Turn on : 50.8318
Width : 2.512
Height : 9.622
Entry
ampl
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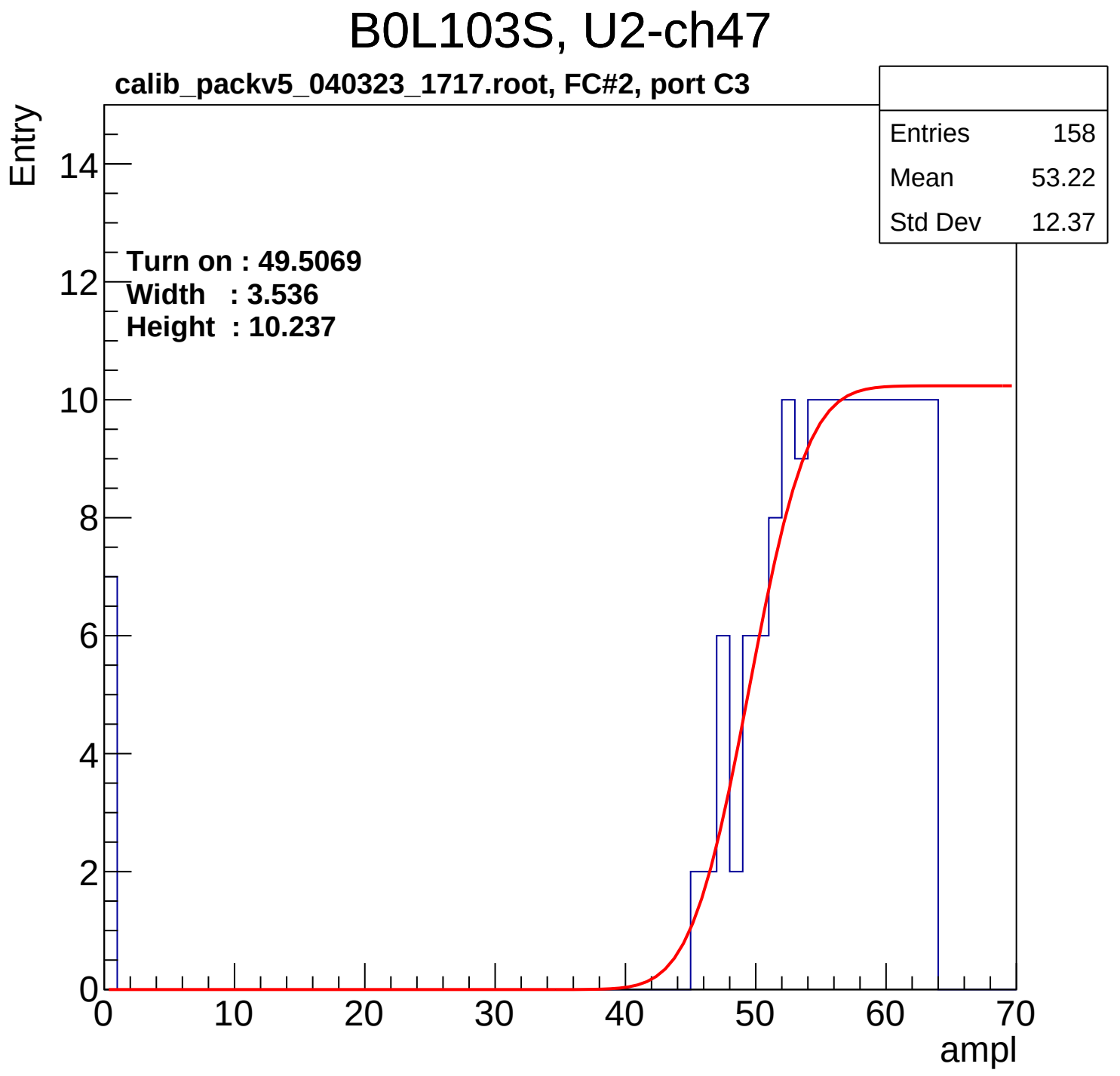
B0L103S, U2-ch47
calib_packv5_040323_1717.root, FC#2, port C3
Entries 158
Mean 53.22
Std Dev 12.37
Turn on : 49.5069
Width : 3.536
Height : 10.237
Entry
ampl
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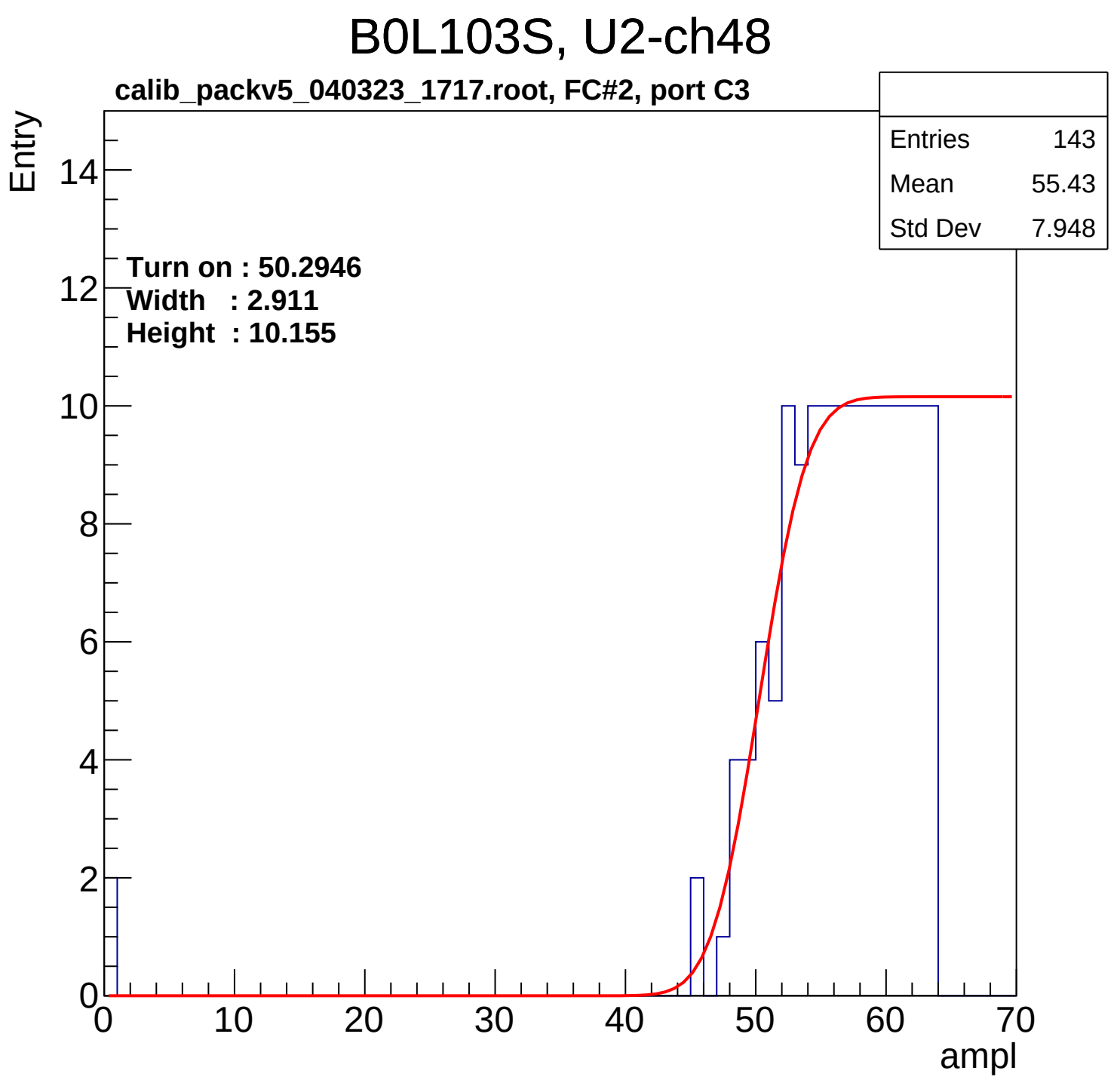
B0L103S, U2-ch48
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 55.43
Std Dev 7.948
Turn on : 50.2946
Width : 2.911
Height : 10.155
Entry
ampl
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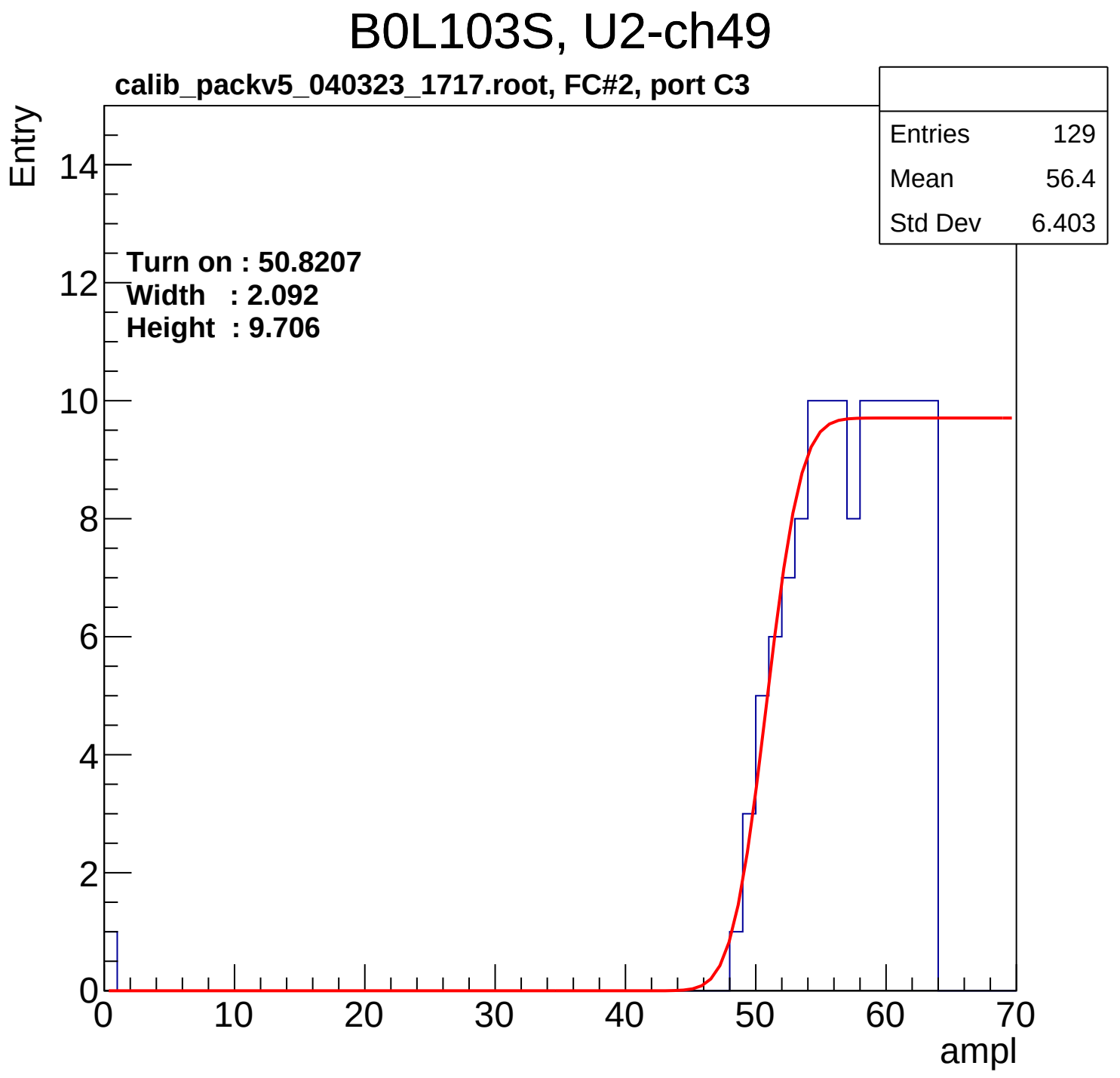
B0L103S, U2-ch49
calib_packv5_040323_1717.root, FC#2, port C3
Entries 129
Mean 56.4
Std Dev 6.403
Turn on : 50.8207
Width : 2.092
Height : 9.706
Entry
ampl
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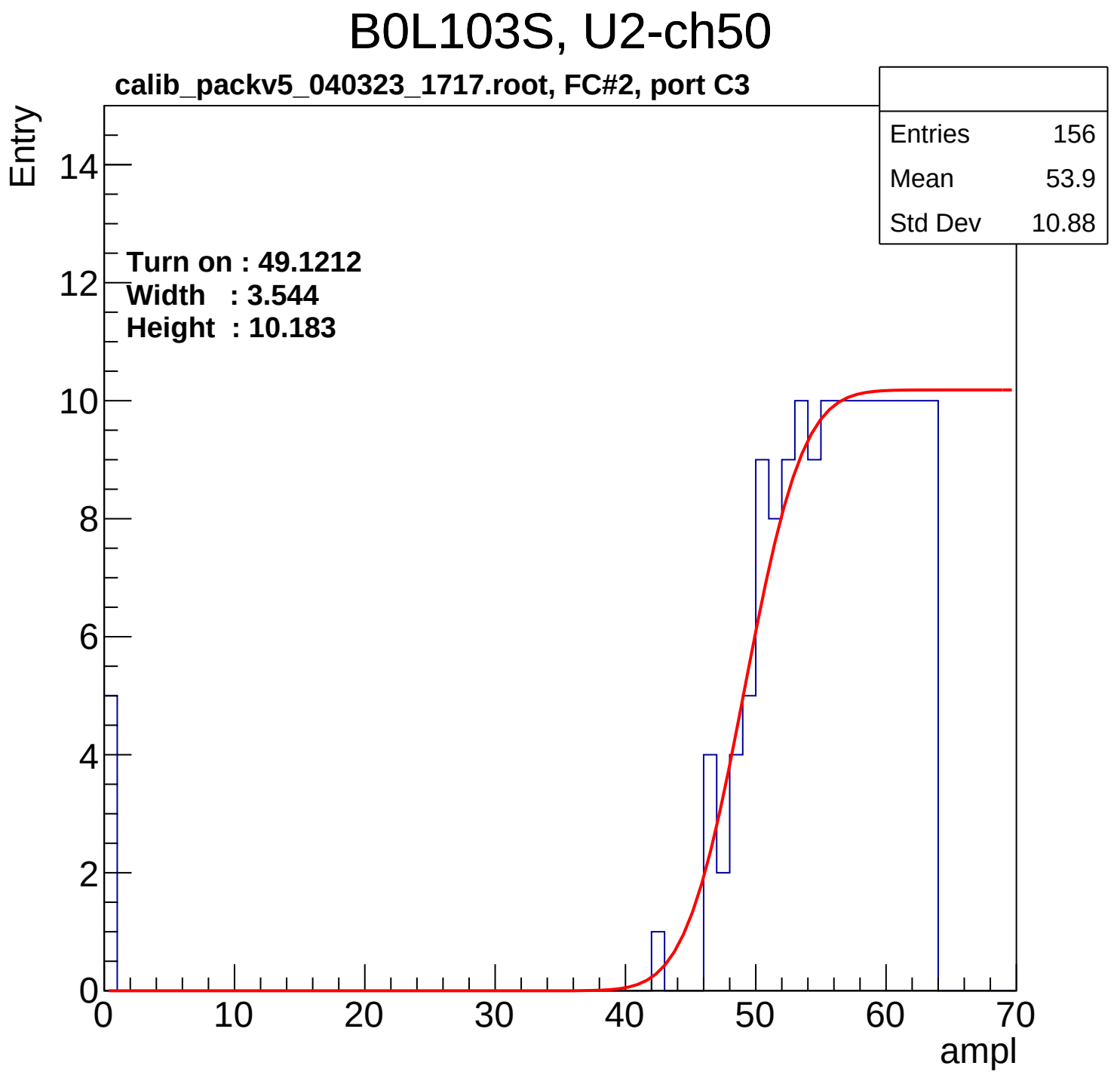
B0L103S, U2-ch50
calib_packv5_040323_1717.root, FC#2, port C3
Entries 156
Mean 53.9
Std Dev 10.88
Turn on : 49.1212
Width : 3.544
Height : 10.183
Entry
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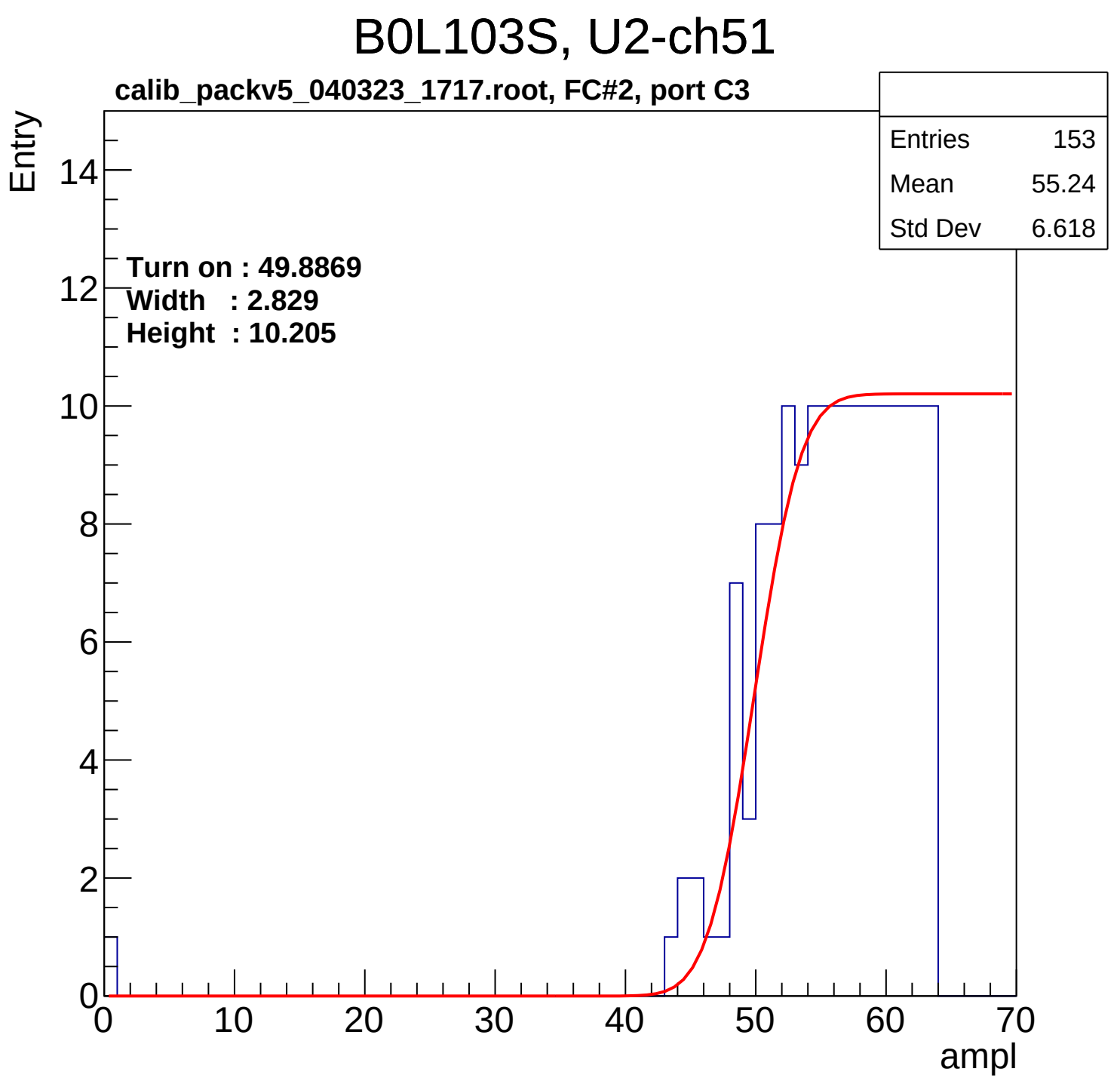
B0L103S, U2-ch51
calib_packv5_040323_1717.root, FC#2, port C3
Entries 153
Mean 55.24
Std Dev 6.618
Turn on : 49.8869
Width : 2.829
Height : 10.205
Entry
ampl
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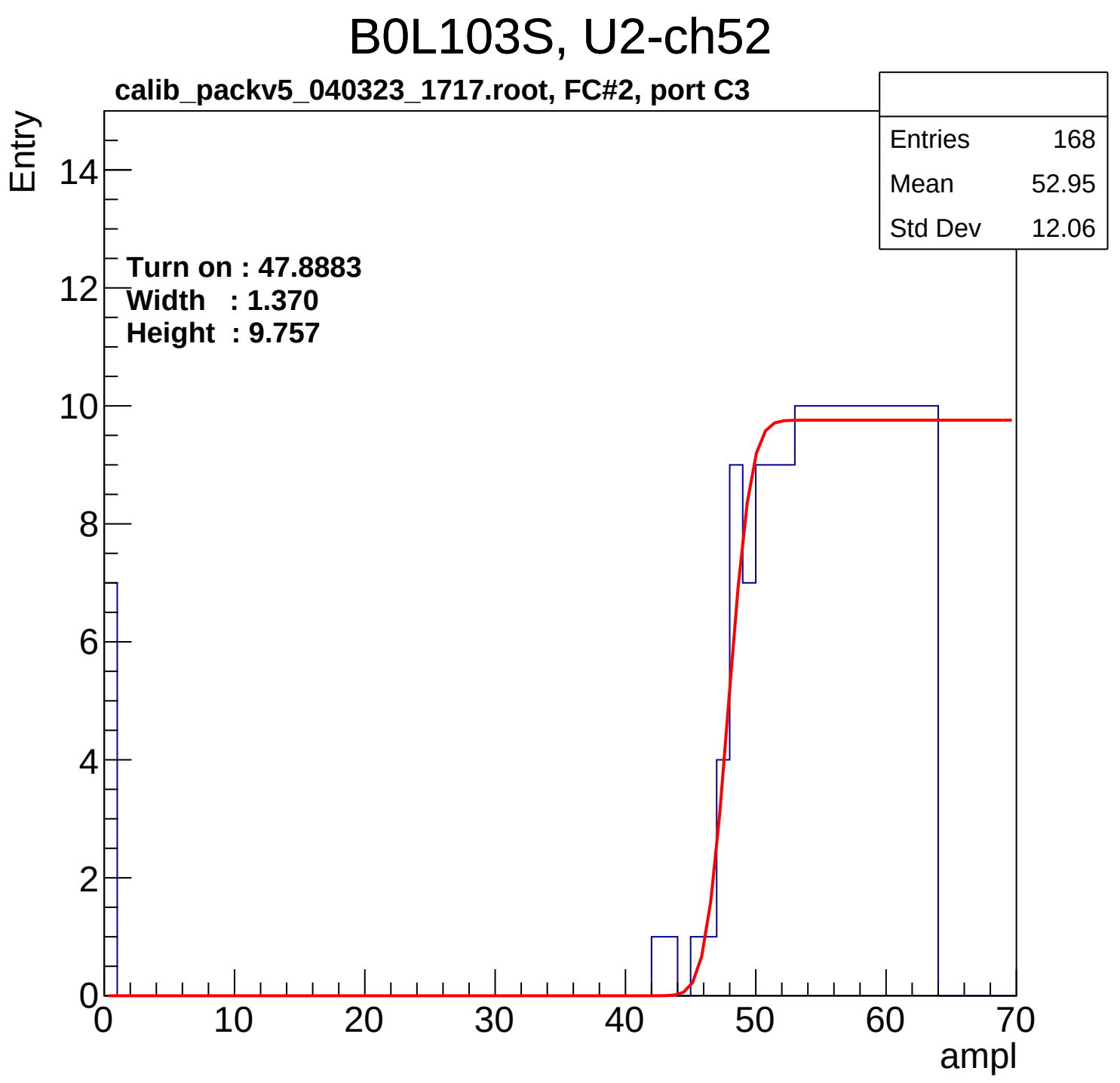
B0L103S, U2-ch52
calib_packv5_040323_1717.root, FC#2, port C3
Entries 168
Mean 52.95
Std Dev 12.06
Turn on : 47.8883
Width : 1.370
Height : 9.757
Entry
ampl
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8
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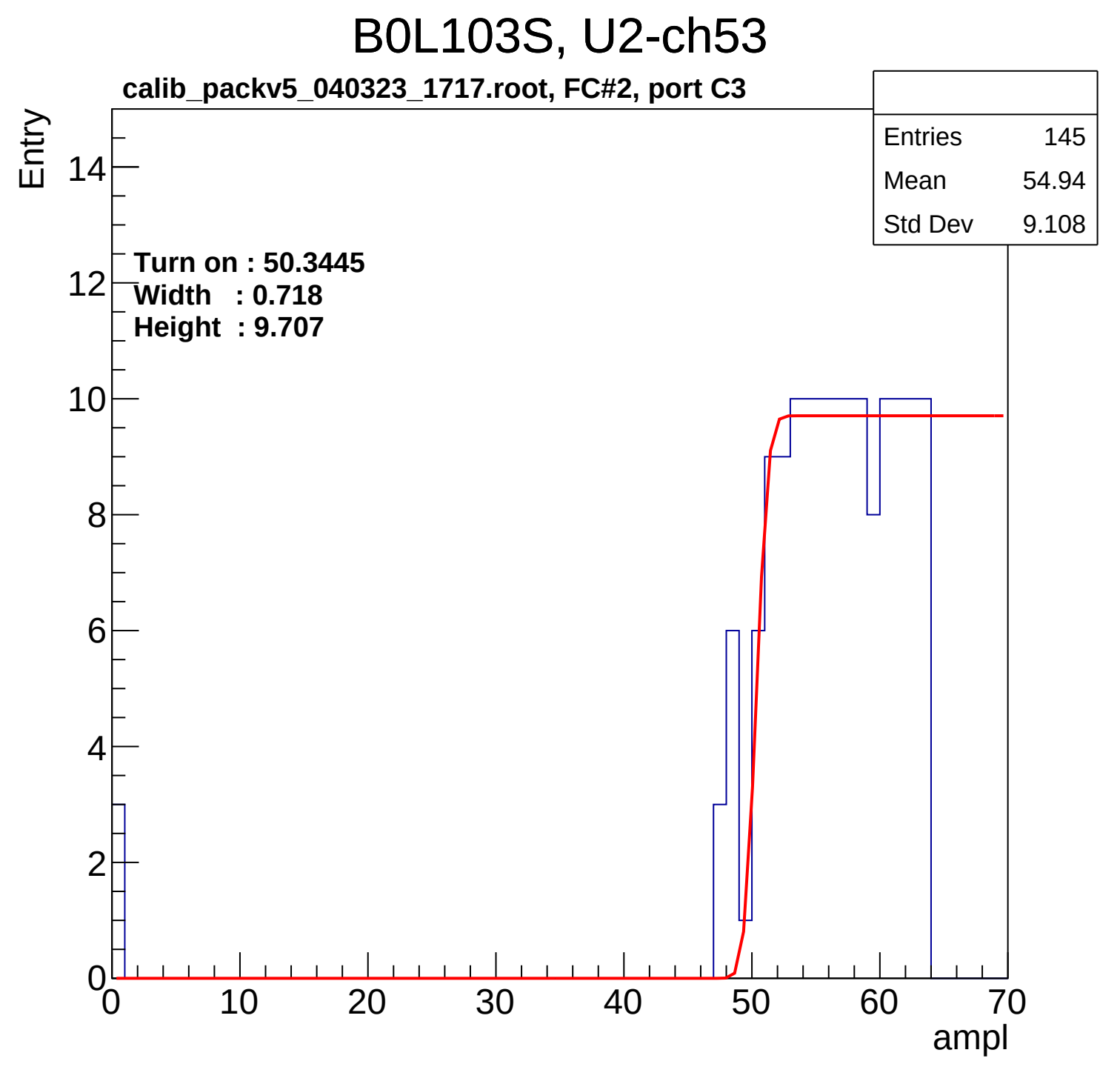
B0L103S, U2-ch53
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 54.94
Std Dev 9.108
Turn on : 50.3445
Width : 0.718
Height : 9.707
Entry
ampl
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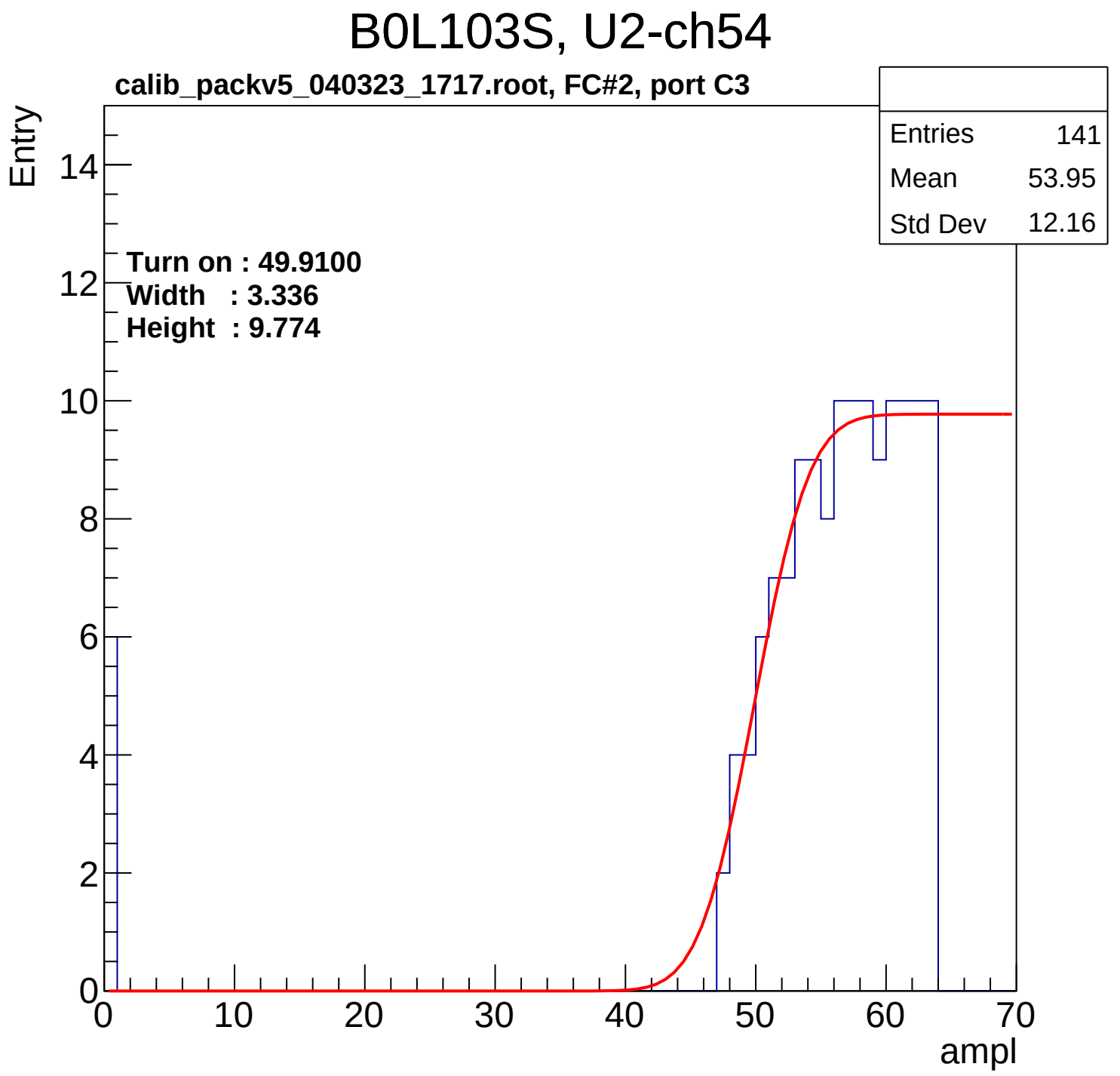
B0L103S, U2-ch54
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 53.95
Std Dev 12.16
Turn on : 49.9100
Width : 3.336
Height : 9.774
Entry
ampl
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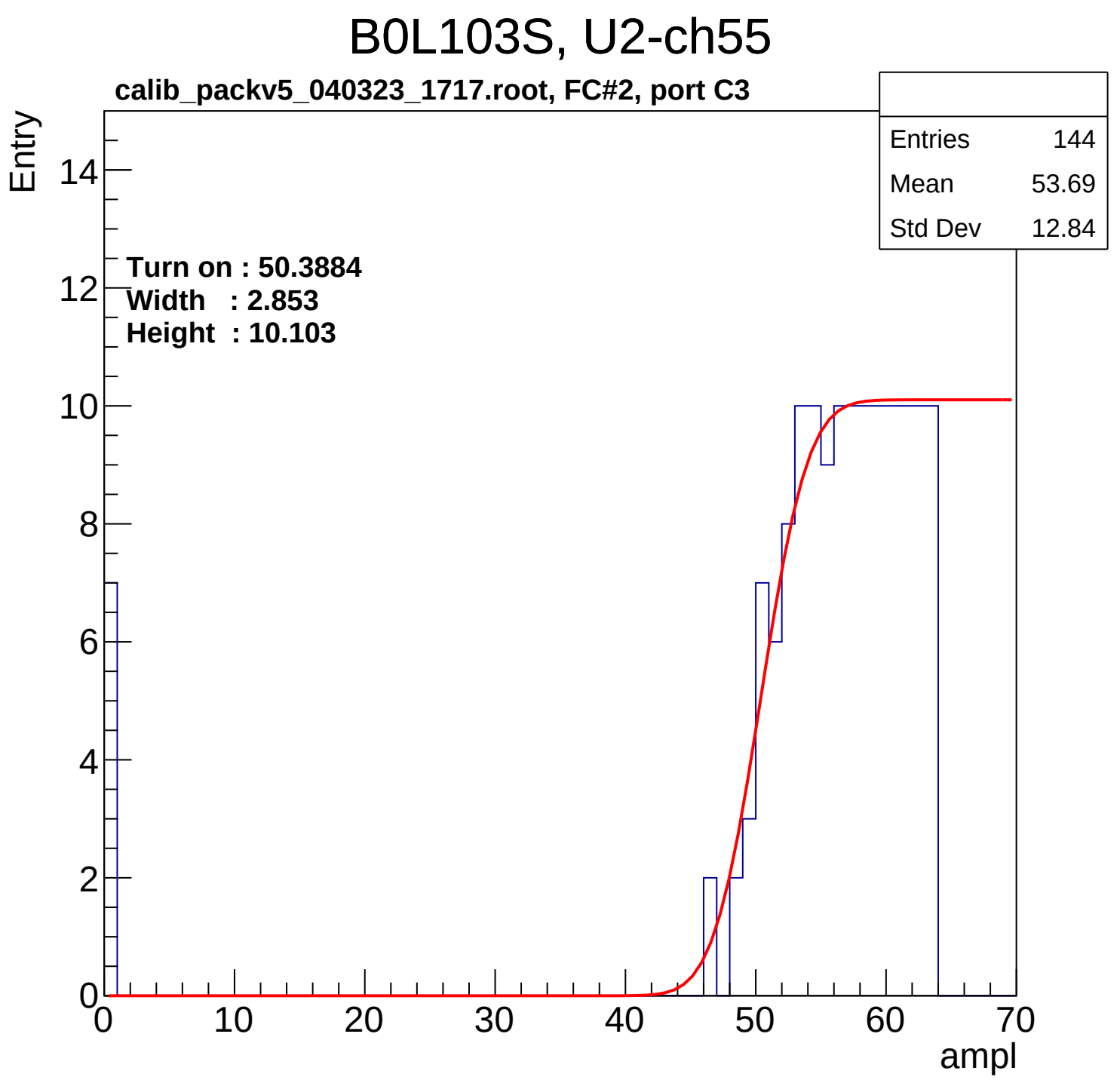
B0L103S, U2-ch55
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 53.69
Std Dev 12.84
Turn on : 50.3884
Width : 2.853
Height : 10.103
Entry
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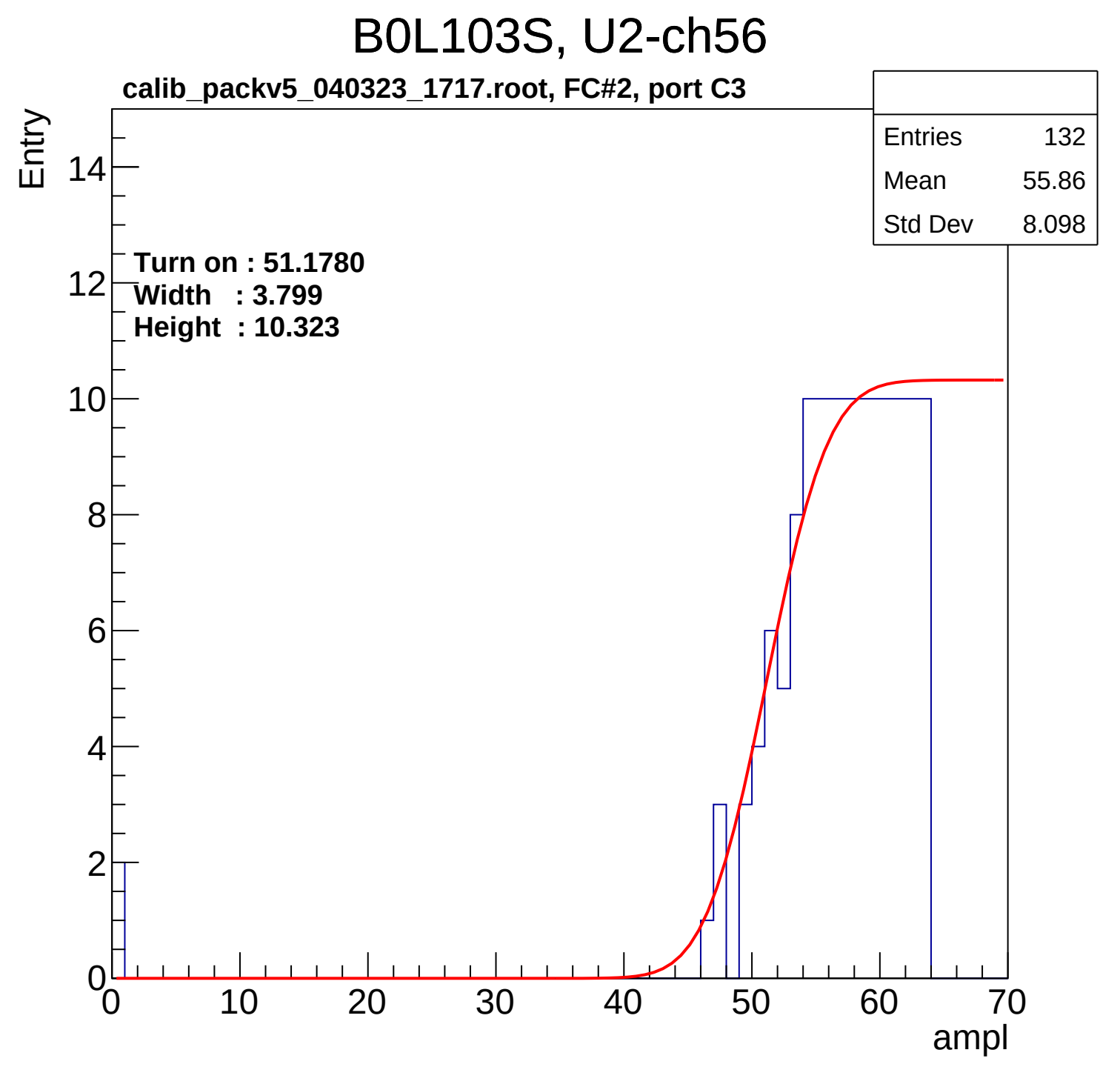
B0L103S, U2-ch56
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 55.86
Std Dev 8.098
Turn on : 51.1780
Width : 3.799
Height : 10.323
Entry
ampl
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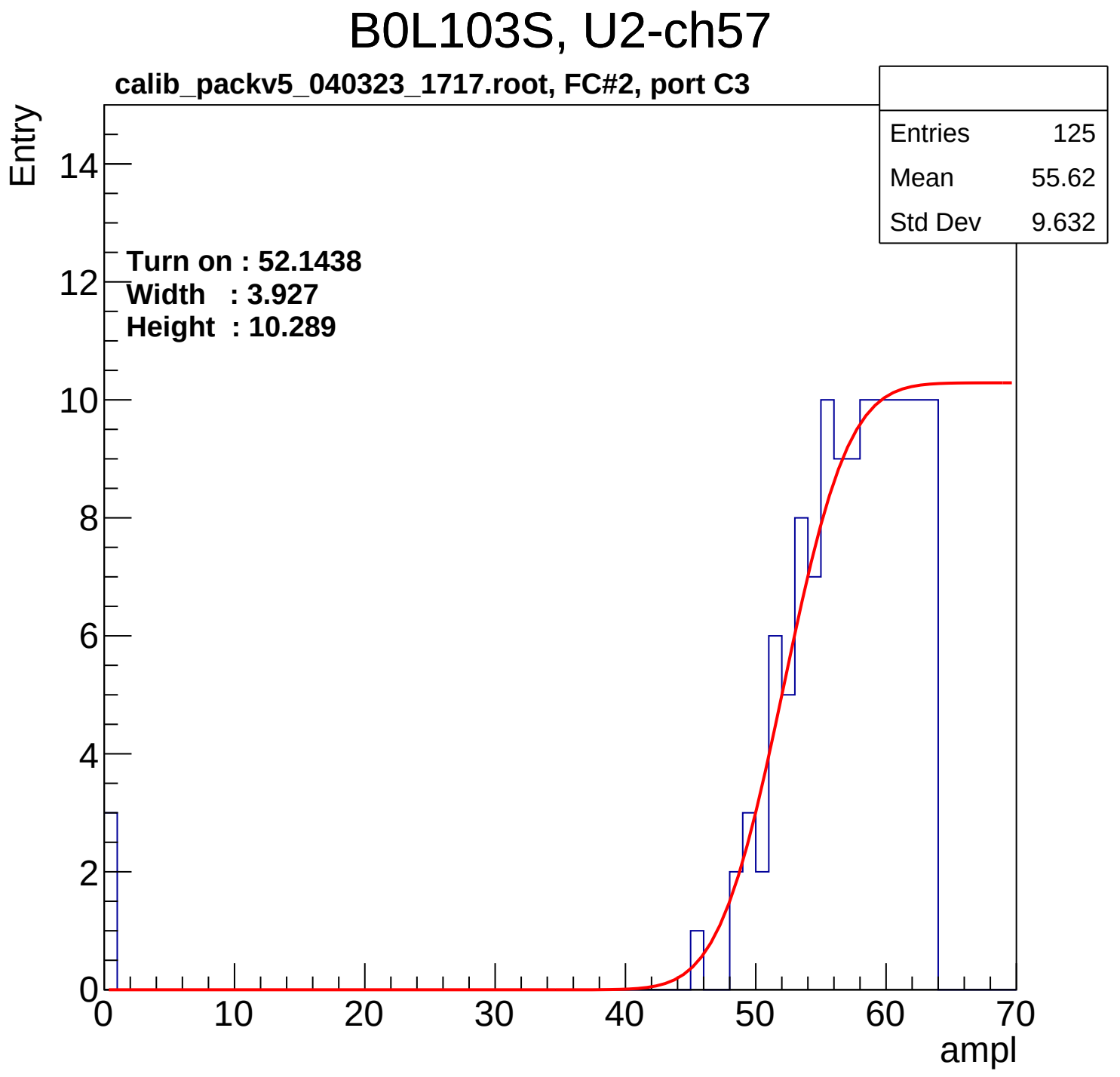
B0L103S, U2-ch57
calib_packv5_040323_1717.root, FC#2, port C3
Entries 125
Mean 55.62
Std Dev 9.632
Turn on : 52.1438
Width : 3.927
Height : 10.289
Entry
ampl
0
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4
6
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12
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20
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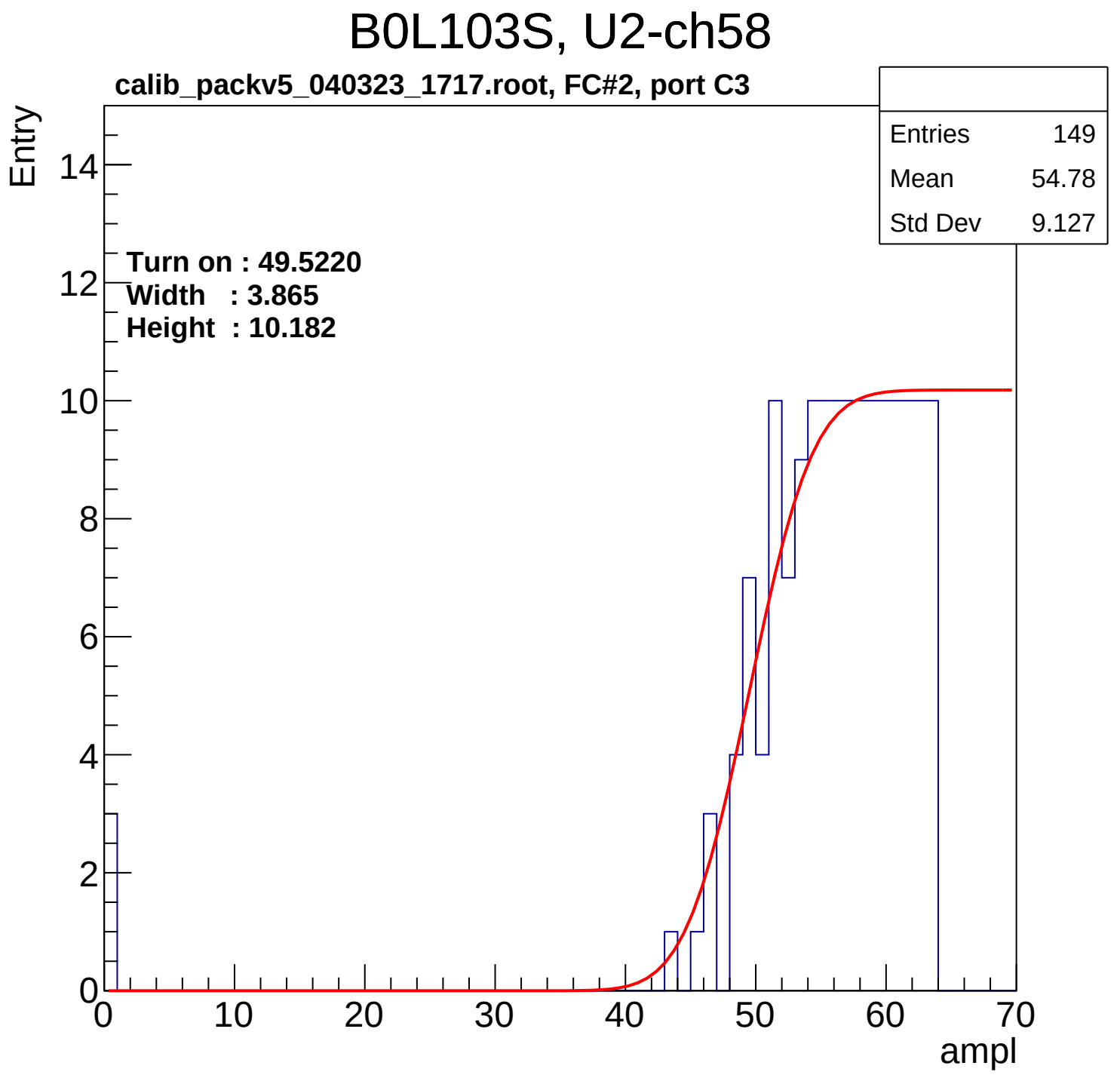
B0L103S, U2-ch58
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 54.78
Std Dev 9.127
Turn on : 49.5220
Width : 3.865
Height : 10.182
Entry
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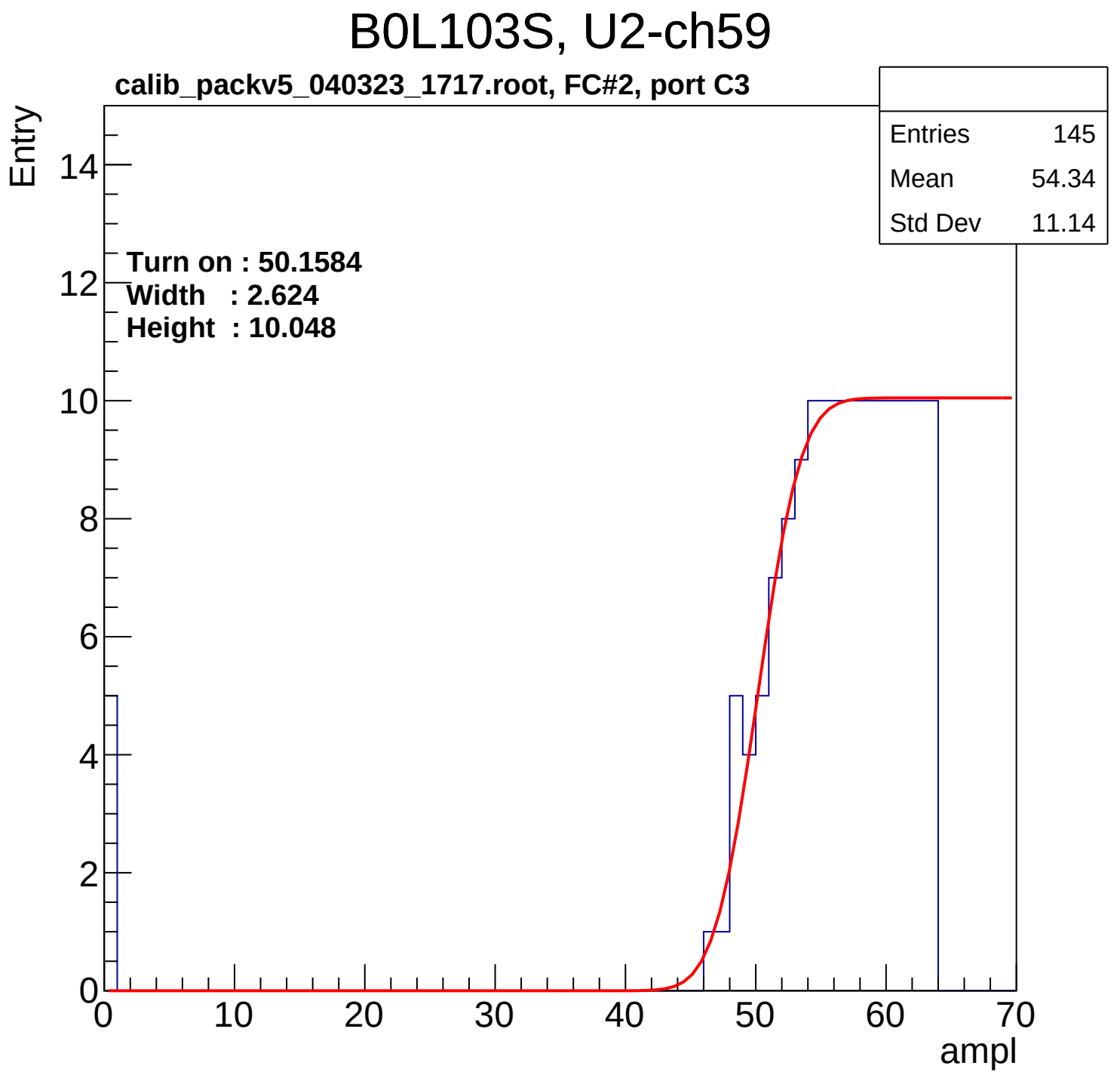
B0L103S, U2-ch59
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 54.34
Std Dev 11.14
Turn on : 50.1584
Width : 2.624
Height : 10.048
Entry
ampl
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2
4
6
8
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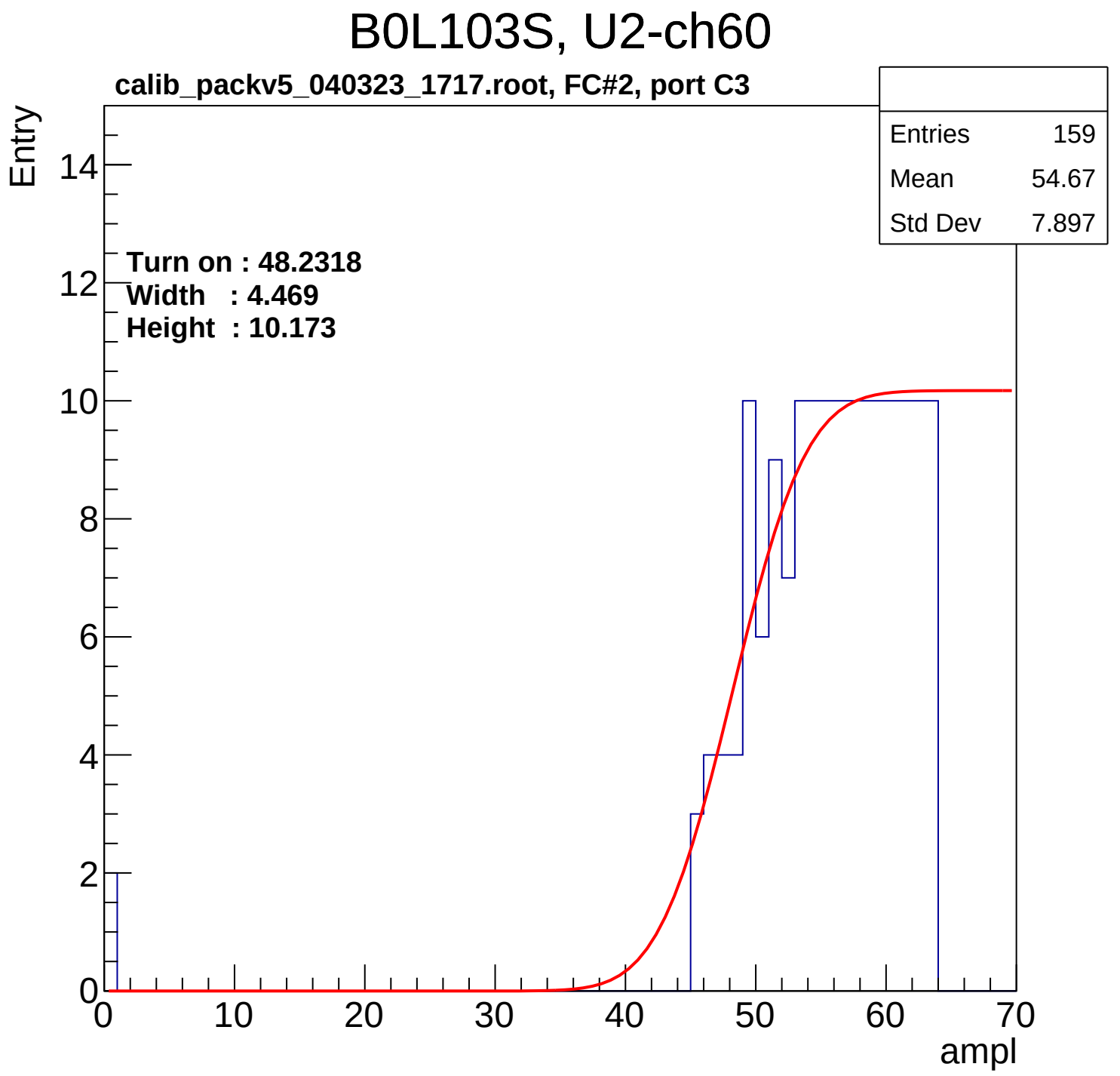
B0L103S, U2-ch60
calib_packv5_040323_1717.root, FC#2, port C3
Entries 159
Mean 54.67
Std Dev 7.897
Turn on : 48.2318
Width : 4.469
Height : 10.173
Entry
ampl
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2
4
6
8
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12
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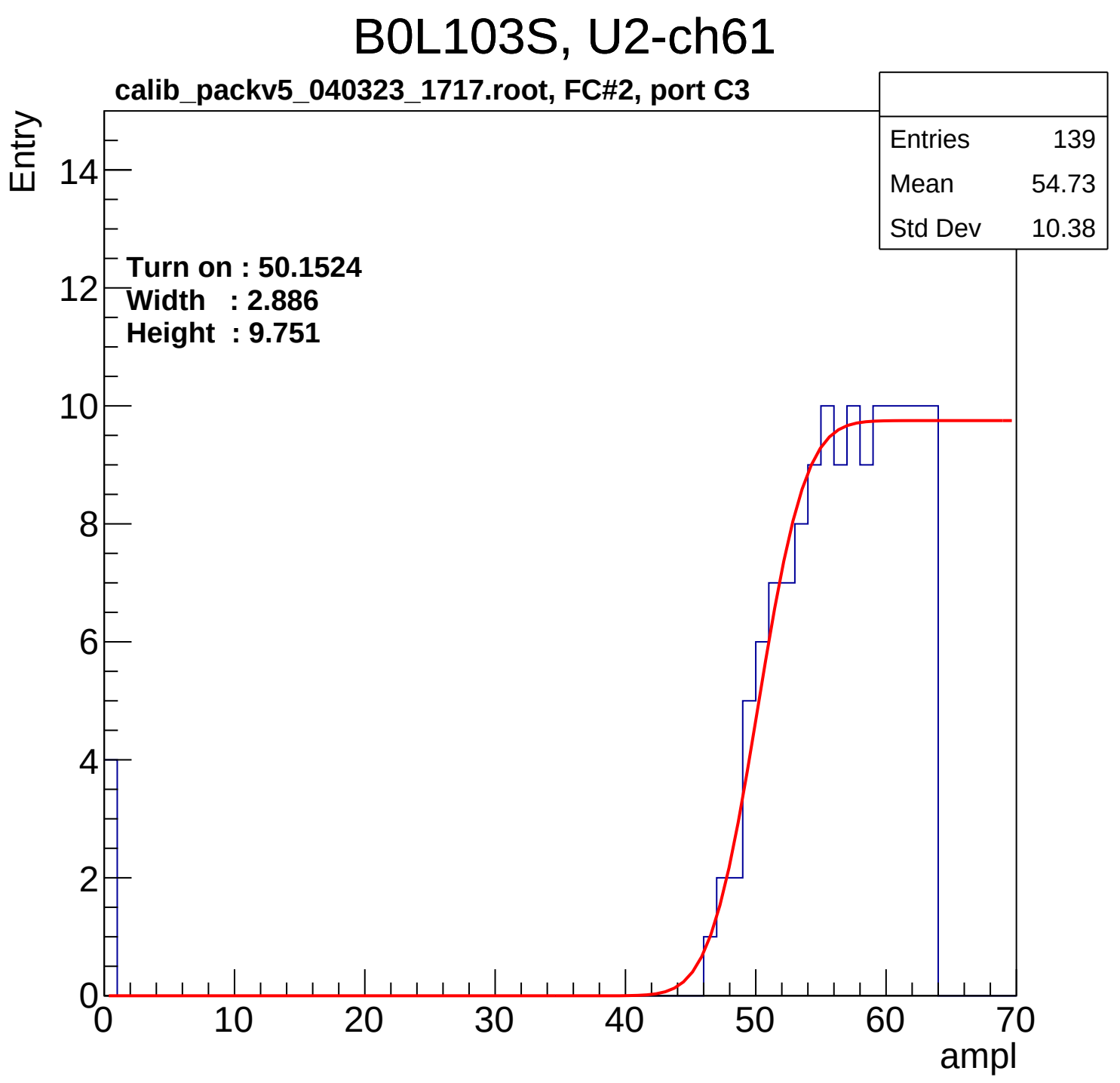
B0L103S, U2-ch61
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 54.73
Std Dev 10.38
Turn on : 50.1524
Width : 2.886
Height : 9.751
Entry
ampl
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2
4
6
8
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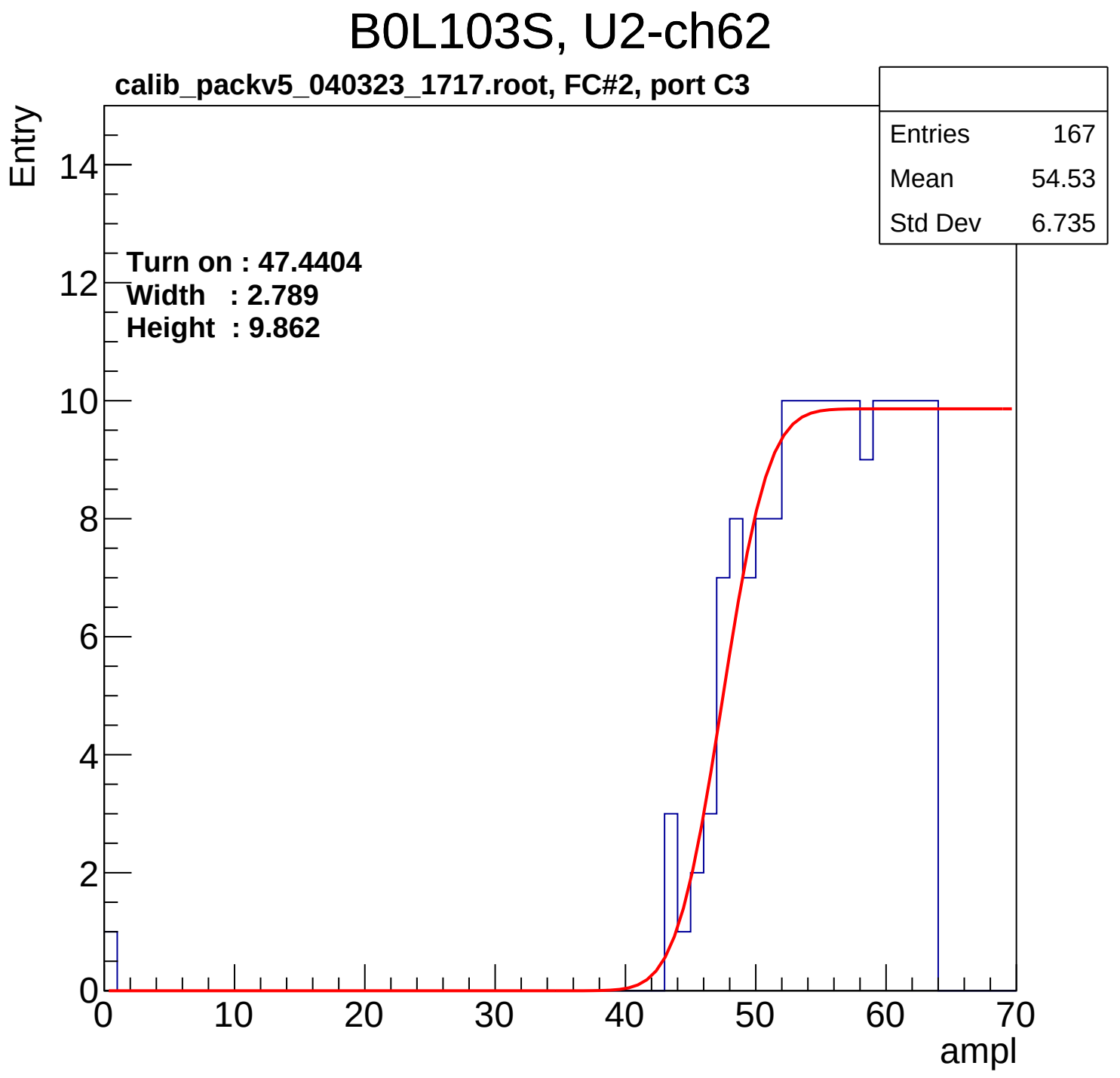
B0L103S, U2-ch62
calib_packv5_040323_1717.root, FC#2, port C3
Entries 167
Mean 54.53
Std Dev 6.735
Turn on : 47.4404
Width : 2.789
Height : 9.862
Entry
ampl
0
2
4
6
8
10
12
14
0
10
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60
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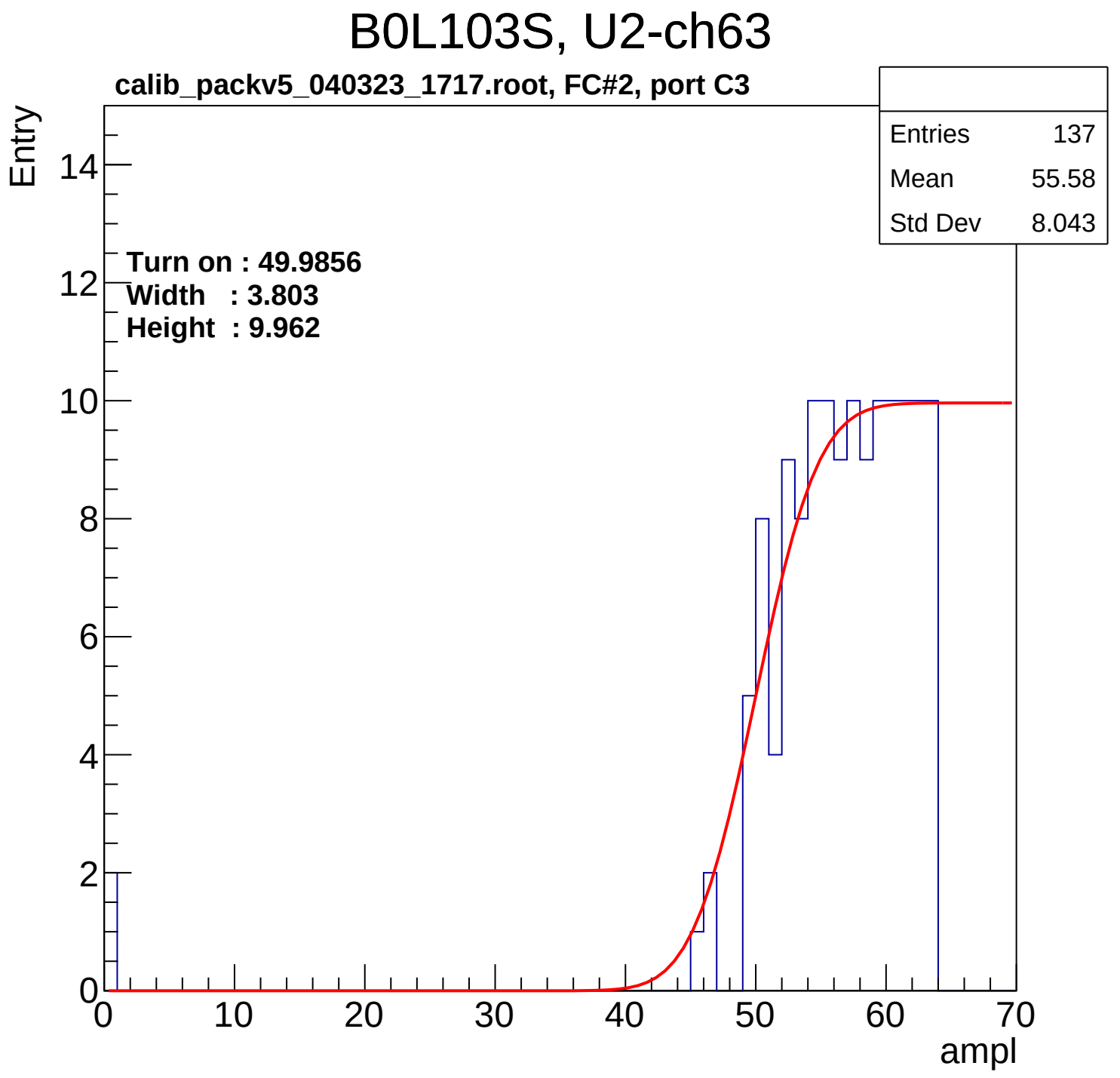
B0L103S, U2-ch63
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 55.58
Std Dev 8.043
Turn on : 49.9856
Width : 3.803
Height : 9.962
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
30
40
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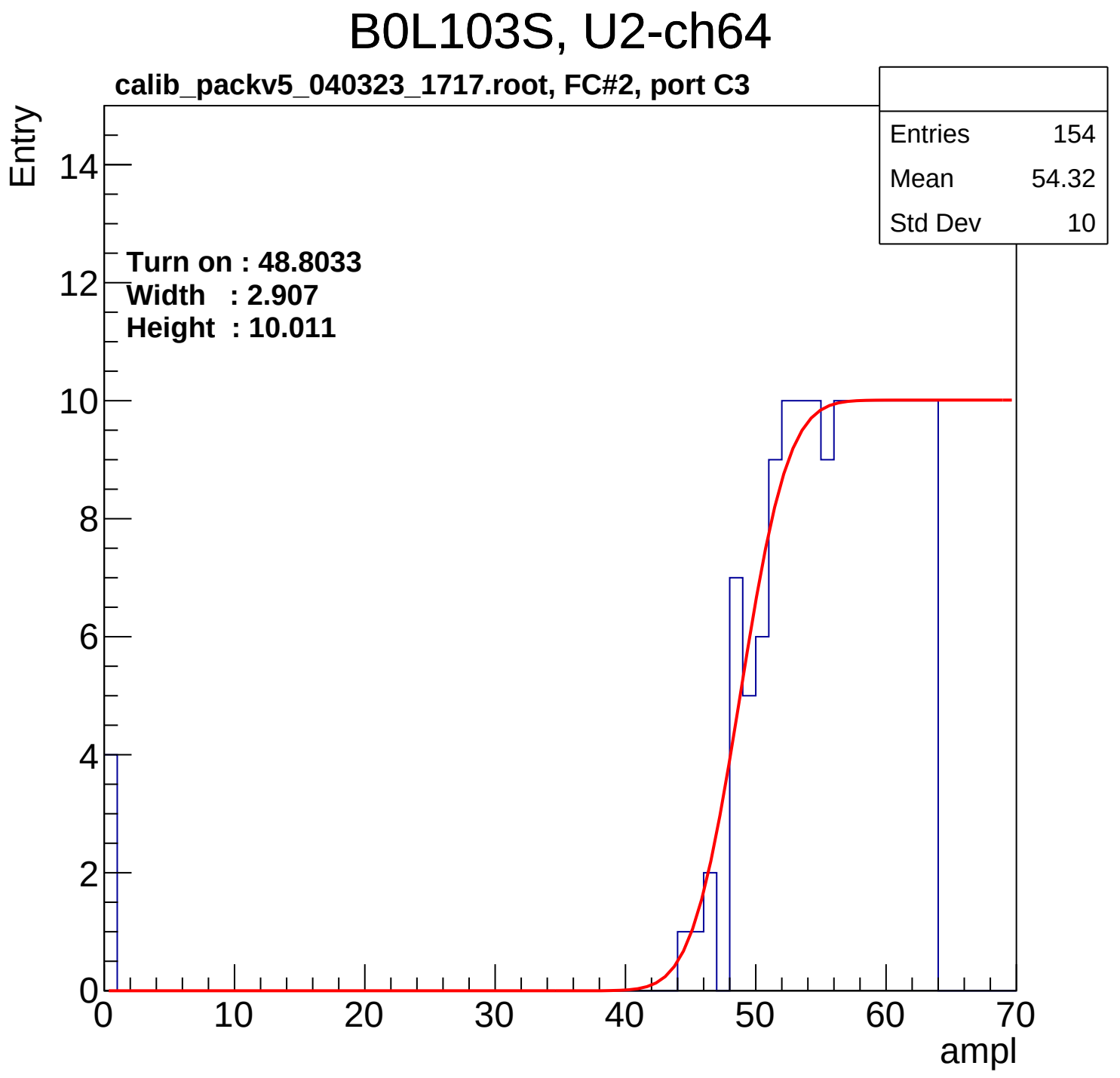
B0L103S, U2-ch64
calib_packv5_040323_1717.root, FC#2, port C3
Entries 154
Mean 54.32
Std Dev 10
Turn on : 48.8033
Width : 2.907
Height : 10.011
Entry
ampl
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2
4
6
8
10
12
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0
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60
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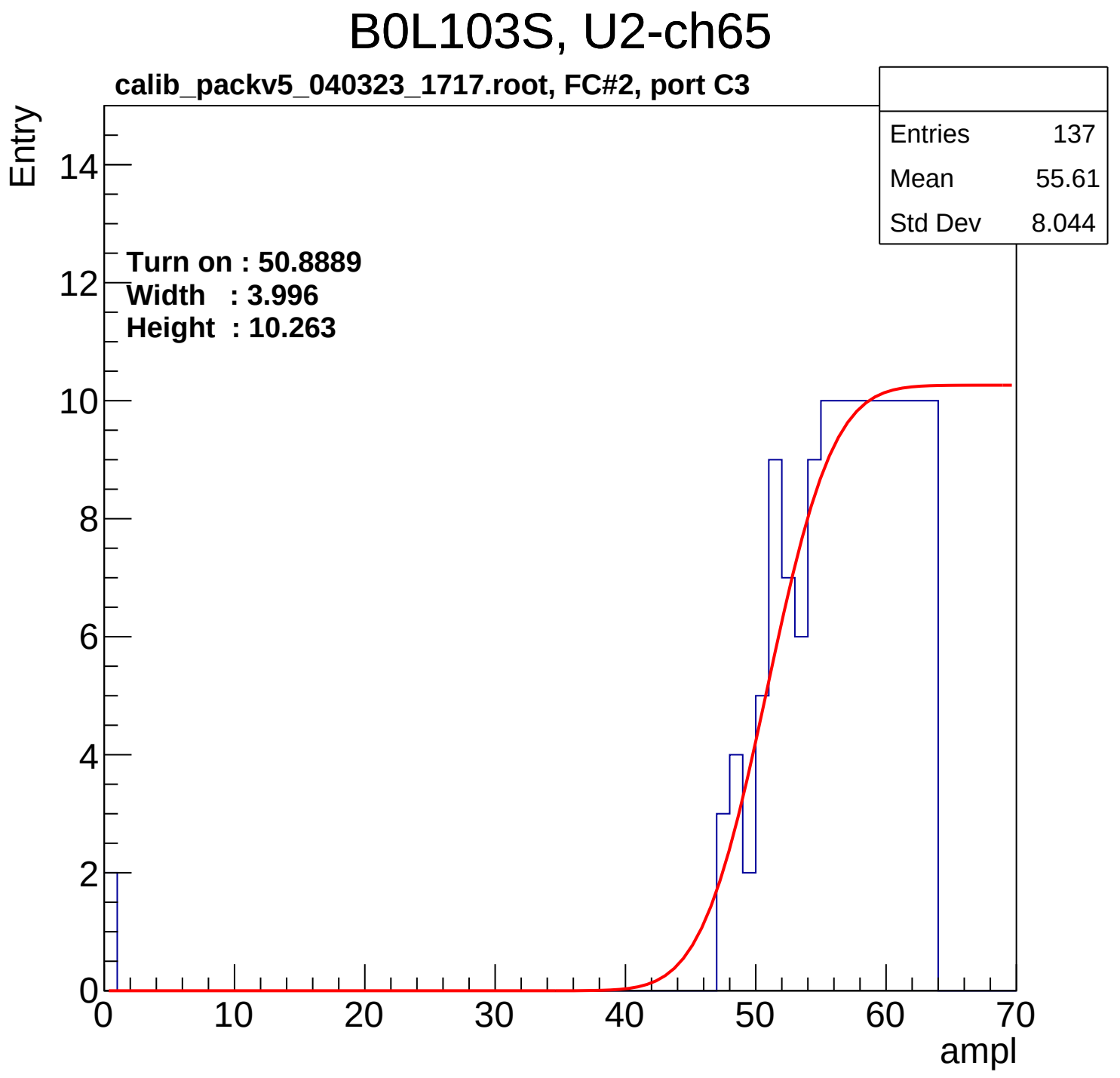
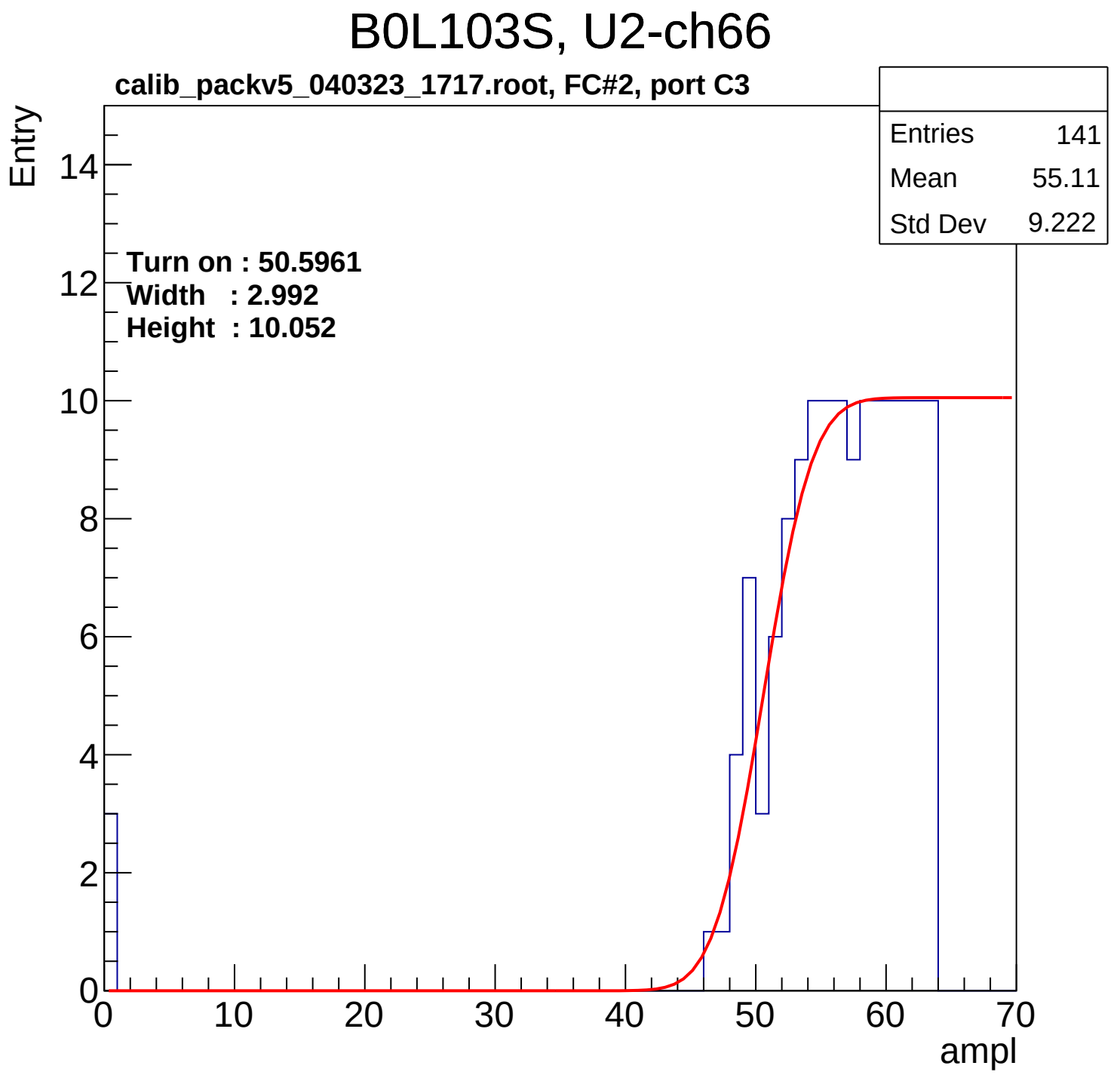

B0L103S, U2-ch65
calib_packv5_040323_1717.root, FC#2, port C3
Entries 137
Mean 55.61
Std Dev 8.044
Turn on : 50.8889
Width : 3.996
Height : 10.263
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U2-ch66
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 55.11
Std Dev 9.222
Turn on : 50.5961
Width : 2.992
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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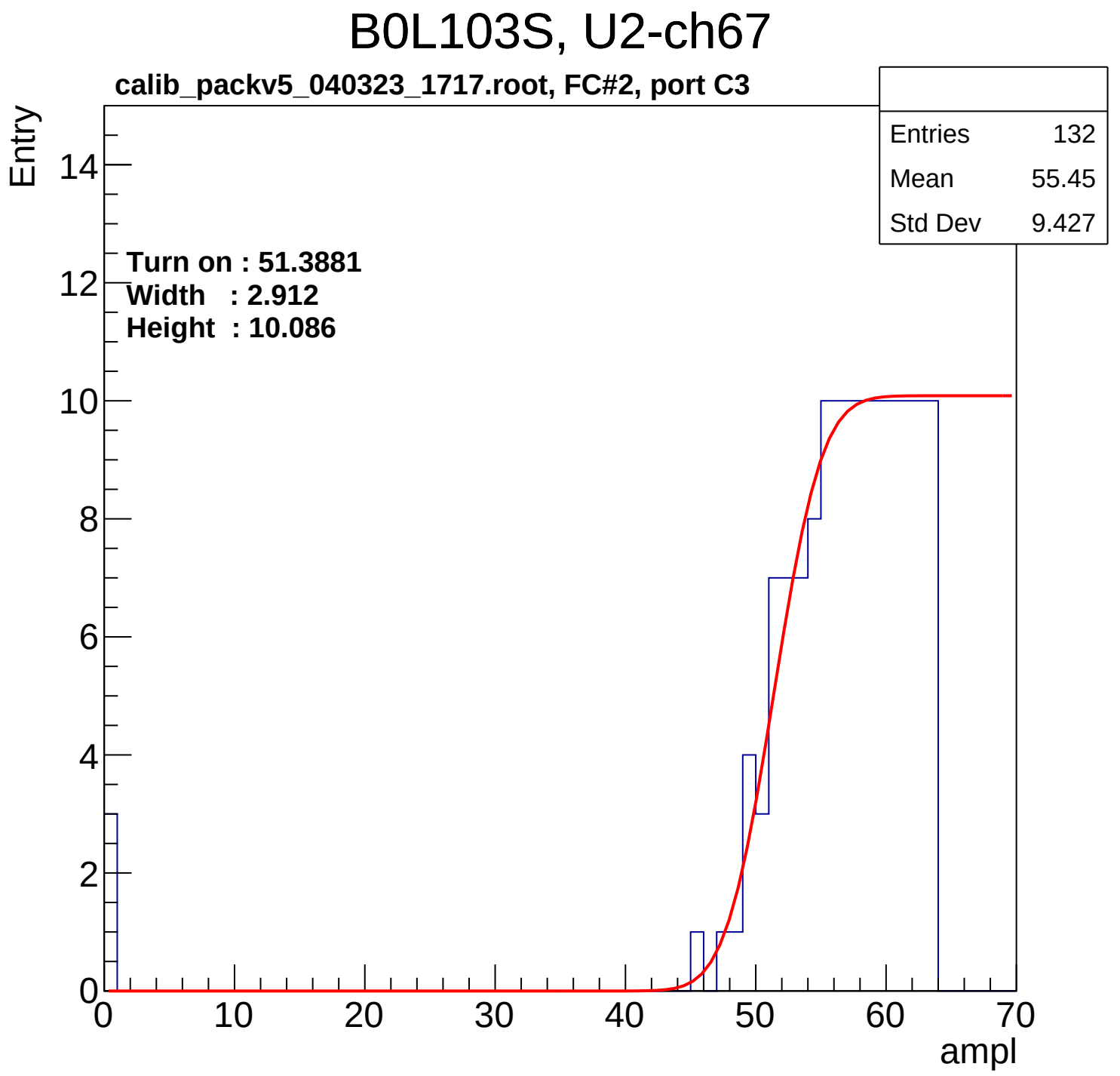
B0L103S, U2-ch67
calib_packv5_040323_1717.root, FC#2, port C3
Entries 132
Mean 55.45
Std Dev 9.427
Turn on : 51.3881
Width : 2.912
Height : 10.086
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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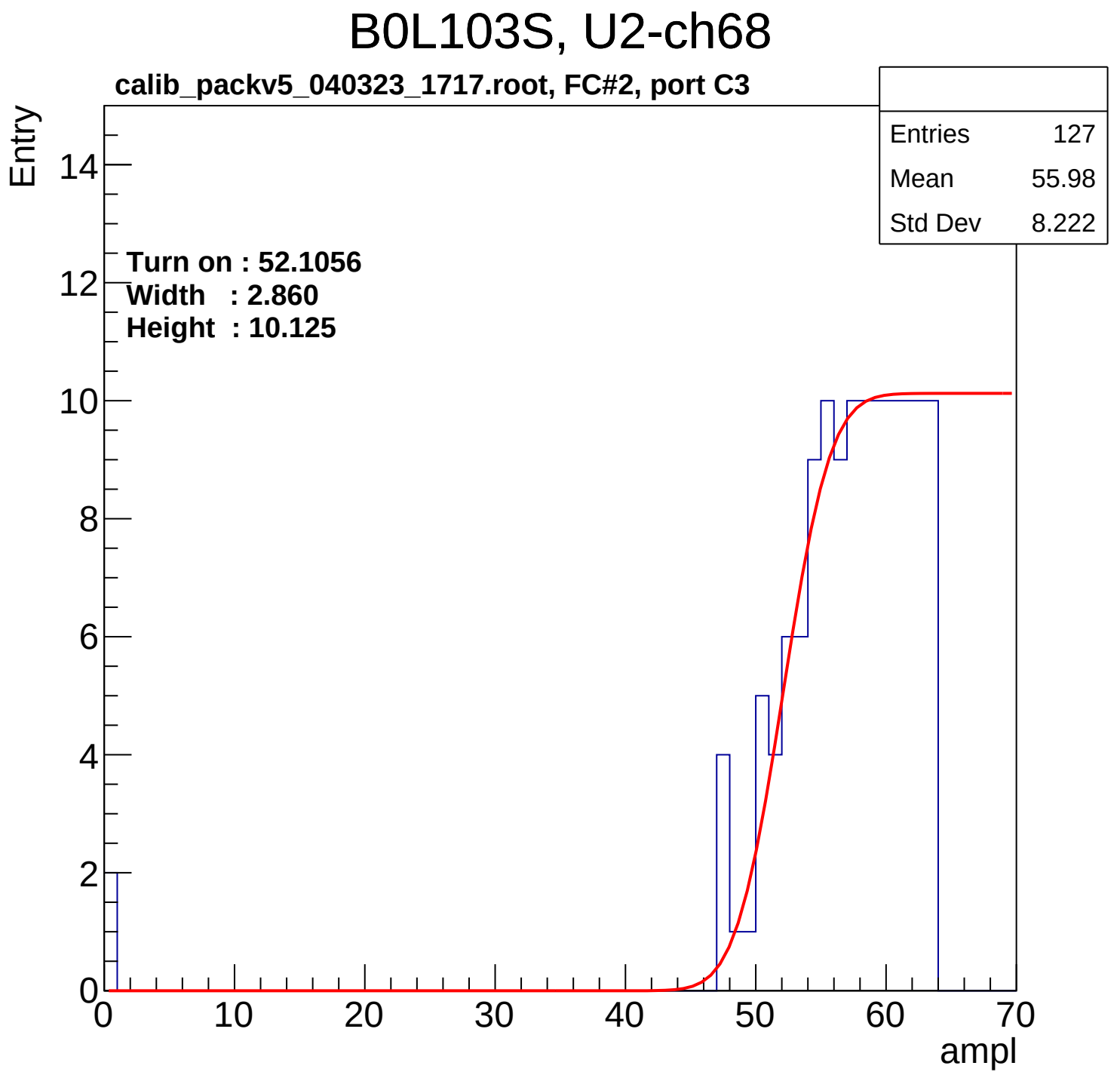
B0L103S, U2-ch68
calib_packv5_040323_1717.root, FC#2, port C3
Entries 127
Mean 55.98
Std Dev 8.222
Turn on : 52.1056
Width : 2.860
Height : 10.125
Entry
ampl
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2
4
6
8
10
12
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0
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20
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60
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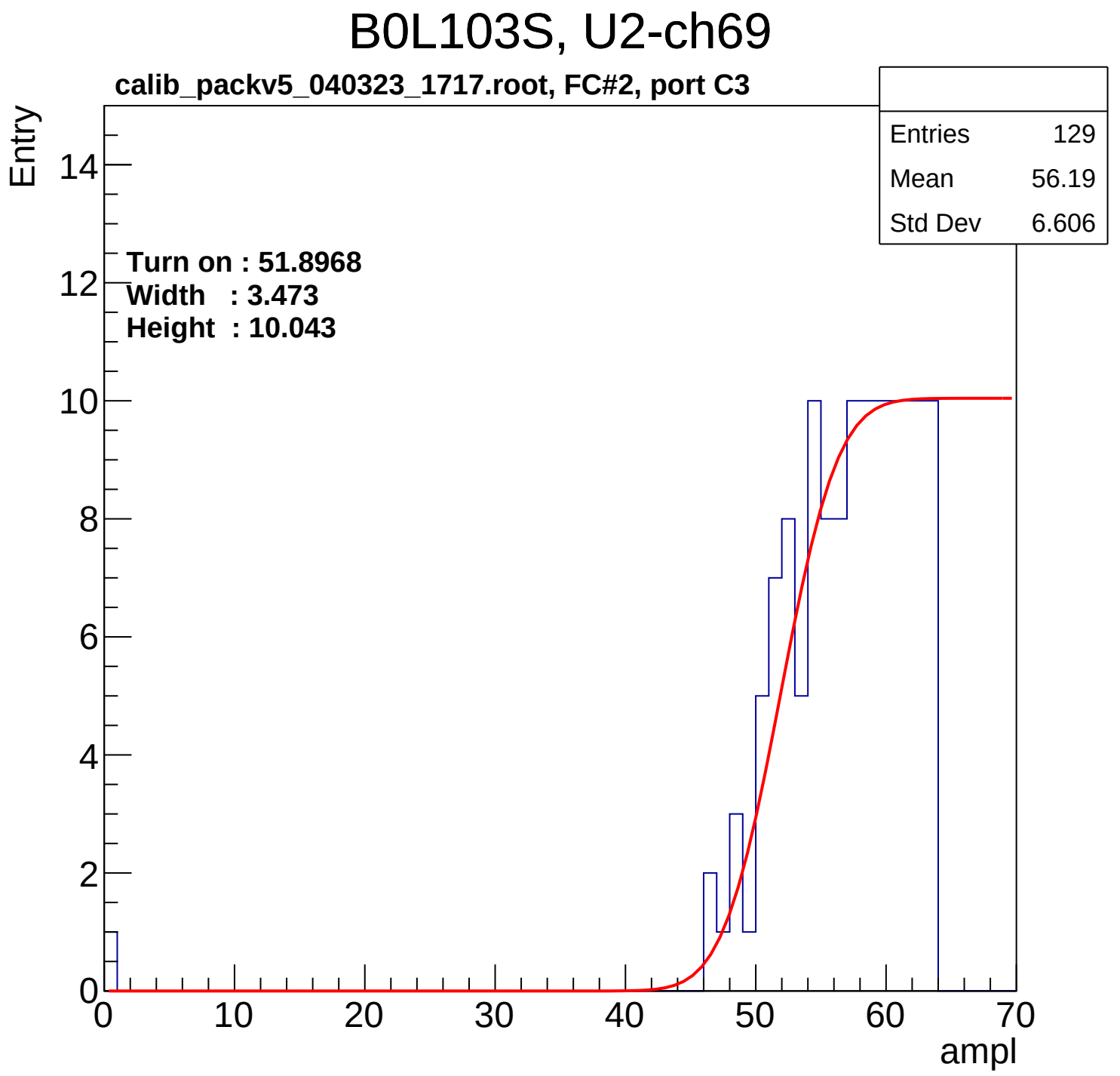
B0L103S, U2-ch69
calib_packv5_040323_1717.root, FC#2, port C3
Entries 129
Mean 56.19
Std Dev 6.606
Turn on : 51.8968
Width : 3.473
Height : 10.043
Entry
ampl
0
2
4
6
8
10
12
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0
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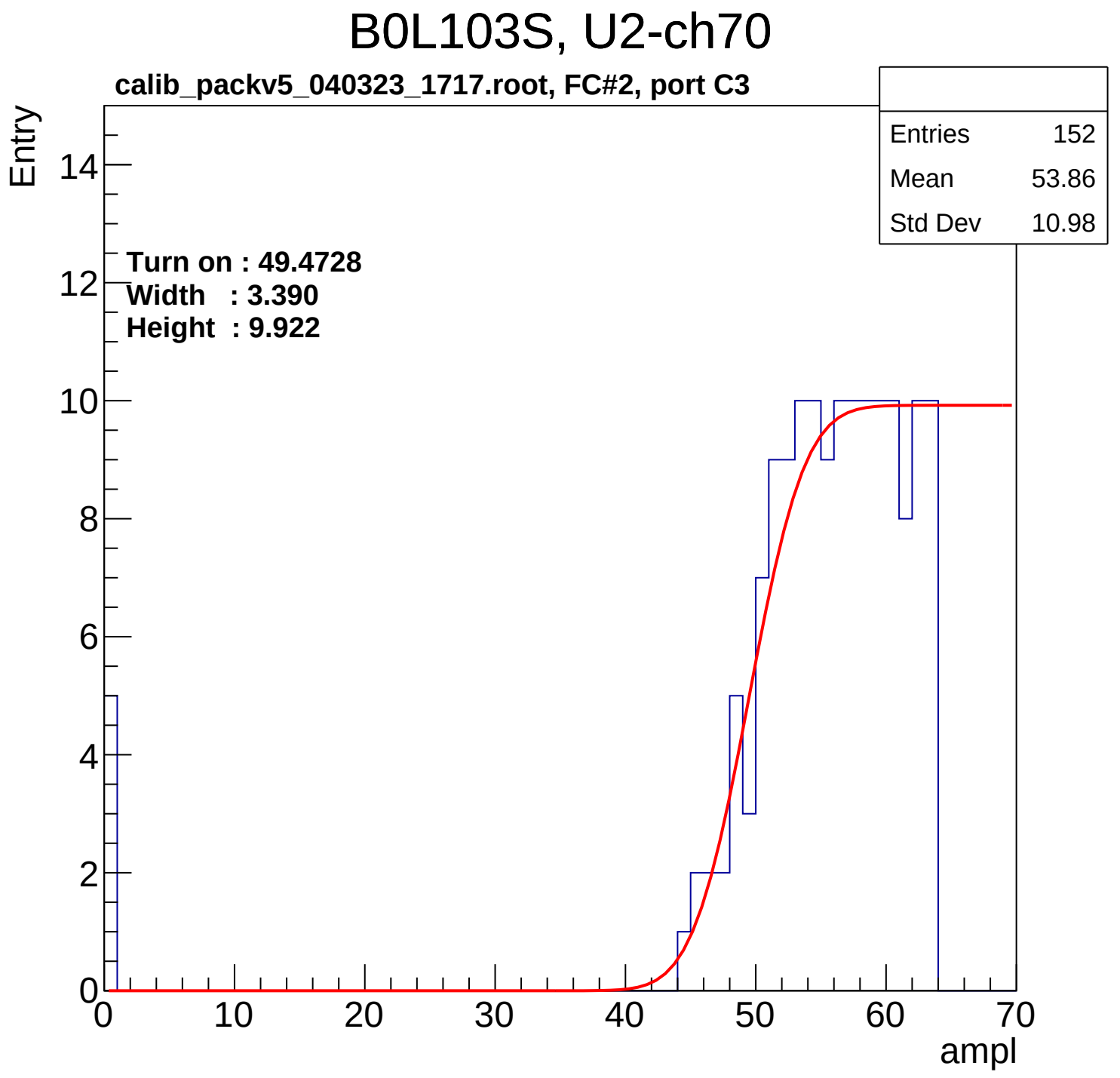
B0L103S, U2-ch70
calib_packv5_040323_1717.root, FC#2, port C3
Entries 152
Mean 53.86
Std Dev 10.98
Turn on : 49.4728
Width : 3.390
Height : 9.922
Entry
ampl
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4
6
8
10
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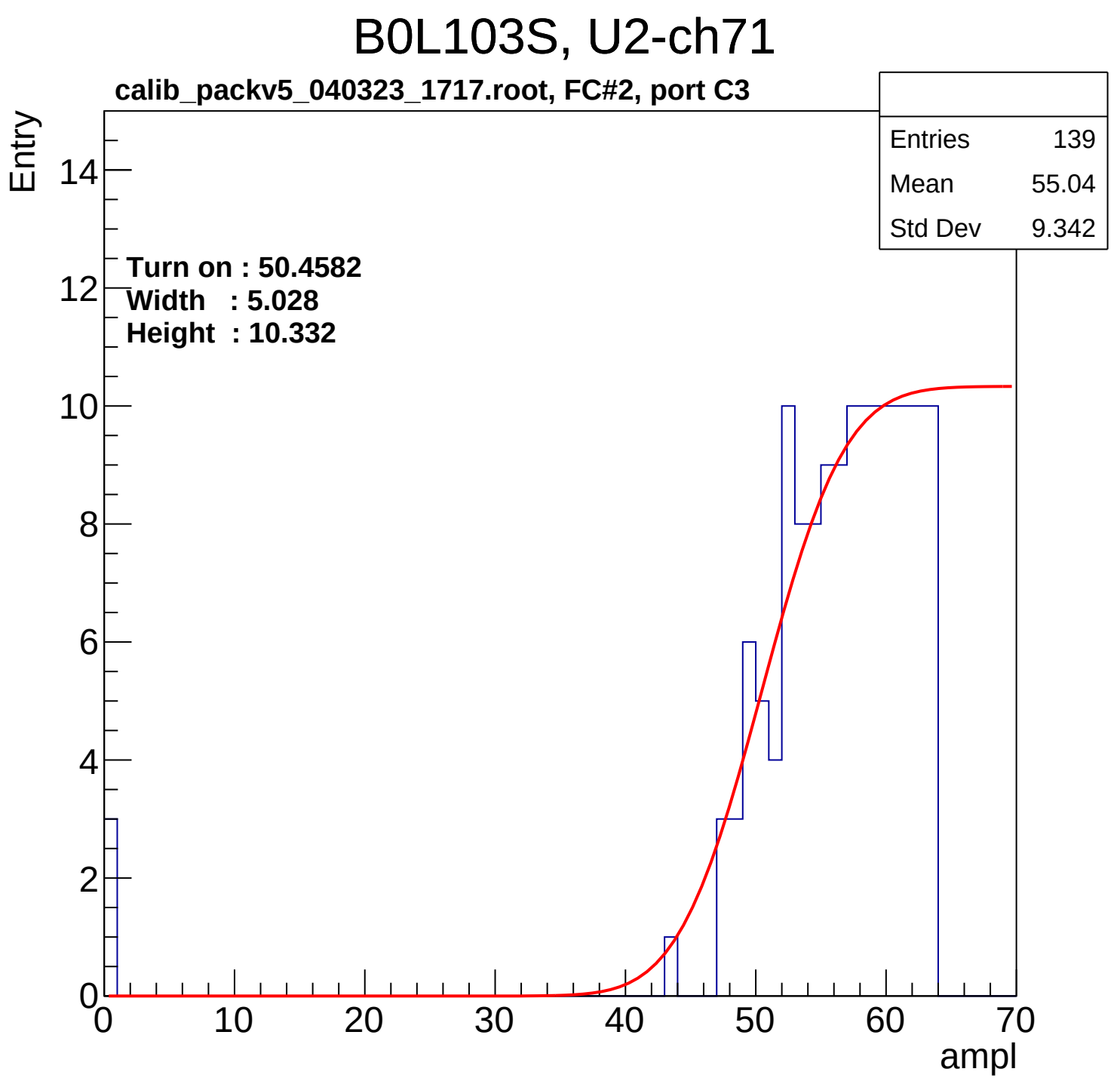
B0L103S, U2-ch71
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 55.04
Std Dev 9.342
Turn on : 50.4582
Width : 5.028
Height : 10.332
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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60
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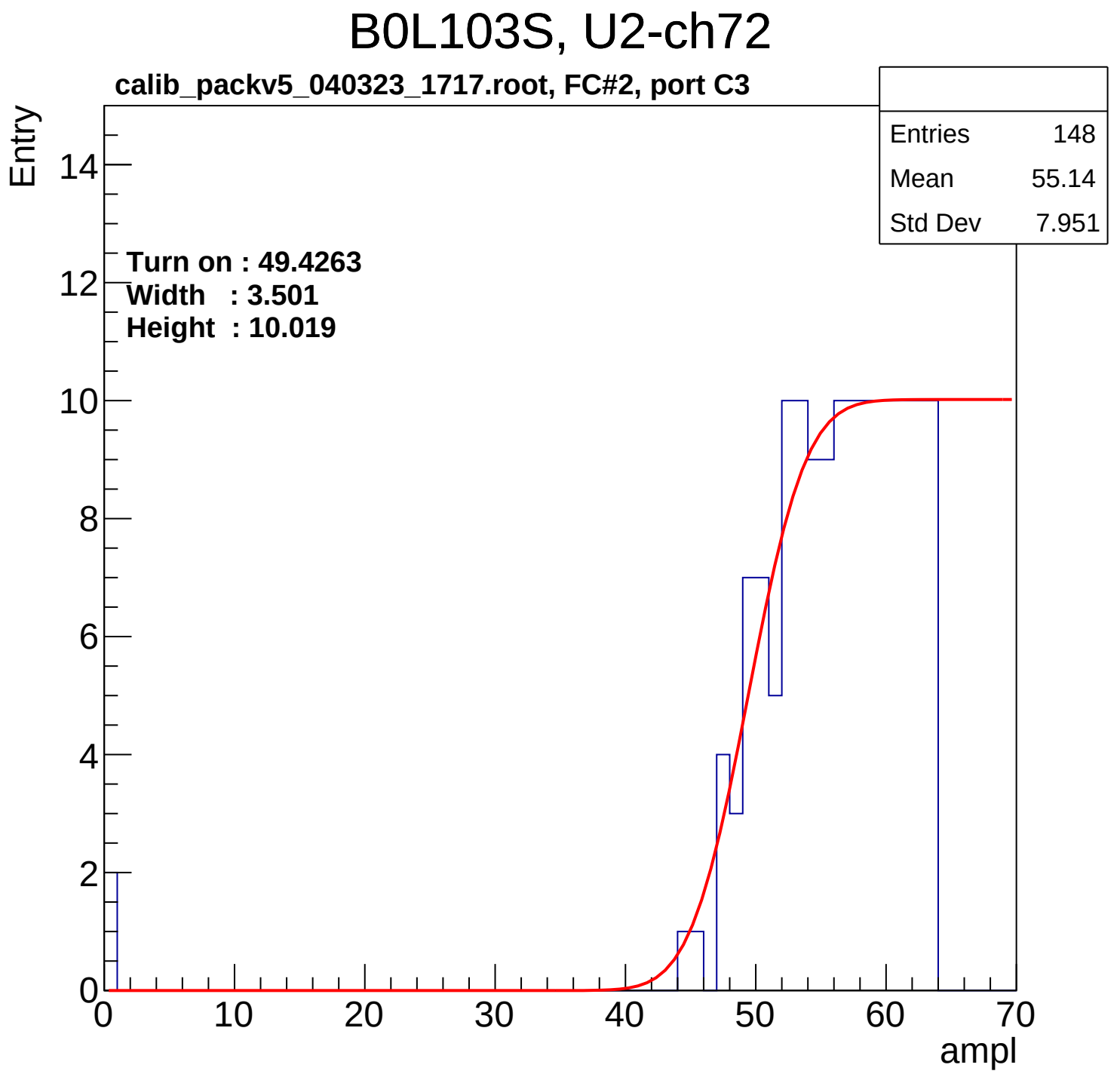
B0L103S, U2-ch72
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 55.14
Std Dev 7.951
Turn on : 49.4263
Width : 3.501
Height : 10.019
Entry
ampl
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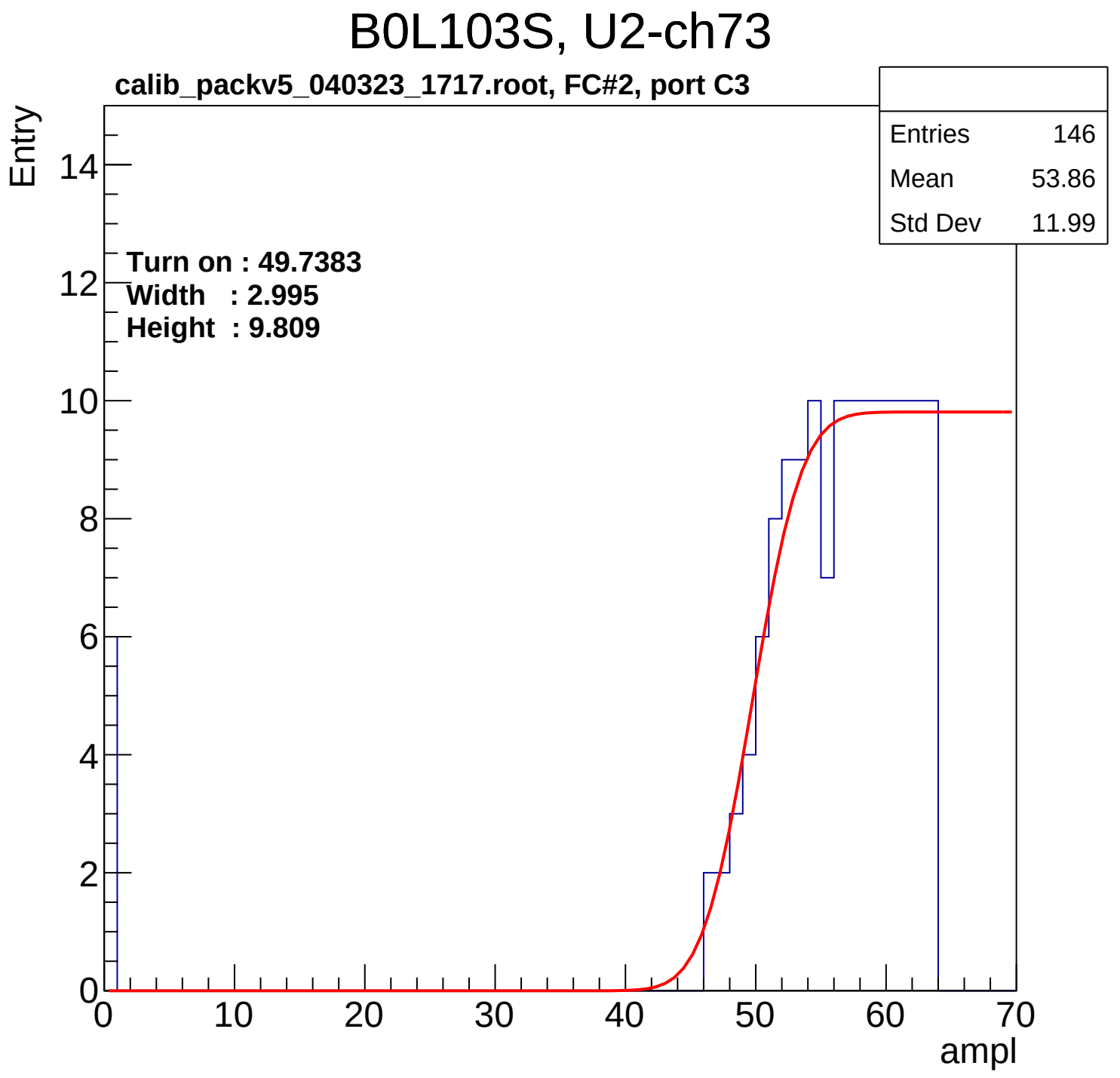
B0L103S, U2-ch73
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 53.86
Std Dev 11.99
Turn on : 49.7383
Width : 2.995
Height : 9.809
Entry
ampl
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4
6
8
10
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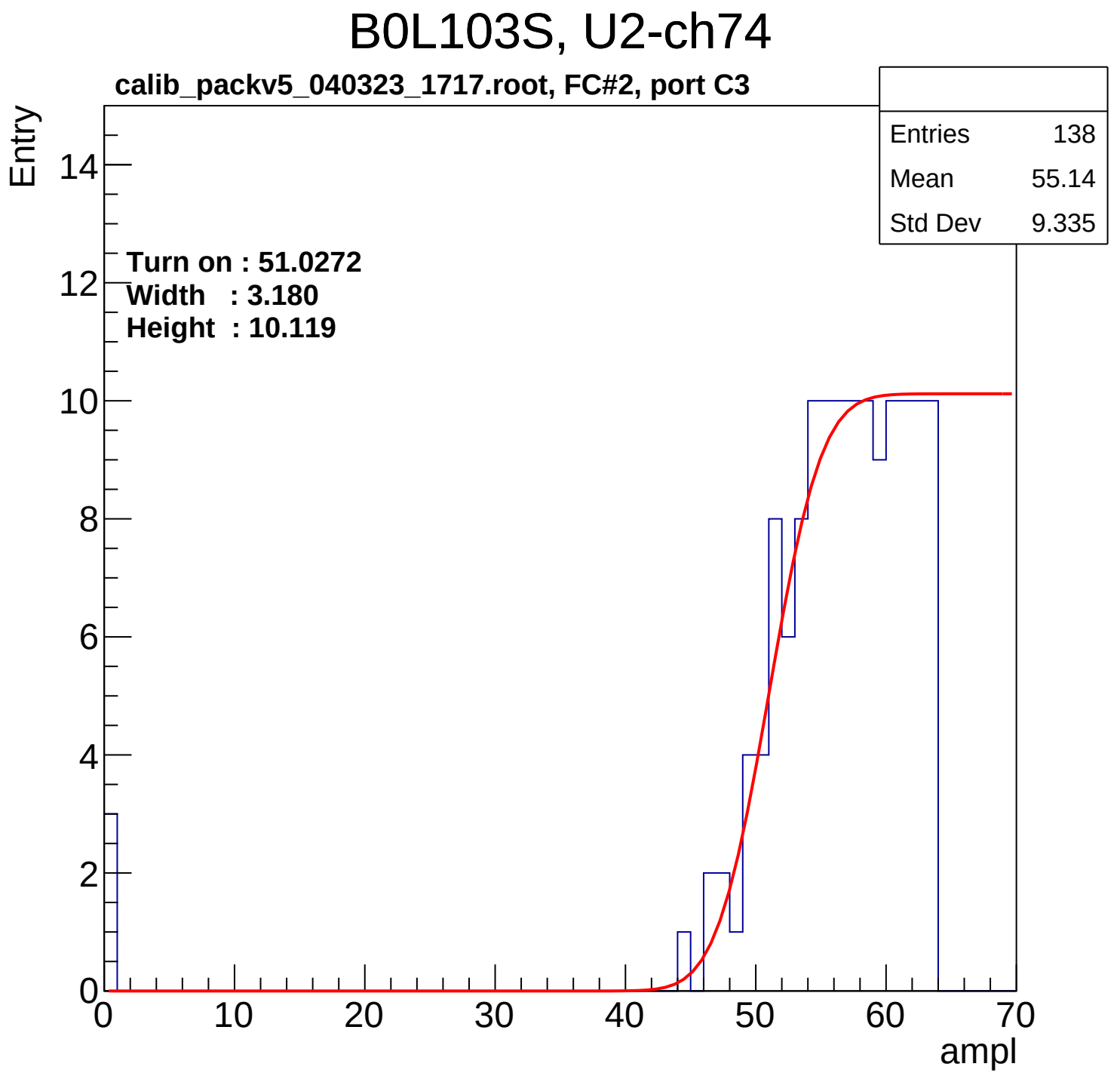
B0L103S, U2-ch74
calib_packv5_040323_1717.root, FC#2, port C3
Entries 138
Mean 55.14
Std Dev 9.335
Turn on : 51.0272
Width : 3.180
Height : 10.119
Entry
ampl
0
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6
8
10
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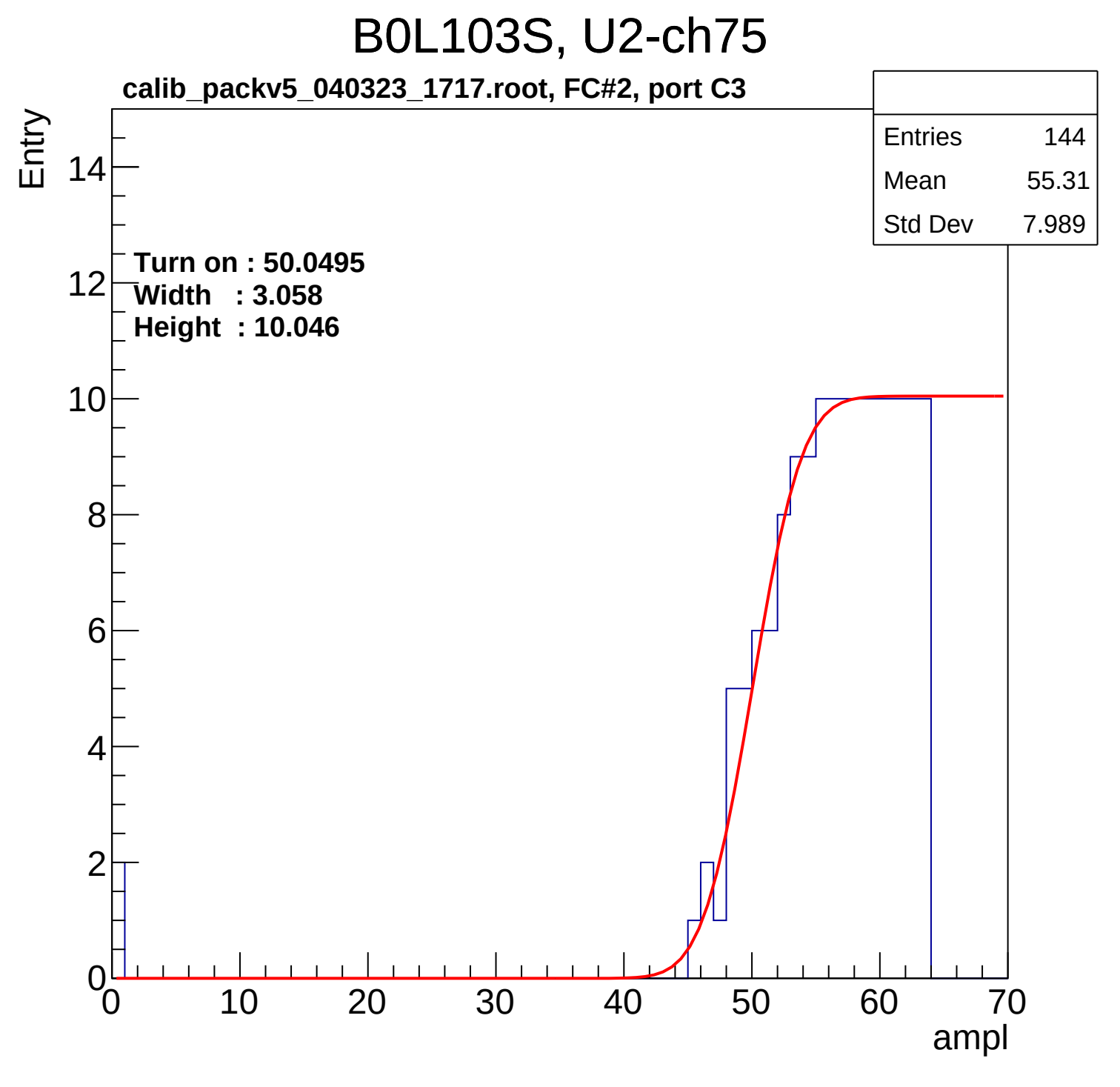
B0L103S, U2-ch75
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 55.31
Std Dev 7.989
Turn on : 50.0495
Width : 3.058
Height : 10.046
Entry
ampl
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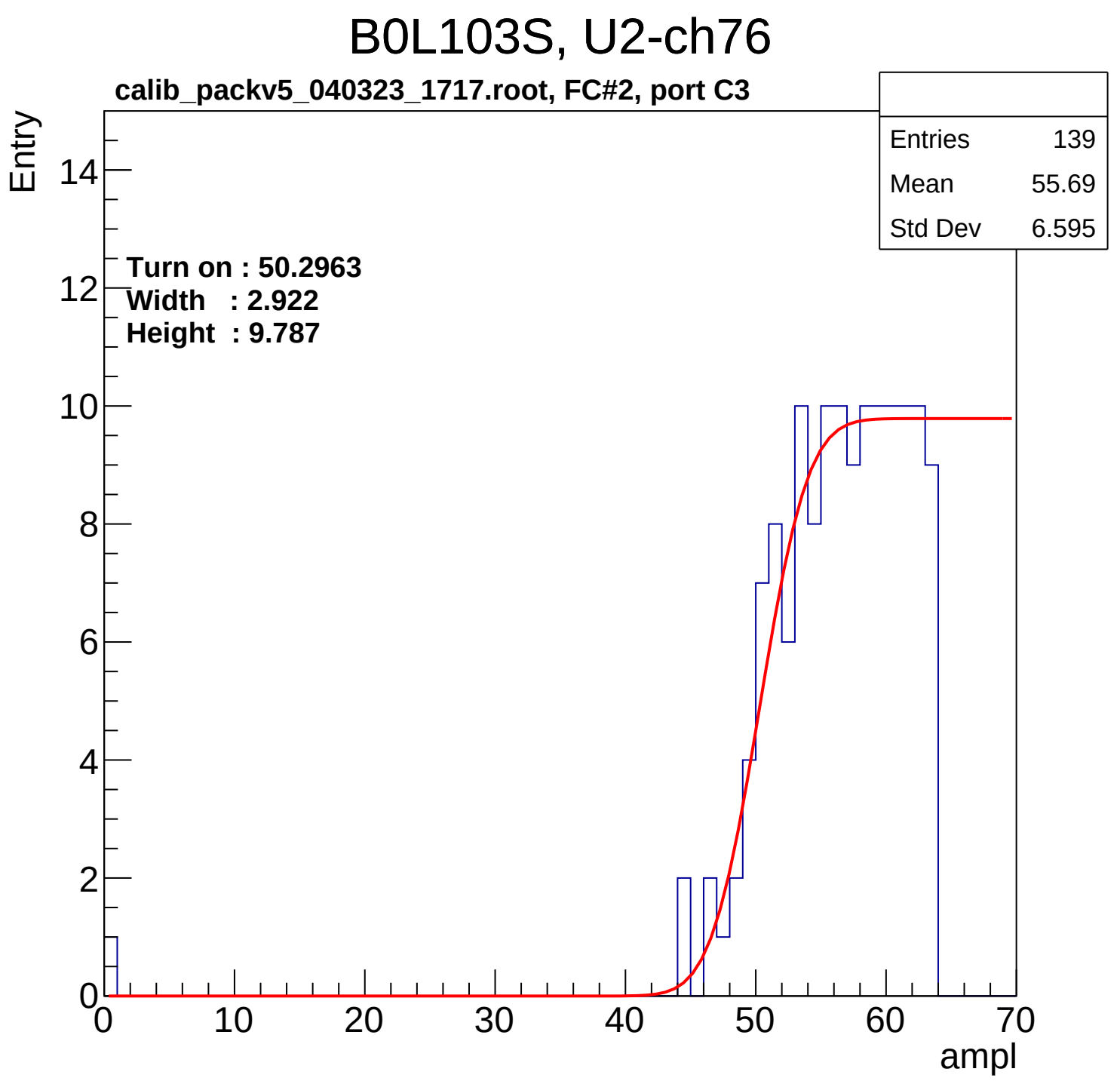
B0L103S, U2-ch76
calib_packv5_040323_1717.root, FC#2, port C3
Entries 139
Mean 55.69
Std Dev 6.595
Turn on : 50.2963
Width : 2.922
Height : 9.787
Entry
ampl
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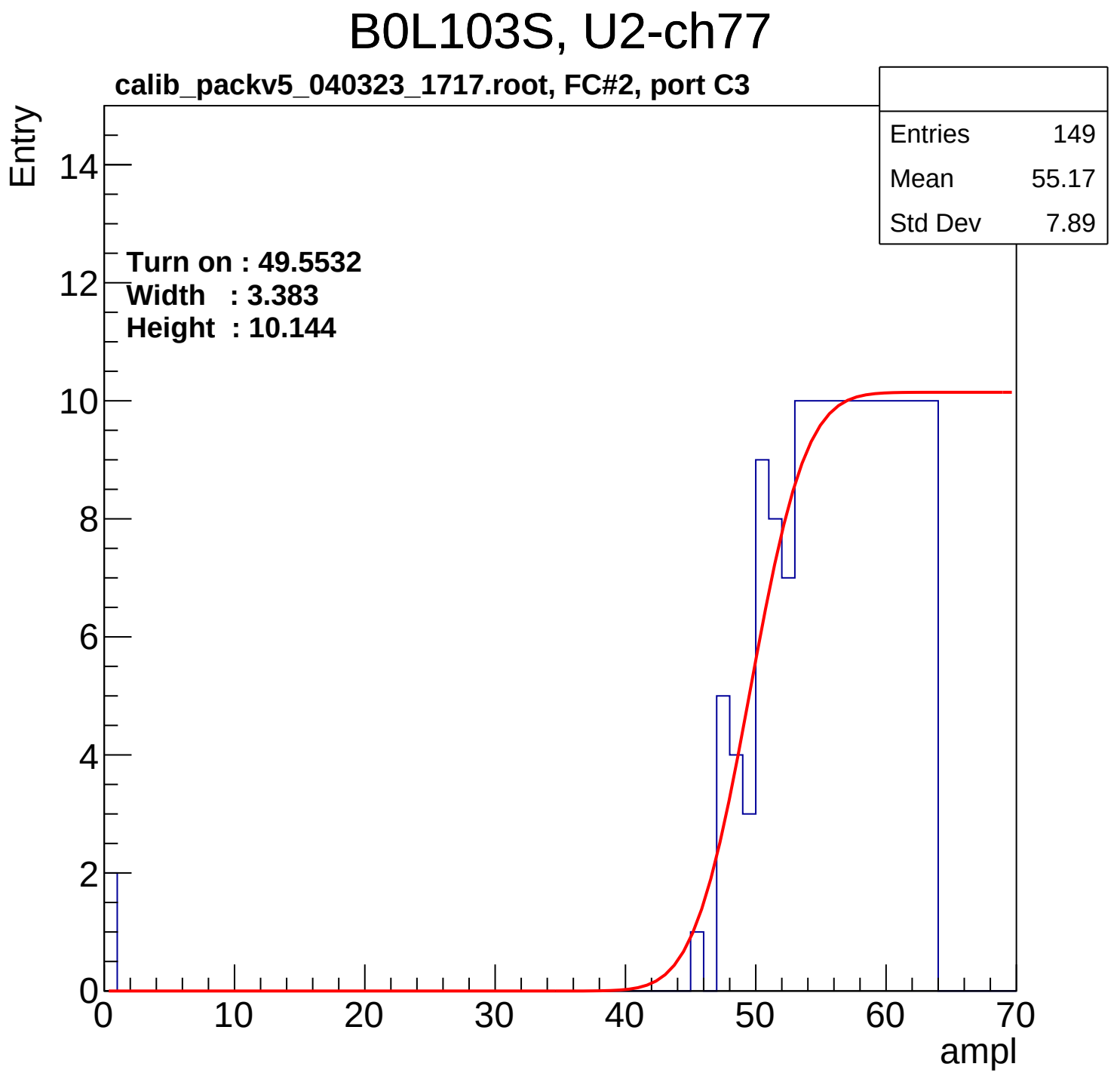
B0L103S, U2-ch77
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 55.17
Std Dev 7.89
Turn on : 49.5532
Width : 3.383
Height : 10.144
Entry
ampl
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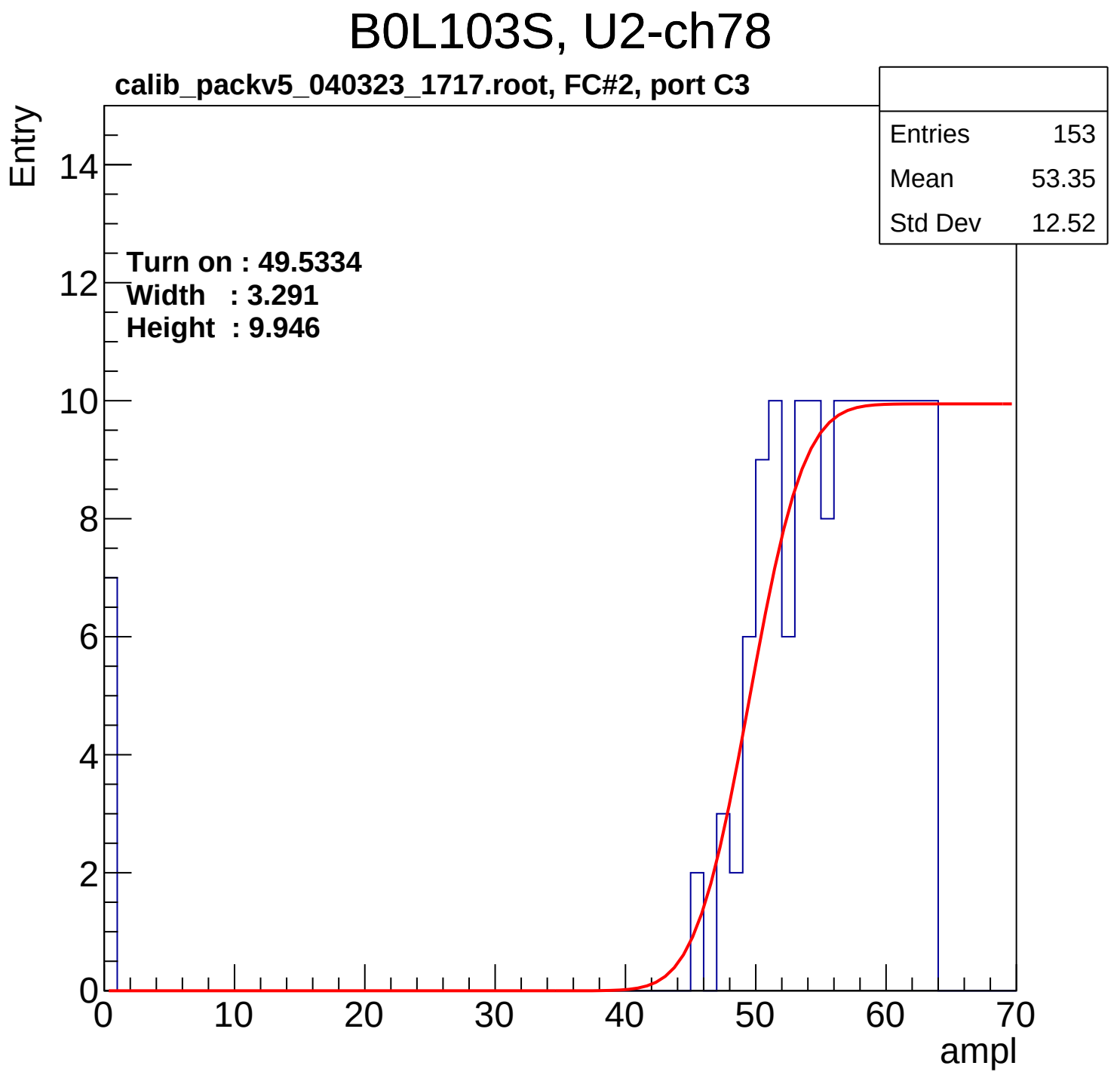
B0L103S, U2-ch78
calib_packv5_040323_1717.root, FC#2, port C3
Entries 153
Mean 53.35
Std Dev 12.52
Turn on : 49.5334
Width : 3.291
Height : 9.946
Entry
ampl
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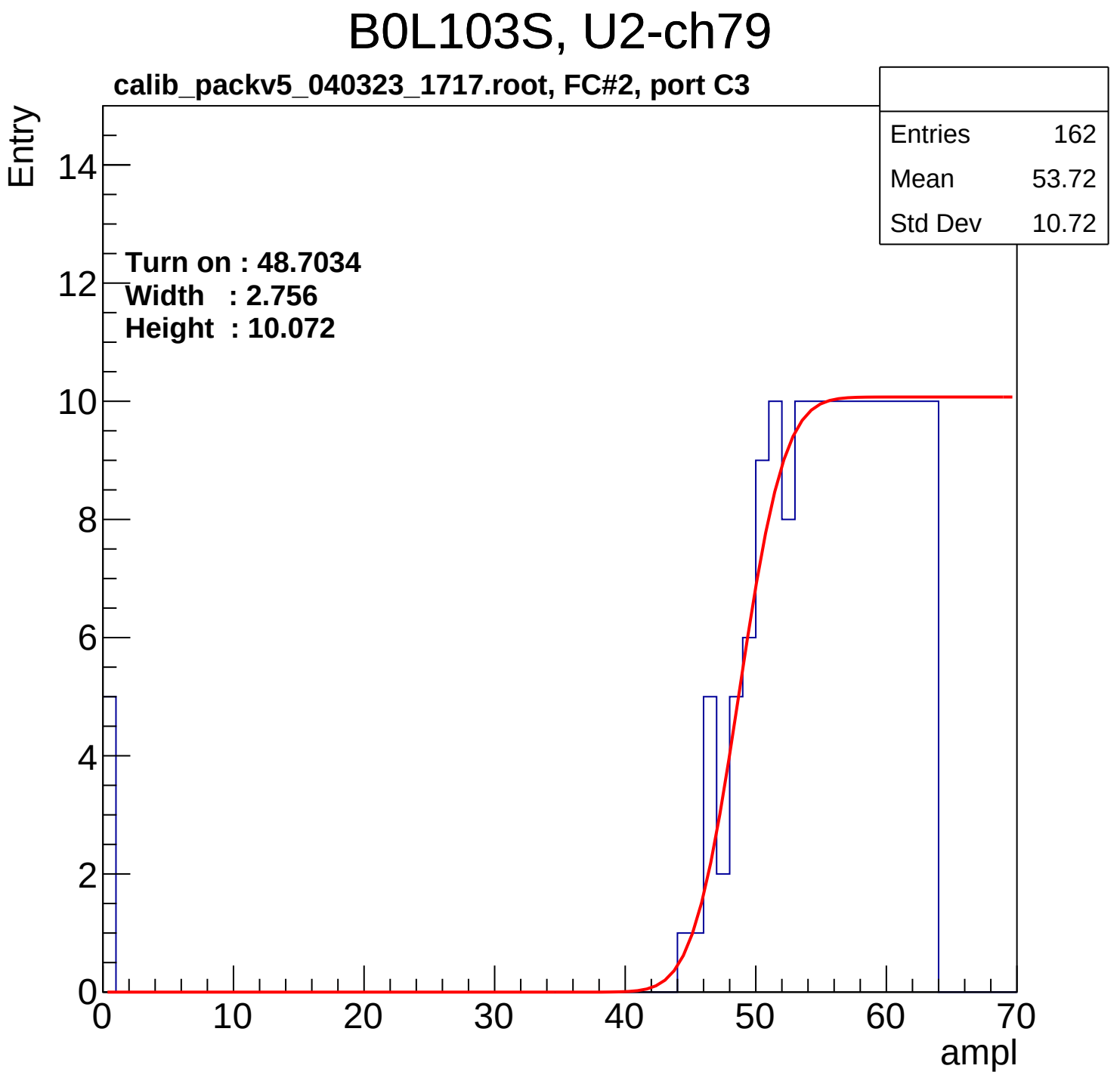
B0L103S, U2-ch79
calib_packv5_040323_1717.root, FC#2, port C3
Entries 162
Mean 53.72
Std Dev 10.72
Turn on : 48.7034
Width : 2.756
Height : 10.072
Entry
ampl
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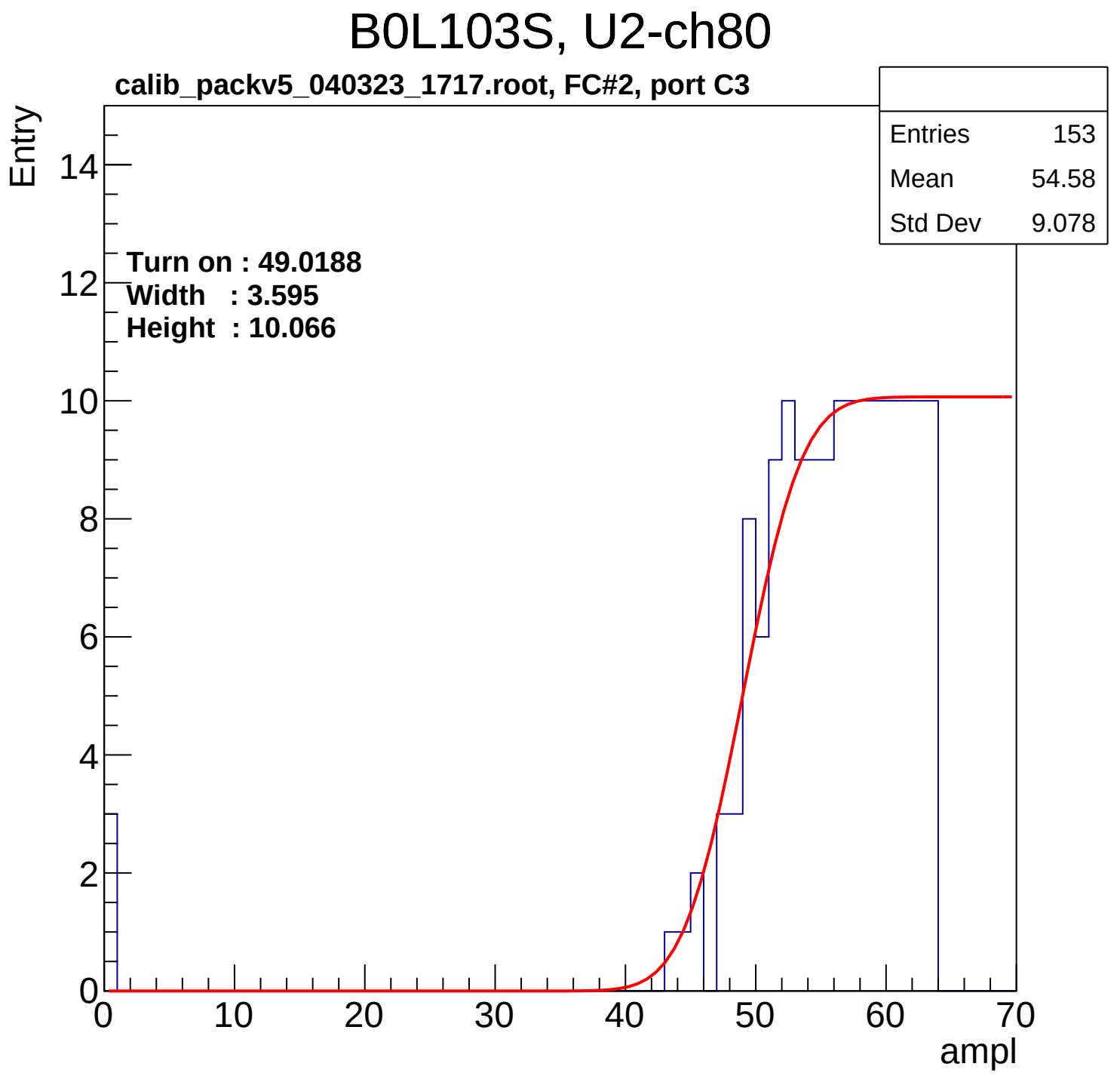
B0L103S, U2-ch80
calib_packv5_040323_1717.root, FC#2, port C3
Entries 153
Mean 54.58
Std Dev 9.078
Turn on : 49.0188
Width : 3.595
Height : 10.066
Entry
ampl
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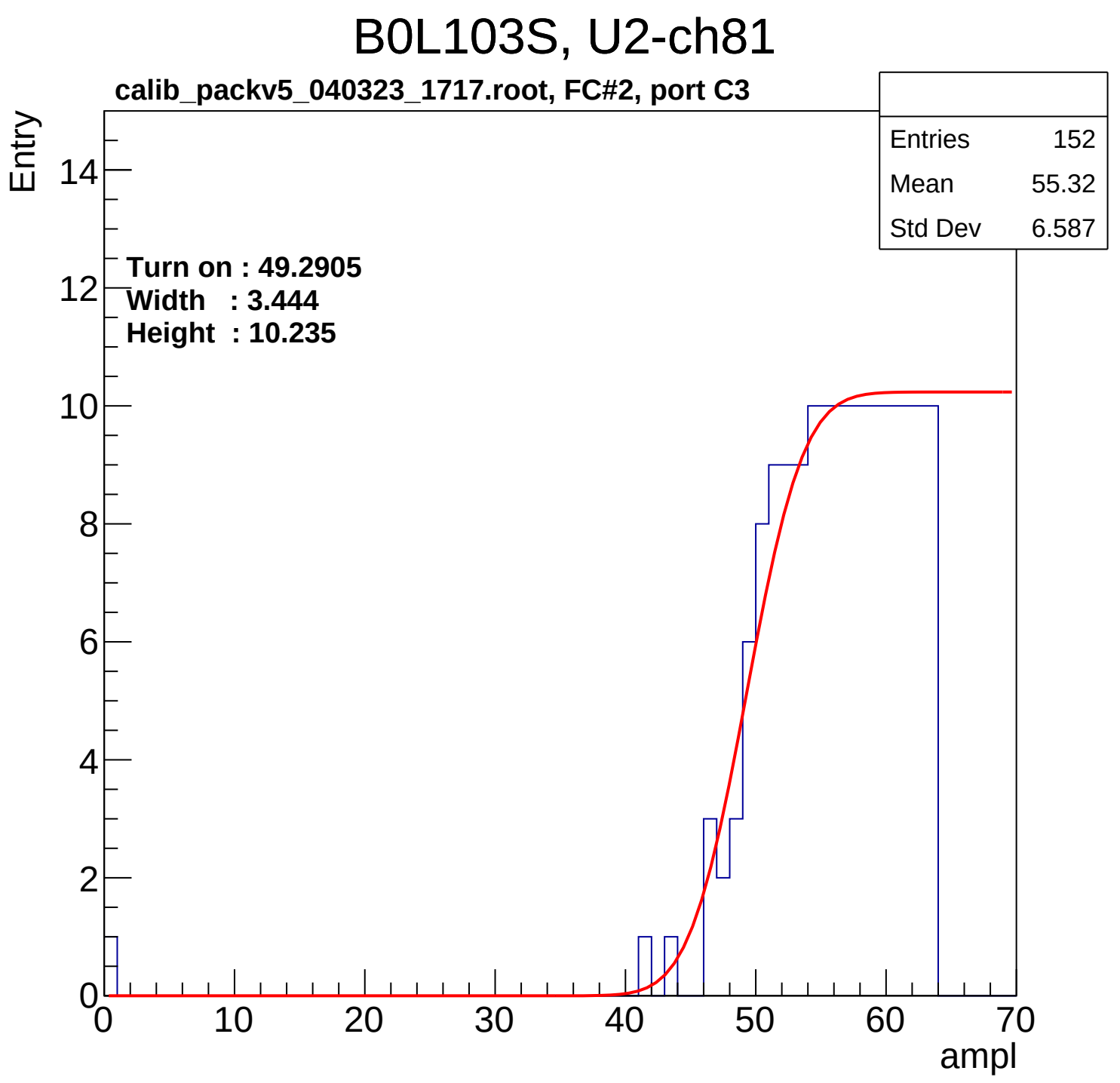
B0L103S, U2-ch81
calib_packv5_040323_1717.root, FC#2, port C3
Entries 152
Mean 55.32
Std Dev 6.587
Turn on : 49.2905
Width : 3.444
Height : 10.235
Entry
ampl
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4
6
8
10
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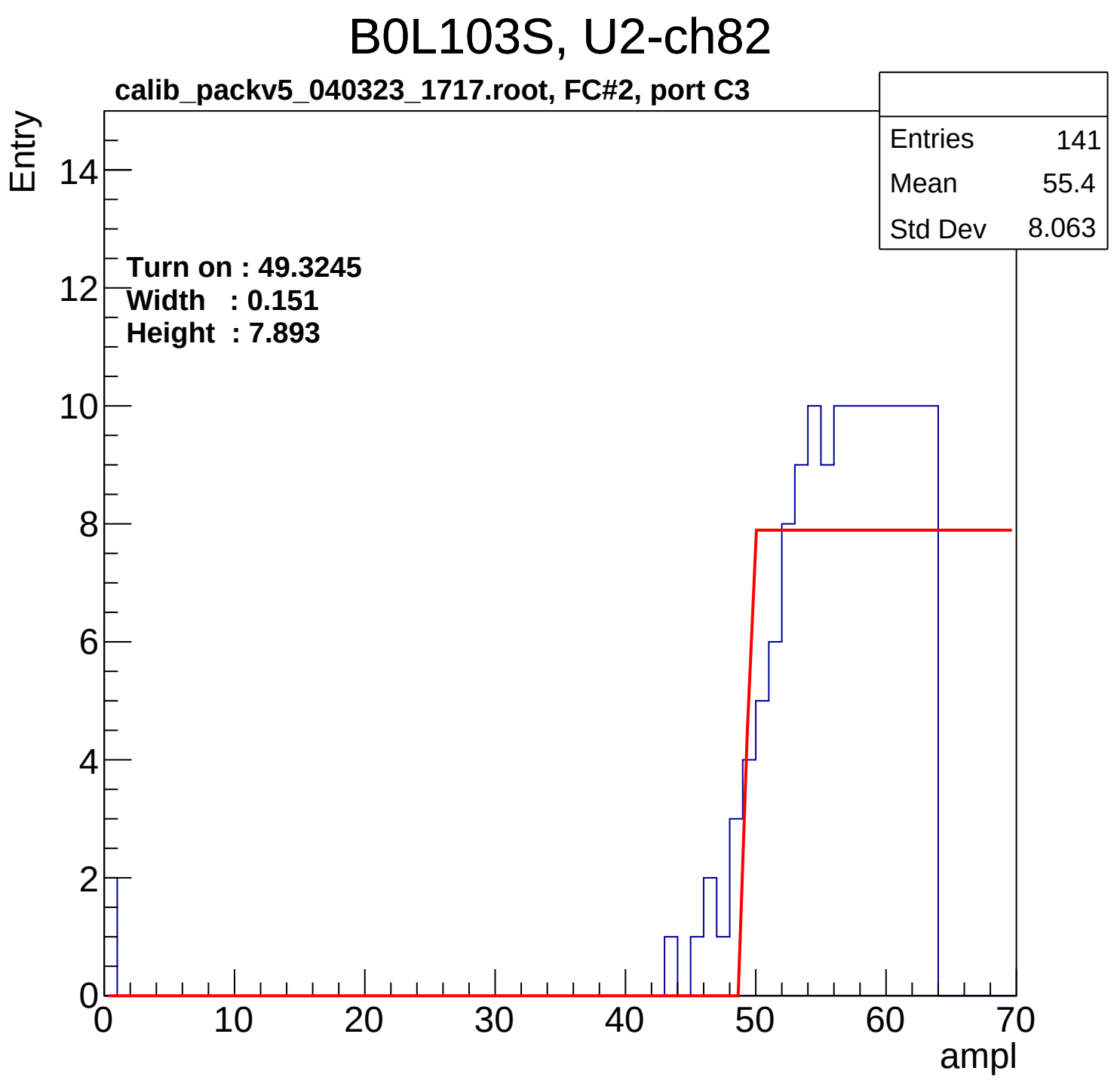
B0L103S, U2-ch82
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 55.4
Std Dev 8.063
Turn on : 49.3245
Width : 0.151
Height : 7.893
Entry
ampl
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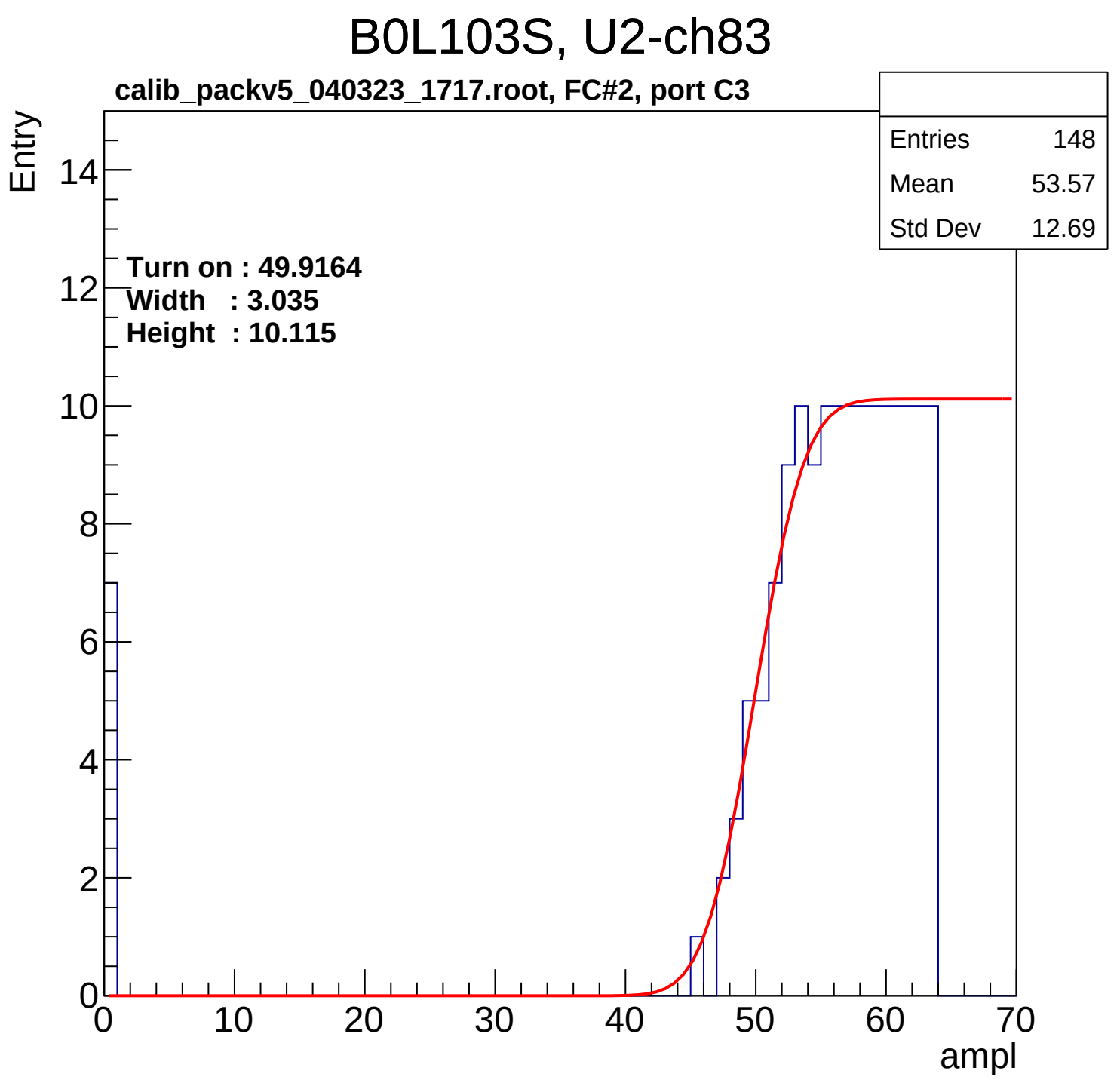
B0L103S, U2-ch83
calib_packv5_040323_1717.root, FC#2, port C3
Entries 148
Mean 53.57
Std Dev 12.69
Turn on : 49.9164
Width : 3.035
Height : 10.115
Entry
ampl
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4
6
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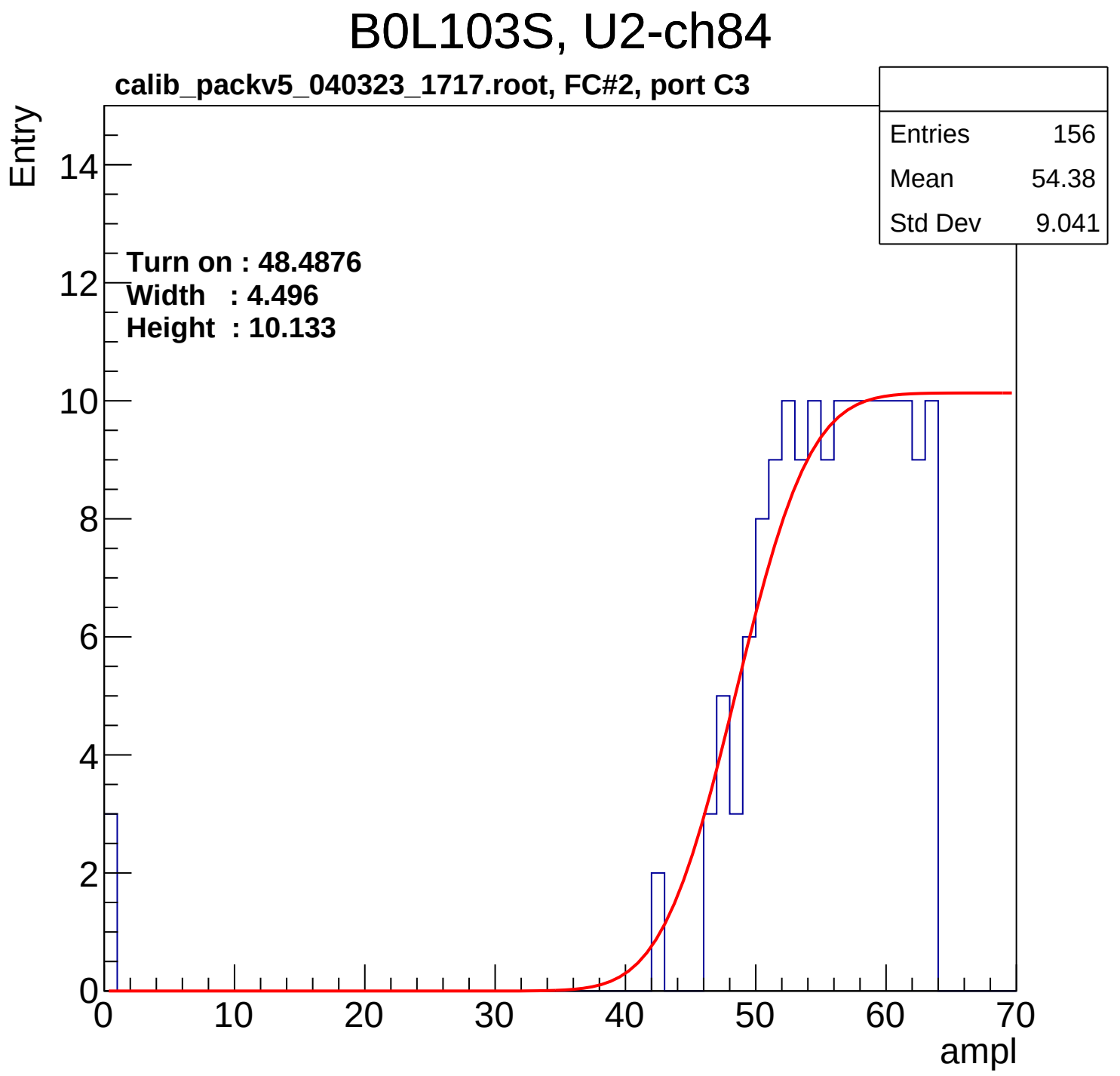
B0L103S, U2-ch84
calib_packv5_040323_1717.root, FC#2, port C3
Entries 156
Mean 54.38
Std Dev 9.041
Turn on : 48.4876
Width : 4.496
Height : 10.133
Entry
ampl
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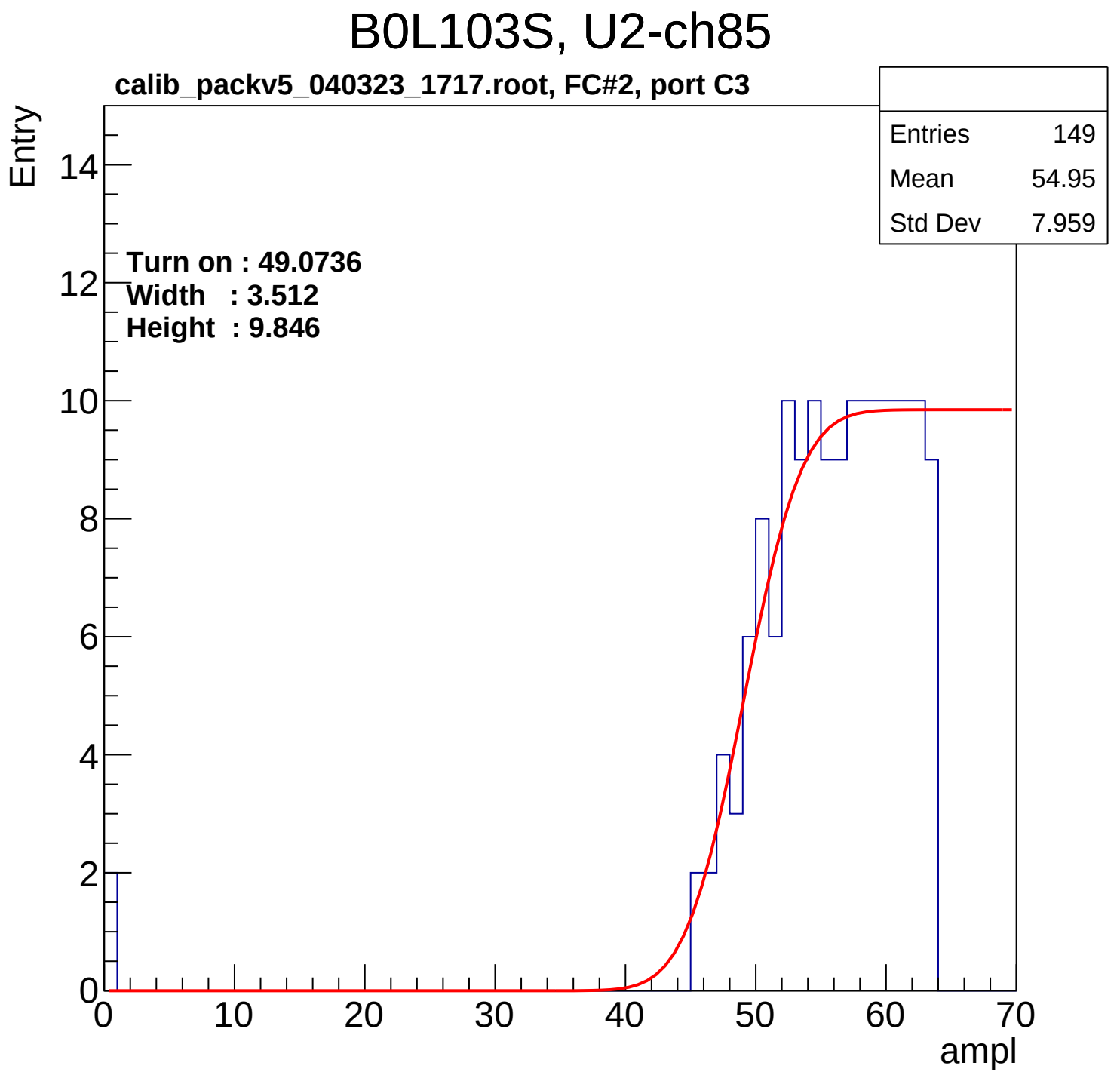
B0L103S, U2-ch85
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 54.95
Std Dev 7.959
Turn on : 49.0736
Width : 3.512
Height : 9.846
Entry
ampl
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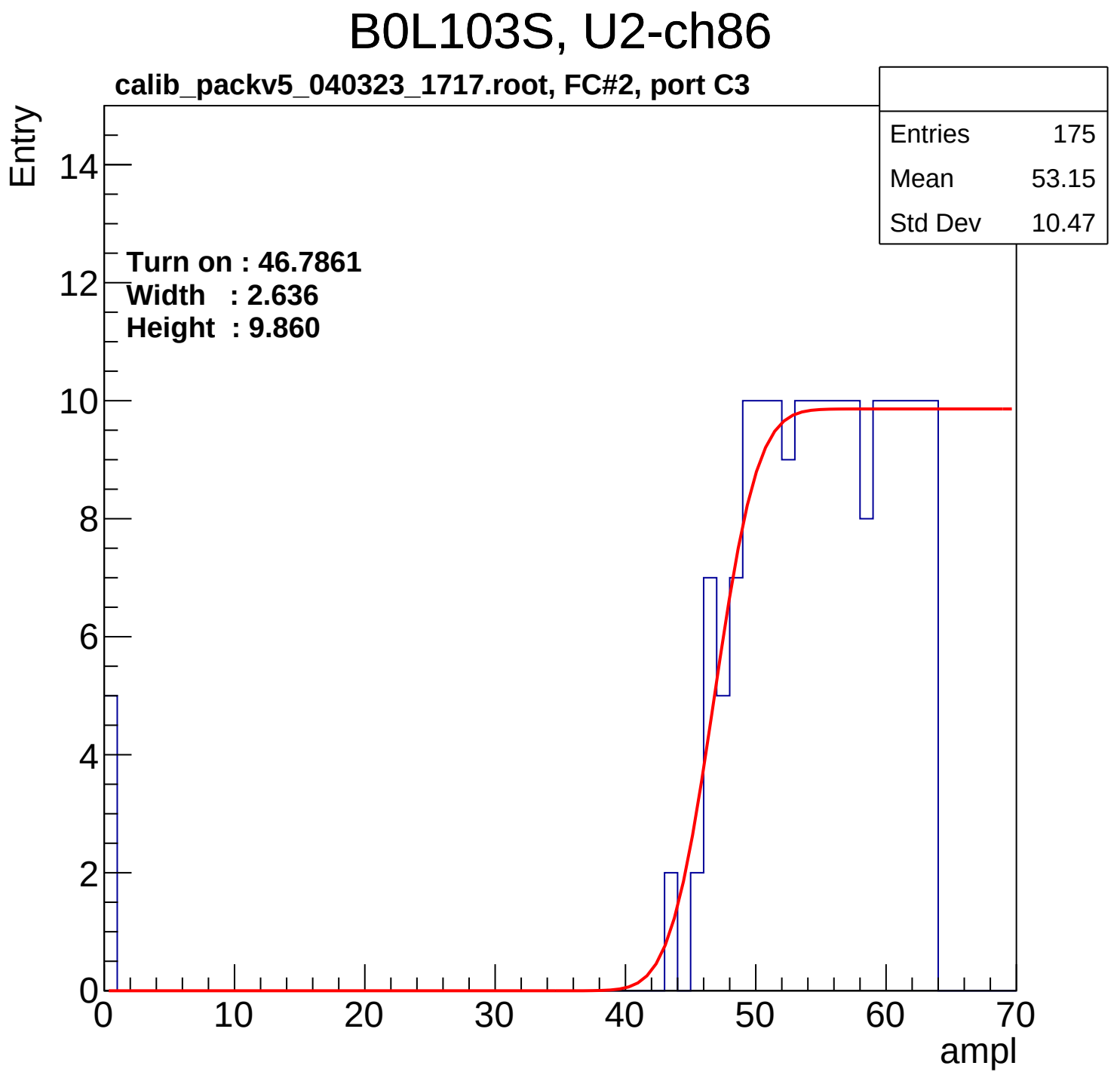
B0L103S, U2-ch86
calib_packv5_040323_1717.root, FC#2, port C3
Entries 175
Mean 53.15
Std Dev 10.47
Turn on : 46.7861
Width : 2.636
Height : 9.860
Entry
ampl
0
2
4
6
8
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12
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10
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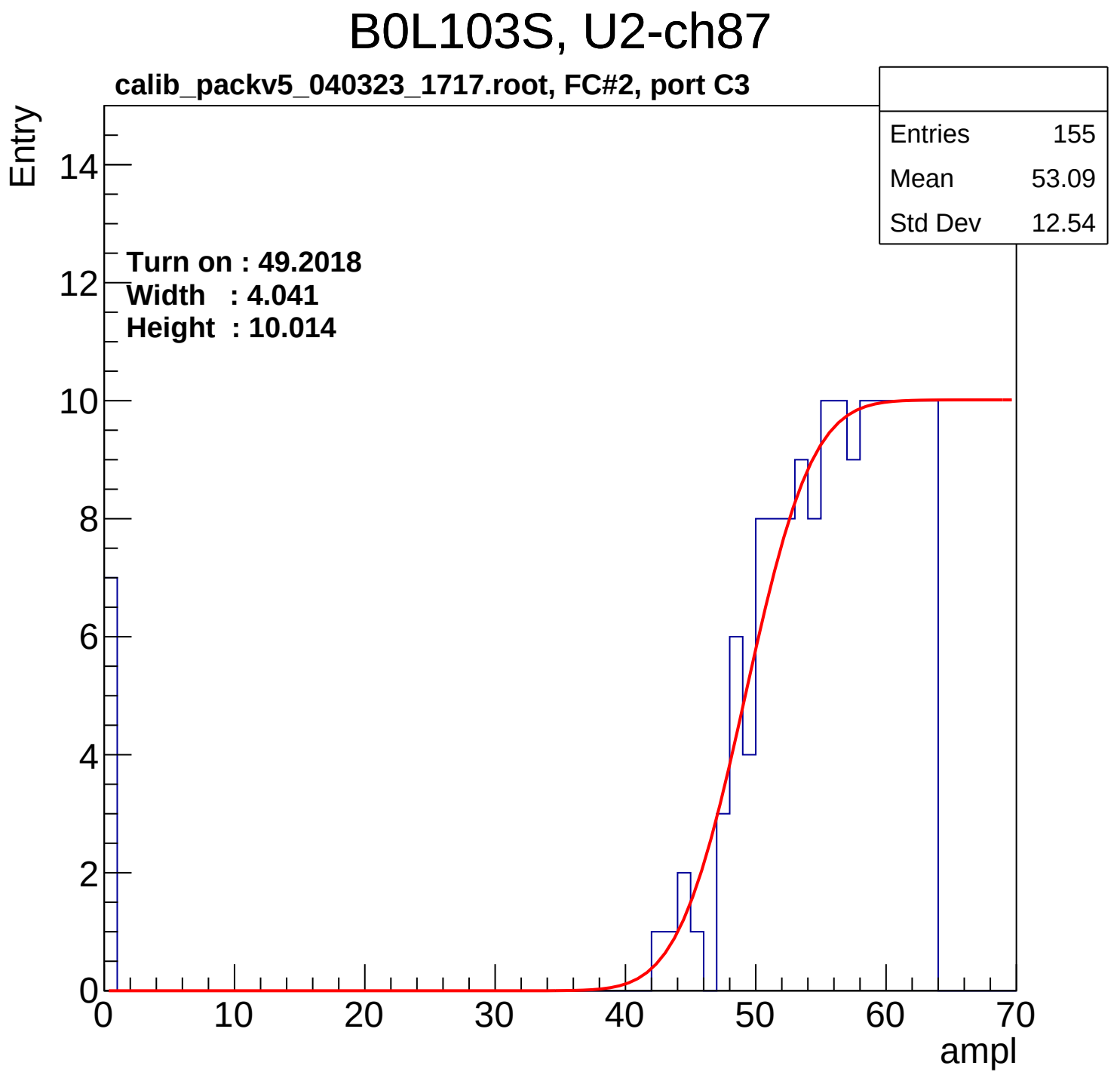
B0L103S, U2-ch87
calib_packv5_040323_1717.root, FC#2, port C3
Entries 155
Mean 53.09
Std Dev 12.54
Turn on : 49.2018
Width : 4.041
Height : 10.014
Entry
ampl
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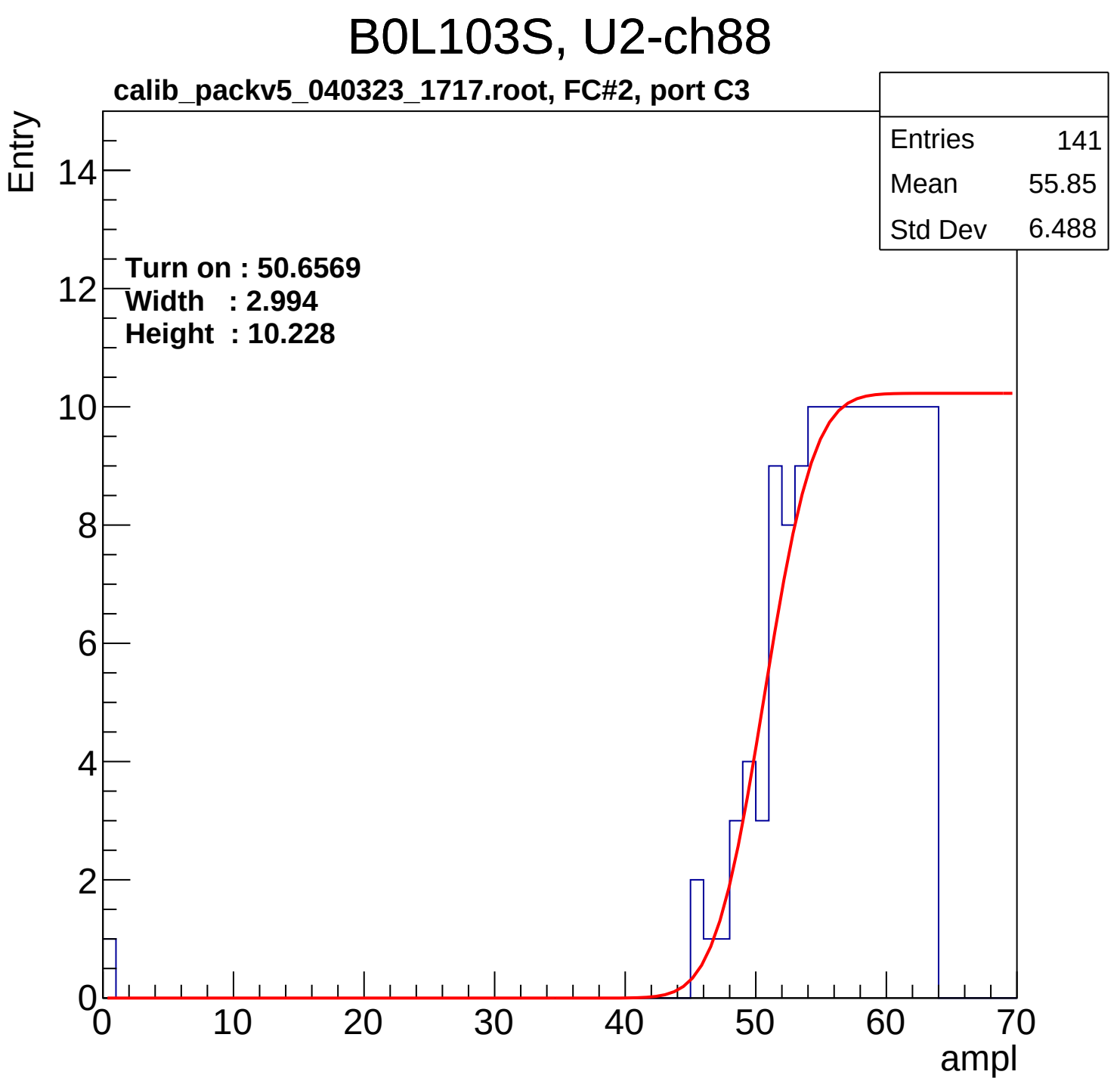
B0L103S, U2-ch88
calib_packv5_040323_1717.root, FC#2, port C3
Entries 141
Mean 55.85
Std Dev 6.488
Turn on : 50.6569
Width : 2.994
Height : 10.228
Entry
ampl
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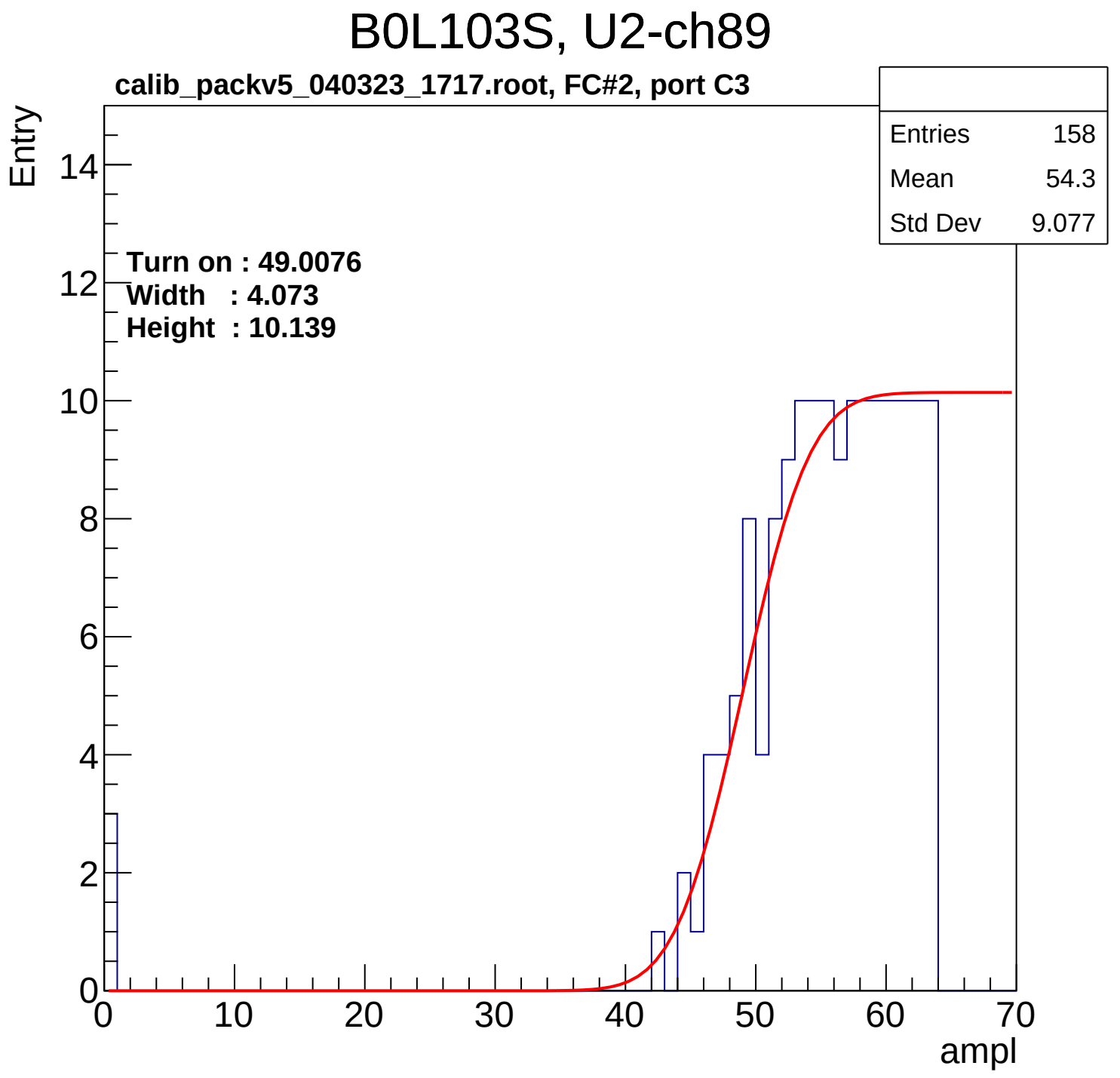
B0L103S, U2-ch89
calib_packv5_040323_1717.root, FC#2, port C3
Entries 158
Mean 54.3
Std Dev 9.077
Turn on : 49.0076
Width : 4.073
Height : 10.139
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ampl
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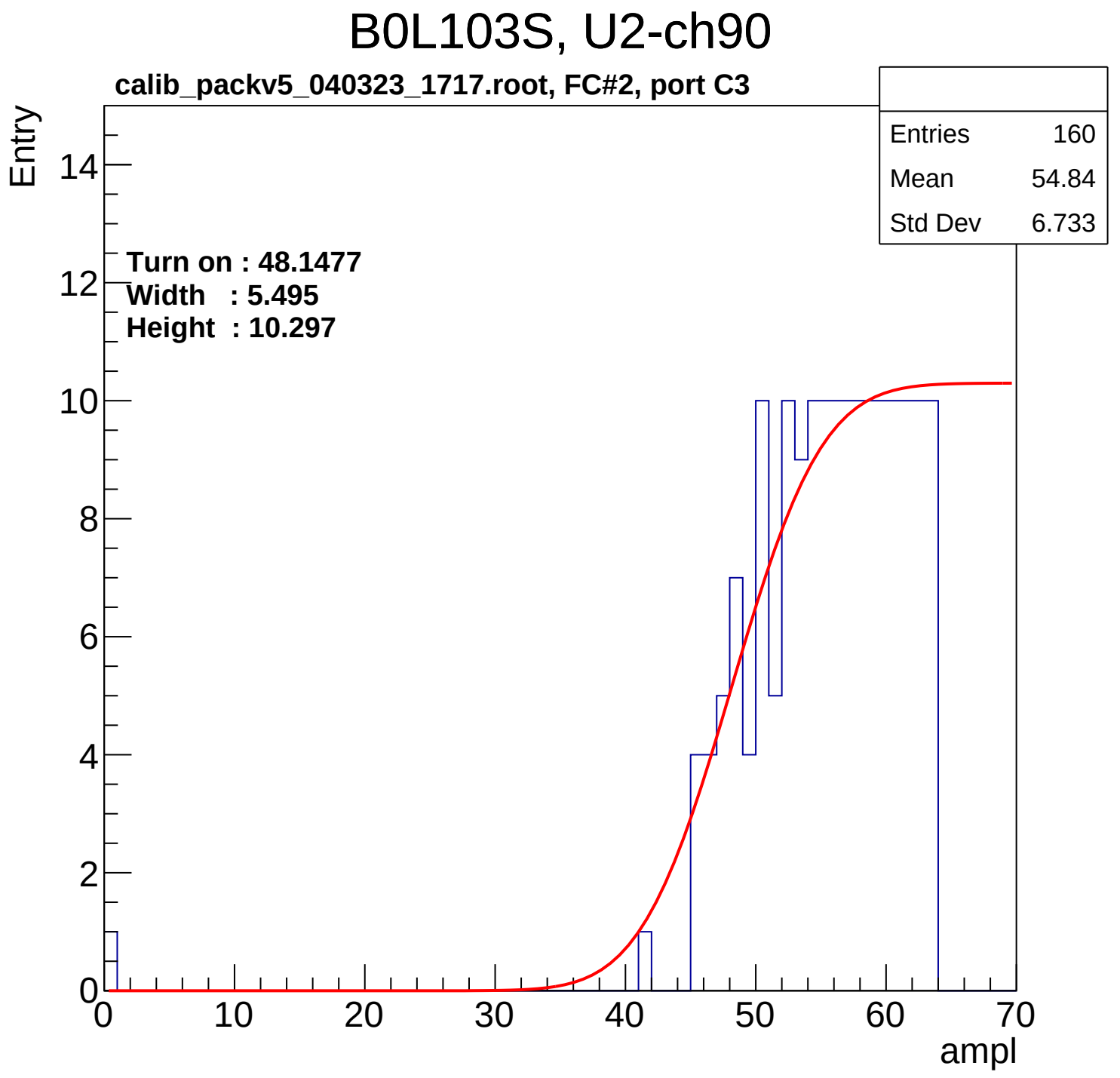
B0L103S, U2-ch90
calib_packv5_040323_1717.root, FC#2, port C3
Entries 160
Mean 54.84
Std Dev 6.733
Turn on : 48.1477
Width : 5.495
Height : 10.297
Entry
ampl
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8
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0
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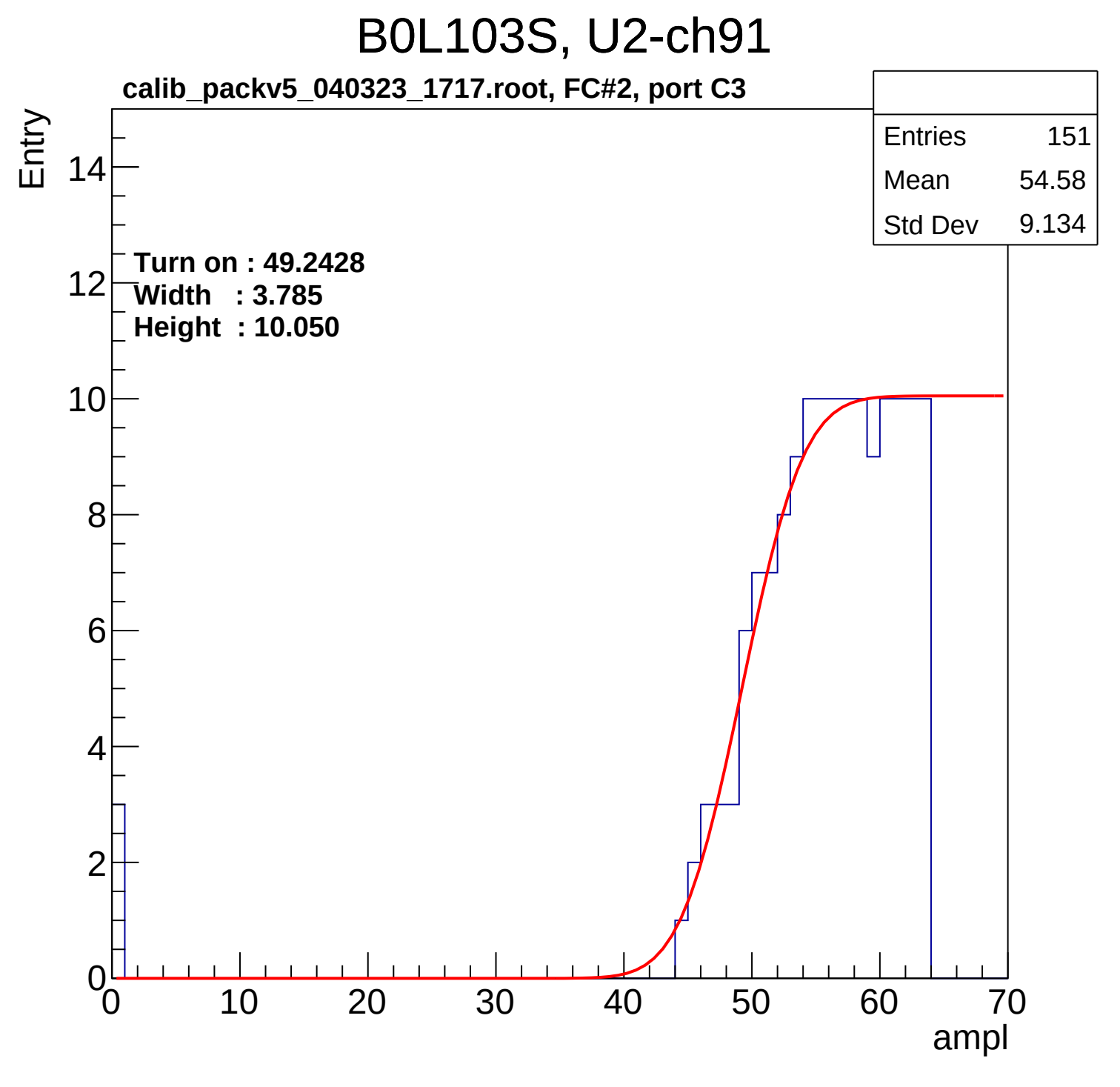
B0L103S, U2-ch91
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 54.58
Std Dev 9.134
Turn on : 49.2428
Width : 3.785
Height : 10.050
Entry
ampl
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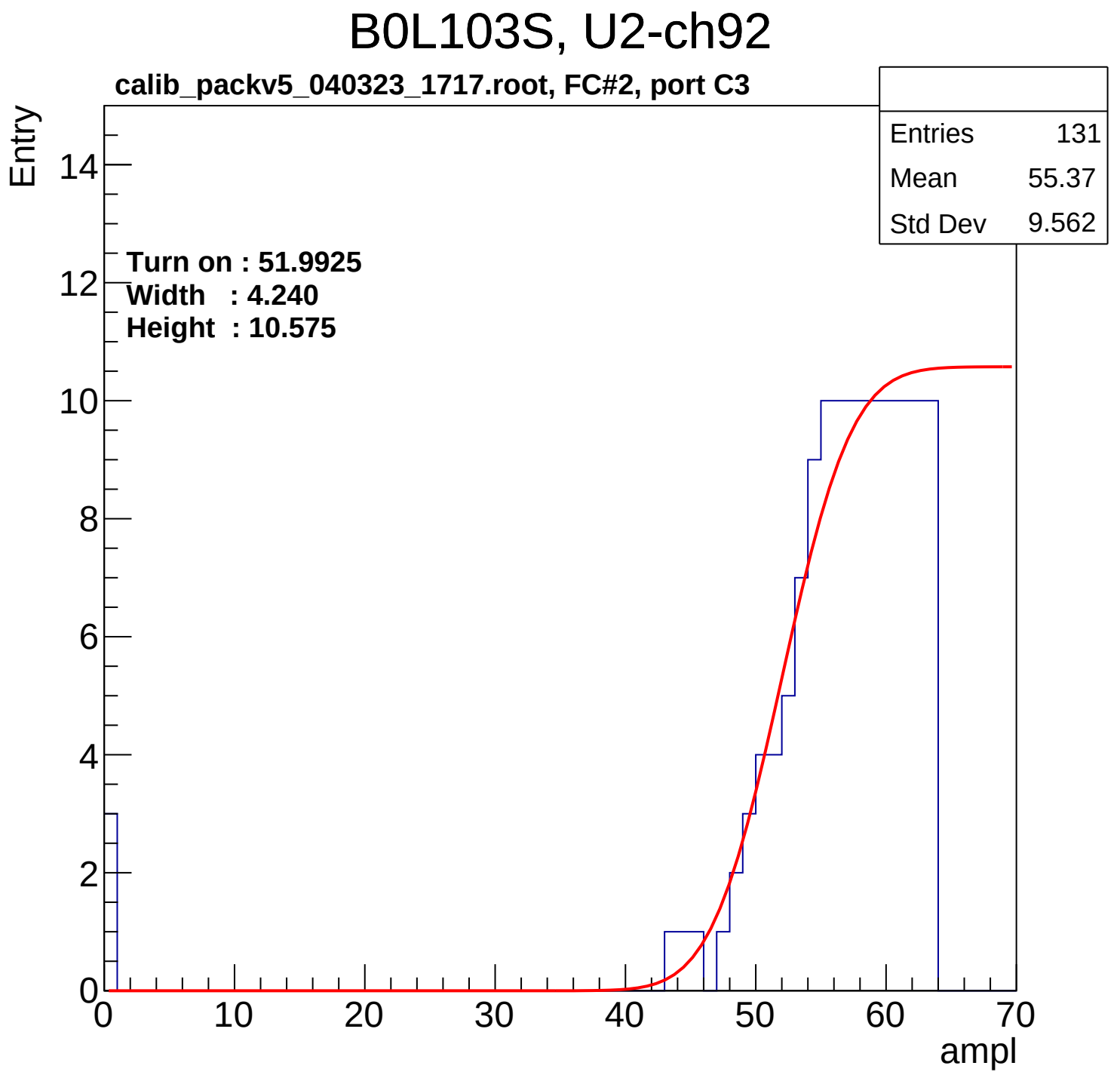
B0L103S, U2-ch92
calib_packv5_040323_1717.root, FC#2, port C3
Entries 131
Mean 55.37
Std Dev 9.562
Turn on : 51.9925
Width : 4.240
Height : 10.575
Entry
ampl
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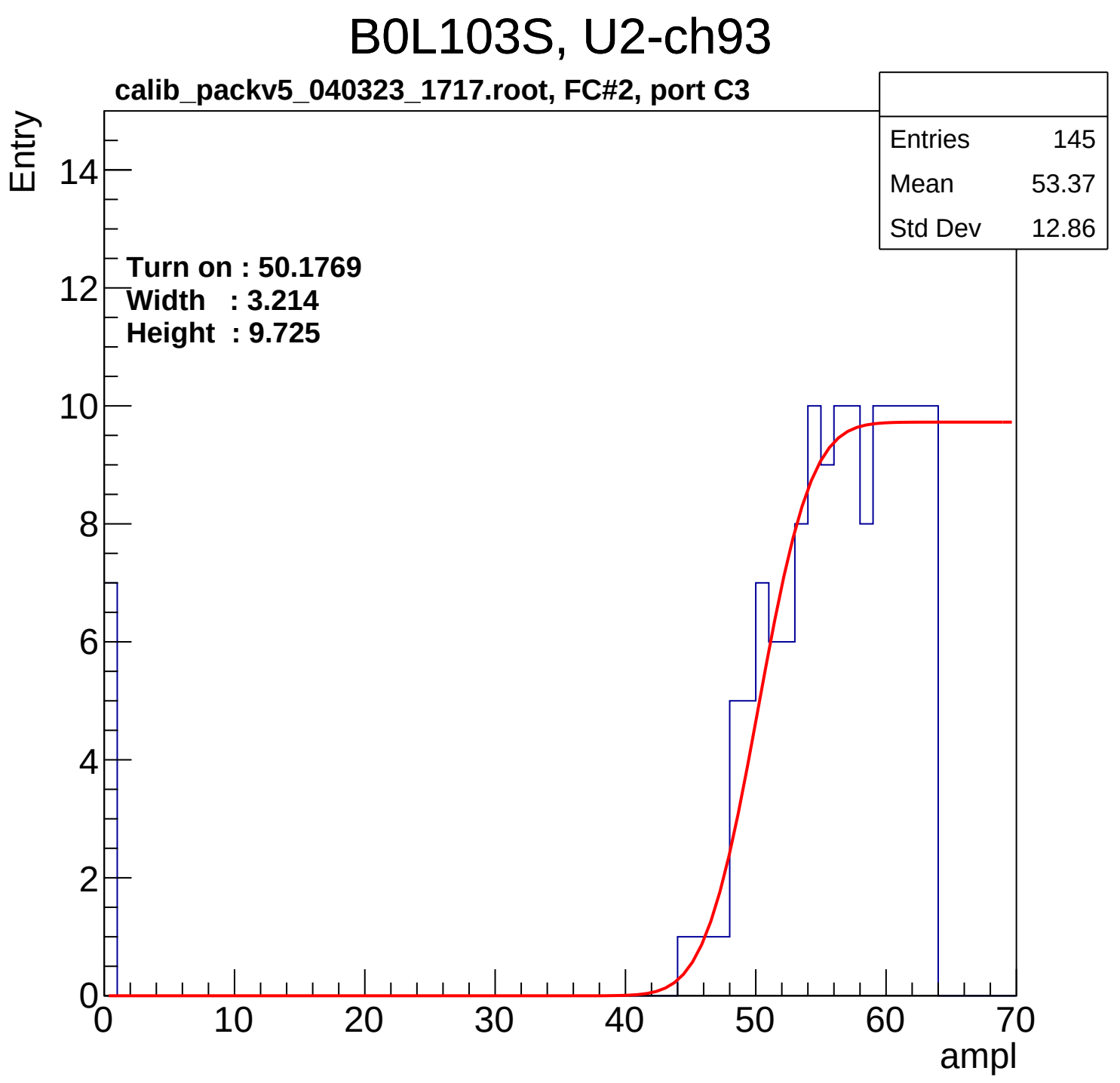
B0L103S, U2-ch93
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 53.37
Std Dev 12.86
Turn on : 50.1769
Width : 3.214
Height : 9.725
Entry
ampl
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6
8
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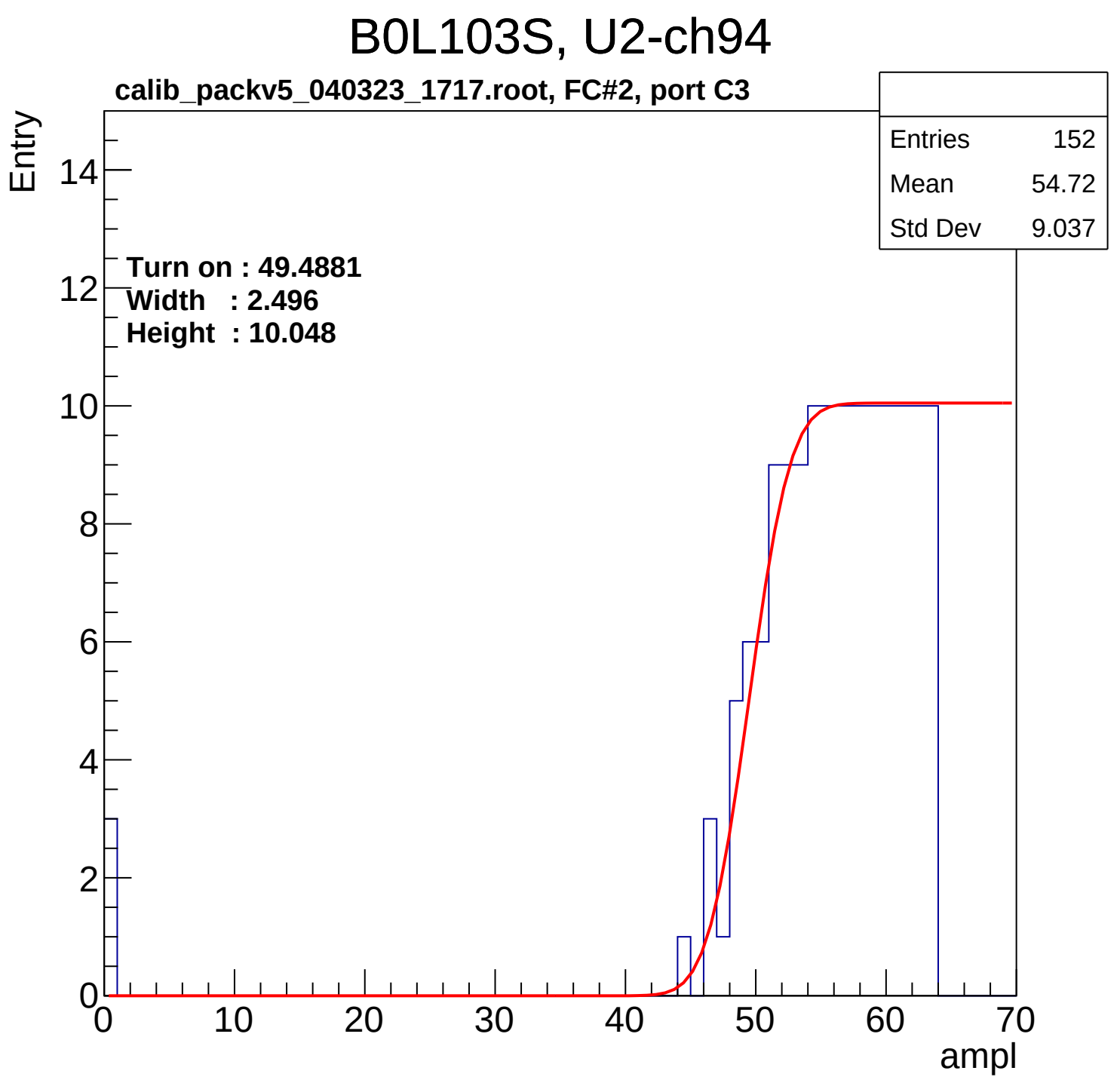
B0L103S, U2-ch94
calib_packv5_040323_1717.root, FC#2, port C3
Entries 152
Mean 54.72
Std Dev 9.037
Turn on : 49.4881
Width : 2.496
Height : 10.048
Entry
ampl
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2
4
6
8
10
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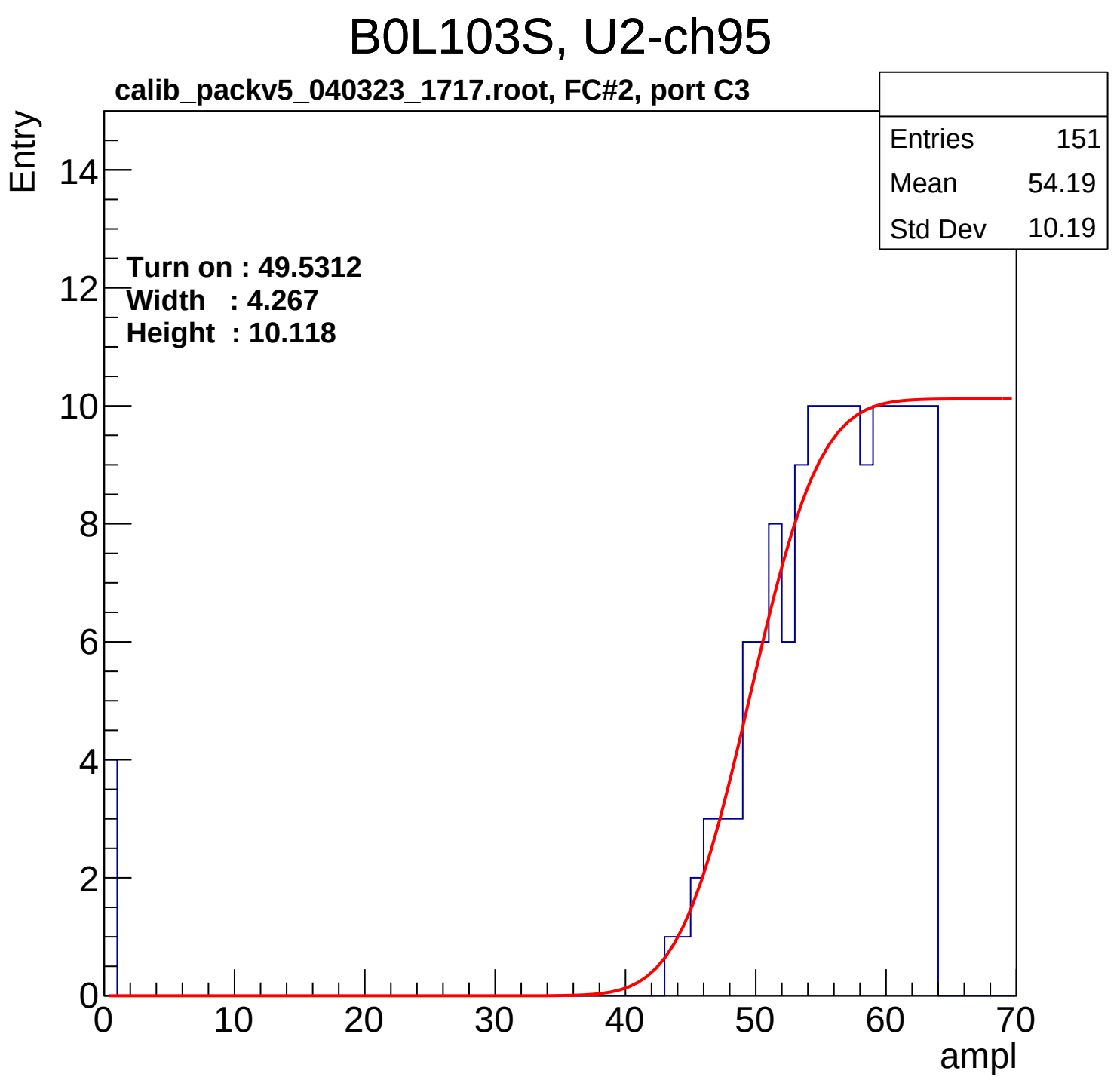
B0L103S, U2-ch95
calib_packv5_040323_1717.root, FC#2, port C3
Entries 151
Mean 54.19
Std Dev 10.19
Turn on : 49.5312
Width : 4.267
Height : 10.118
Entry
ampl
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6
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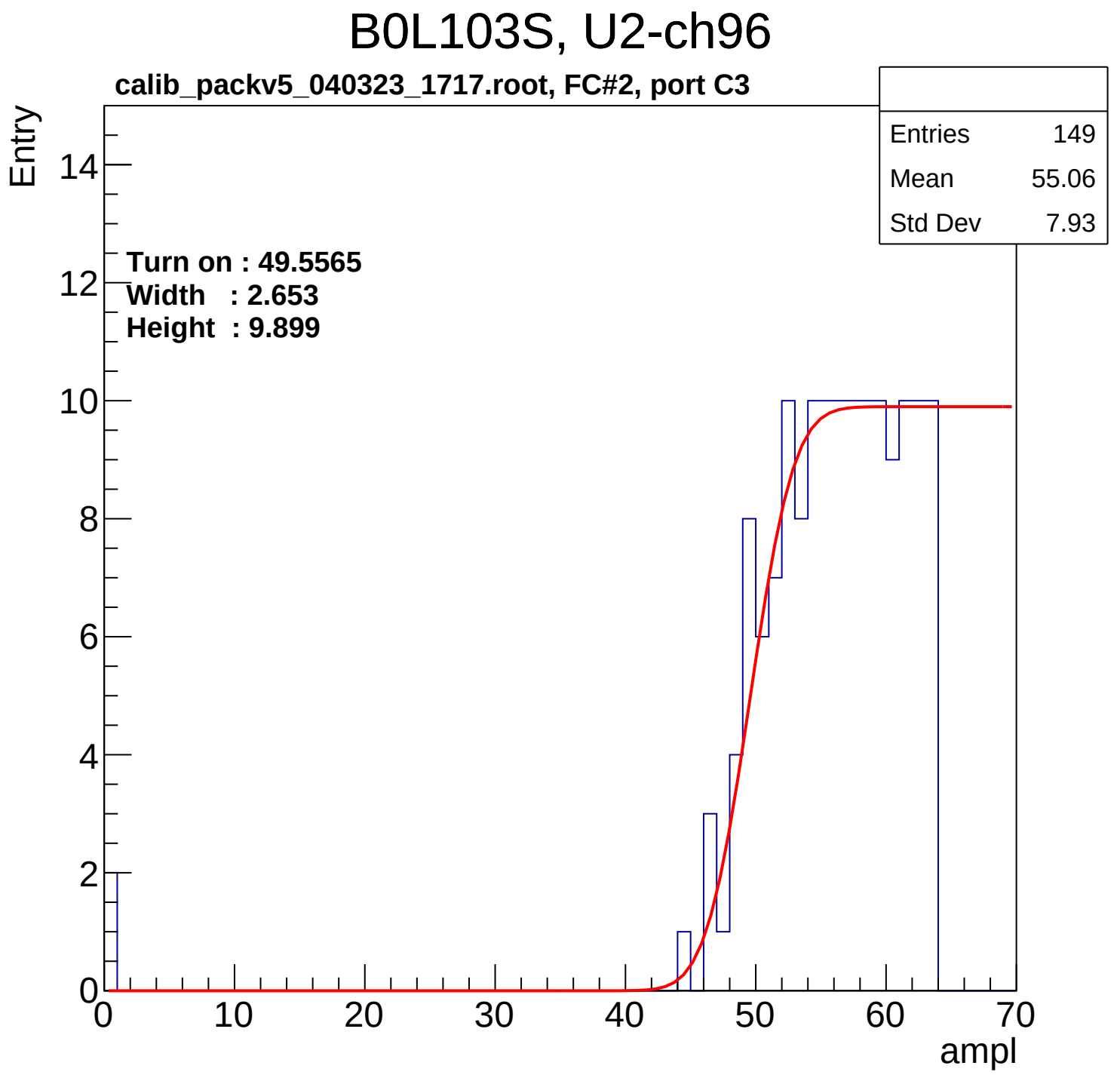
B0L103S, U2-ch96
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 55.06
Std Dev 7.93
Turn on : 49.5565
Width : 2.653
Height : 9.899
Entry
ampl
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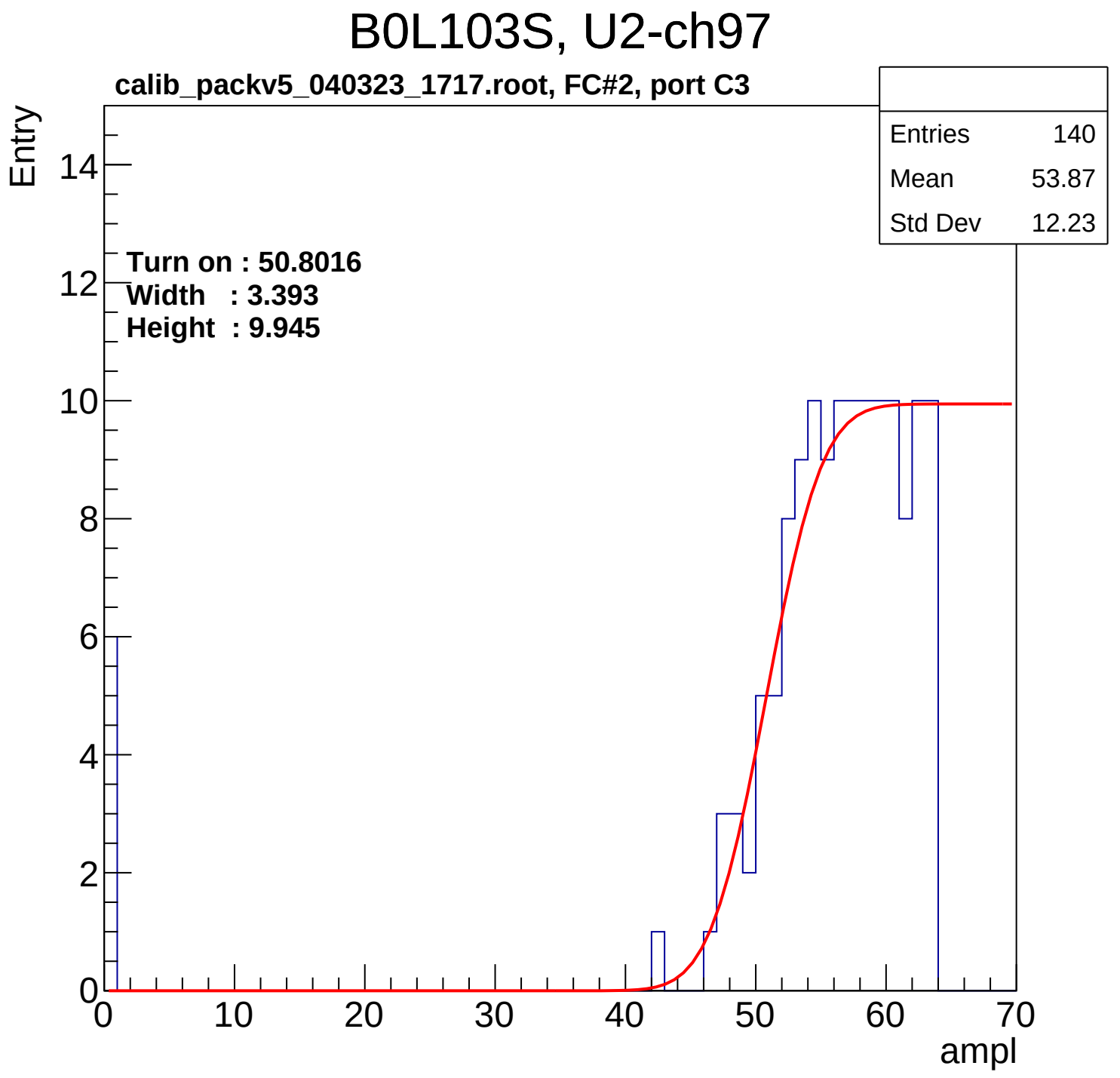
B0L103S, U2-ch97
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 53.87
Std Dev 12.23
Turn on : 50.8016
Width : 3.393
Height : 9.945
Entry
ampl
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4
6
8
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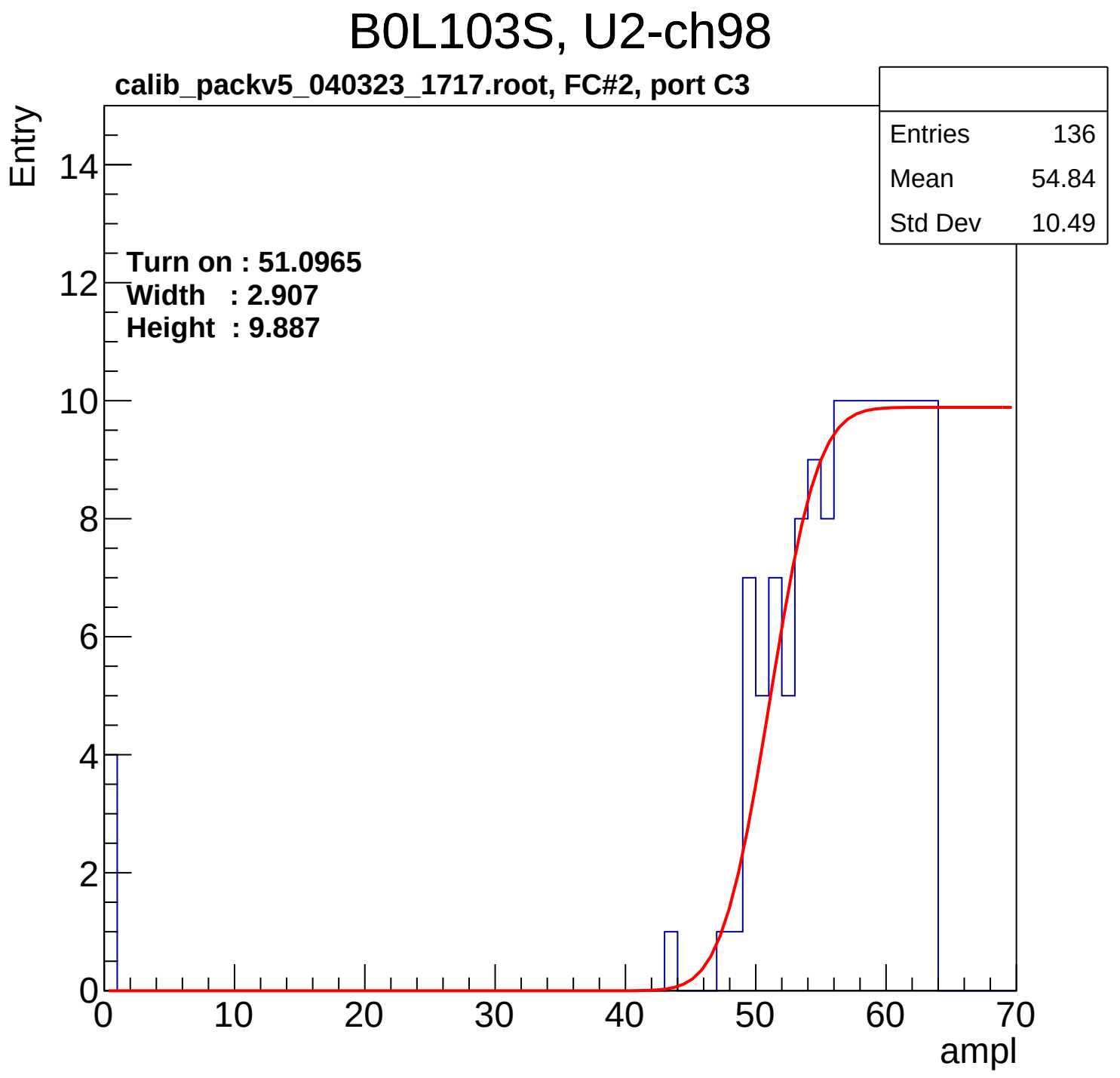
B0L103S, U2-ch98
calib_packv5_040323_1717.root, FC#2, port C3
Entries 136
Mean 54.84
Std Dev 10.49
Turn on : 51.0965
Width : 2.907
Height : 9.887
Entry
ampl
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6
8
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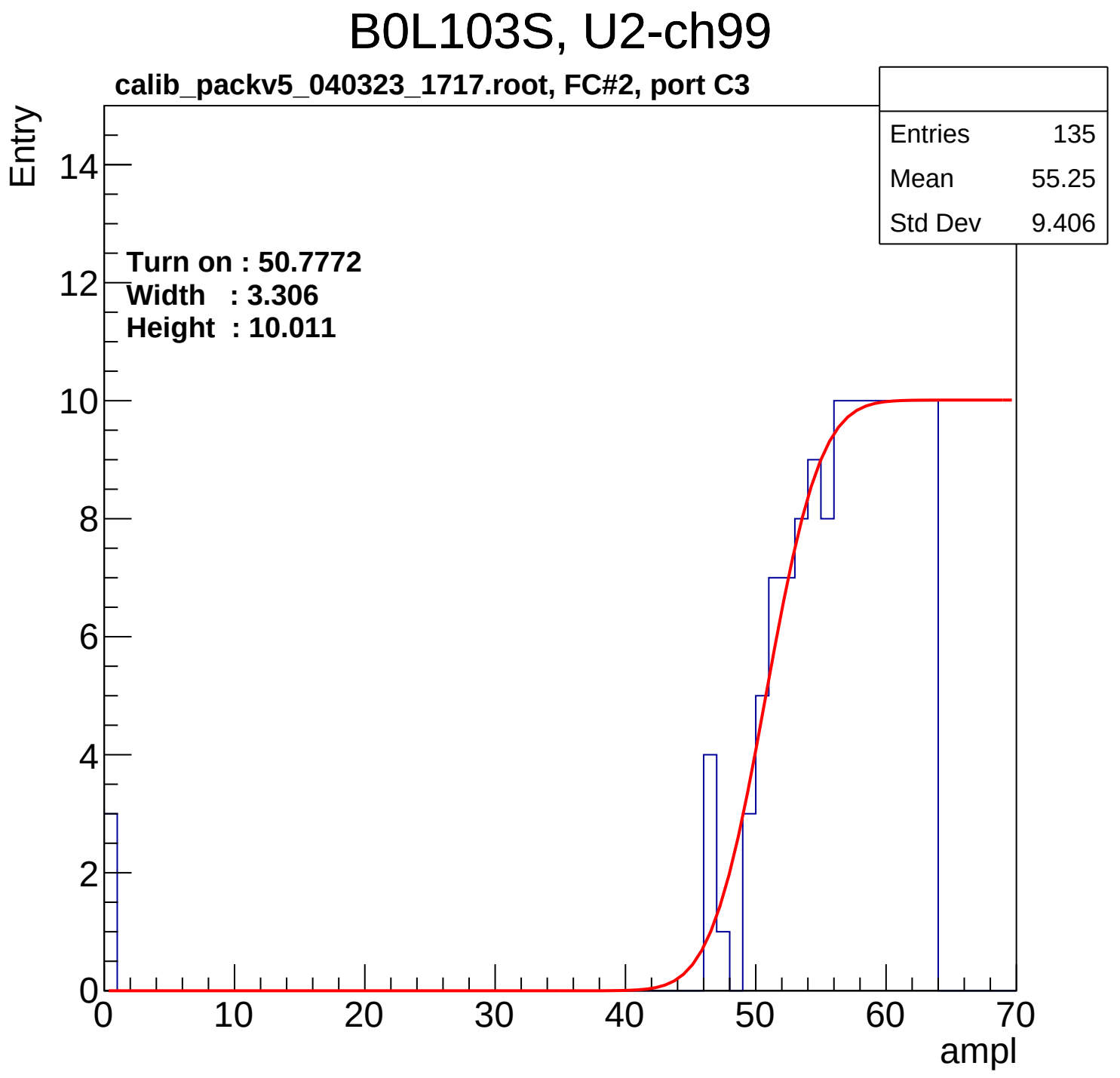
B0L103S, U2-ch99
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 55.25
Std Dev 9.406
Turn on : 50.7772
Width : 3.306
Height : 10.011
Entry
ampl
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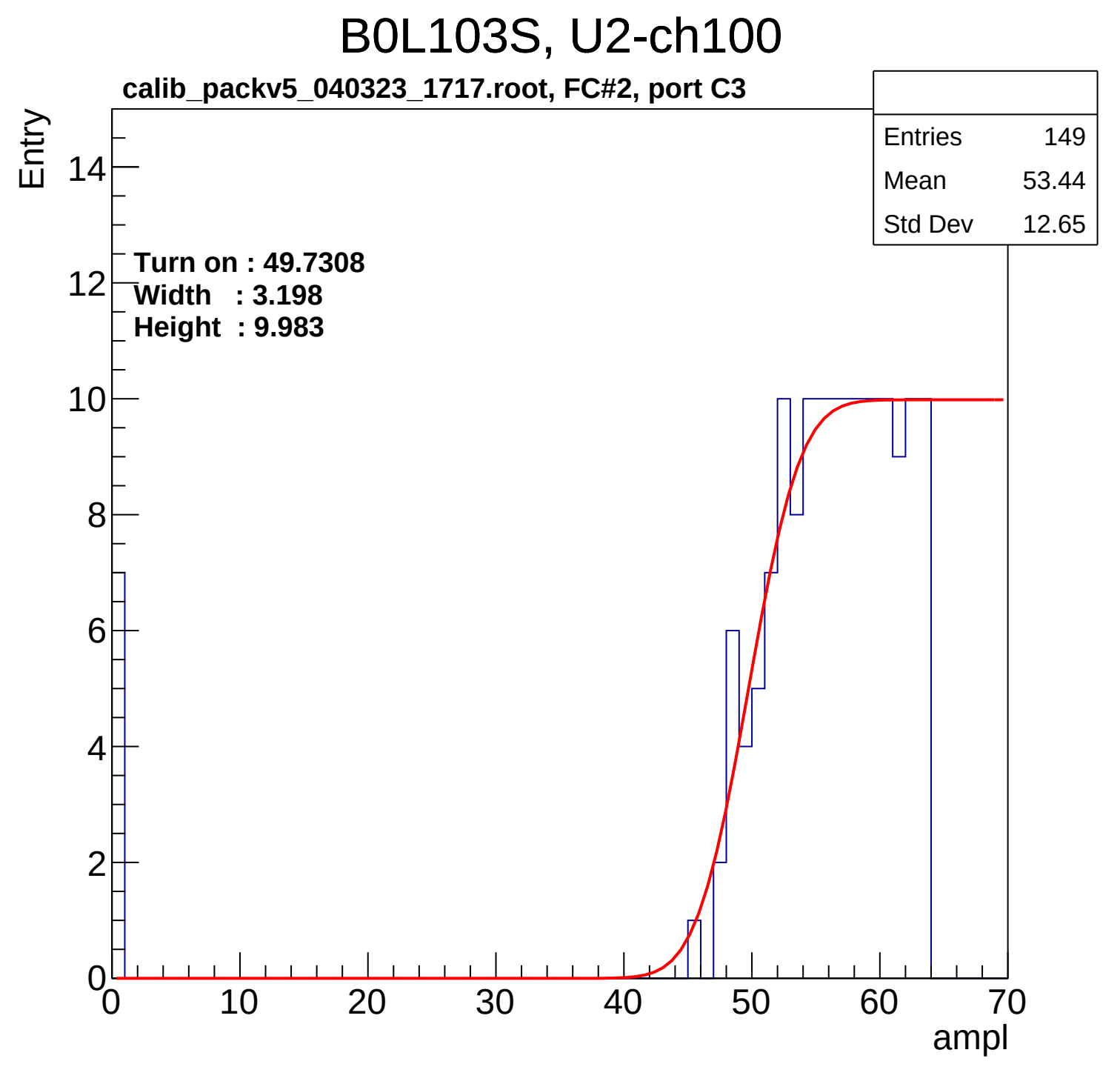
B0L103S, U2-ch100
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 53.44
Std Dev 12.65
Turn on : 49.7308
Width : 3.198
Height : 9.983
Entry
ampl
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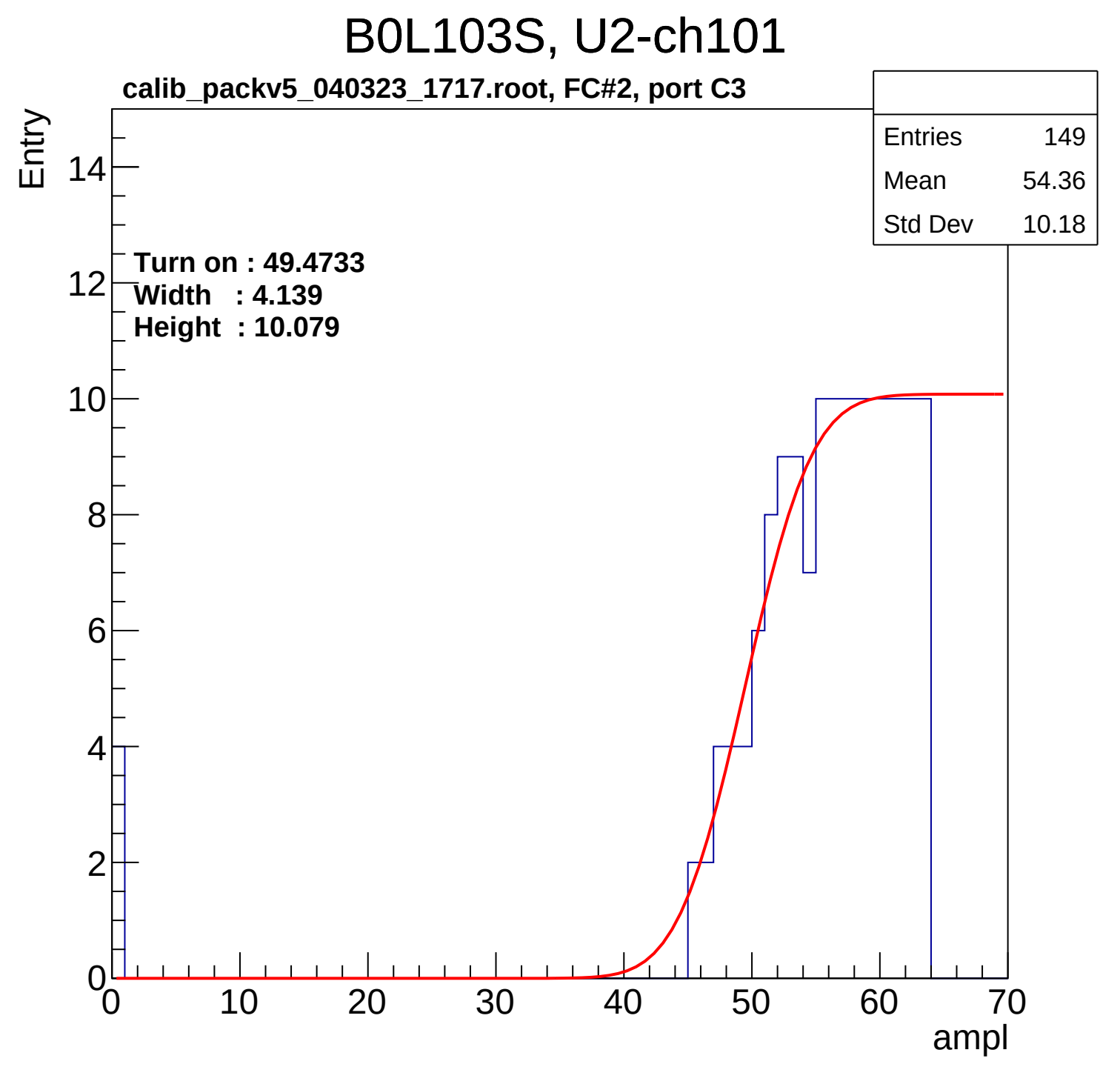
B0L103S, U2-ch101
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 54.36
Std Dev 10.18
Turn on : 49.4733
Width : 4.139
Height : 10.079
Entry
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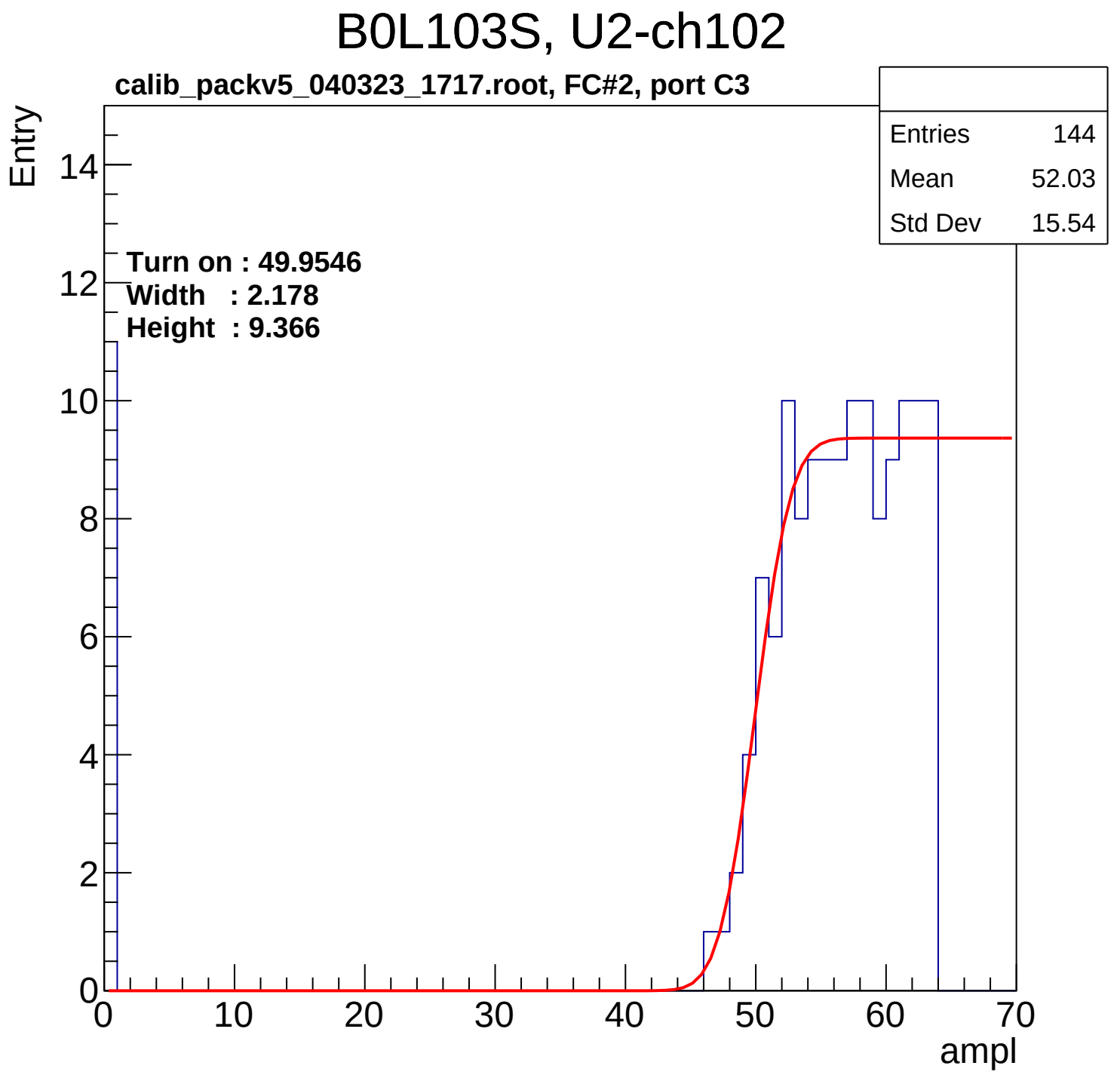
B0L103S, U2-ch102
calib_packv5_040323_1717.root, FC#2, port C3
Entries 144
Mean 52.03
Std Dev 15.54
Turn on : 49.9546
Width : 2.178
Height : 9.366
Entry
ampl
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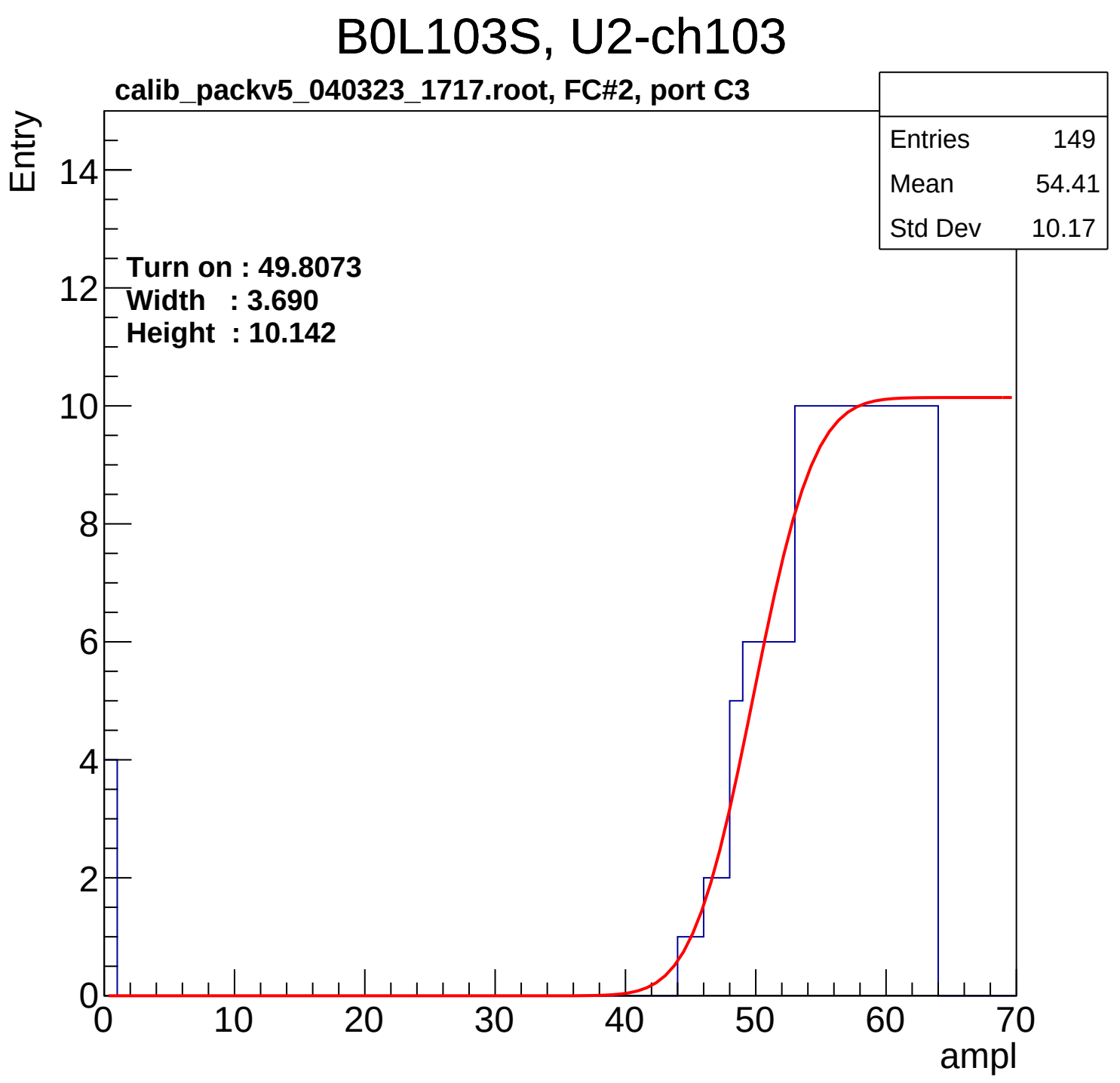
B0L103S, U2-ch103
calib_packv5_040323_1717.root, FC#2, port C3
Entries 149
Mean 54.41
Std Dev 10.17
Turn on : 49.8073
Width : 3.690
Height : 10.142
Entry
ampl
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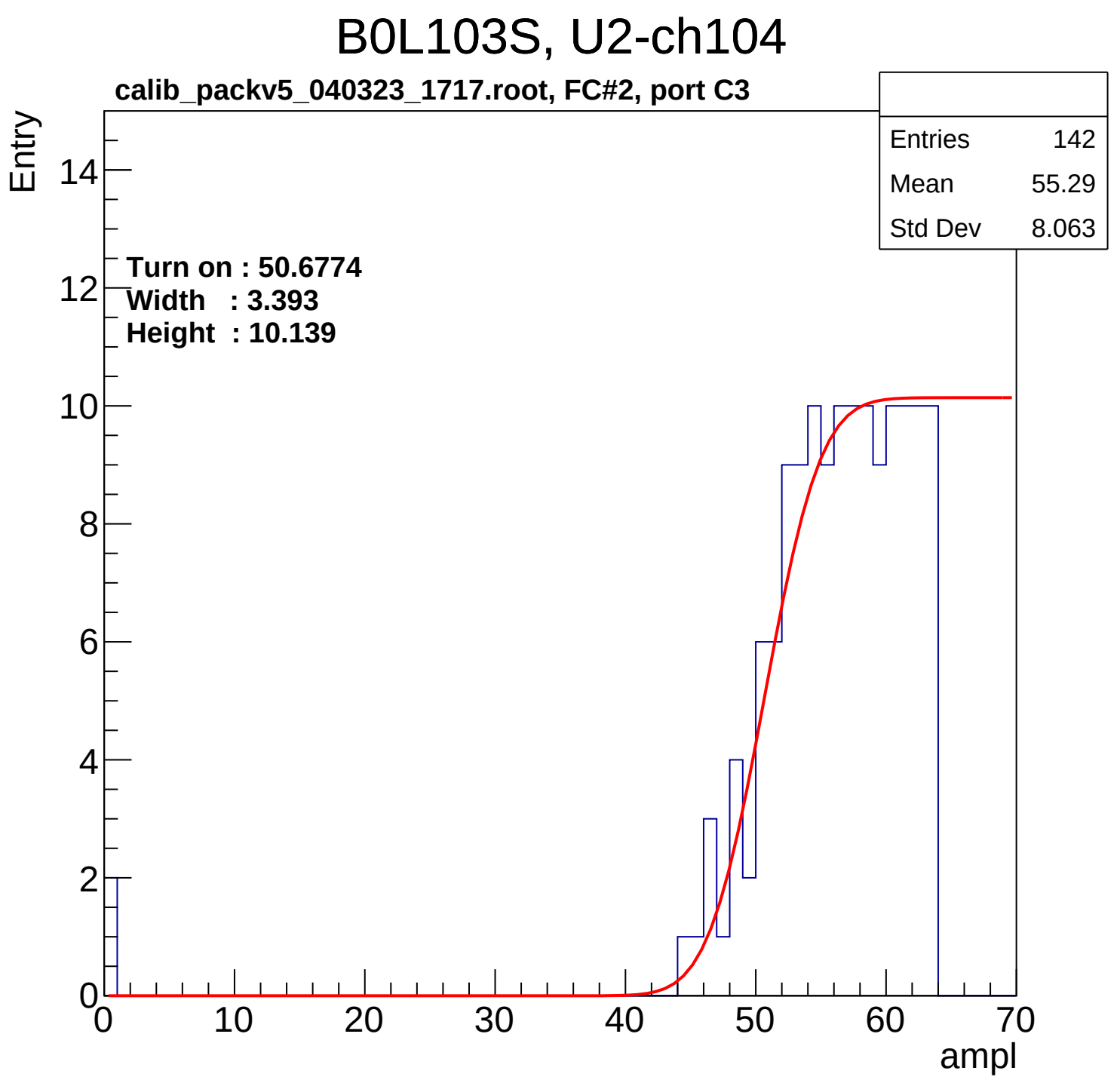
B0L103S, U2-ch104
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 55.29
Std Dev 8.063
Turn on : 50.6774
Width : 3.393
Height : 10.139
Entry
ampl
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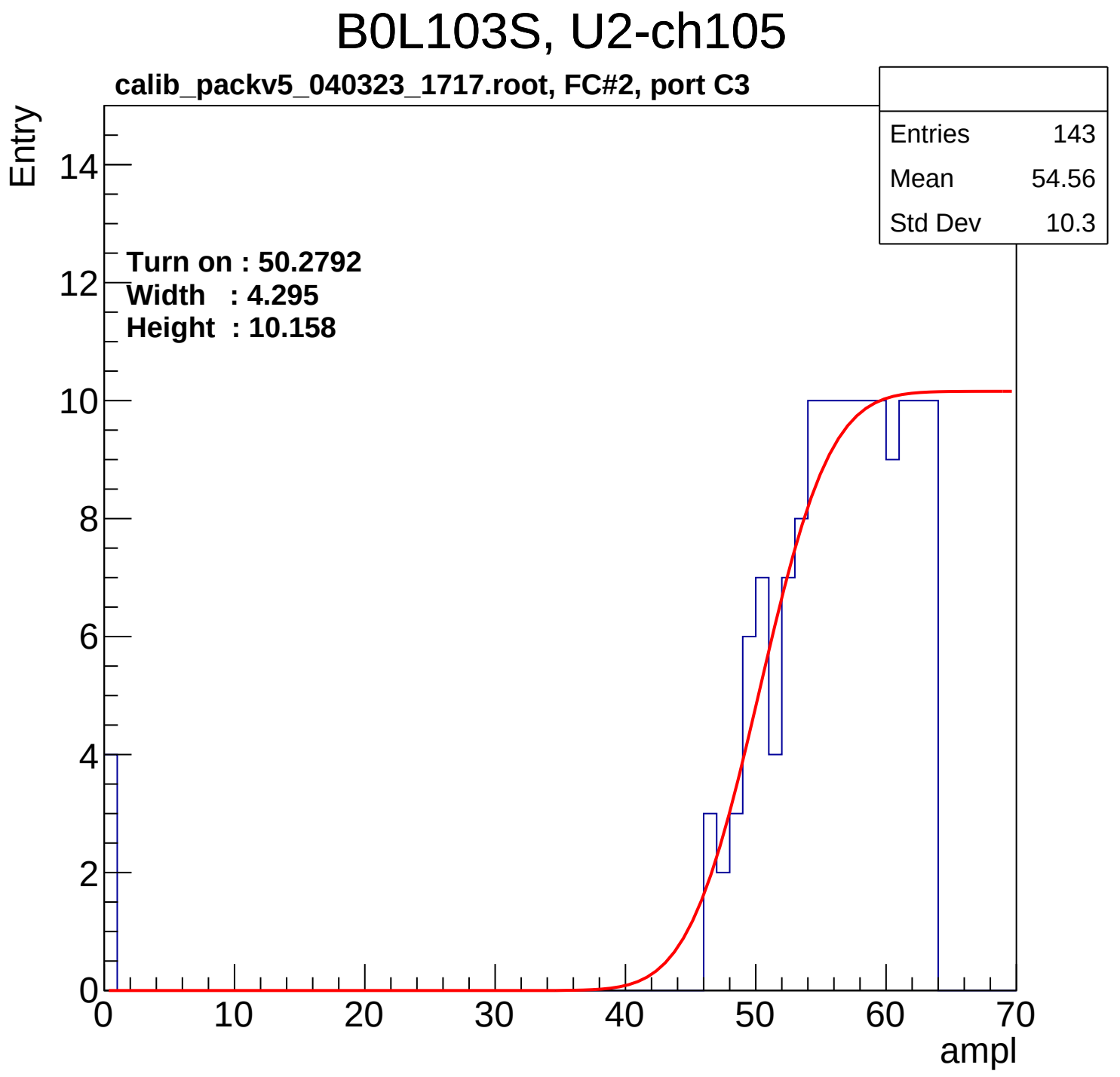
B0L103S, U2-ch105
calib_packv5_040323_1717.root, FC#2, port C3
Entries 143
Mean 54.56
Std Dev 10.3
Turn on : 50.2792
Width : 4.295
Height : 10.158
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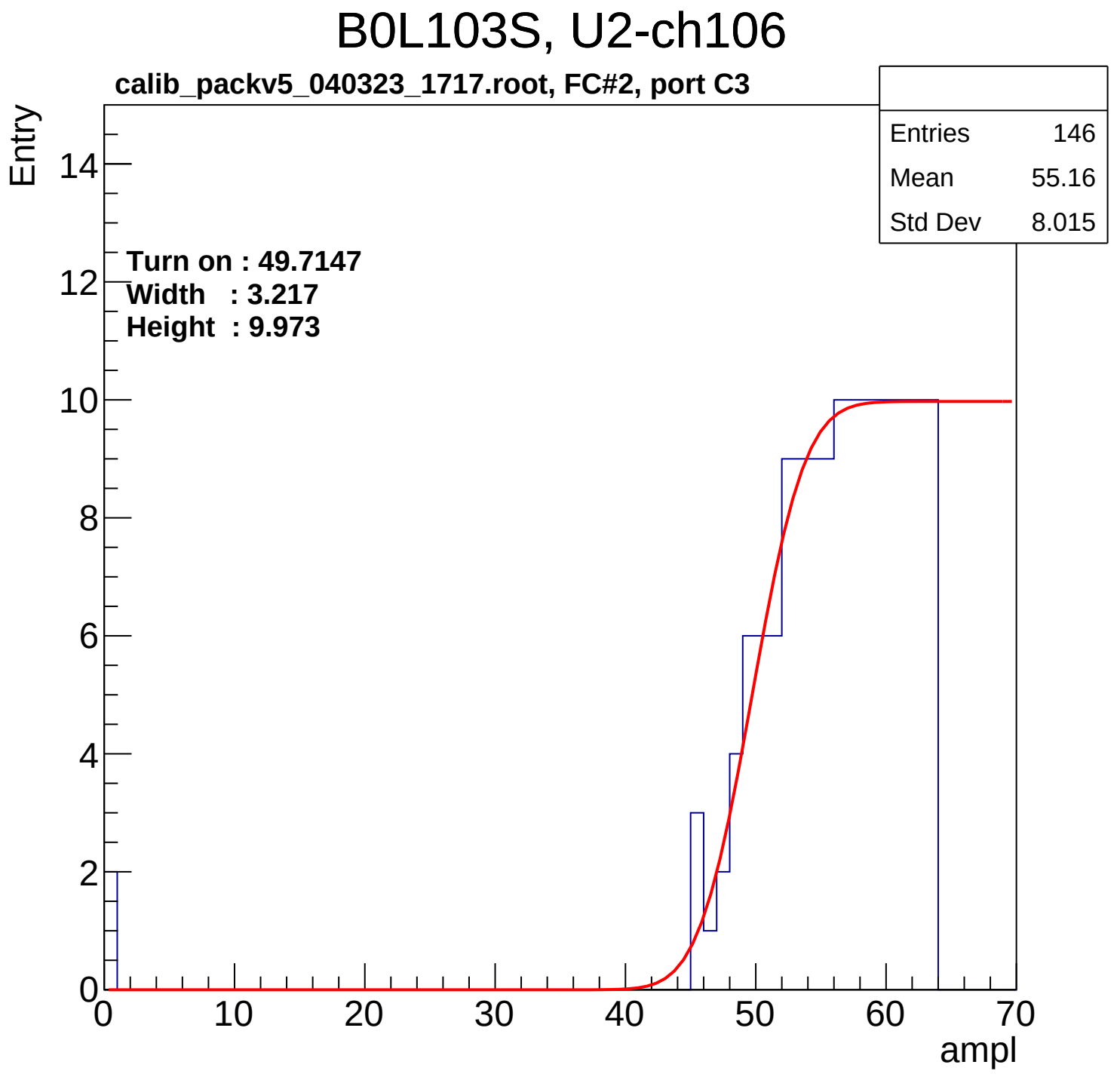
B0L103S, U2-ch106
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 55.16
Std Dev 8.015
Turn on : 49.7147
Width : 3.217
Height : 9.973
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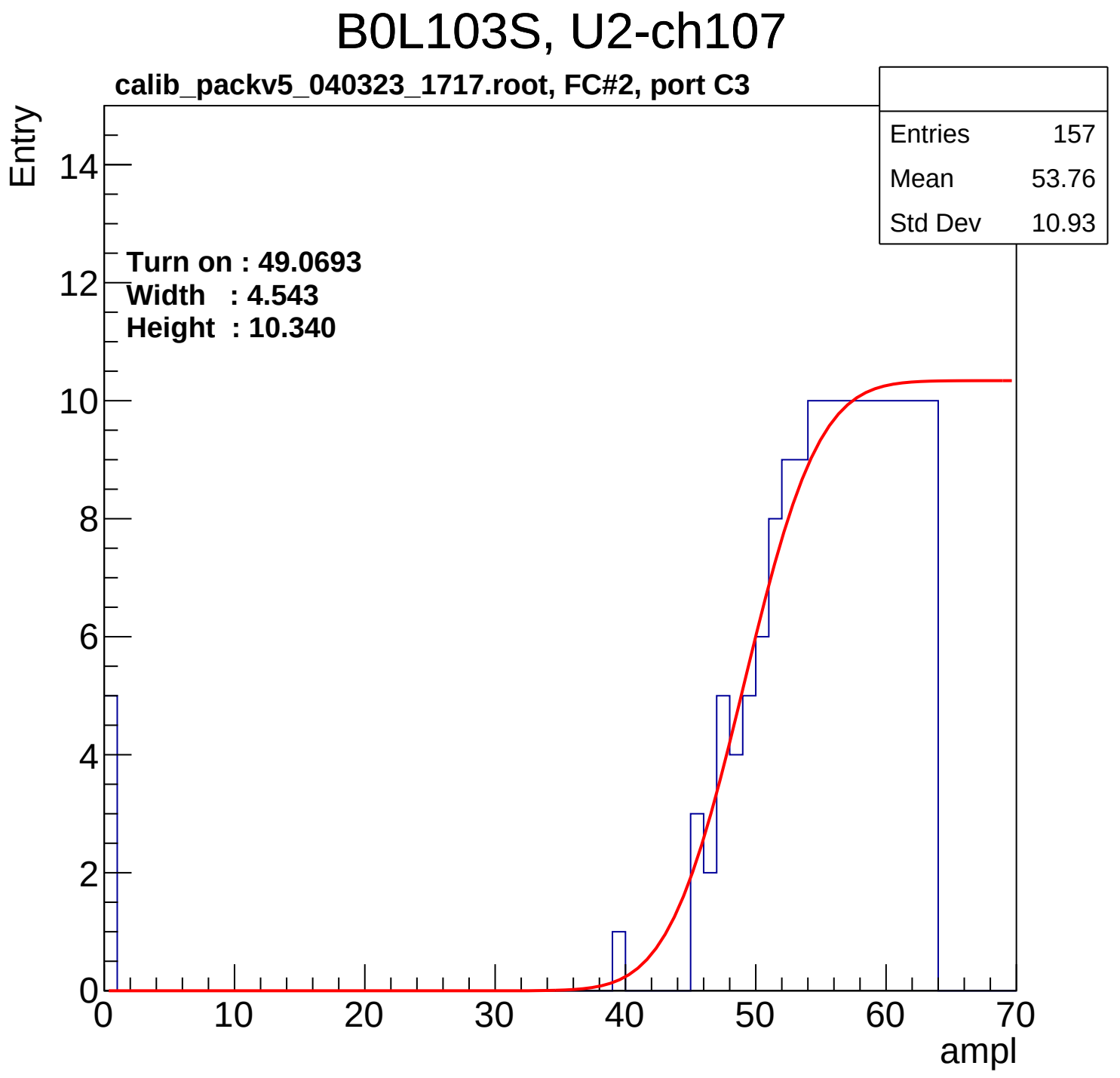
B0L103S, U2-ch107
calib_packv5_040323_1717.root, FC#2, port C3
Entries 157
Mean 53.76
Std Dev 10.93
Turn on : 49.0693
Width : 4.543
Height : 10.340
Entry
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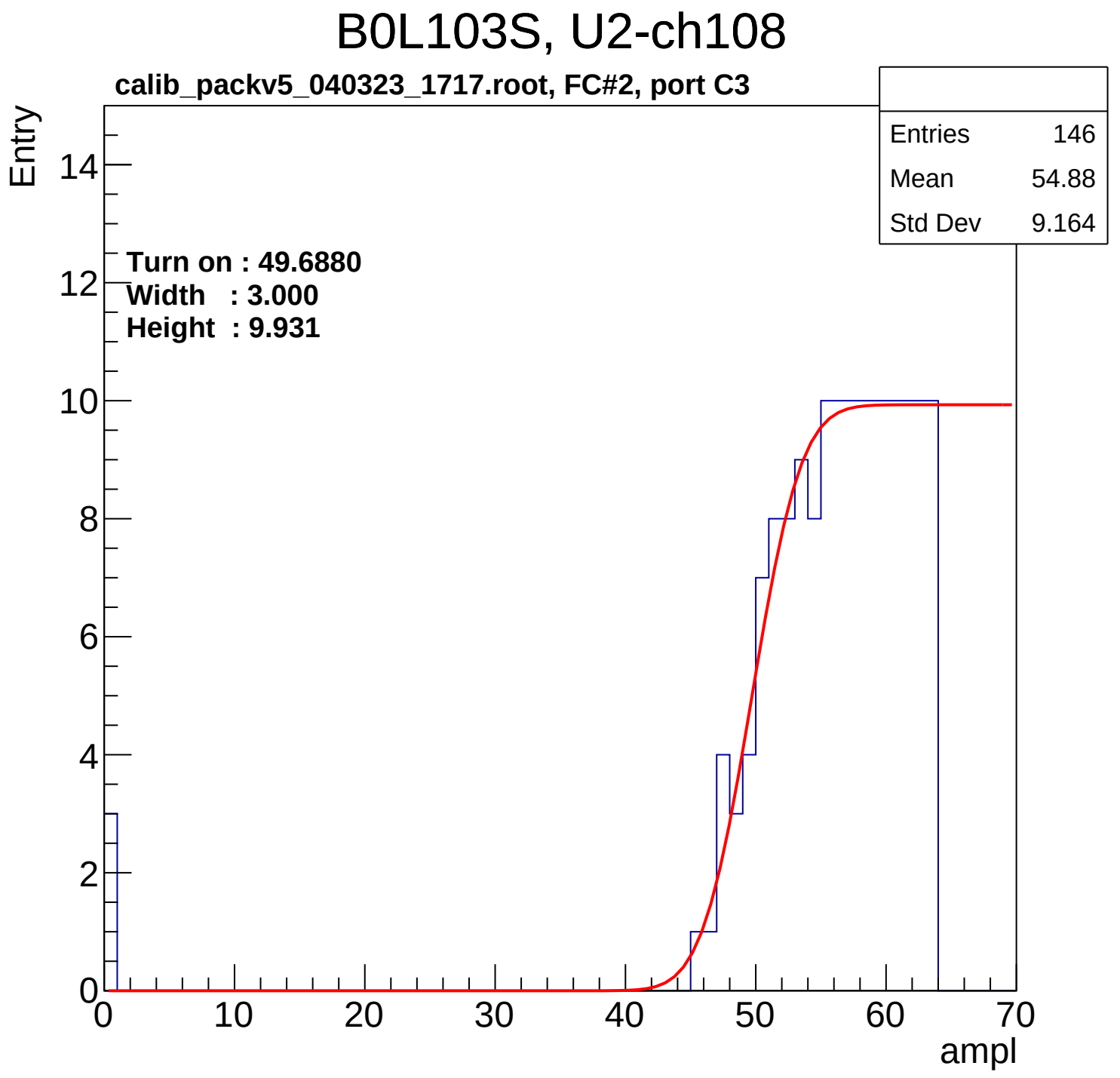
B0L103S, U2-ch108
calib_packv5_040323_1717.root, FC#2, port C3
Entries 146
Mean 54.88
Std Dev 9.164
Turn on : 49.6880
Width : 3.000
Height : 9.931
Entry
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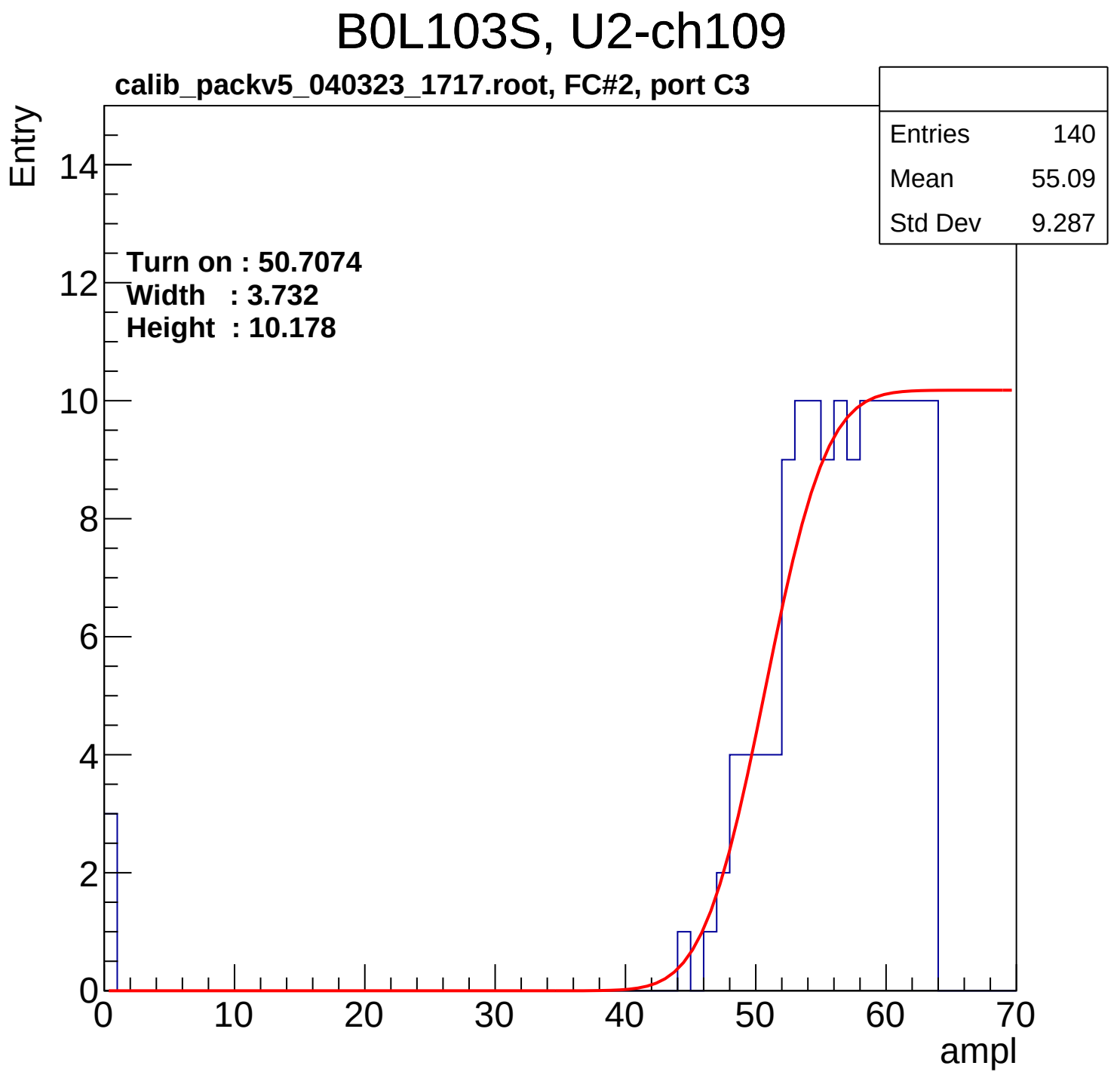
B0L103S, U2-ch109
calib_packv5_040323_1717.root, FC#2, port C3
Entries 140
Mean 55.09
Std Dev 9.287
Turn on : 50.7074
Width : 3.732
Height : 10.178
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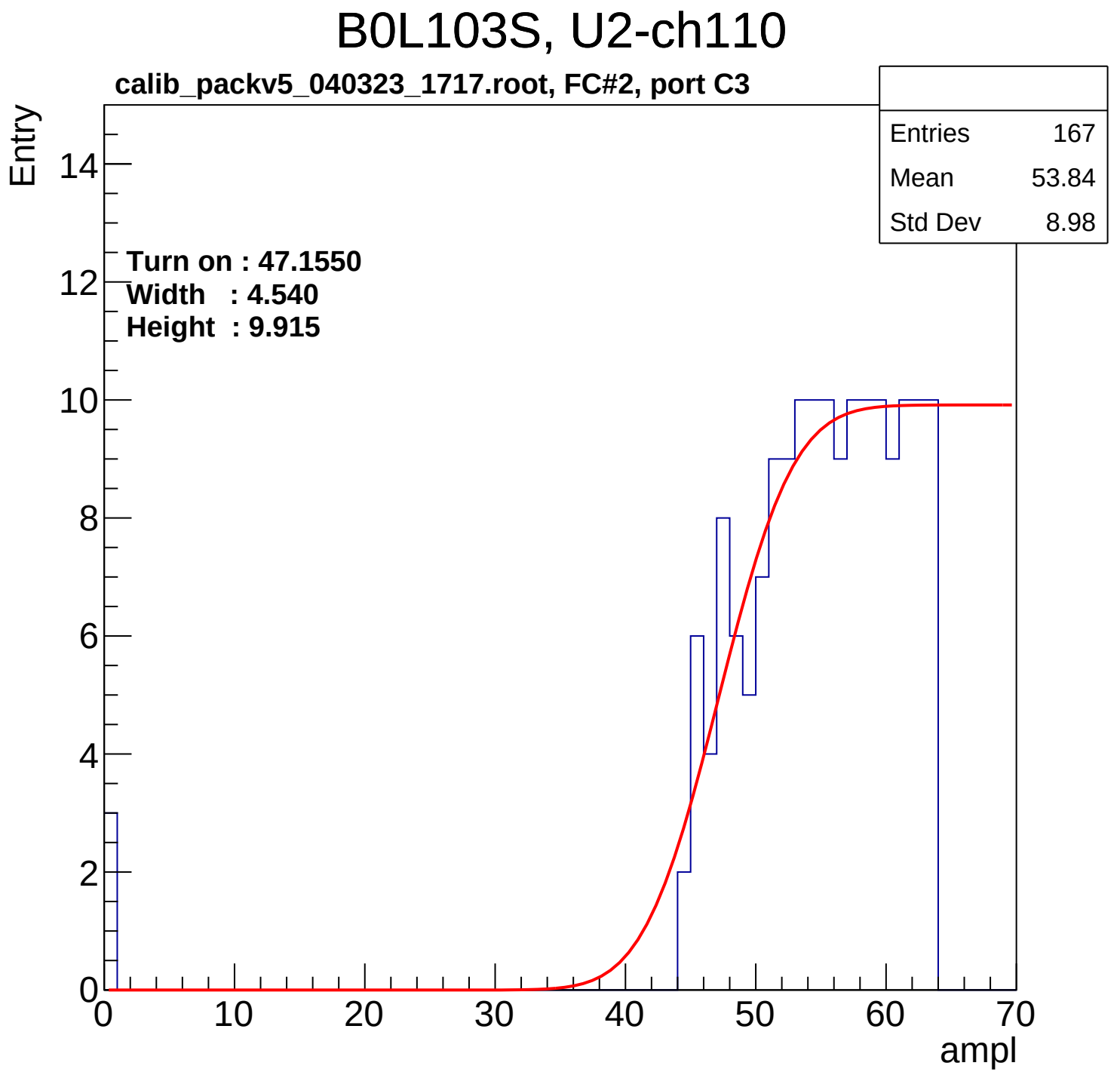
B0L103S, U2-ch110
calib_packv5_040323_1717.root, FC#2, port C3
Entries 167
Mean 53.84
Std Dev 8.98
Turn on : 47.1550
Width : 4.540
Height : 9.915
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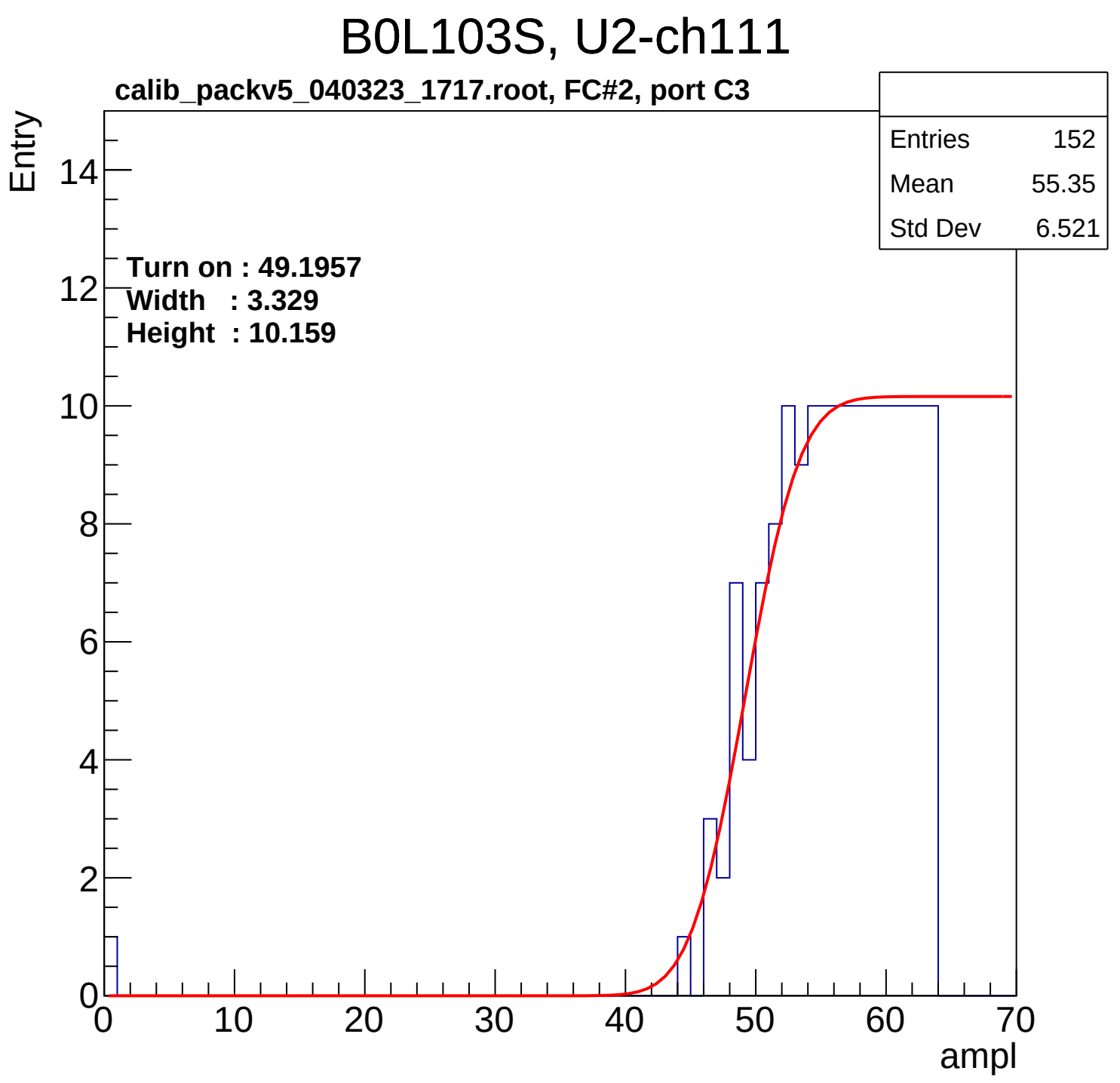
B0L103S, U2-ch111
calib_packv5_040323_1717.root, FC#2, port C3
Entries 152
Mean 55.35
Std Dev 6.521
Turn on : 49.1957
Width : 3.329
Height : 10.159
Entry
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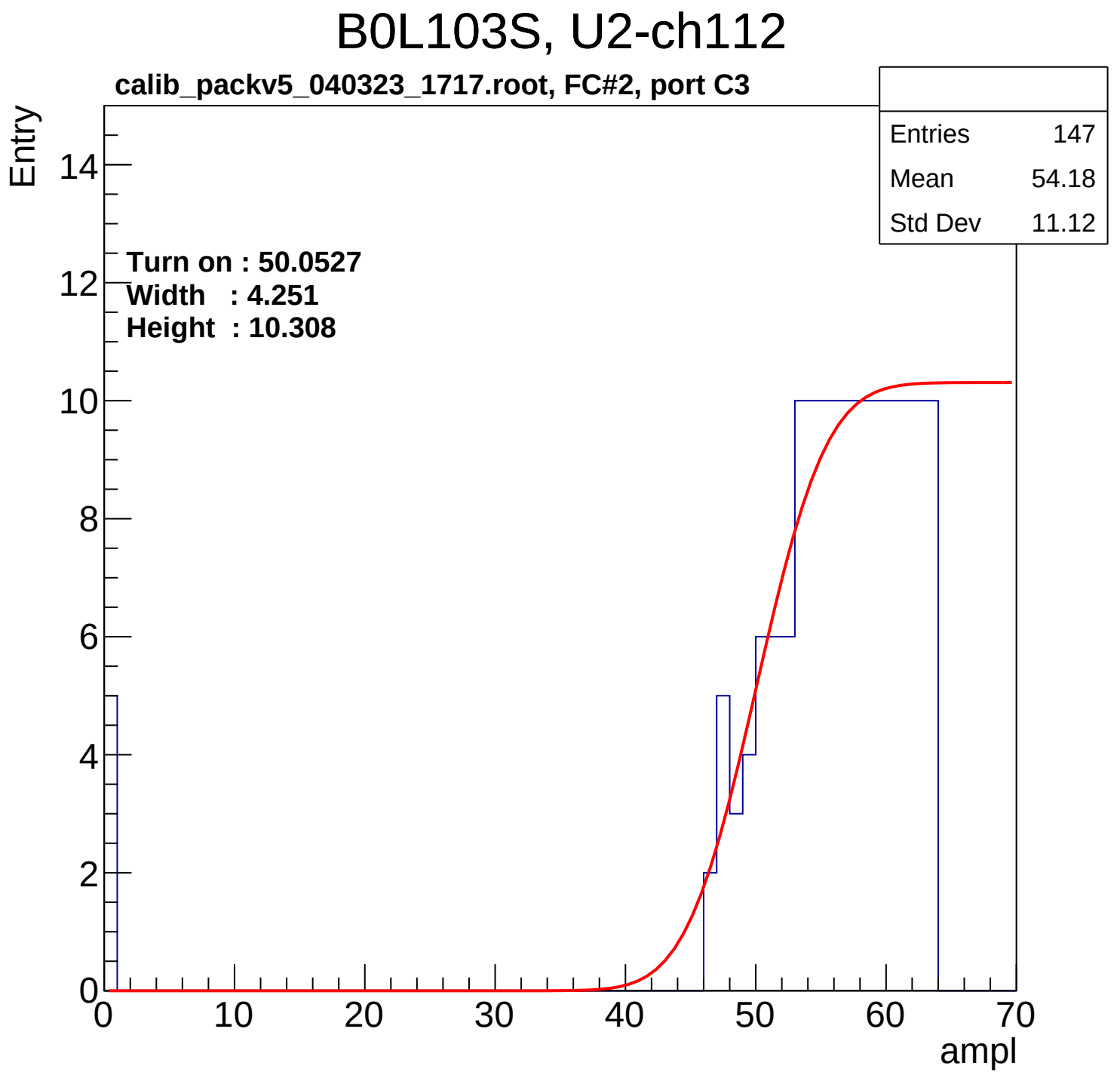
B0L103S, U2-ch112
calib_packv5_040323_1717.root, FC#2, port C3
Entries 147
Mean 54.18
Std Dev 11.12
Turn on : 50.0527
Width : 4.251
Height : 10.308
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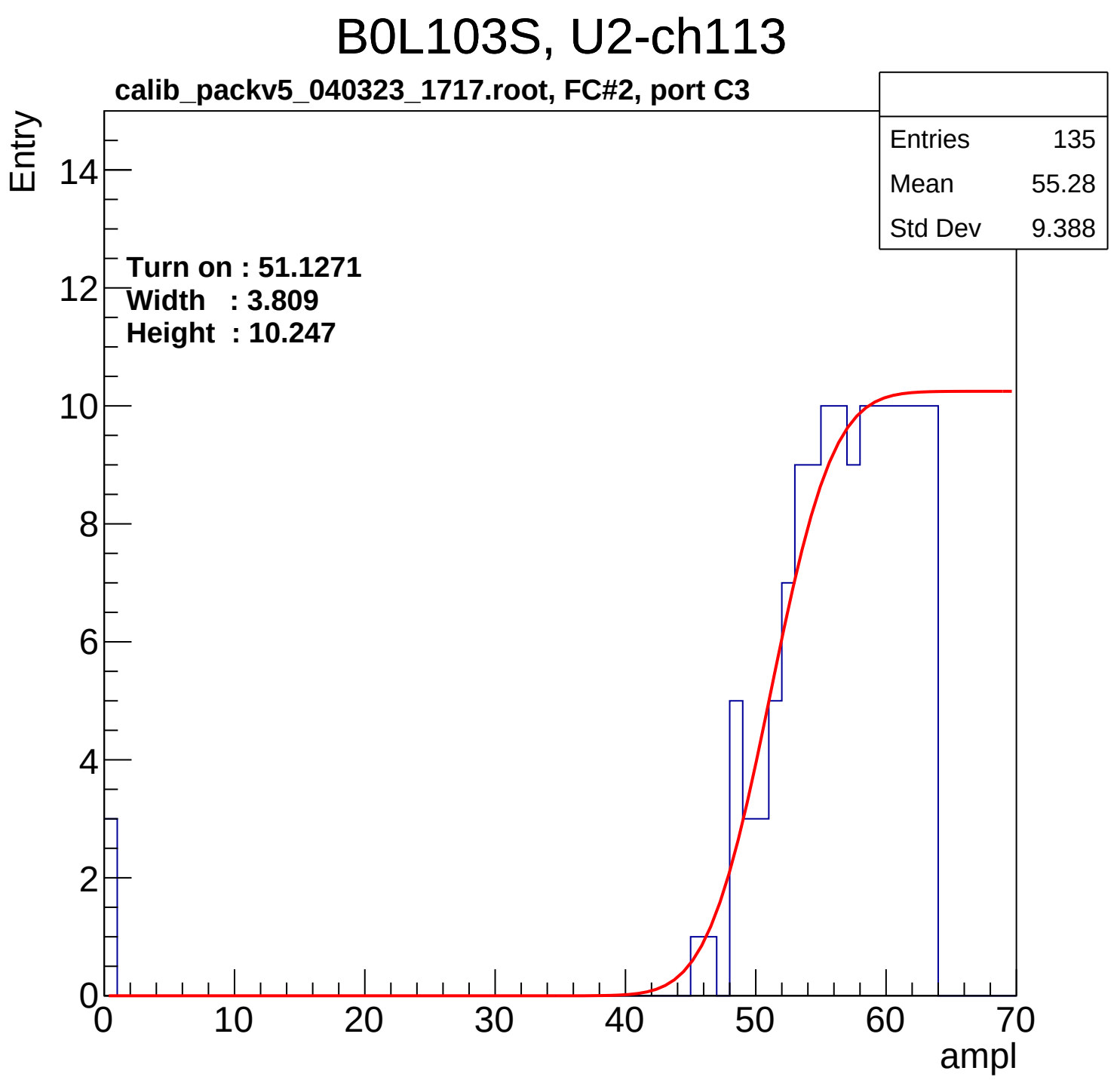
B0L103S, U2-ch113
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 55.28
Std Dev 9.388
Turn on : 51.1271
Width : 3.809
Height : 10.247
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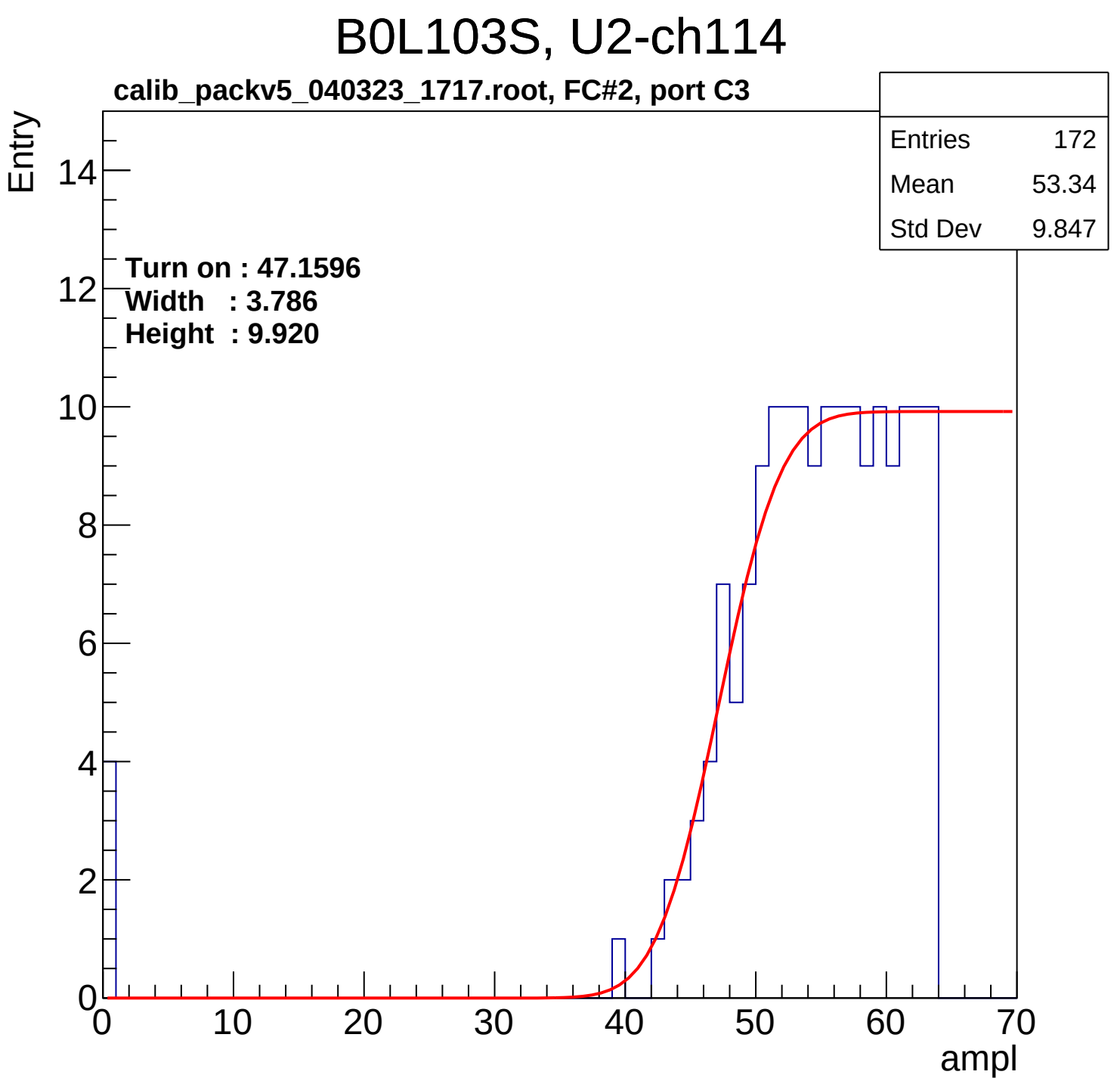
B0L103S, U2-ch114
calib_packv5_040323_1717.root, FC#2, port C3
Entries 172
Mean 53.34
Std Dev 9.847
Turn on : 47.1596
Width : 3.786
Height : 9.920
Entry
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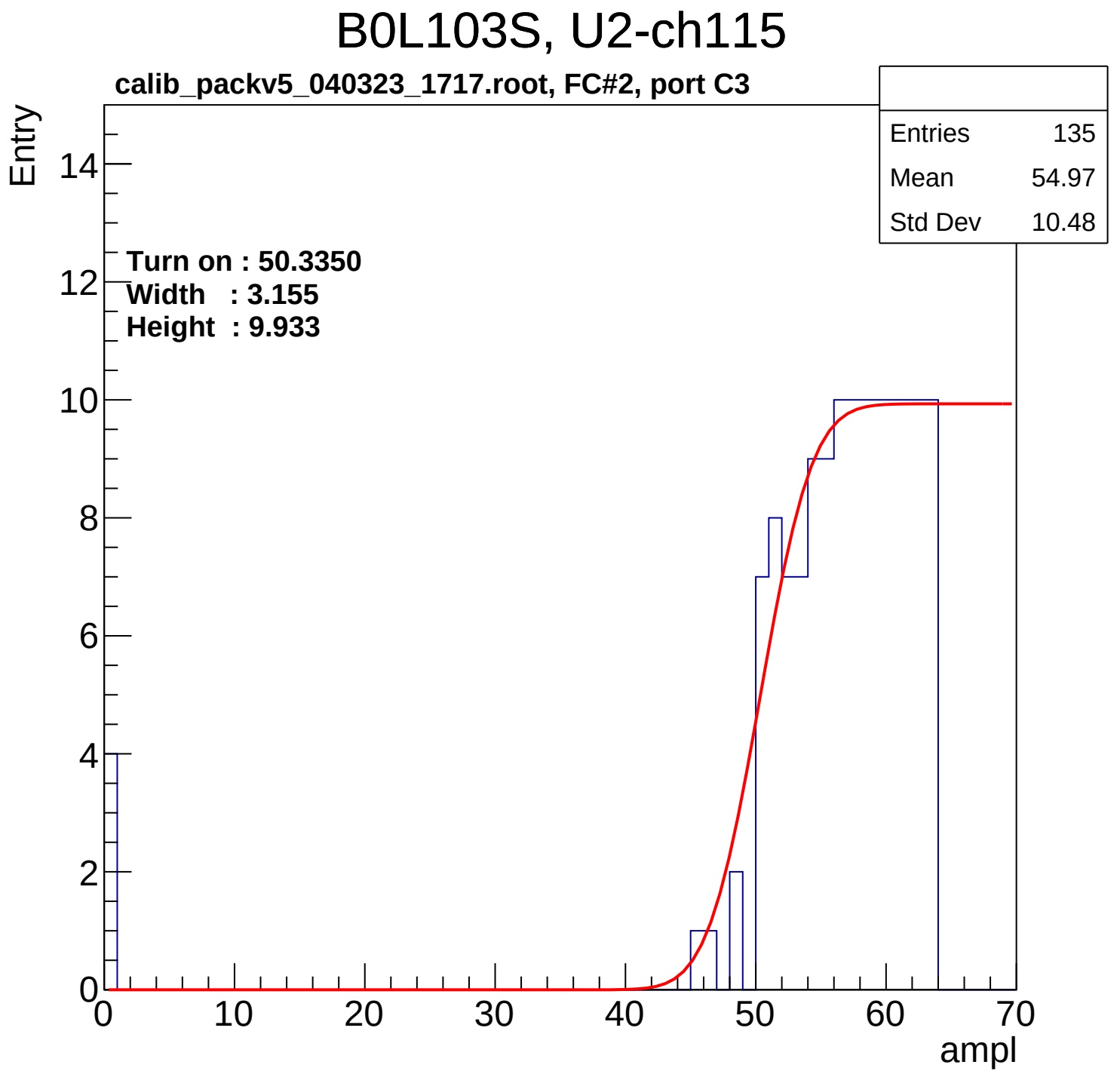
B0L103S, U2-ch115
calib_packv5_040323_1717.root, FC#2, port C3
Entries 135
Mean 54.97
Std Dev 10.48
Turn on : 50.3350
Width : 3.155
Height : 9.933
Entry
ampl
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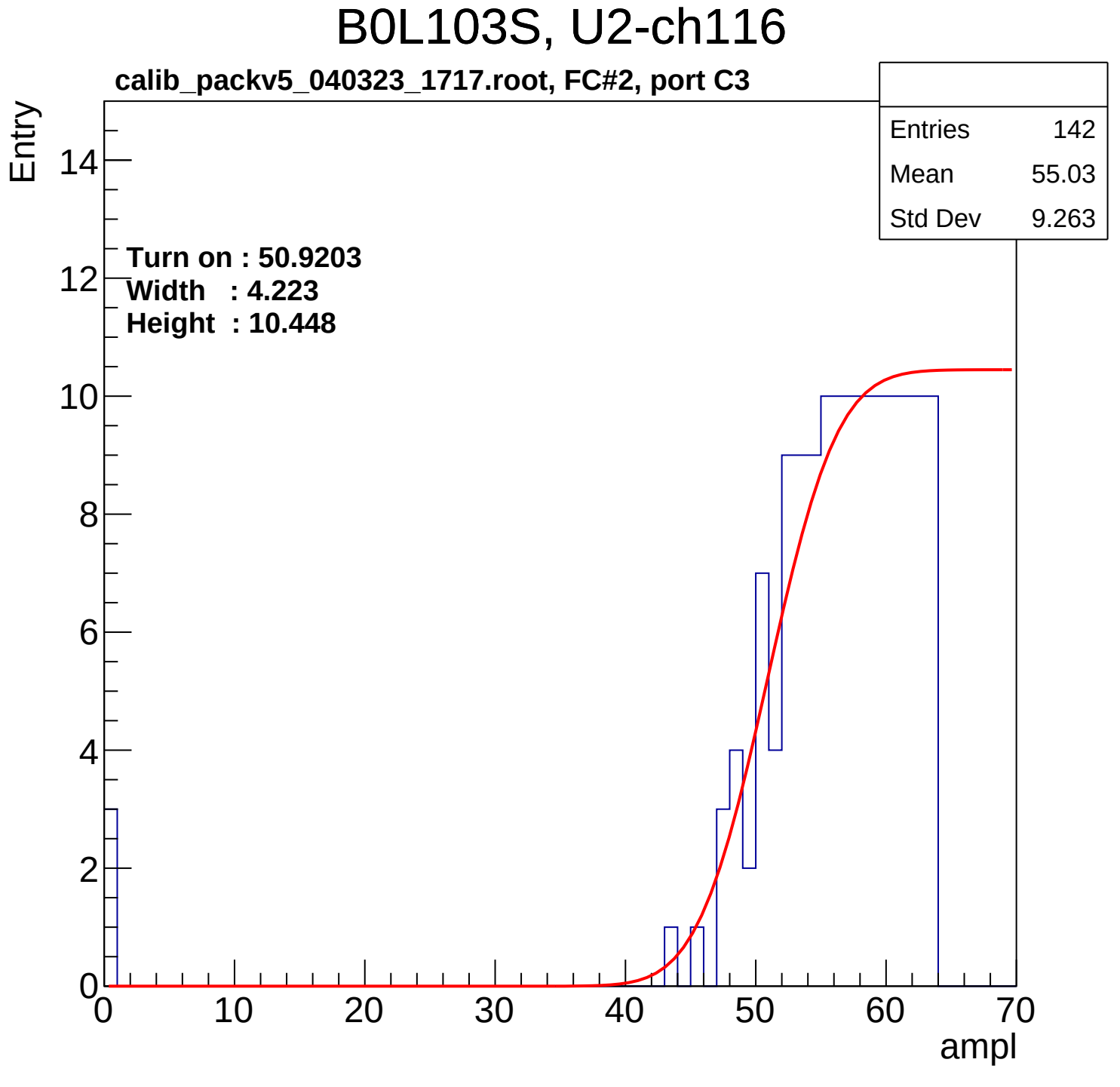
B0L103S, U2-ch116
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 55.03
Std Dev 9.263
Turn on : 50.9203
Width : 4.223
Height : 10.448
Entry
ampl
0
2
4
6
8
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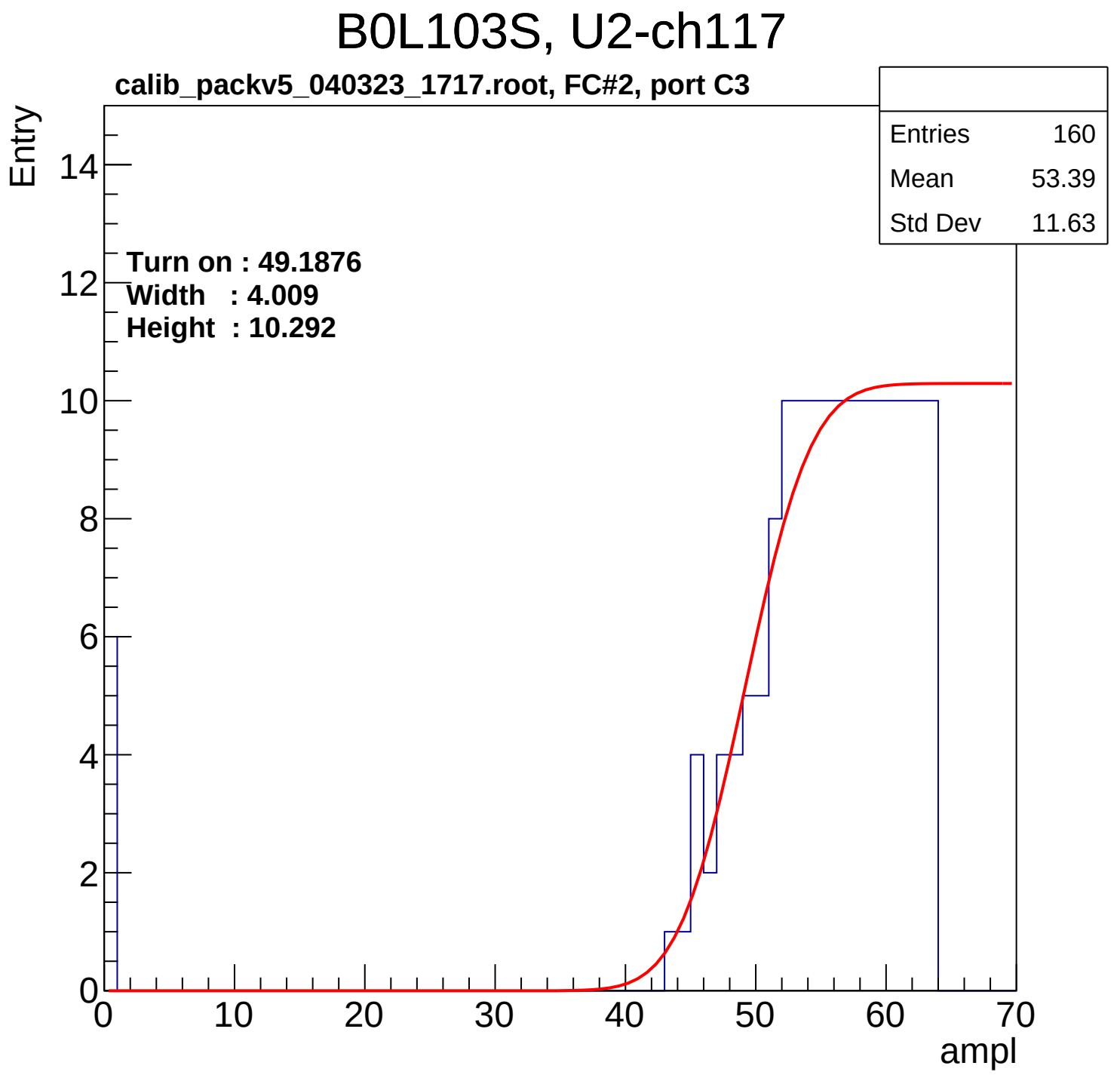
B0L103S, U2-ch117
calib_packv5_040323_1717.root, FC#2, port C3
Entries 160
Mean 53.39
Std Dev 11.63
Turn on : 49.1876
Width : 4.009
Height : 10.292
Entry
ampl
0
2
4
6
8
10
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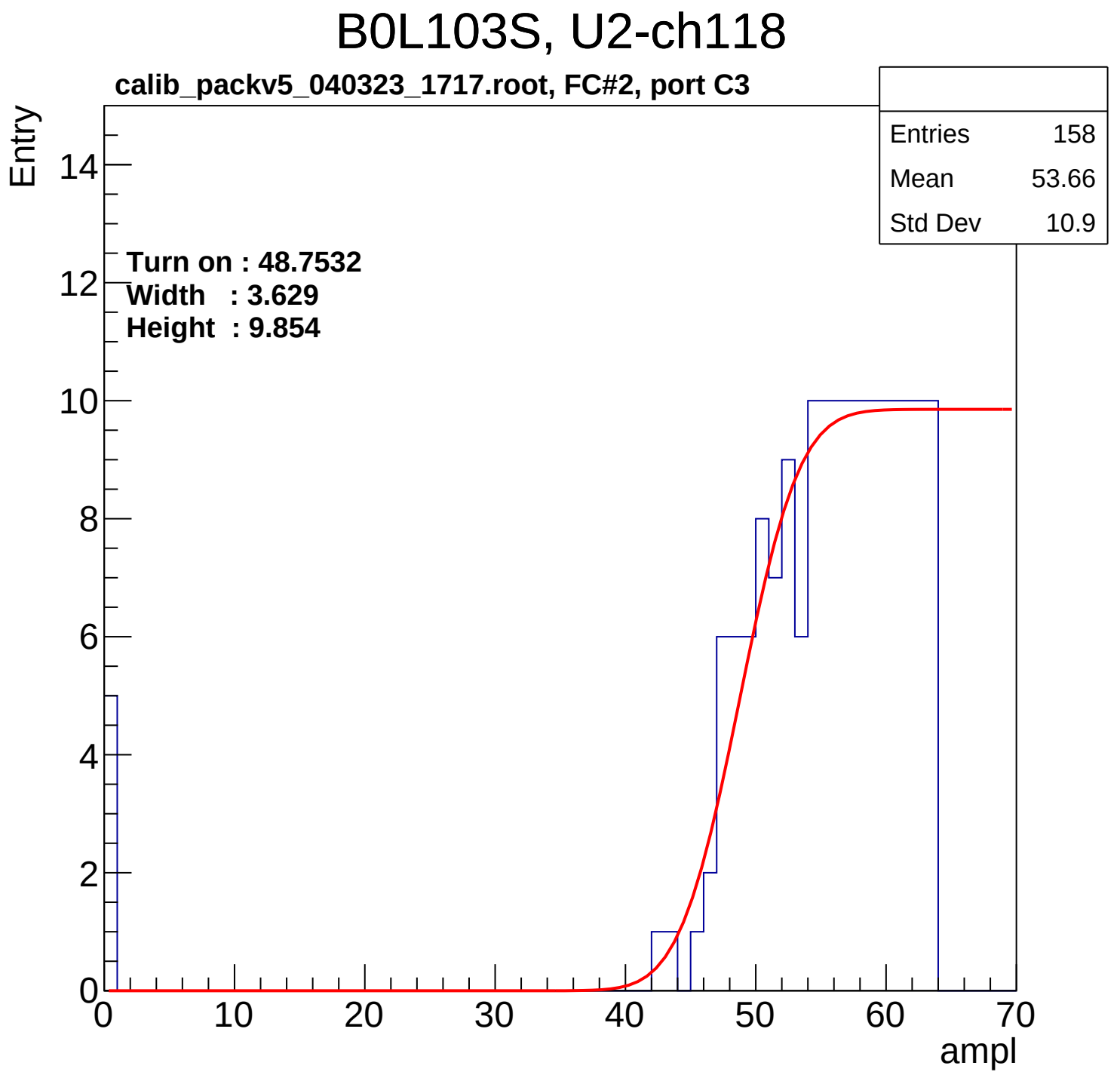
B0L103S, U2-ch118
calib_packv5_040323_1717.root, FC#2, port C3
Entries 158
Mean 53.66
Std Dev 10.9
Turn on : 48.7532
Width : 3.629
Height : 9.854
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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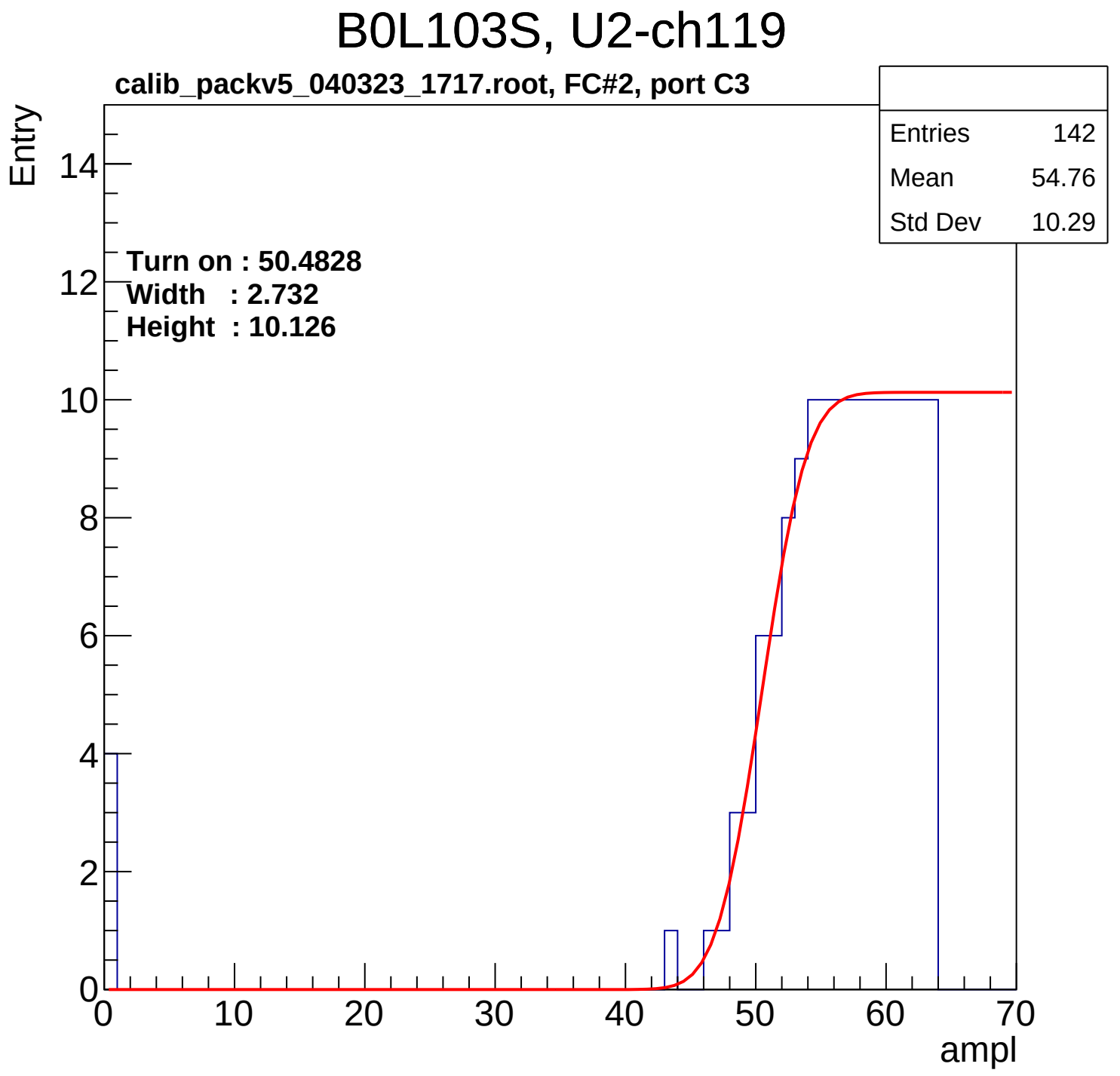
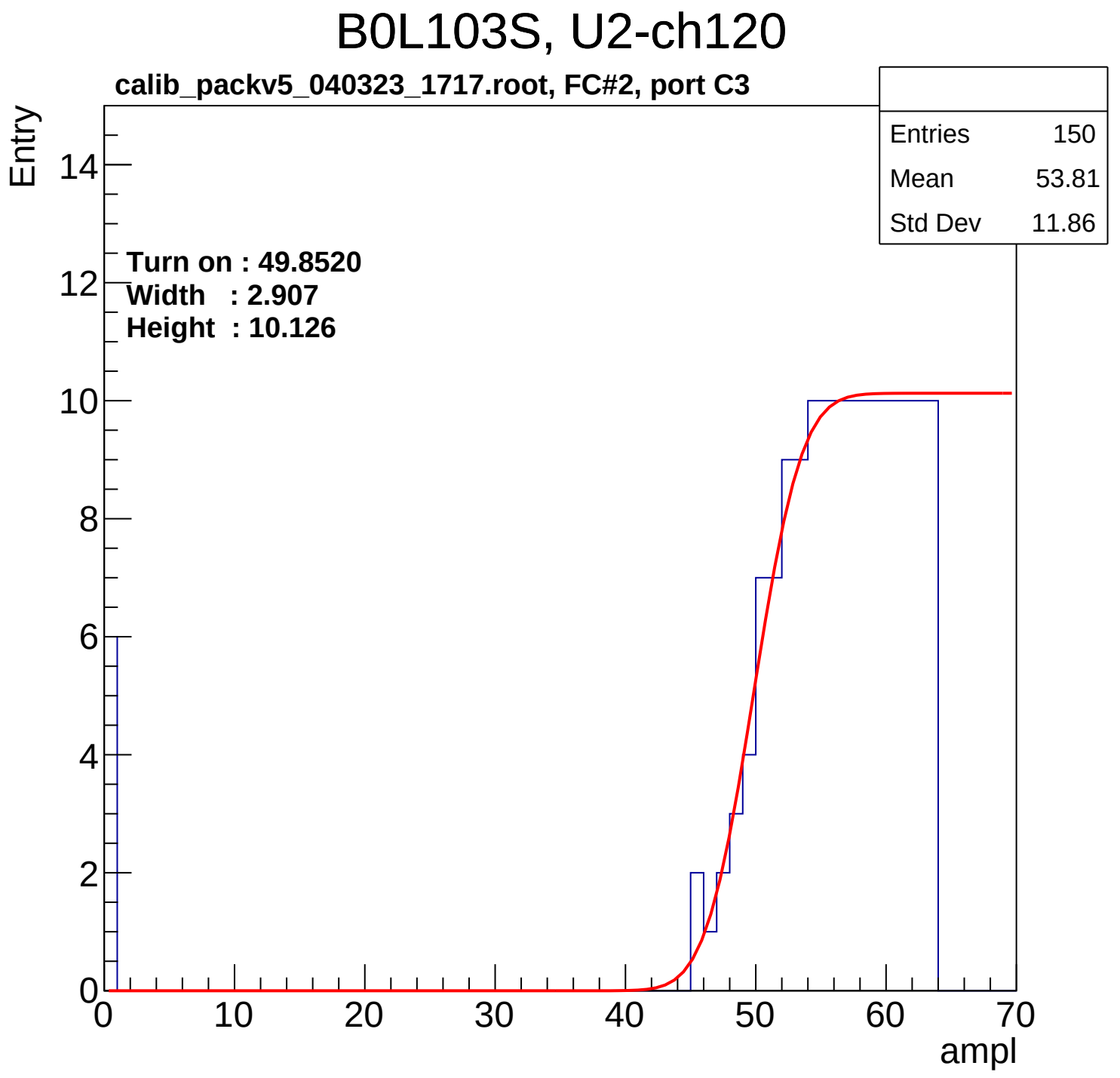
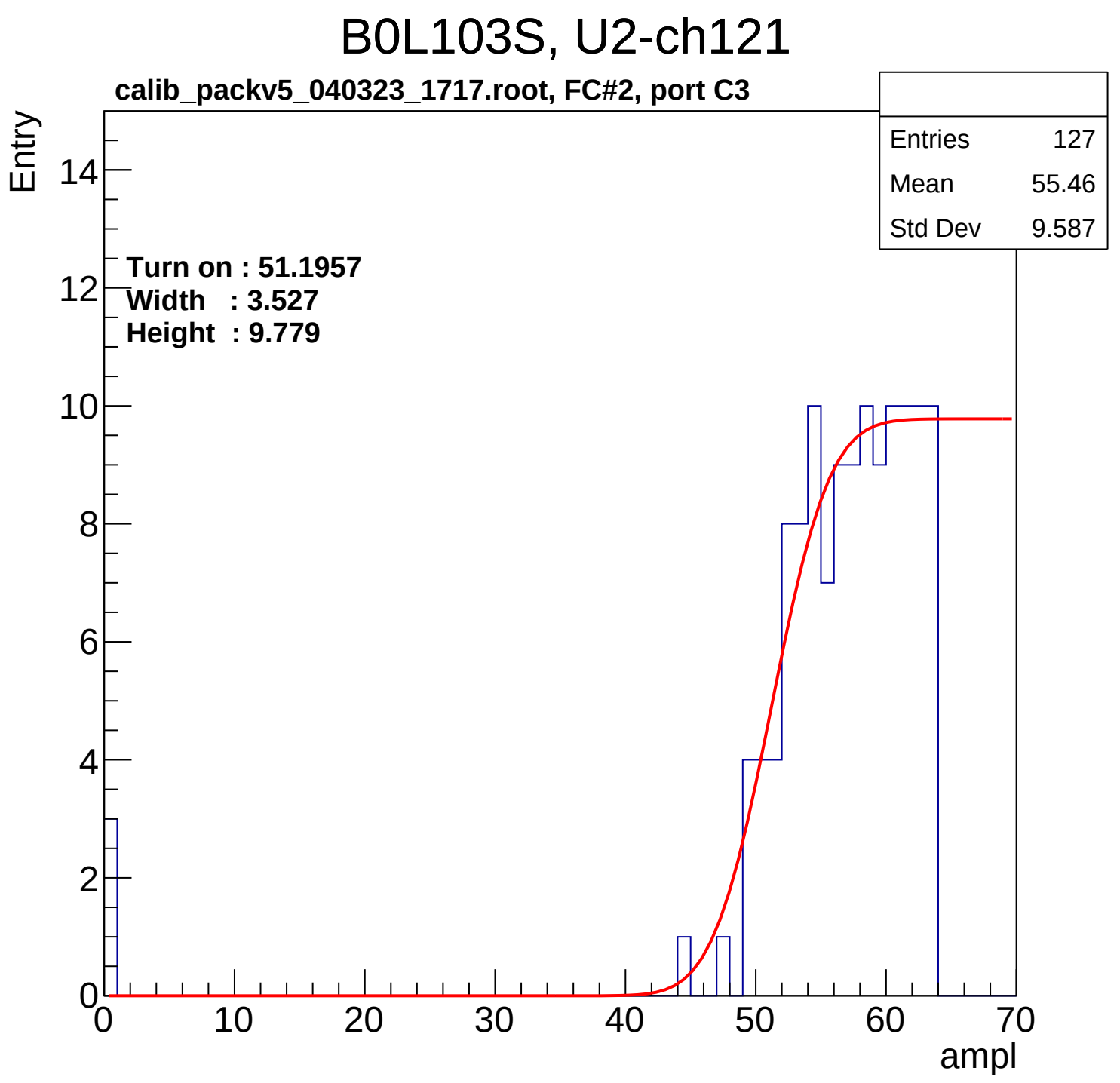
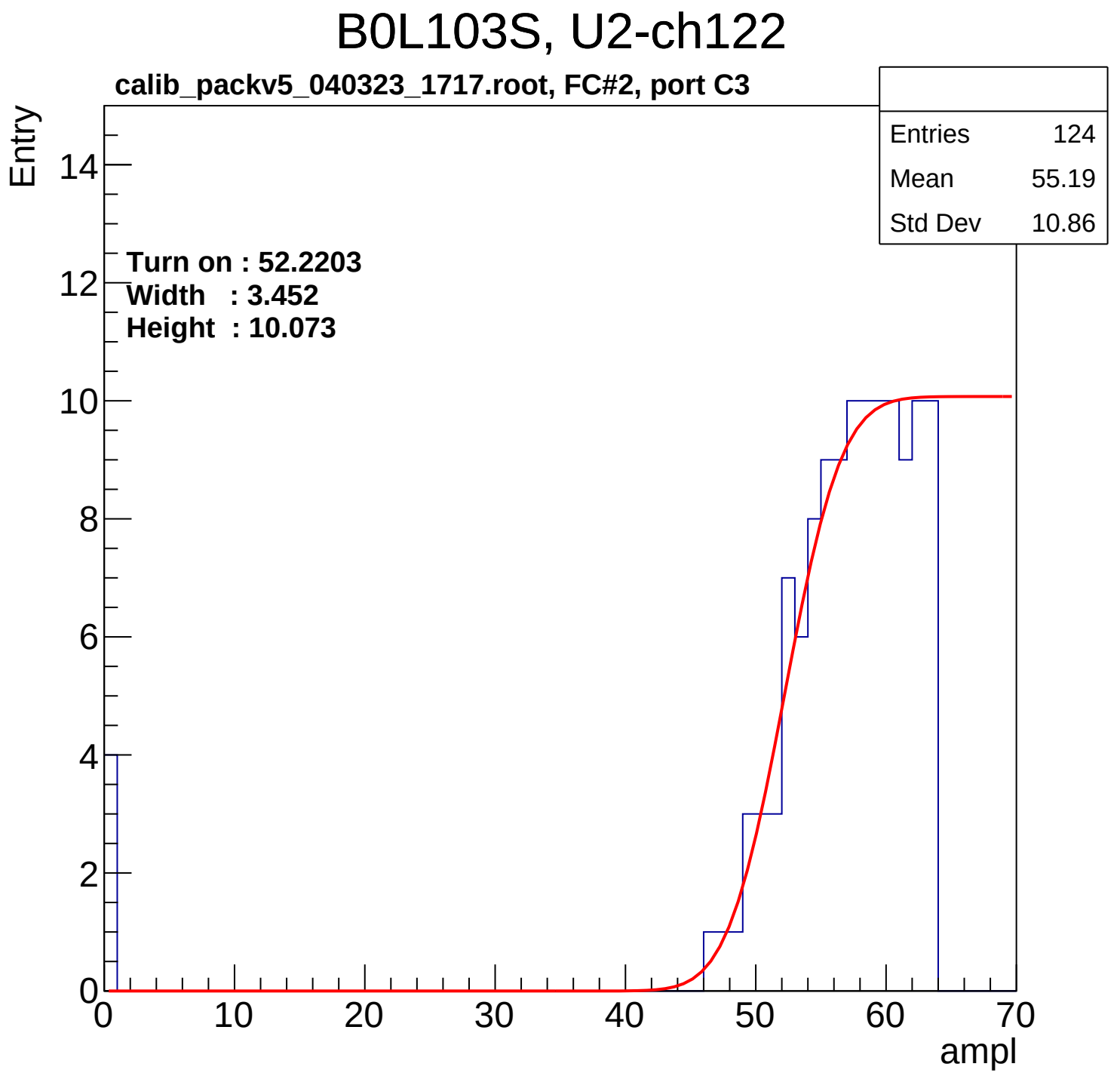

B0L103S, U2-ch119
calib_packv5_040323_1717.root, FC#2, port C3
Entries 142
Mean 54.76
Std Dev 10.29
Turn on : 50.4828
Width : 2.732
Height : 10.126
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U2-ch120
calib_packv5_040323_1717.root, FC#2, port C3
Entries 150
Mean 53.81
Std Dev 11.86
Turn on : 49.8520
Width : 2.907
Height : 10.126
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U2-ch121
calib_packv5_040323_1717.root, FC#2, port C3
Entries 127
Mean 55.46
Std Dev 9.587
Turn on : 51.1957
Width : 3.527
Height : 9.779
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U2-ch122
calib_packv5_040323_1717.root, FC#2, port C3
Entries 124
Mean 55.19
Std Dev 10.86
Turn on : 52.2203
Width : 3.452
Height : 10.073
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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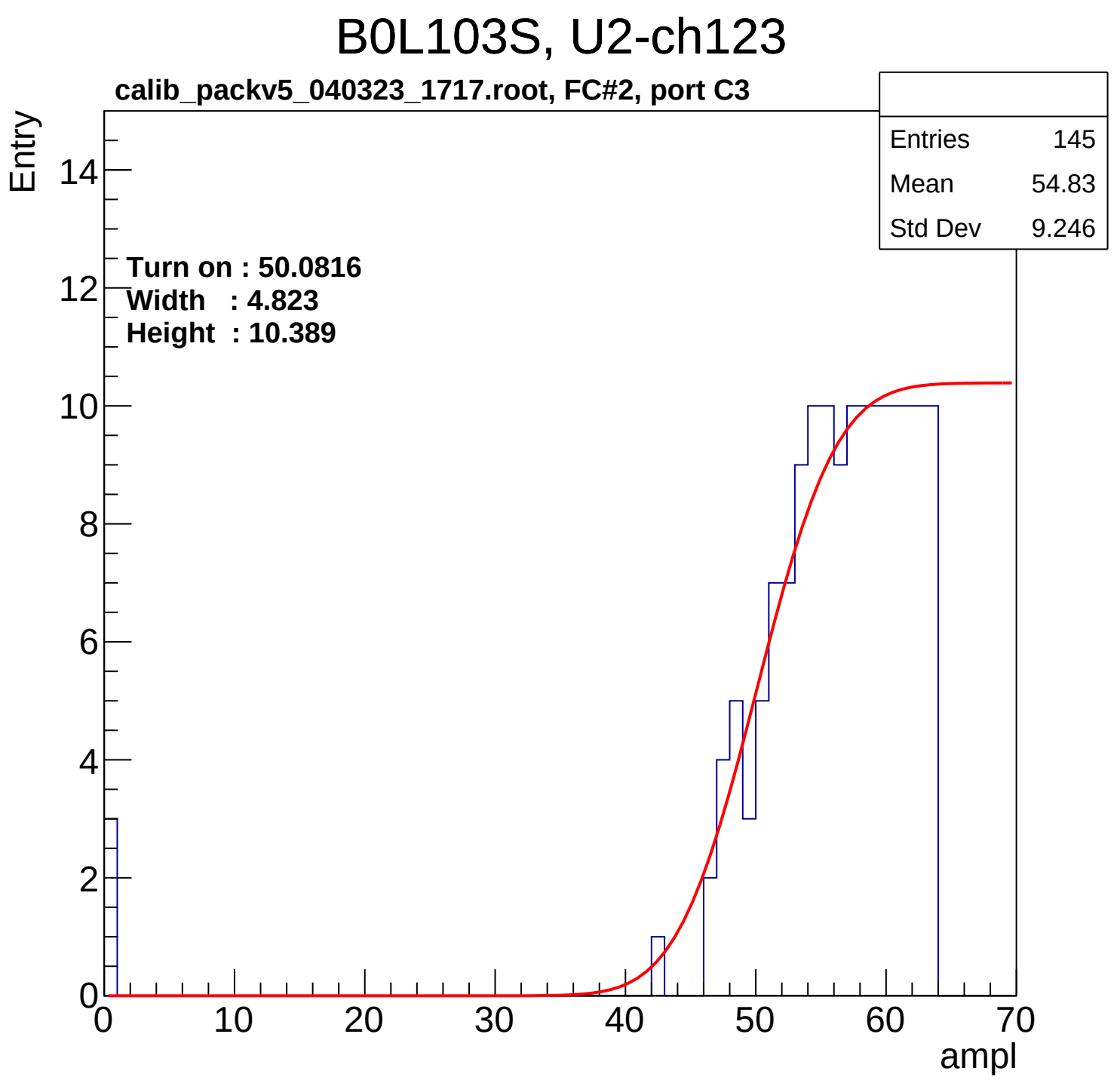
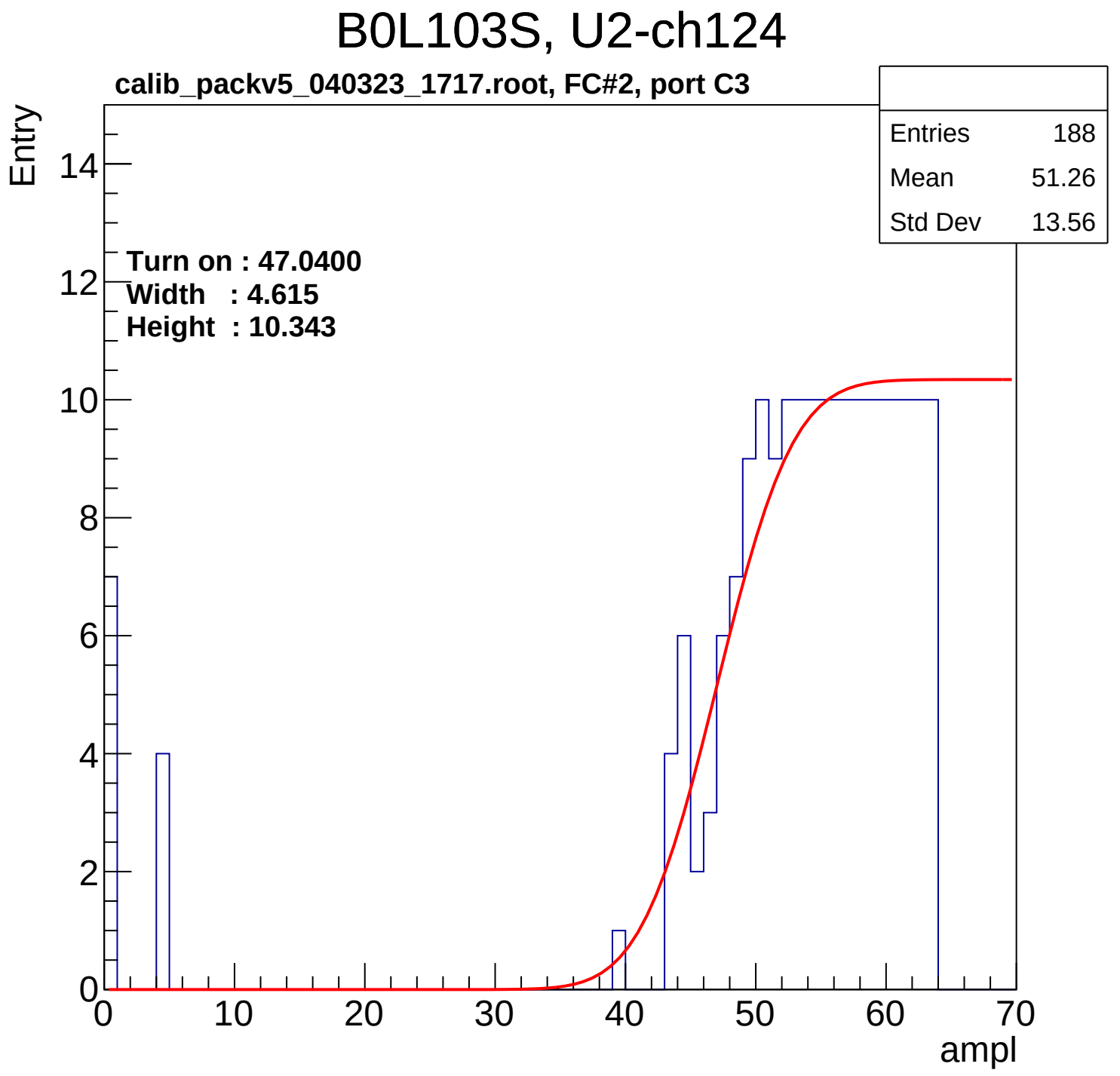

B0L103S, U2-ch123
calib_packv5_040323_1717.root, FC#2, port C3
Entries 145
Mean 54.83
Std Dev 9.246
Turn on : 50.0816
Width : 4.823
Height : 10.389
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U2-ch124
calib_packv5_040323_1717.root, FC#2, port C3
Entries 188
Mean 51.26
Std Dev 13.56
Turn on : 47.0400
Width : 4.615
Height : 10.343
Entry
ampl
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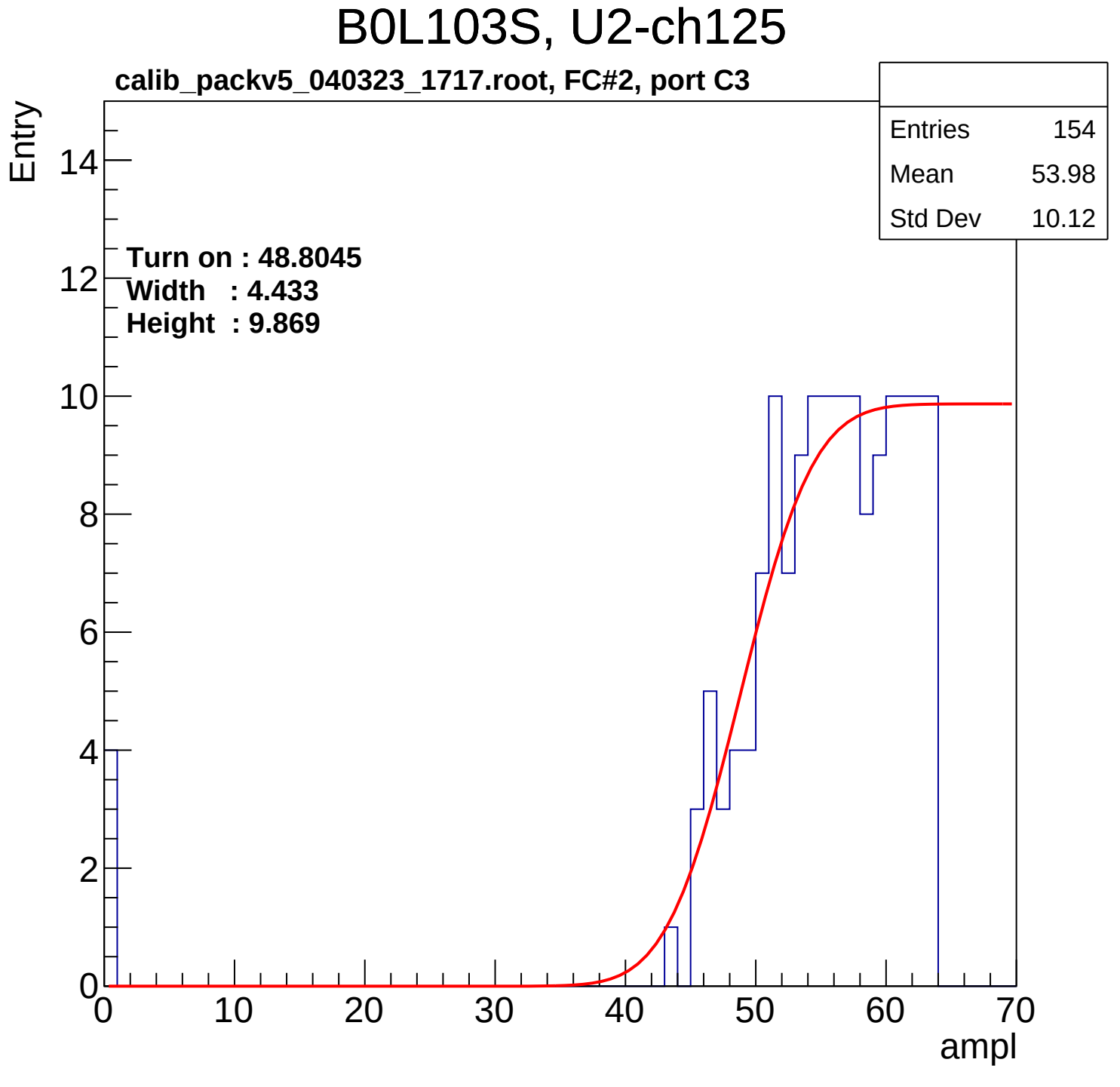
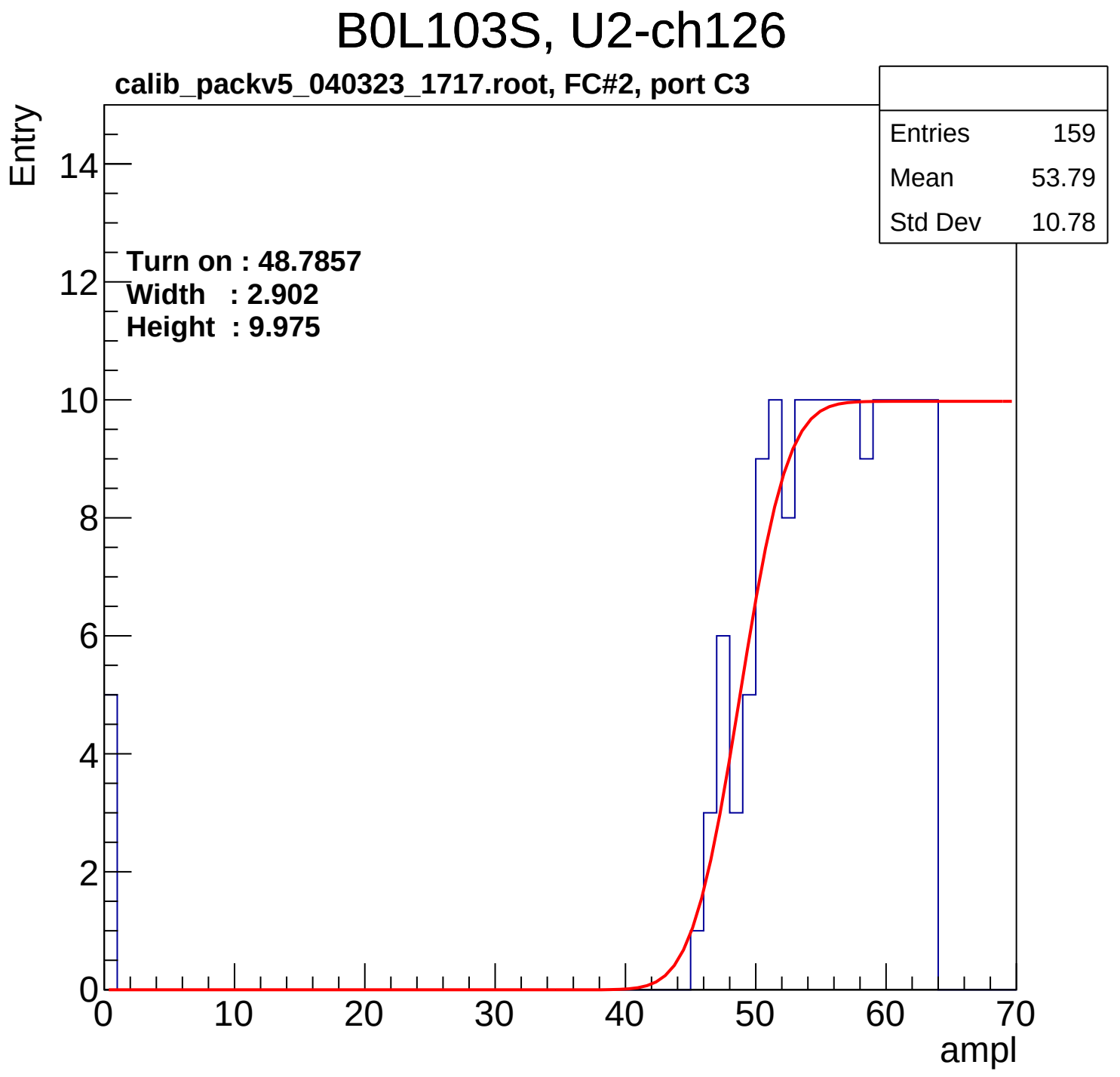
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U2-ch125
calib_packv5_040323_1717.root, FC#2, port C3
Entries 154
Mean 53.98
Std Dev 10.12
Turn on : 48.8045
Width : 4.433
Height : 9.869
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U2-ch126
calib_packv5_040323_1717.root, FC#2, port C3
Entries 159
Mean 53.79
Std Dev 10.78
Turn on : 48.7857
Width : 2.902
Height : 9.975
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
30
40
50
60
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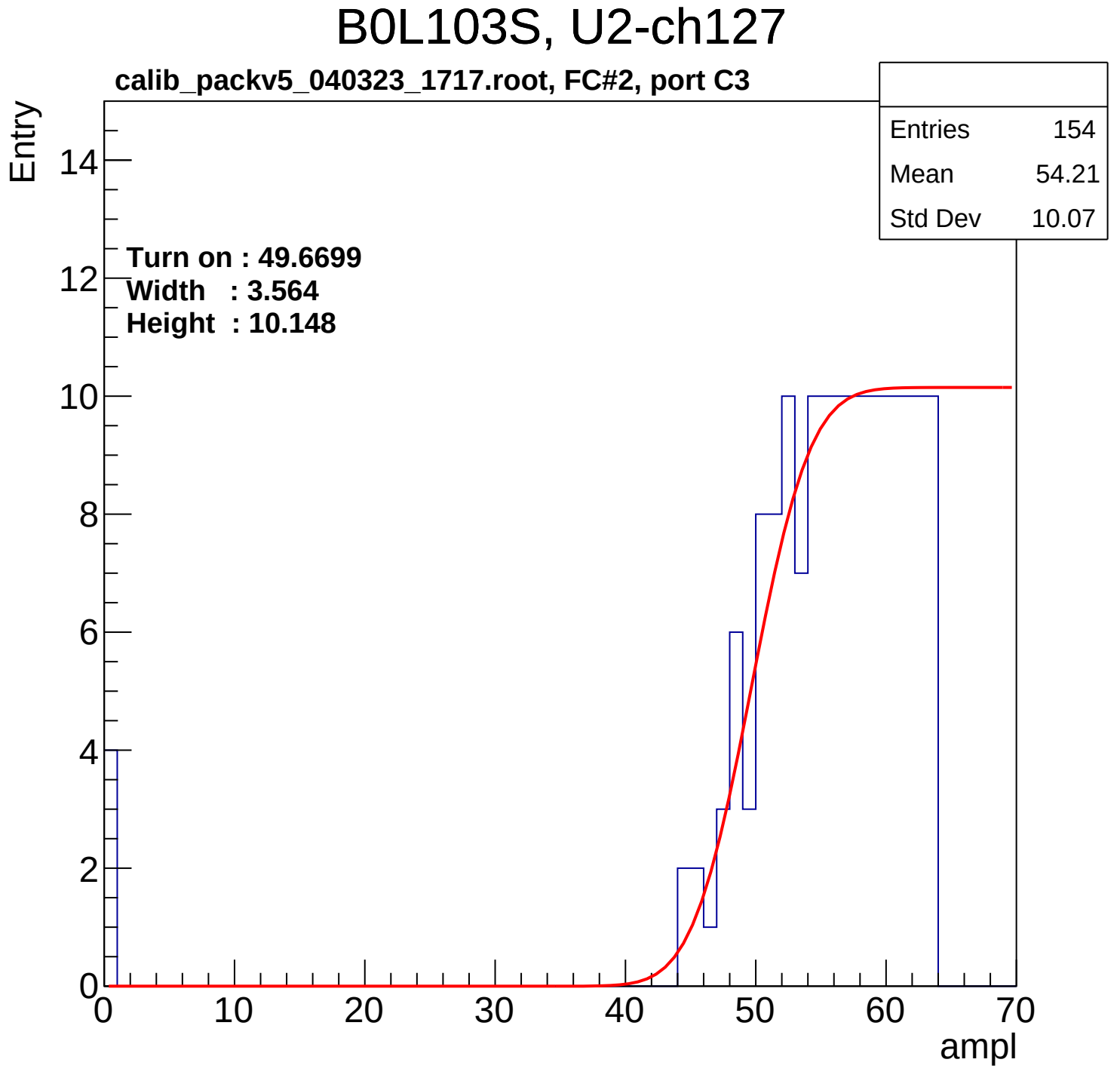
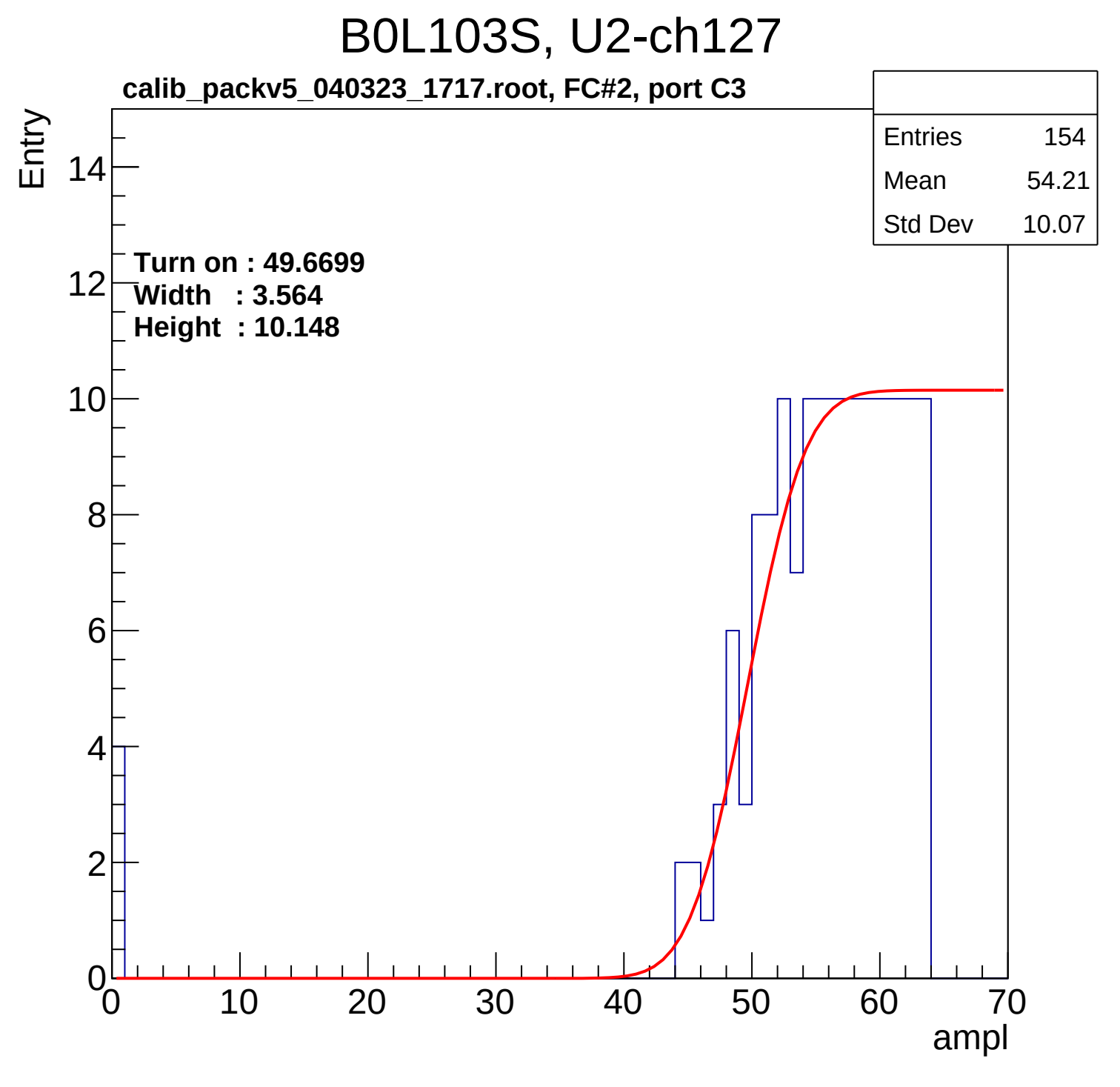

B0L103S, U2-ch127
calib_packv5_040323_1717.root, FC#2, port C3
Entries 154
Mean 54.21
Std Dev 10.07
Turn on : 49.6699
Width : 3.564
Height : 10.148
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L103S, U2-ch127
calib_packv5_040323_1717.root, FC#2, port C3
Entries 154
Mean 54.21
Std Dev 10.07
Turn on : 49.6699
Width : 3.564
Height : 10.148
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70