

B1L103S, U7-ch0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	467
Mean	37.84
Std Dev	17.69

Turn on : 23.0530

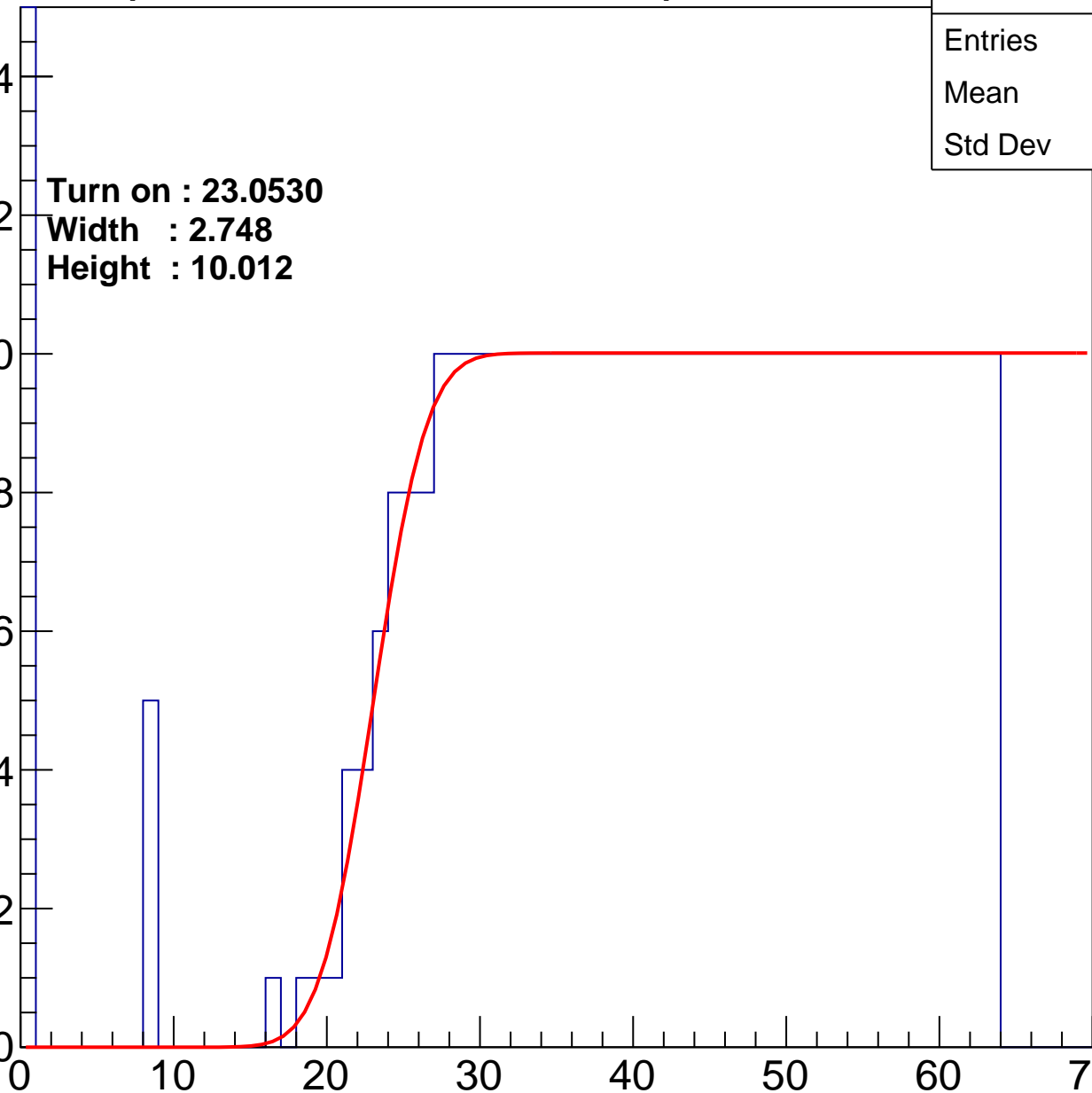
Width : 2.748

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	415
Mean	40.18
Std Dev	17.1

Turn on : 26.8358

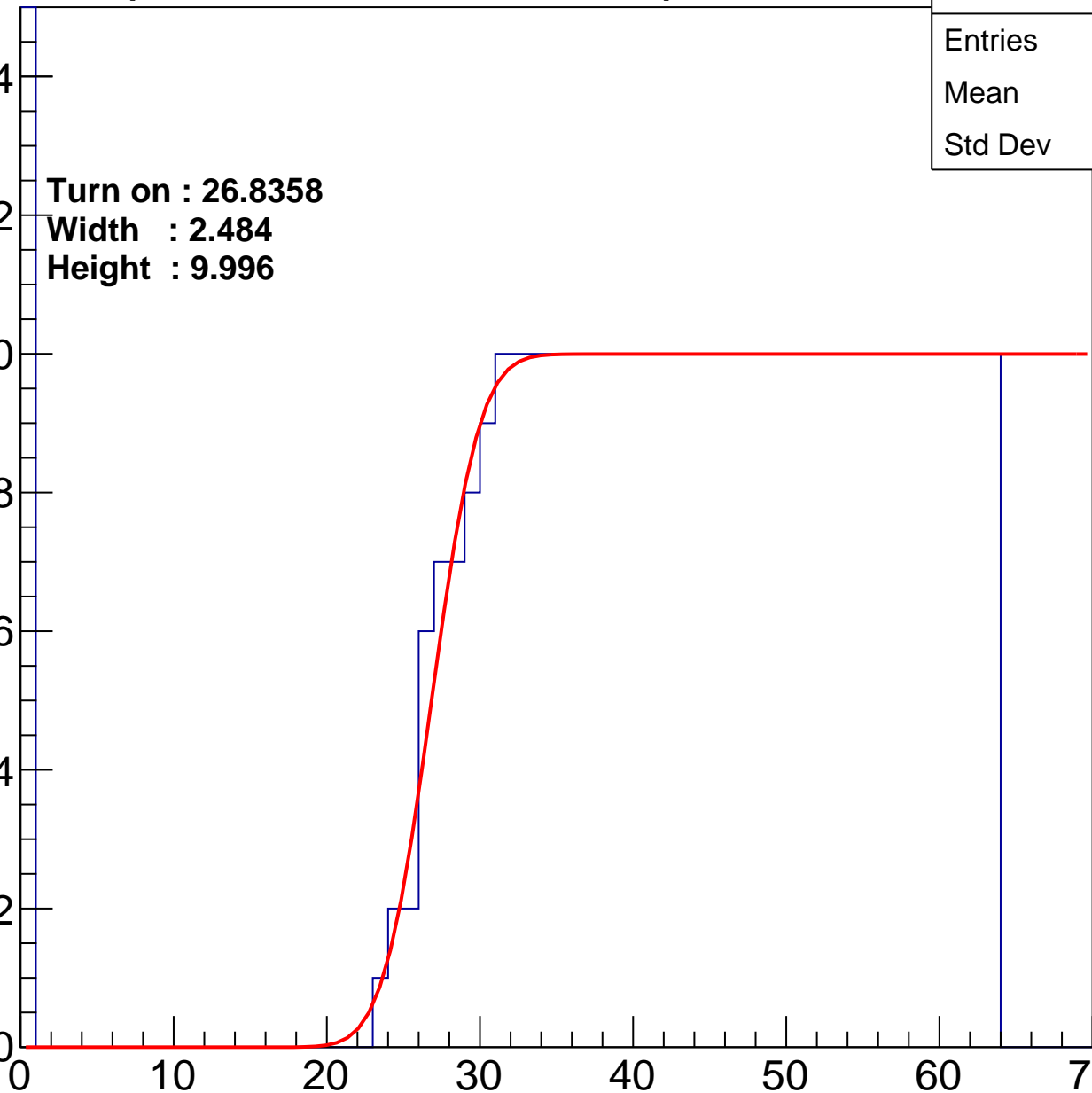
Width : 2.484

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	415
Mean	40.61
Std Dev	16.39

Turn on : 26.1332

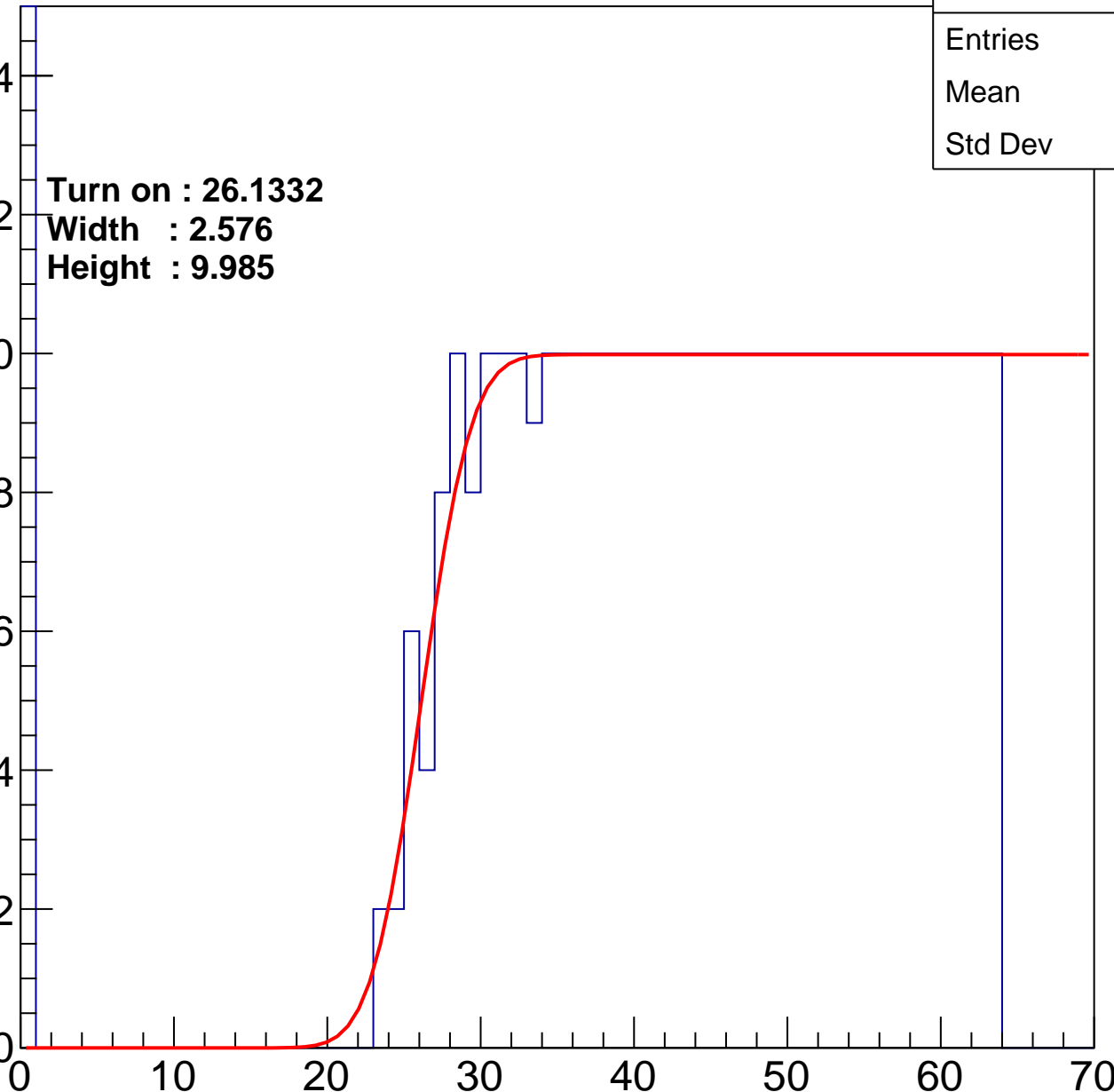
Width : 2.576

Height : 9.985

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	396
Mean	40.9
Std Dev	17.06

Turn on : 28.6673

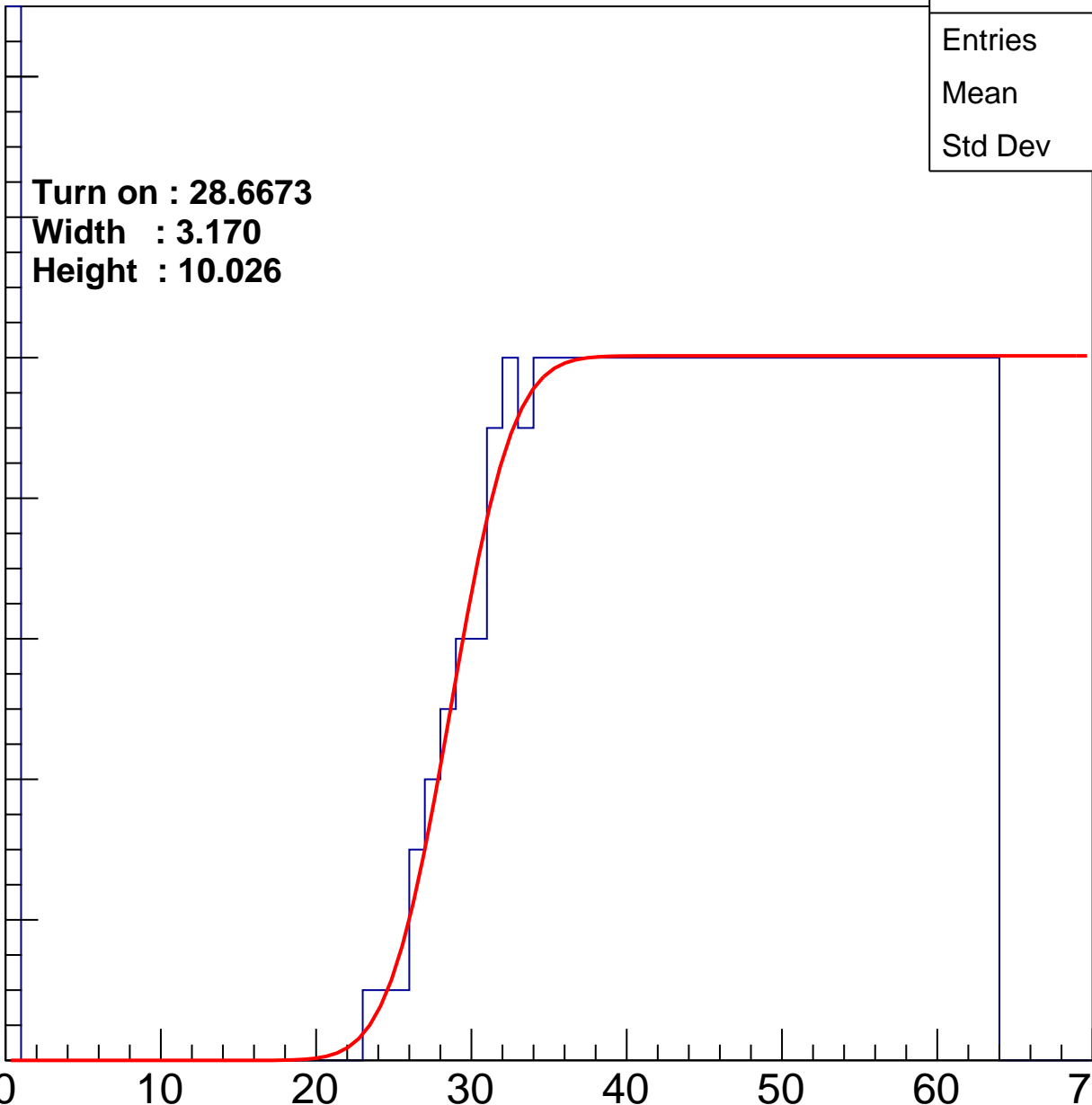
Width : 3.170

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	39.03
Std Dev	17.54

Turn on : 25.2522

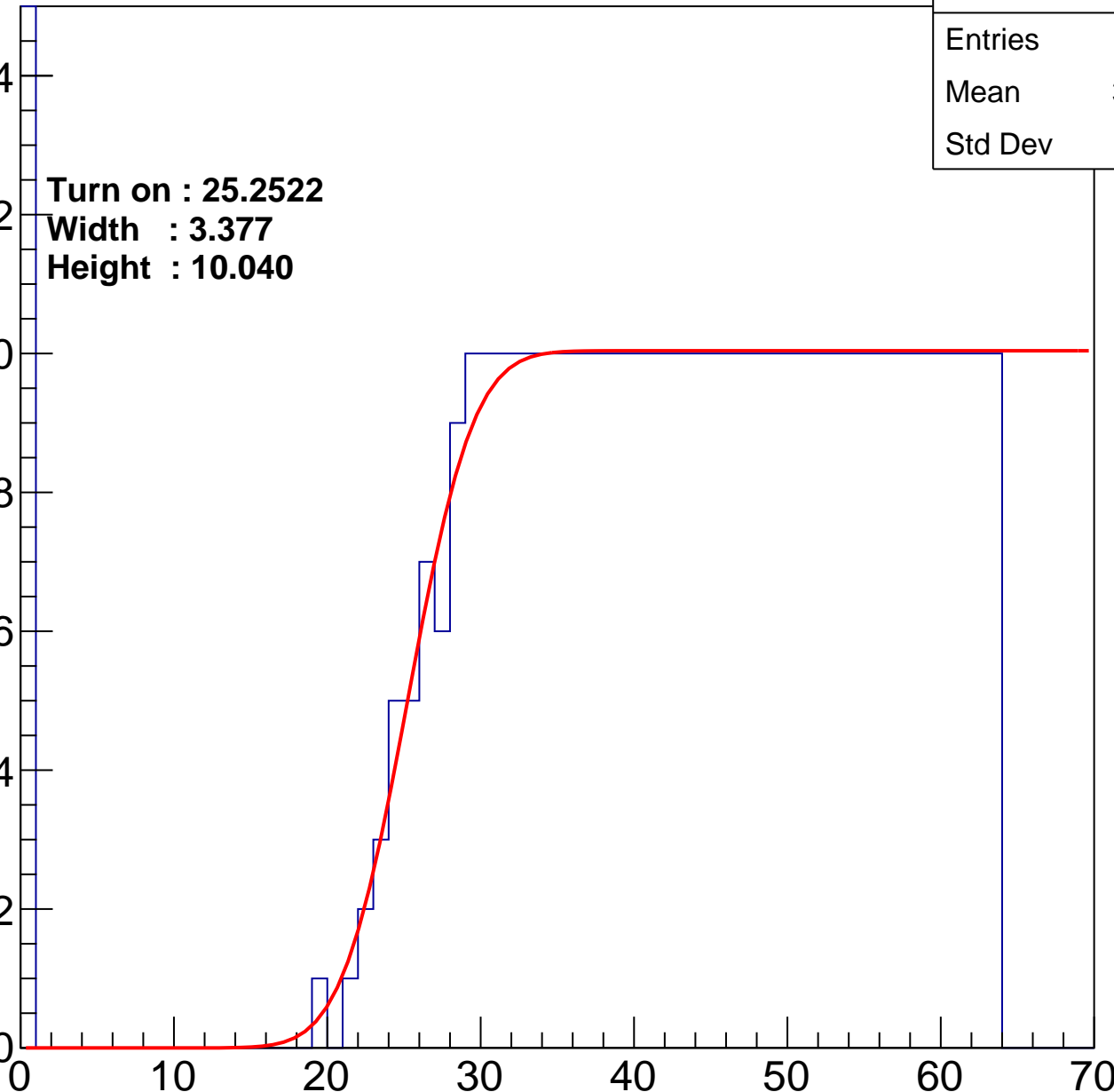
Width : 3.377

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch5

calib_packv5_041523_1651.root, FC#0, port C2

Entries	405
Mean	40.65
Std Dev	16.91

Turn on : 27.8137

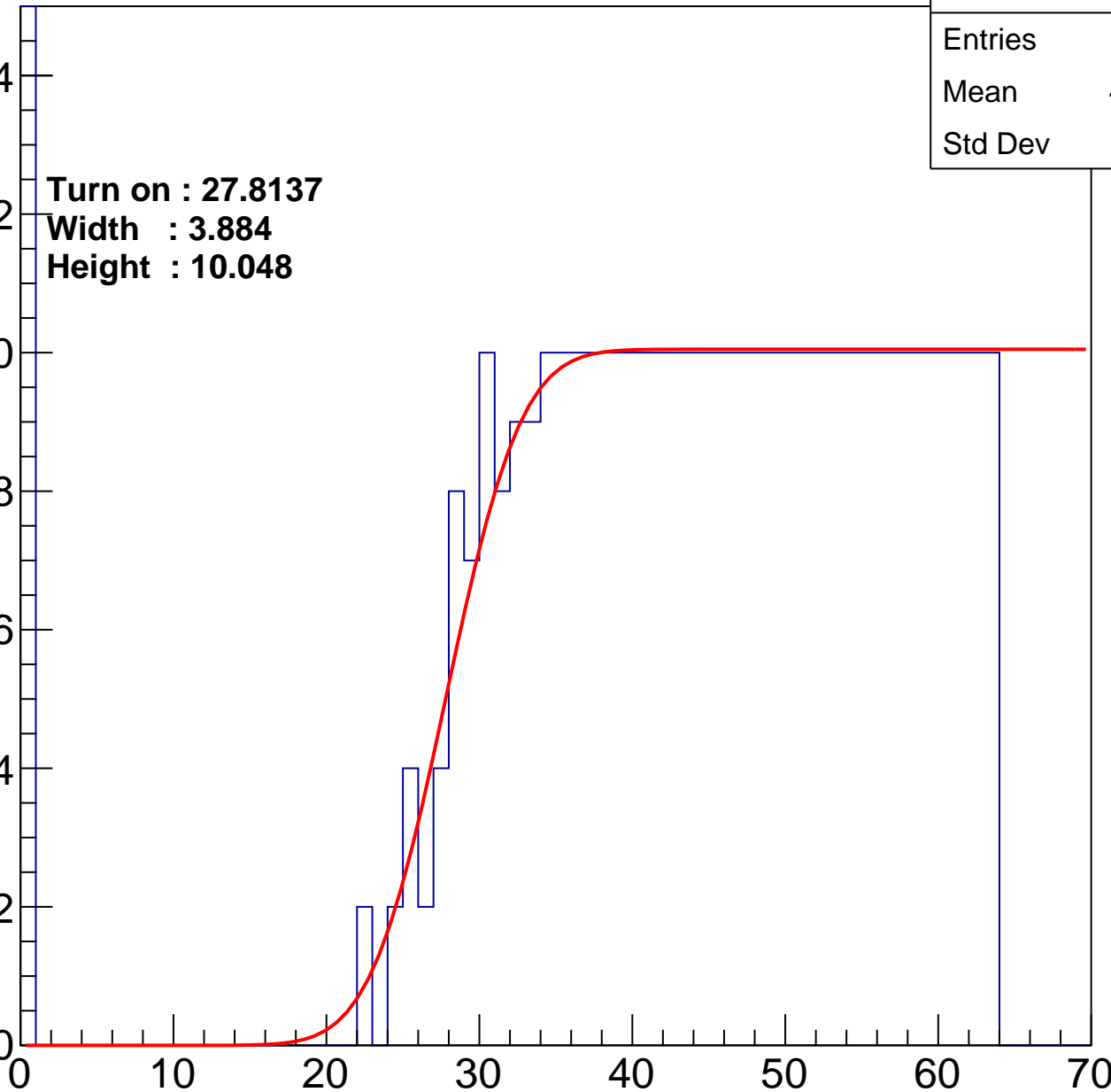
Width : 3.884

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch6

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	40.48
Std Dev	16.29

Turn on : 25.2775

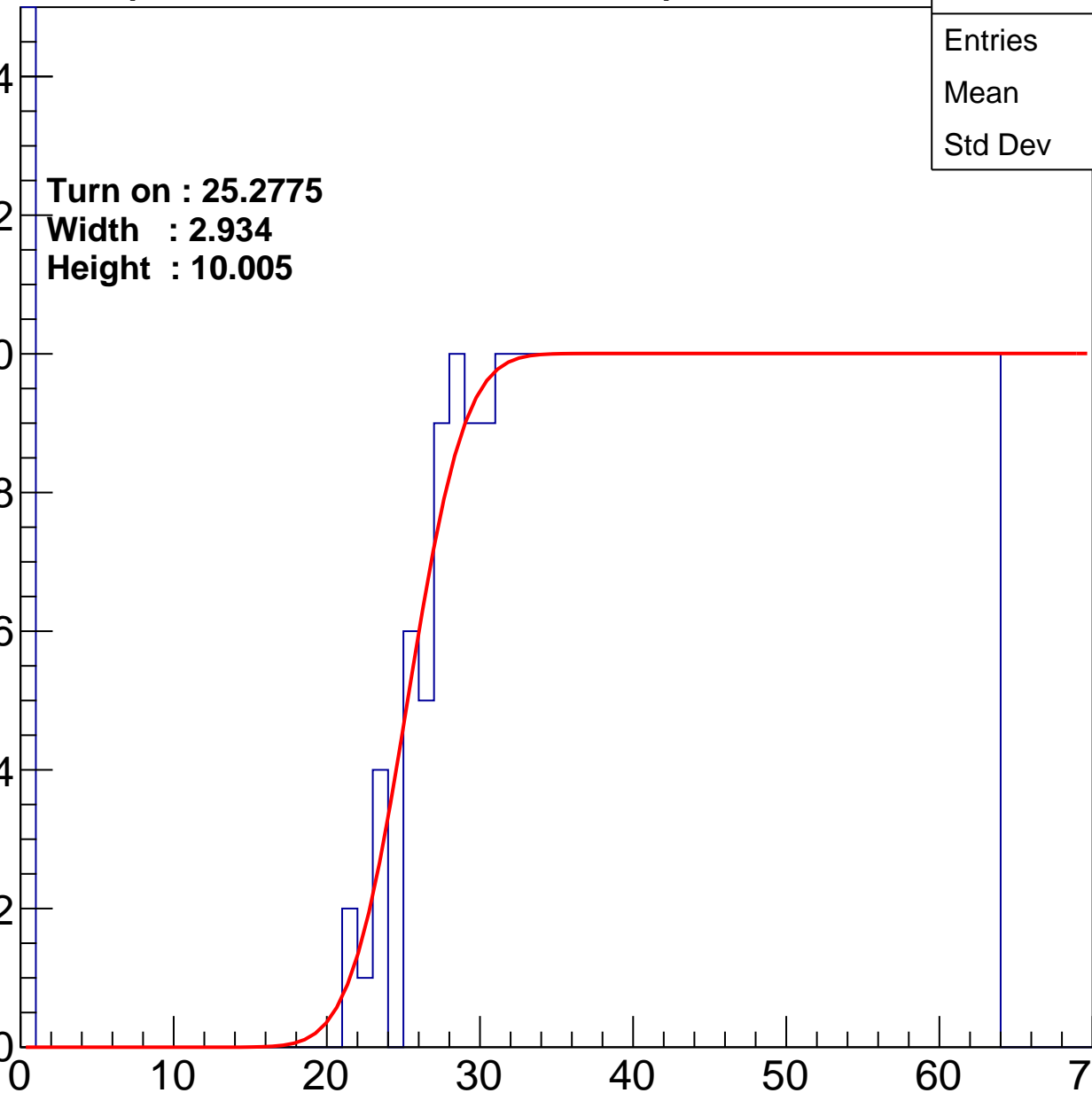
Width : 2.934

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	40.65
Std Dev	15.98

Turn on : 25.5279

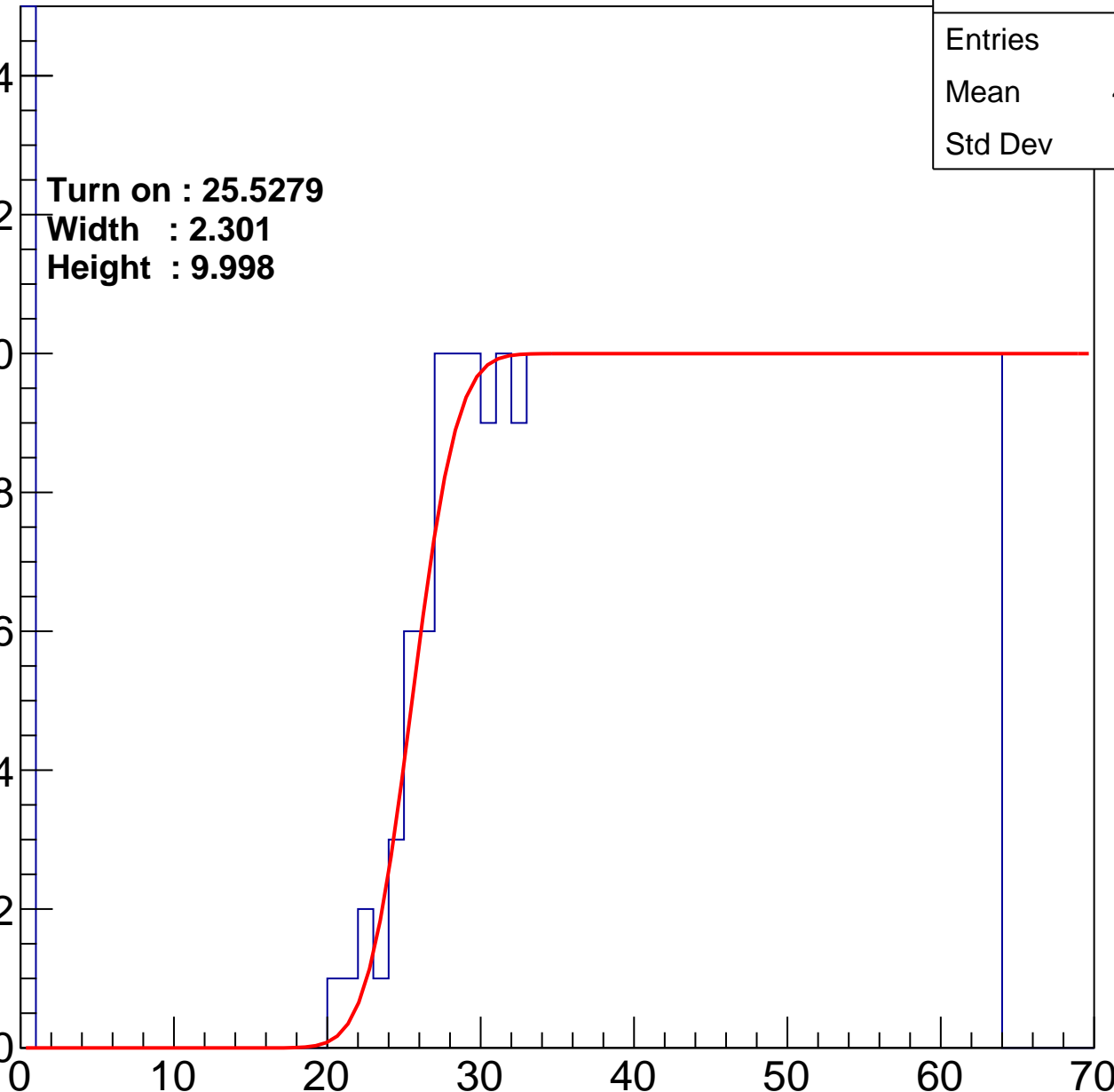
Width : 2.301

Height : 9.998

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch8

calib_packv5_041523_1651.root, FC#0, port C2

Entries	441
Mean	39.28
Std Dev	16.99

Turn on : 24.6085

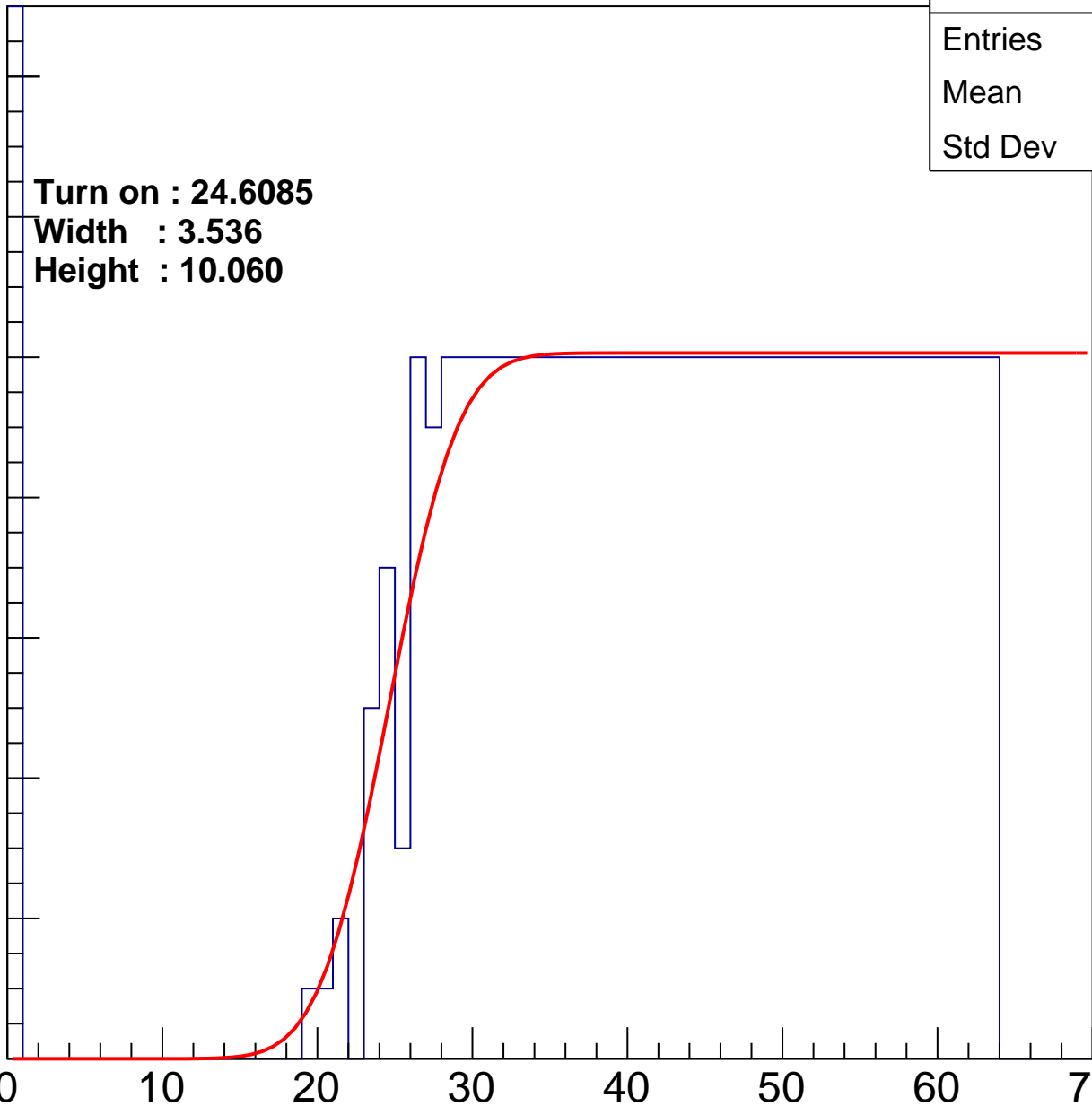
Width : 3.536

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch9

calib_packv5_041523_1651.root, FC#0, port C2

Entries	411
Mean	40.78
Std Dev	16.34

Turn on : 27.1023

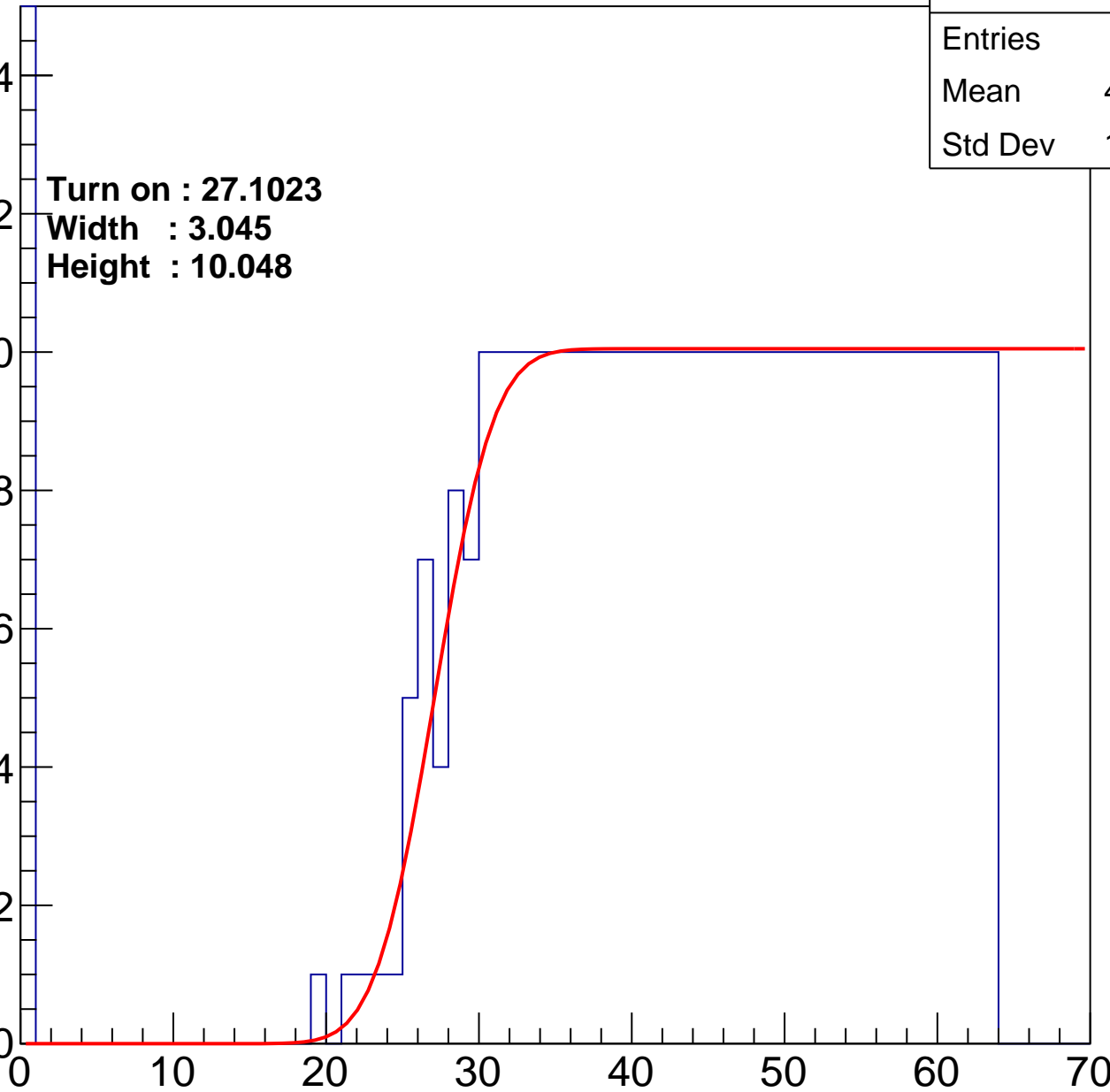
Width : 3.045

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch10

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	40.05
Std Dev	16.31

Turn on : 24.6145

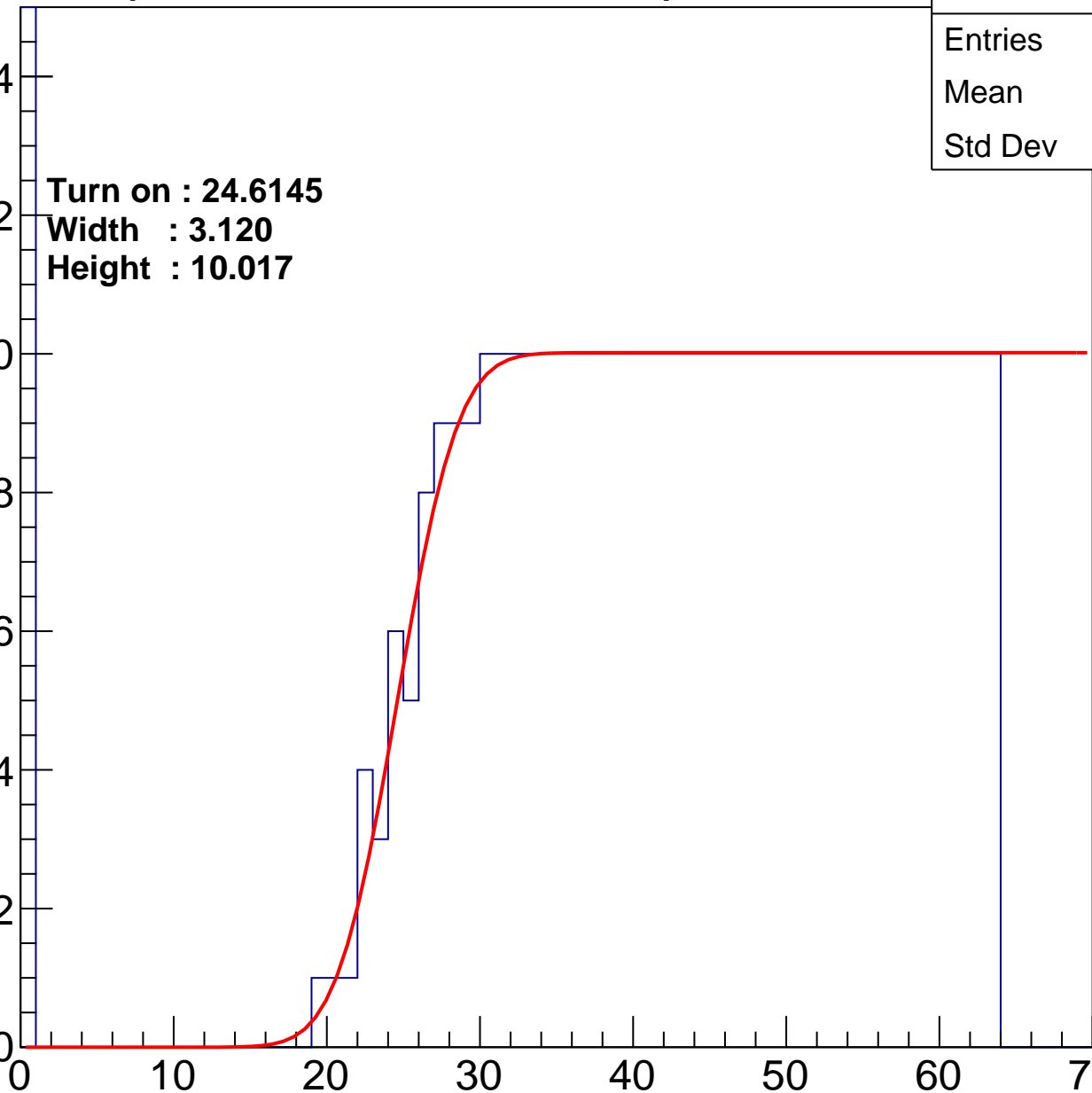
Width : 3.120

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch11

calib_packv5_041523_1651.root, FC#0, port C2

Entries	448
Mean	38.6
Std Dev	17.63

Turn on : 24.5628

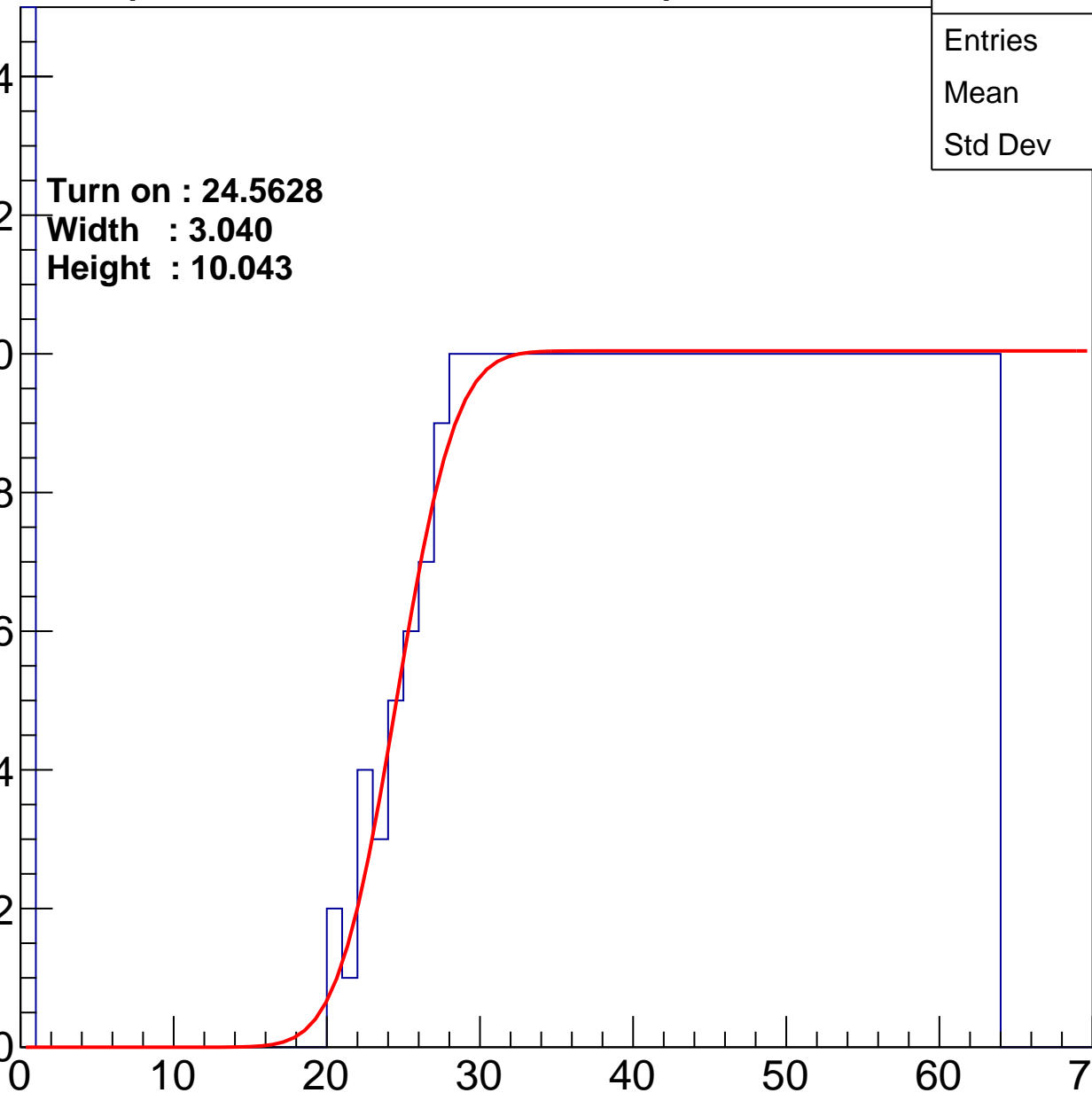
Width : 3.040

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch12

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	38.7
Std Dev	18.24

Turn on : 26.6414

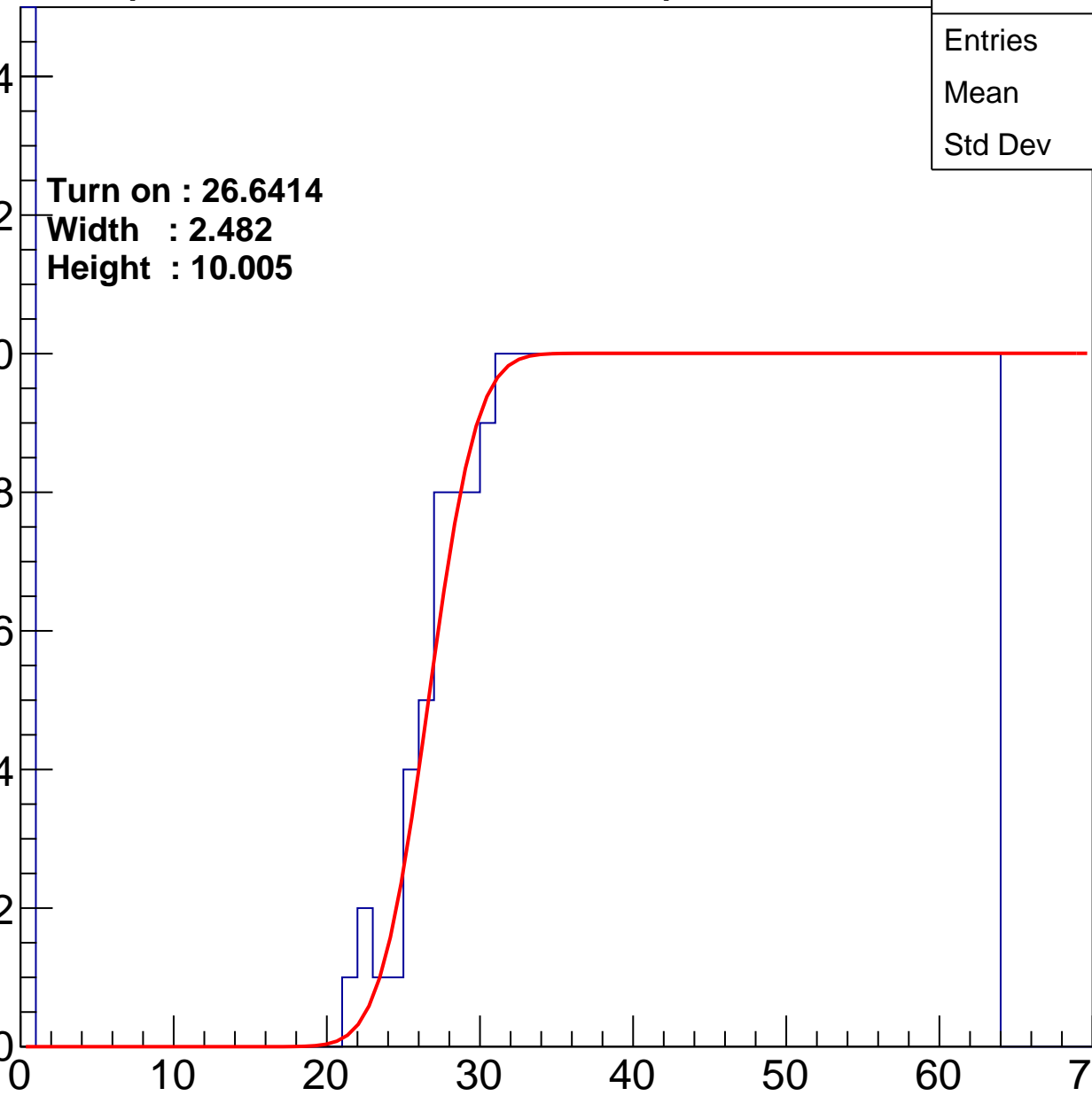
Width : 2.482

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch13

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	39.49
Std Dev	17.62

Turn on : 25.8004

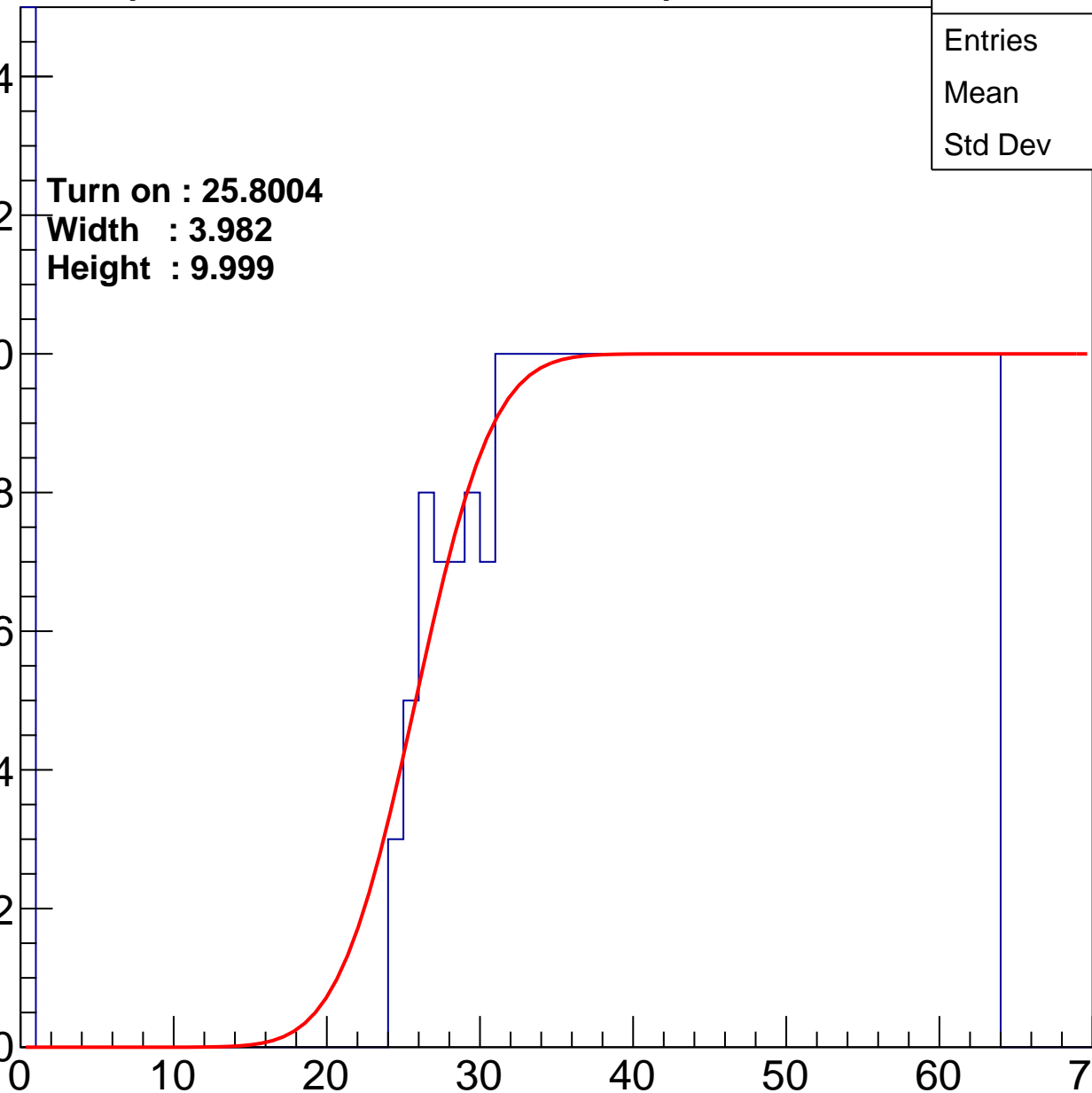
Width : 3.982

Height : 9.999

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch14

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	39.25
Std Dev	17.44

Turn on : 25.5868

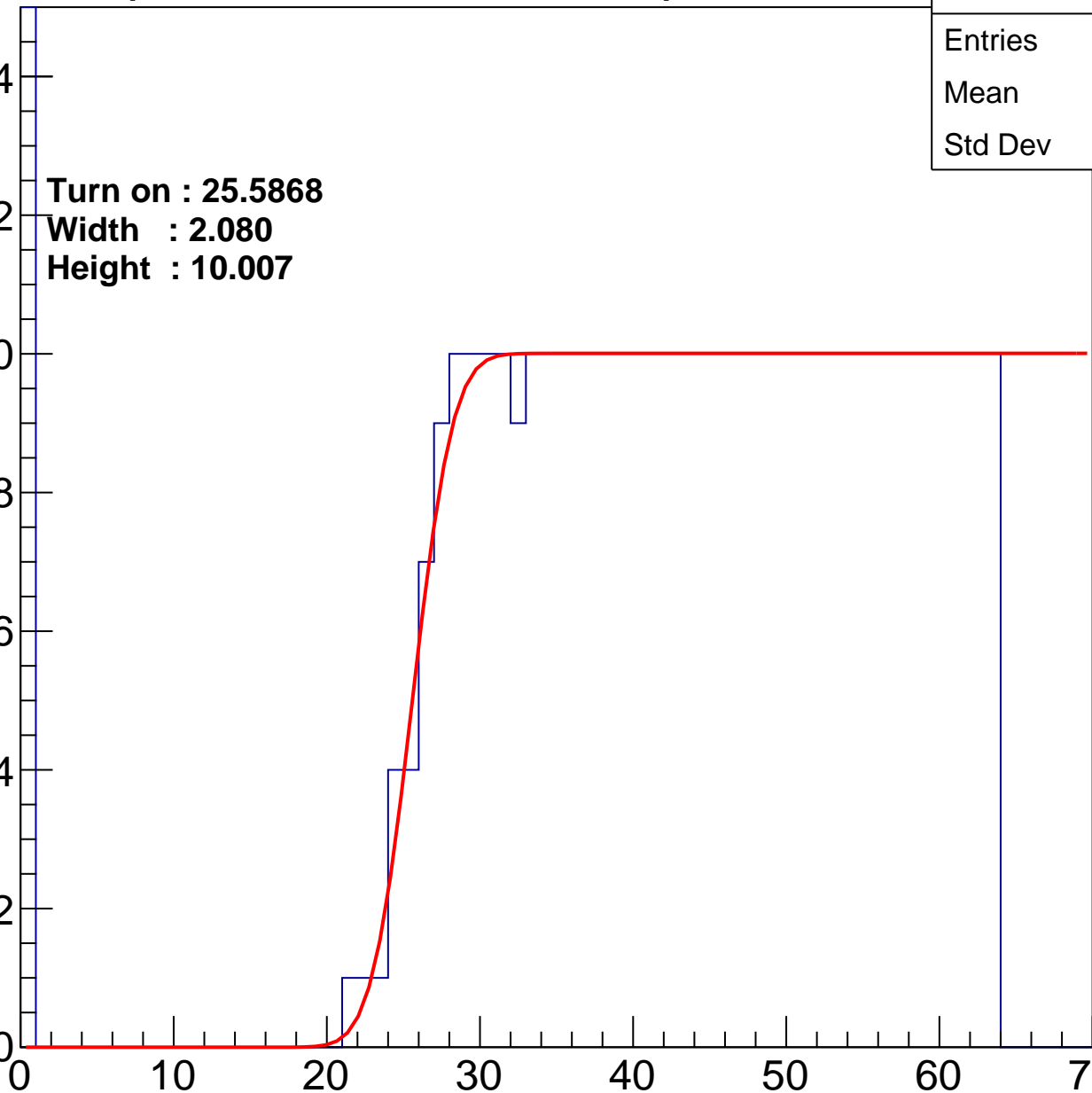
Width : 2.080

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch15

calib_packv5_041523_1651.root, FC#0, port C2

Entries	404
Mean	41.29
Std Dev	15.92

Turn on : 27.0882

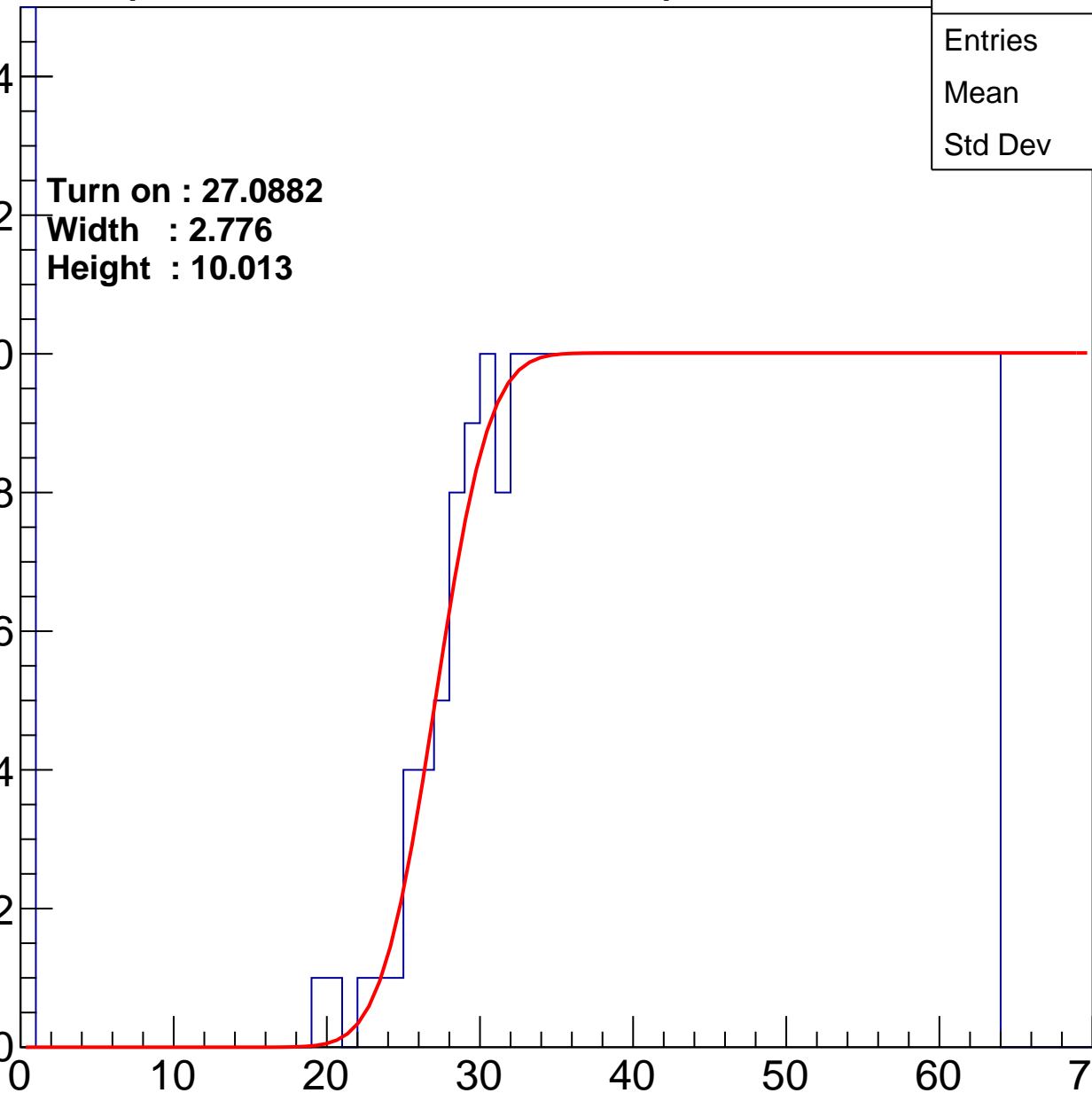
Width : 2.776

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch16

calib_packv5_041523_1651.root, FC#0, port C2

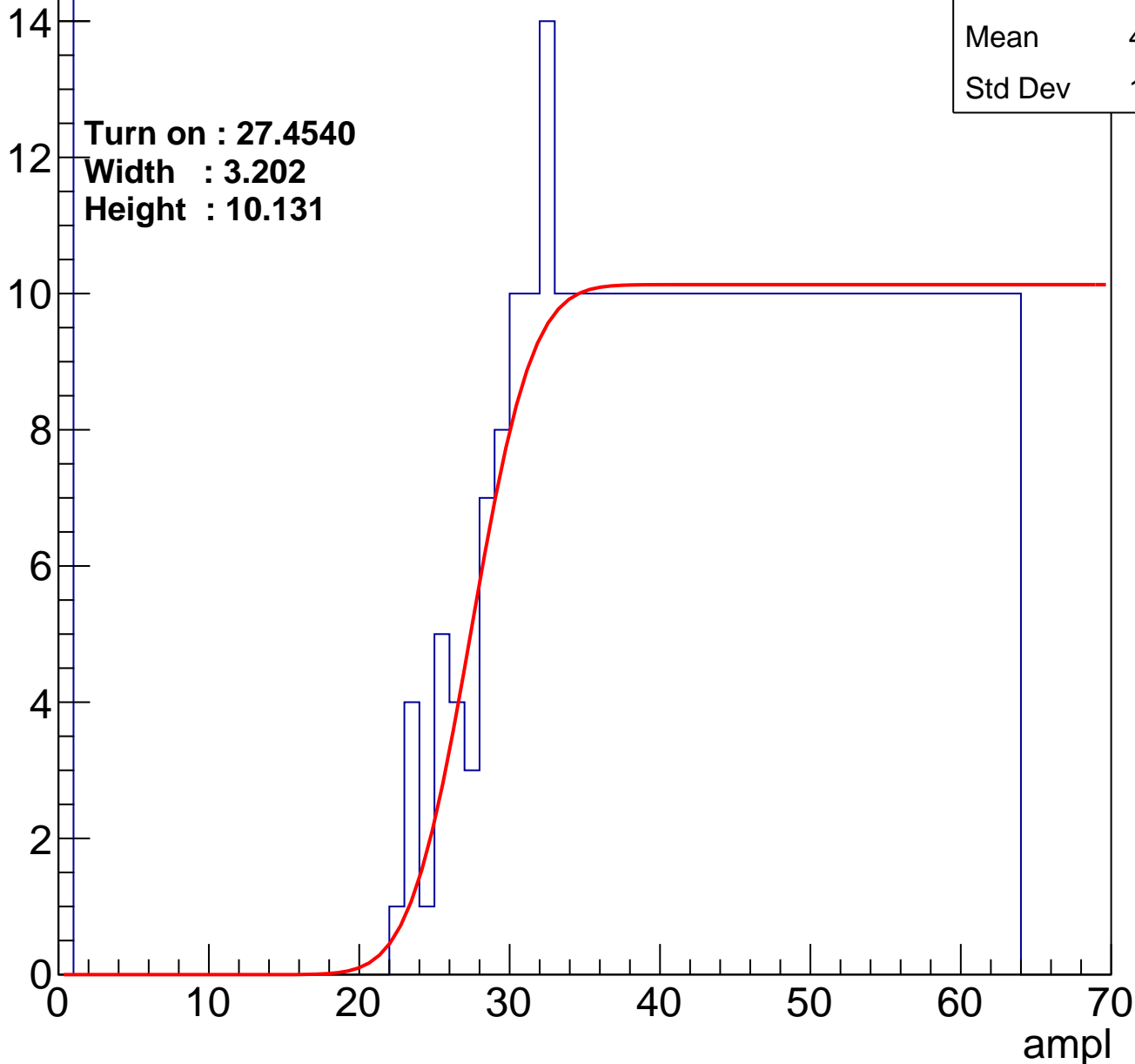
Entries	415
Mean	40.52
Std Dev	16.59

Turn on : 27.4540

Width : 3.202

Height : 10.131

Entry



B1L103S, U7-ch17

calib_packv5_041523_1651.root, FC#0, port C2

Entries	458
Mean	37.71
Std Dev	18.4

Turn on : 24.9573

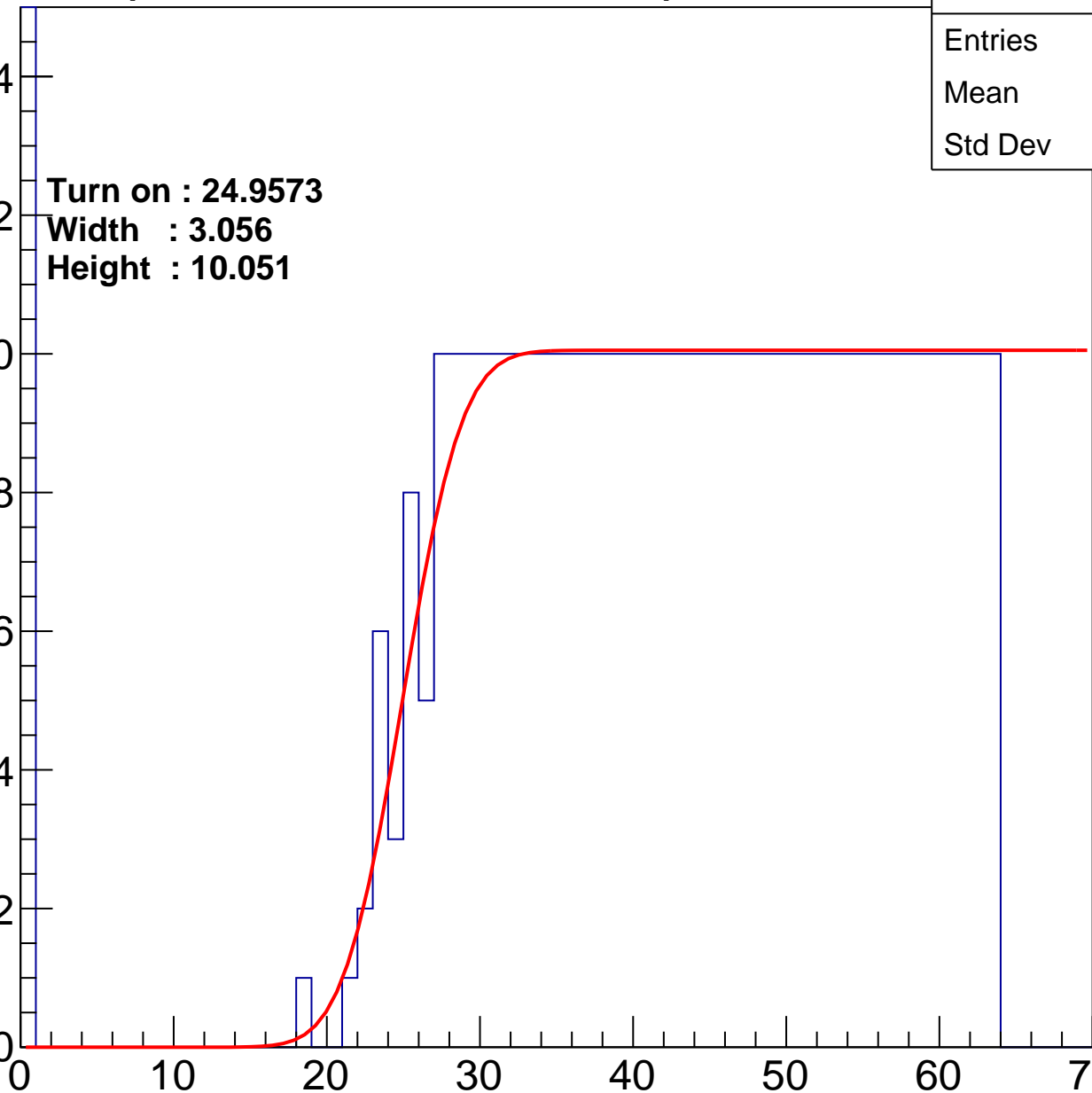
Width : 3.056

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch18

calib_packv5_041523_1651.root, FC#0, port C2

Entries	422
Mean	39.92
Std Dev	17.07

Turn on : 25.8474

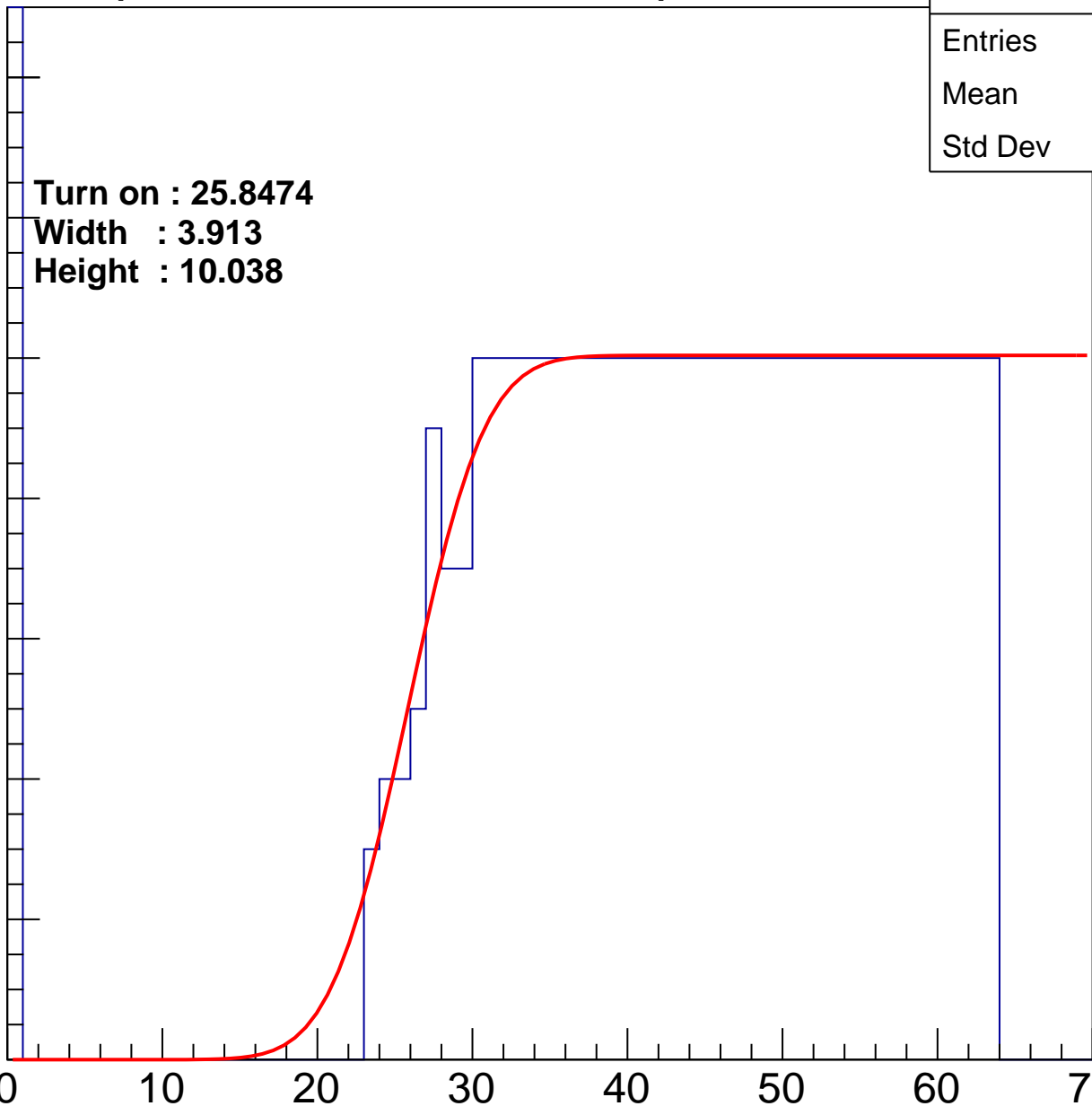
Width : 3.913

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch19

calib_packv5_041523_1651.root, FC#0, port C2

Entries	410
Mean	39.75
Std Dev	18.03

Turn on : 28.4171

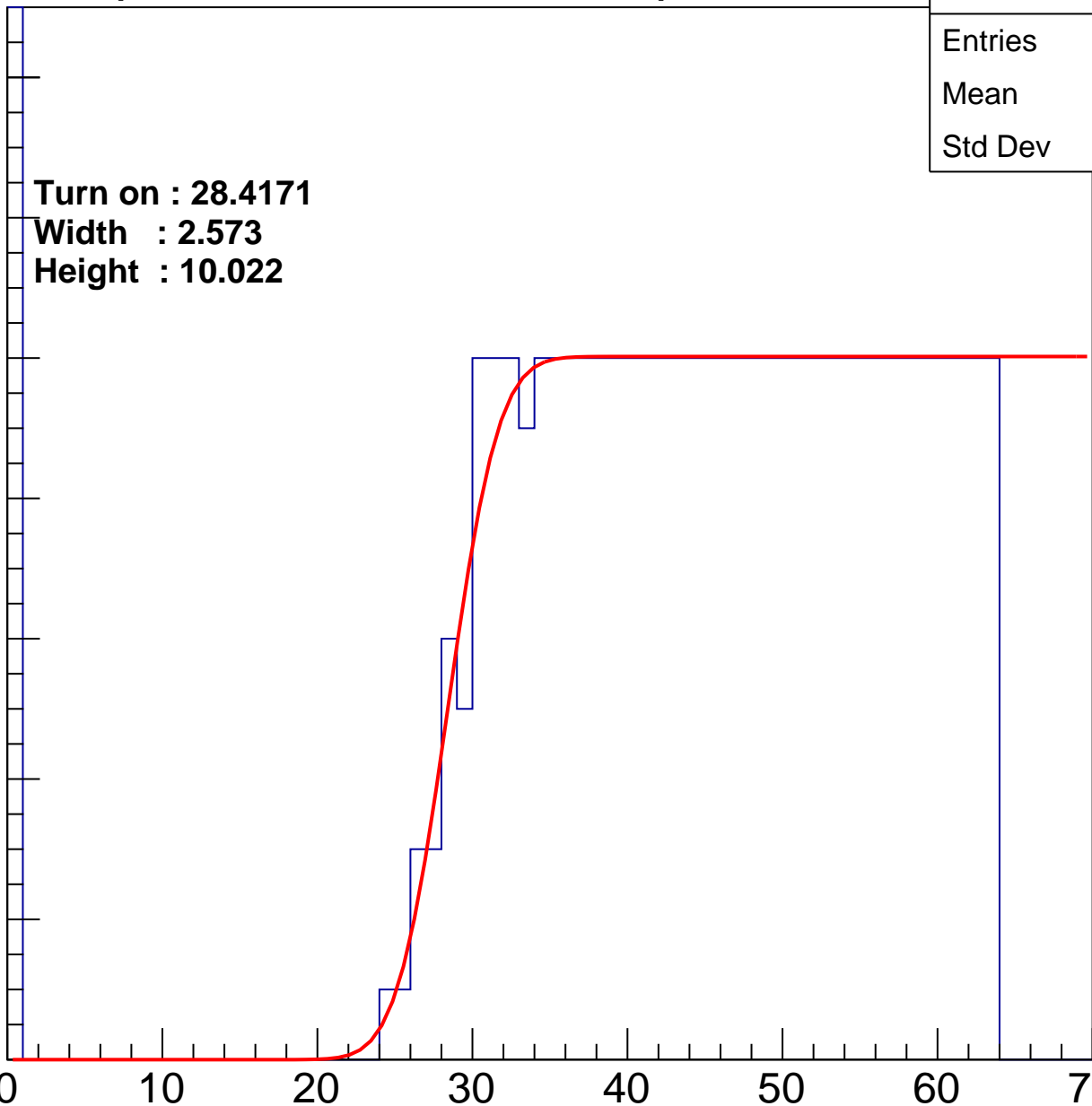
Width : 2.573

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch20

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	40.38
Std Dev	16.71

Turn on : 26.2220

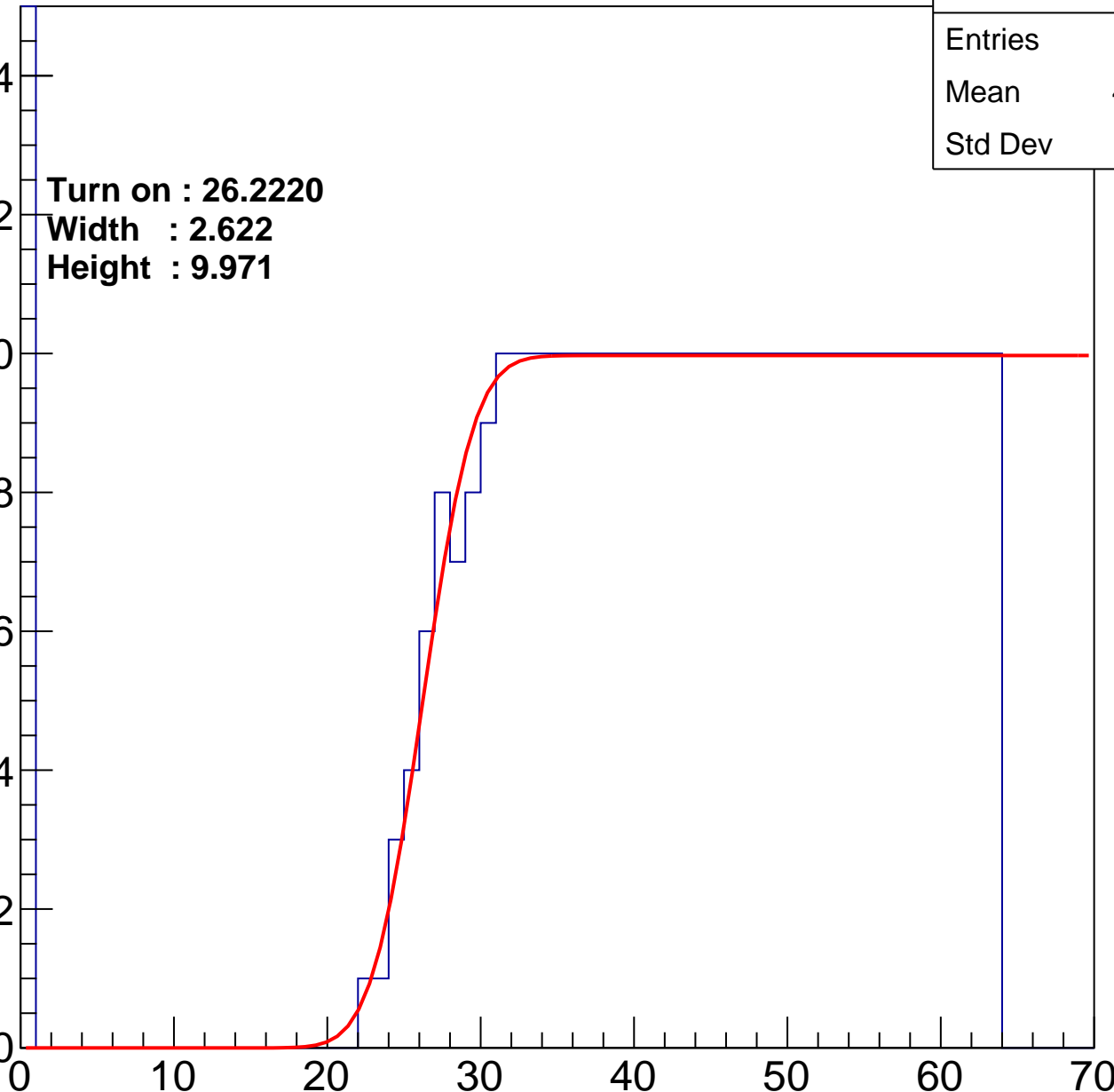
Width : 2.622

Height : 9.971

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch21

calib_packv5_041523_1651.root, FC#0, port C2

Entries	415
Mean	40.58
Std Dev	16.41

Turn on : 25.9100

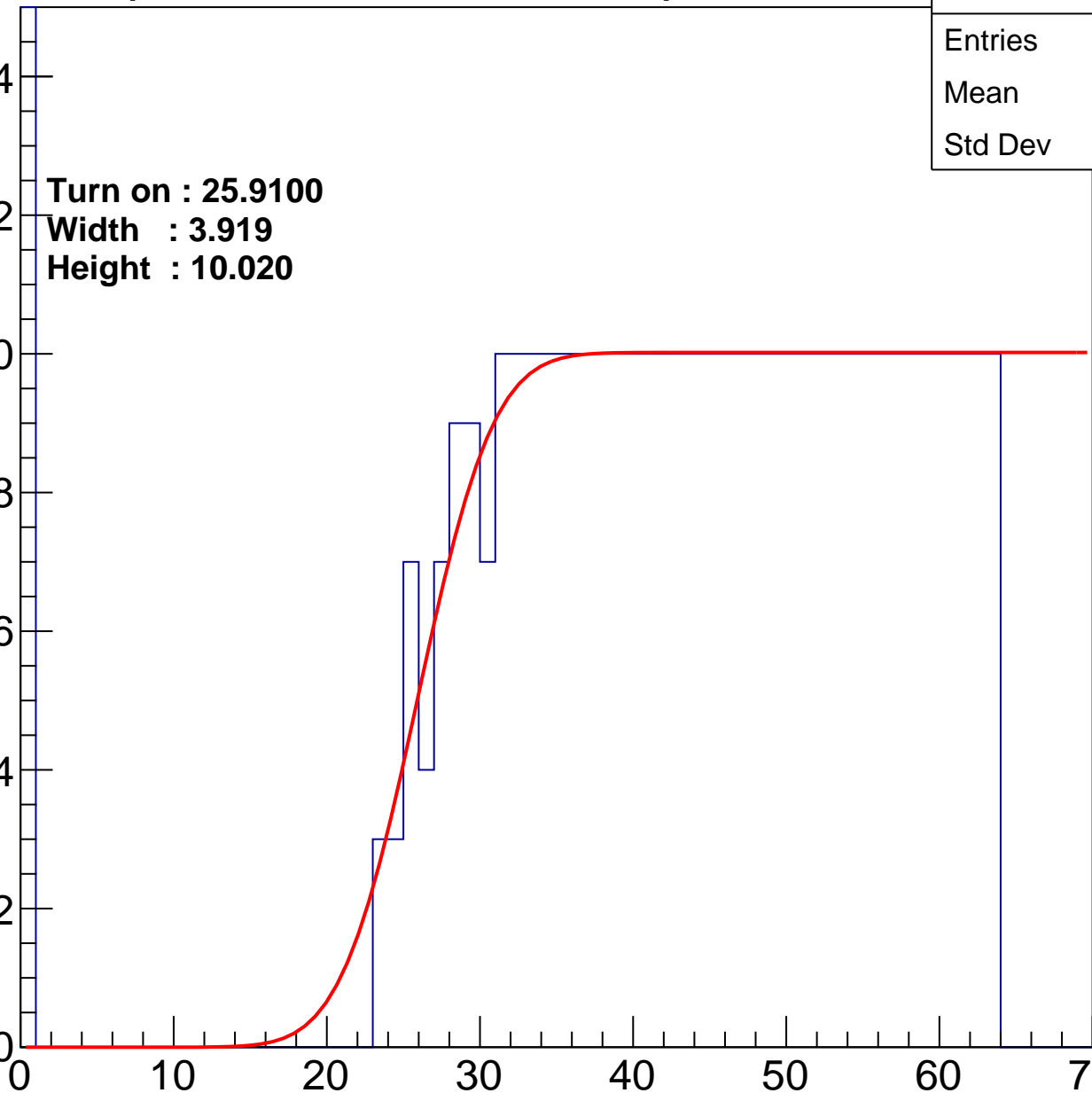
Width : 3.919

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch22

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	38.88
Std Dev	17.67

Turn on : 25.4342

Width : 2.214

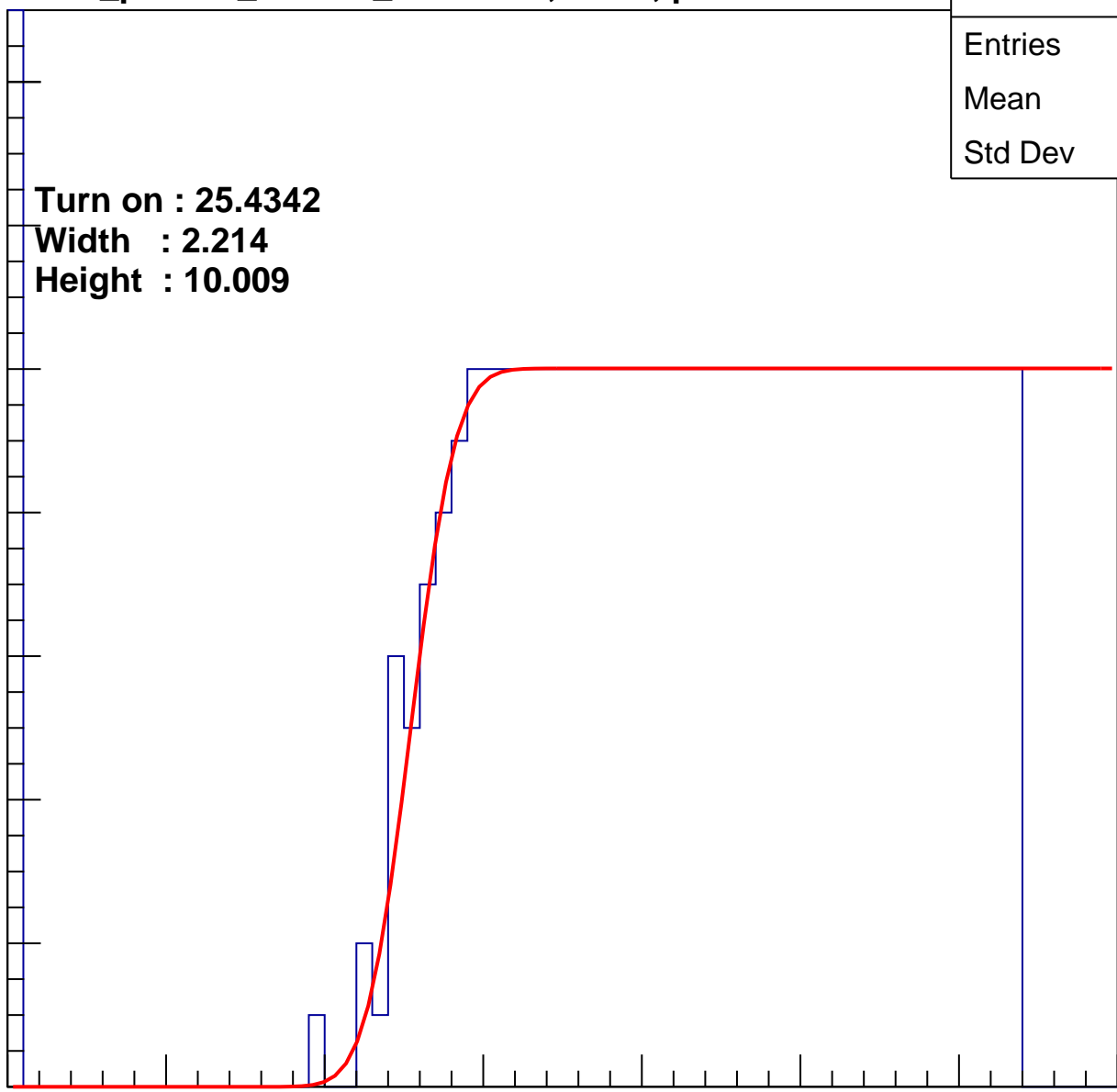
Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U7-ch23

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	39.68
Std Dev	17.24

Turn on : 26.0836

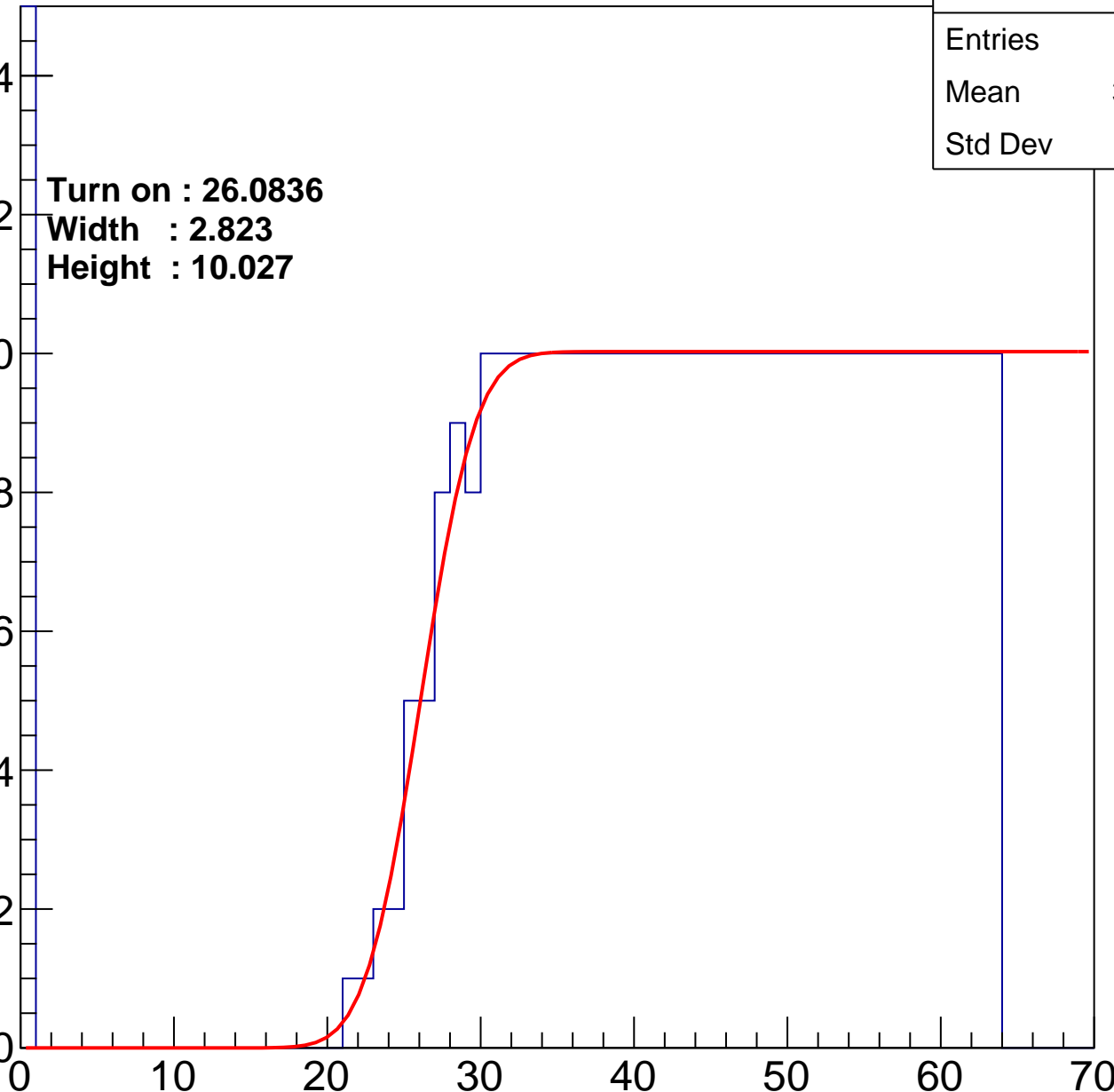
Width : 2.823

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch24

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	40.89
Std Dev	15.68

Turn on : 25.0814

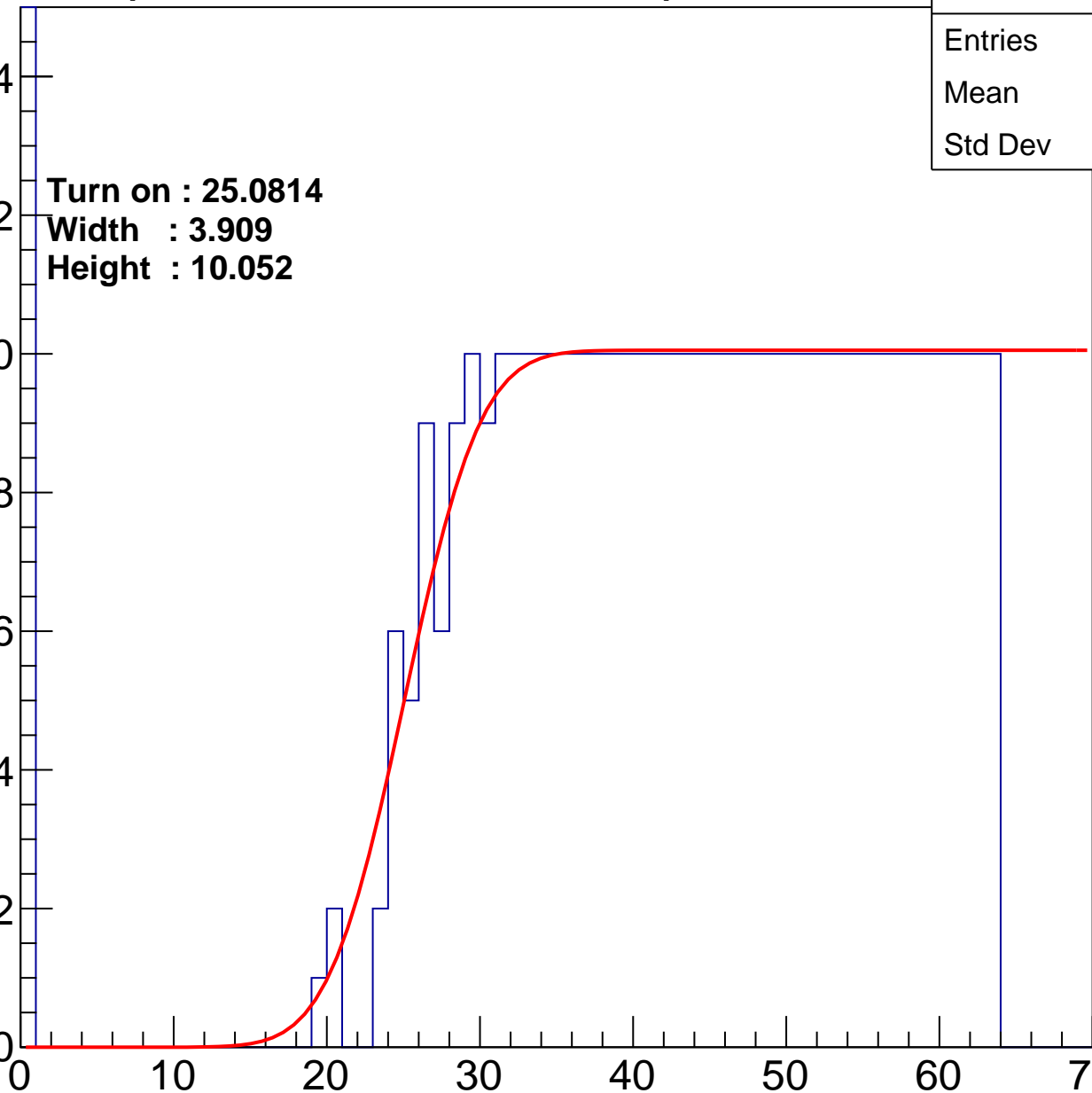
Width : 3.909

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch25

calib_packv5_041523_1651.root, FC#0, port C2

Entries	444
Mean	39.03
Std Dev	17.18

Turn on : 24.6722

Width : 3.740

Height : 10.069

Entry

14

12

10

8

6

4

2

0

0

10

20

30

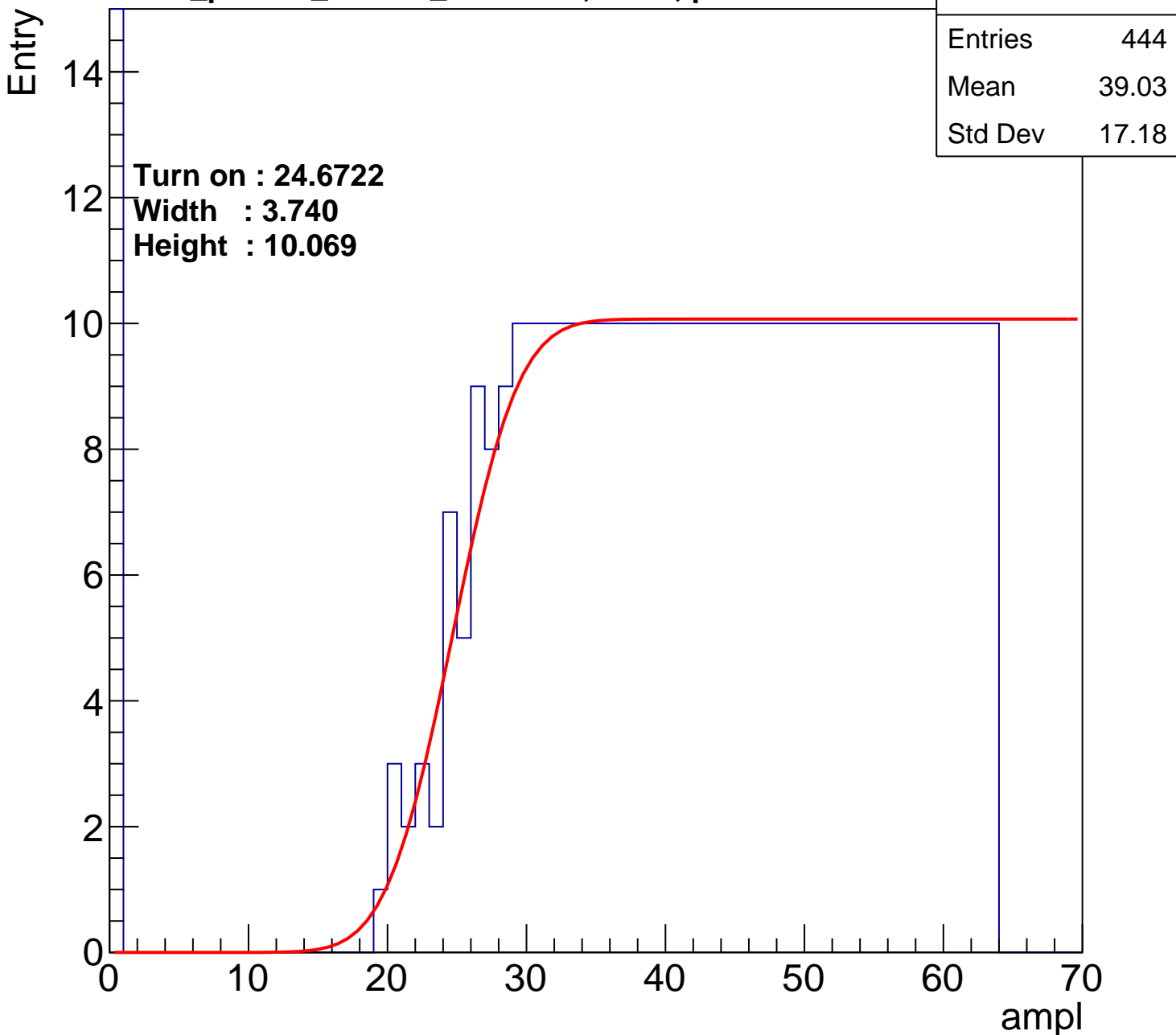
40

50

60

70

ampl



B1L103S, U7-ch26

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	39.98
Std Dev	17.17

Turn on : 26.1890

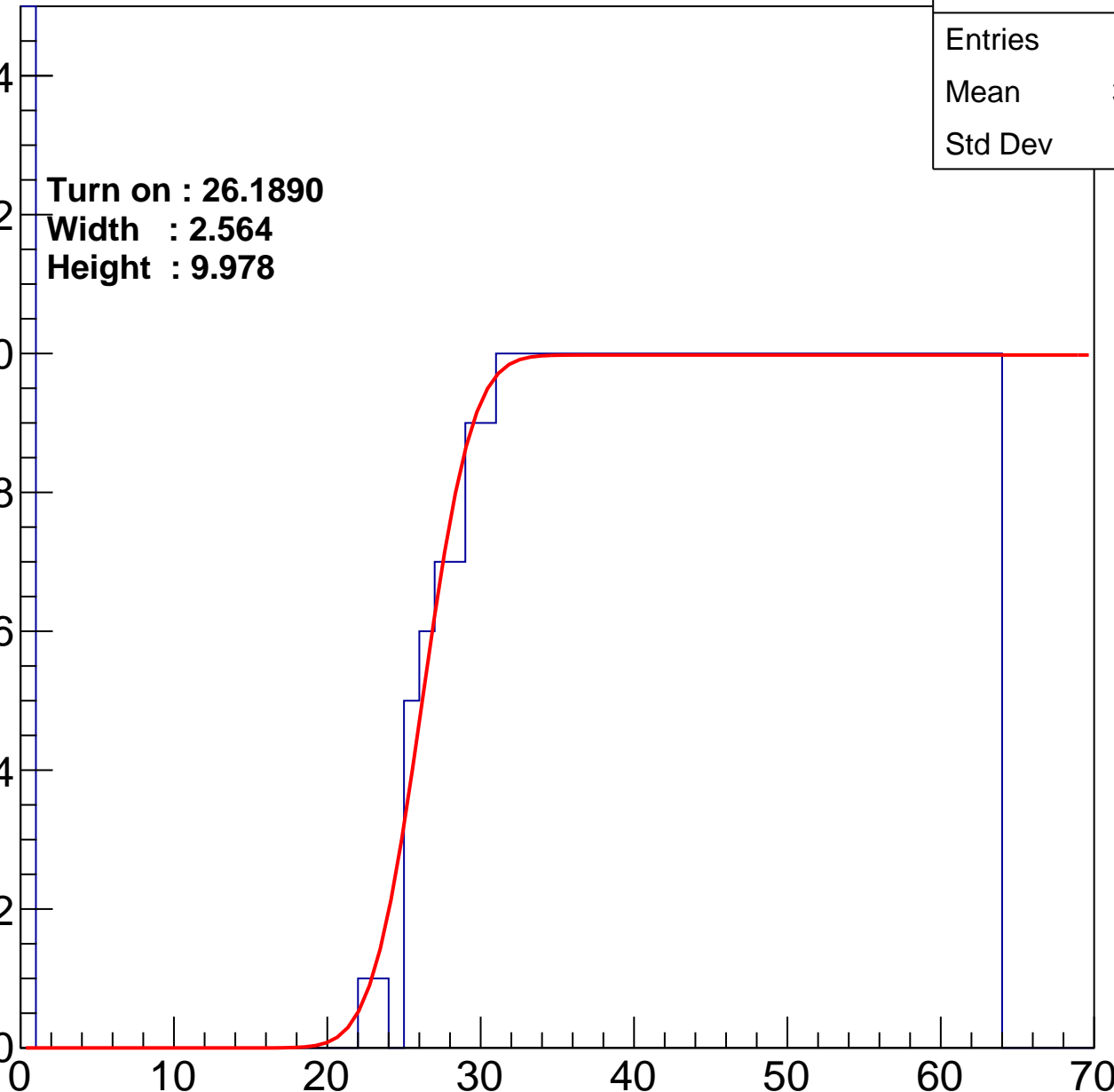
Width : 2.564

Height : 9.978

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch27

calib_packv5_041523_1651.root, FC#0, port C2

Entries	411
Mean	40.8
Std Dev	16.31

Turn on : 26.4509

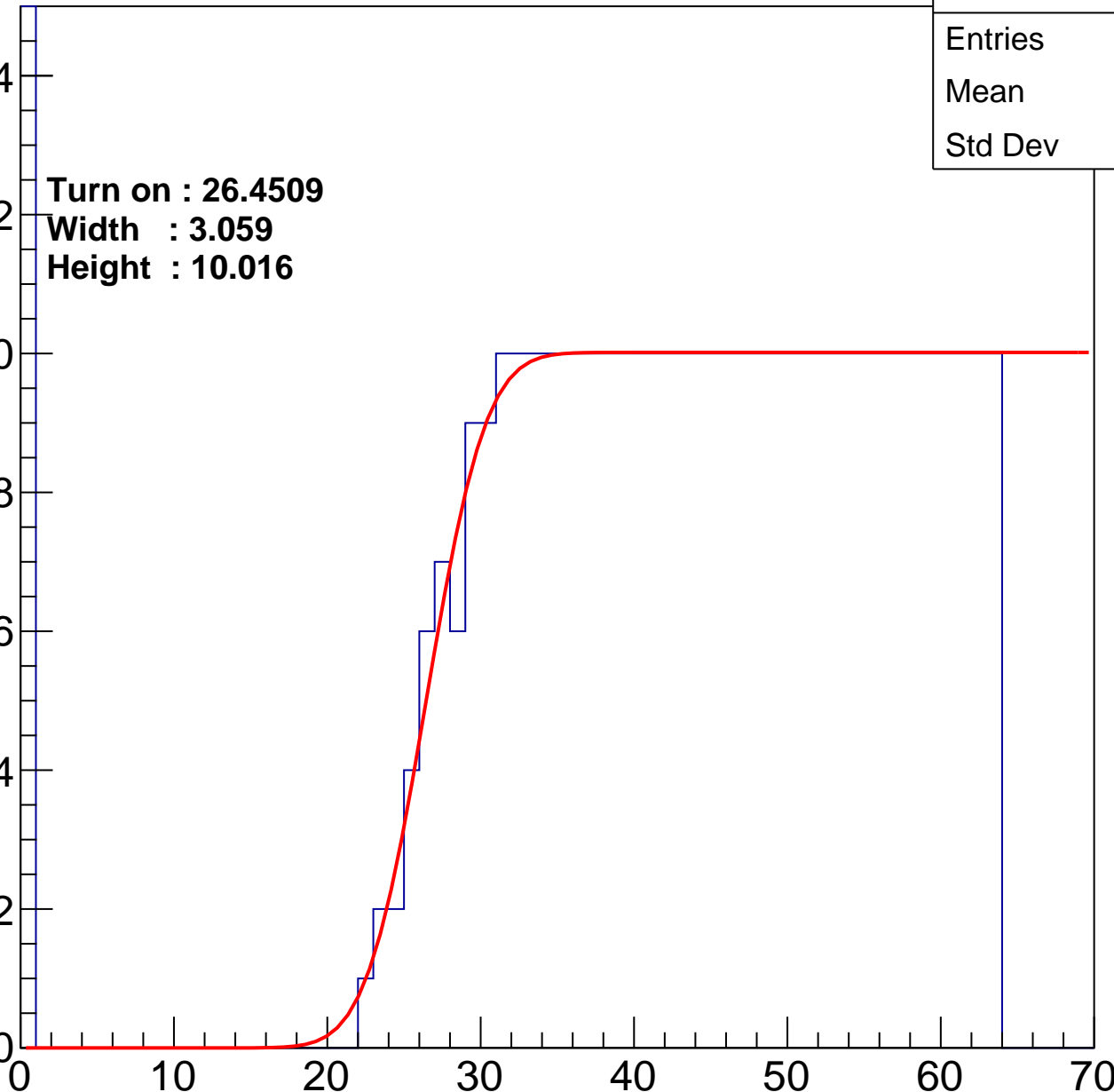
Width : 3.059

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch28

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	39.01
Std Dev	17.8

Turn on : 25.8788

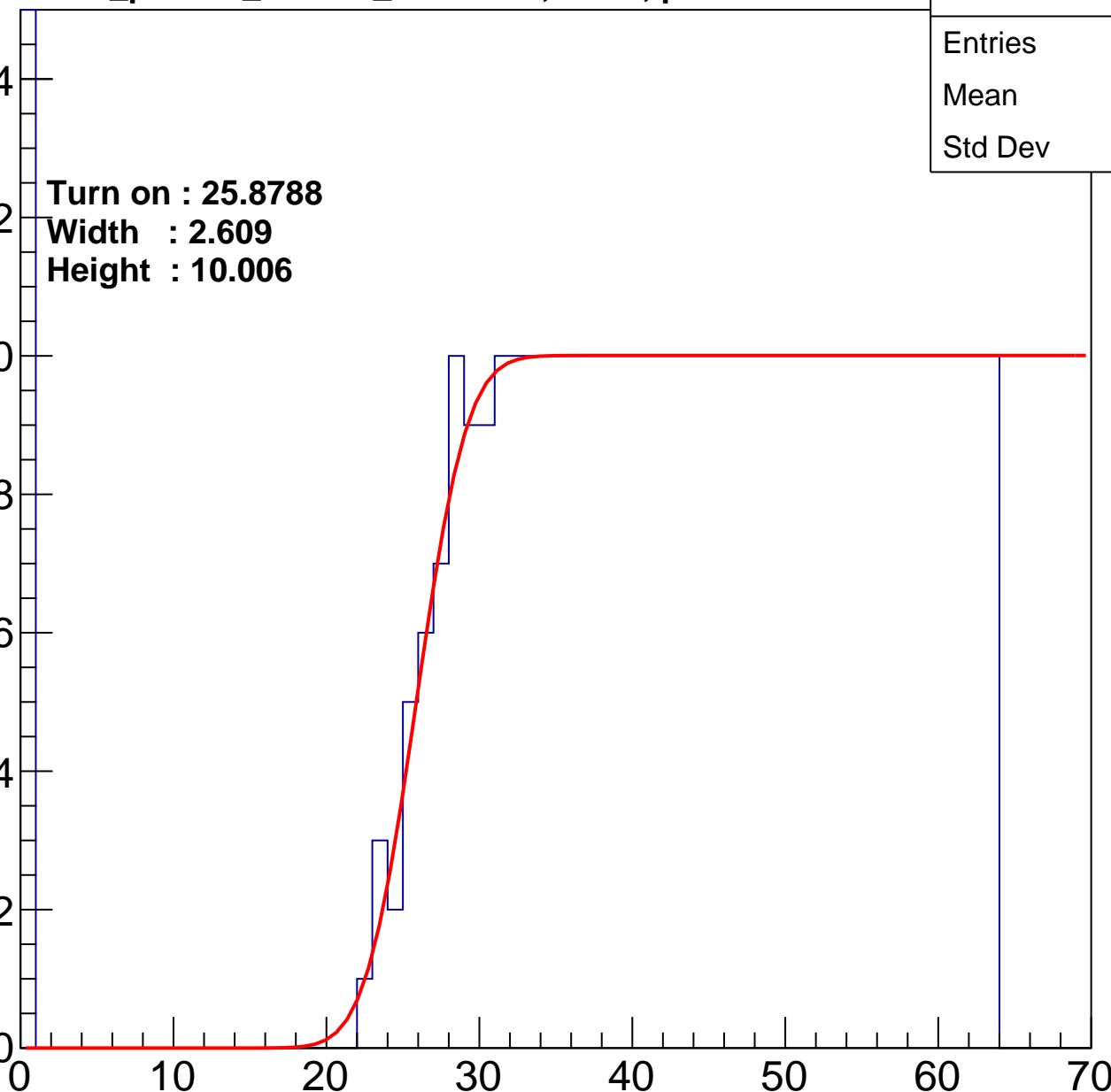
Width : 2.609

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch29

calib_packv5_041523_1651.root, FC#0, port C2

Entries	398
Mean	41.45
Std Dev	16.03

Turn on : 27.7195

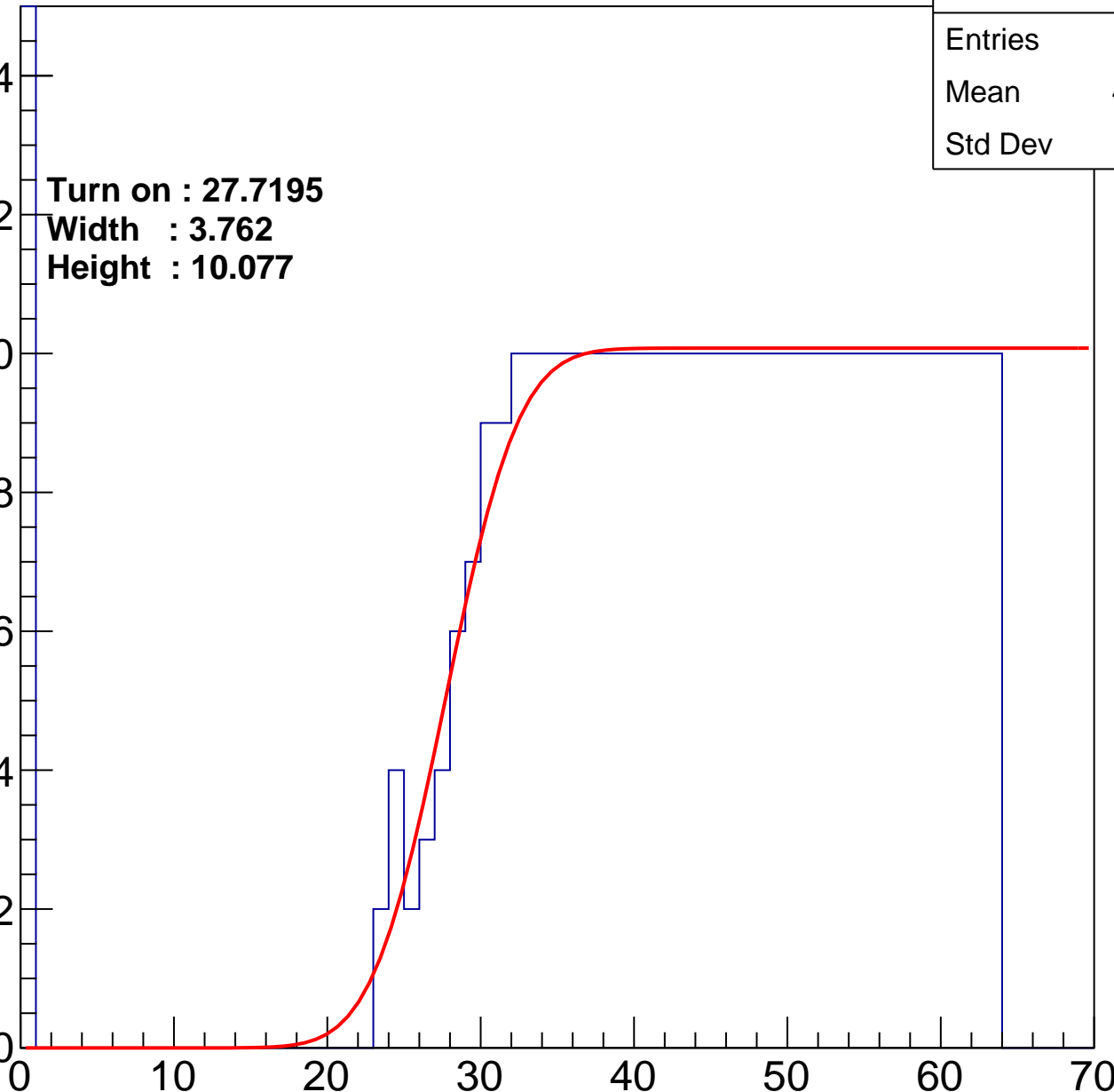
Width : 3.762

Height : 10.077

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch30

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	39.79
Std Dev	17.05

Turn on : 25.8142

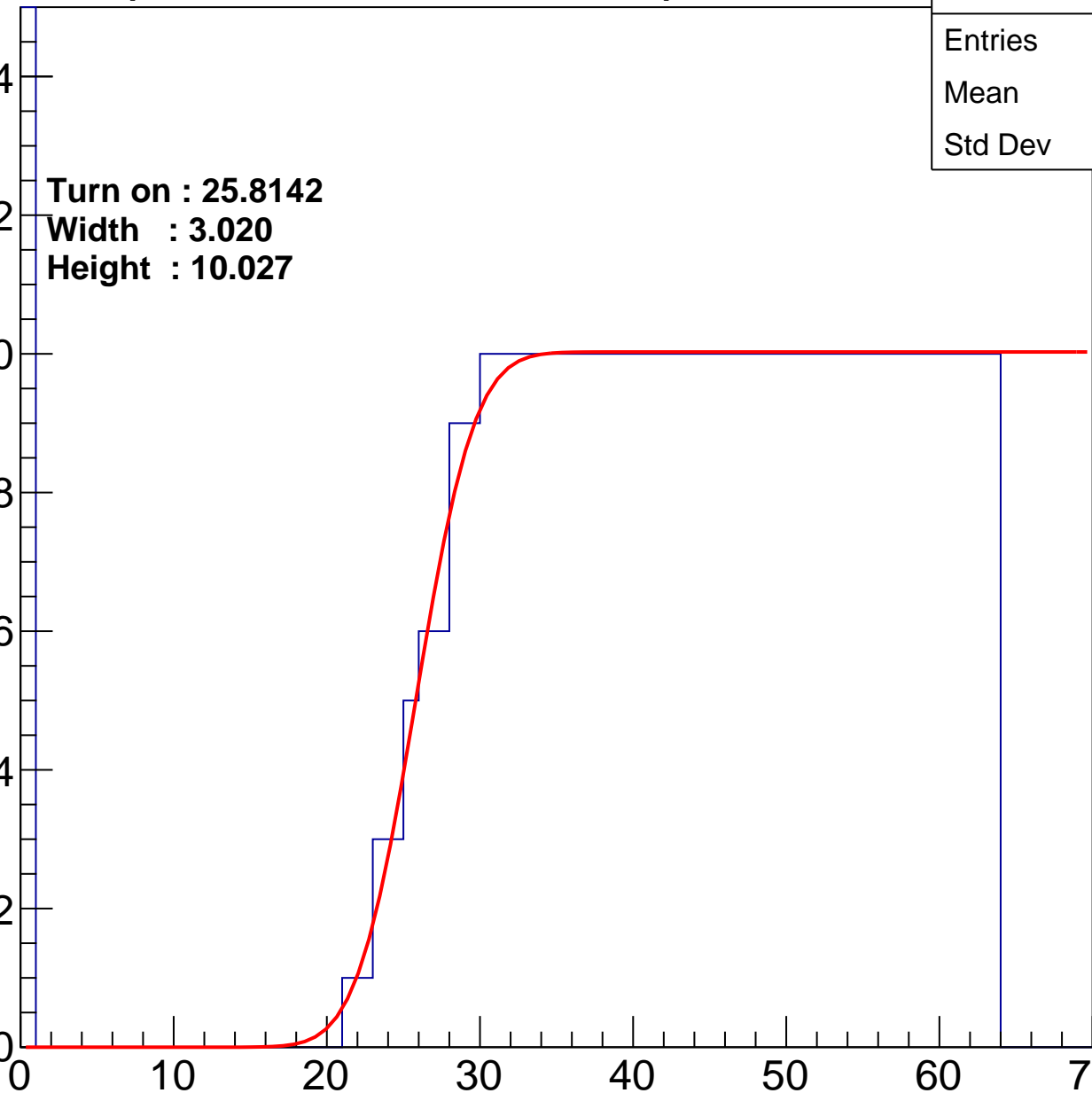
Width : 3.020

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch31

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	40.07
Std Dev	16.97

Turn on : 26.7137

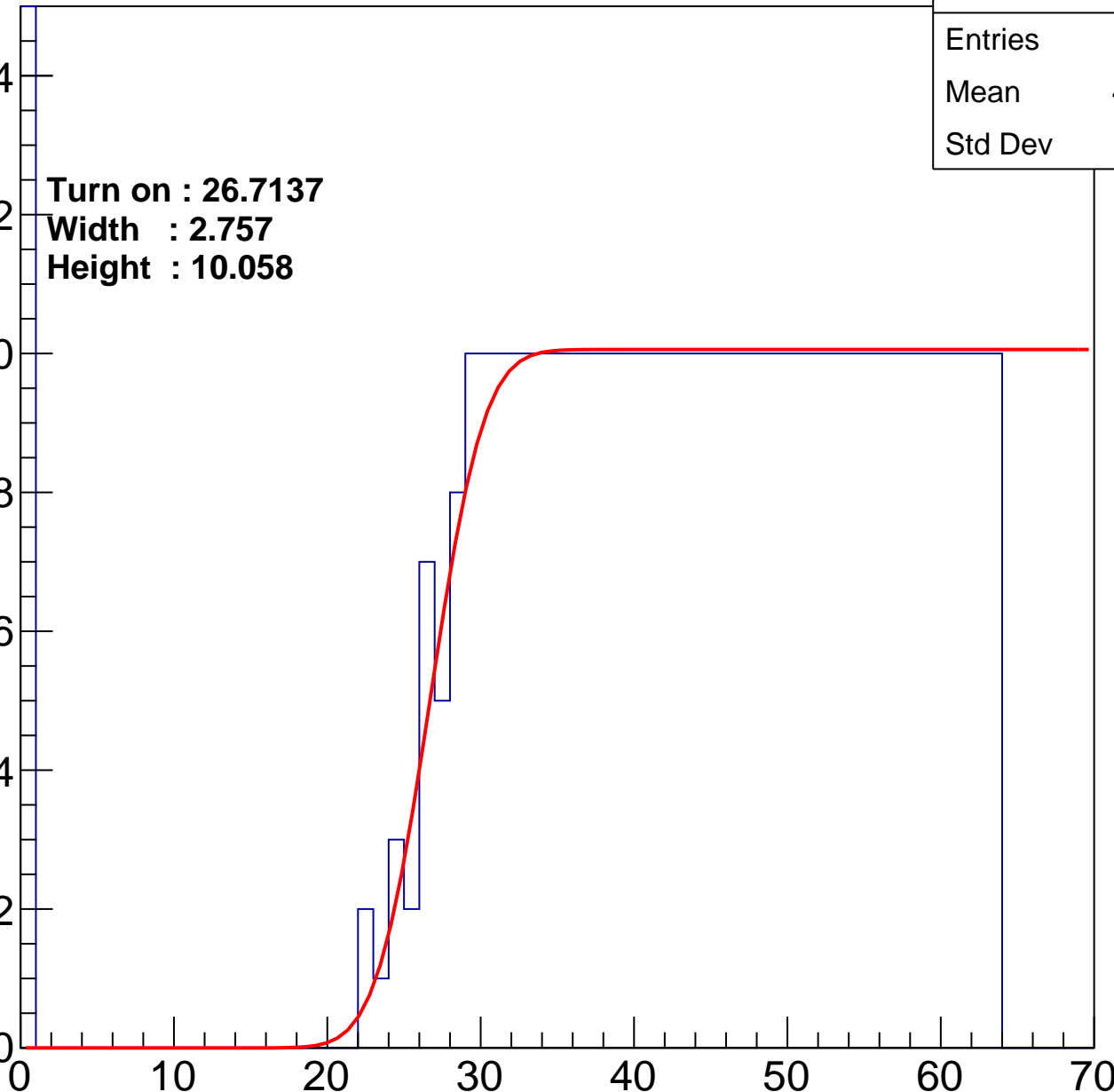
Width : 2.757

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch32

calib_packv5_041523_1651.root, FC#0, port C2

Entries	405
Mean	40.47
Std Dev	17.26

Turn on : 27.7462

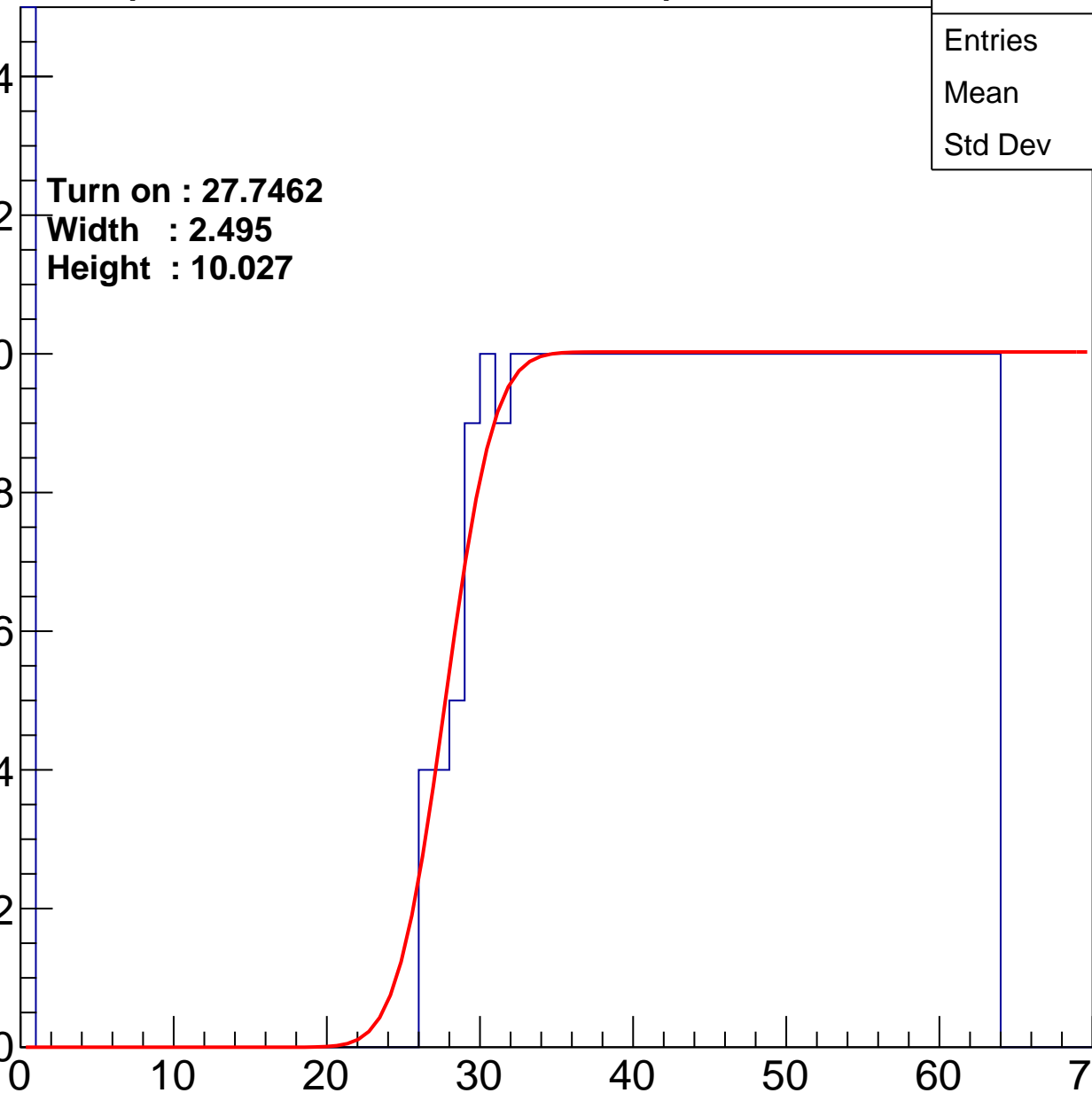
Width : 2.495

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch33

calib_packv5_041523_1651.root, FC#0, port C2

Entries	445
Mean	38.72
Std Dev	17.63

Turn on : 24.9637

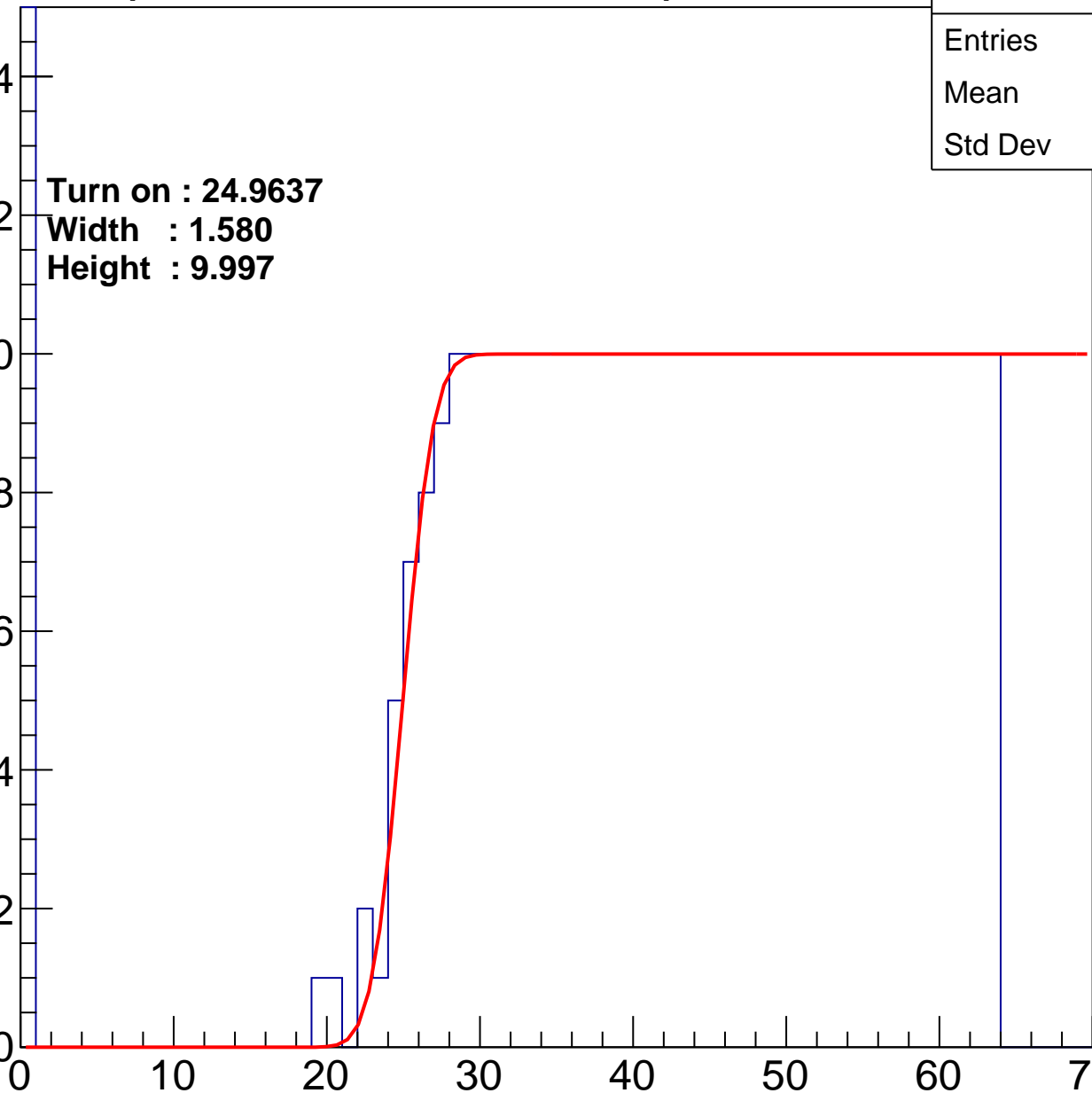
Width : 1.580

Height : 9.997

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch34

calib_packv5_041523_1651.root, FC#0, port C2

Entries	427
Mean	39.89
Std Dev	16.84

Turn on : 25.3044

Width : 1.916

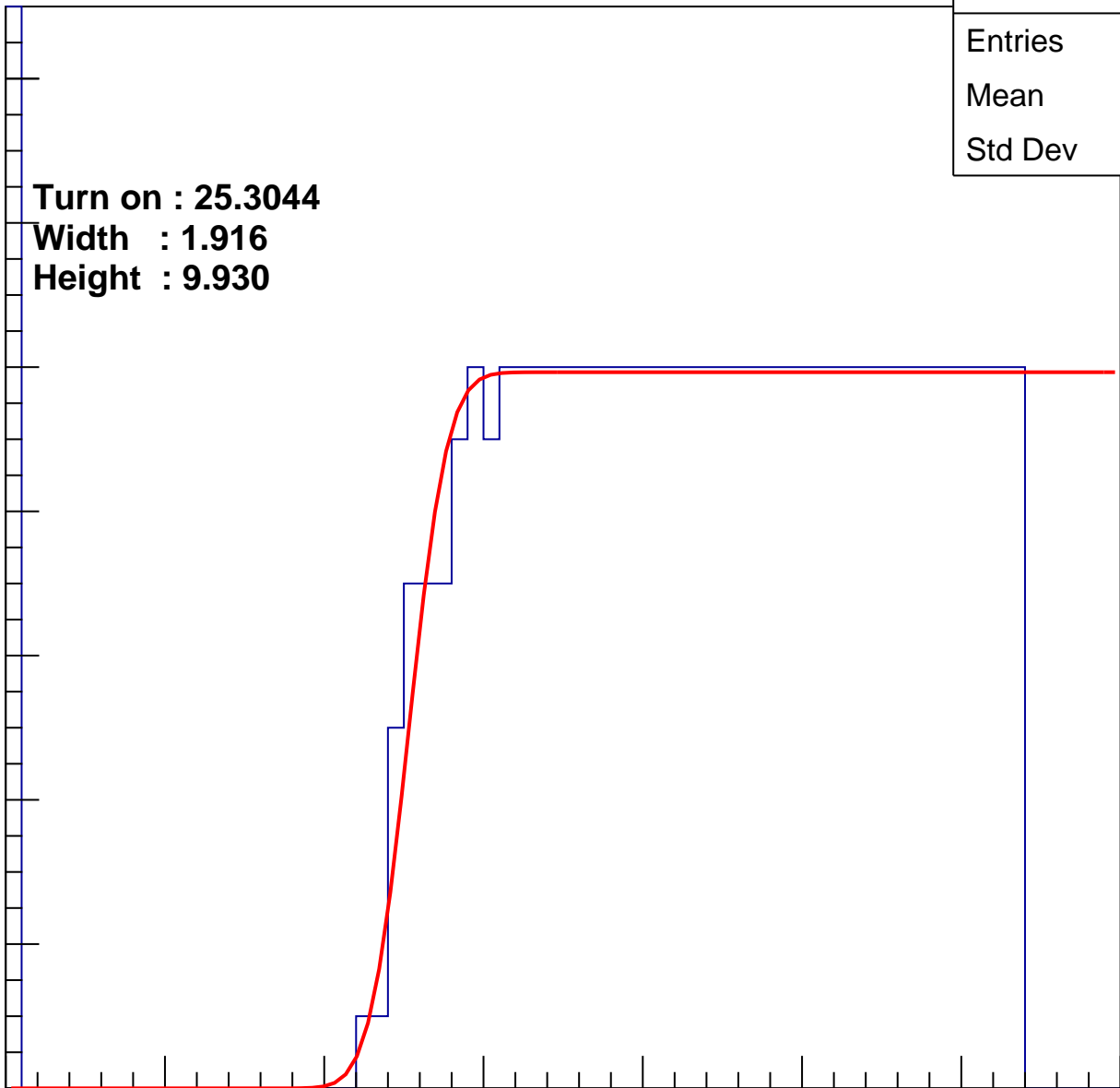
Height : 9.930

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U7-ch35

calib_packv5_041523_1651.root, FC#0, port C2

Entries	408
Mean	41.05
Std Dev	16.09

Turn on : 26.5840

Width : 2.804

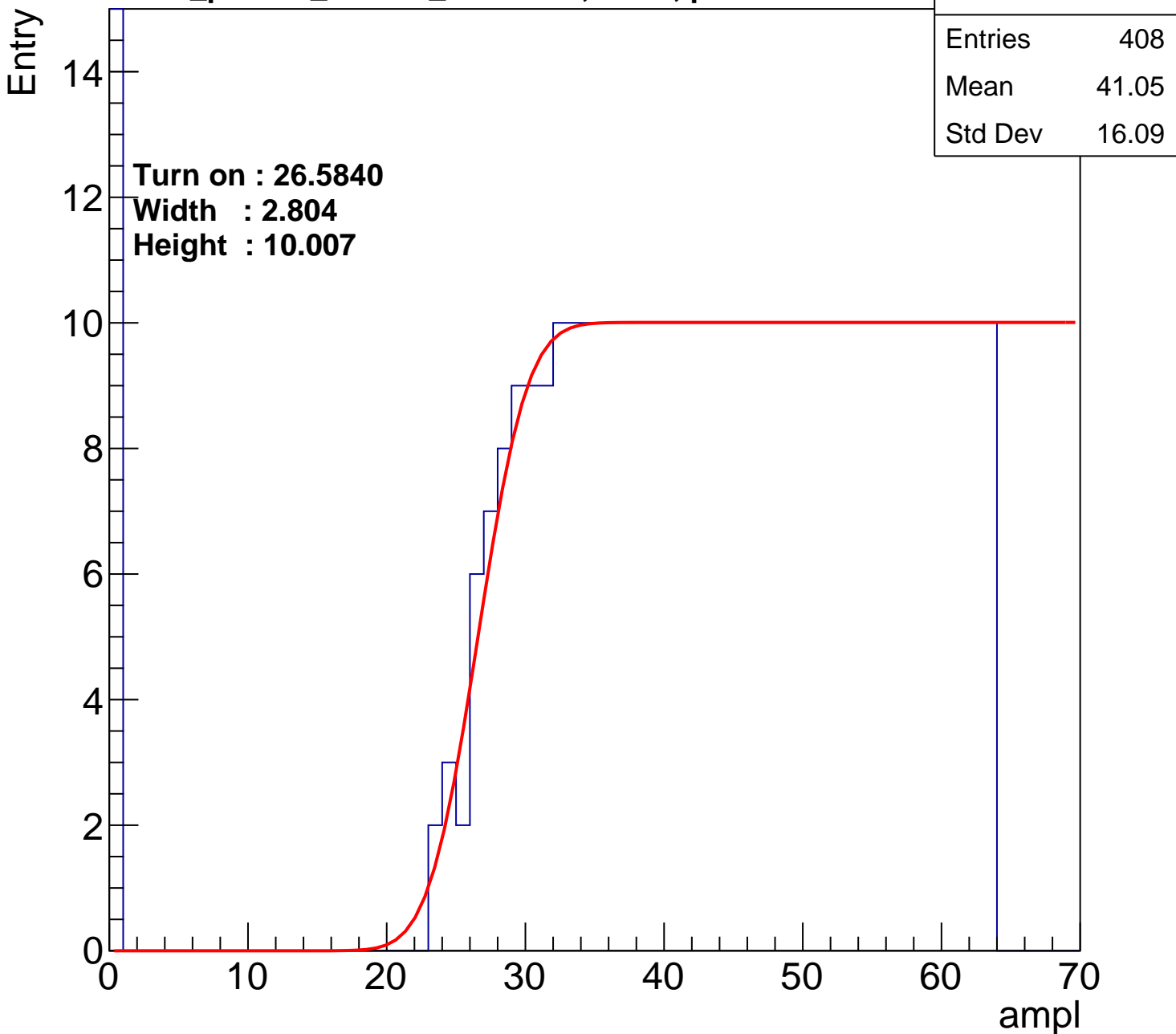
Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U7-ch36

calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	40.16
Std Dev	15.99

Turn on : 24.0939

Width : 2.756

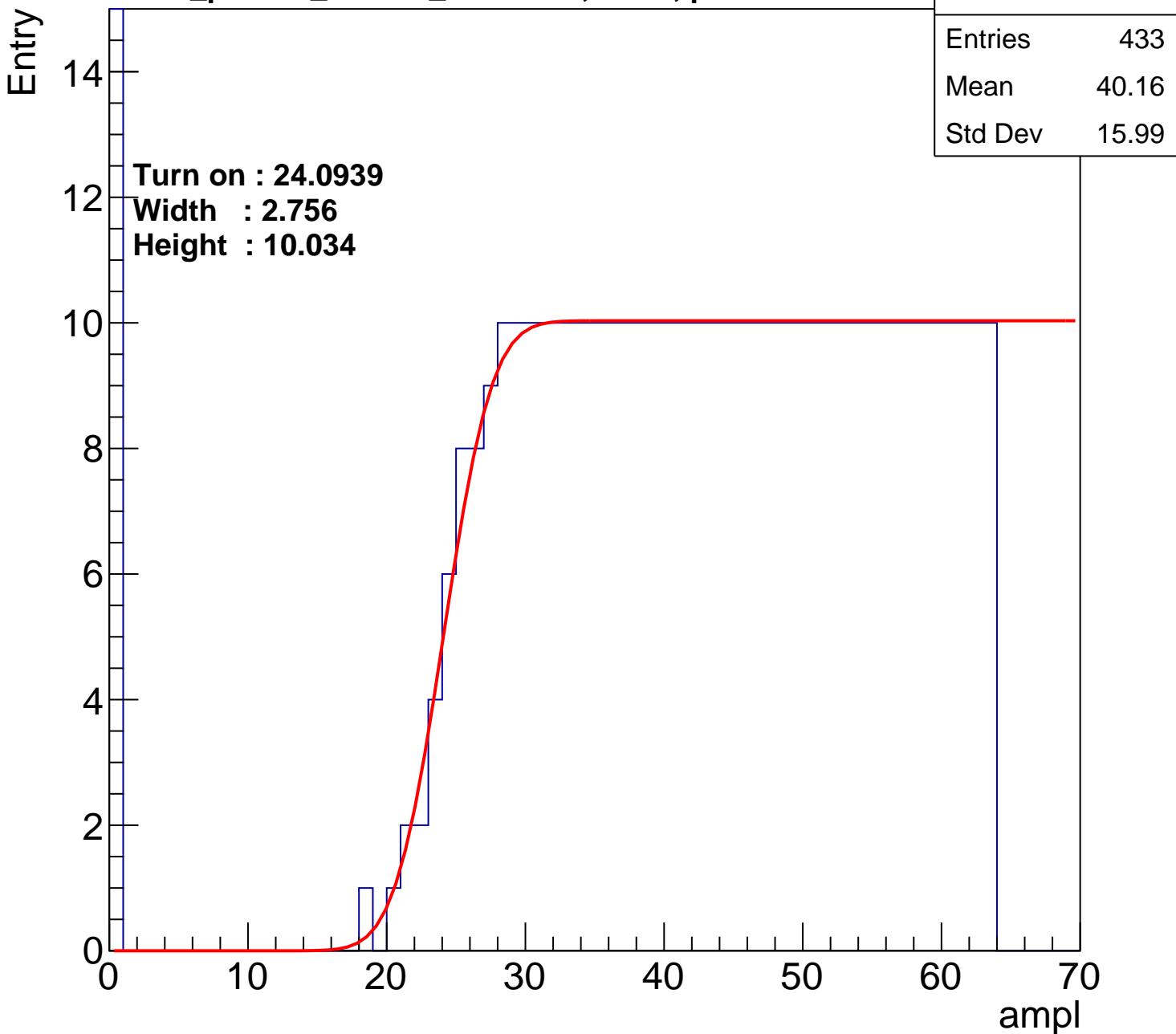
Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U7-ch37

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	39.11
Std Dev	17.5

Turn on : 25.8289

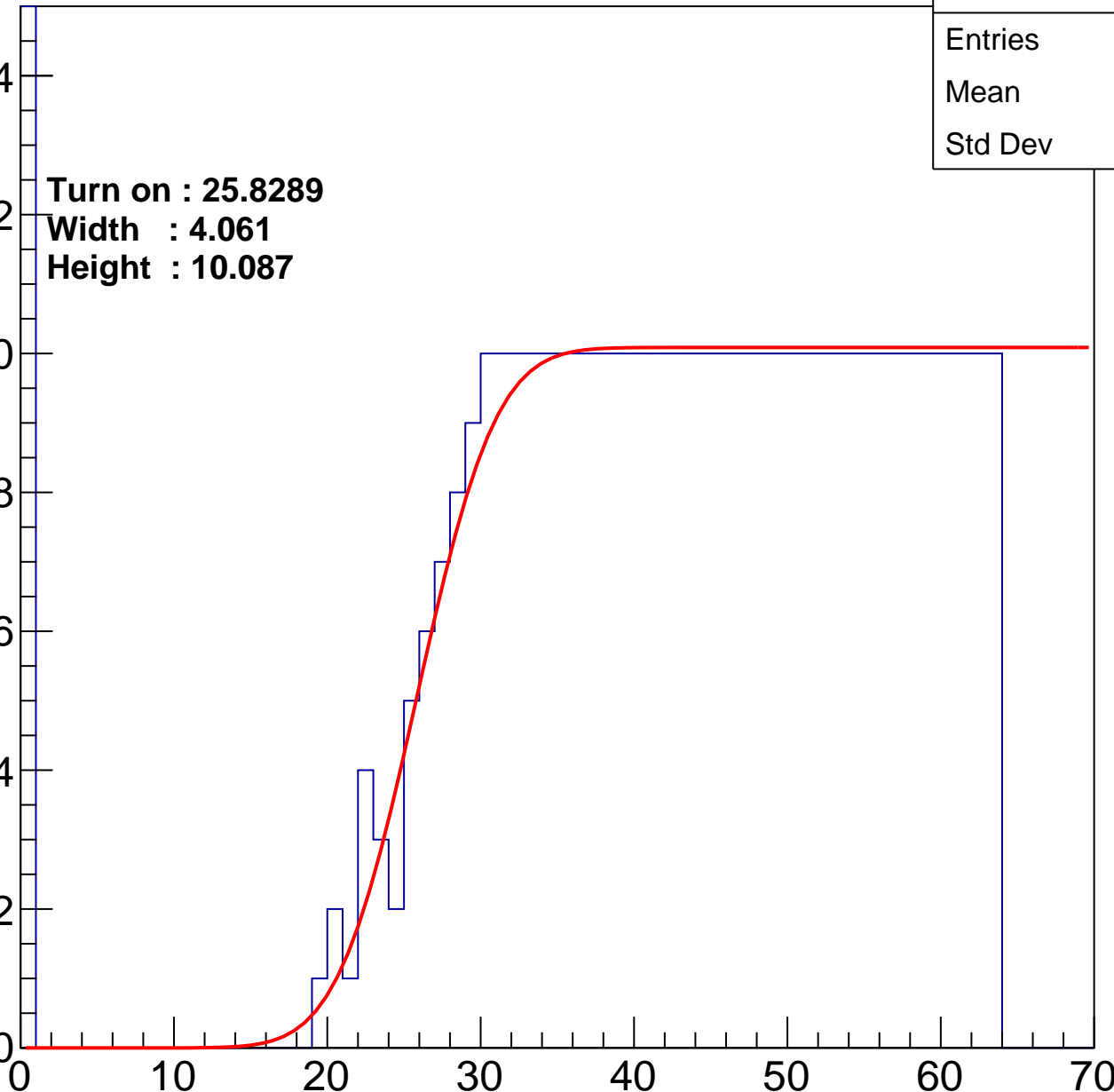
Width : 4.061

Height : 10.087

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch38

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	39.61
Std Dev	16.3

Turn on : 23.5170

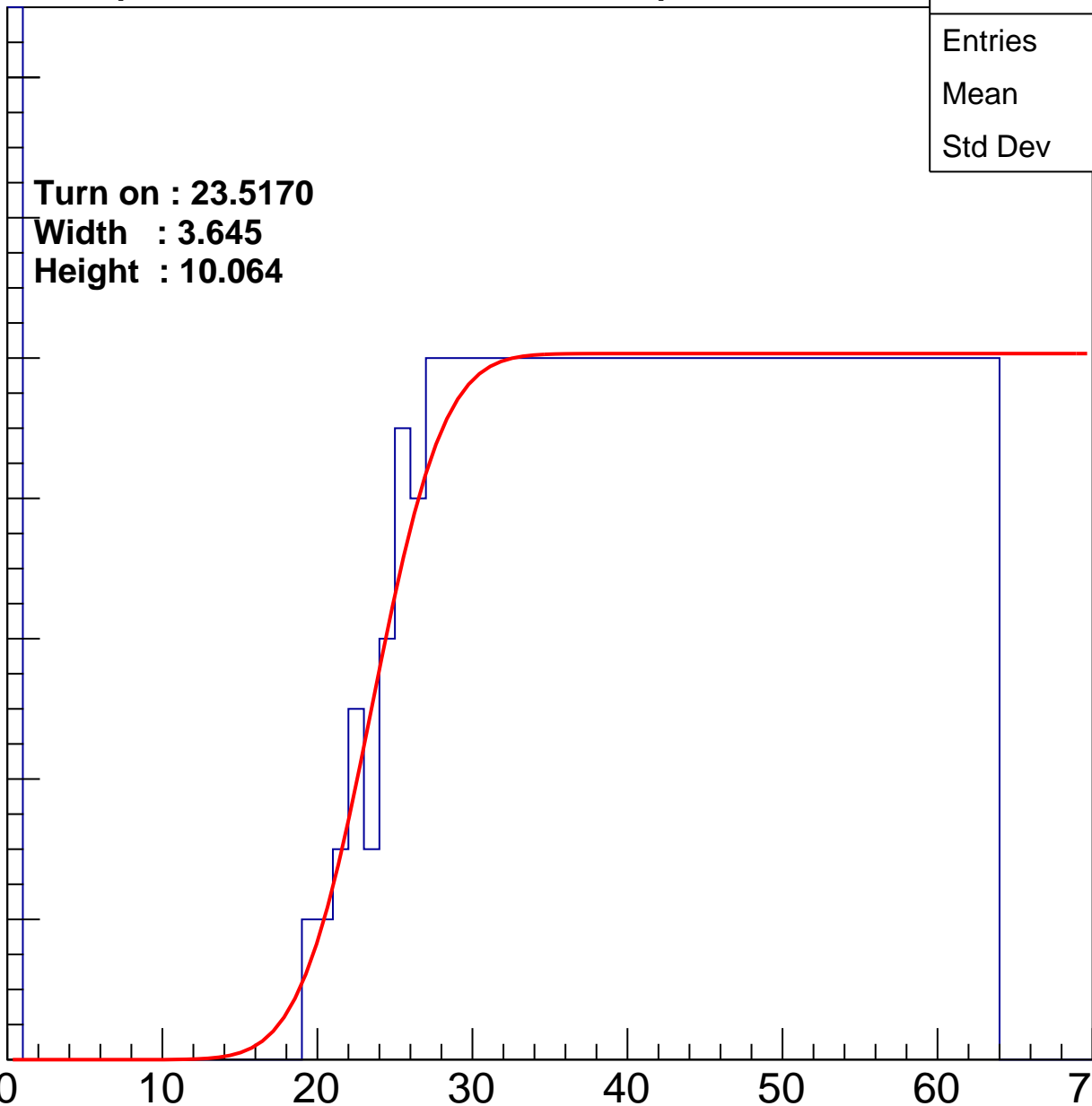
Width : 3.645

Height : 10.064

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch39

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	39.07
Std Dev	18.24

Turn on : 27.8189

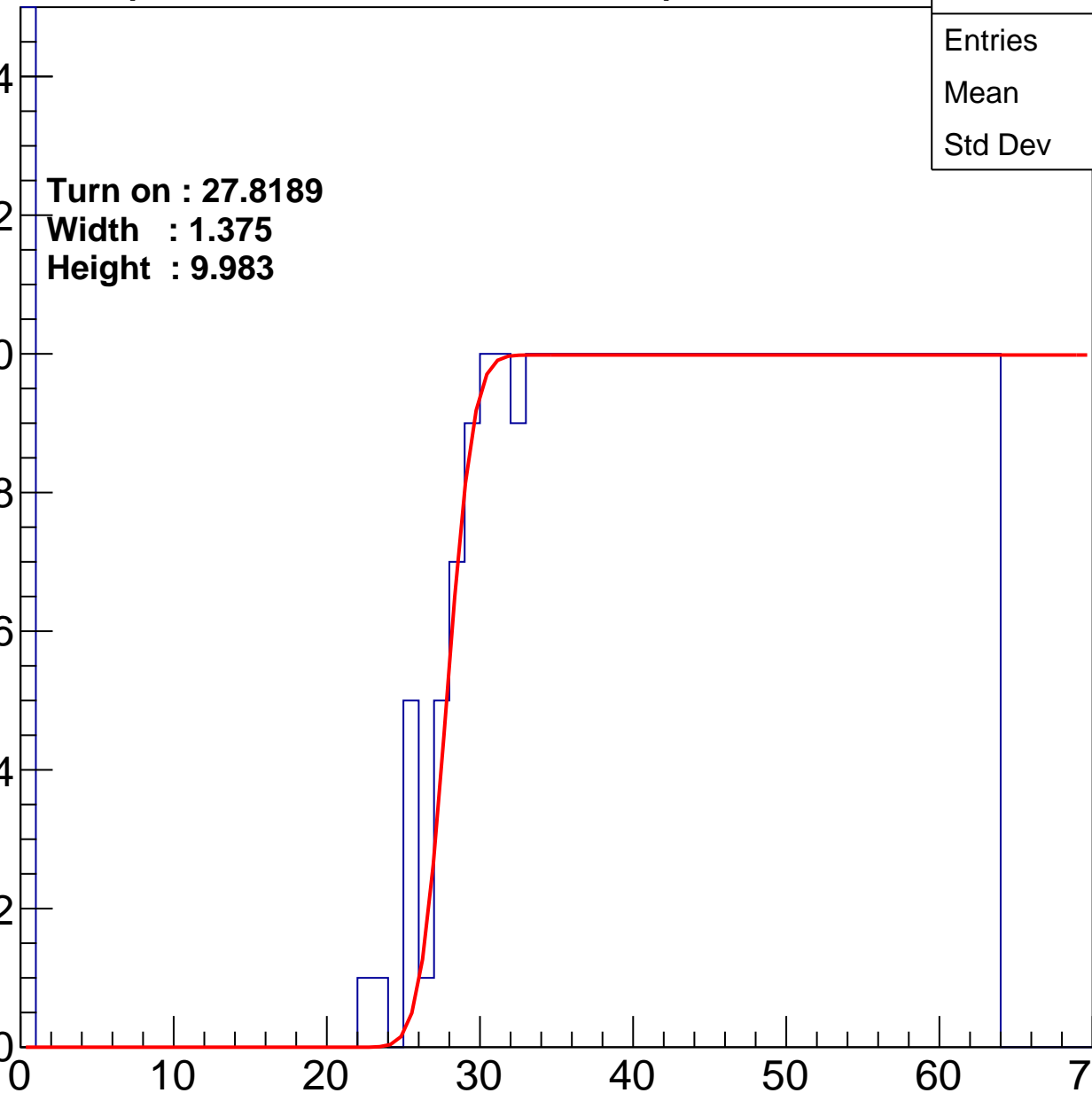
Width : 1.375

Height : 9.983

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch40

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	39.76
Std Dev	16.83

Turn on : 24.4814

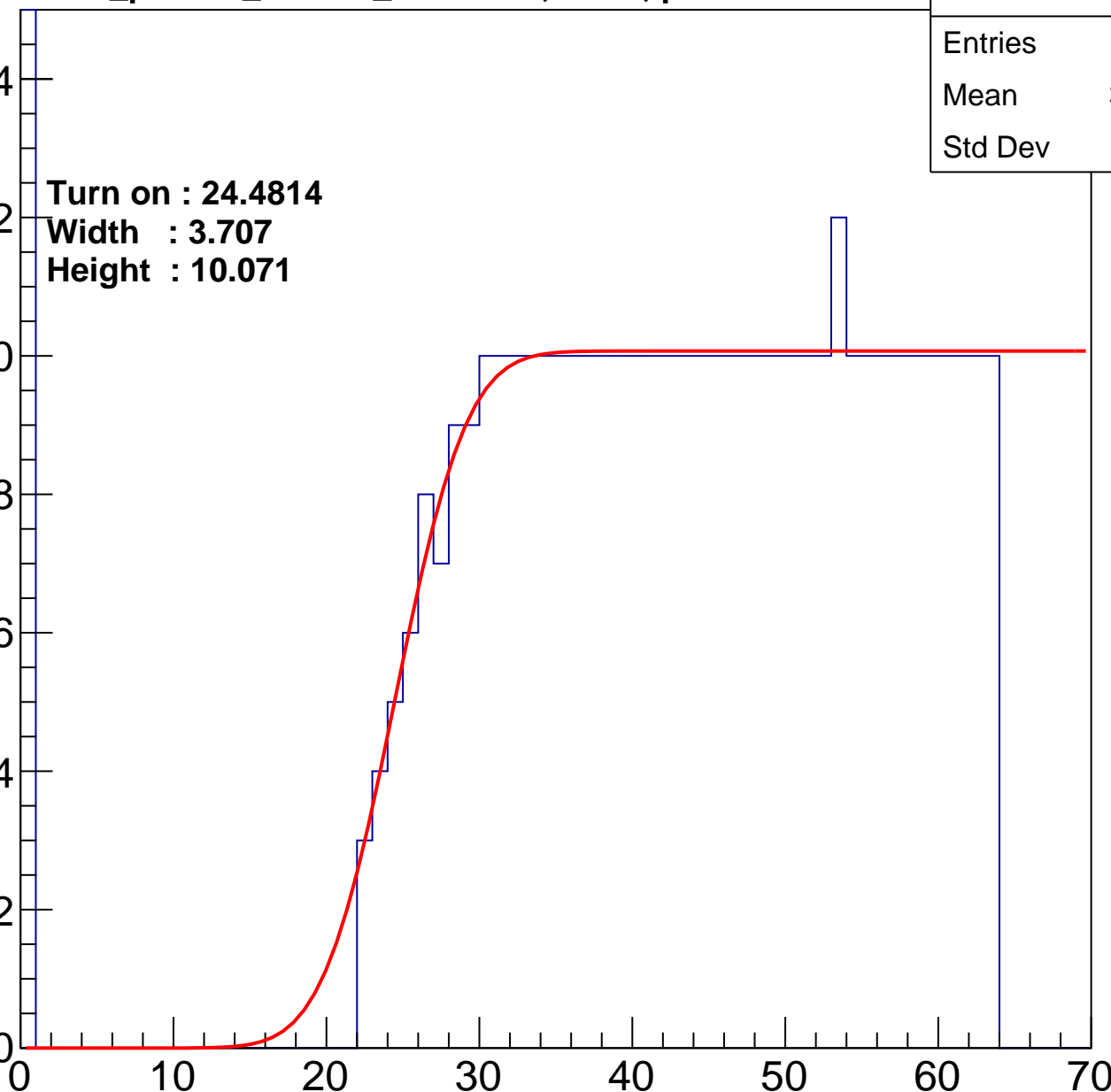
Width : 3.707

Height : 10.071

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch41

calib_packv5_041523_1651.root, FC#0, port C2

Entries	414
Mean	40.48
Std Dev	16.64

Turn on : 26.4494

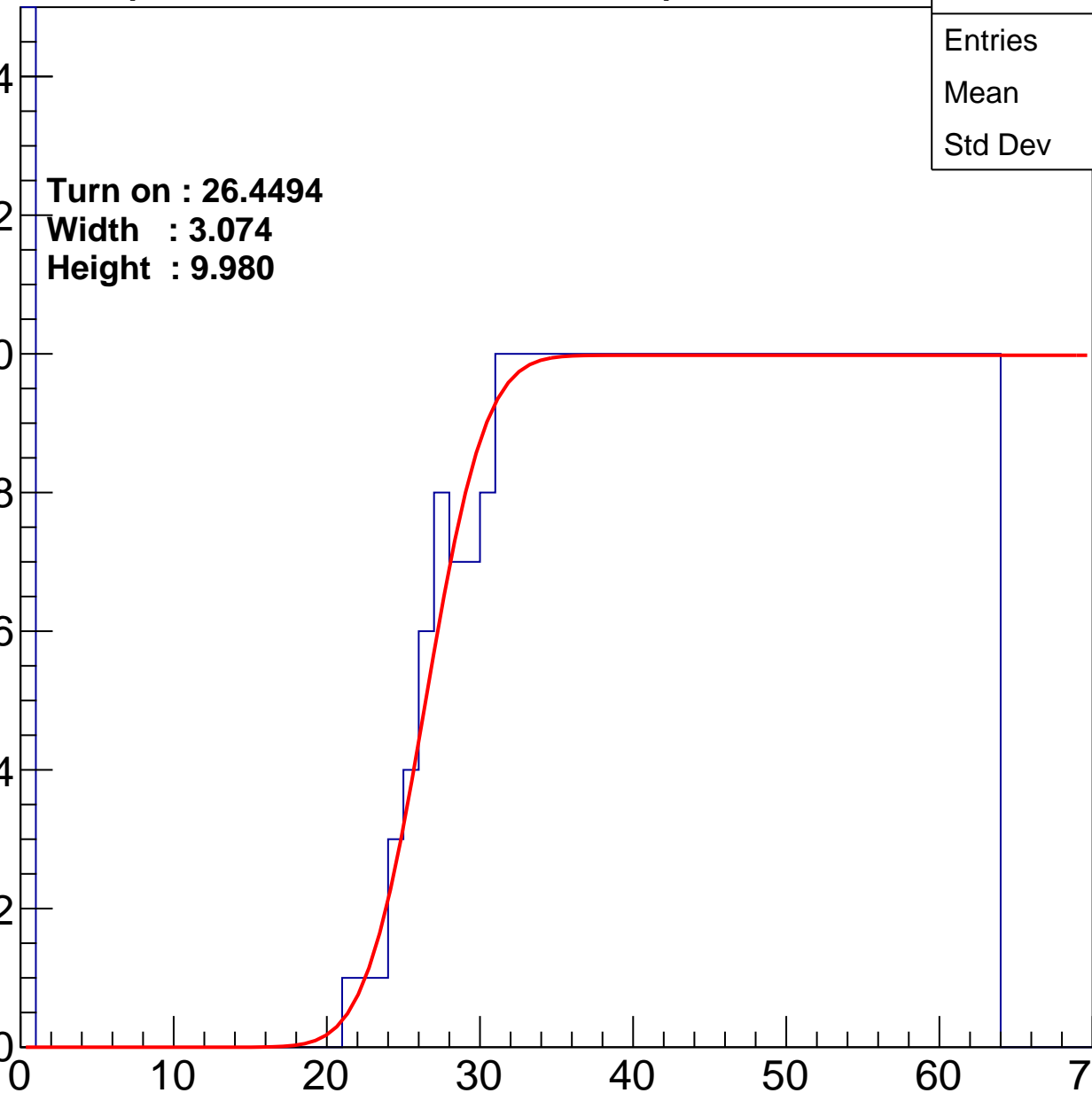
Width : 3.074

Height : 9.980

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch42

calib_packv5_041523_1651.root, FC#0, port C2

Entries	407
Mean	40.53
Std Dev	16.99

Turn on : 27.7177

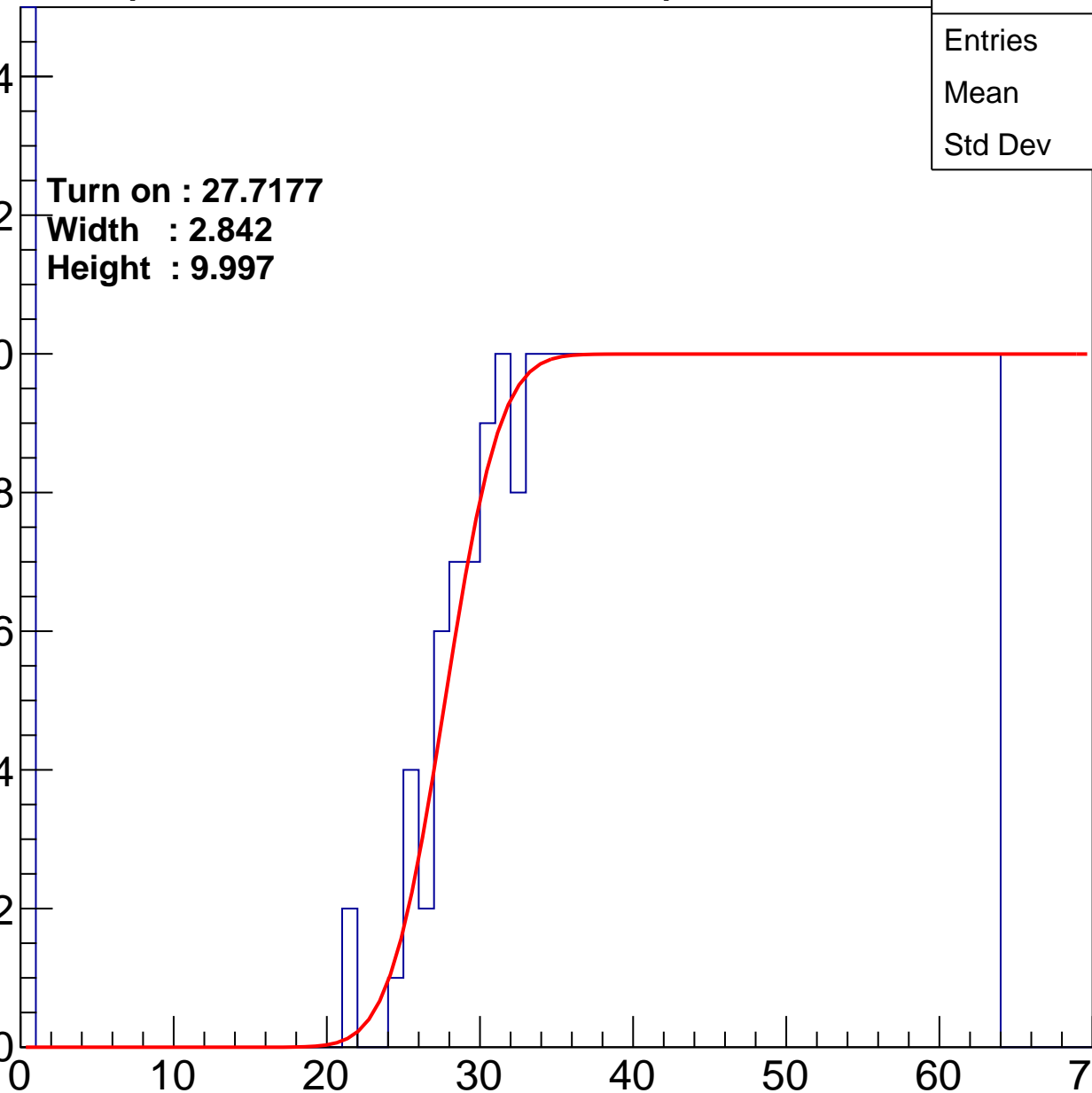
Width : 2.842

Height : 9.997

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch43

calib_packv5_041523_1651.root, FC#0, port C2

Entries	427
Mean	39.29
Std Dev	17.73

Turn on : 26.7756

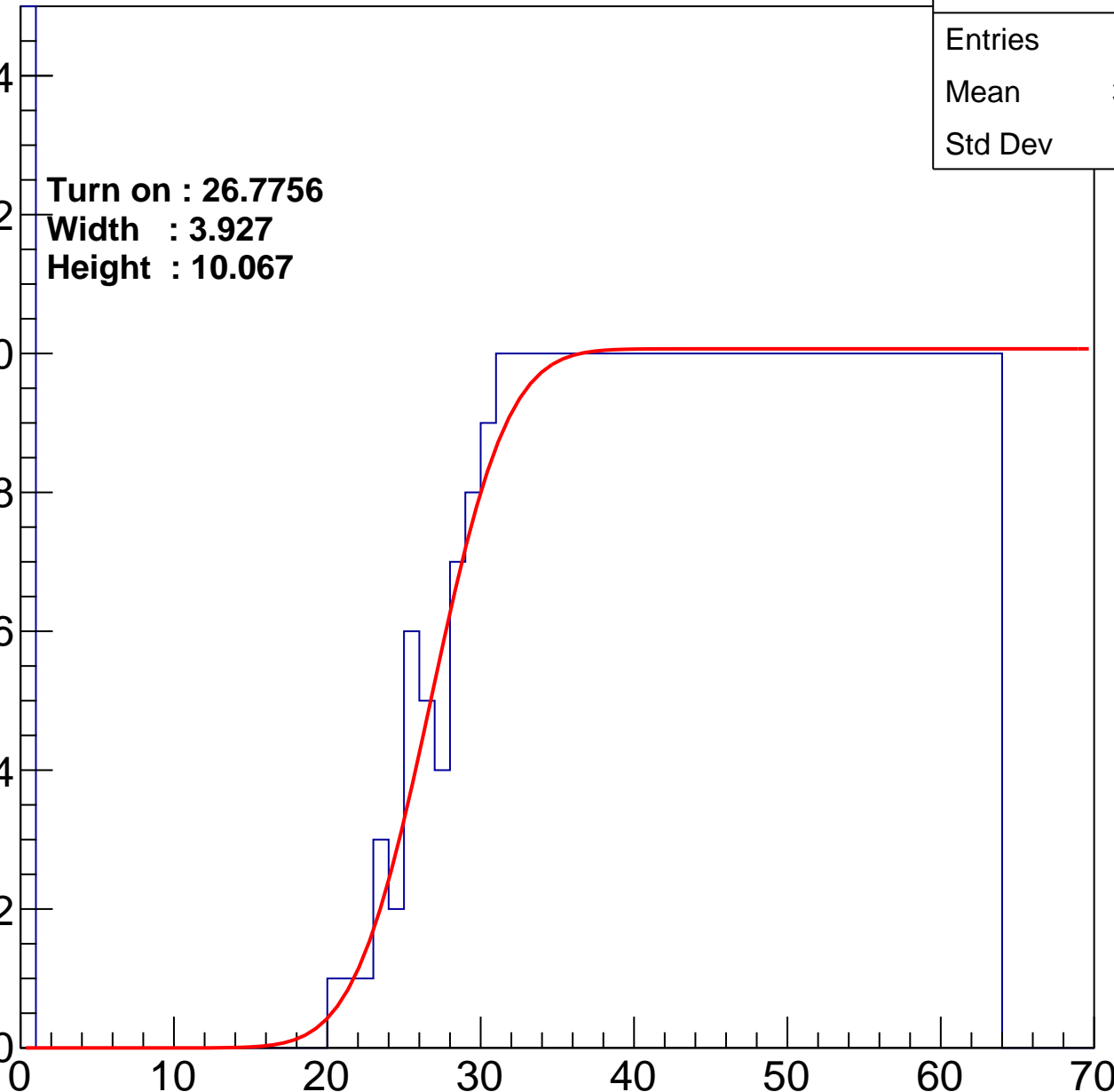
Width : 3.927

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch44

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	38.94
Std Dev	17.4

Turn on : 24.5668

Width : 2.059

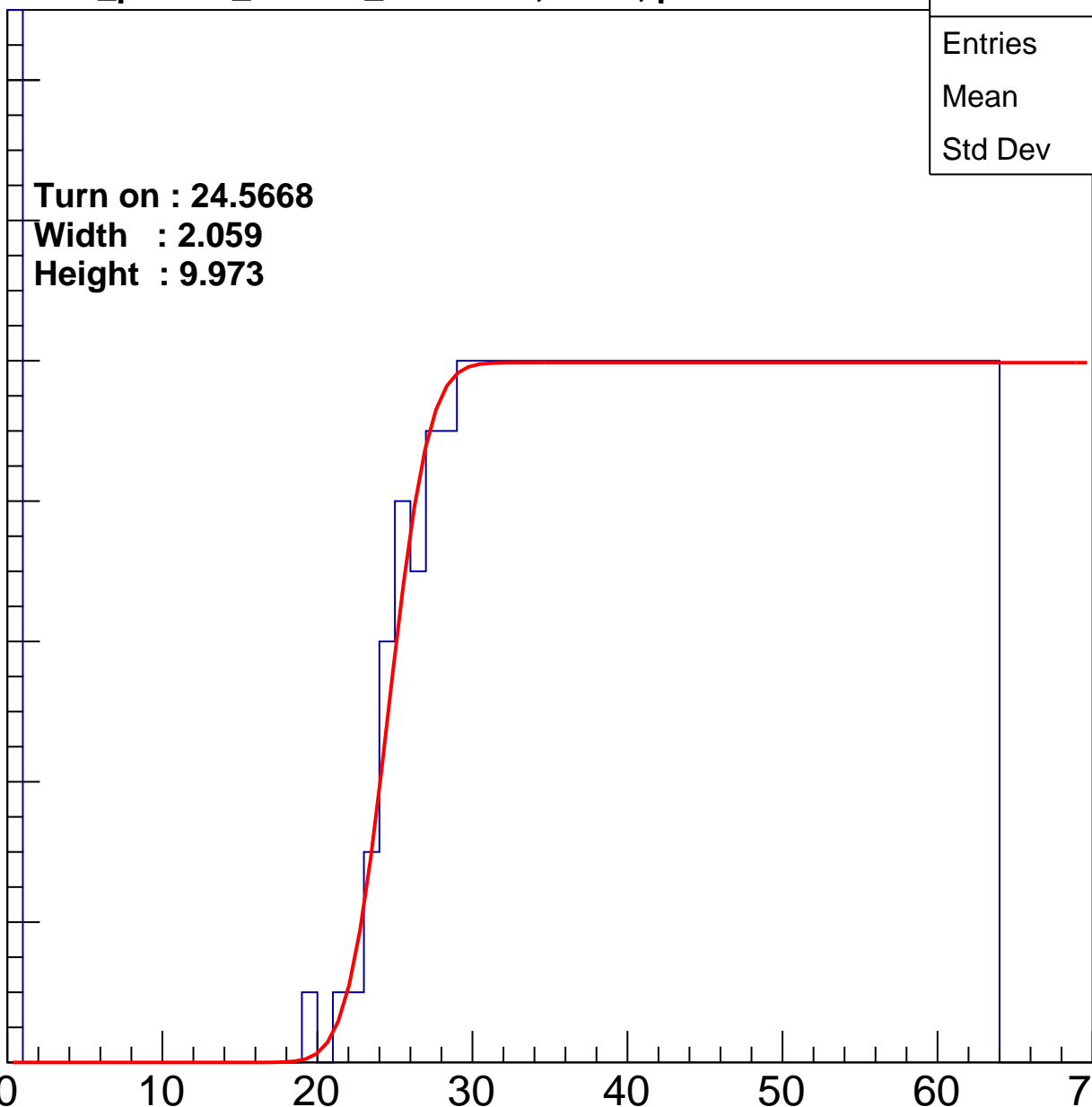
Height : 9.973

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U7-ch45

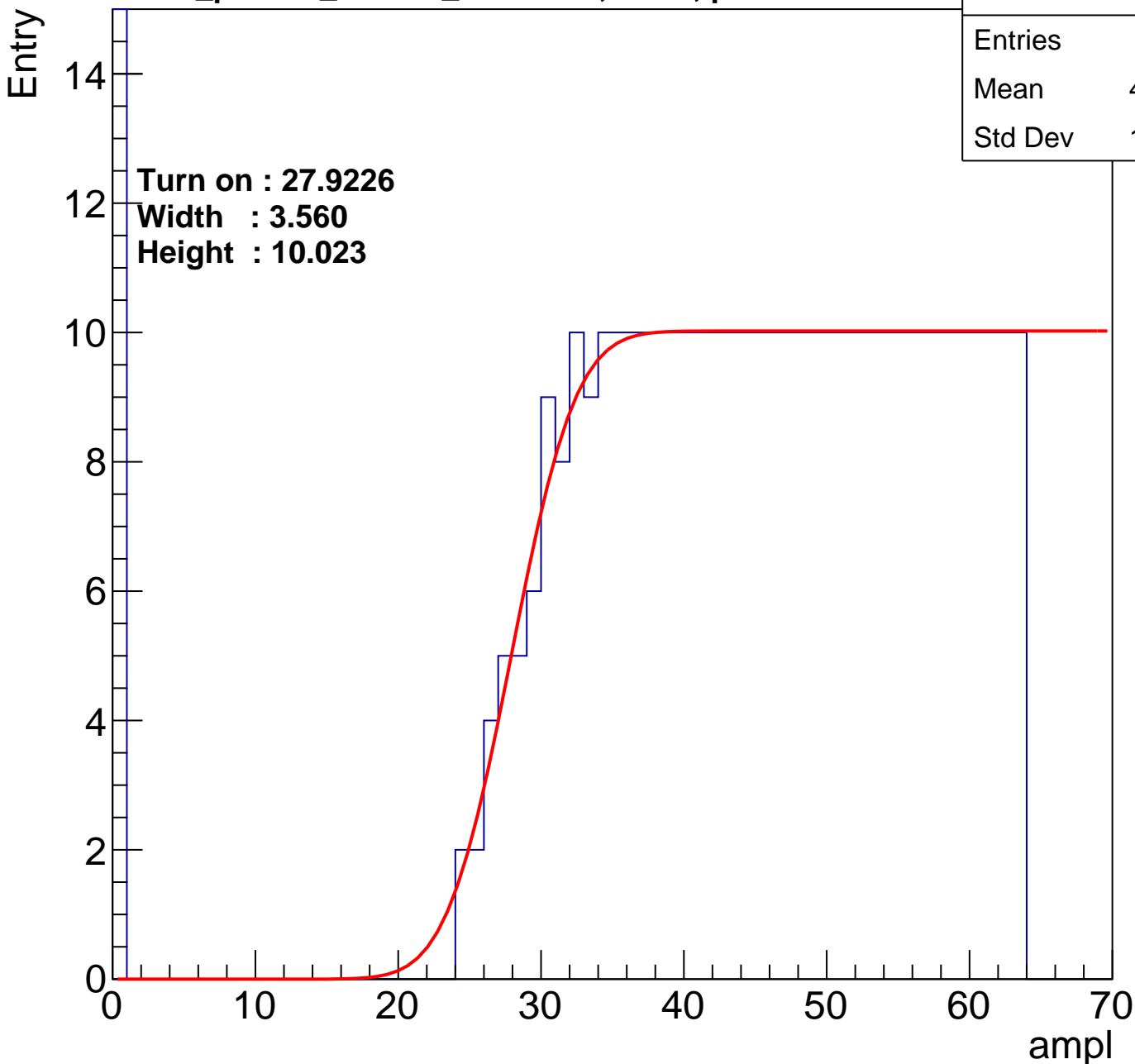
calib_packv5_041523_1651.root, FC#0, port C2

Entries	399
Mean	40.94
Std Dev	16.82

Turn on : 27.9226

Width : 3.560

Height : 10.023



B1L103S, U7-ch46

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	39.39
Std Dev	16.95

Turn on : 25.0652

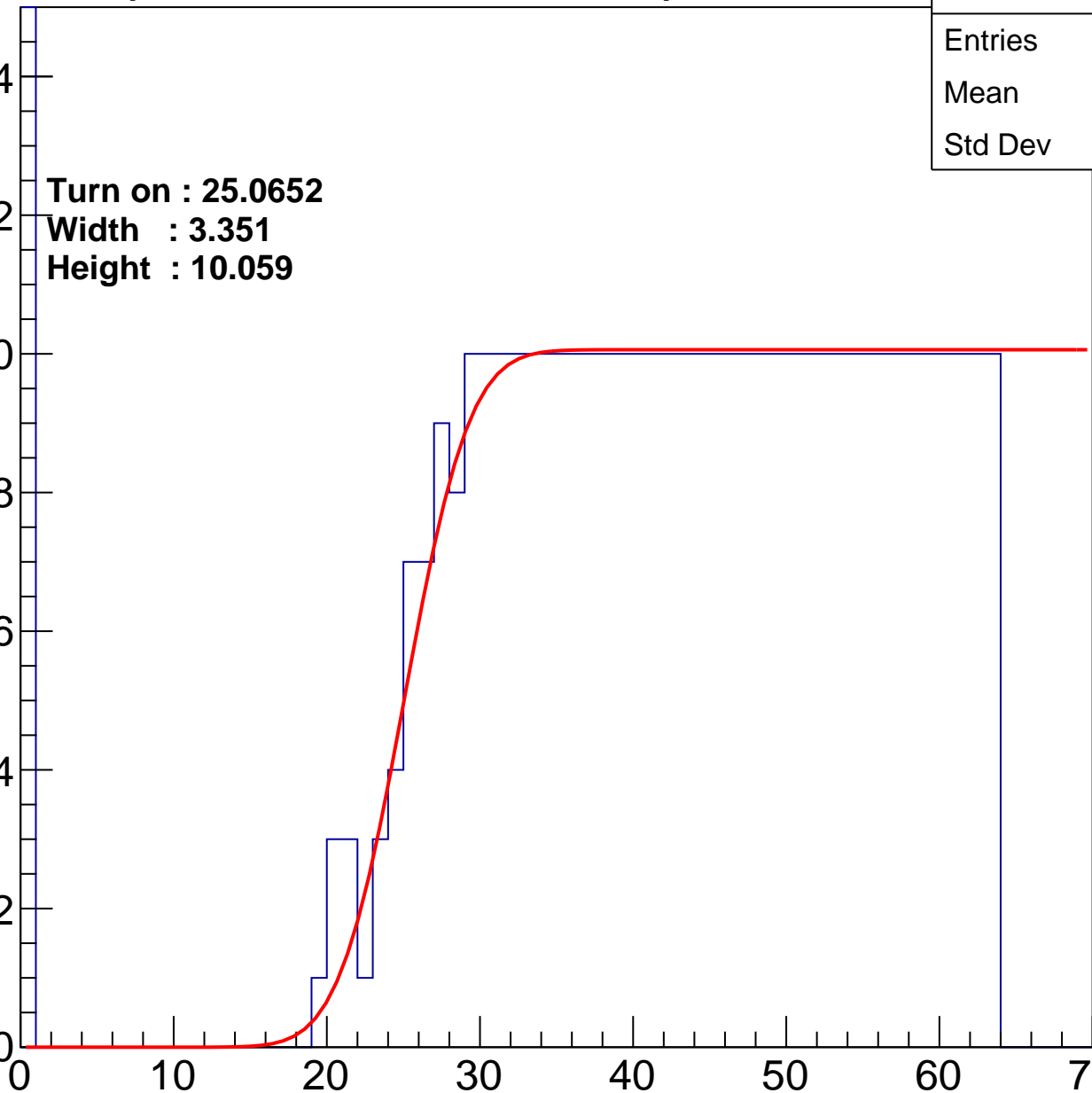
Width : 3.351

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch47

calib_packv5_041523_1651.root, FC#0, port C2

Entries	408
Mean	40.33
Std Dev	17.27

Turn on : 27.8981

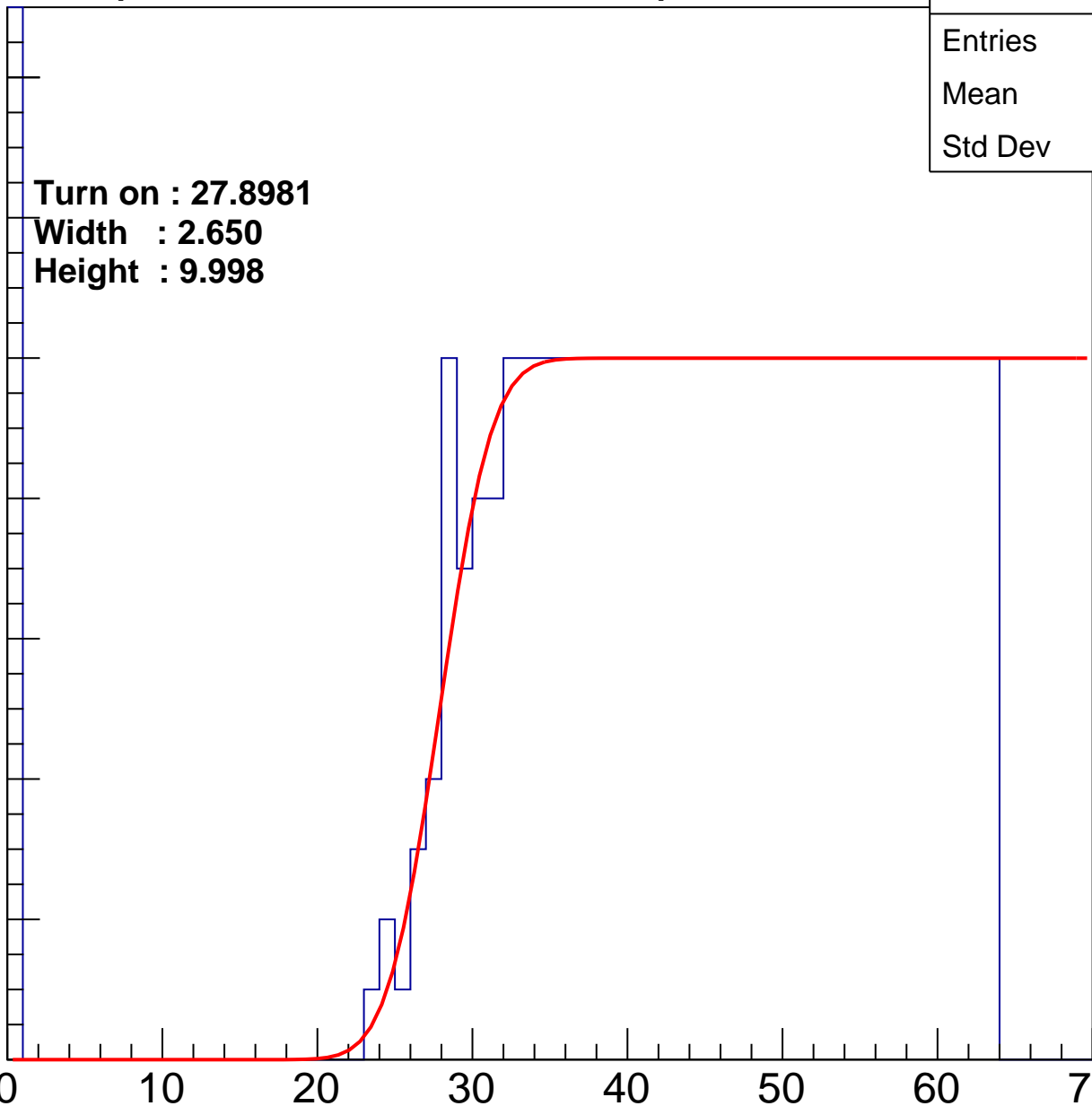
Width : 2.650

Height : 9.998

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch48

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	39.42
Std Dev	17

Turn on : 24.6772

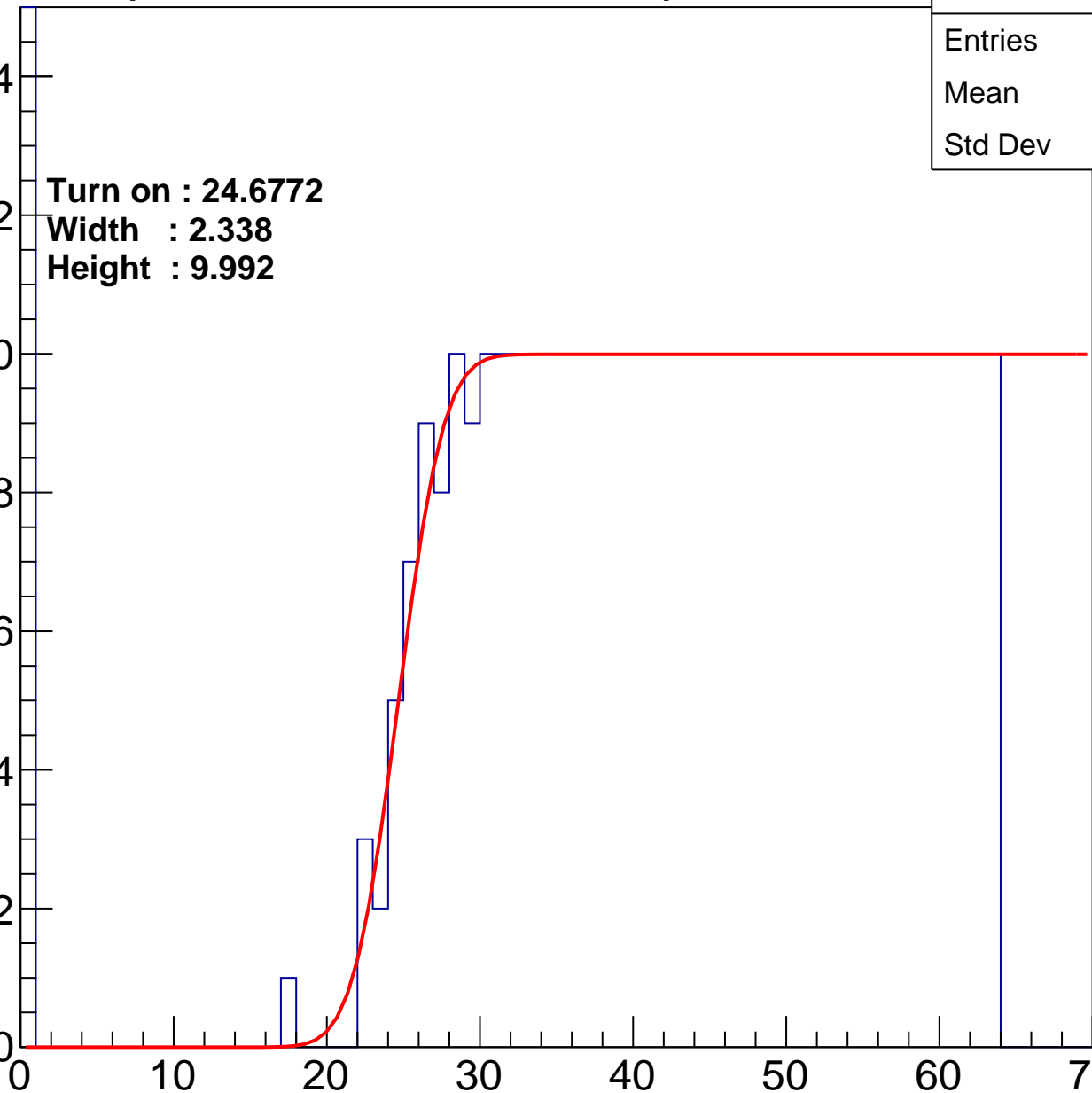
Width : 2.338

Height : 9.992

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch49

calib_packv5_041523_1651.root, FC#0, port C2

Entries	405
Mean	41.1
Std Dev	16.2

Turn on : 27.4735

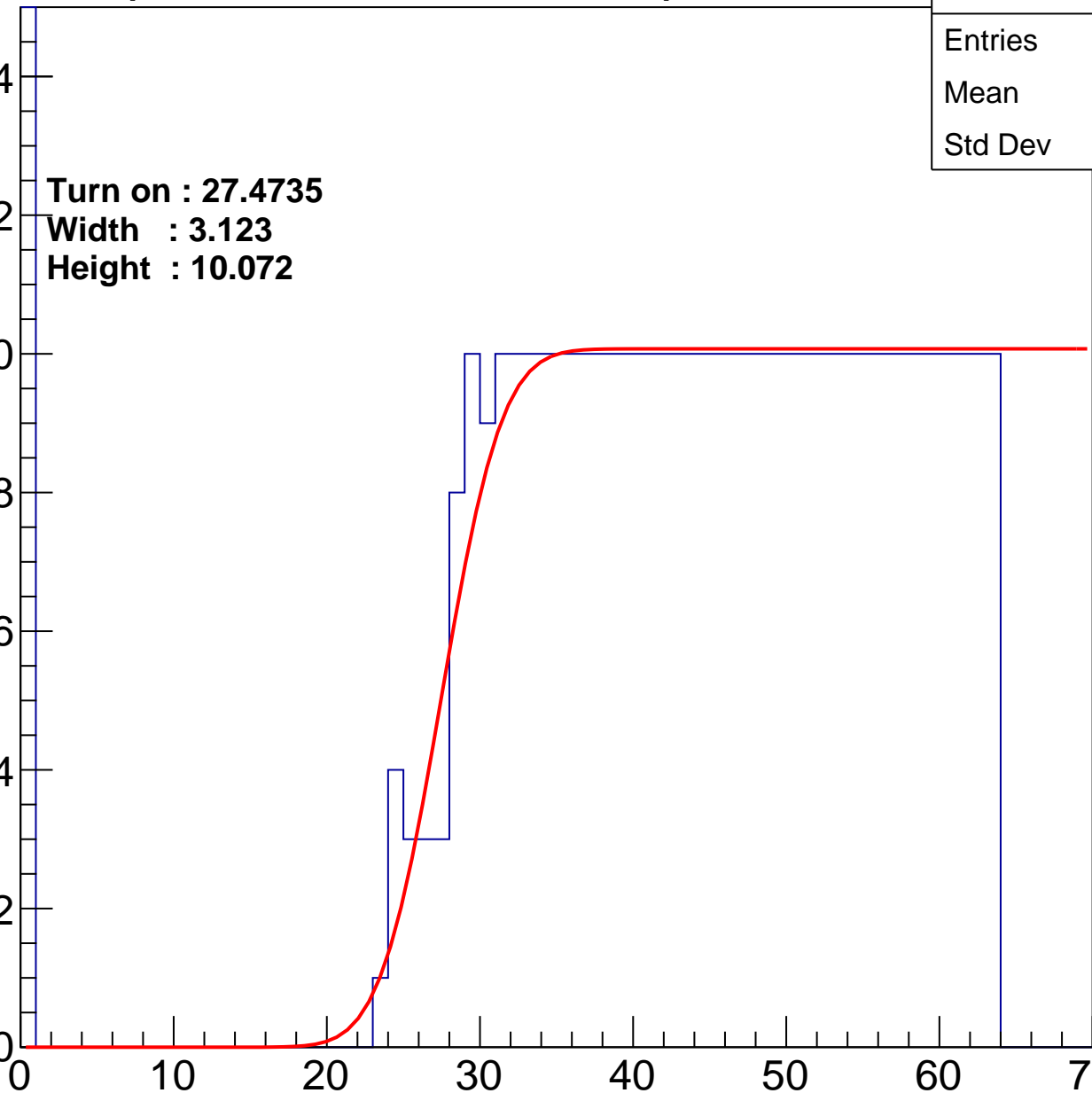
Width : 3.123

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch50

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	39.56
Std Dev	17.74

Turn on : 26.7794

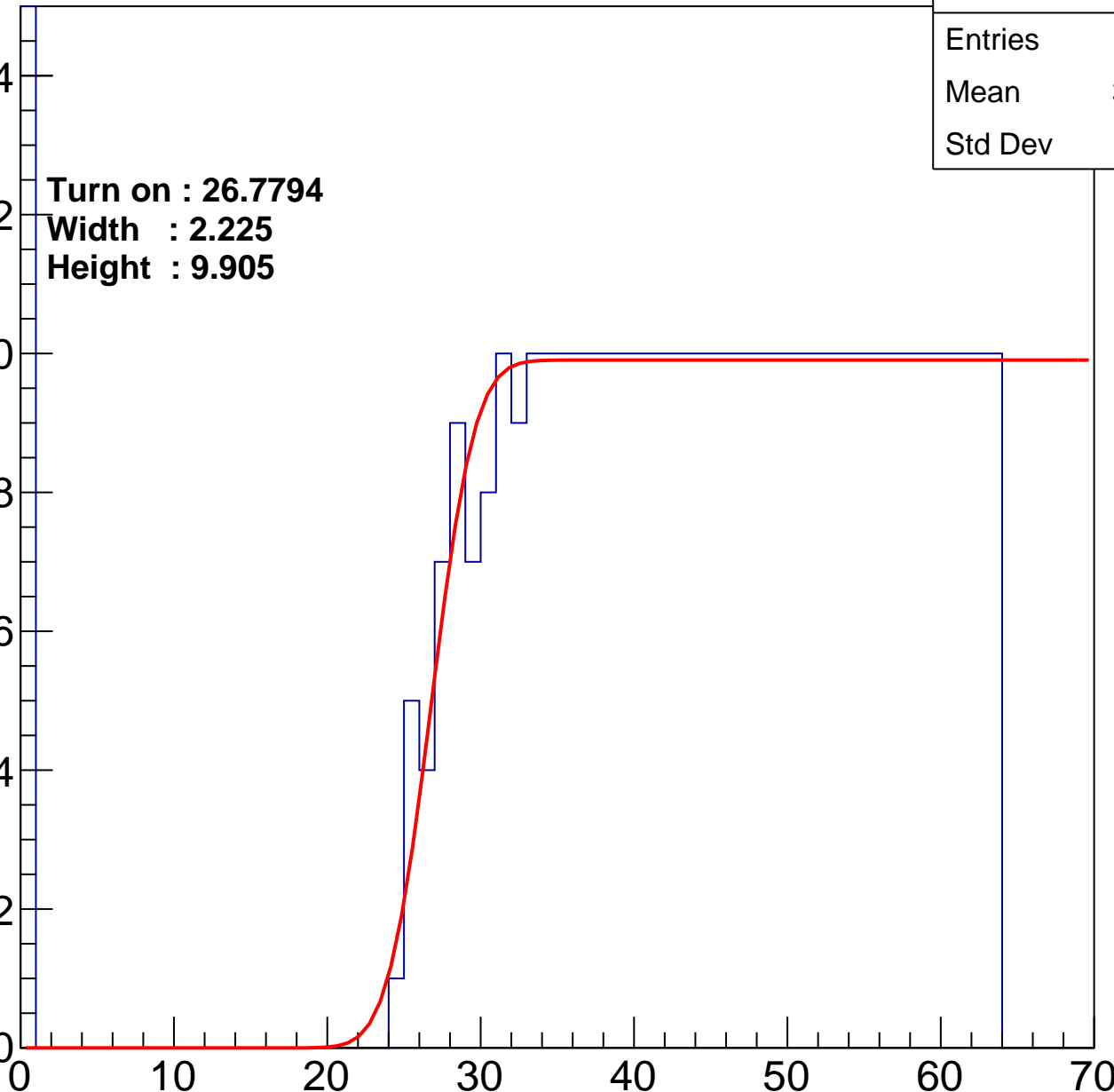
Width : 2.225

Height : 9.905

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch51

calib_packv5_041523_1651.root, FC#0, port C2

Entries	406
Mean	40.97
Std Dev	16.34

Turn on : 27.5112

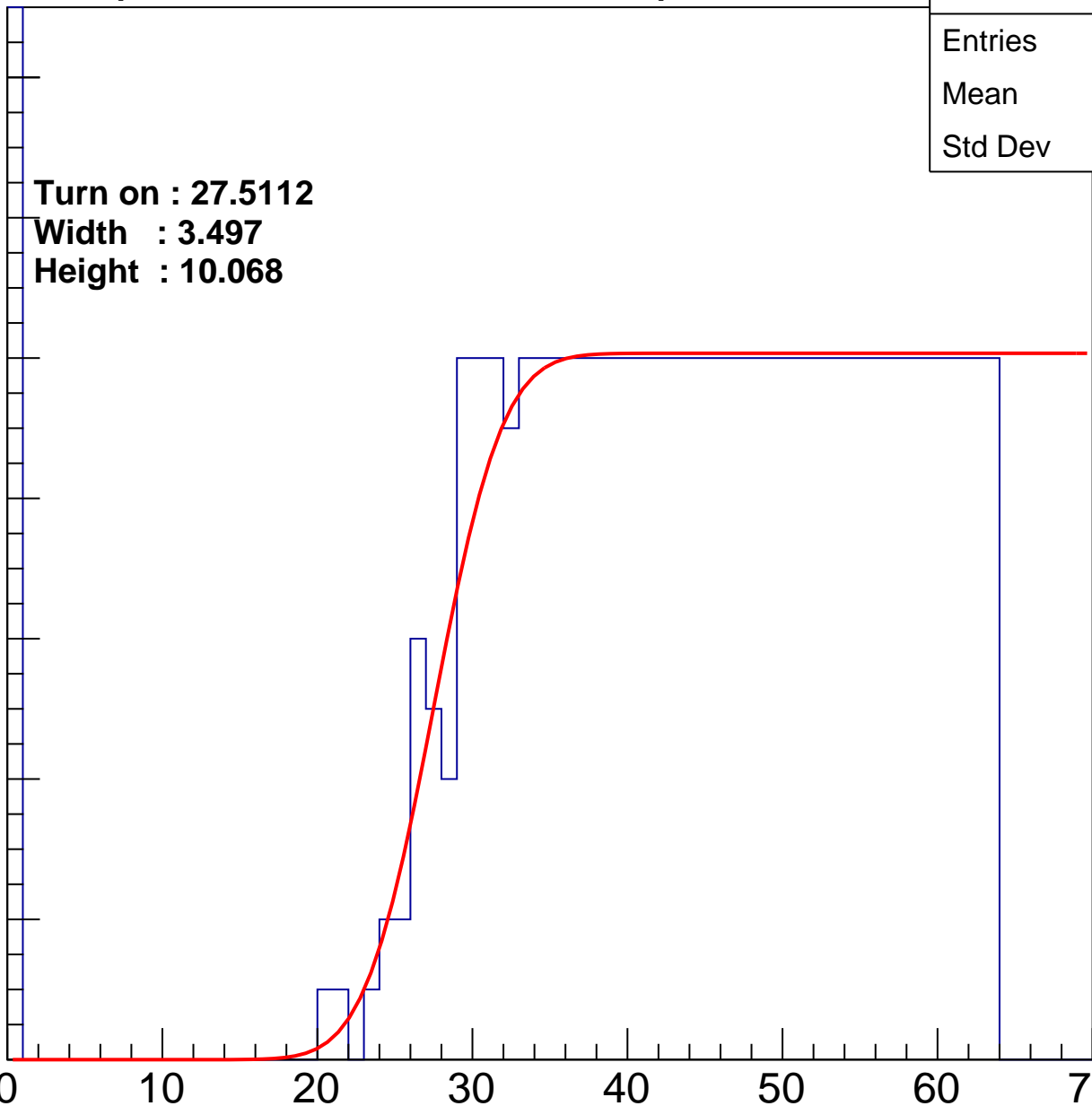
Width : 3.497

Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch52

calib_packv5_041523_1651.root, FC#0, port C2

Entries	479
Mean	37.02
Std Dev	18.31

Turn on : 22.4081

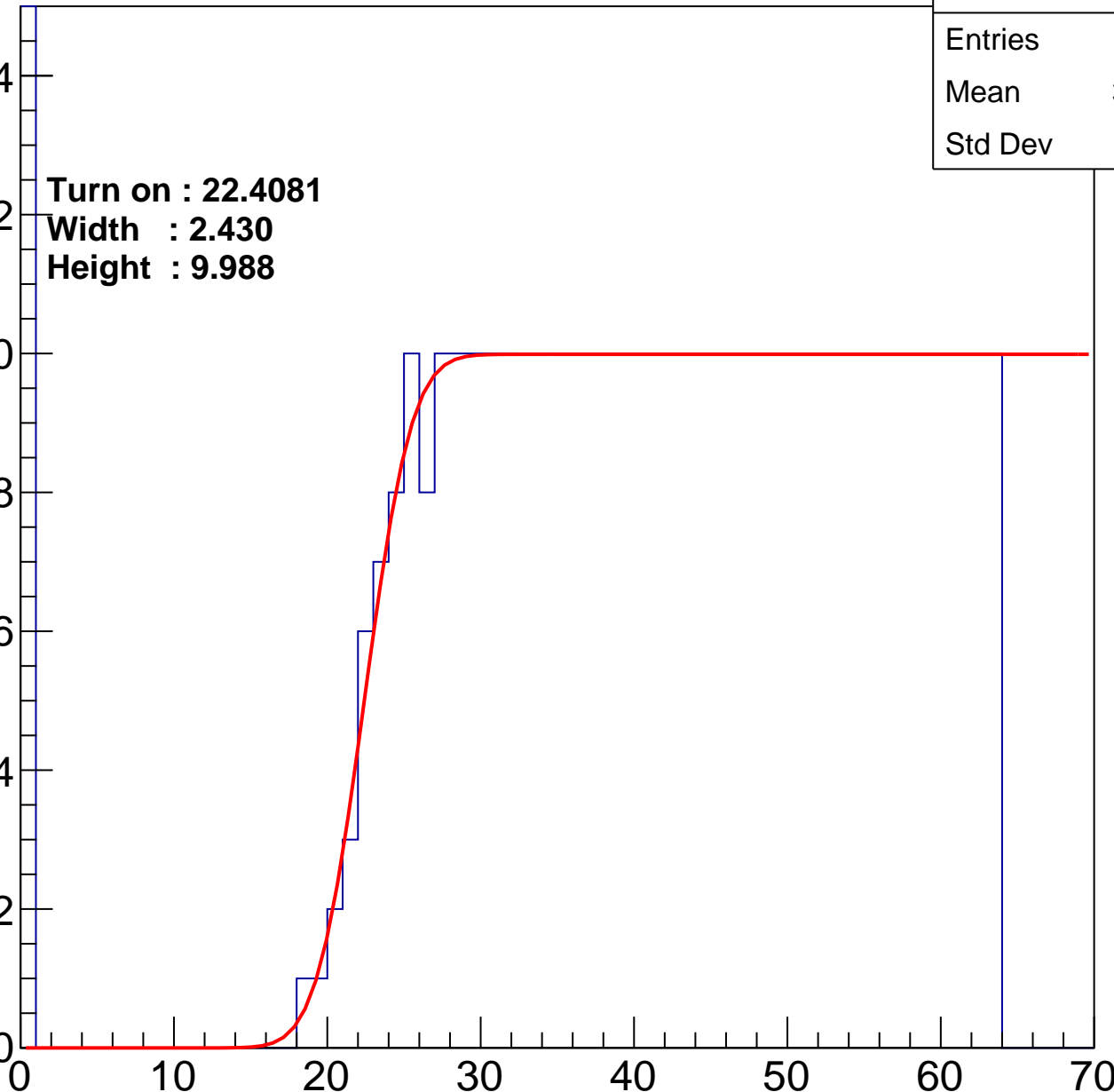
Width : 2.430

Height : 9.988

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch53

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	38.71
Std Dev	17.88

Turn on : 25.8101

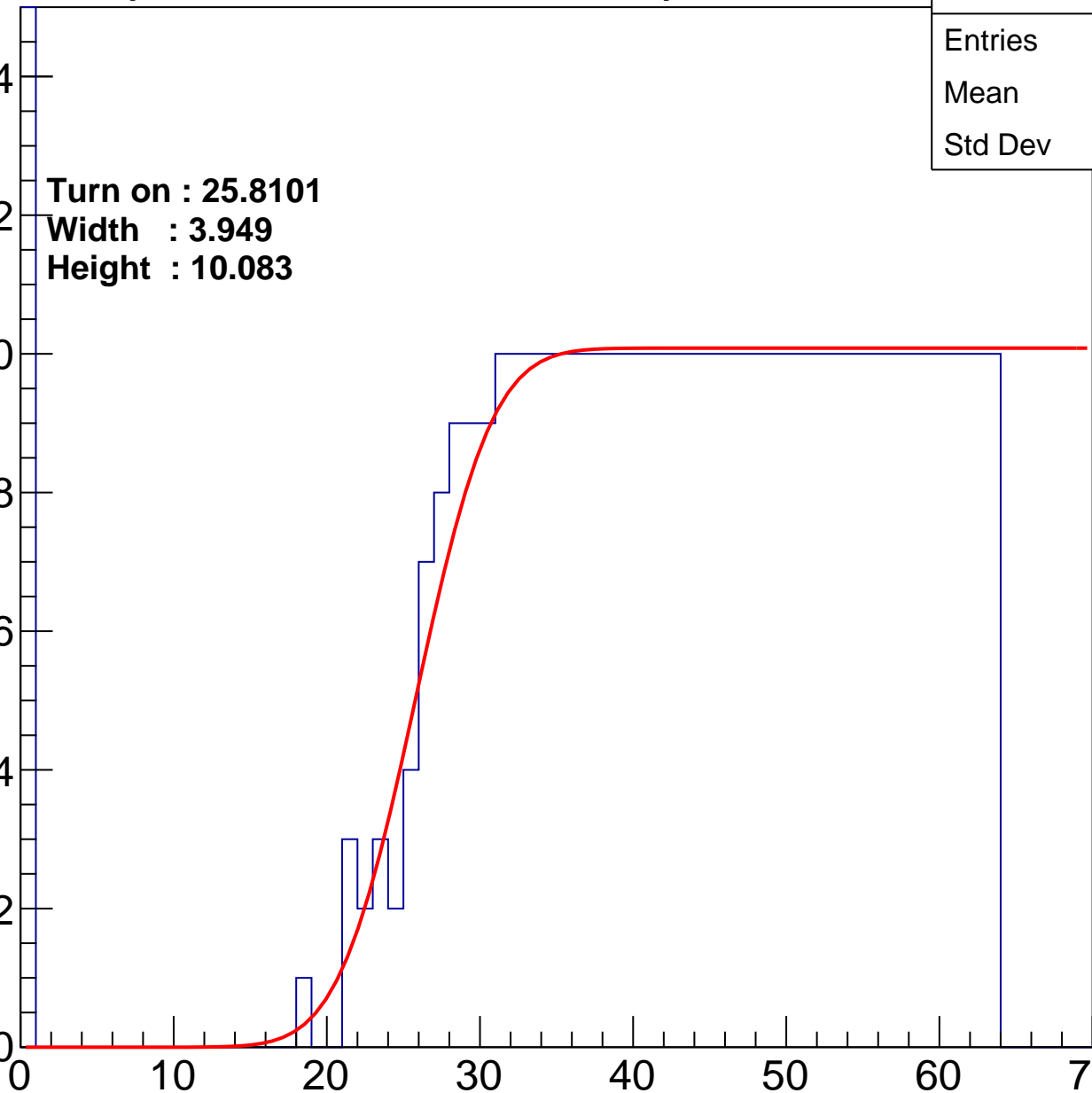
Width : 3.949

Height : 10.083

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch54

calib_packv5_041523_1651.root, FC#0, port C2

Entries	453
Mean	38.22
Std Dev	17.89

Turn on : 24.4748

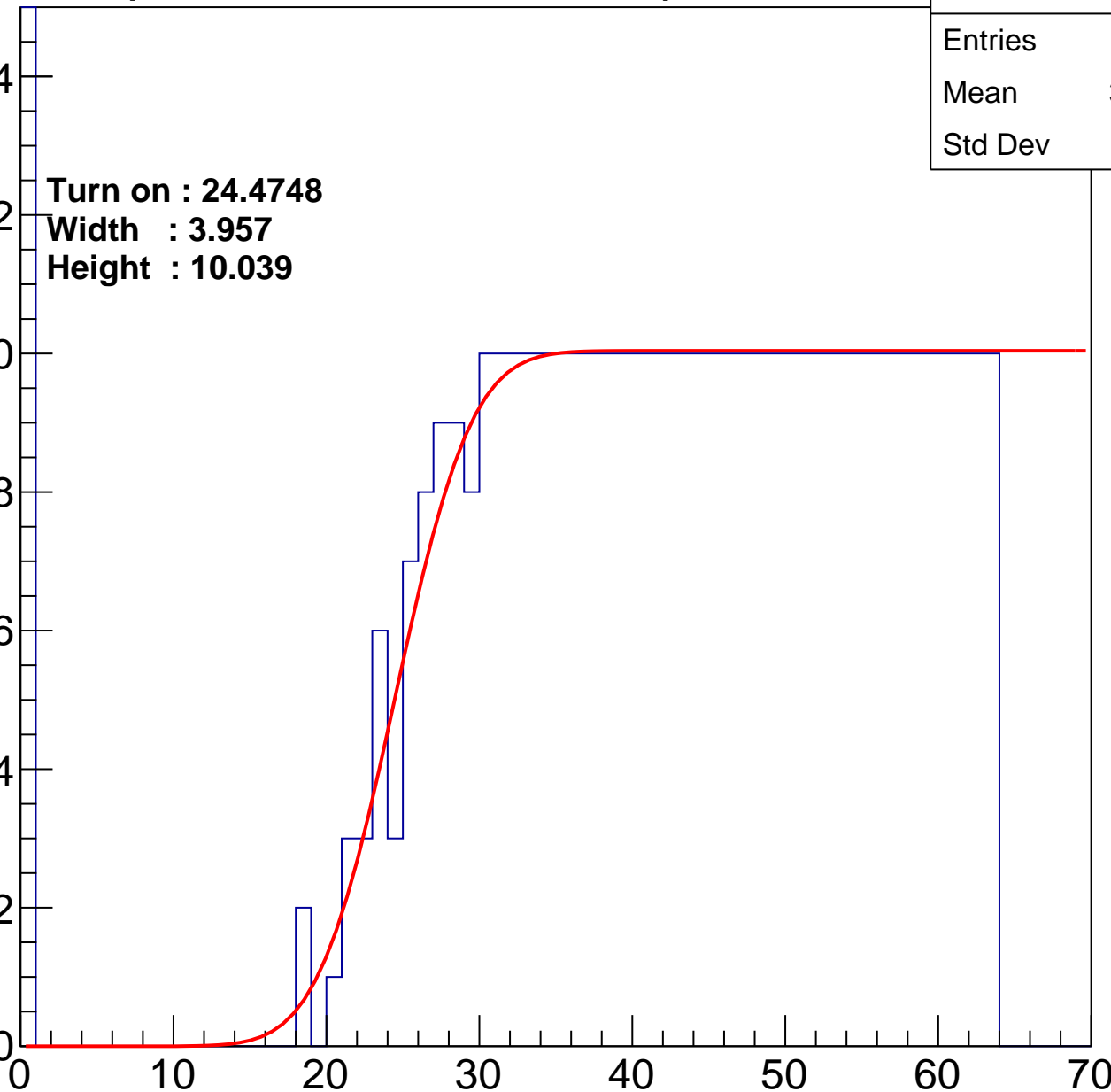
Width : 3.957

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch55

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	38.69
Std Dev	17.94

Turn on : 25.6998

Width : 2.465

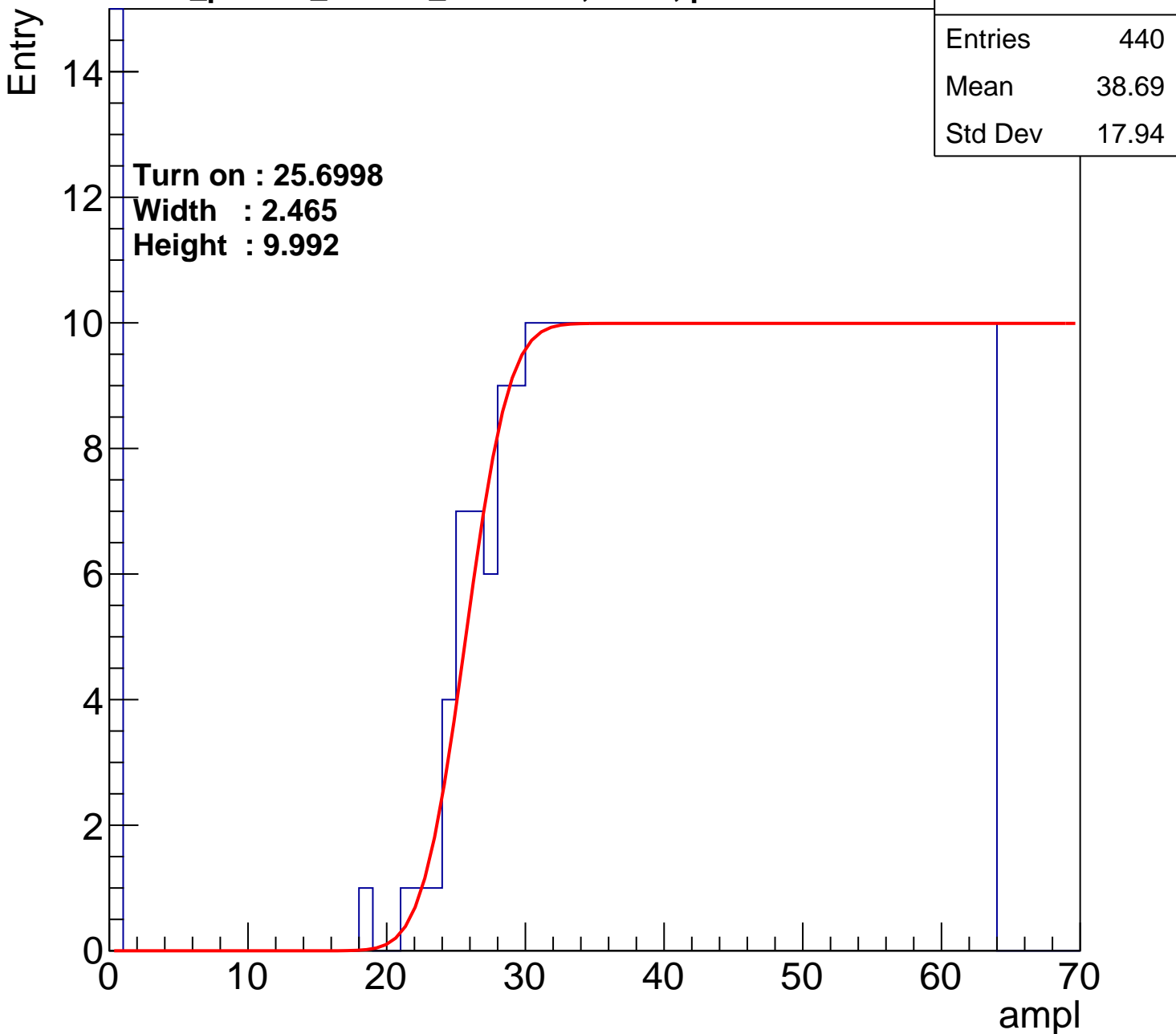
Height : 9.992

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U7-ch56

calib_packv5_041523_1651.root, FC#0, port C2

Entries	448
Mean	38.92
Std Dev	17.11

Turn on : 24.3096

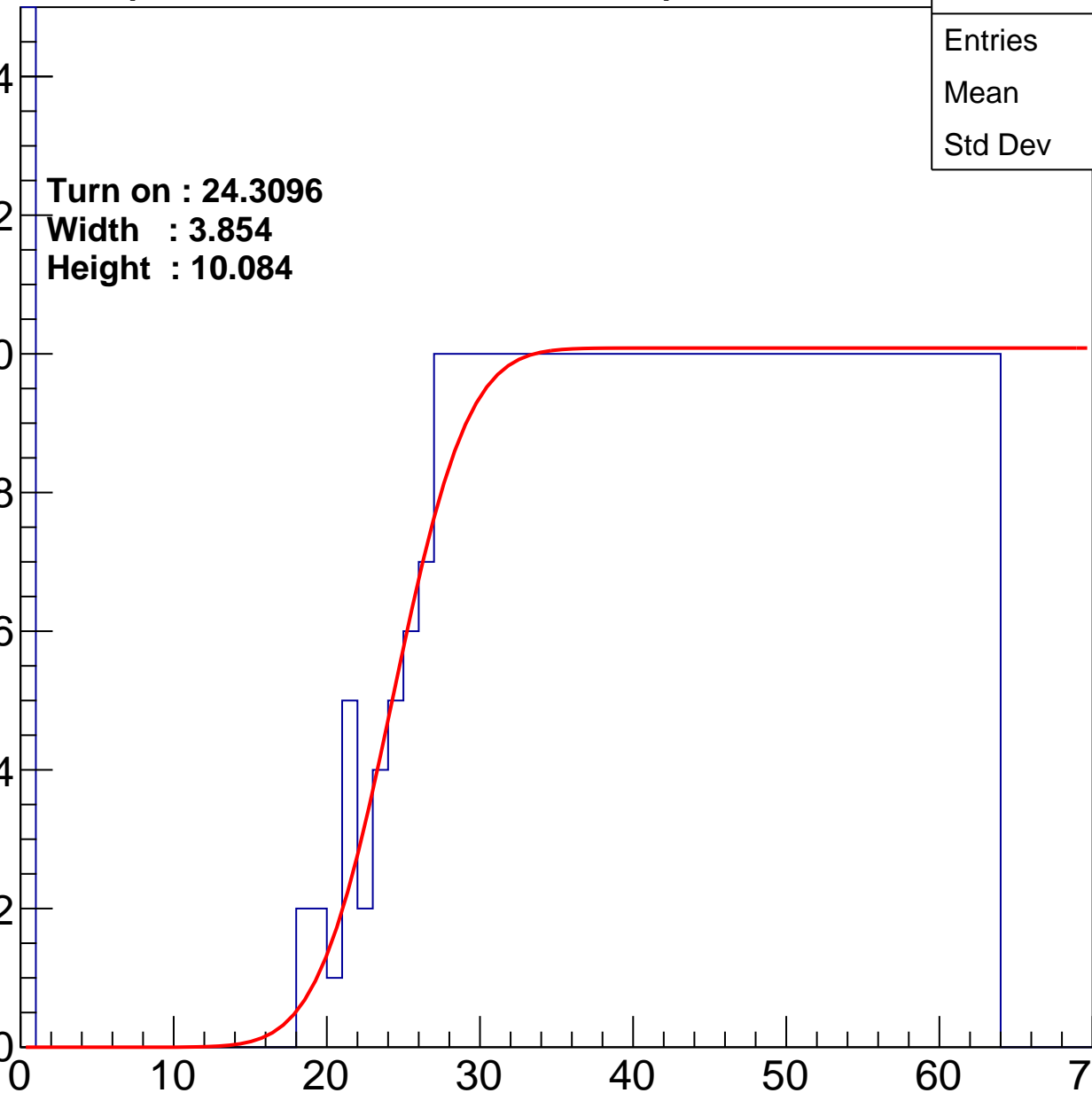
Width : 3.854

Height : 10.084

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch57

calib_packv5_041523_1651.root, FC#0, port C2

Entries	406
Mean	40.4
Std Dev	17.22

Turn on : 27.8022

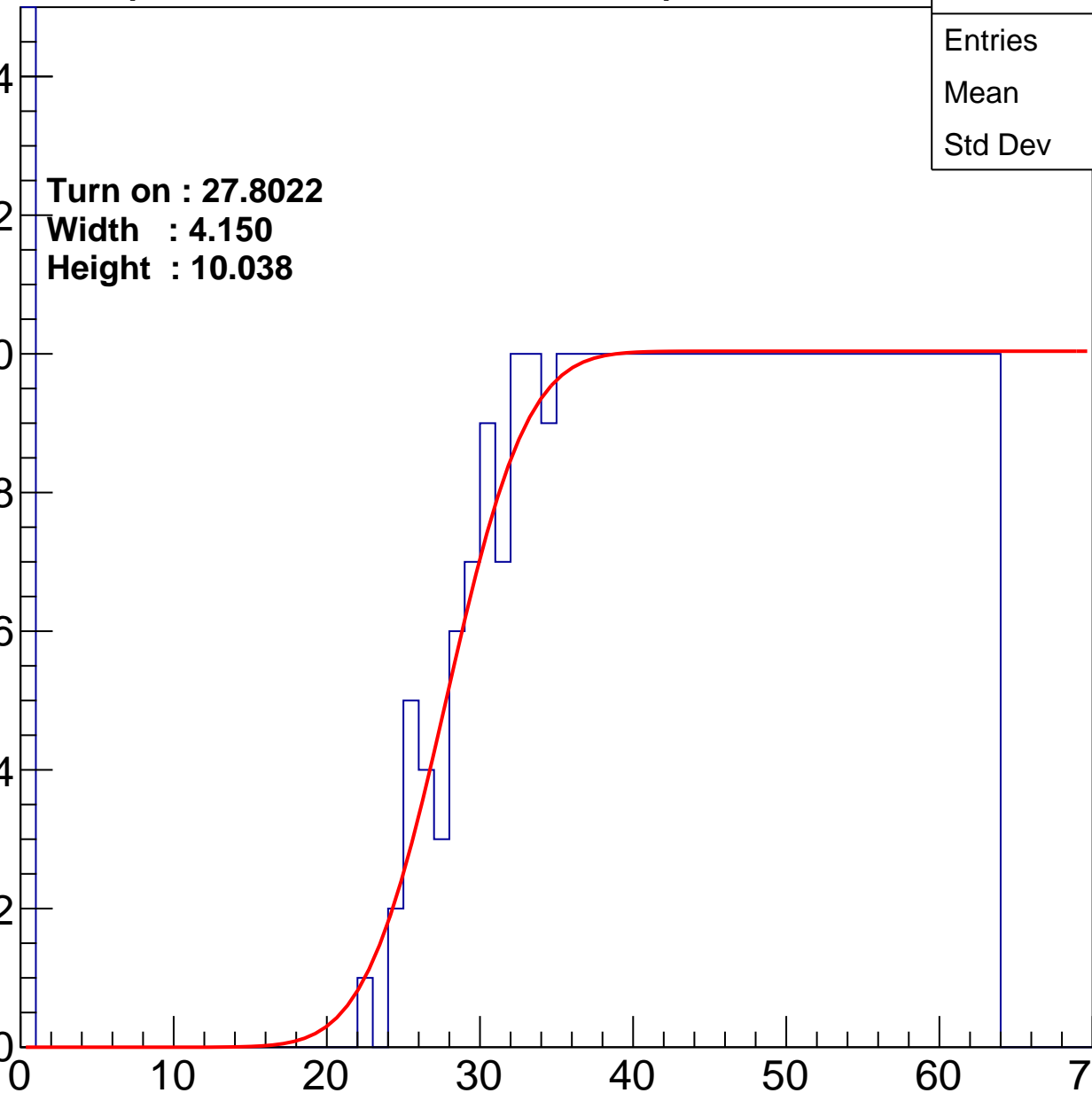
Width : 4.150

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch58

calib_packv5_041523_1651.root, FC#0, port C2

Entries	414
Mean	40.72
Std Dev	16.23

Turn on : 26.5235

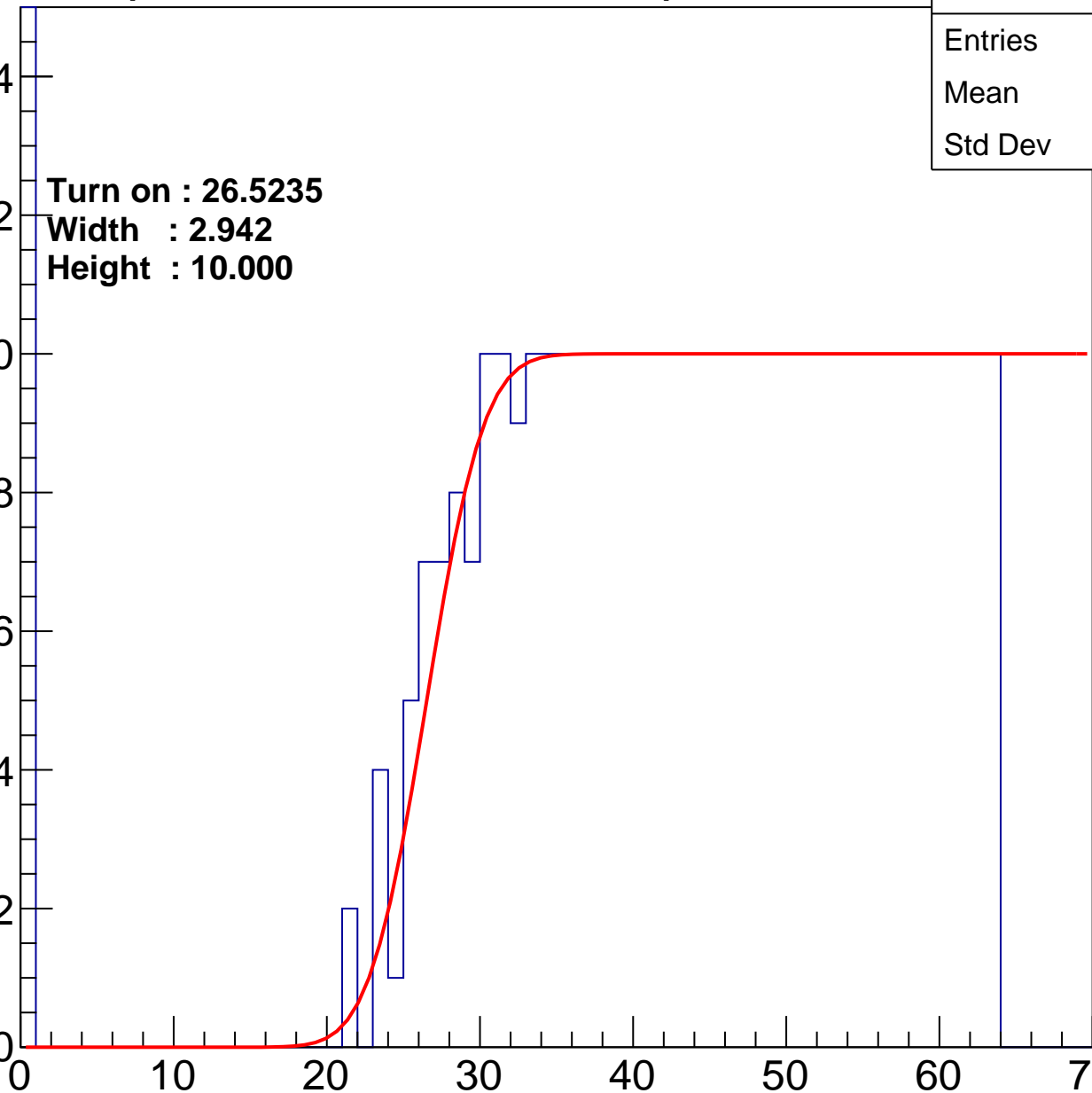
Width : 2.942

Height : 10.000

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch59

calib_packv5_041523_1651.root, FC#0, port C2

Entries	450
Mean	38.49
Std Dev	17.69

Turn on : 24.4988

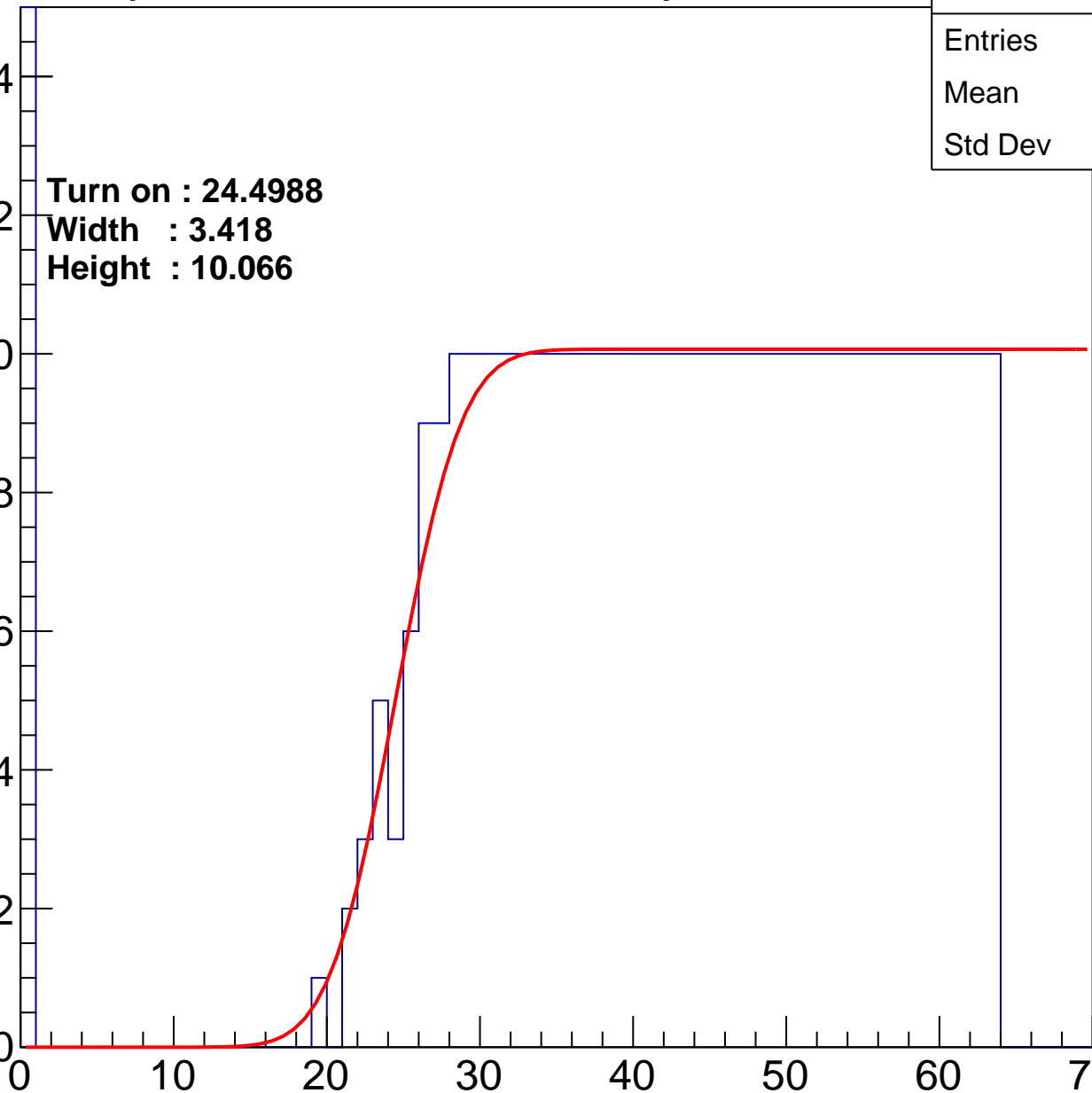
Width : 3.418

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch60

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	39.03
Std Dev	17.26

Turn on : 24.5466

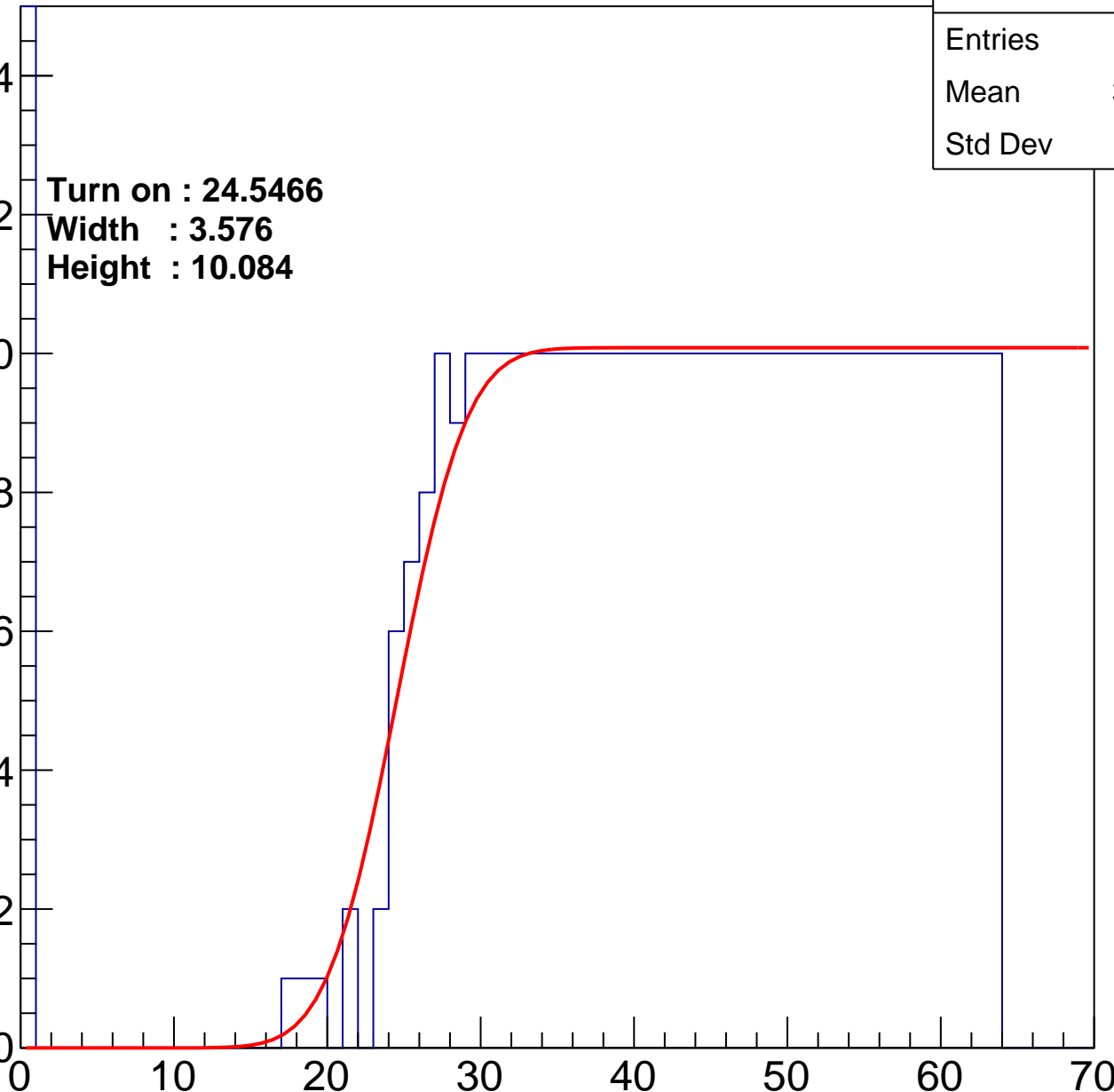
Width : 3.576

Height : 10.084

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch61

calib_packv5_041523_1651.root, FC#0, port C2

Entries	414
Mean	40.66
Std Dev	16.38

Turn on : 26.5030

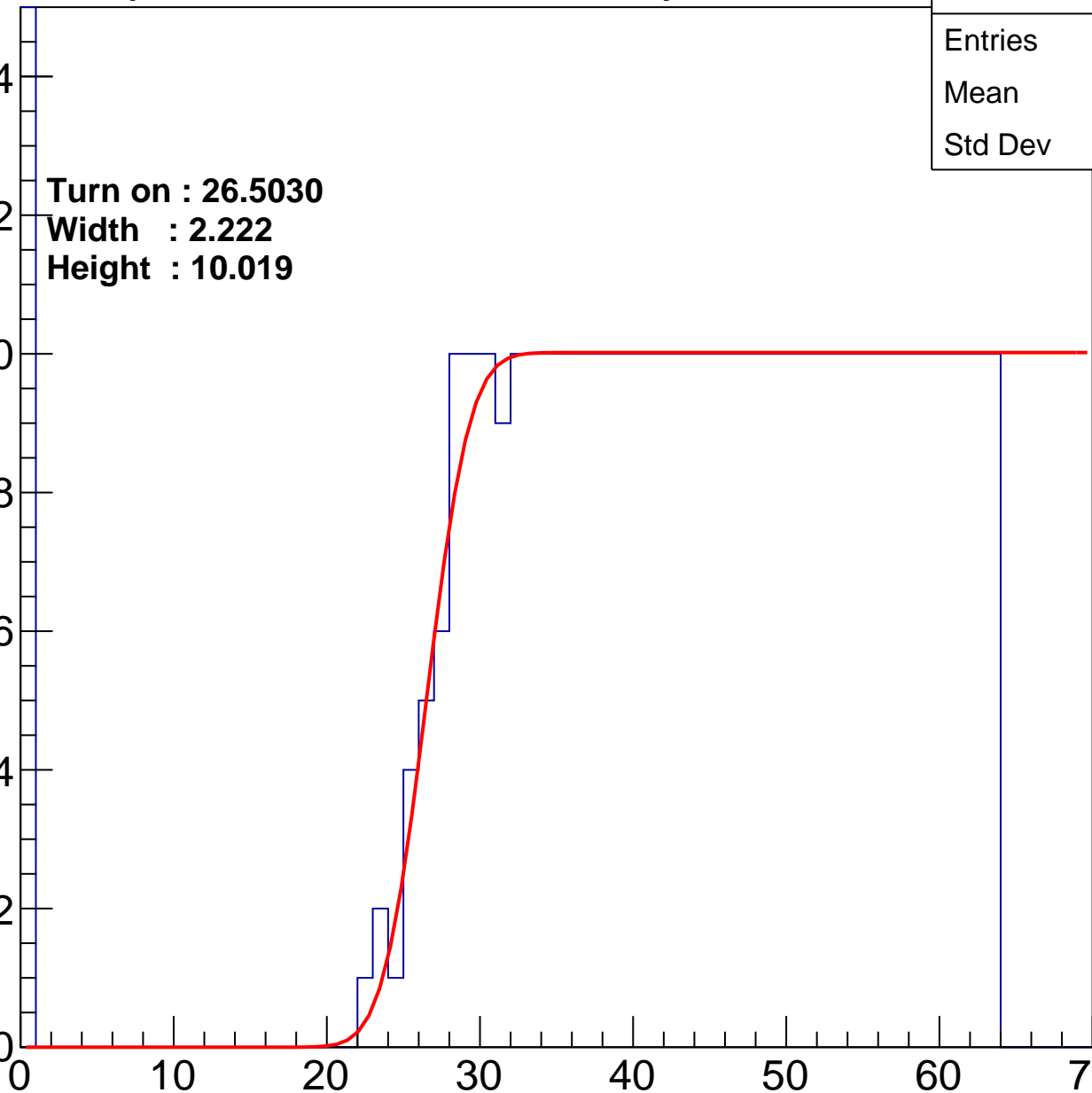
Width : 2.222

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch62

calib_packv5_041523_1651.root, FC#0, port C2

Entries	453
Mean	38.75
Std Dev	17.13

Turn on : 23.1063

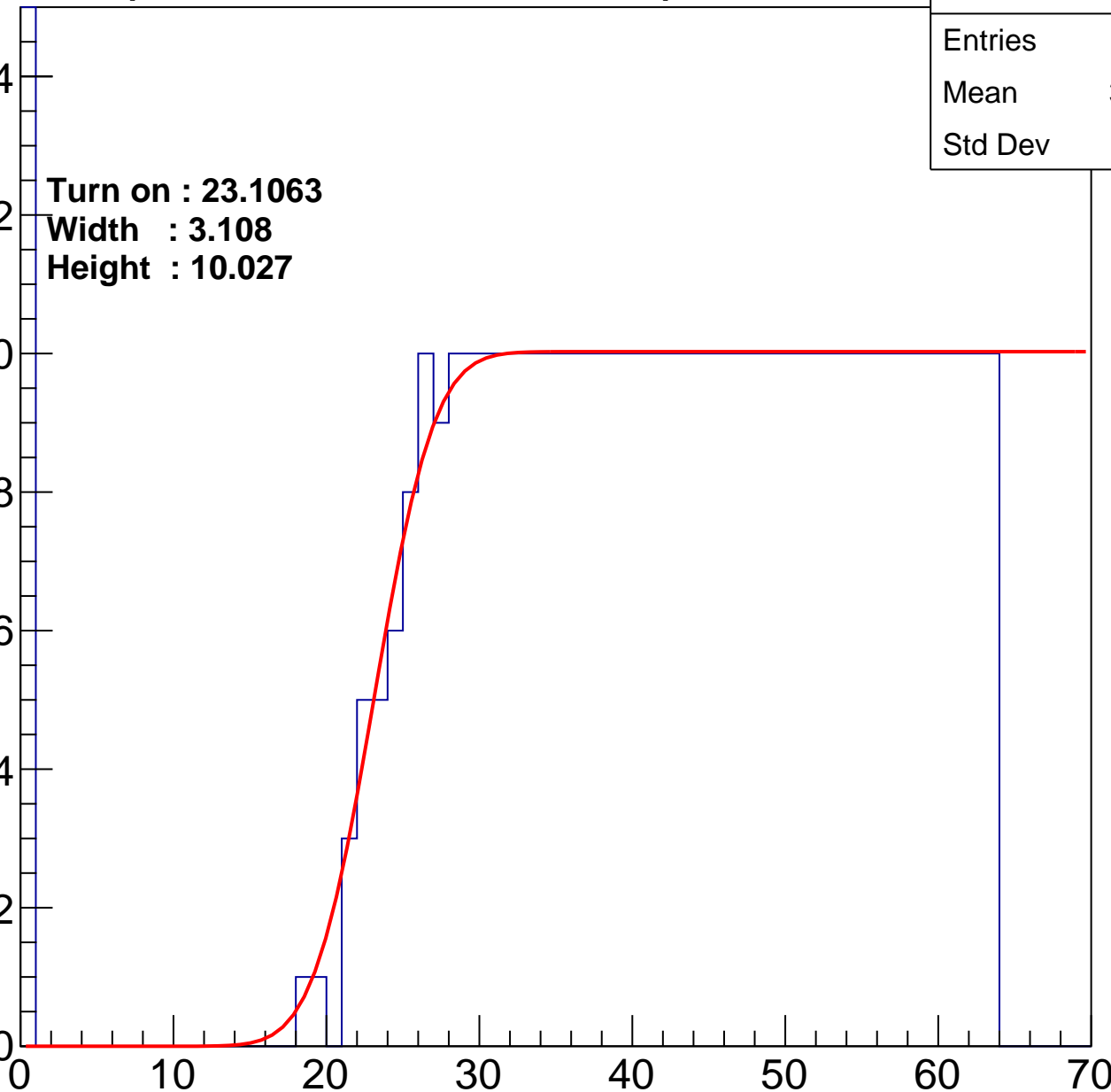
Width : 3.108

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch63

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	38.93
Std Dev	18.08

Turn on : 26.5546

Width : 2.156

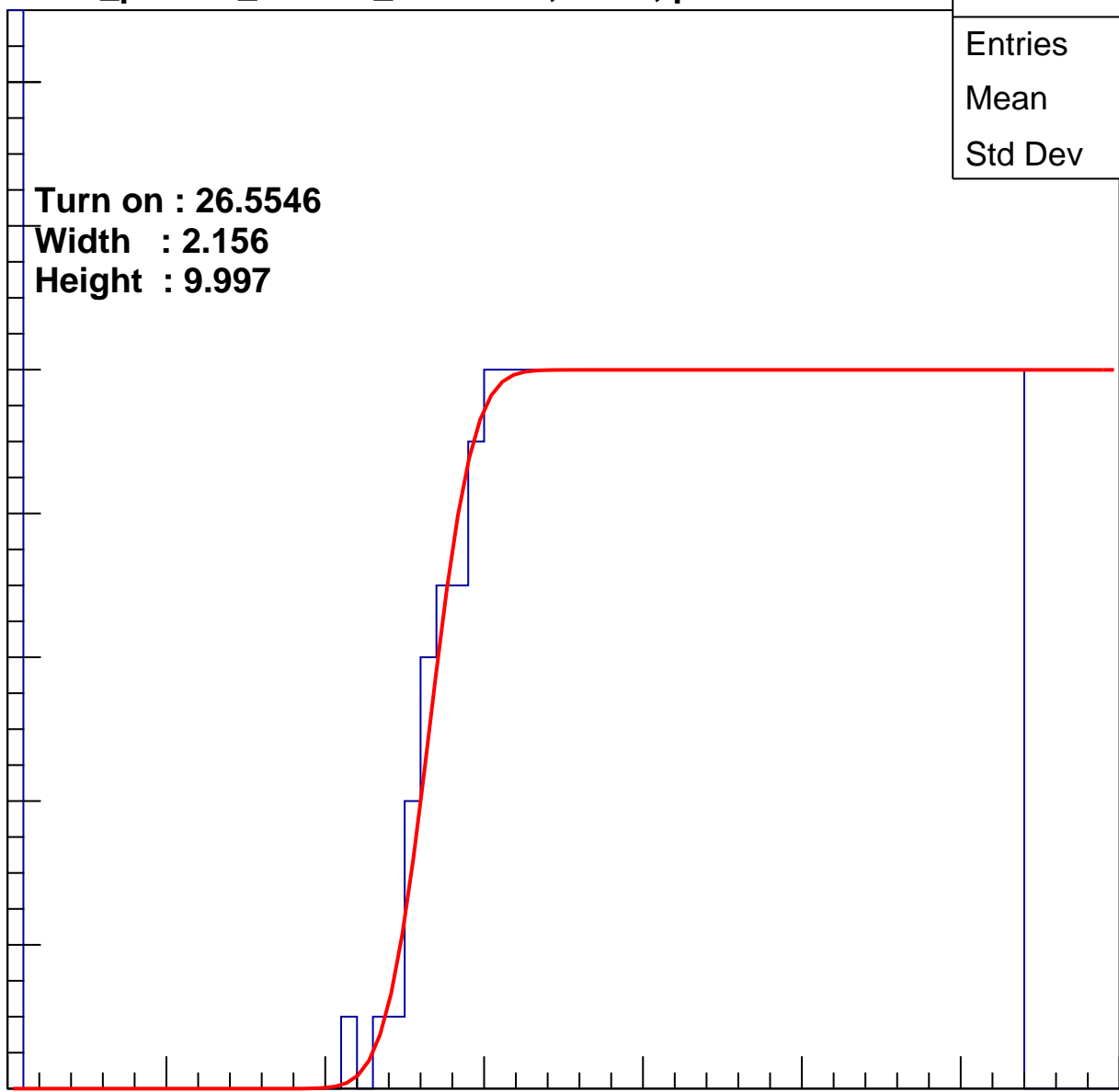
Height : 9.997

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U7-ch64

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	39.26
Std Dev	17.19

Turn on : 24.8089

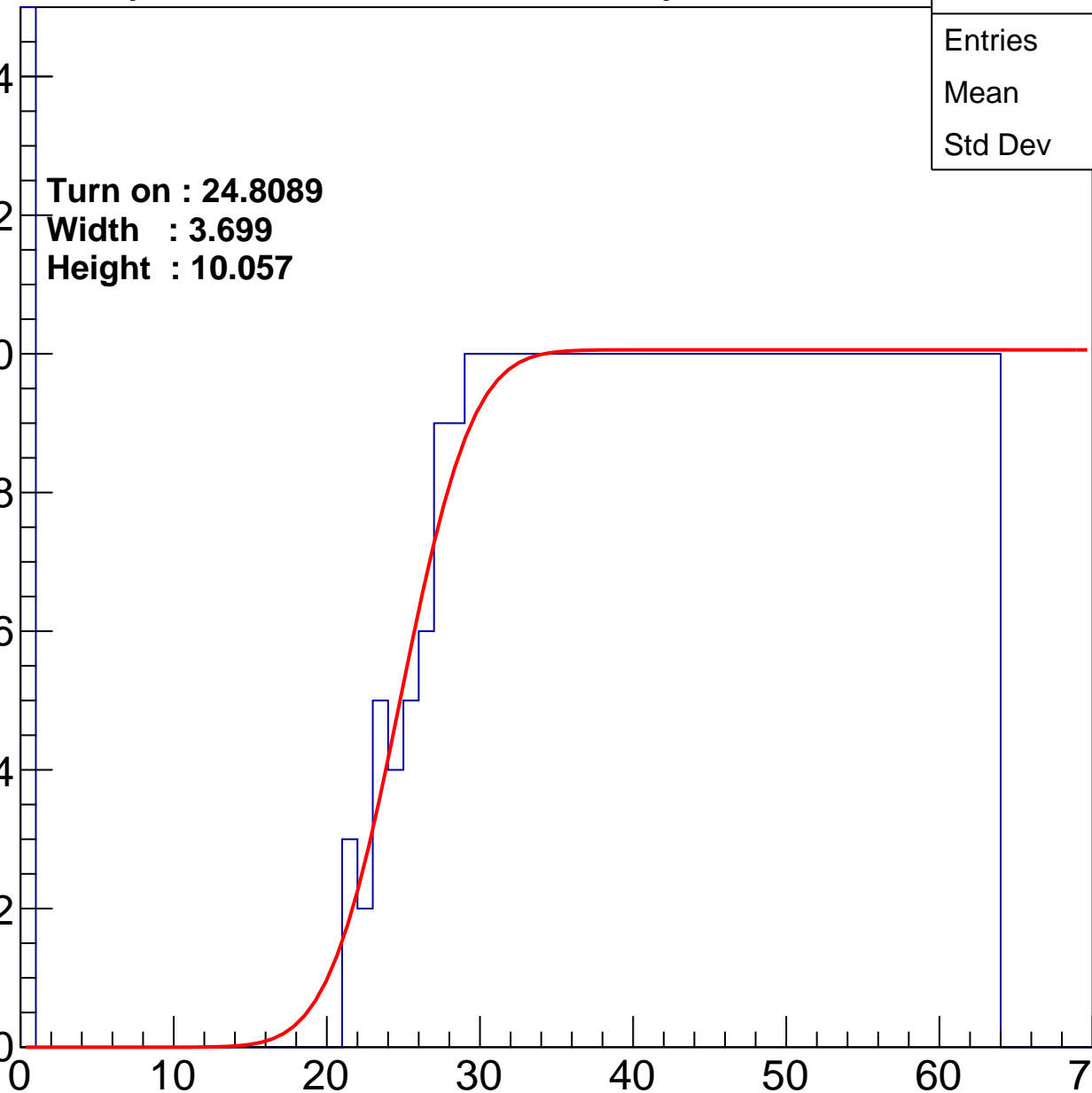
Width : 3.699

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch65

calib_packv5_041523_1651.root, FC#0, port C2

Entries	404
Mean	41.24
Std Dev	16.01

Turn on : 26.9477

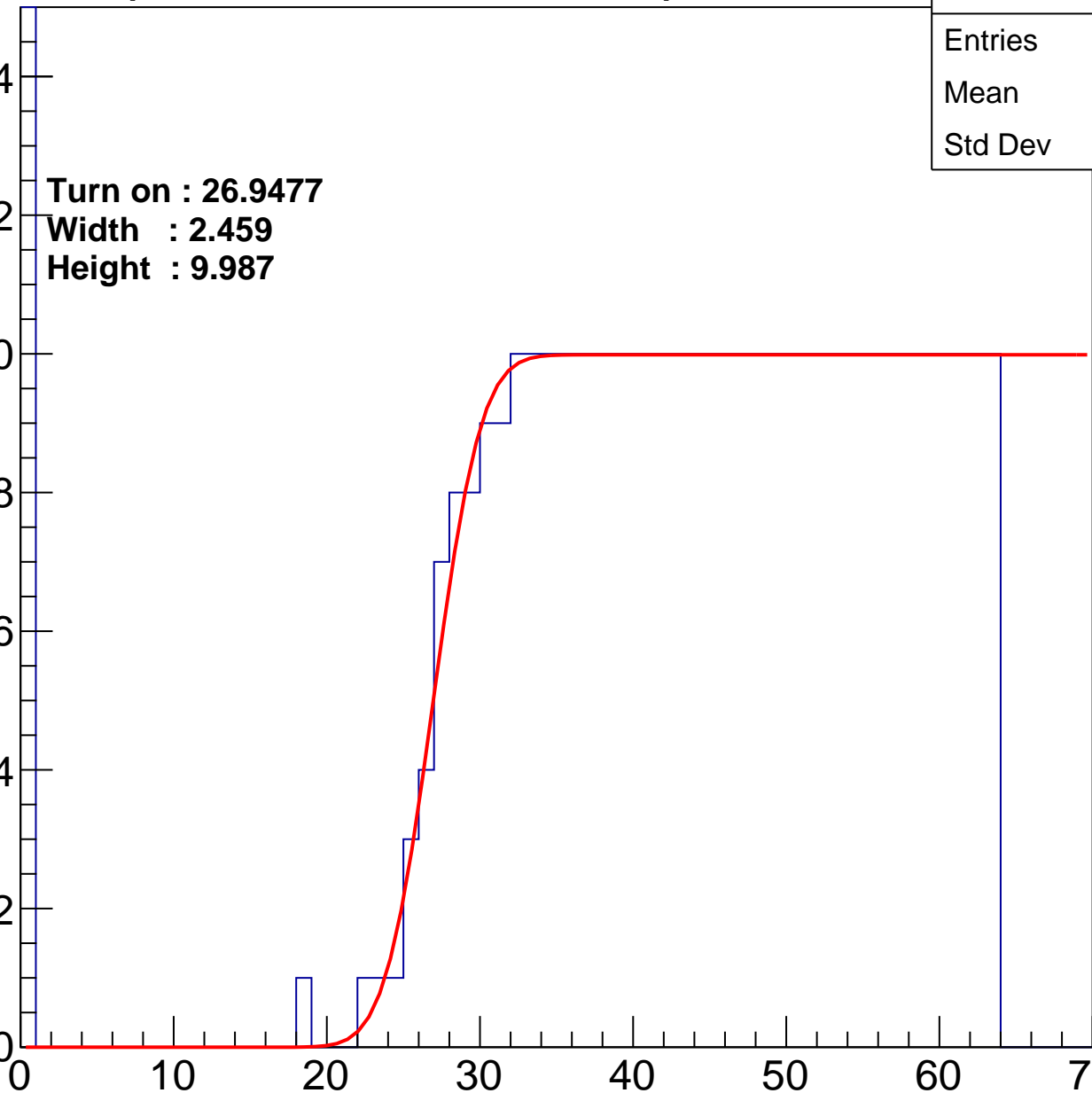
Width : 2.459

Height : 9.987

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch66

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	38.72
Std Dev	18.01

Turn on : 26.2696

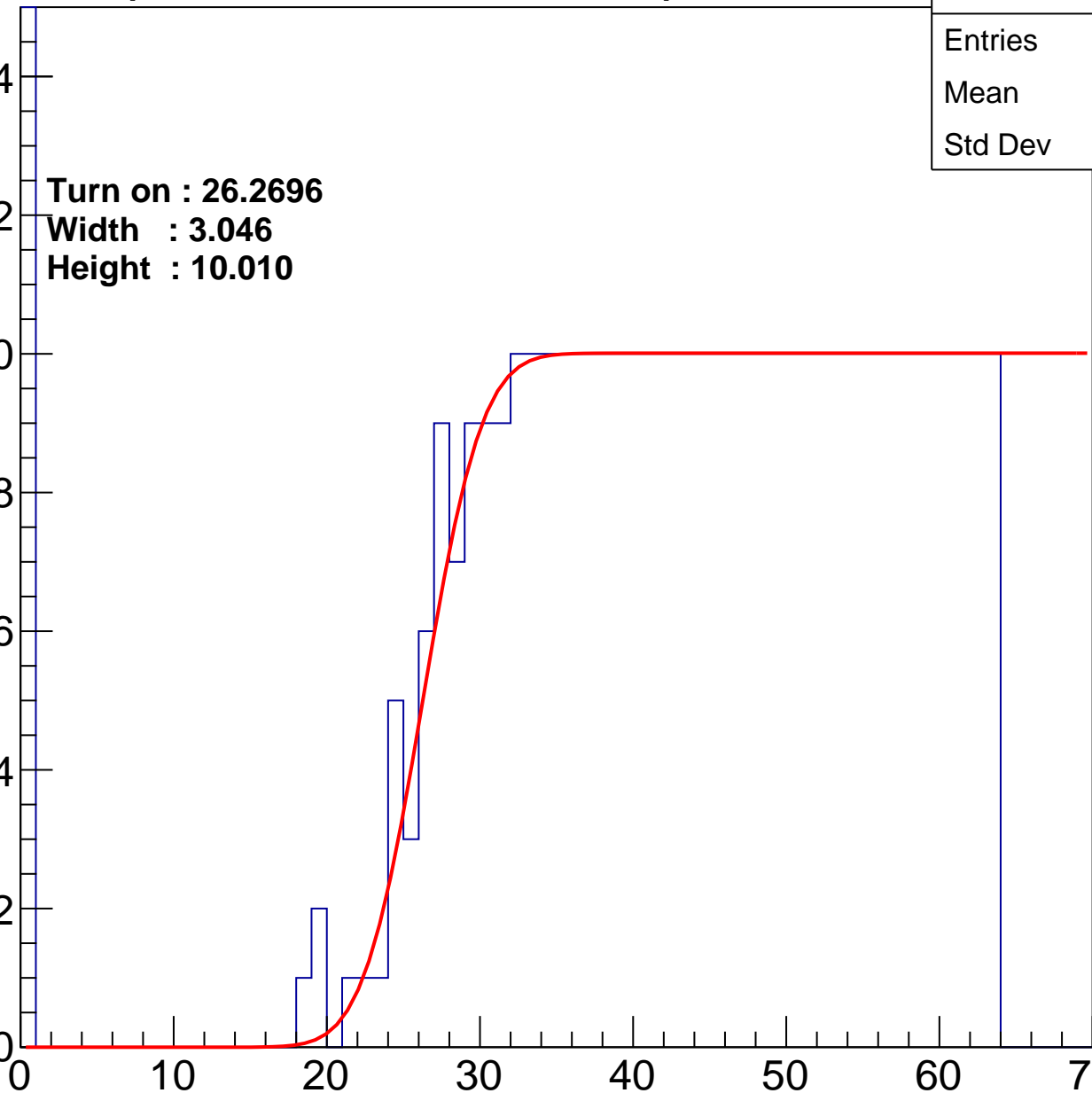
Width : 3.046

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch67

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	39.72
Std Dev	17.22

Turn on : 26.7264

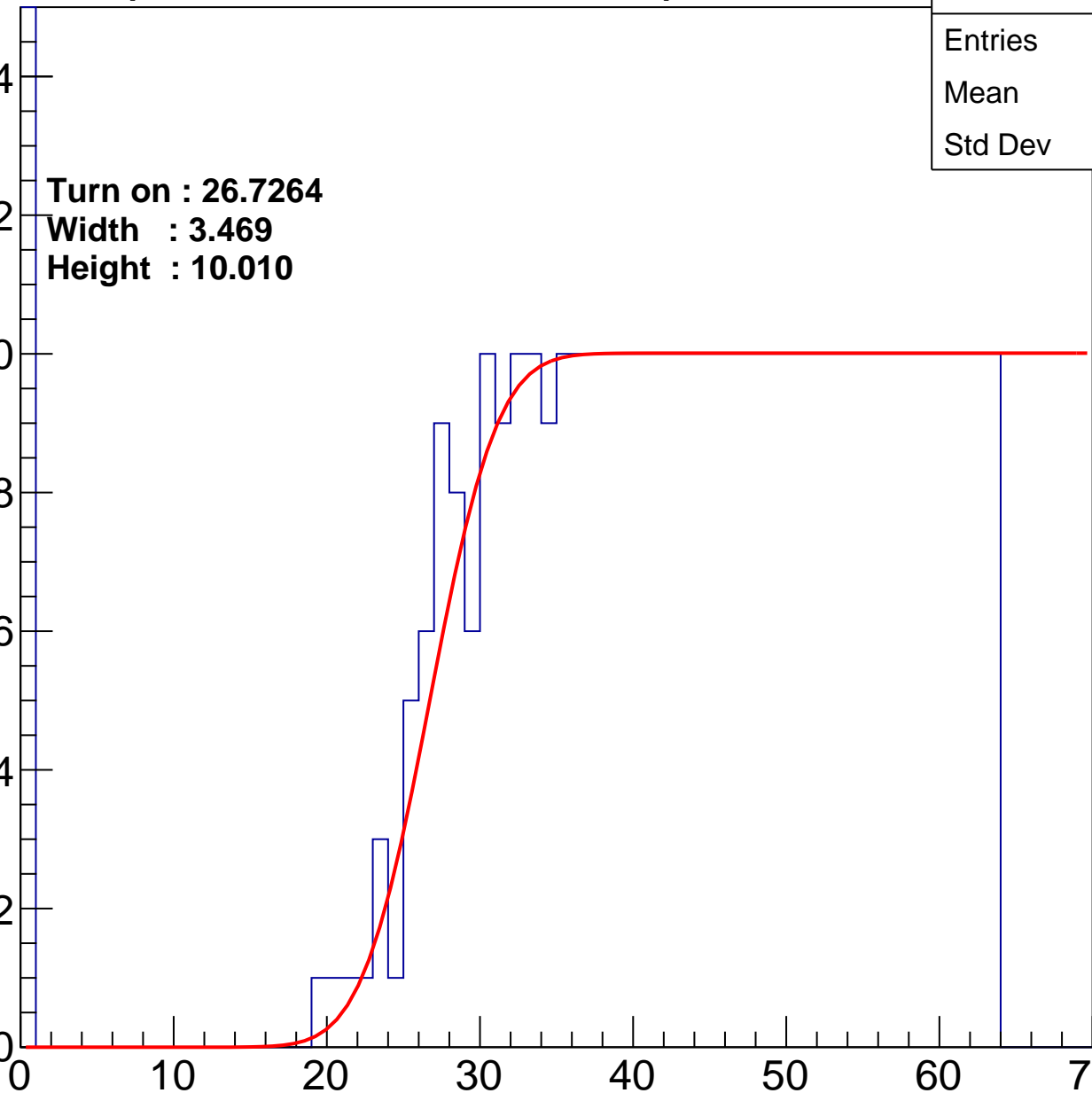
Width : 3.469

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch68

calib_packv5_041523_1651.root, FC#0, port C2

Entries	450
Mean	38.57
Std Dev	17.55

Turn on : 23.8369

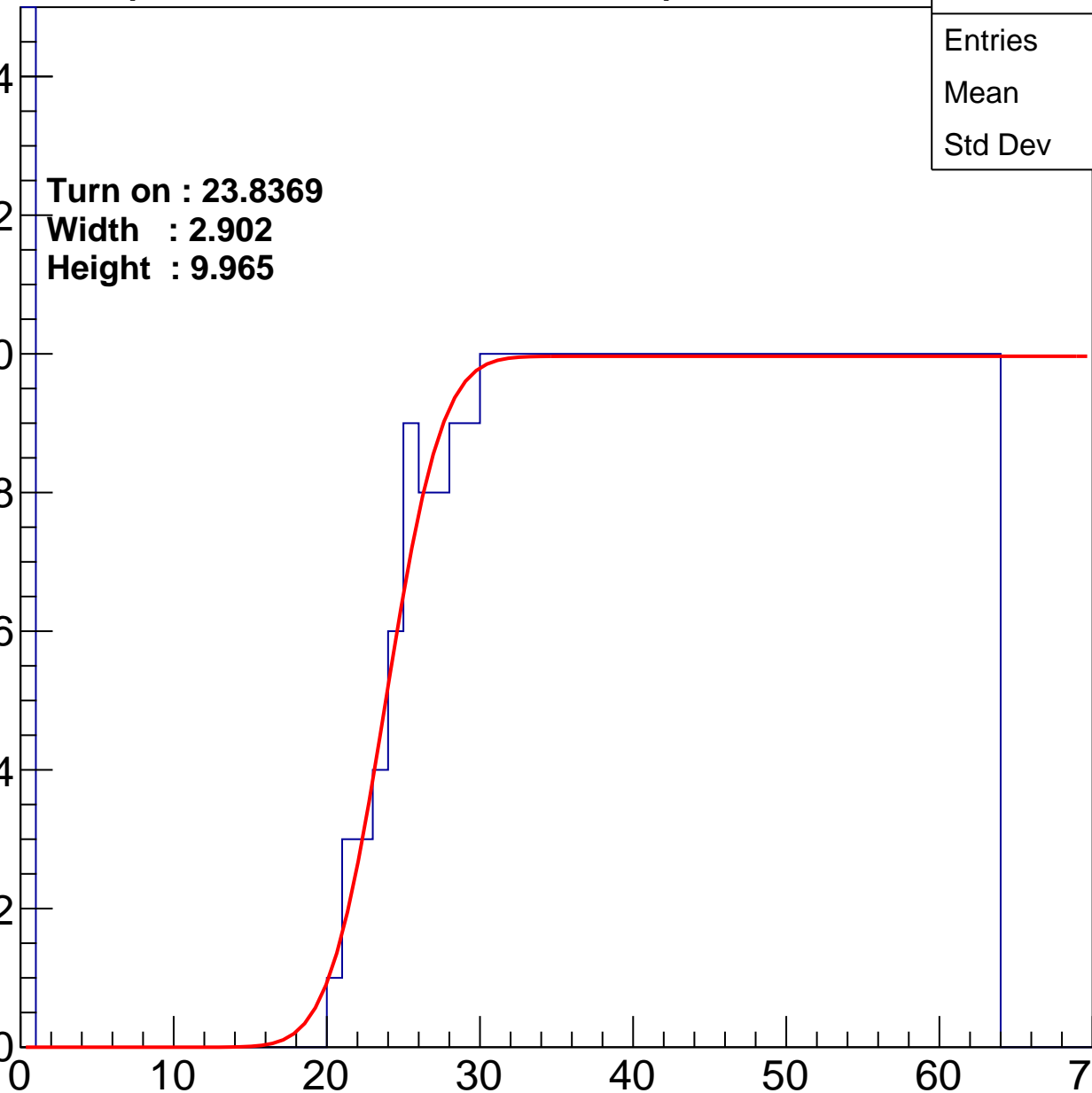
Width : 2.902

Height : 9.965

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch69

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.6
Std Dev	17.15

Turn on : 24.9128

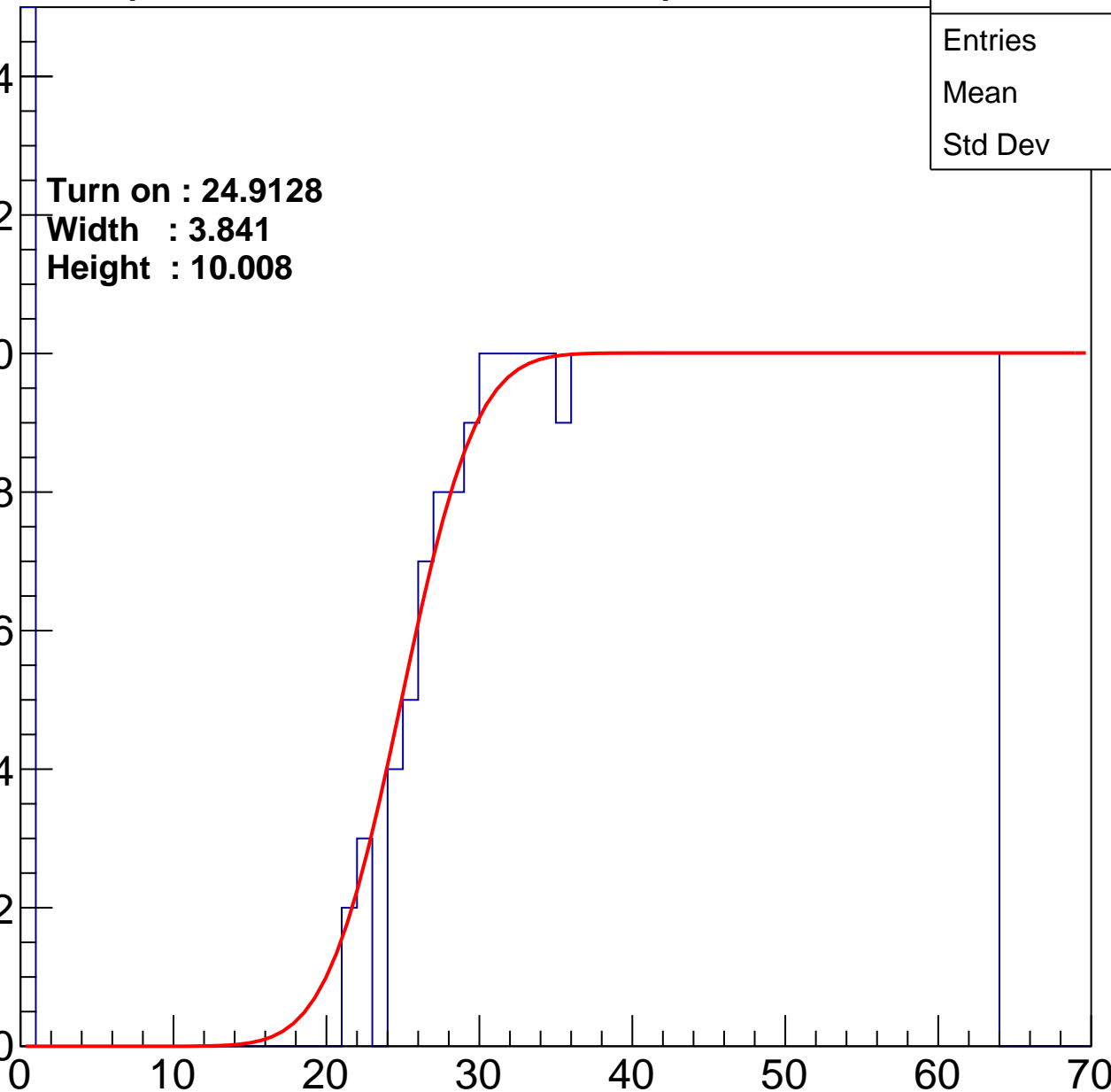
Width : 3.841

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch70

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	39.44
Std Dev	17.02

Turn on : 24.8009

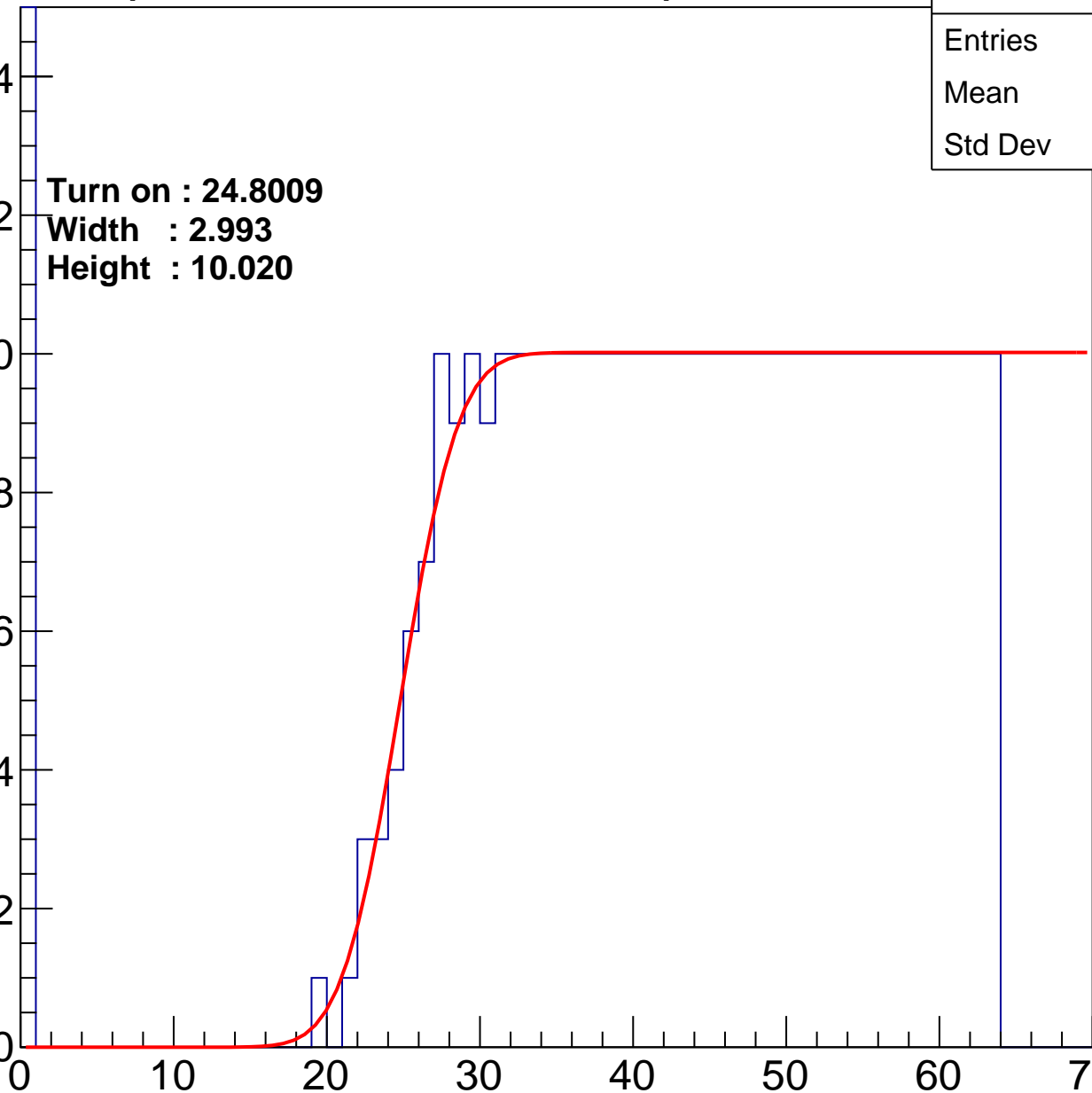
Width : 2.993

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch71

calib_packv5_041523_1651.root, FC#0, port C2

Entries	413
Mean	40.62
Std Dev	16.51

Turn on : 26.6095

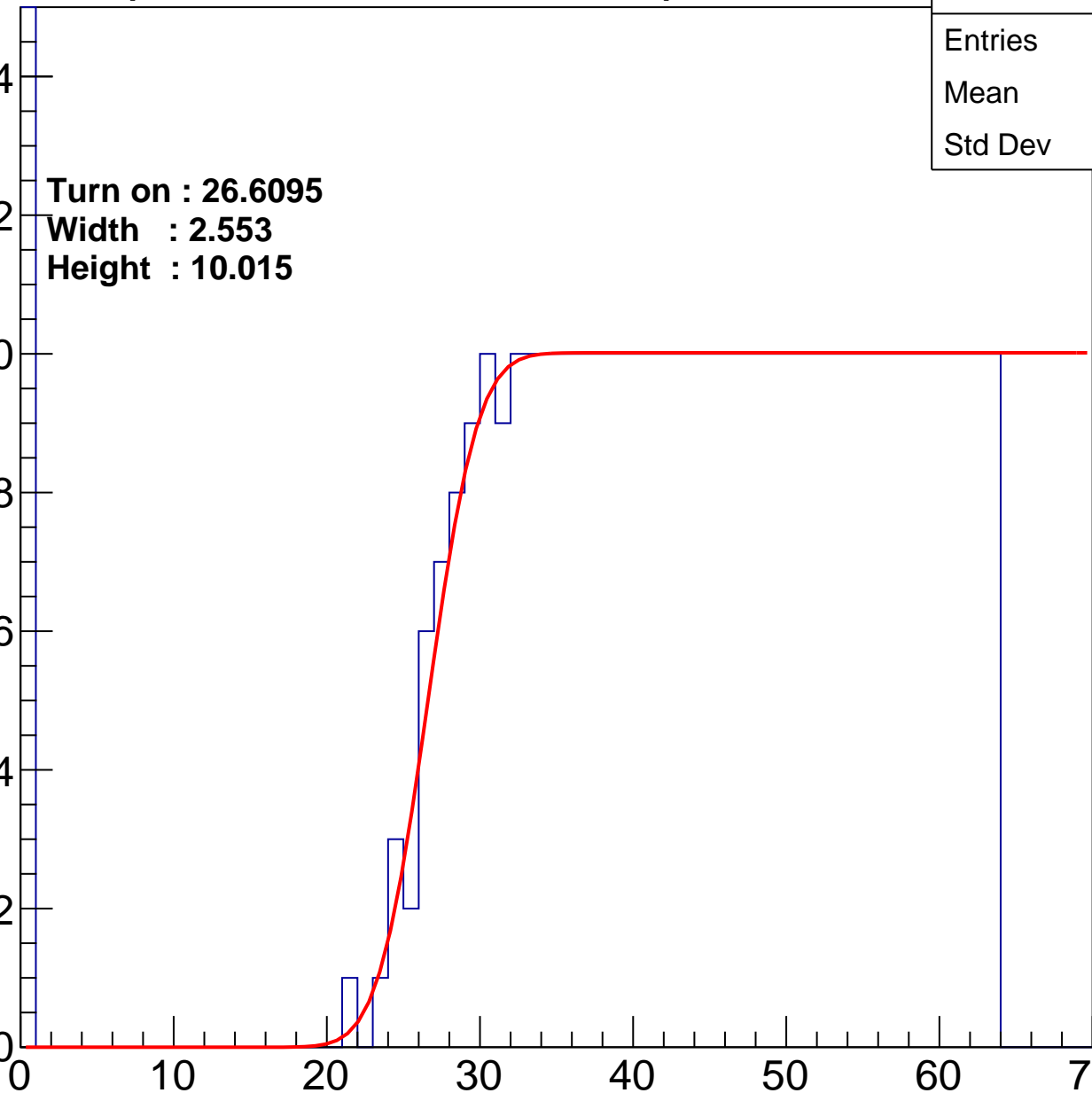
Width : 2.553

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch72

calib_packv5_041523_1651.root, FC#0, port C2

Entries	452
Mean	38.46
Std Dev	17.62

Turn on : 23.9529

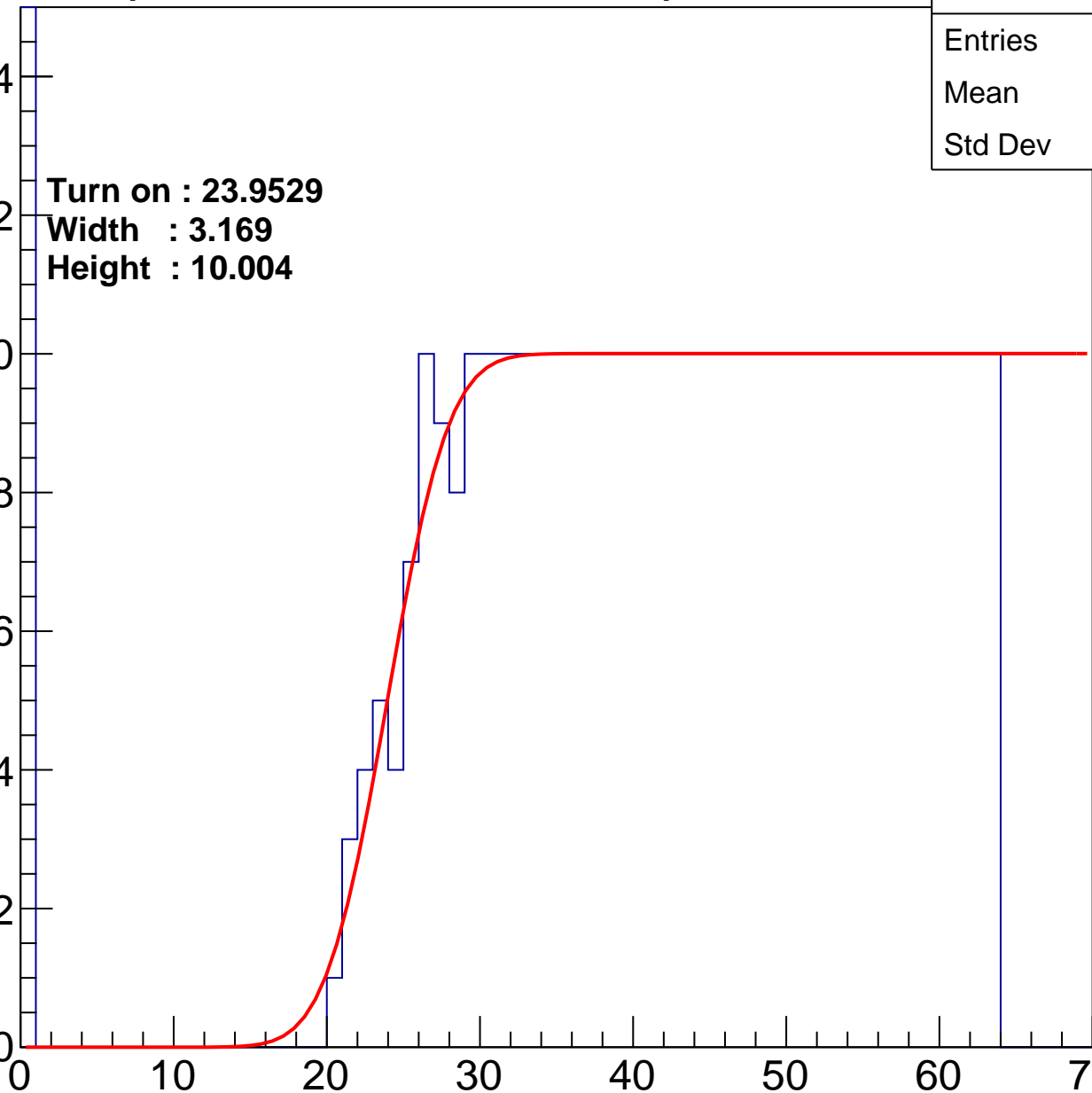
Width : 3.169

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch73

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	38.87
Std Dev	18.2

Turn on : 26.9940

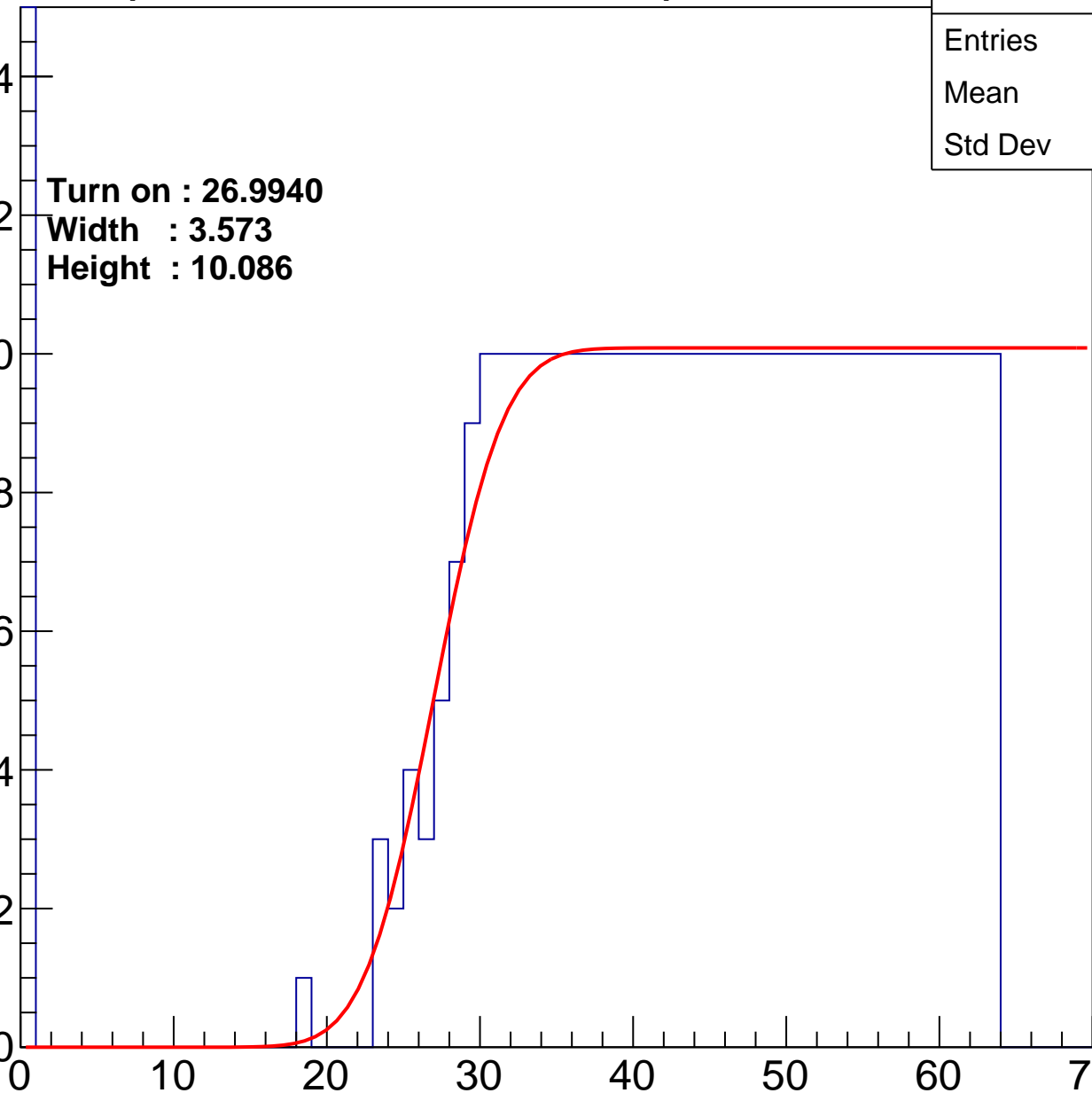
Width : 3.573

Height : 10.086

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch74

calib_packv5_041523_1651.root, FC#0, port C2

Entries	425
Mean	39.67
Std Dev	17.28

Turn on : 26.6060

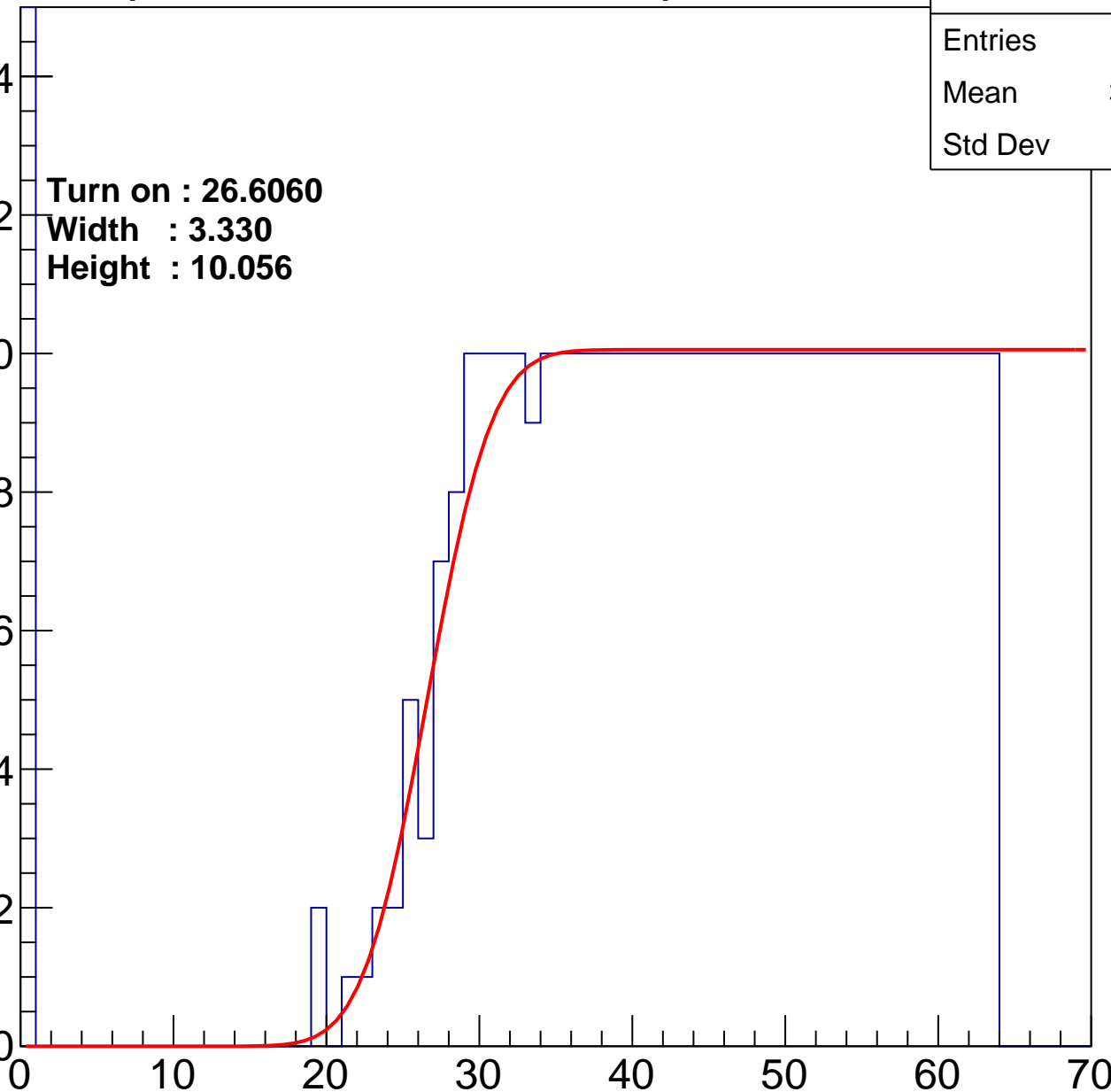
Width : 3.330

Height : 10.056

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch75

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39
Std Dev	18.05

Turn on : 27.3090

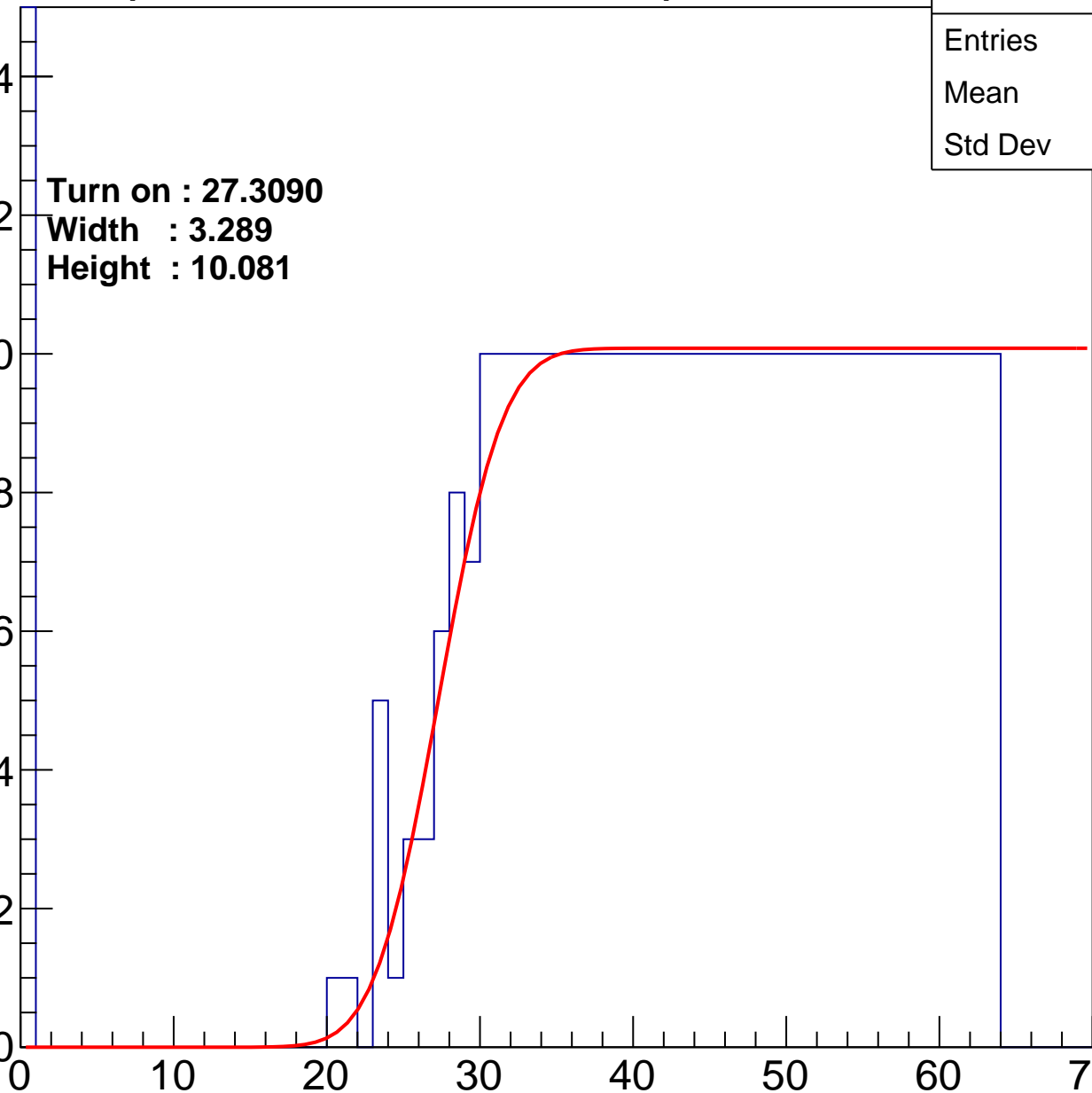
Width : 3.289

Height : 10.081

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch76

calib_packv5_041523_1651.root, FC#0, port C2

Entries	421
Mean	39.95
Std Dev	17.08

Turn on : 26.2001

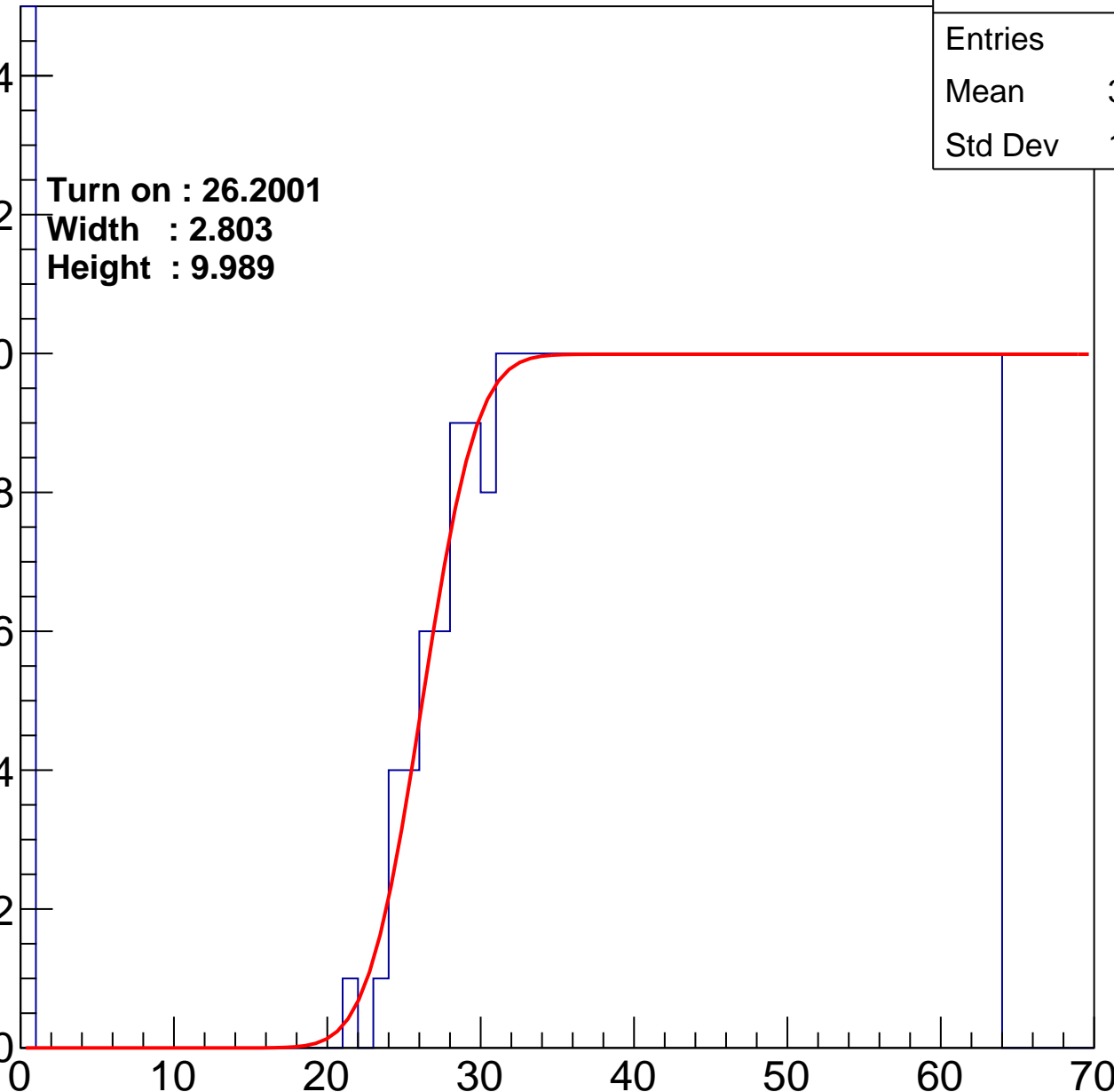
Width : 2.803

Height : 9.989

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch77

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	39.61
Std Dev	17.89

Turn on : 27.8485

Width : 2.478

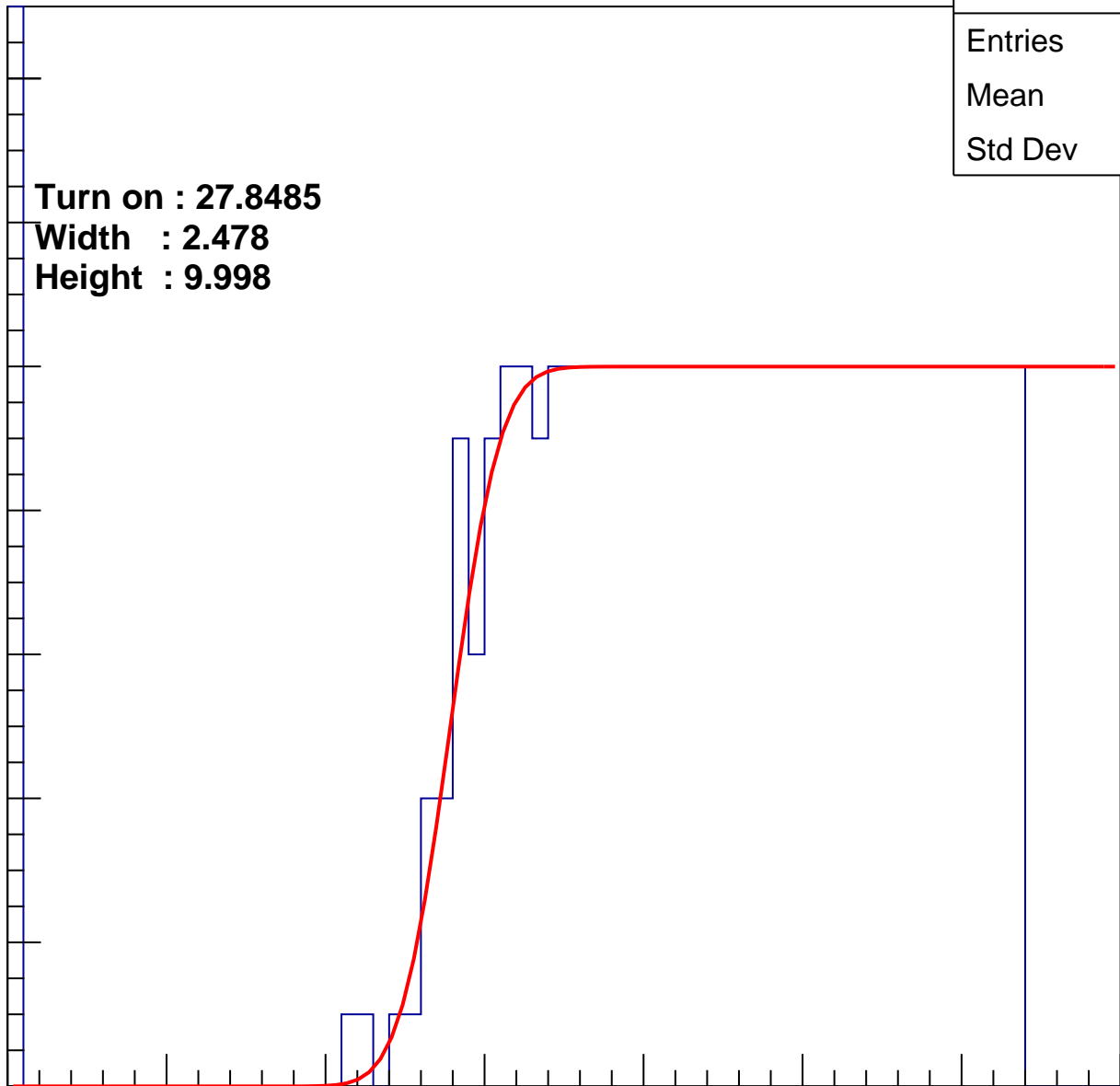
Height : 9.998

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U7-ch78

calib_packv5_041523_1651.root, FC#0, port C2

Entries	446
Mean	39.03
Std Dev	17.07

Turn on : 24.1771

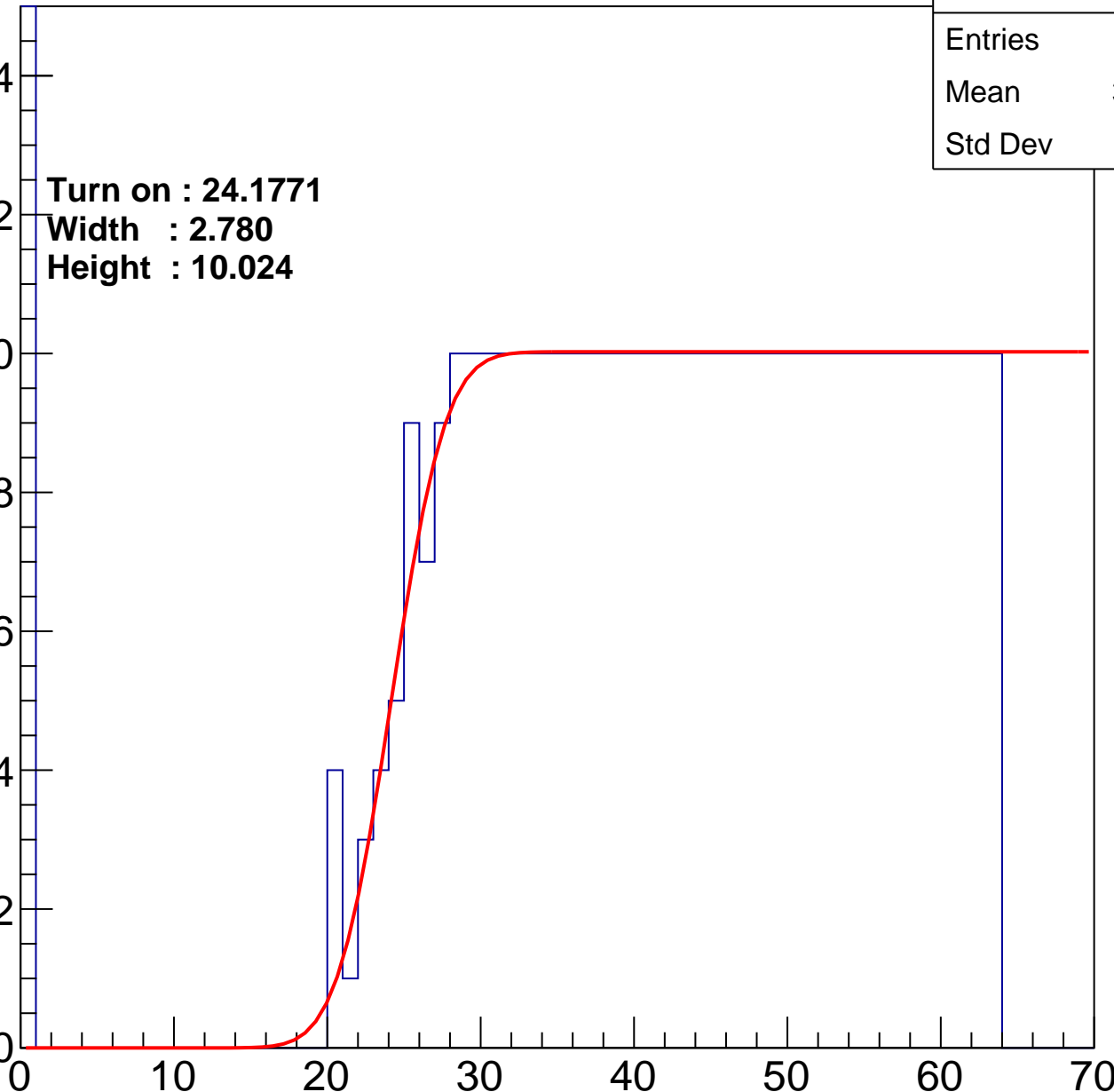
Width : 2.780

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch79

calib_packv5_041523_1651.root, FC#0, port C2

Entries	422
Mean	39.74
Std Dev	17.36

Turn on : 26.4619

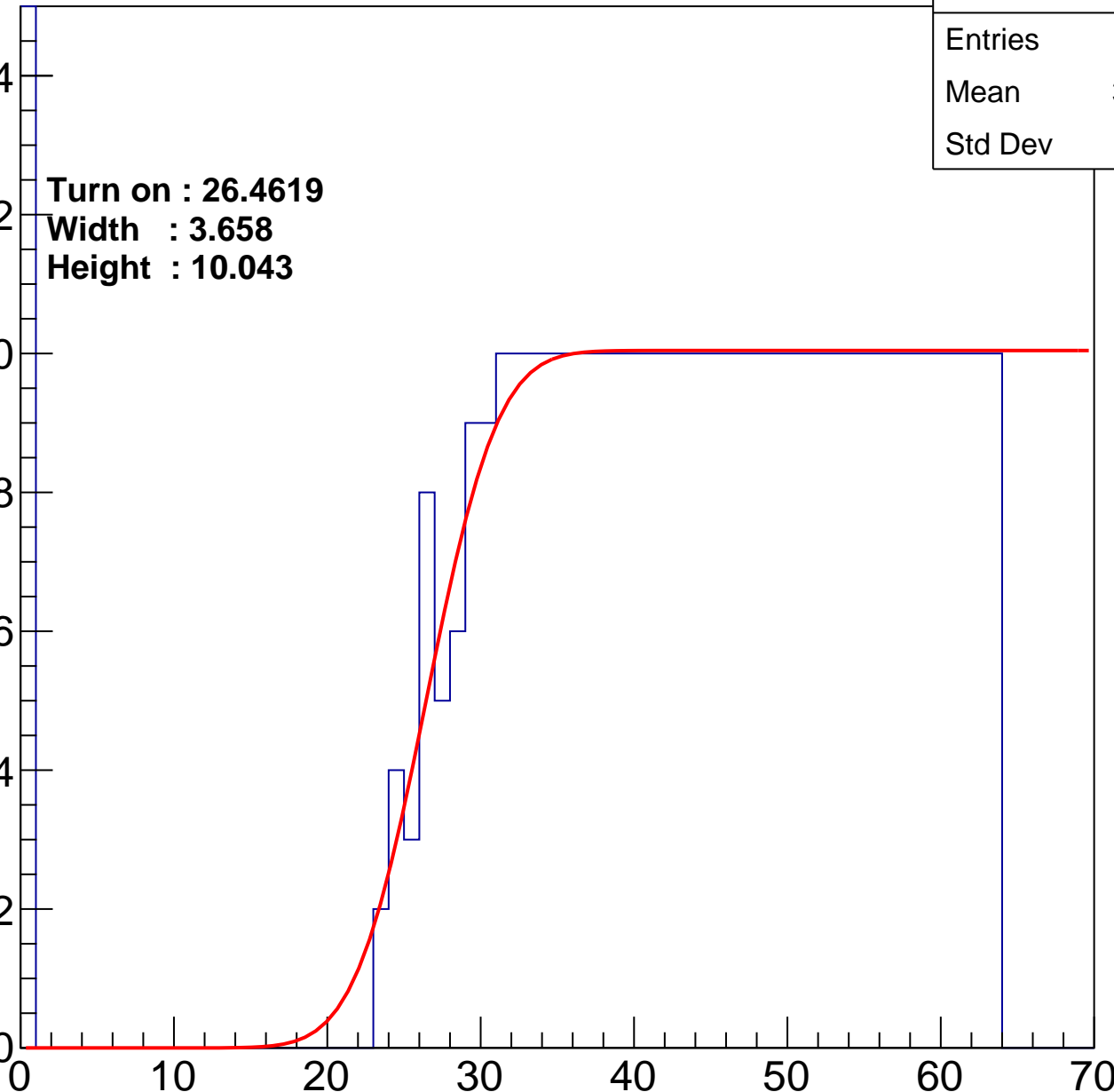
Width : 3.658

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch80

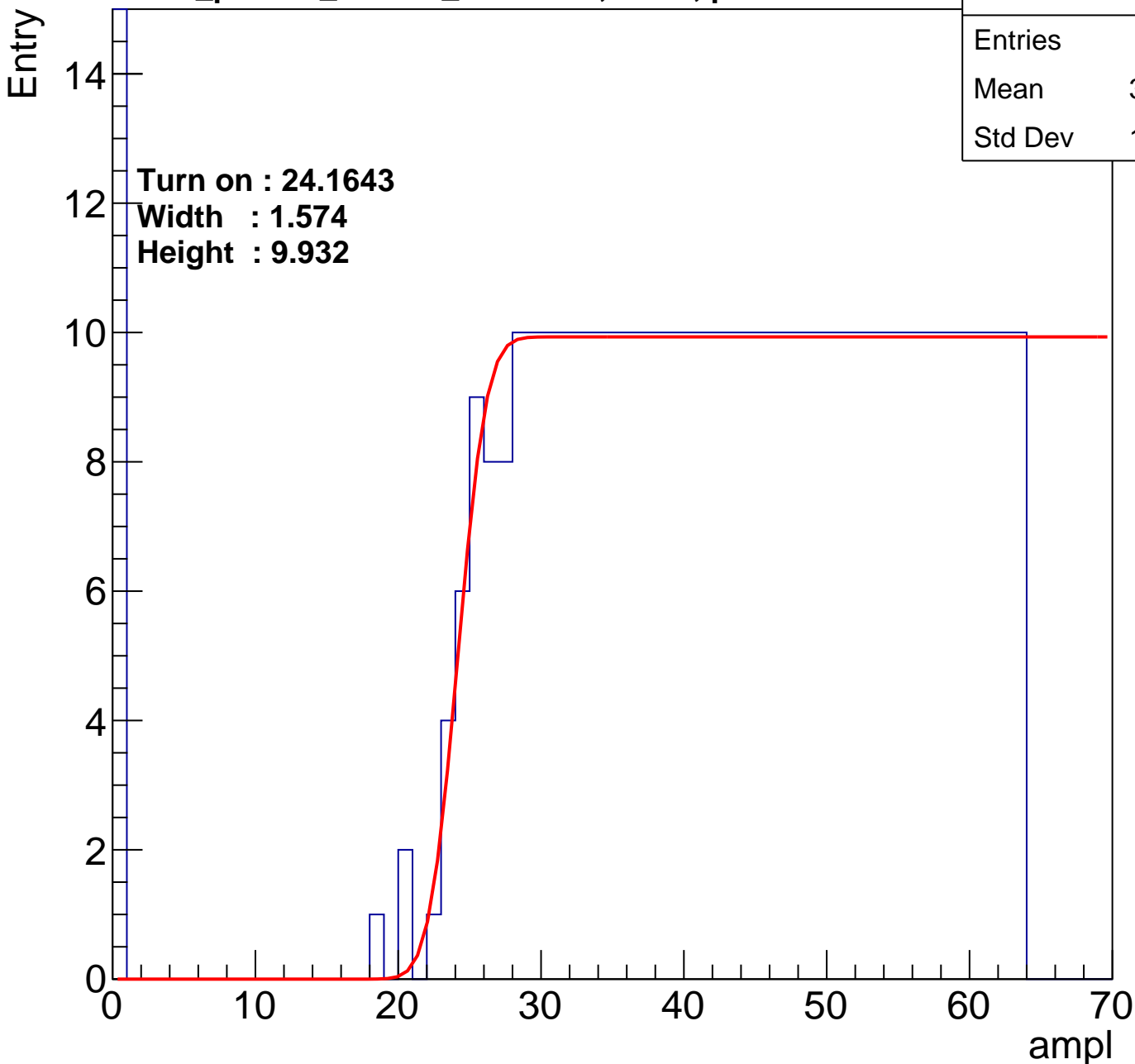
calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	39.69
Std Dev	16.55

Turn on : 24.1643

Width : 1.574

Height : 9.932



B1L103S, U7-ch81

calib_packv5_041523_1651.root, FC#0, port C2

Entries	403
Mean	40.64
Std Dev	17.09

Turn on : 27.8787

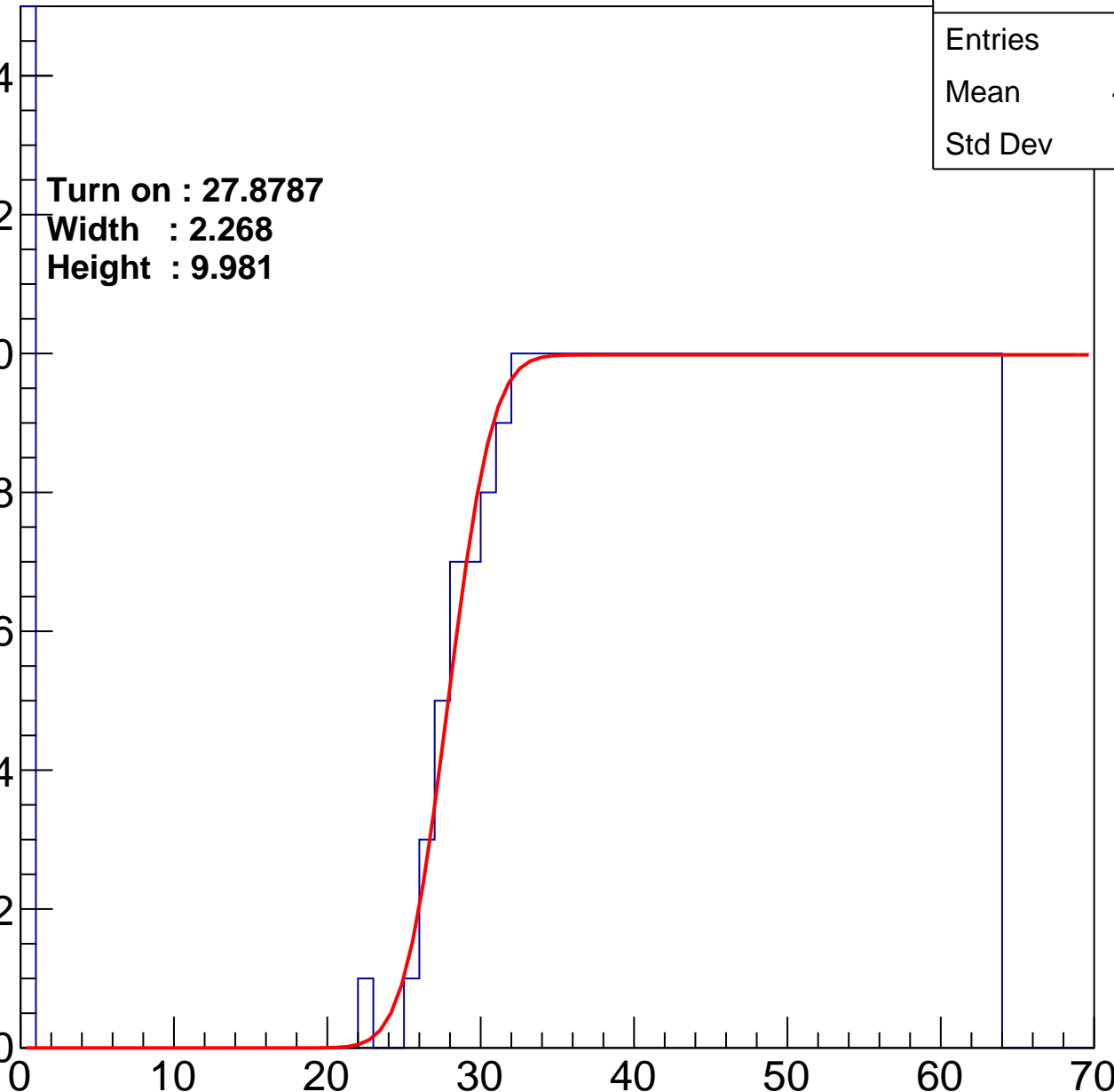
Width : 2.268

Height : 9.981

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch82

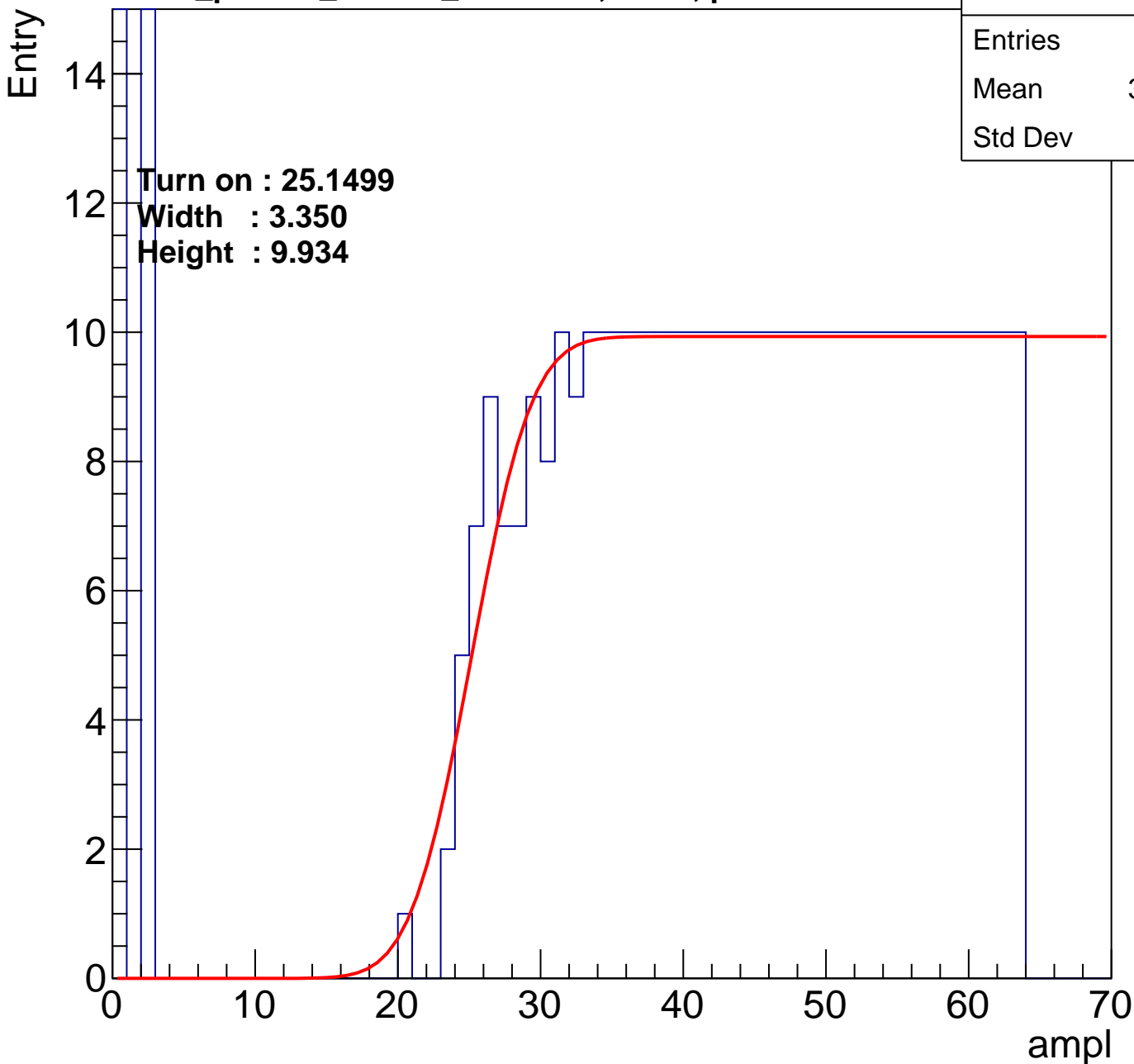
calib_packv5_041523_1651.root, FC#0, port C2

Entries	457
Mean	37.22
Std Dev	19

Turn on : 25.1499

Width : 3.350

Height : 9.934



B1L103S, U7-ch83

calib_packv5_041523_1651.root, FC#0, port C2

Entries	425
Mean	39.52
Std Dev	17.52

Turn on : 26.2758

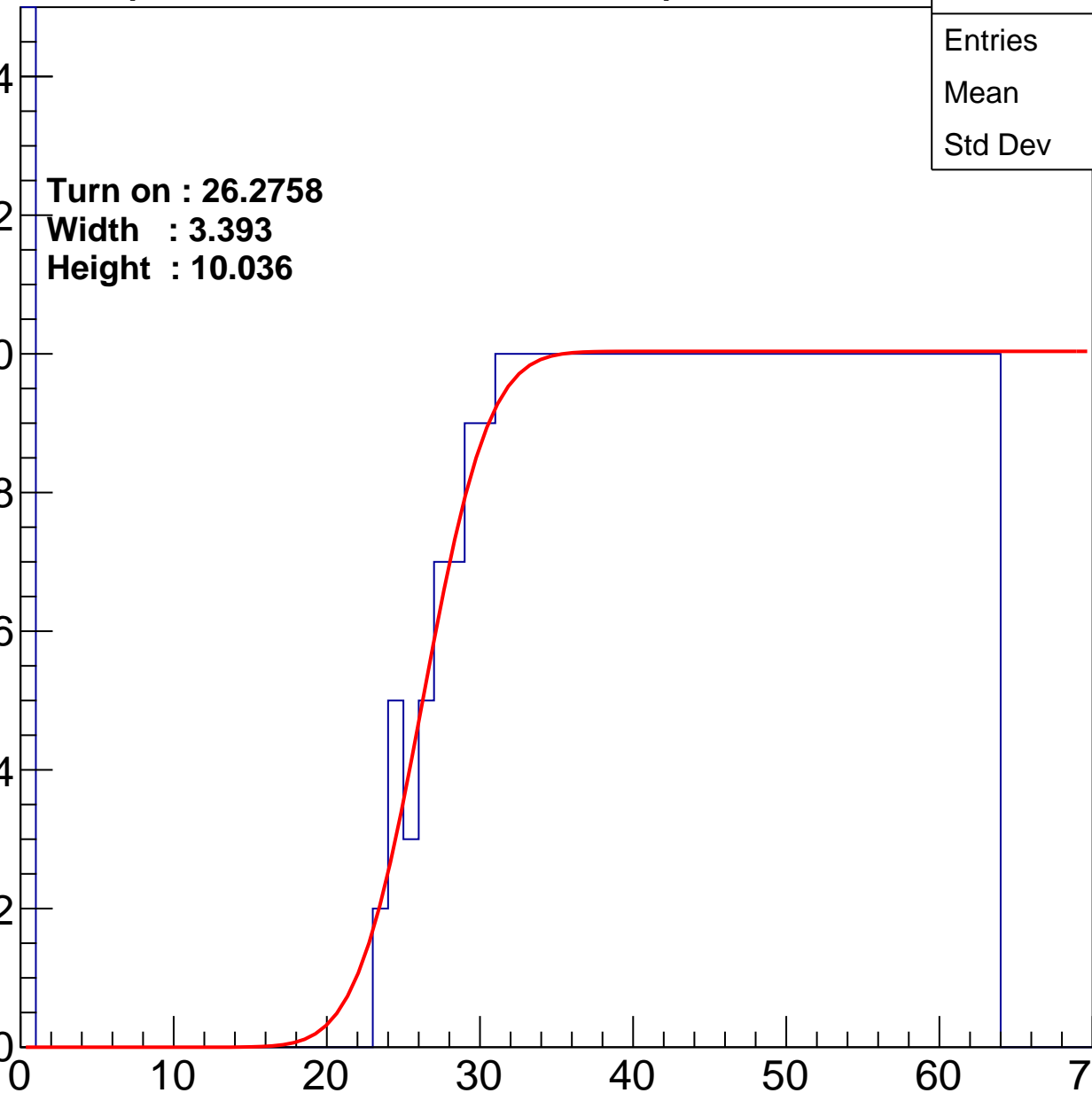
Width : 3.393

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch84

calib_packv5_041523_1651.root, FC#0, port C2

Entries	417
Mean	40.39
Std Dev	16.61

Turn on : 26.4126

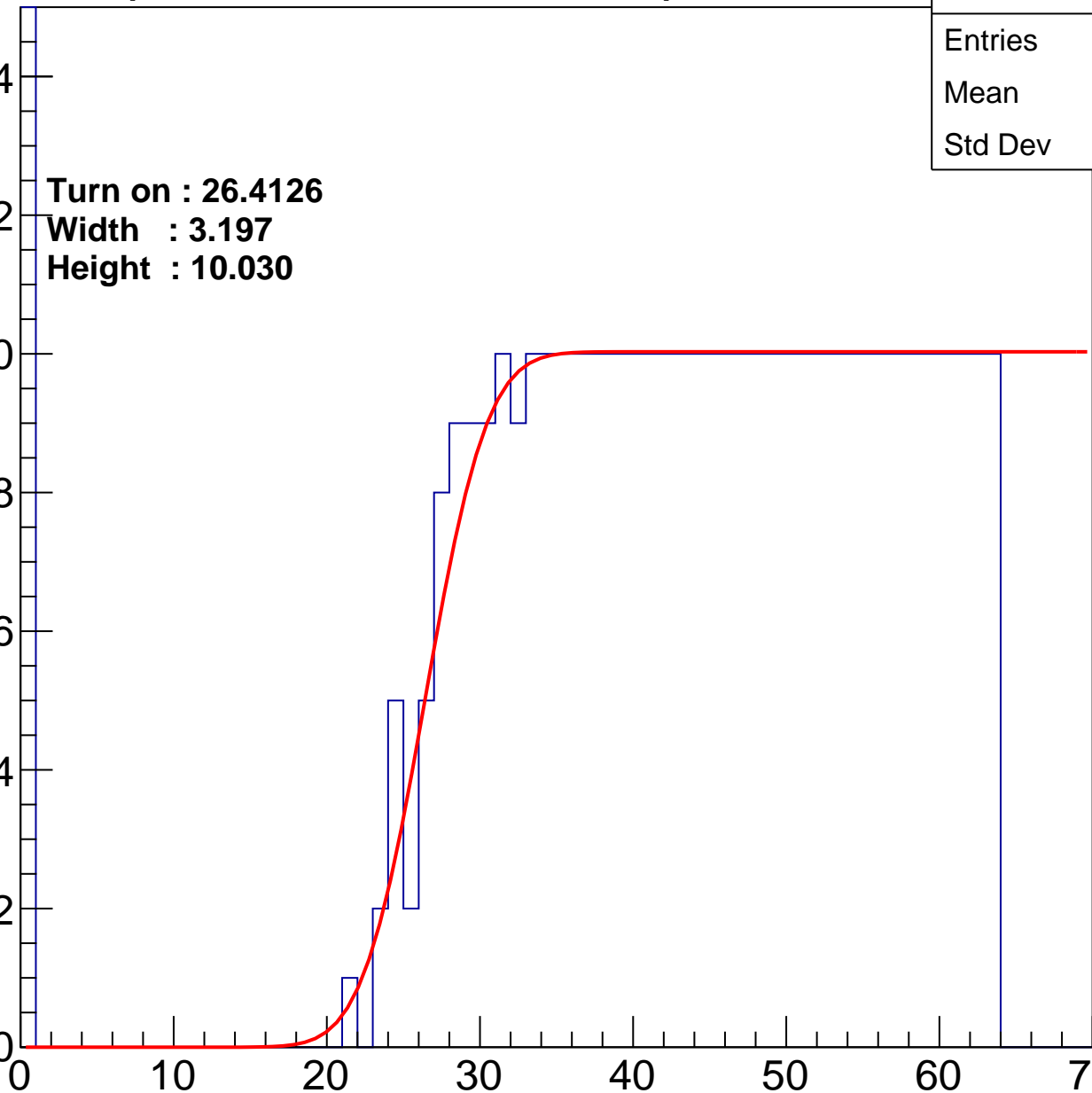
Width : 3.197

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch85

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	39.25
Std Dev	17.56

Turn on : 25.8874

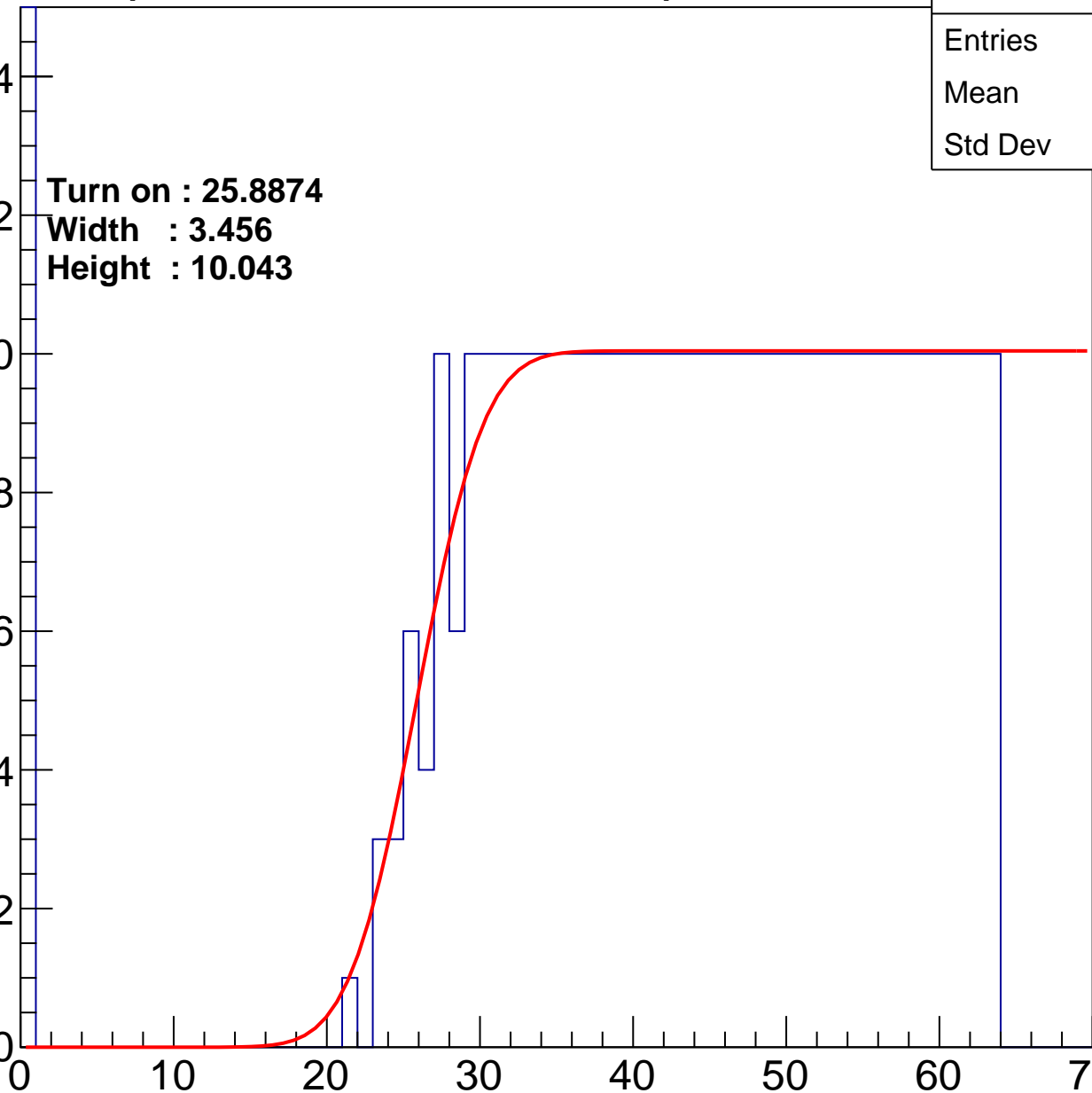
Width : 3.456

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch86

calib_packv5_041523_1651.root, FC#0, port C2

Entries	448
Mean	37.99
Std Dev	18.5

Turn on : 25.6021

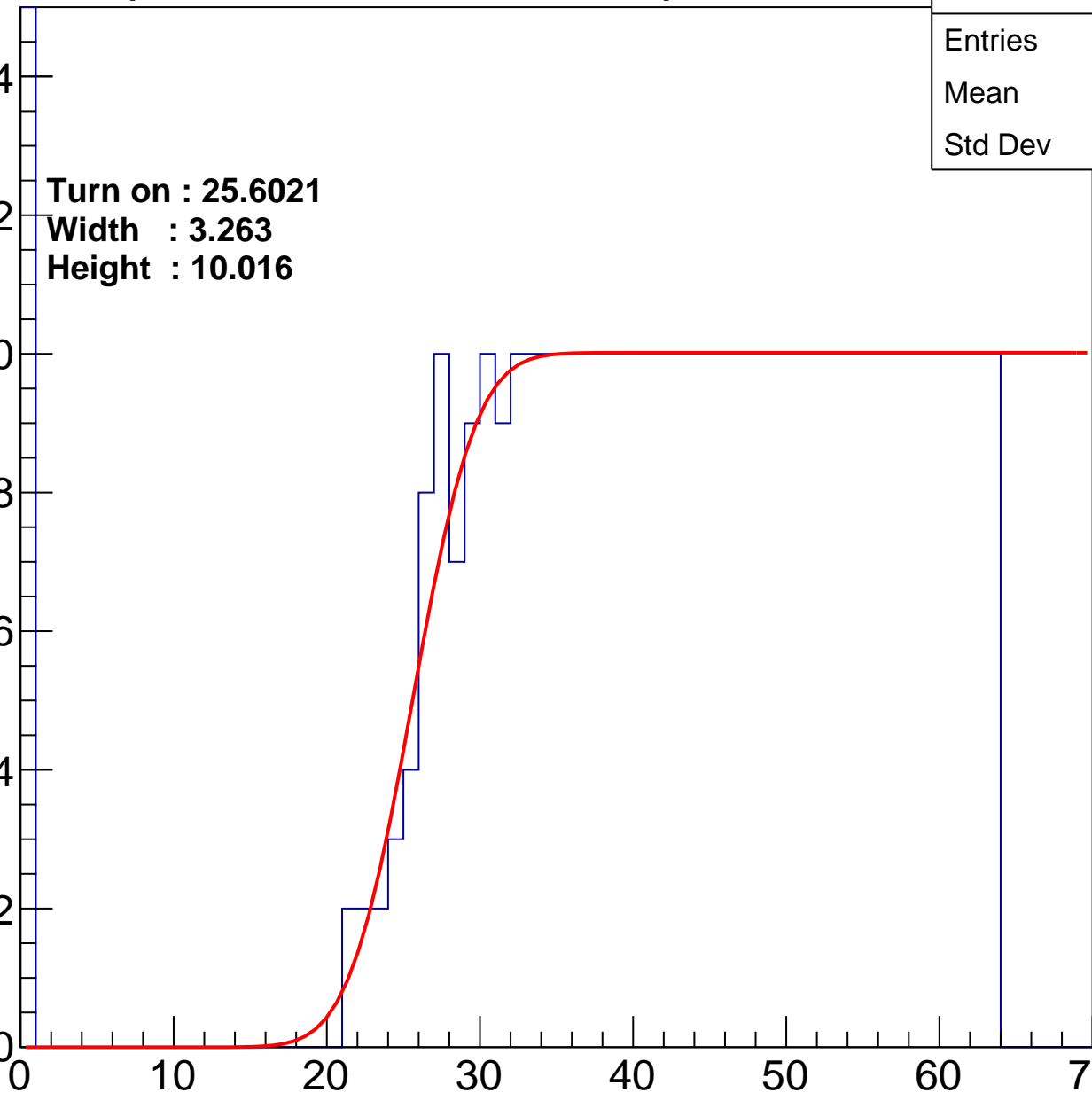
Width : 3.263

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch87

calib_packv5_041523_1651.root, FC#0, port C2

Entries	411
Mean	40.65
Std Dev	16.59

Turn on : 26.2368

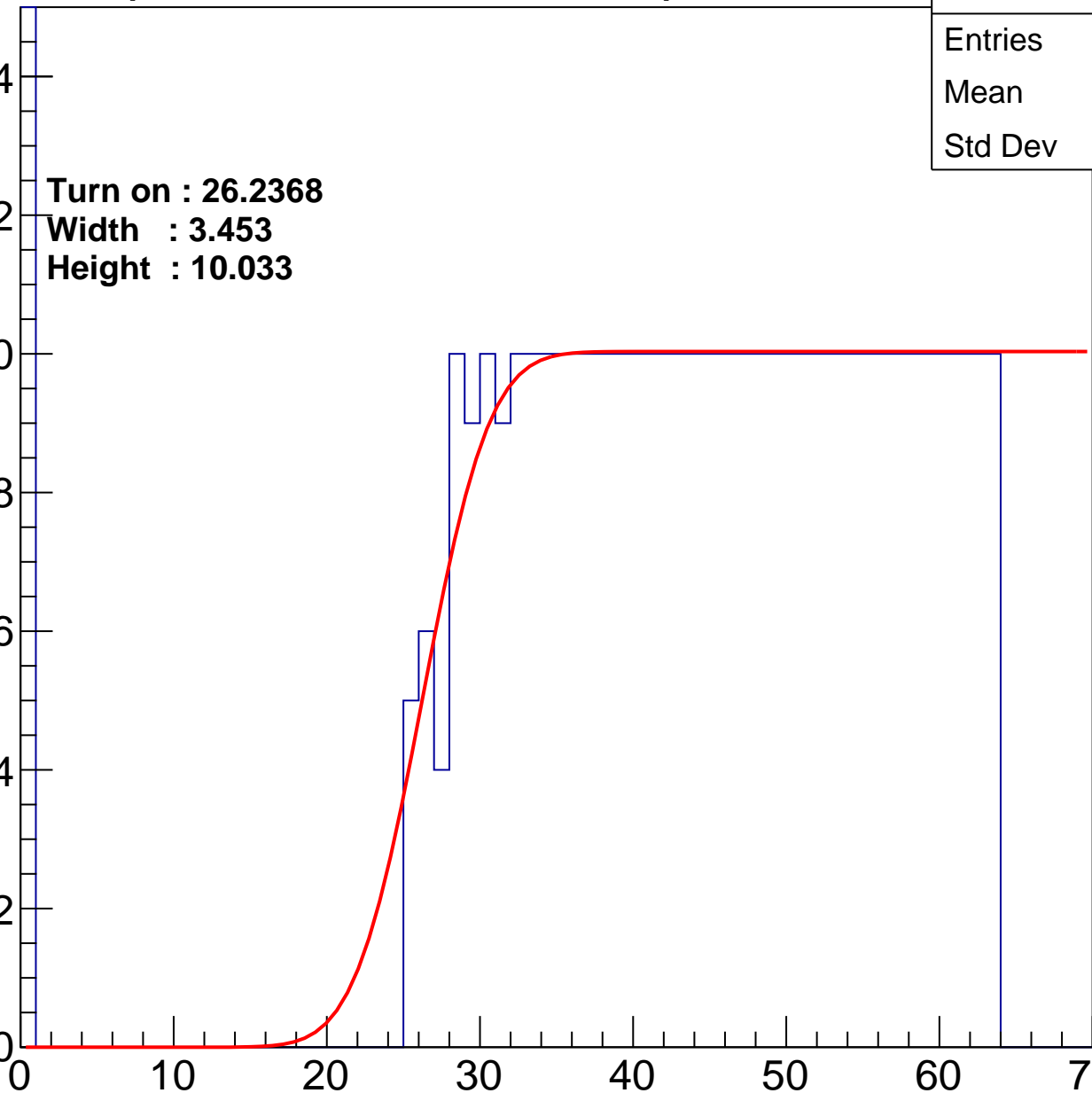
Width : 3.453

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch88

calib_packv5_041523_1651.root, FC#0, port C2

Entries	457
Mean	38.45
Std Dev	17.36

Turn on : 23.2112

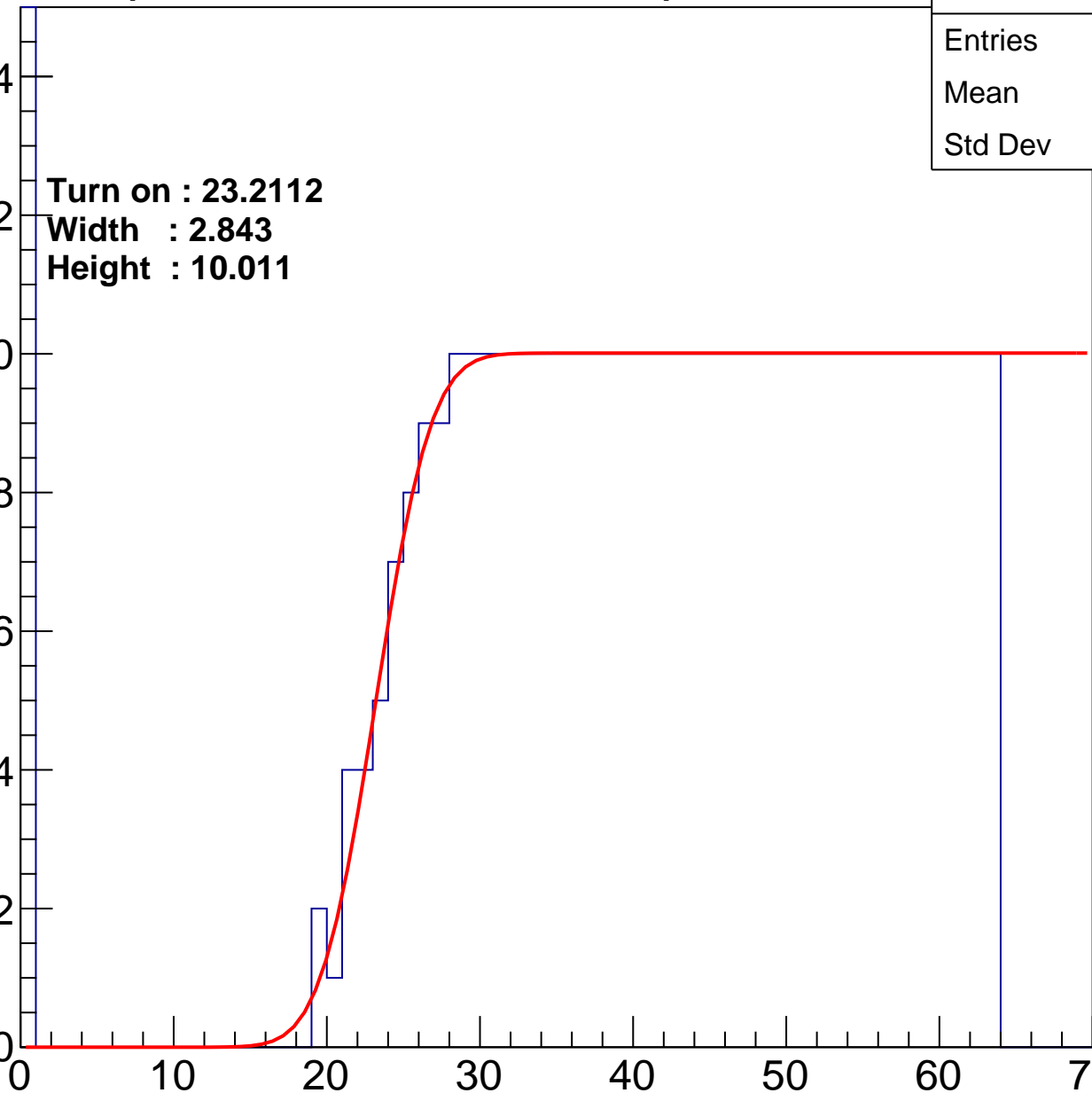
Width : 2.843

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch89

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	40.05
Std Dev	16.79

Turn on : 25.5573

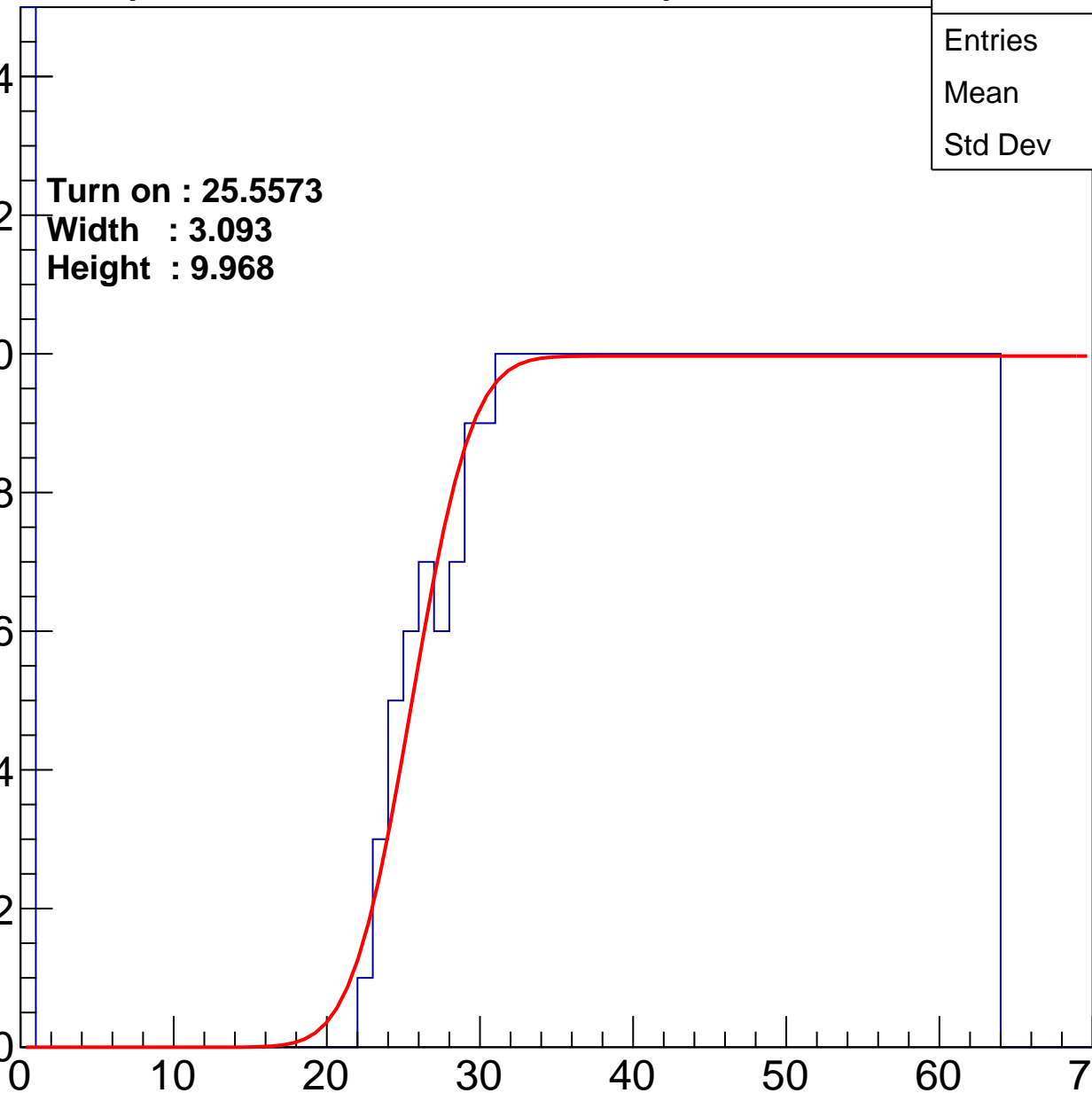
Width : 3.093

Height : 9.968

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch90

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	38.79
Std Dev	17.68

Turn on : 25.1045

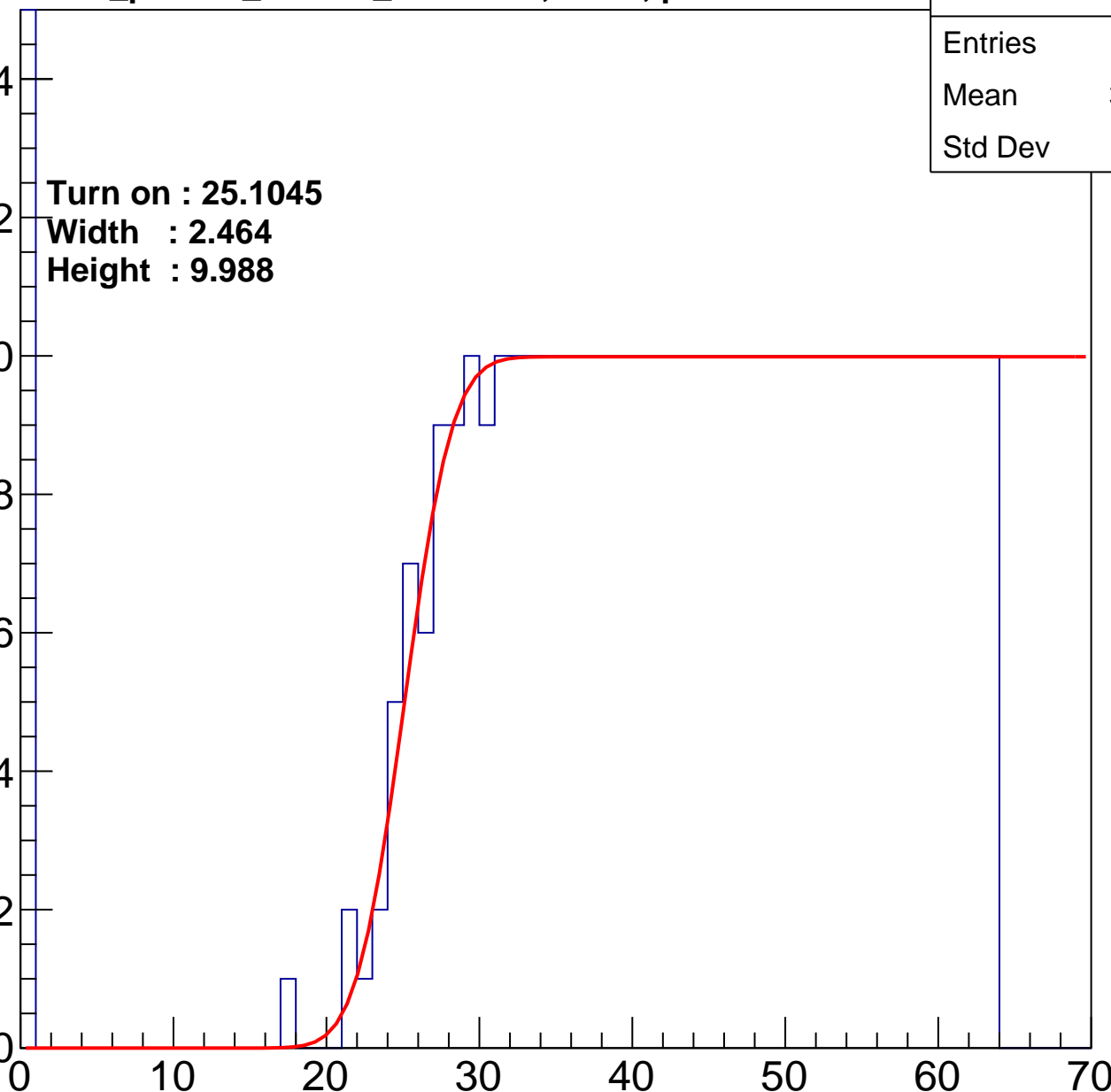
Width : 2.464

Height : 9.988

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch91

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	39.44
Std Dev	17.56

Turn on : 26.6669

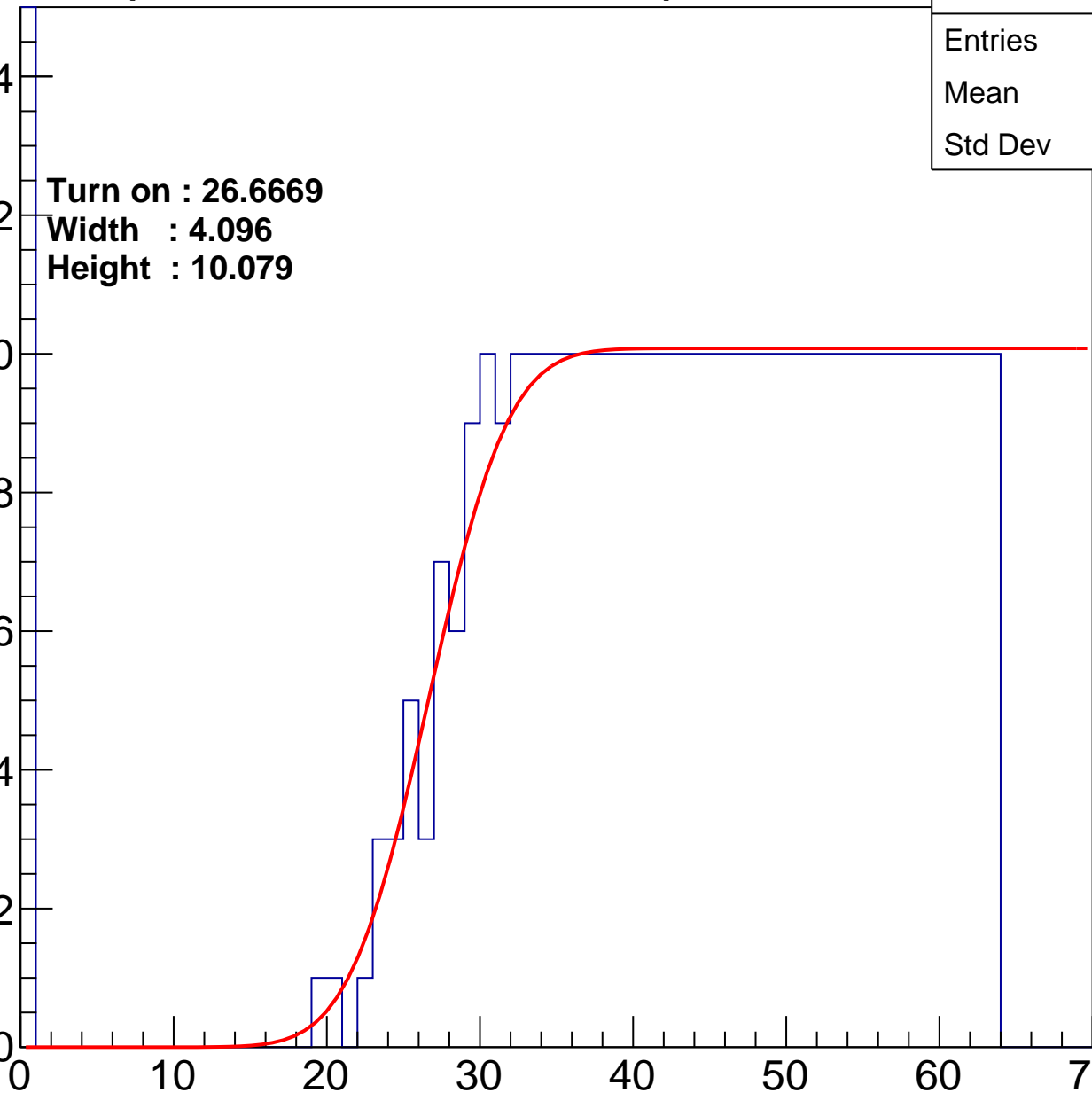
Width : 4.096

Height : 10.079

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch92

calib_packv5_041523_1651.root, FC#0, port C2

Entries	459
Mean	38.46
Std Dev	17.22

Turn on : 22.7656

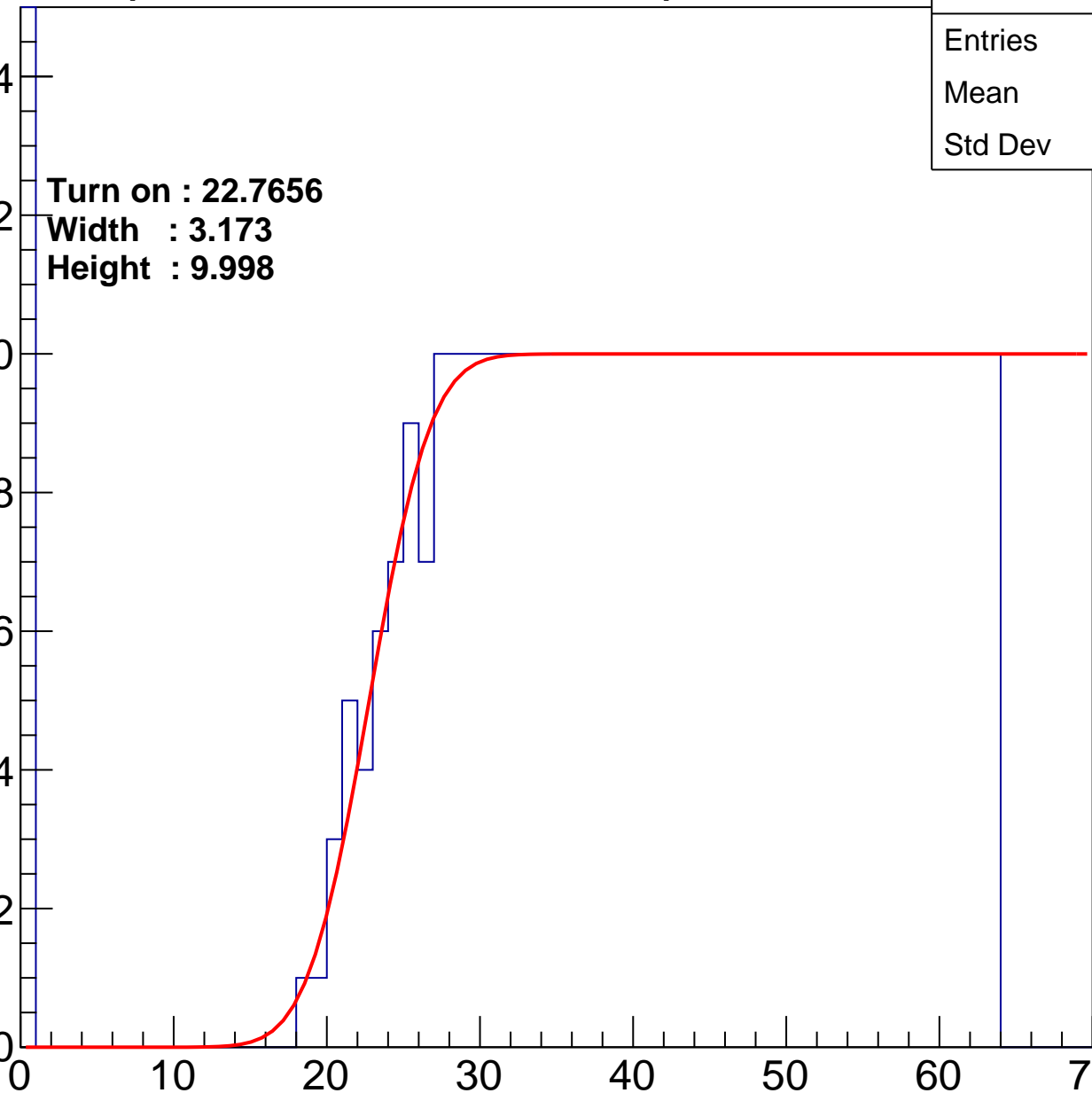
Width : 3.173

Height : 9.998

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch93

calib_packv5_041523_1651.root, FC#0, port C2

Entries	425
Mean	39.78
Std Dev	17.09

Turn on : 25.7849

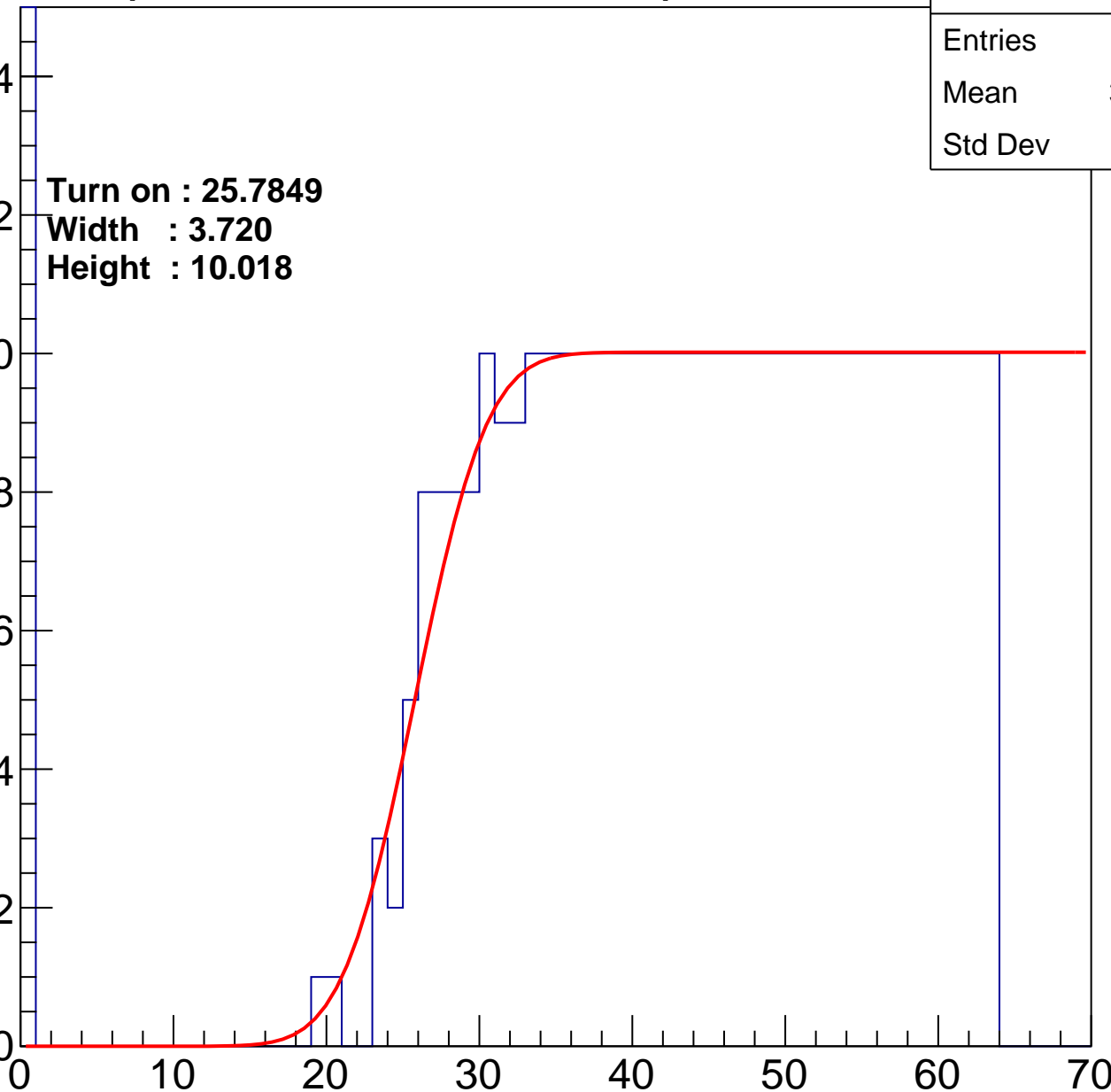
Width : 3.720

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch94

calib_packv5_041523_1651.root, FC#0, port C2

Entries	411
Mean	40.49
Std Dev	16.83

Turn on : 27.2895

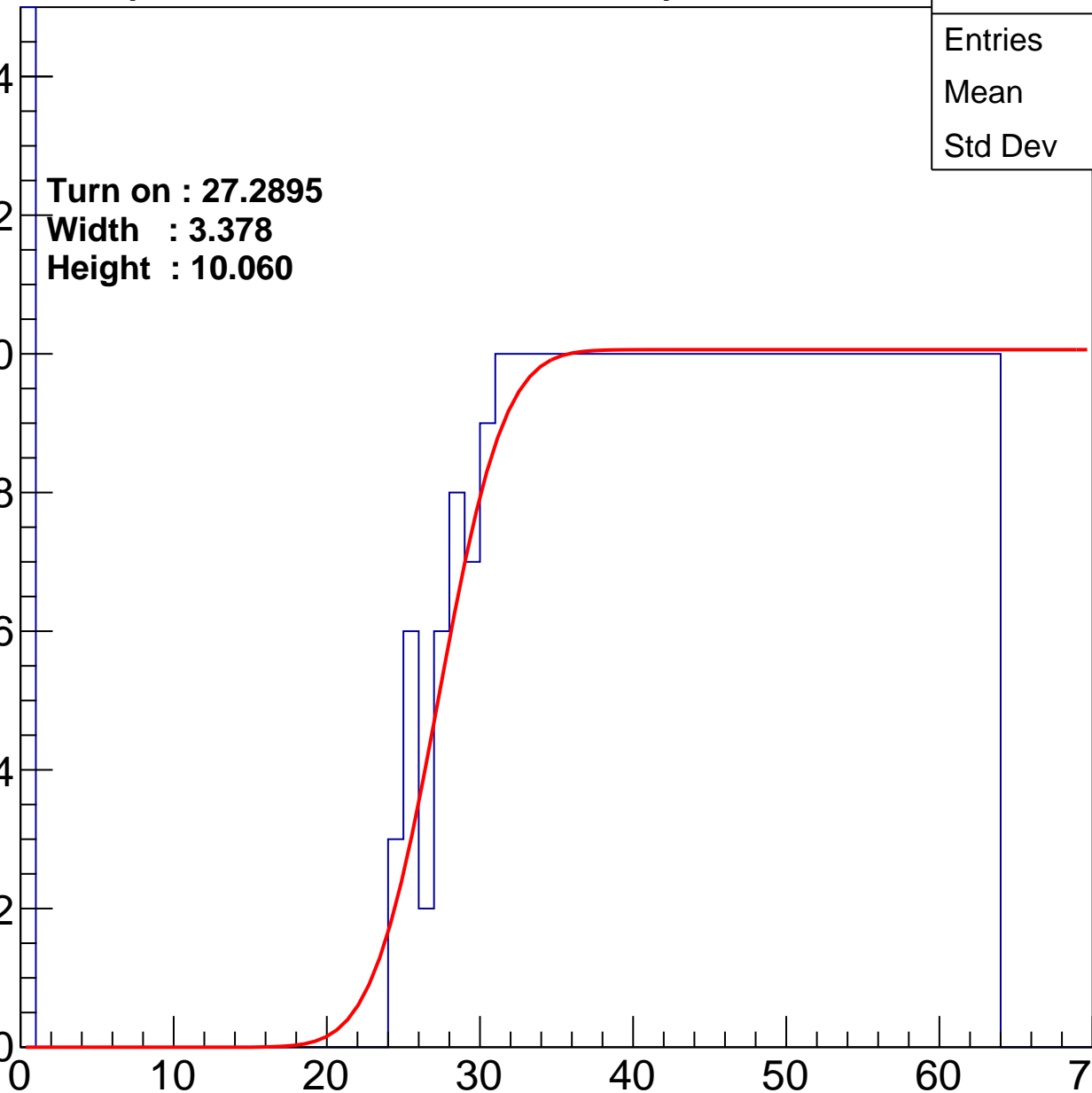
Width : 3.378

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch95

calib_packv5_041523_1651.root, FC#0, port C2

Entries	403
Mean	41.01
Std Dev	16.46

Turn on : 27.6750

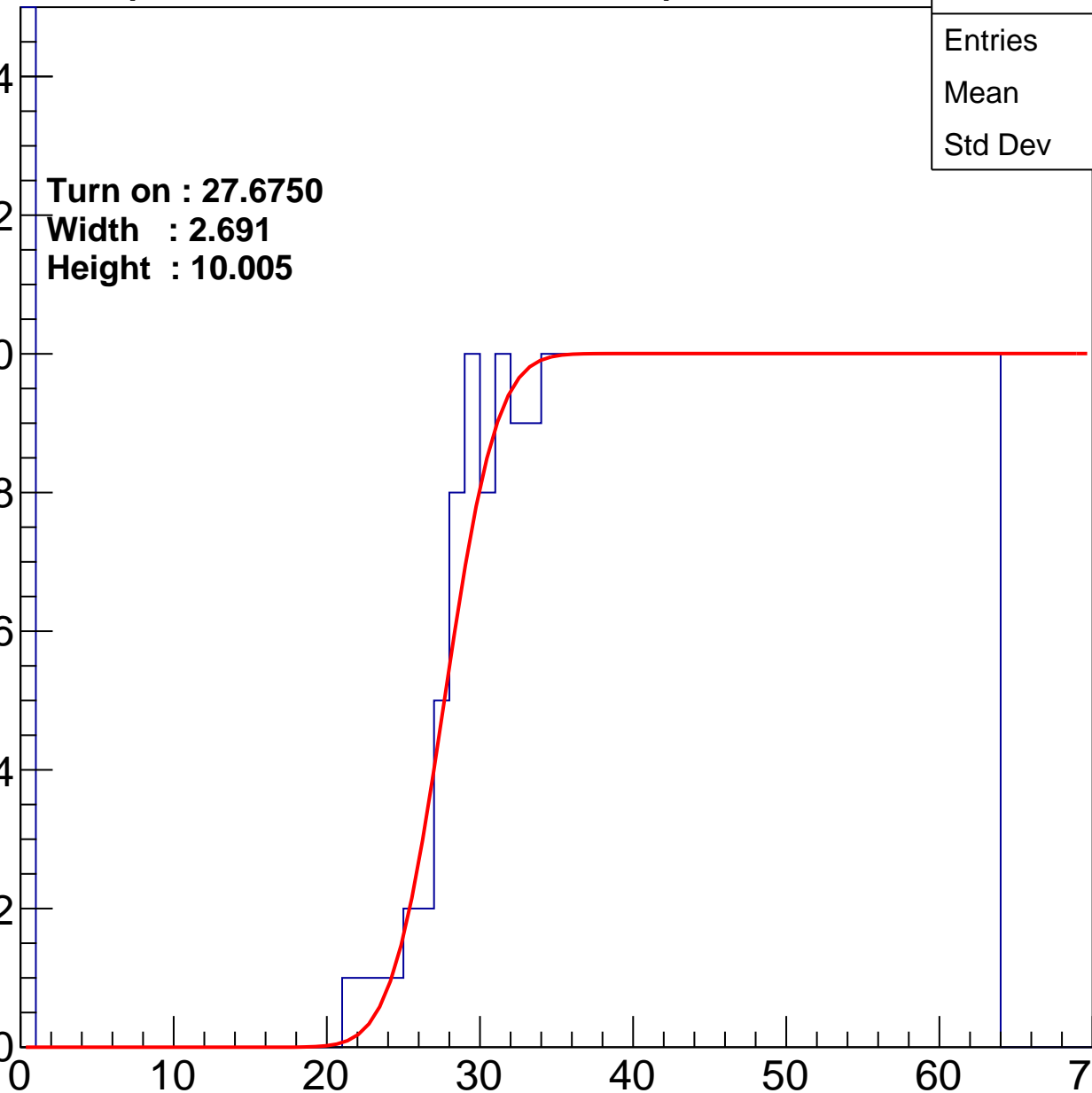
Width : 2.691

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch96

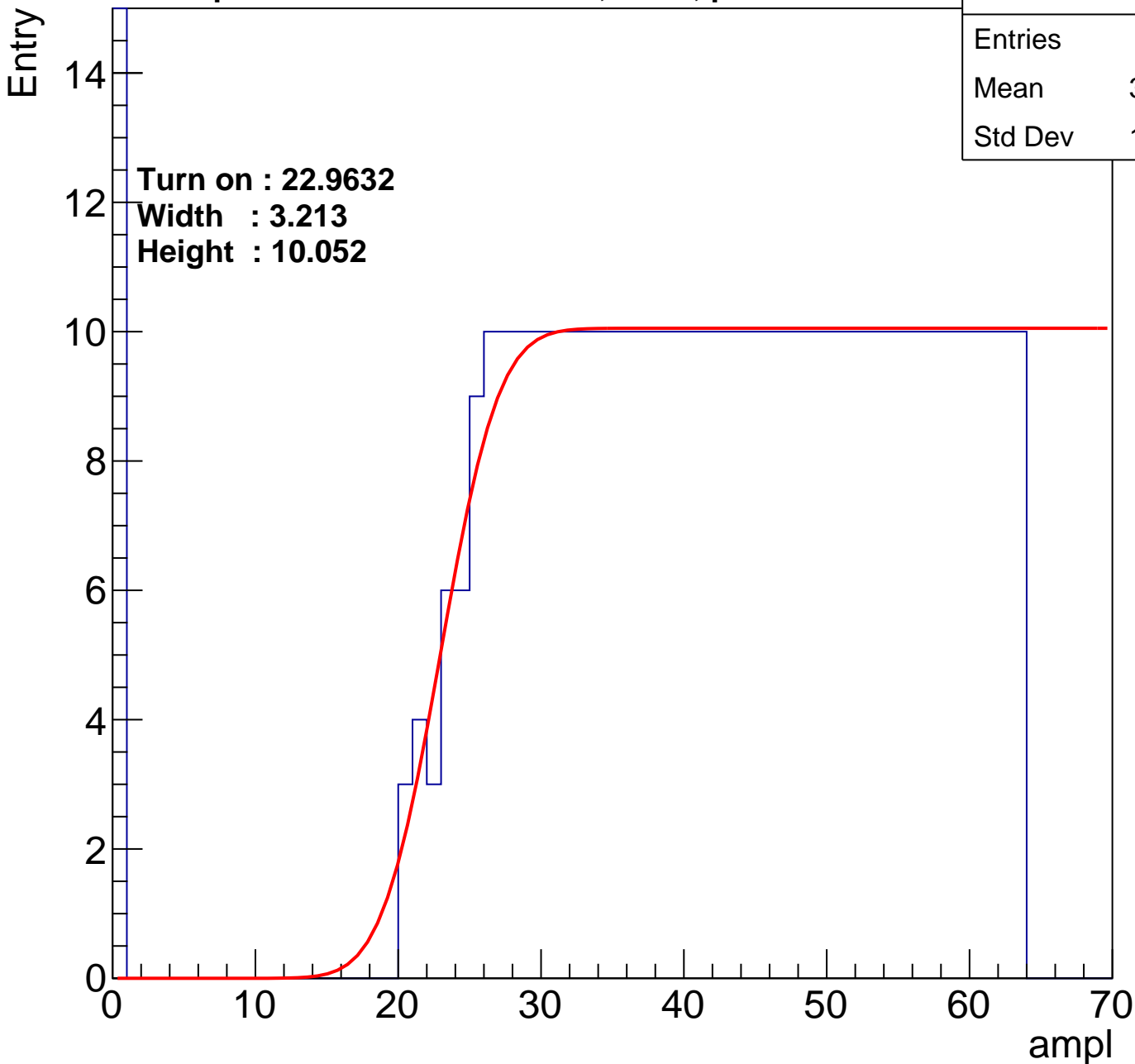
calib_packv5_041523_1651.root, FC#0, port C2

Entries	467
Mean	37.75
Std Dev	17.89

Turn on : 22.9632

Width : 3.213

Height : 10.052



B1L103S, U7-ch97

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	40.04
Std Dev	16.39

Turn on : 24.8250

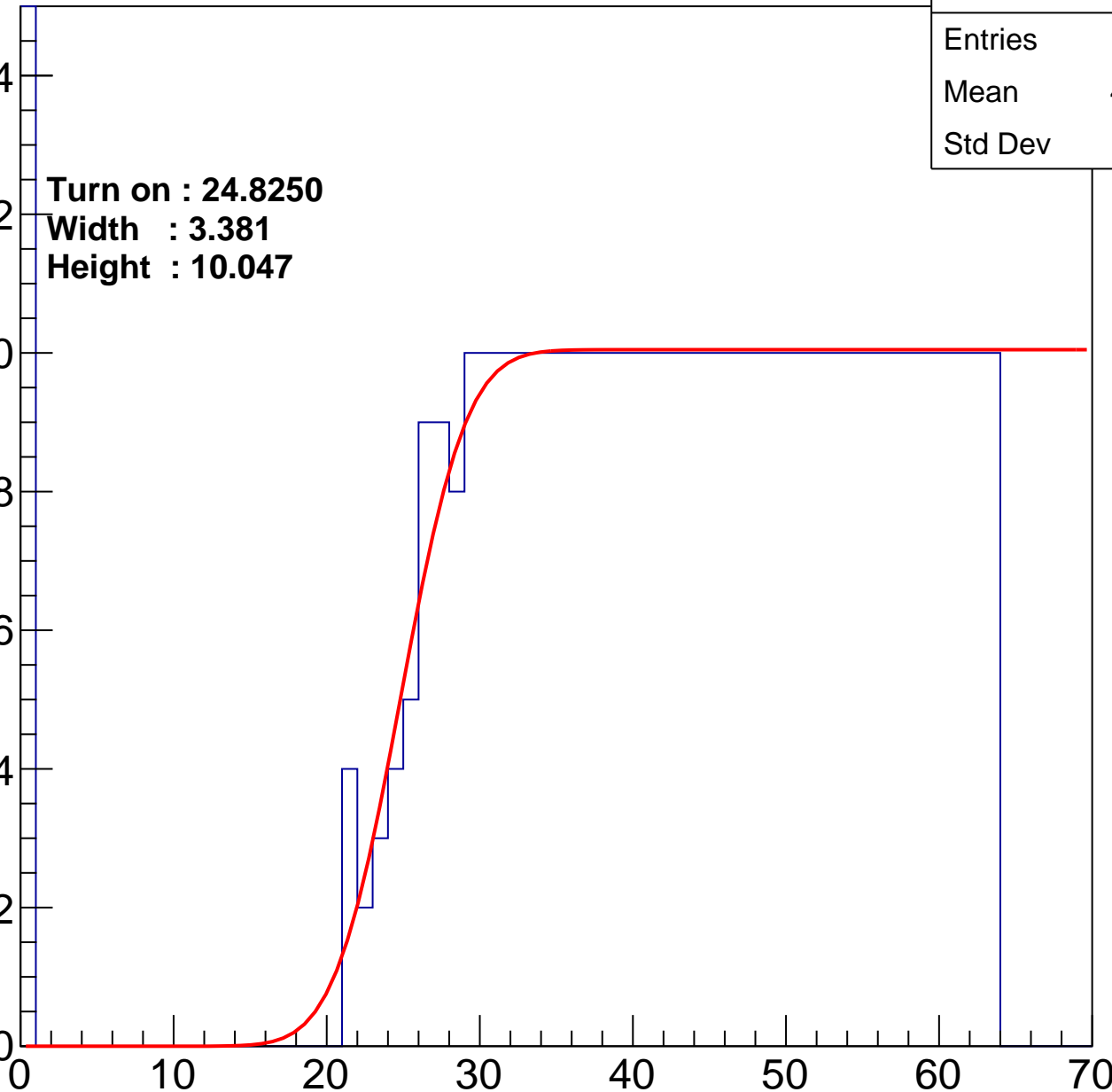
Width : 3.381

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch98

calib_packv5_041523_1651.root, FC#0, port C2

Entries	454
Mean	38.54
Std Dev	17.41

Turn on : 24.8304

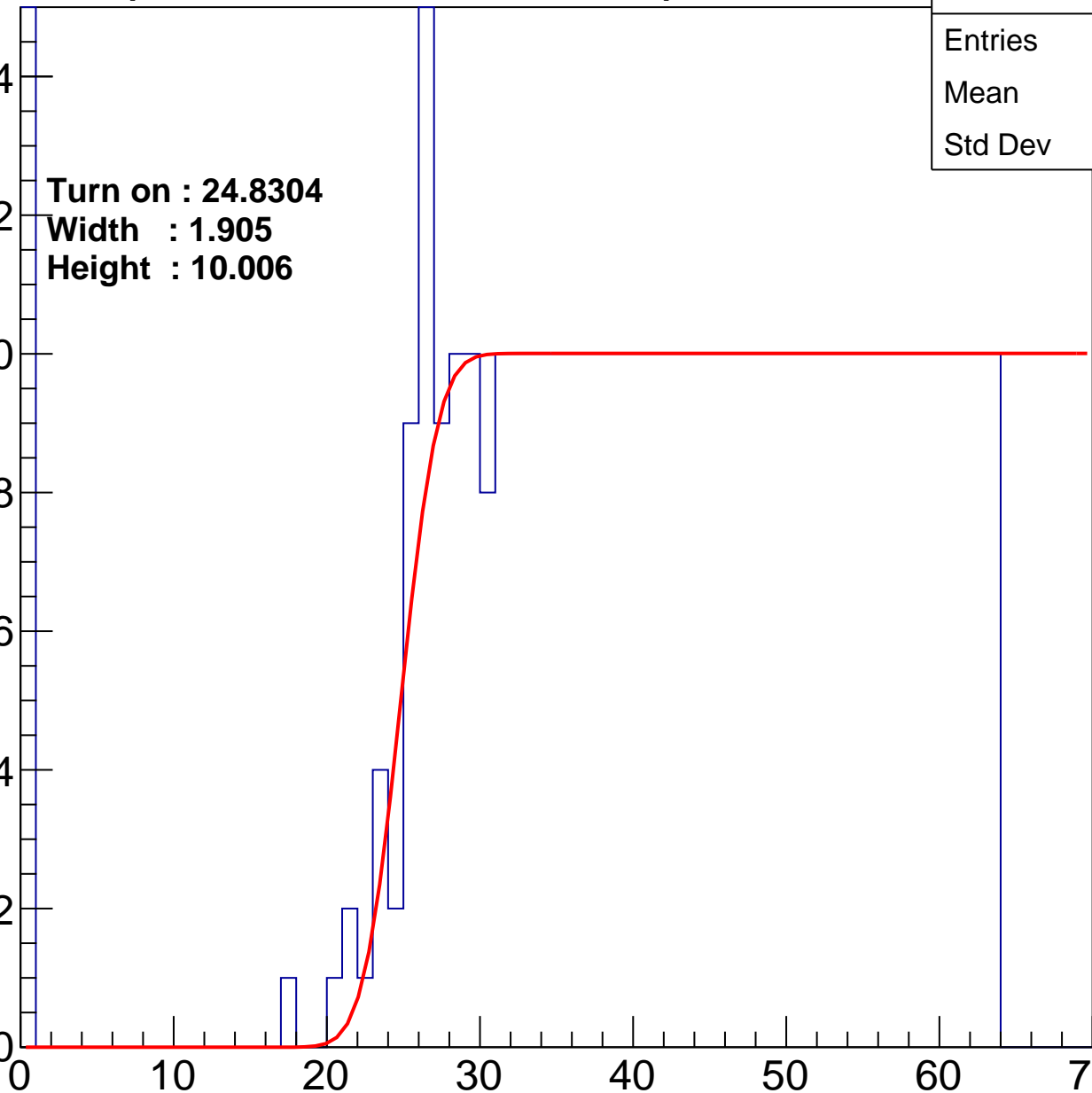
Width : 1.905

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch99

calib_packv5_041523_1651.root, FC#0, port C2

Entries	444
Mean	38.48
Std Dev	18.04

Turn on : 25.3302

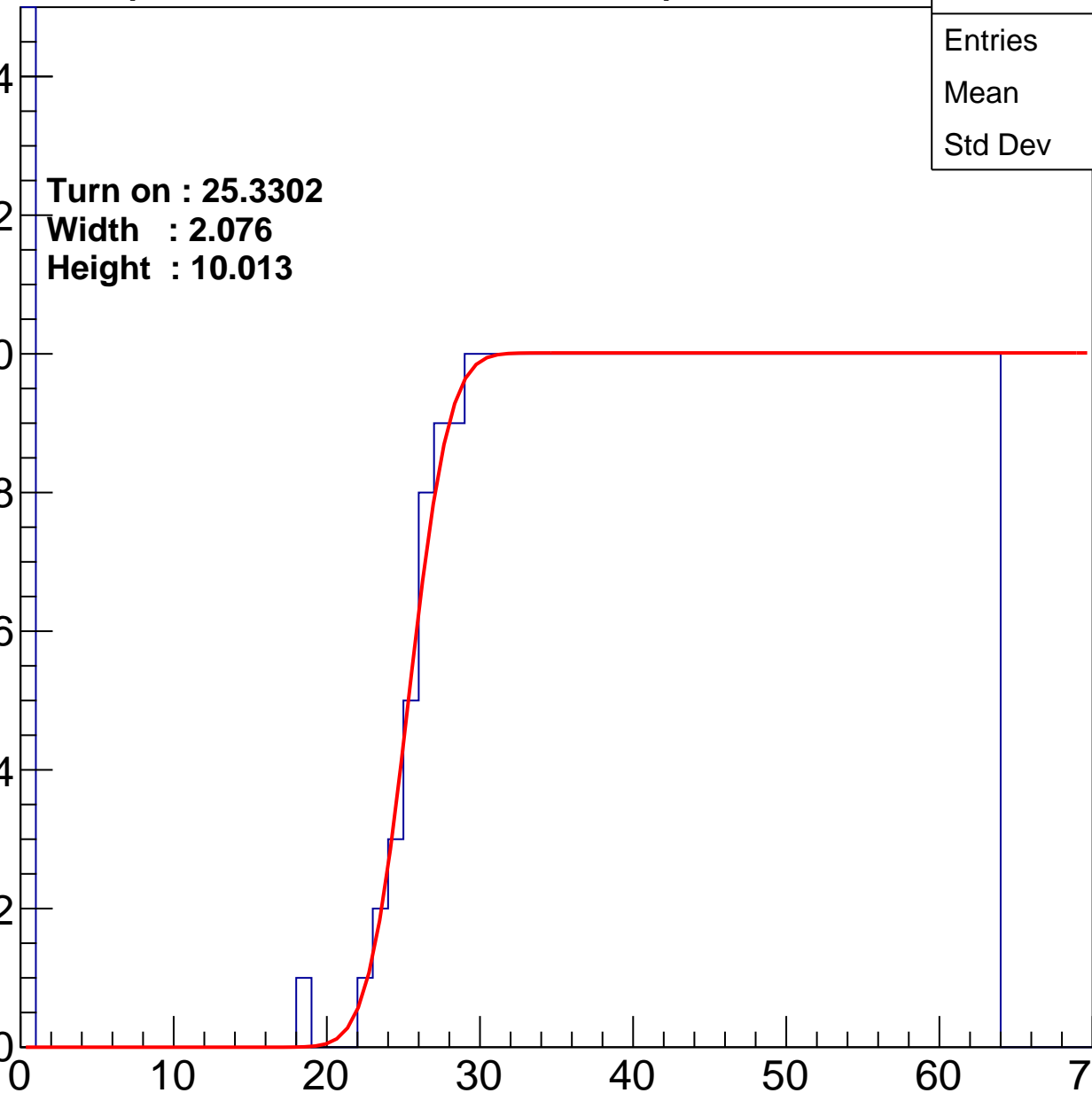
Width : 2.076

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch100

calib_packv5_041523_1651.root, FC#0, port C2

Entries	453
Mean	37.66
Std Dev	18.69

Turn on : 25.3794

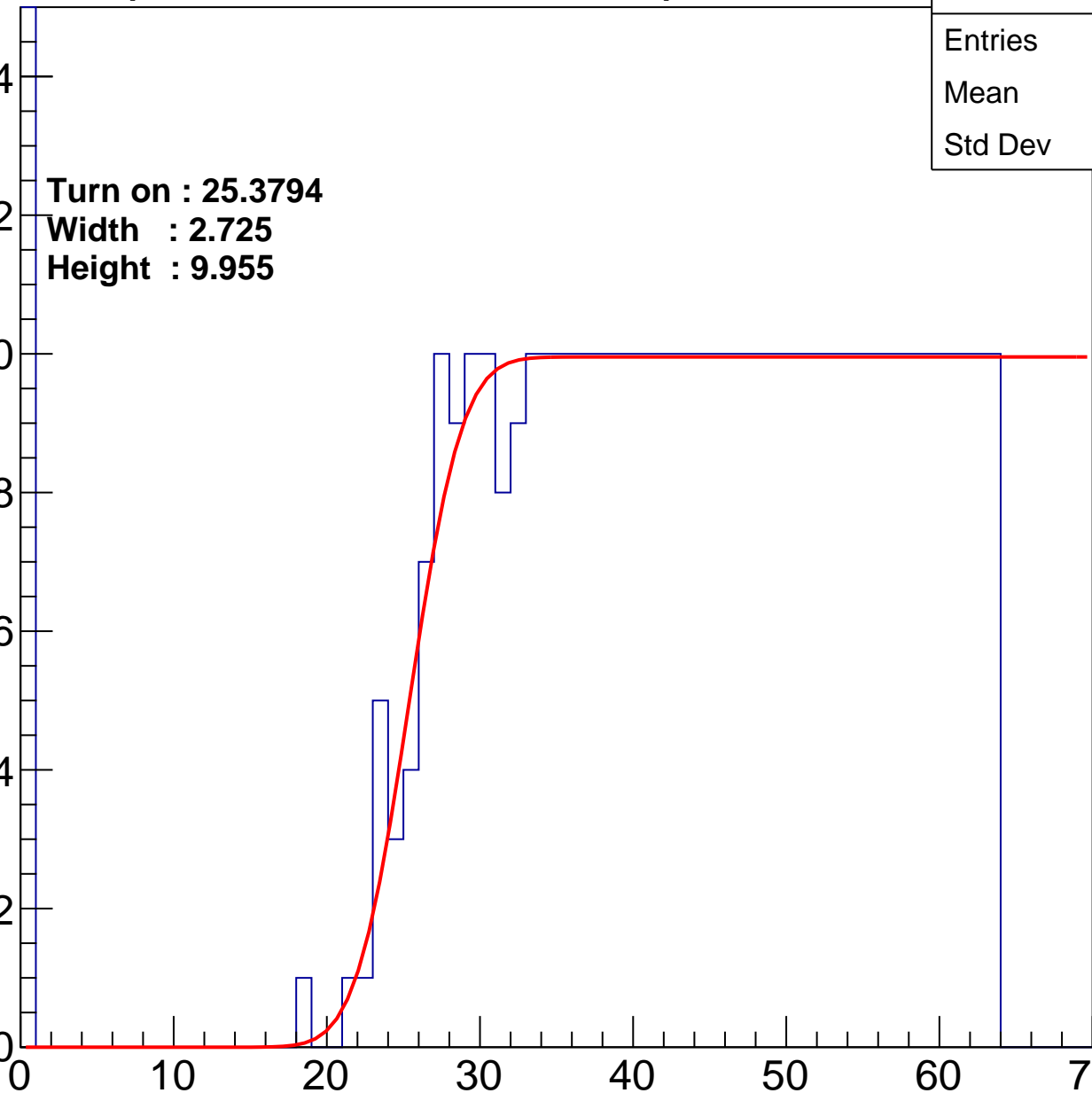
Width : 2.725

Height : 9.955

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch101

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	39.3
Std Dev	17.01

Turn on : 24.5872

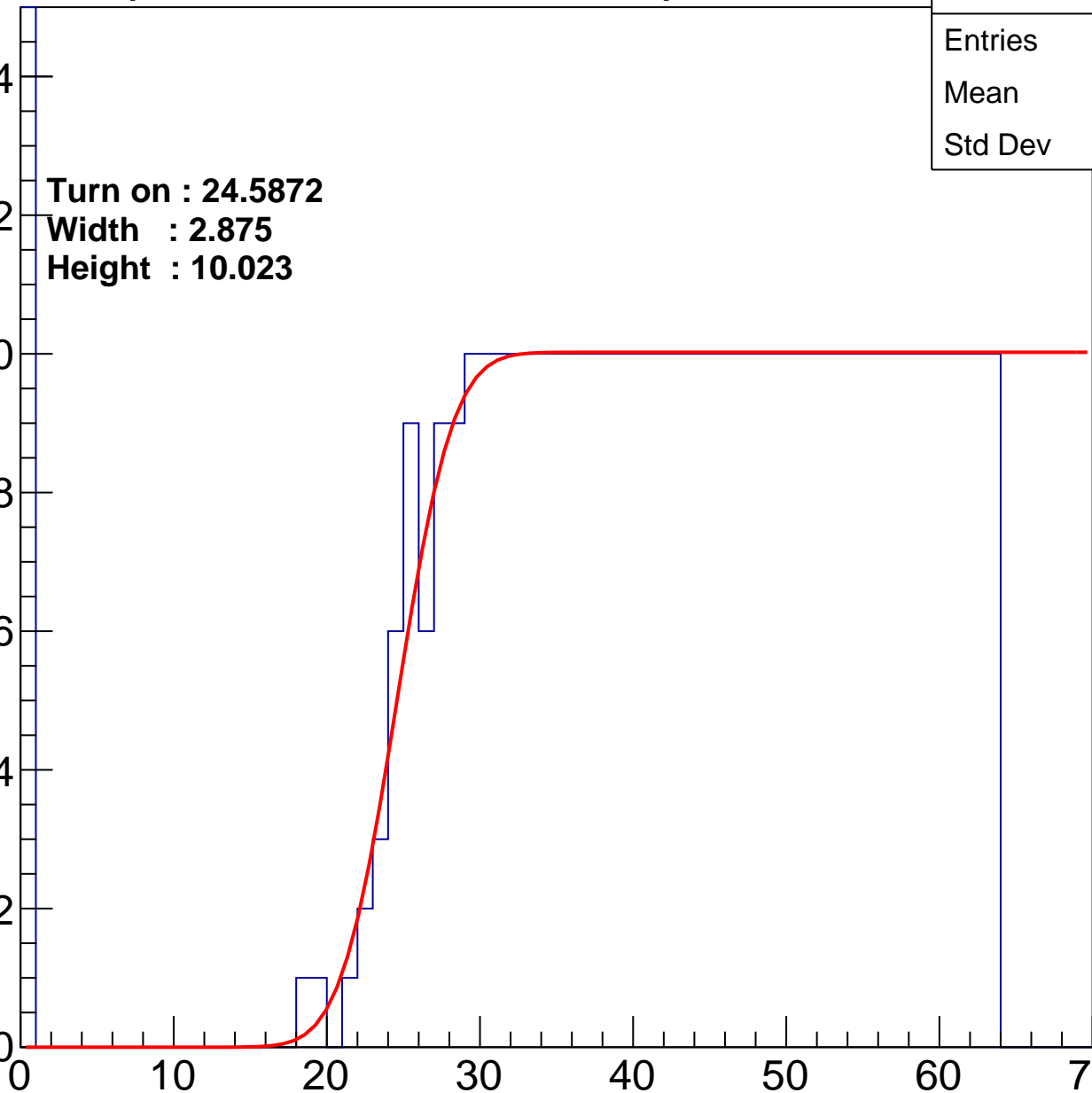
Width : 2.875

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch102

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	38.99
Std Dev	17.32

Turn on : 24.6441

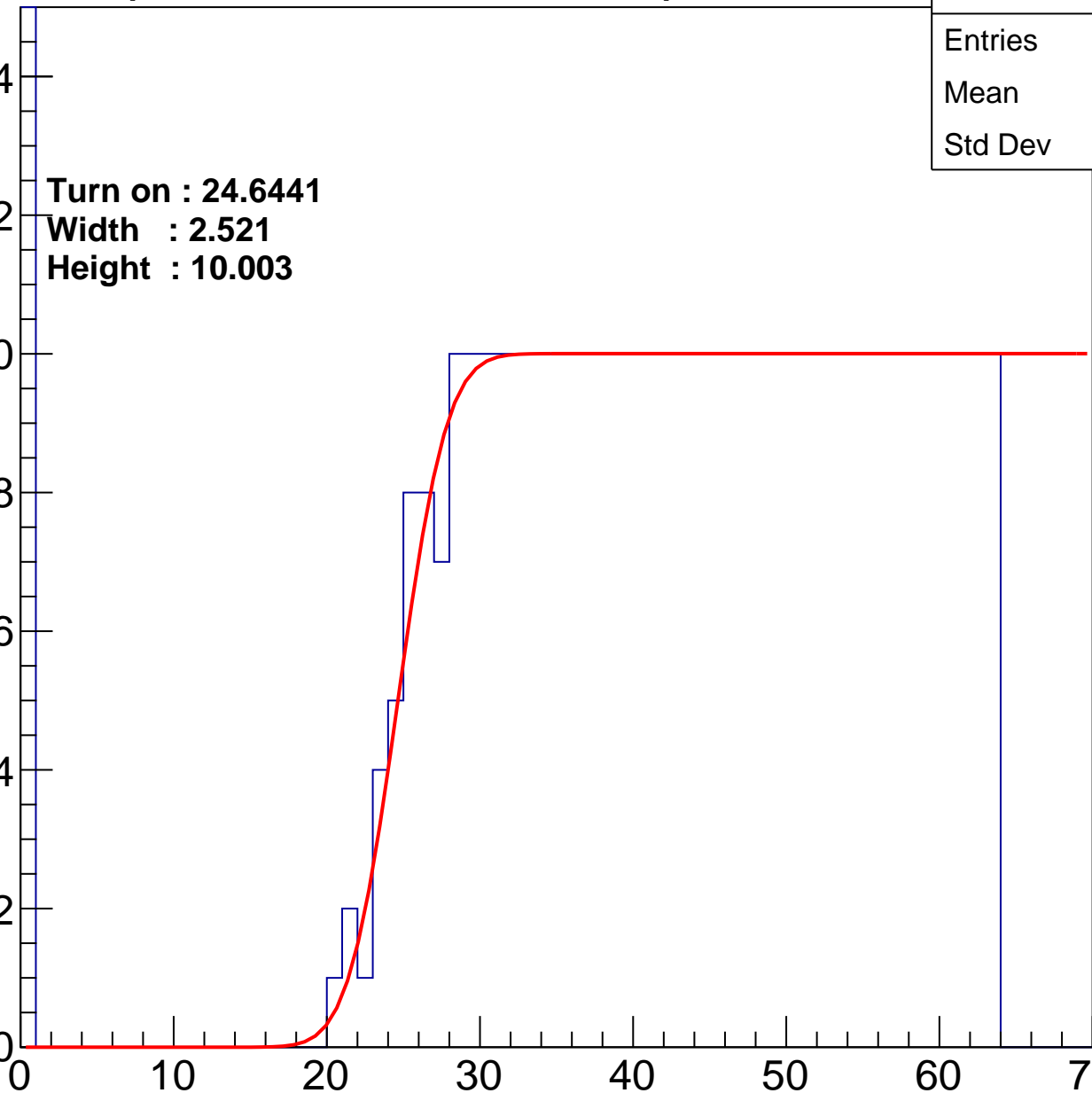
Width : 2.521

Height : 10.003

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch103

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	39.24
Std Dev	17.45

Turn on : 25.2467

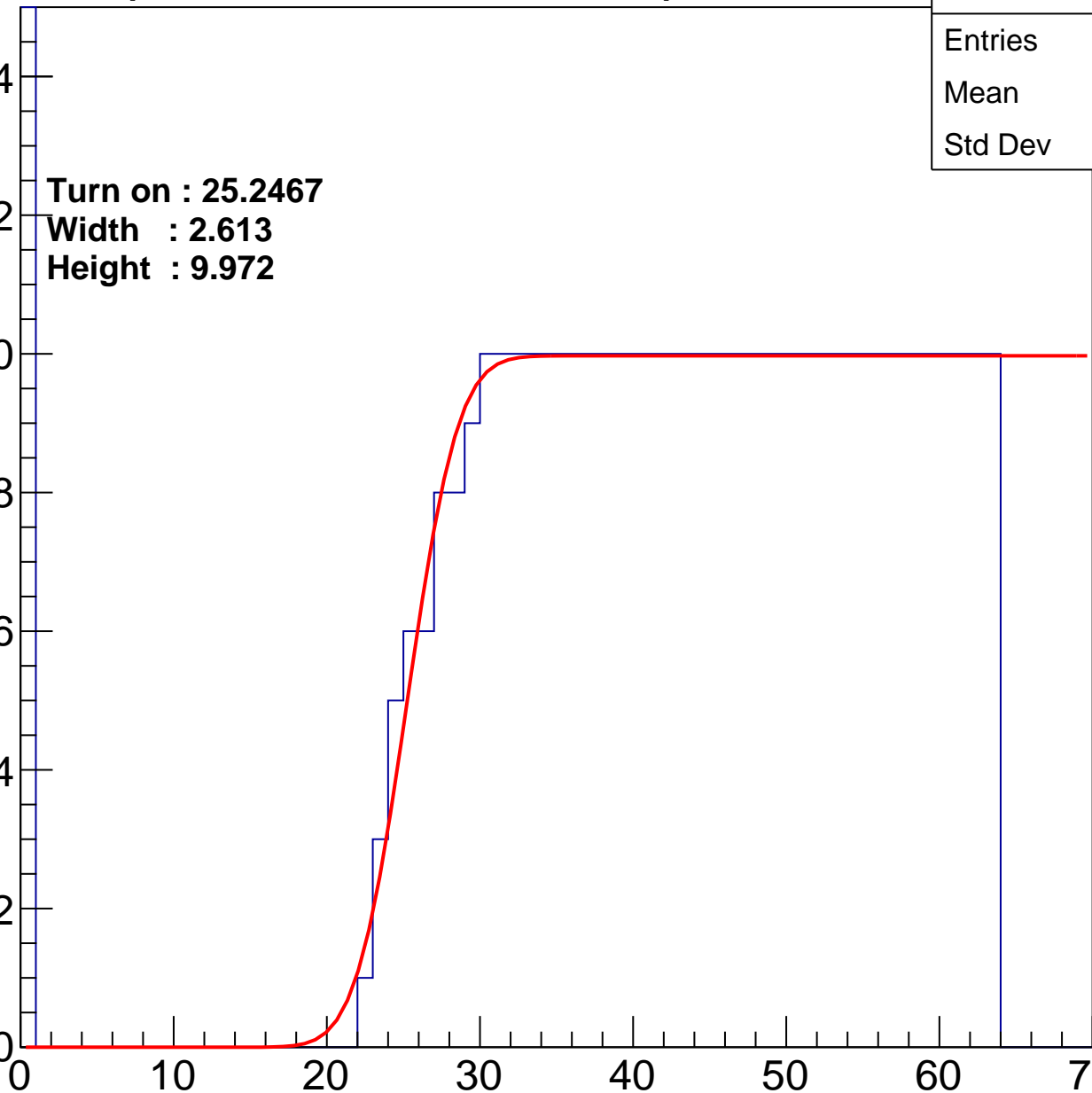
Width : 2.613

Height : 9.972

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch104

calib_packv5_041523_1651.root, FC#0, port C2

Entries	427
Mean	39.95
Std Dev	16.71

Turn on : 25.7826

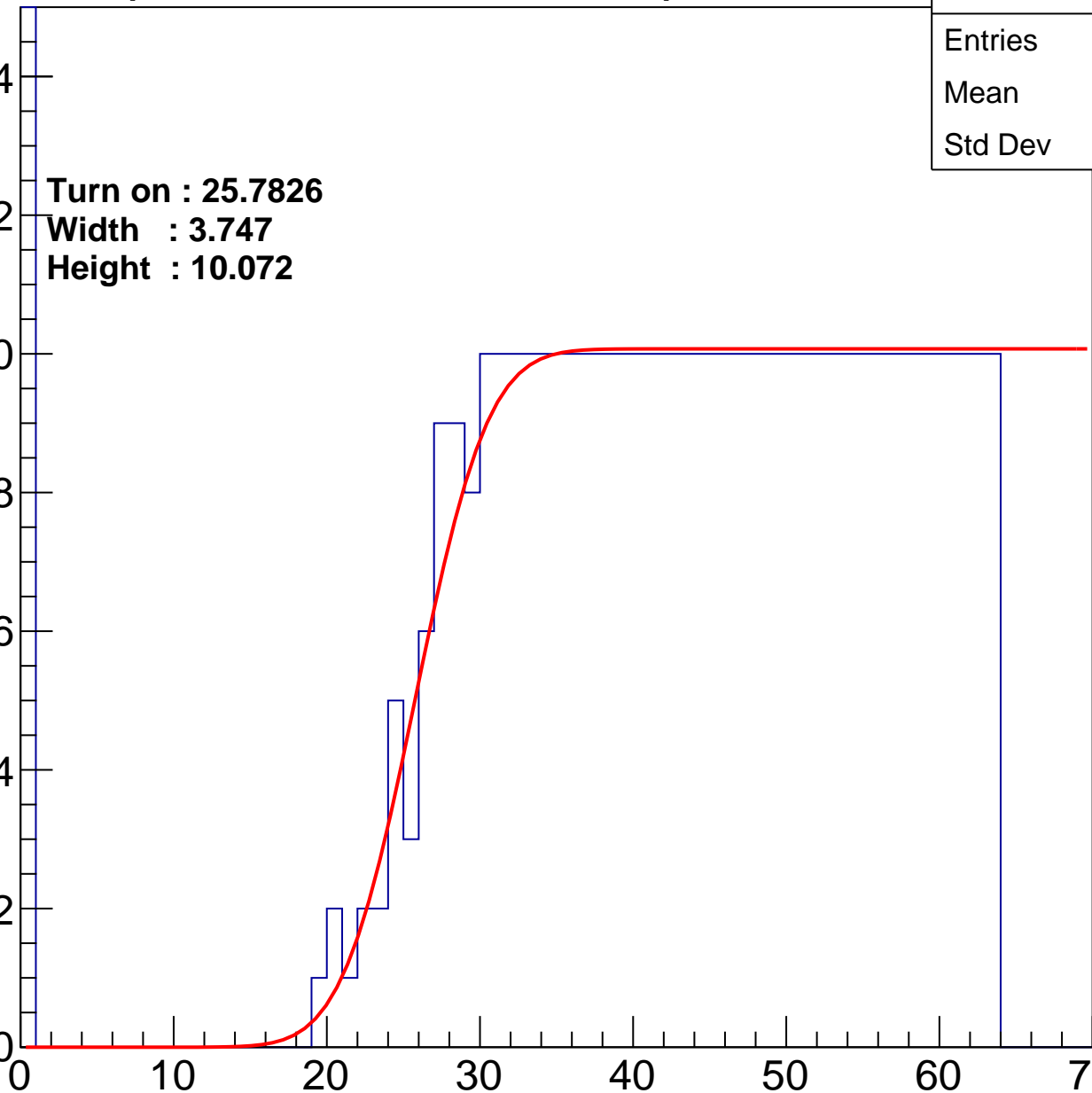
Width : 3.747

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch105

calib_packv5_041523_1651.root, FC#0, port C2

Entries	427
Mean	39.91
Std Dev	16.78

Turn on : 25.2547

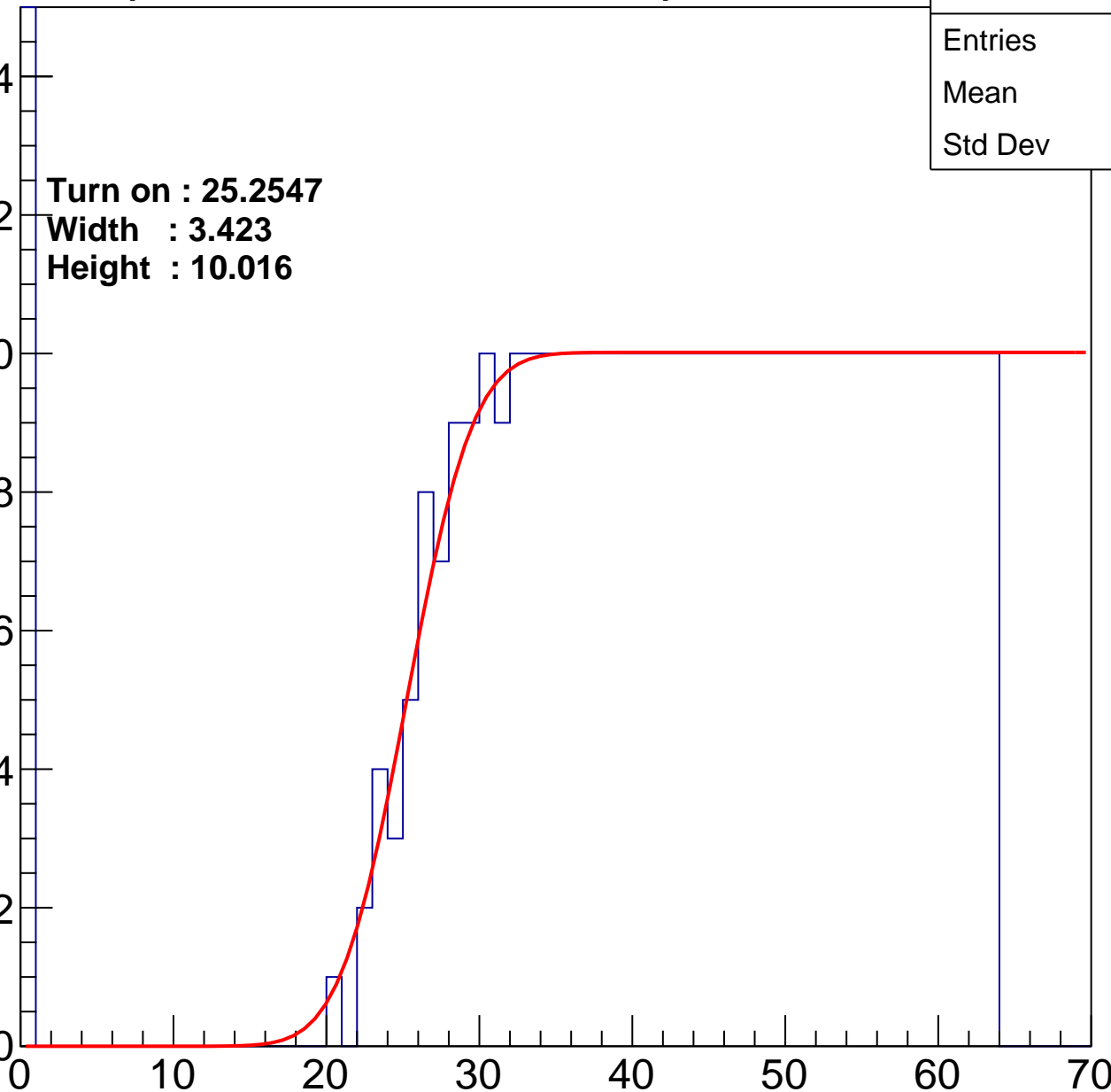
Width : 3.423

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch106

calib_packv5_041523_1651.root, FC#0, port C2

Entries	454
Mean	38.23
Std Dev	17.81

Turn on : 24.6087

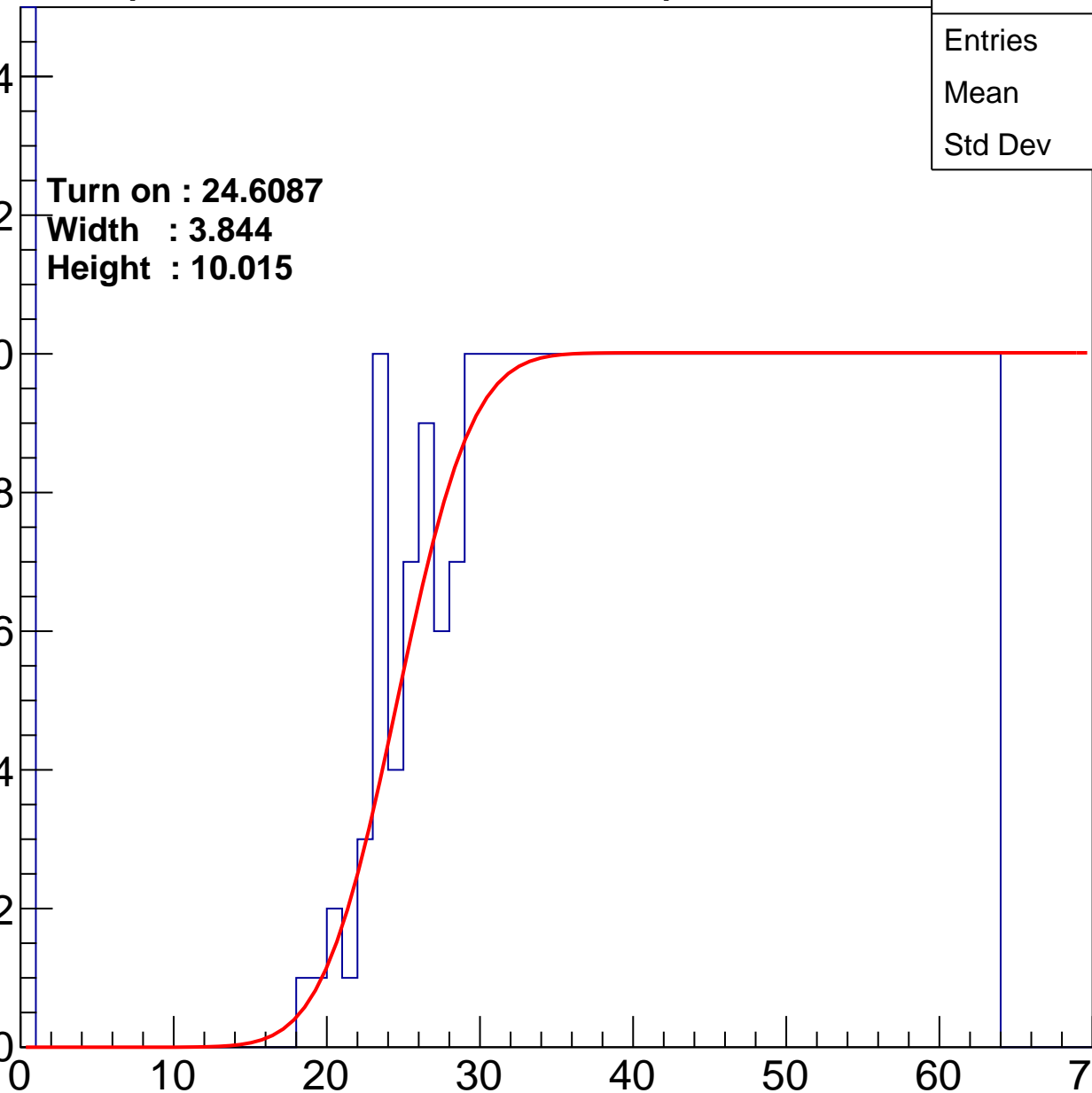
Width : 3.844

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch107

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	39.4
Std Dev	17.95

Turn on : 27.1644

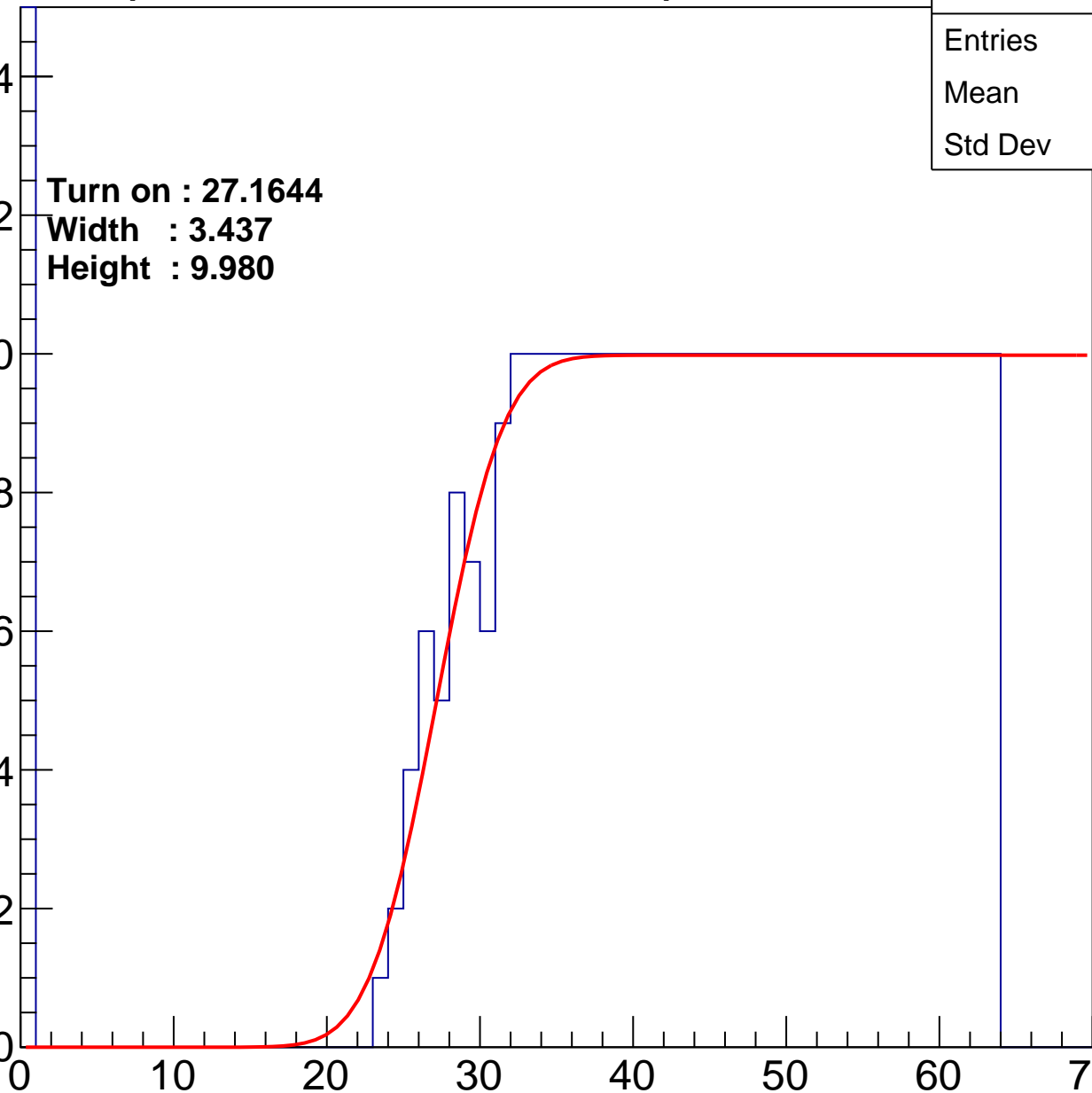
Width : 3.437

Height : 9.980

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch108

calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	39.11
Std Dev	17.67

Turn on : 26.2945

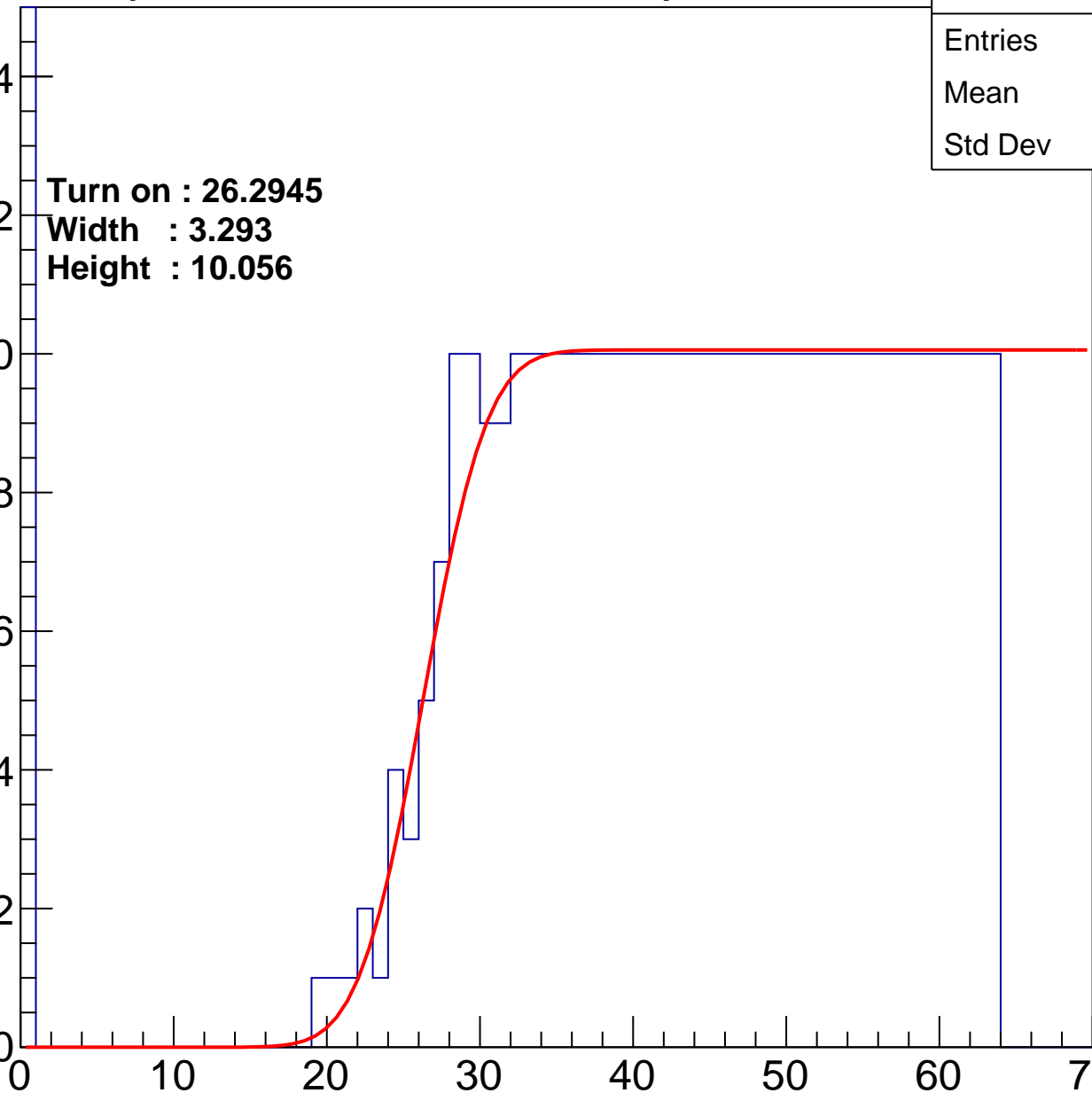
Width : 3.293

Height : 10.056

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch109

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	39.59
Std Dev	17.13

Turn on : 25.5989

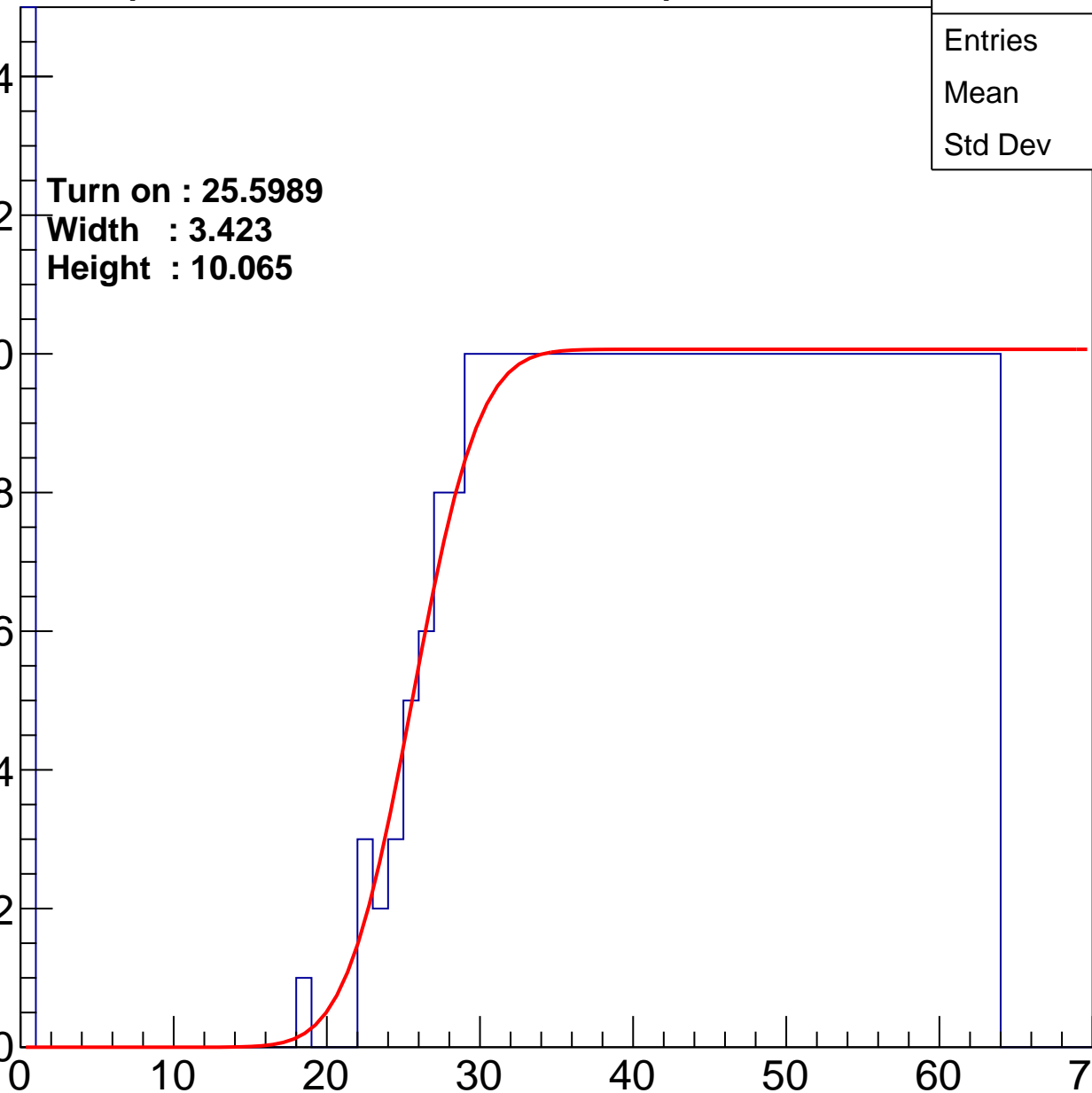
Width : 3.423

Height : 10.065

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch110

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	39.14
Std Dev	17.79

Turn on : 26.3399

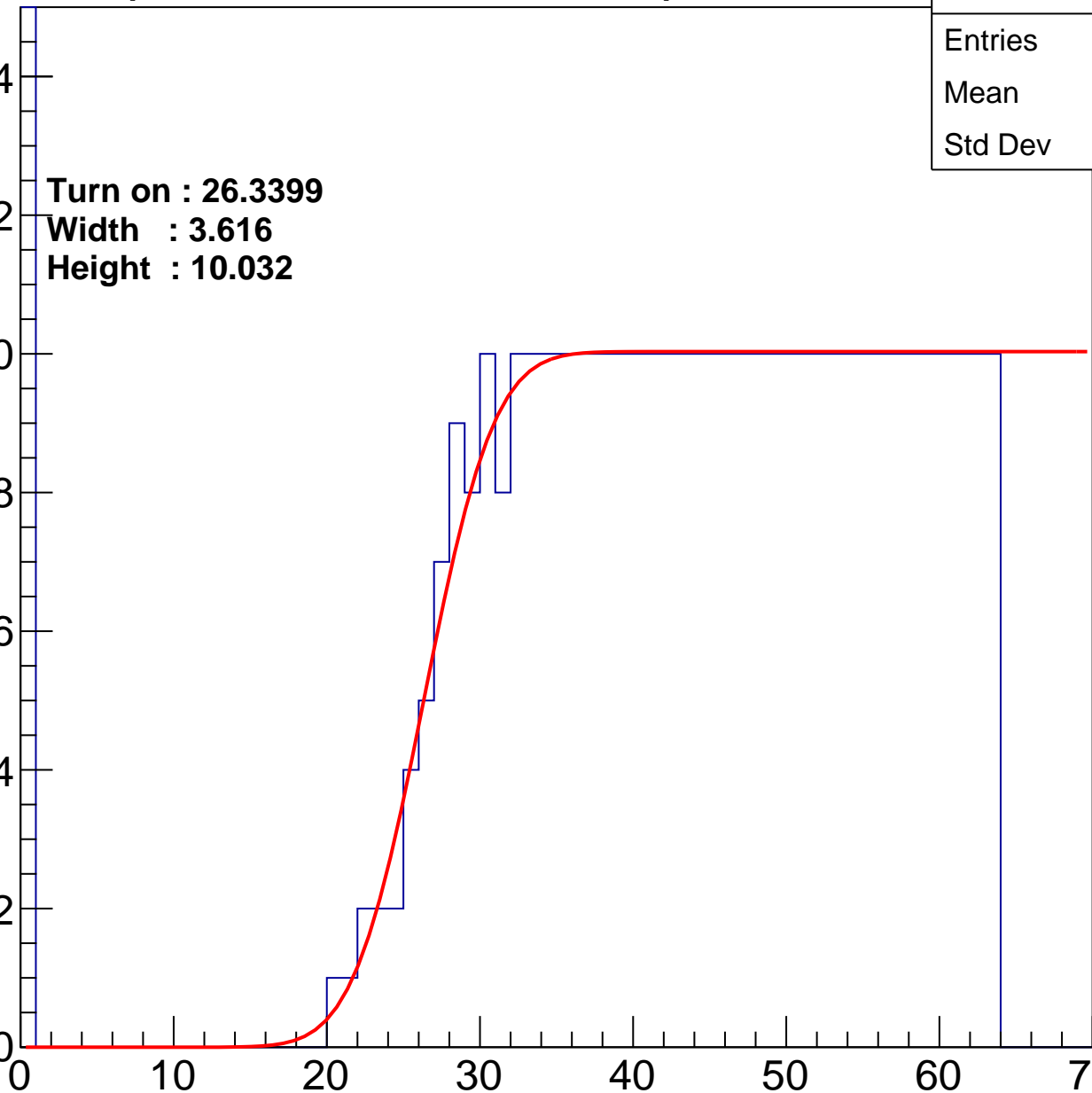
Width : 3.616

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch111

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	40.29
Std Dev	16.83

Turn on : 26.4743

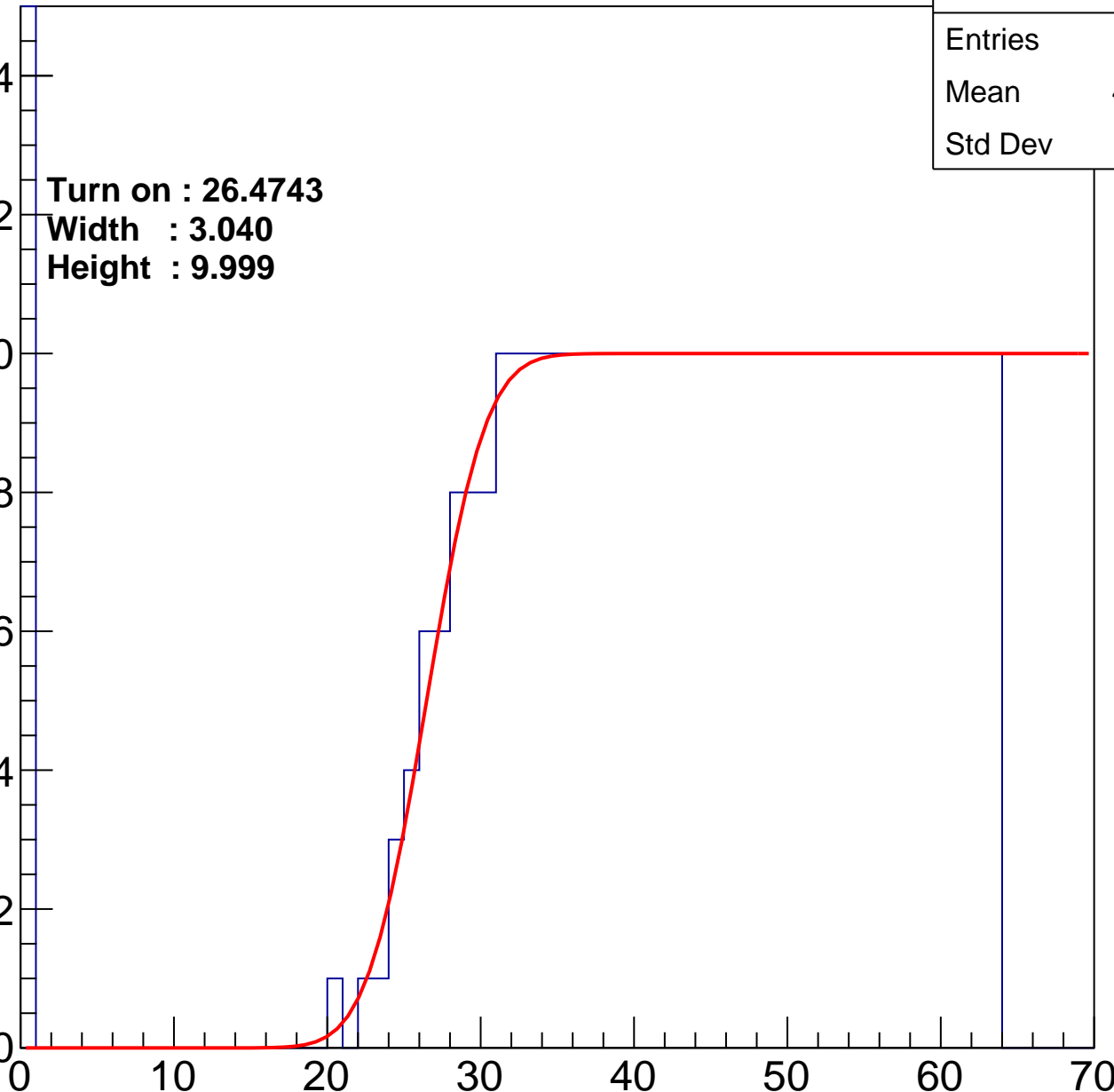
Width : 3.040

Height : 9.999

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch112

calib_packv5_041523_1651.root, FC#0, port C2

Entries	427
Mean	39.93
Std Dev	16.72

Turn on : 25.0151

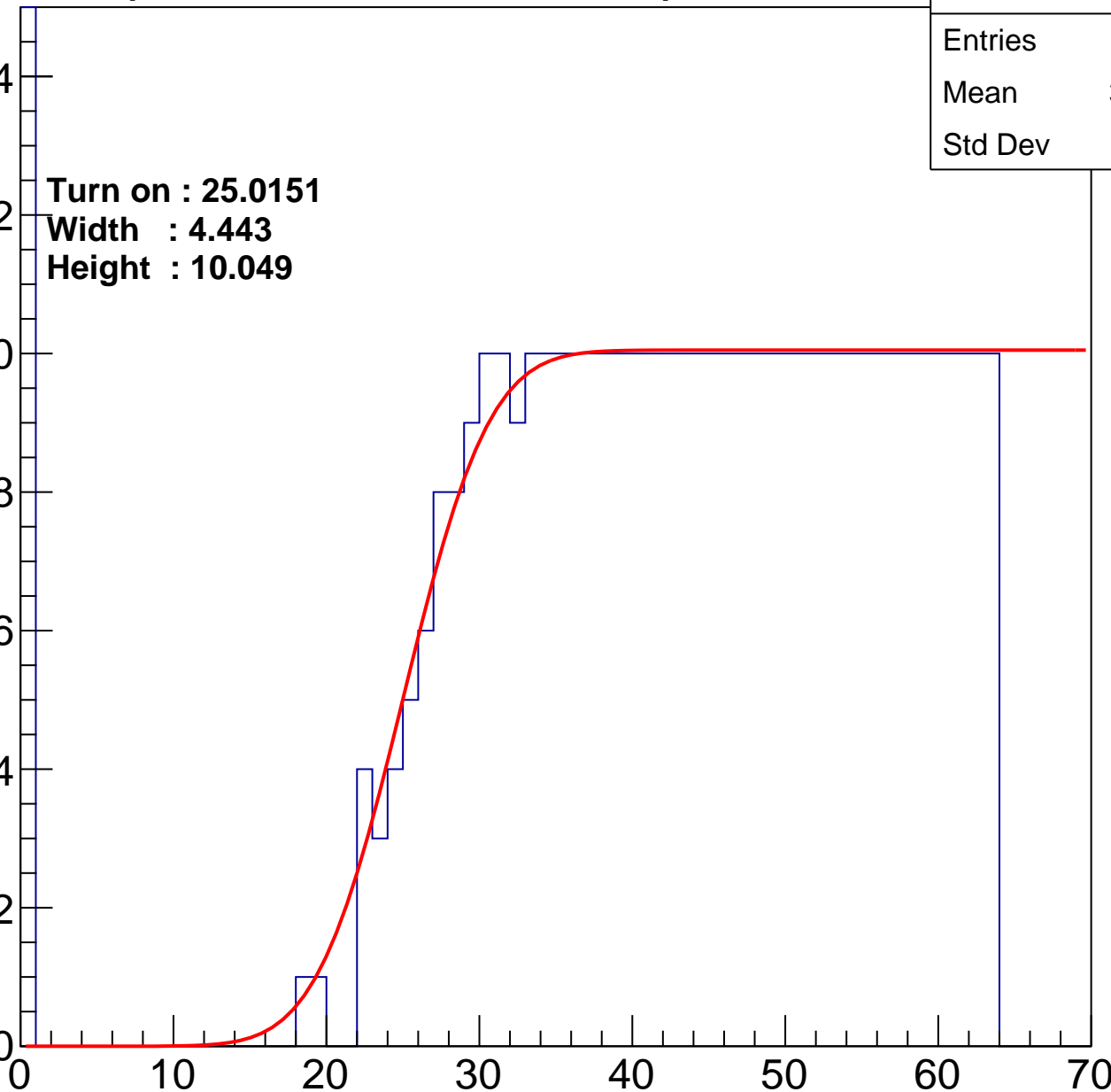
Width : 4.443

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch113

calib_packv5_041523_1651.root, FC#0, port C2

Entries	456
Mean	38.06
Std Dev	17.99

Turn on : 23.9473

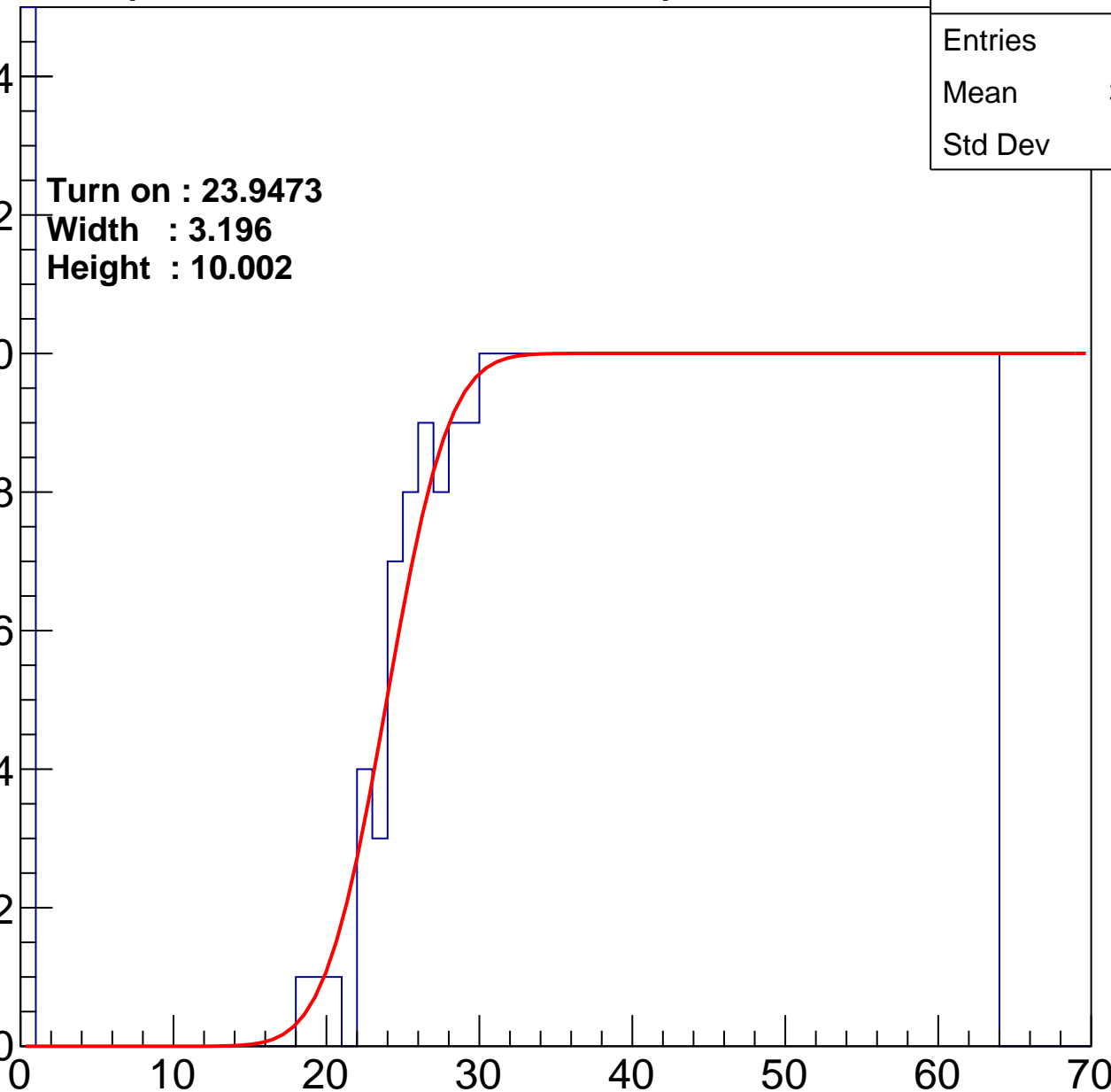
Width : 3.196

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch114

calib_packv5_041523_1651.root, FC#0, port C2

Entries	455
Mean	37.97
Std Dev	18.16

Turn on : 24.3863

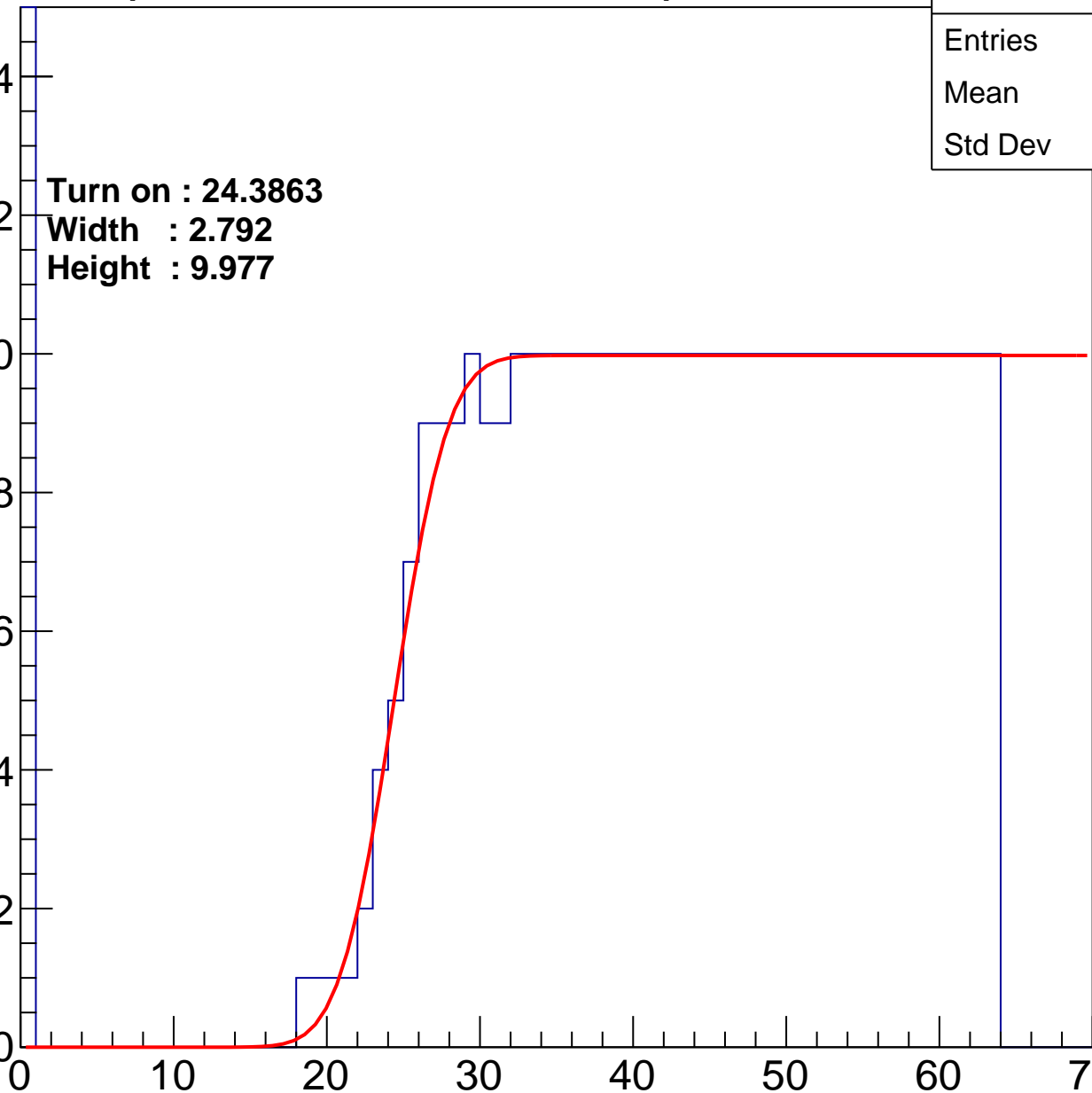
Width : 2.792

Height : 9.977

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch115

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	38.13
Std Dev	18.84

Turn on : 27.2776

Width : 2.886

Height : 10.041

Entry

14

12

10

8

6

4

2

0

0

10

20

30

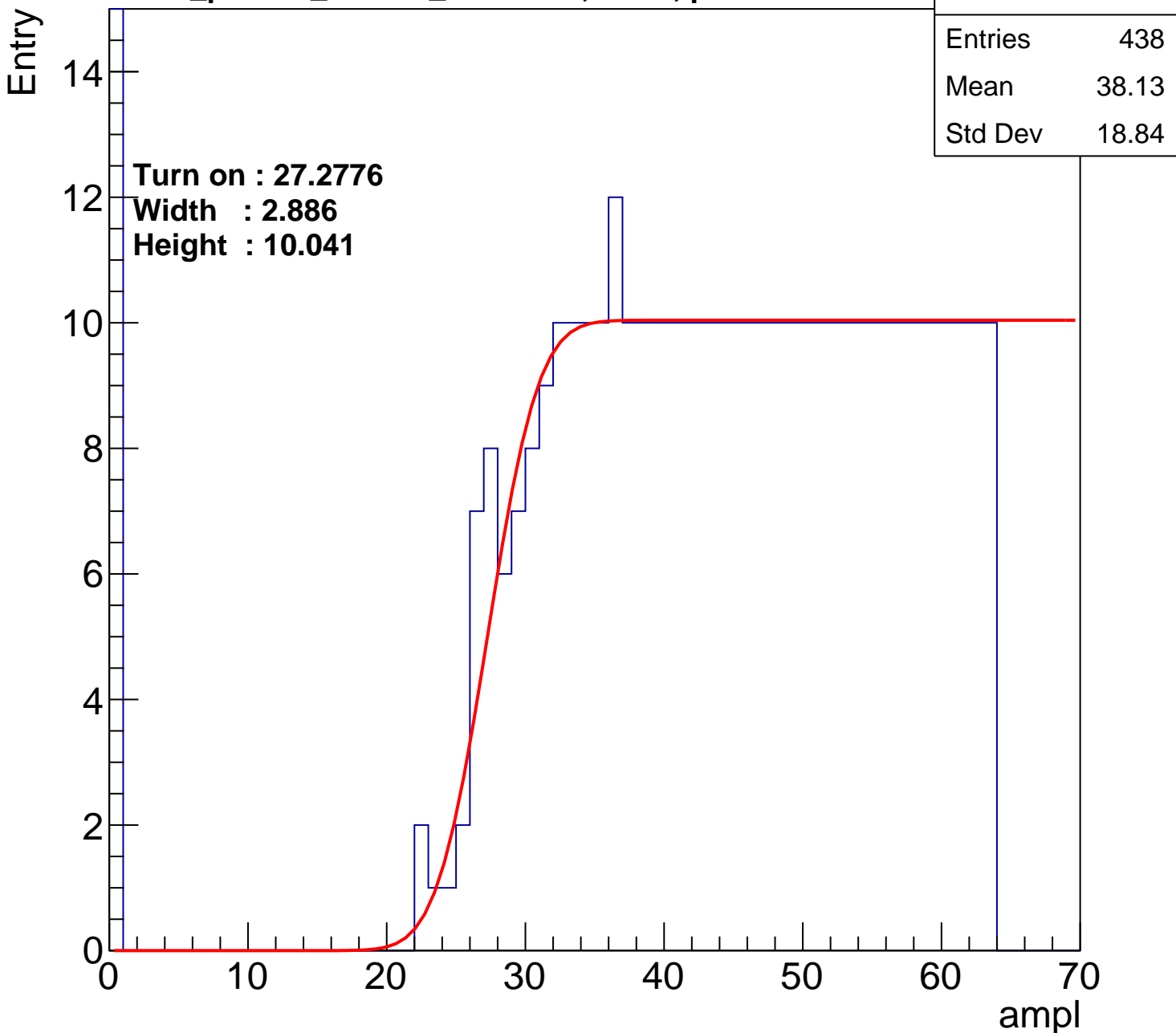
40

50

60

70

ampl



B1L103S, U7-ch116

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.87
Std Dev	16.75

Turn on : 25.0561

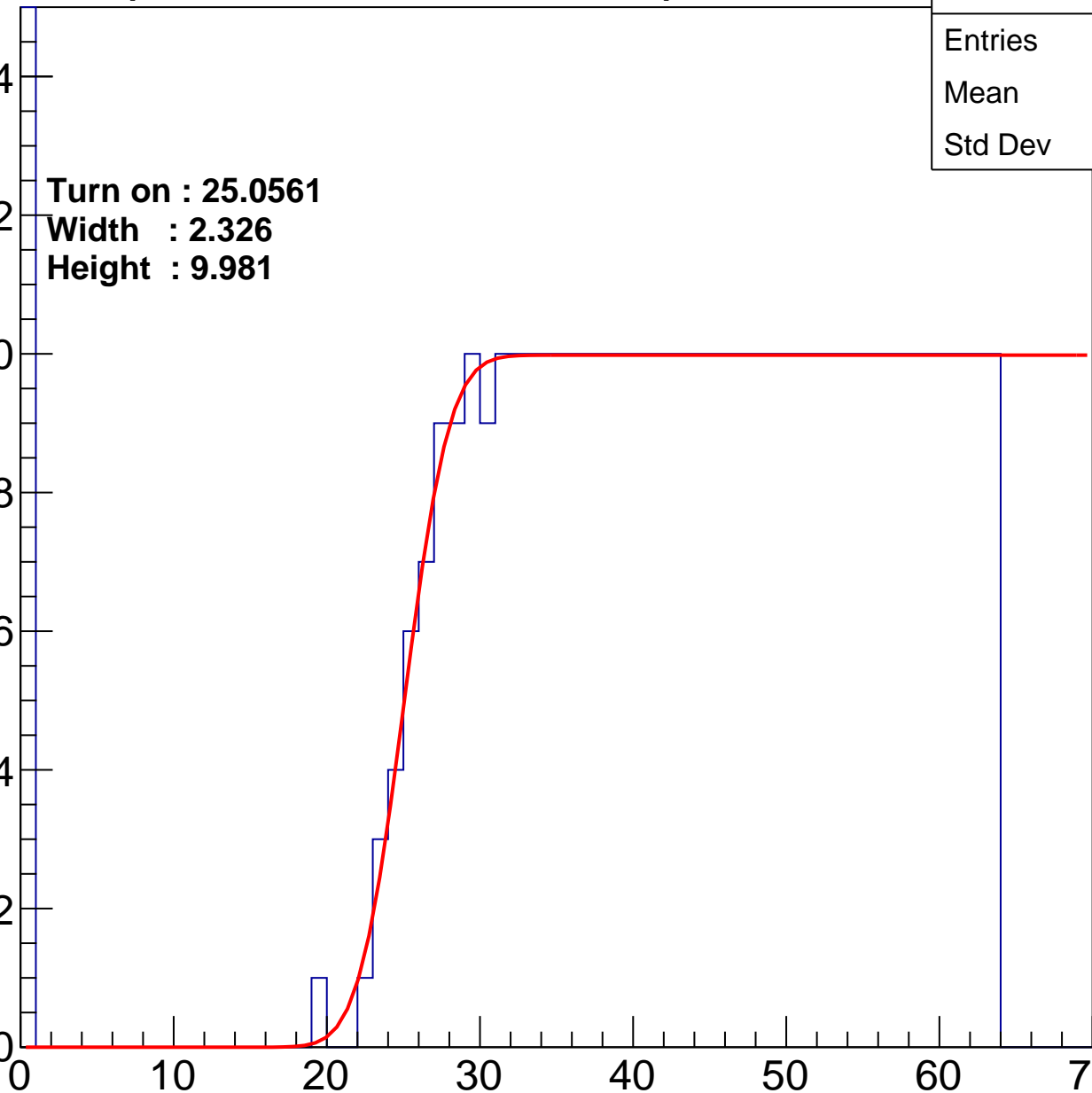
Width : 2.326

Height : 9.981

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch117

calib_packv5_041523_1651.root, FC#0, port C2

Entries	410
Mean	39.51
Std Dev	18.34

Turn on : 28.6706

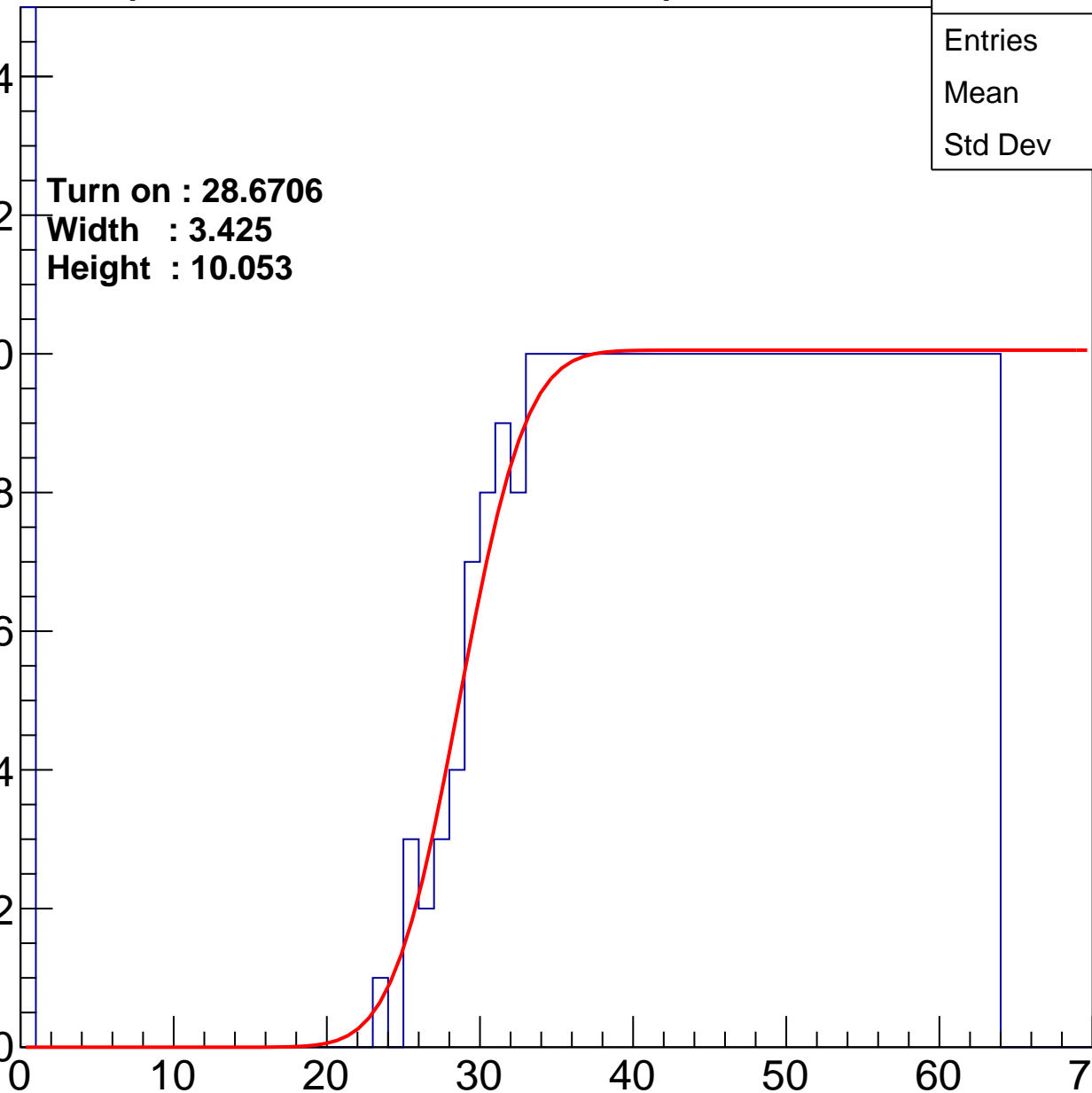
Width : 3.425

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch118

calib_packv5_041523_1651.root, FC#0, port C2

Entries	448
Mean	38.3
Std Dev	18.05

Turn on : 25.2730

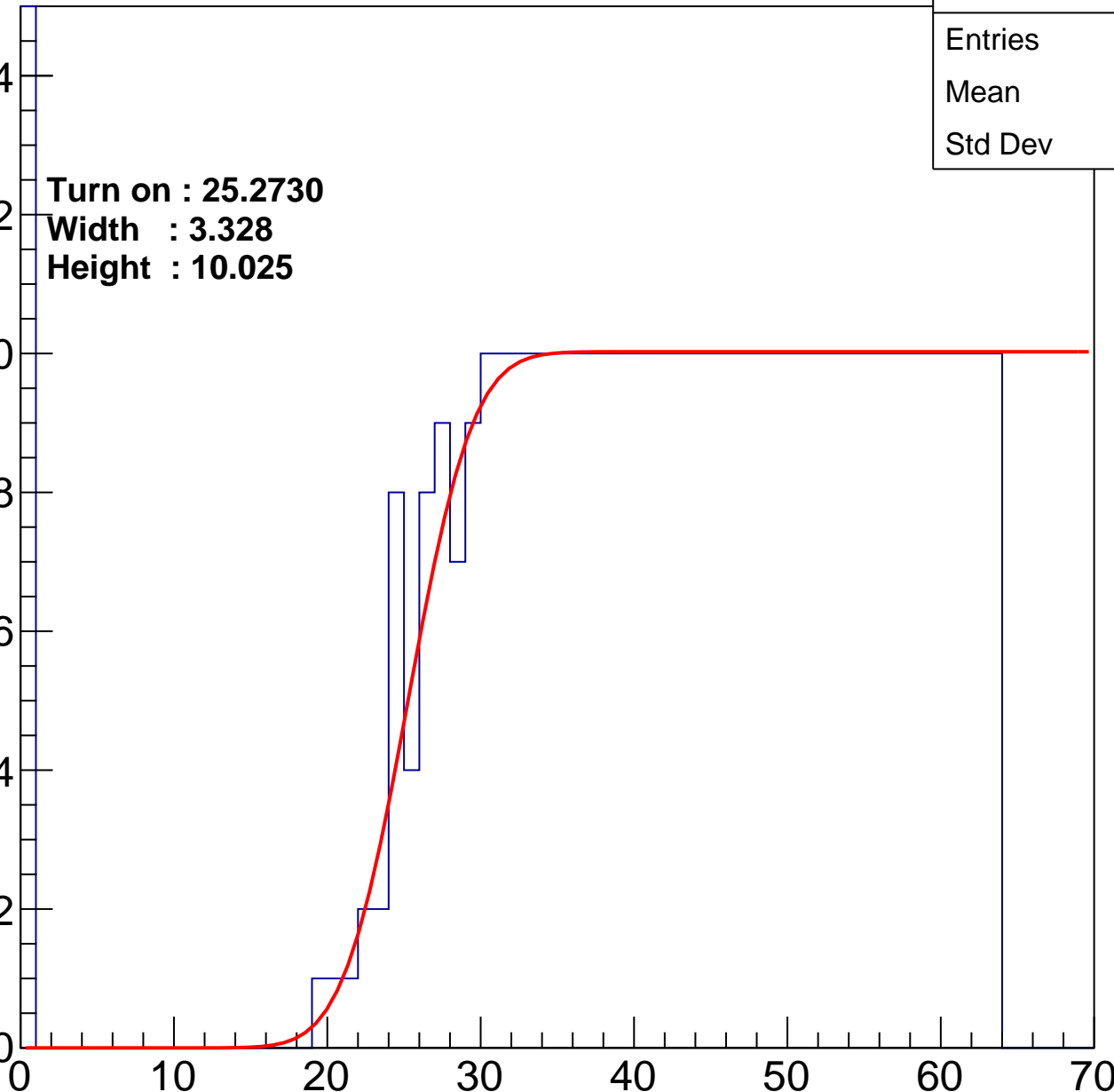
Width : 3.328

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch119

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	38.34
Std Dev	18.45

Turn on : 26.2827

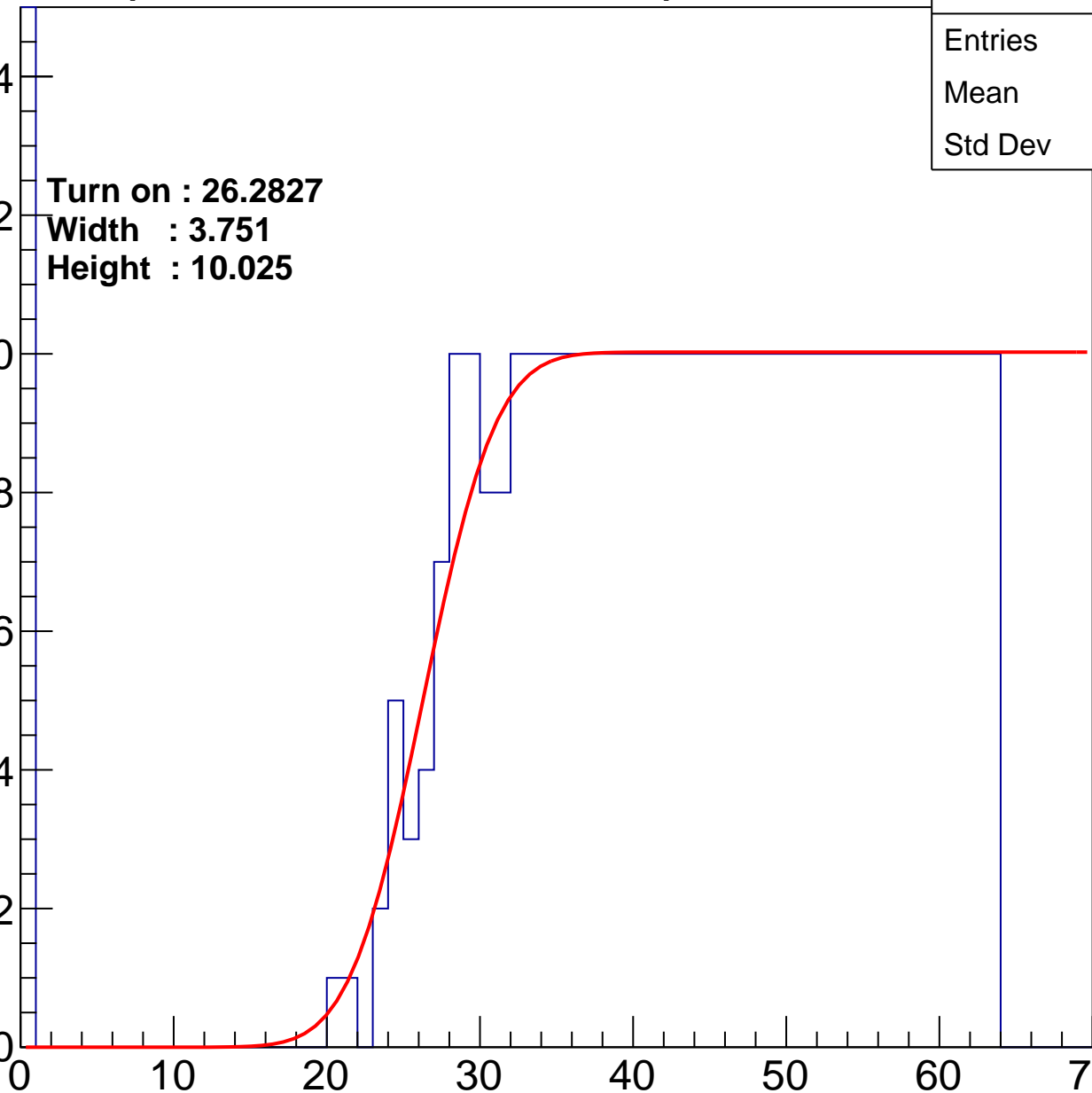
Width : 3.751

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch120

calib_packv5_041523_1651.root, FC#0, port C2

Entries	409
Mean	40.49
Std Dev	16.9

Turn on : 27.7711

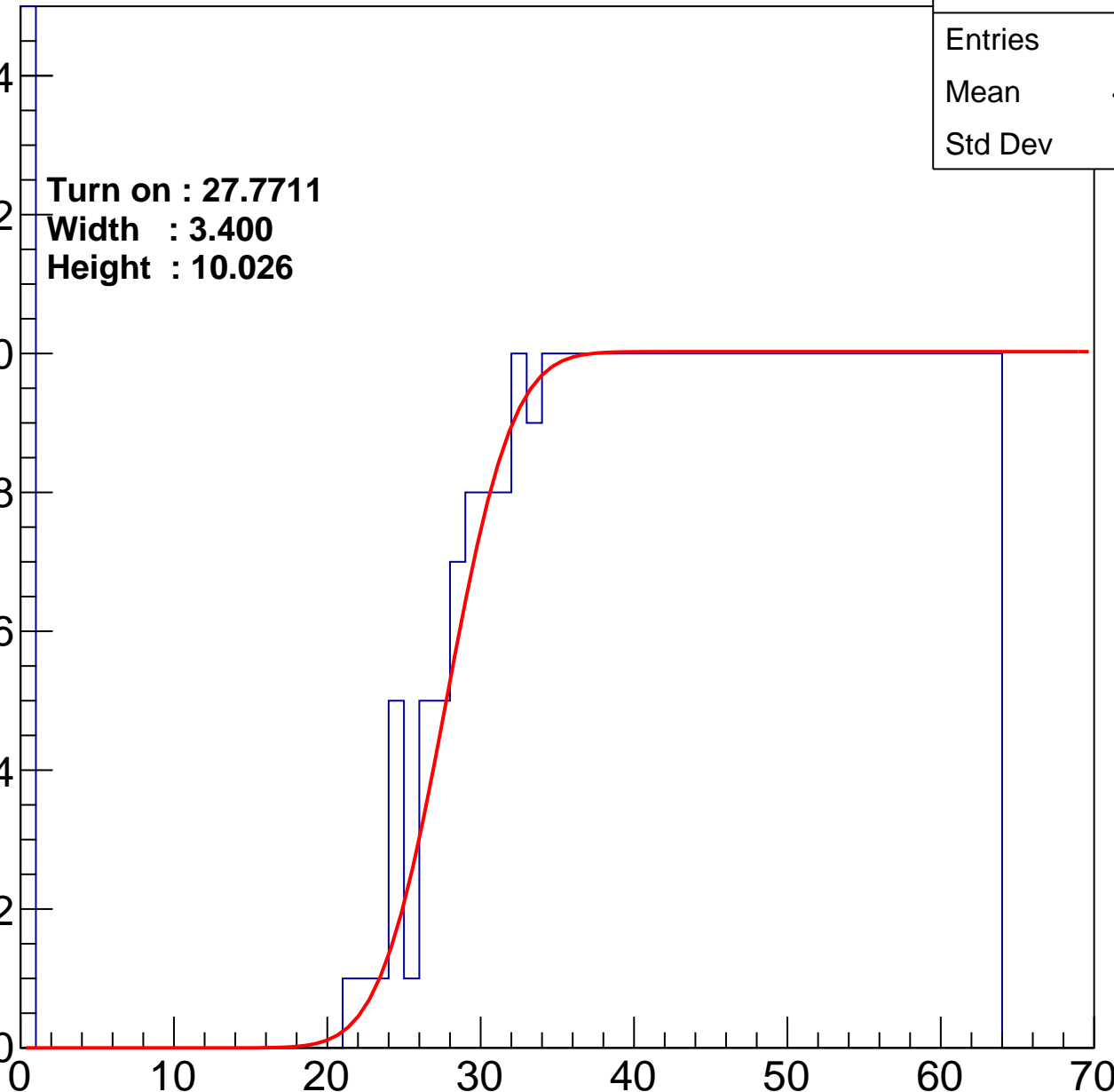
Width : 3.400

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch121

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	39.89
Std Dev	16.58

Turn on : 25.0242

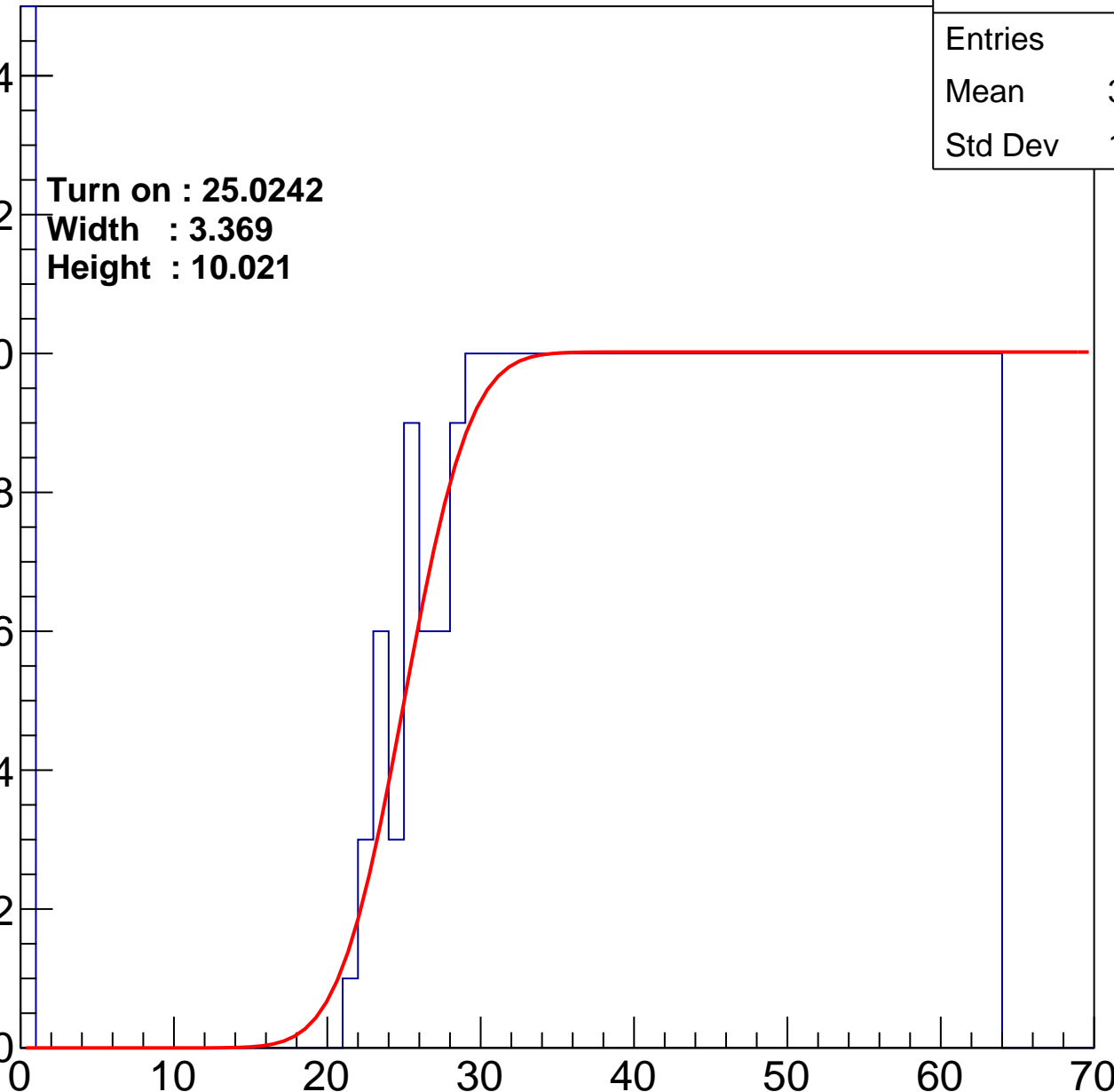
Width : 3.369

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch122

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	39.57
Std Dev	16.6

Turn on : 24.1257

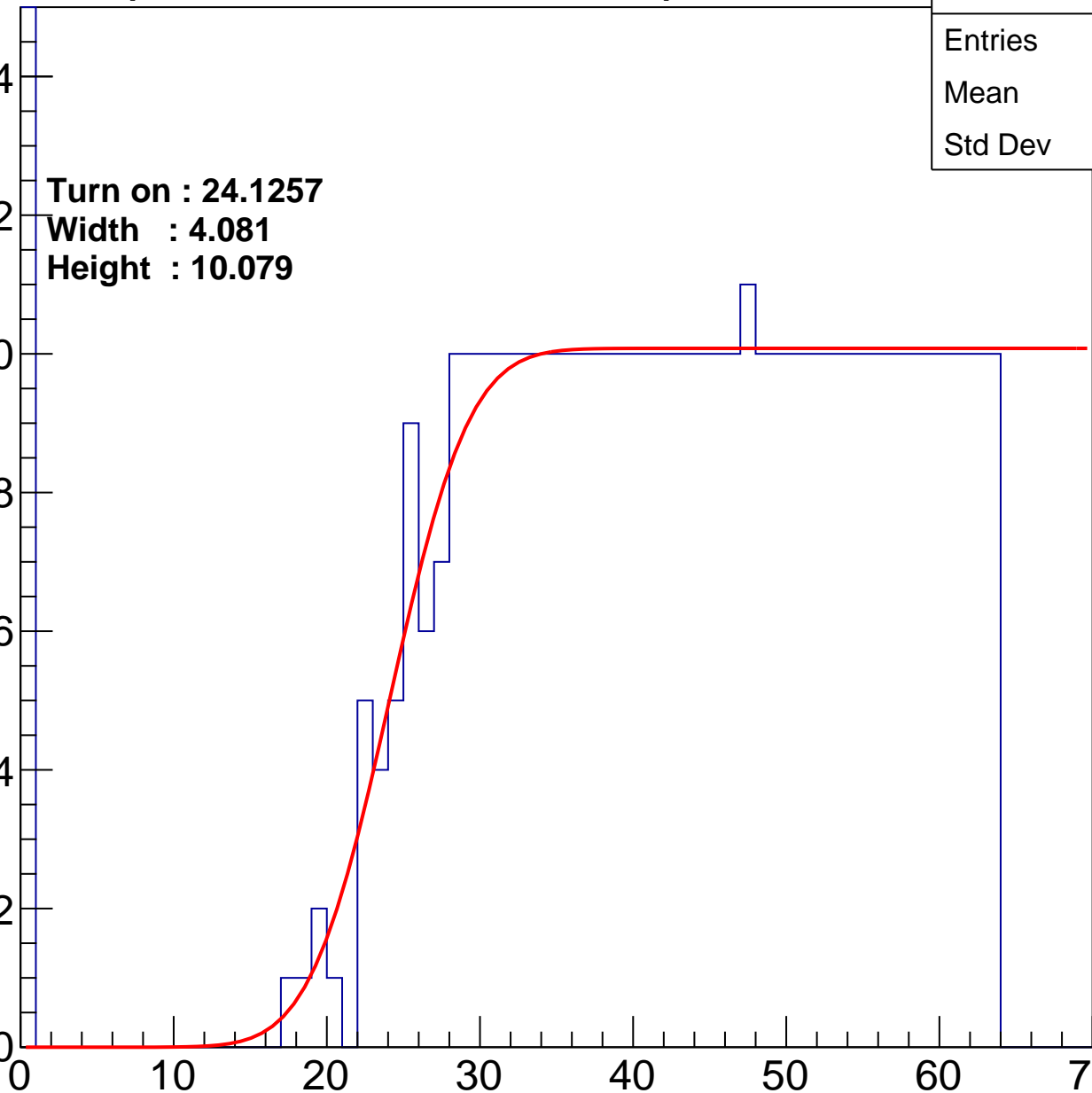
Width : 4.081

Height : 10.079

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch123

calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	38.97
Std Dev	17.9

Turn on : 26.2807

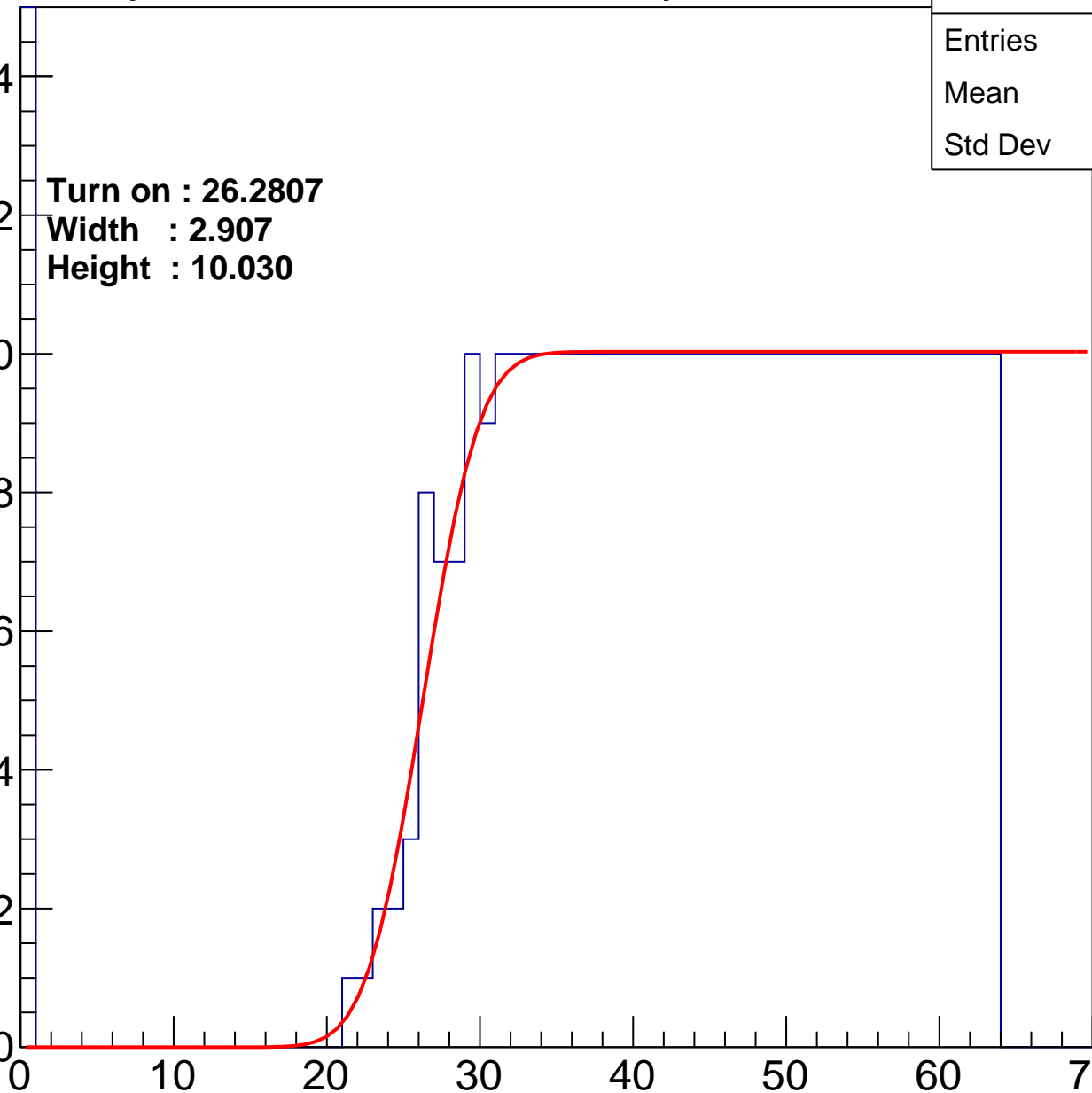
Width : 2.907

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch124

calib_packv5_041523_1651.root, FC#0, port C2

Entries	450
Mean	38.31
Std Dev	17.94

Turn on : 25.2540

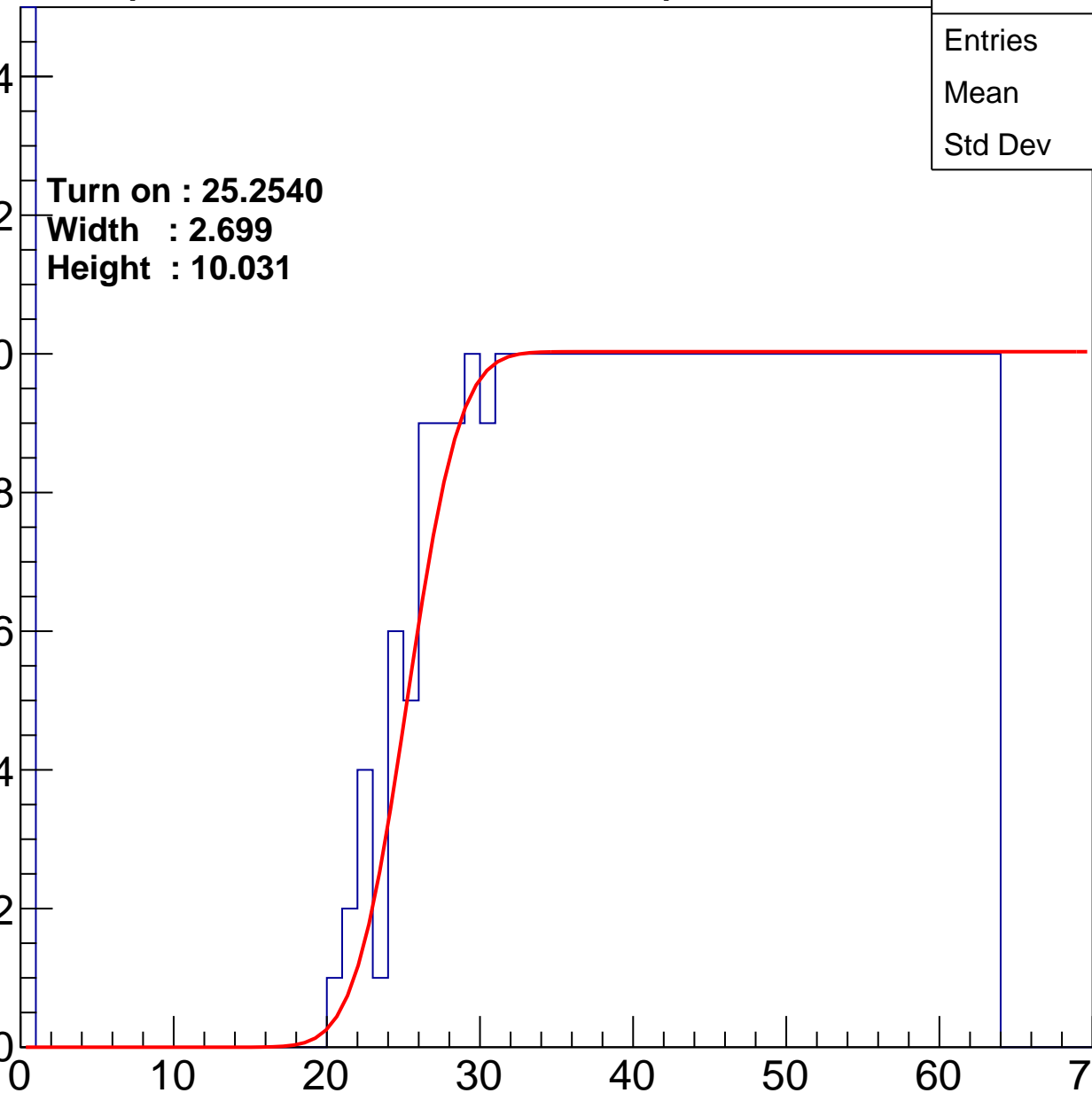
Width : 2.699

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch125

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	38.87
Std Dev	17.88

Turn on : 25.4408

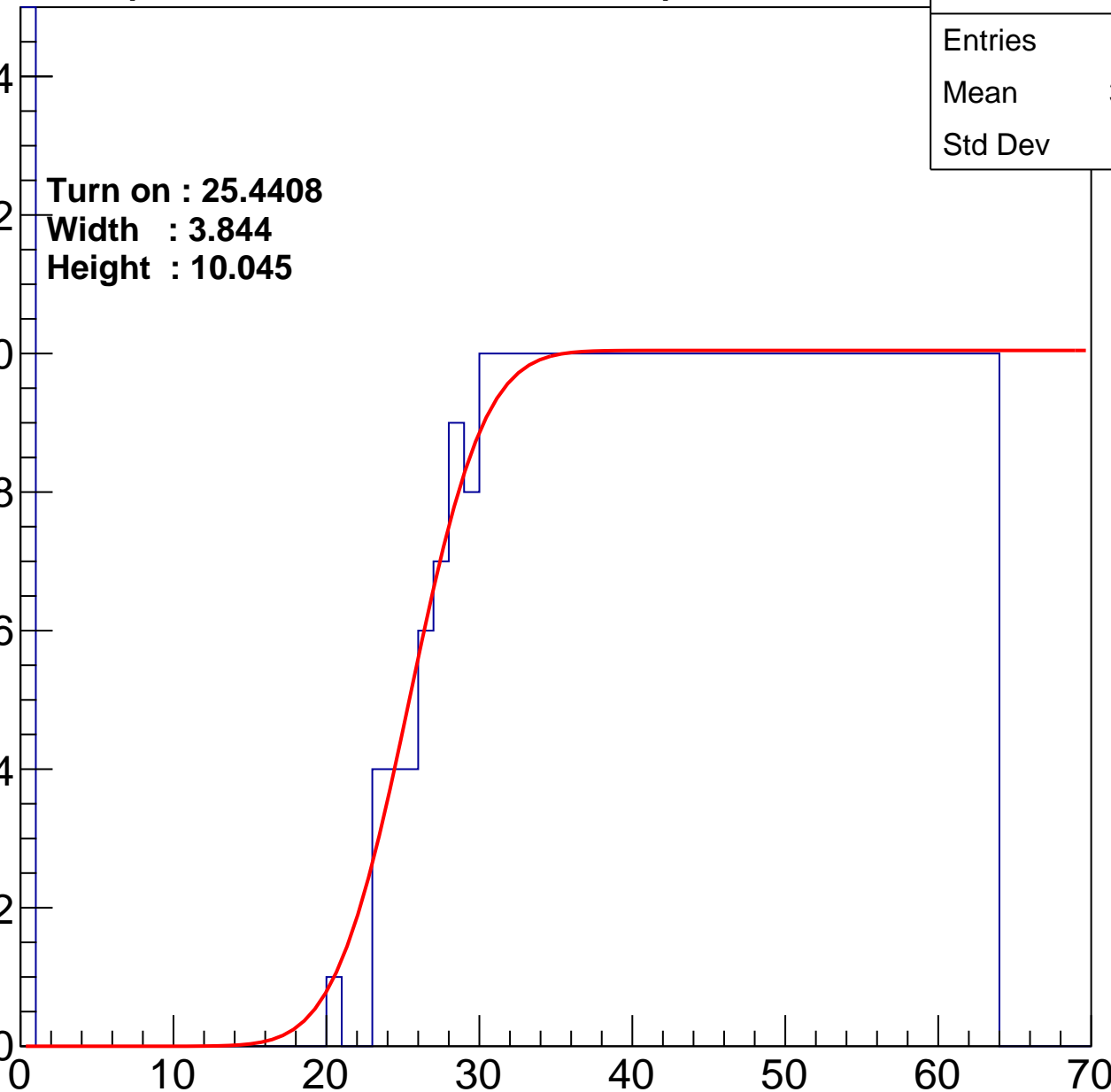
Width : 3.844

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch126

calib_packv5_041523_1651.root, FC#0, port C2

Entries	462
Mean	38.36
Std Dev	17.24

Turn on : 22.1393

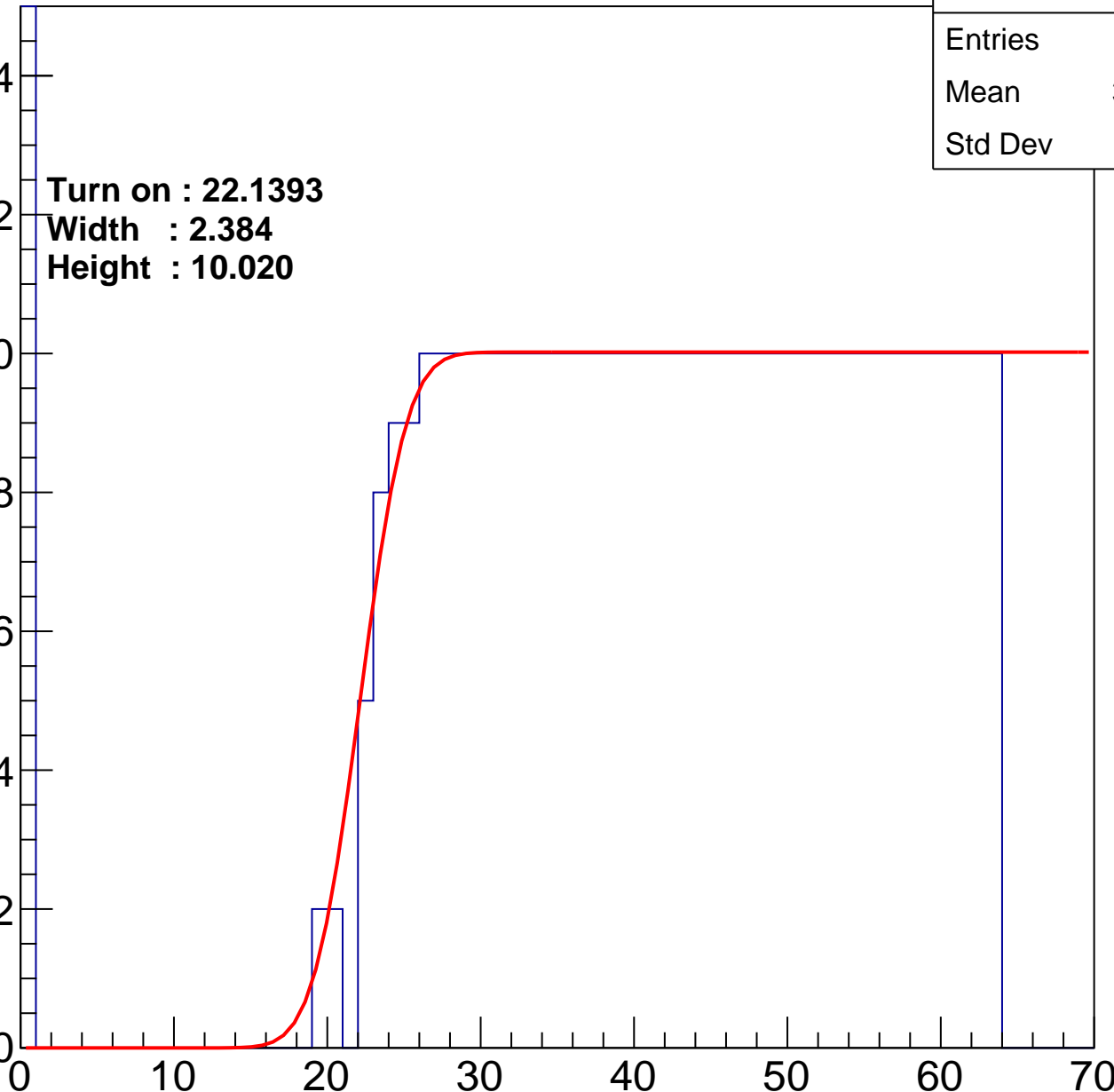
Width : 2.384

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch127

calib_packv5_041523_1651.root, FC#0, port C2

Entries	451
Mean	38.3
Std Dev	17.85

Turn on : 24.2721

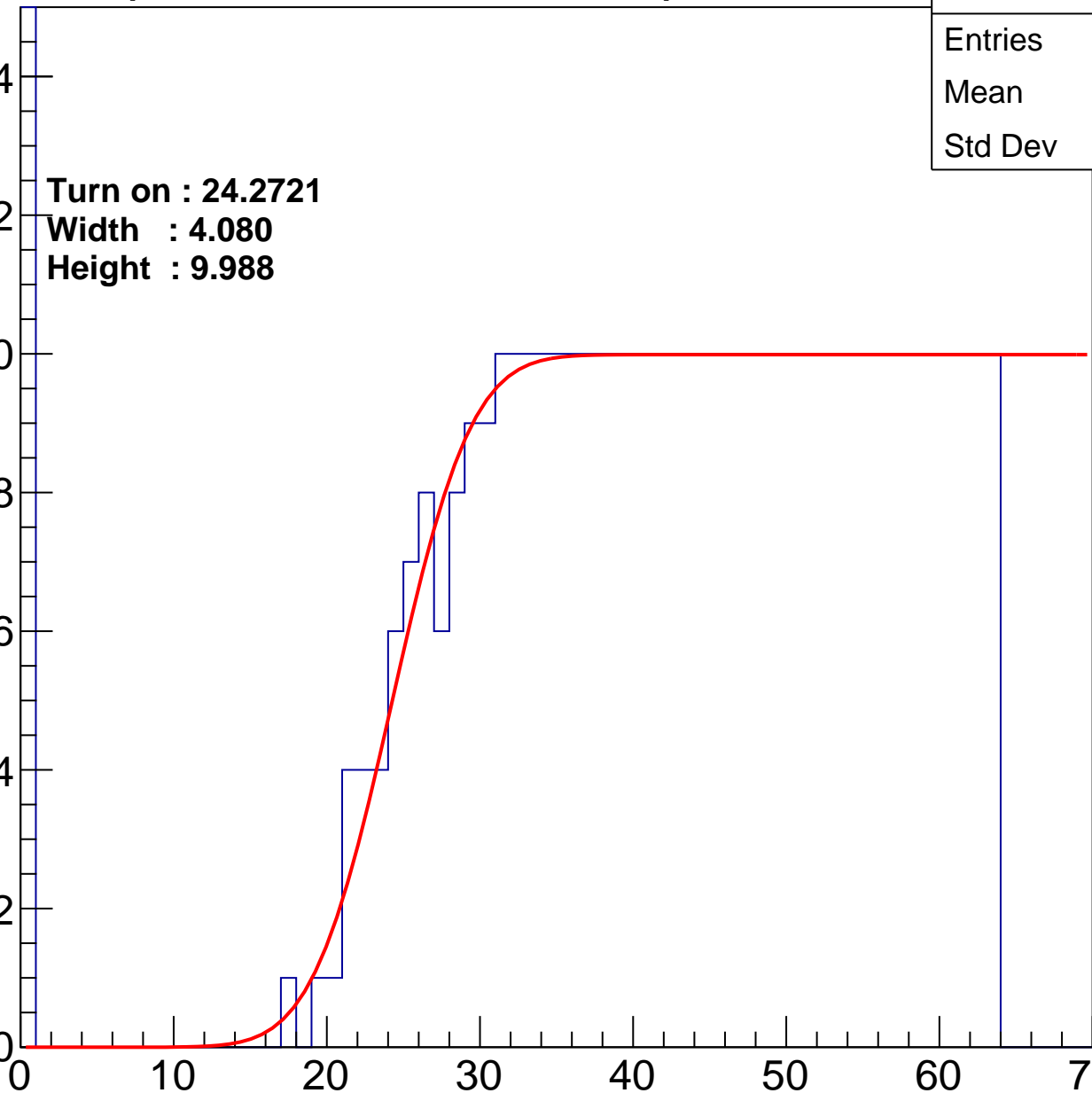
Width : 4.080

Height : 9.988

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U7-ch127

calib_packv5_041523_1651.root, FC#0, port C2

Entries	451
Mean	38.3
Std Dev	17.85

Turn on : 24.2721

Width : 4.080

Height : 9.988

Entry

14
12
10
8
6
4
2
0

ampl

