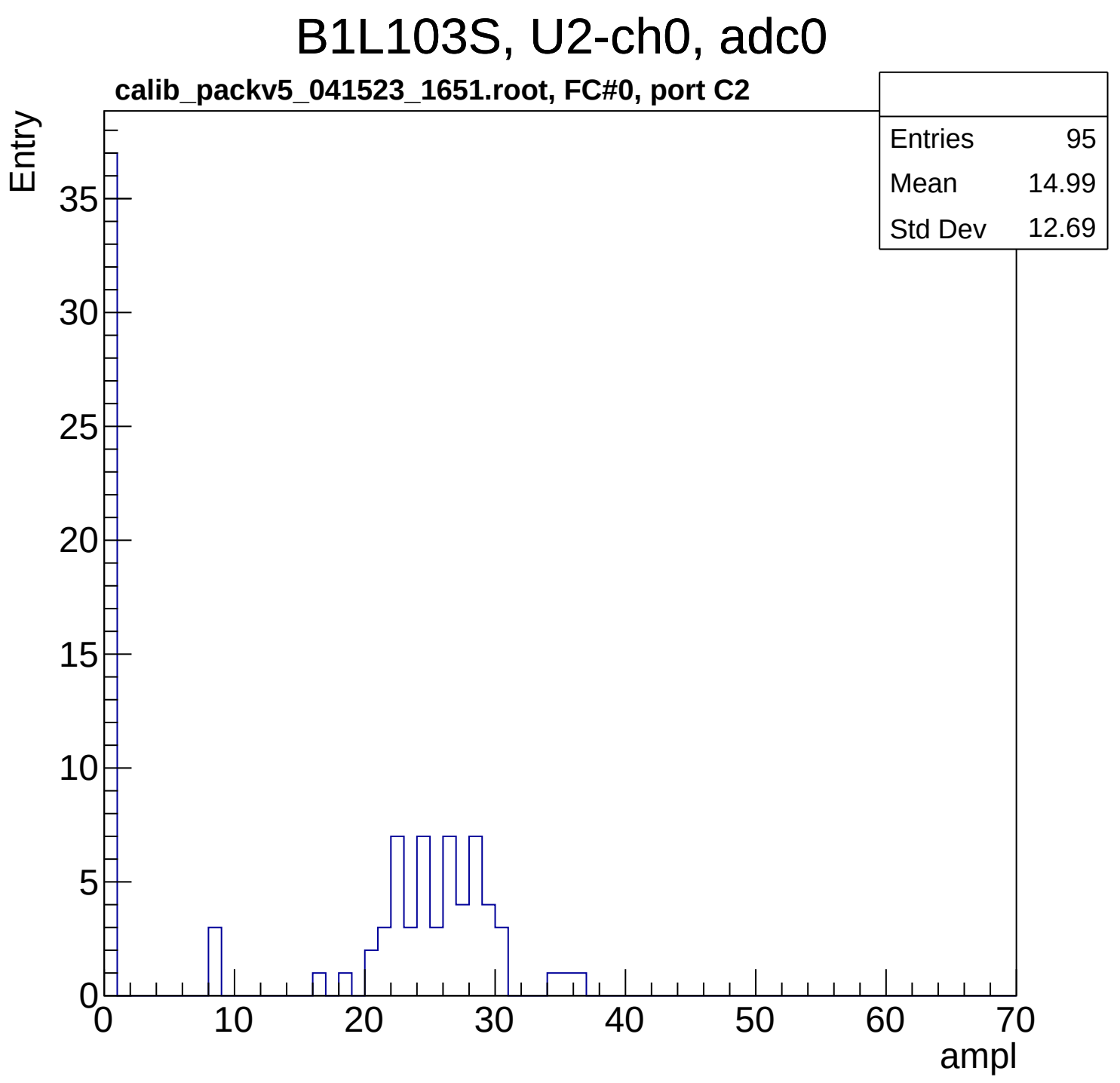
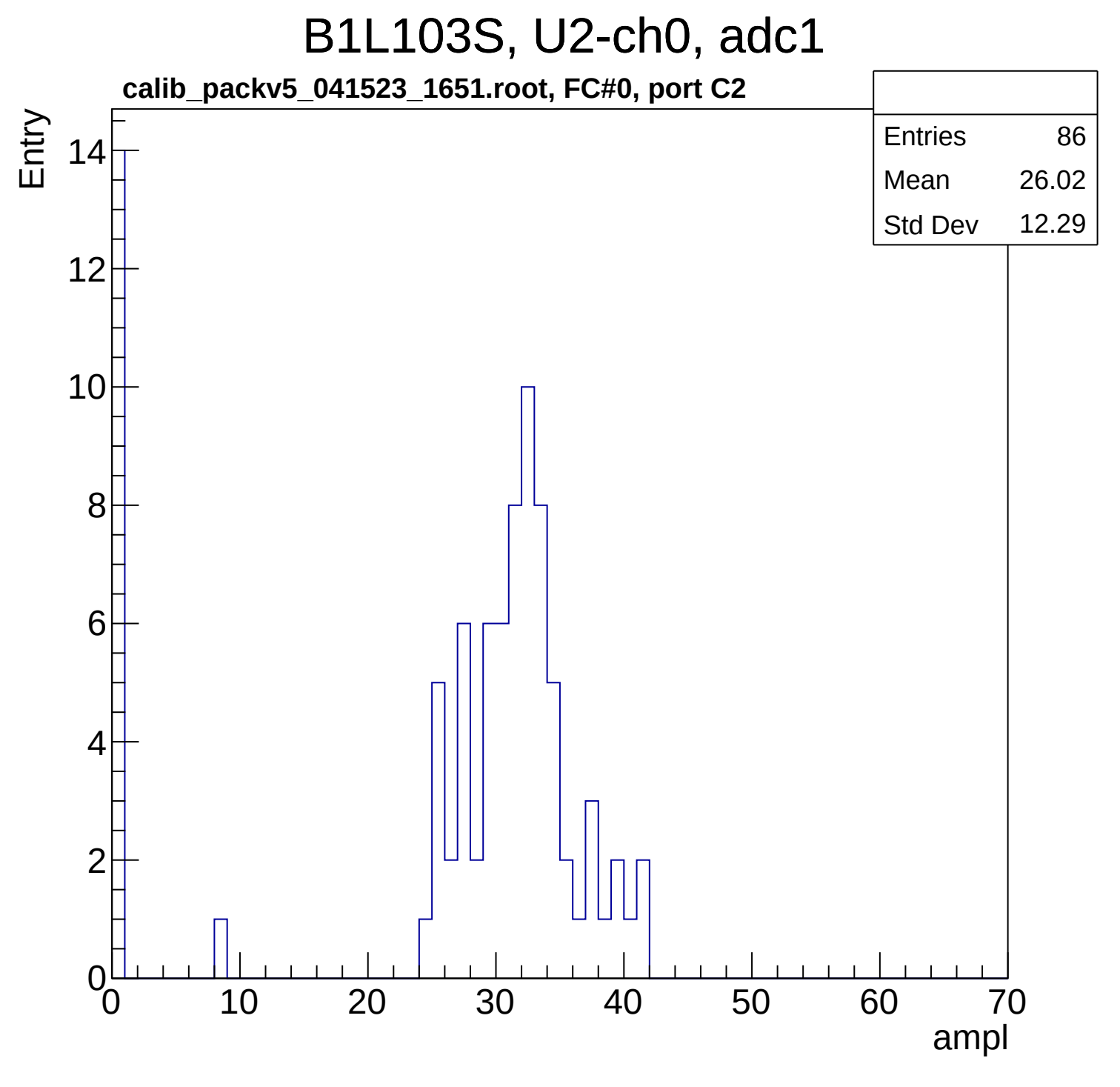
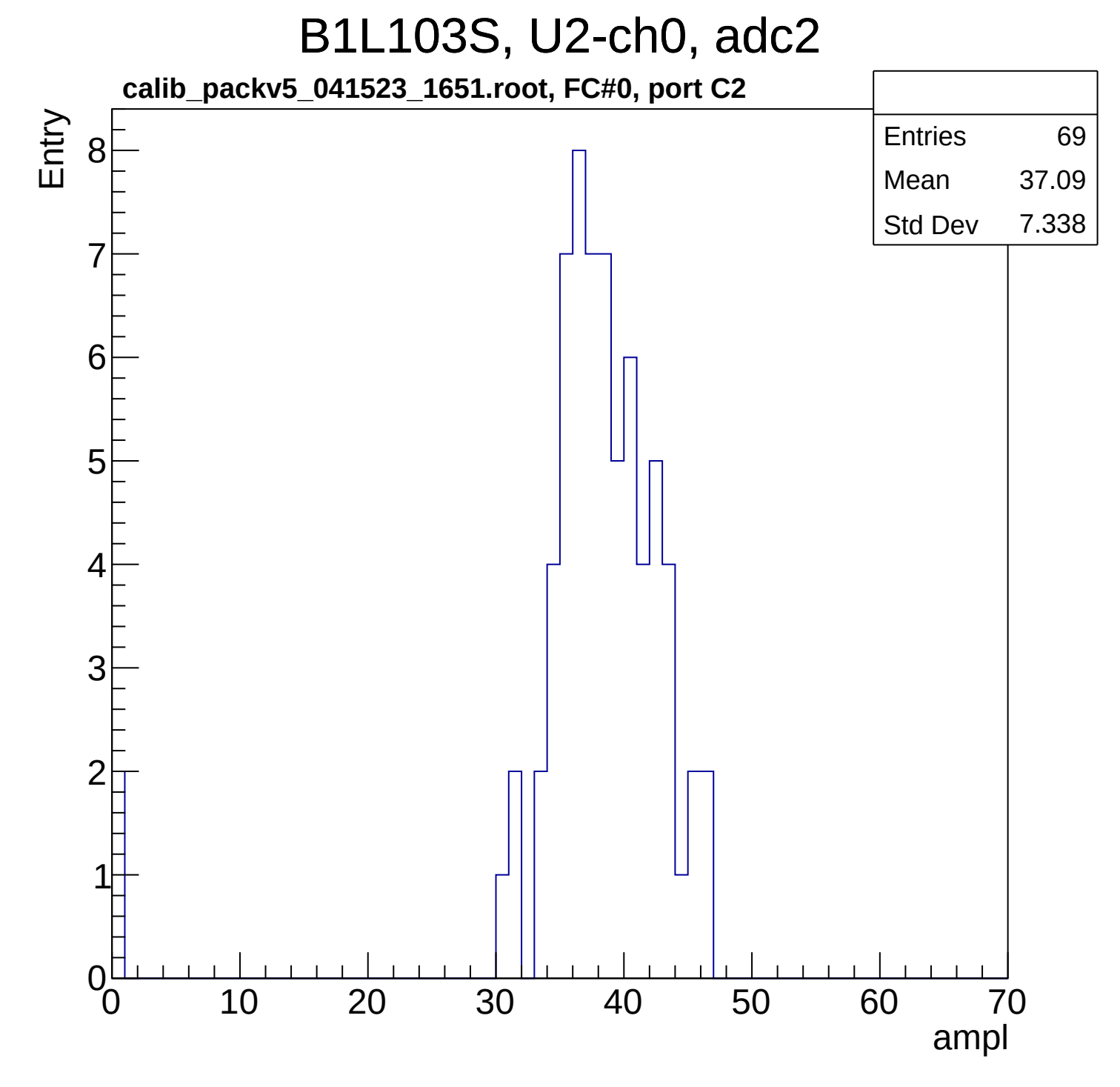
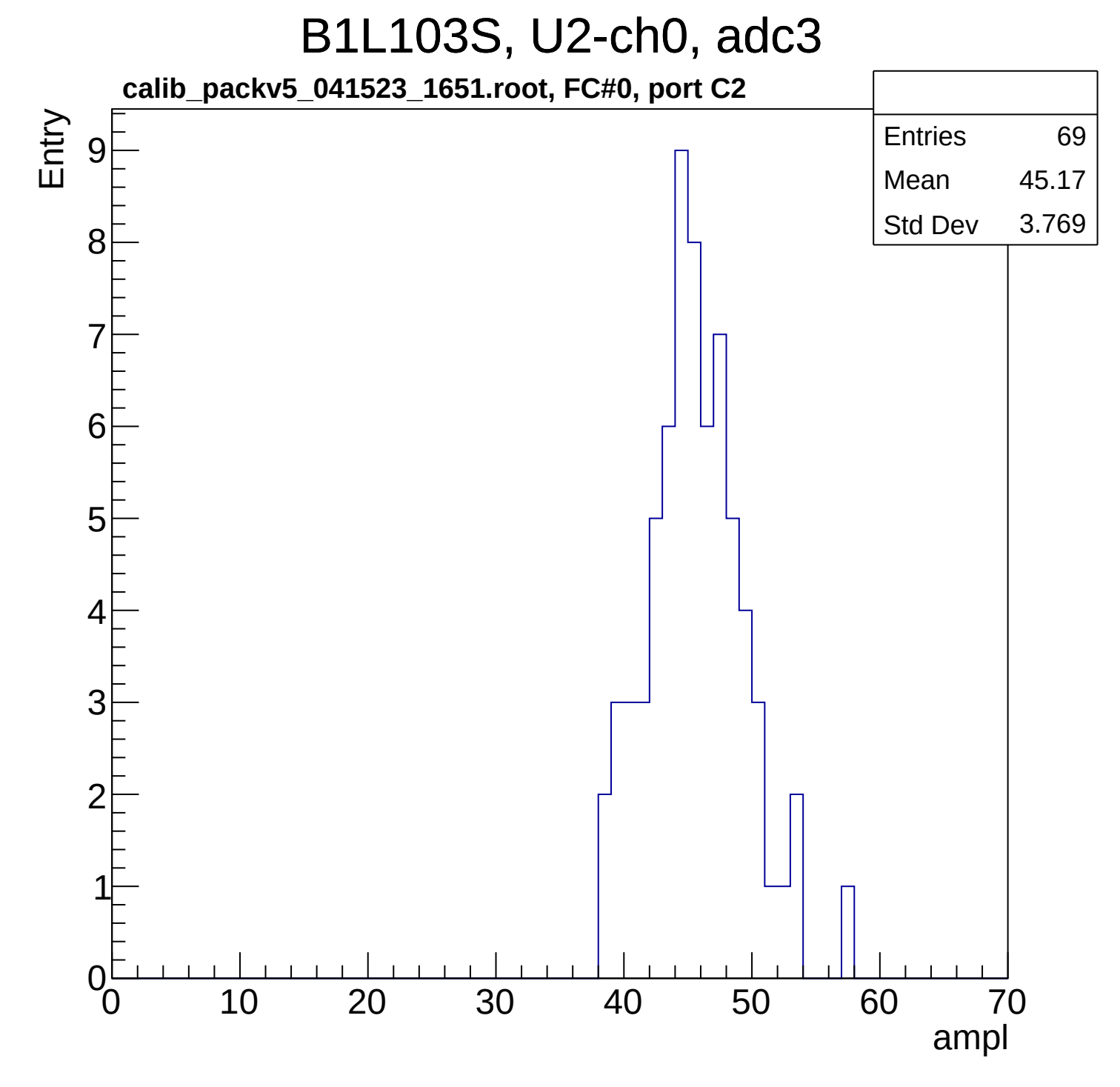
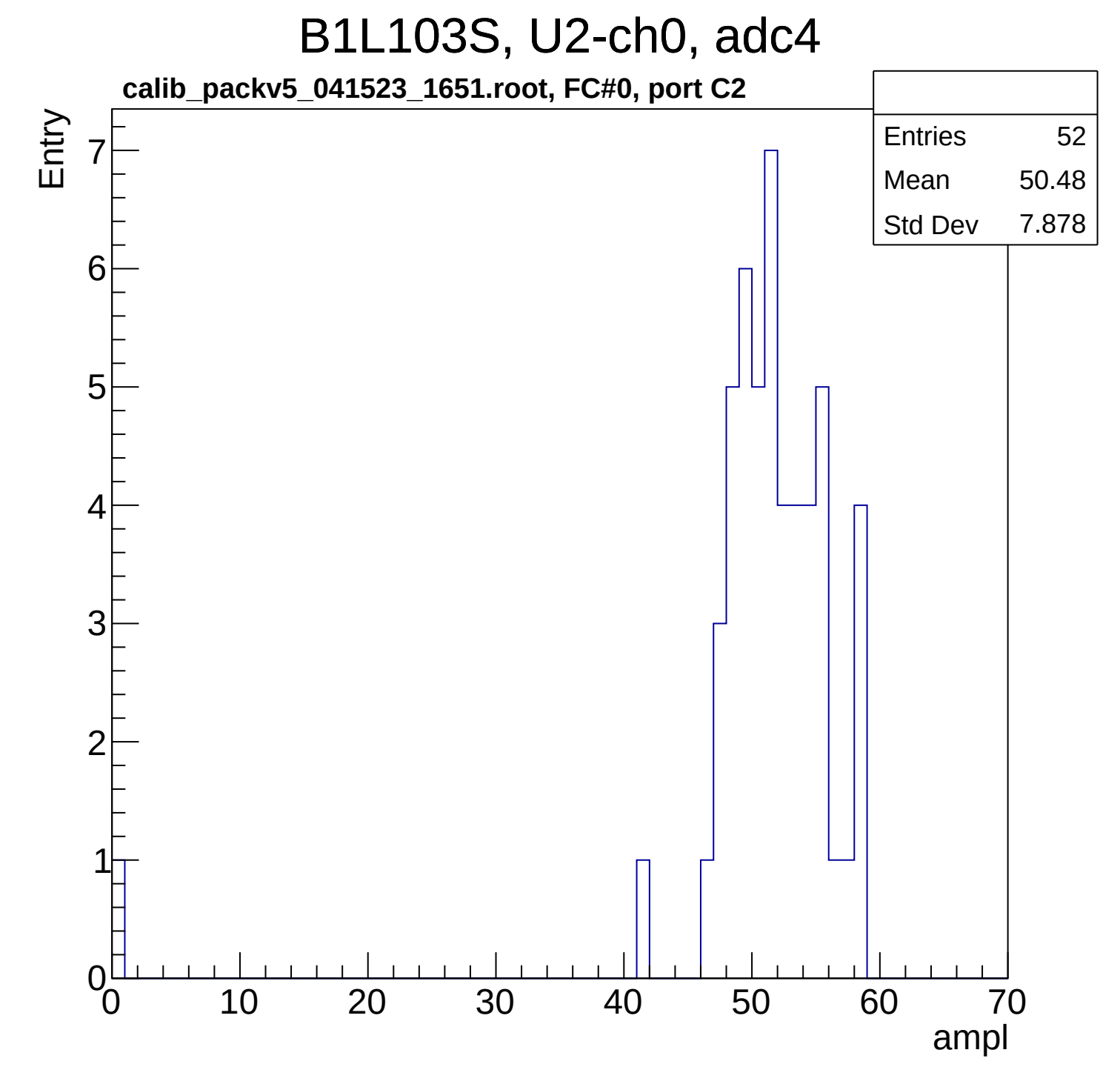
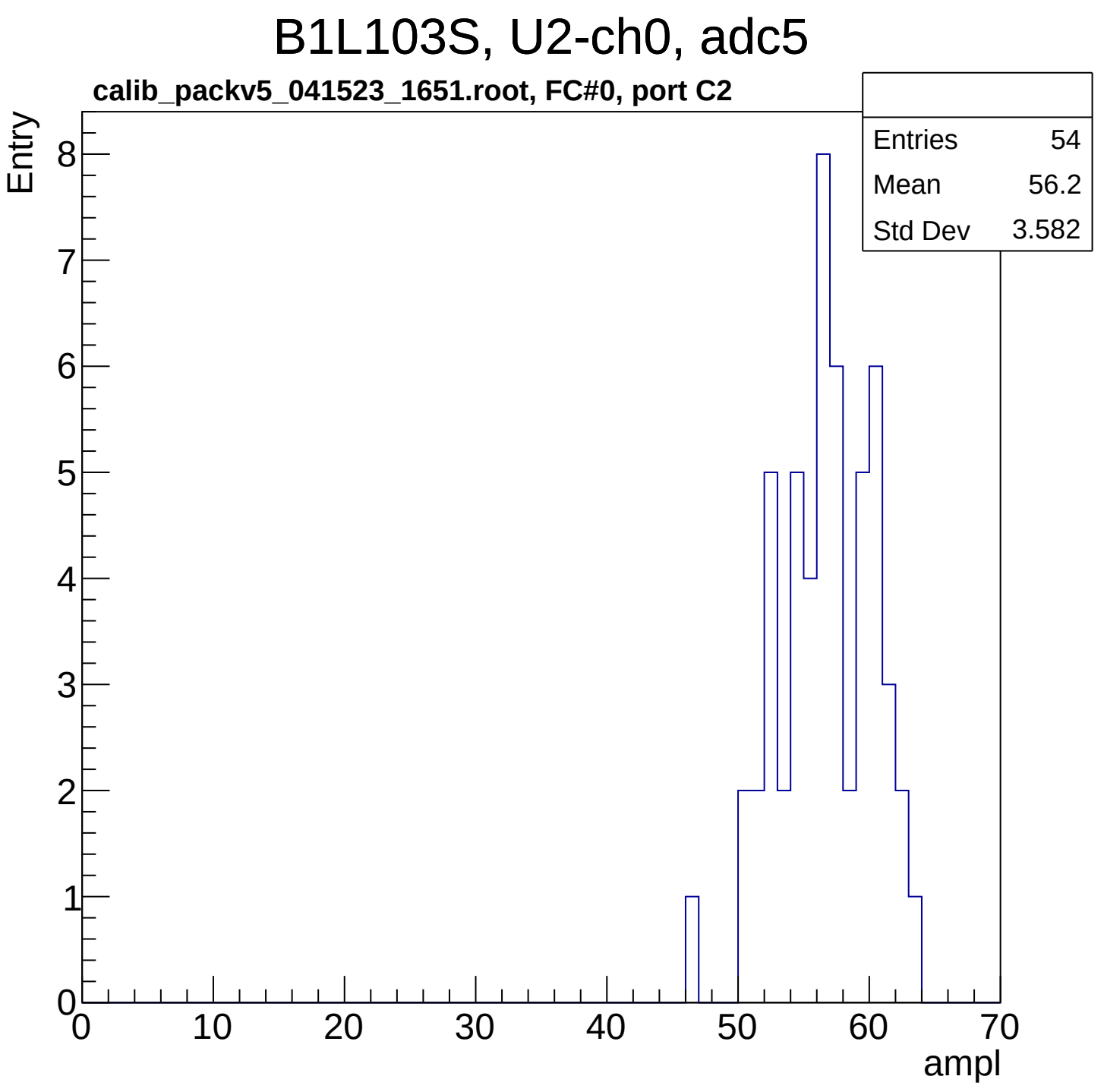

B1L103S, U2-ch0, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 14.99
Std Dev 12.69
Entry
0
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70
ampl

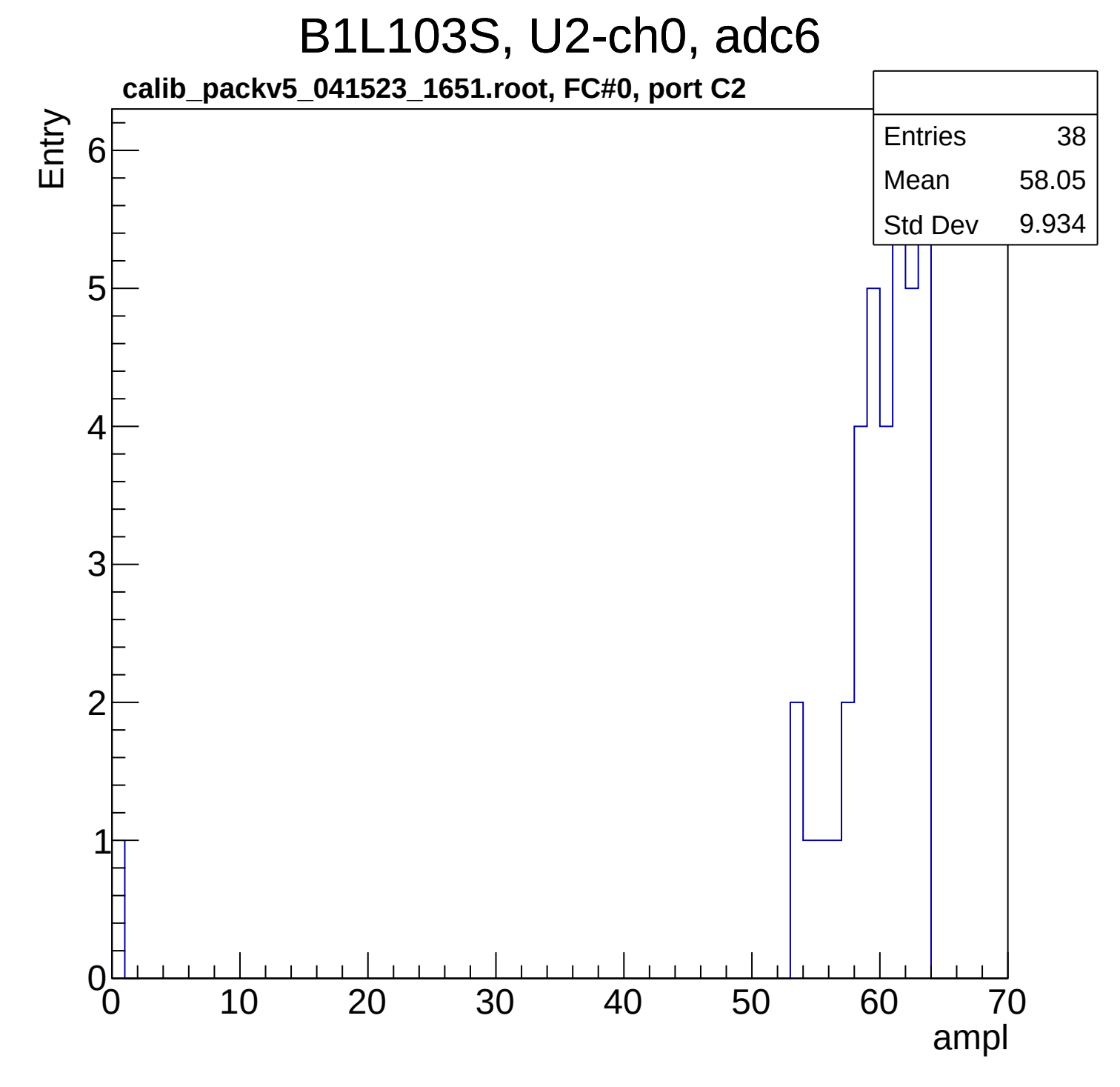

B1L103S, U2-ch0, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 26.02
Std Dev 12.29
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

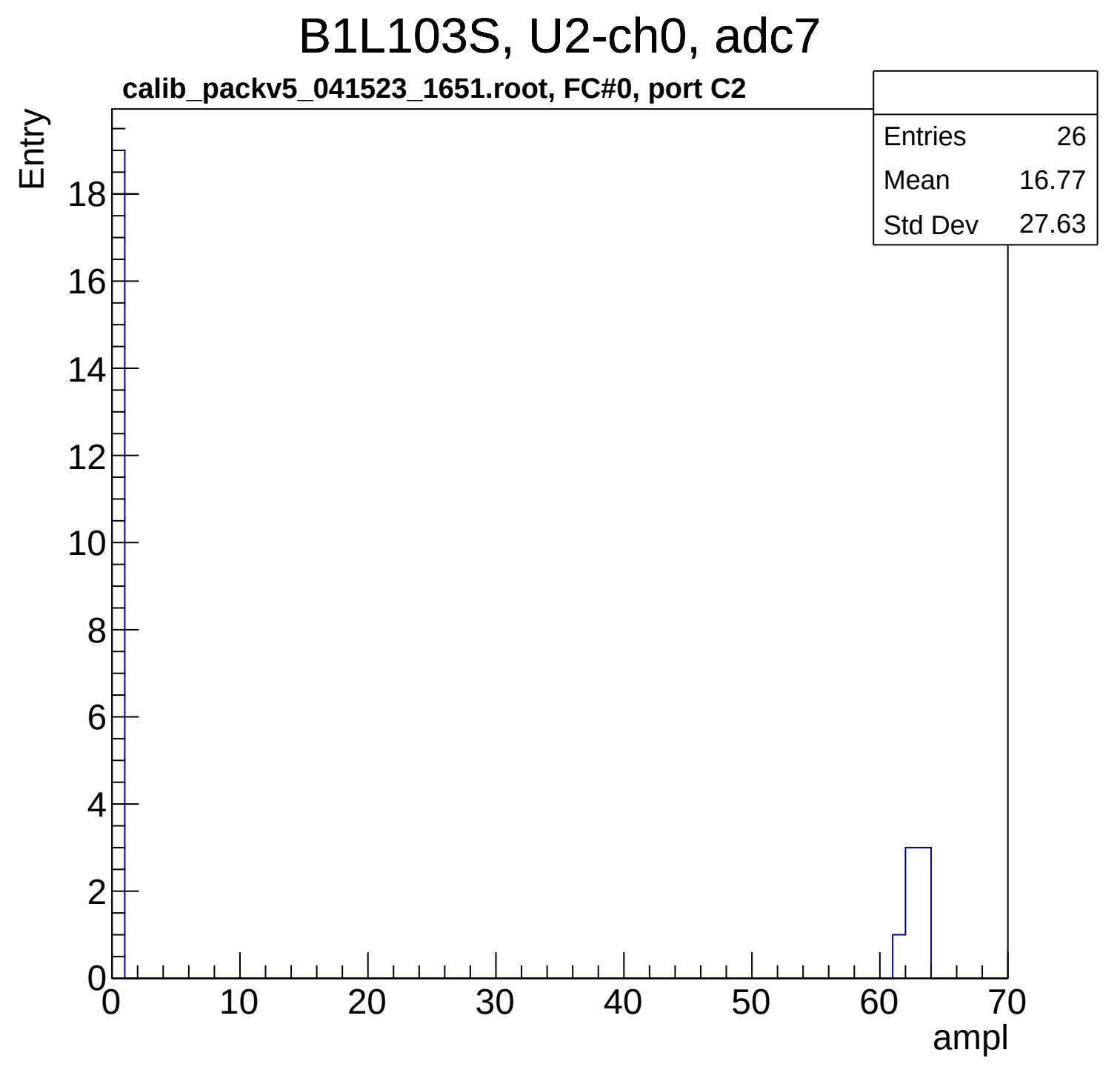

B1L103S, U2-ch0, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 37.09
Std Dev 7.338
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

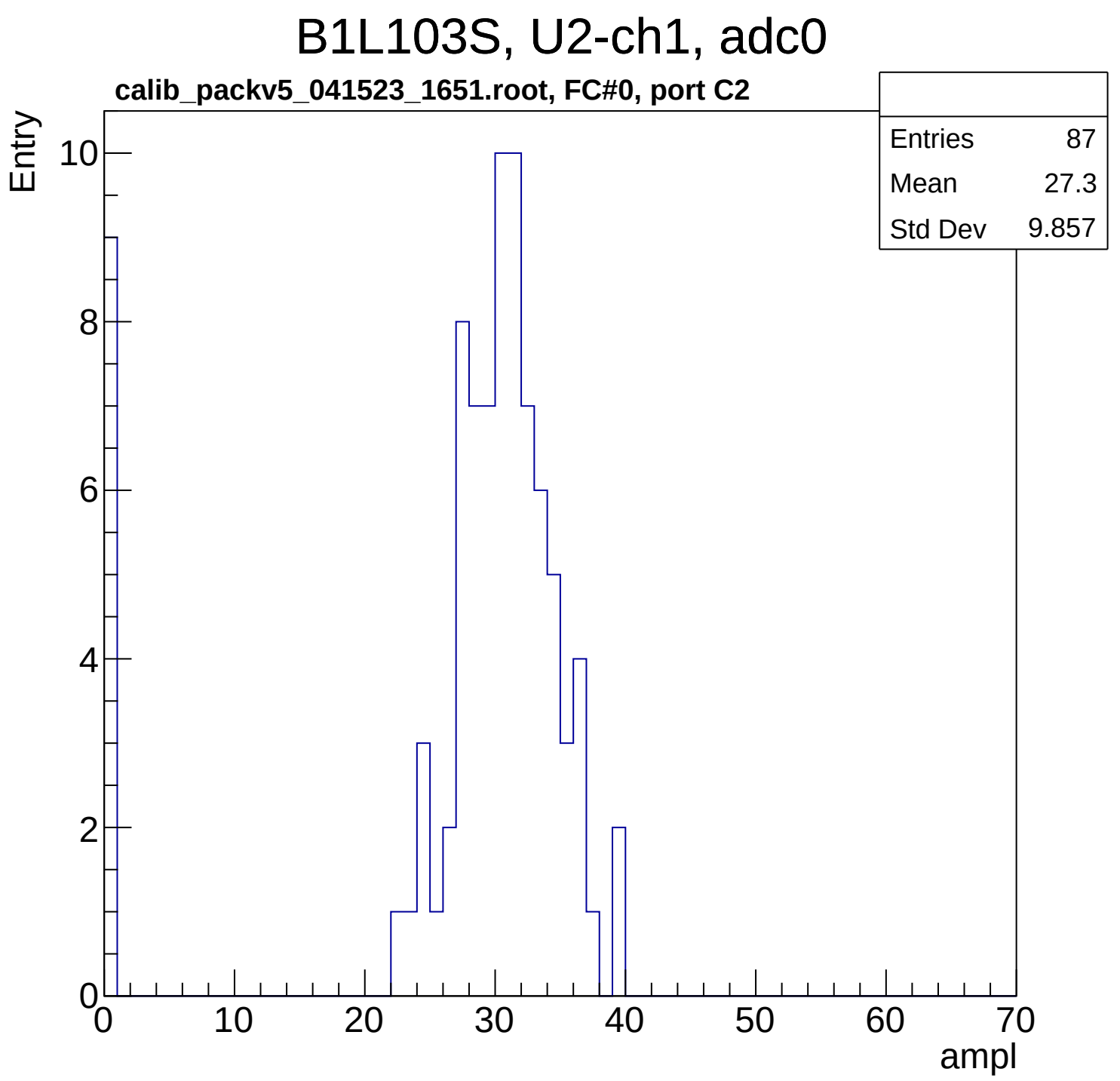

B1L103S, U2-ch0, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 45.17
Std Dev 3.769
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

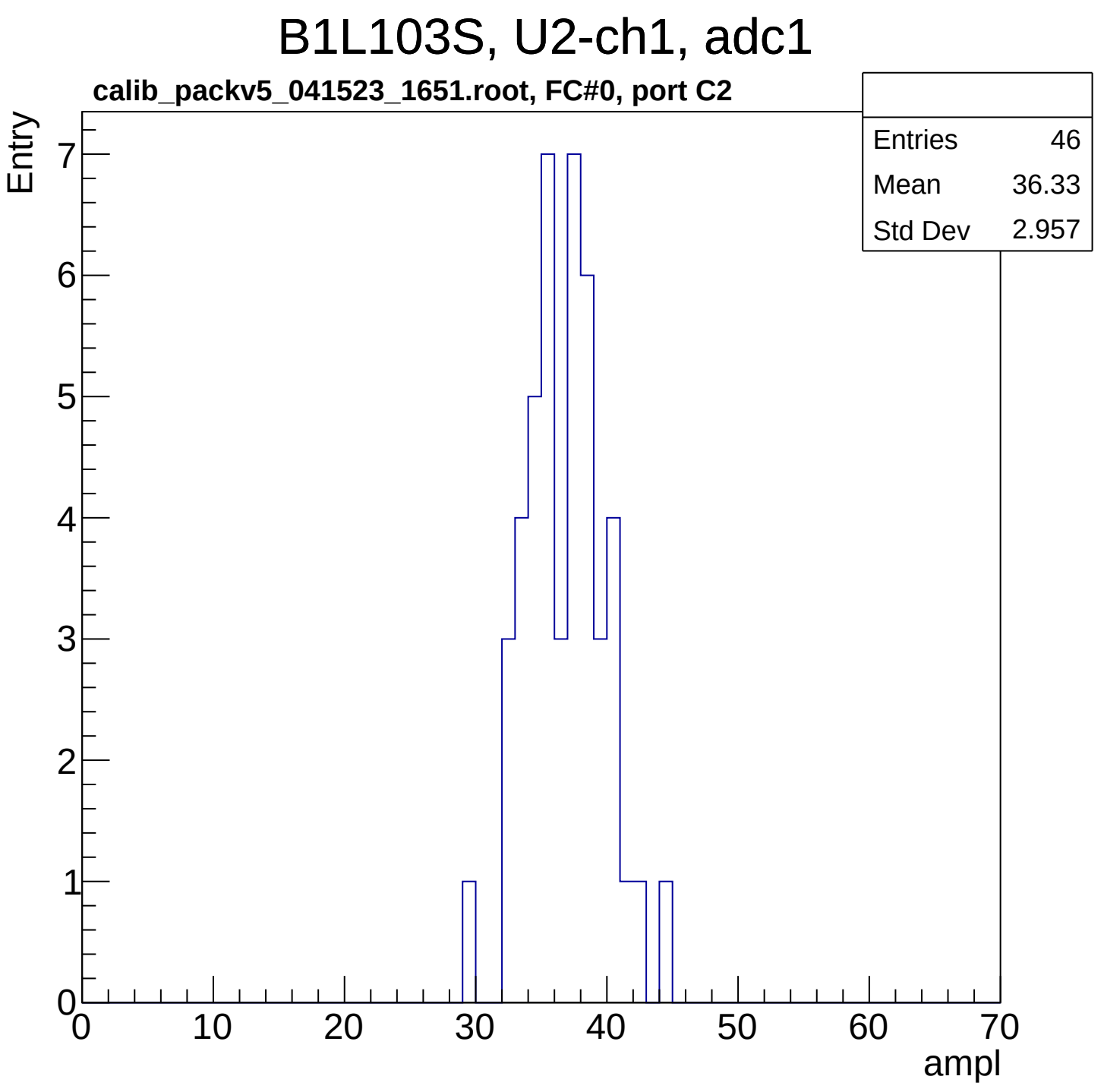

B1L103S, U2-ch0, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 50.48
Std Dev 7.878
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

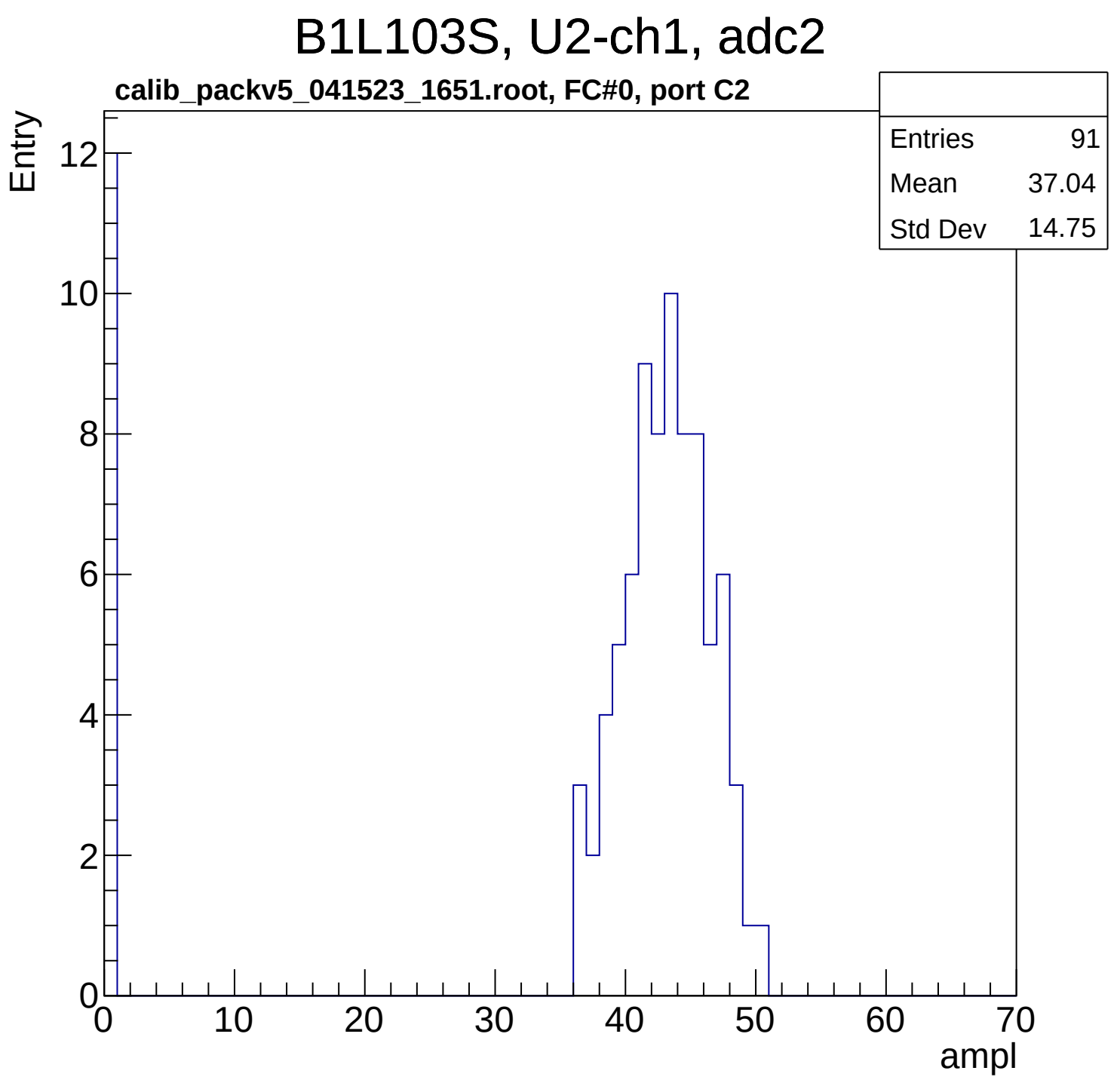

B1L103S, U2-ch0, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 56.2
Std Dev 3.582
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

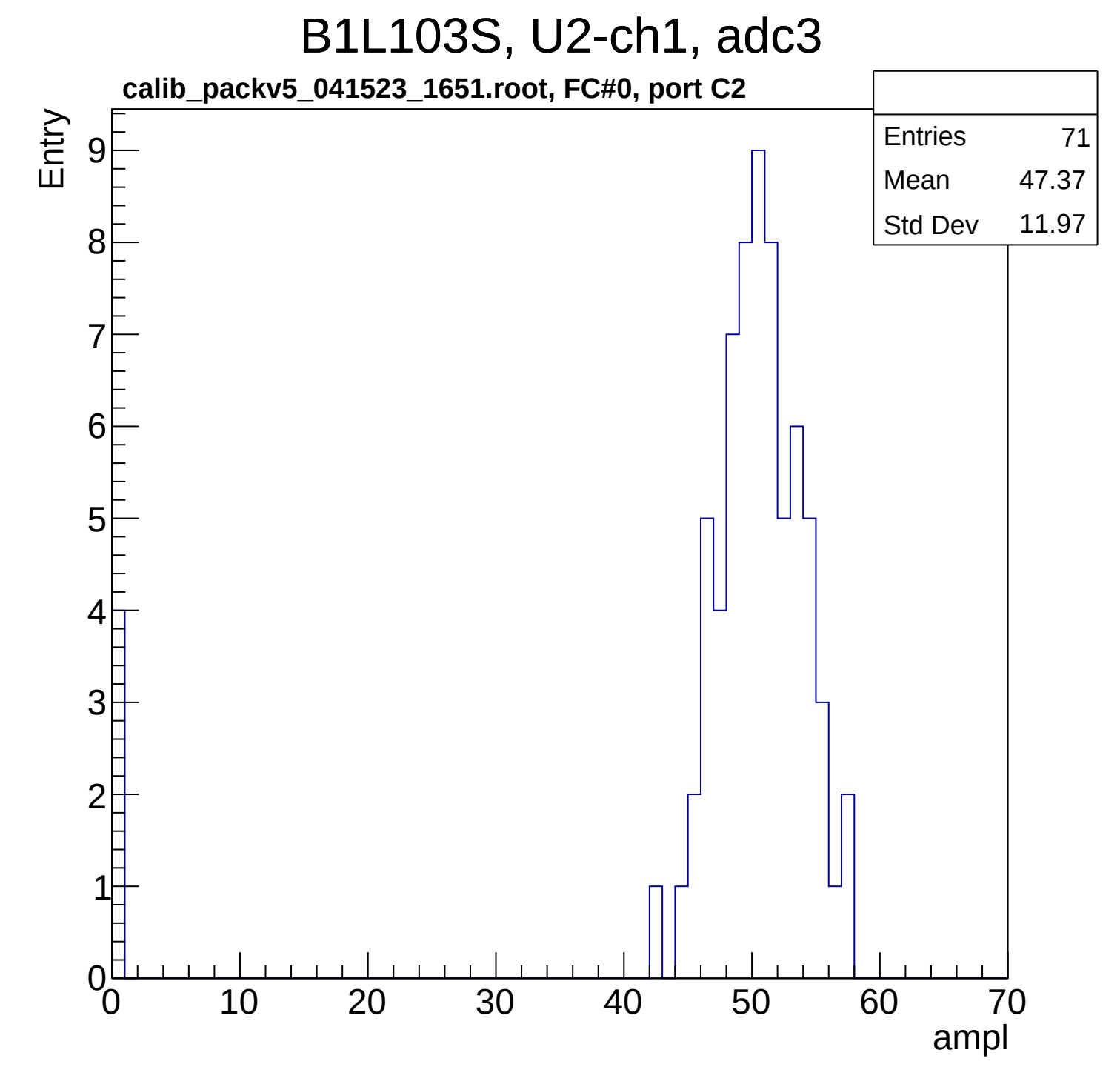

B1L103S, U2-ch0, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 58.05
Std Dev 9.934
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

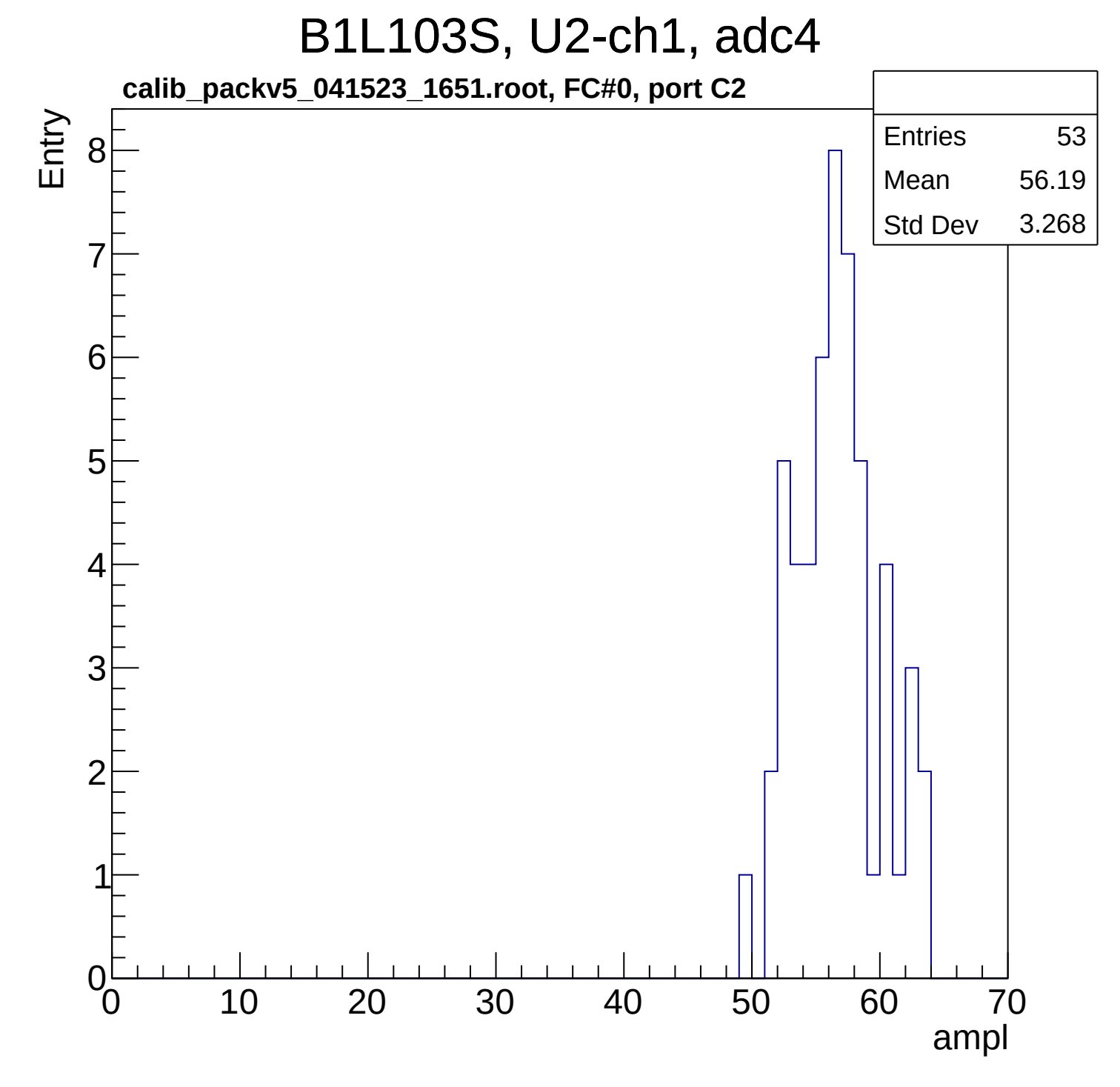

B1L103S, U2-ch0, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 16.77
Std Dev 27.63
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

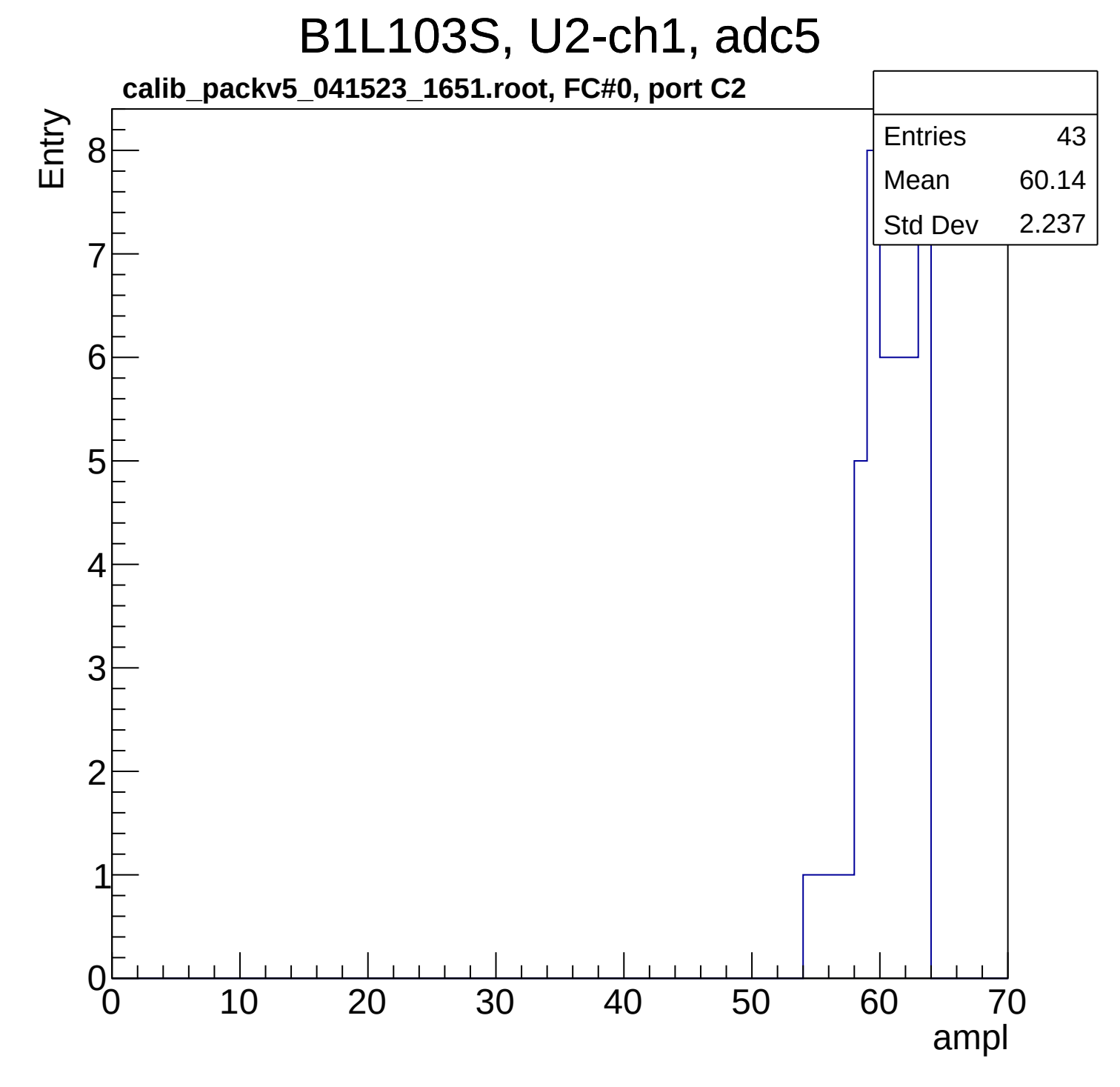

B1L103S, U2-ch1, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 27.3
Std Dev 9.857
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

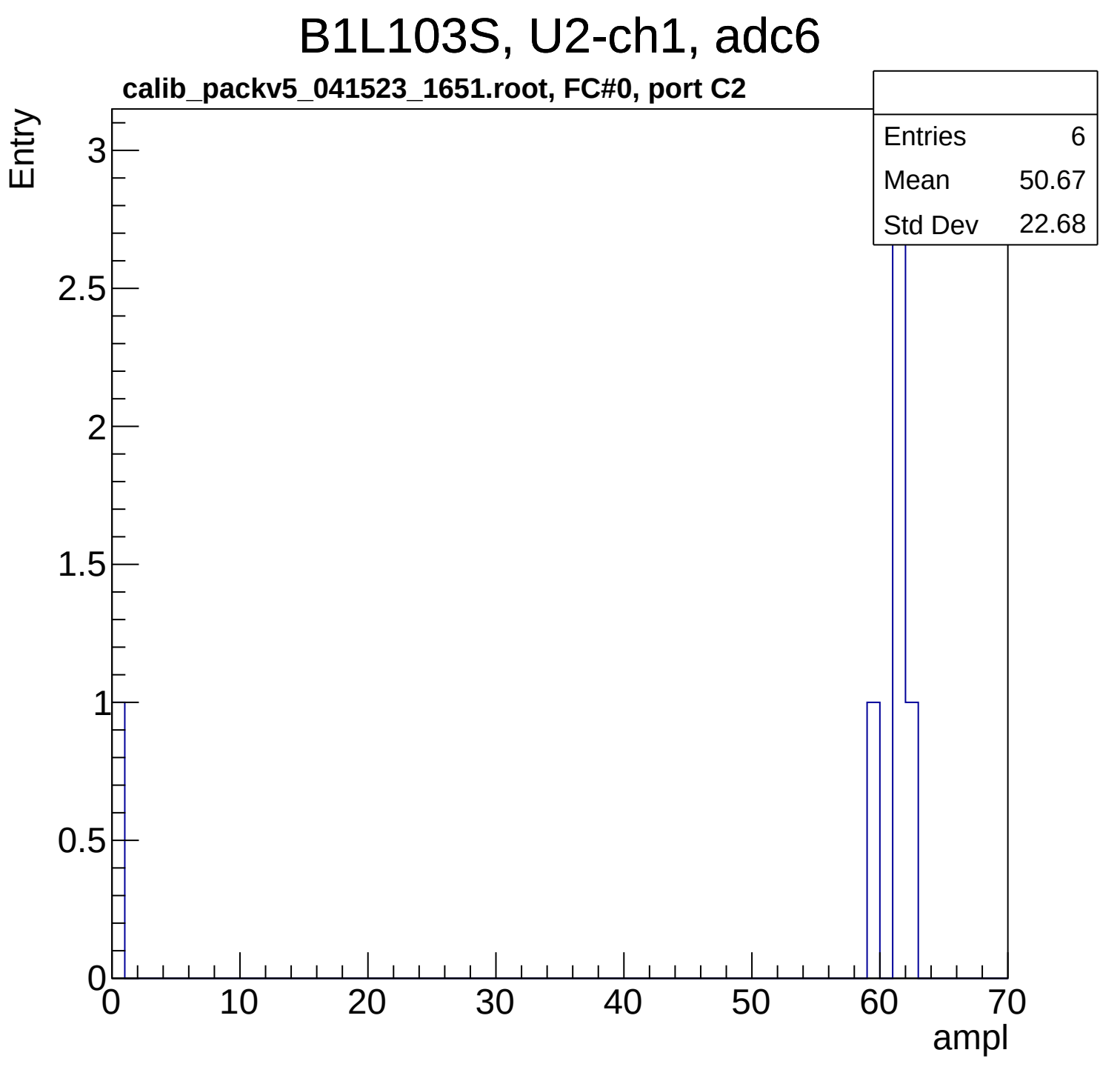

B1L103S, U2-ch1, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 36.33
Std Dev 2.957
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

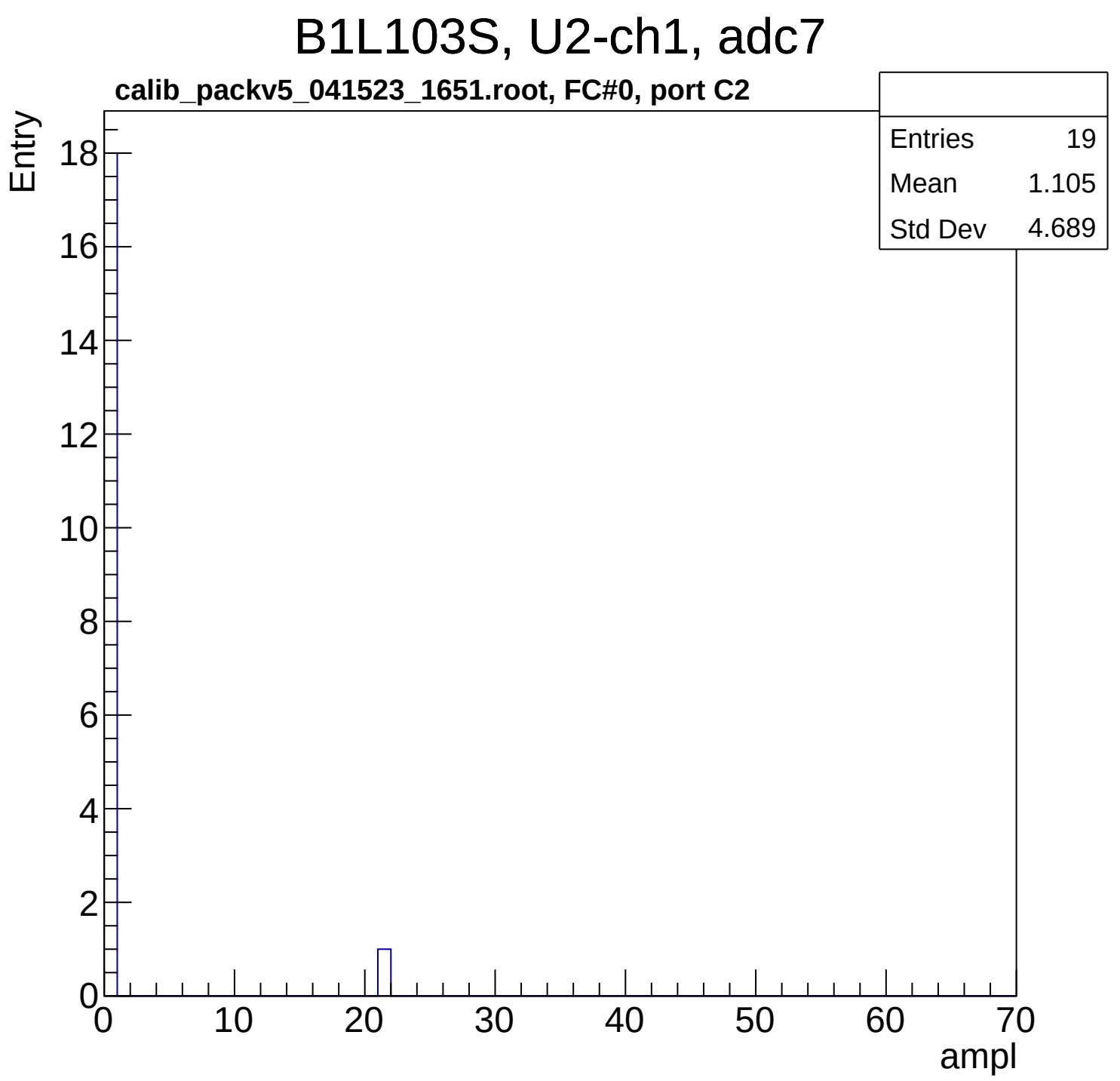

B1L103S, U2-ch1, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 37.04
Std Dev 14.75
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

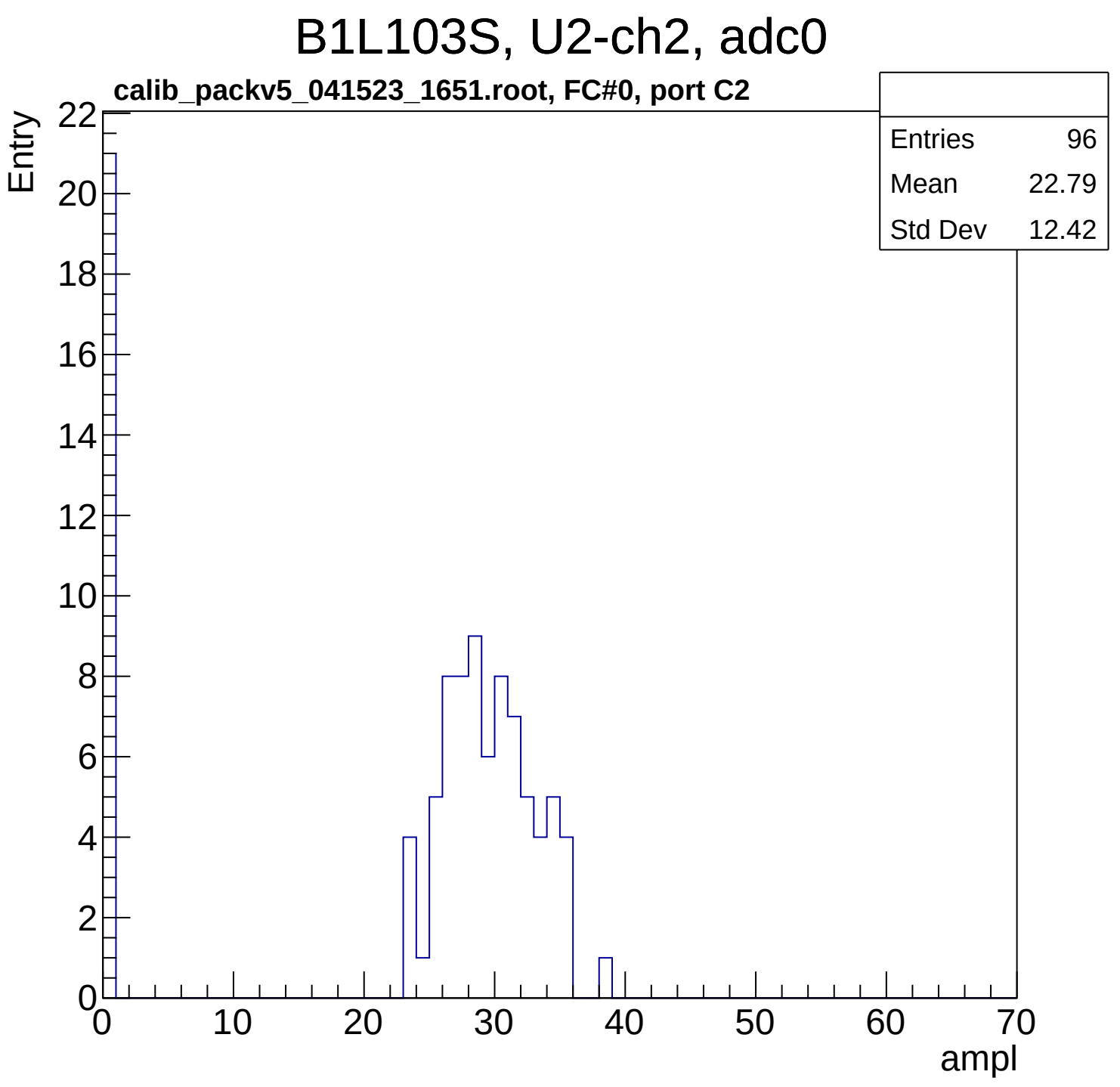

B1L103S, U2-ch1, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 47.37
Std Dev 11.97
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

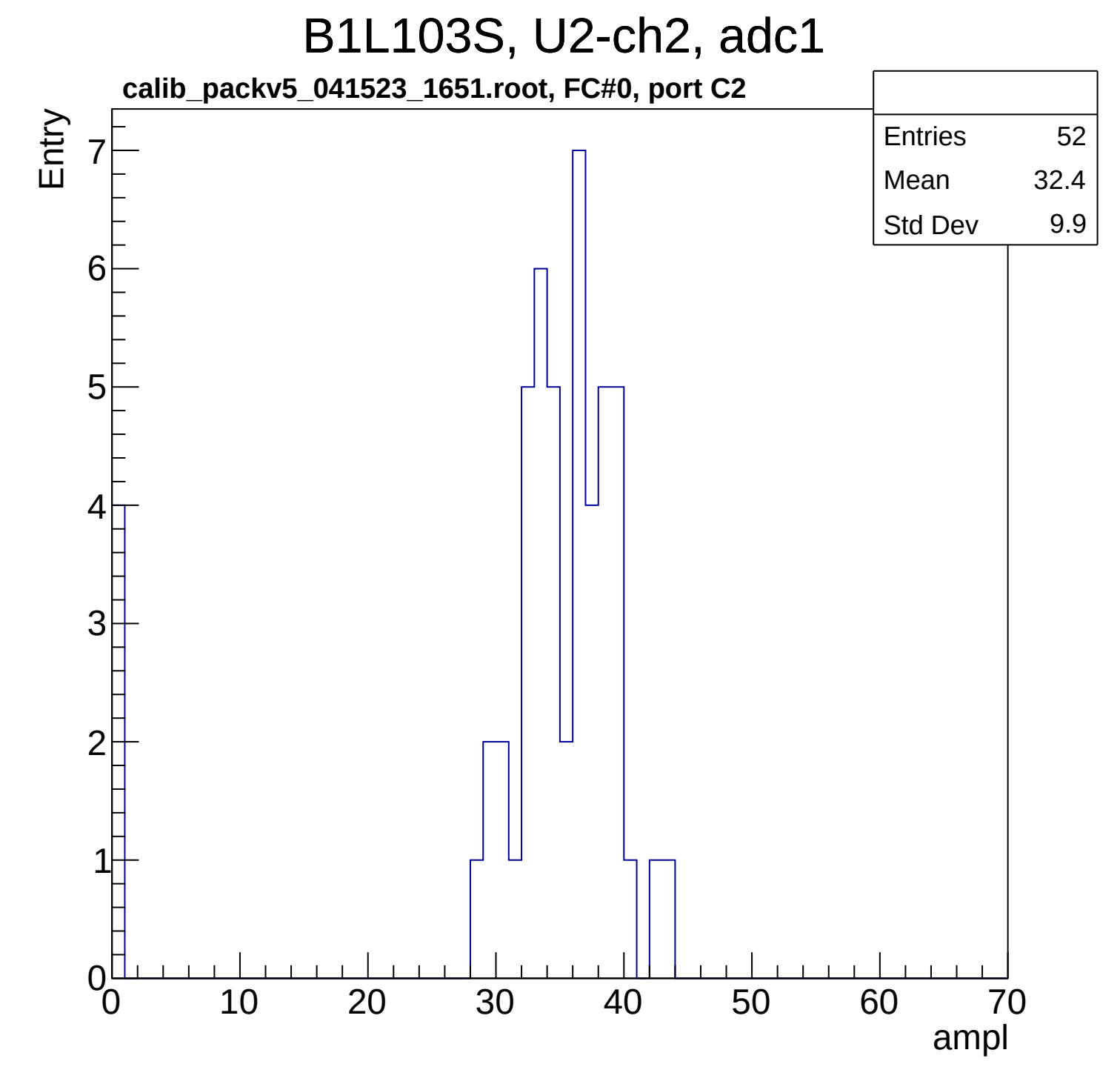

B1L103S, U2-ch1, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 56.19
Std Dev 3.268
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

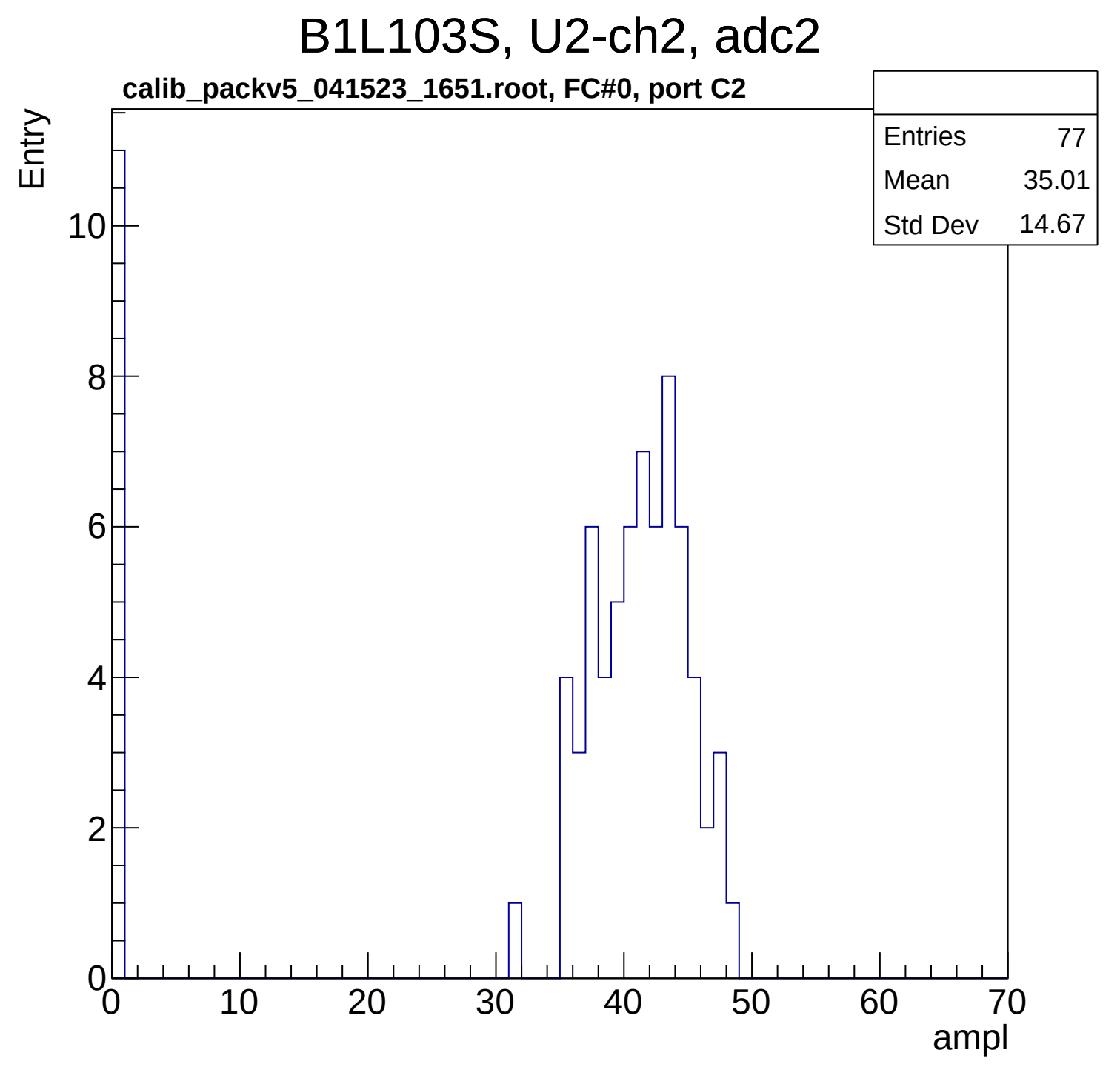

B1L103S, U2-ch1, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 60.14
Std Dev 2.237
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

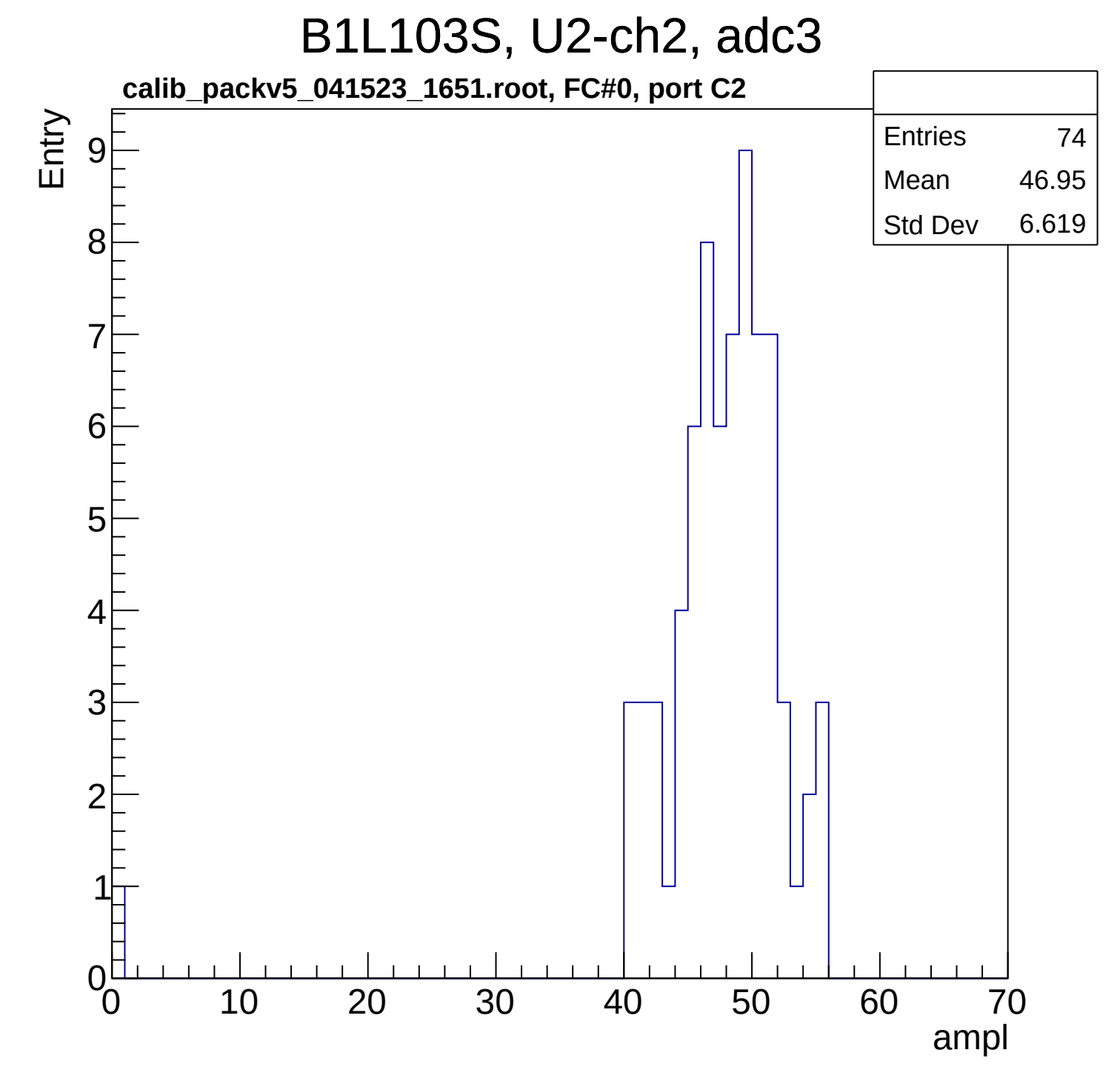

B1L103S, U2-ch1, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 50.67
Std Dev 22.68
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

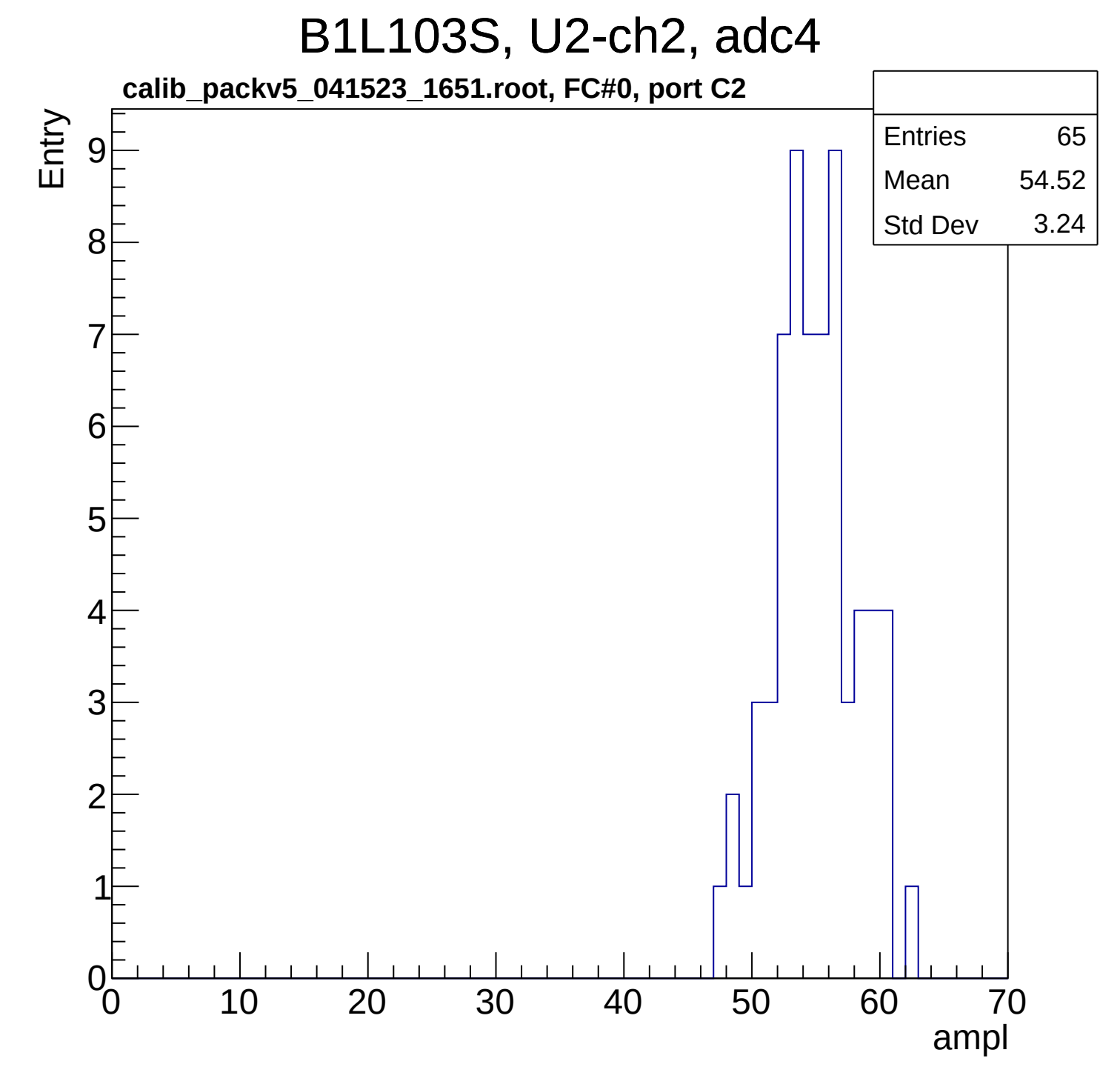

B1L103S, U2-ch1, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

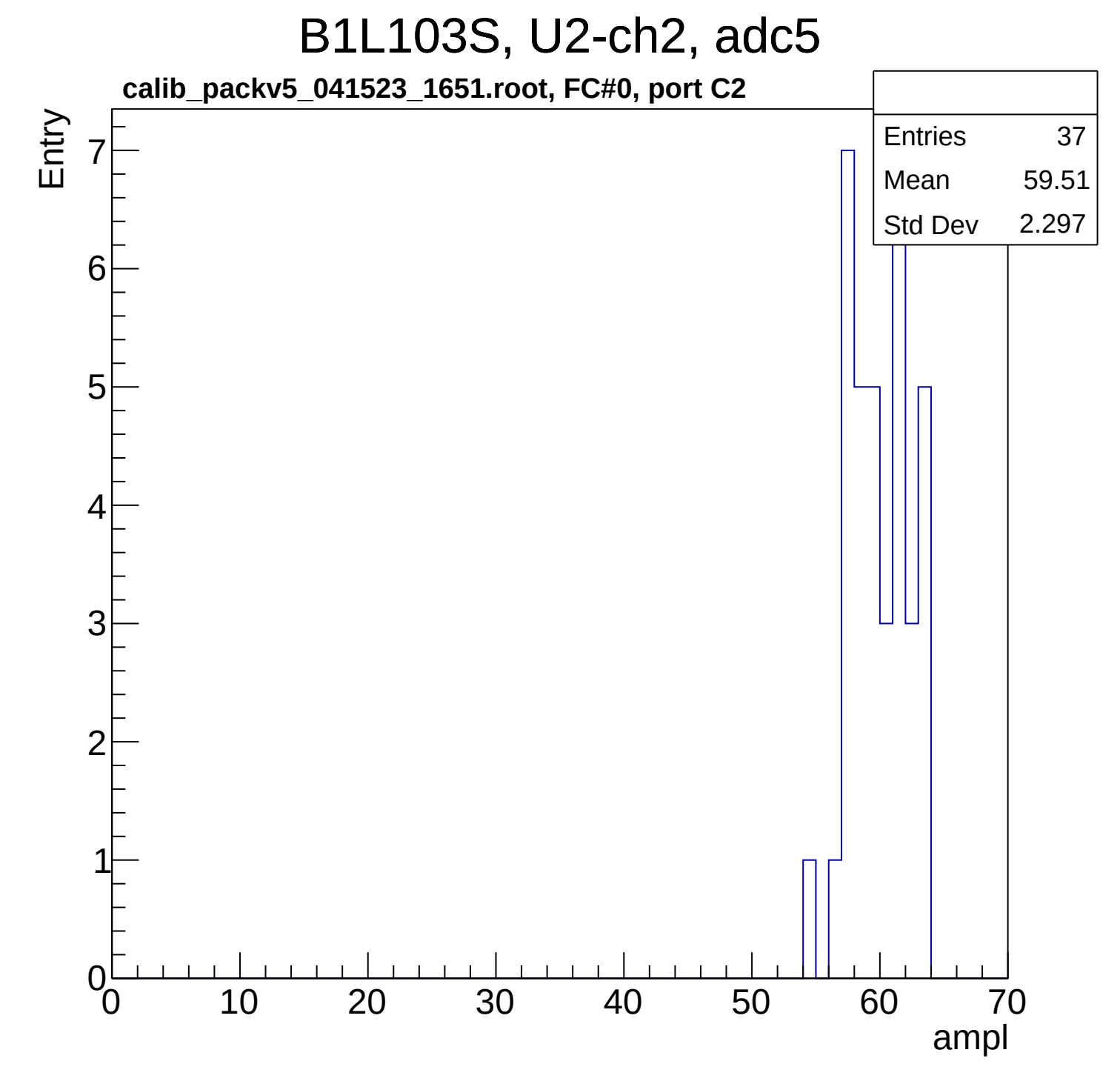

B1L103S, U2-ch2, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 22.79
Std Dev 12.42
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70

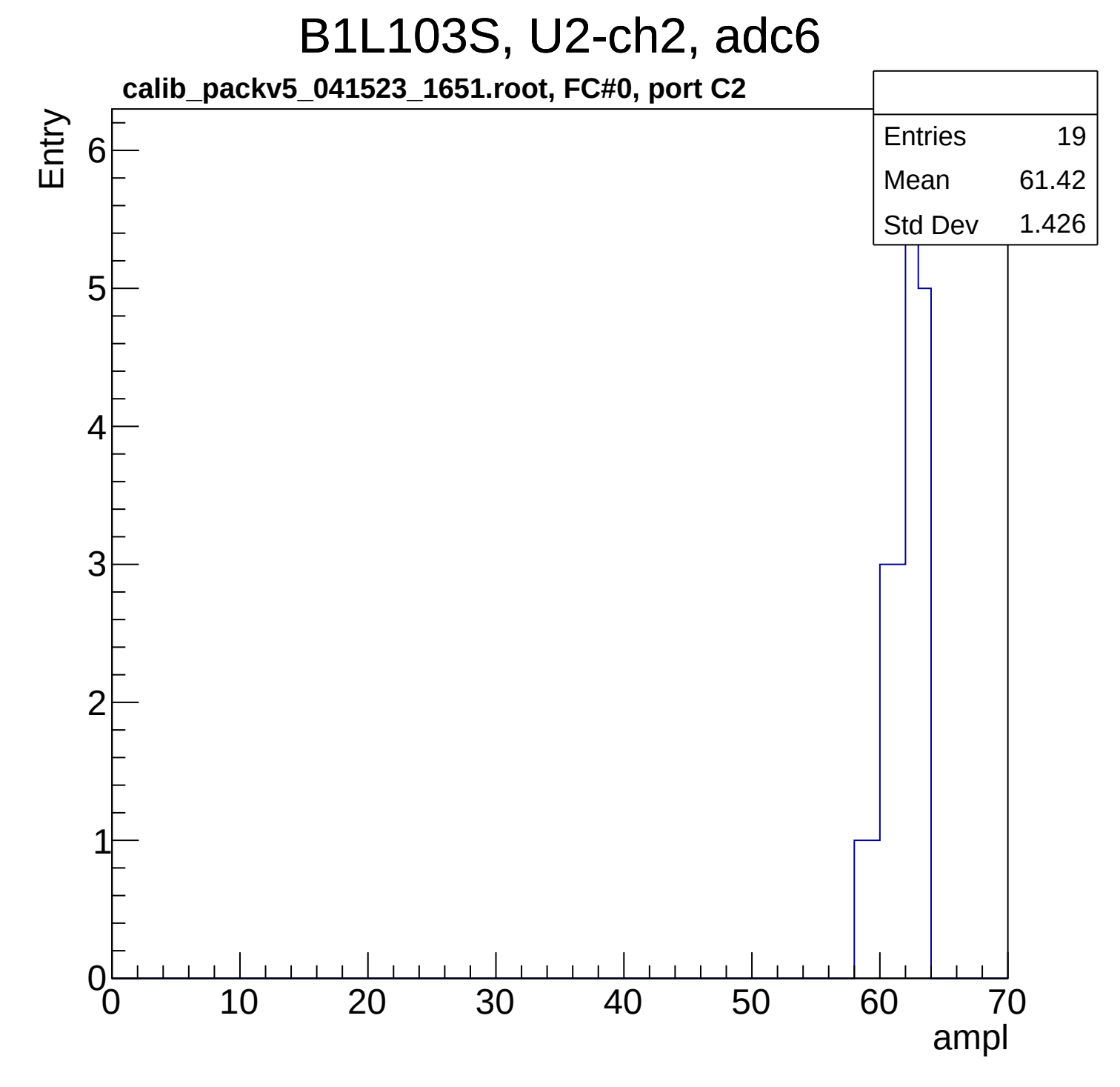

B1L103S, U2-ch2, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 32.4
Std Dev 9.9
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

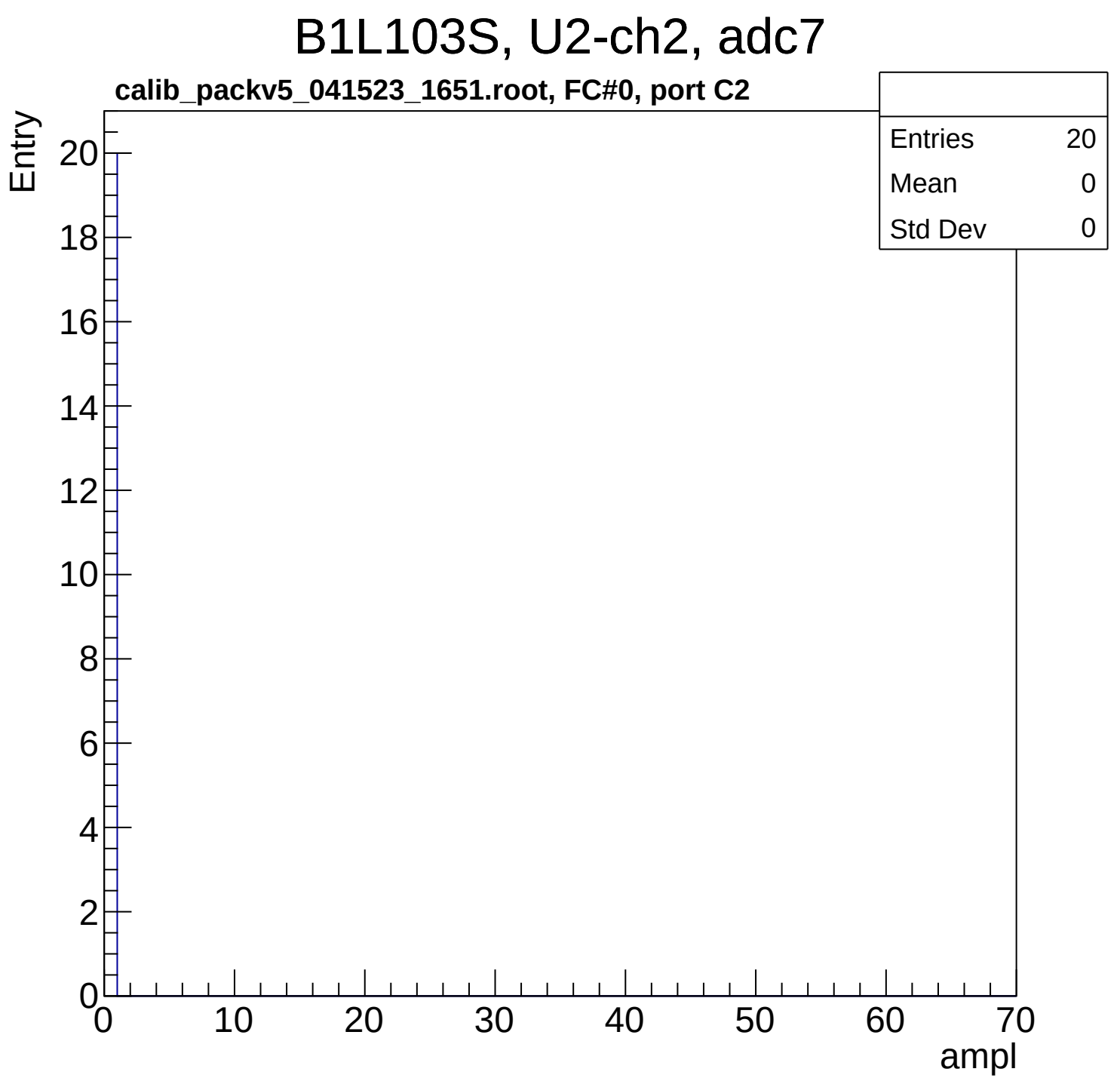

B1L103S, U2-ch2, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 35.01
Std Dev 14.67
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

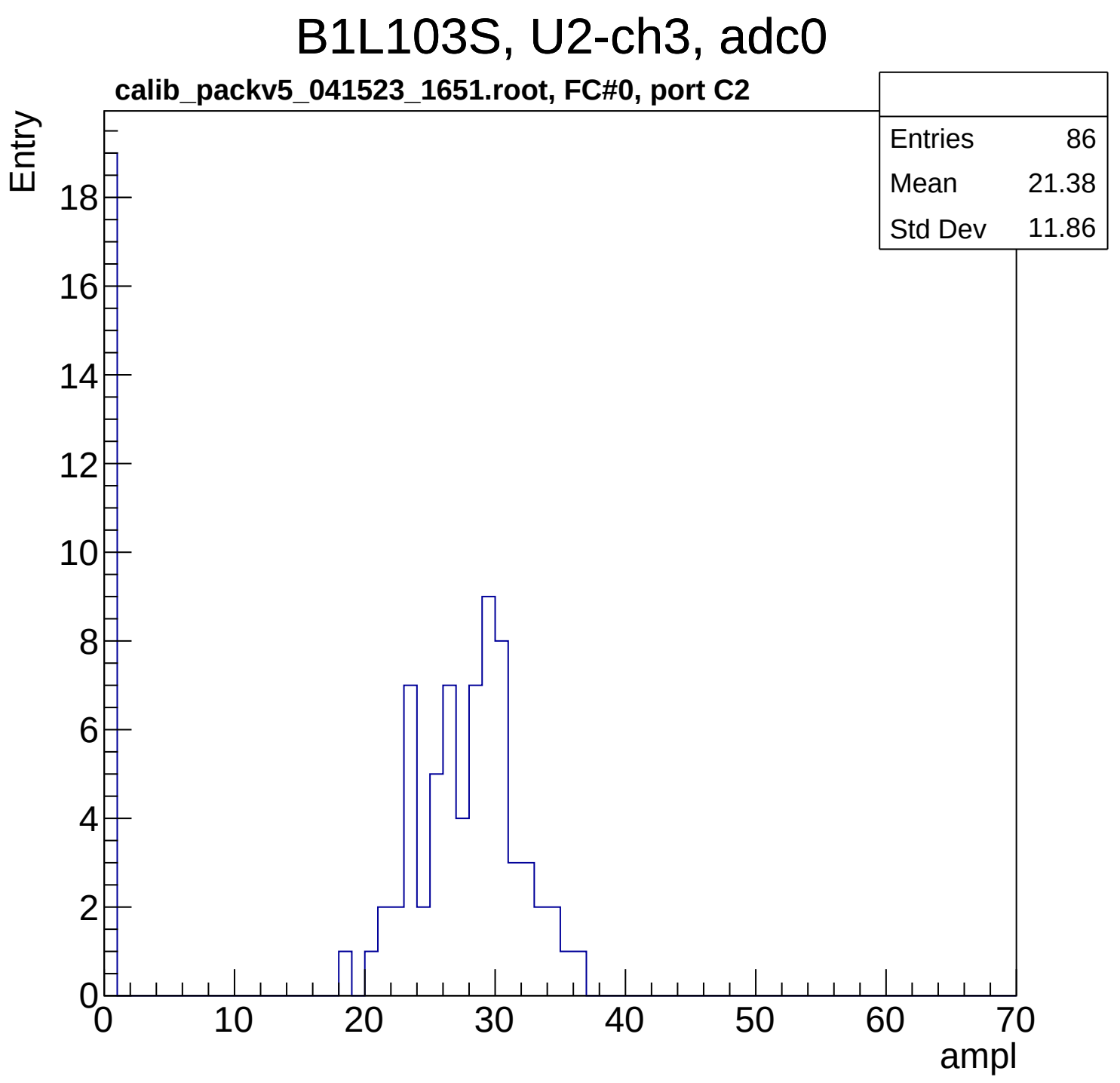

B1L103S, U2-ch2, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 46.95
Std Dev 6.619
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

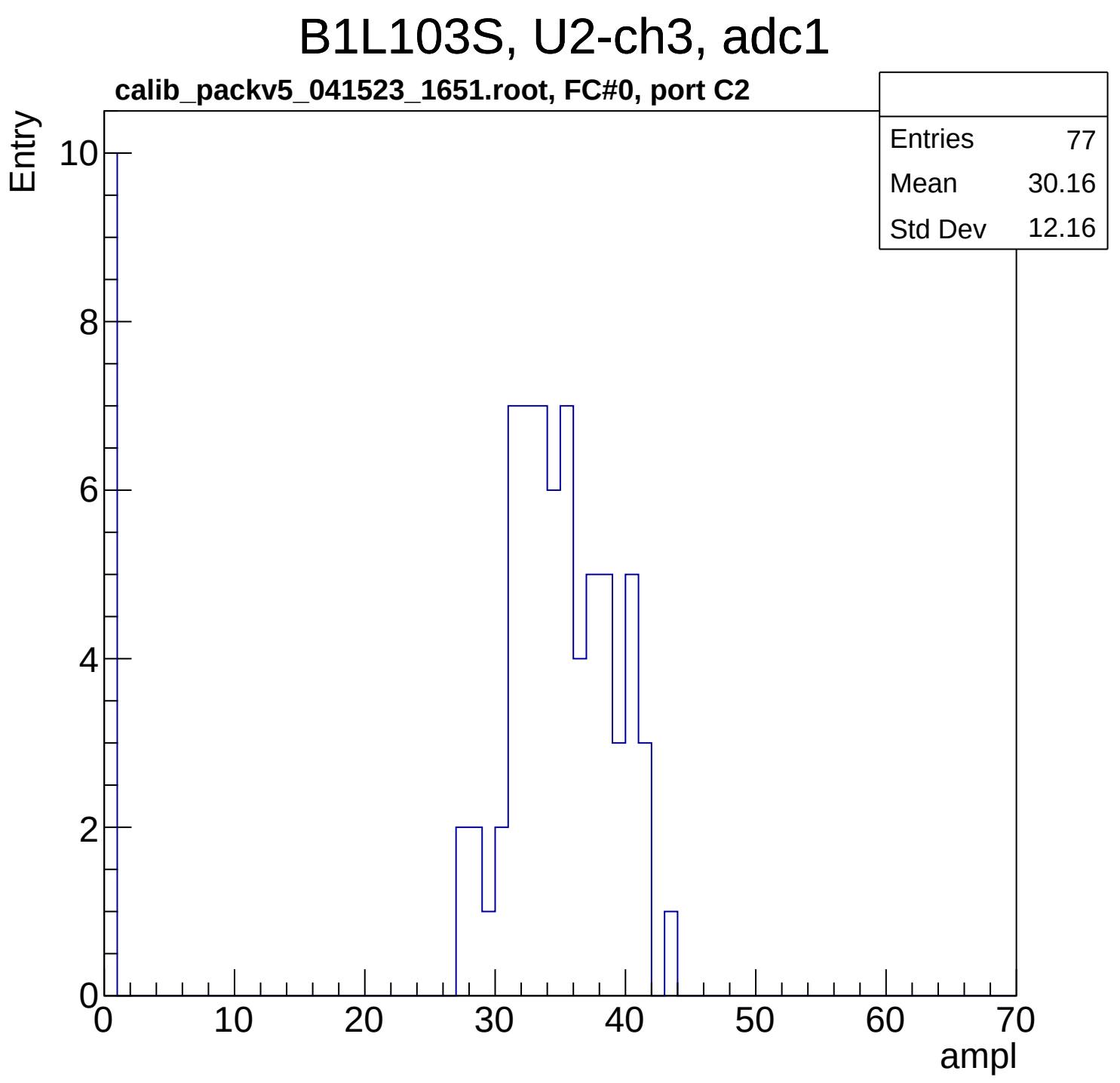

B1L103S, U2-ch2, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 54.52
Std Dev 3.24
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

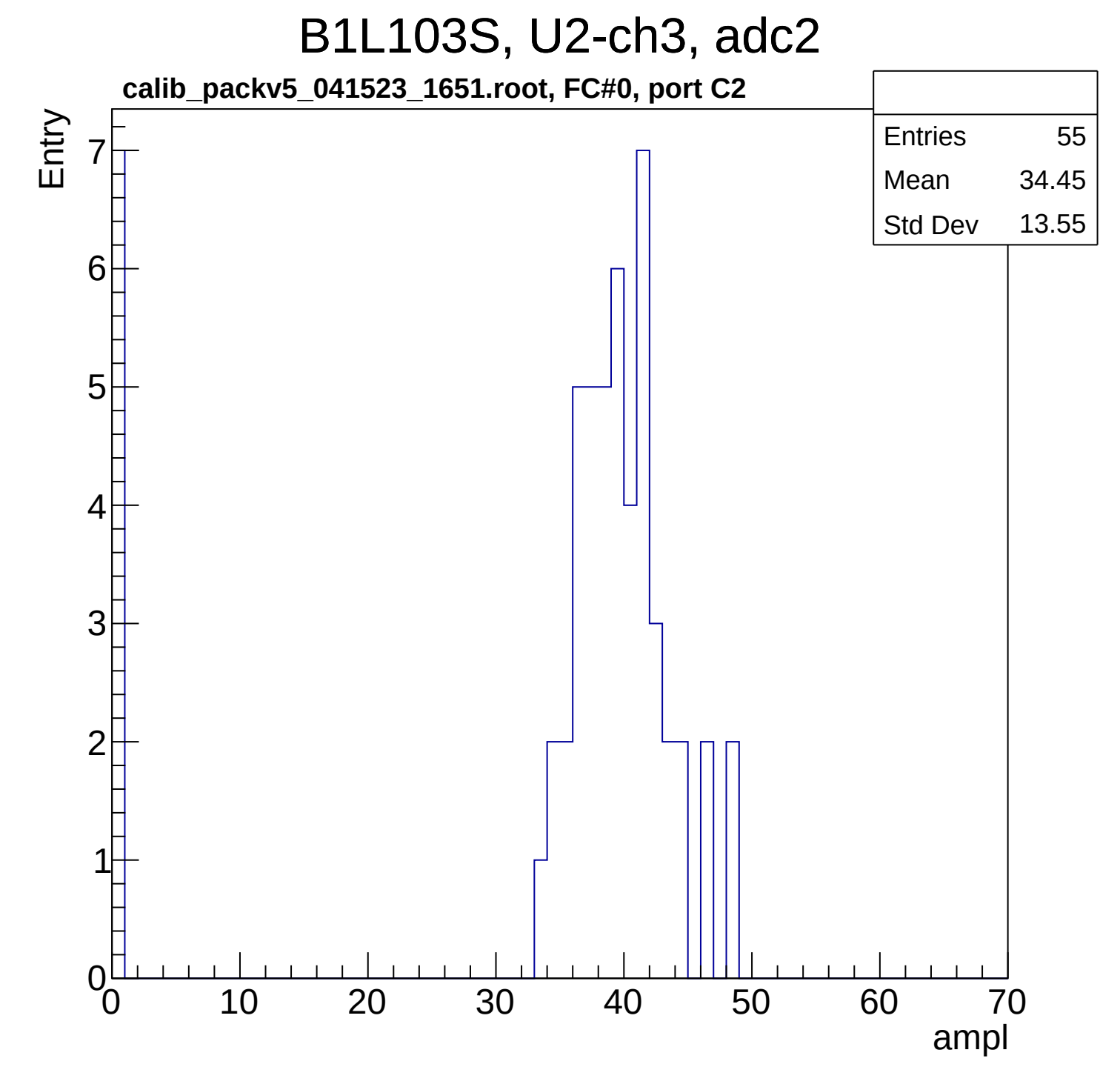

B1L103S, U2-ch2, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 59.51
Std Dev 2.297
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

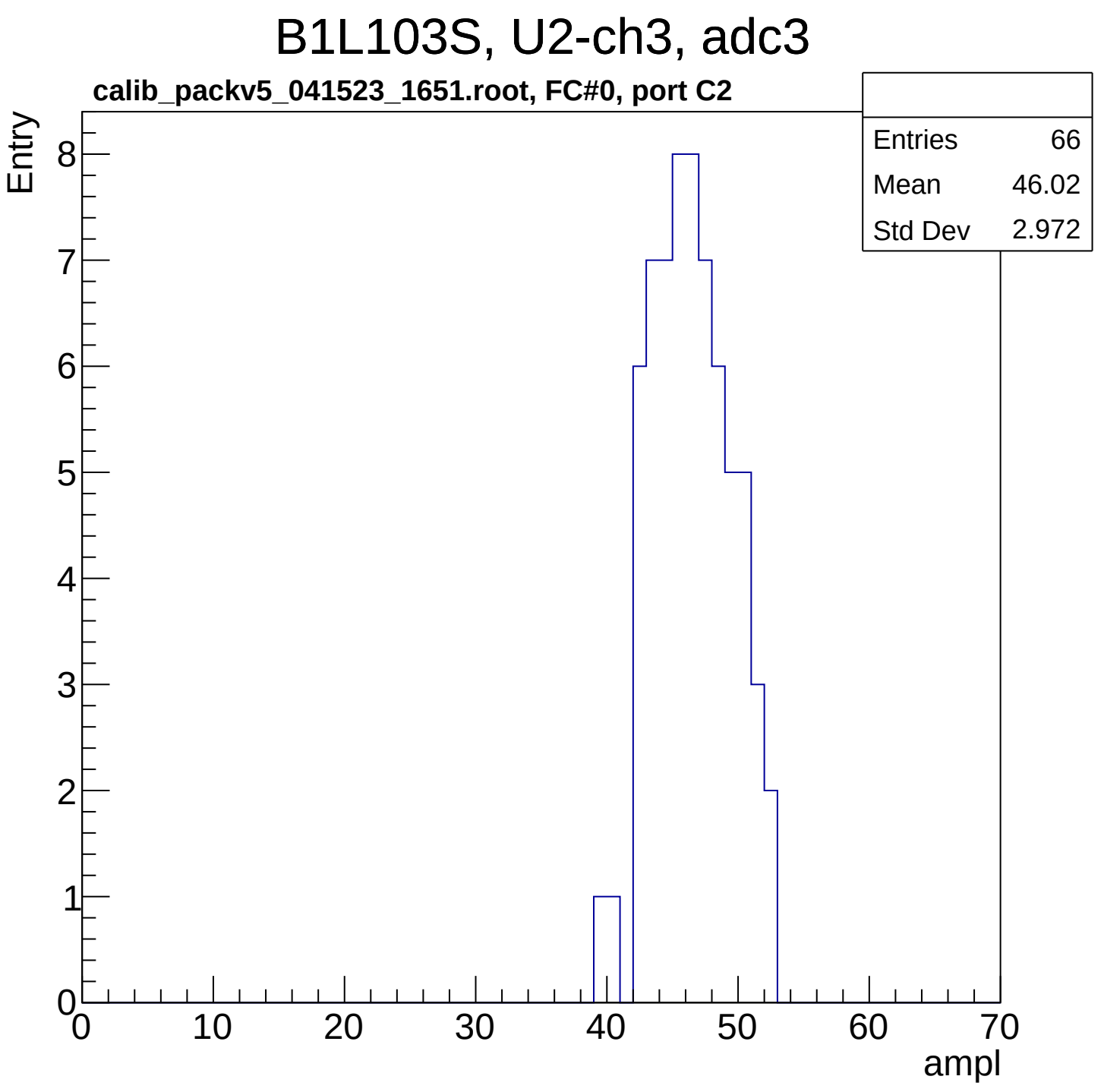

B1L103S, U2-ch2, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 61.42
Std Dev 1.426
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

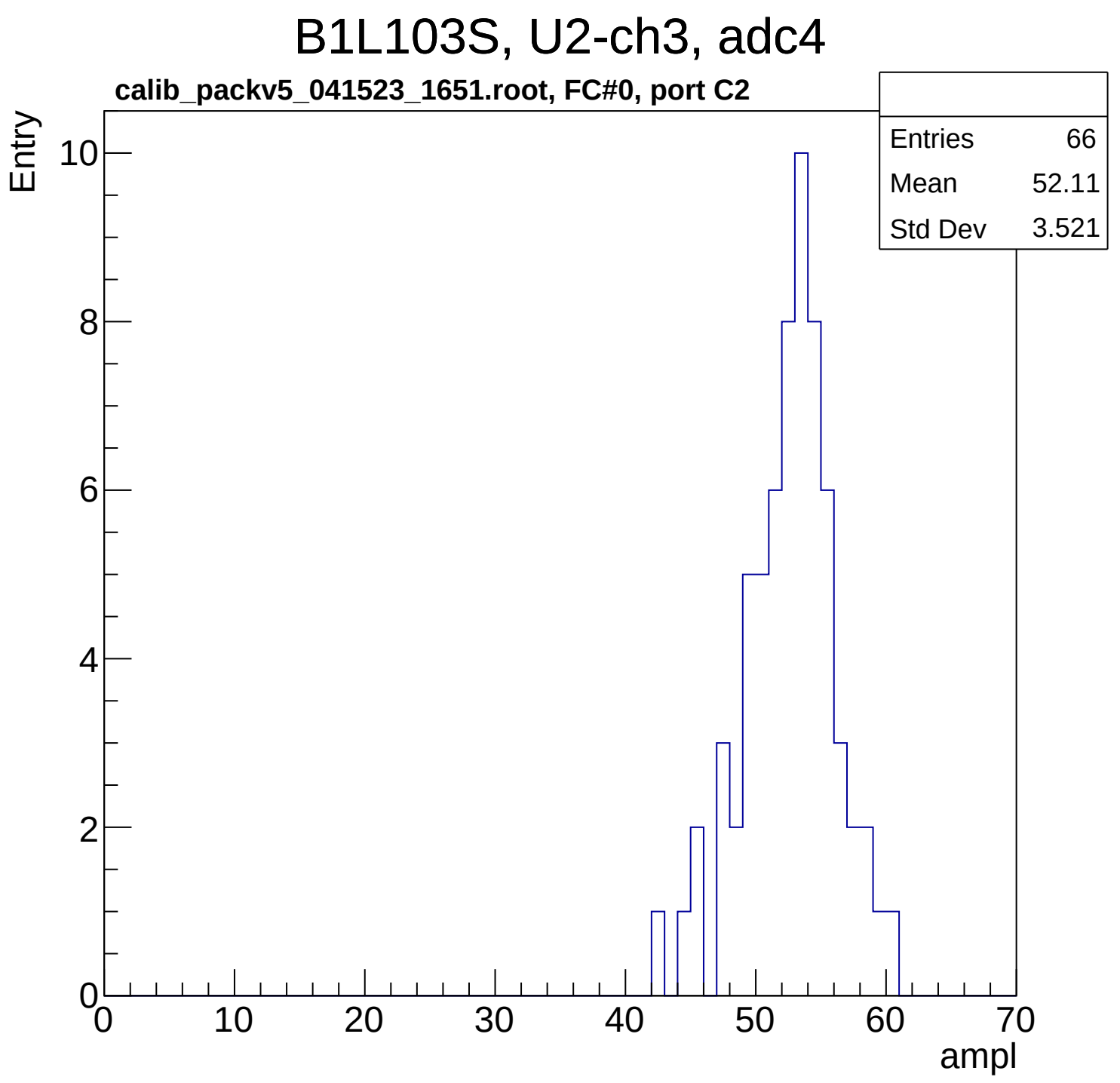

B1L103S, U2-ch2, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl

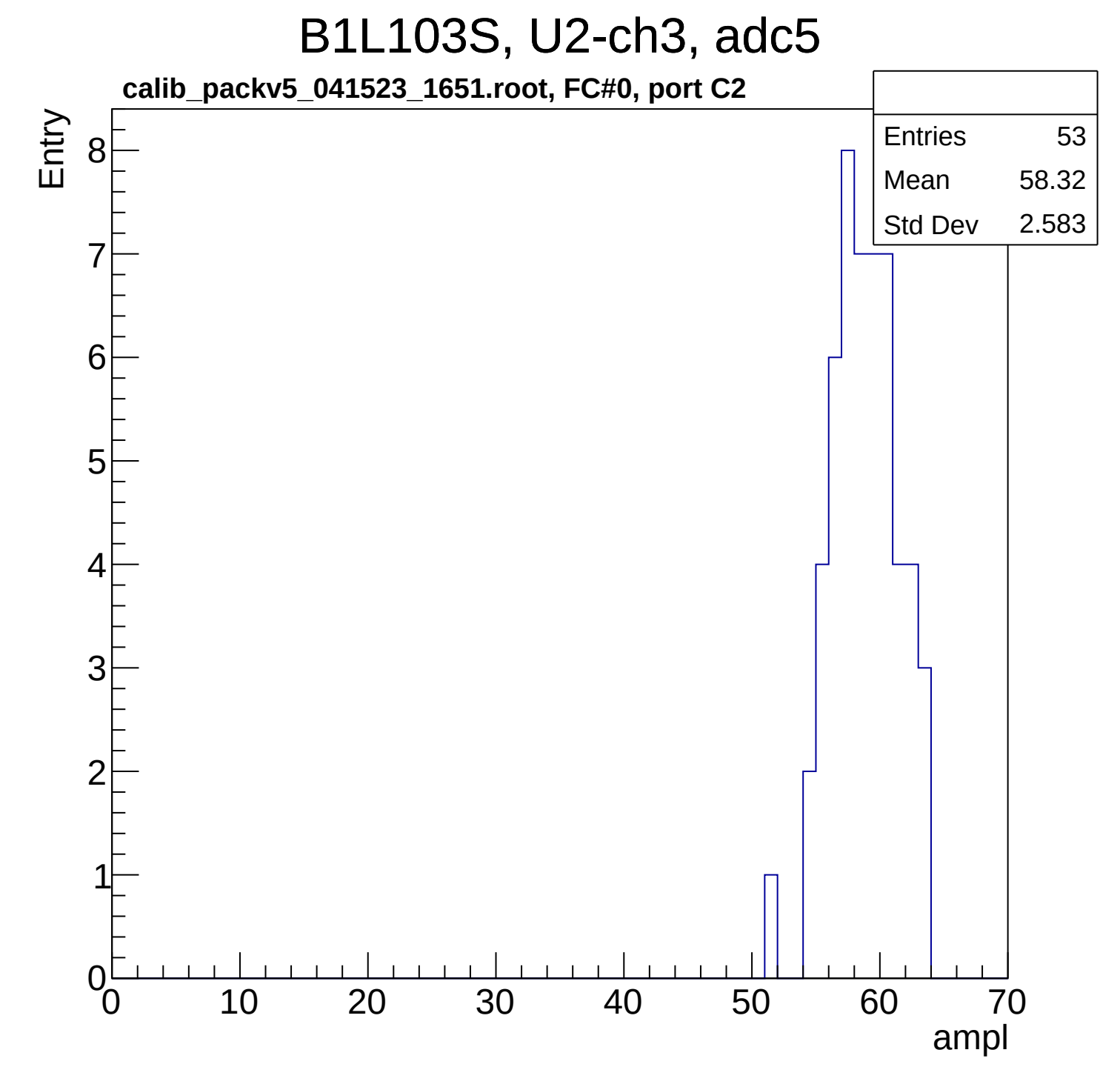

B1L103S, U2-ch3, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 21.38
Std Dev 11.86
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

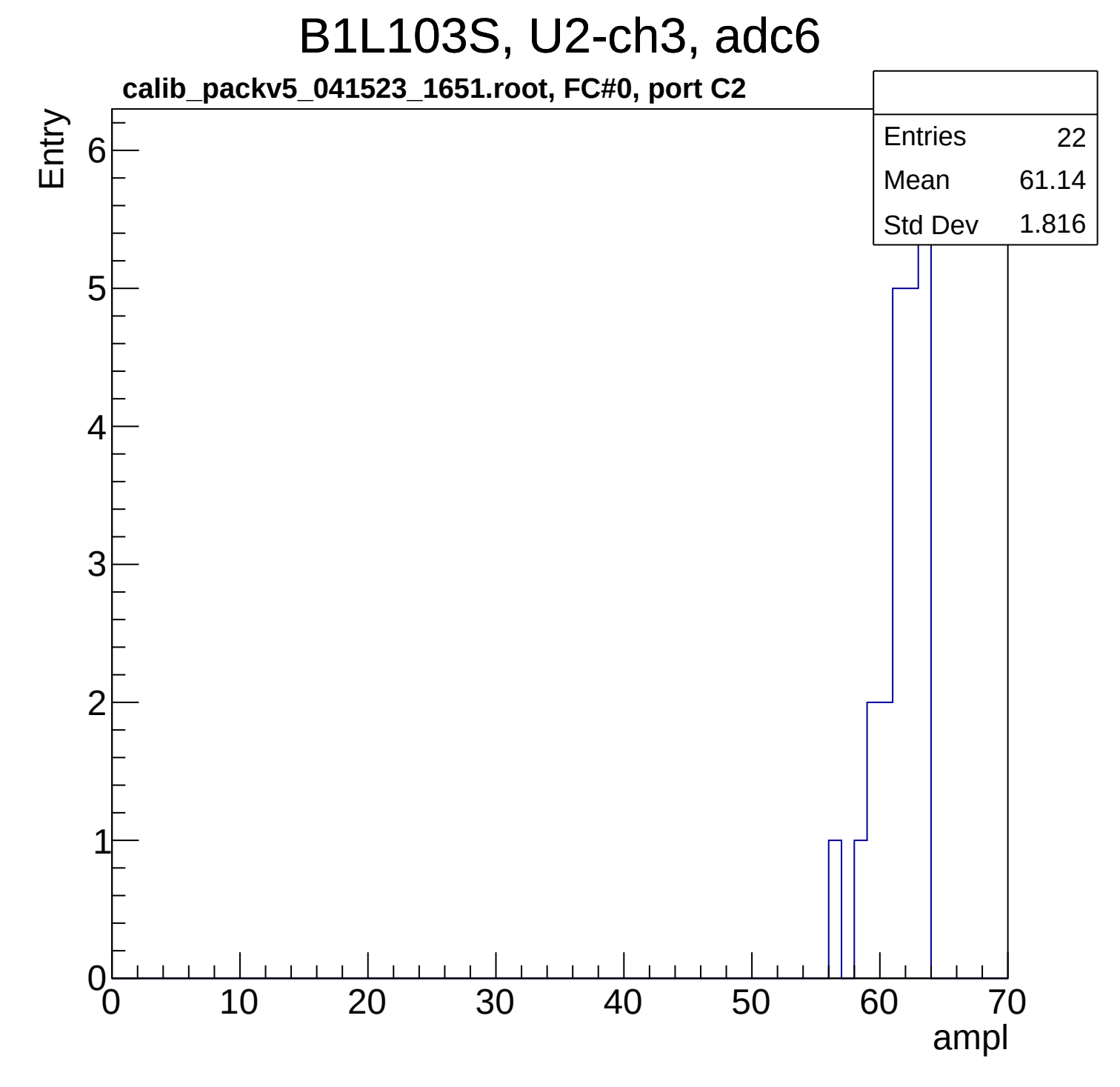

B1L103S, U2-ch3, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 30.16
Std Dev 12.16
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

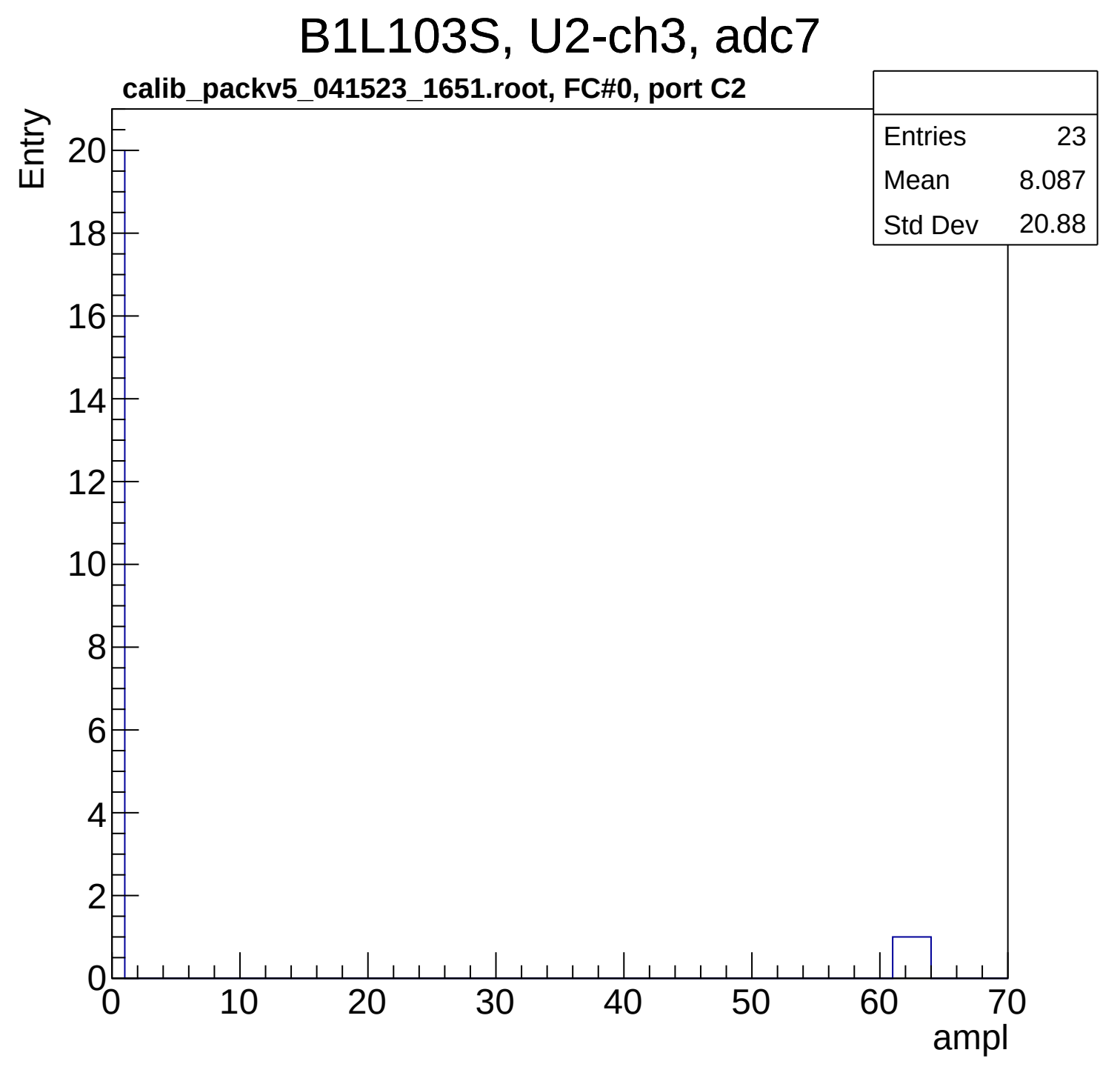

B1L103S, U2-ch3, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 34.45
Std Dev 13.55
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

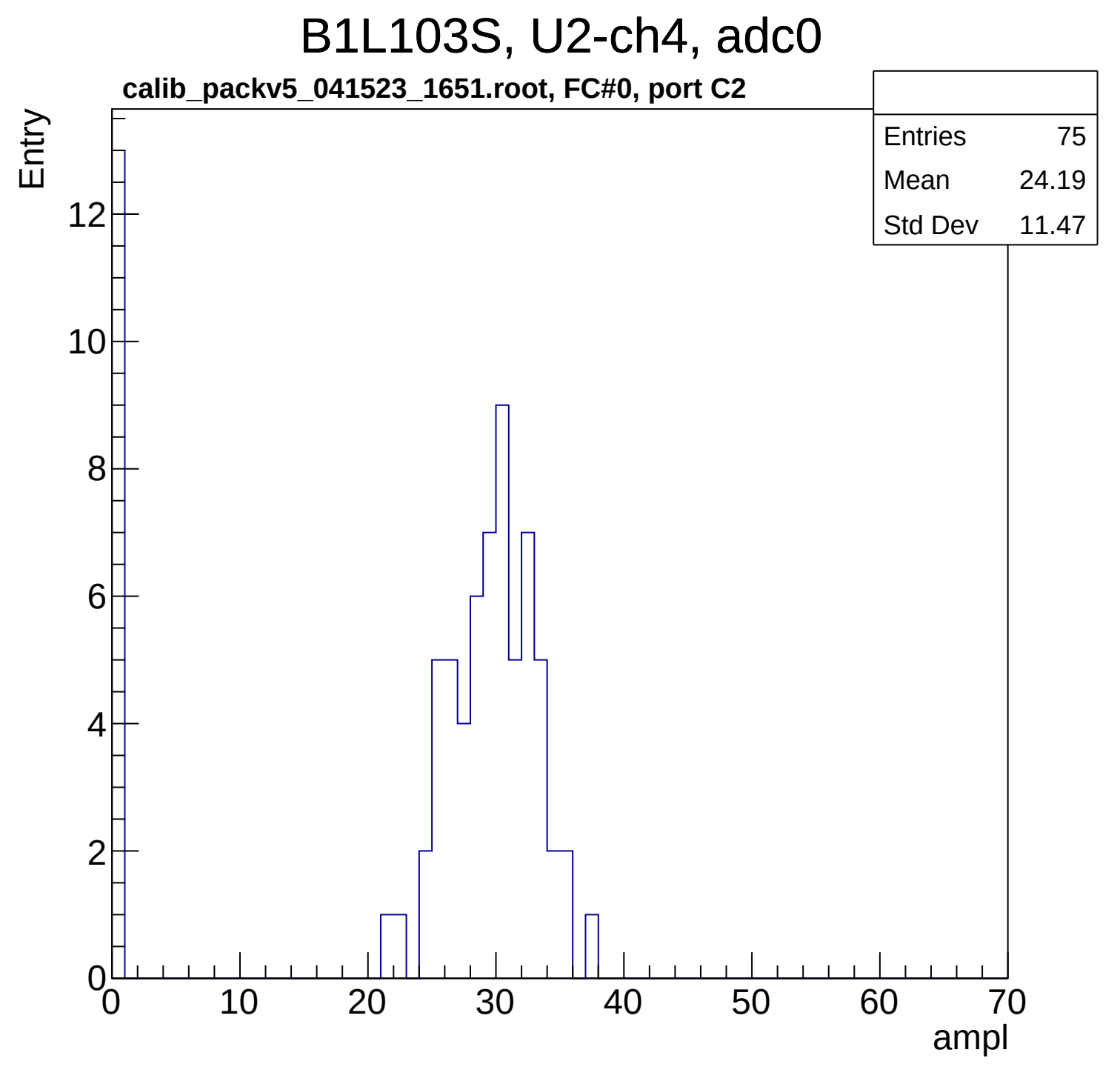

B1L103S, U2-ch3, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 46.02
Std Dev 2.972
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

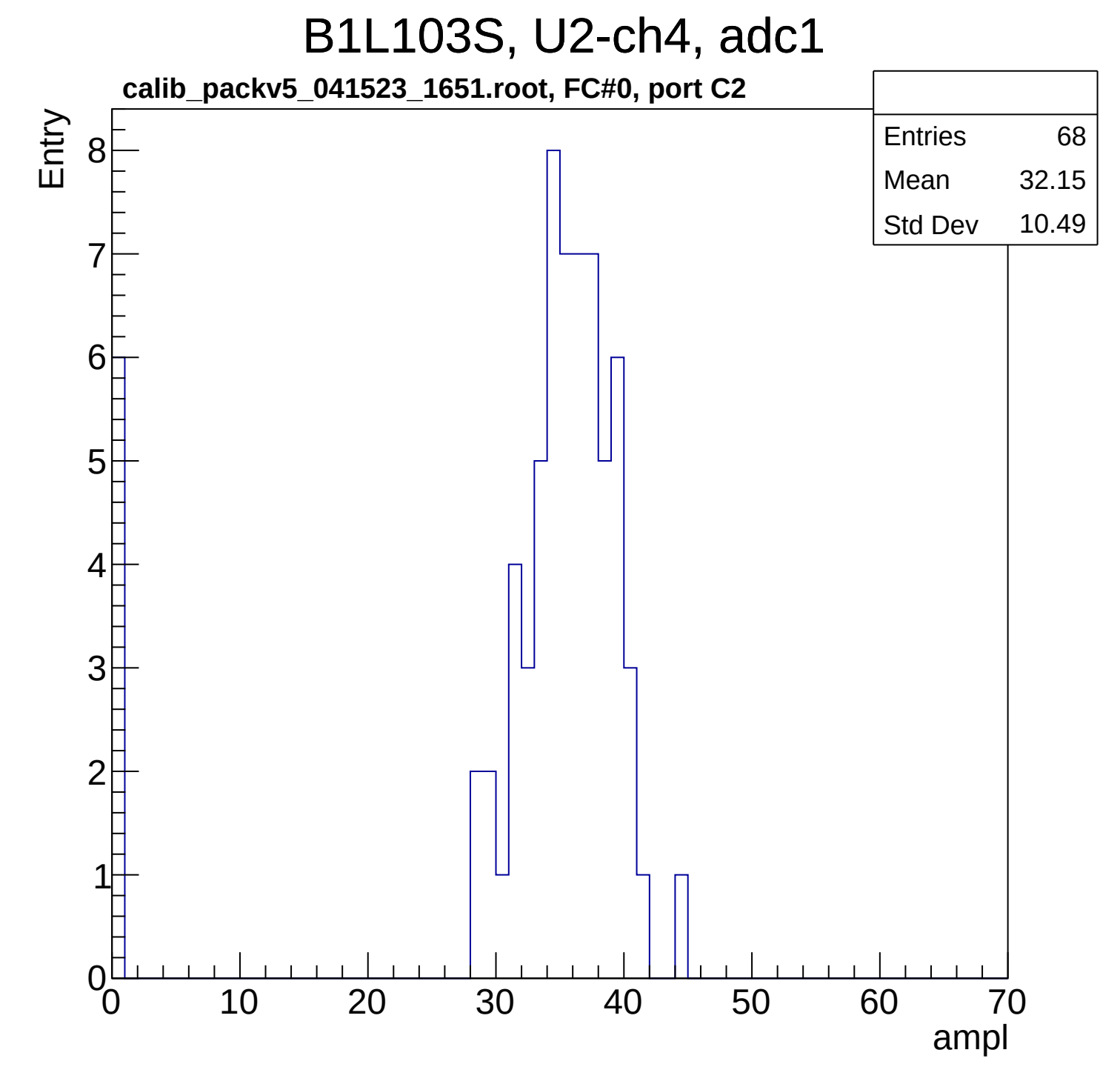

B1L103S, U2-ch3, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 52.11
Std Dev 3.521
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

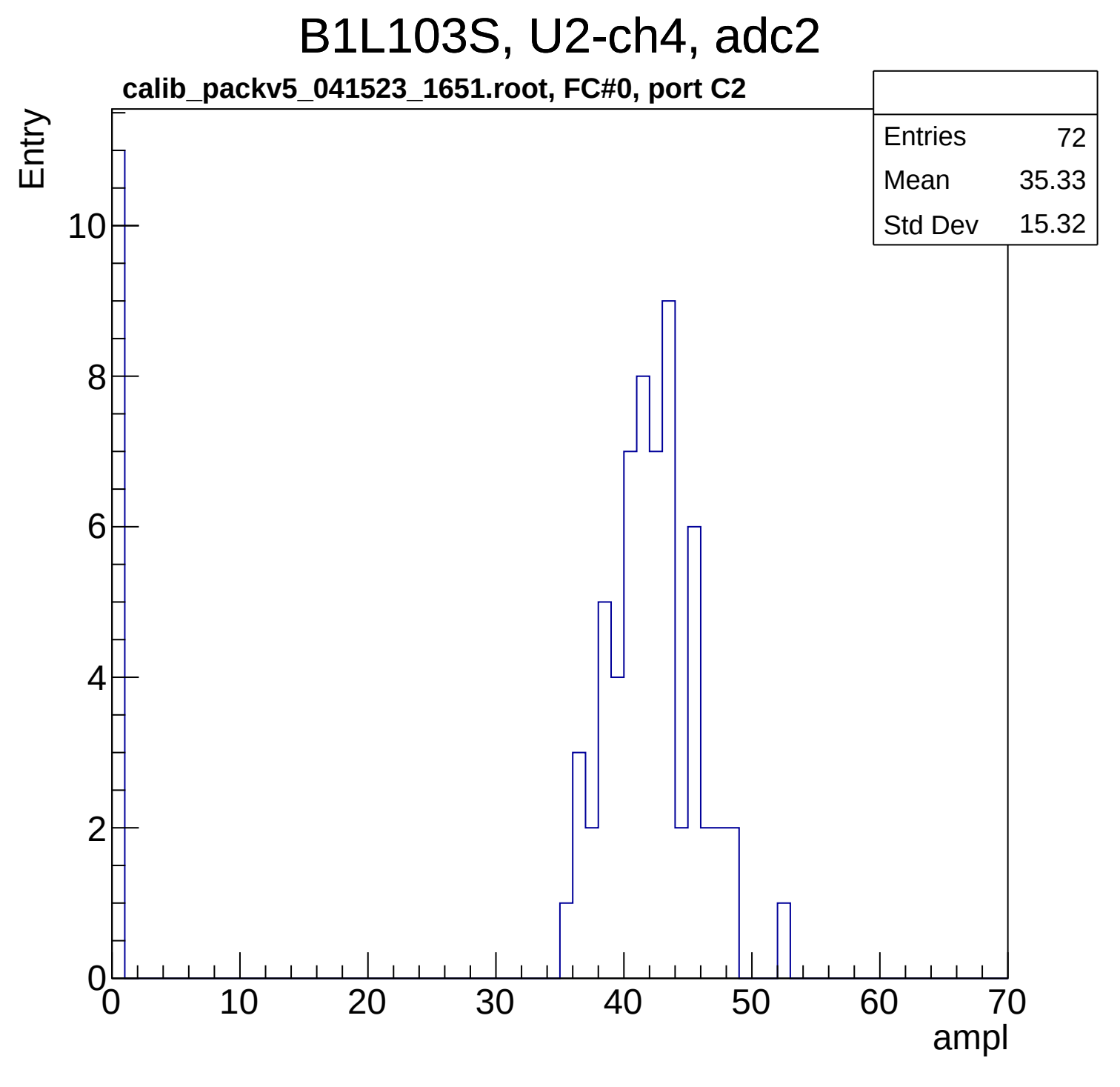

B1L103S, U2-ch3, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.32
Std Dev 2.583
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

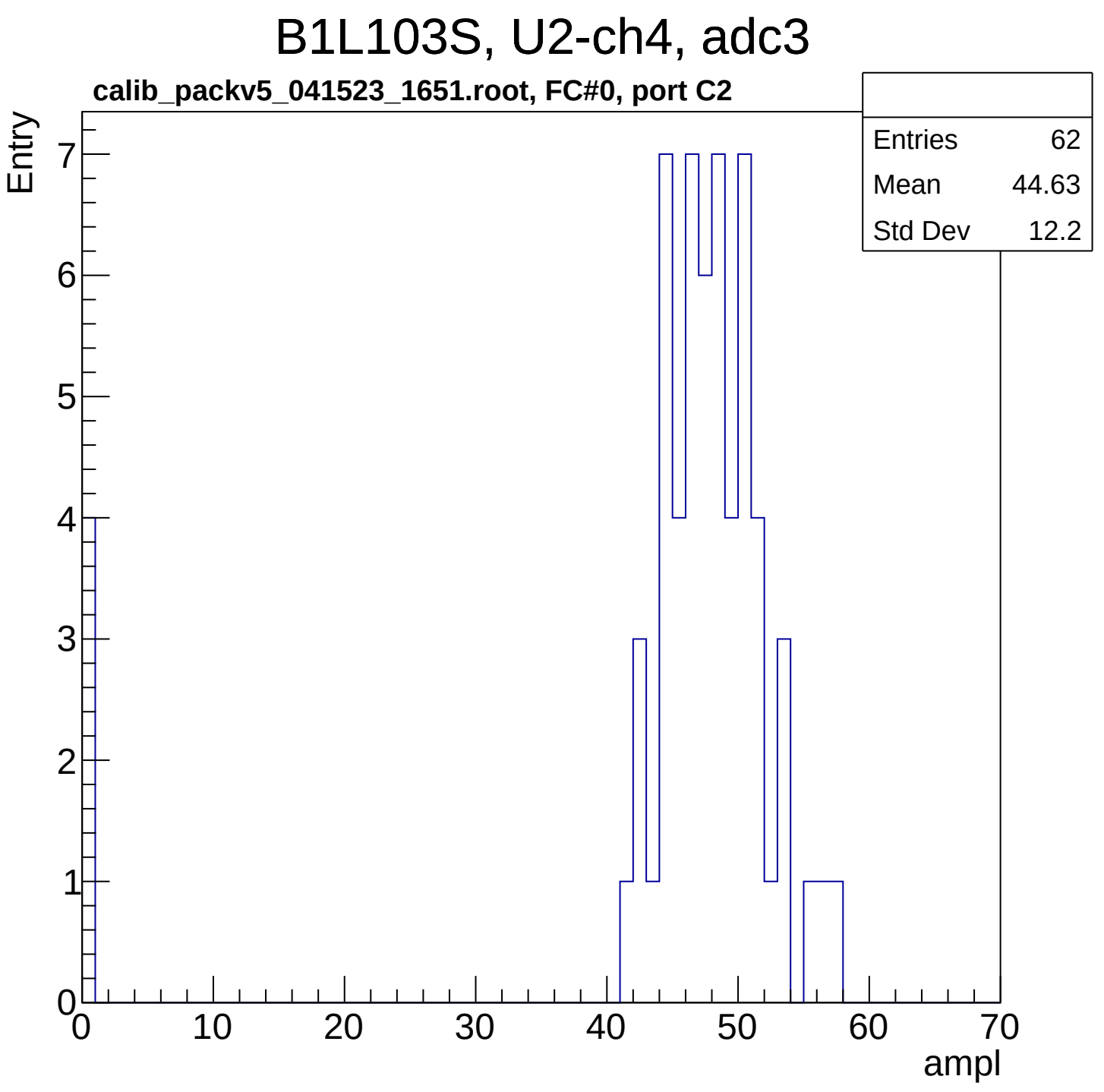

B1L103S, U2-ch3, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 61.14
Std Dev 1.816
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

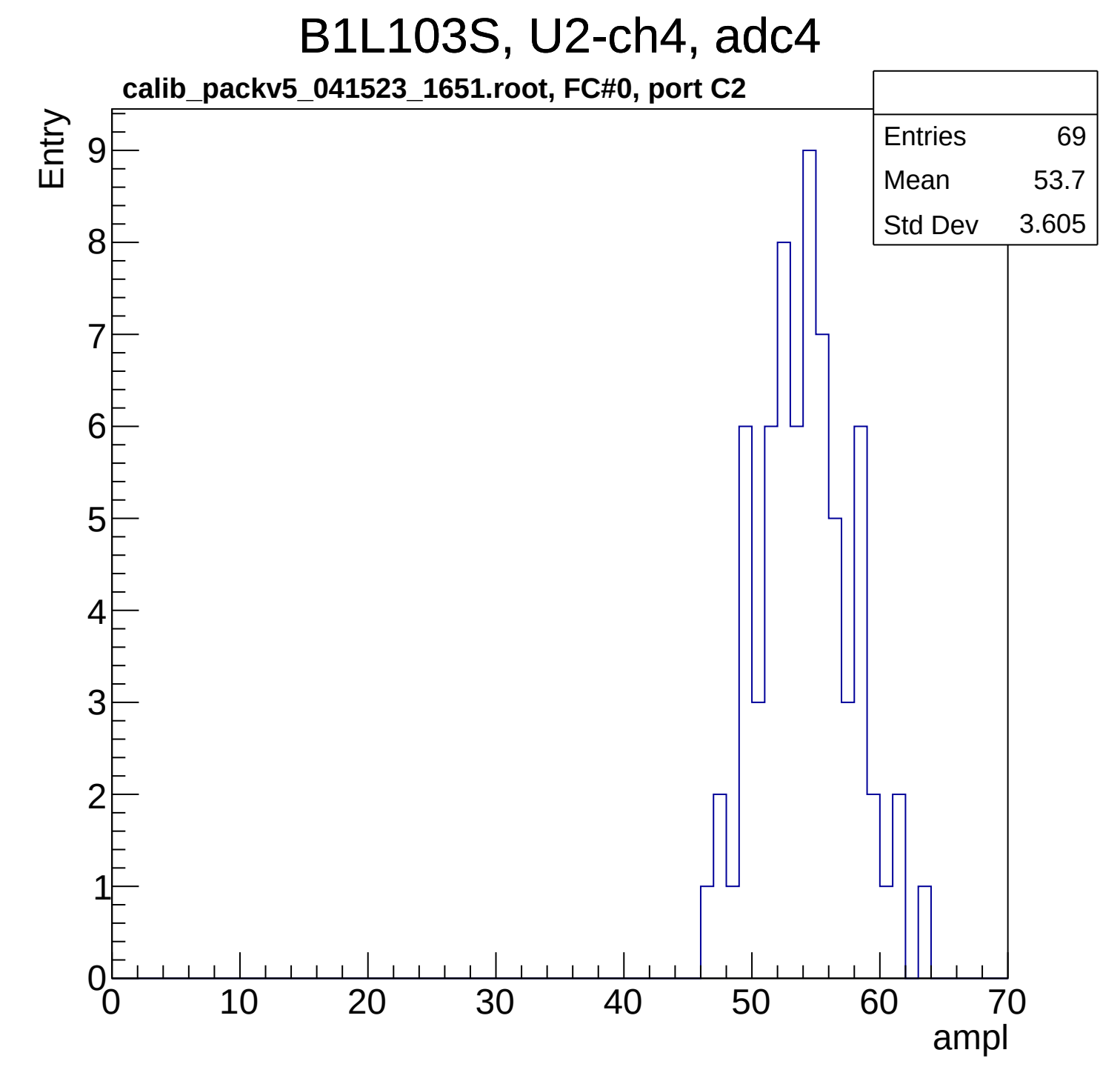

B1L103S, U2-ch3, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 8.087
Std Dev 20.88
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl

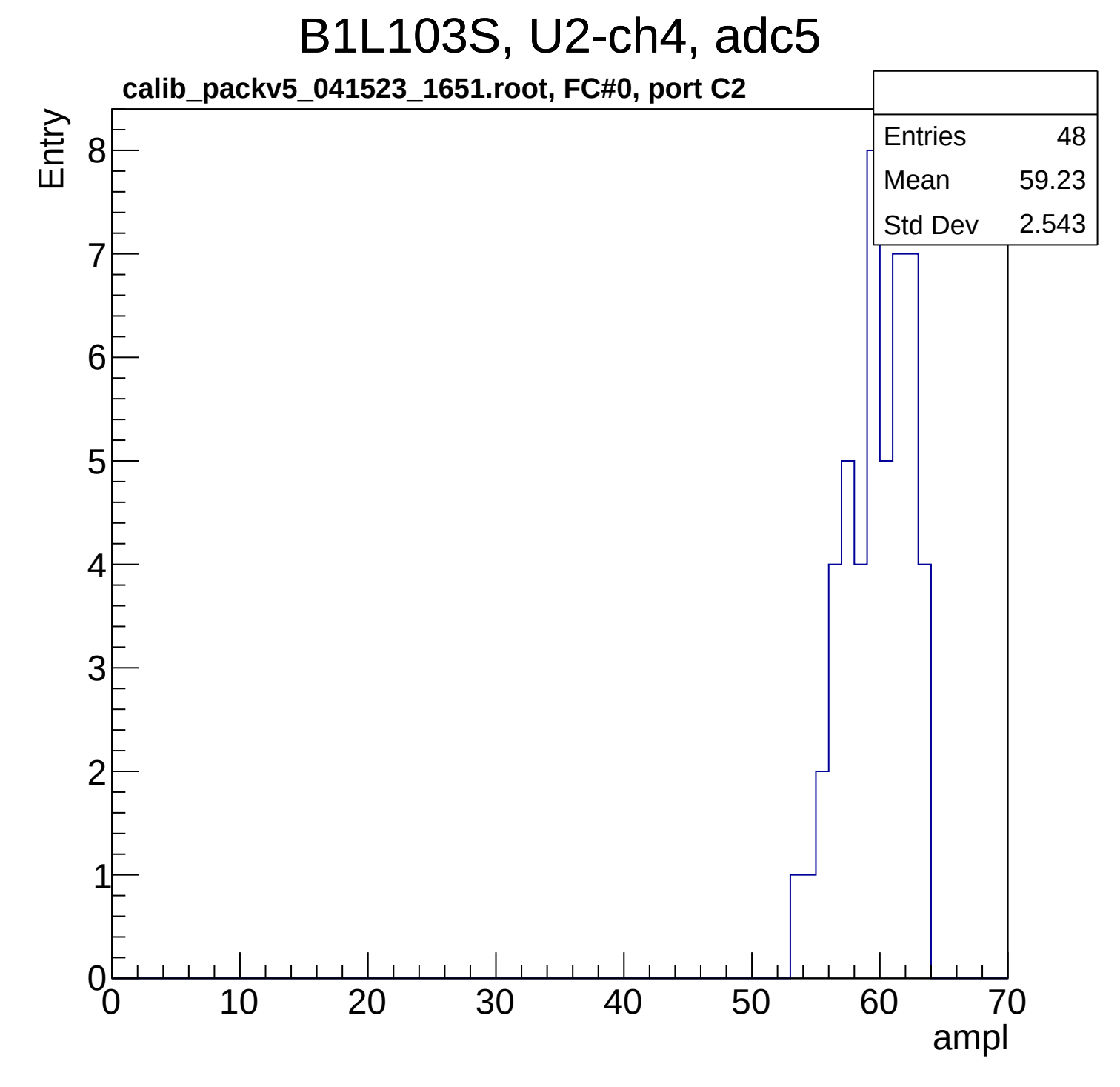

B1L103S, U2-ch4, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 24.19
Std Dev 11.47
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

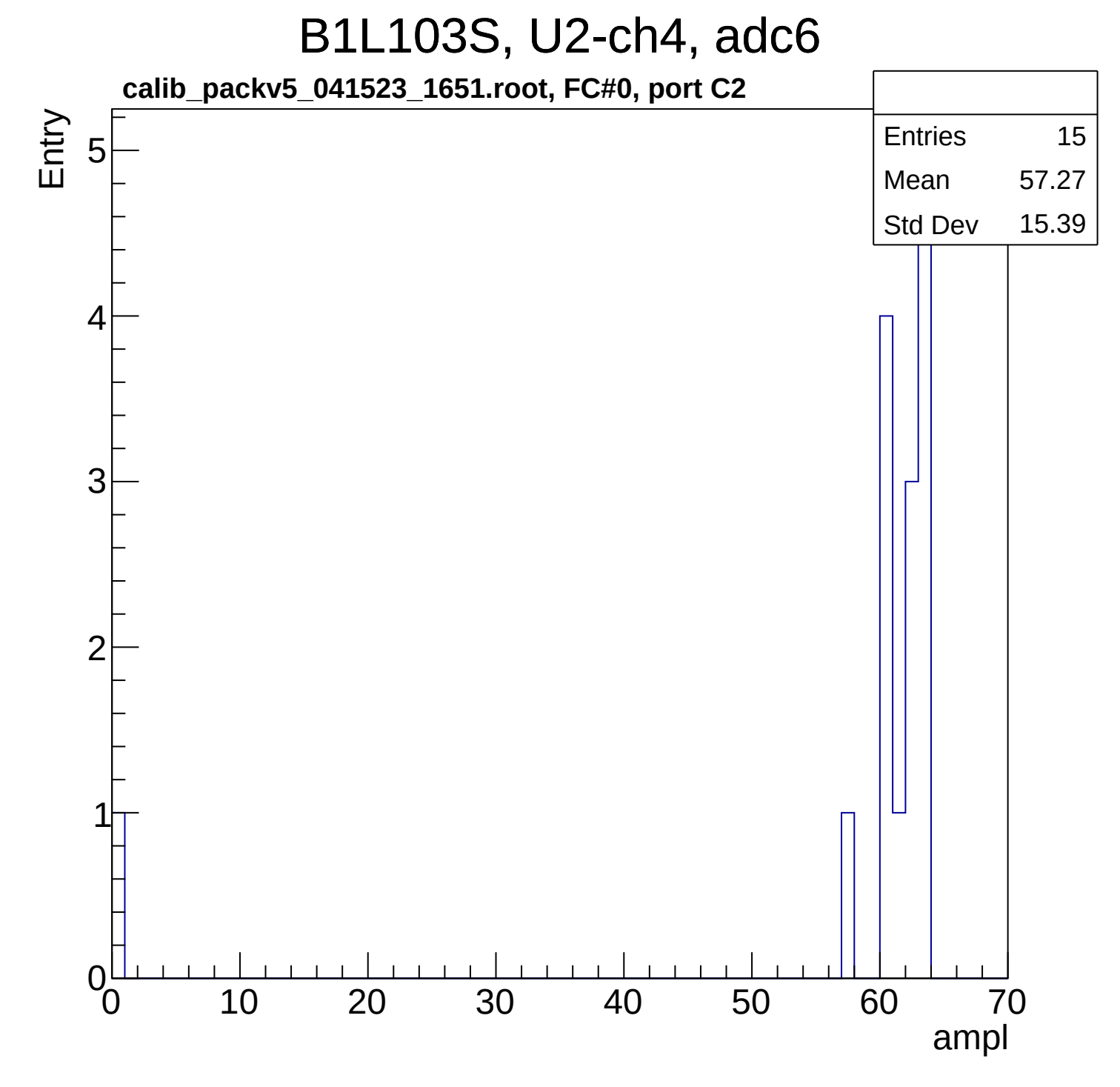

B1L103S, U2-ch4, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 32.15
Std Dev 10.49
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

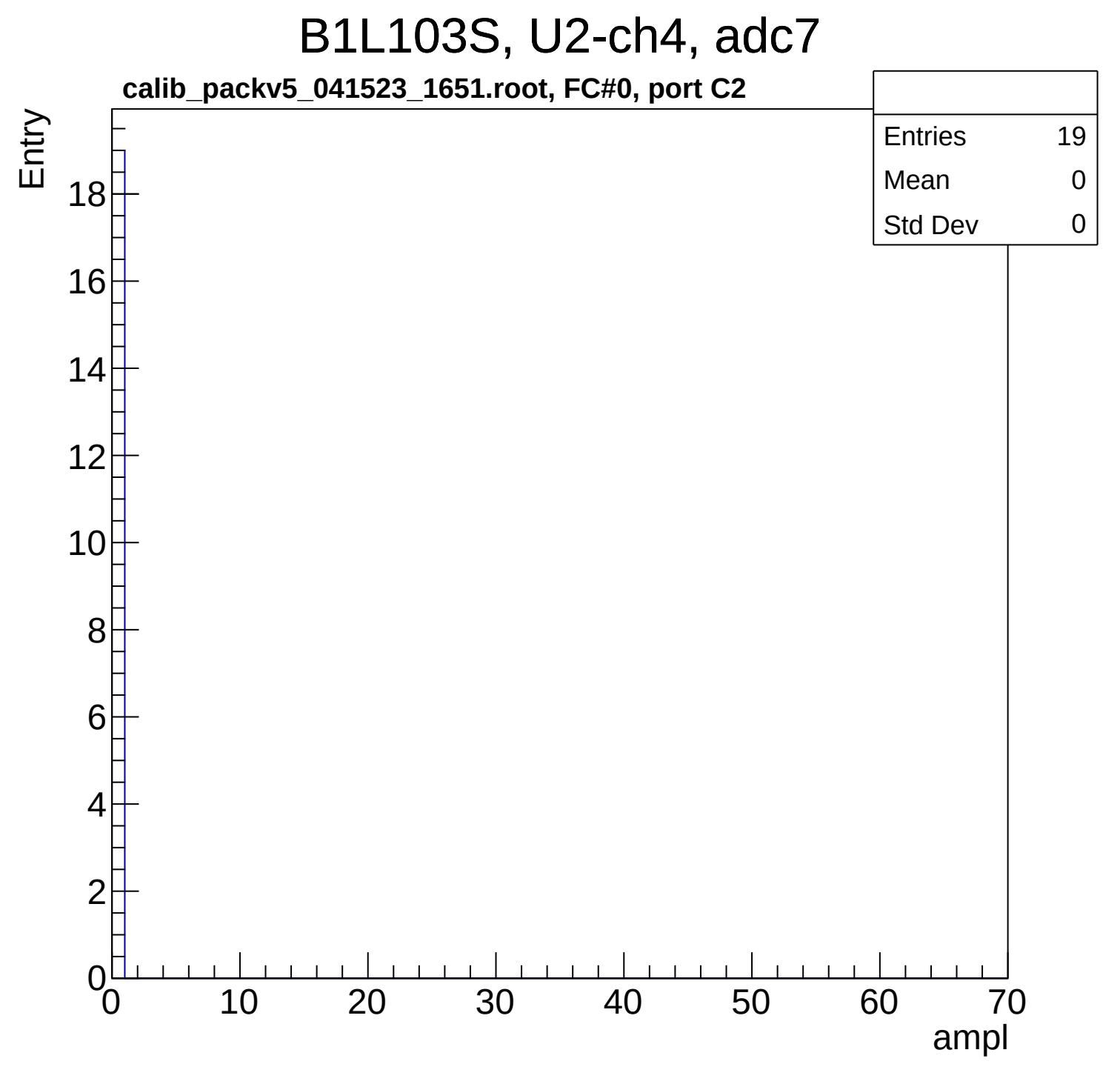

B1L103S, U2-ch4, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 35.33
Std Dev 15.32
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

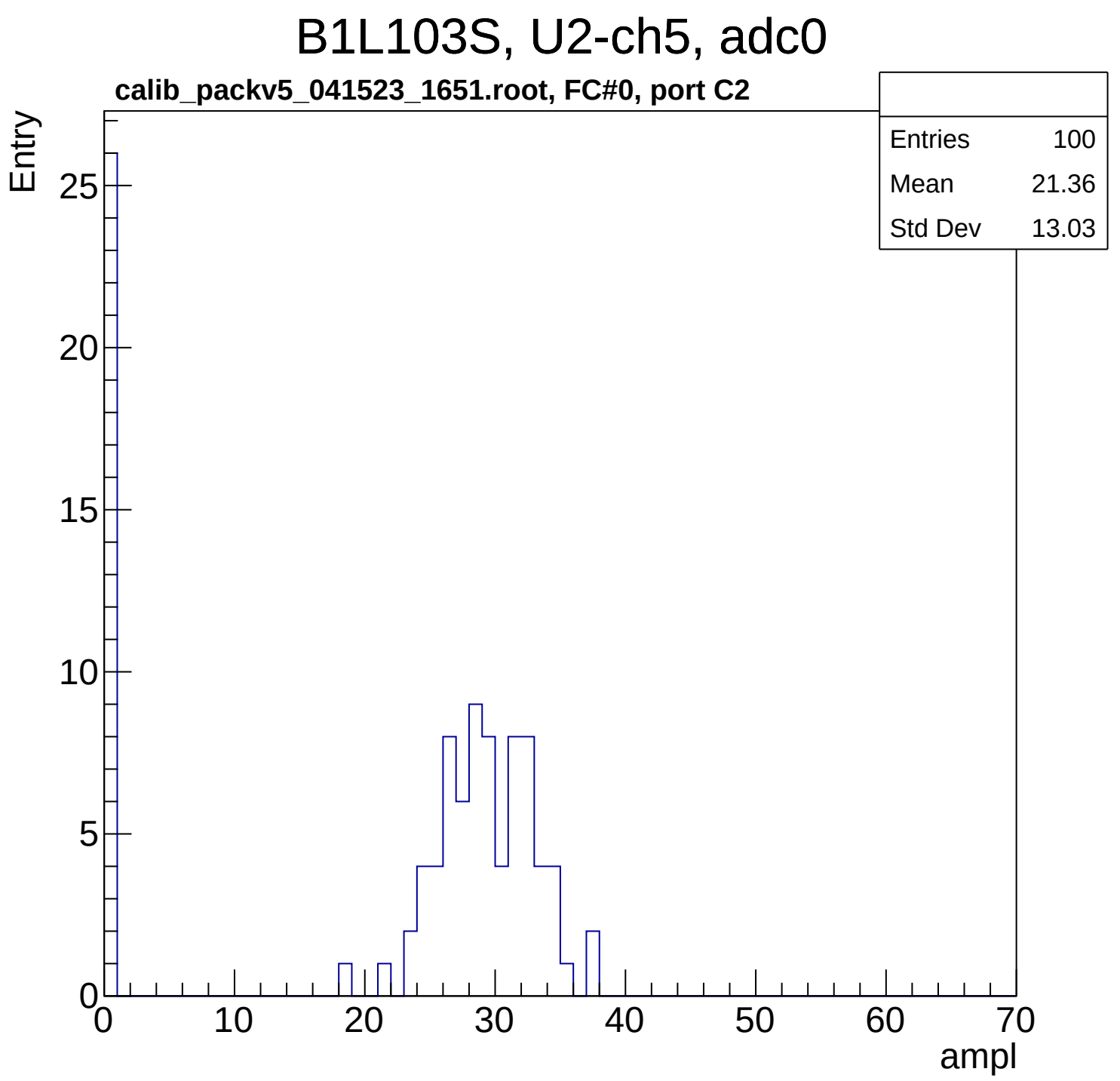

B1L103S, U2-ch4, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 44.63
Std Dev 12.2
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

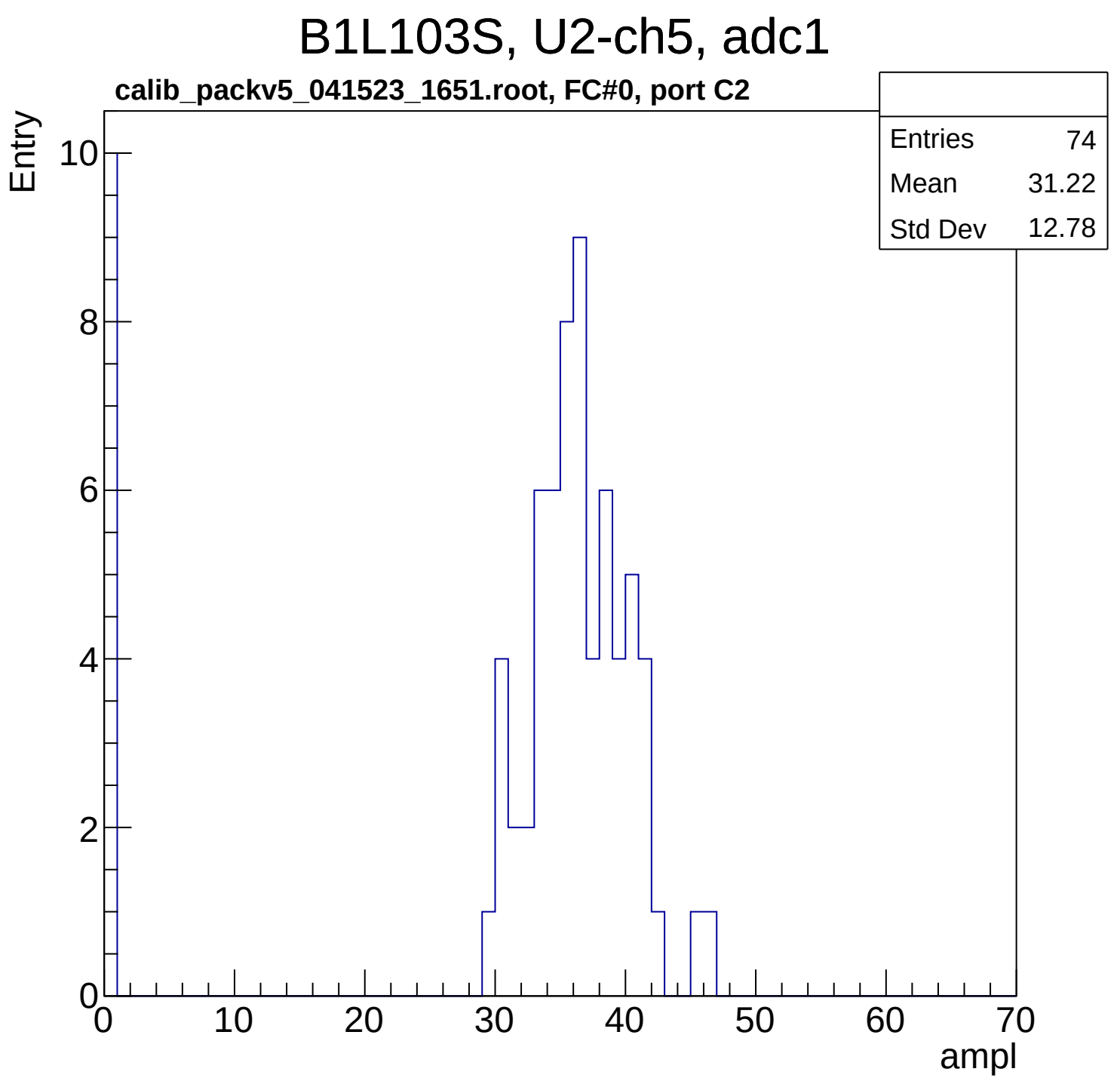

B1L103S, U2-ch4, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 53.7
Std Dev 3.605
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

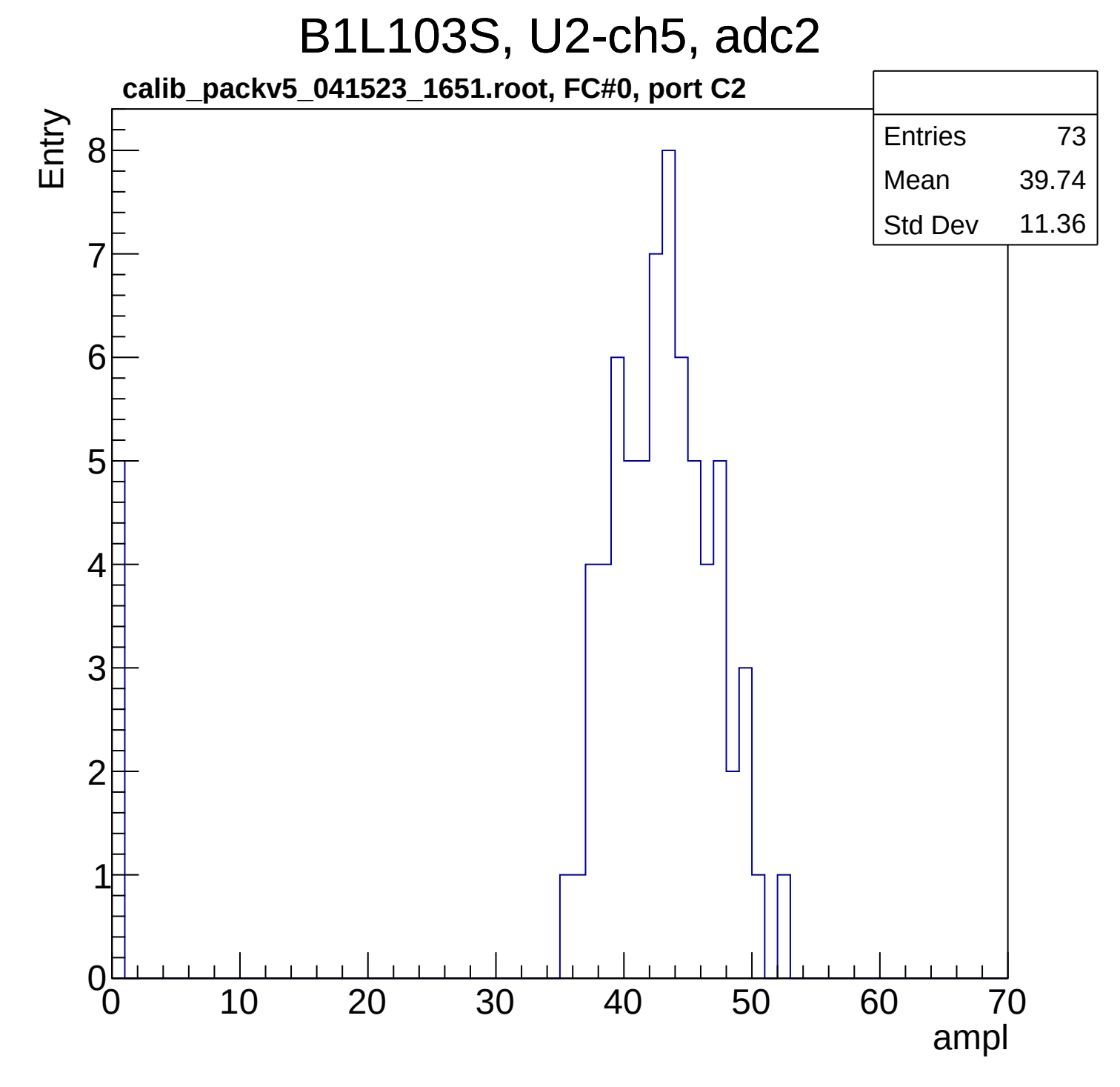

B1L103S, U2-ch4, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 59.23
Std Dev 2.543
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

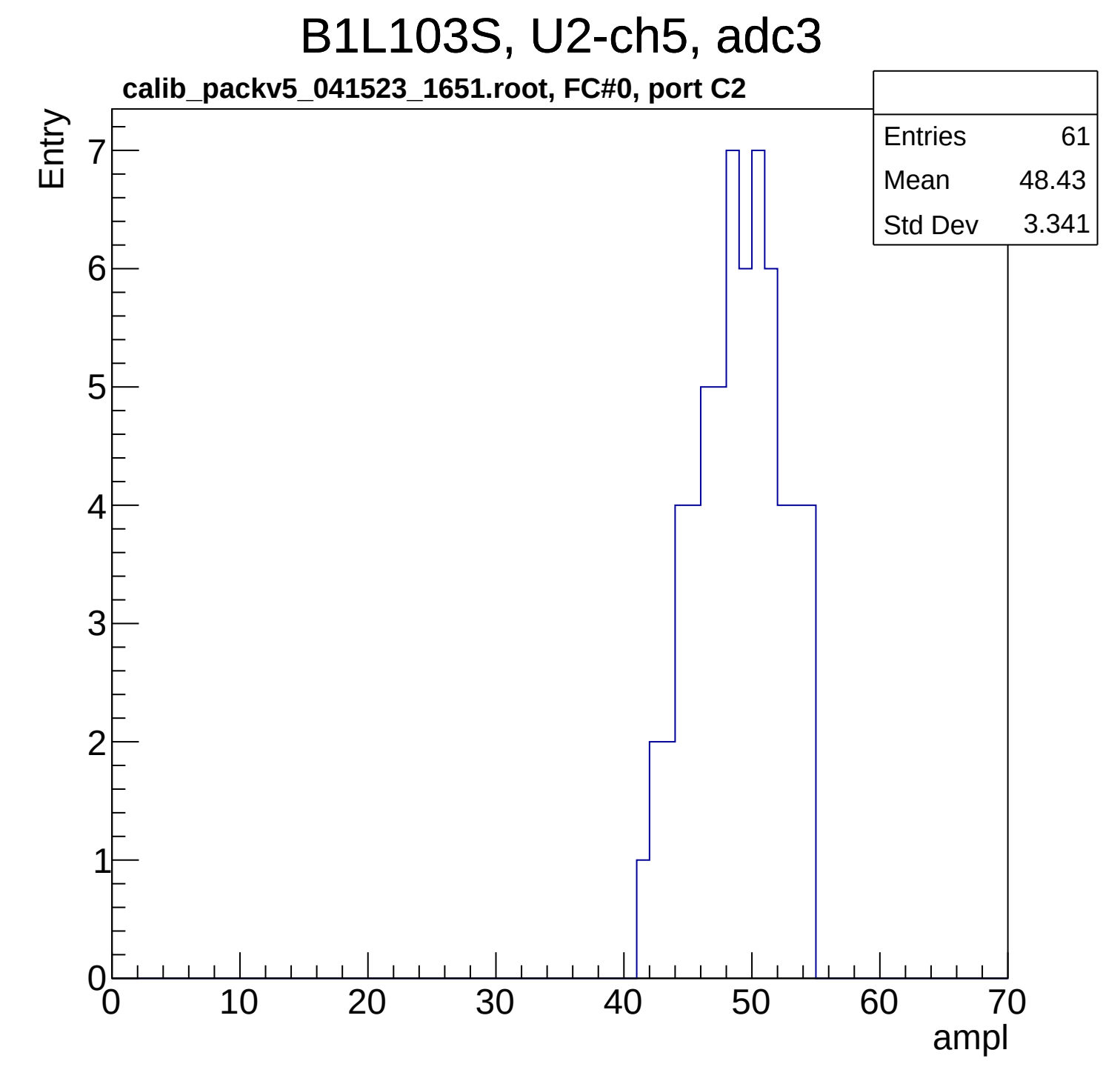

B1L103S, U2-ch4, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.27
Std Dev 15.39
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

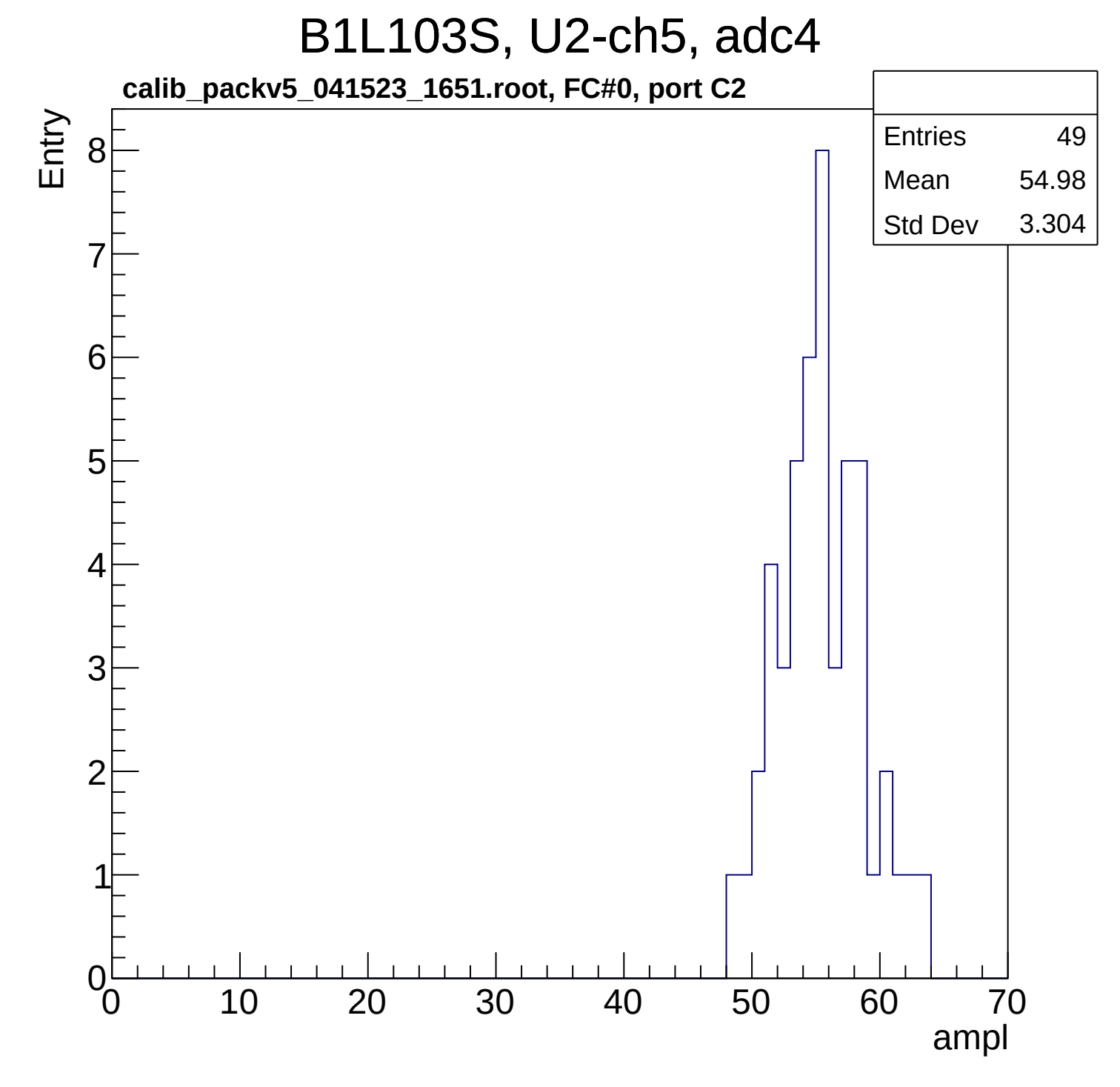

B1L103S, U2-ch4, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

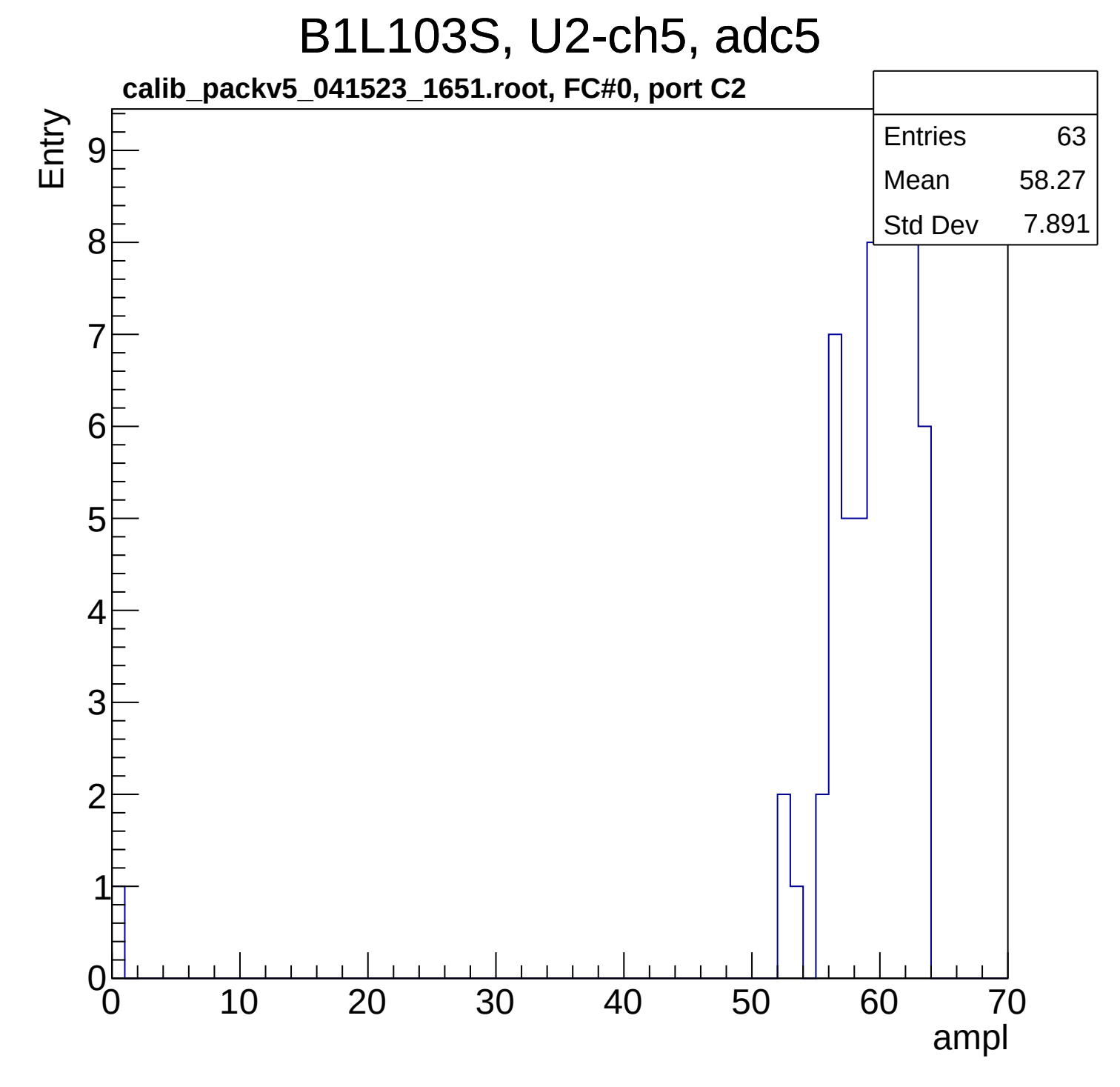

B1L103S, U2-ch5, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 21.36
Std Dev 13.03
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl

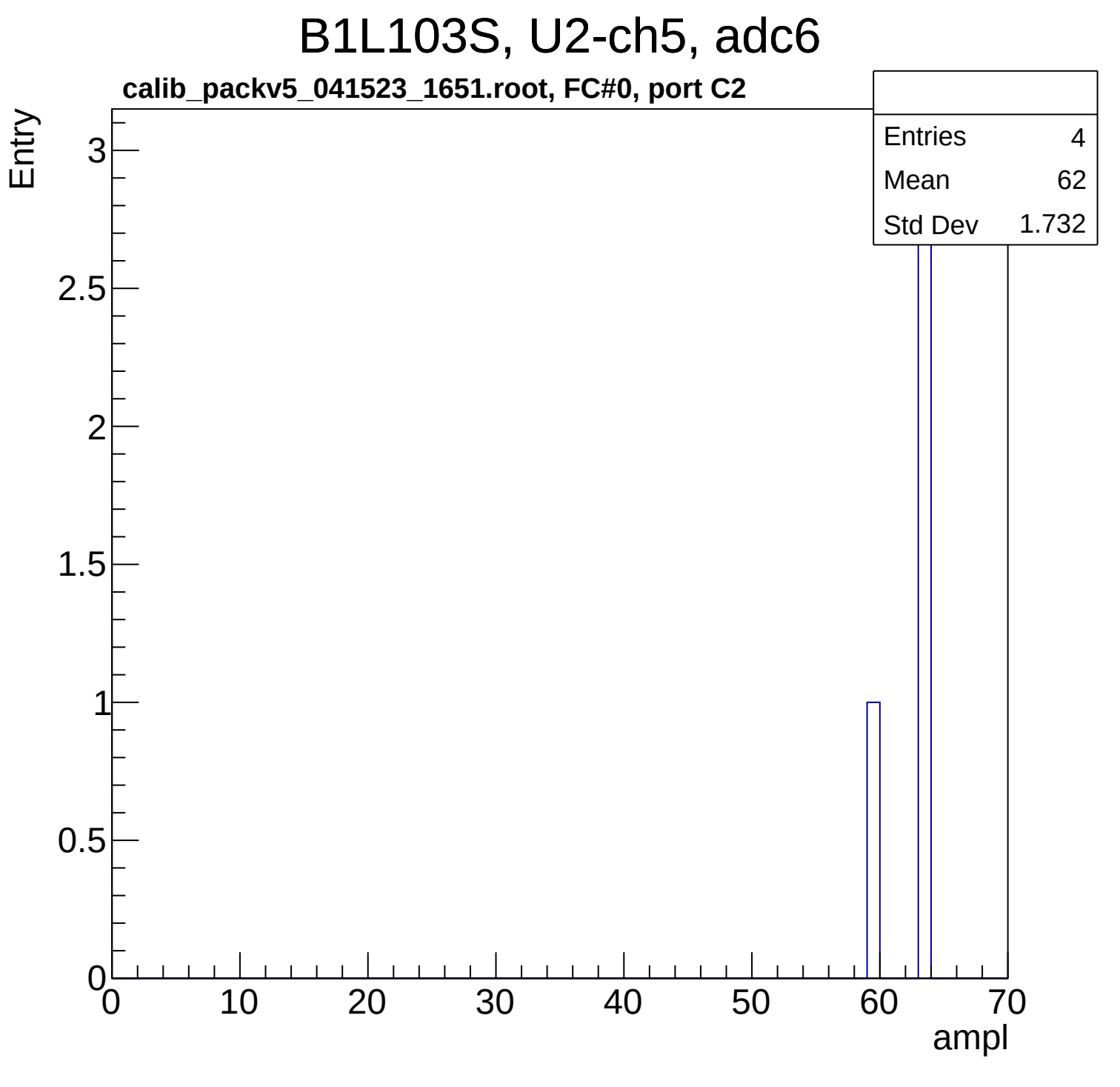

B1L103S, U2-ch5, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 31.22
Std Dev 12.78
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

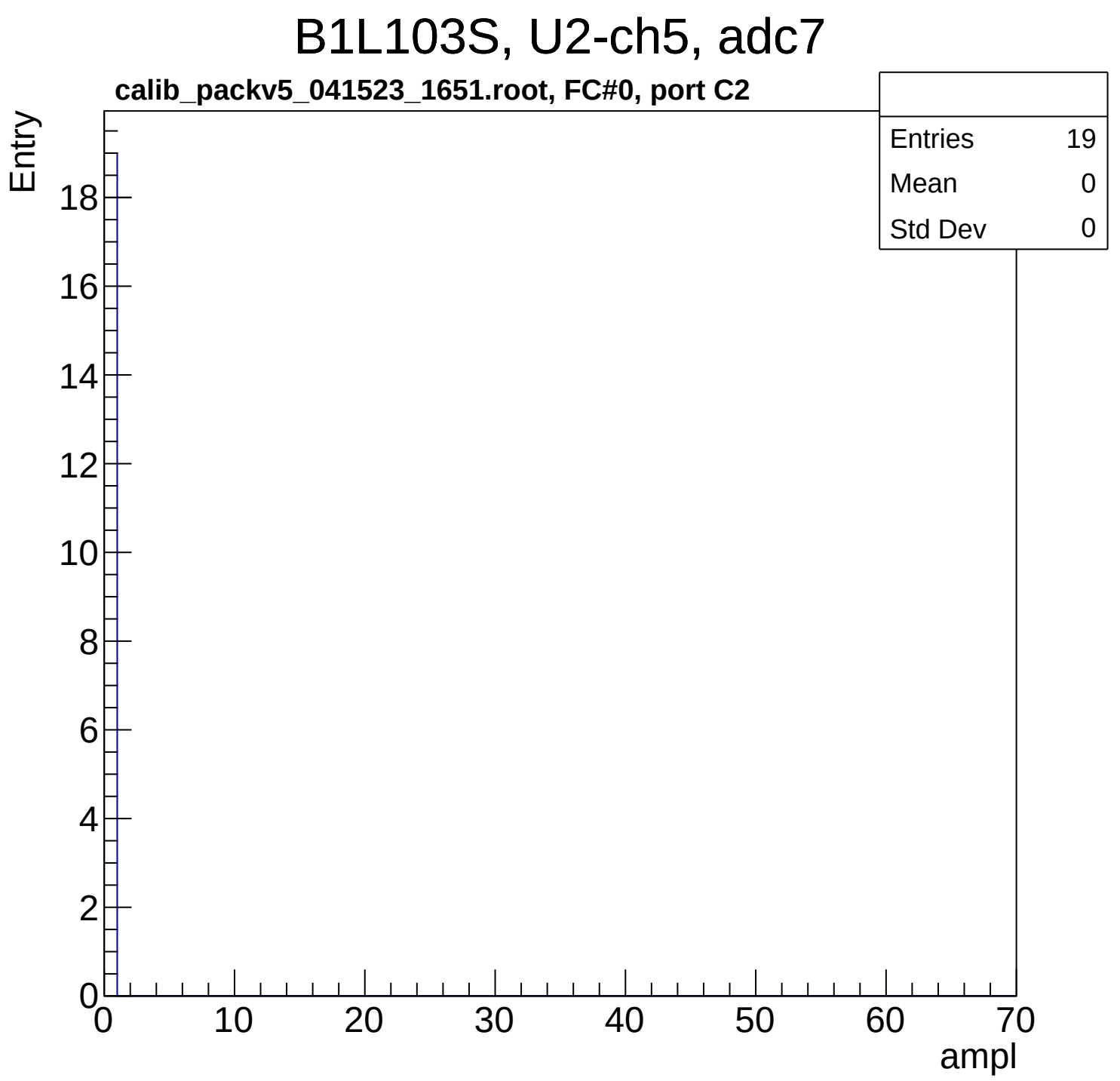

B1L103S, U2-ch5, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 39.74
Std Dev 11.36
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

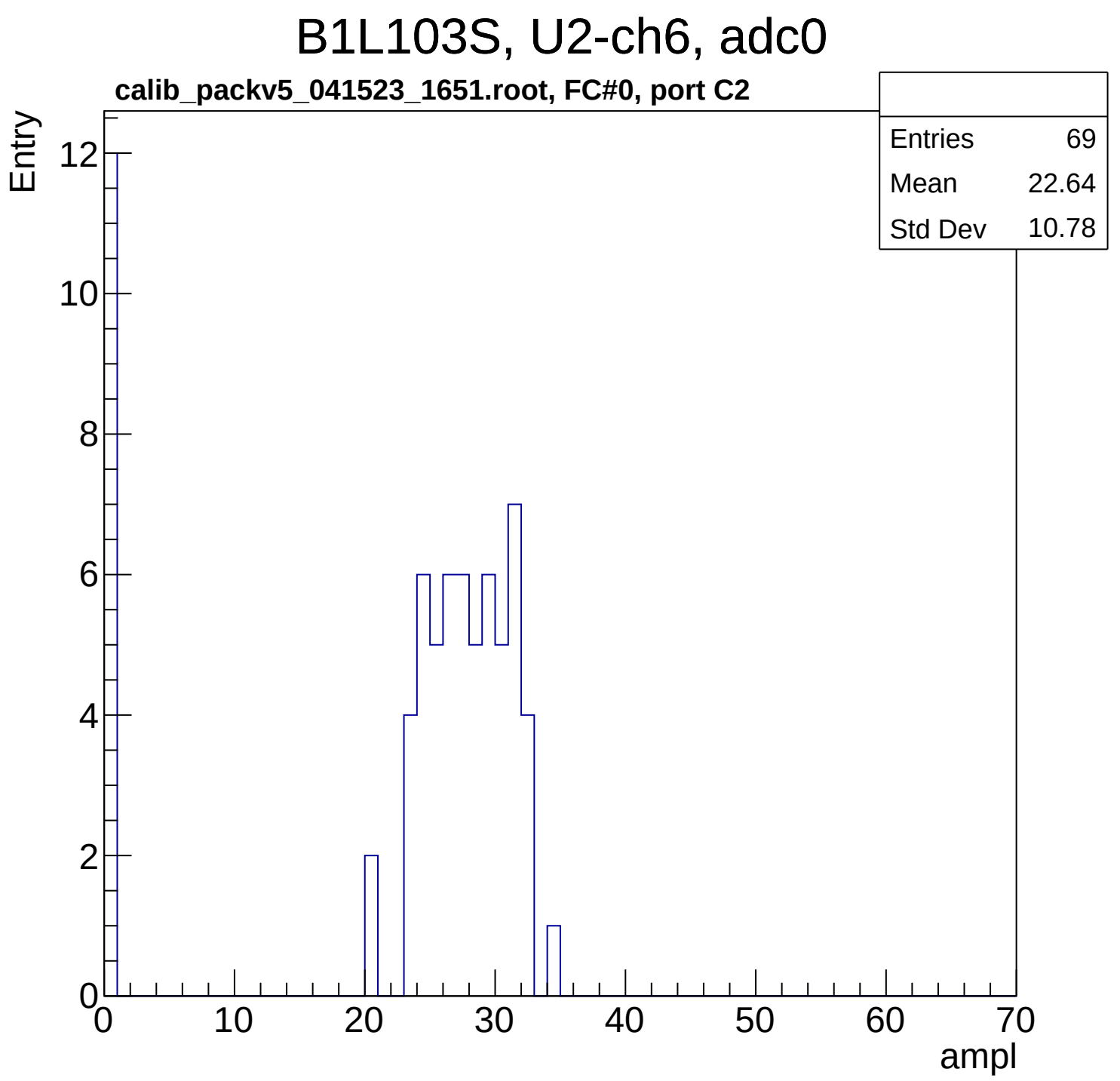

B1L103S, U2-ch5, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 48.43
Std Dev 3.341
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

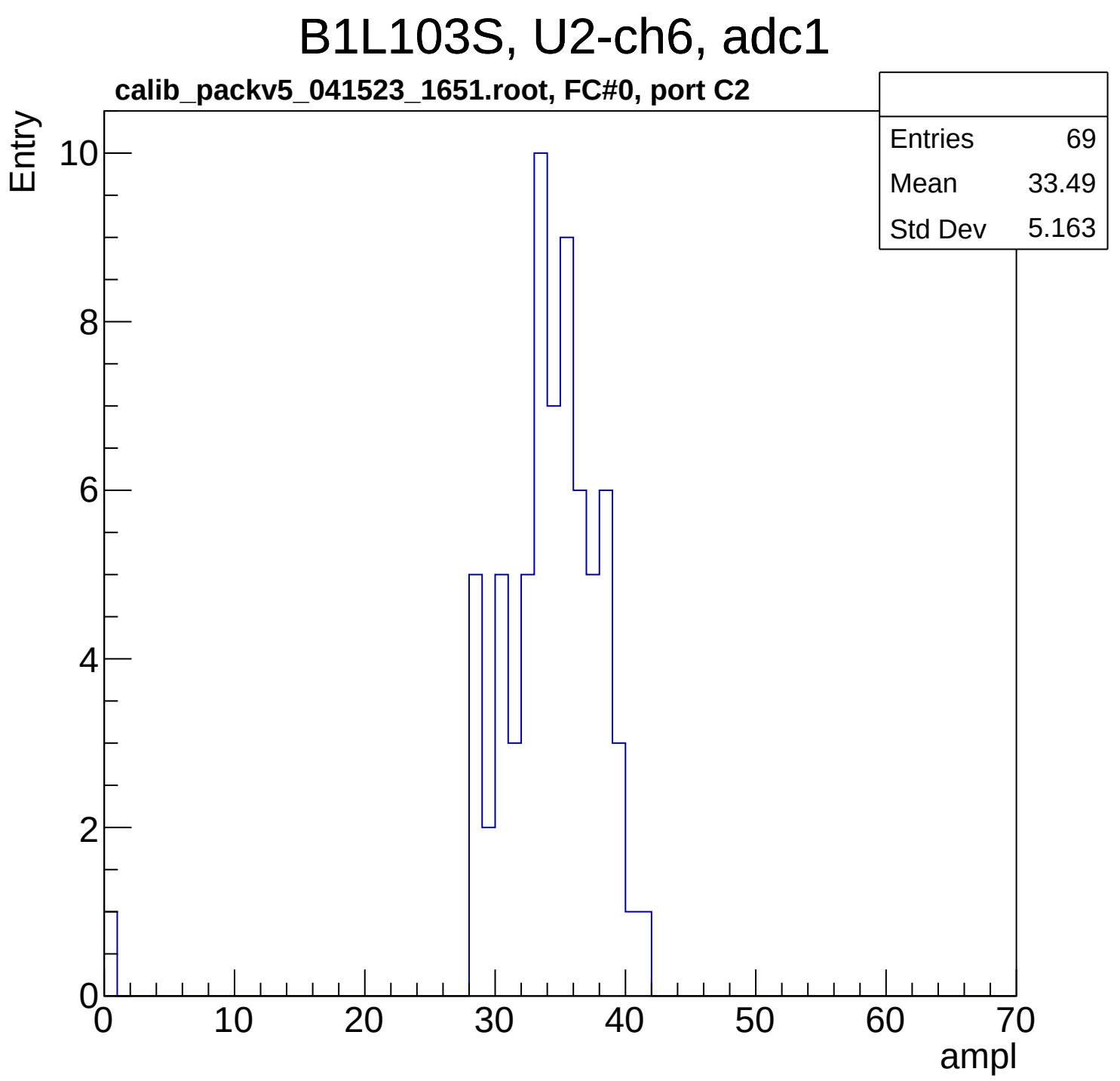

B1L103S, U2-ch5, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 54.98
Std Dev 3.304
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

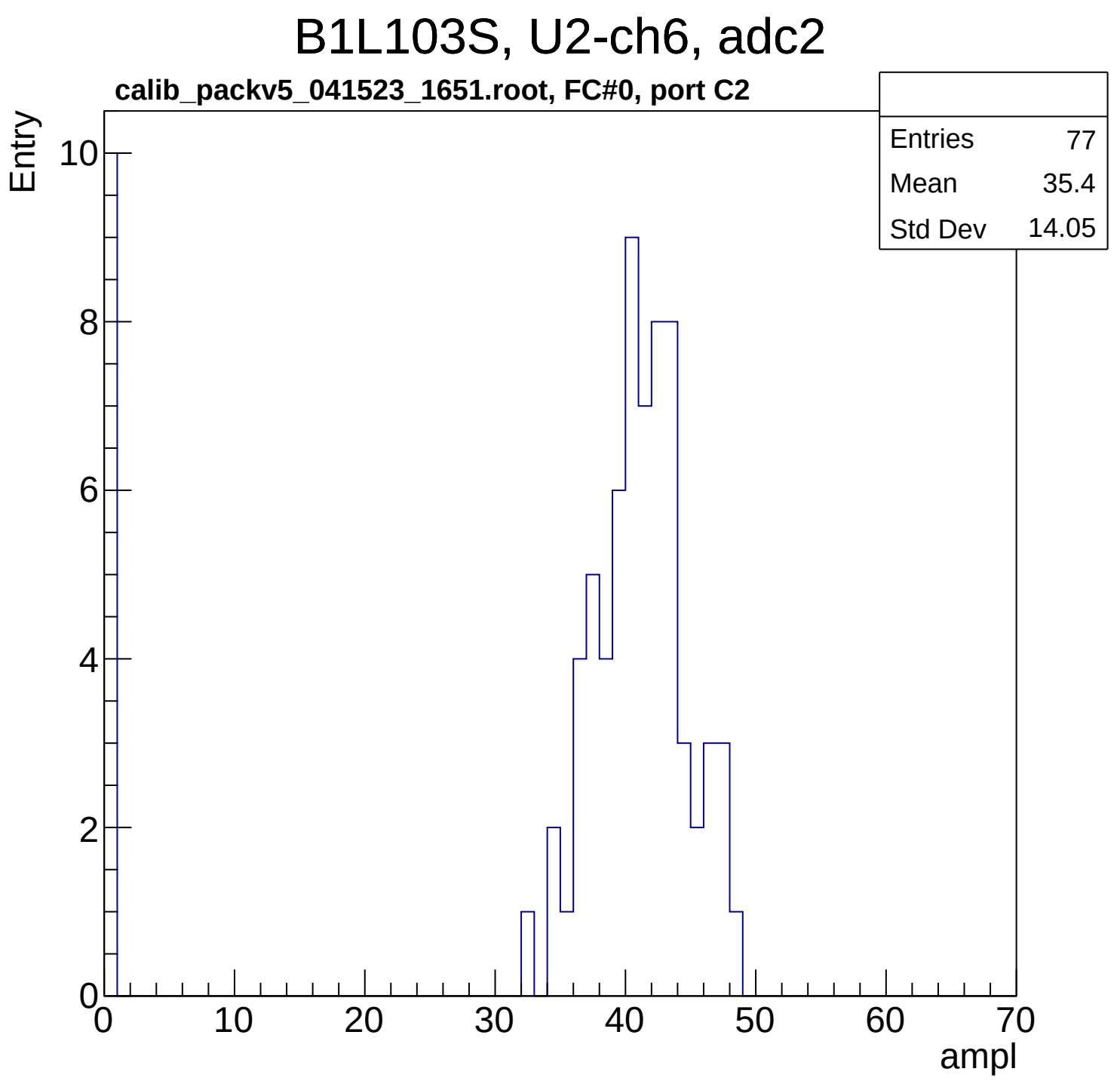

B1L103S, U2-ch5, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 58.27
Std Dev 7.891
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

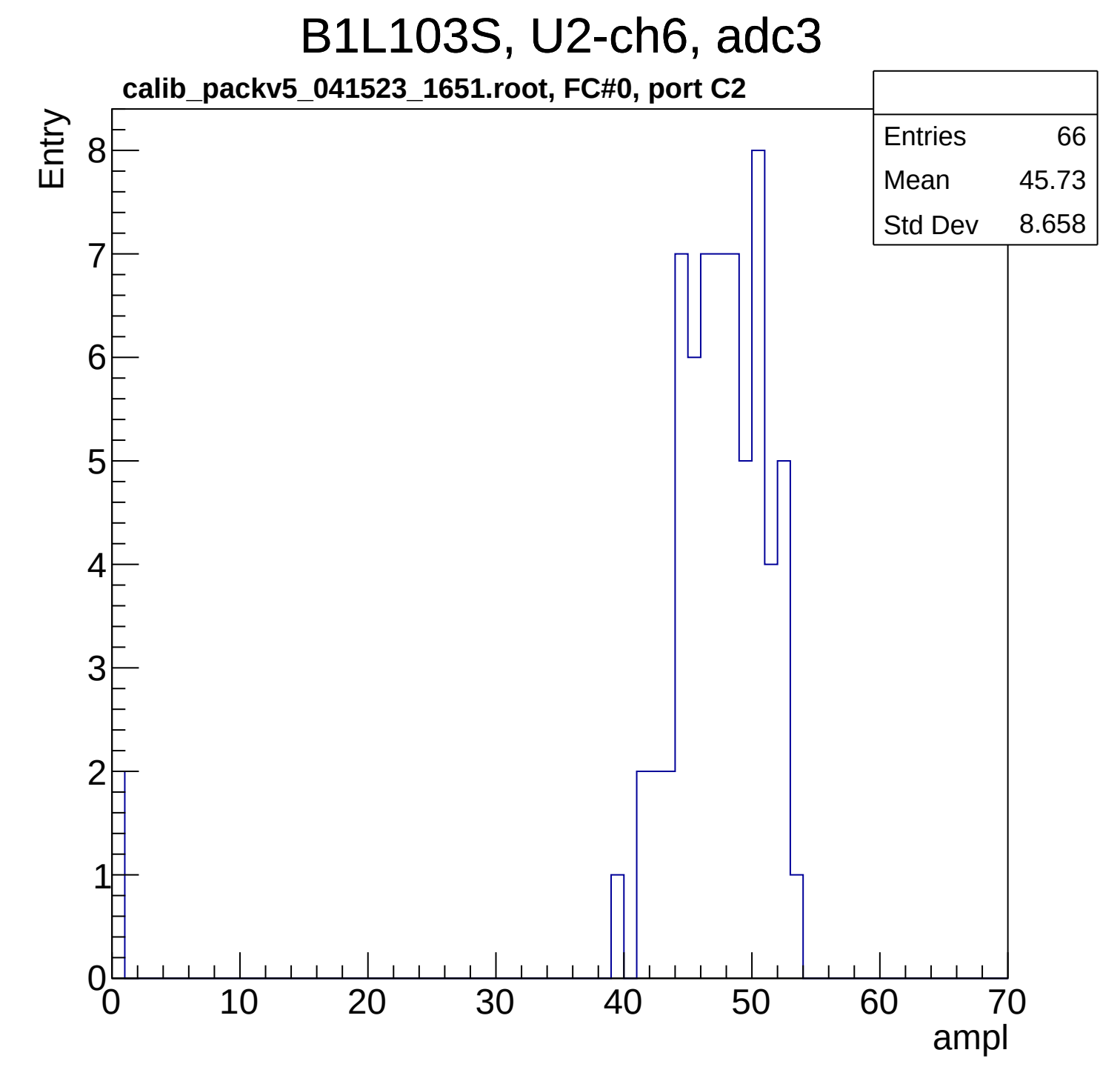

B1L103S, U2-ch5, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62
Std Dev 1.732
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

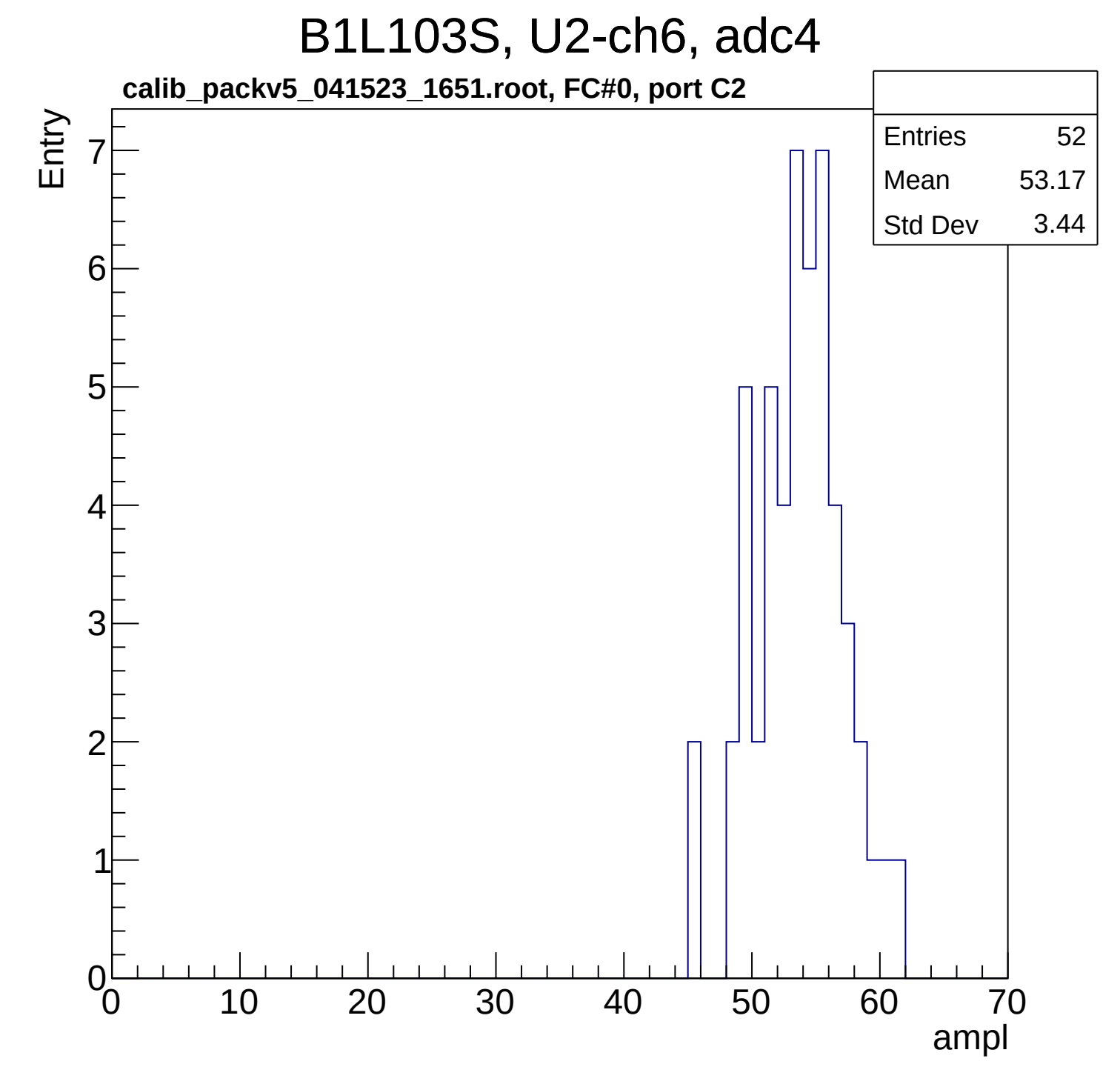

B1L103S, U2-ch5, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

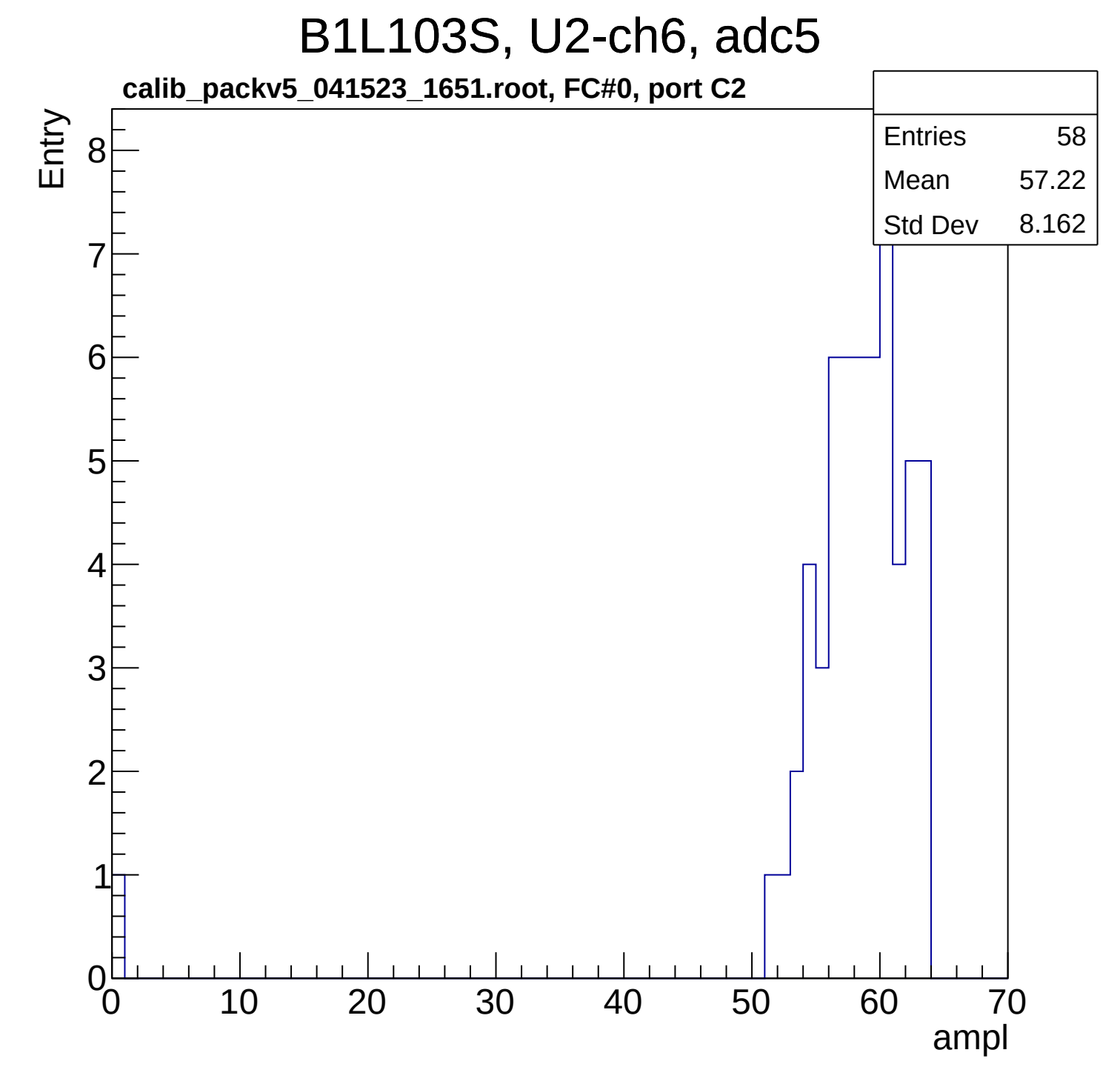

B1L103S, U2-ch6, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 22.64
Std Dev 10.78
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

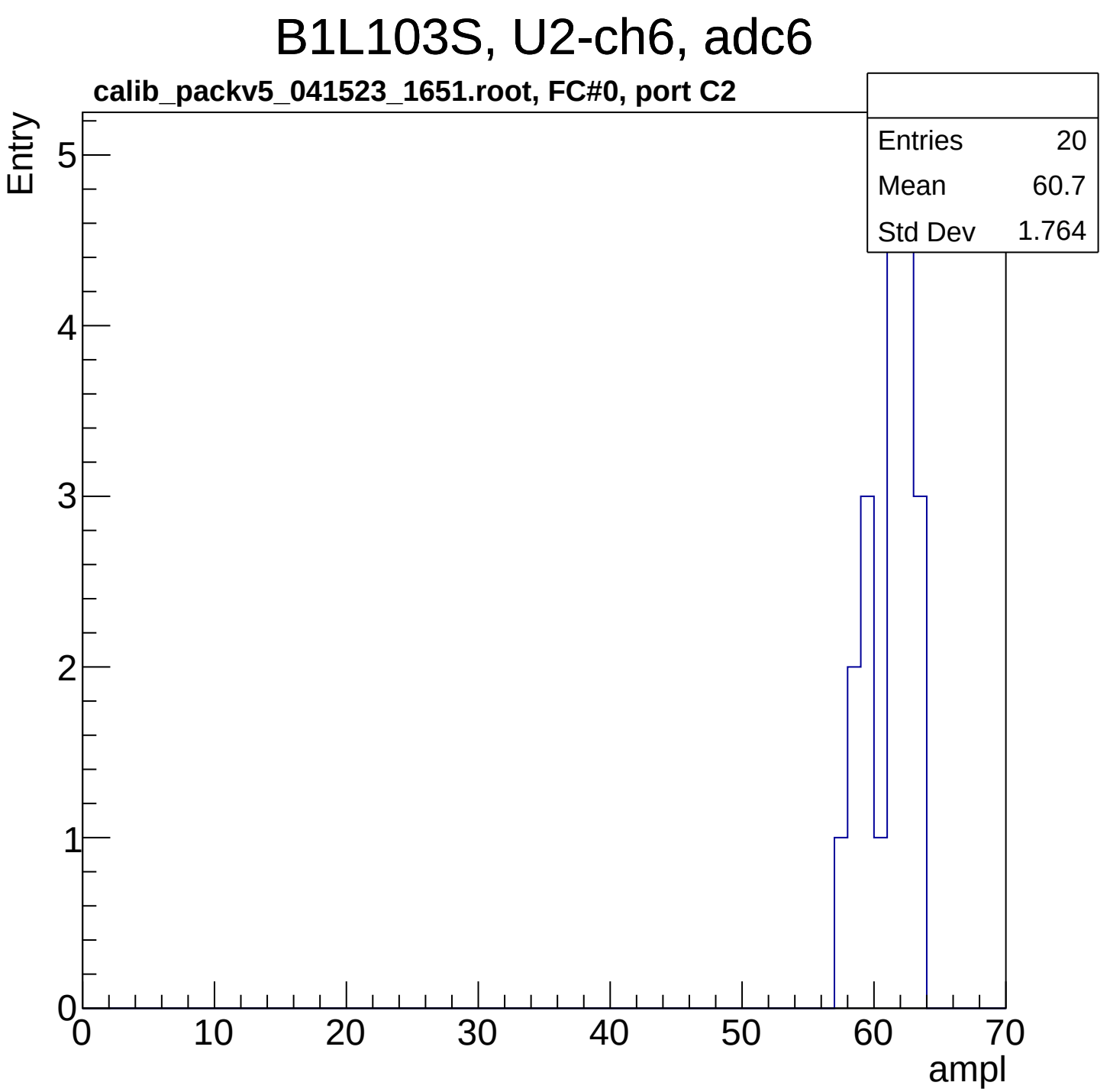

B1L103S, U2-ch6, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 33.49
Std Dev 5.163
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

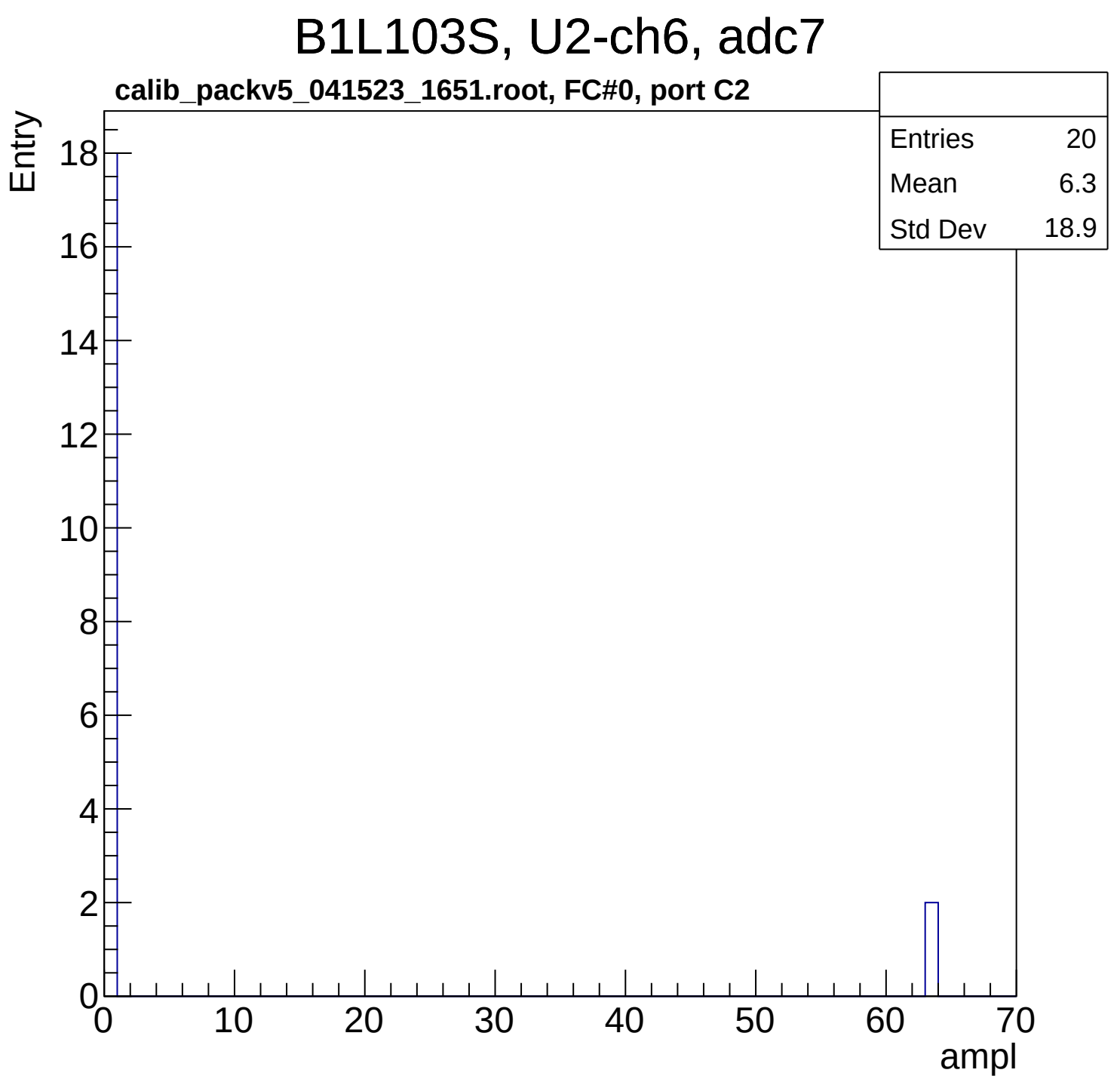

B1L103S, U2-ch6, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 35.4
Std Dev 14.05
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

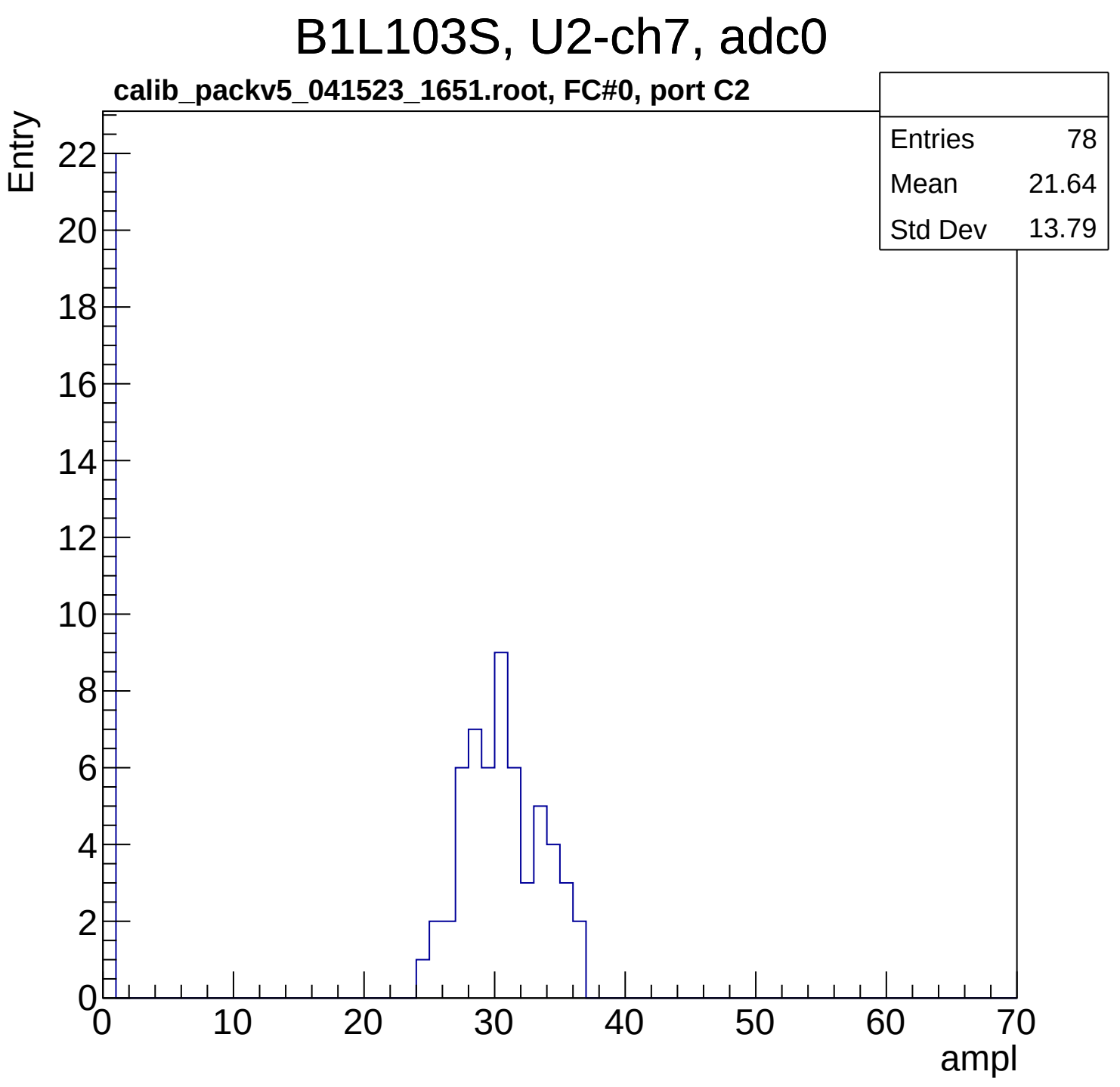

B1L103S, U2-ch6, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 45.73
Std Dev 8.658
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

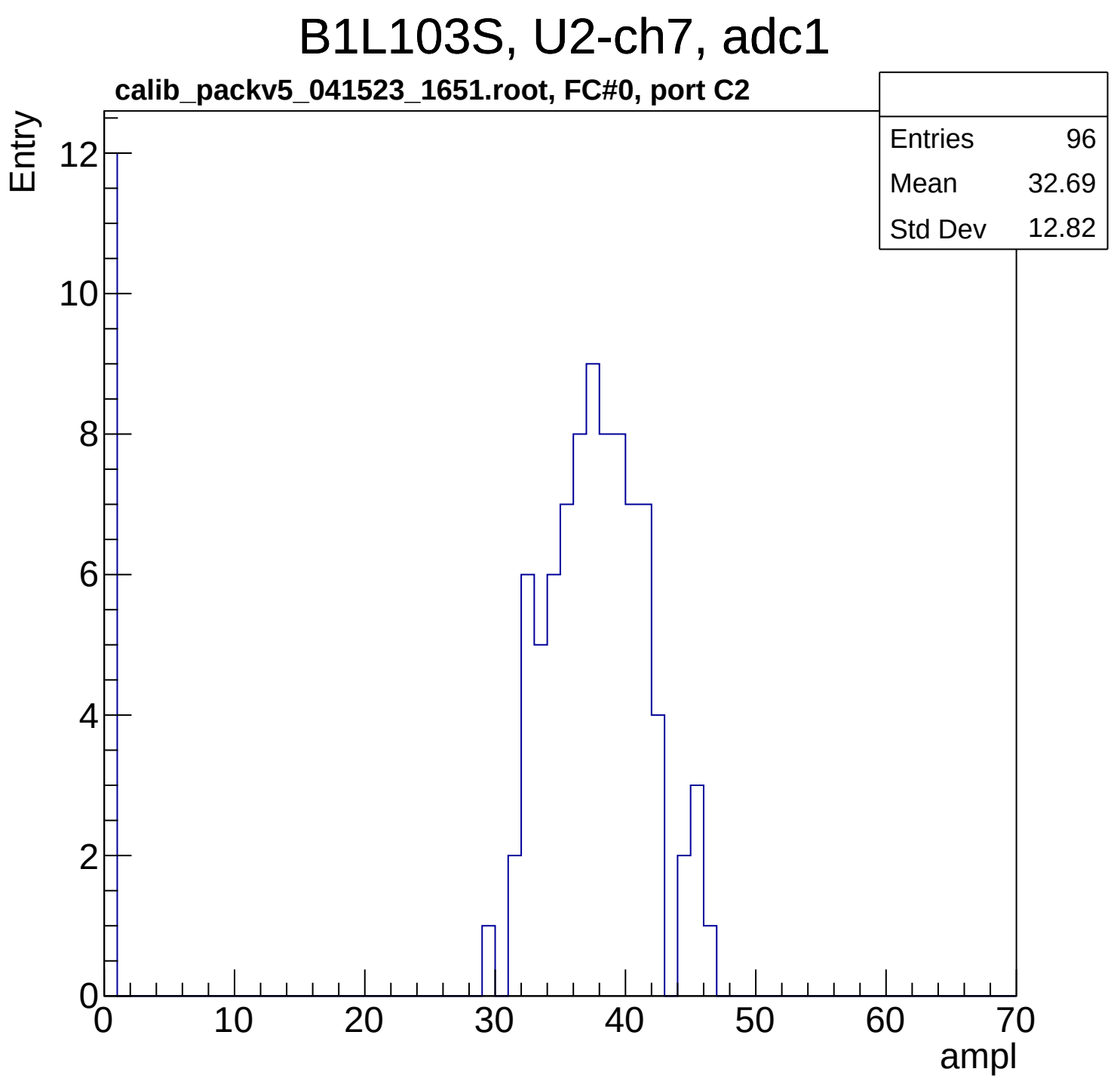

B1L103S, U2-ch6, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 53.17
Std Dev 3.44
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

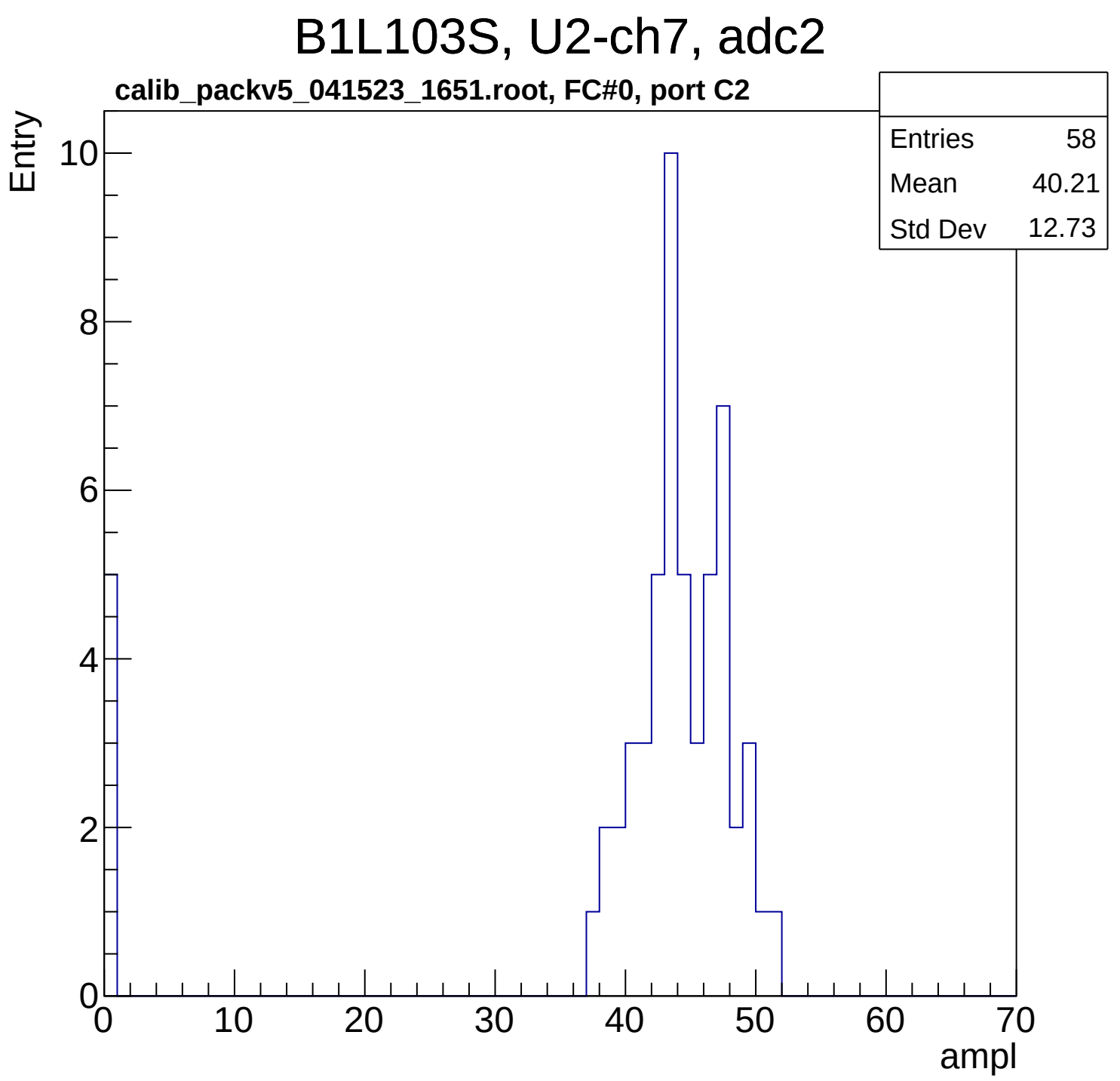

B1L103S, U2-ch6, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 57.22
Std Dev 8.162
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

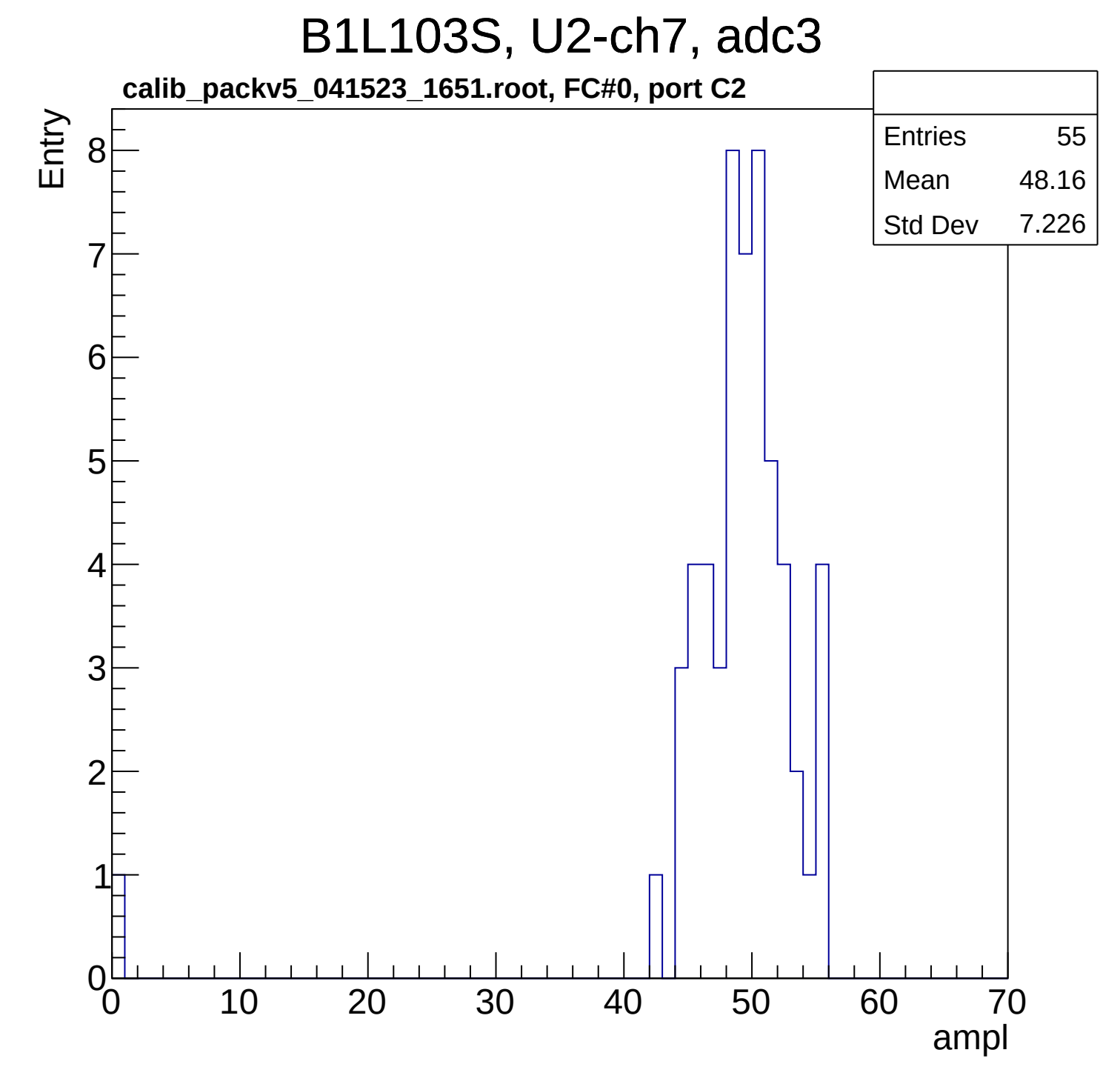

B1L103S, U2-ch6, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 60.7
Std Dev 1.764
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

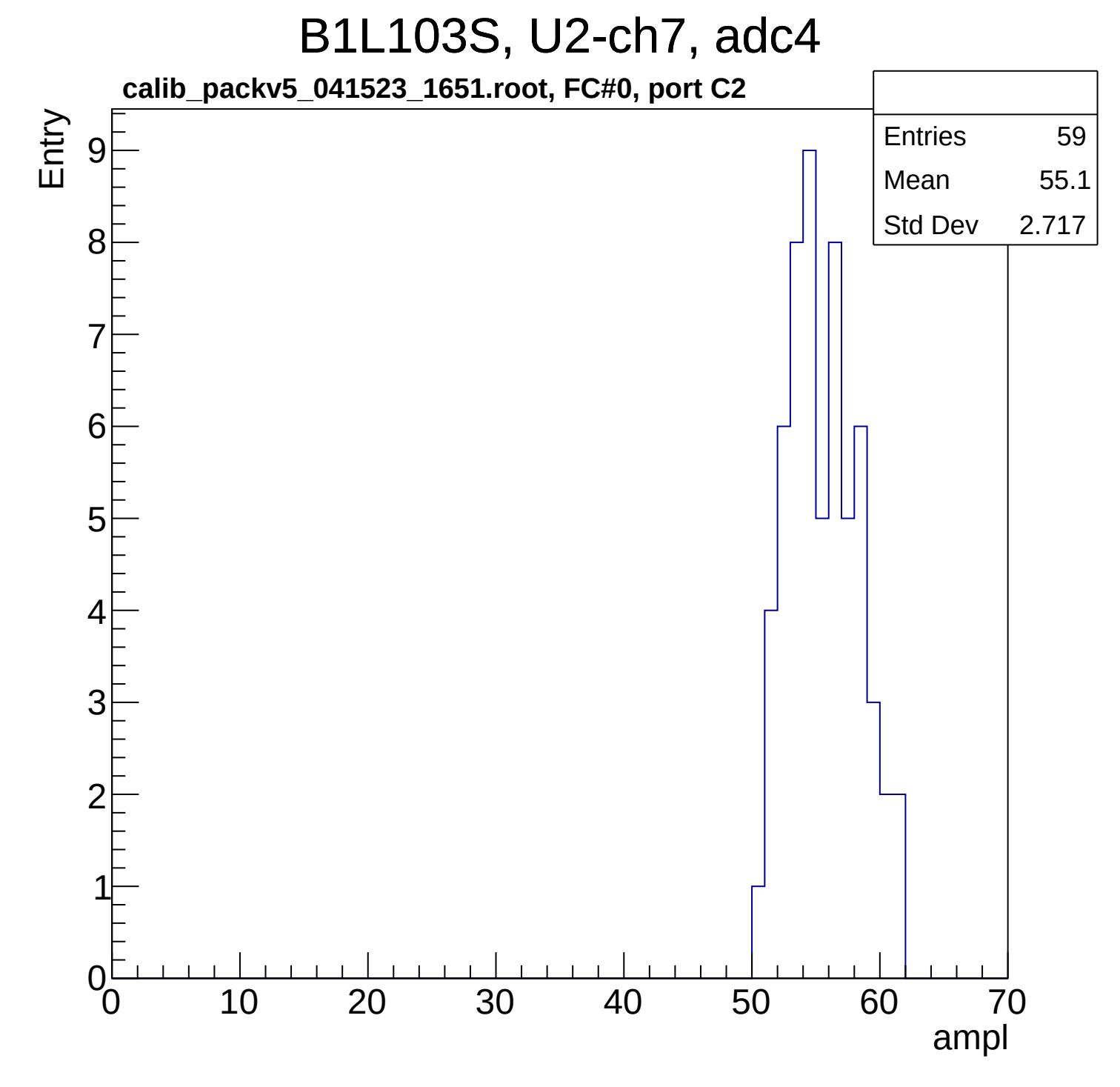

B1L103S, U2-ch6, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.3
Std Dev 18.9
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

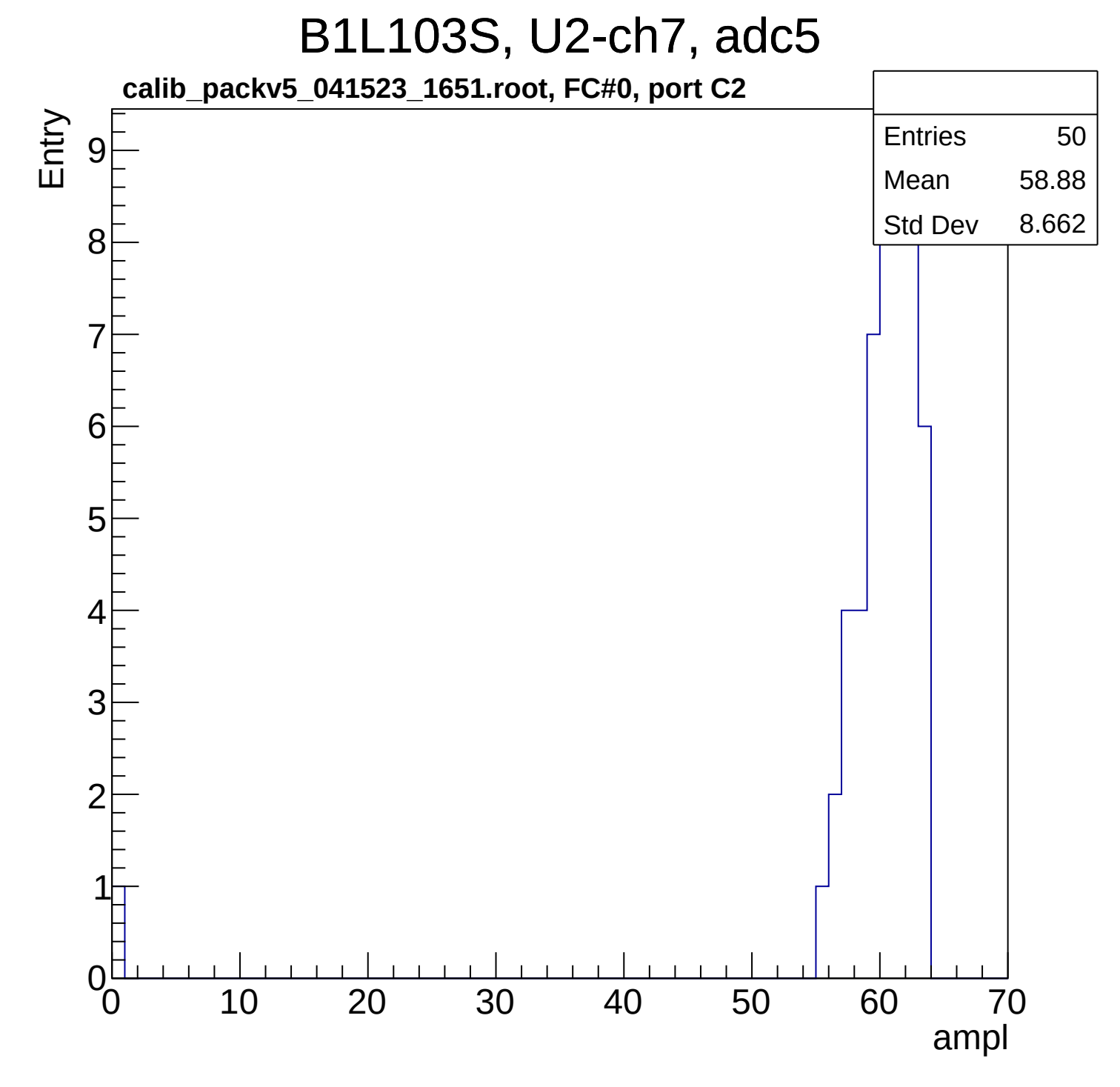

B1L103S, U2-ch7, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 21.64
Std Dev 13.79
Entry
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70
ampl

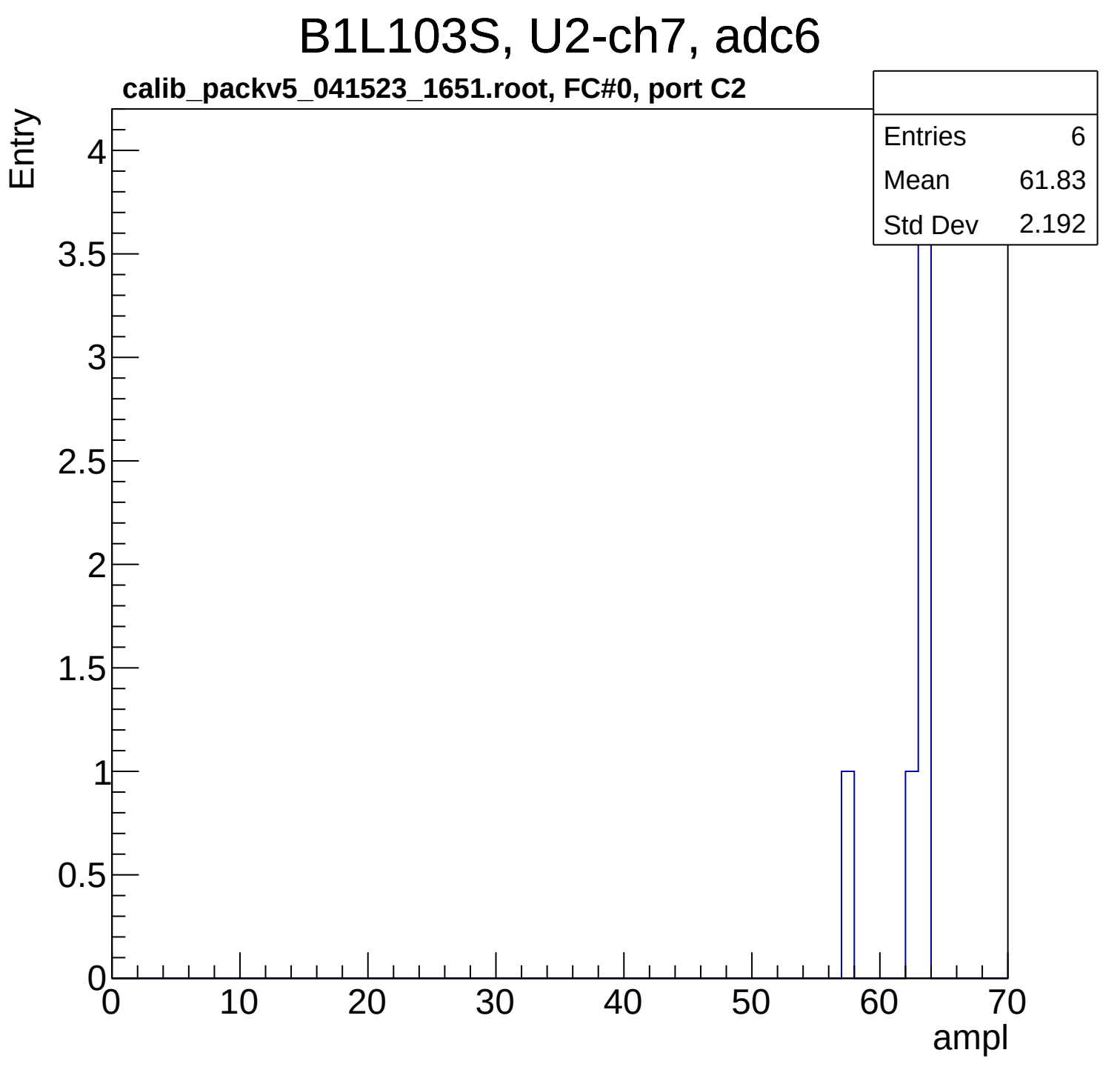

B1L103S, U2-ch7, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 32.69
Std Dev 12.82
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

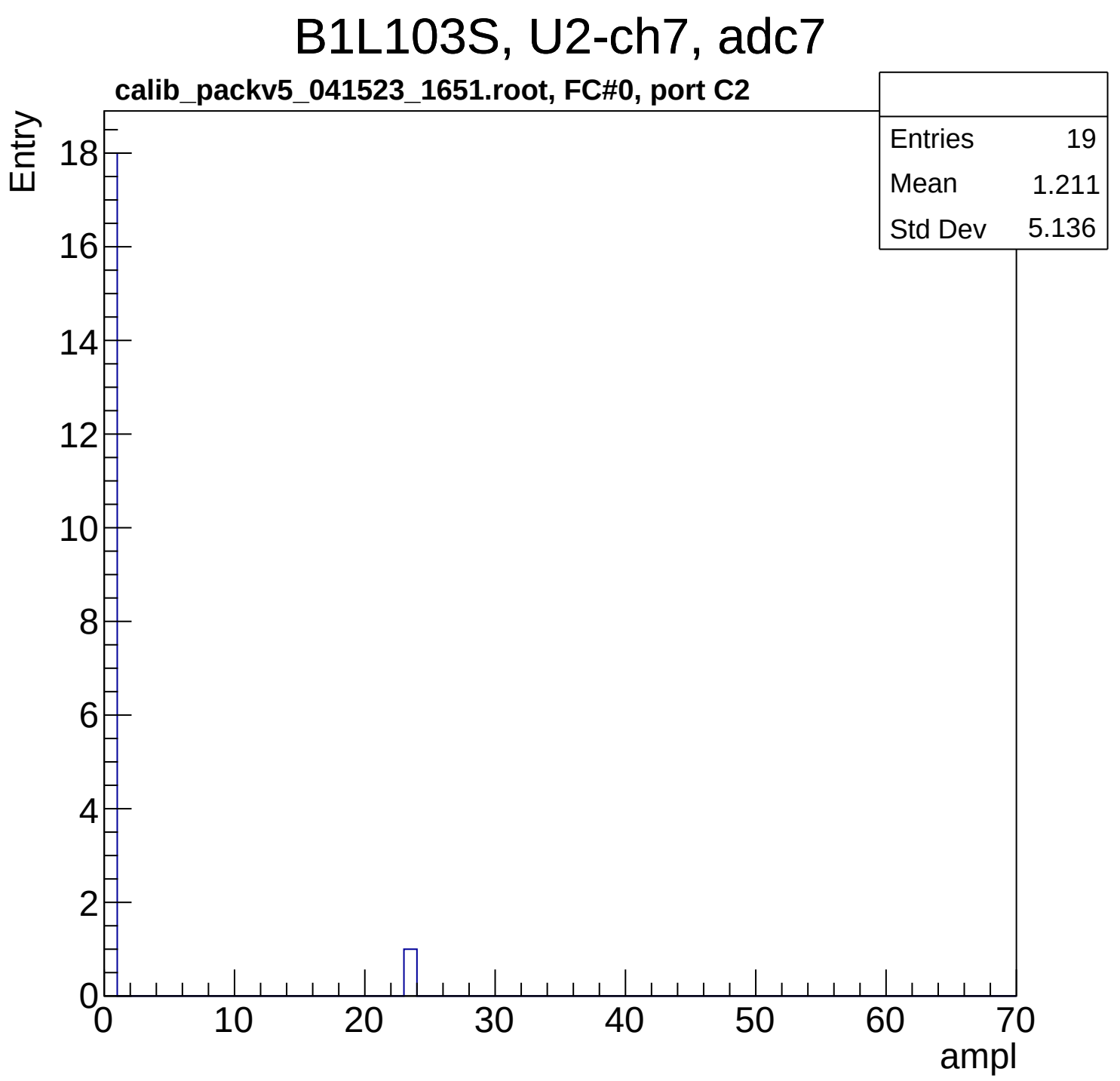

B1L103S, U2-ch7, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 40.21
Std Dev 12.73
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

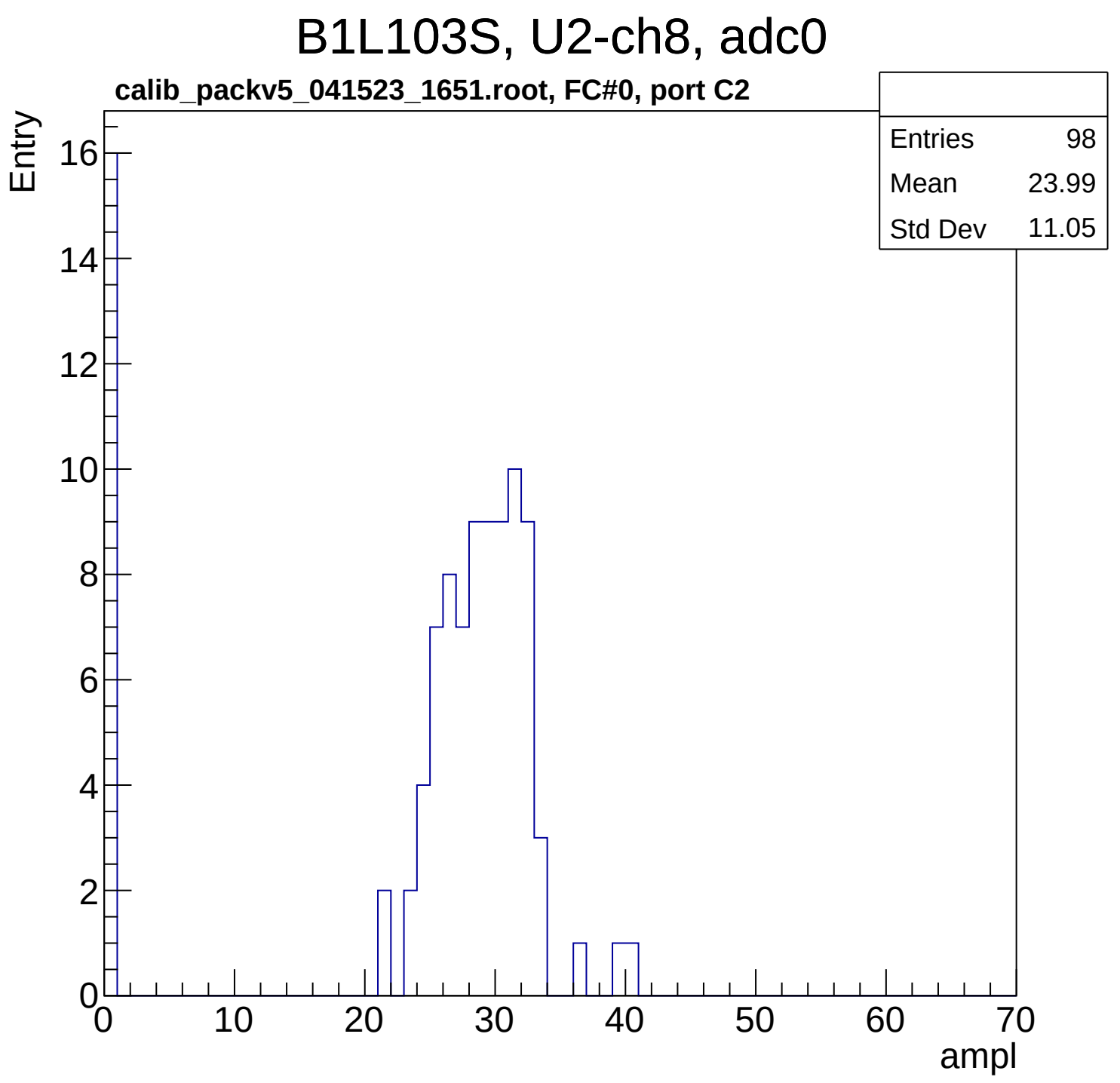

B1L103S, U2-ch7, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 48.16
Std Dev 7.226
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

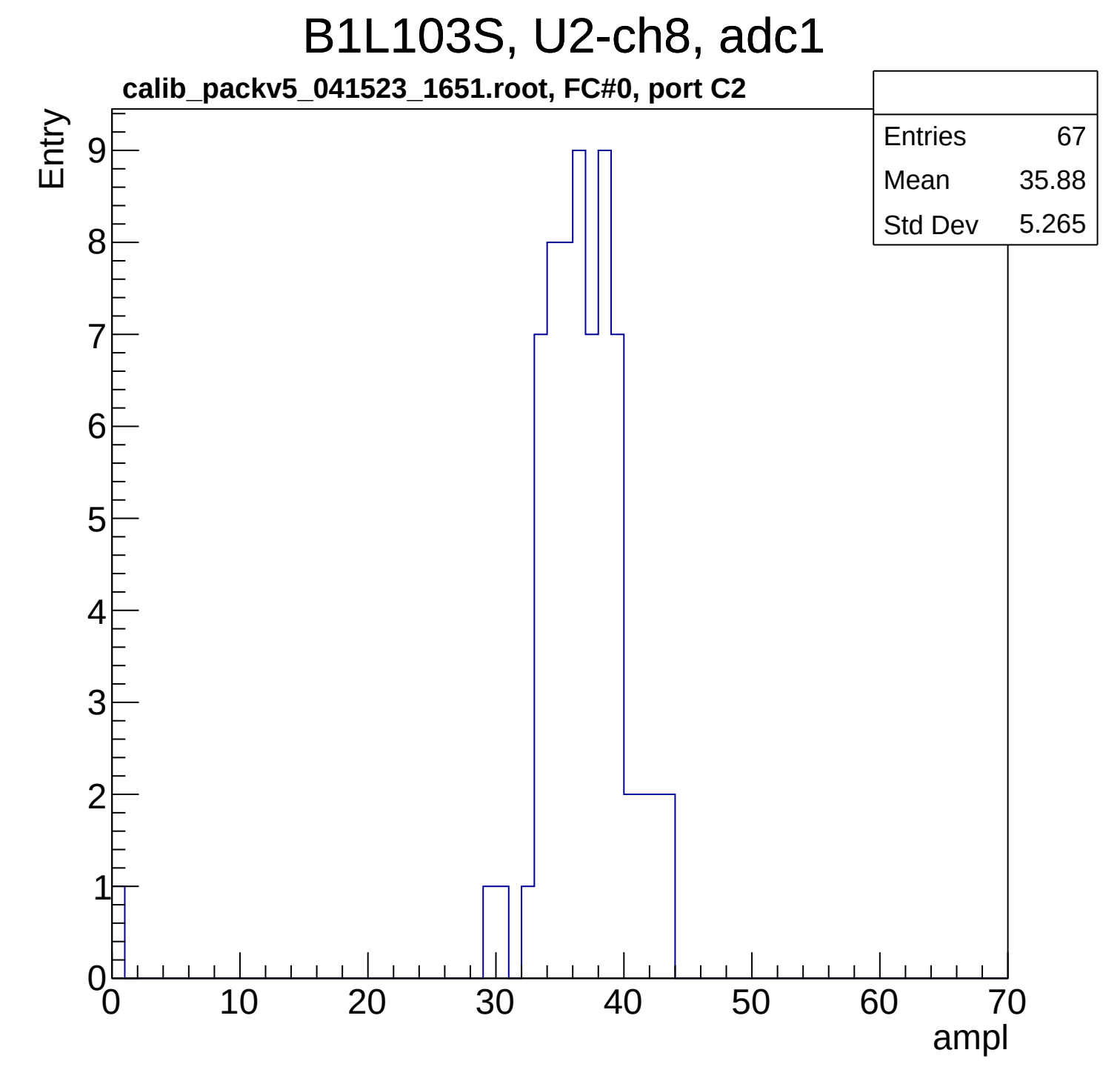

B1L103S, U2-ch7, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 55.1
Std Dev 2.717
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

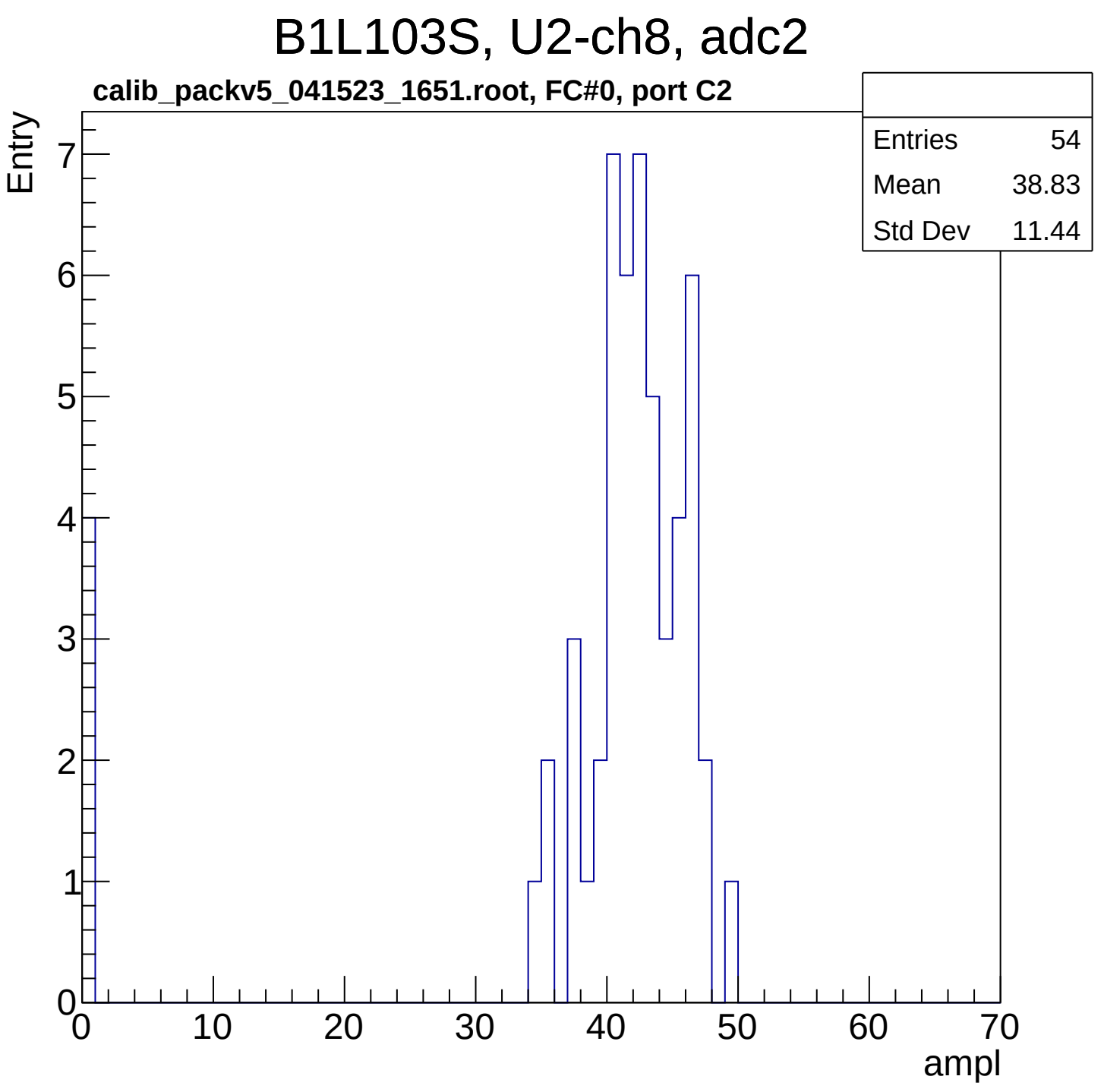

B1L103S, U2-ch7, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.88
Std Dev 8.662
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

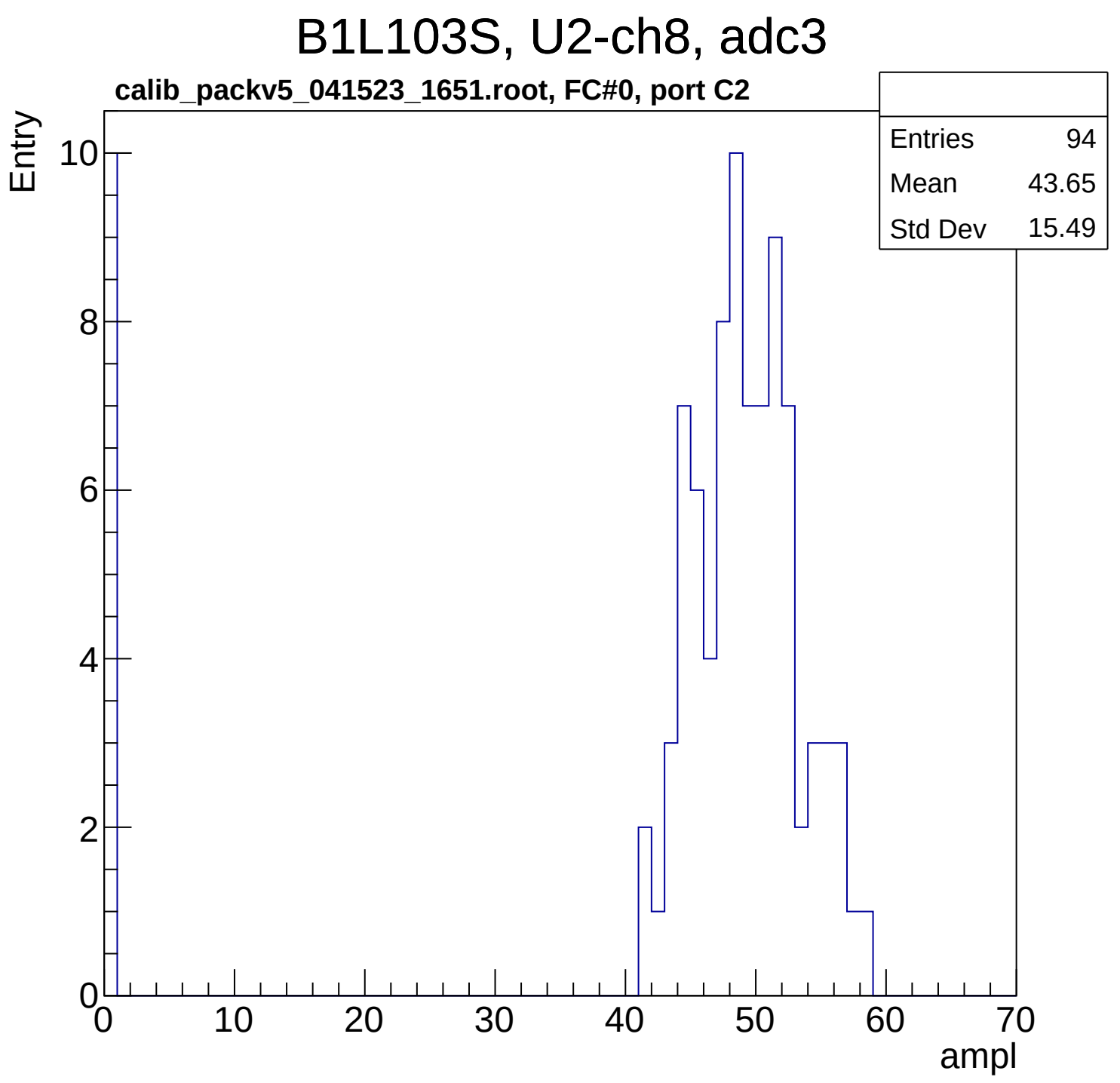

B1L103S, U2-ch7, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.83
Std Dev 2.192
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

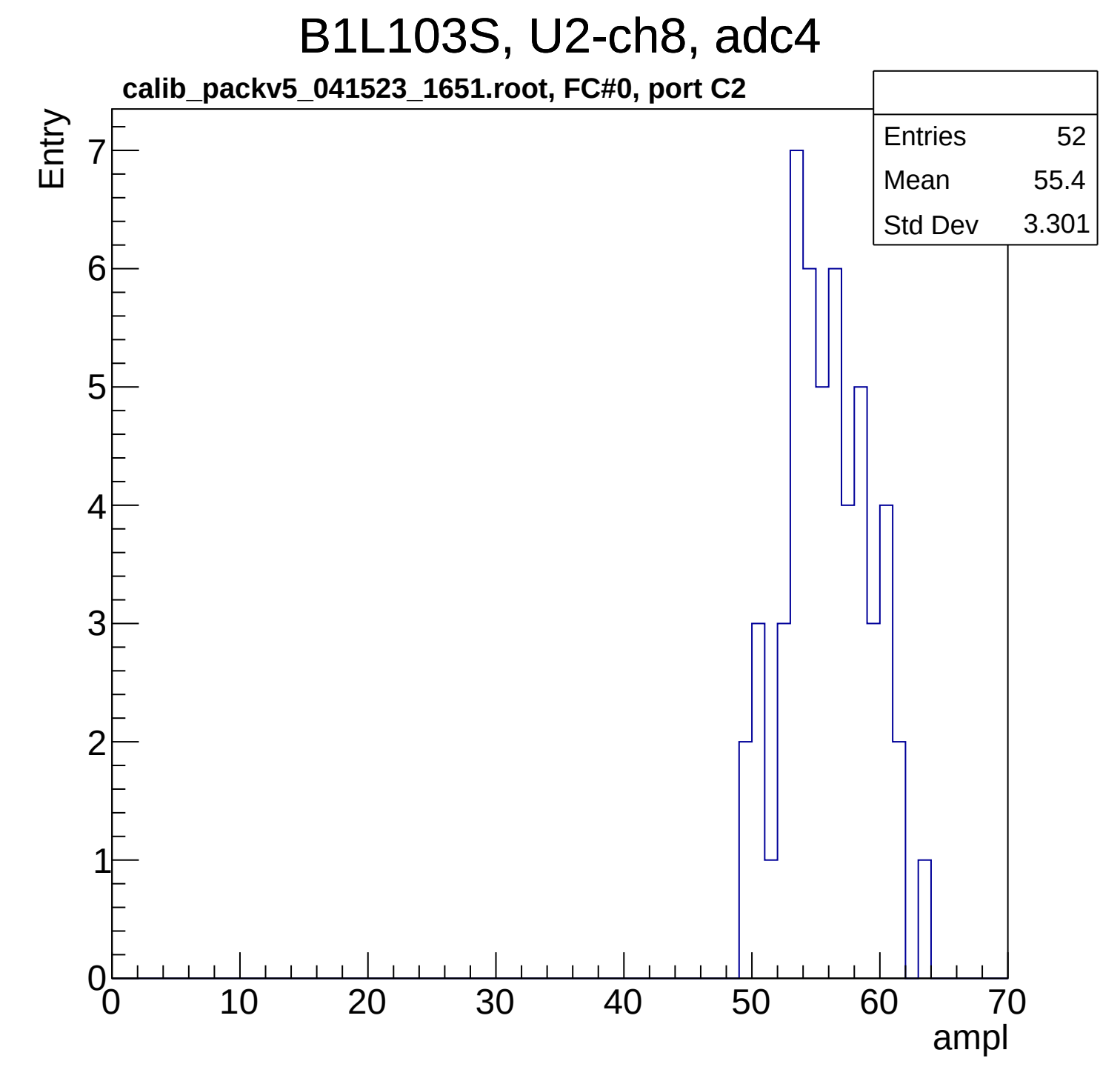

B1L103S, U2-ch7, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.211
Std Dev 5.136
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

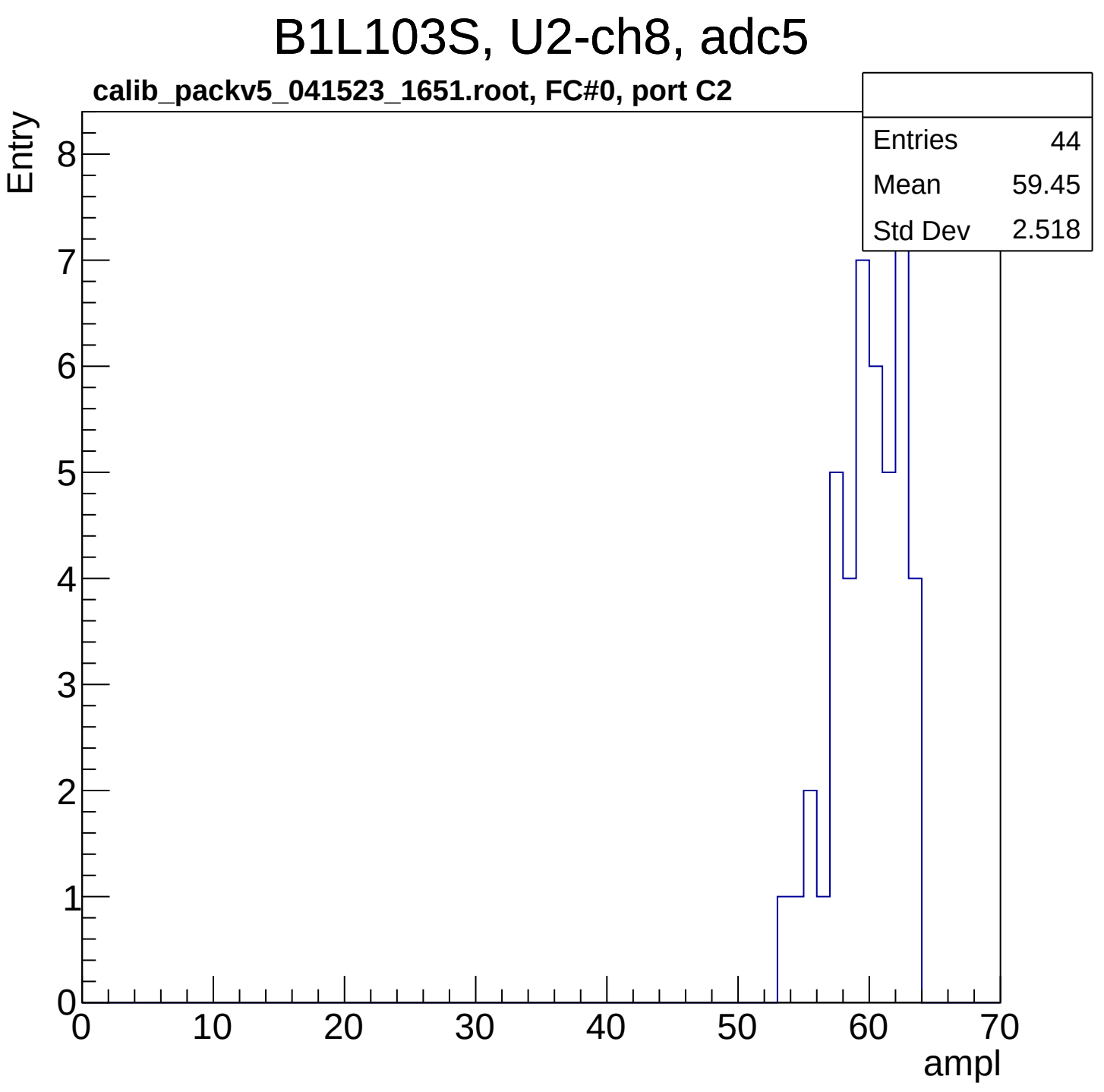

B1L103S, U2-ch8, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 23.99
Std Dev 11.05
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

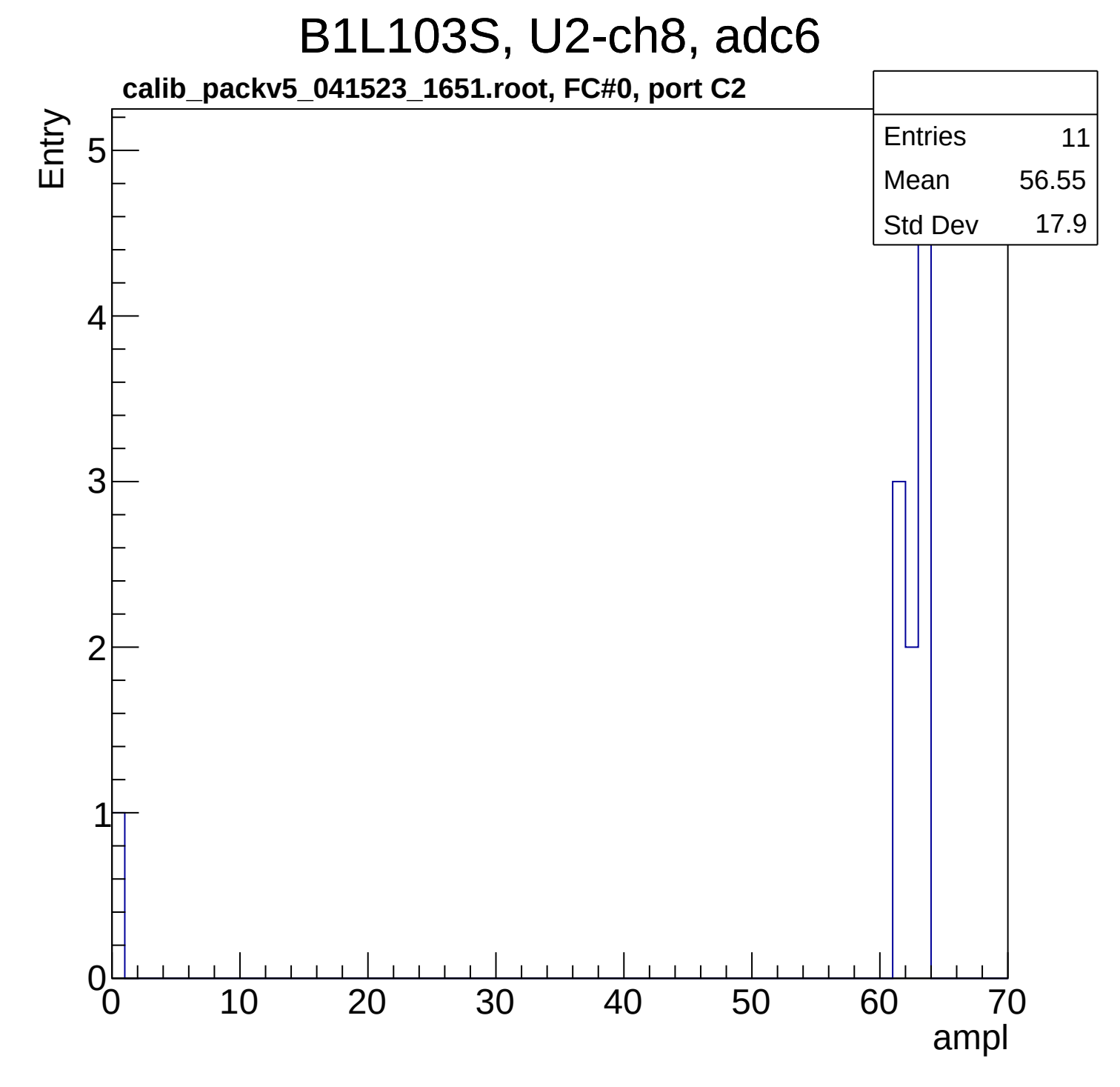

B1L103S, U2-ch8, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 35.88
Std Dev 5.265
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

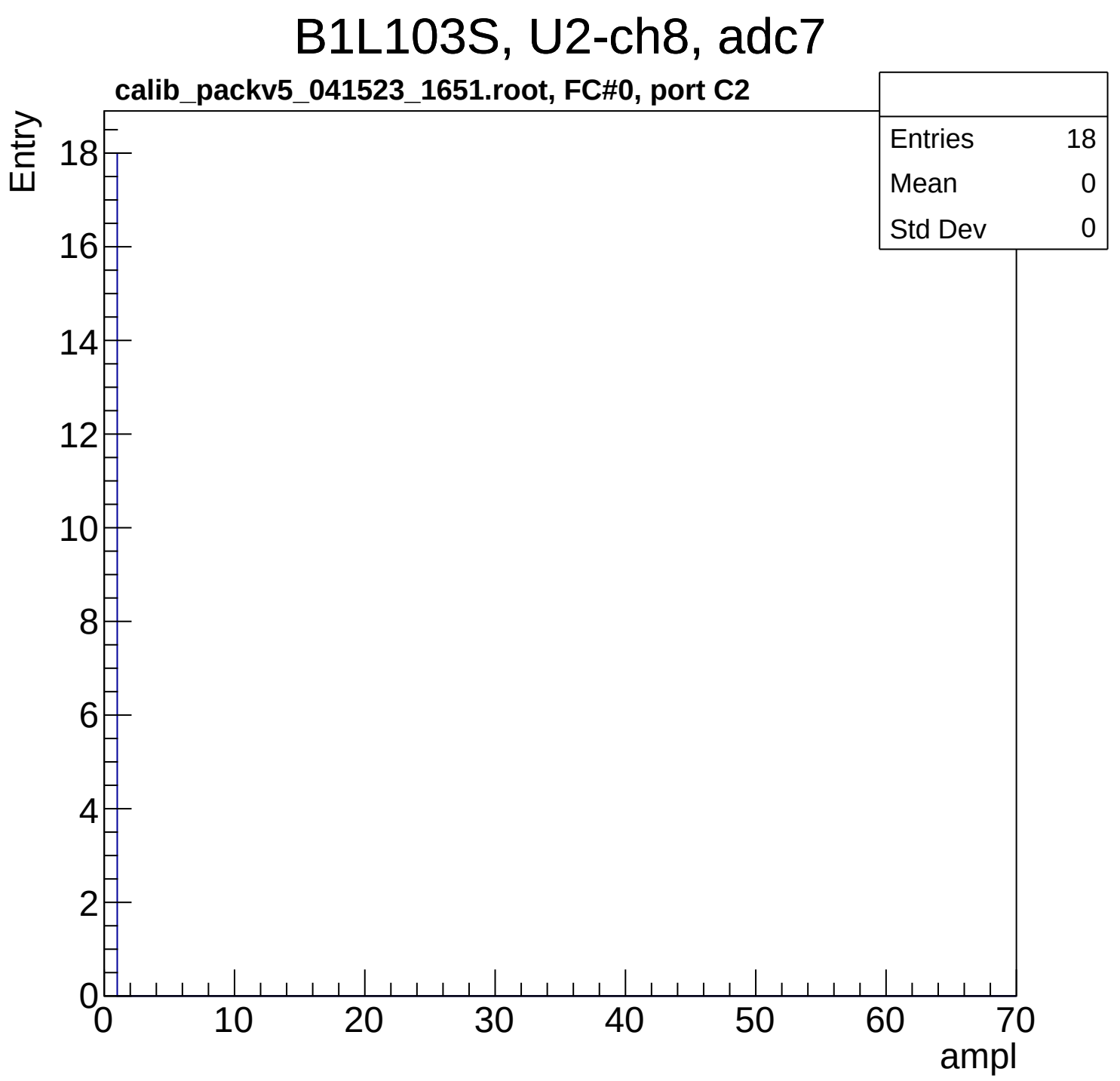

B1L103S, U2-ch8, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 38.83
Std Dev 11.44
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

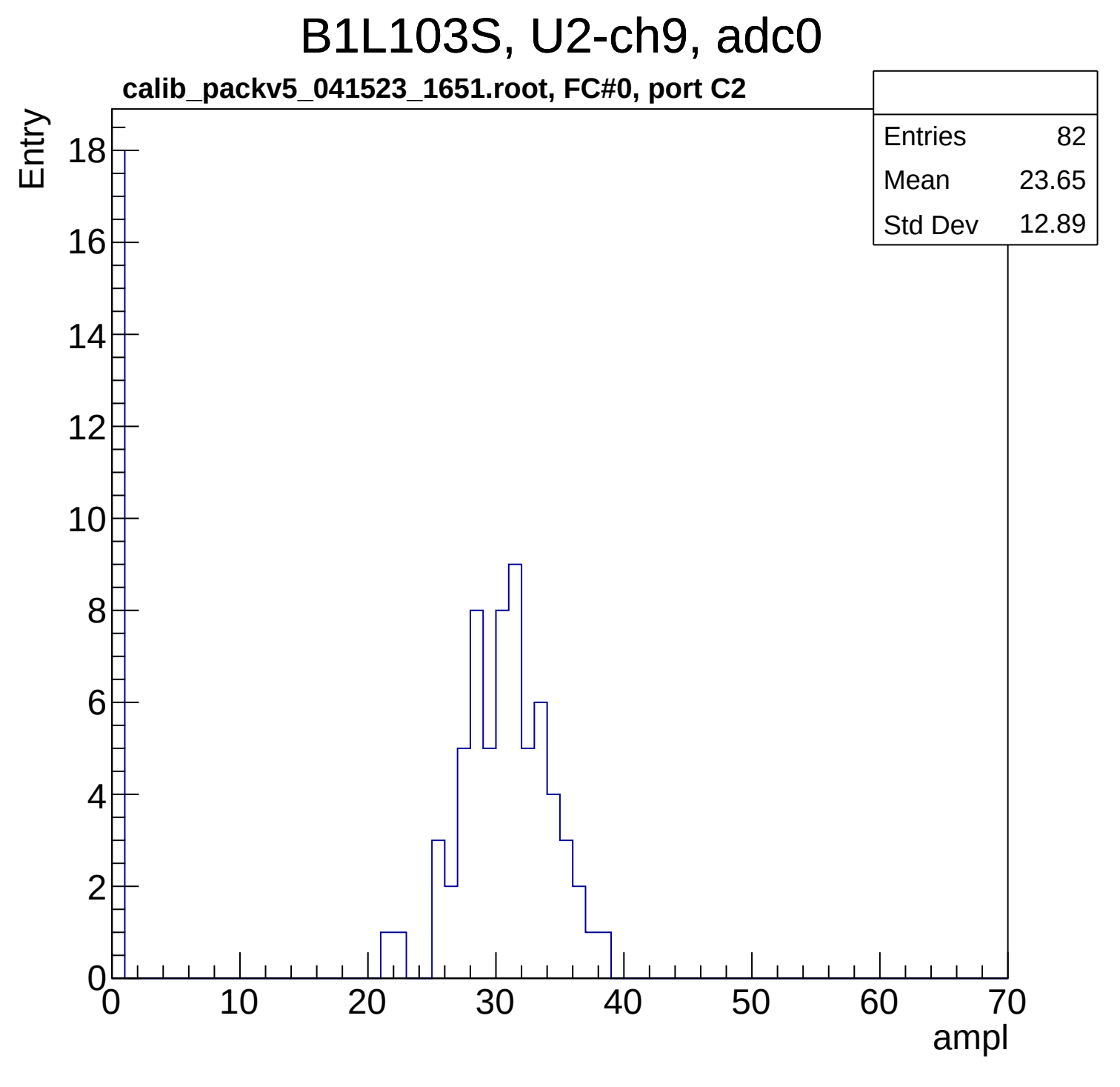

B1L103S, U2-ch8, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 43.65
Std Dev 15.49
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

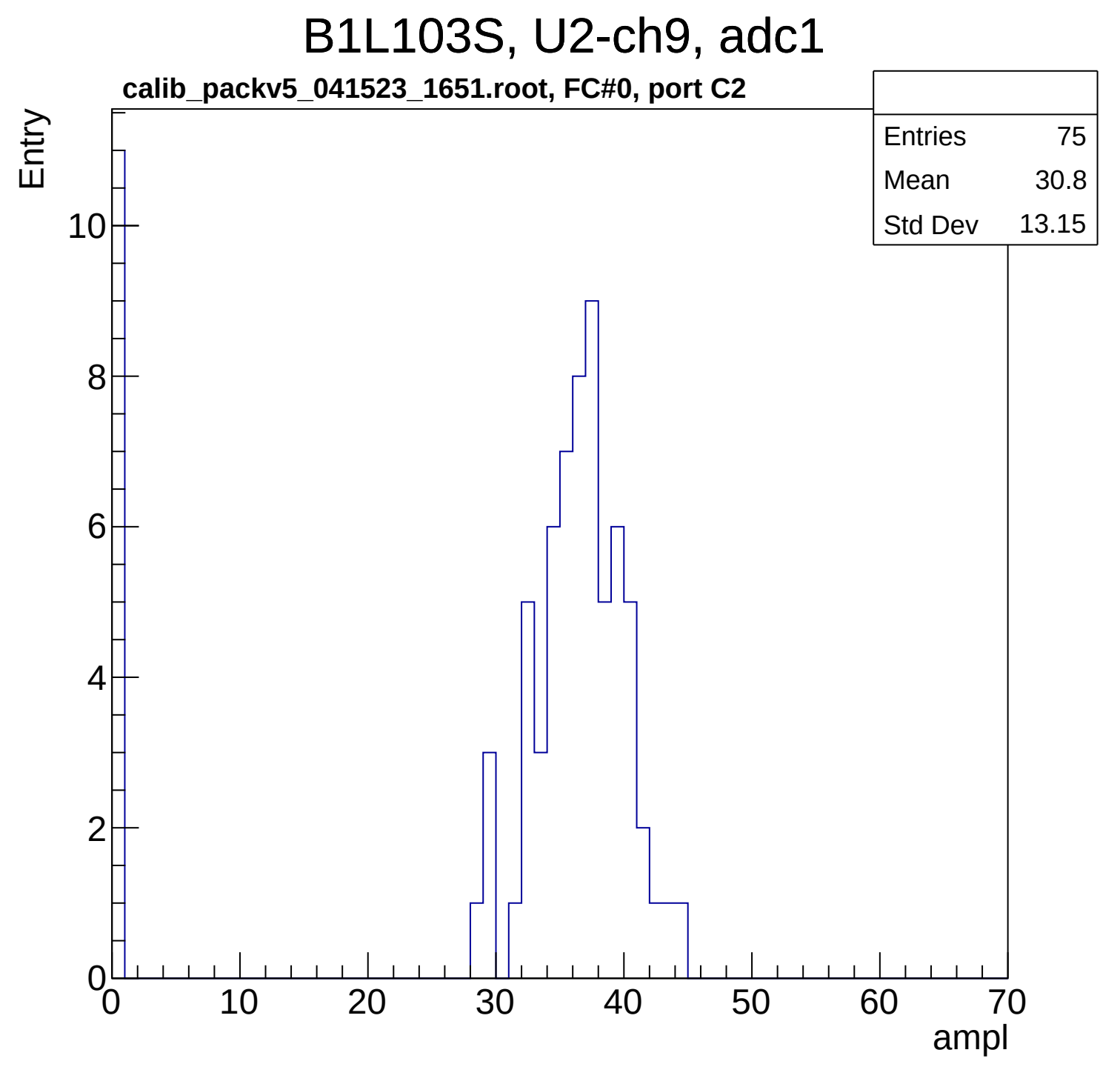

B1L103S, U2-ch8, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 55.4
Std Dev 3.301
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

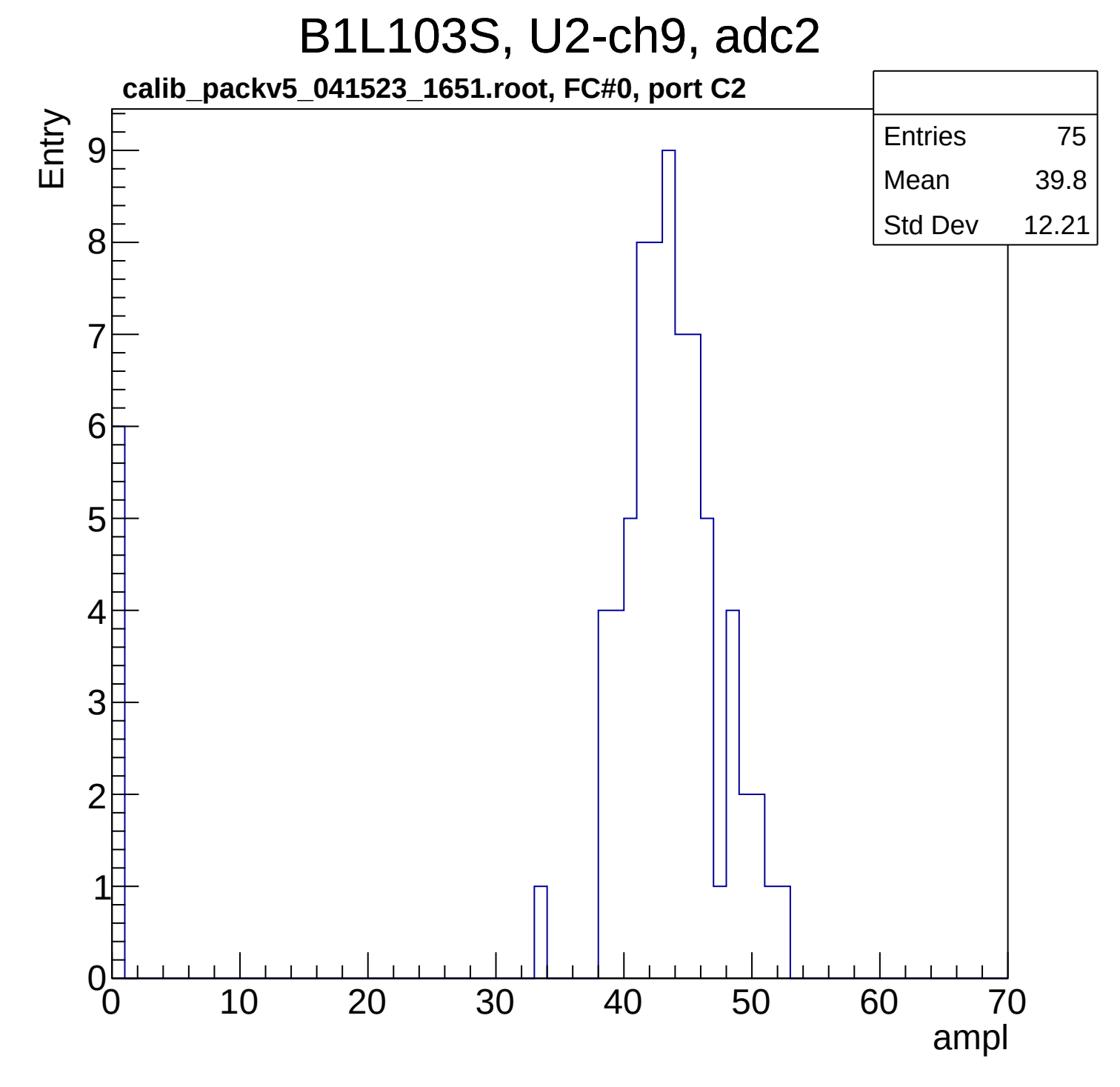

B1L103S, U2-ch8, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 59.45
Std Dev 2.518
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

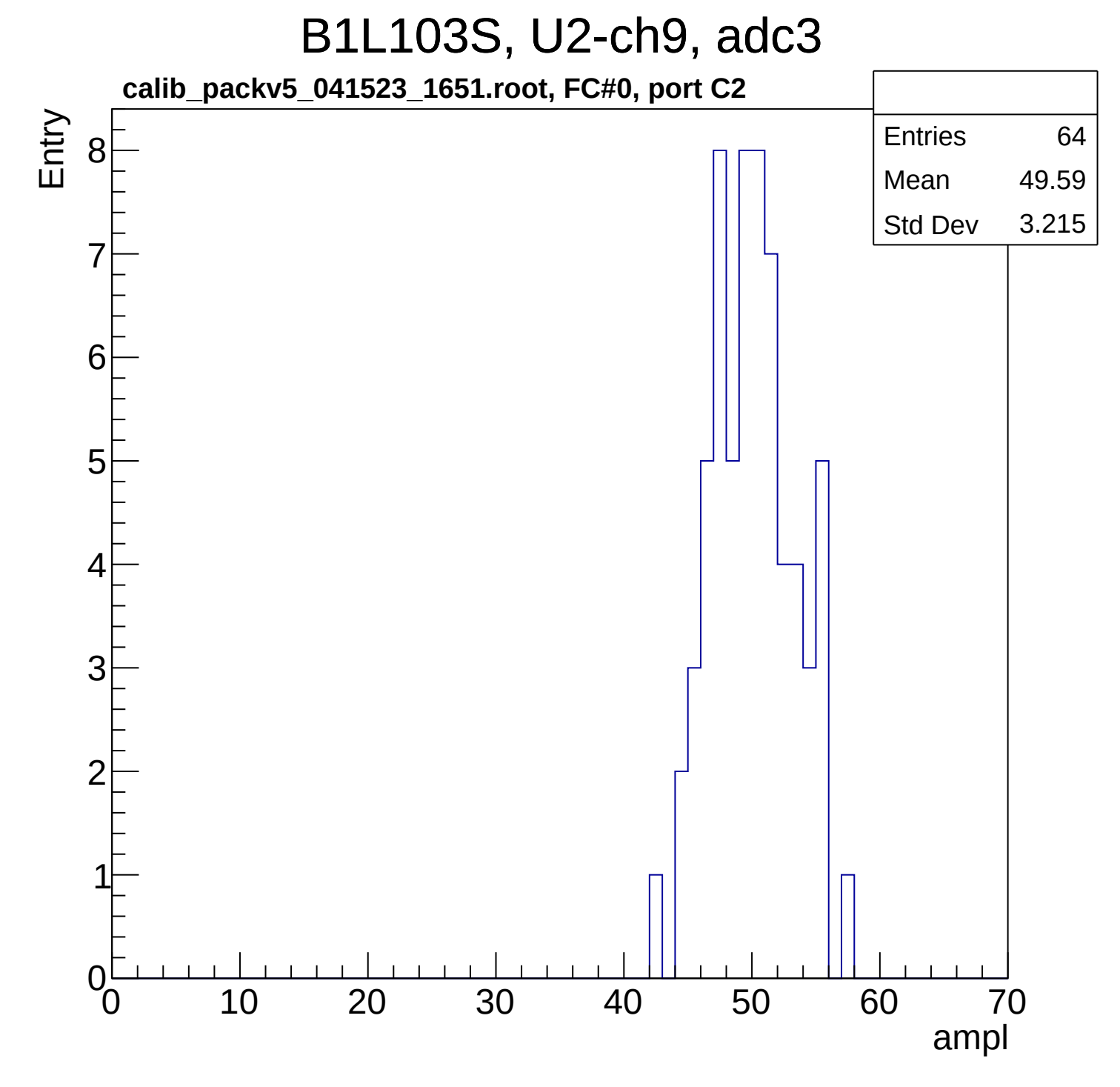

B1L103S, U2-ch8, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 56.55
Std Dev 17.9
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

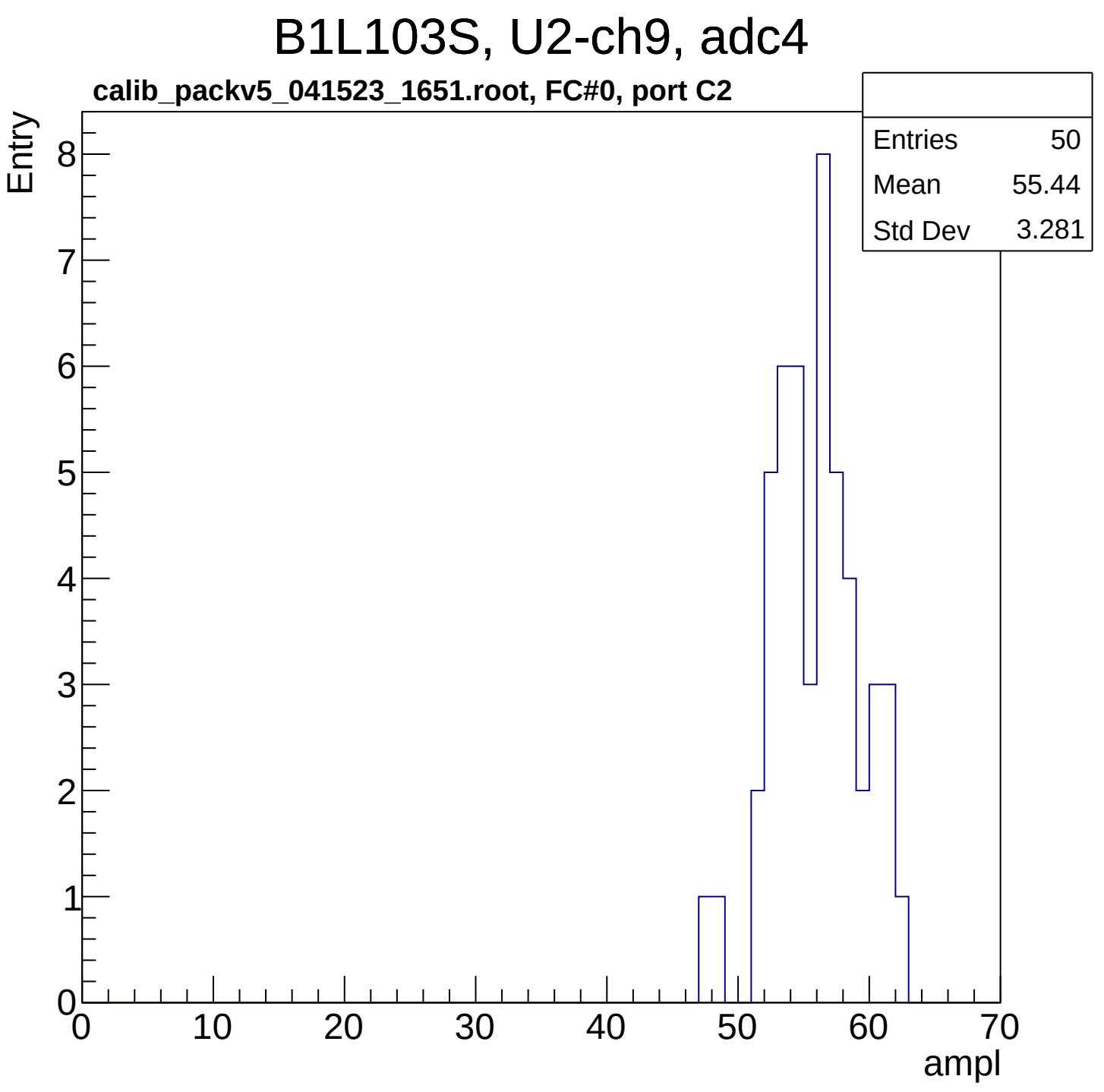

B1L103S, U2-ch8, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

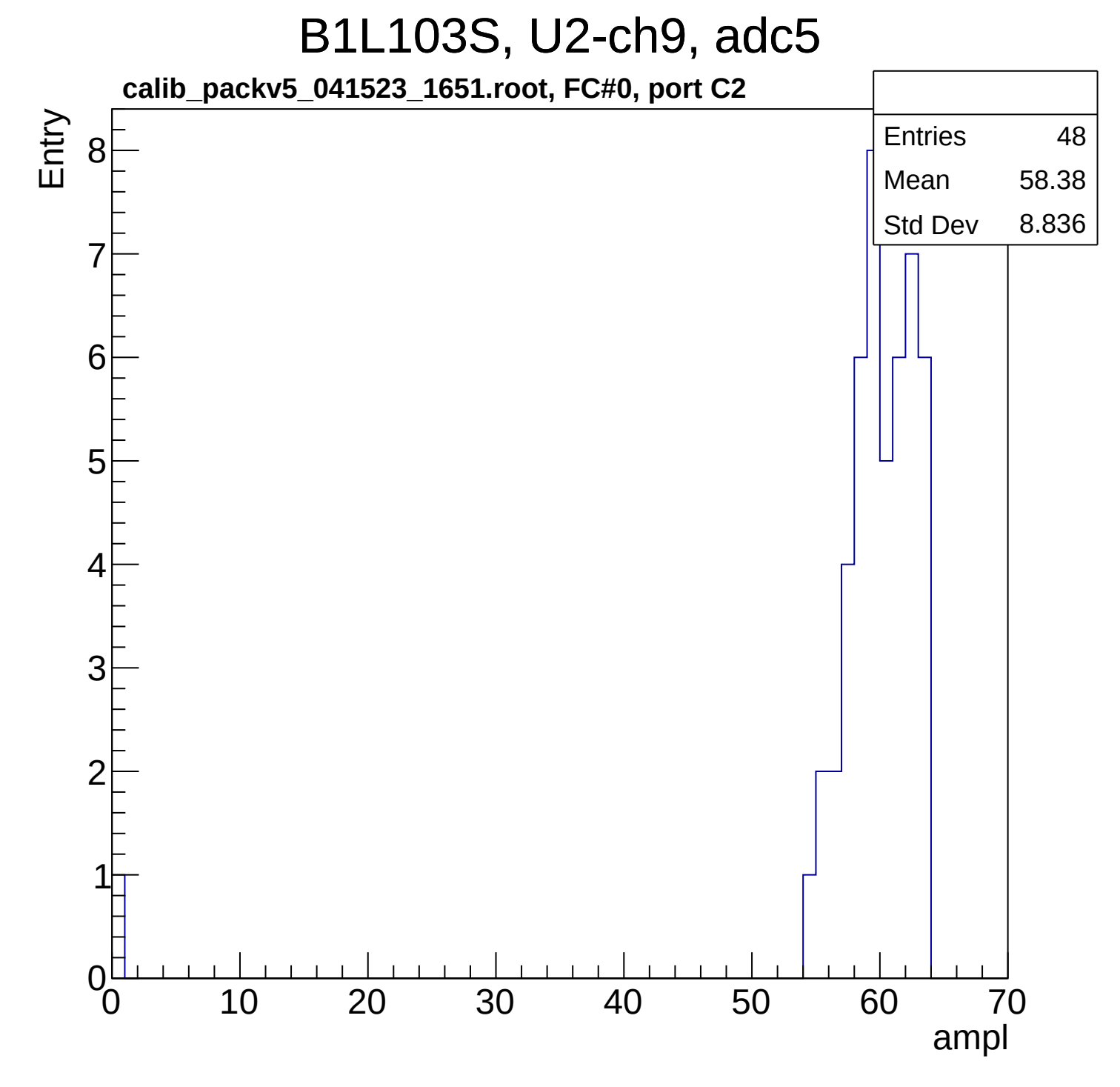

B1L103S, U2-ch9, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 23.65
Std Dev 12.89
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

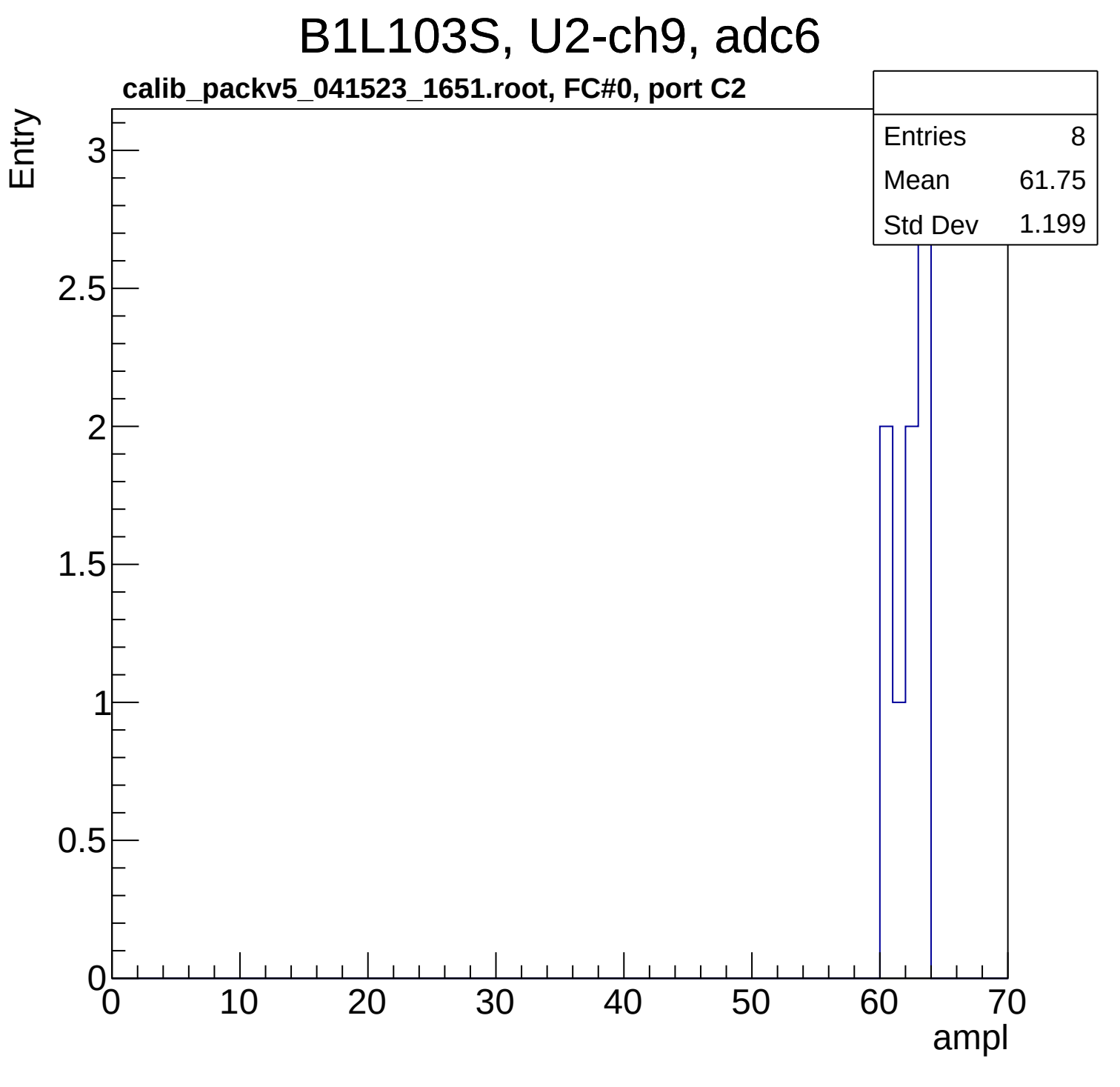

B1L103S, U2-ch9, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 30.8
Std Dev 13.15
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

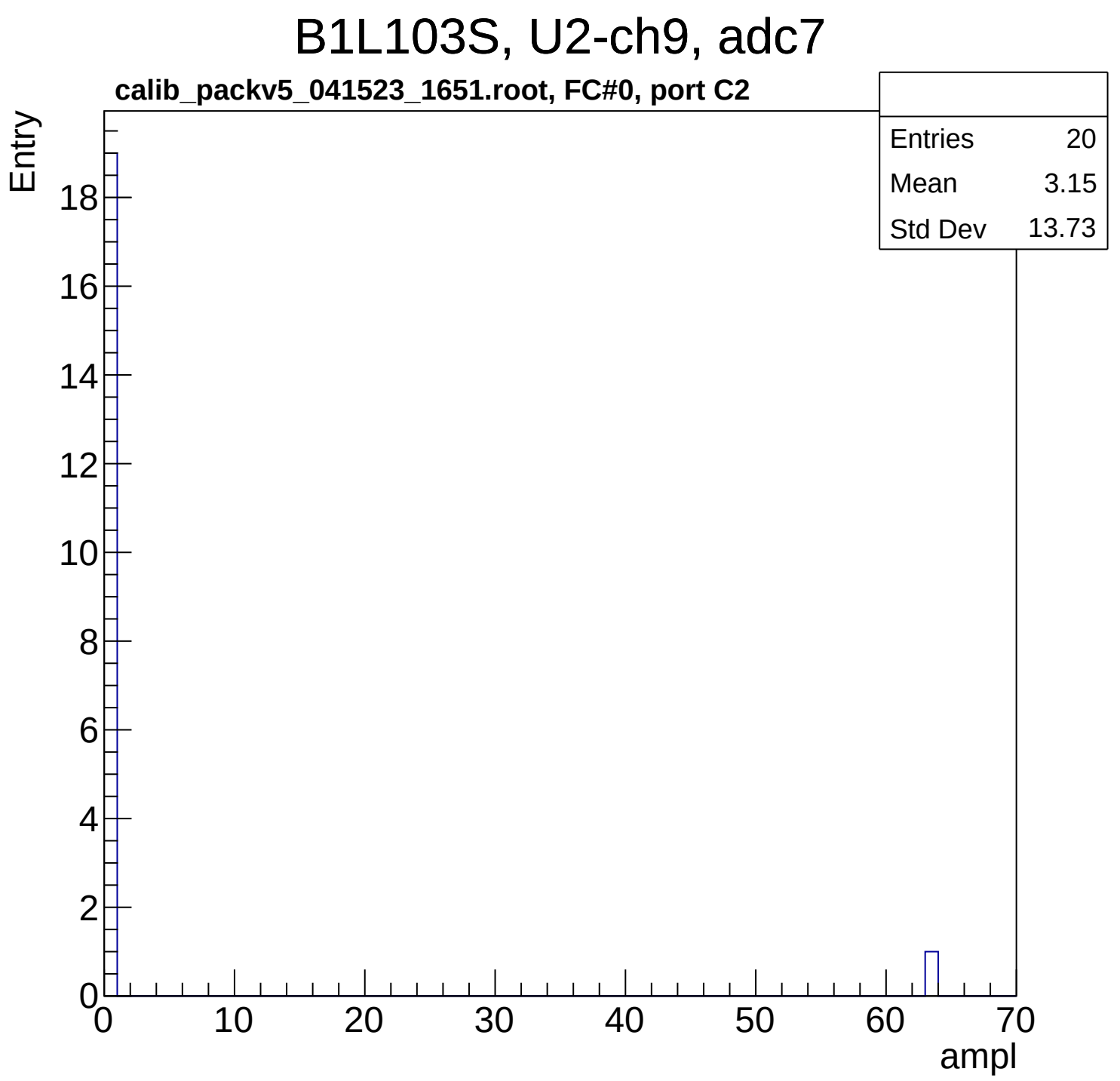

B1L103S, U2-ch9, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 39.8
Std Dev 12.21
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

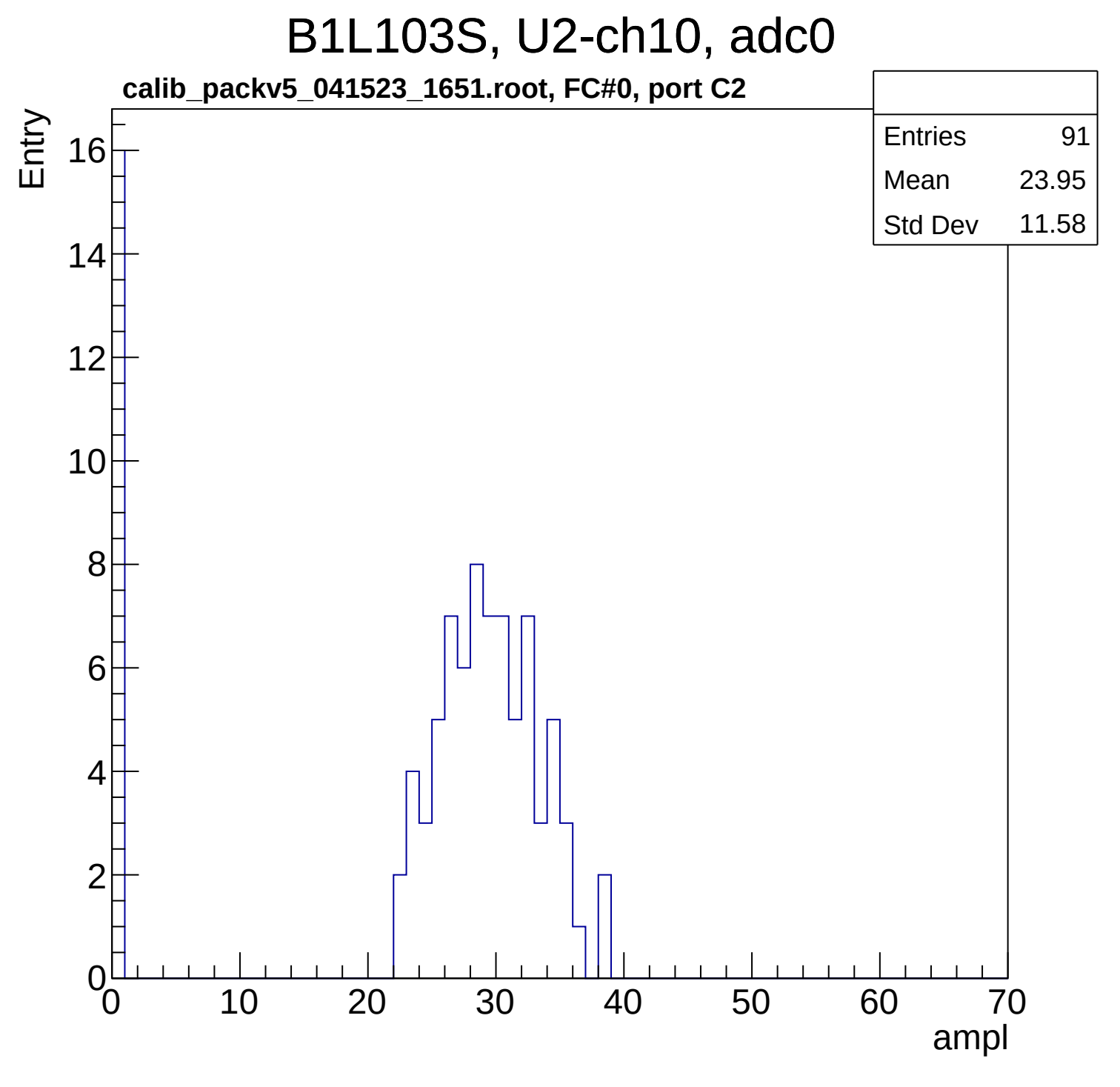

B1L103S, U2-ch9, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 49.59
Std Dev 3.215
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

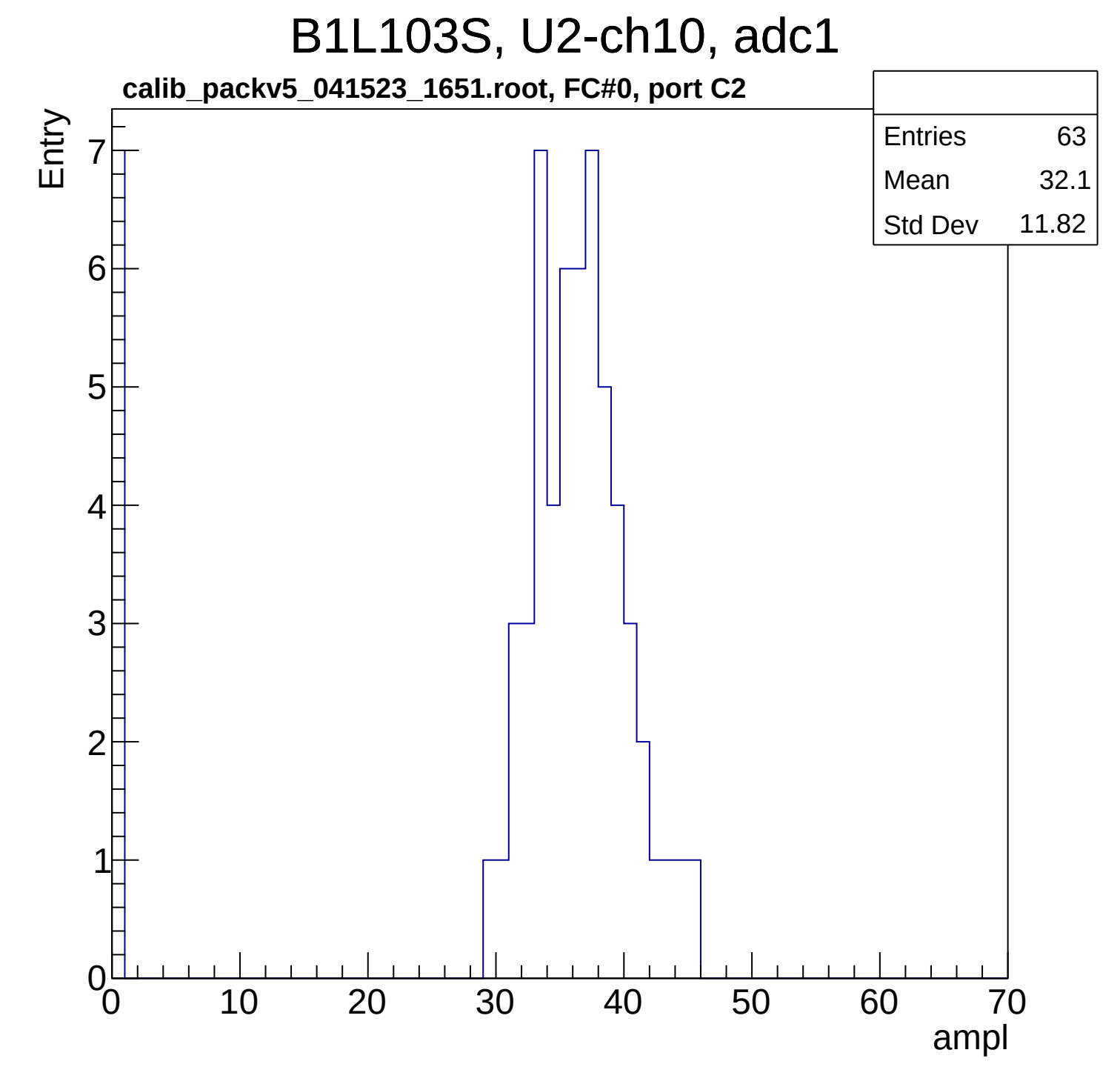

B1L103S, U2-ch9, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 55.44
Std Dev 3.281
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

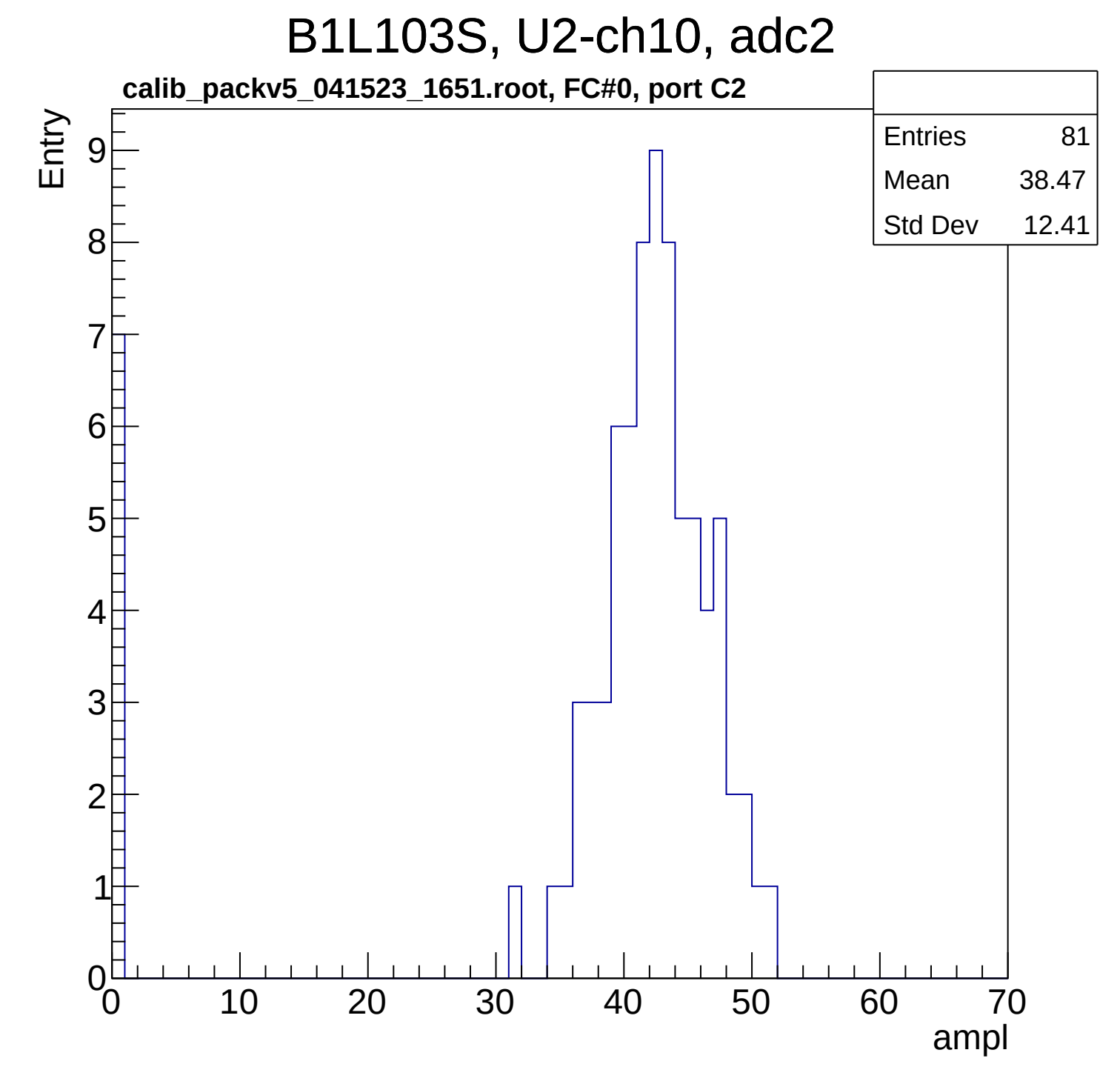

B1L103S, U2-ch9, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.38
Std Dev 8.836
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

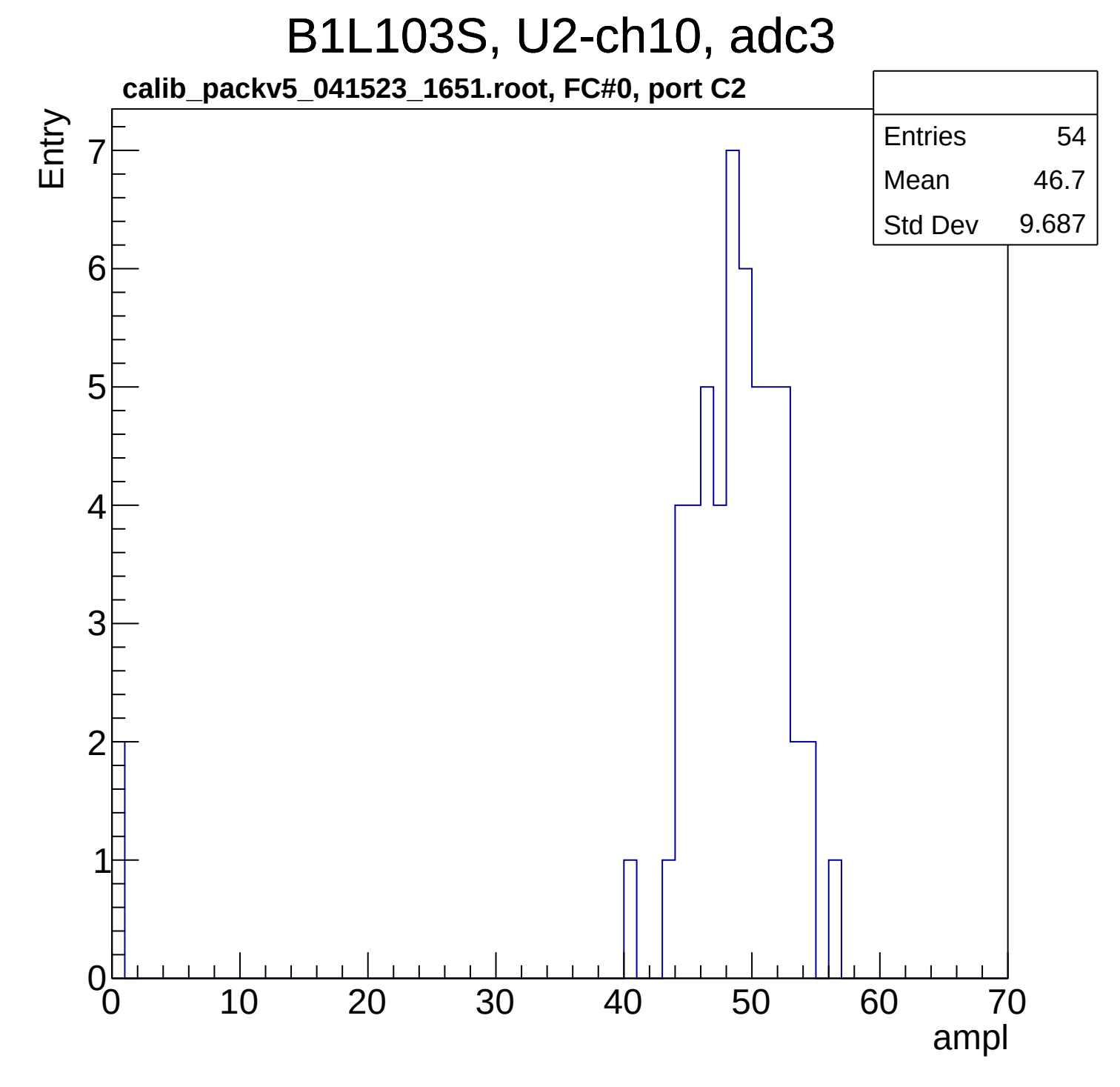

B1L103S, U2-ch9, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.75
Std Dev 1.199
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

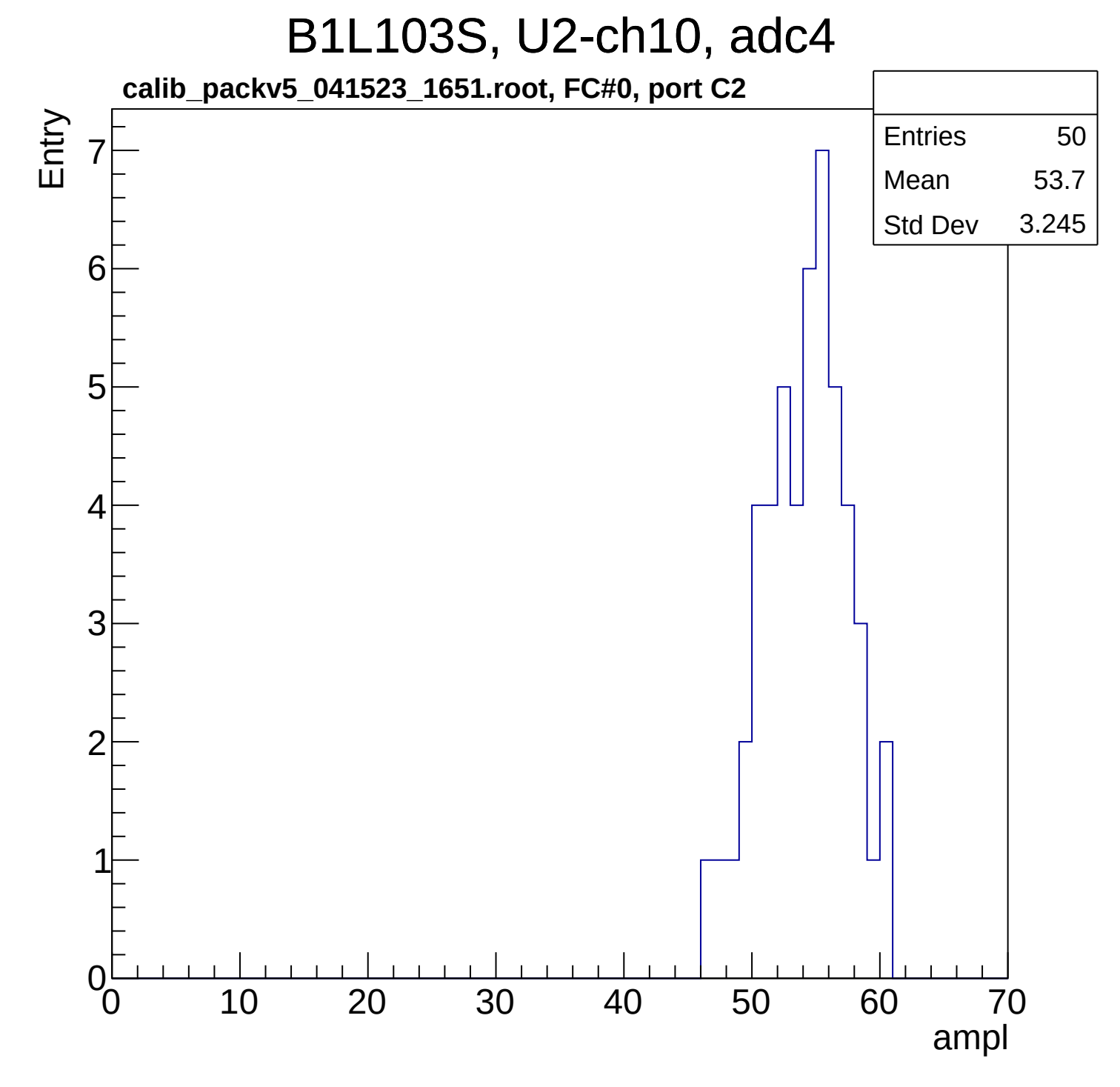

B1L103S, U2-ch9, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

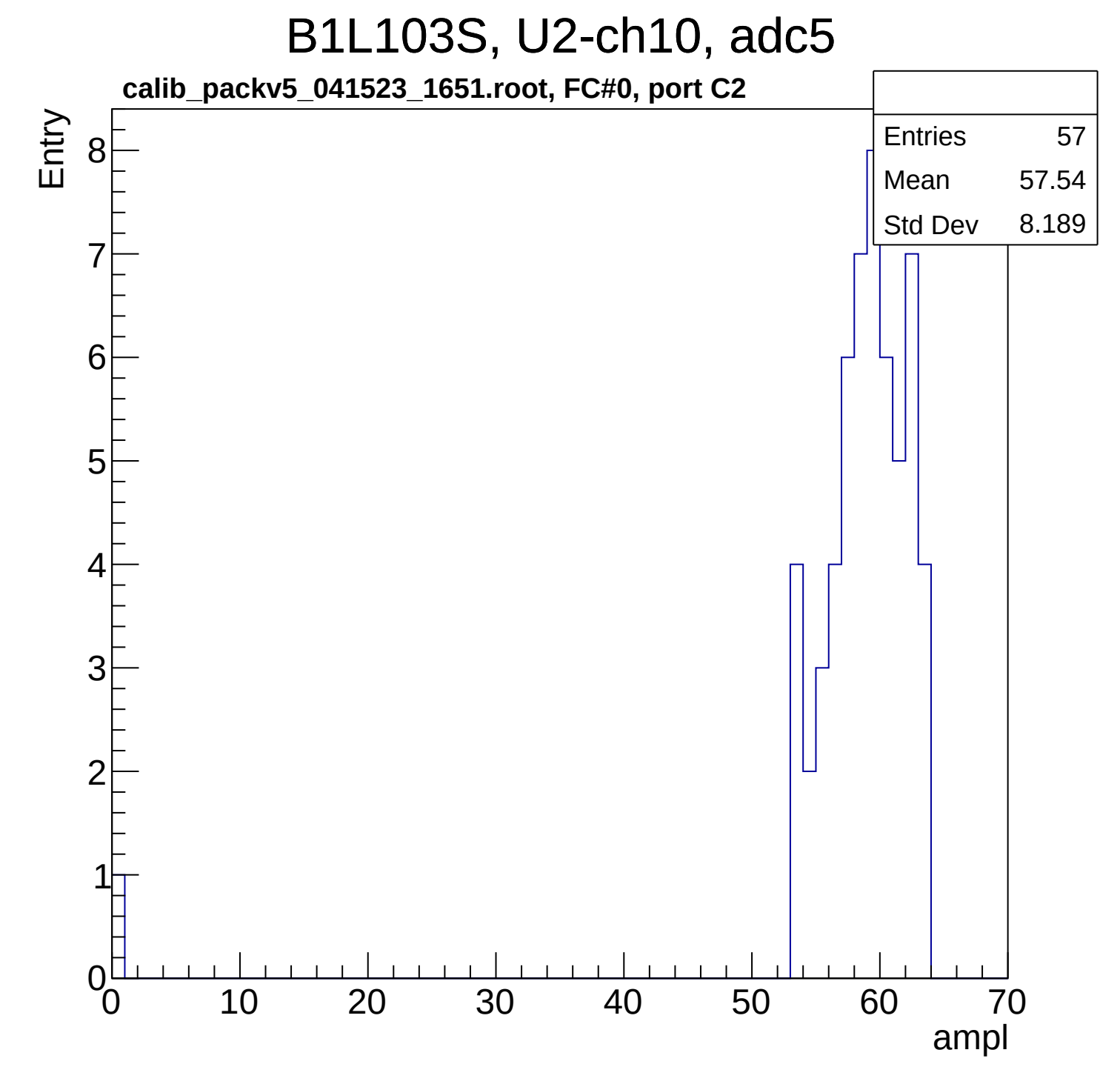

B1L103S, U2-ch10, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 23.95
Std Dev 11.58
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

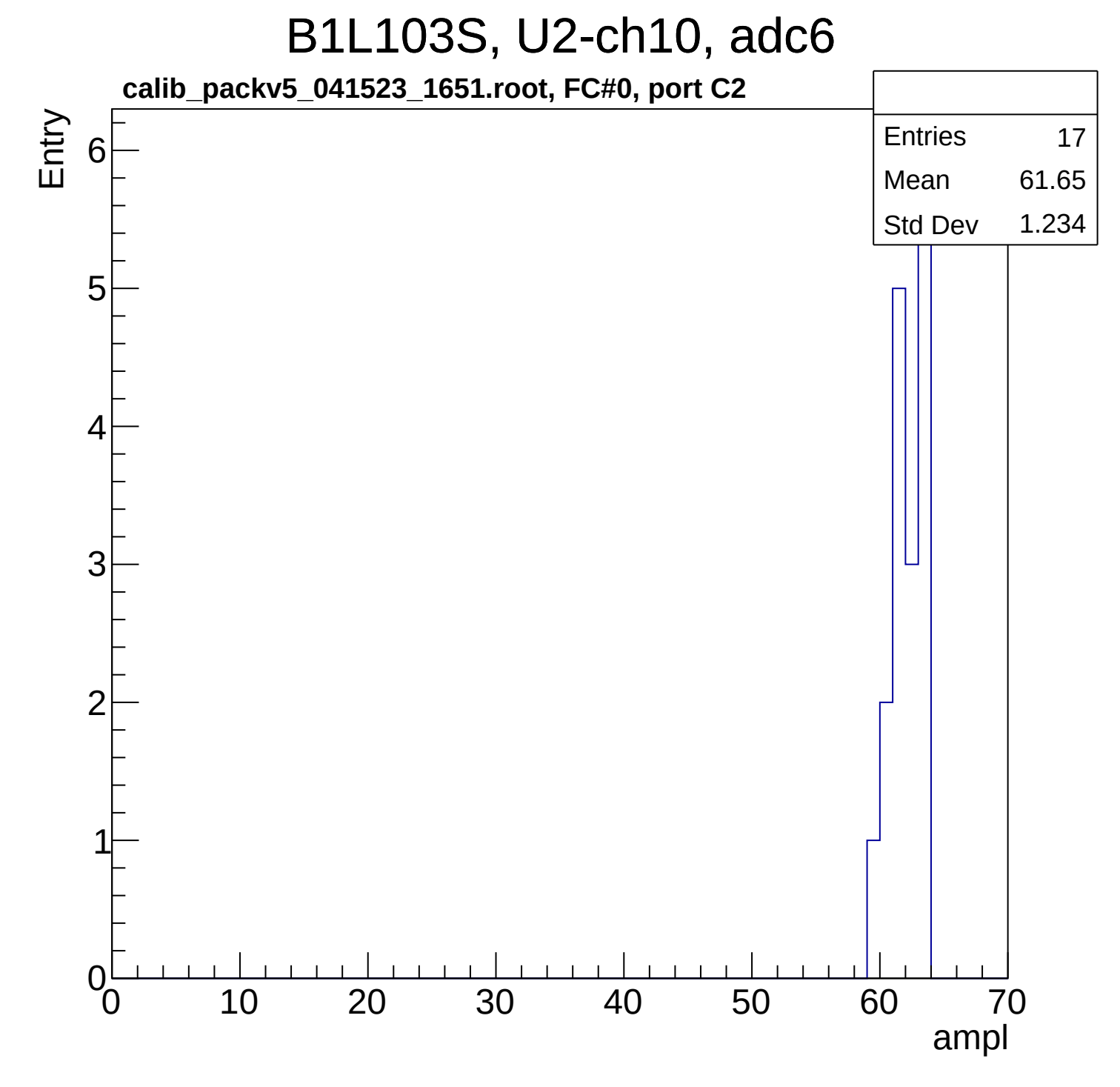

B1L103S, U2-ch10, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 32.1
Std Dev 11.82
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

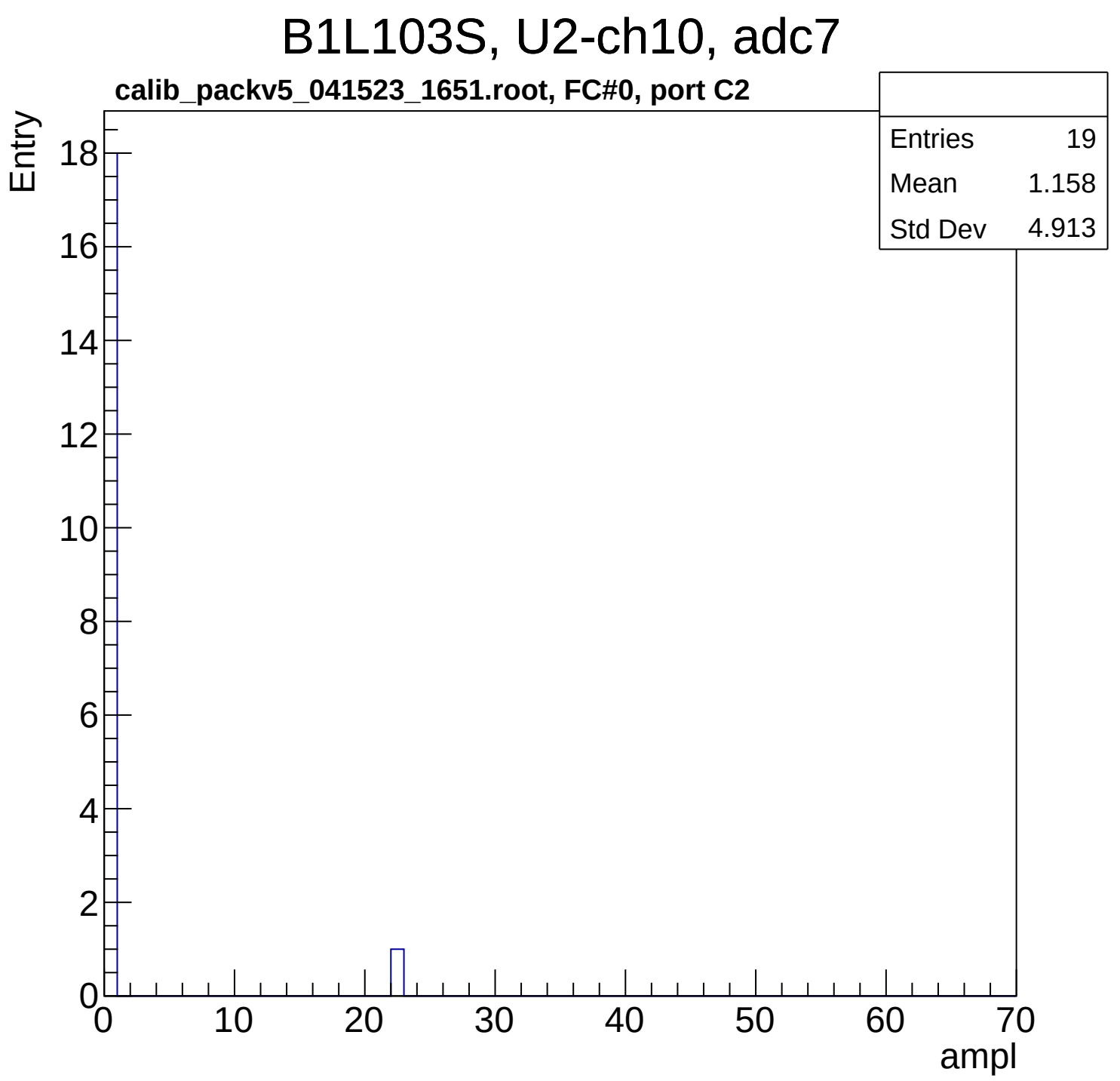

B1L103S, U2-ch10, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 38.47
Std Dev 12.41
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

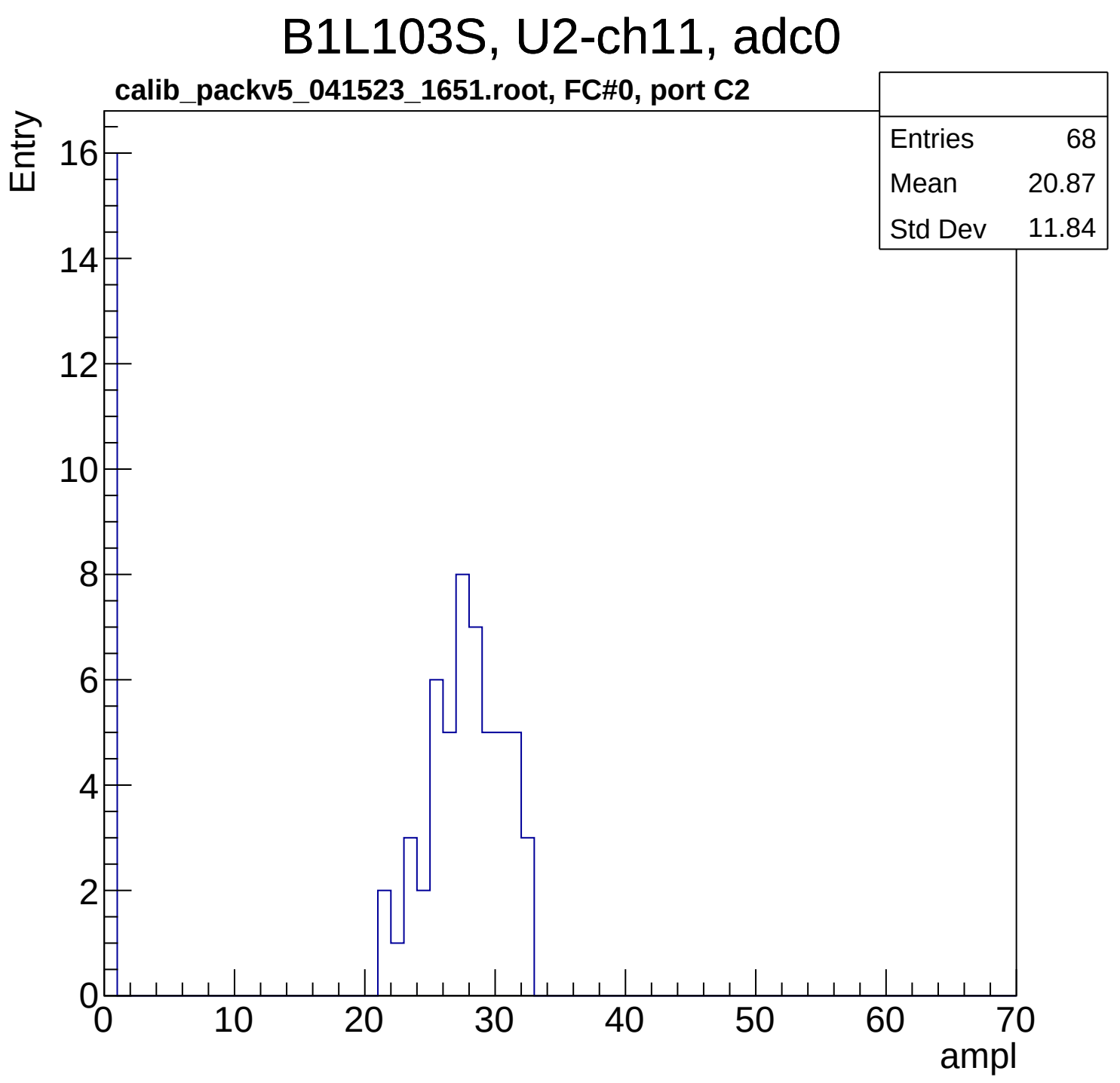

B1L103S, U2-ch10, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 46.7
Std Dev 9.687
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

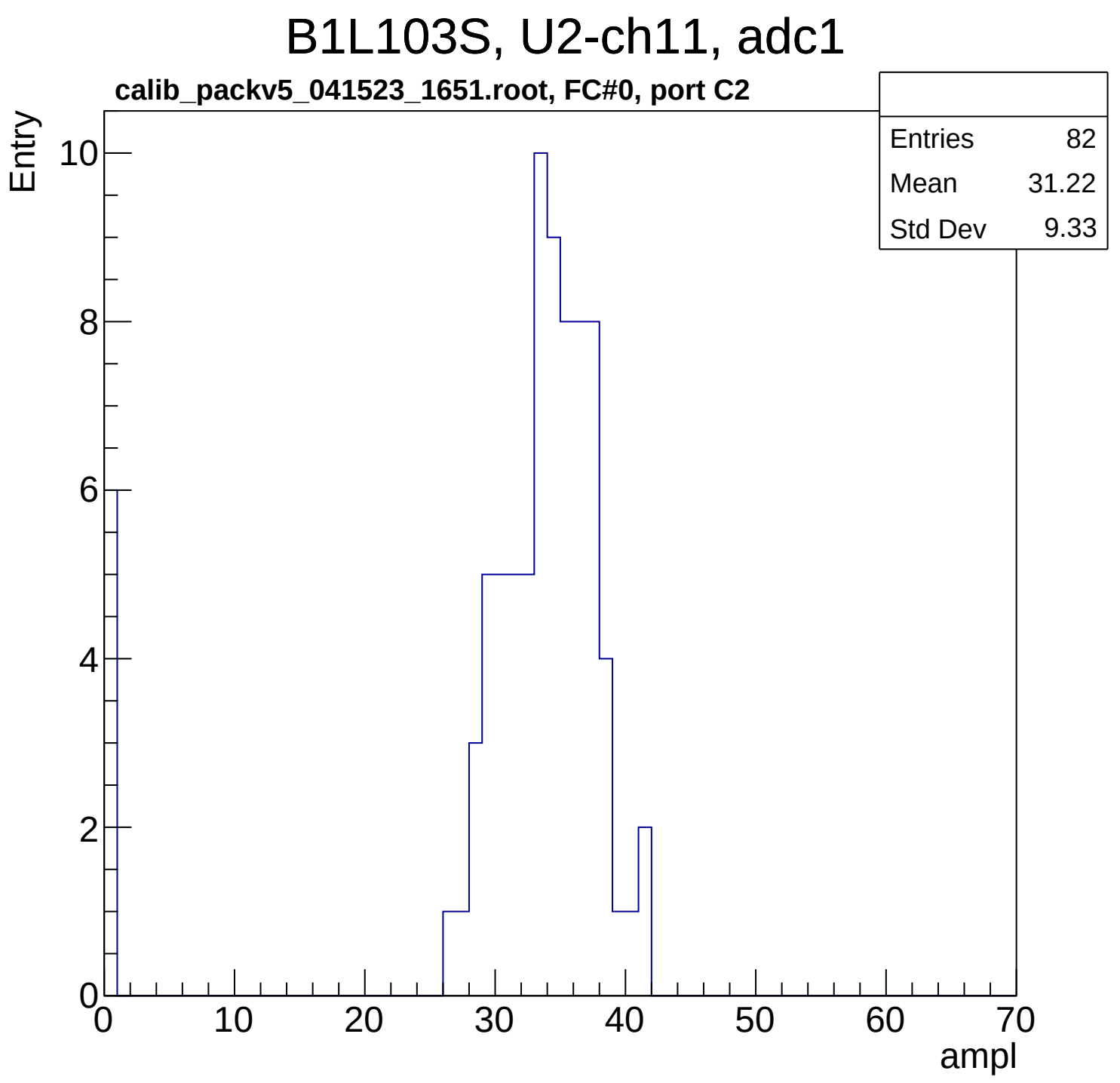

B1L103S, U2-ch10, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 53.7
Std Dev 3.245
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

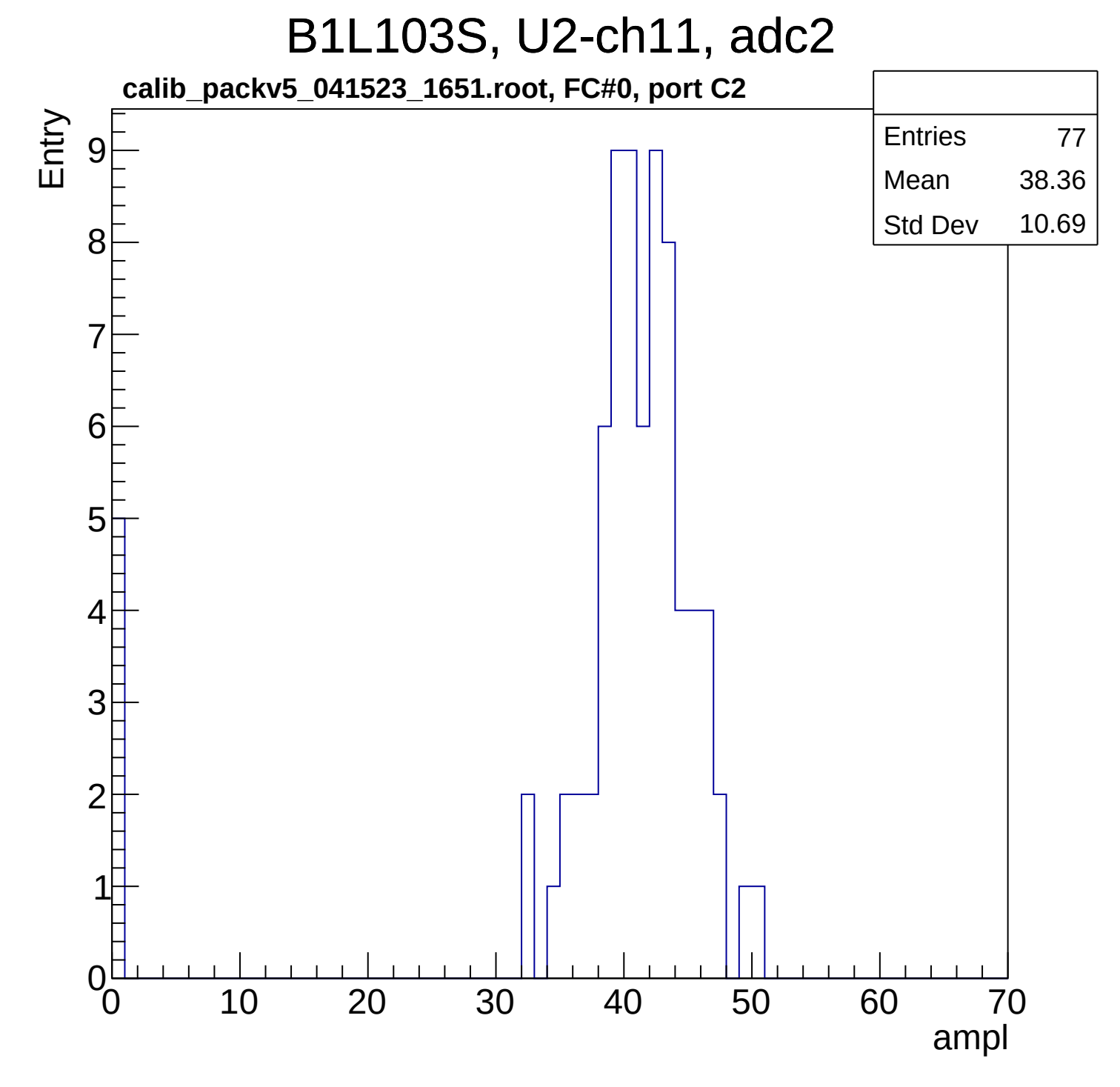

B1L103S, U2-ch10, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 57.54
Std Dev 8.189
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

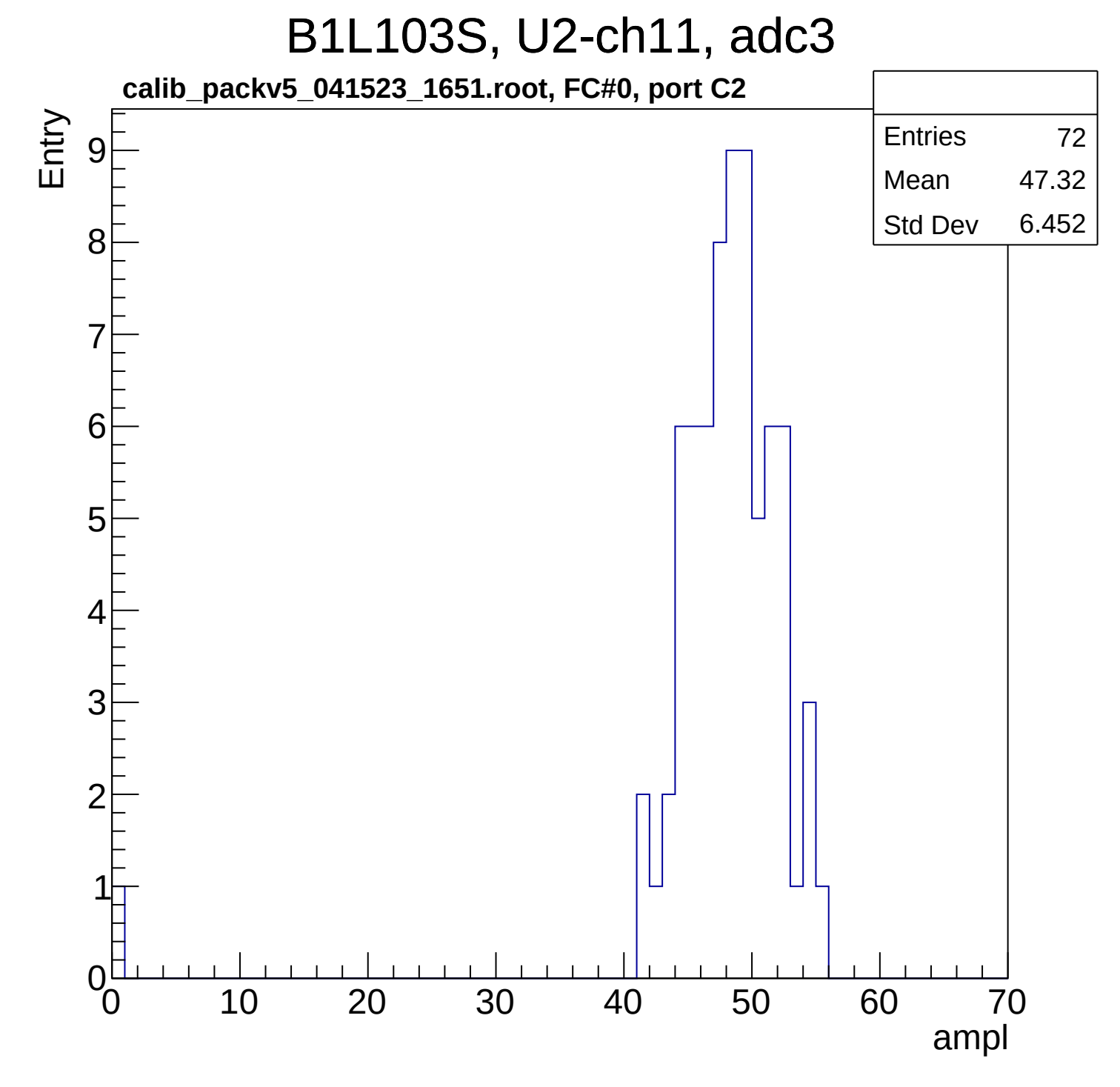

B1L103S, U2-ch10, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.65
Std Dev 1.234
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

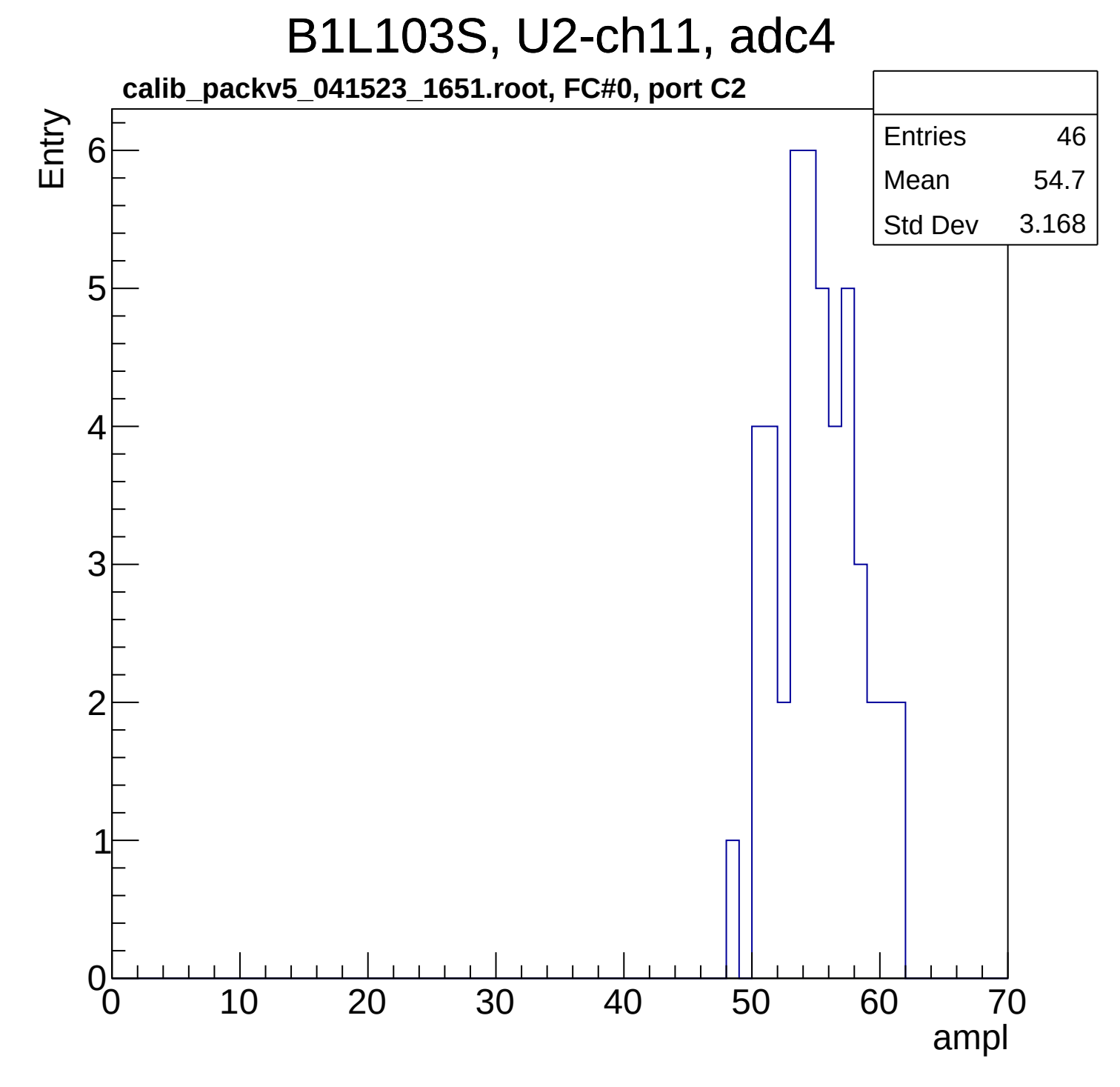

B1L103S, U2-ch10, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

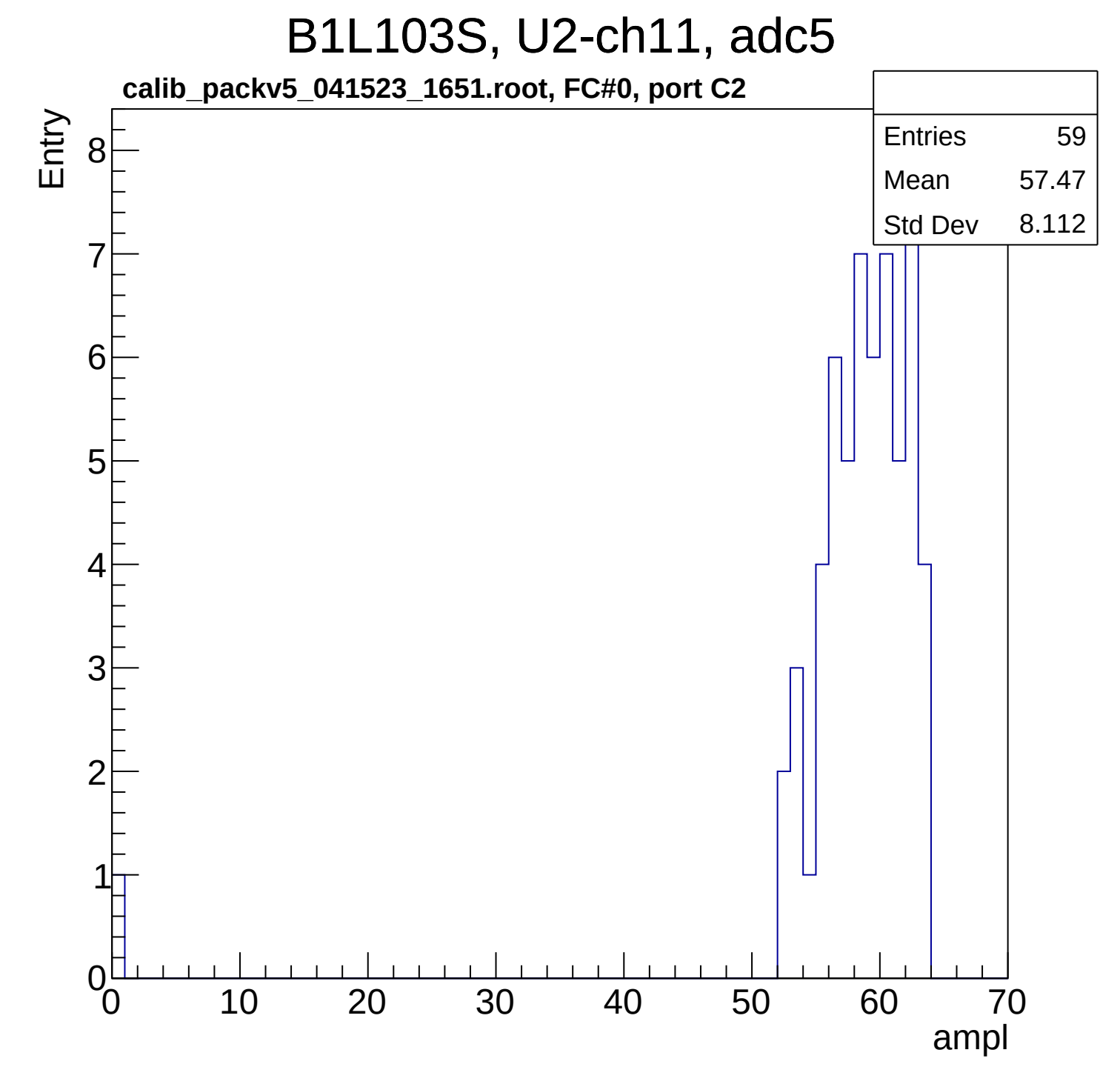

B1L103S, U2-ch11, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 20.87
Std Dev 11.84
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

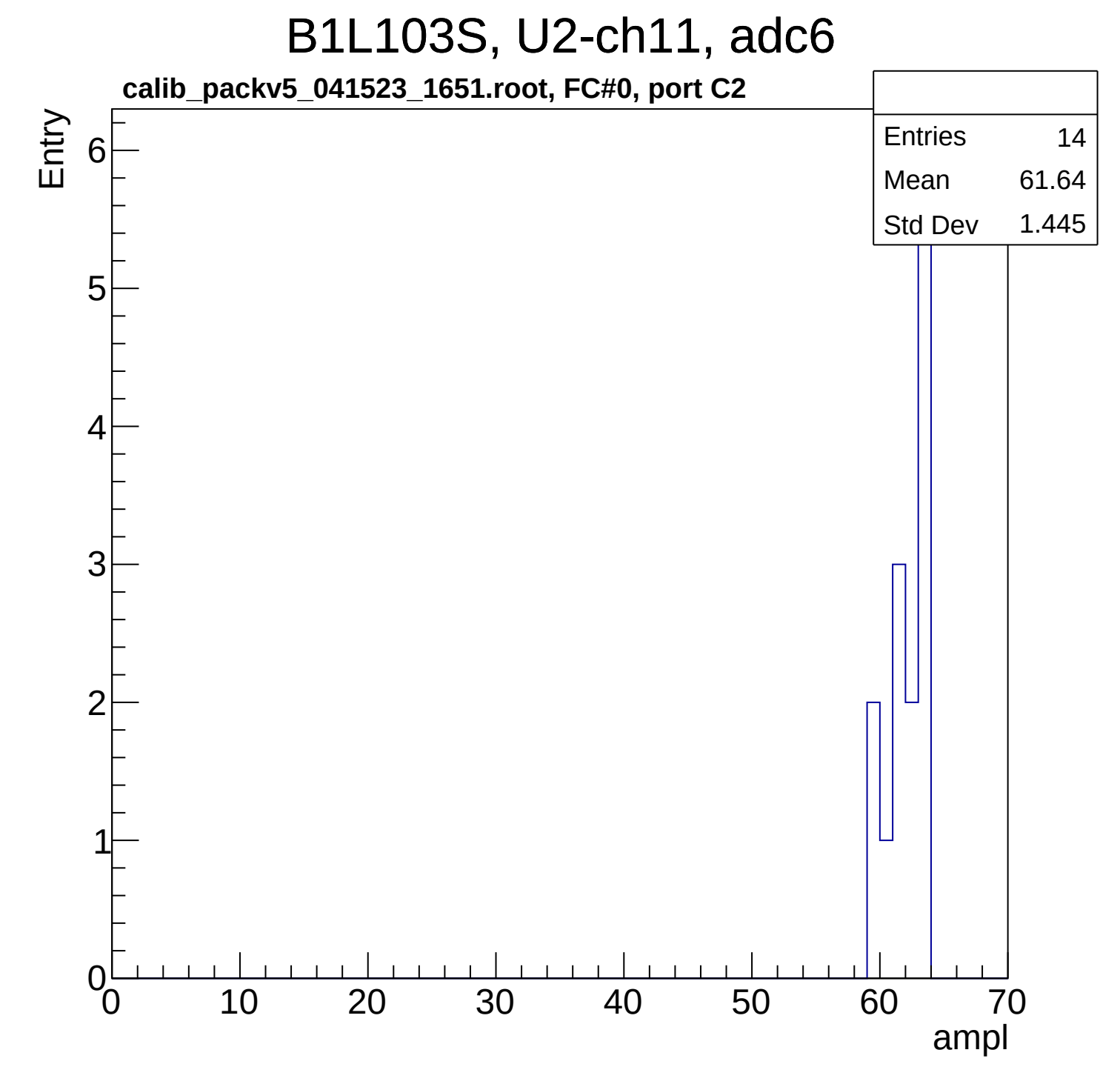

B1L103S, U2-ch11, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 31.22
Std Dev 9.33
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

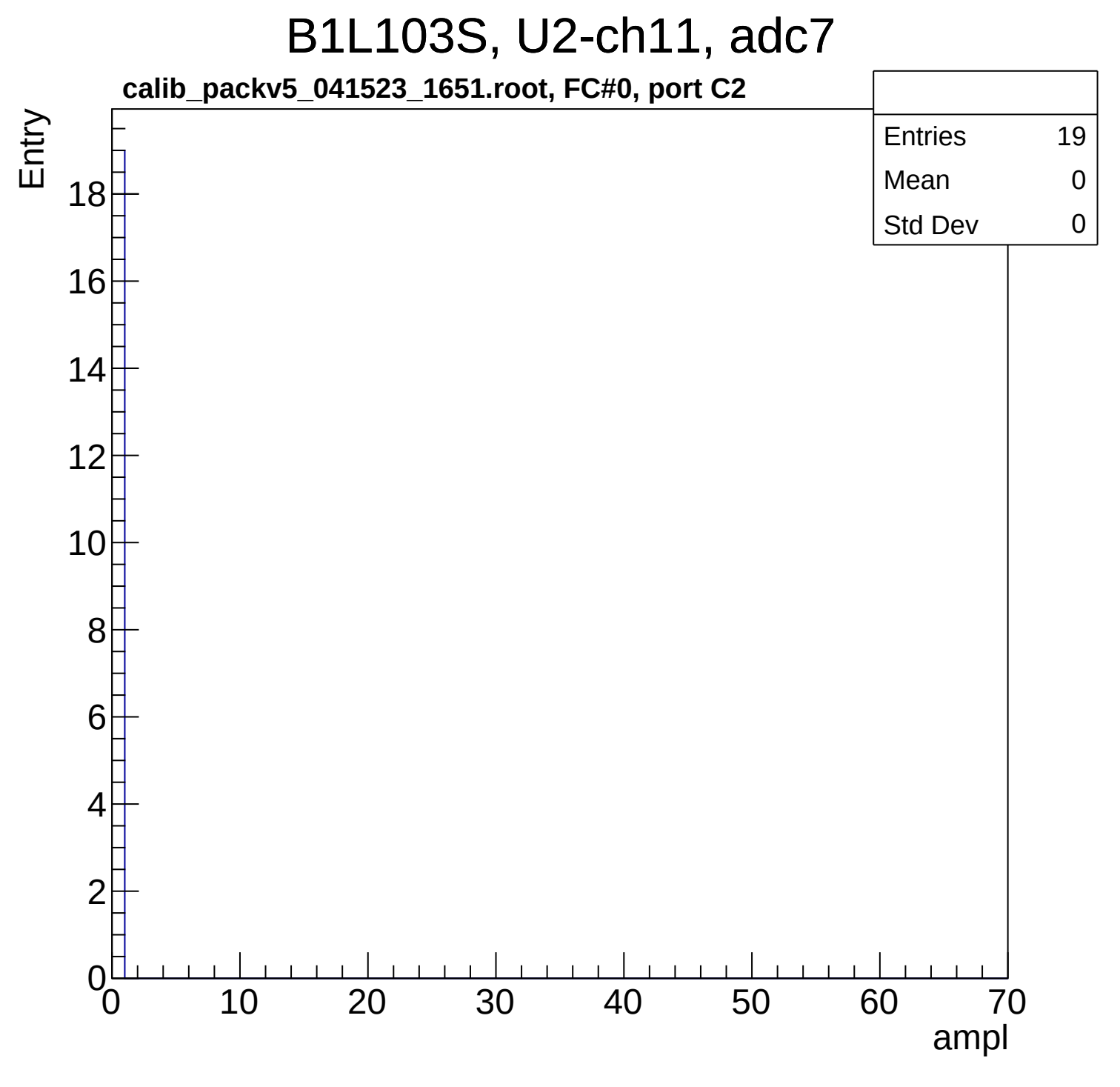

B1L103S, U2-ch11, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 38.36
Std Dev 10.69
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

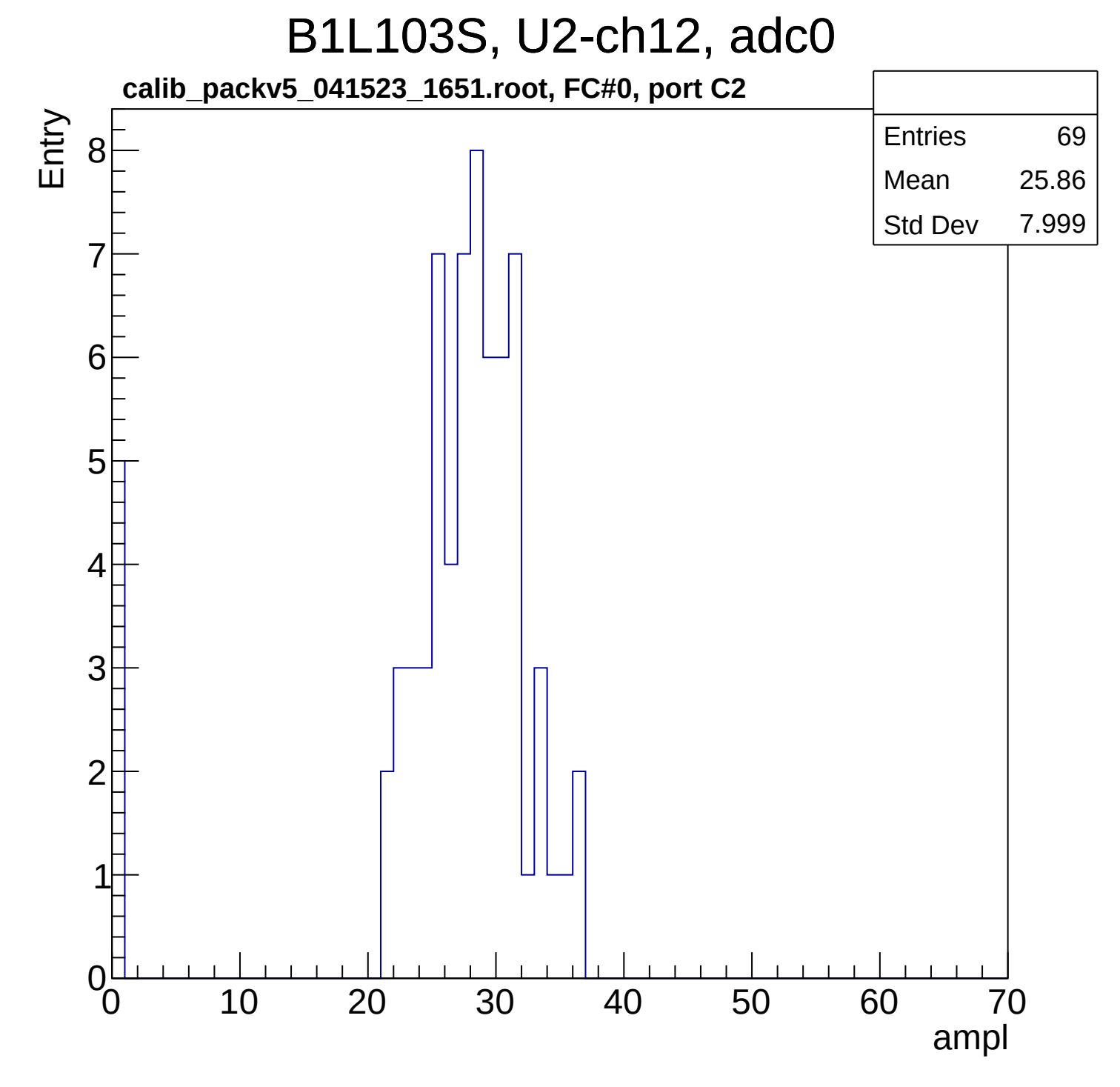

B1L103S, U2-ch11, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 47.32
Std Dev 6.452
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

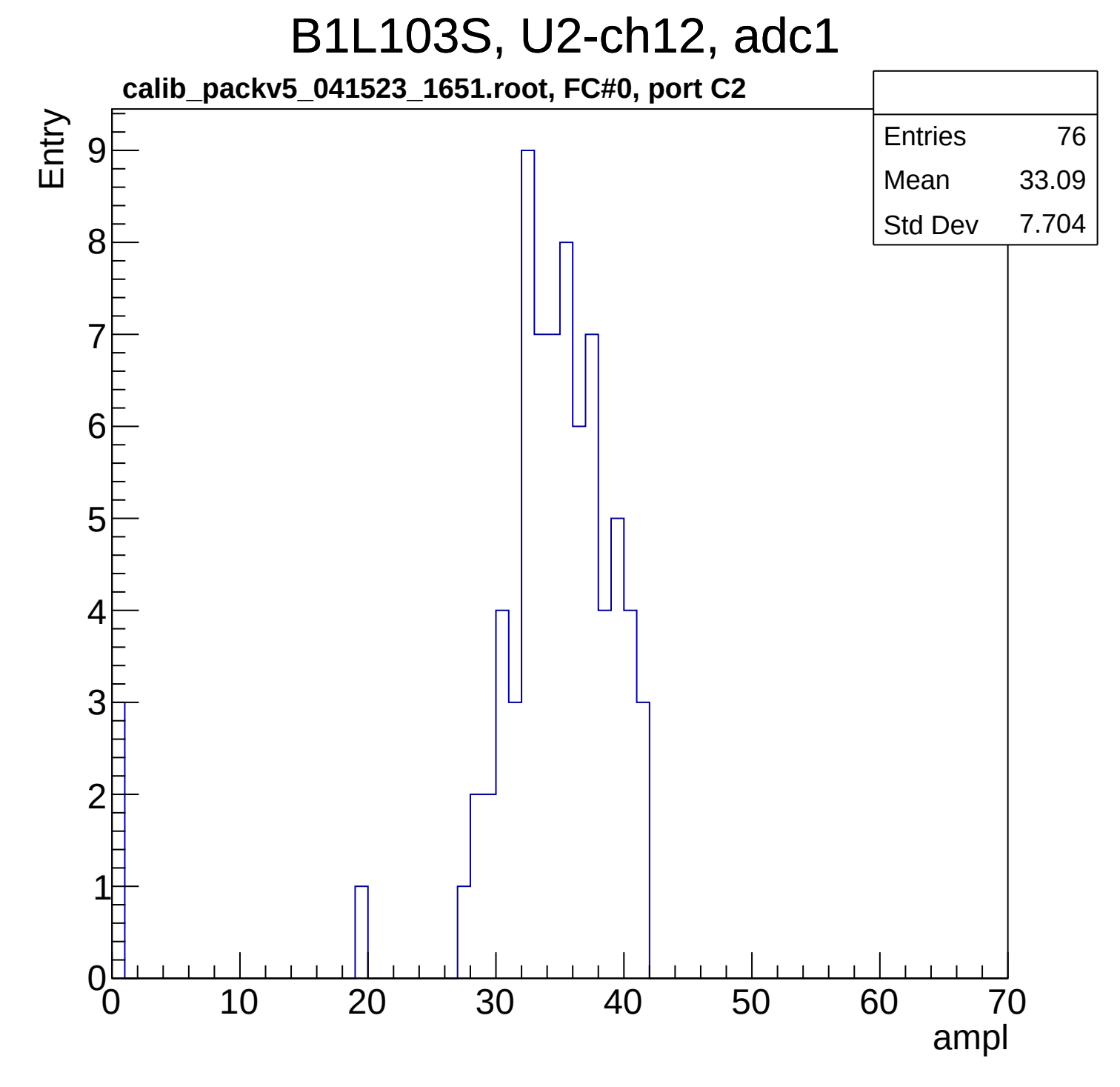

B1L103S, U2-ch11, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 54.7
Std Dev 3.168
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

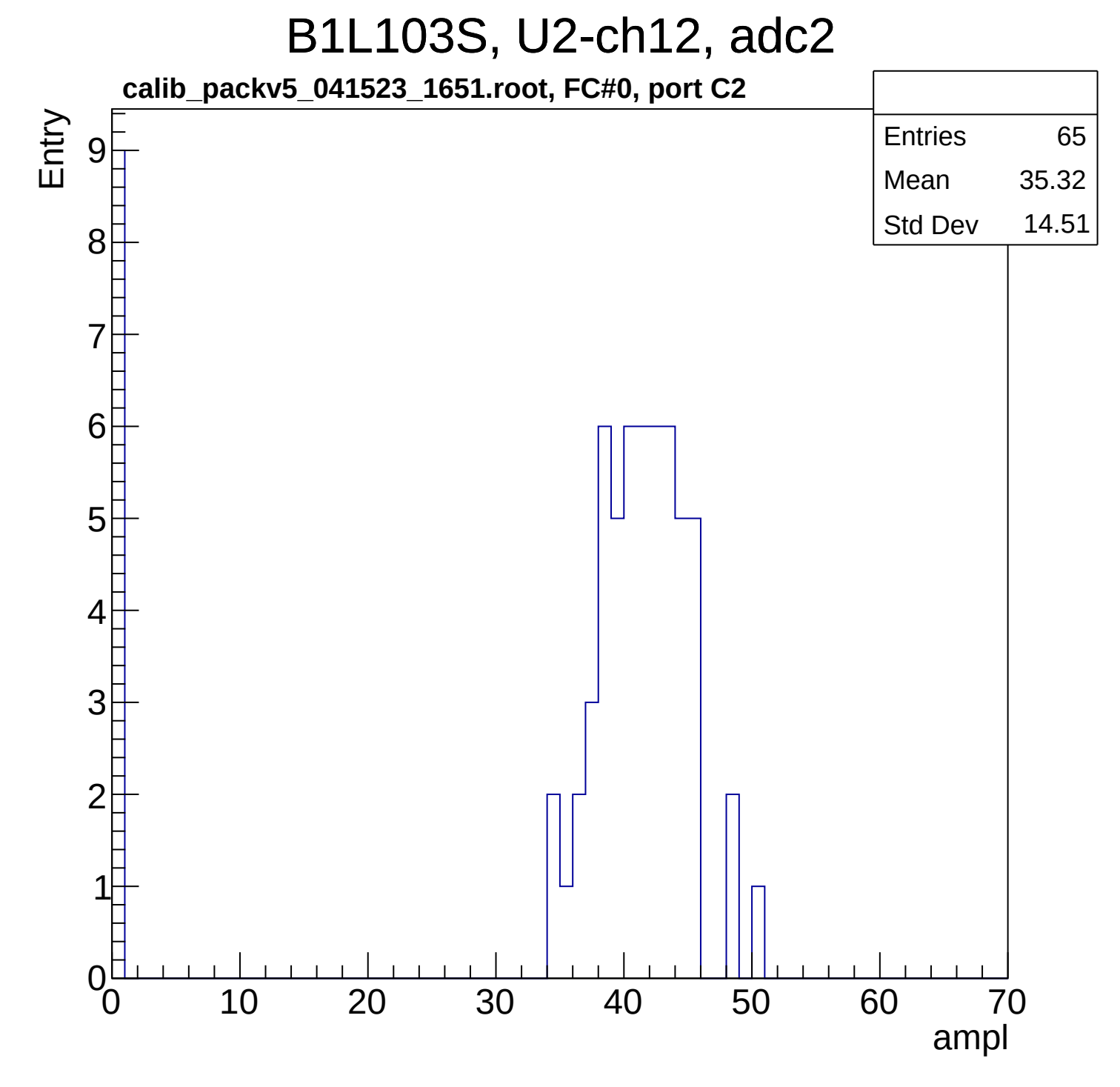

B1L103S, U2-ch11, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 57.47
Std Dev 8.112
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

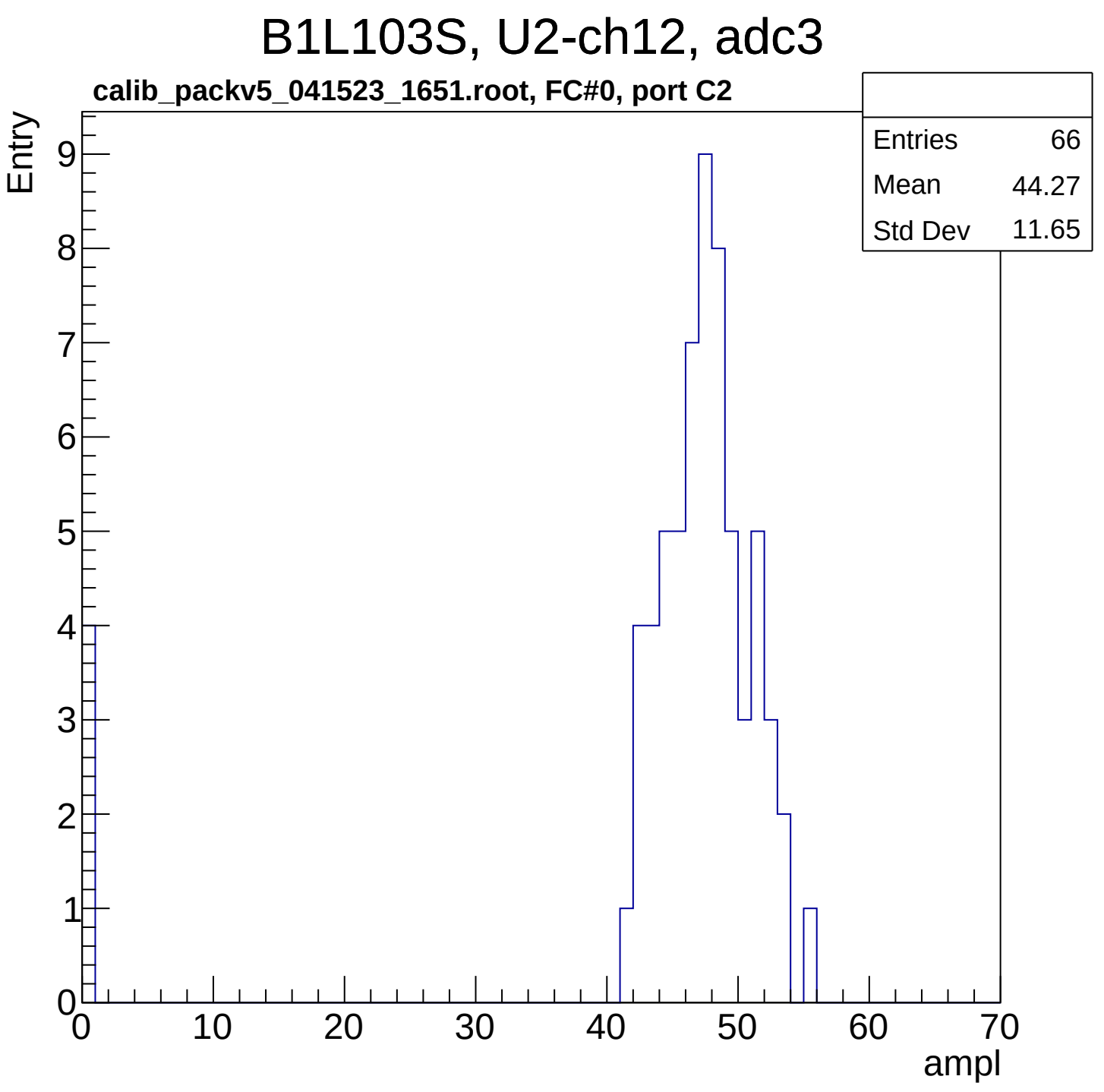

B1L103S, U2-ch11, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.64
Std Dev 1.445
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

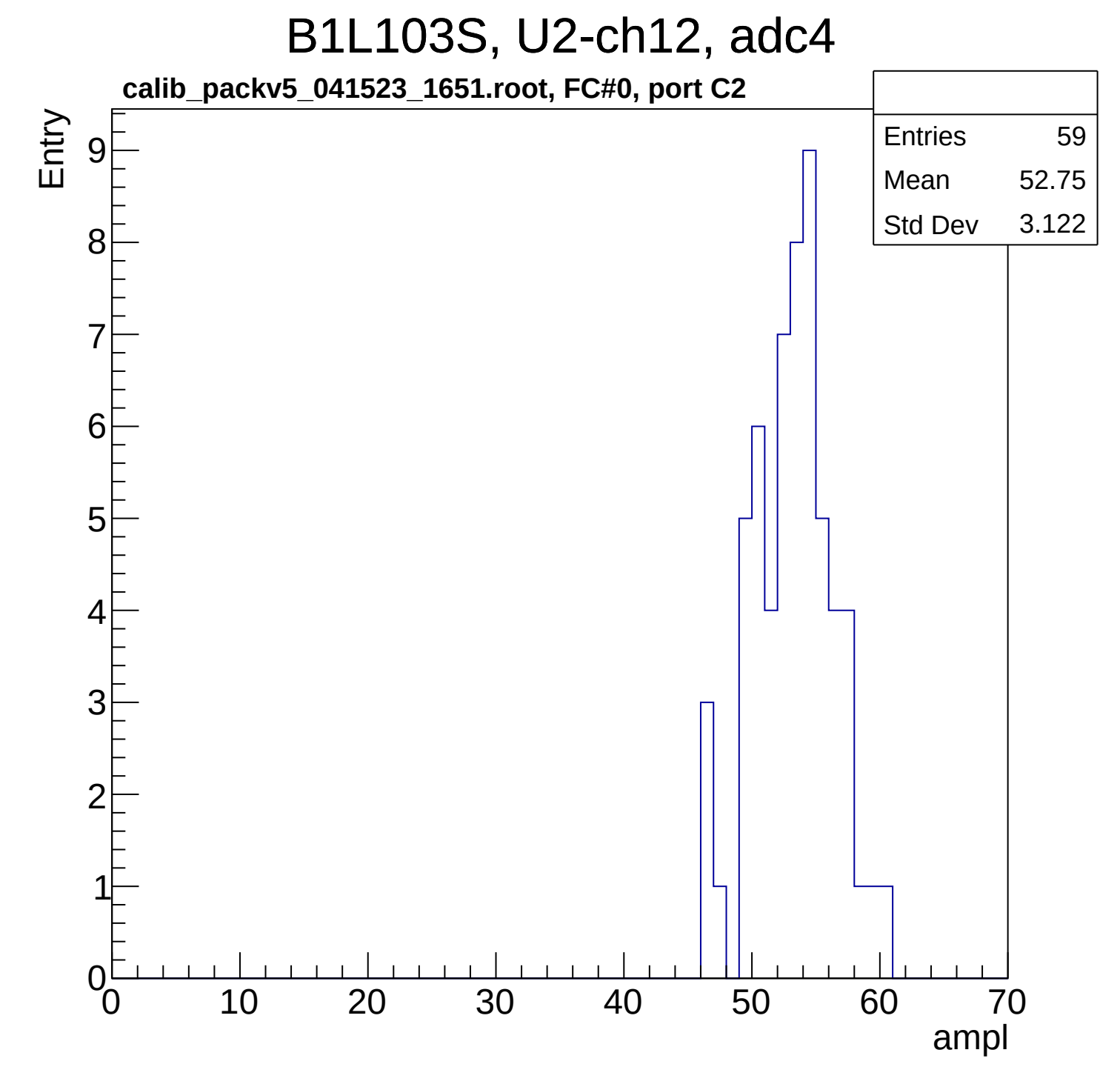

B1L103S, U2-ch11, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

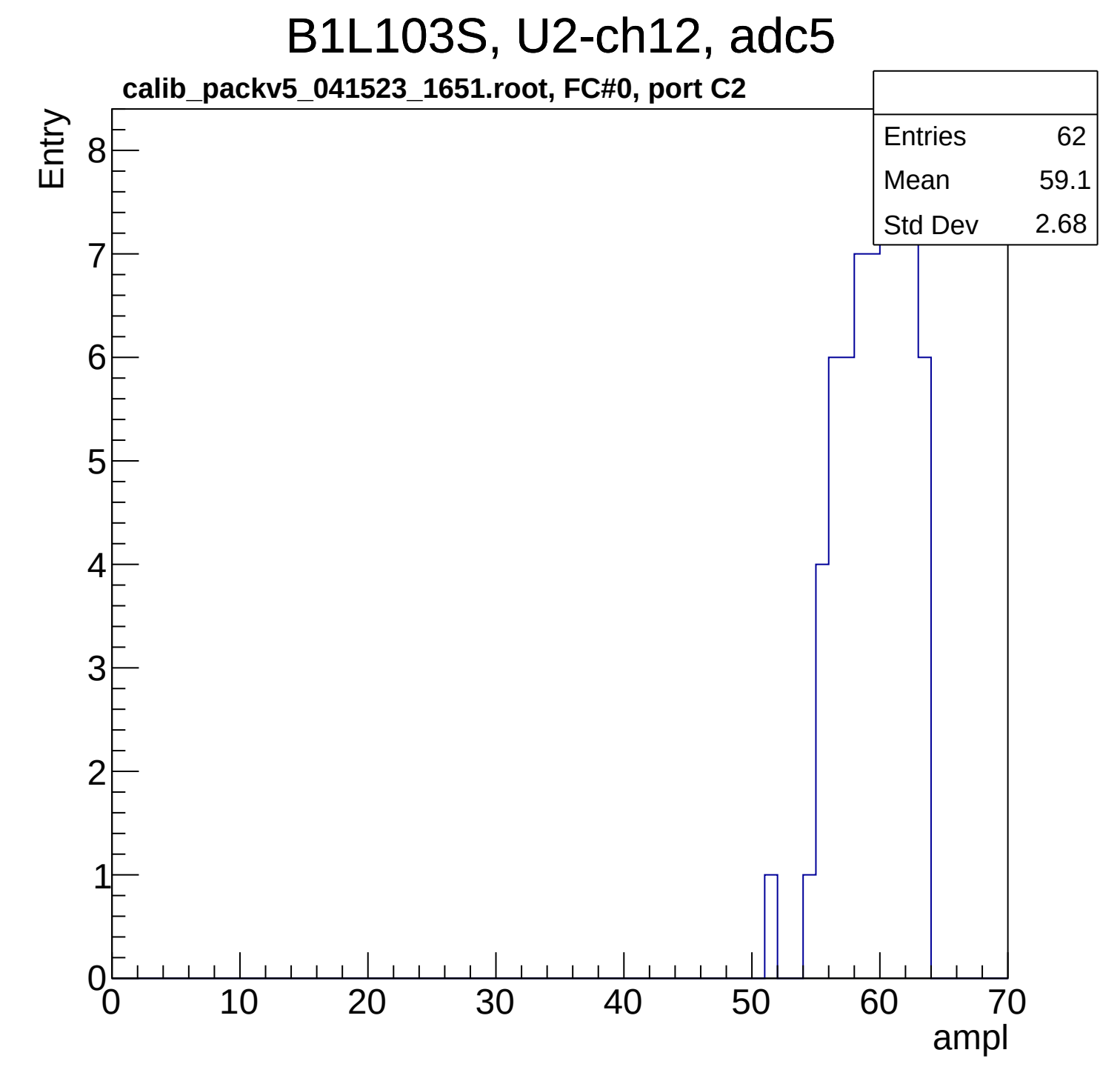

B1L103S, U2-ch12, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 25.86
Std Dev 7.999
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

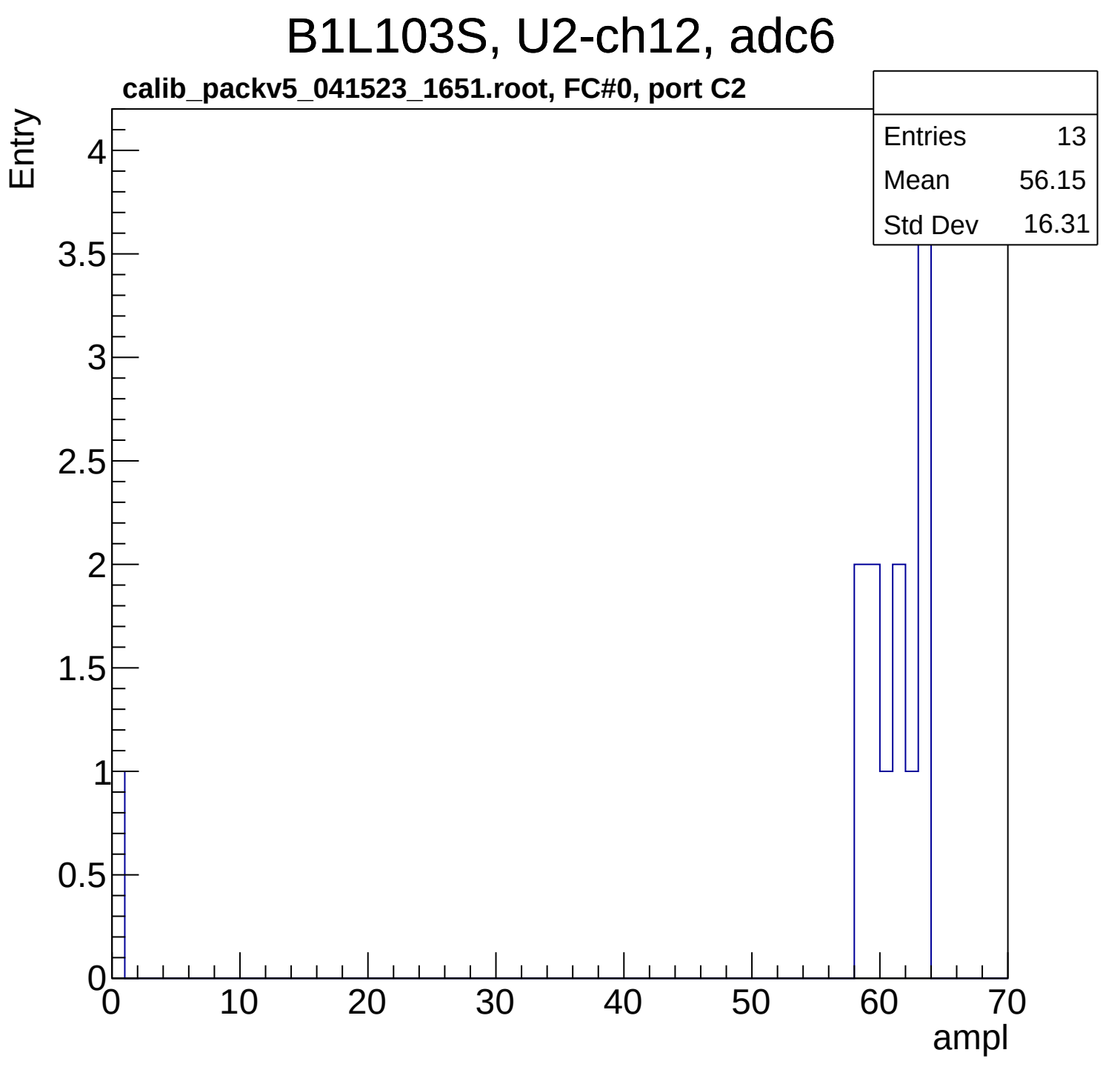

B1L103S, U2-ch12, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 33.09
Std Dev 7.704
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

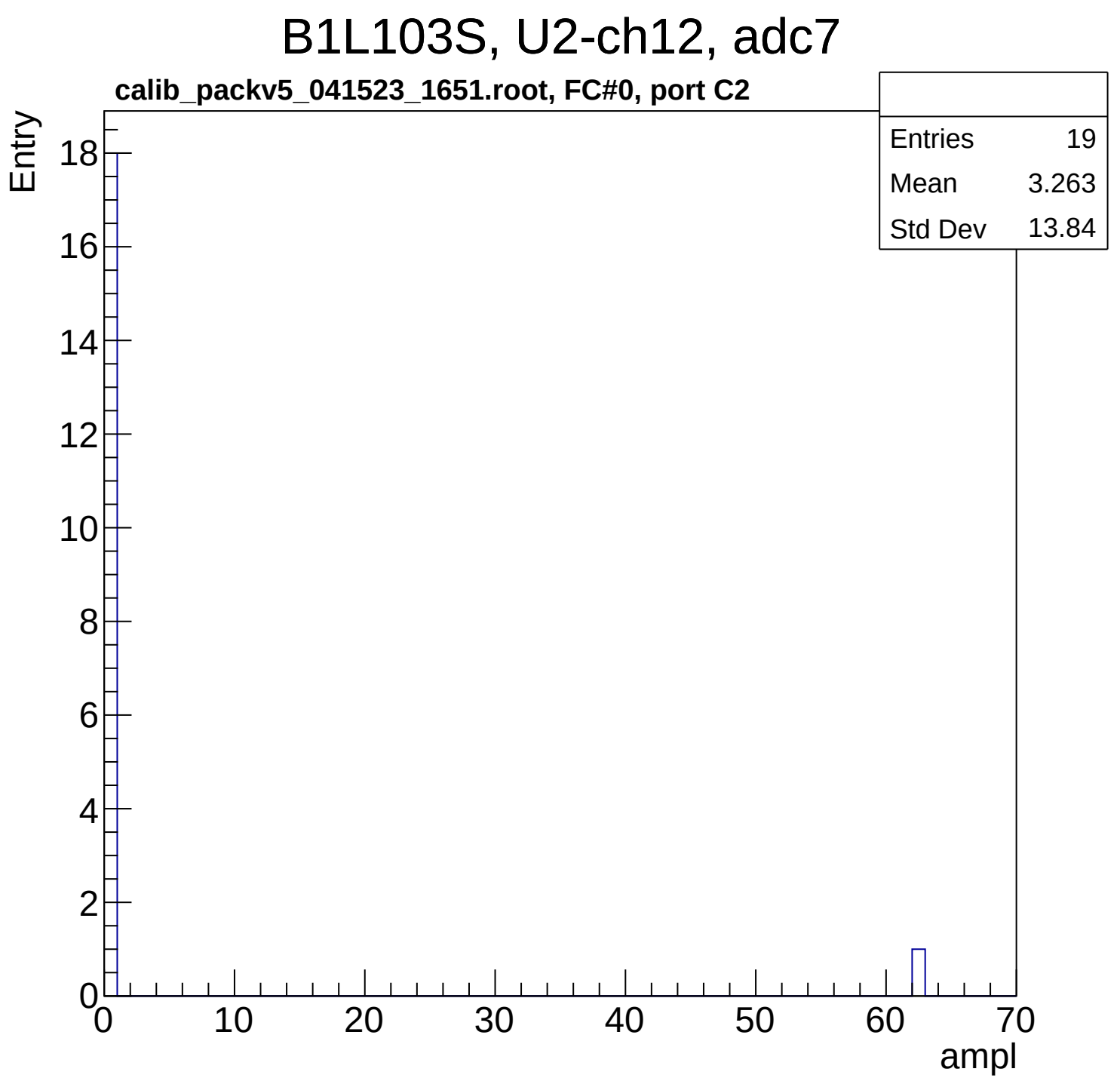

B1L103S, U2-ch12, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 35.32
Std Dev 14.51
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

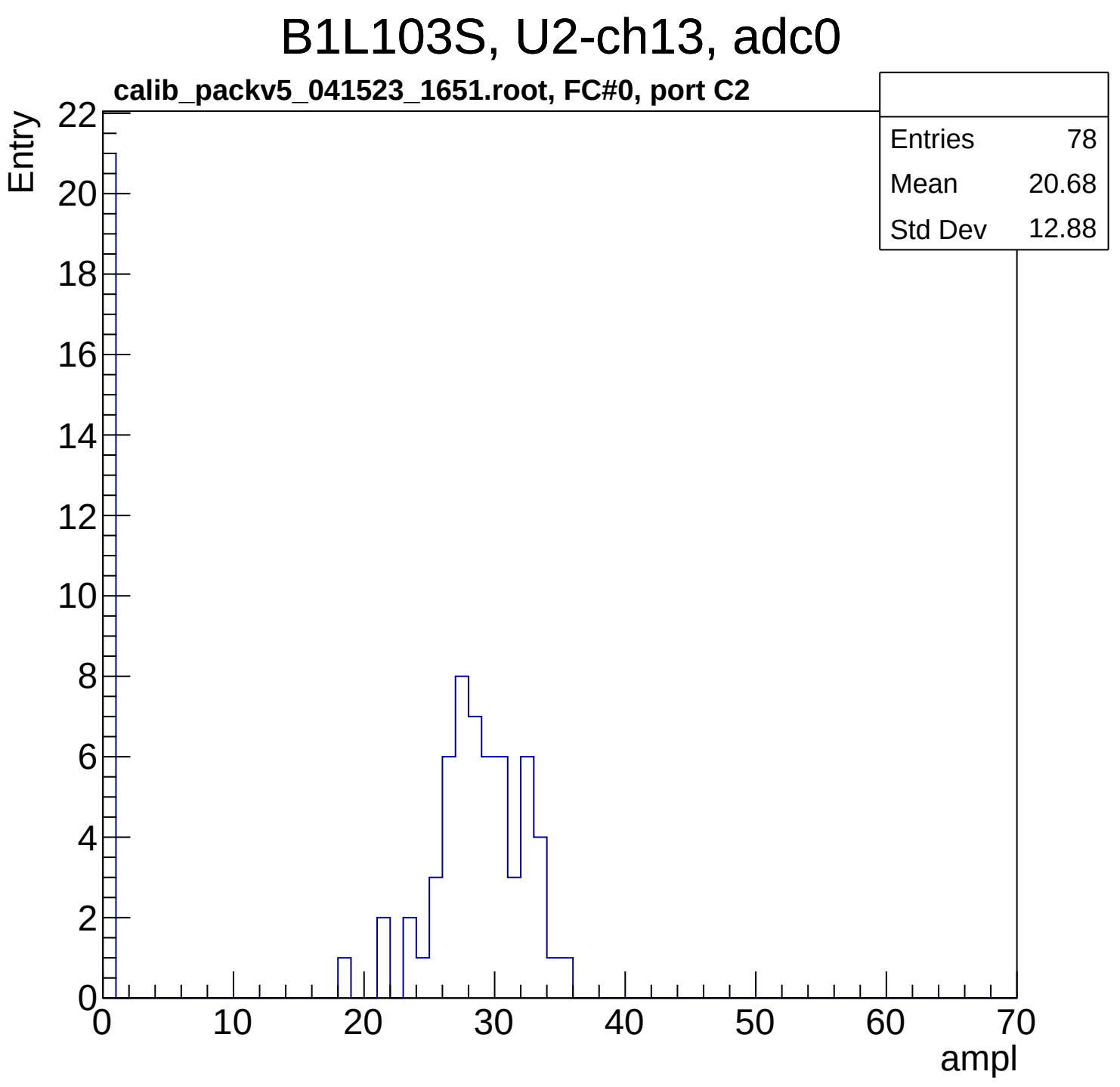

B1L103S, U2-ch12, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 44.27
Std Dev 11.65
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

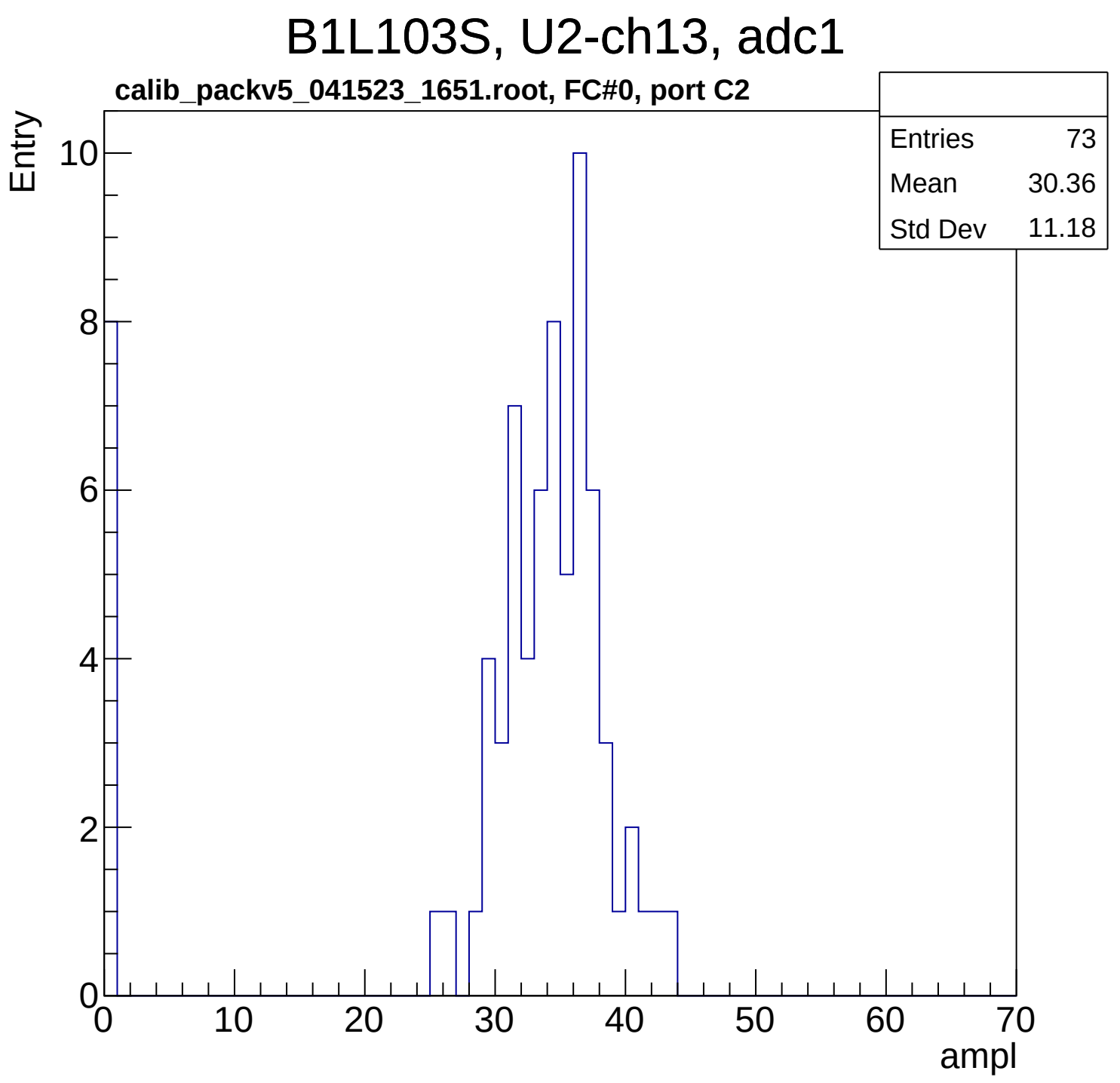

B1L103S, U2-ch12, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 52.75
Std Dev 3.122
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

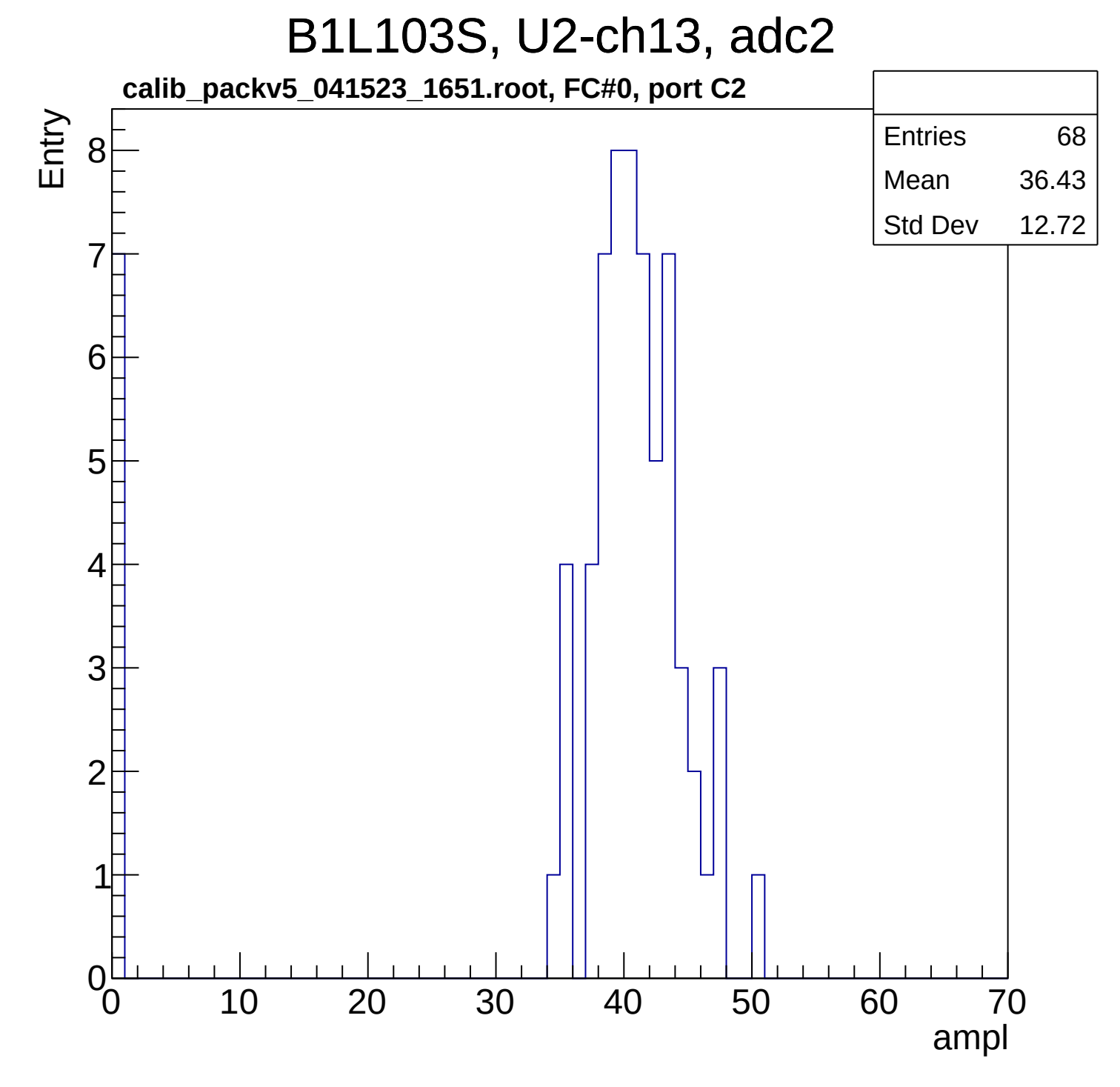

B1L103S, U2-ch12, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 59.1
Std Dev 2.68
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

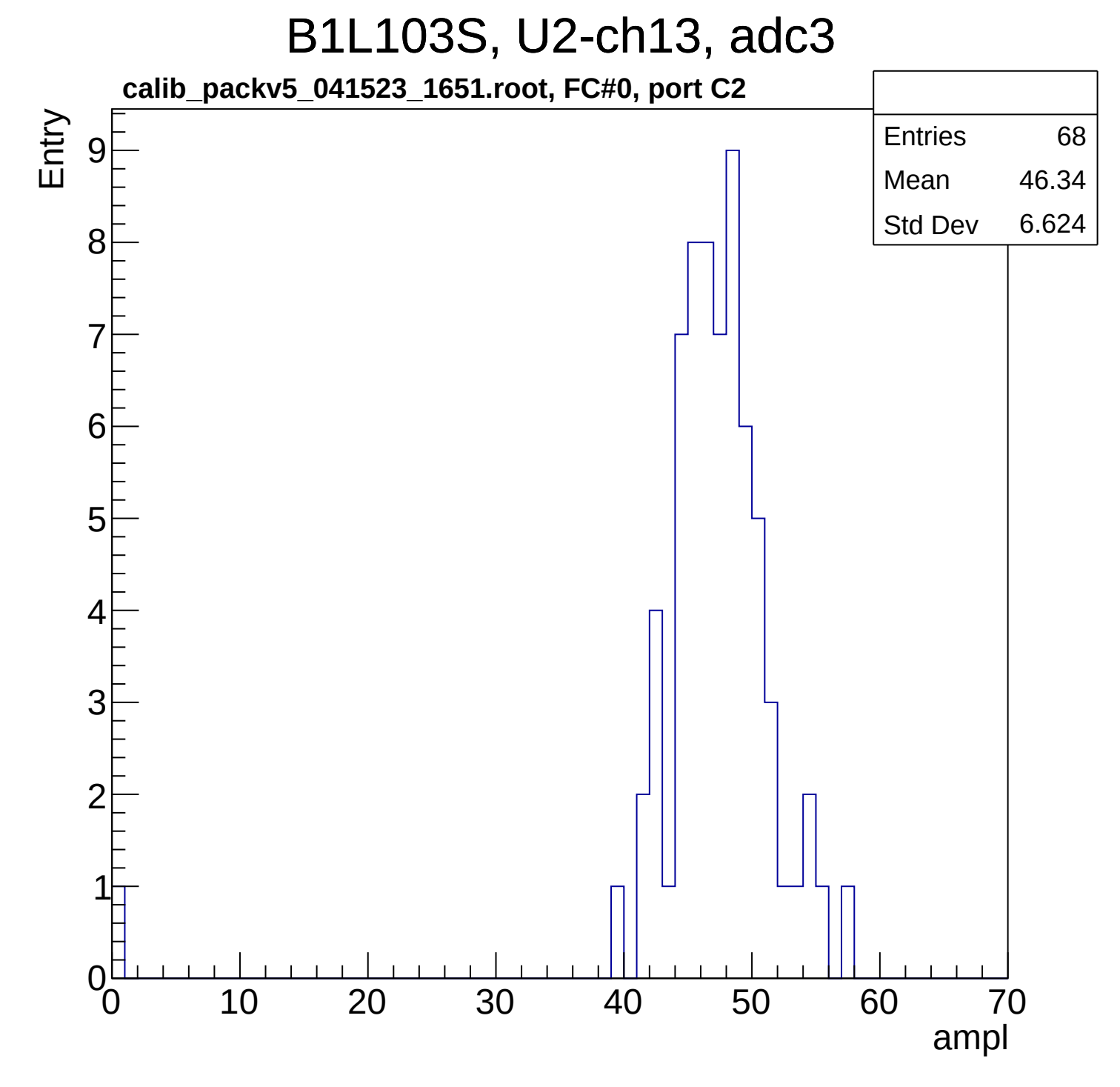

B1L103S, U2-ch12, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 56.15
Std Dev 16.31
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

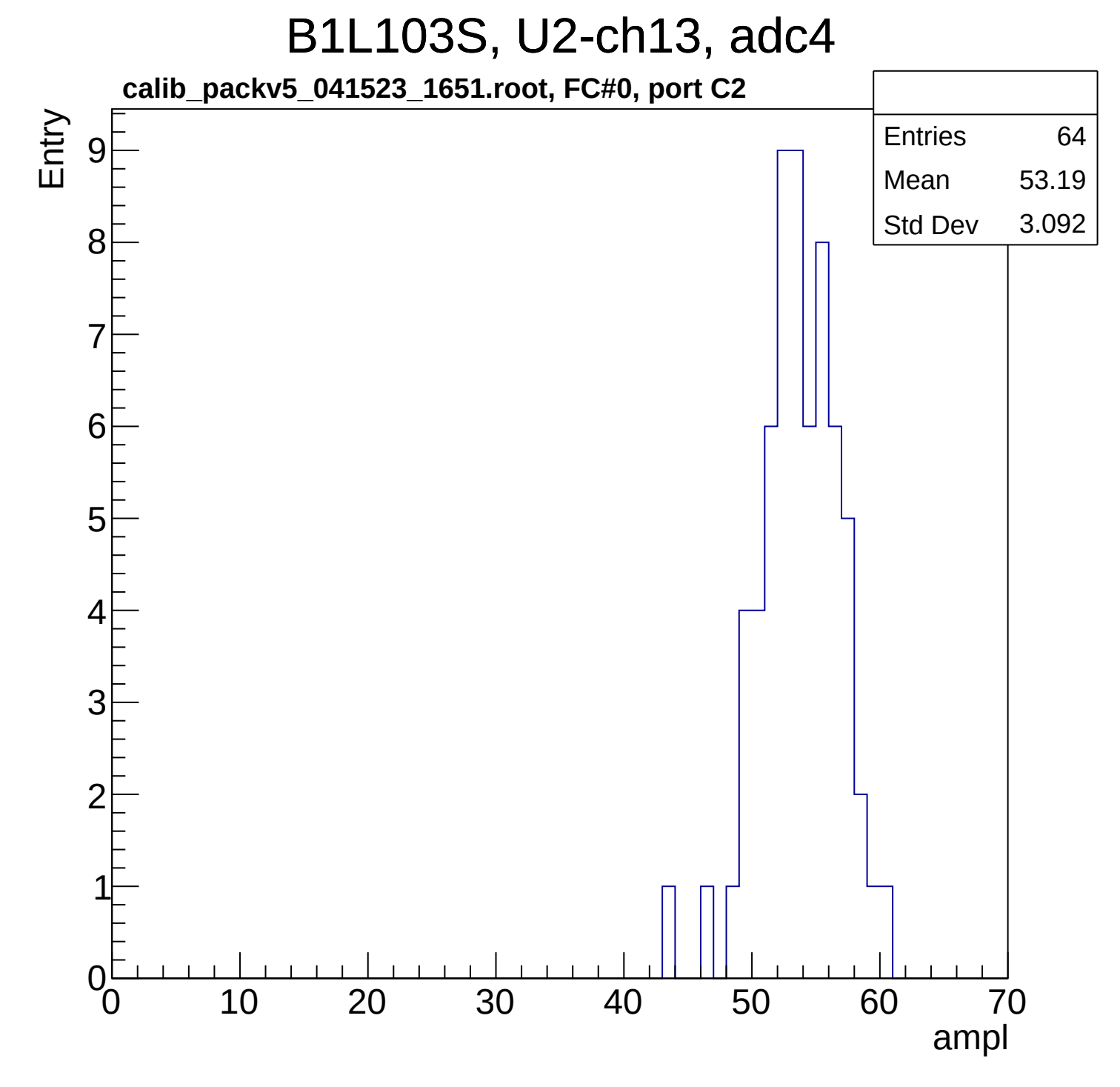

B1L103S, U2-ch12, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.263
Std Dev 13.84
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

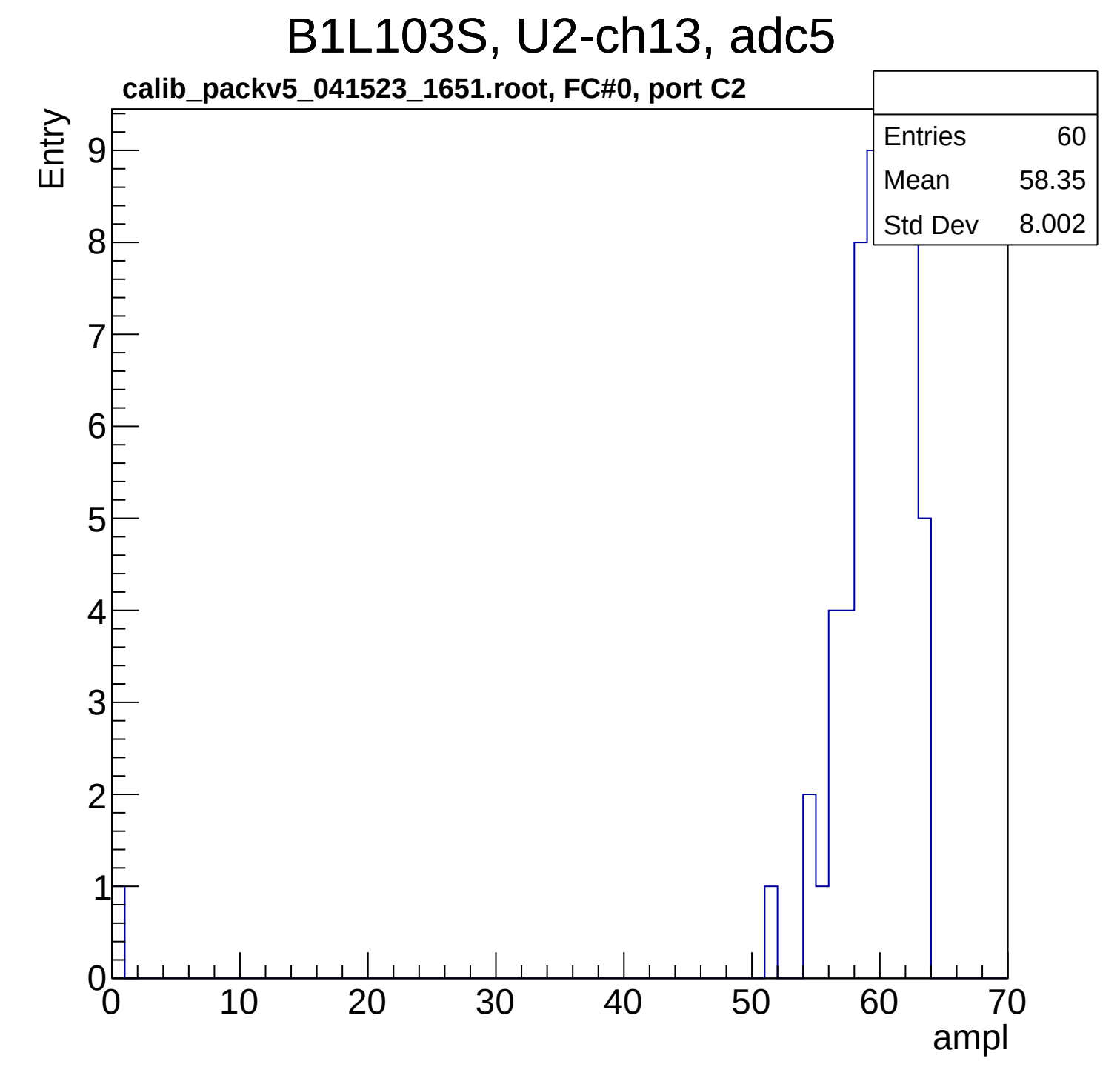

B1L103S, U2-ch13, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 20.68
Std Dev 12.88
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70

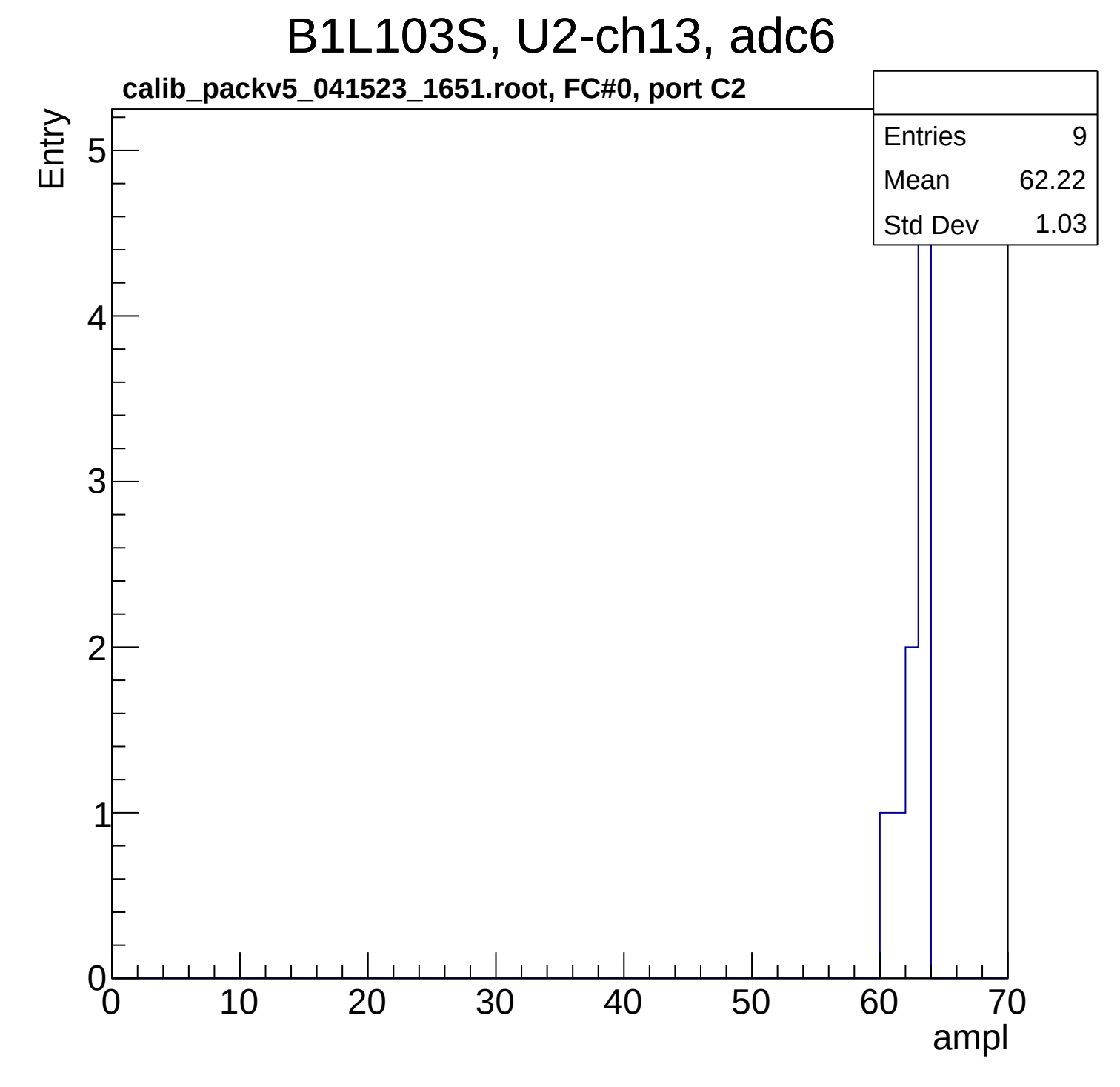

B1L103S, U2-ch13, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 30.36
Std Dev 11.18
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

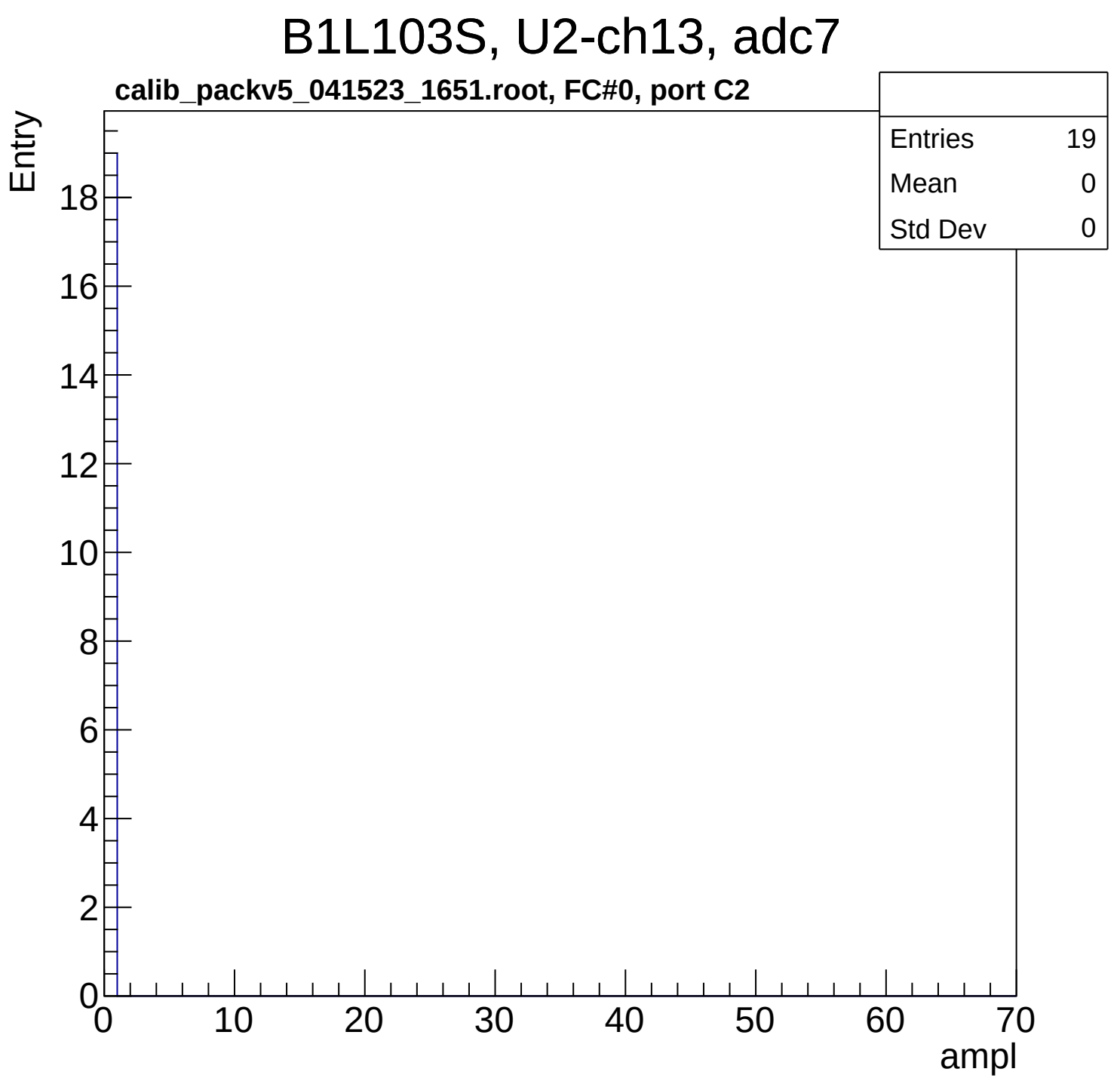

B1L103S, U2-ch13, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 36.43
Std Dev 12.72
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

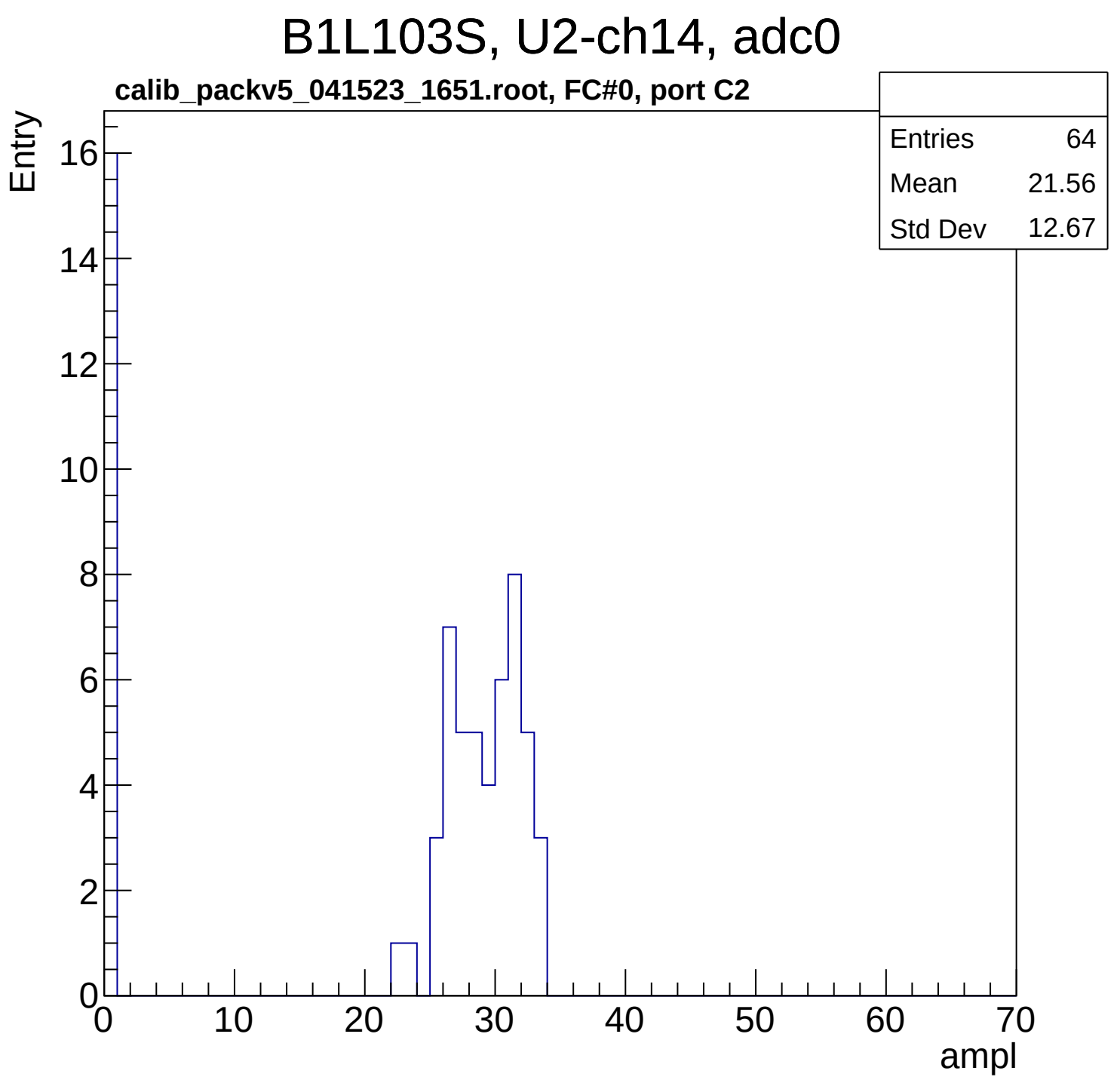

B1L103S, U2-ch13, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 46.34
Std Dev 6.624
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

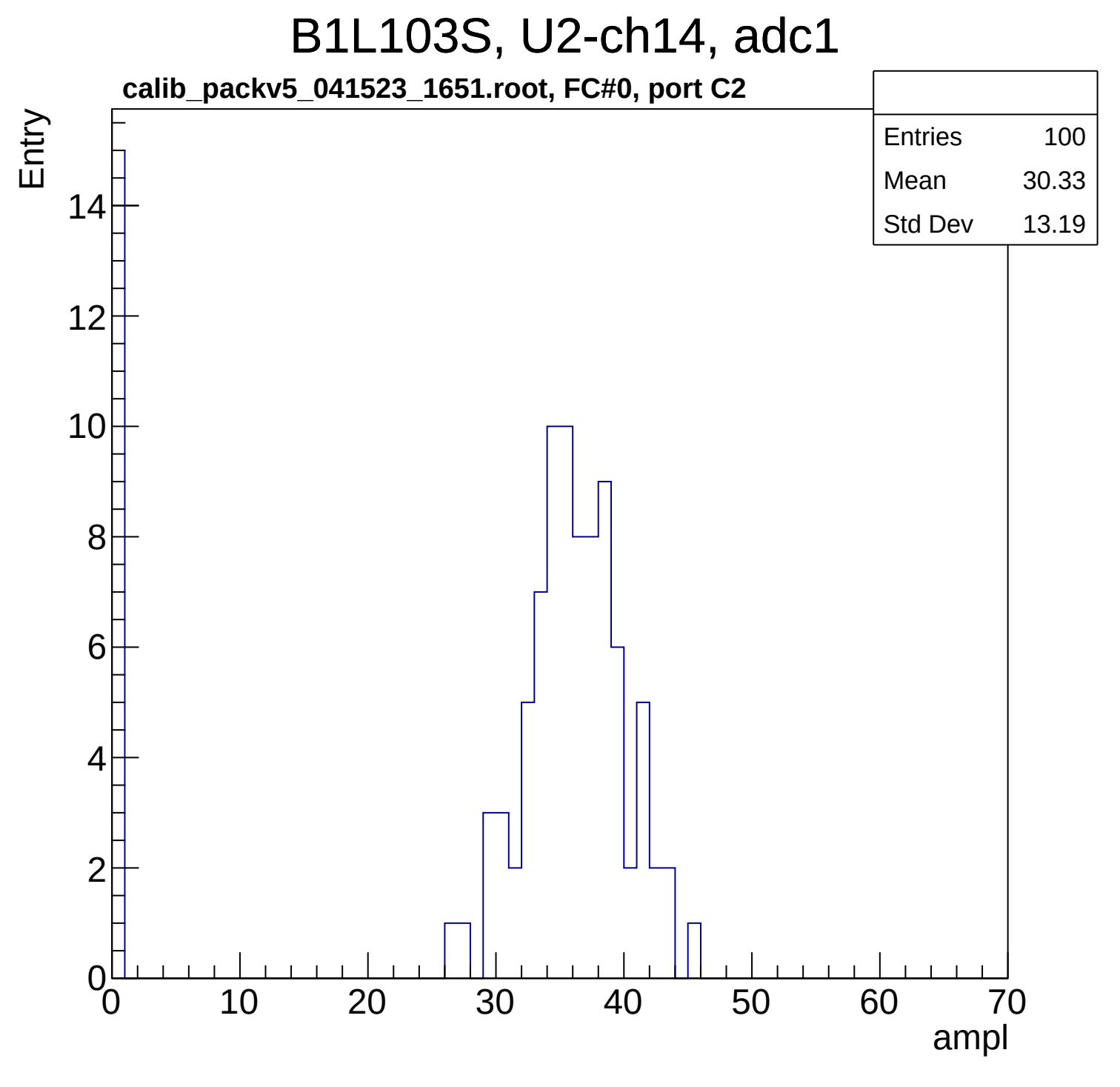

B1L103S, U2-ch13, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 53.19
Std Dev 3.092
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

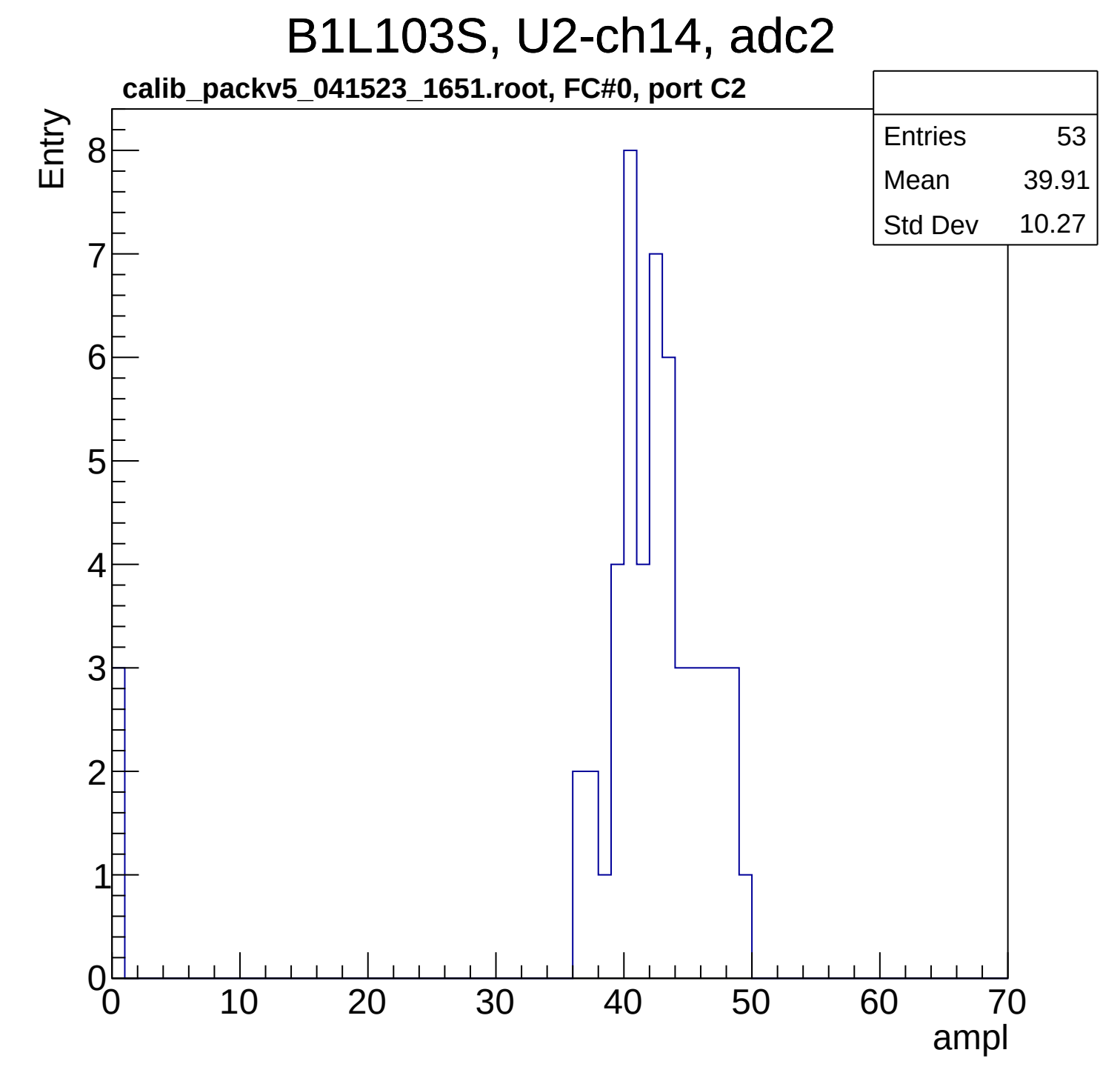

B1L103S, U2-ch13, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 58.35
Std Dev 8.002
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

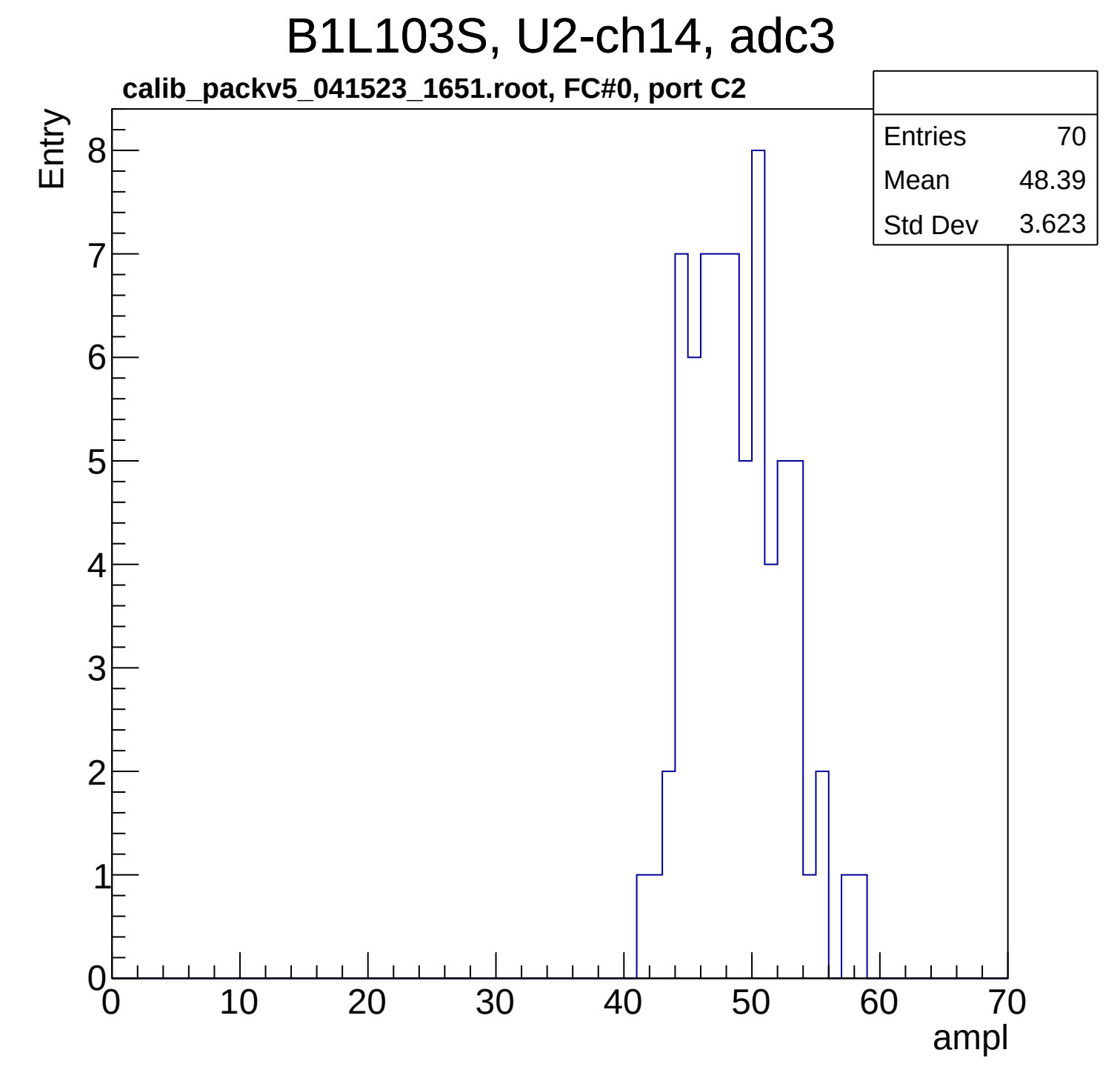

B1L103S, U2-ch13, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 62.22
Std Dev 1.03
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

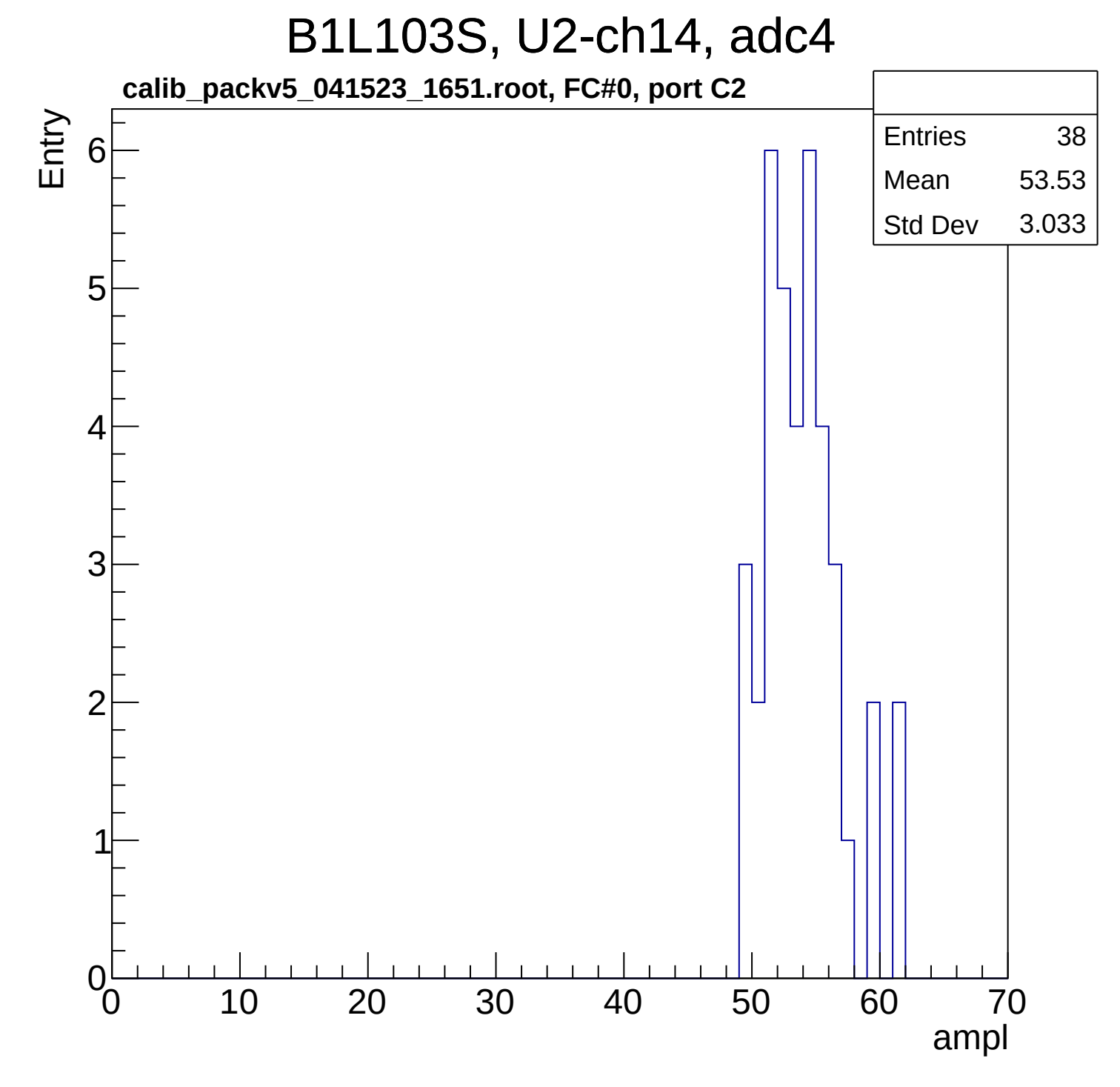

B1L103S, U2-ch13, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

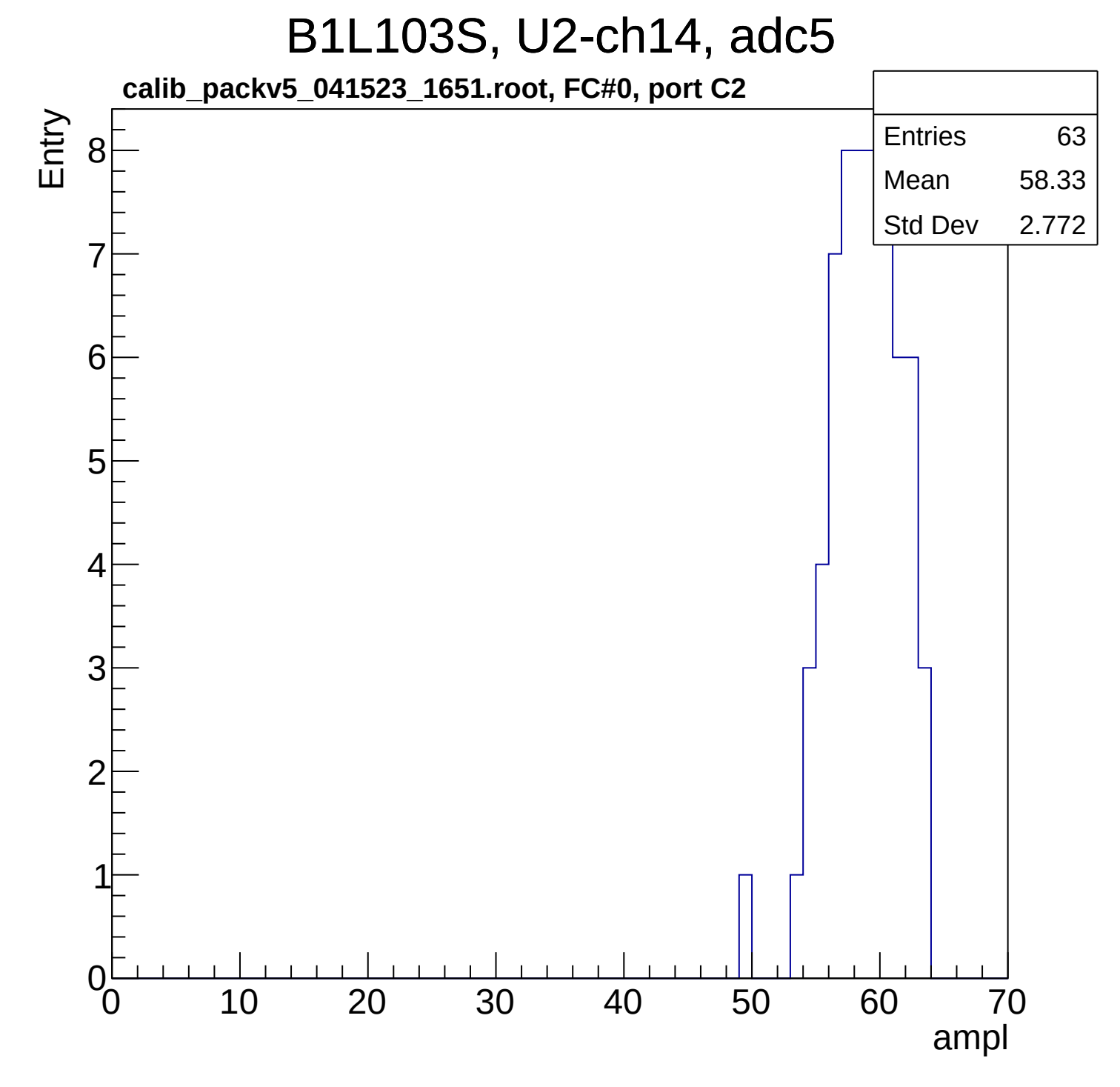

B1L103S, U2-ch14, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 21.56
Std Dev 12.67
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

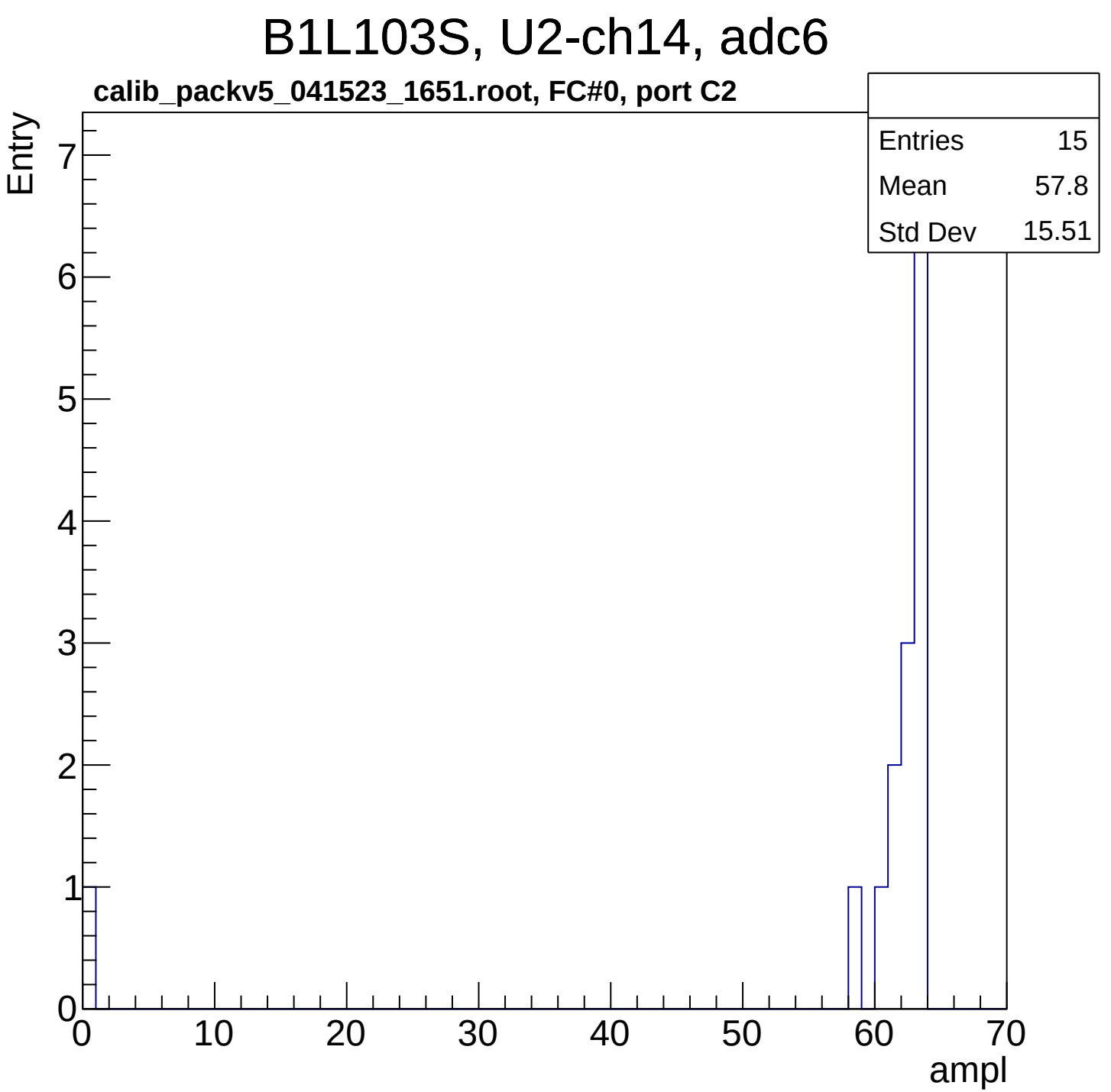

B1L103S, U2-ch14, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 30.33
Std Dev 13.19
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

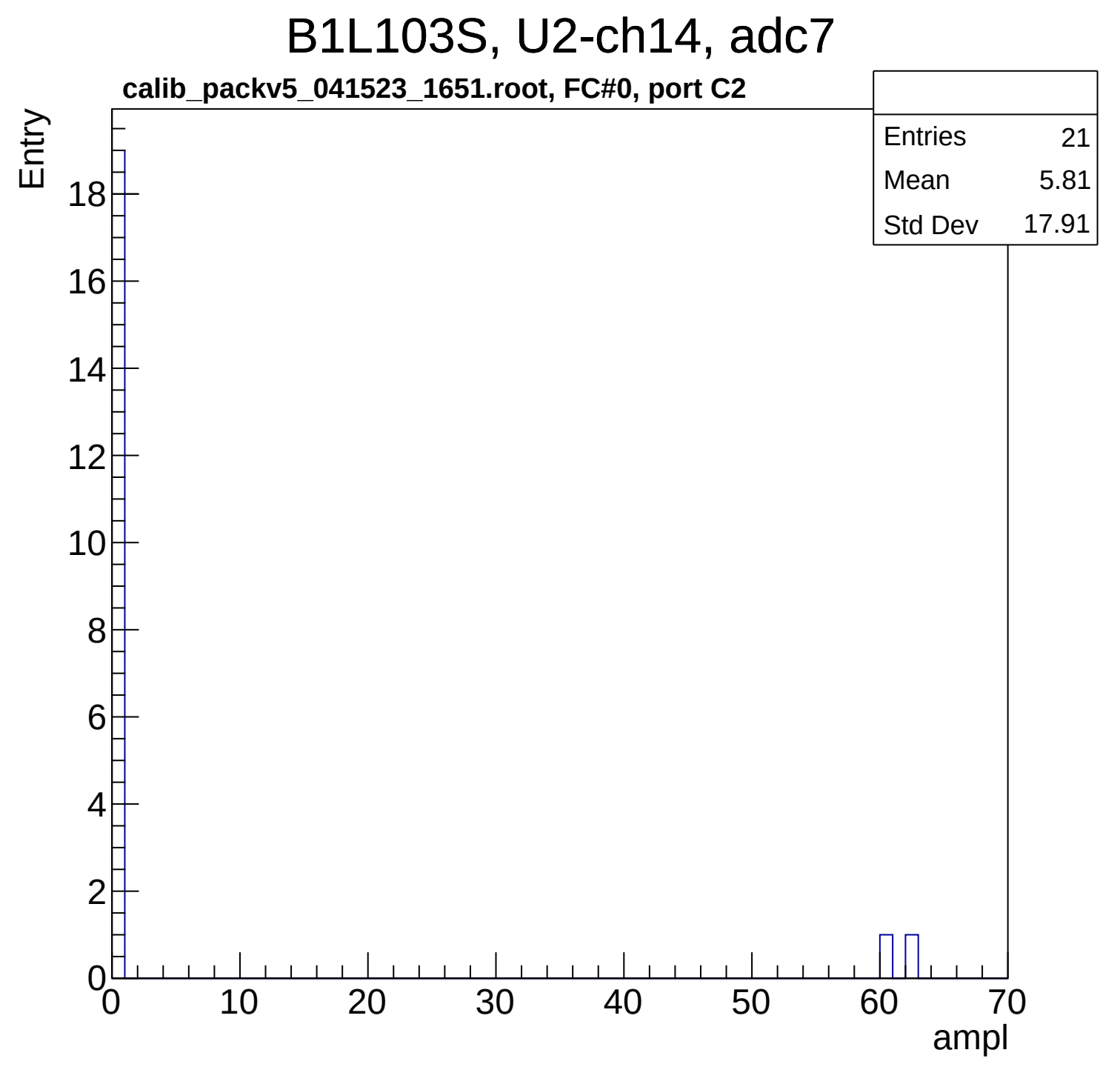

B1L103S, U2-ch14, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 39.91
Std Dev 10.27
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

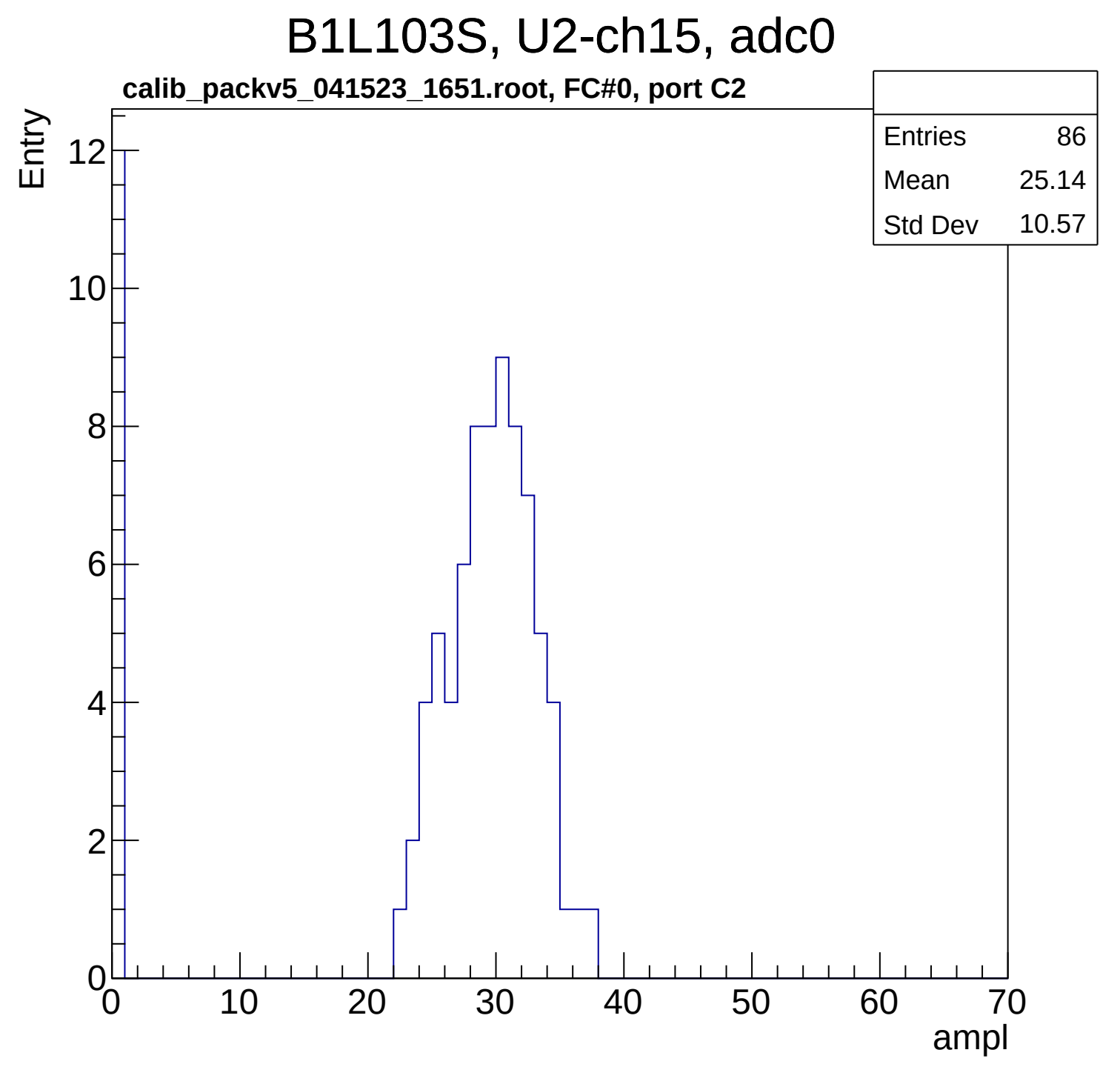

B1L103S, U2-ch14, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 48.39
Std Dev 3.623
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

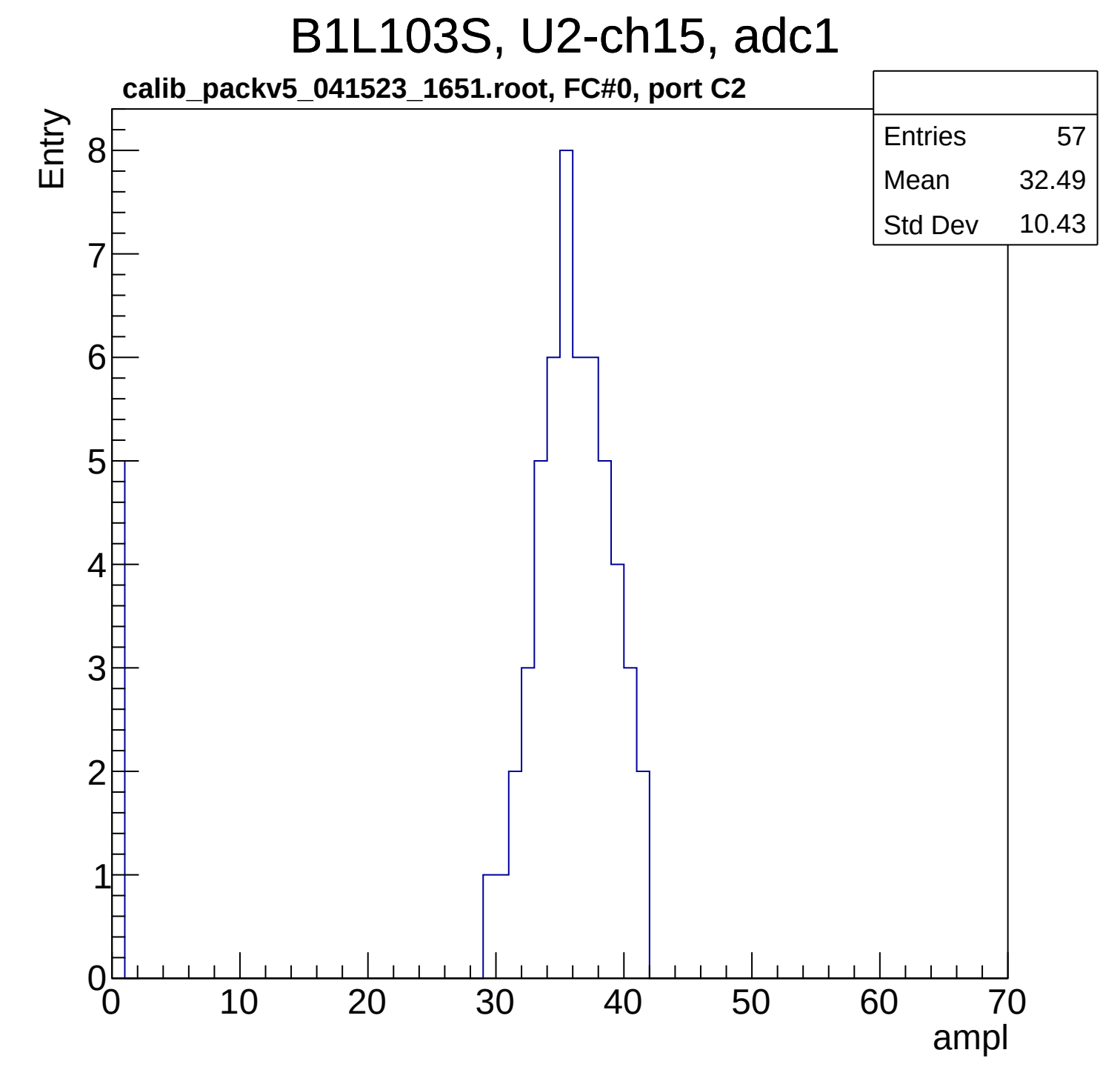

B1L103S, U2-ch14, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 53.53
Std Dev 3.033
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

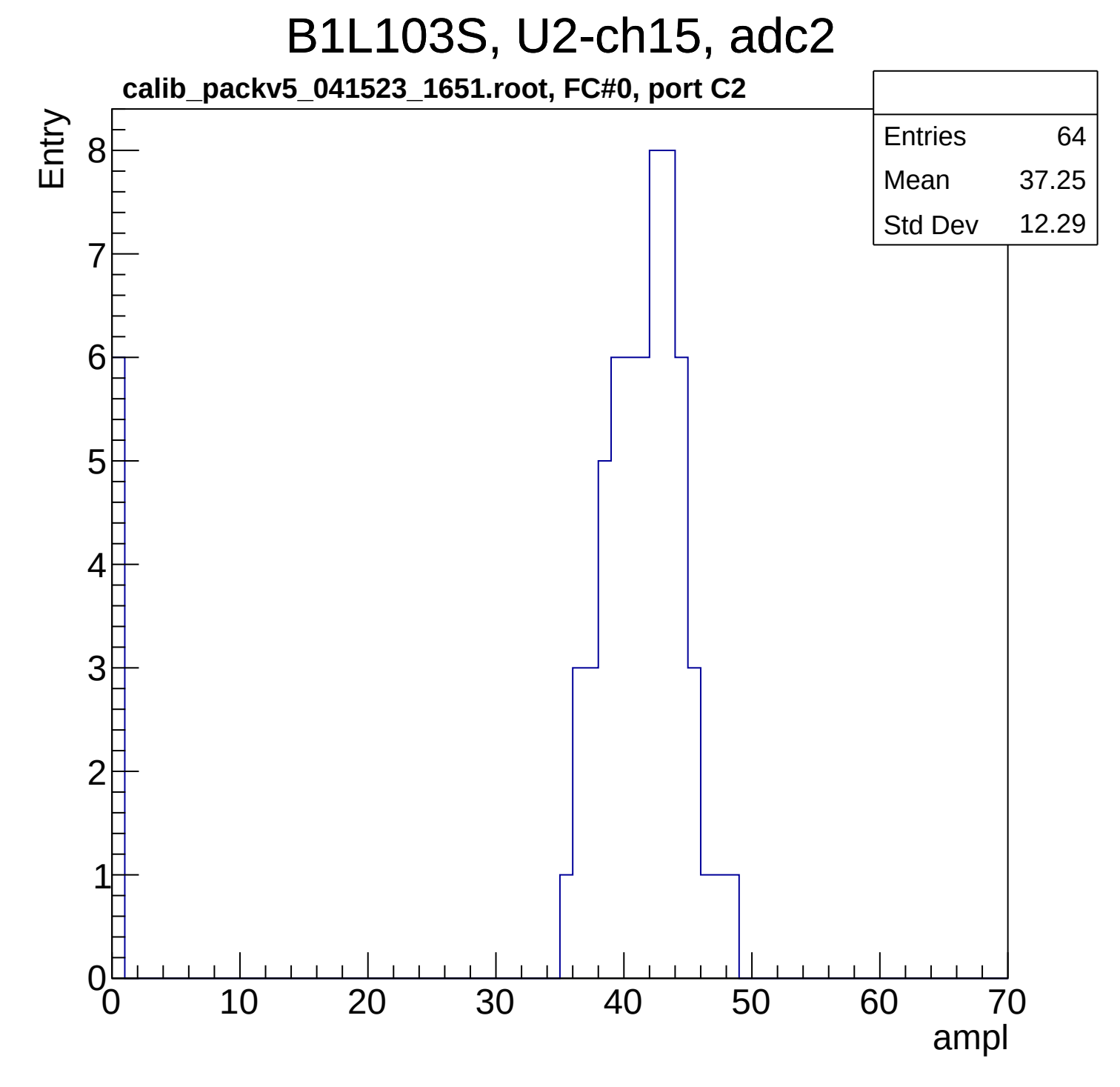

B1L103S, U2-ch14, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 58.33
Std Dev 2.772
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

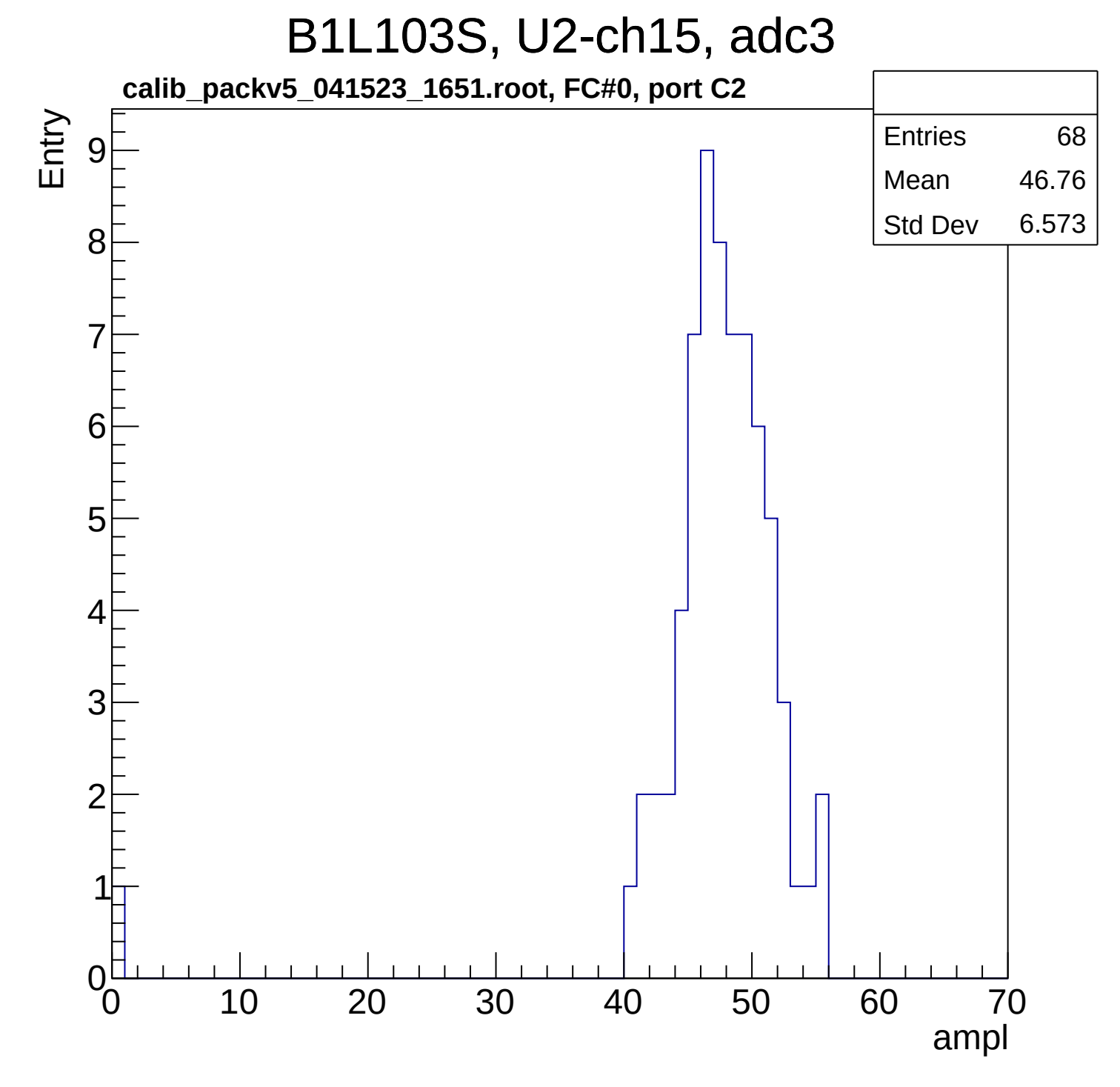

B1L103S, U2-ch14, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.8
Std Dev 15.51
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

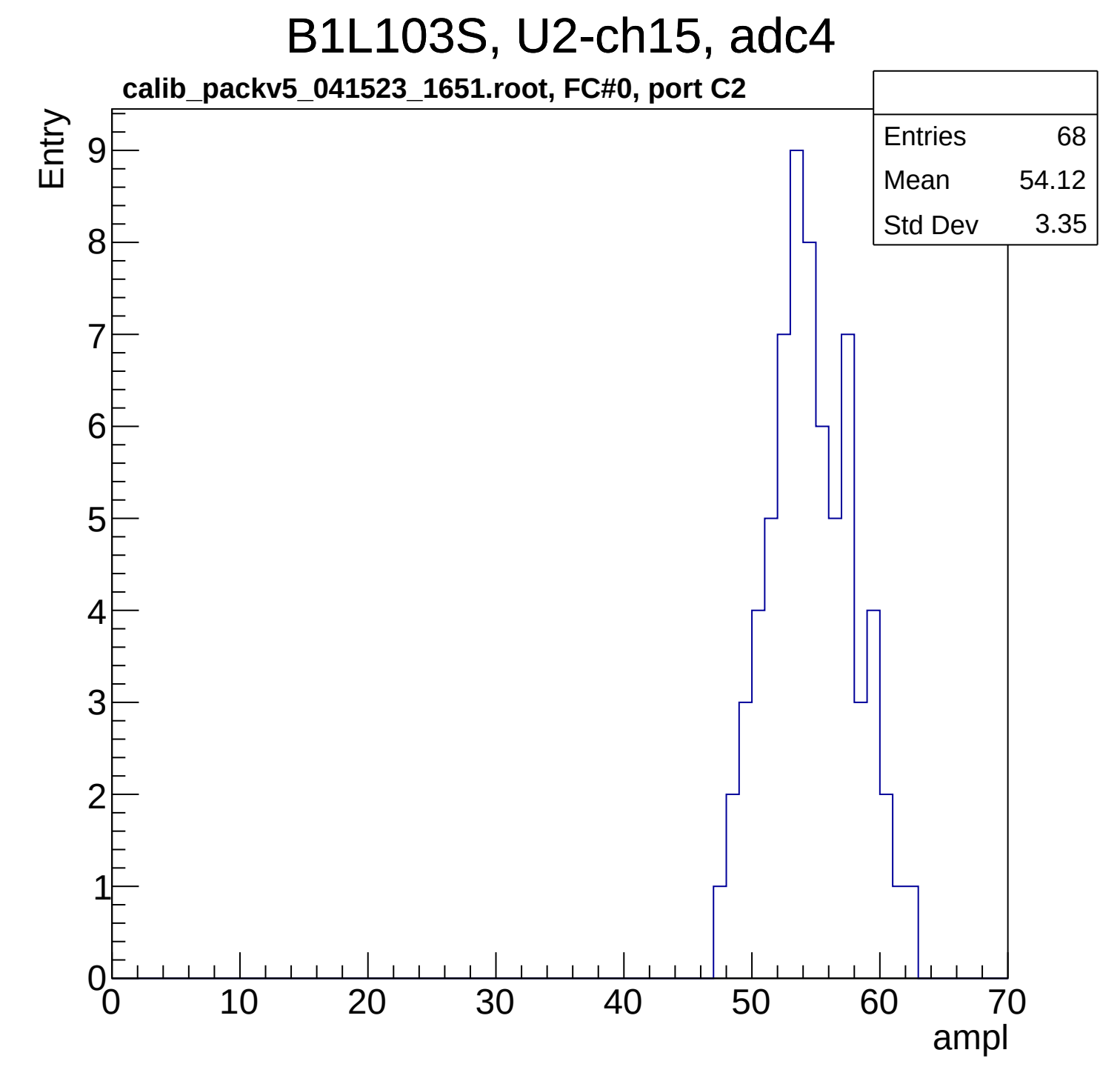

B1L103S, U2-ch14, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.81
Std Dev 17.91
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

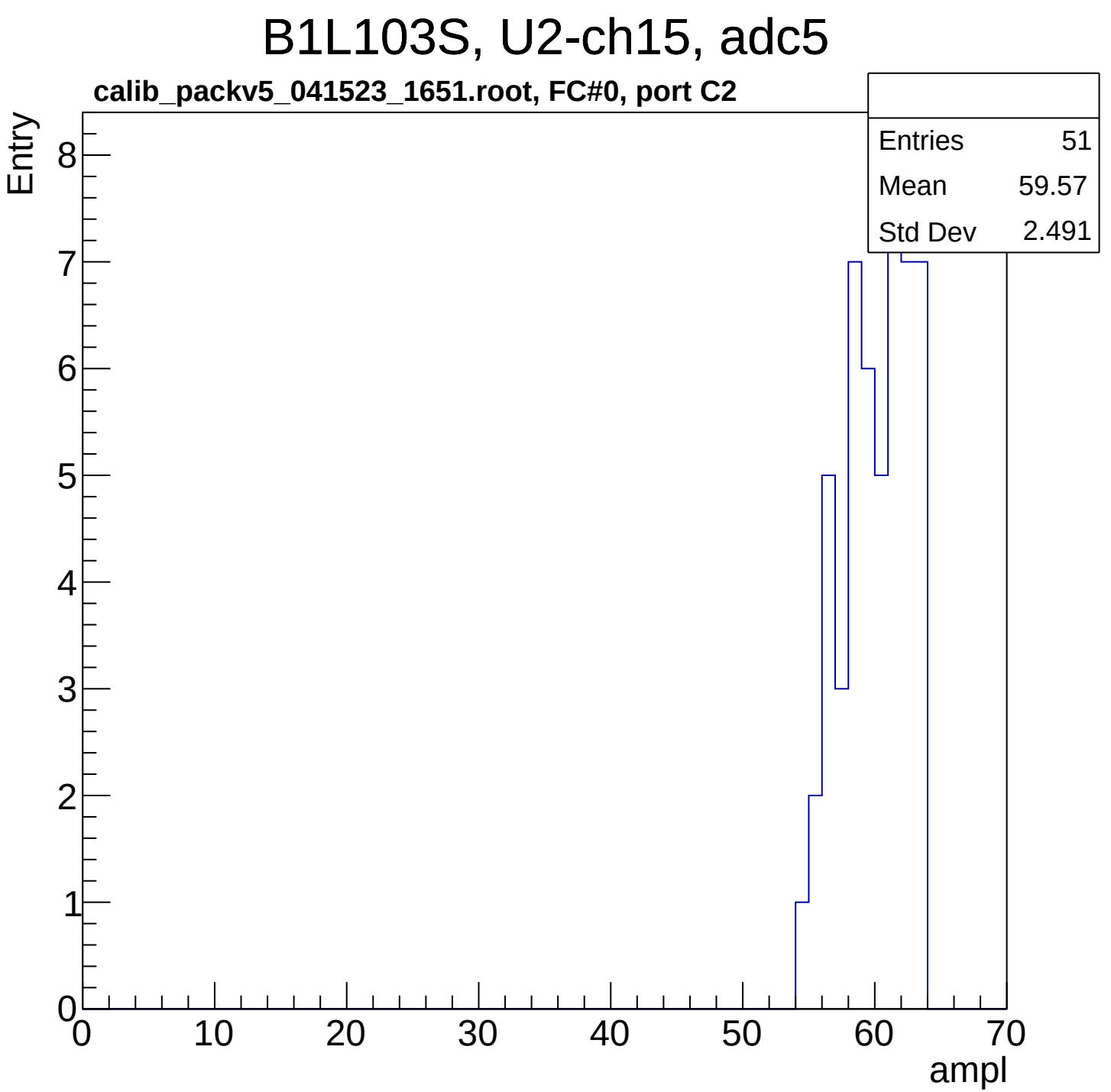

B1L103S, U2-ch15, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 25.14
Std Dev 10.57
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

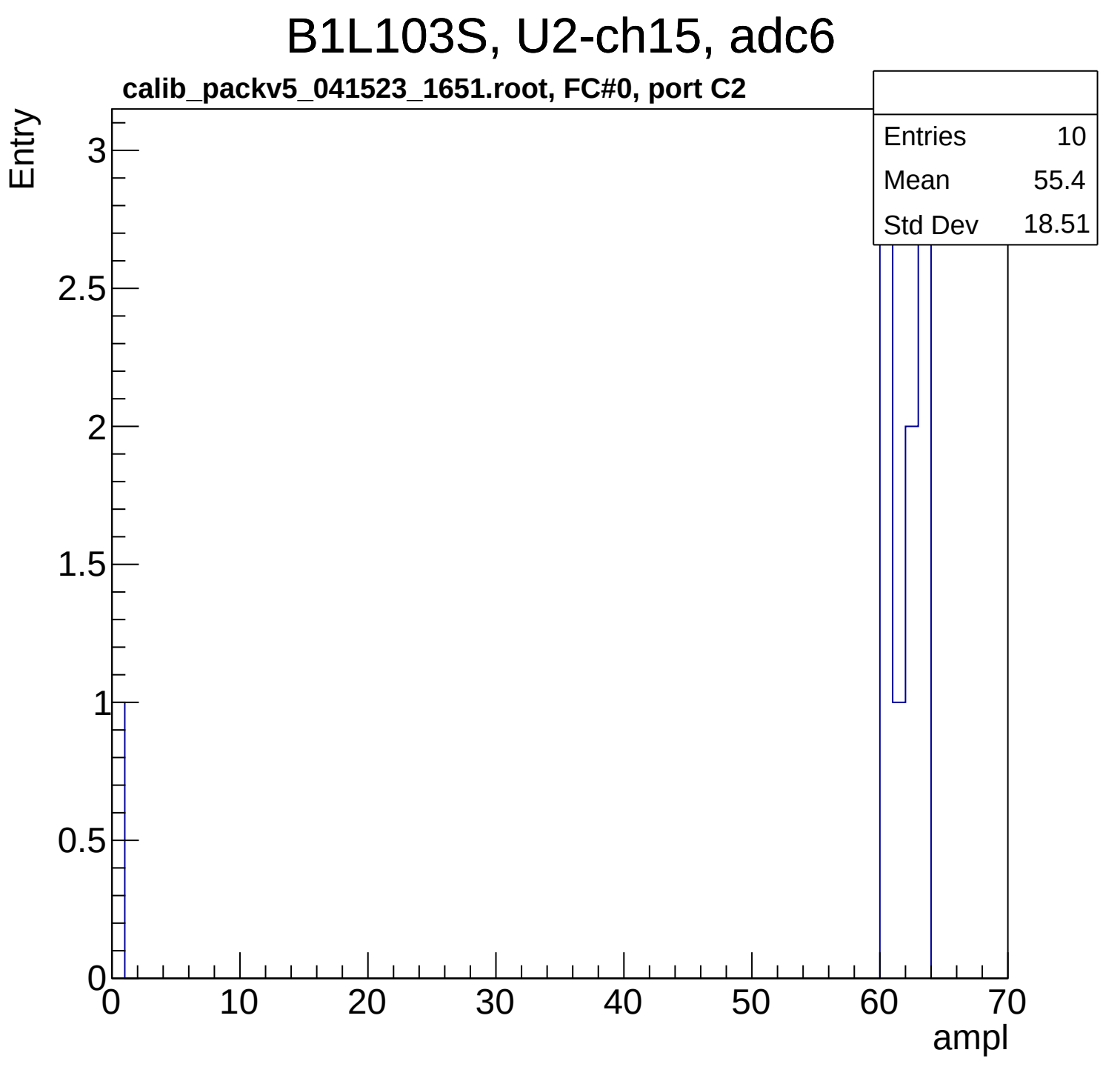

B1L103S, U2-ch15, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 32.49
Std Dev 10.43
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

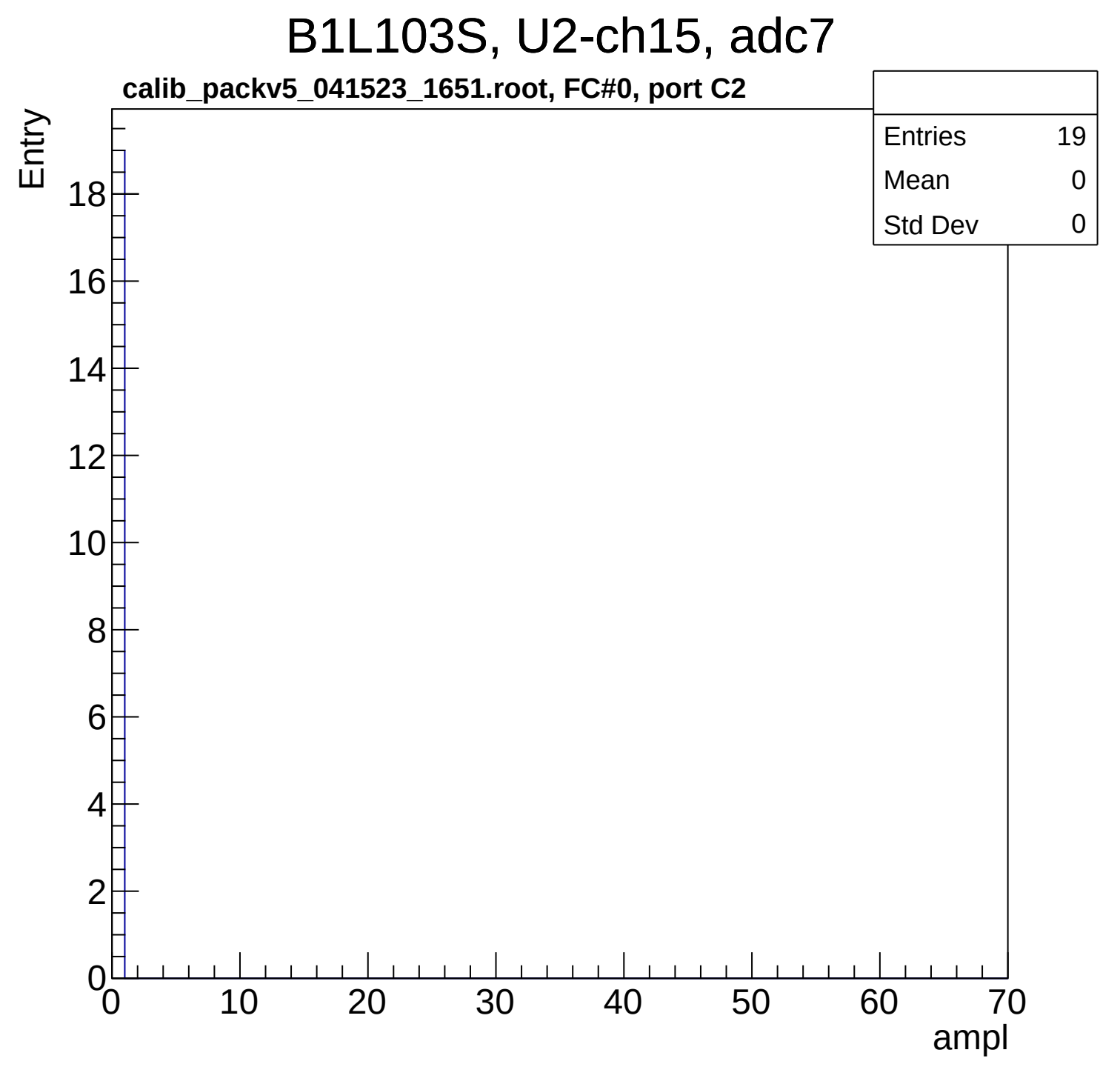

B1L103S, U2-ch15, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 37.25
Std Dev 12.29
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

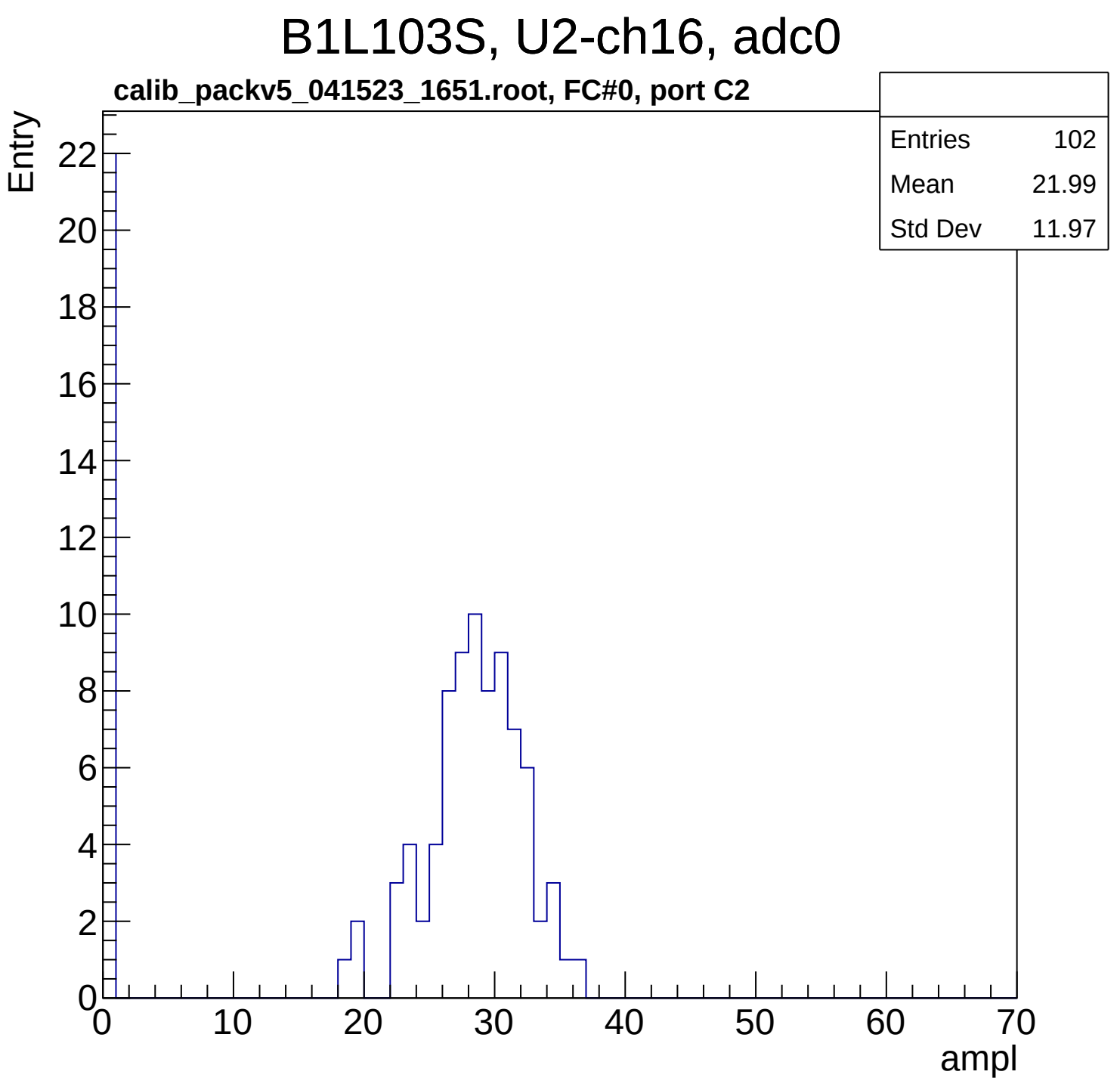

B1L103S, U2-ch15, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 46.76
Std Dev 6.573
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

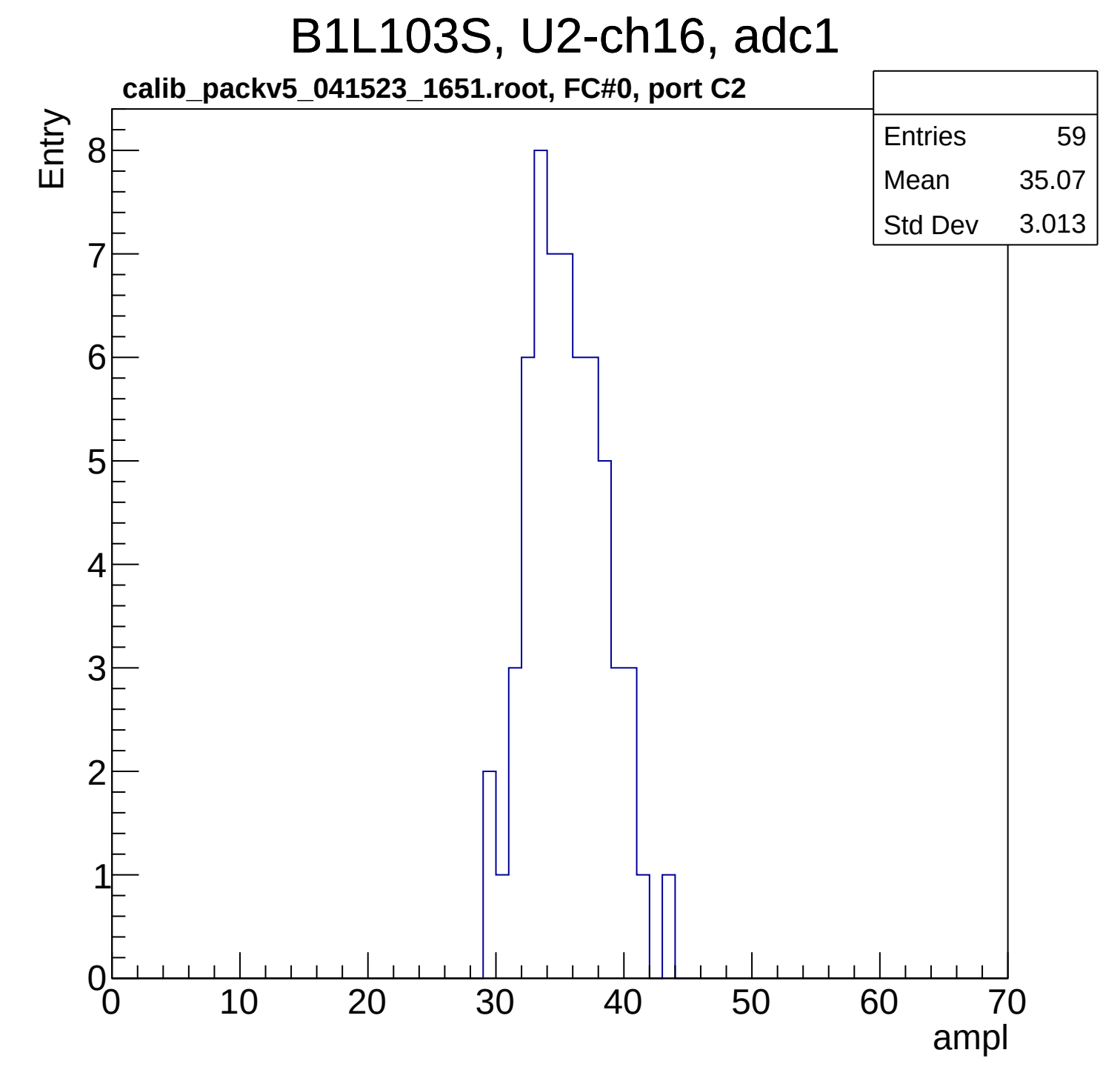

B1L103S, U2-ch15, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 54.12
Std Dev 3.35
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

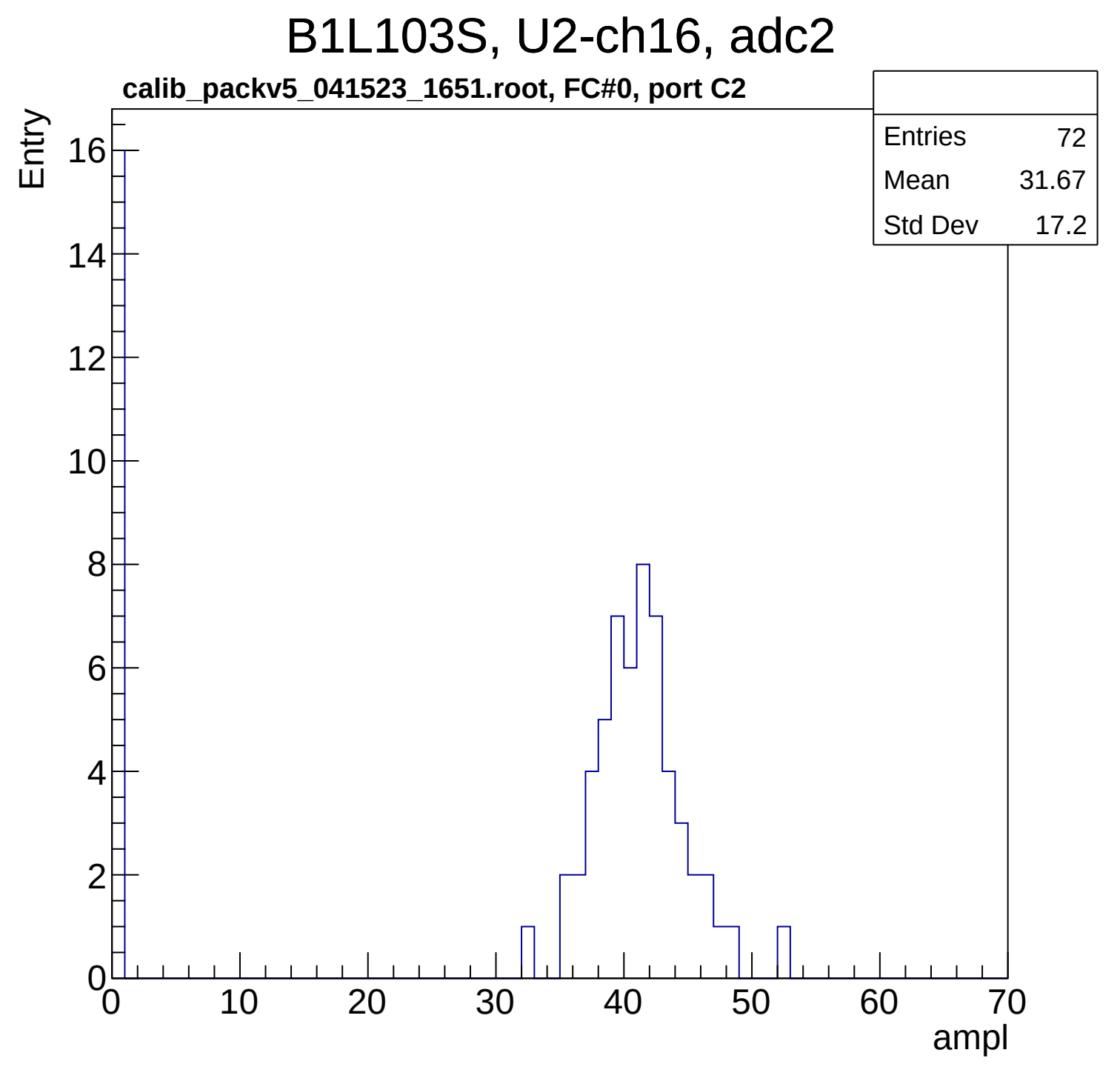

B1L103S, U2-ch15, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 59.57
Std Dev 2.491
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

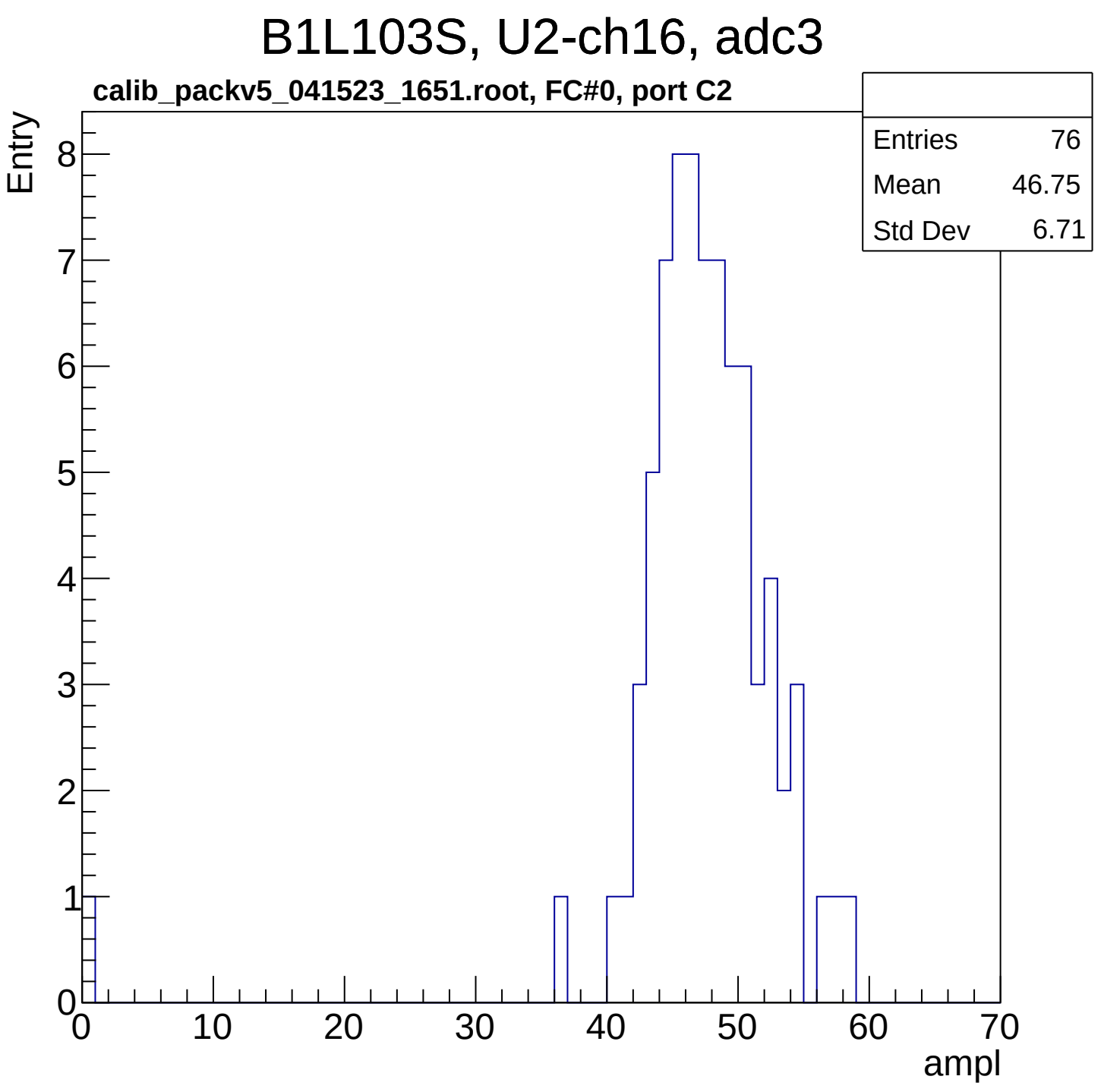

B1L103S, U2-ch15, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.4
Std Dev 18.51
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

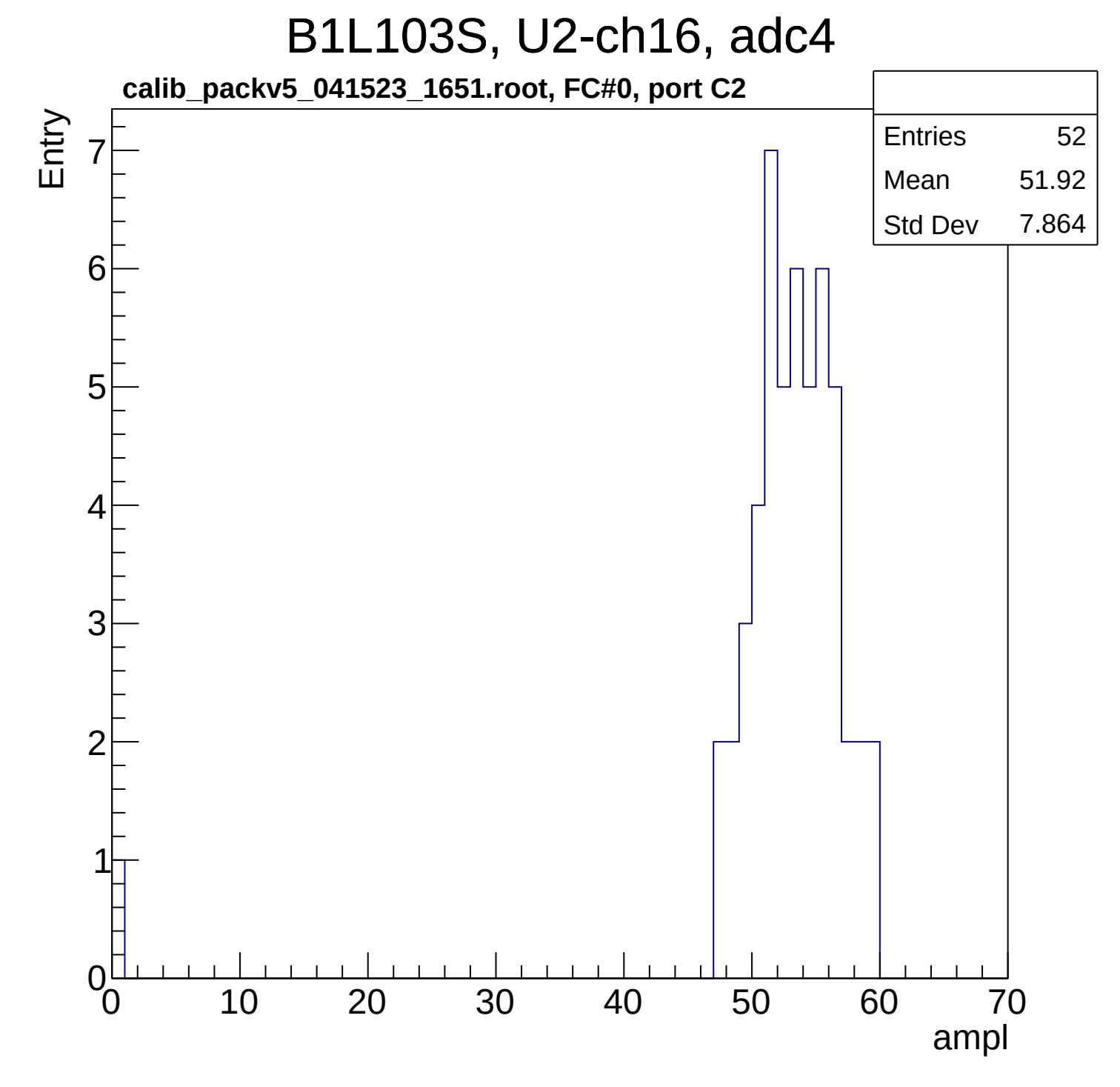

B1L103S, U2-ch15, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

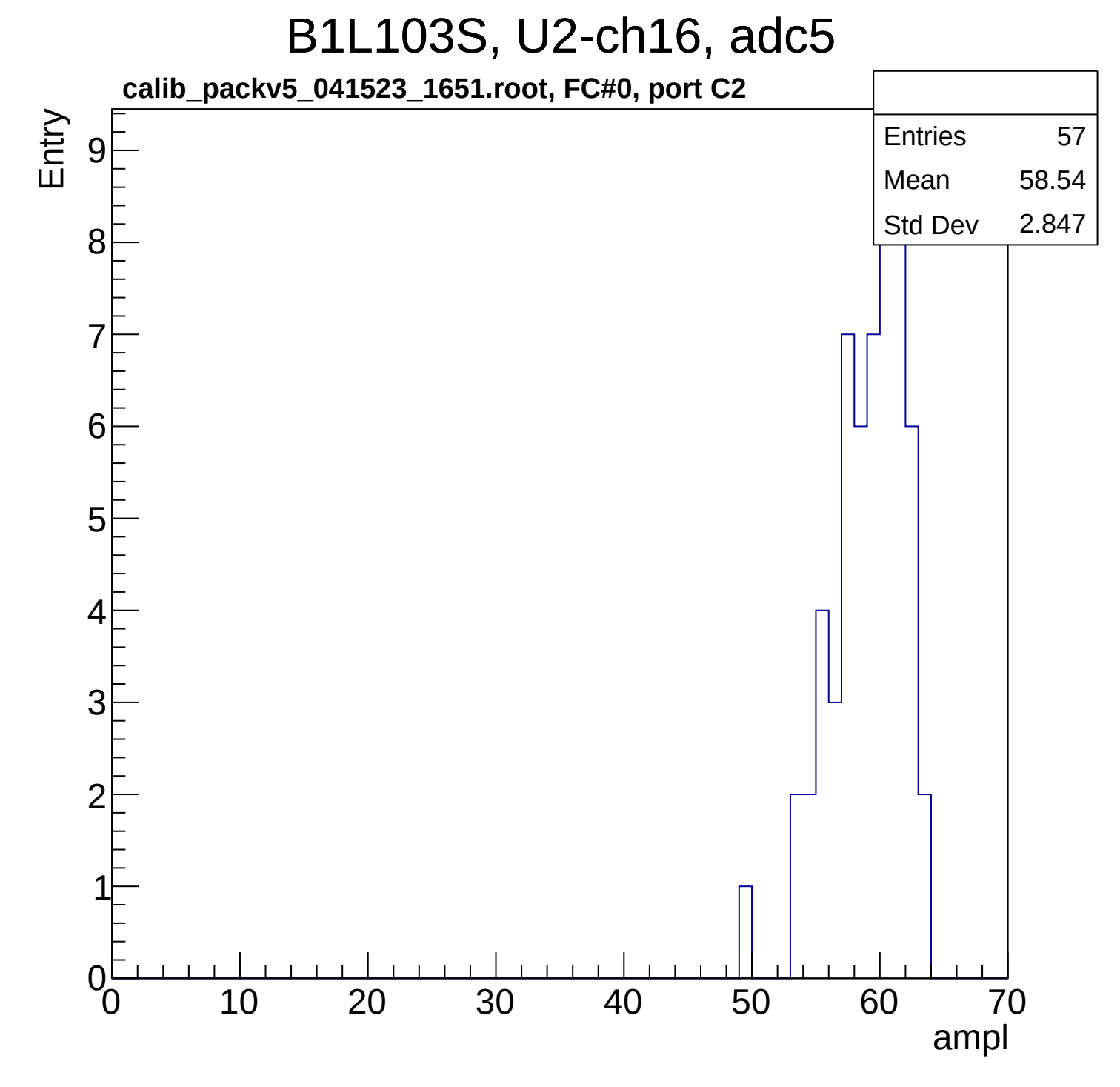

B1L103S, U2-ch16, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 21.99
Std Dev 11.97
Entry
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70
ampl

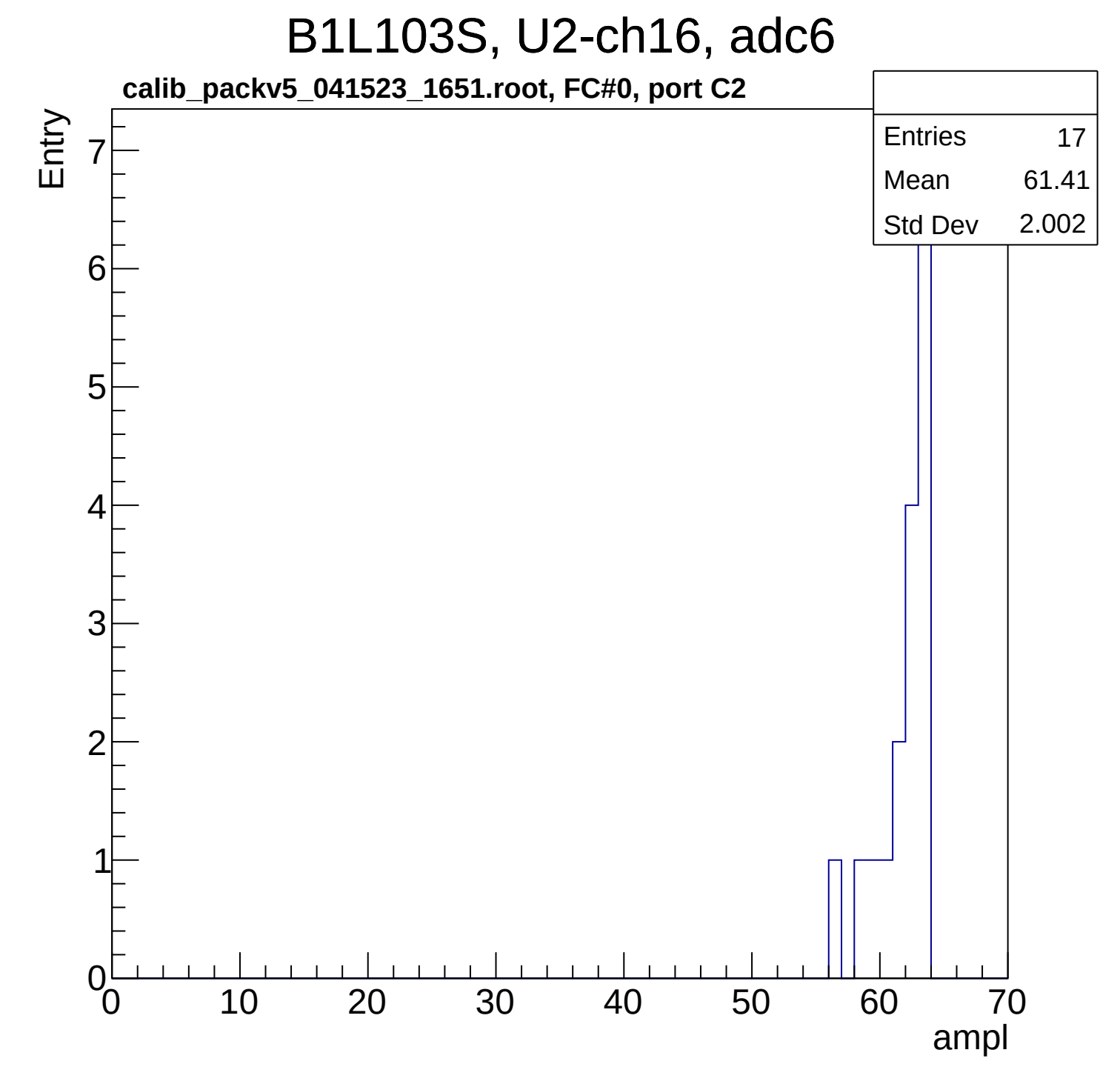

B1L103S, U2-ch16, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 35.07
Std Dev 3.013
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

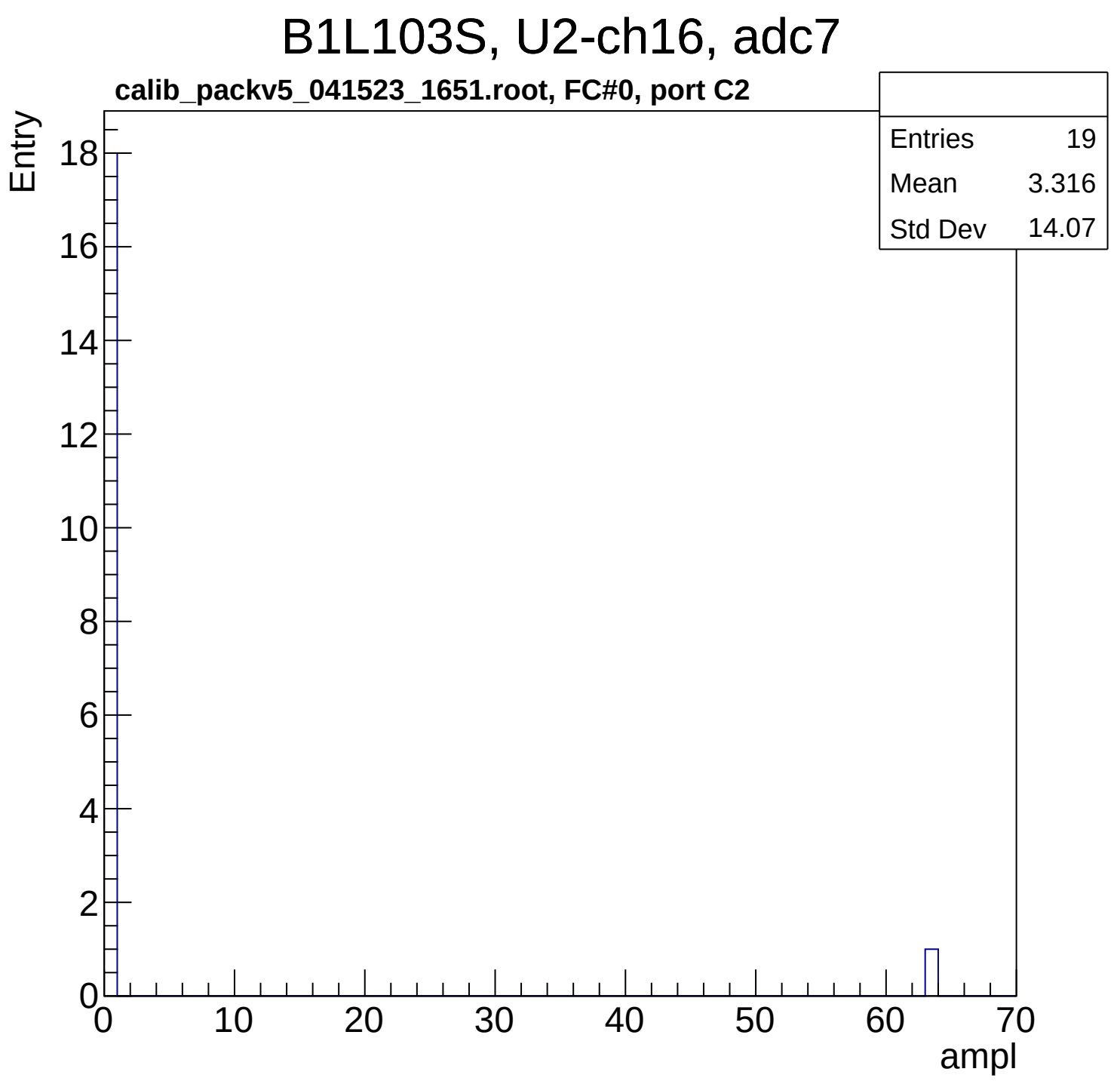

B1L103S, U2-ch16, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 31.67
Std Dev 17.2
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

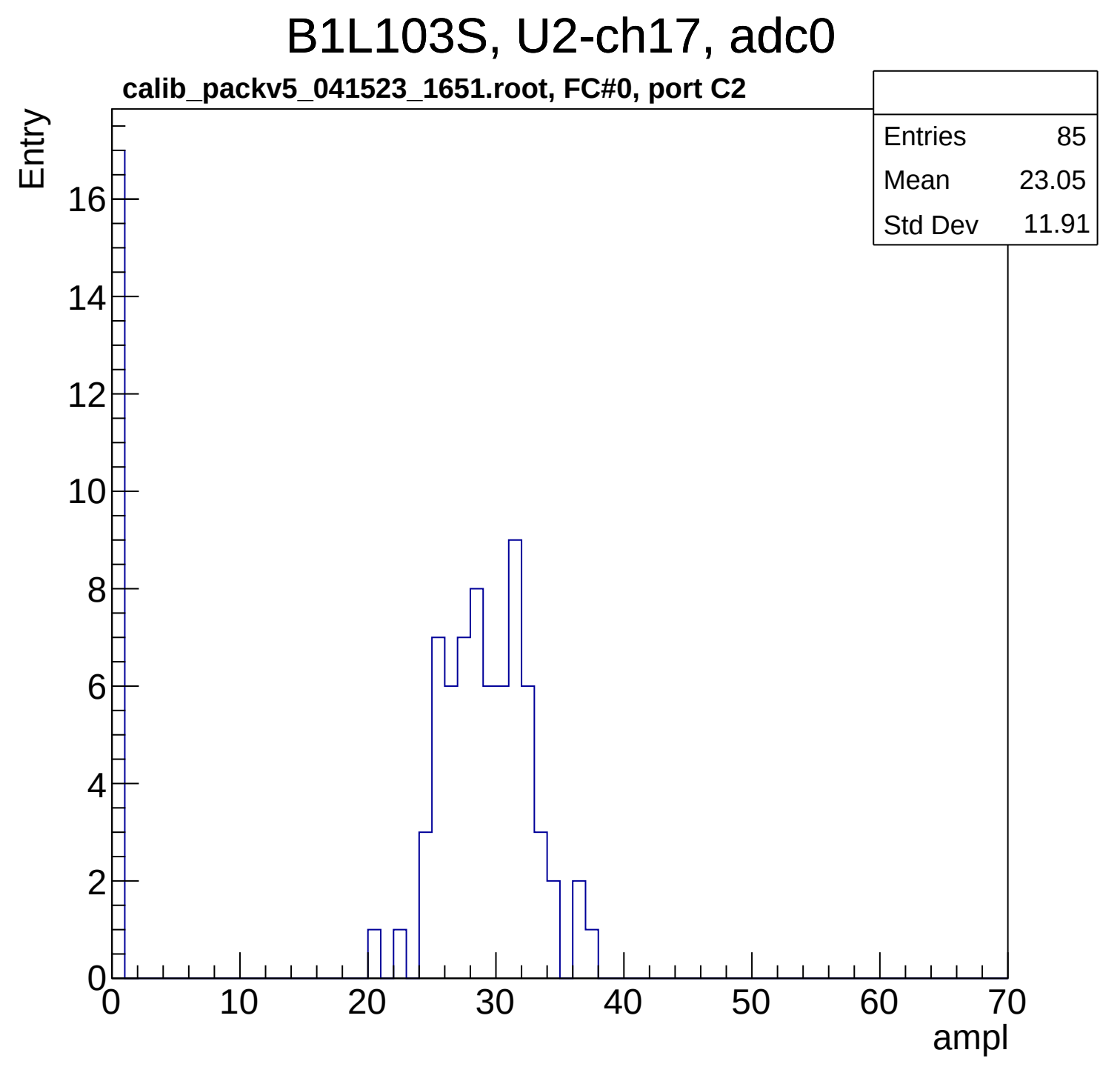

B1L103S, U2-ch16, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 46.75
Std Dev 6.71
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

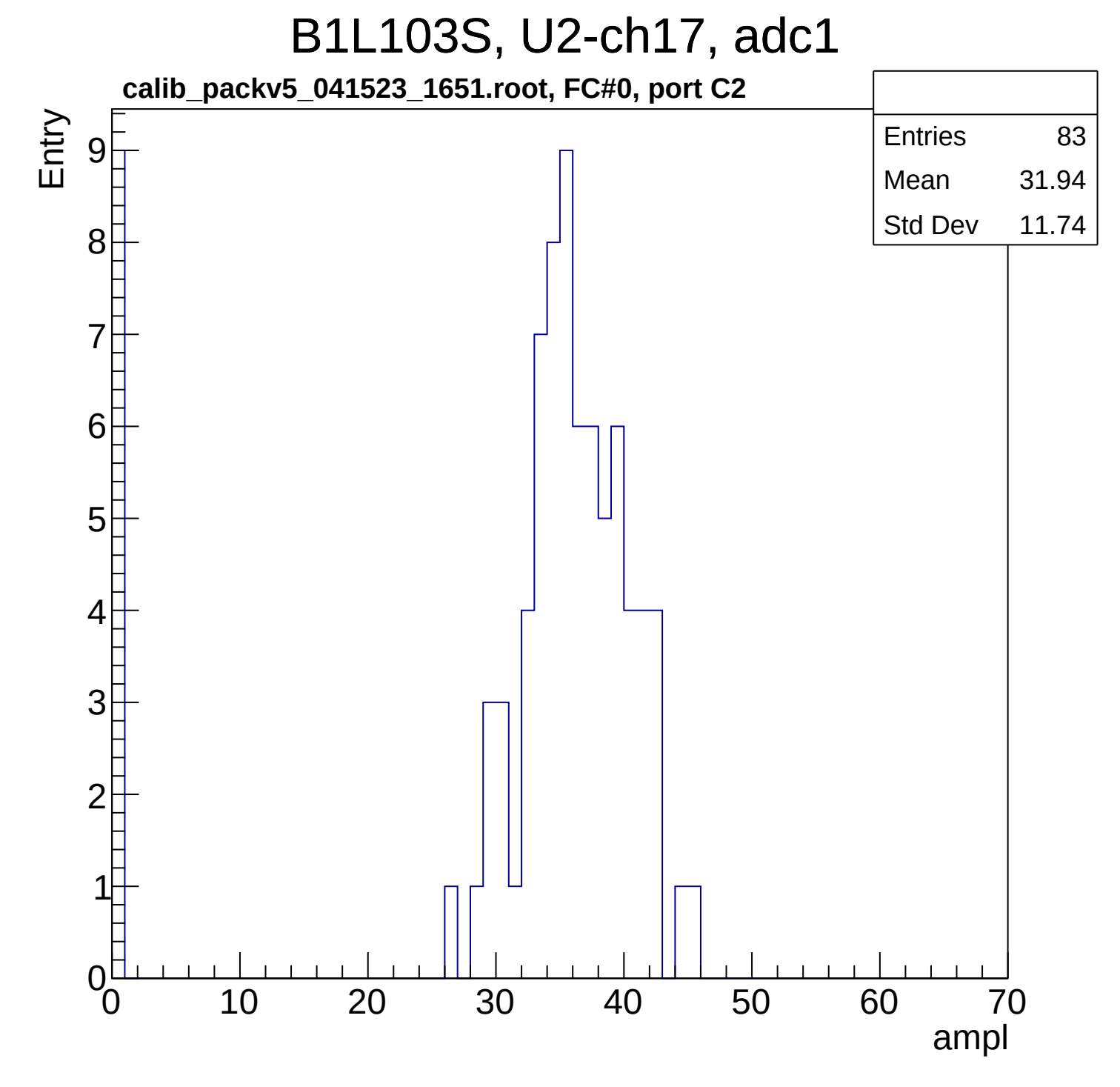

B1L103S, U2-ch16, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 51.92
Std Dev 7.864
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

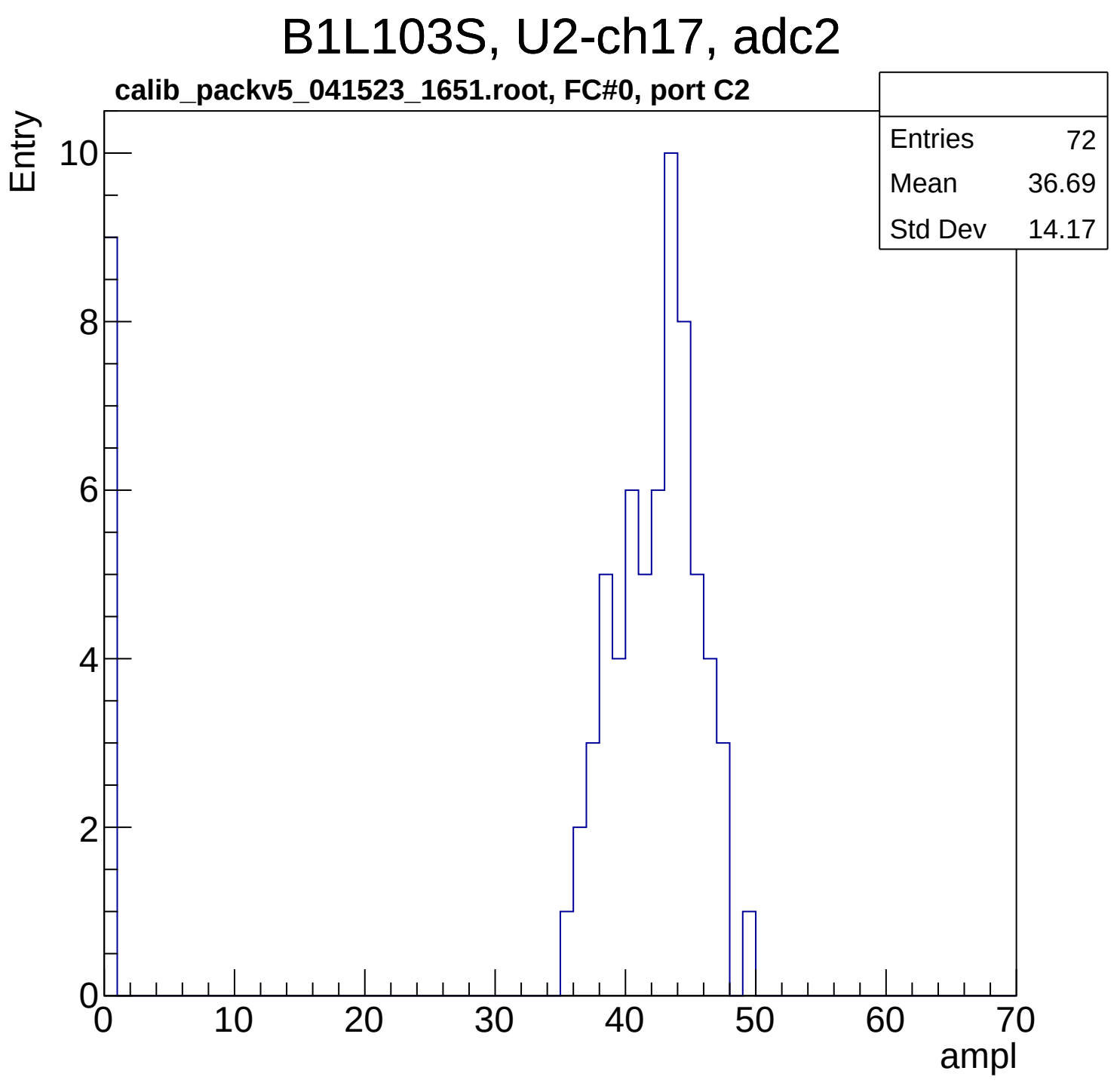

B1L103S, U2-ch16, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.54
Std Dev 2.847
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

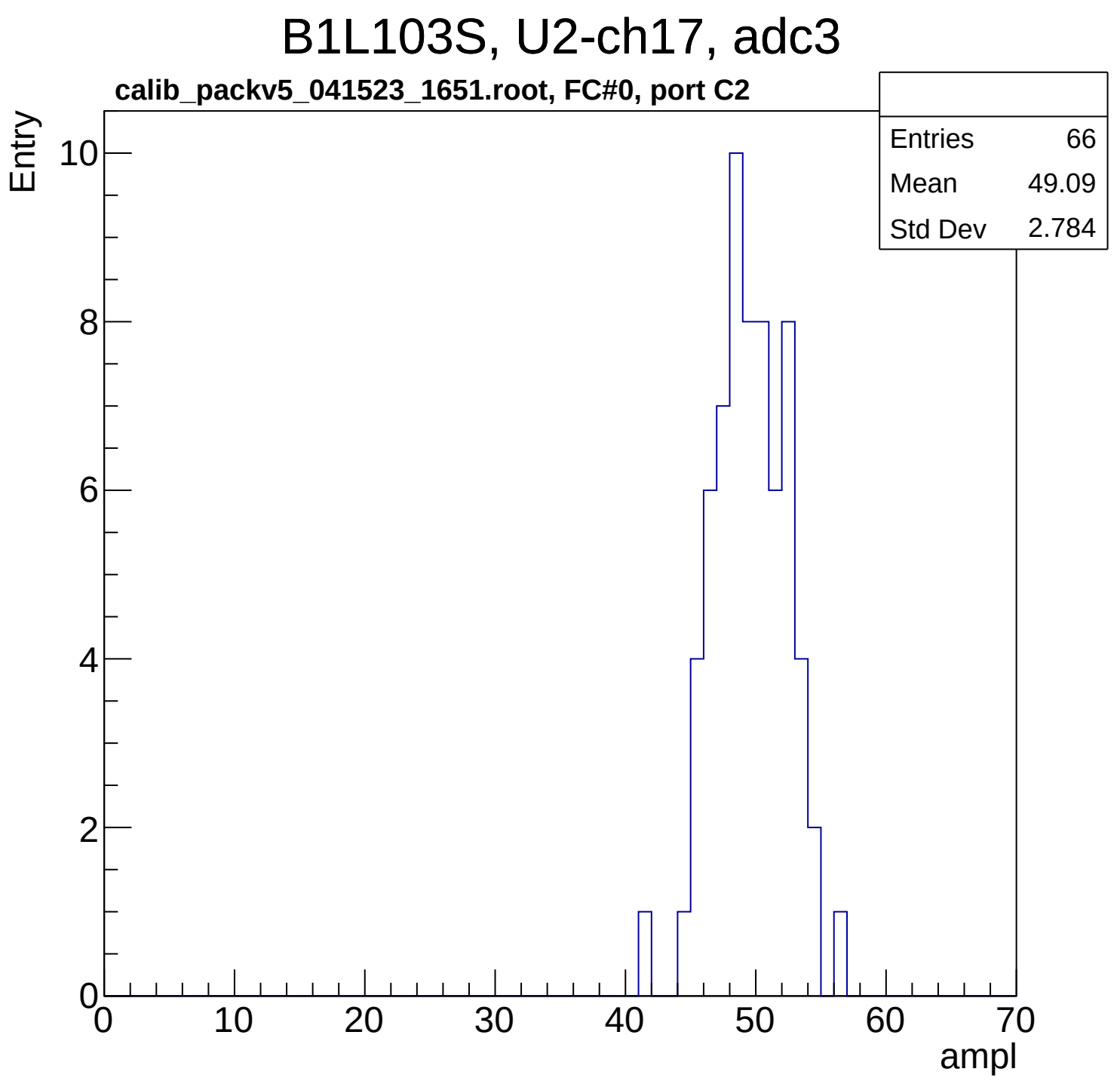

B1L103S, U2-ch16, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.41
Std Dev 2.002
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

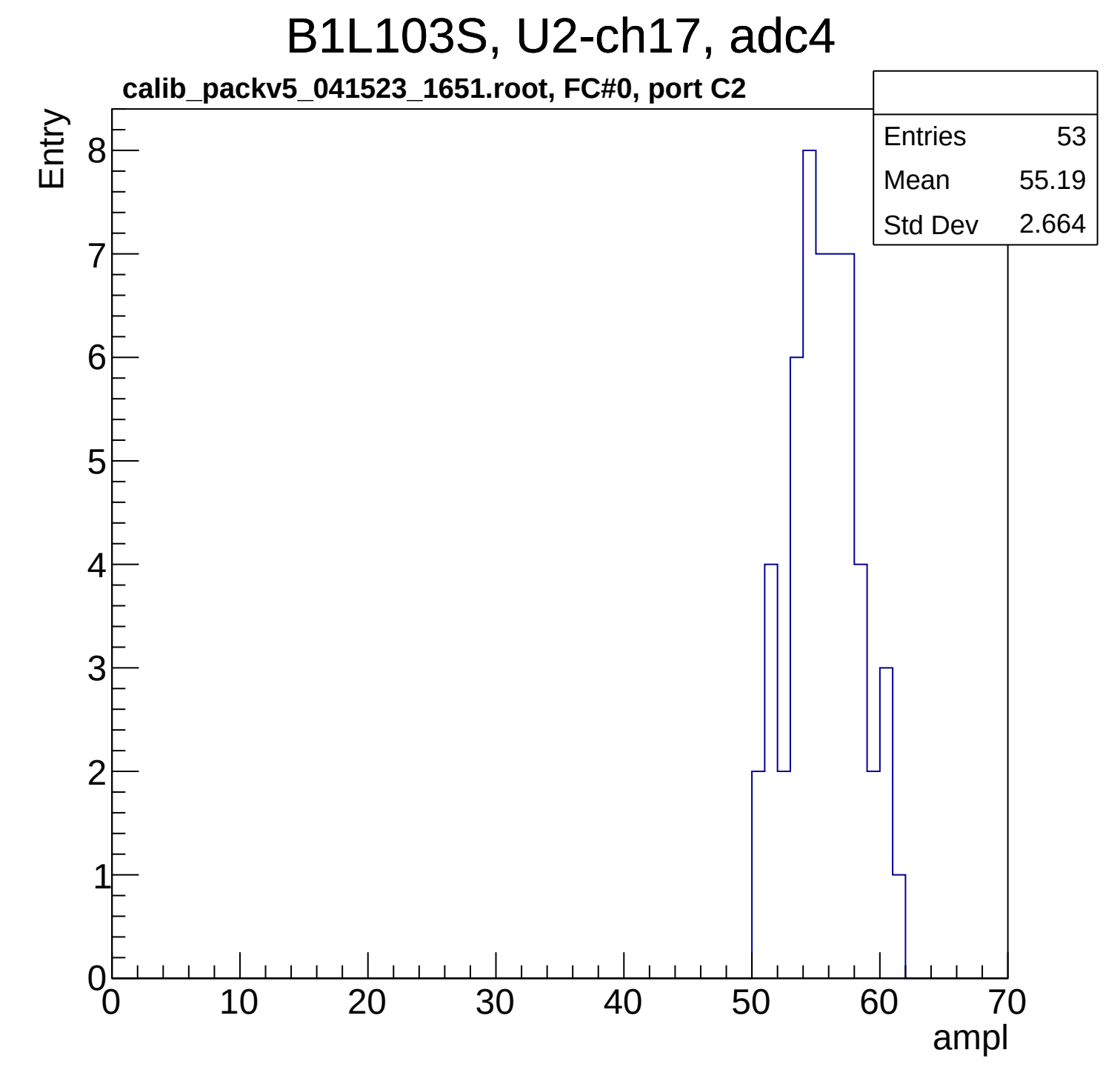

B1L103S, U2-ch16, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

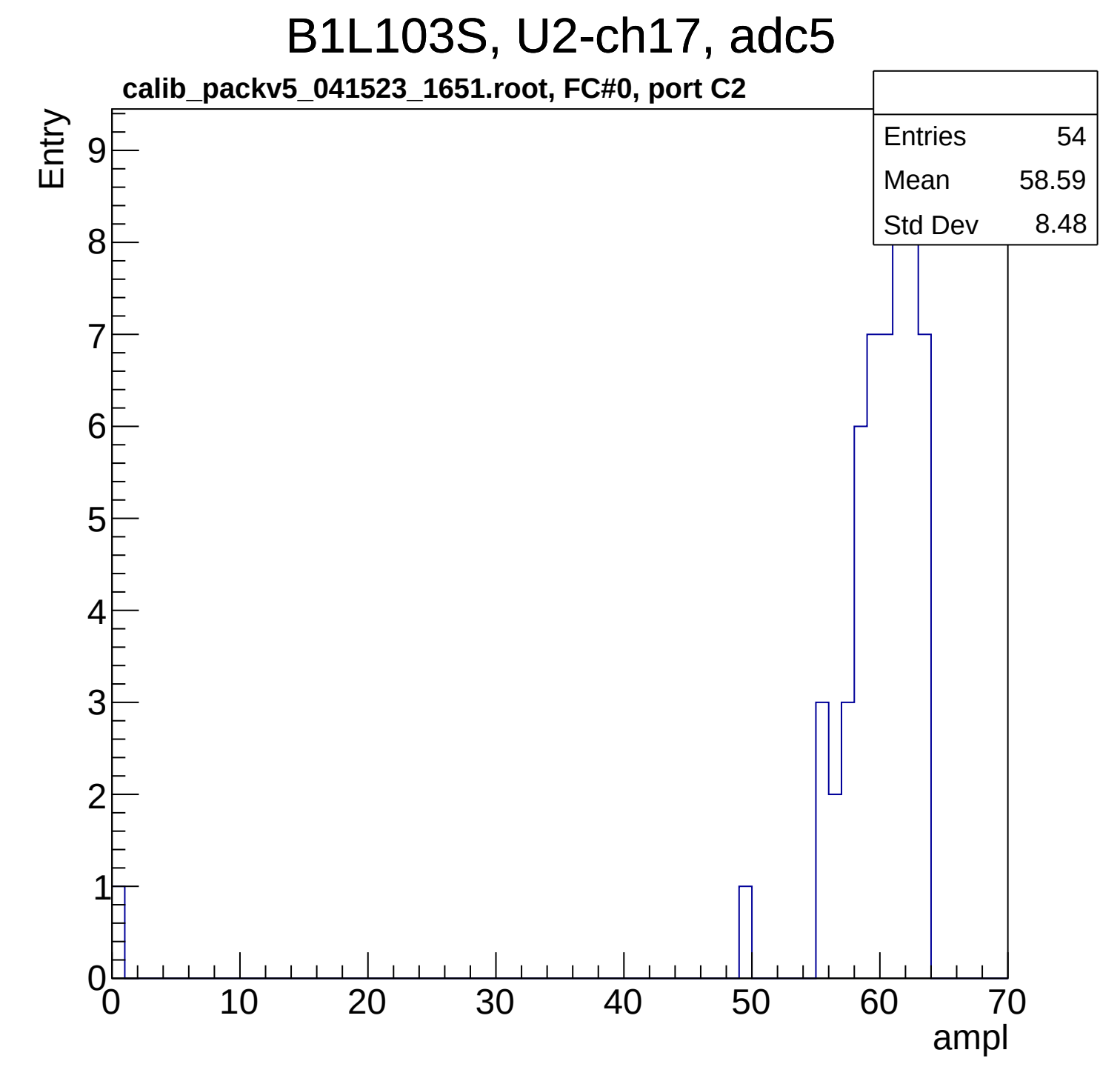

B1L103S, U2-ch17, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 23.05
Std Dev 11.91
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

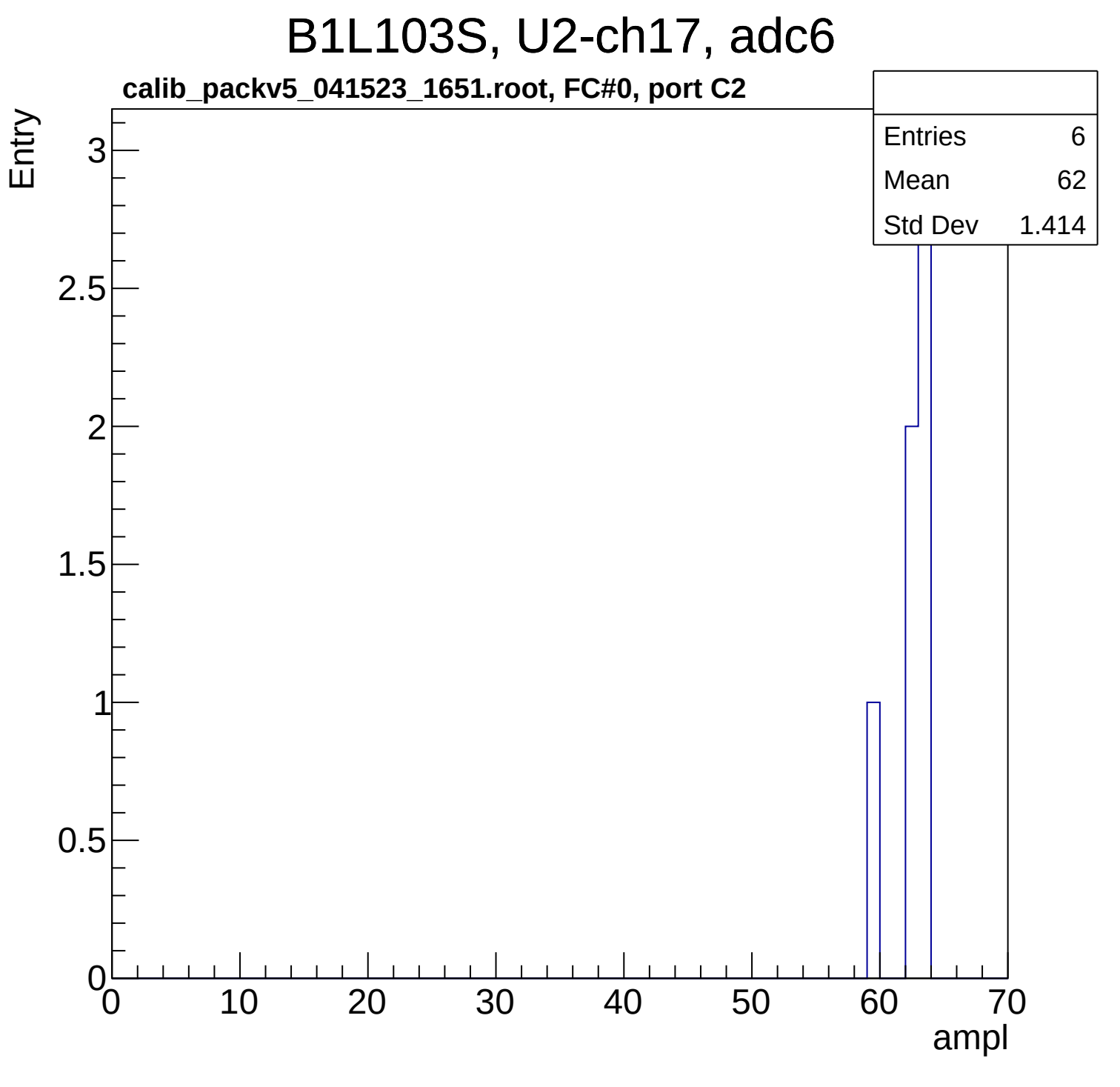

B1L103S, U2-ch17, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 31.94
Std Dev 11.74
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

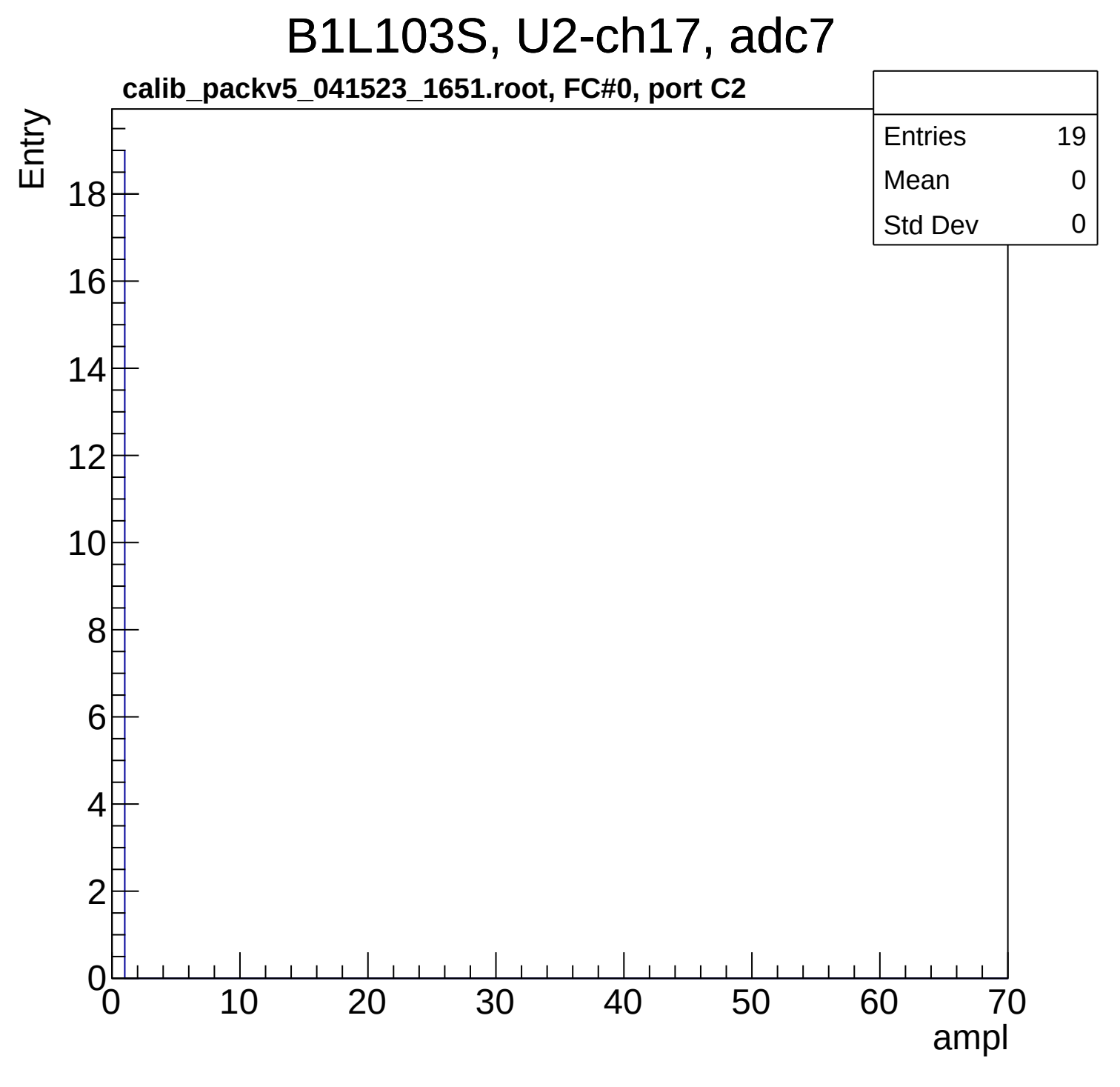

B1L103S, U2-ch17, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 36.69
Std Dev 14.17
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

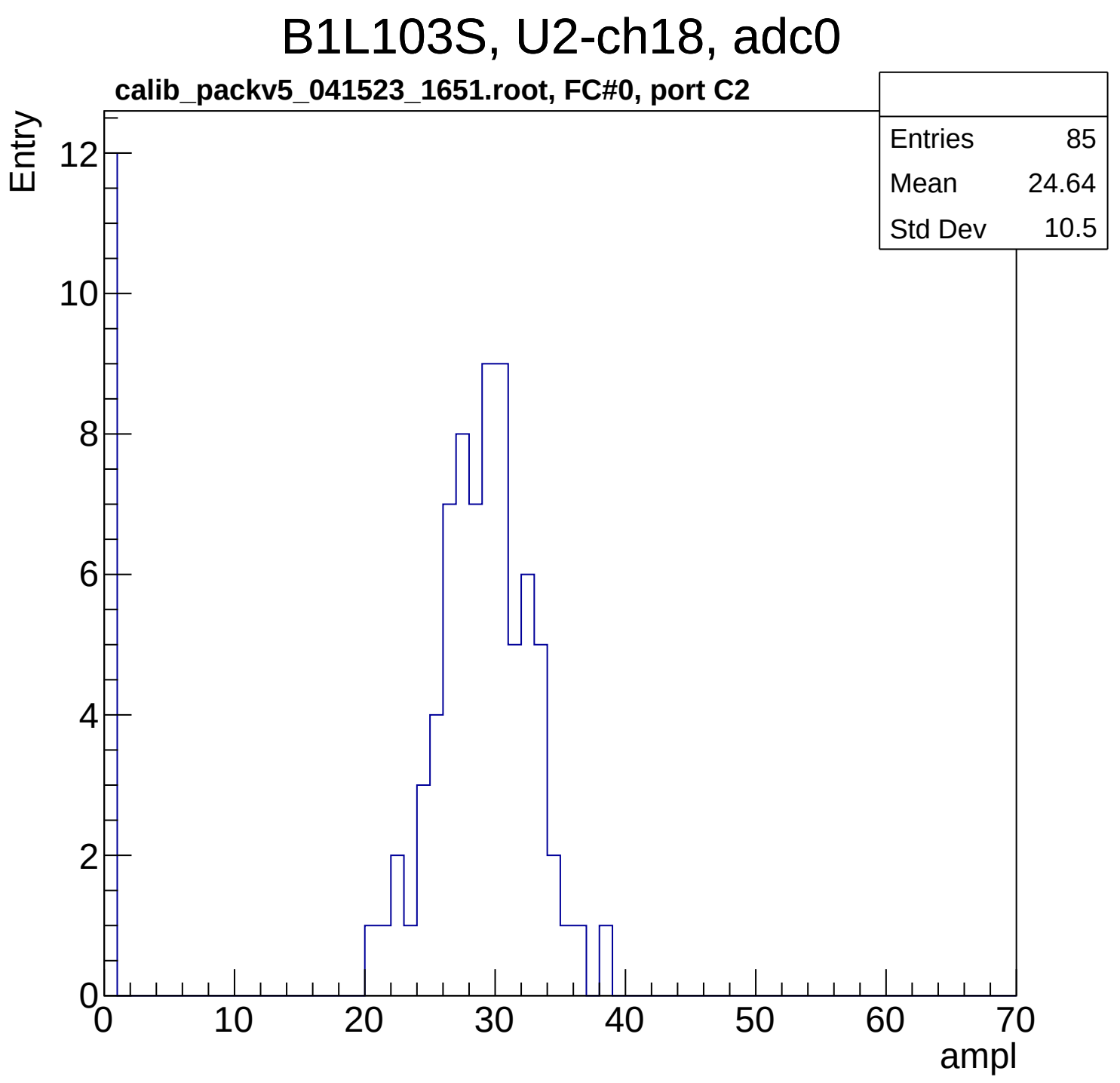

B1L103S, U2-ch17, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 49.09
Std Dev 2.784
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

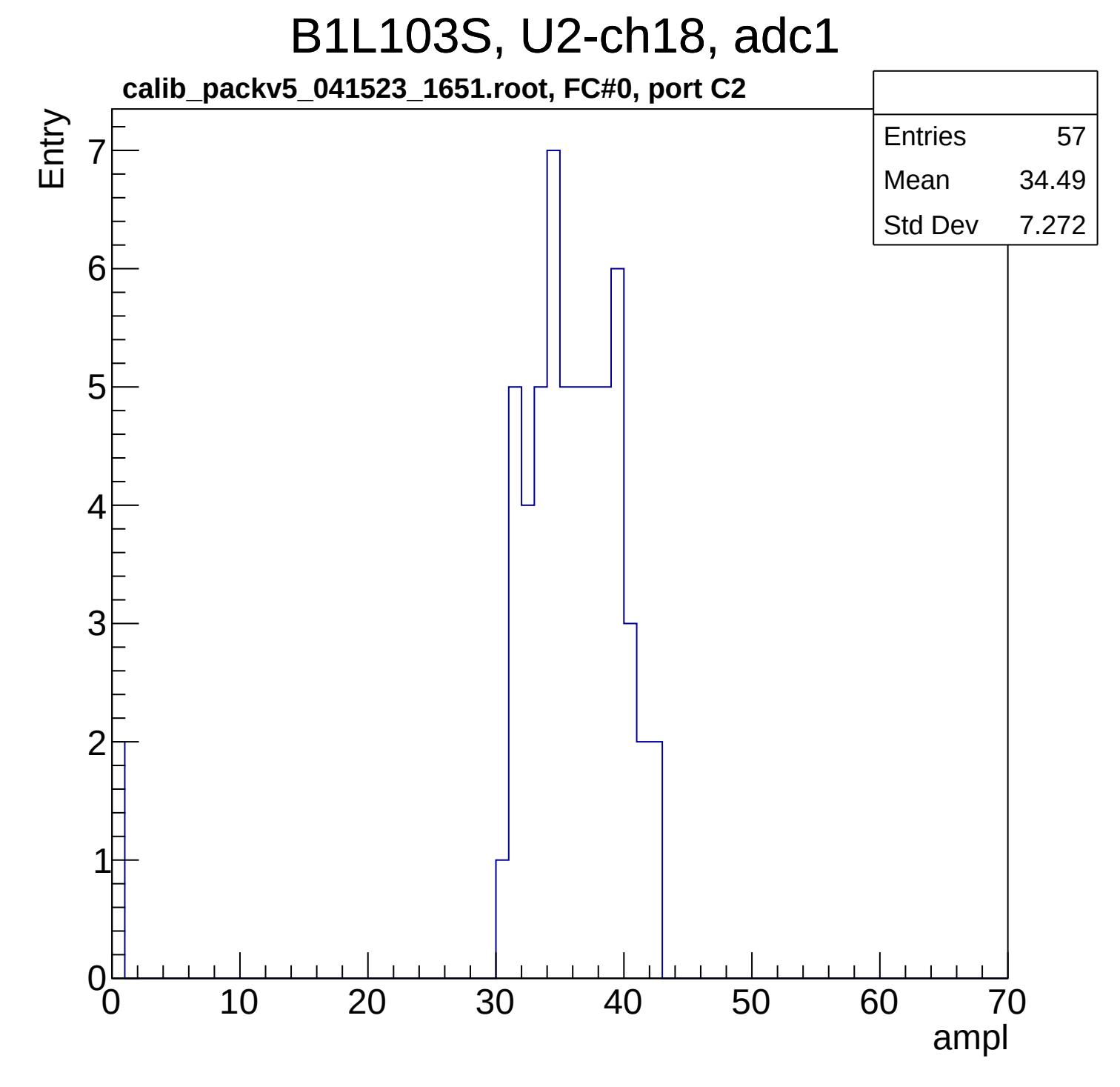

B1L103S, U2-ch17, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 55.19
Std Dev 2.664
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

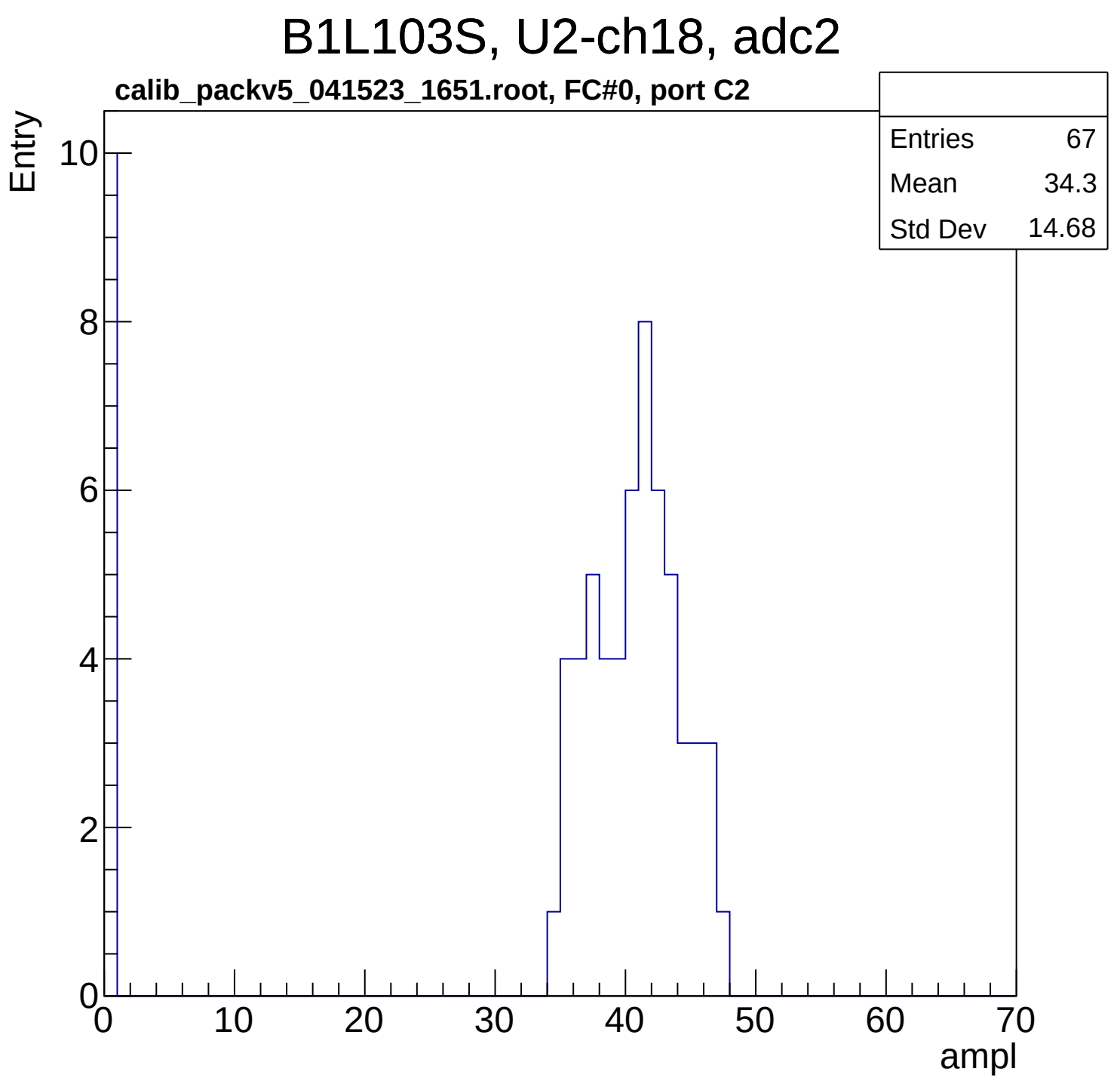

B1L103S, U2-ch17, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.59
Std Dev 8.48
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

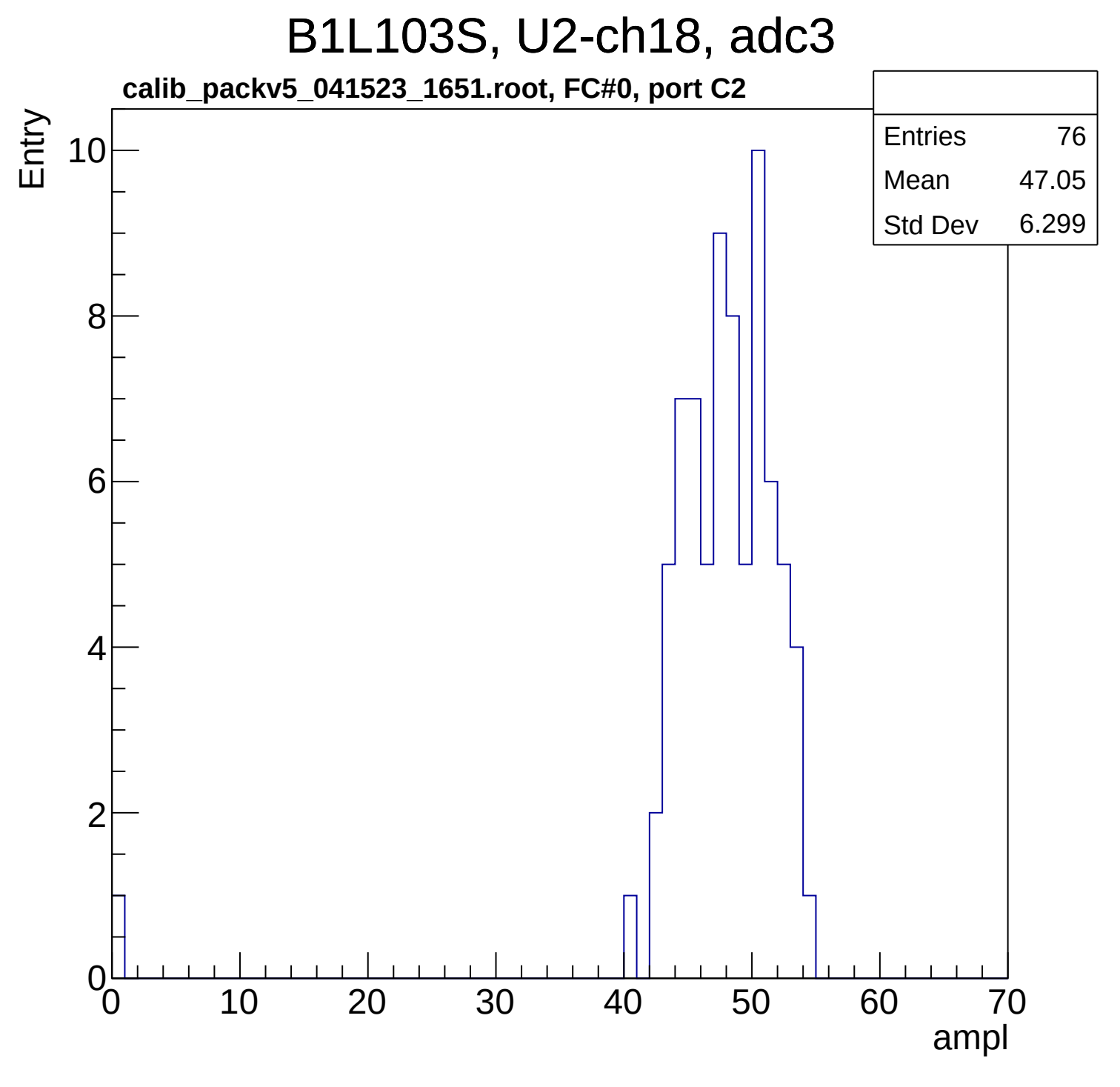

B1L103S, U2-ch17, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62
Std Dev 1.414
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

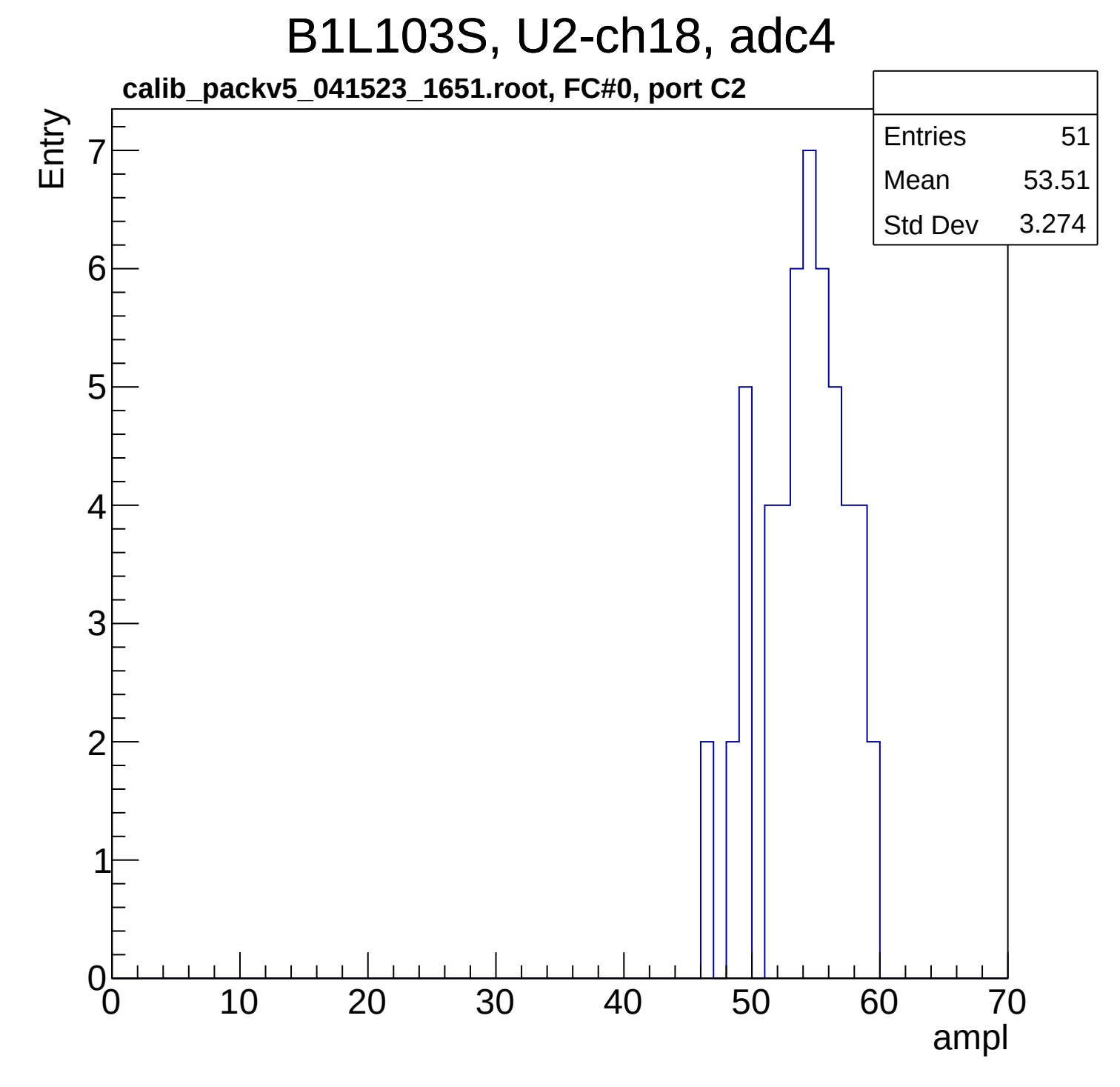

B1L103S, U2-ch17, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

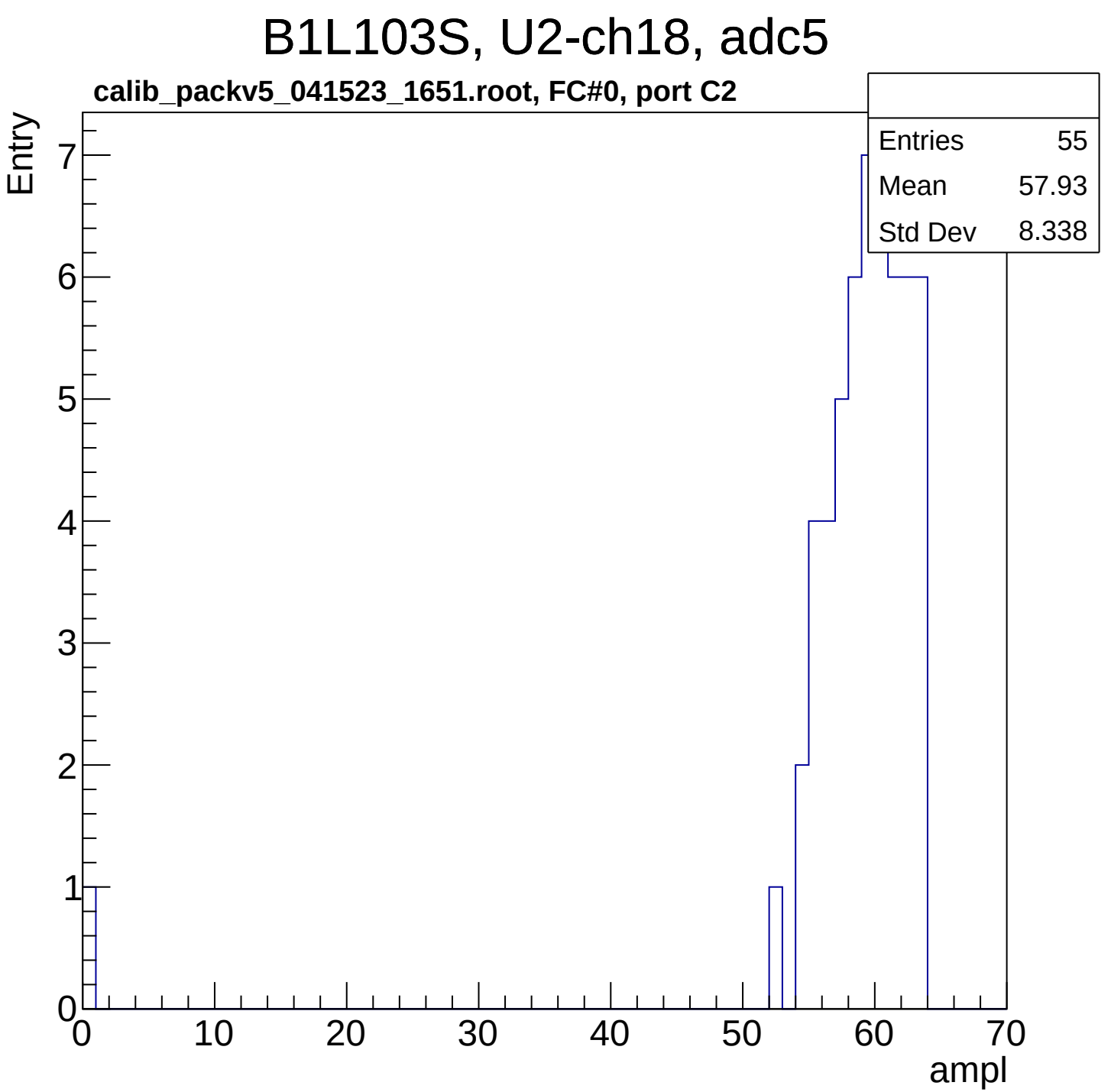

B1L103S, U2-ch18, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 24.64
Std Dev 10.5
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

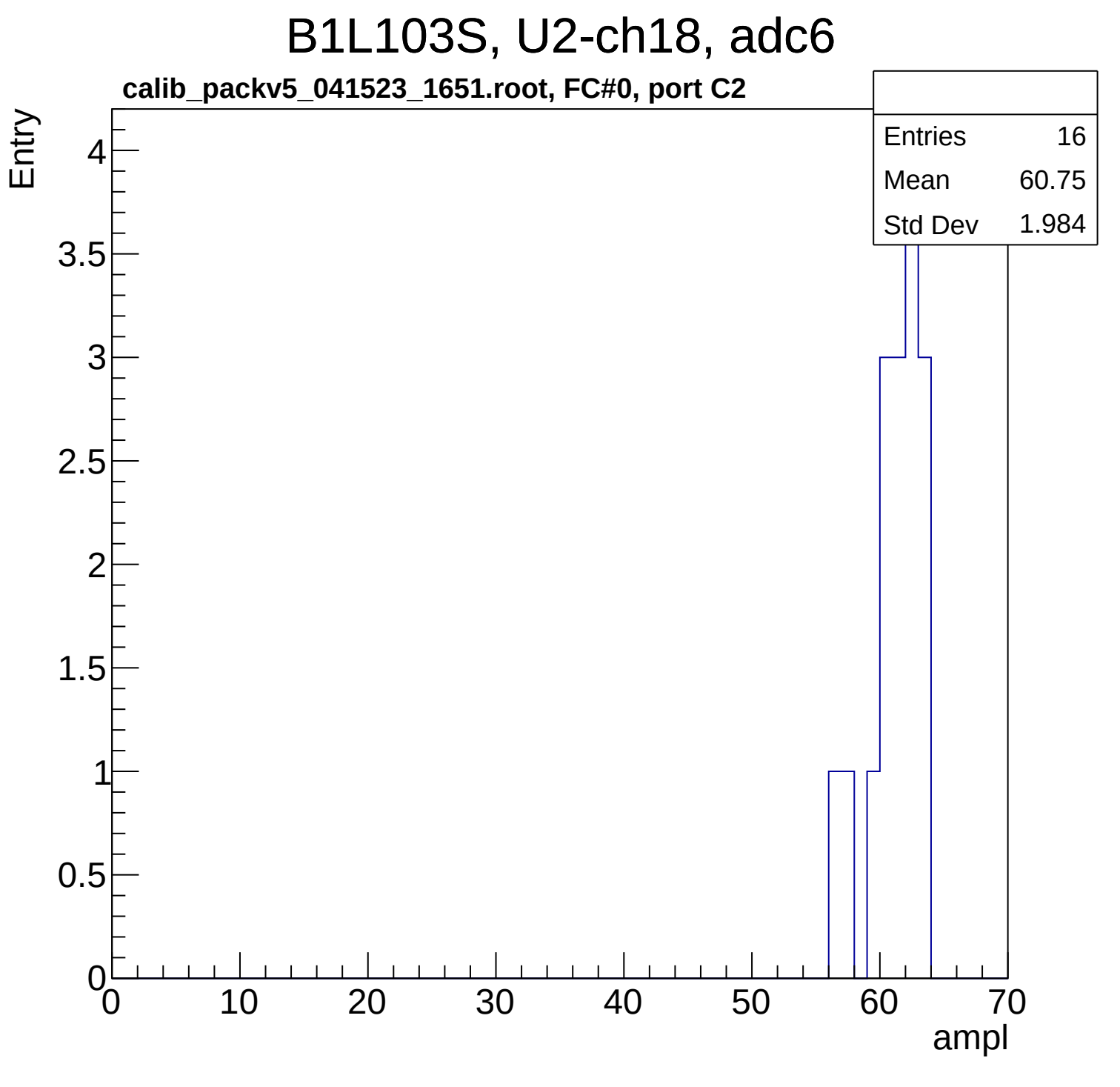

B1L103S, U2-ch18, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 34.49
Std Dev 7.272
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

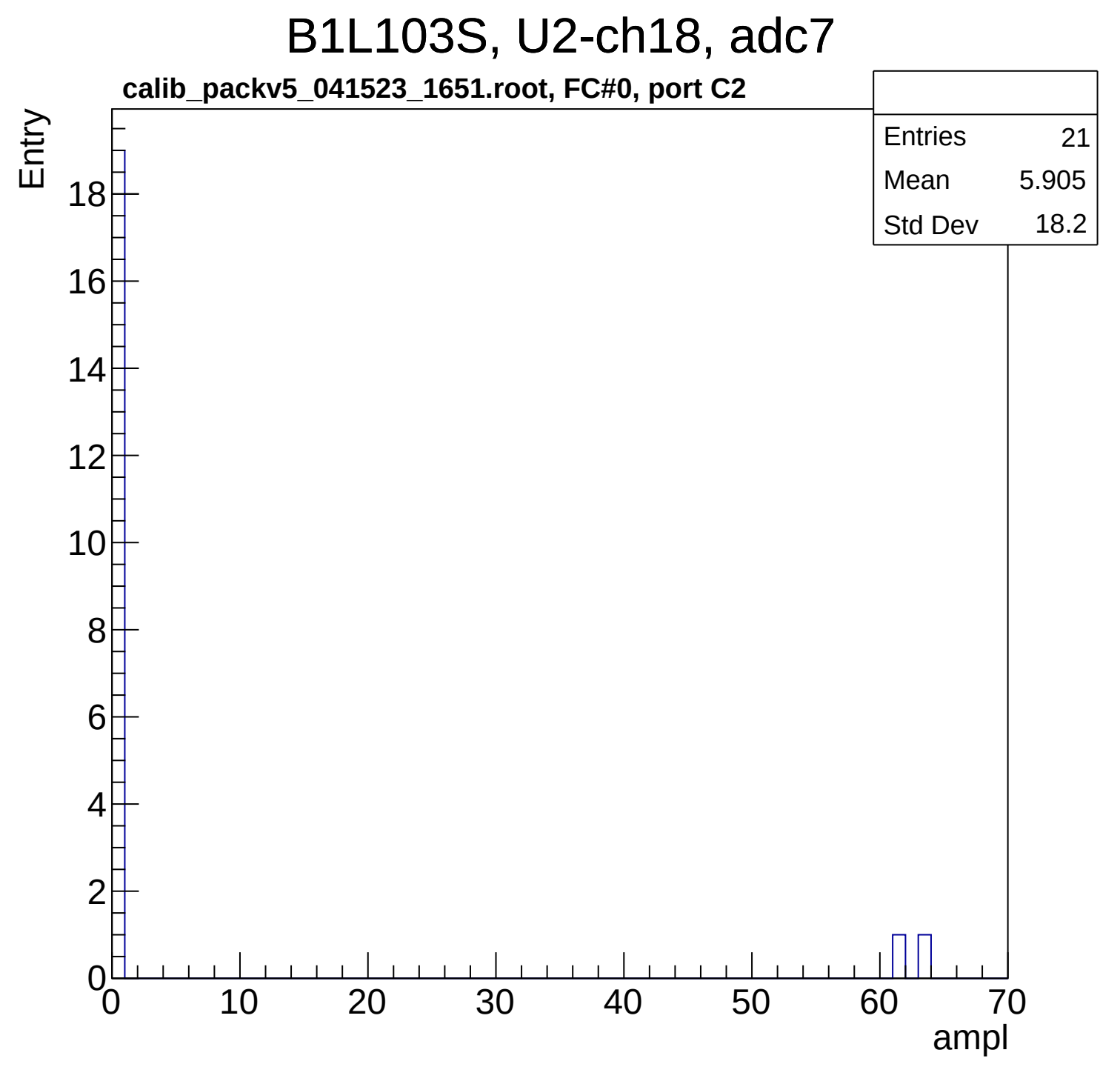

B1L103S, U2-ch18, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 34.3
Std Dev 14.68
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

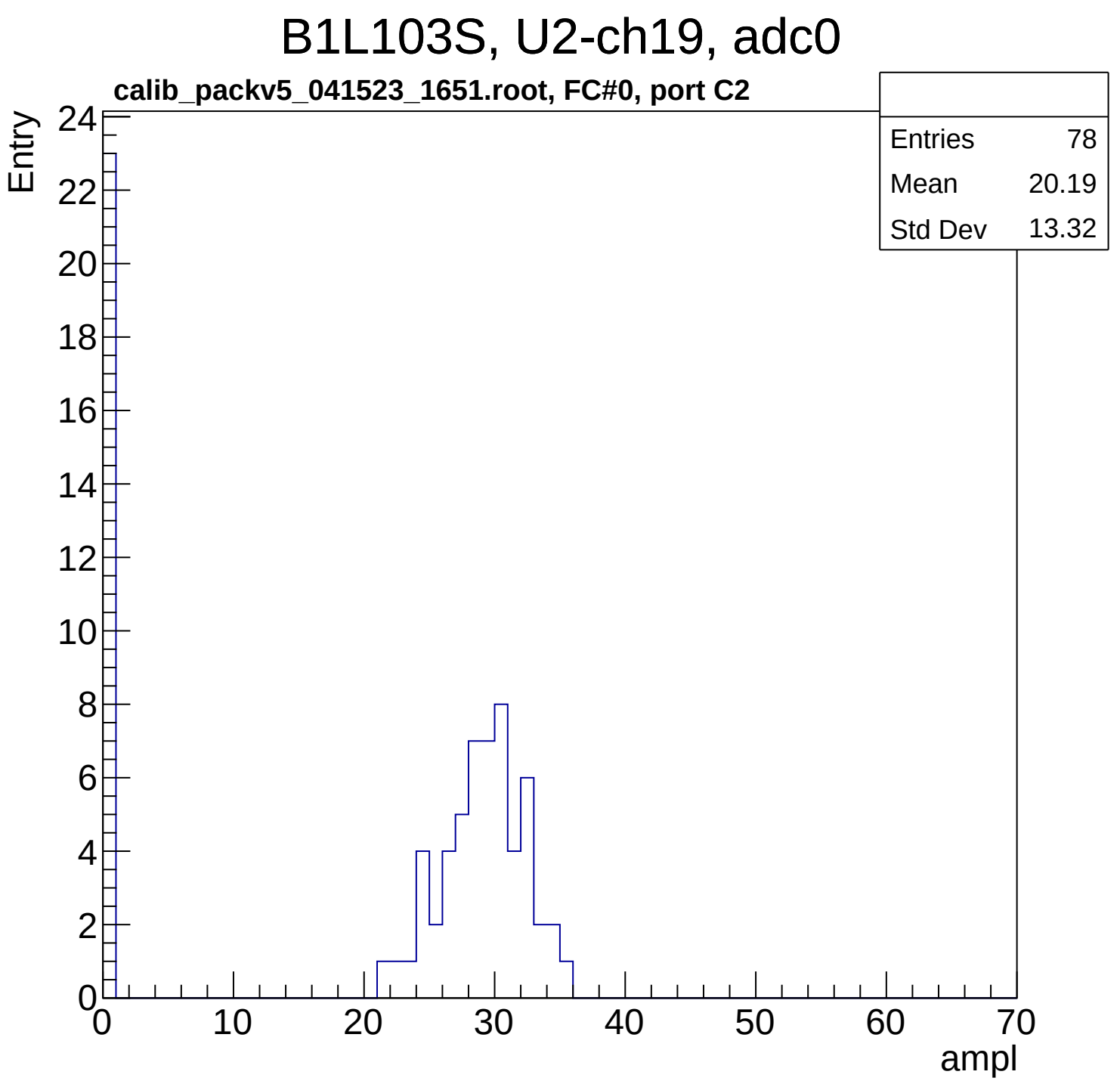

B1L103S, U2-ch18, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 47.05
Std Dev 6.299
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

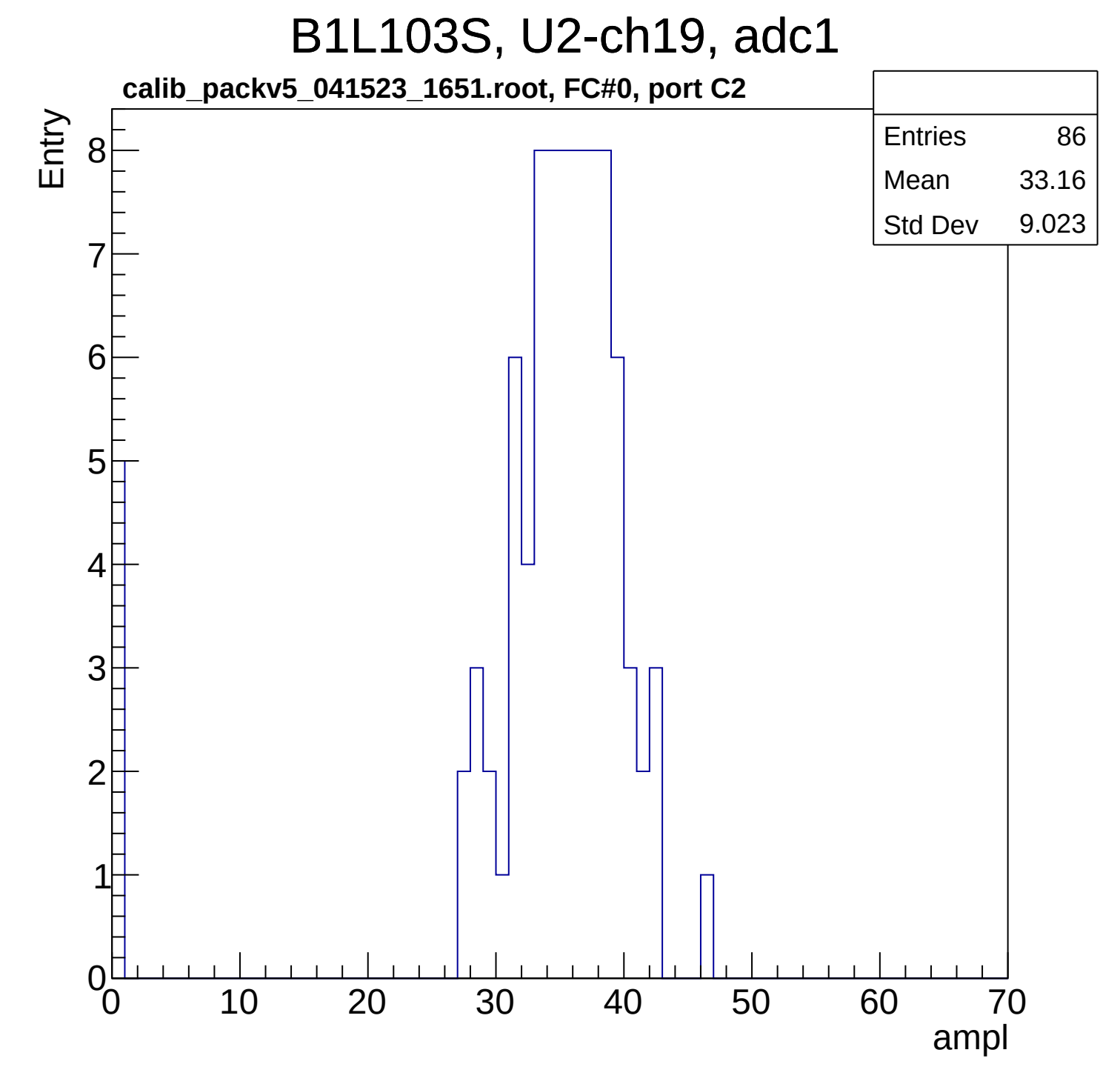

B1L103S, U2-ch18, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 53.51
Std Dev 3.274
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

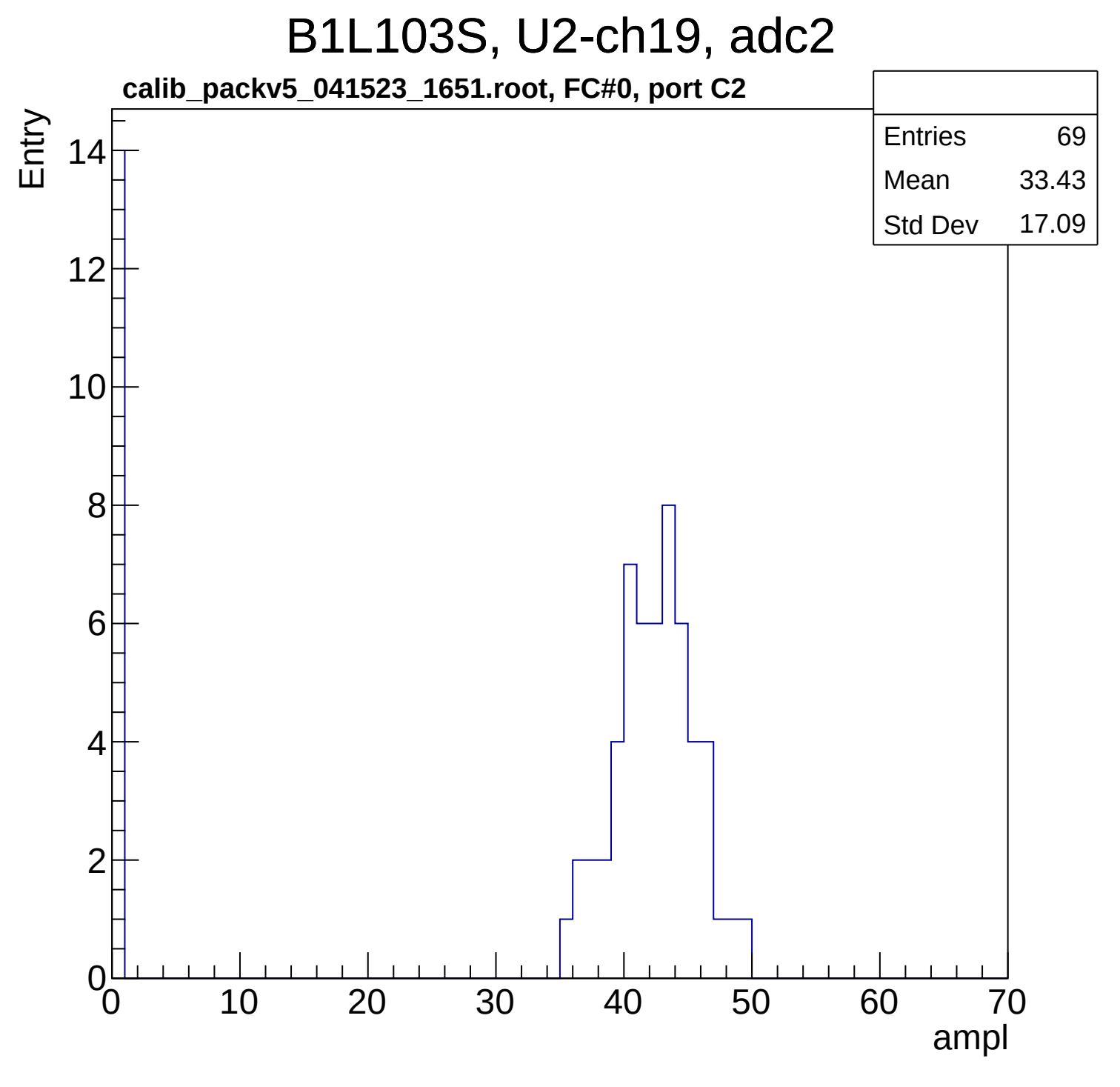

B1L103S, U2-ch18, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.93
Std Dev 8.338
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

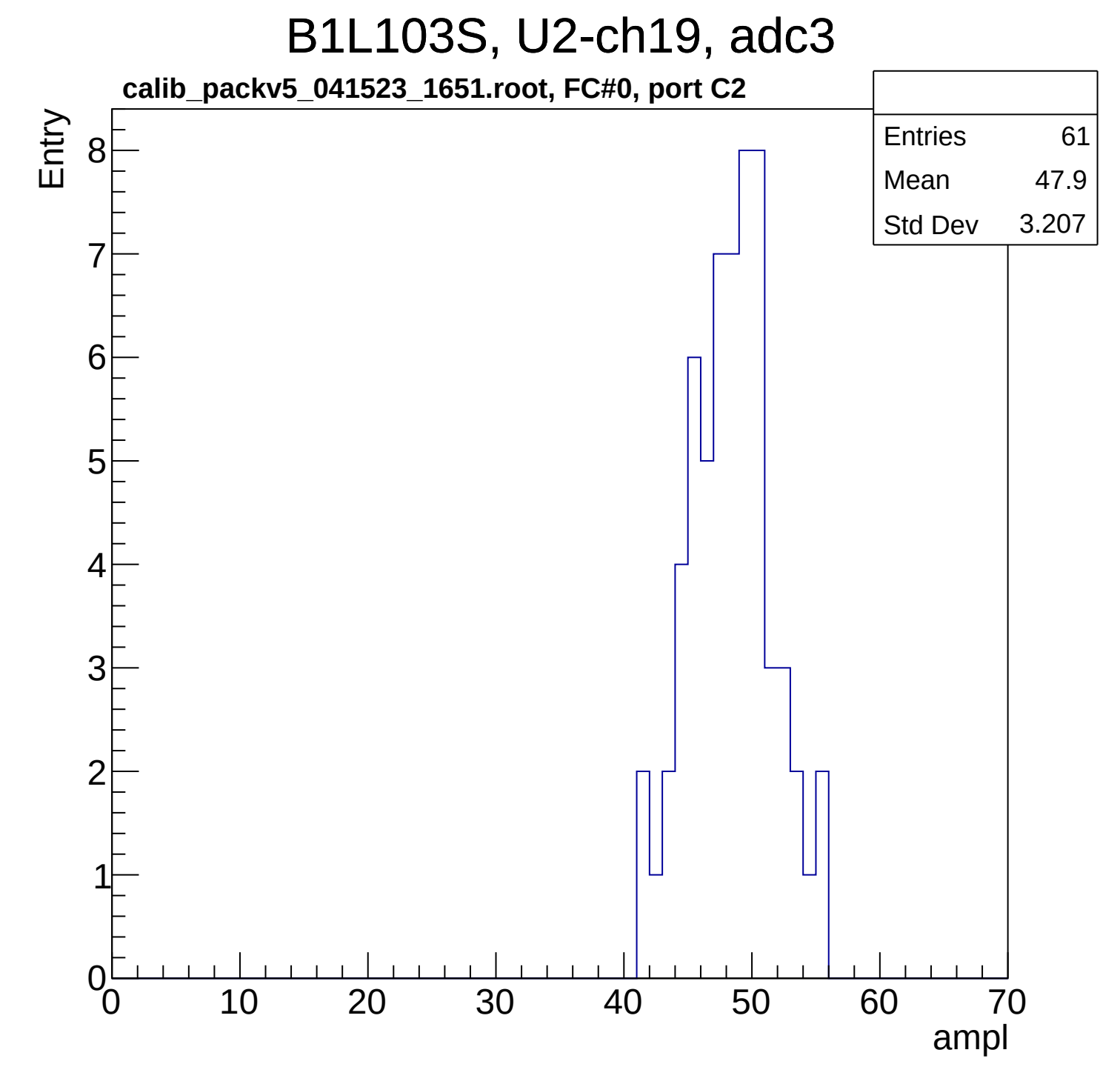

B1L103S, U2-ch18, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 60.75
Std Dev 1.984
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

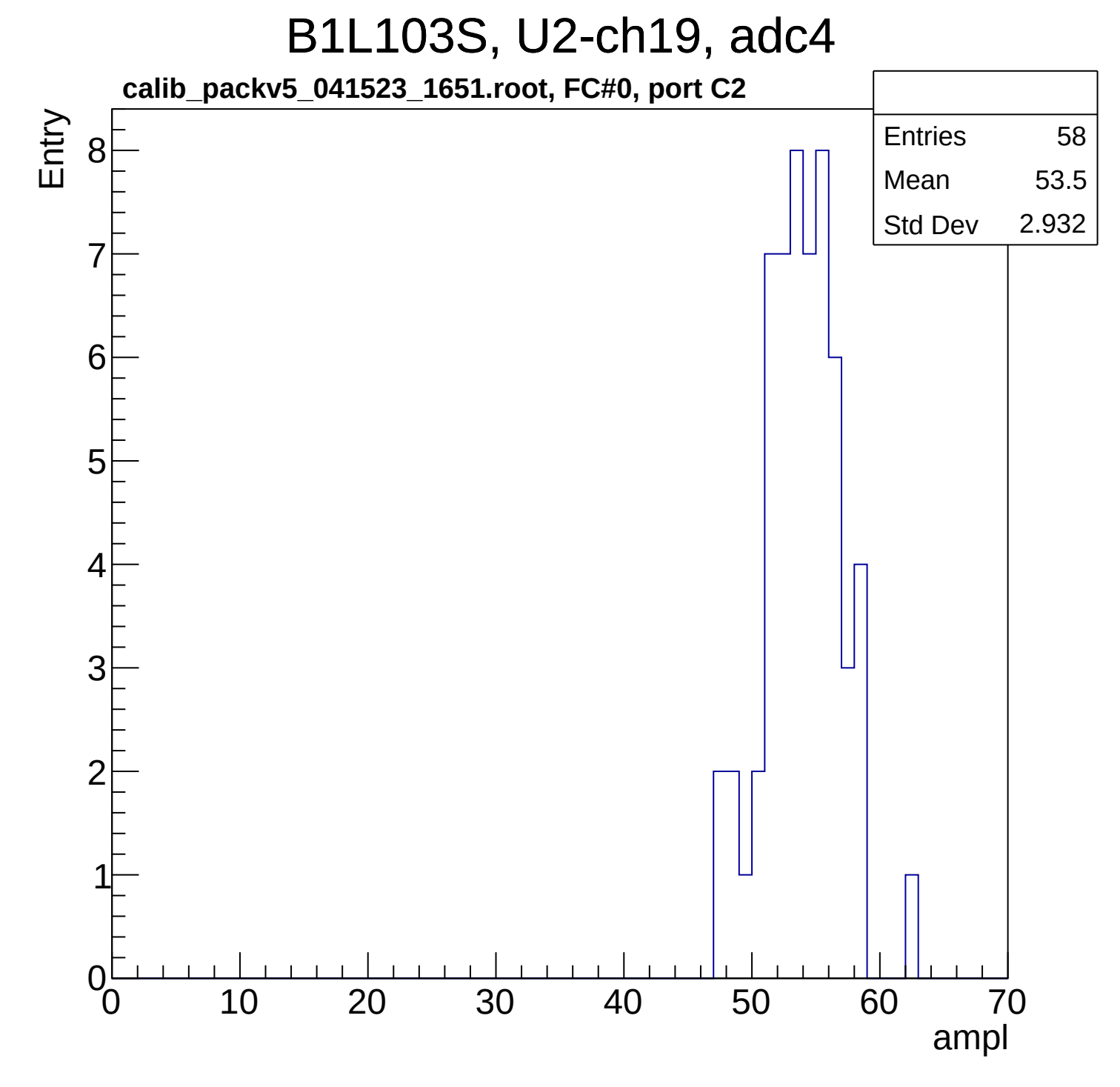

B1L103S, U2-ch18, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

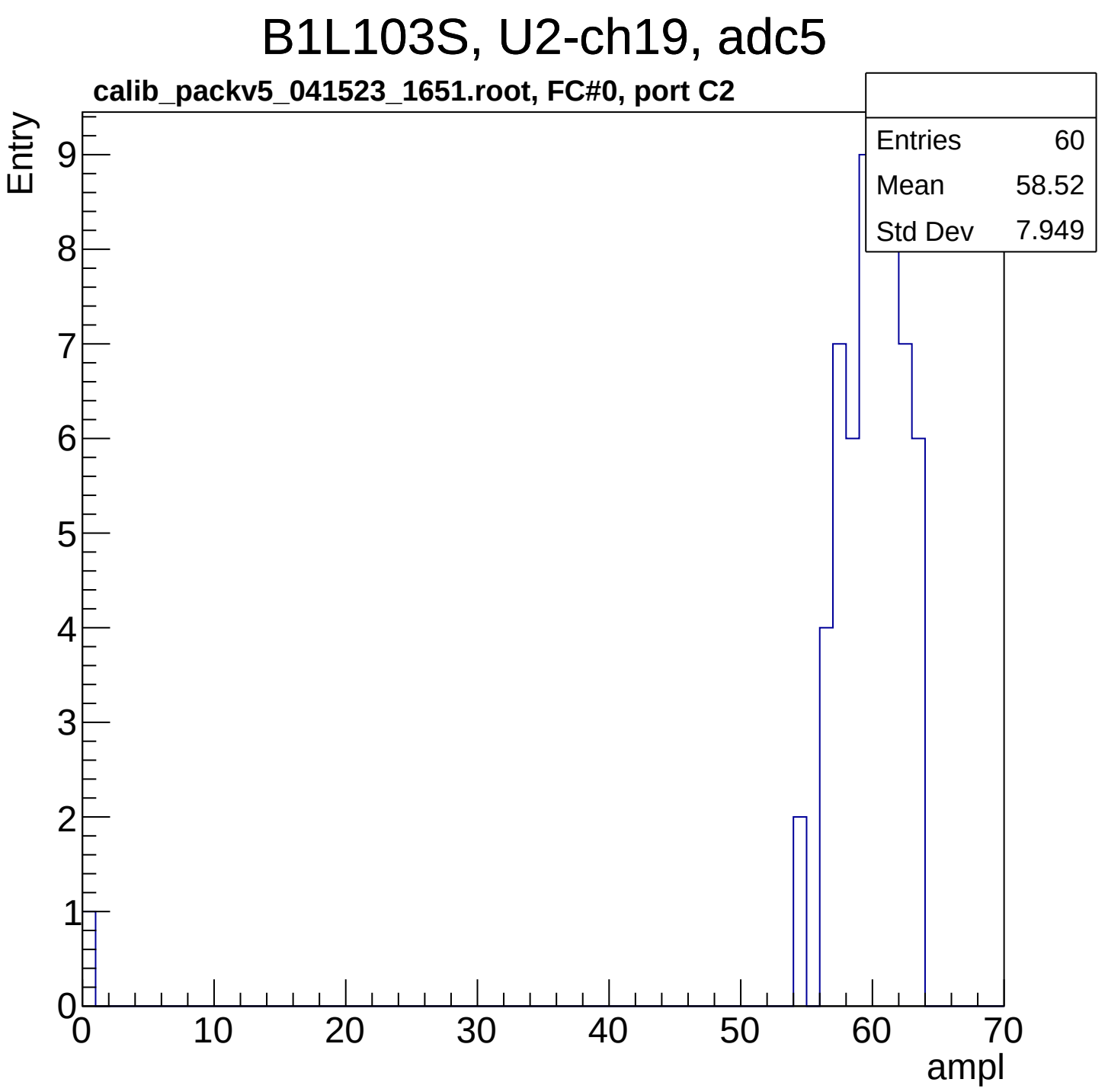

B1L103S, U2-ch19, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 20.19
Std Dev 13.32
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70

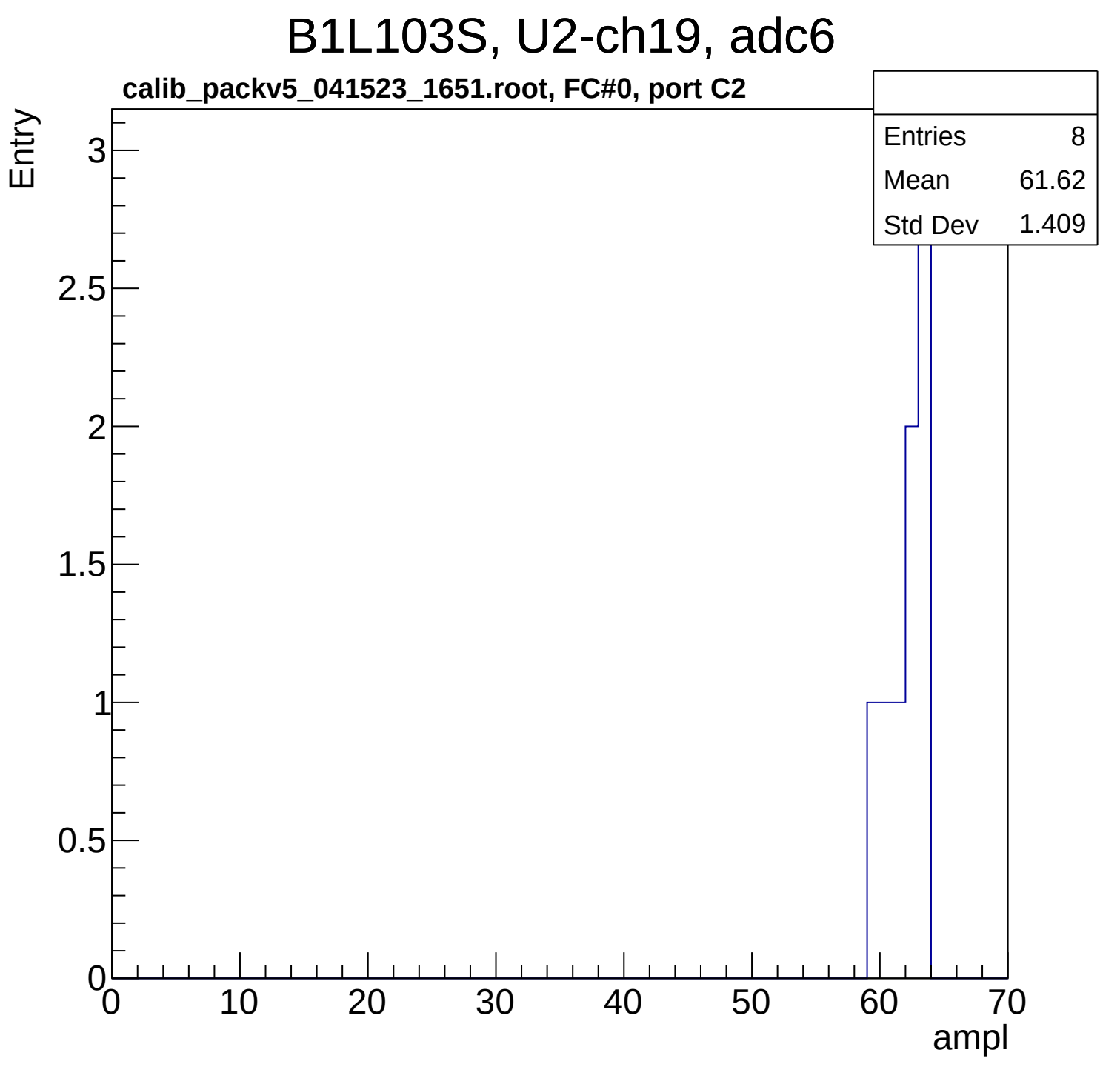

B1L103S, U2-ch19, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 33.16
Std Dev 9.023
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

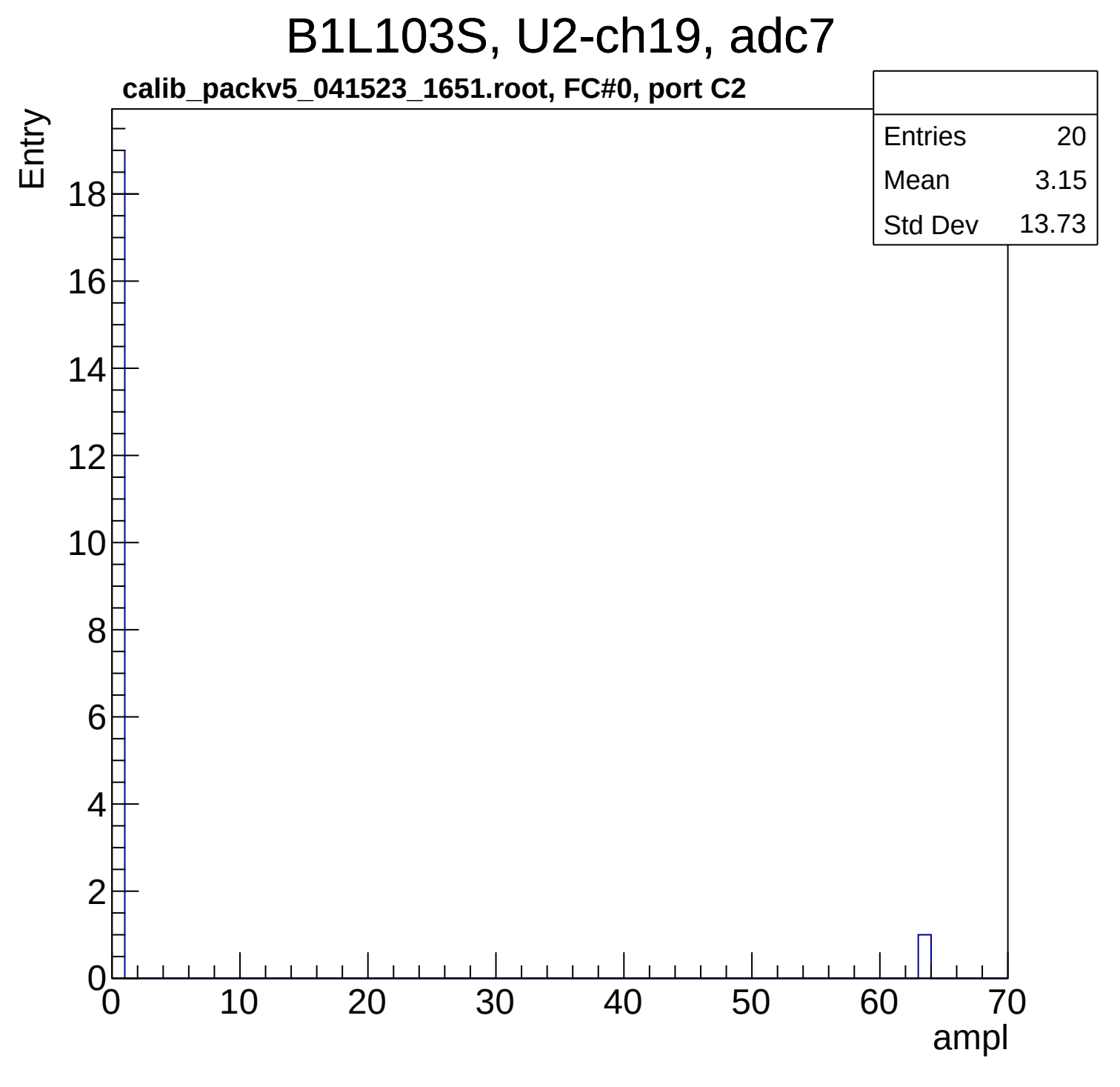

B1L103S, U2-ch19, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 33.43
Std Dev 17.09
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

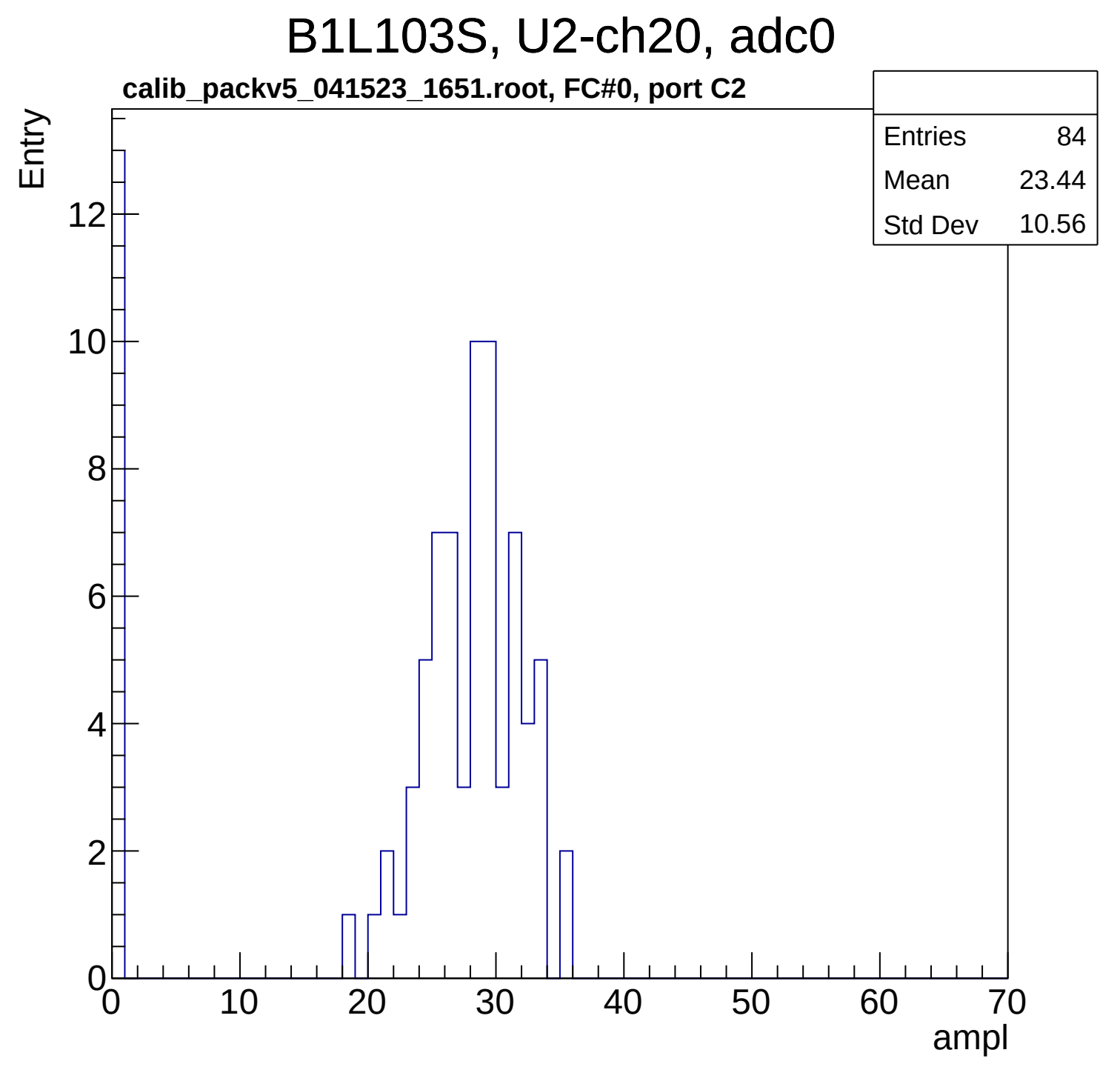

B1L103S, U2-ch19, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 47.9
Std Dev 3.207
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

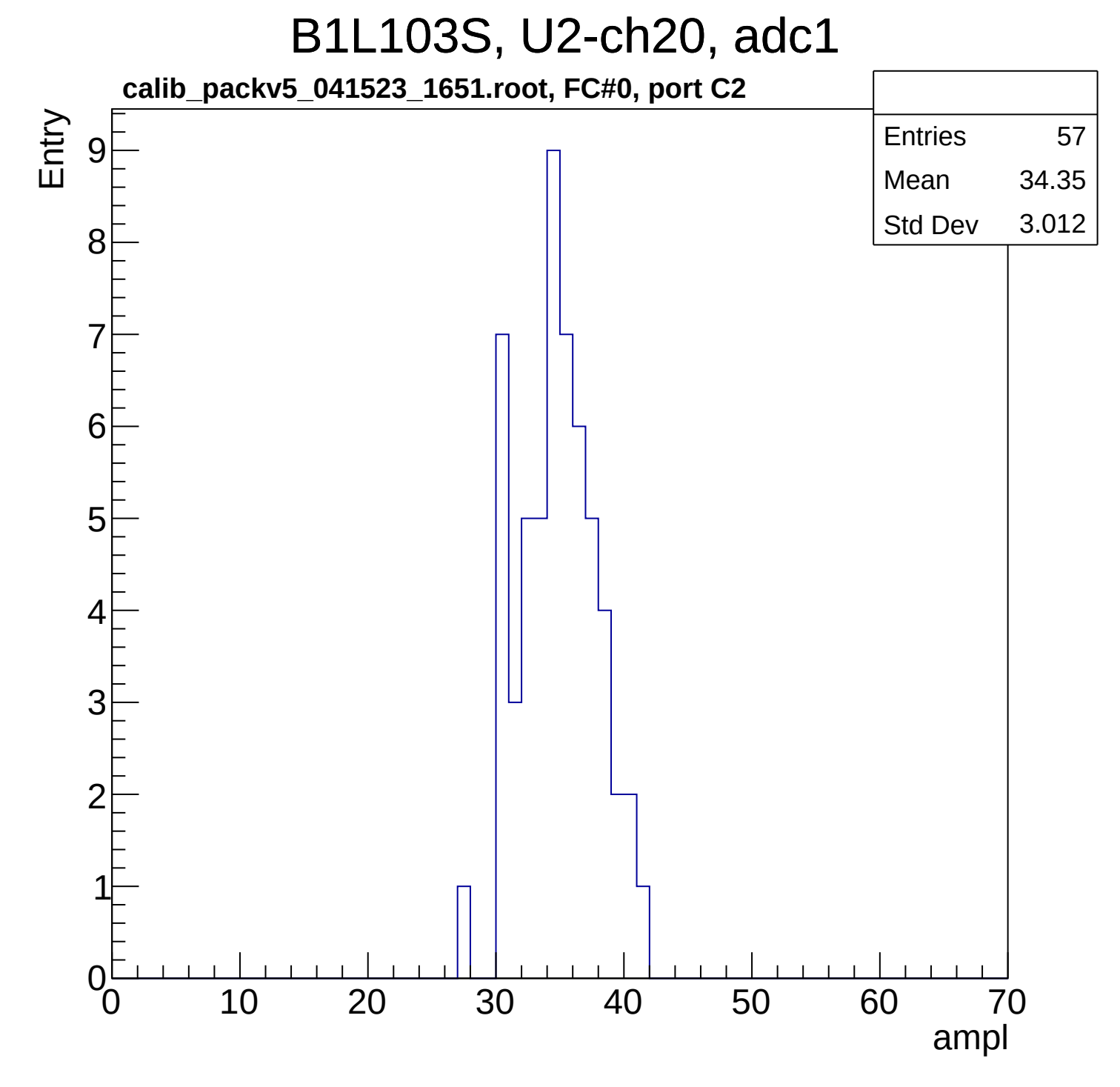

B1L103S, U2-ch19, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 53.5
Std Dev 2.932
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

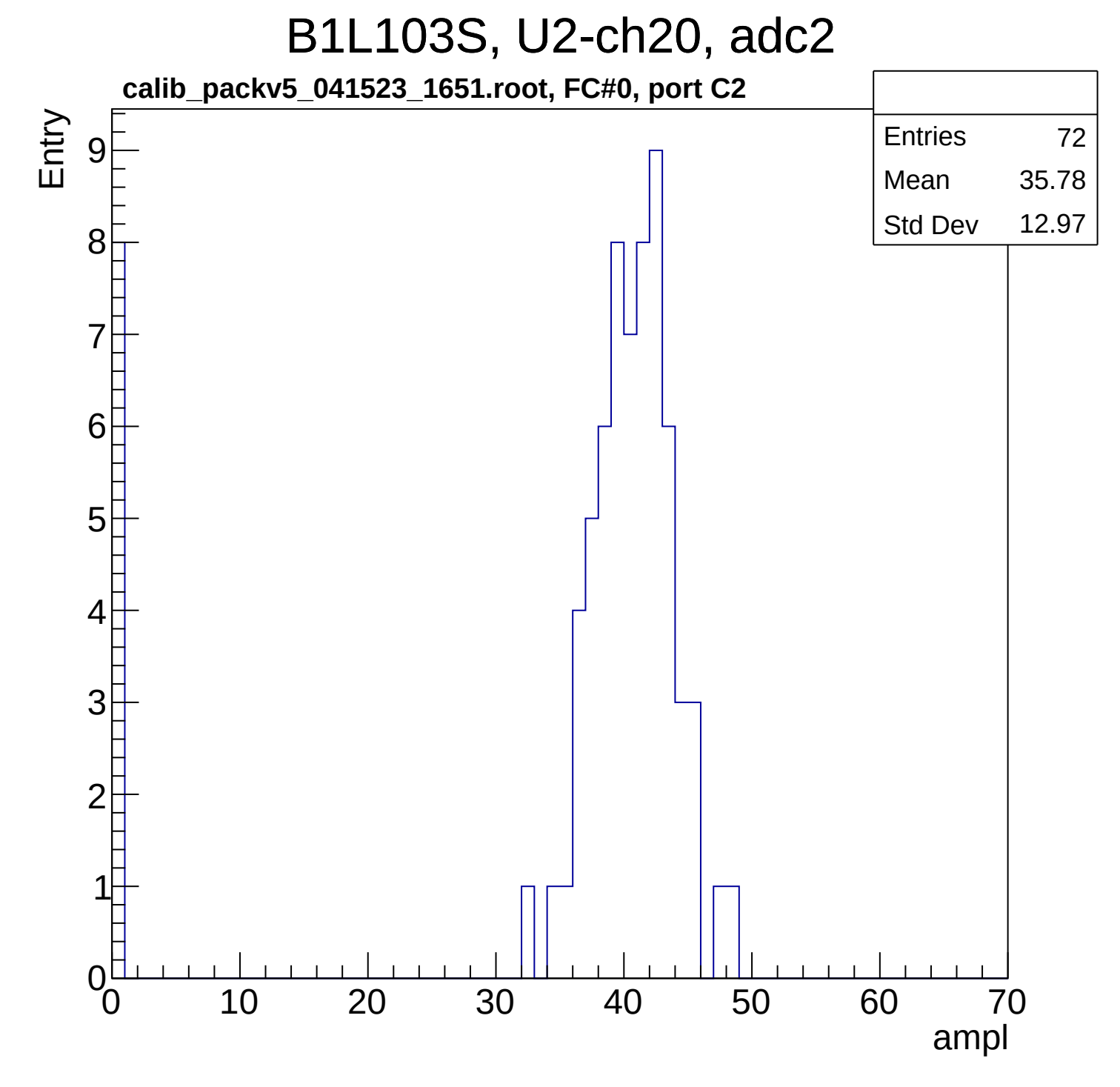

B1L103S, U2-ch19, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 58.52
Std Dev 7.949
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

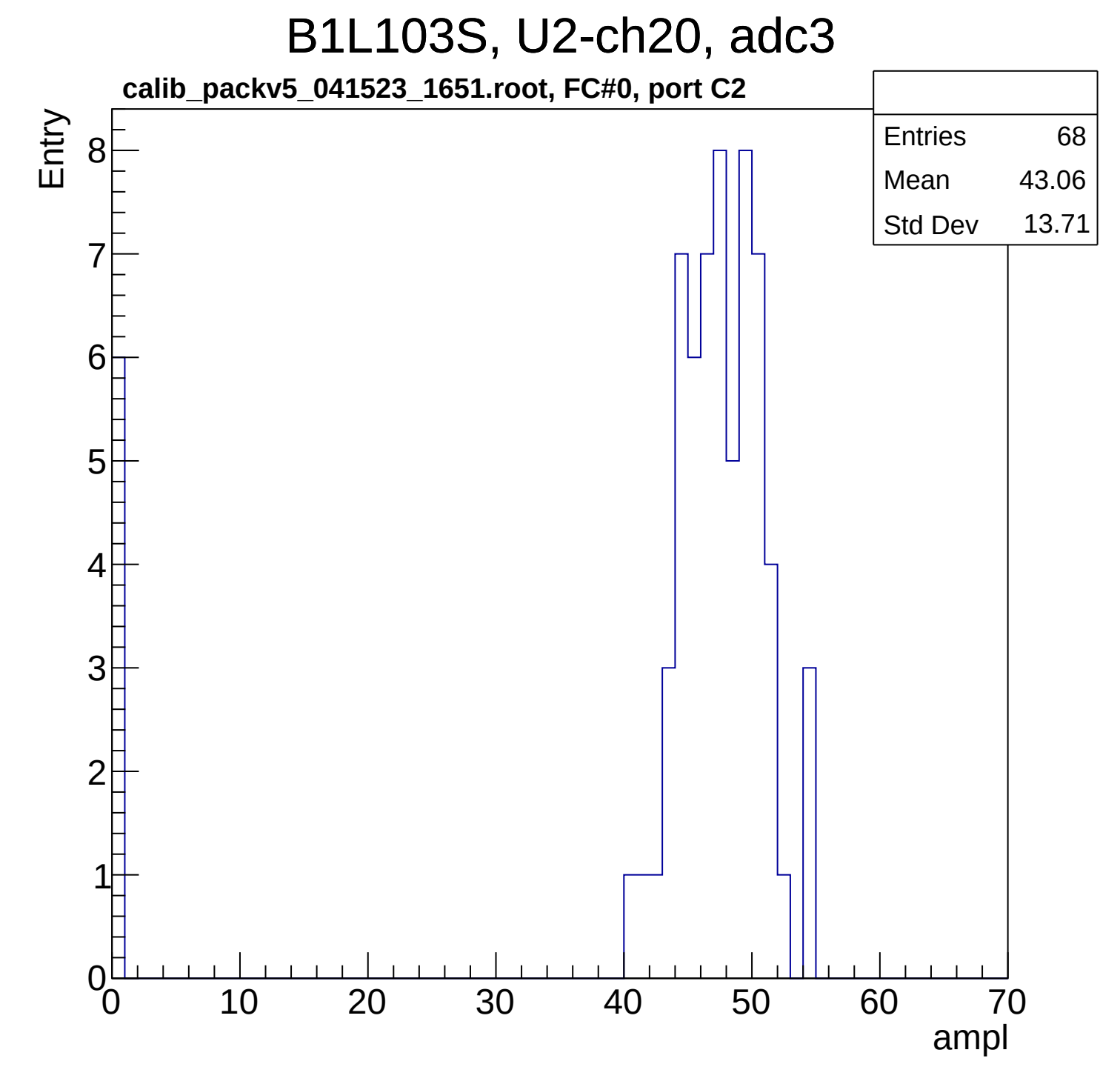

B1L103S, U2-ch19, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.62
Std Dev 1.409
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

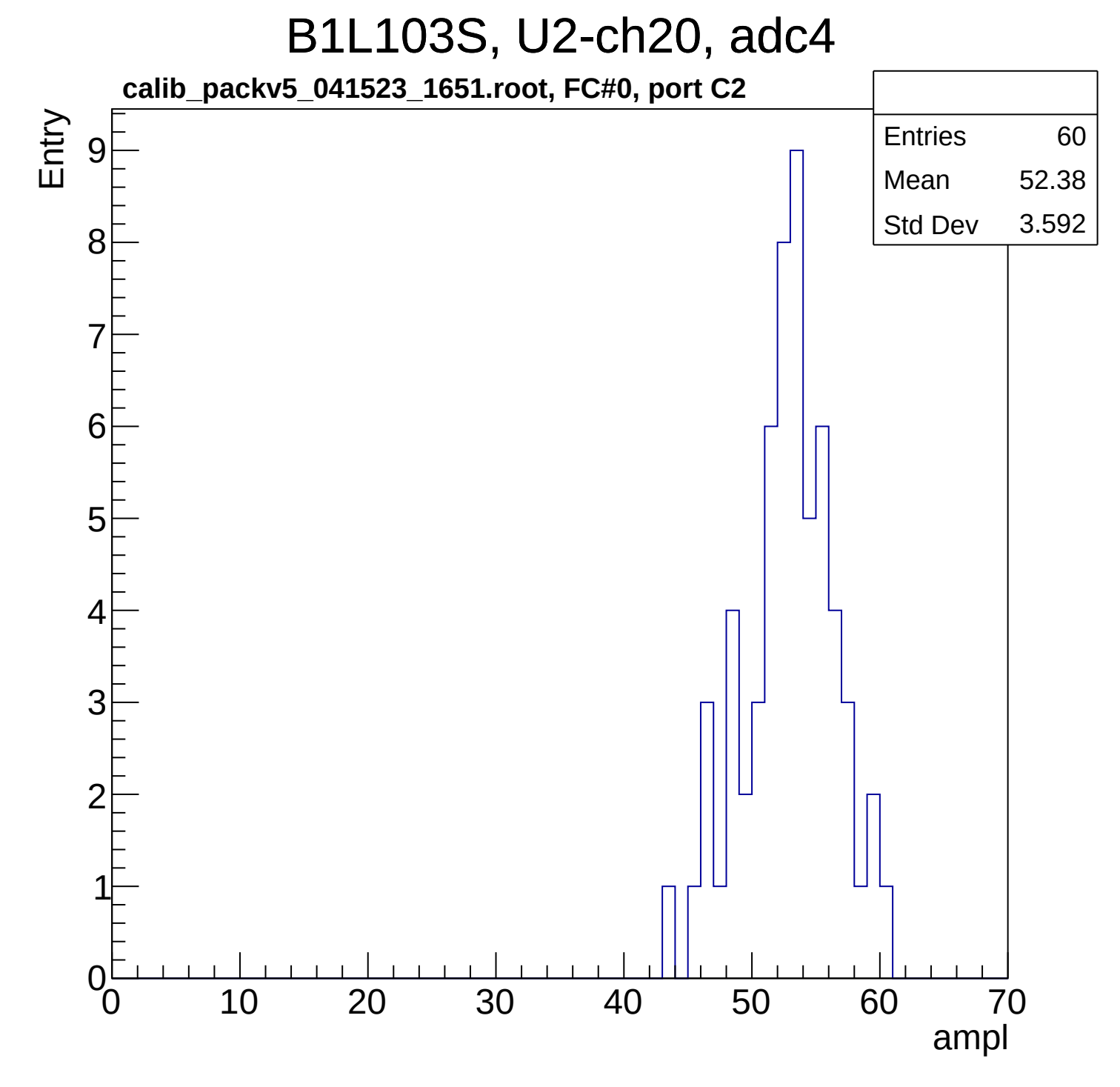

B1L103S, U2-ch19, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

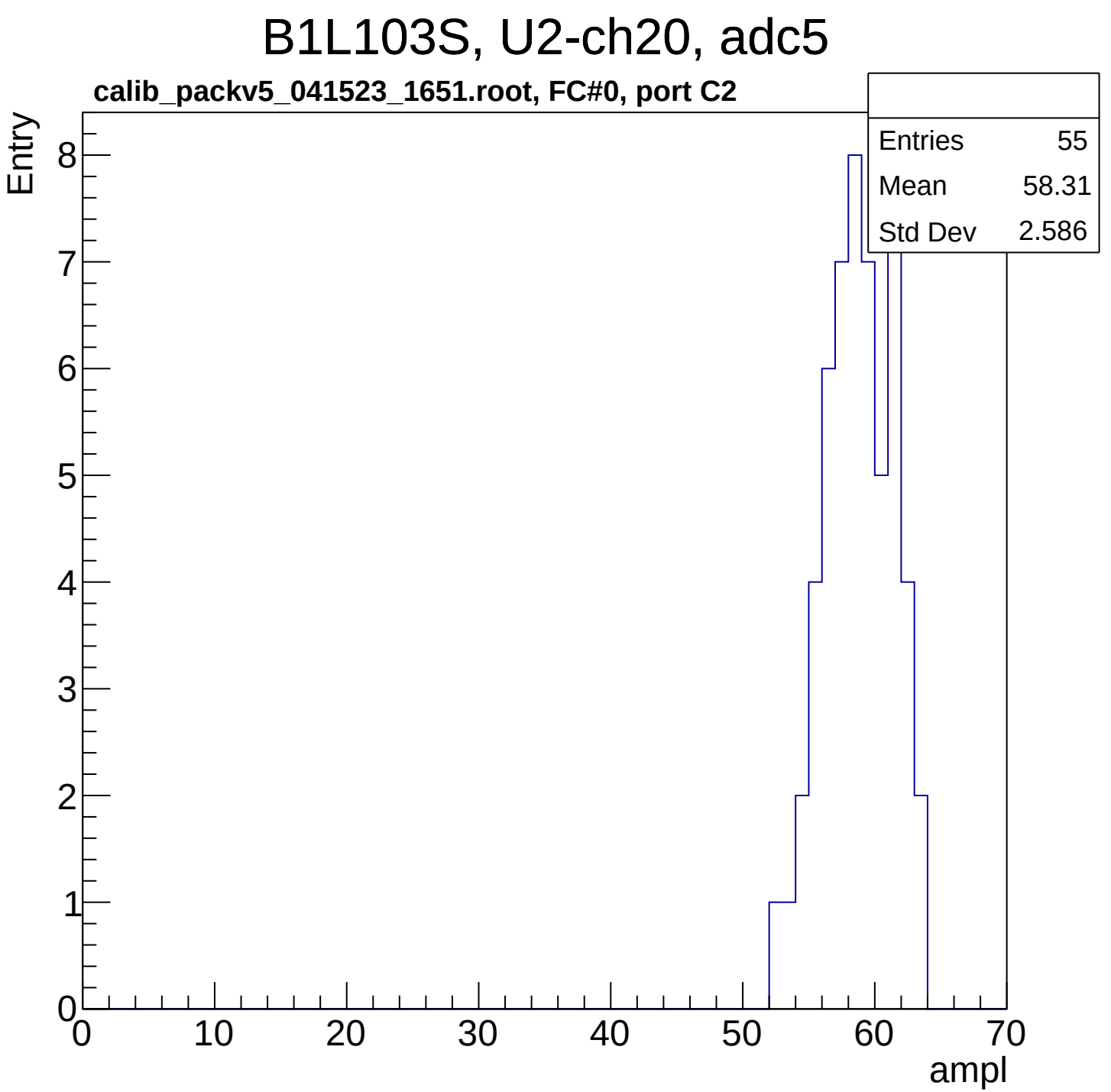

B1L103S, U2-ch20, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 23.44
Std Dev 10.56
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70

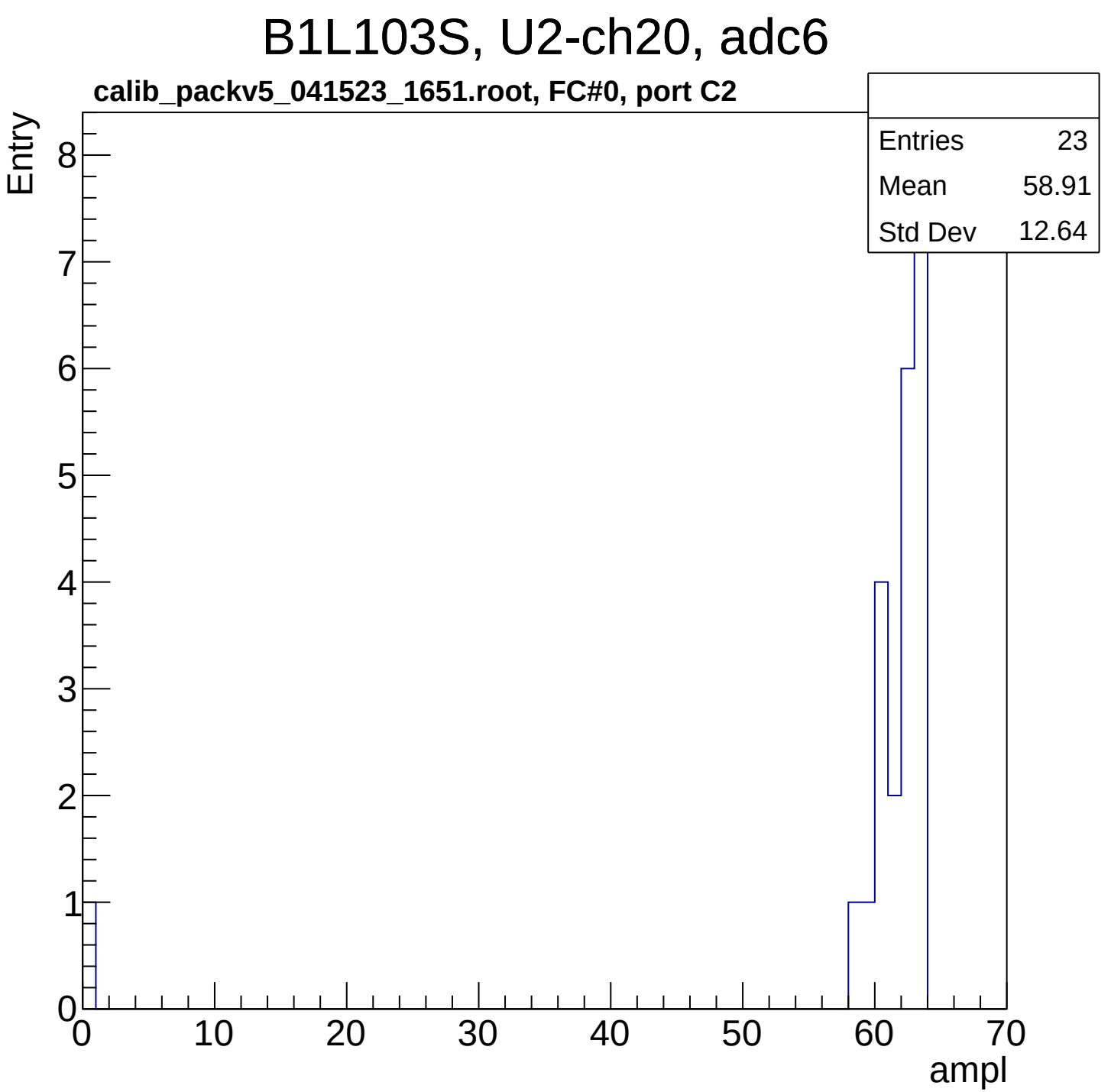

B1L103S, U2-ch20, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 34.35
Std Dev 3.012
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

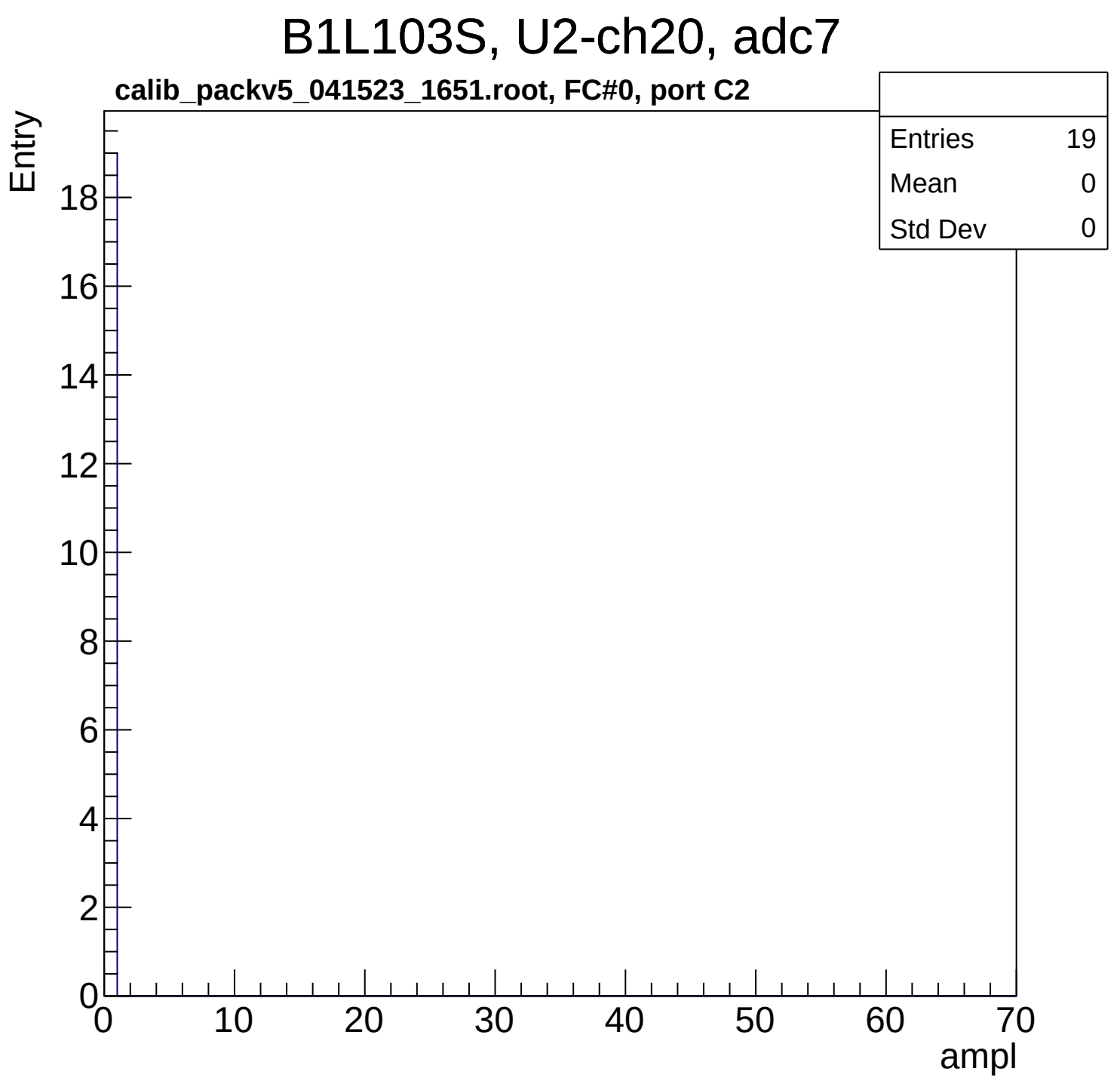

B1L103S, U2-ch20, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 35.78
Std Dev 12.97
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

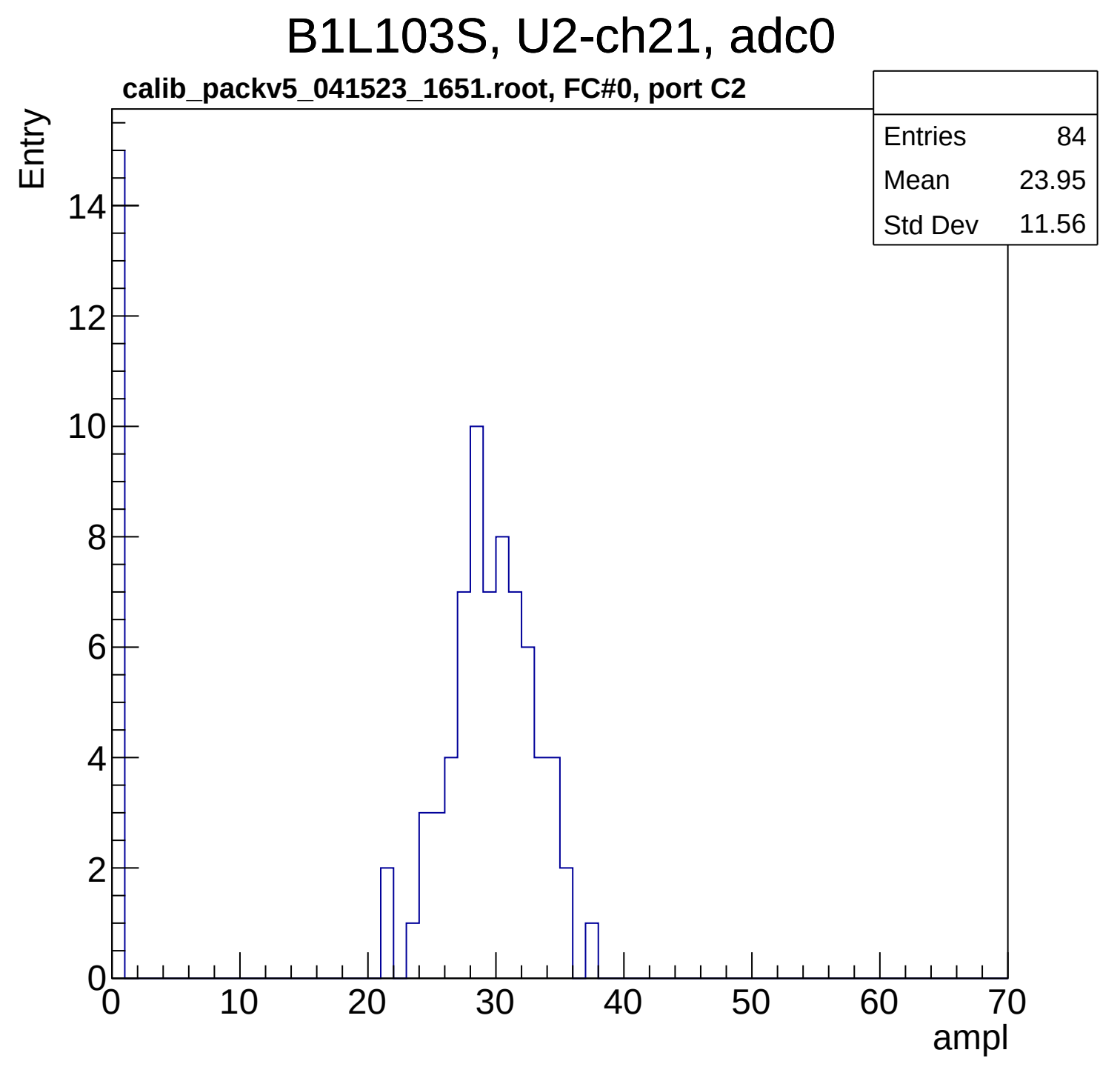

B1L103S, U2-ch20, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 43.06
Std Dev 13.71
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

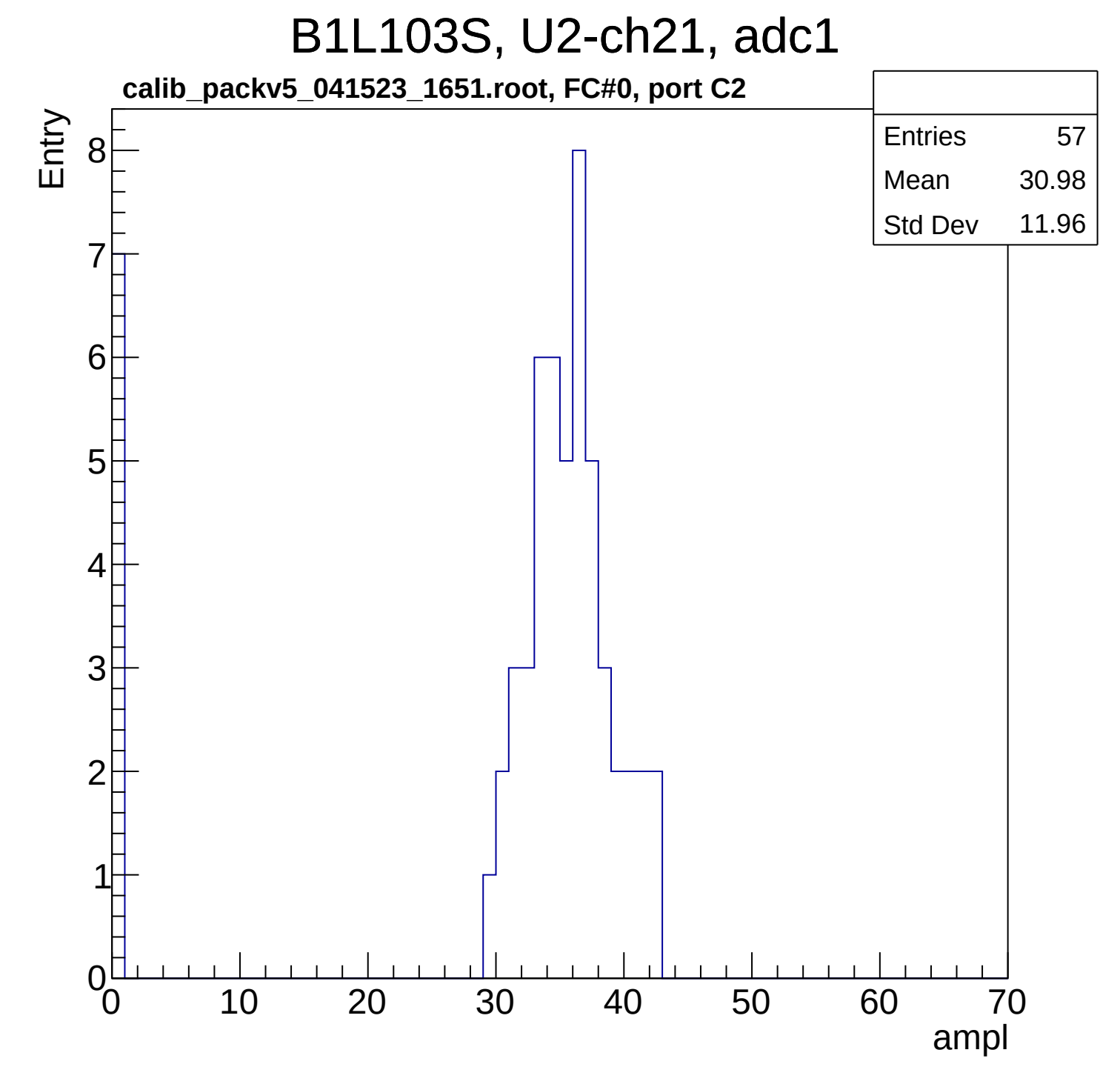

B1L103S, U2-ch20, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 52.38
Std Dev 3.592
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

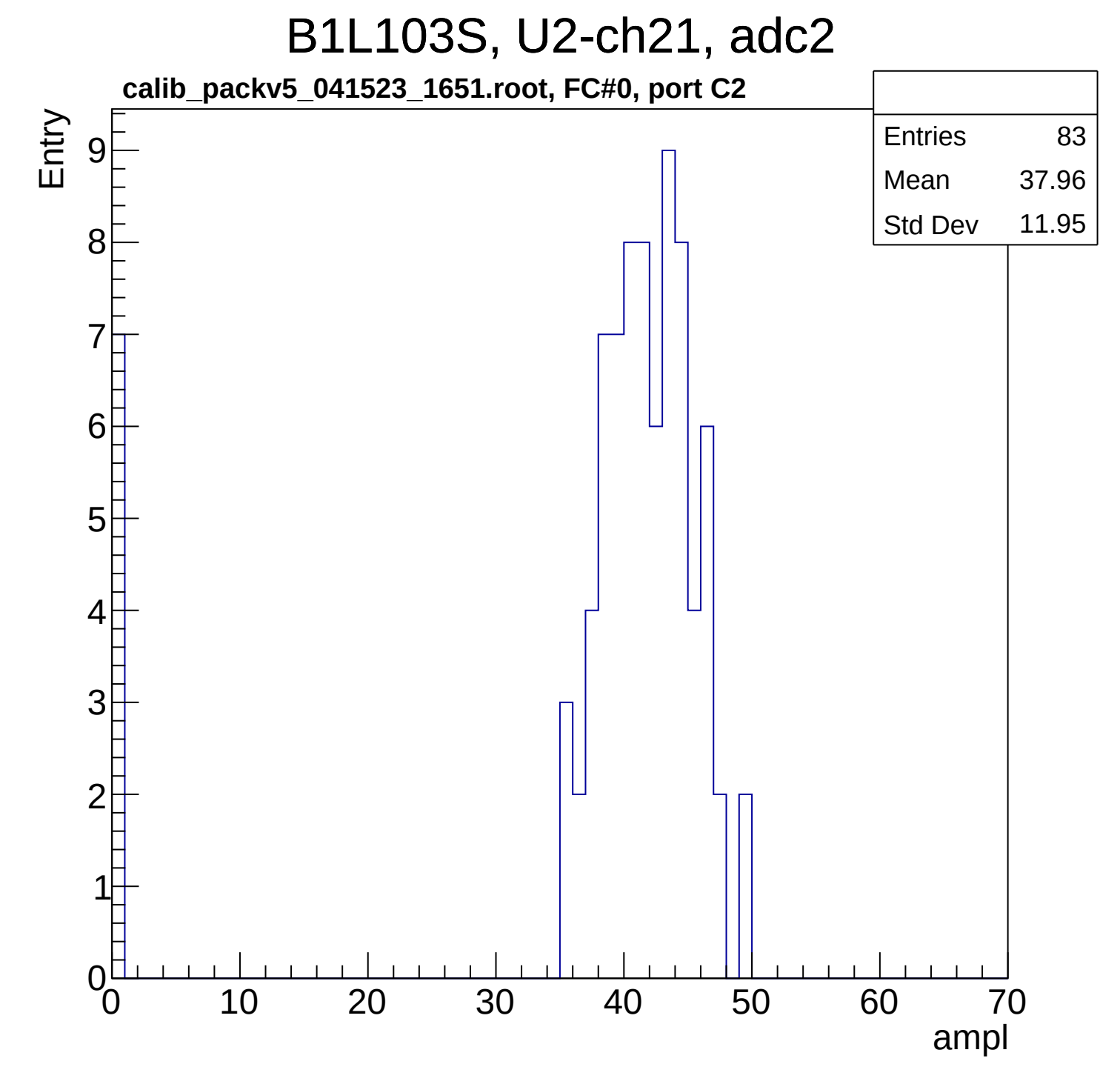

B1L103S, U2-ch20, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.31
Std Dev 2.586
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

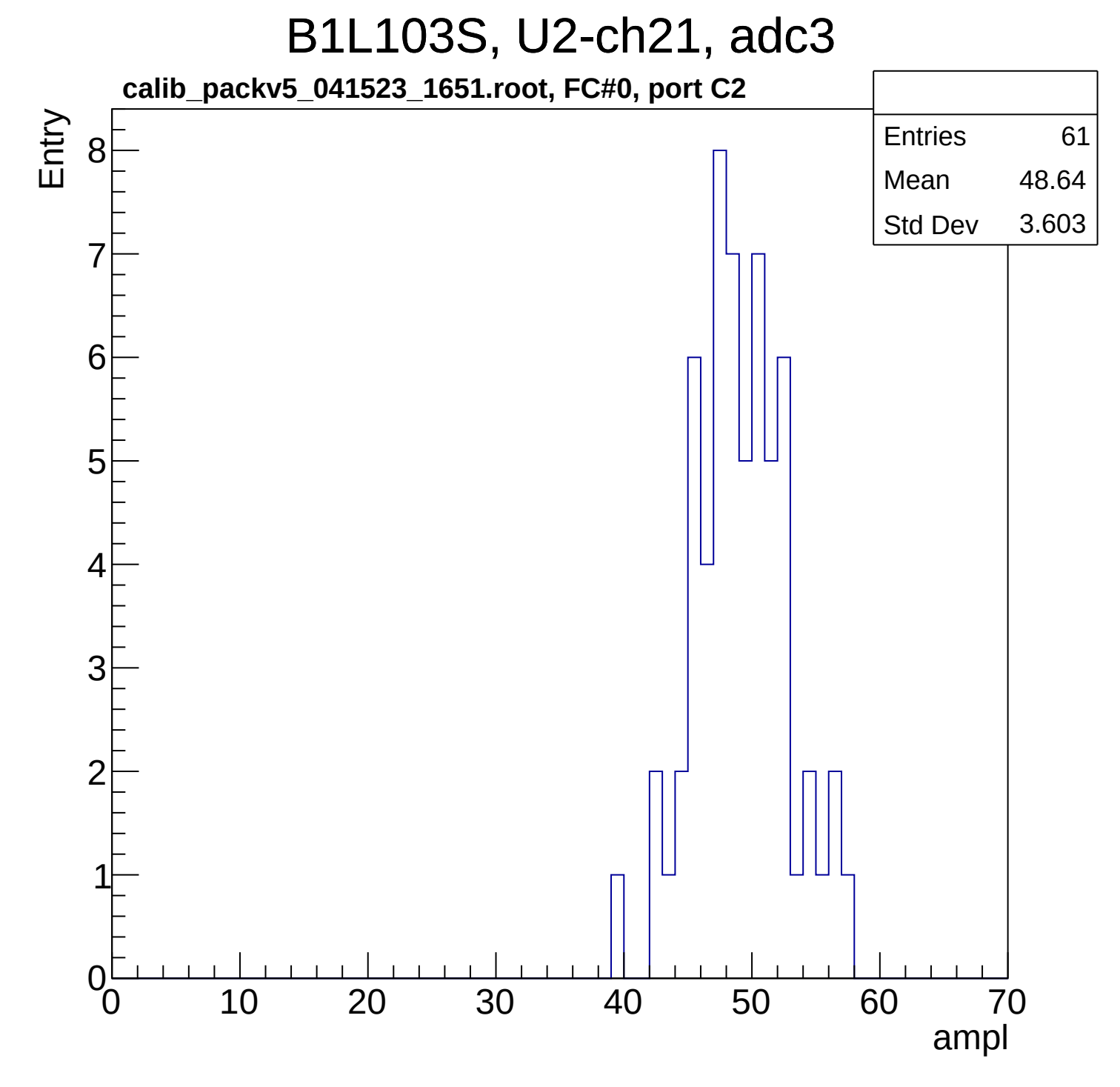

B1L103S, U2-ch20, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 58.91
Std Dev 12.64
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

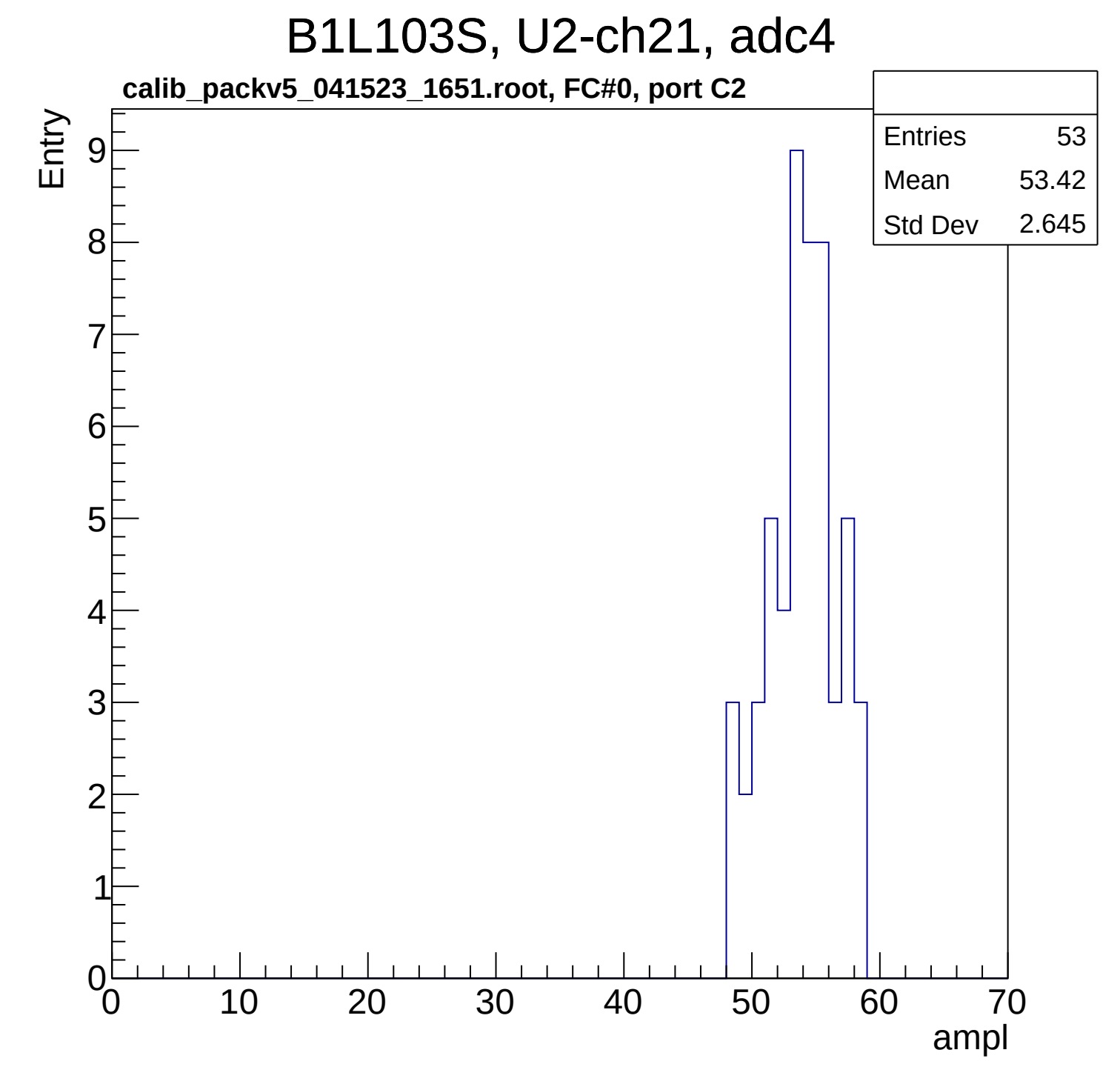

B1L103S, U2-ch20, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

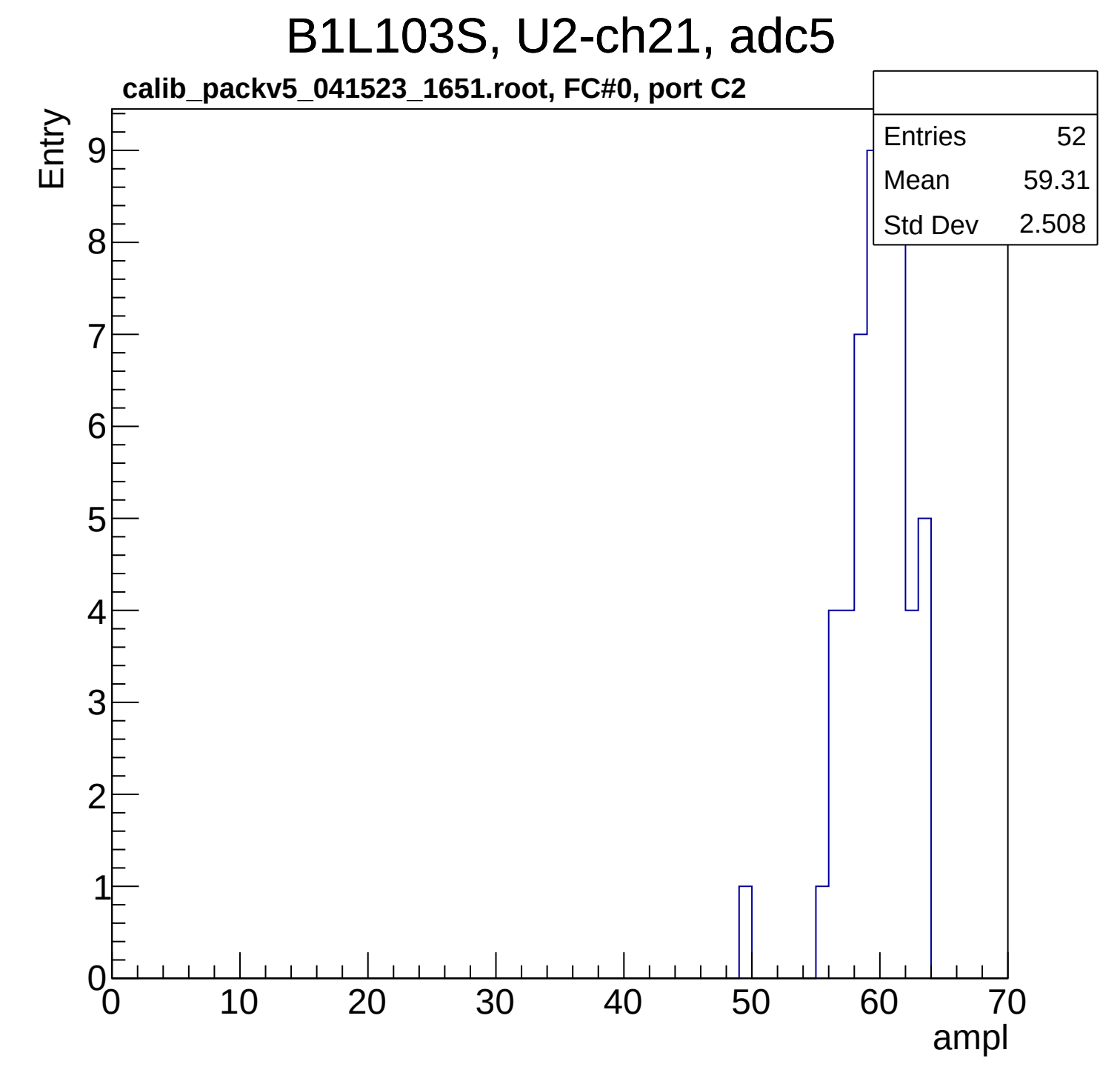

B1L103S, U2-ch21, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 23.95
Std Dev 11.56
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

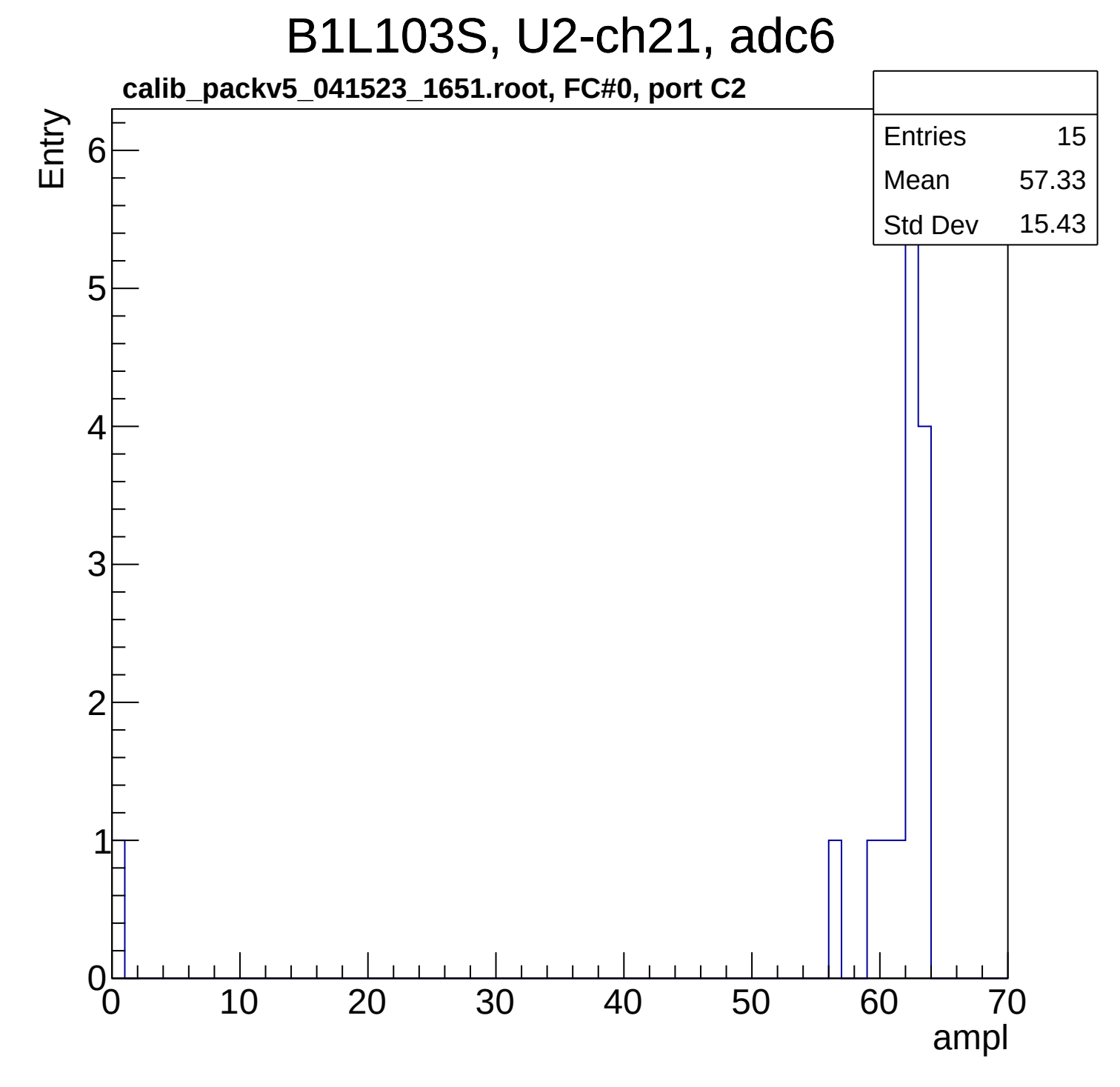

B1L103S, U2-ch21, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 30.98
Std Dev 11.96
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

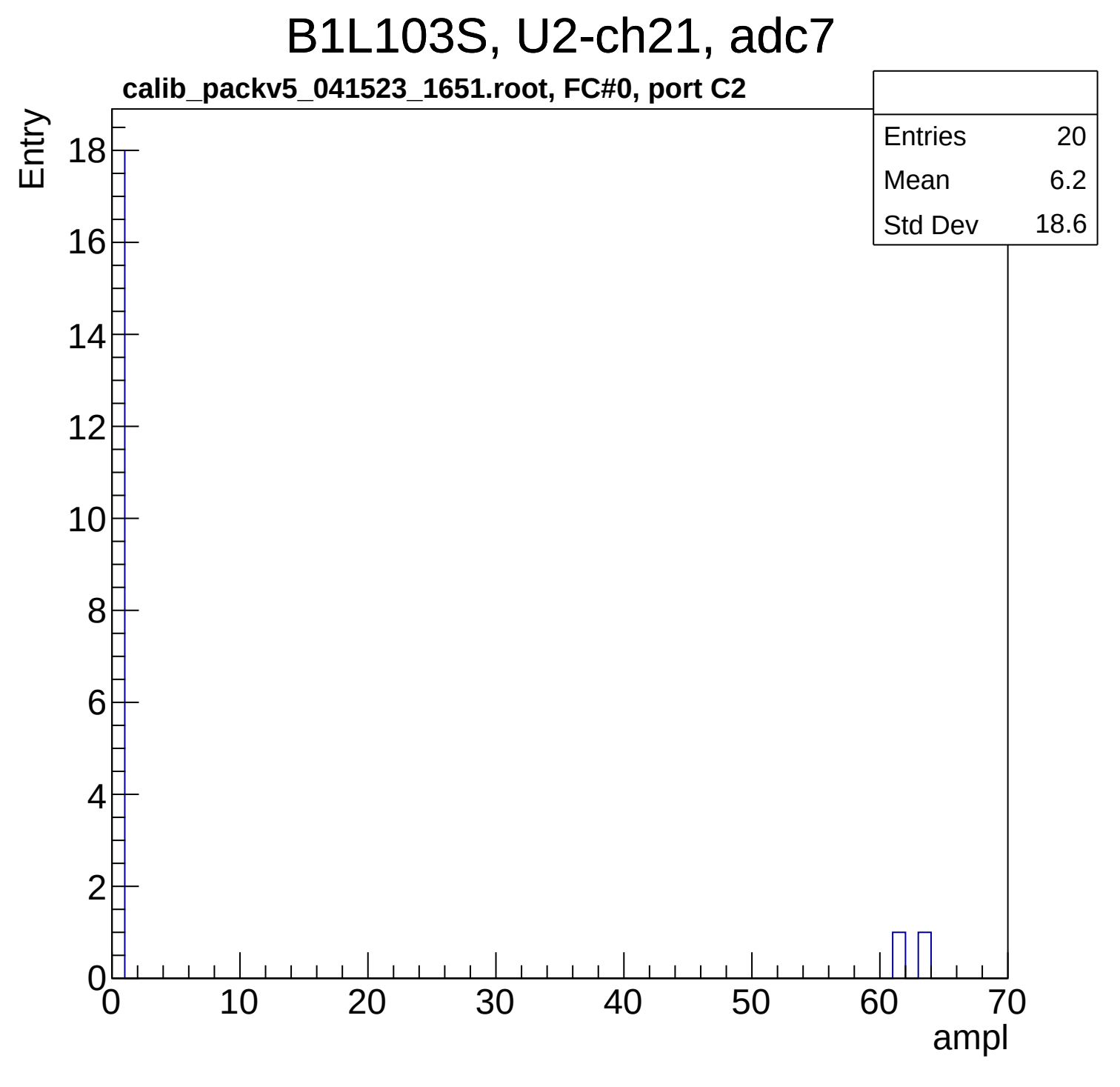

B1L103S, U2-ch21, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 37.96
Std Dev 11.95
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

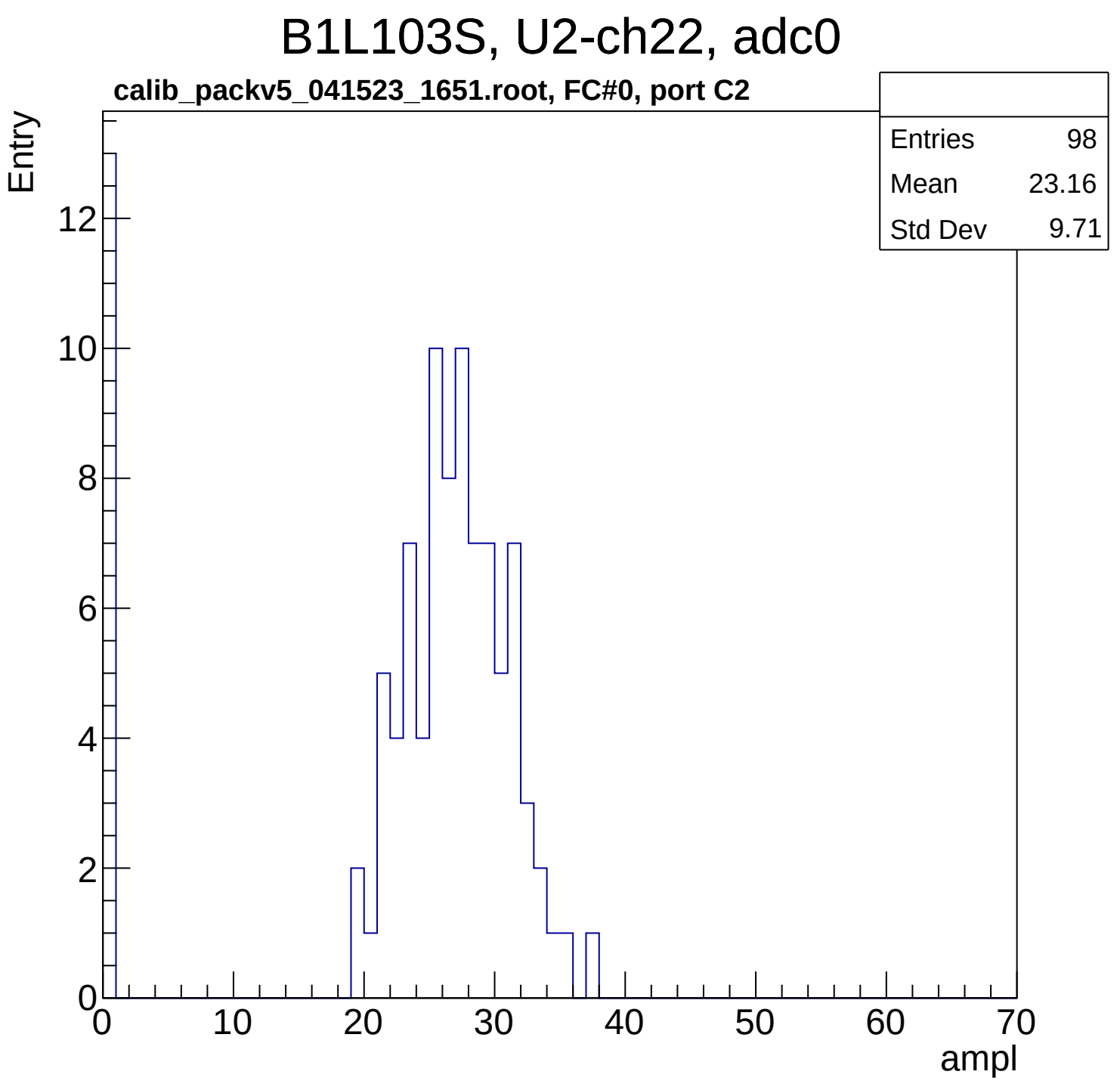

B1L103S, U2-ch21, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 48.64
Std Dev 3.603
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

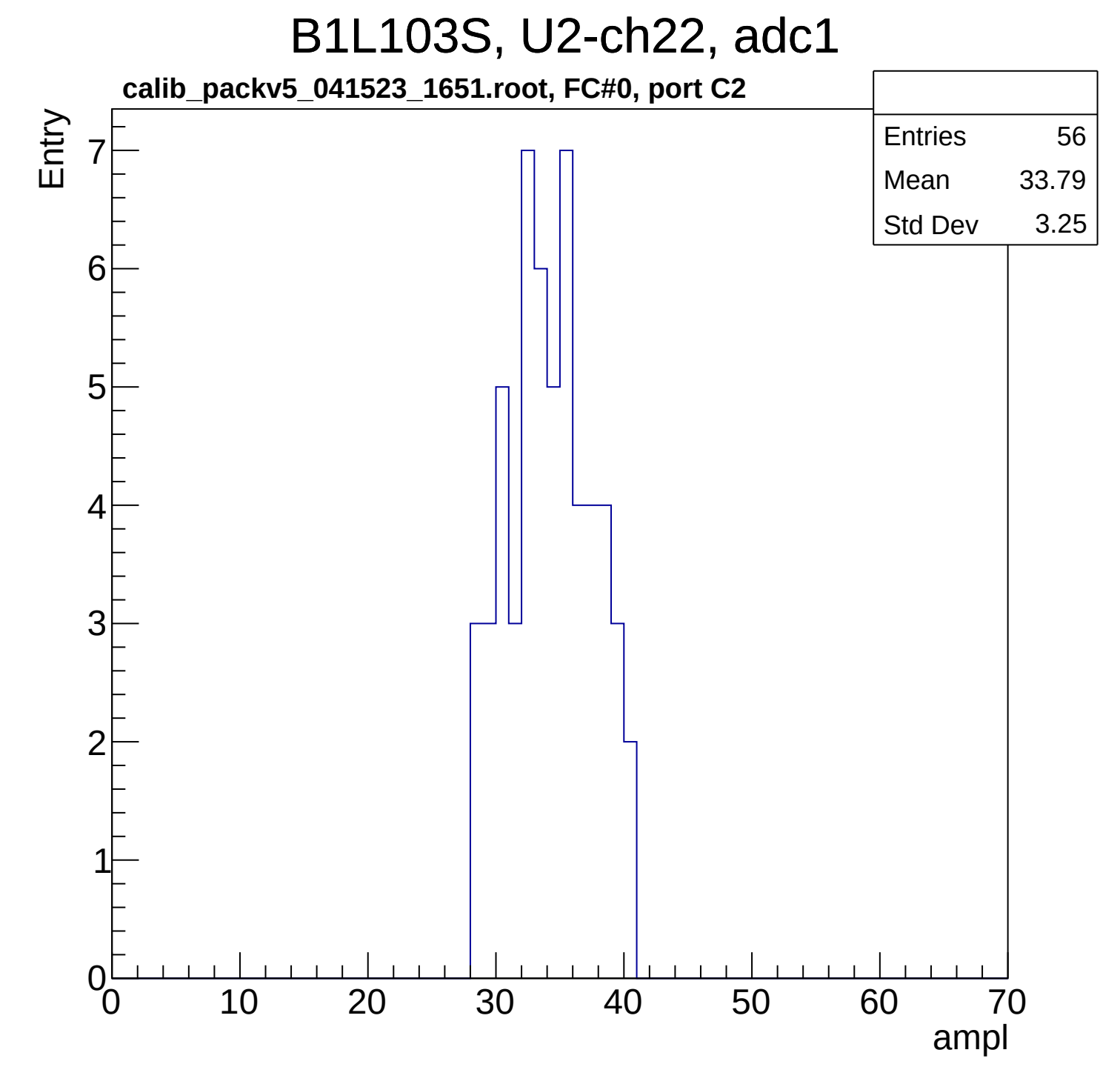

B1L103S, U2-ch21, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 53.42
Std Dev 2.645
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

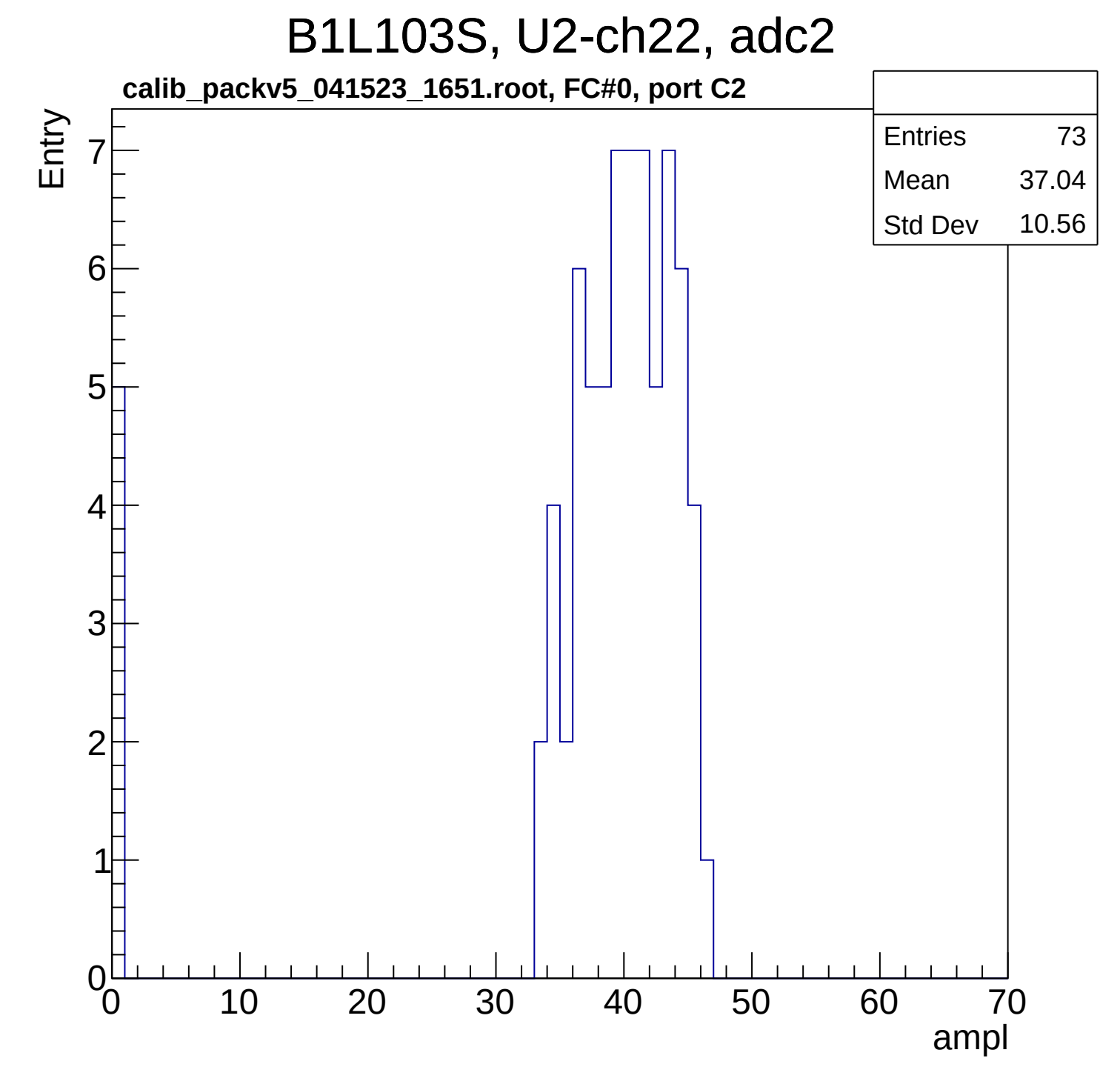

B1L103S, U2-ch21, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 59.31
Std Dev 2.508
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

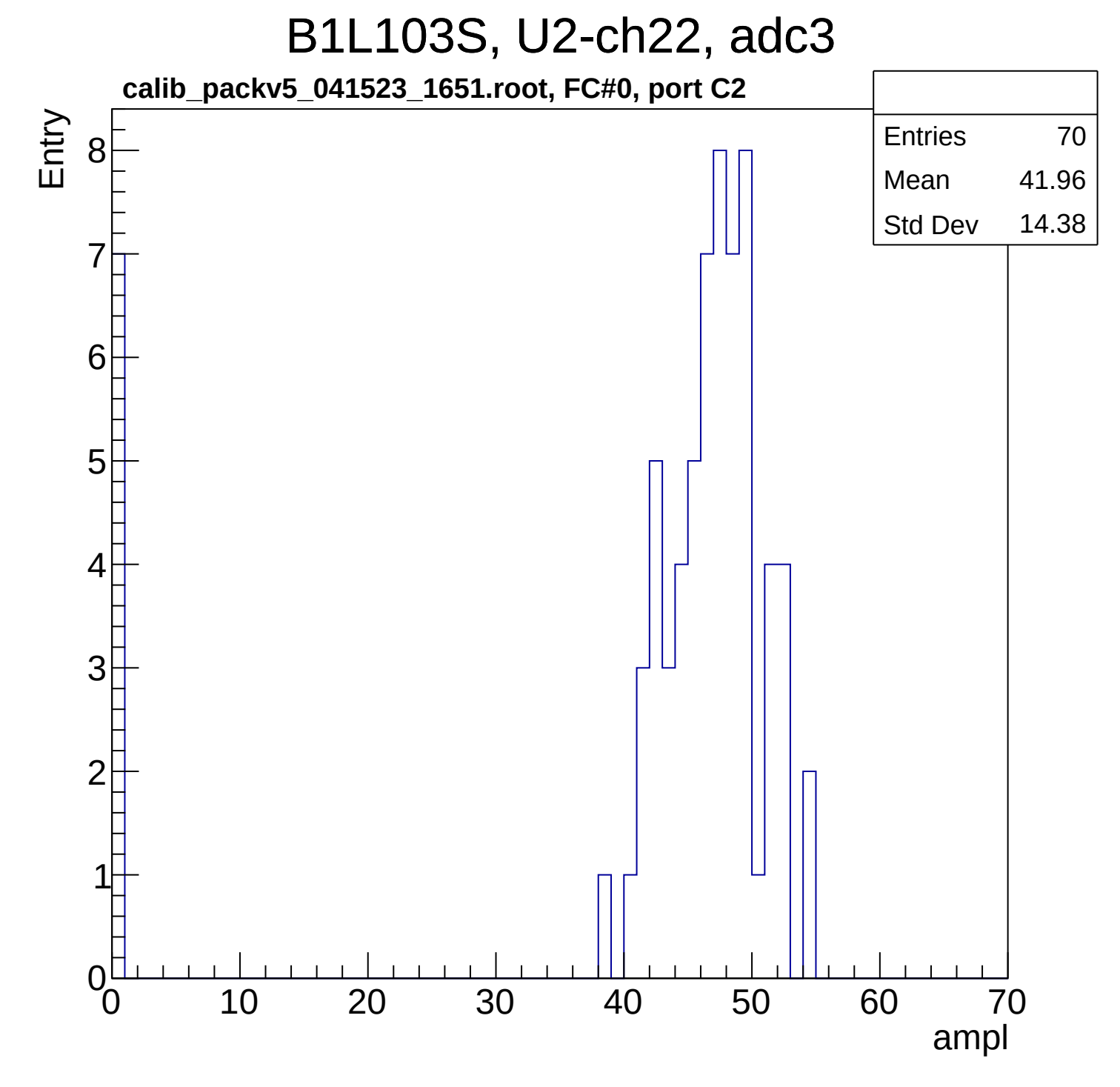

B1L103S, U2-ch21, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.33
Std Dev 15.43
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

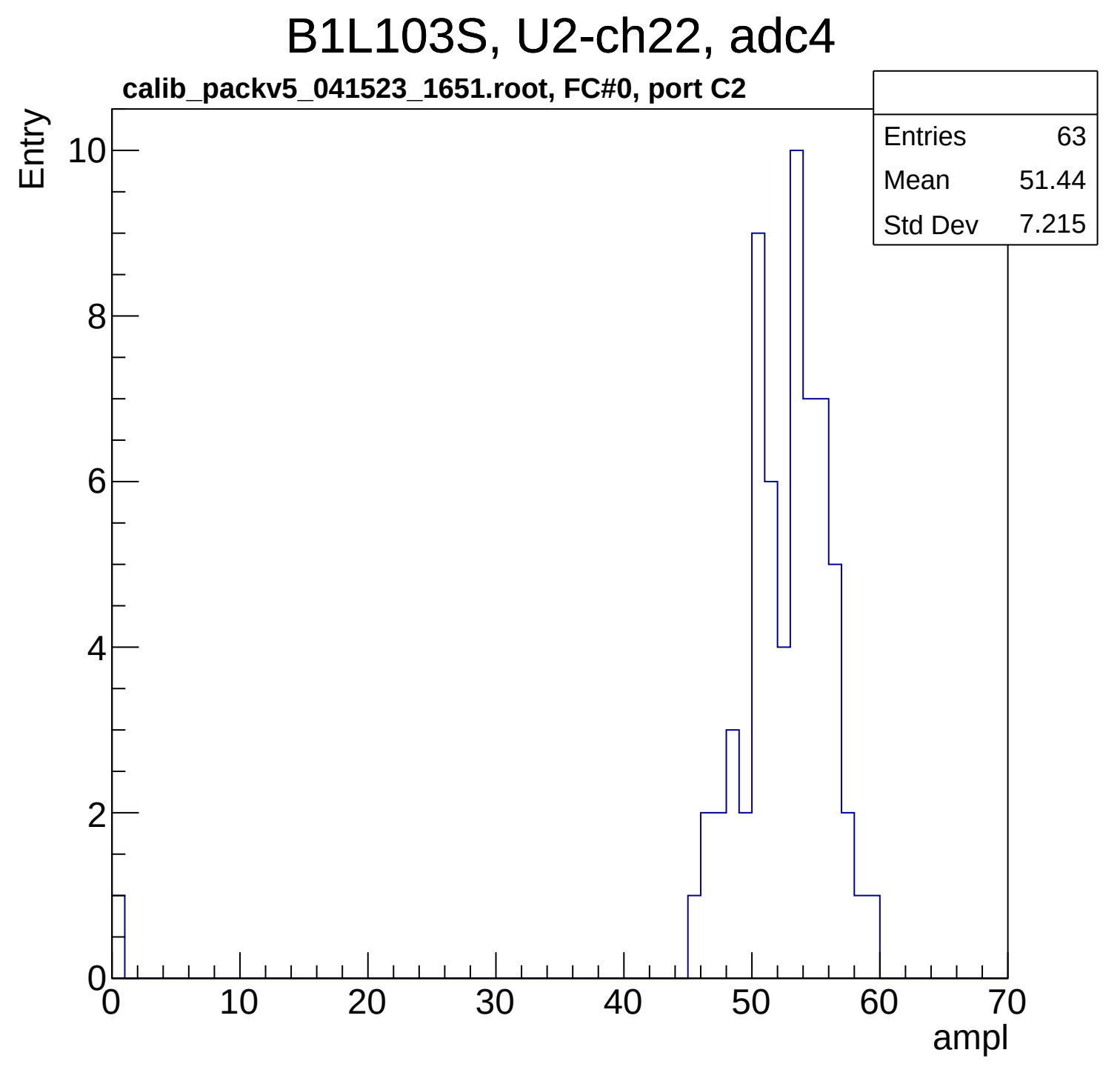

B1L103S, U2-ch21, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.2
Std Dev 18.6
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

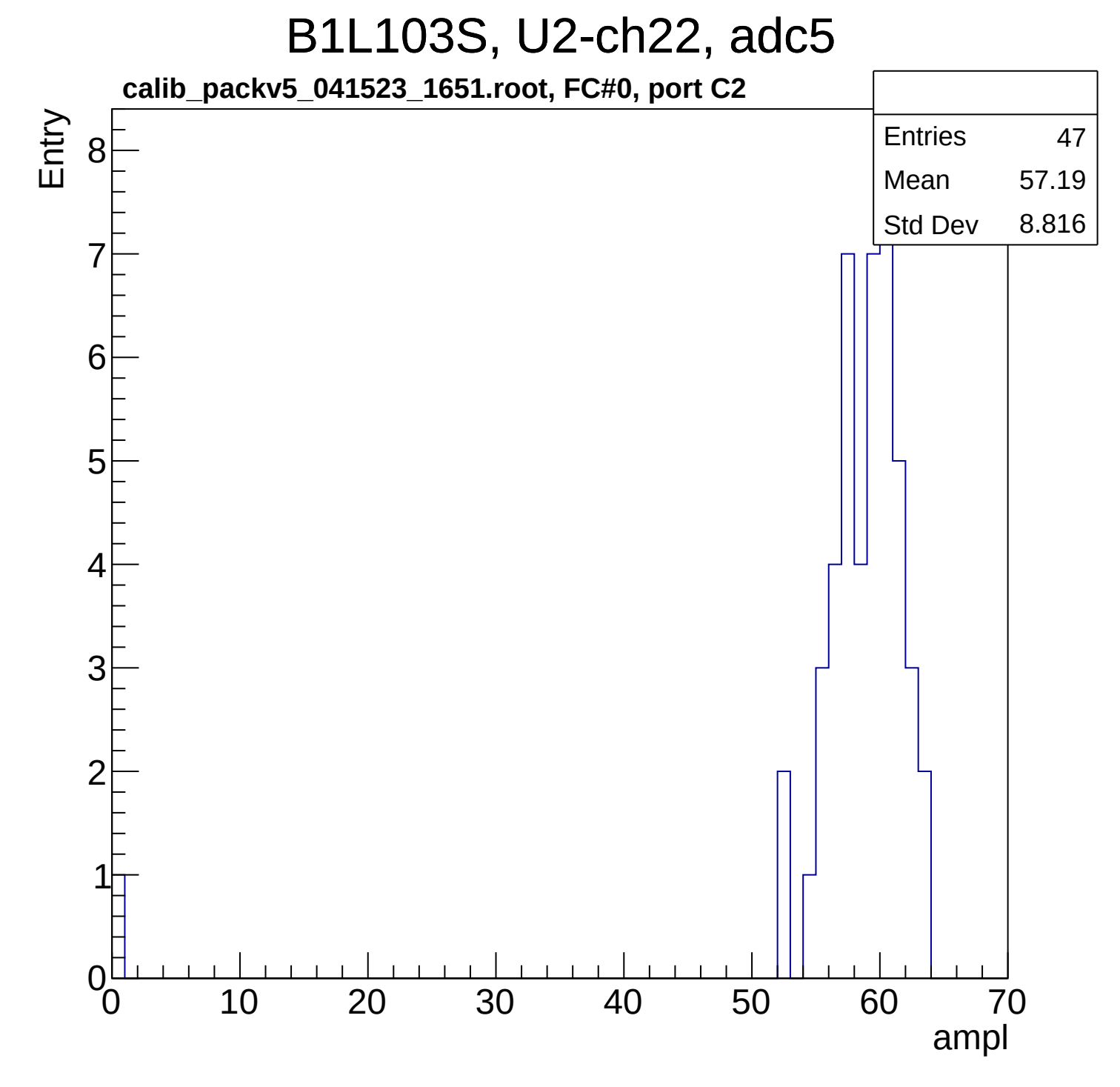

B1L103S, U2-ch22, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 23.16
Std Dev 9.71
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

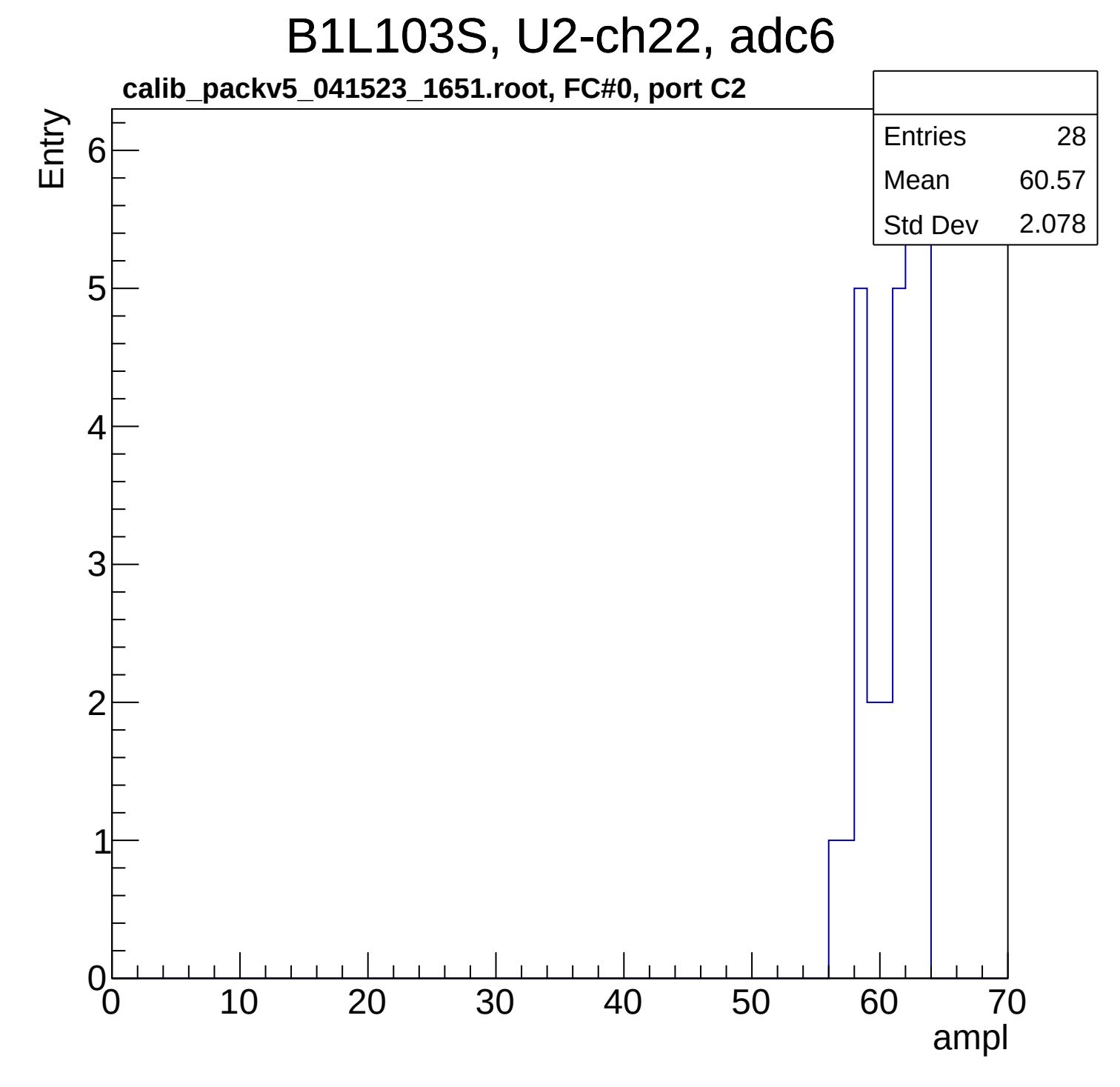

B1L103S, U2-ch22, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 33.79
Std Dev 3.25
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

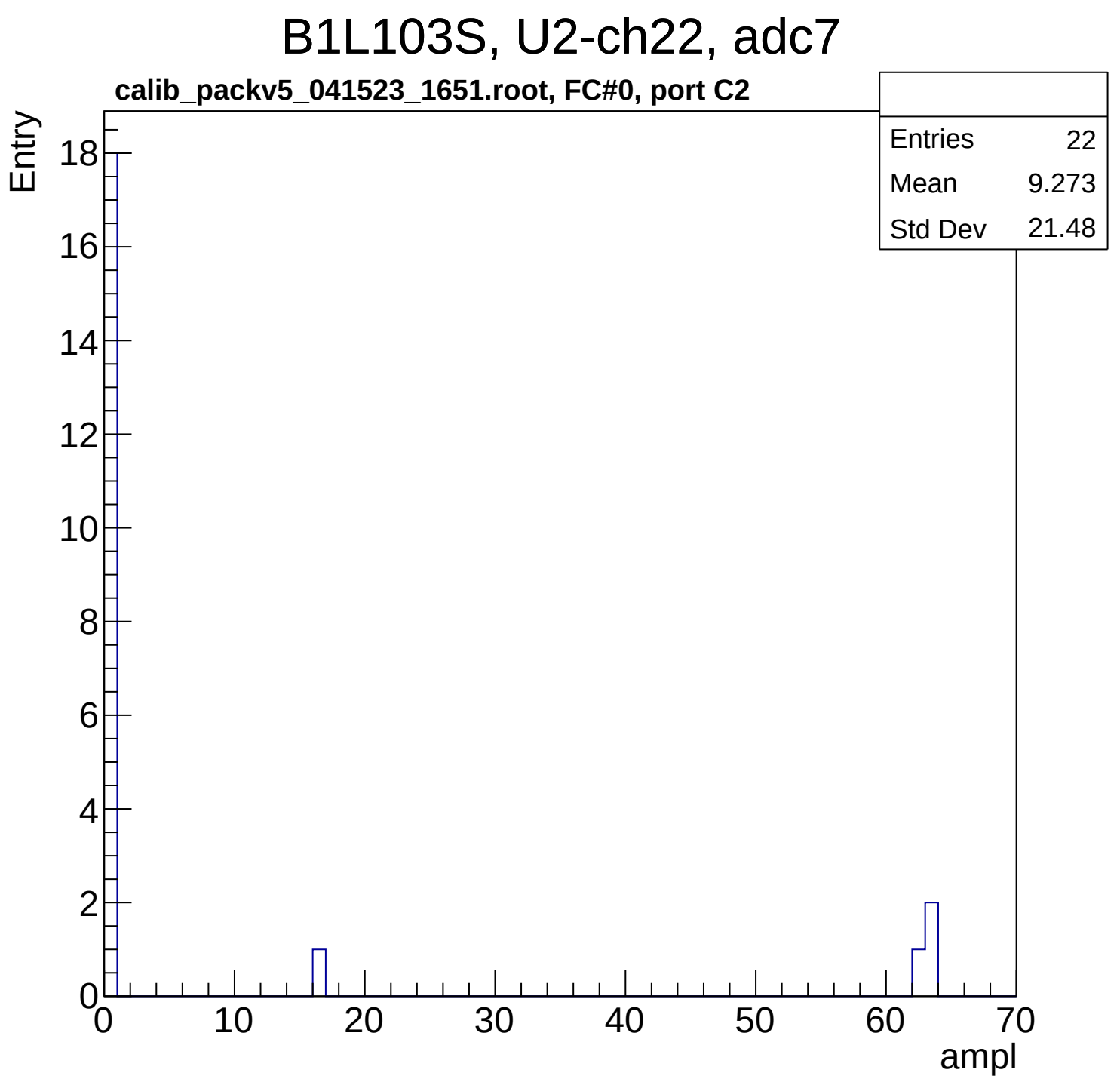

B1L103S, U2-ch22, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 37.04
Std Dev 10.56
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

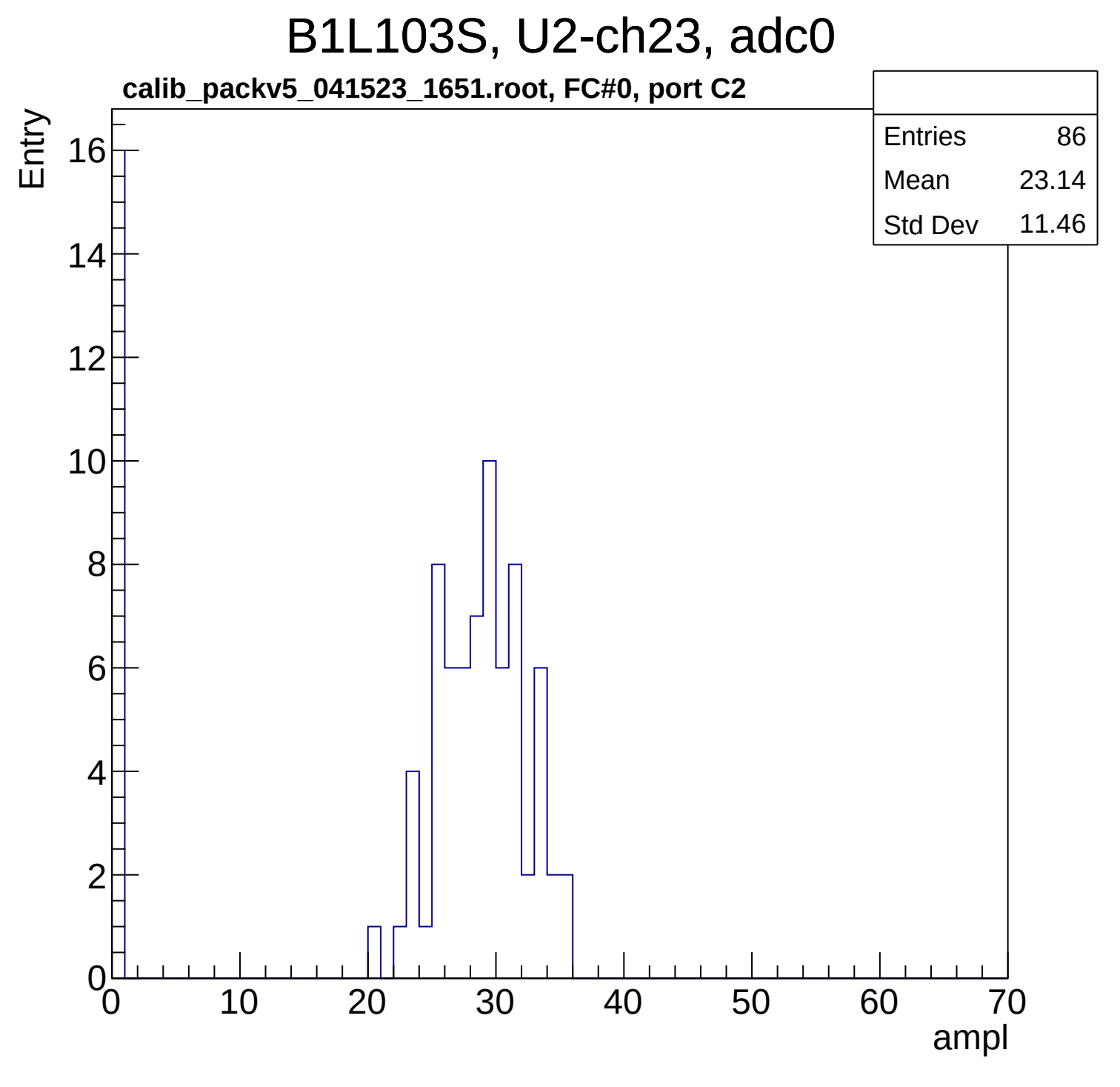

B1L103S, U2-ch22, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 41.96
Std Dev 14.38
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

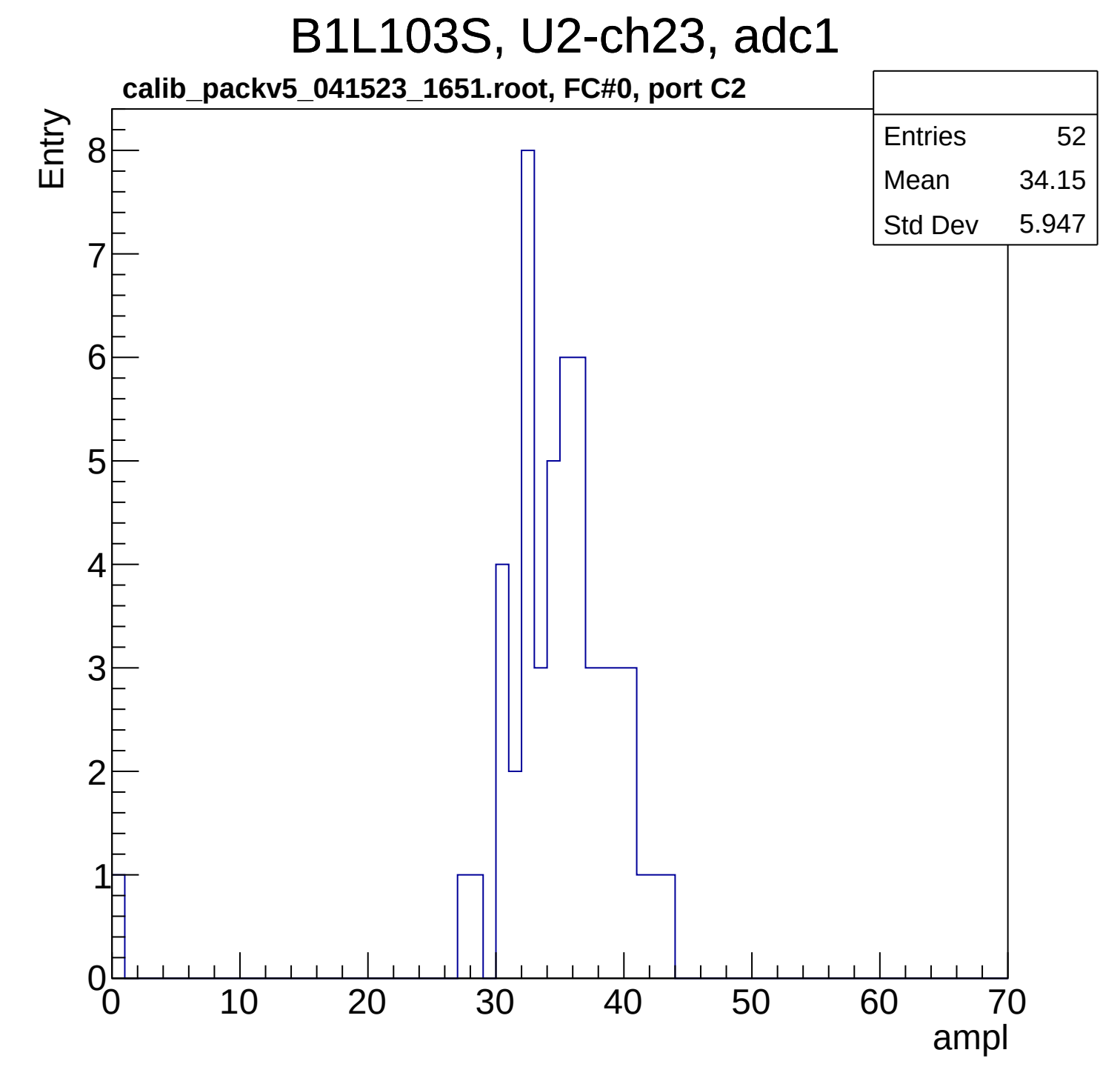

B1L103S, U2-ch22, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 51.44
Std Dev 7.215
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

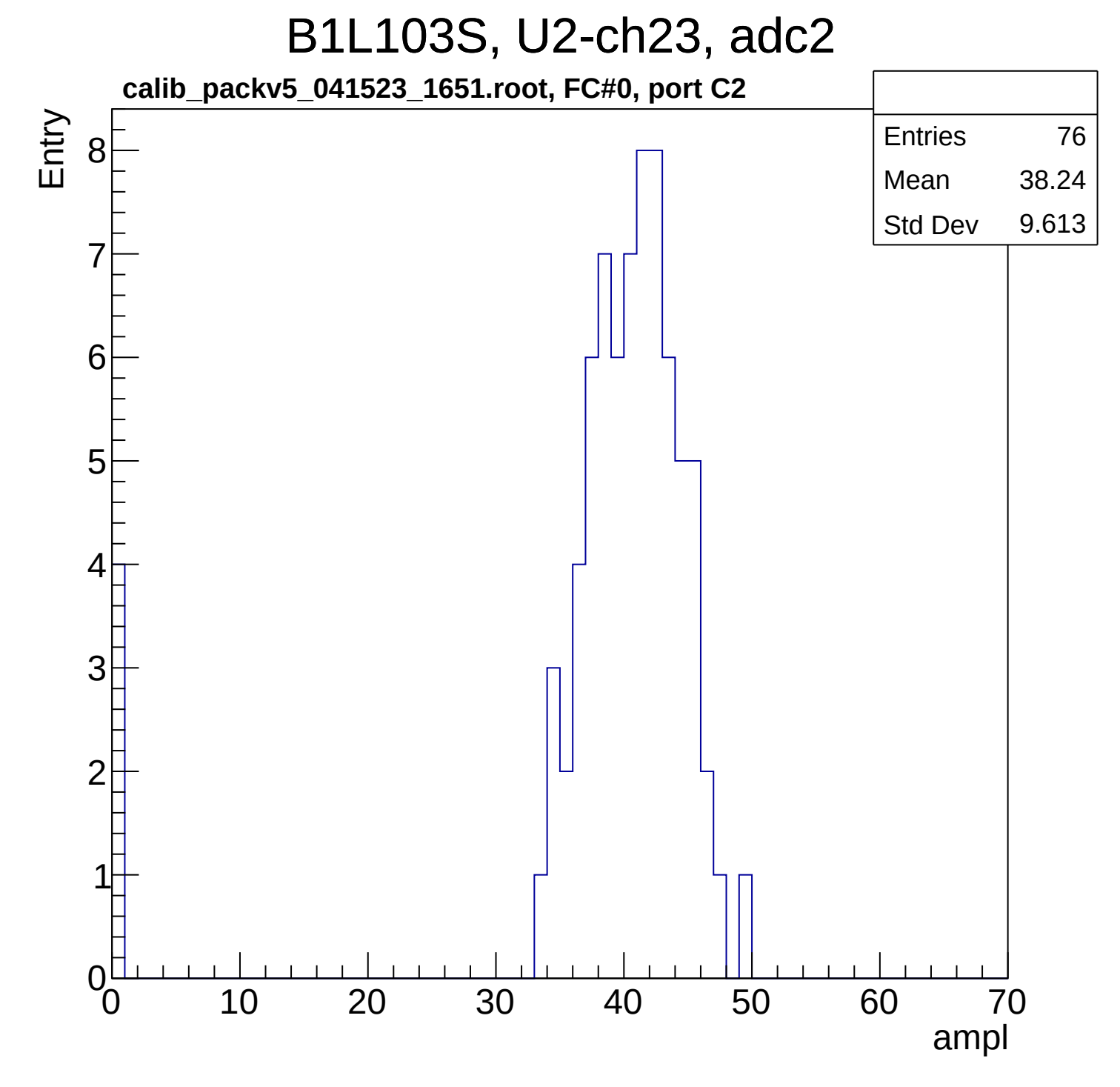

B1L103S, U2-ch22, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 57.19
Std Dev 8.816
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

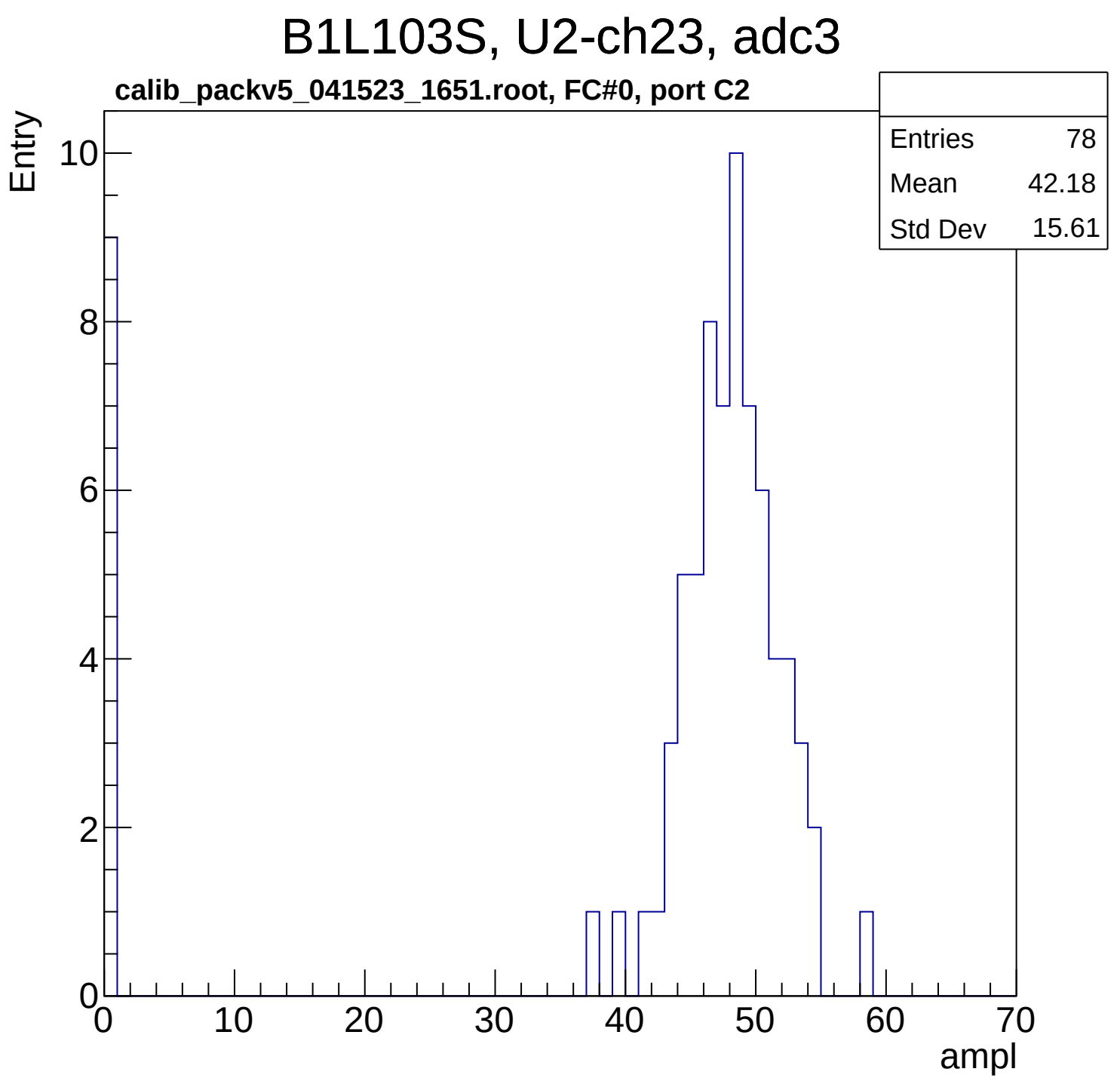

B1L103S, U2-ch22, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 60.57
Std Dev 2.078
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

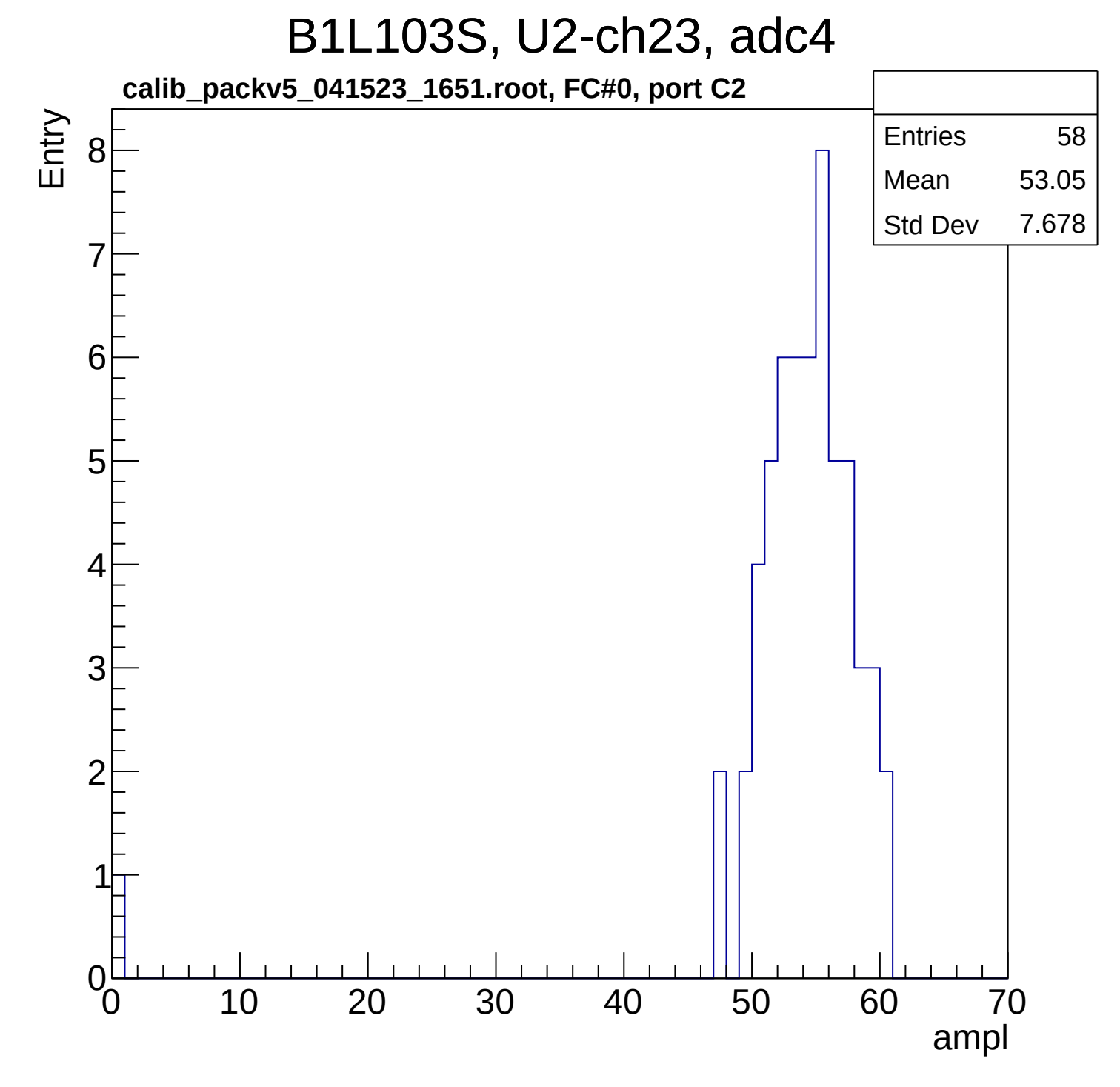

B1L103S, U2-ch22, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 9.273
Std Dev 21.48
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

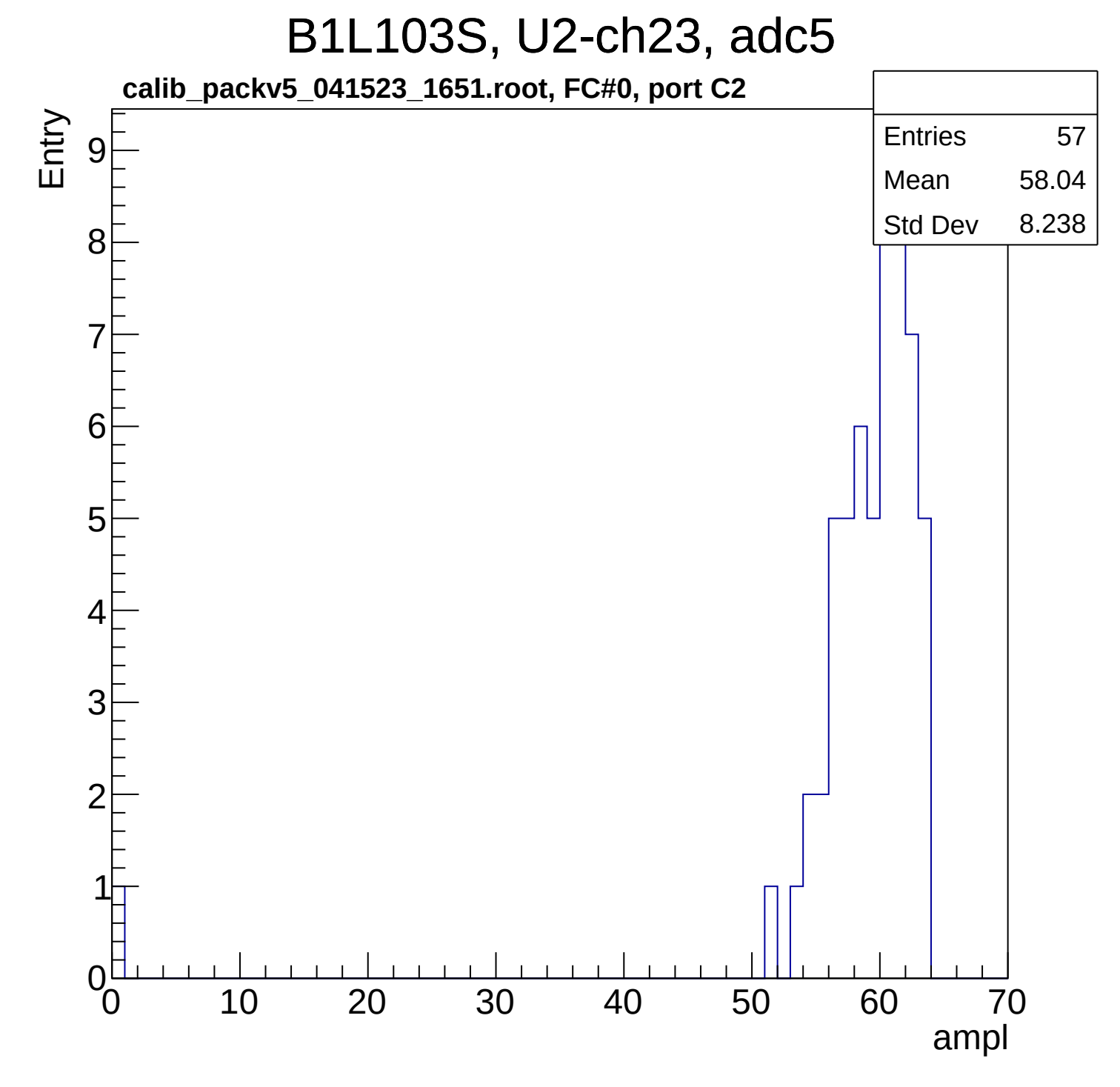

B1L103S, U2-ch23, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 23.14
Std Dev 11.46
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

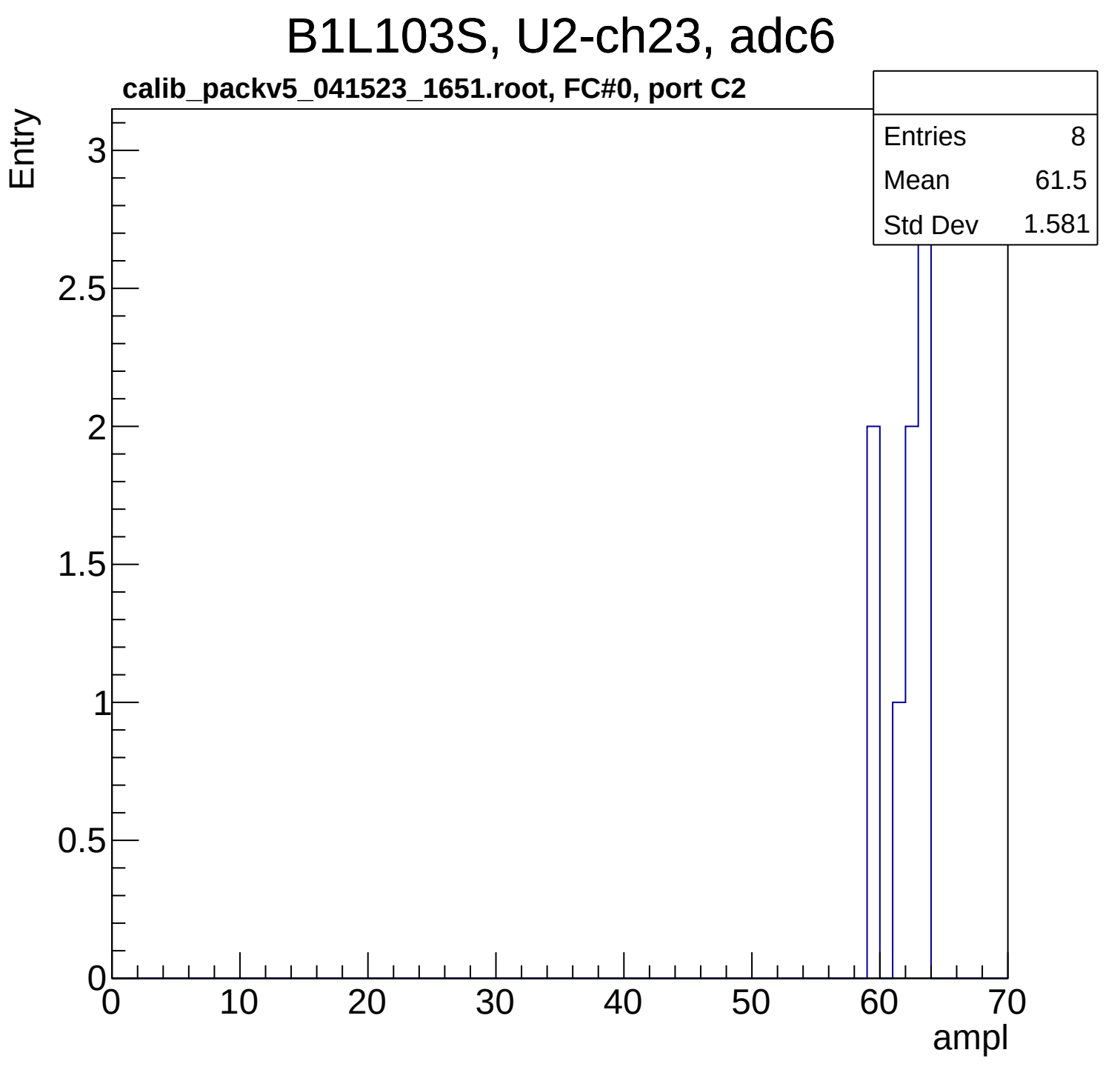

B1L103S, U2-ch23, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 34.15
Std Dev 5.947
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

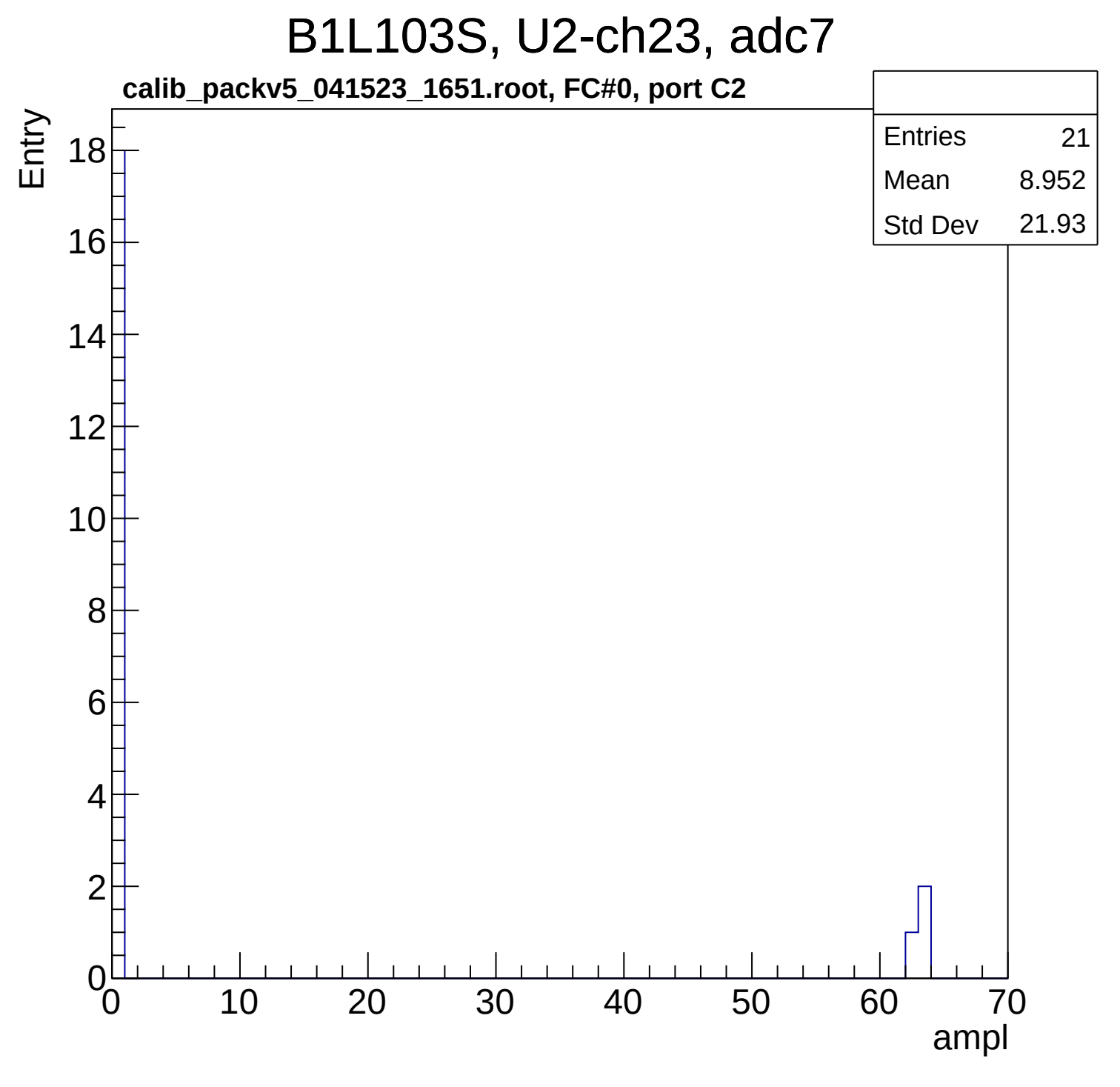

B1L103S, U2-ch23, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 38.24
Std Dev 9.613
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

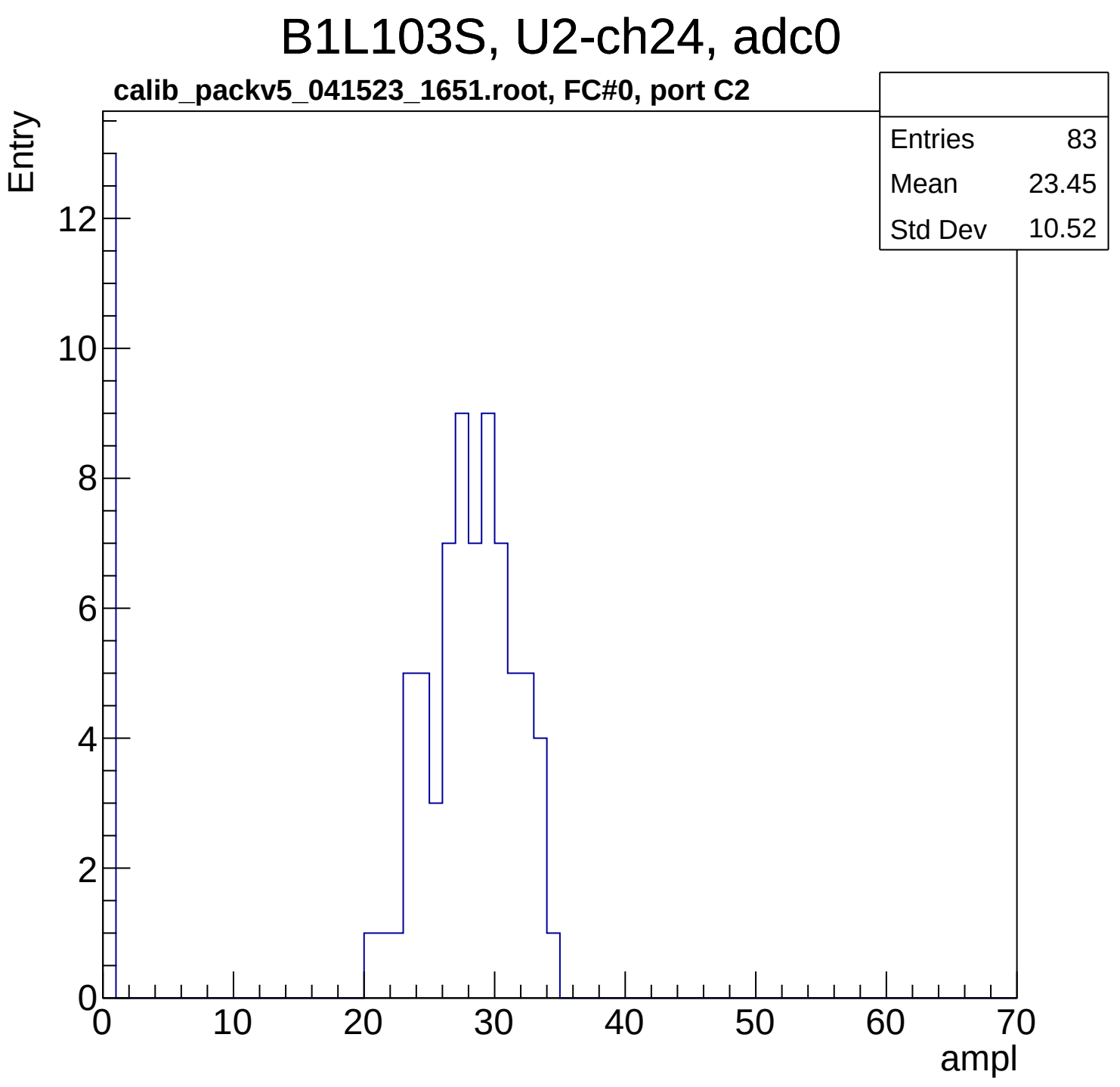

B1L103S, U2-ch23, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 42.18
Std Dev 15.61
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

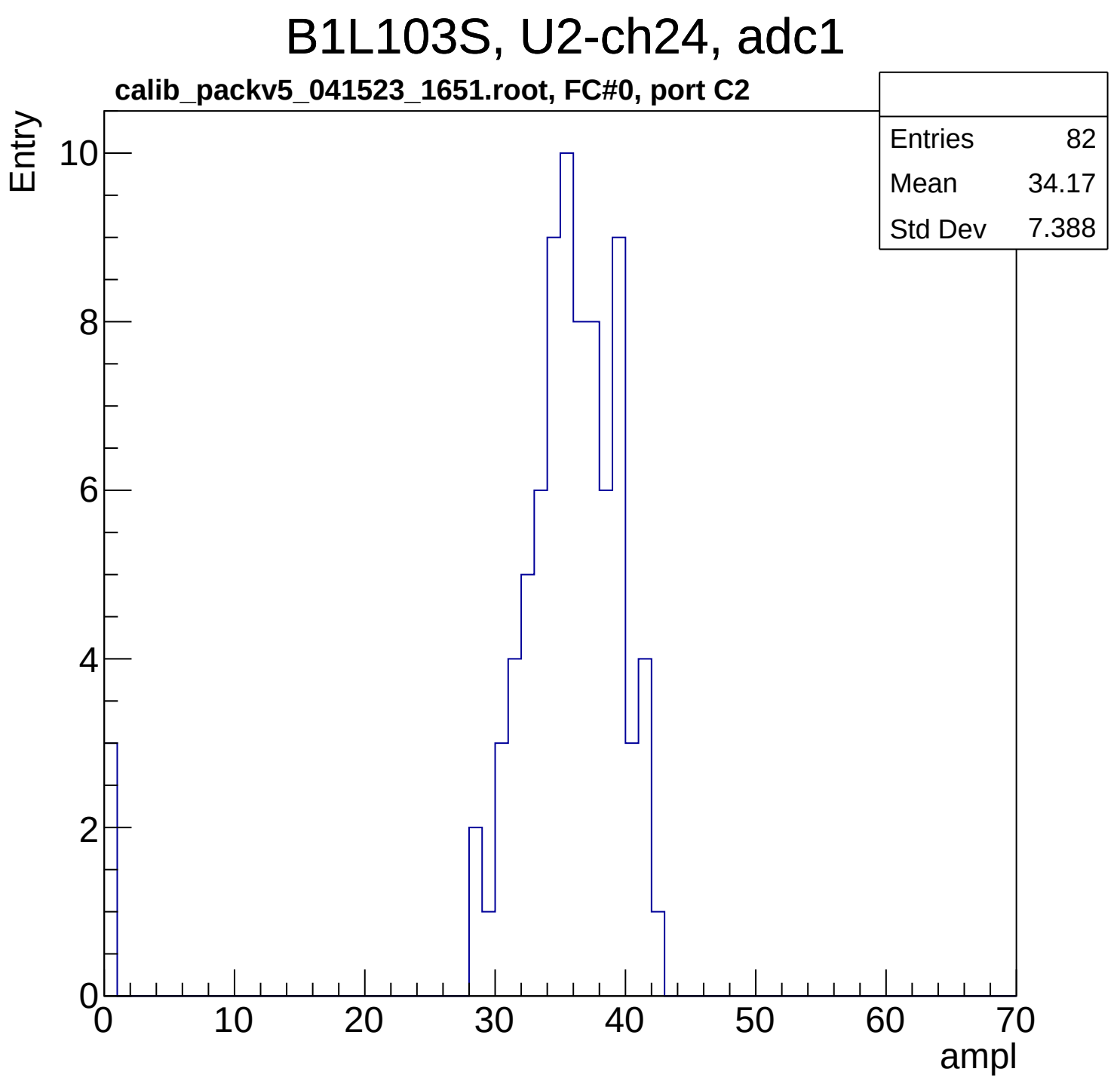

B1L103S, U2-ch23, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 53.05
Std Dev 7.678
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

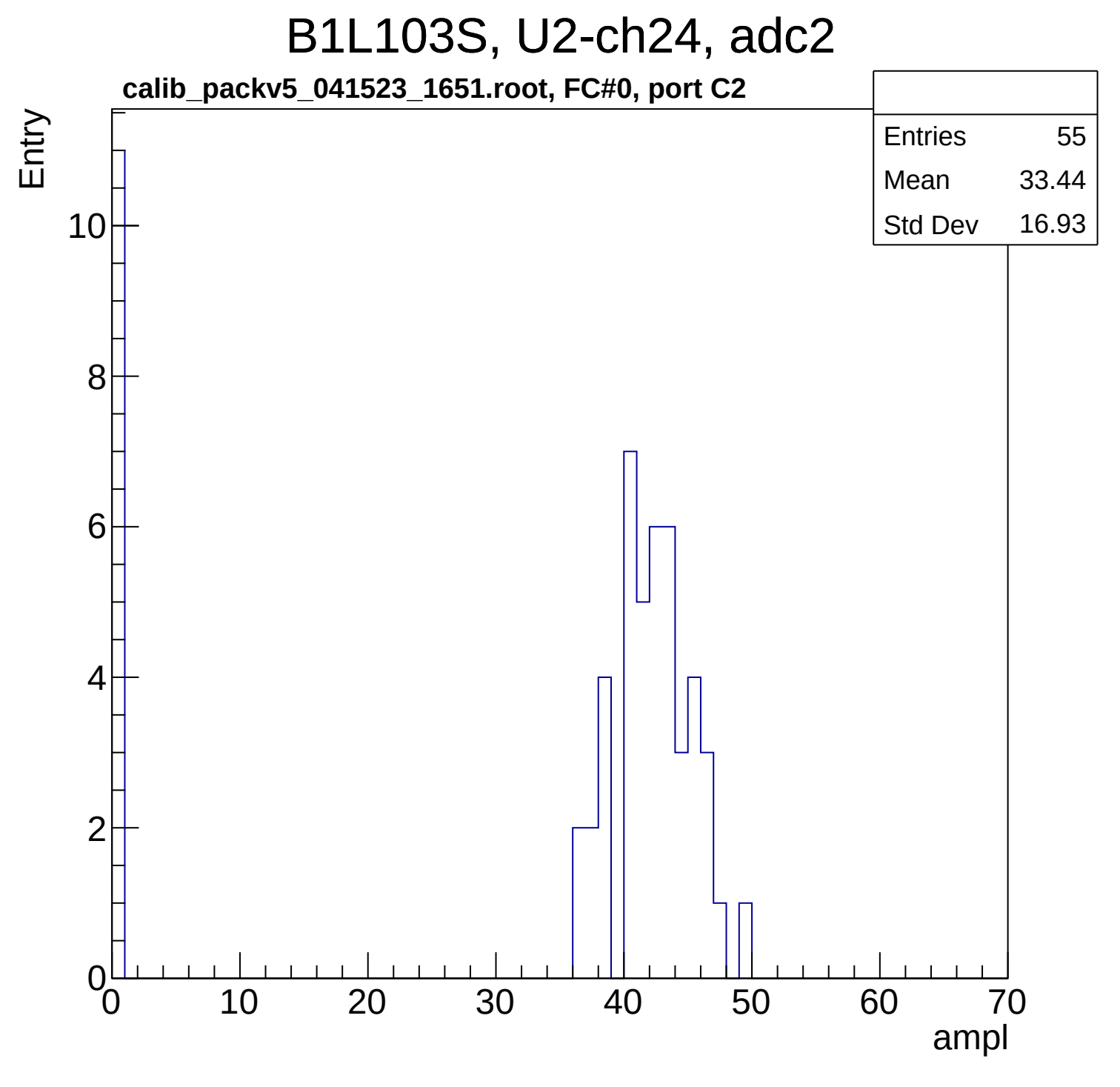

B1L103S, U2-ch23, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.04
Std Dev 8.238
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

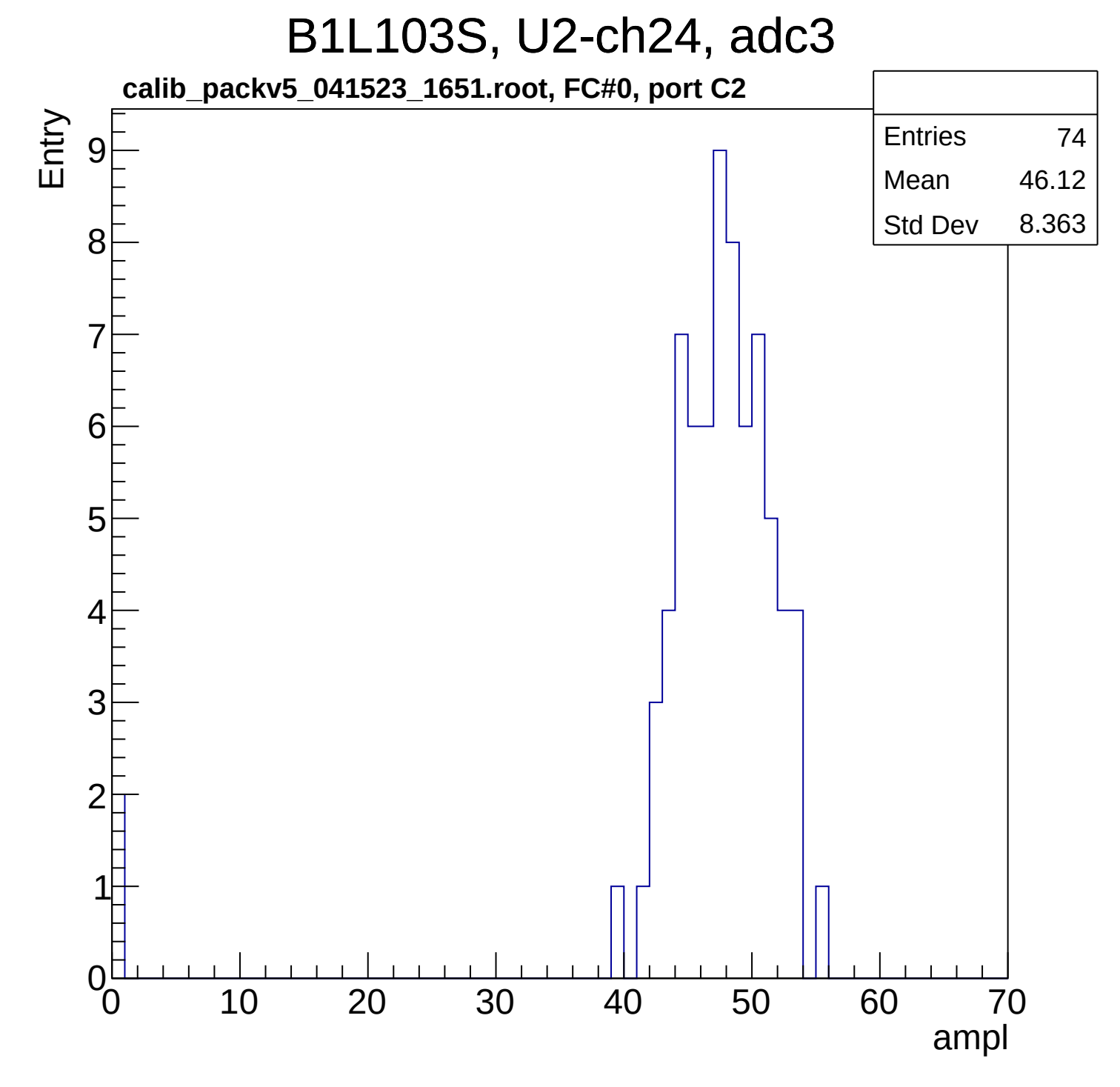

B1L103S, U2-ch23, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.5
Std Dev 1.581
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

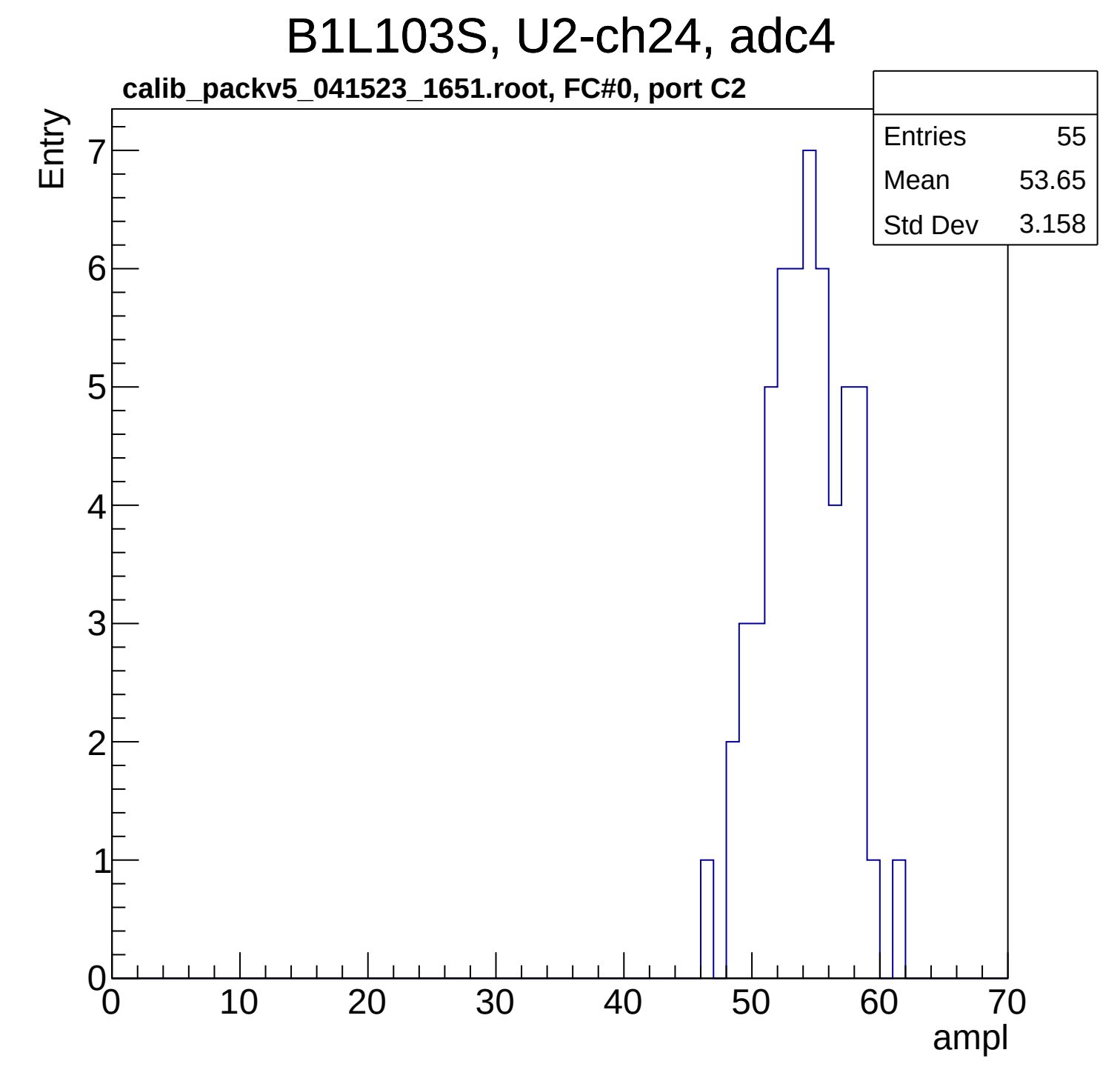

B1L103S, U2-ch23, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 8.952
Std Dev 21.93
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

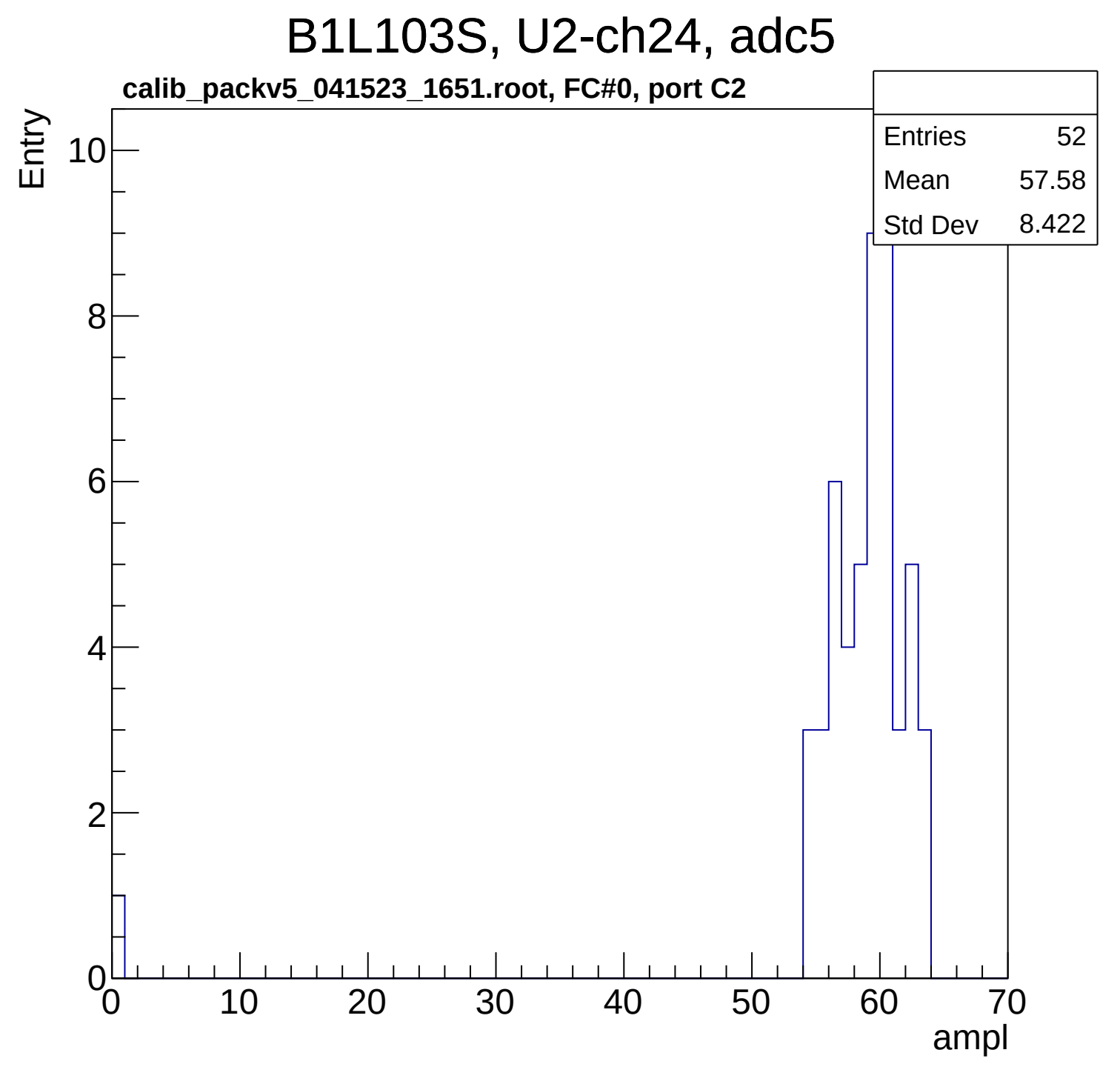

B1L103S, U2-ch24, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 23.45
Std Dev 10.52
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

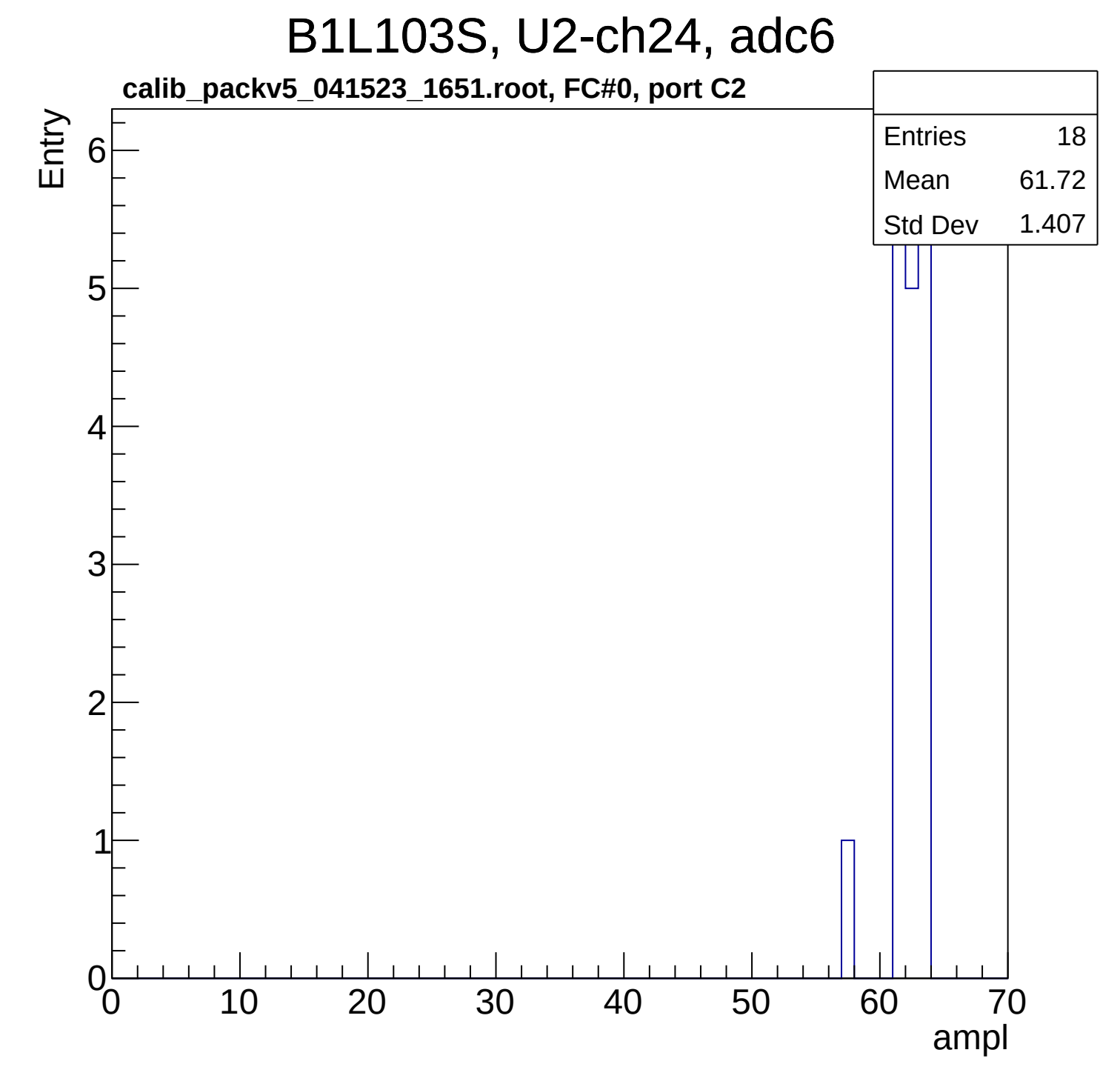

B1L103S, U2-ch24, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 34.17
Std Dev 7.388
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

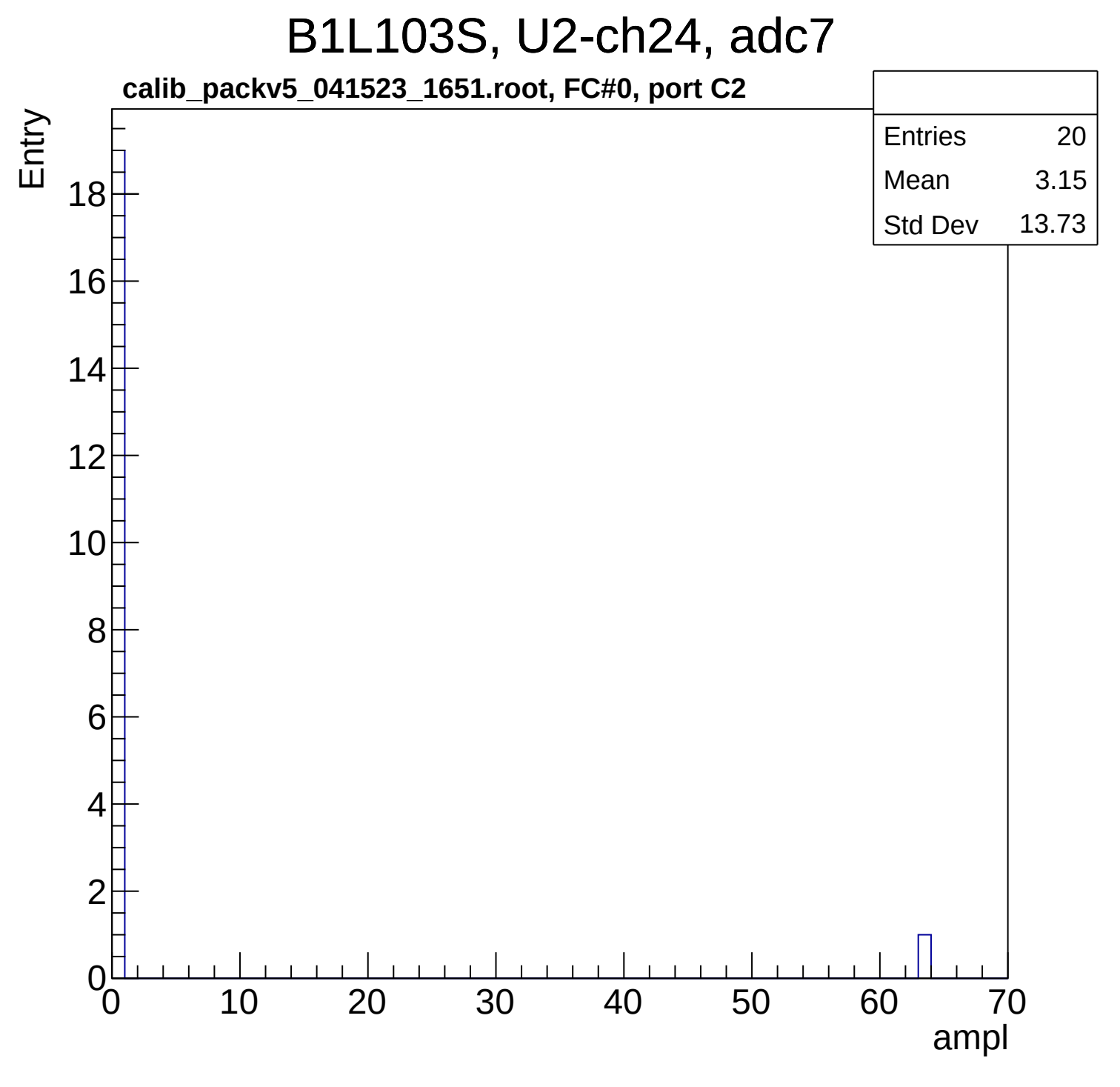

B1L103S, U2-ch24, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 33.44
Std Dev 16.93
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

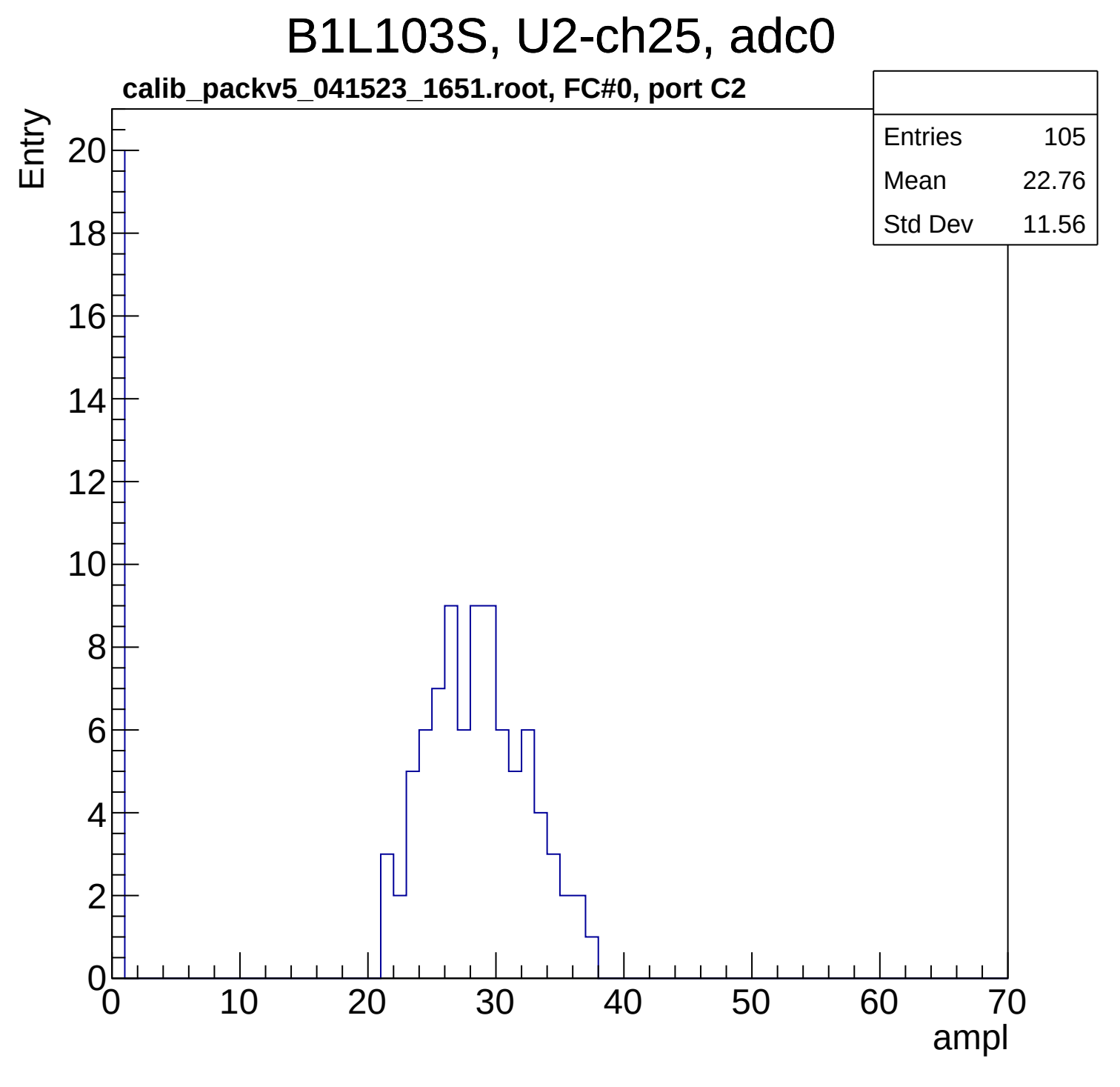

B1L103S, U2-ch24, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 46.12
Std Dev 8.363
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

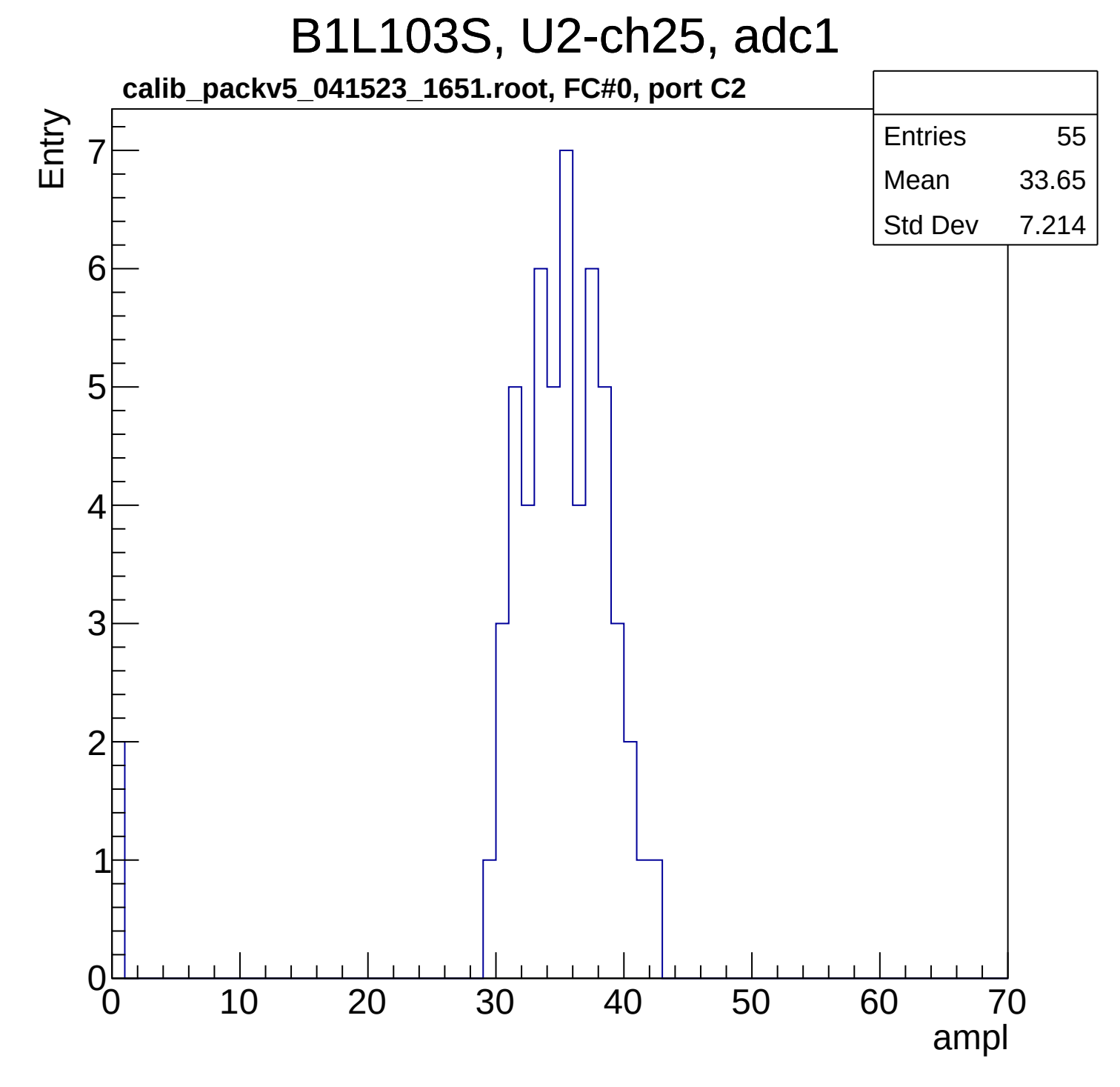

B1L103S, U2-ch24, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 53.65
Std Dev 3.158
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

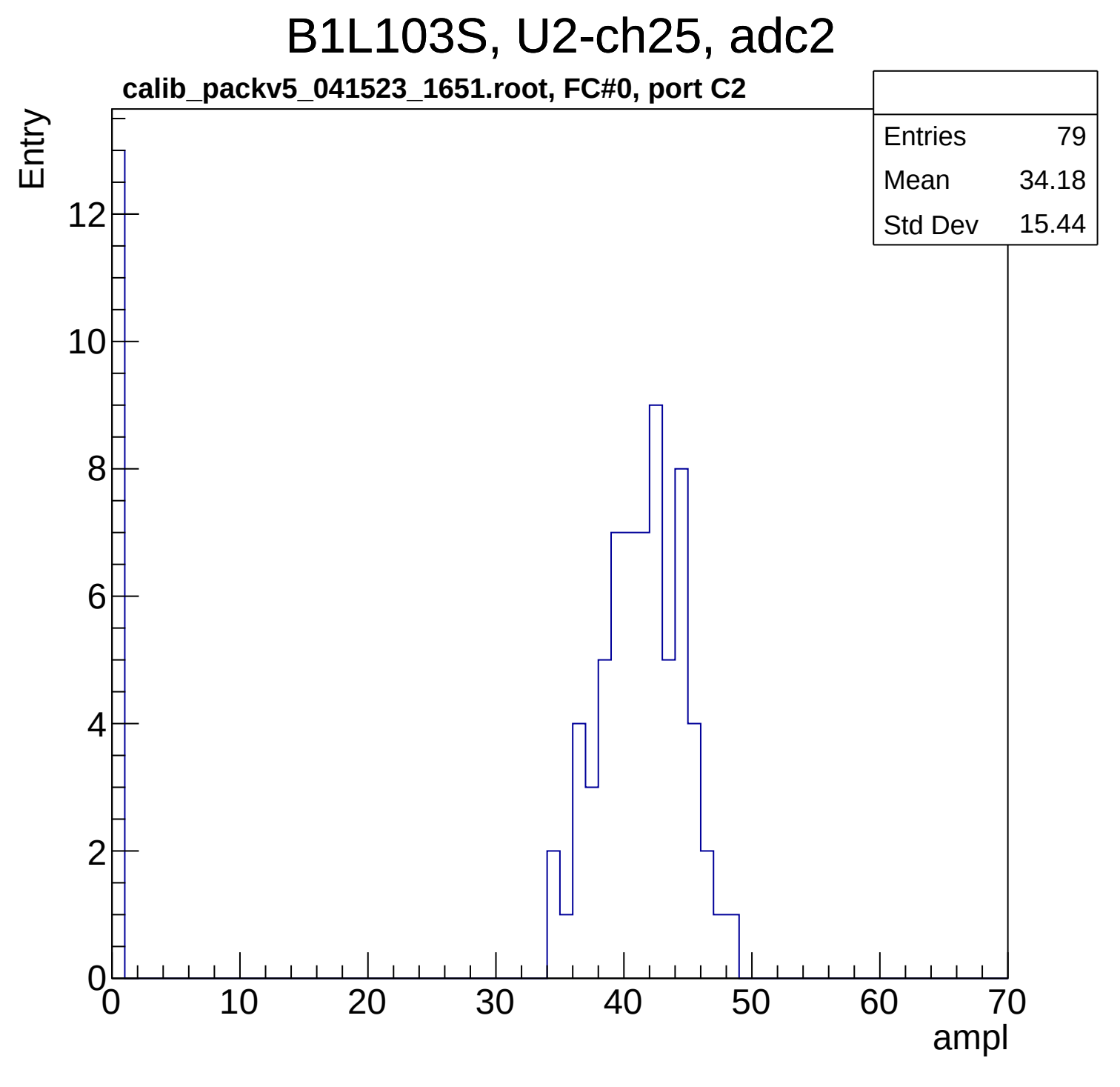

B1L103S, U2-ch24, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 57.58
Std Dev 8.422
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

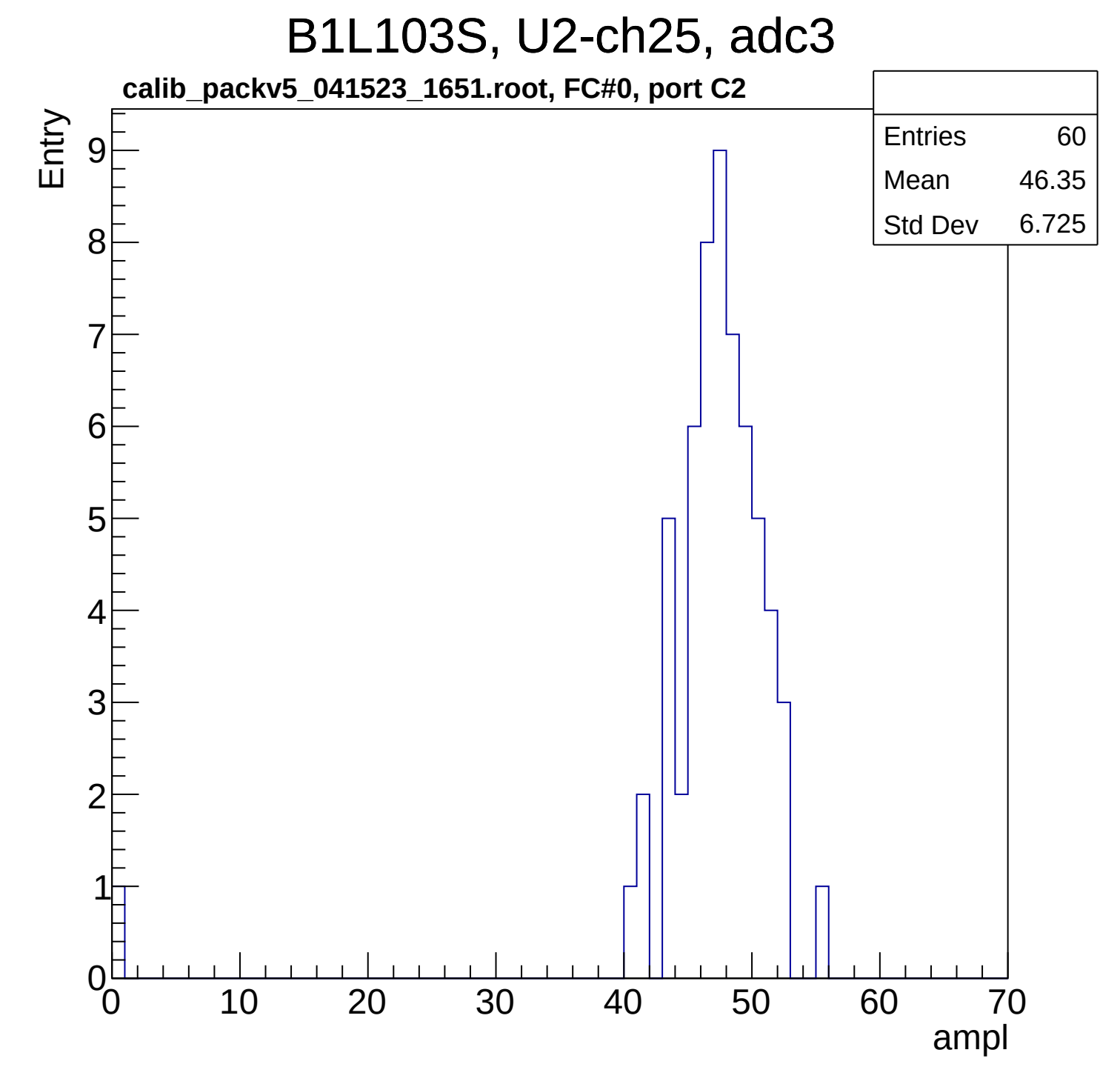

B1L103S, U2-ch24, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 61.72
Std Dev 1.407
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

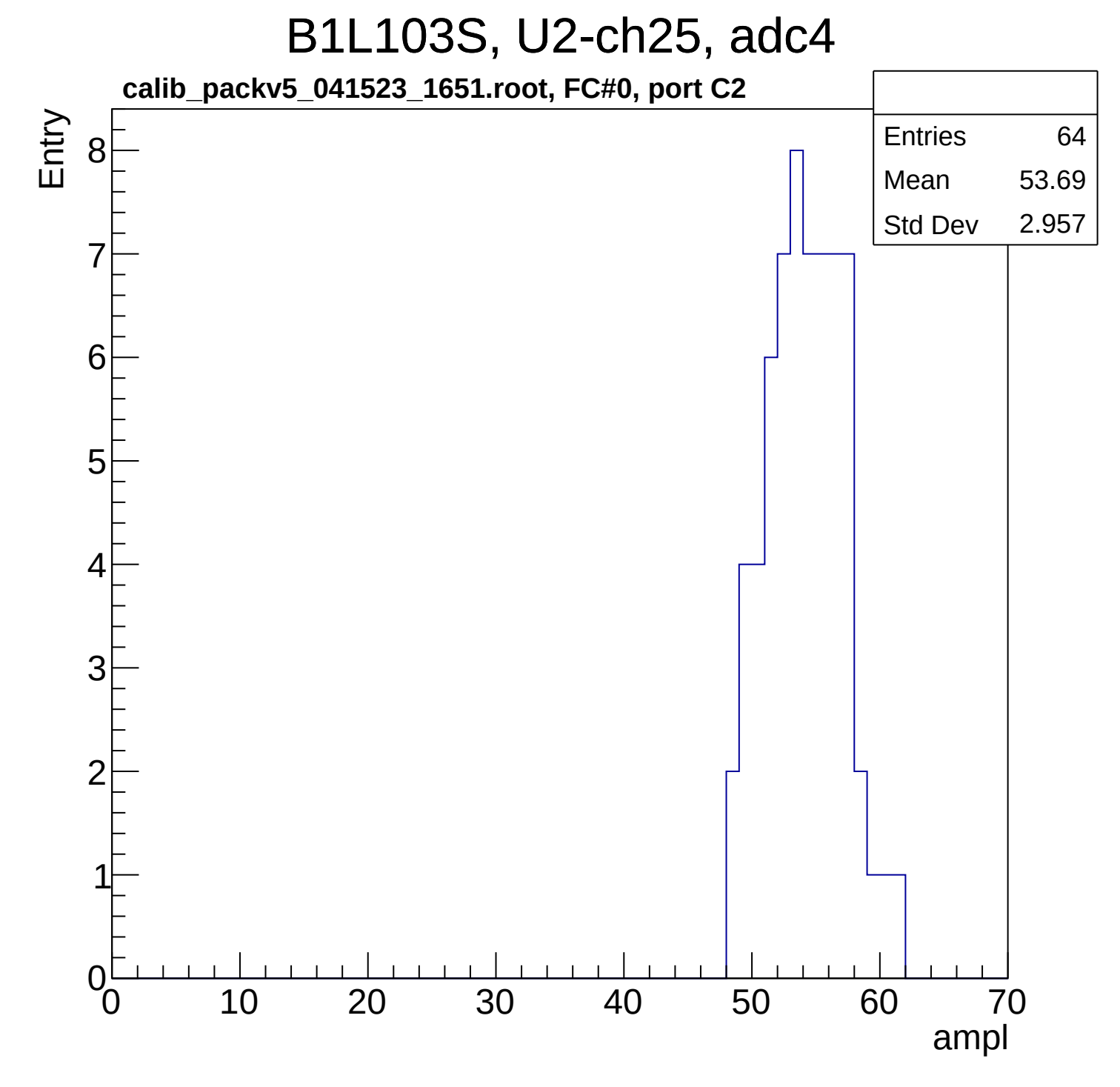

B1L103S, U2-ch24, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

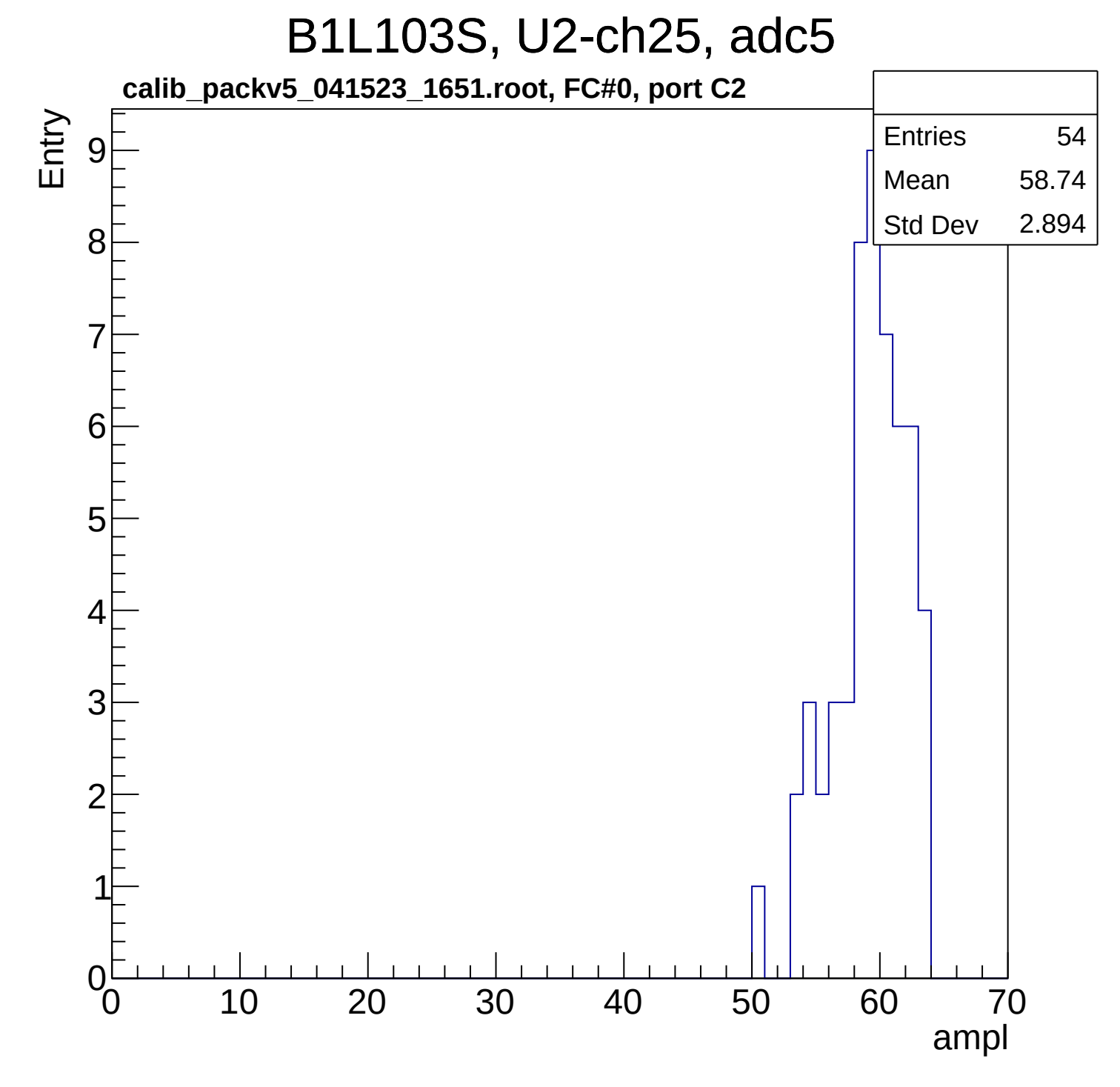

B1L103S, U2-ch25, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 105
Mean 22.76
Std Dev 11.56
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl

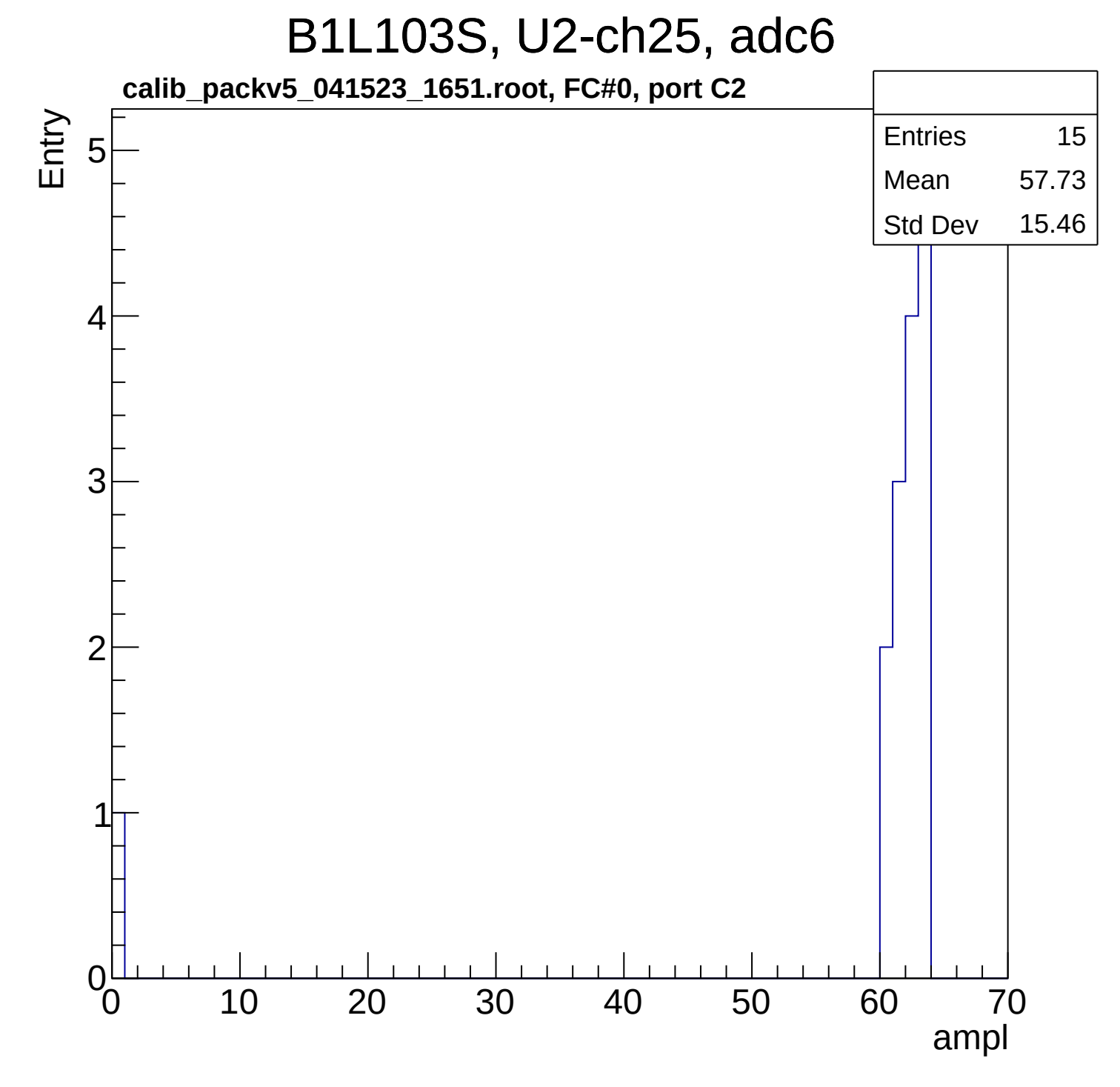

B1L103S, U2-ch25, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 33.65
Std Dev 7.214
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

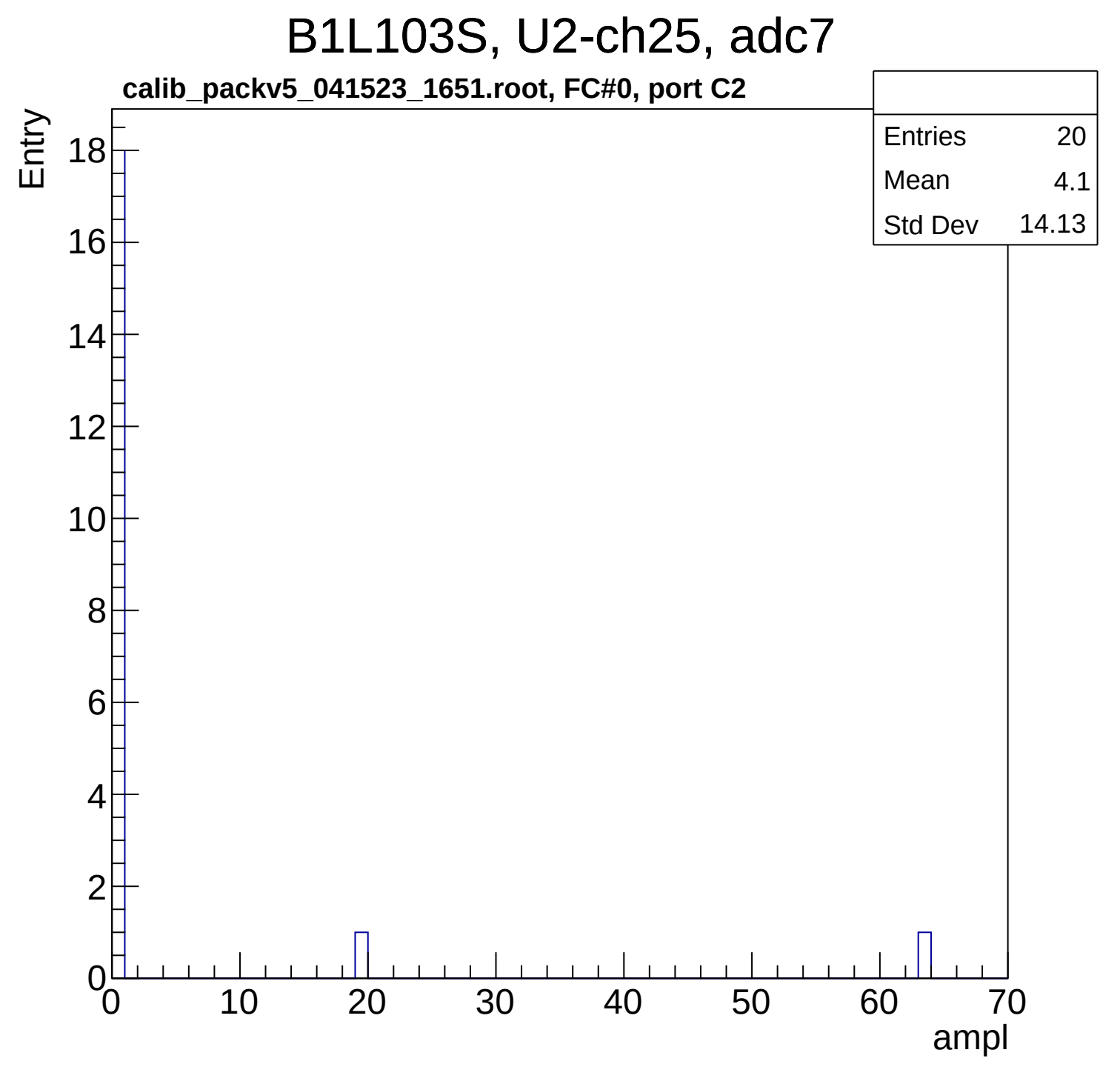

B1L103S, U2-ch25, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 34.18
Std Dev 15.44
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

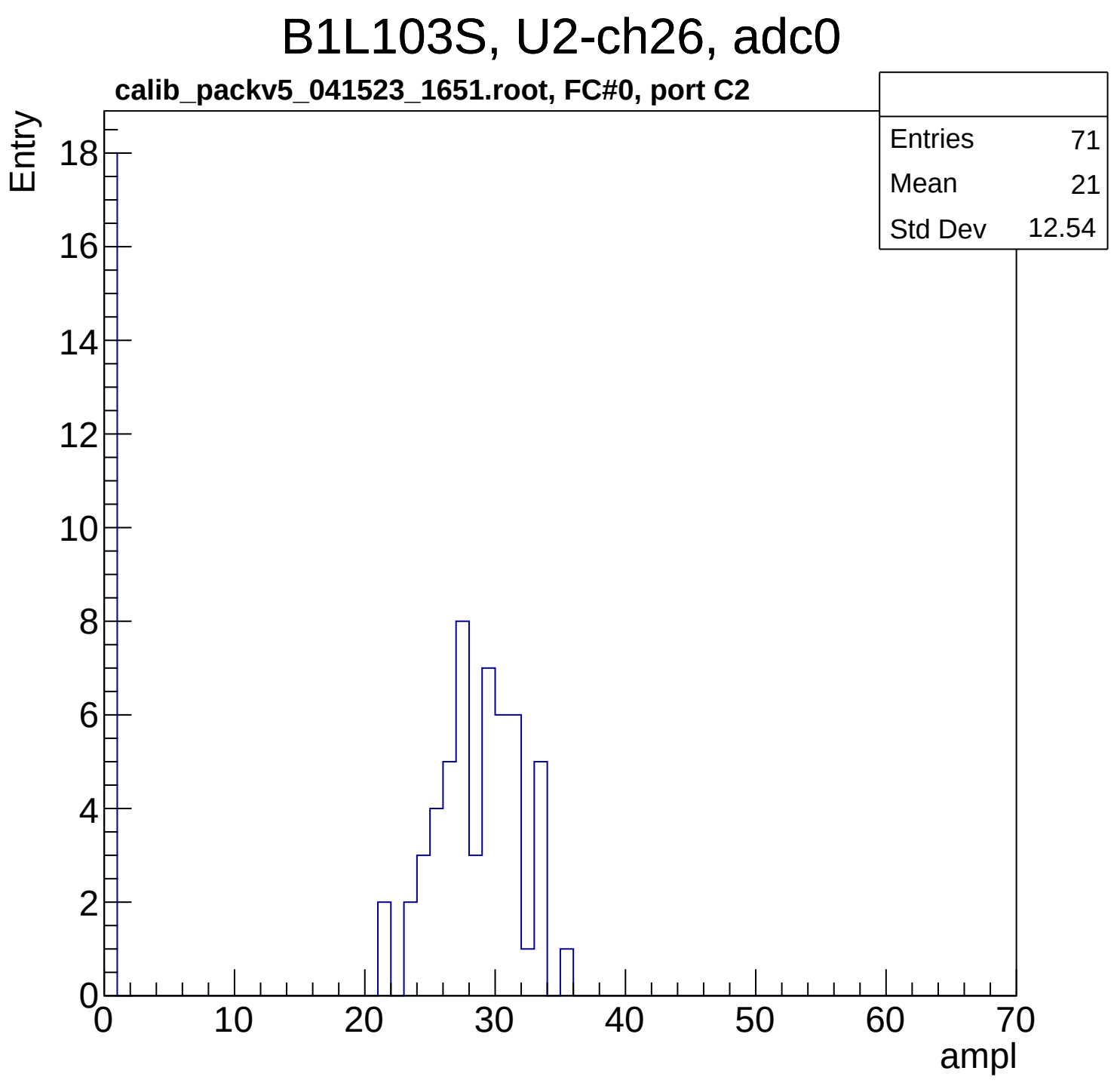

B1L103S, U2-ch25, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 46.35
Std Dev 6.725
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

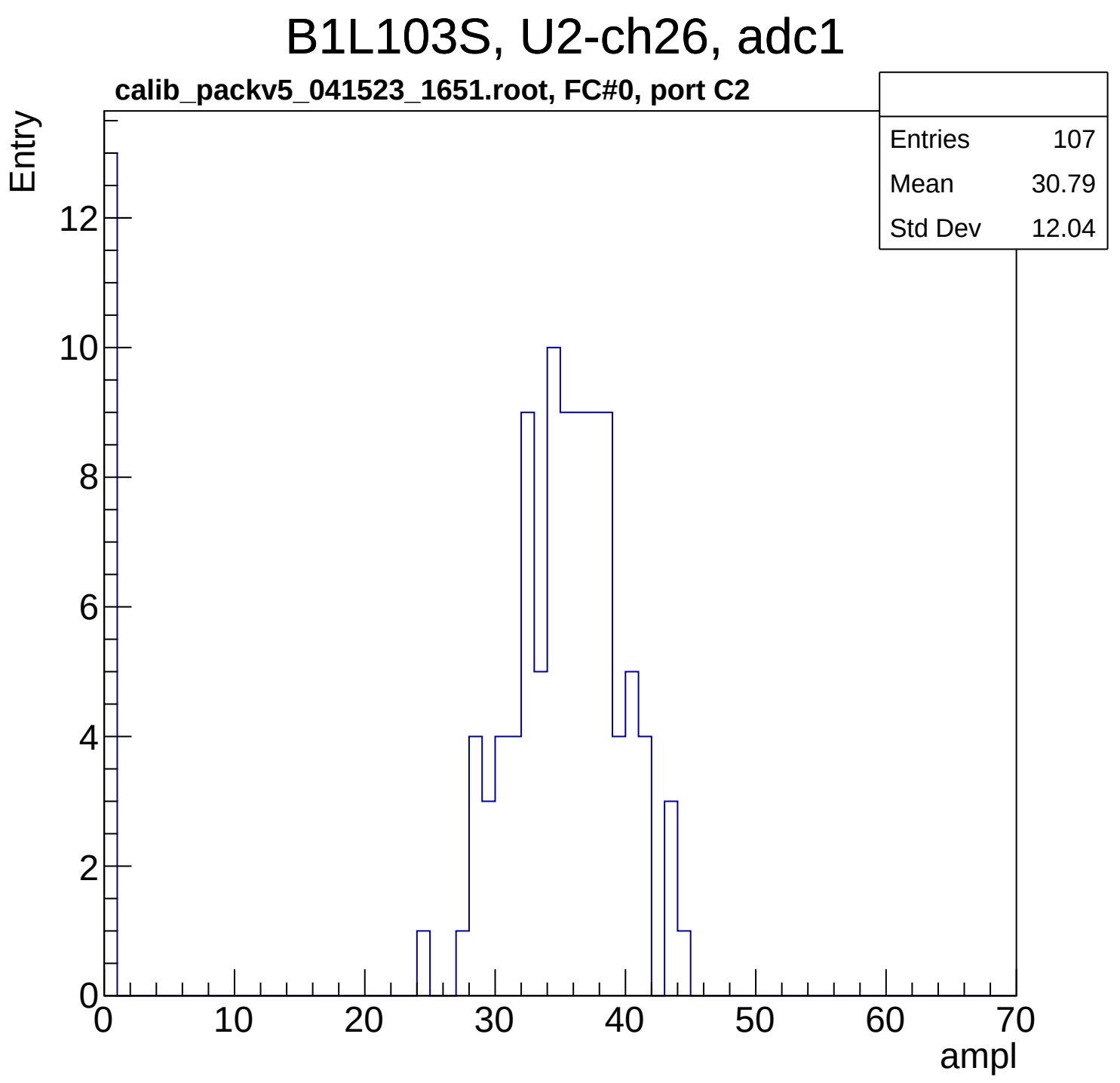

B1L103S, U2-ch25, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 53.69
Std Dev 2.957
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

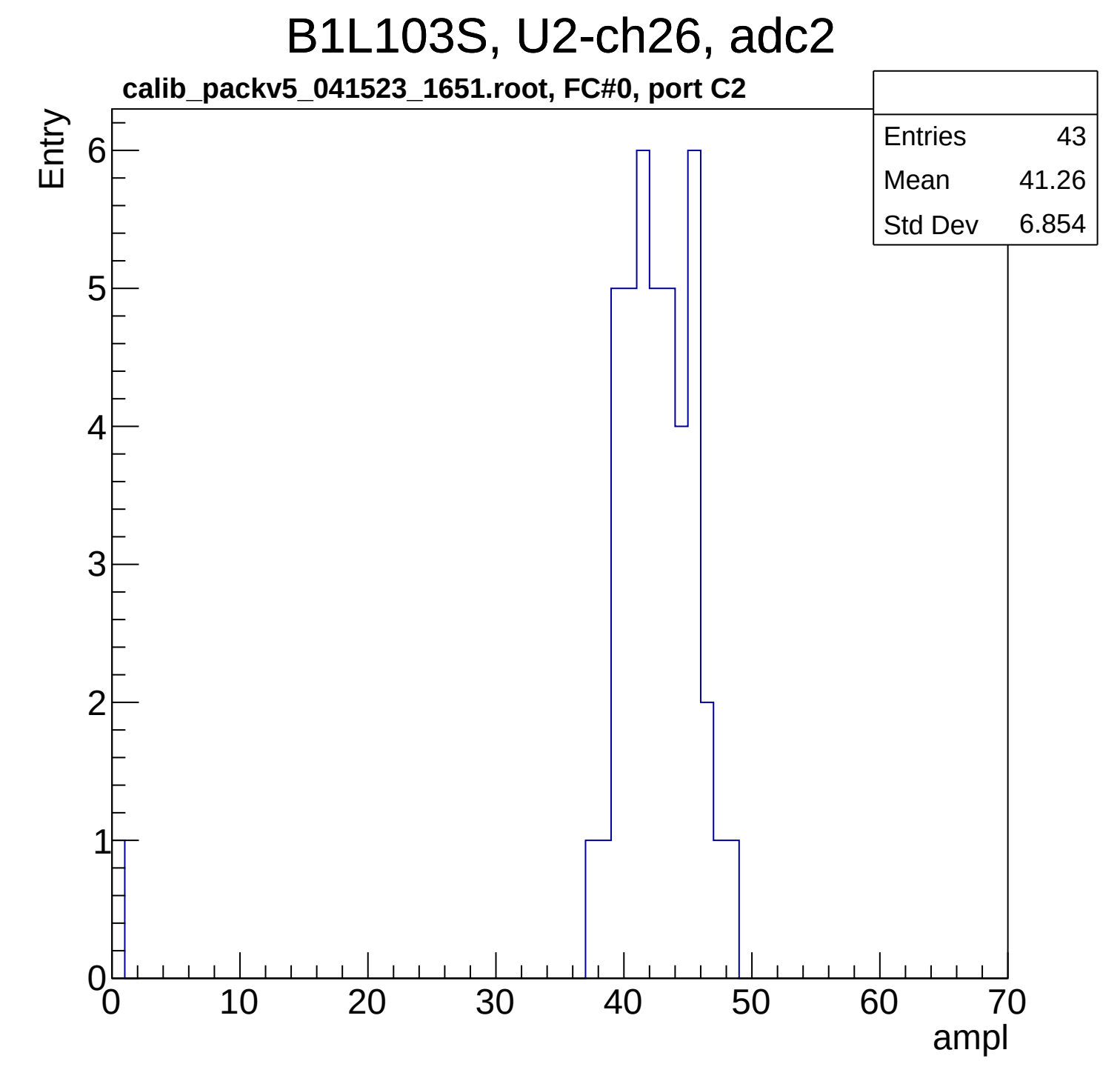

B1L103S, U2-ch25, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.74
Std Dev 2.894
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

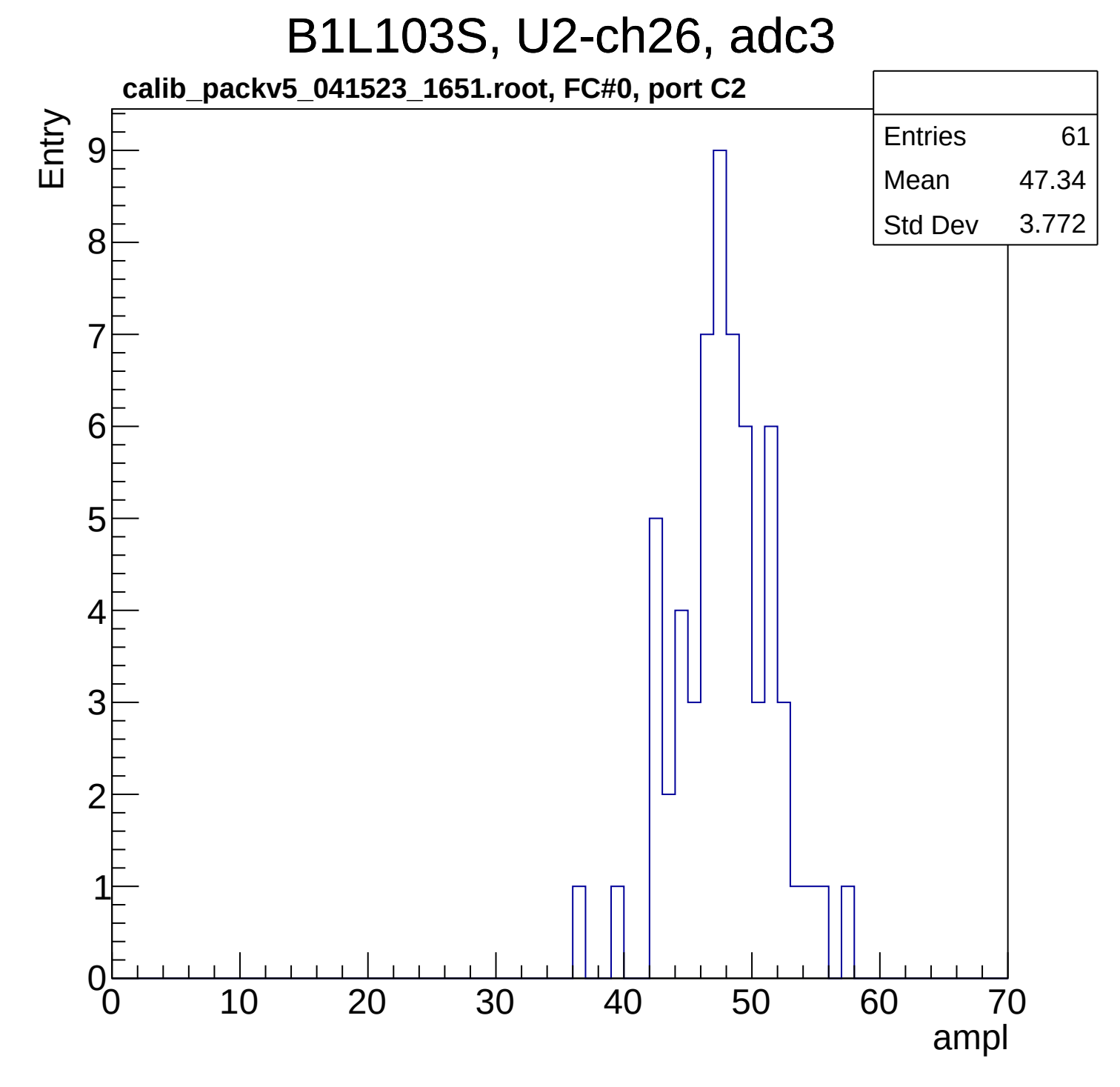

B1L103S, U2-ch25, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.73
Std Dev 15.46
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

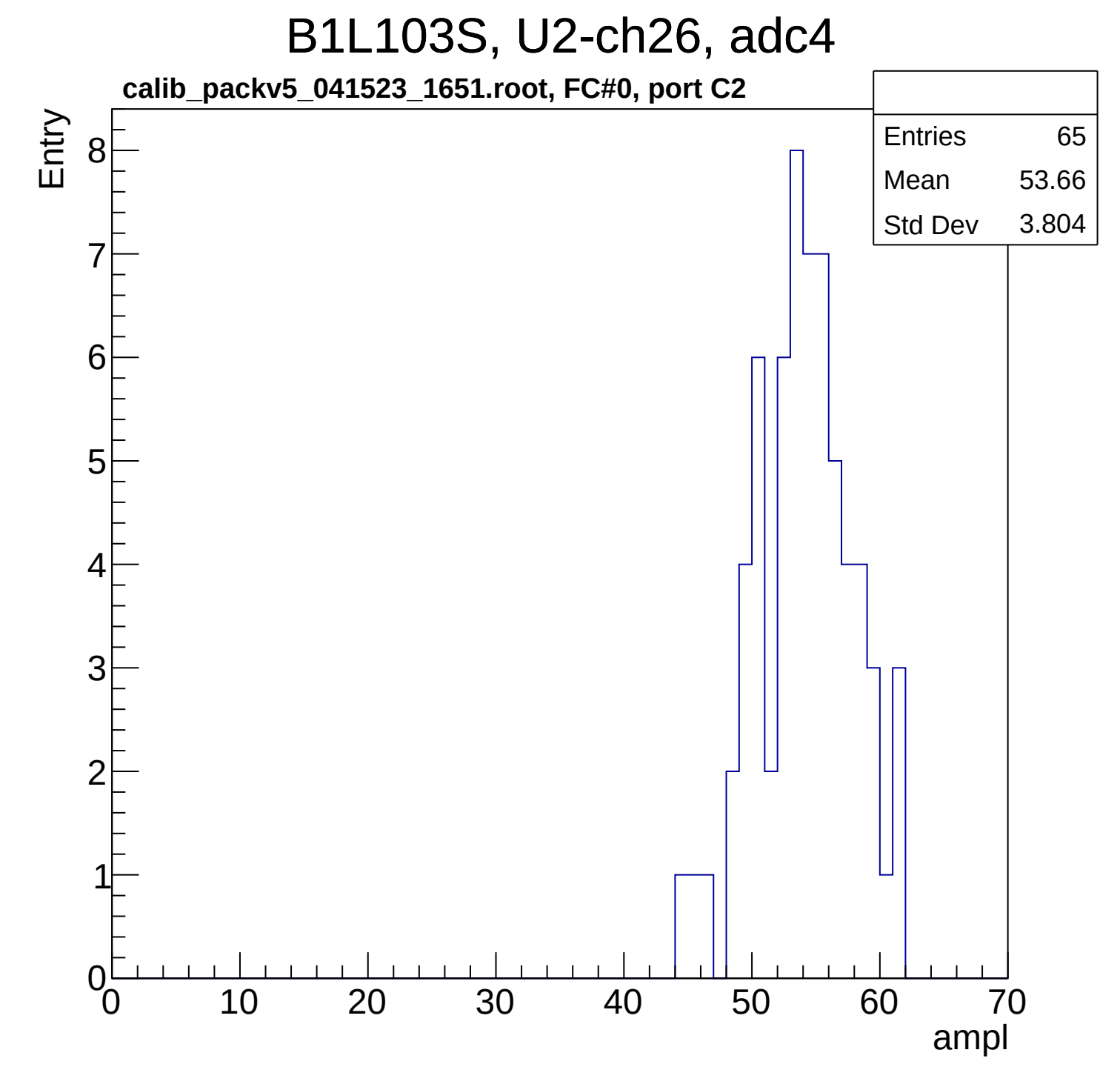

B1L103S, U2-ch25, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.1
Std Dev 14.13
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

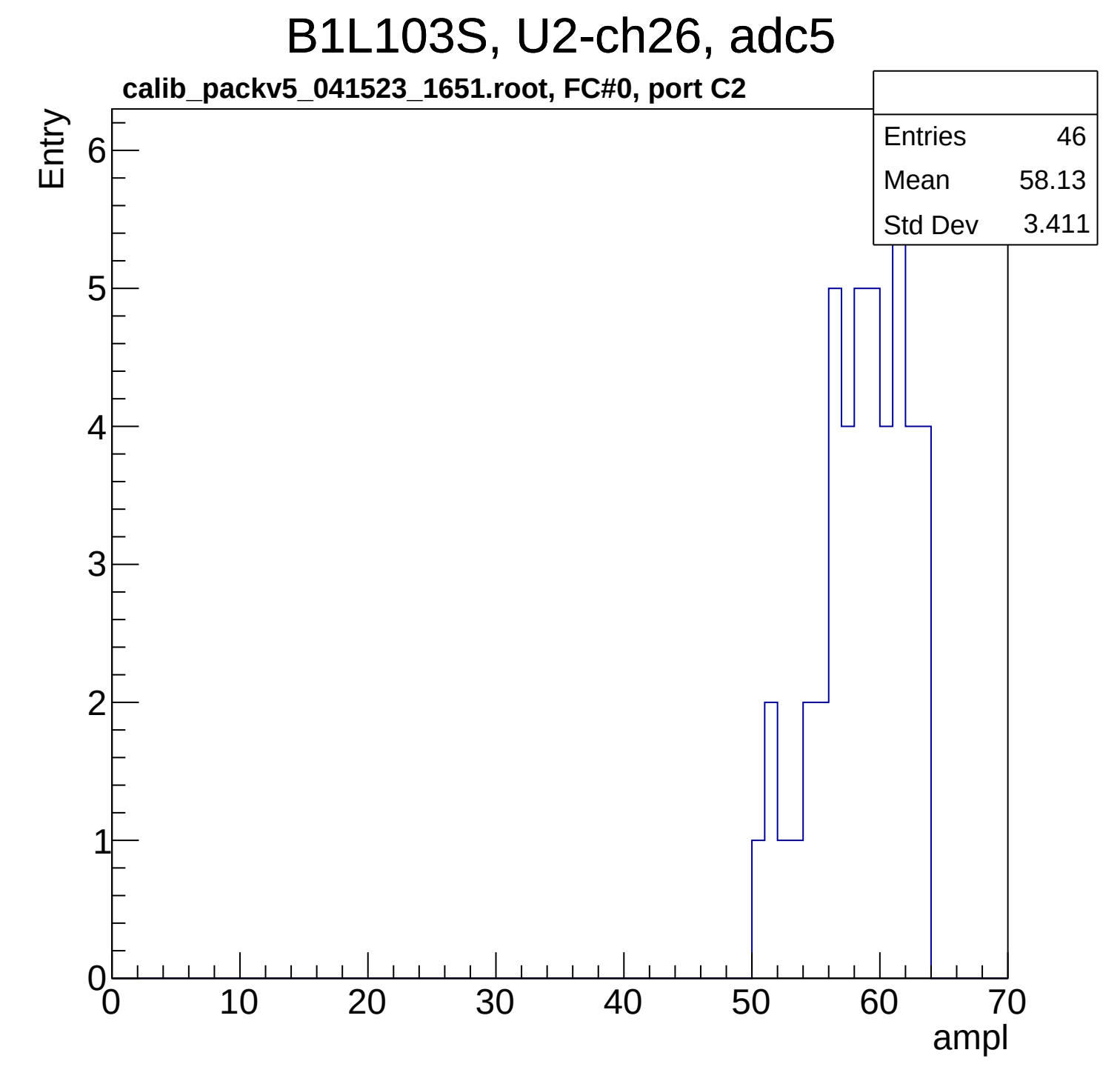

B1L103S, U2-ch26, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 21
Std Dev 12.54
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

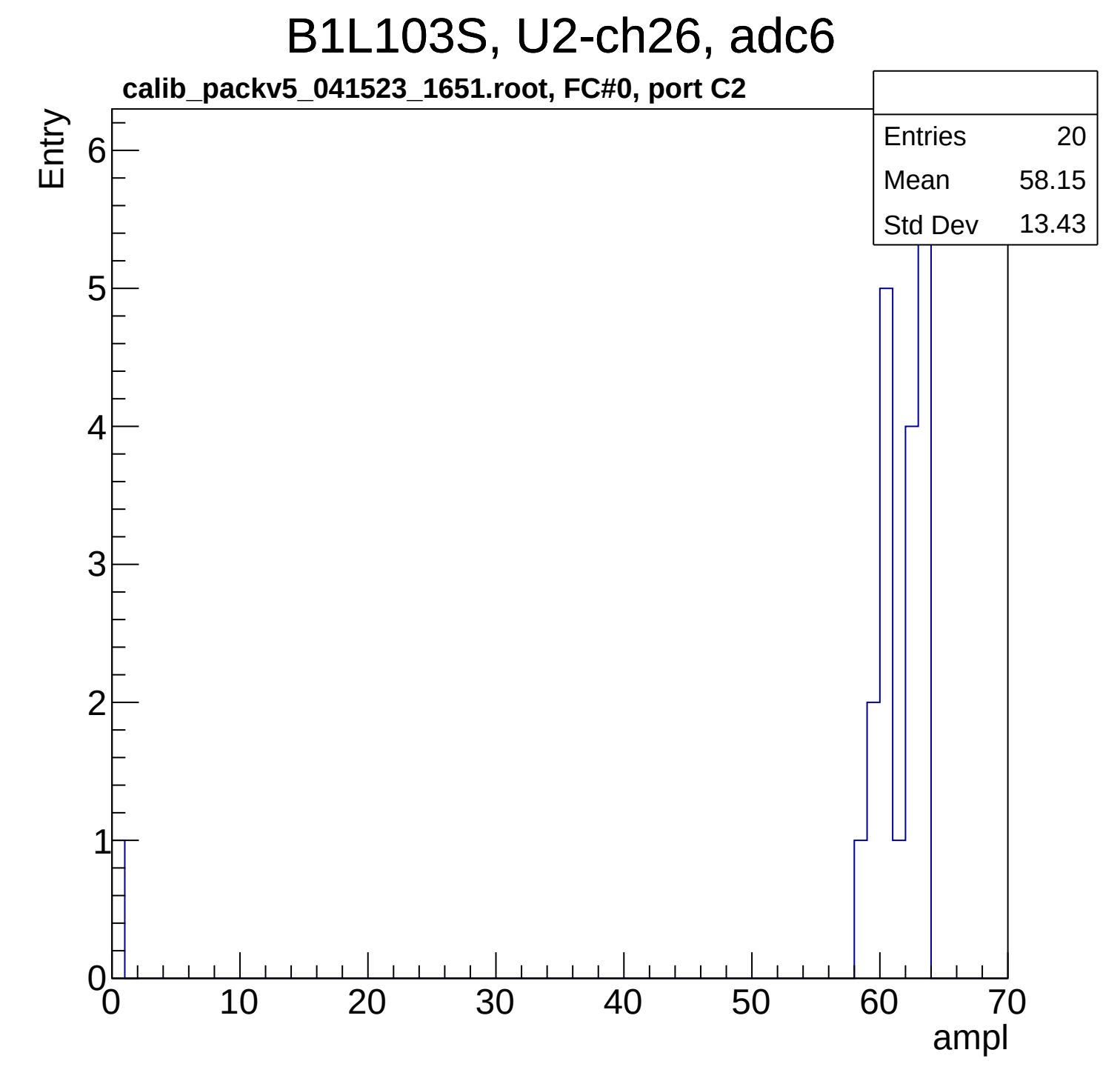

B1L103S, U2-ch26, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 107
Mean 30.79
Std Dev 12.04
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

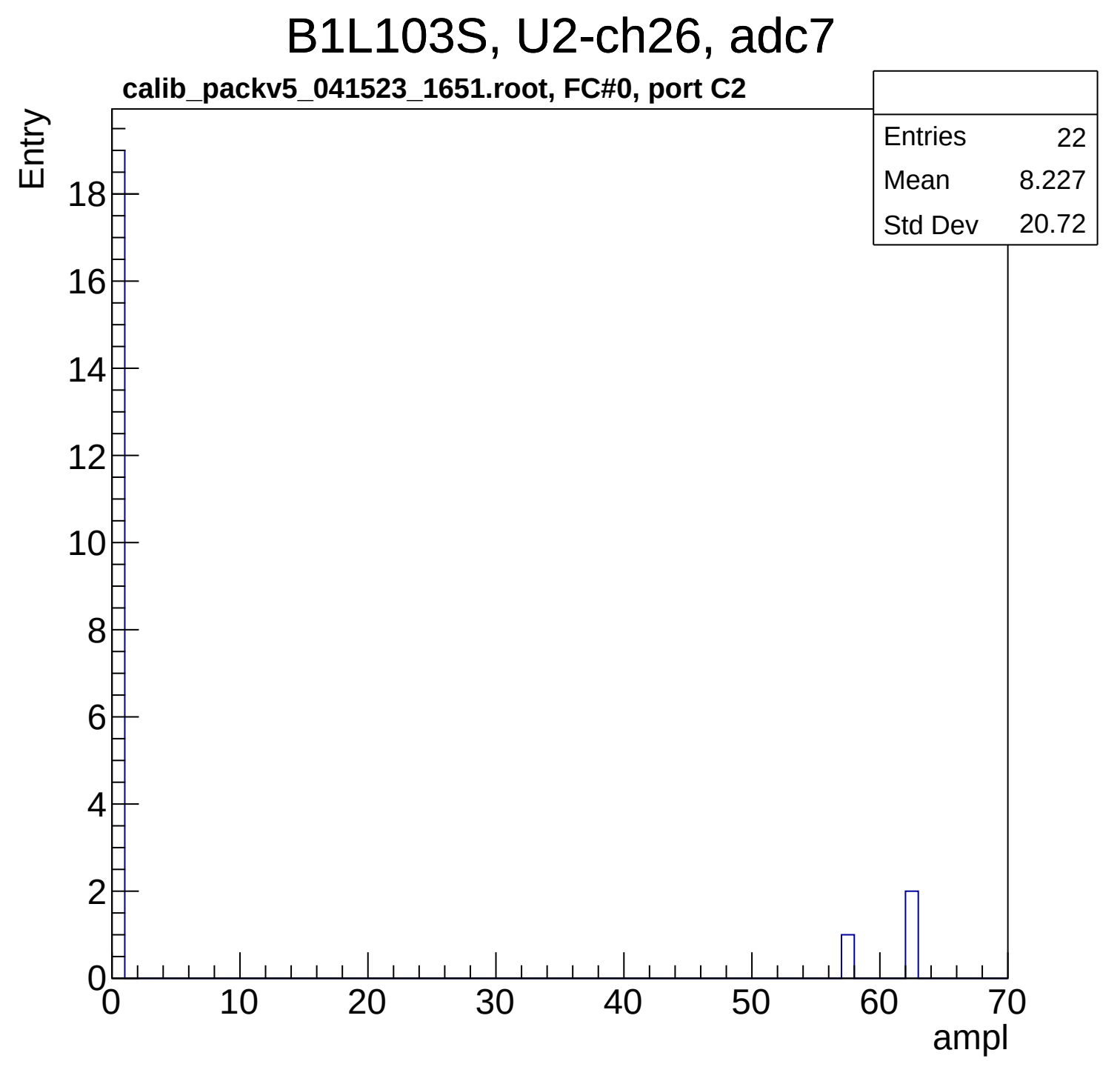

B1L103S, U2-ch26, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 41.26
Std Dev 6.854
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

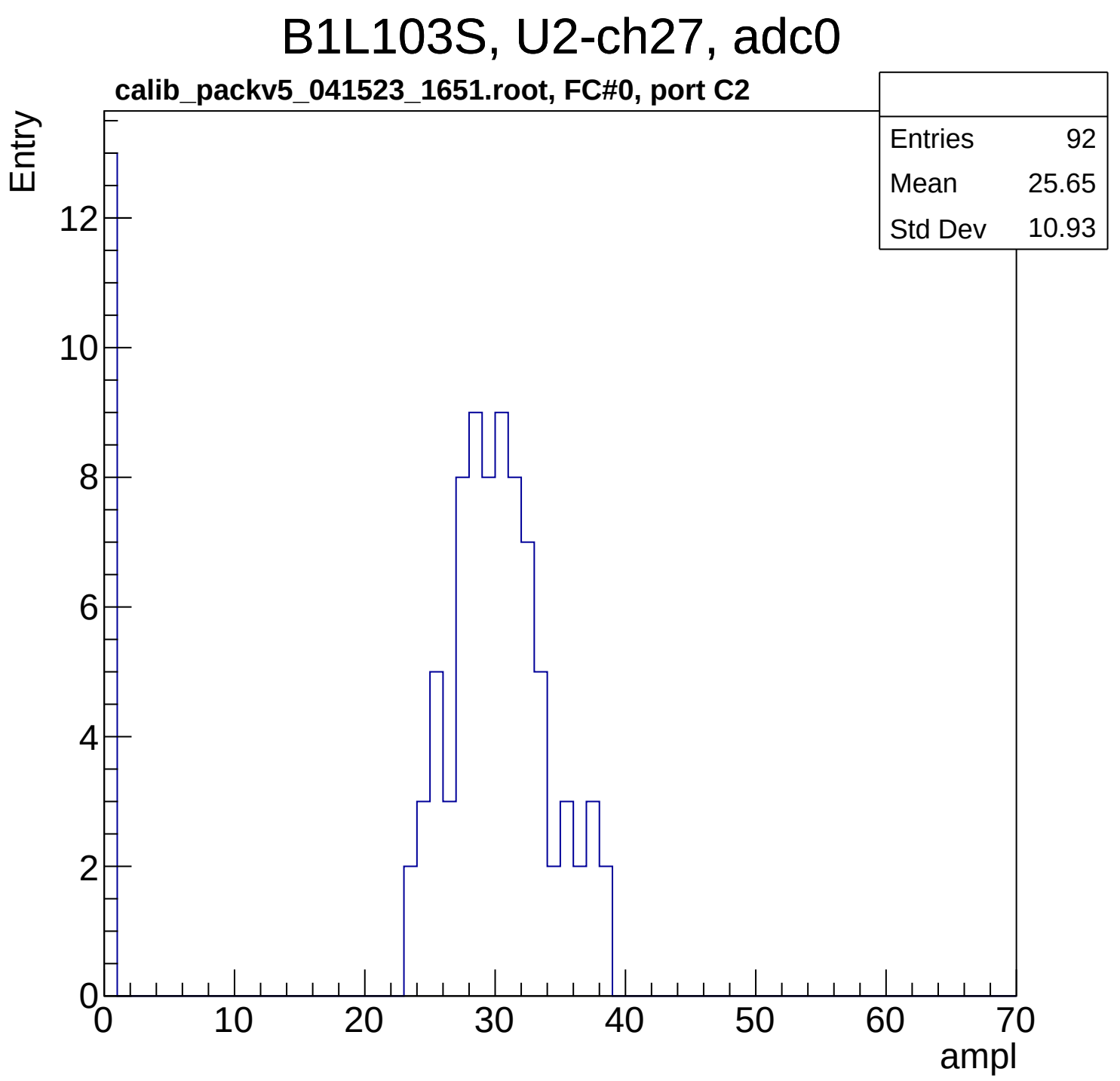

B1L103S, U2-ch26, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 47.34
Std Dev 3.772
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

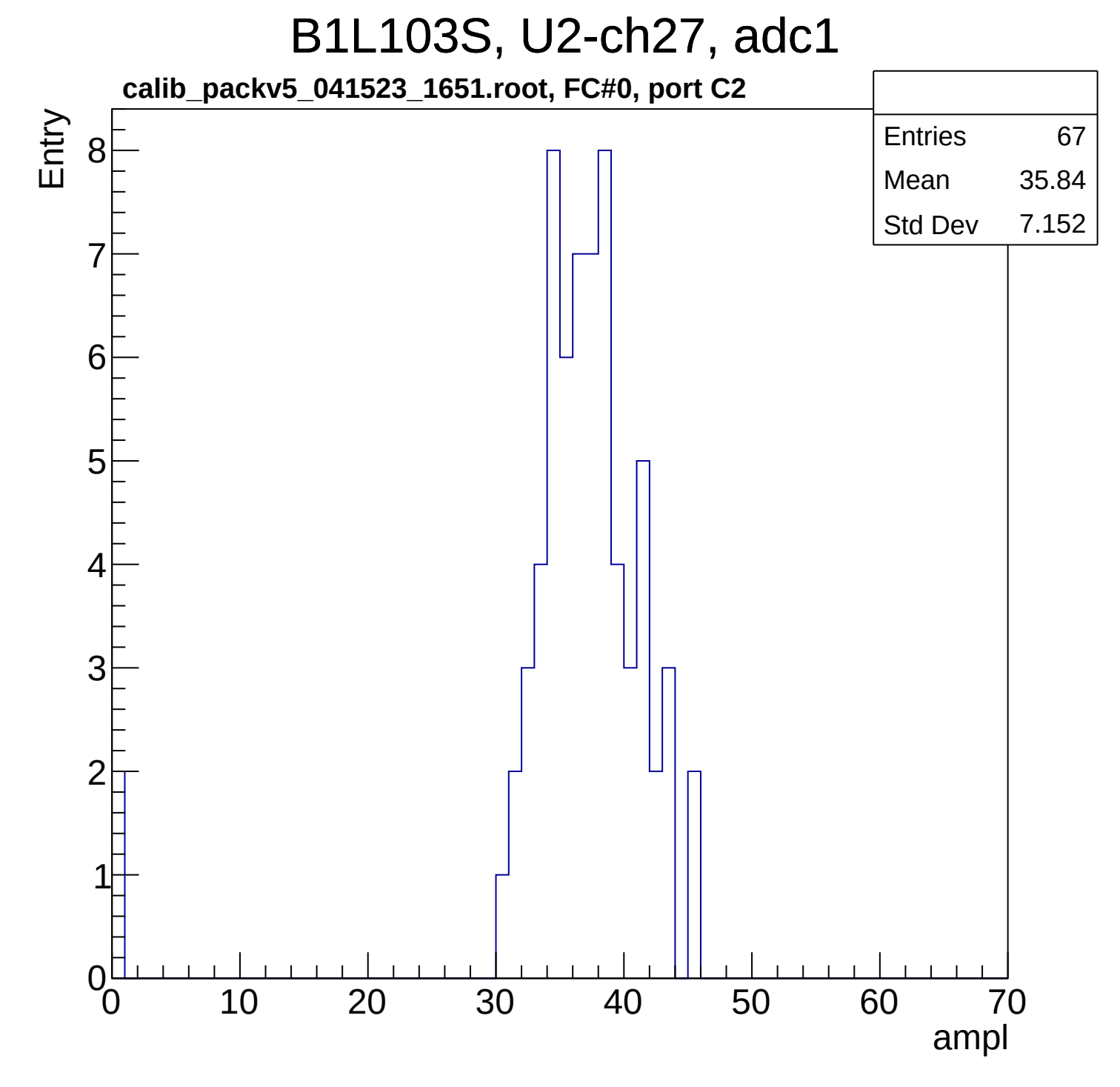

B1L103S, U2-ch26, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 53.66
Std Dev 3.804
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

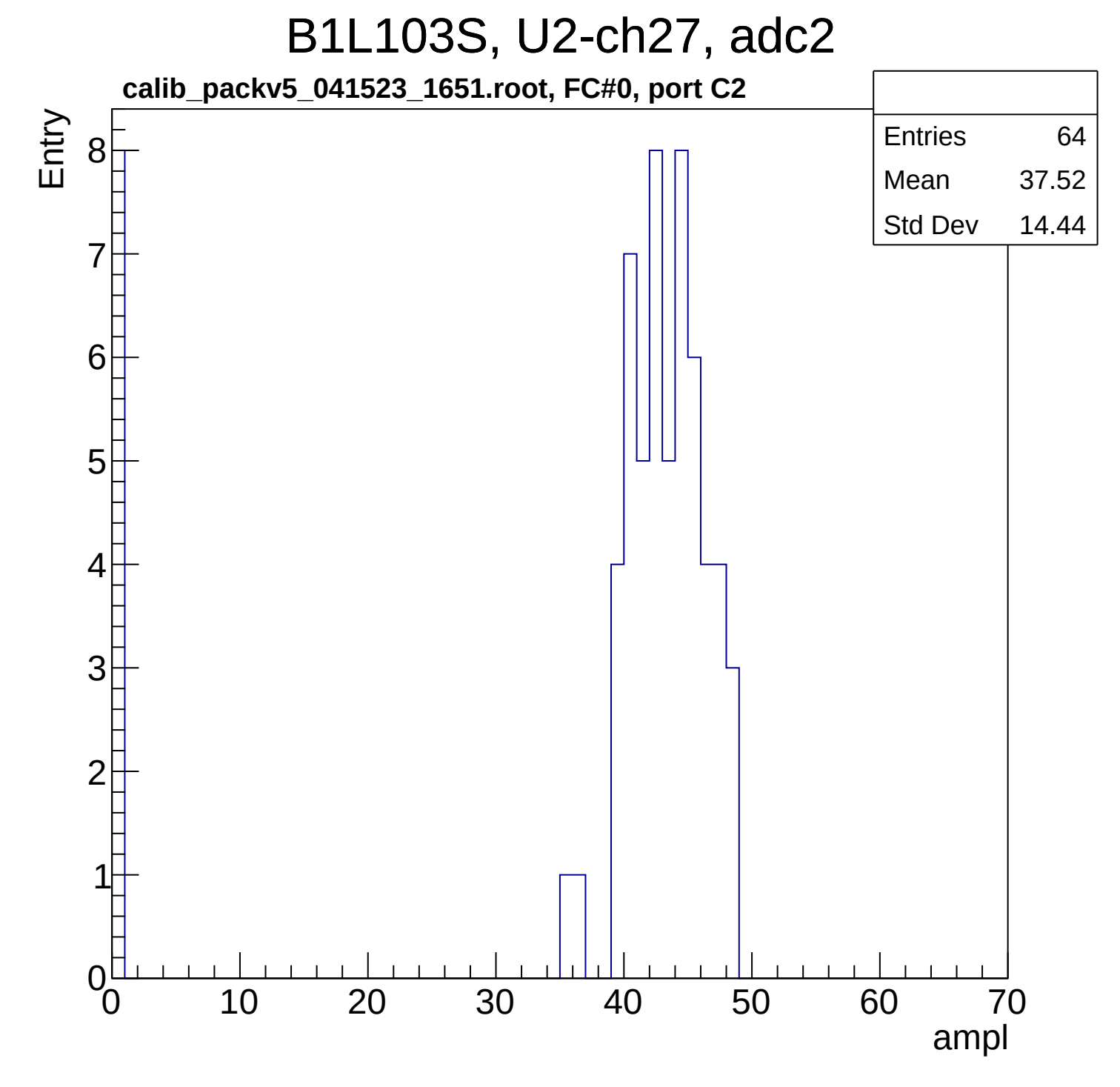

B1L103S, U2-ch26, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.13
Std Dev 3.411
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

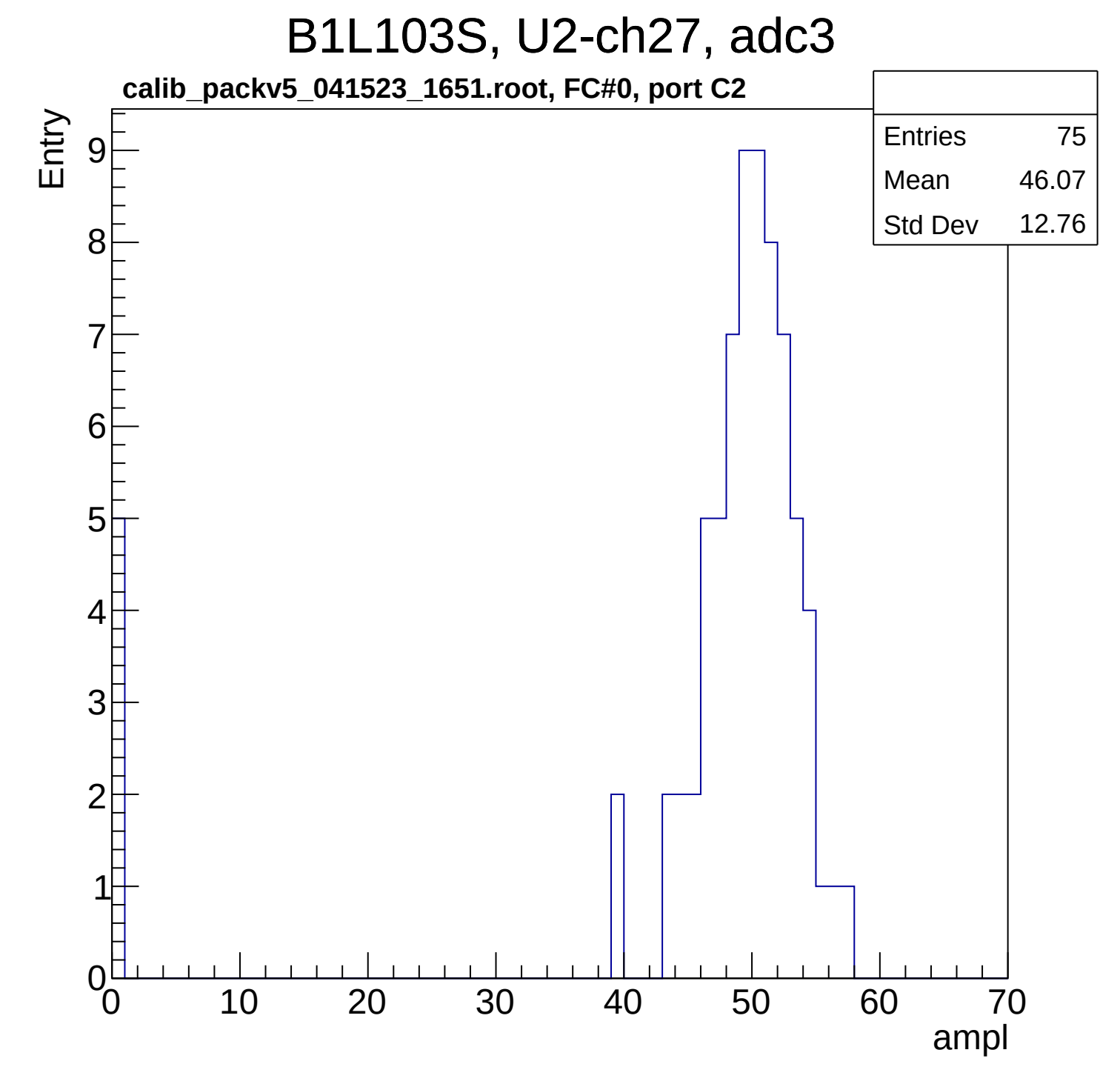

B1L103S, U2-ch26, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 58.15
Std Dev 13.43
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

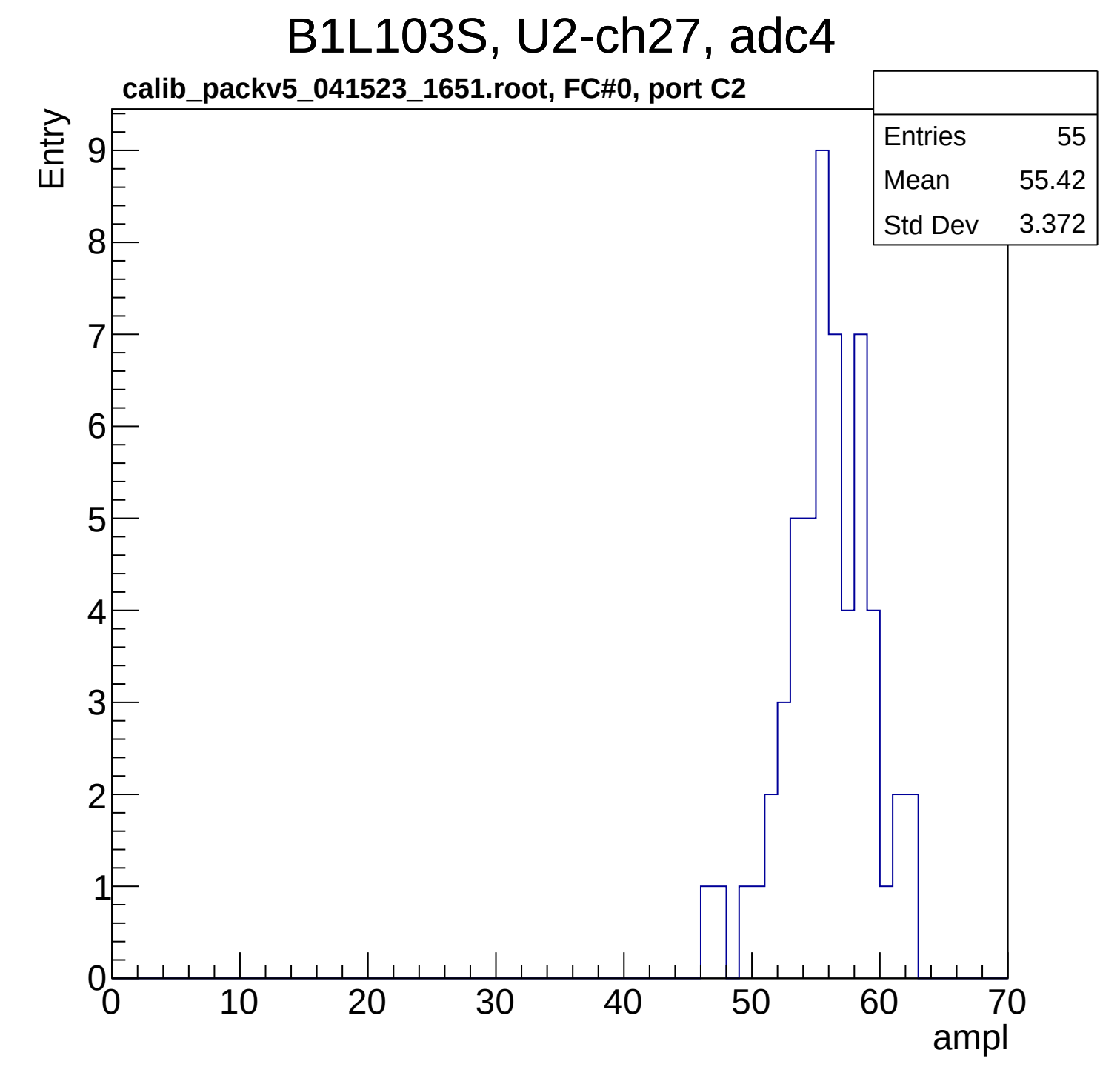

B1L103S, U2-ch26, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.227
Std Dev 20.72
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

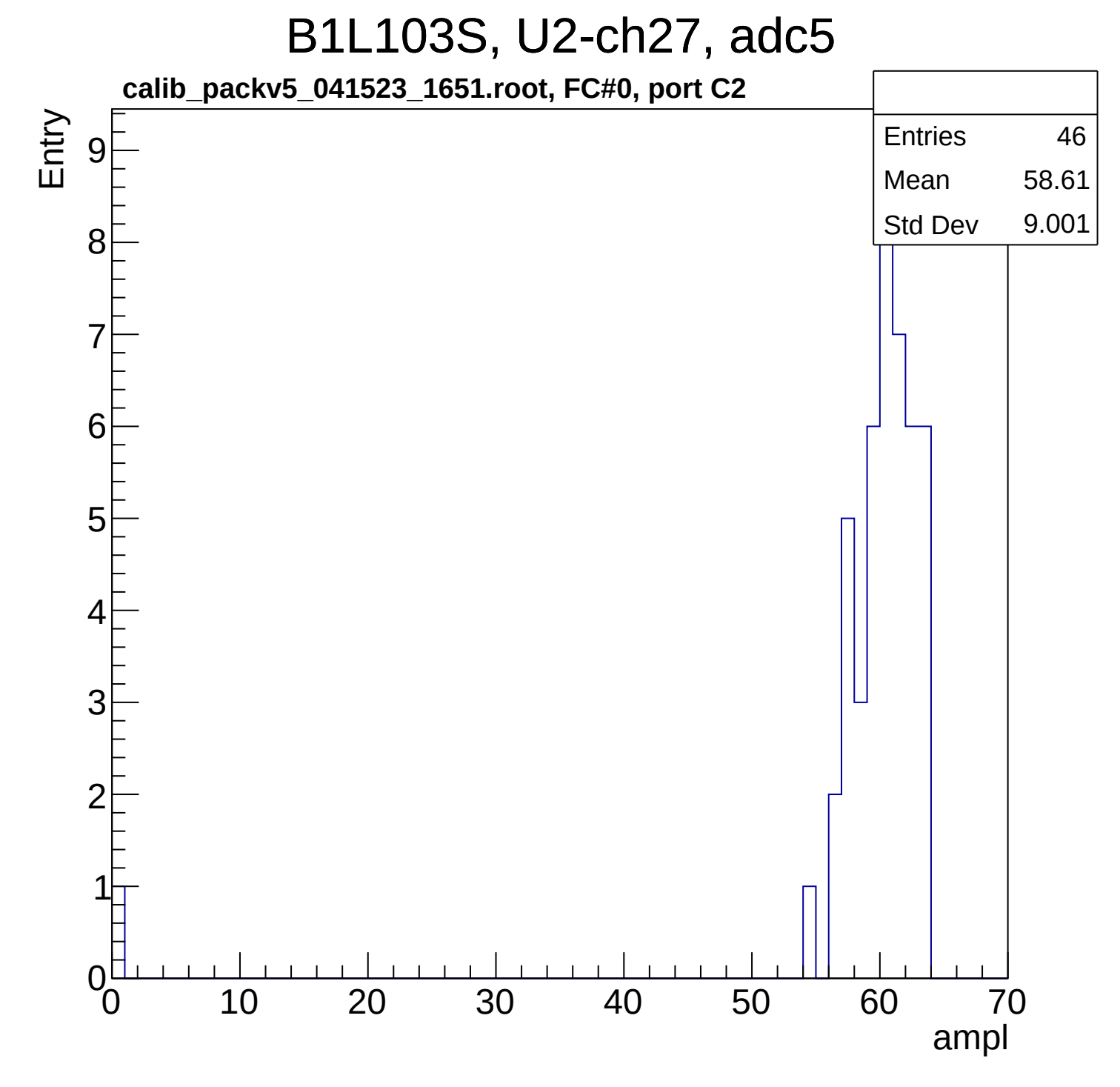

B1L103S, U2-ch27, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 25.65
Std Dev 10.93
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

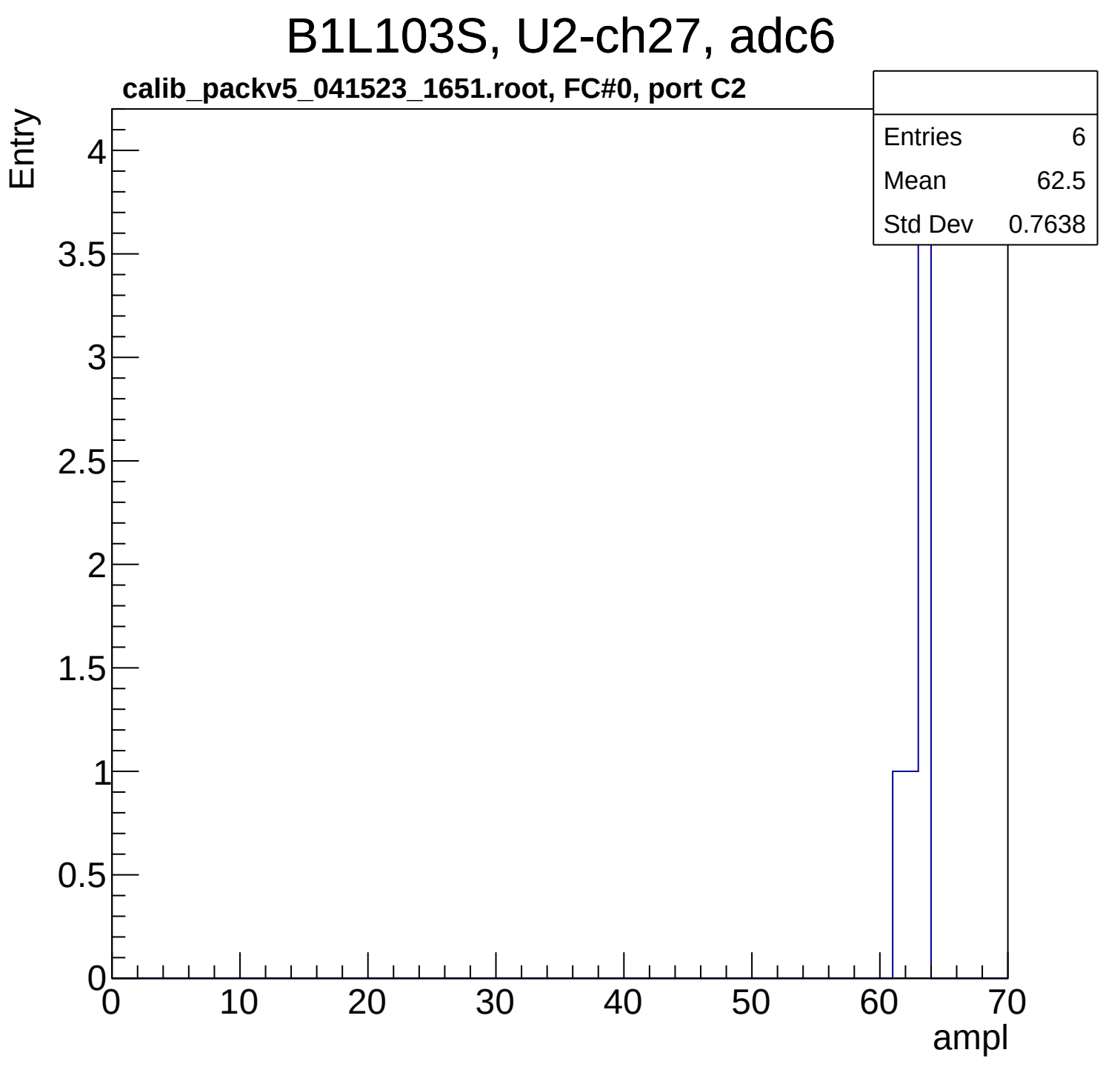

B1L103S, U2-ch27, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 35.84
Std Dev 7.152
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

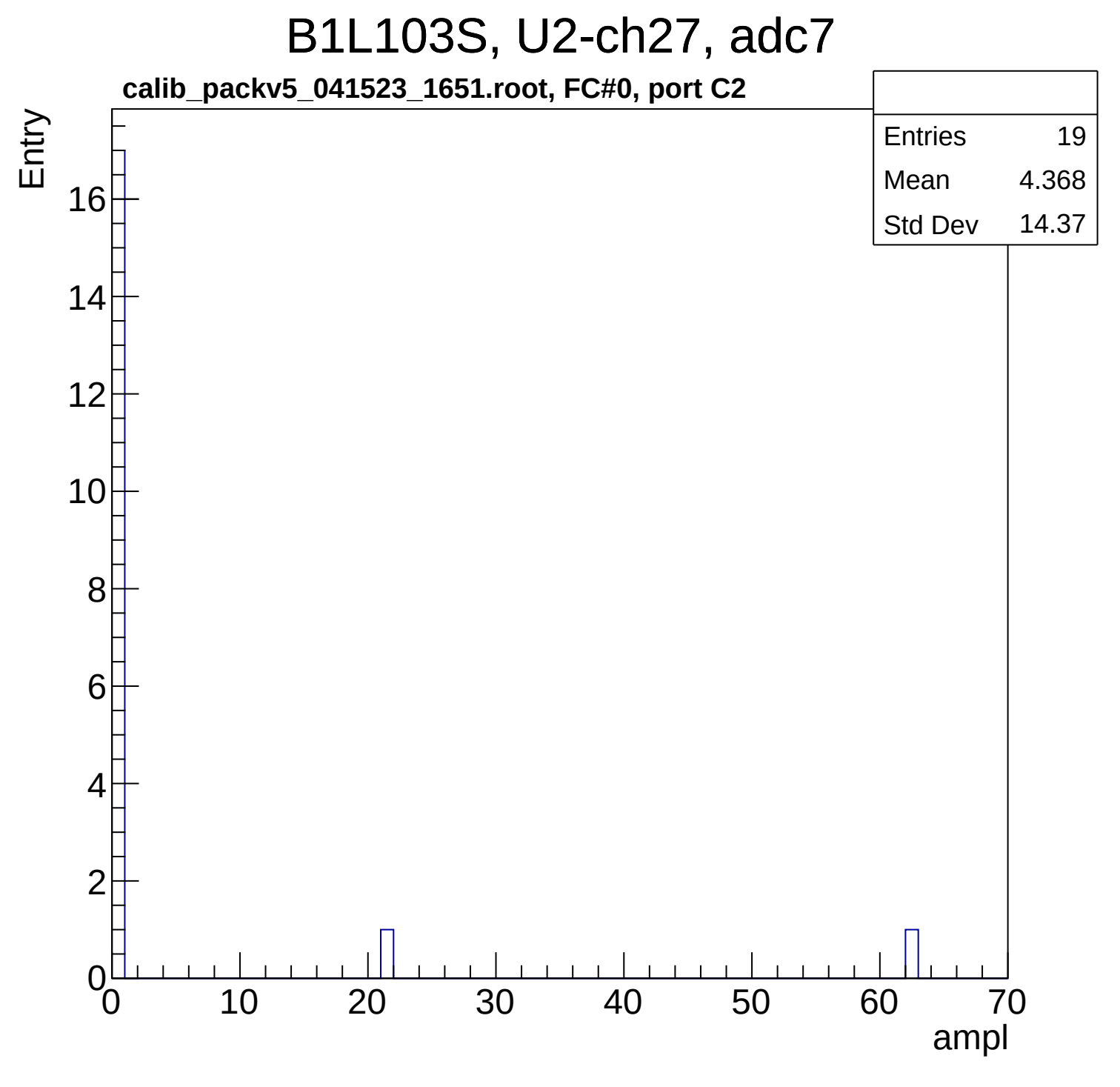

B1L103S, U2-ch27, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 37.52
Std Dev 14.44
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

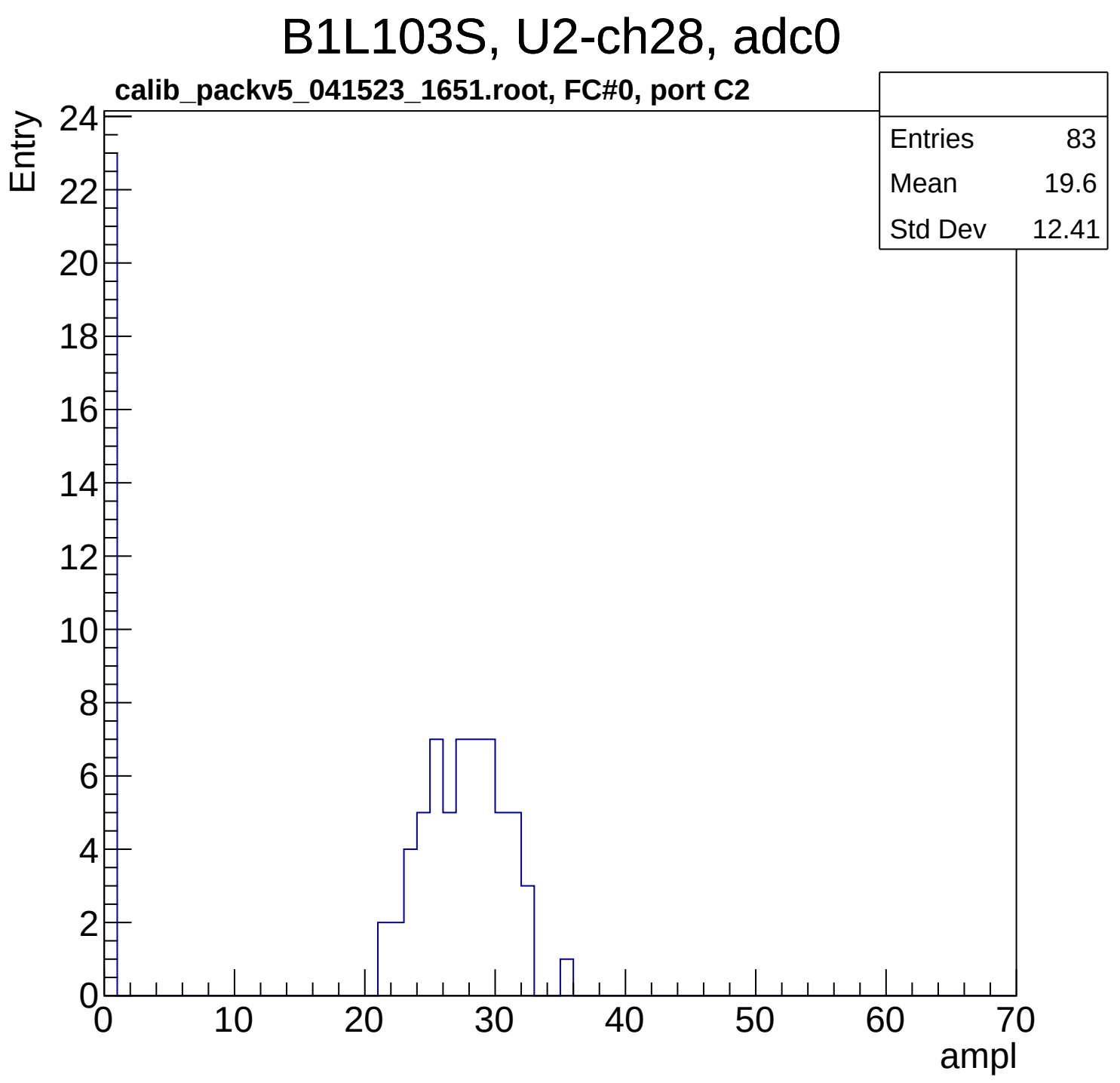

B1L103S, U2-ch27, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 46.07
Std Dev 12.76
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

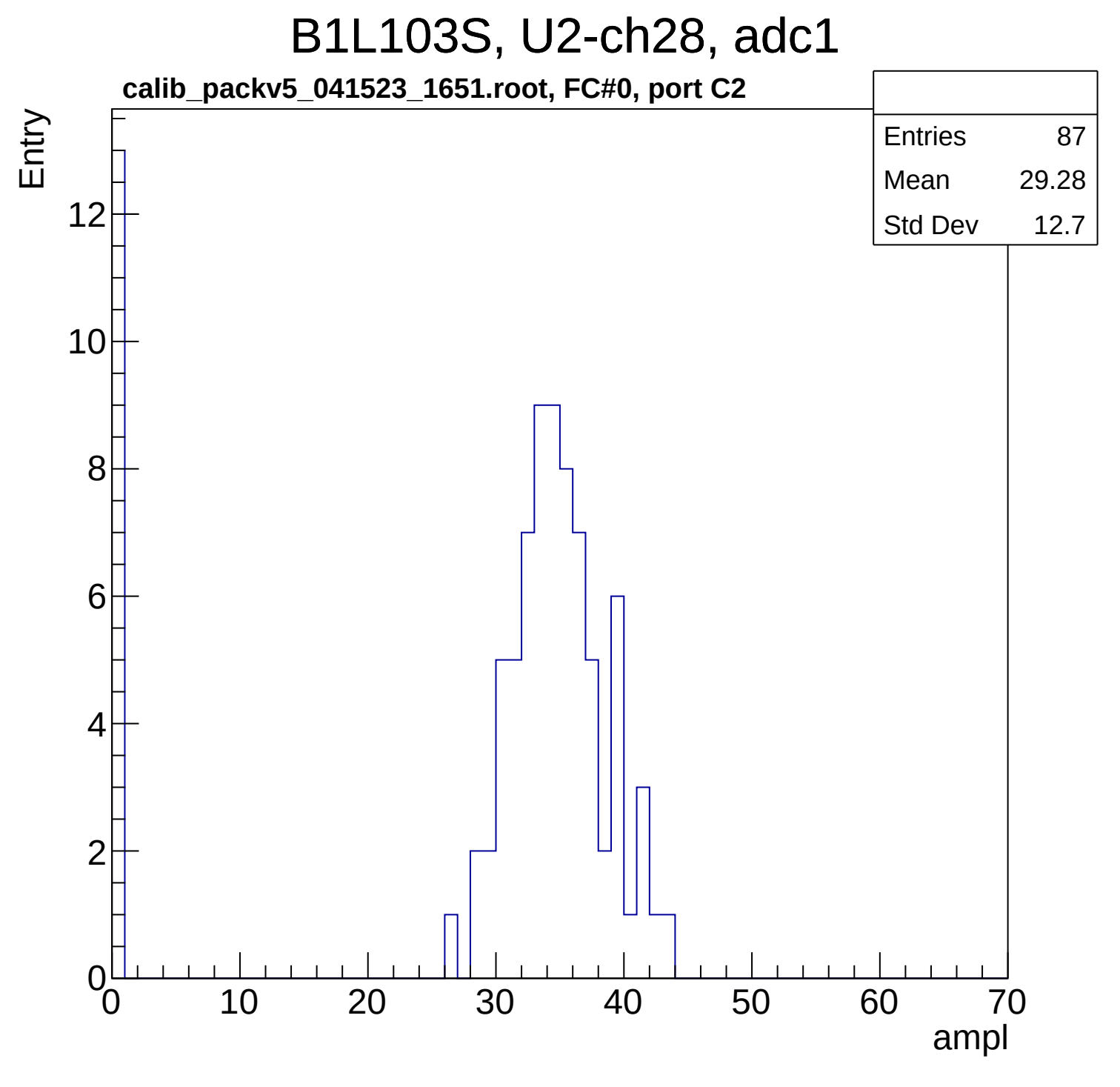

B1L103S, U2-ch27, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 55.42
Std Dev 3.372
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

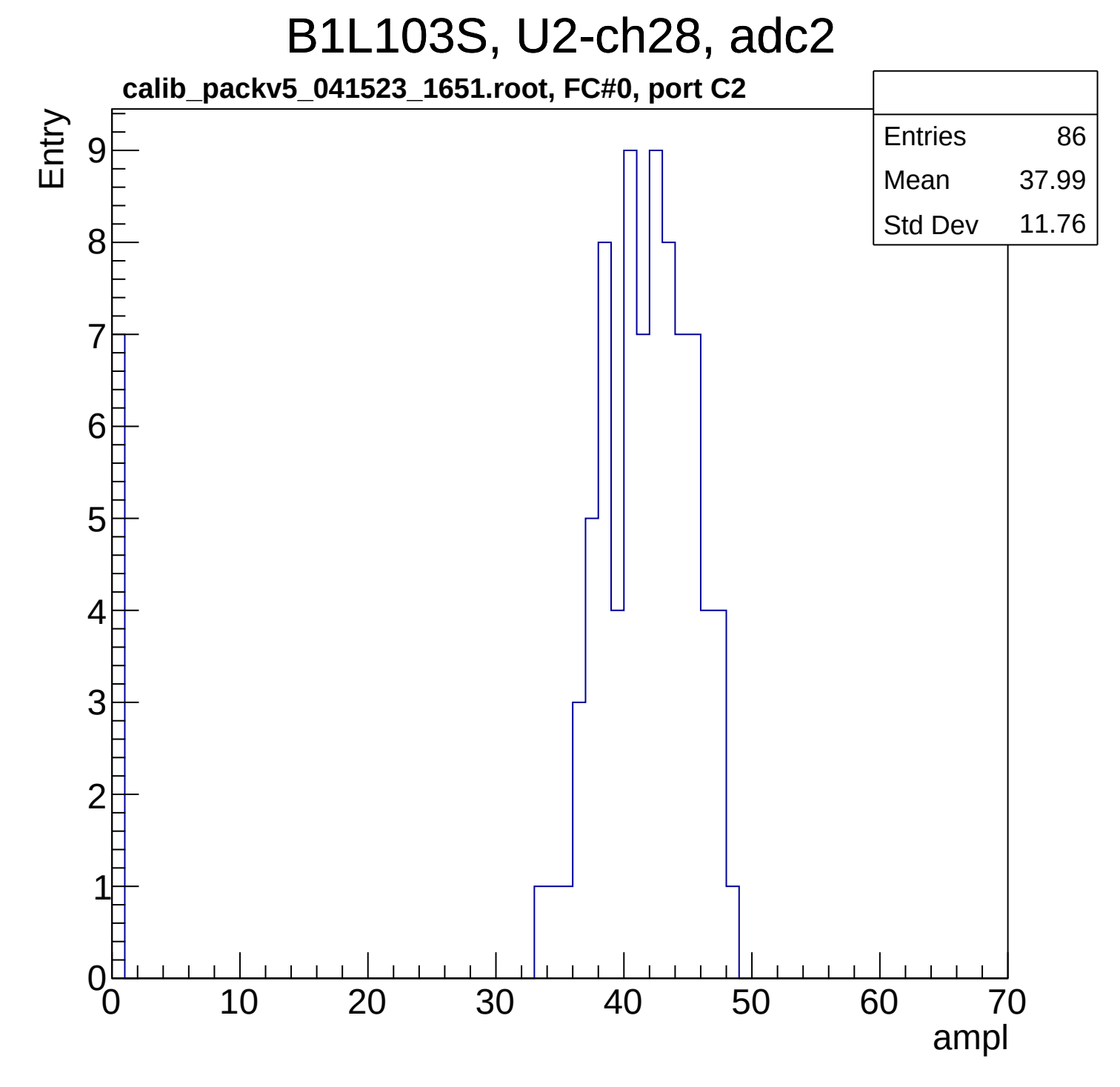

B1L103S, U2-ch27, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.61
Std Dev 9.001
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

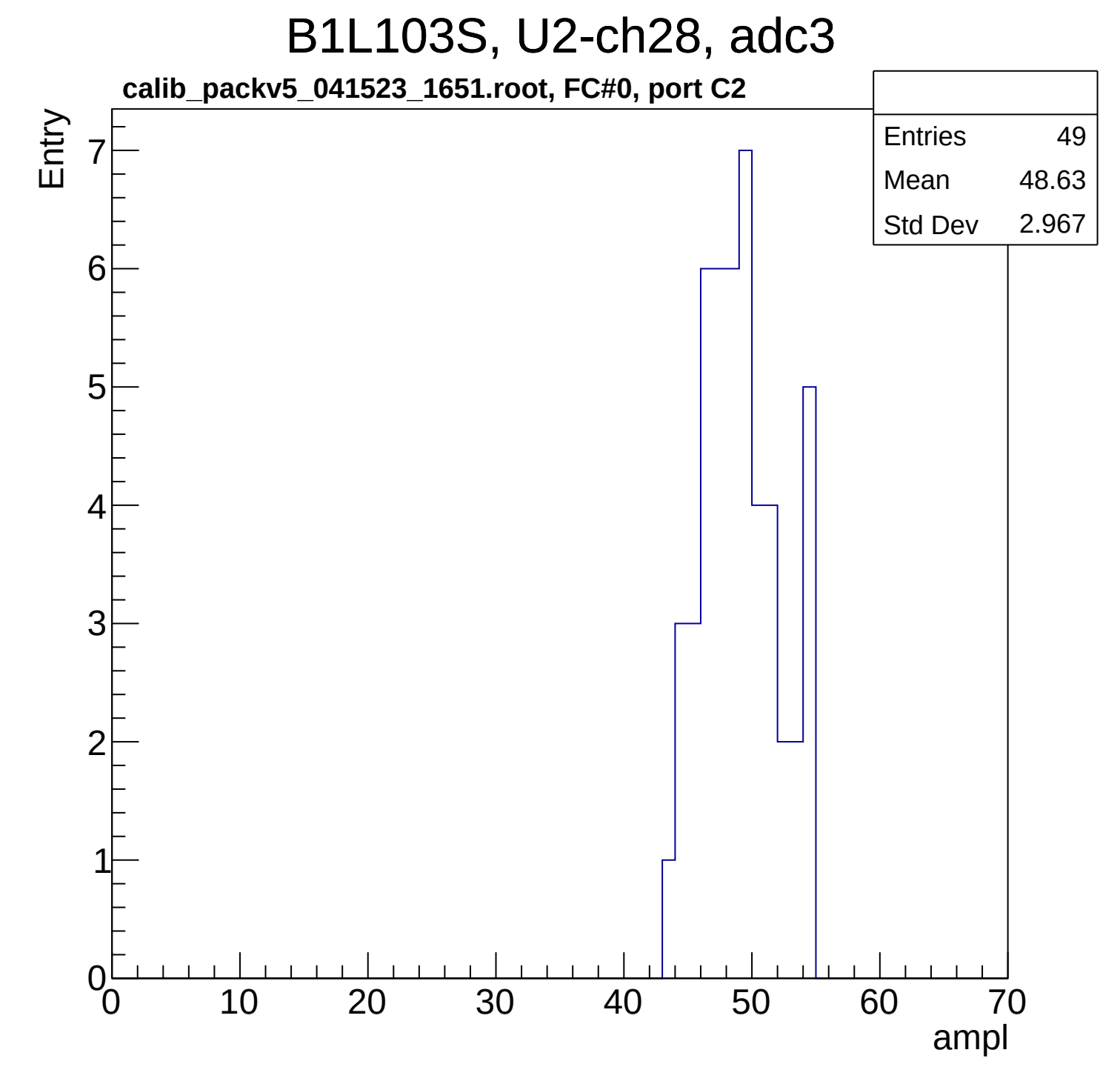

B1L103S, U2-ch27, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.5
Std Dev 0.7638
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

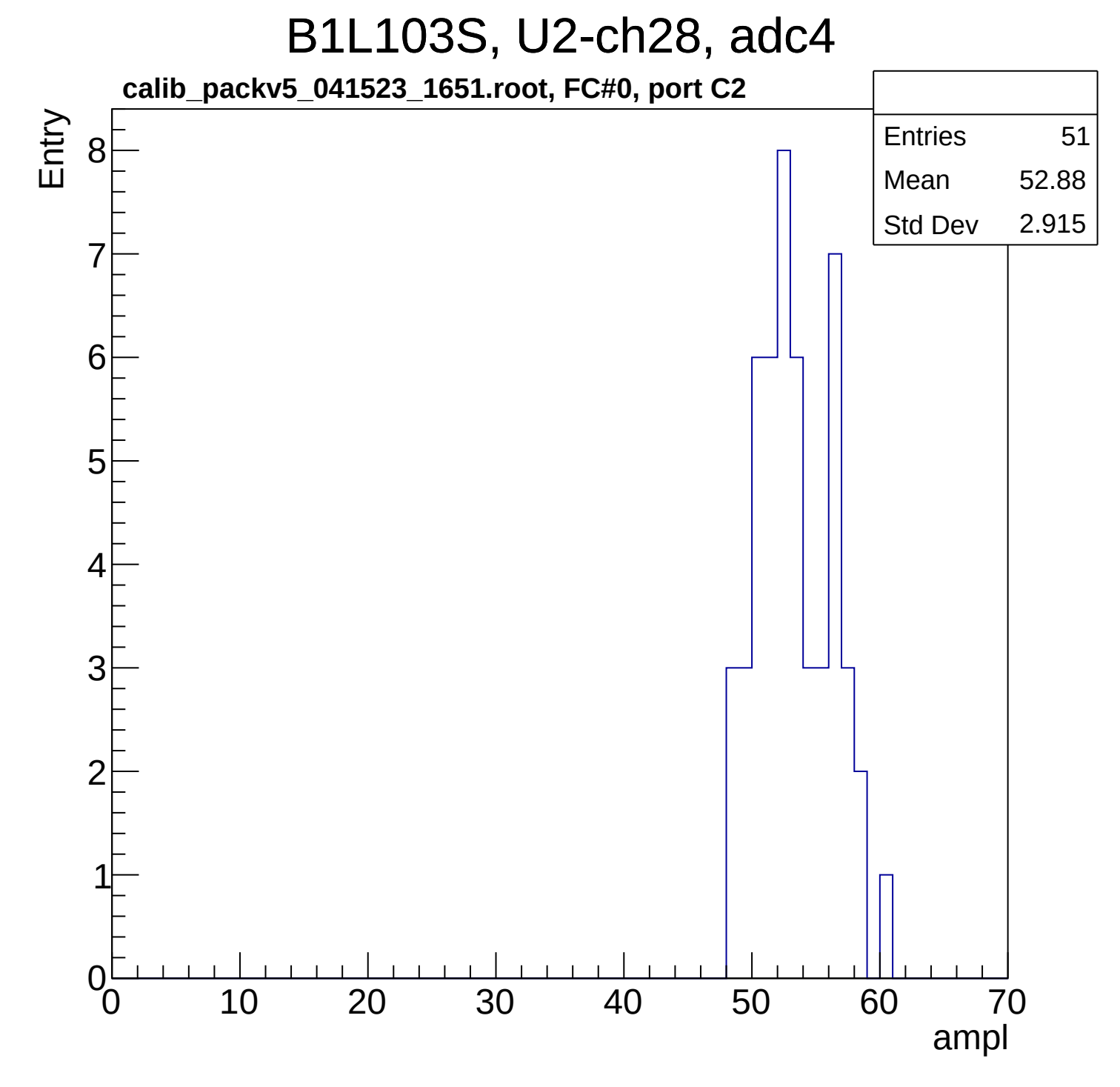

B1L103S, U2-ch27, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 4.368
Std Dev 14.37
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

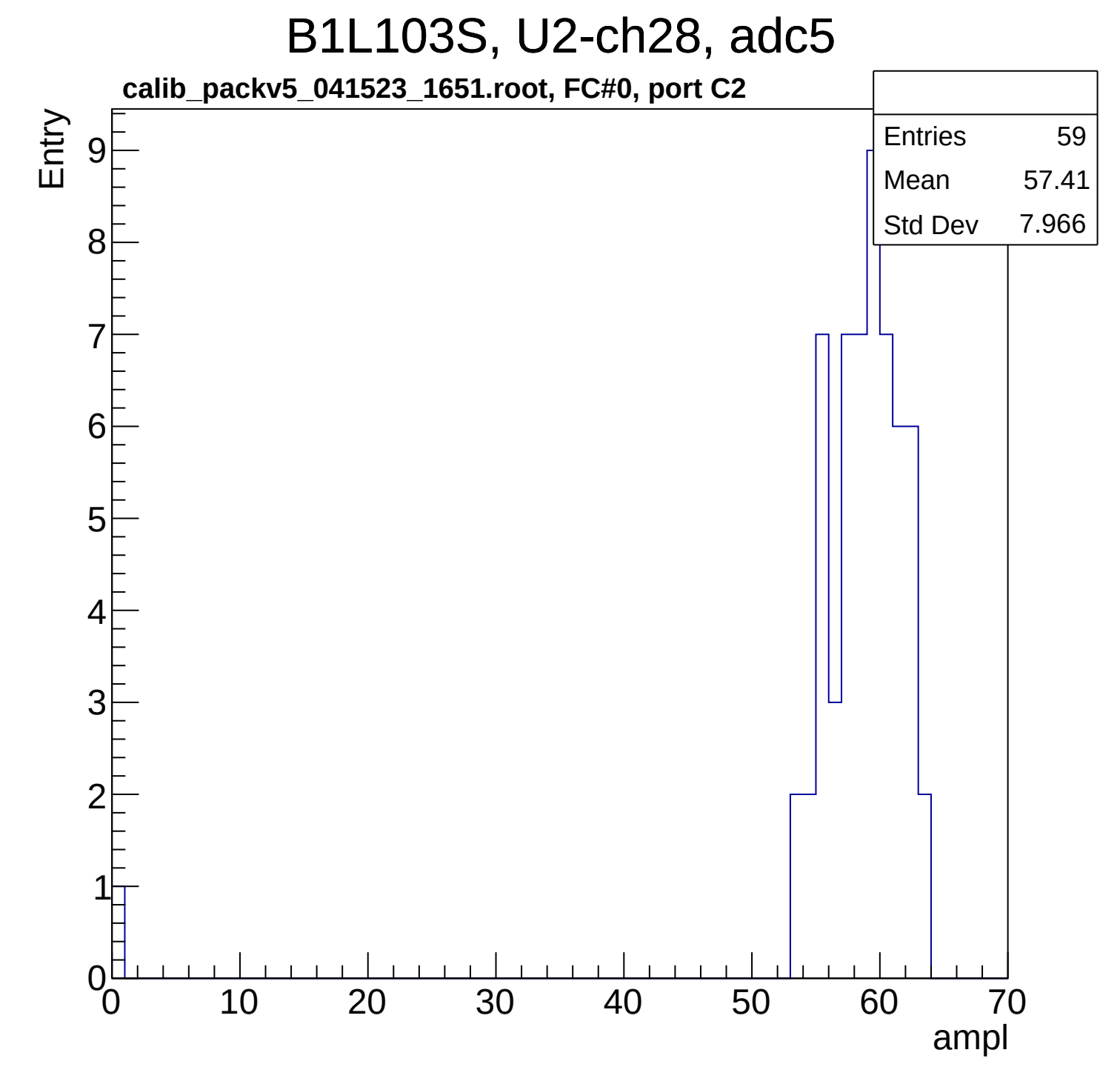

B1L103S, U2-ch28, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 19.6
Std Dev 12.41
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70

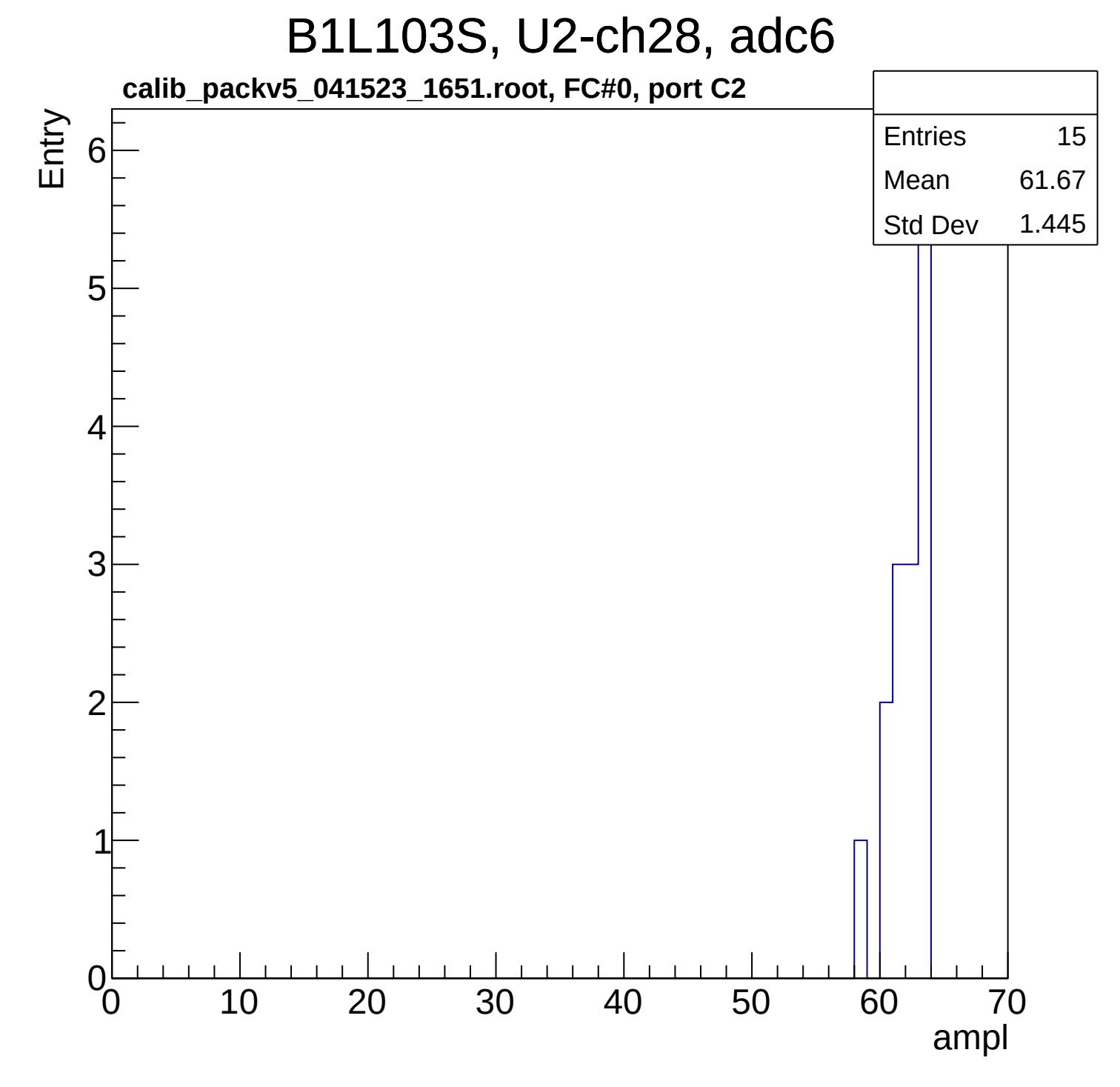

B1L103S, U2-ch28, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 29.28
Std Dev 12.7
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

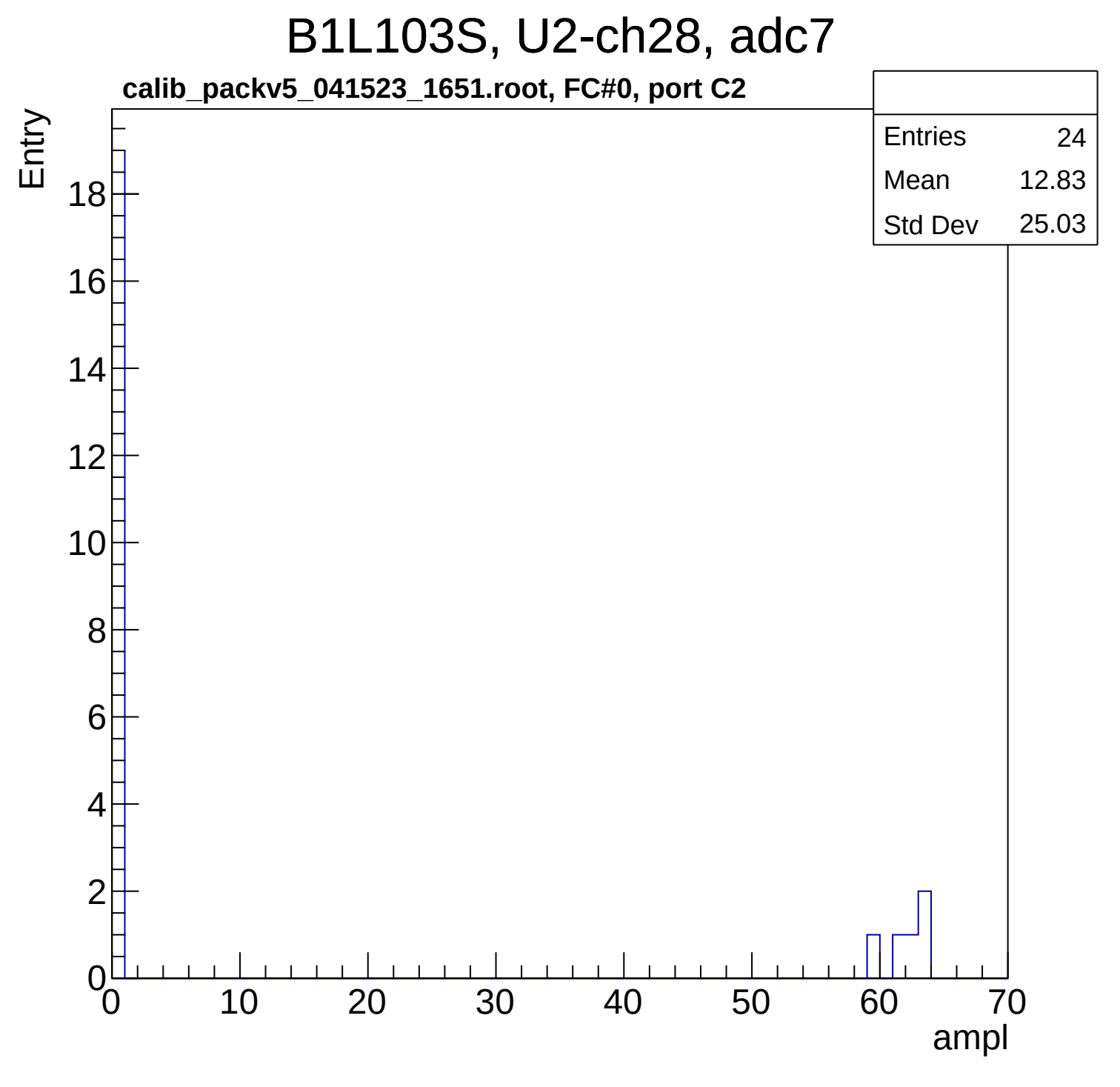

B1L103S, U2-ch28, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 37.99
Std Dev 11.76
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

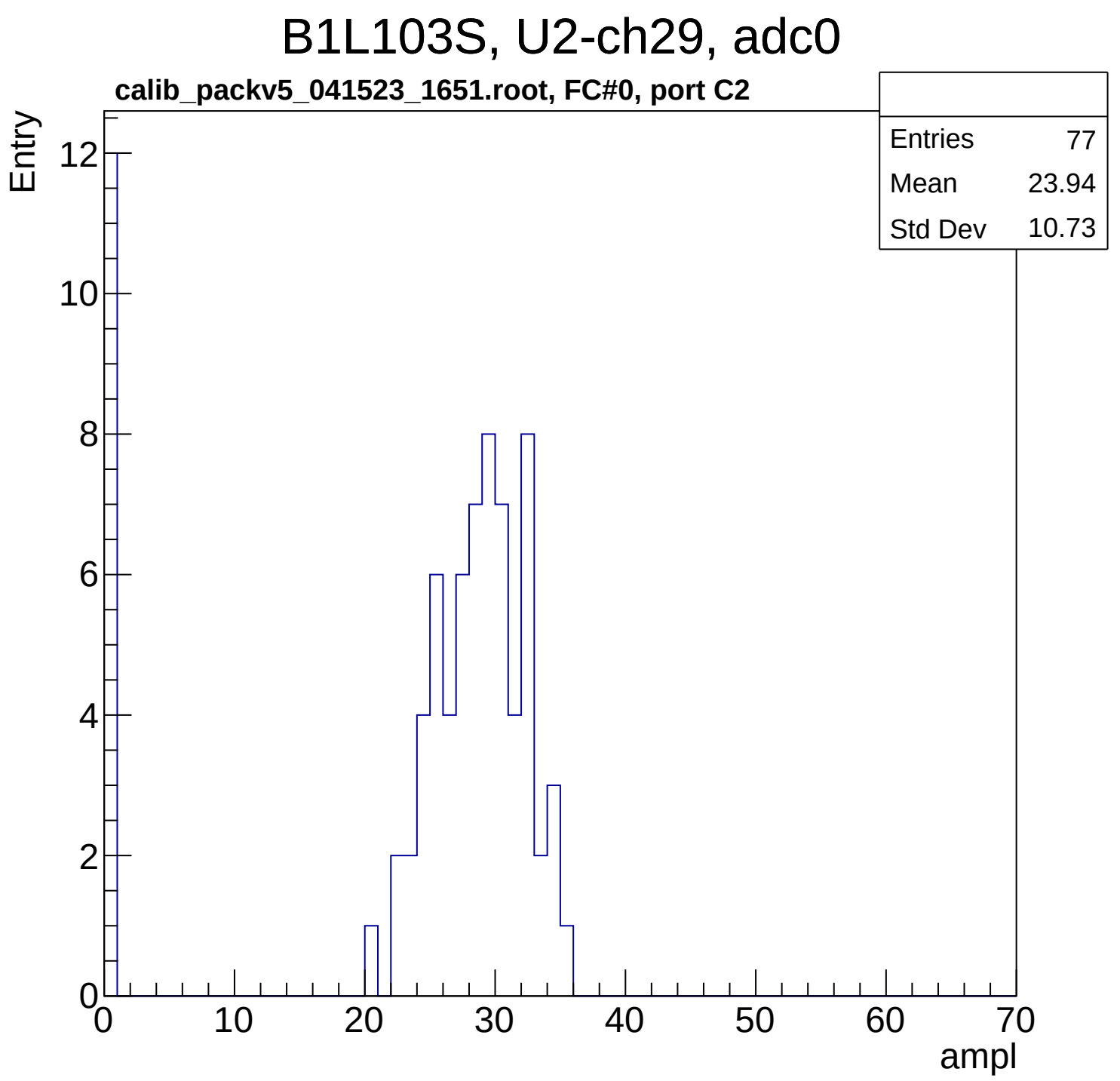

B1L103S, U2-ch28, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 48.63
Std Dev 2.967
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

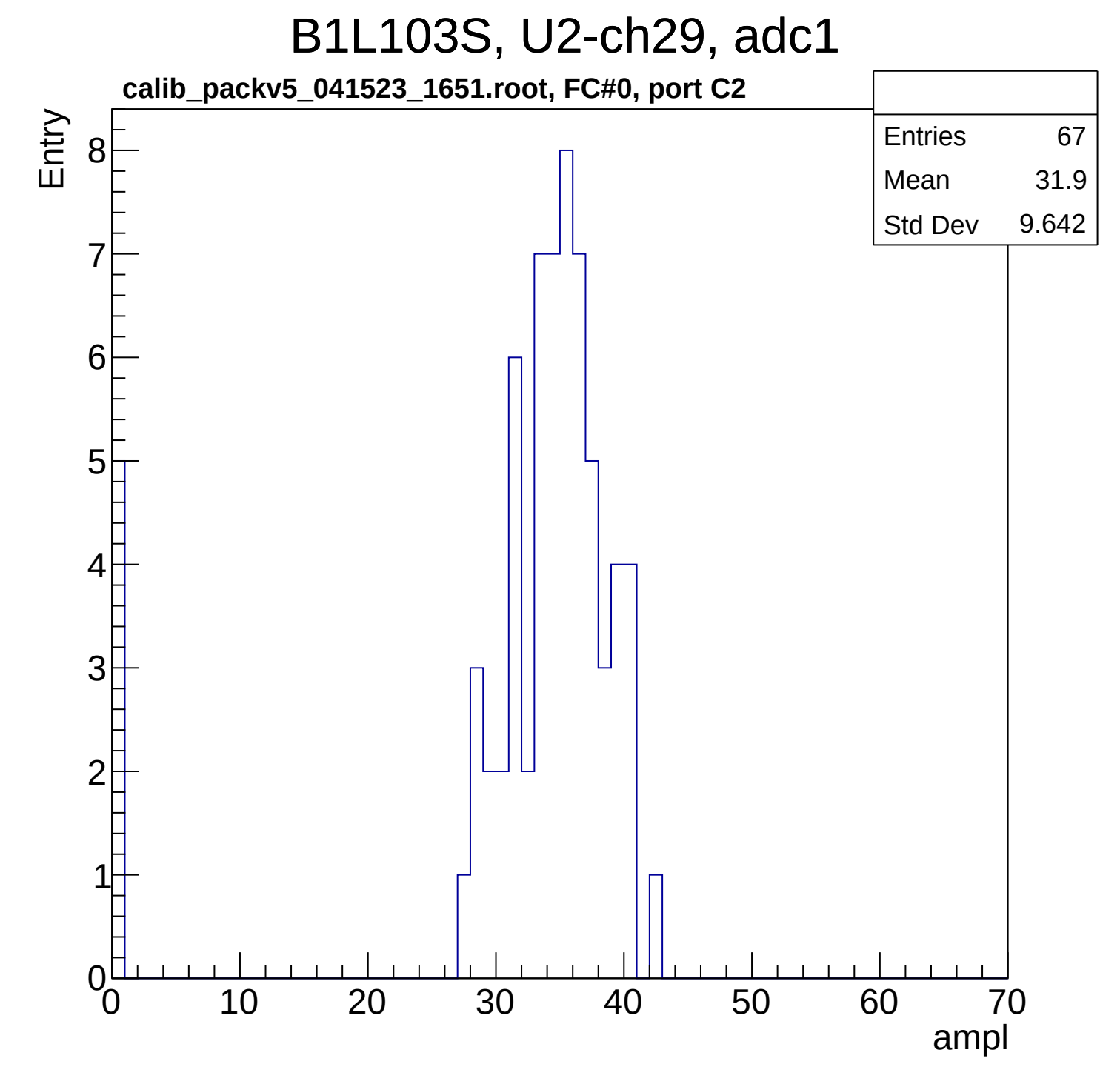

B1L103S, U2-ch28, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 52.88
Std Dev 2.915
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

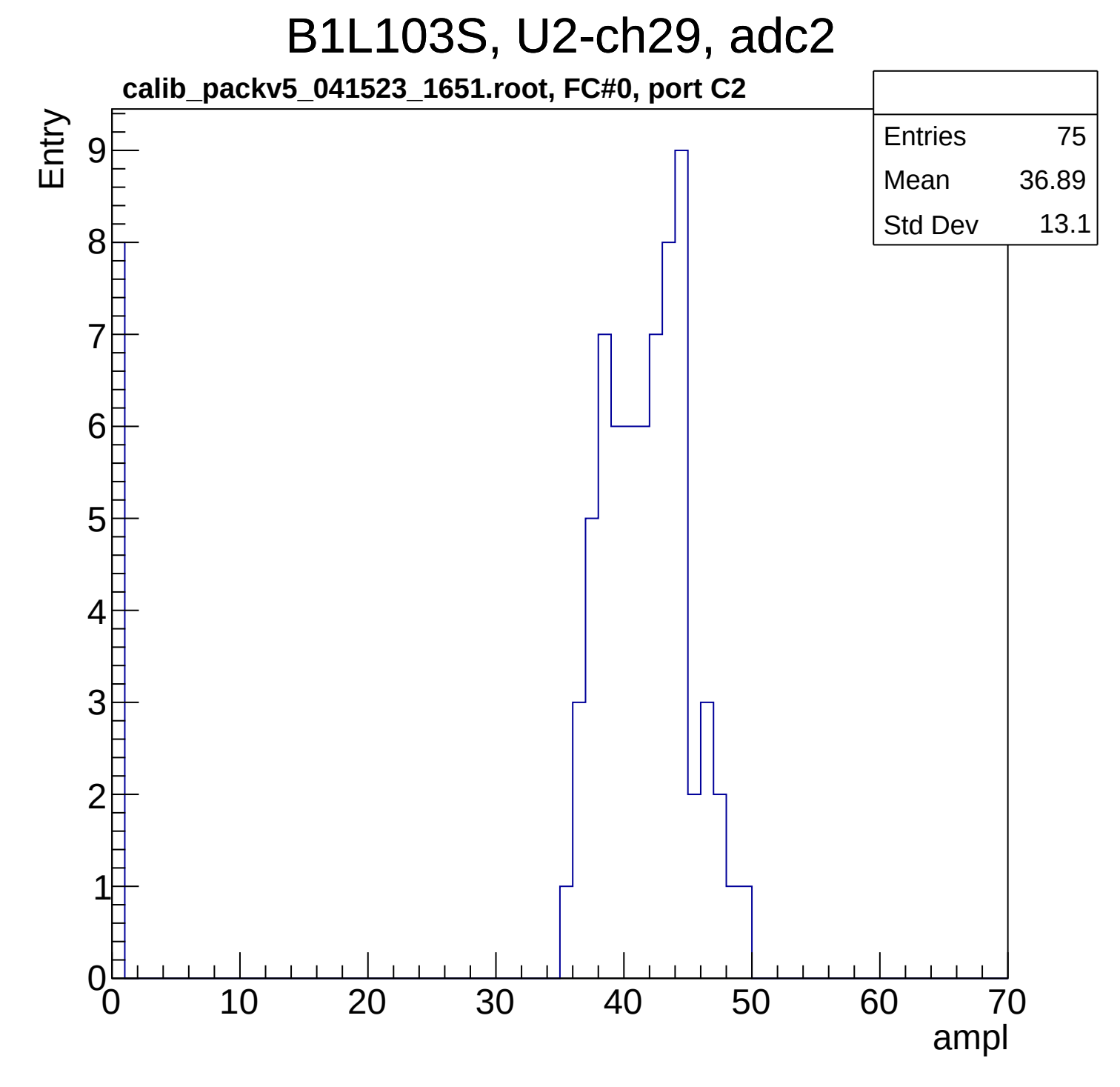

B1L103S, U2-ch28, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 57.41
Std Dev 7.966
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

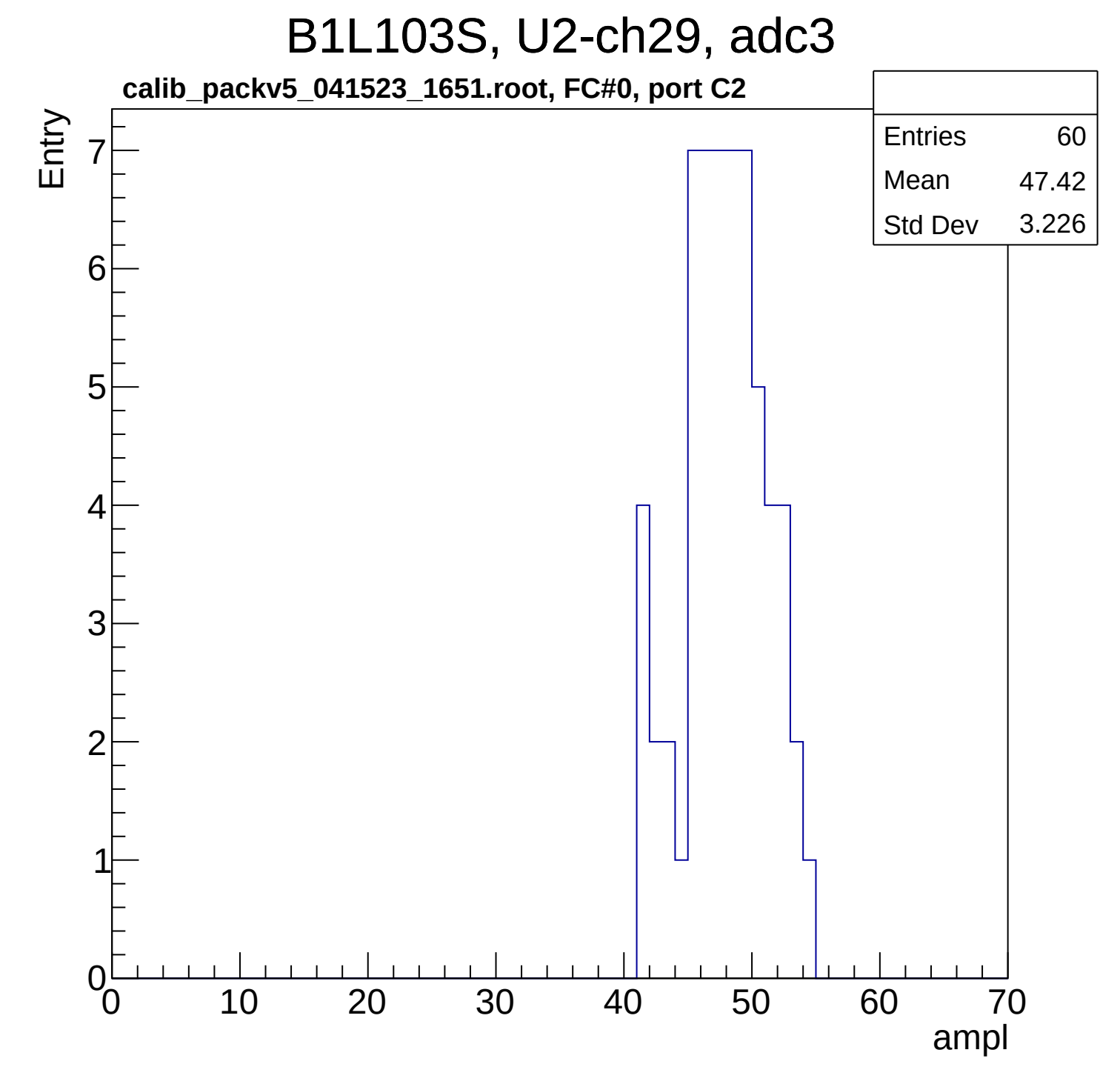

B1L103S, U2-ch28, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.67
Std Dev 1.445
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

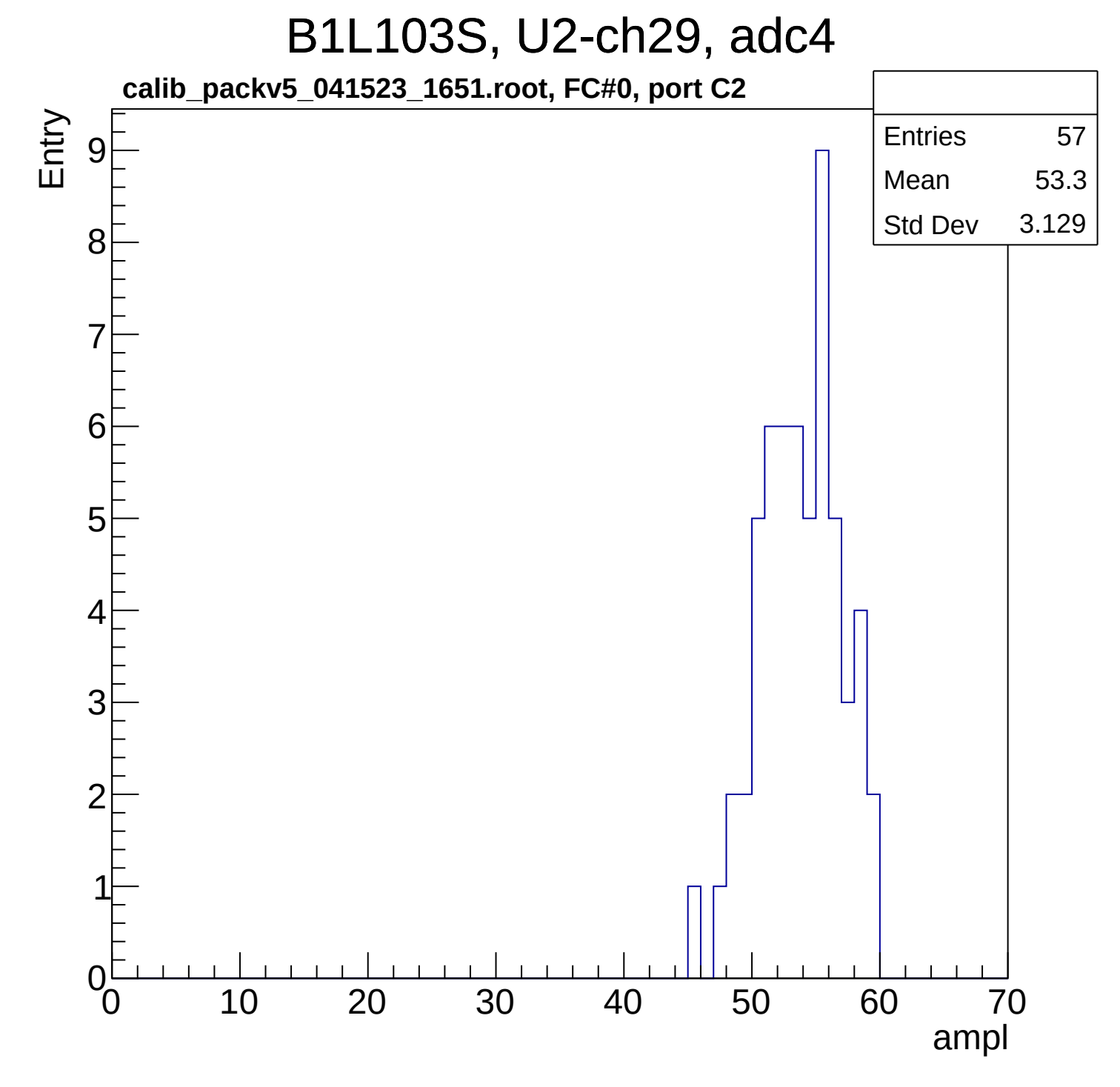

B1L103S, U2-ch28, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 12.83
Std Dev 25.03
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

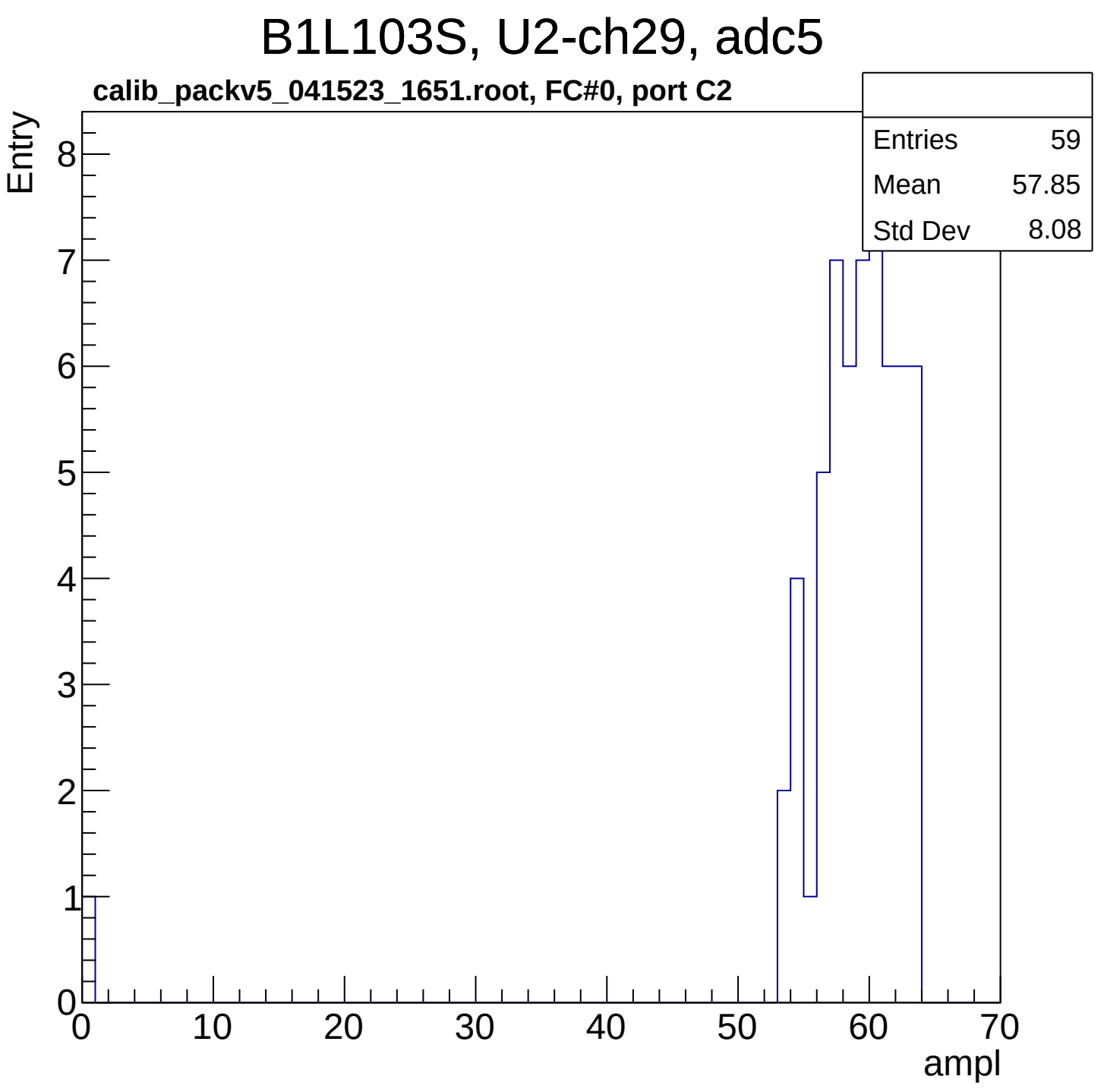

B1L103S, U2-ch29, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 23.94
Std Dev 10.73
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

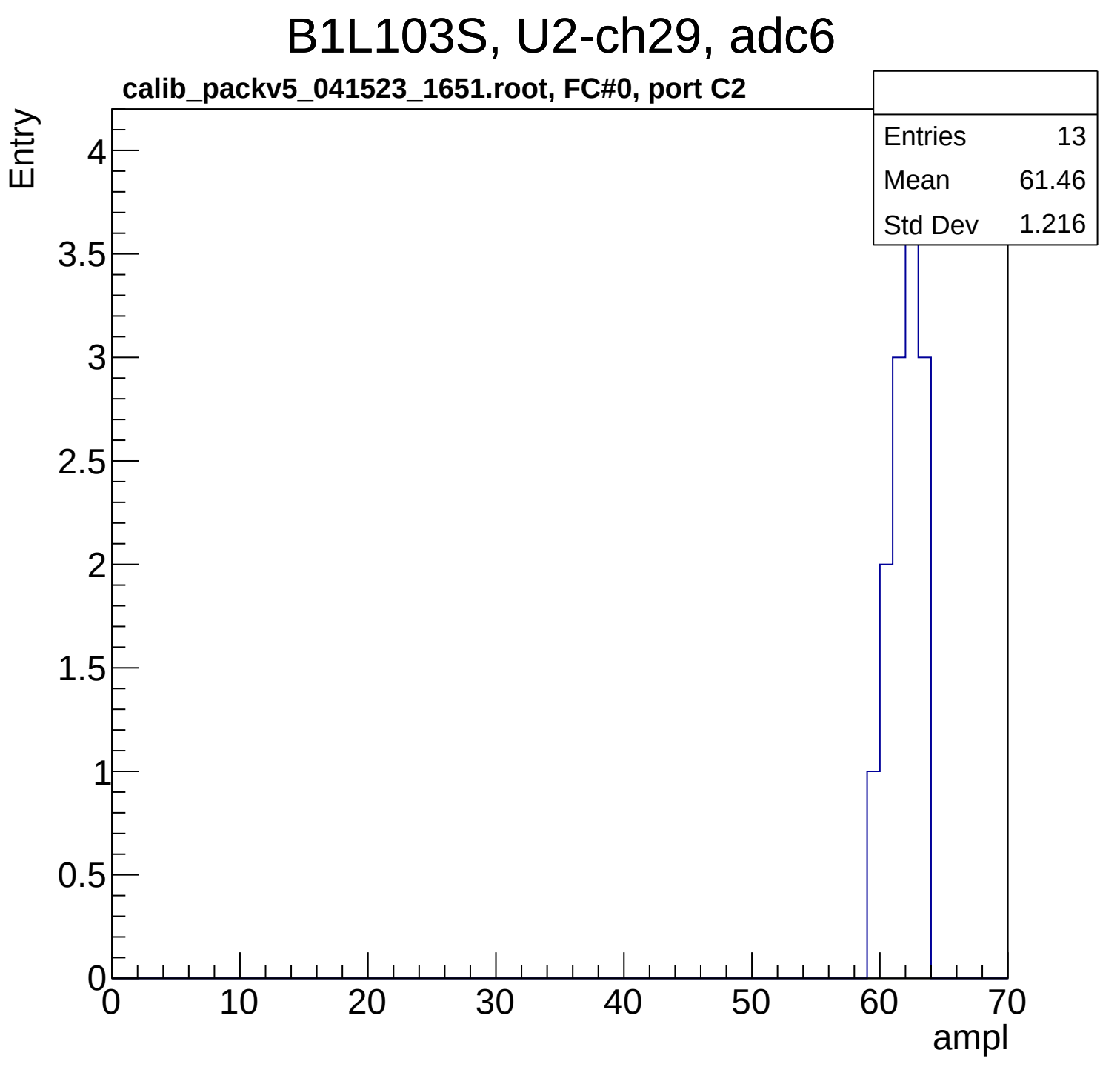

B1L103S, U2-ch29, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 31.9
Std Dev 9.642
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

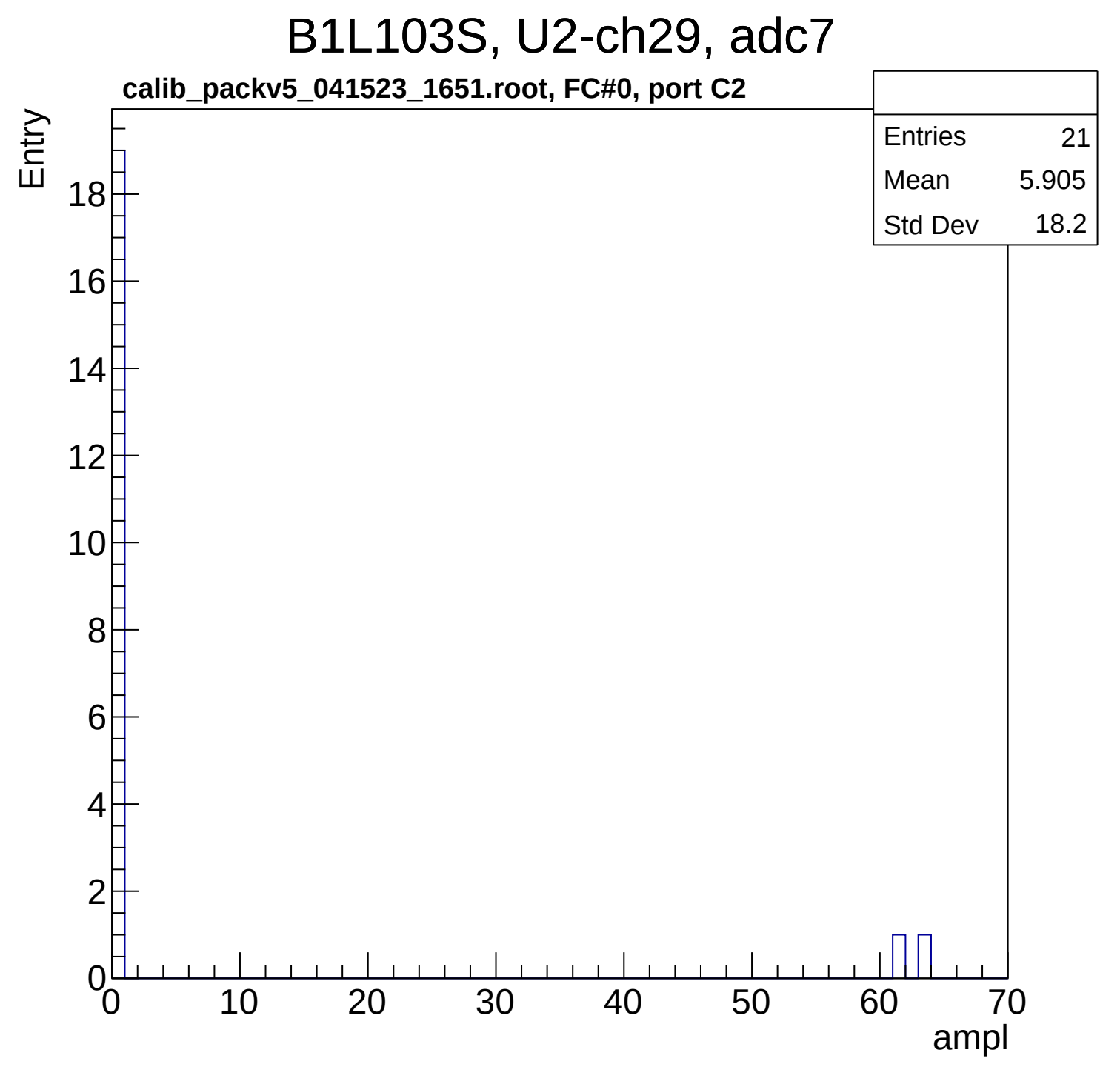

B1L103S, U2-ch29, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 36.89
Std Dev 13.1
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

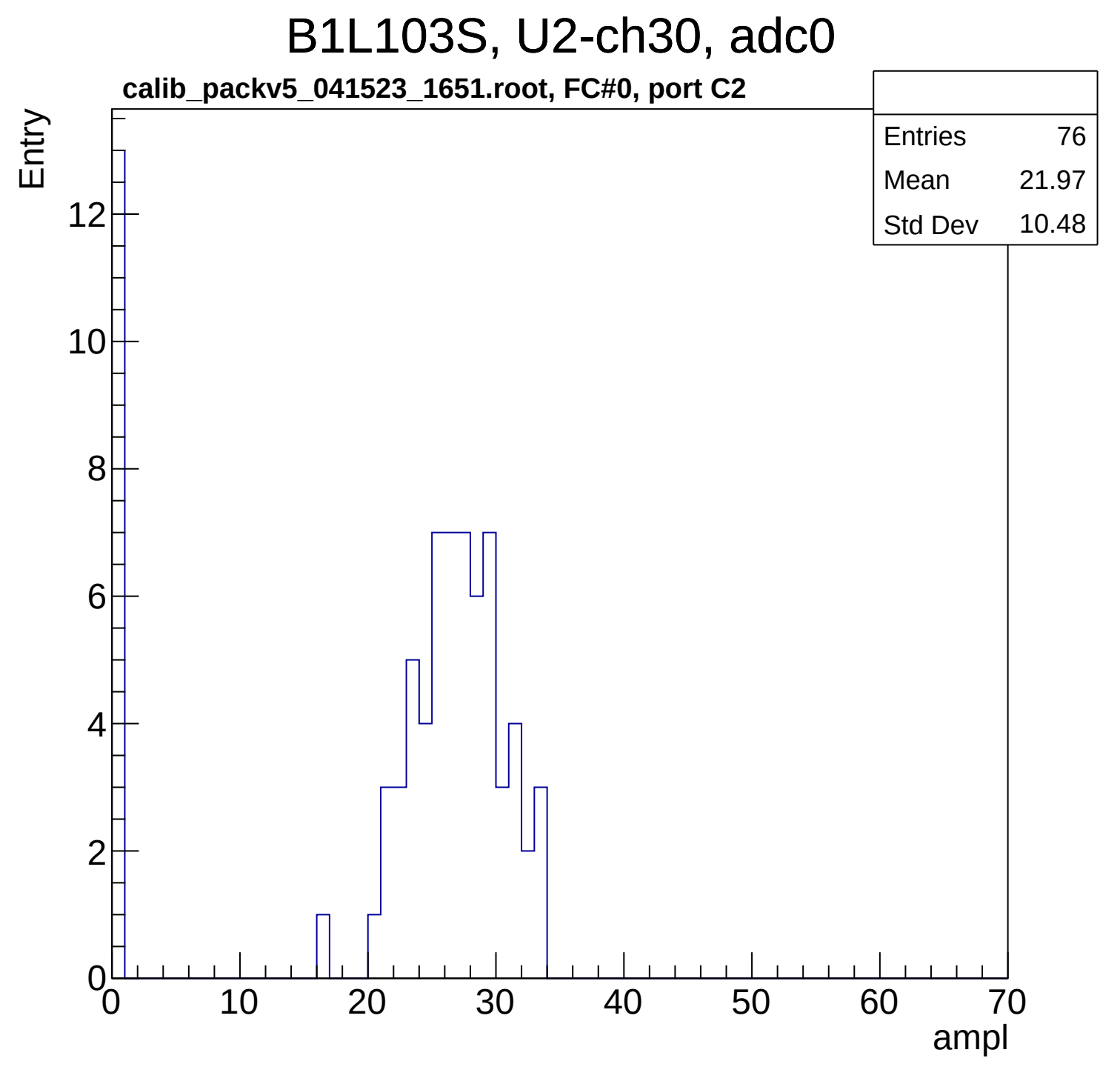

B1L103S, U2-ch29, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 47.42
Std Dev 3.226
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

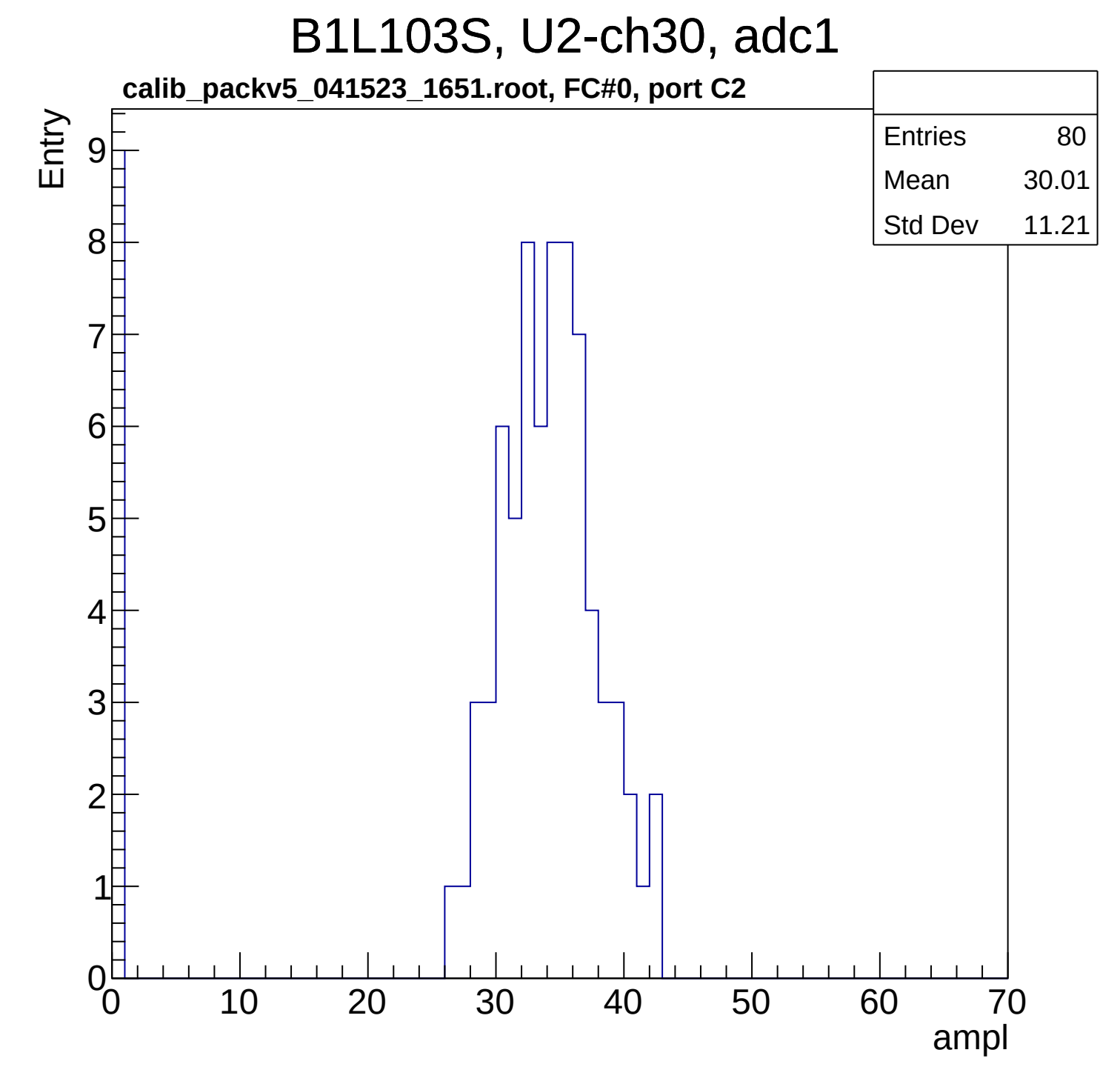

B1L103S, U2-ch29, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 53.3
Std Dev 3.129
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

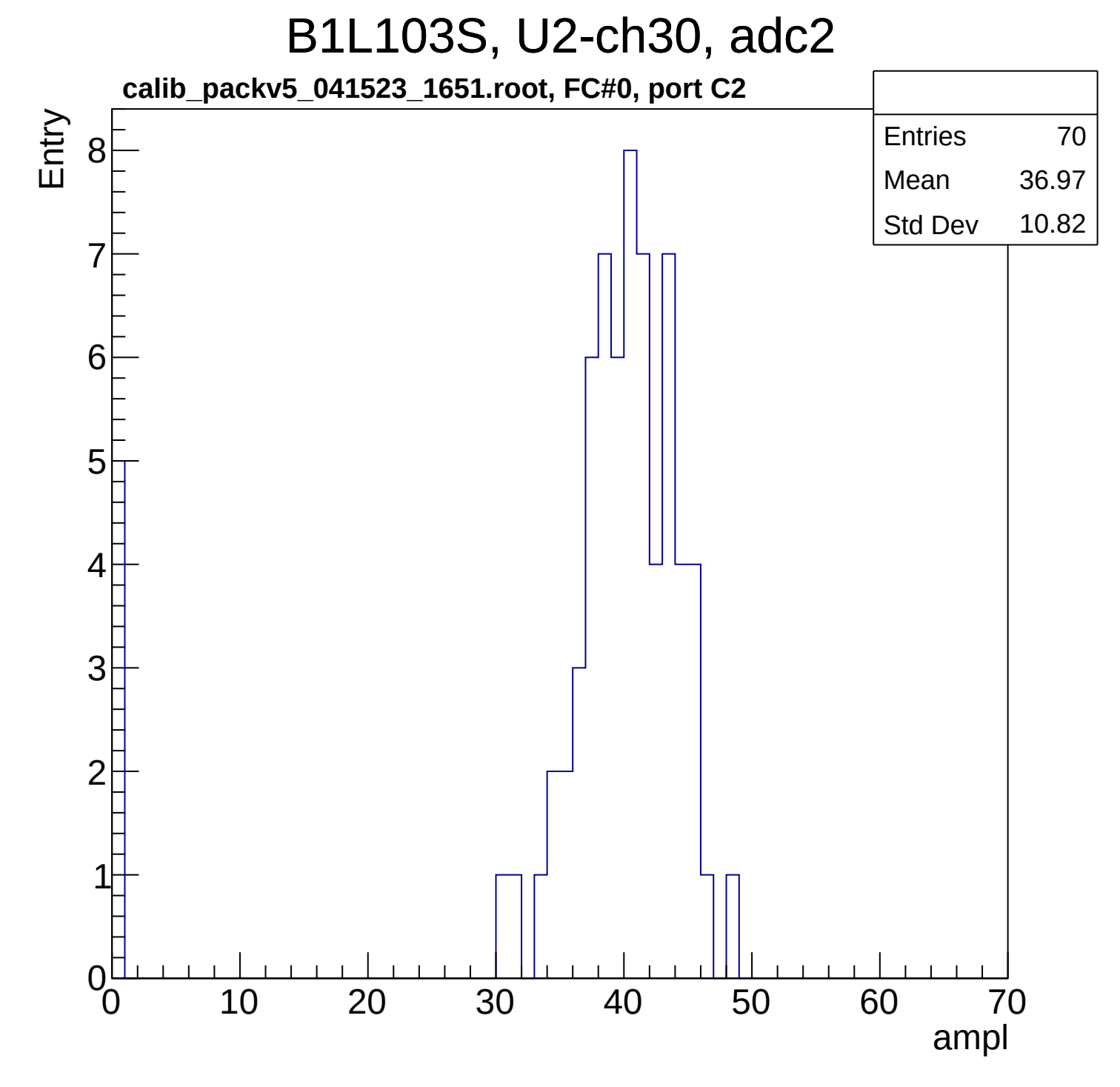

B1L103S, U2-ch29, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 57.85
Std Dev 8.08
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

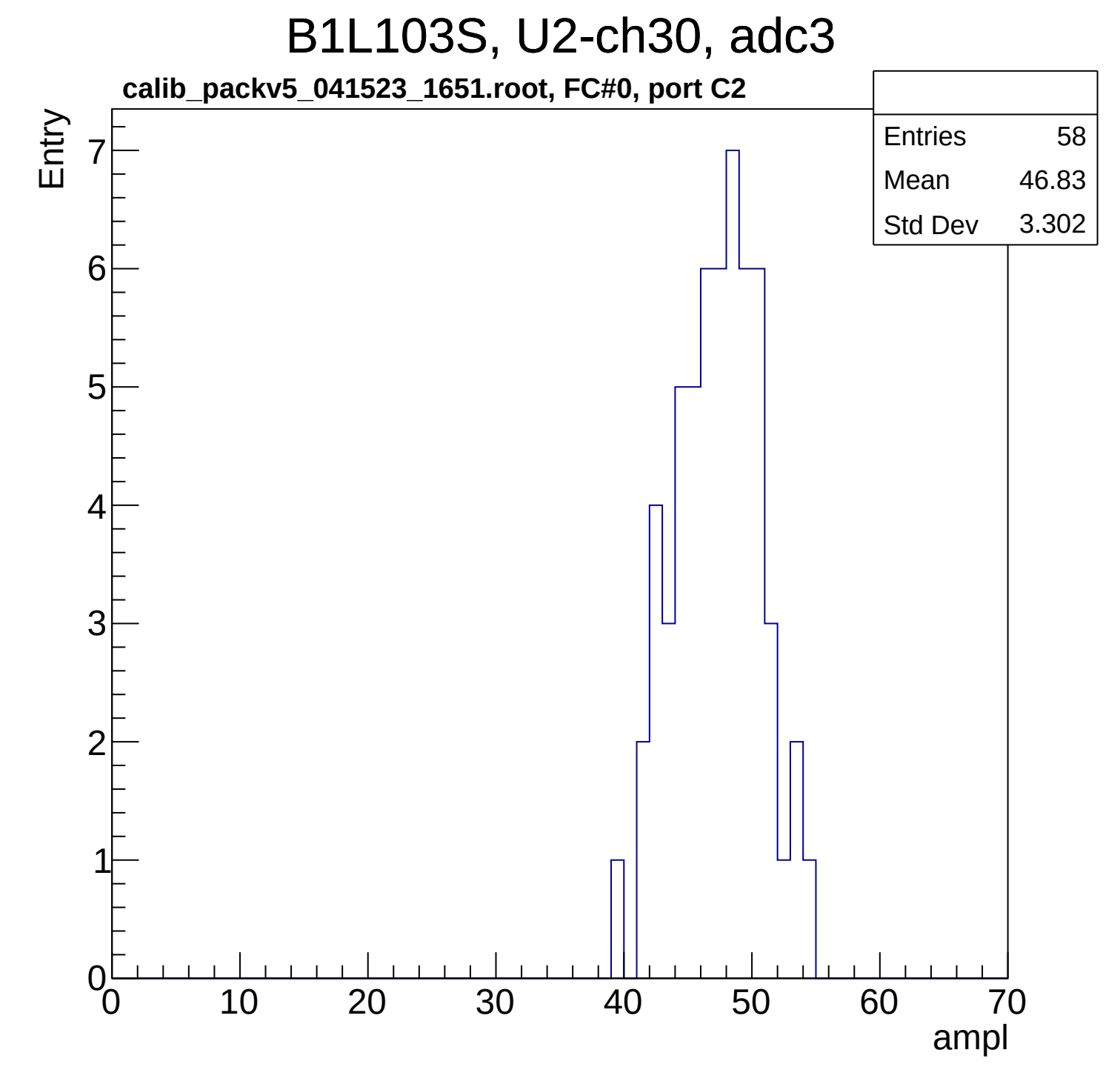

B1L103S, U2-ch29, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.46
Std Dev 1.216
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

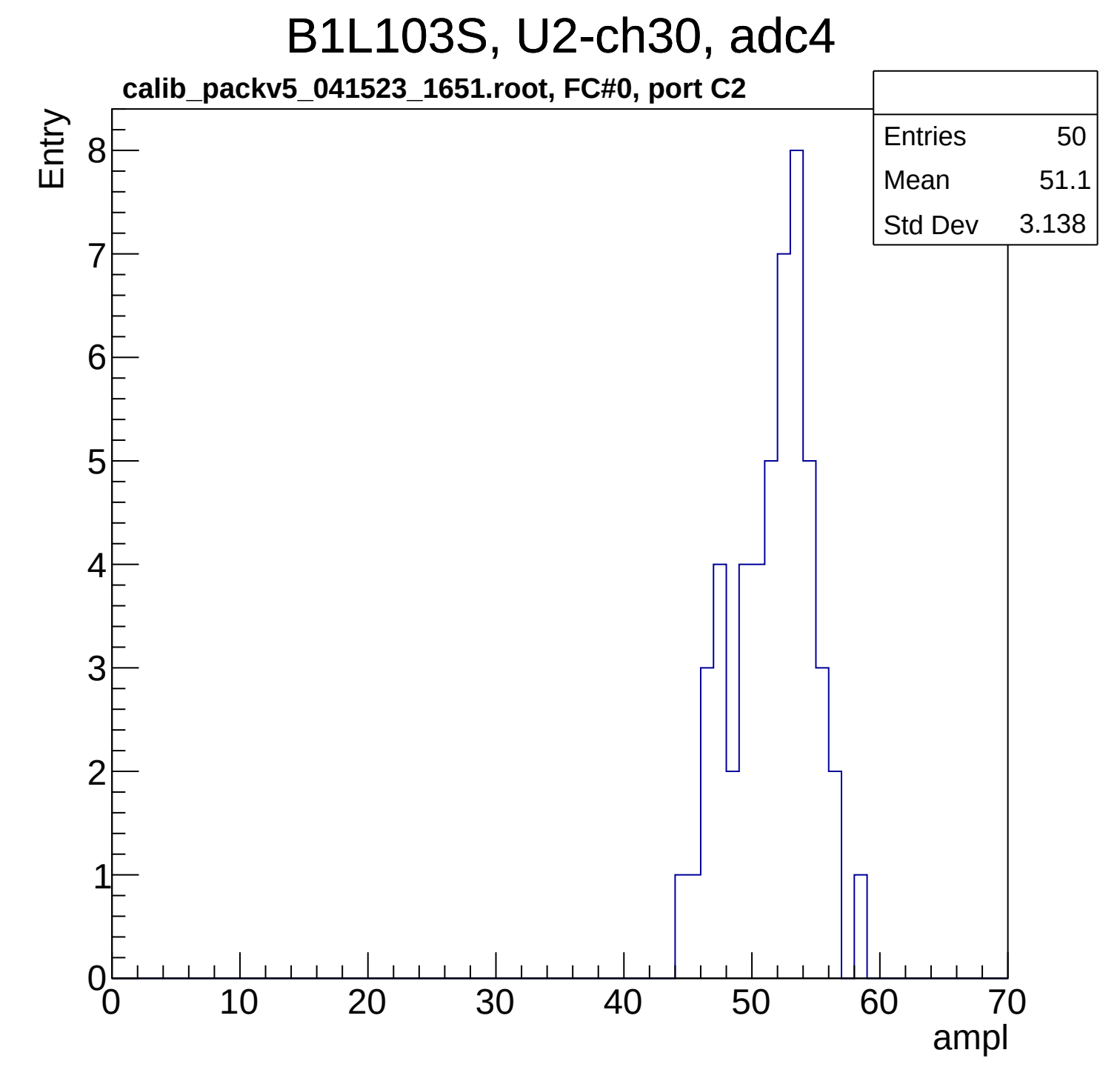

B1L103S, U2-ch29, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

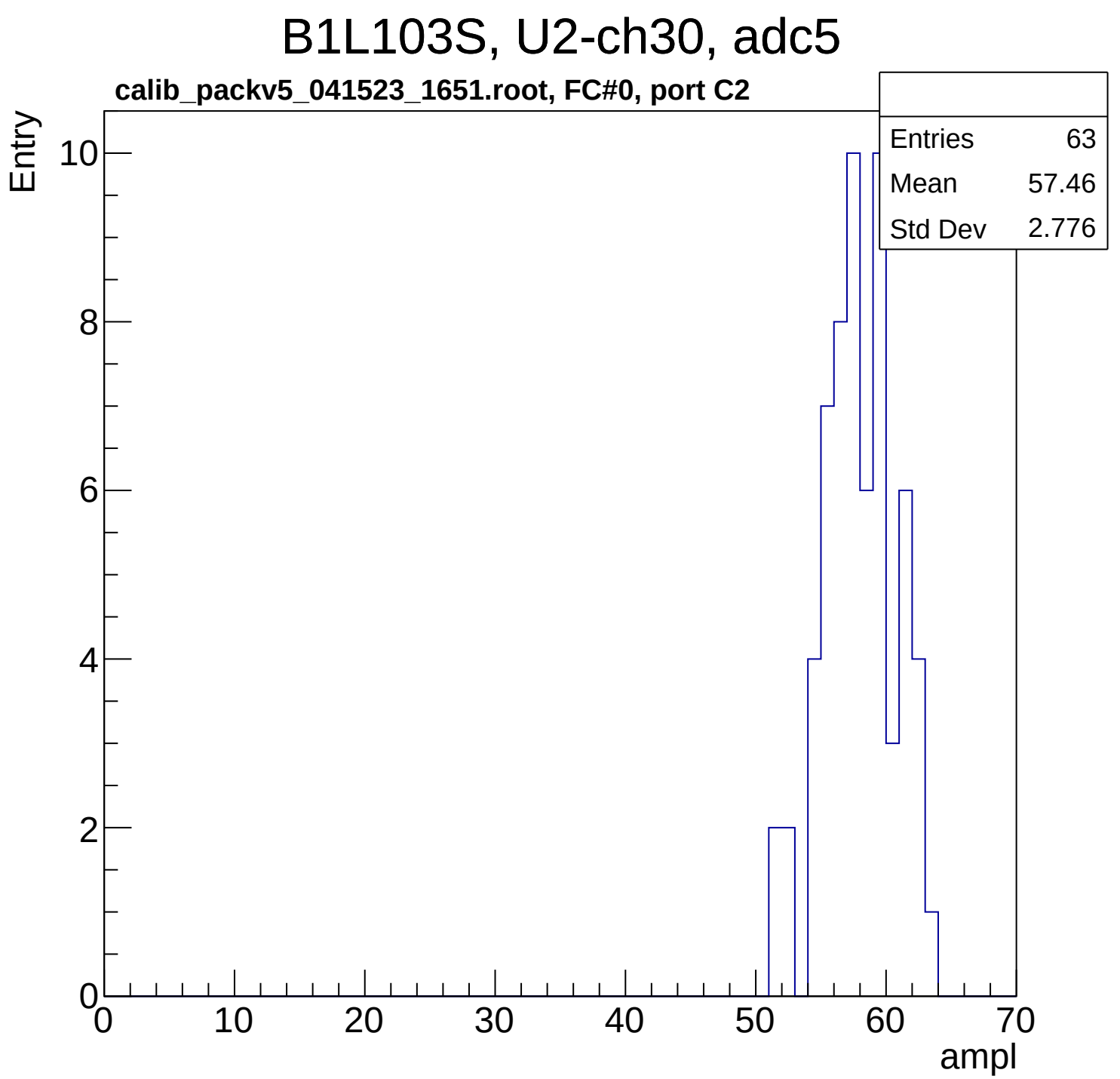

B1L103S, U2-ch30, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 21.97
Std Dev 10.48
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

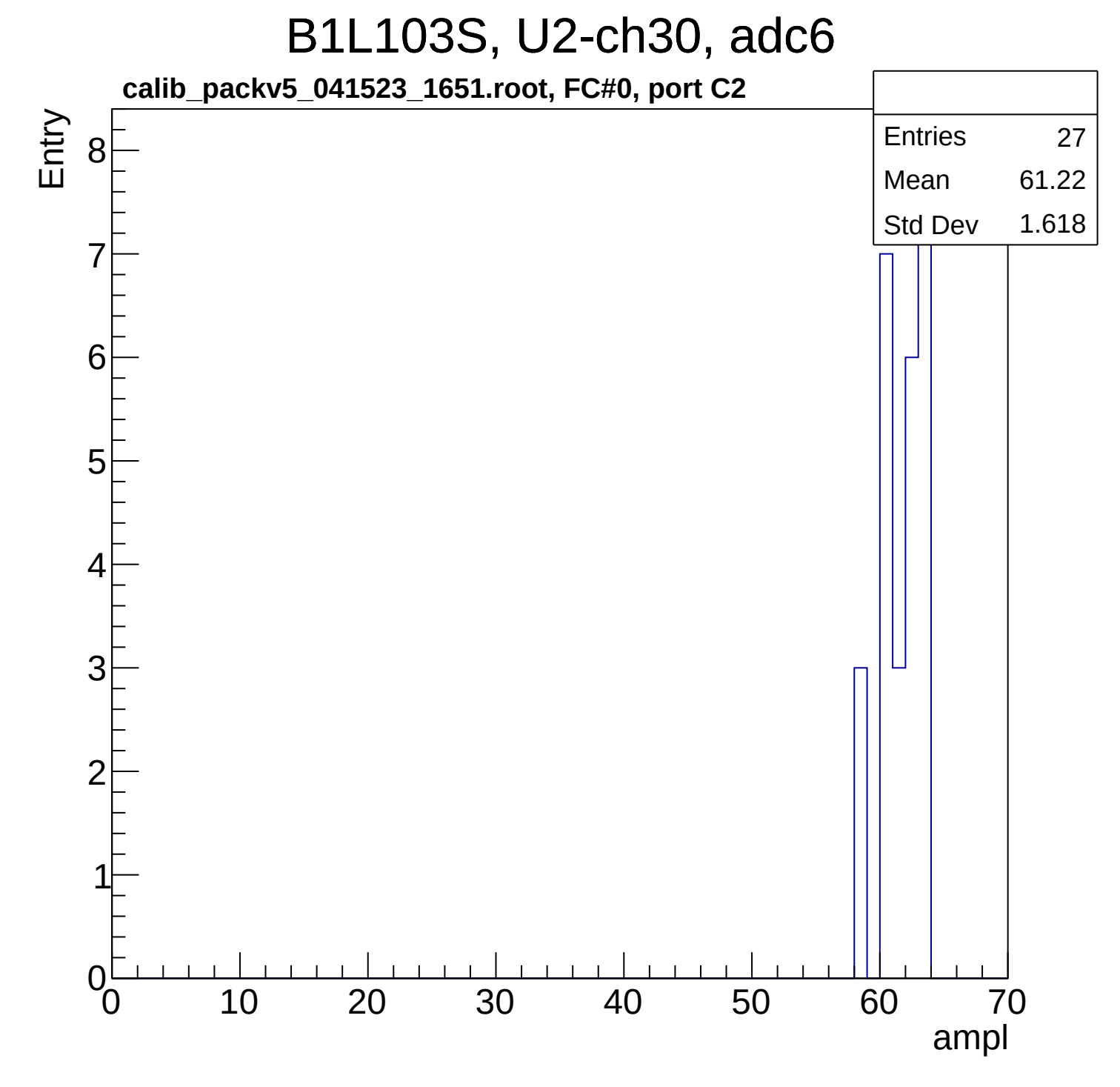

B1L103S, U2-ch30, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 30.01
Std Dev 11.21
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

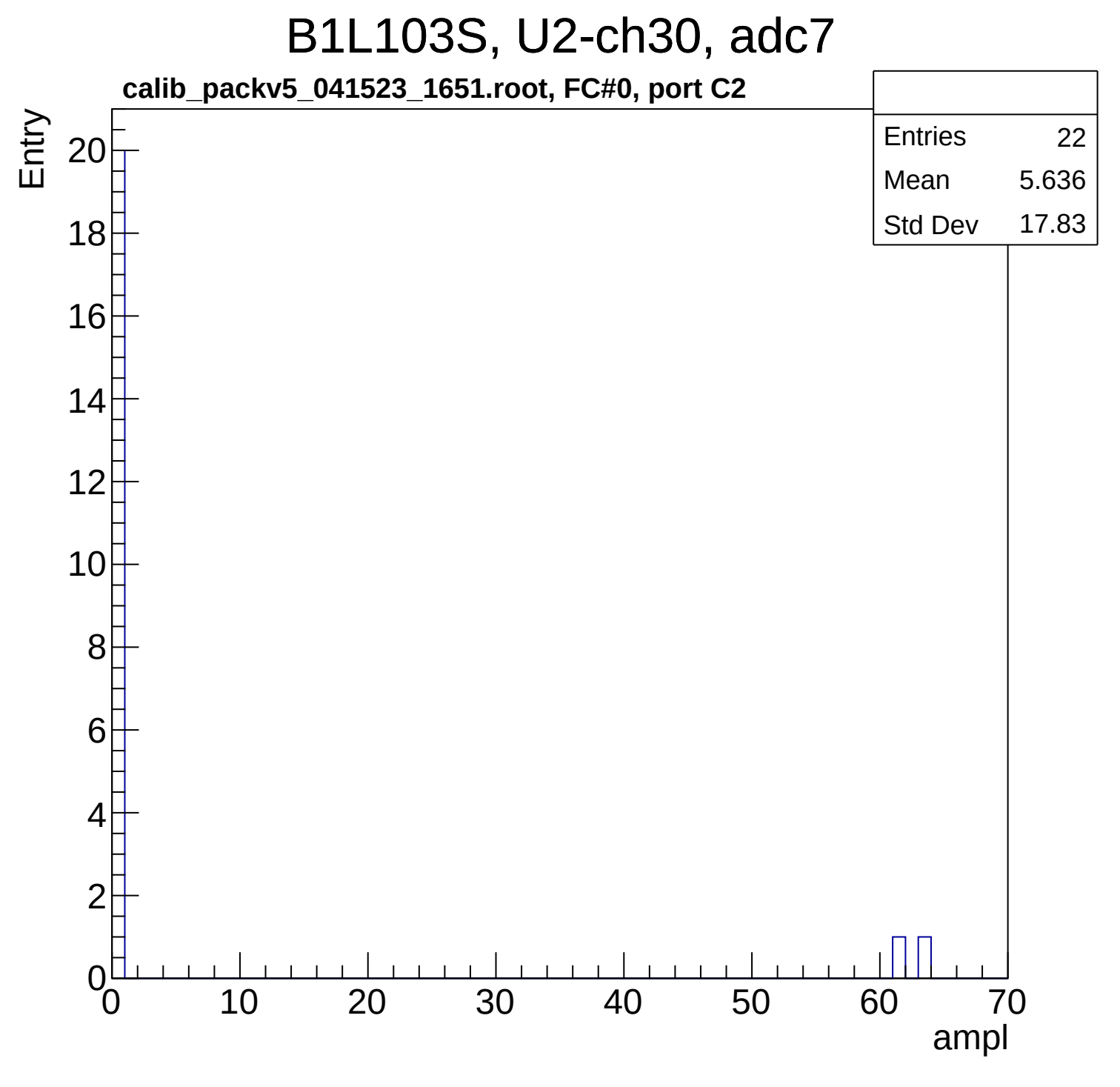

B1L103S, U2-ch30, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 36.97
Std Dev 10.82
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

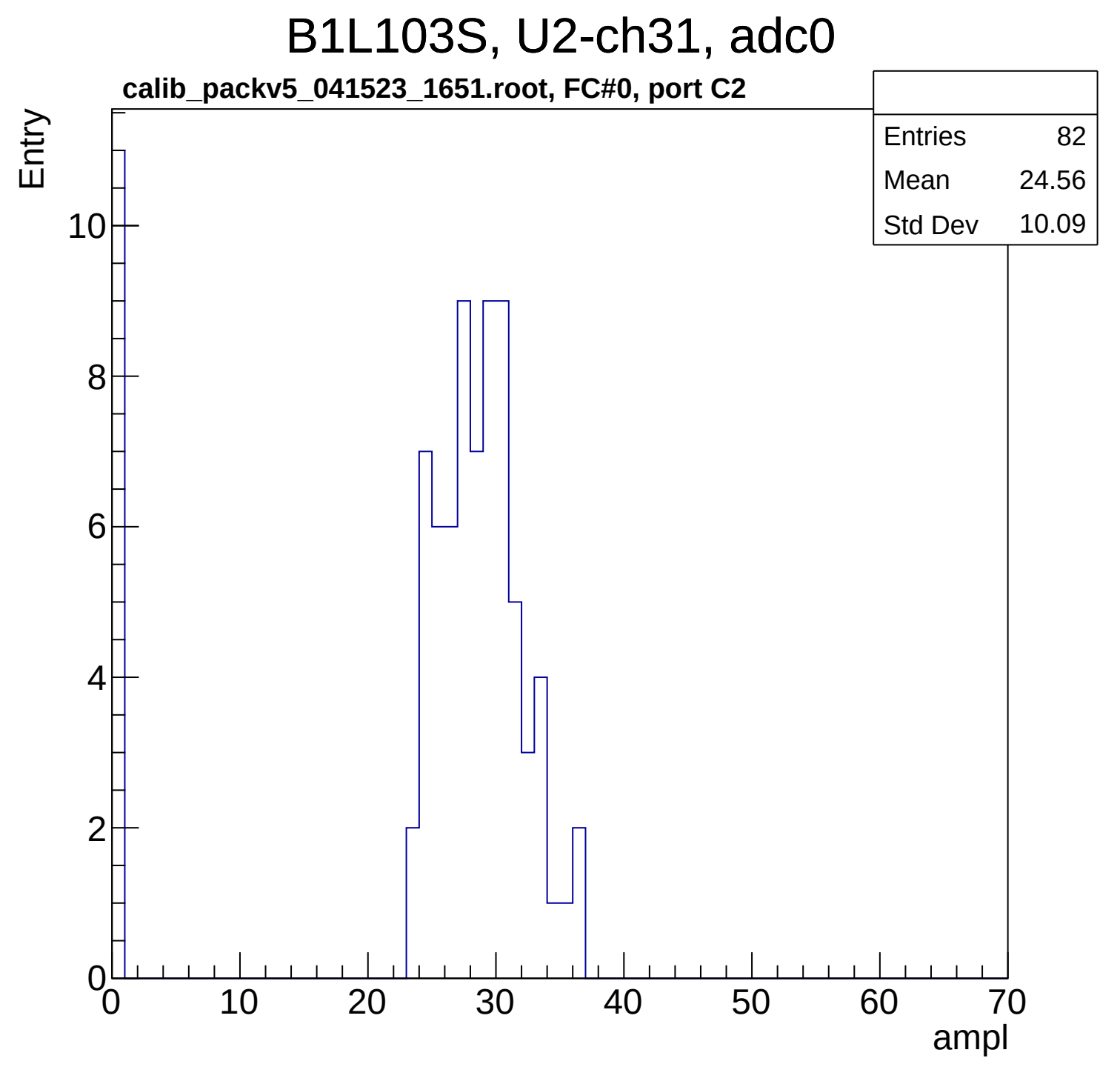

B1L103S, U2-ch30, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 46.83
Std Dev 3.302
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

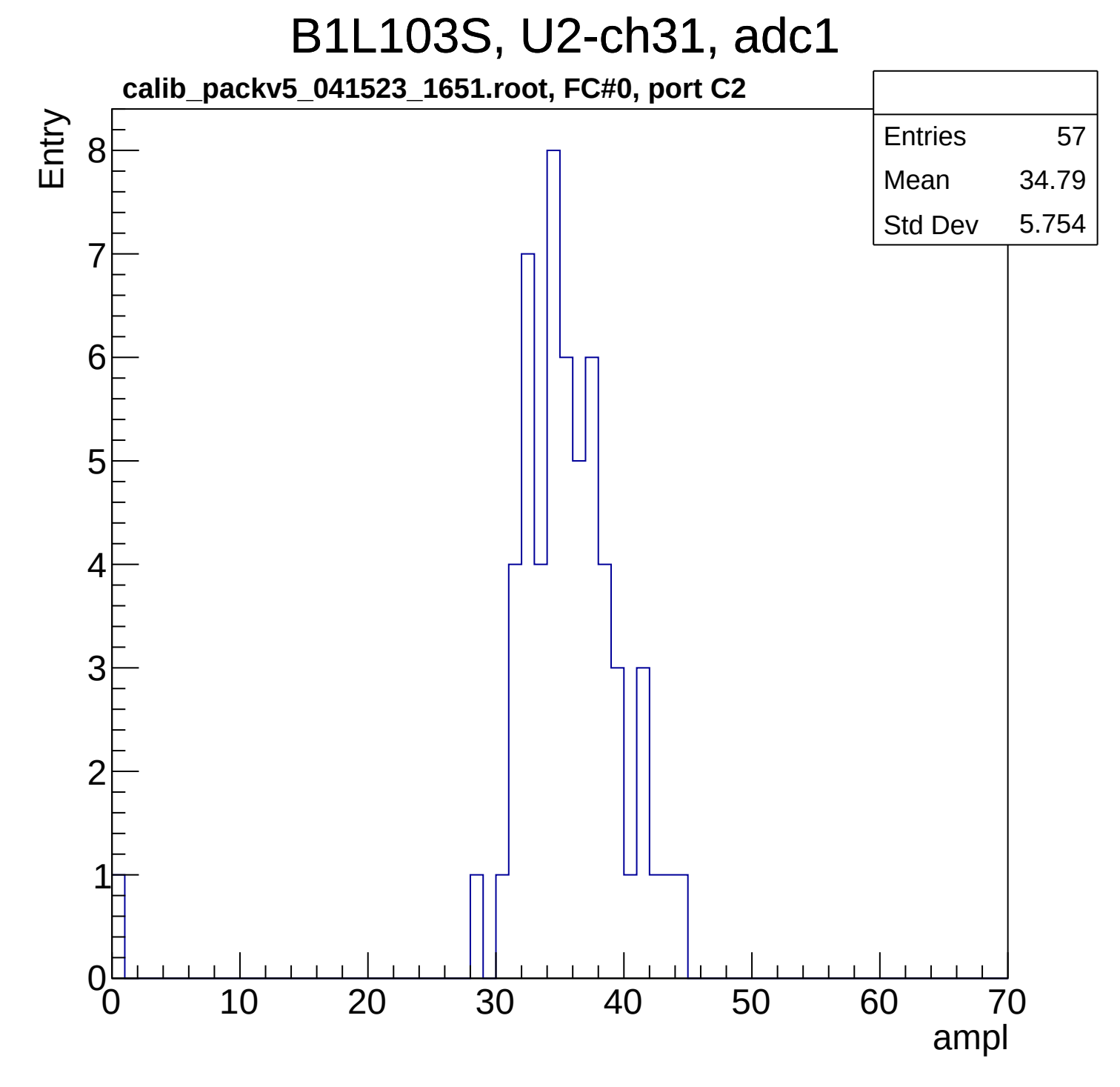

B1L103S, U2-ch30, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 51.1
Std Dev 3.138
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

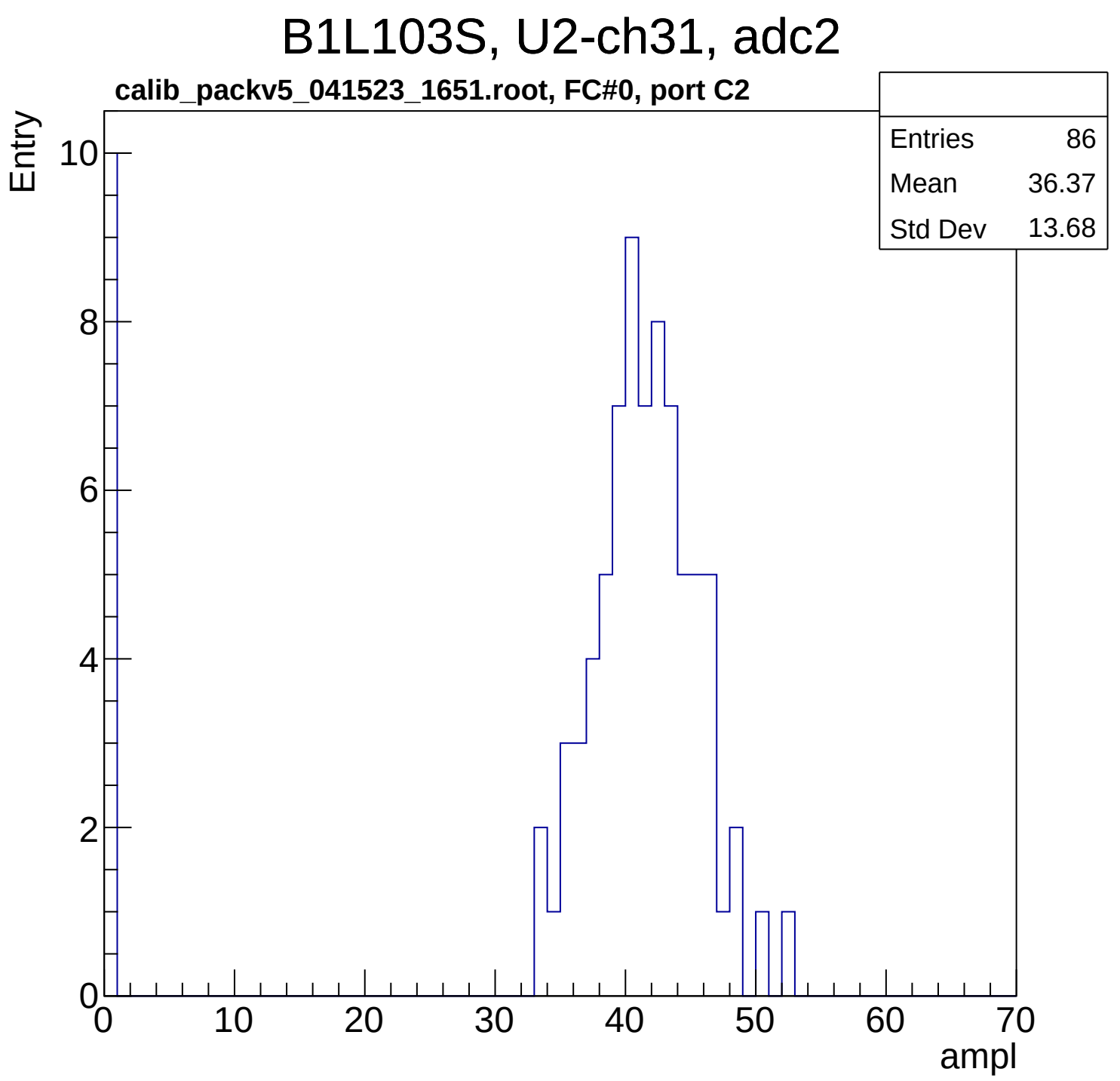

B1L103S, U2-ch30, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 57.46
Std Dev 2.776
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

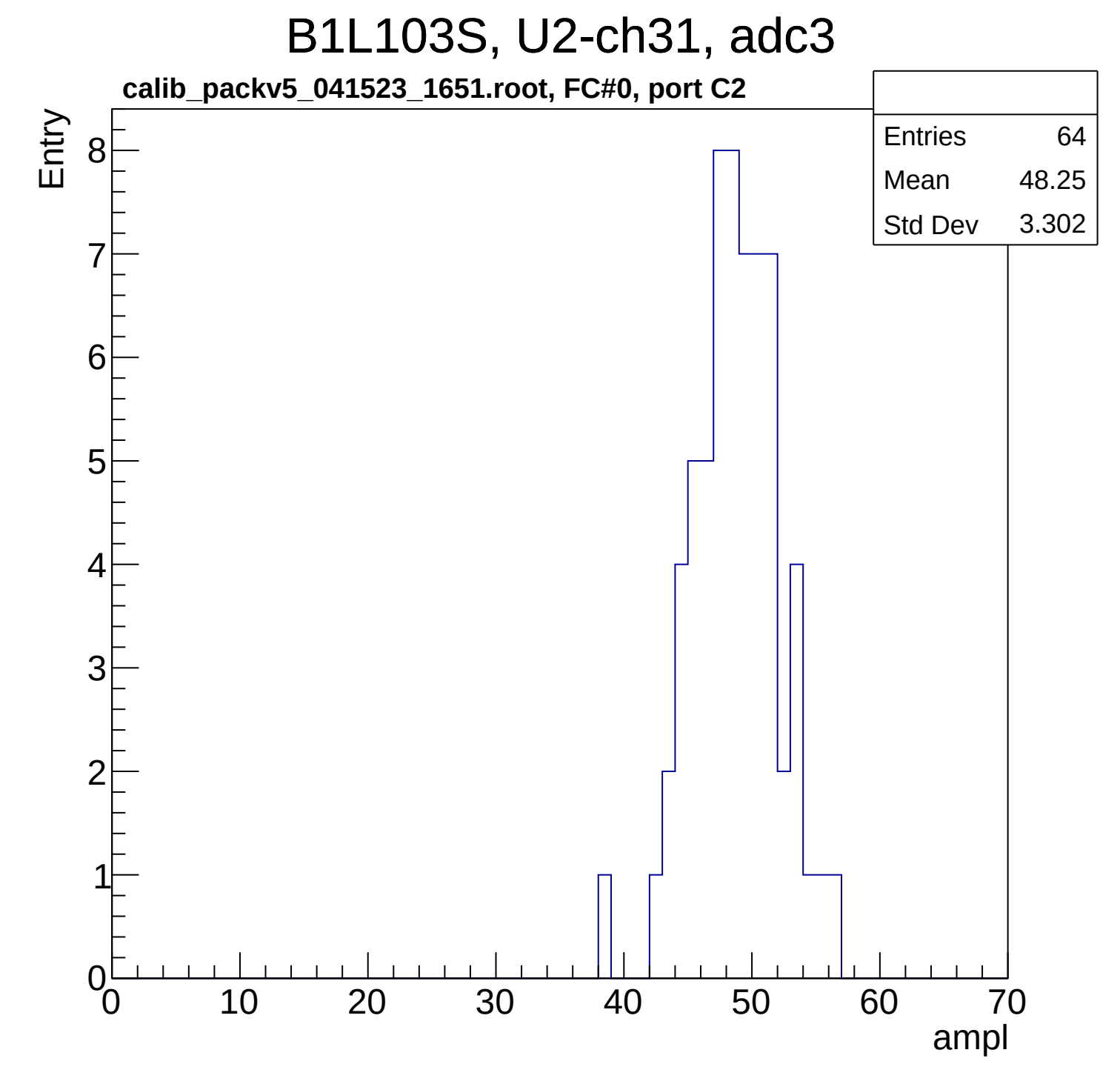

B1L103S, U2-ch30, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 61.22
Std Dev 1.618
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

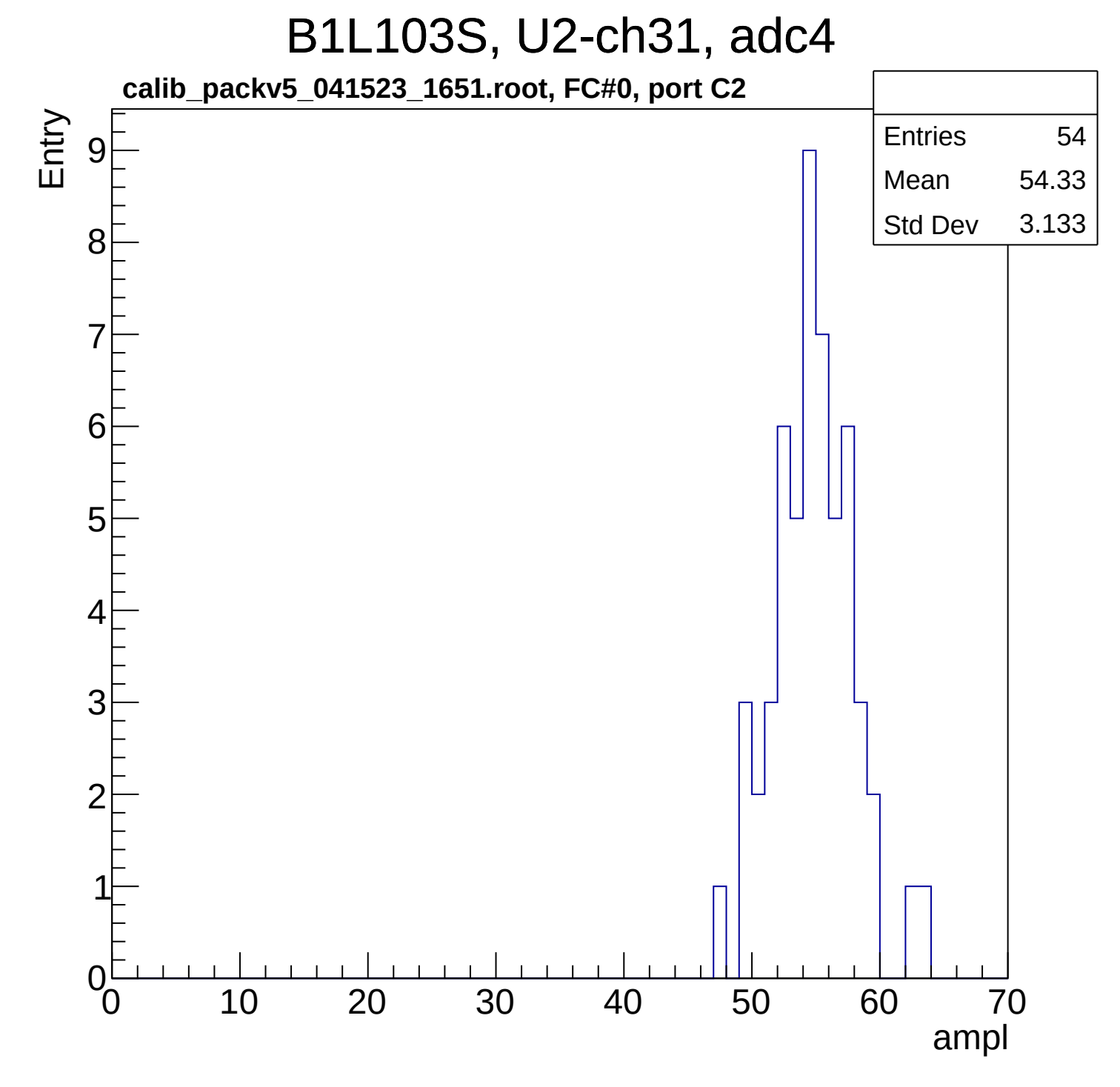

B1L103S, U2-ch30, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 5.636
Std Dev 17.83
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl

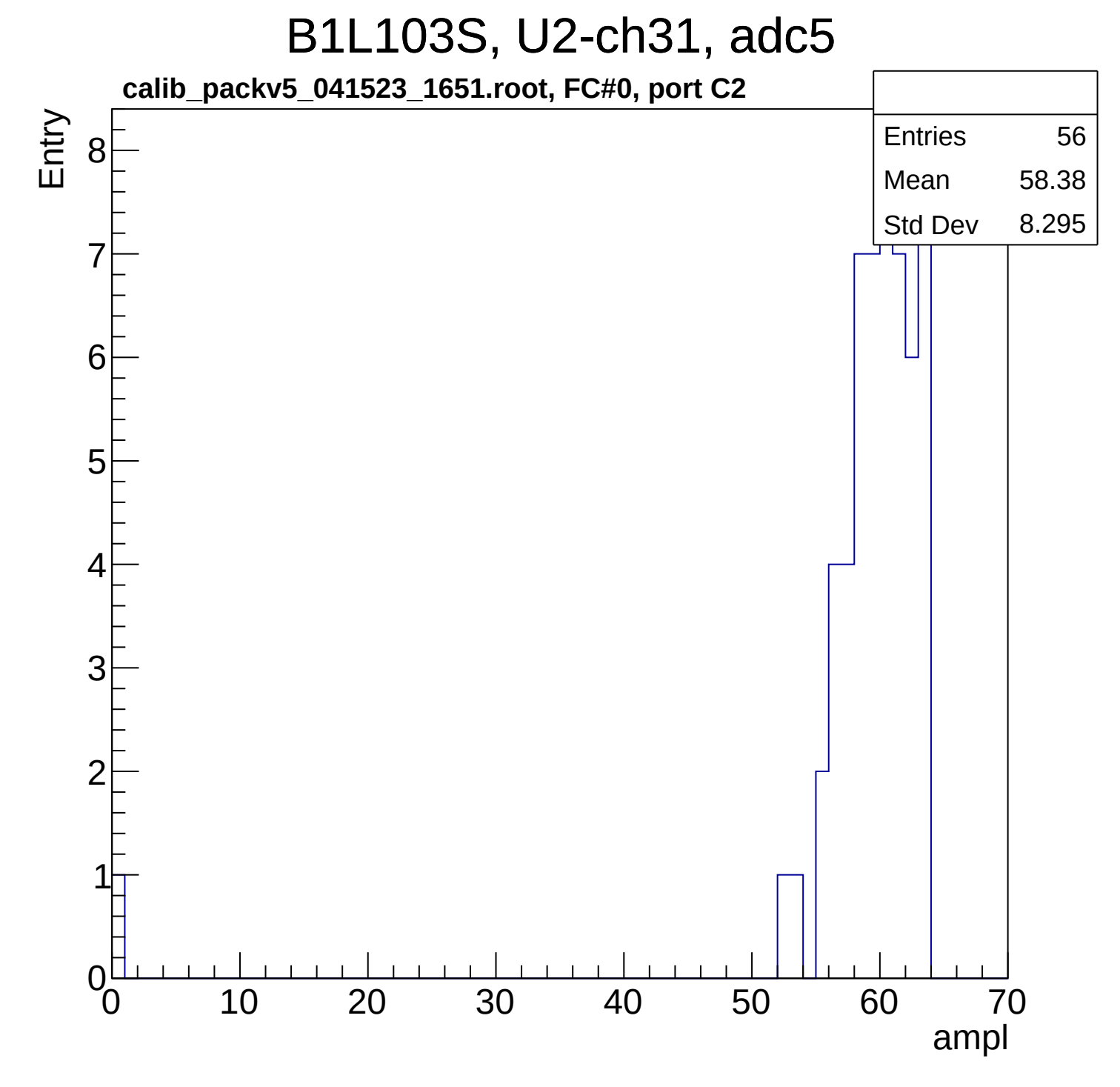

B1L103S, U2-ch31, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 24.56
Std Dev 10.09
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

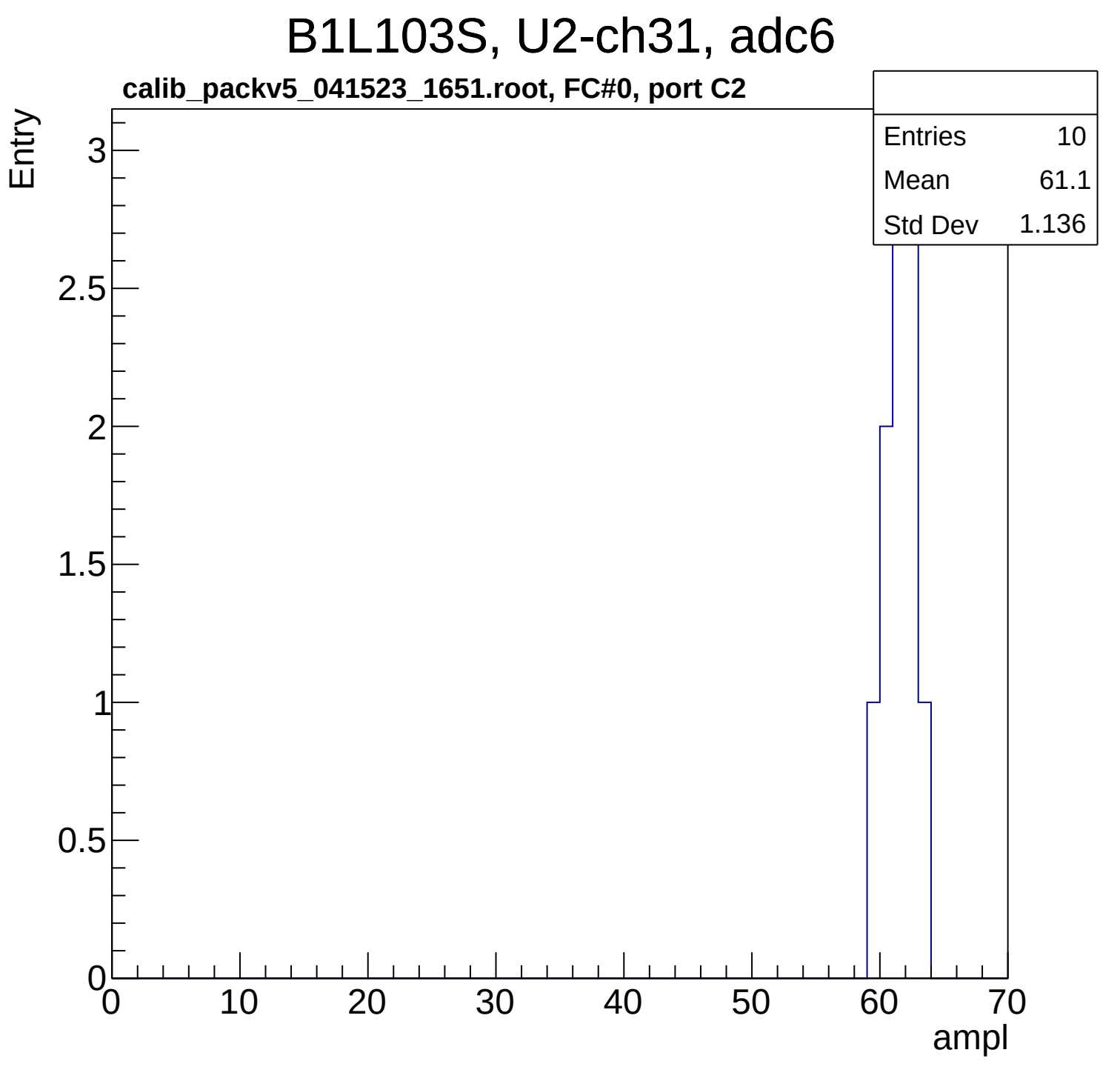

B1L103S, U2-ch31, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 34.79
Std Dev 5.754
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

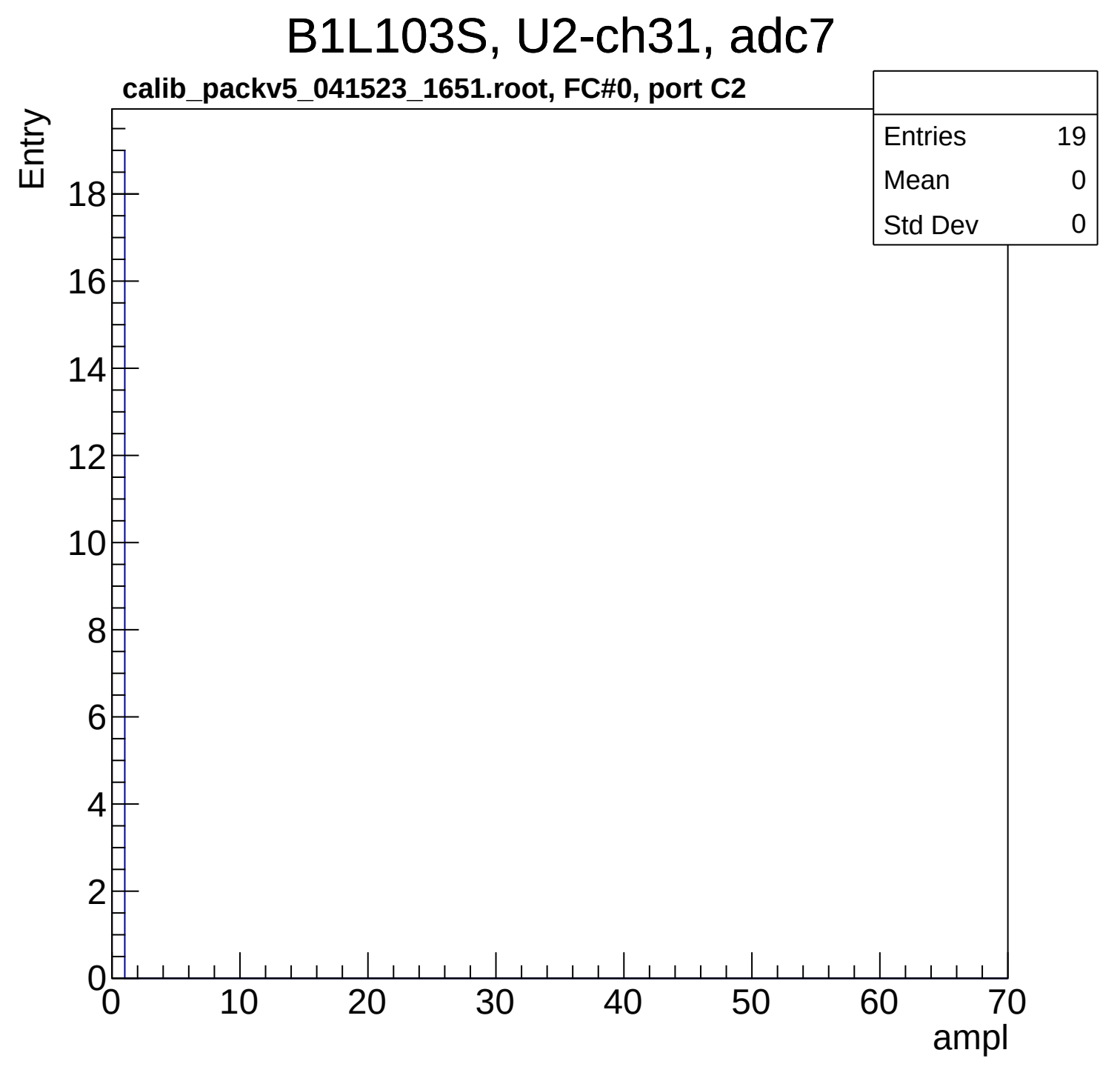

B1L103S, U2-ch31, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 36.37
Std Dev 13.68
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

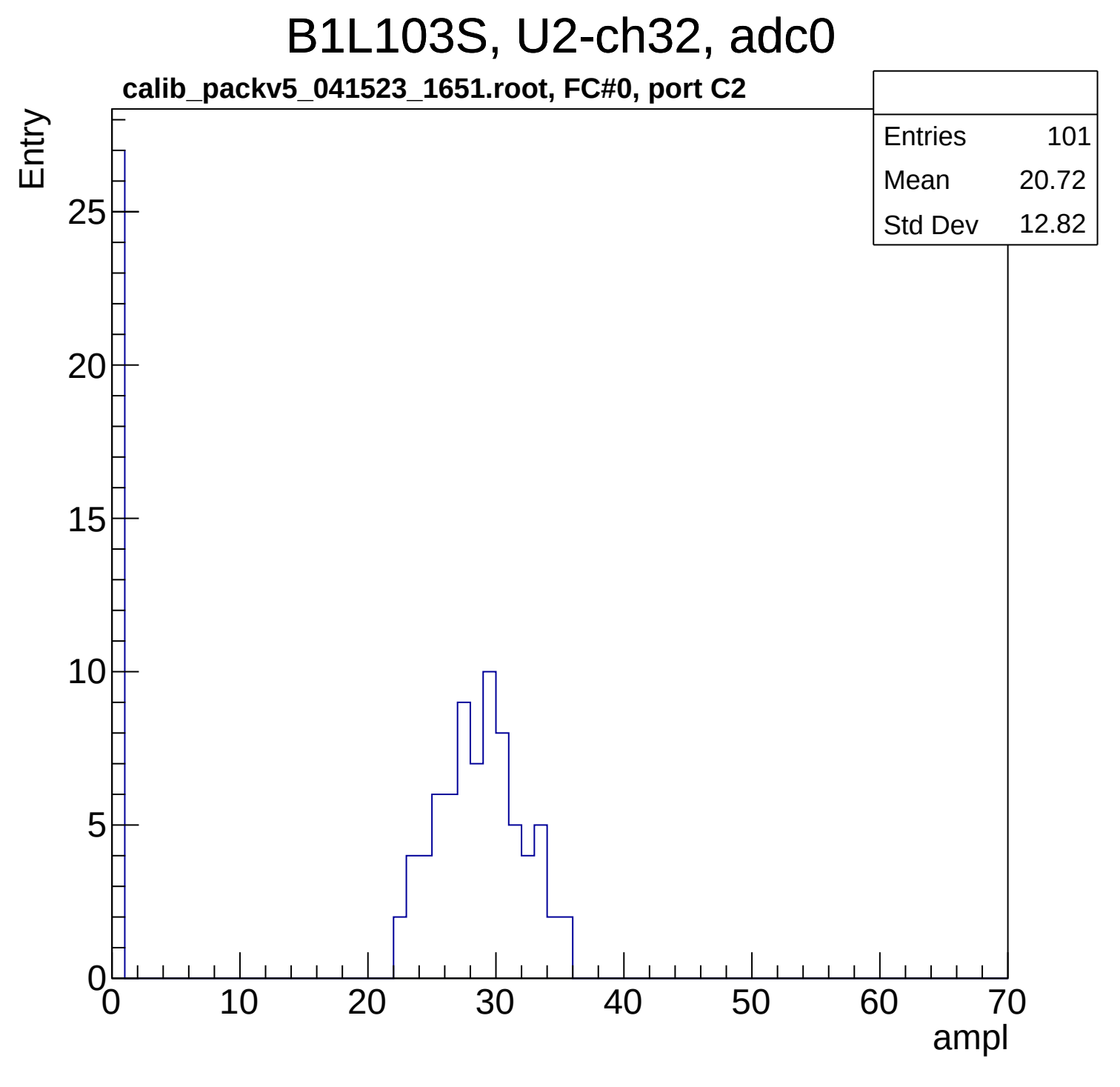

B1L103S, U2-ch31, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 48.25
Std Dev 3.302
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

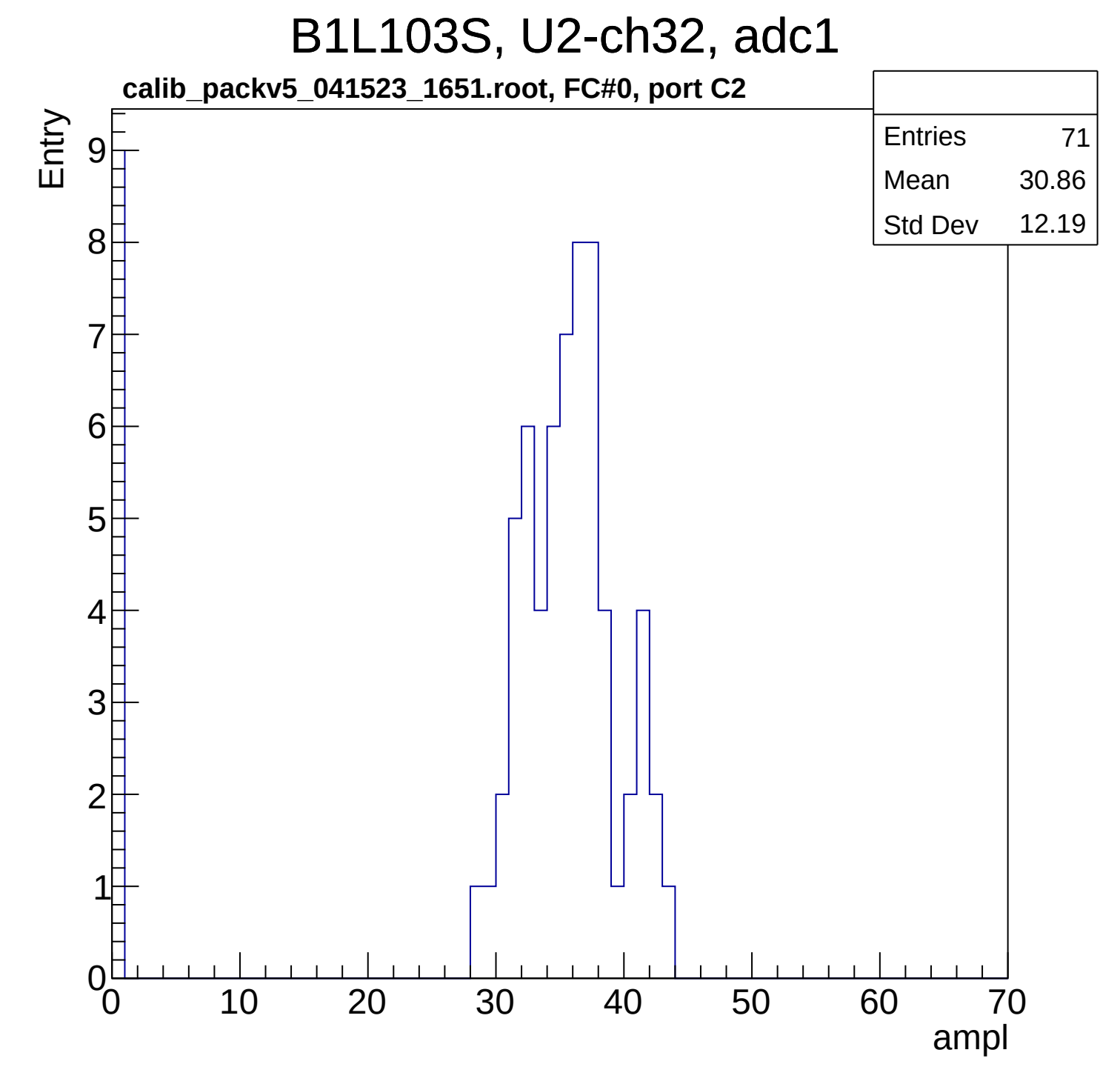

B1L103S, U2-ch31, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 54.33
Std Dev 3.133
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

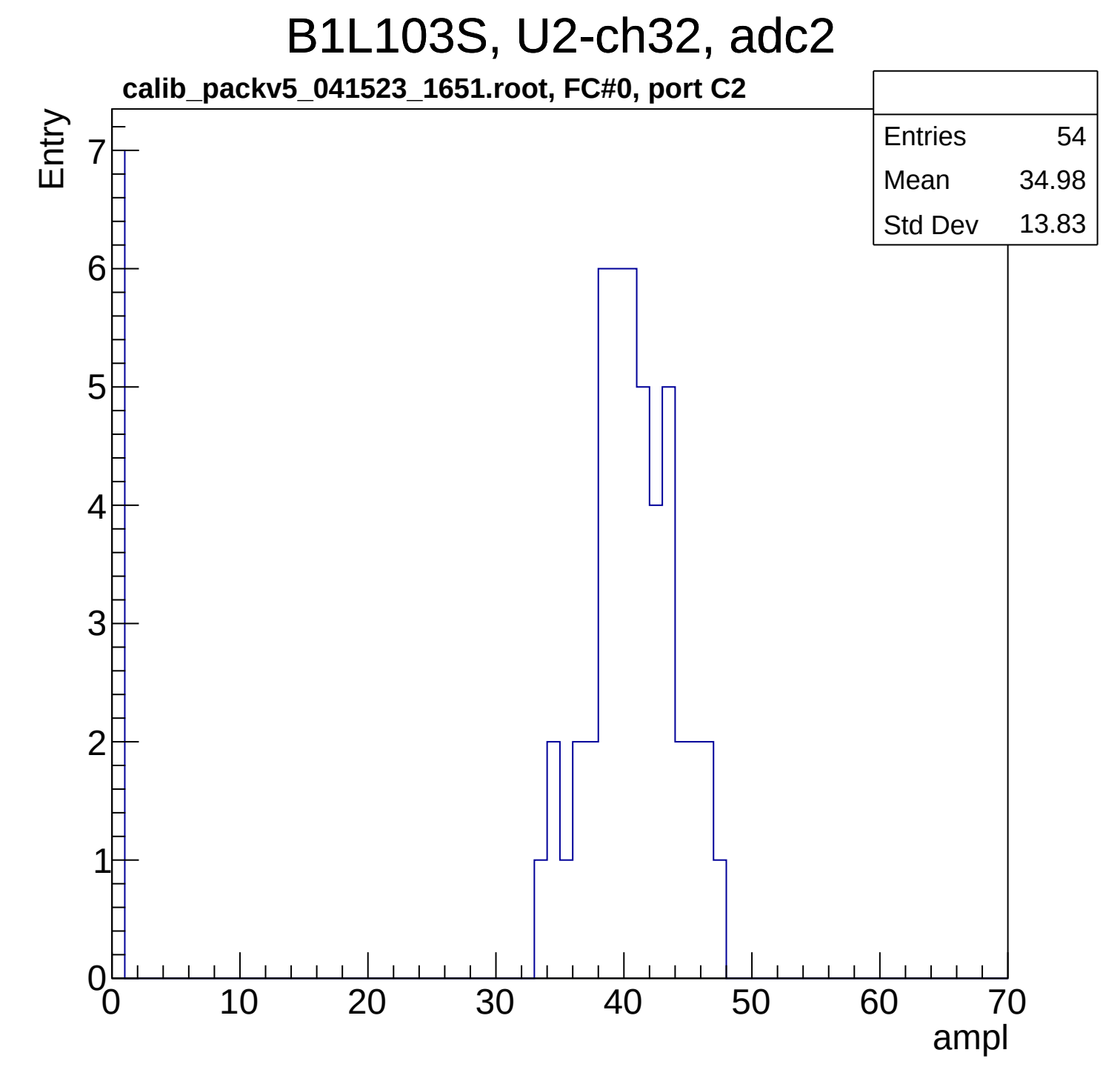

B1L103S, U2-ch31, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.38
Std Dev 8.295
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

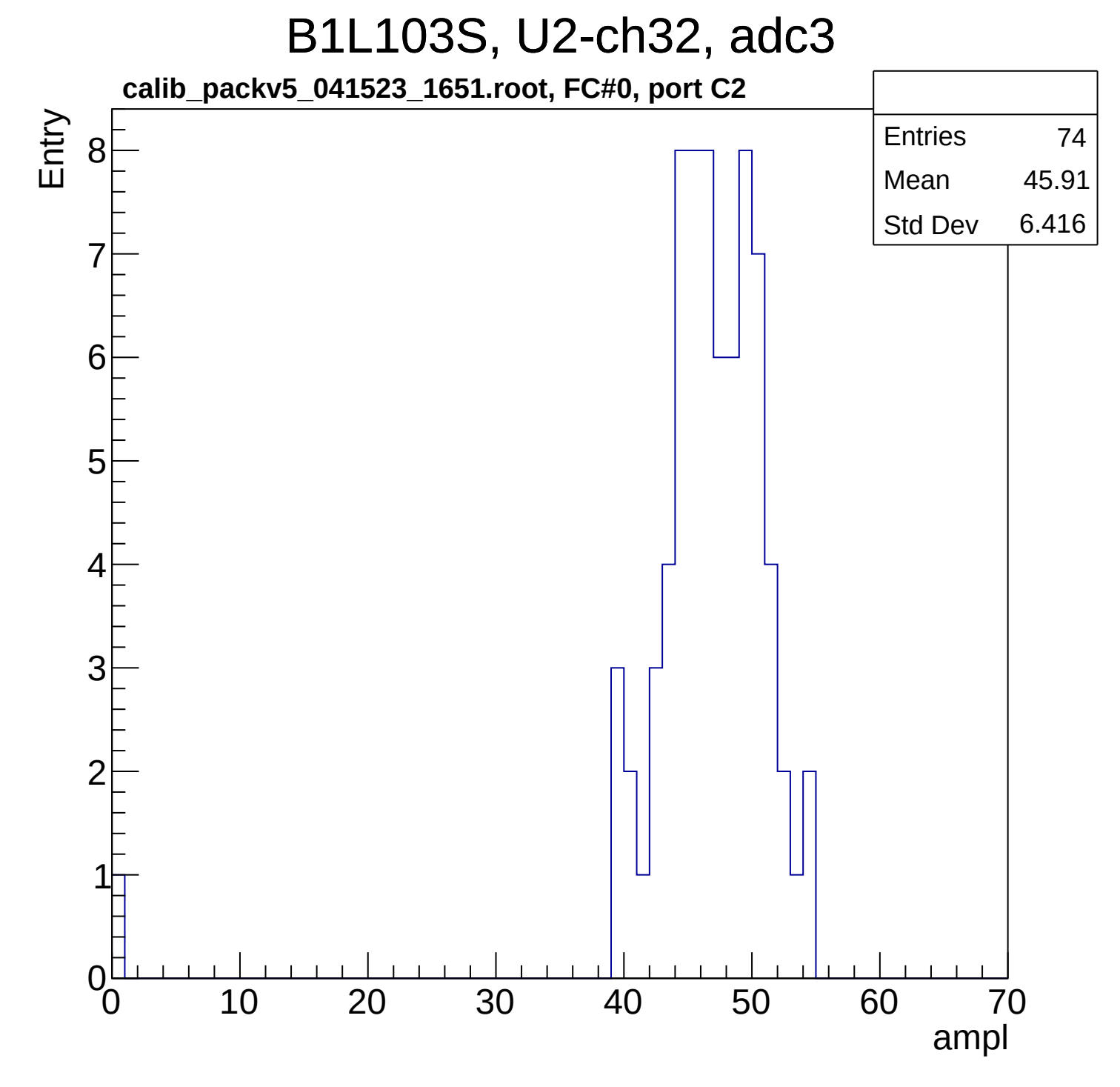

B1L103S, U2-ch31, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.1
Std Dev 1.136
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

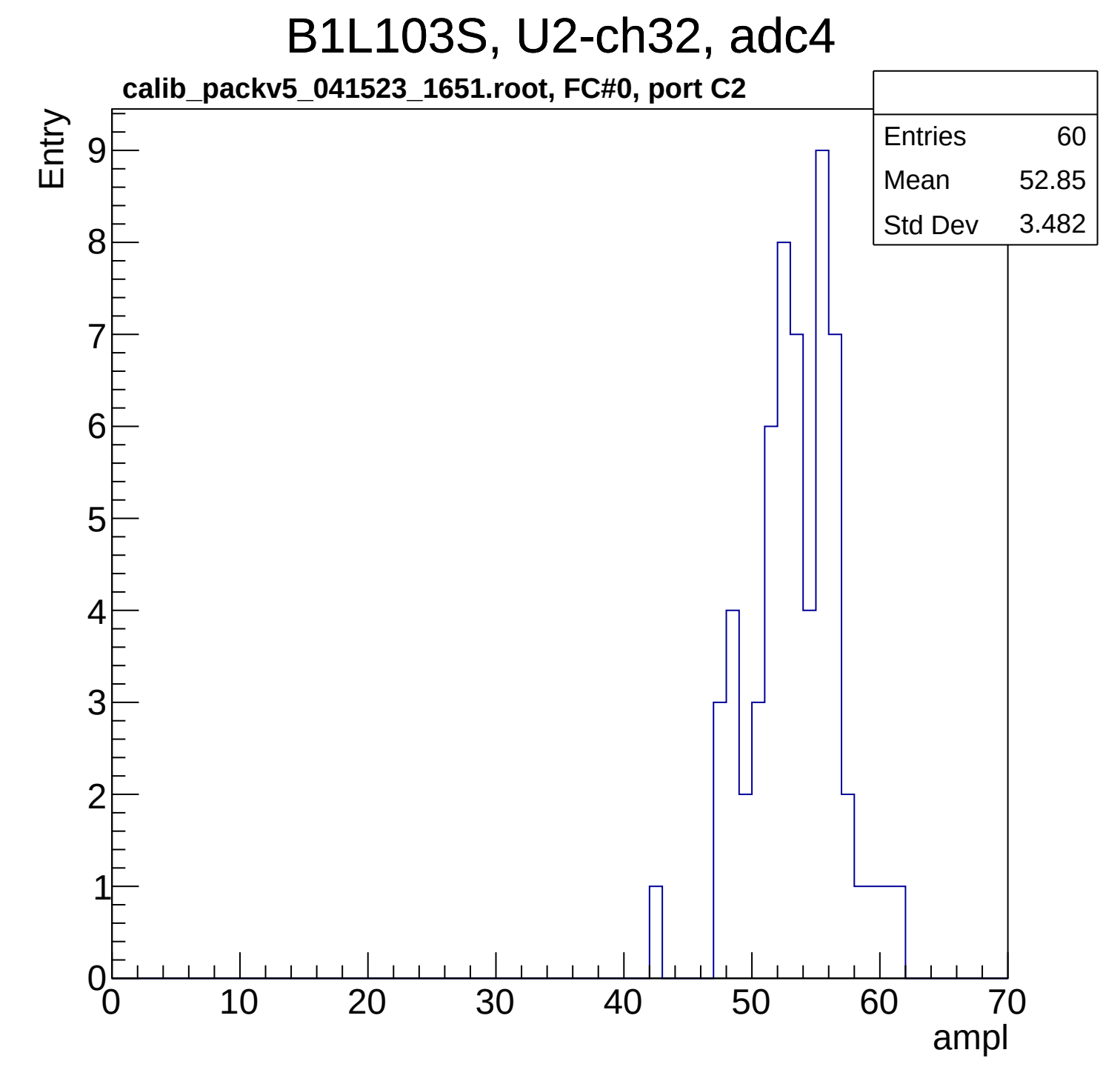

B1L103S, U2-ch31, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

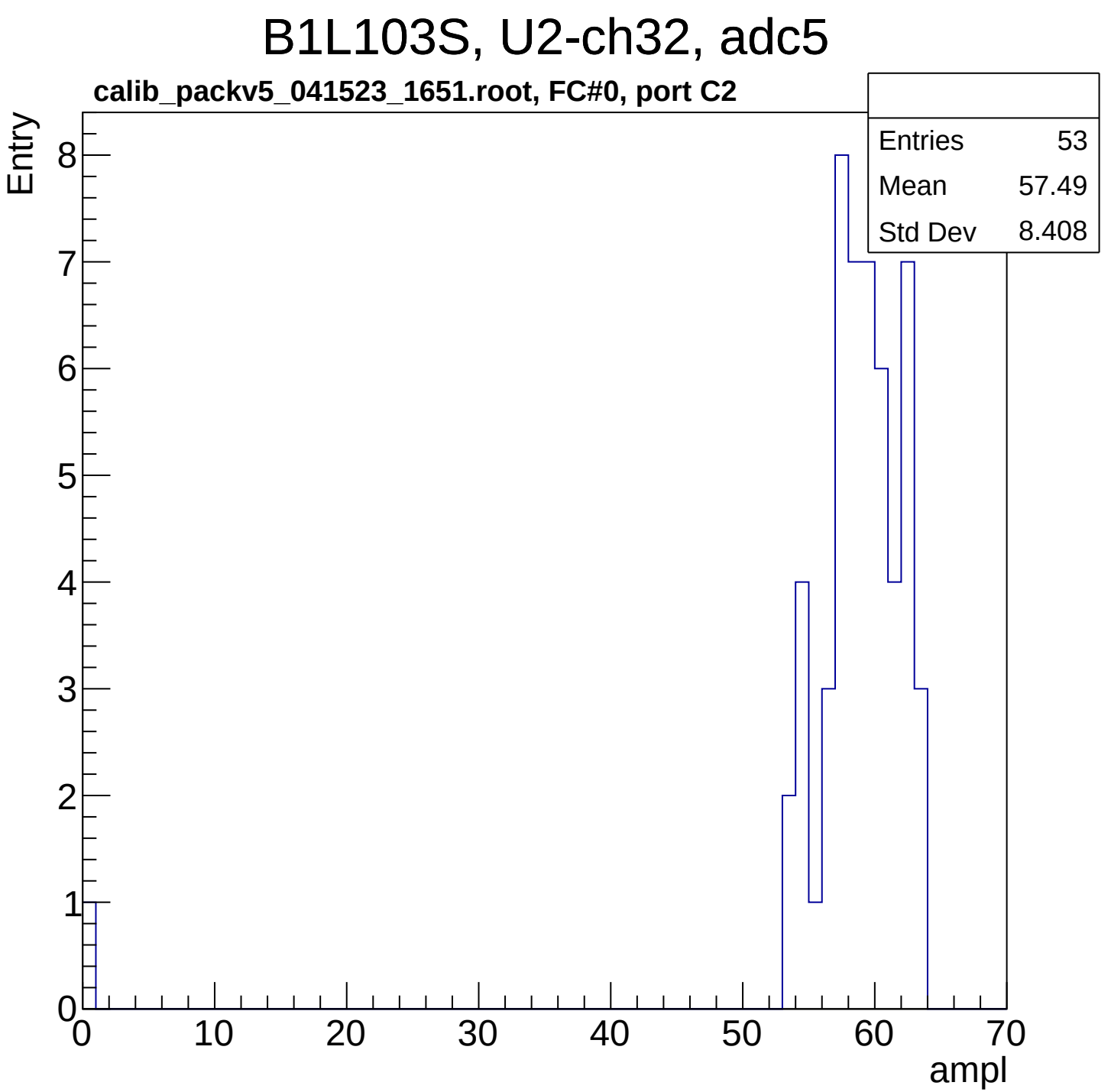

B1L103S, U2-ch32, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 20.72
Std Dev 12.82
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl

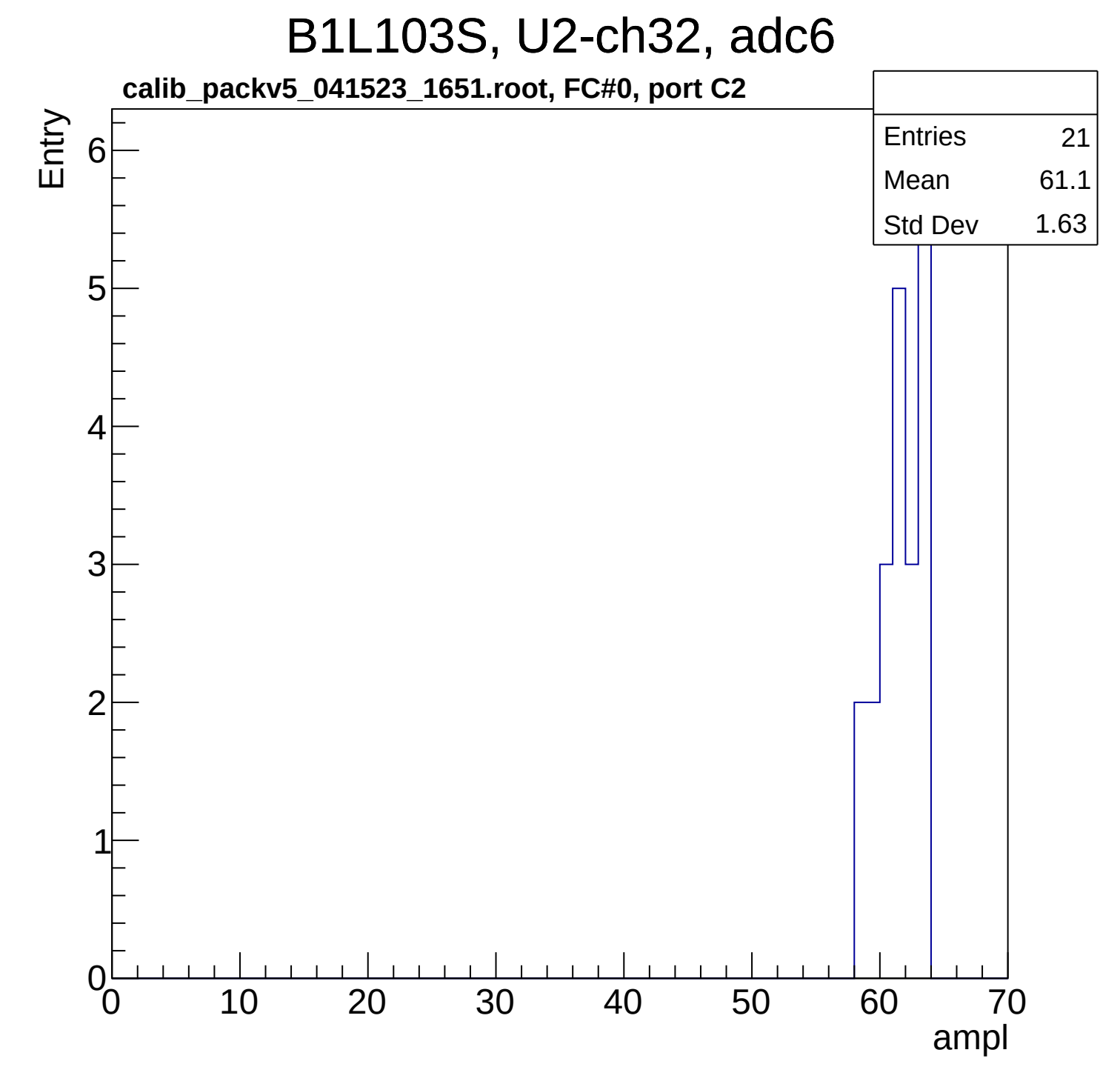

B1L103S, U2-ch32, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 30.86
Std Dev 12.19
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

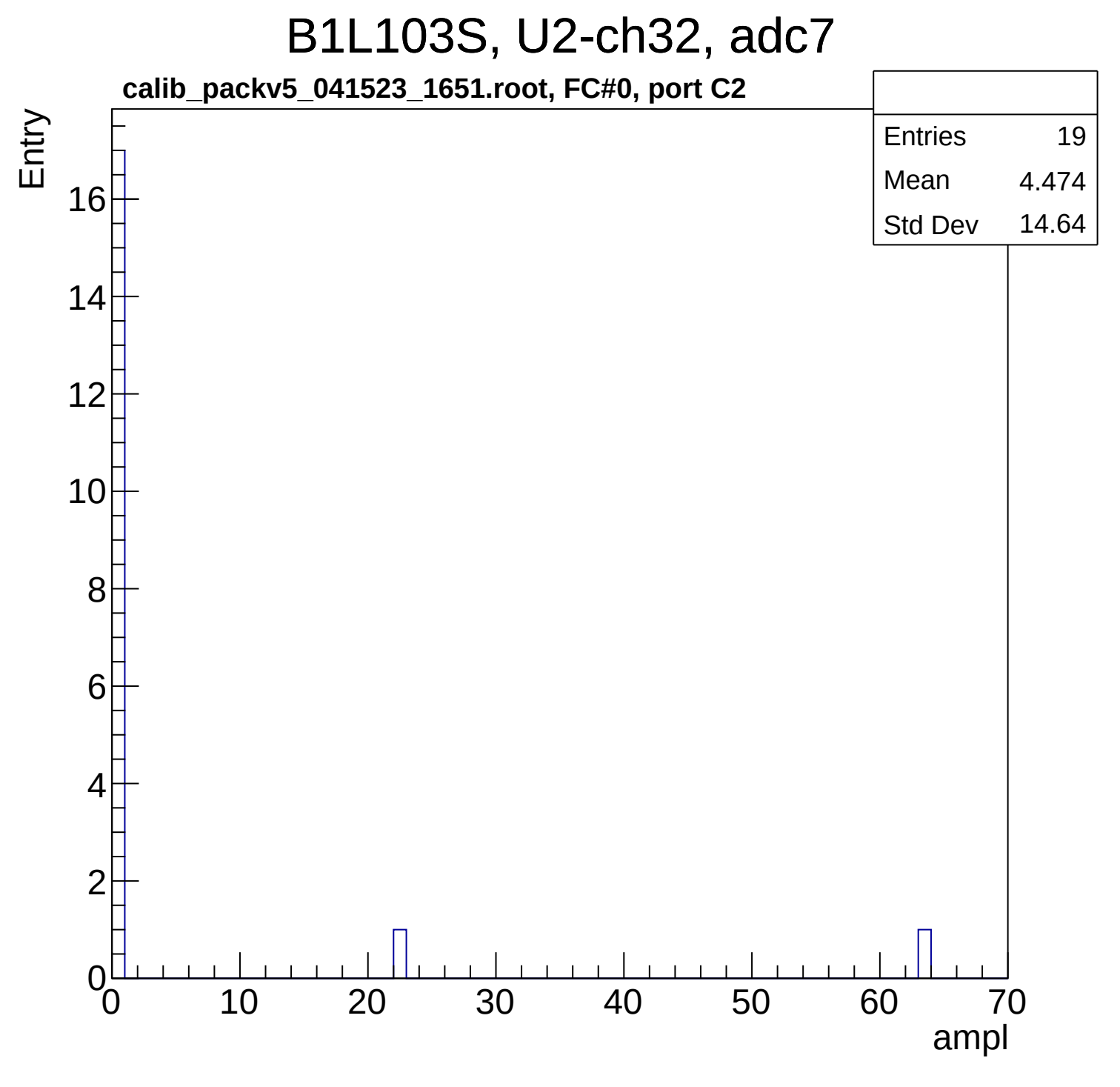

B1L103S, U2-ch32, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 34.98
Std Dev 13.83
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

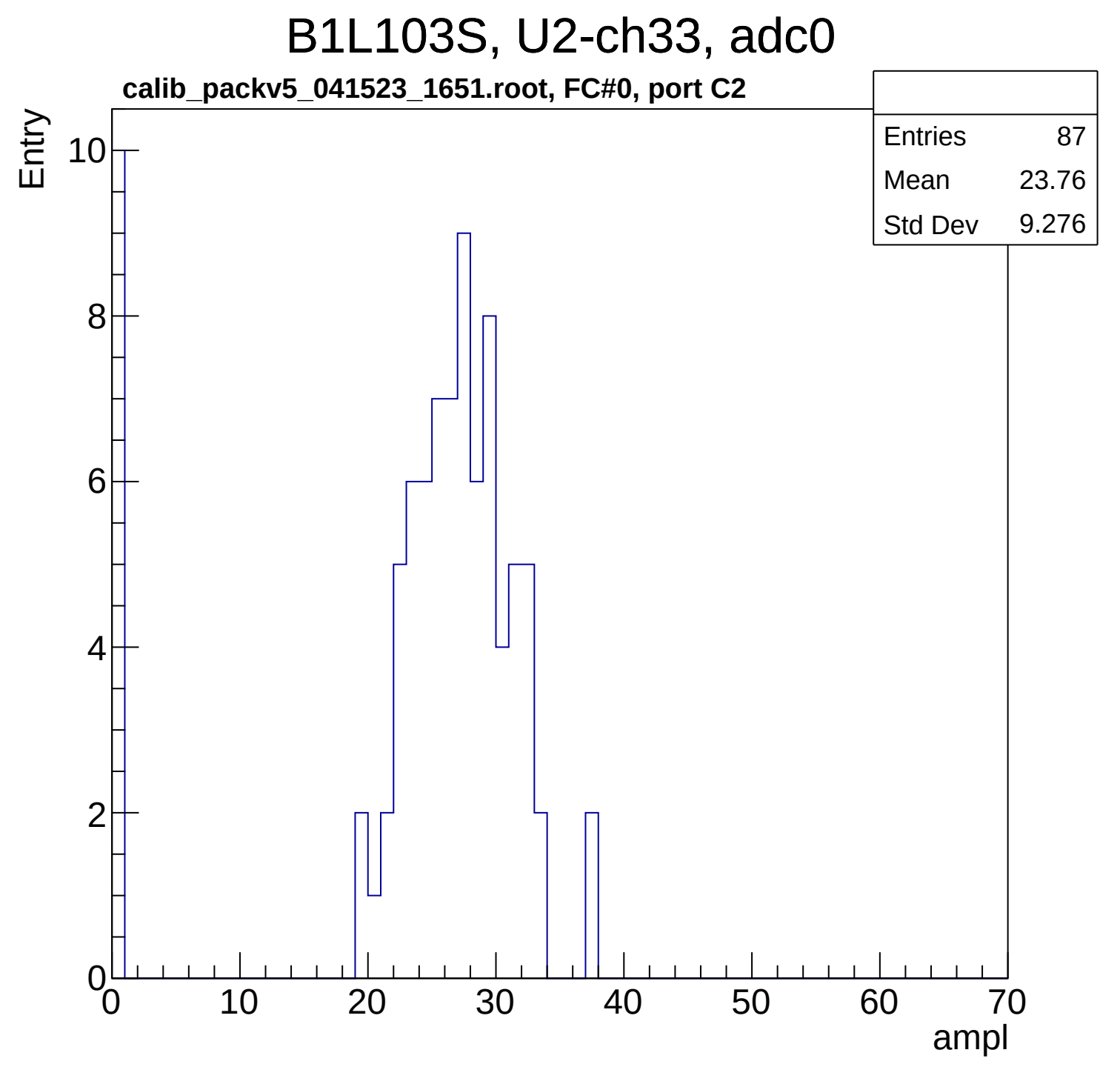

B1L103S, U2-ch32, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 45.91
Std Dev 6.416
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

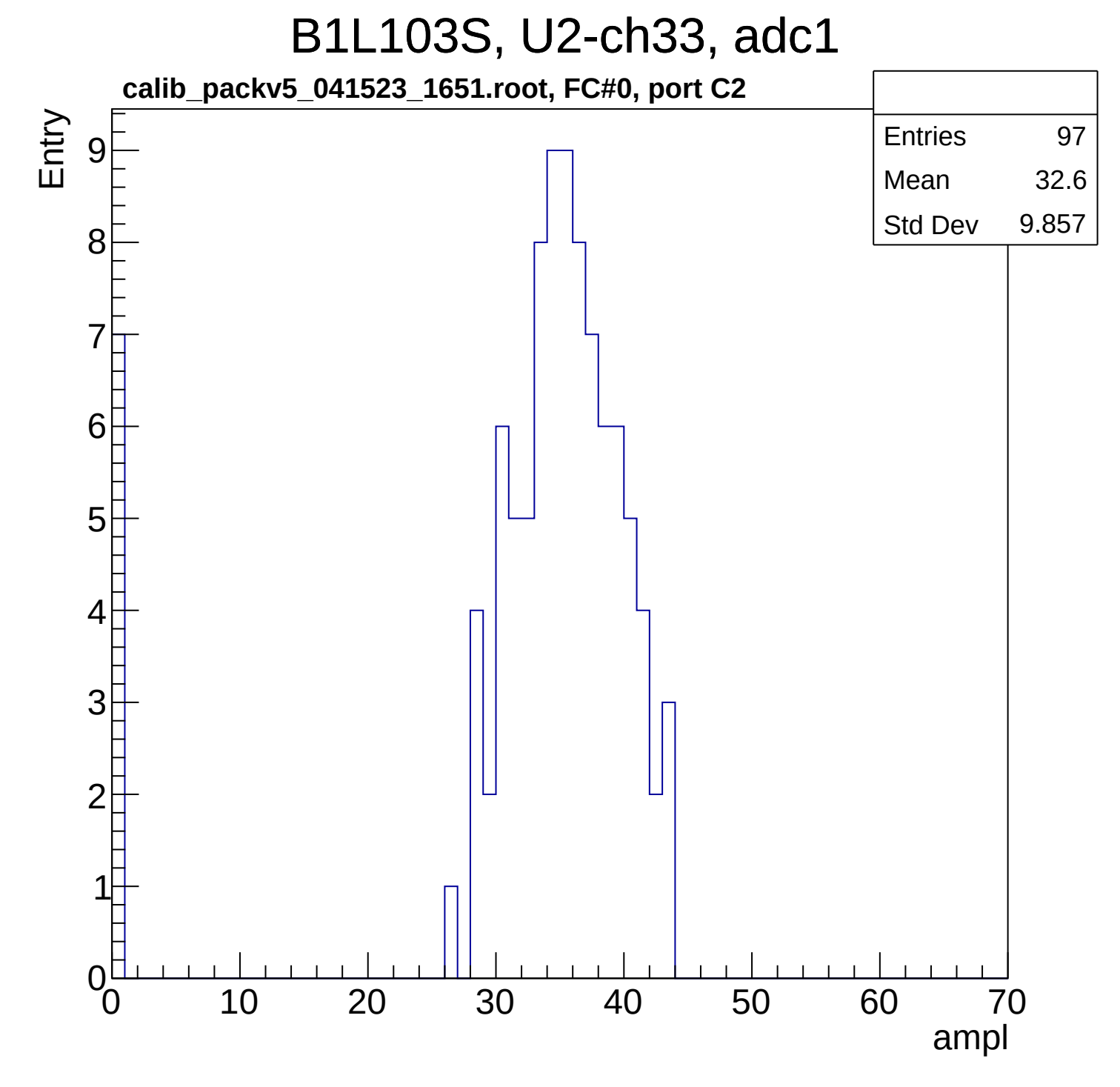

B1L103S, U2-ch32, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 52.85
Std Dev 3.482
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

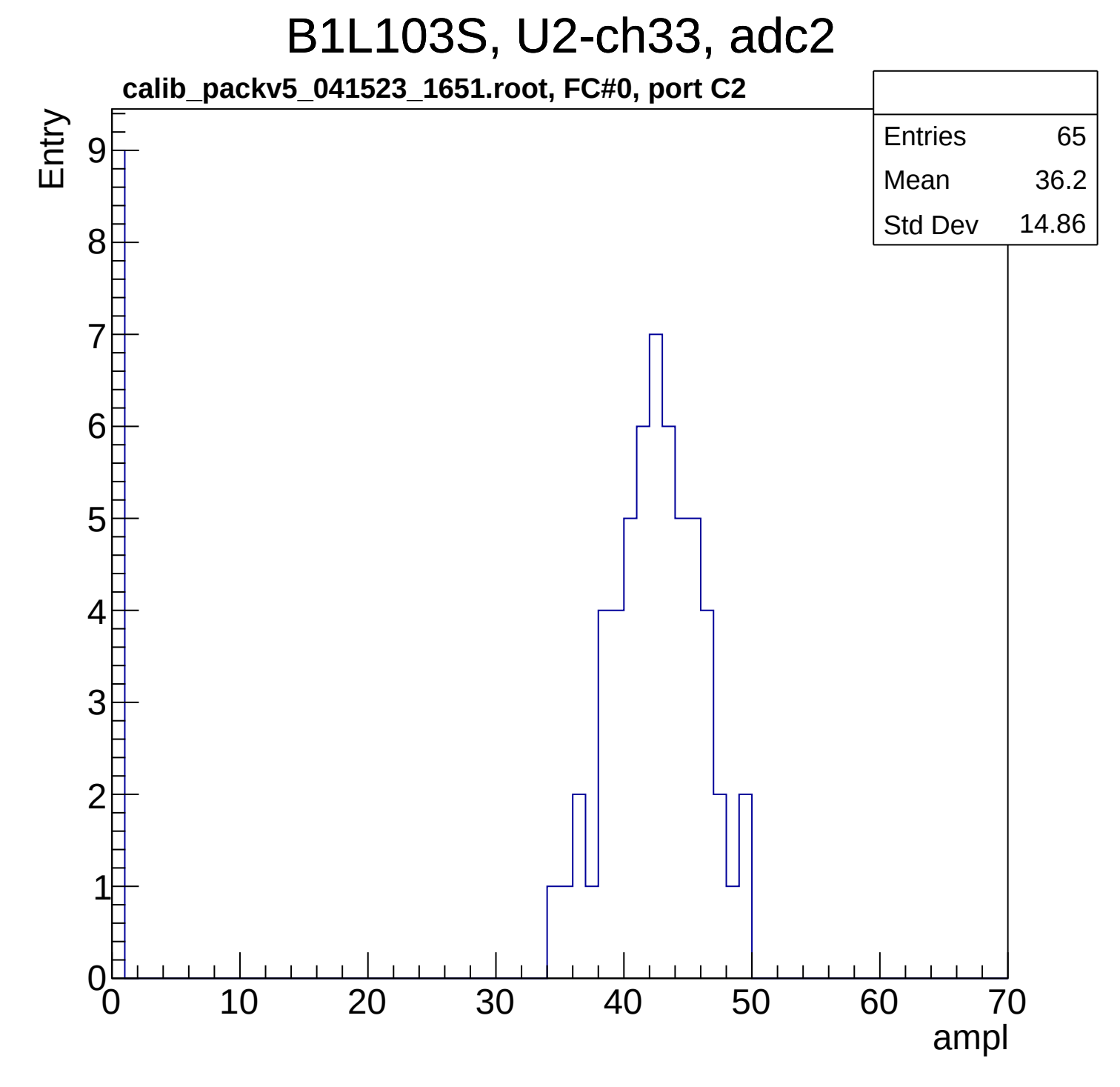

B1L103S, U2-ch32, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 57.49
Std Dev 8.408
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

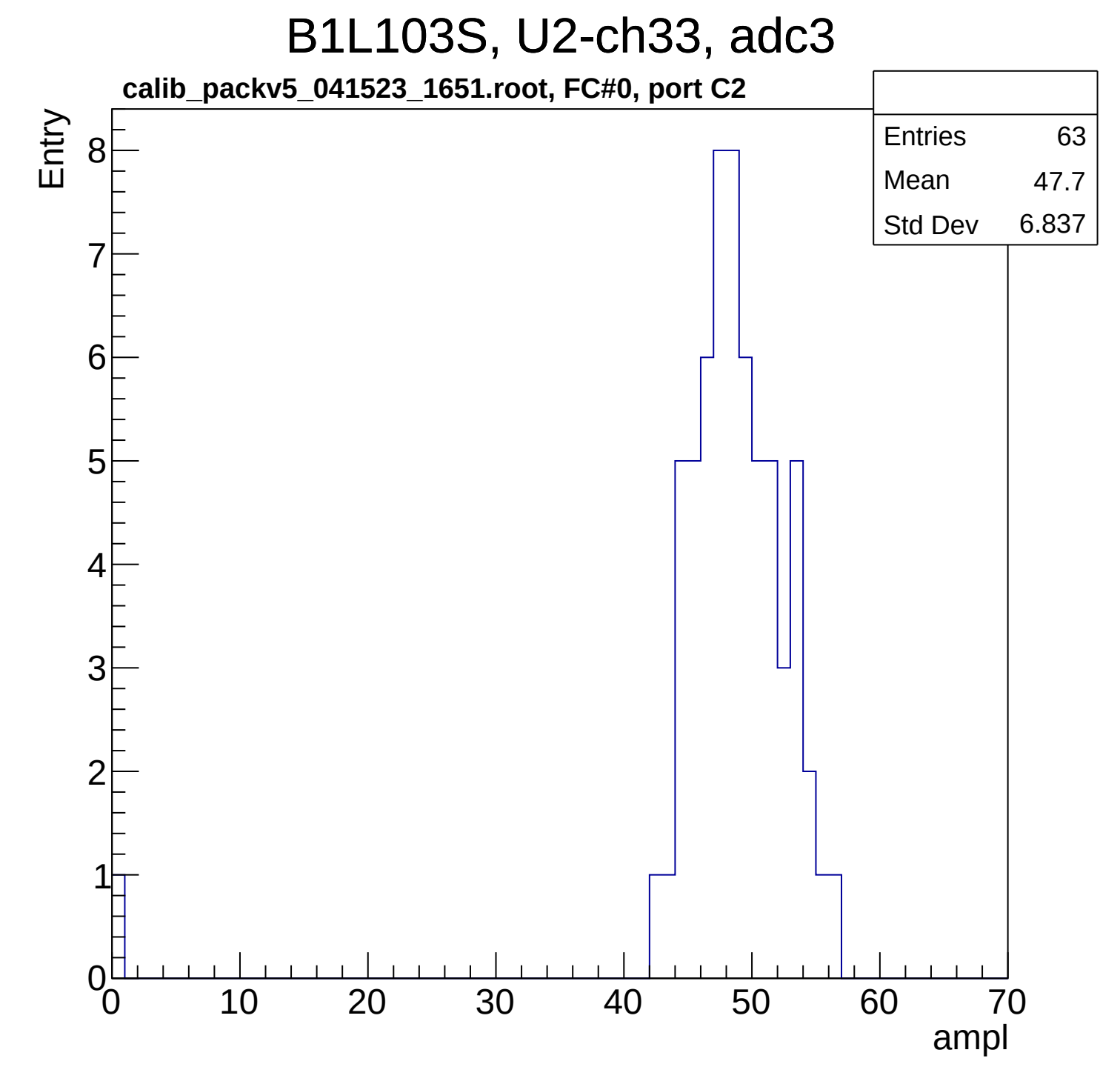

B1L103S, U2-ch32, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 61.1
Std Dev 1.63
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

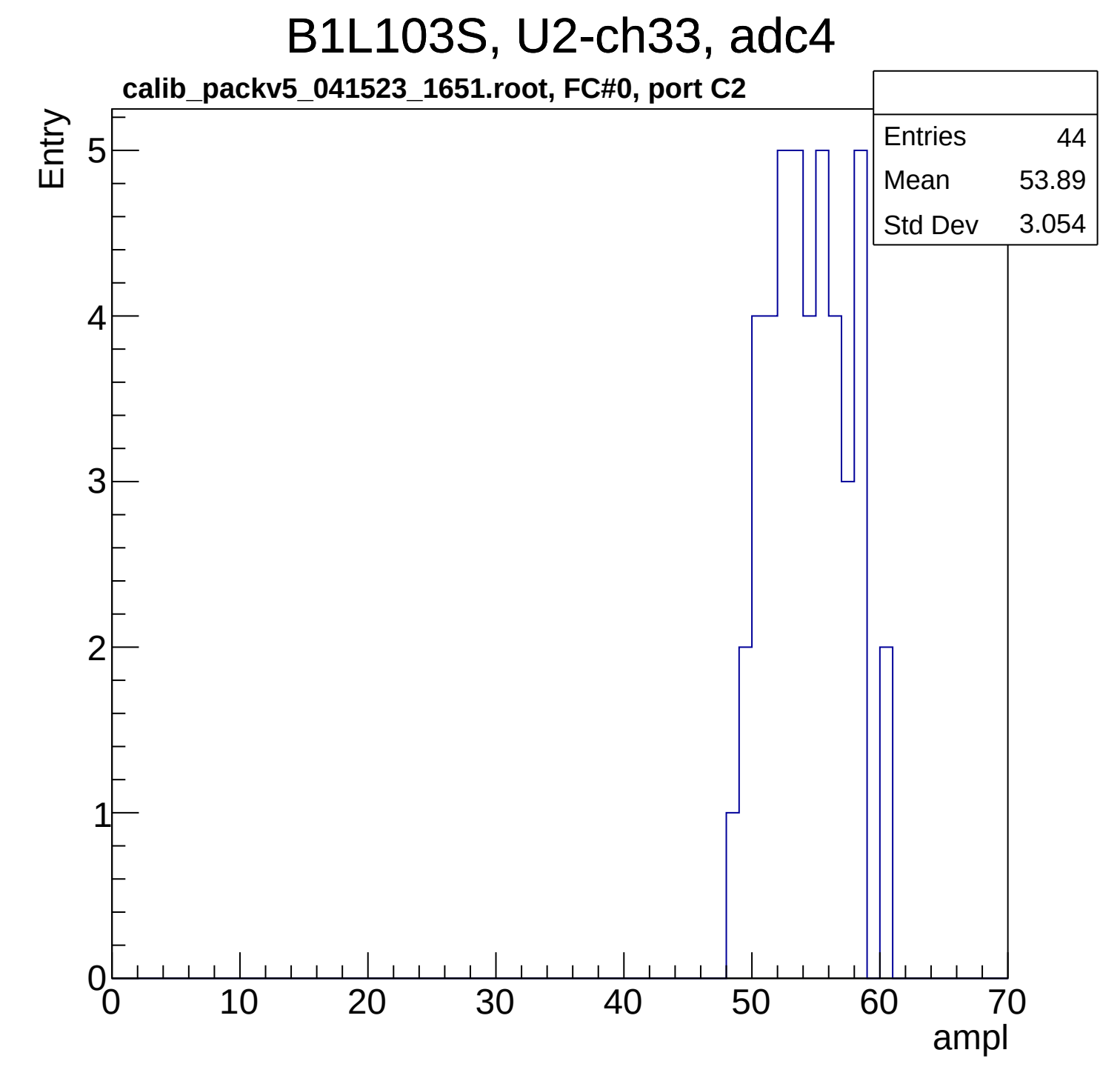

B1L103S, U2-ch32, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 4.474
Std Dev 14.64
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

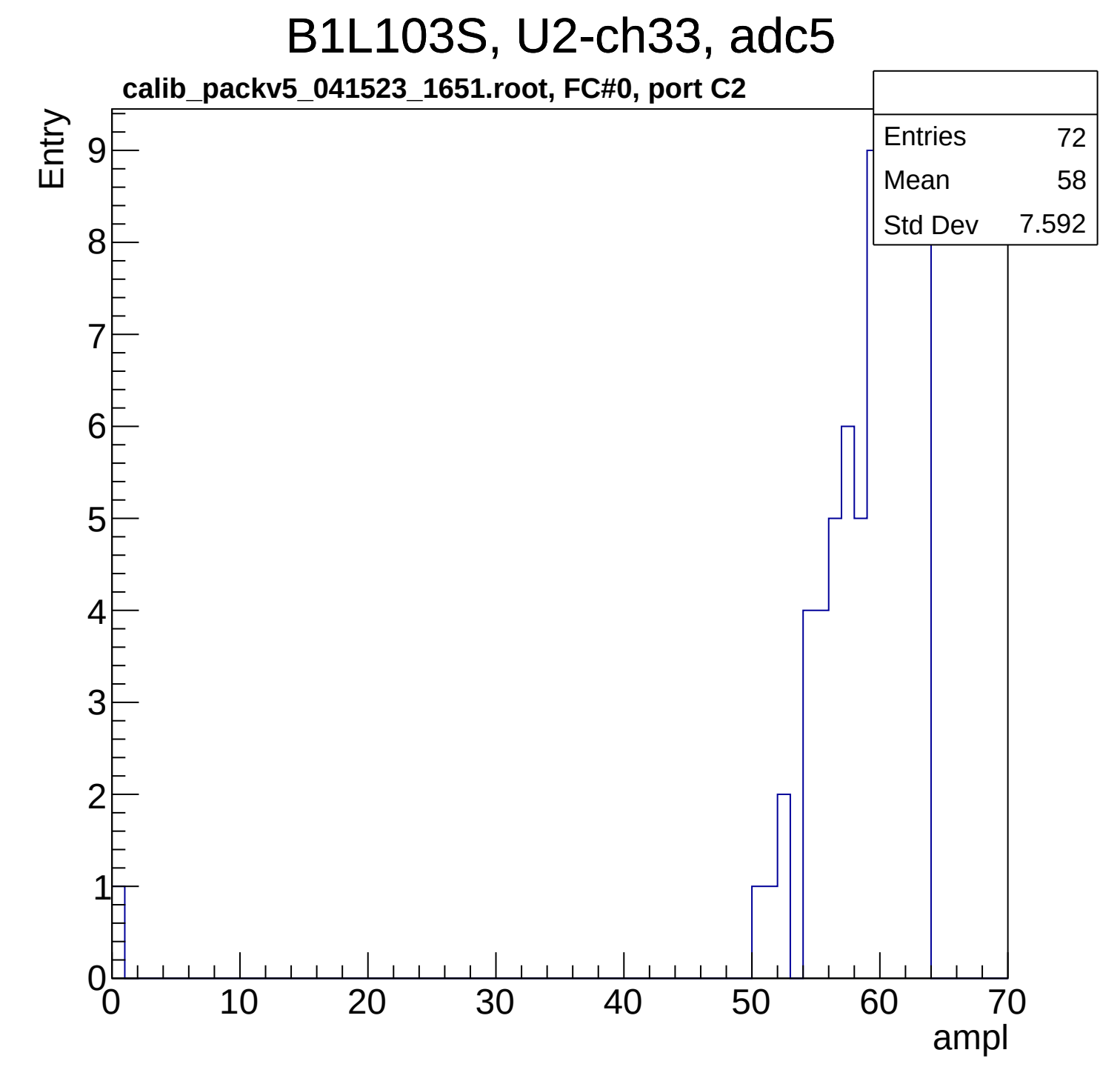

B1L103S, U2-ch33, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 23.76
Std Dev 9.276
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

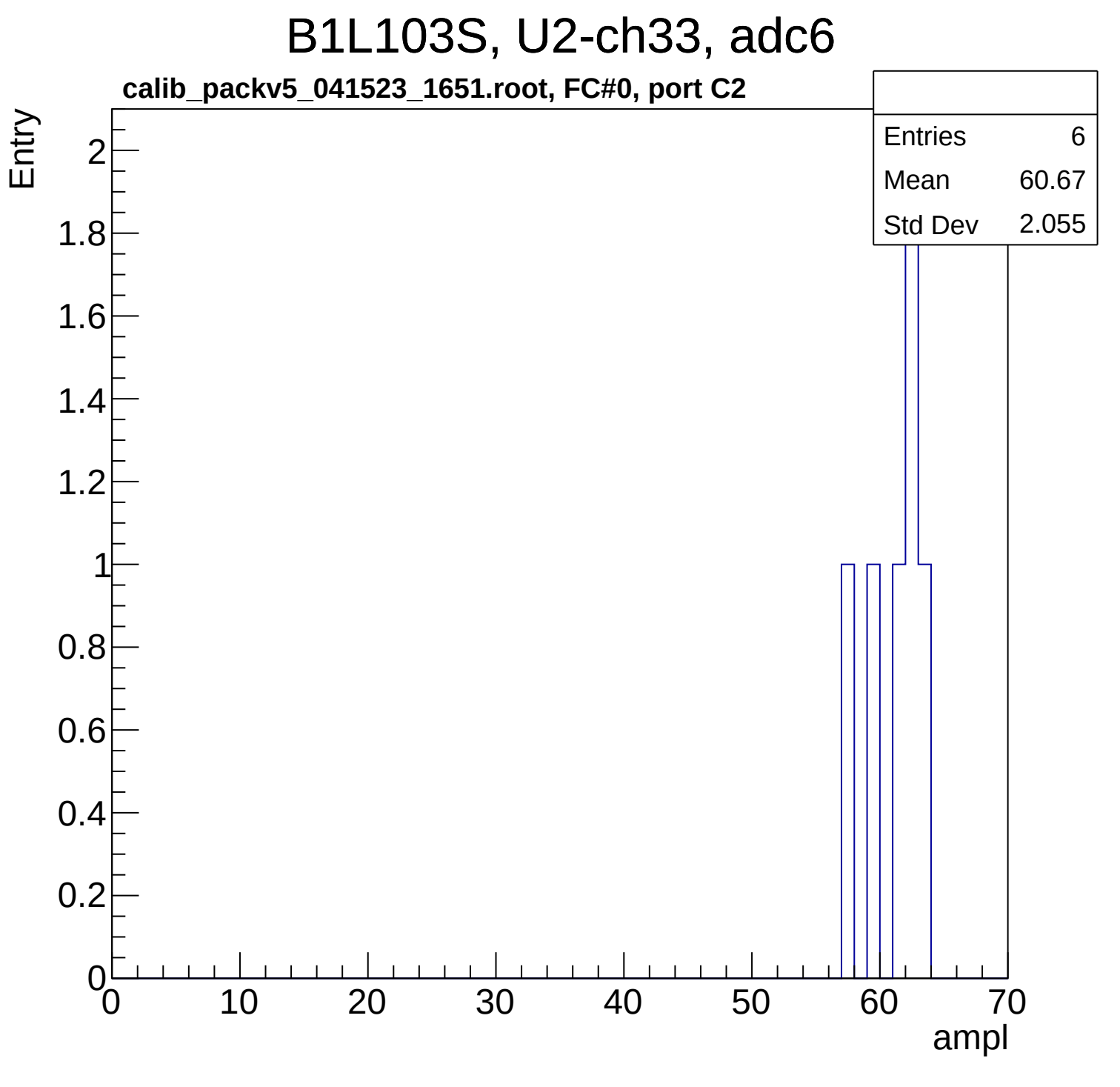

B1L103S, U2-ch33, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 32.6
Std Dev 9.857
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

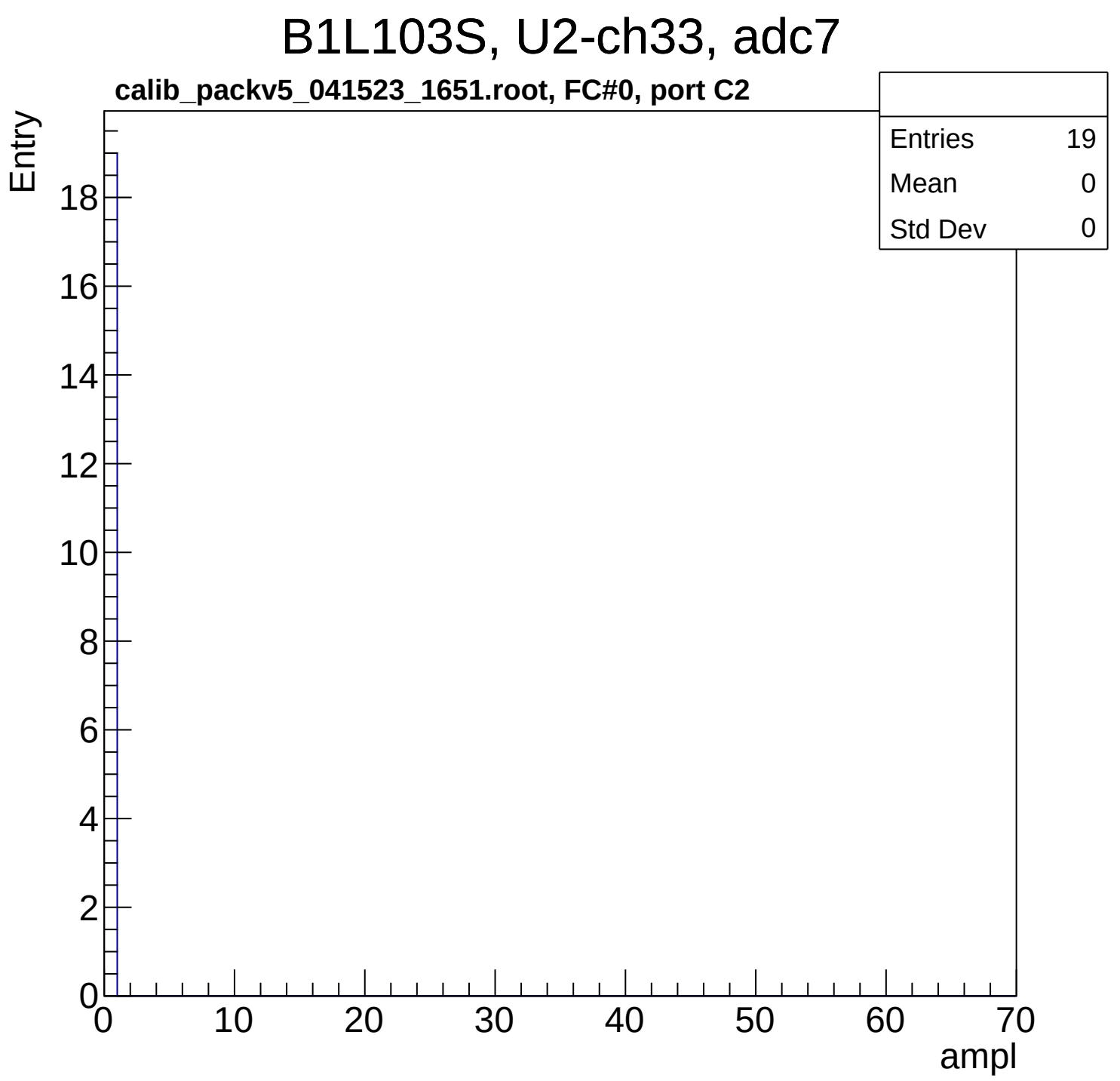

B1L103S, U2-ch33, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 36.2
Std Dev 14.86
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

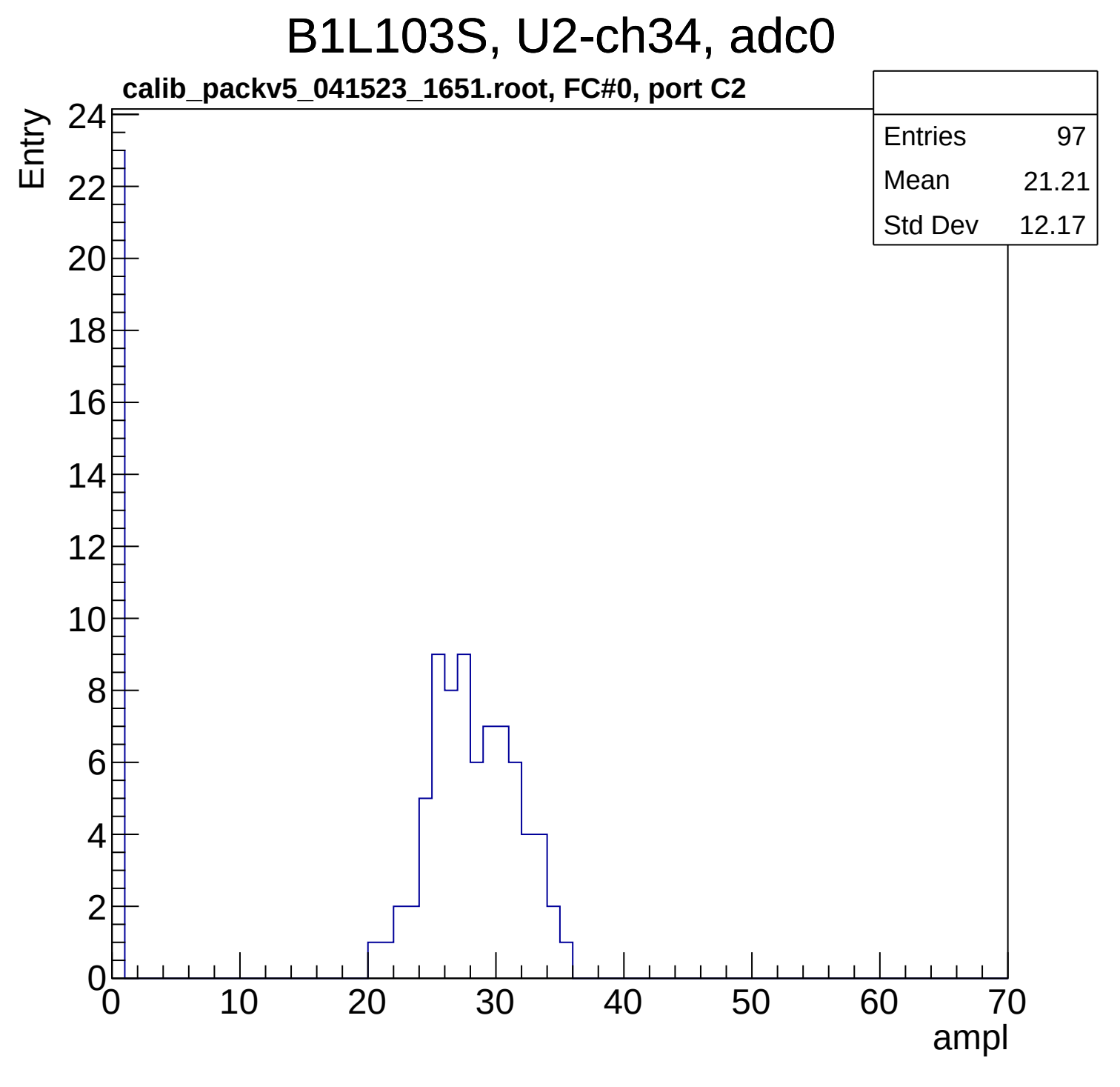

B1L103S, U2-ch33, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 47.7
Std Dev 6.837
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

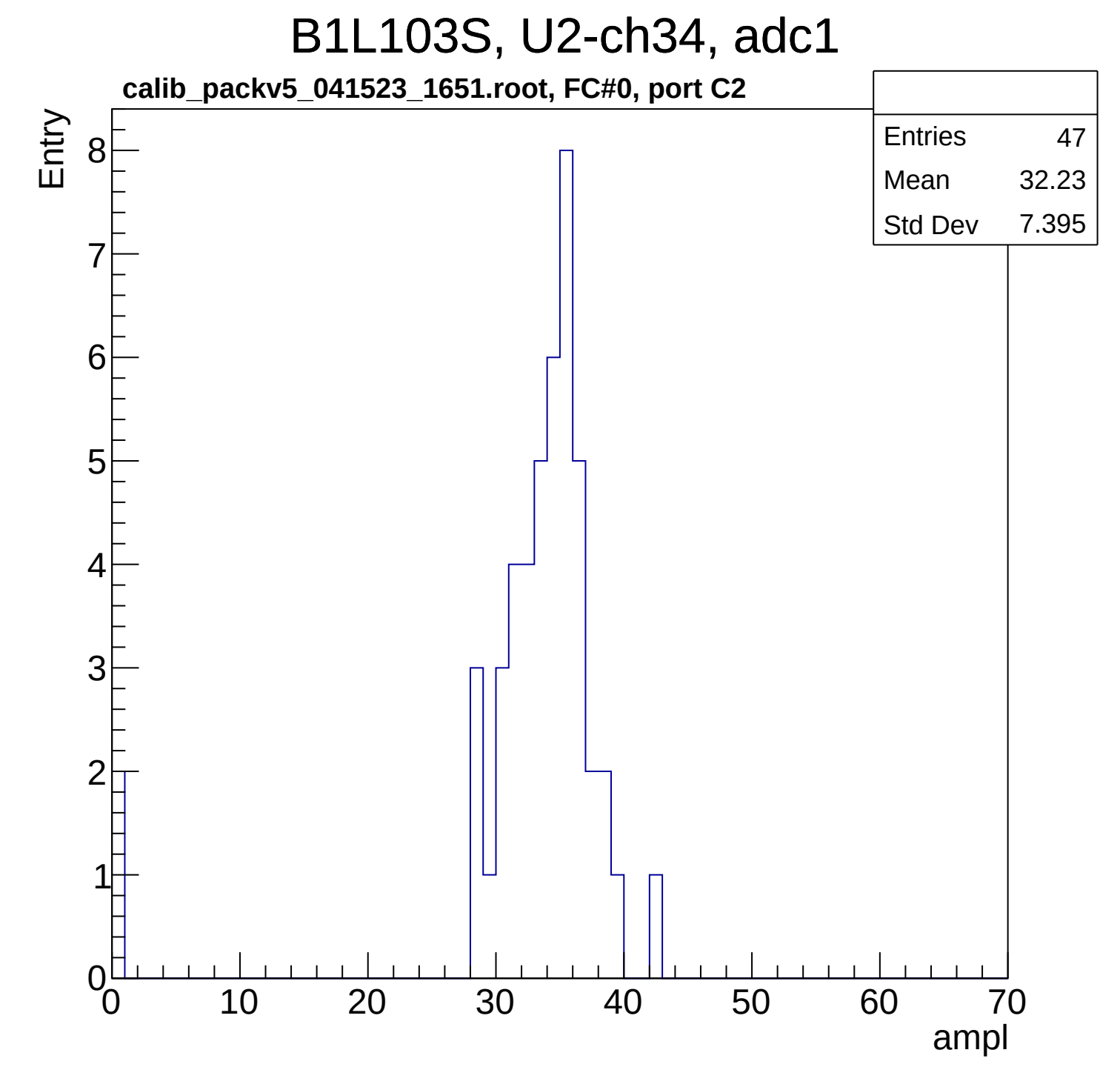

B1L103S, U2-ch33, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 53.89
Std Dev 3.054
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

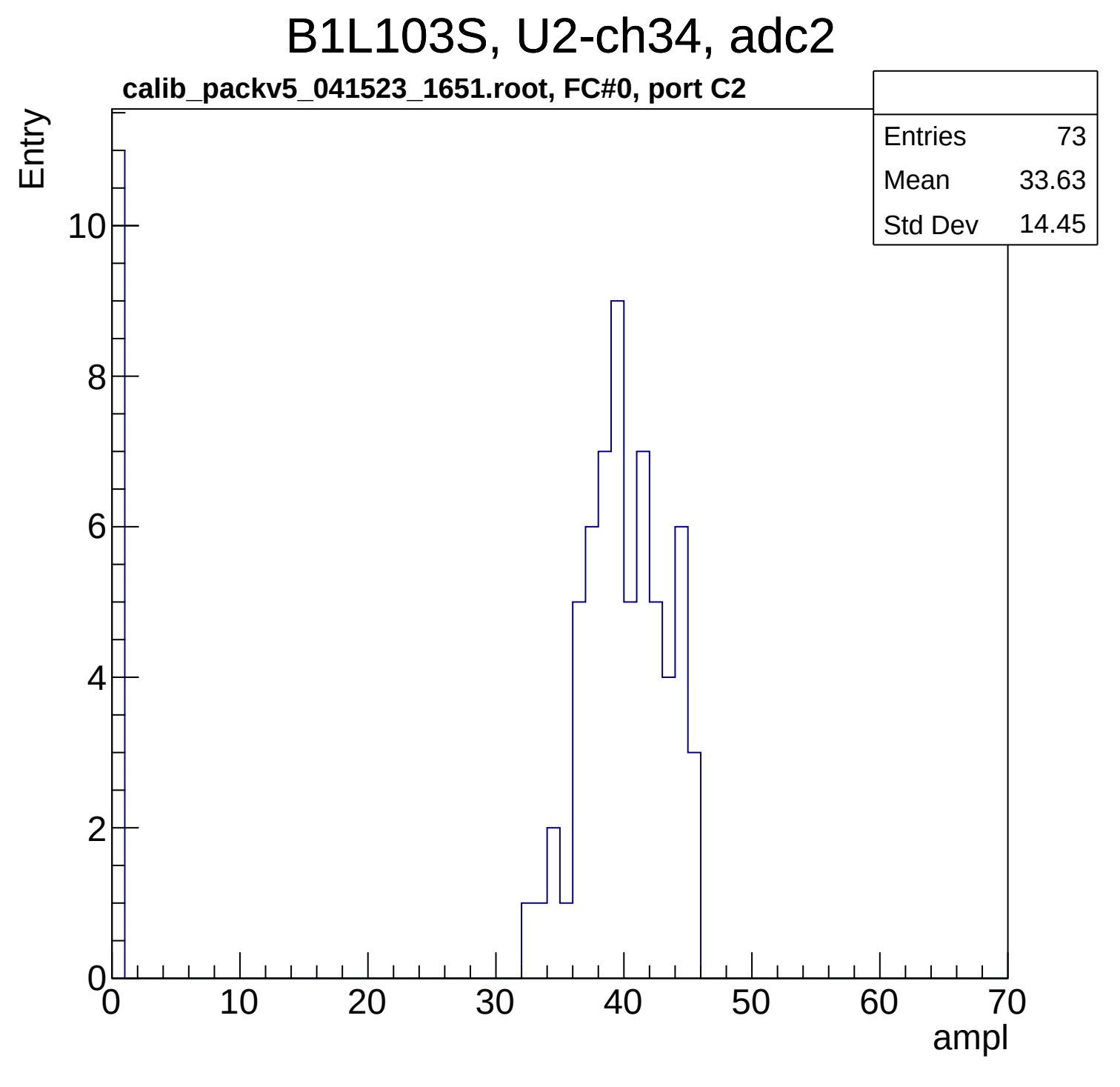

B1L103S, U2-ch33, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 58
Std Dev 7.592
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

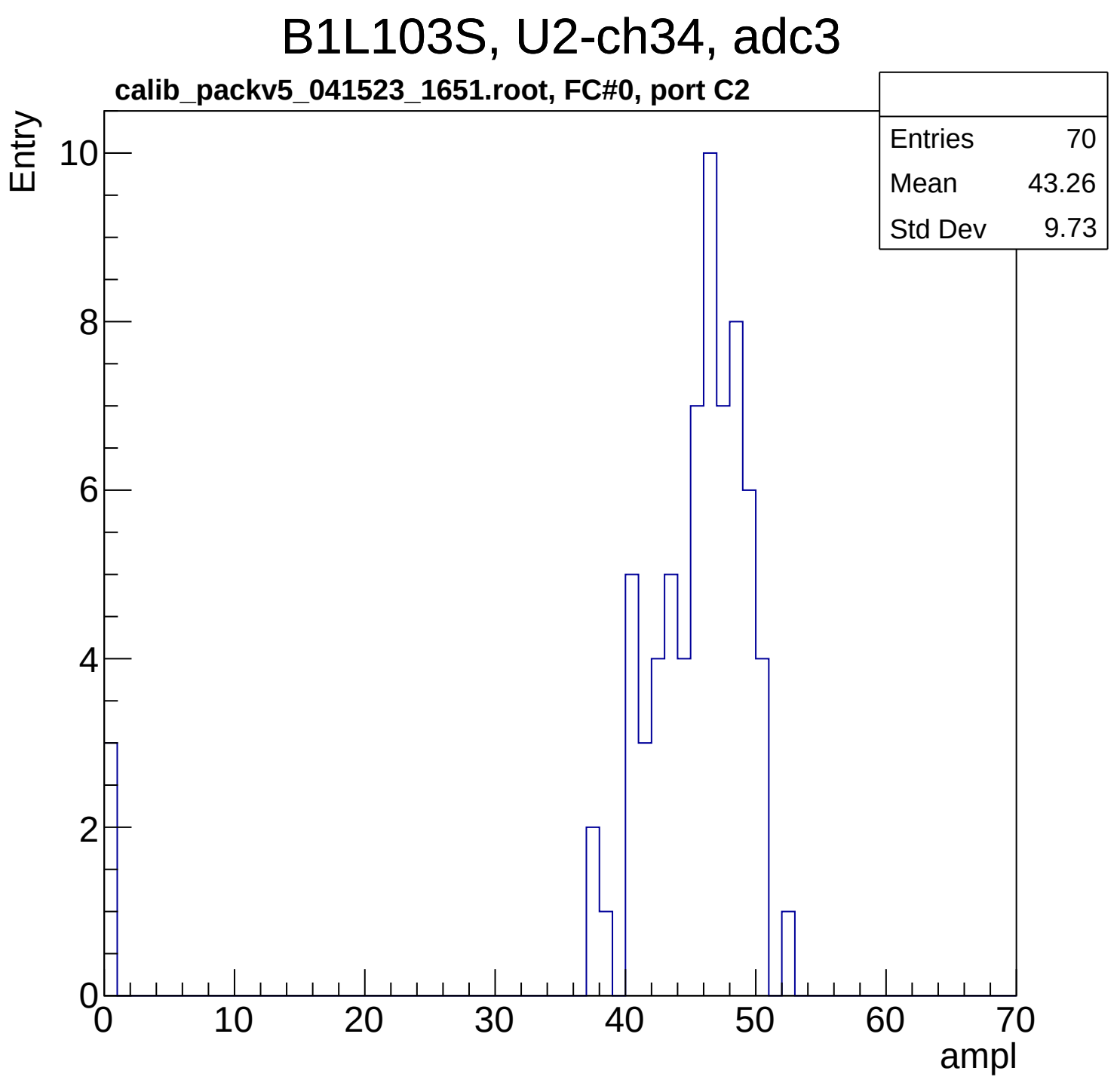

B1L103S, U2-ch33, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 60.67
Std Dev 2.055
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

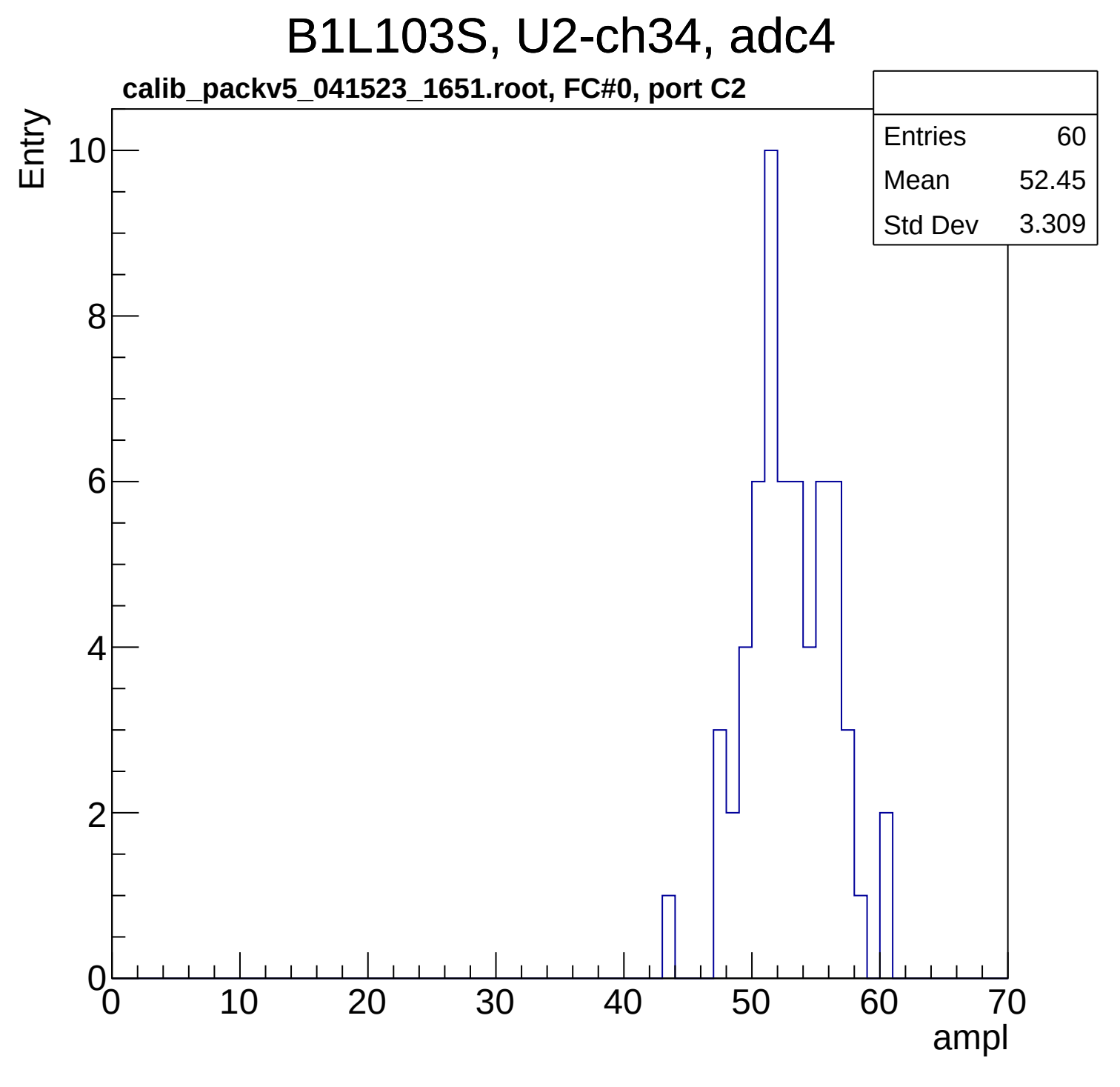

B1L103S, U2-ch33, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

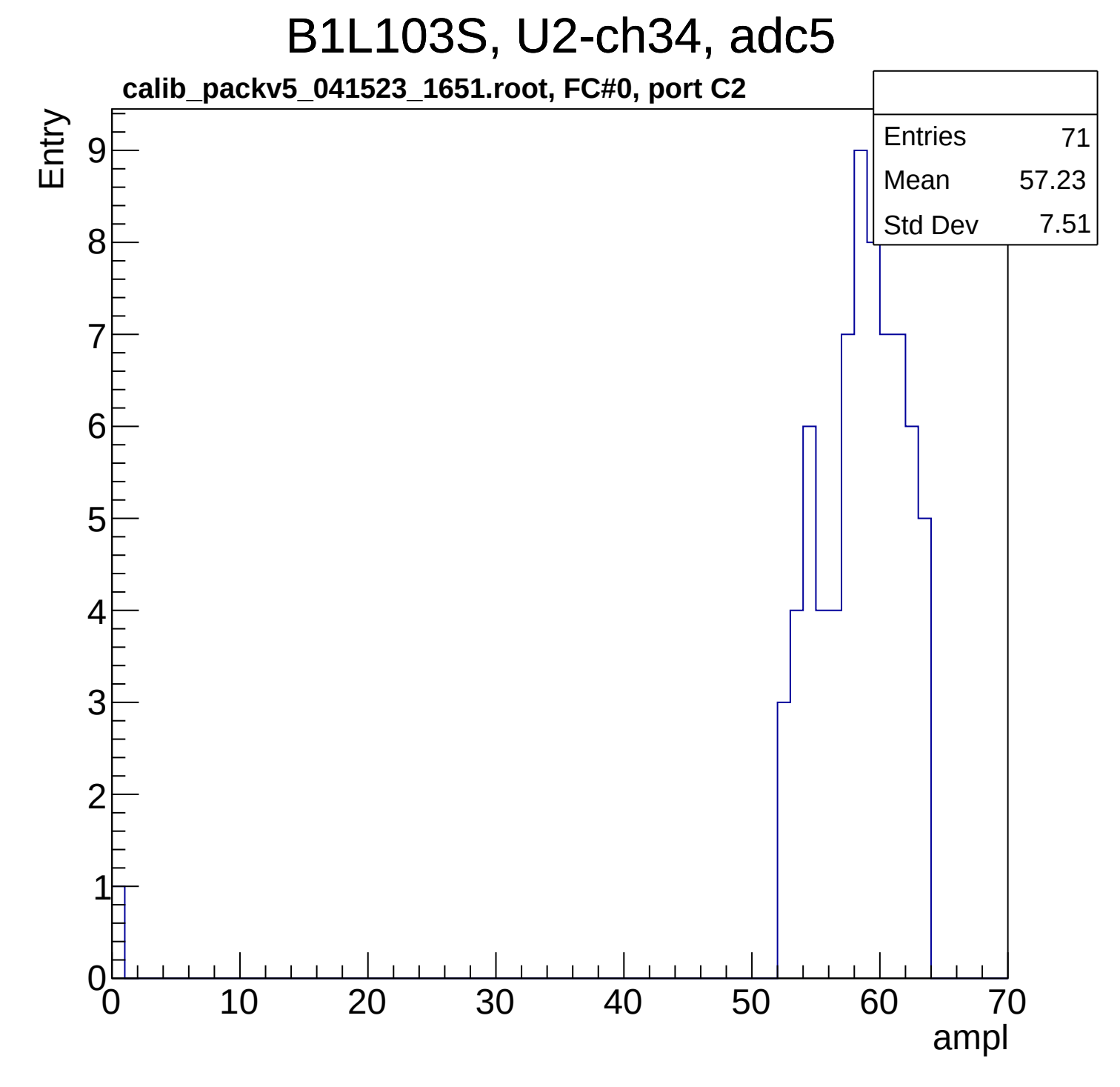

B1L103S, U2-ch34, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 21.21
Std Dev 12.17
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70

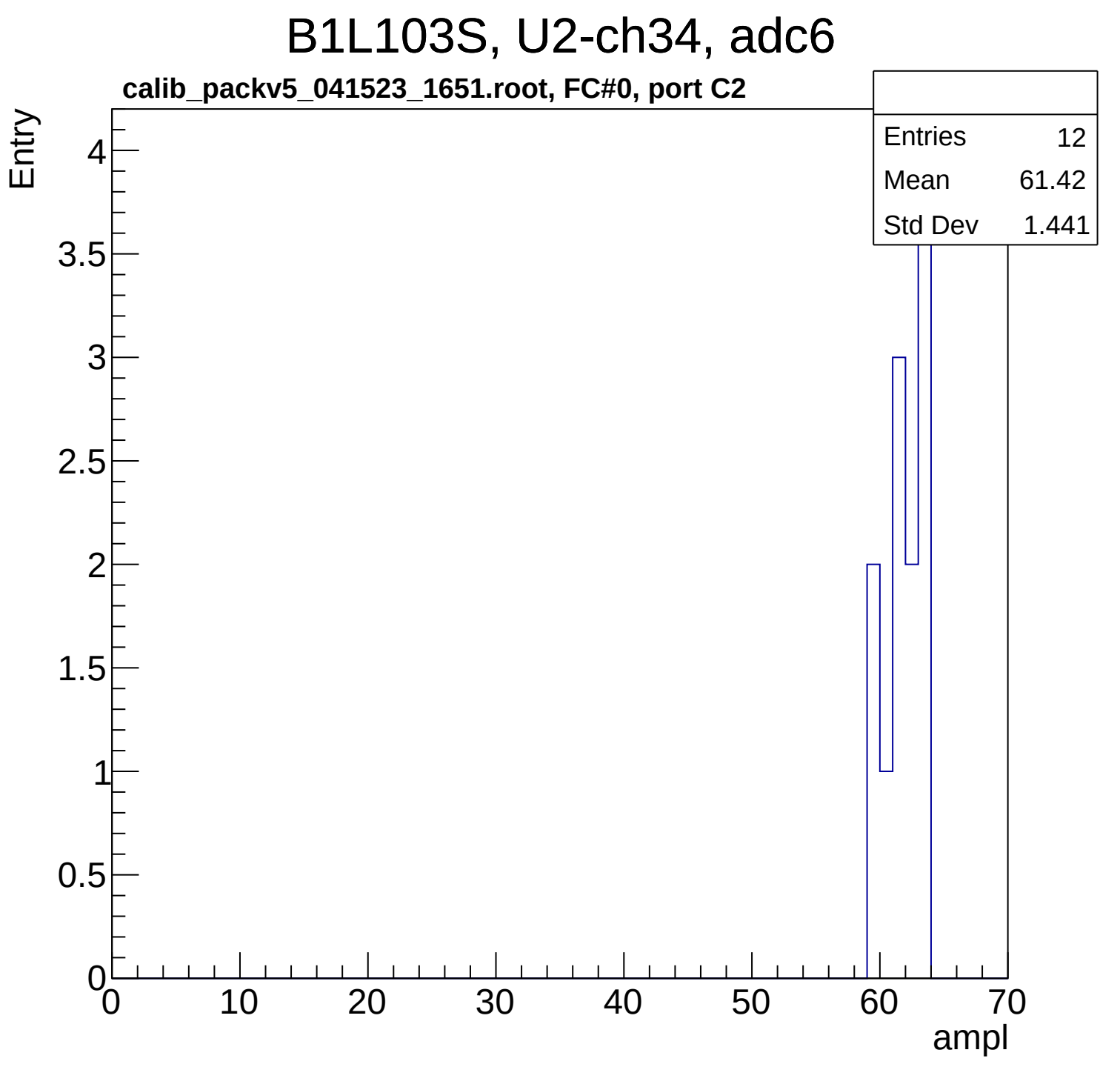

B1L103S, U2-ch34, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 32.23
Std Dev 7.395
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

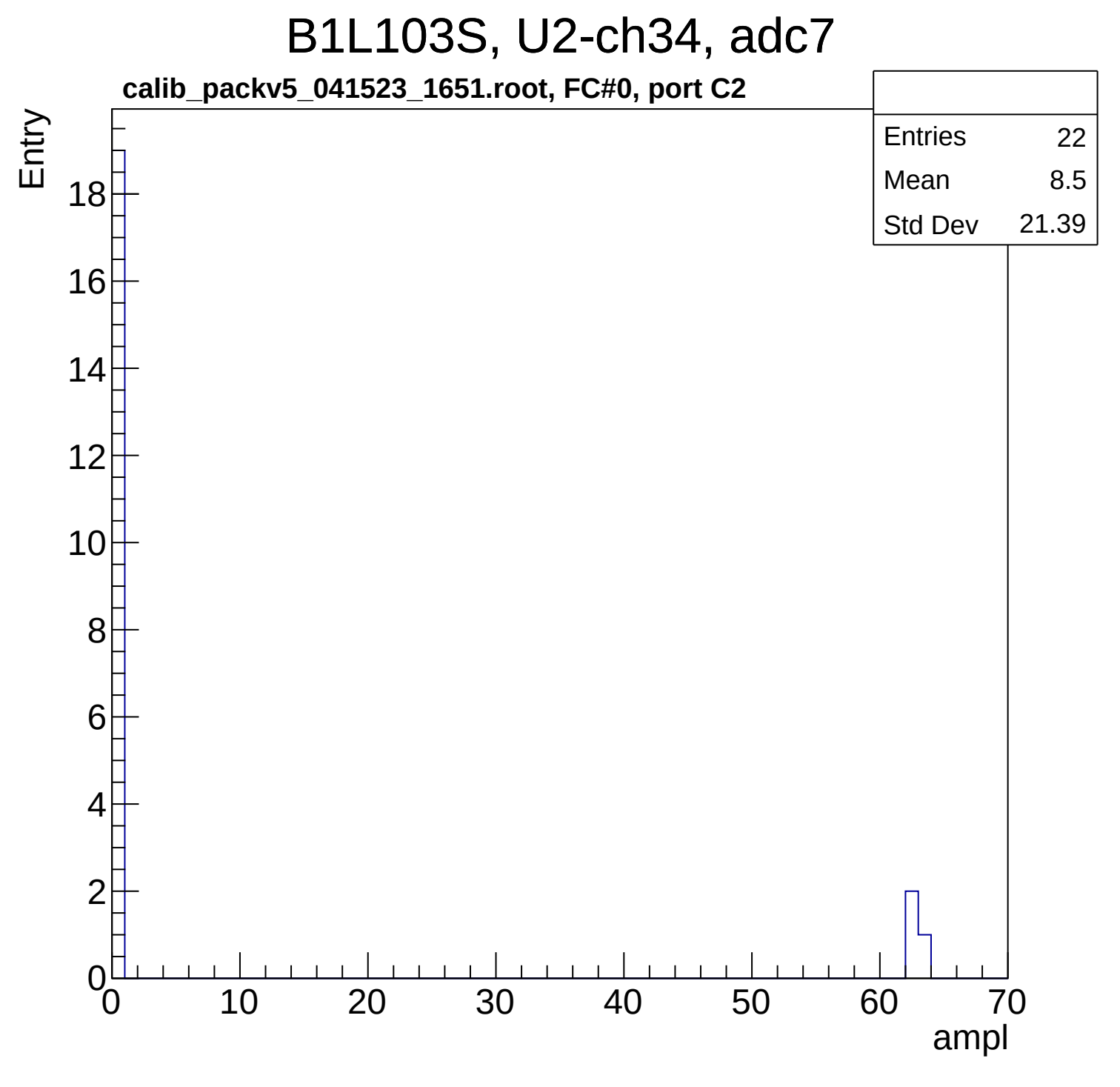

B1L103S, U2-ch34, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 33.63
Std Dev 14.45
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

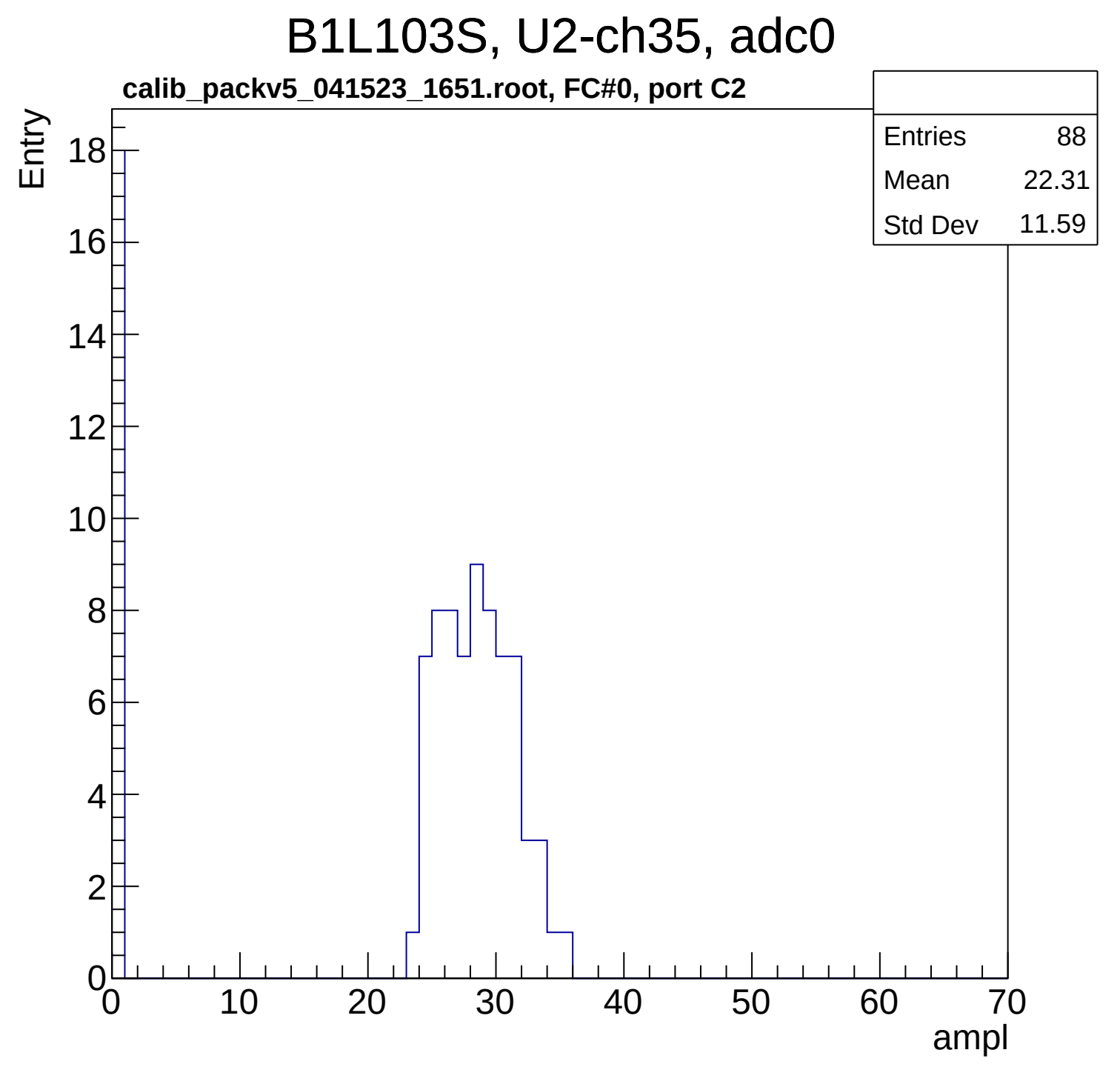

B1L103S, U2-ch34, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 43.26
Std Dev 9.73
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

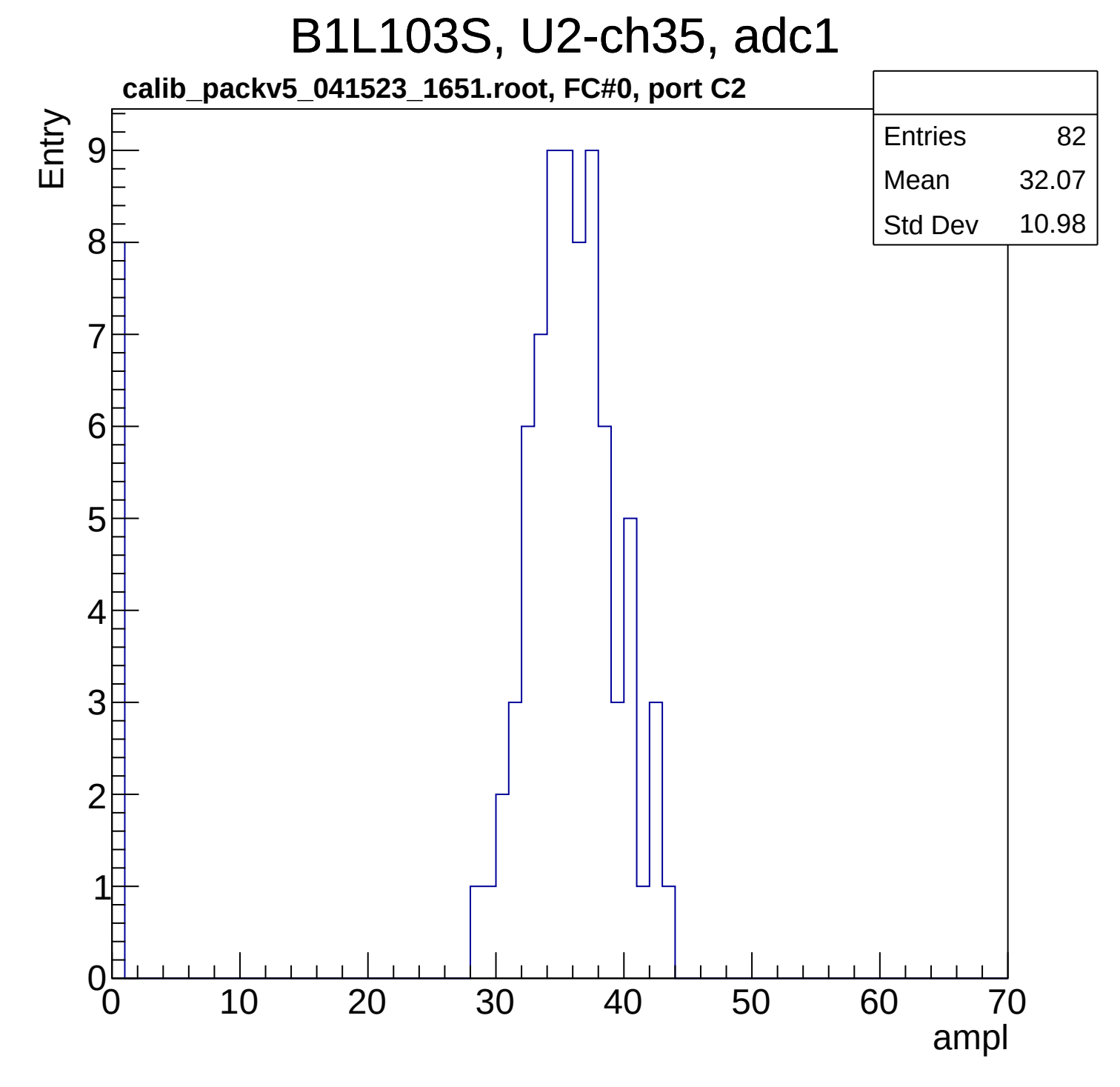

B1L103S, U2-ch34, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 52.45
Std Dev 3.309
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

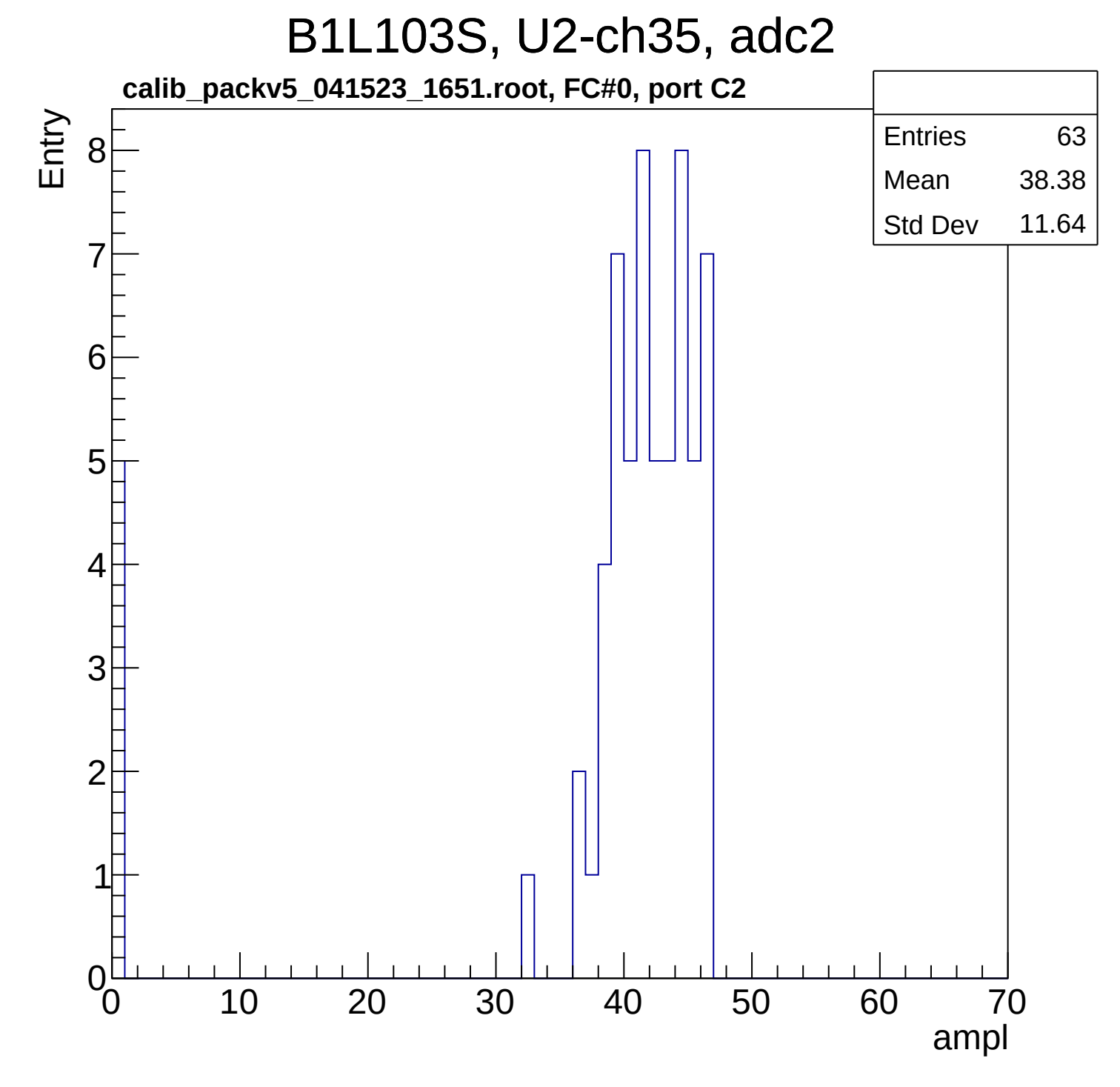

B1L103S, U2-ch34, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 57.23
Std Dev 7.51
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

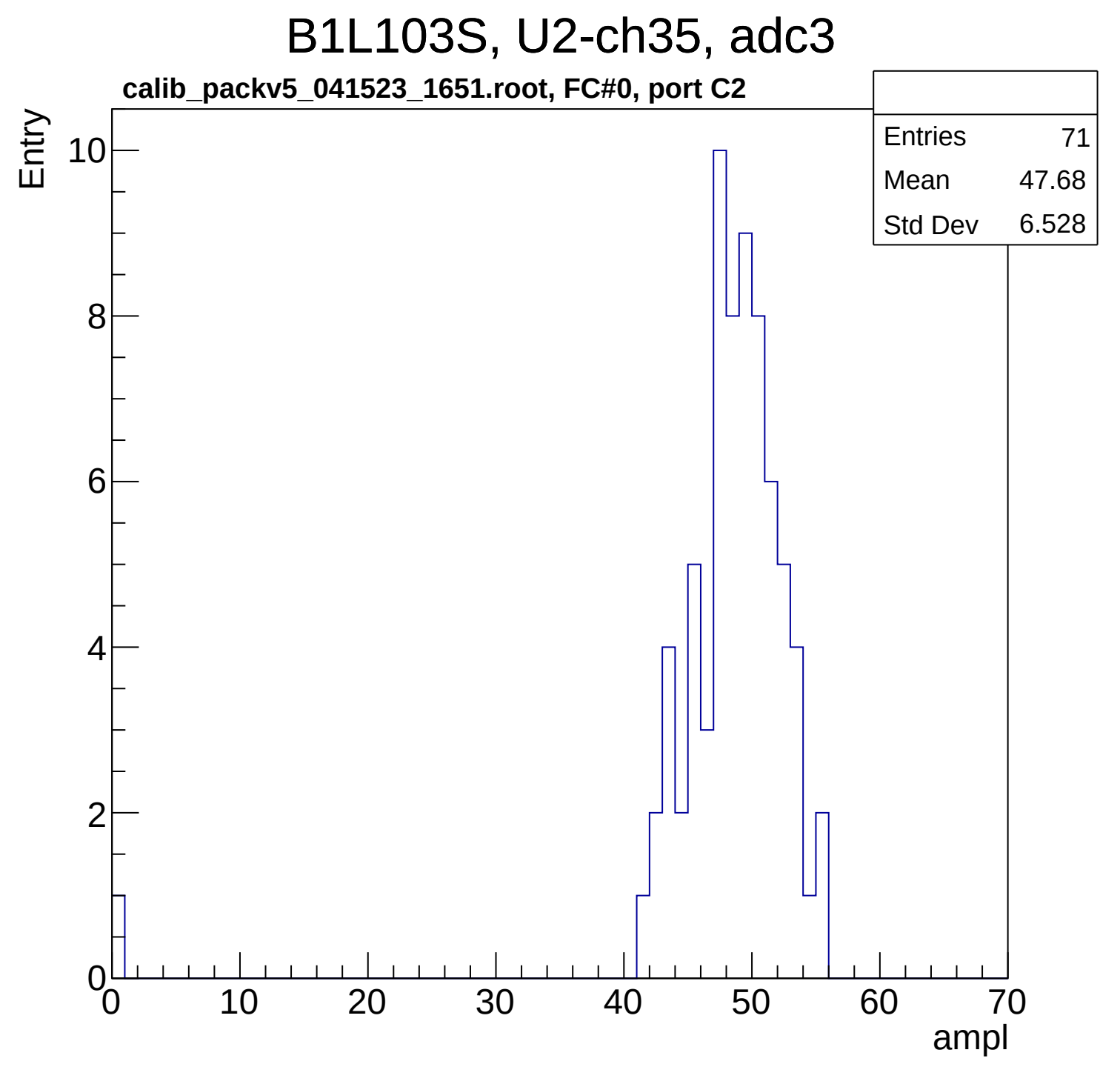

B1L103S, U2-ch34, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.42
Std Dev 1.441
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

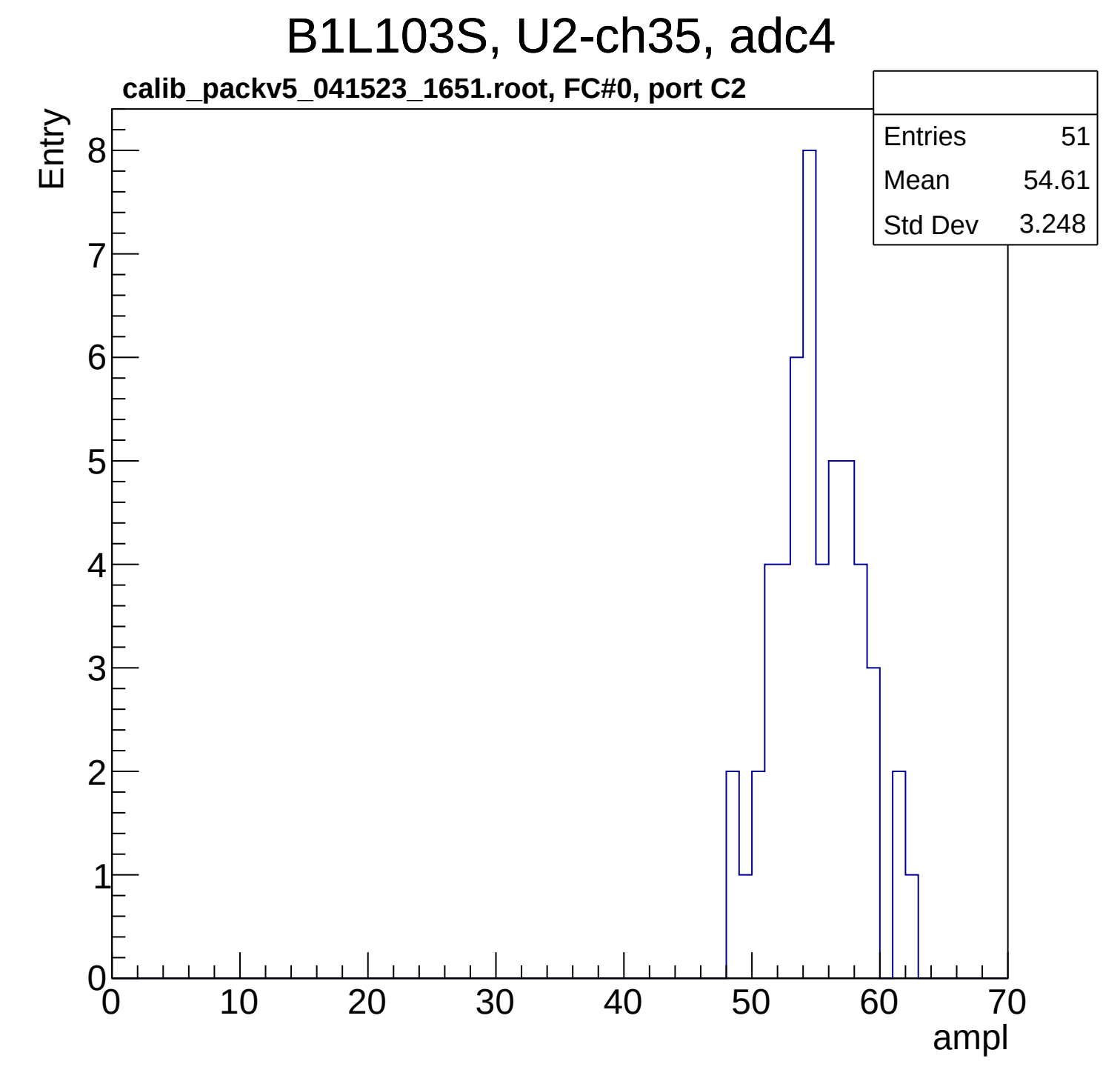

B1L103S, U2-ch34, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.5
Std Dev 21.39
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

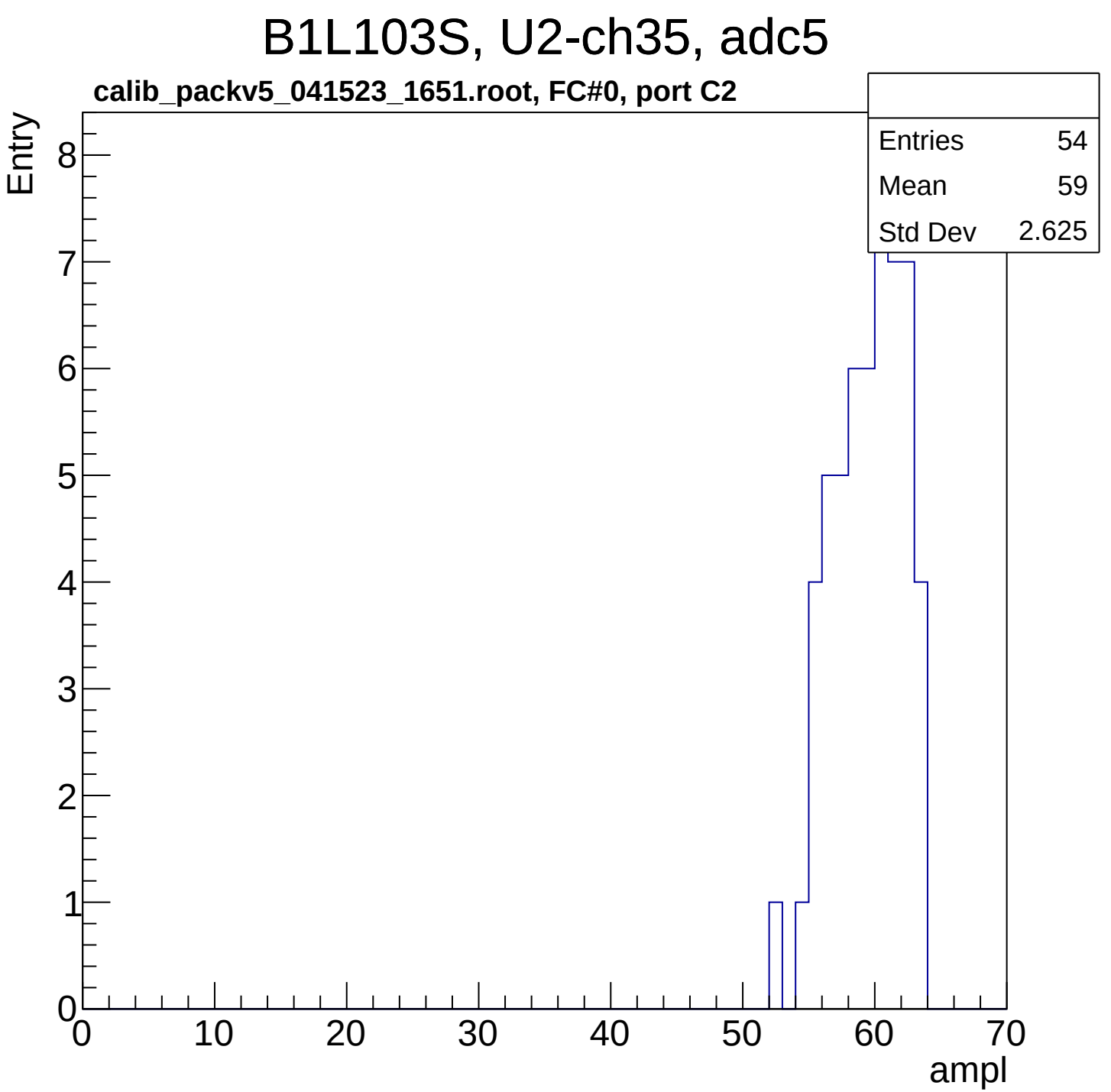

B1L103S, U2-ch35, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 22.31
Std Dev 11.59
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

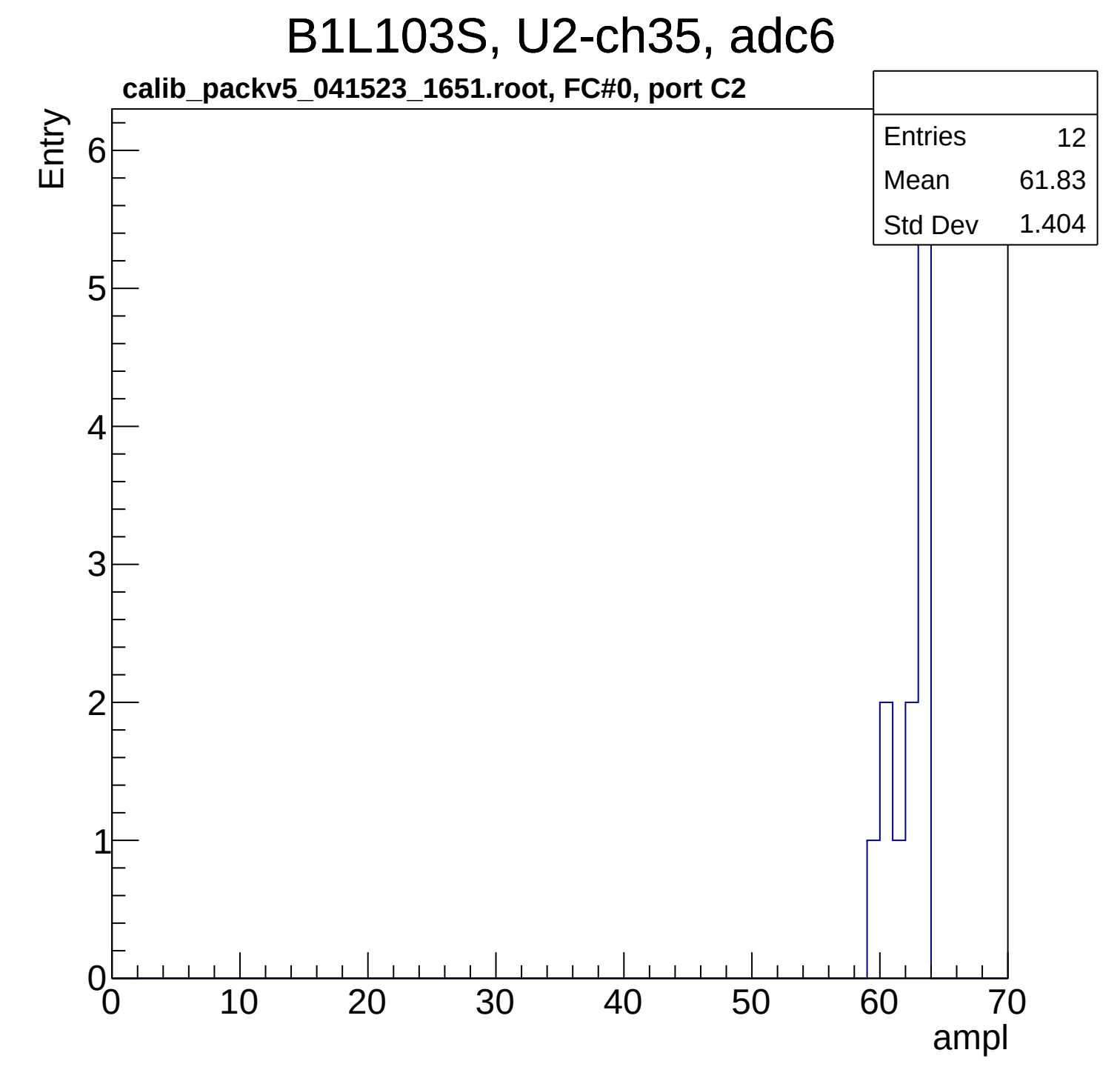

B1L103S, U2-ch35, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 32.07
Std Dev 10.98
Entry
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70
ampl

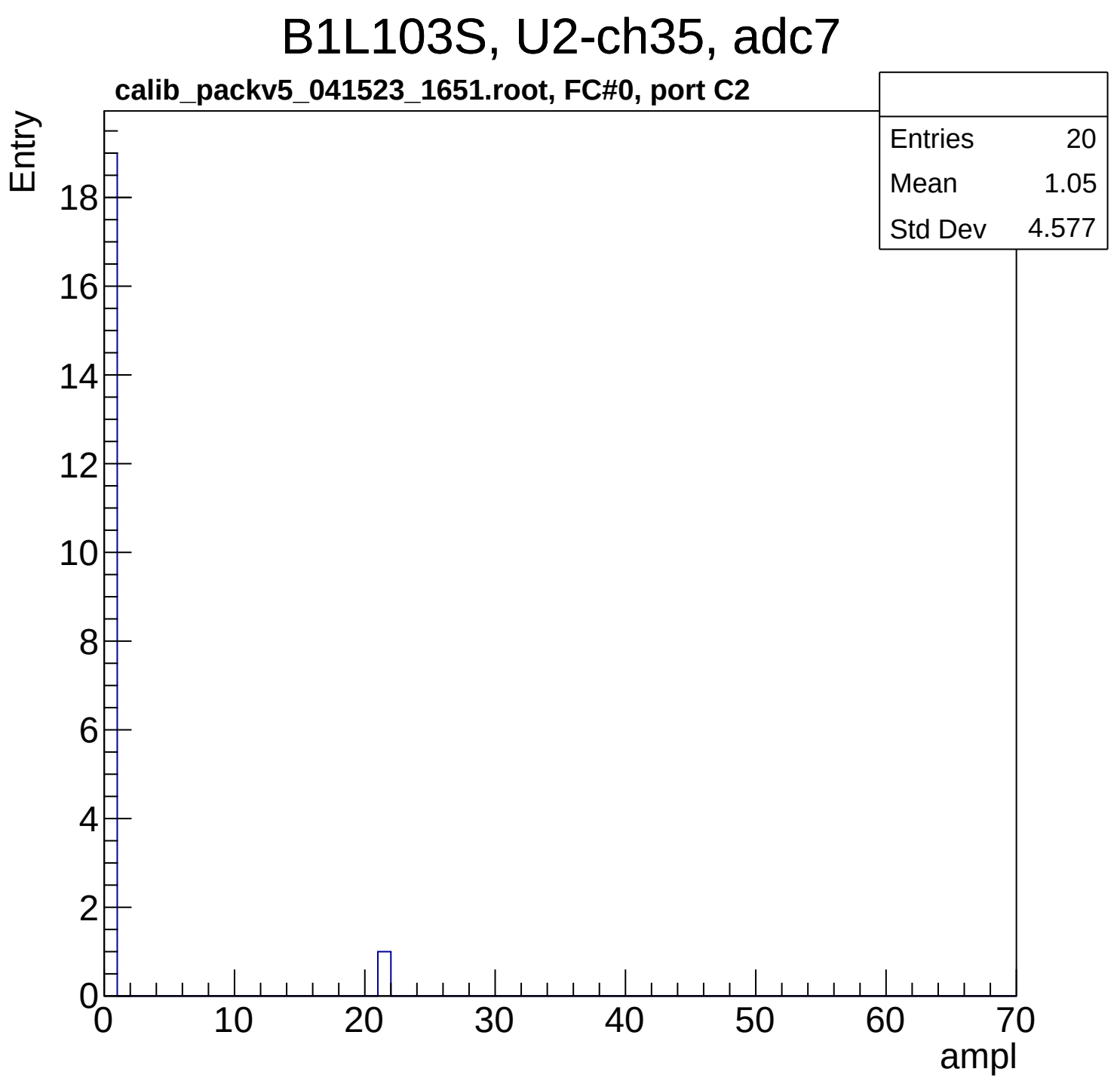

B1L103S, U2-ch35, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 38.38
Std Dev 11.64
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

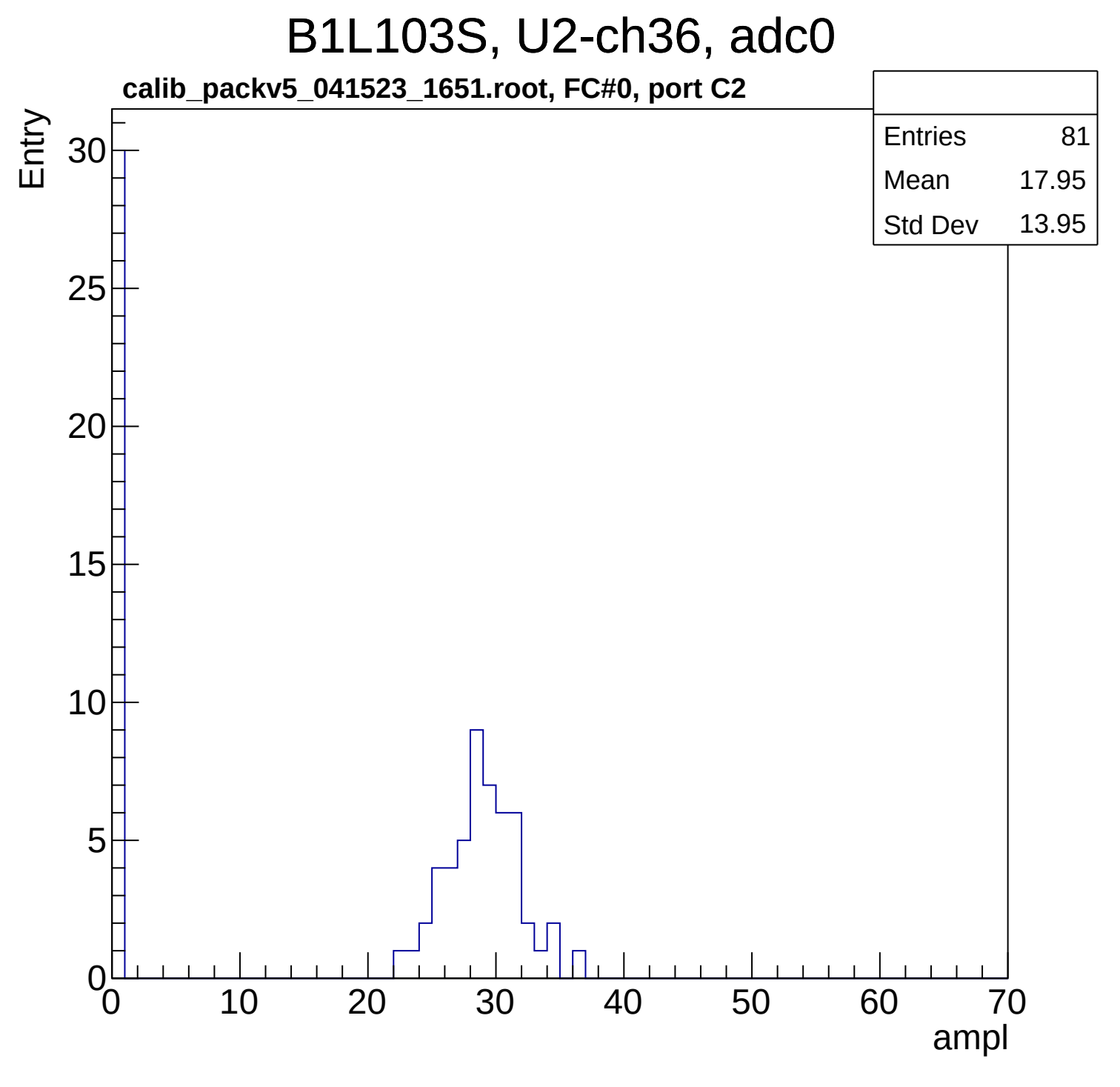

B1L103S, U2-ch35, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 47.68
Std Dev 6.528
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

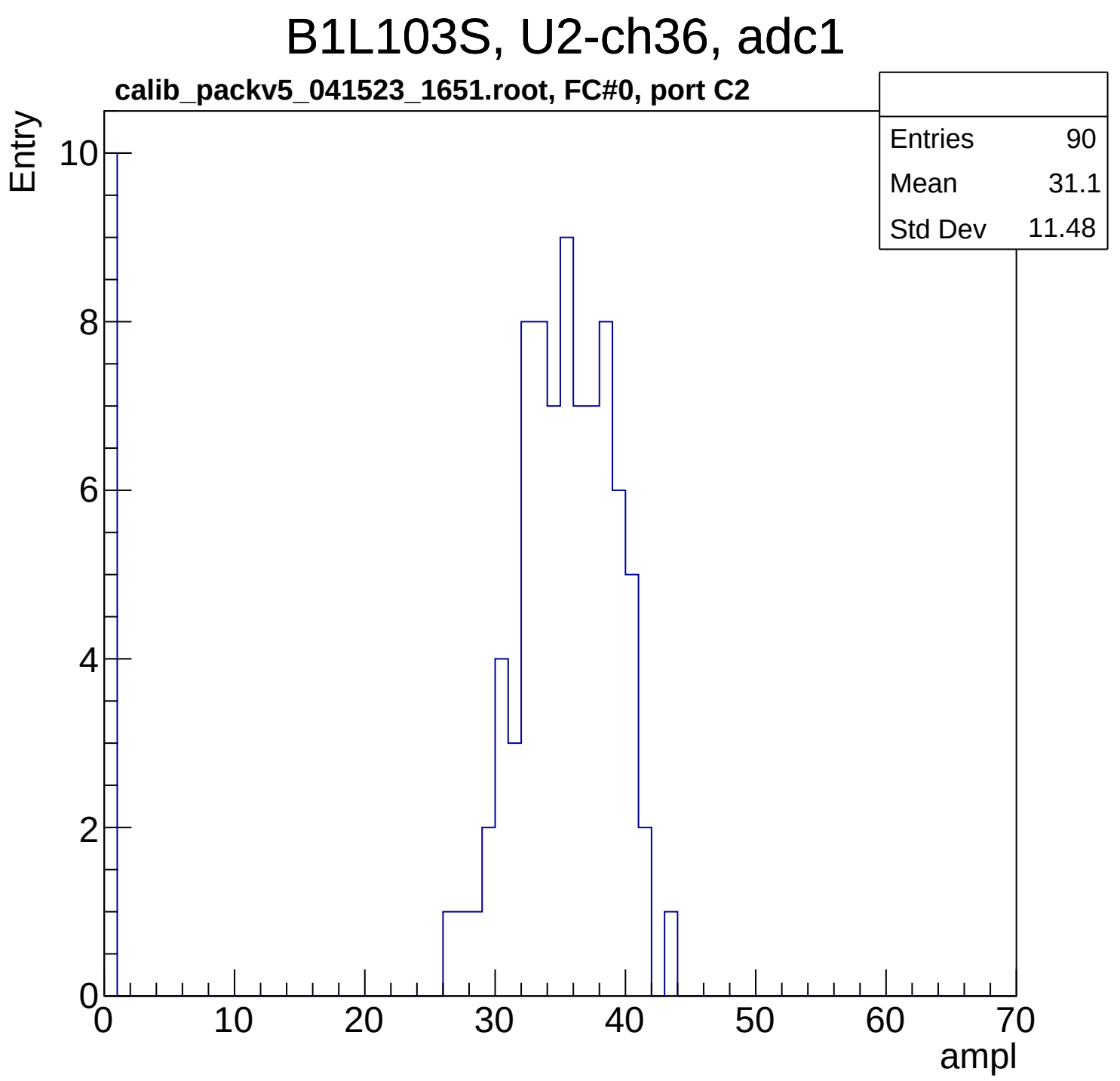

B1L103S, U2-ch35, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 54.61
Std Dev 3.248
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

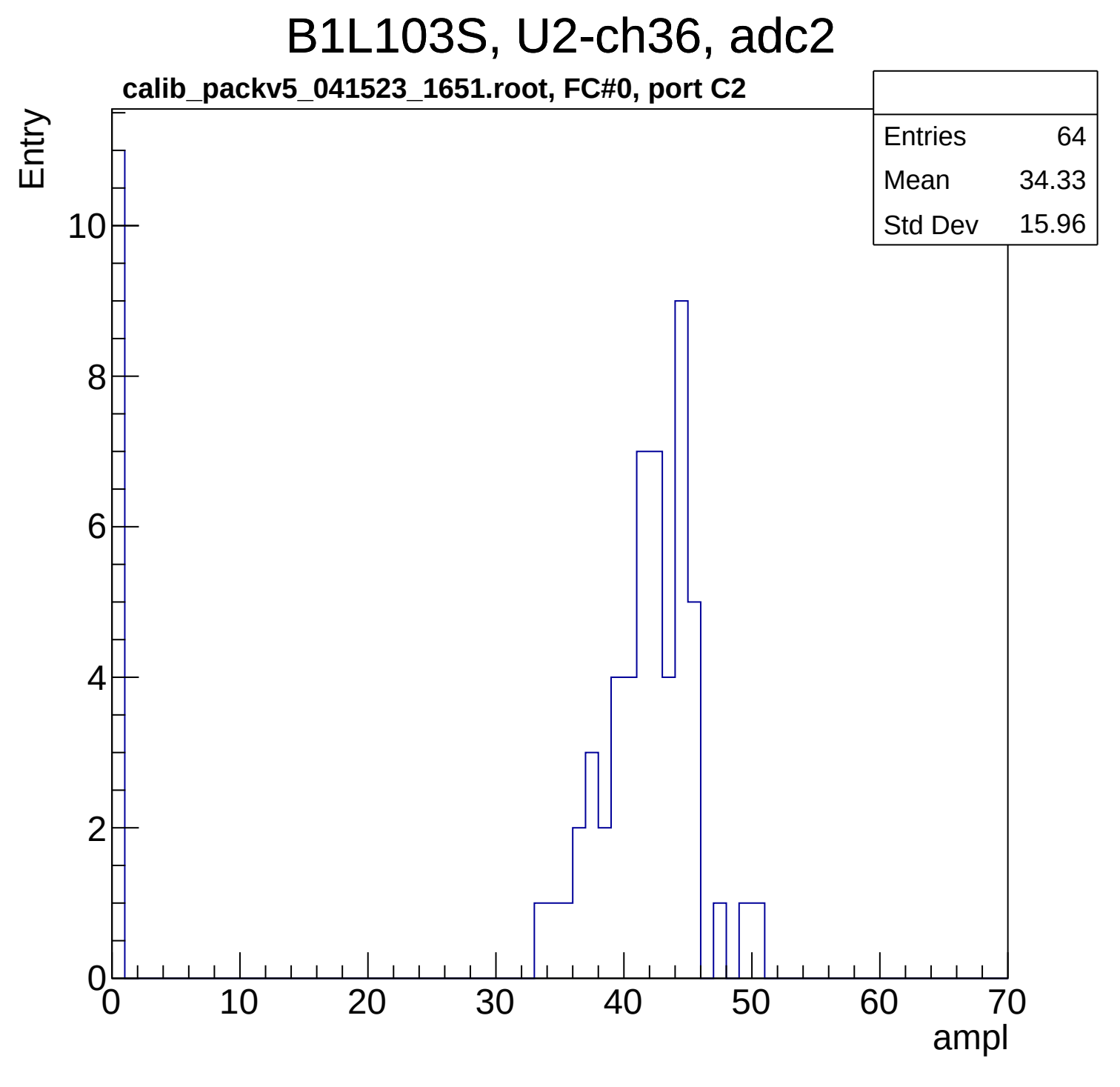

B1L103S, U2-ch35, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 59
Std Dev 2.625
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

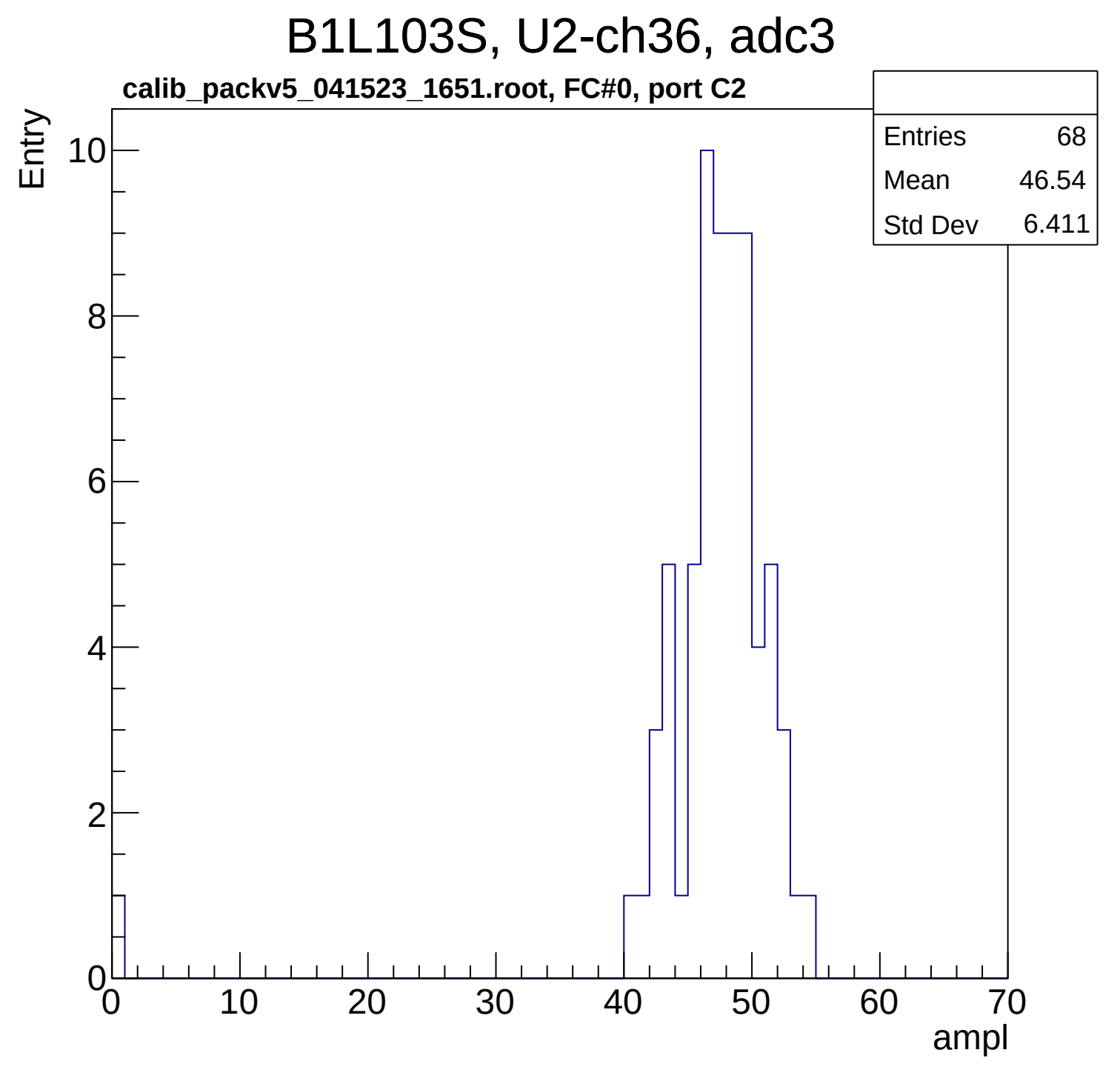

B1L103S, U2-ch35, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.83
Std Dev 1.404
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

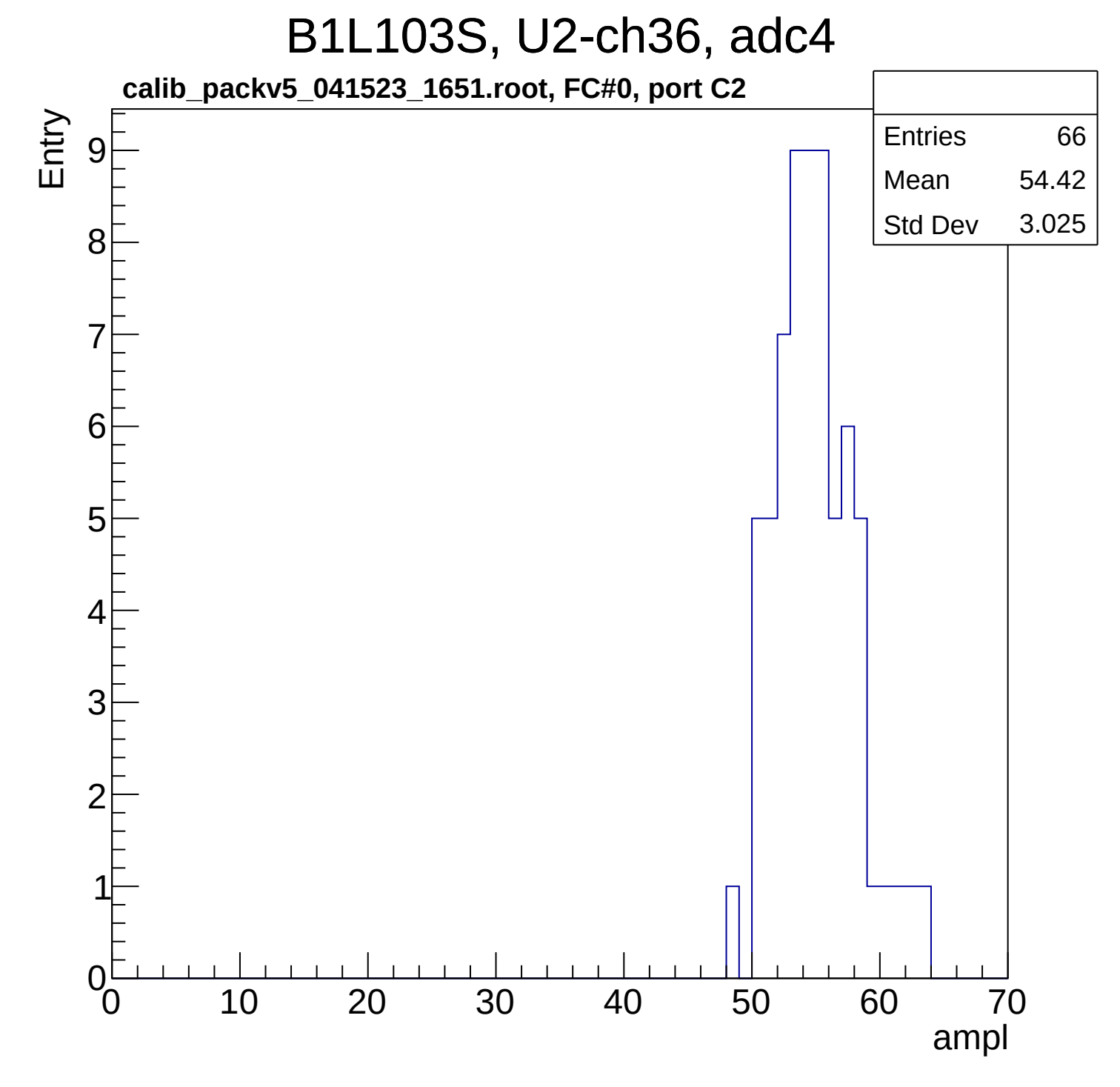

B1L103S, U2-ch35, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 1.05
Std Dev 4.577
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

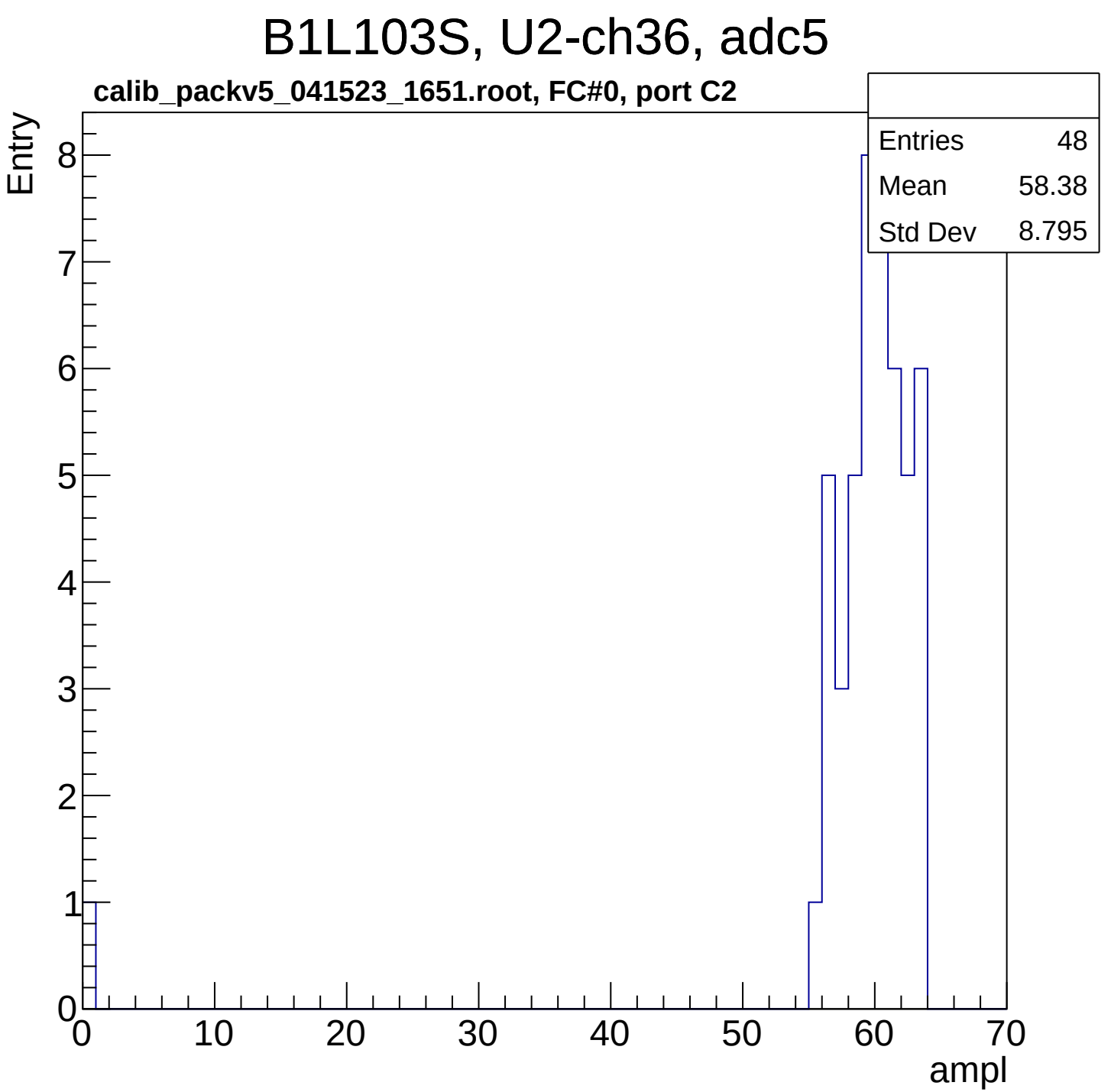

B1L103S, U2-ch36, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 17.95
Std Dev 13.95
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl

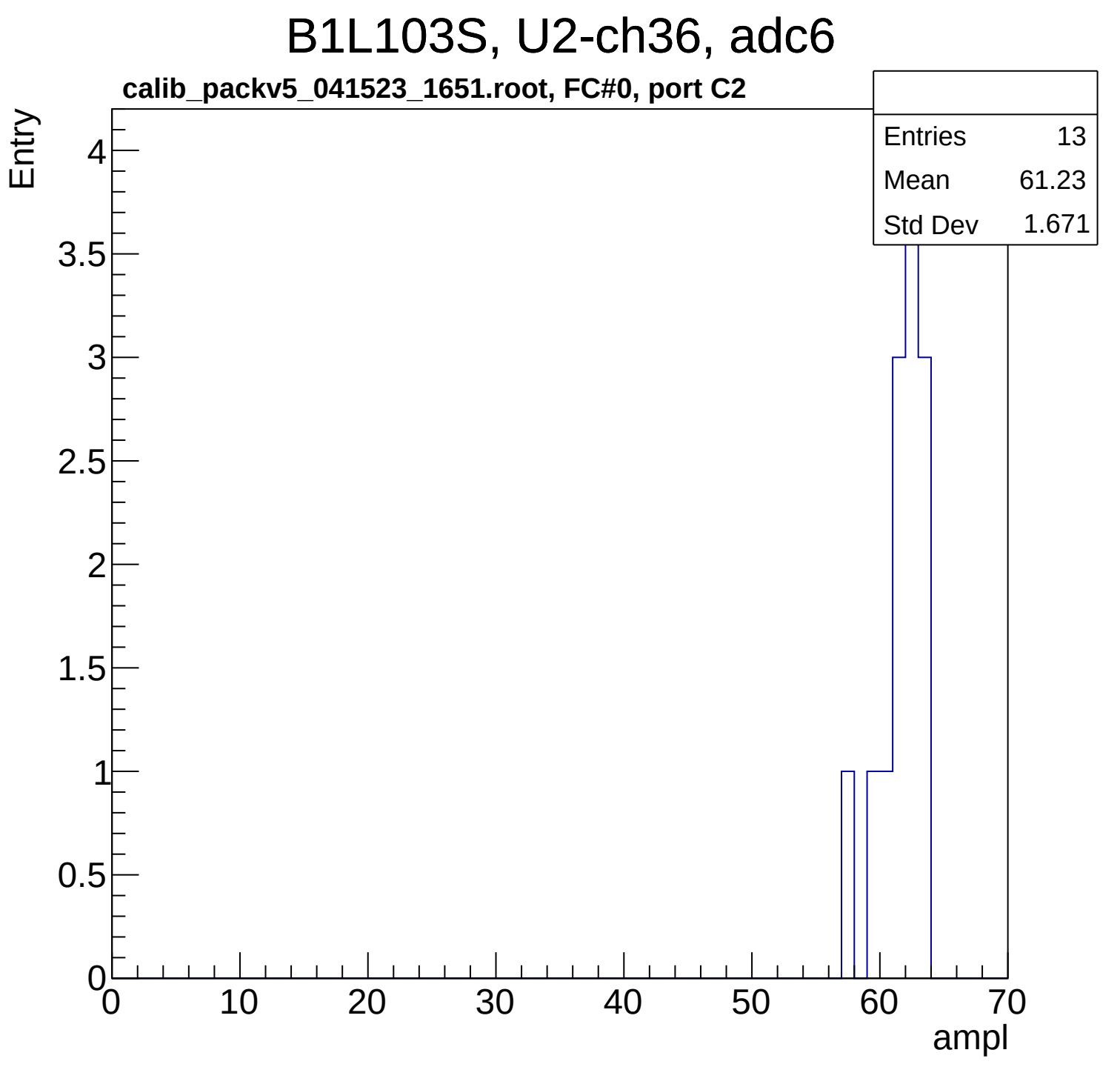

B1L103S, U2-ch36, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 31.1
Std Dev 11.48
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

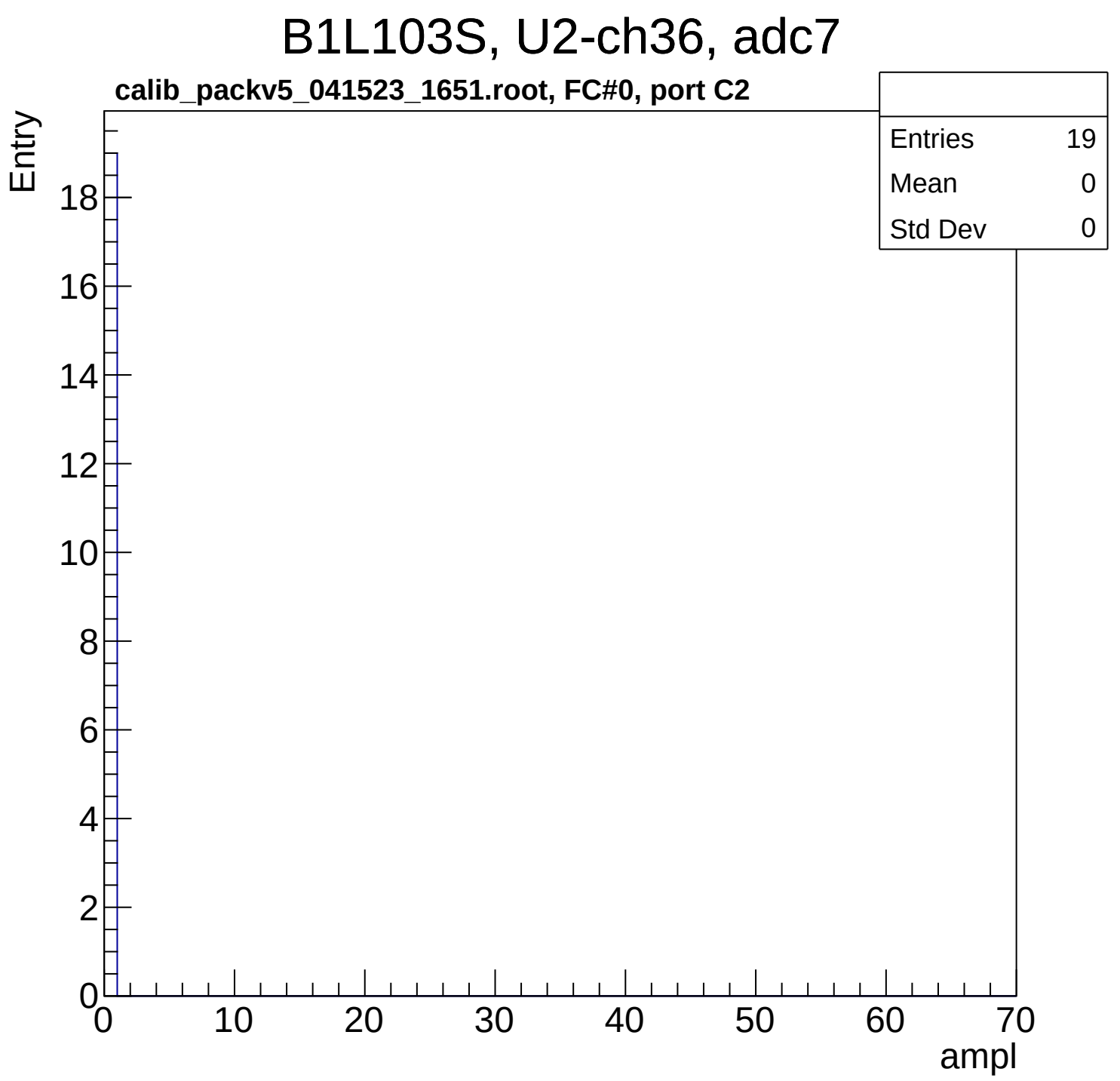

B1L103S, U2-ch36, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 34.33
Std Dev 15.96
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

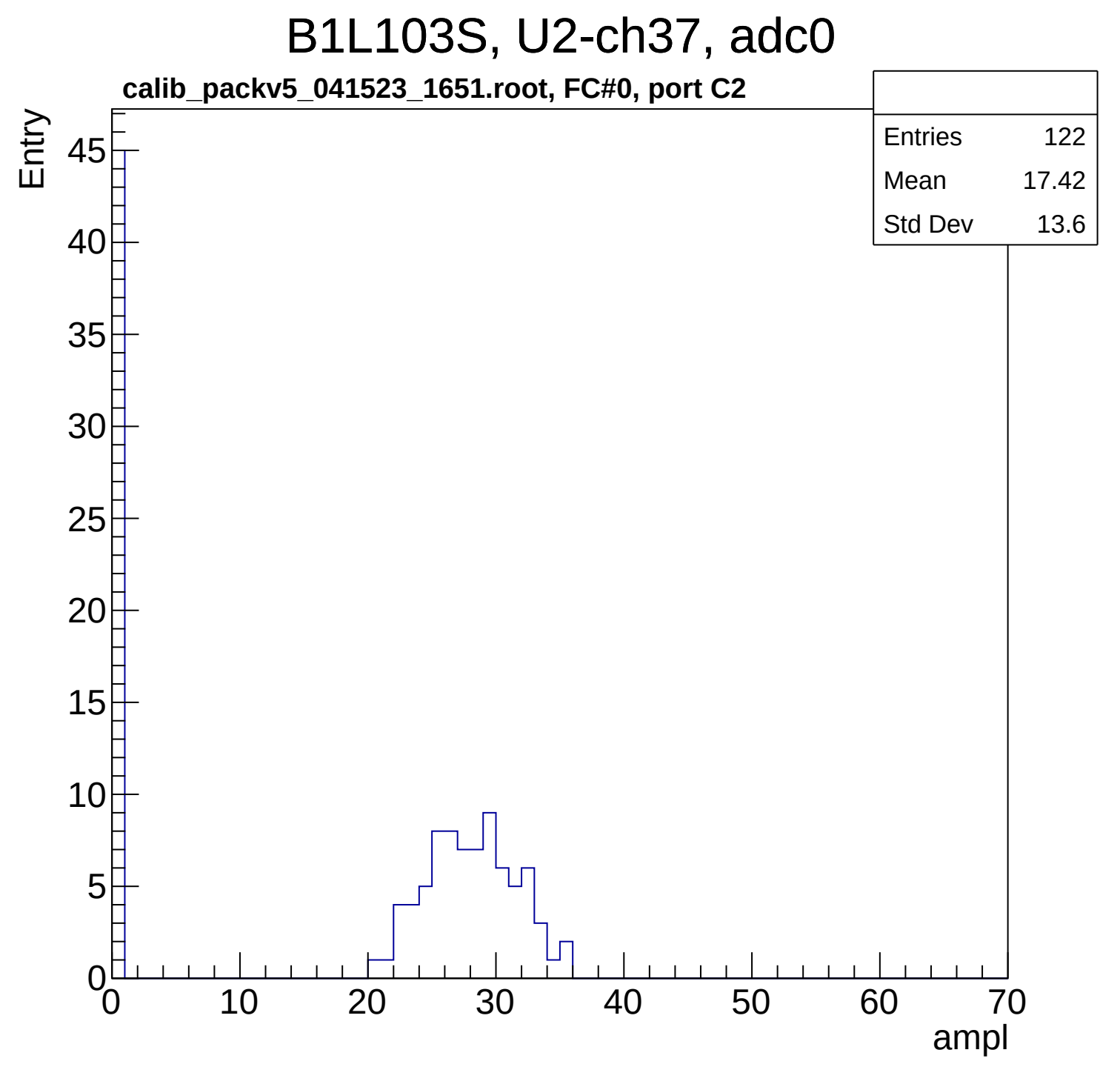

B1L103S, U2-ch36, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 46.54
Std Dev 6.411
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

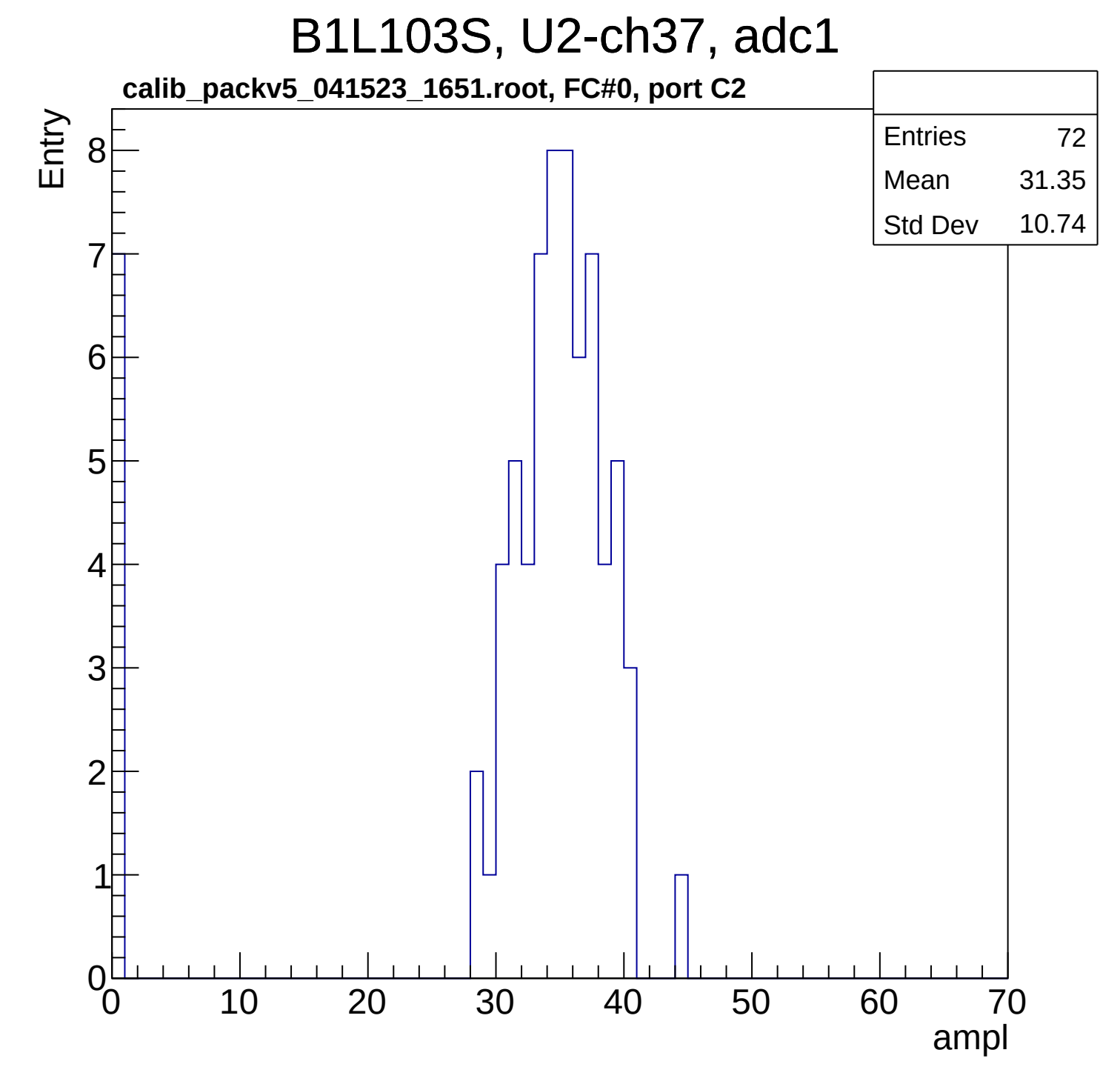

B1L103S, U2-ch36, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 54.42
Std Dev 3.025
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

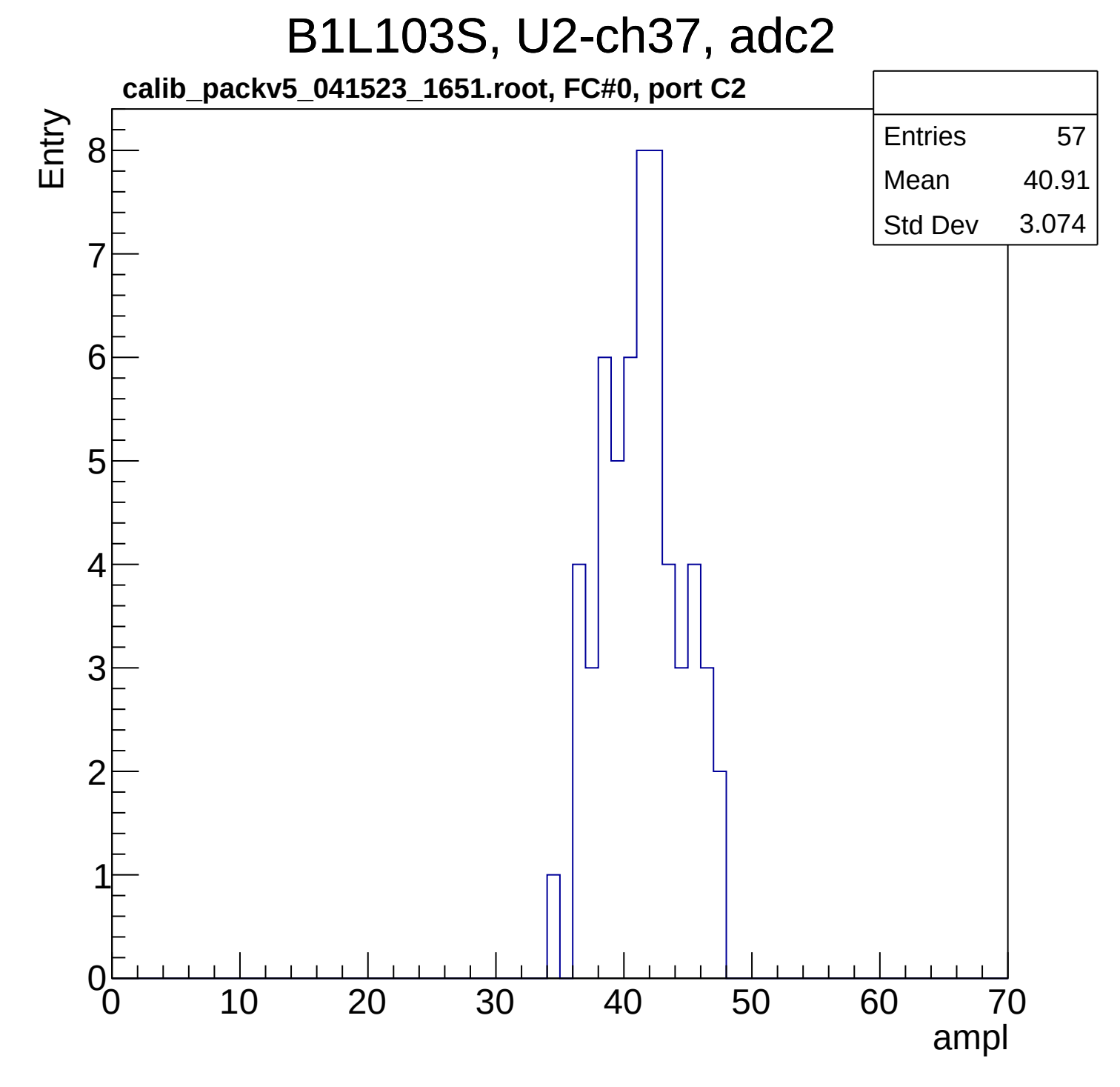

B1L103S, U2-ch36, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.38
Std Dev 8.795
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

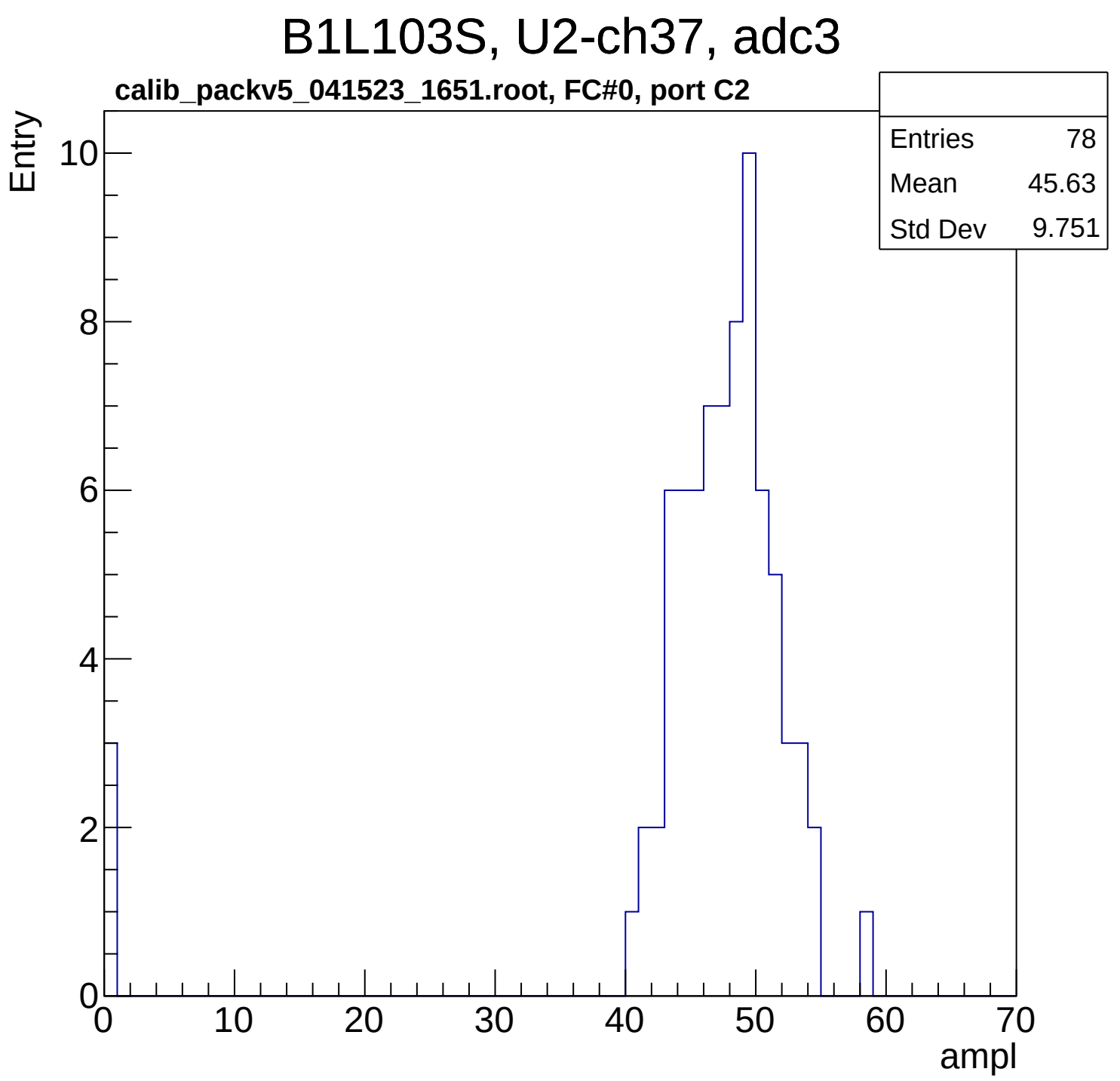

B1L103S, U2-ch36, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.23
Std Dev 1.671
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

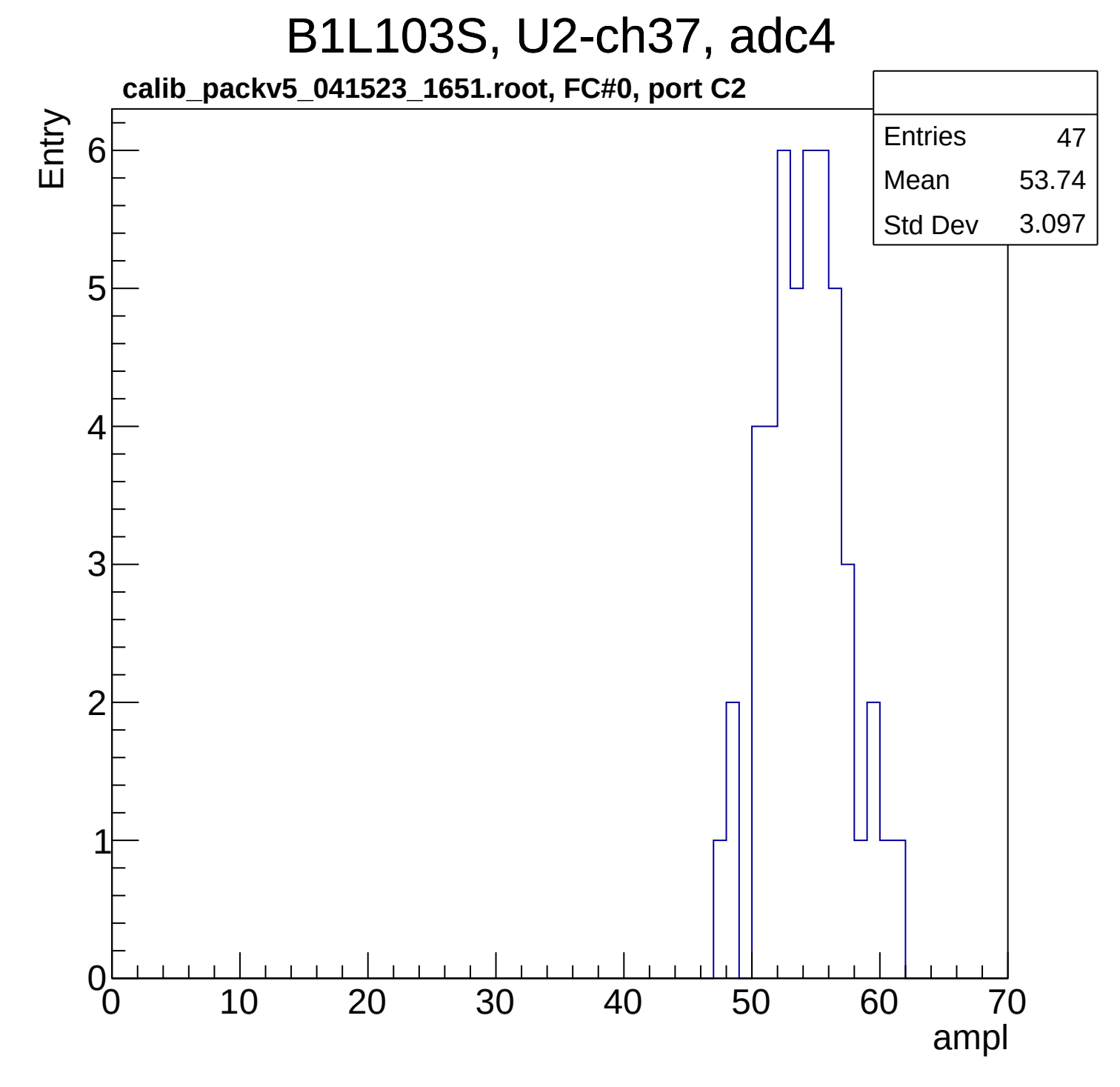

B1L103S, U2-ch36, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

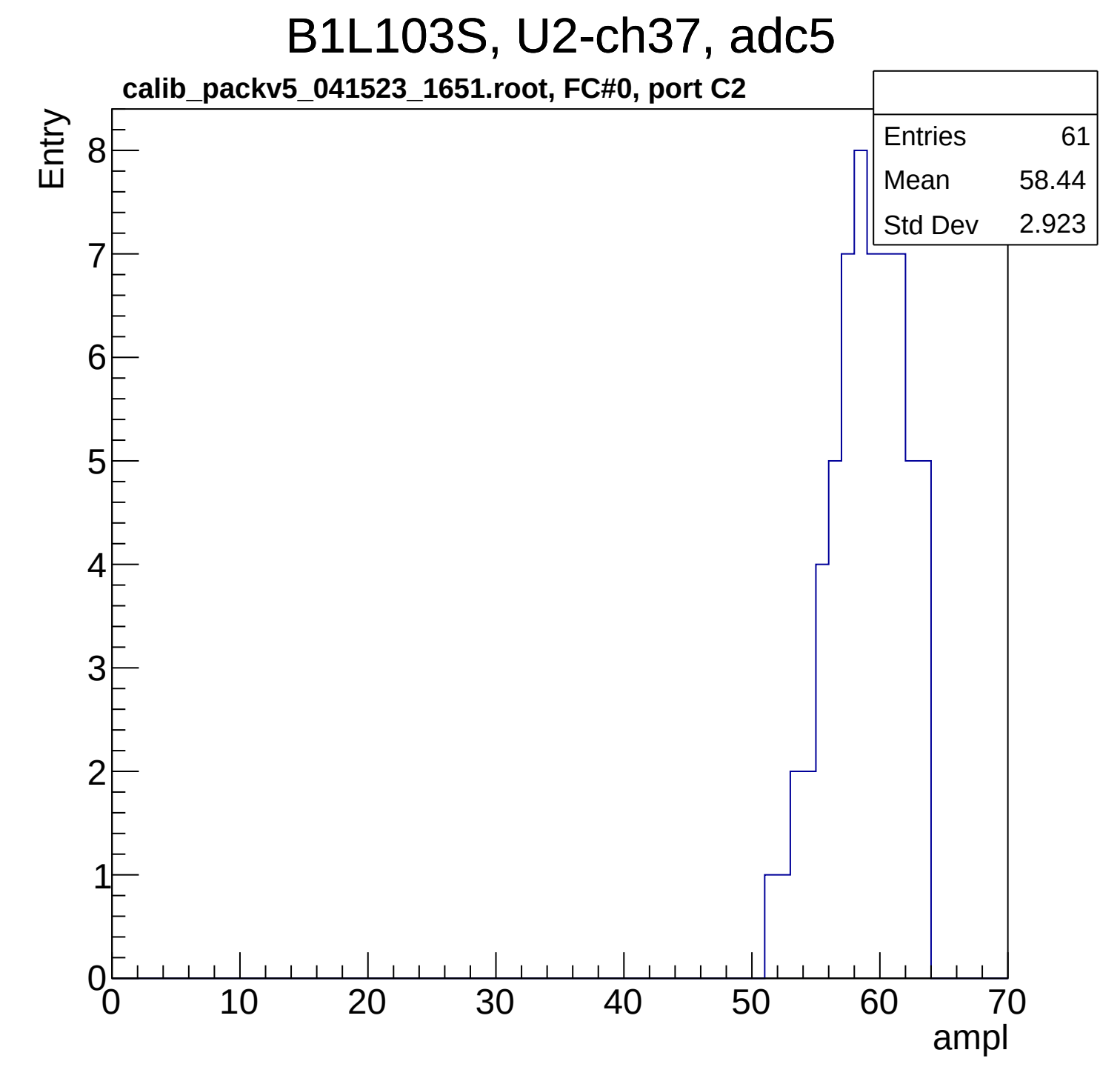

B1L103S, U2-ch37, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 122
Mean 17.42
Std Dev 13.6
Entry
0
5
10
15
20
25
30
35
40
45
0
10
20
30
40
50
60
70
ampl

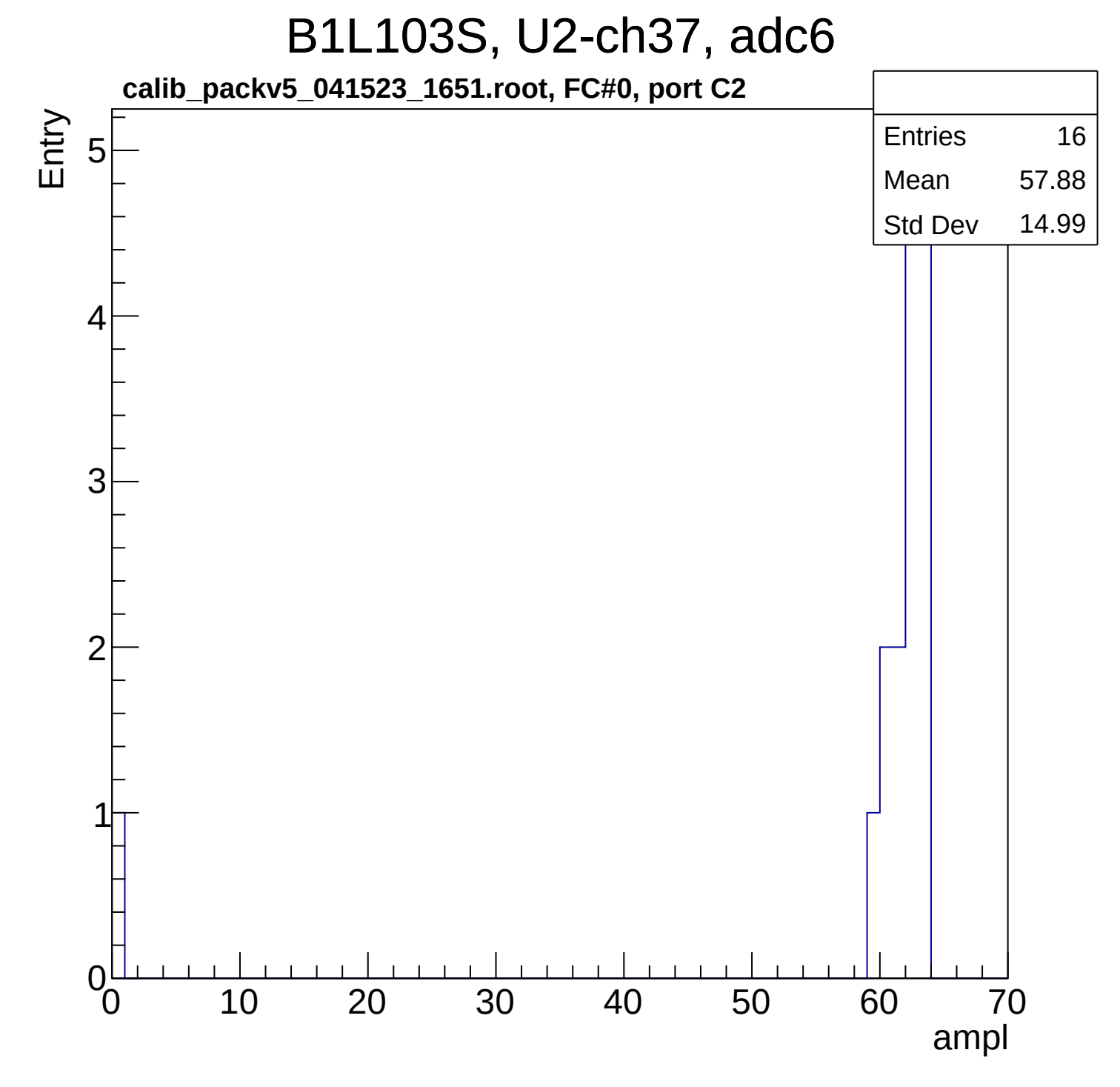

B1L103S, U2-ch37, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 31.35
Std Dev 10.74
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

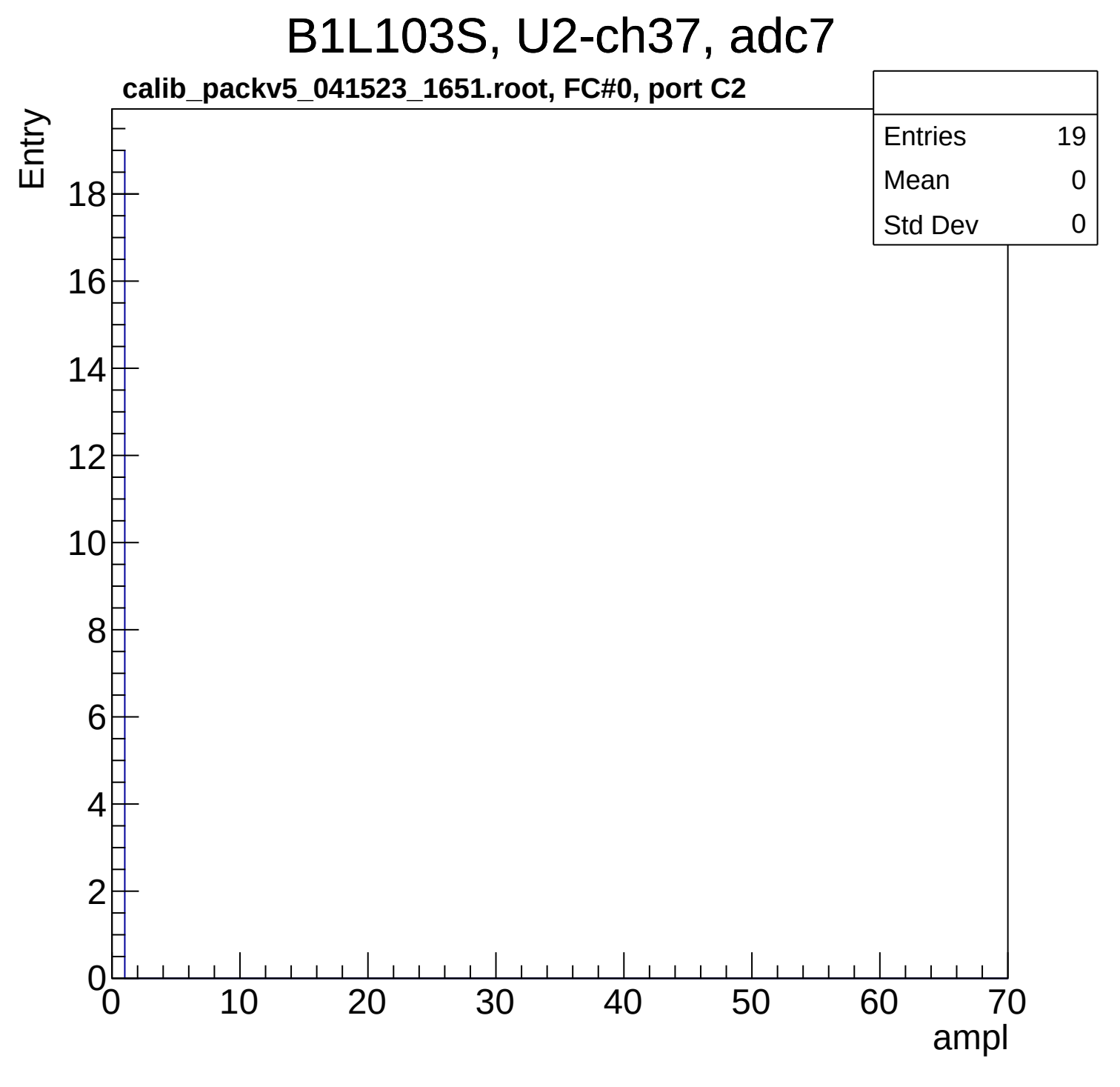

B1L103S, U2-ch37, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 40.91
Std Dev 3.074
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

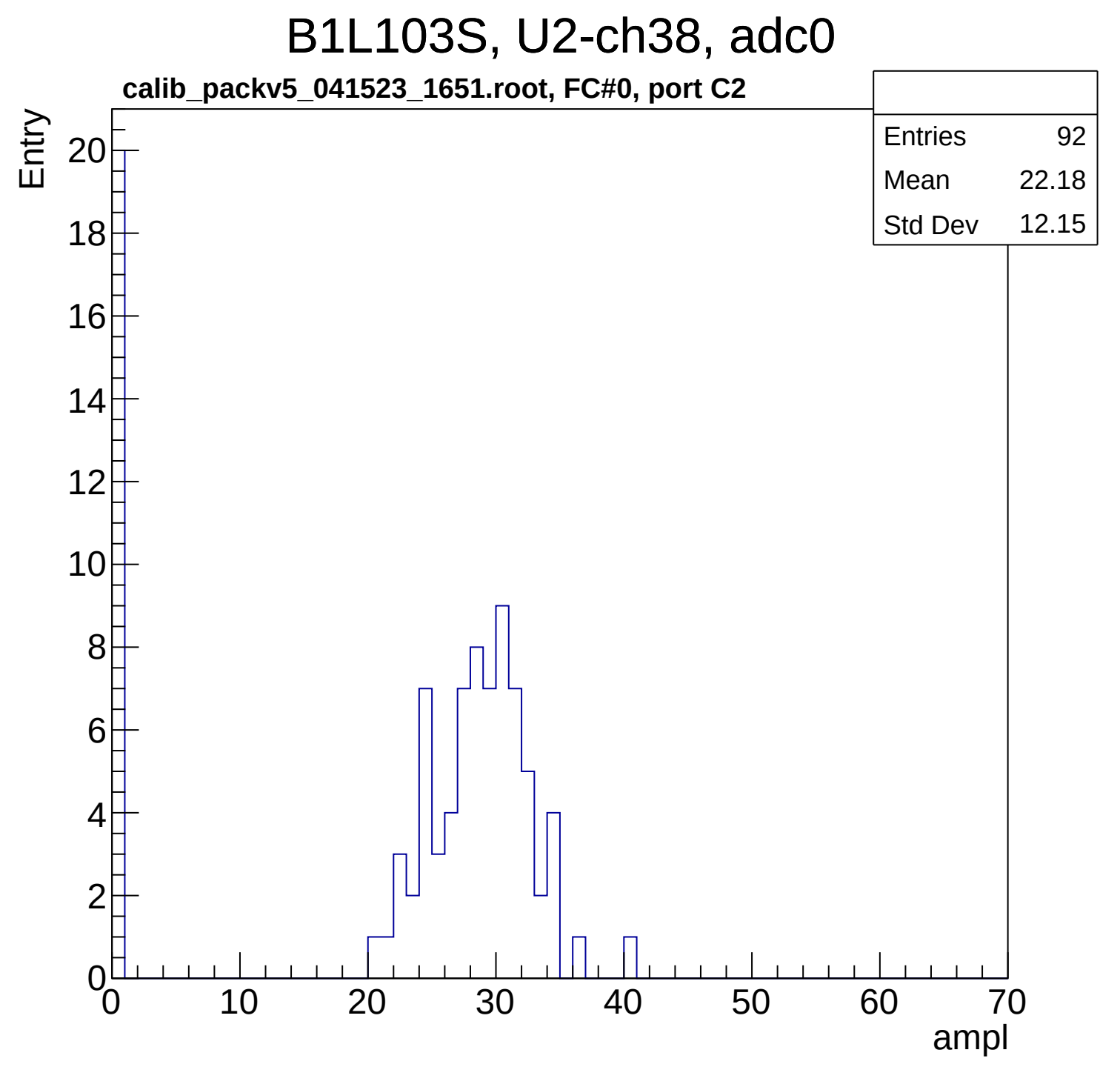

B1L103S, U2-ch37, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 45.63
Std Dev 9.751
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

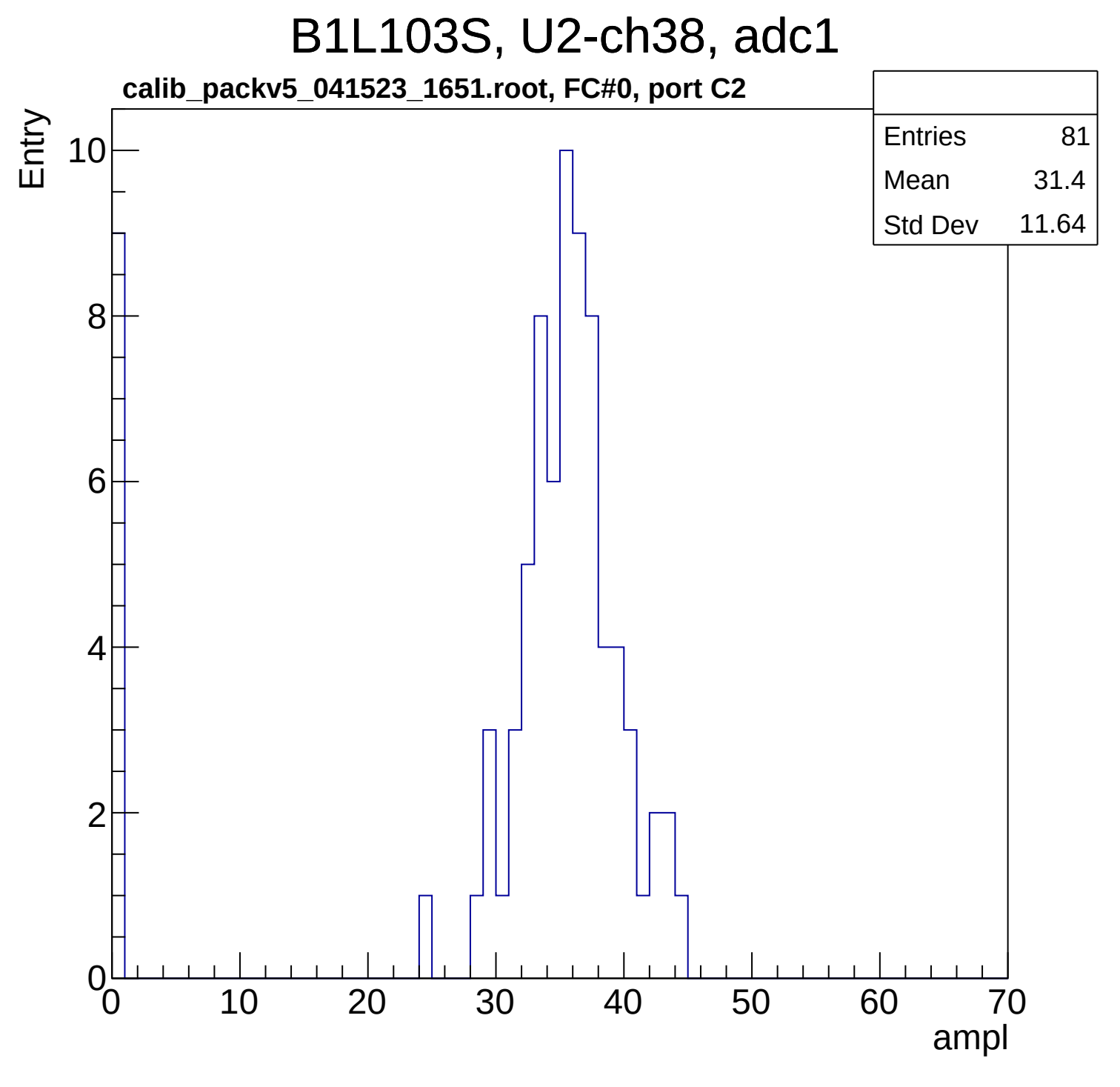

B1L103S, U2-ch37, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 53.74
Std Dev 3.097
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

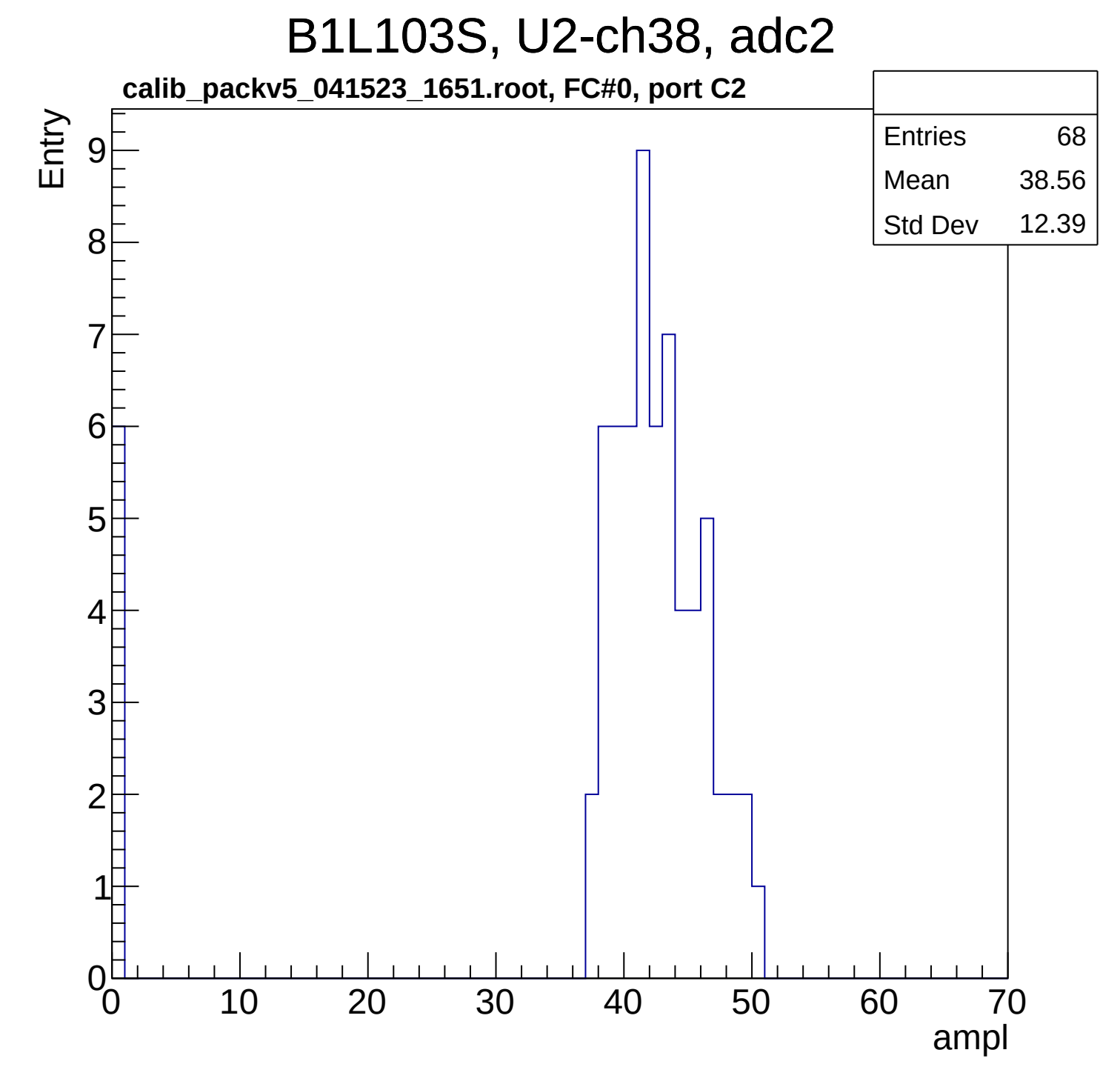

B1L103S, U2-ch37, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 58.44
Std Dev 2.923
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

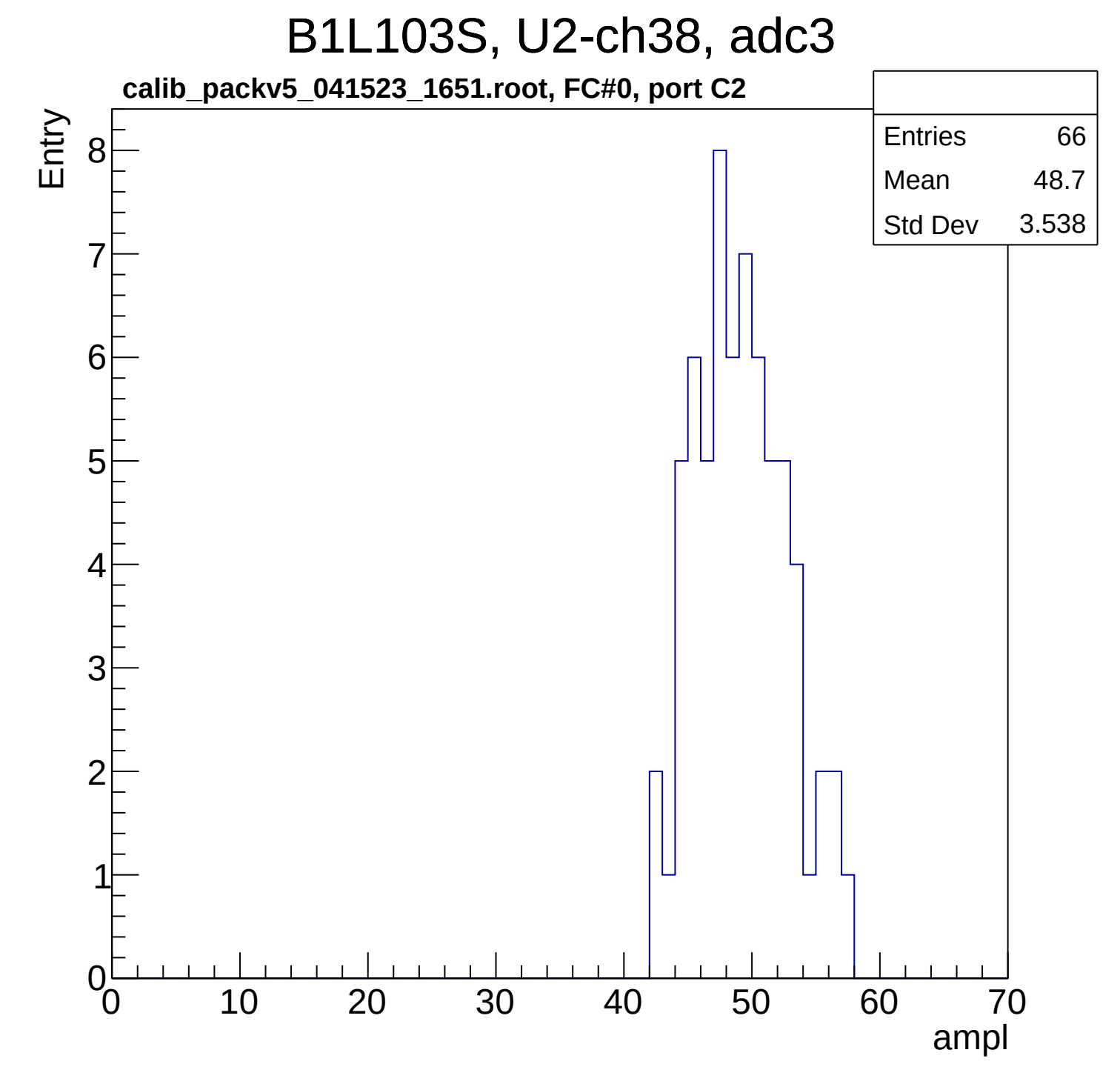

B1L103S, U2-ch37, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.88
Std Dev 14.99
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

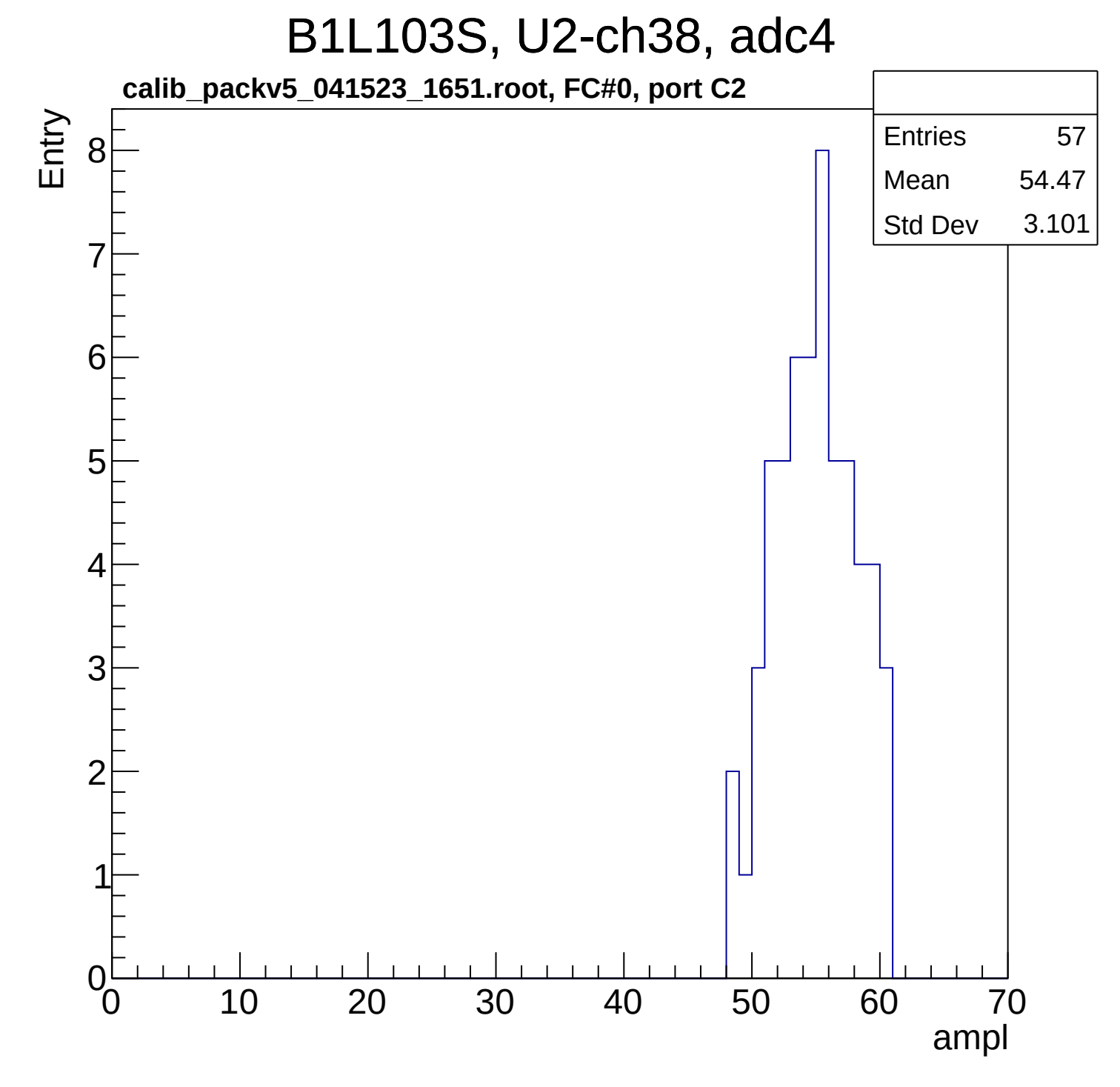

B1L103S, U2-ch37, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

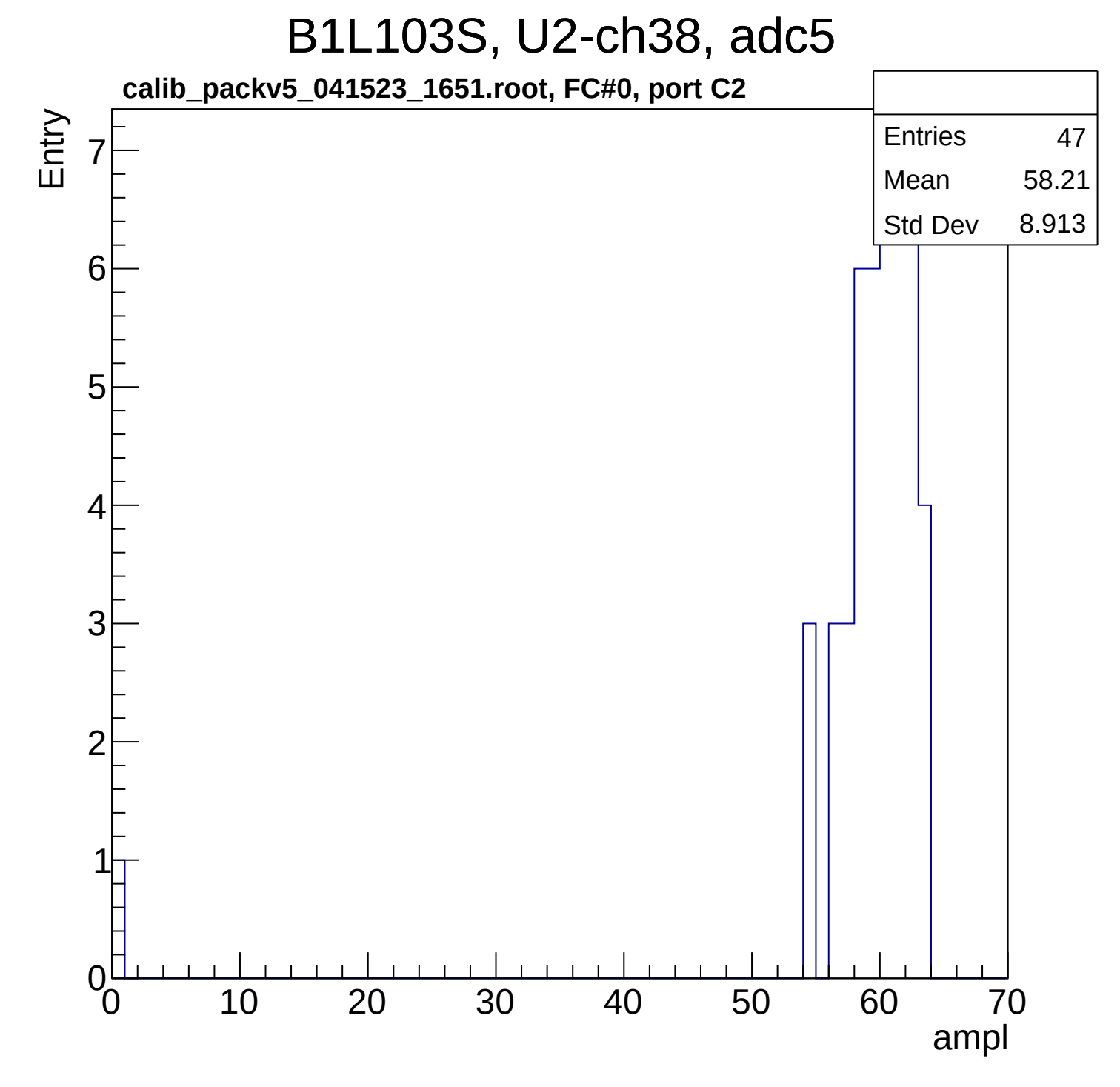

B1L103S, U2-ch38, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 22.18
Std Dev 12.15
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

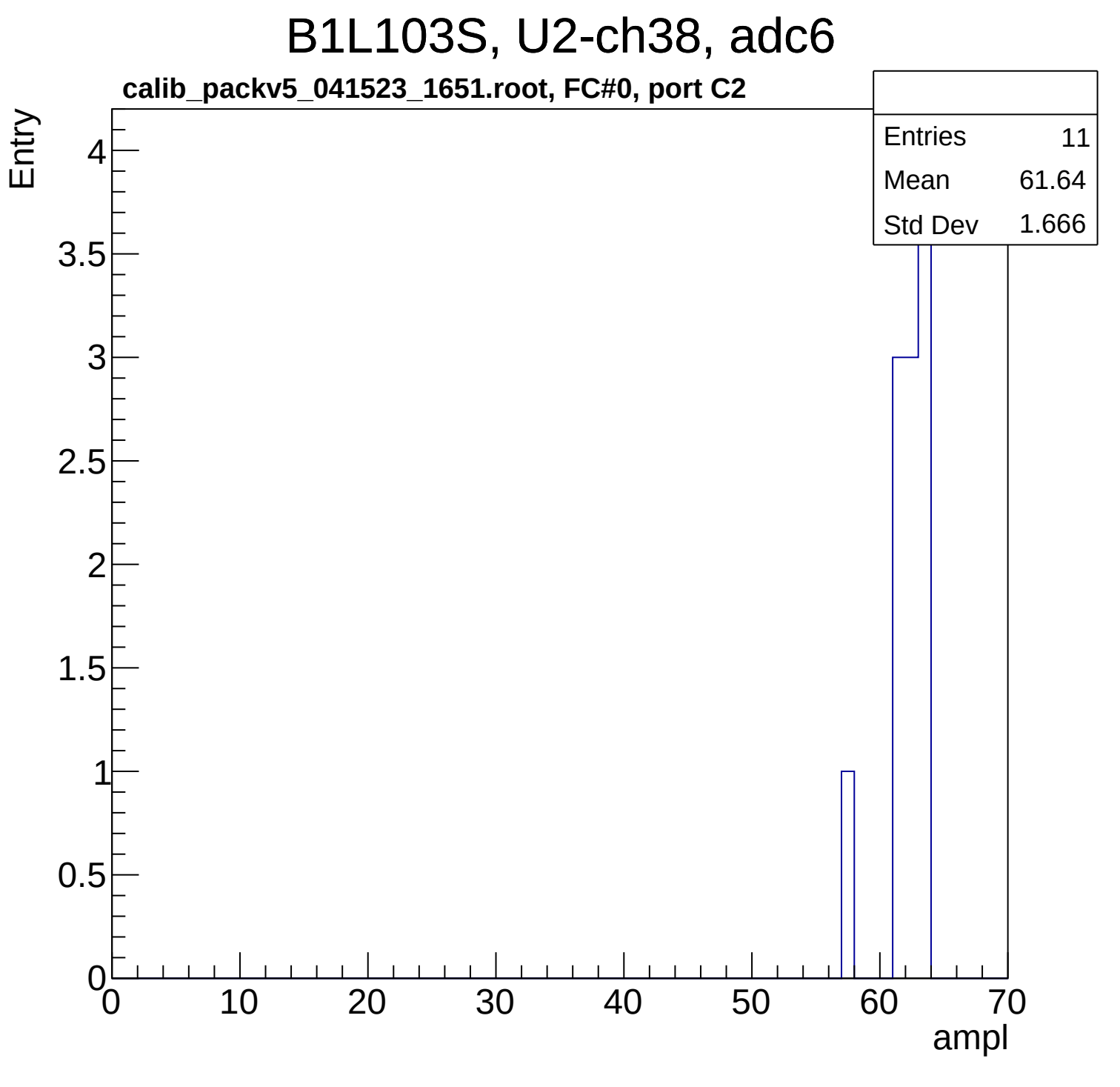

B1L103S, U2-ch38, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 31.4
Std Dev 11.64
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

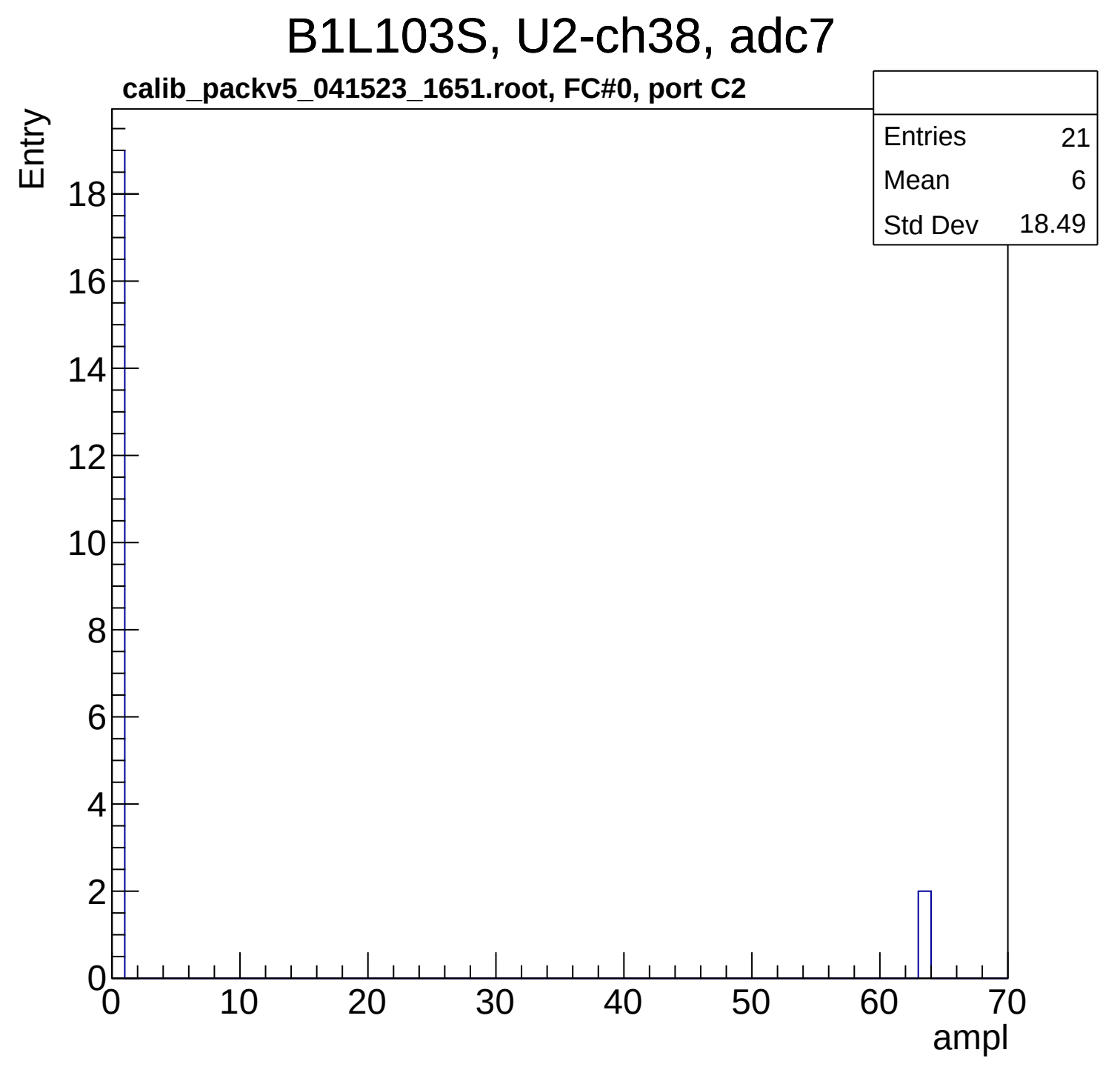

B1L103S, U2-ch38, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 38.56
Std Dev 12.39
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

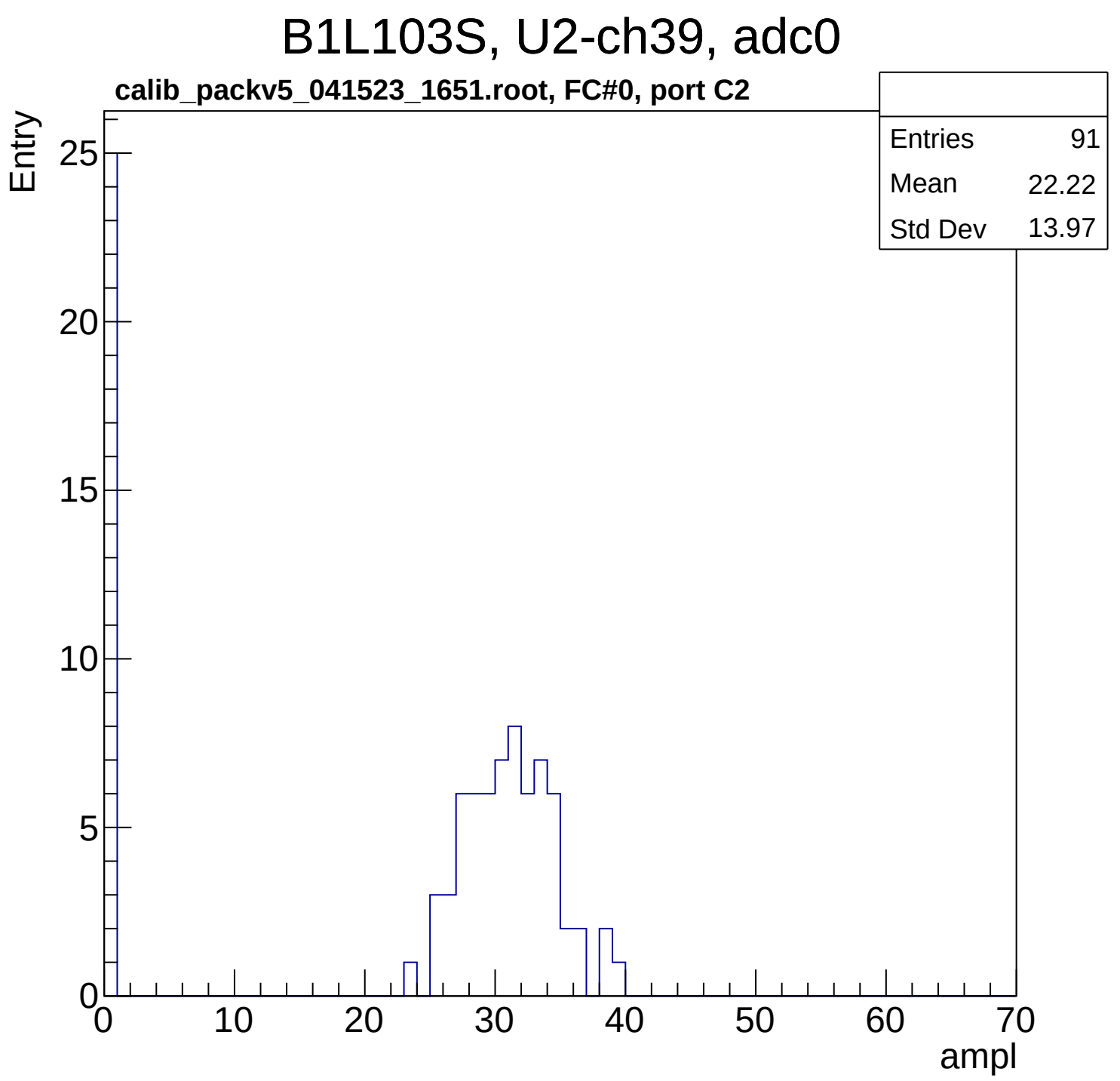

B1L103S, U2-ch38, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 48.7
Std Dev 3.538
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

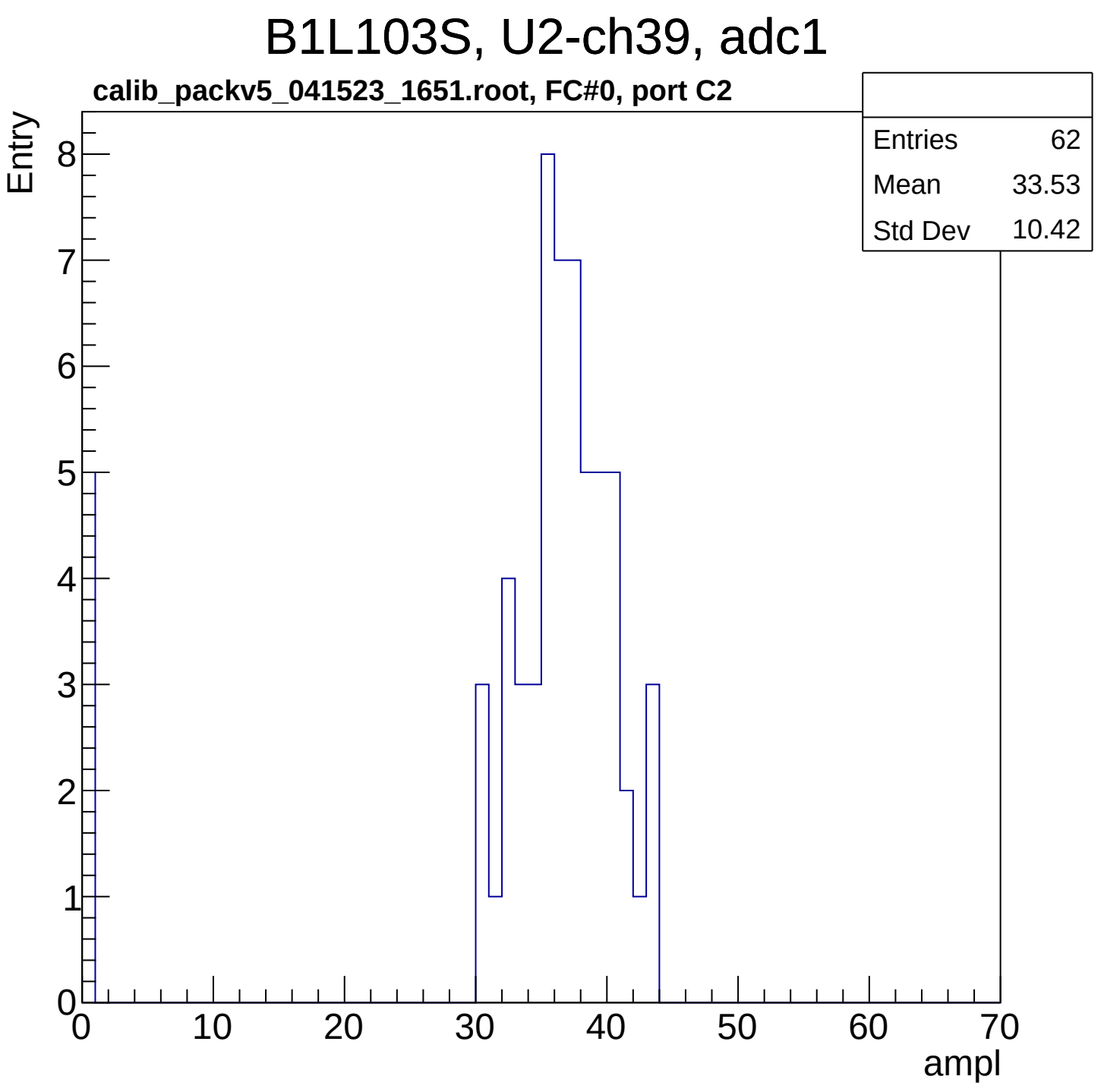

B1L103S, U2-ch38, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 54.47
Std Dev 3.101
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

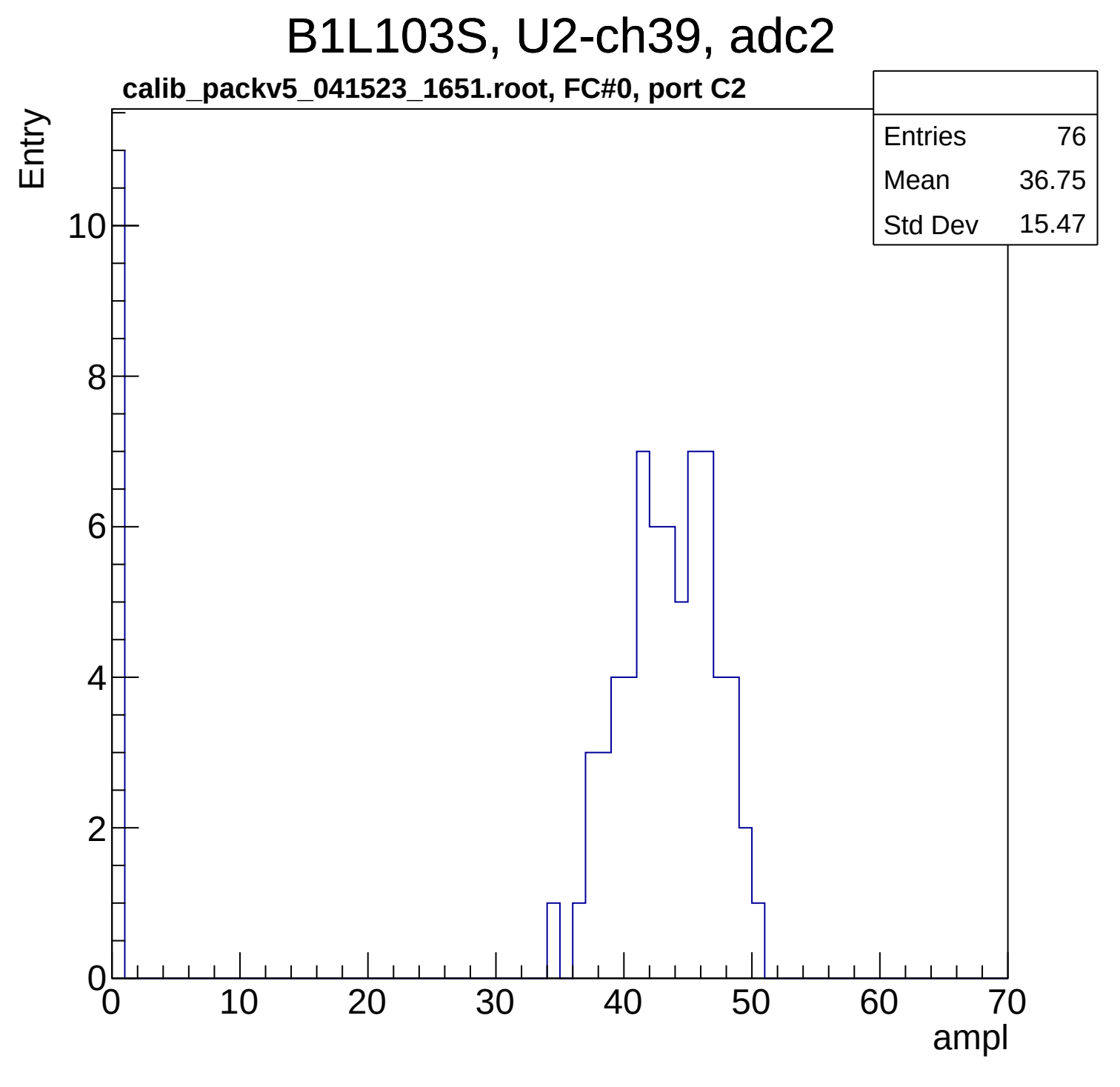

B1L103S, U2-ch38, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.21
Std Dev 8.913
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

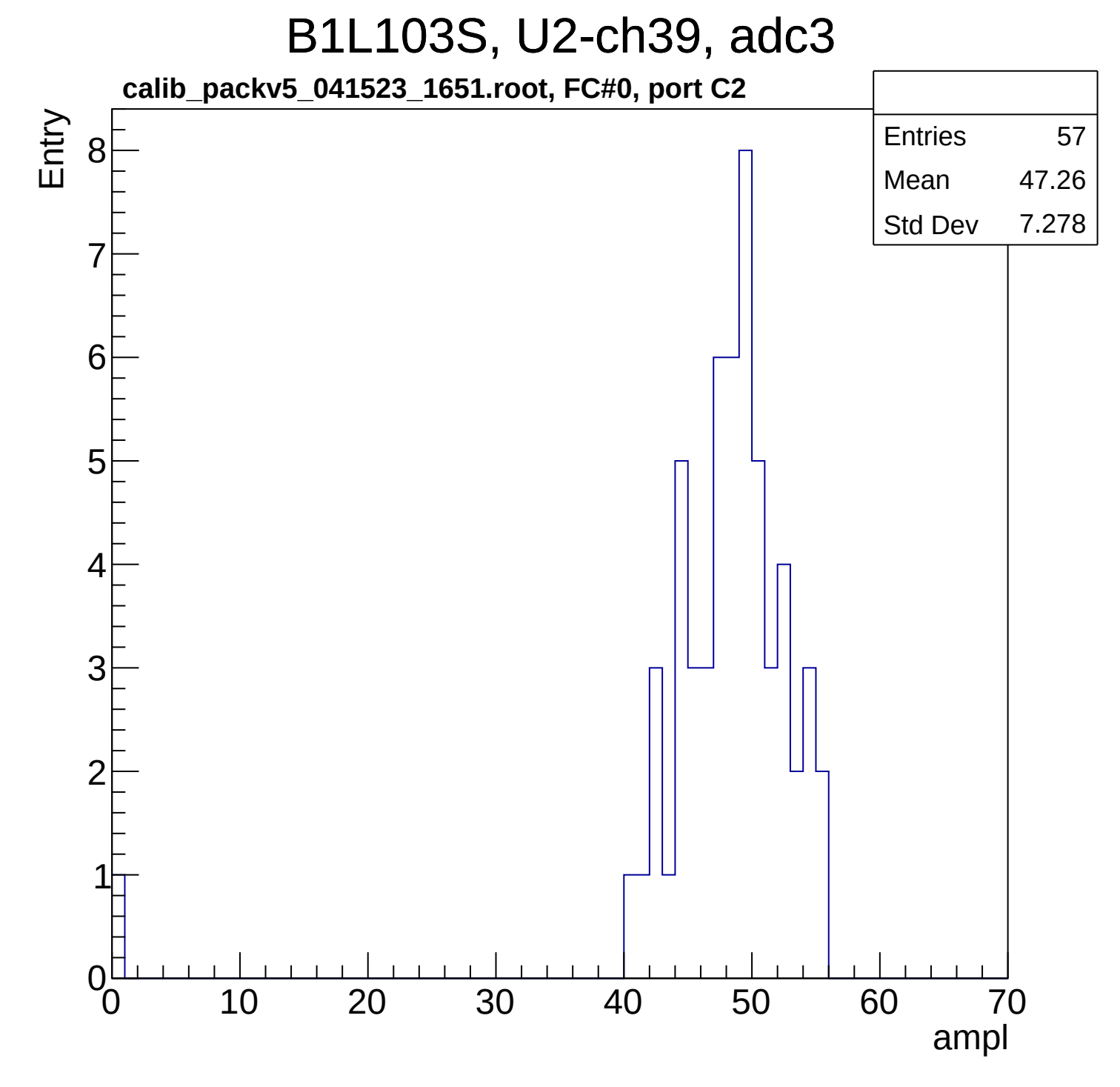

B1L103S, U2-ch38, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.64
Std Dev 1.666
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

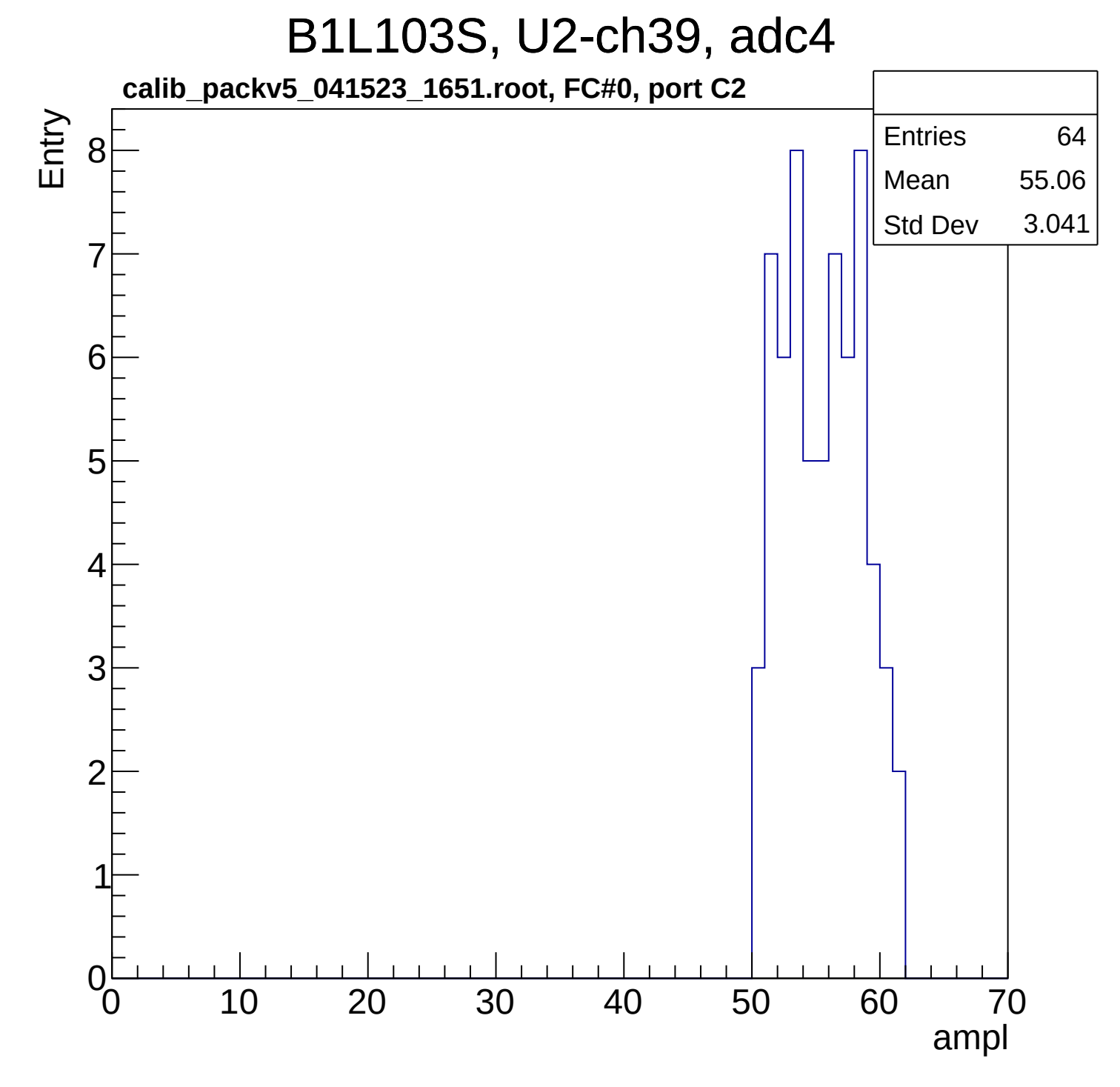

B1L103S, U2-ch38, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

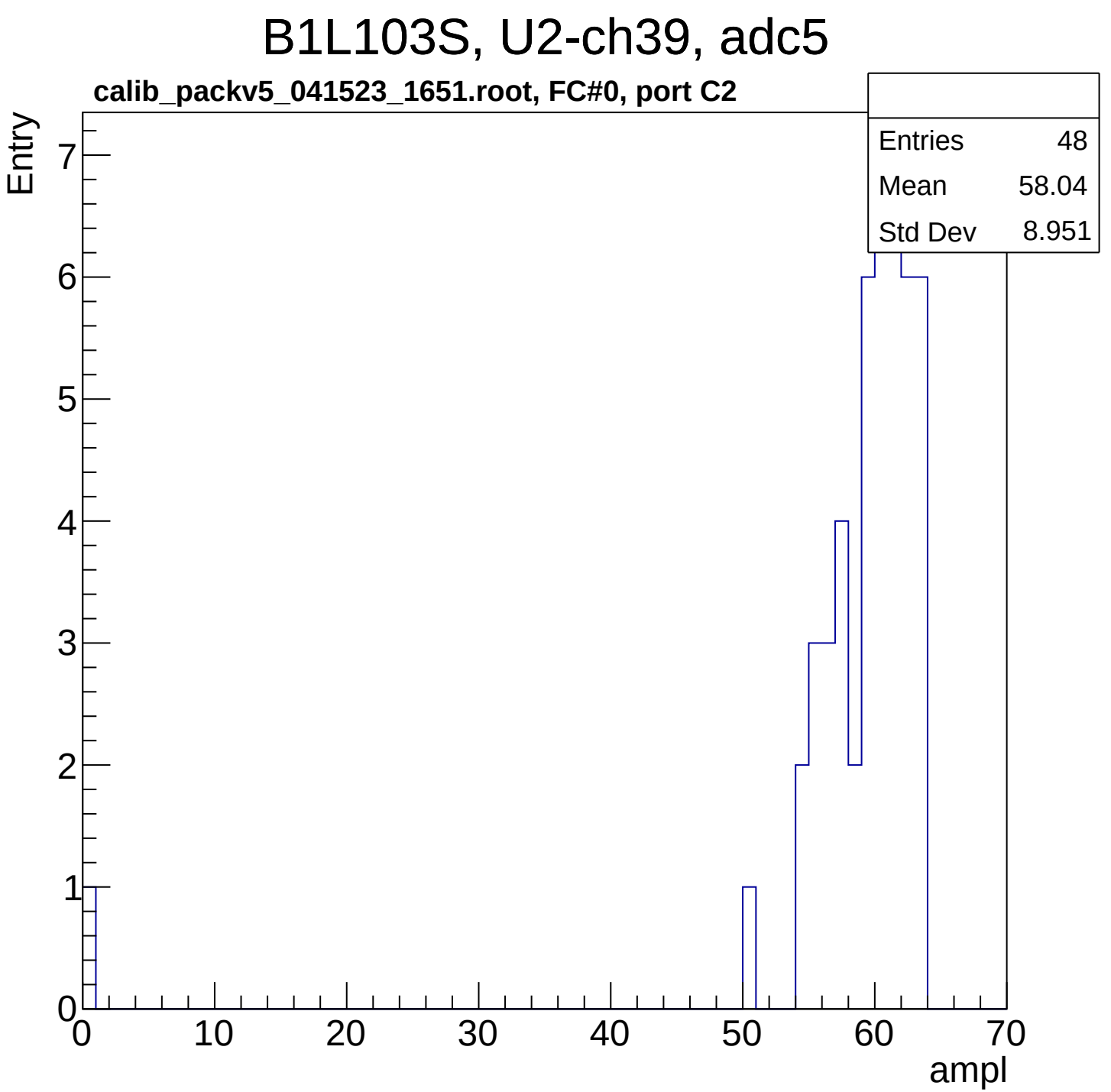

B1L103S, U2-ch39, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 22.22
Std Dev 13.97
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl

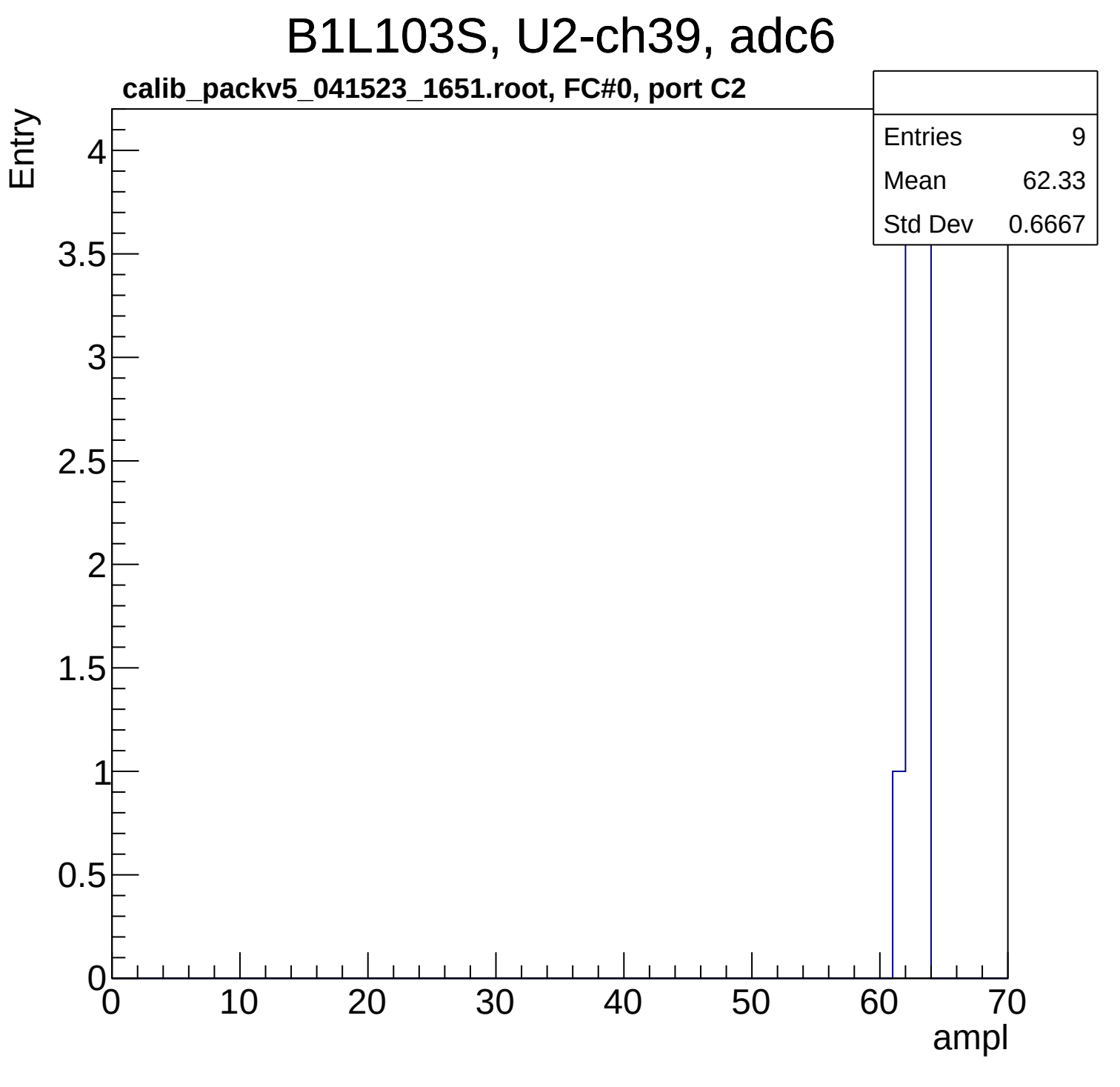

B1L103S, U2-ch39, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 33.53
Std Dev 10.42
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

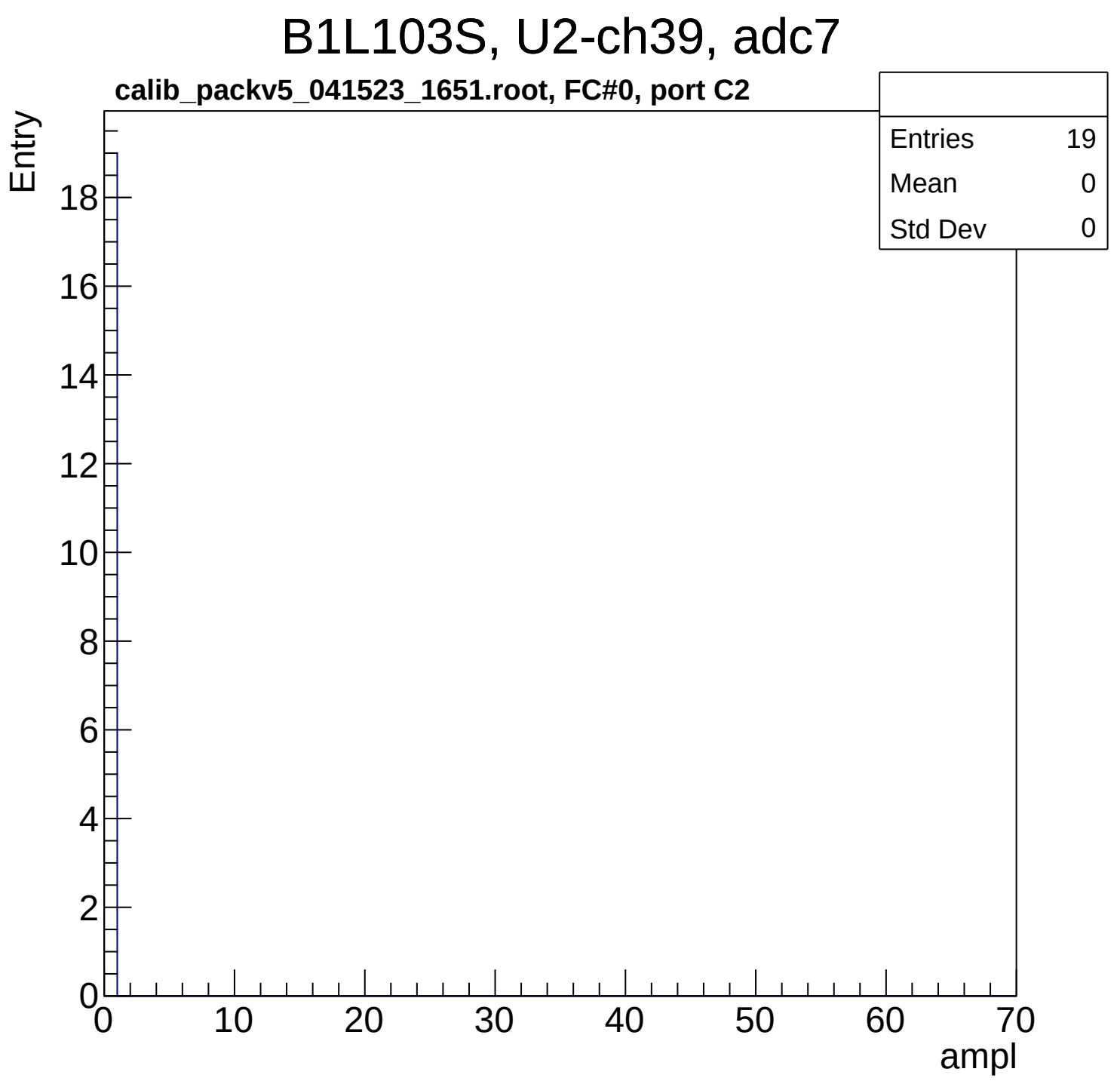

B1L103S, U2-ch39, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 36.75
Std Dev 15.47
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

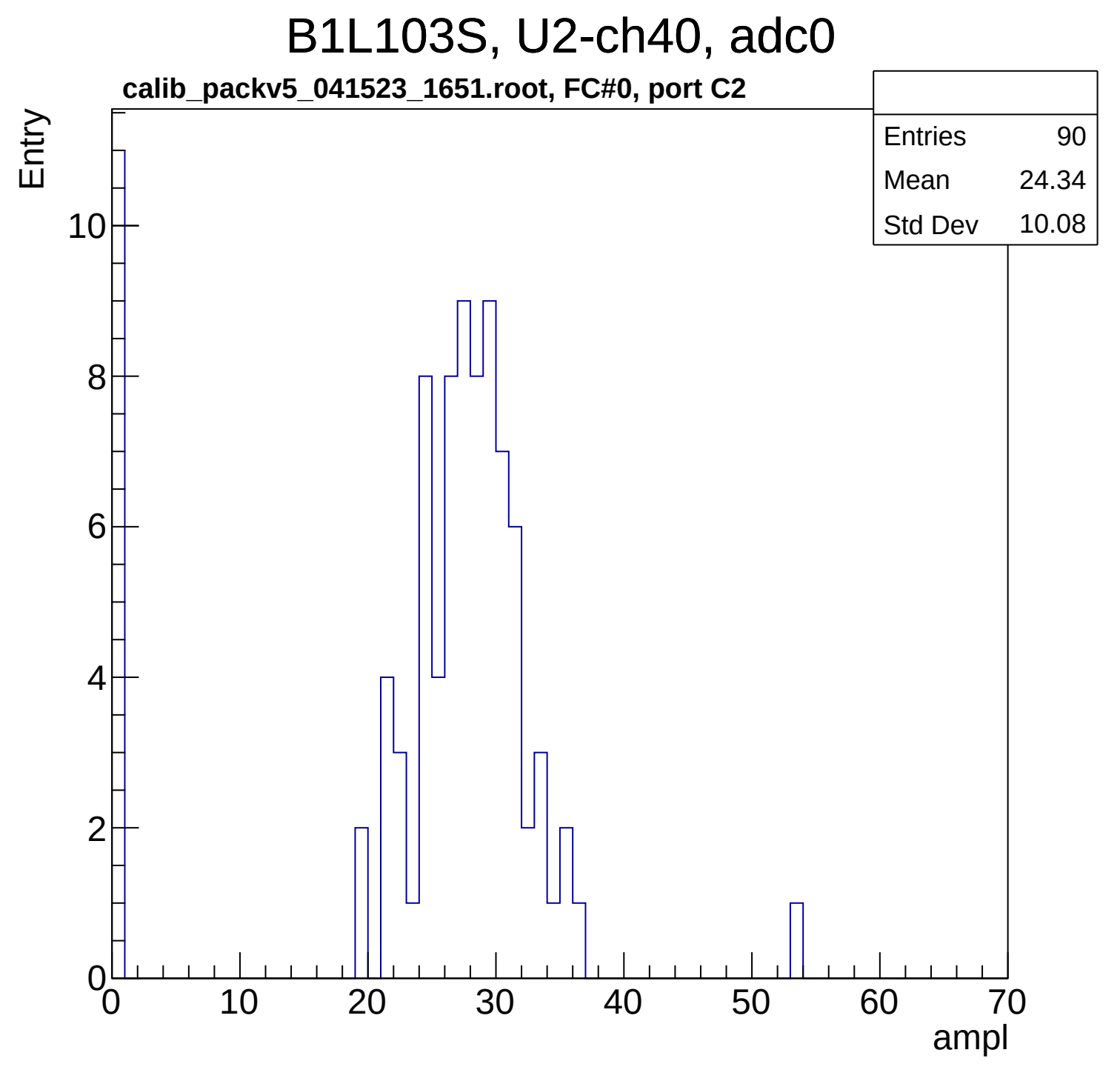

B1L103S, U2-ch39, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 47.26
Std Dev 7.278
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

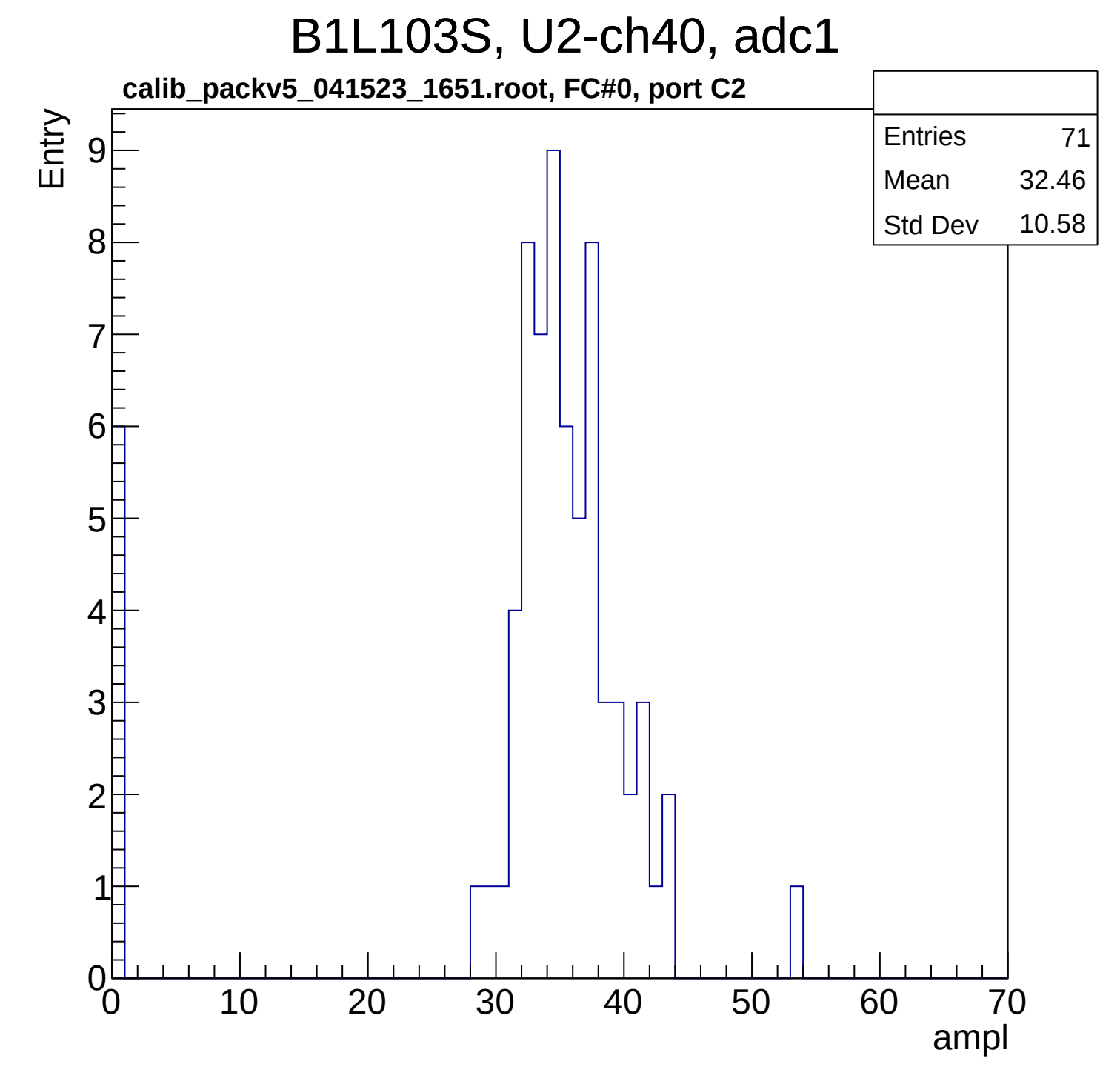

B1L103S, U2-ch39, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 55.06
Std Dev 3.041
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

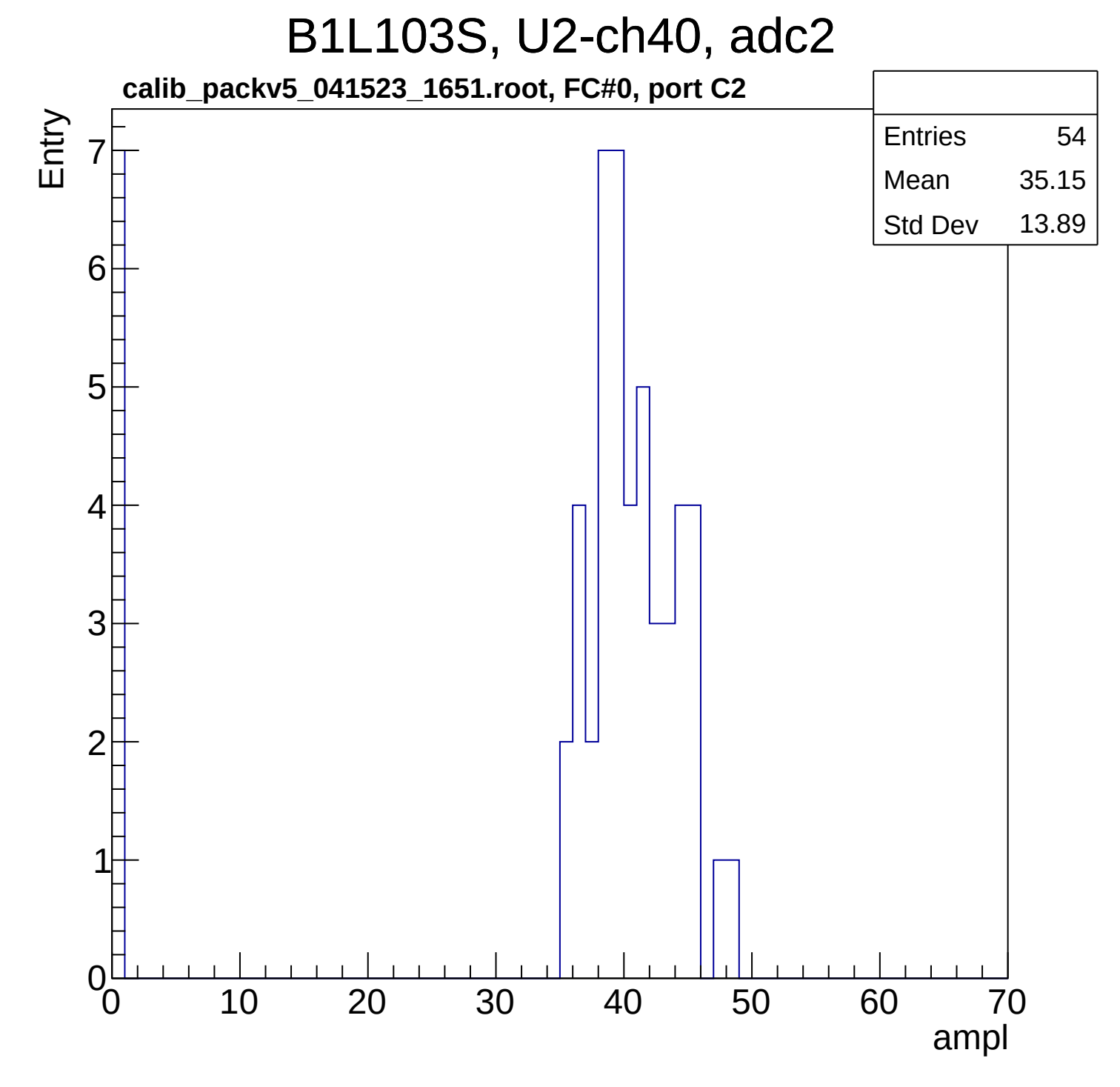

B1L103S, U2-ch39, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.04
Std Dev 8.951
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

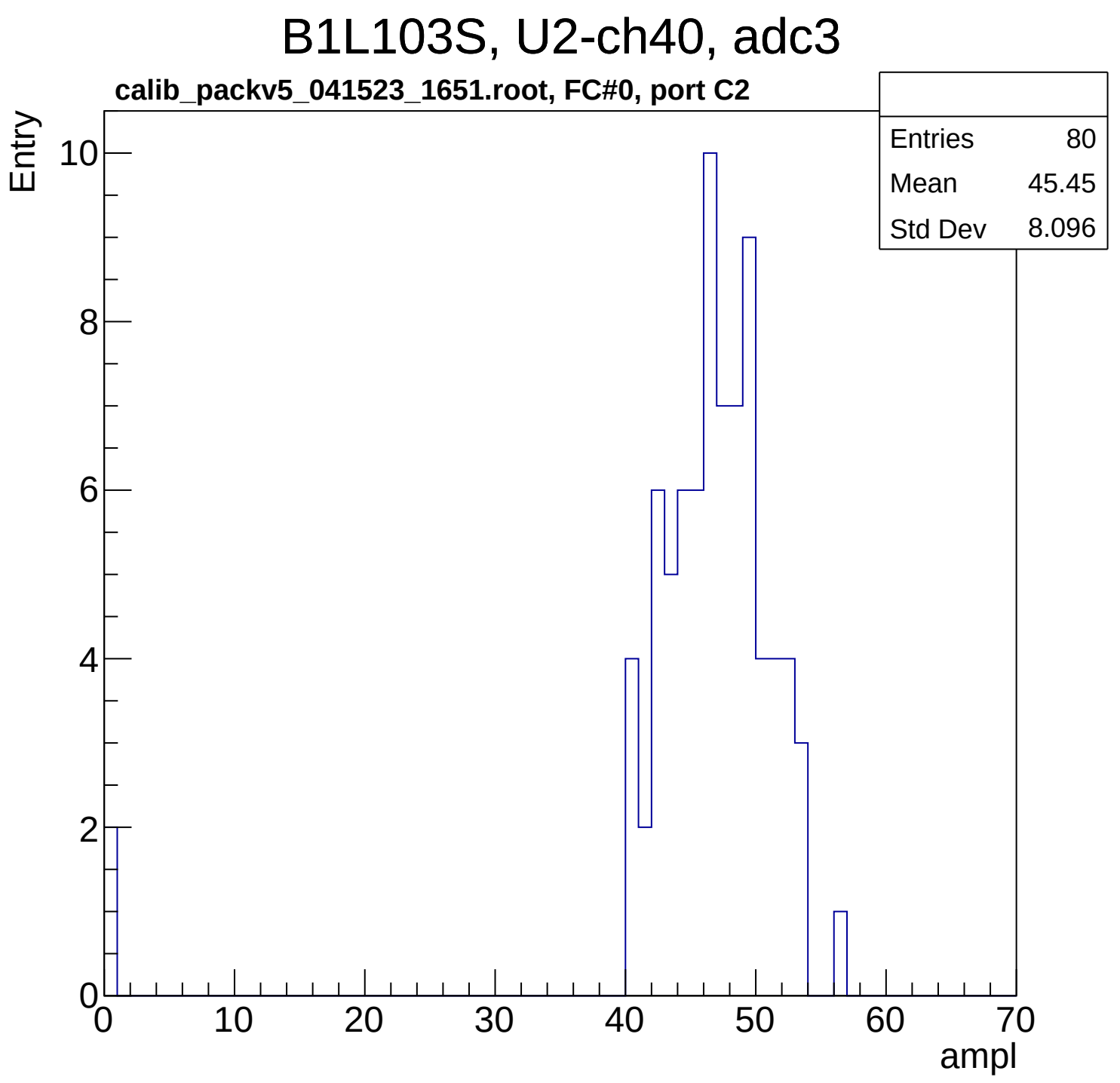

B1L103S, U2-ch39, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 62.33
Std Dev 0.6667
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

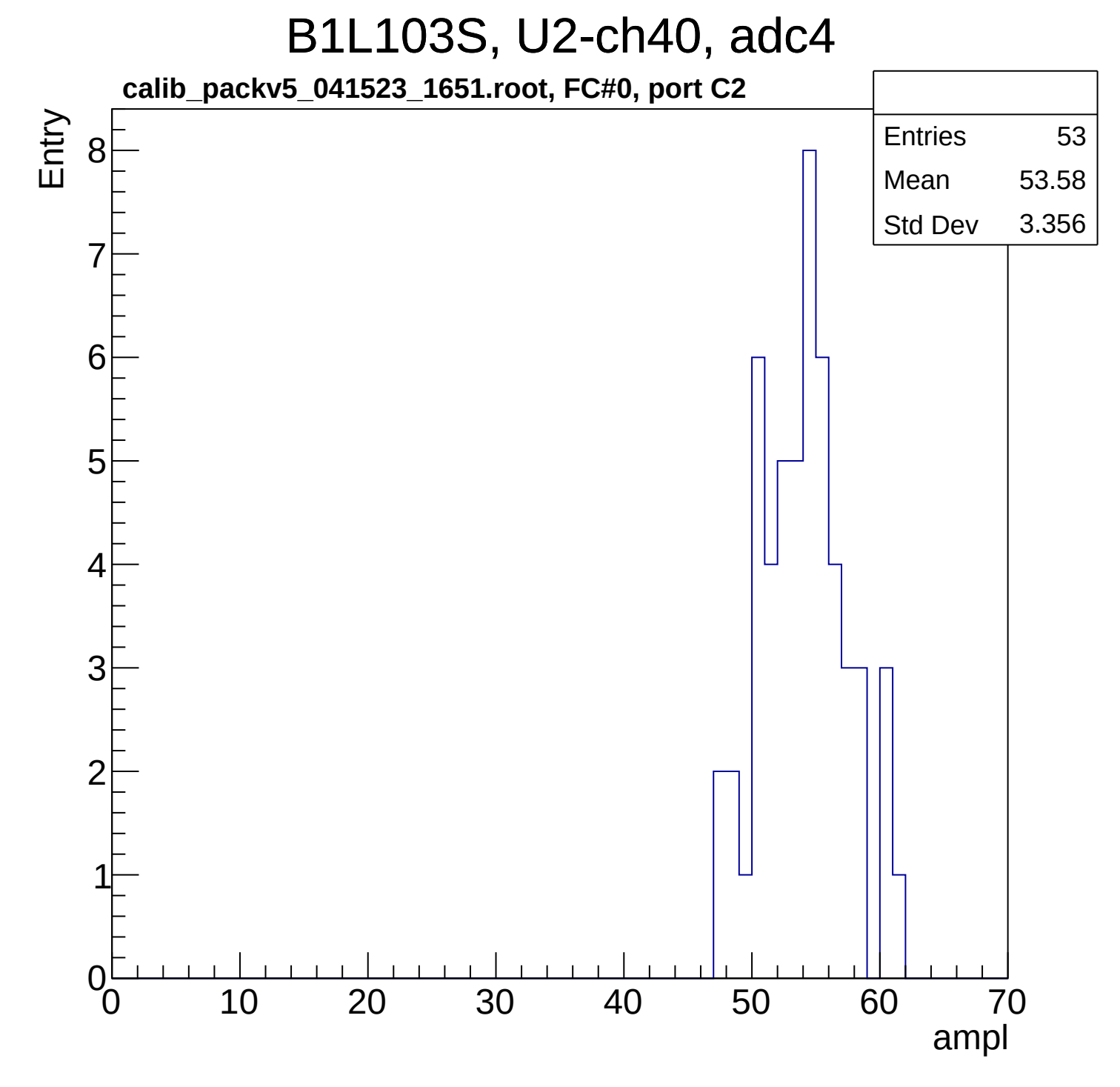

B1L103S, U2-ch39, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

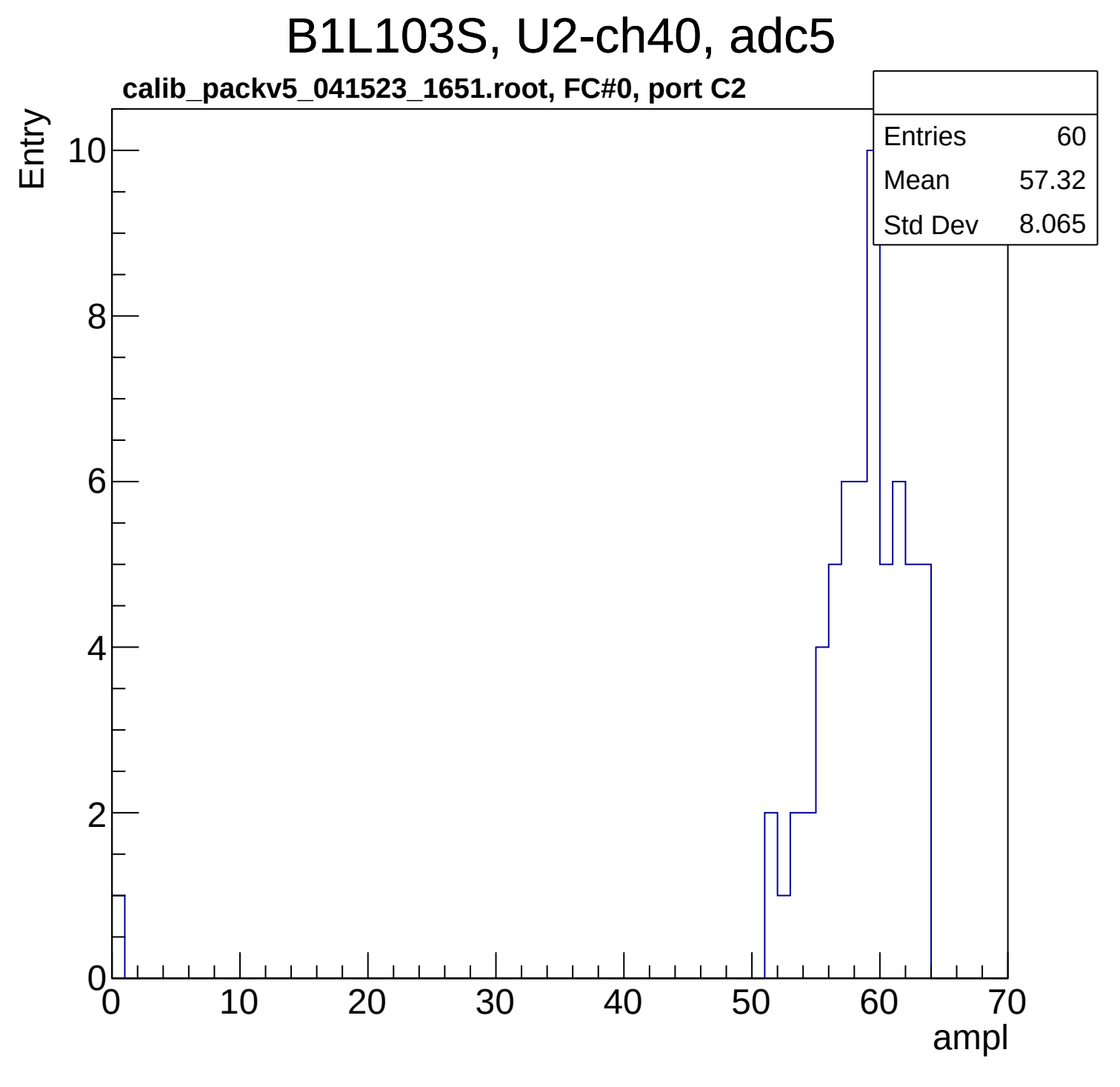

B1L103S, U2-ch40, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 24.34
Std Dev 10.08
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

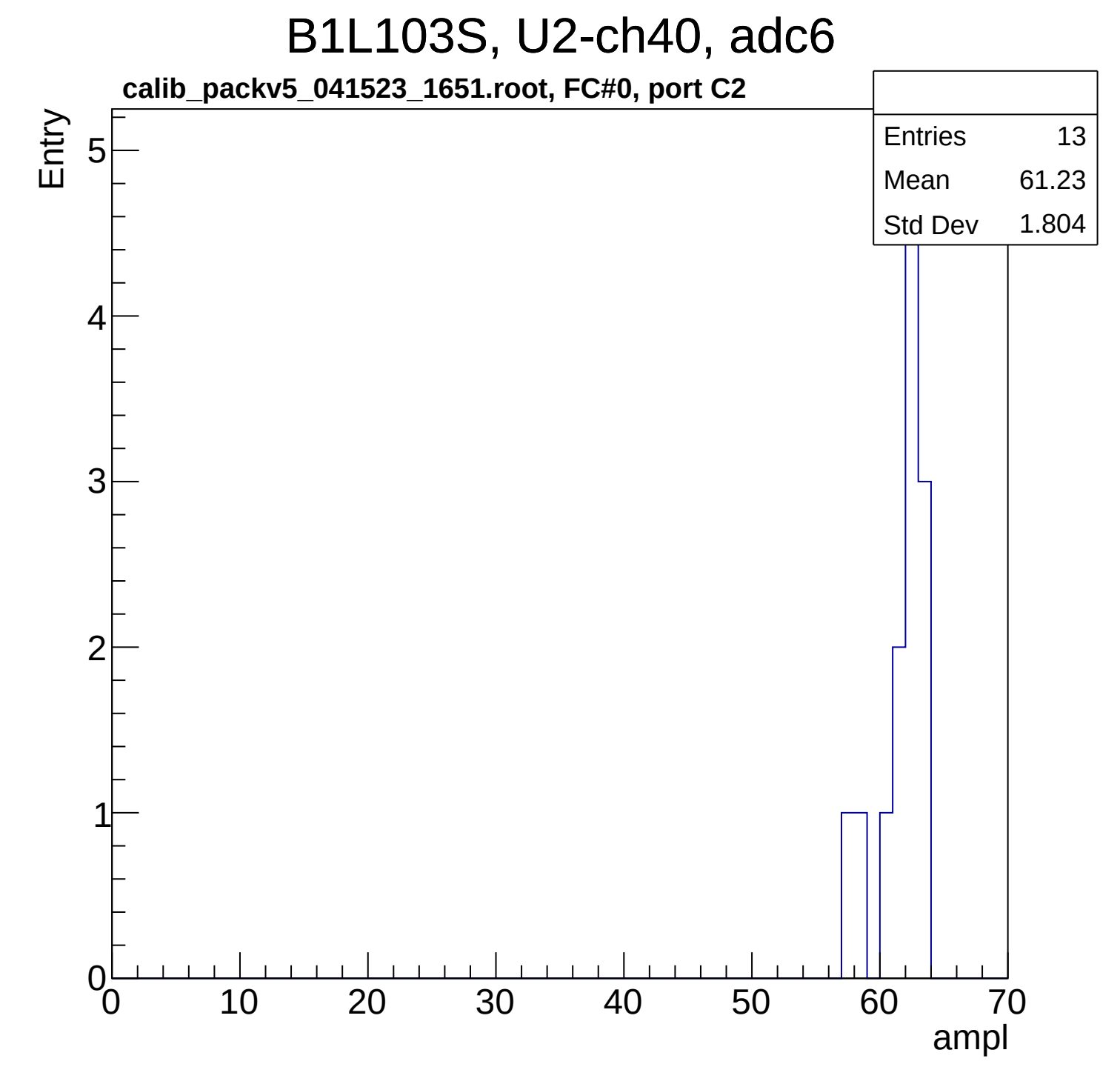

B1L103S, U2-ch40, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 32.46
Std Dev 10.58
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

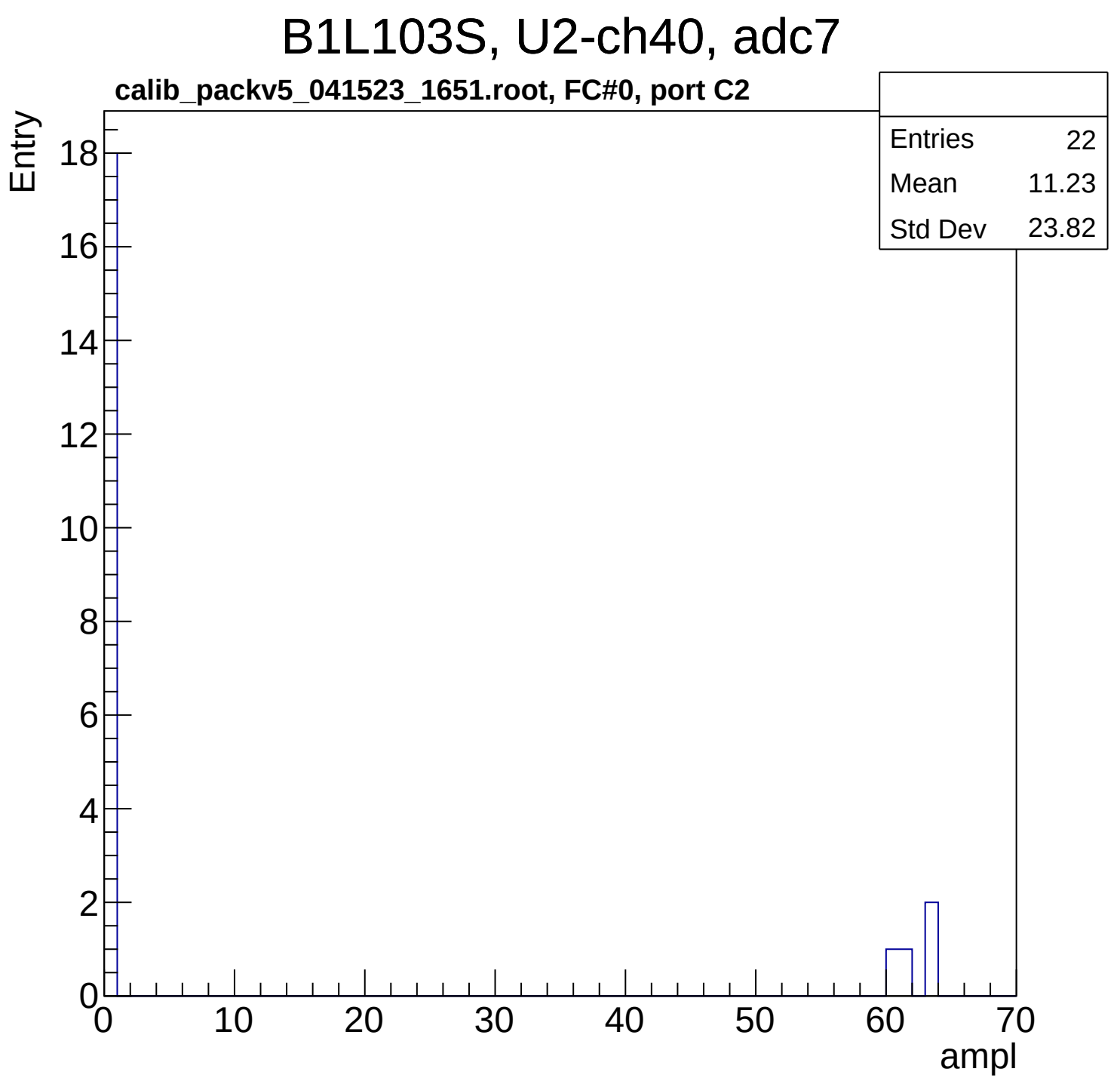

B1L103S, U2-ch40, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 35.15
Std Dev 13.89
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

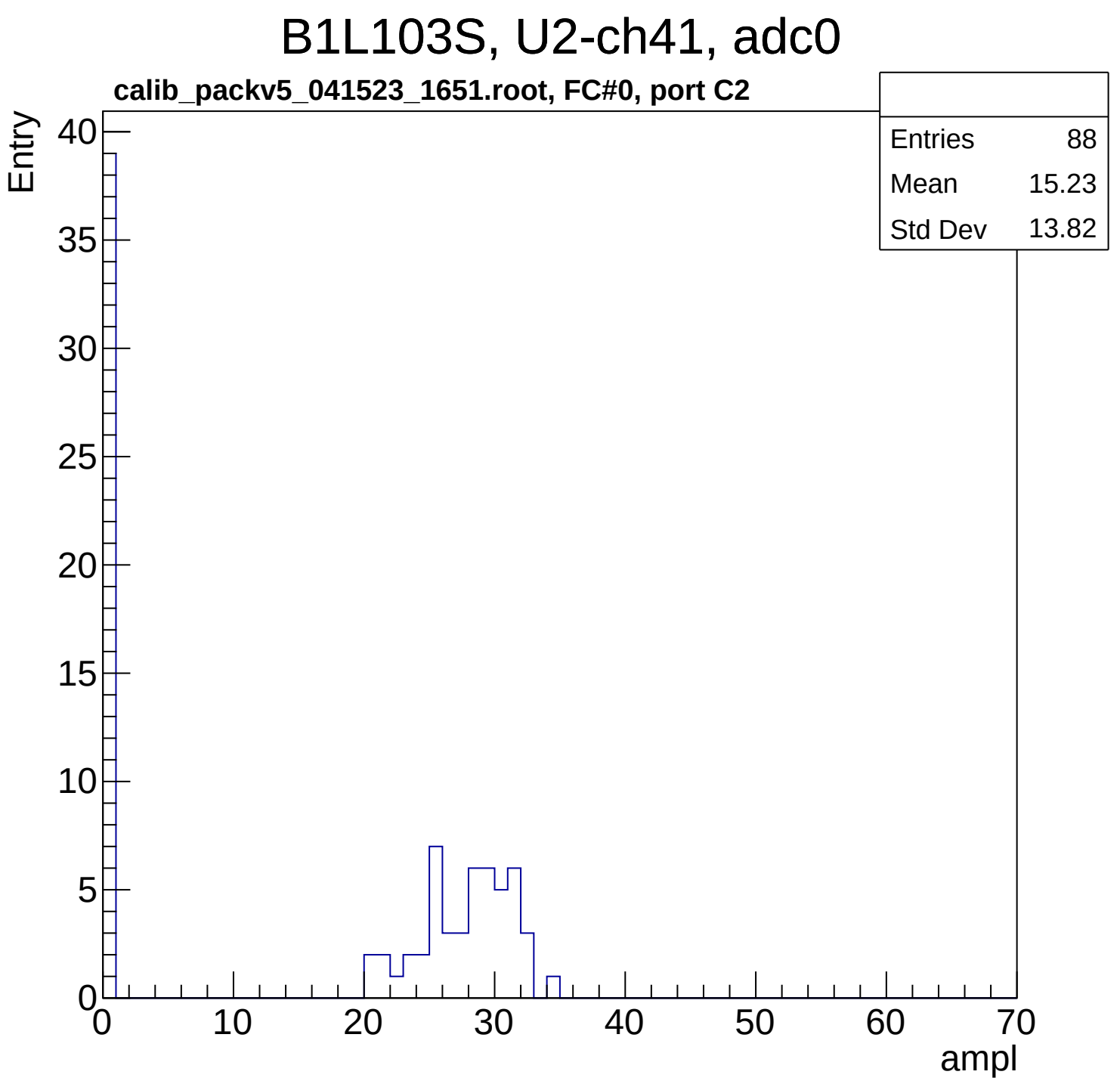

B1L103S, U2-ch40, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 45.45
Std Dev 8.096
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

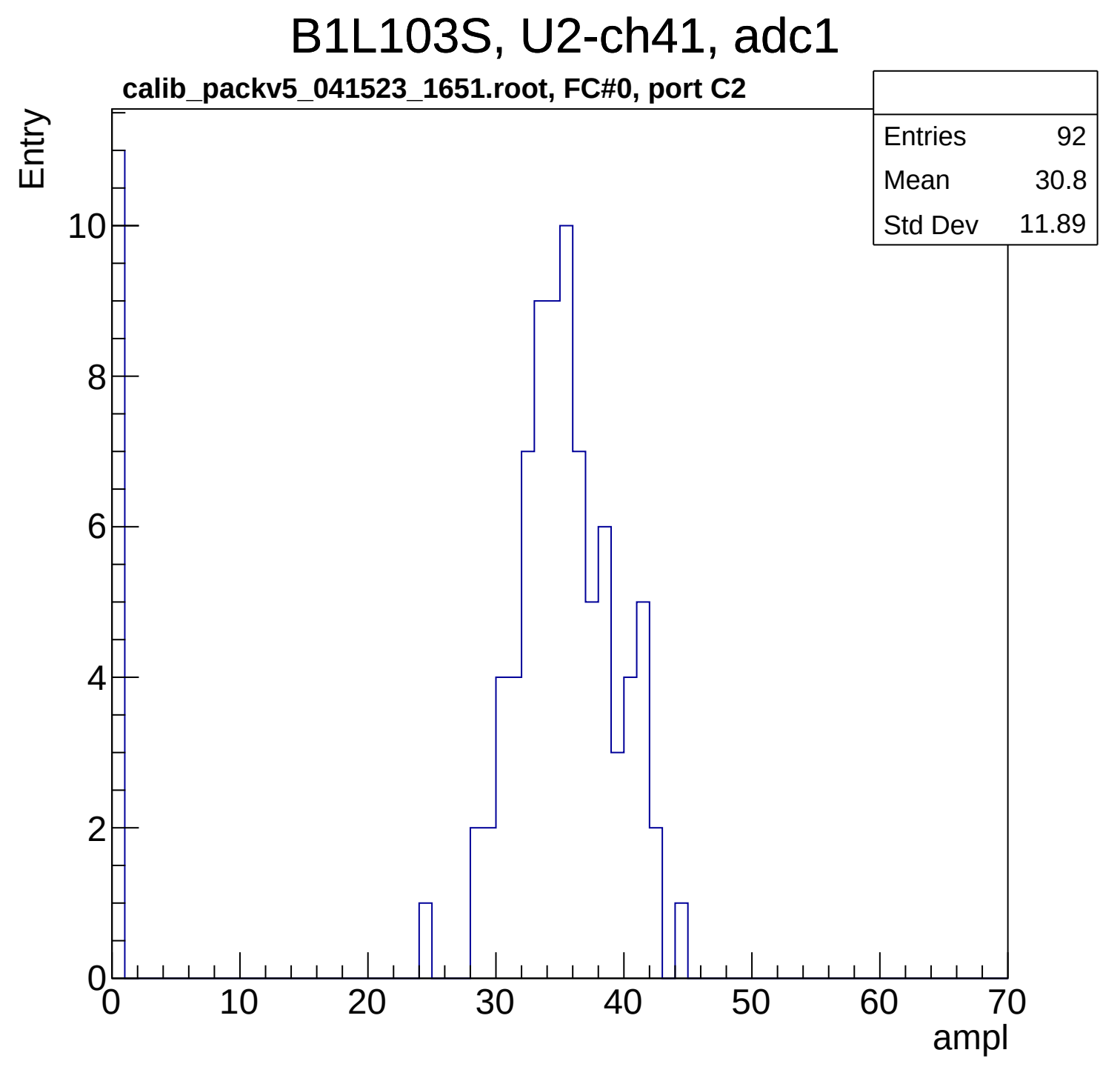

B1L103S, U2-ch40, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 53.58
Std Dev 3.356
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

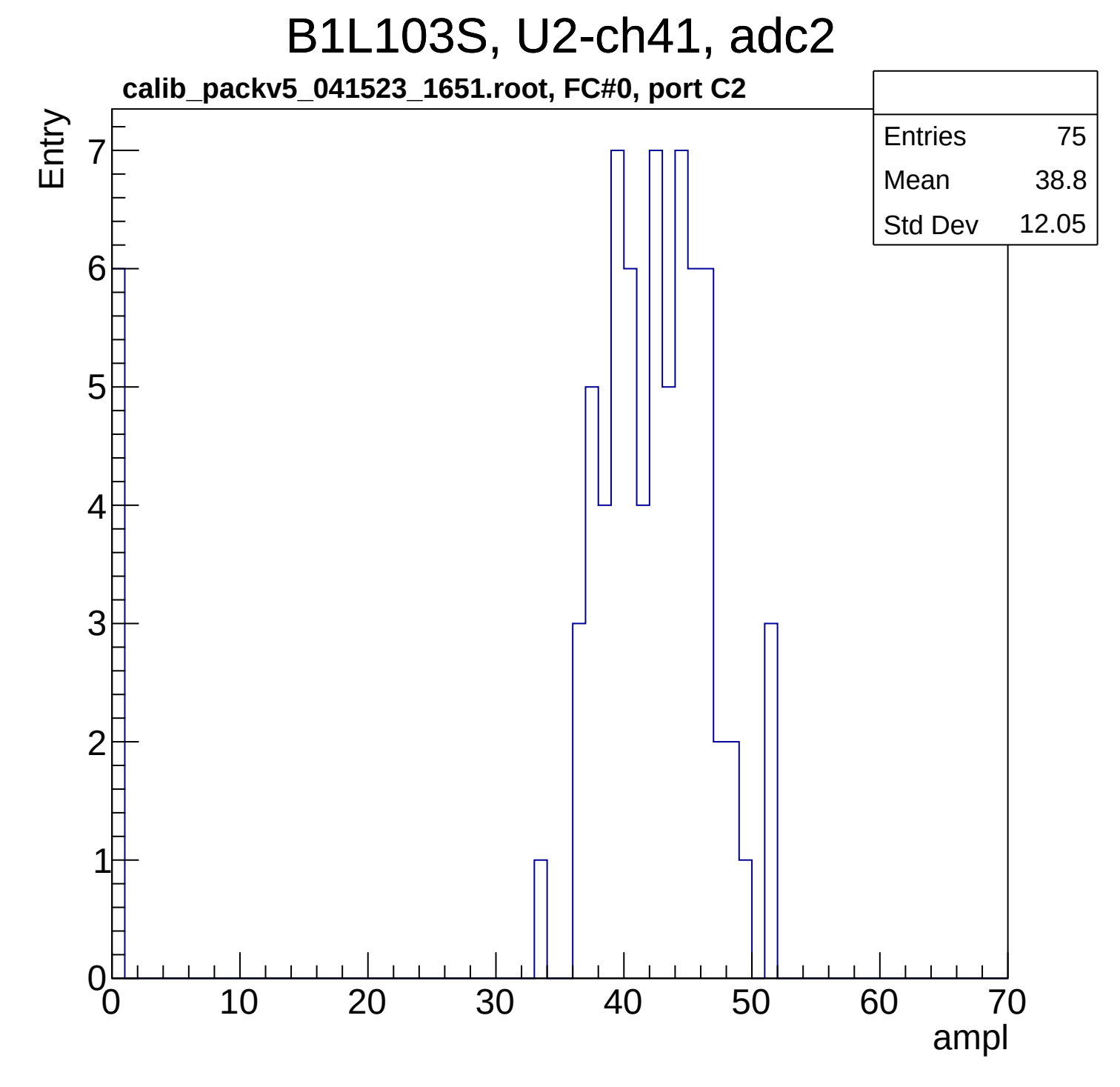

B1L103S, U2-ch40, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 57.32
Std Dev 8.065
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

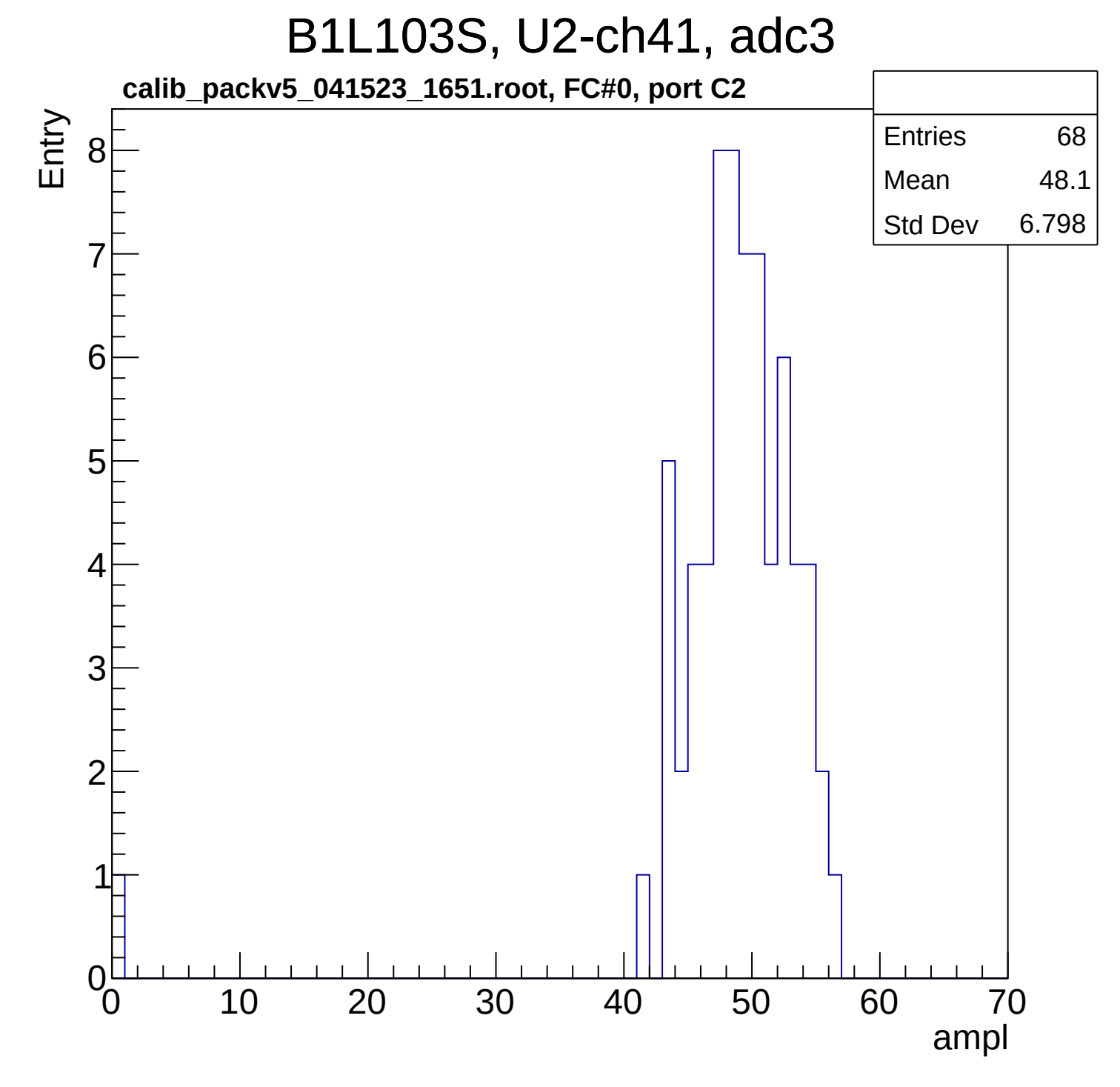

B1L103S, U2-ch40, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.23
Std Dev 1.804
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

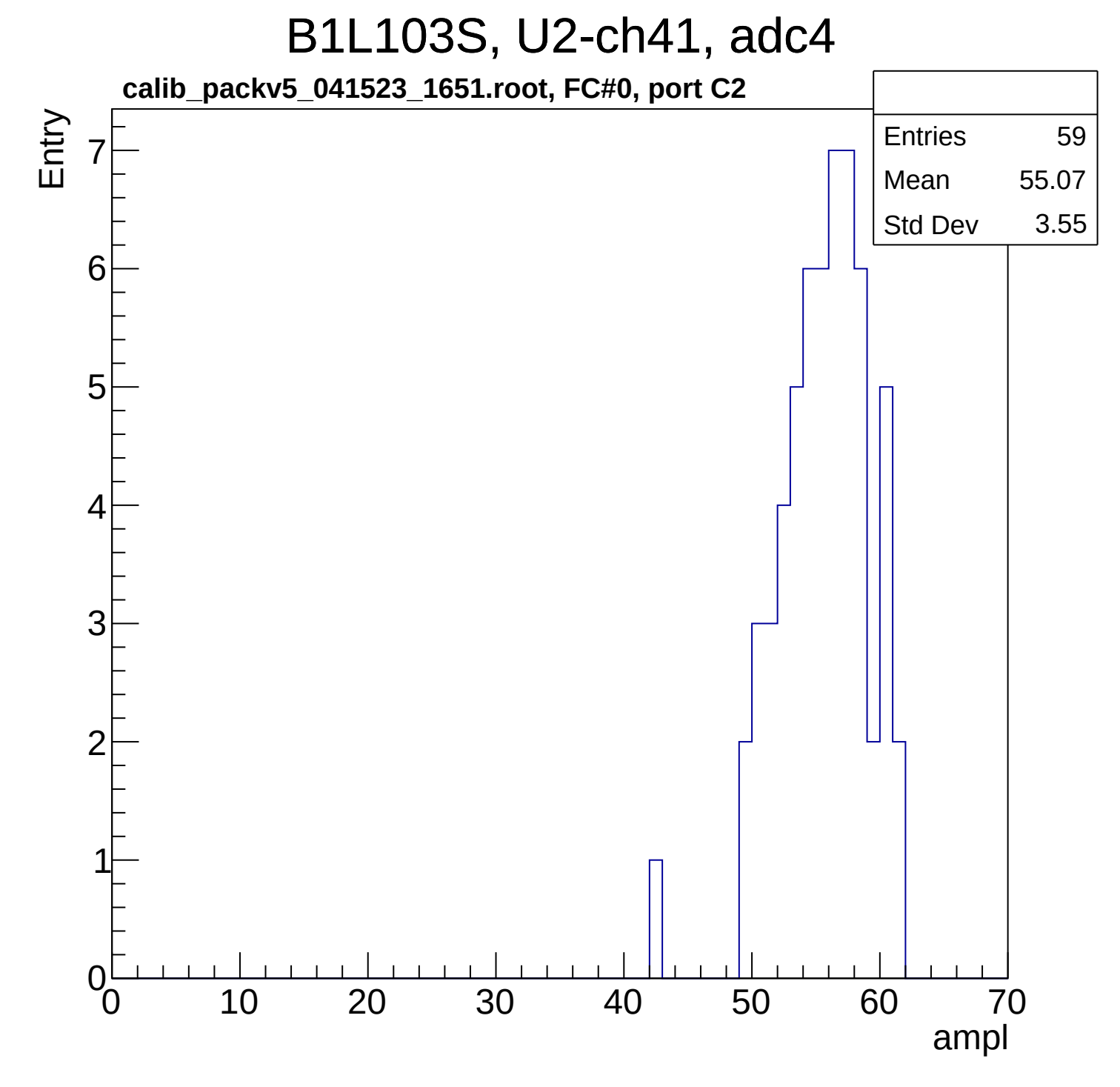

B1L103S, U2-ch40, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 11.23
Std Dev 23.82
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

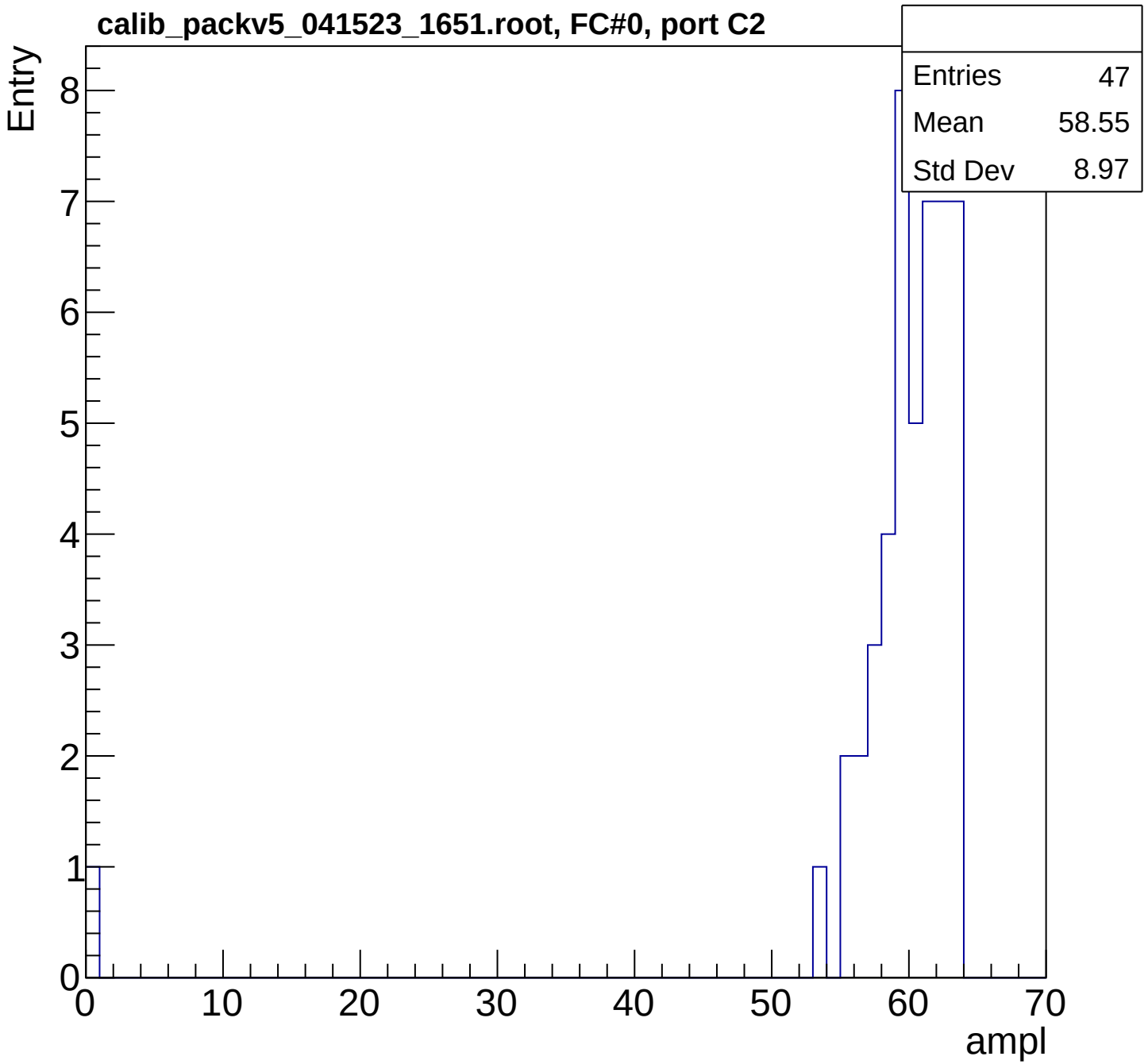

B1L103S, U2-ch41, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 15.23
Std Dev 13.82
Entry
ampl
0
5
10
15
20
25
30
35
40
0
10
20
30
40
50
60
70

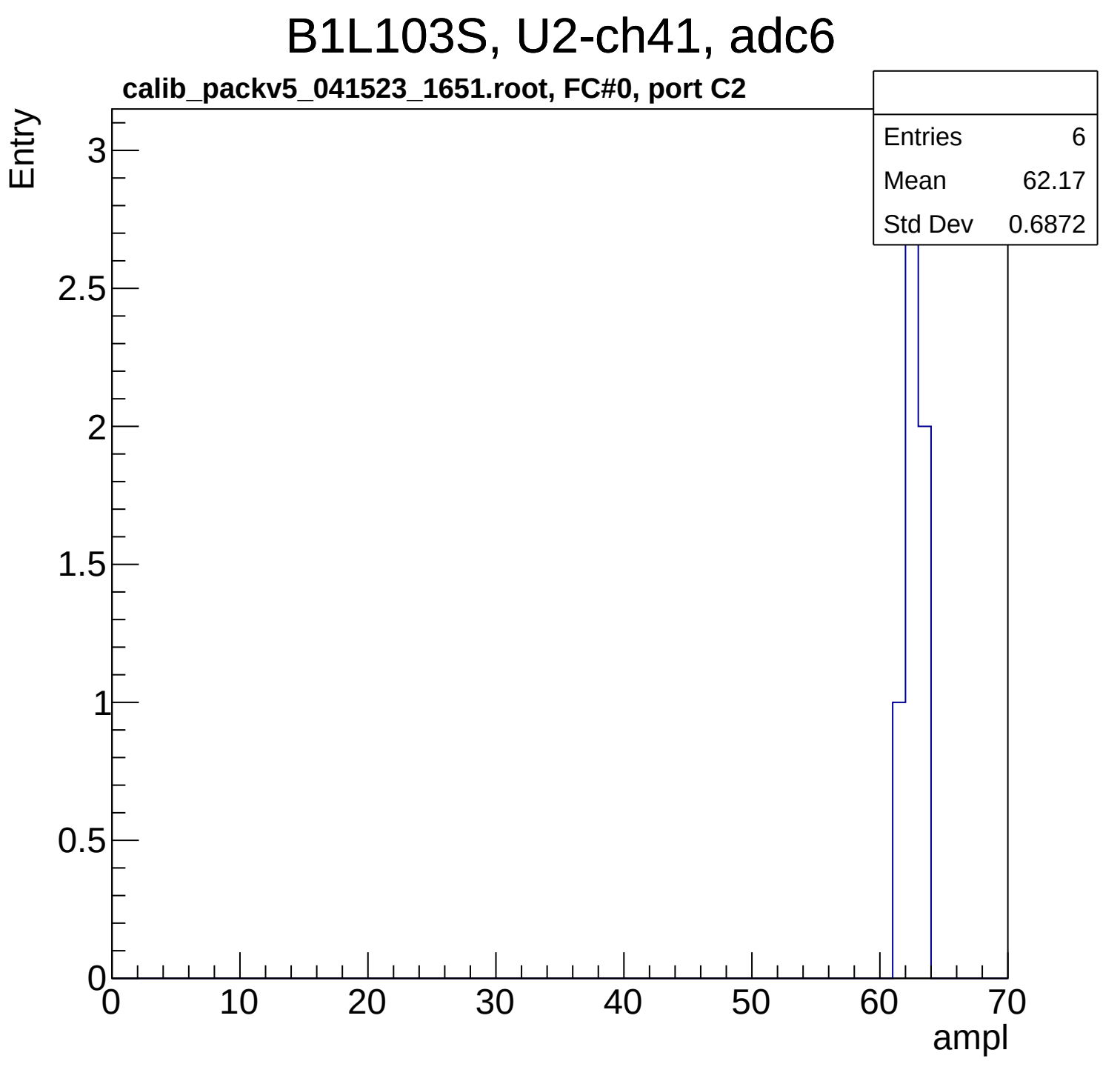

B1L103S, U2-ch41, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 30.8
Std Dev 11.89
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

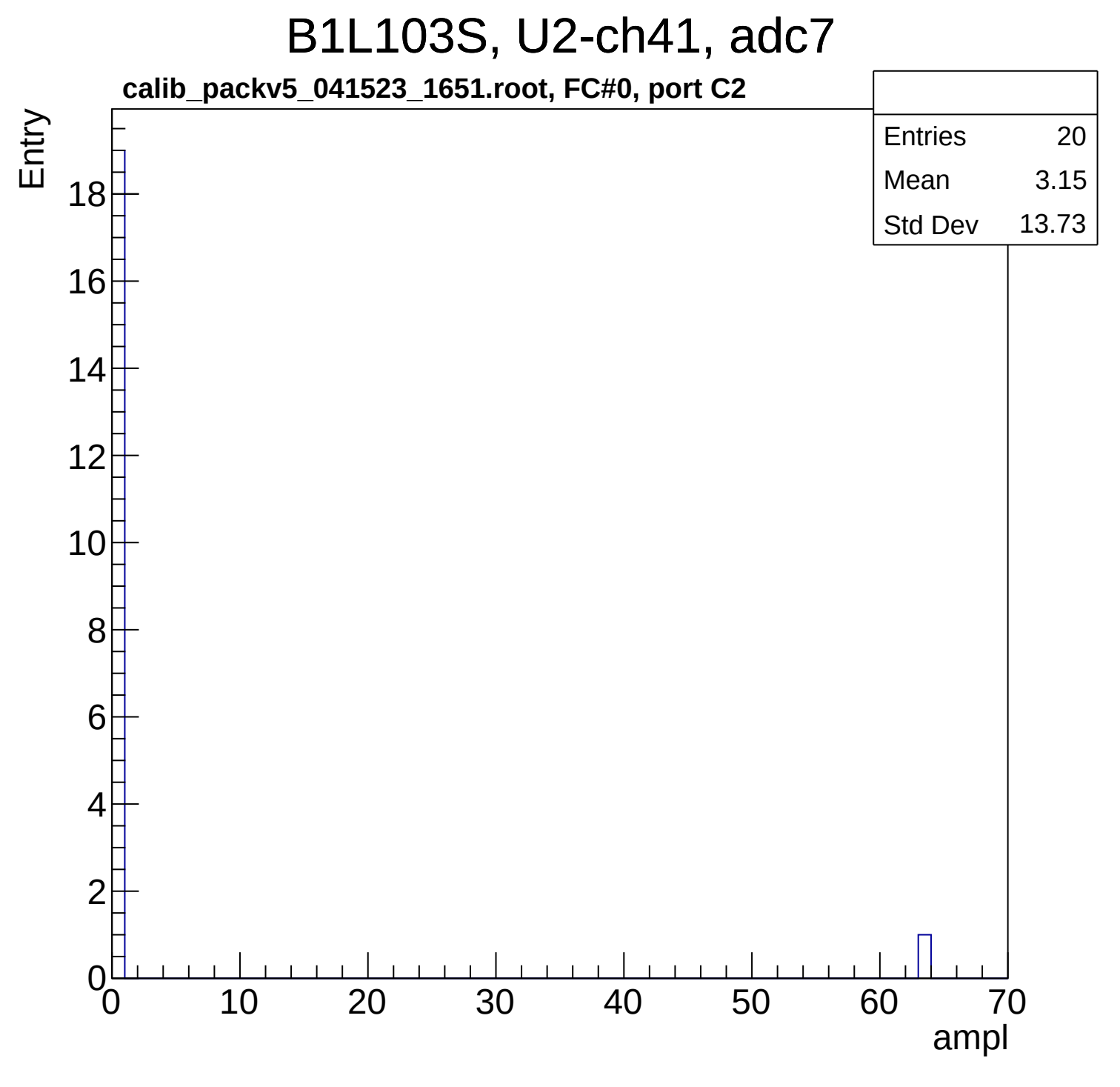

B1L103S, U2-ch41, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 38.8
Std Dev 12.05
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

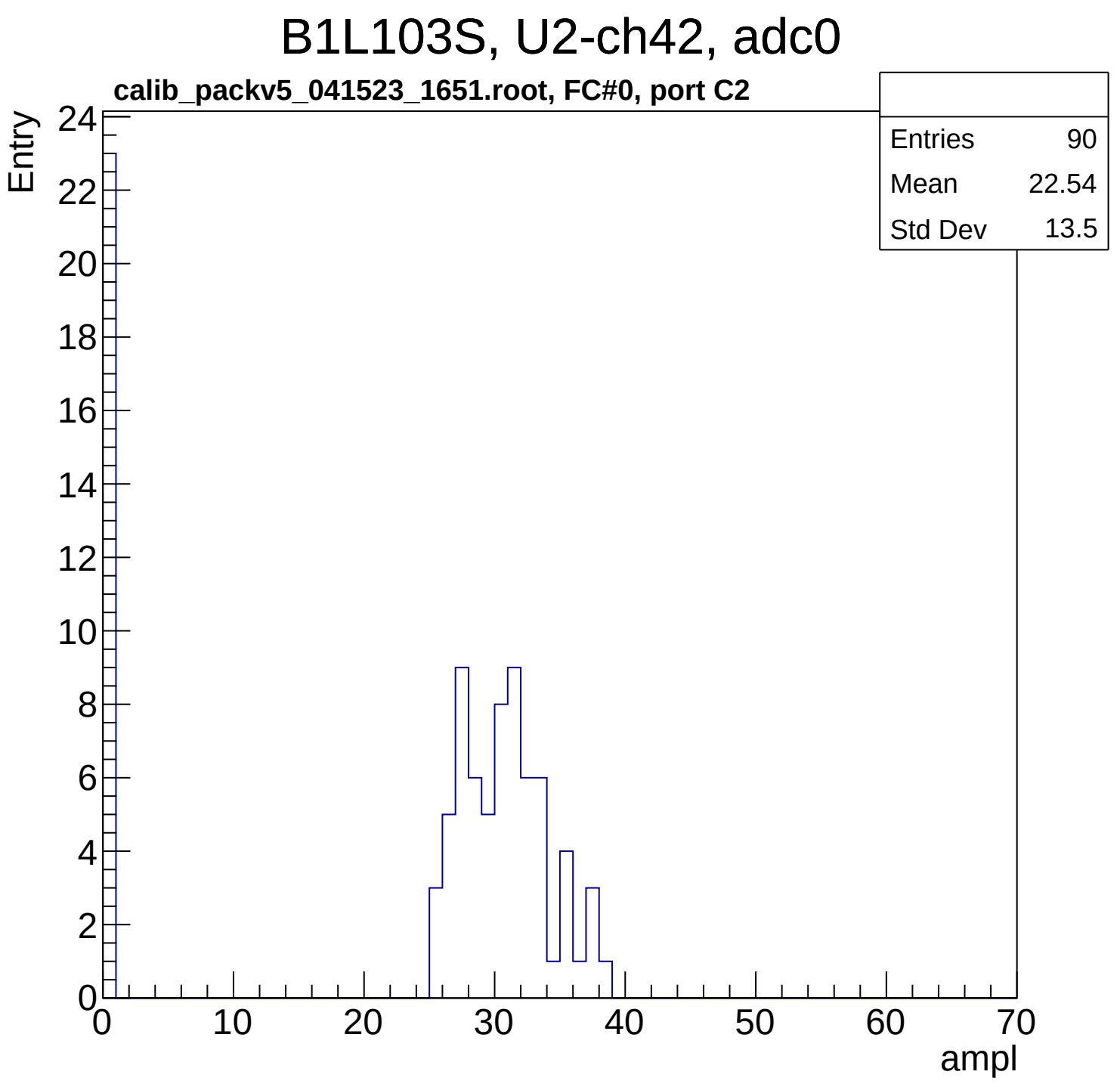

B1L103S, U2-ch41, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 48.1
Std Dev 6.798
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

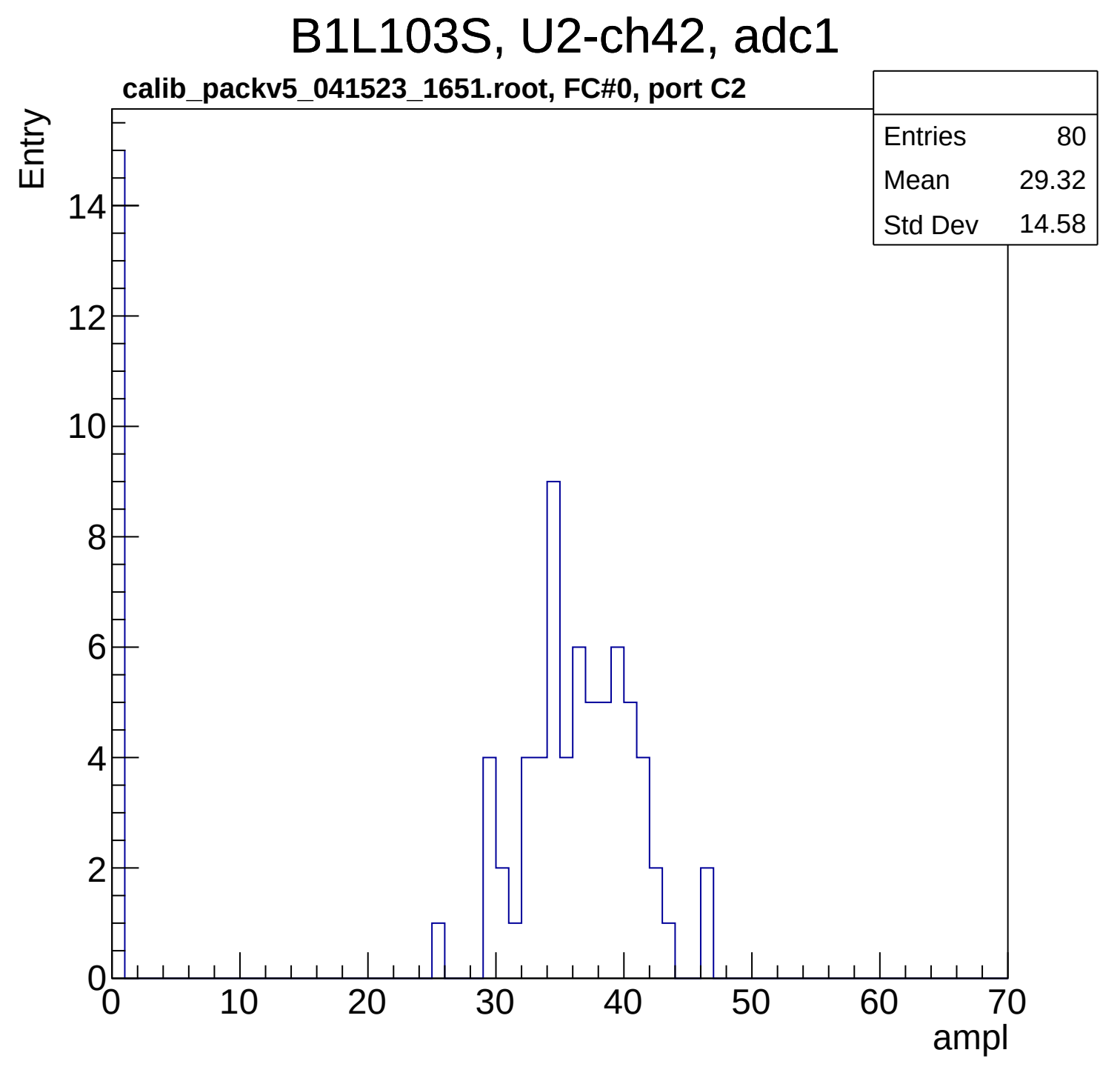

B1L103S, U2-ch41, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 55.07
Std Dev 3.55
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

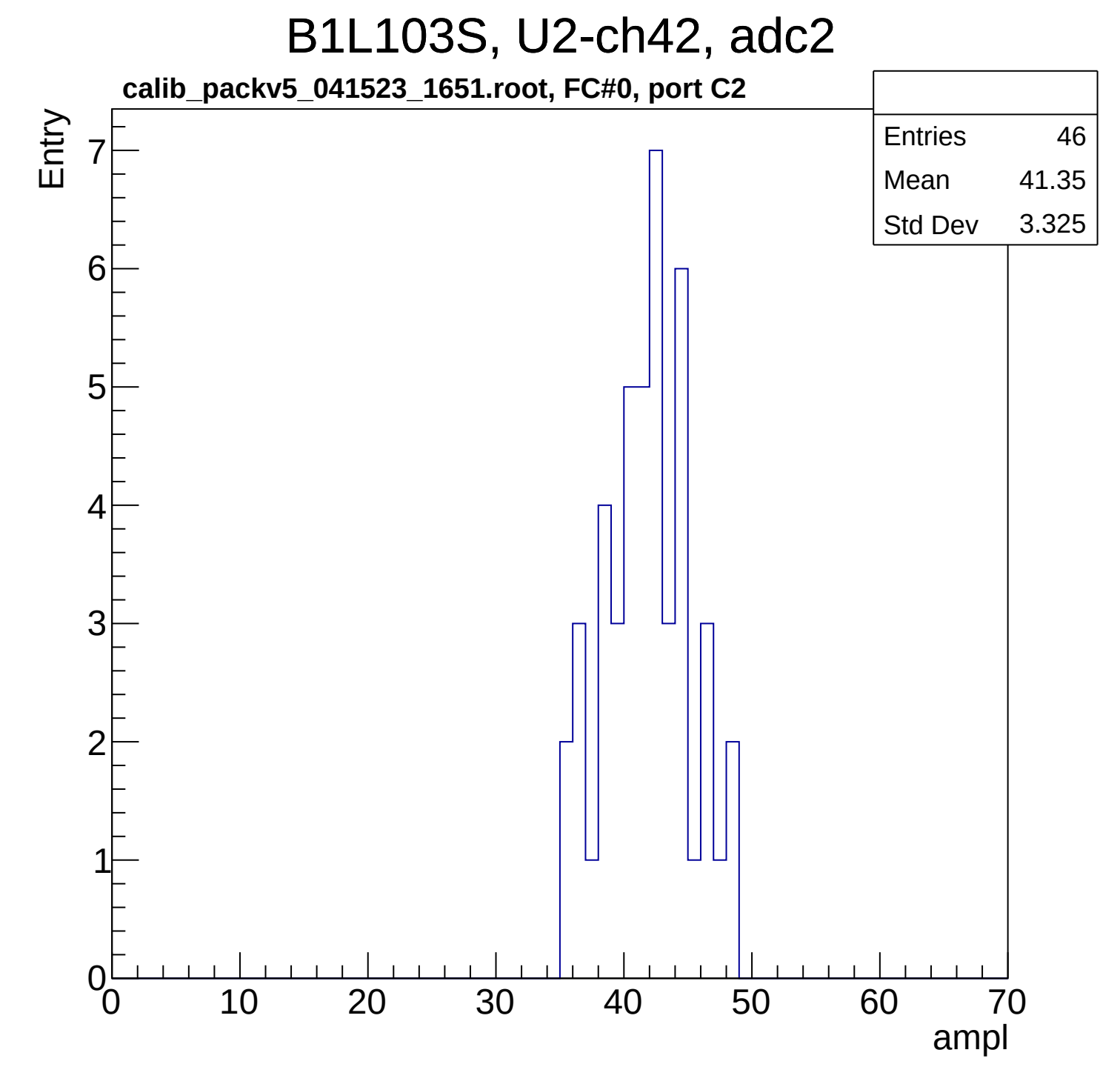

B1L103S, U2-ch41, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.55
Std Dev 8.97
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

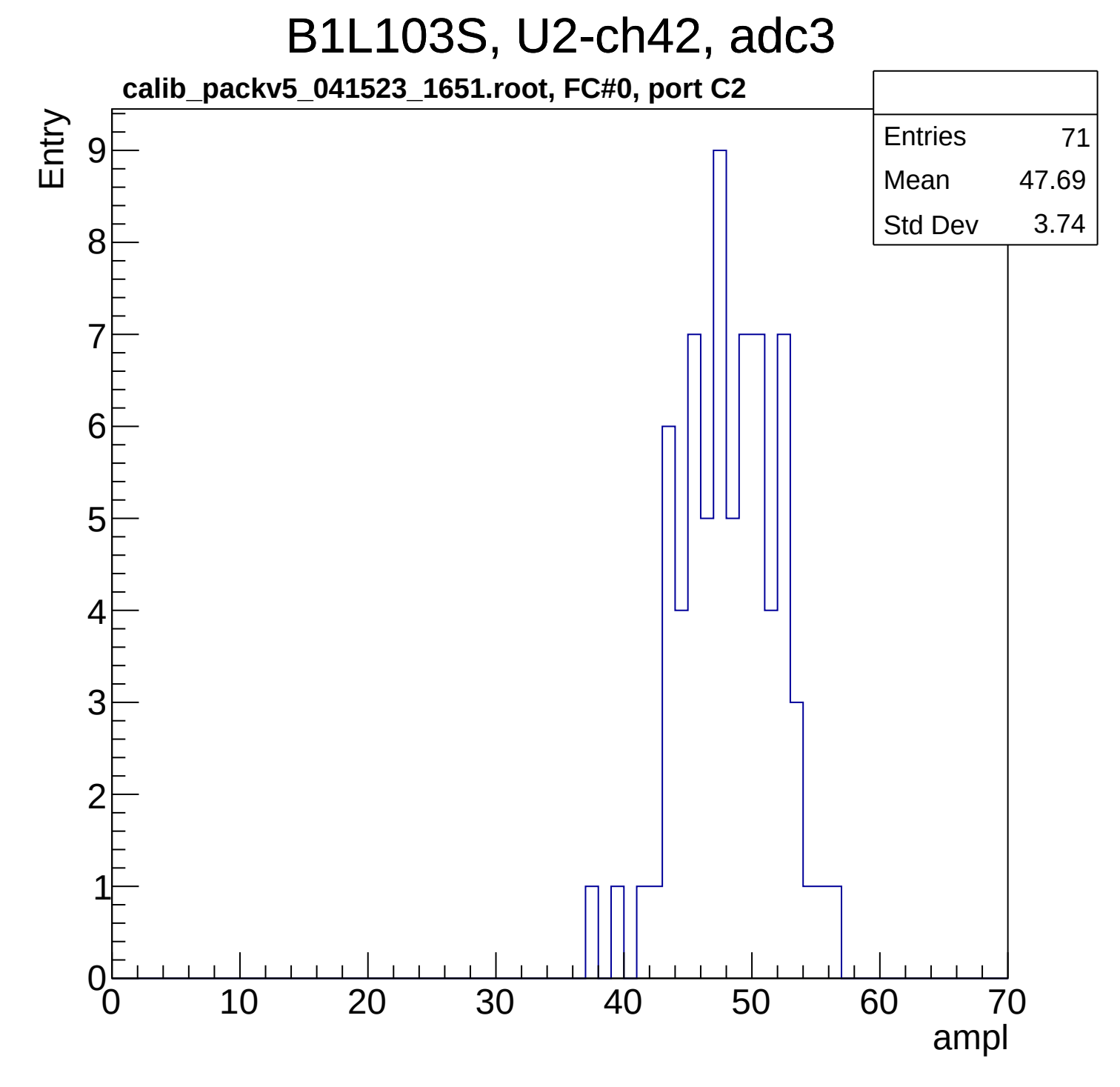

B1L103S, U2-ch41, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.17
Std Dev 0.6872
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

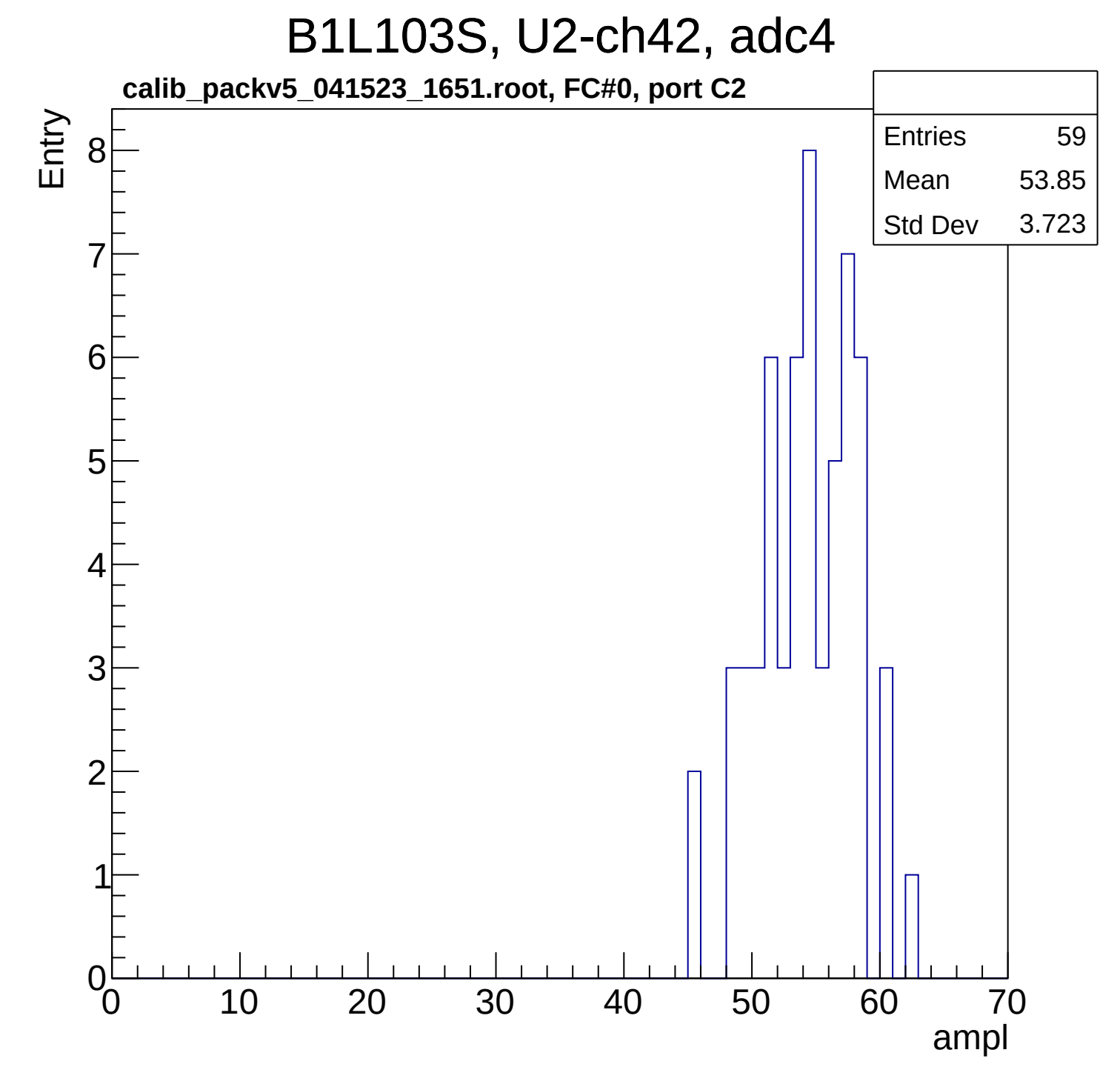

B1L103S, U2-ch41, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

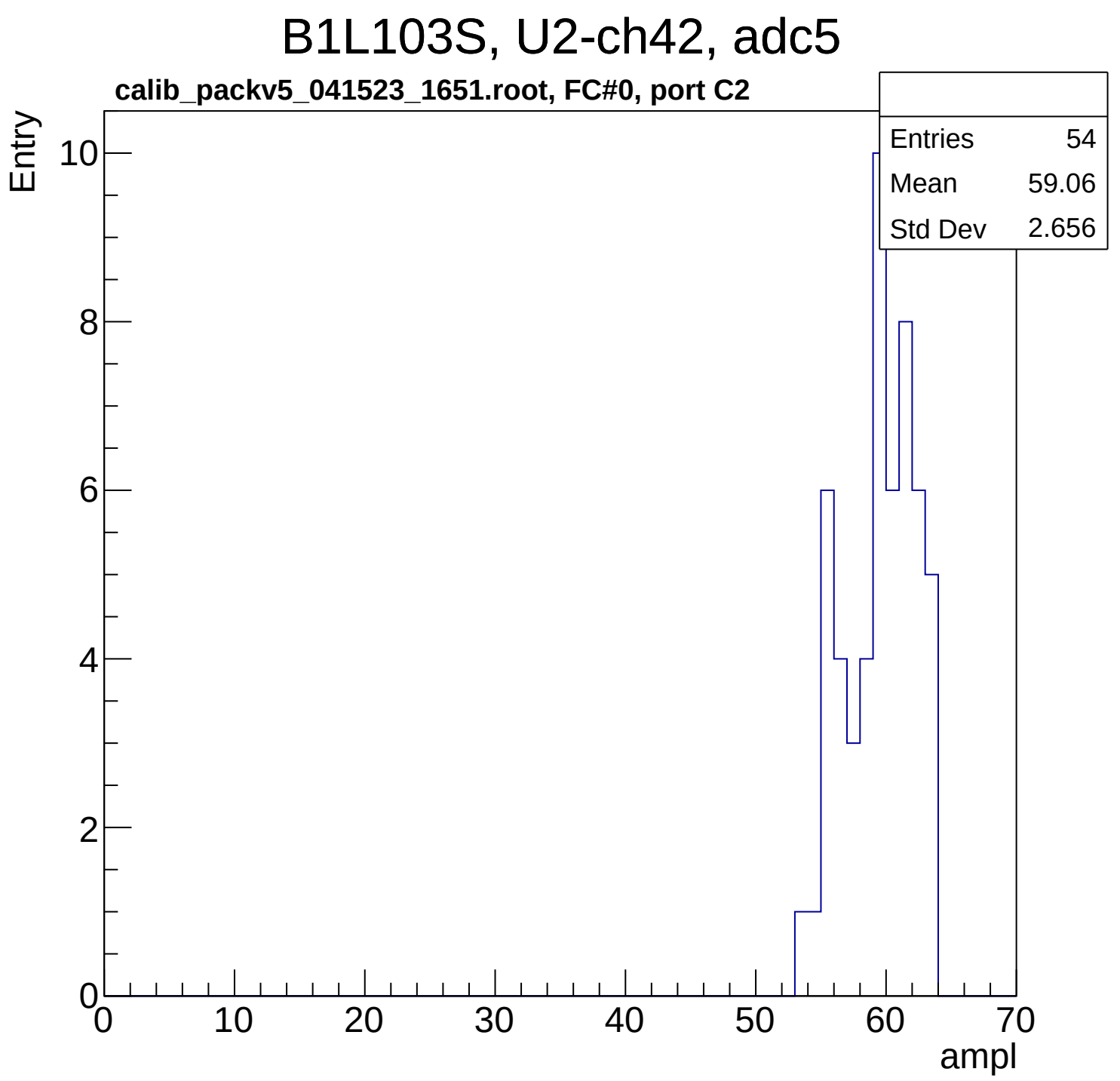

B1L103S, U2-ch42, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 22.54
Std Dev 13.5
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70

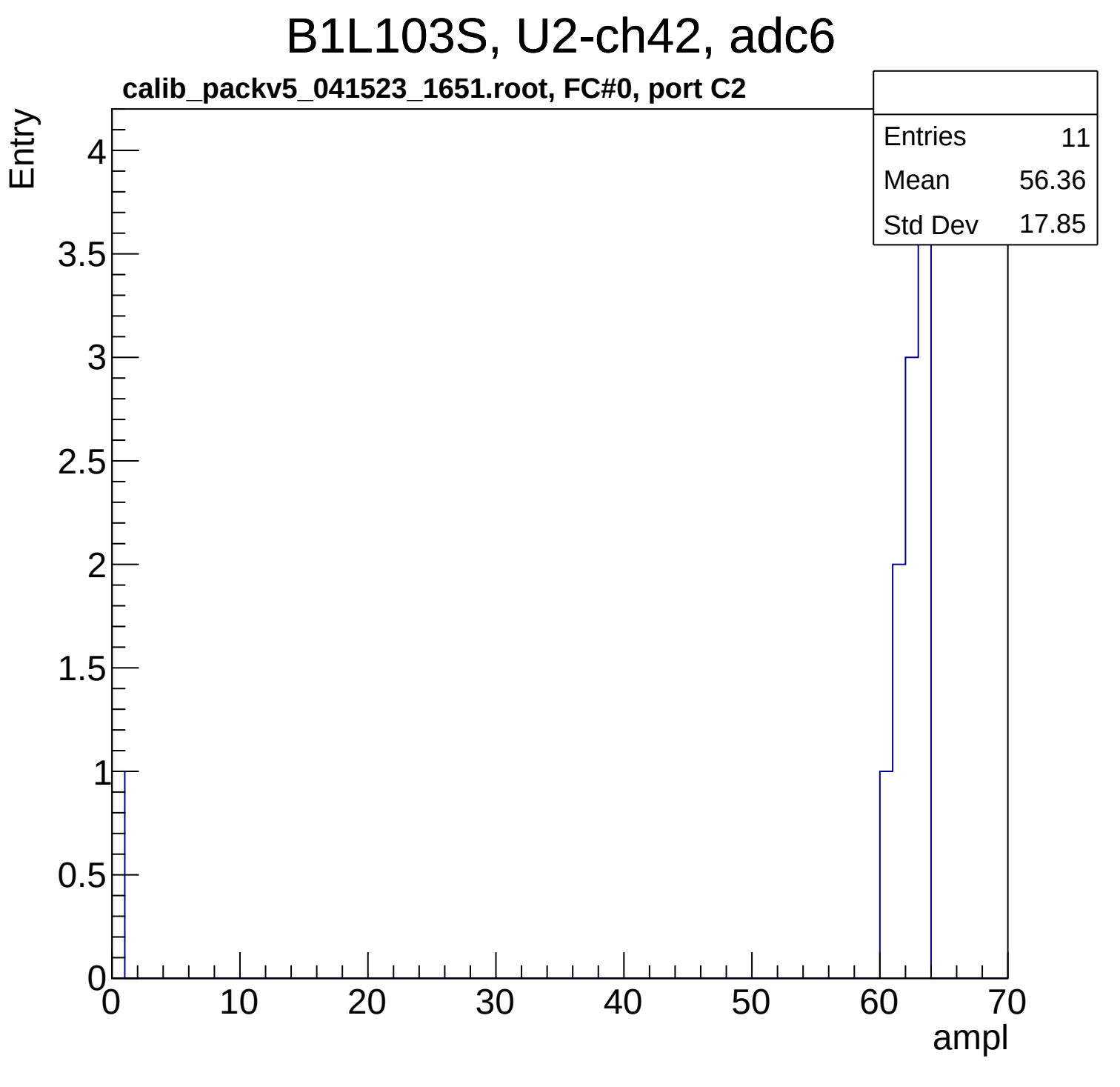

B1L103S, U2-ch42, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 29.32
Std Dev 14.58
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

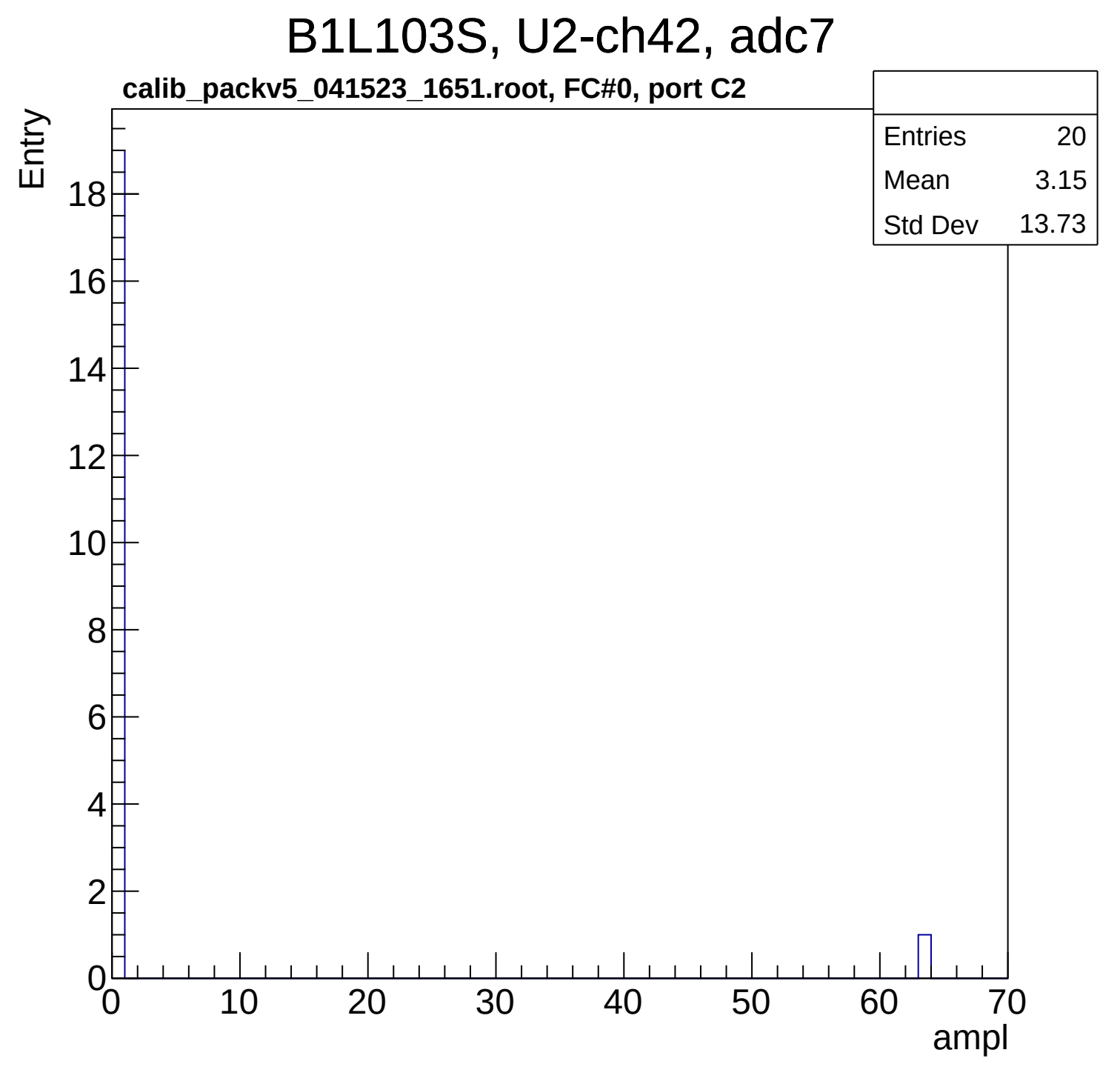

B1L103S, U2-ch42, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 41.35
Std Dev 3.325
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

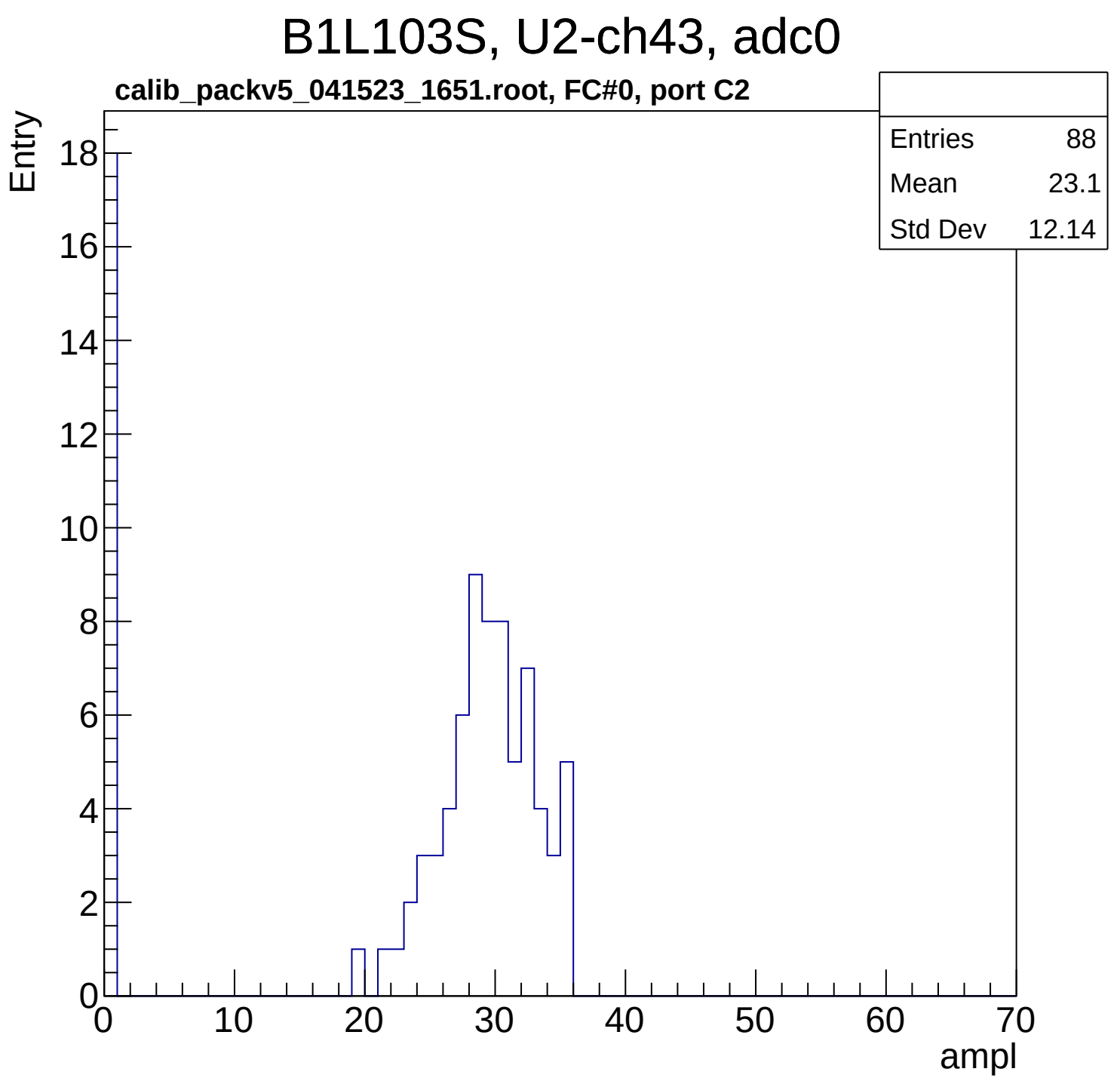

B1L103S, U2-ch42, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 47.69
Std Dev 3.74
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

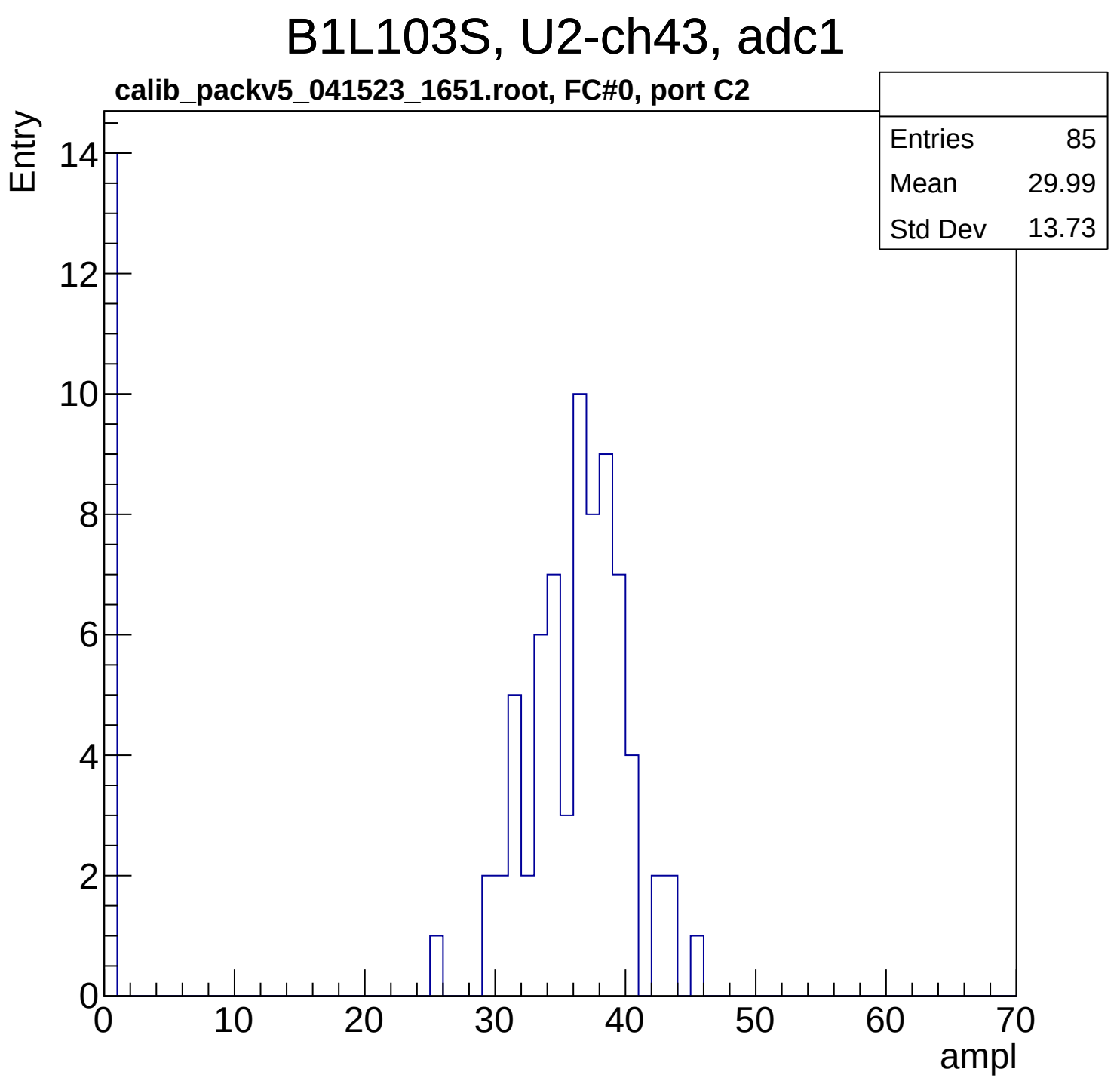

B1L103S, U2-ch42, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 53.85
Std Dev 3.723
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

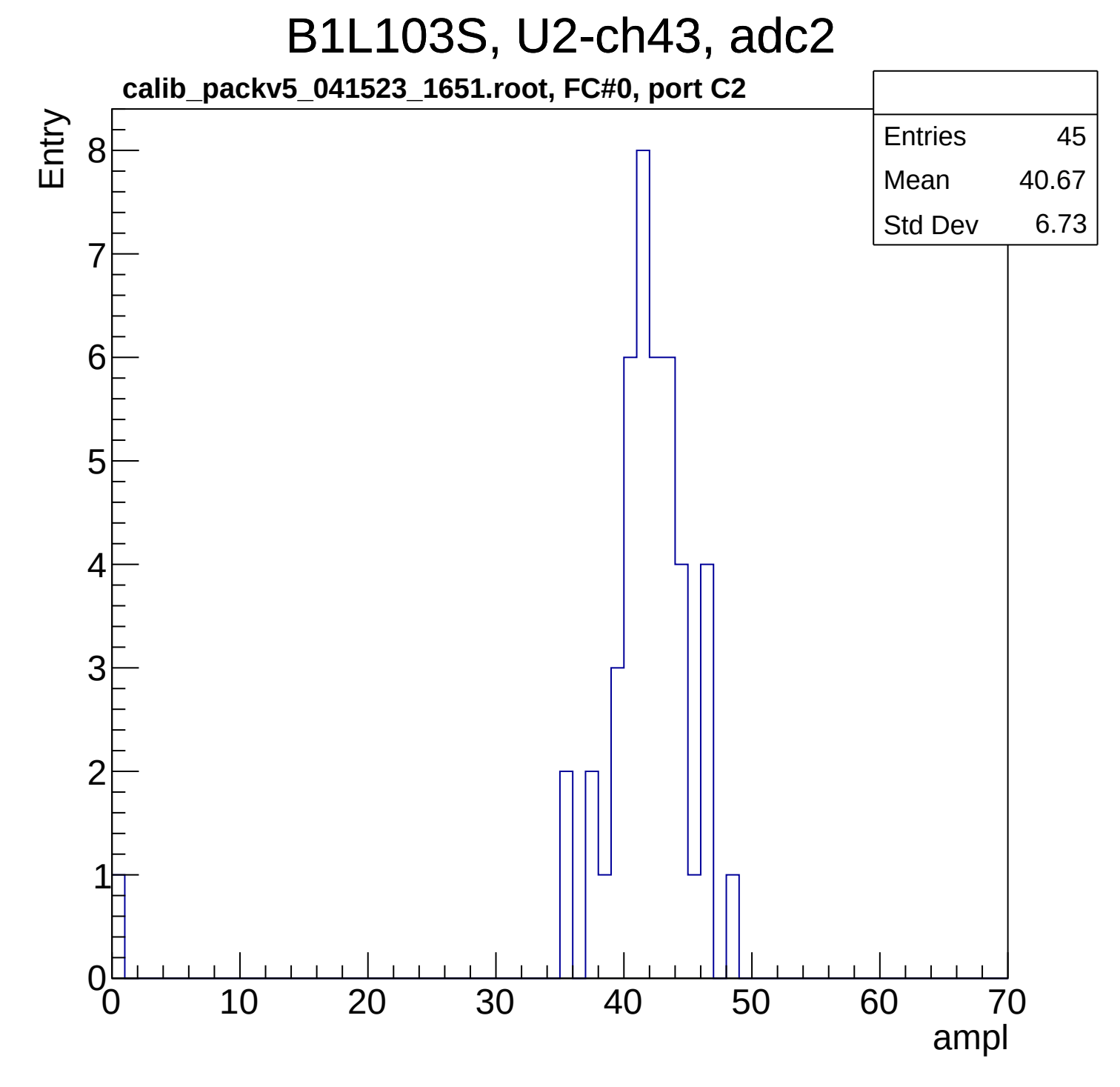

B1L103S, U2-ch42, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 59.06
Std Dev 2.656
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

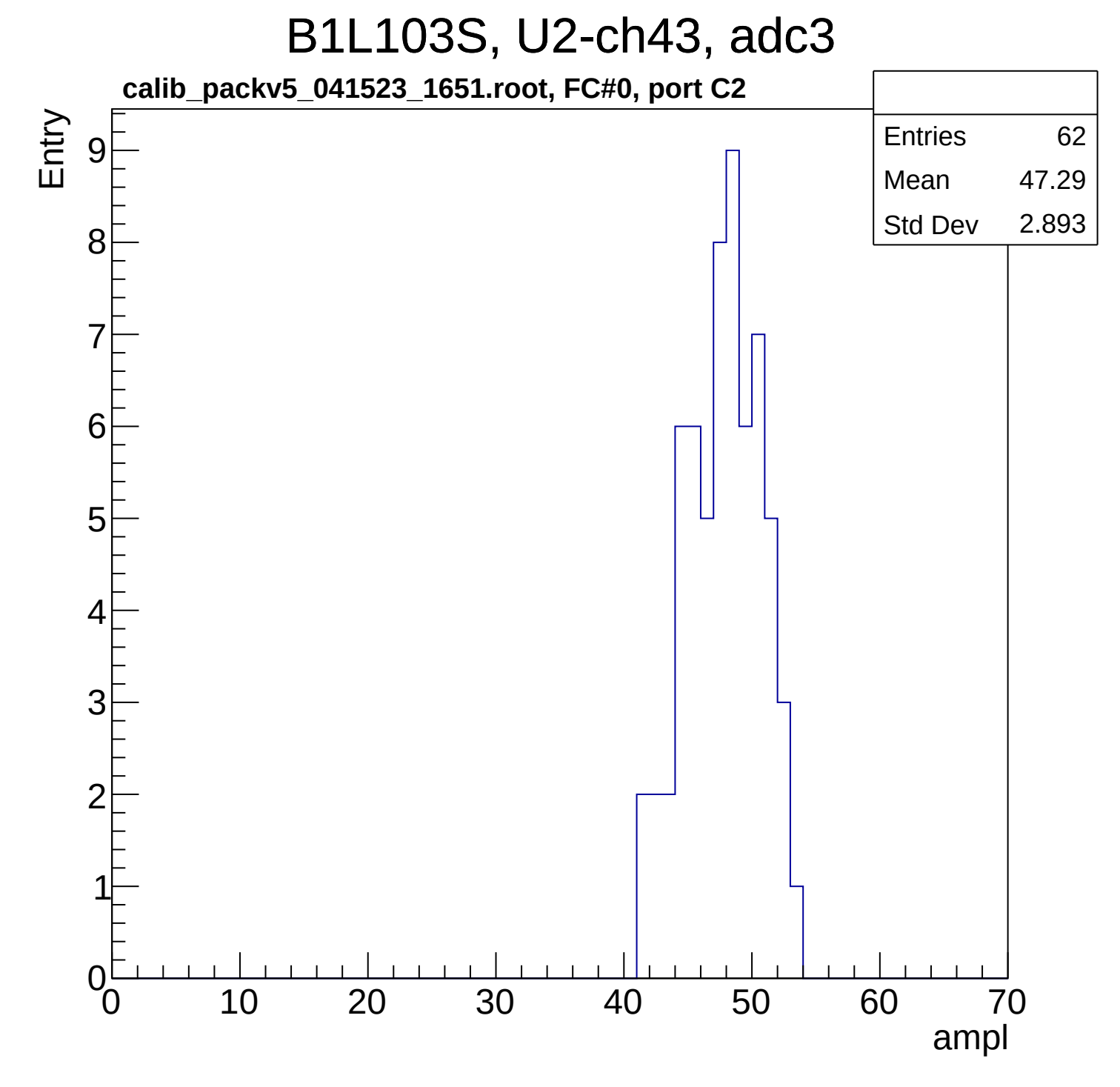

B1L103S, U2-ch42, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 56.36
Std Dev 17.85
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

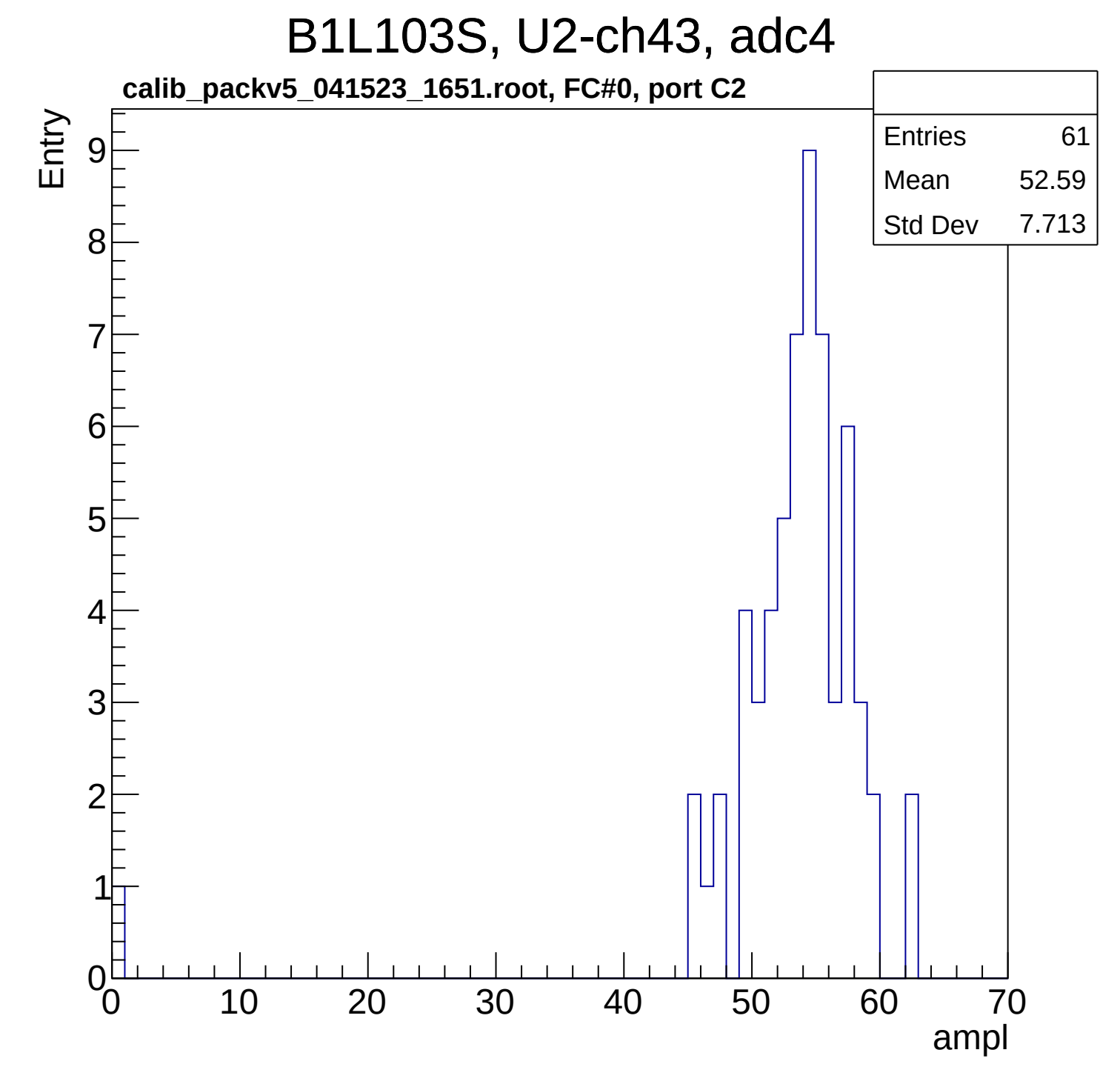

B1L103S, U2-ch42, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

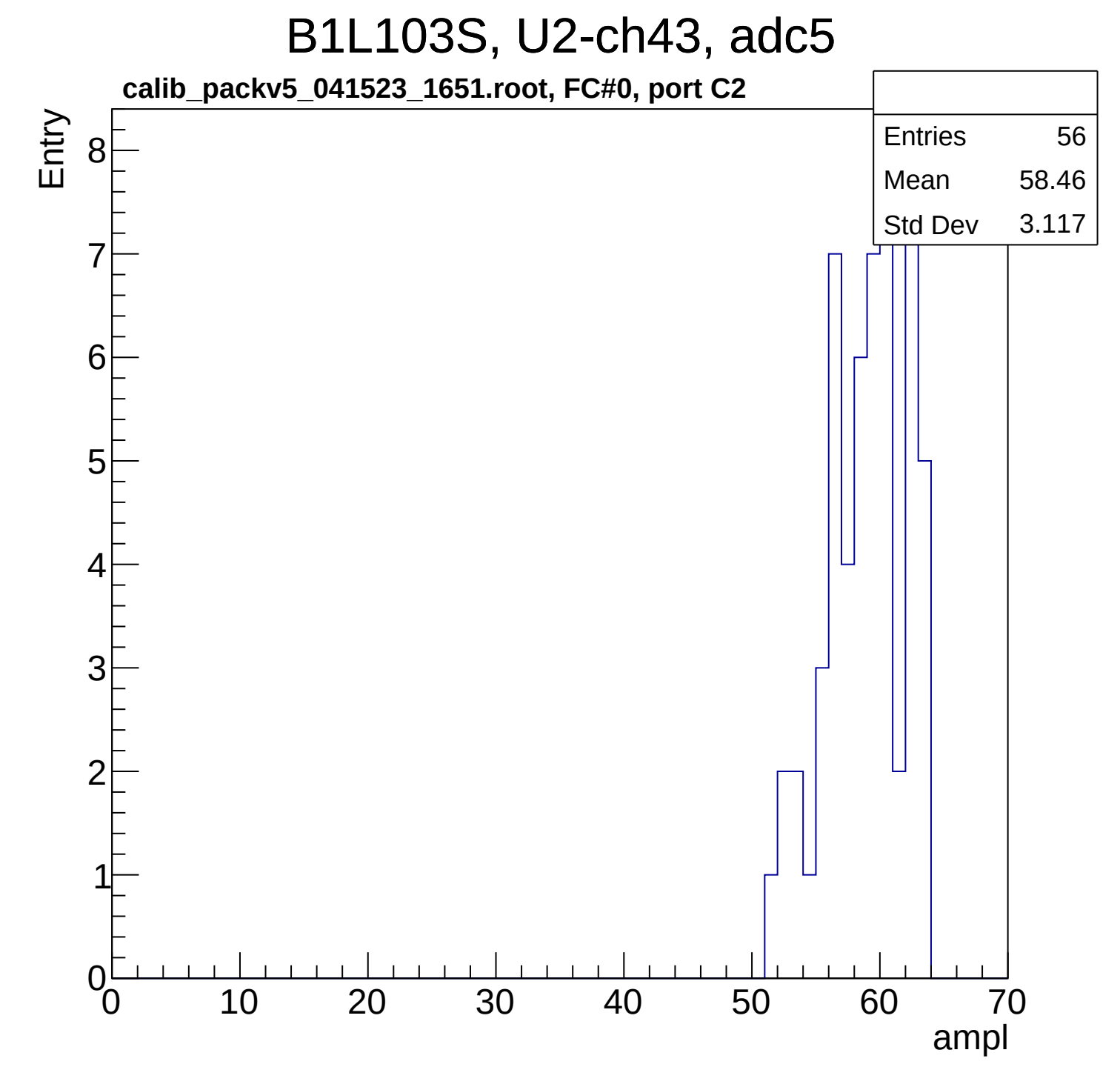

B1L103S, U2-ch43, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 23.1
Std Dev 12.14
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

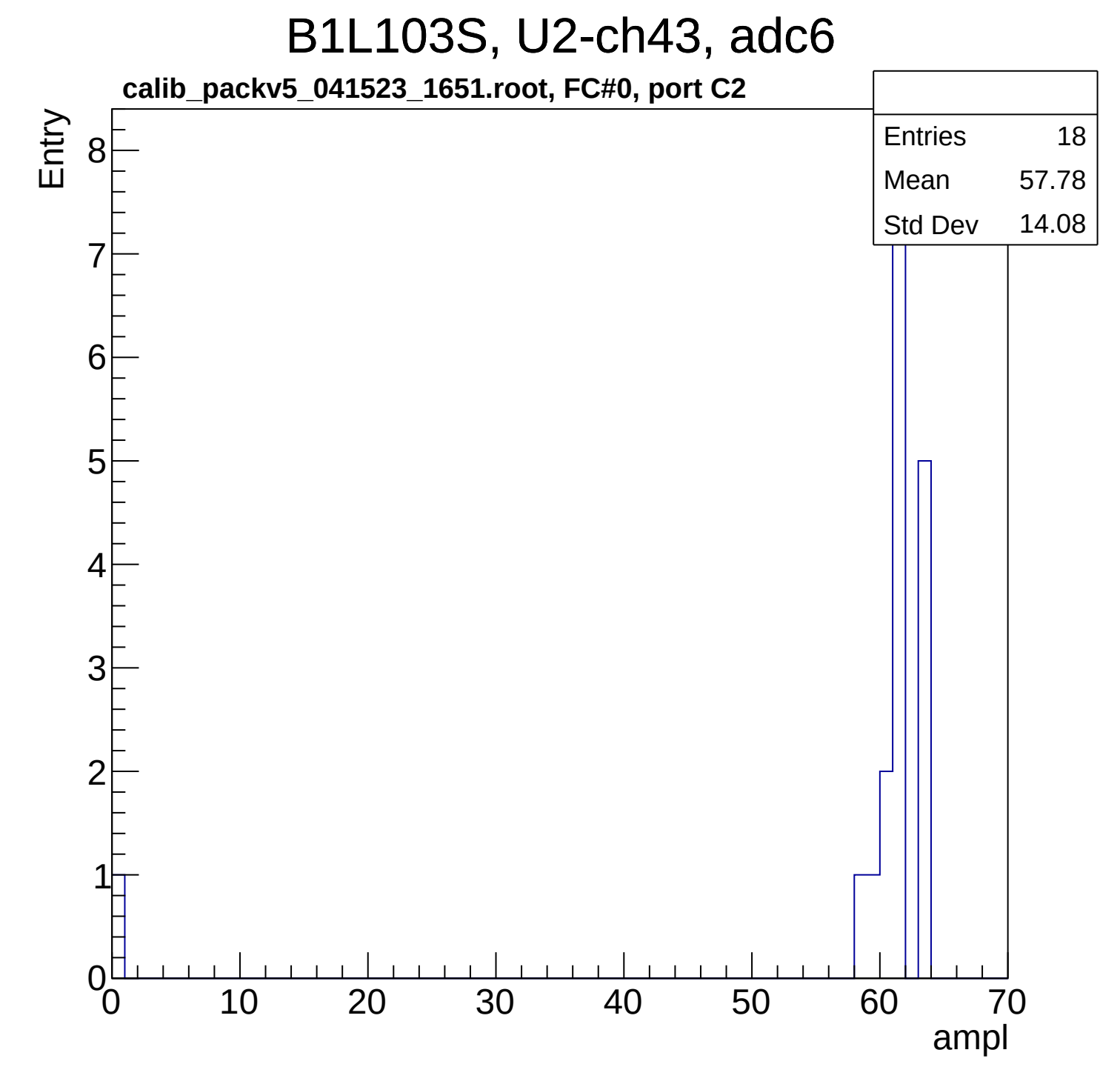

B1L103S, U2-ch43, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 29.99
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

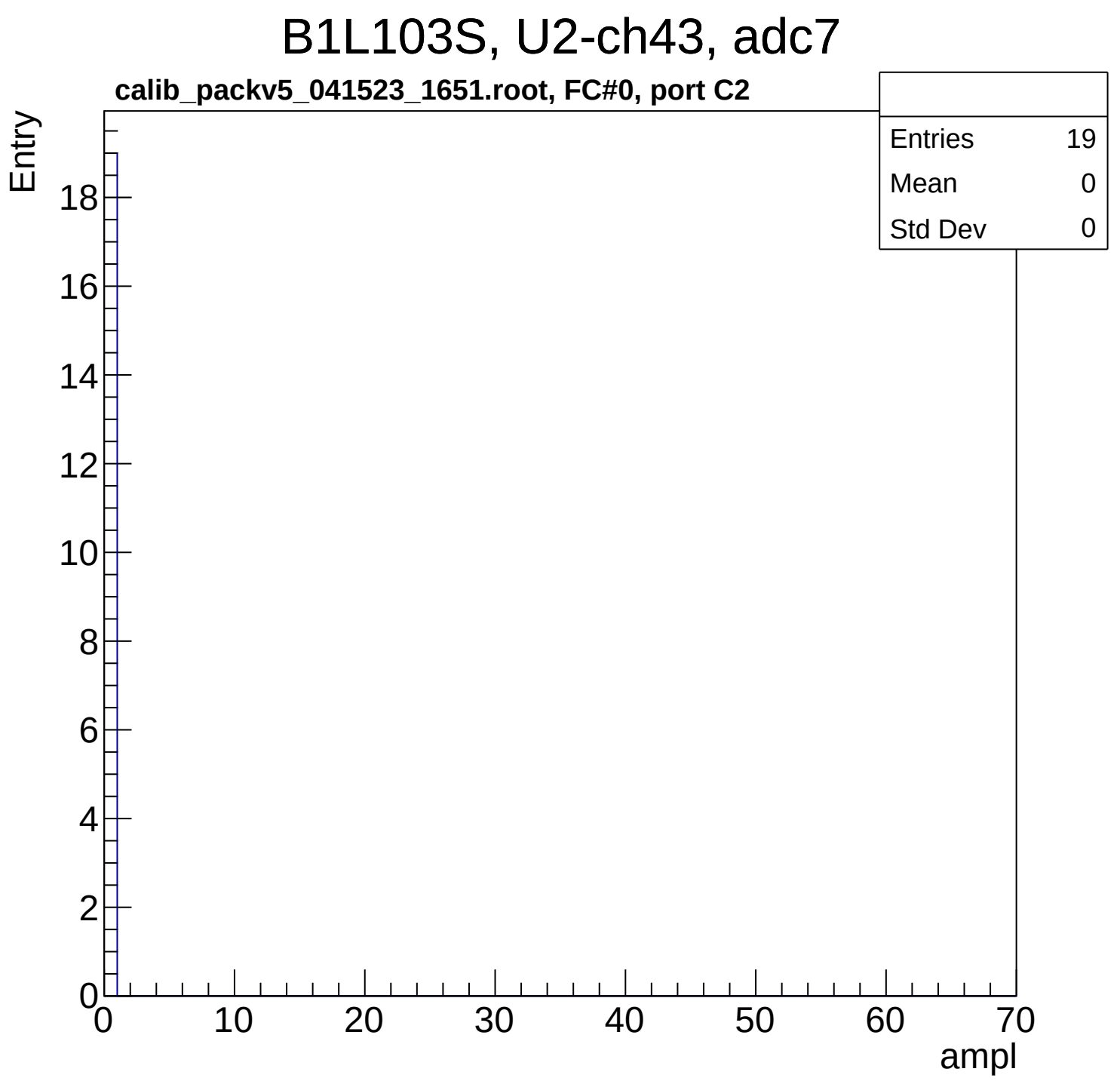

B1L103S, U2-ch43, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 40.67
Std Dev 6.73
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

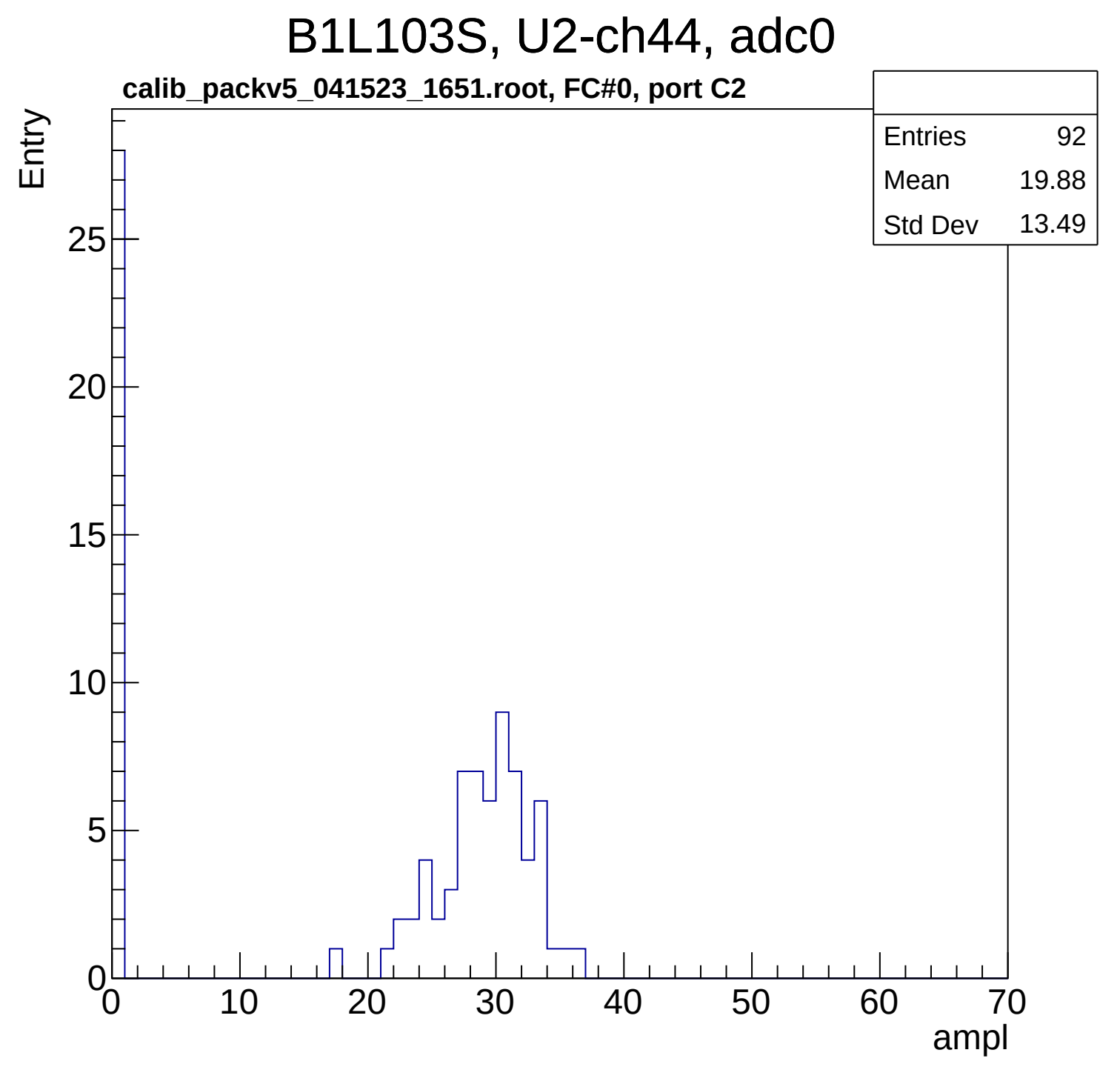

B1L103S, U2-ch43, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 47.29
Std Dev 2.893
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

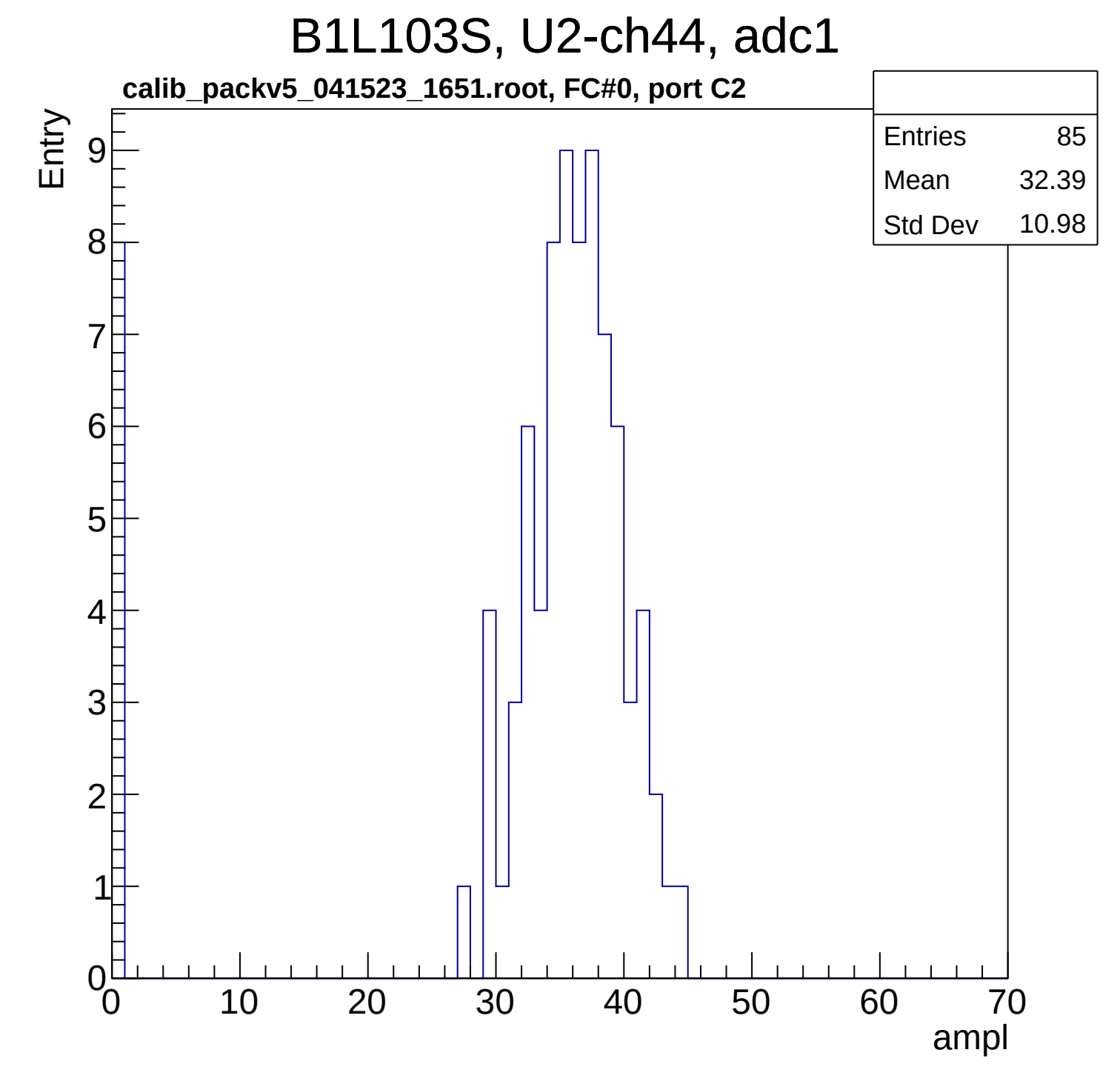

B1L103S, U2-ch43, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 52.59
Std Dev 7.713
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

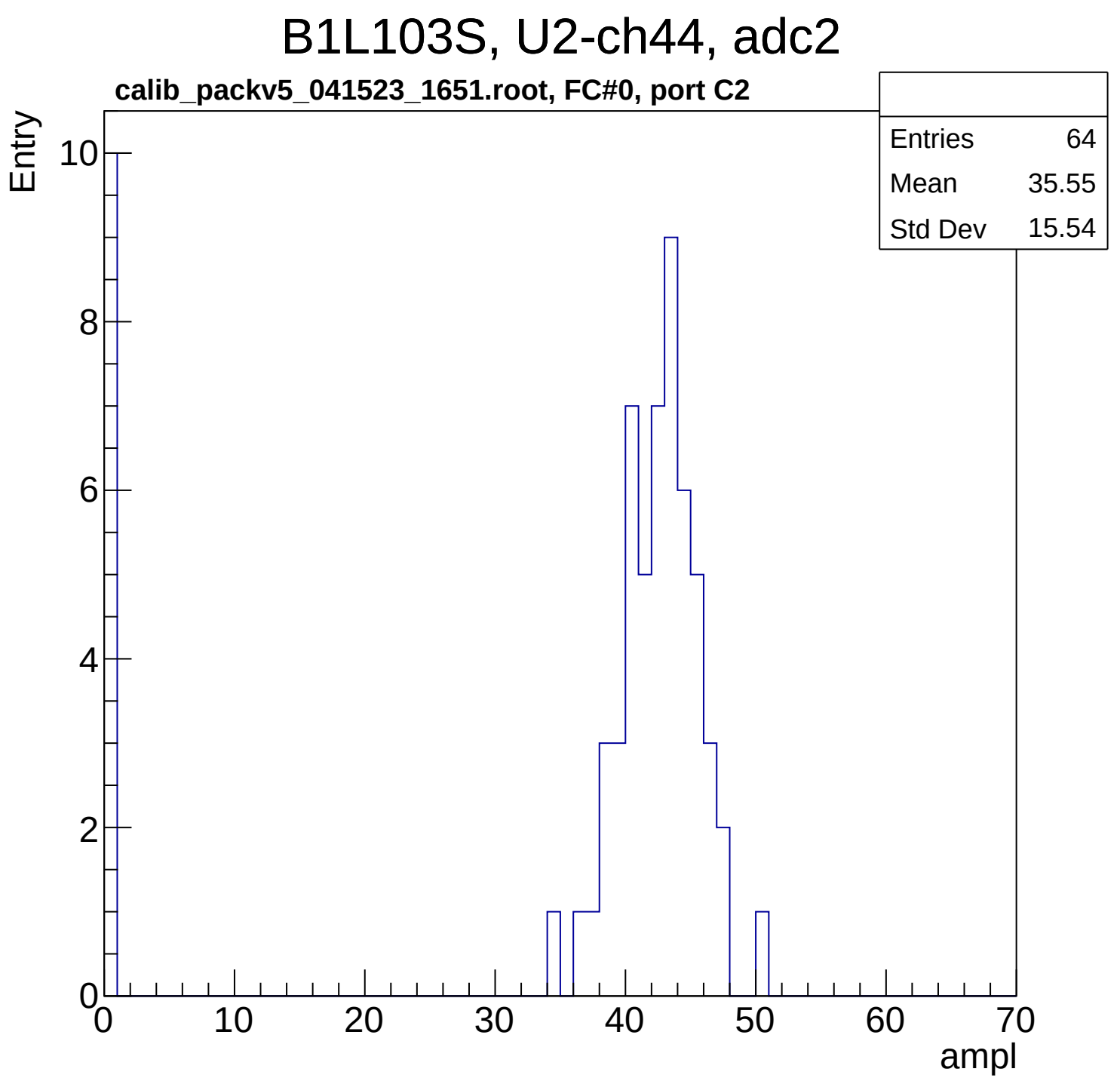

B1L103S, U2-ch43, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.46
Std Dev 3.117
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

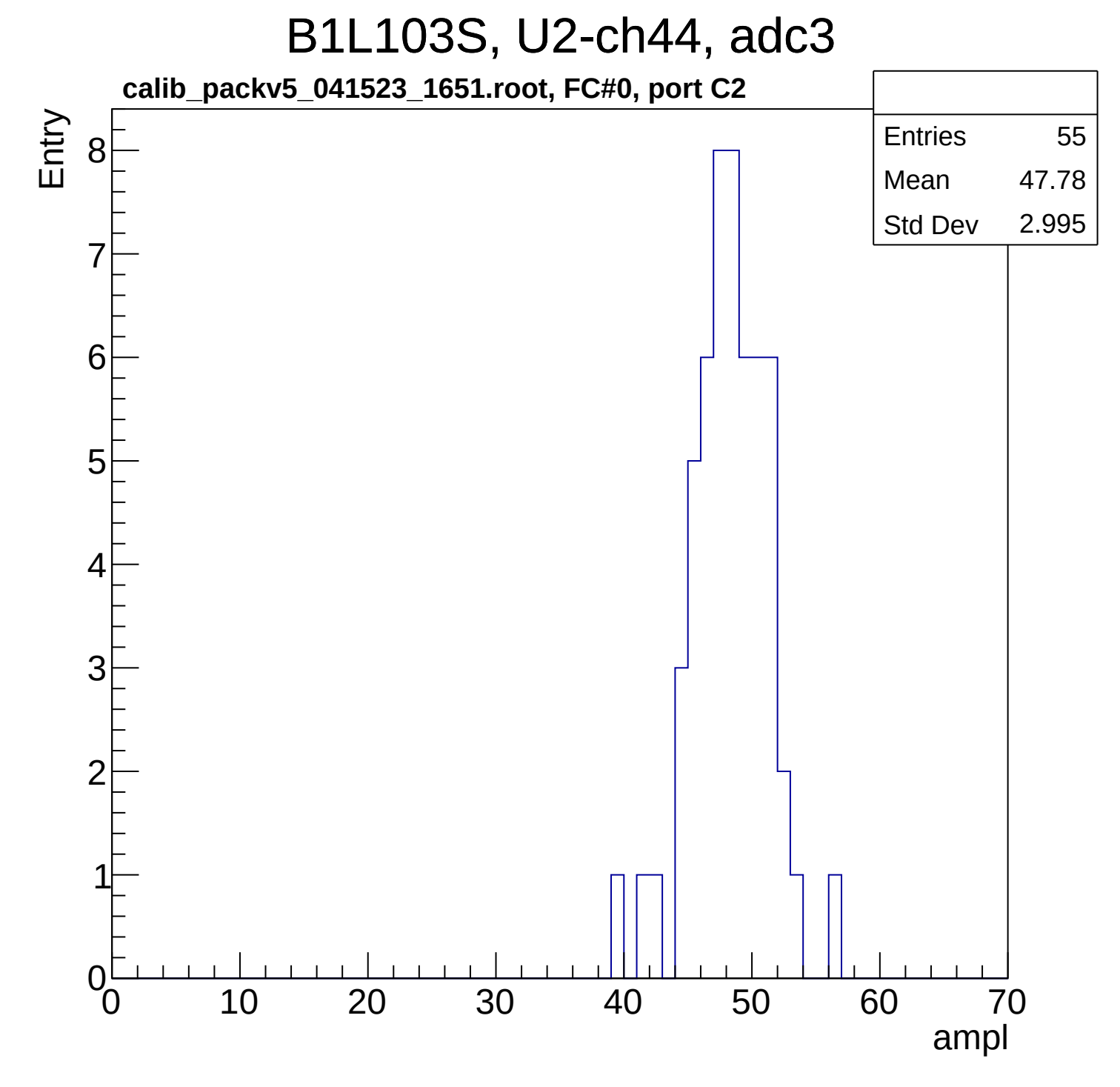

B1L103S, U2-ch43, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 57.78
Std Dev 14.08
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

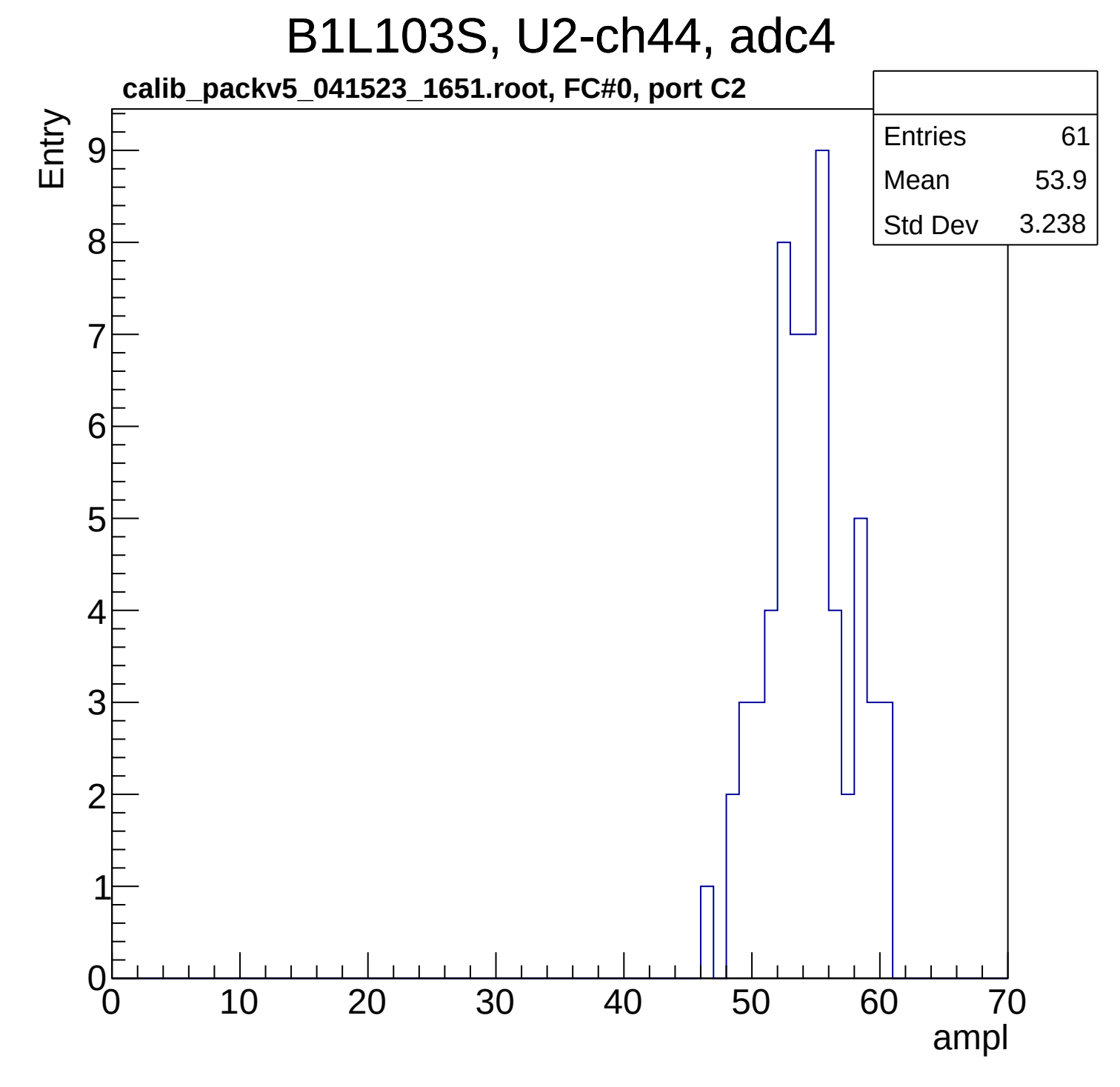

B1L103S, U2-ch43, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

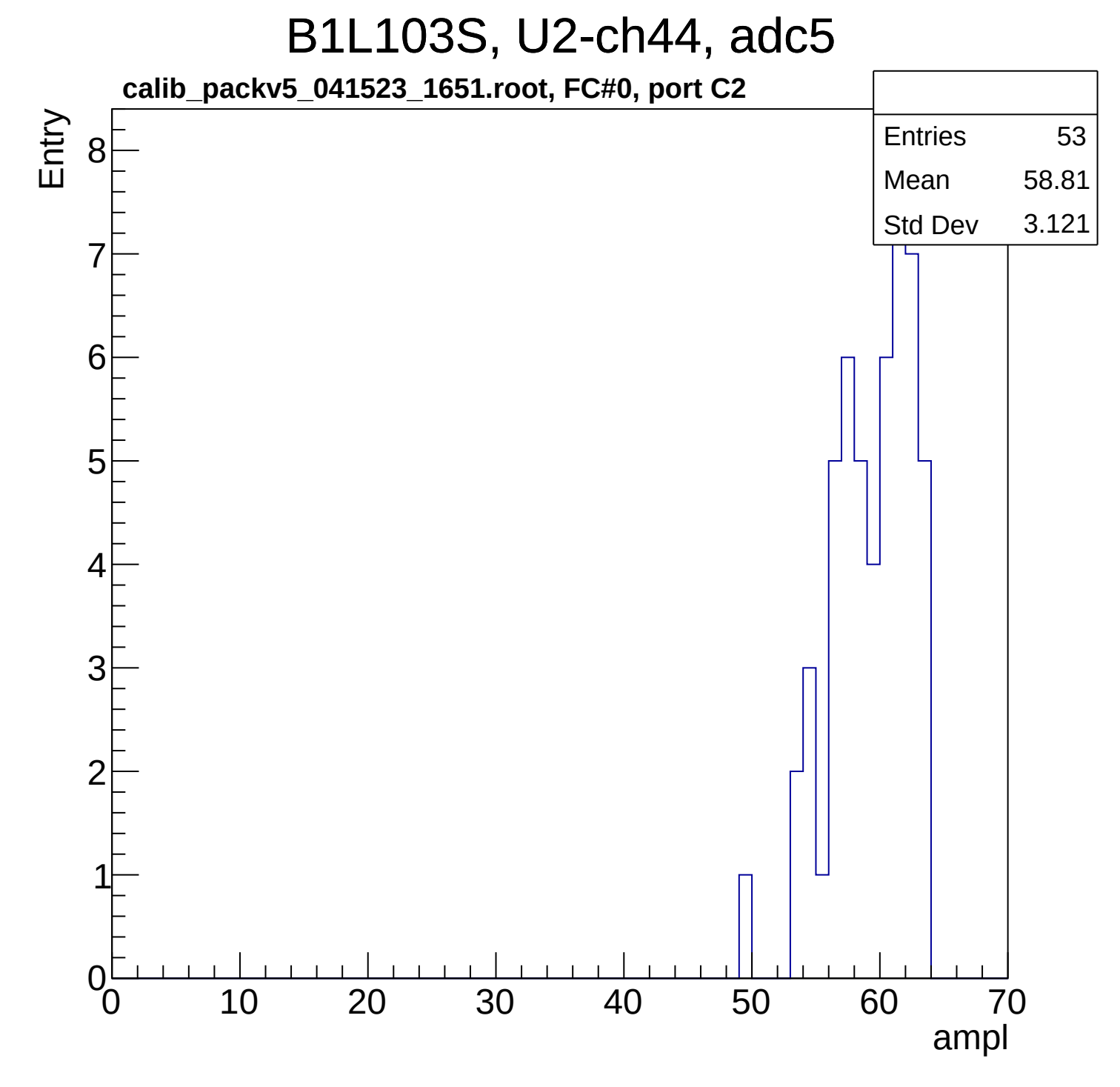

B1L103S, U2-ch44, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 19.88
Std Dev 13.49
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl

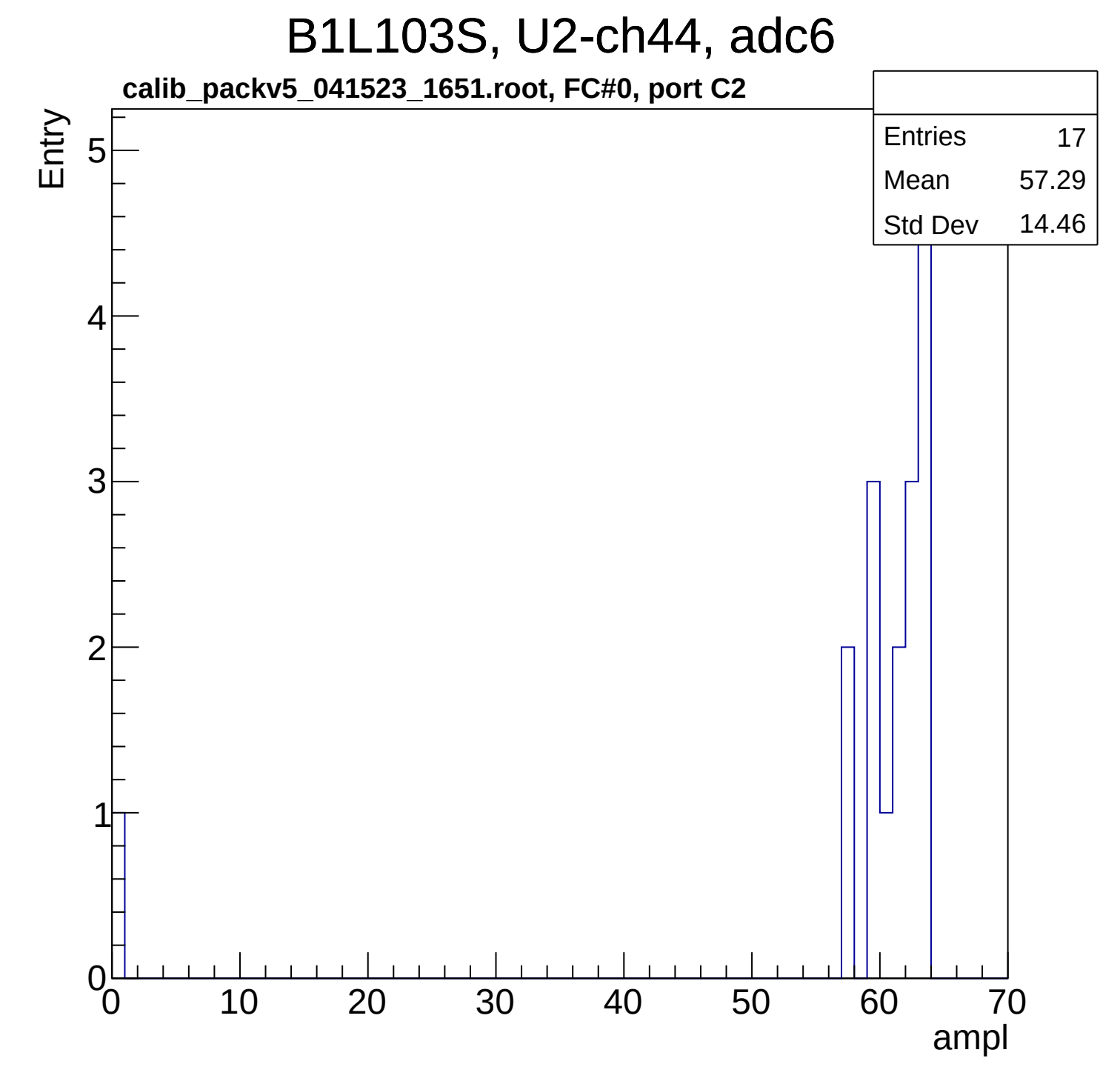

B1L103S, U2-ch44, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 32.39
Std Dev 10.98
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

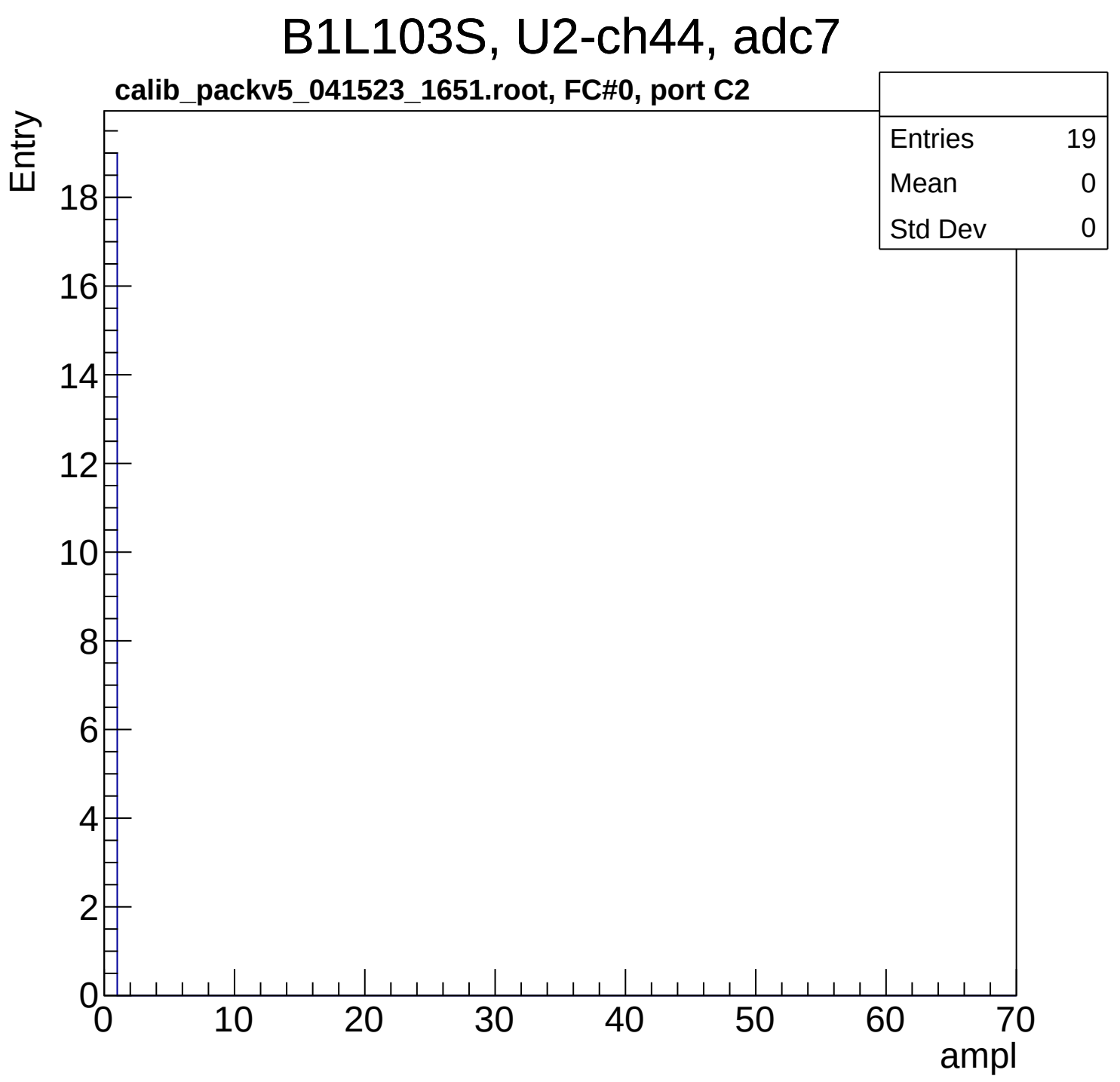

B1L103S, U2-ch44, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 35.55
Std Dev 15.54
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

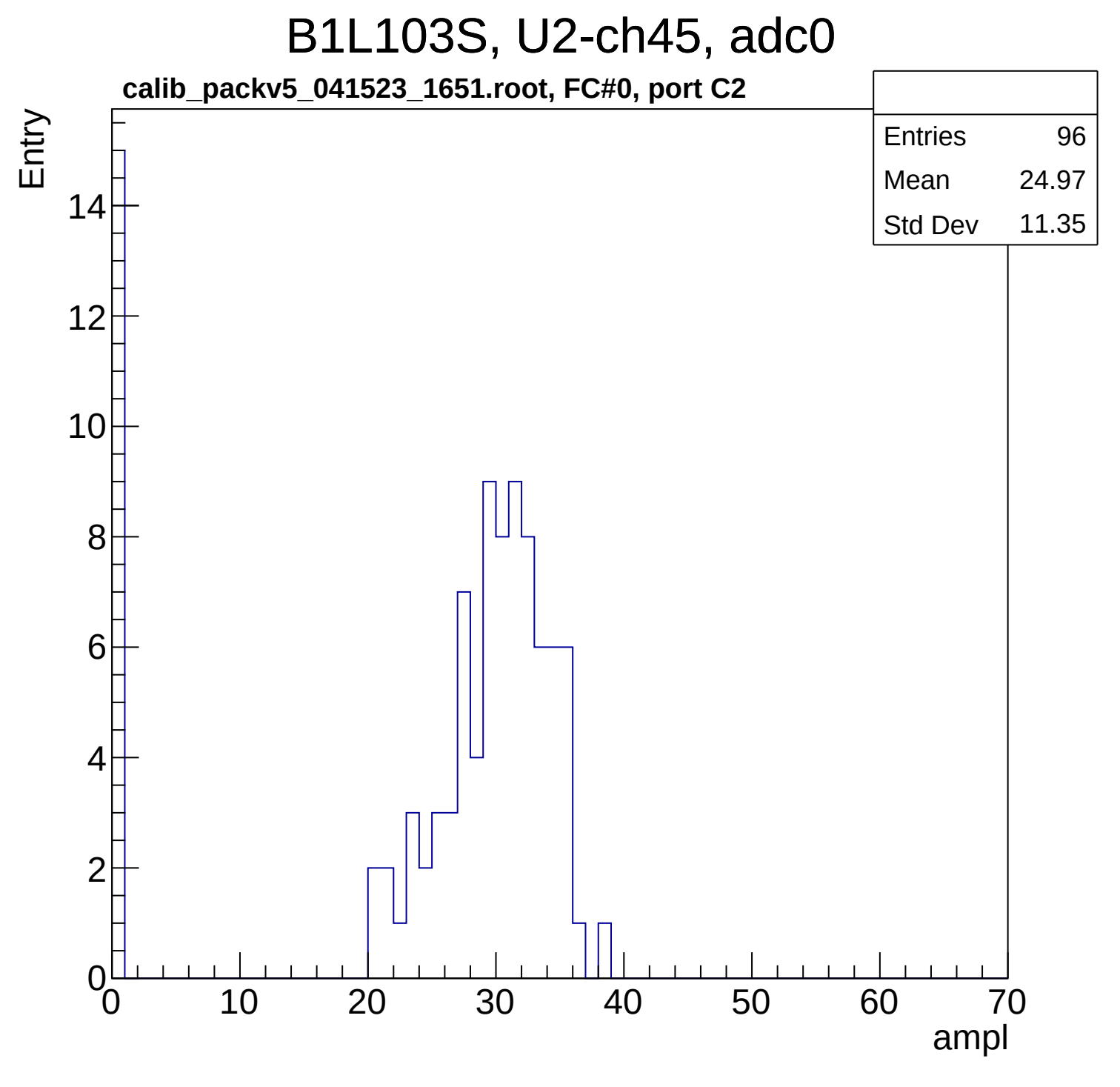

B1L103S, U2-ch44, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 47.78
Std Dev 2.995
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

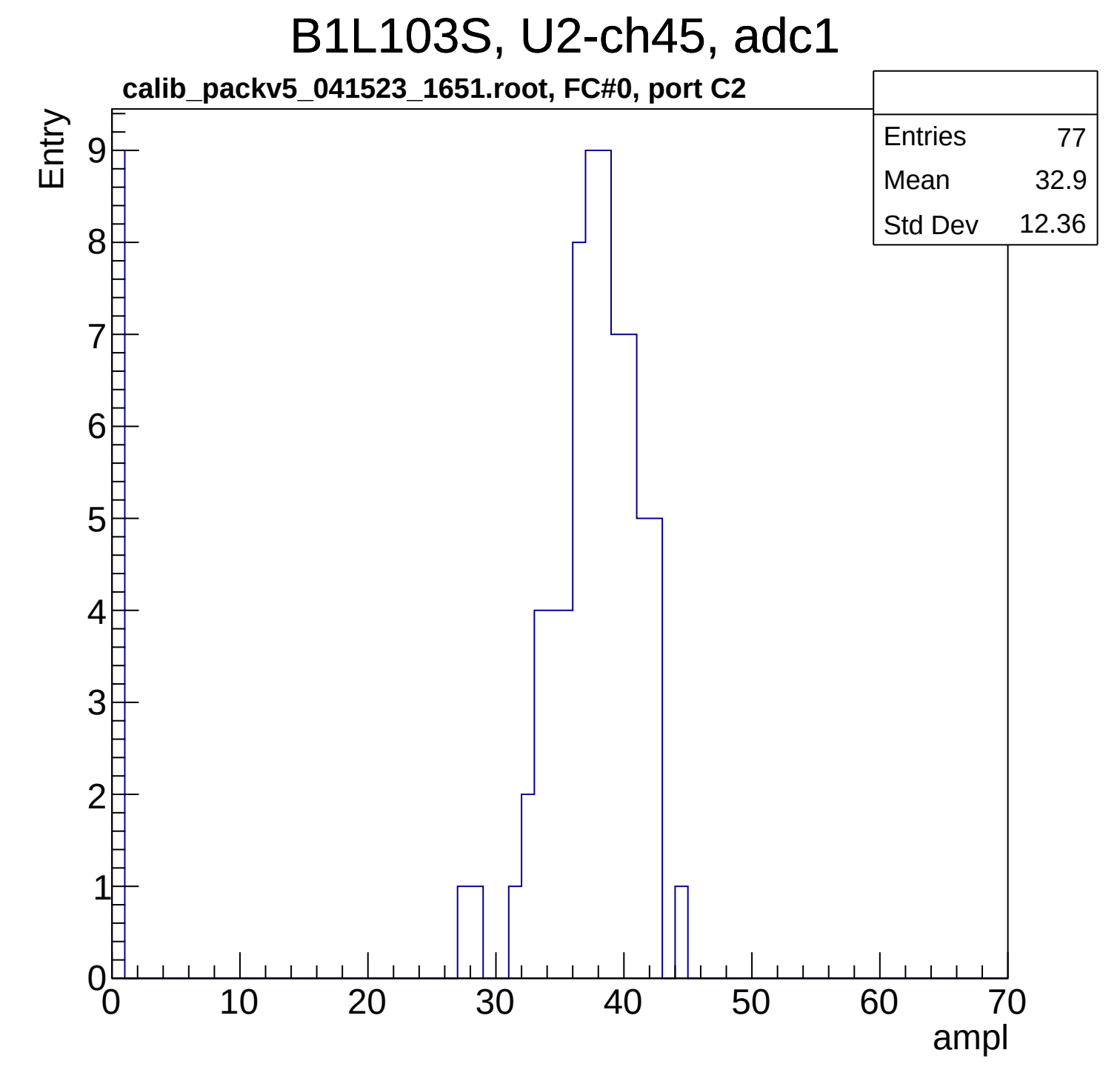

B1L103S, U2-ch44, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 53.9
Std Dev 3.238
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

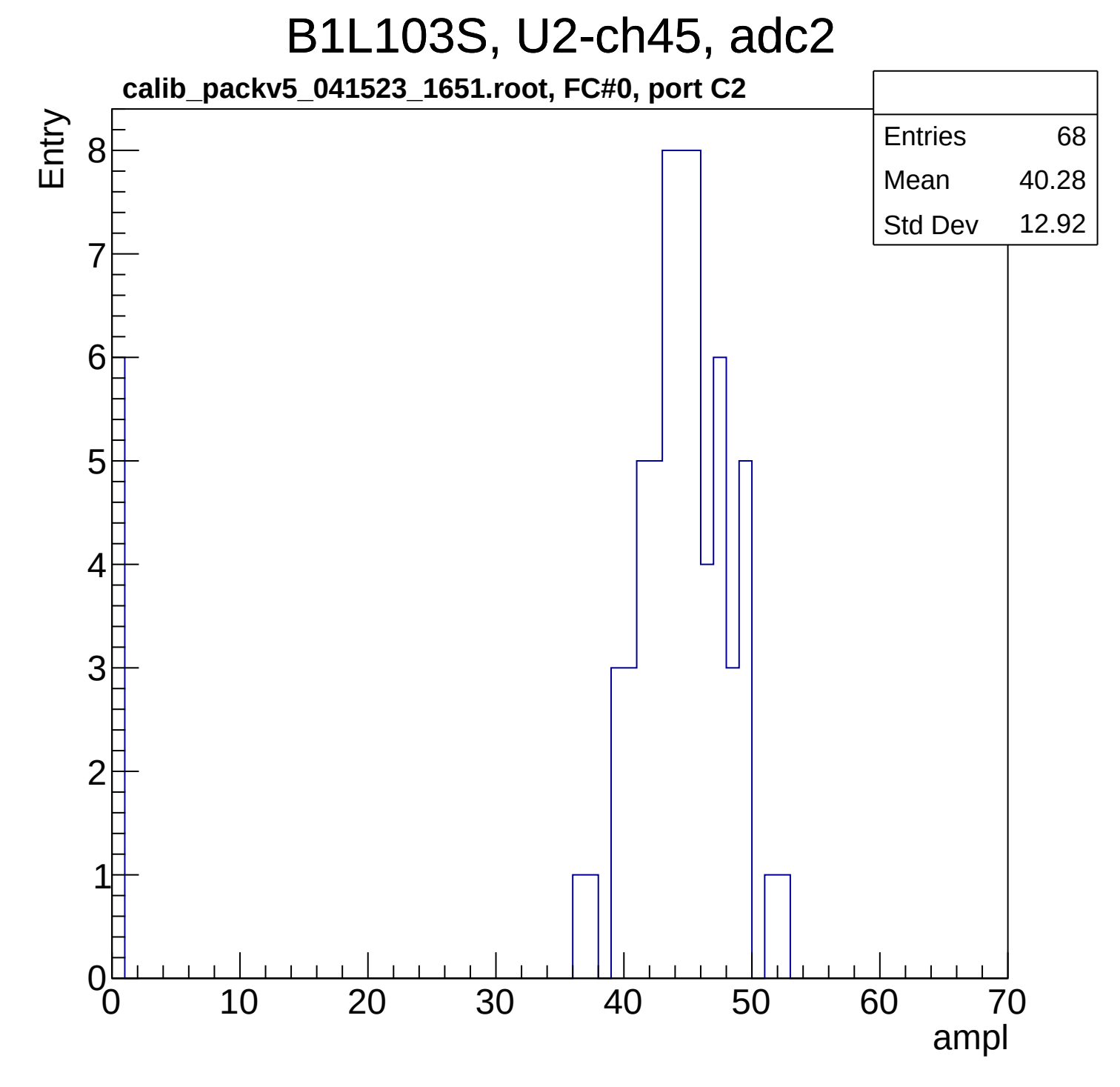

B1L103S, U2-ch44, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.81
Std Dev 3.121
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

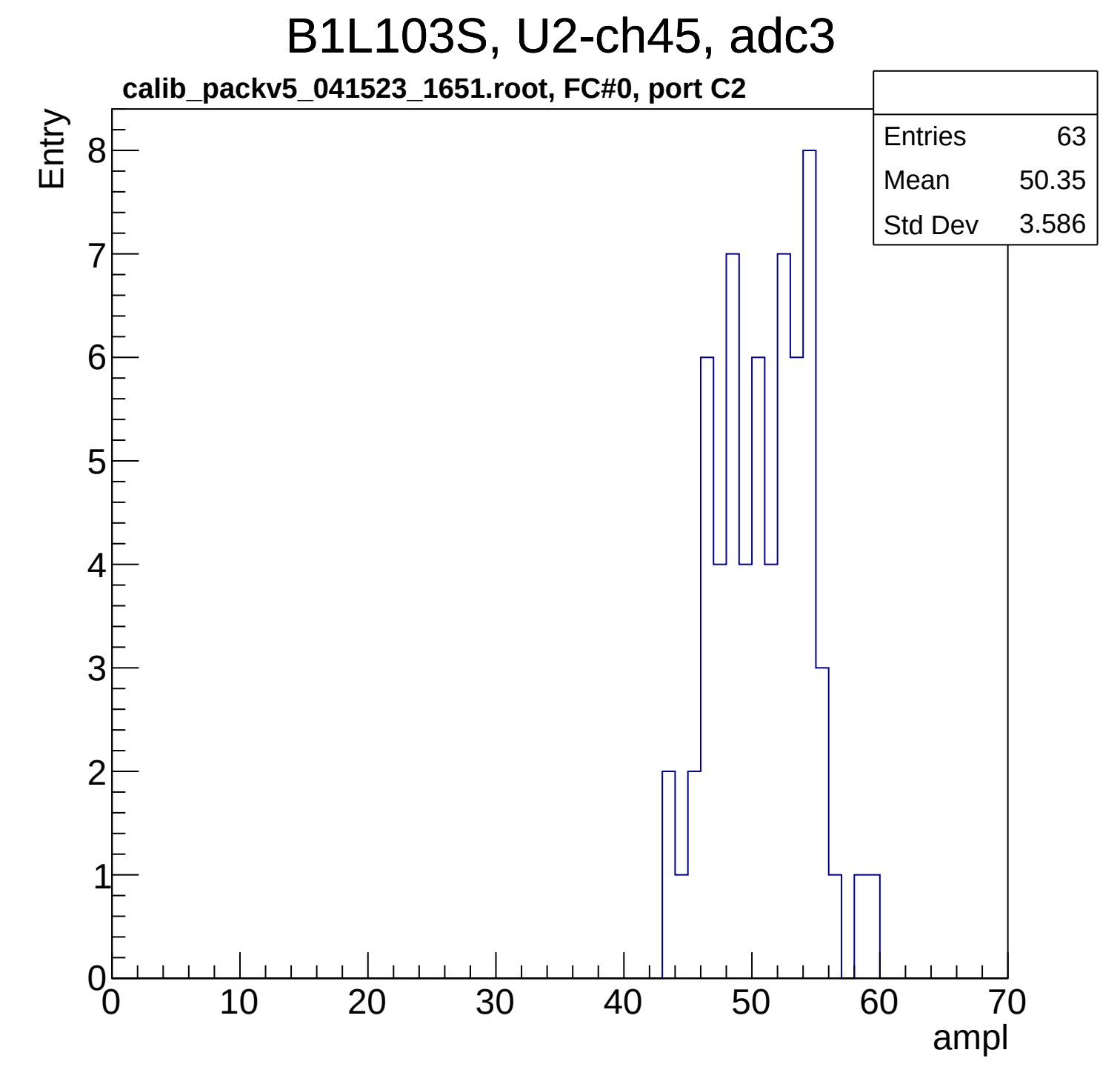

B1L103S, U2-ch44, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 57.29
Std Dev 14.46
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

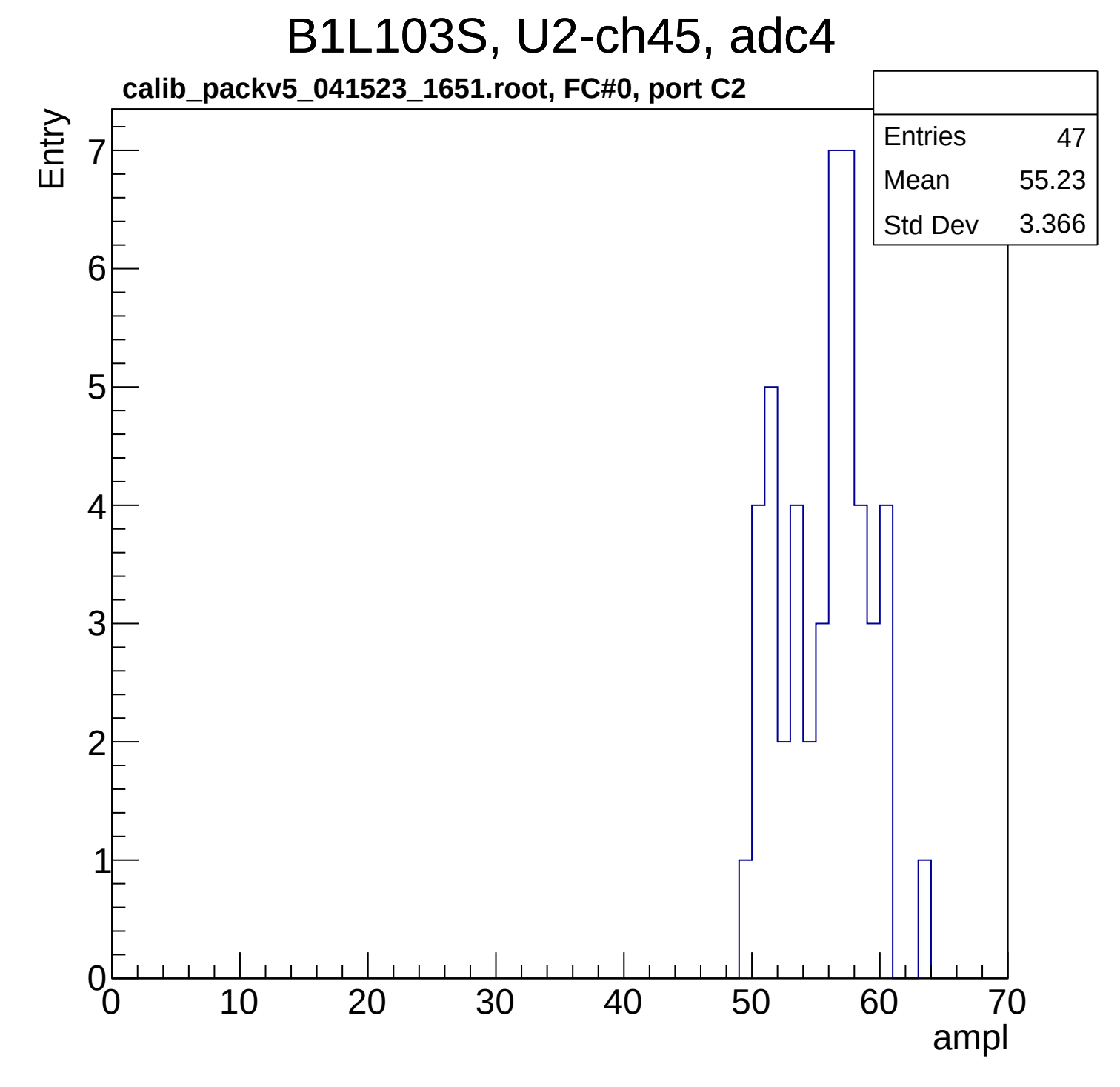

B1L103S, U2-ch44, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

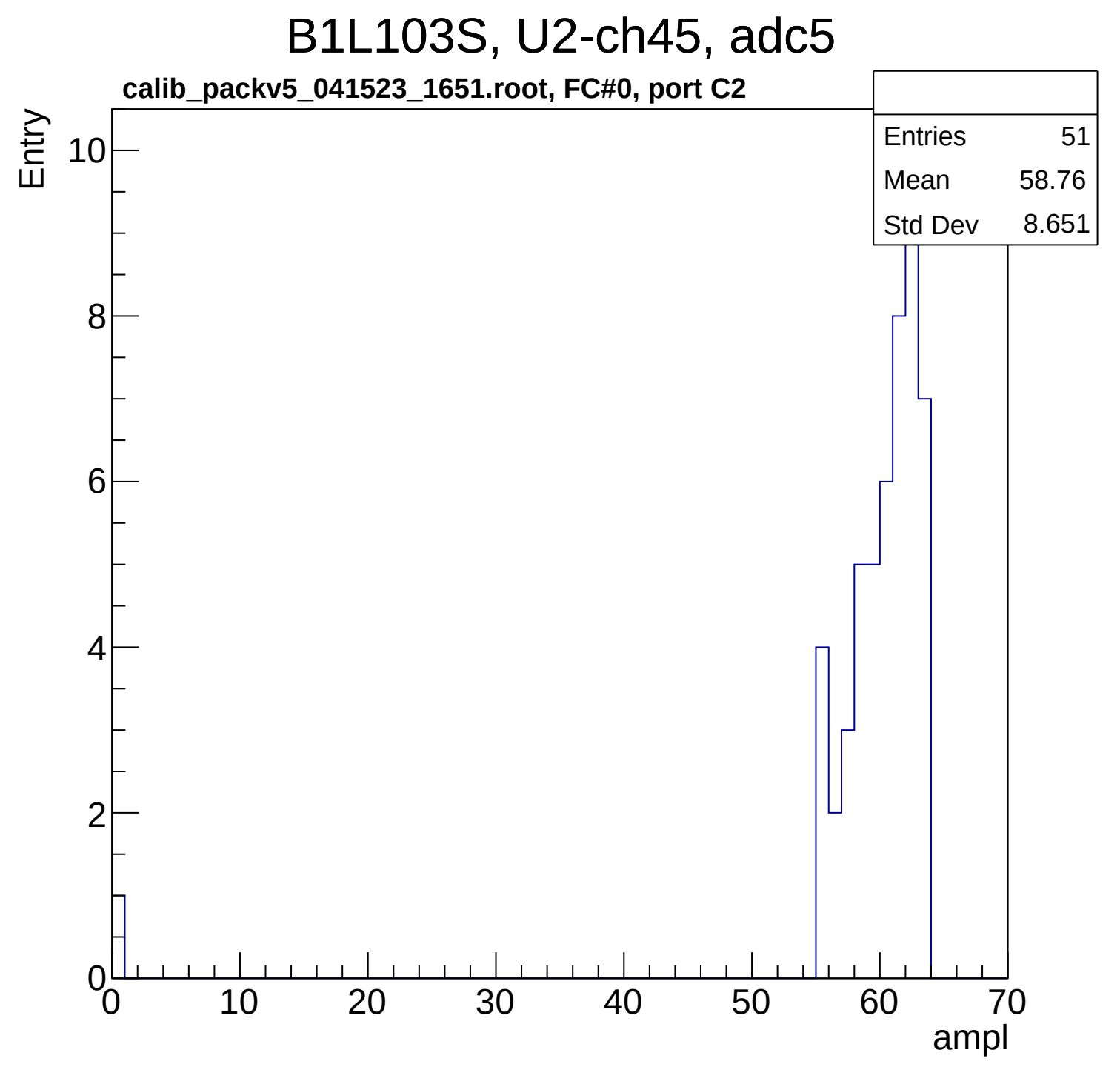

B1L103S, U2-ch45, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 24.97
Std Dev 11.35
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

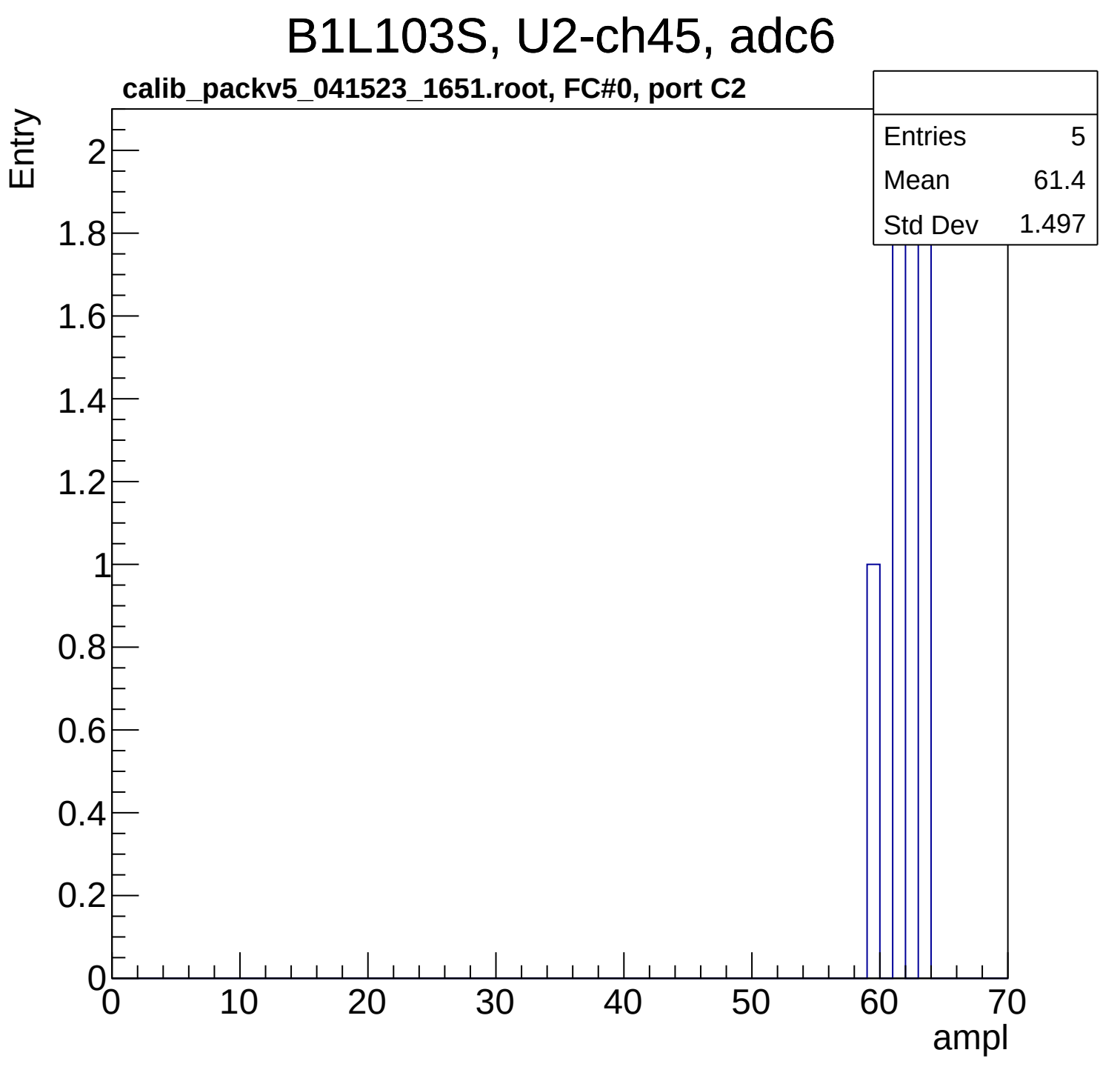

B1L103S, U2-ch45, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 32.9
Std Dev 12.36
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

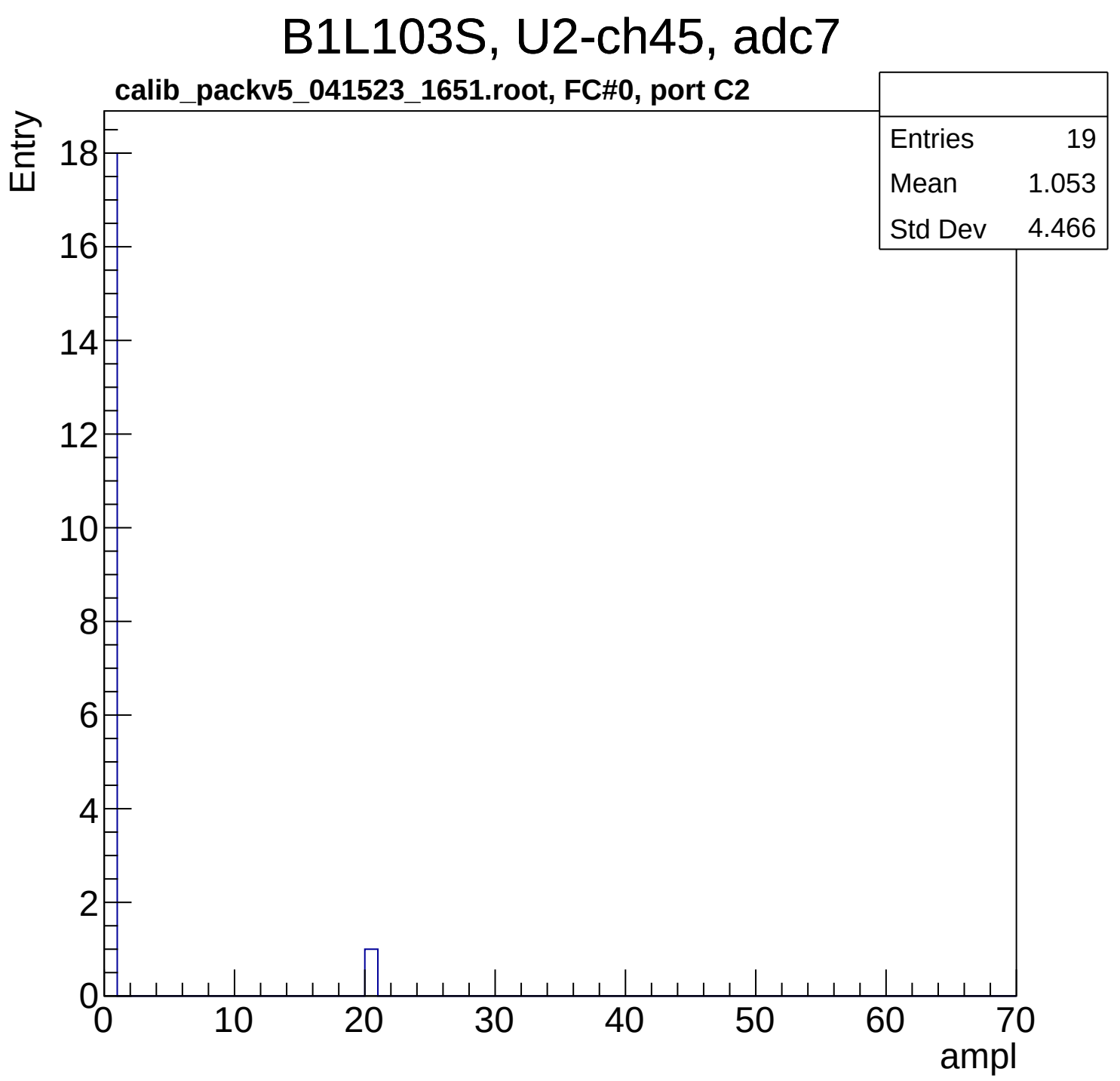

B1L103S, U2-ch45, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 40.28
Std Dev 12.92
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

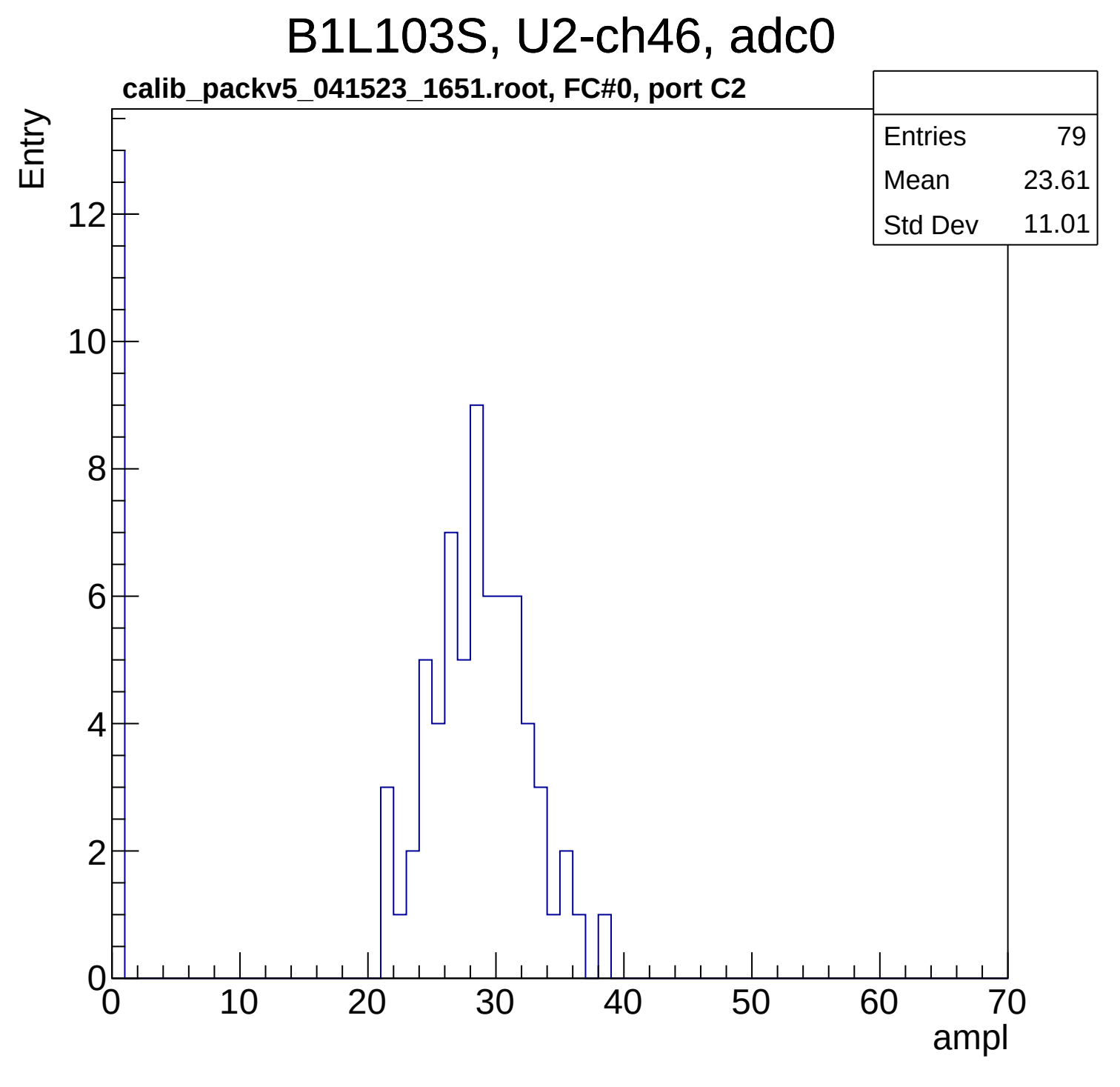

B1L103S, U2-ch45, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 50.35
Std Dev 3.586
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

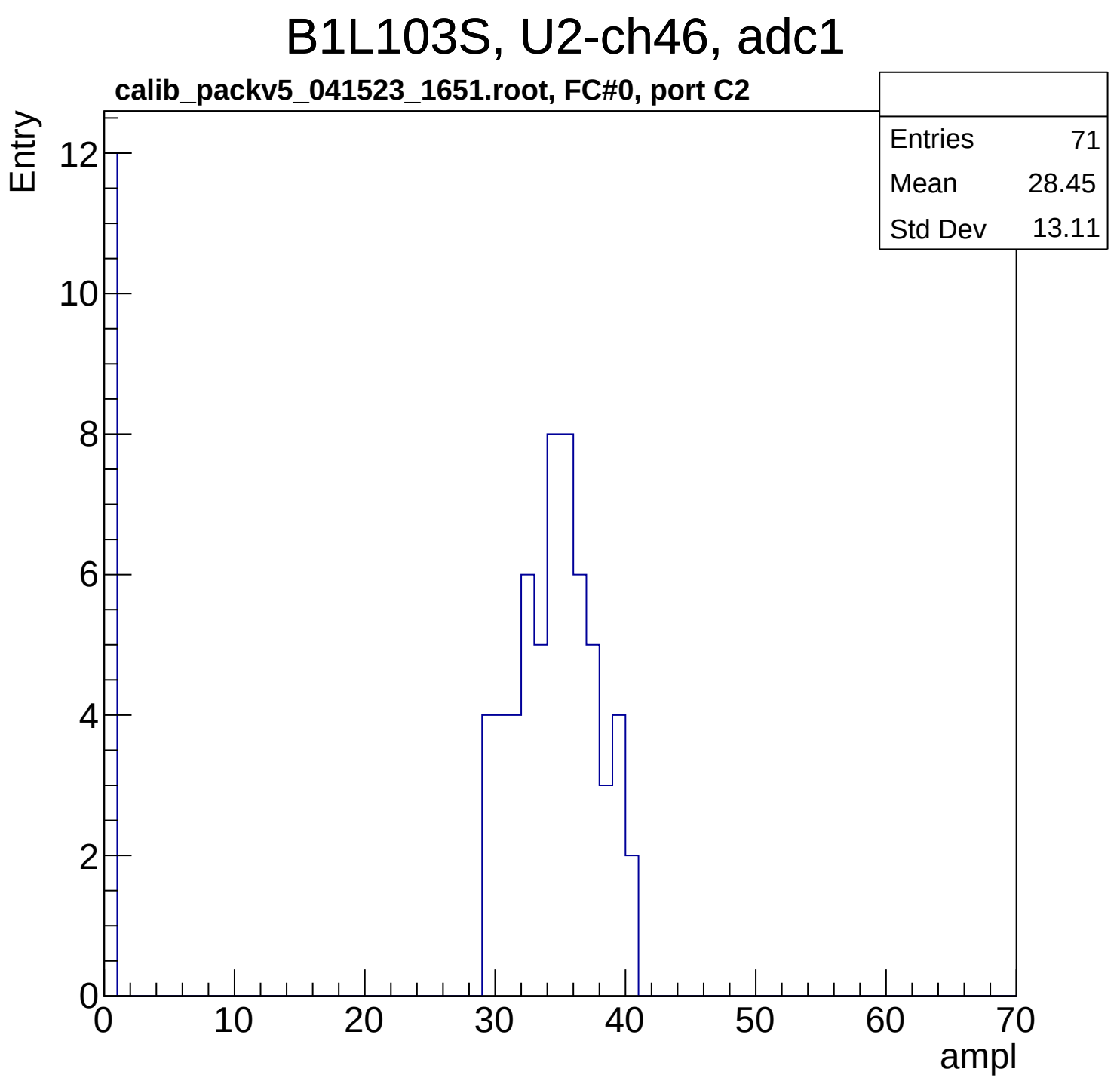

B1L103S, U2-ch45, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 55.23
Std Dev 3.366
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

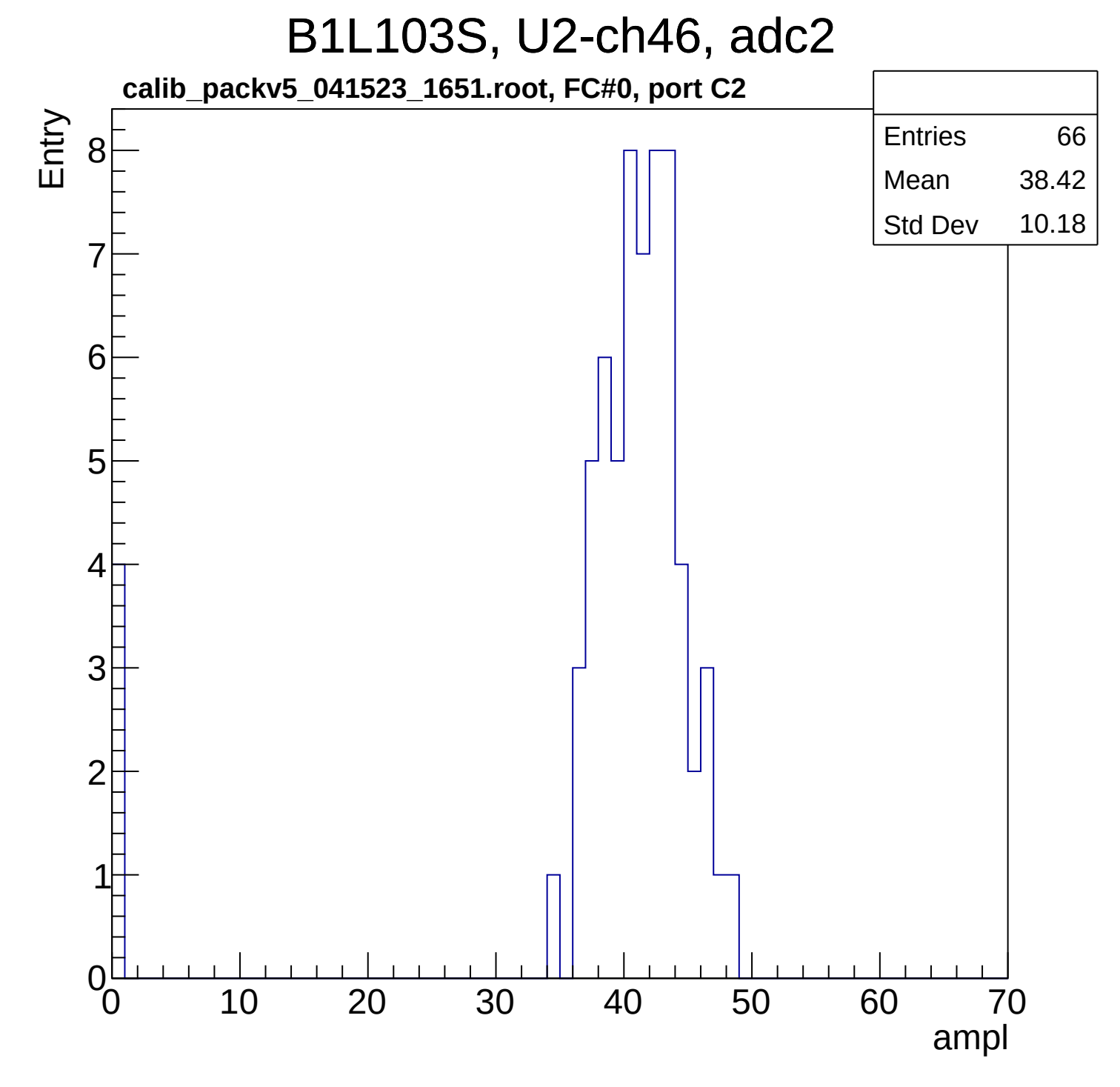

B1L103S, U2-ch45, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.76
Std Dev 8.651
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

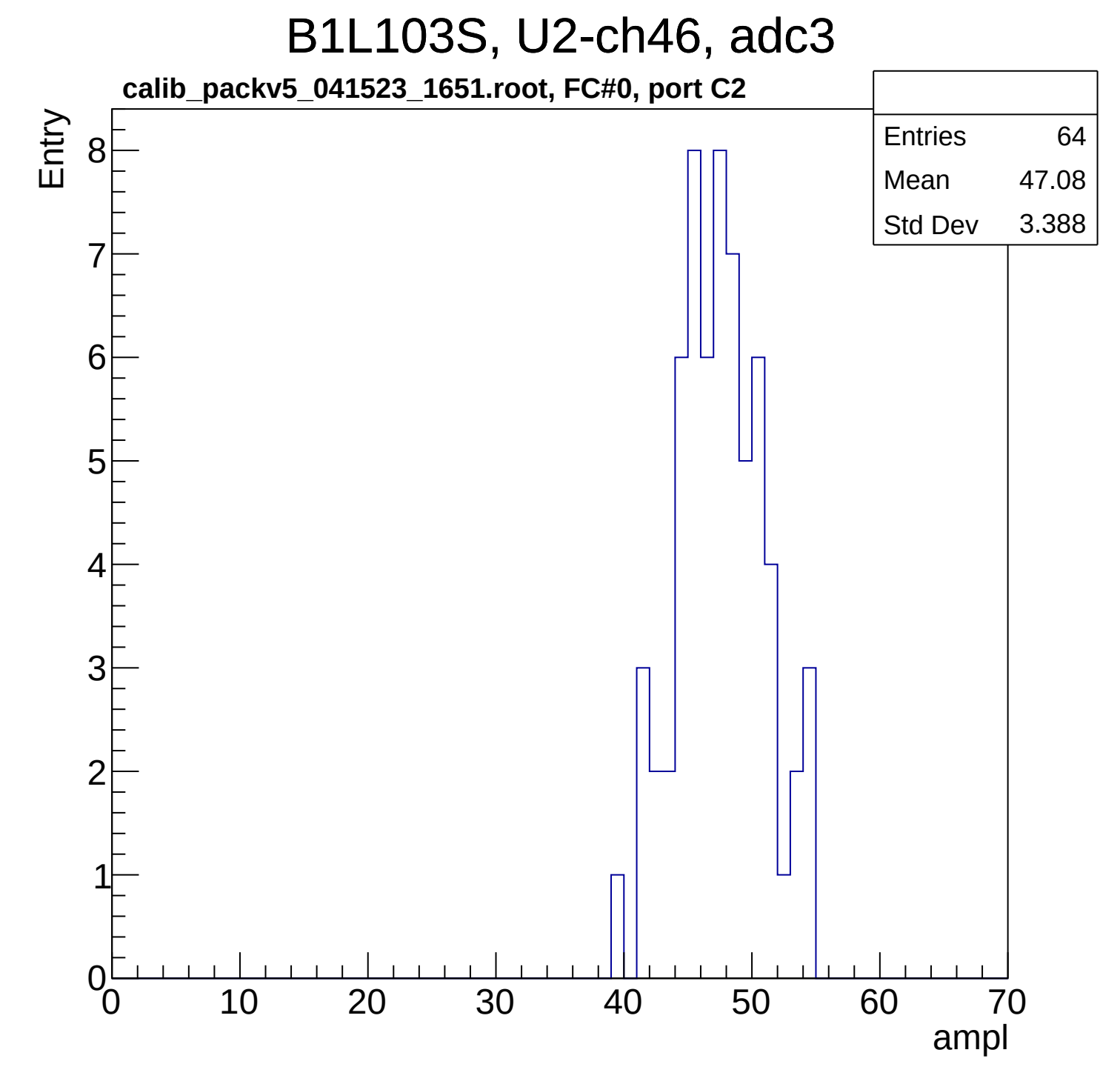

B1L103S, U2-ch45, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.4
Std Dev 1.497
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

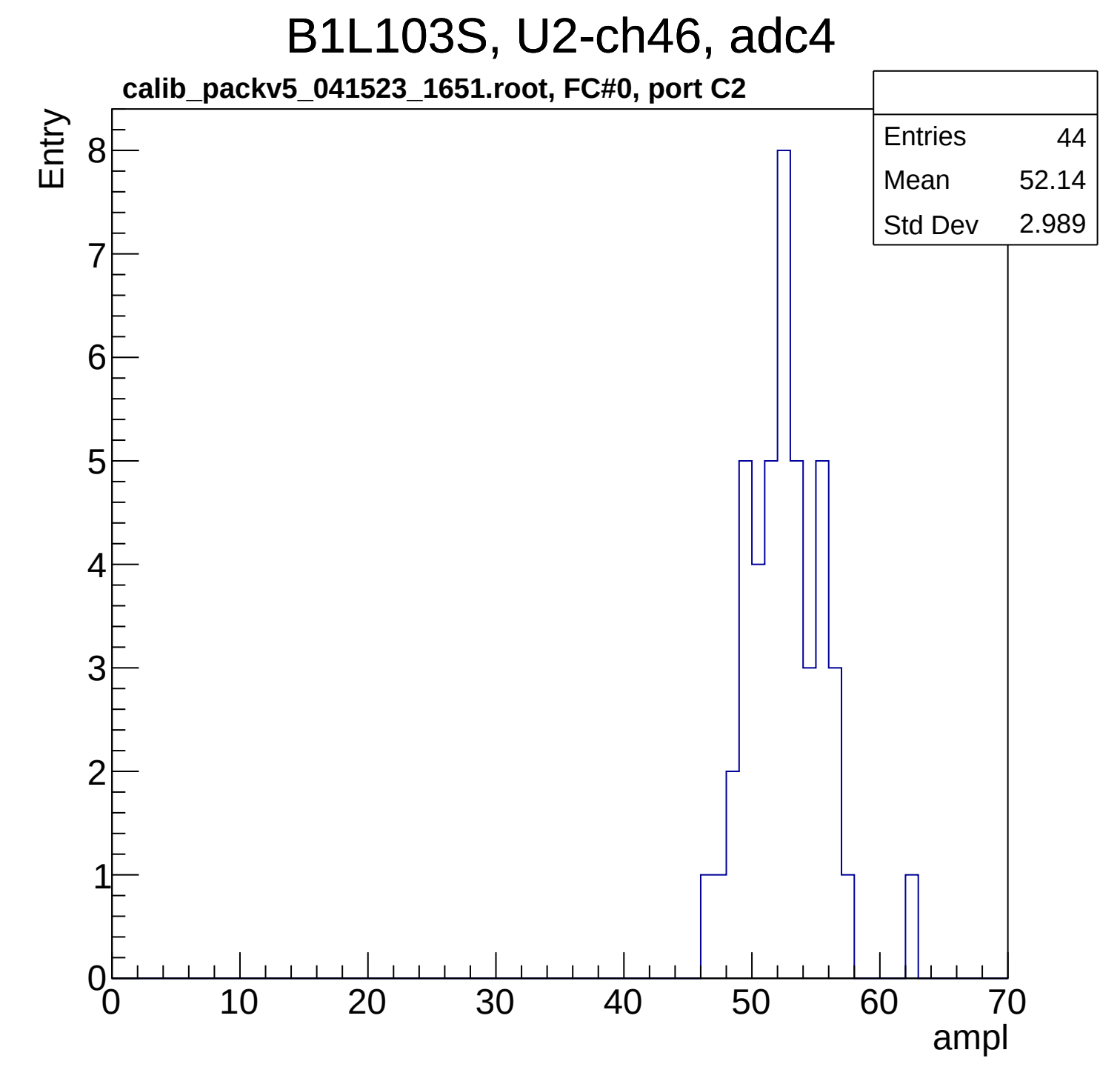

B1L103S, U2-ch45, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.053
Std Dev 4.466
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

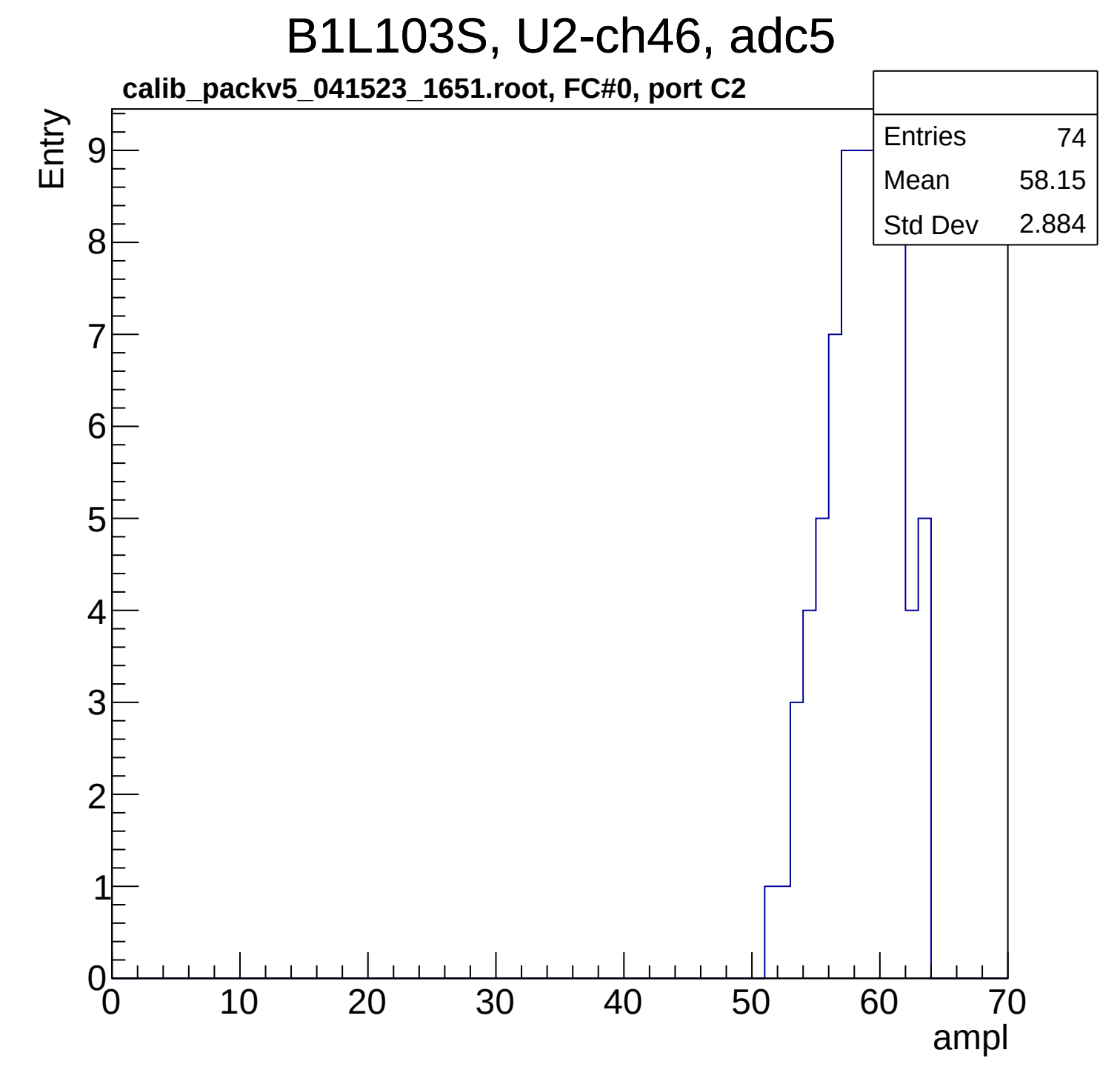

B1L103S, U2-ch46, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 23.61
Std Dev 11.01
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

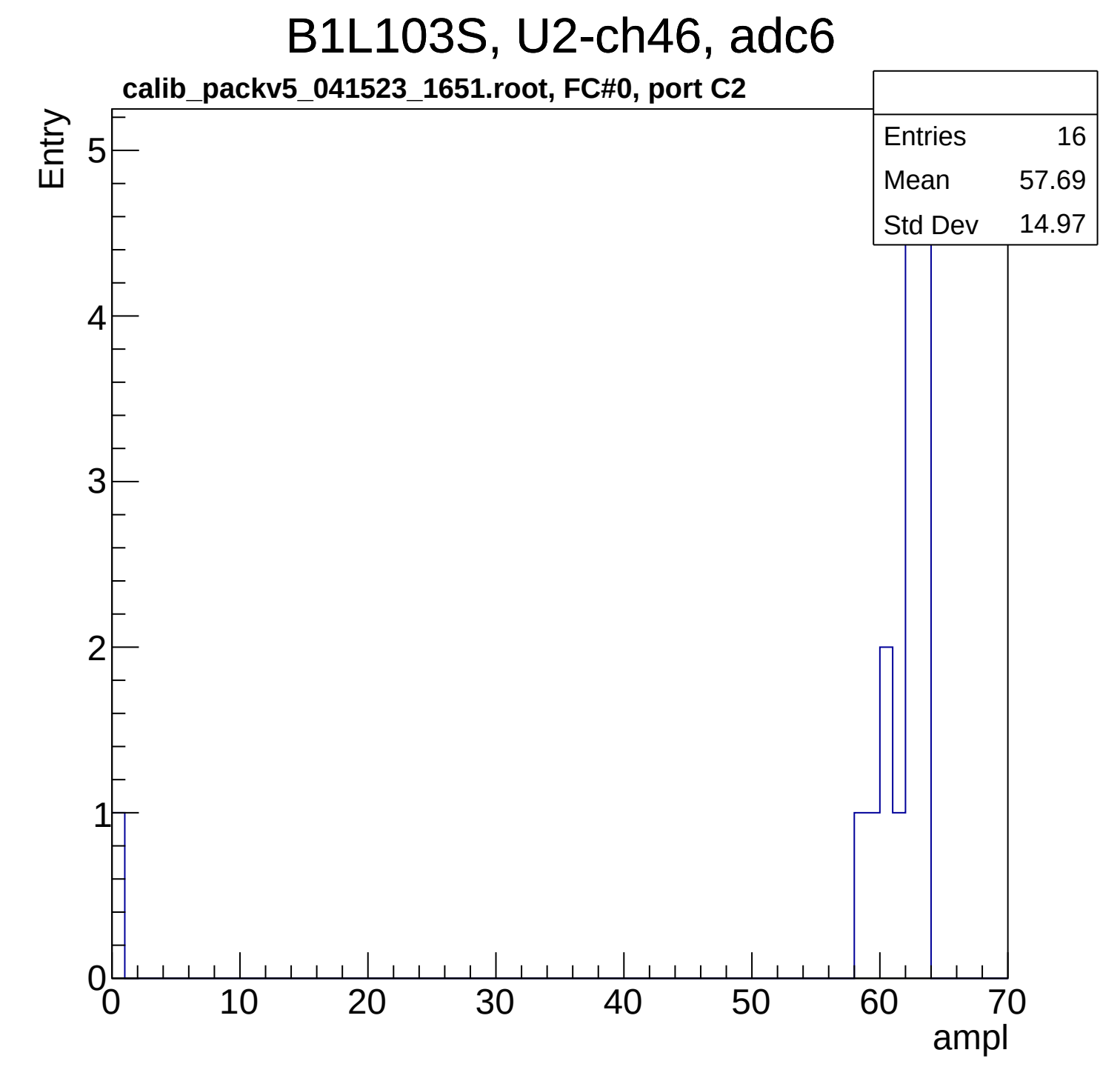

B1L103S, U2-ch46, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 28.45
Std Dev 13.11
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

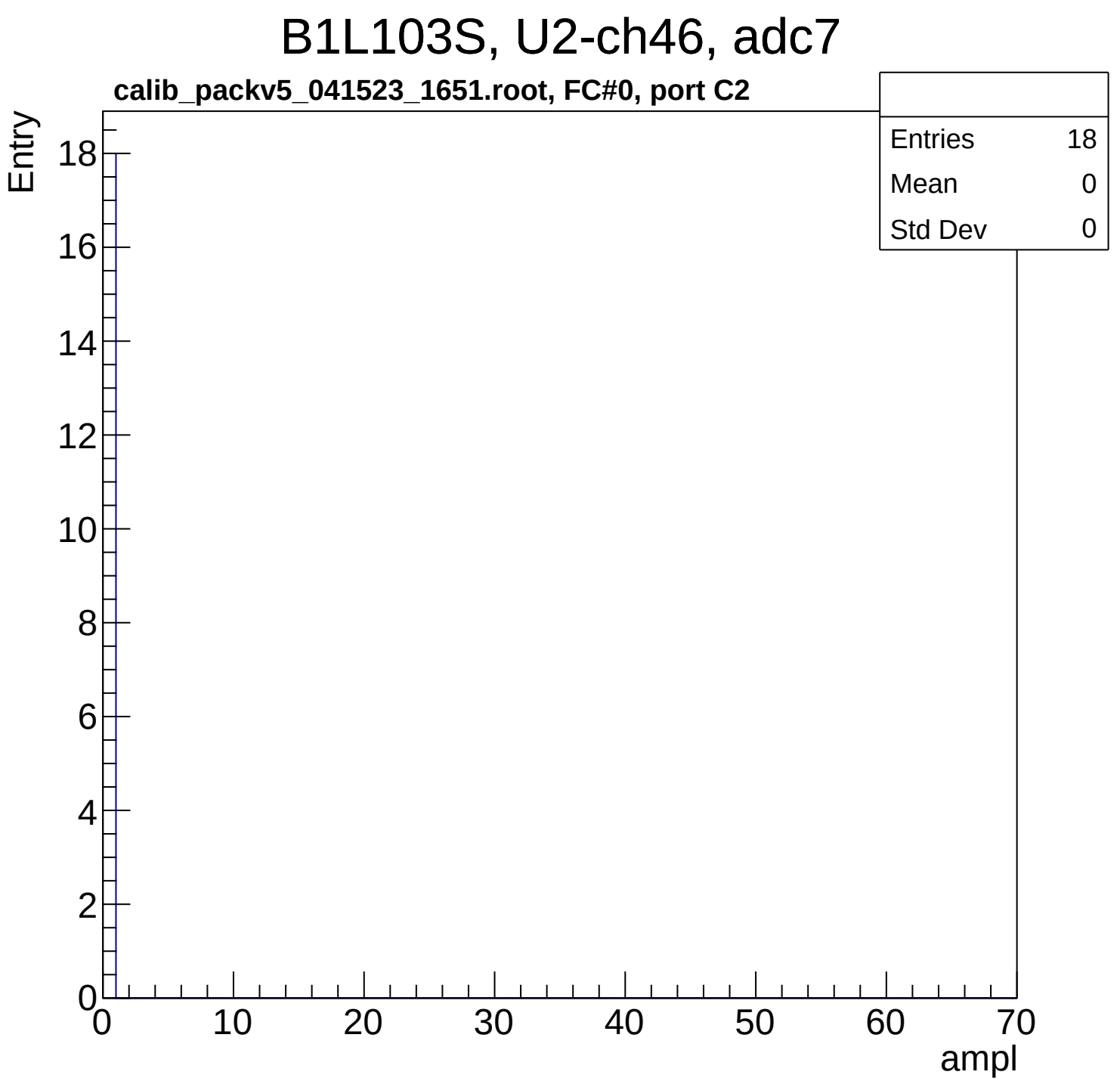

B1L103S, U2-ch46, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 38.42
Std Dev 10.18
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

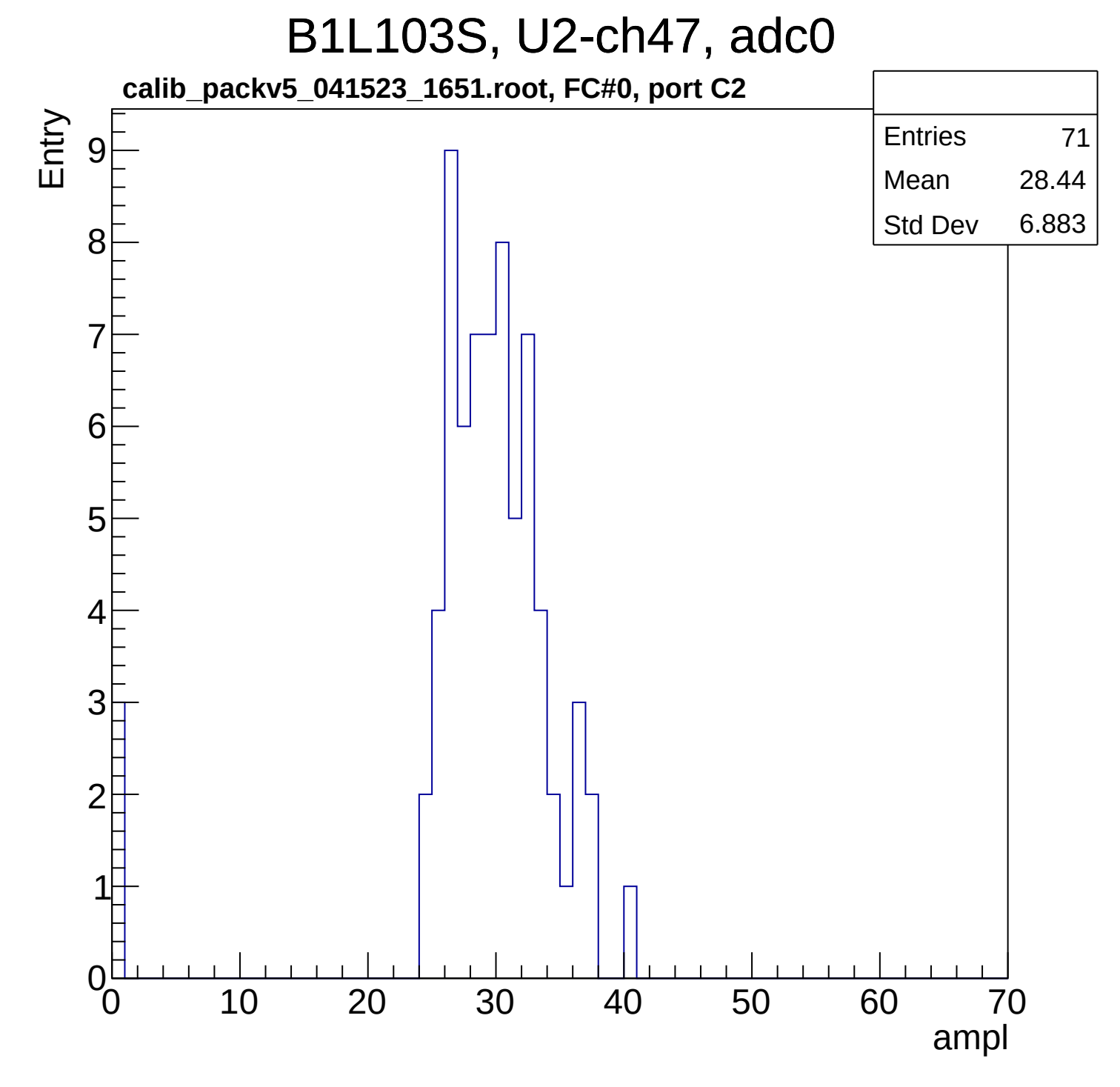

B1L103S, U2-ch46, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 47.08
Std Dev 3.388
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

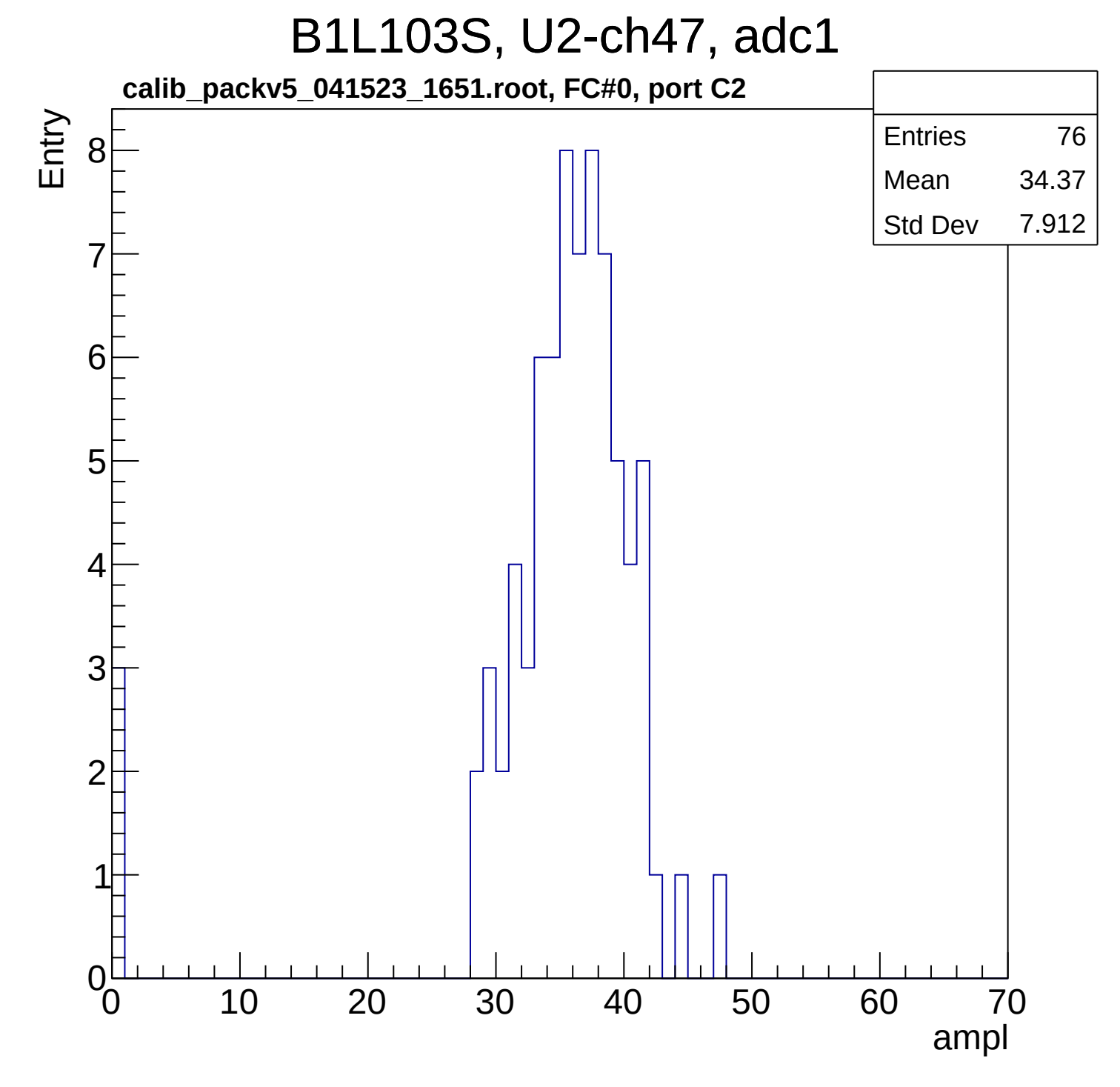

B1L103S, U2-ch46, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 52.14
Std Dev 2.989
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

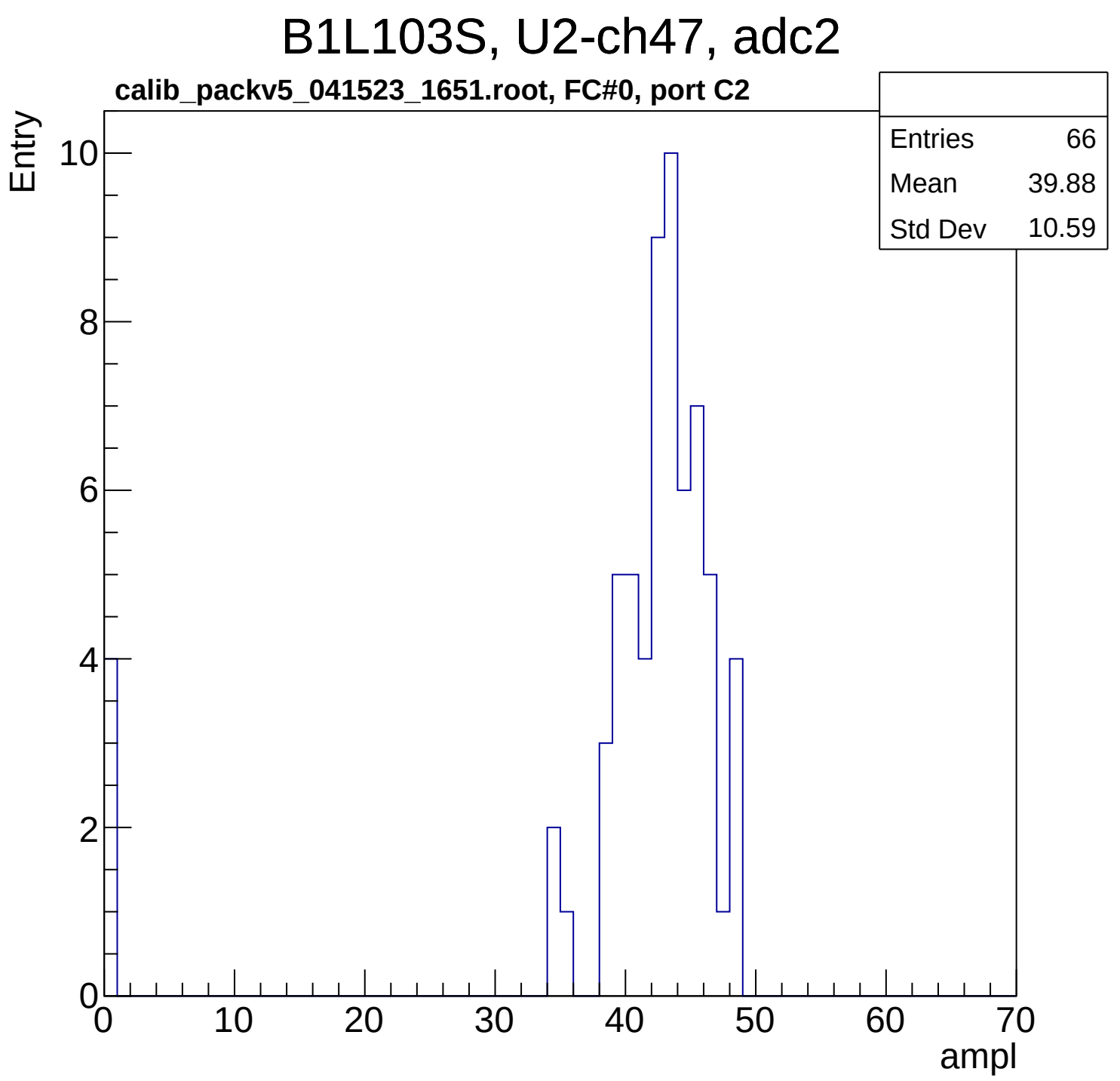

B1L103S, U2-ch46, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 58.15
Std Dev 2.884
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

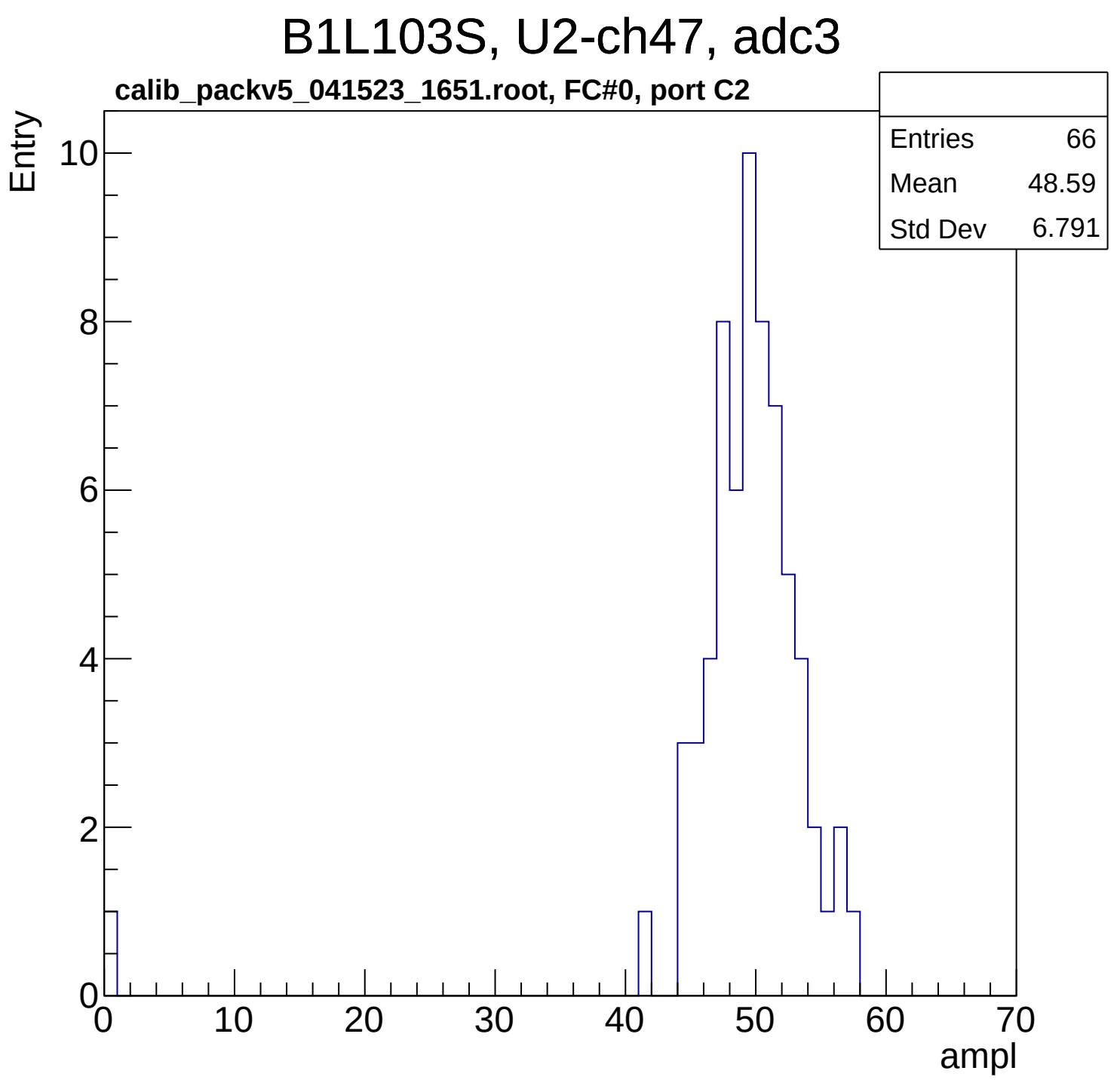

B1L103S, U2-ch46, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.69
Std Dev 14.97
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

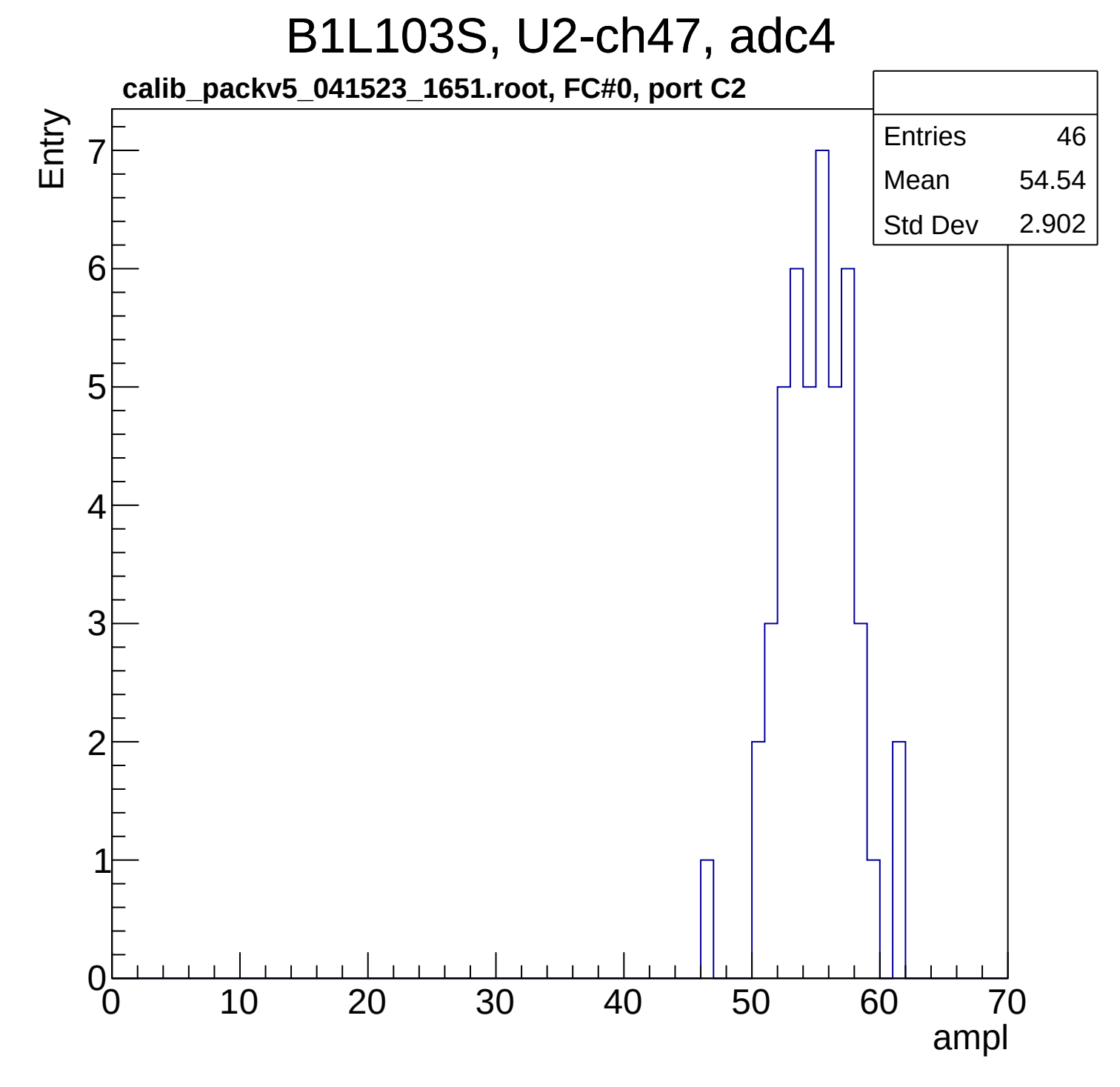

B1L103S, U2-ch46, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

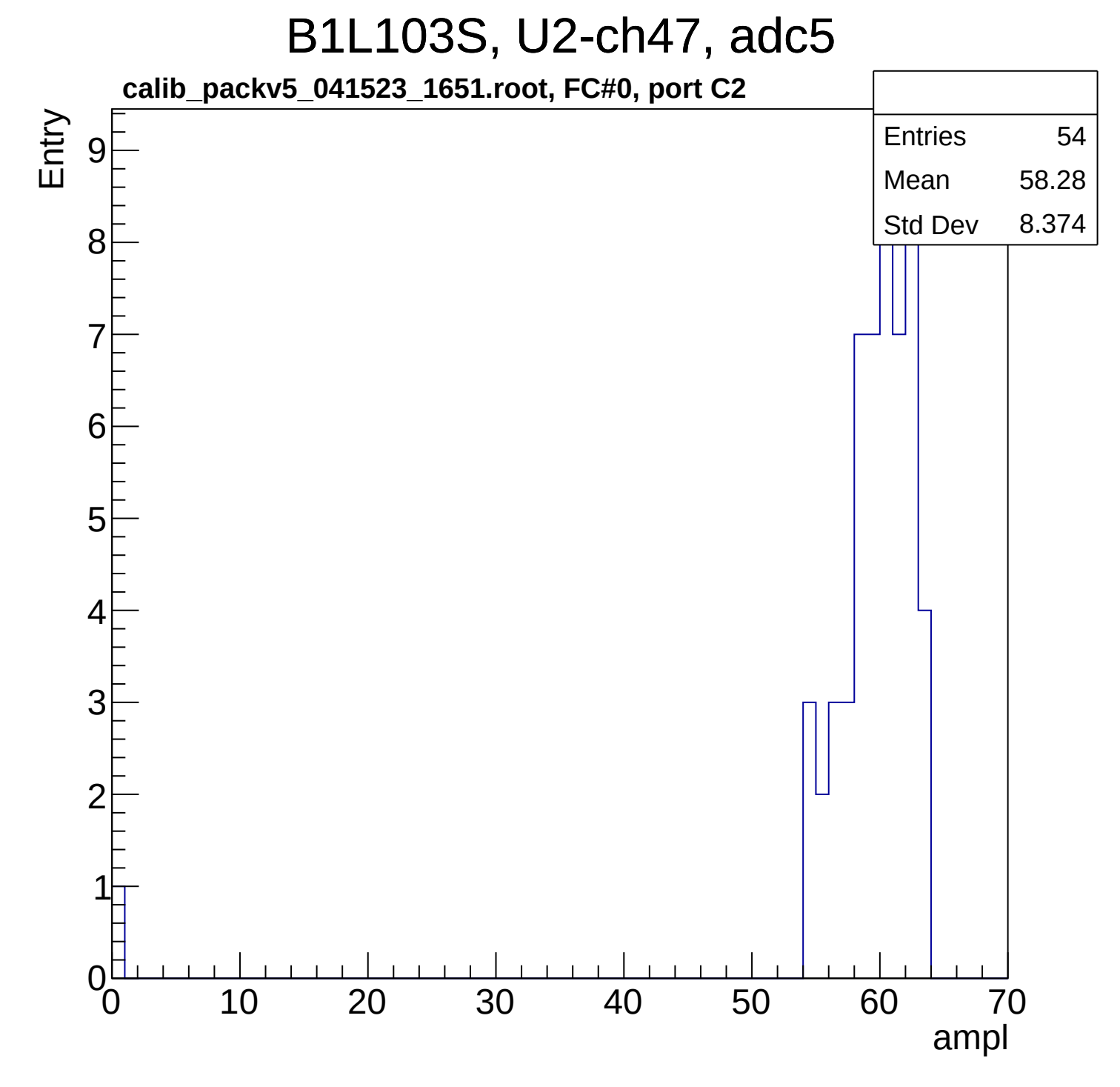

B1L103S, U2-ch47, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 28.44
Std Dev 6.883
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

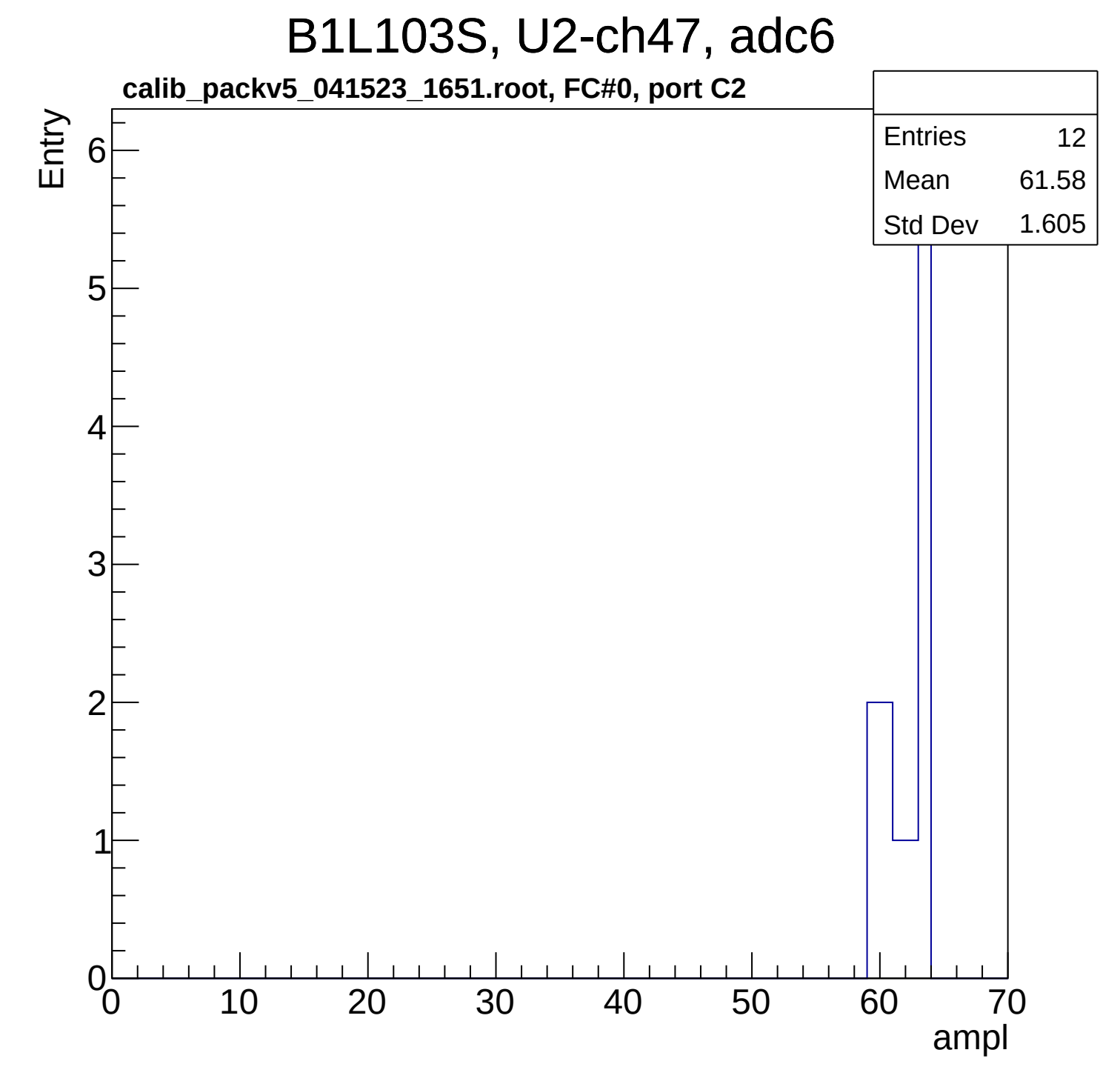

B1L103S, U2-ch47, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 34.37
Std Dev 7.912
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

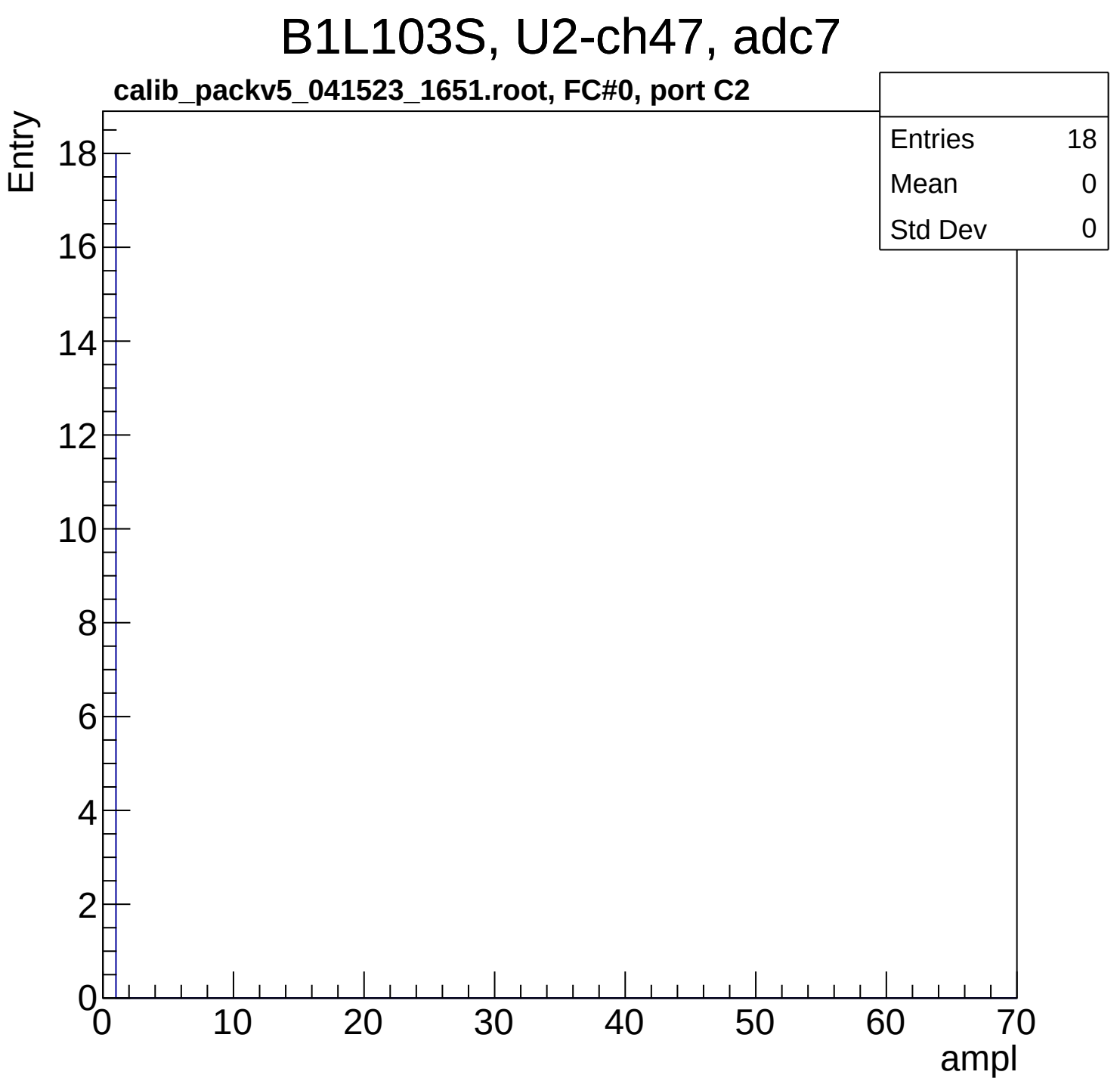

B1L103S, U2-ch47, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 39.88
Std Dev 10.59
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

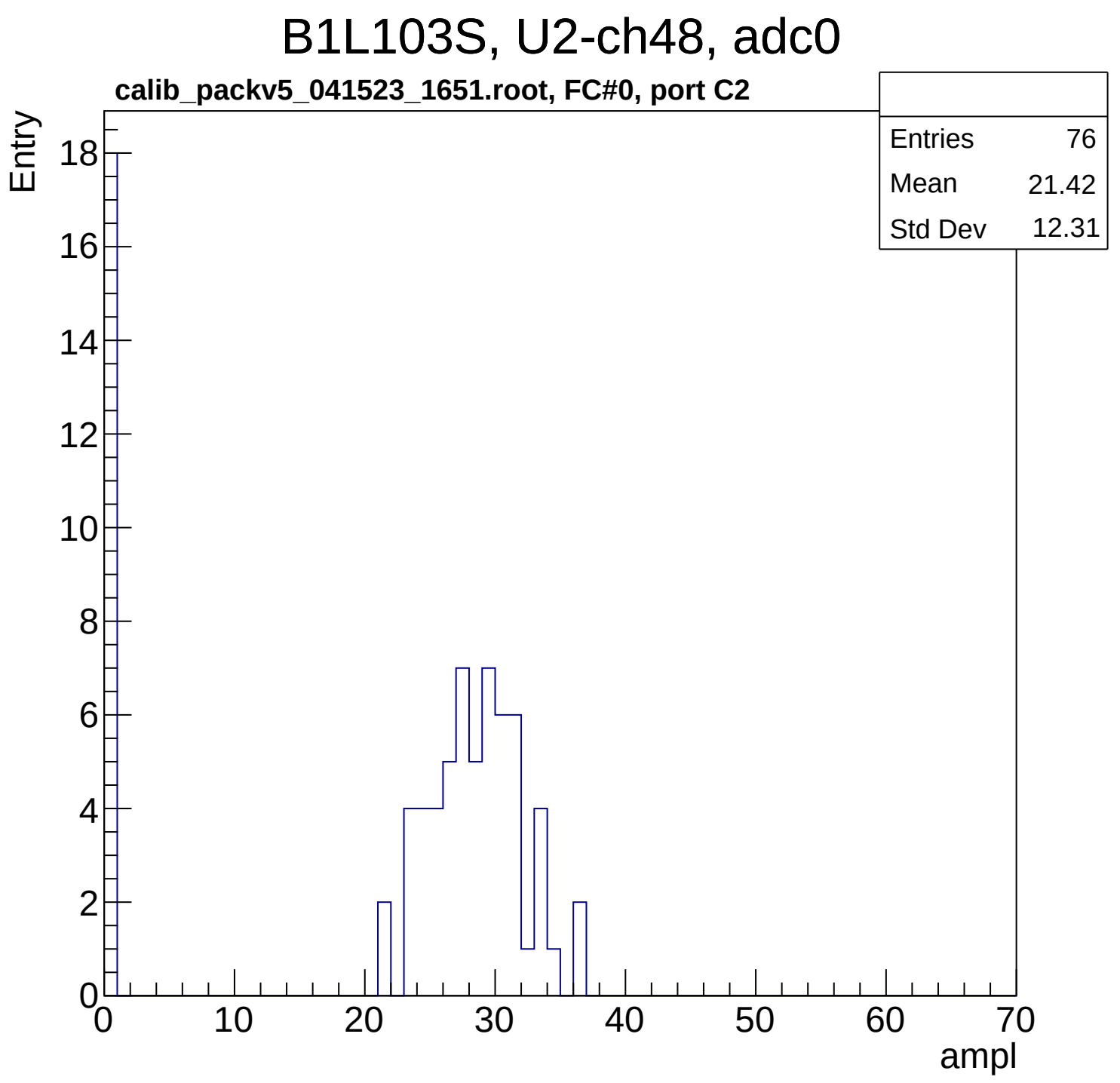

B1L103S, U2-ch47, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 48.59
Std Dev 6.791
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

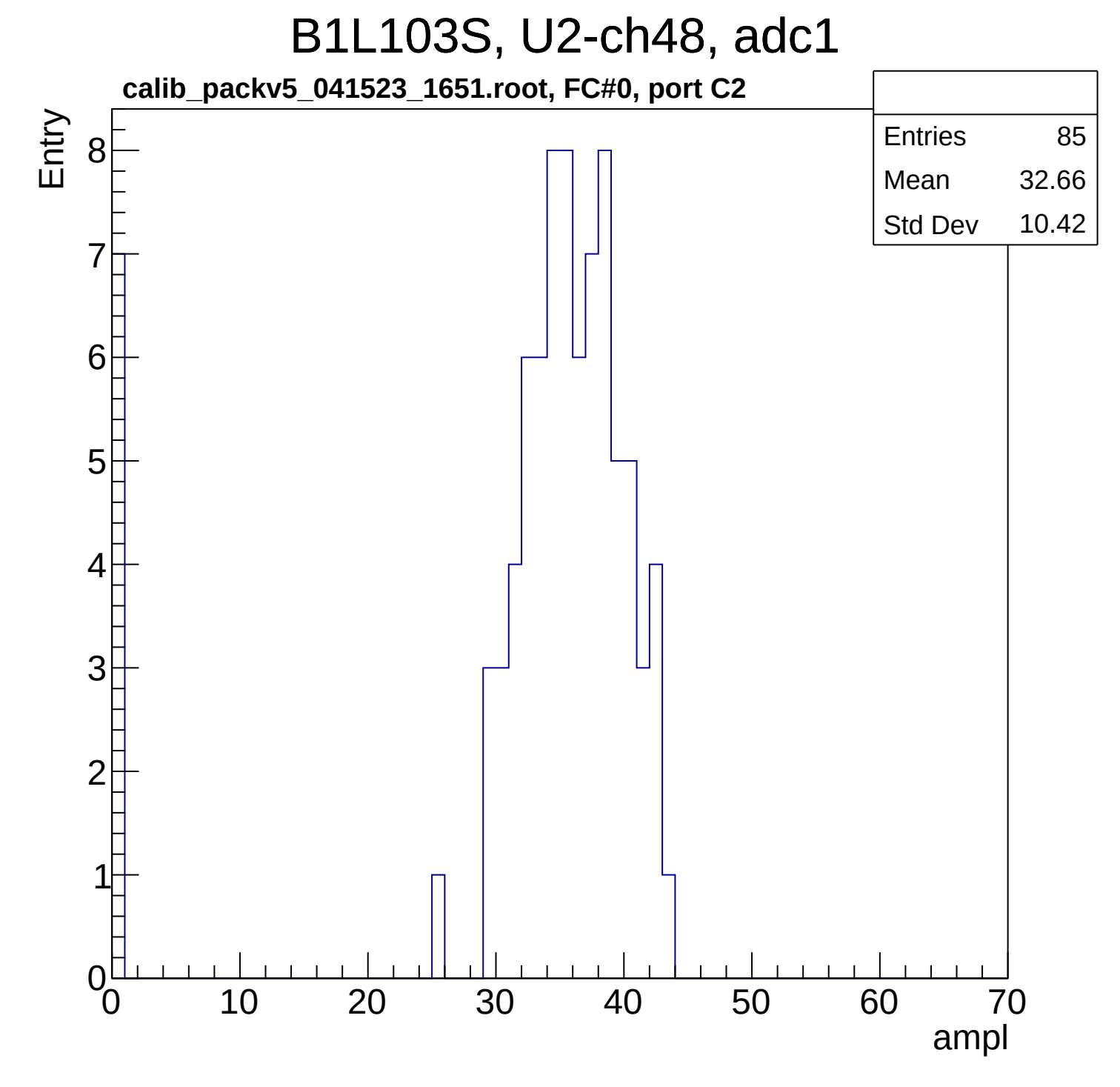

B1L103S, U2-ch47, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 54.54
Std Dev 2.902
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

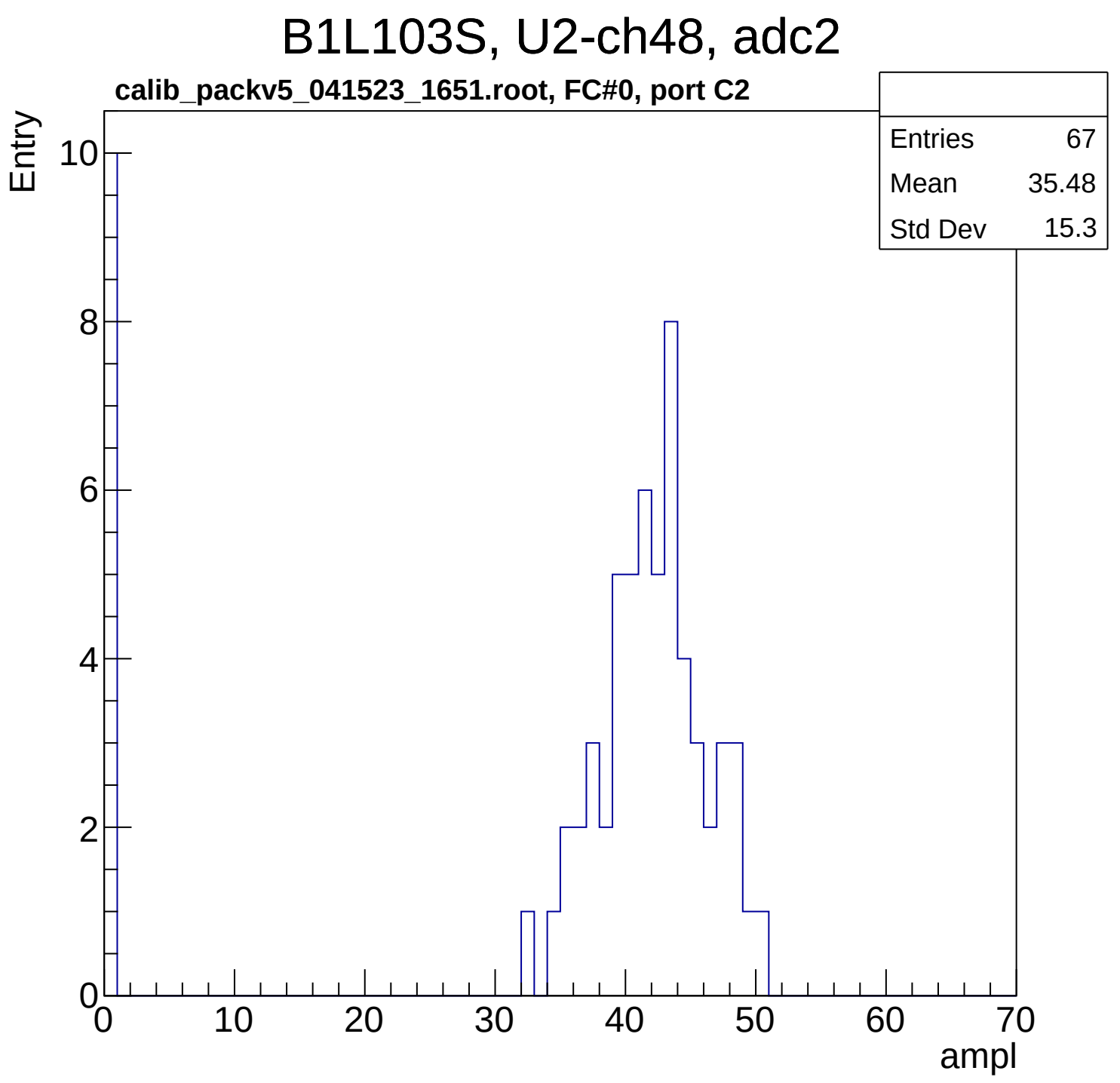

B1L103S, U2-ch47, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.28
Std Dev 8.374
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

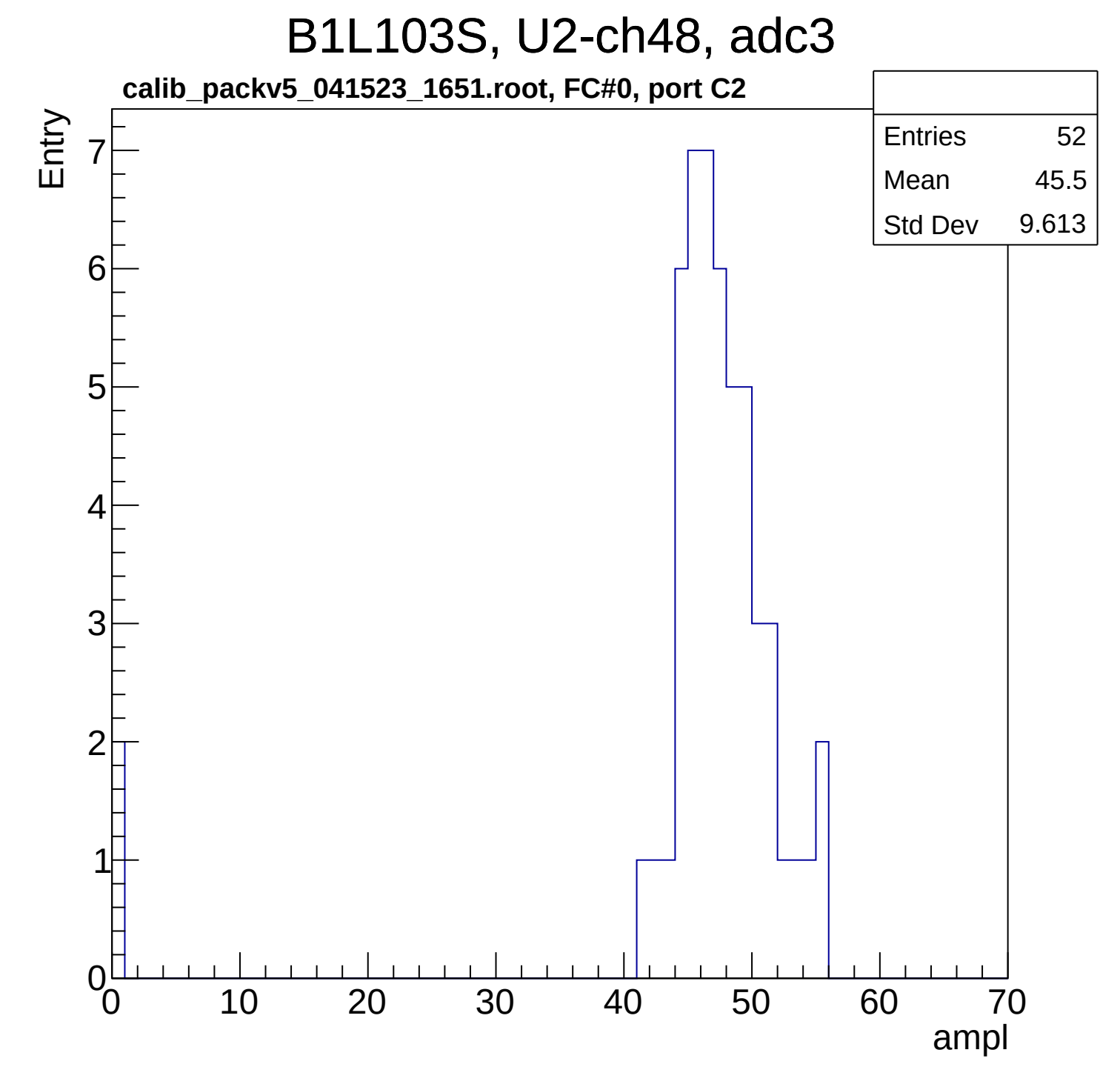

B1L103S, U2-ch47, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.58
Std Dev 1.605
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

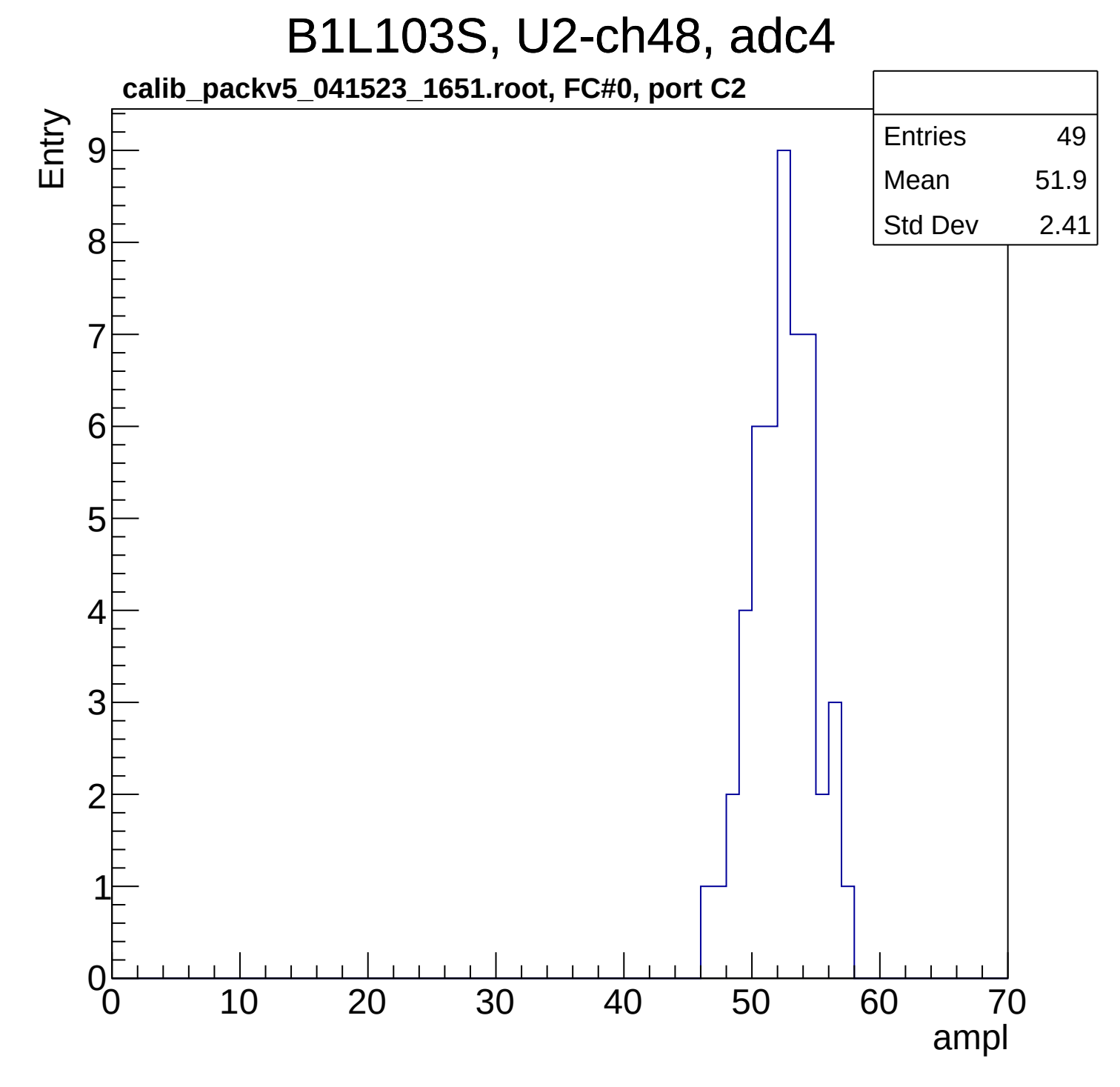

B1L103S, U2-ch47, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

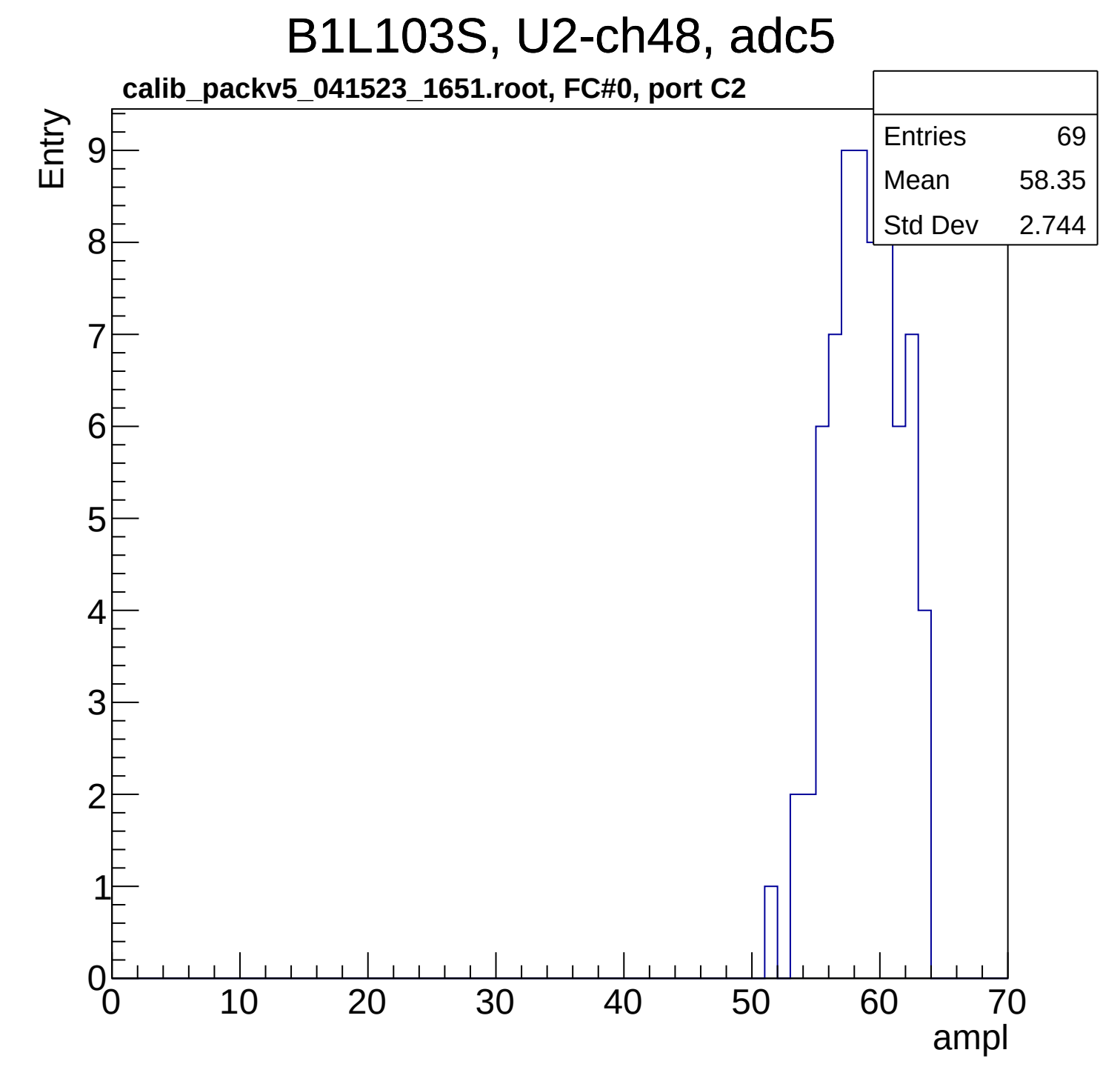

B1L103S, U2-ch48, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 21.42
Std Dev 12.31
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

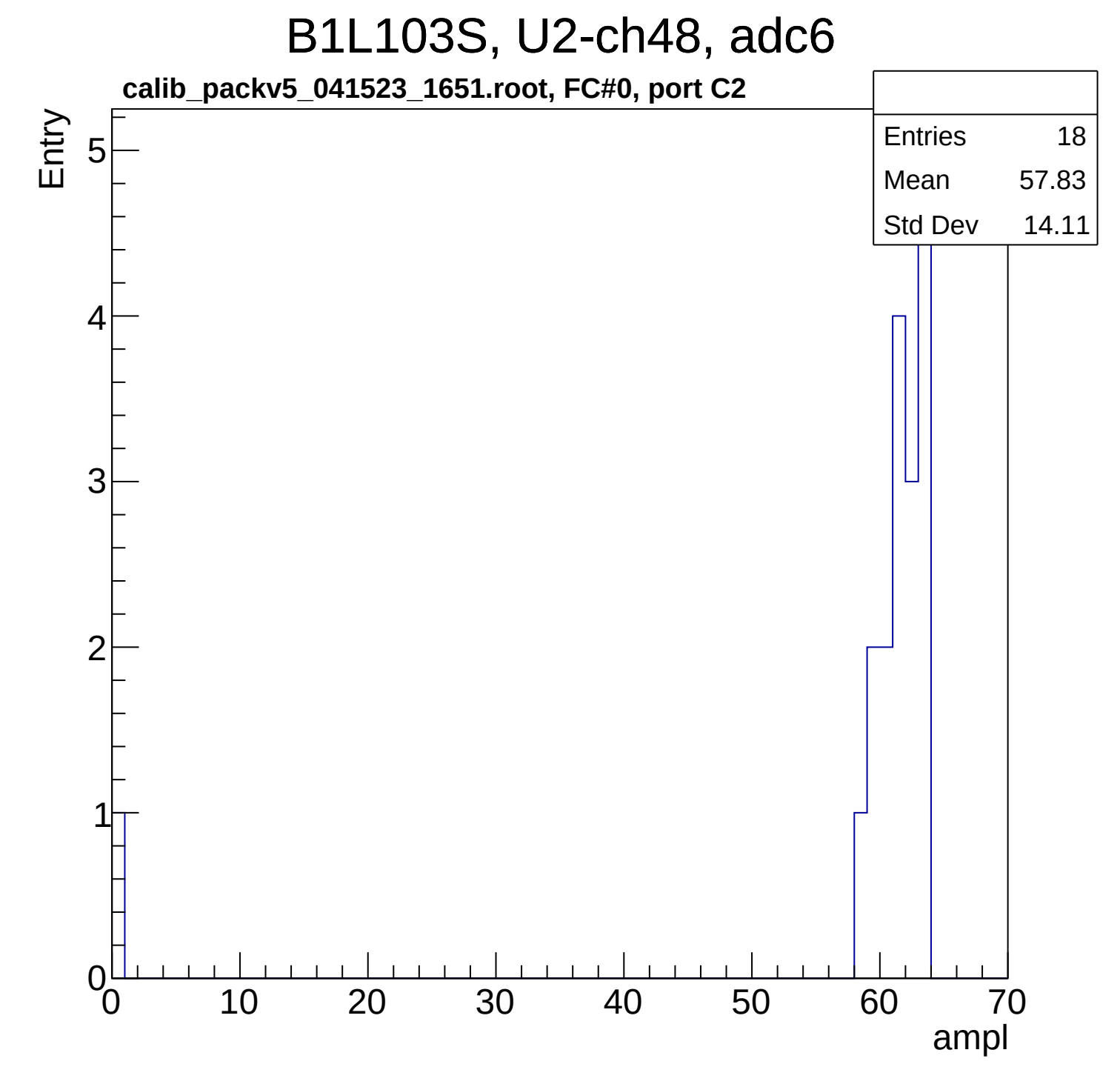

B1L103S, U2-ch48, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 32.66
Std Dev 10.42
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

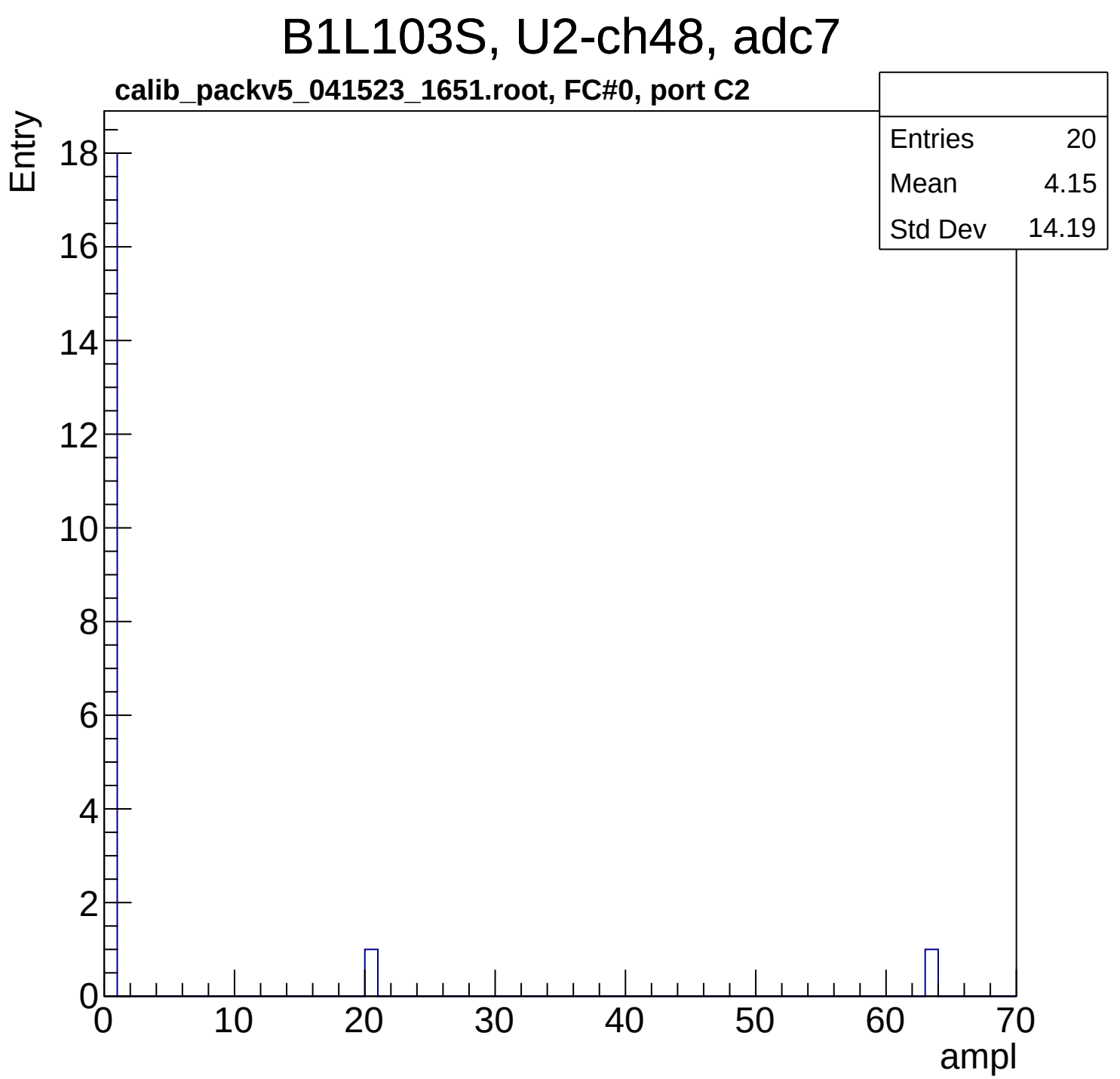

B1L103S, U2-ch48, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 35.48
Std Dev 15.3
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

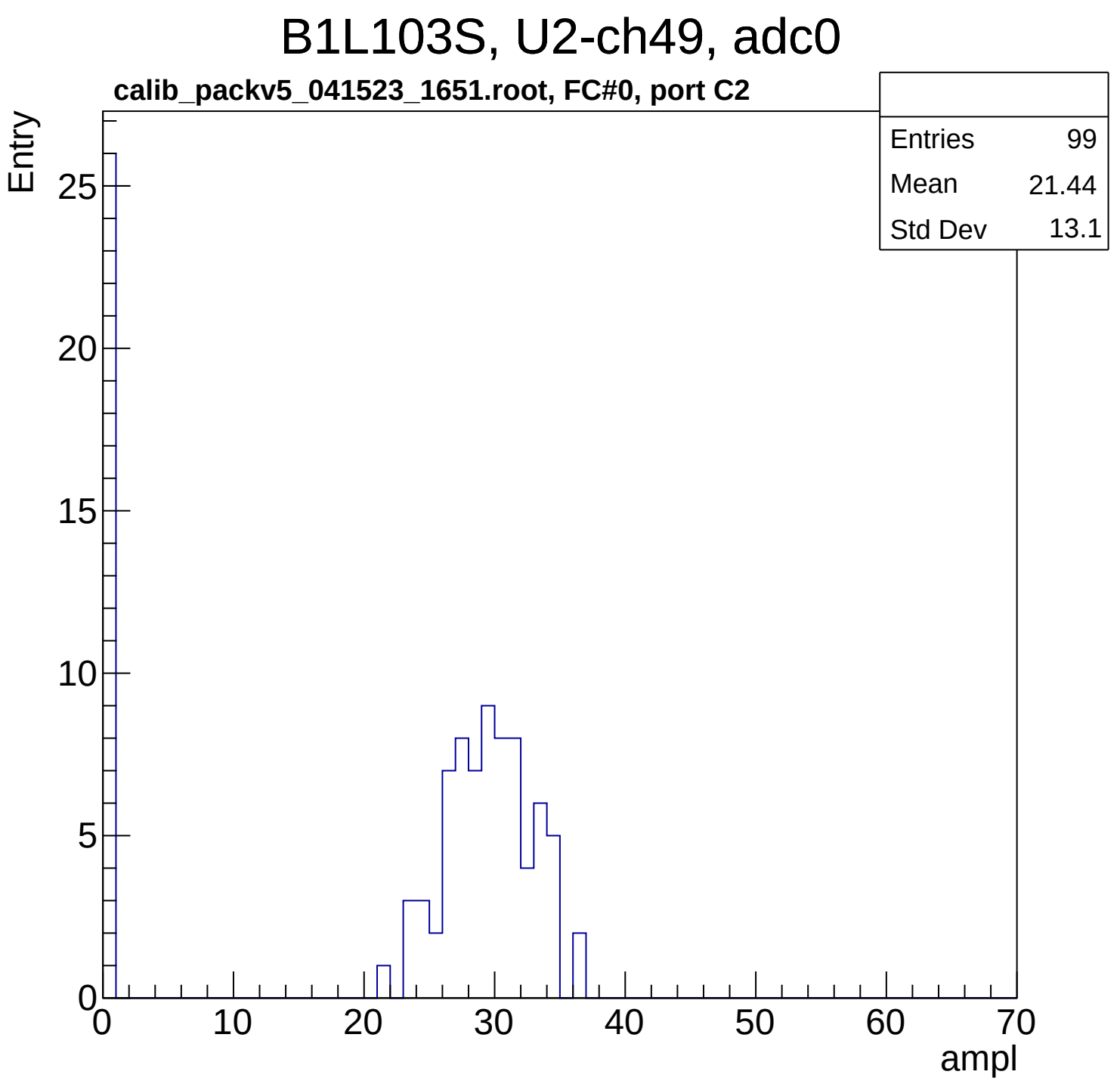

B1L103S, U2-ch48, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 45.5
Std Dev 9.613
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

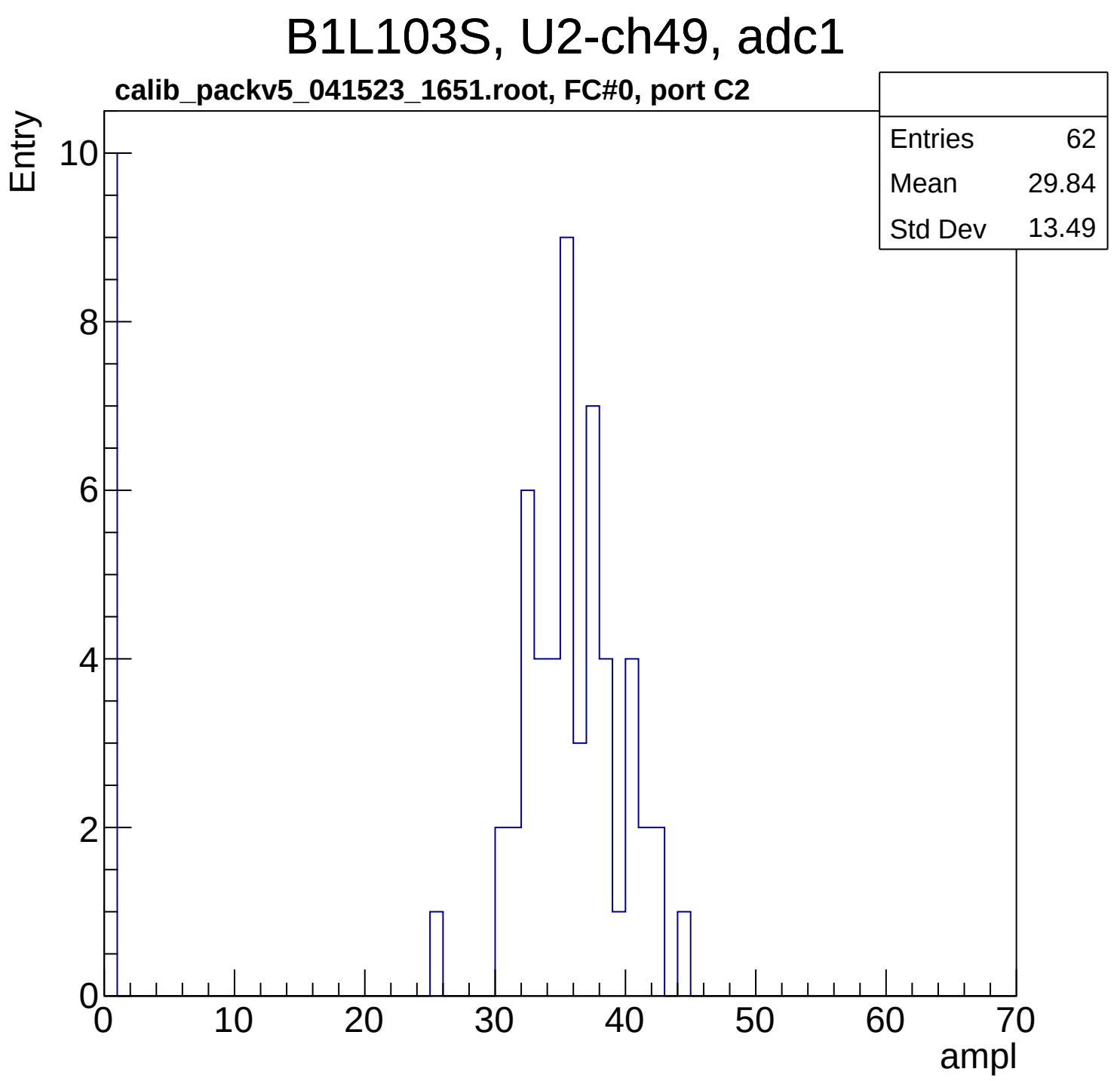

B1L103S, U2-ch48, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 51.9
Std Dev 2.41
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

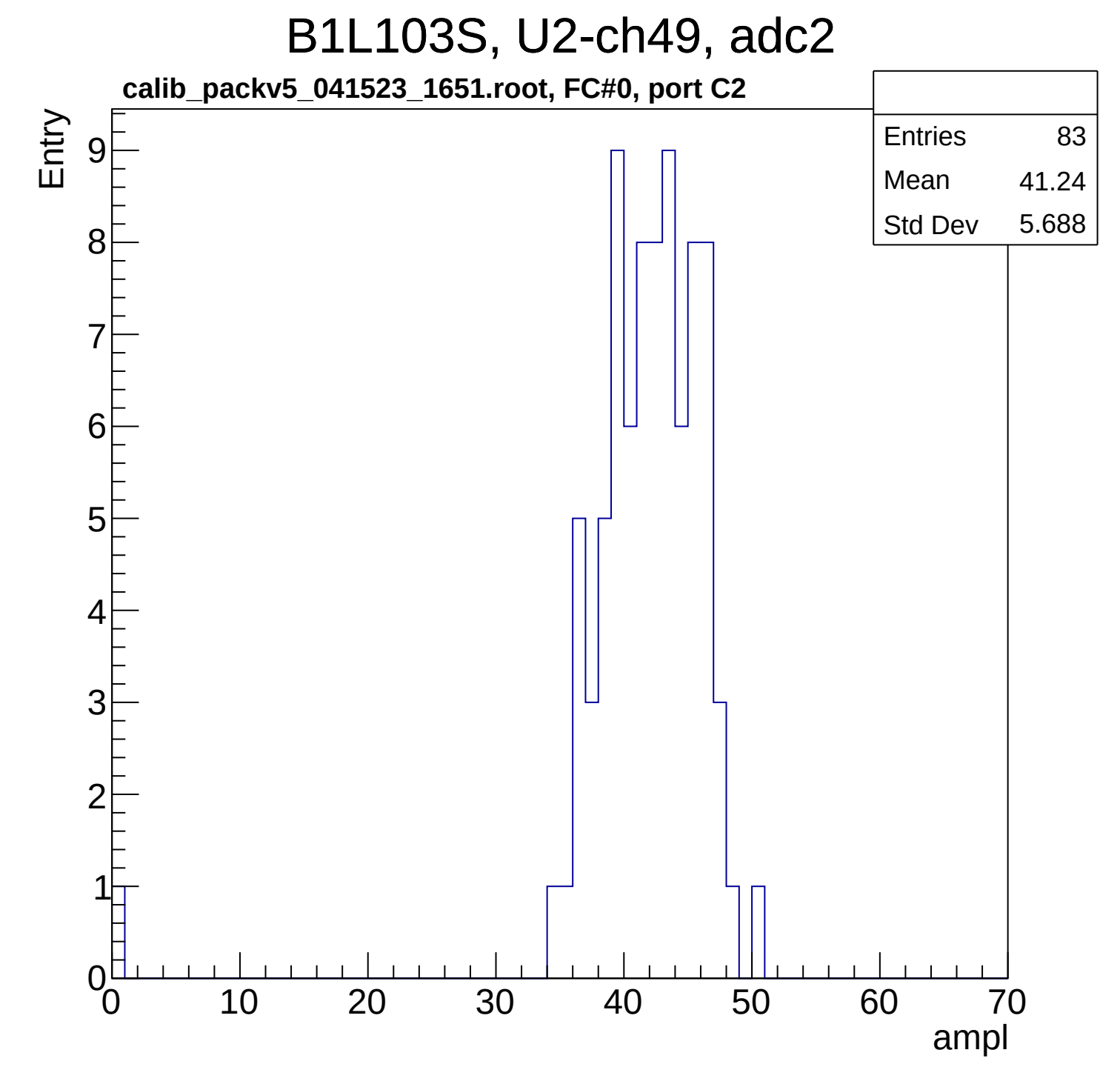

B1L103S, U2-ch48, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 58.35
Std Dev 2.744
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

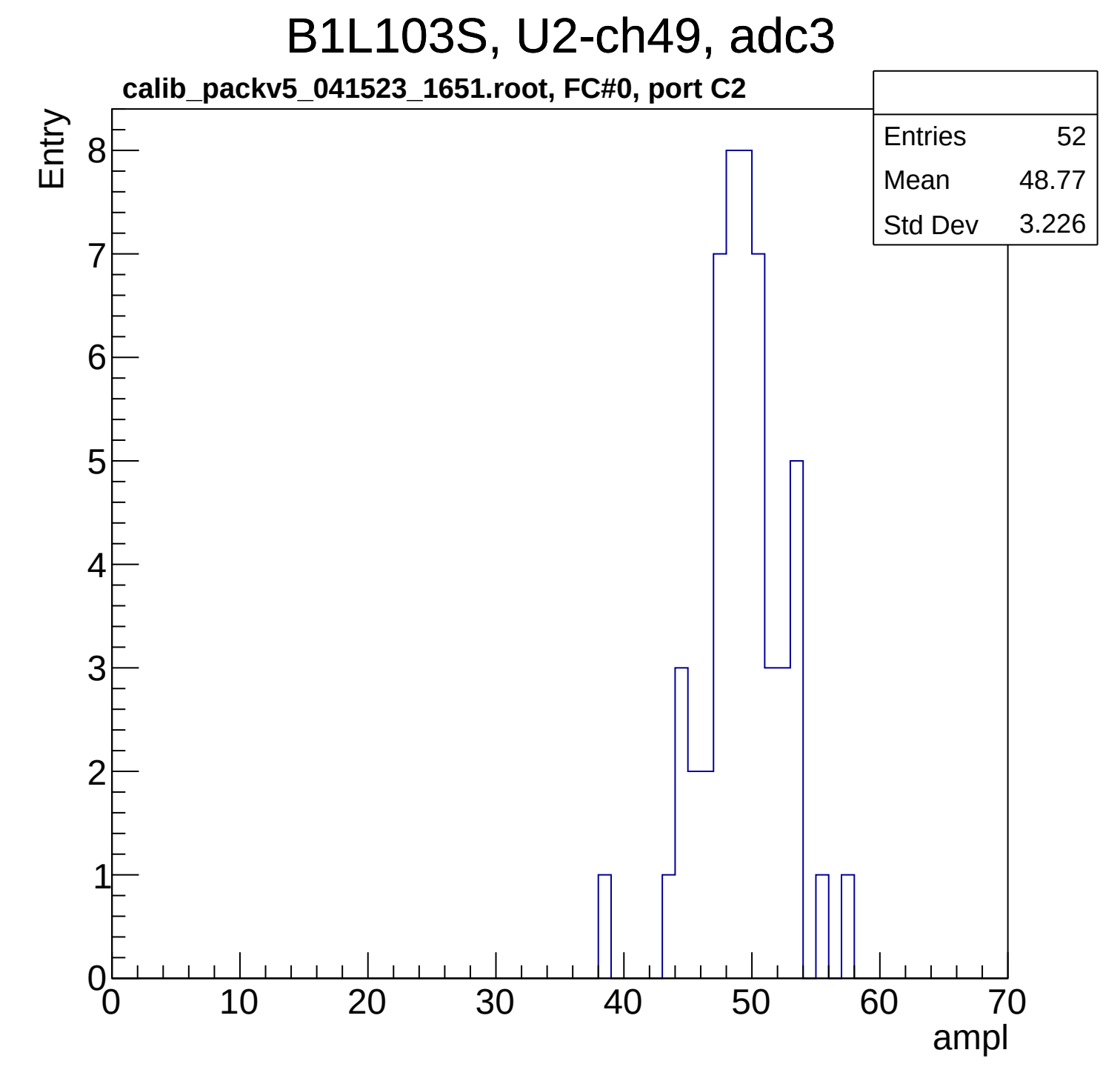

B1L103S, U2-ch48, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 57.83
Std Dev 14.11
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

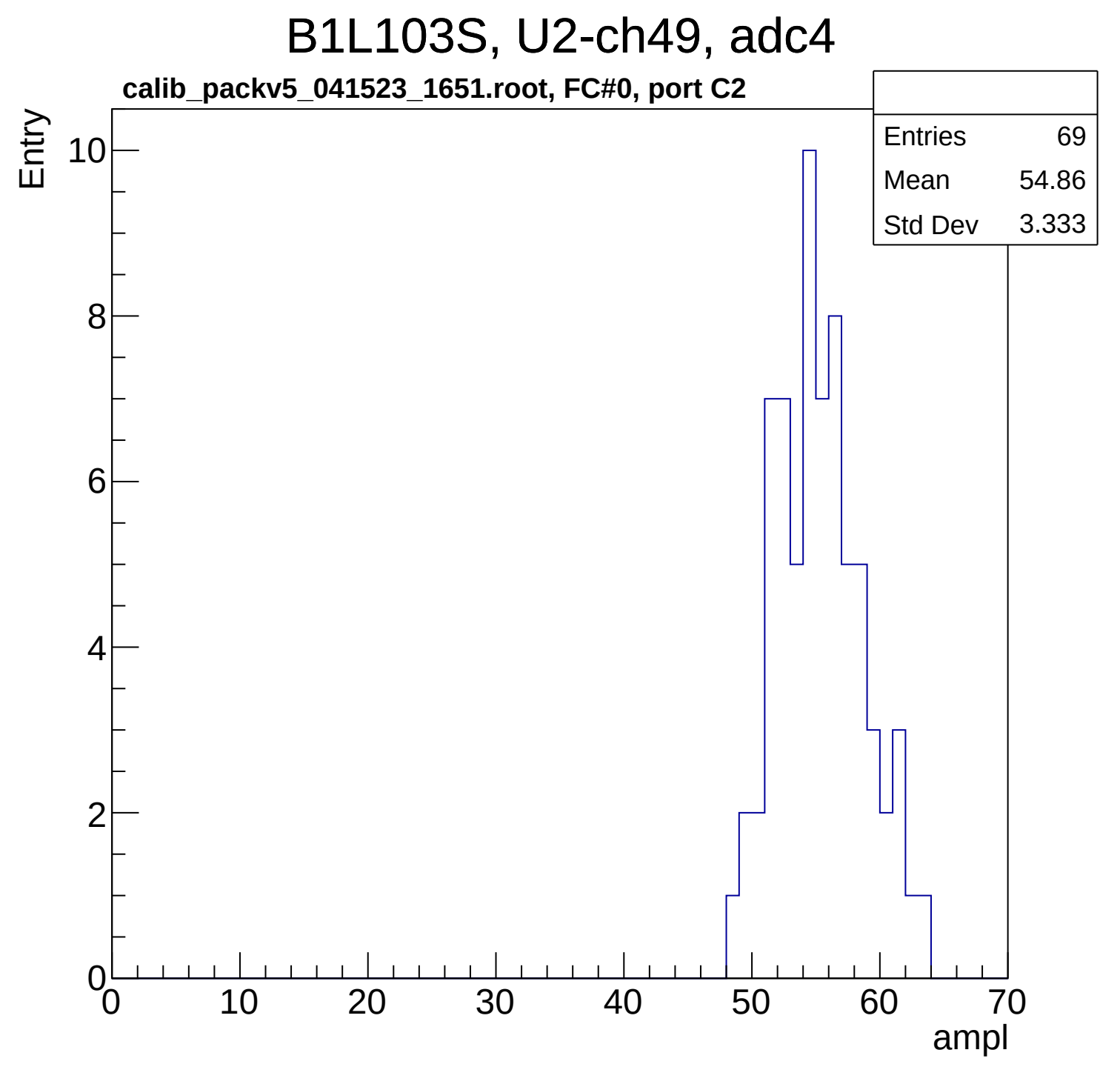

B1L103S, U2-ch48, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.15
Std Dev 14.19
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

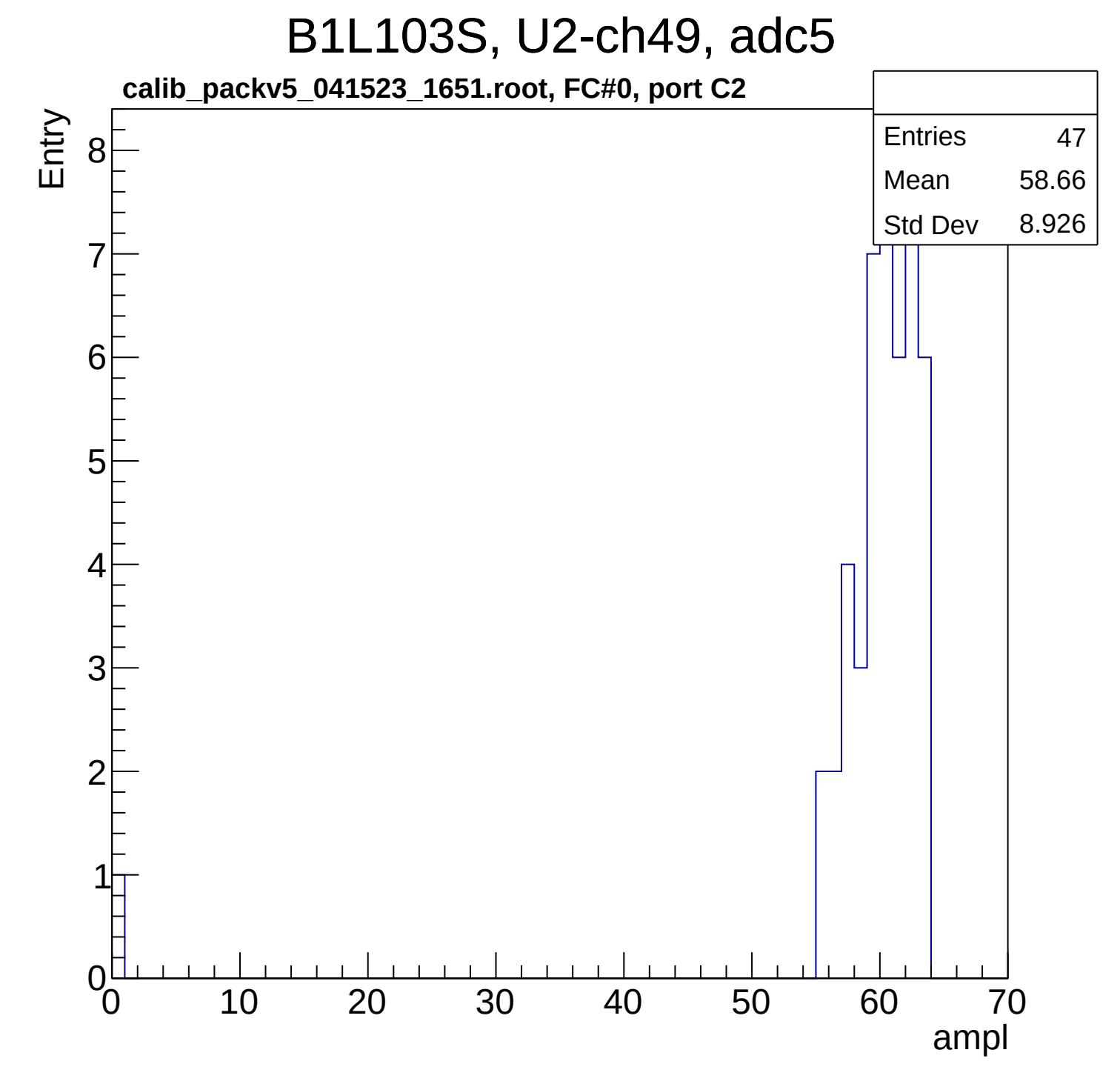

B1L103S, U2-ch49, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 21.44
Std Dev 13.1
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl

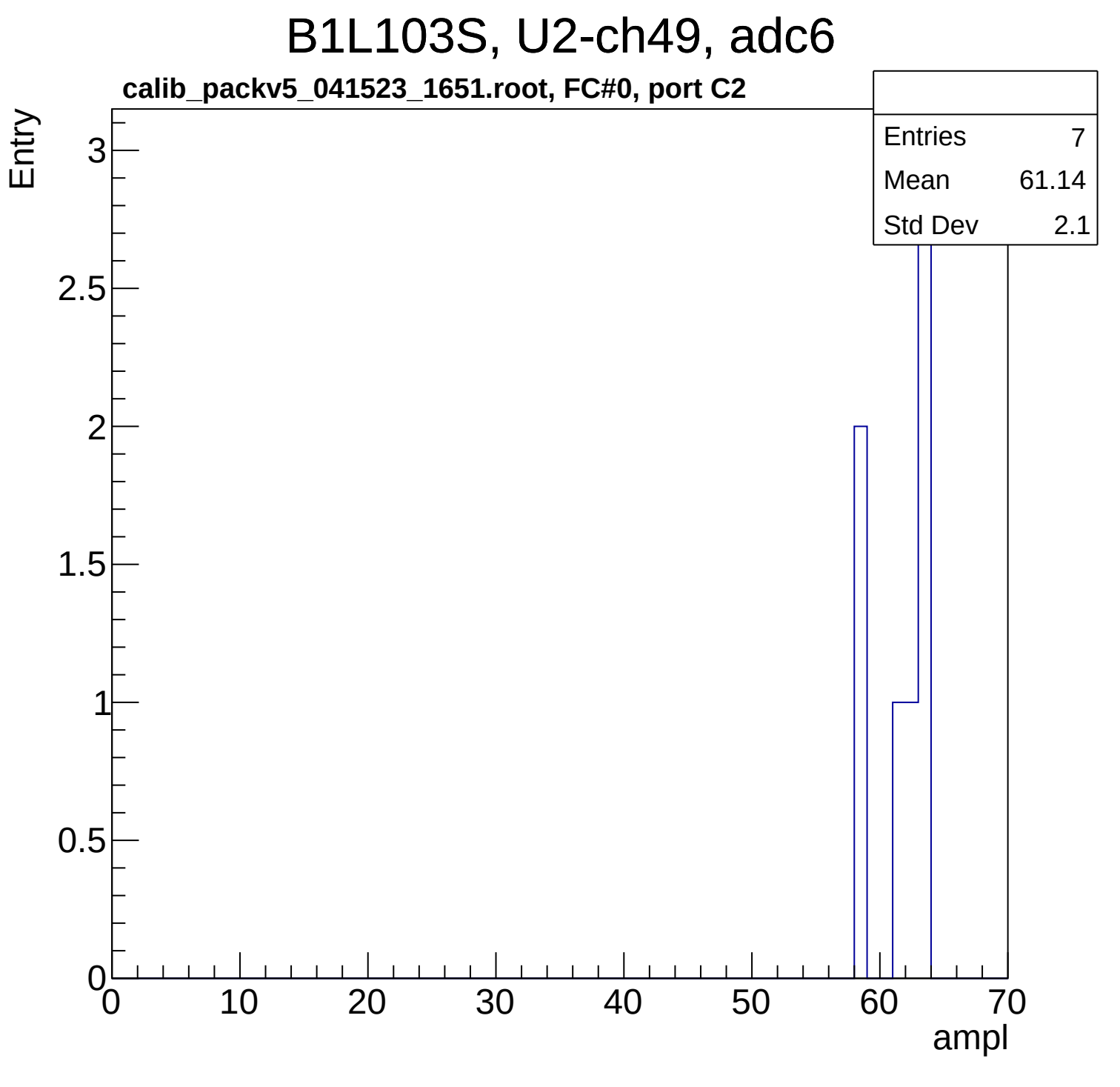

B1L103S, U2-ch49, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 29.84
Std Dev 13.49
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

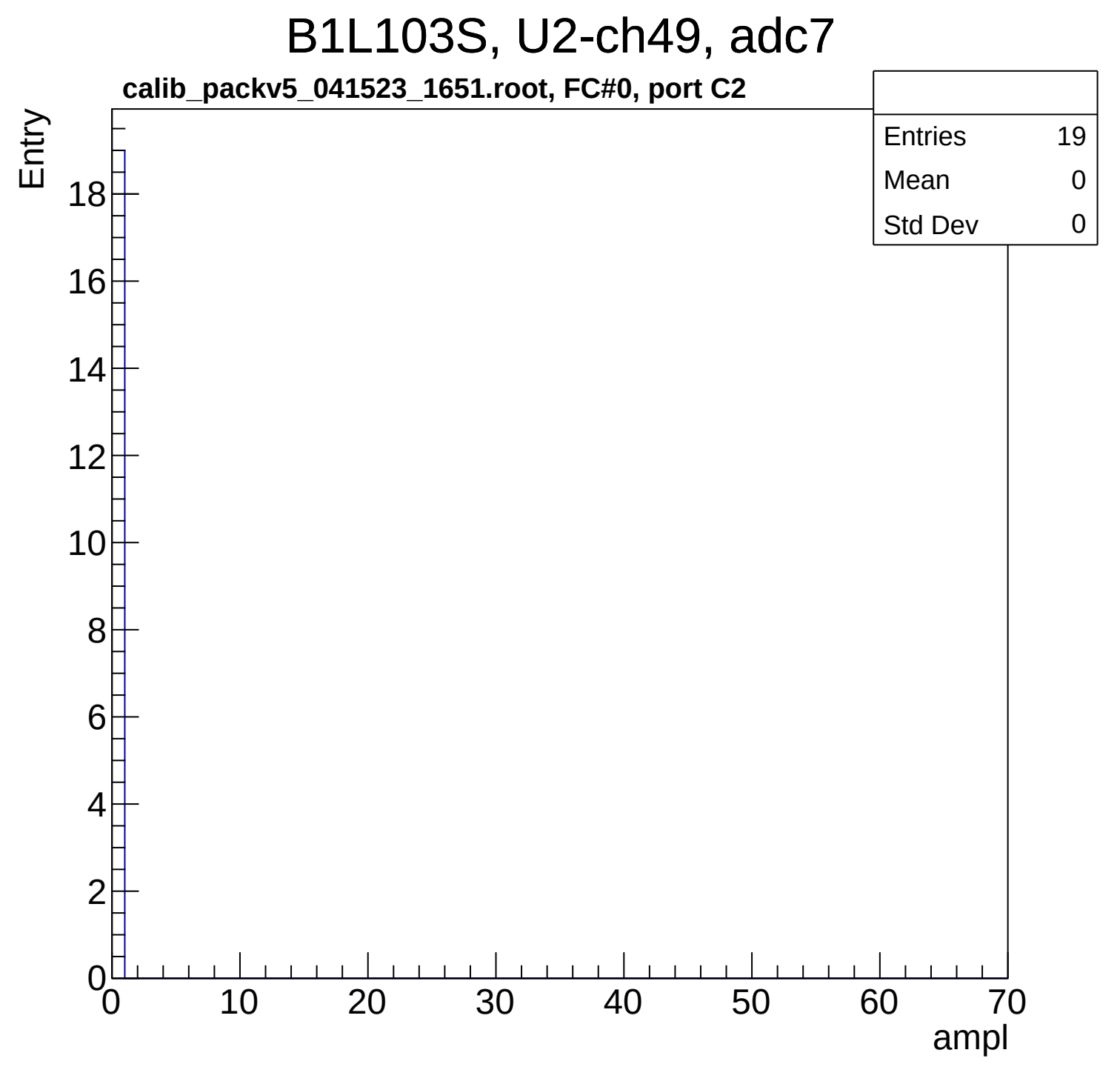

B1L103S, U2-ch49, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 41.24
Std Dev 5.688
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

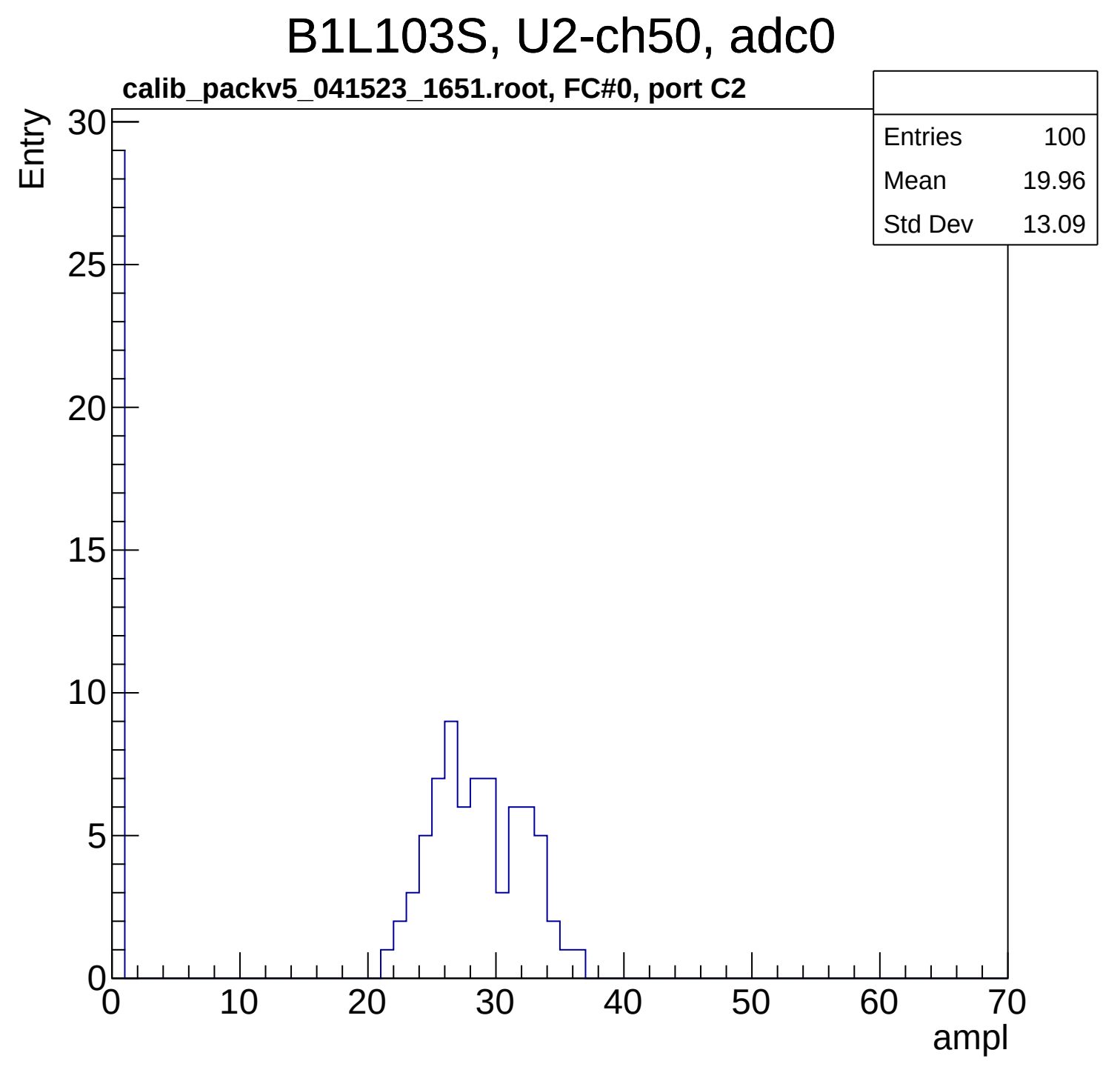

B1L103S, U2-ch49, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 48.77
Std Dev 3.226
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

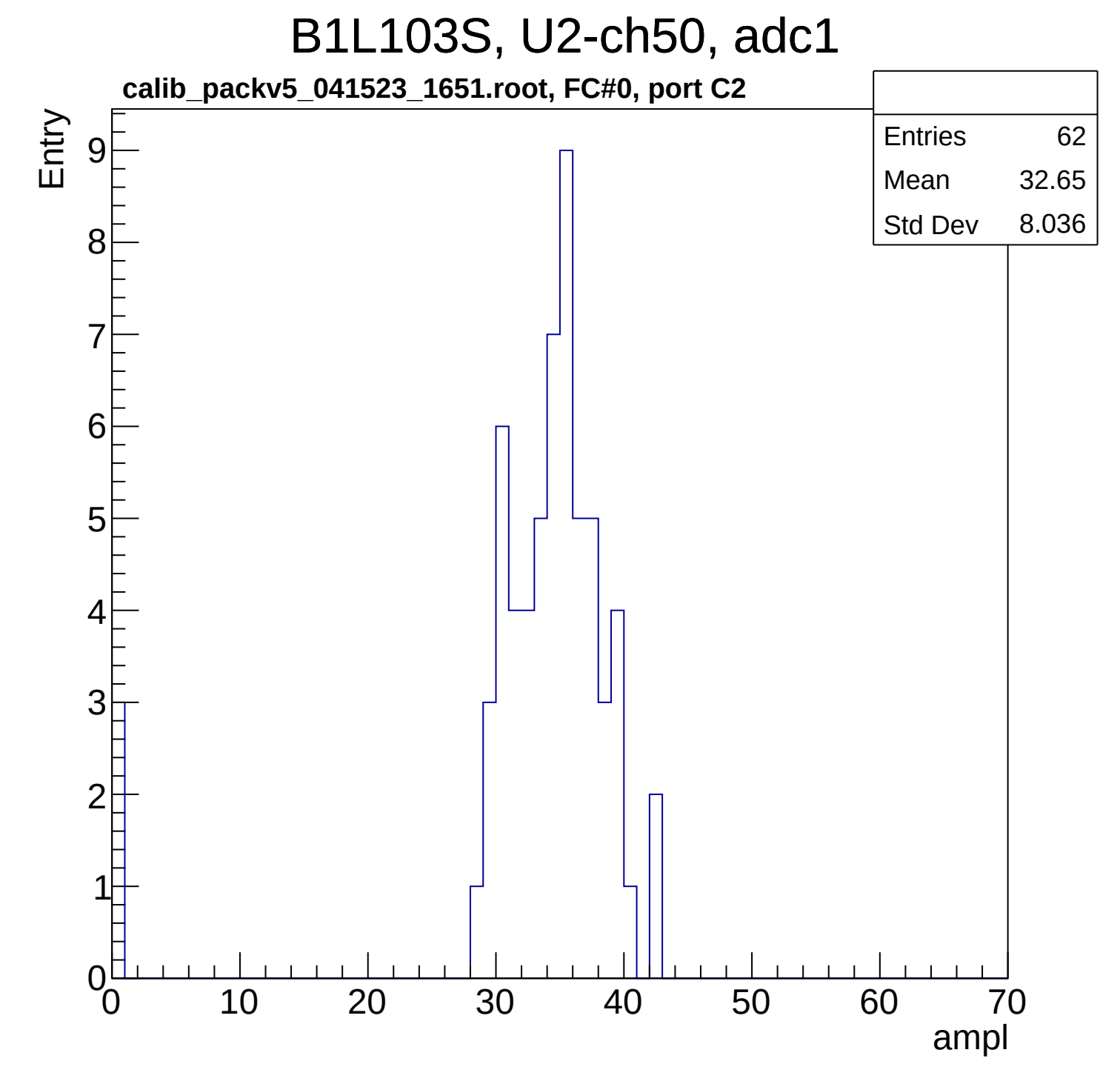

B1L103S, U2-ch49, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 54.86
Std Dev 3.333
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

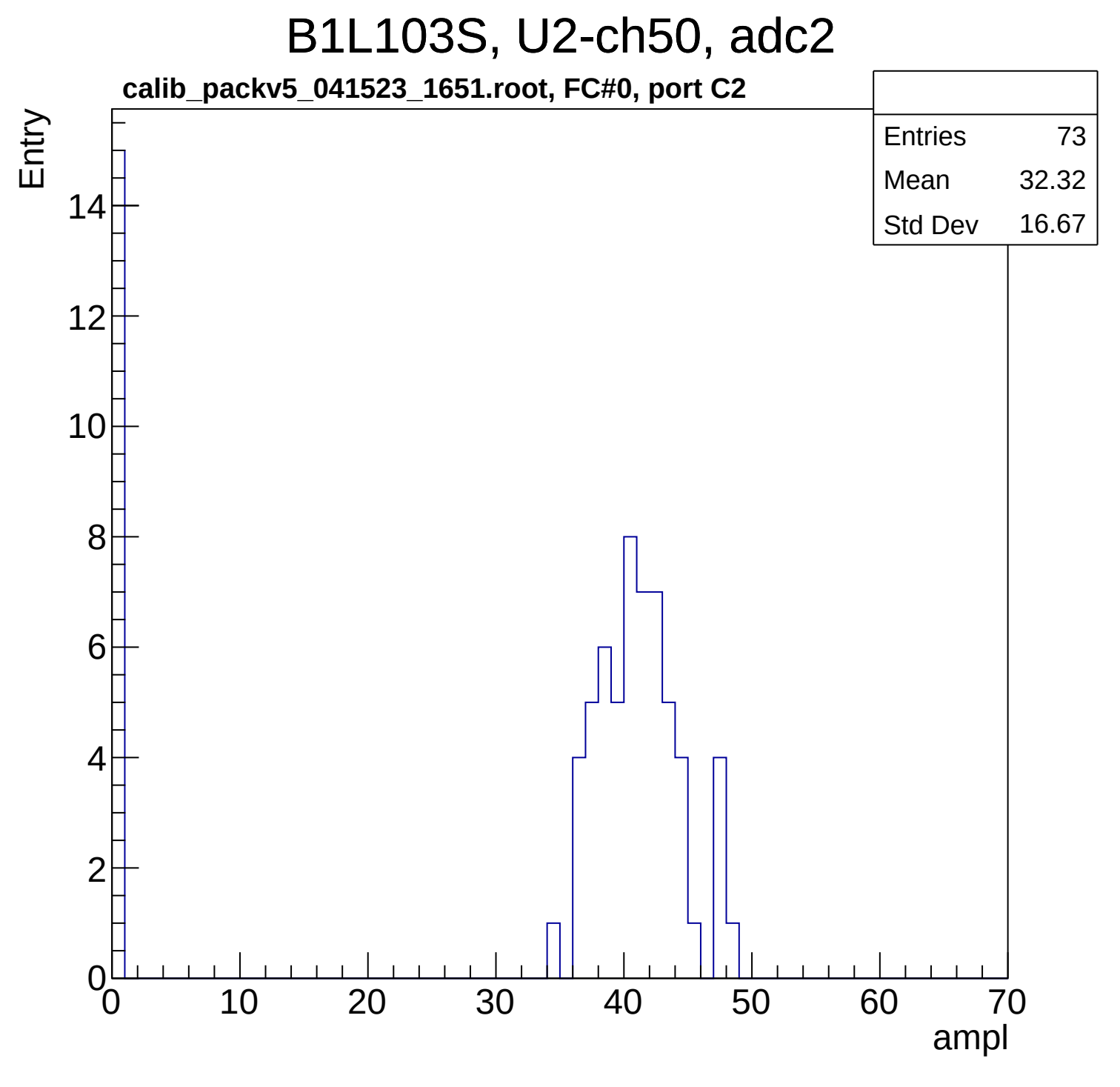

B1L103S, U2-ch49, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.66
Std Dev 8.926
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

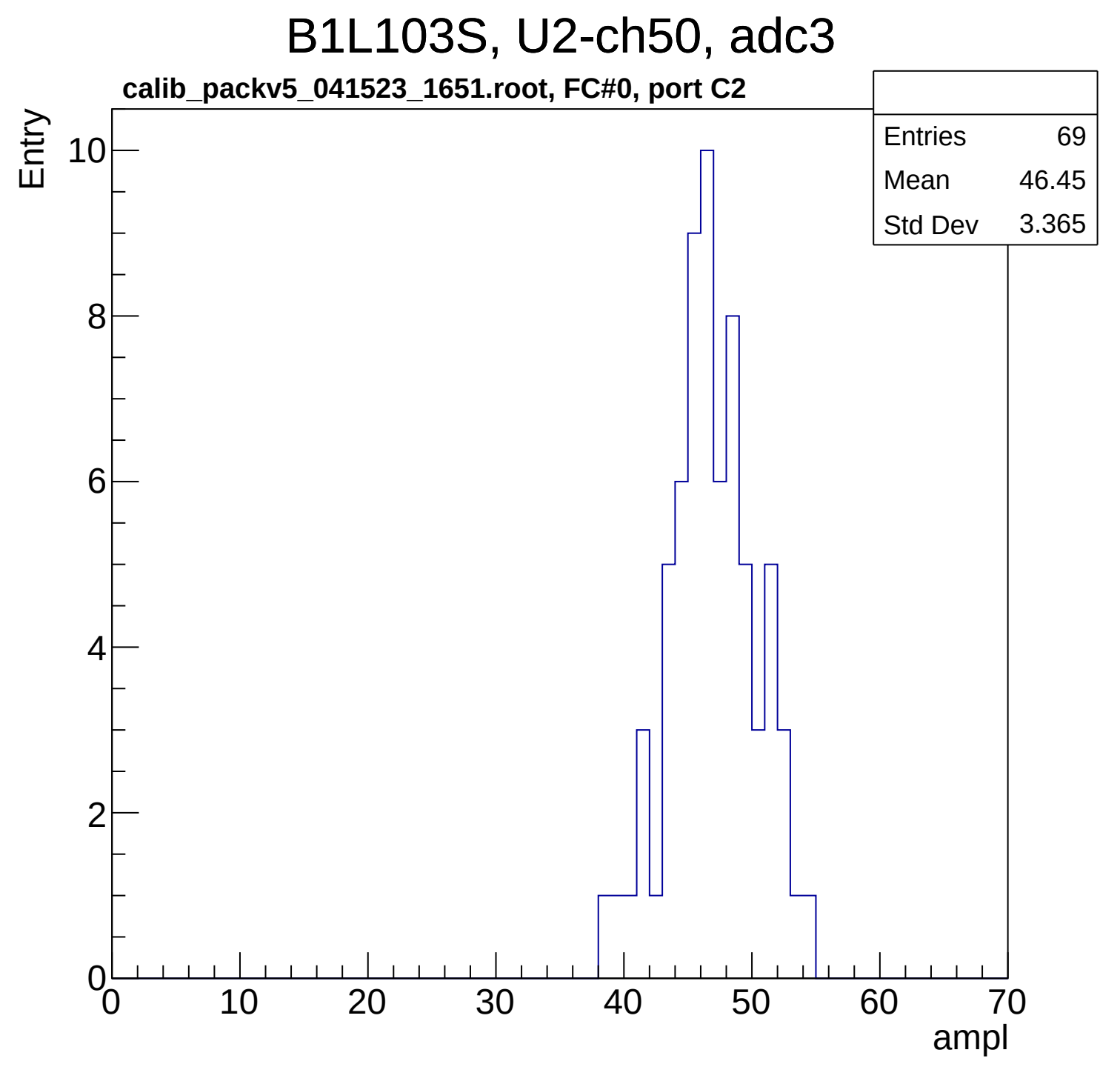

B1L103S, U2-ch49, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.14
Std Dev 2.1
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

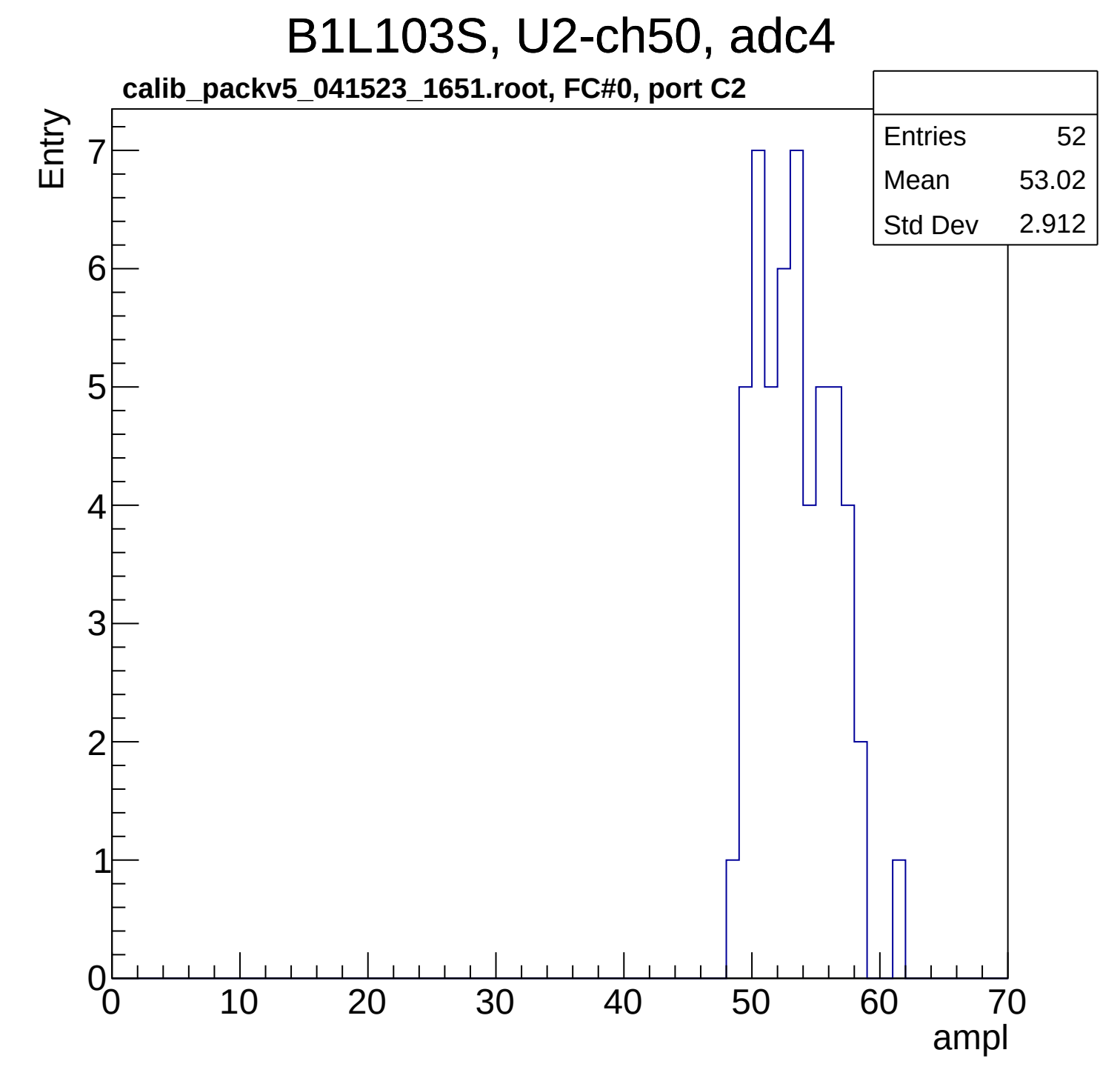

B1L103S, U2-ch49, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

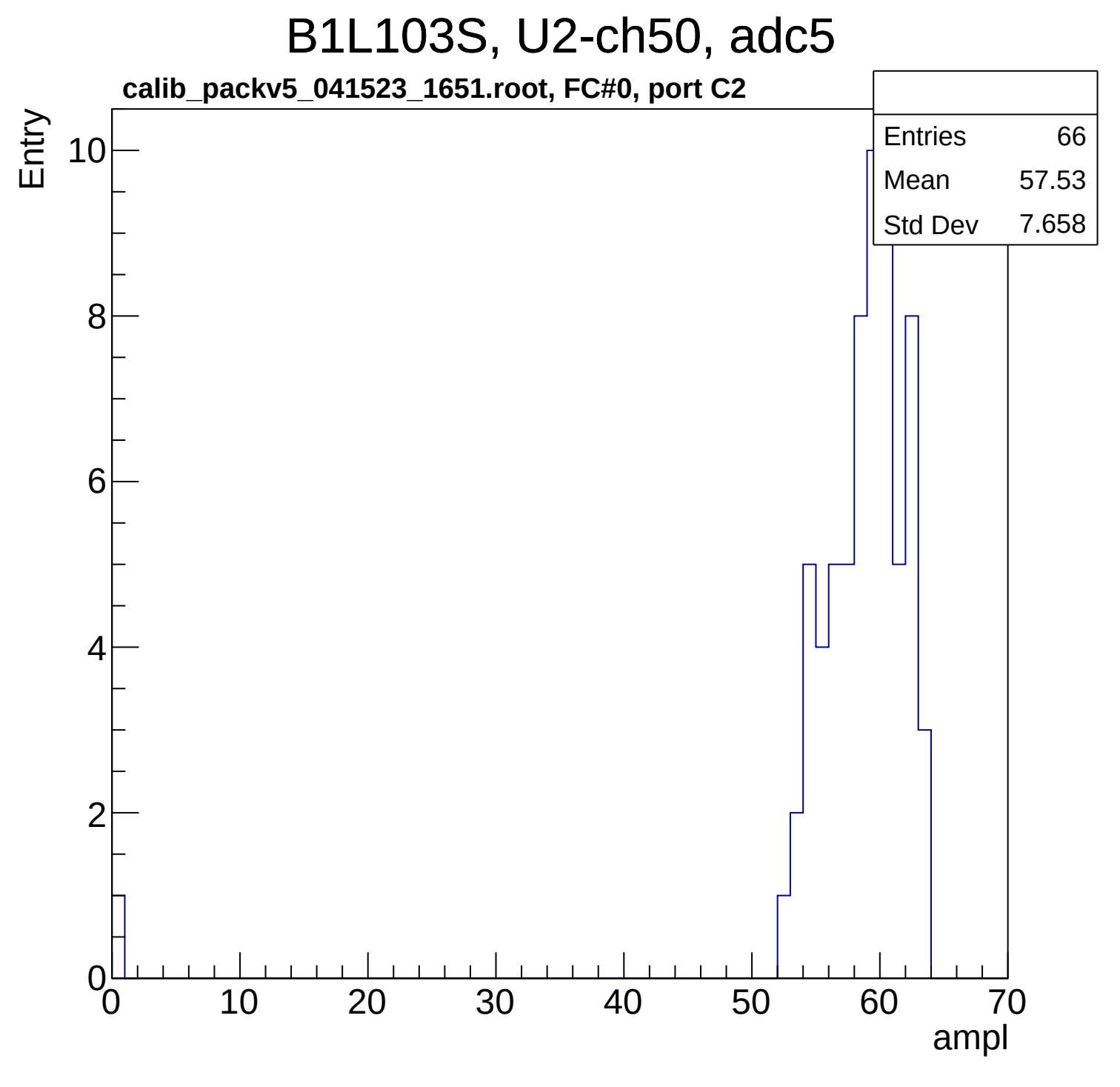

B1L103S, U2-ch50, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 19.96
Std Dev 13.09
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70

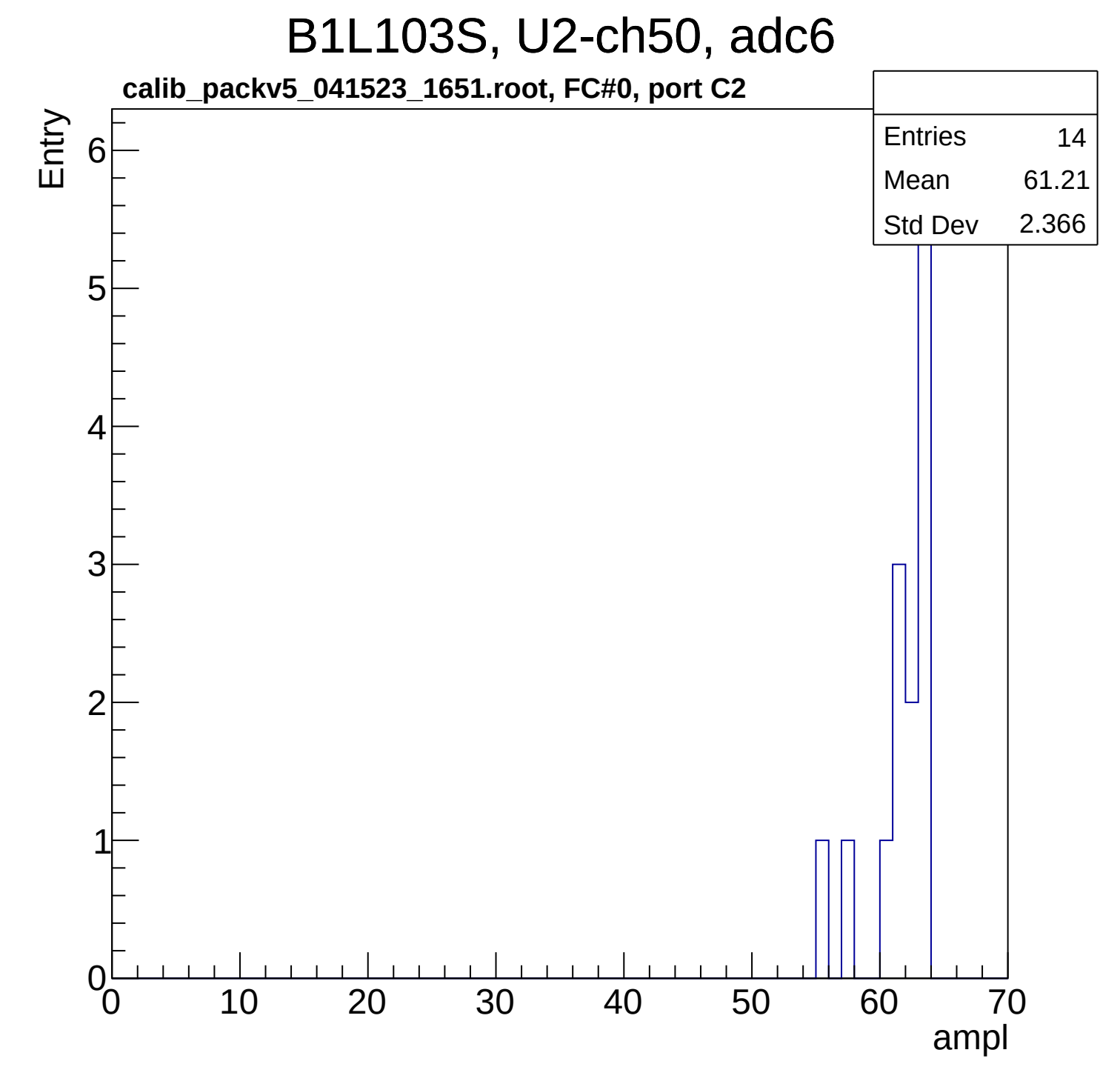

B1L103S, U2-ch50, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 32.65
Std Dev 8.036
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

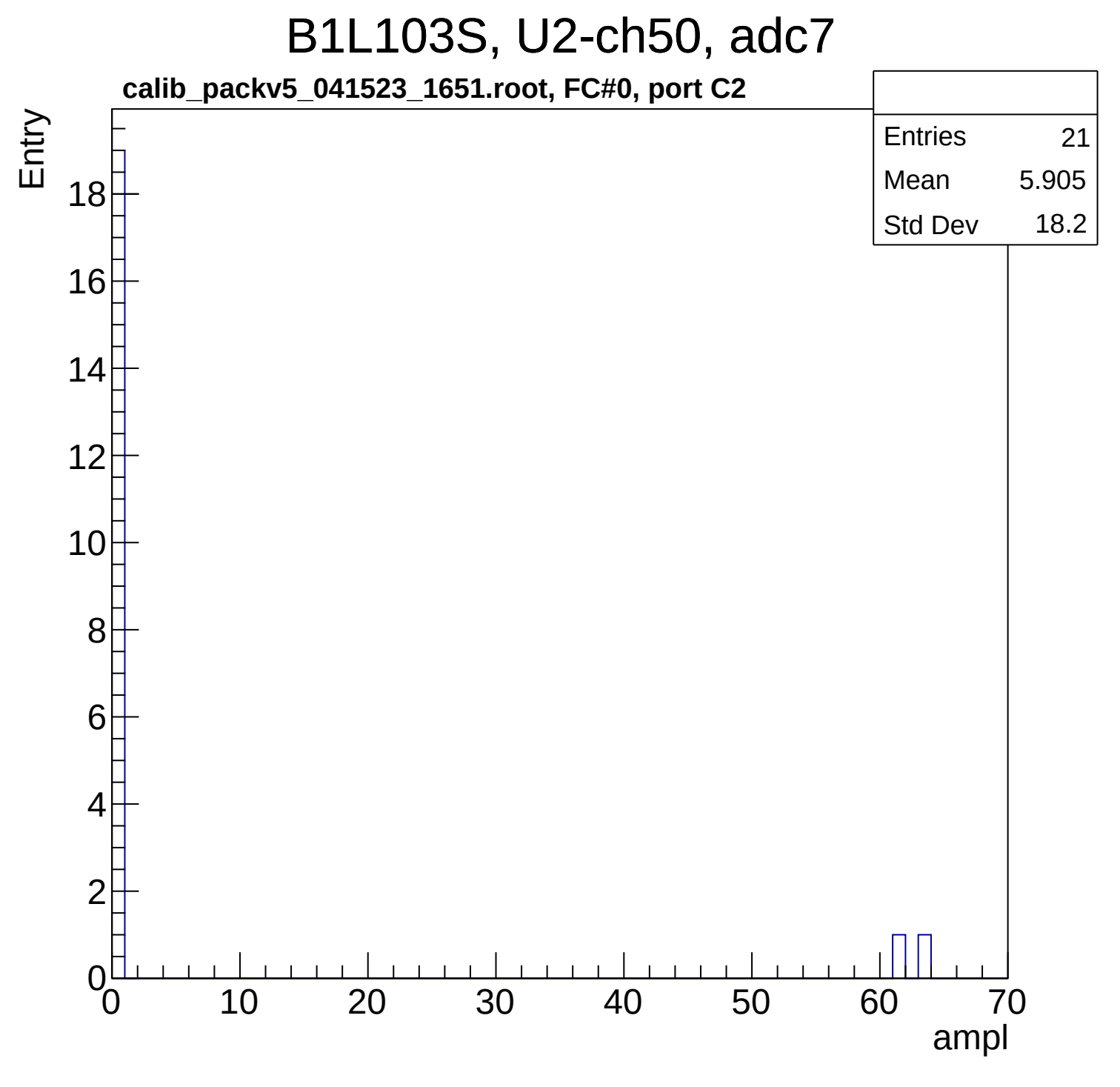

B1L103S, U2-ch50, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 32.32
Std Dev 16.67
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

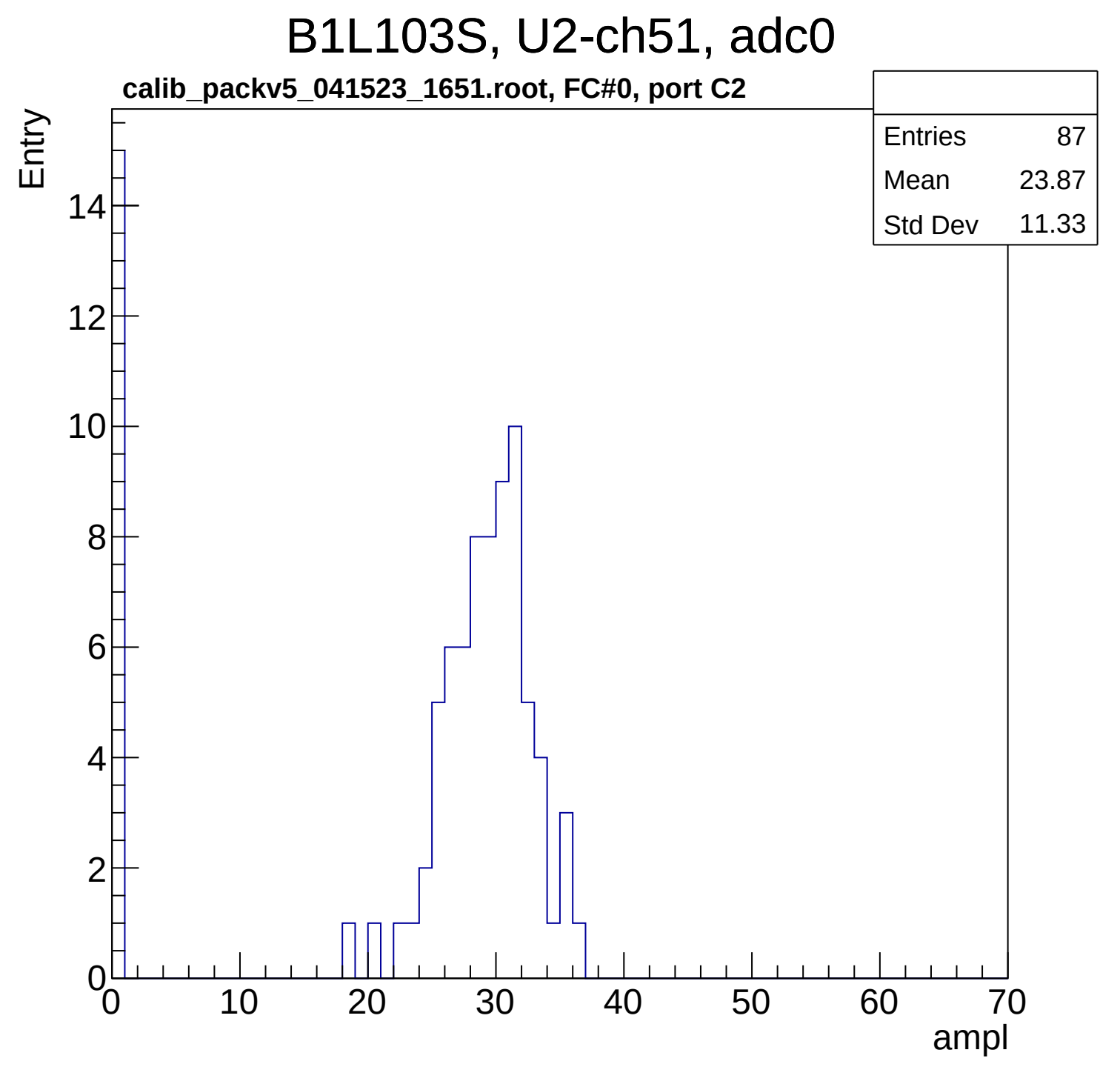

B1L103S, U2-ch50, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 46.45
Std Dev 3.365
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

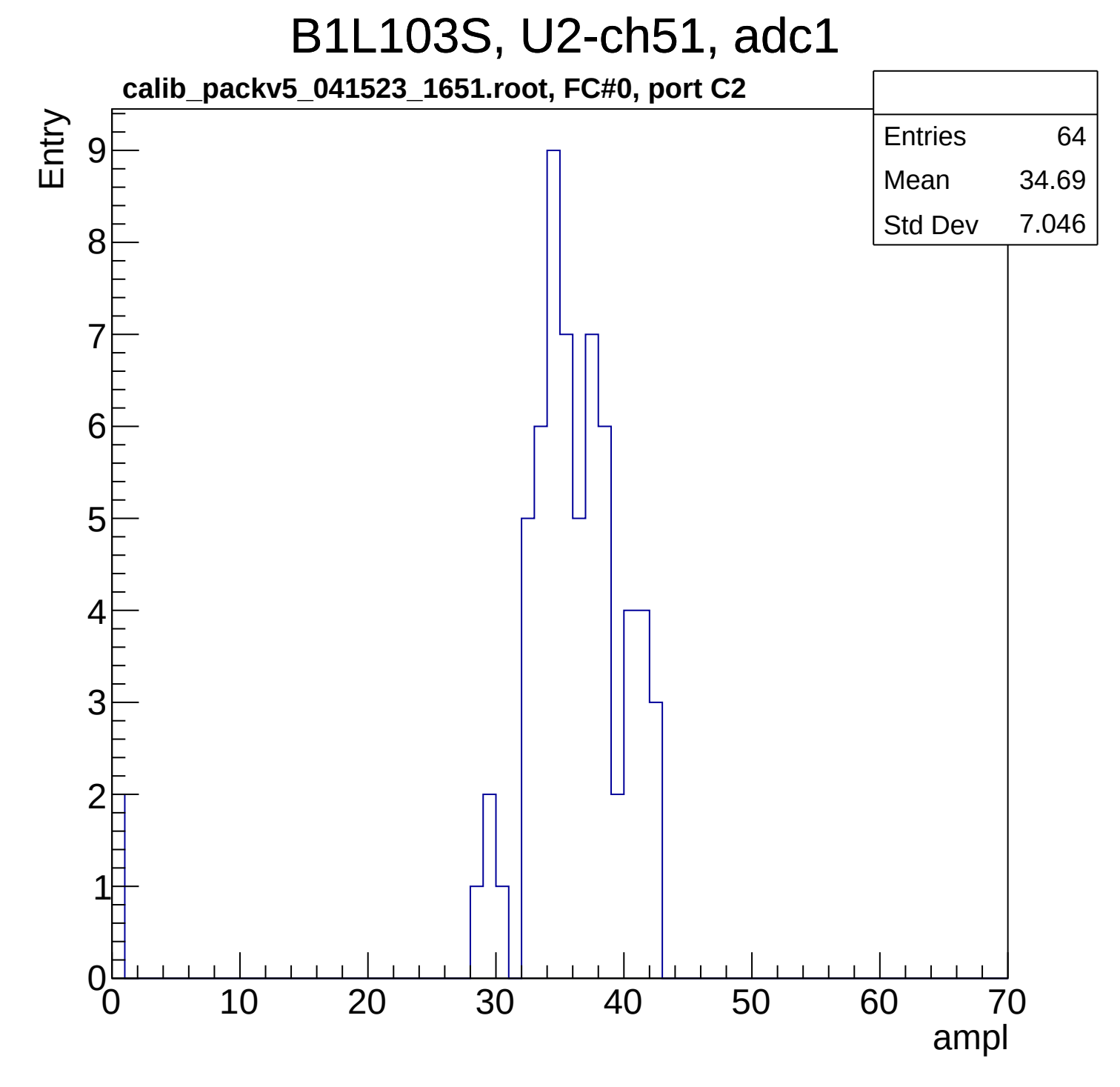

B1L103S, U2-ch50, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 53.02
Std Dev 2.912
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

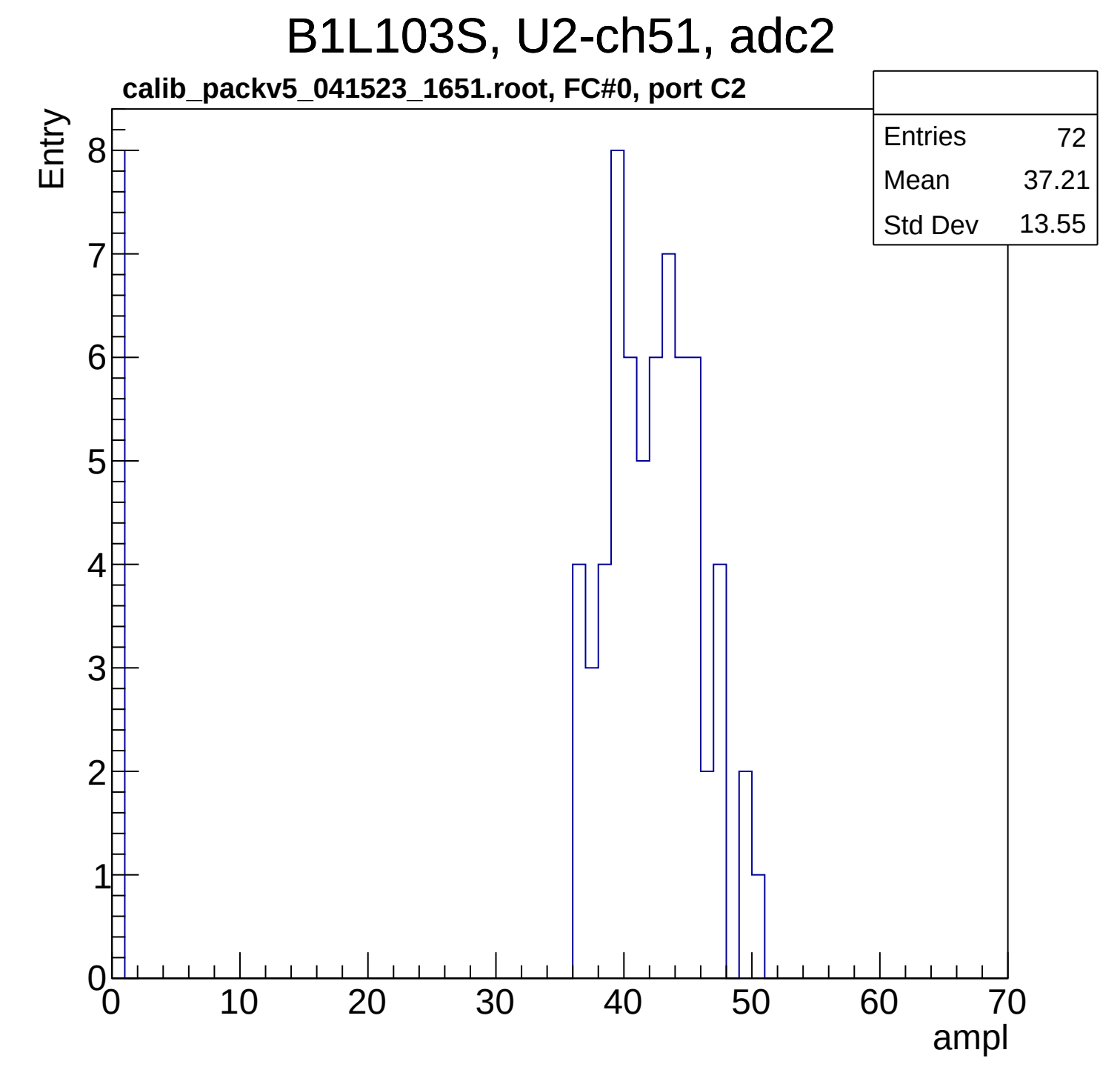

B1L103S, U2-ch50, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 57.53
Std Dev 7.658
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

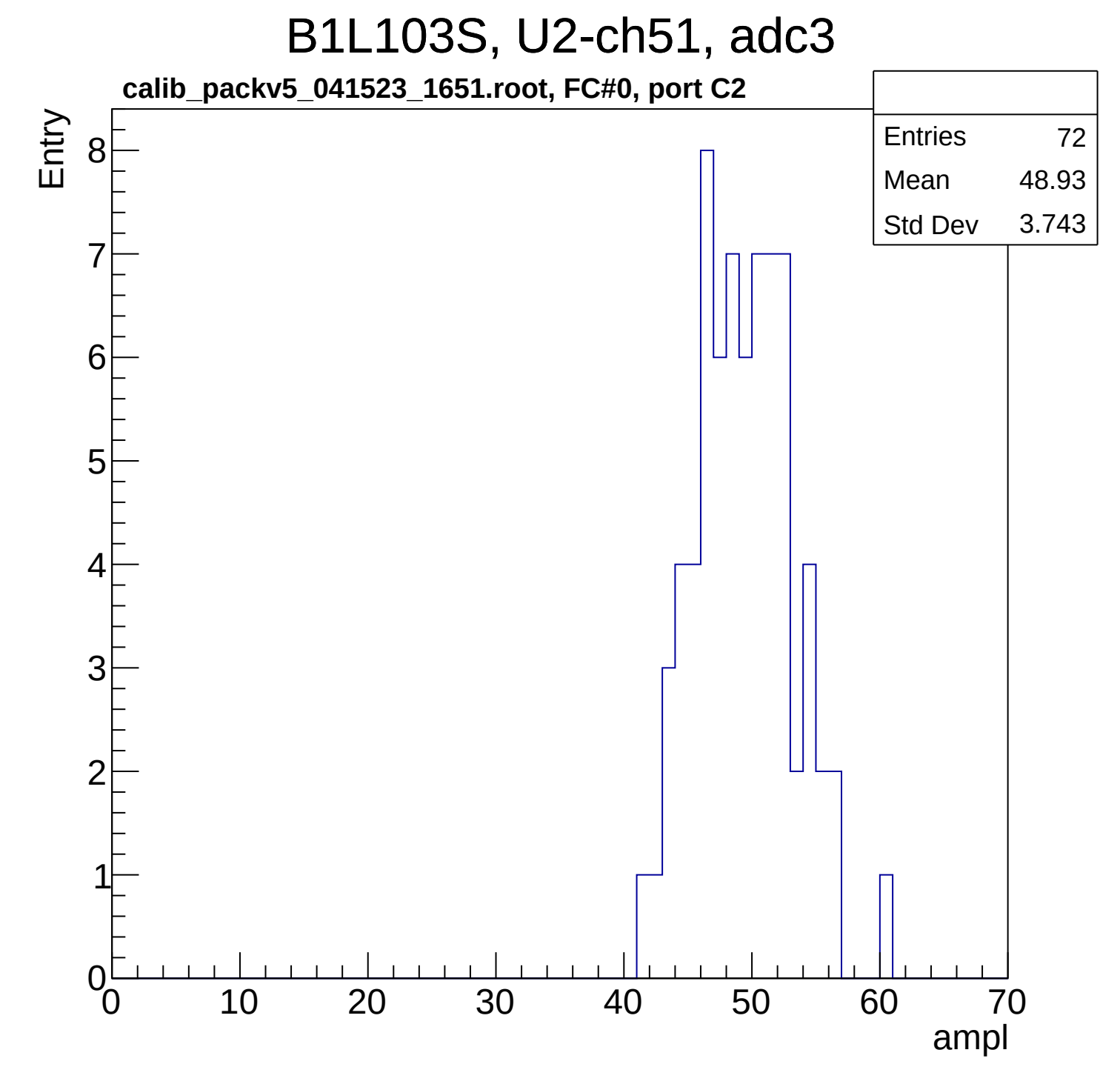

B1L103S, U2-ch50, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.21
Std Dev 2.366
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

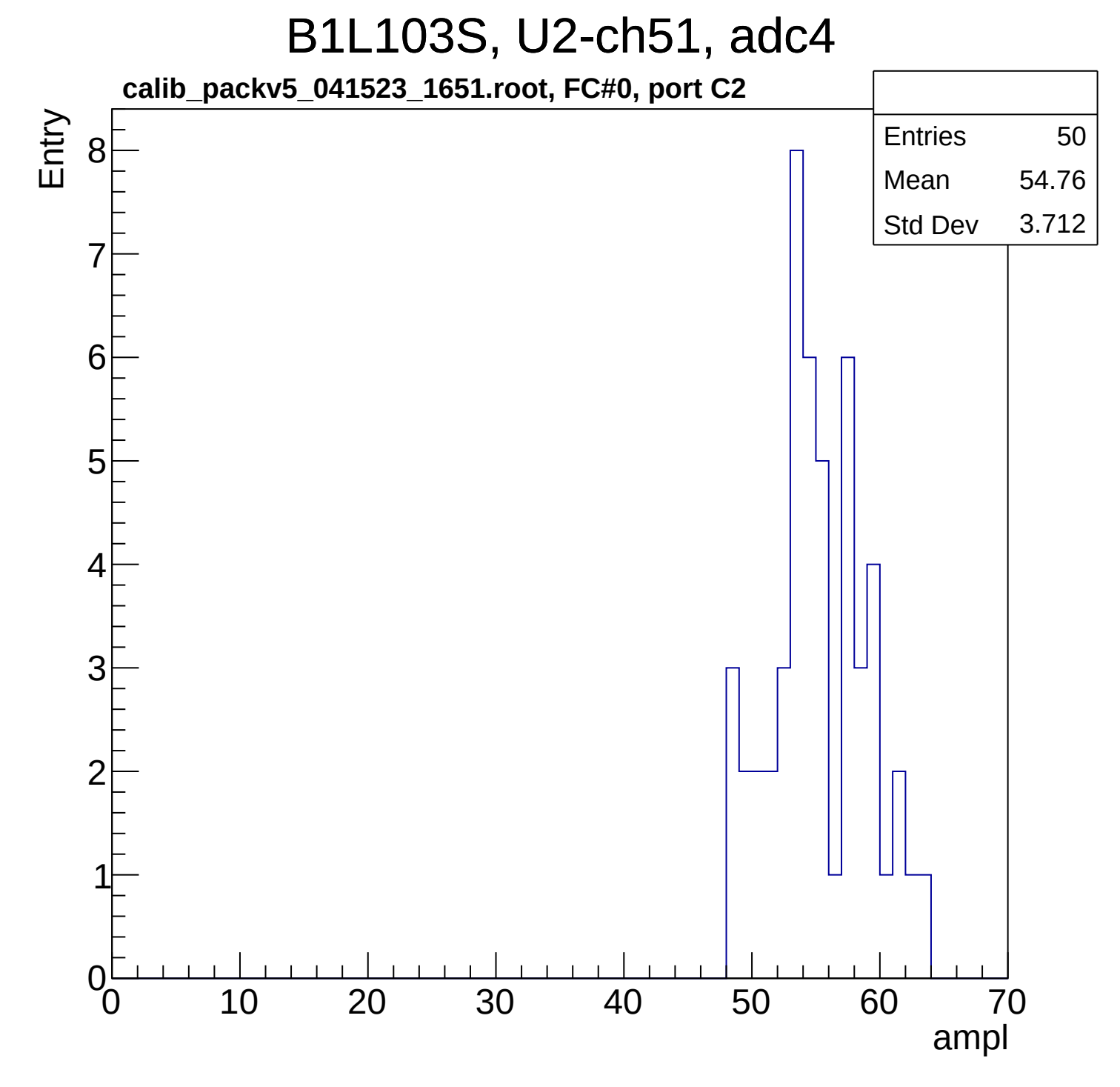

B1L103S, U2-ch50, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

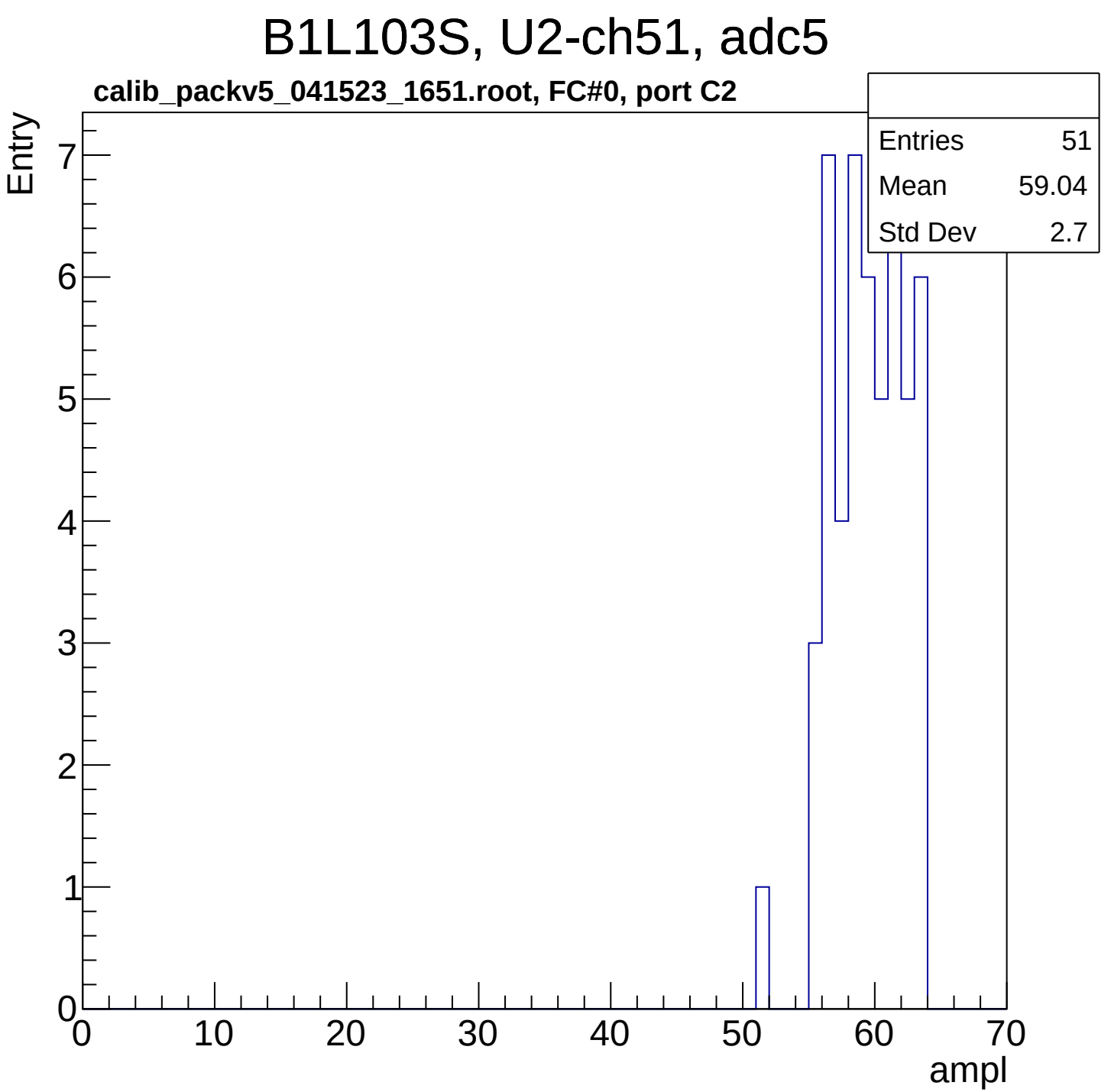

B1L103S, U2-ch51, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 23.87
Std Dev 11.33
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

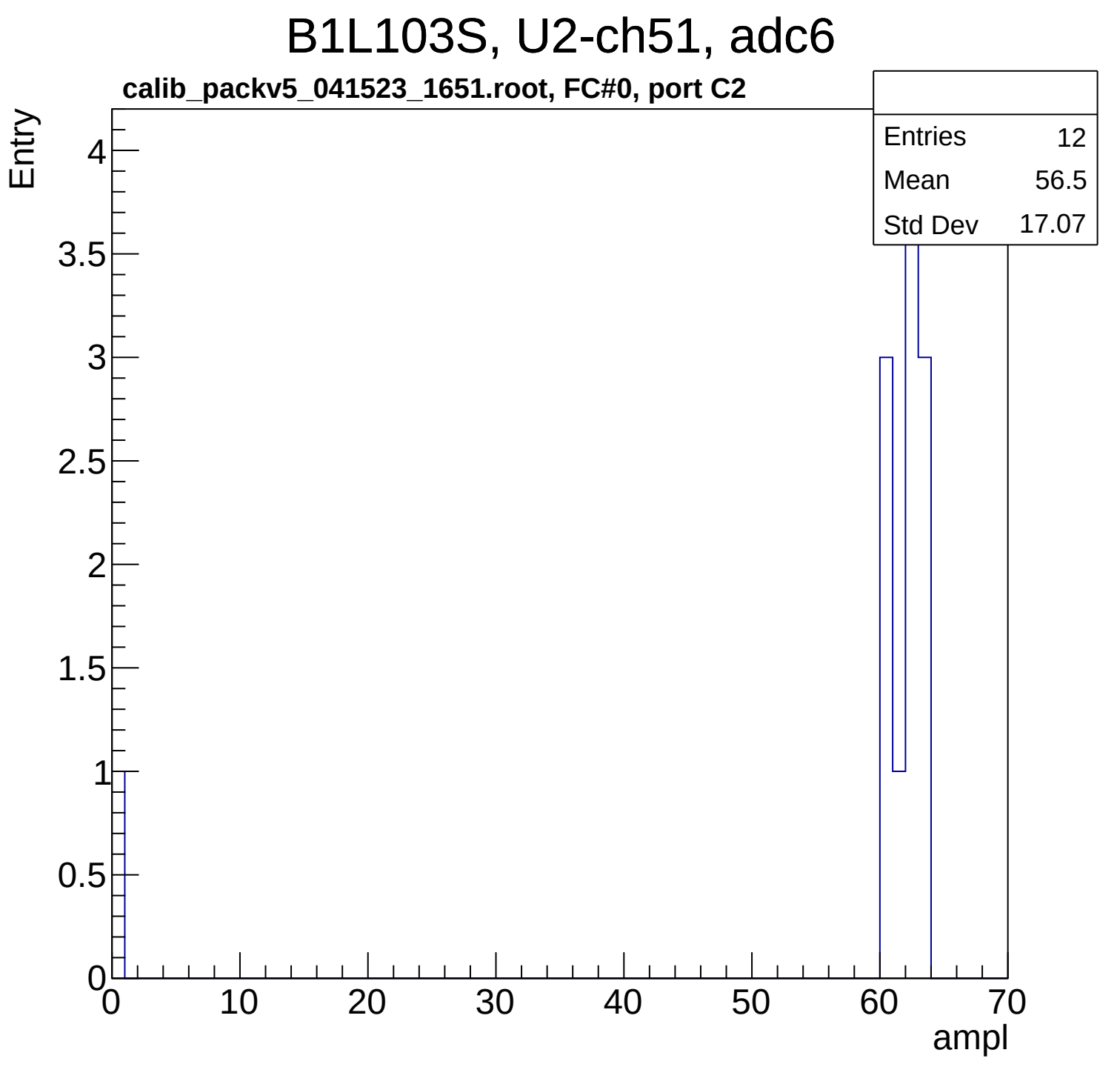

B1L103S, U2-ch51, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 34.69
Std Dev 7.046
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

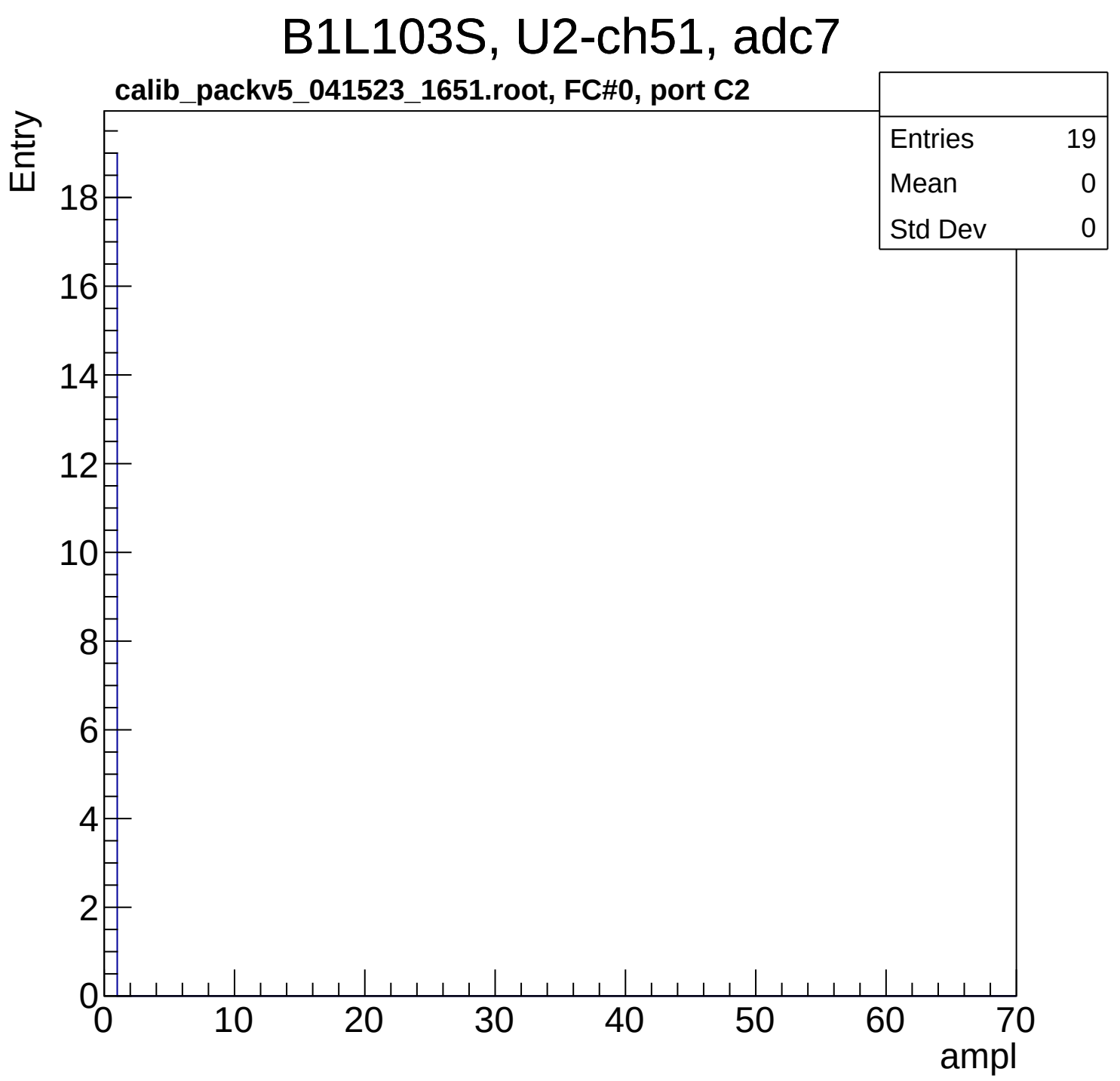

B1L103S, U2-ch51, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 37.21
Std Dev 13.55
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

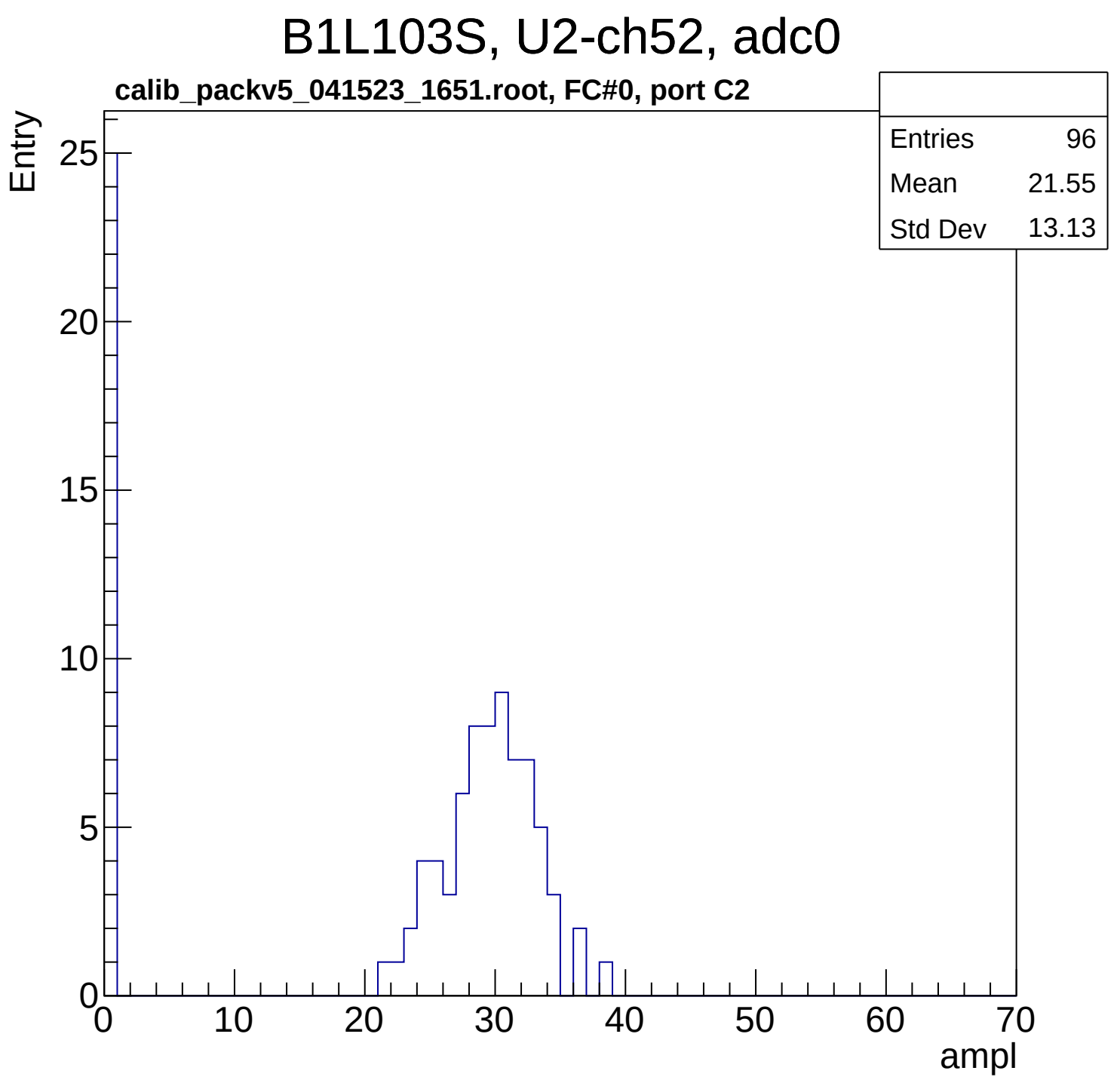

B1L103S, U2-ch51, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 48.93
Std Dev 3.743
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

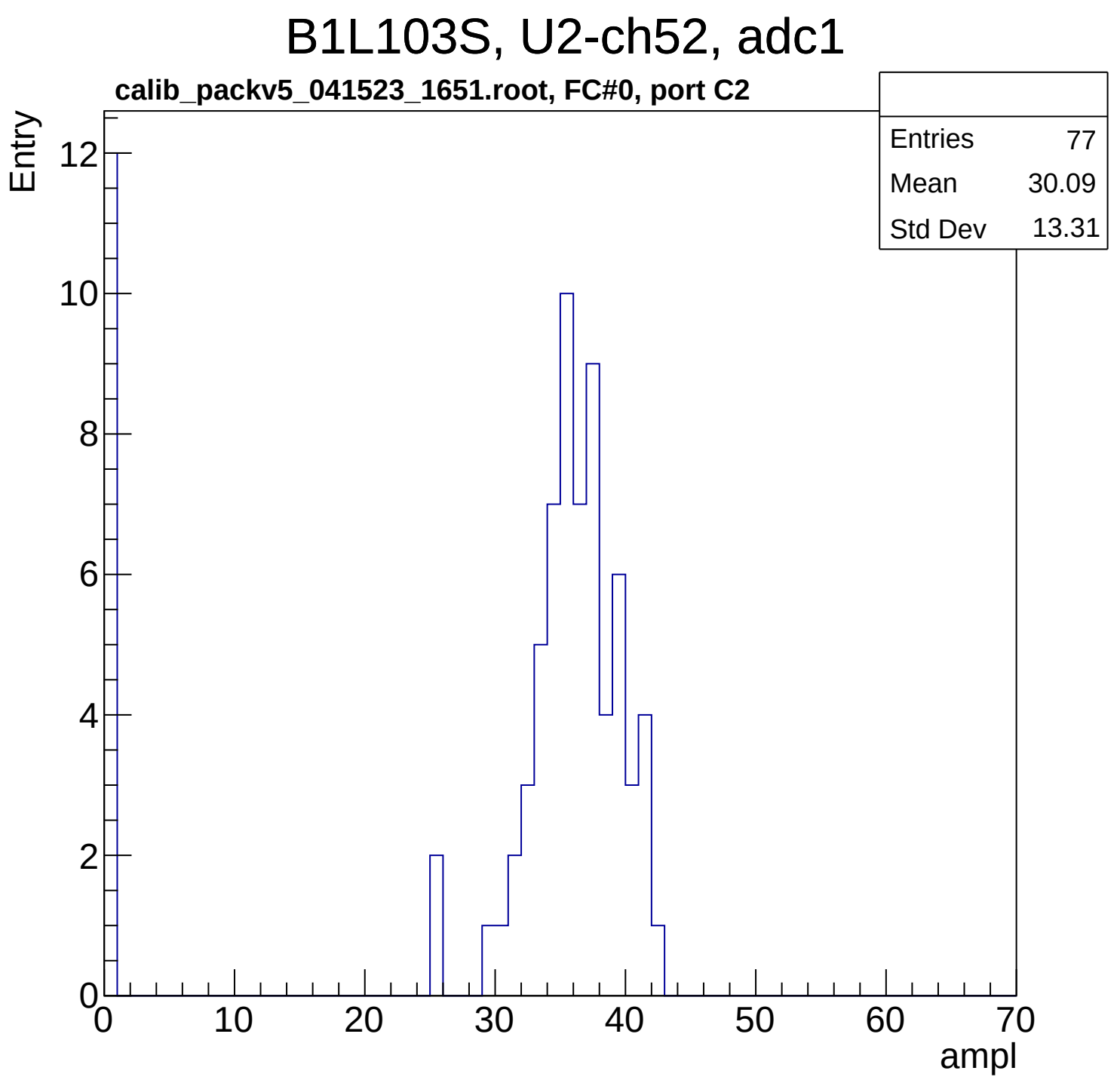

B1L103S, U2-ch51, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 54.76
Std Dev 3.712
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

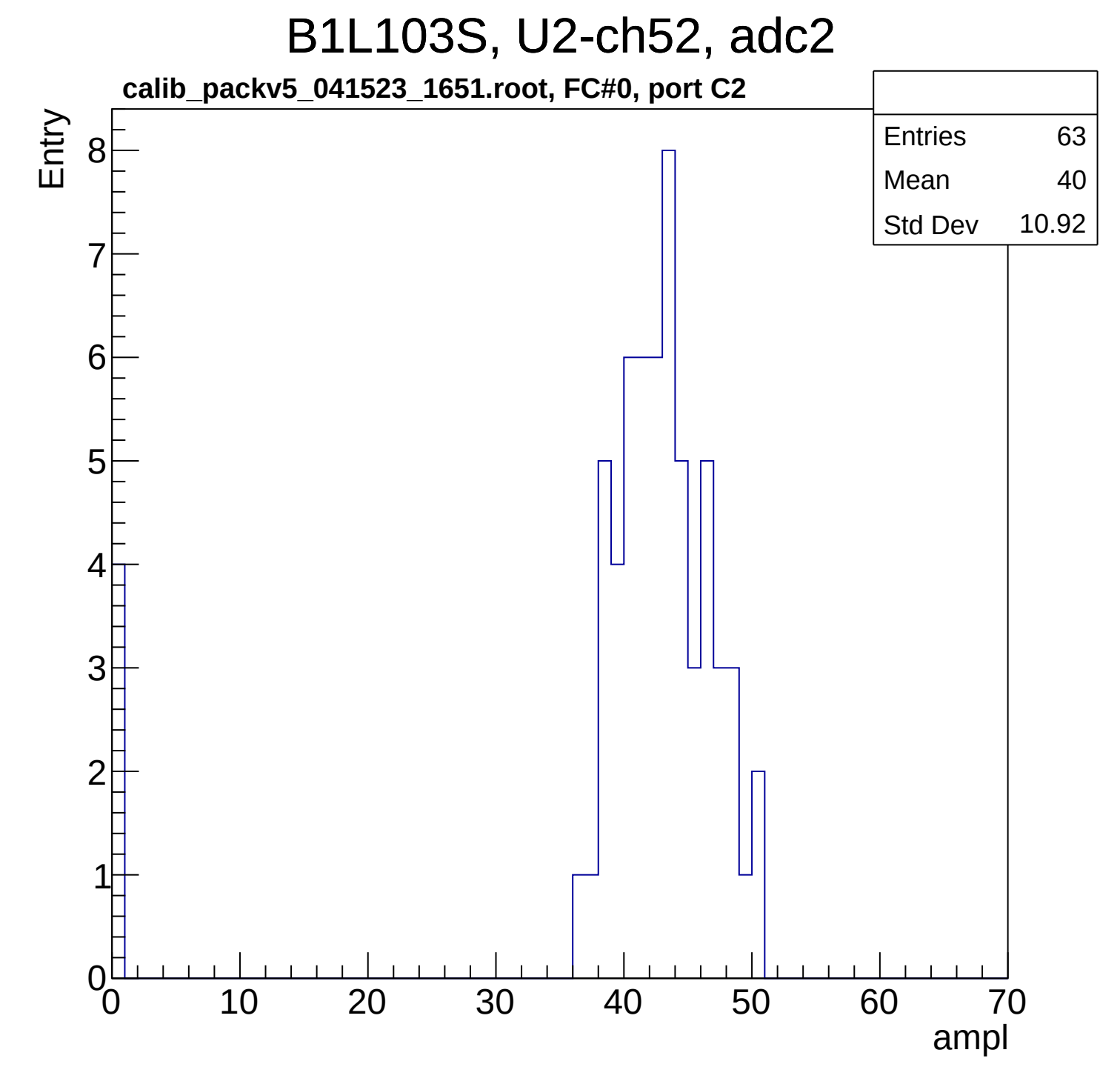

B1L103S, U2-ch51, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 59.04
Std Dev 2.7
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

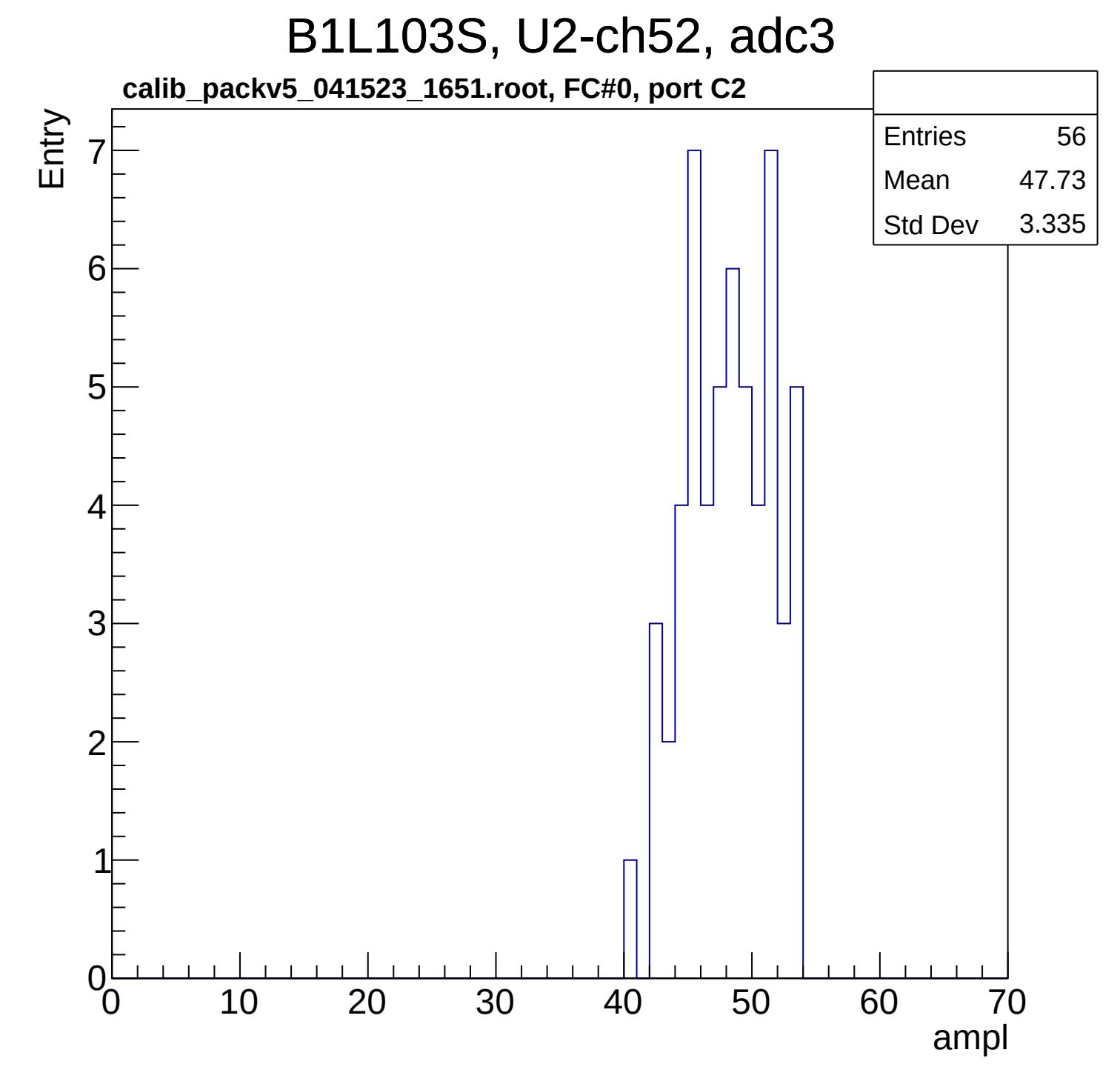

B1L103S, U2-ch51, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.5
Std Dev 17.07
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

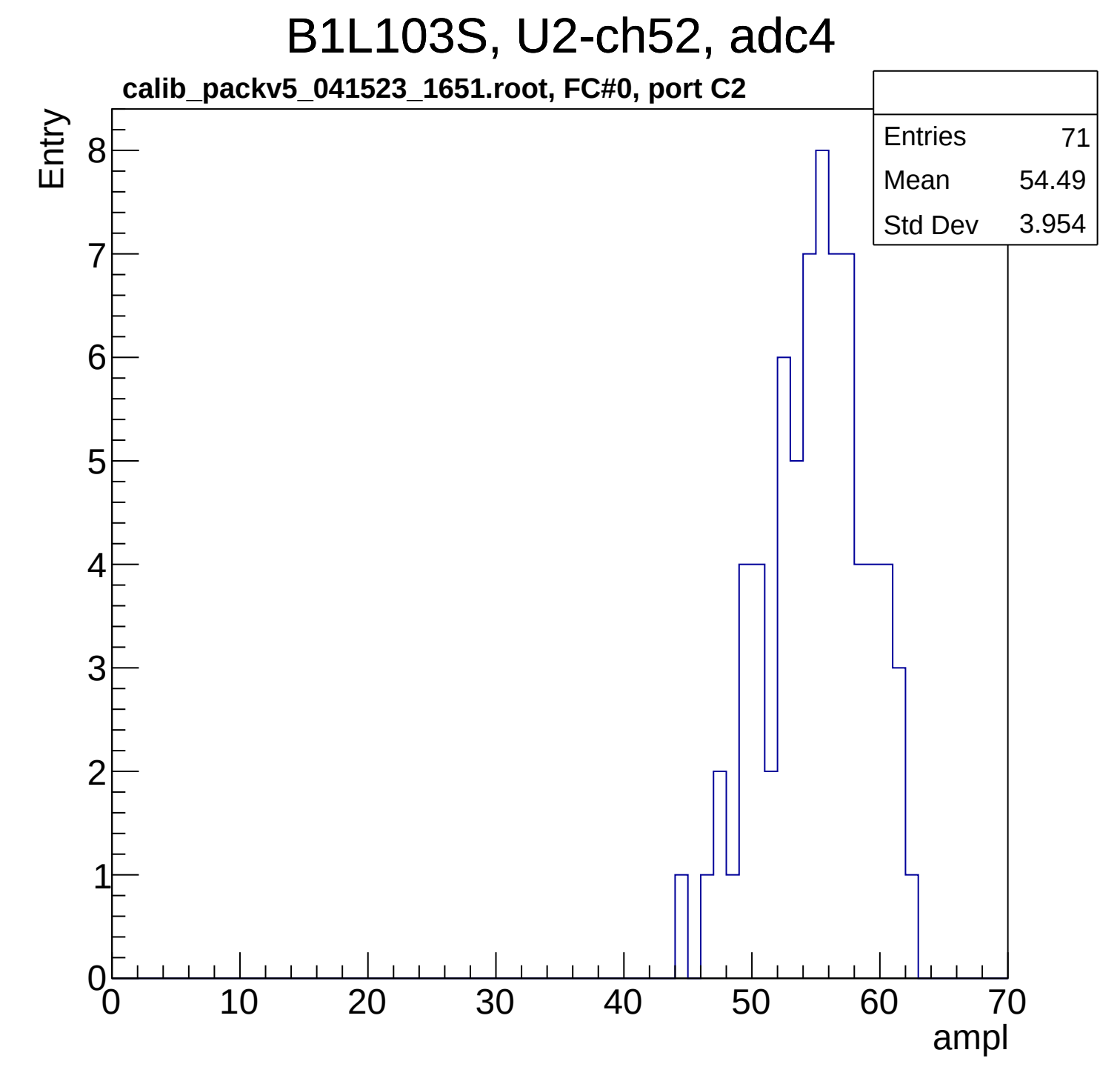

B1L103S, U2-ch51, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

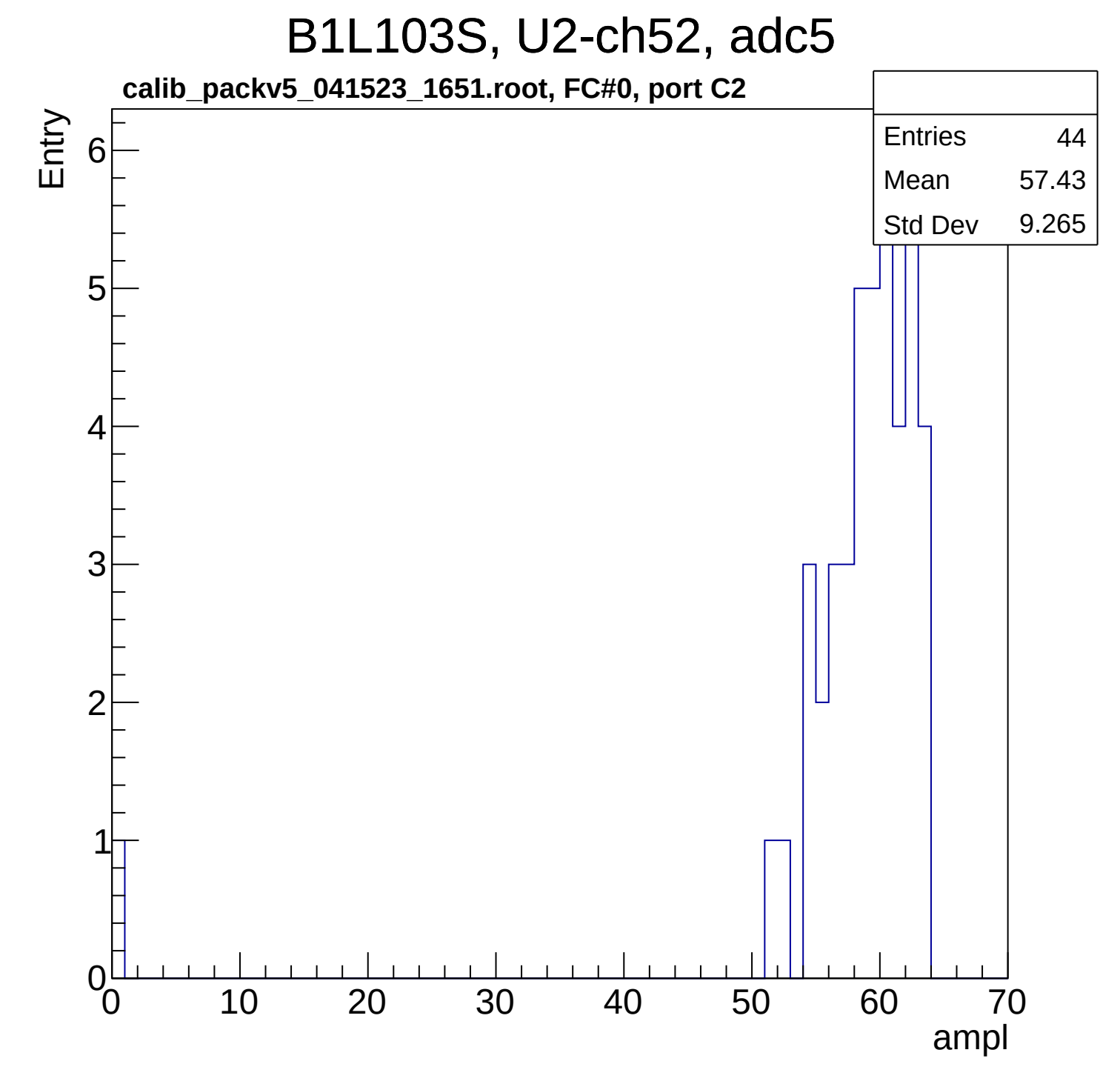

B1L103S, U2-ch52, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 21.55
Std Dev 13.13
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl

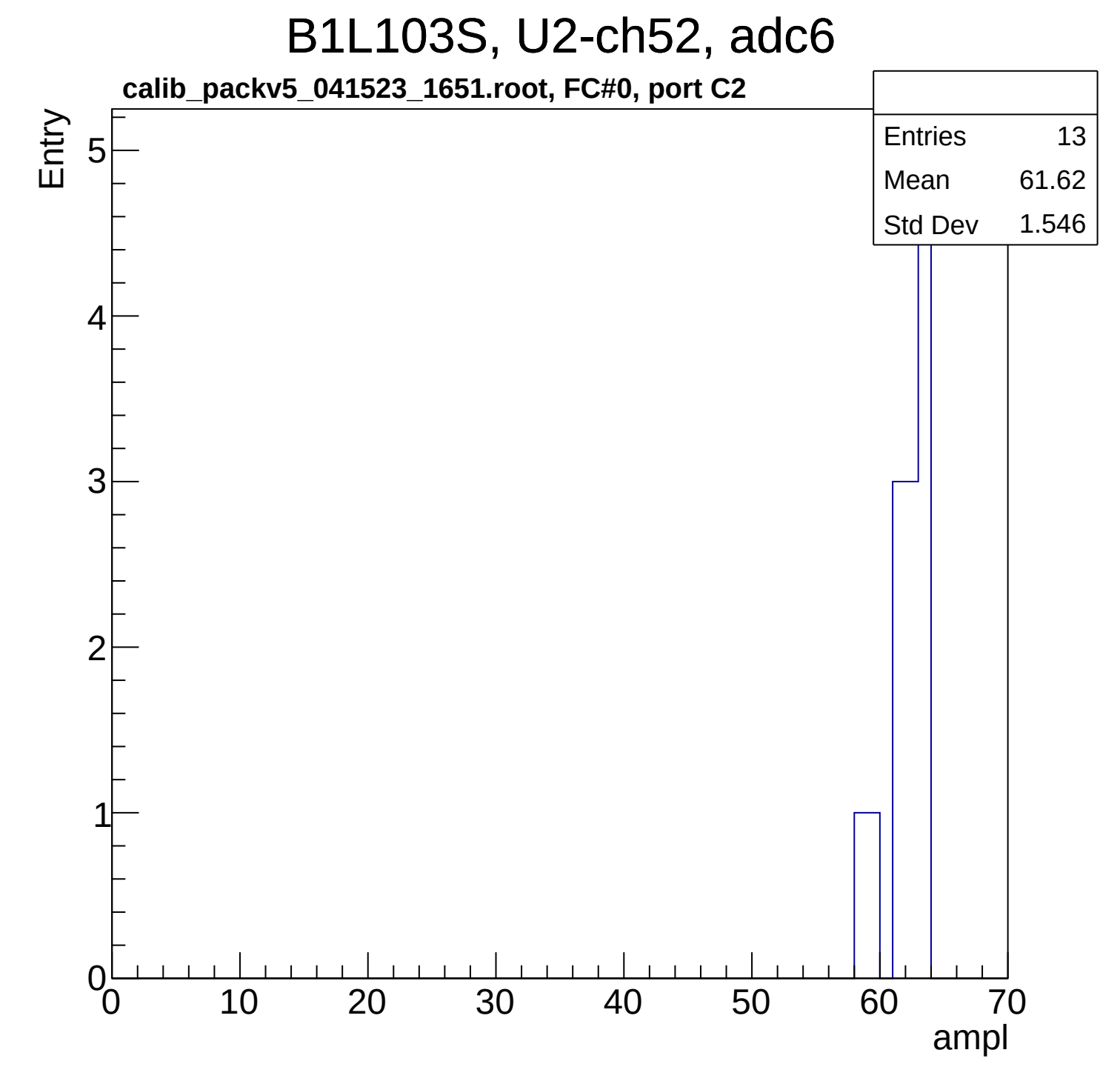

B1L103S, U2-ch52, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 30.09
Std Dev 13.31
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

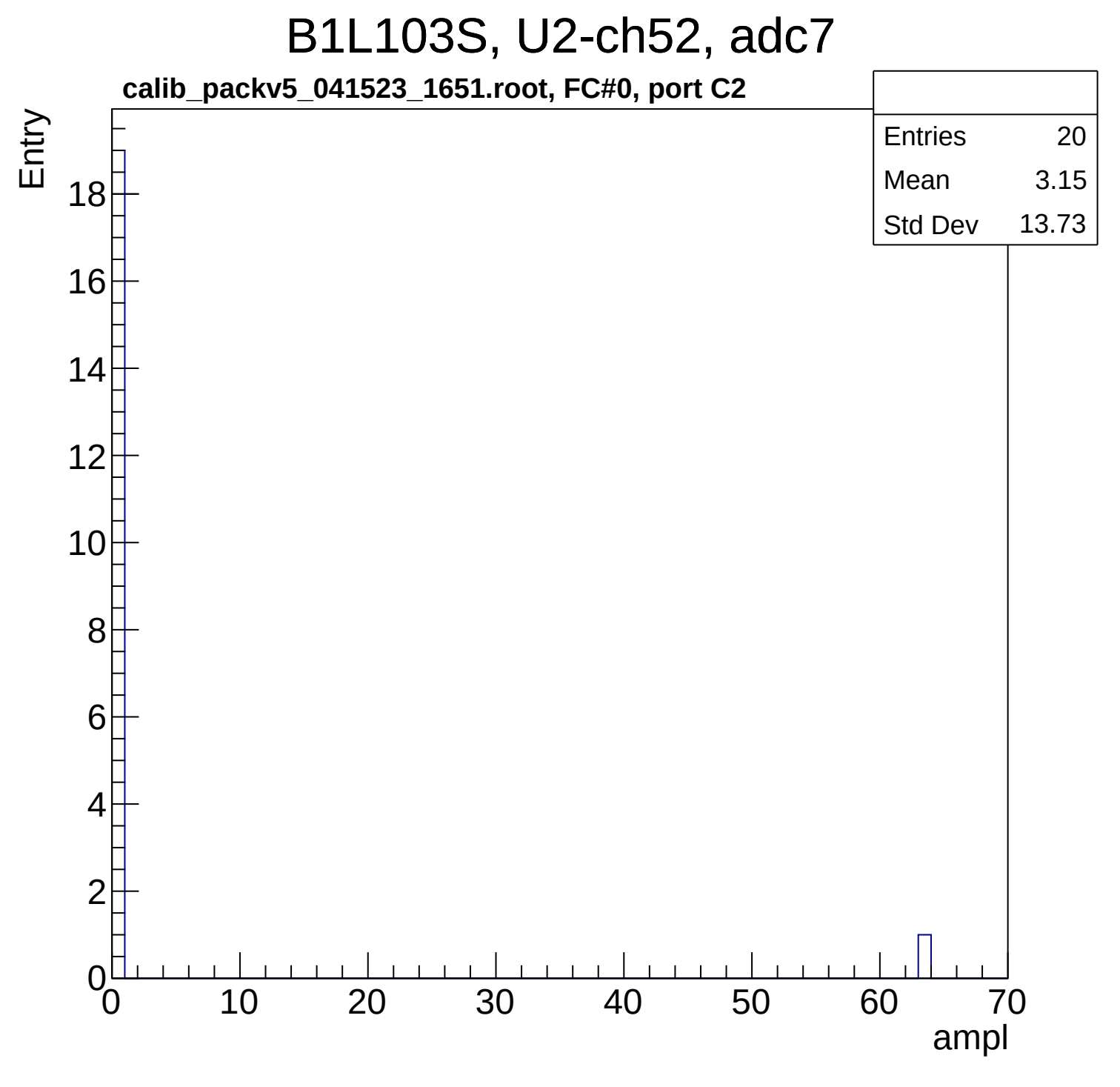

B1L103S, U2-ch52, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 40
Std Dev 10.92
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

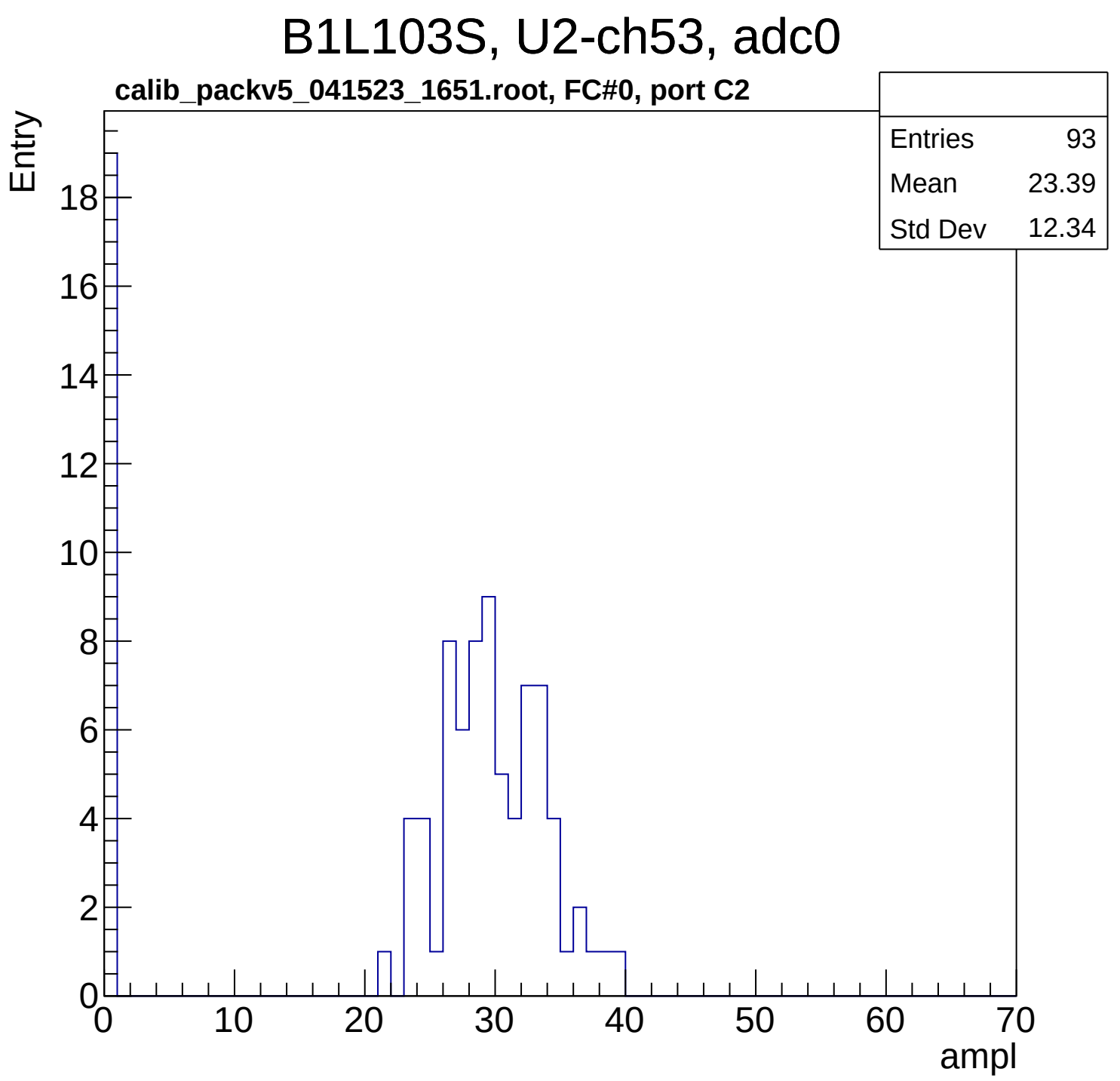

B1L103S, U2-ch52, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 47.73
Std Dev 3.335
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

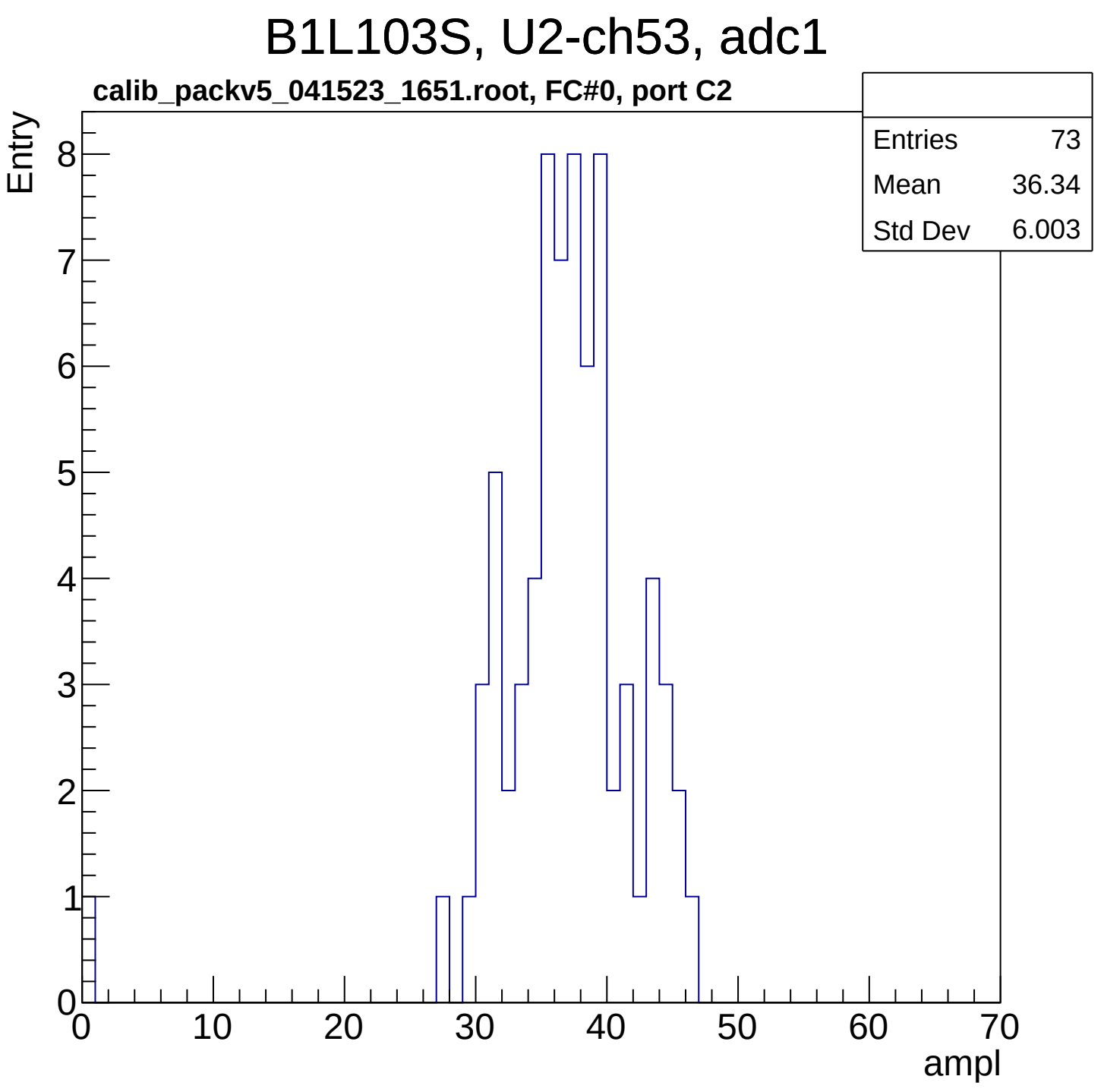

B1L103S, U2-ch52, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 54.49
Std Dev 3.954
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

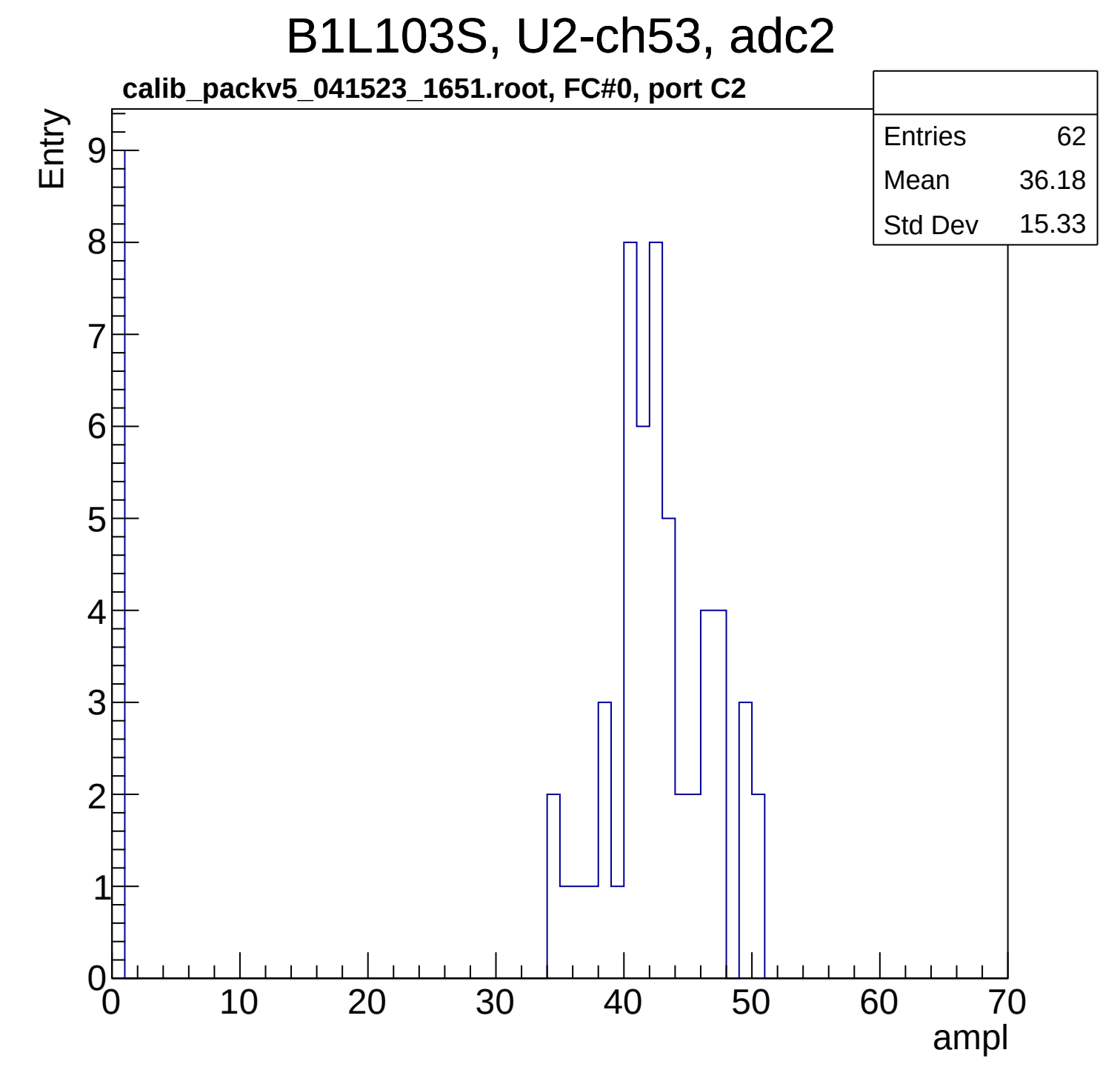

B1L103S, U2-ch52, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 57.43
Std Dev 9.265
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

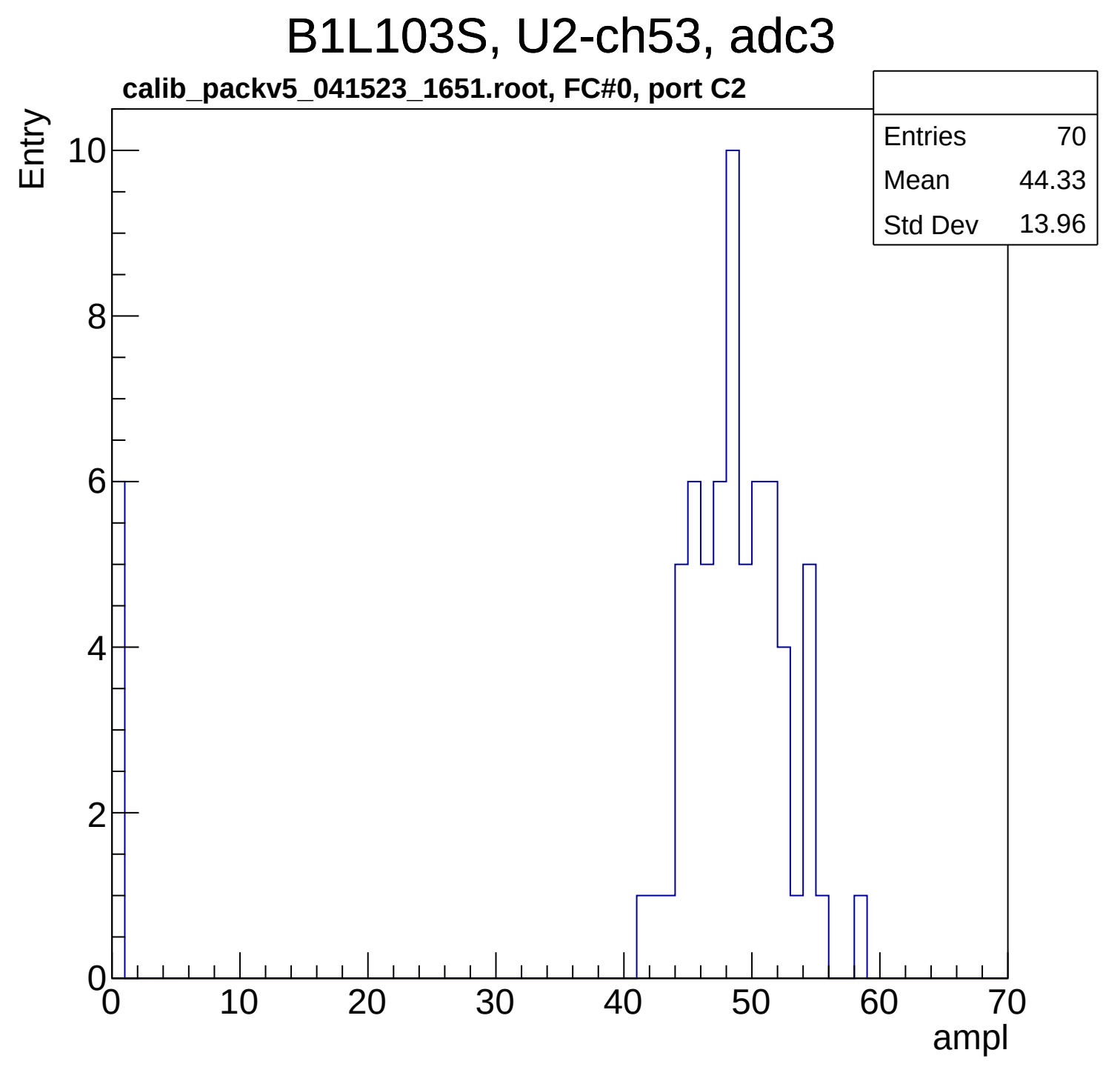

B1L103S, U2-ch52, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.62
Std Dev 1.546
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

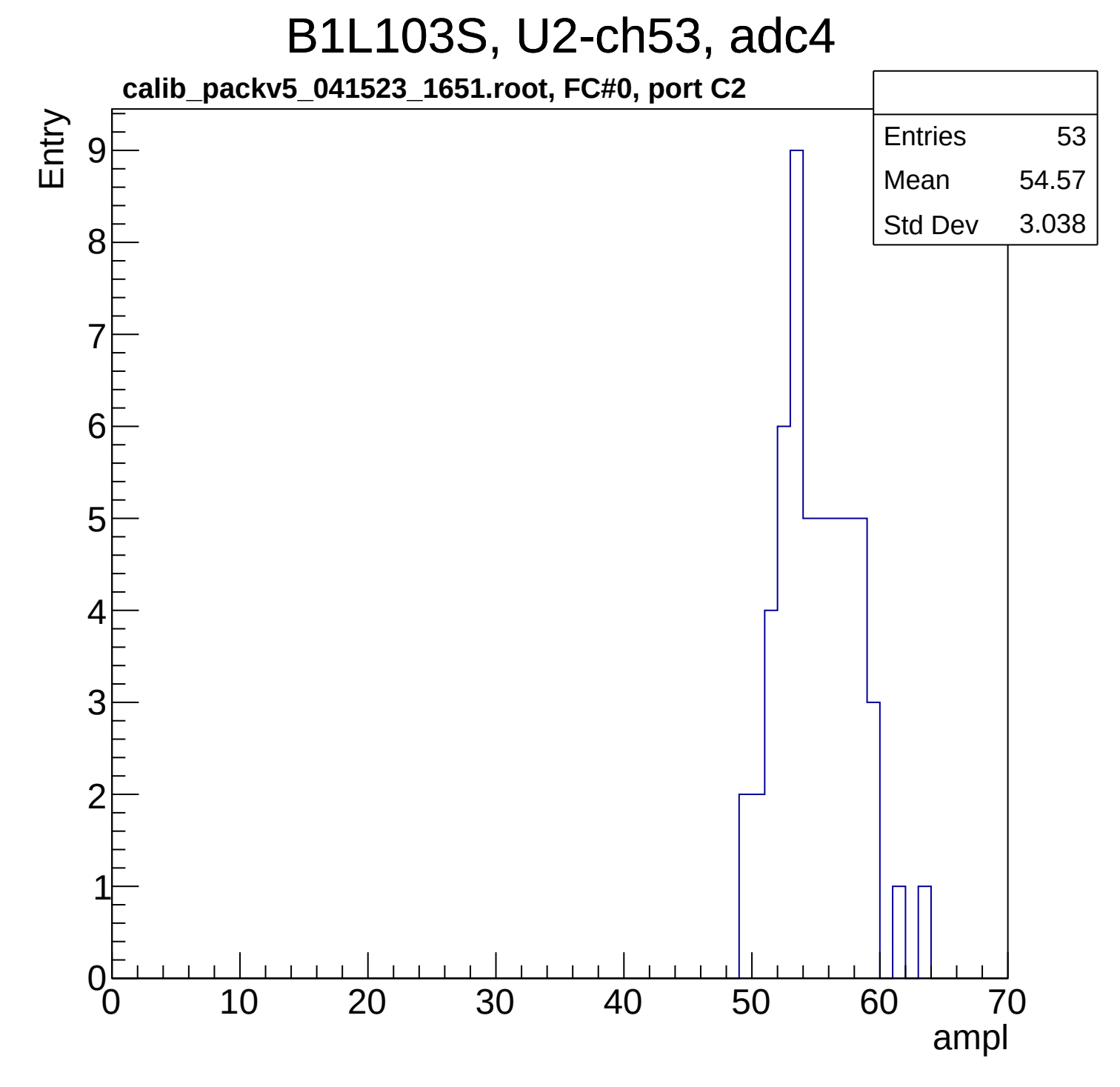

B1L103S, U2-ch52, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

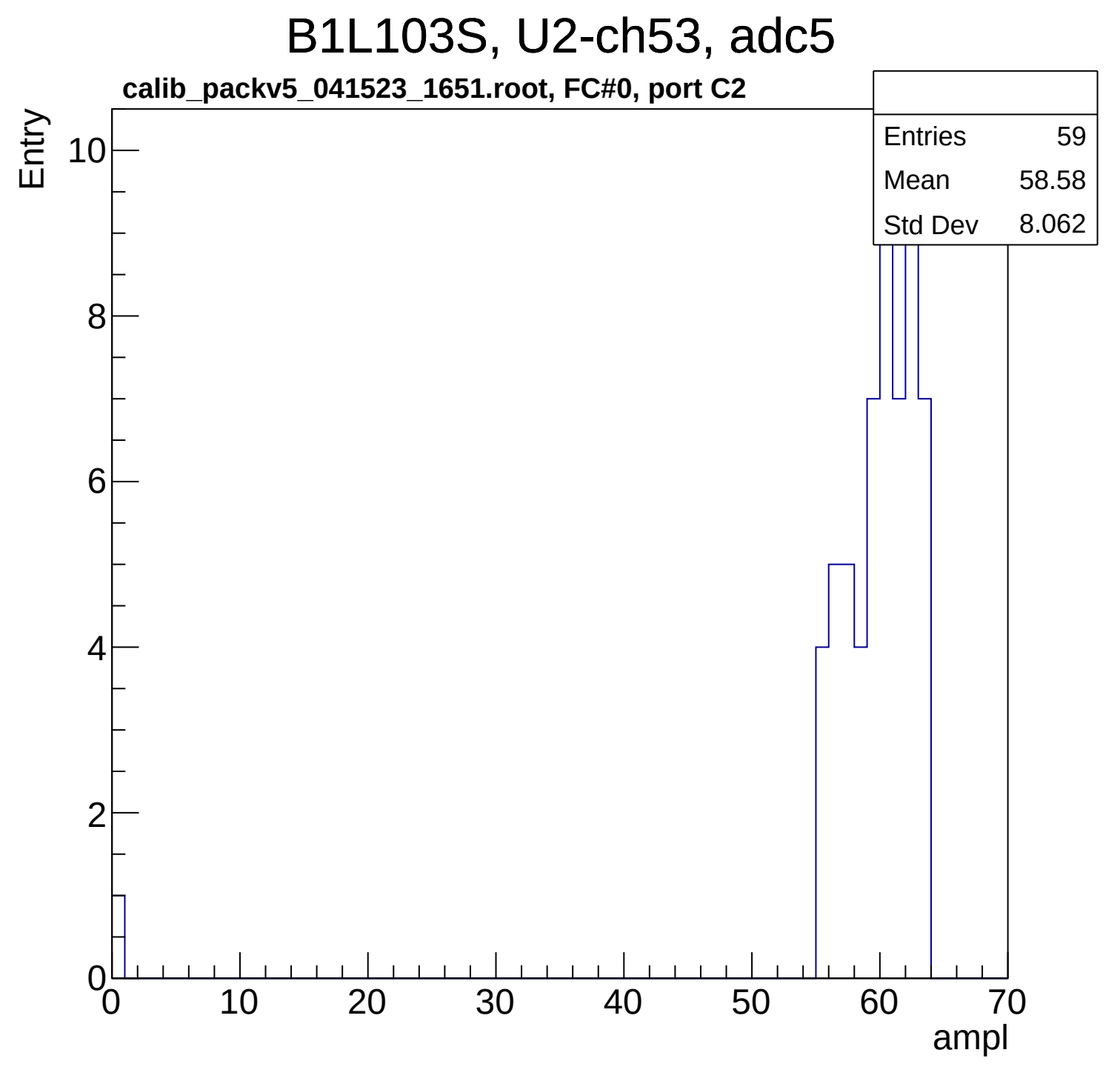

B1L103S, U2-ch53, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 23.39
Std Dev 12.34
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

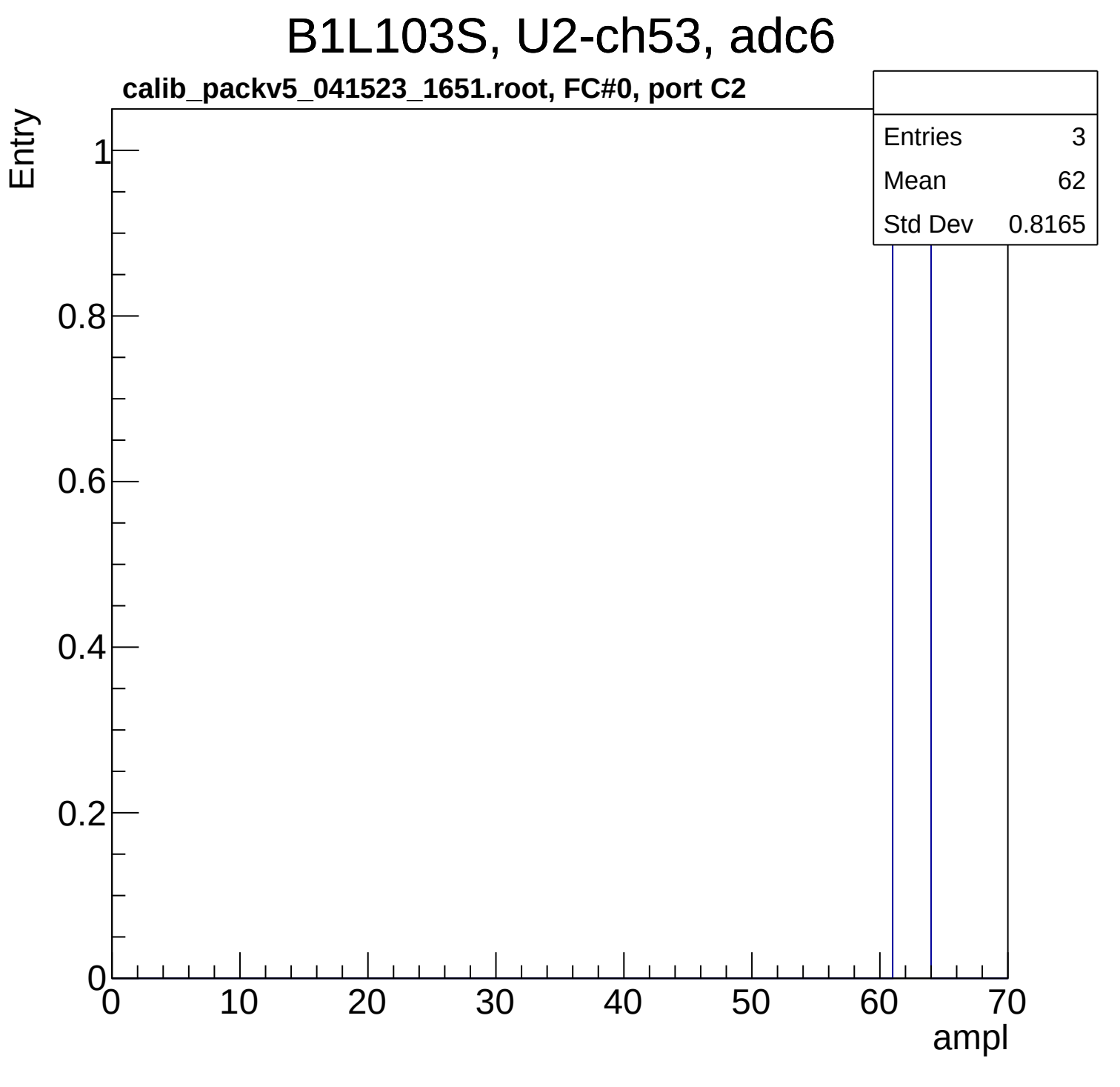

B1L103S, U2-ch53, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 36.34
Std Dev 6.003
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

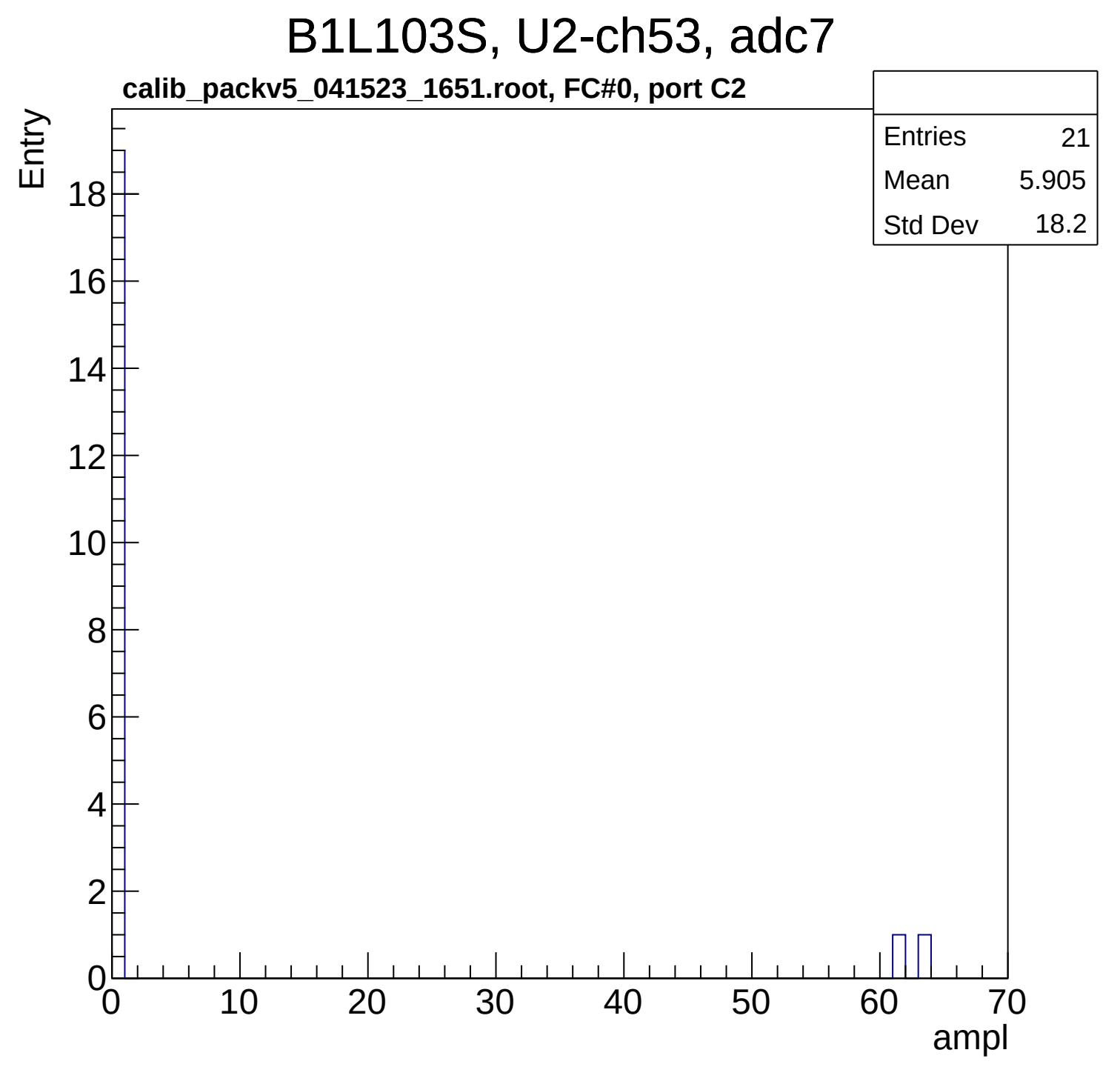

B1L103S, U2-ch53, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 36.18
Std Dev 15.33
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

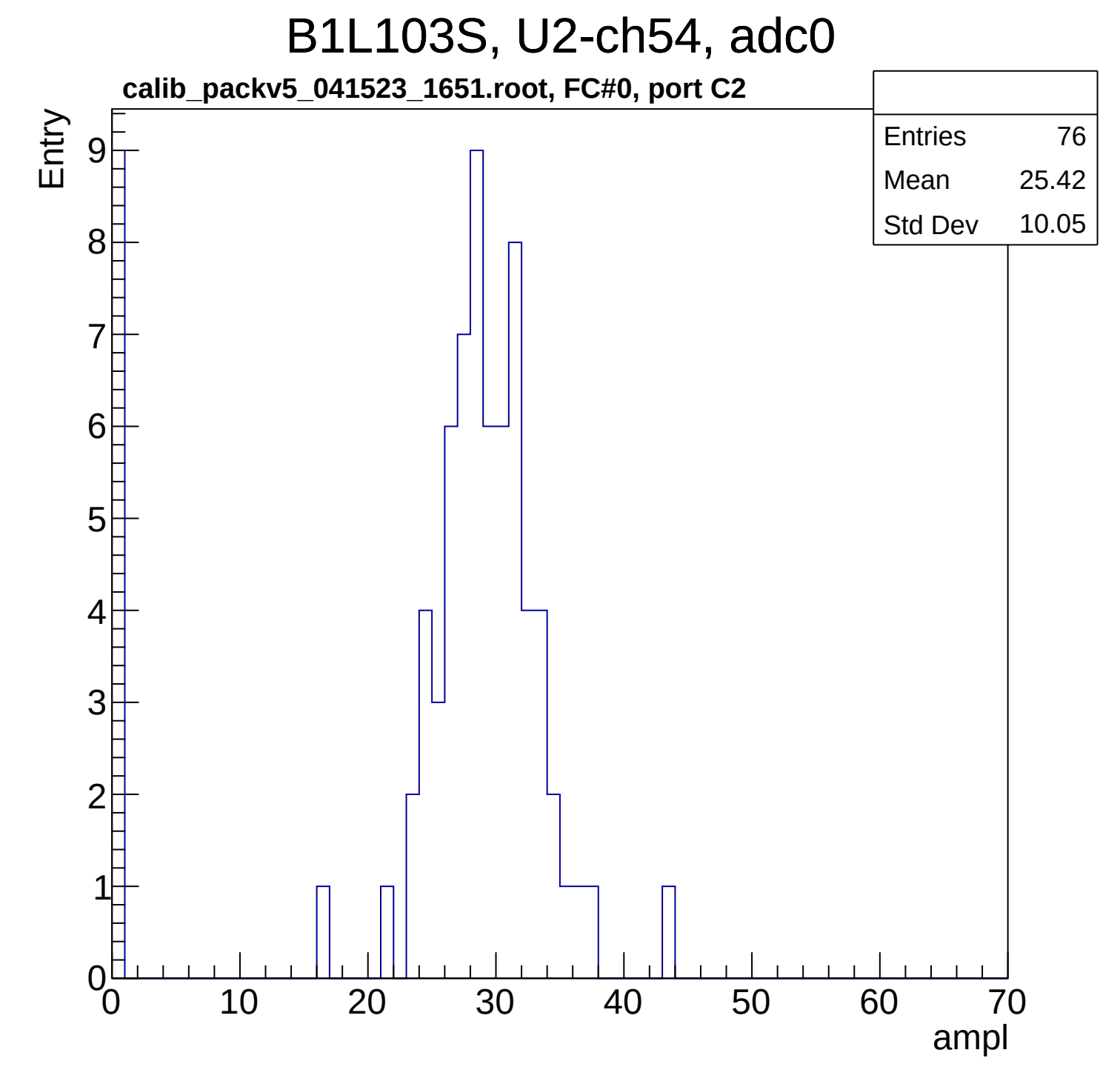

B1L103S, U2-ch53, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 44.33
Std Dev 13.96
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

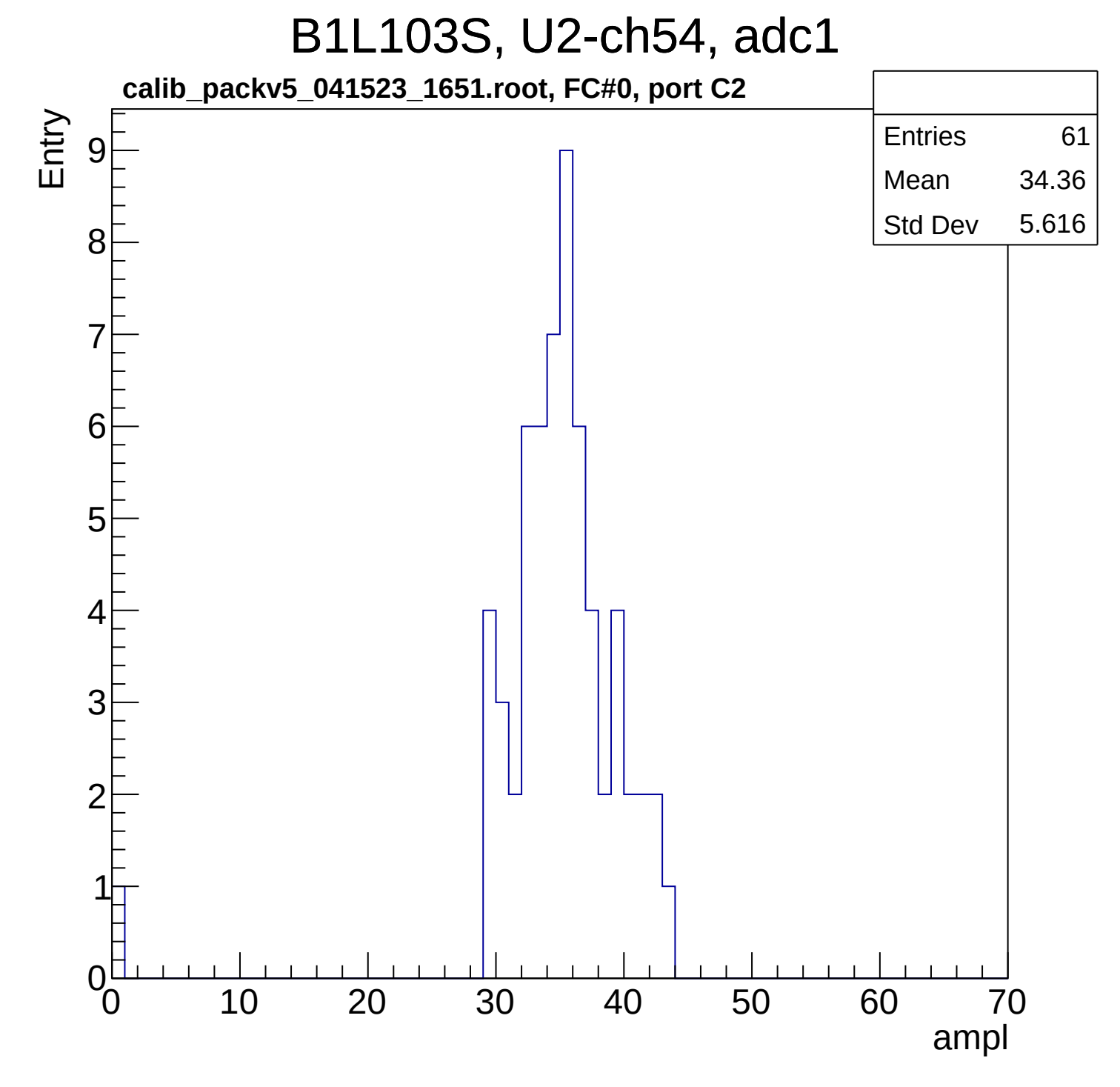

B1L103S, U2-ch53, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 54.57
Std Dev 3.038
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

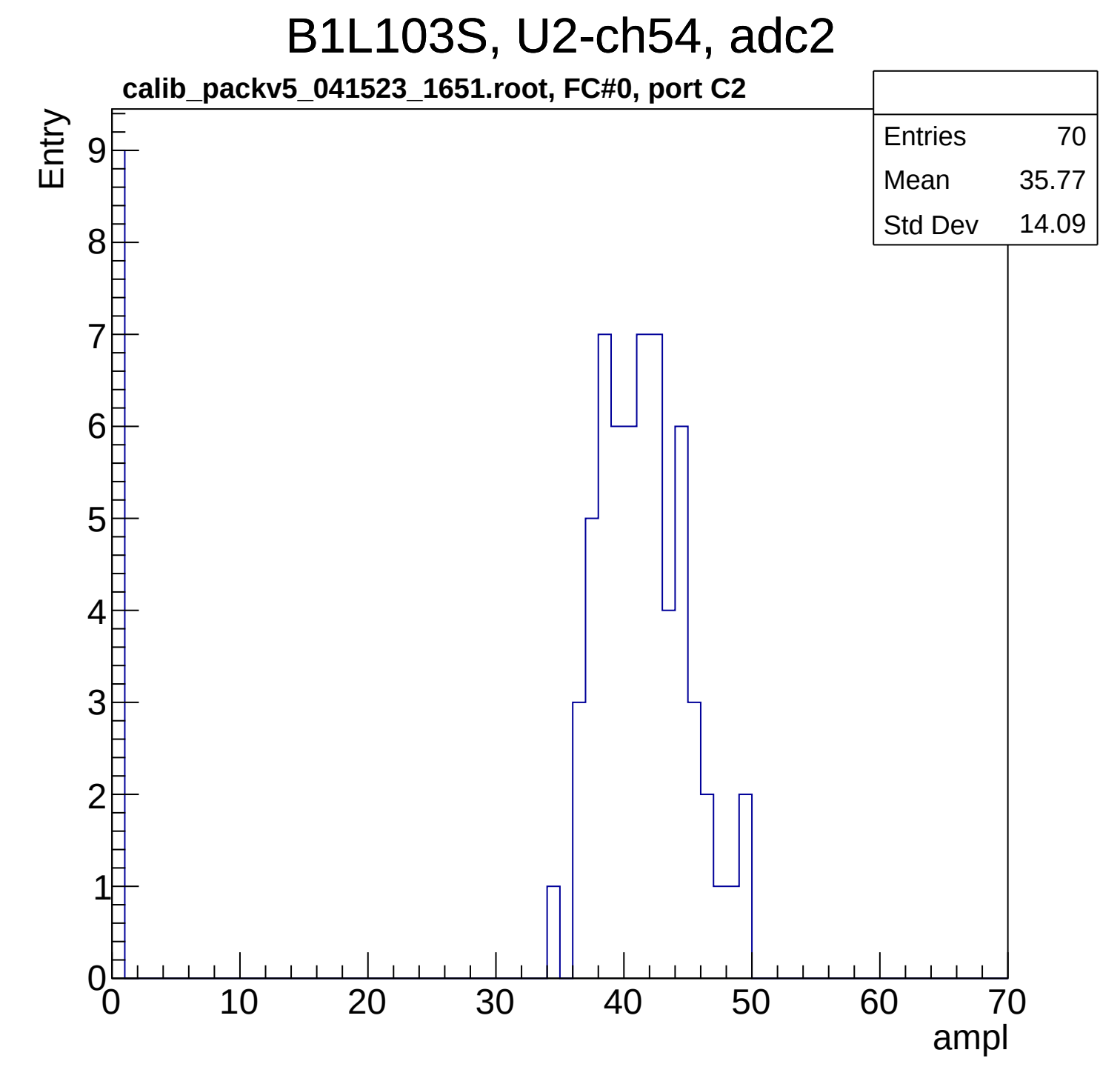

B1L103S, U2-ch53, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 58.58
Std Dev 8.062
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

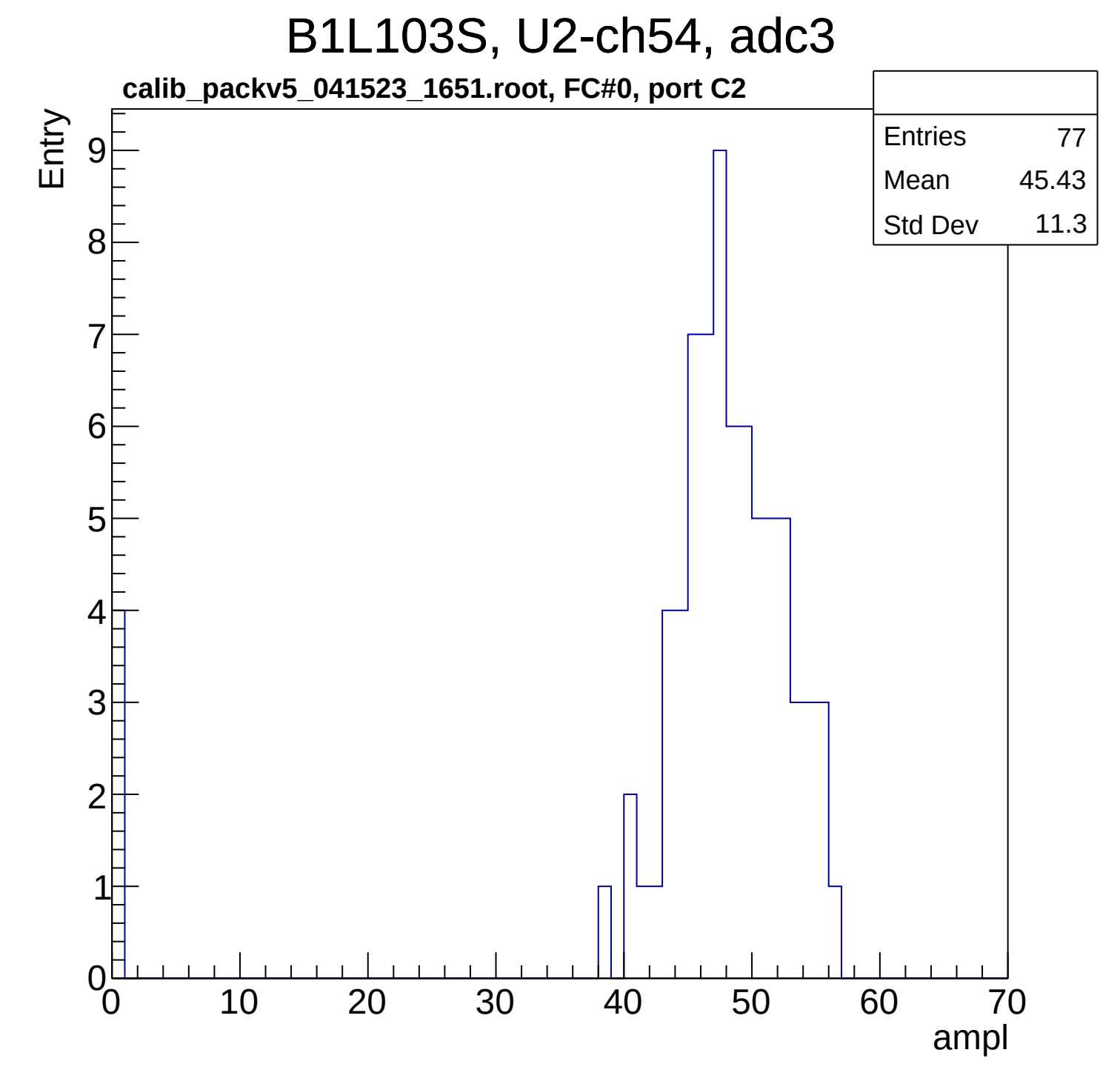

B1L103S, U2-ch53, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62
Std Dev 0.8165
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

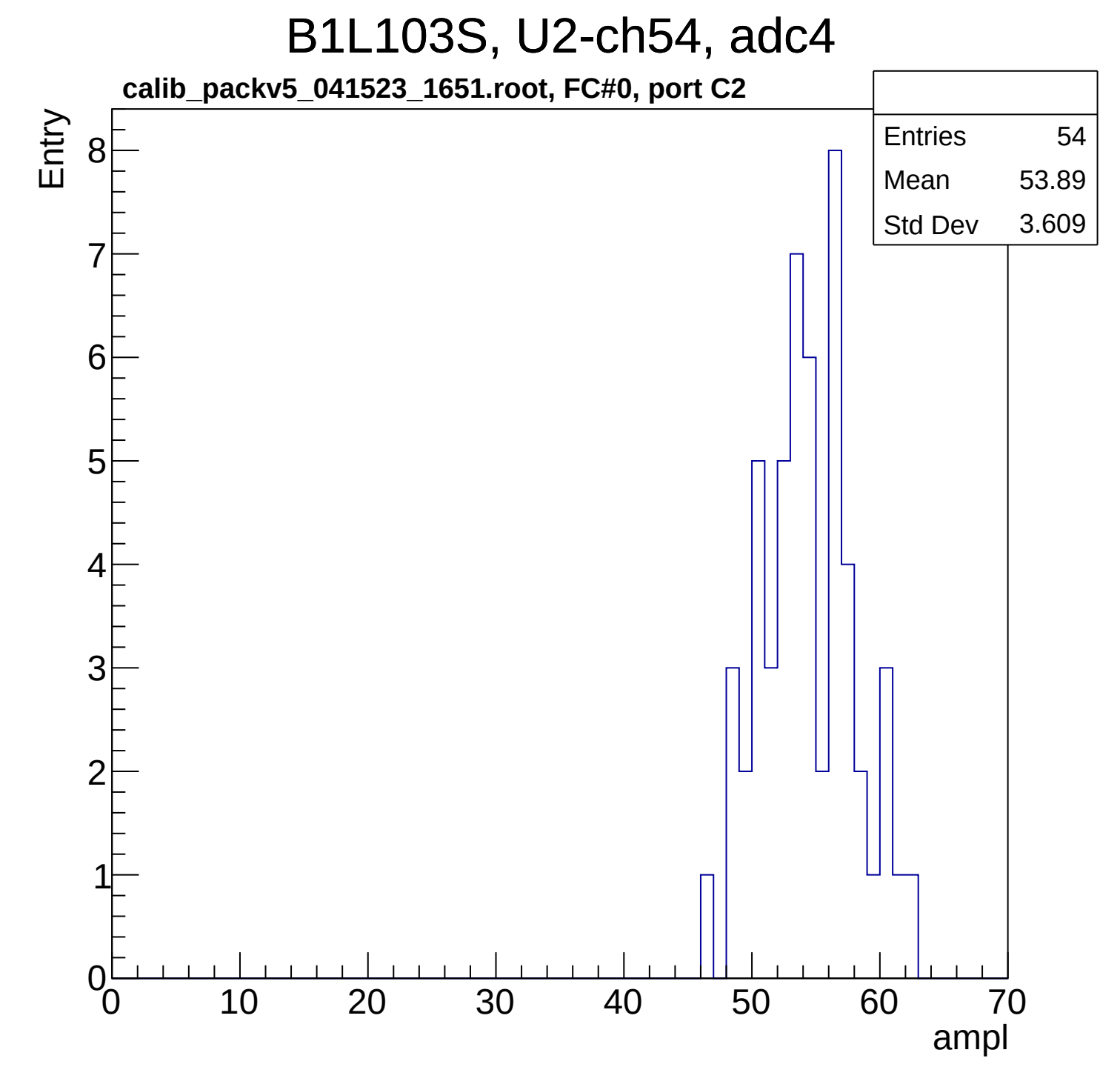

B1L103S, U2-ch53, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

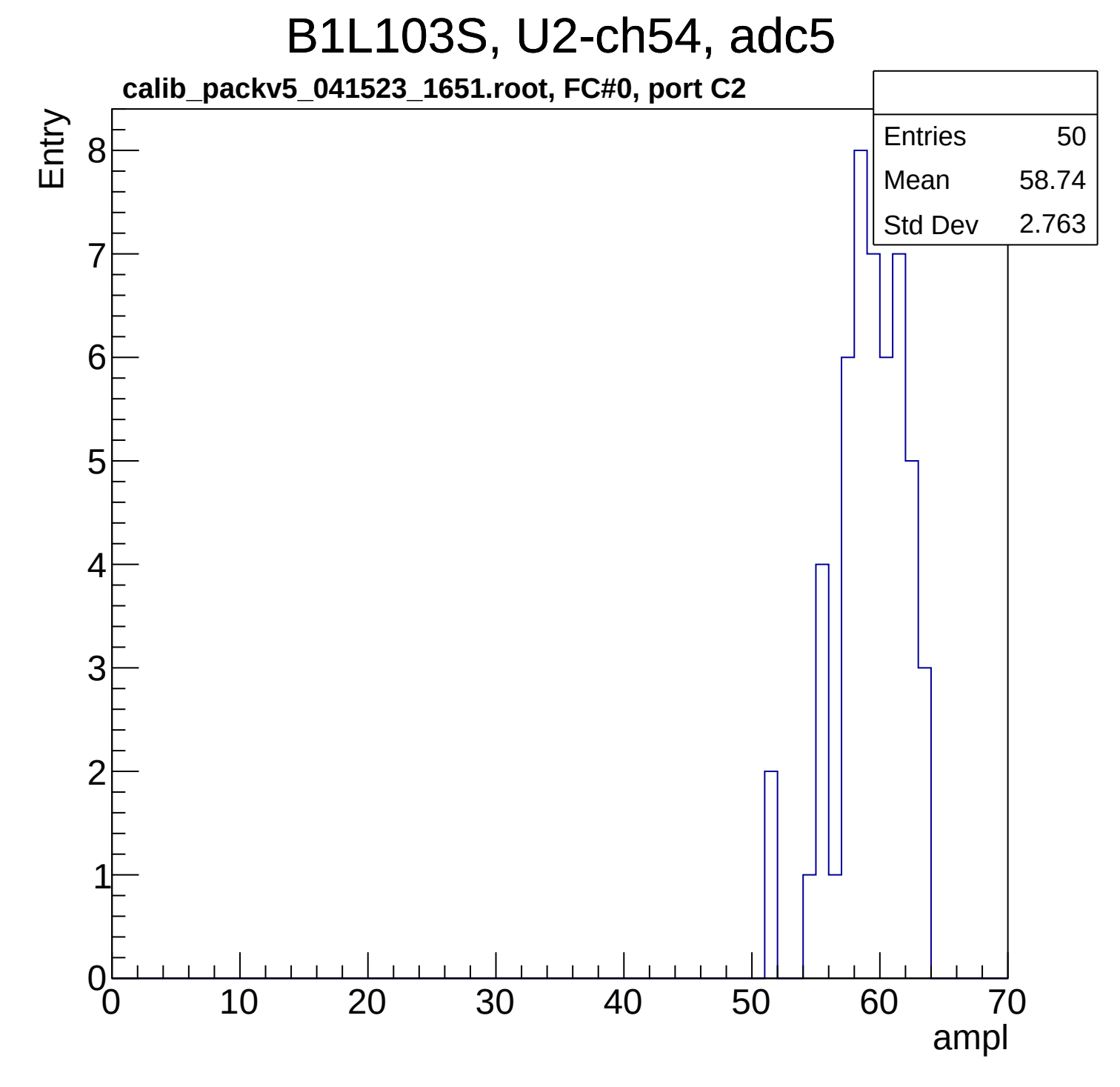

B1L103S, U2-ch54, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 25.42
Std Dev 10.05
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

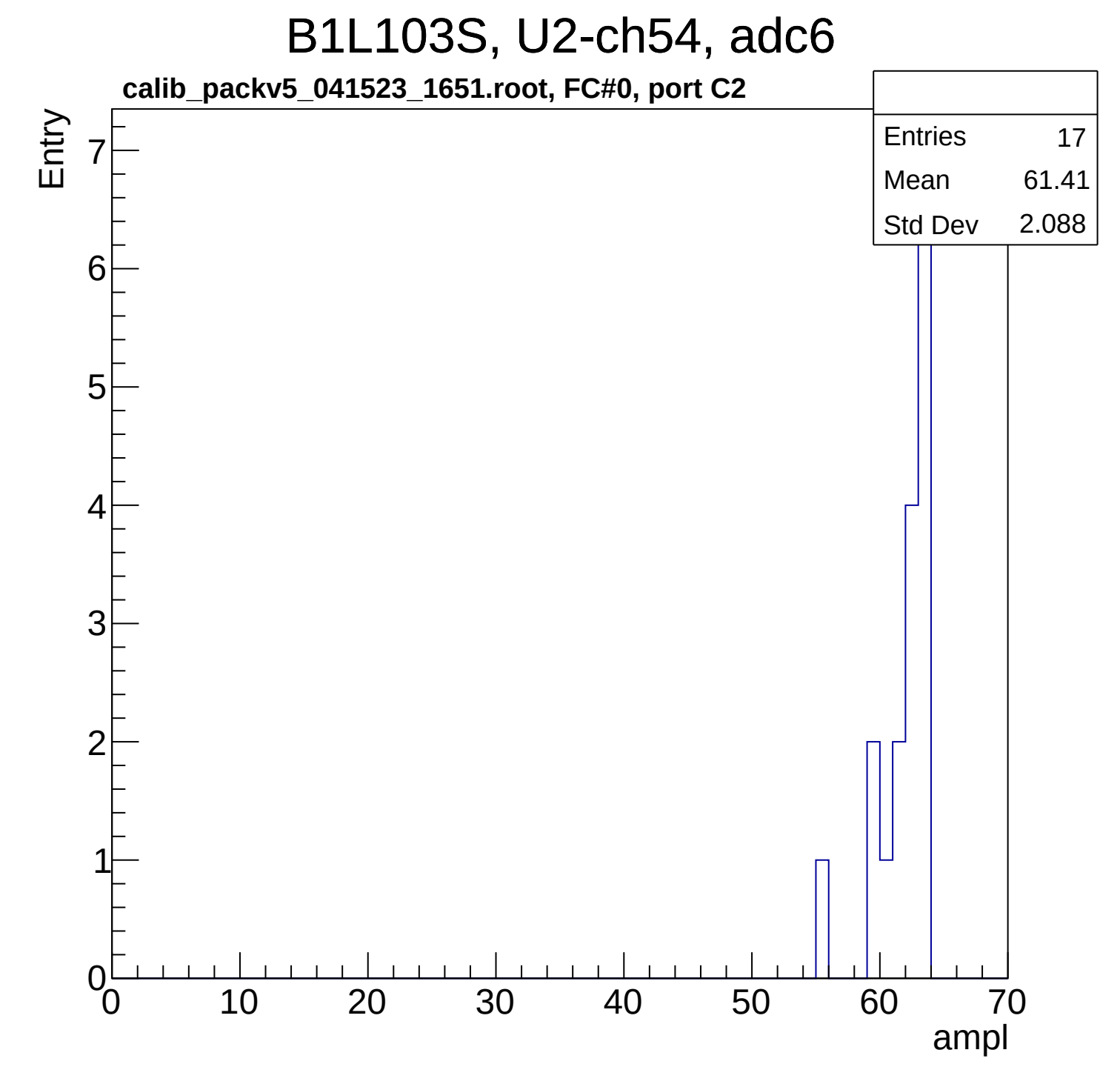

B1L103S, U2-ch54, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 34.36
Std Dev 5.616
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

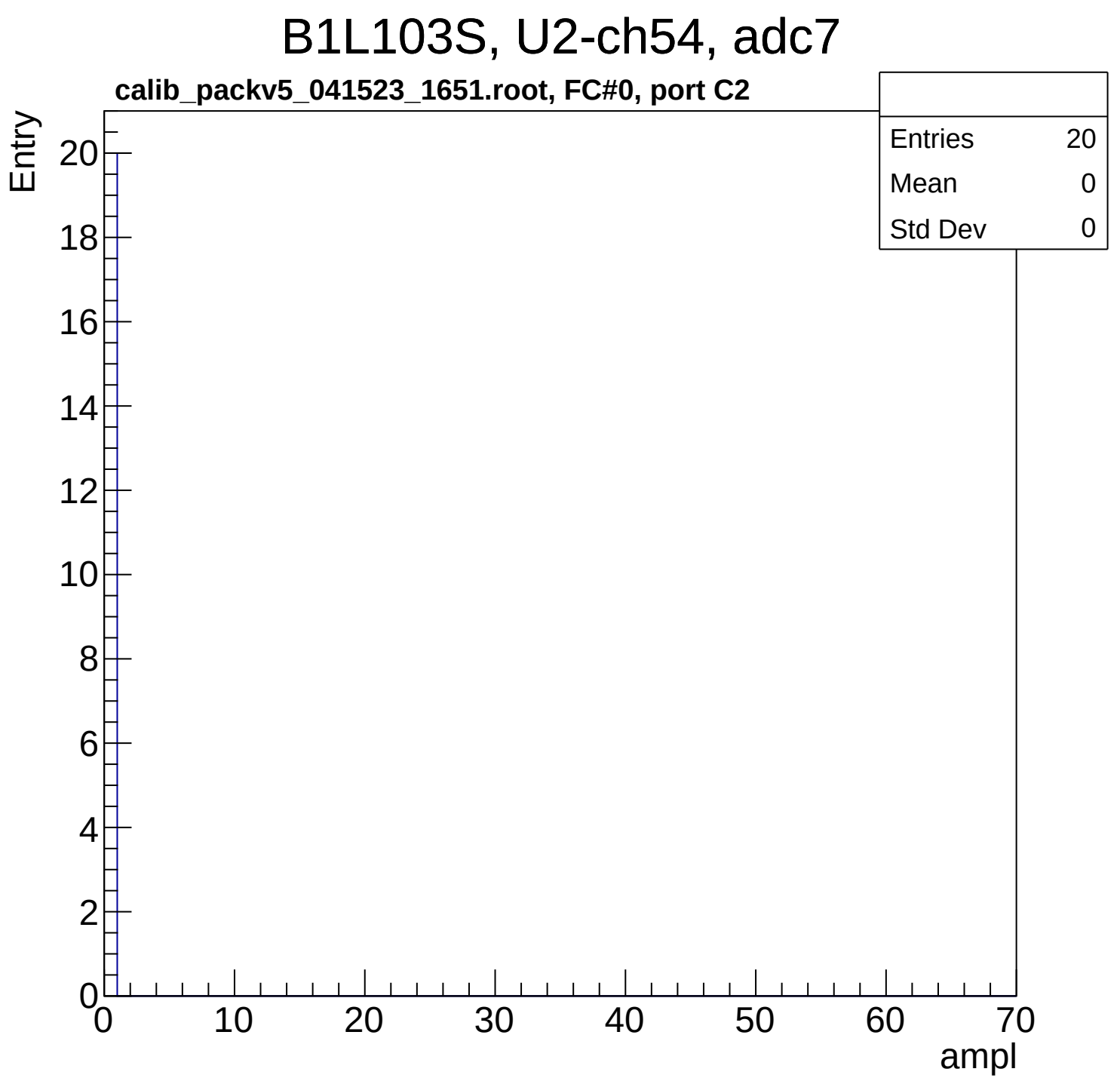

B1L103S, U2-ch54, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 35.77
Std Dev 14.09
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

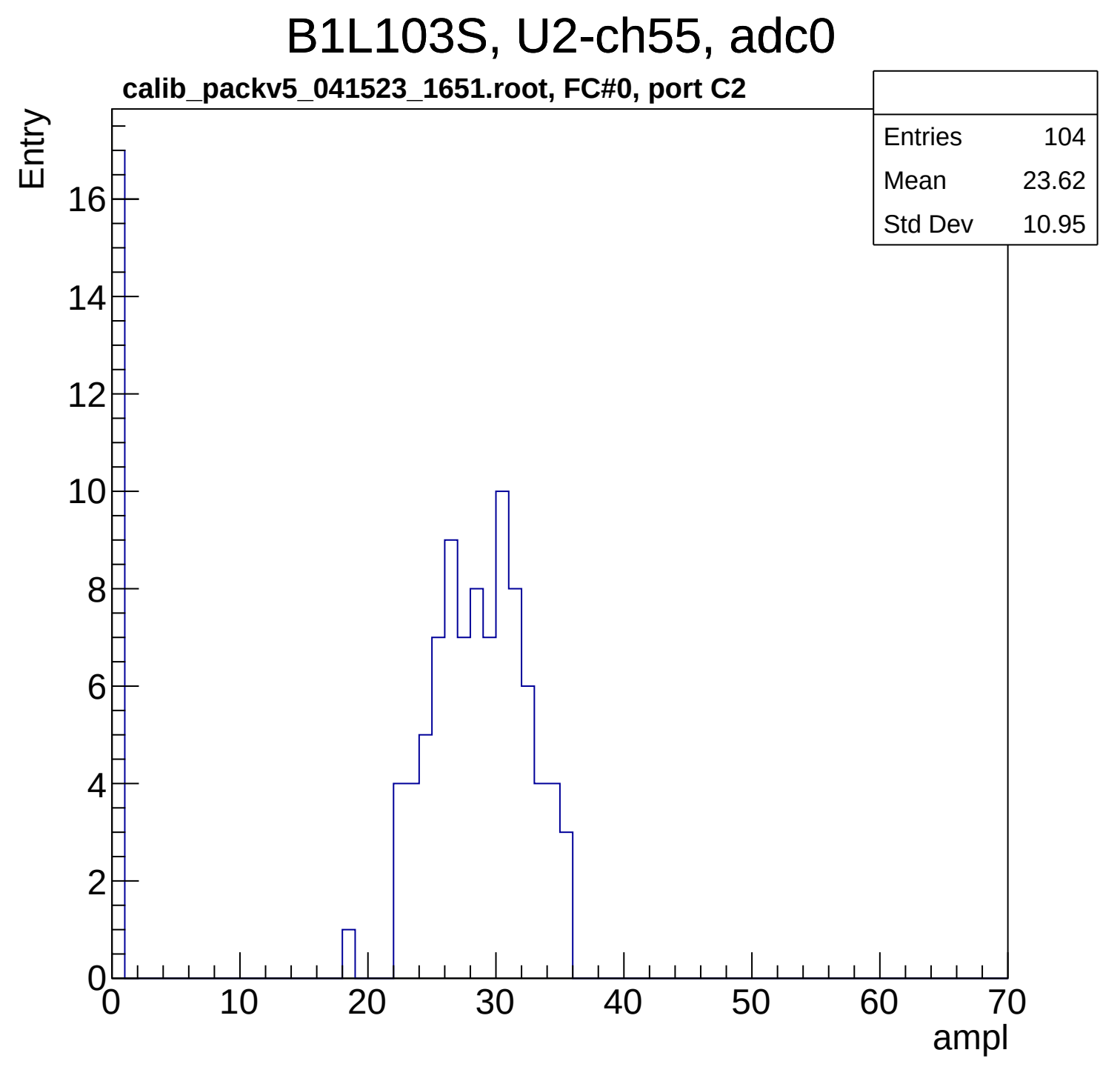

B1L103S, U2-ch54, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 45.43
Std Dev 11.3
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

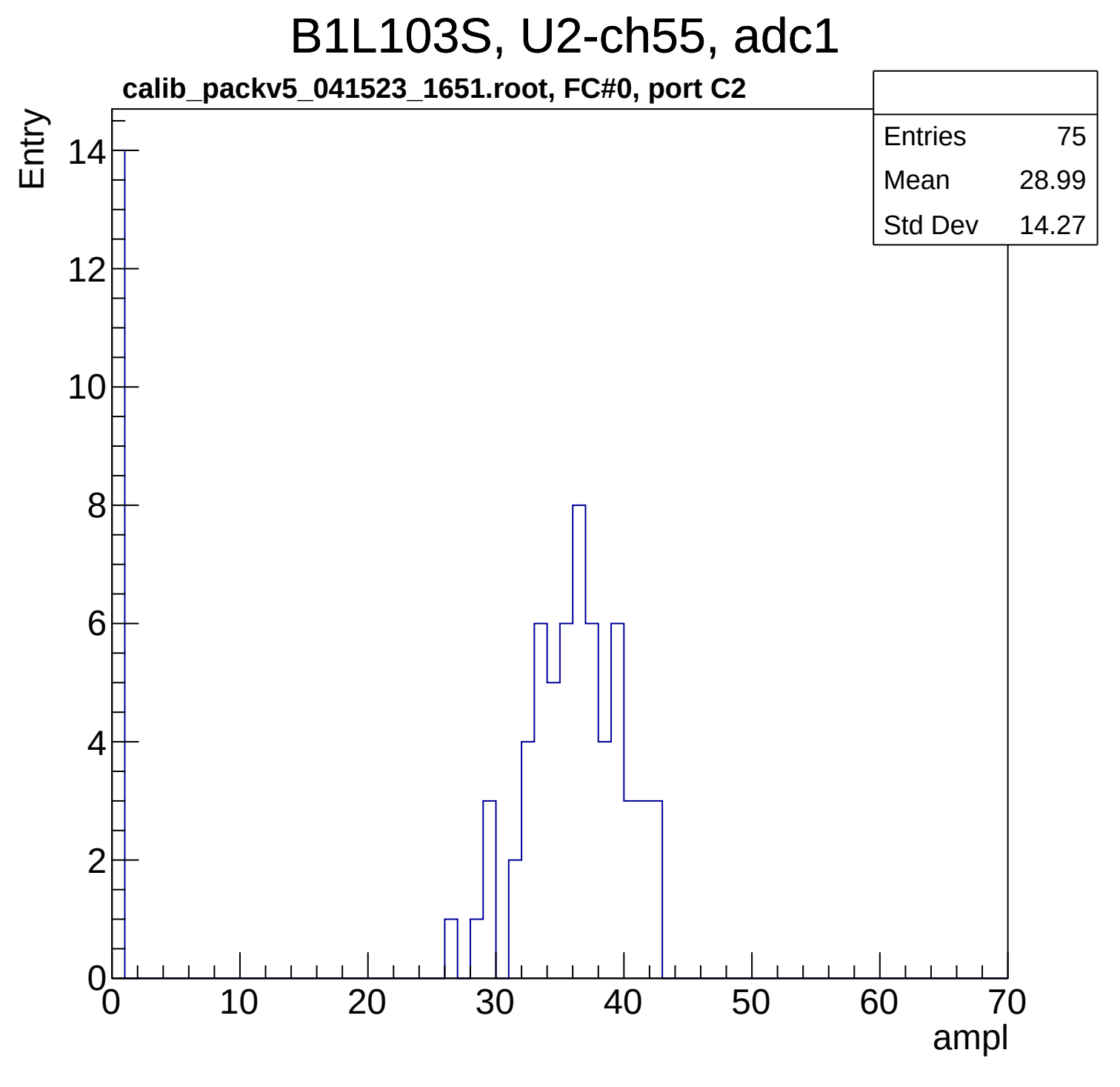

B1L103S, U2-ch54, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 53.89
Std Dev 3.609
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

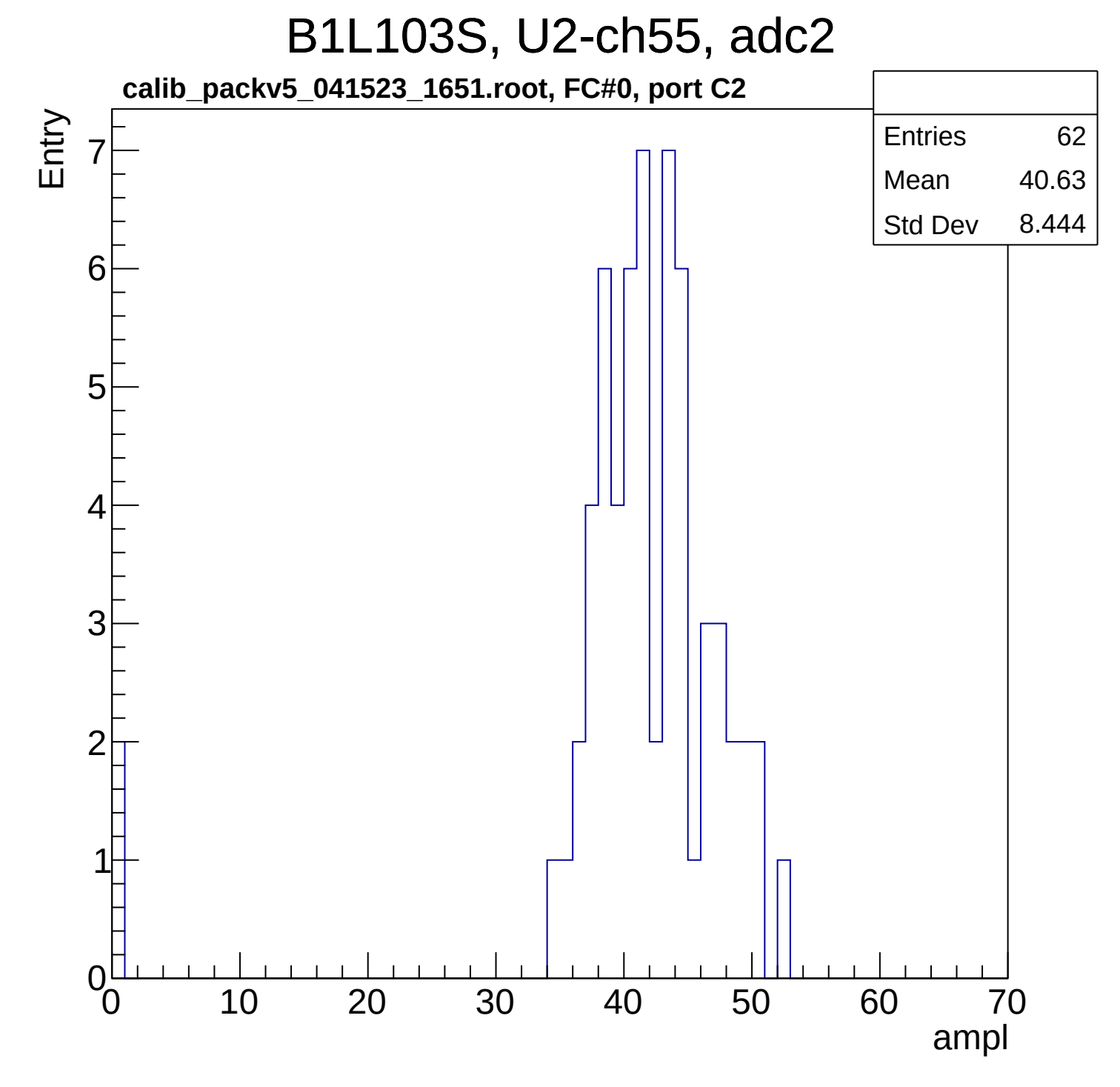

B1L103S, U2-ch54, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.74
Std Dev 2.763
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

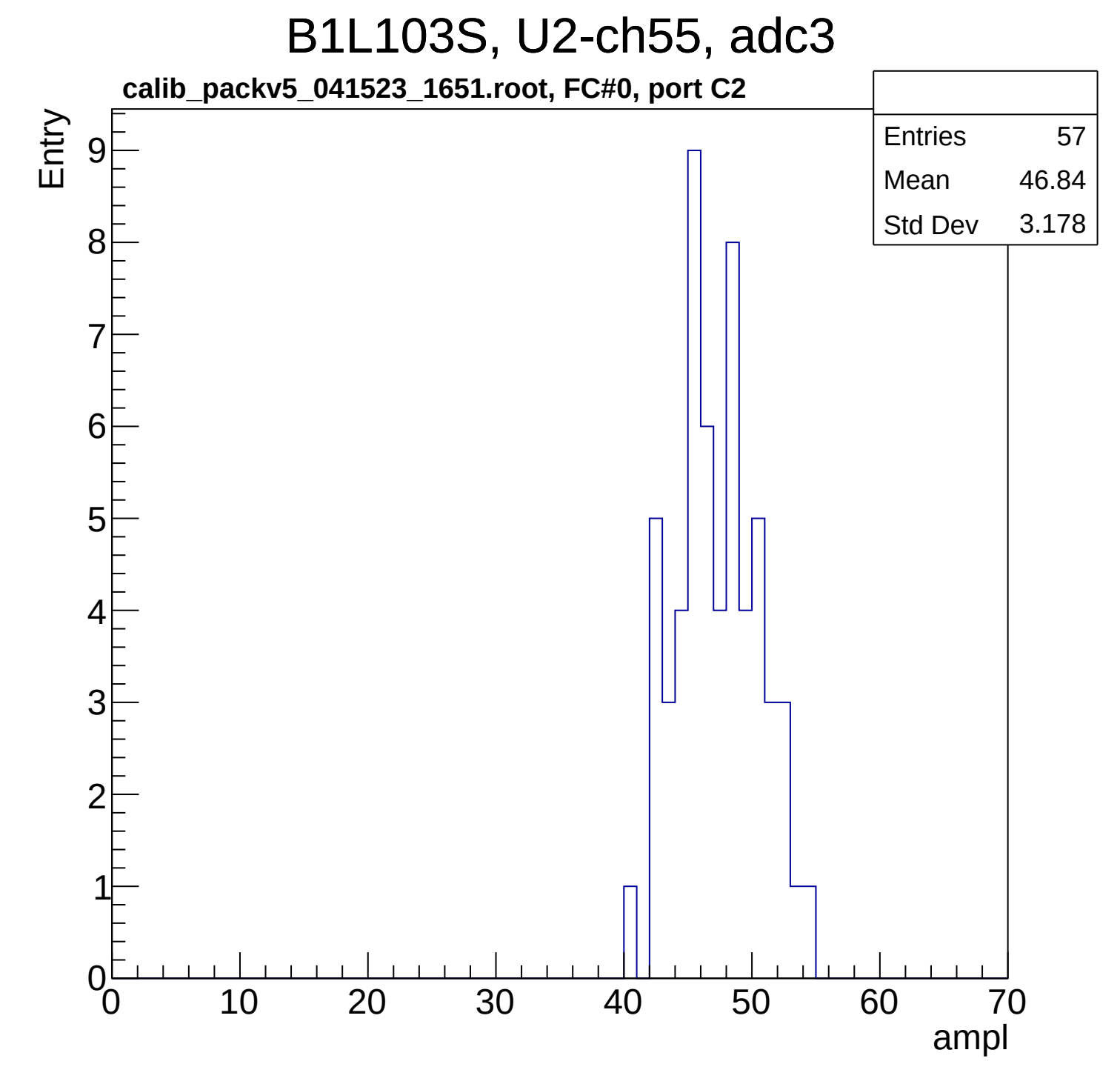

B1L103S, U2-ch54, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.41
Std Dev 2.088
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

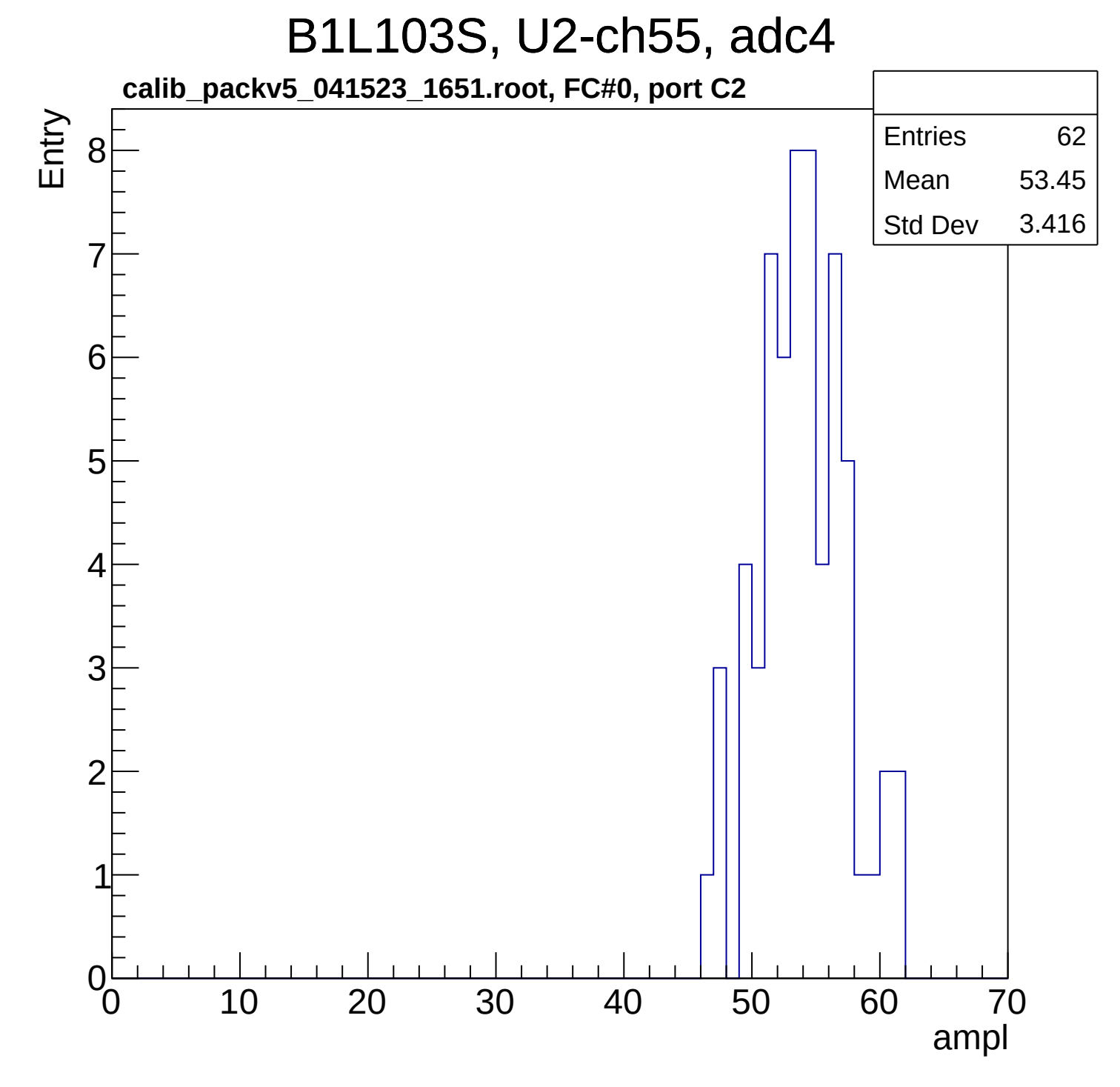

B1L103S, U2-ch54, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl

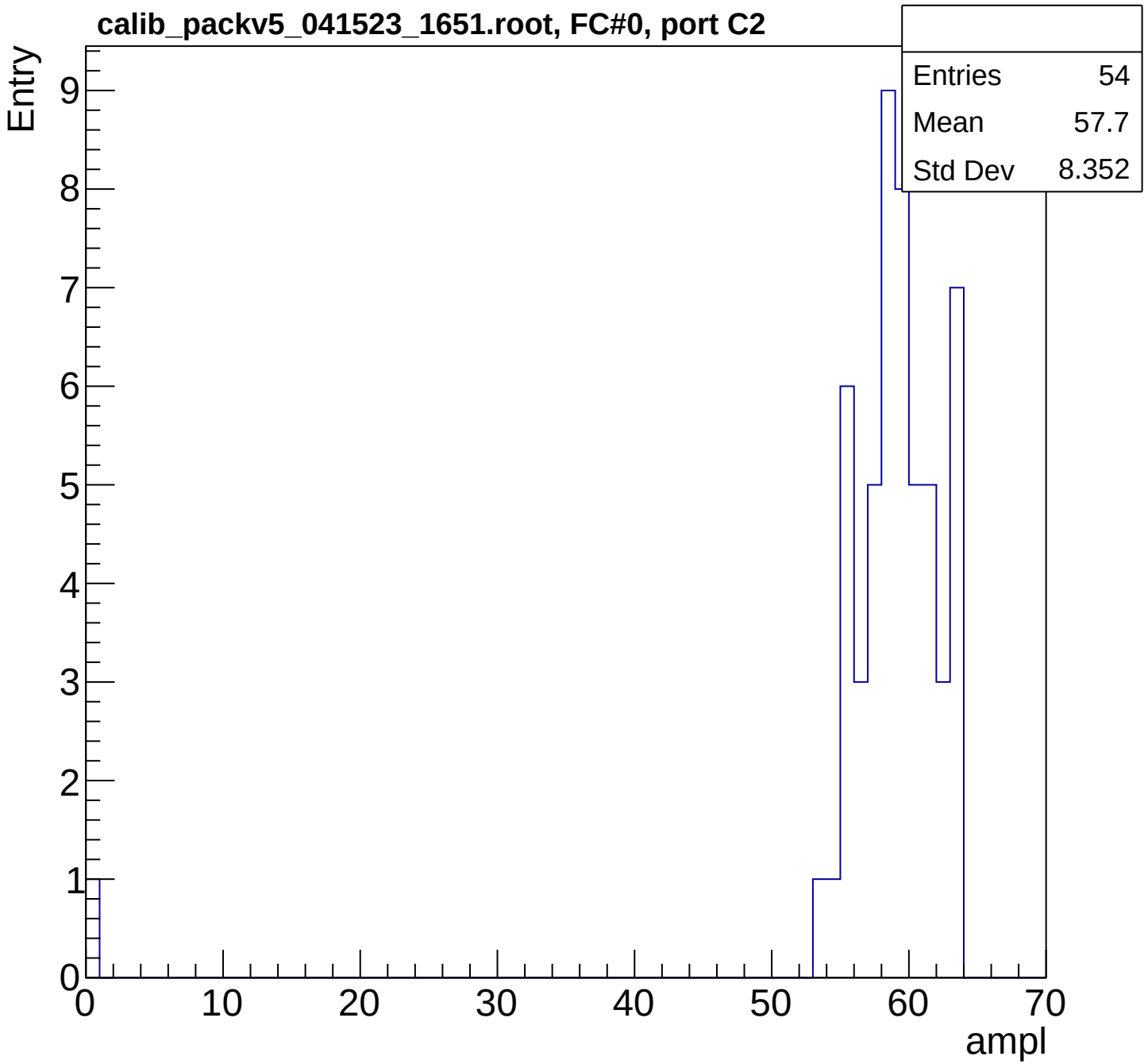

B1L103S, U2-ch55, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 23.62
Std Dev 10.95
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

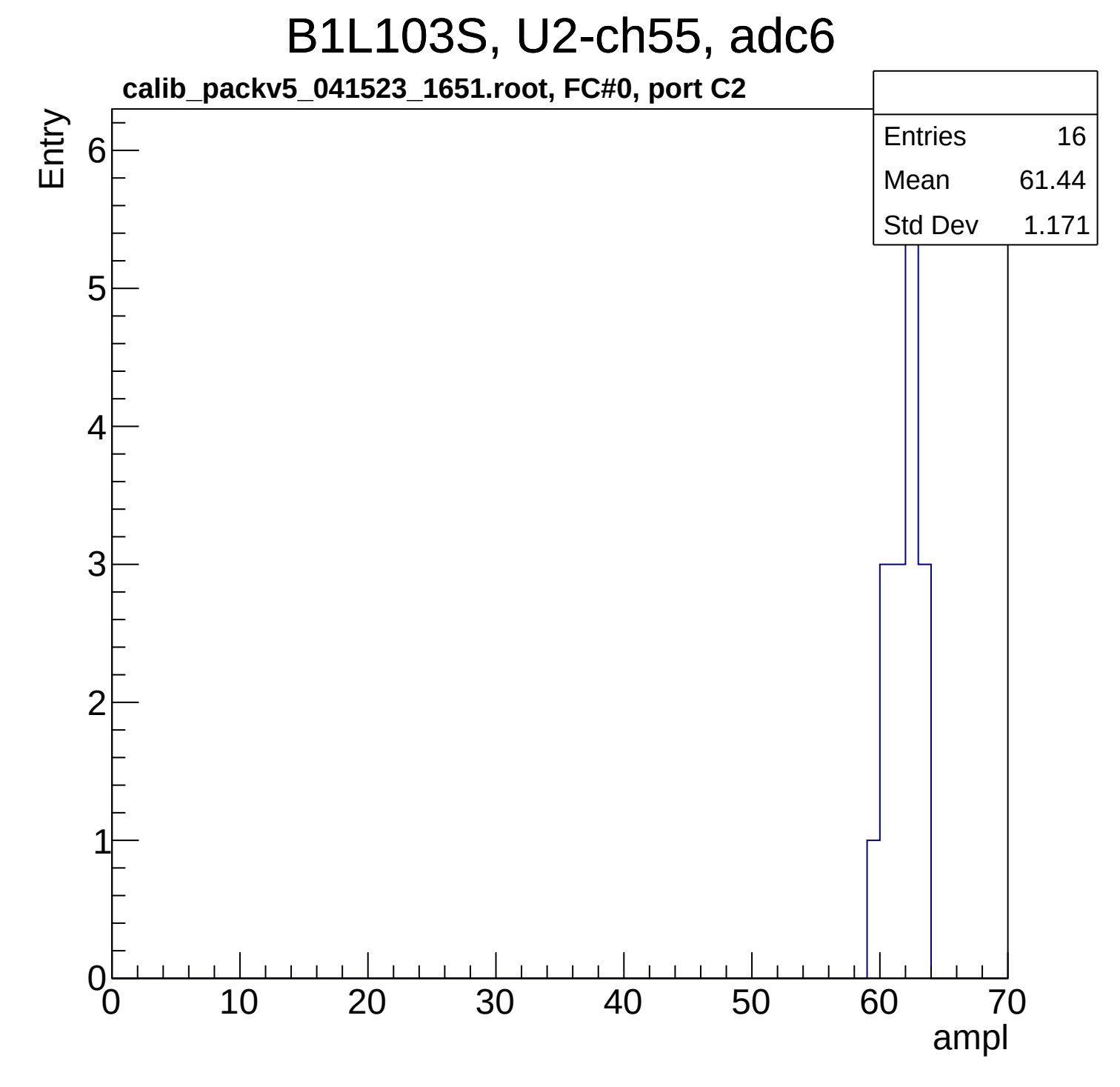

B1L103S, U2-ch55, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 28.99
Std Dev 14.27
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

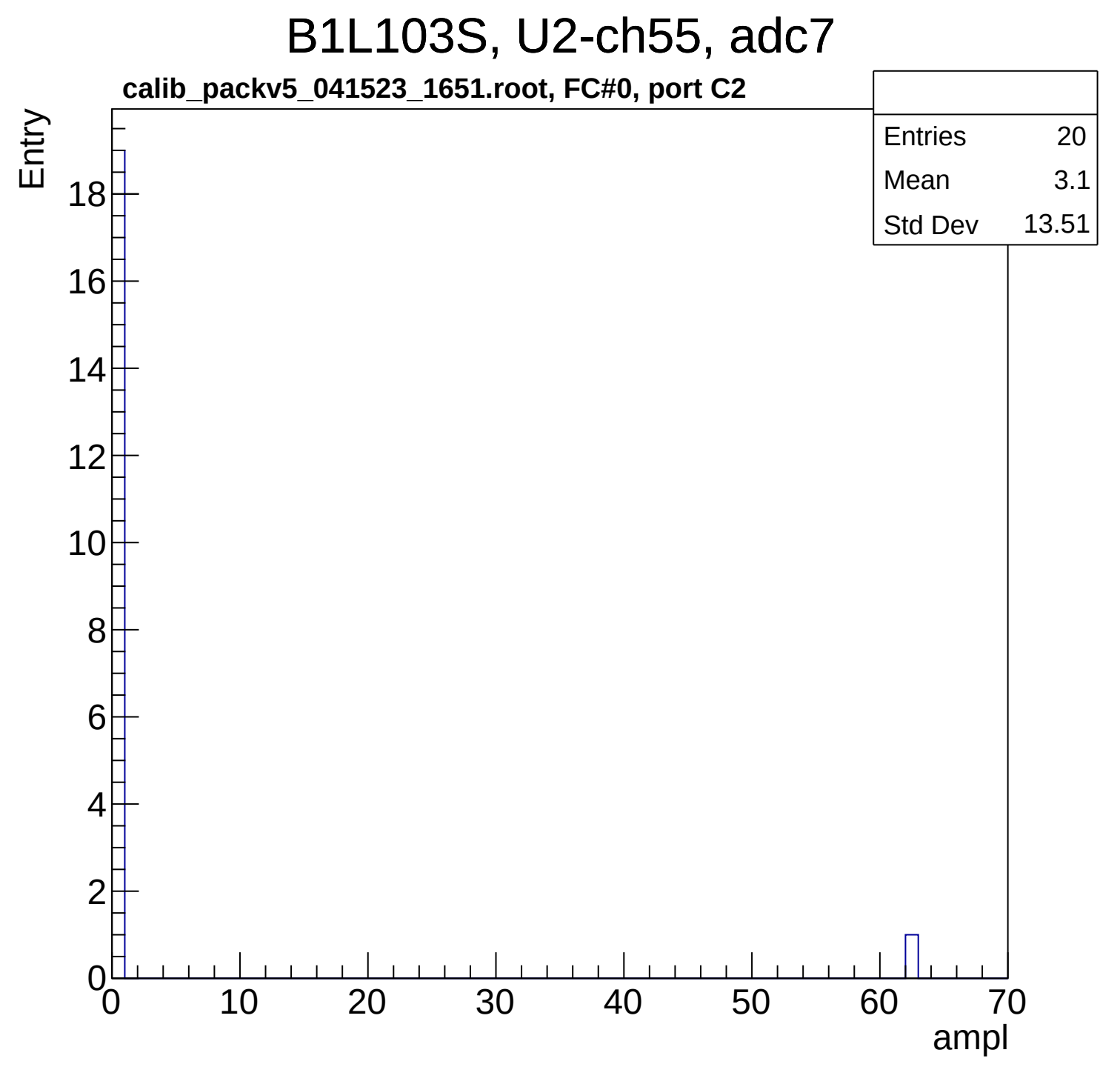

B1L103S, U2-ch55, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 40.63
Std Dev 8.444
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

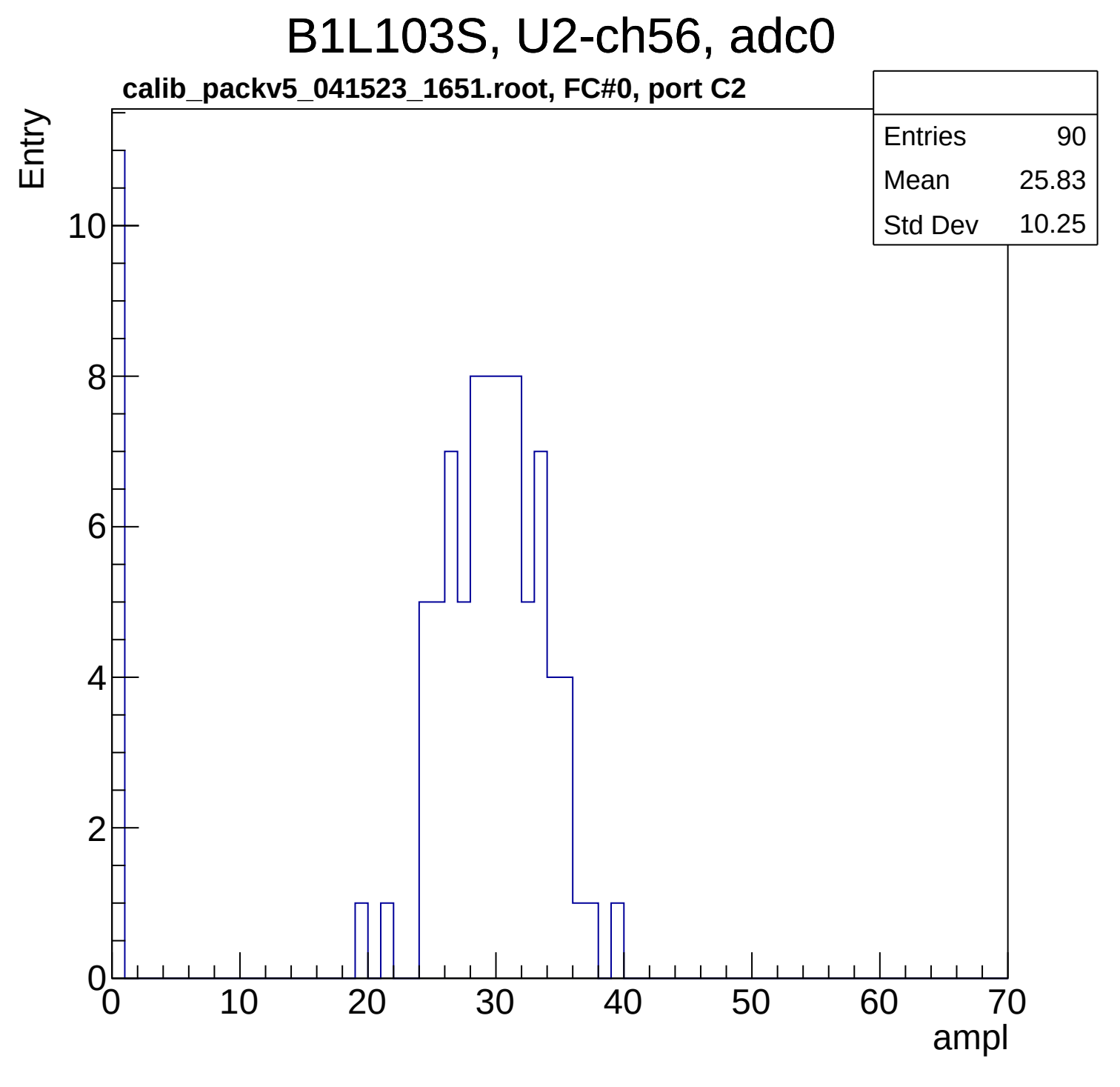

B1L103S, U2-ch55, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 46.84
Std Dev 3.178
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

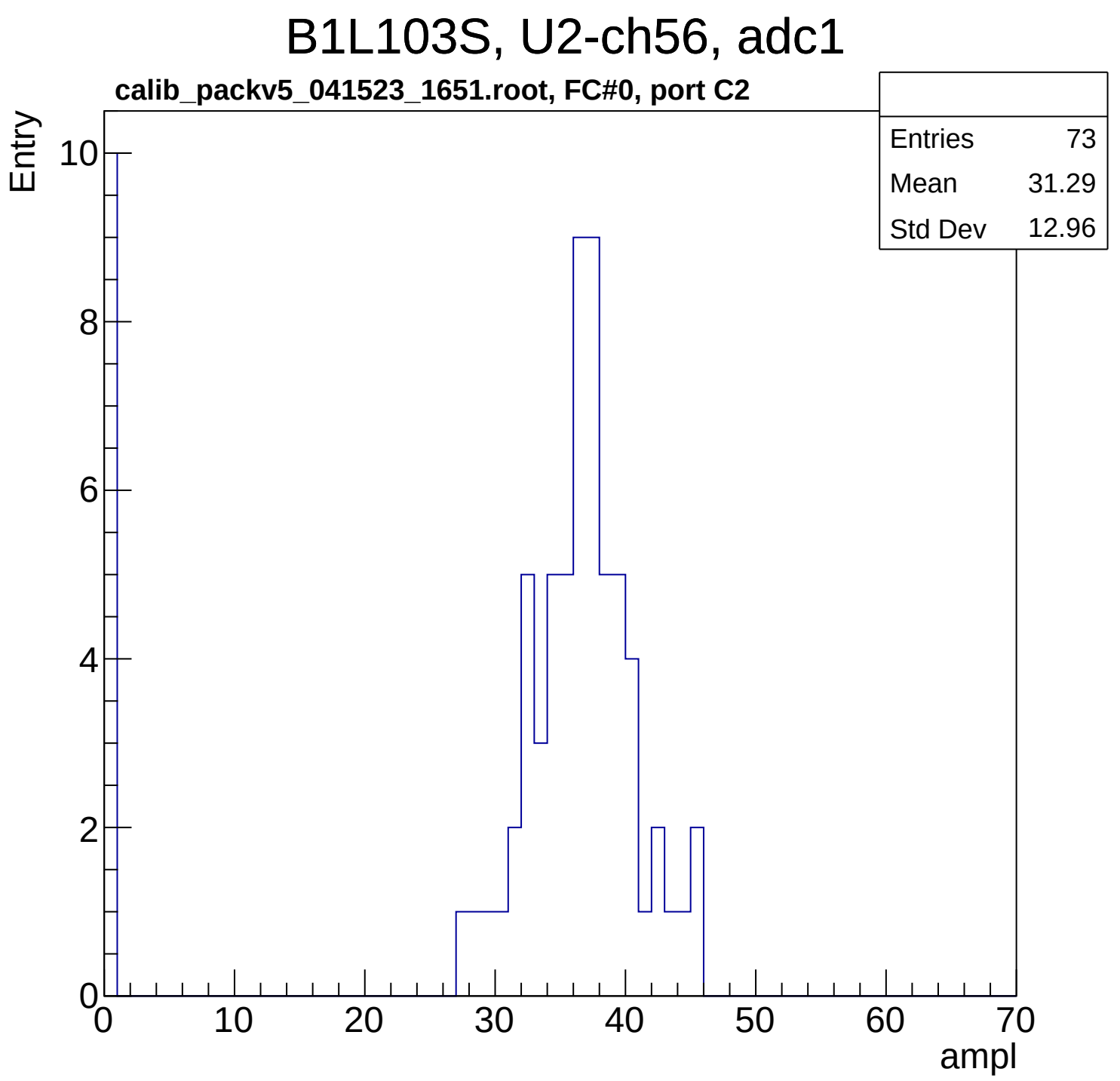

B1L103S, U2-ch55, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 53.45
Std Dev 3.416
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

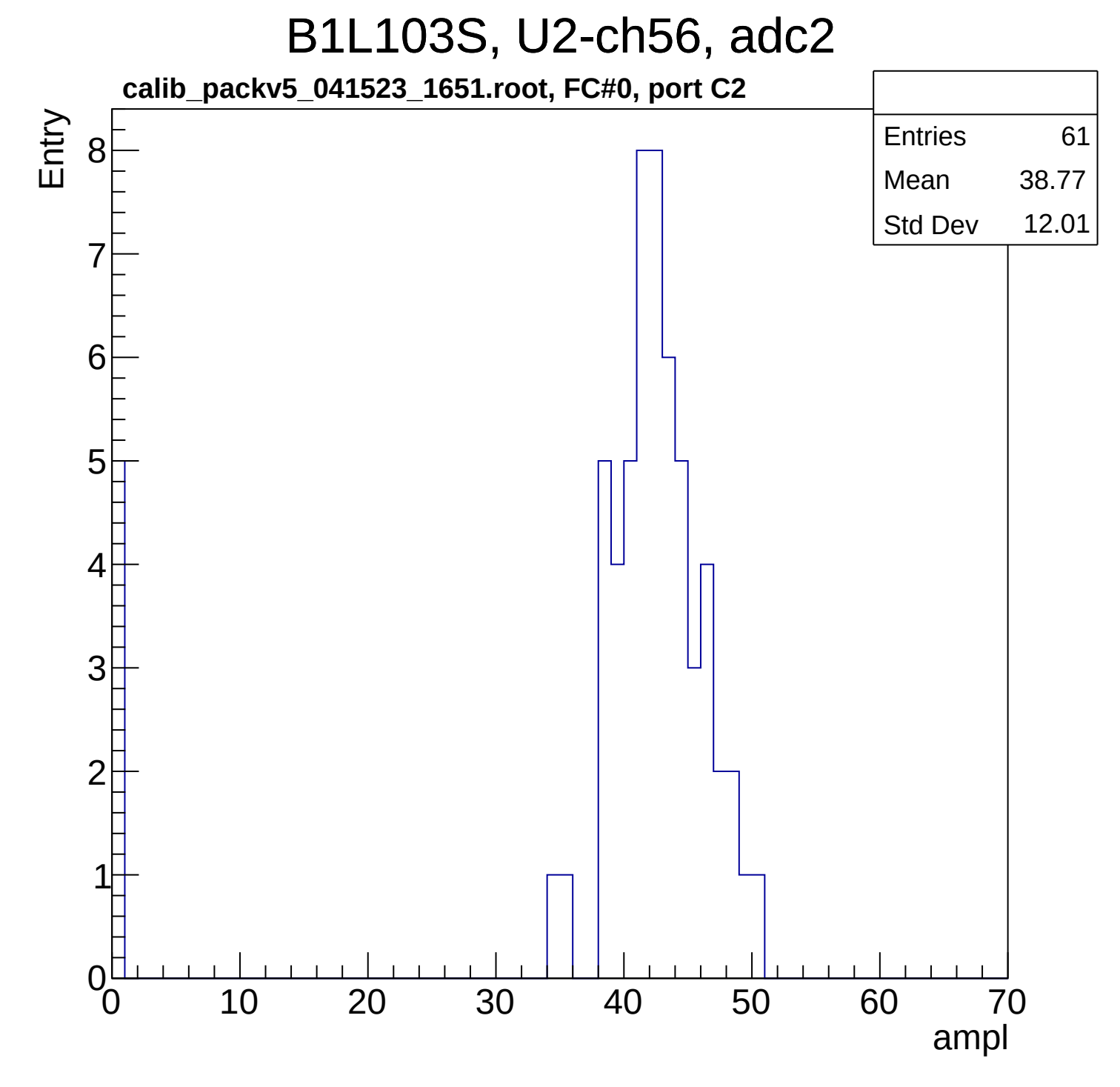

B1L103S, U2-ch55, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.7
Std Dev 8.352
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

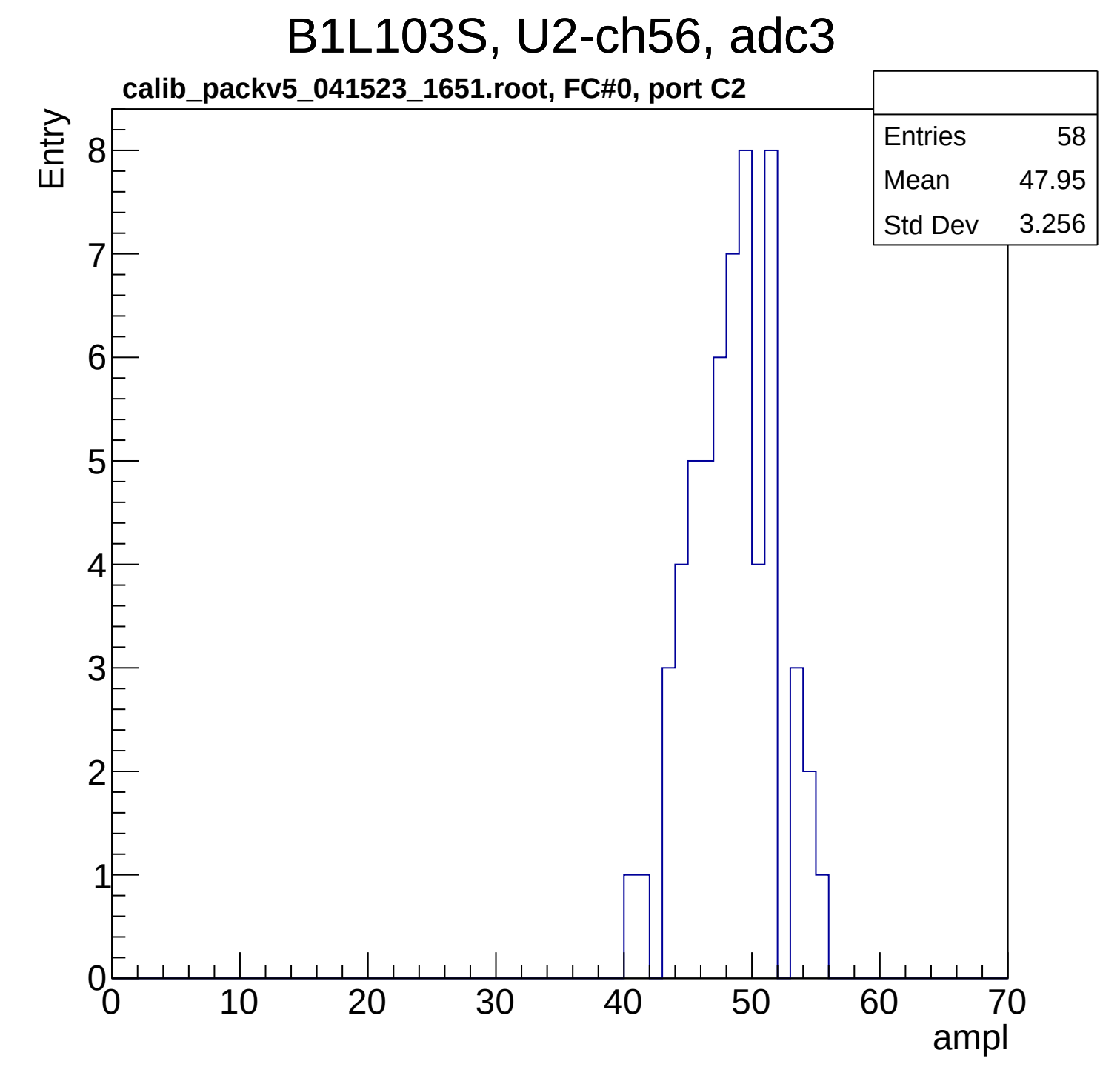

B1L103S, U2-ch55, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 61.44
Std Dev 1.171
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

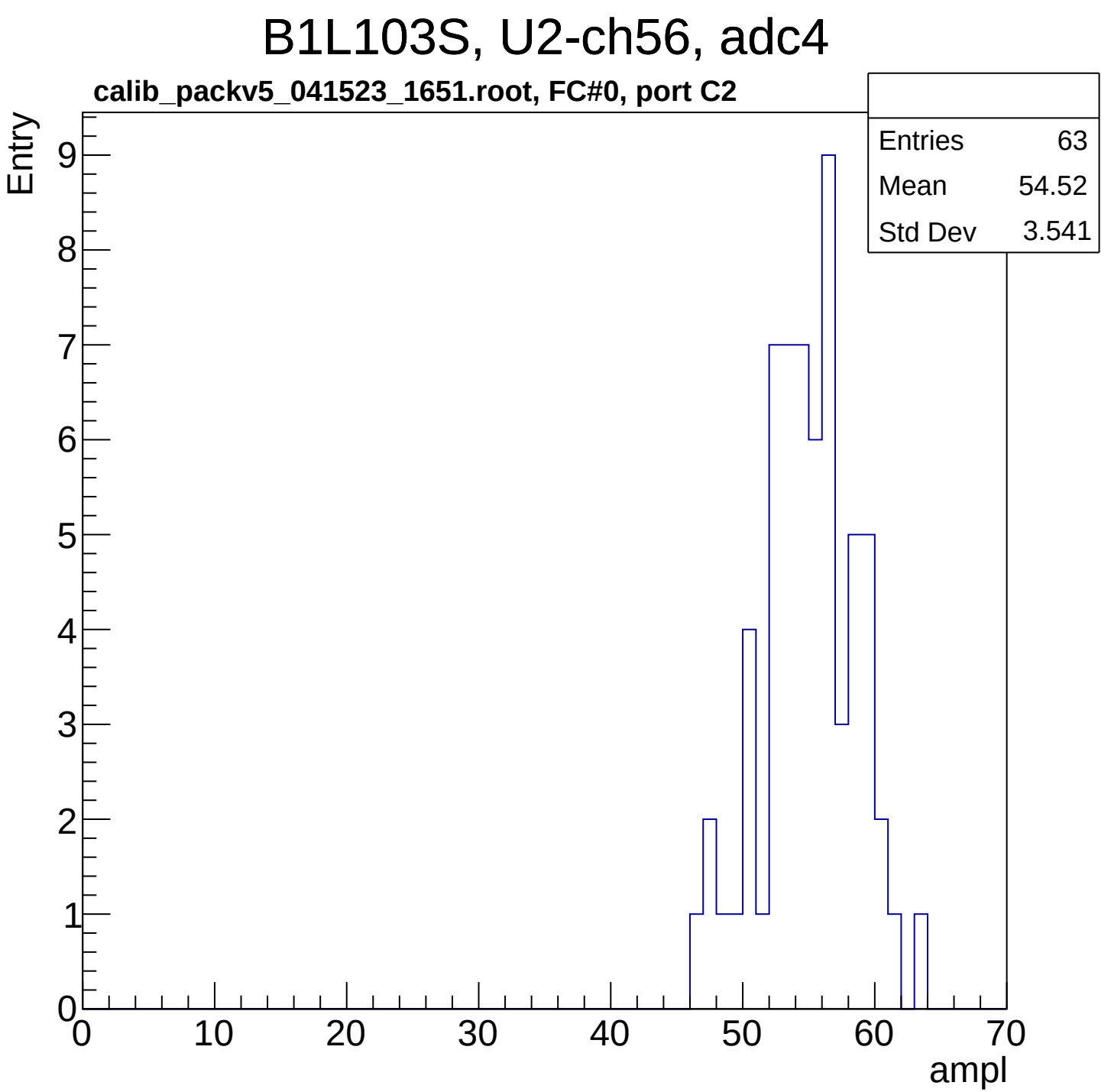

B1L103S, U2-ch55, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

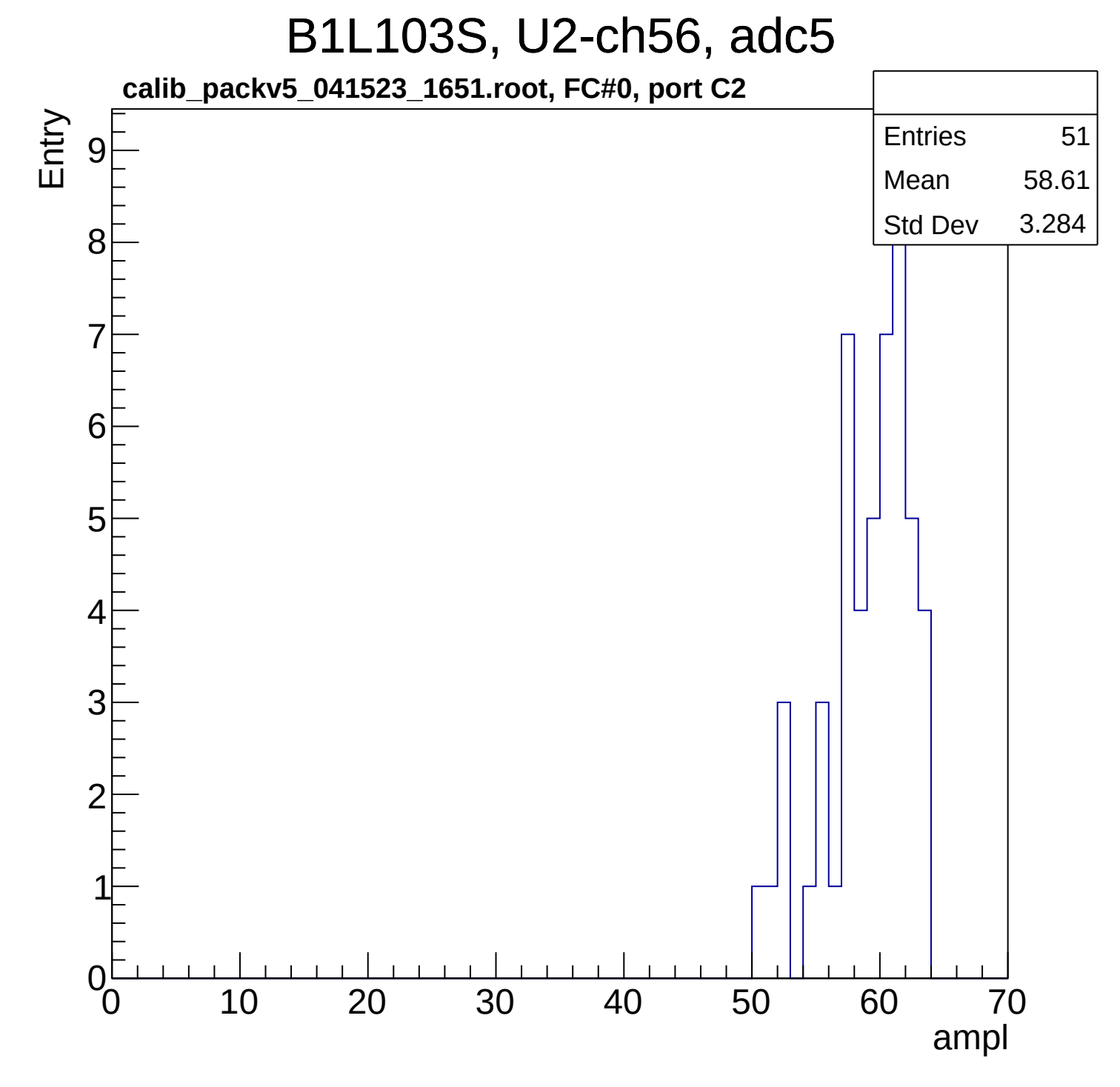

B1L103S, U2-ch56, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 25.83
Std Dev 10.25
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

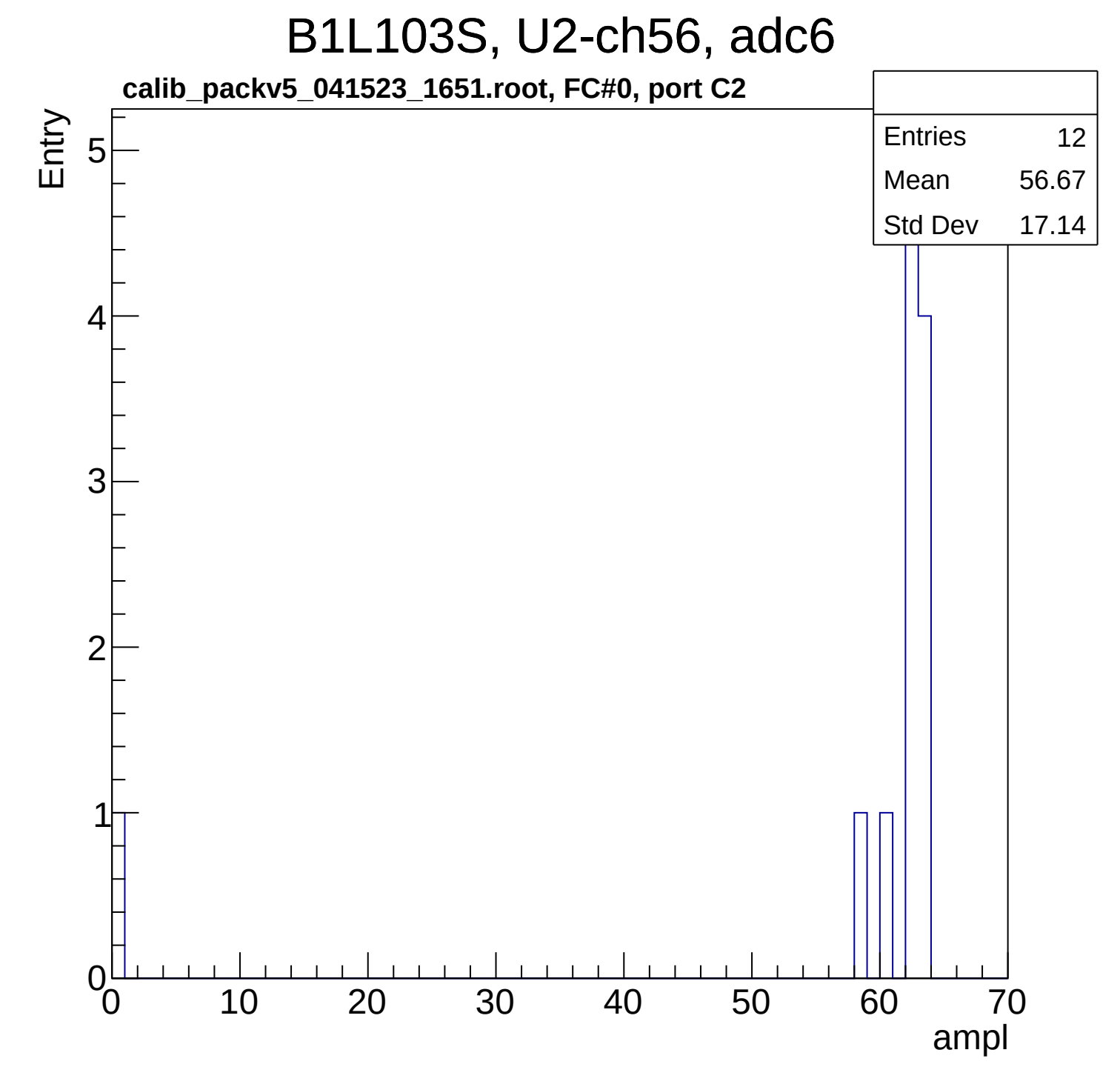

B1L103S, U2-ch56, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 31.29
Std Dev 12.96
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

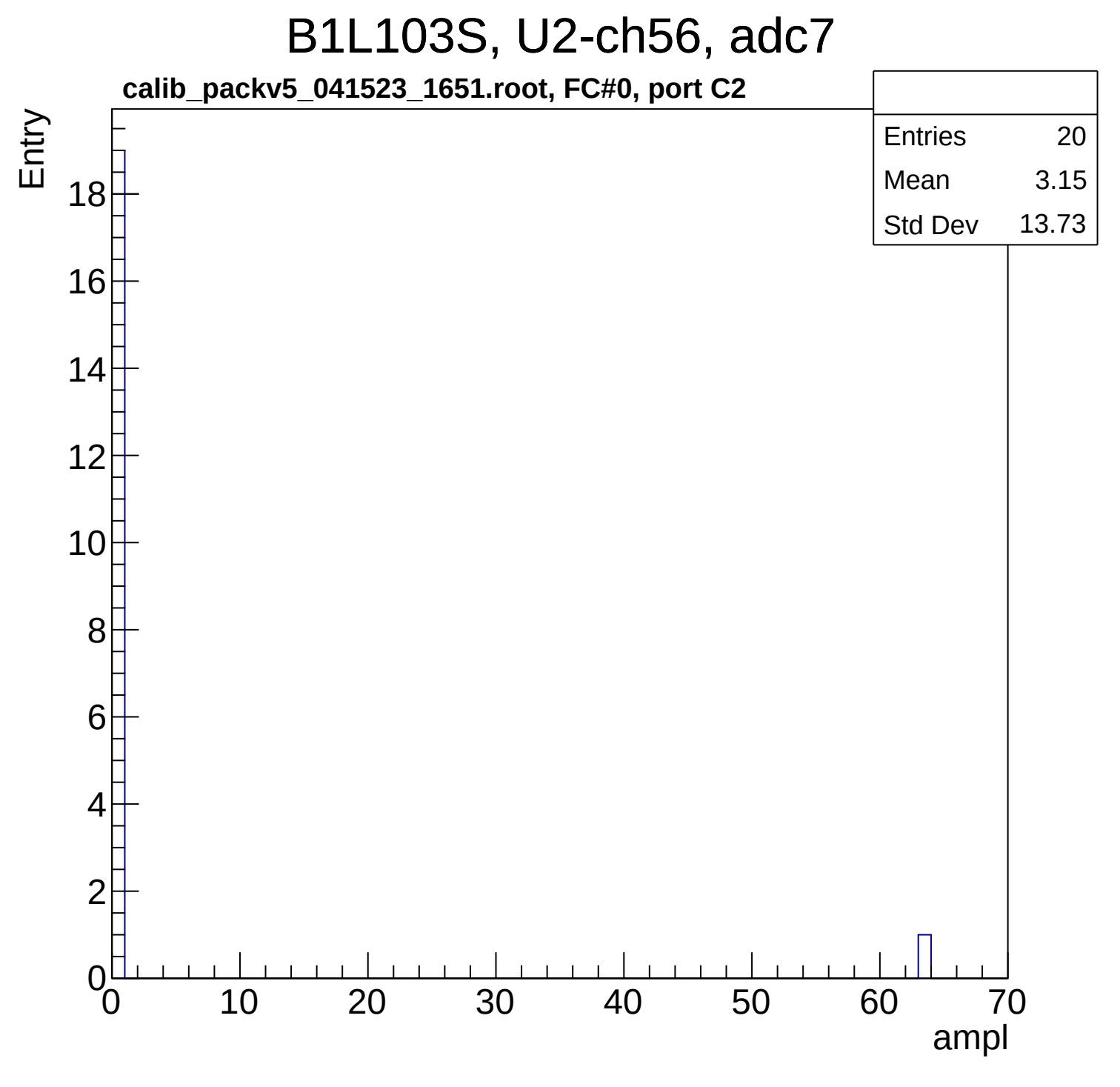

B1L103S, U2-ch56, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 38.77
Std Dev 12.01
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

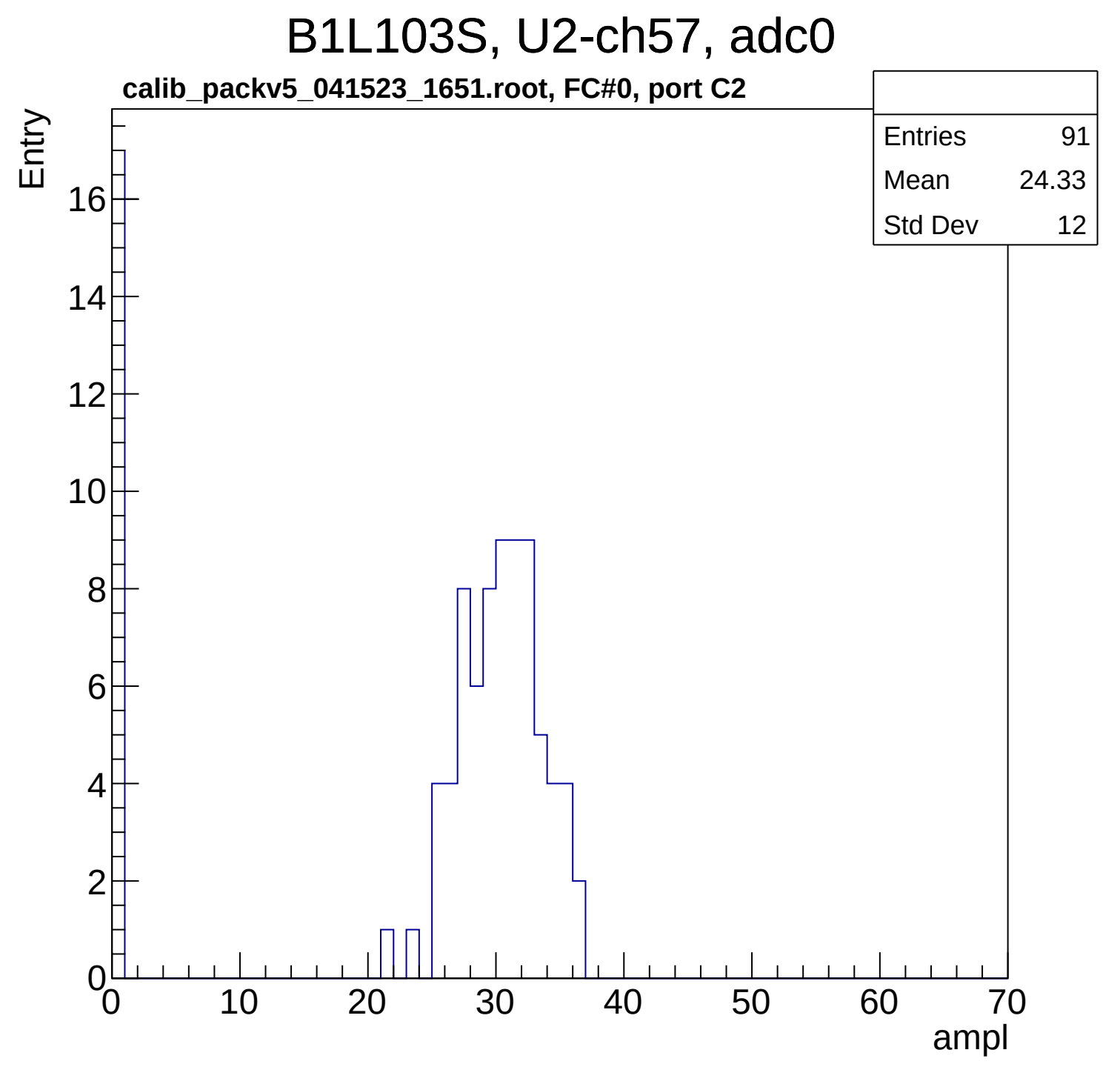

B1L103S, U2-ch56, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 47.95
Std Dev 3.256
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

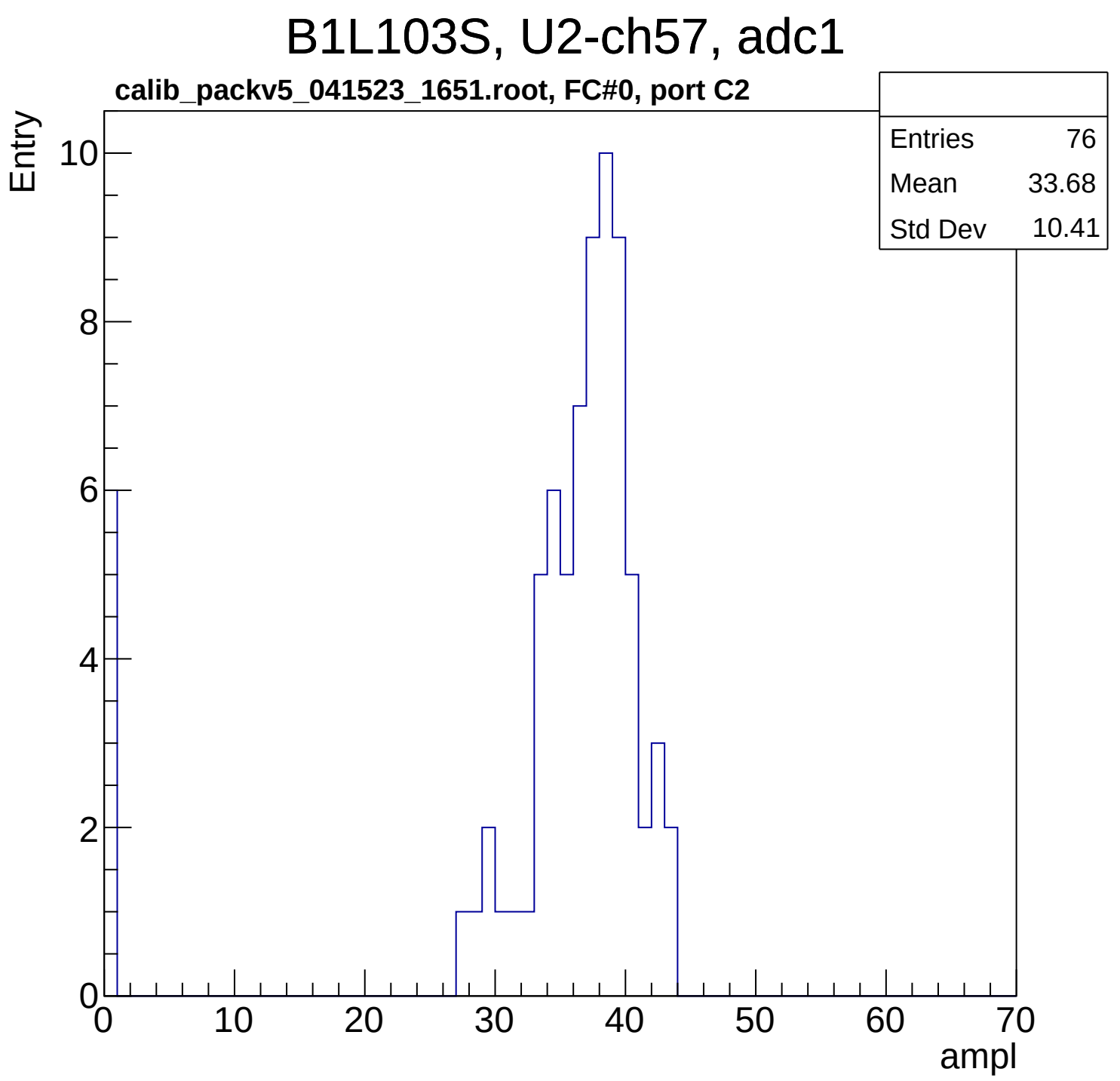

B1L103S, U2-ch56, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 54.52
Std Dev 3.541
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

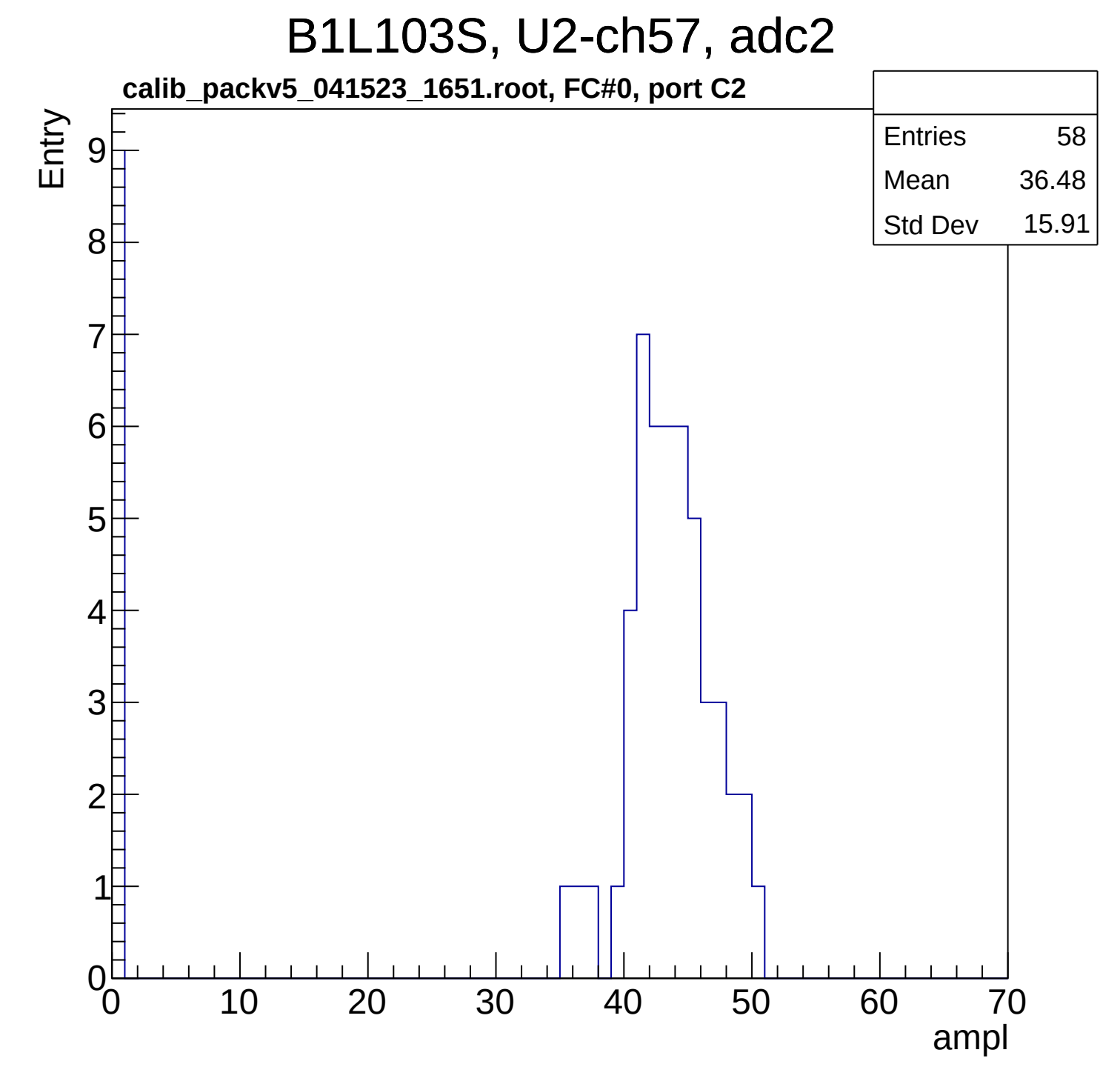

B1L103S, U2-ch56, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.61
Std Dev 3.284
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

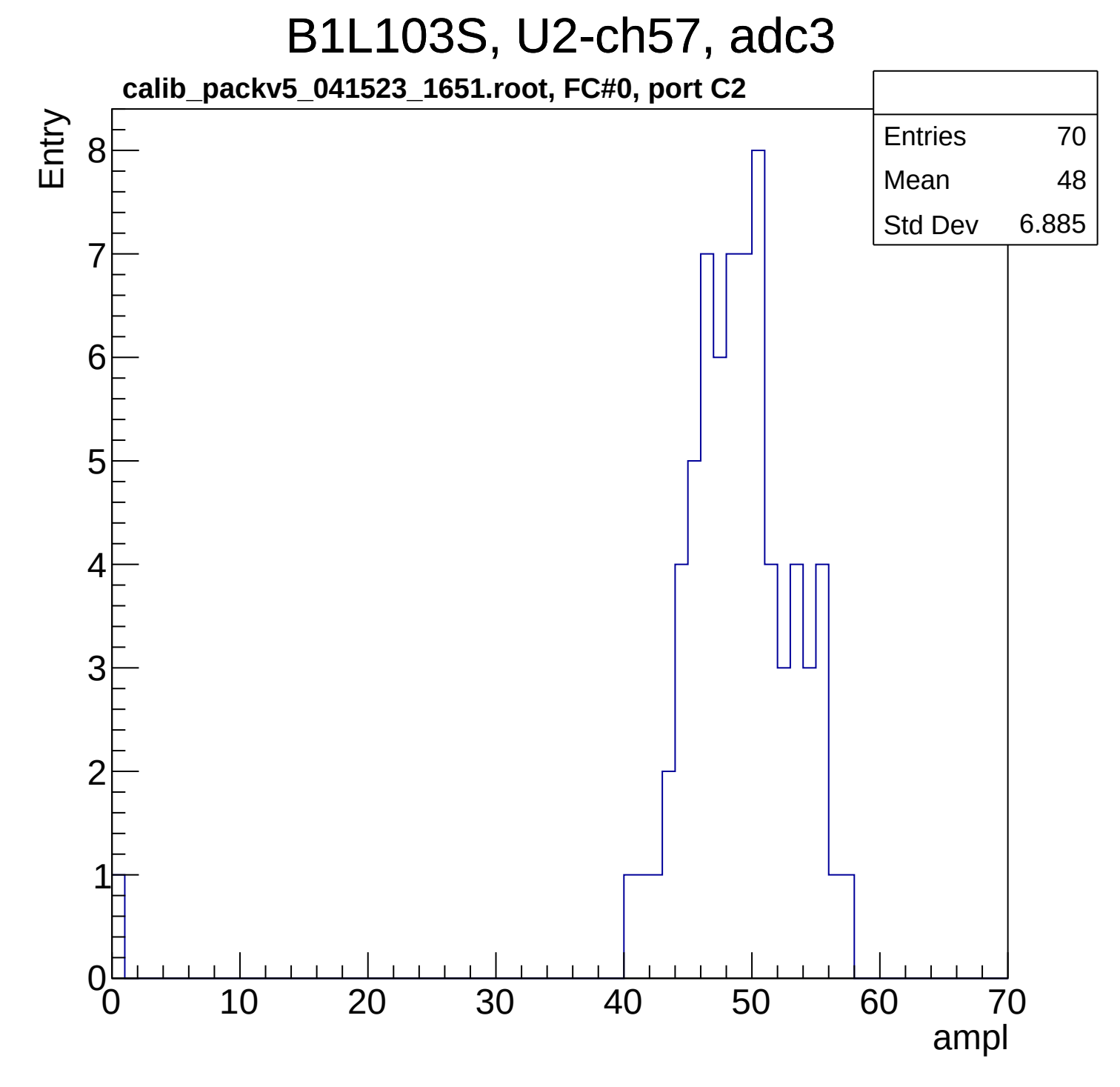

B1L103S, U2-ch56, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.67
Std Dev 17.14
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

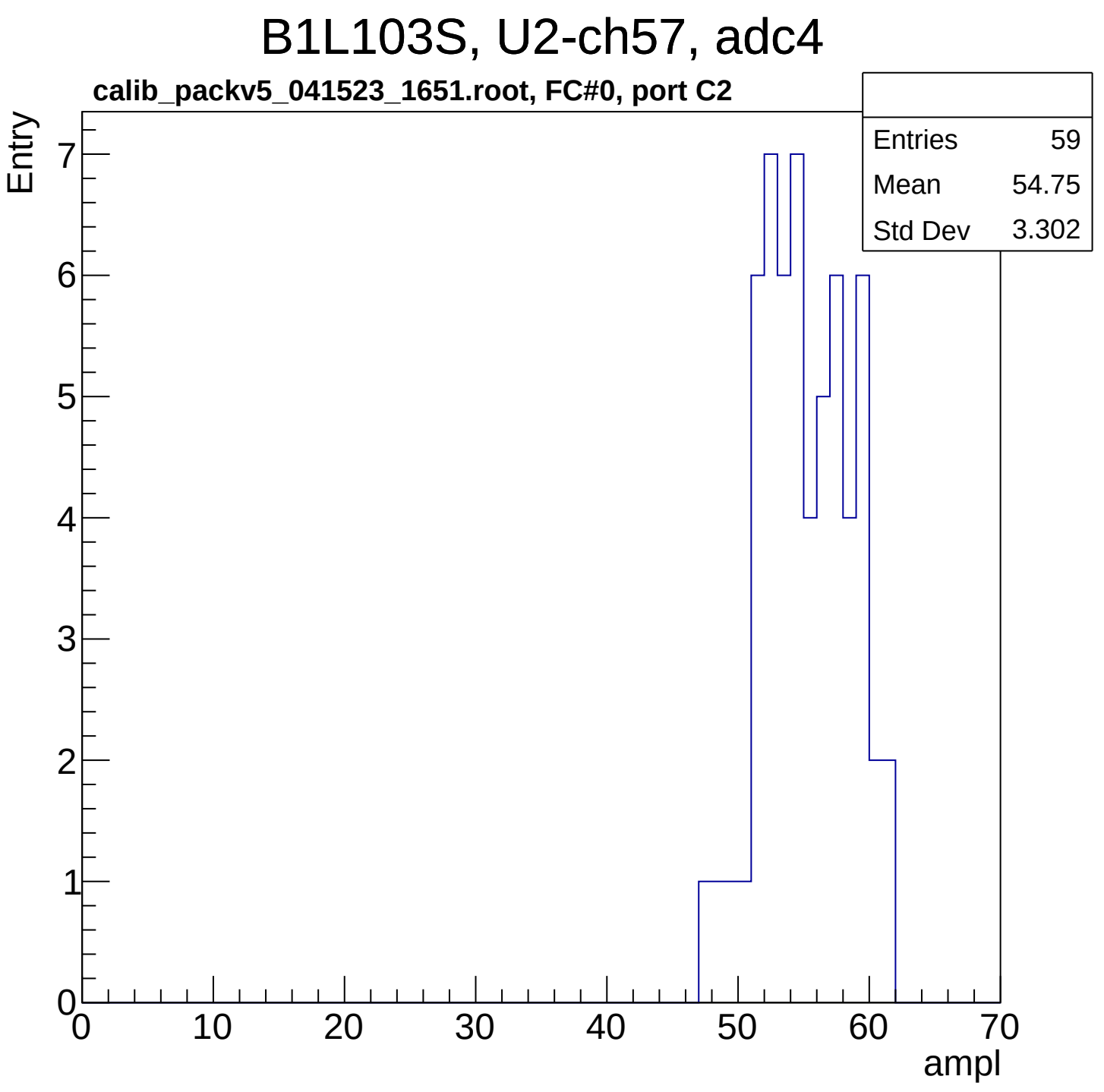

B1L103S, U2-ch56, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

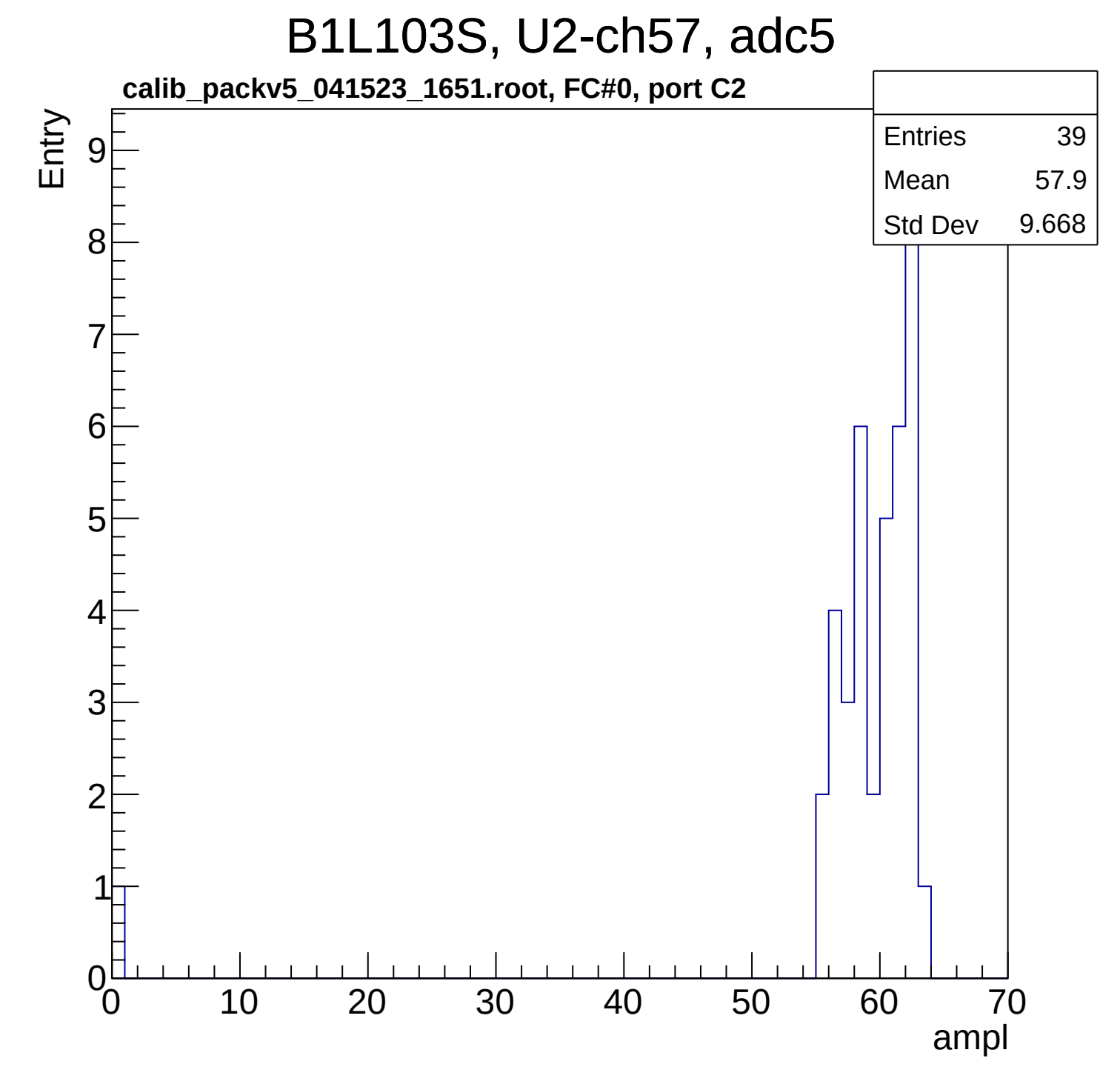

B1L103S, U2-ch57, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 24.33
Std Dev 12
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

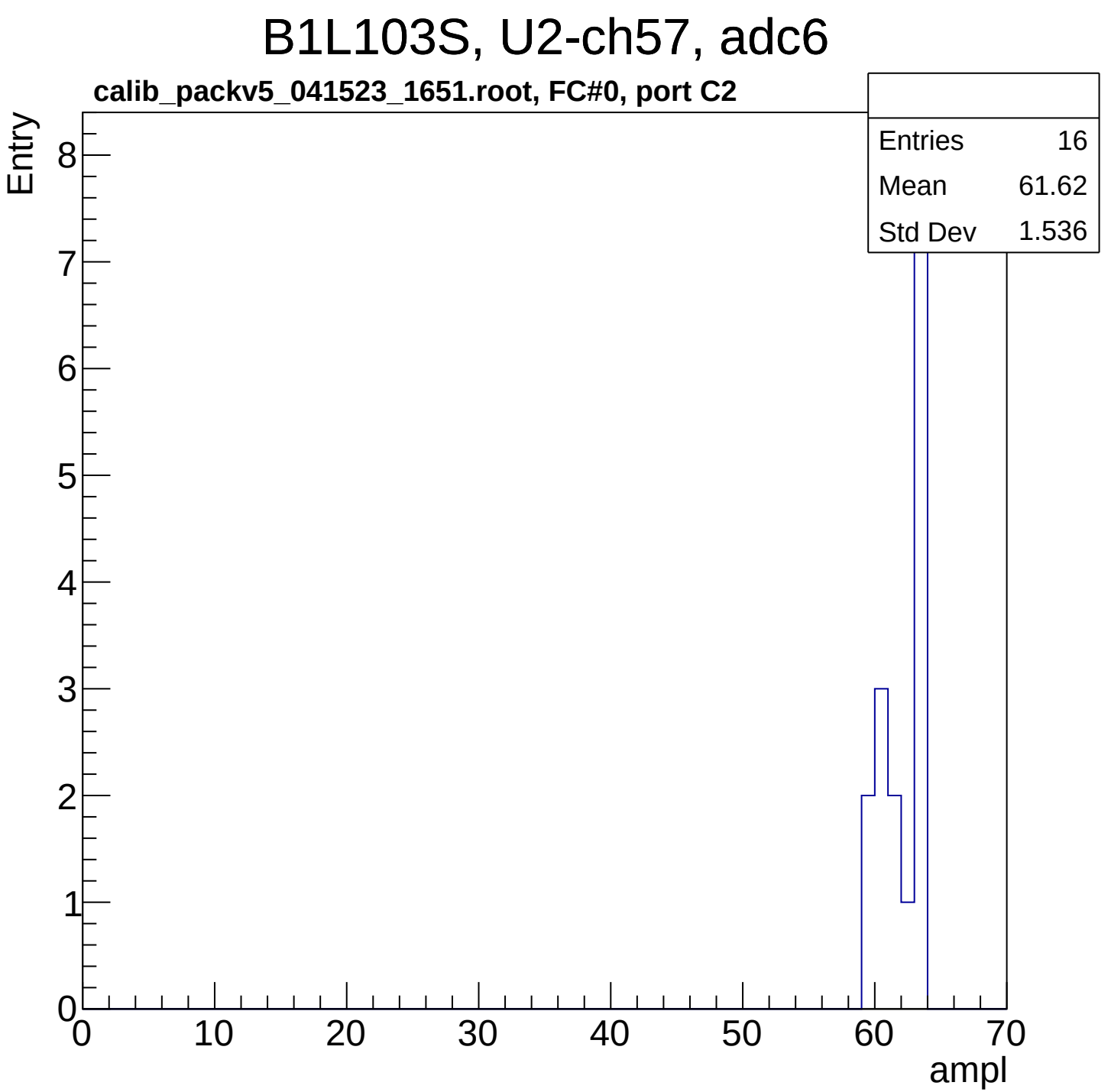

B1L103S, U2-ch57, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 33.68
Std Dev 10.41
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

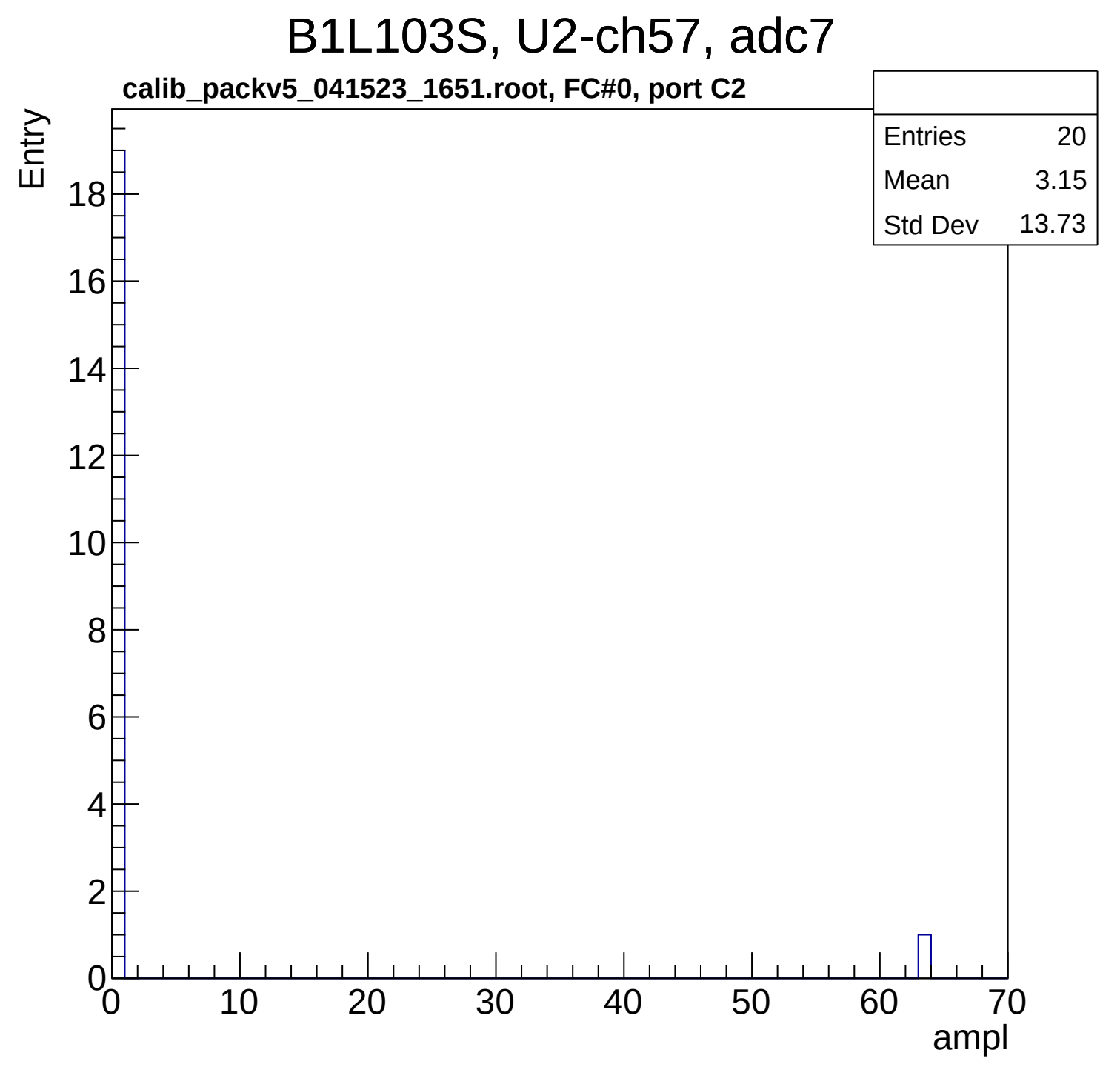

B1L103S, U2-ch57, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 36.48
Std Dev 15.91
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

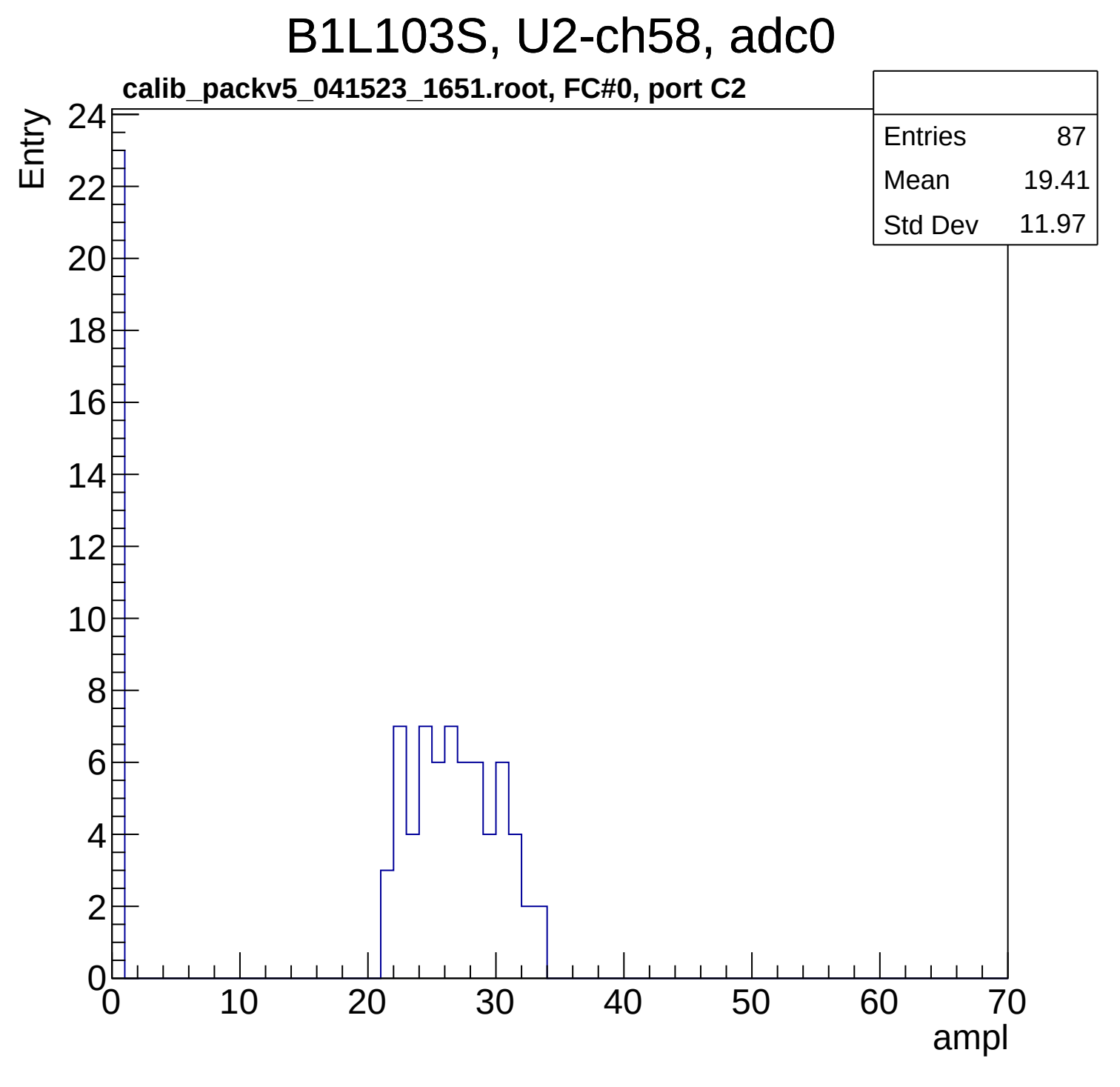

B1L103S, U2-ch57, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 48
Std Dev 6.885
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

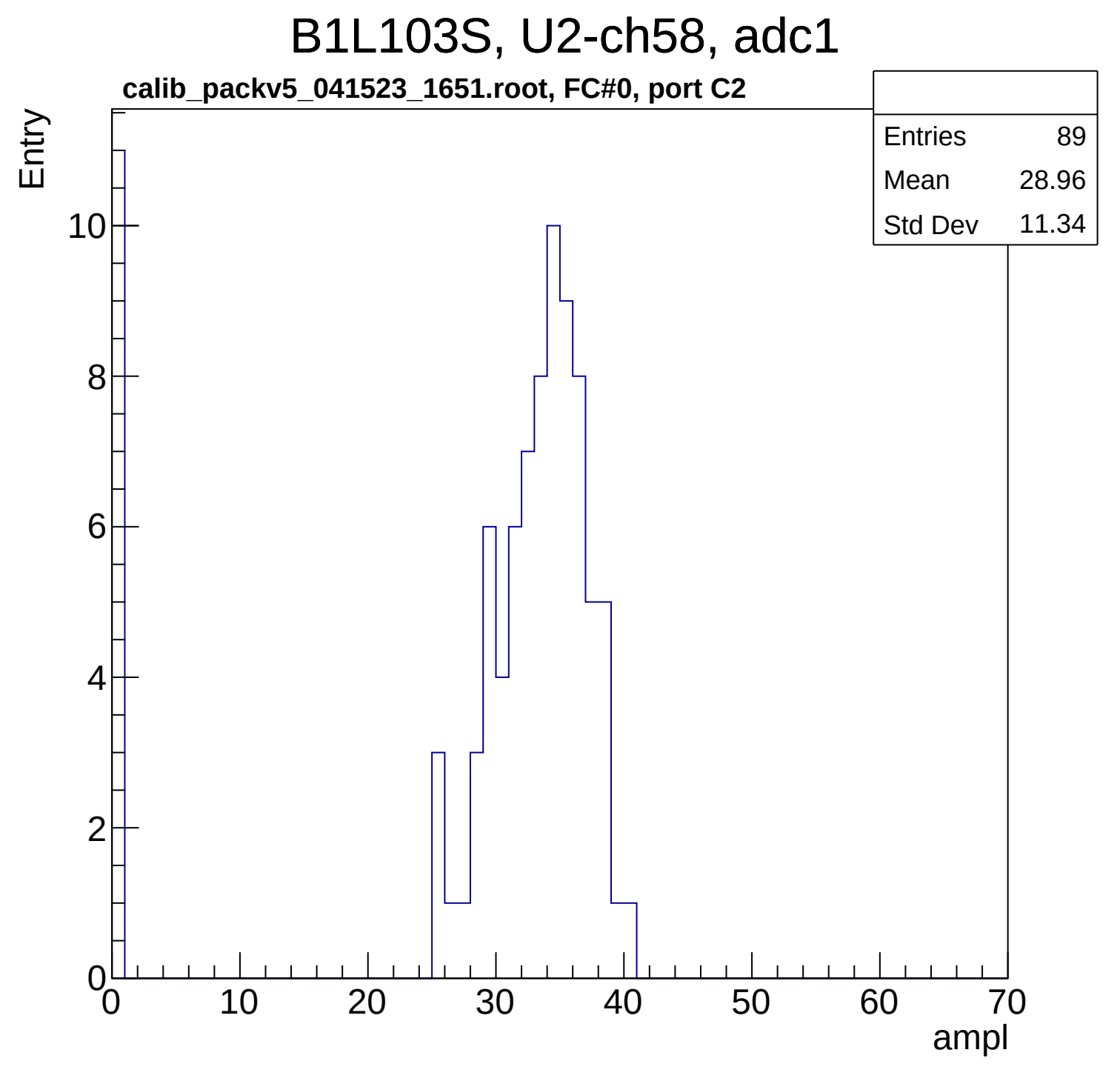

B1L103S, U2-ch57, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.75
Std Dev 3.302
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

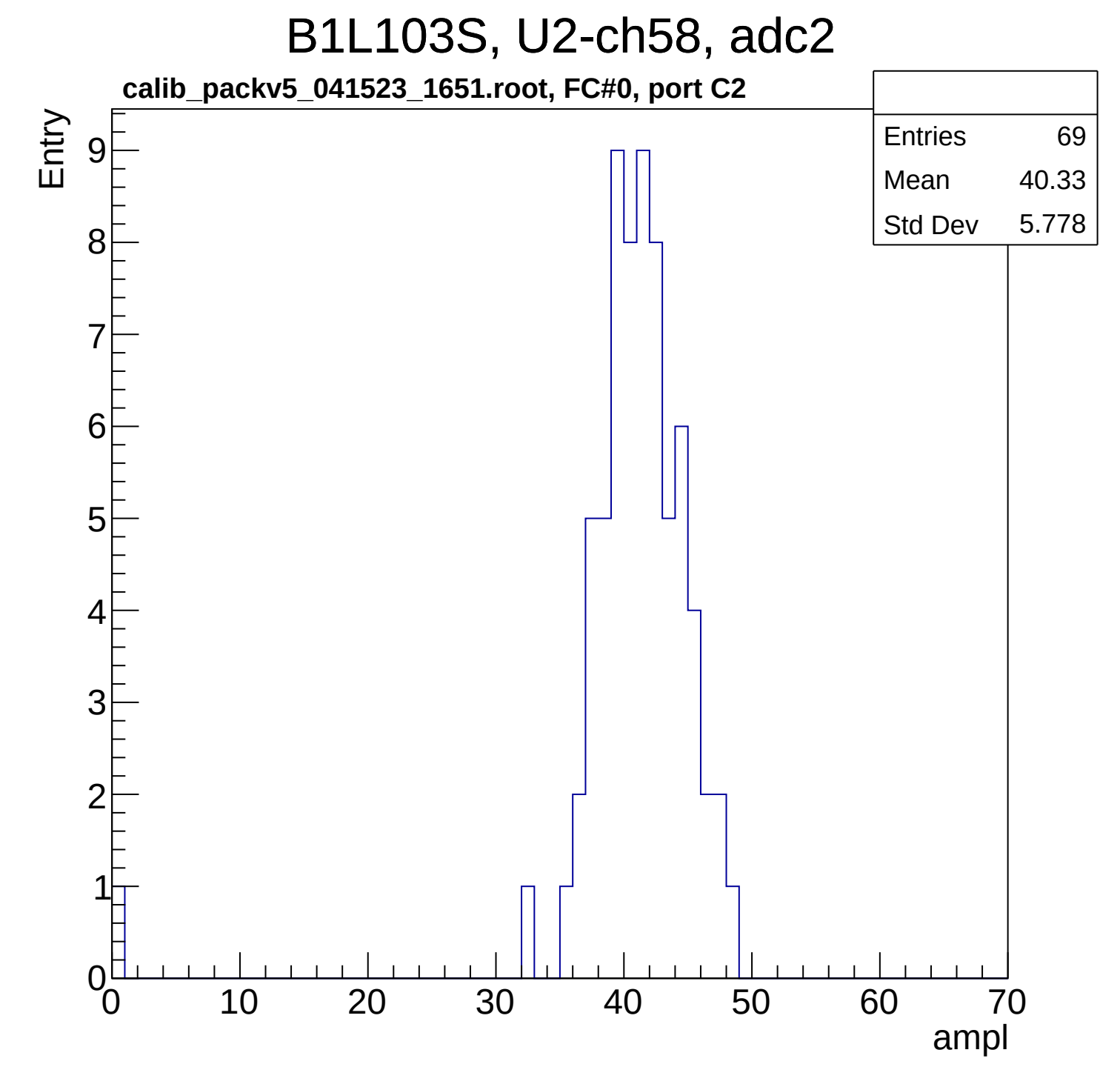

B1L103S, U2-ch57, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 57.9
Std Dev 9.668
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

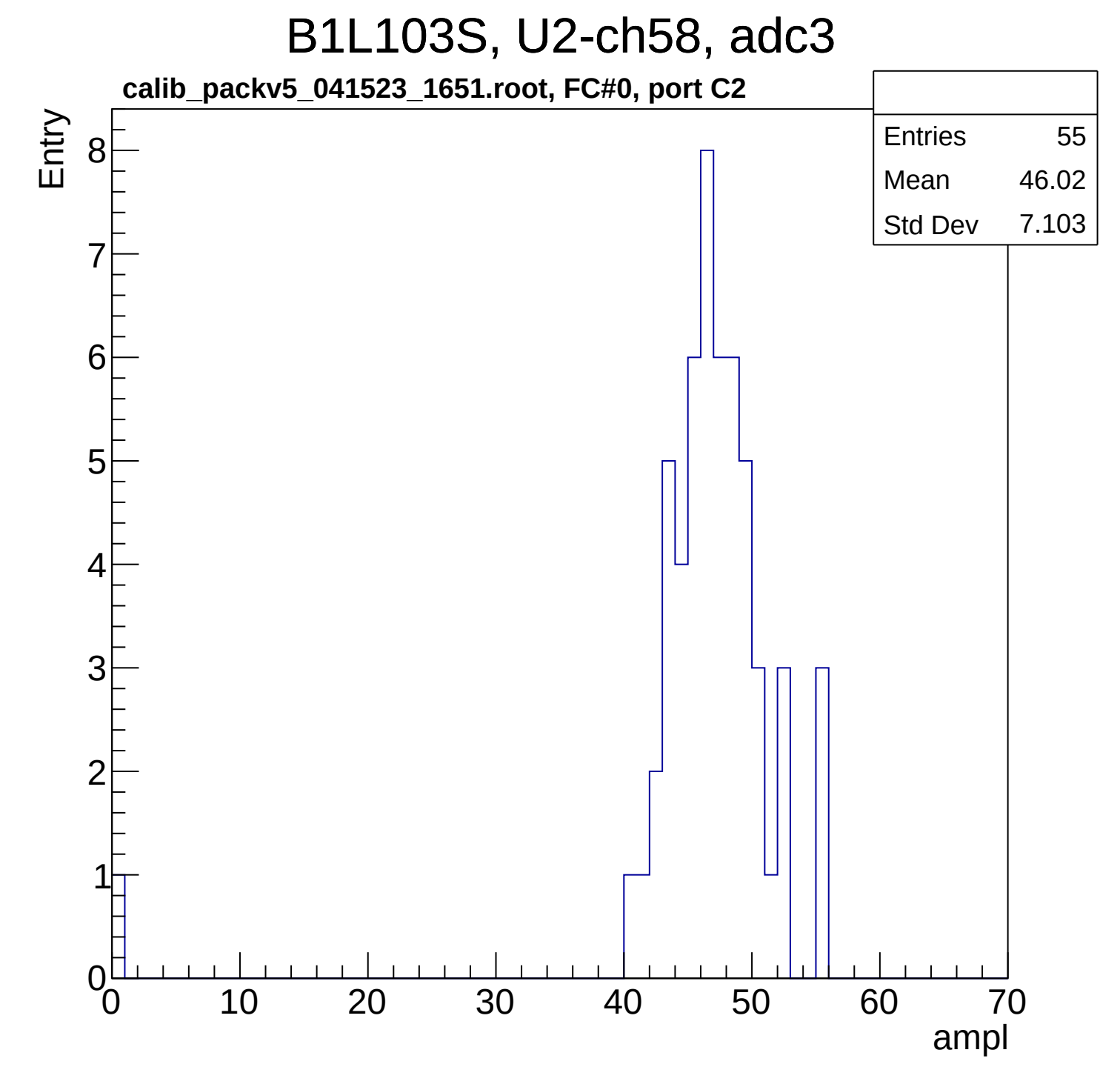

B1L103S, U2-ch57, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 61.62
Std Dev 1.536
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

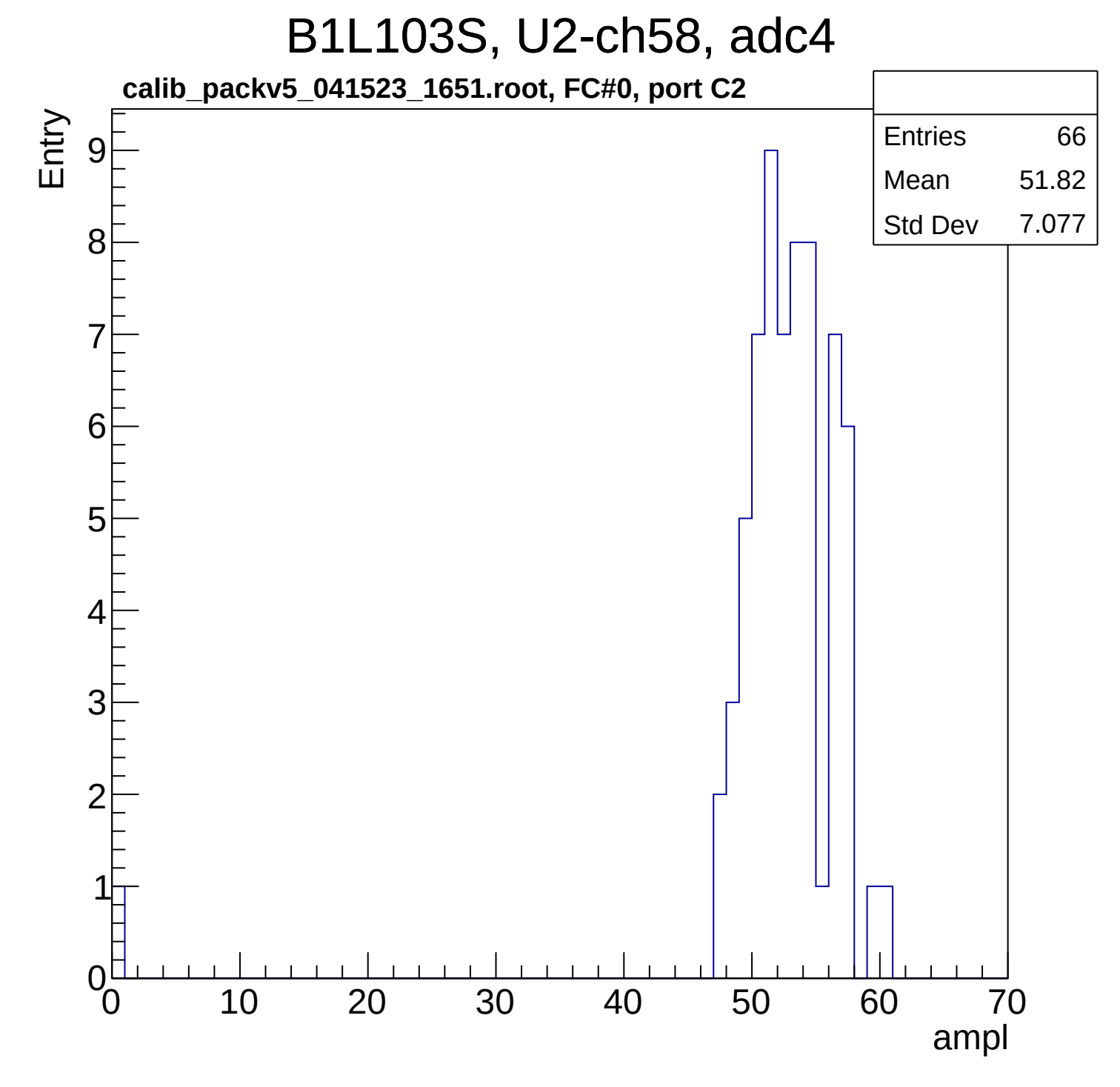

B1L103S, U2-ch57, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

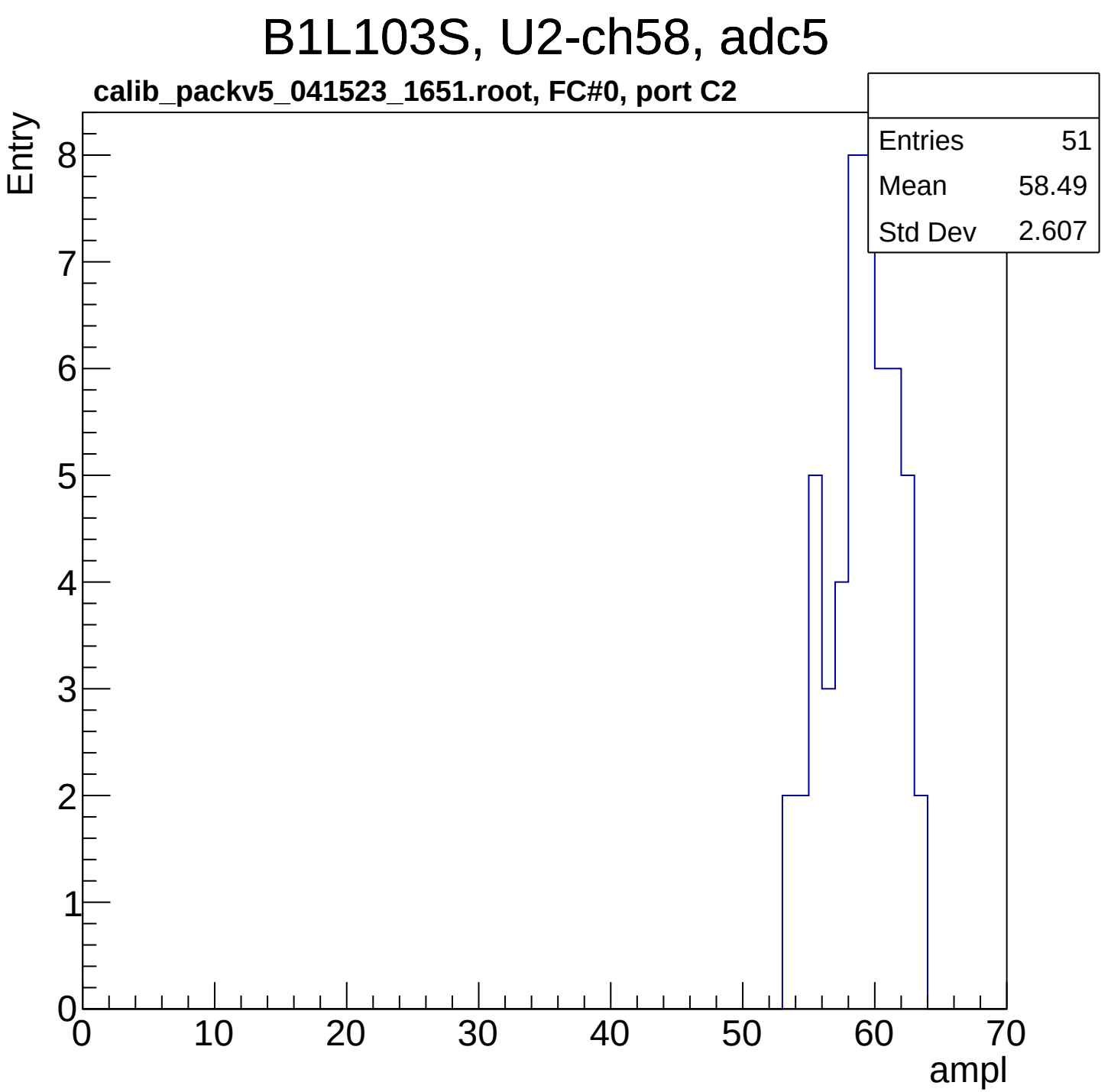

B1L103S, U2-ch58, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 19.41
Std Dev 11.97
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70

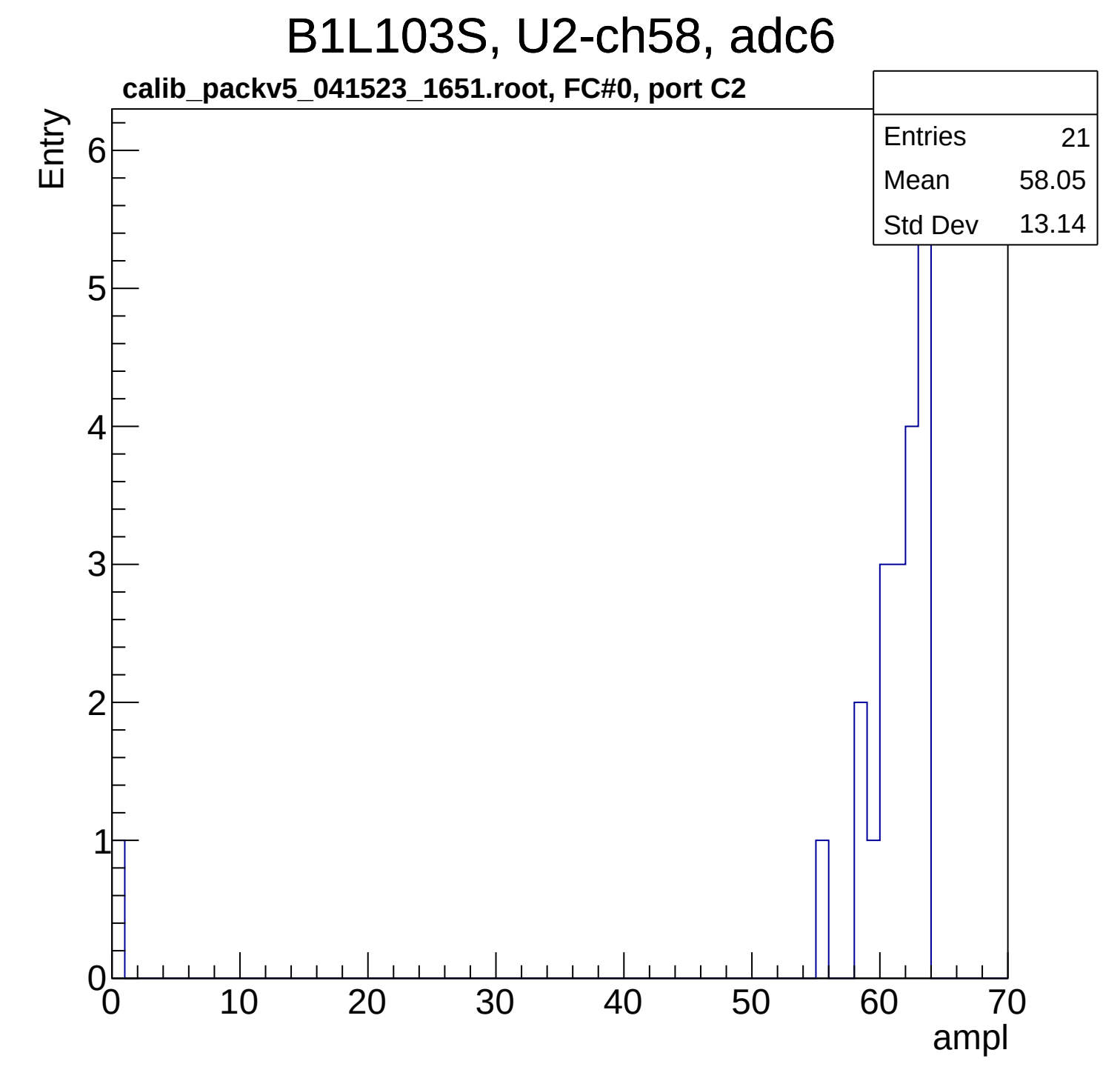

B1L103S, U2-ch58, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 28.96
Std Dev 11.34
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

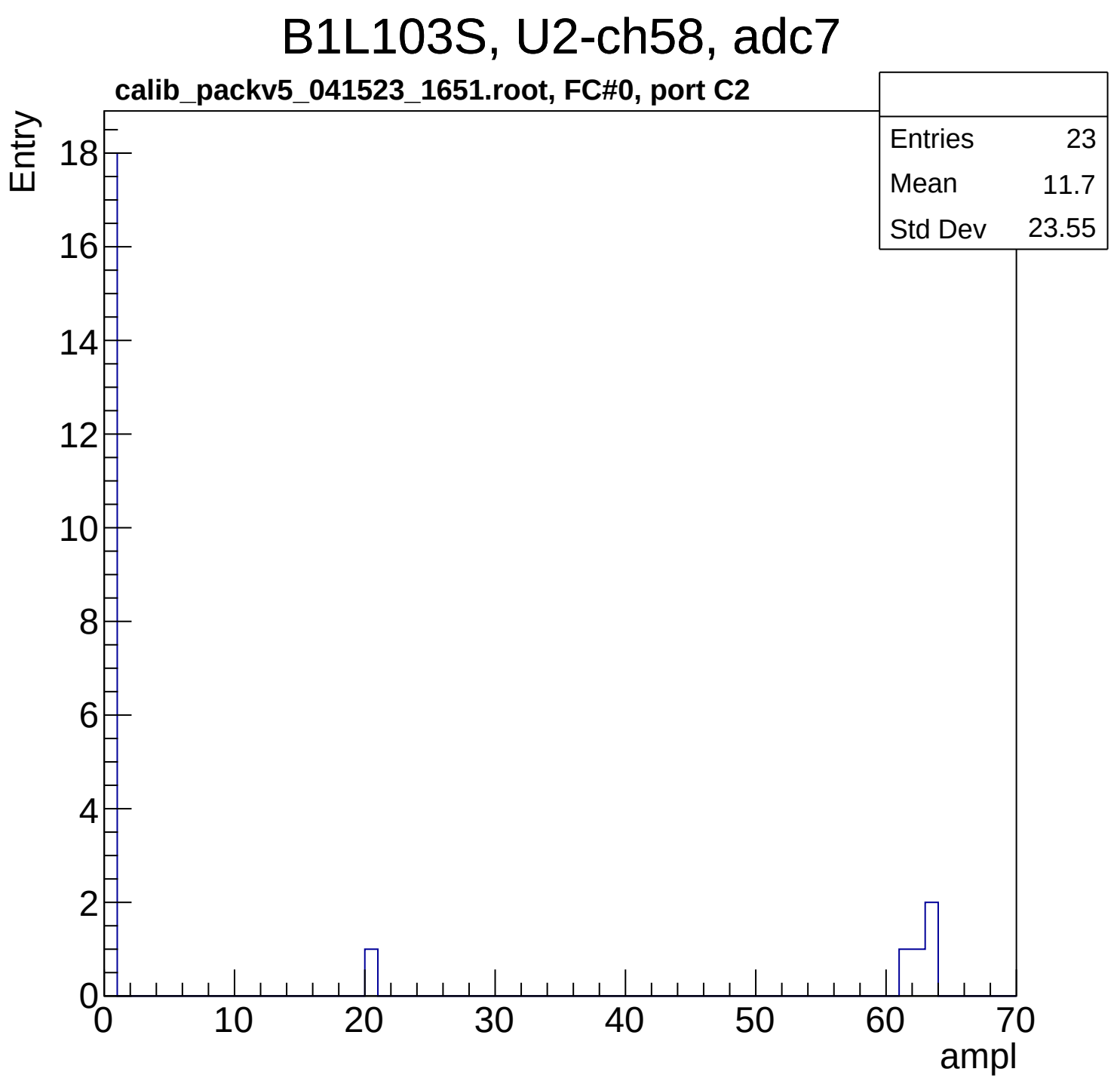

B1L103S, U2-ch58, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 40.33
Std Dev 5.778
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

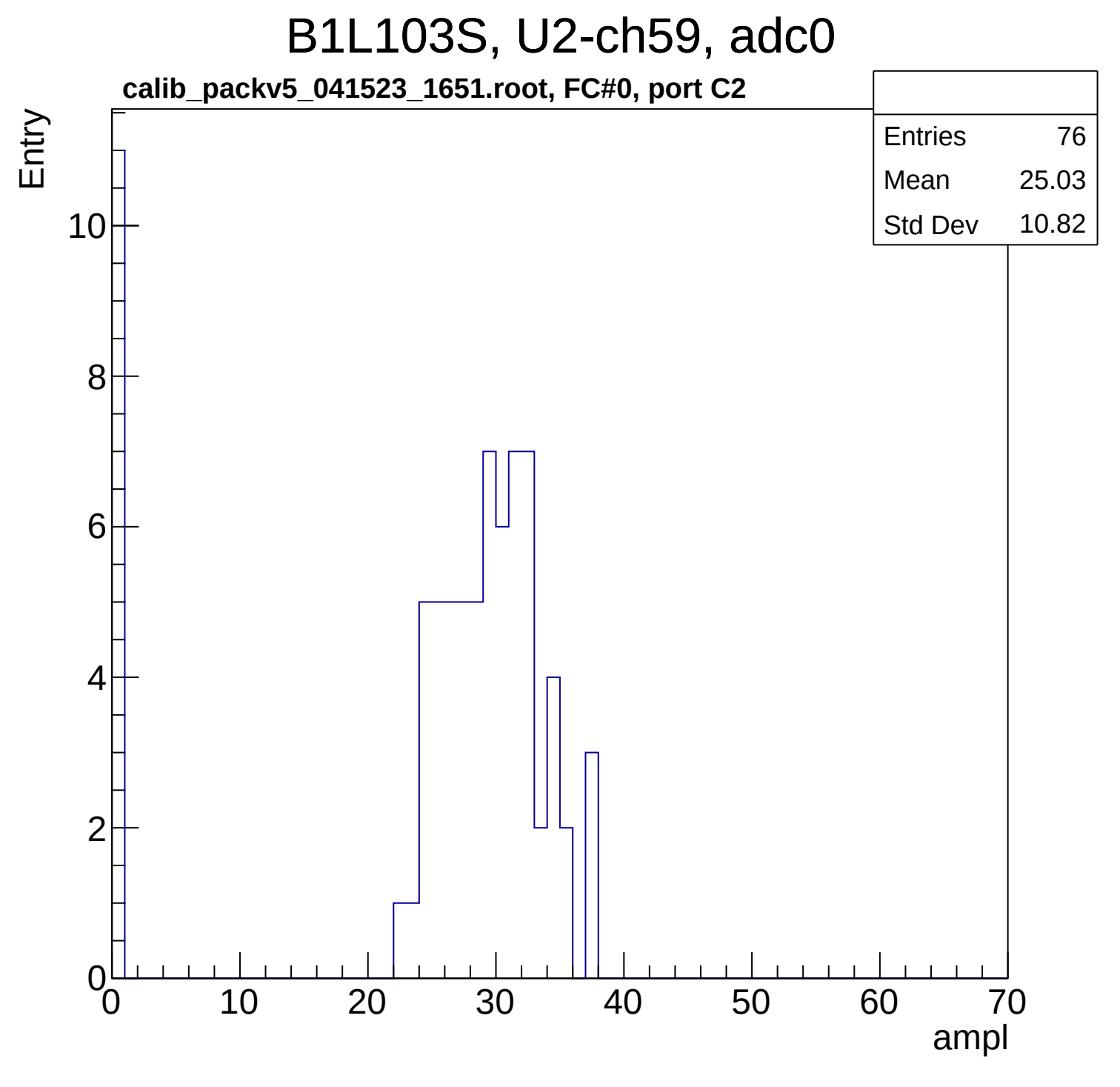

B1L103S, U2-ch58, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 46.02
Std Dev 7.103
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

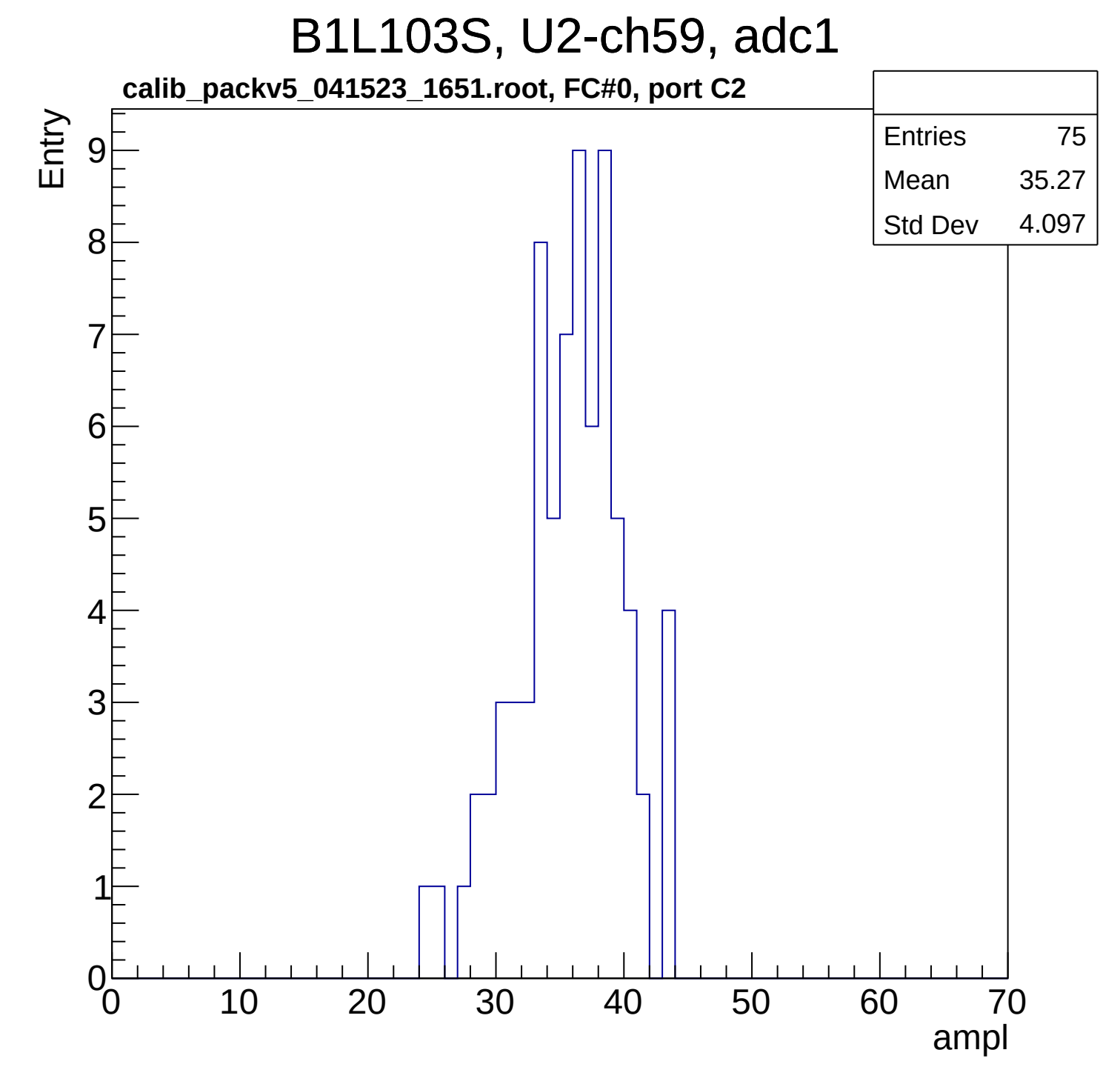

B1L103S, U2-ch58, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 51.82
Std Dev 7.077
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

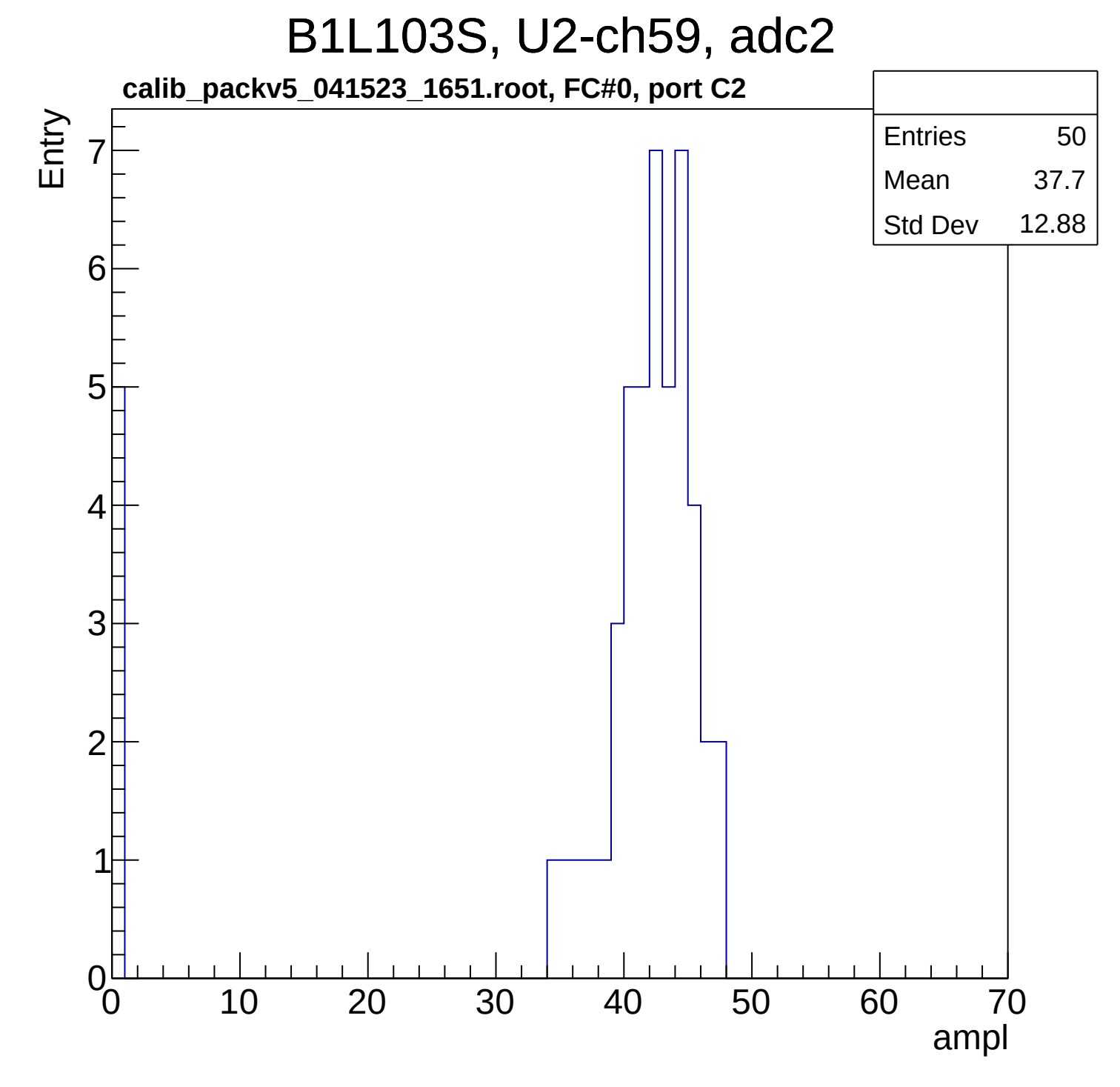

B1L103S, U2-ch58, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.49
Std Dev 2.607
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

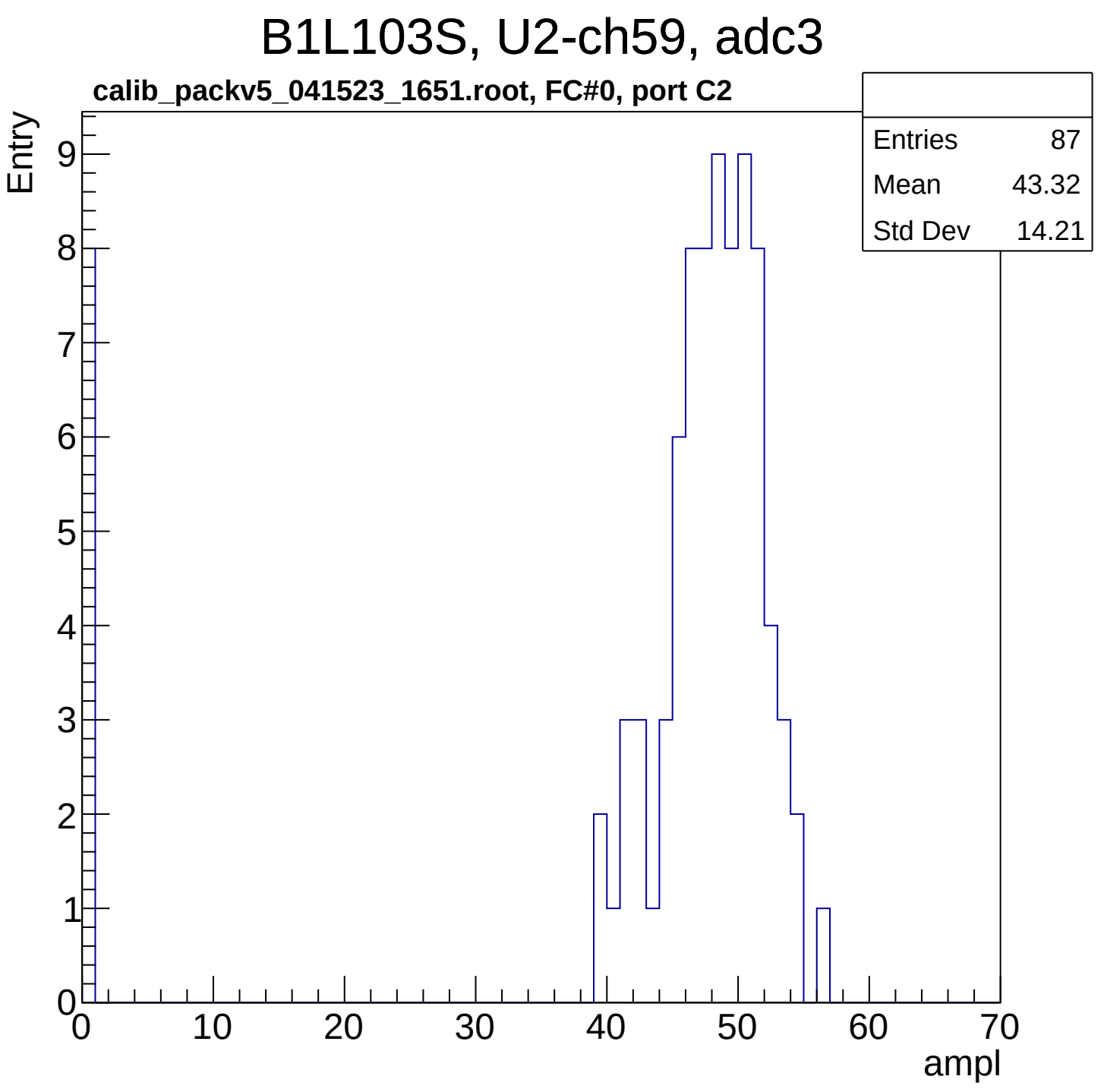

B1L103S, U2-ch58, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 58.05
Std Dev 13.14
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

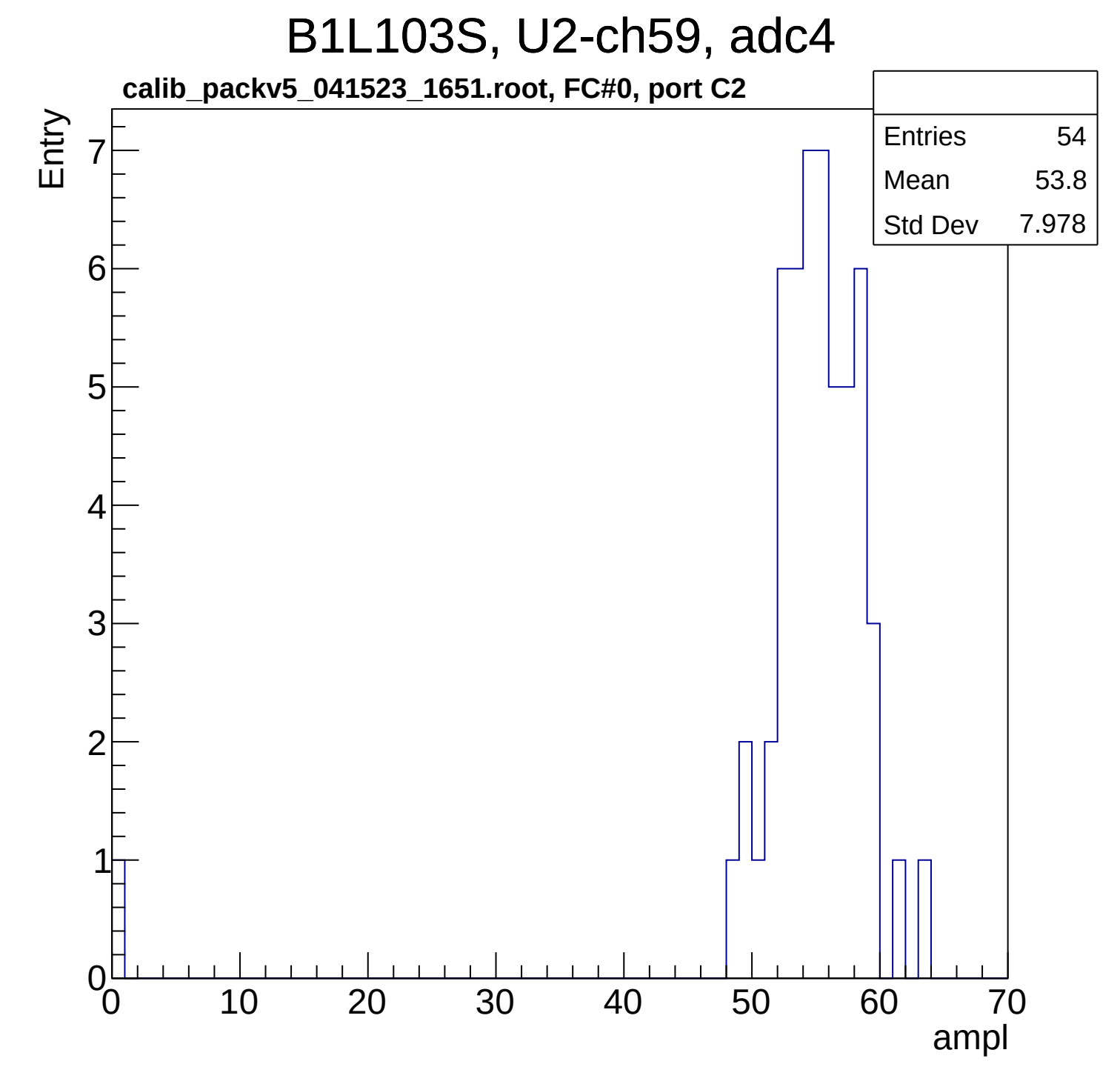

B1L103S, U2-ch58, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 11.7
Std Dev 23.55
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

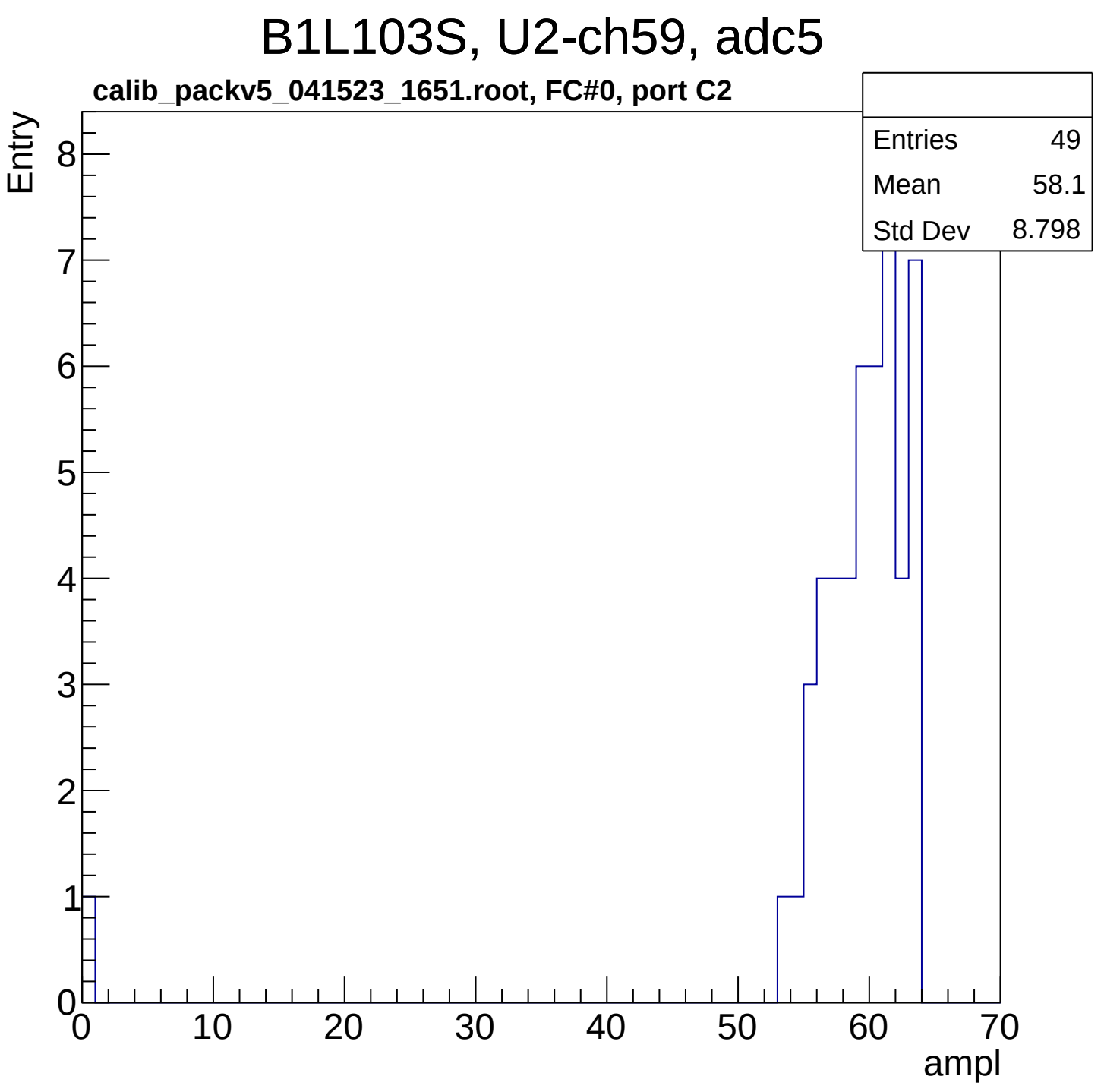

B1L103S, U2-ch59, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 25.03
Std Dev 10.82
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

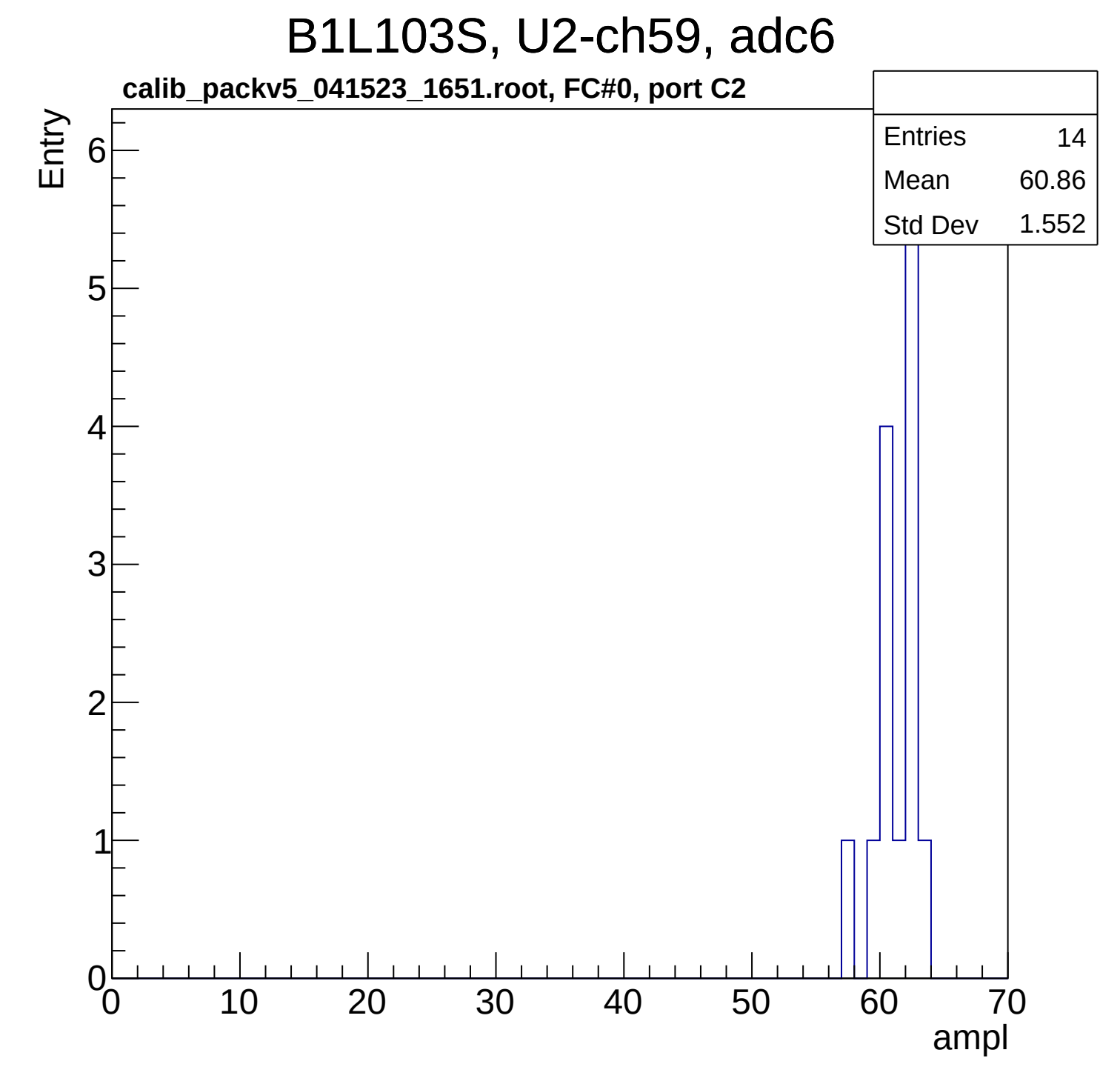

B1L103S, U2-ch59, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 35.27
Std Dev 4.097
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

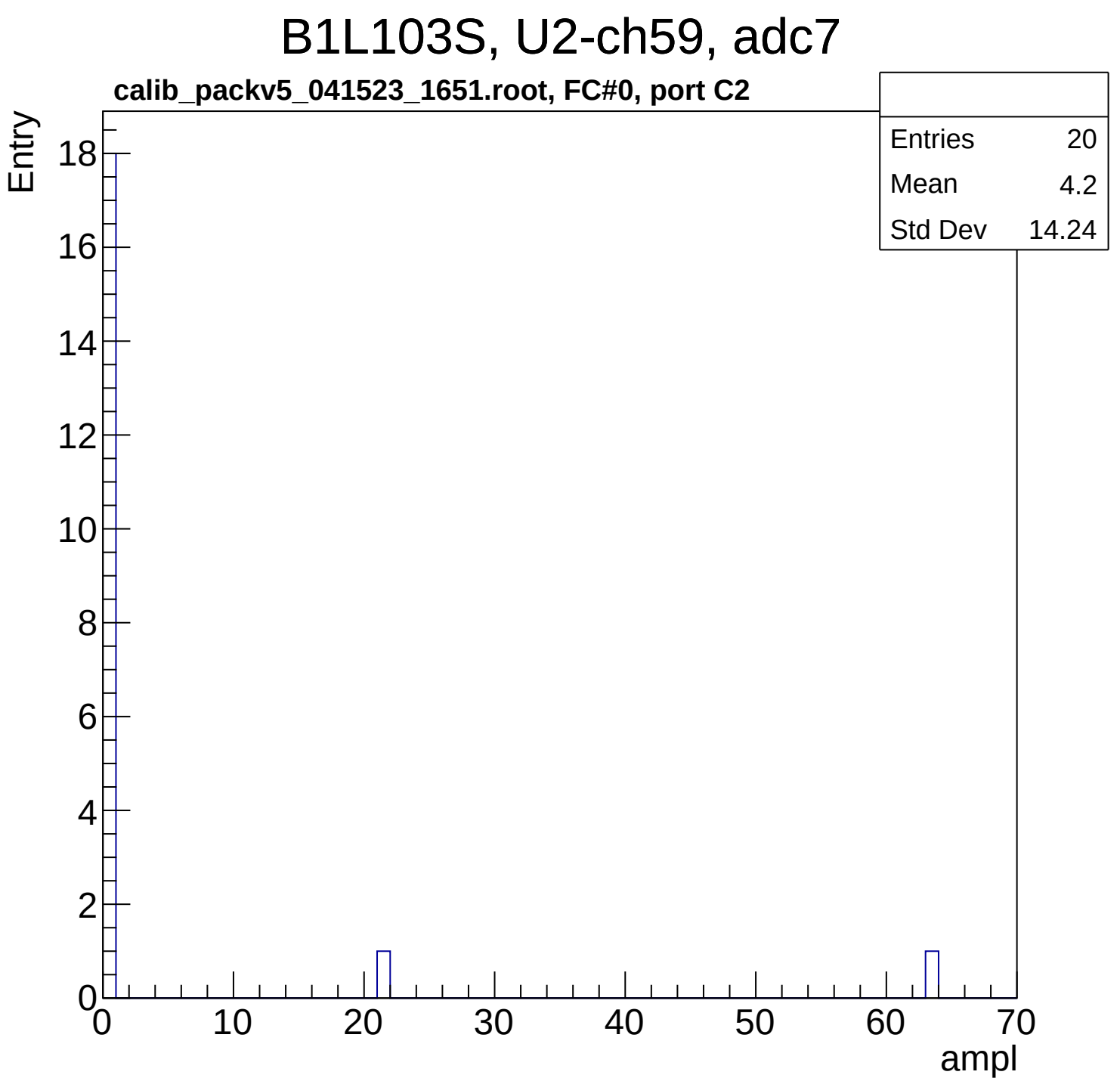

B1L103S, U2-ch59, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 37.7
Std Dev 12.88
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

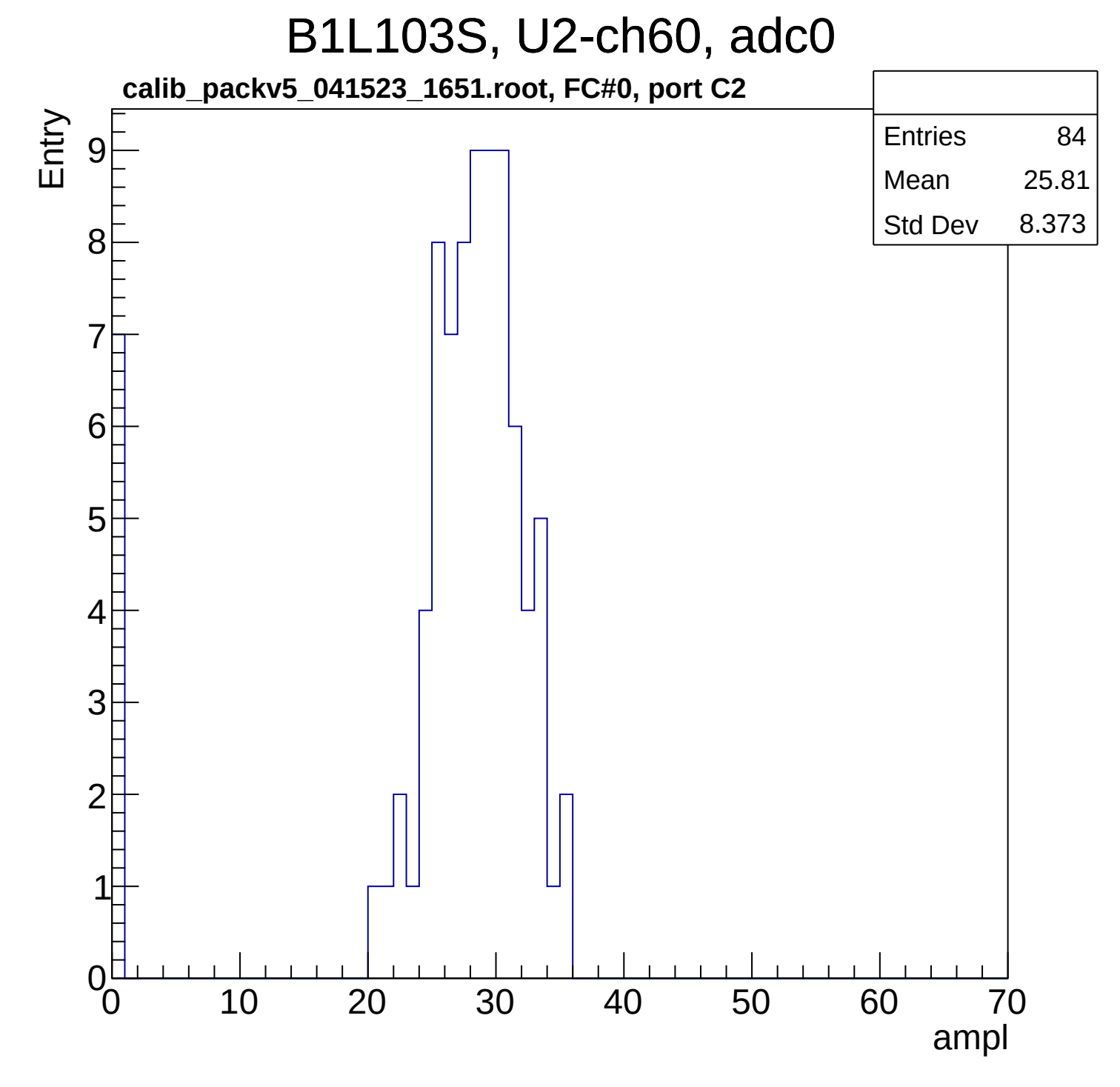

B1L103S, U2-ch59, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 43.32
Std Dev 14.21
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

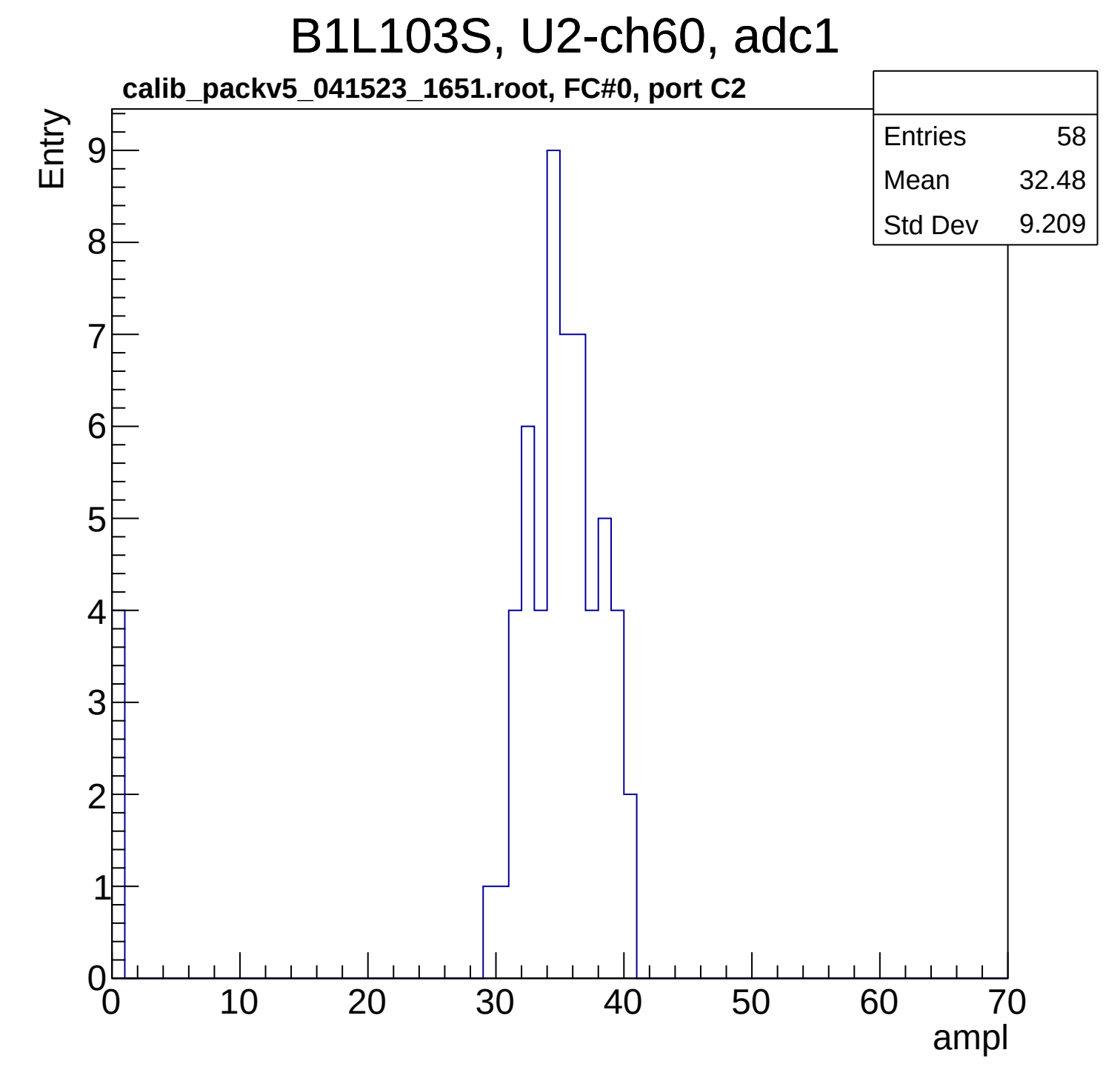

B1L103S, U2-ch59, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 53.8
Std Dev 7.978
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

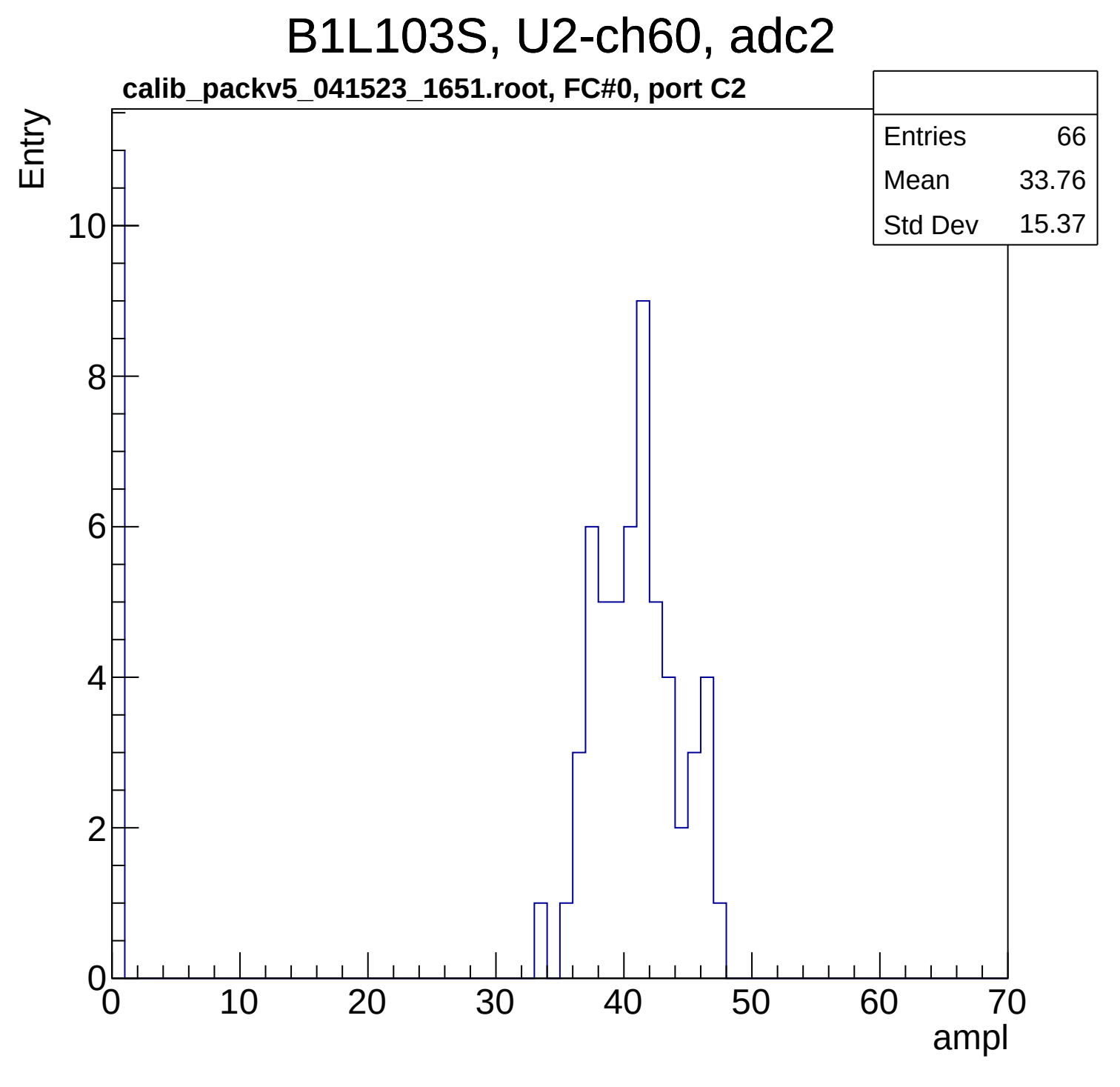

B1L103S, U2-ch59, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.1
Std Dev 8.798
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

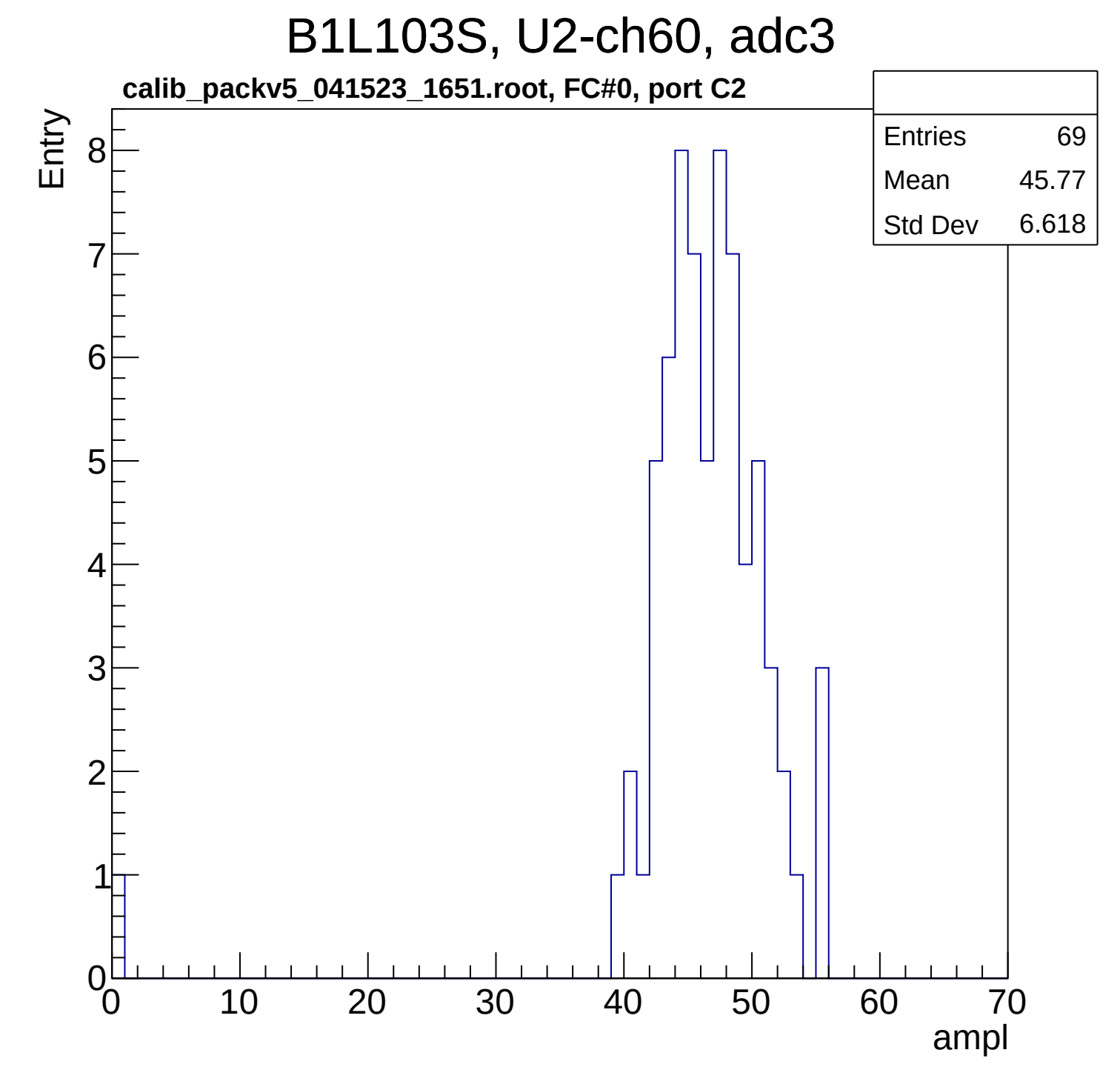

B1L103S, U2-ch59, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 60.86
Std Dev 1.552
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

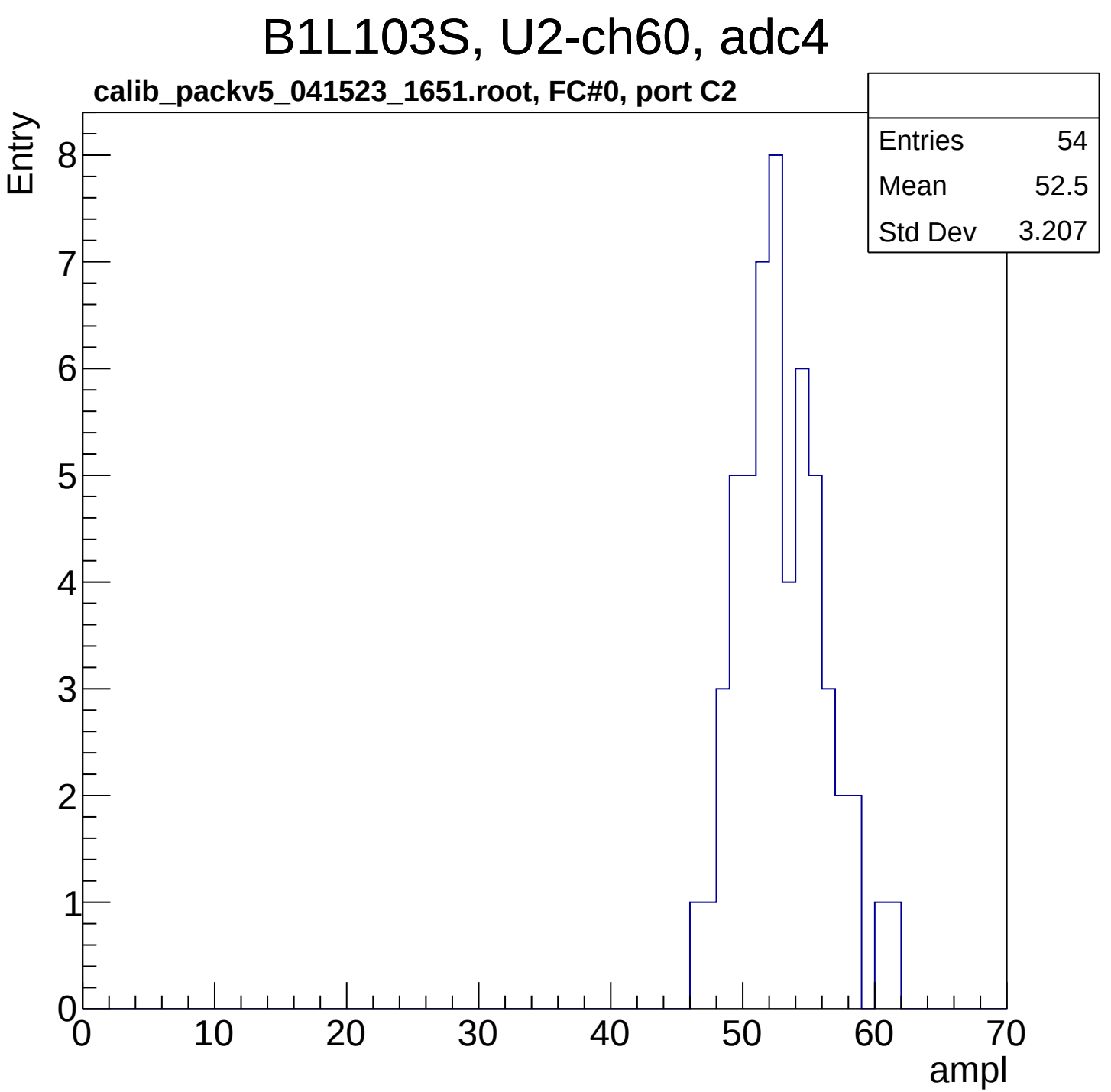

B1L103S, U2-ch59, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.2
Std Dev 14.24
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

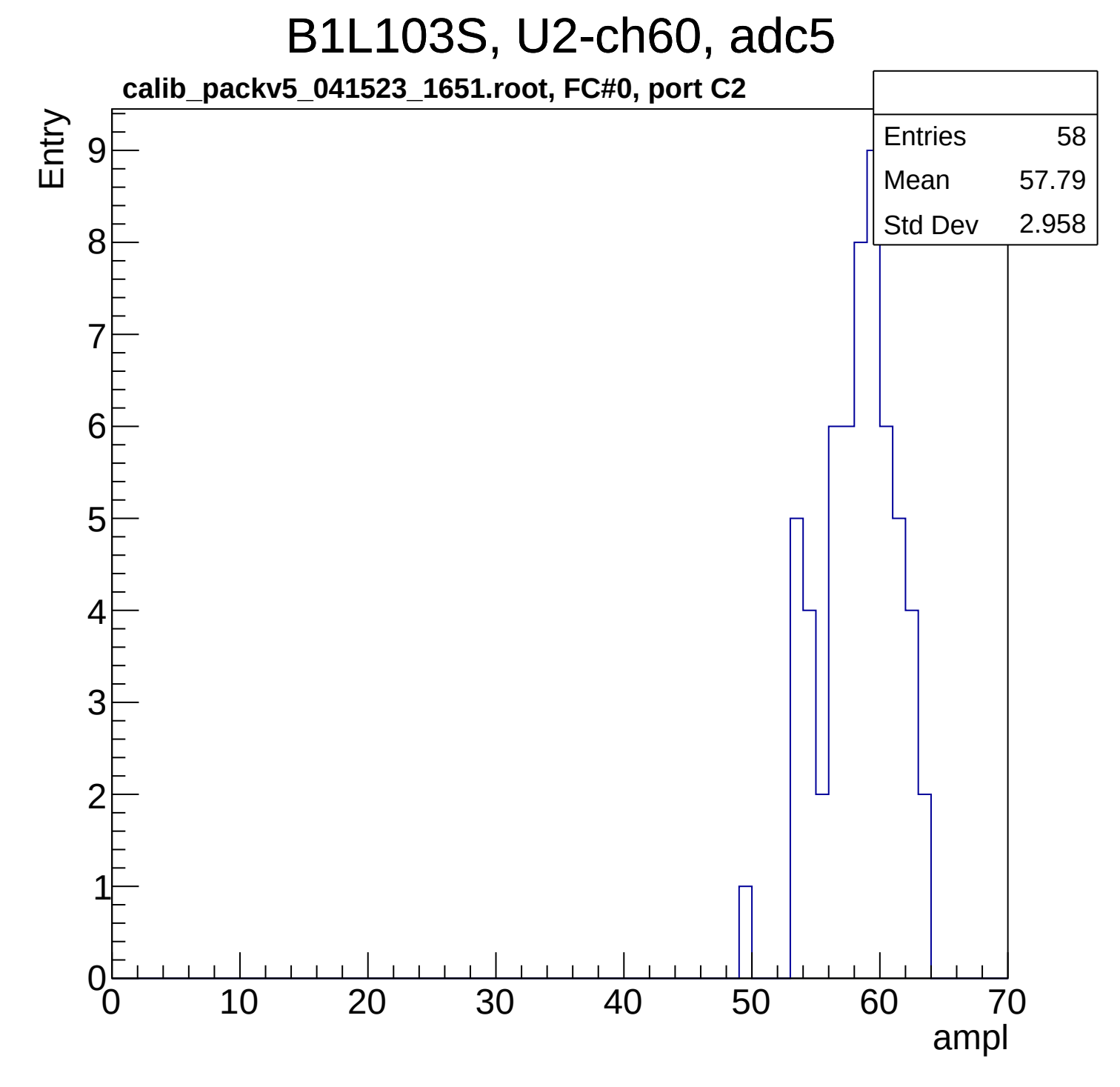

B1L103S, U2-ch60, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 25.81
Std Dev 8.373
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

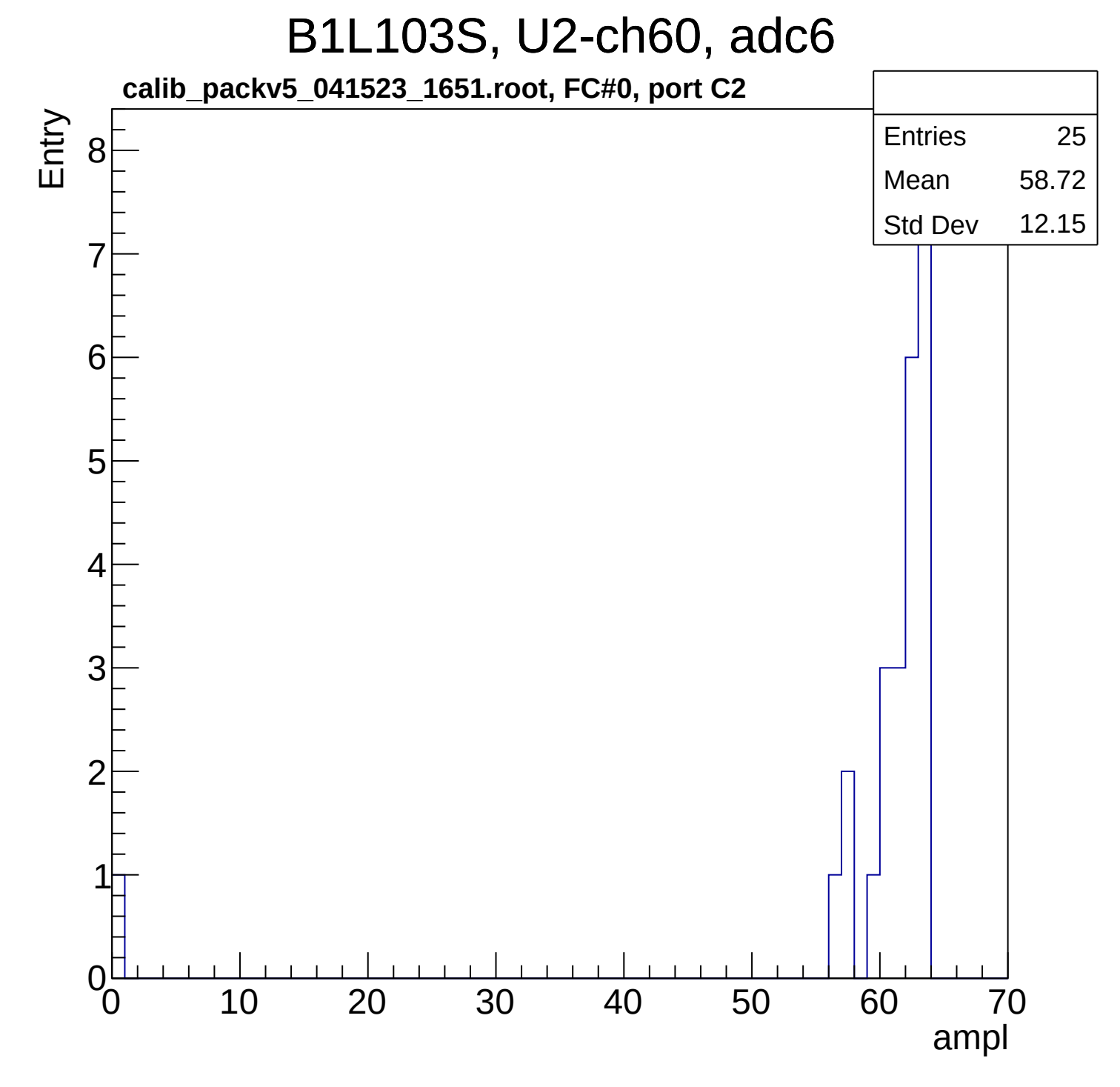

B1L103S, U2-ch60, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 32.48
Std Dev 9.209
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

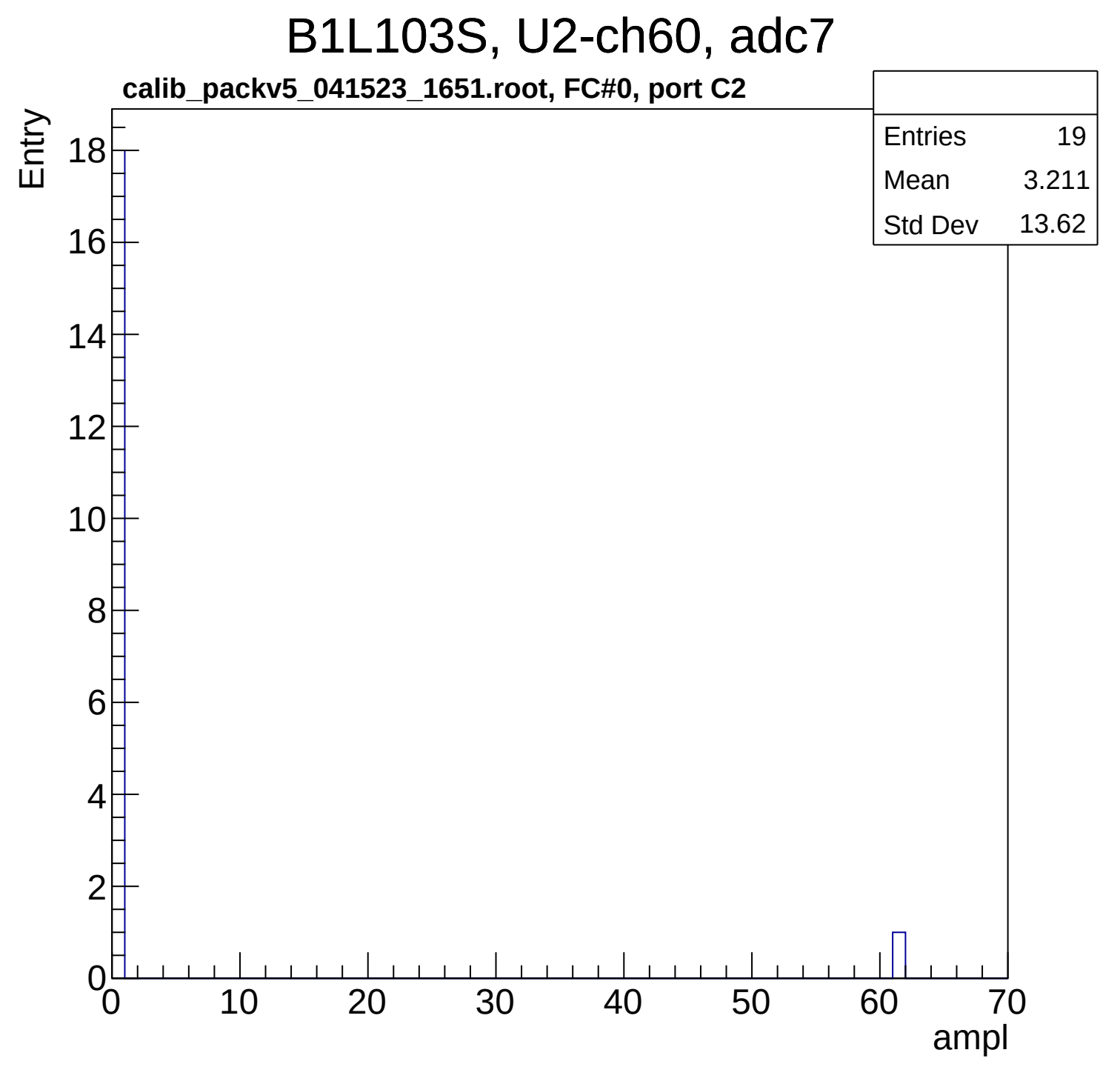

B1L103S, U2-ch60, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 33.76
Std Dev 15.37
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

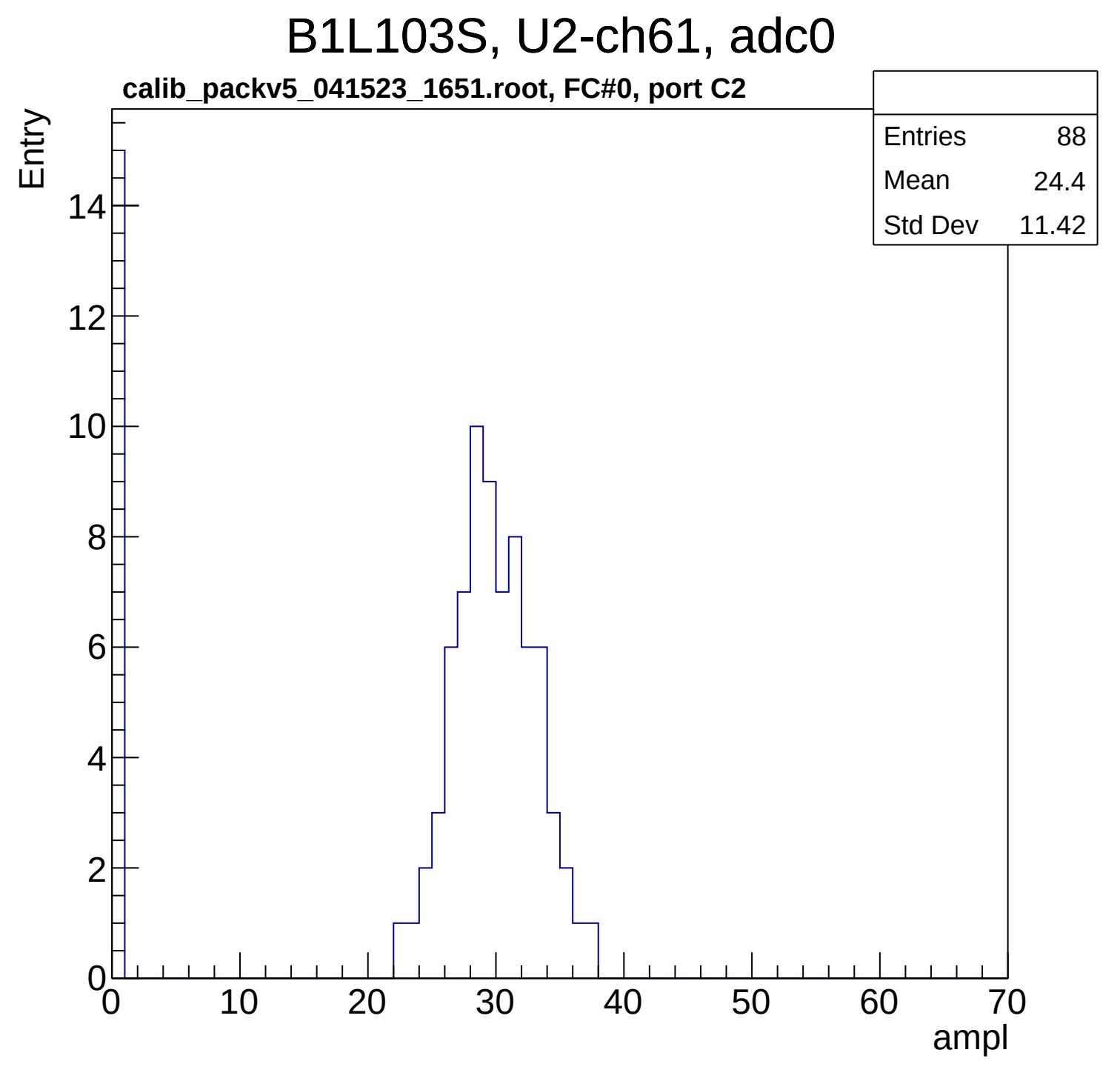

B1L103S, U2-ch60, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 45.77
Std Dev 6.618
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

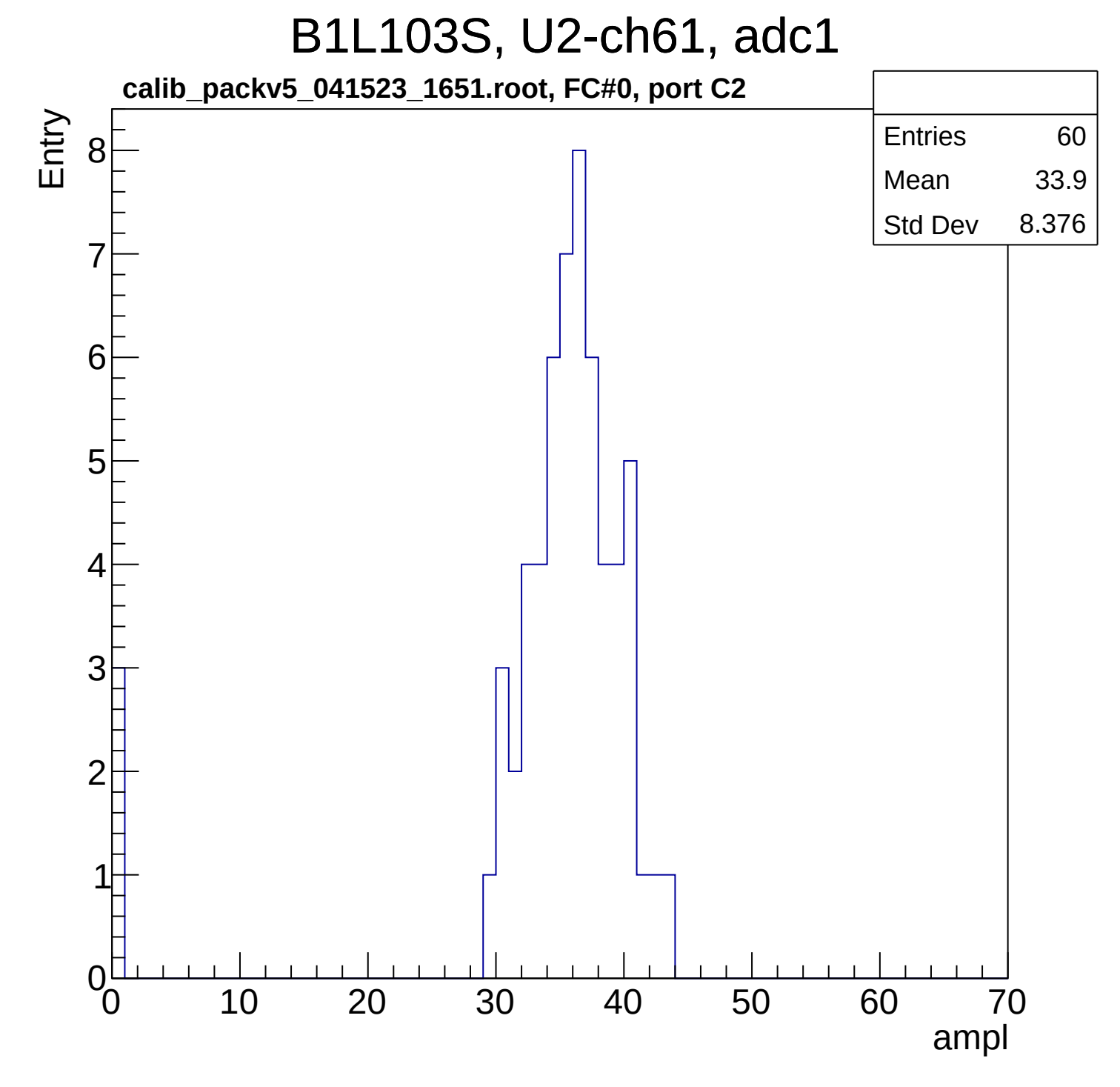

B1L103S, U2-ch60, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 52.5
Std Dev 3.207
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

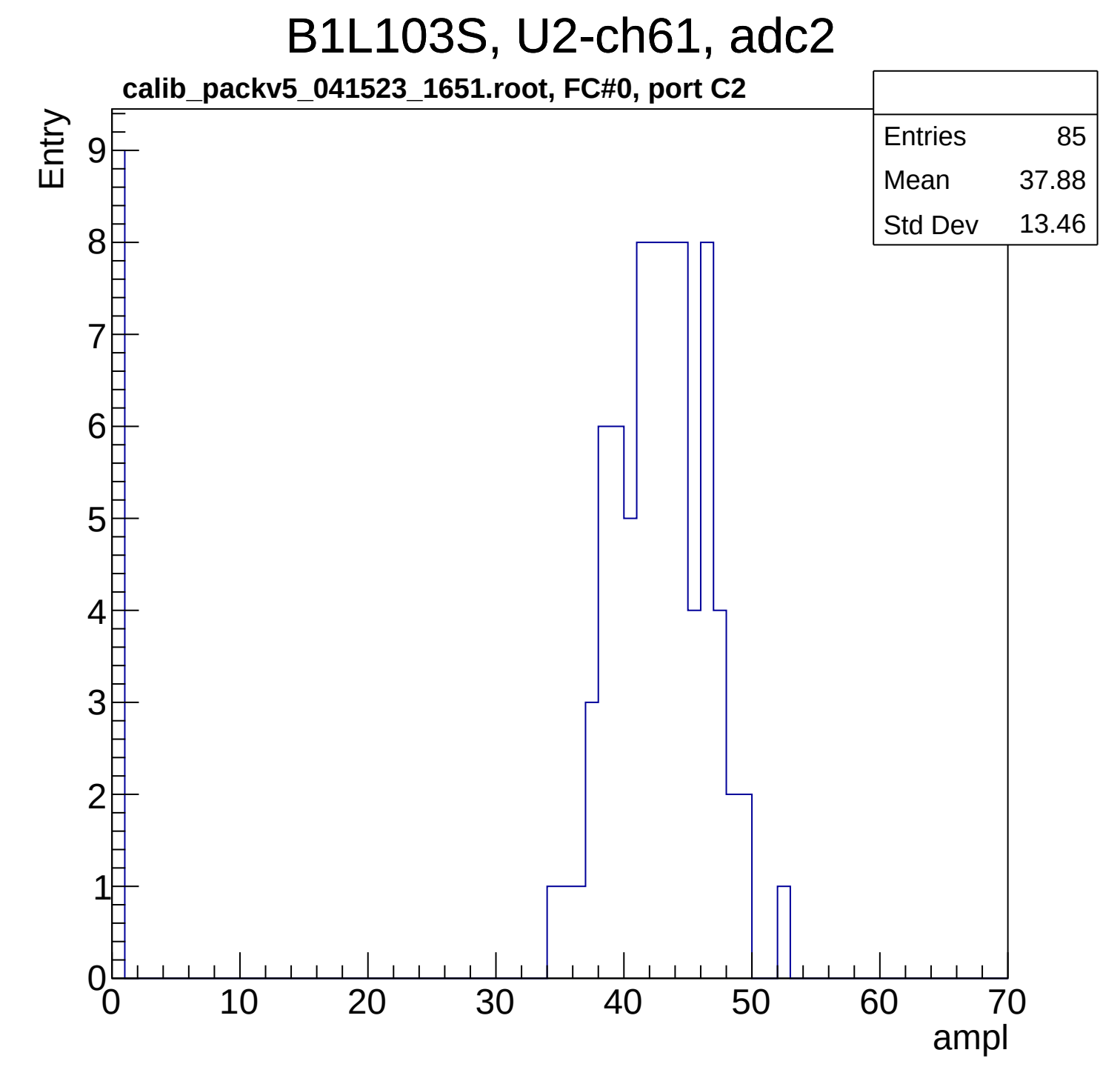

B1L103S, U2-ch60, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 57.79
Std Dev 2.958
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

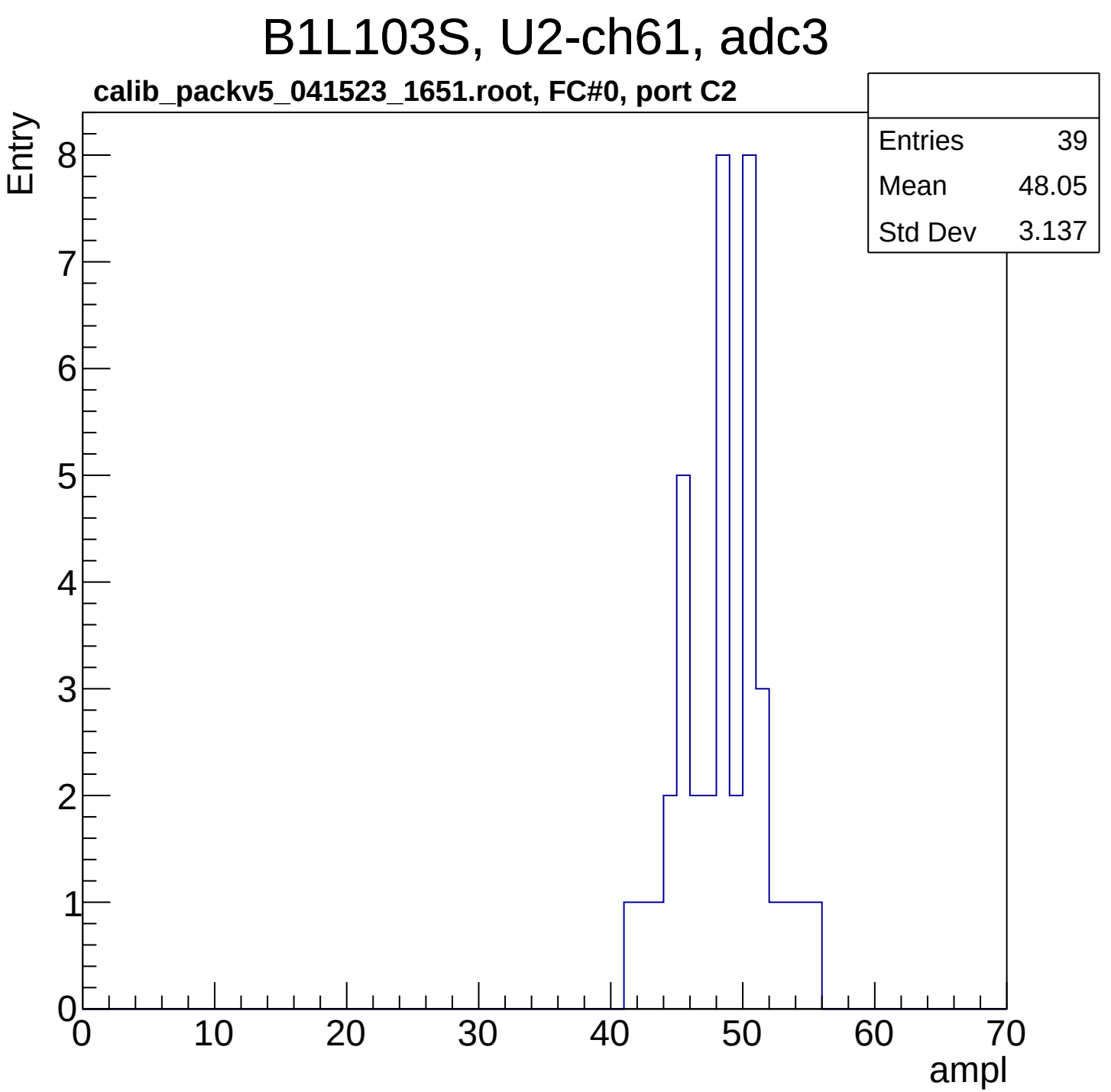

B1L103S, U2-ch60, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 58.72
Std Dev 12.15
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

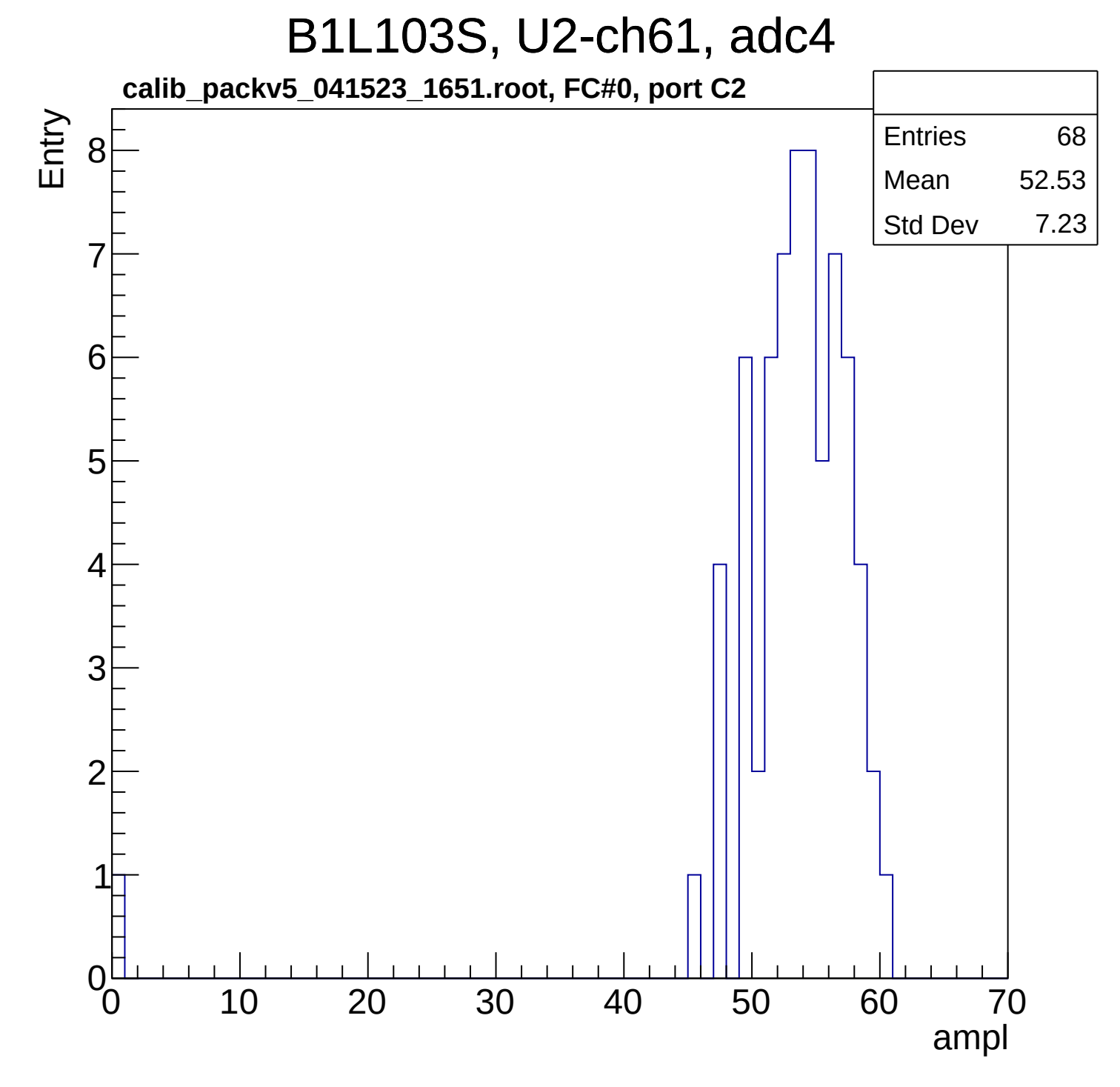

B1L103S, U2-ch60, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.211
Std Dev 13.62
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

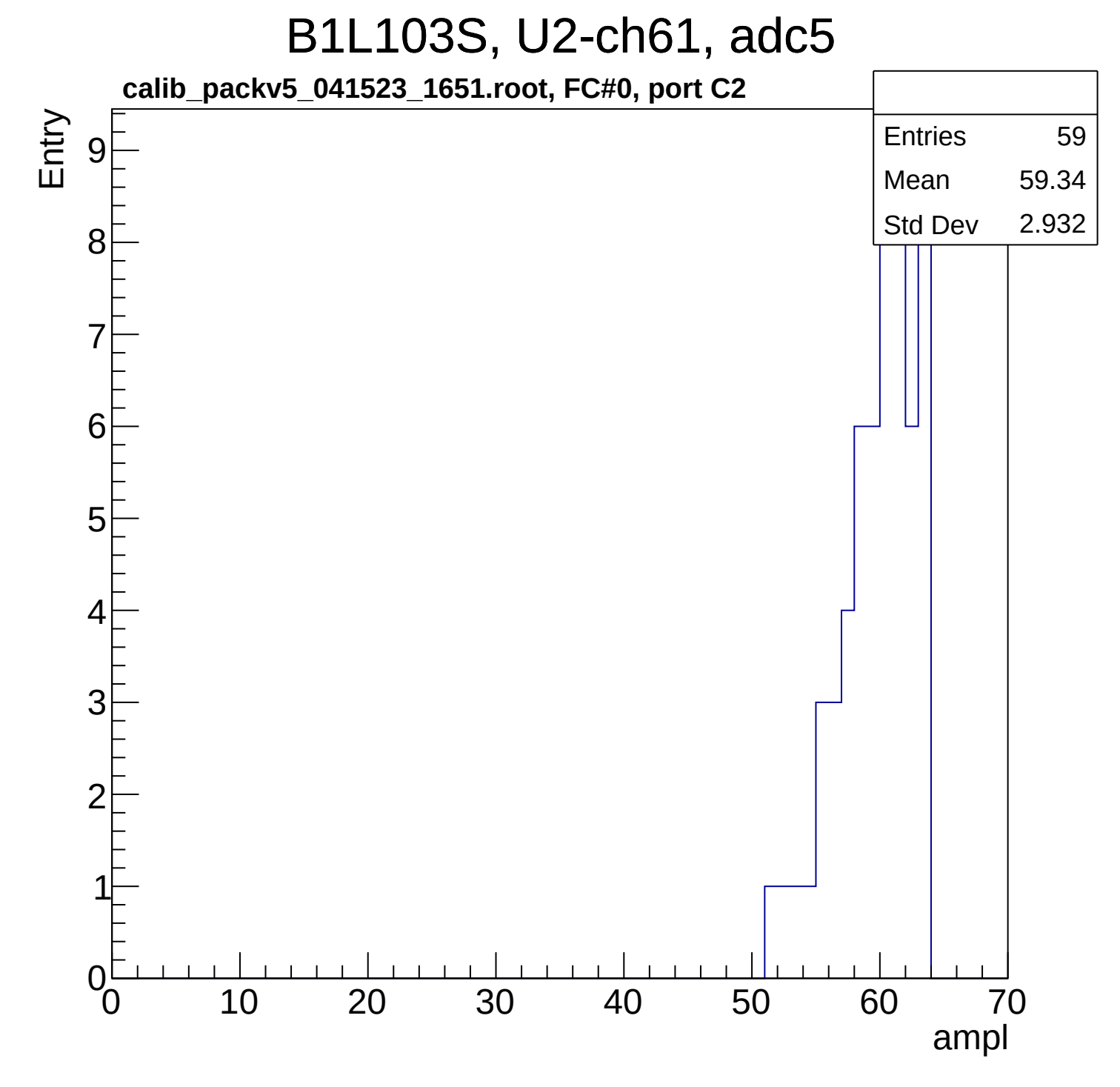

B1L103S, U2-ch61, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 24.4
Std Dev 11.42
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

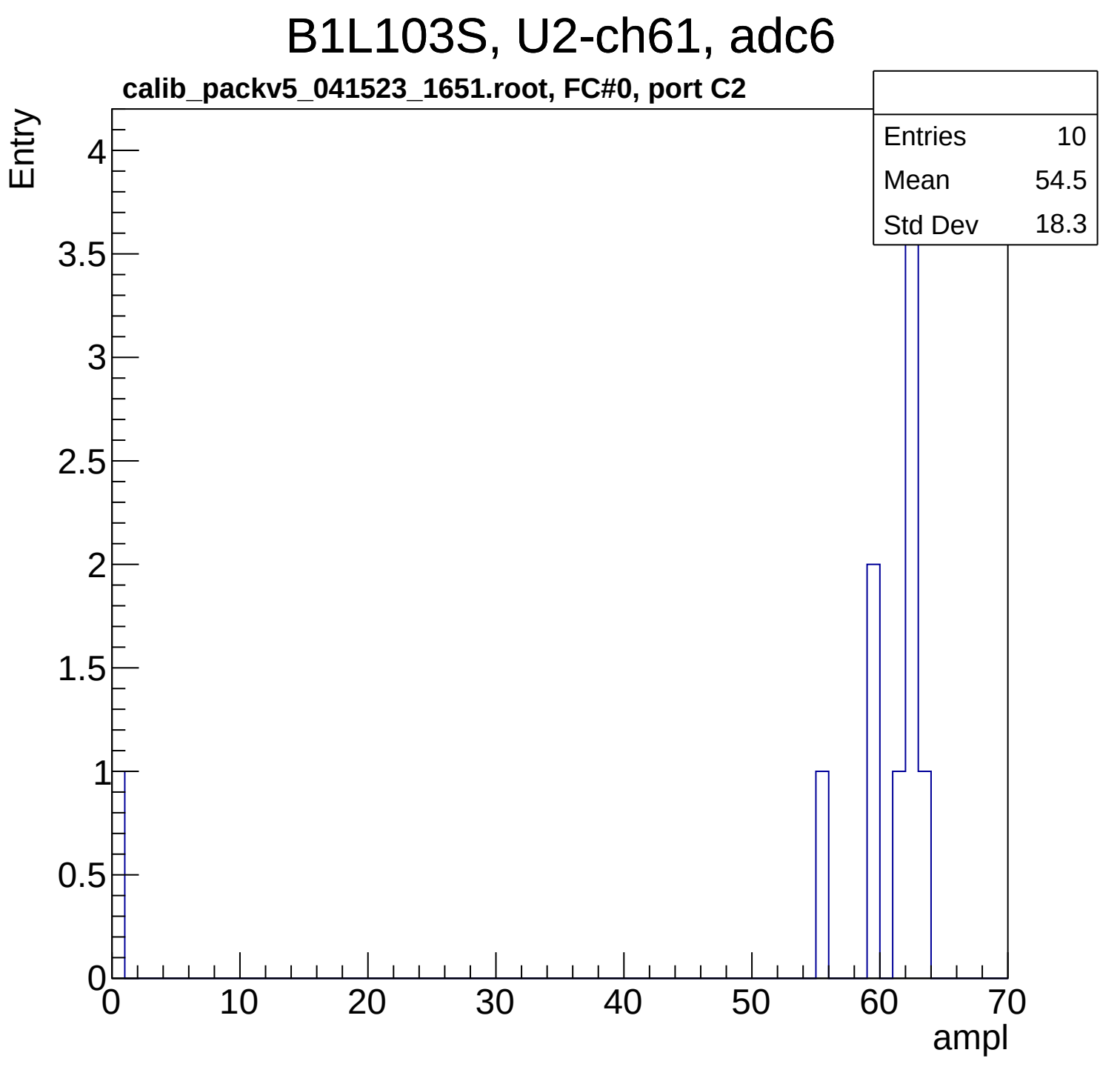

B1L103S, U2-ch61, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 33.9
Std Dev 8.376
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

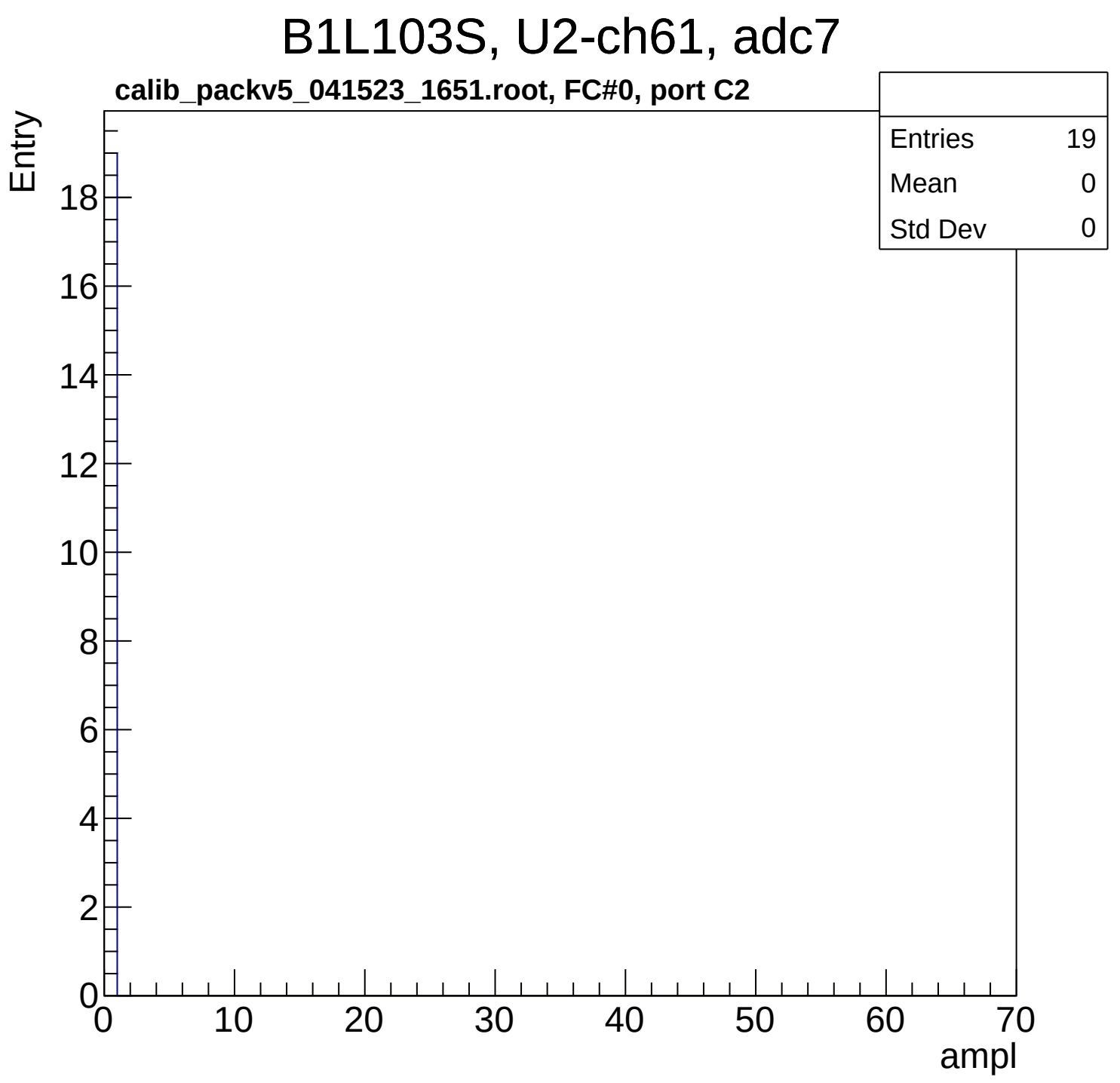

B1L103S, U2-ch61, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 37.88
Std Dev 13.46
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

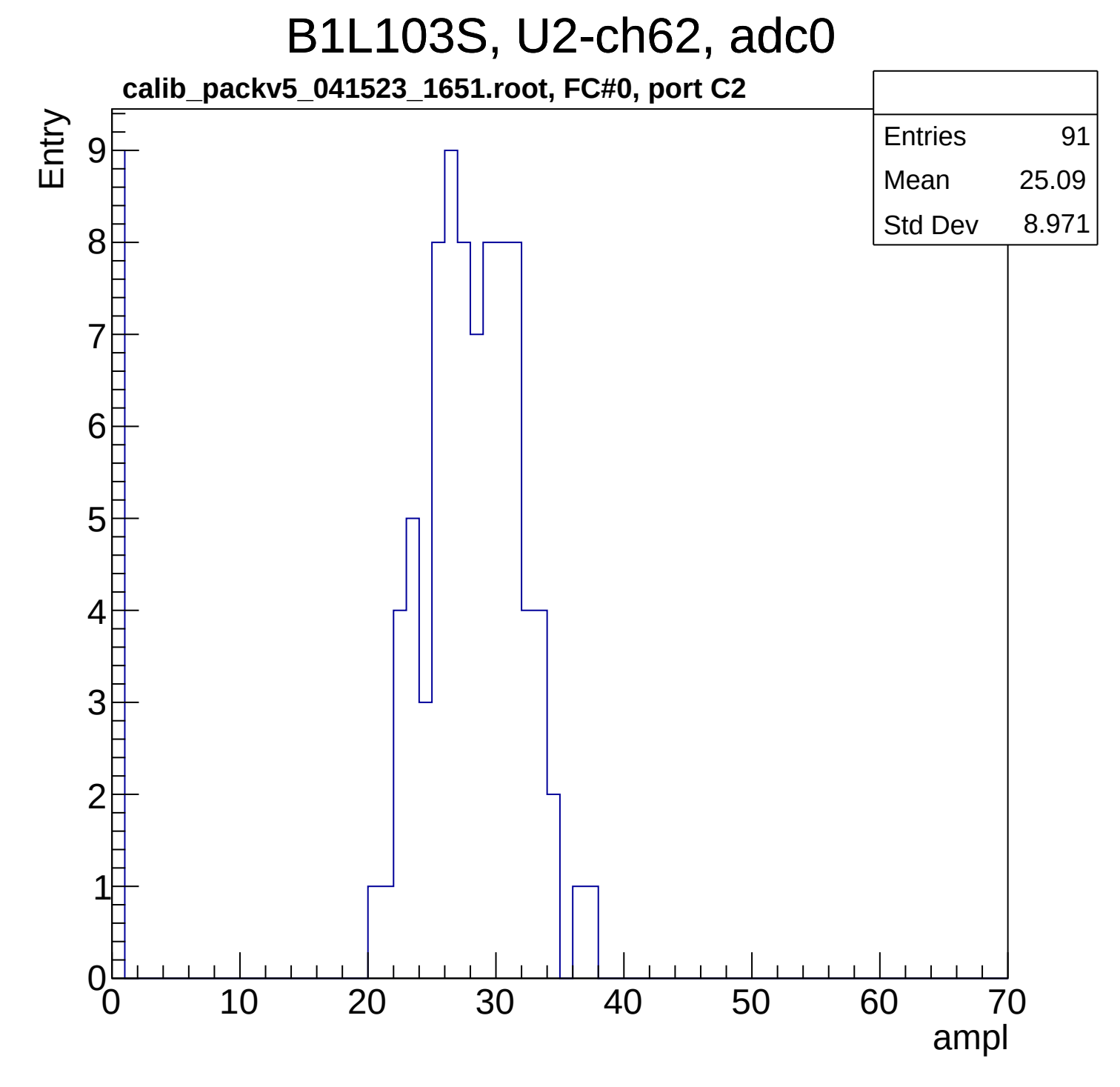

B1L103S, U2-ch61, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 48.05
Std Dev 3.137
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

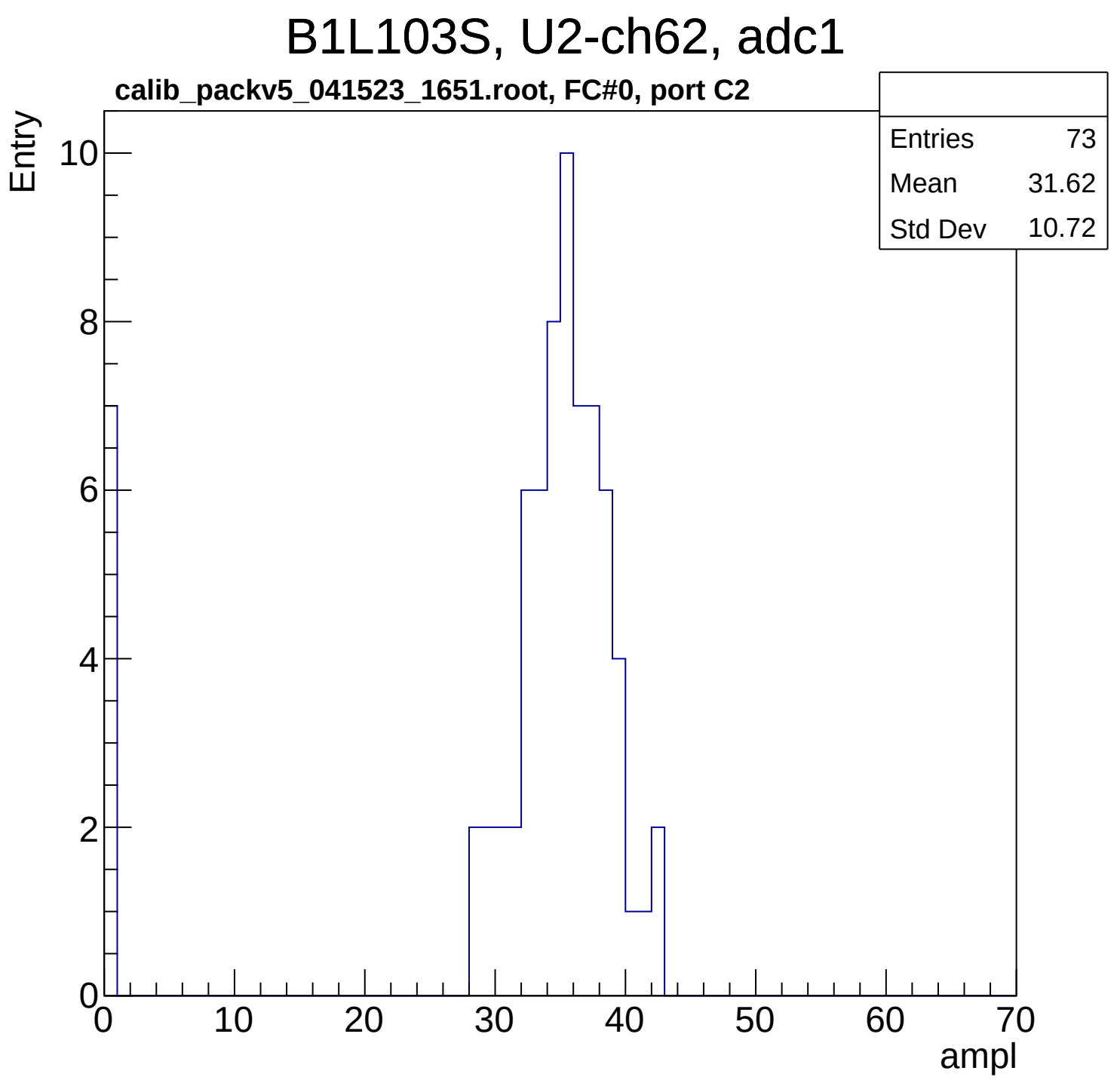

B1L103S, U2-ch61, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 52.53
Std Dev 7.23
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

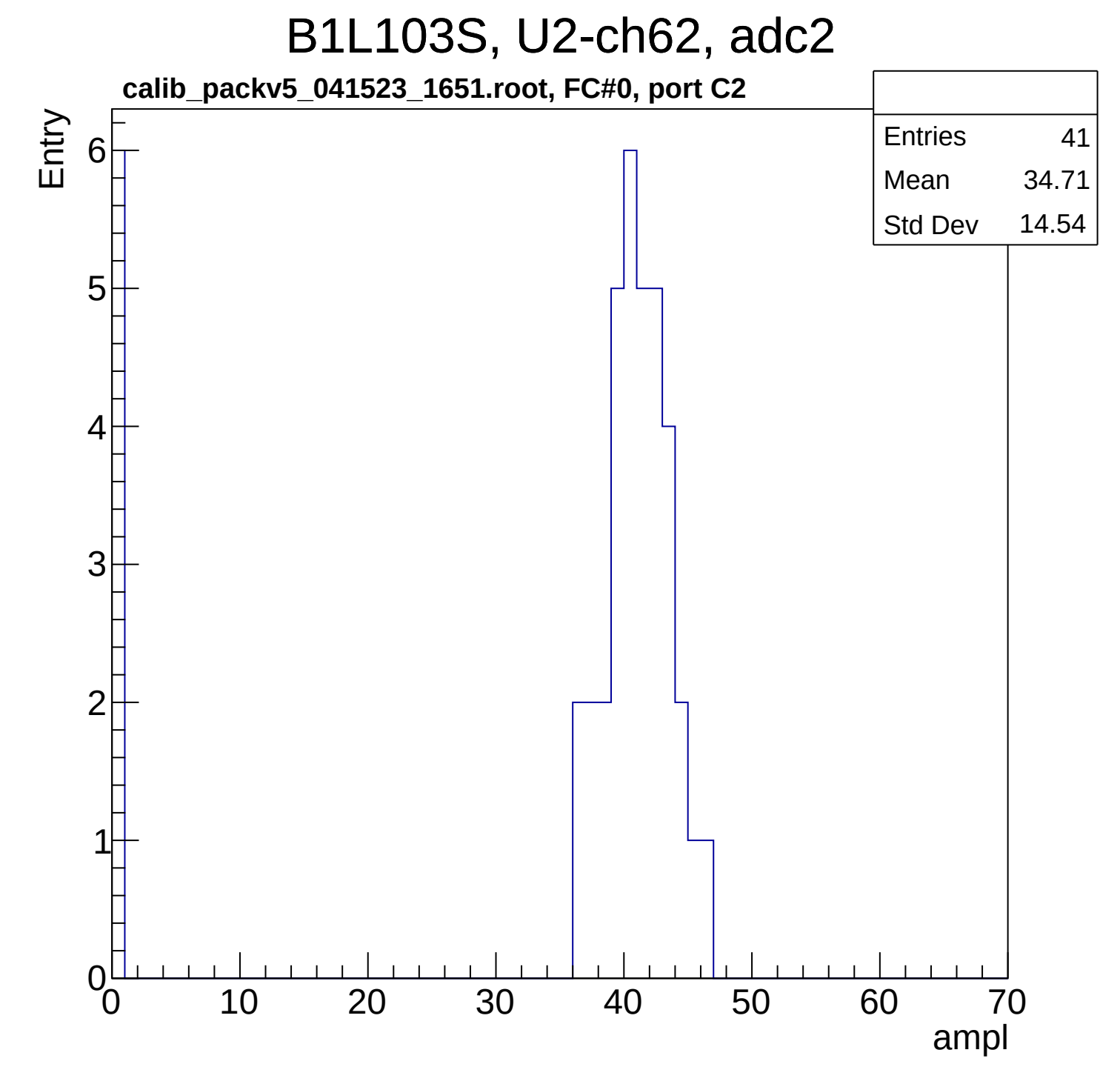

B1L103S, U2-ch61, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 59.34
Std Dev 2.932
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

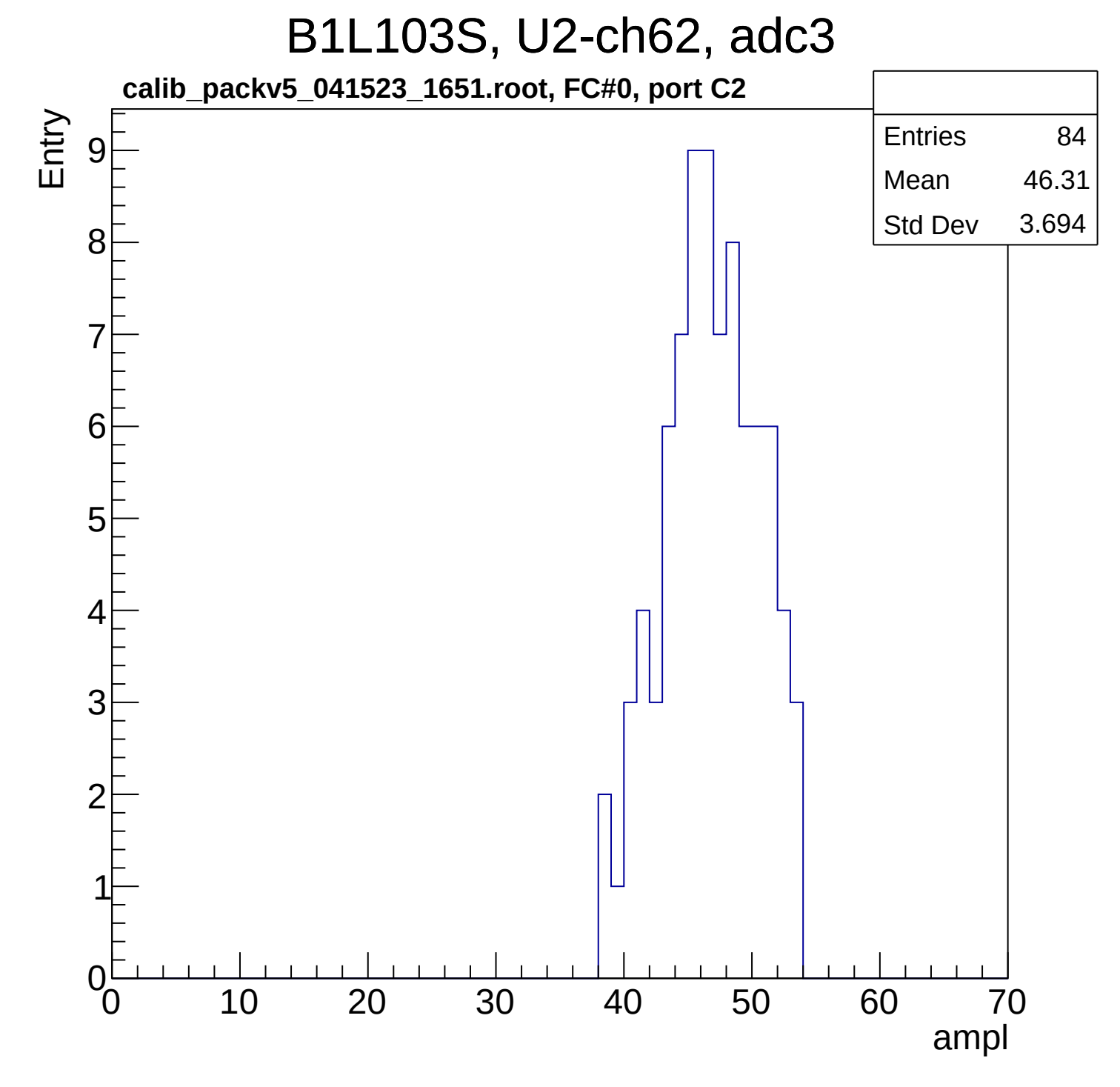

B1L103S, U2-ch61, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 54.5
Std Dev 18.3
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

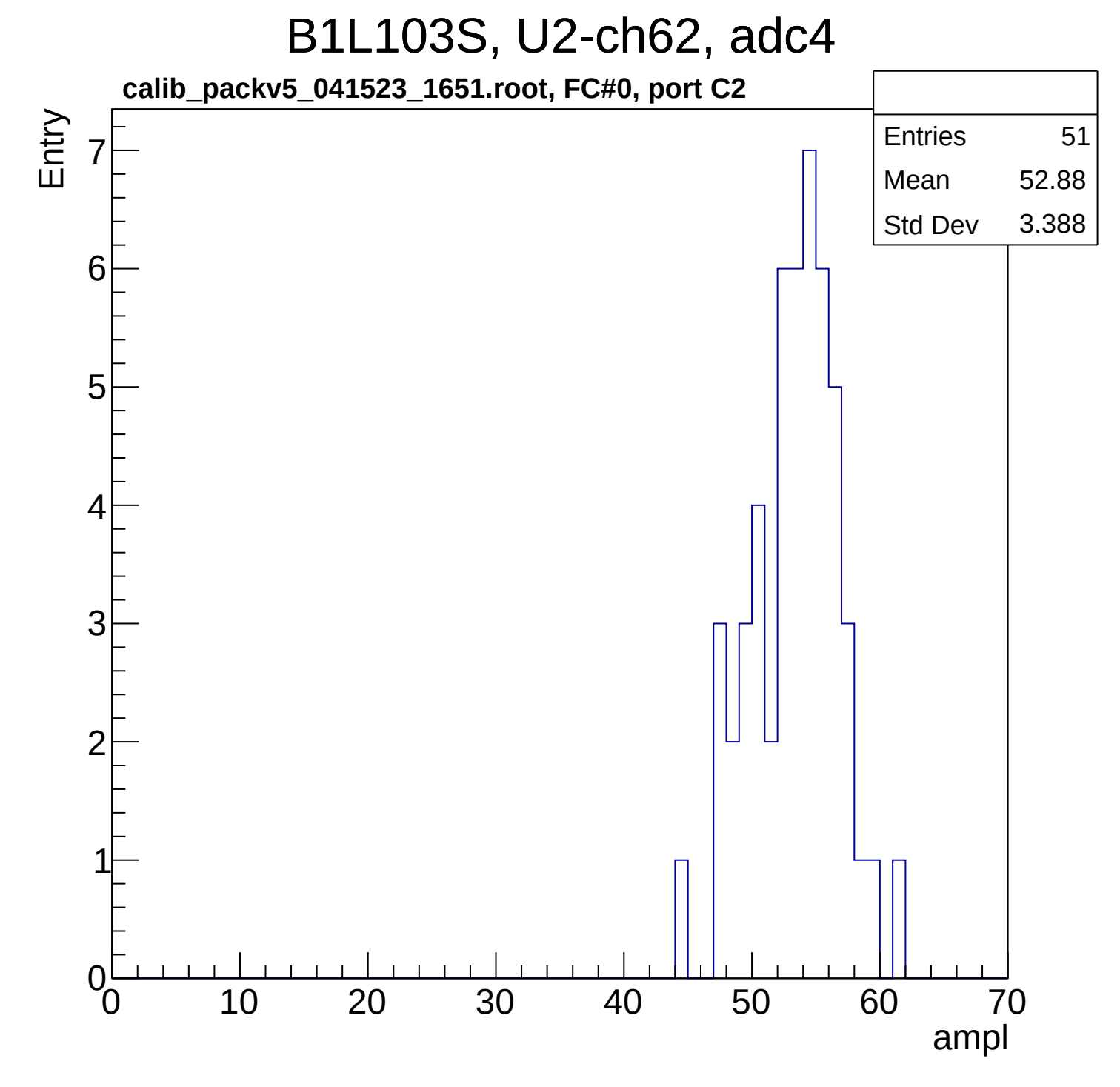

B1L103S, U2-ch61, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

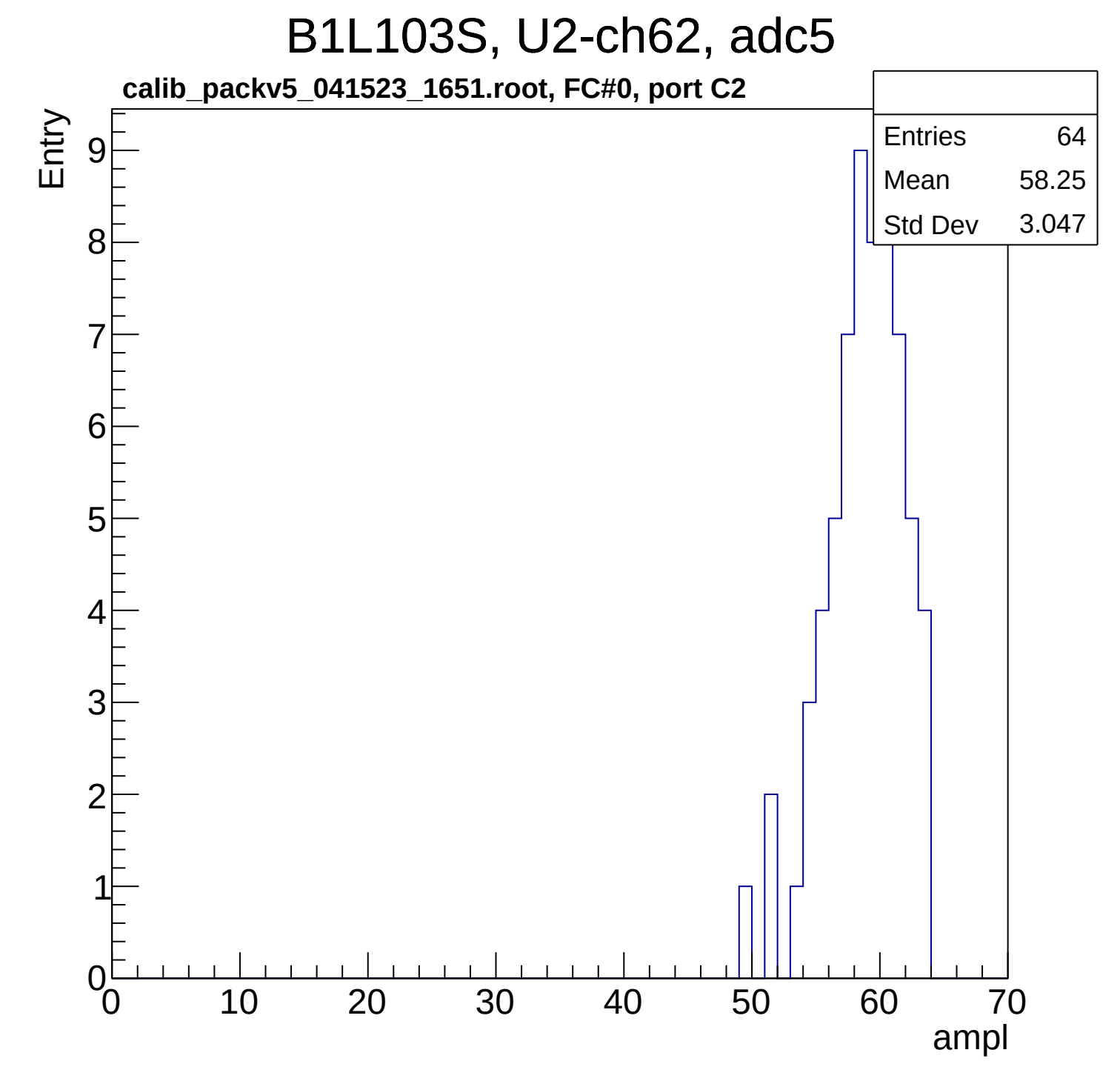

B1L103S, U2-ch62, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 25.09
Std Dev 8.971
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

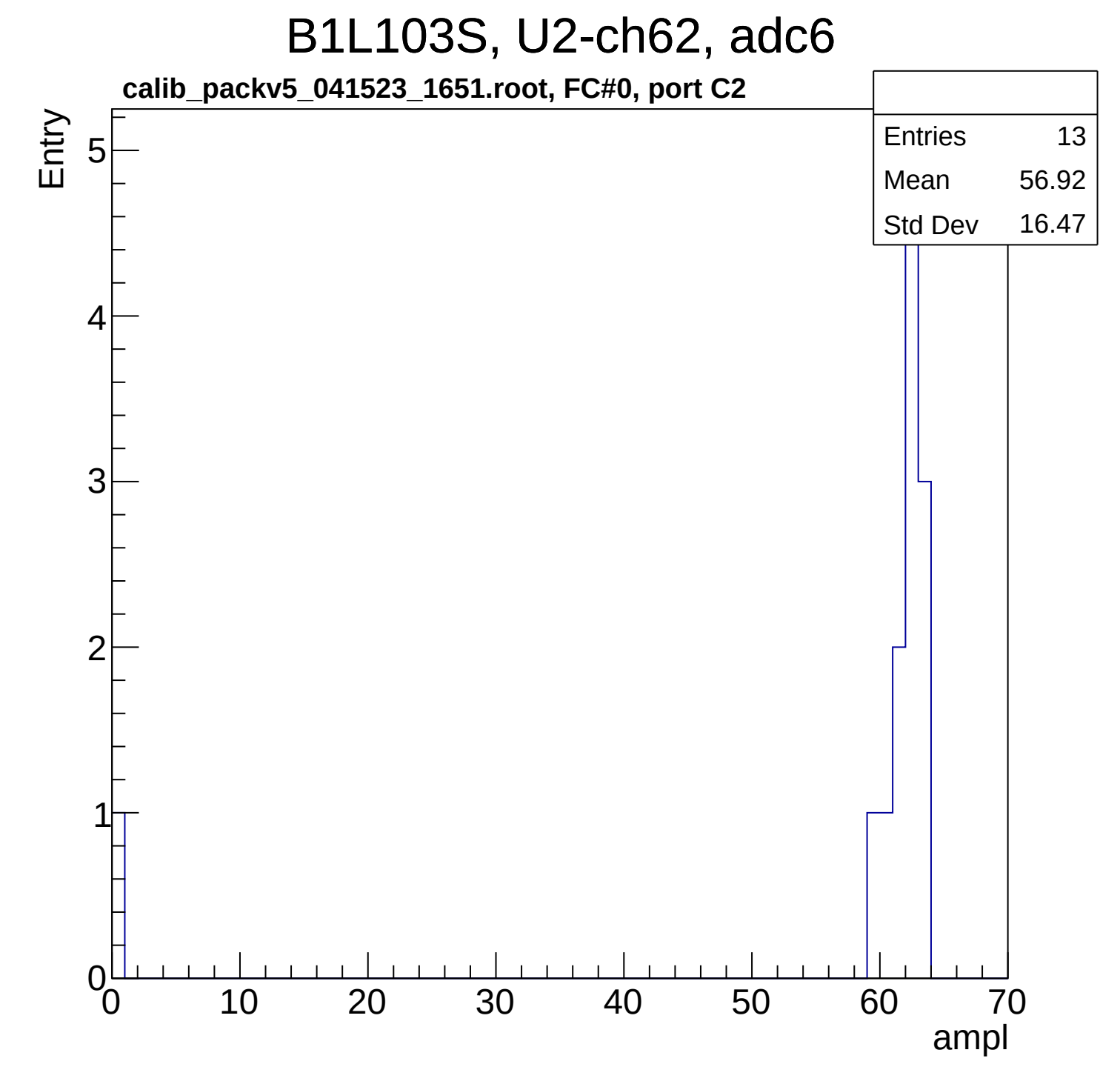

B1L103S, U2-ch62, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 31.62
Std Dev 10.72
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

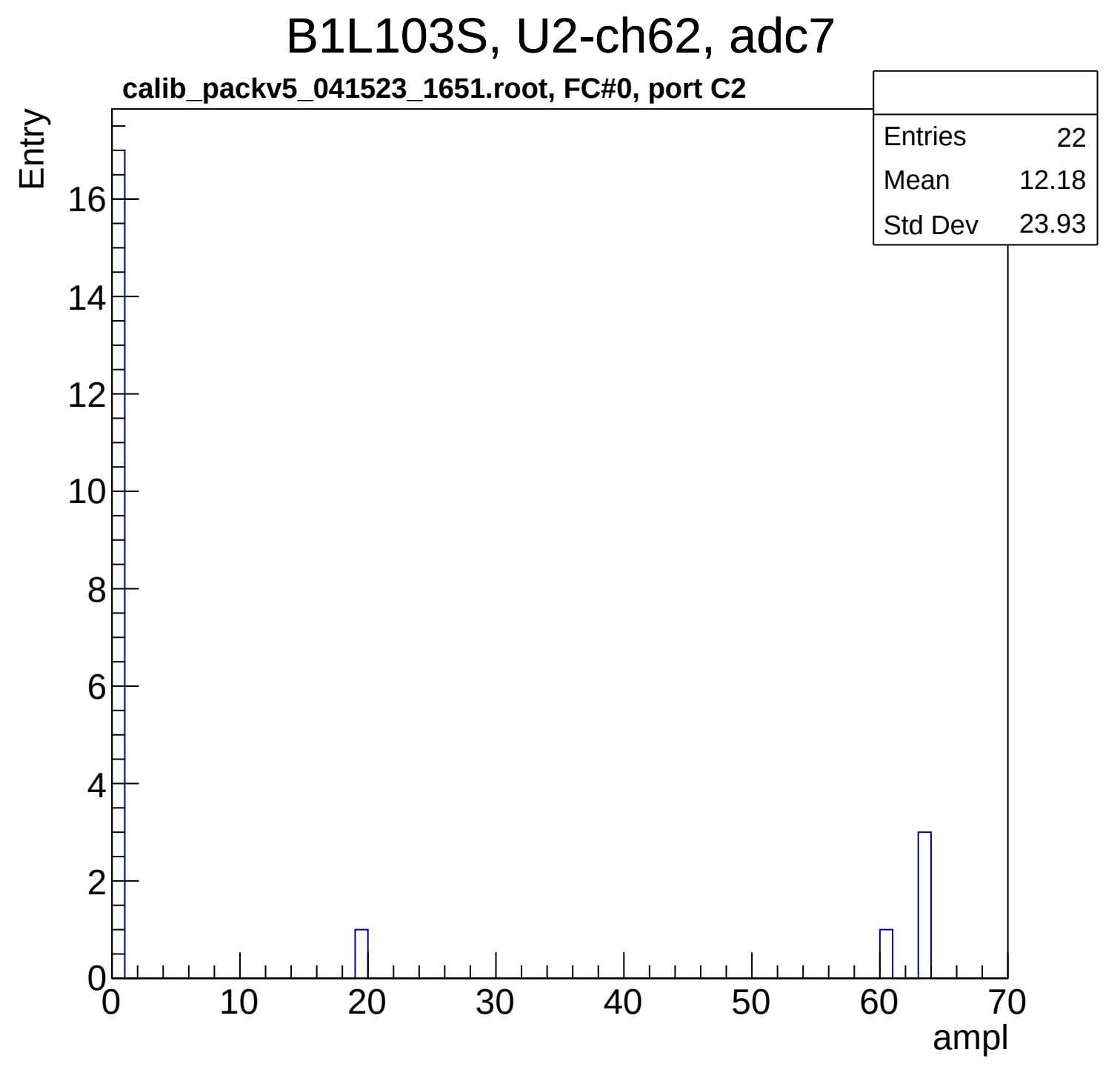

B1L103S, U2-ch62, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 34.71
Std Dev 14.54
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

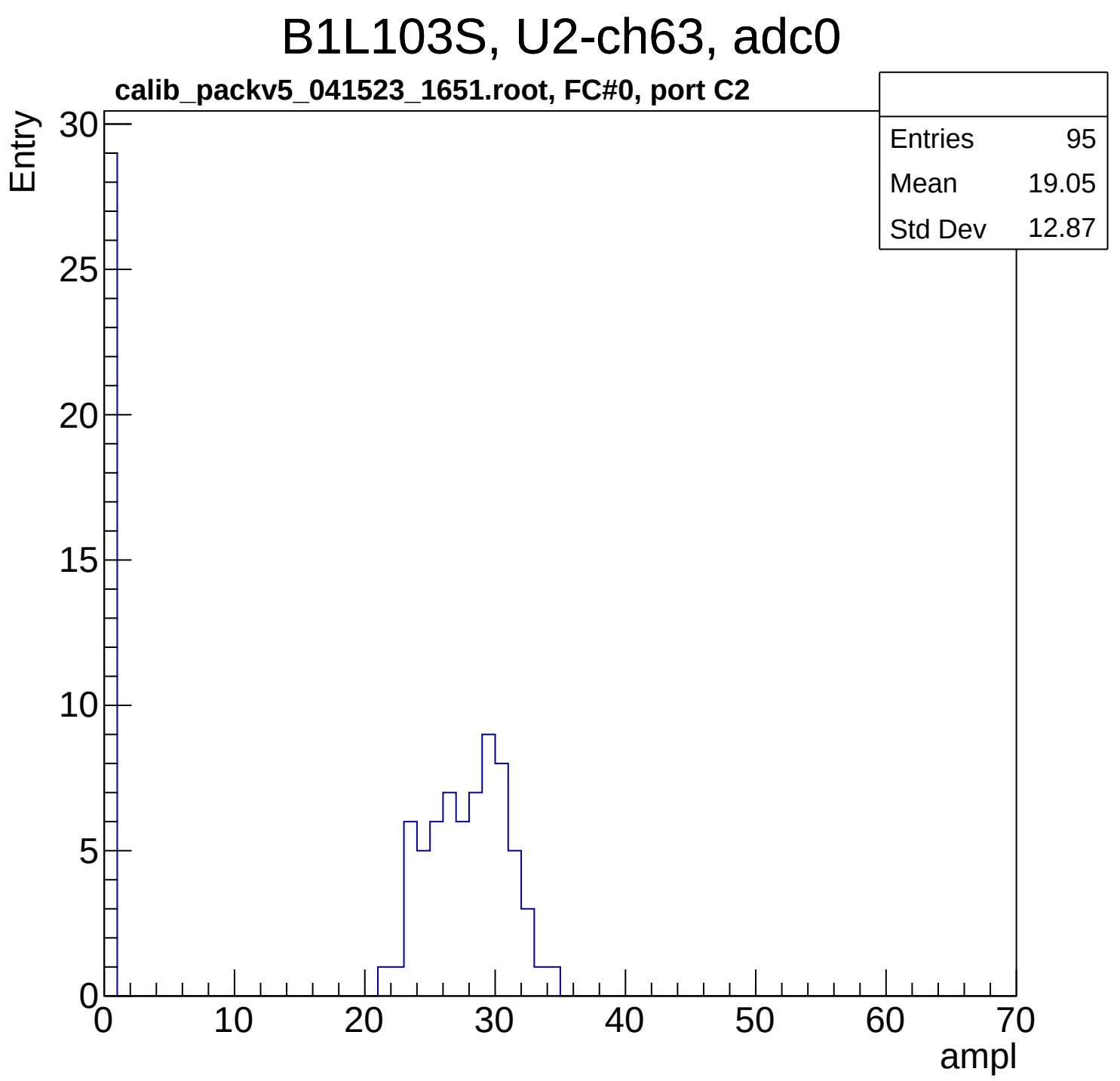

B1L103S, U2-ch62, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 46.31
Std Dev 3.694
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

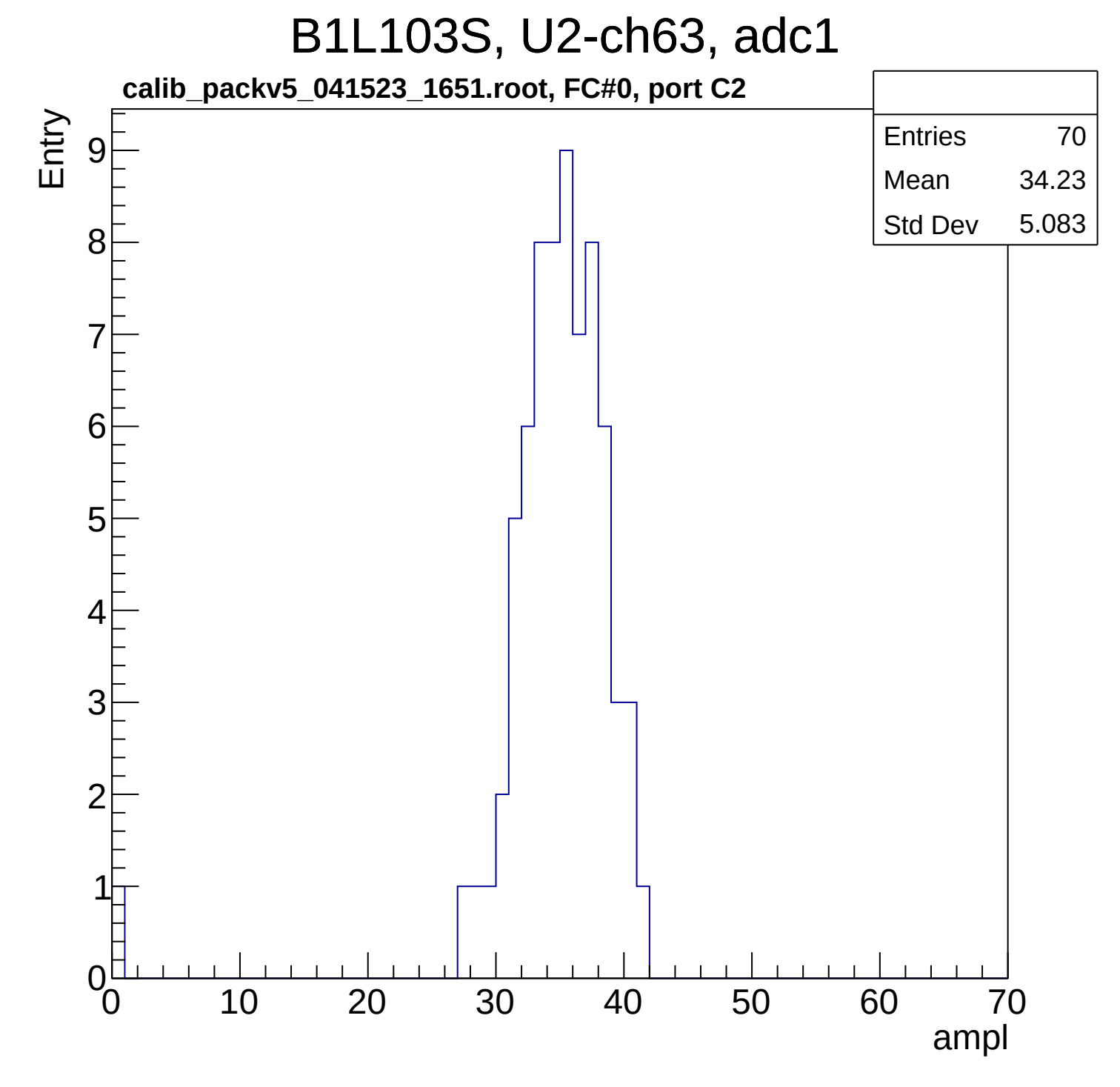

B1L103S, U2-ch62, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 52.88
Std Dev 3.388
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

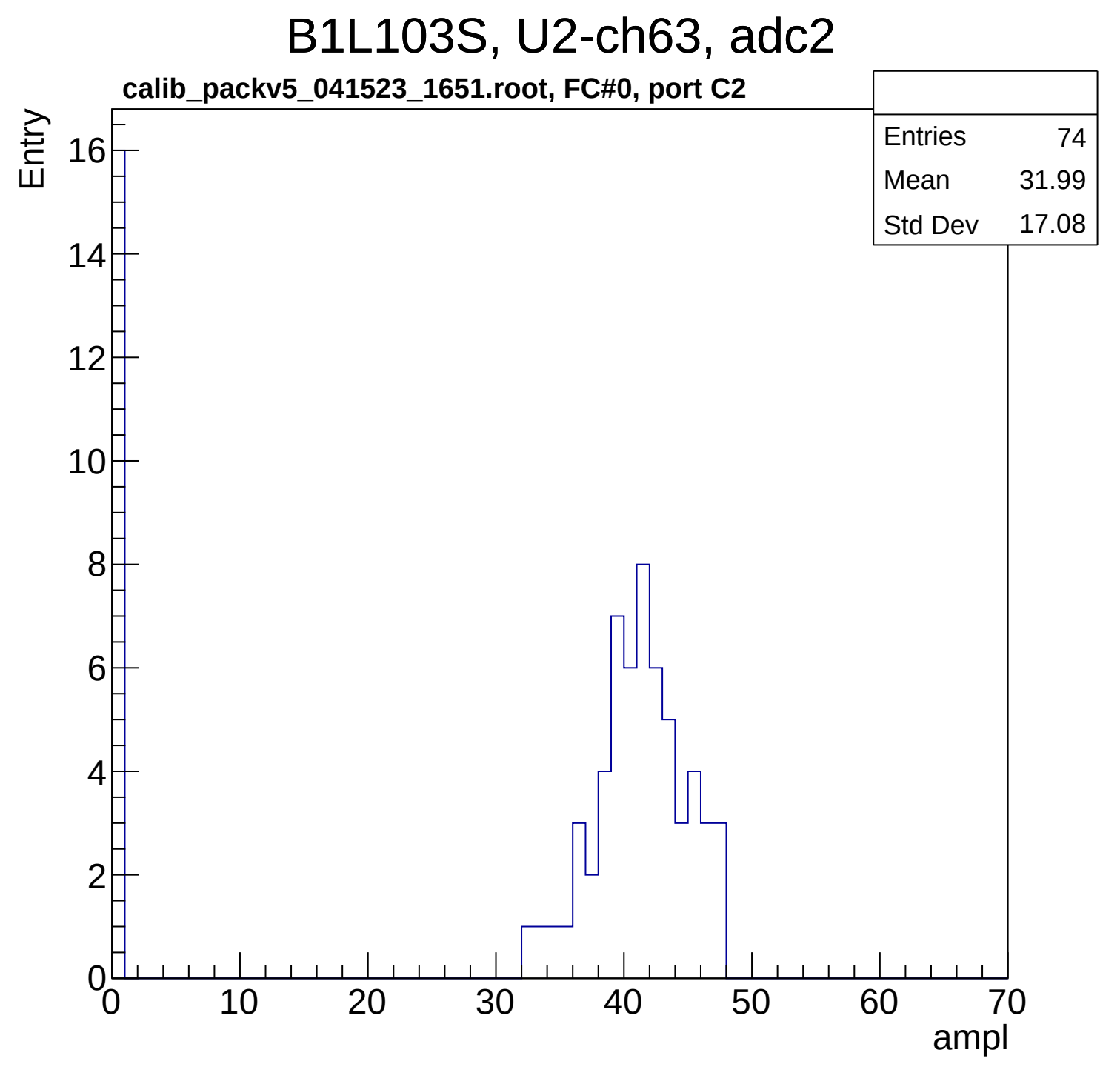

B1L103S, U2-ch62, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 58.25
Std Dev 3.047
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

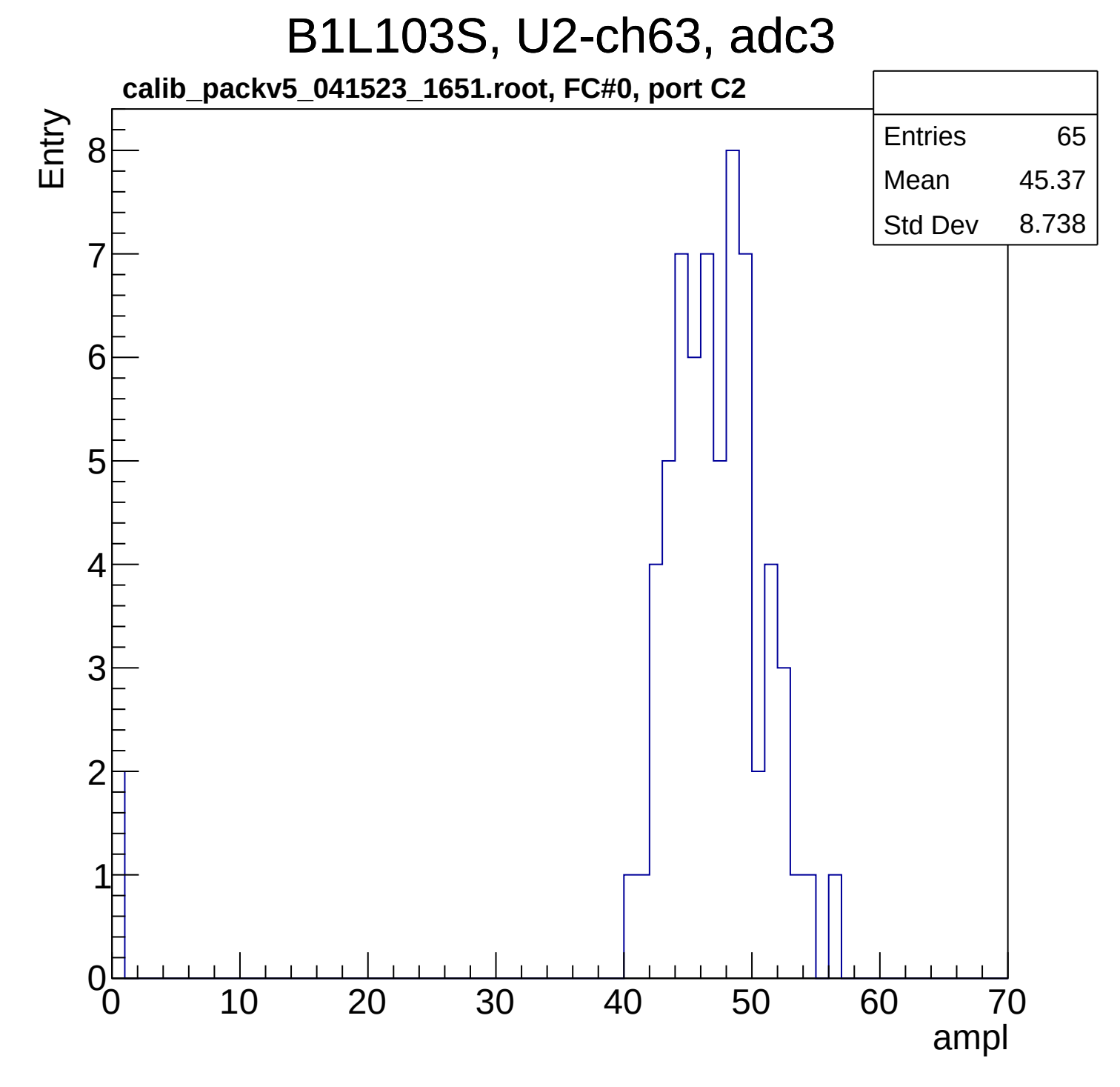

B1L103S, U2-ch62, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 56.92
Std Dev 16.47
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

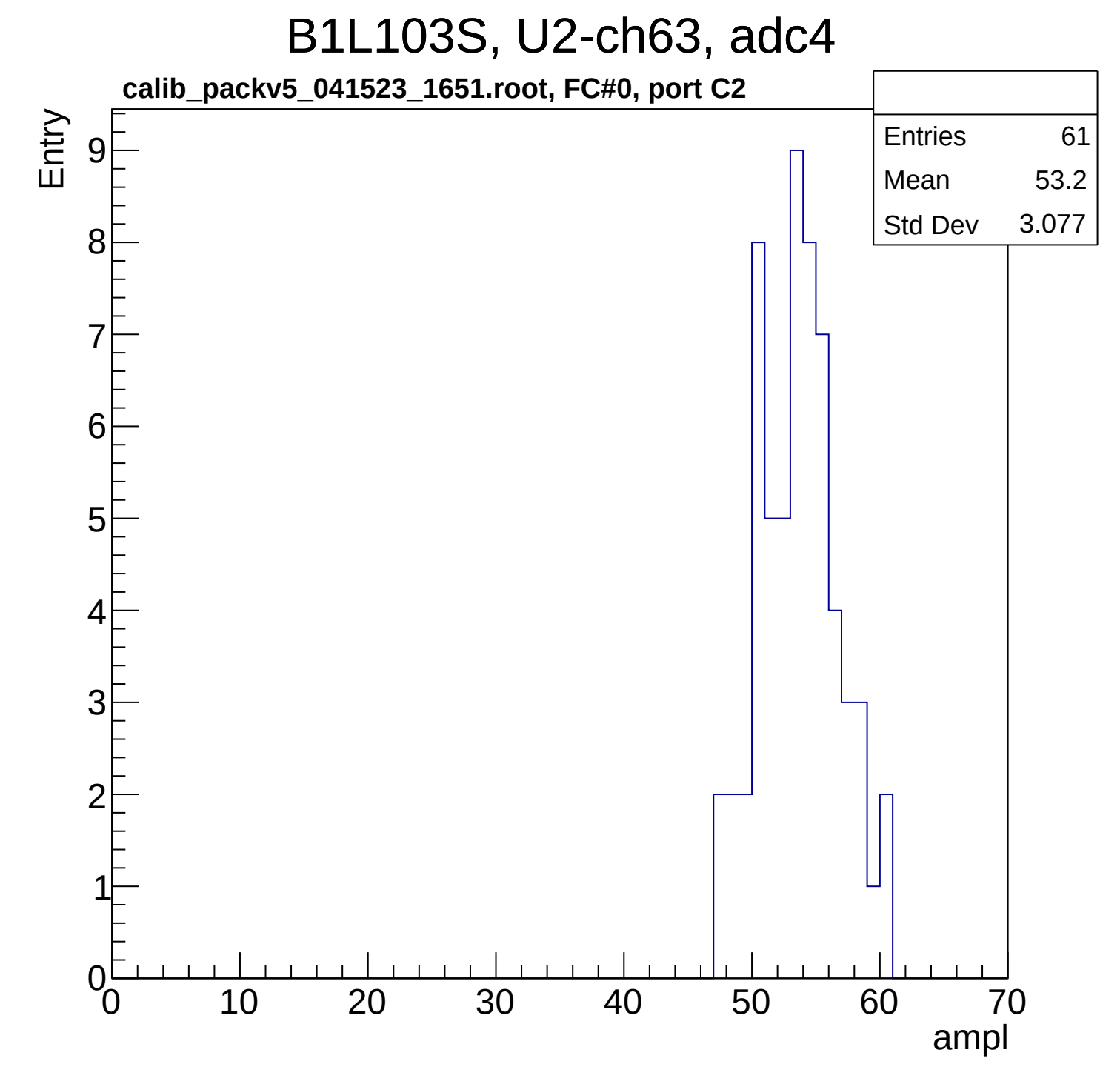

B1L103S, U2-ch62, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 12.18
Std Dev 23.93
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

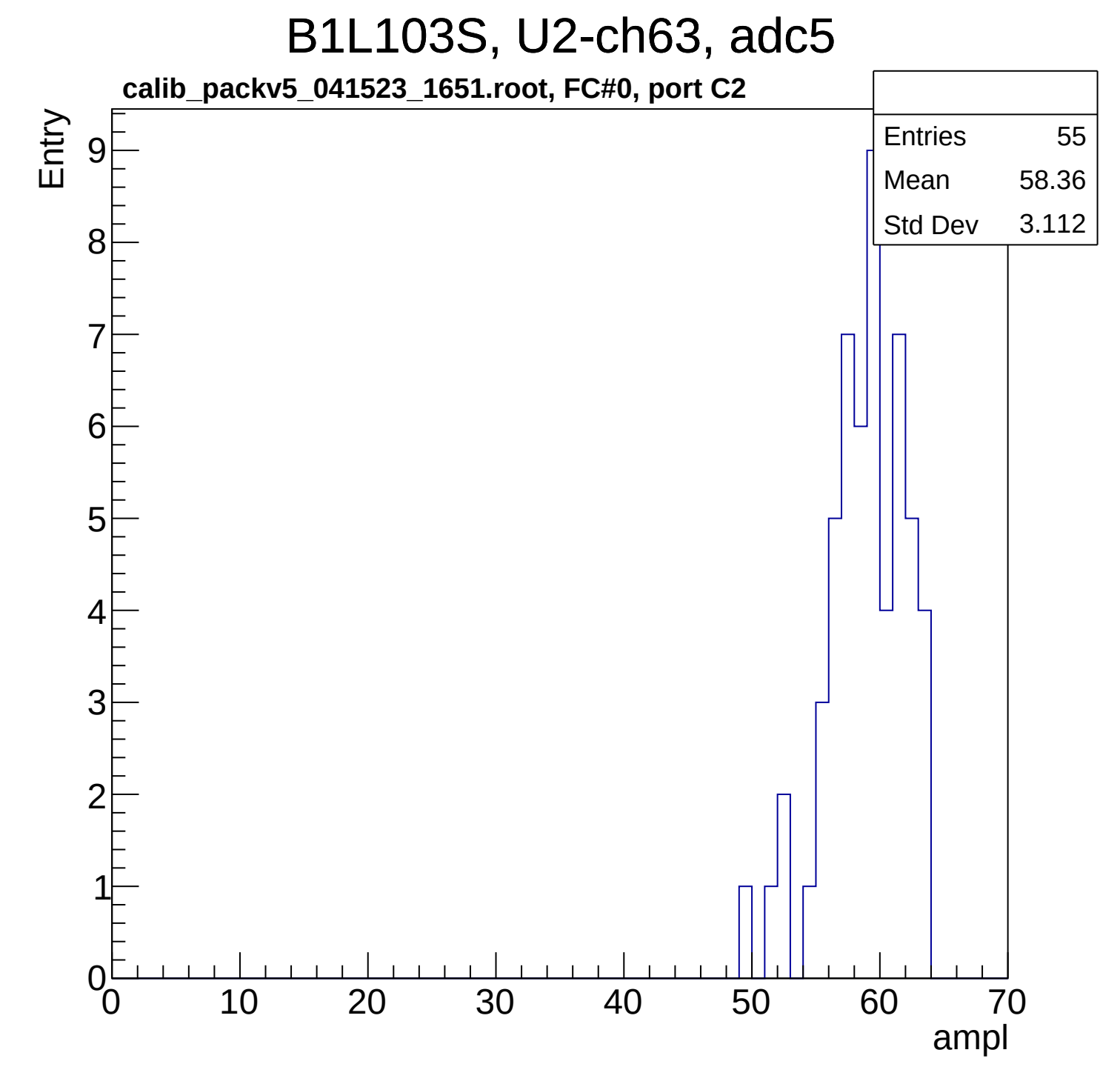

B1L103S, U2-ch63, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 19.05
Std Dev 12.87
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70

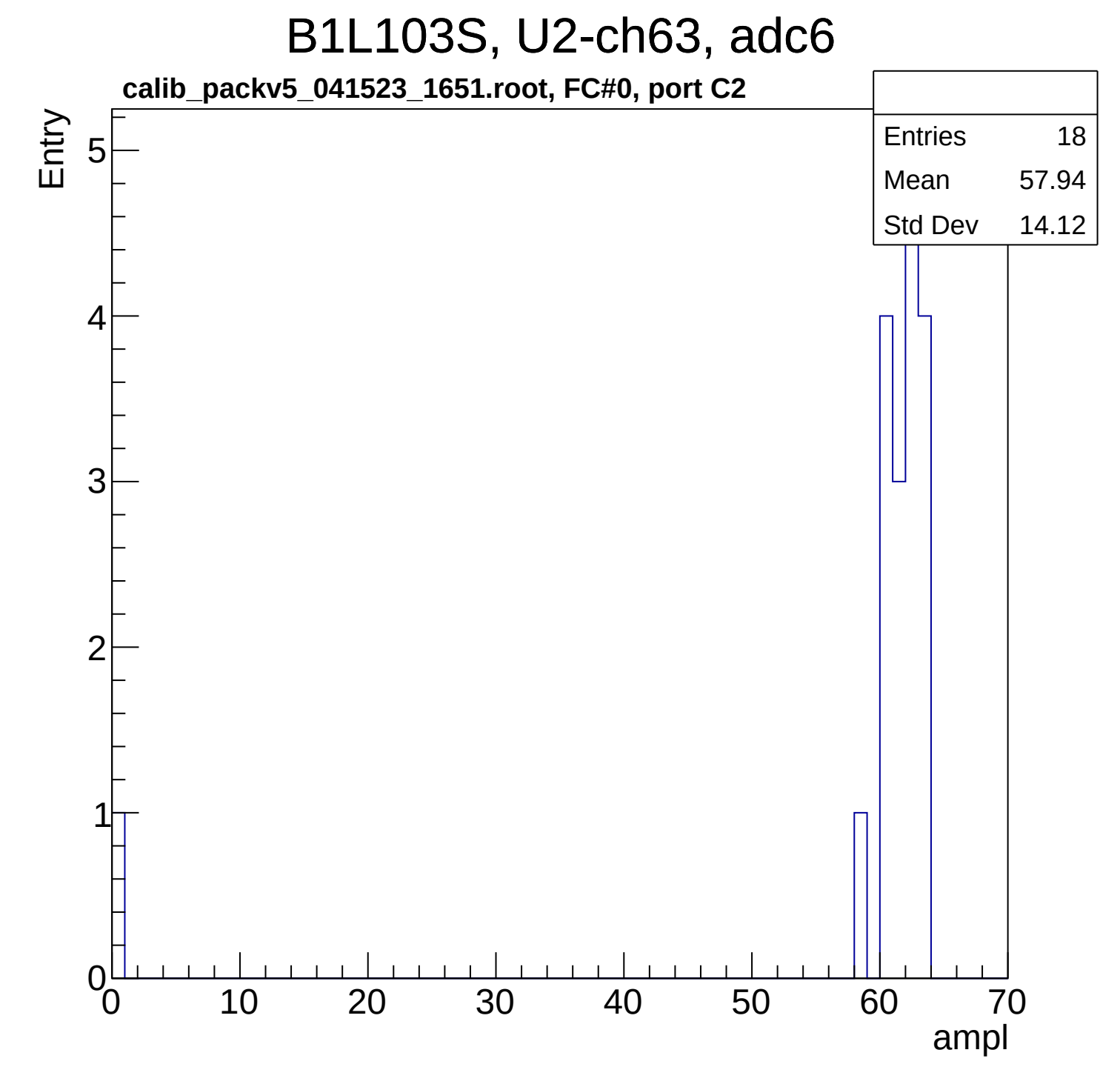

B1L103S, U2-ch63, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 34.23
Std Dev 5.083
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

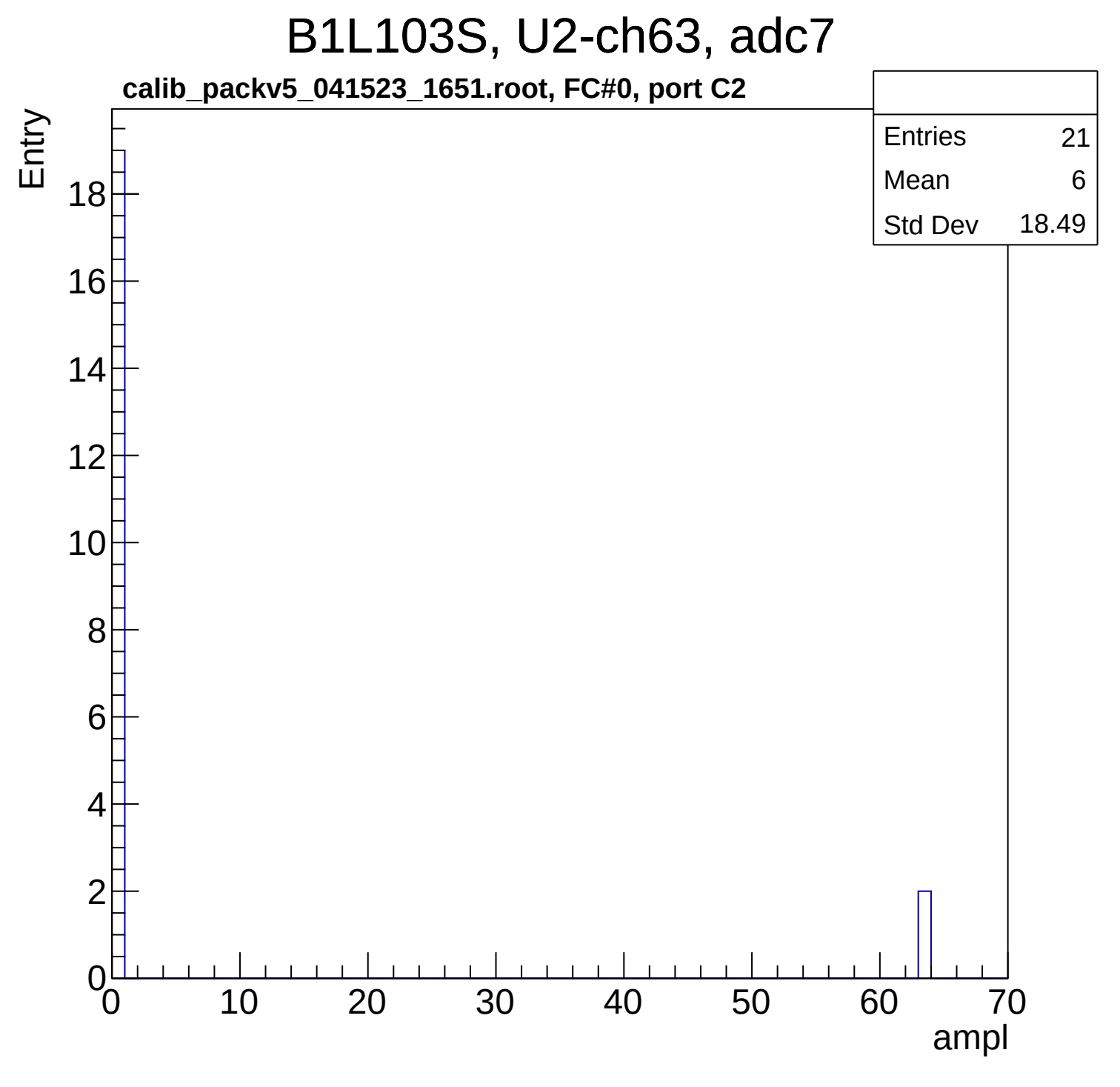

B1L103S, U2-ch63, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 31.99
Std Dev 17.08
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

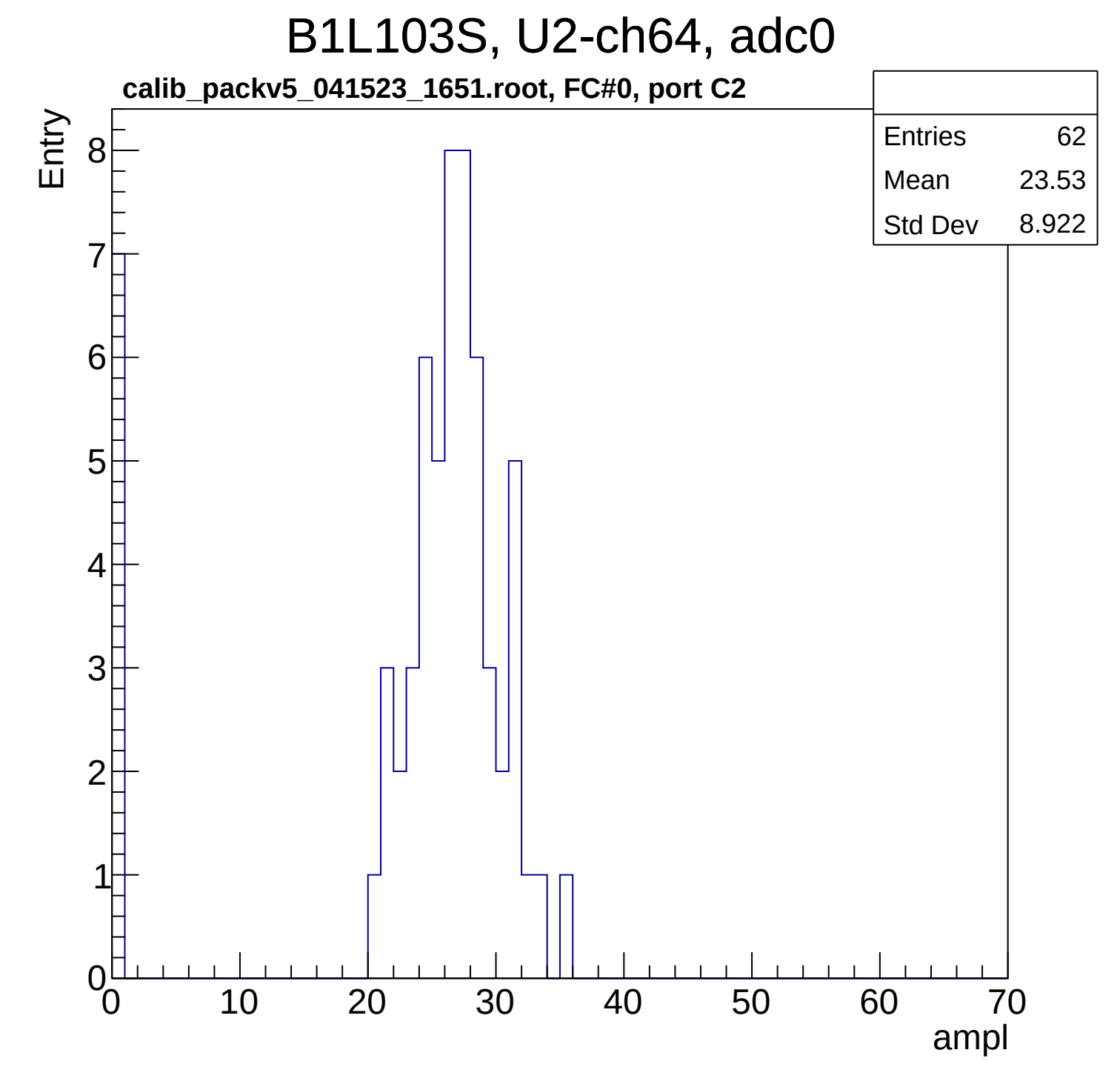

B1L103S, U2-ch63, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 45.37
Std Dev 8.738
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

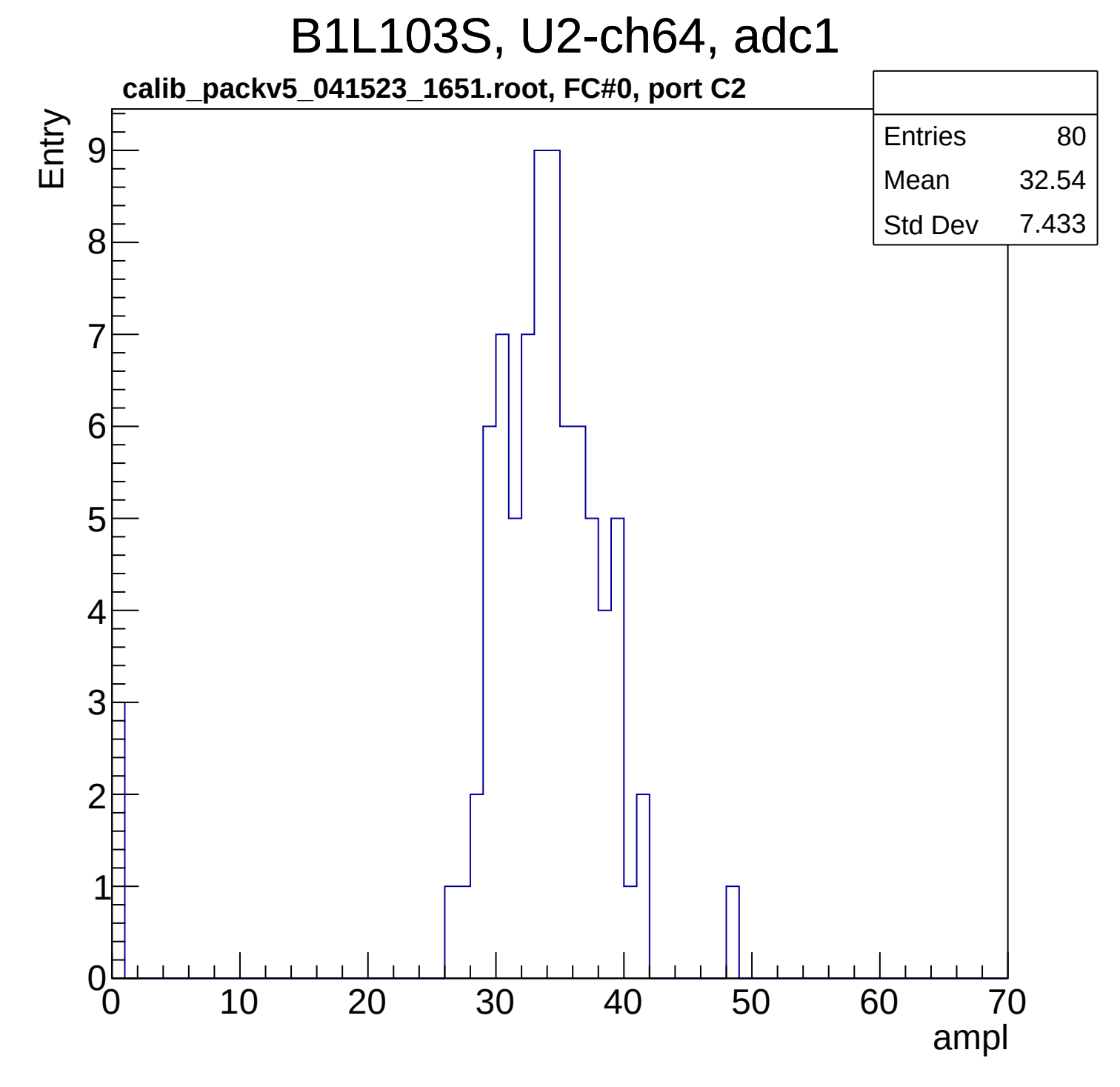

B1L103S, U2-ch63, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 53.2
Std Dev 3.077
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

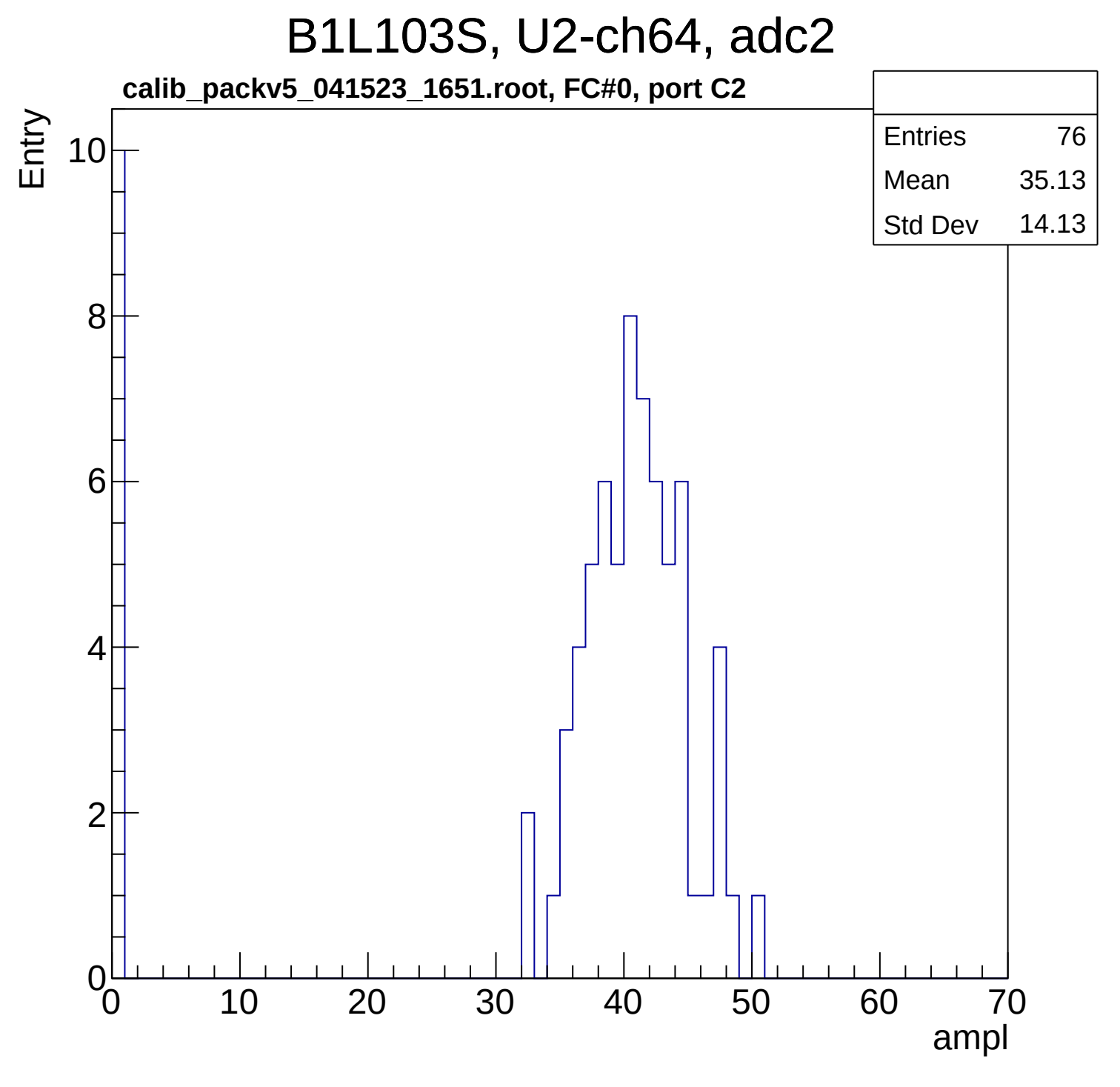

B1L103S, U2-ch63, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.36
Std Dev 3.112
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

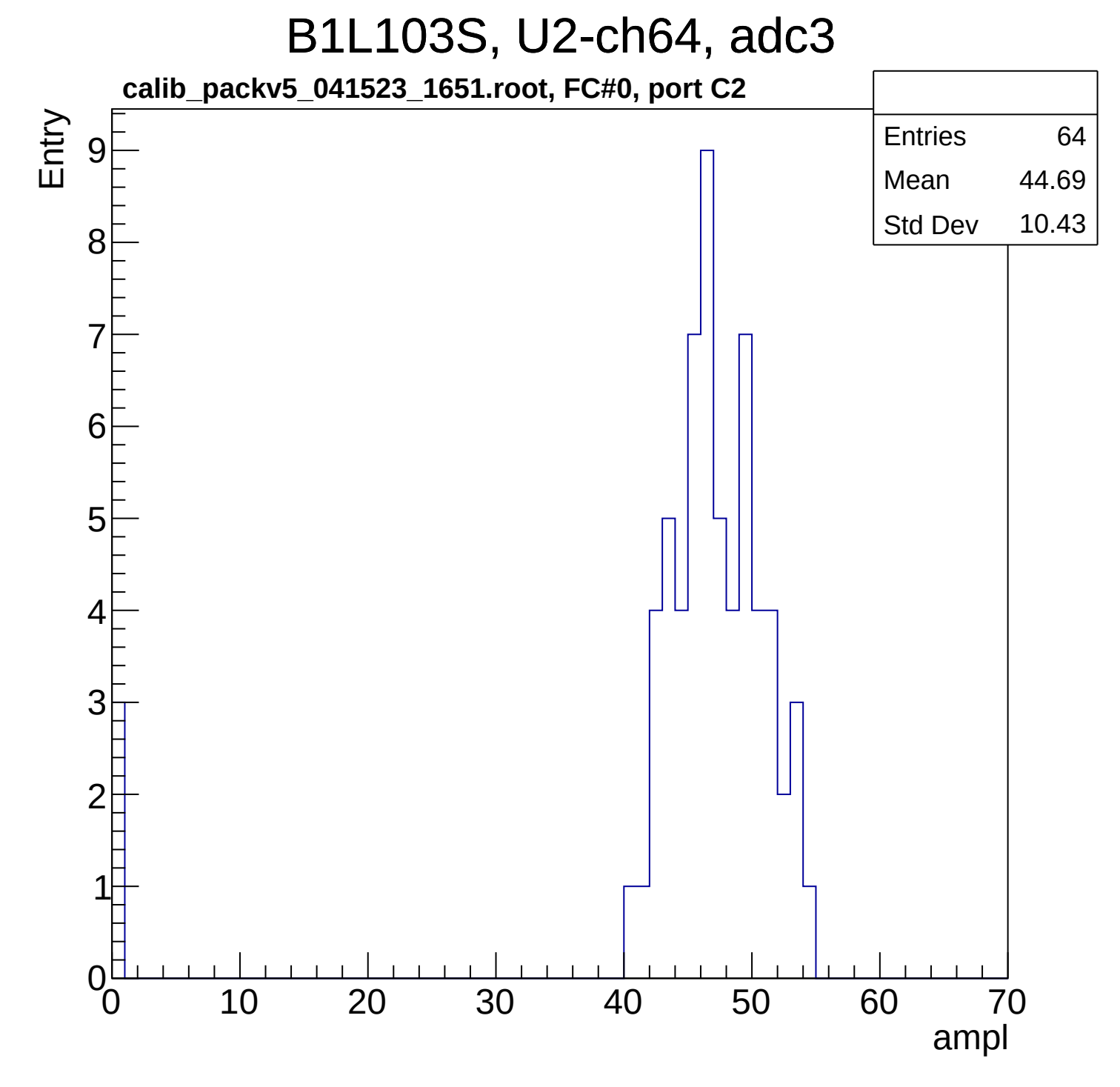

B1L103S, U2-ch63, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 57.94
Std Dev 14.12
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

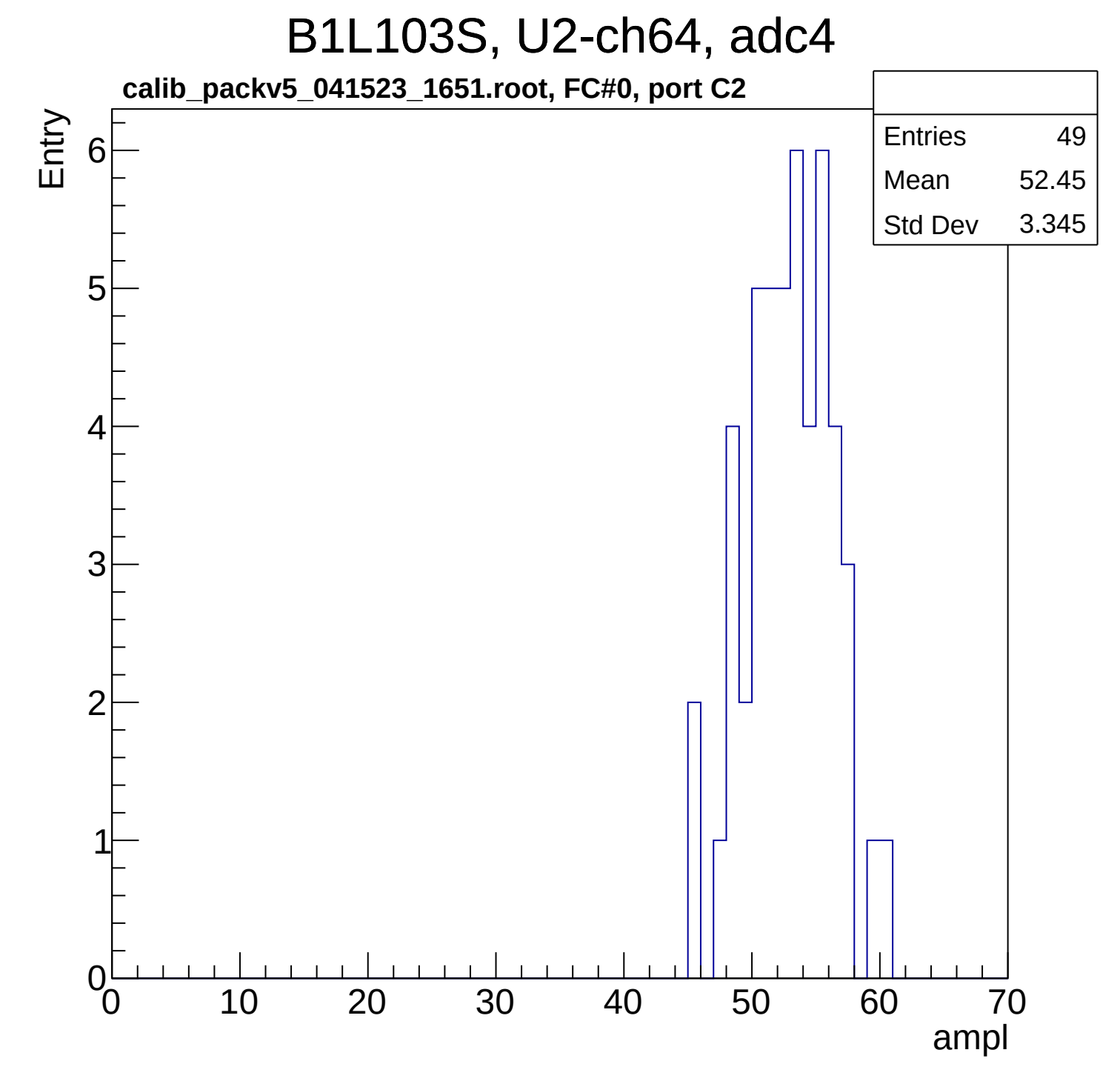

B1L103S, U2-ch63, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

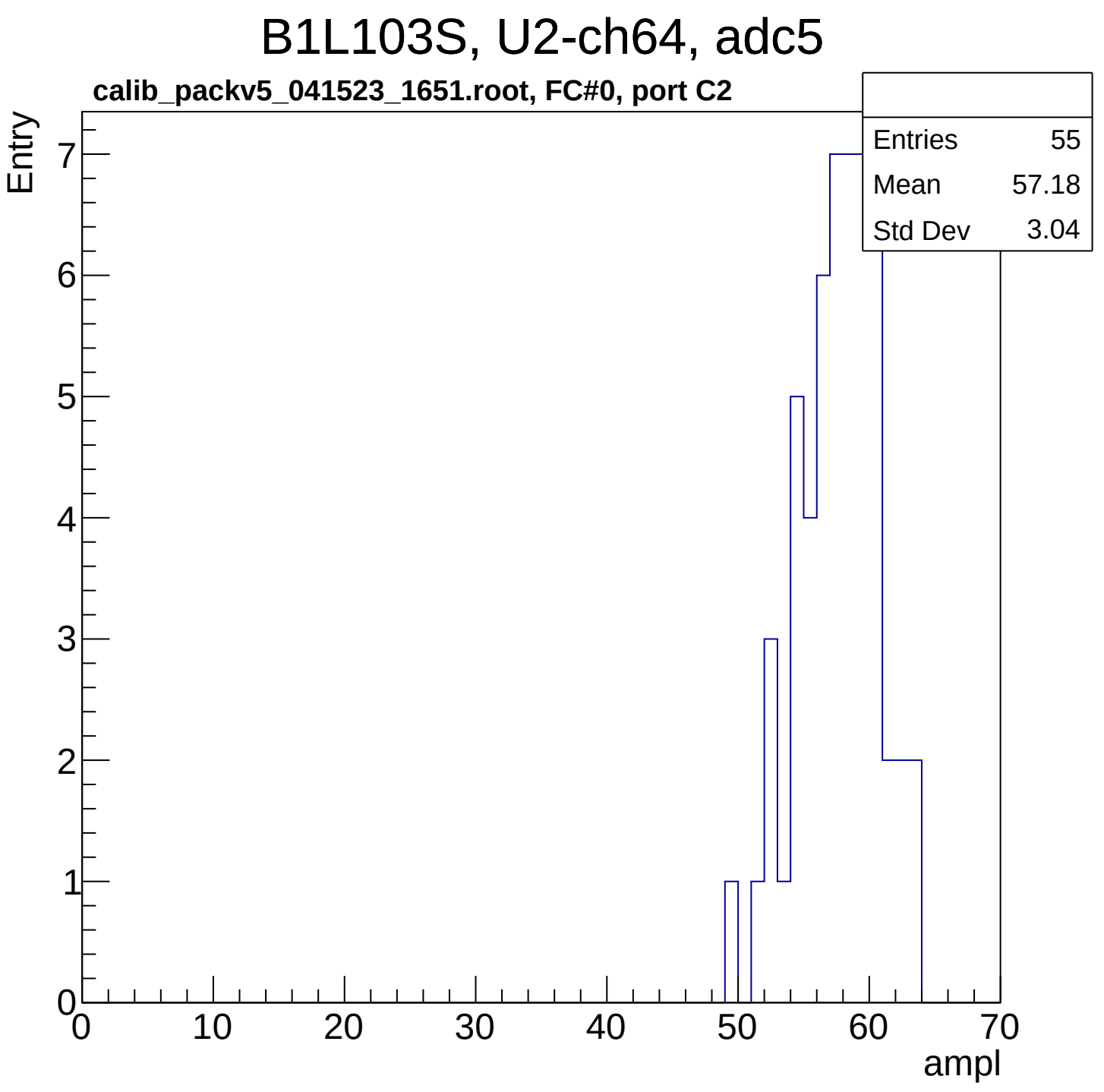

B1L103S, U2-ch64, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 23.53
Std Dev 8.922
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

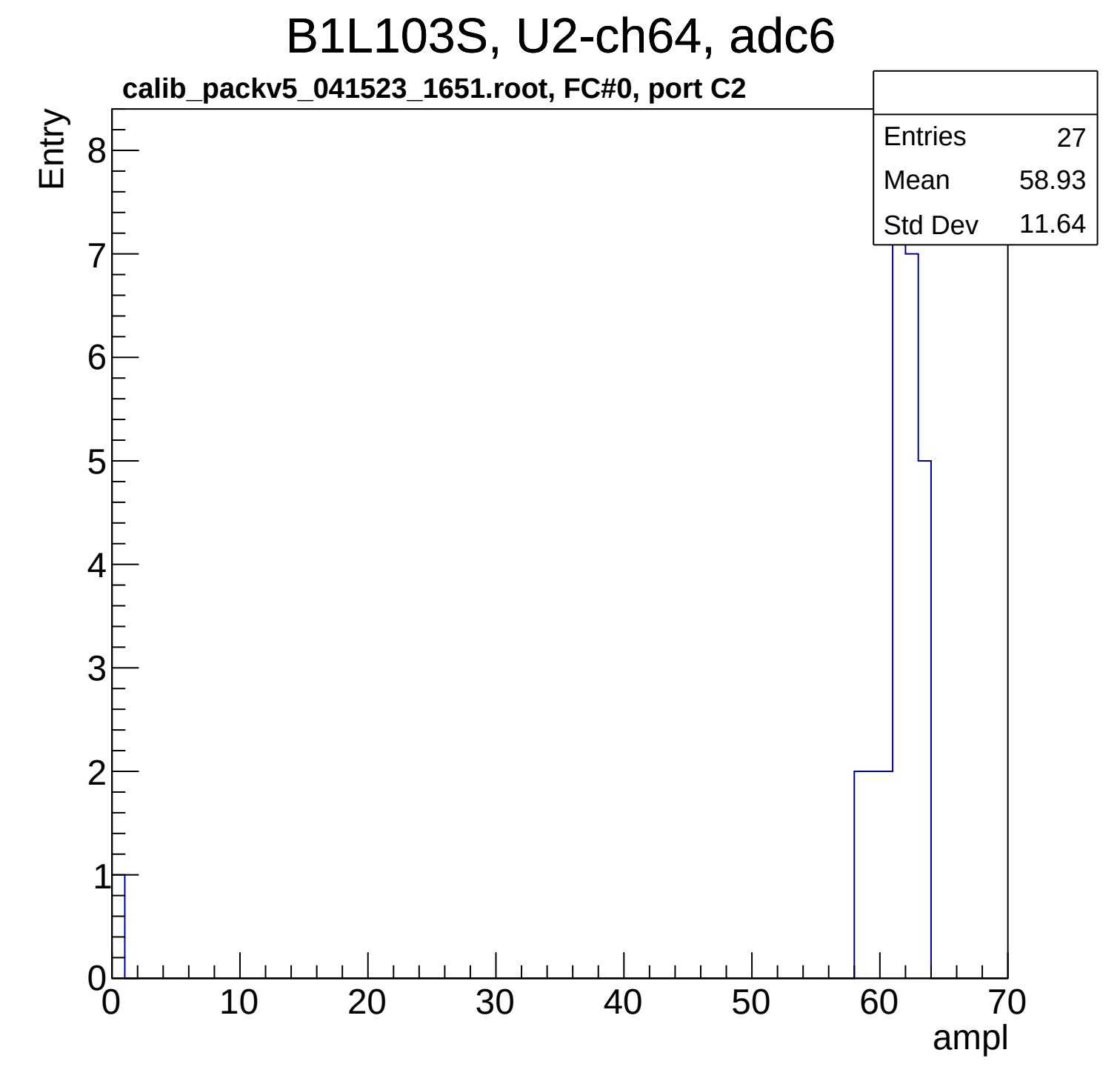

B1L103S, U2-ch64, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 32.54
Std Dev 7.433
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

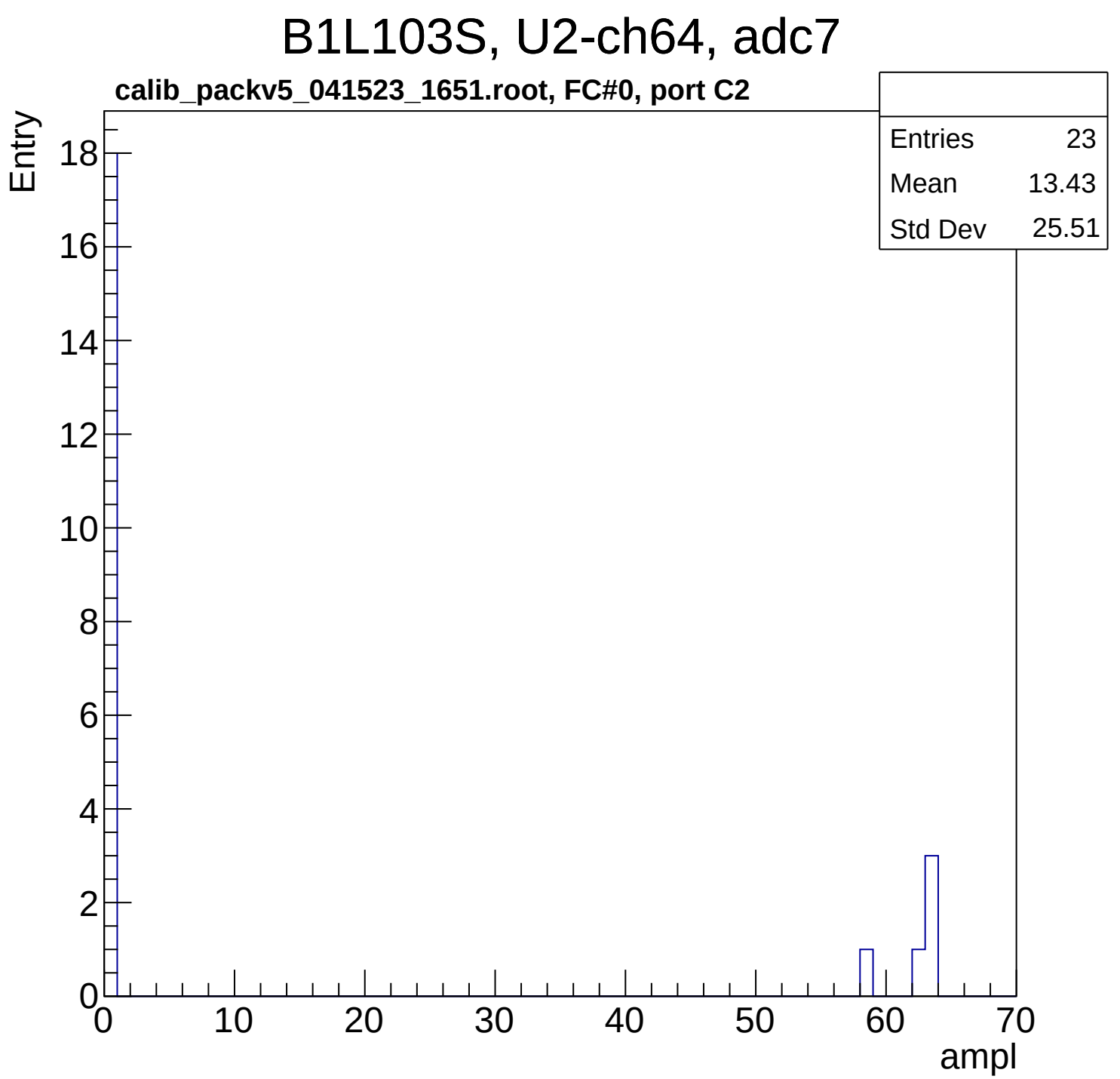

B1L103S, U2-ch64, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 35.13
Std Dev 14.13
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

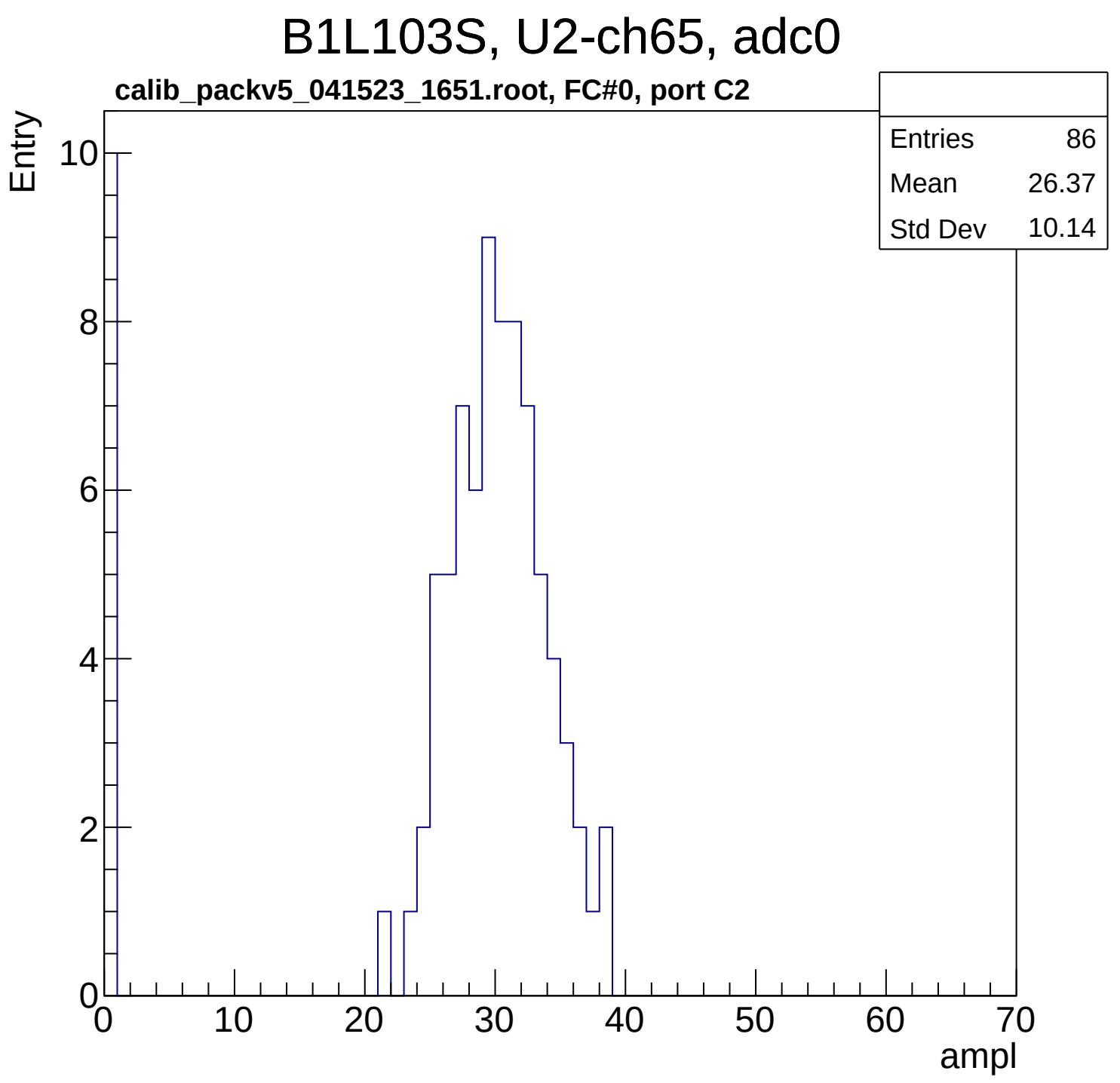

B1L103S, U2-ch64, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 44.69
Std Dev 10.43
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

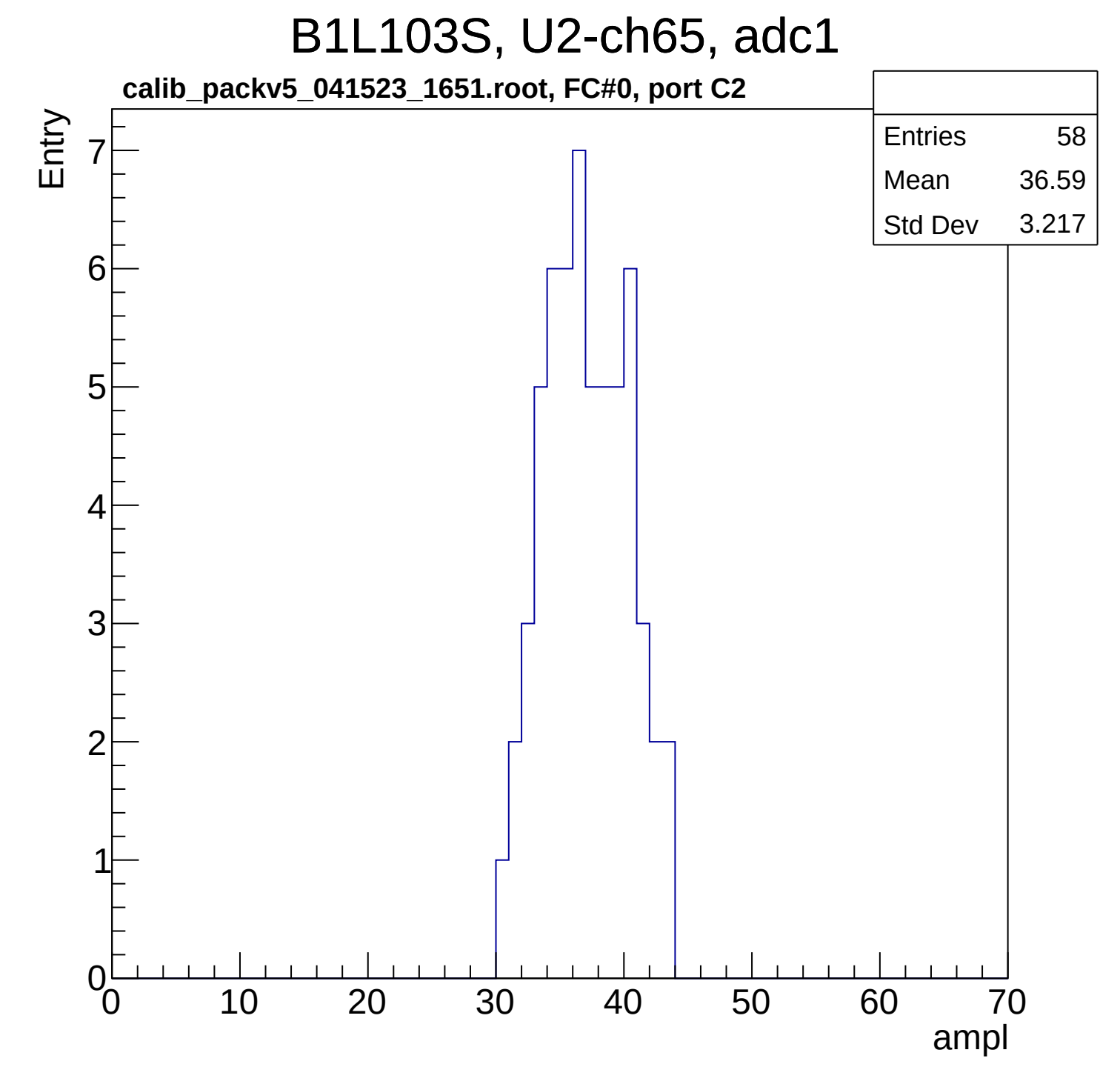

B1L103S, U2-ch64, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 52.45
Std Dev 3.345
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

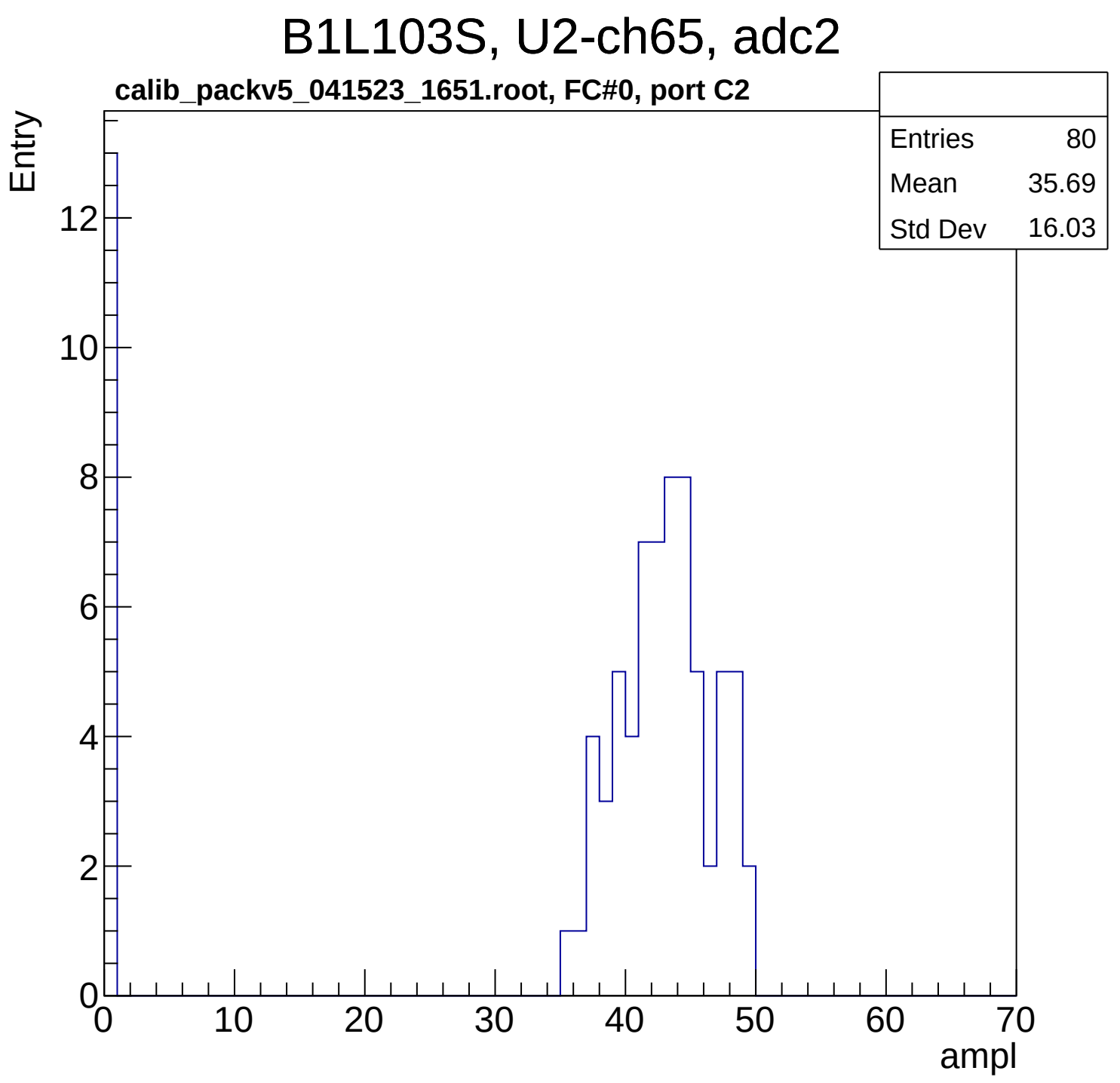

B1L103S, U2-ch64, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.18
Std Dev 3.04
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

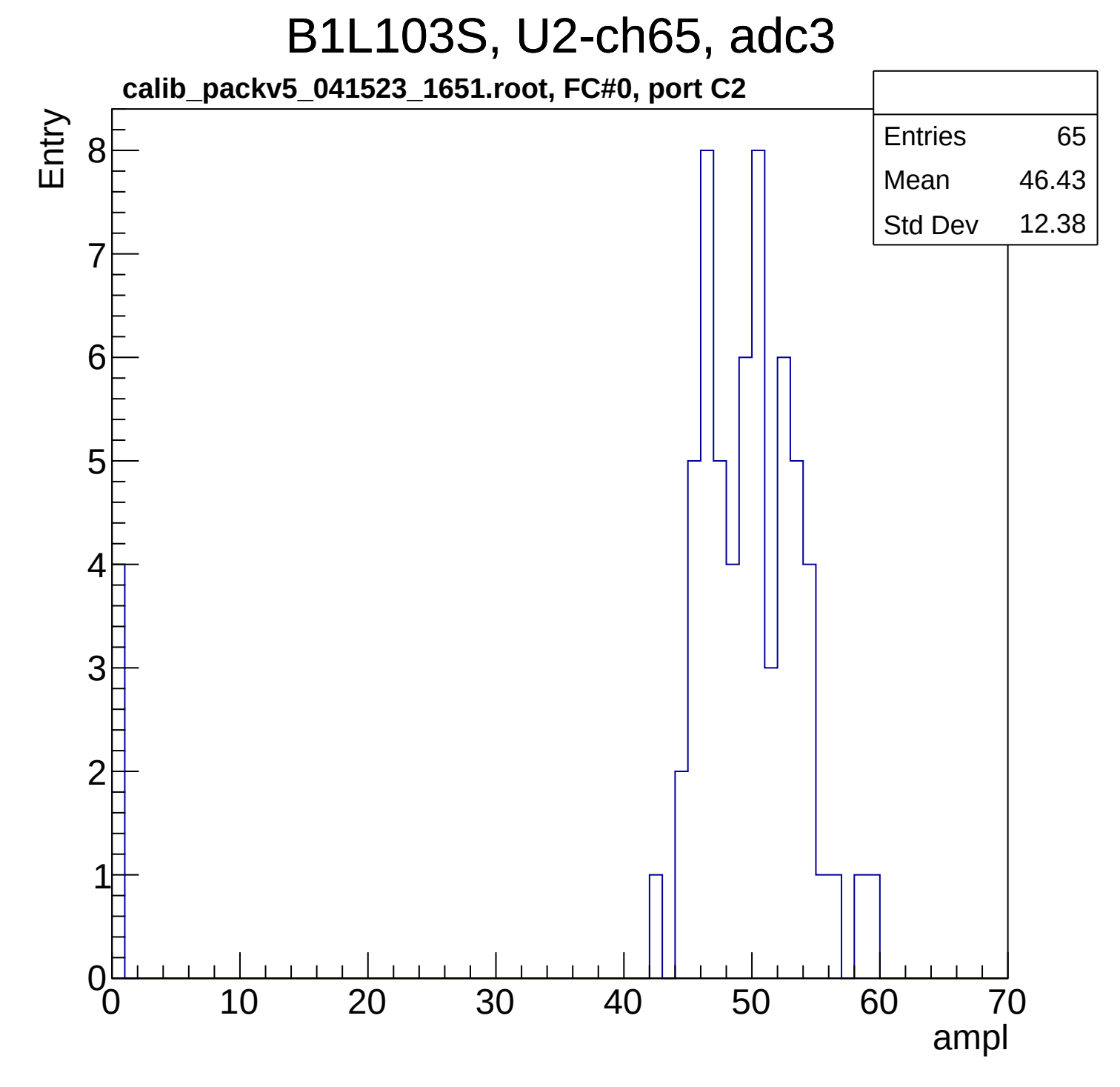

B1L103S, U2-ch64, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 58.93
Std Dev 11.64
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

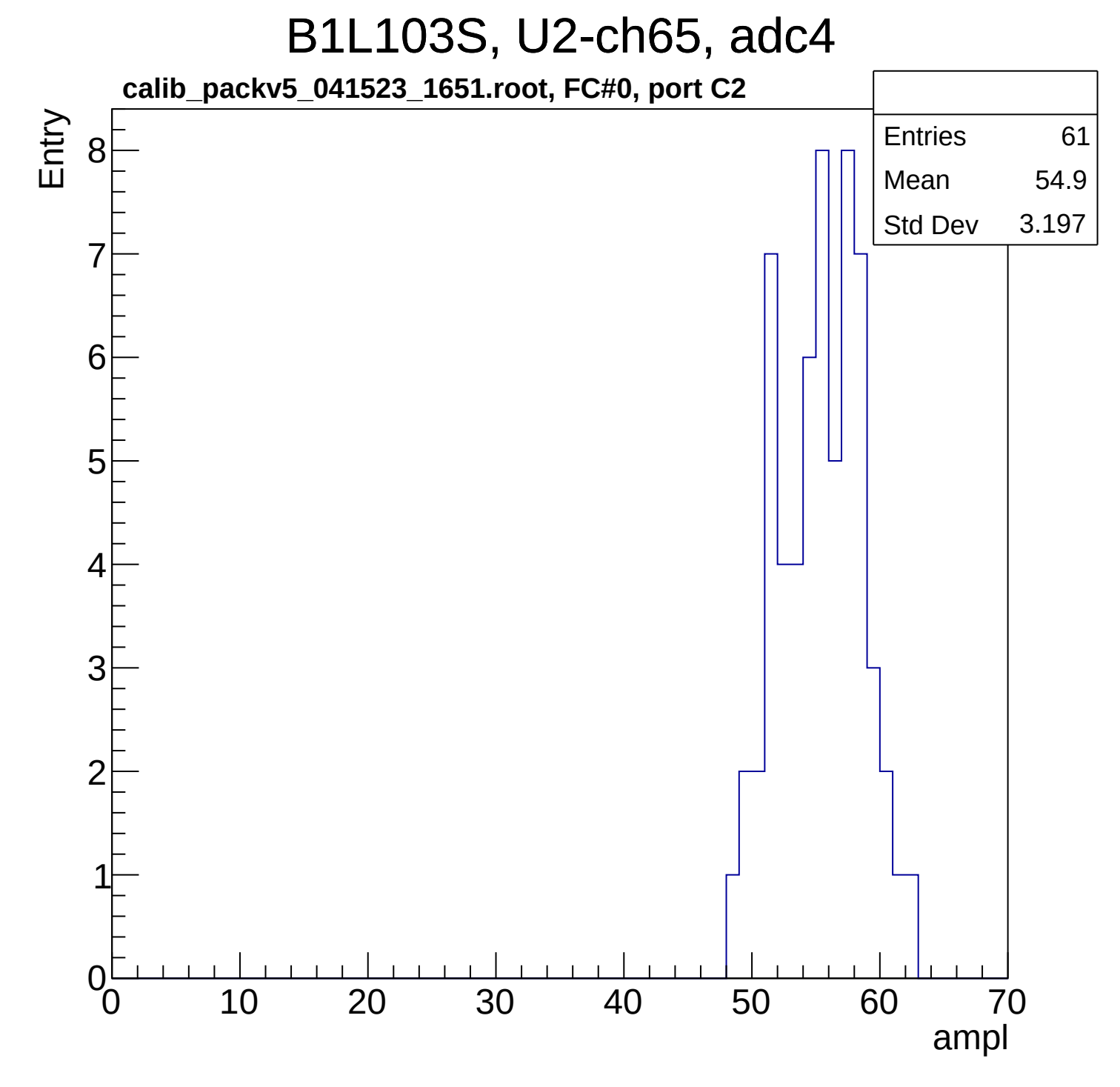

B1L103S, U2-ch64, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 13.43
Std Dev 25.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

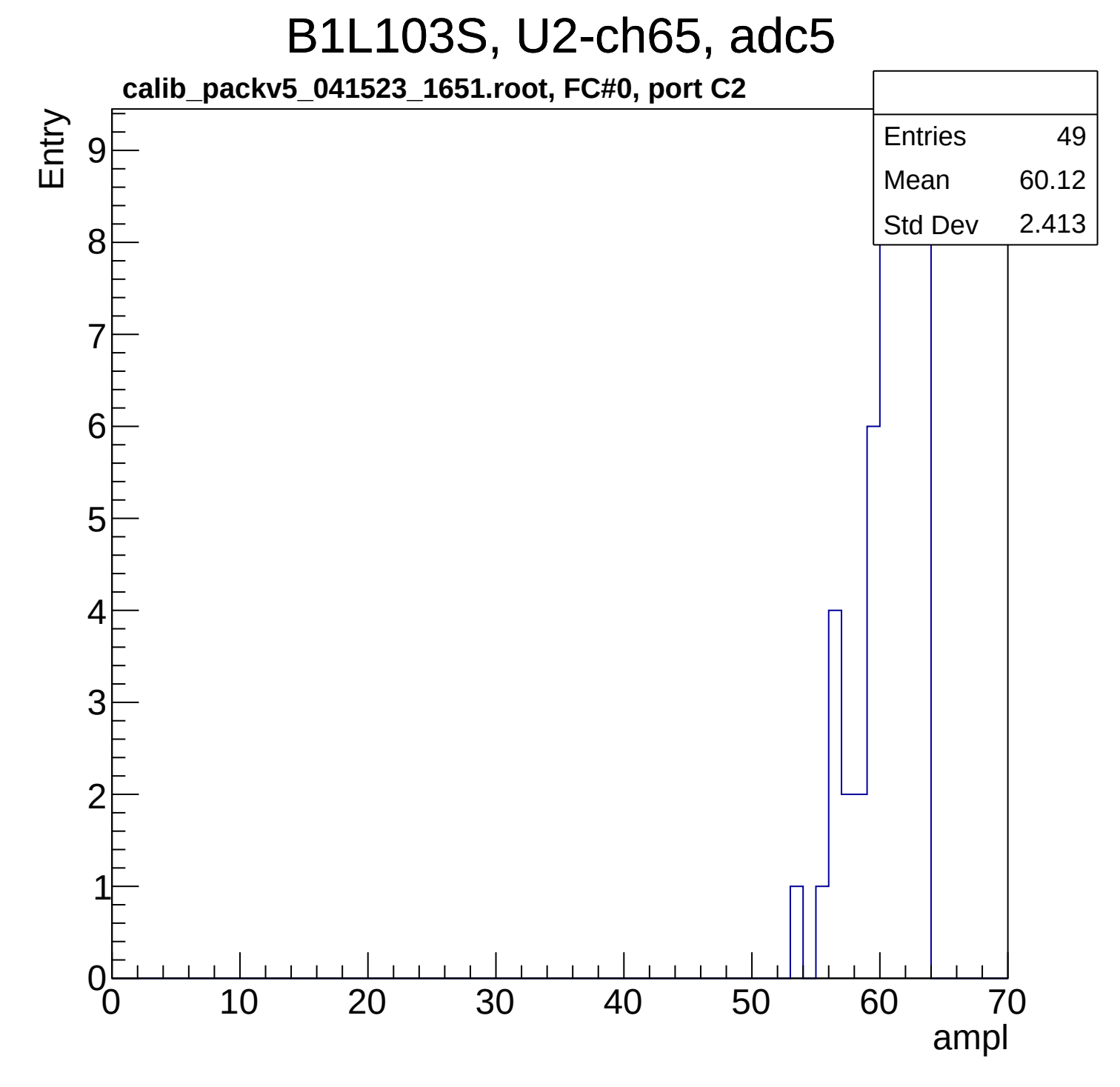

B1L103S, U2-ch65, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 26.37
Std Dev 10.14
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

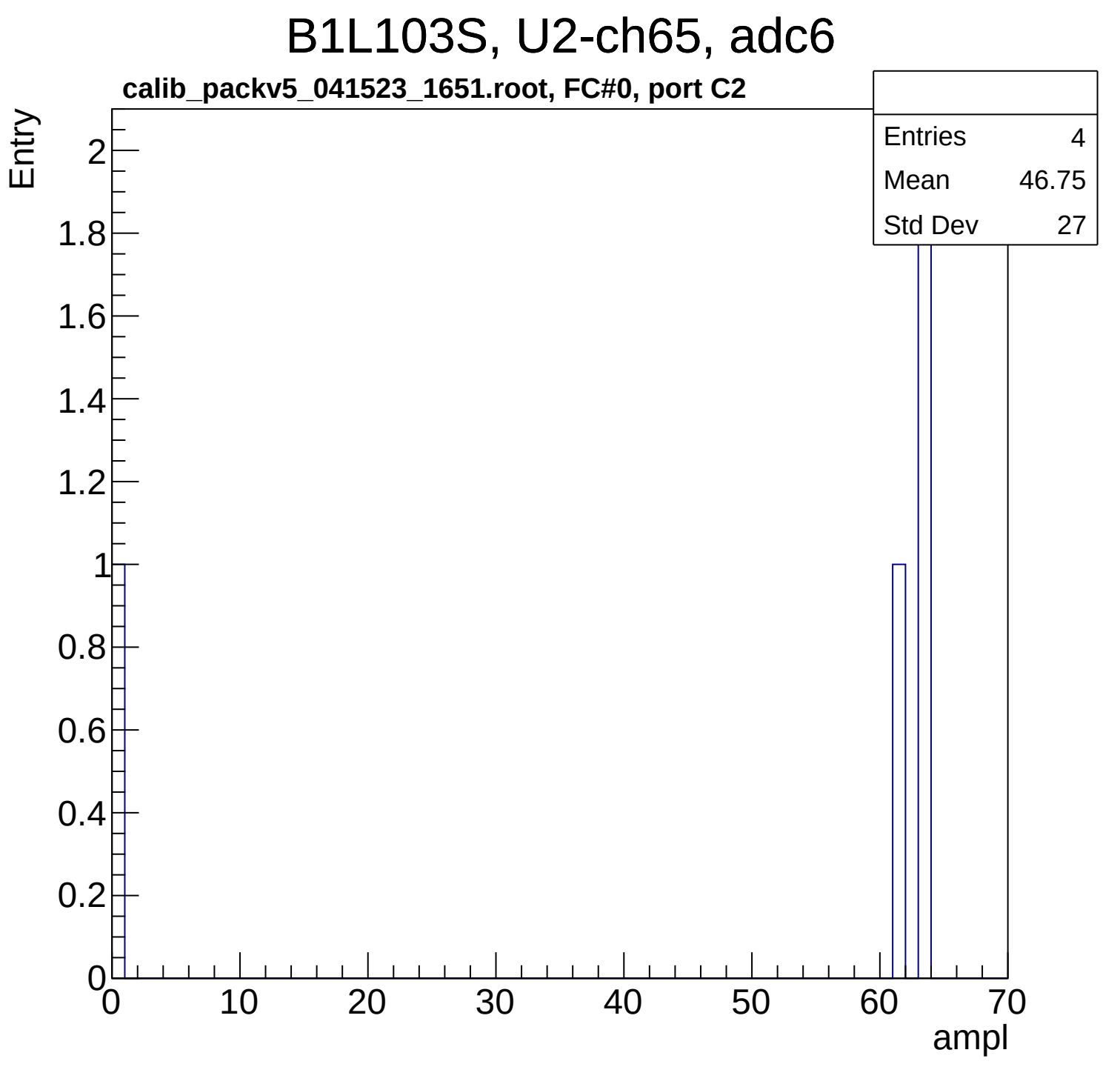

B1L103S, U2-ch65, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 36.59
Std Dev 3.217
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

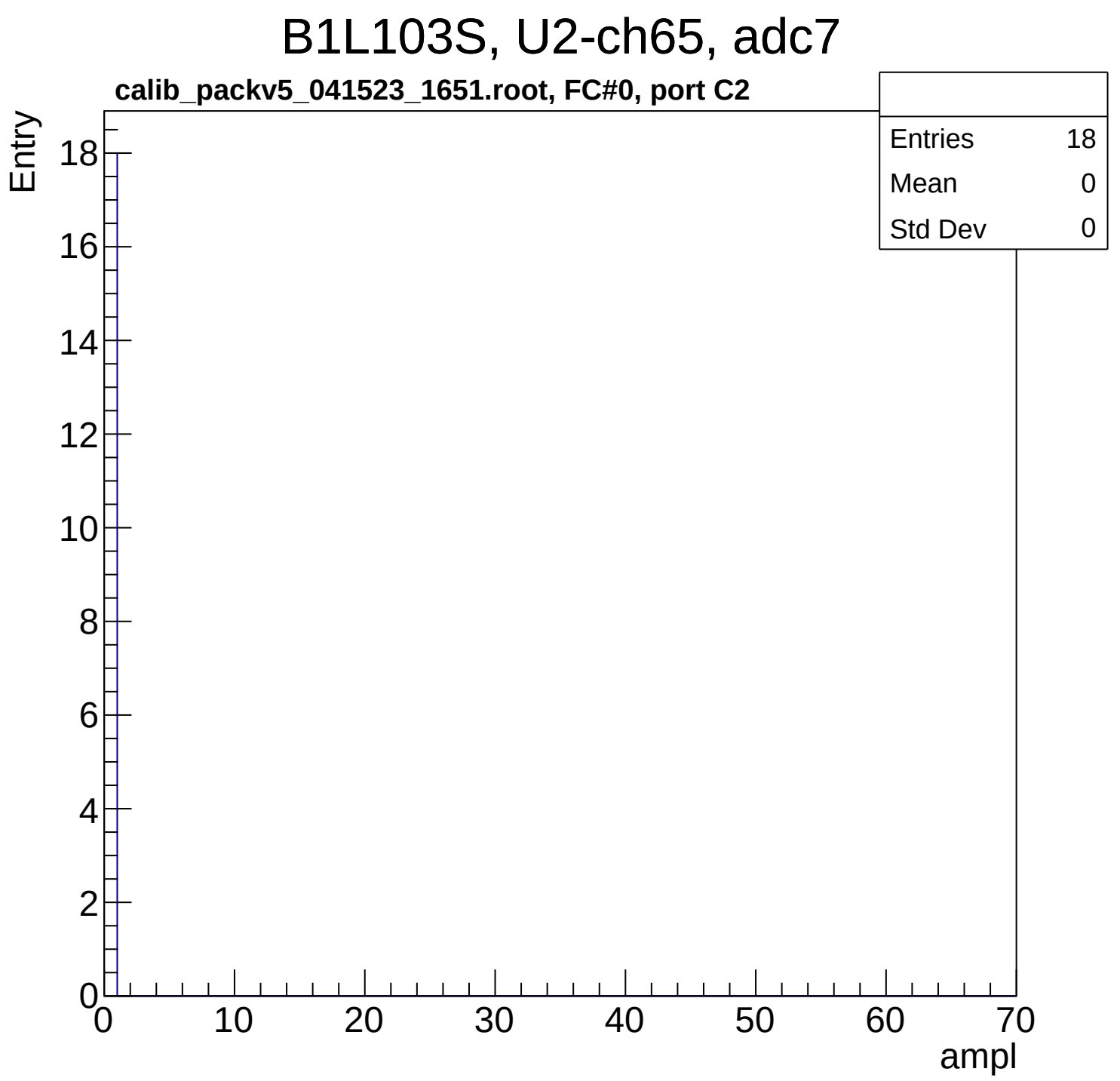

B1L103S, U2-ch65, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 35.69
Std Dev 16.03
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

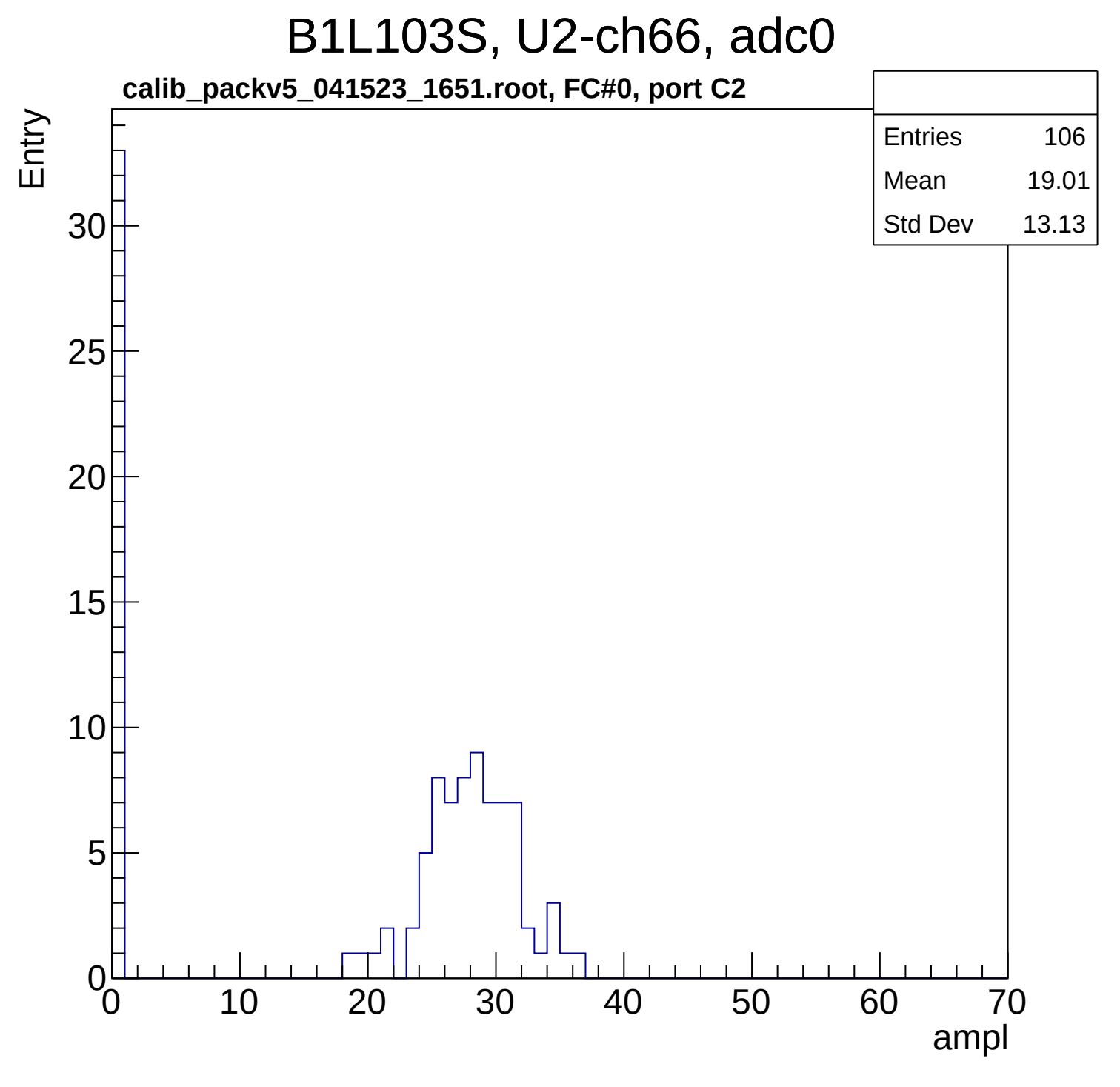

B1L103S, U2-ch65, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 46.43
Std Dev 12.38
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

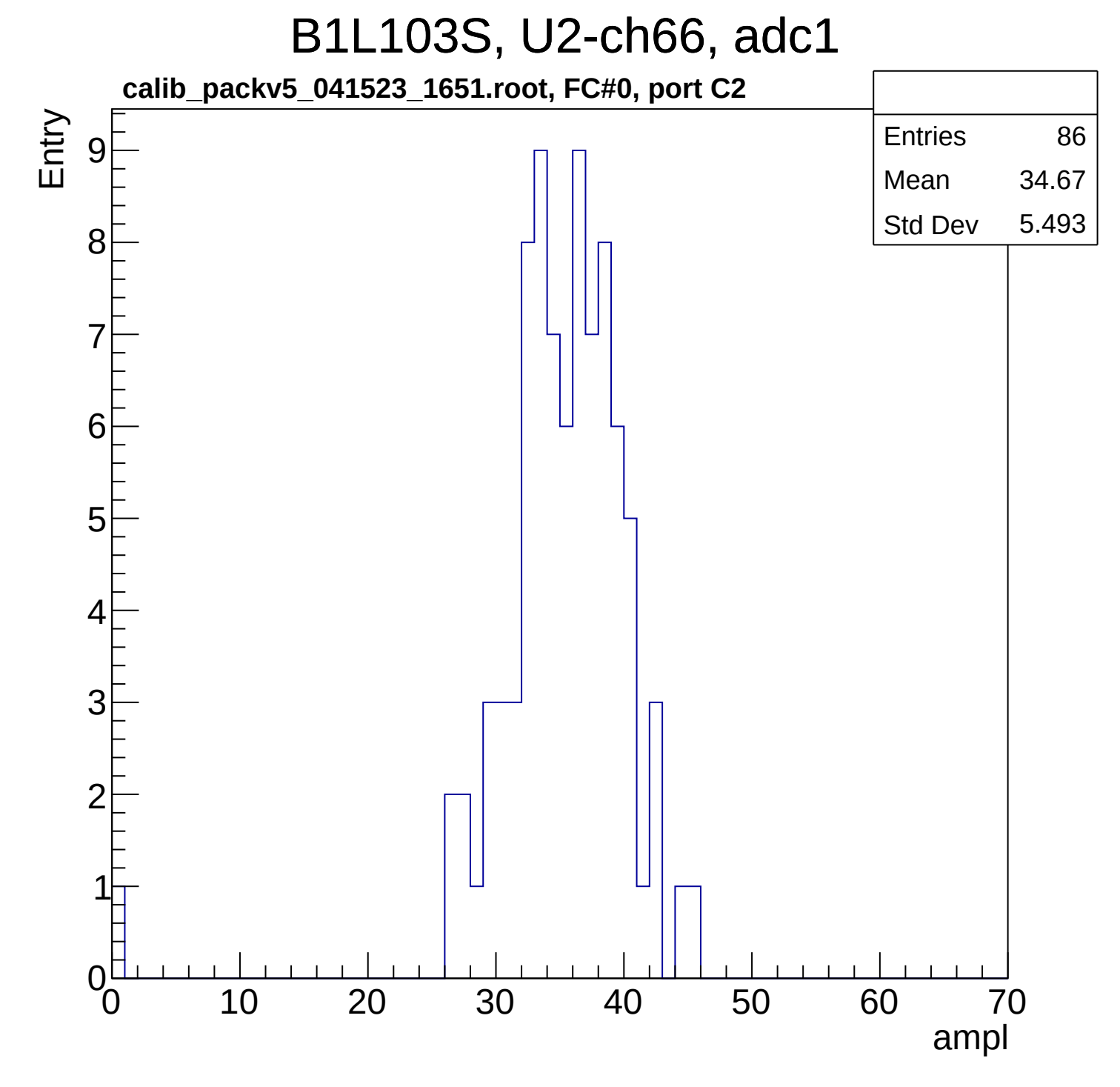

B1L103S, U2-ch65, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 54.9
Std Dev 3.197
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

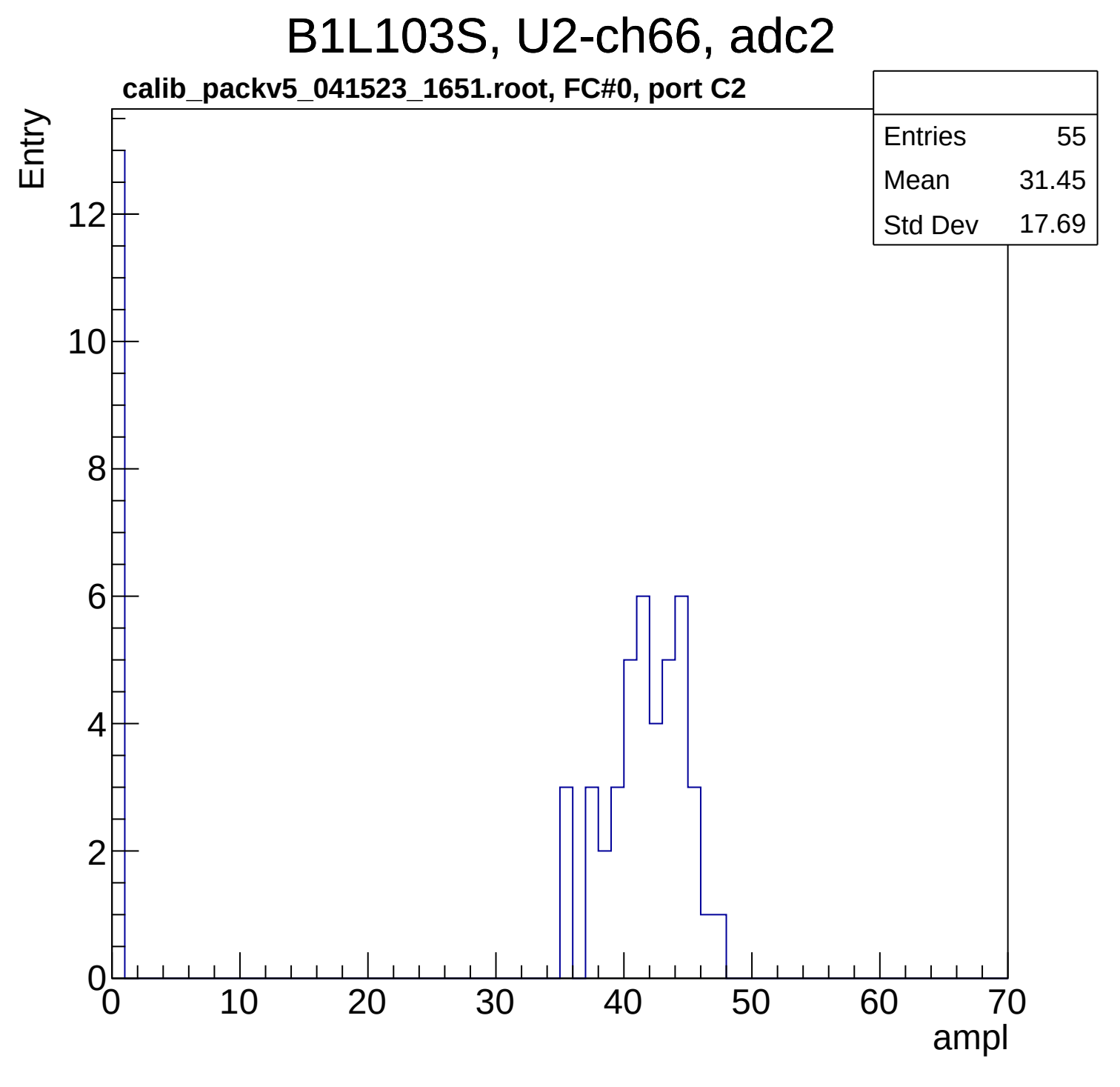

B1L103S, U2-ch65, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 60.12
Std Dev 2.413
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

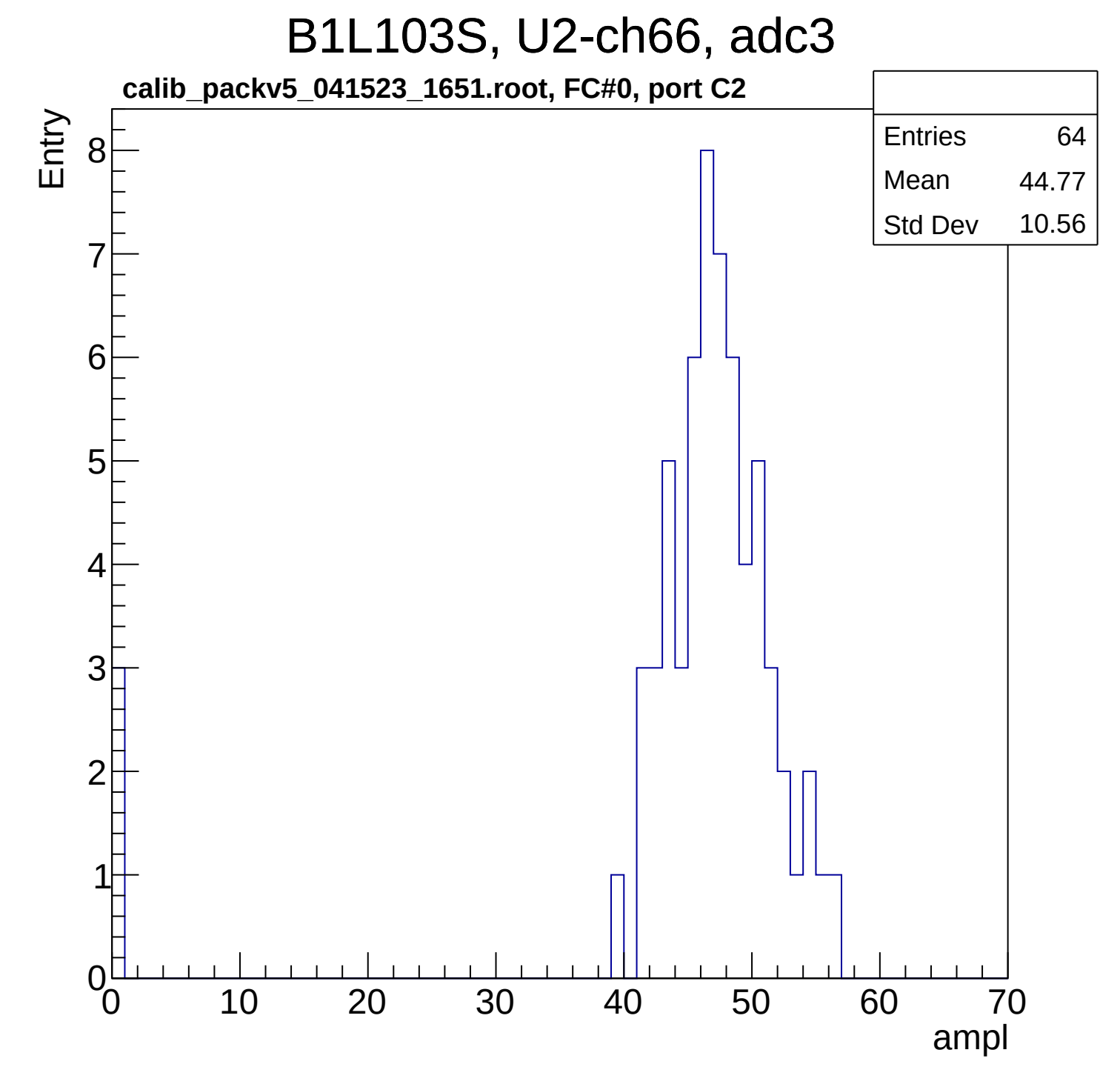

B1L103S, U2-ch65, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 46.75
Std Dev 27
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

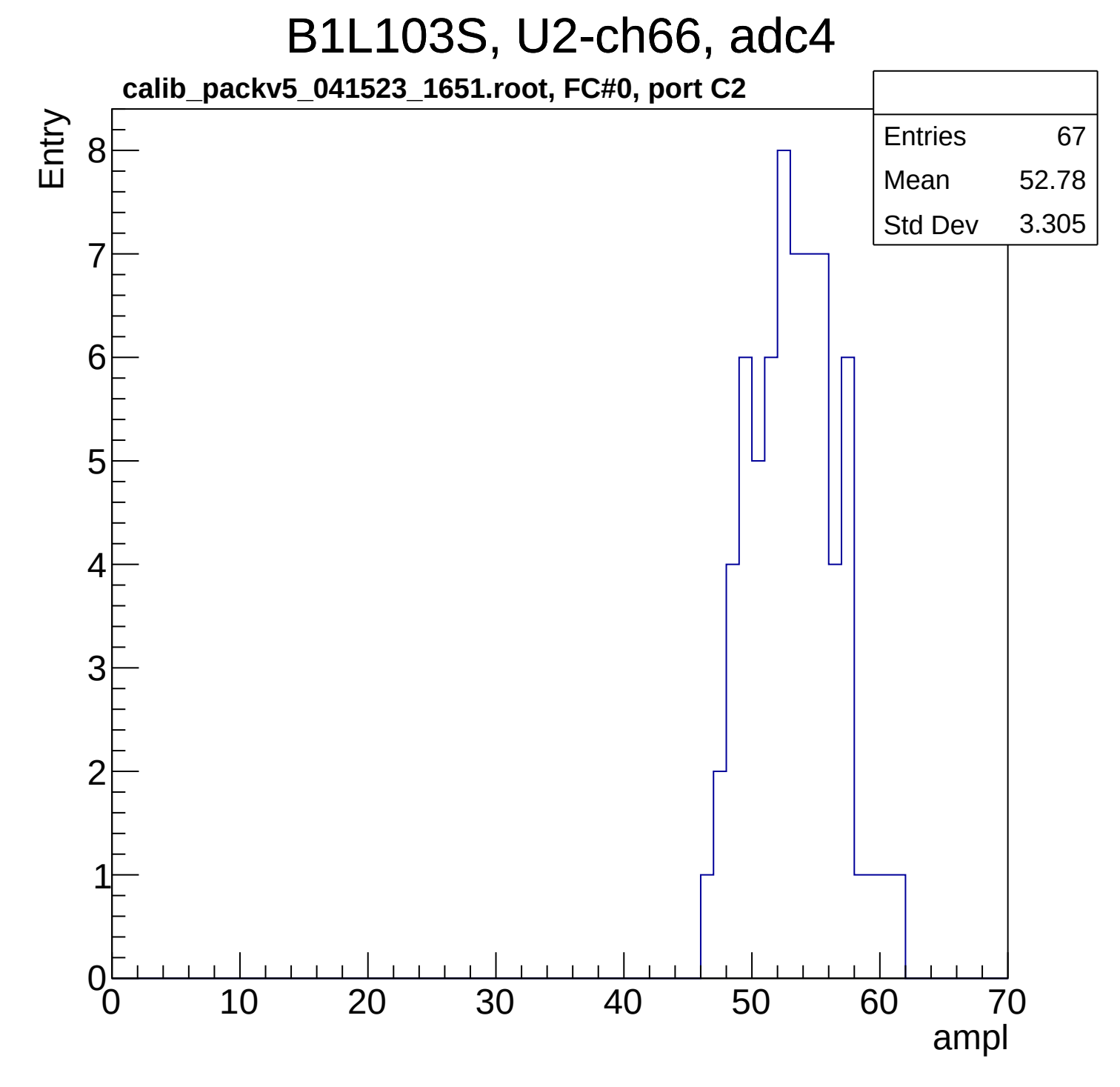

B1L103S, U2-ch65, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

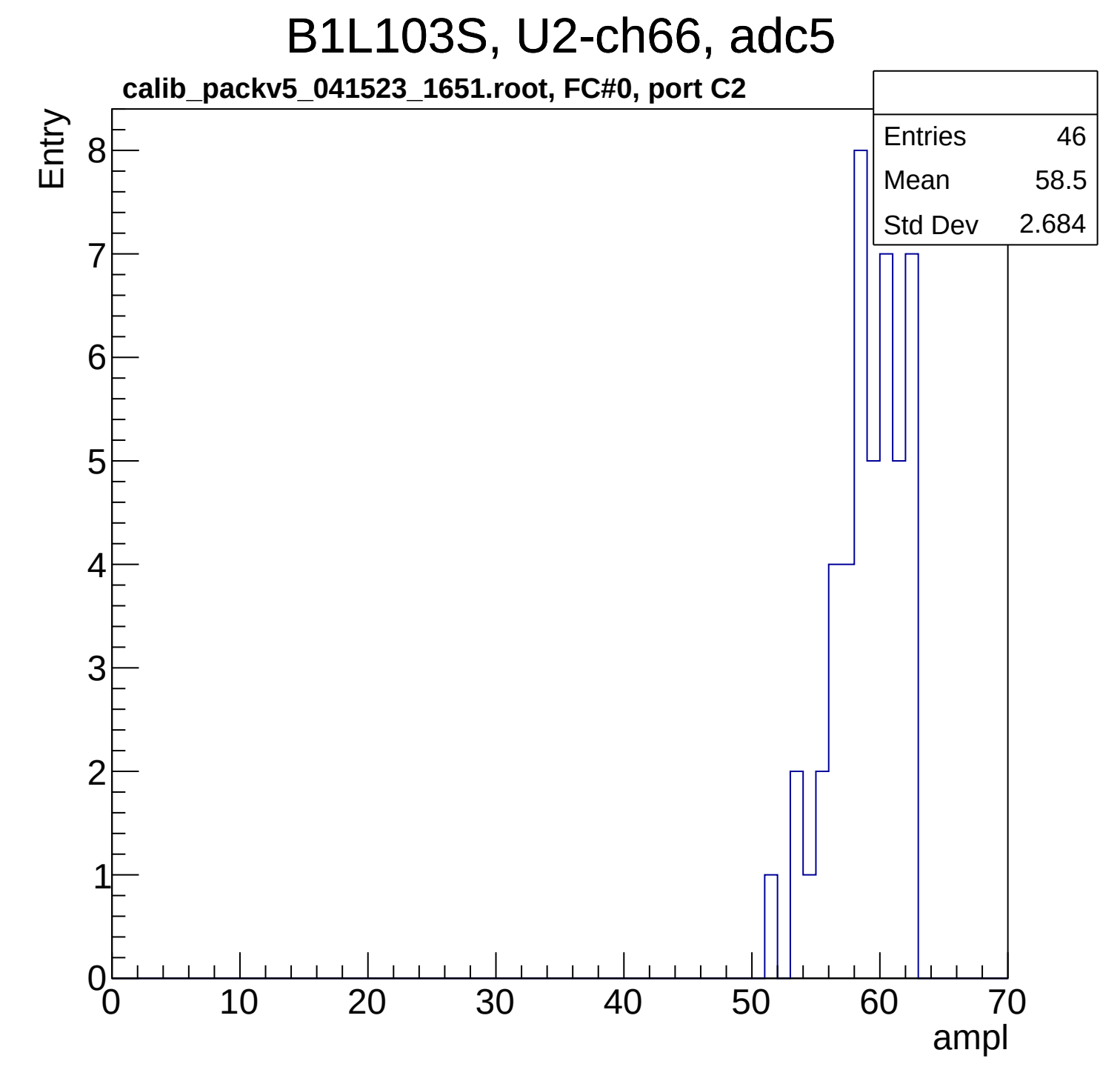

B1L103S, U2-ch66, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 106
Mean 19.01
Std Dev 13.13
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl

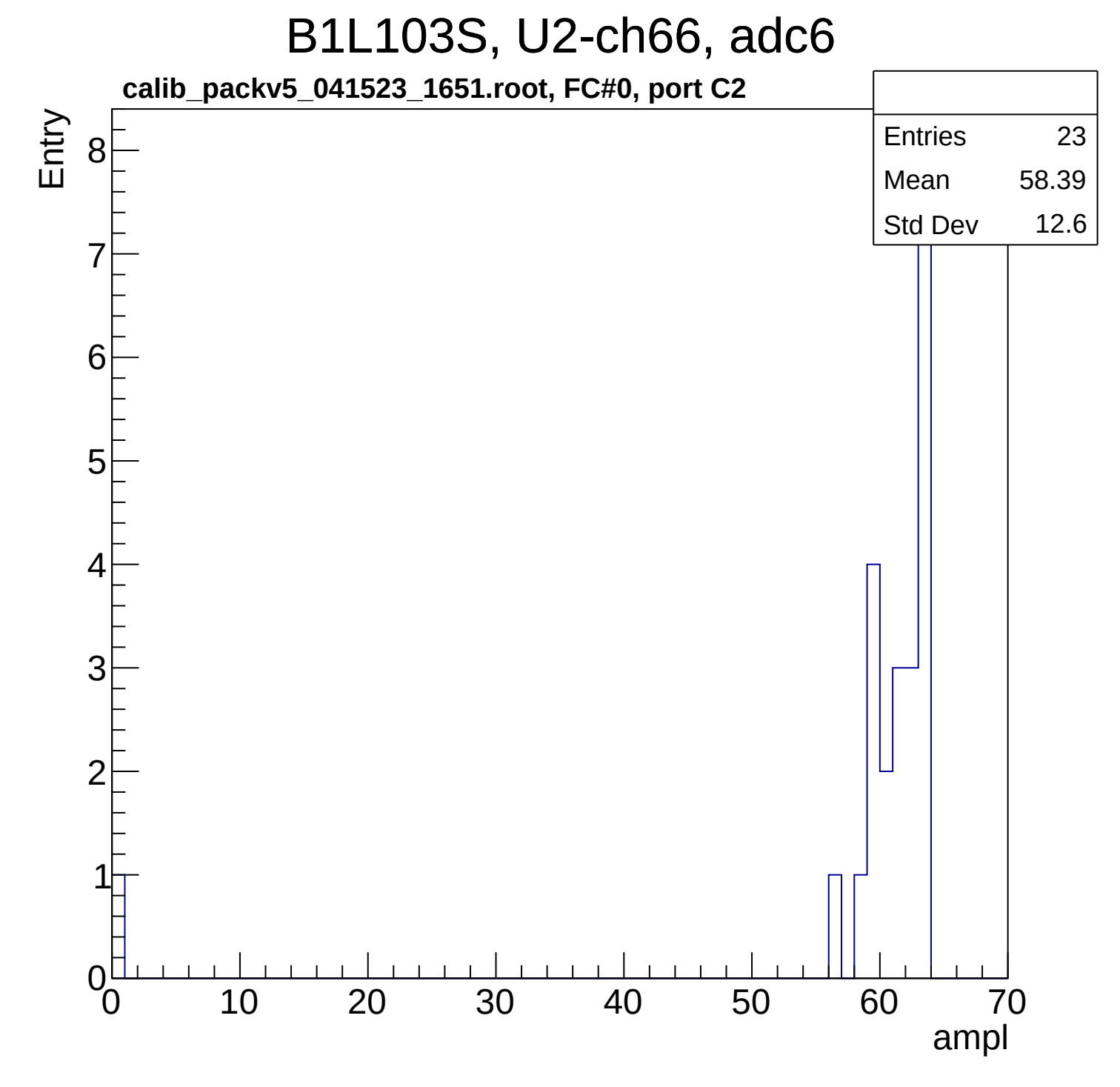

B1L103S, U2-ch66, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 34.67
Std Dev 5.493
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

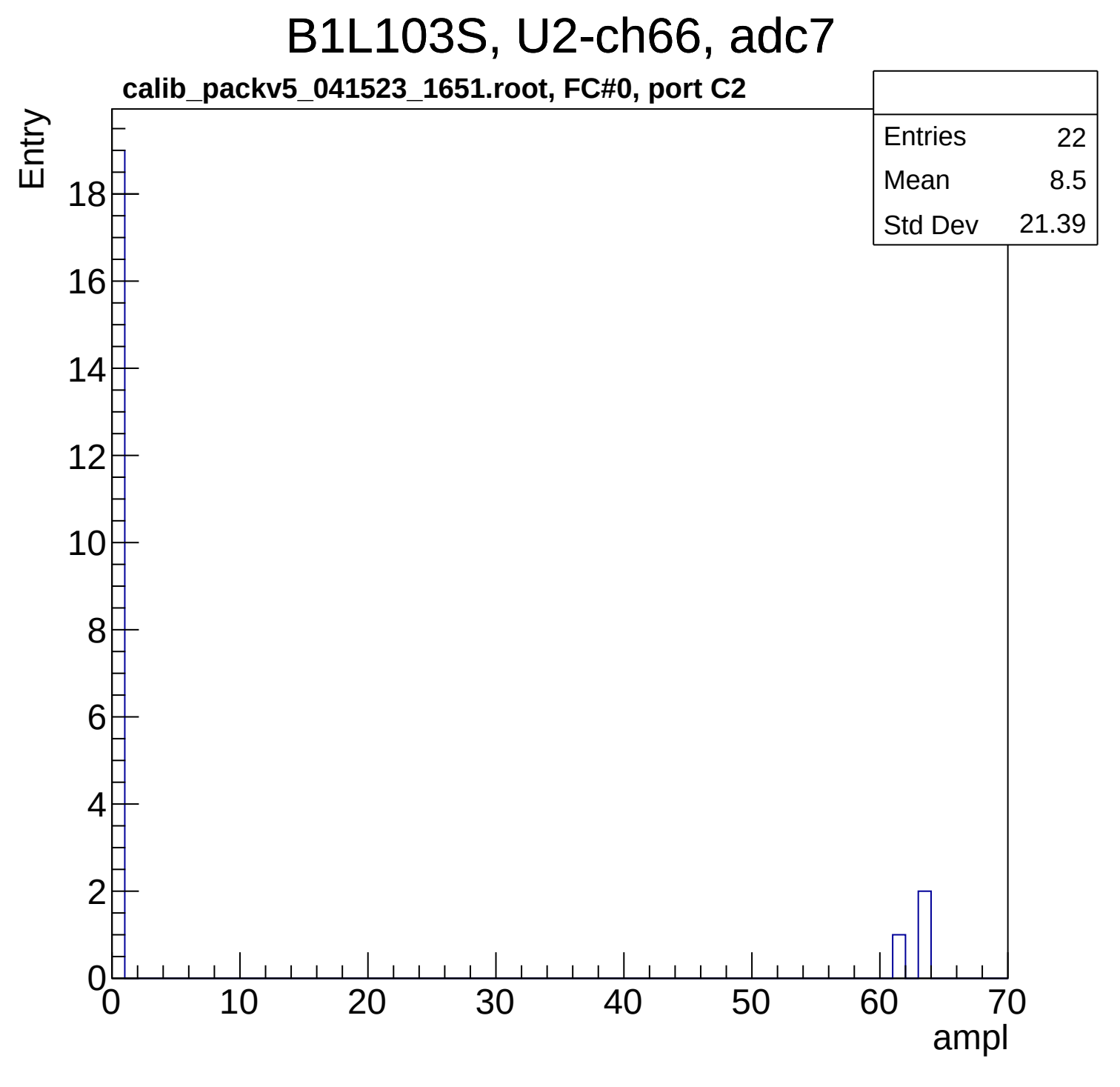

B1L103S, U2-ch66, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 31.45
Std Dev 17.69
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

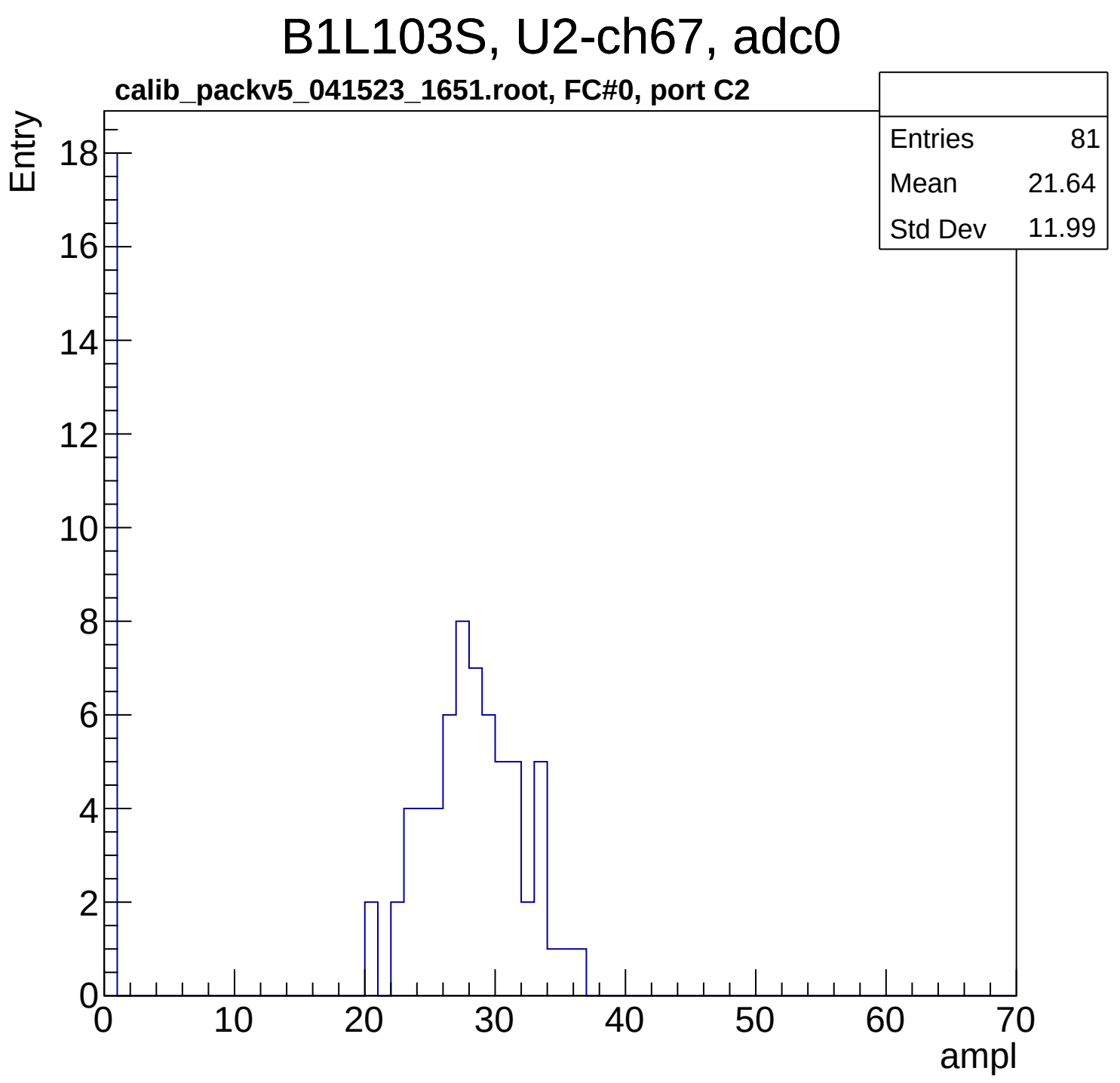

B1L103S, U2-ch66, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 44.77
Std Dev 10.56
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

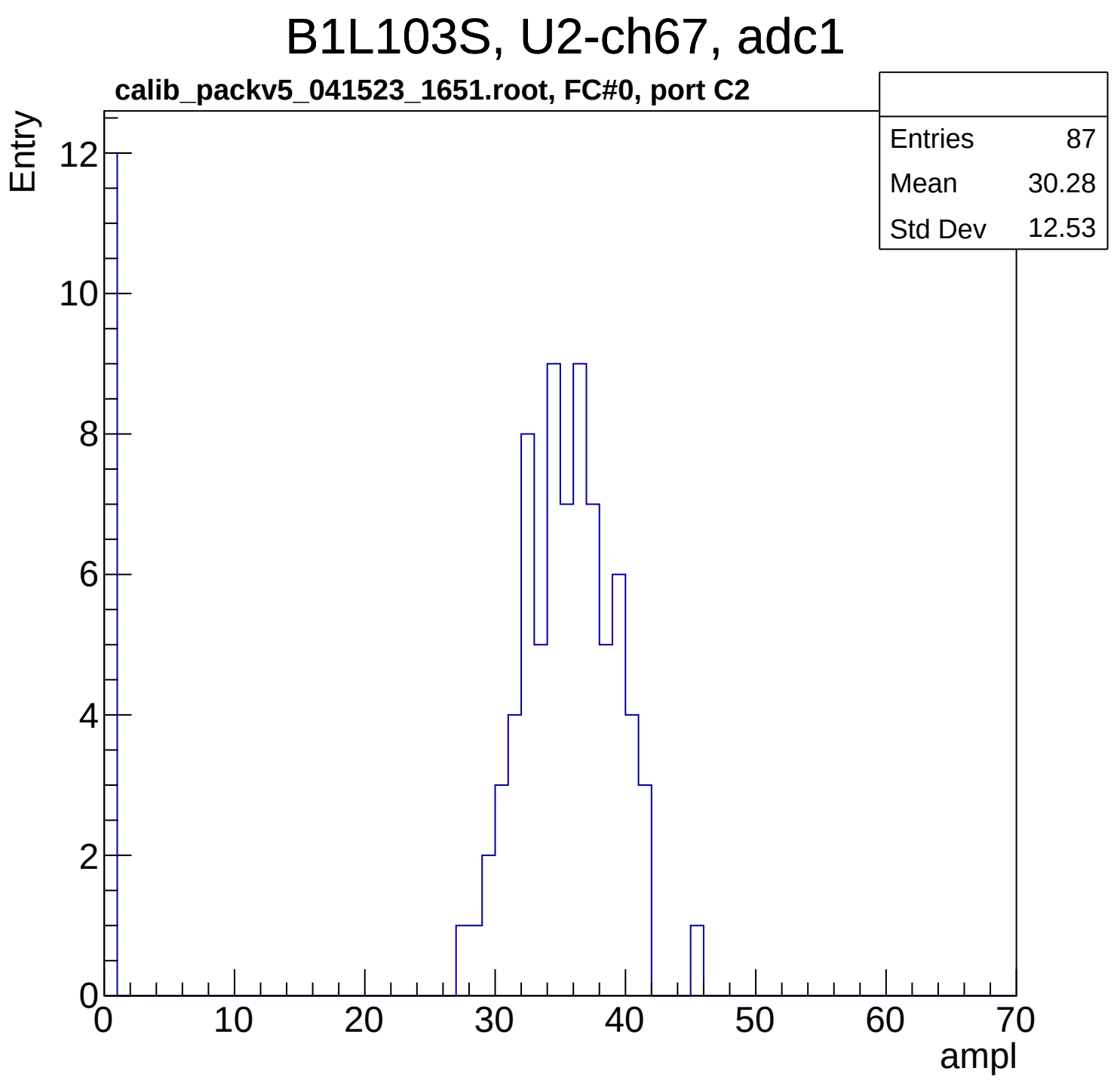

B1L103S, U2-ch66, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 52.78
Std Dev 3.305
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

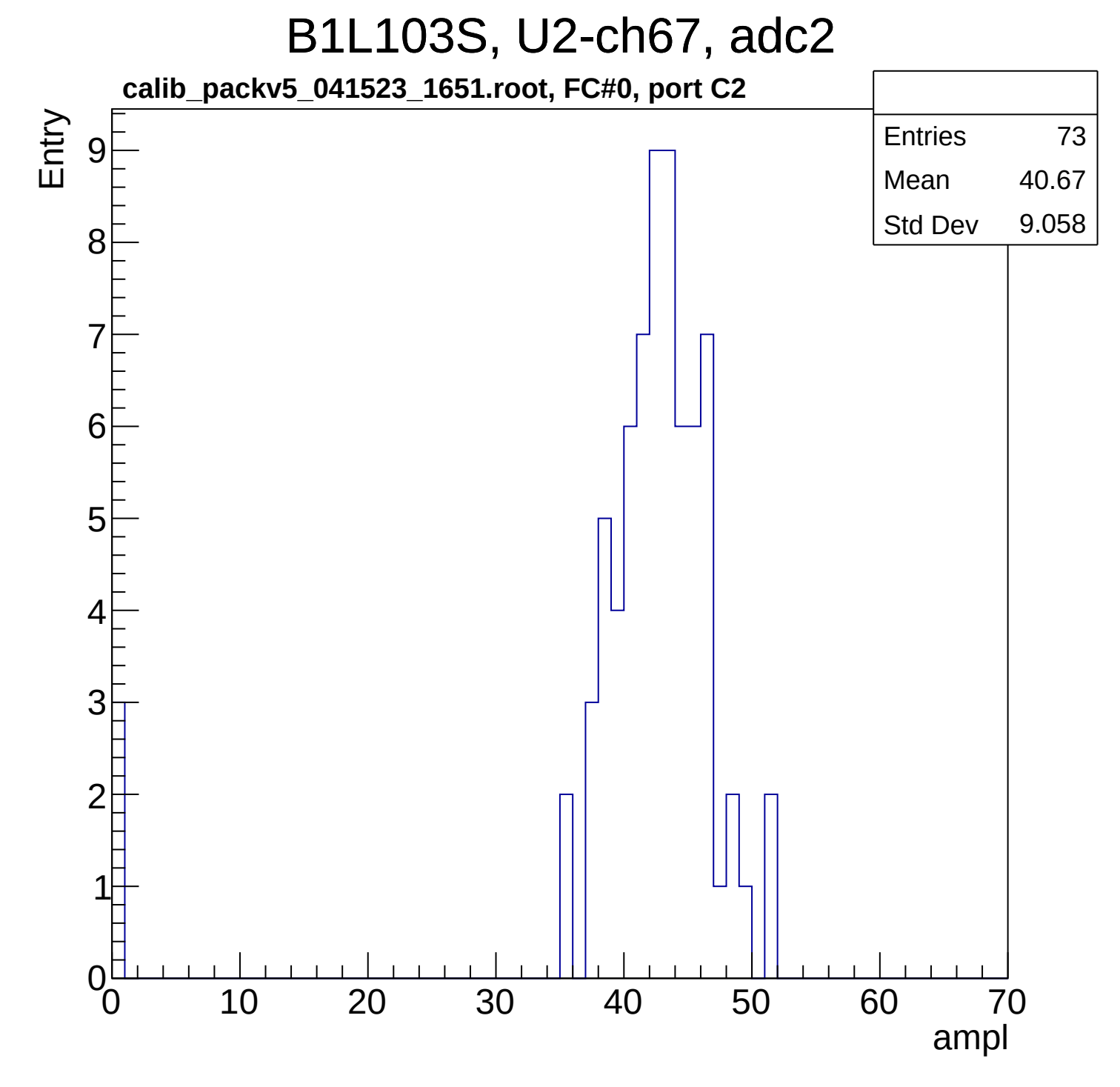

B1L103S, U2-ch66, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.5
Std Dev 2.684
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

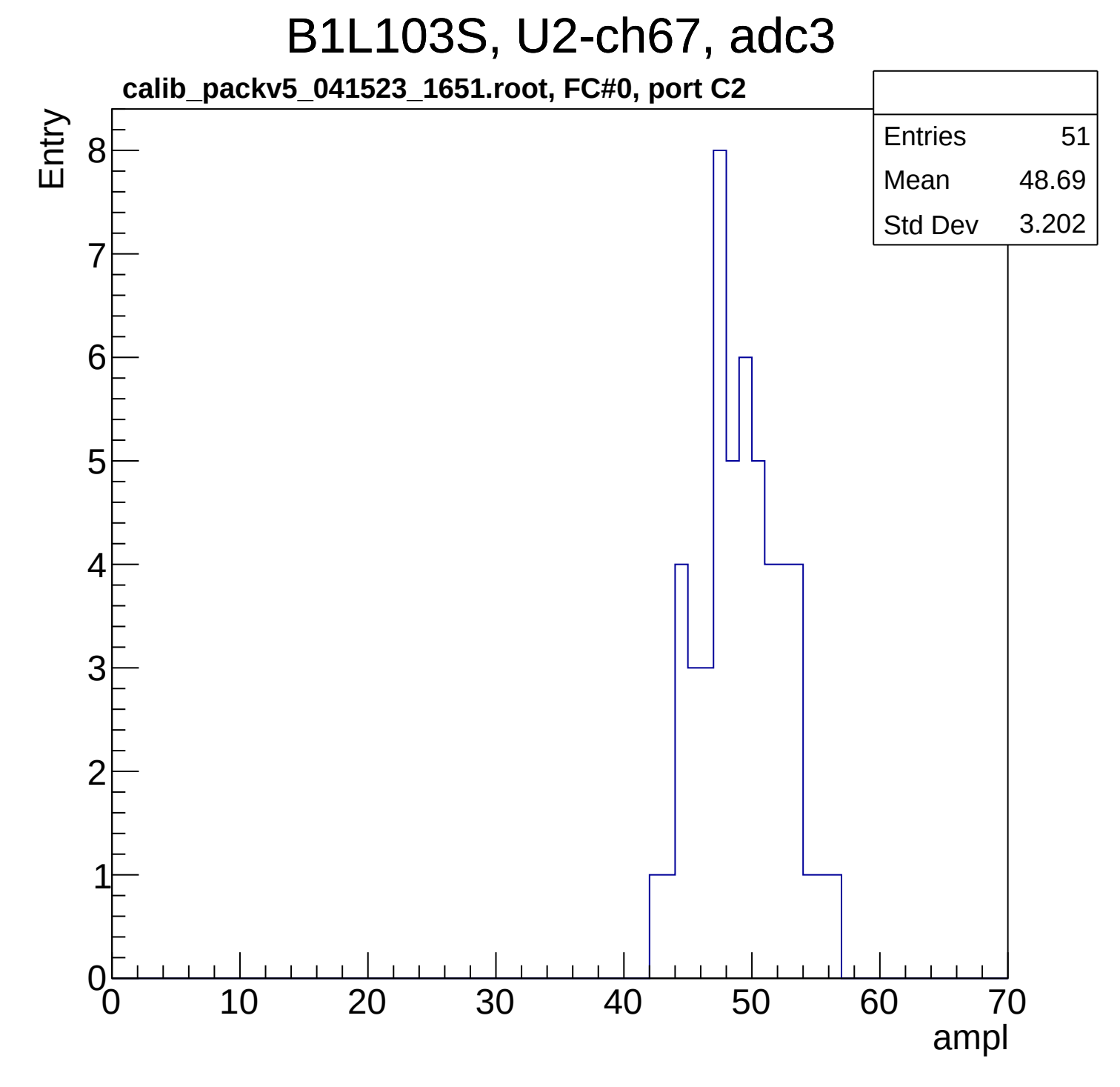

B1L103S, U2-ch66, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 58.39
Std Dev 12.6
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

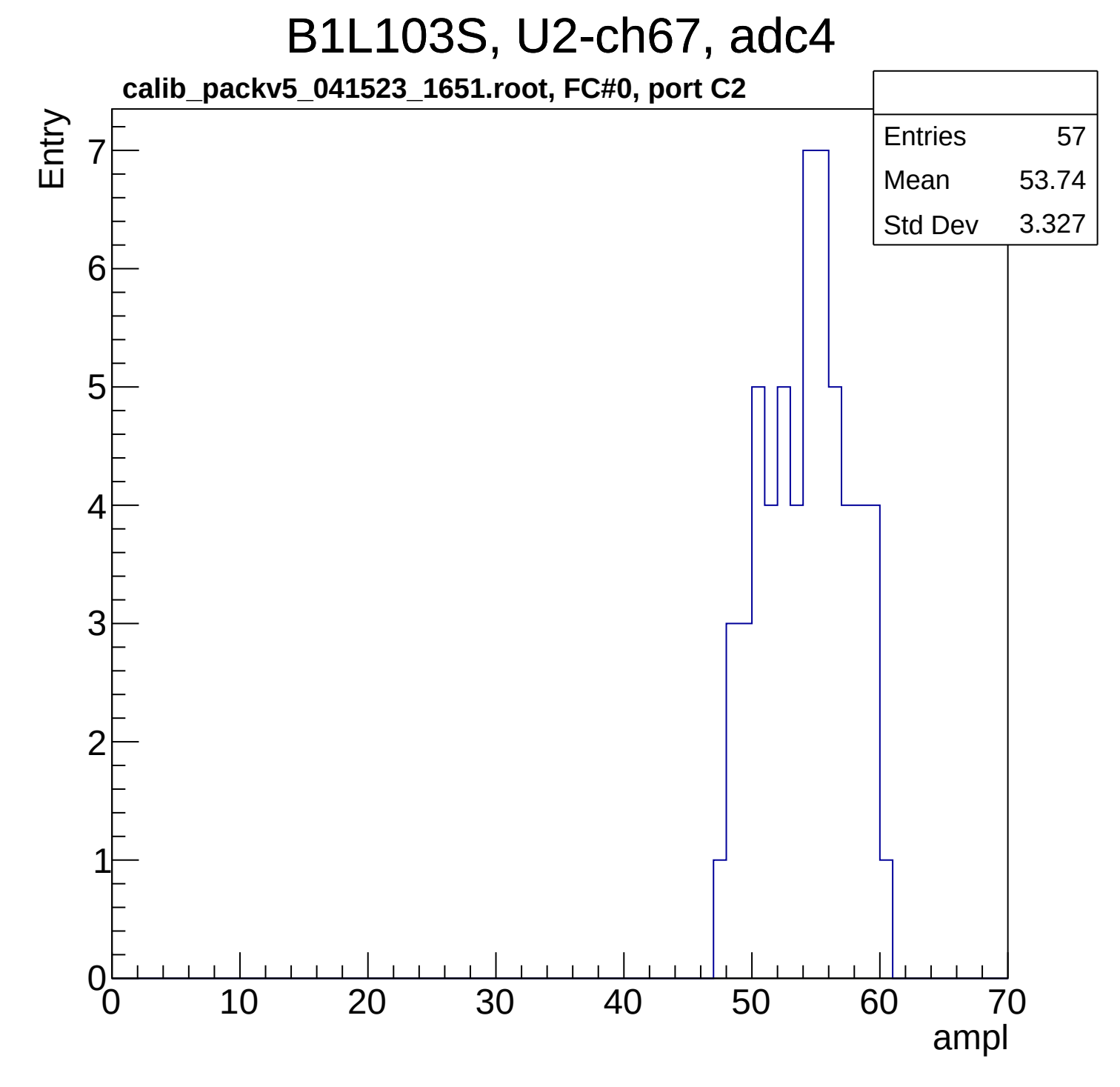

B1L103S, U2-ch66, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.5
Std Dev 21.39
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

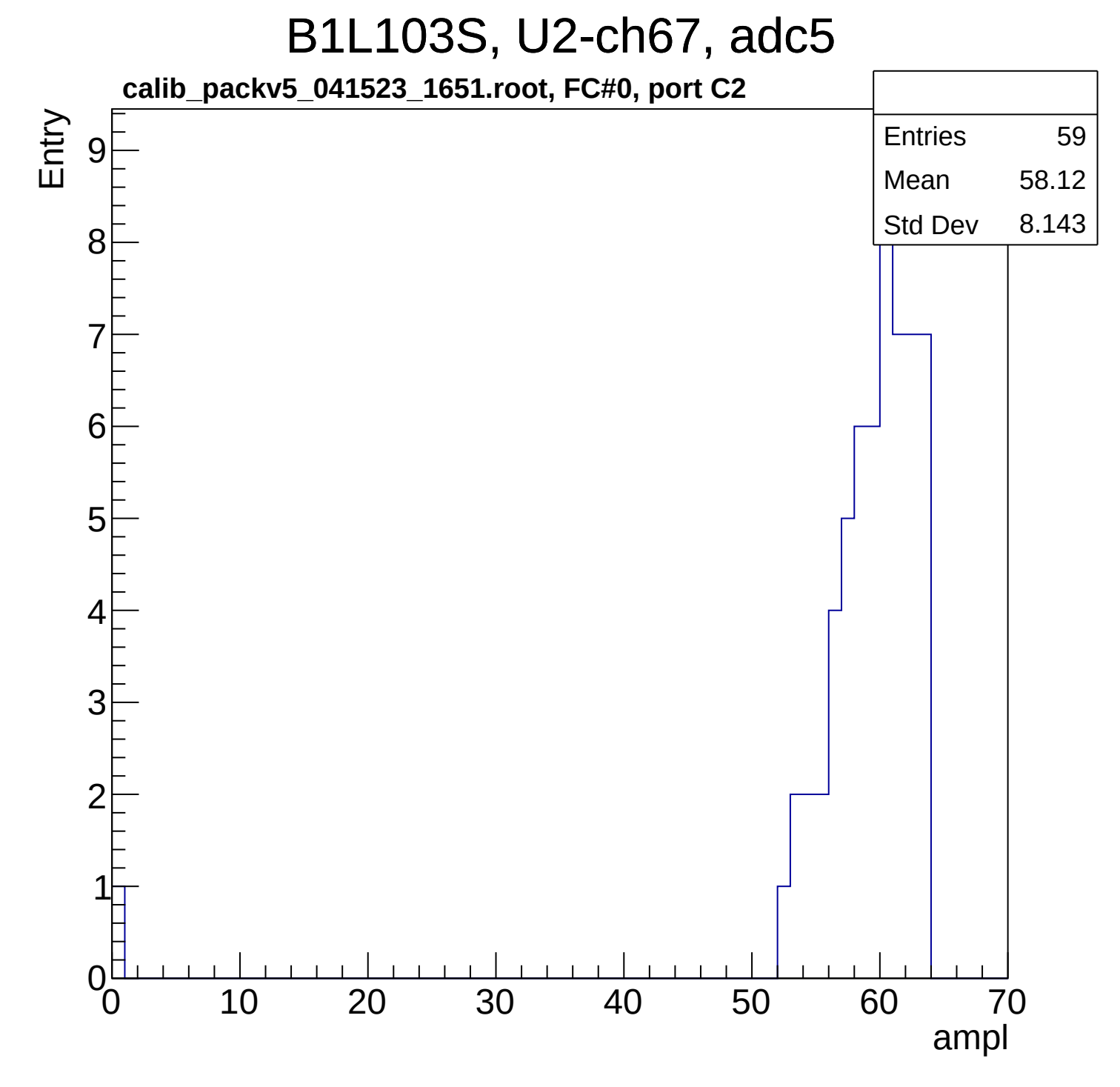

B1L103S, U2-ch67, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 21.64
Std Dev 11.99
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

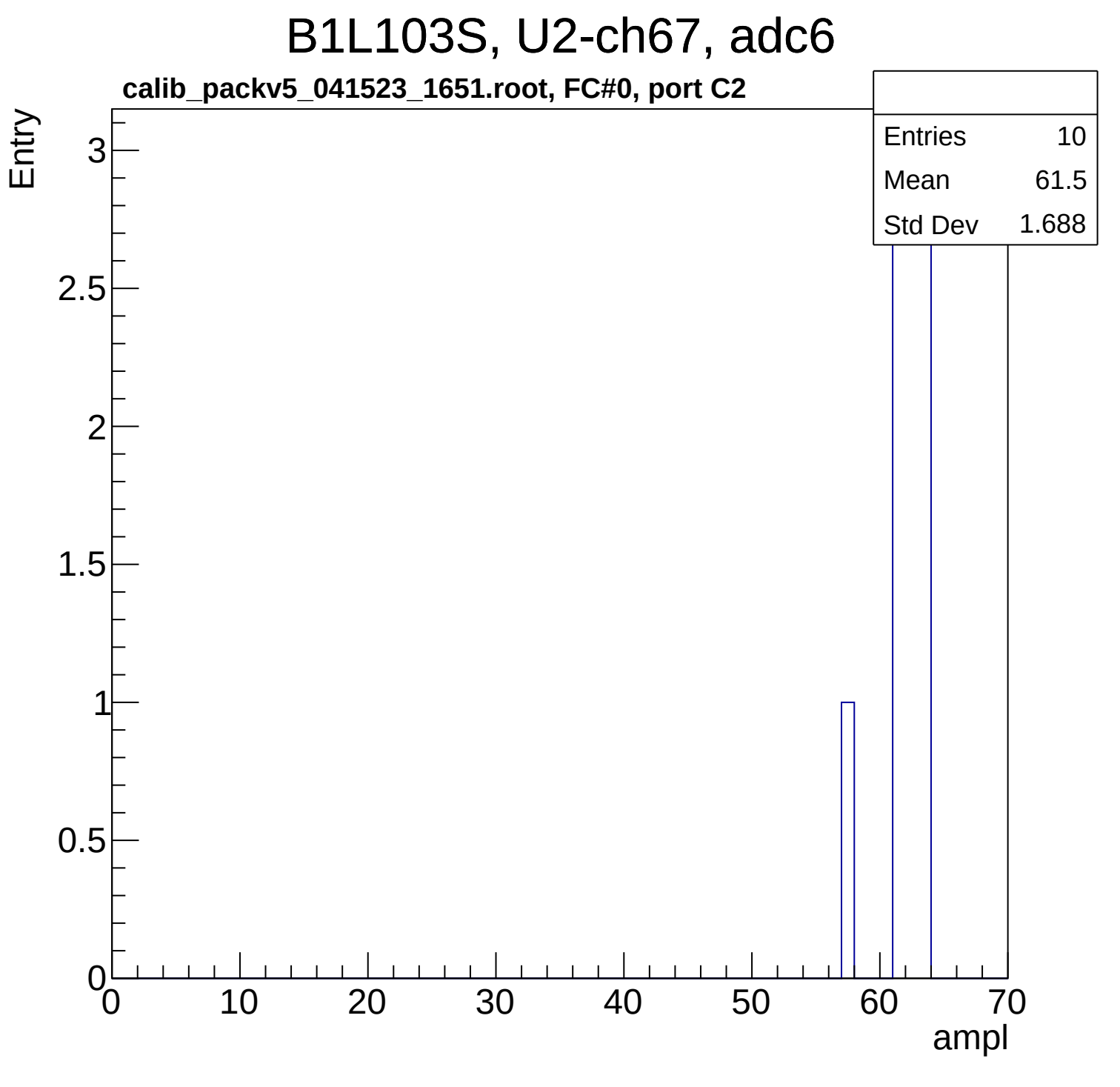

B1L103S, U2-ch67, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 30.28
Std Dev 12.53
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

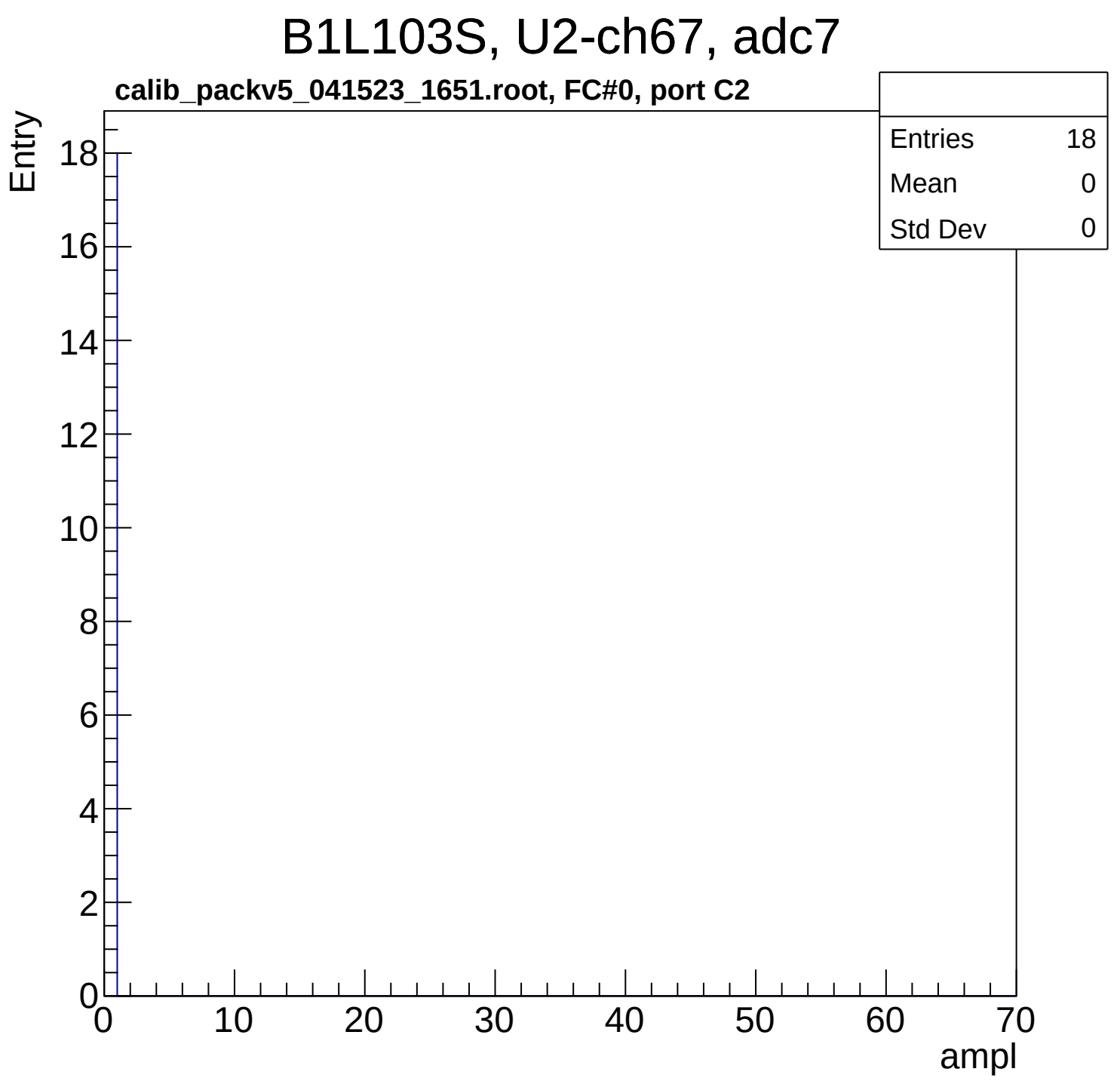

B1L103S, U2-ch67, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 40.67
Std Dev 9.058
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

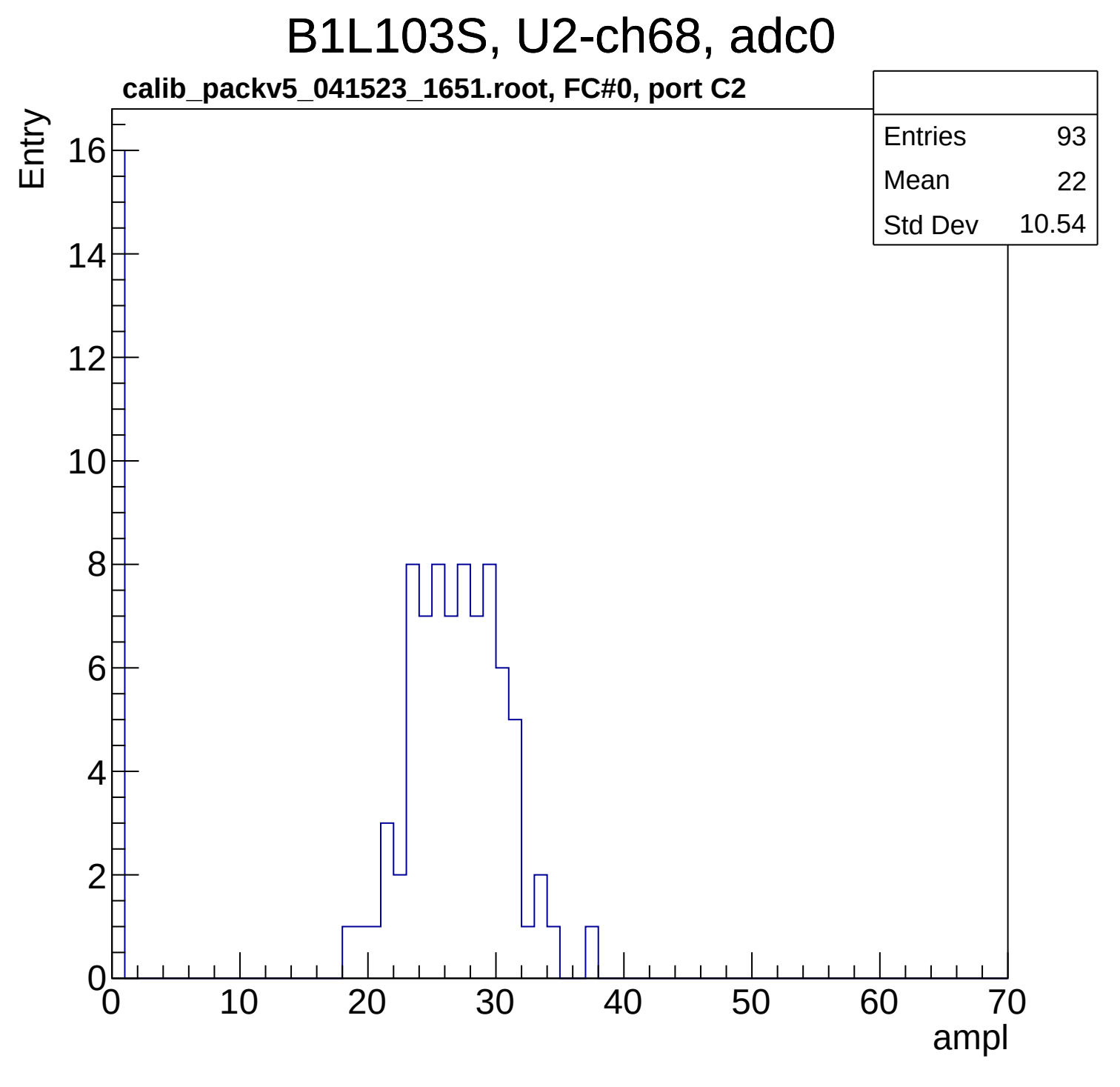

B1L103S, U2-ch67, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 48.69
Std Dev 3.202
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

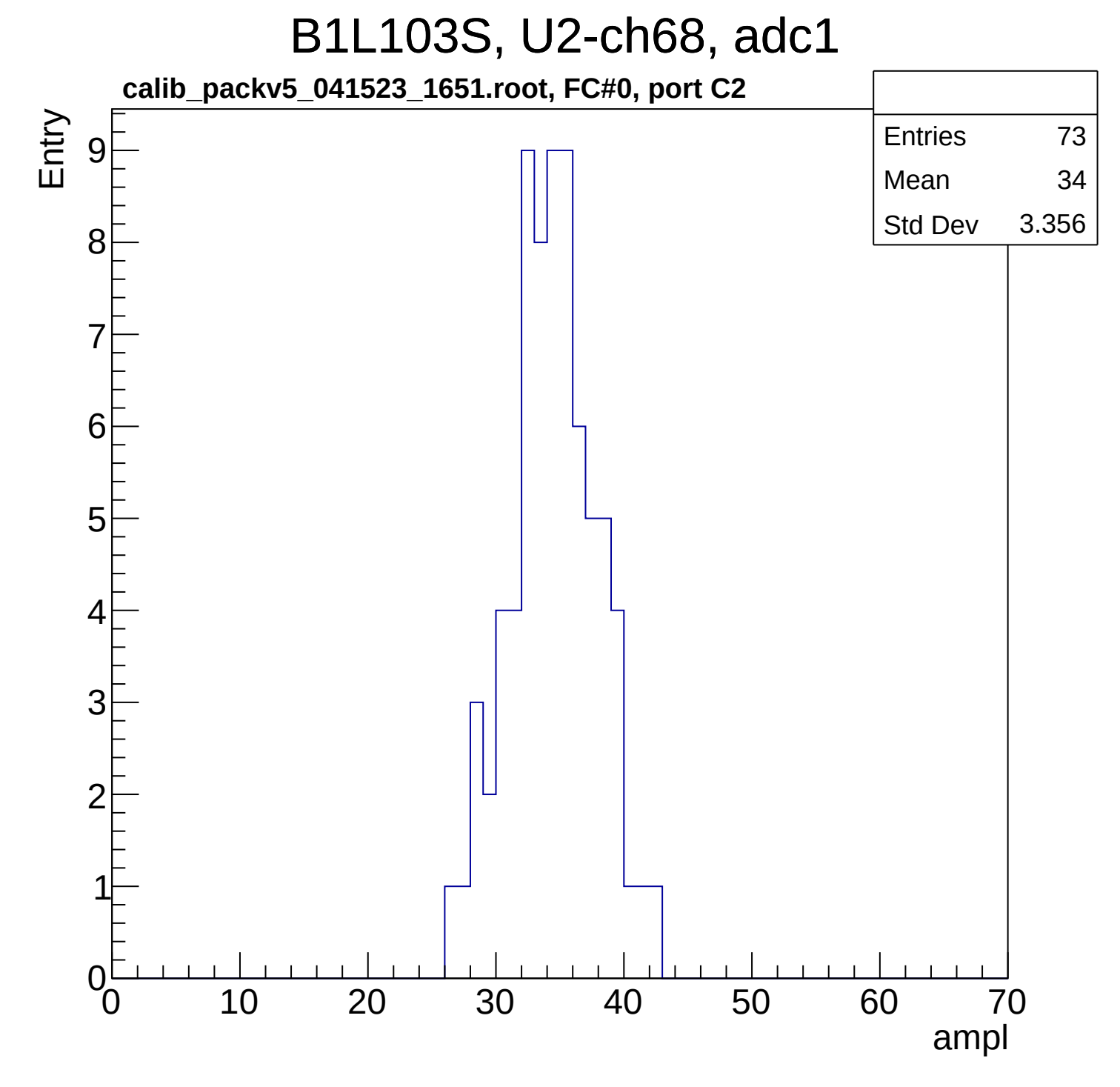

B1L103S, U2-ch67, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 53.74
Std Dev 3.327
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

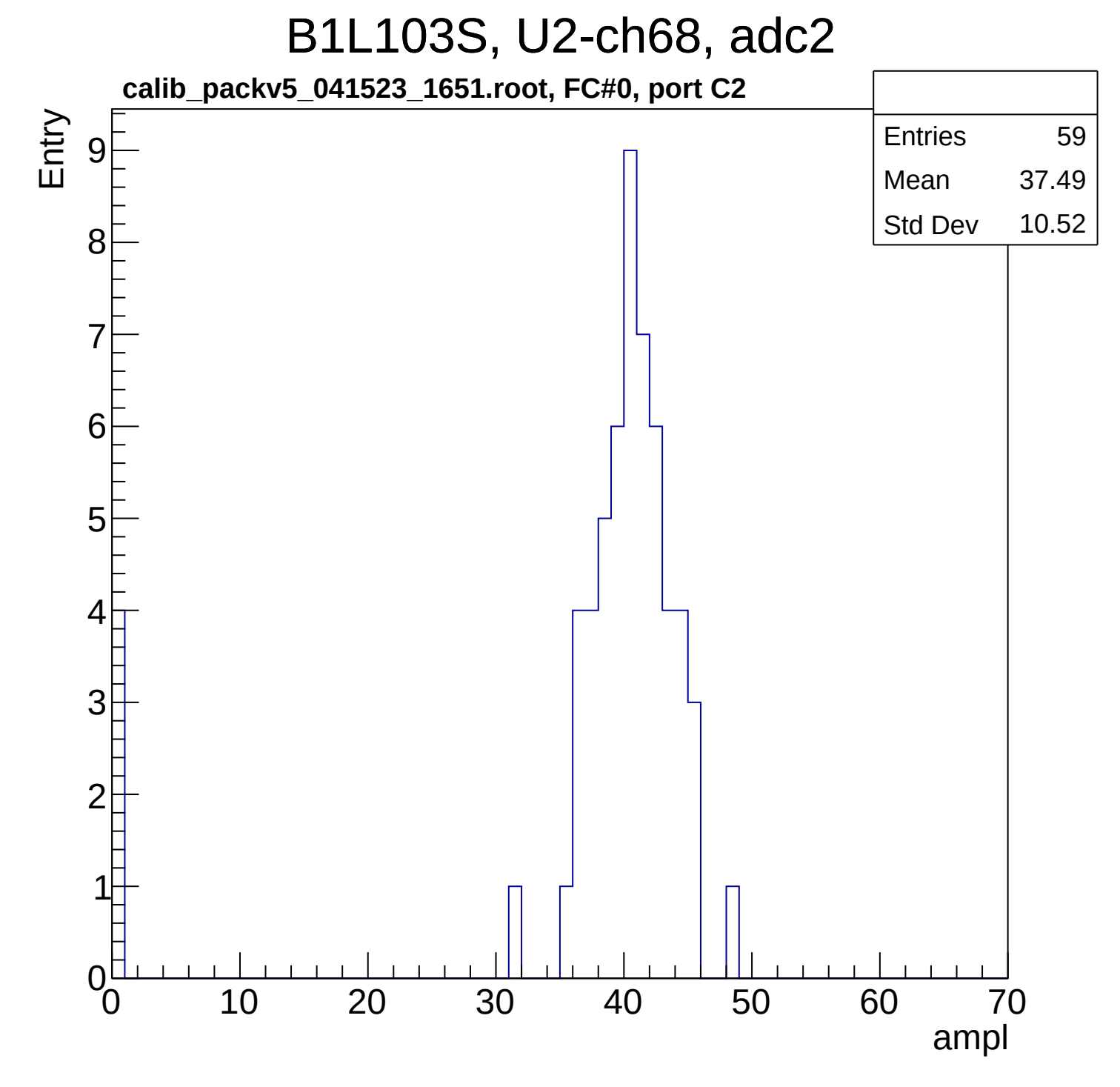

B1L103S, U2-ch67, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 58.12
Std Dev 8.143
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

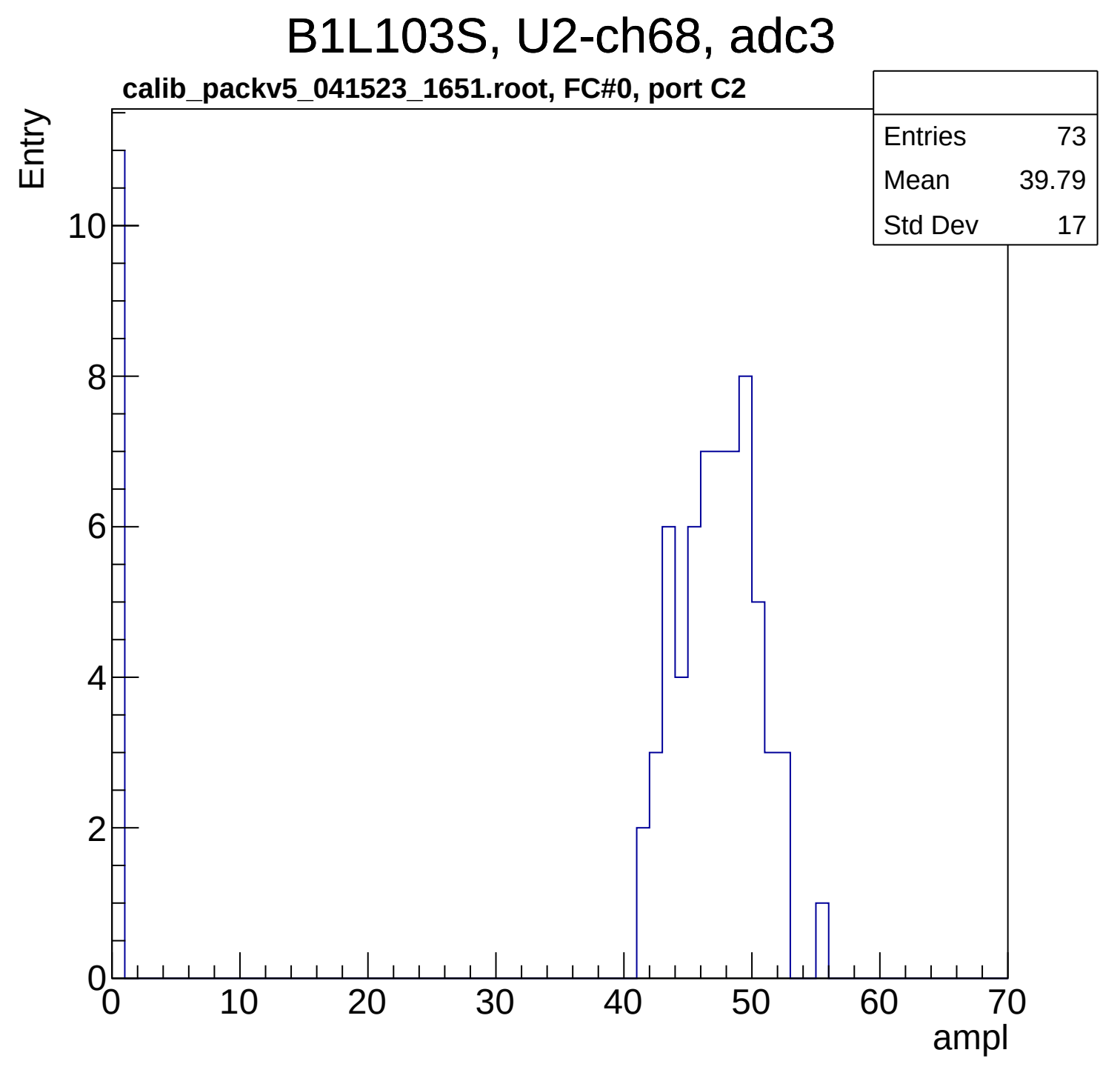

B1L103S, U2-ch67, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.5
Std Dev 1.688
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

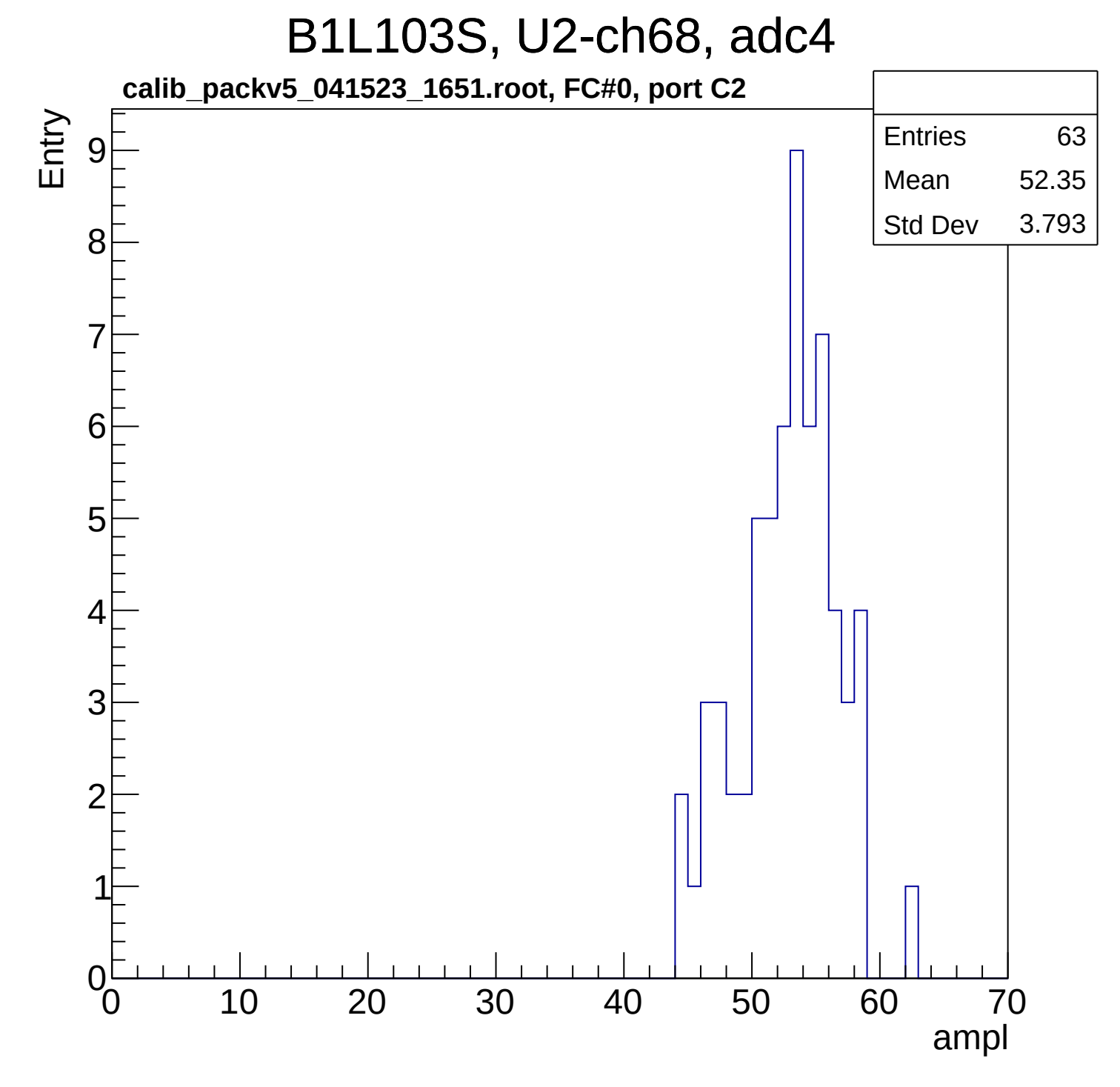

B1L103S, U2-ch67, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

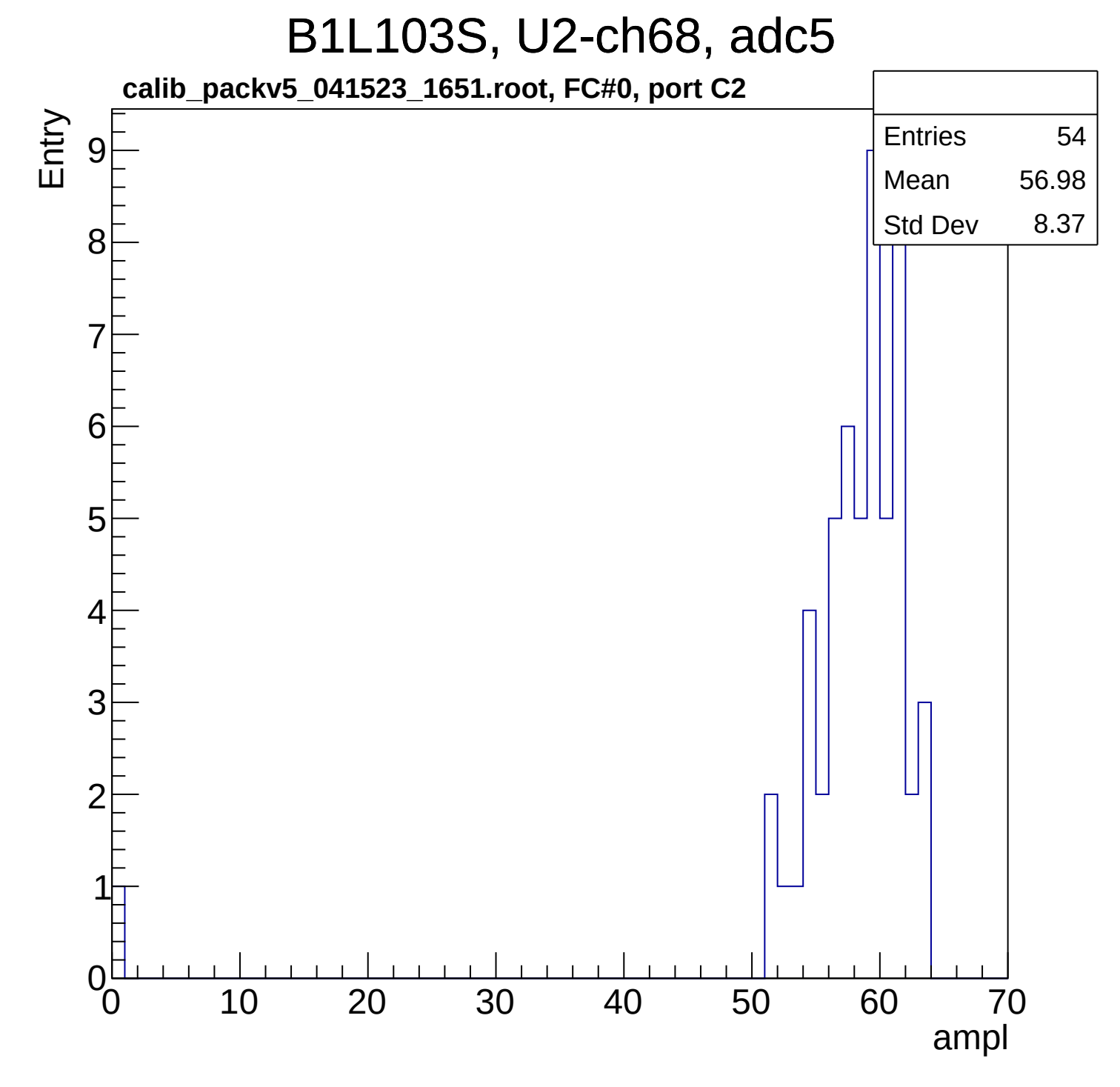

B1L103S, U2-ch68, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 22
Std Dev 10.54
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

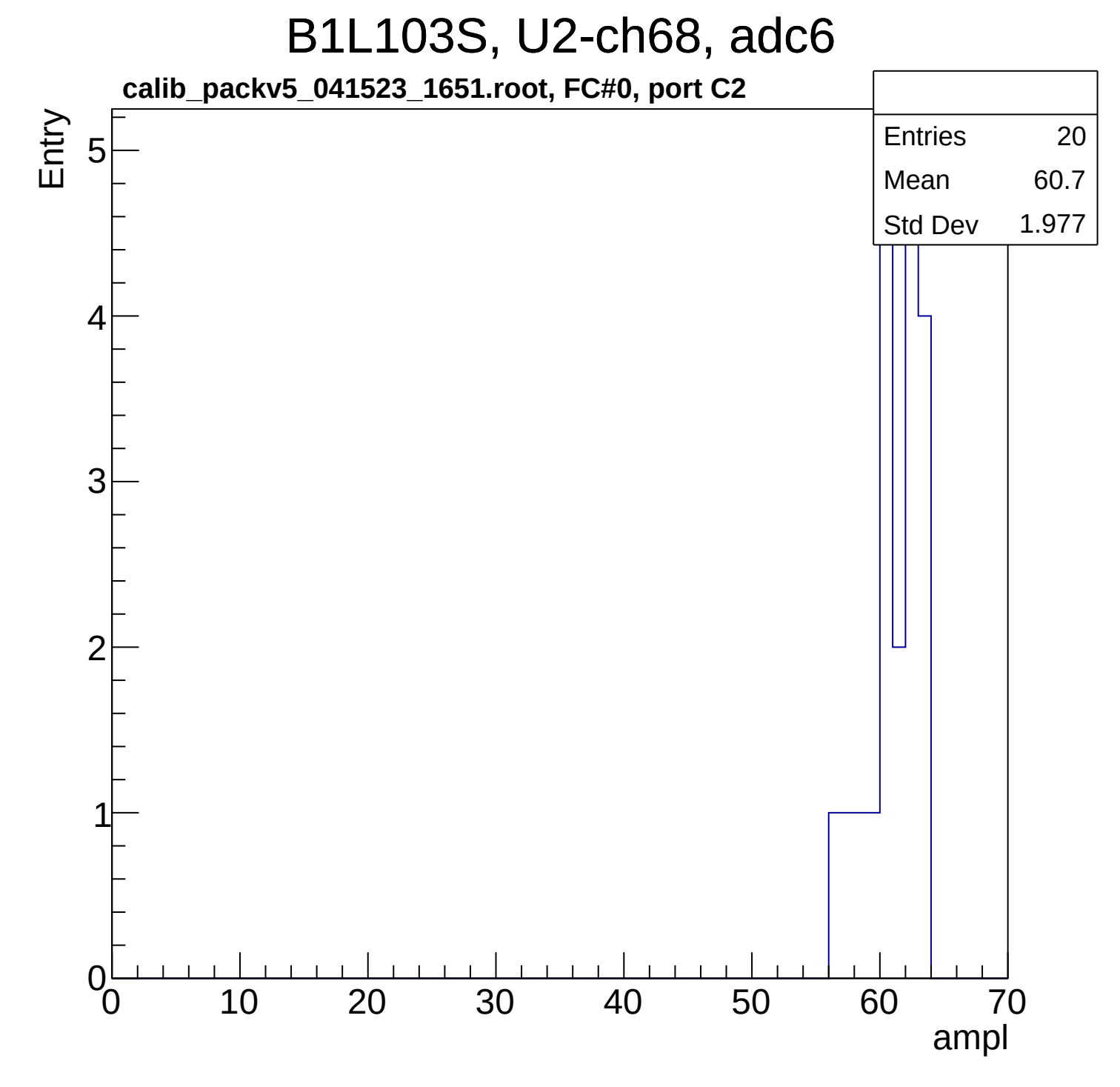

B1L103S, U2-ch68, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 34
Std Dev 3.356
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

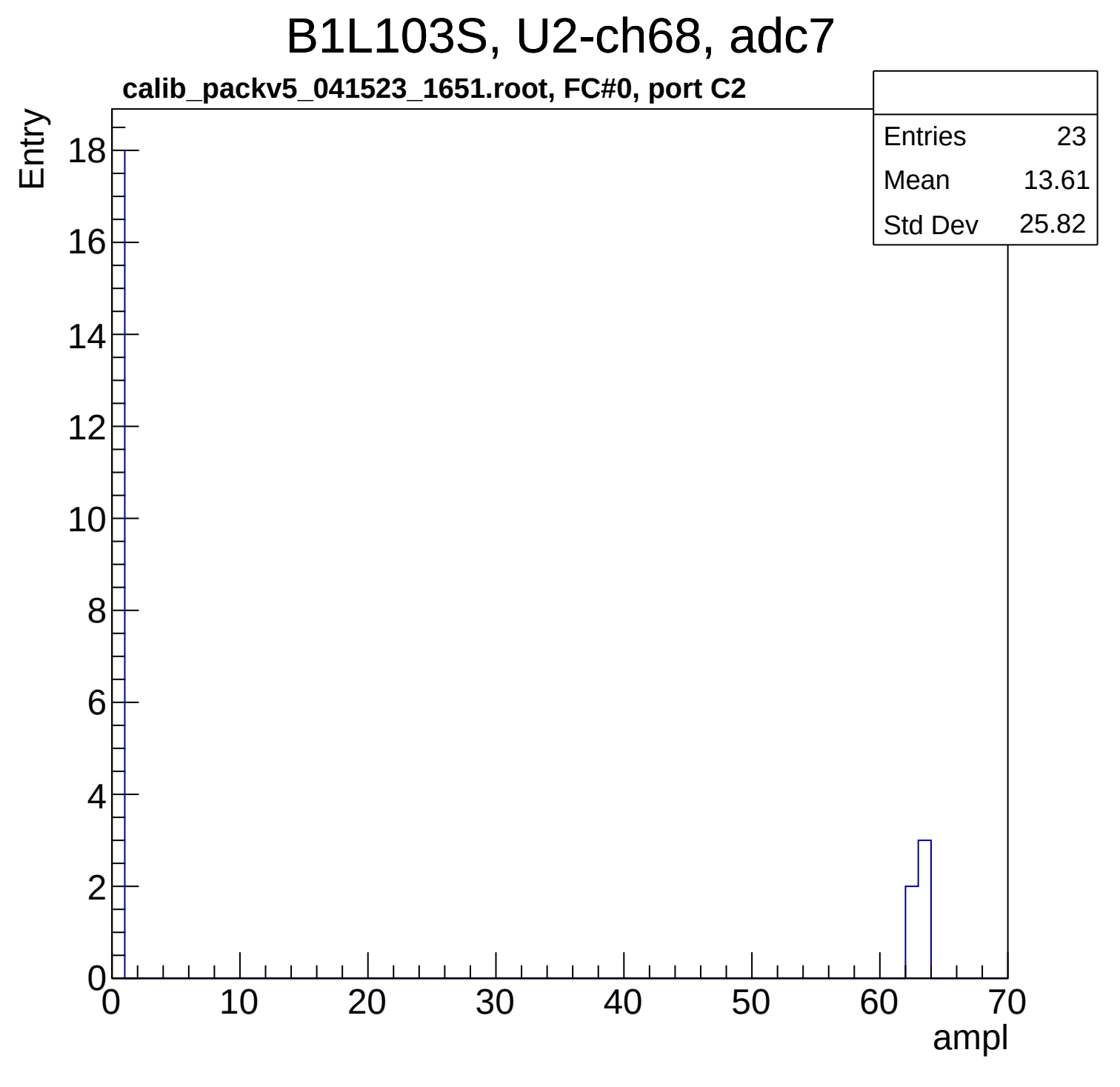

B1L103S, U2-ch68, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 37.49
Std Dev 10.52
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

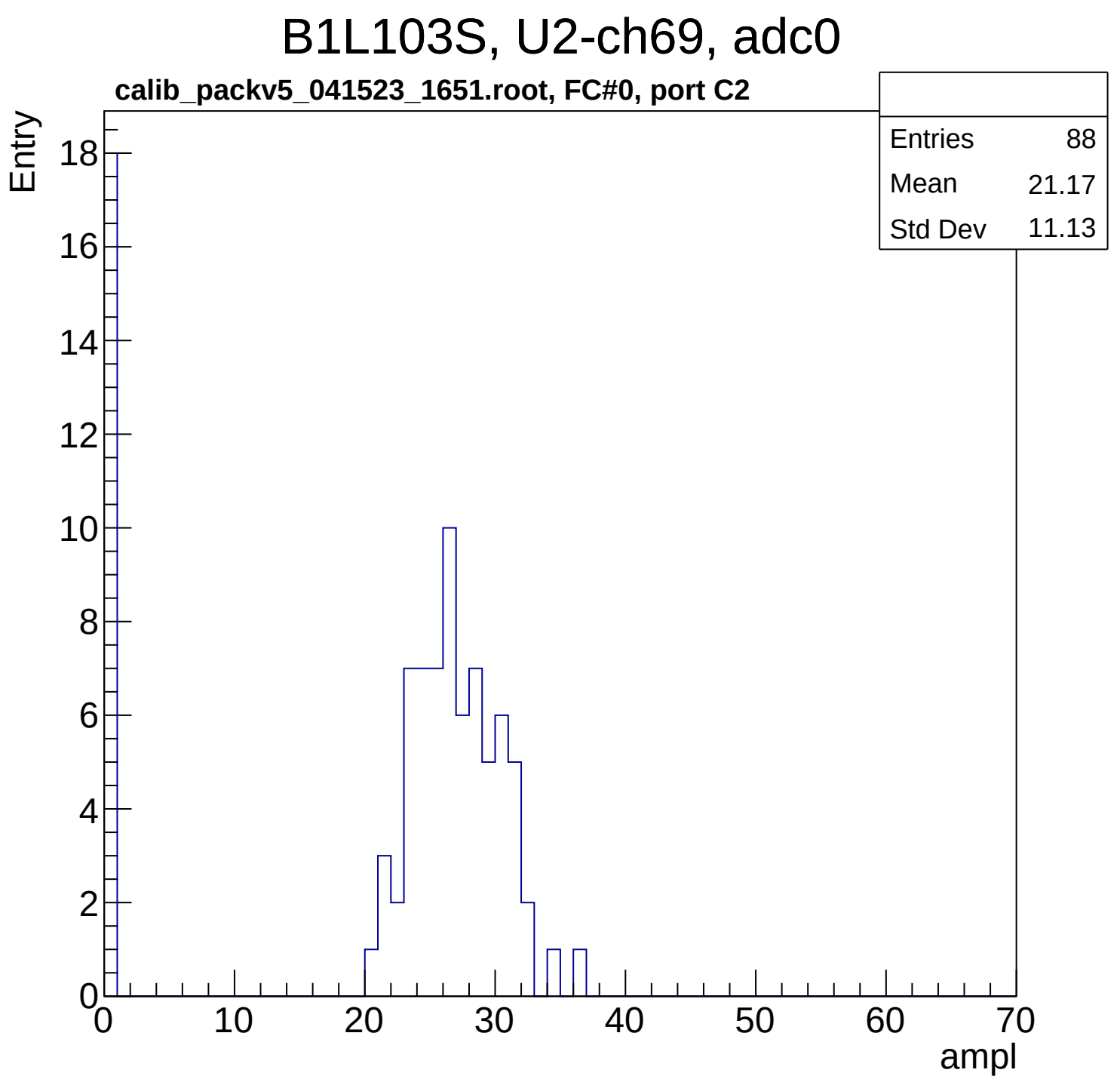

B1L103S, U2-ch68, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 39.79
Std Dev 17
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

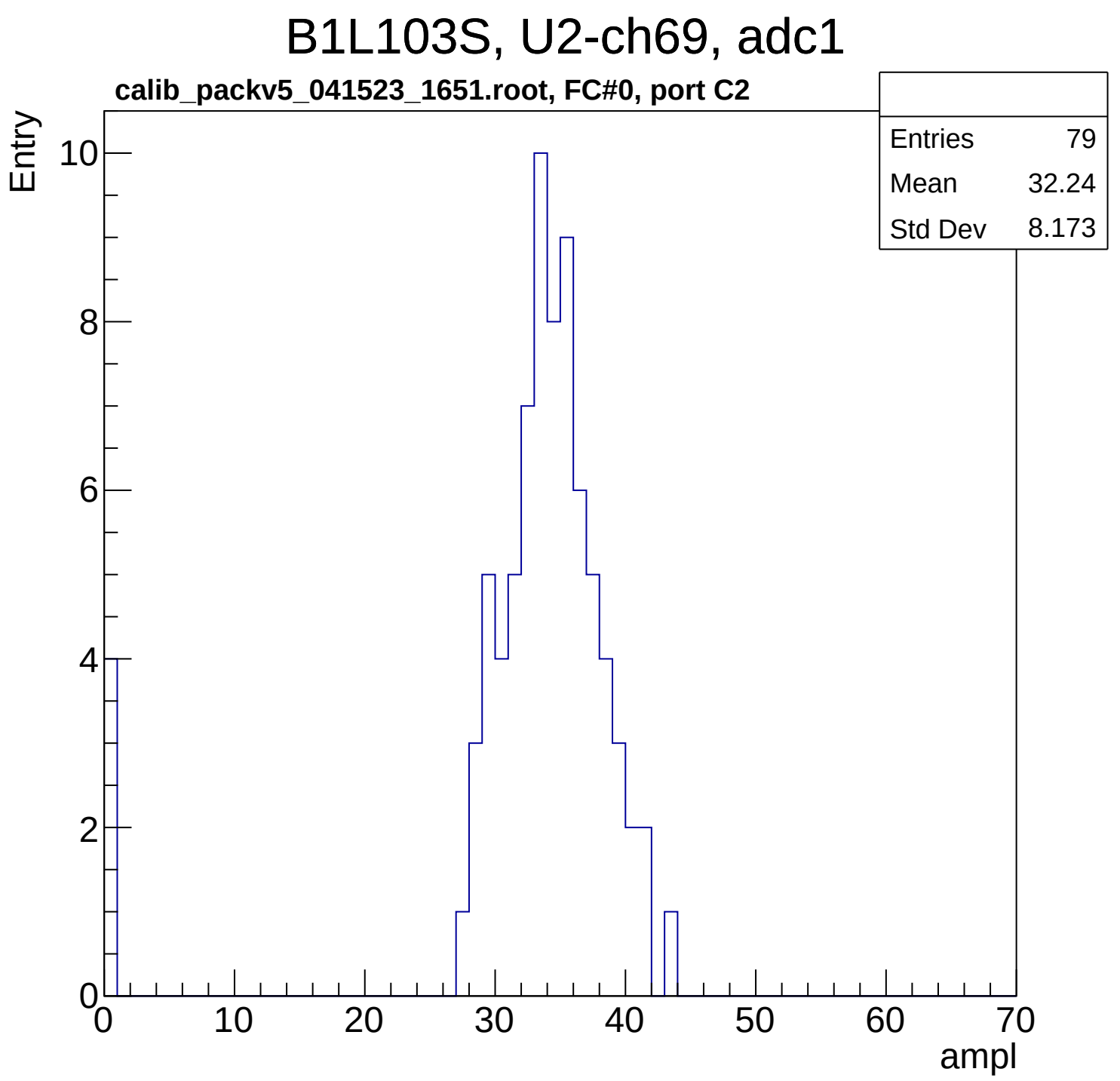

B1L103S, U2-ch68, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 52.35
Std Dev 3.793
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

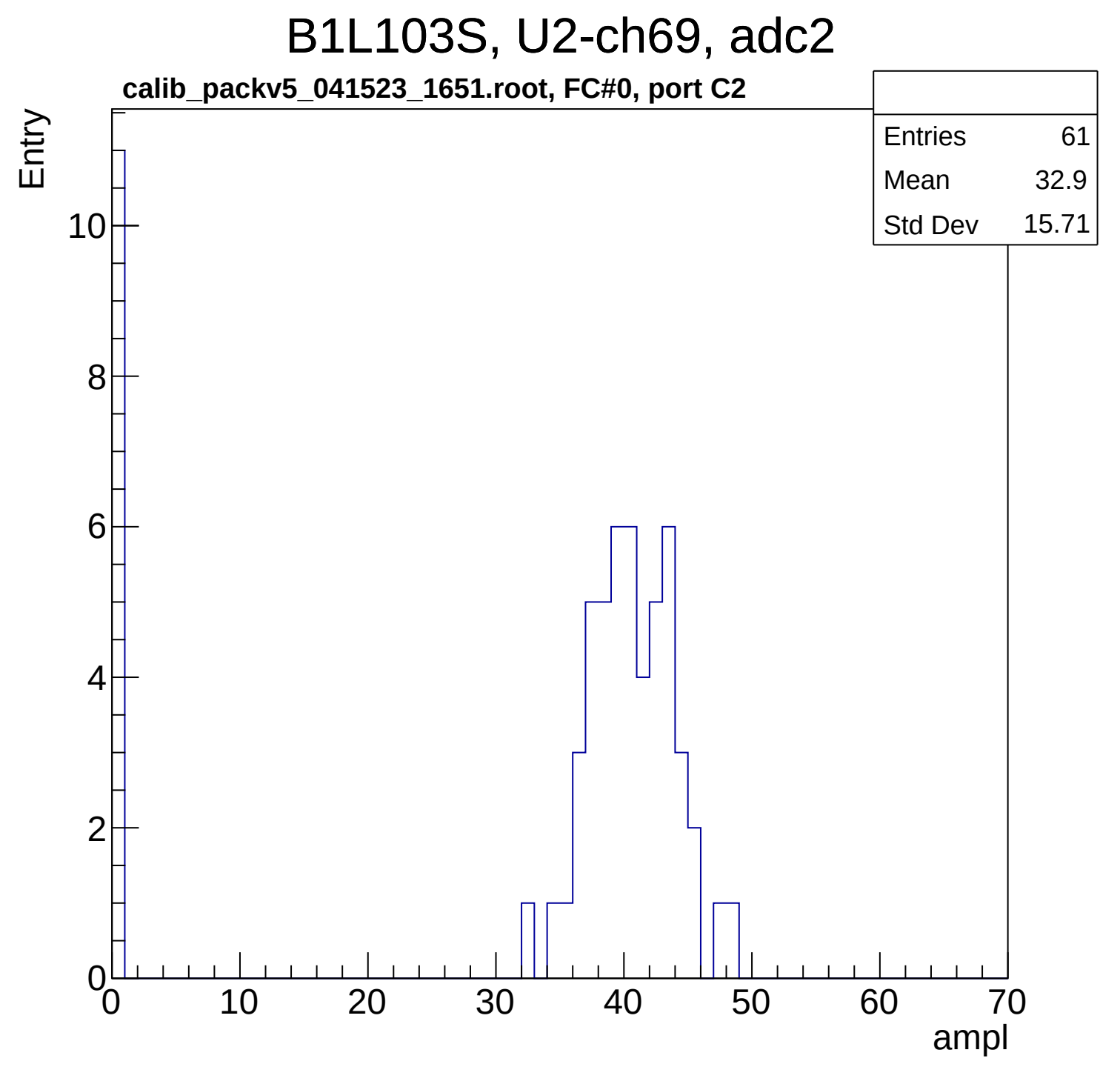

B1L103S, U2-ch68, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 56.98
Std Dev 8.37
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

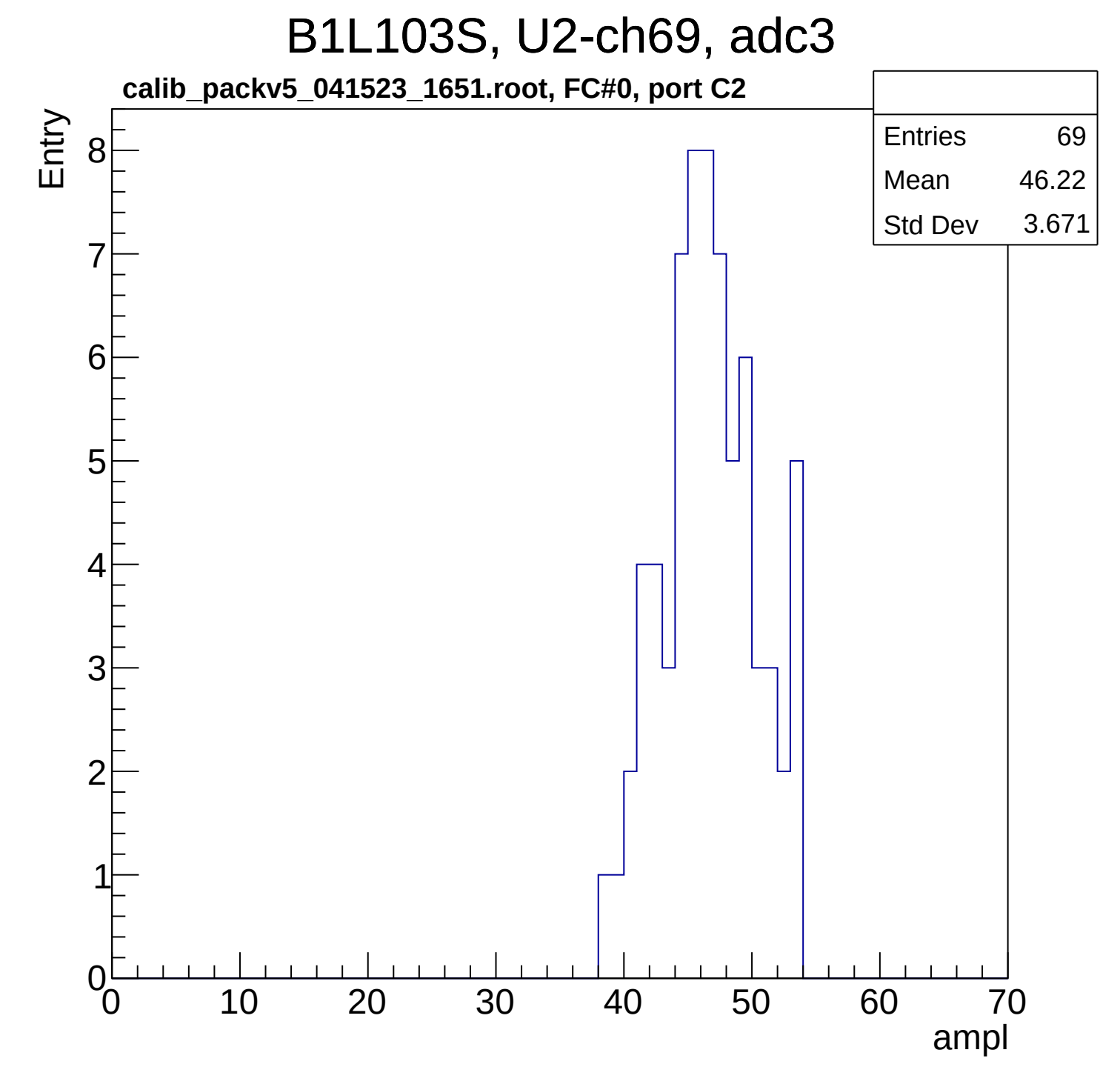

B1L103S, U2-ch68, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 60.7
Std Dev 1.977
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

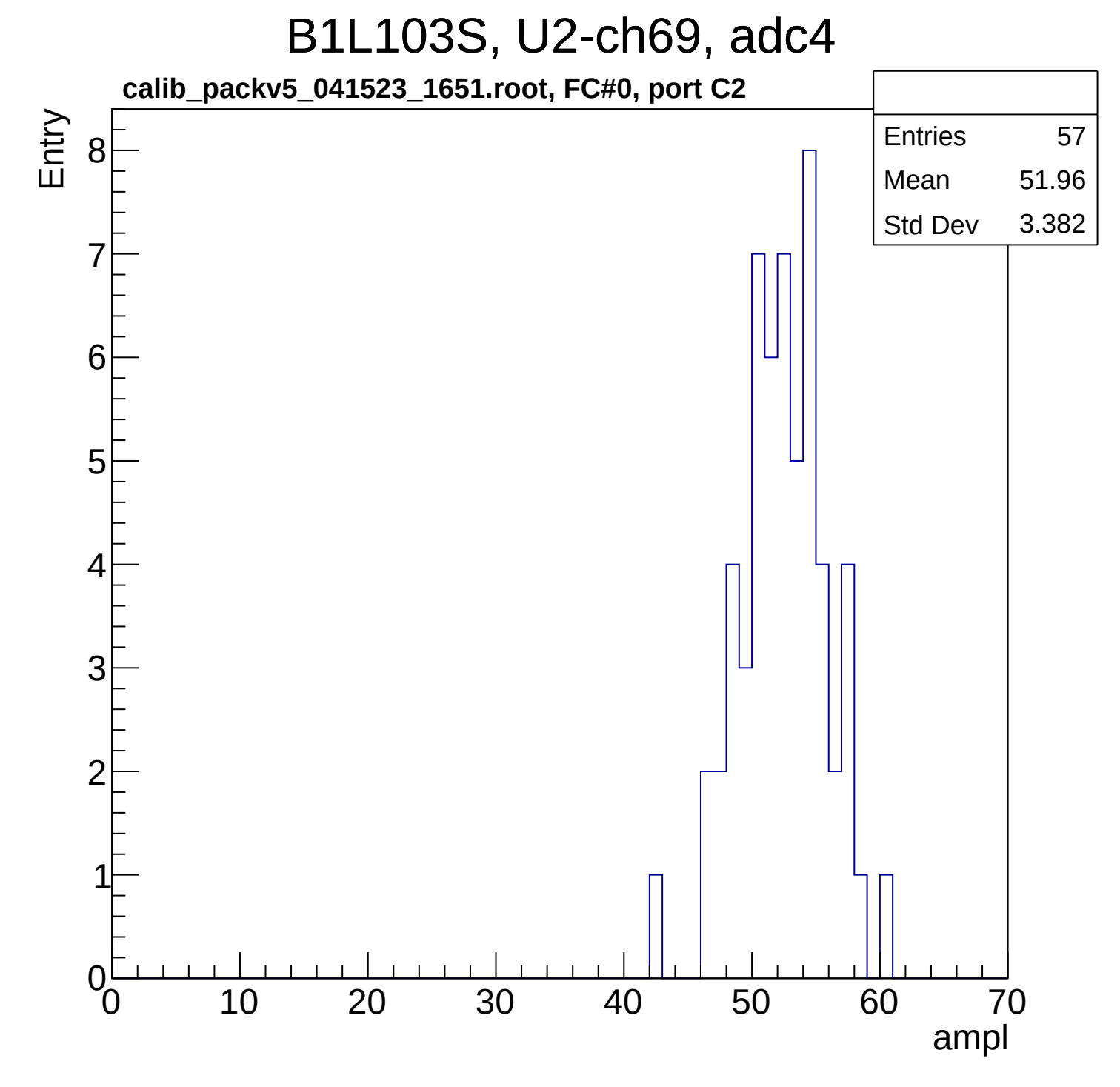

B1L103S, U2-ch68, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 13.61
Std Dev 25.82
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

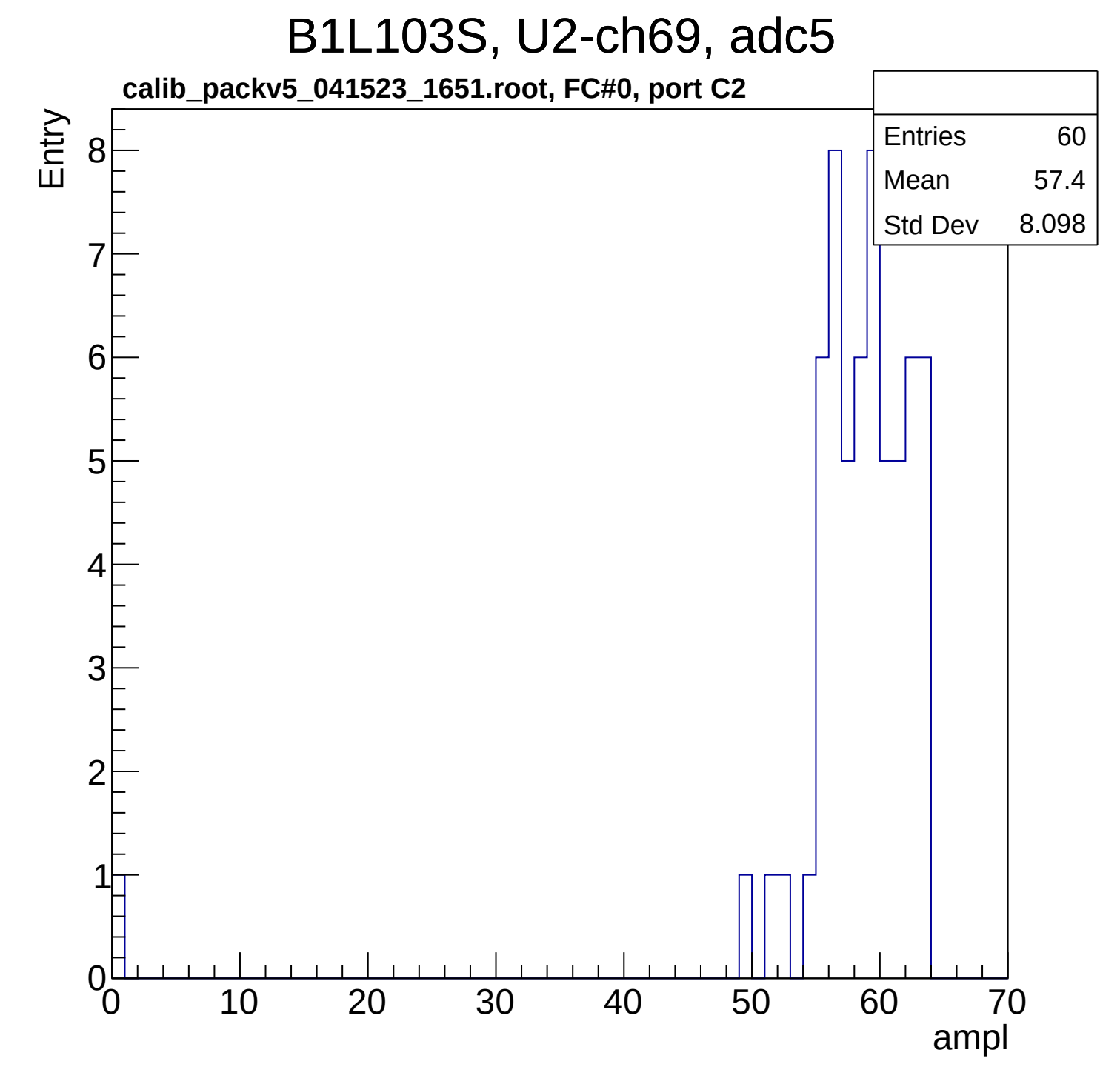

B1L103S, U2-ch69, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 21.17
Std Dev 11.13
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

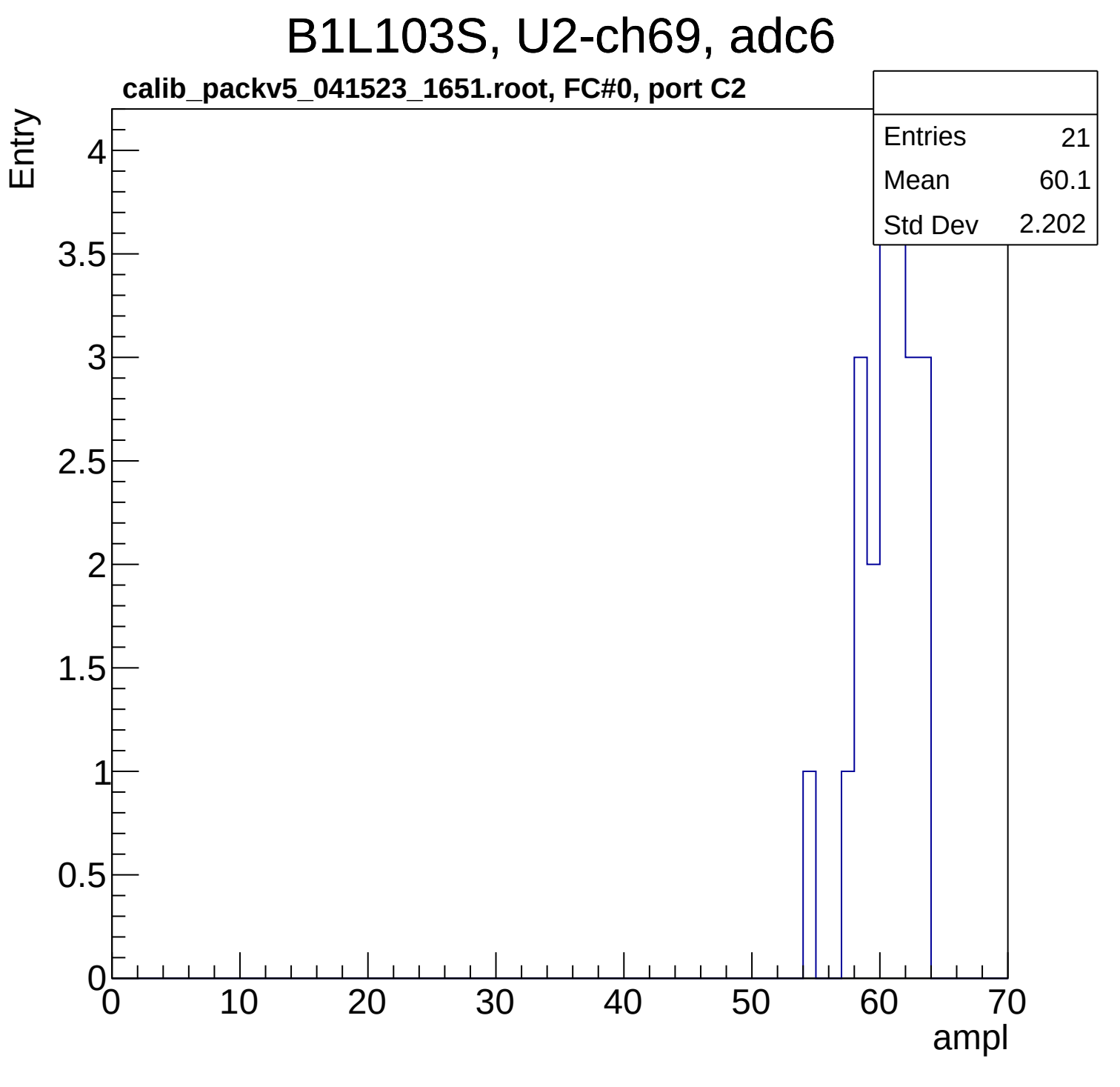

B1L103S, U2-ch69, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 32.24
Std Dev 8.173
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

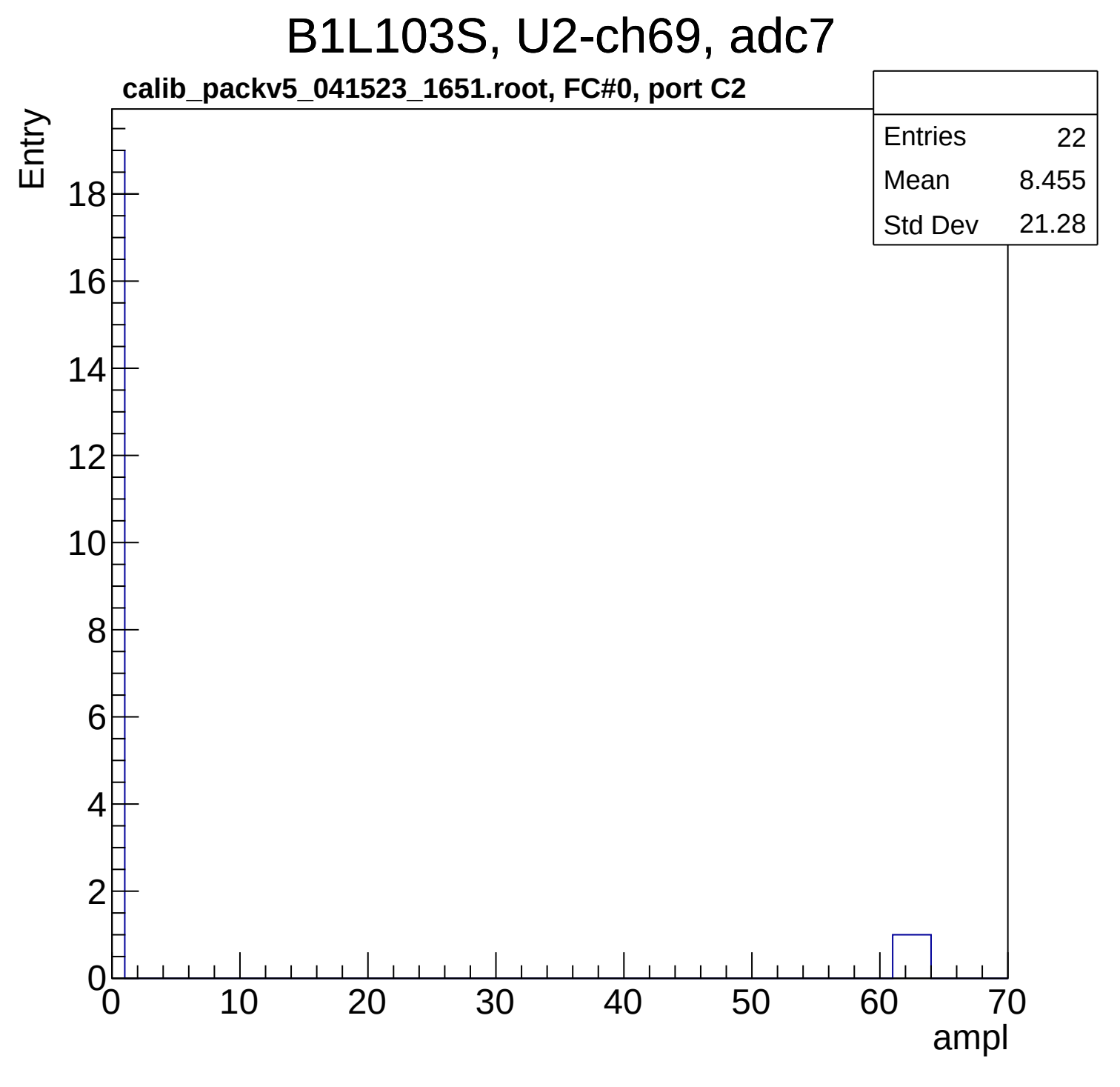

B1L103S, U2-ch69, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 32.9
Std Dev 15.71
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

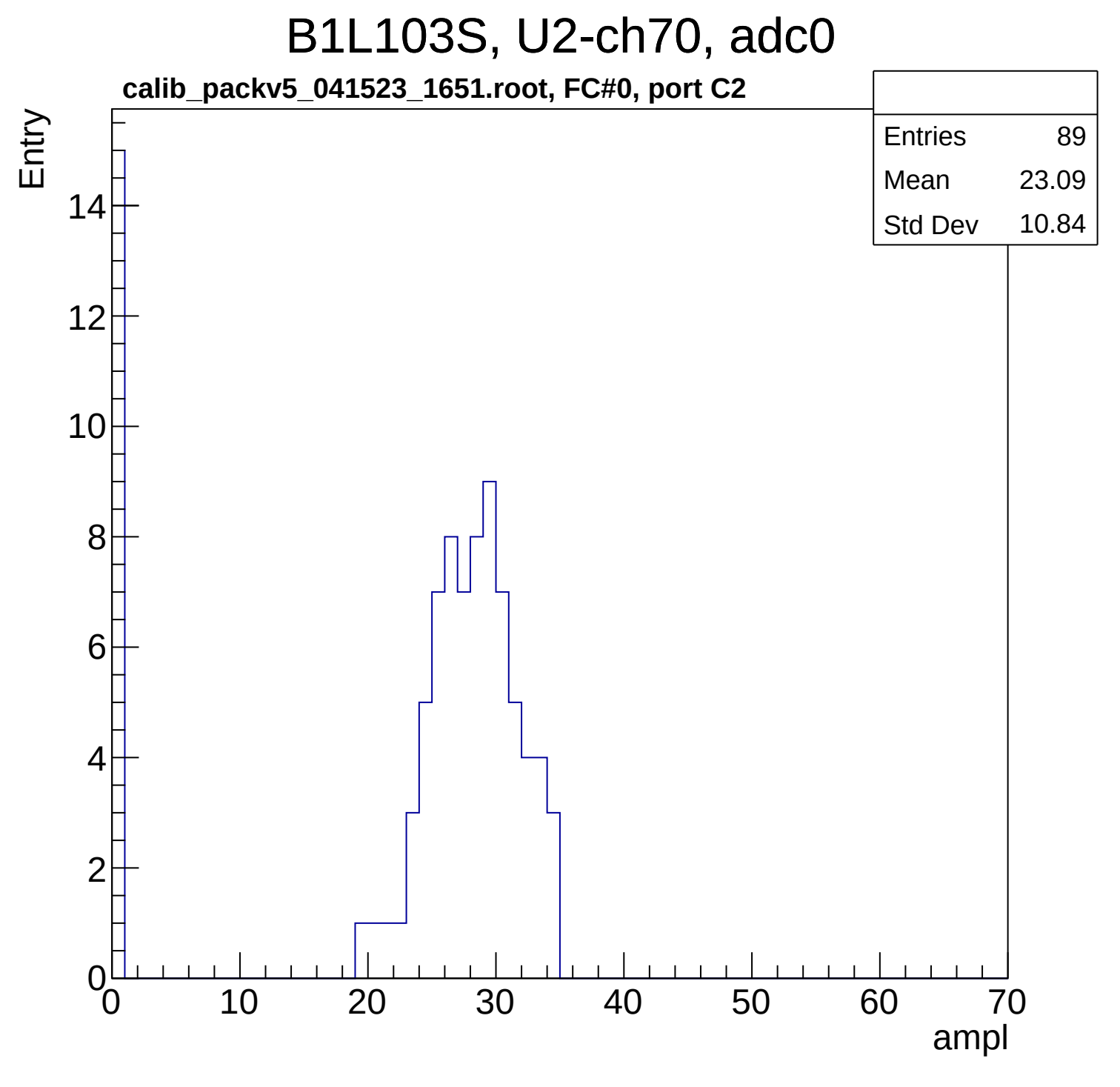

B1L103S, U2-ch69, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 46.22
Std Dev 3.671
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

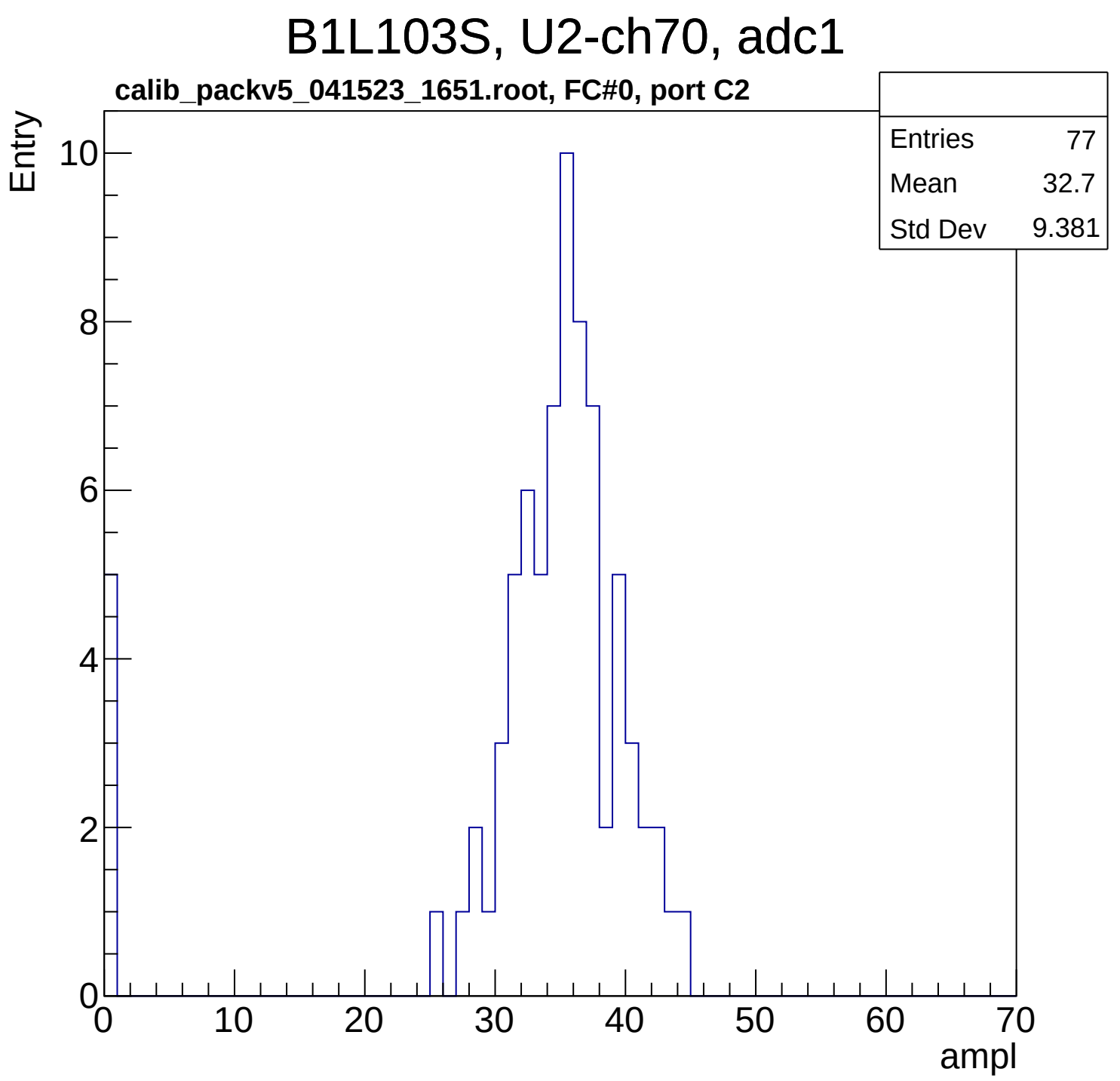

B1L103S, U2-ch69, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 51.96
Std Dev 3.382
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

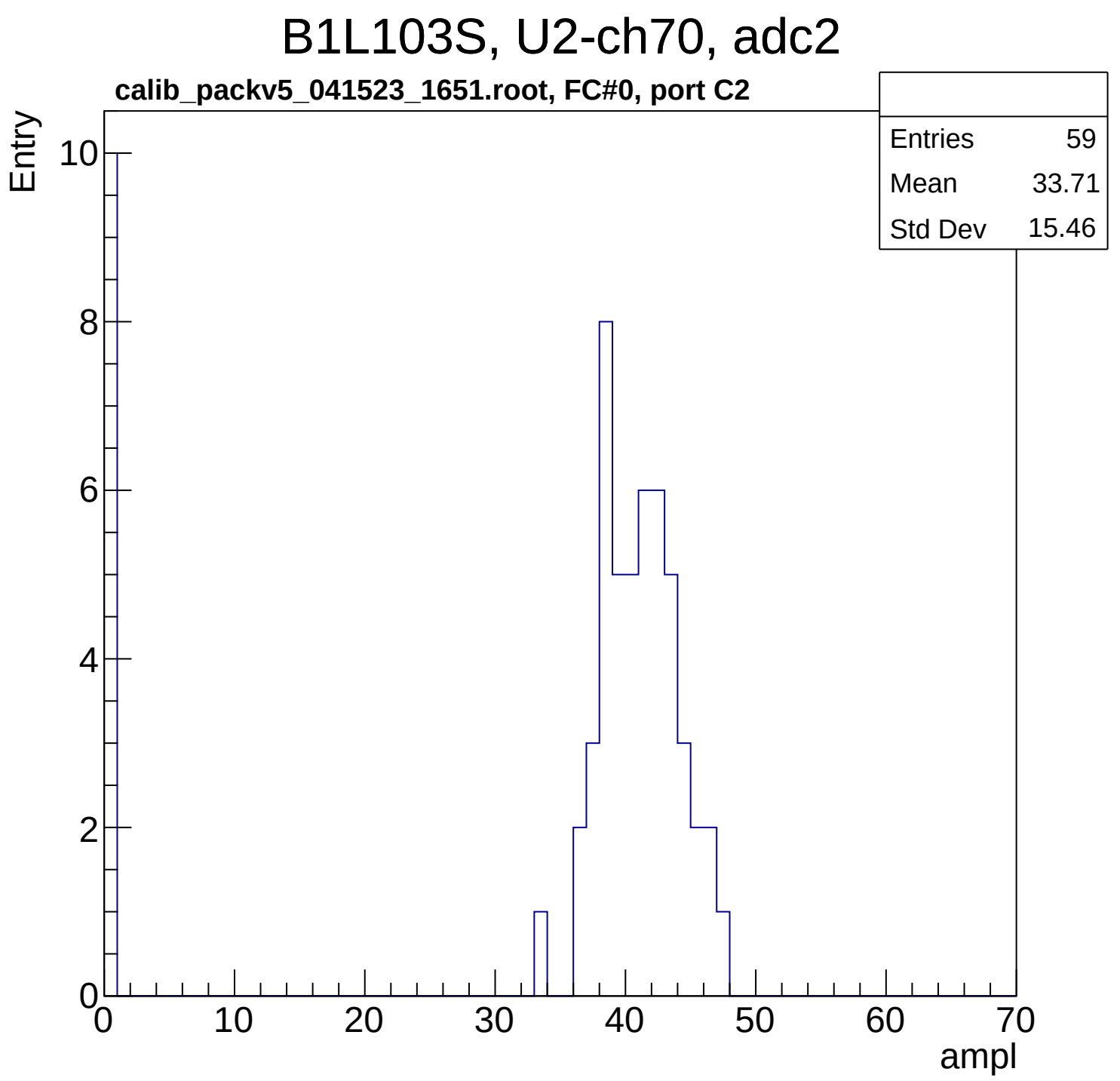

B1L103S, U2-ch69, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 57.4
Std Dev 8.098
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

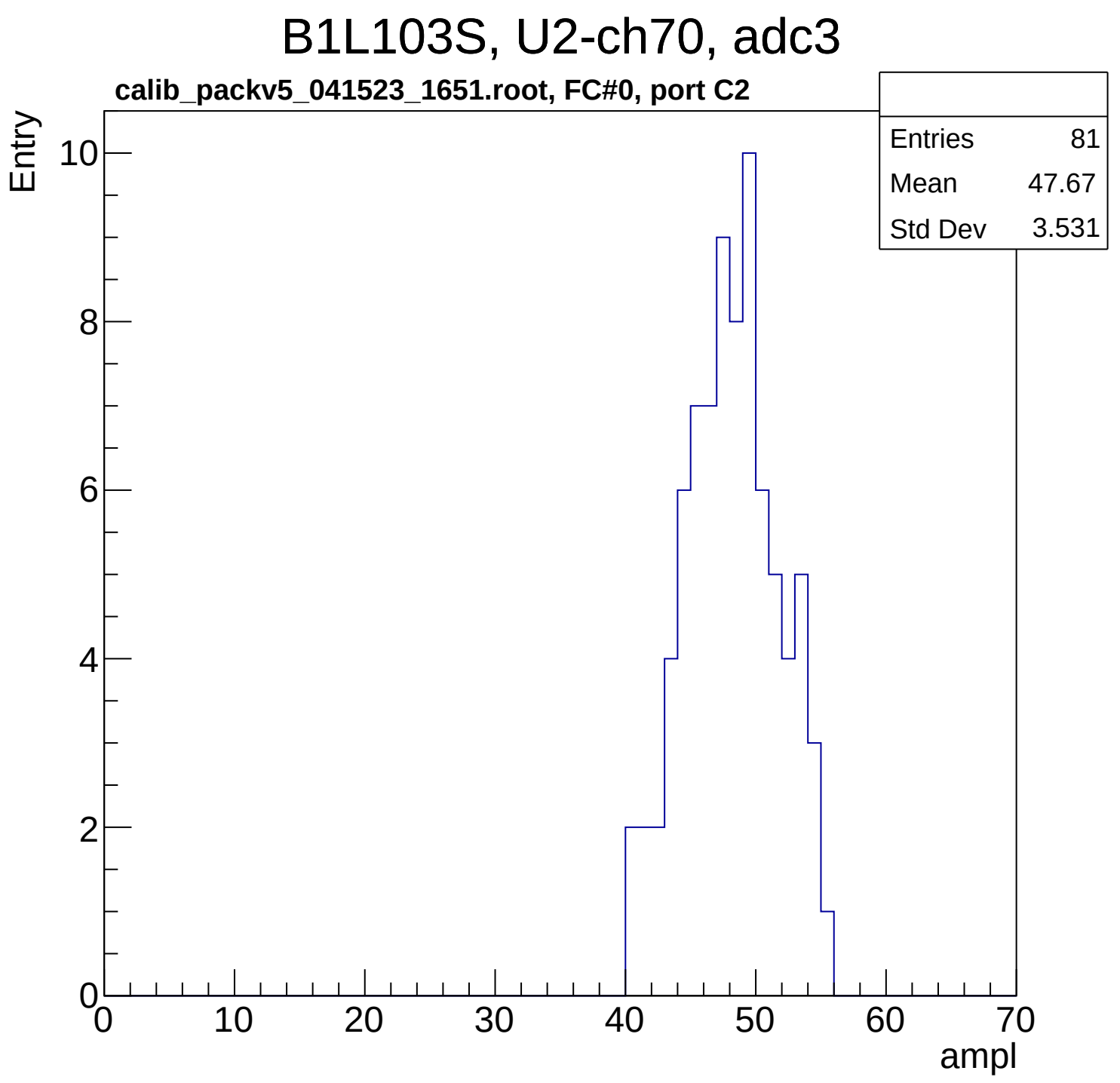

B1L103S, U2-ch69, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 60.1
Std Dev 2.202
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

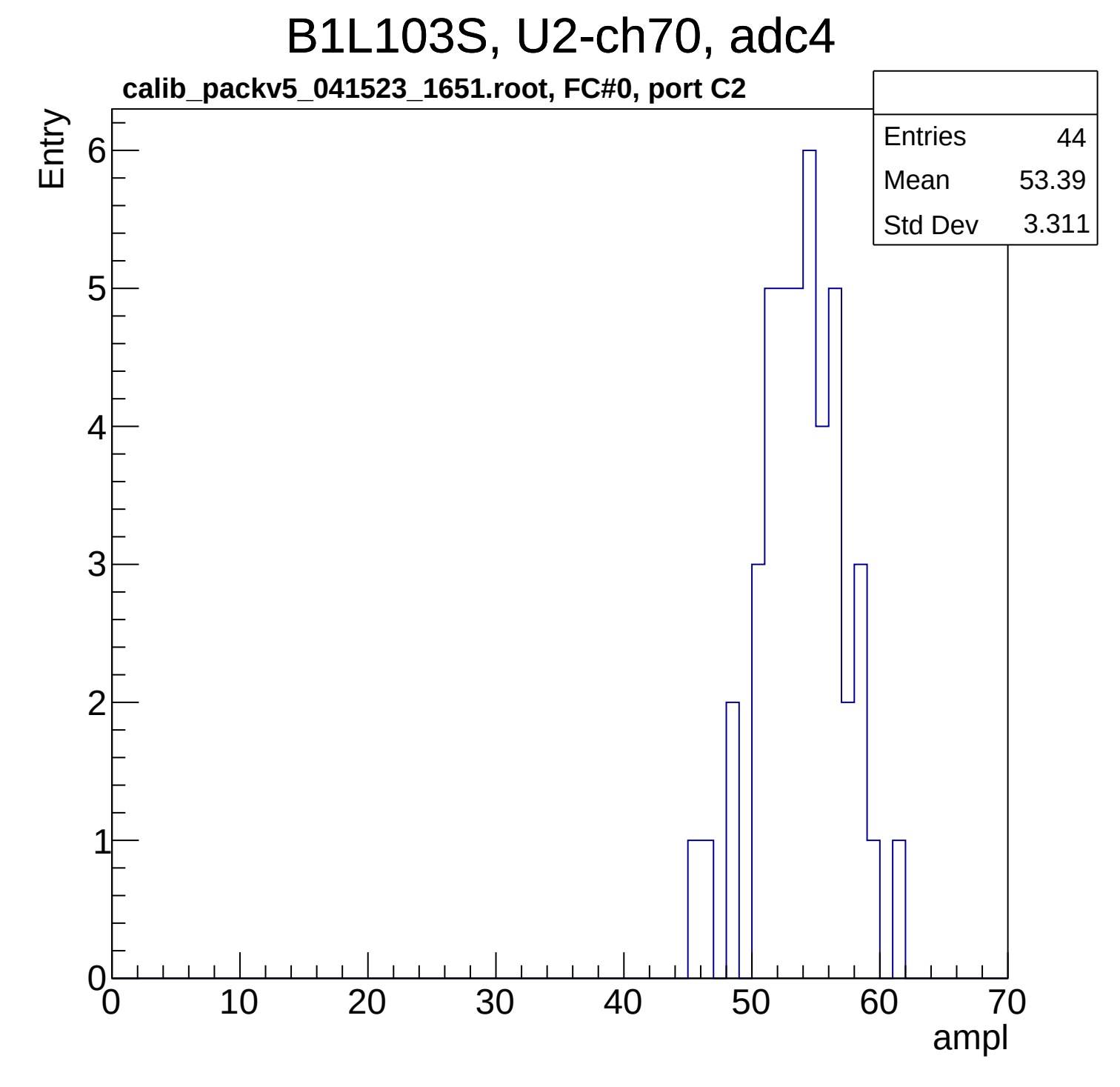

B1L103S, U2-ch69, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.455
Std Dev 21.28
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

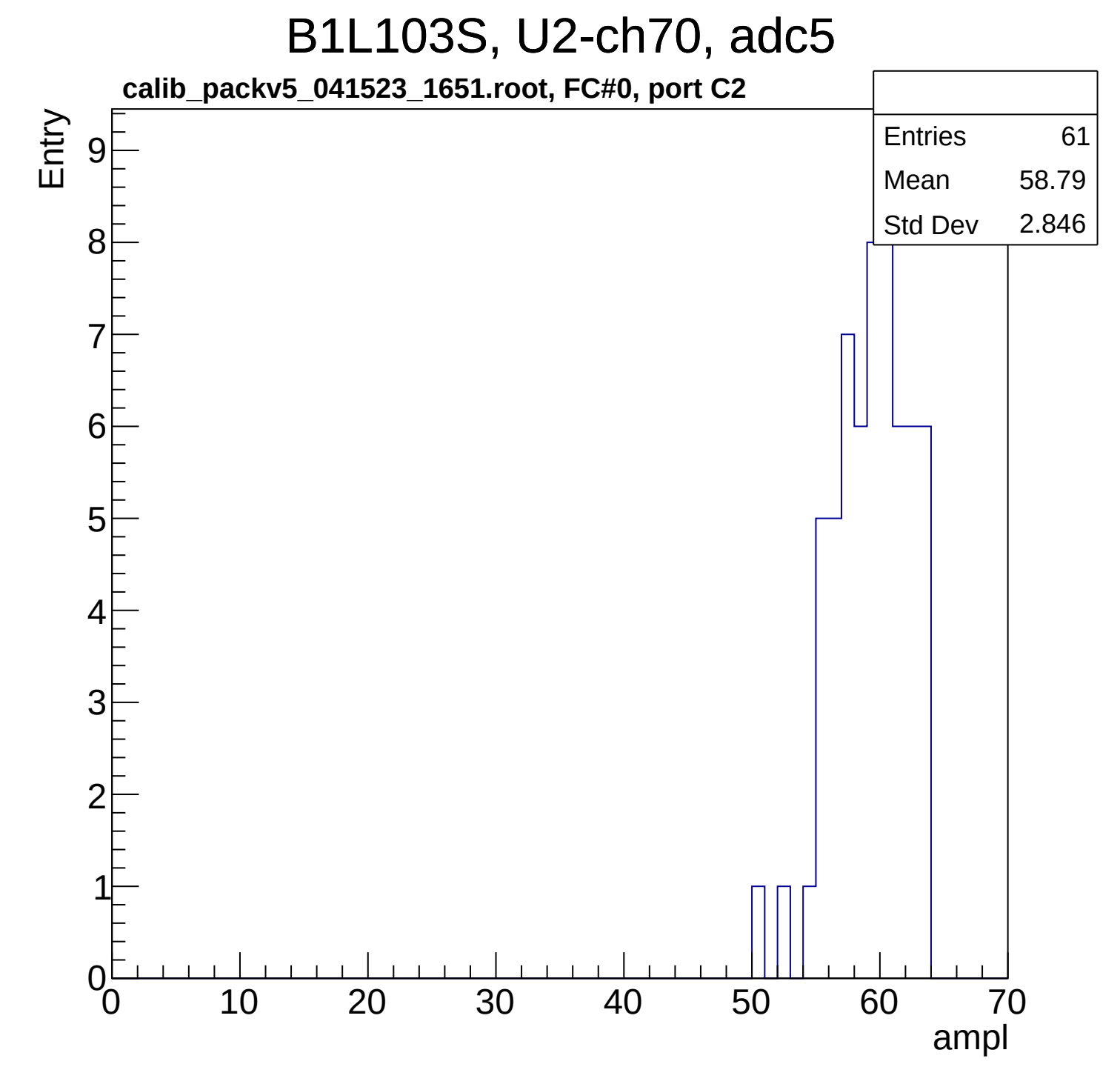

B1L103S, U2-ch70, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 23.09
Std Dev 10.84
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

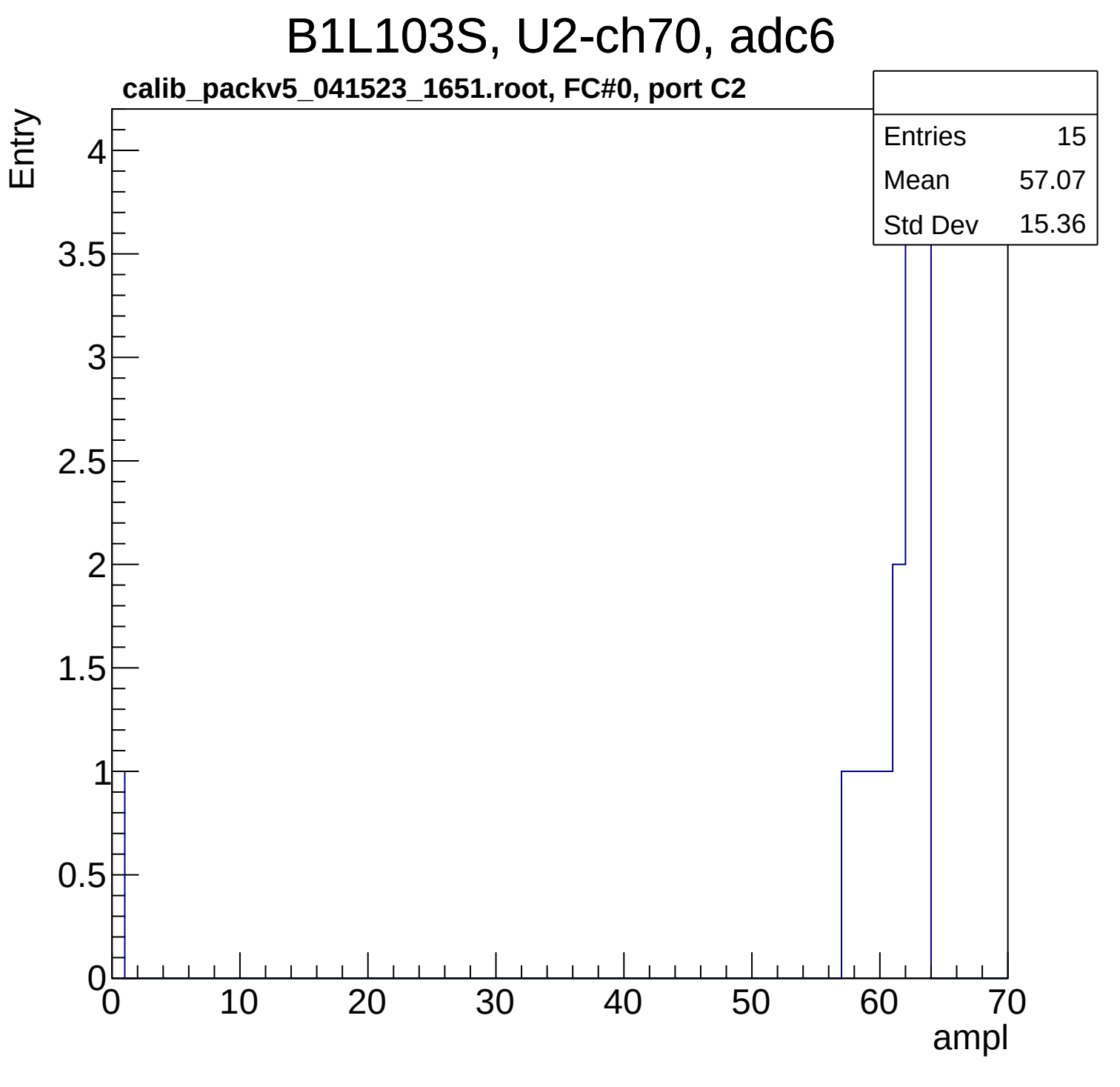

B1L103S, U2-ch70, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 32.7
Std Dev 9.381
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

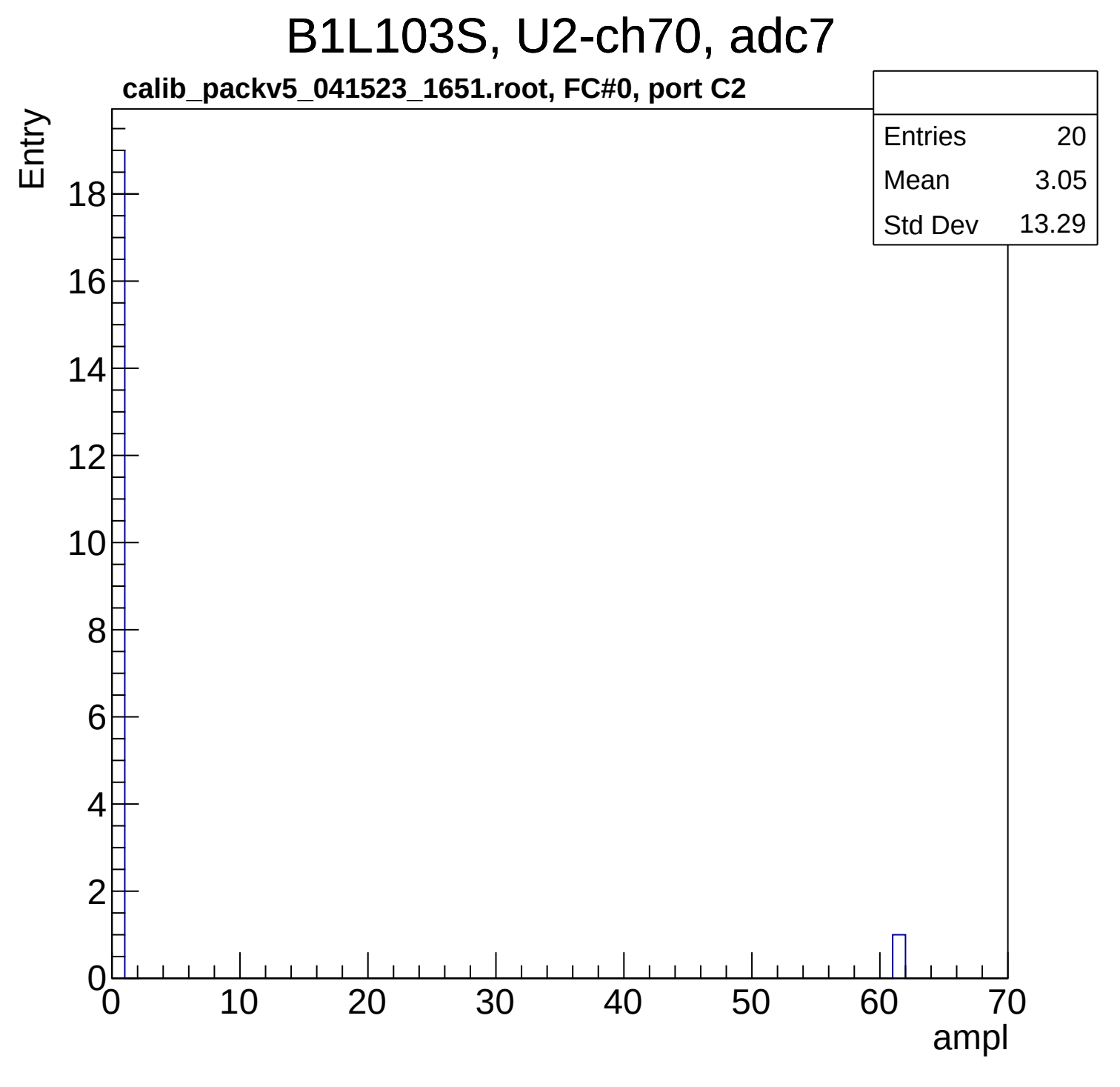

B1L103S, U2-ch70, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 33.71
Std Dev 15.46
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

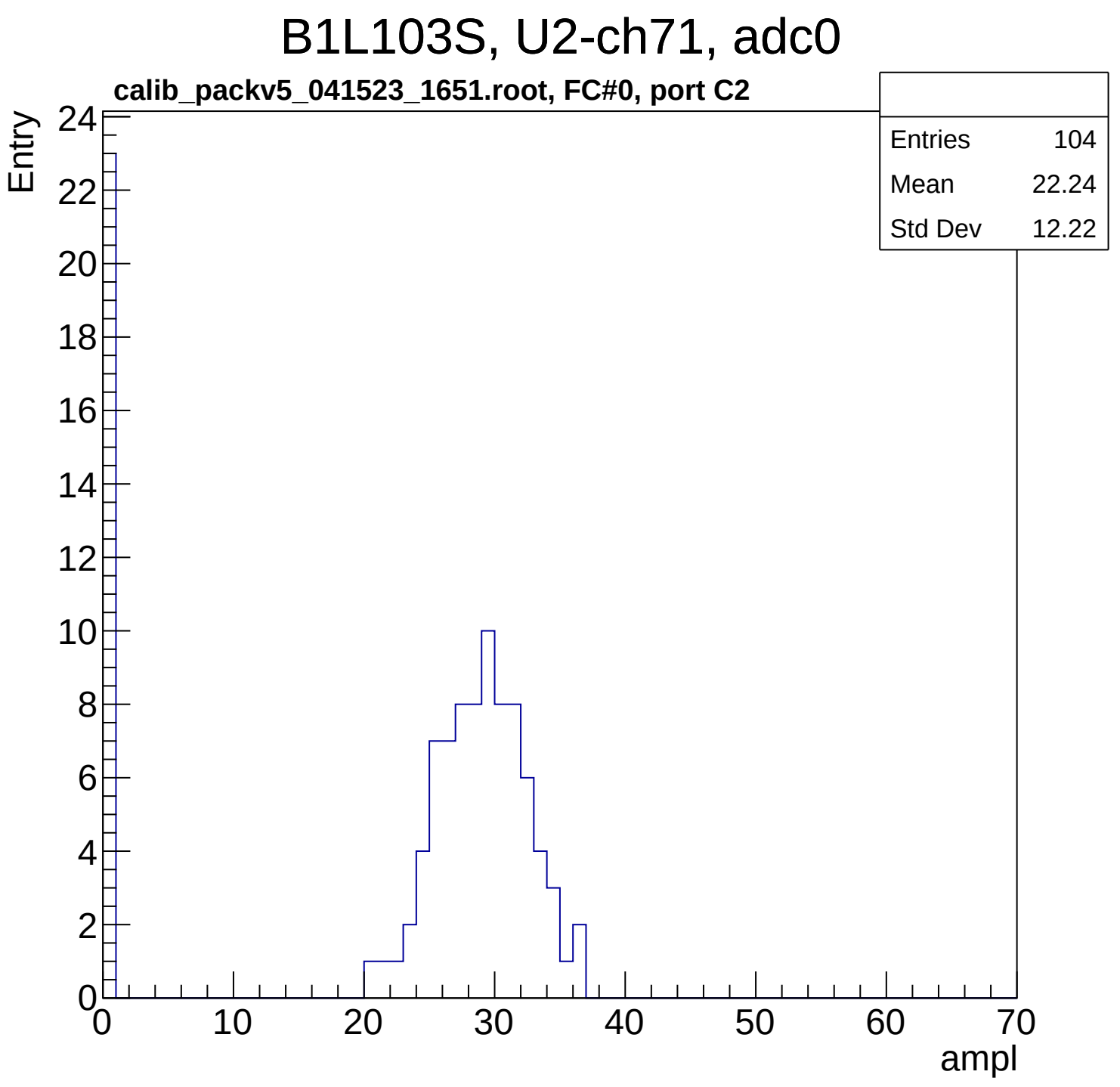

B1L103S, U2-ch70, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 47.67
Std Dev 3.531
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

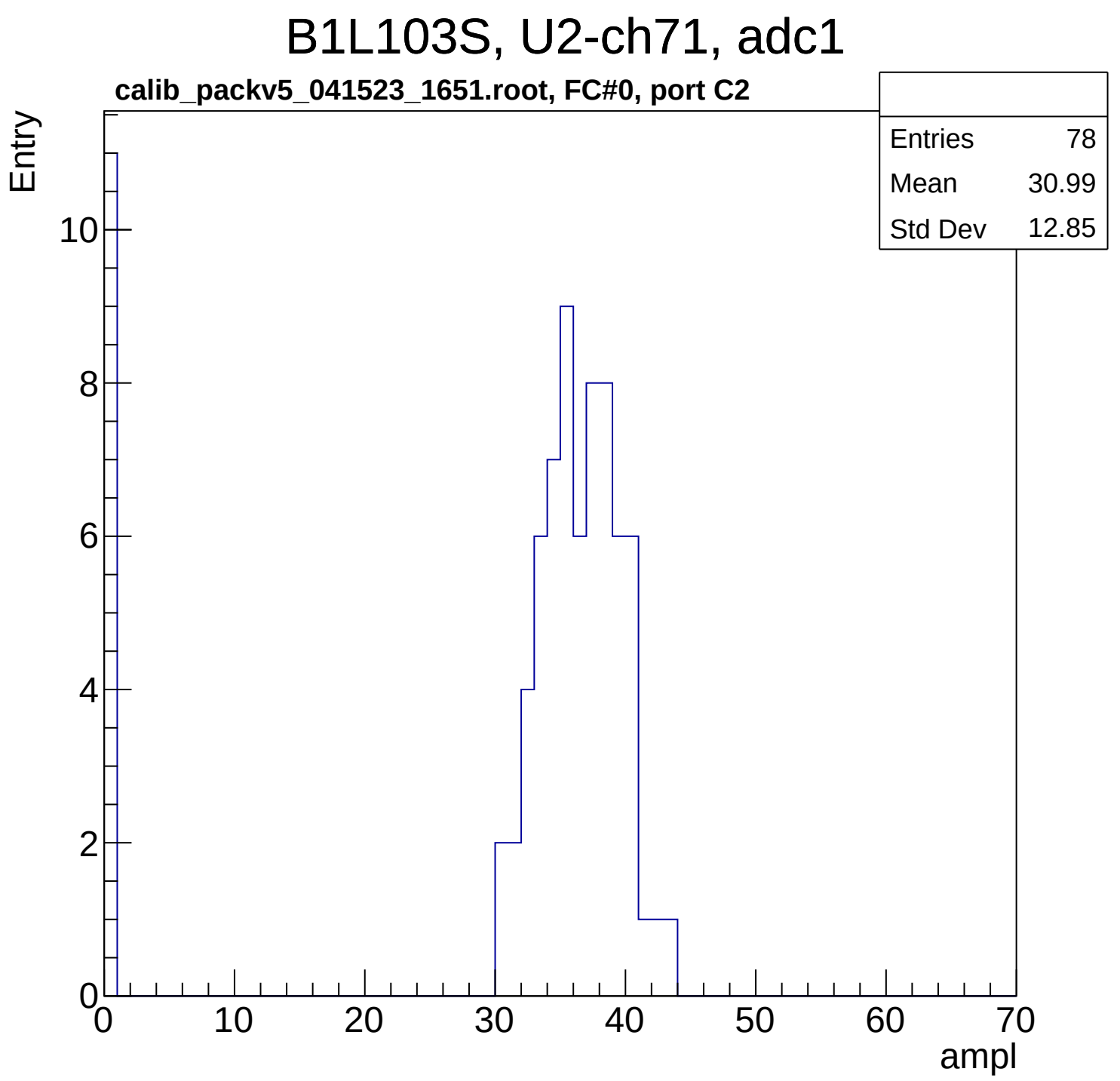

B1L103S, U2-ch70, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 53.39
Std Dev 3.311
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

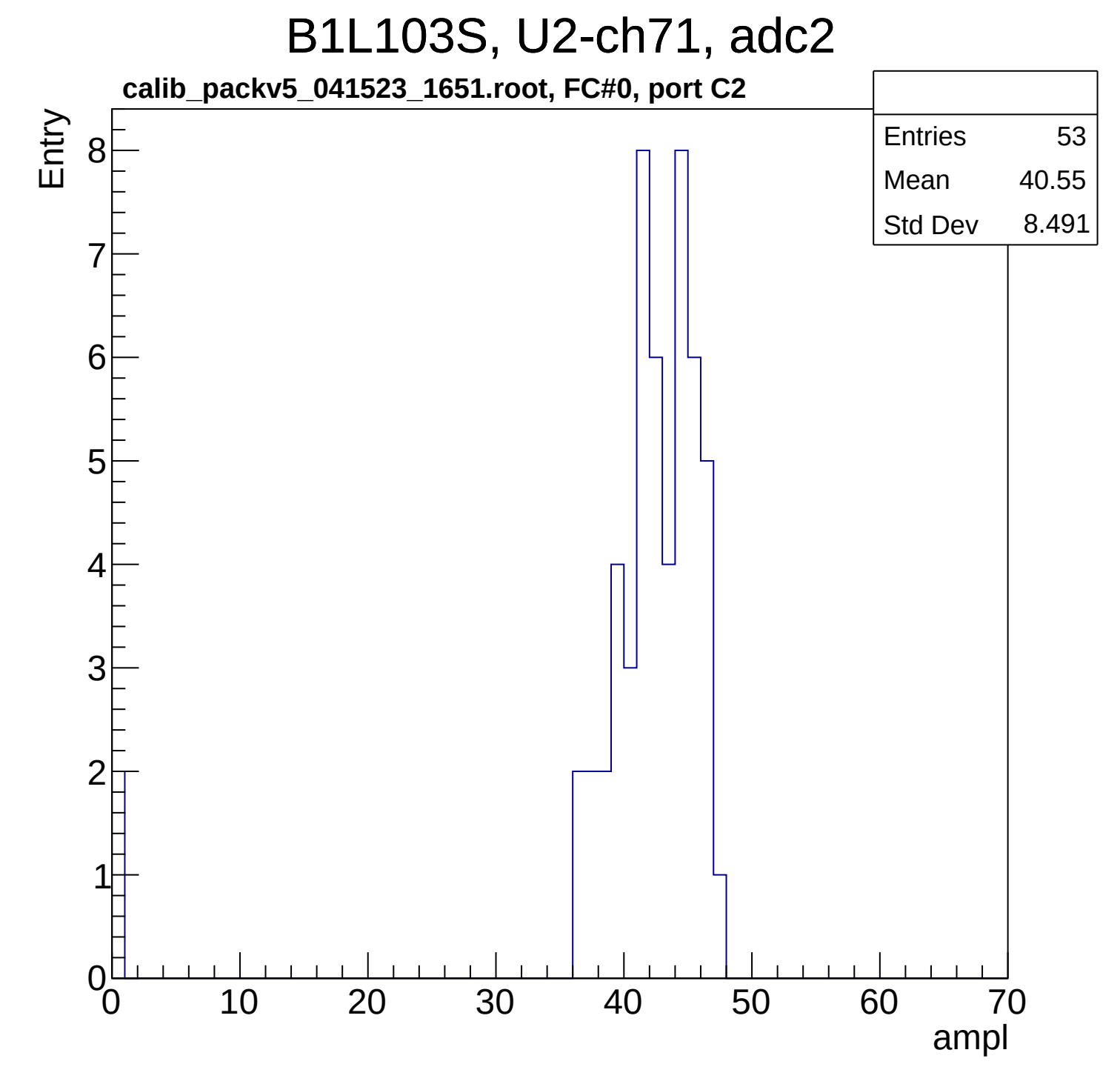

B1L103S, U2-ch70, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 58.79
Std Dev 2.846
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

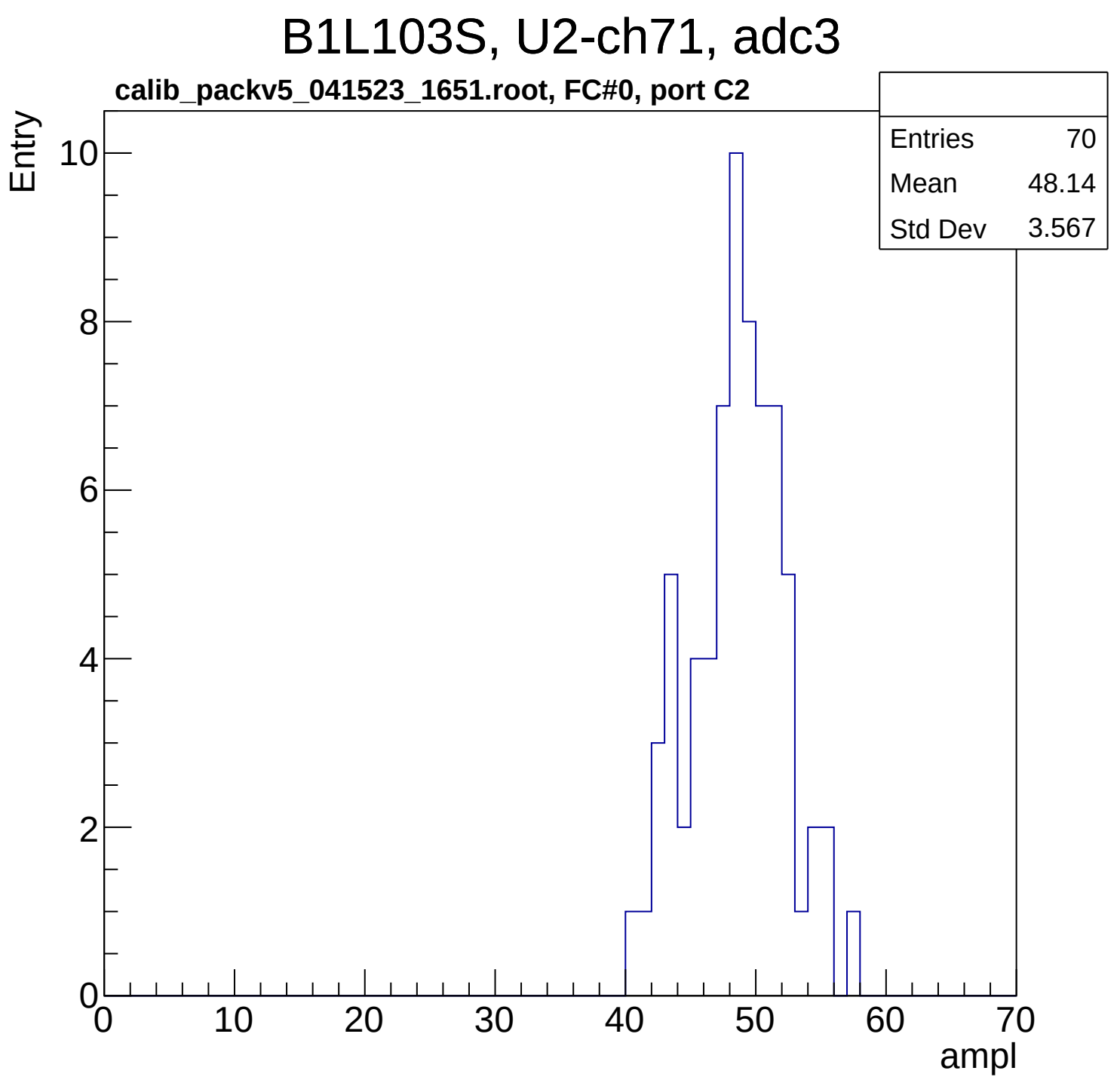

B1L103S, U2-ch70, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 57.07
Std Dev 15.36
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

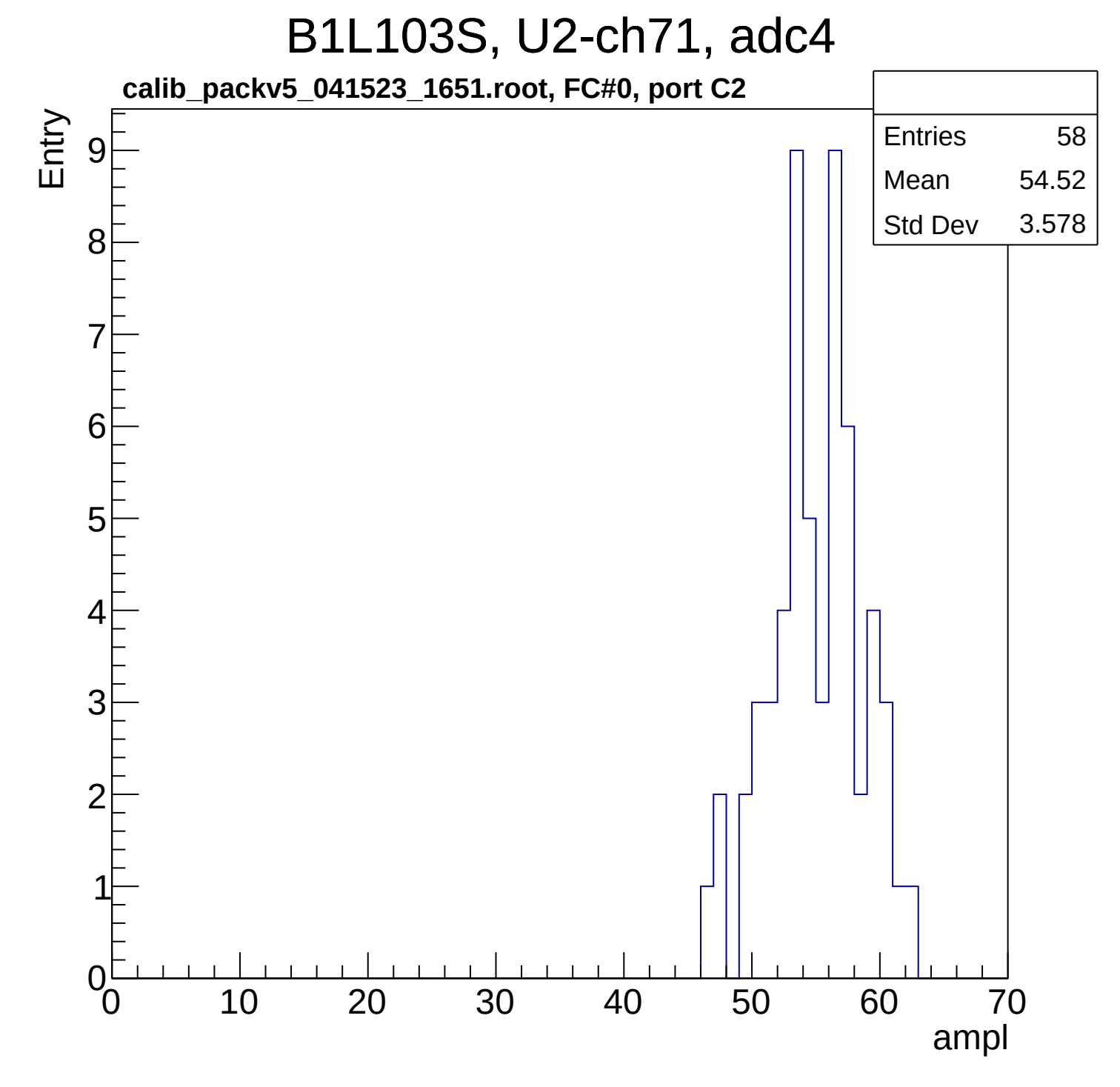

B1L103S, U2-ch70, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

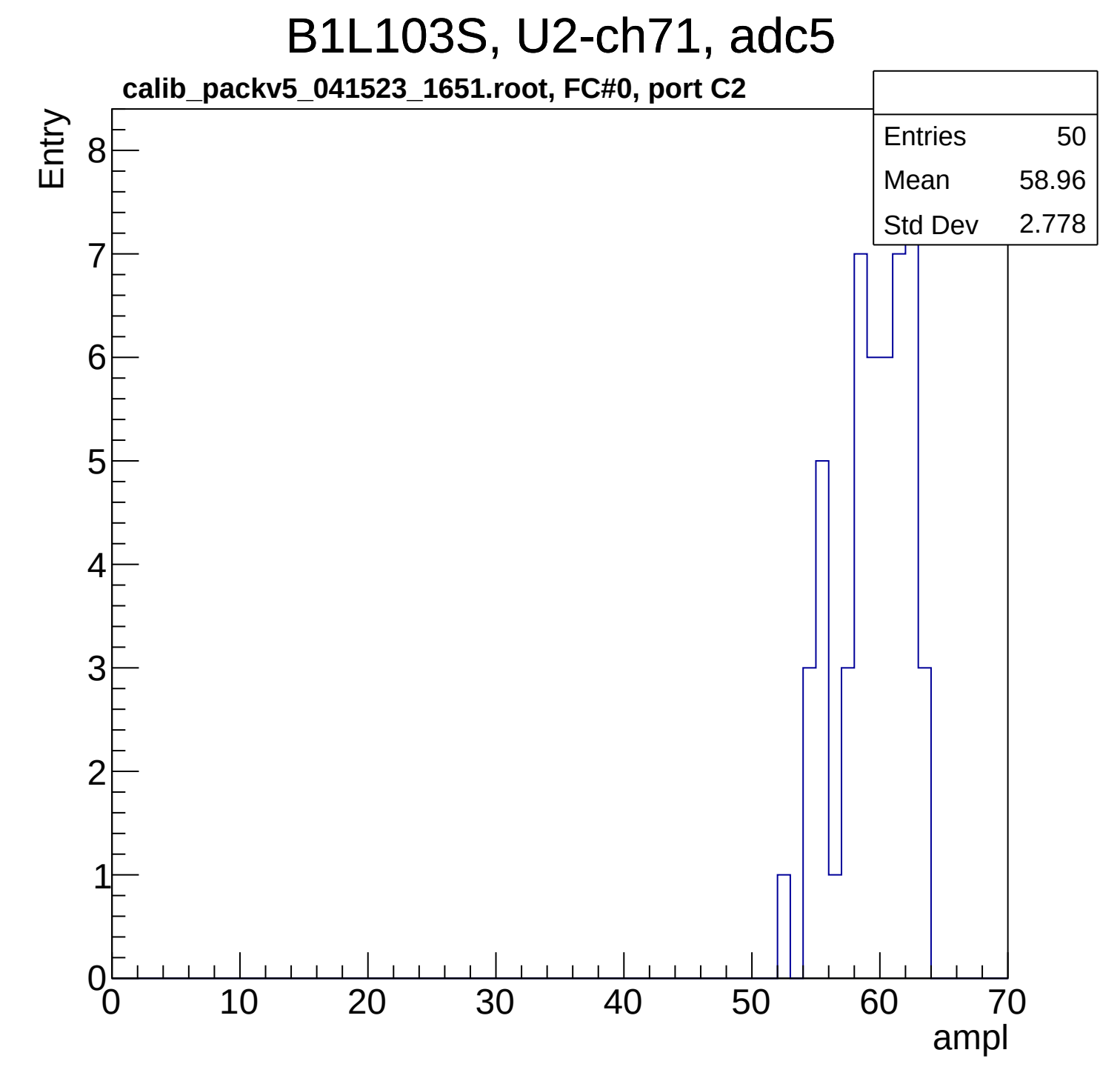

B1L103S, U2-ch71, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 22.24
Std Dev 12.22
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70

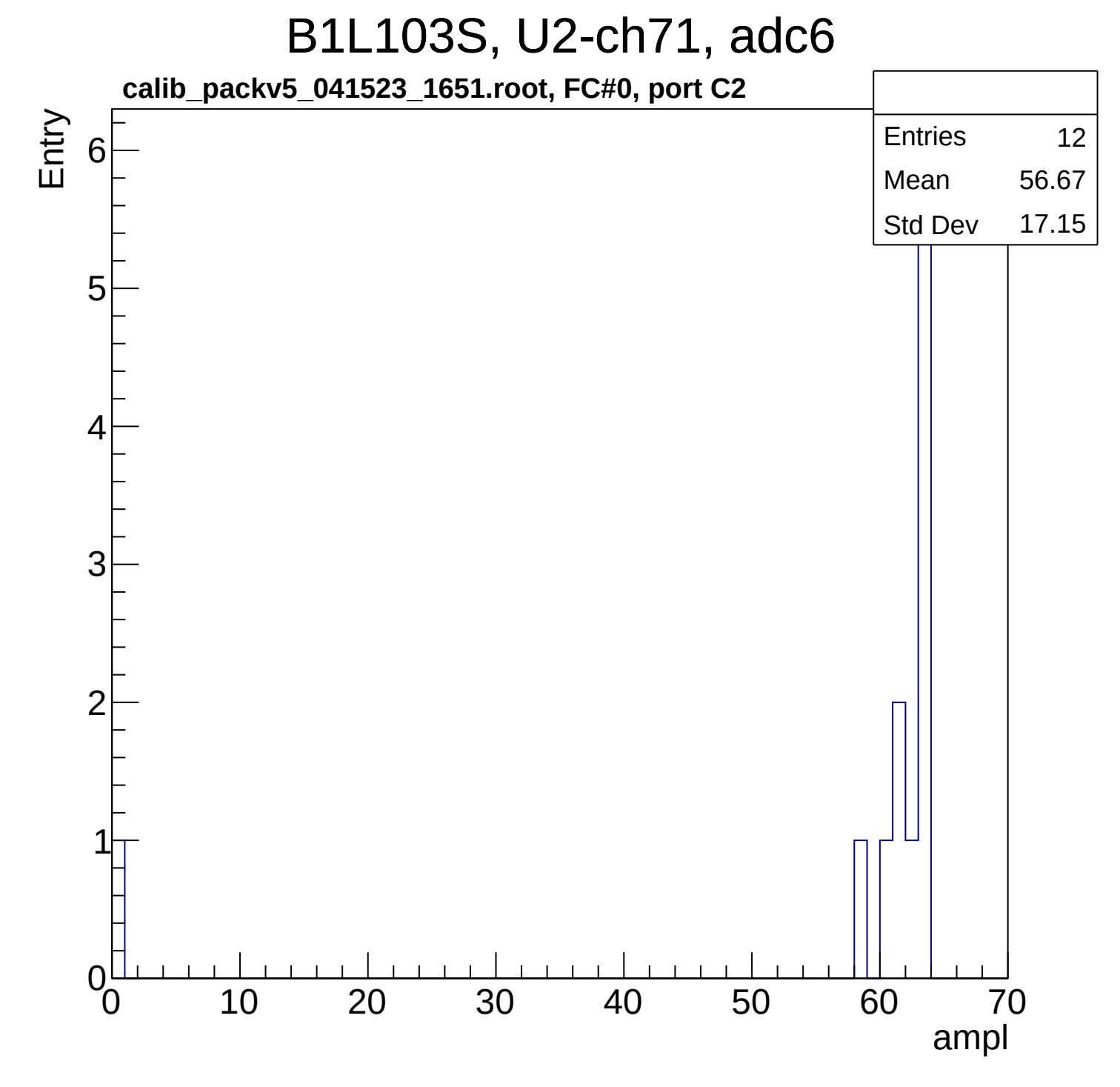

B1L103S, U2-ch71, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 30.99
Std Dev 12.85
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

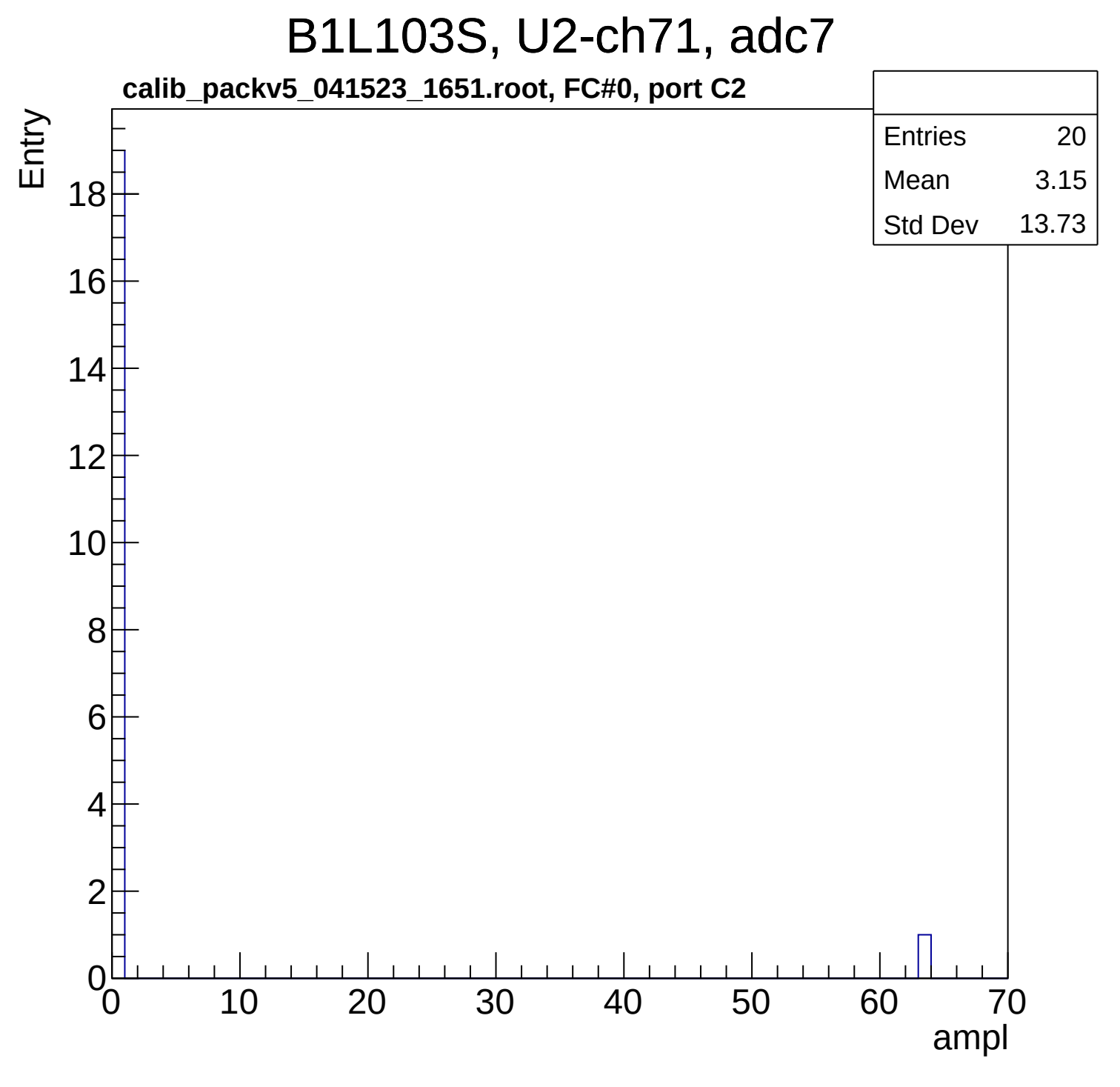

B1L103S, U2-ch71, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 40.55
Std Dev 8.491
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

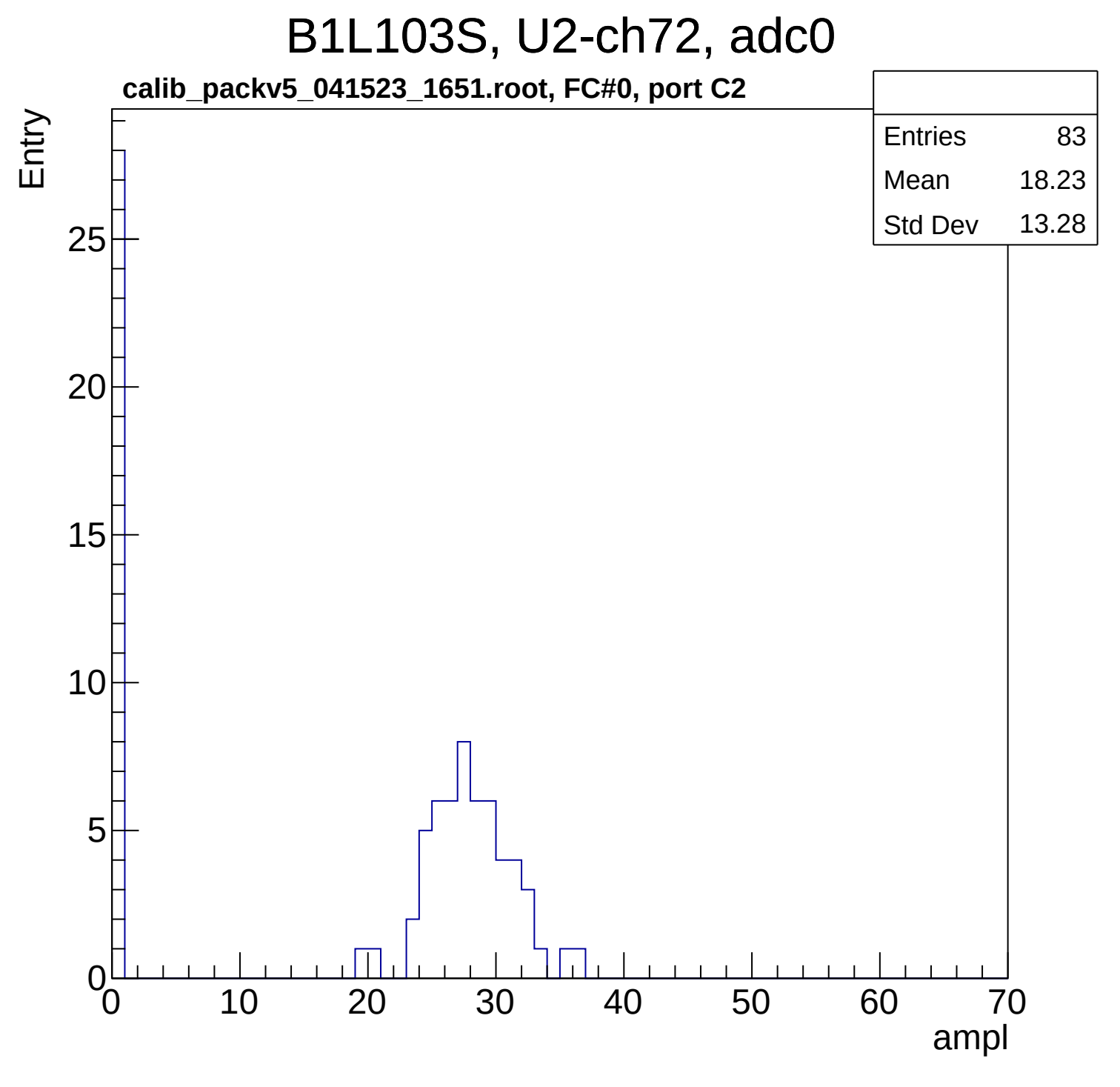

B1L103S, U2-ch71, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 48.14
Std Dev 3.567
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

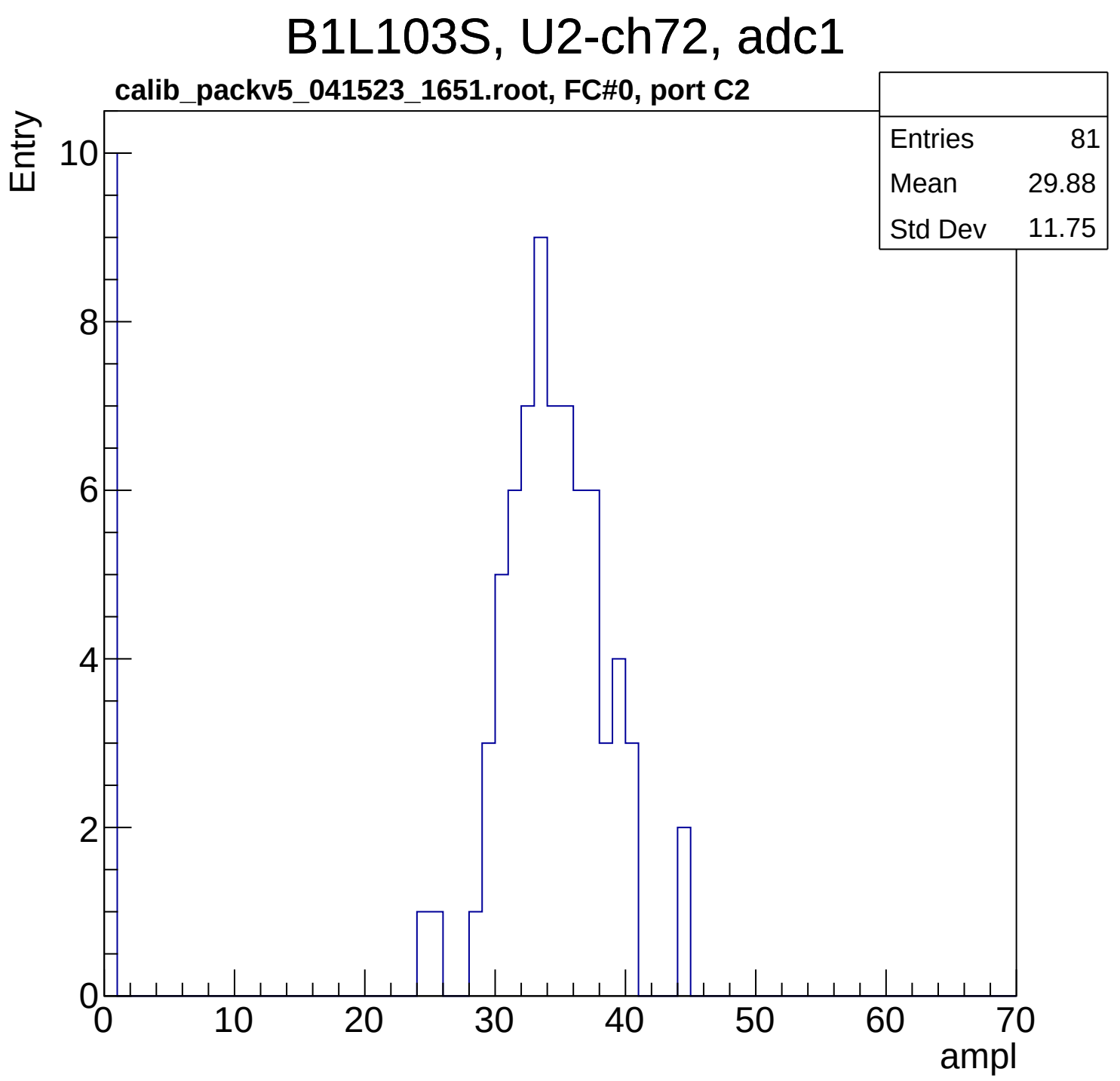

B1L103S, U2-ch71, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 54.52
Std Dev 3.578
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

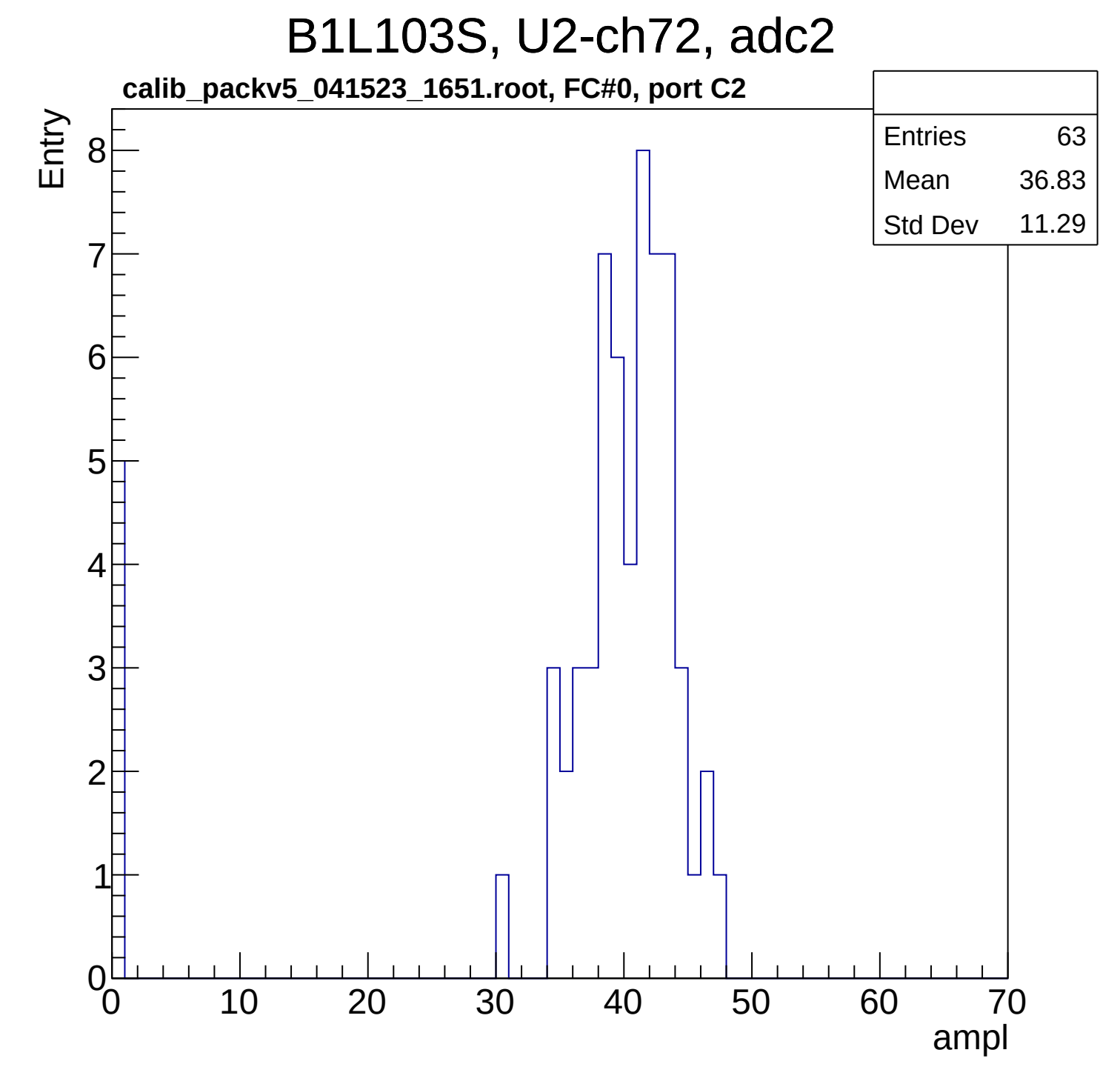

B1L103S, U2-ch71, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.96
Std Dev 2.778
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

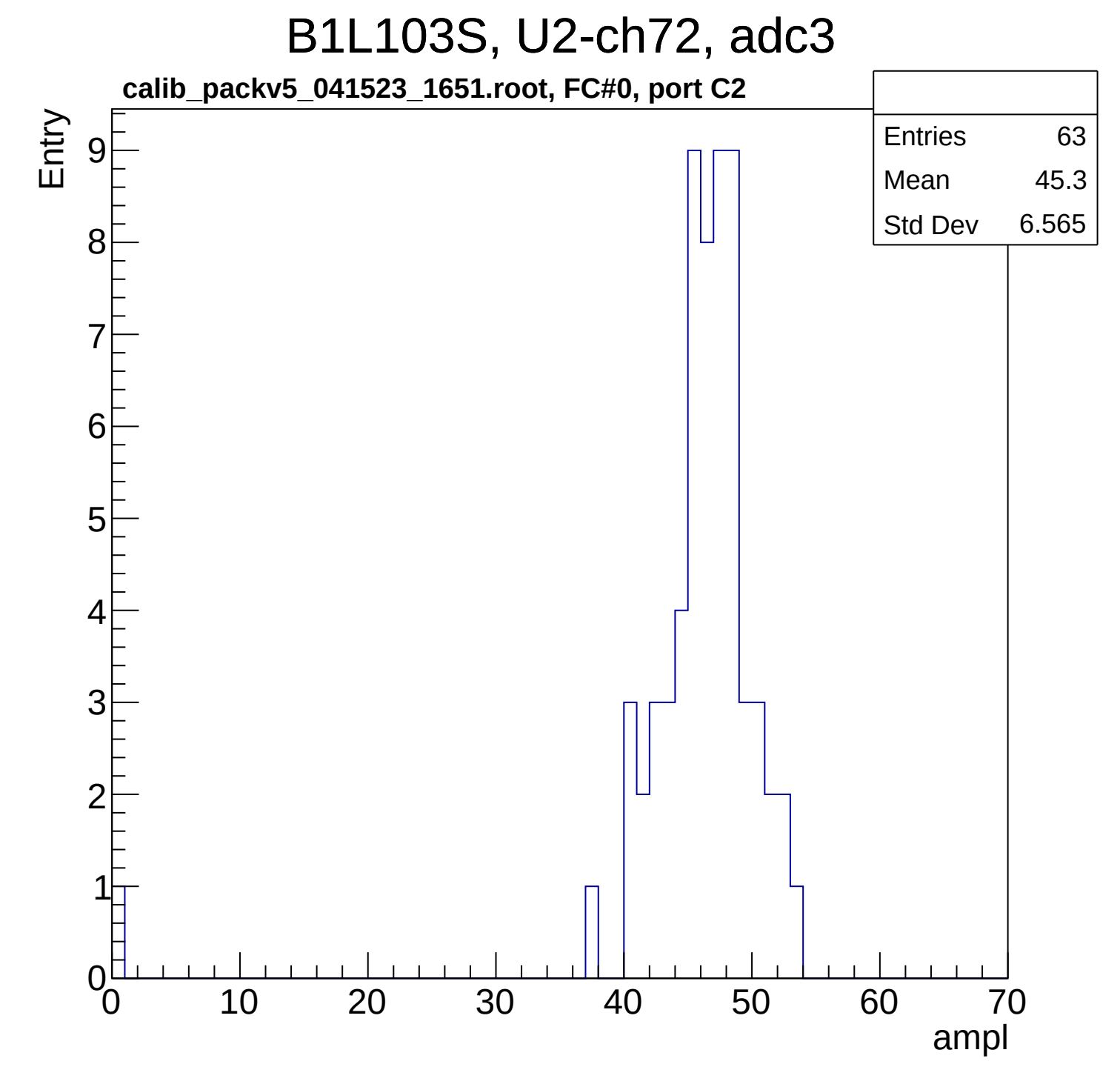

B1L103S, U2-ch71, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.67
Std Dev 17.15
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

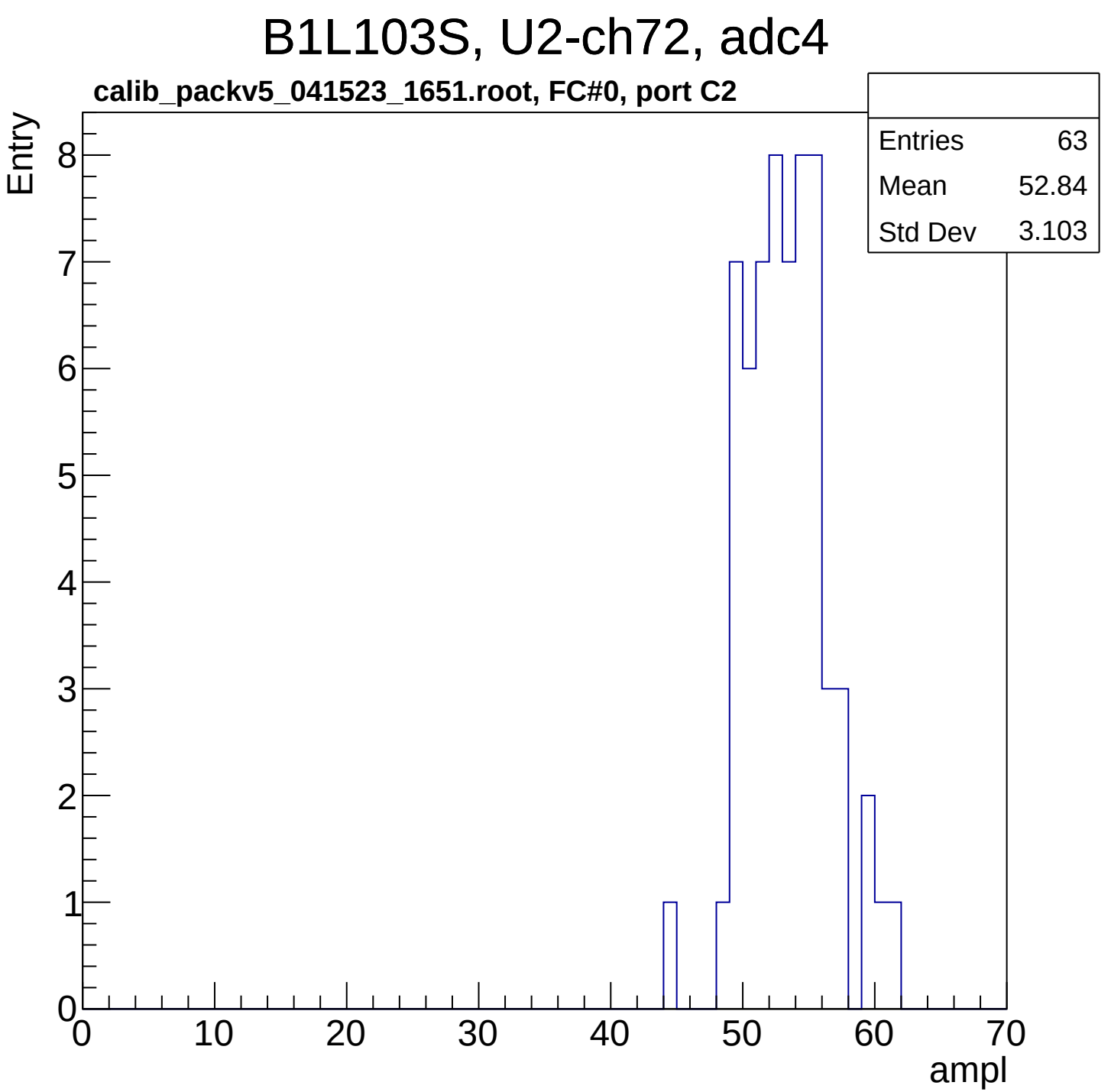

B1L103S, U2-ch71, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

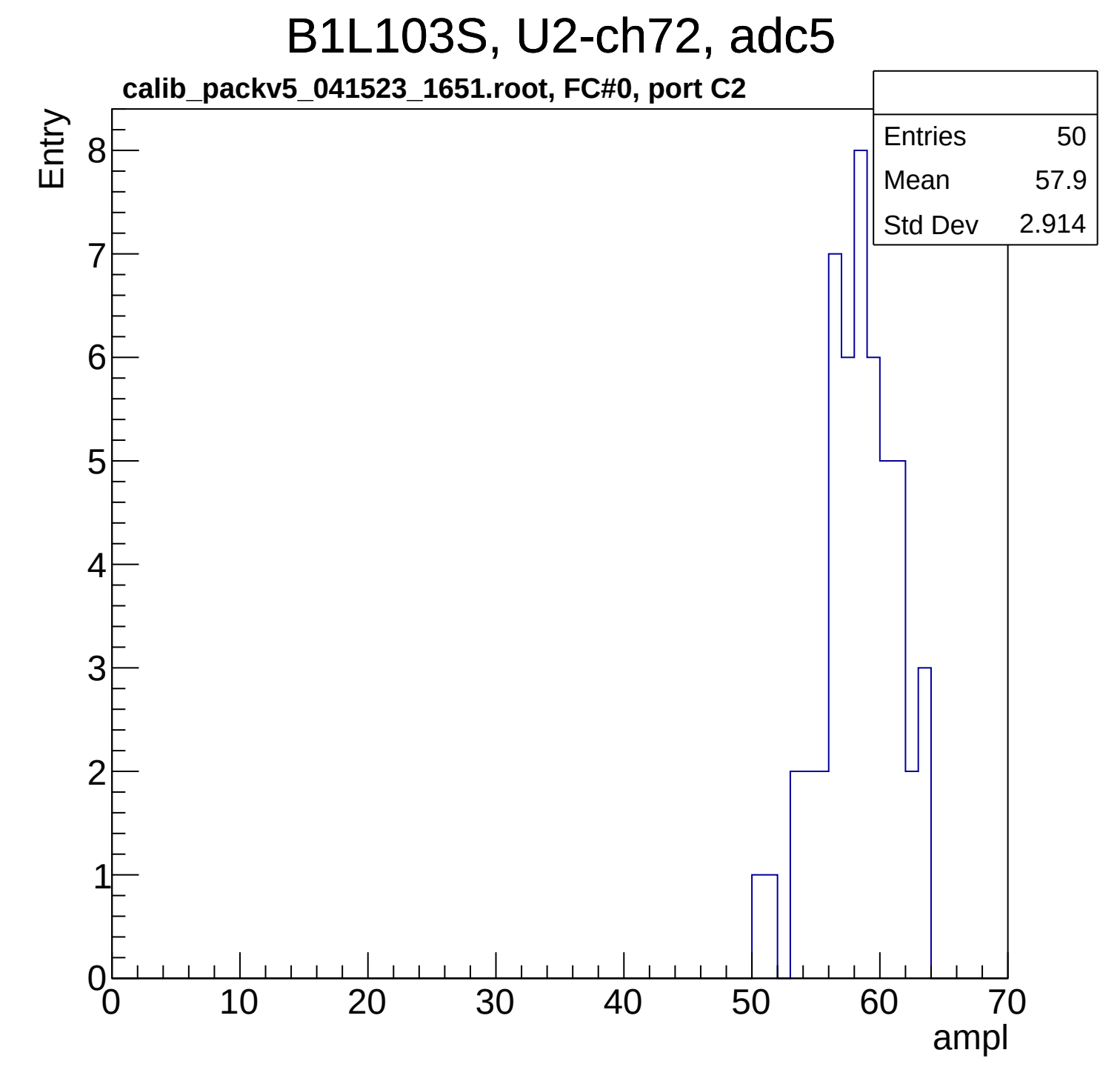

B1L103S, U2-ch72, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 18.23
Std Dev 13.28
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl

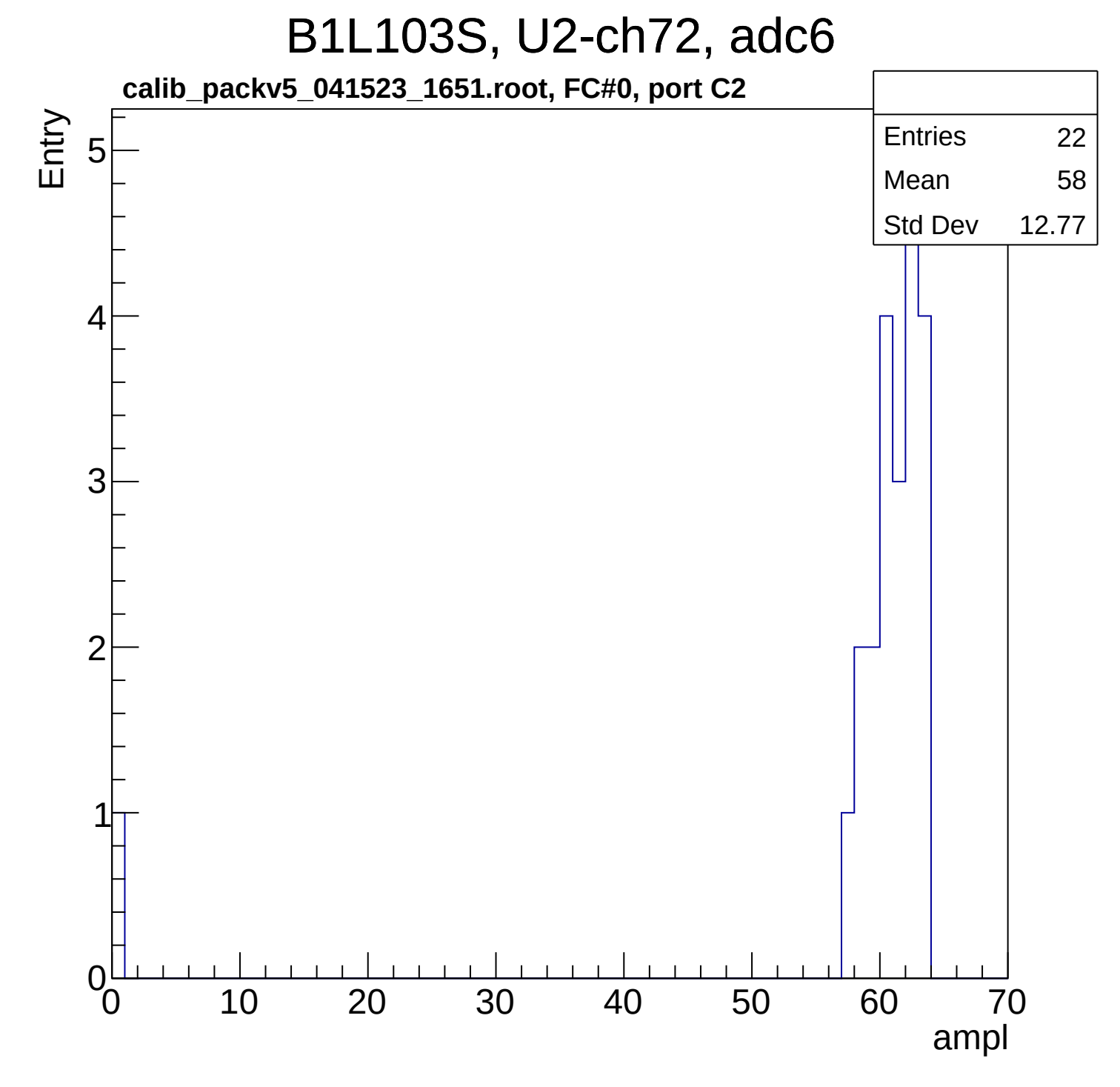

B1L103S, U2-ch72, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 29.88
Std Dev 11.75
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

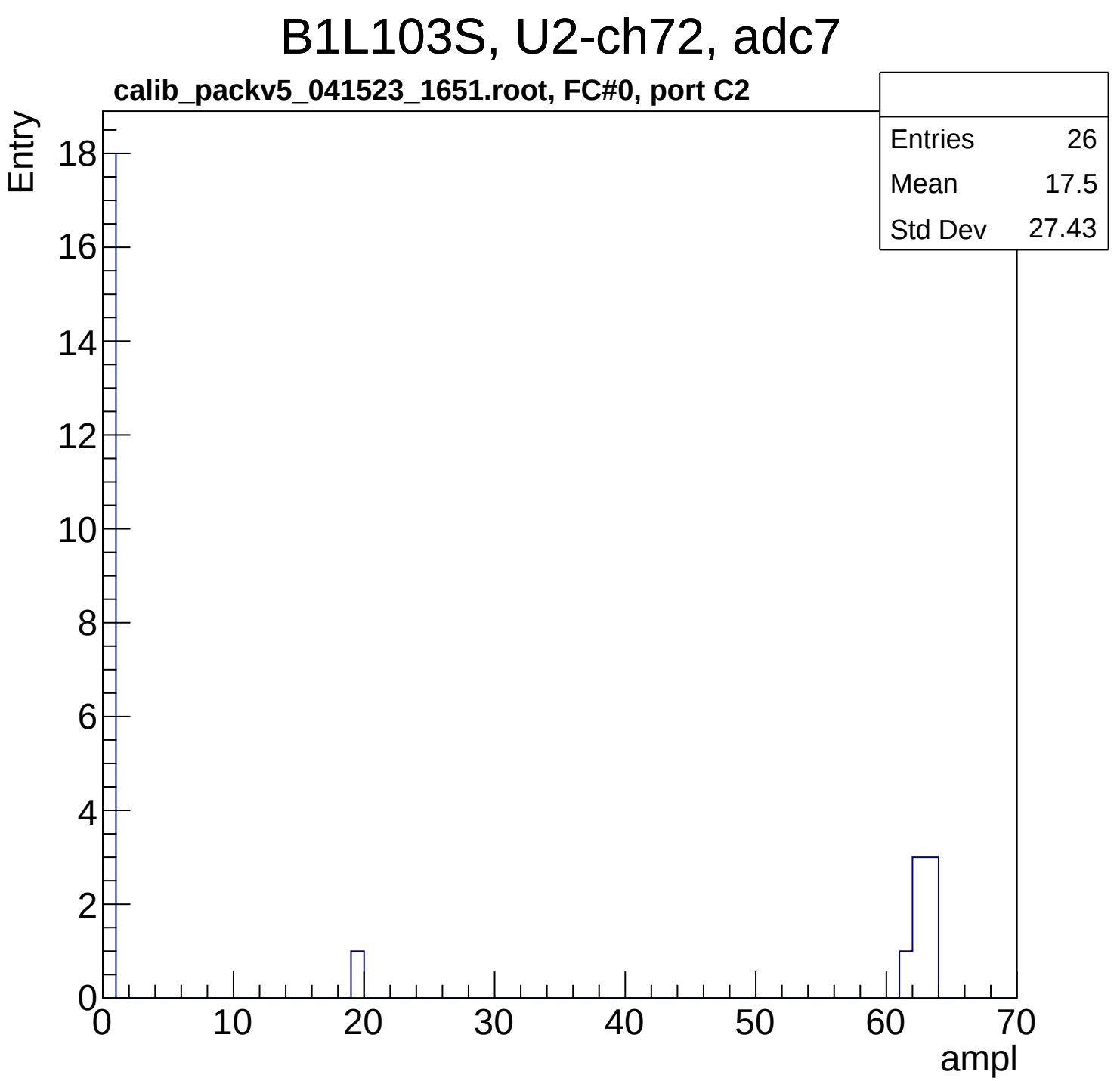

B1L103S, U2-ch72, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 36.83
Std Dev 11.29
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

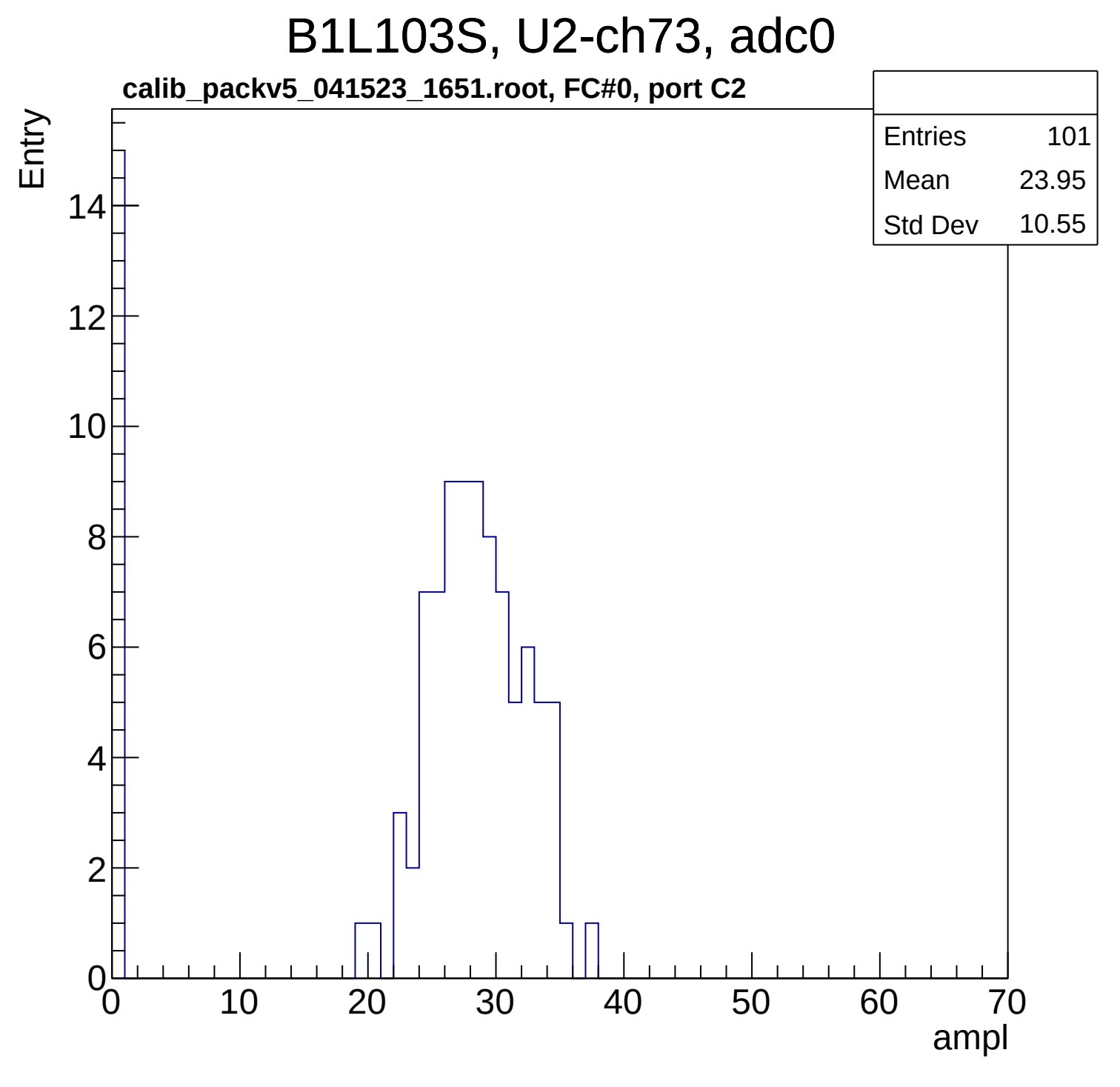

B1L103S, U2-ch72, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 45.3
Std Dev 6.565
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

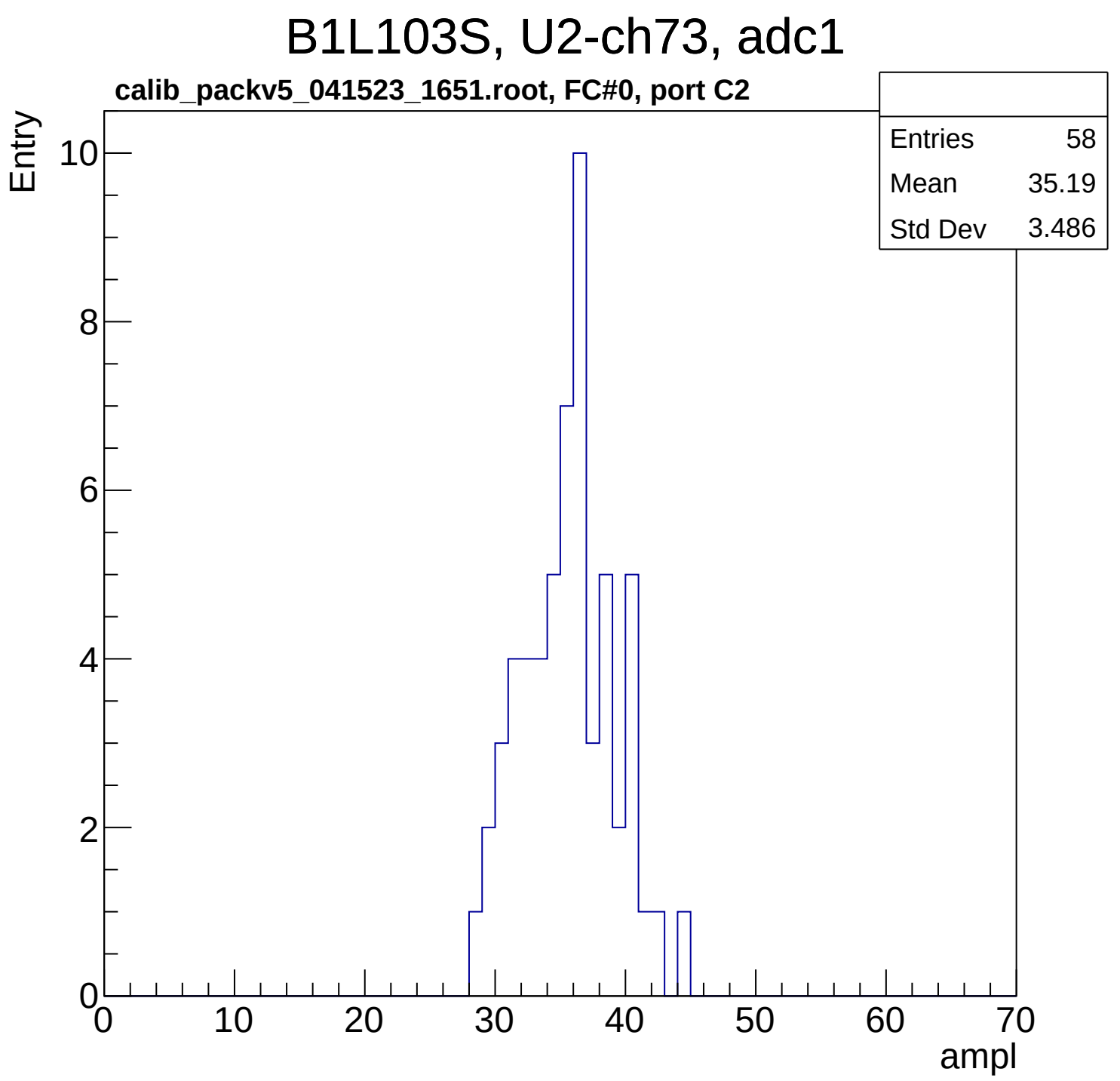

B1L103S, U2-ch72, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 52.84
Std Dev 3.103
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

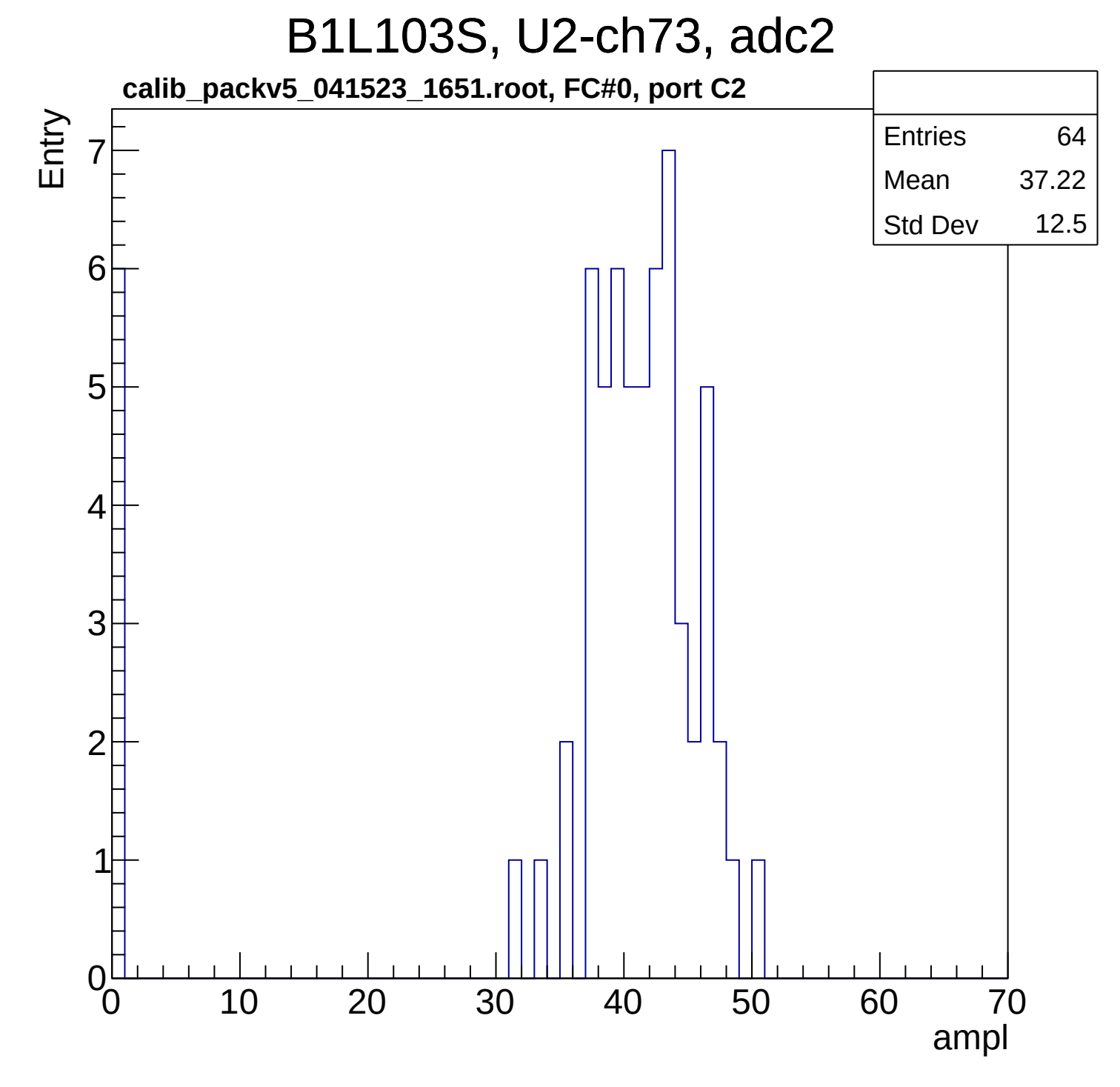

B1L103S, U2-ch72, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 57.9
Std Dev 2.914
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

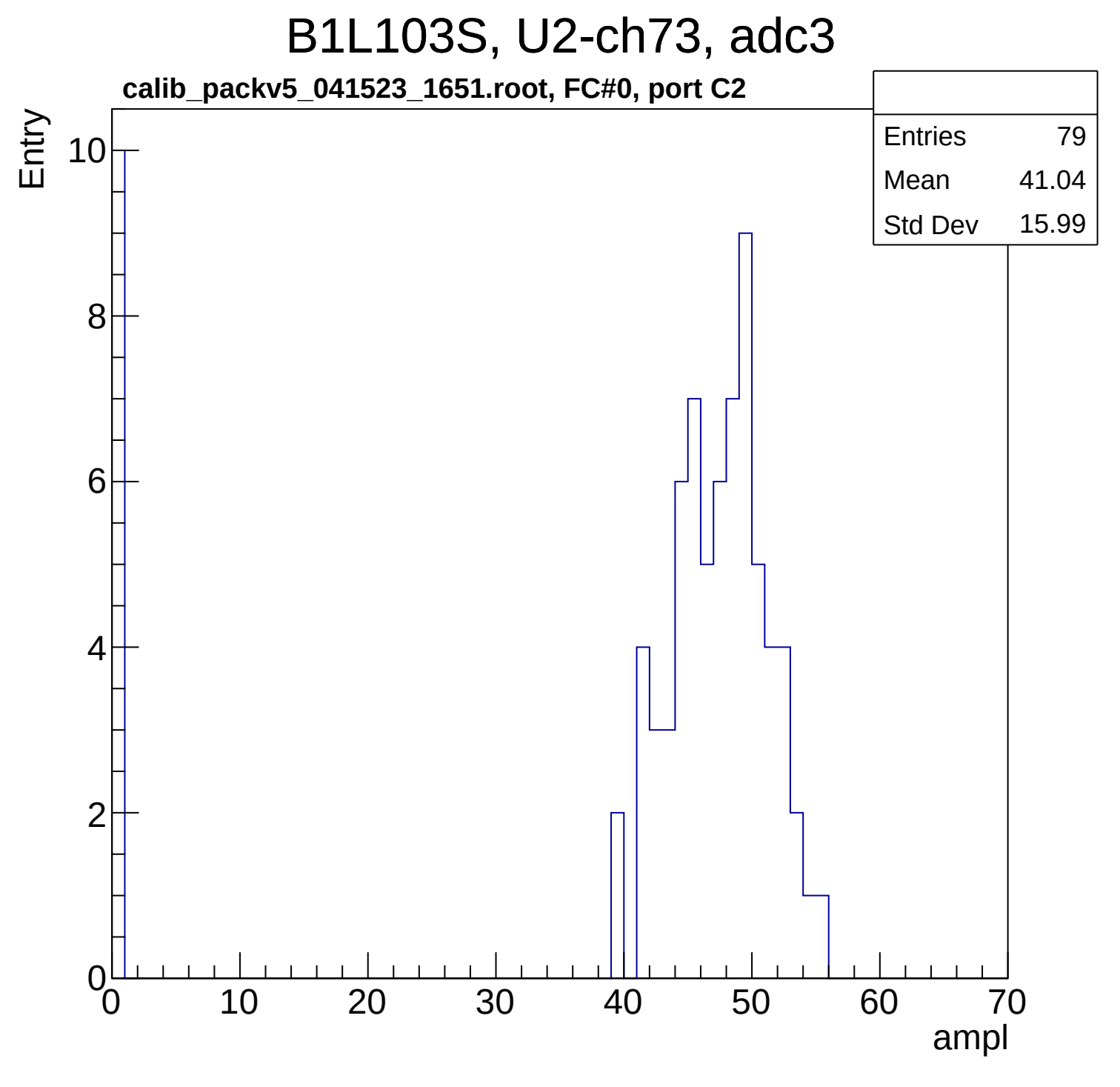

B1L103S, U2-ch72, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58
Std Dev 12.77
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

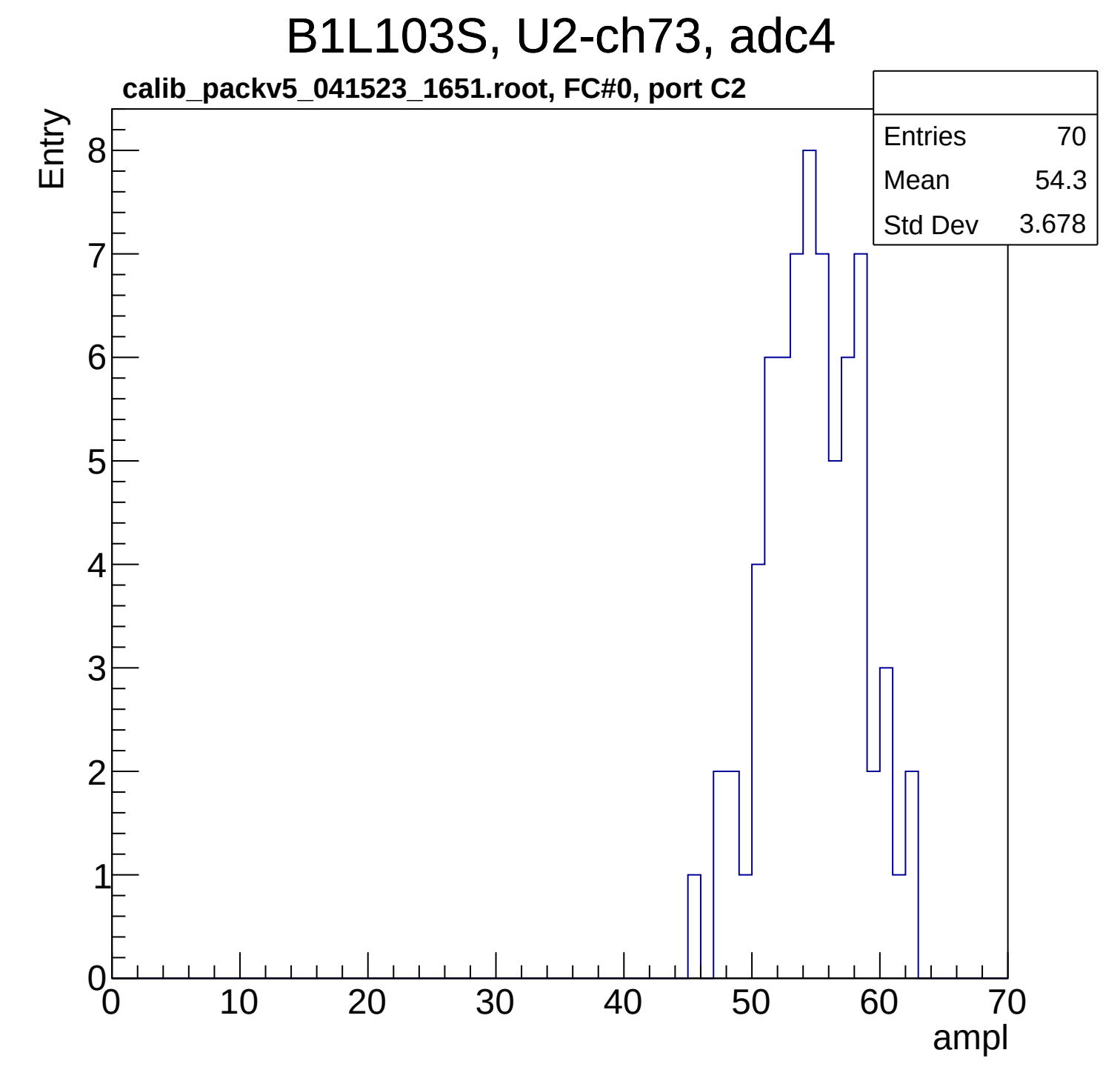

B1L103S, U2-ch72, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 17.5
Std Dev 27.43
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

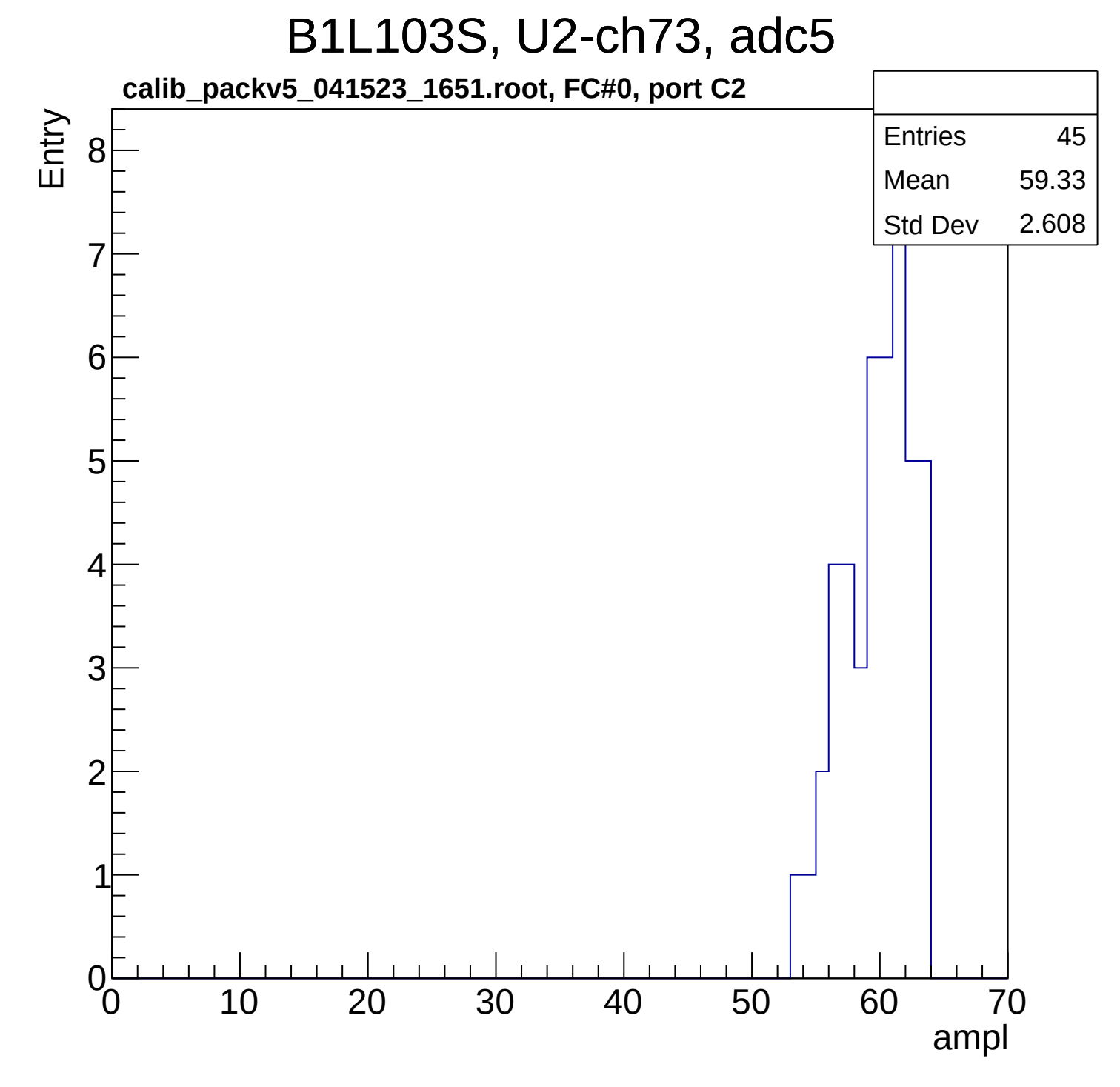

B1L103S, U2-ch73, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 23.95
Std Dev 10.55
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

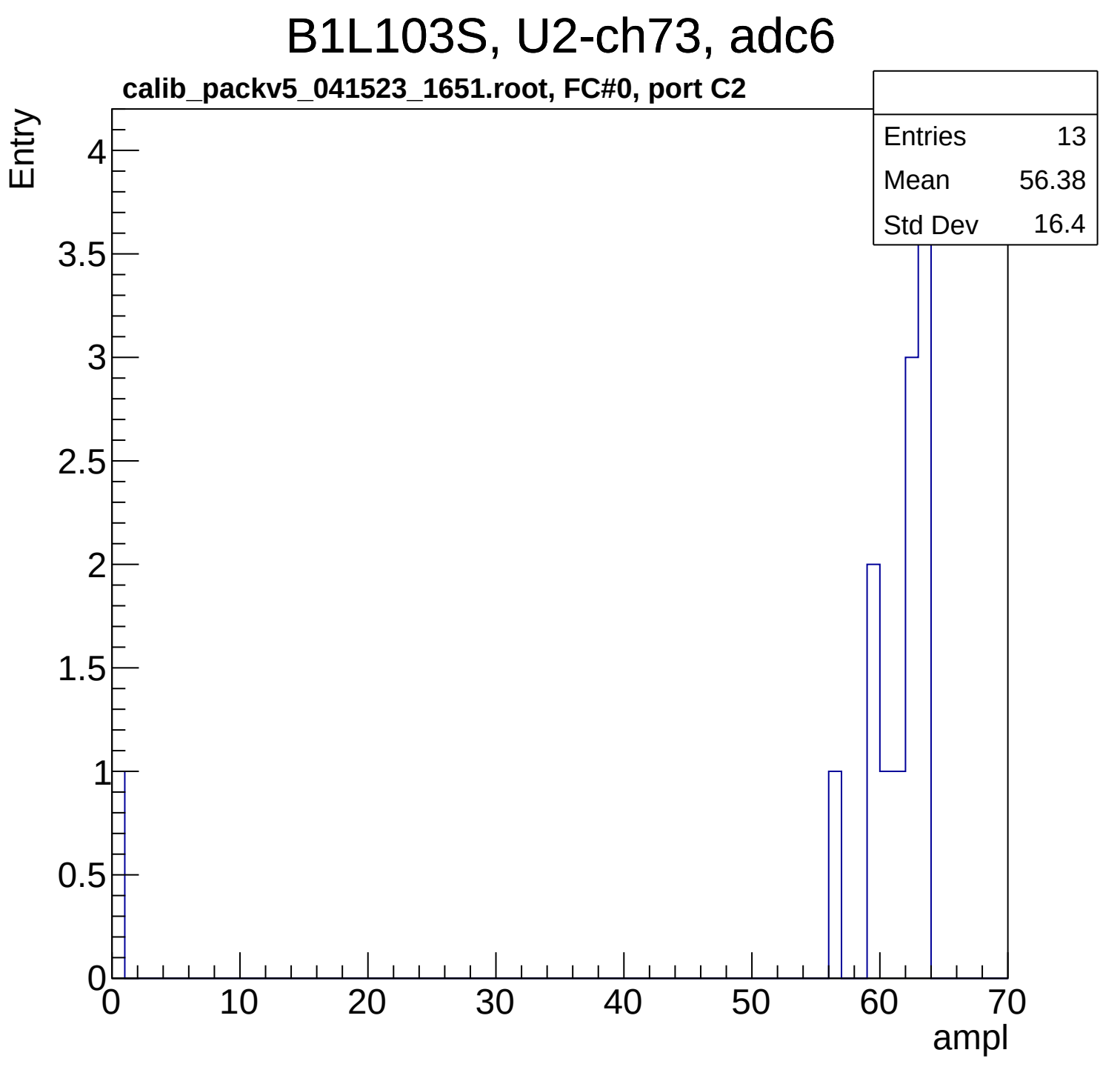

B1L103S, U2-ch73, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 35.19
Std Dev 3.486
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

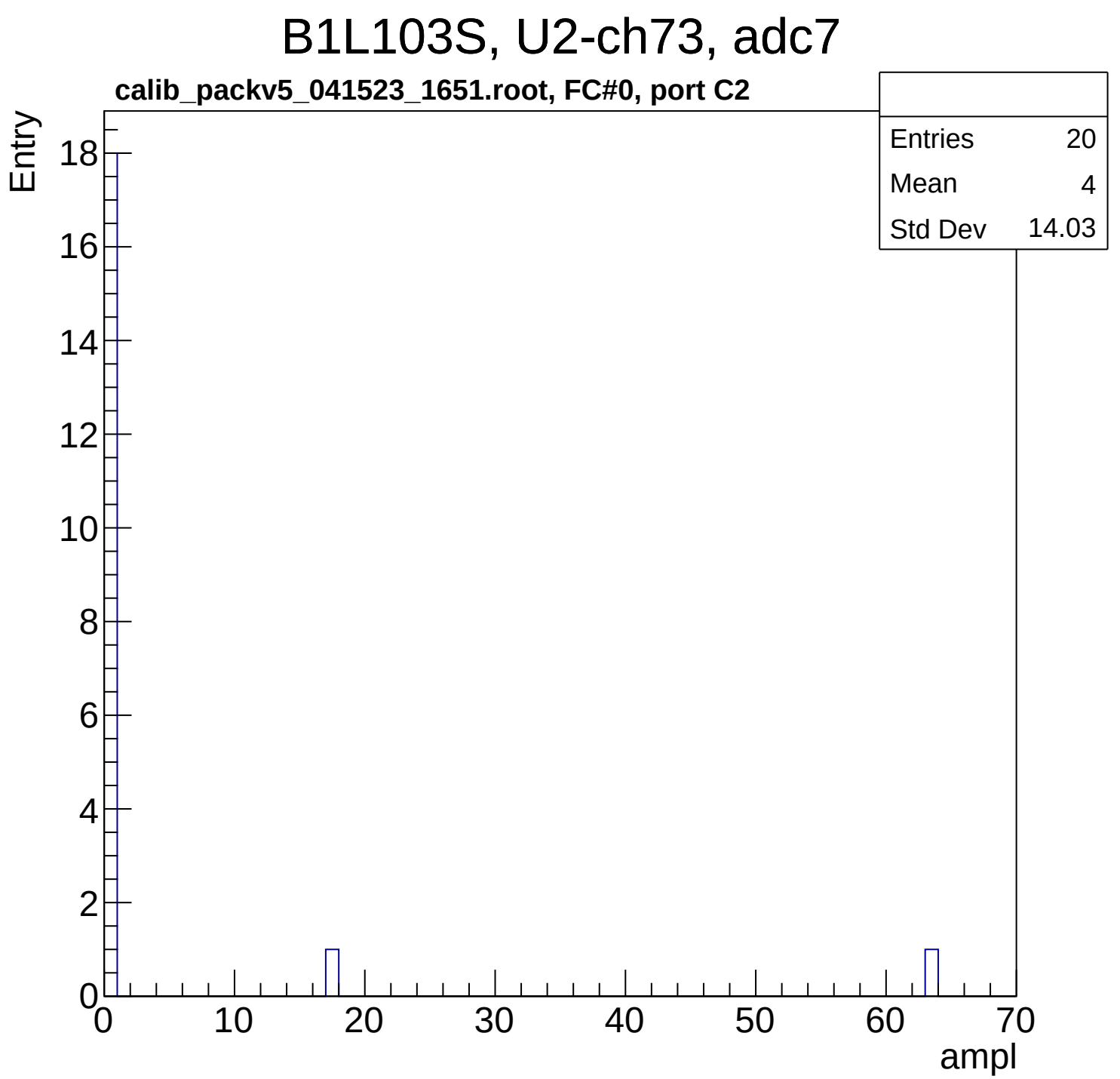

B1L103S, U2-ch73, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 37.22
Std Dev 12.5
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

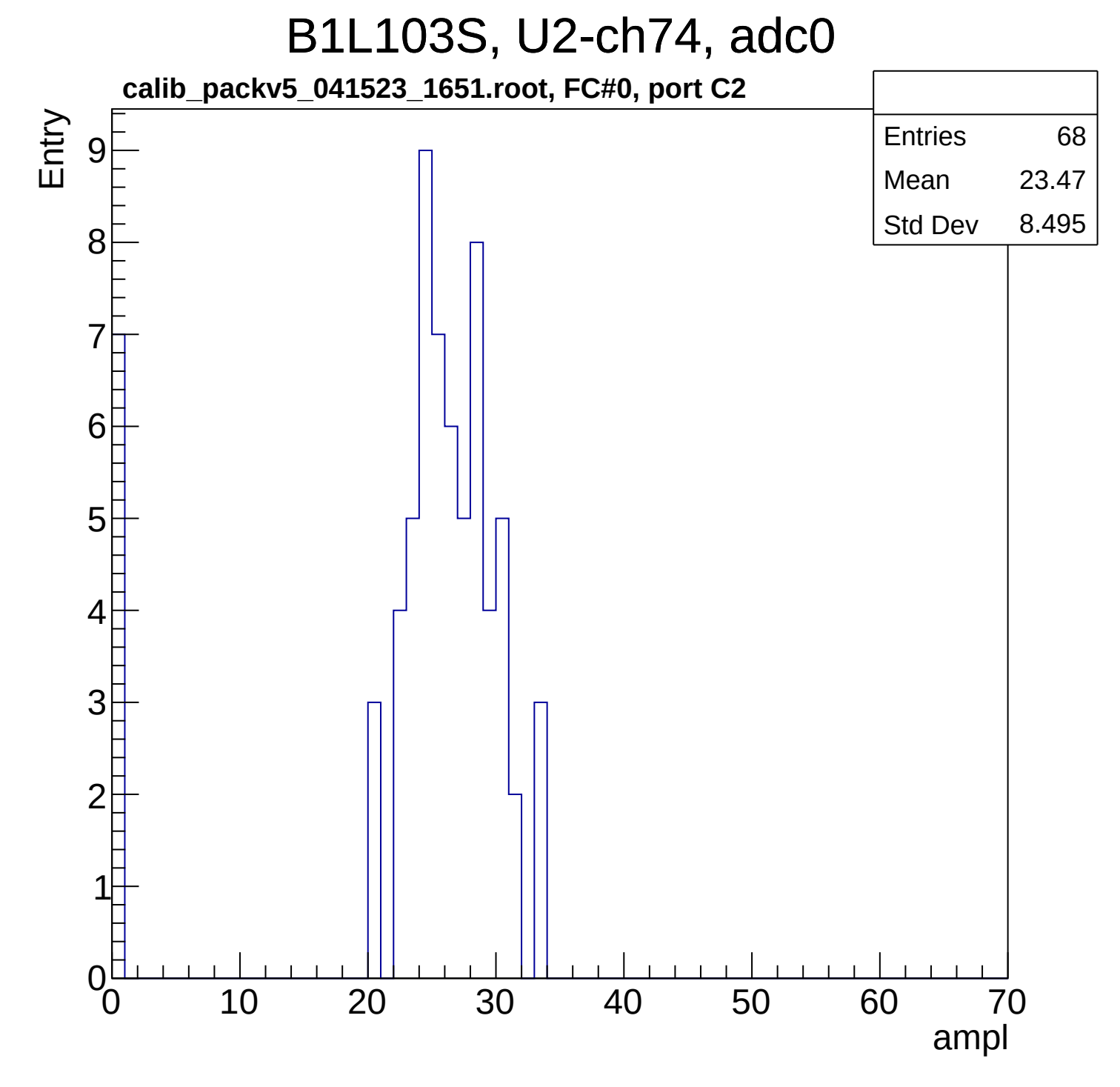

B1L103S, U2-ch73, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 41.04
Std Dev 15.99
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

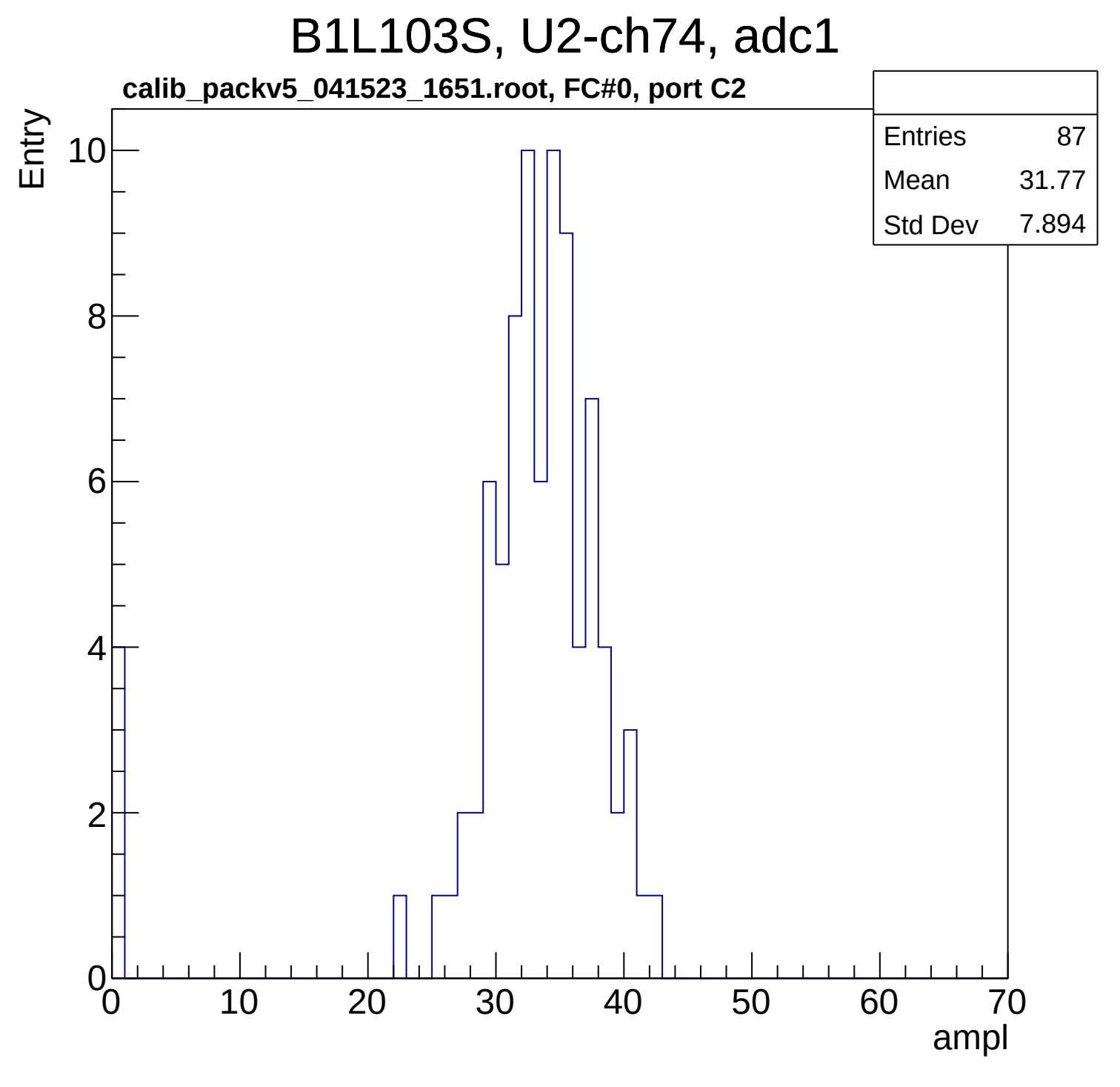

B1L103S, U2-ch73, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 54.3
Std Dev 3.678
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

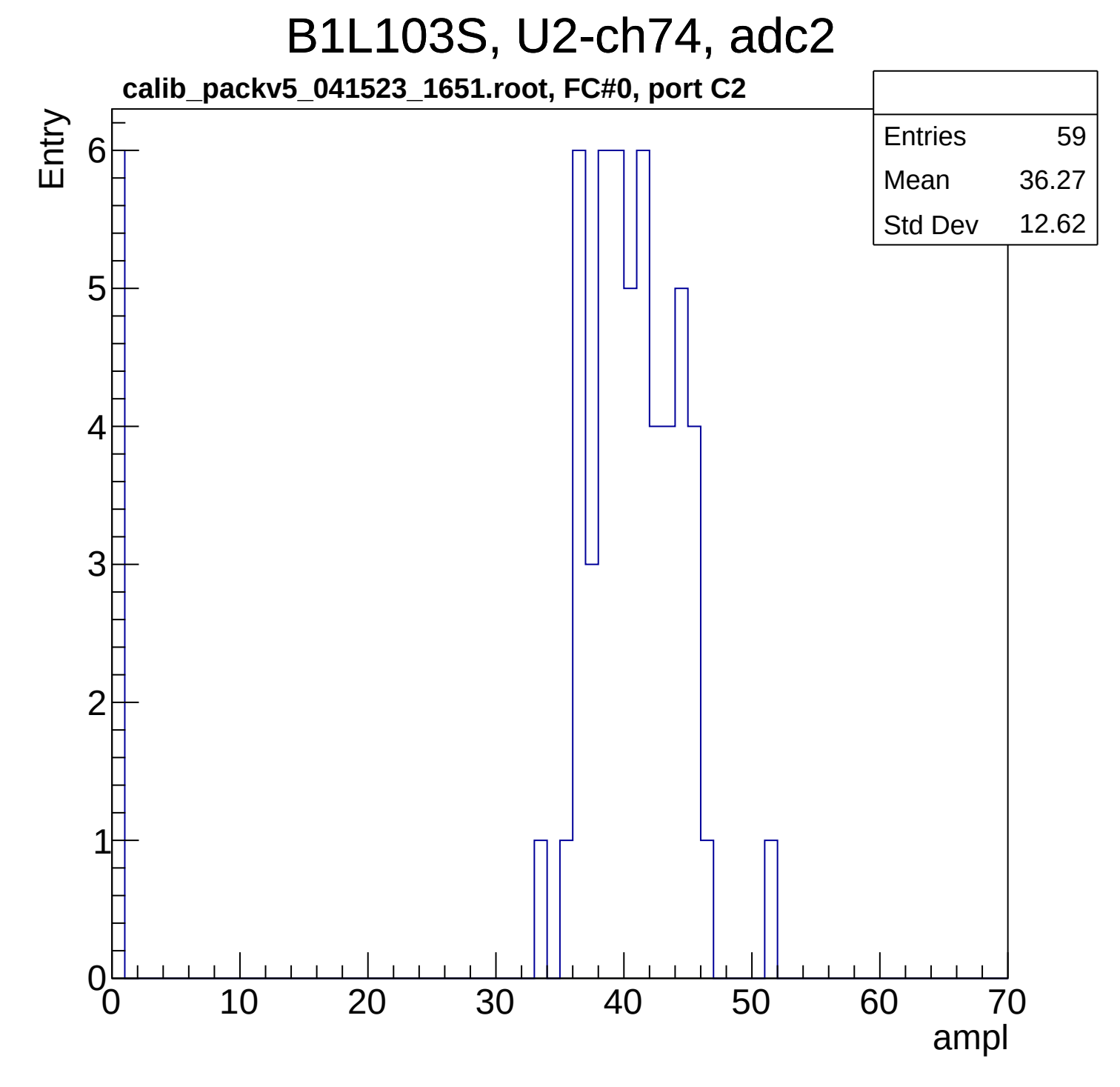

B1L103S, U2-ch73, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 59.33
Std Dev 2.608
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

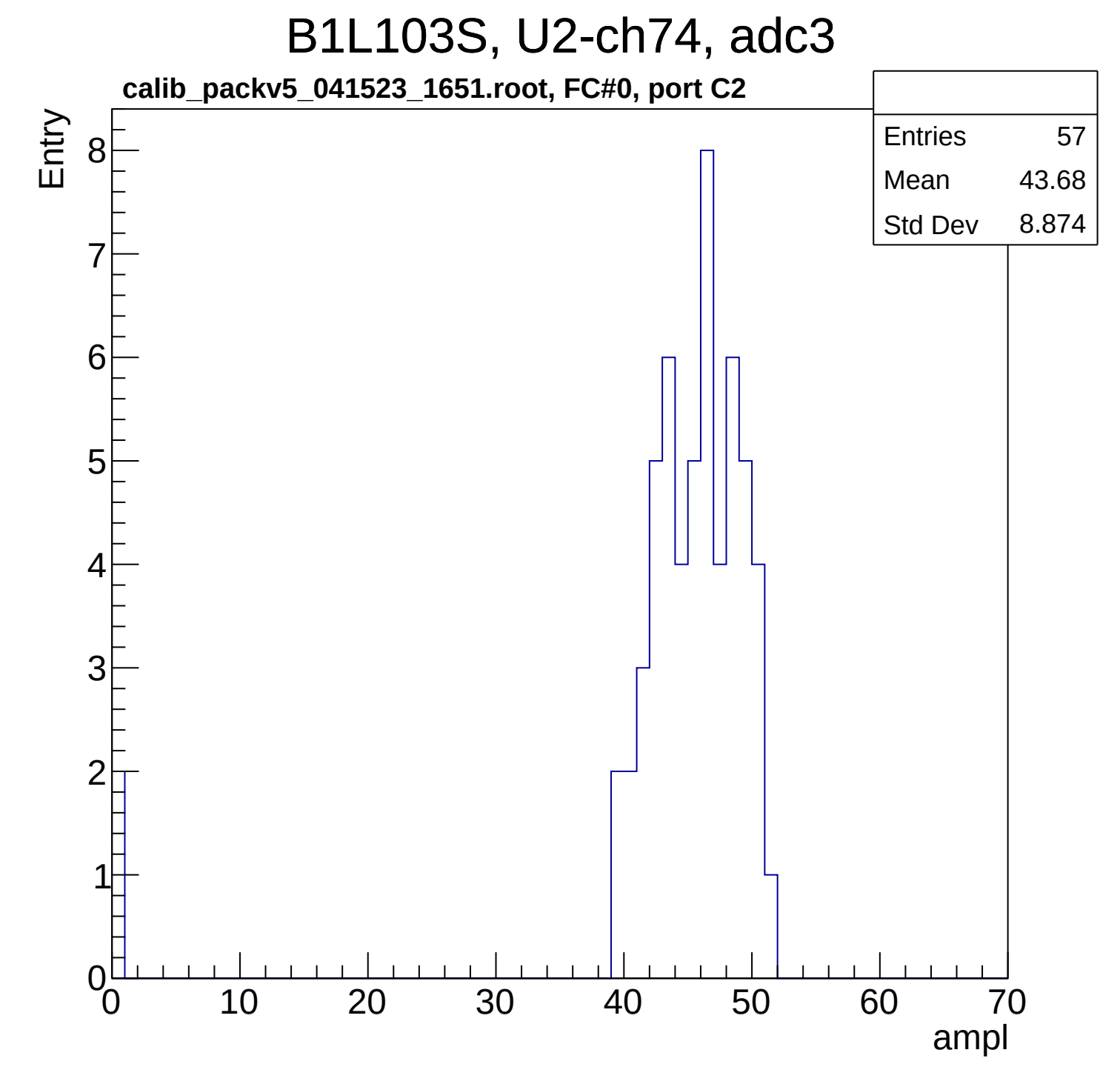

B1L103S, U2-ch73, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 56.38
Std Dev 16.4
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

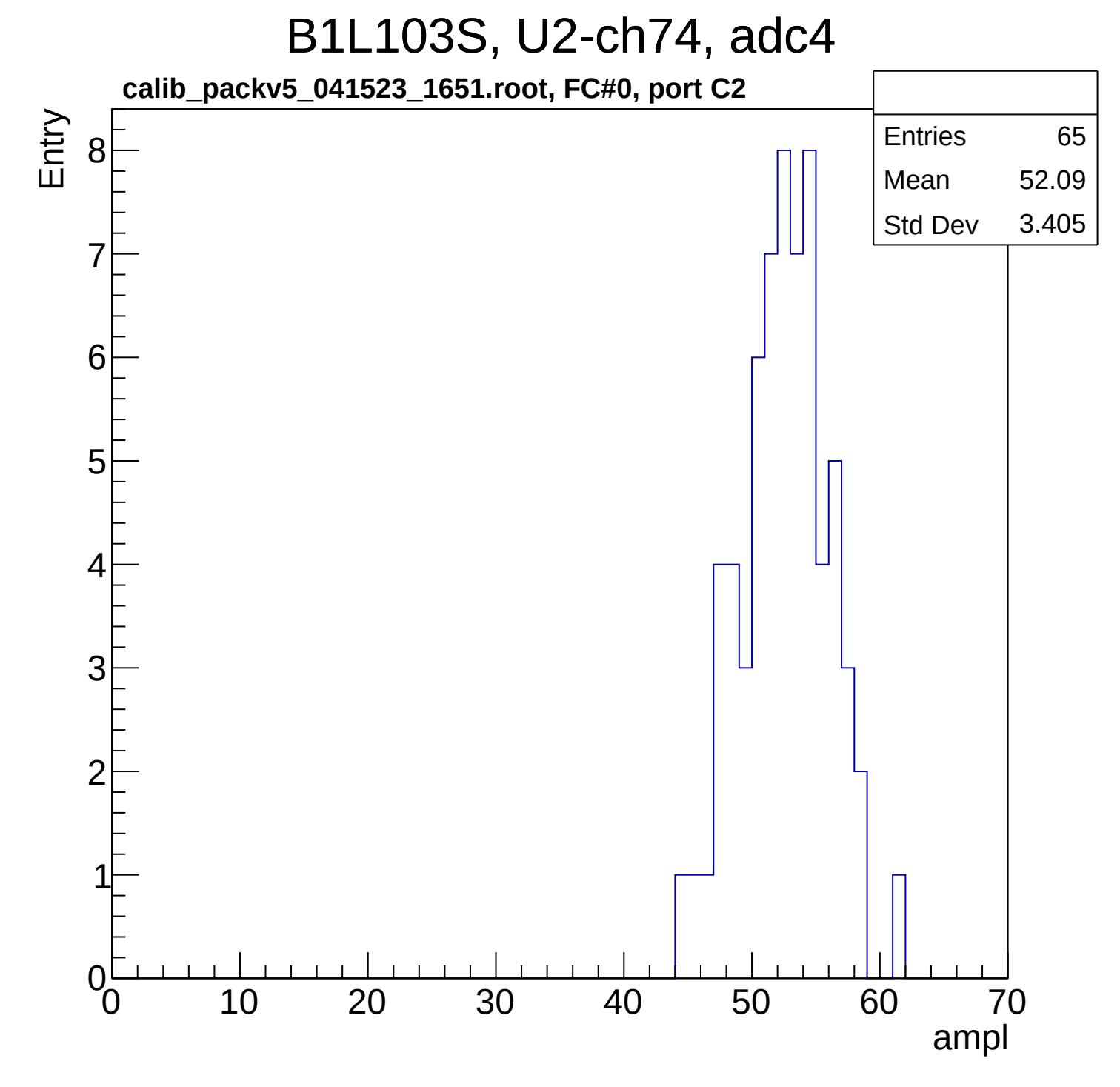

B1L103S, U2-ch73, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4
Std Dev 14.03
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

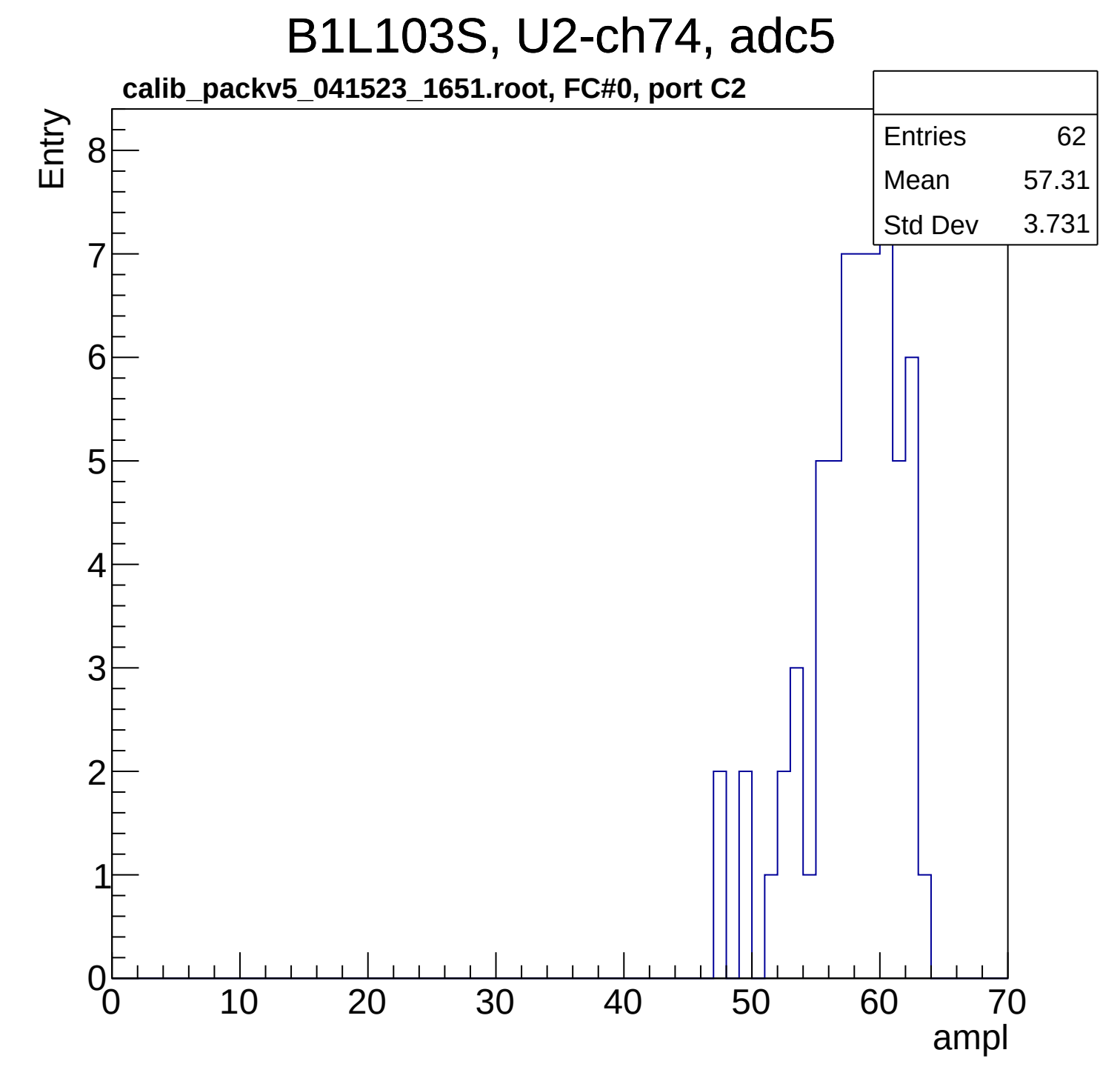

B1L103S, U2-ch74, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 23.47
Std Dev 8.495
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

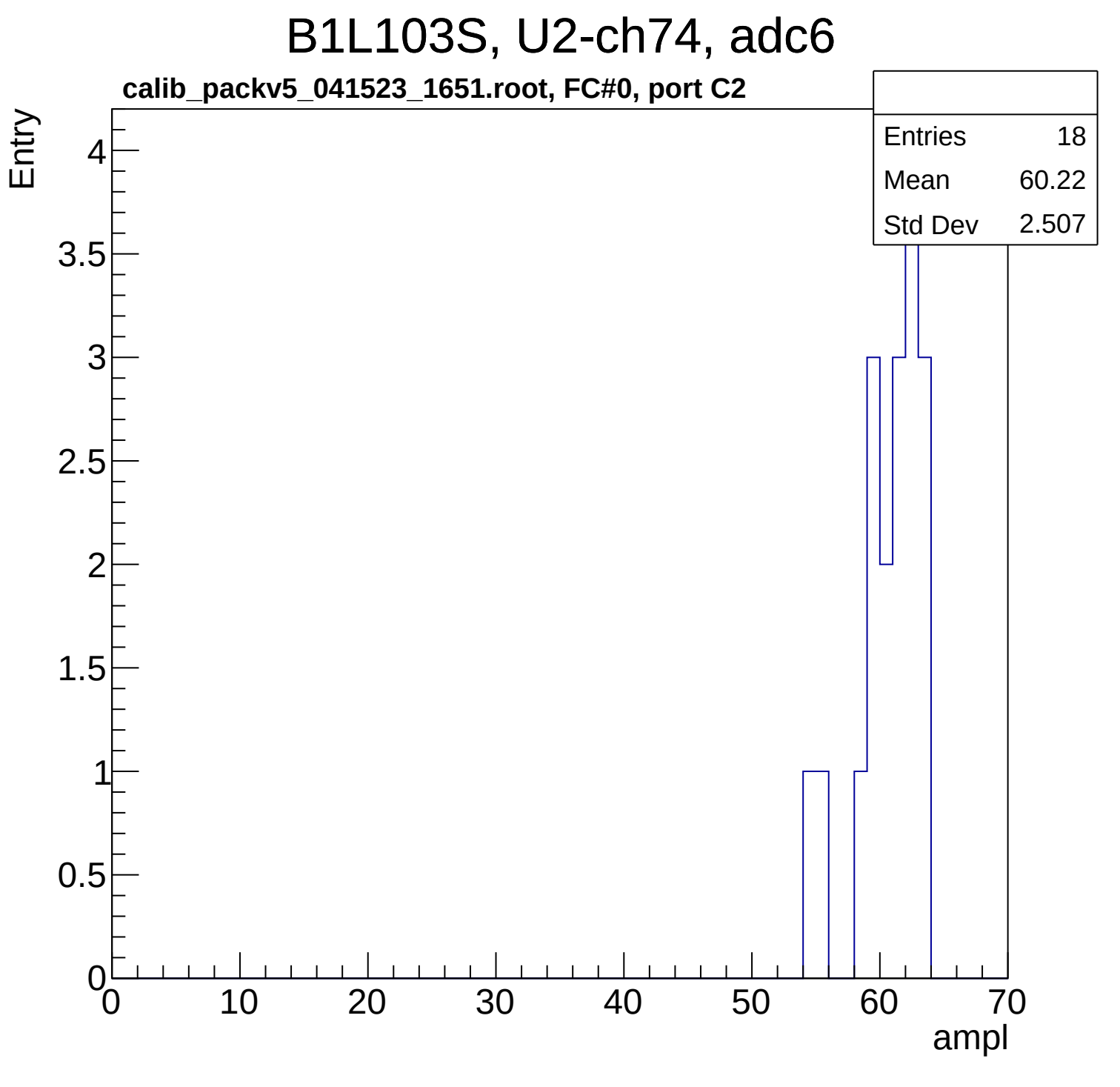

B1L103S, U2-ch74, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 31.77
Std Dev 7.894
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

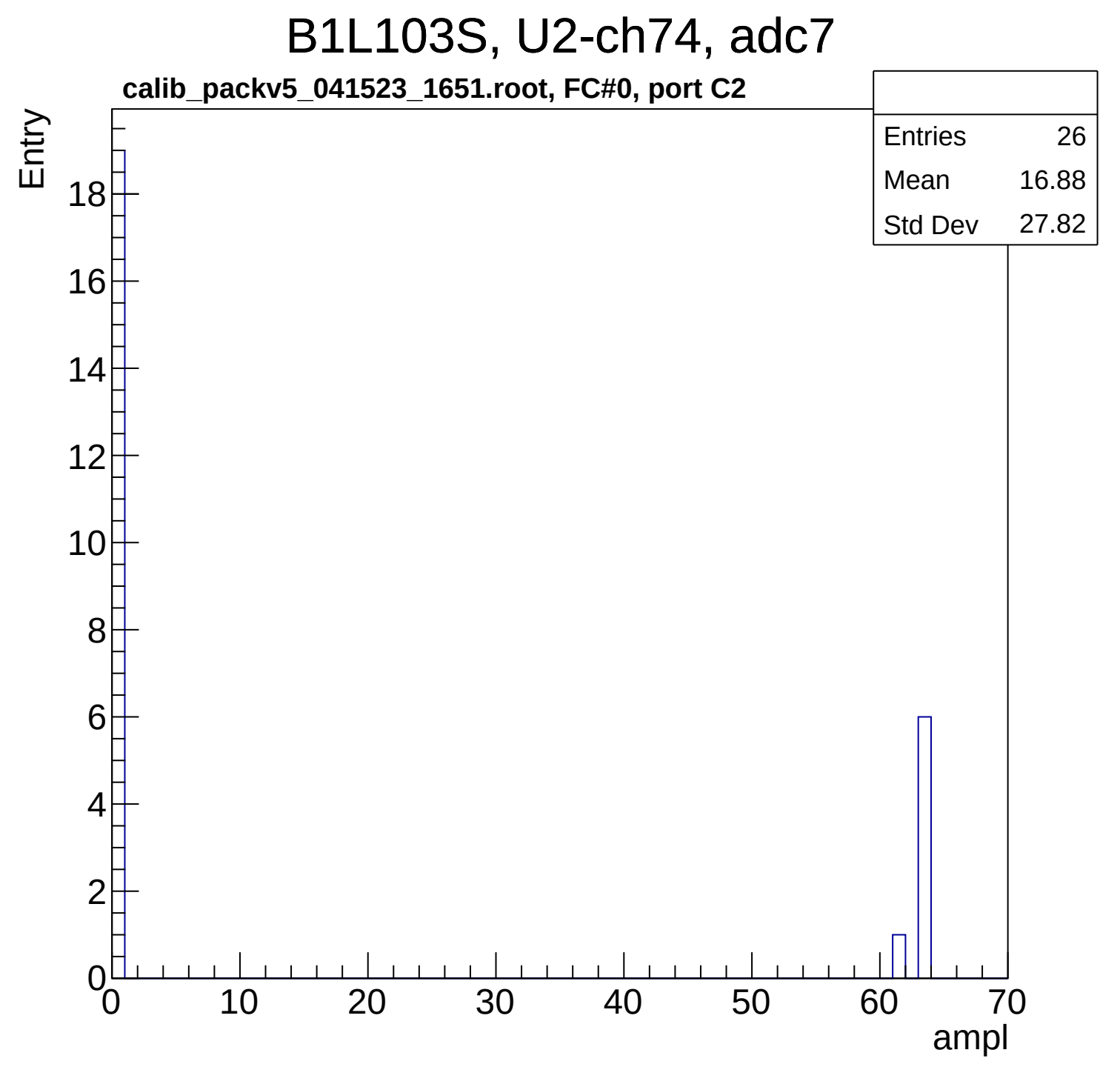

B1L103S, U2-ch74, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 36.27
Std Dev 12.62
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

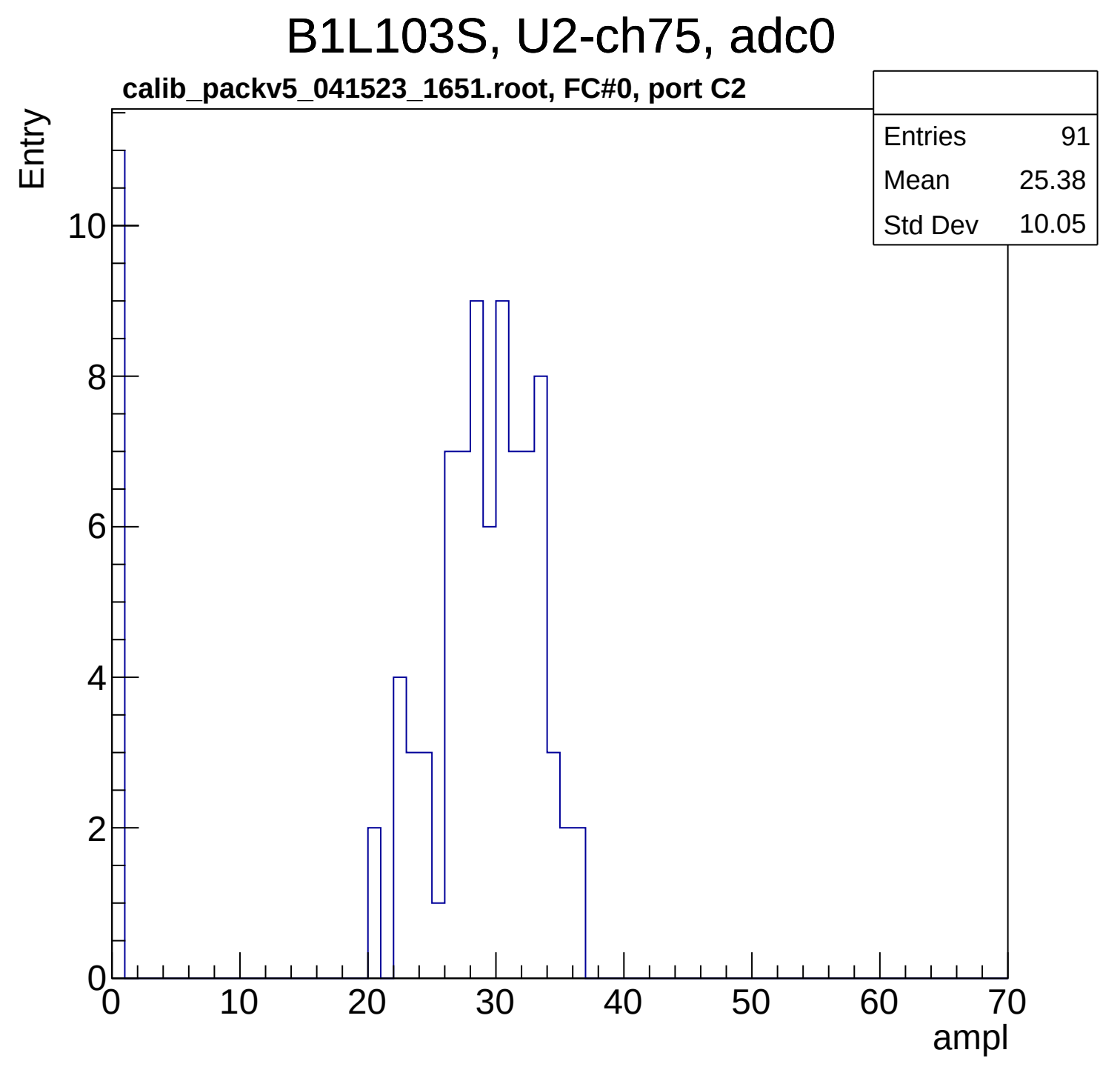

B1L103S, U2-ch74, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 43.68
Std Dev 8.874
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

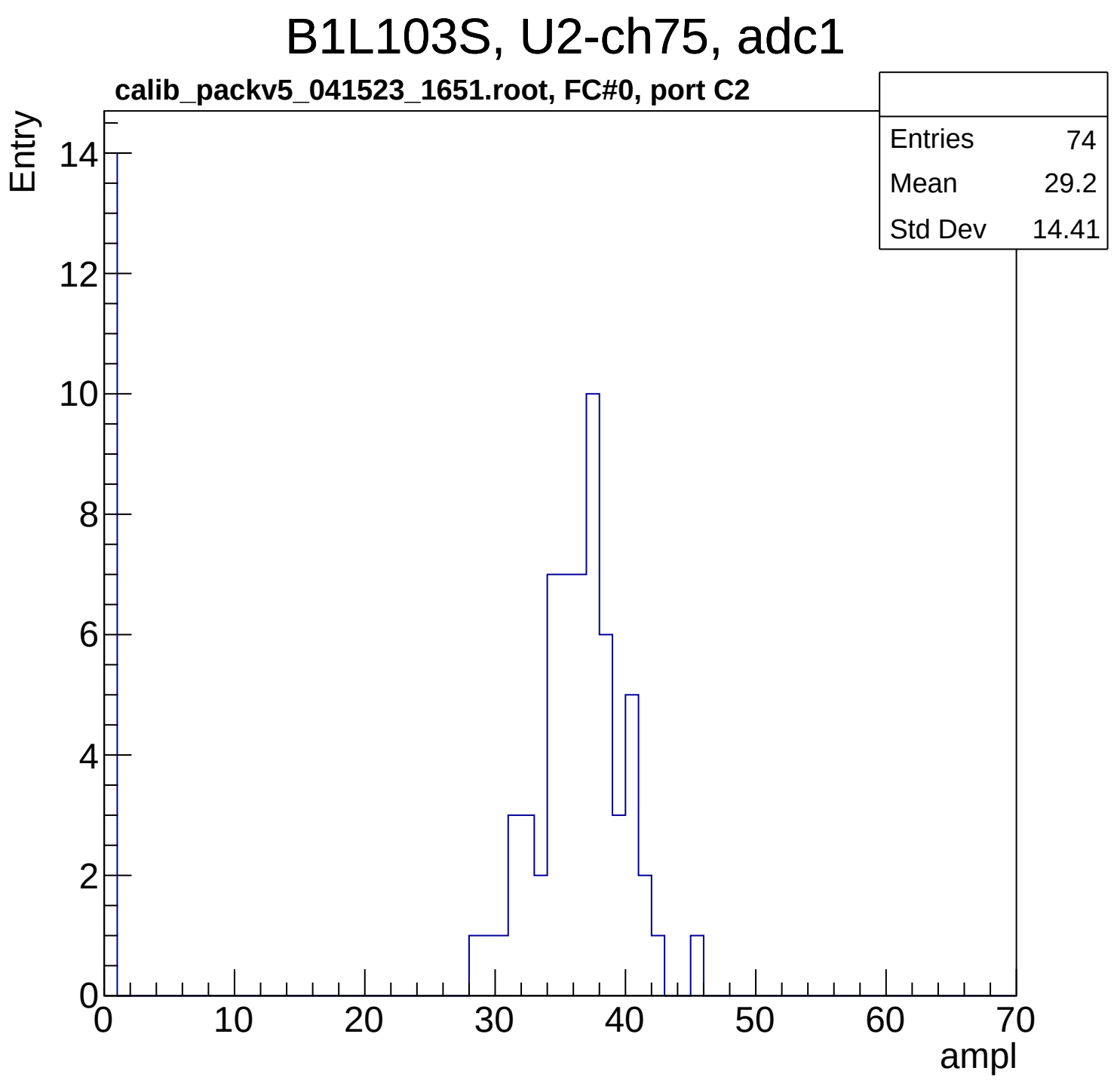

B1L103S, U2-ch74, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 52.09
Std Dev 3.405
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

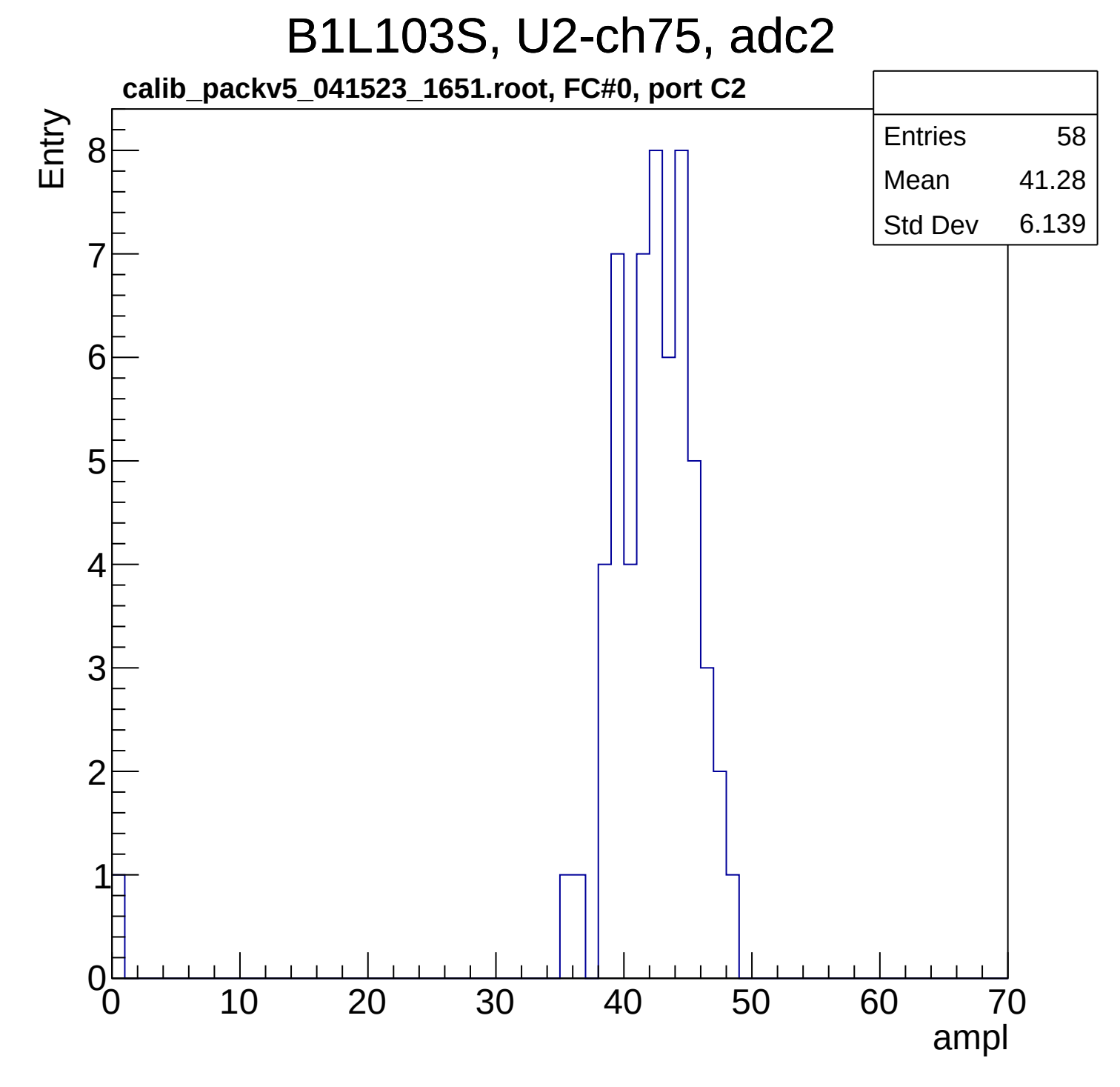

B1L103S, U2-ch74, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 57.31
Std Dev 3.731
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

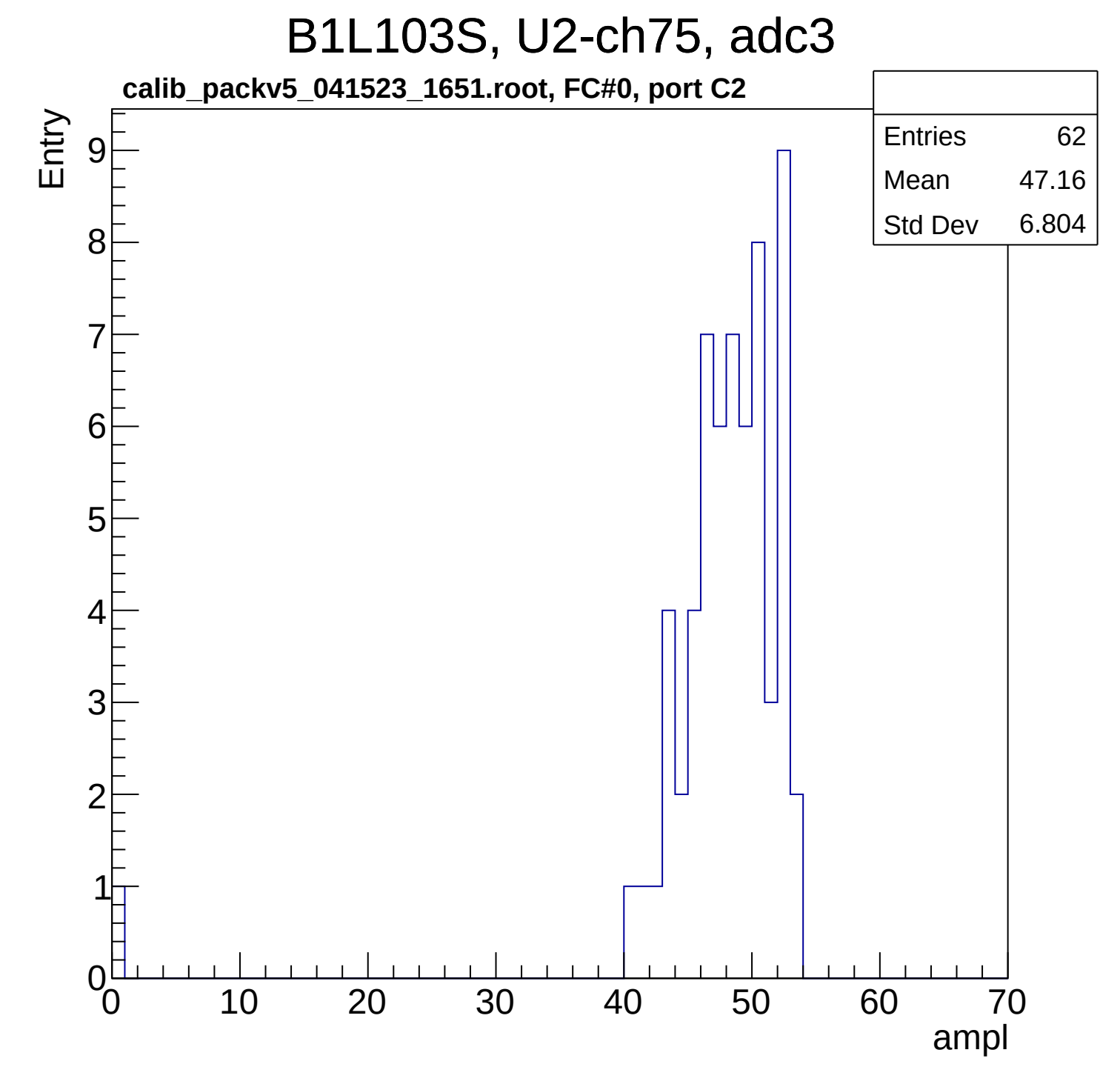

B1L103S, U2-ch74, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 60.22
Std Dev 2.507
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

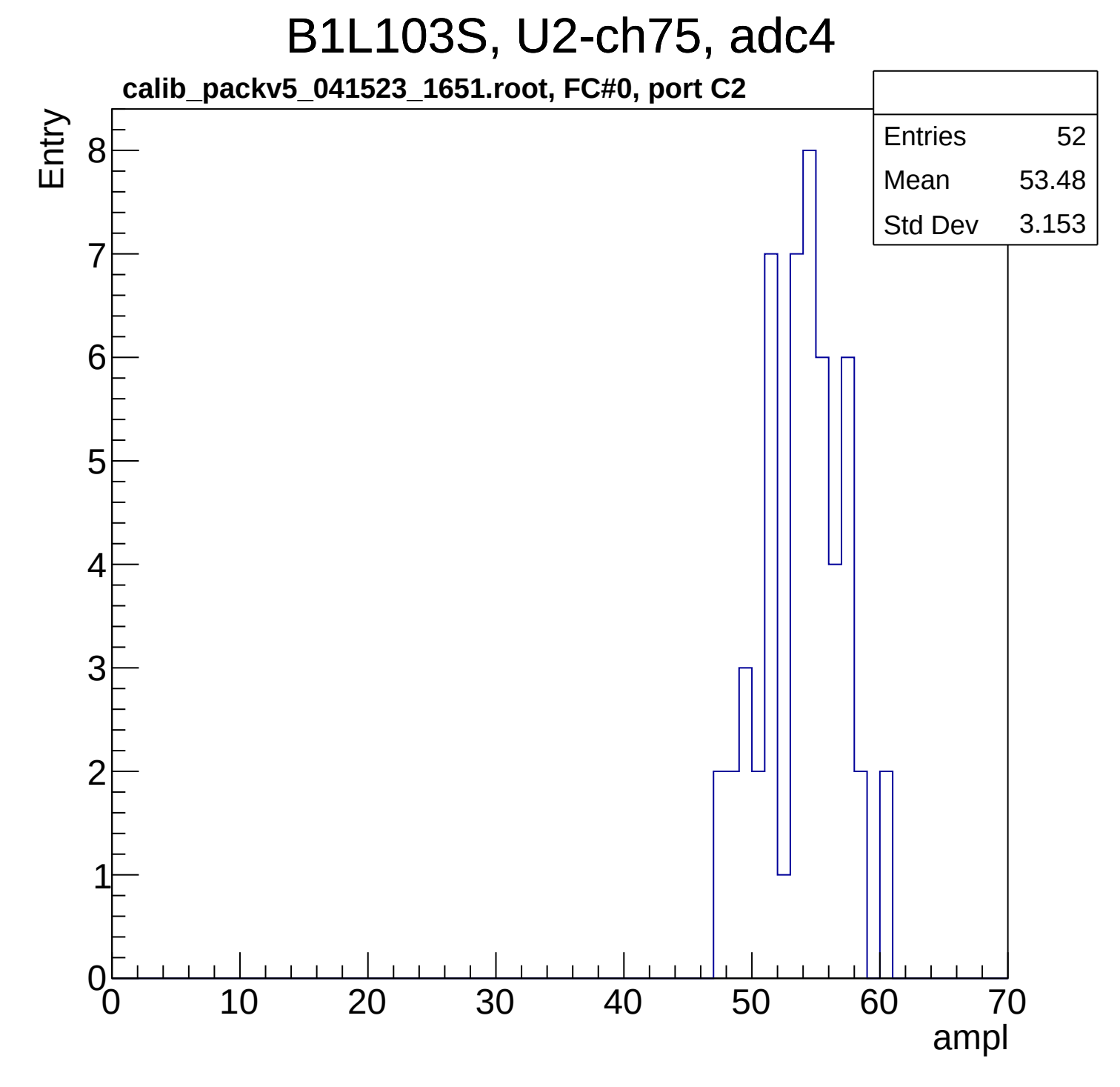

B1L103S, U2-ch74, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 16.88
Std Dev 27.82
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

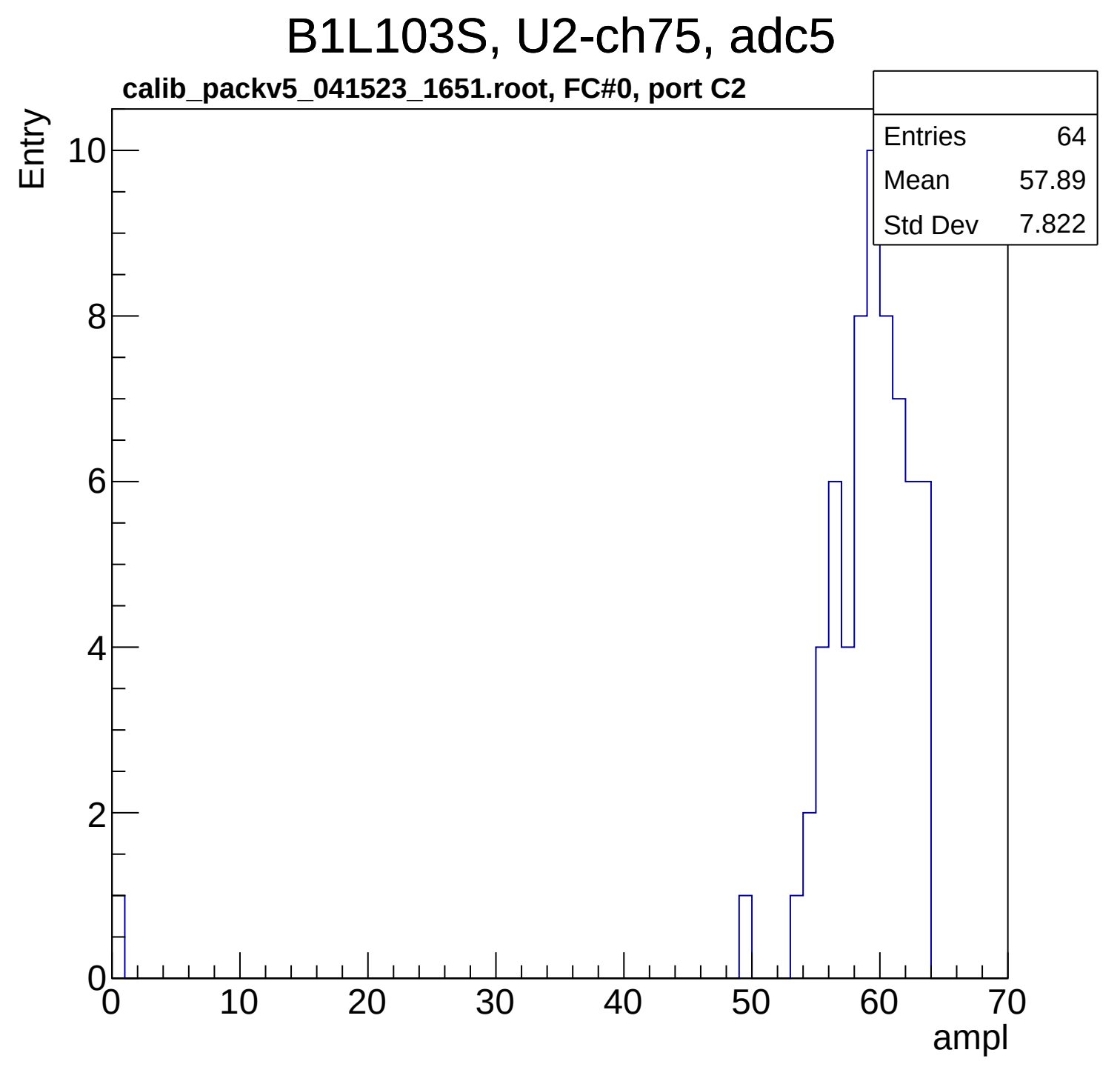

B1L103S, U2-ch75, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 25.38
Std Dev 10.05
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

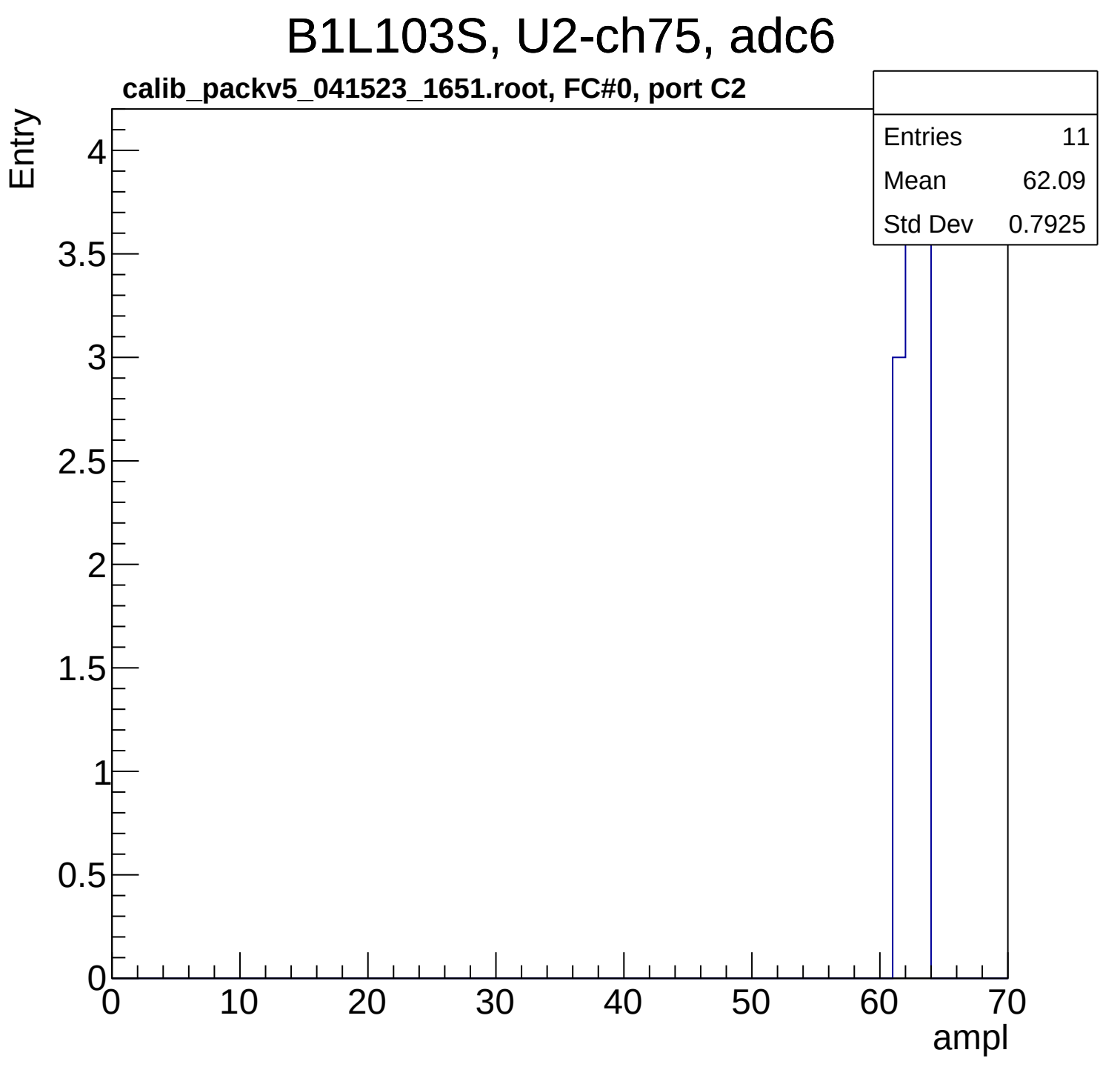

B1L103S, U2-ch75, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 29.2
Std Dev 14.41
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

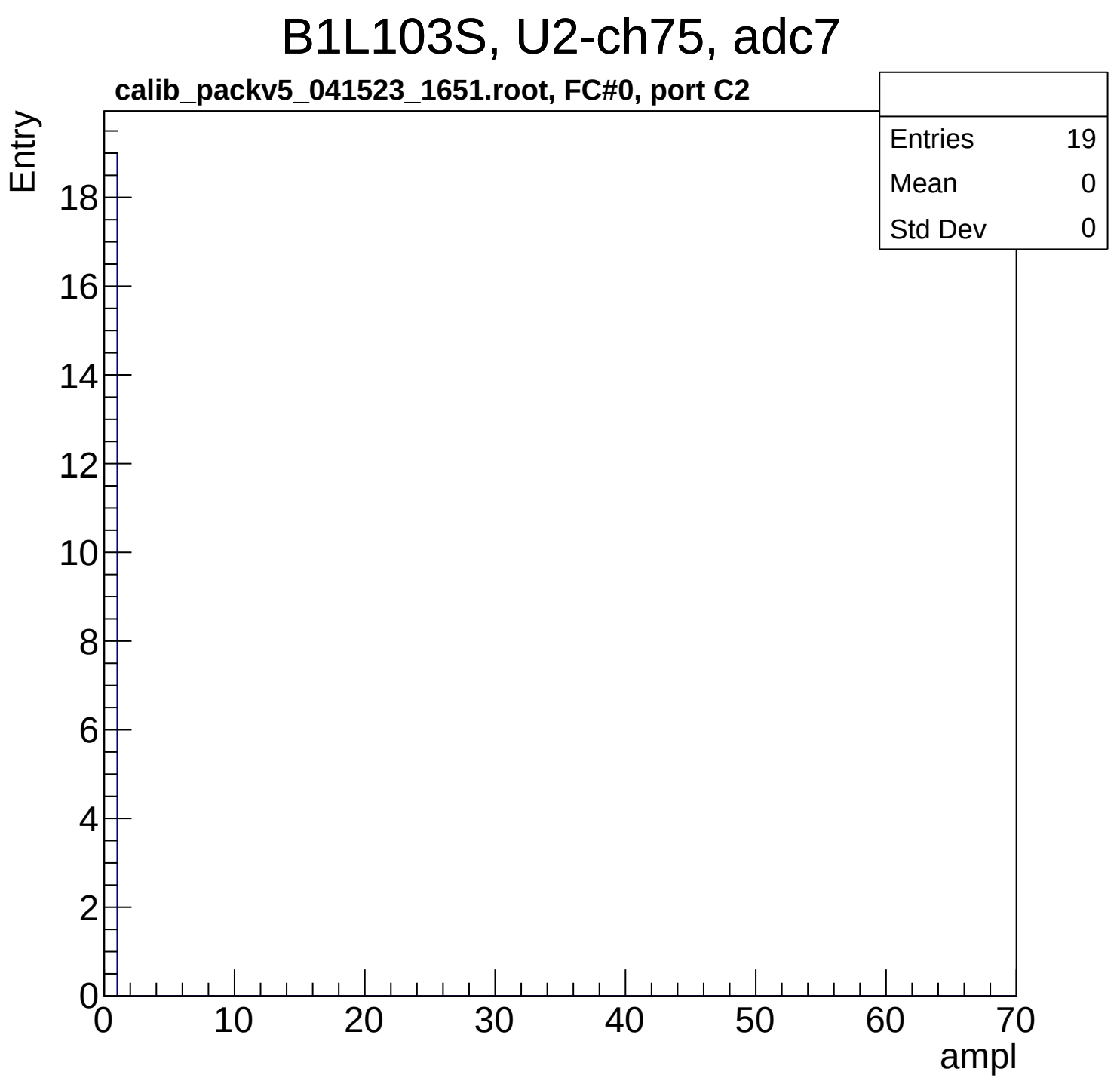

B1L103S, U2-ch75, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 41.28
Std Dev 6.139
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

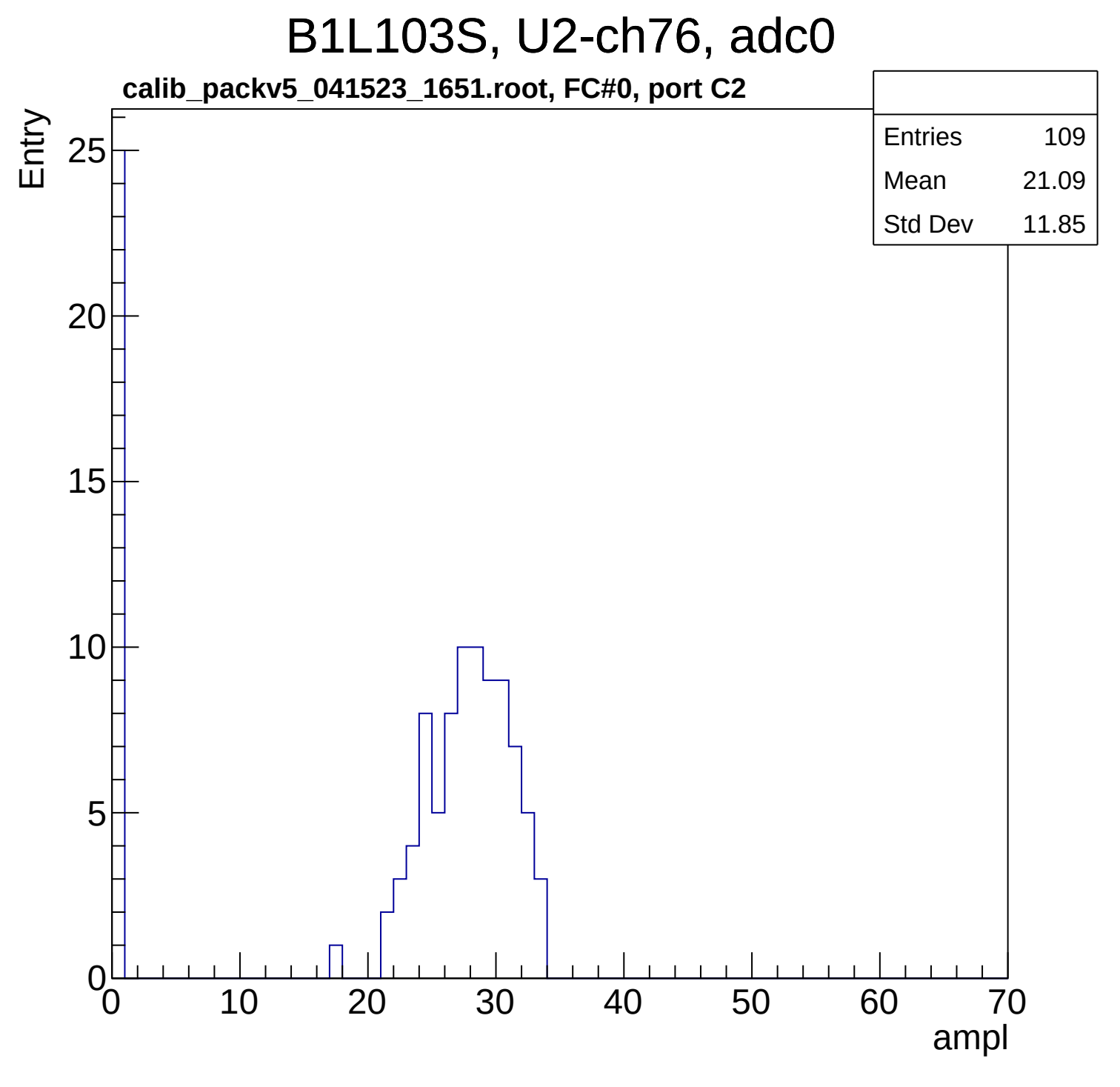

B1L103S, U2-ch75, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 47.16
Std Dev 6.804
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

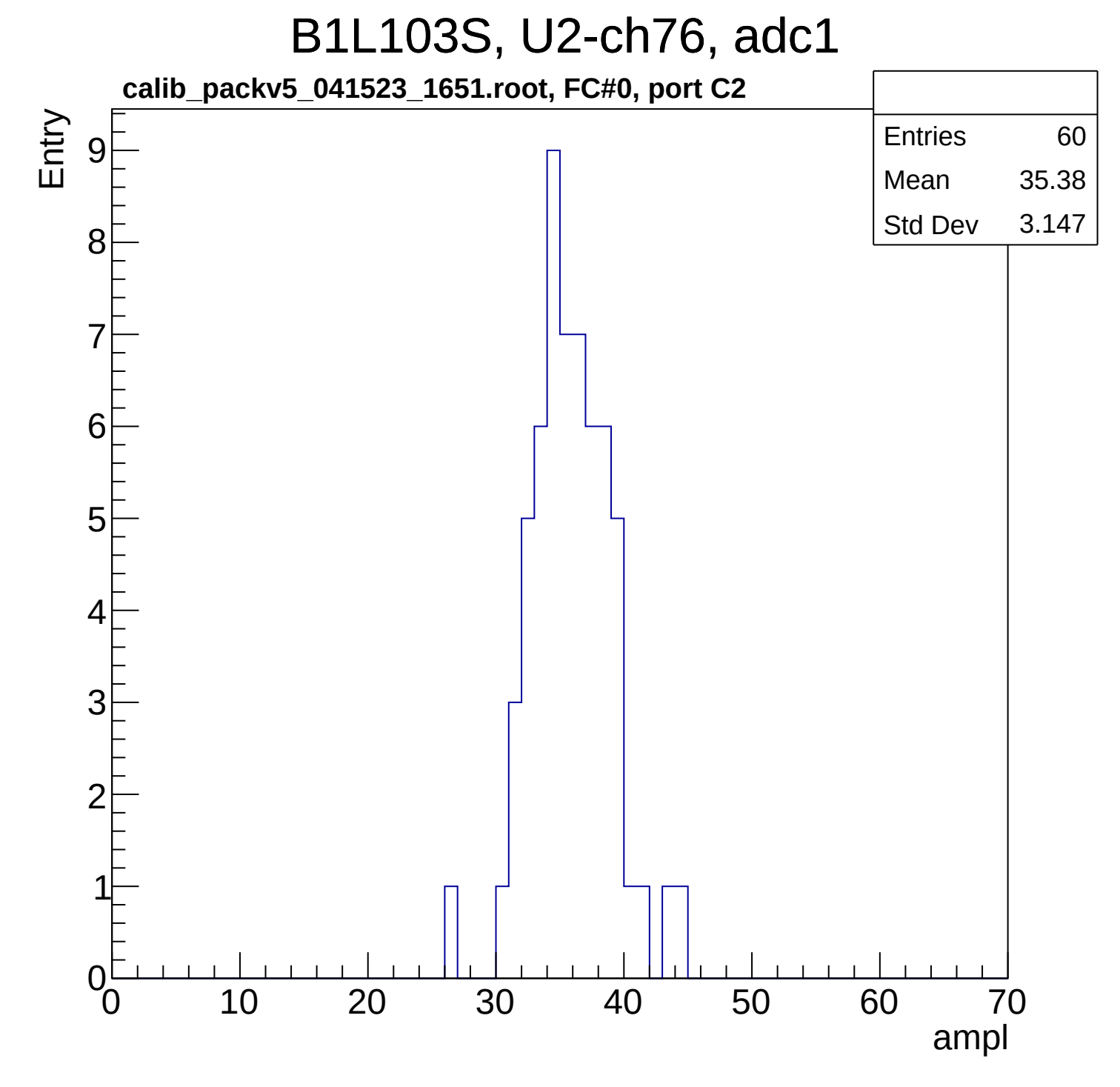

B1L103S, U2-ch75, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 53.48
Std Dev 3.153
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

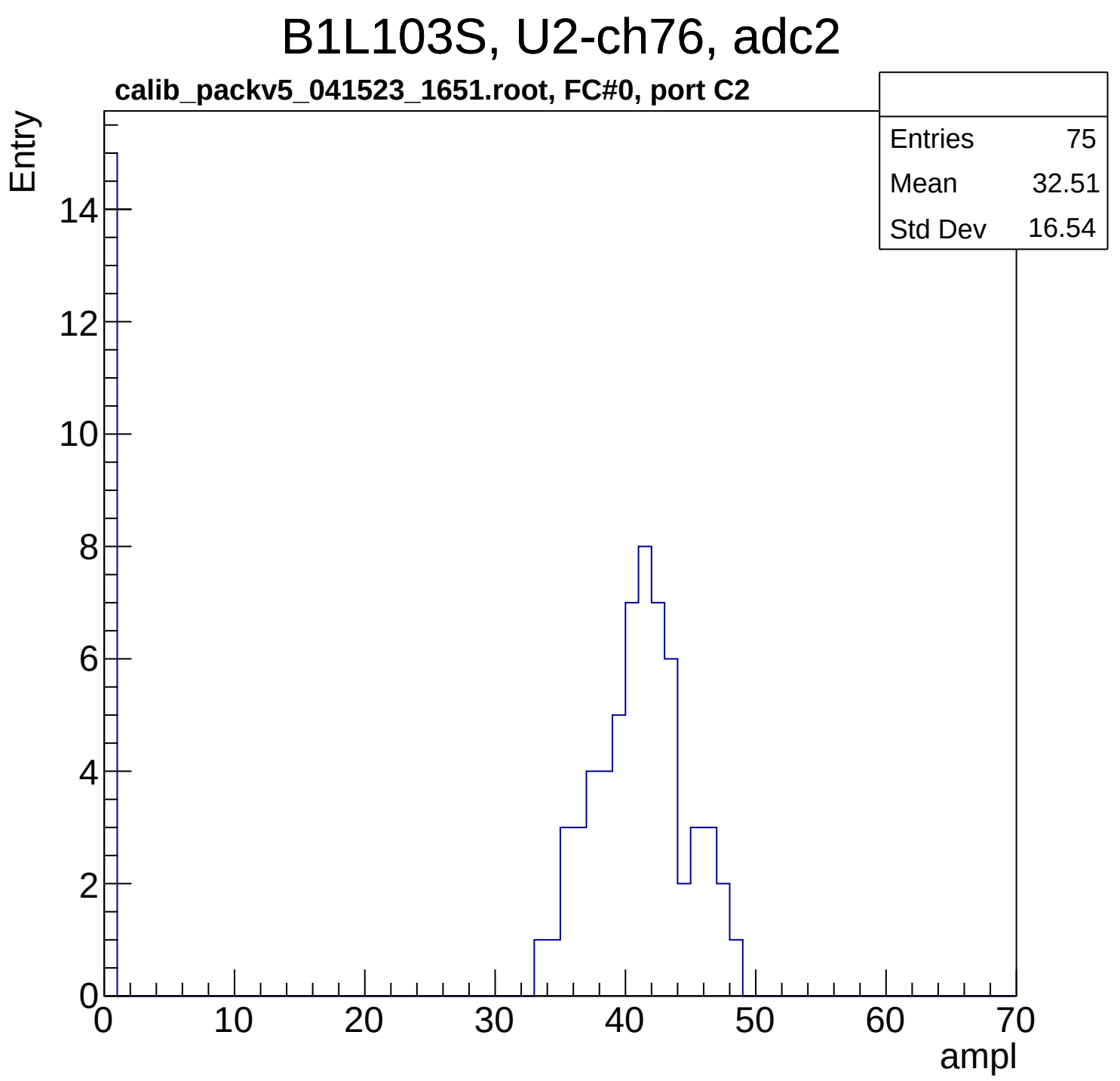

B1L103S, U2-ch75, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 57.89
Std Dev 7.822
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

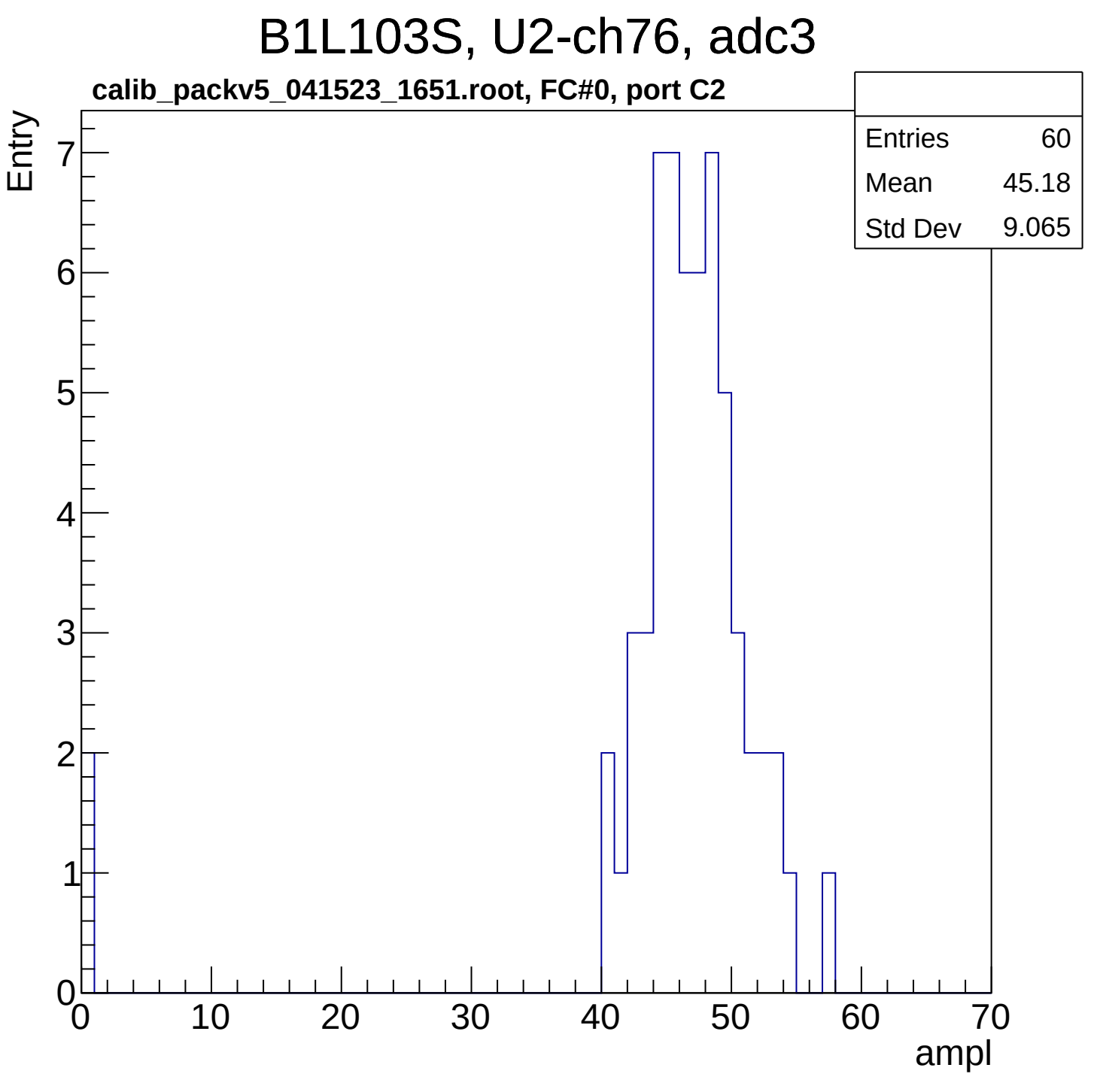

B1L103S, U2-ch75, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 62.09
Std Dev 0.7925
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

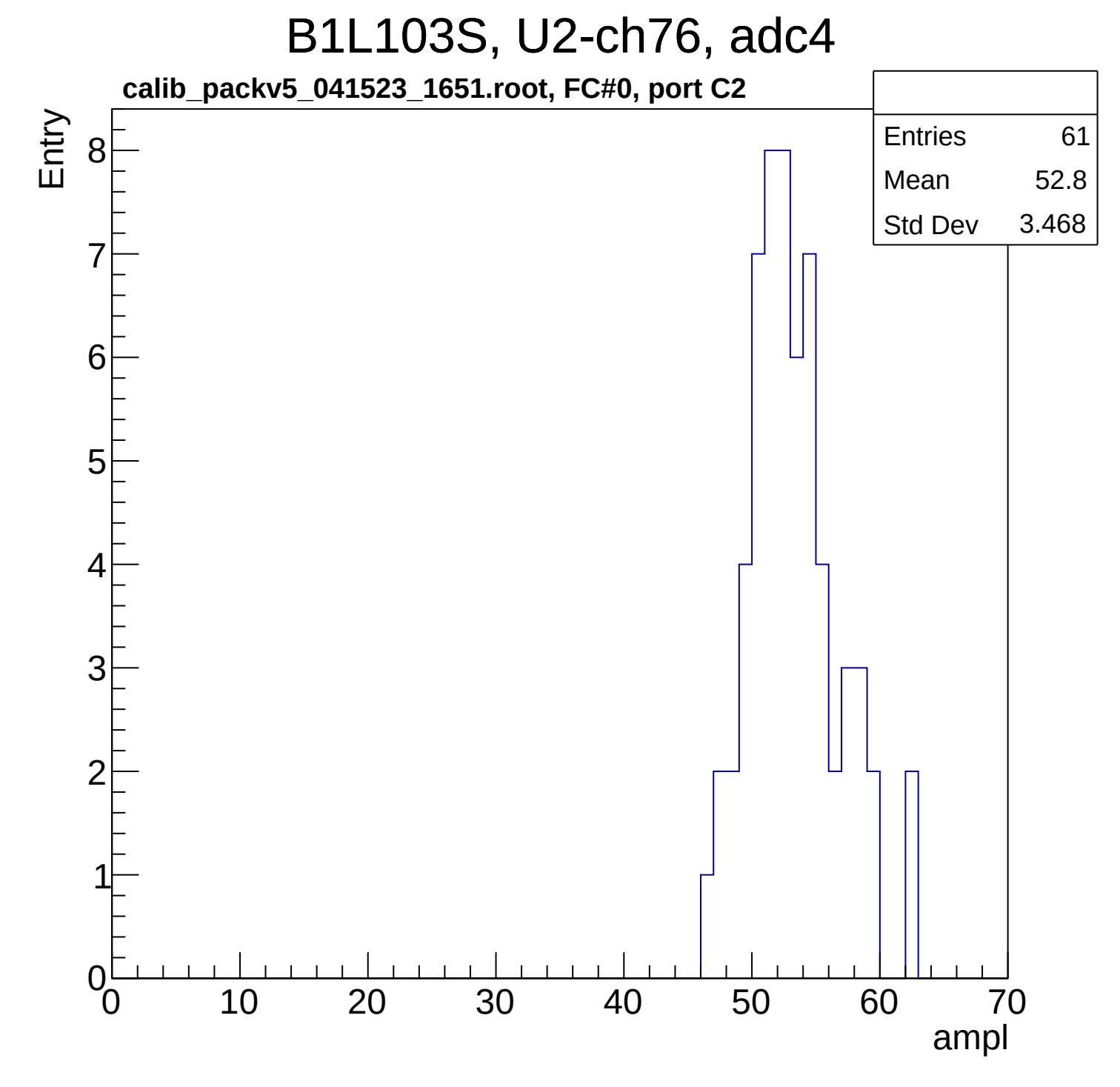

B1L103S, U2-ch75, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

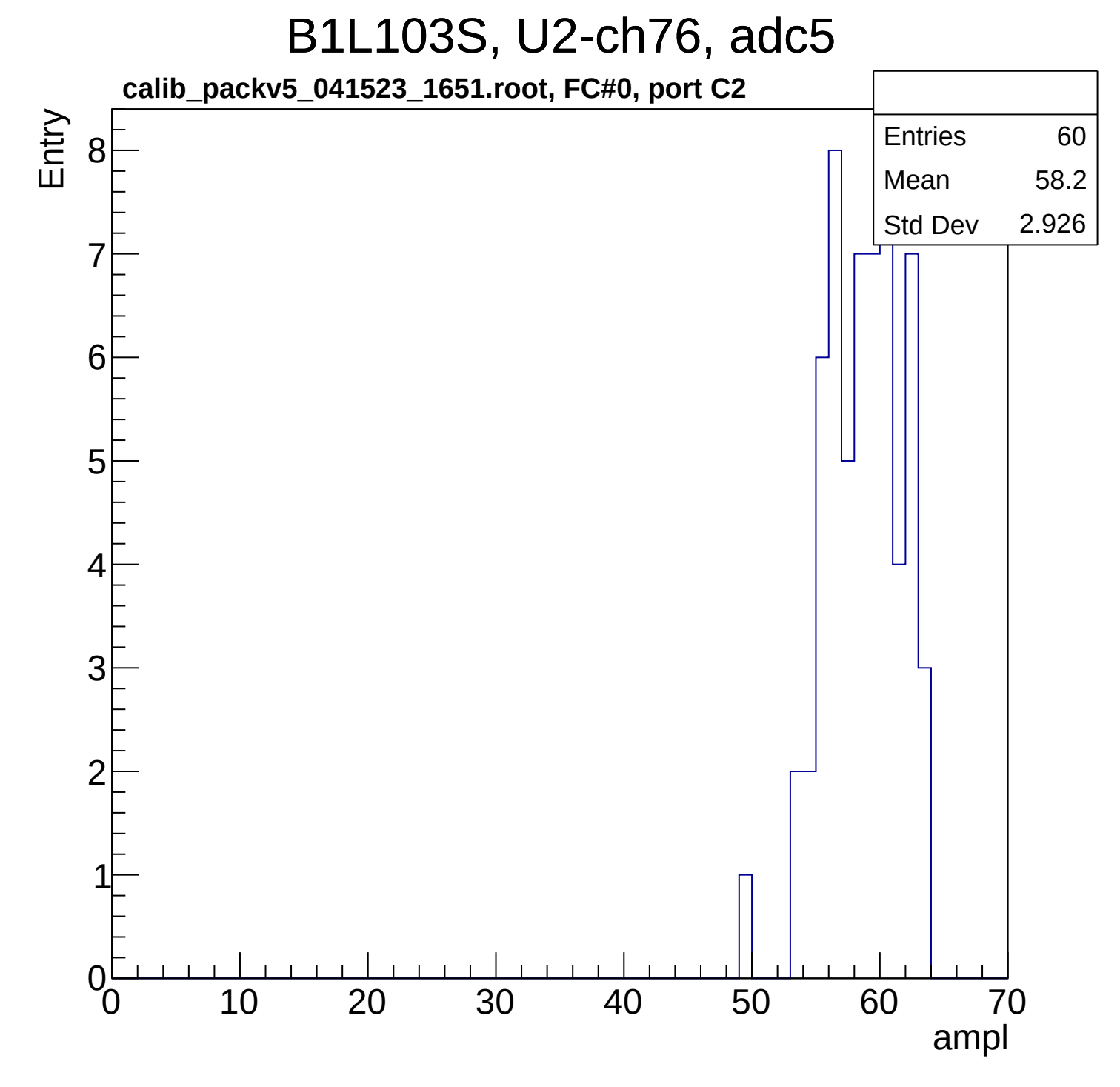

B1L103S, U2-ch76, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 109
Mean 21.09
Std Dev 11.85
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl

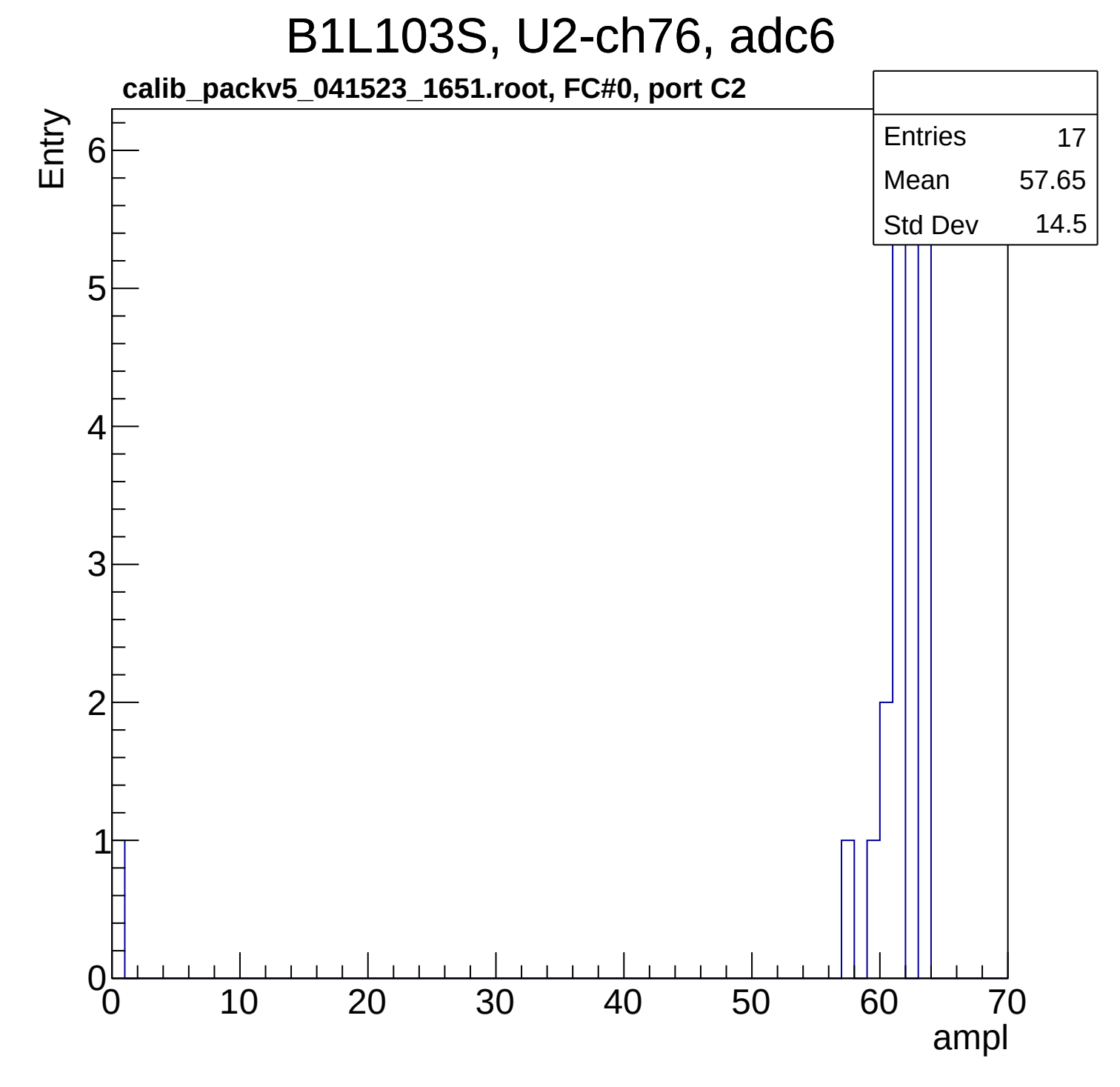

B1L103S, U2-ch76, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 35.38
Std Dev 3.147
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

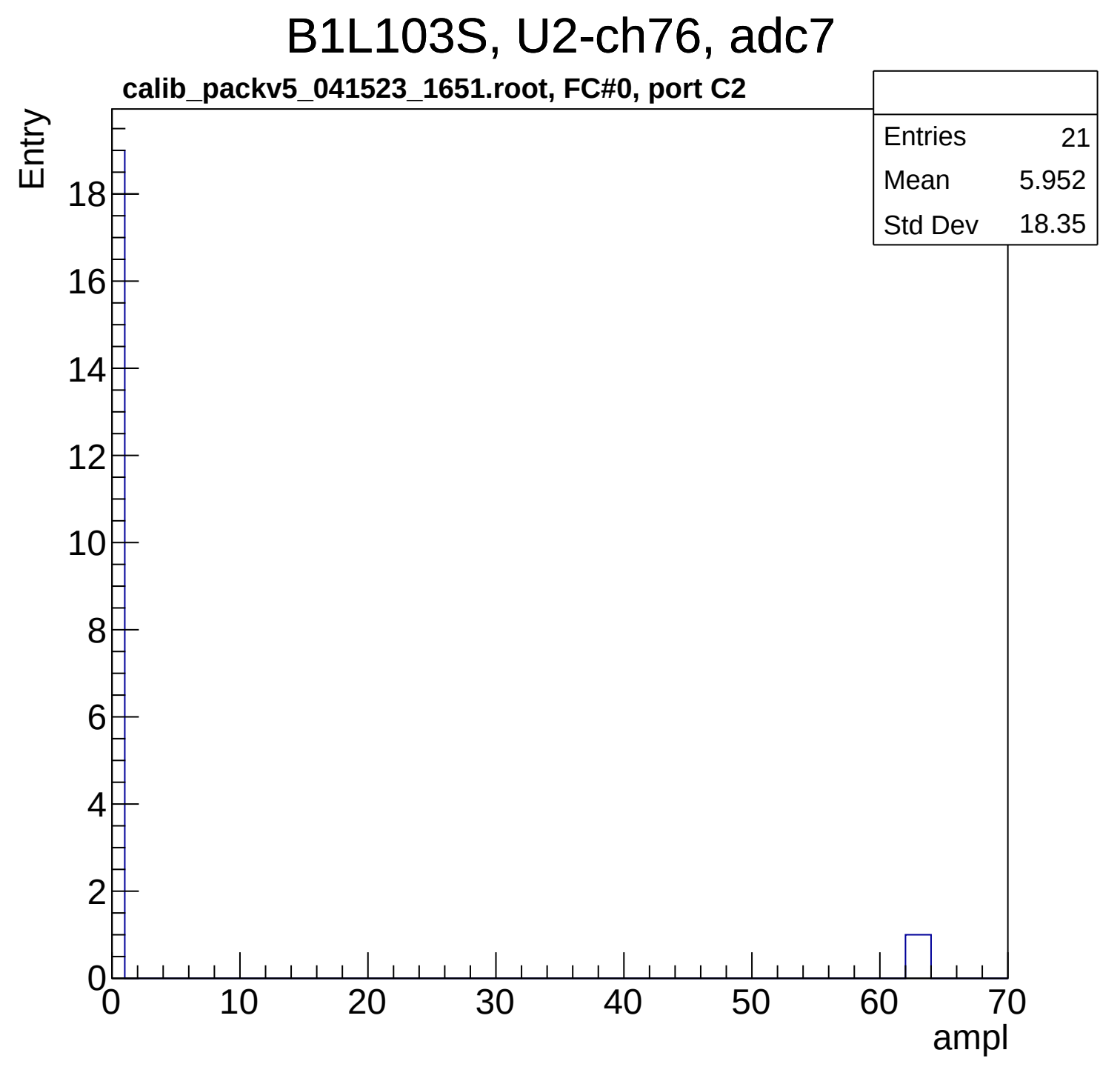

B1L103S, U2-ch76, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 32.51
Std Dev 16.54
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

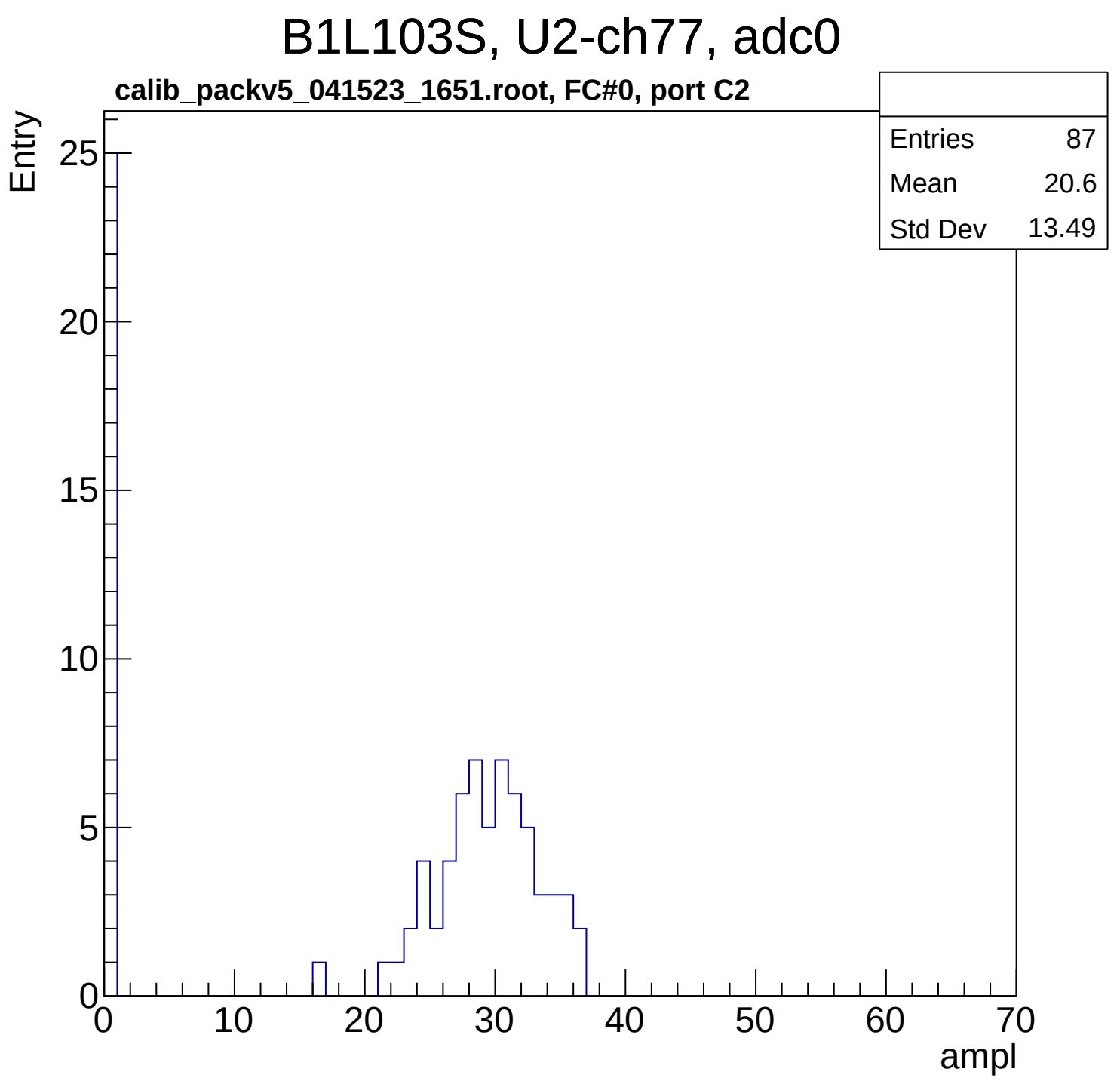

B1L103S, U2-ch76, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 45.18
Std Dev 9.065
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

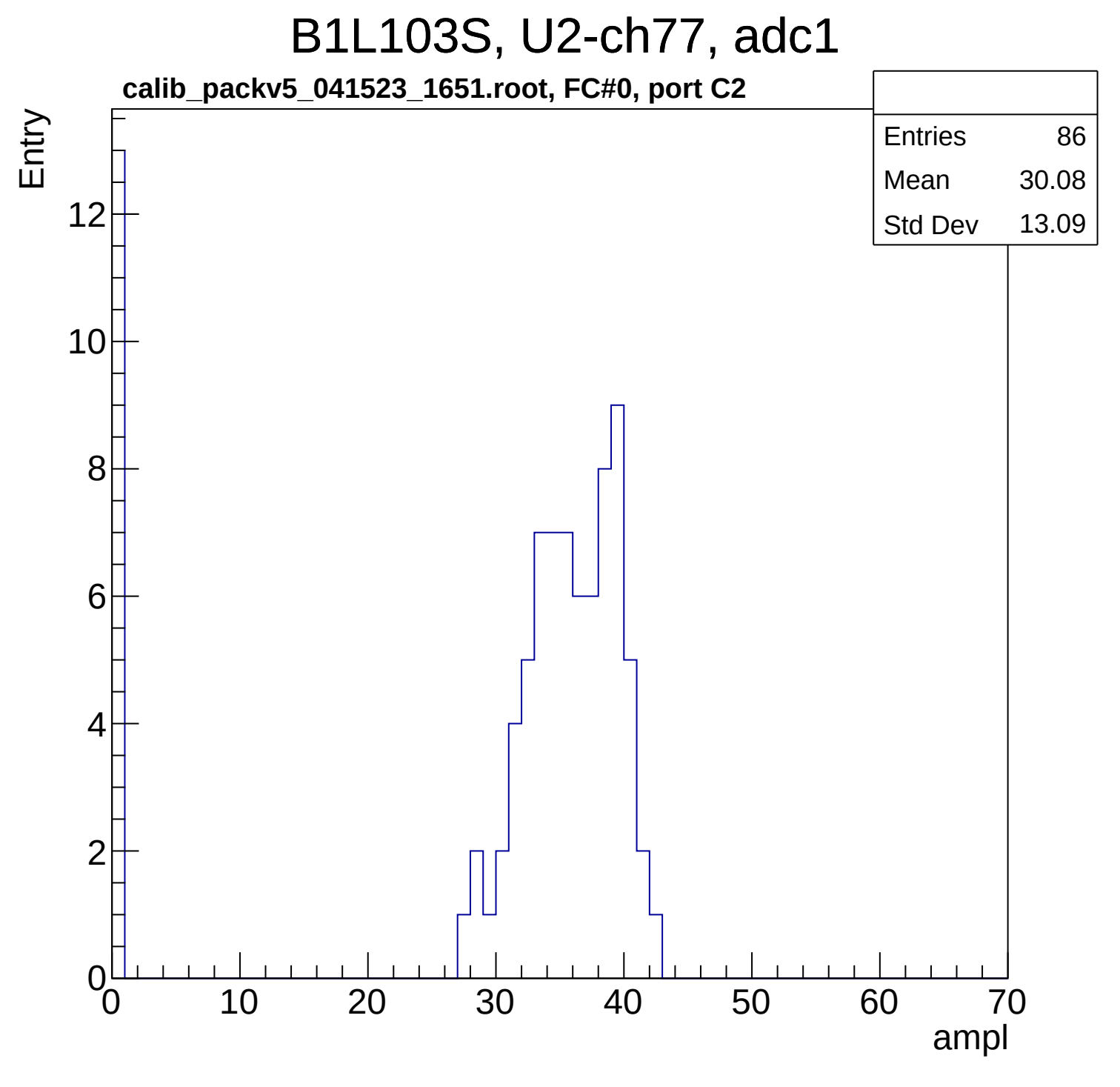

B1L103S, U2-ch76, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 52.8
Std Dev 3.468
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

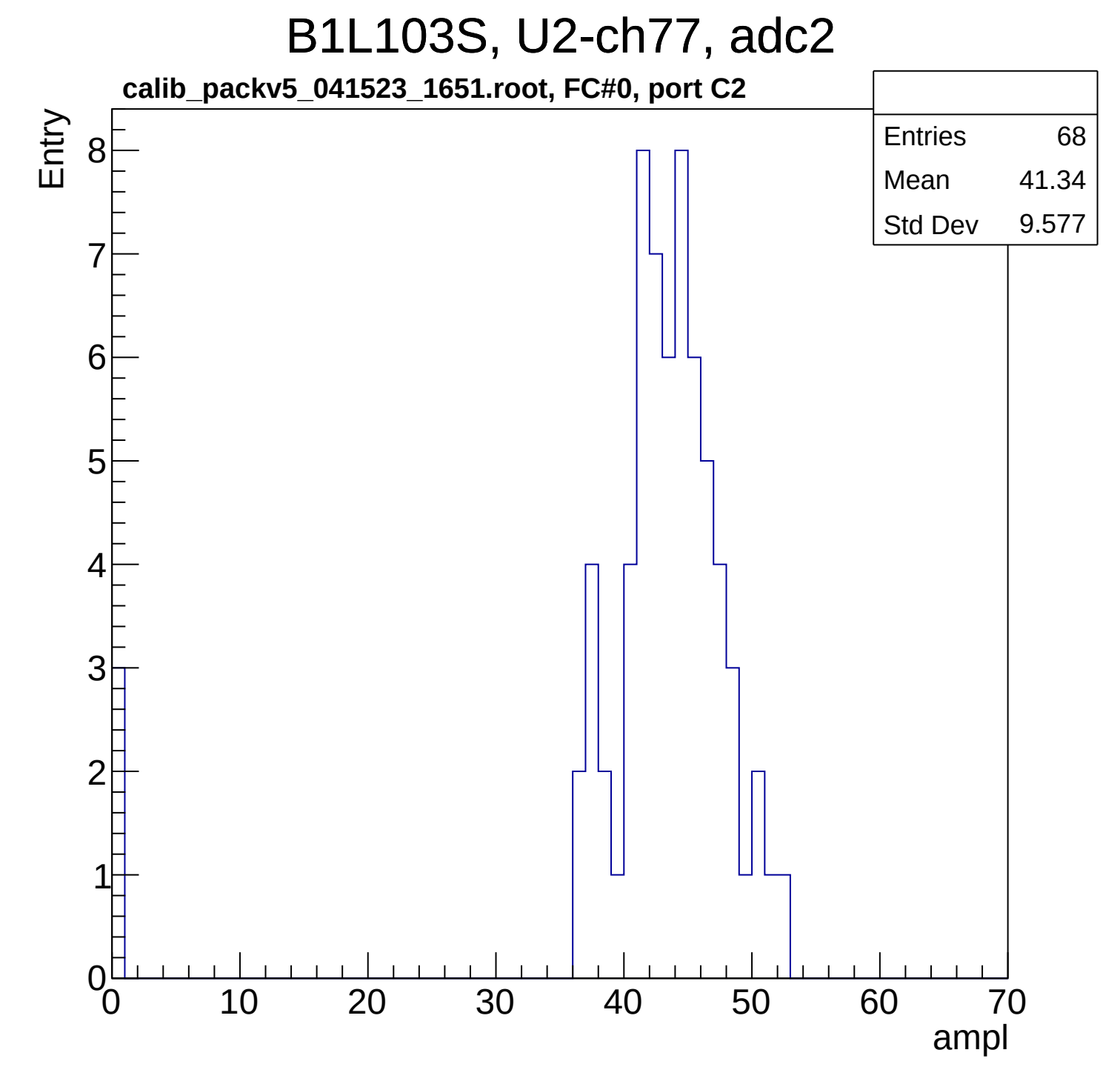

B1L103S, U2-ch76, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 58.2
Std Dev 2.926
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

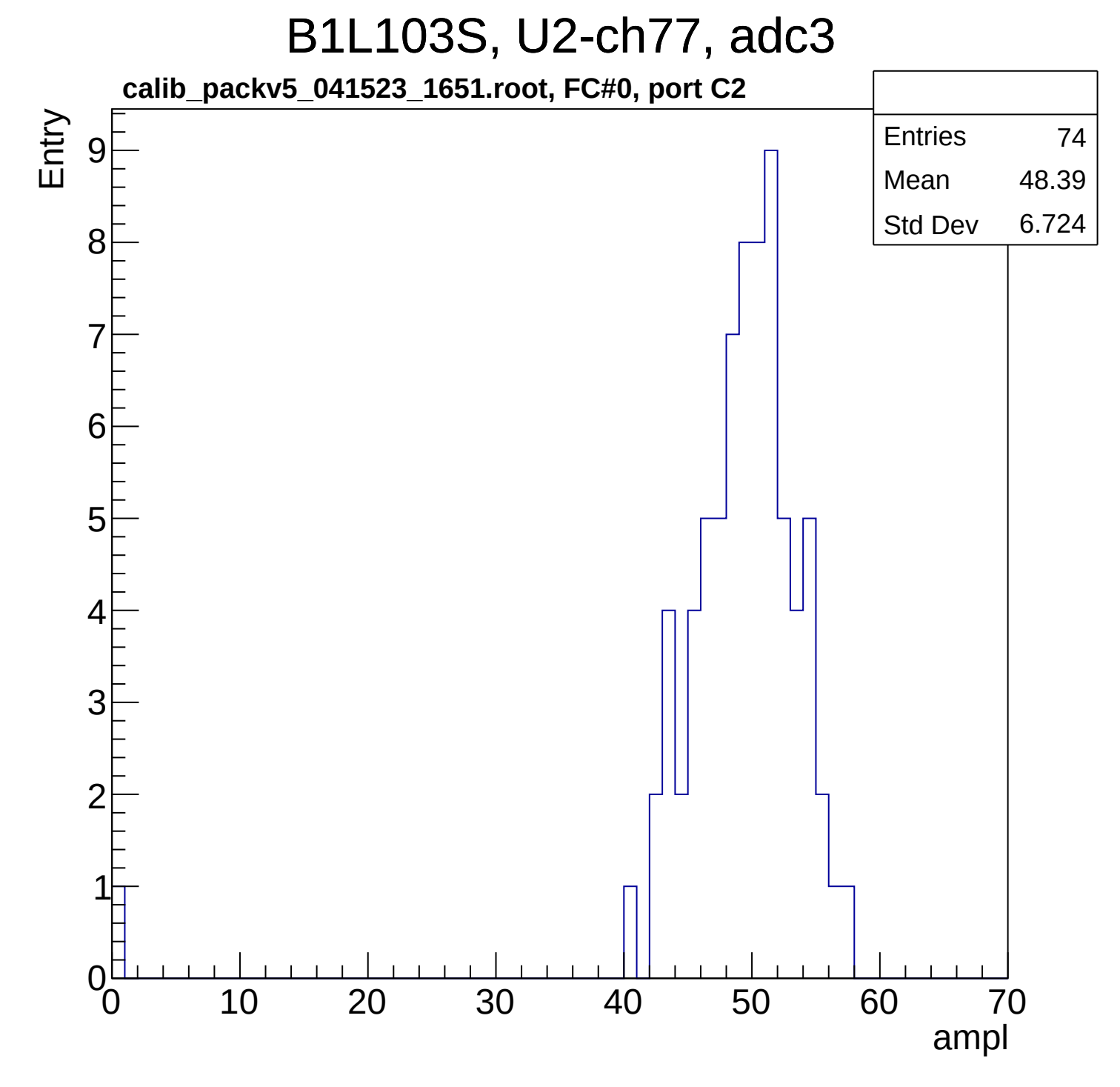

B1L103S, U2-ch76, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 57.65
Std Dev 14.5
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

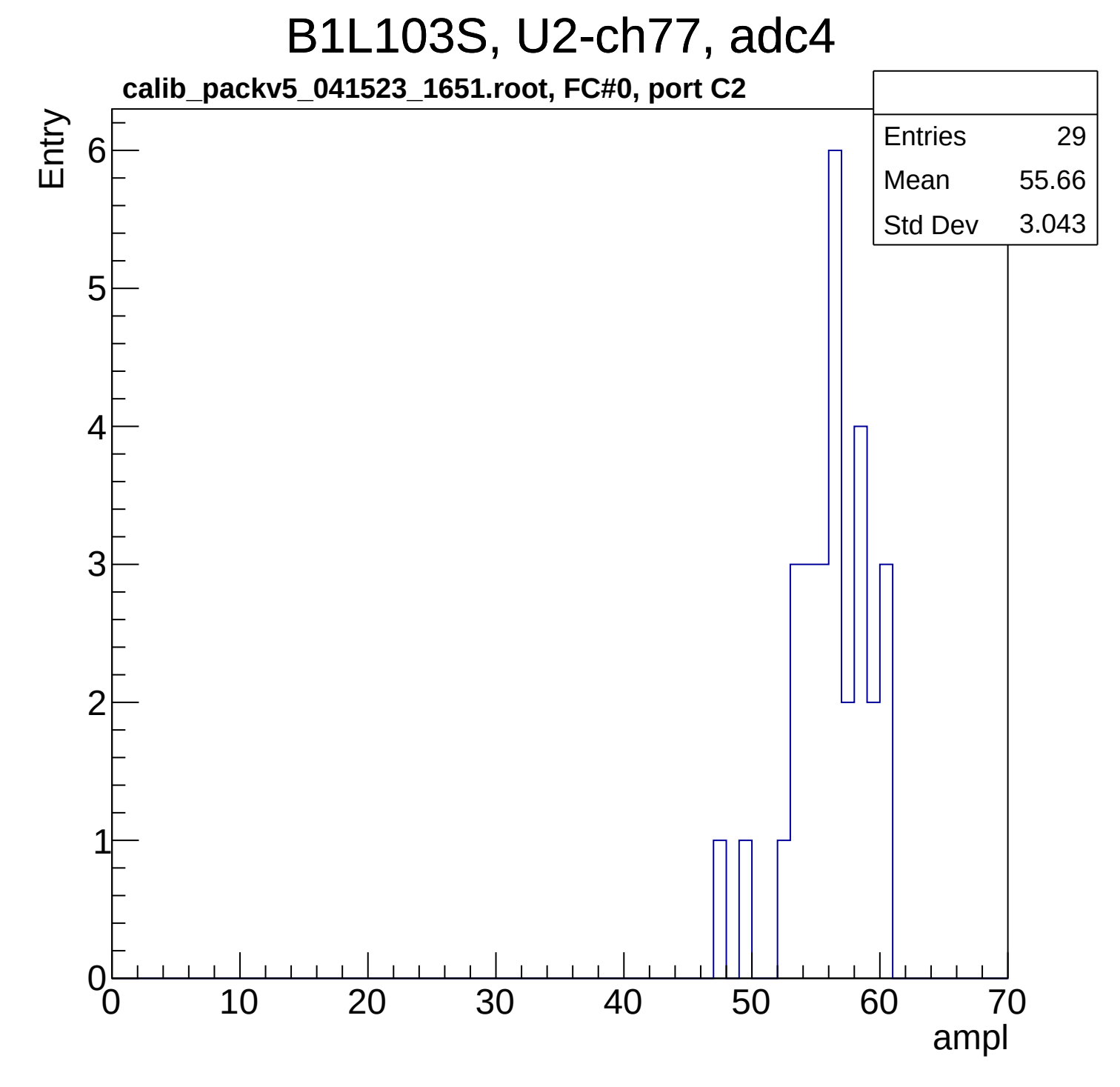

B1L103S, U2-ch76, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

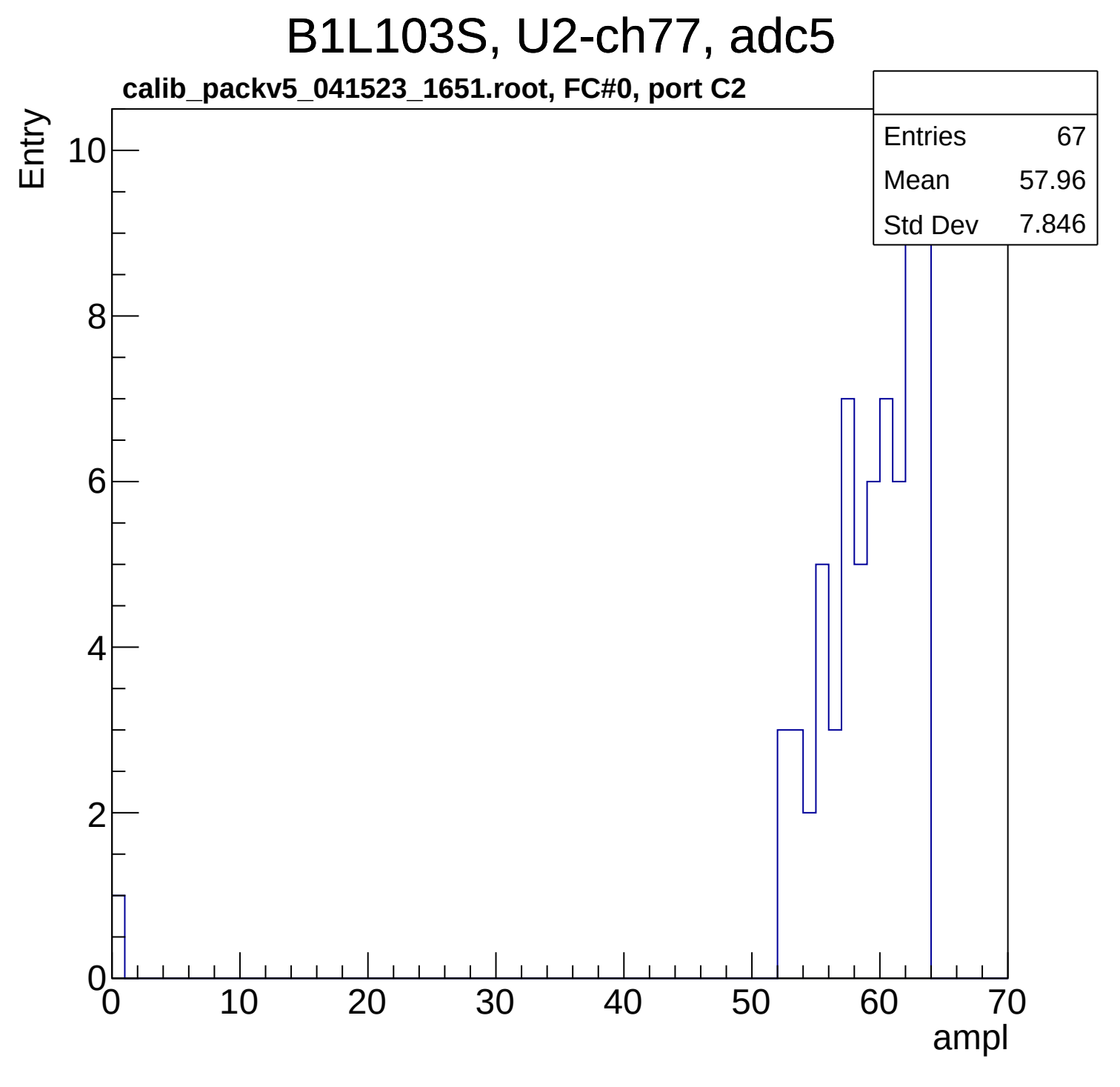

B1L103S, U2-ch77, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 20.6
Std Dev 13.49
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl

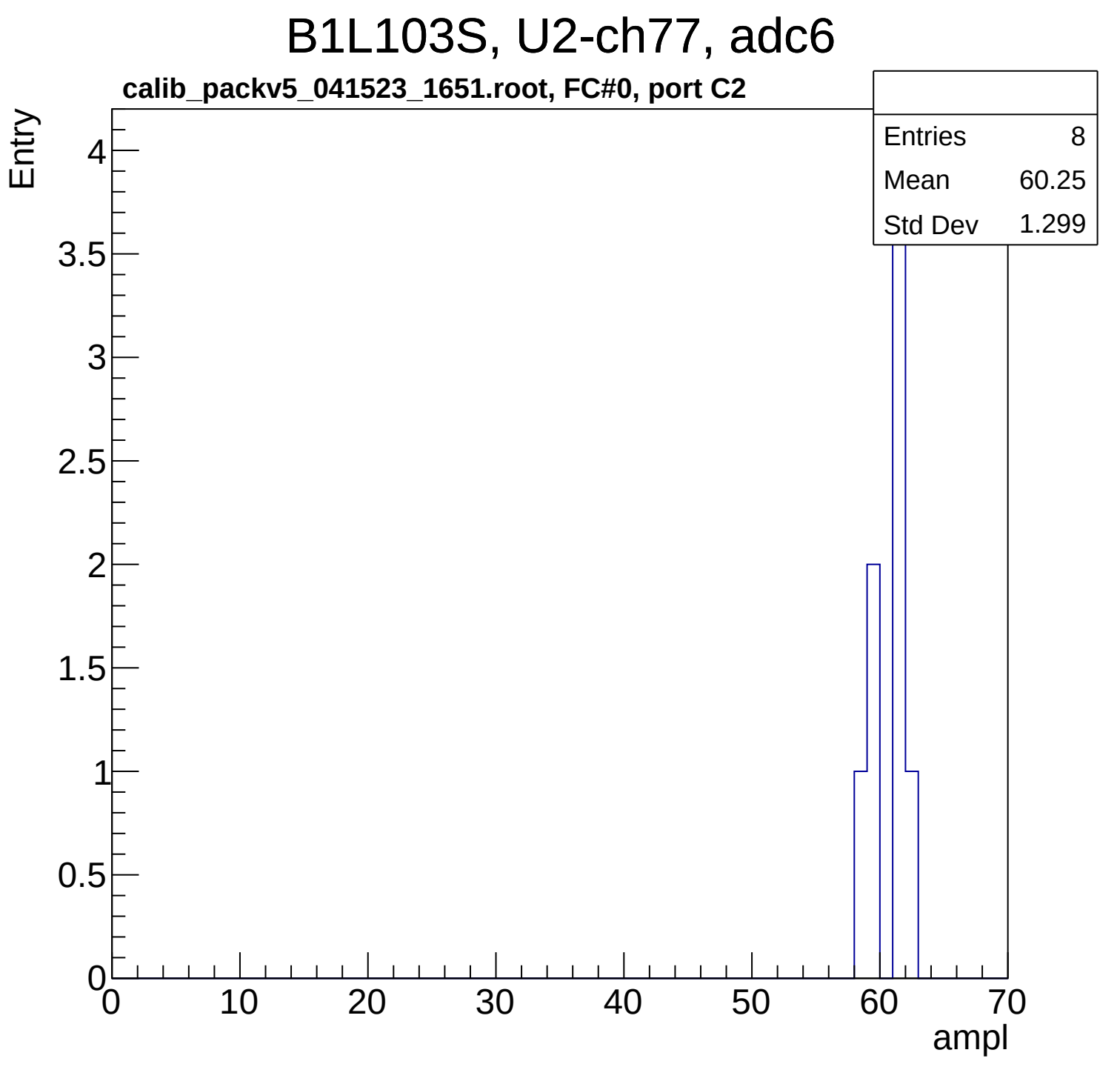

B1L103S, U2-ch77, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 30.08
Std Dev 13.09
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

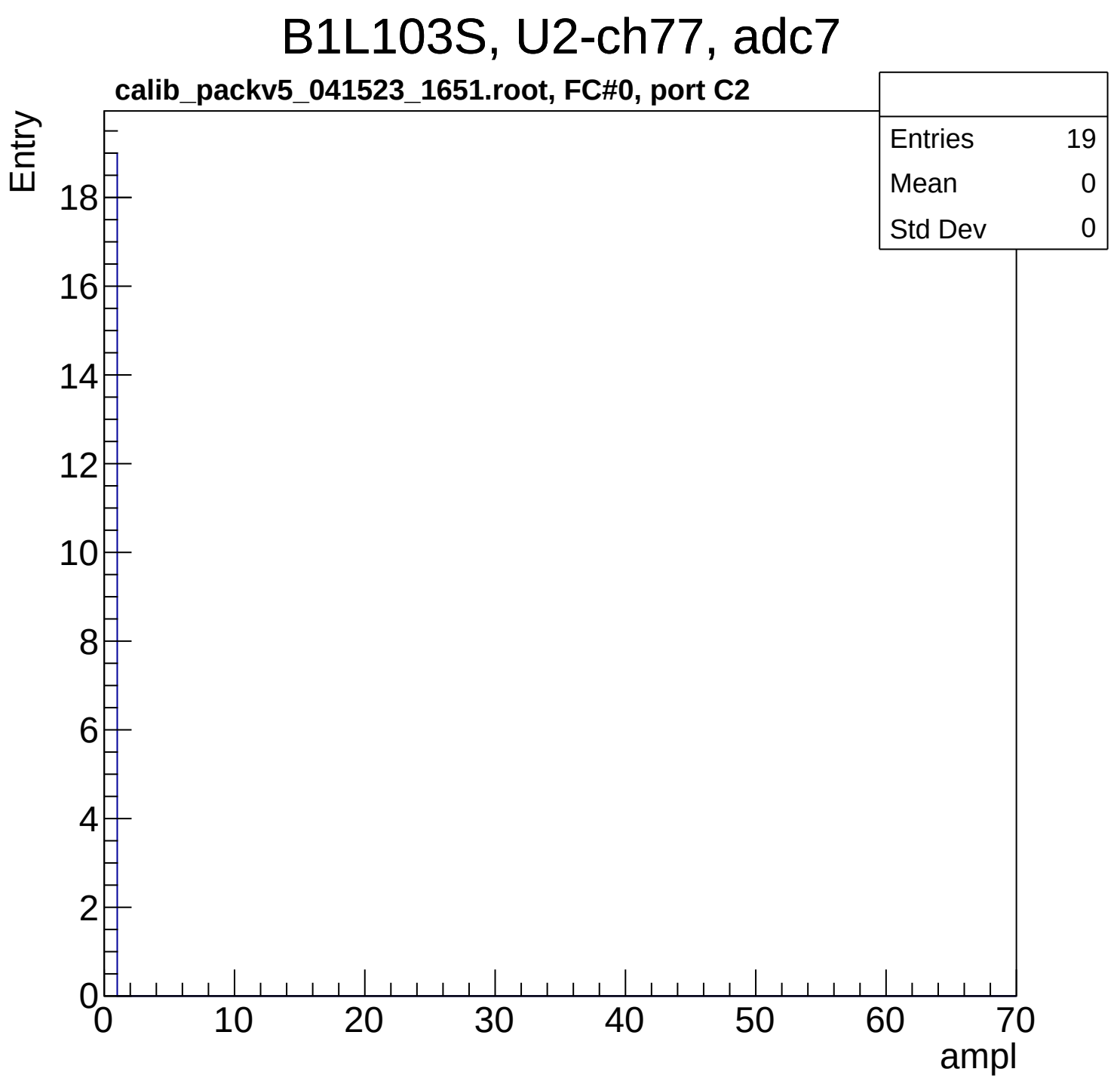

B1L103S, U2-ch77, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 41.34
Std Dev 9.577
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

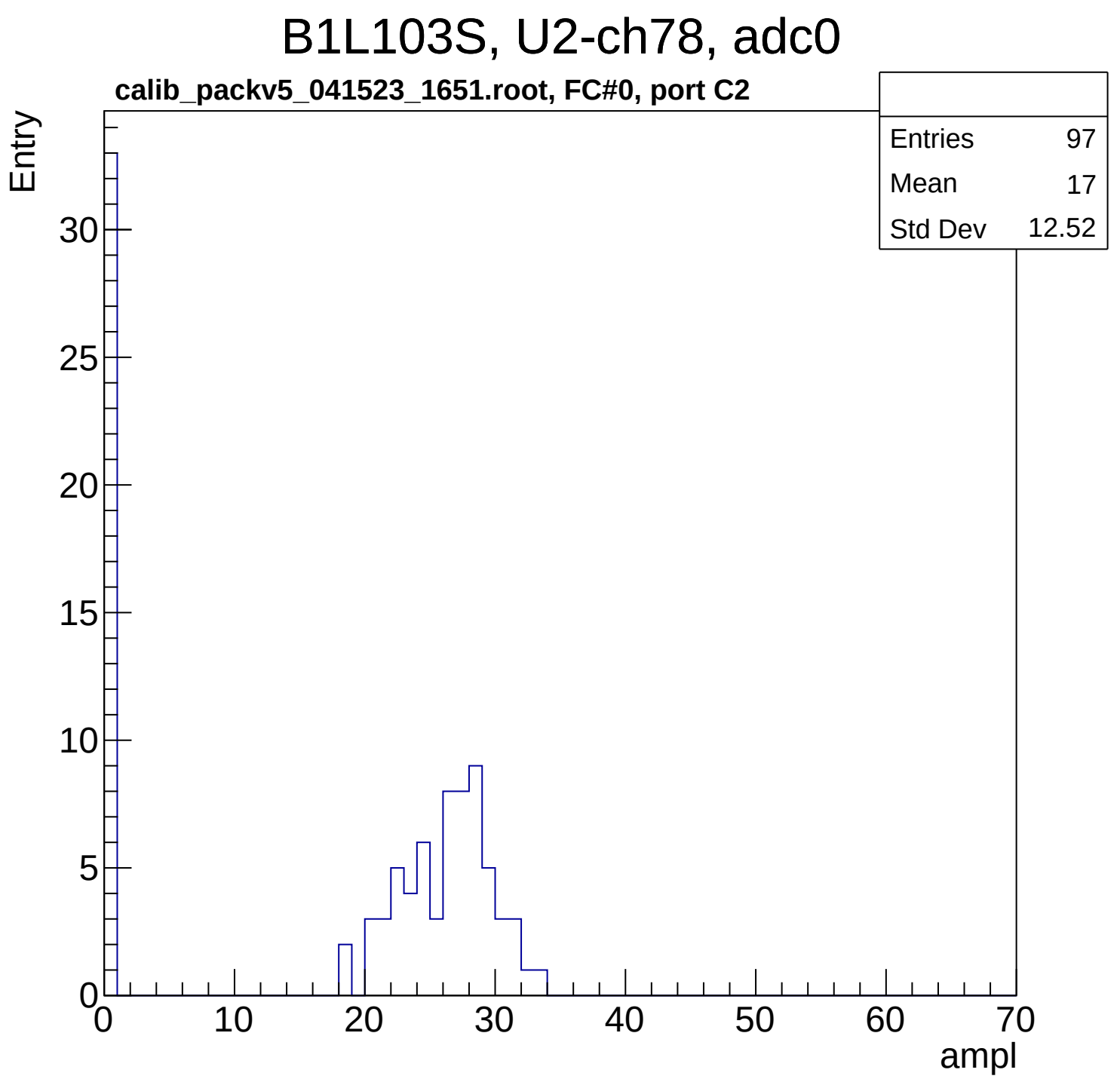

B1L103S, U2-ch77, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 48.39
Std Dev 6.724
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

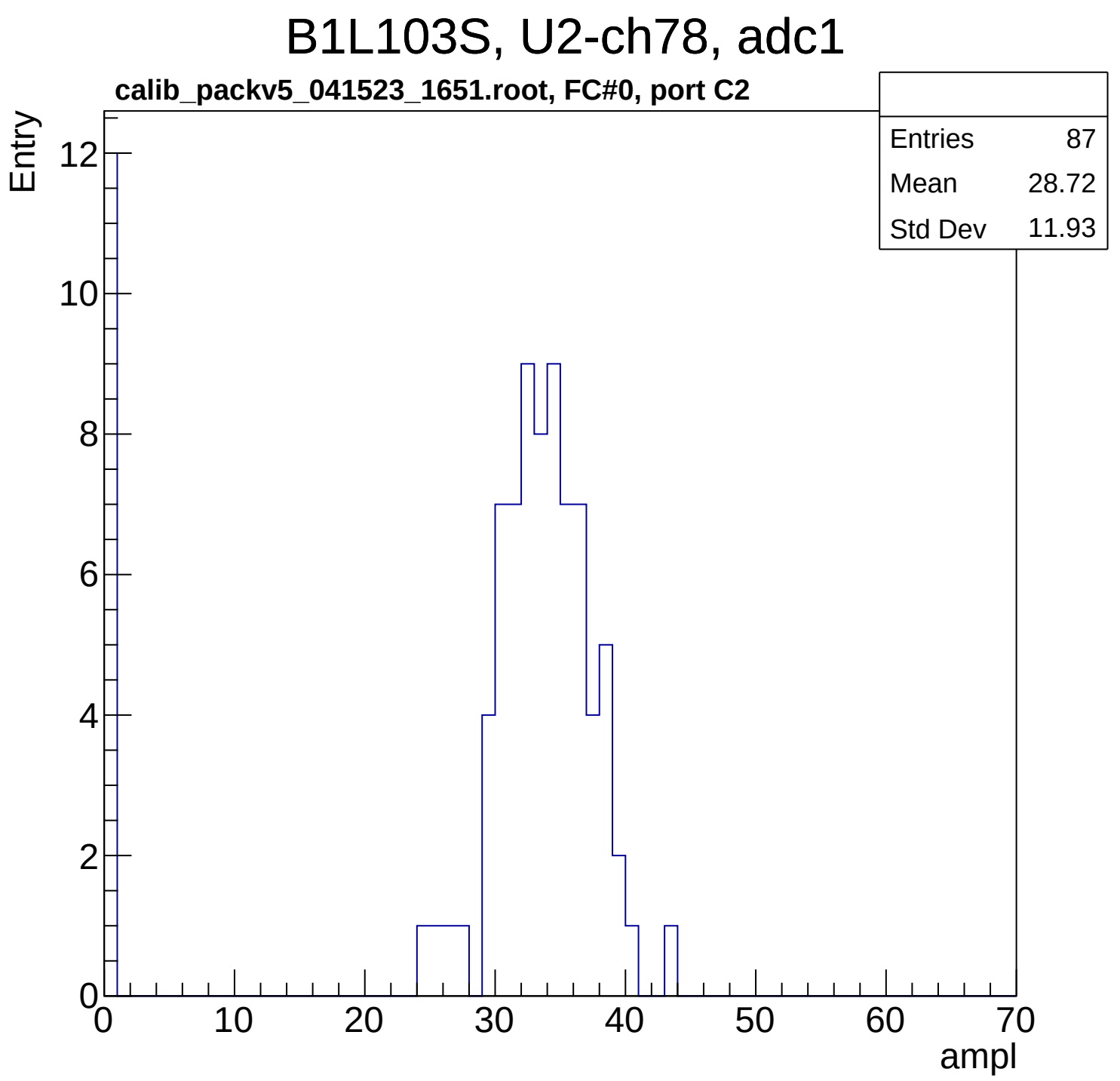

B1L103S, U2-ch77, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 55.66
Std Dev 3.043
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

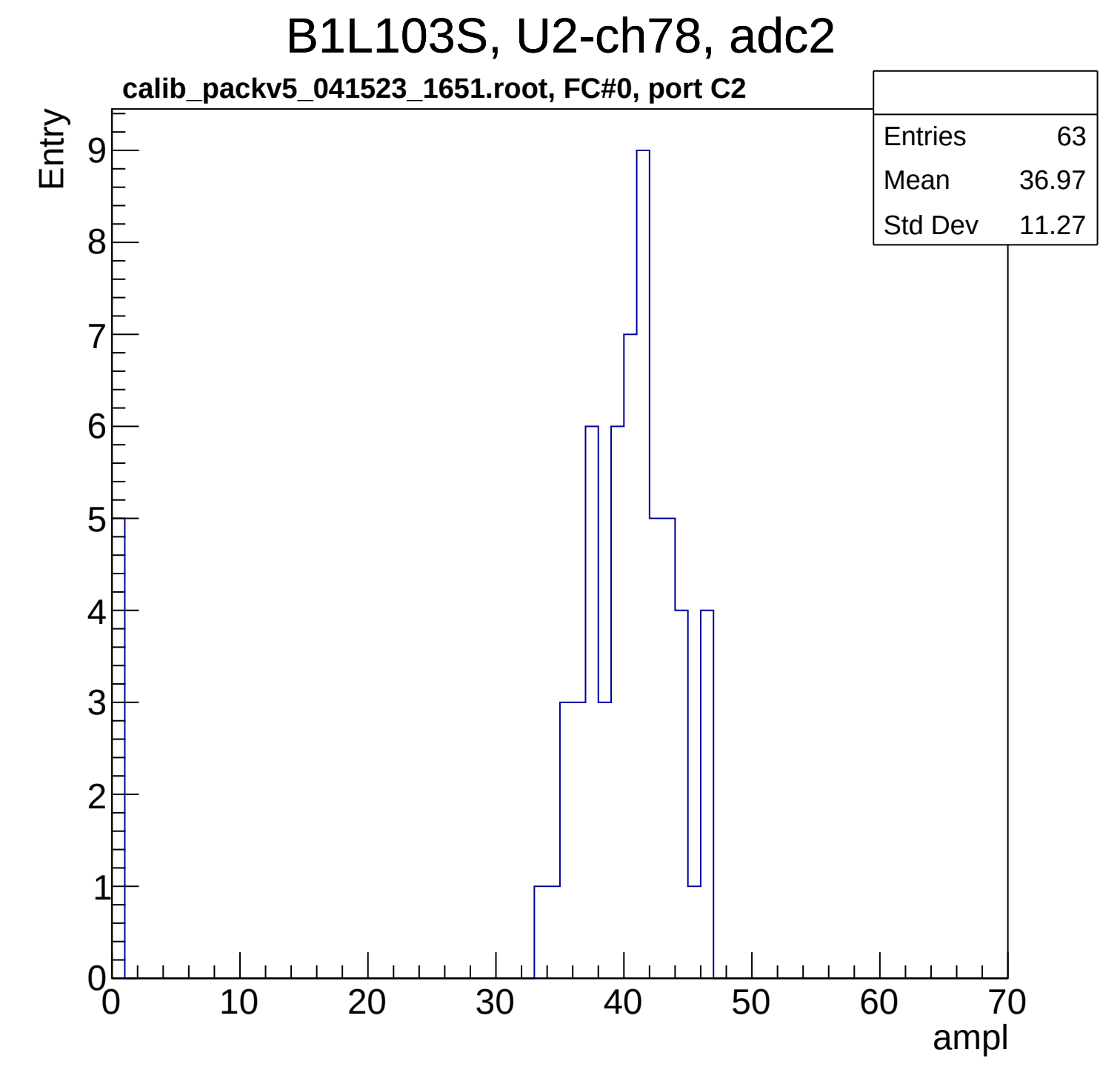

B1L103S, U2-ch77, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 57.96
Std Dev 7.846
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

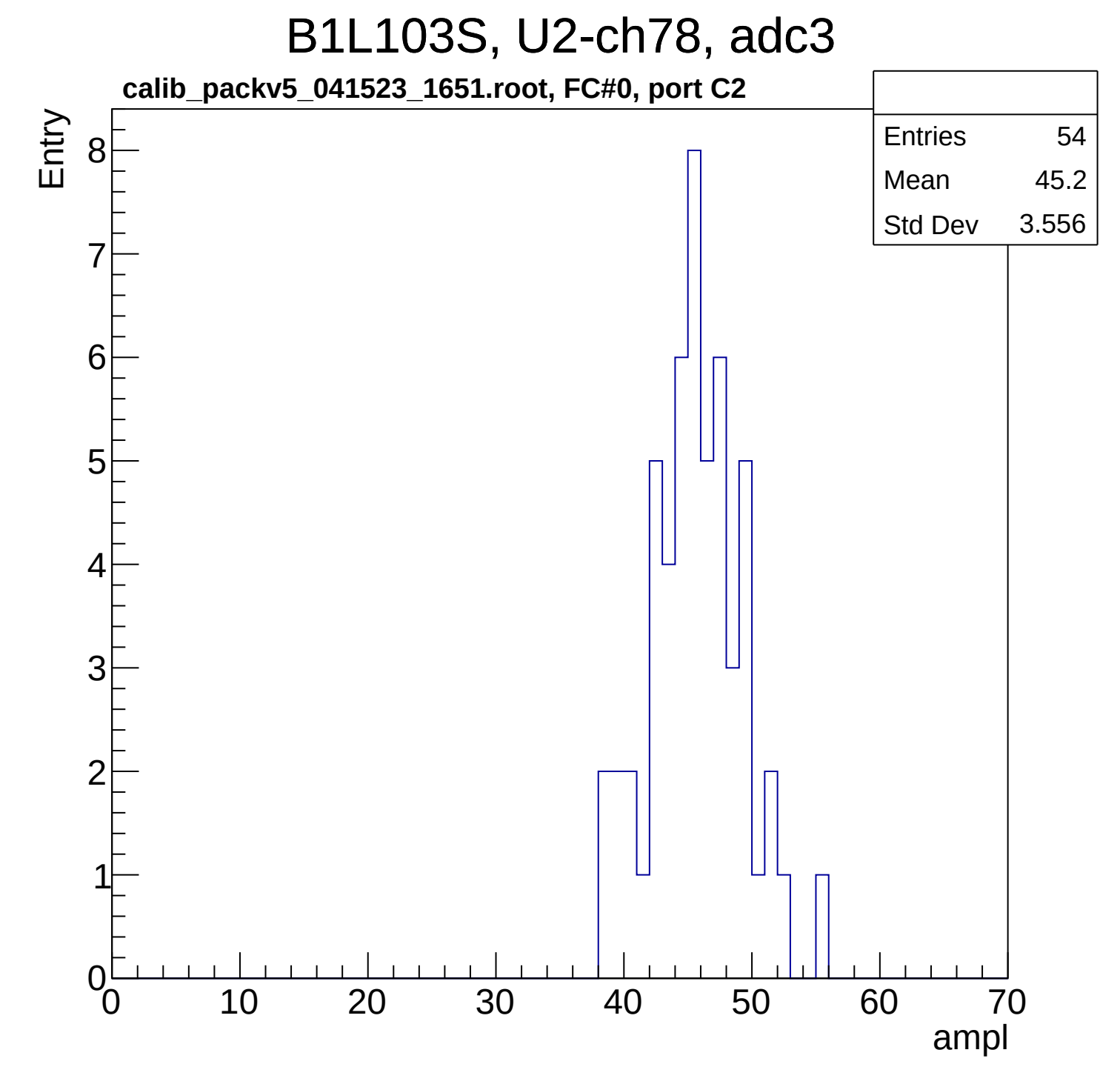

B1L103S, U2-ch77, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 60.25
Std Dev 1.299
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

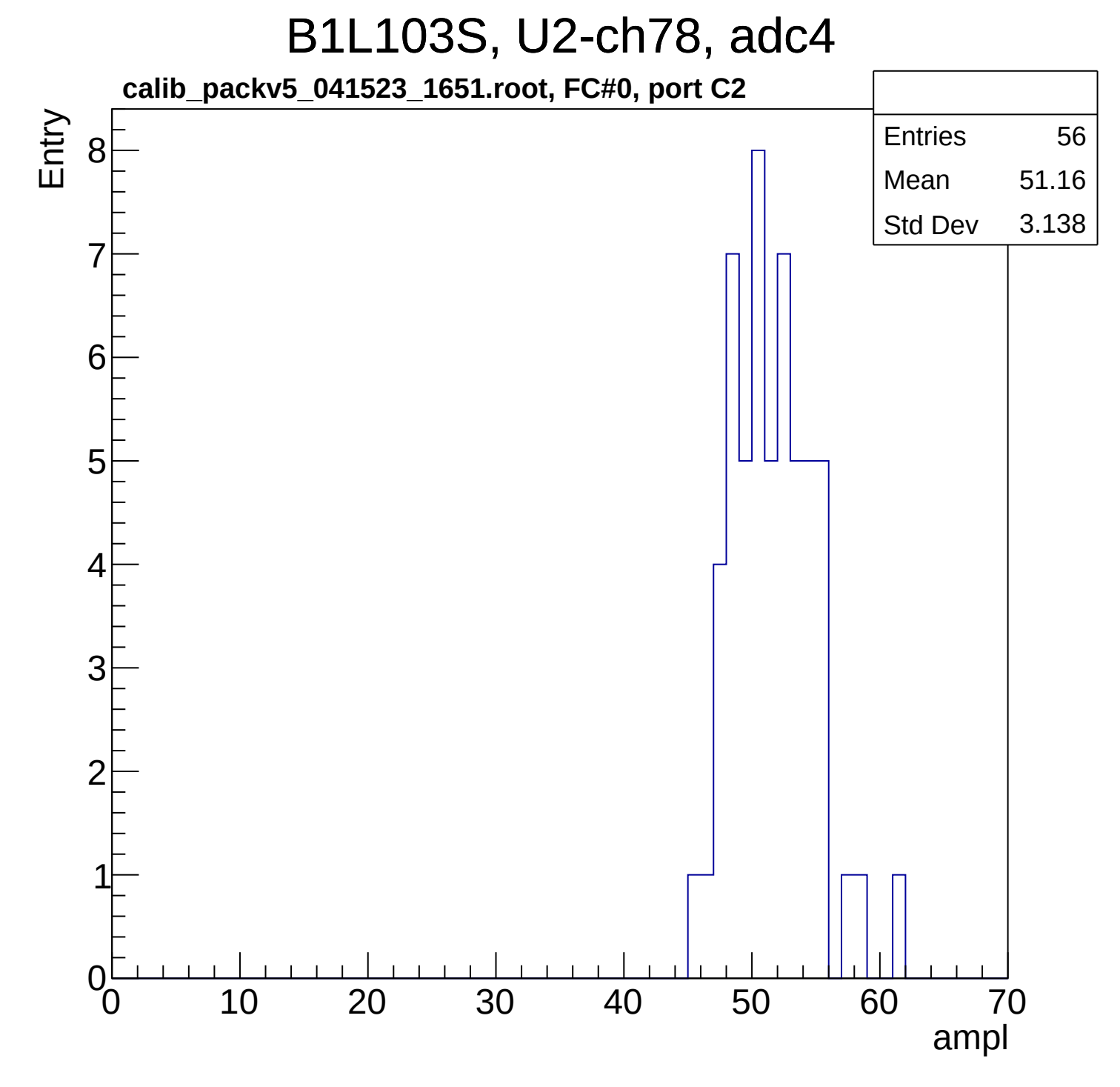

B1L103S, U2-ch77, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

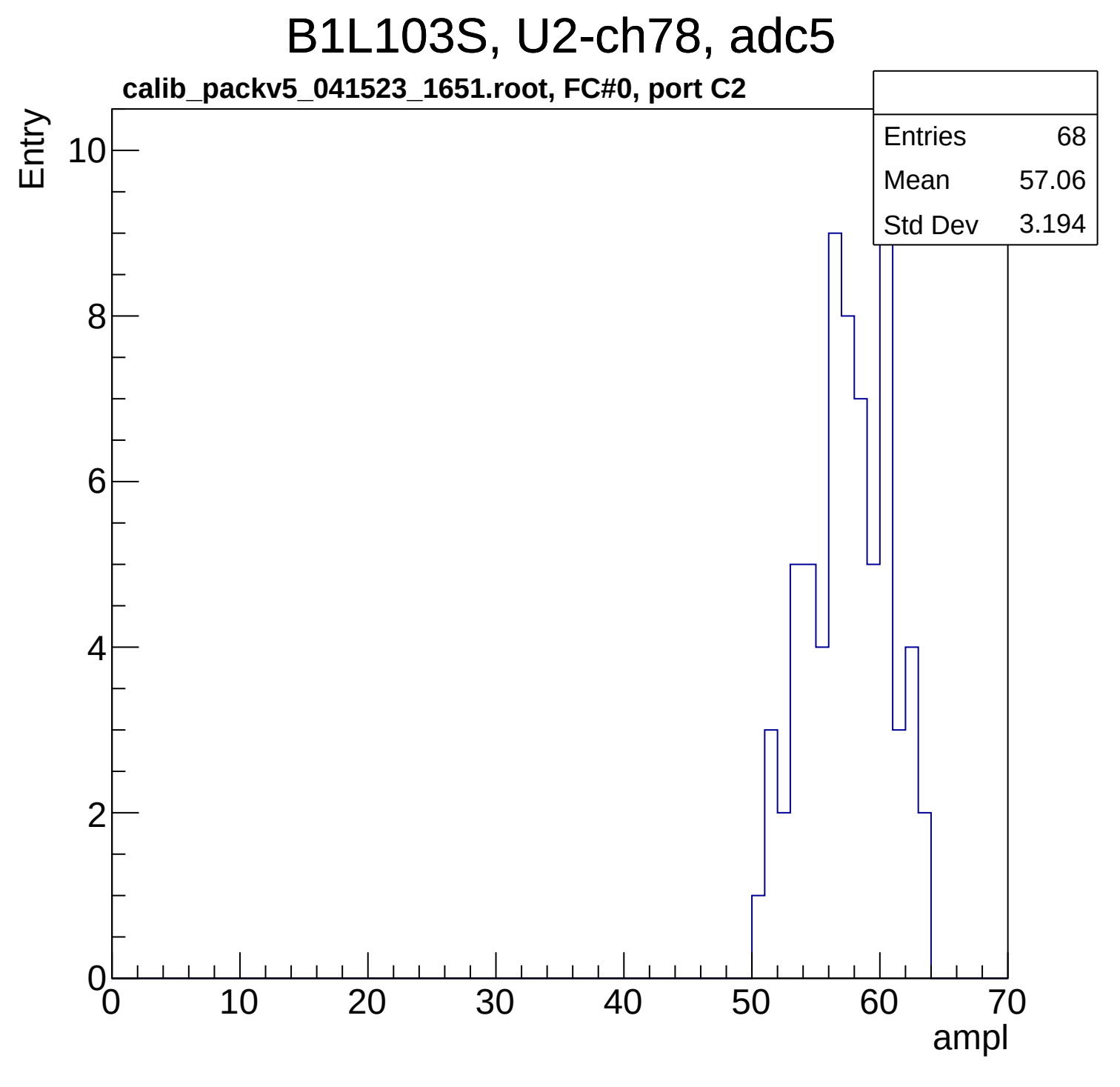

B1L103S, U2-ch78, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 17
Std Dev 12.52
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl

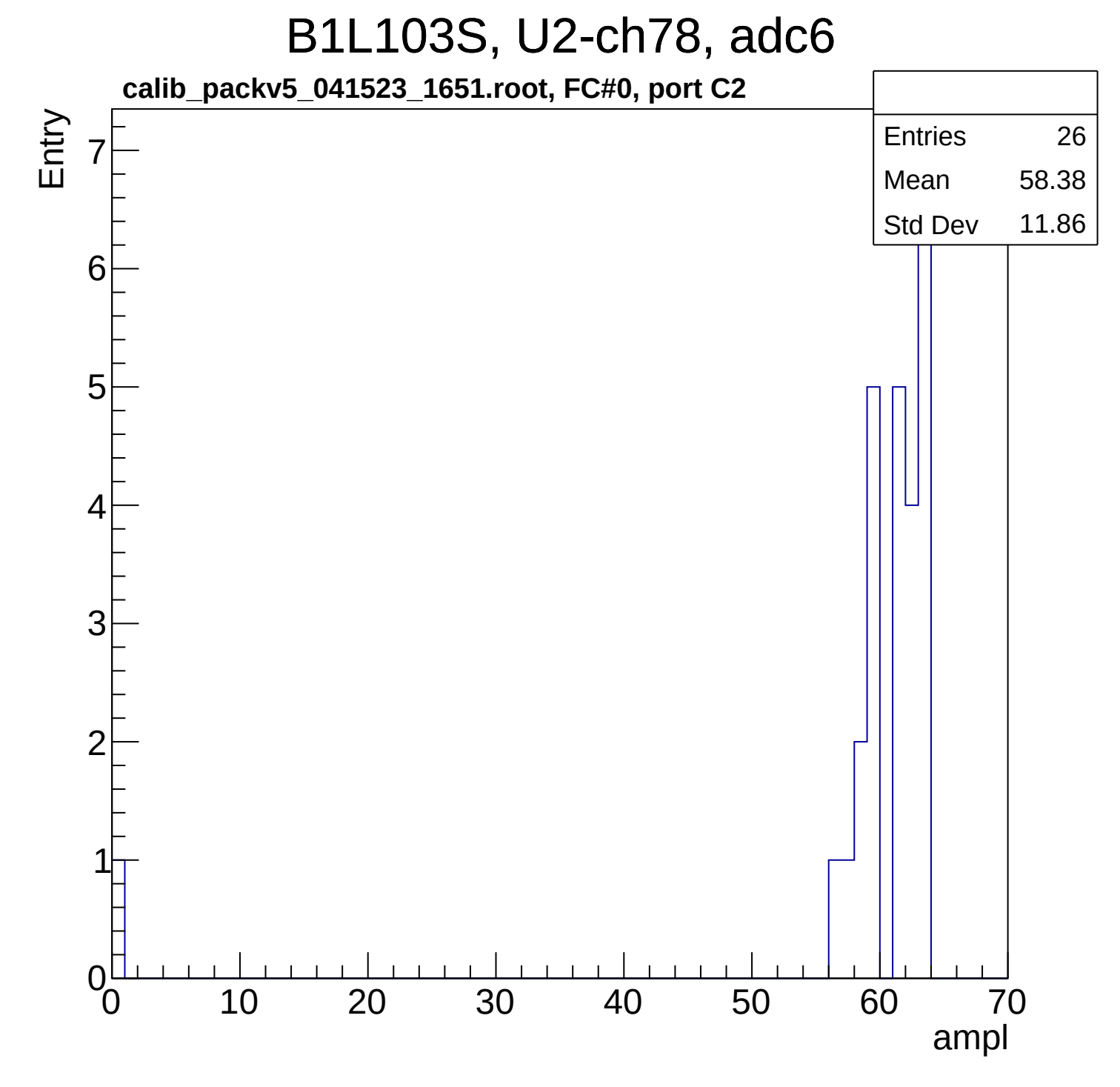

B1L103S, U2-ch78, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 28.72
Std Dev 11.93
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

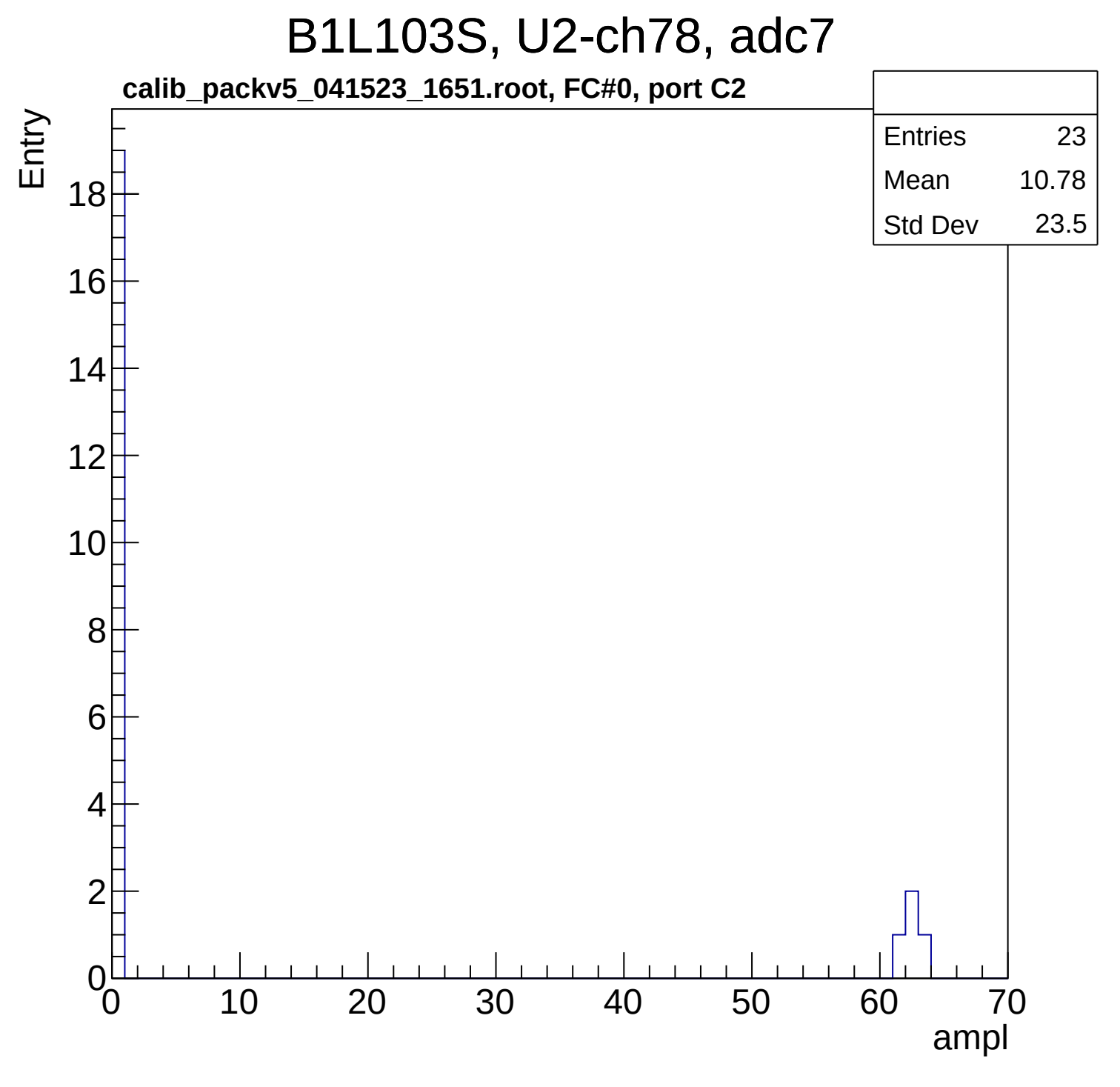

B1L103S, U2-ch78, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 36.97
Std Dev 11.27
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

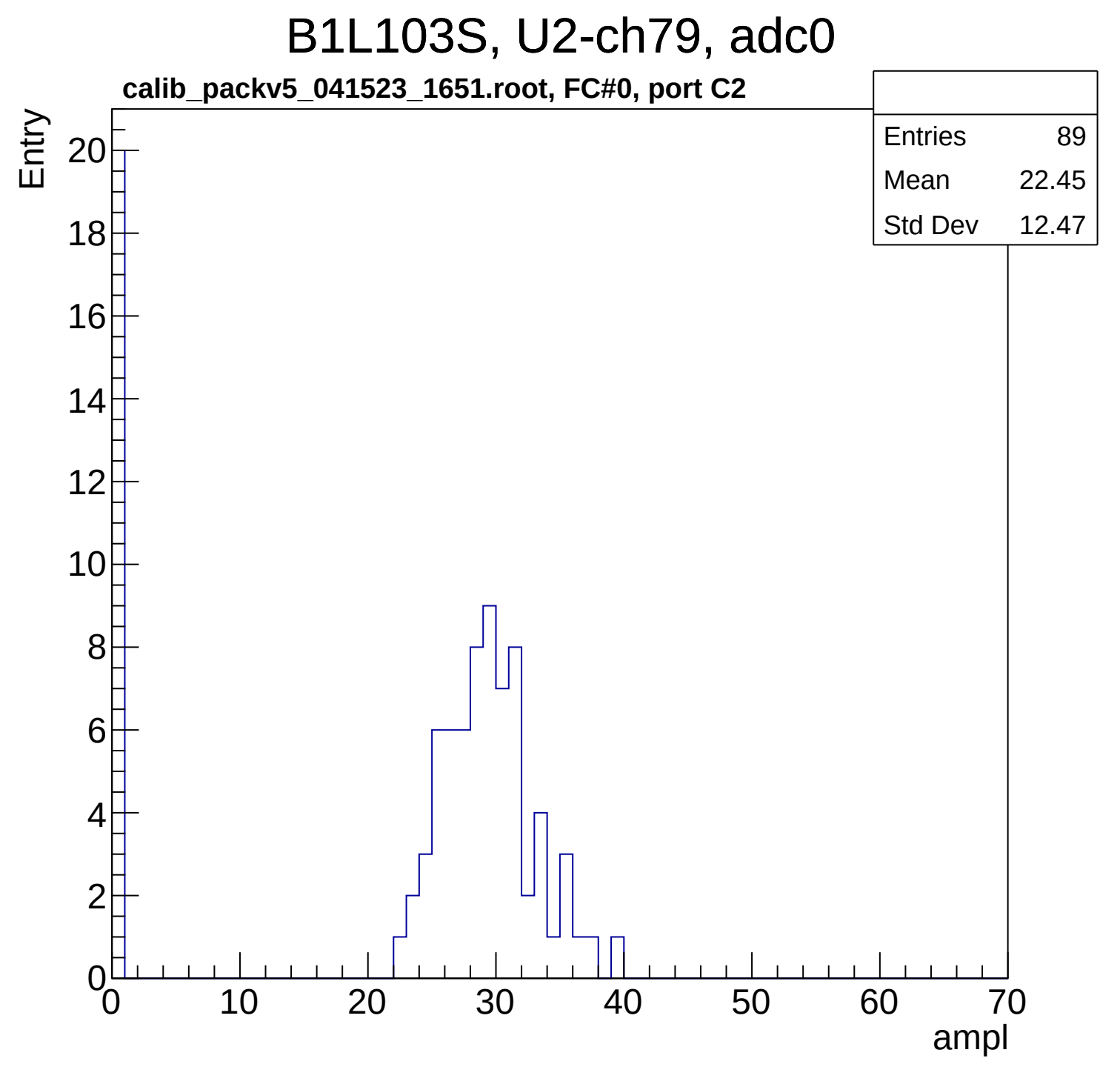

B1L103S, U2-ch78, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 45.2
Std Dev 3.556
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

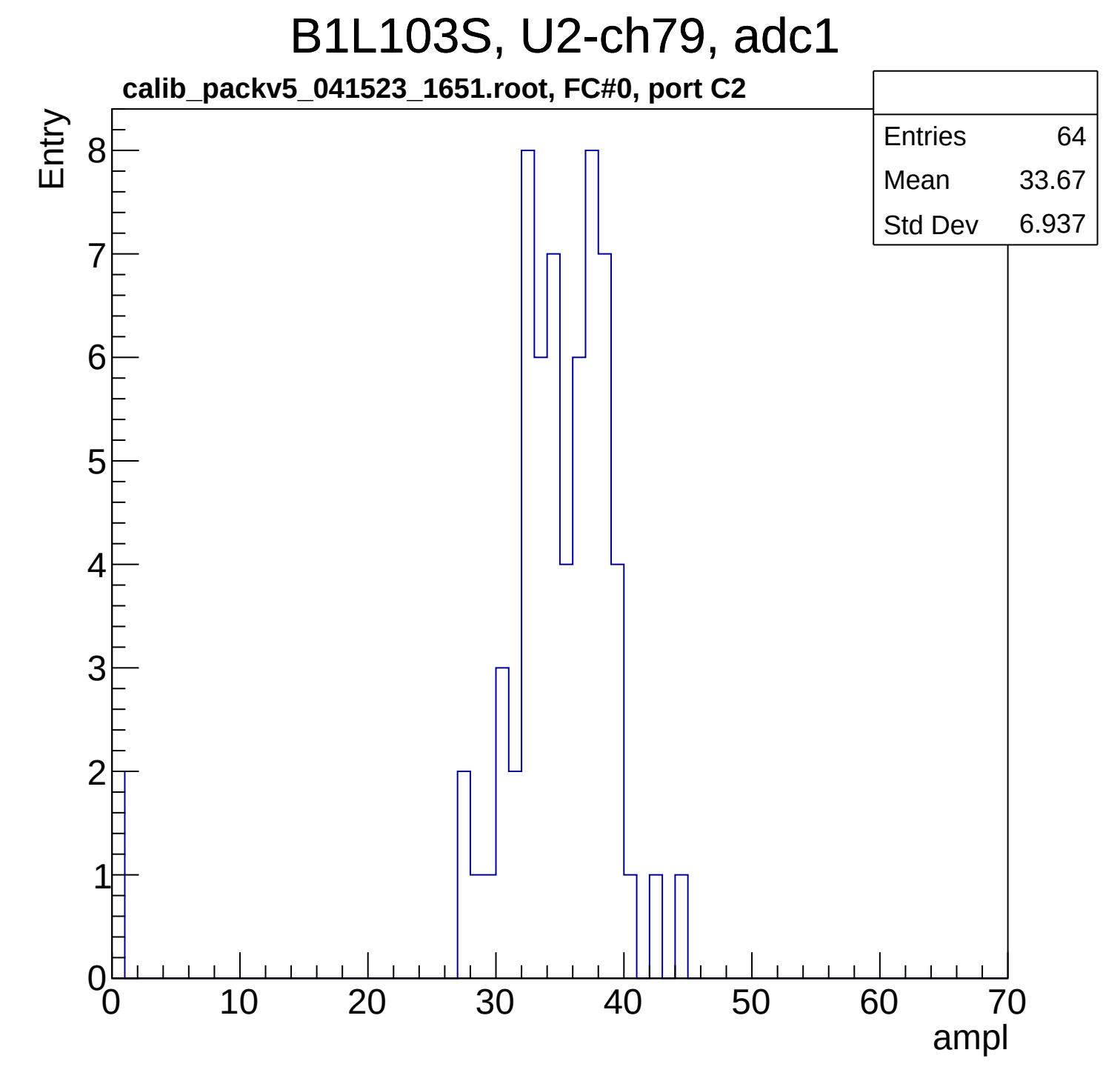

B1L103S, U2-ch78, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 51.16
Std Dev 3.138
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

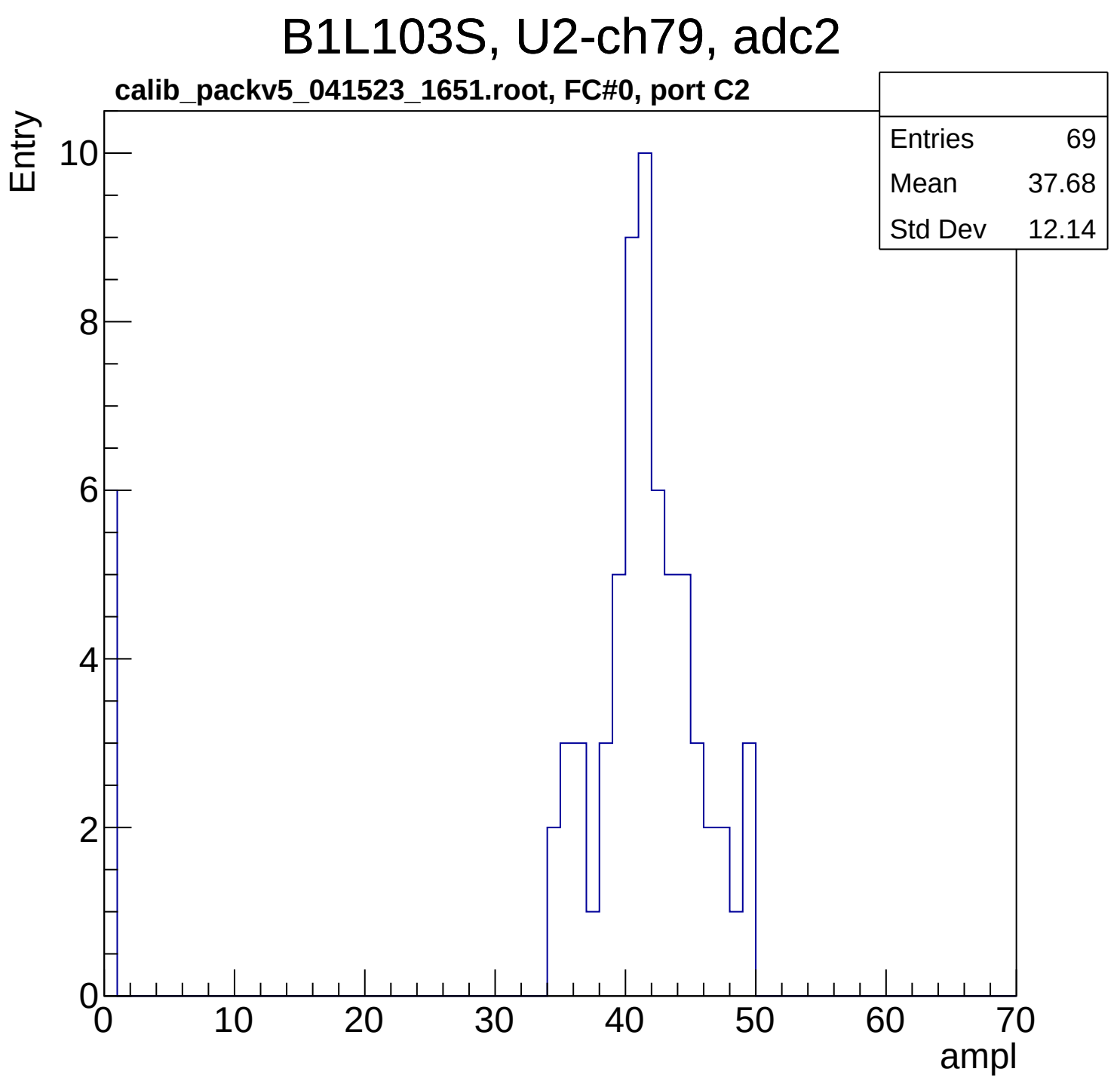

B1L103S, U2-ch78, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 57.06
Std Dev 3.194
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

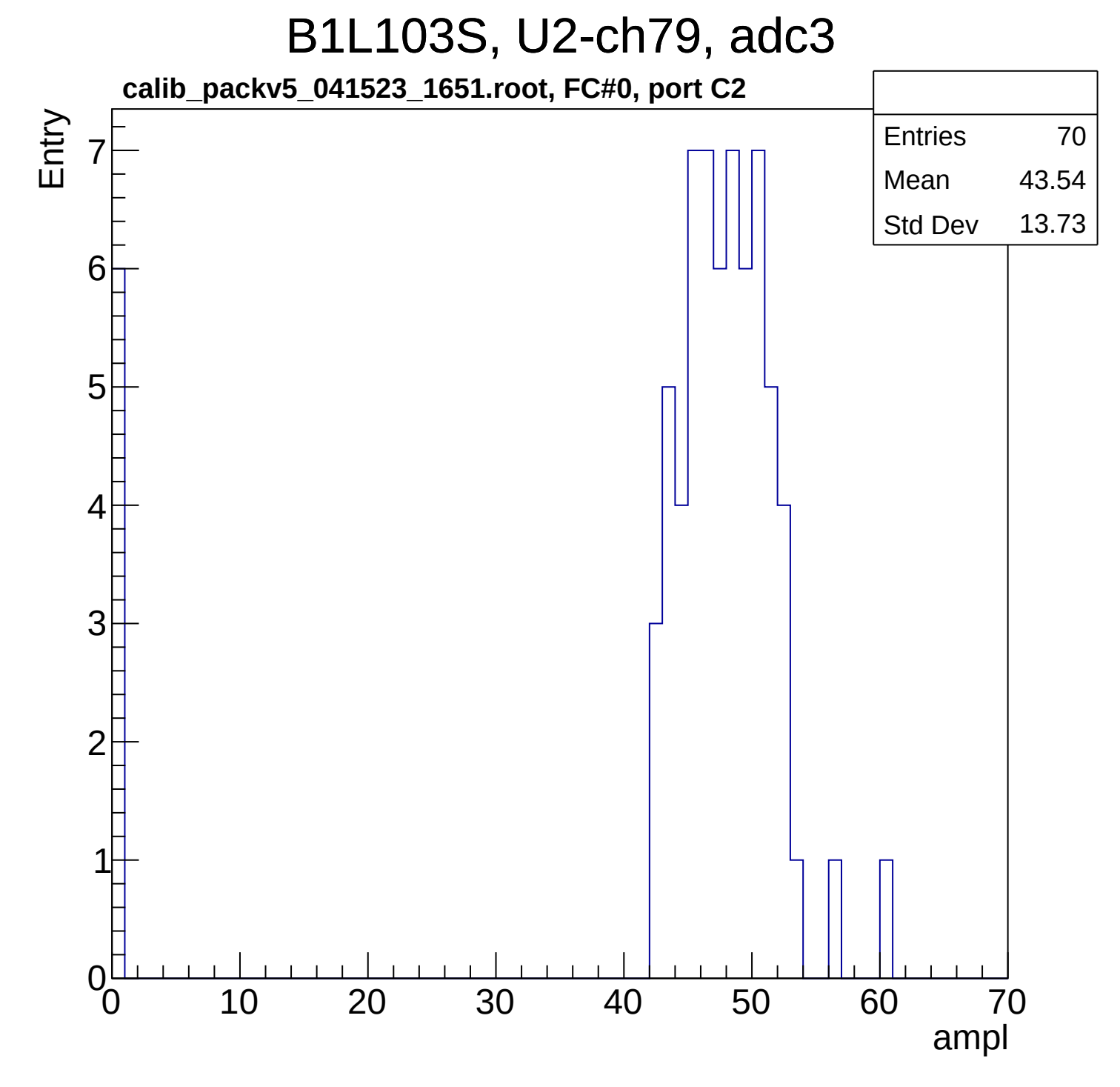

B1L103S, U2-ch78, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 58.38
Std Dev 11.86
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

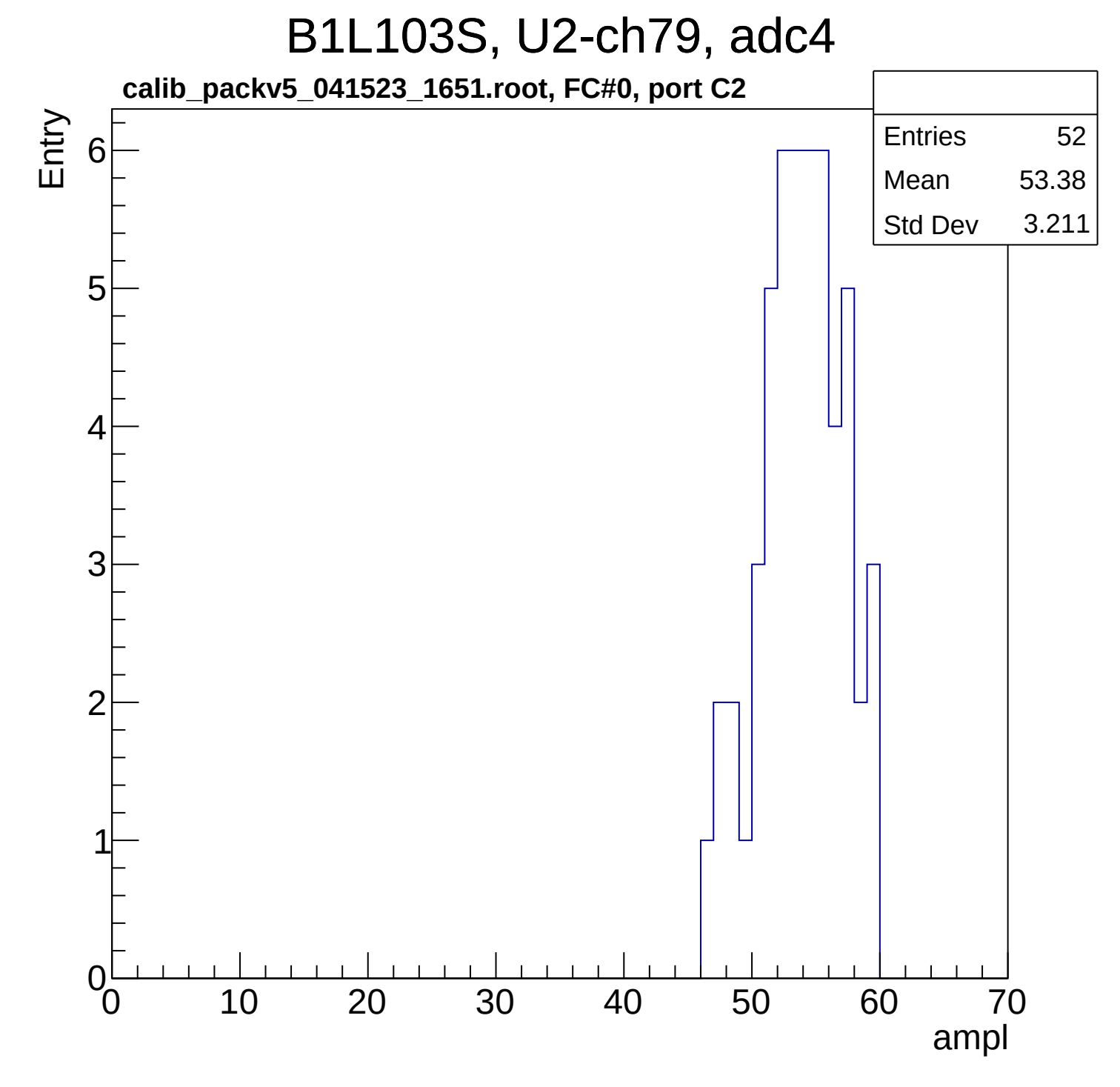

B1L103S, U2-ch78, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.78
Std Dev 23.5
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

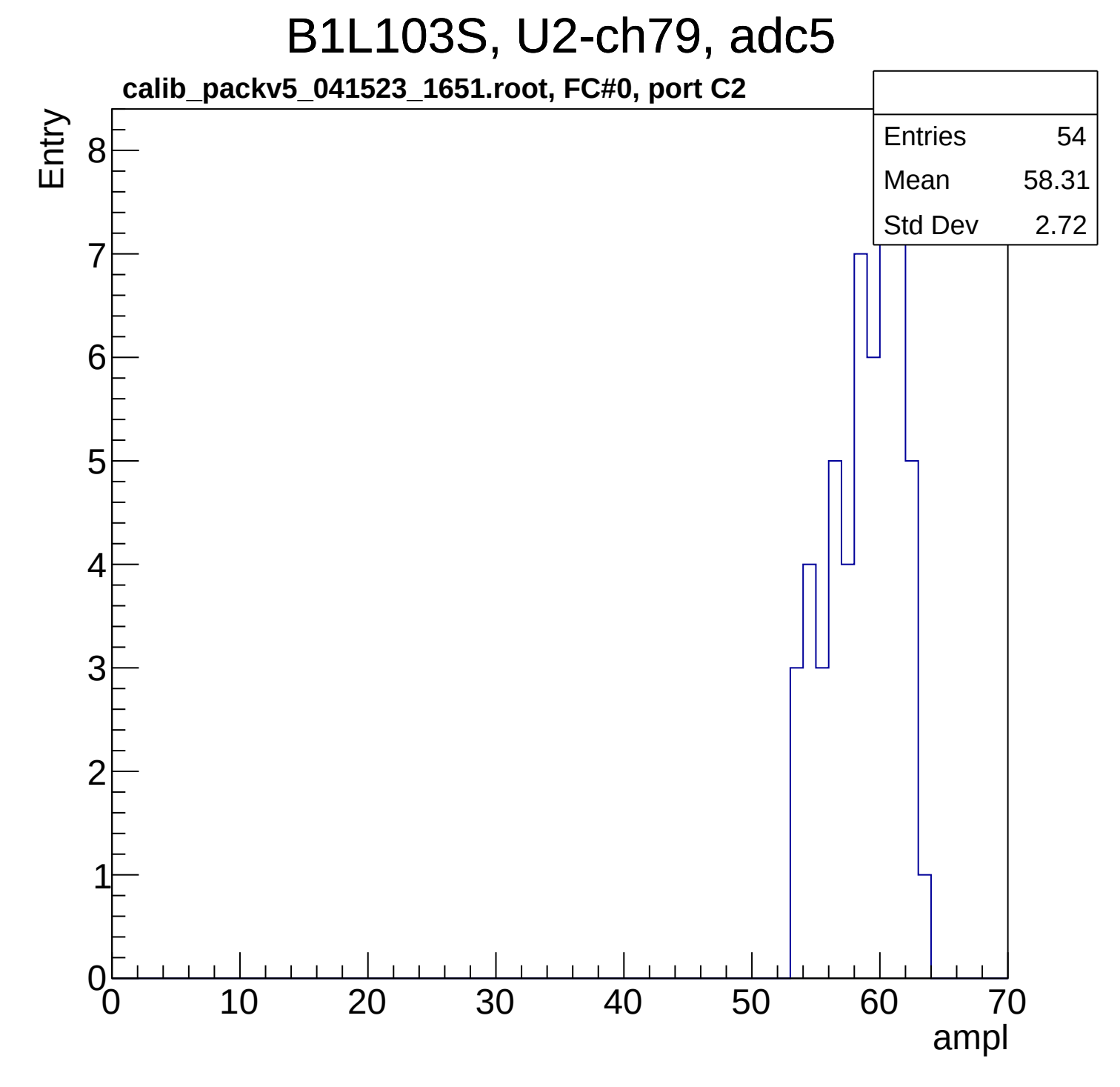

B1L103S, U2-ch79, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 22.45
Std Dev 12.47
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70

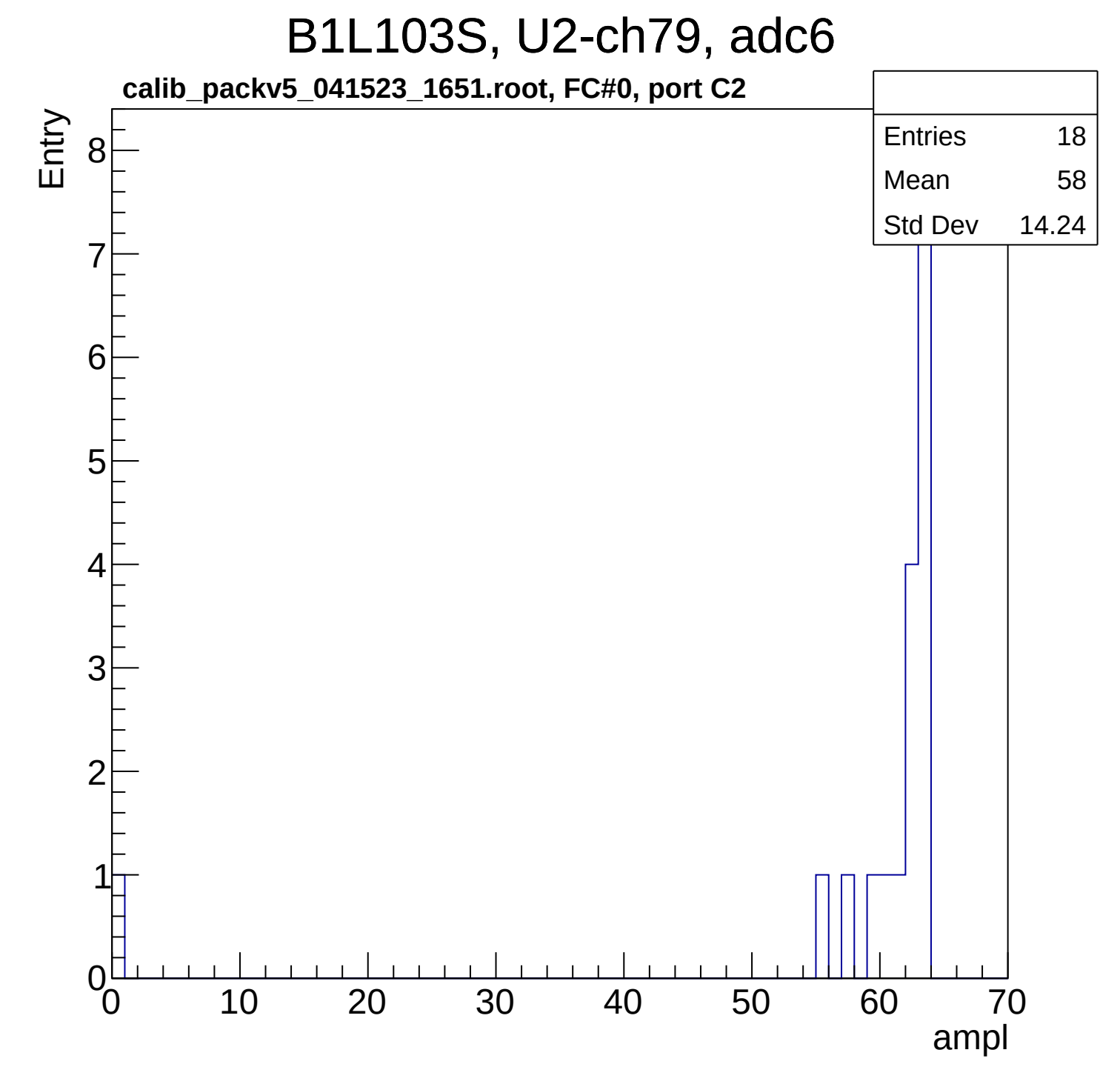

B1L103S, U2-ch79, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 33.67
Std Dev 6.937
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

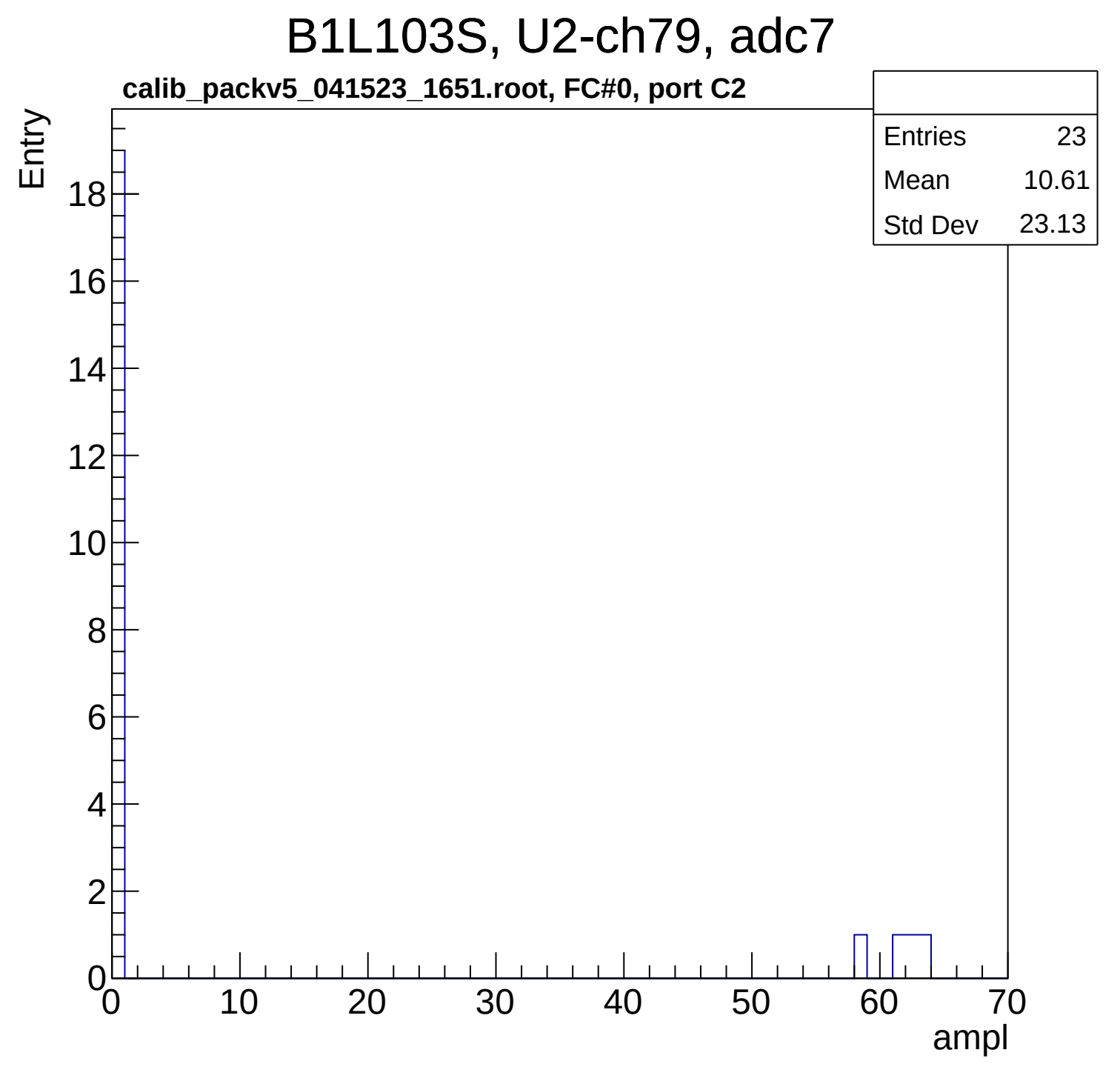

B1L103S, U2-ch79, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 37.68
Std Dev 12.14
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

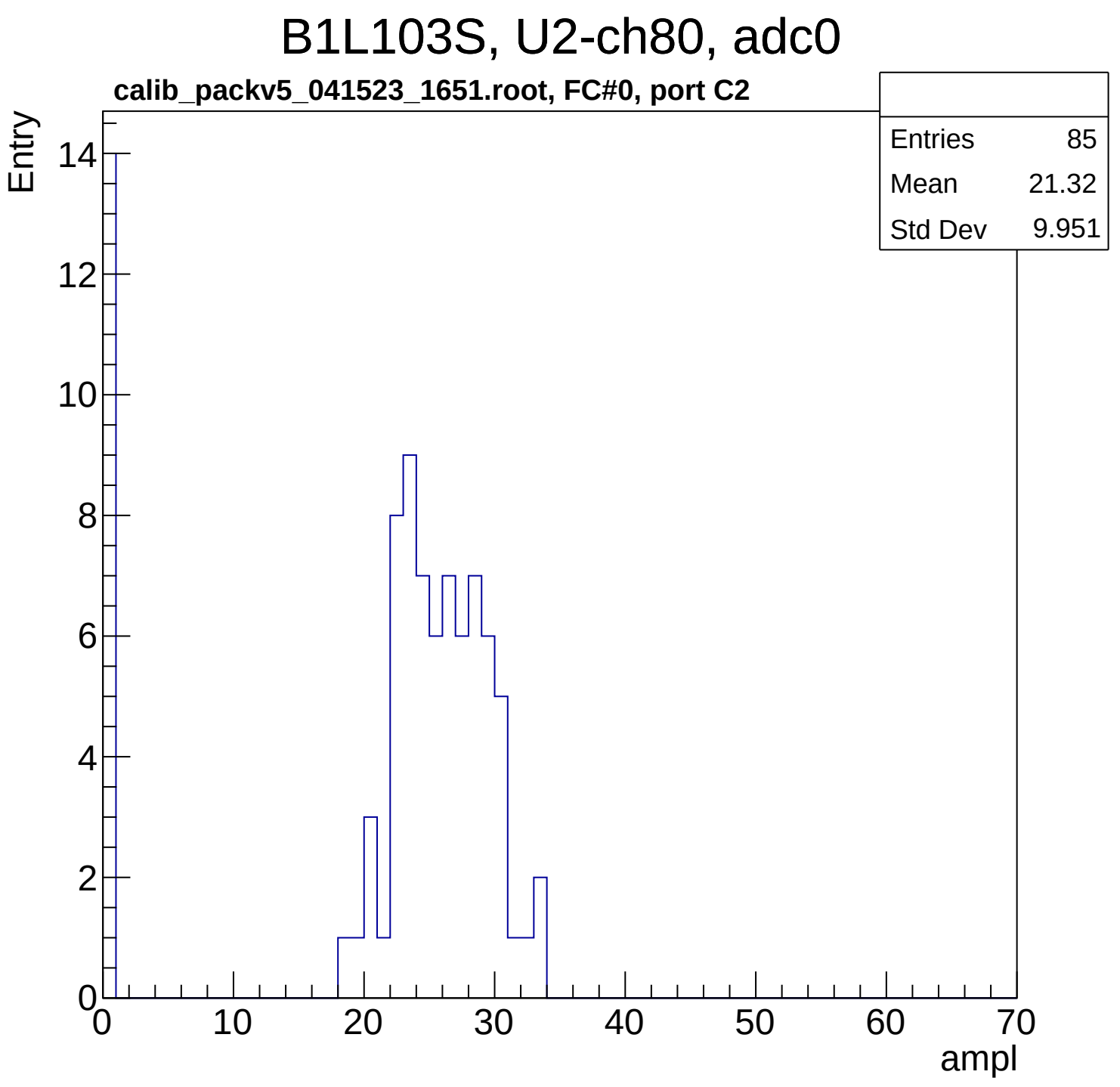

B1L103S, U2-ch79, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 43.54
Std Dev 13.73
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

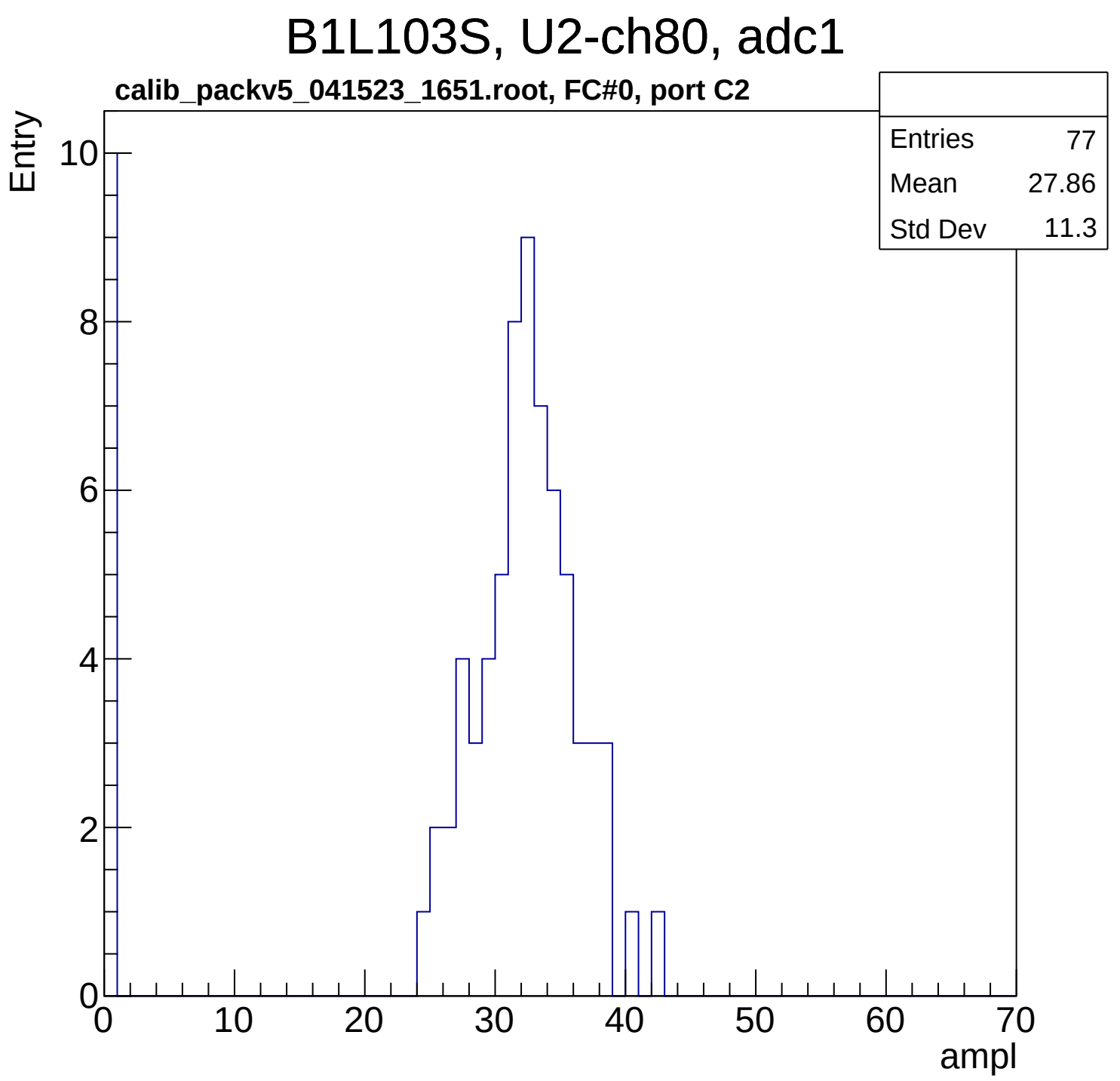

B1L103S, U2-ch79, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 53.38
Std Dev 3.211
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

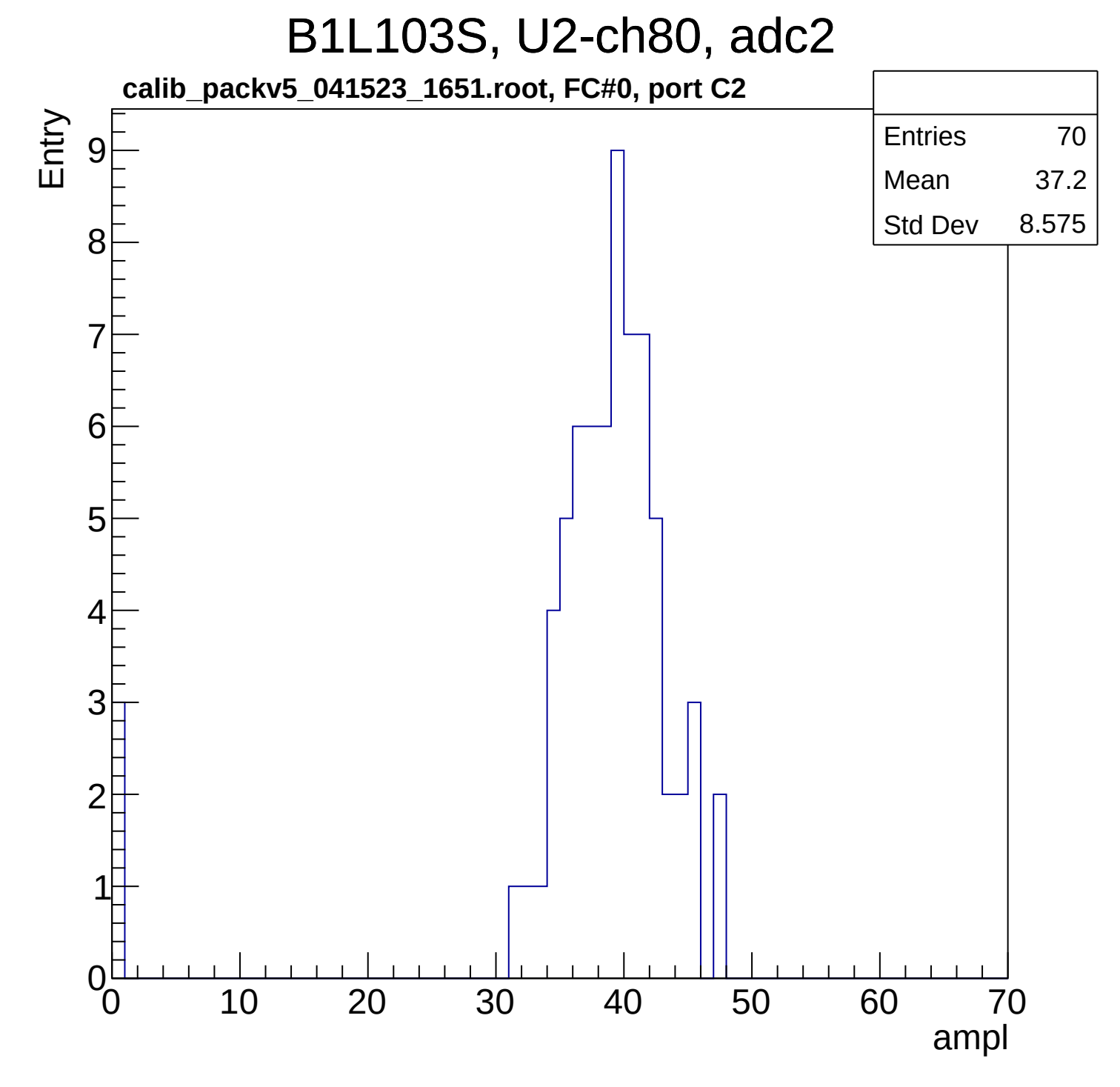

B1L103S, U2-ch79, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.31
Std Dev 2.72
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

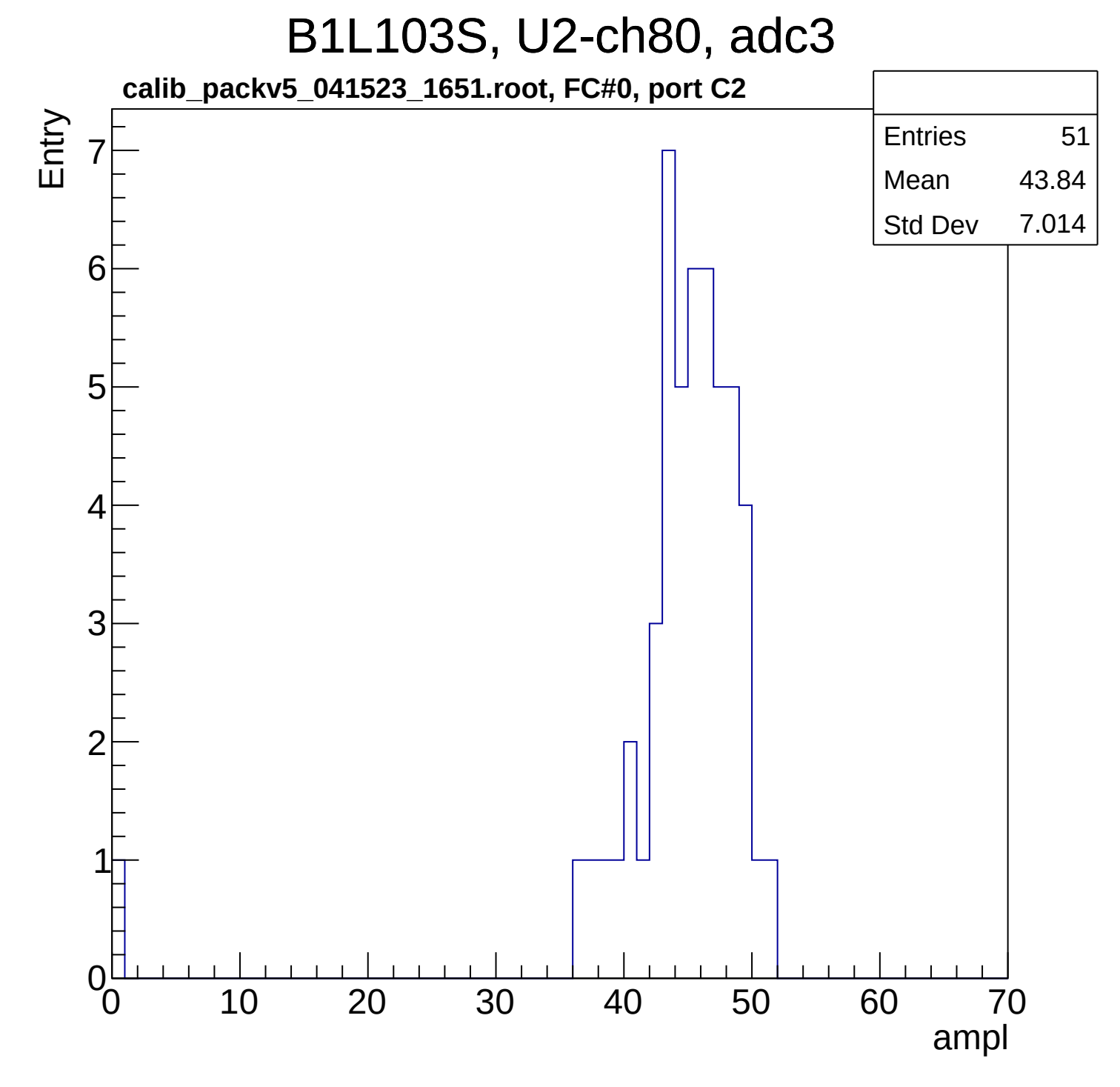

B1L103S, U2-ch79, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 58
Std Dev 14.24
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

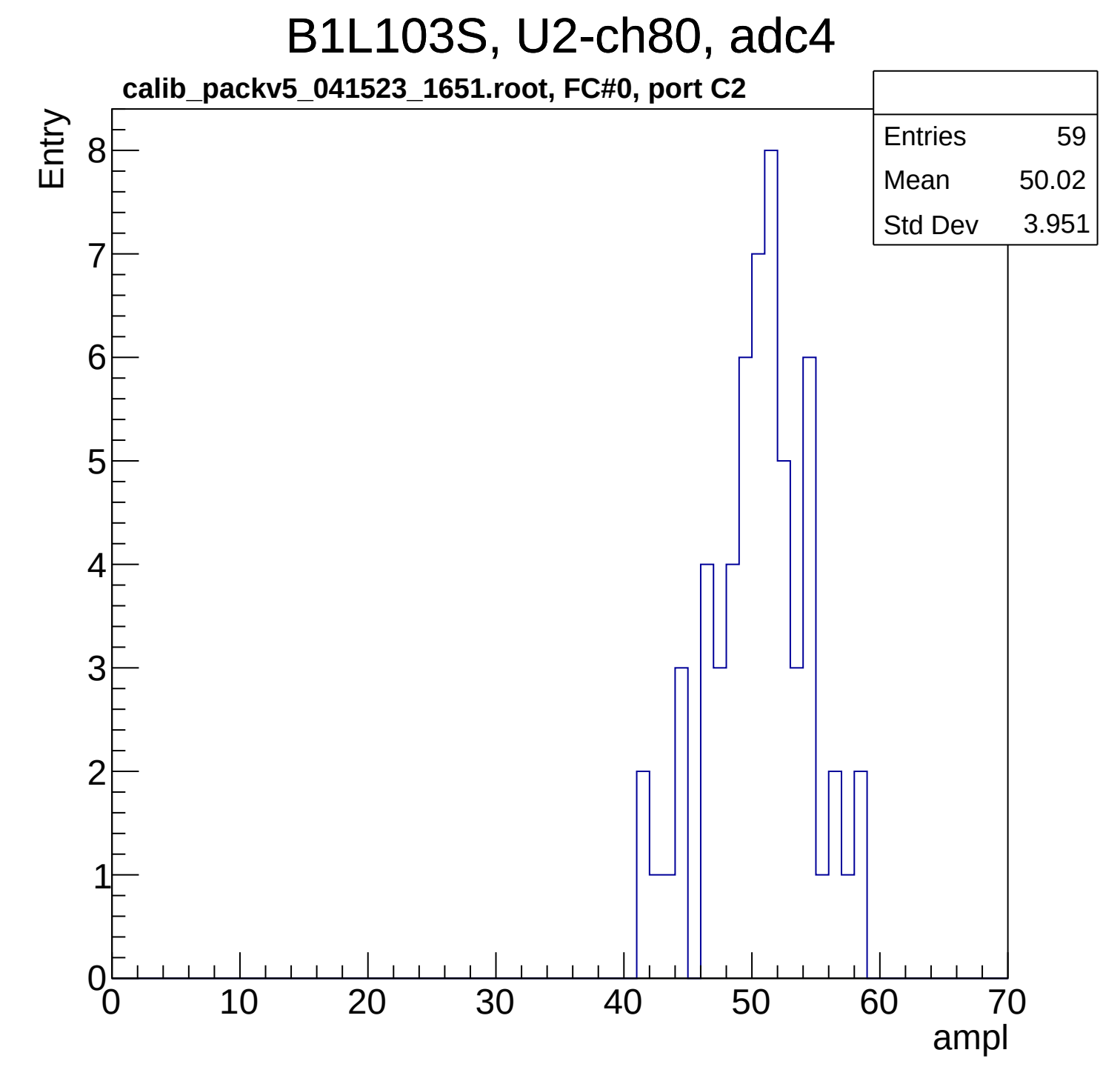

B1L103S, U2-ch79, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.61
Std Dev 23.13
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

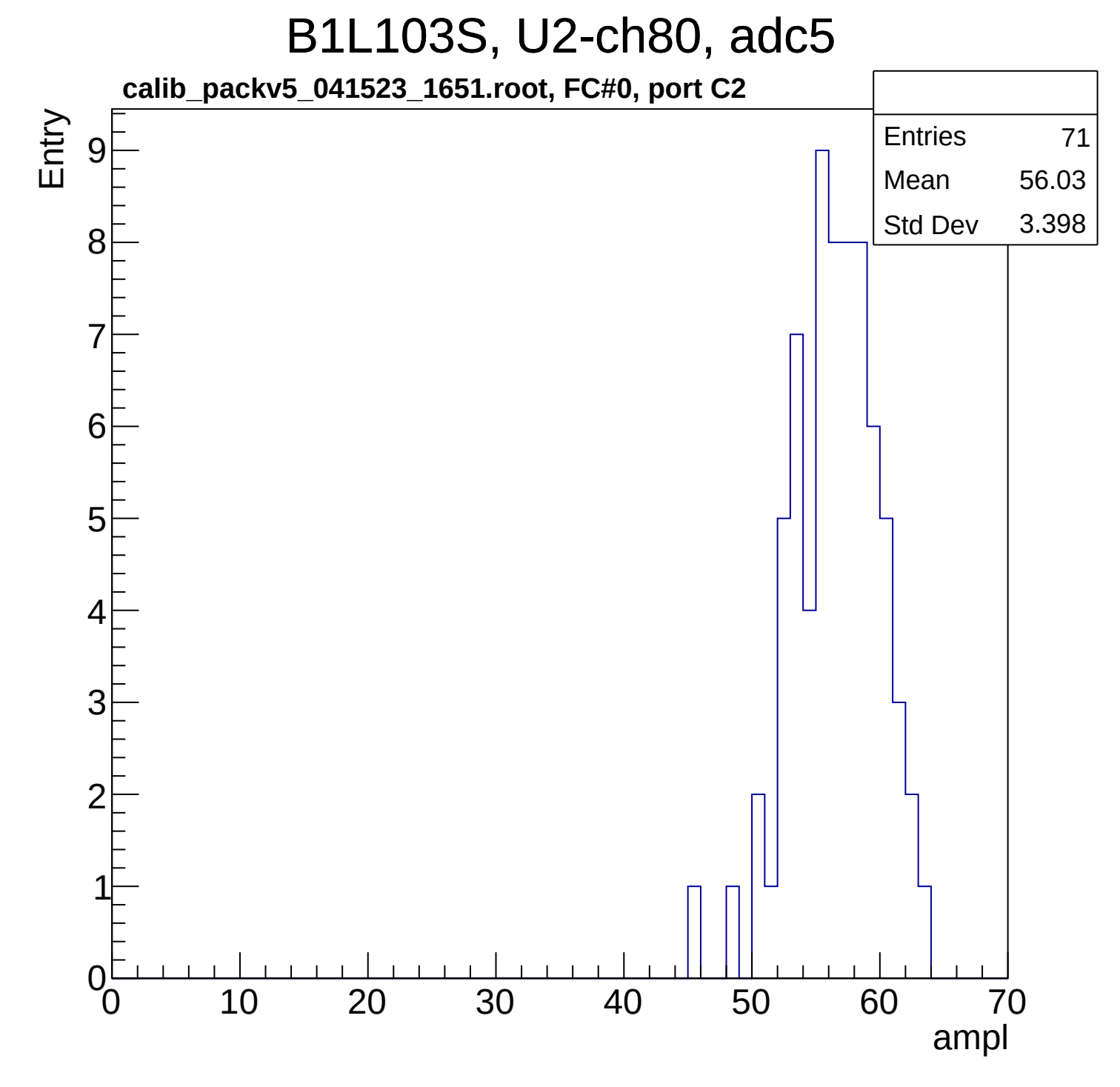

B1L103S, U2-ch80, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 21.32
Std Dev 9.951
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

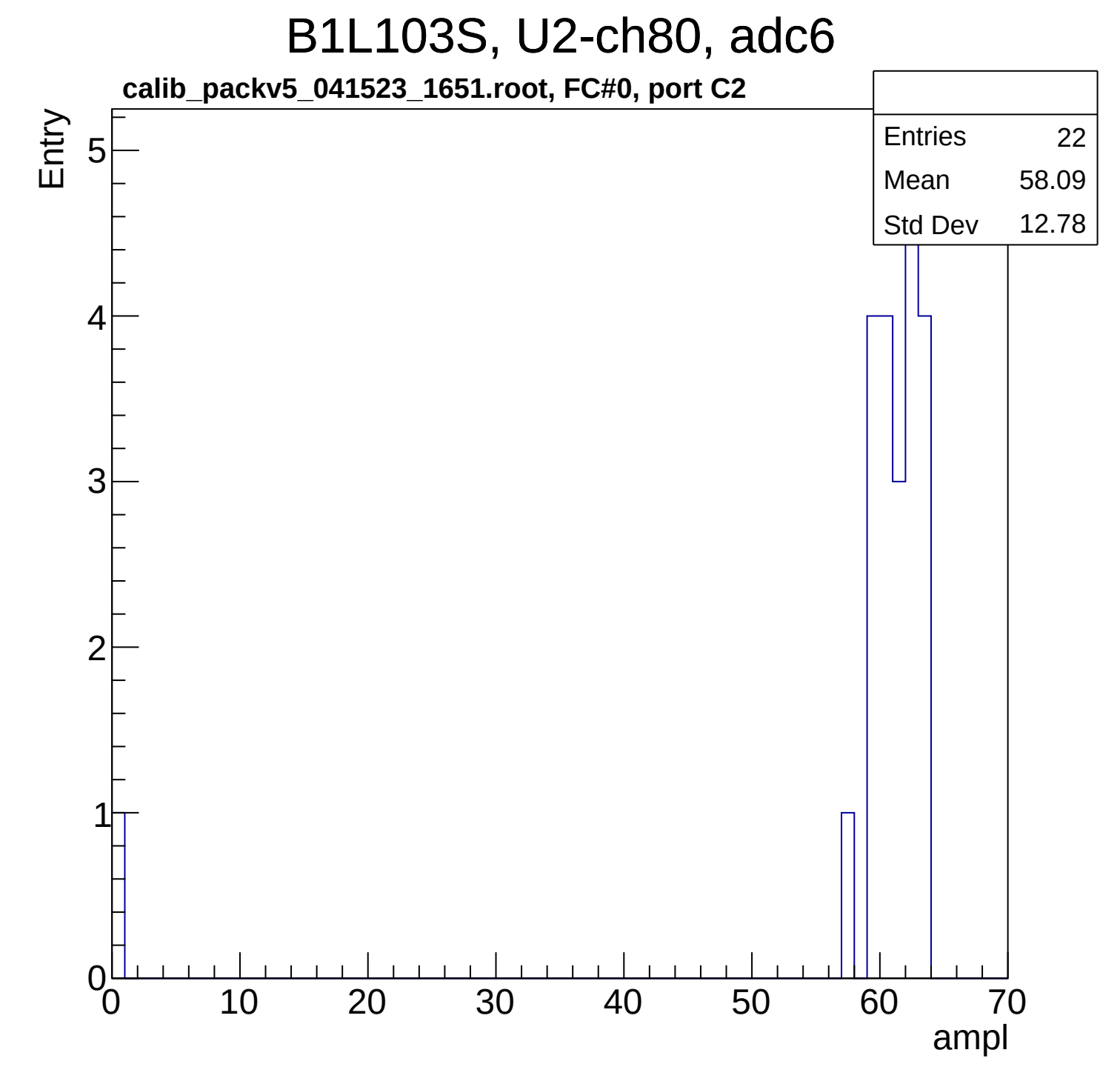

B1L103S, U2-ch80, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 27.86
Std Dev 11.3
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

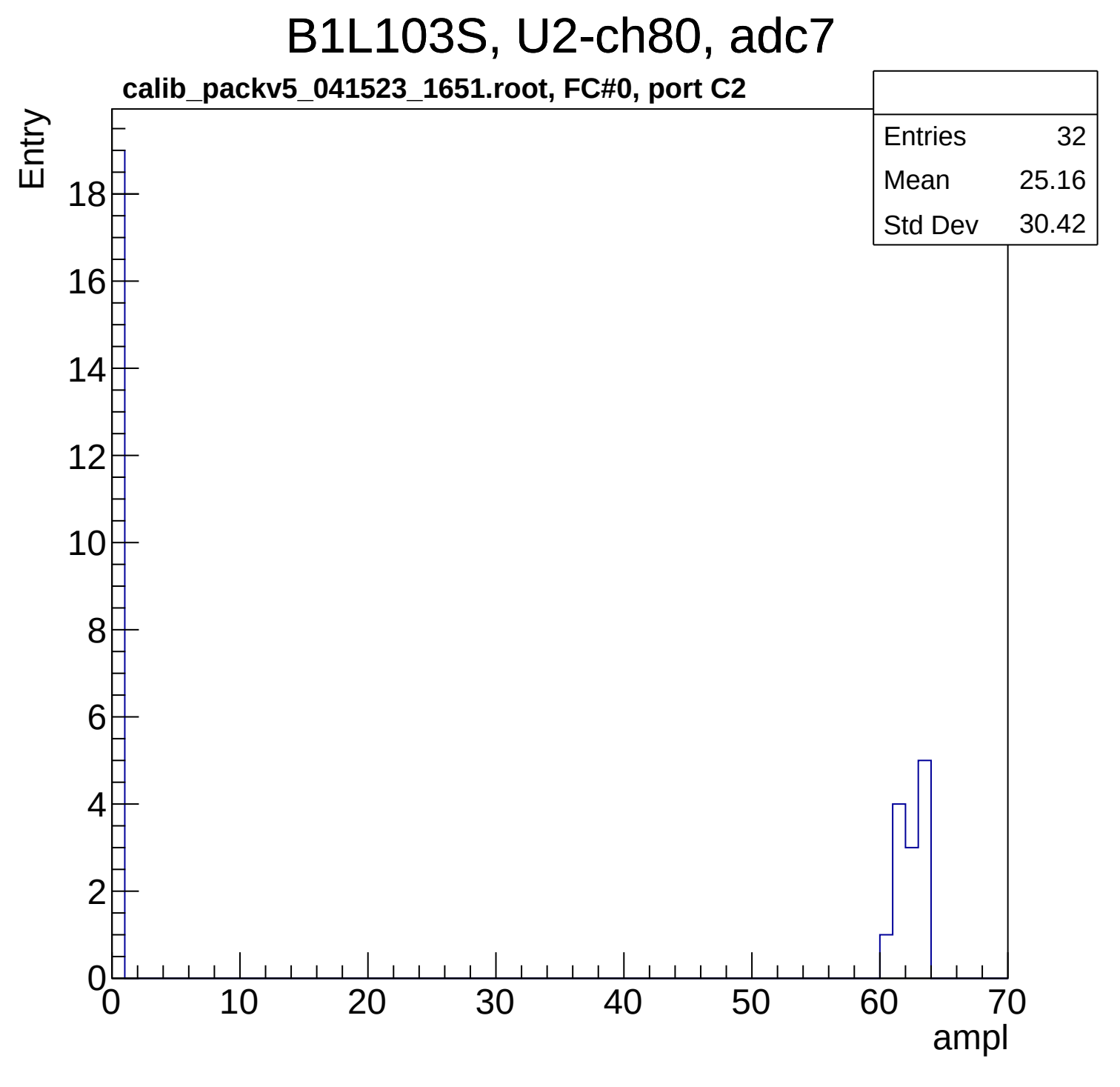

B1L103S, U2-ch80, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 37.2
Std Dev 8.575
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

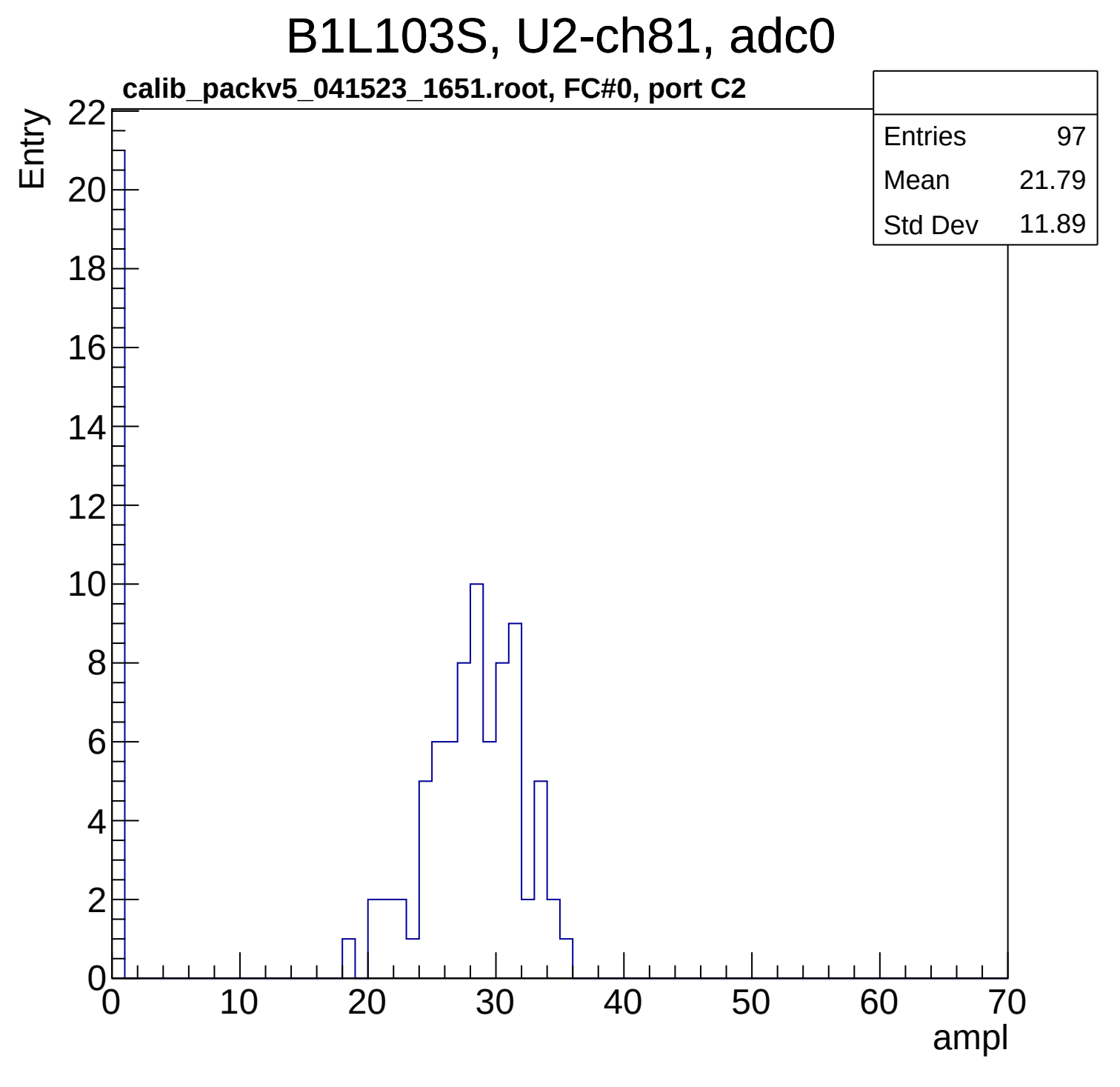

B1L103S, U2-ch80, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 43.84
Std Dev 7.014
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

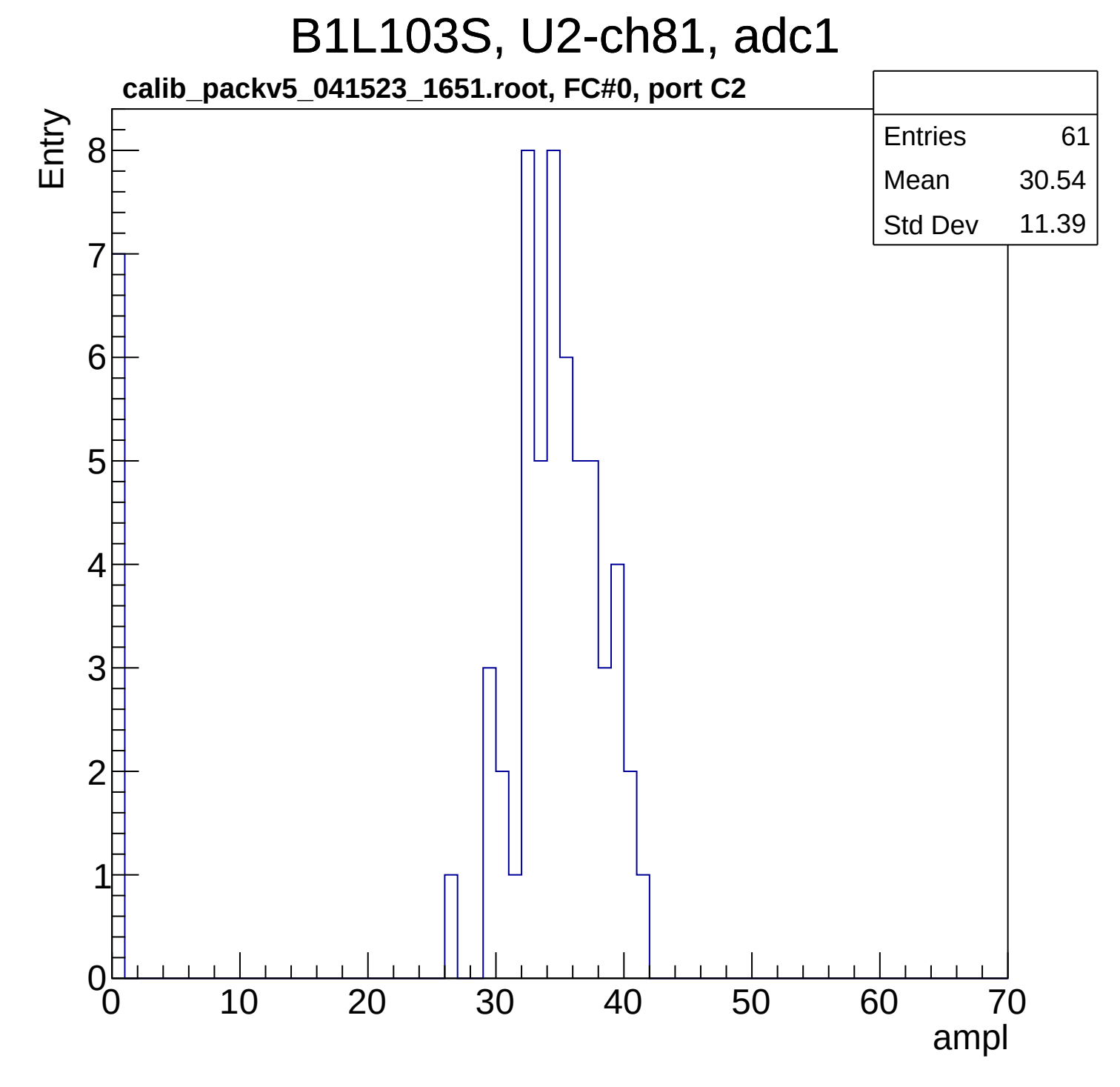

B1L103S, U2-ch80, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 50.02
Std Dev 3.951
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

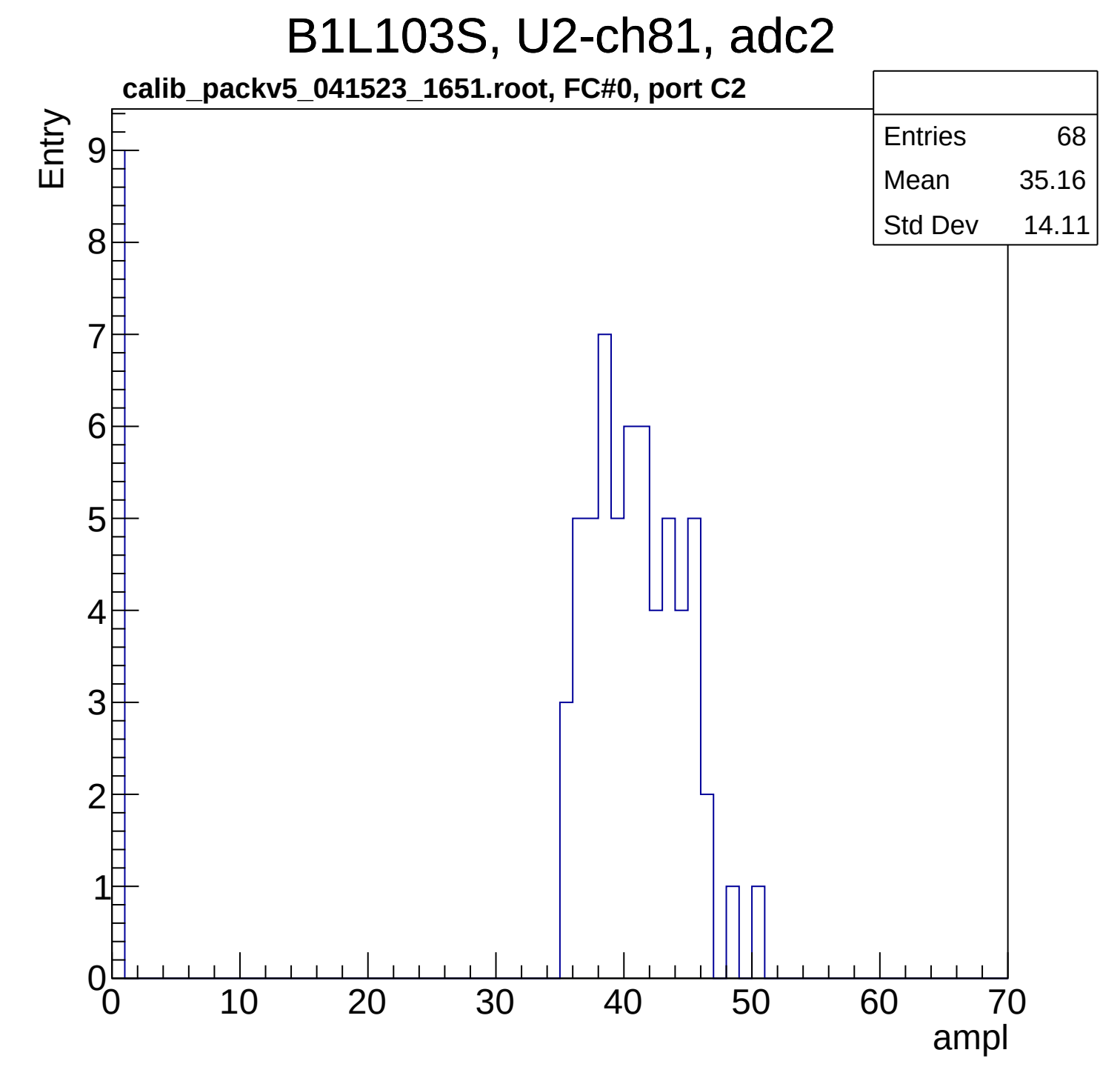

B1L103S, U2-ch80, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 56.03
Std Dev 3.398
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

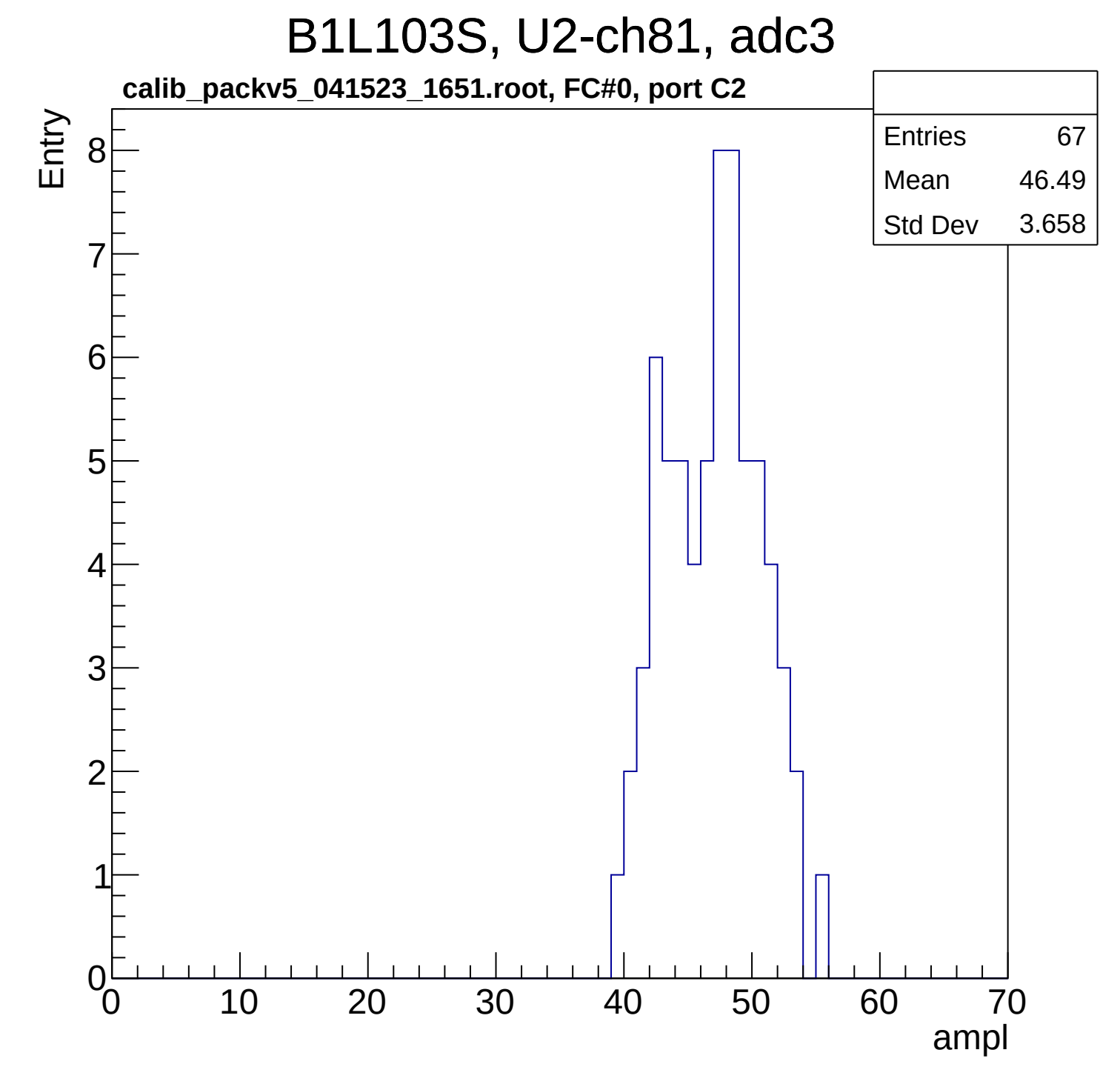

B1L103S, U2-ch80, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.09
Std Dev 12.78
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

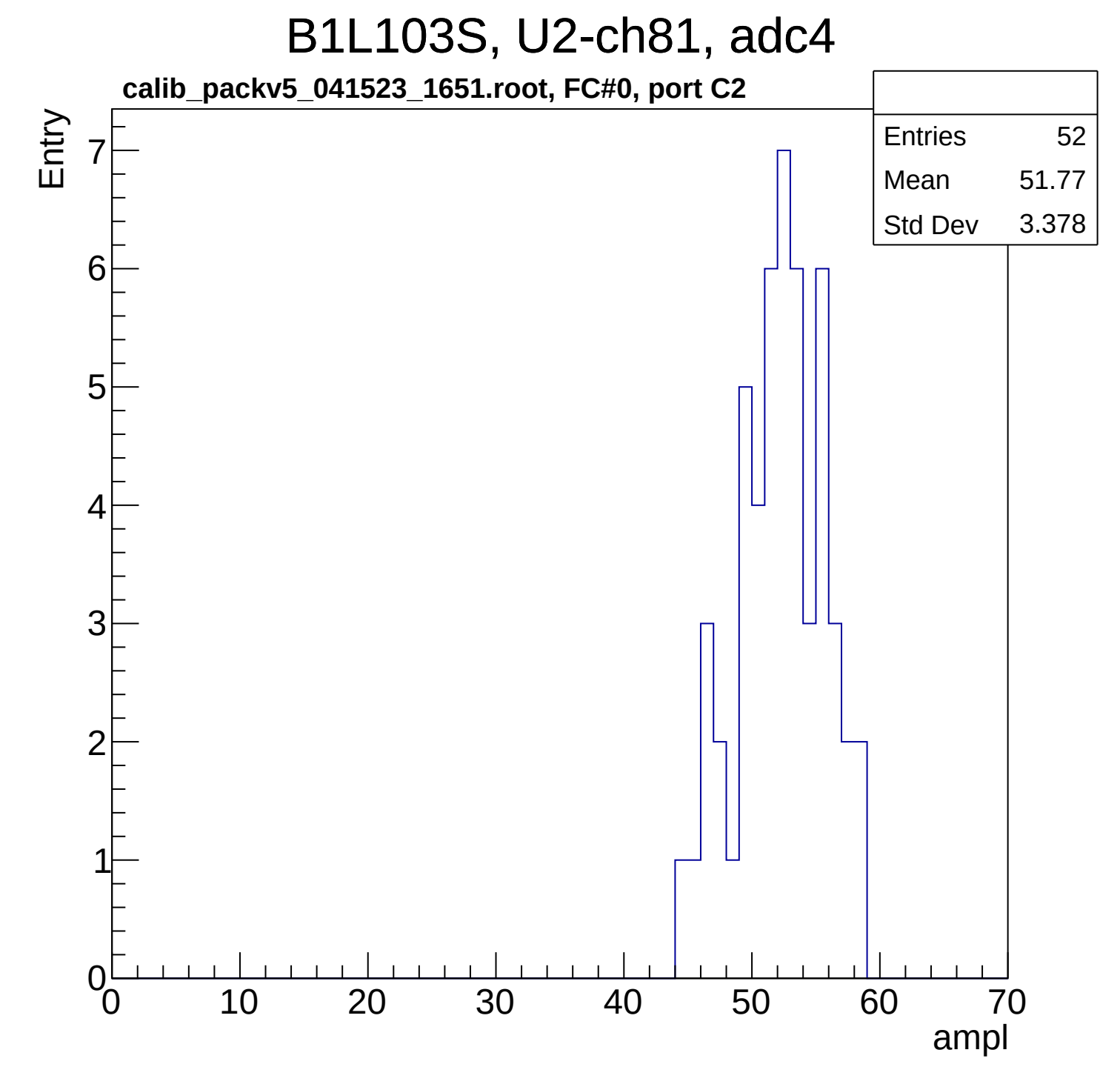

B1L103S, U2-ch80, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 25.16
Std Dev 30.42
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

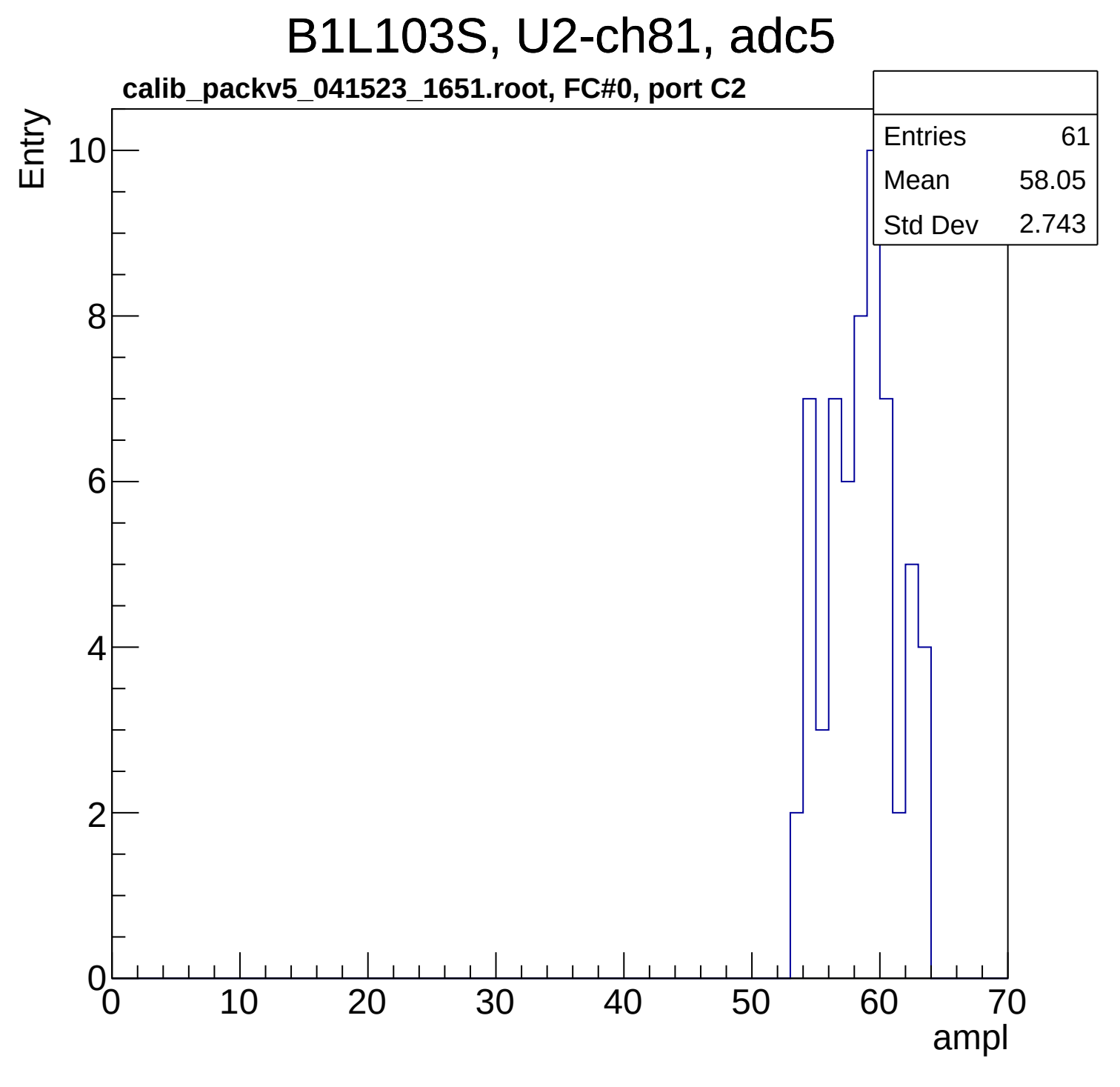

B1L103S, U2-ch81, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 21.79
Std Dev 11.89
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70

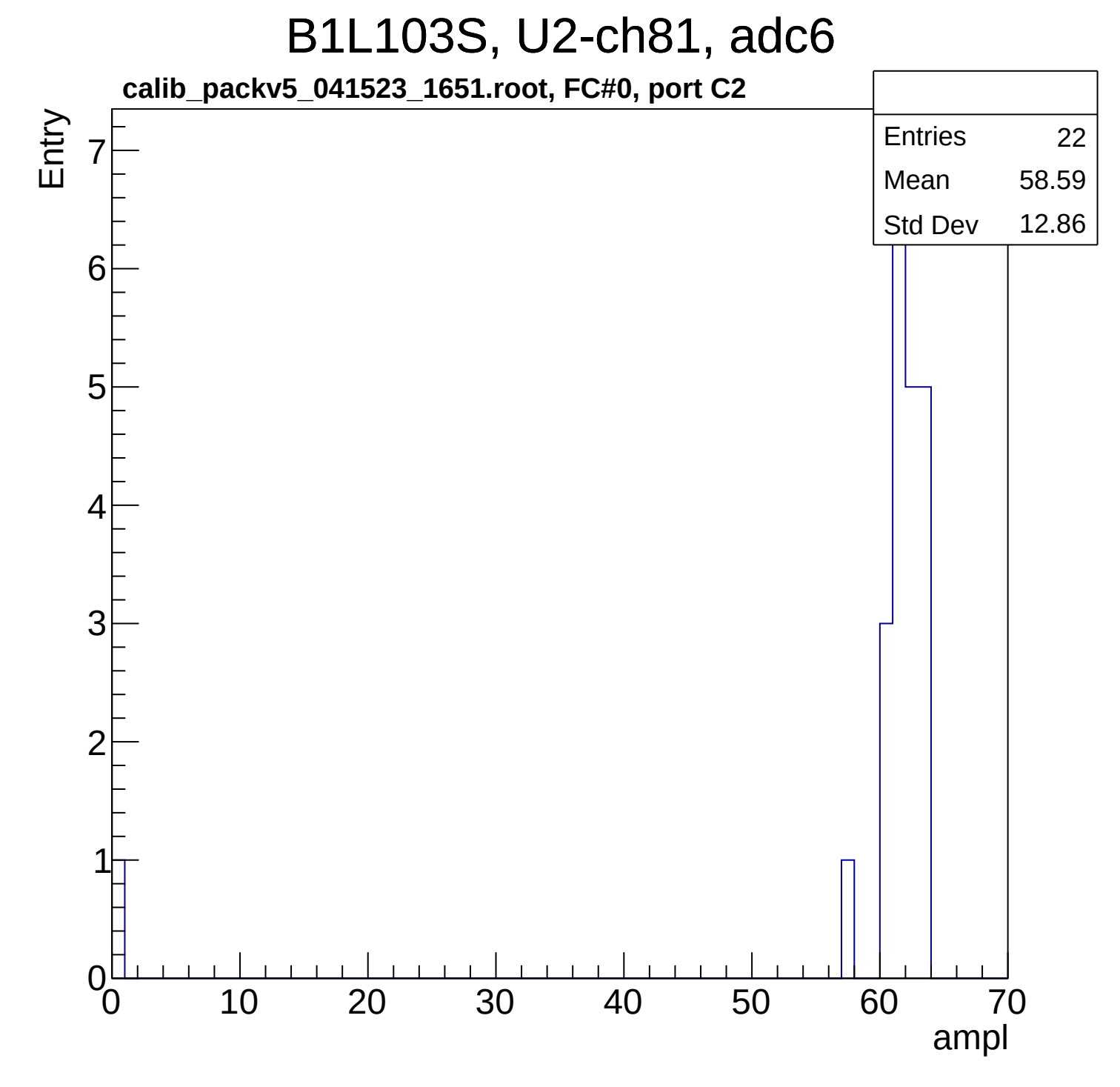

B1L103S, U2-ch81, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 30.54
Std Dev 11.39
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

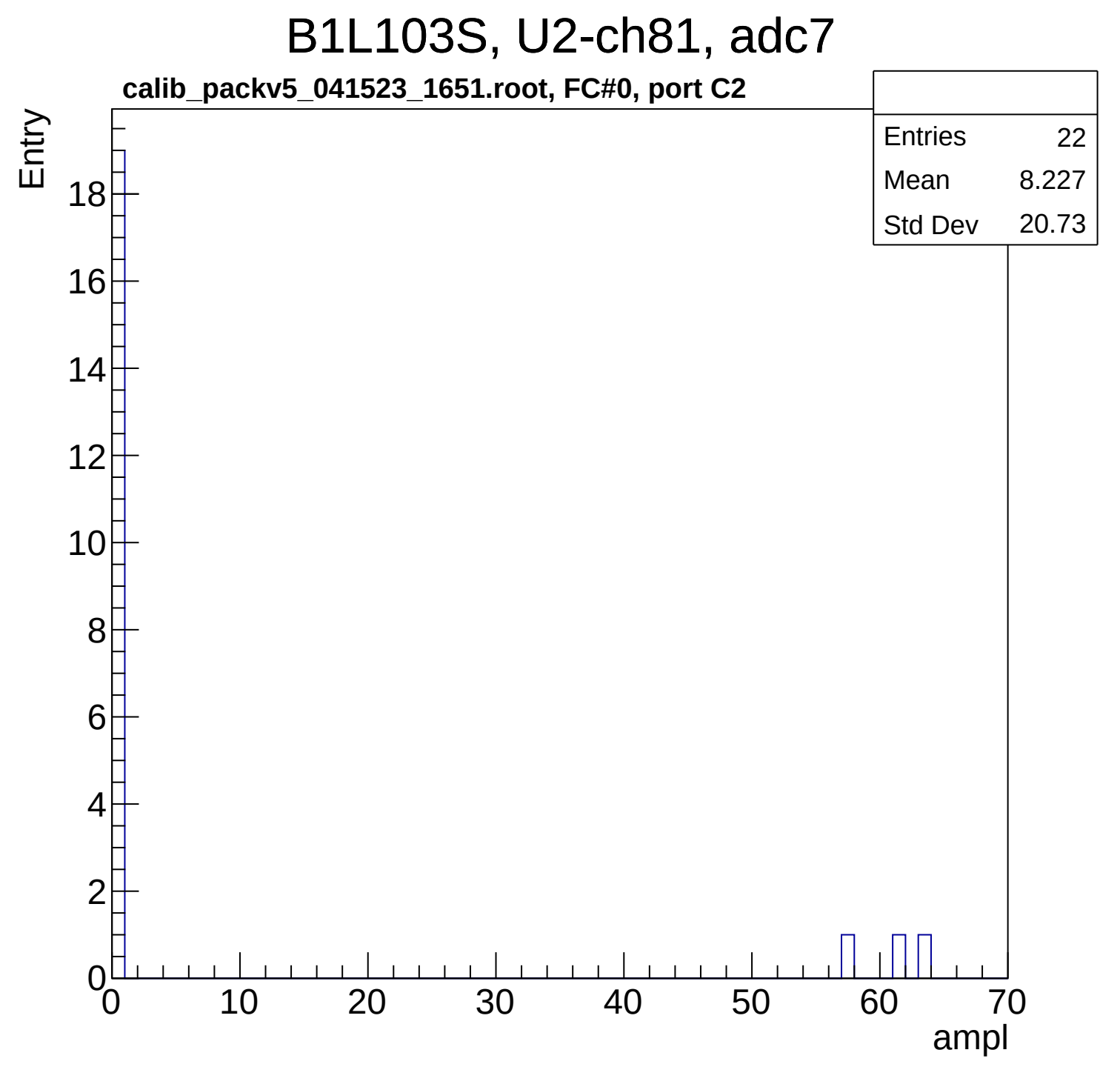

B1L103S, U2-ch81, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 35.16
Std Dev 14.11
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

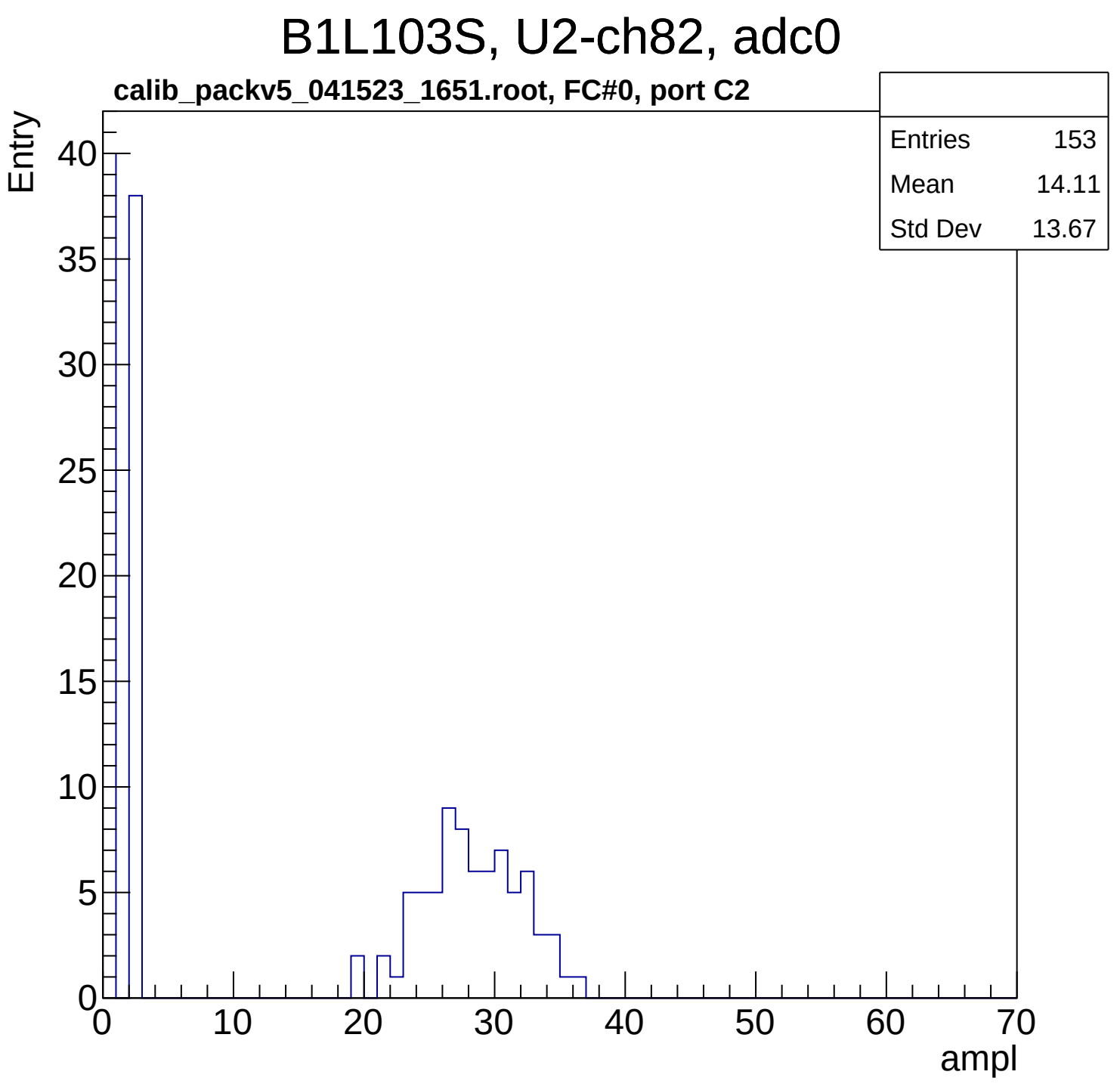

B1L103S, U2-ch81, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 46.49
Std Dev 3.658
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

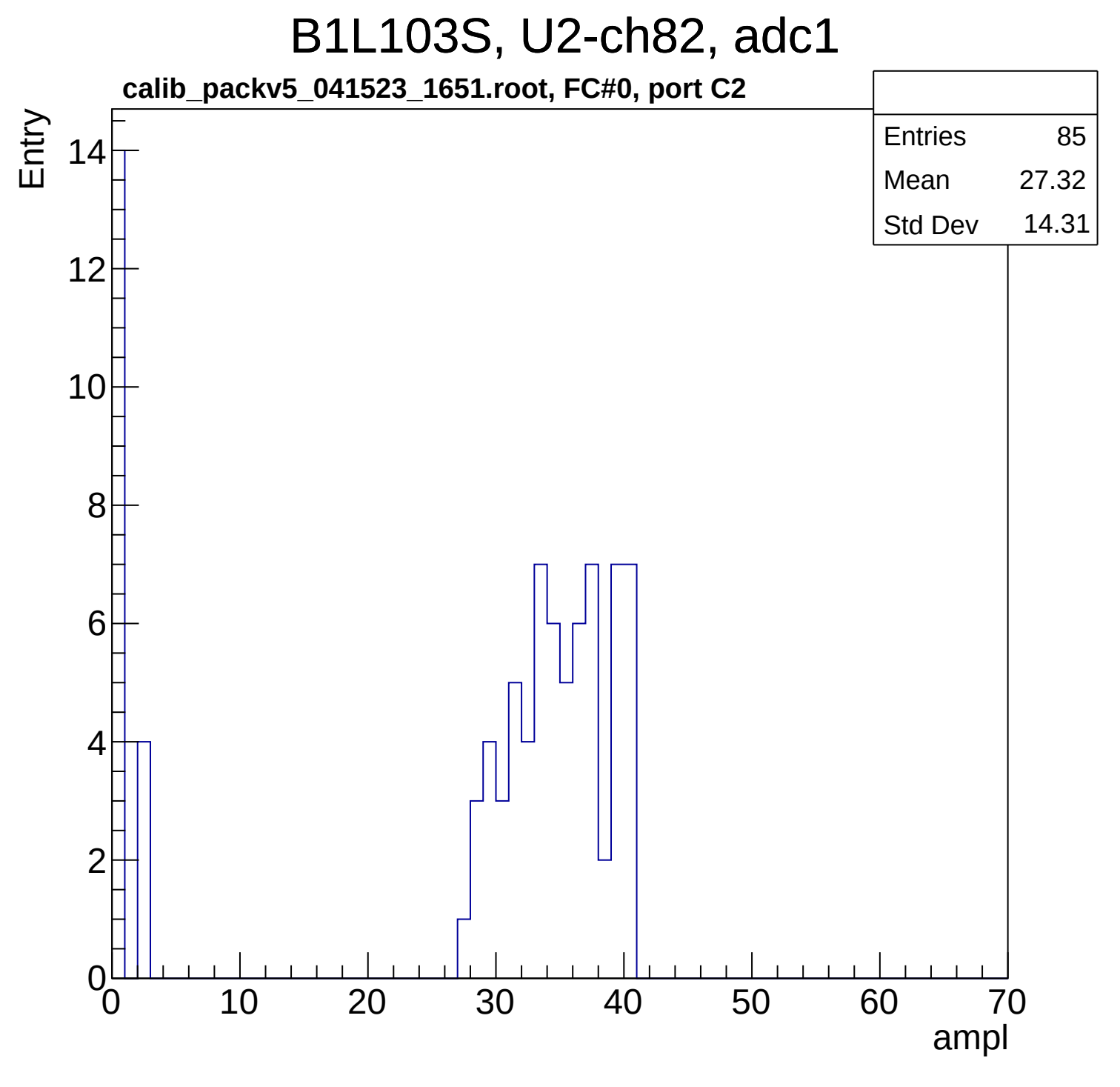

B1L103S, U2-ch81, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 51.77
Std Dev 3.378
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

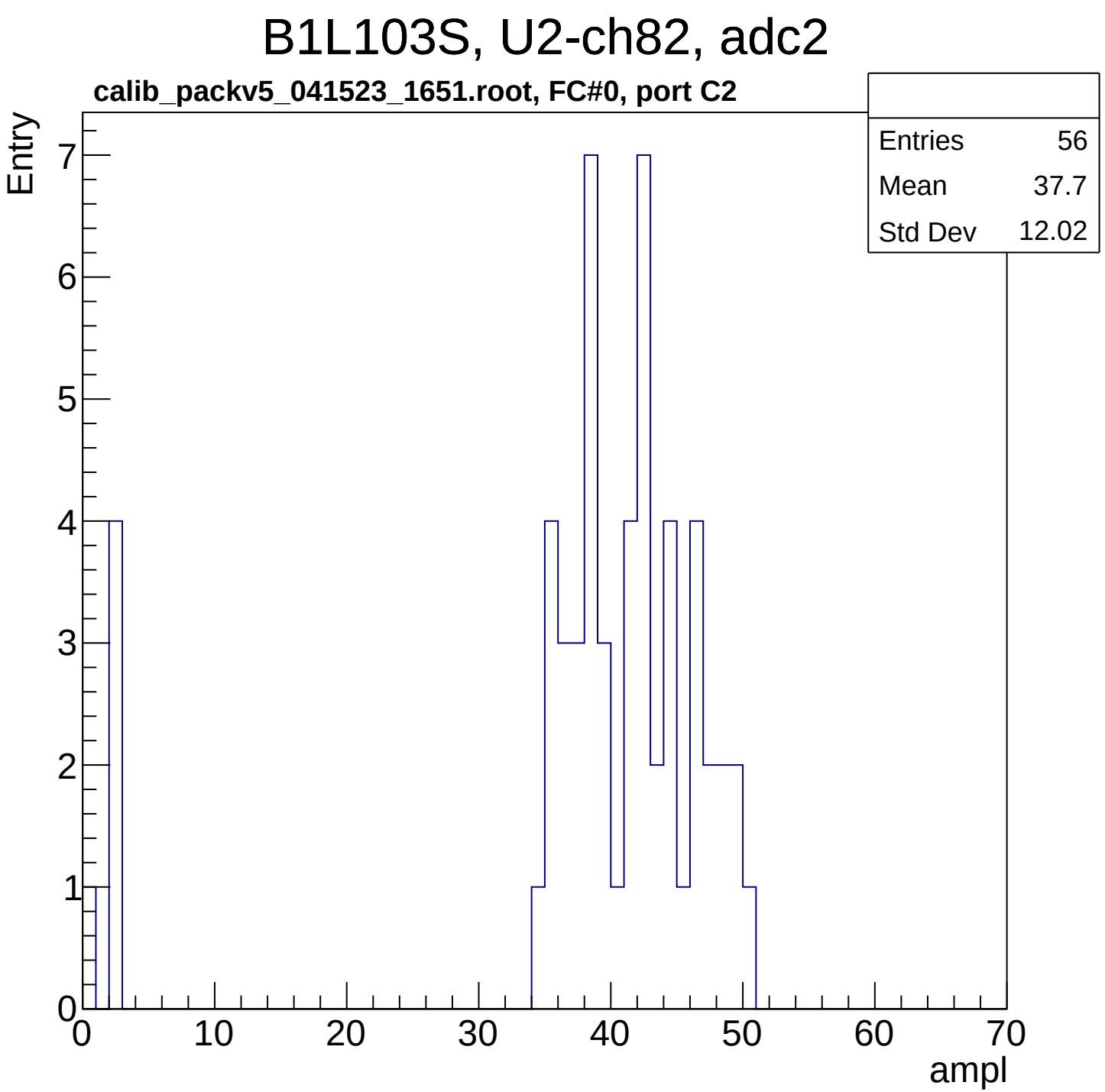

B1L103S, U2-ch81, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 58.05
Std Dev 2.743
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

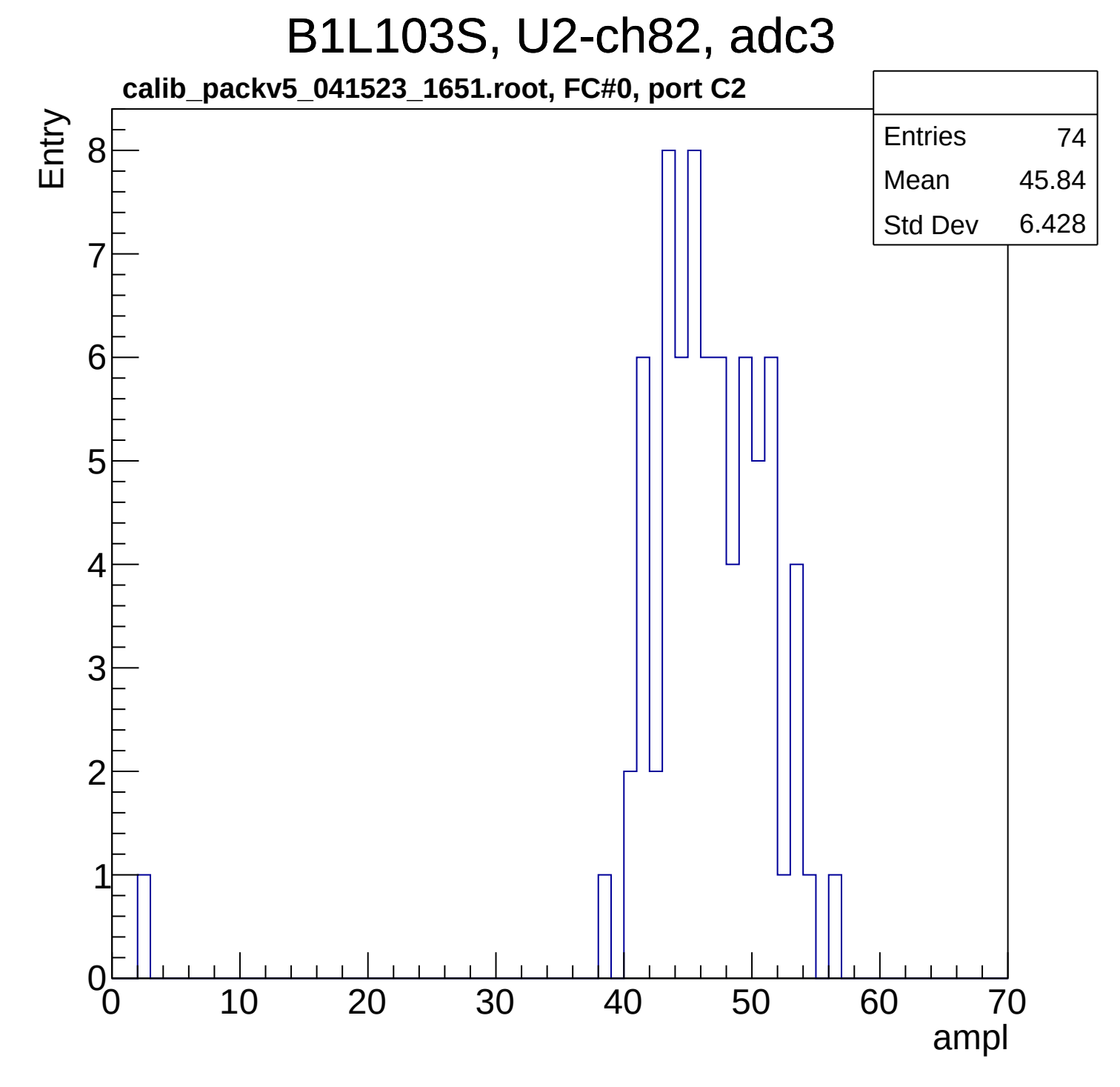

B1L103S, U2-ch81, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 58.59
Std Dev 12.86
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

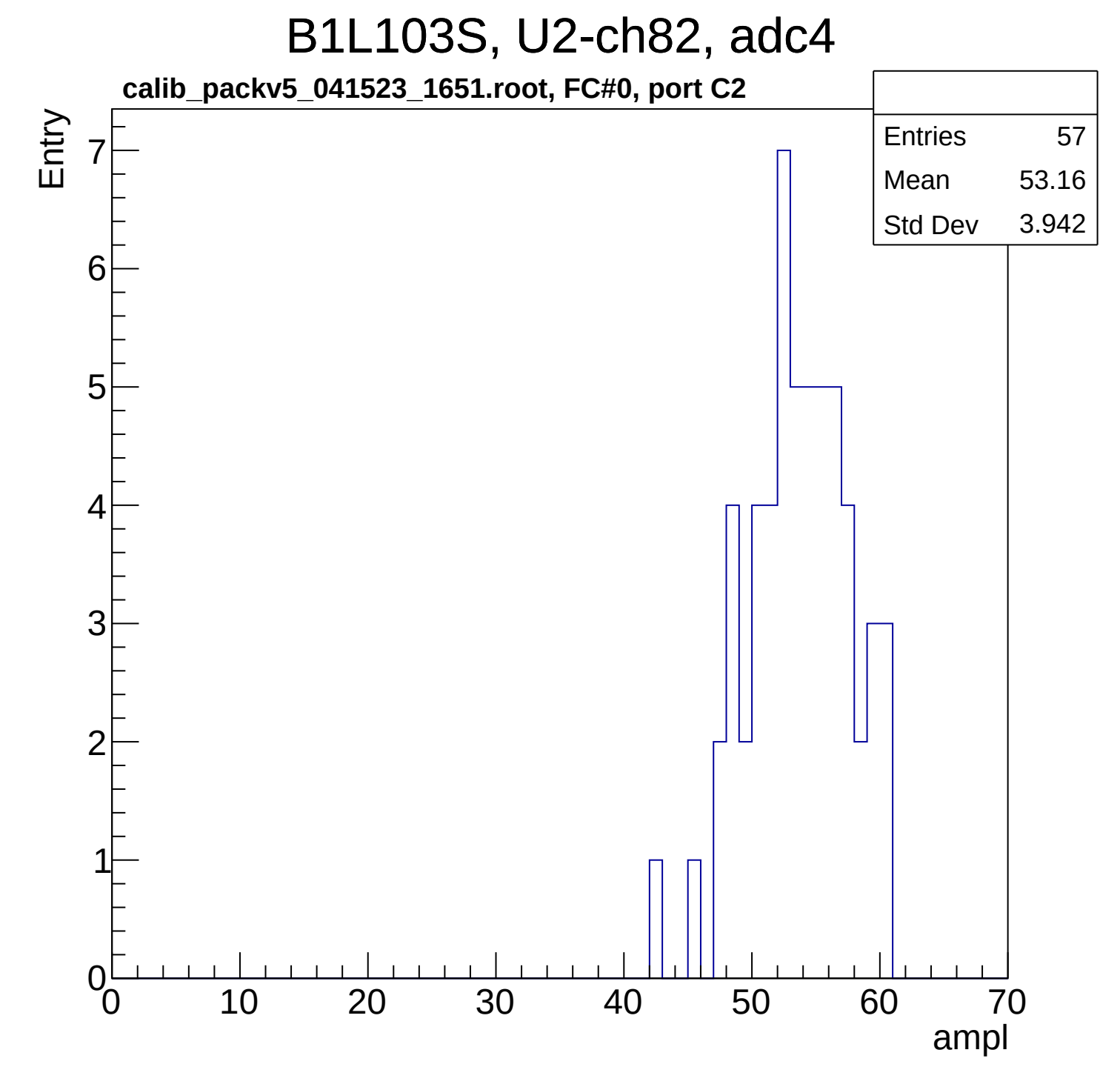

B1L103S, U2-ch81, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.227
Std Dev 20.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

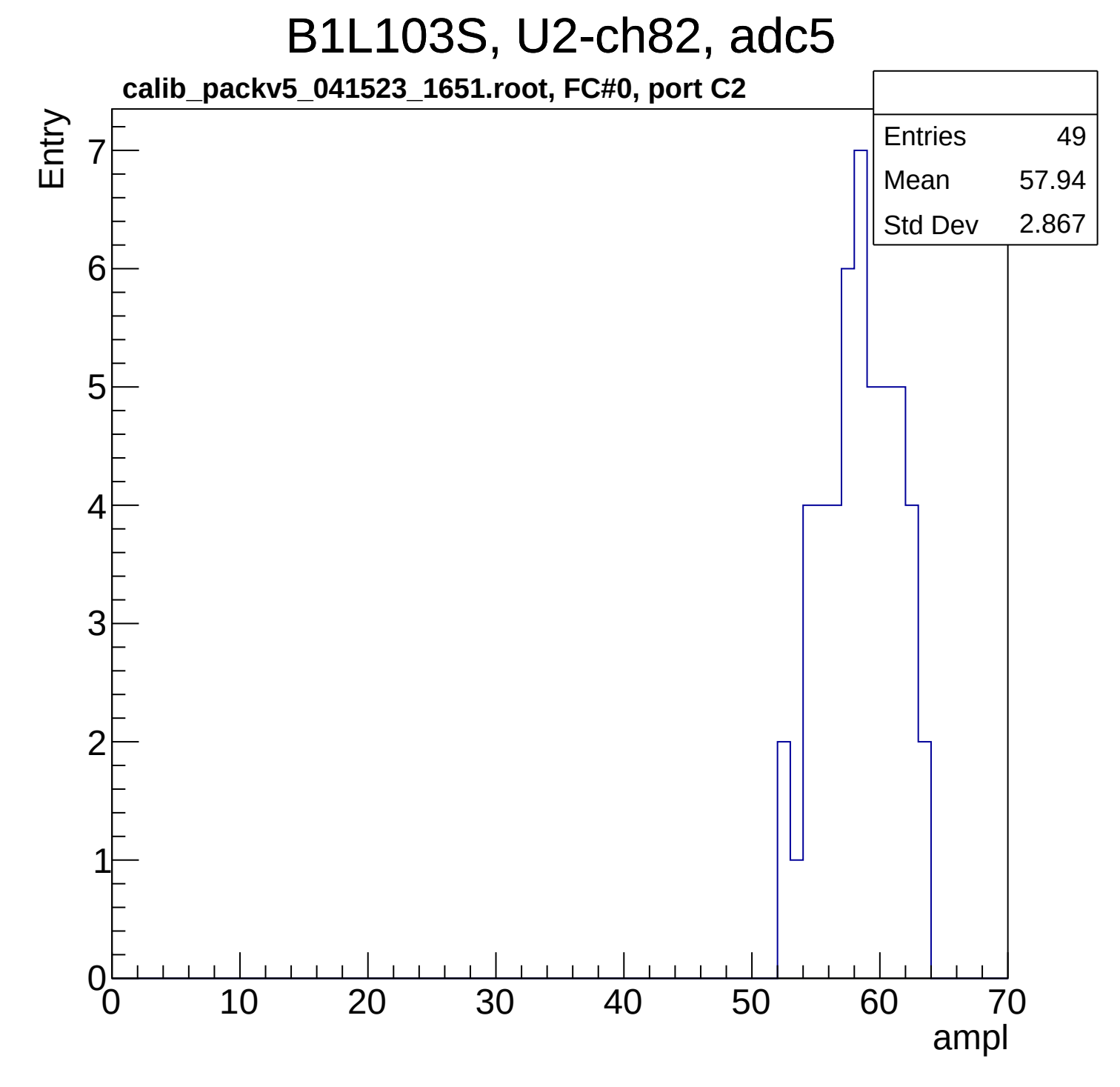

B1L103S, U2-ch82, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 153
Mean 14.11
Std Dev 13.67
Entry
ampl
0
5
10
15
20
25
30
35
40
0
10
20
30
40
50
60
70

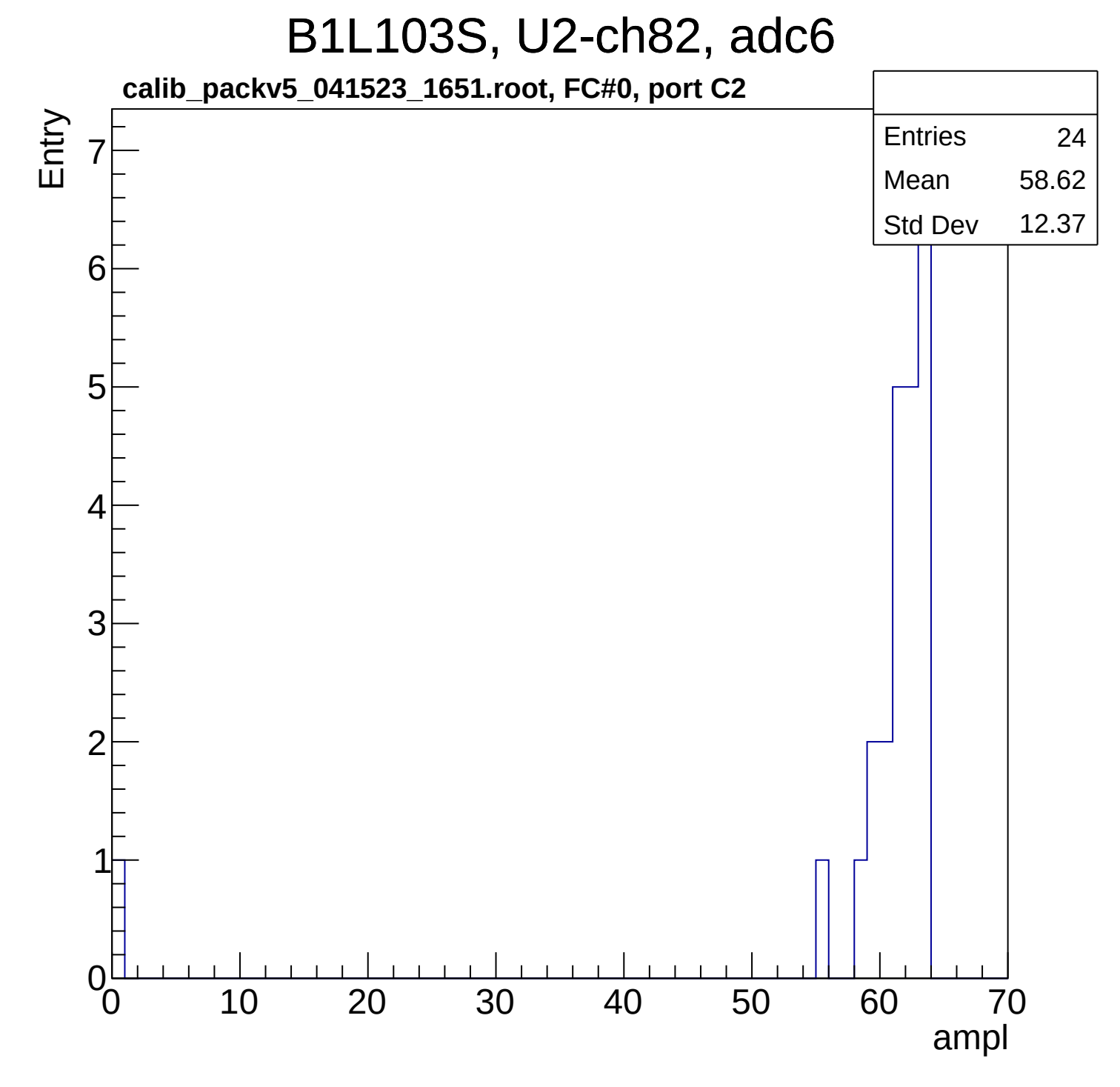

B1L103S, U2-ch82, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 27.32
Std Dev 14.31
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

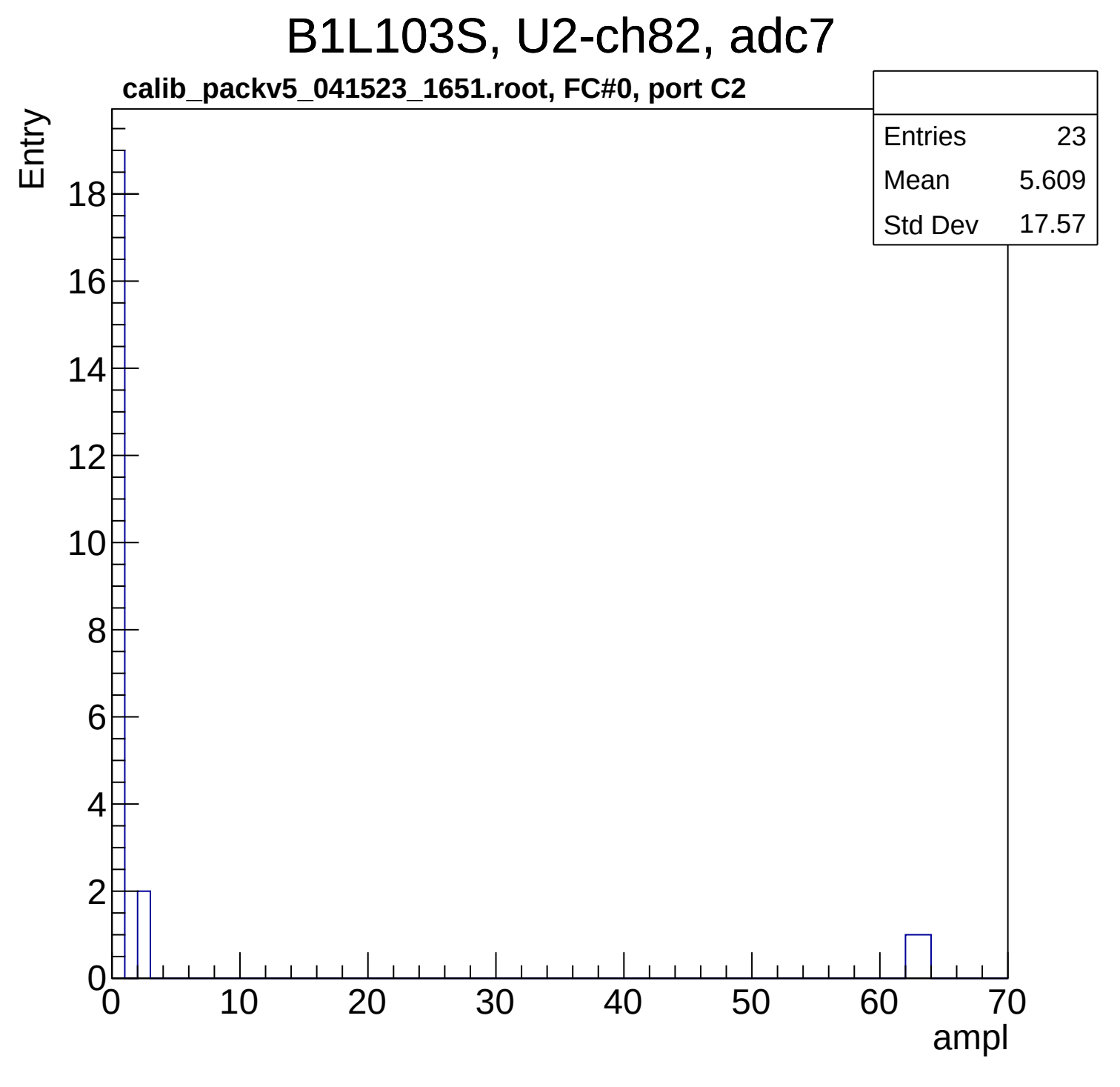

B1L103S, U2-ch82, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 37.7
Std Dev 12.02
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

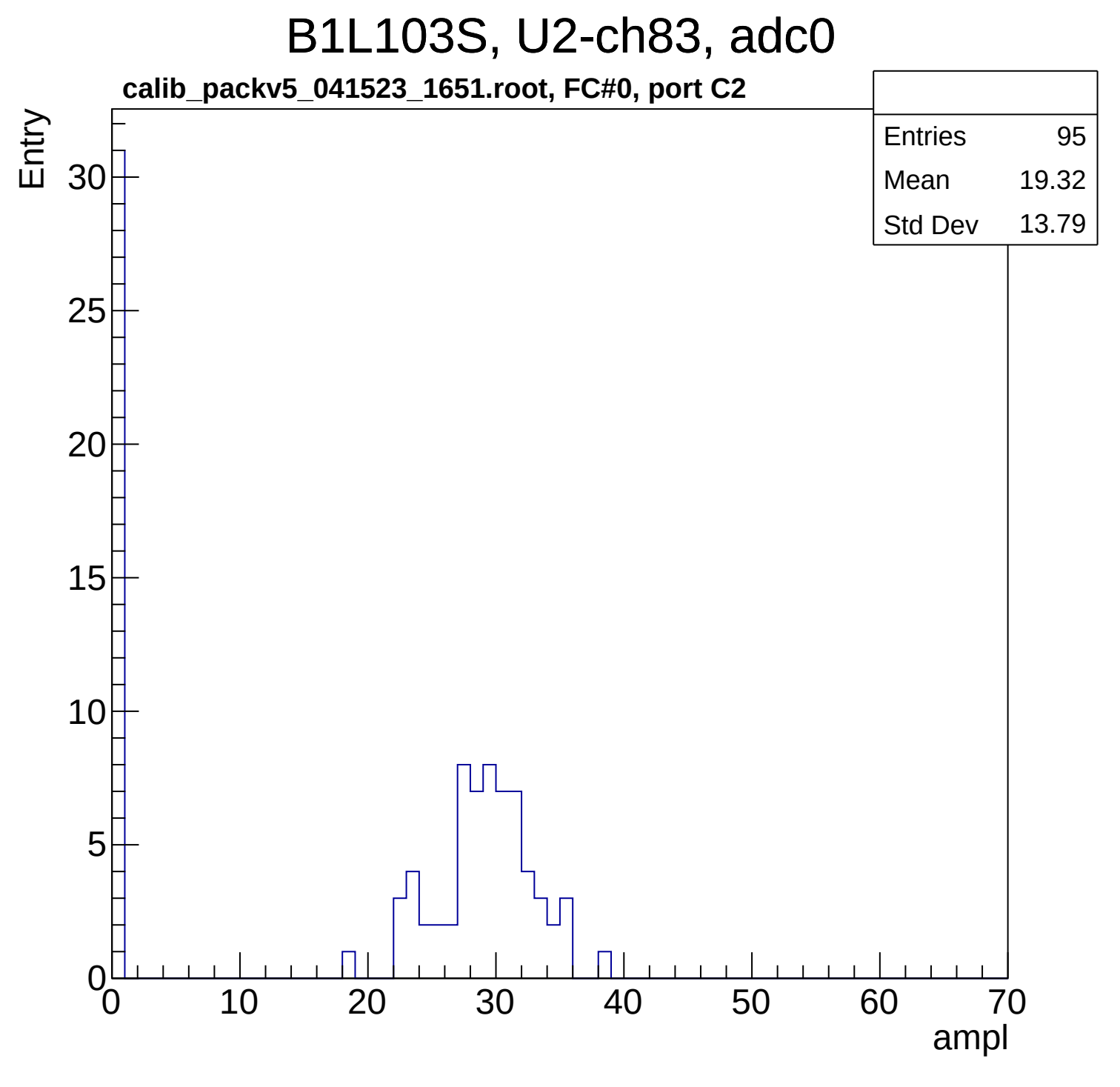

B1L103S, U2-ch82, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 45.84
Std Dev 6.428
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

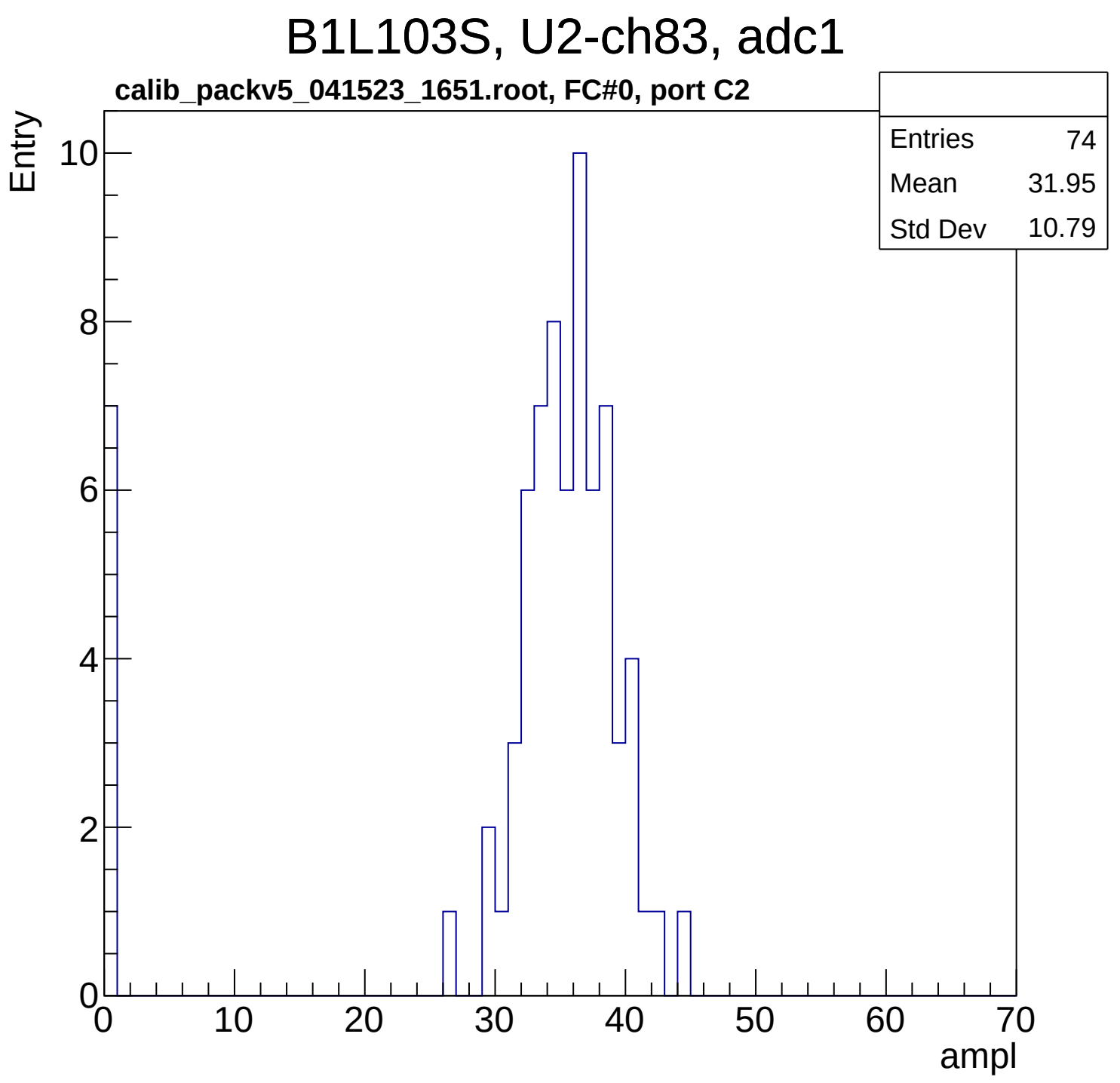

B1L103S, U2-ch82, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 53.16
Std Dev 3.942
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

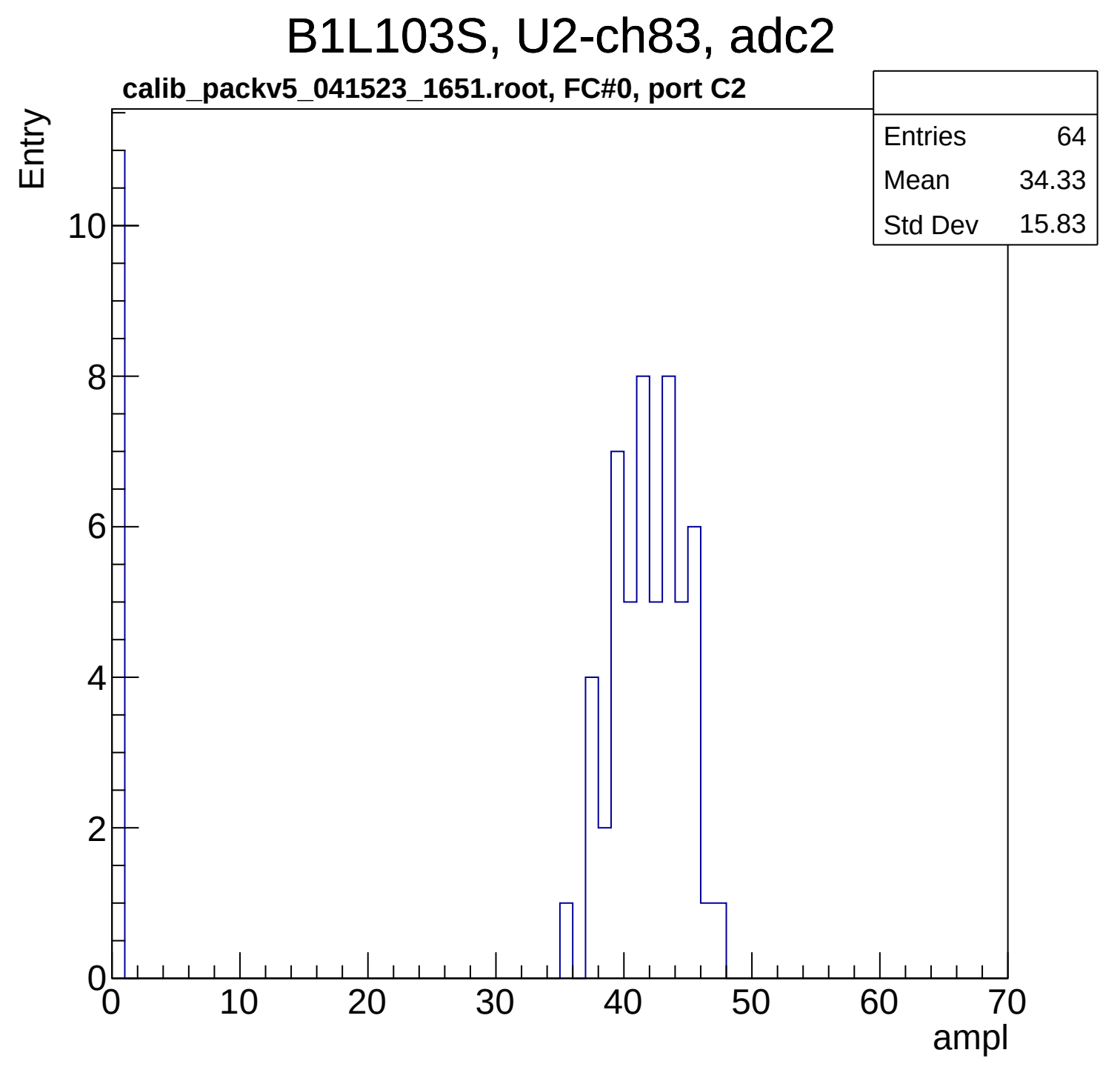

B1L103S, U2-ch82, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 57.94
Std Dev 2.867
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

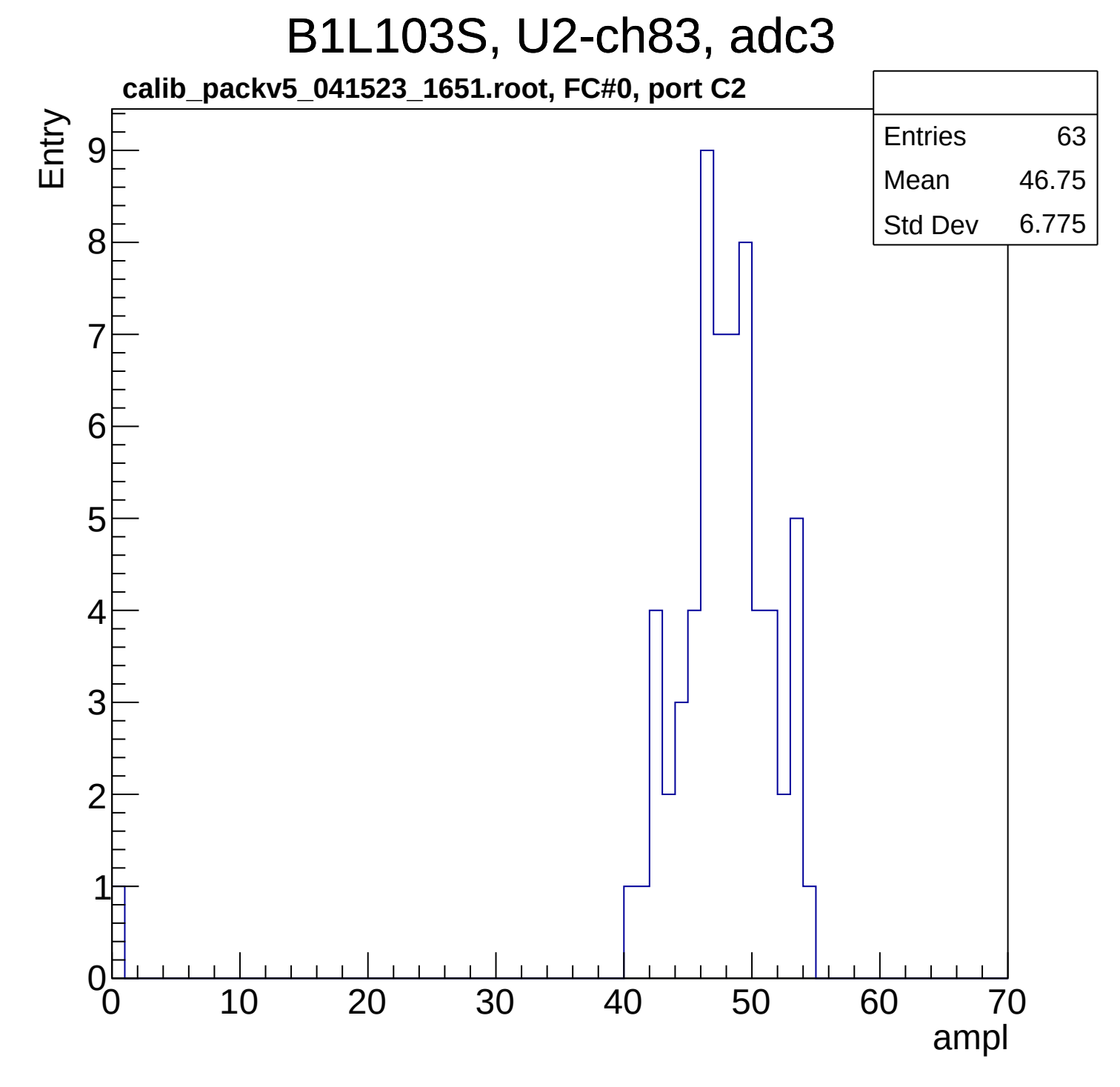

B1L103S, U2-ch82, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 58.62
Std Dev 12.37
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

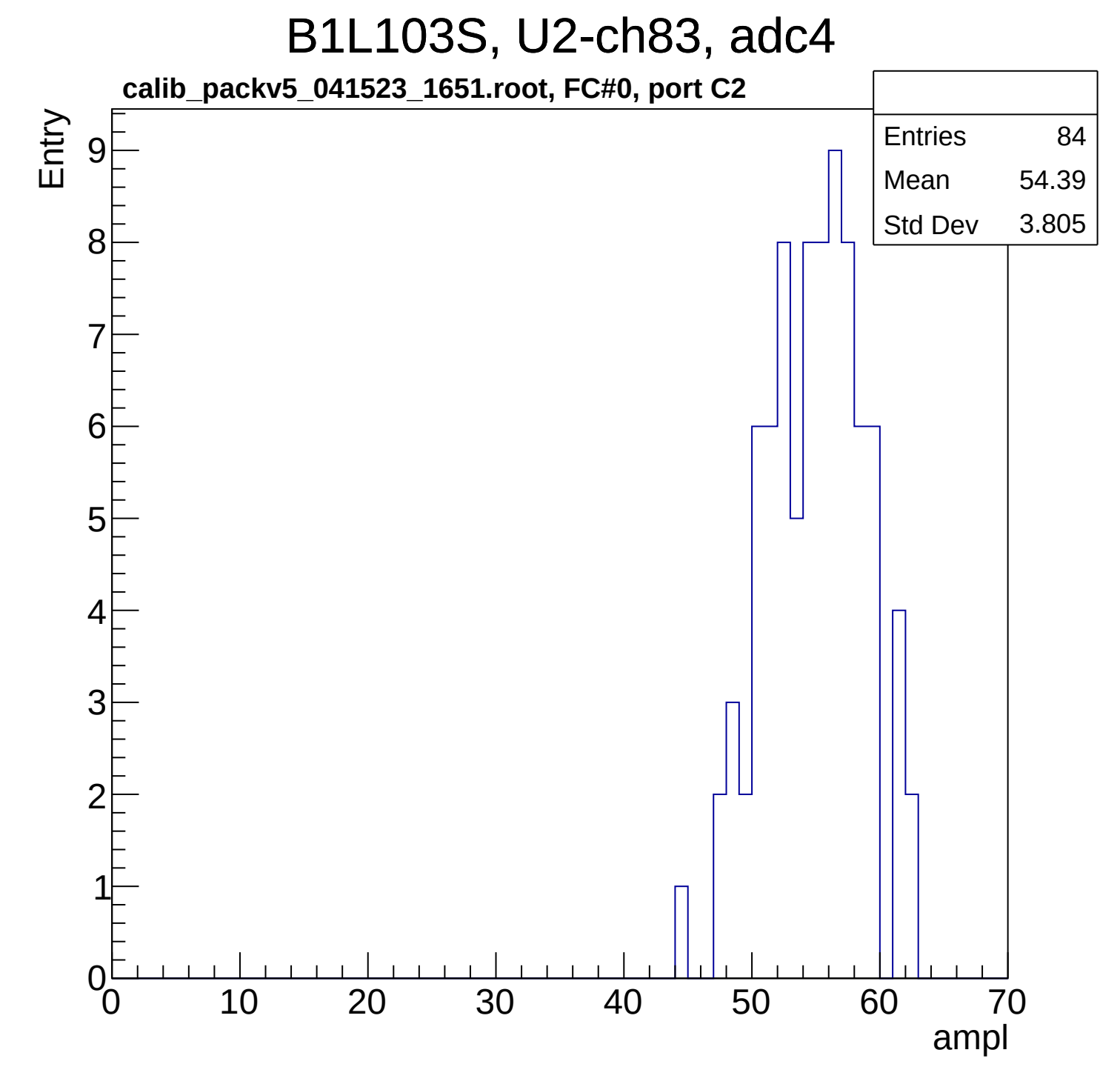

B1L103S, U2-ch82, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 5.609
Std Dev 17.57
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70

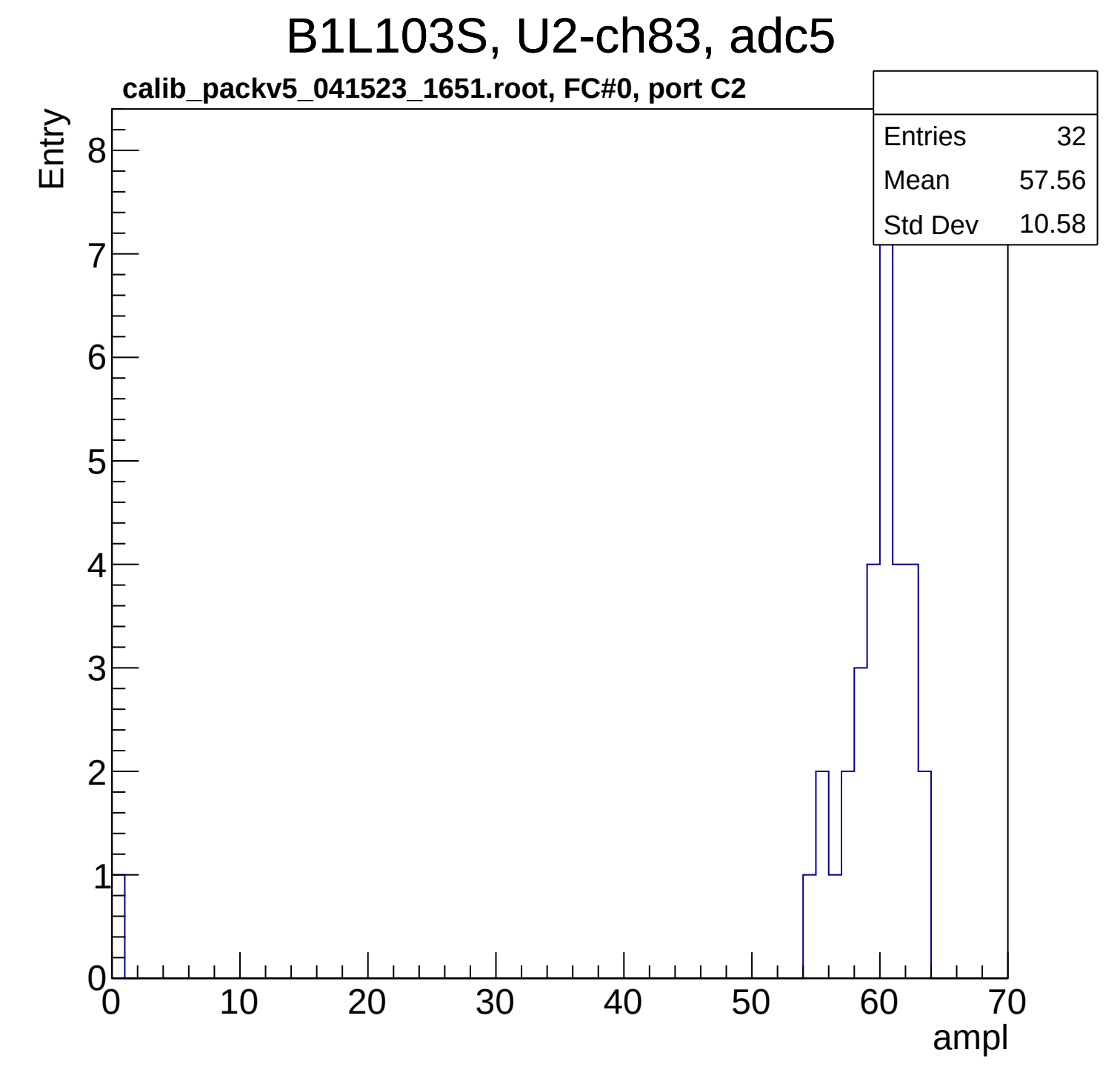

B1L103S, U2-ch83, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 19.32
Std Dev 13.79
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl

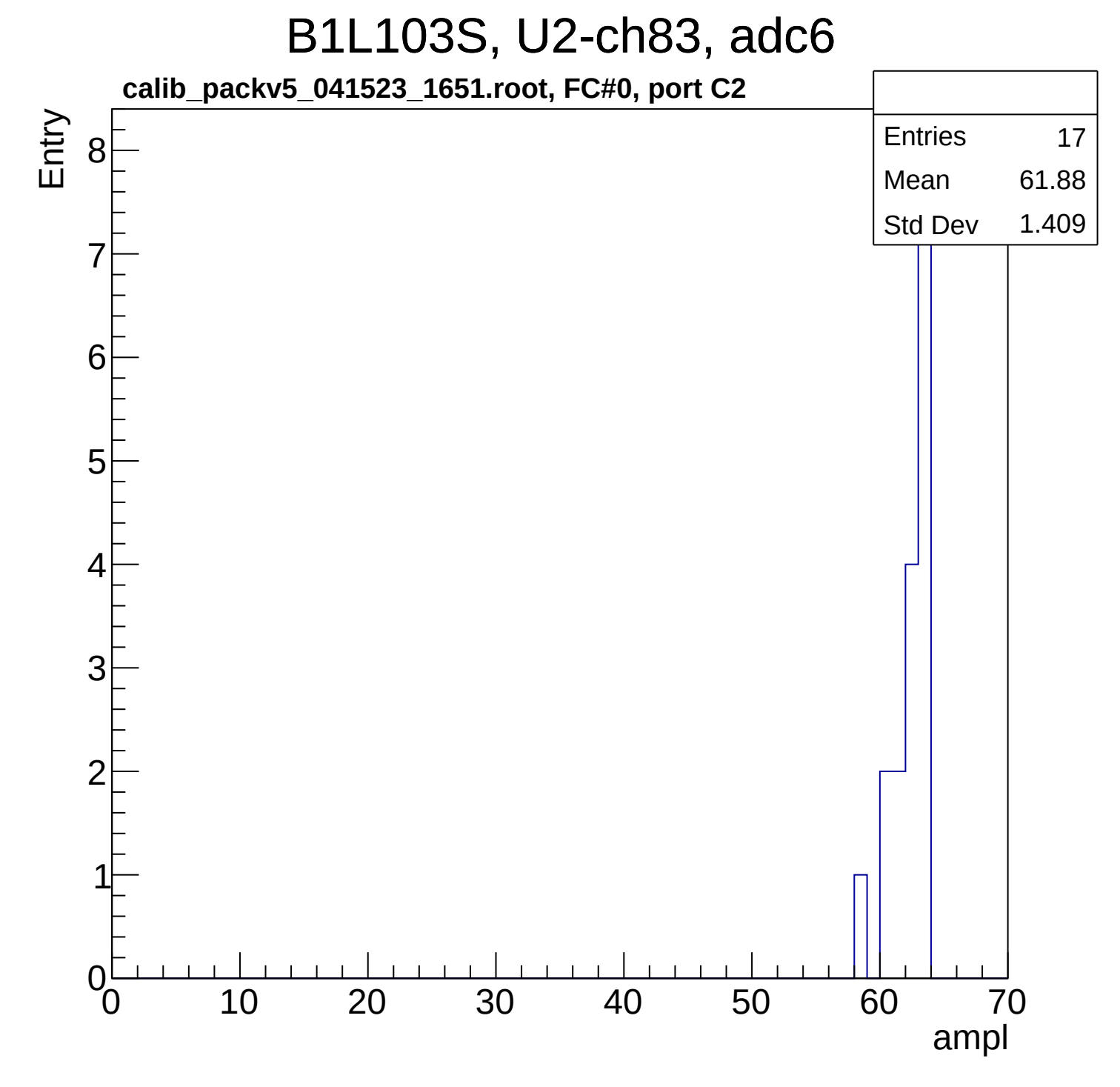

B1L103S, U2-ch83, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 31.95
Std Dev 10.79
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

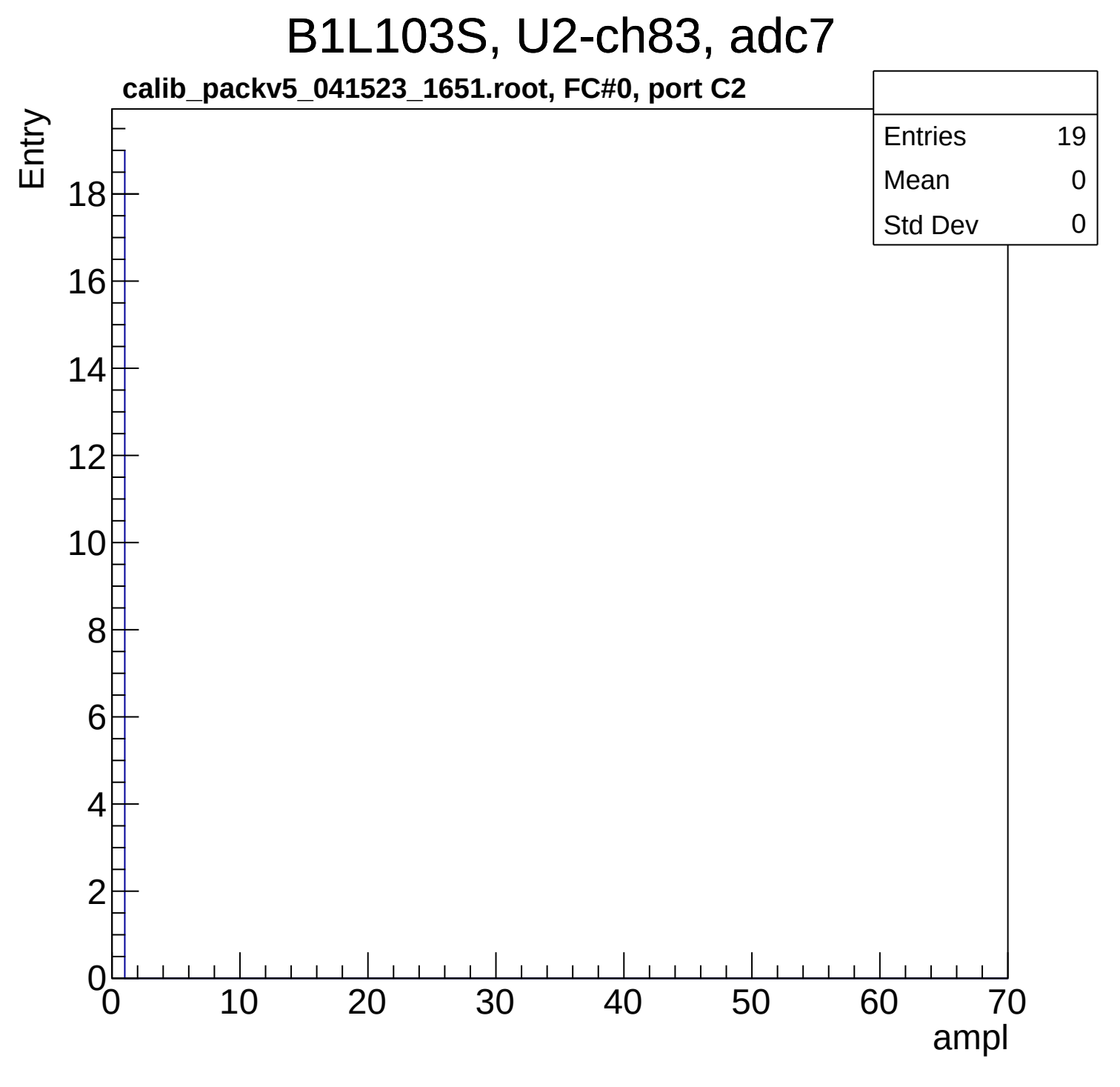

B1L103S, U2-ch83, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 34.33
Std Dev 15.83
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

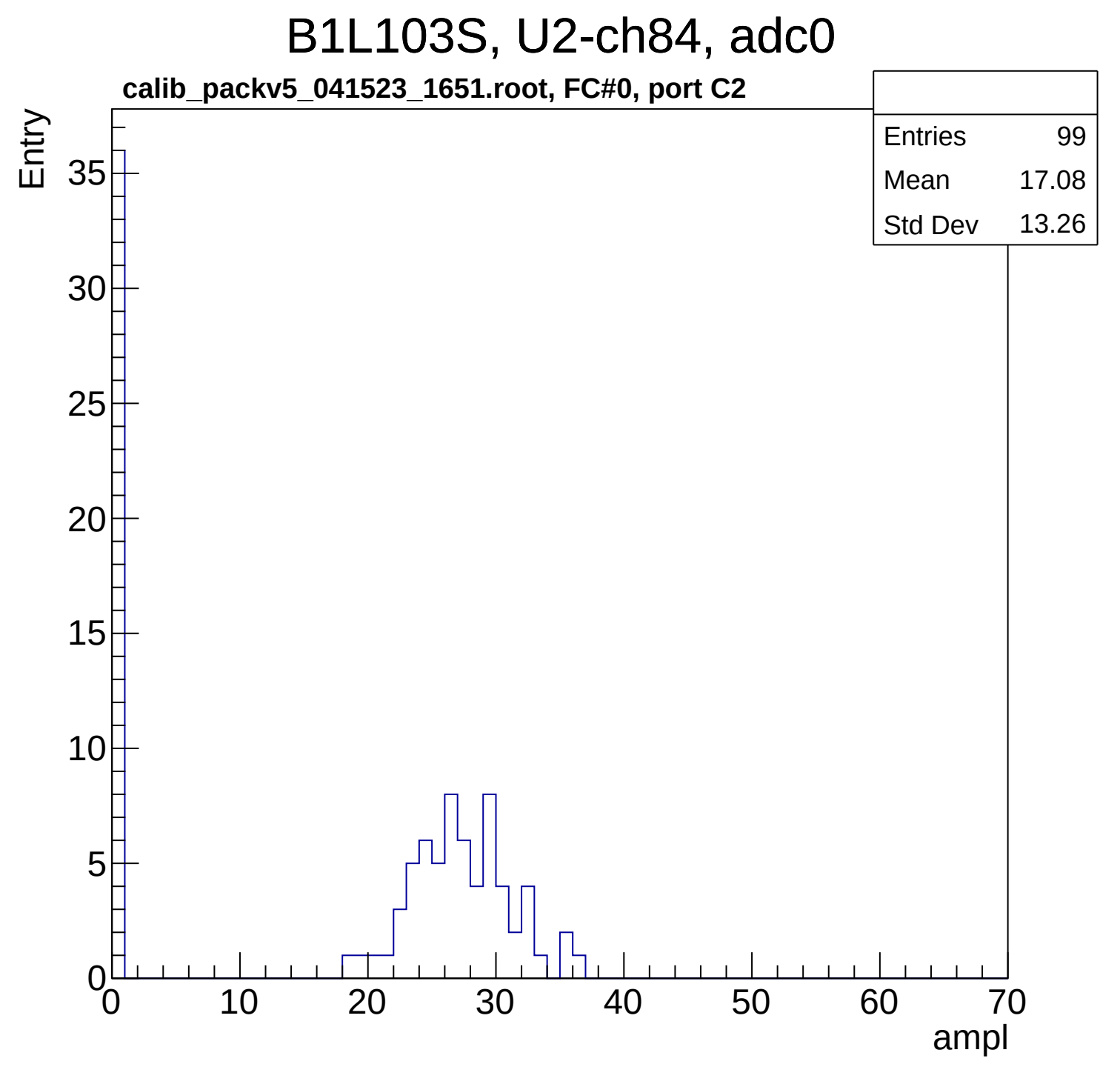

B1L103S, U2-ch83, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 46.75
Std Dev 6.775
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

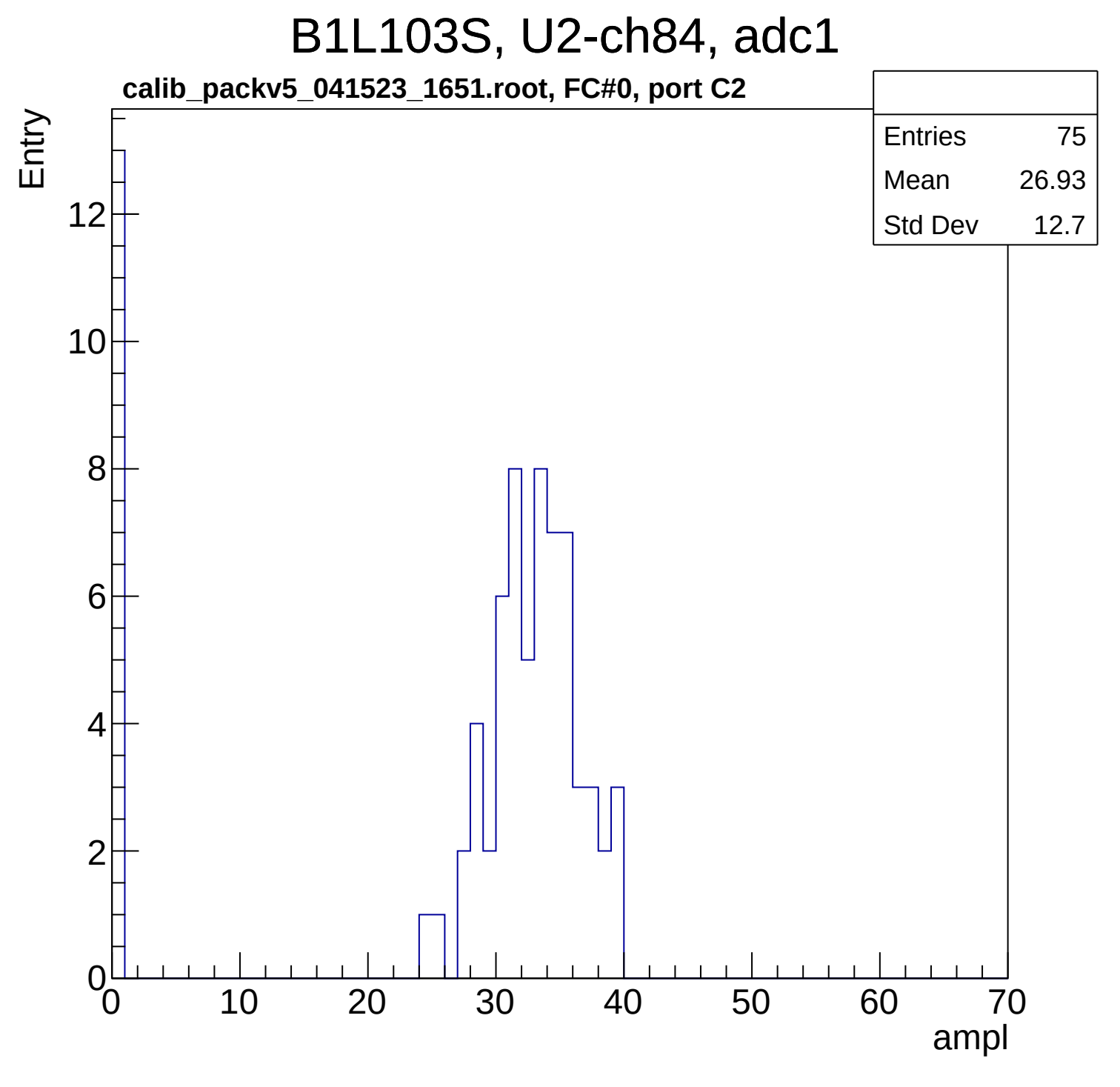

B1L103S, U2-ch83, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 54.39
Std Dev 3.805
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

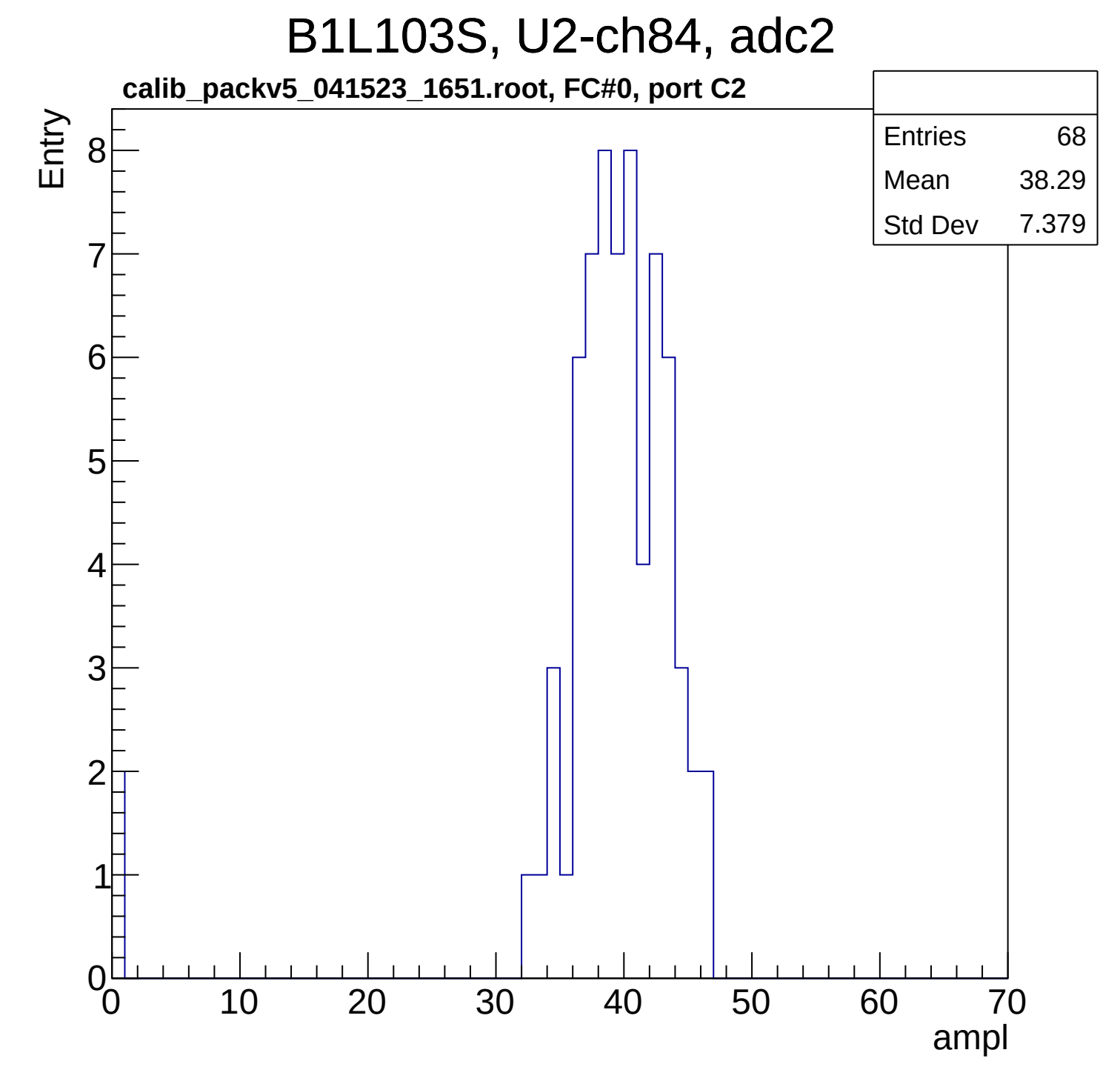

B1L103S, U2-ch83, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 57.56
Std Dev 10.58
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

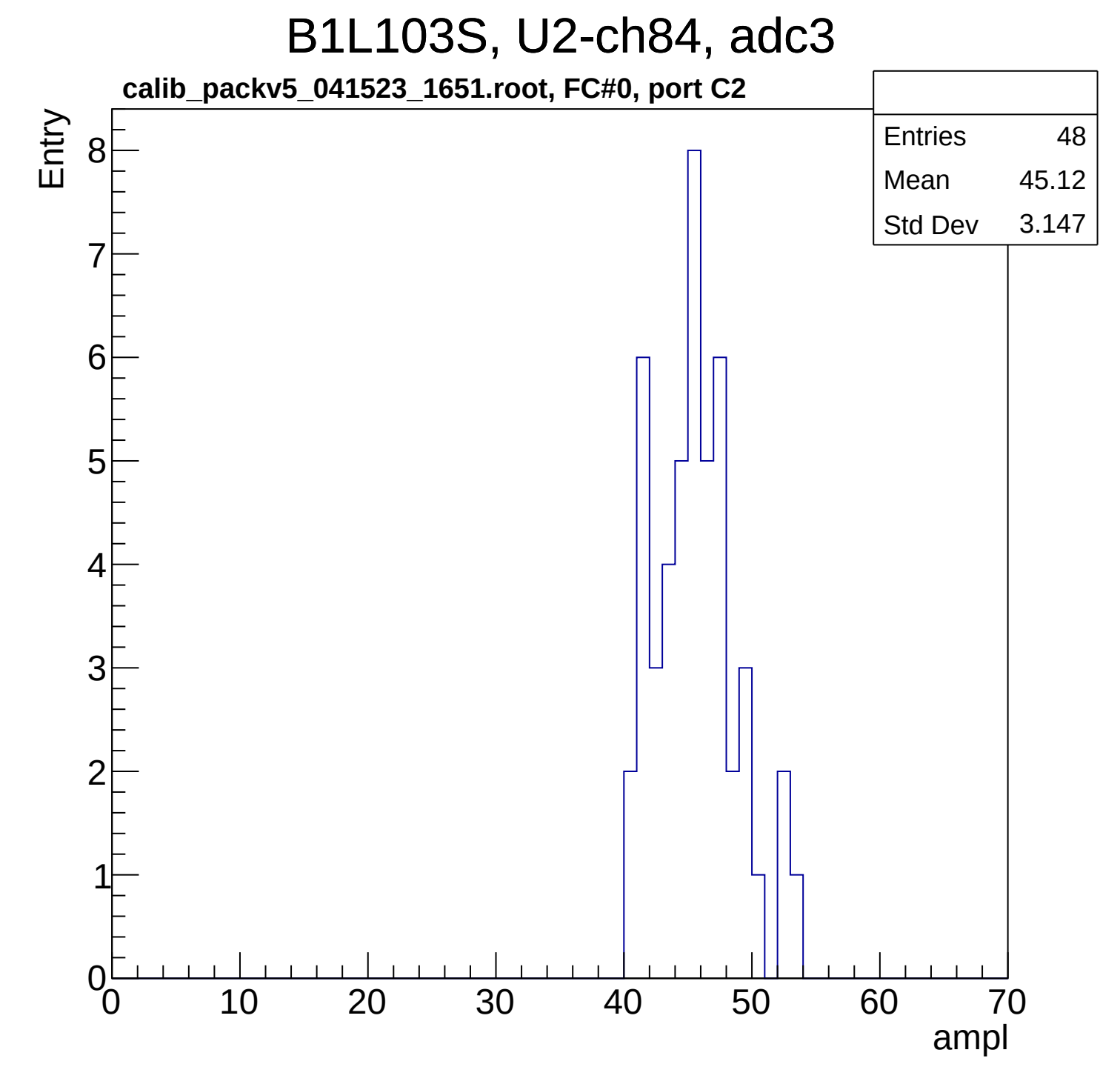

B1L103S, U2-ch83, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.88
Std Dev 1.409
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

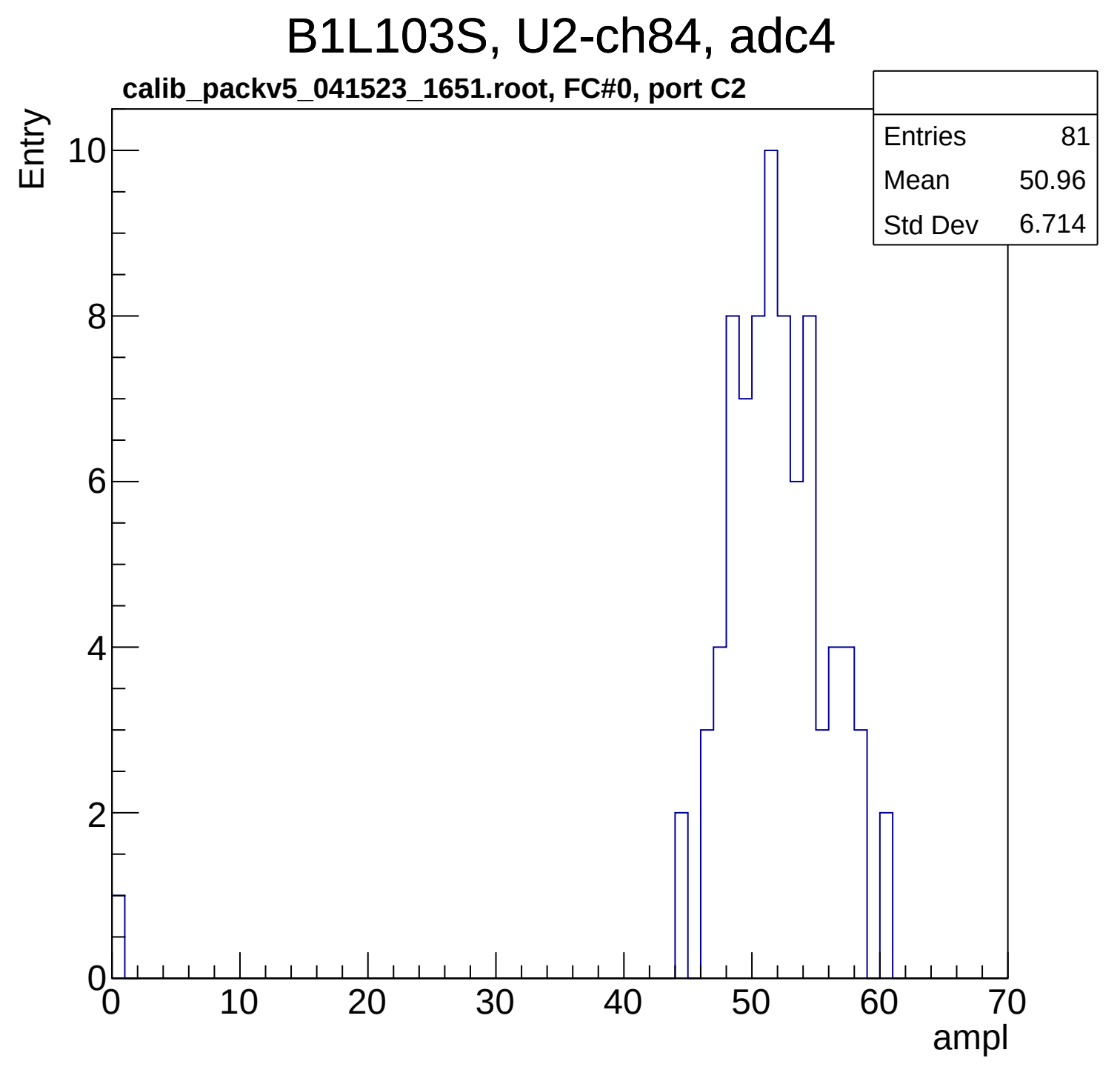

B1L103S, U2-ch83, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

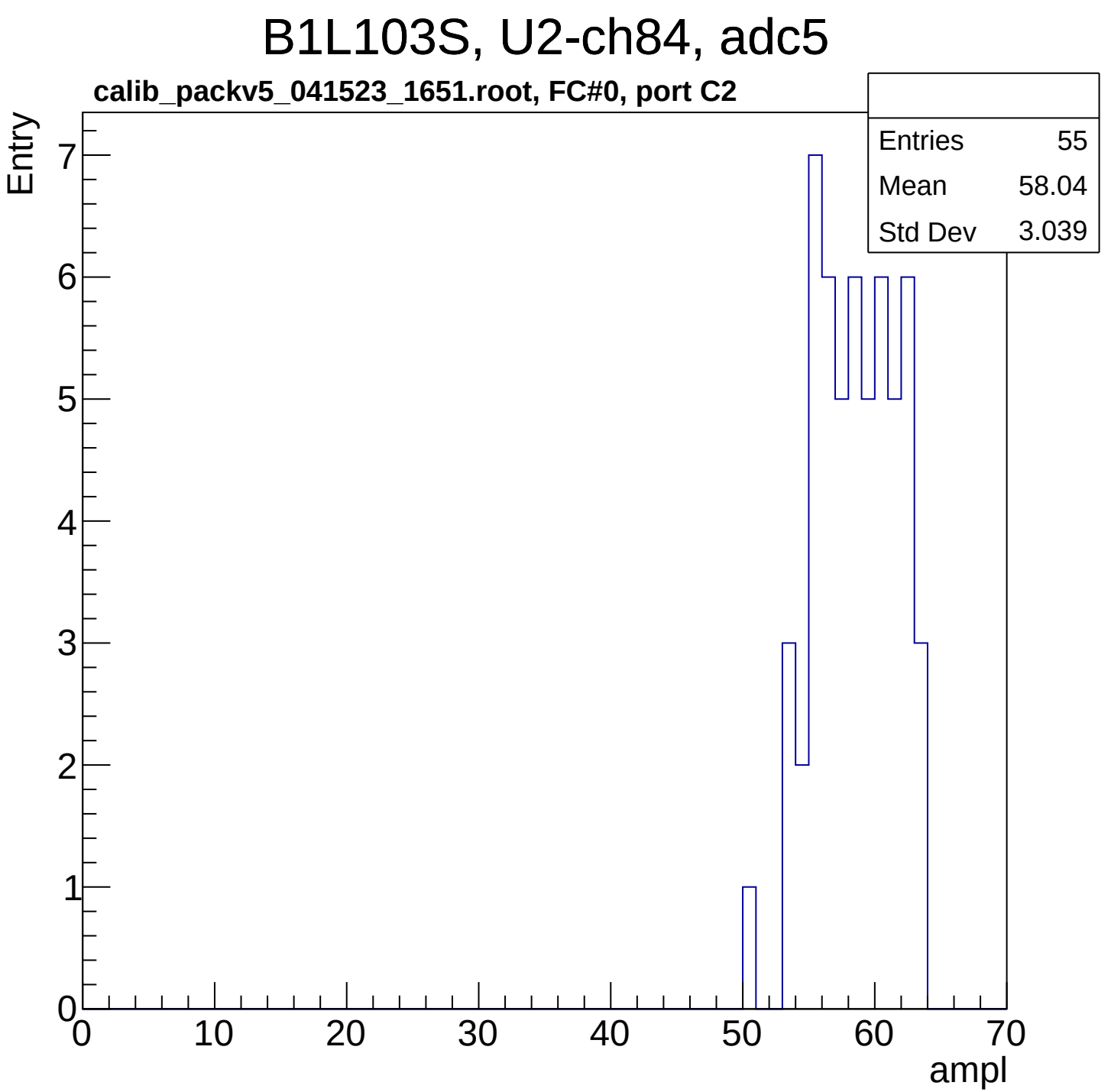

B1L103S, U2-ch84, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 17.08
Std Dev 13.26
Entry
ampl
0
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70

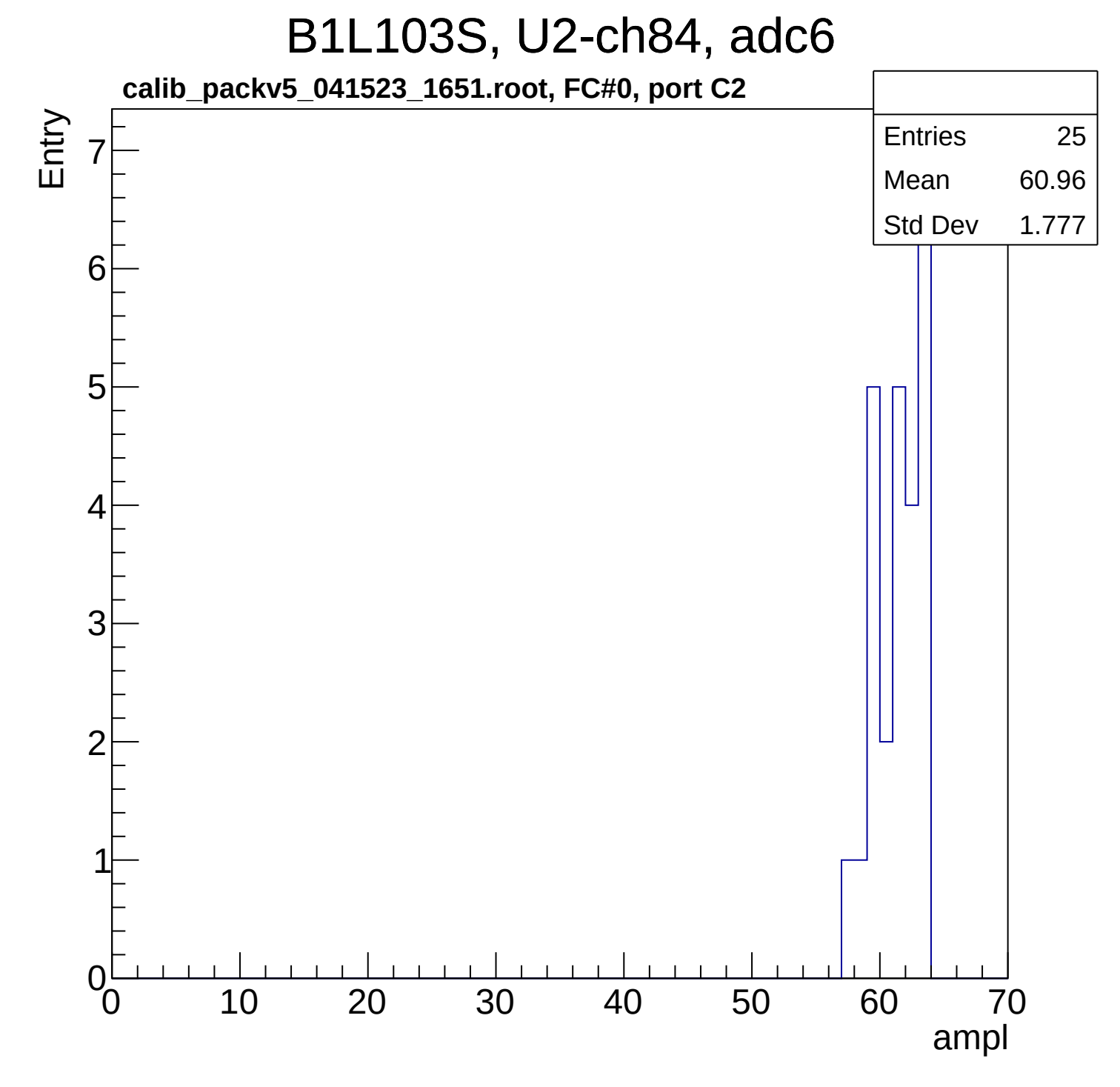

B1L103S, U2-ch84, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 26.93
Std Dev 12.7
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

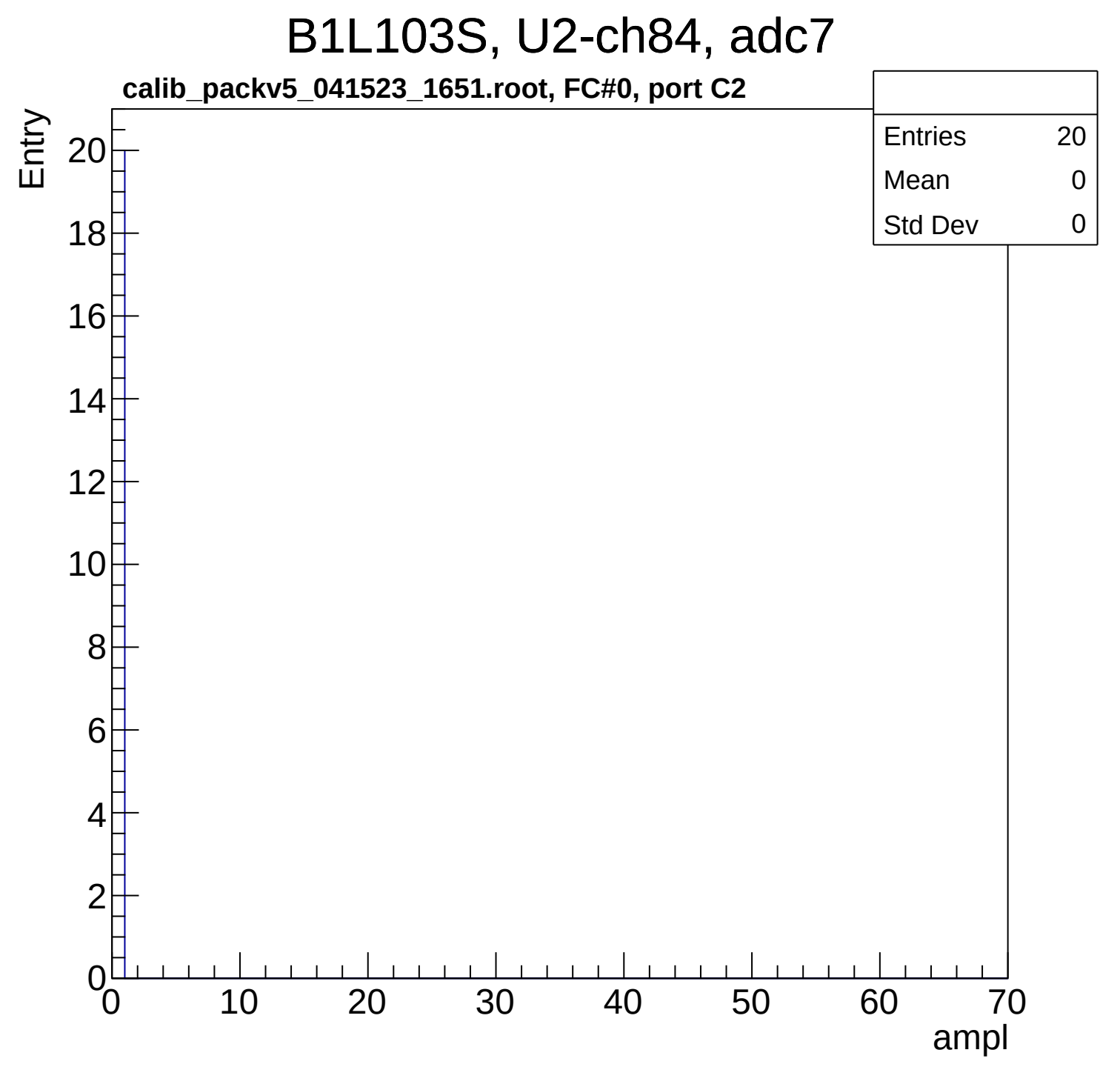

B1L103S, U2-ch84, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 38.29
Std Dev 7.379
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

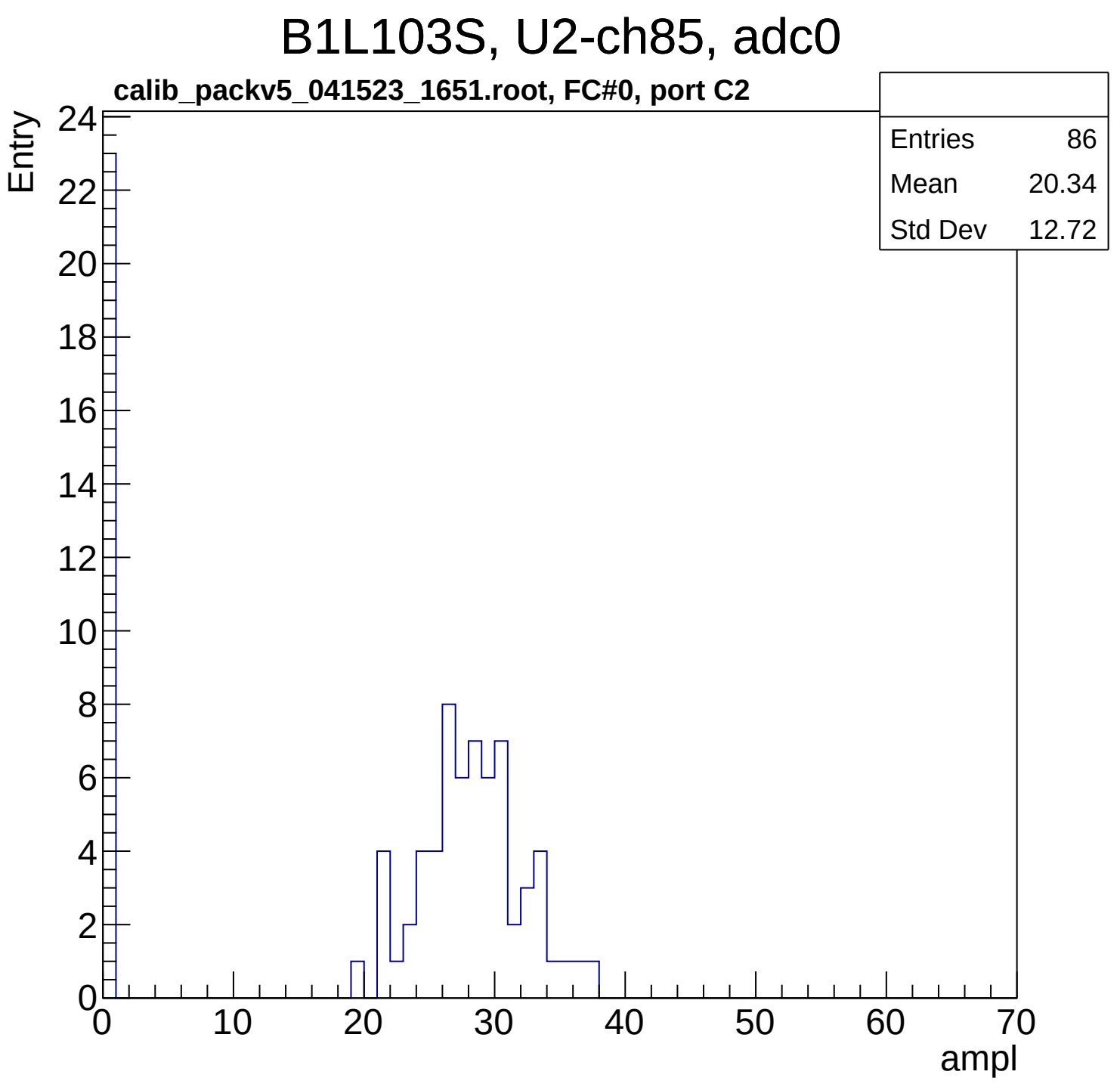

B1L103S, U2-ch84, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 45.12
Std Dev 3.147
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

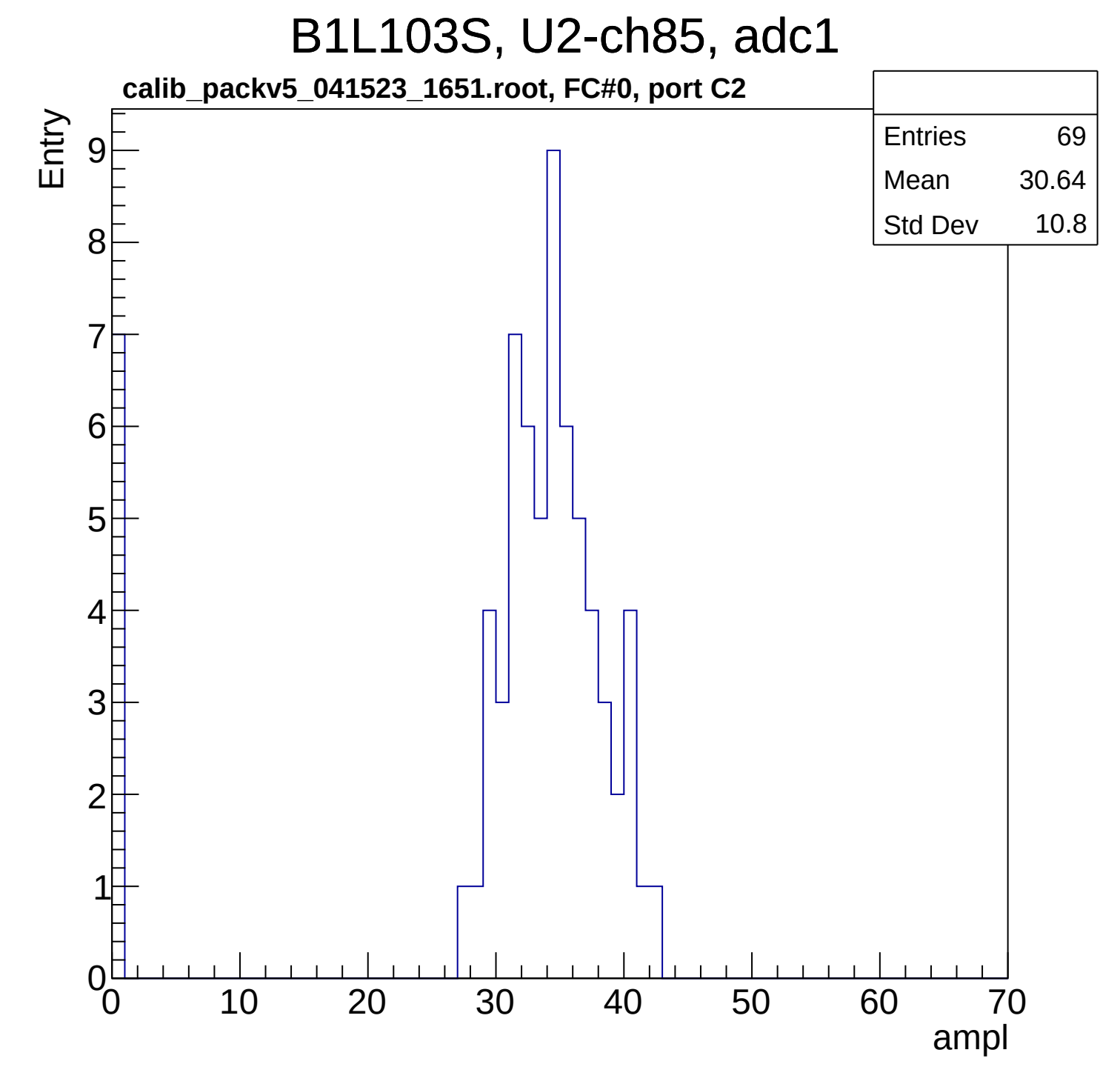

B1L103S, U2-ch84, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 50.96
Std Dev 6.714
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

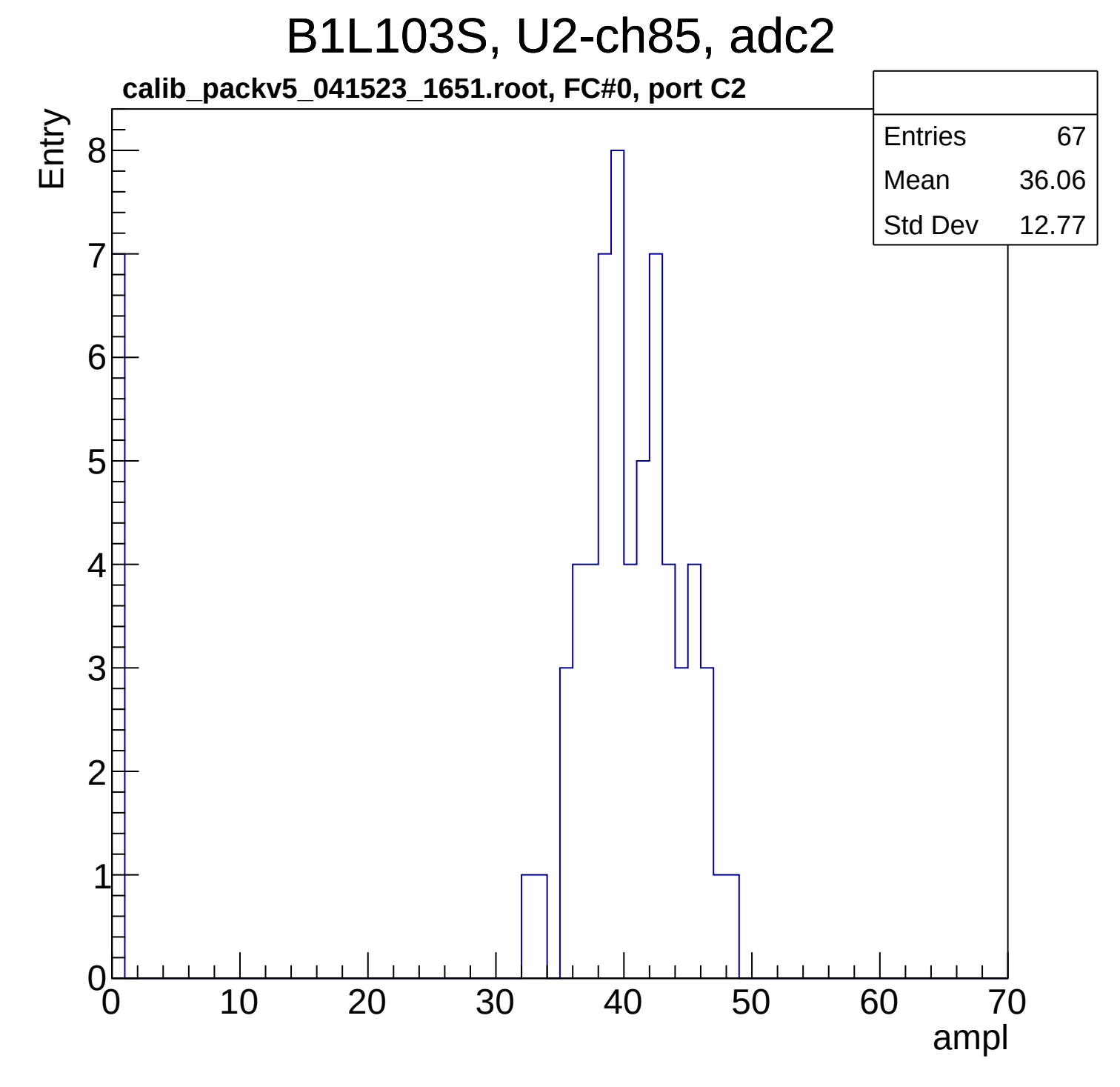

B1L103S, U2-ch84, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.04
Std Dev 3.039
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

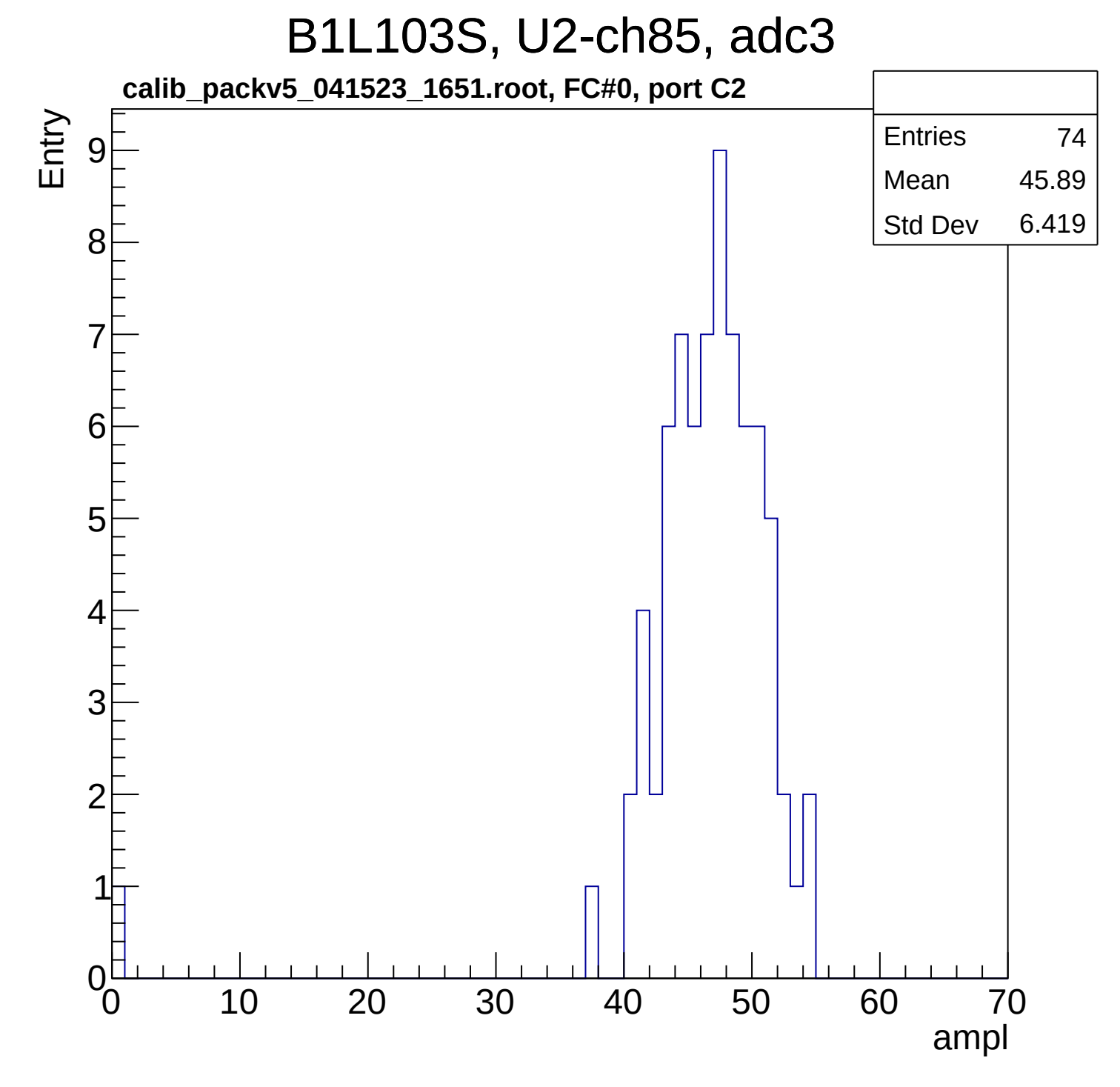

B1L103S, U2-ch84, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 60.96
Std Dev 1.777
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

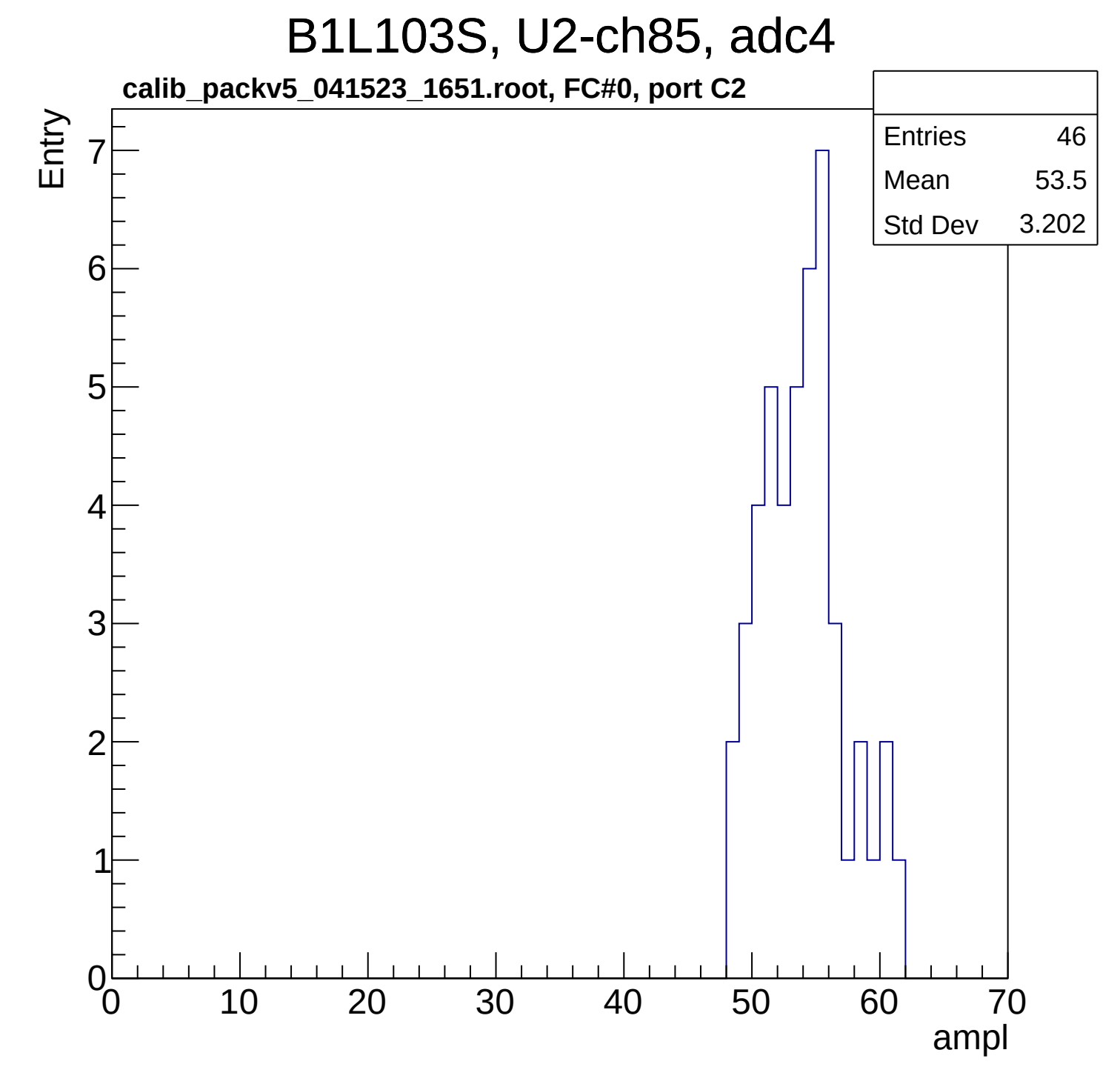

B1L103S, U2-ch84, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl

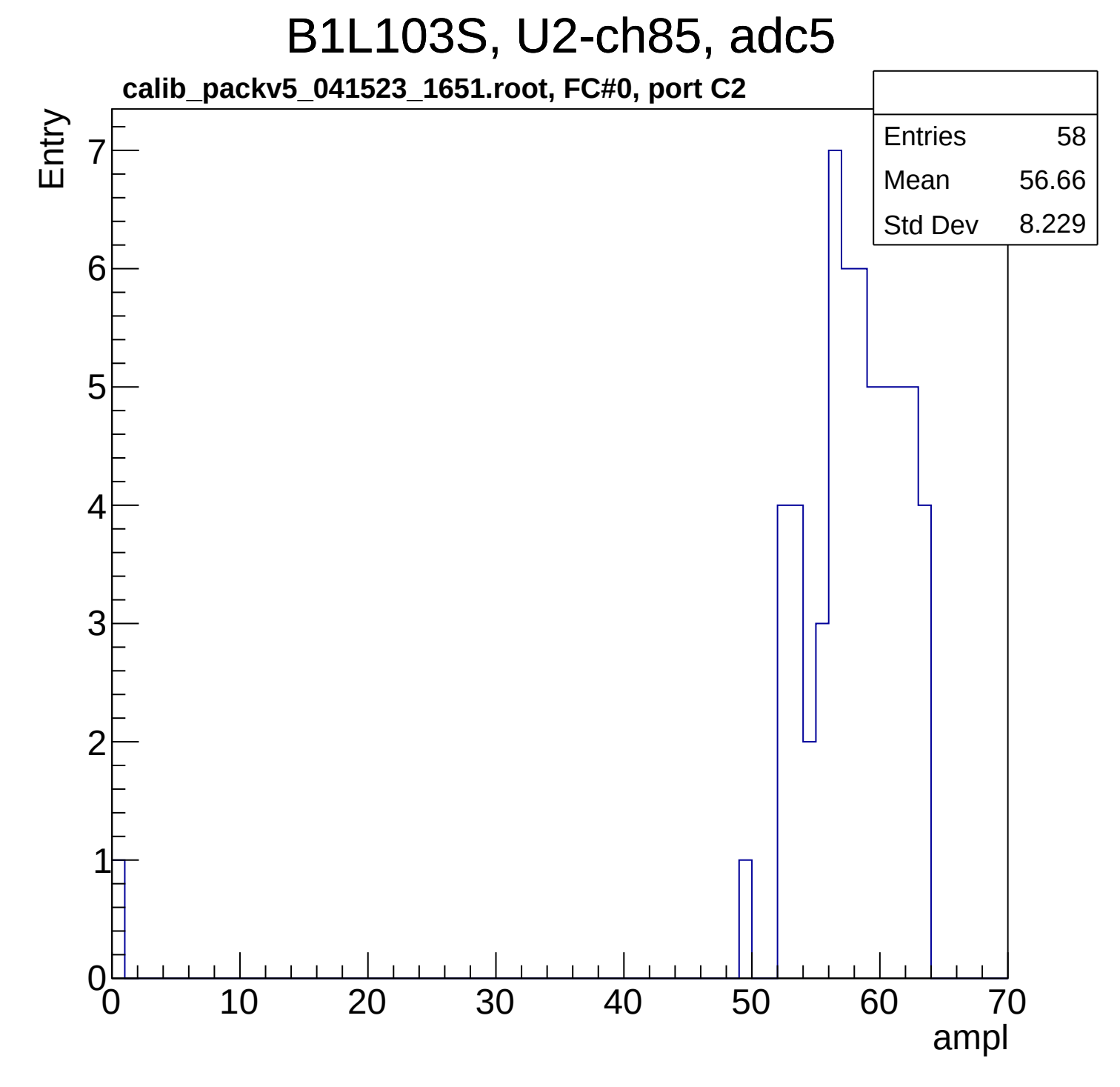

B1L103S, U2-ch85, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 20.34
Std Dev 12.72
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70

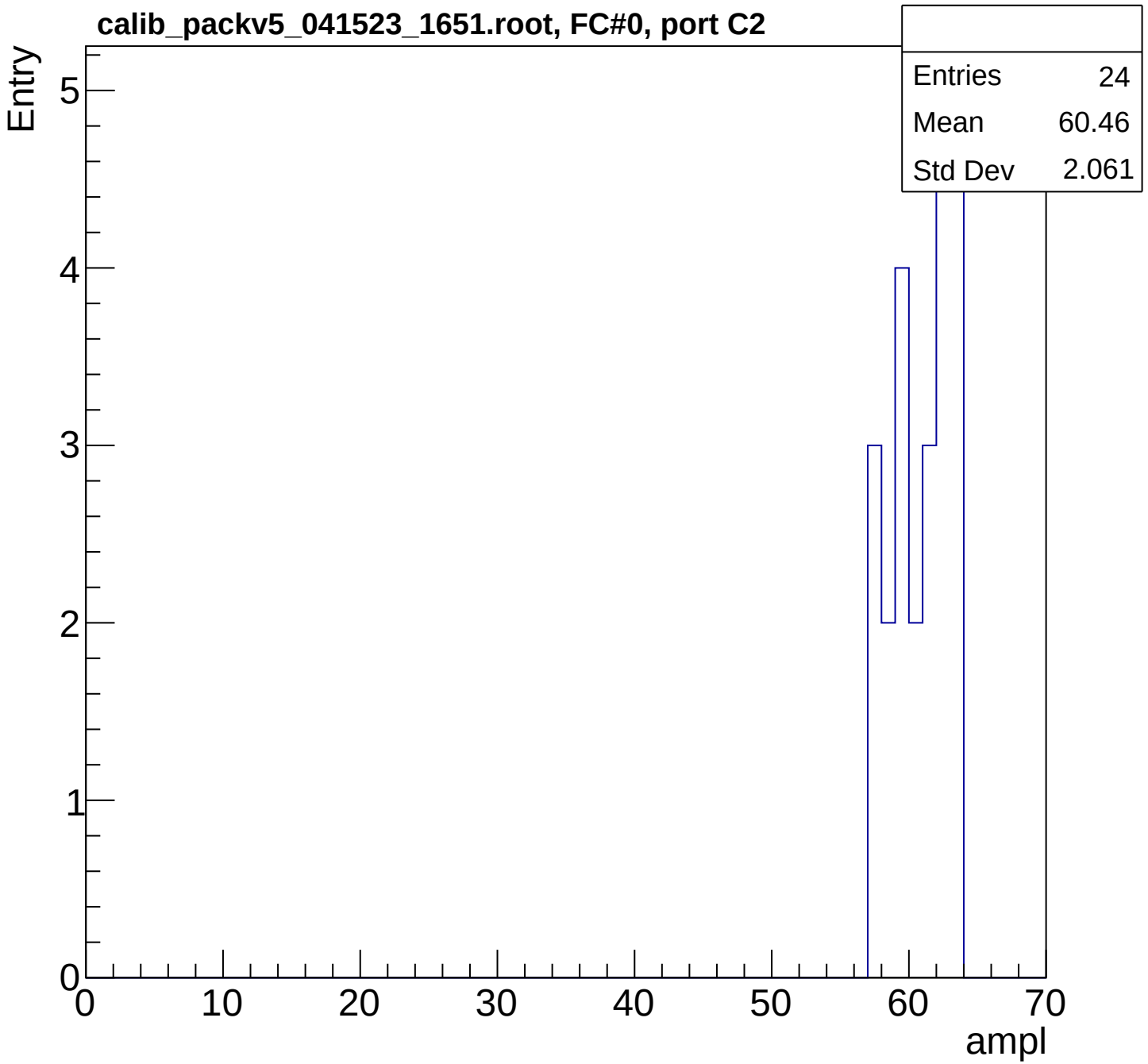

B1L103S, U2-ch85, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 30.64
Std Dev 10.8
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

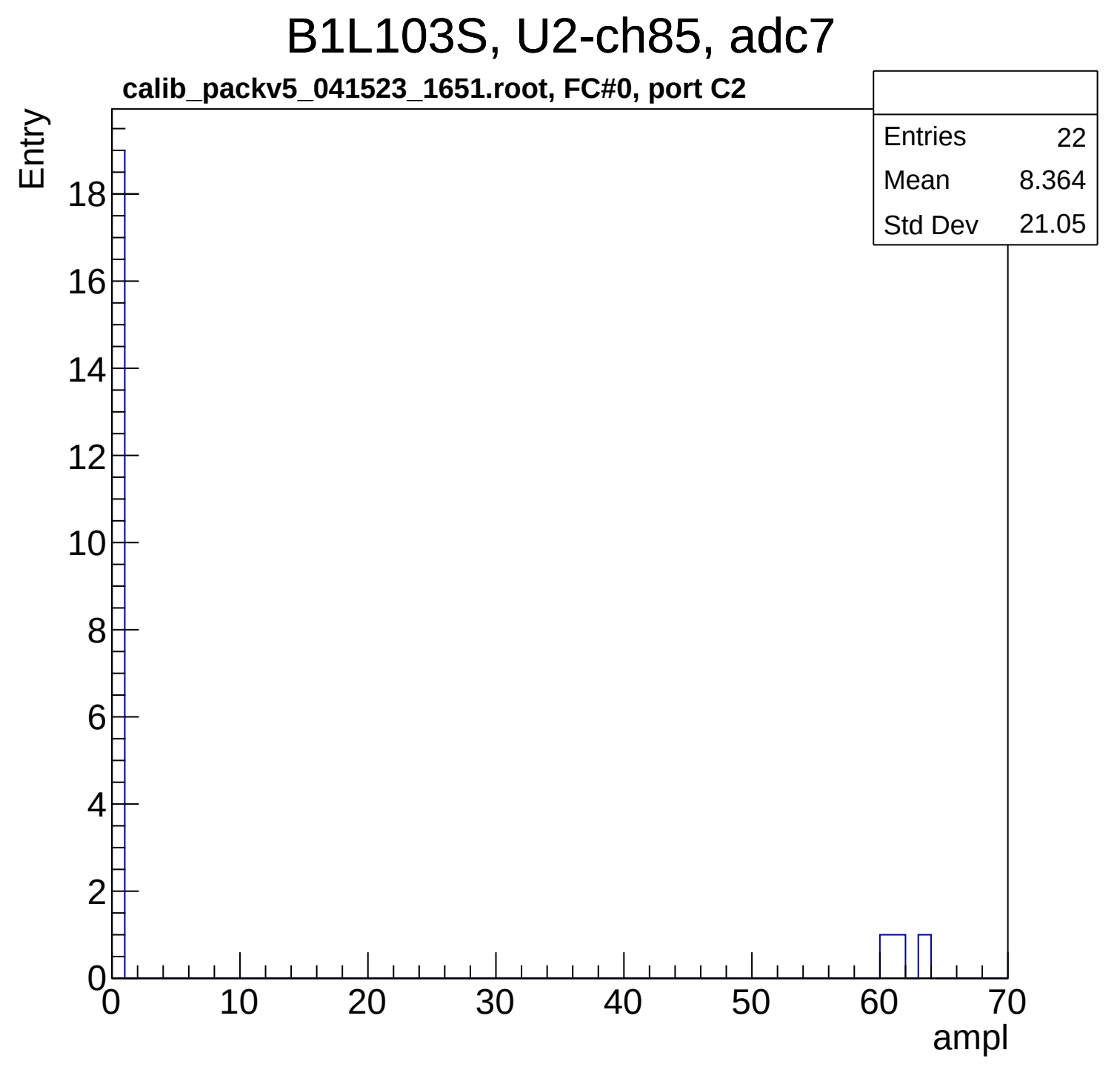

B1L103S, U2-ch85, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 36.06
Std Dev 12.77
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

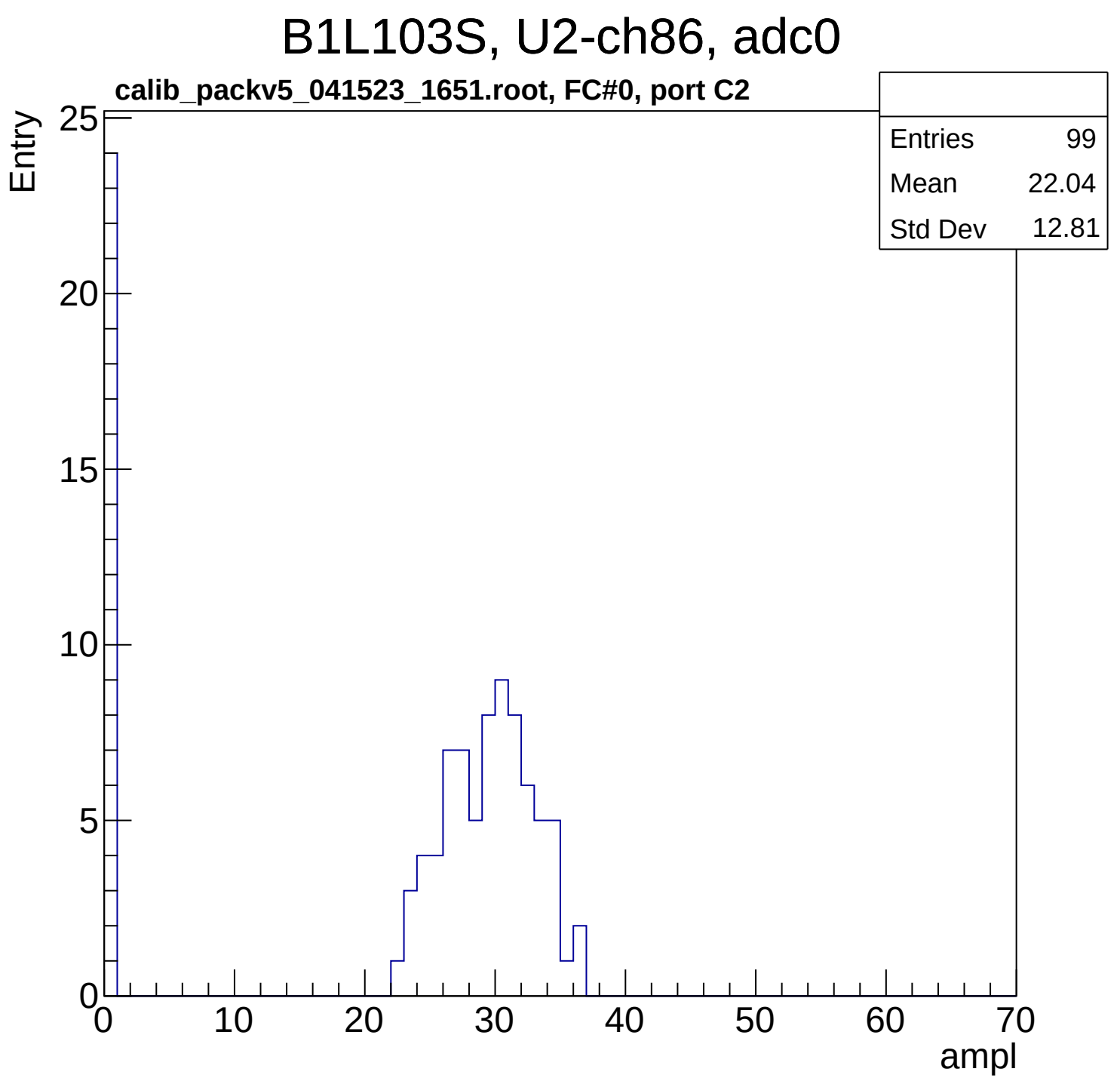

B1L103S, U2-ch85, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 45.89
Std Dev 6.419
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

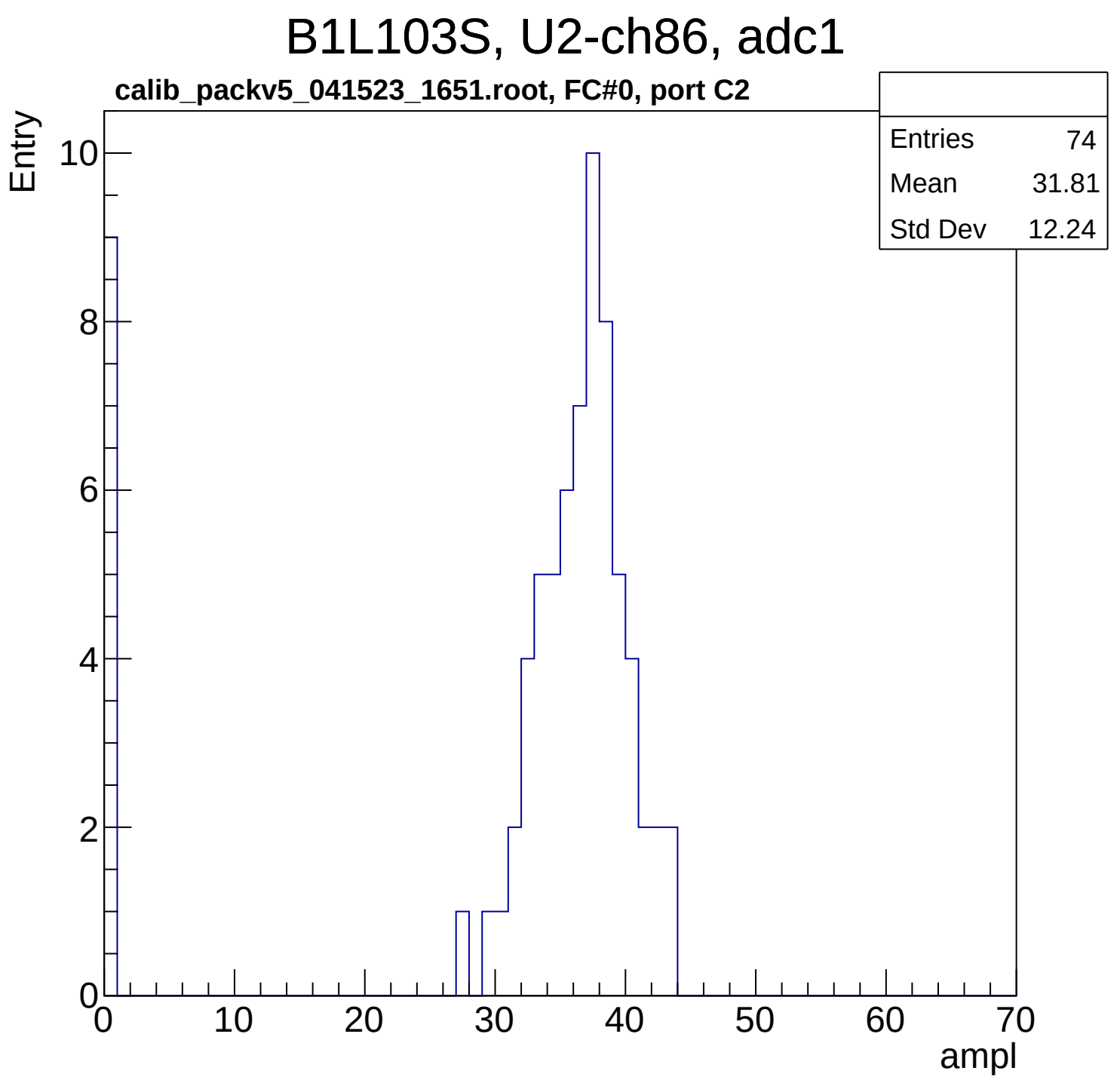

B1L103S, U2-ch85, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 53.5
Std Dev 3.202
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

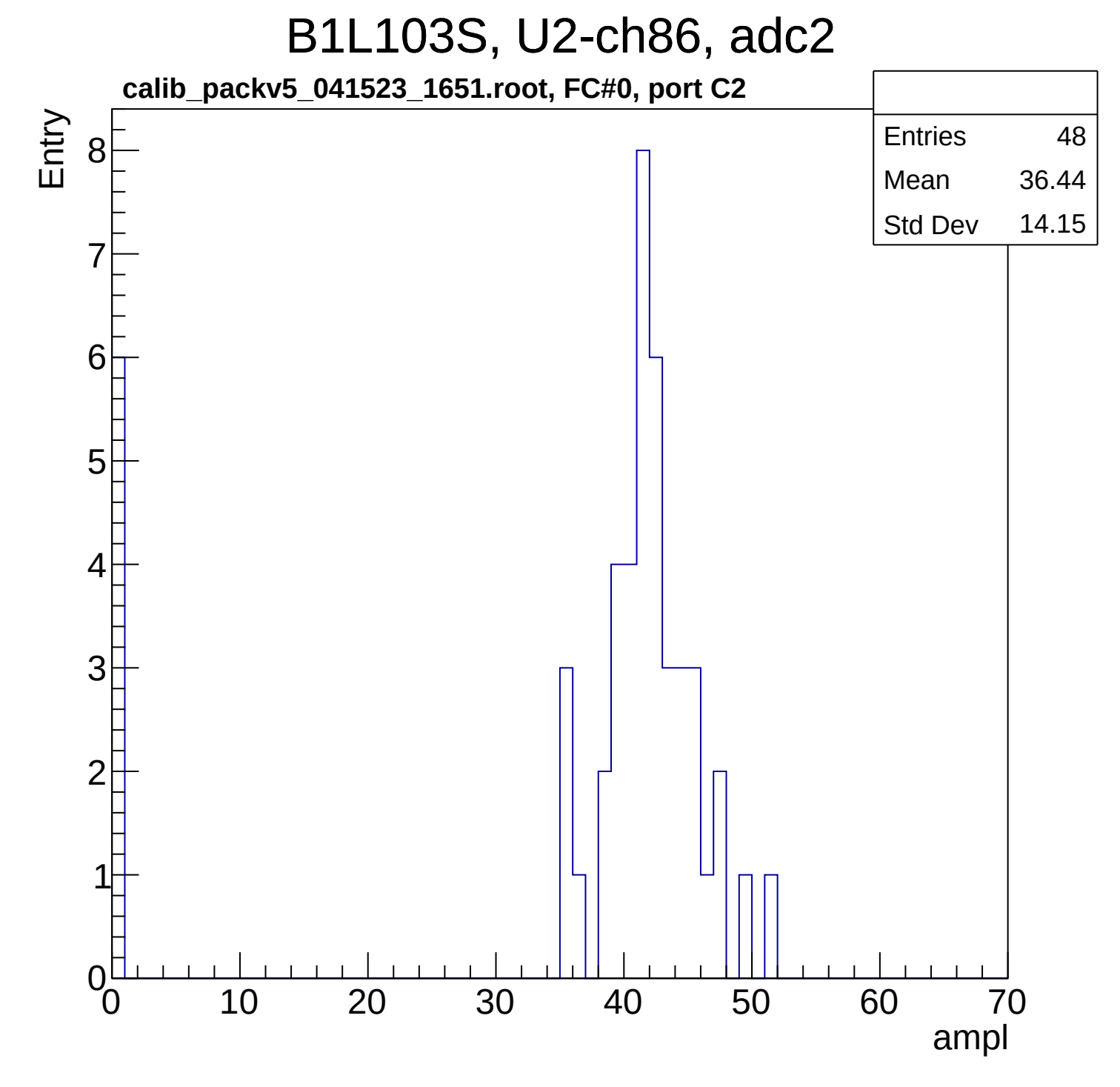

B1L103S, U2-ch85, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 56.66
Std Dev 8.229
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

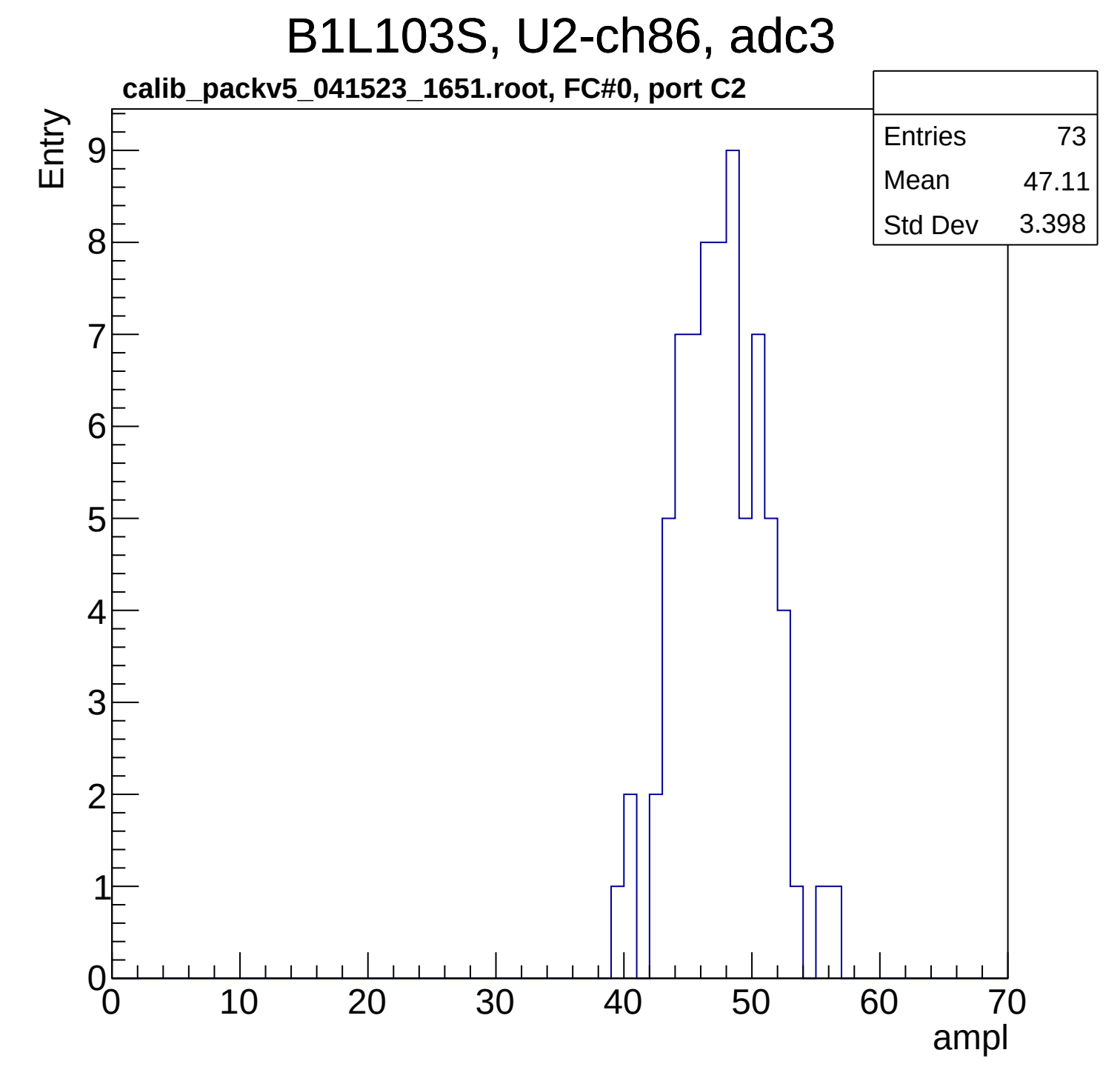

B1L103S, U2-ch85, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 60.46
Std Dev 2.061
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

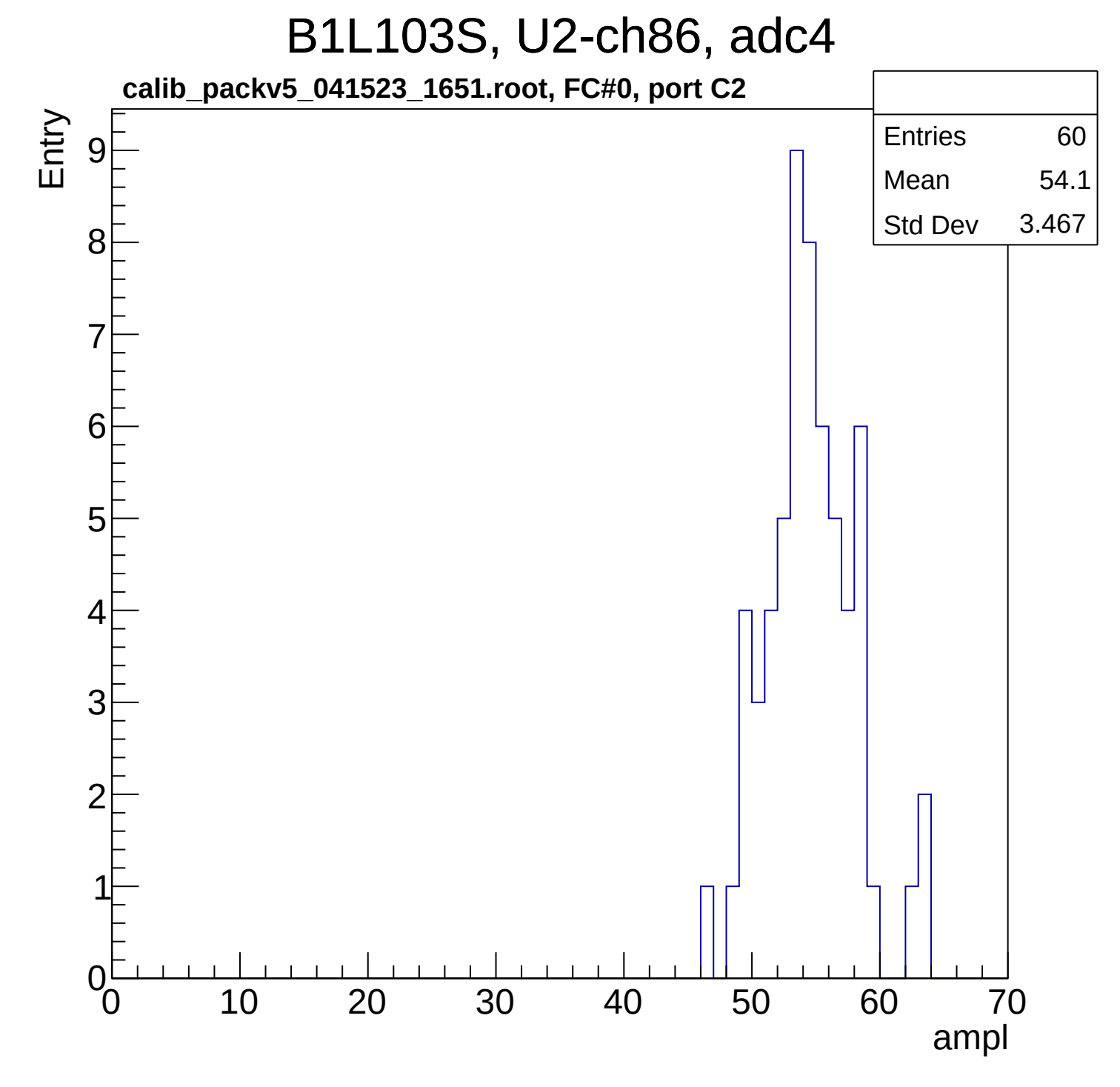

B1L103S, U2-ch85, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.364
Std Dev 21.05
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

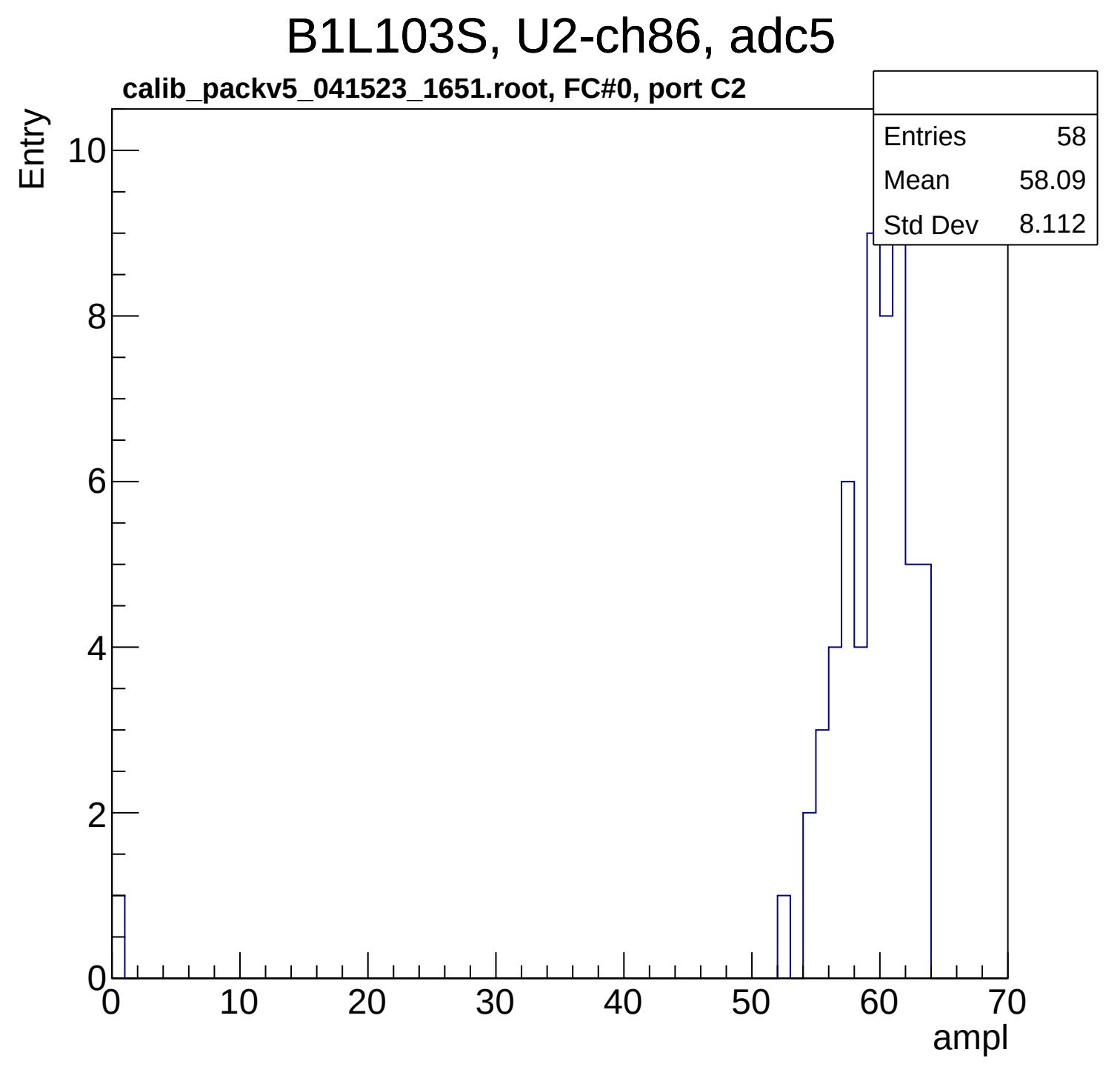

B1L103S, U2-ch86, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 22.04
Std Dev 12.81
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70

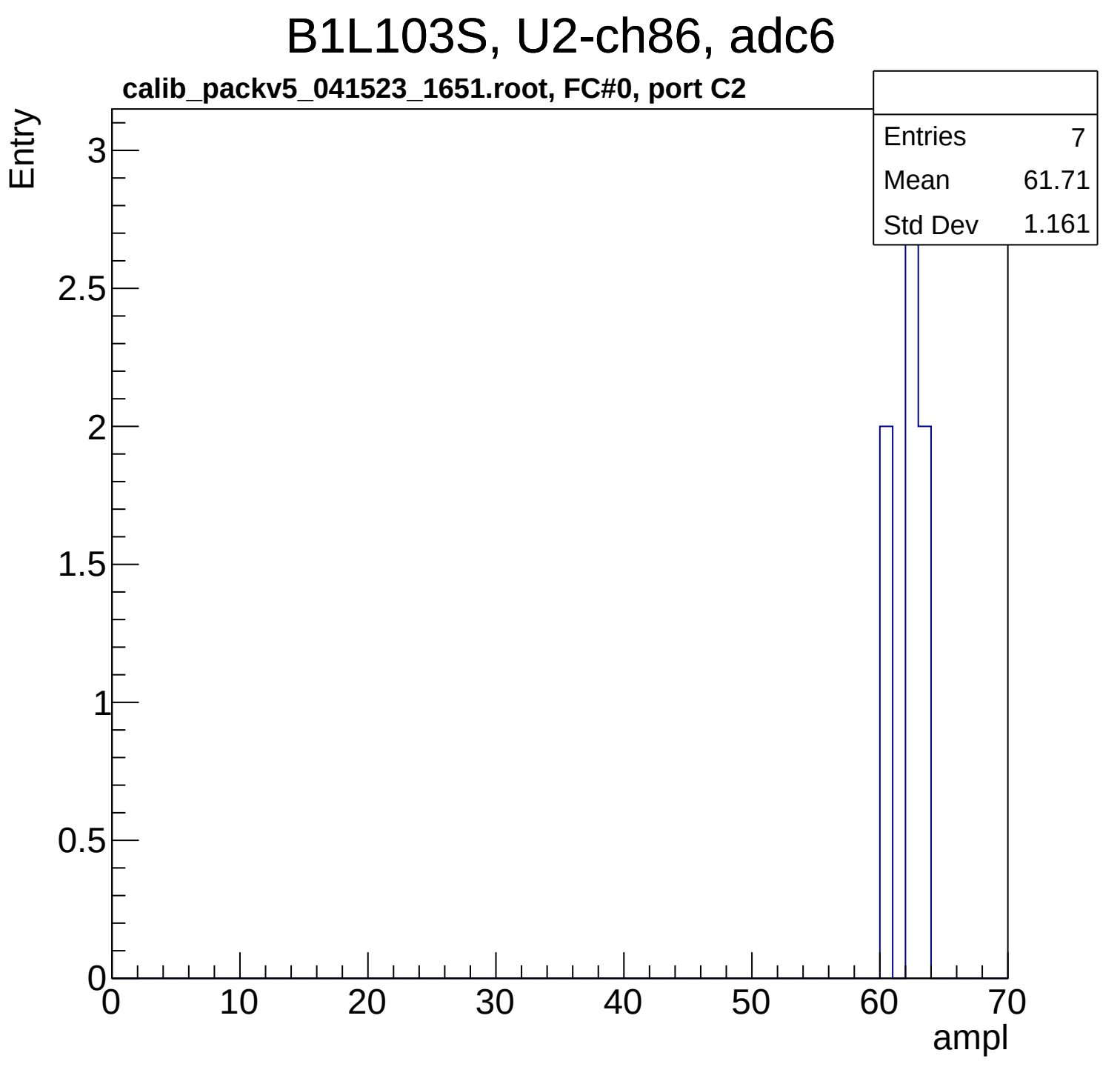

B1L103S, U2-ch86, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 31.81
Std Dev 12.24
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

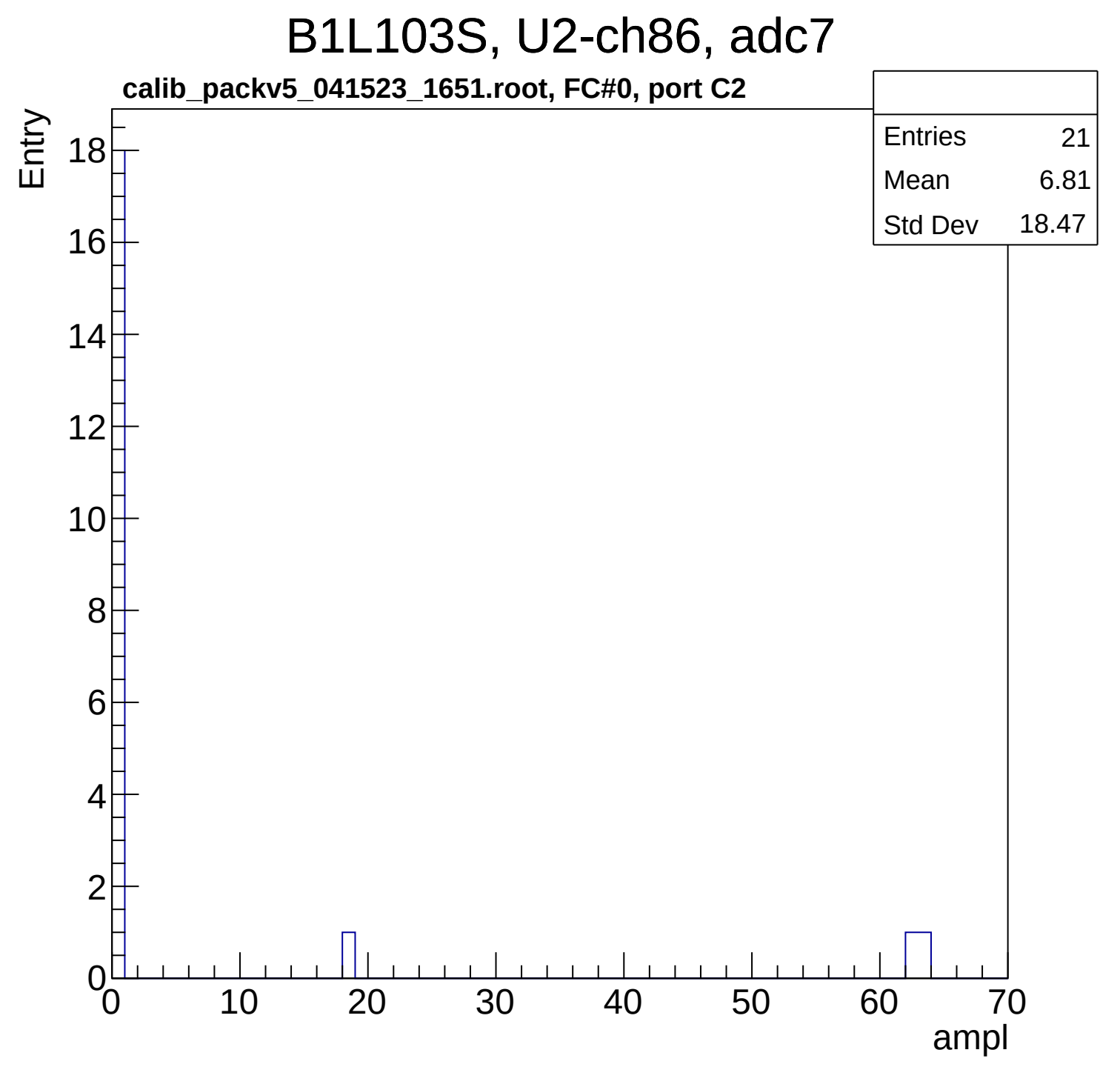

B1L103S, U2-ch86, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 36.44
Std Dev 14.15
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

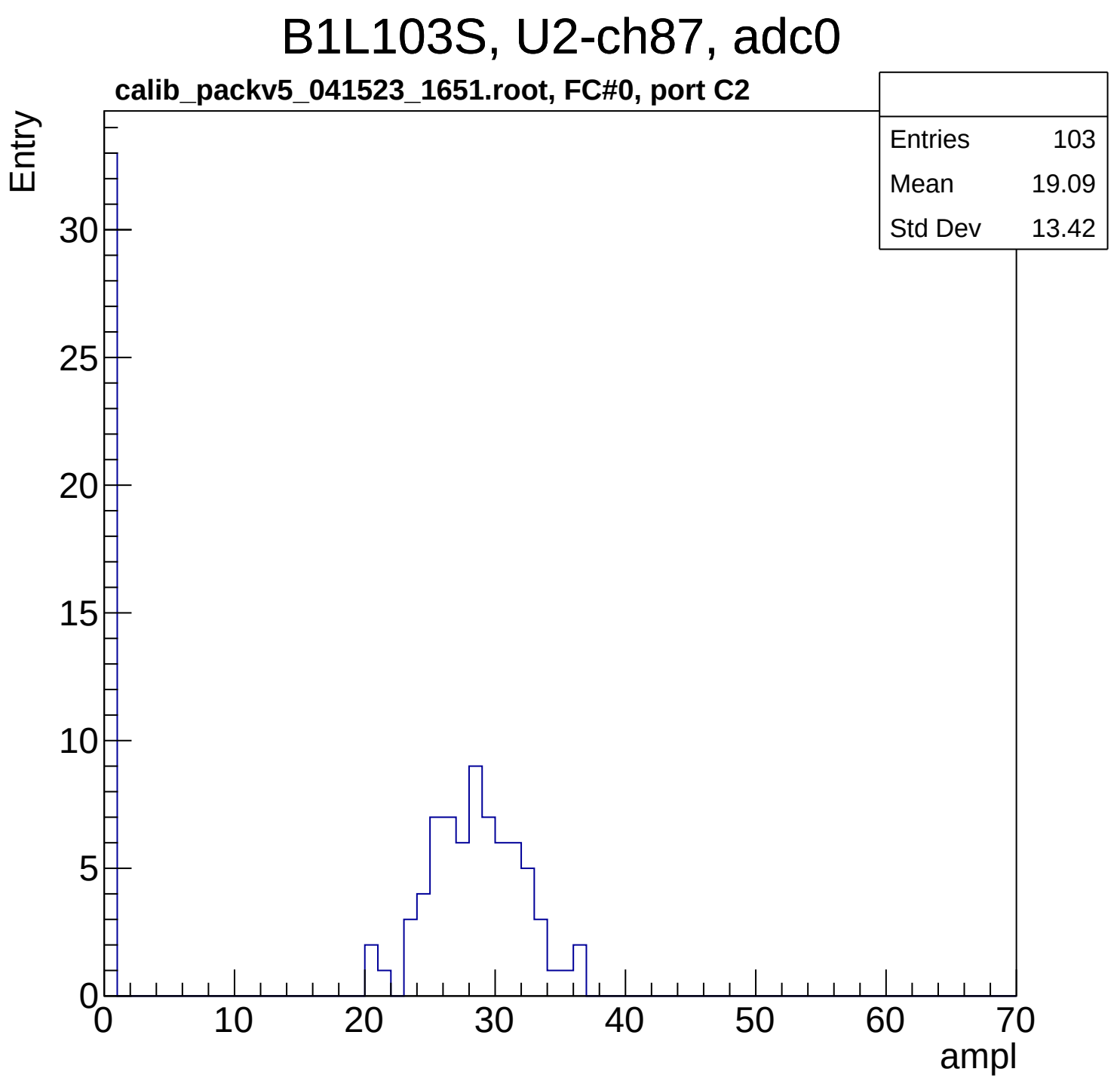

B1L103S, U2-ch86, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 47.11
Std Dev 3.398
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

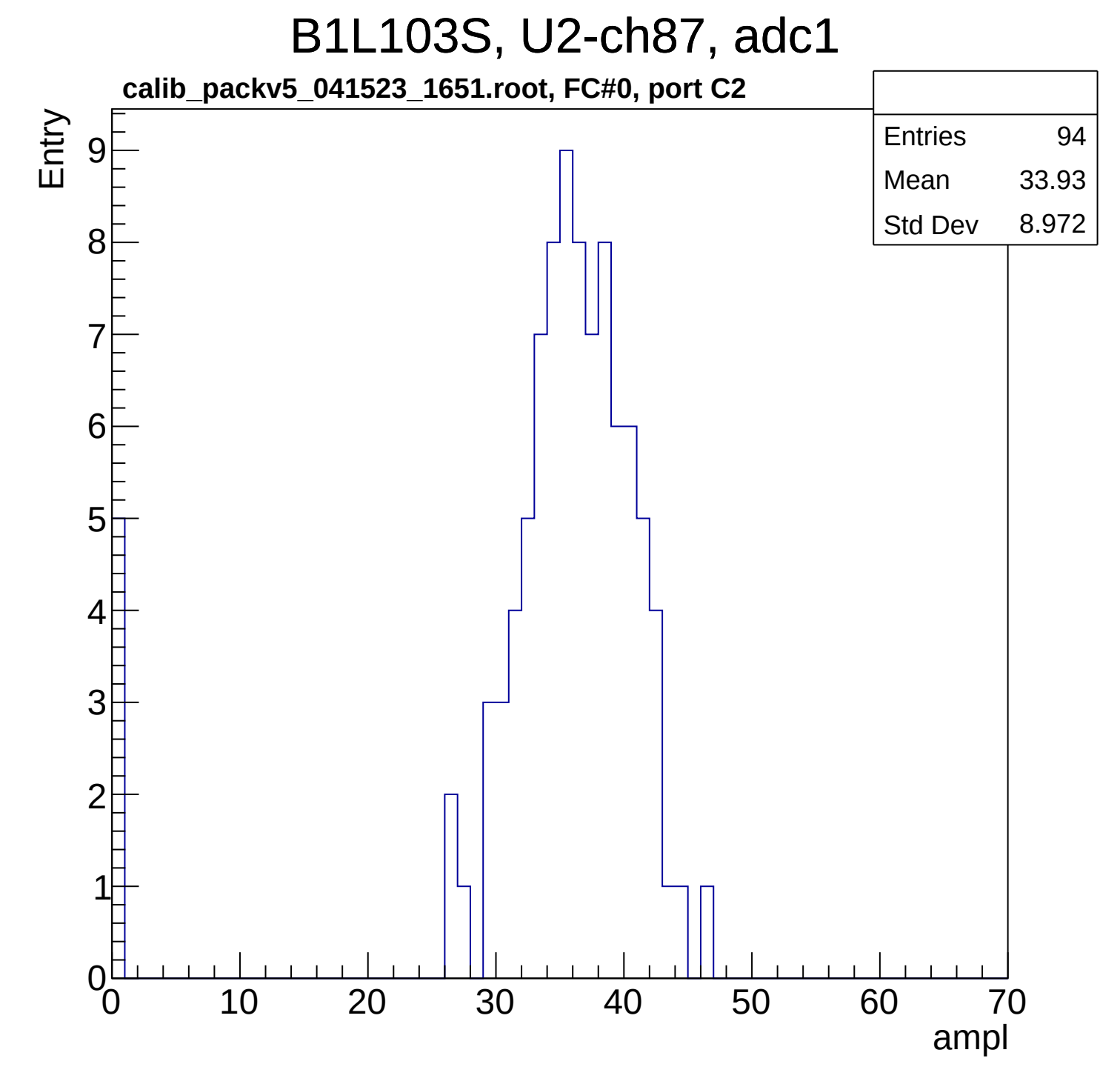

B1L103S, U2-ch86, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 54.1
Std Dev 3.467
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

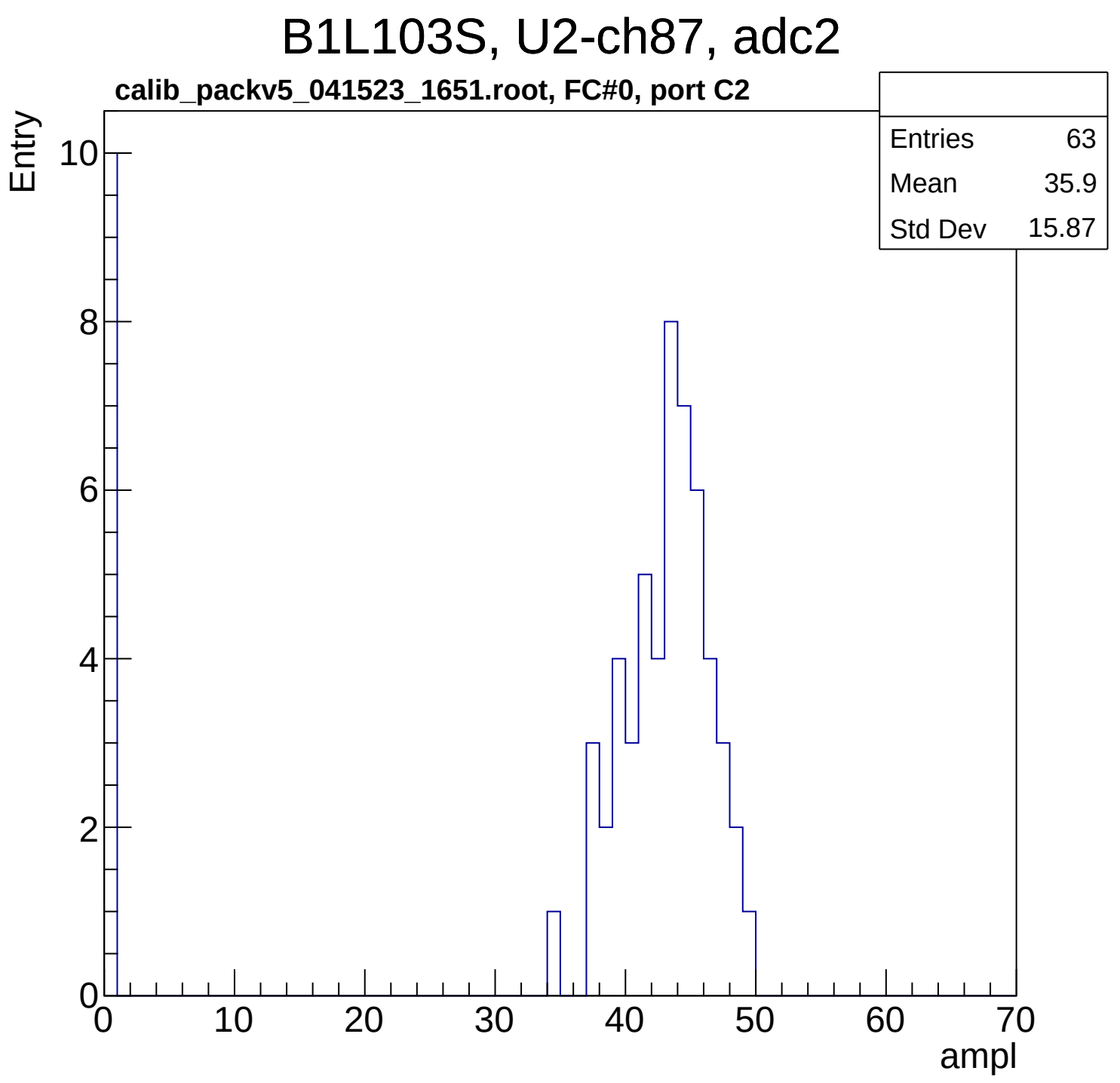

B1L103S, U2-ch86, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.09
Std Dev 8.112
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

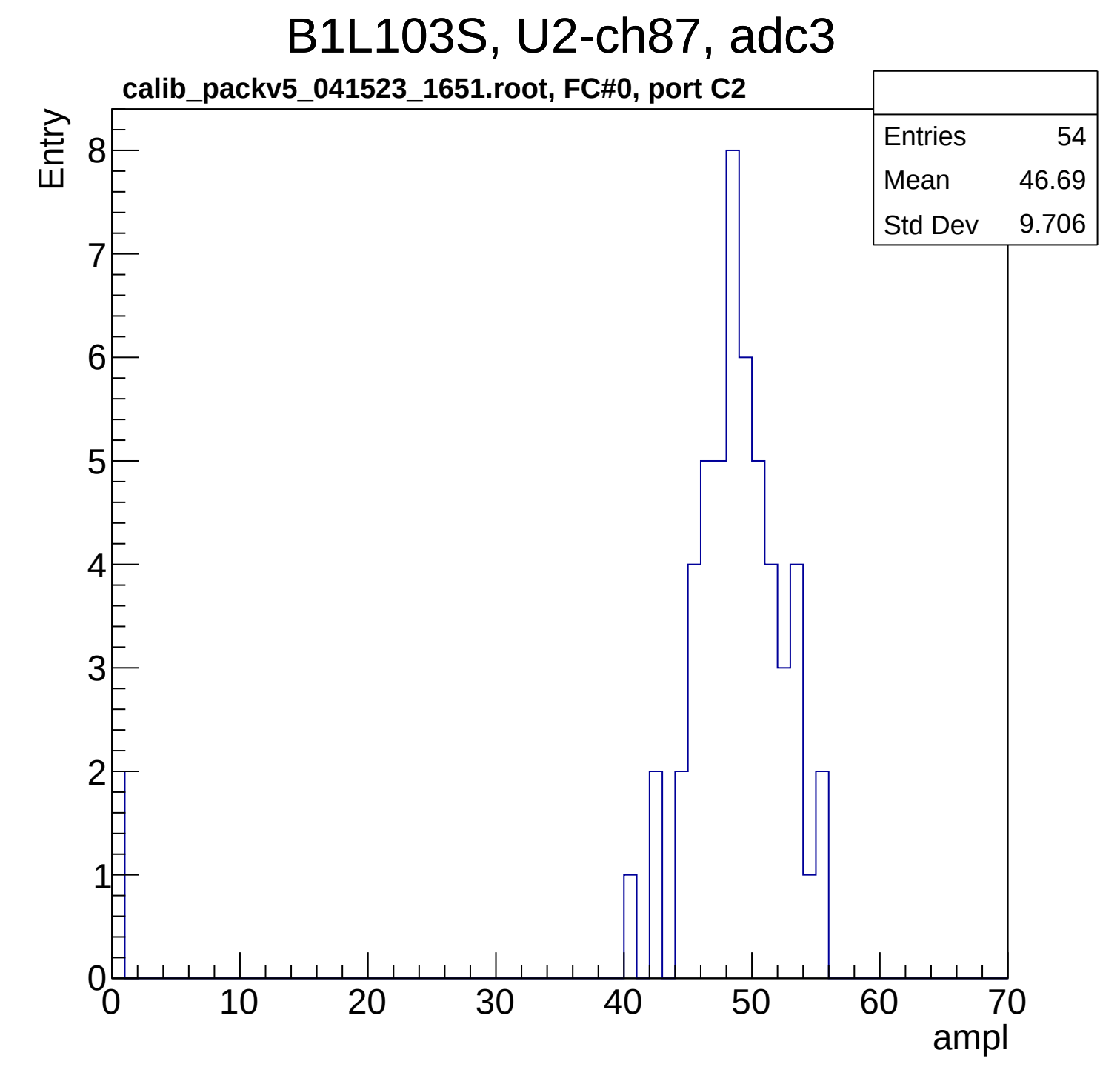

B1L103S, U2-ch86, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.71
Std Dev 1.161
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

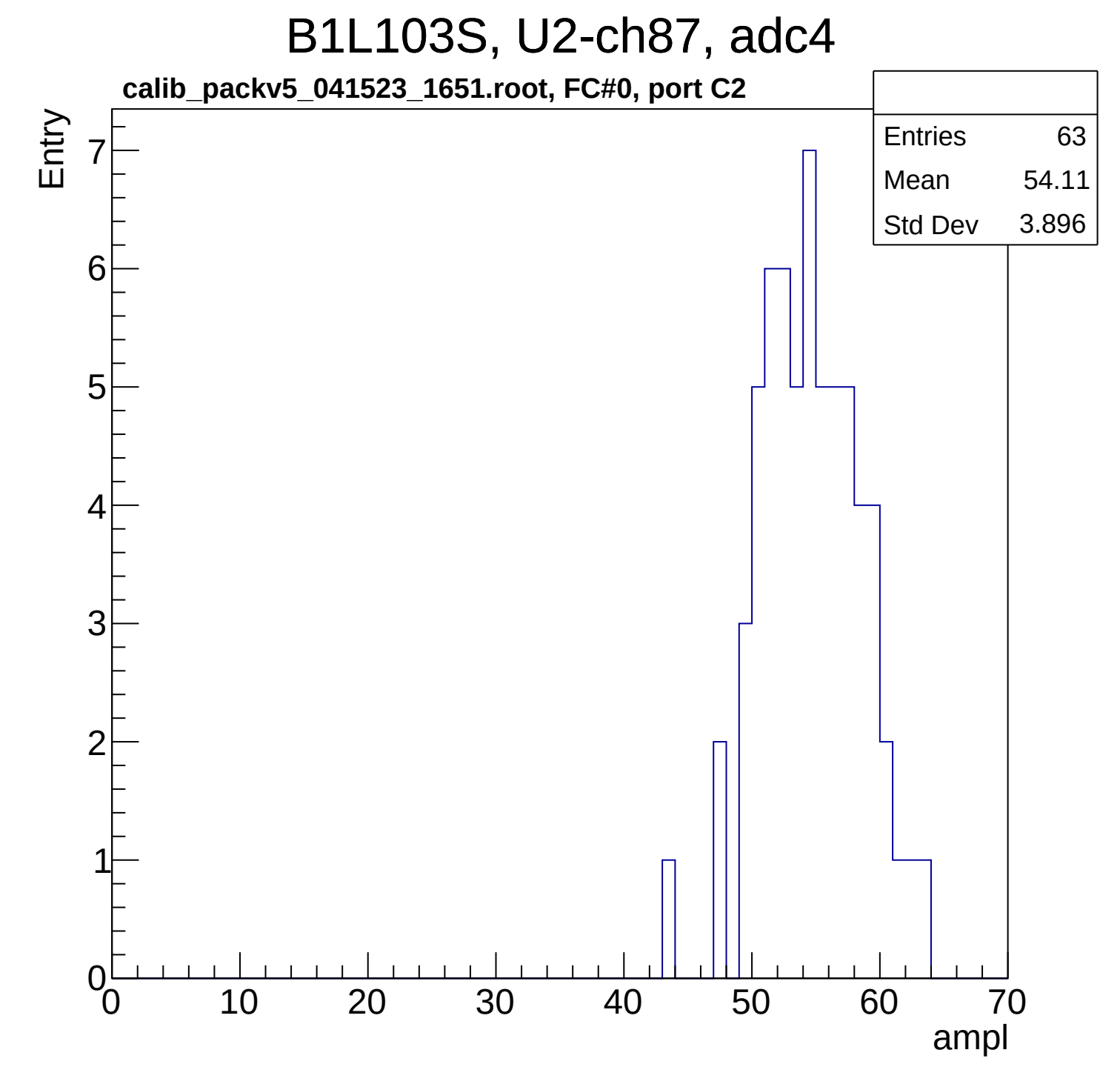

B1L103S, U2-ch86, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6.81
Std Dev 18.47
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

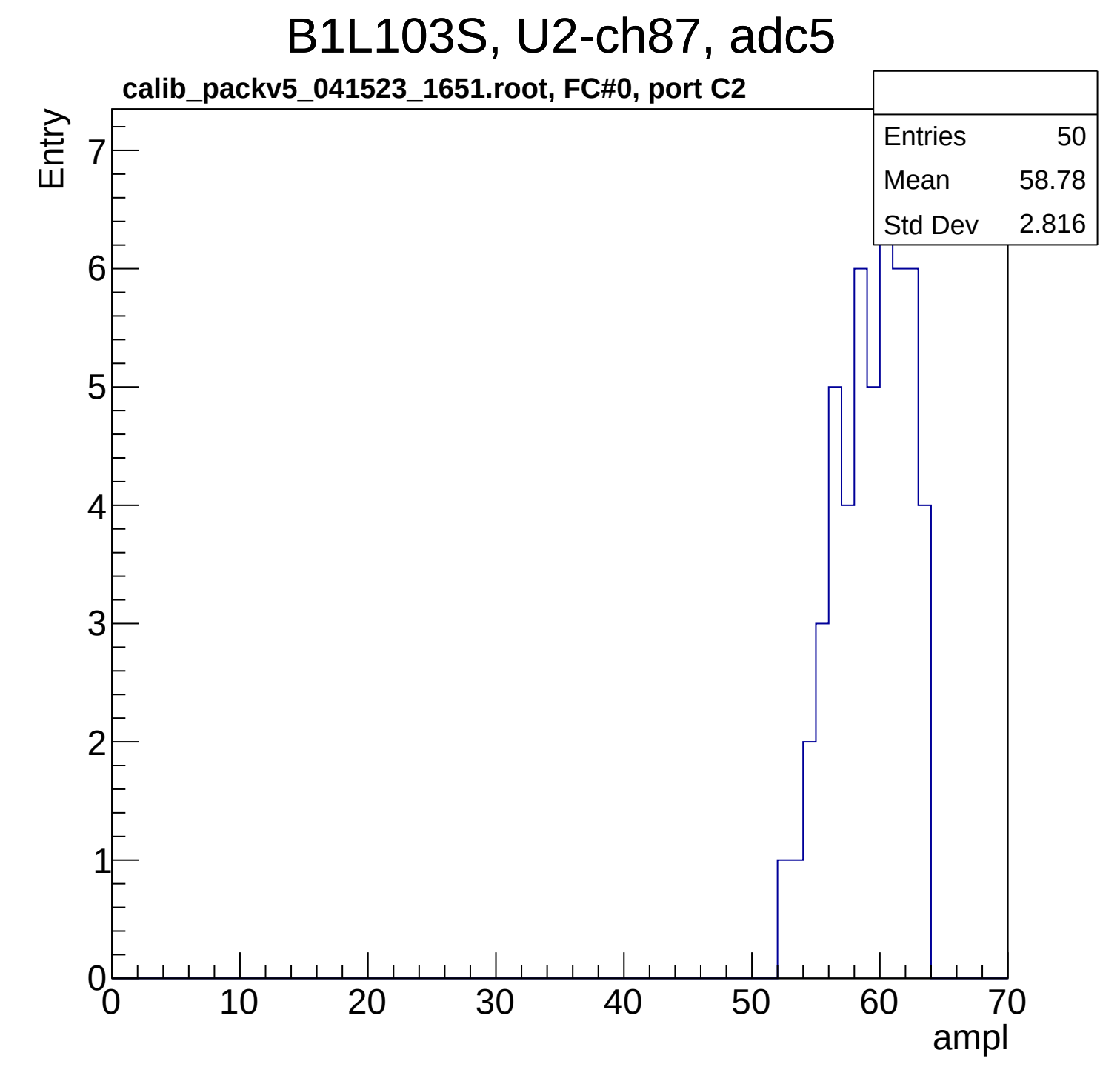

B1L103S, U2-ch87, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 19.09
Std Dev 13.42
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl

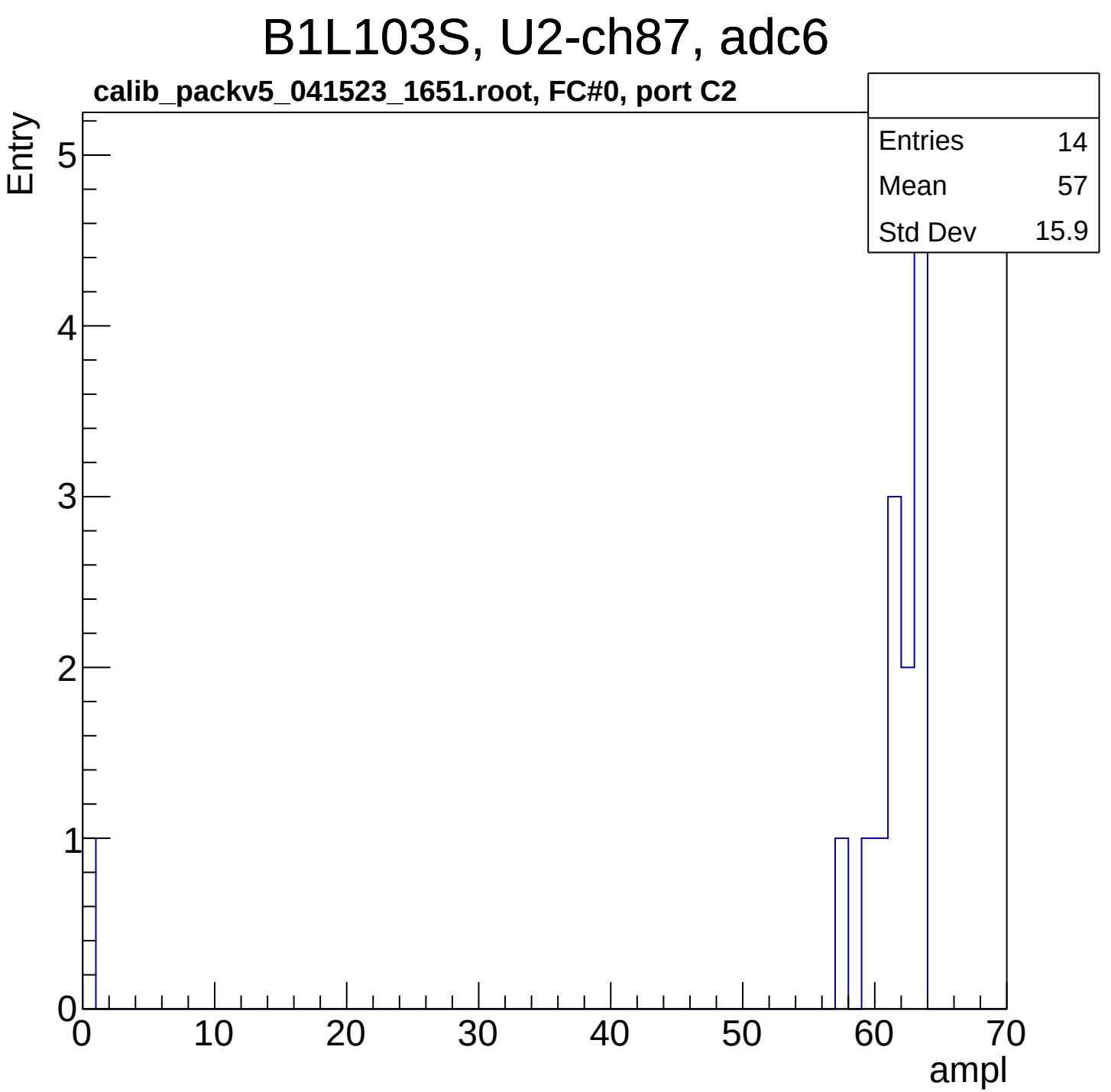

B1L103S, U2-ch87, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 33.93
Std Dev 8.972
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

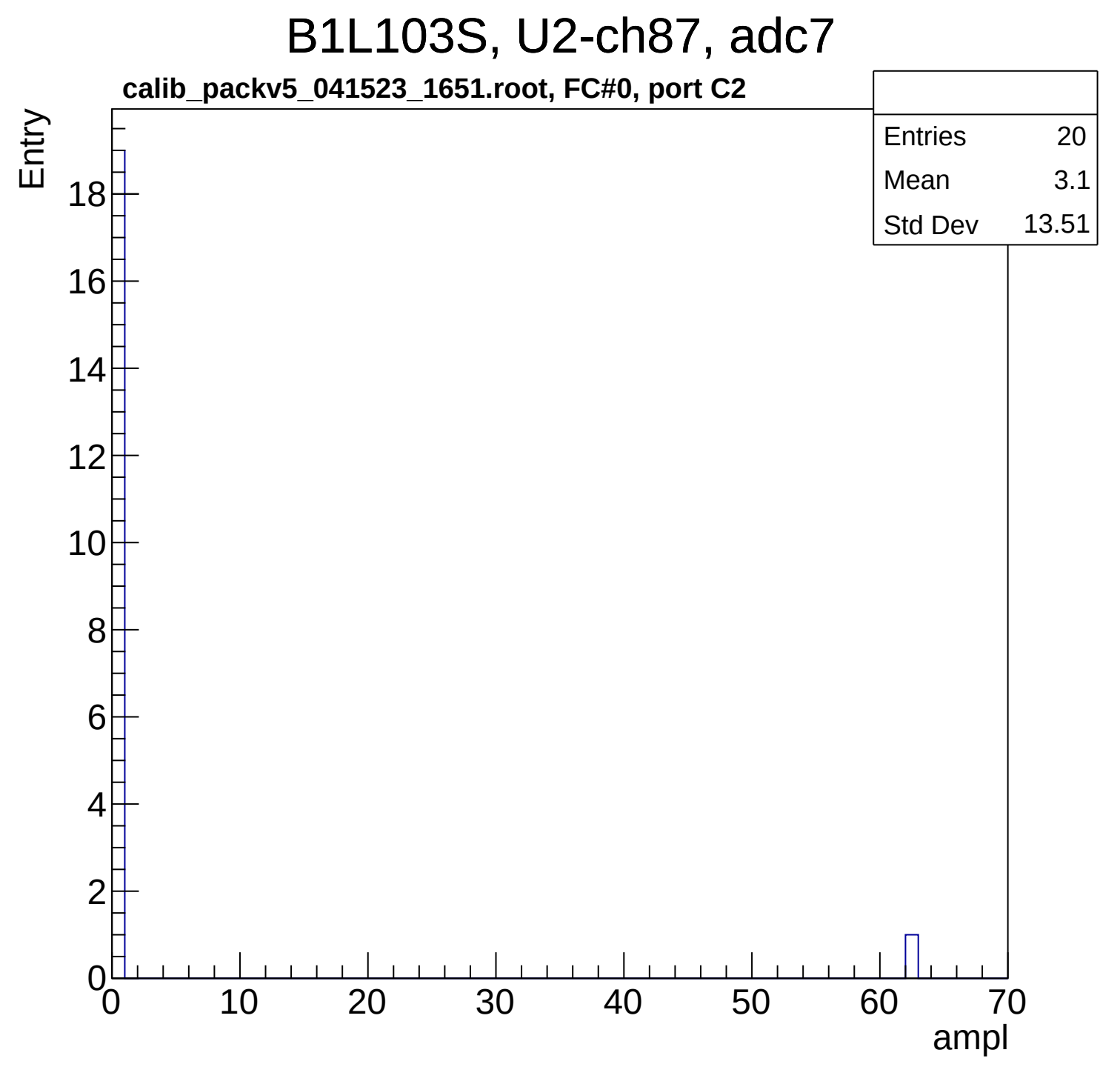

B1L103S, U2-ch87, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 35.9
Std Dev 15.87
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

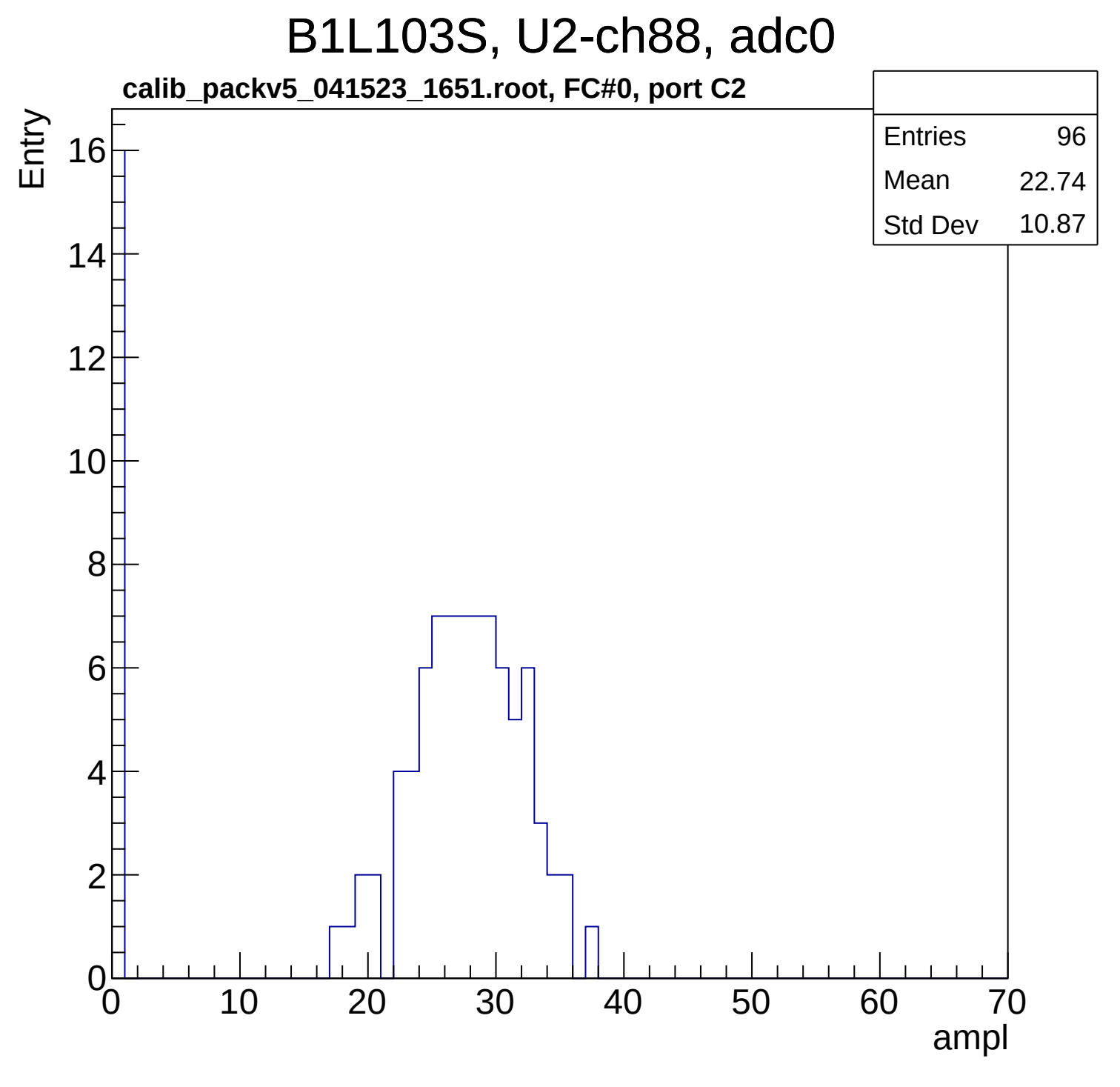

B1L103S, U2-ch87, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 46.69
Std Dev 9.706
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

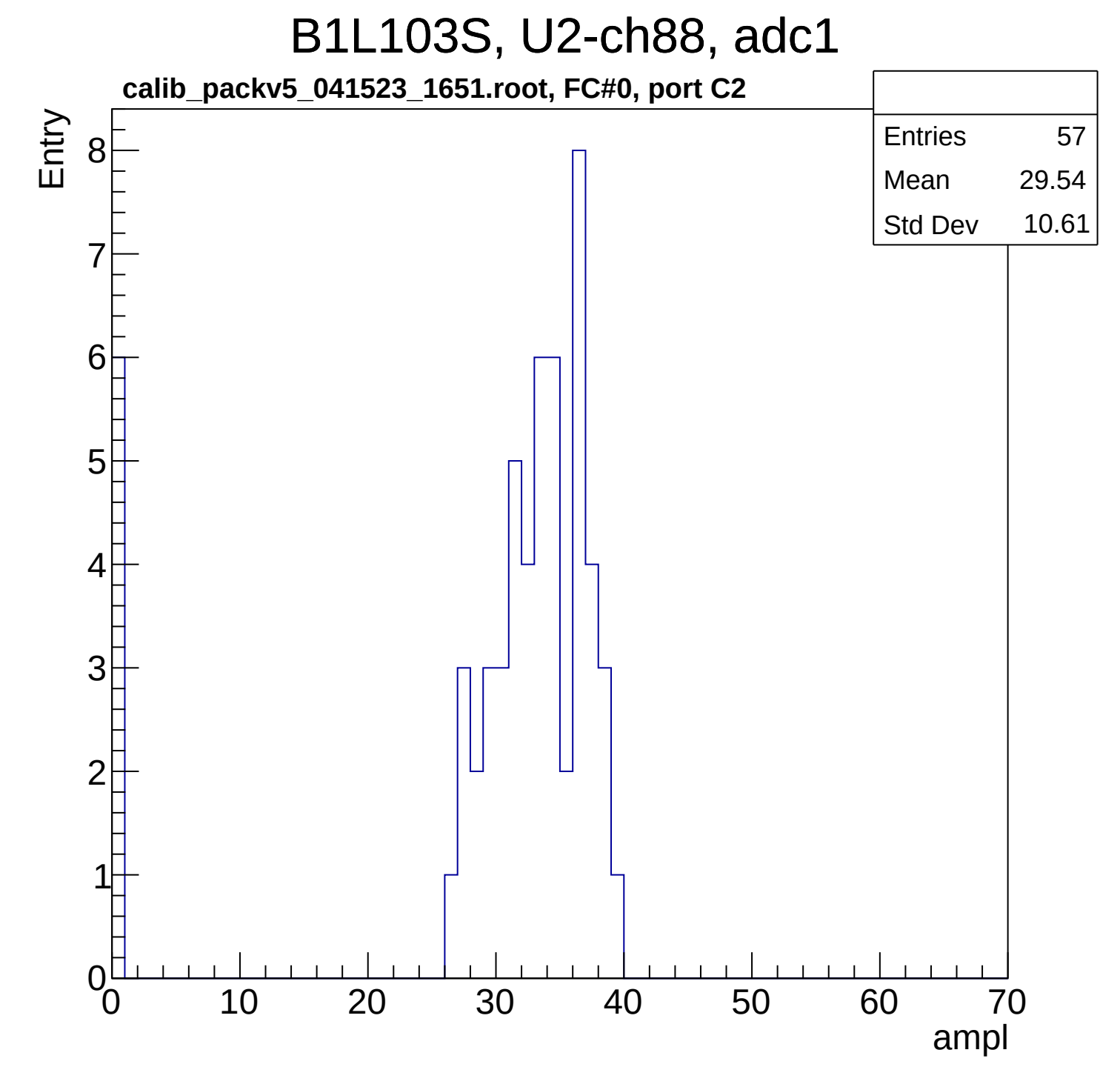

B1L103S, U2-ch87, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 54.11
Std Dev 3.896
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

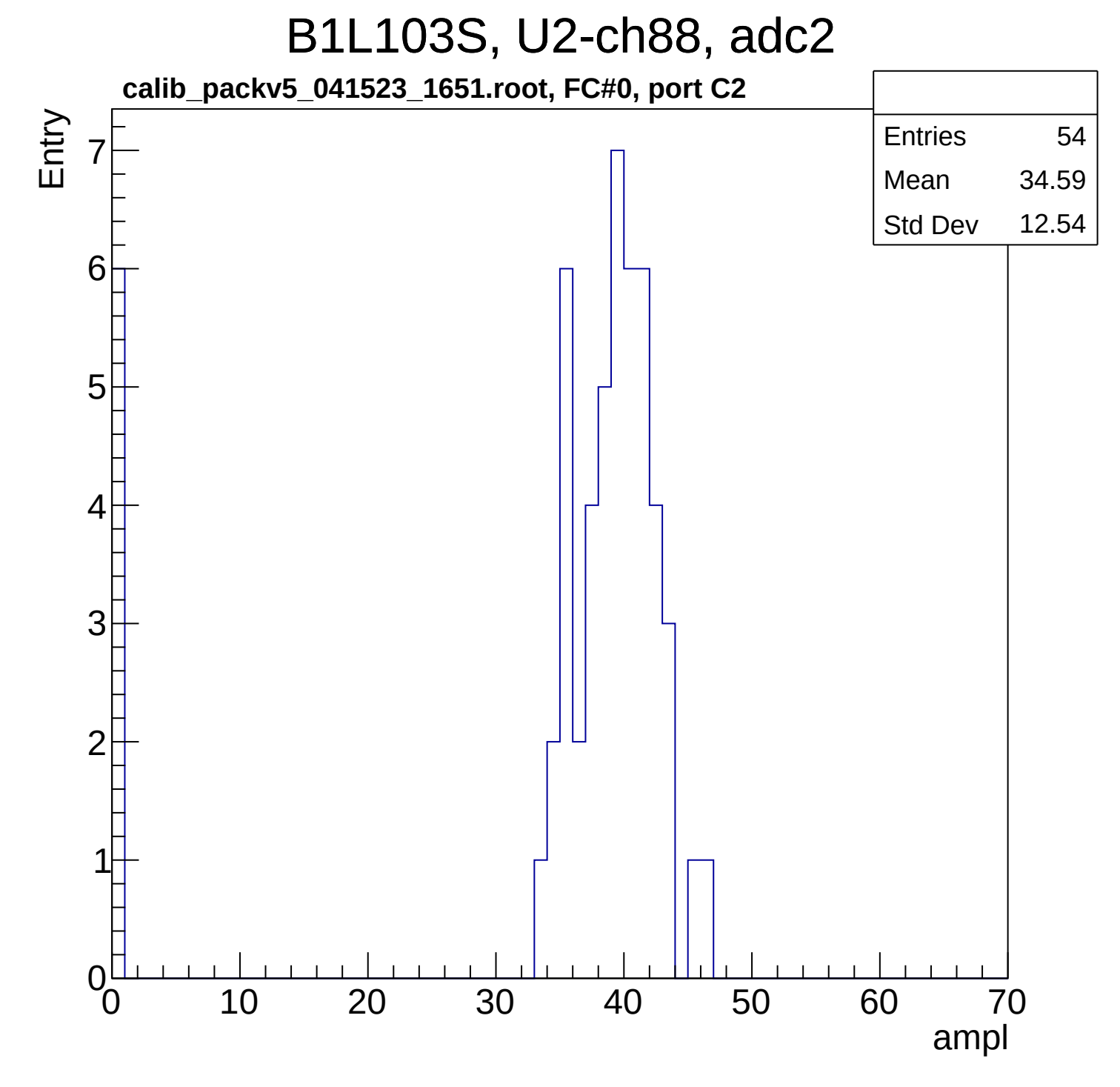

B1L103S, U2-ch87, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.78
Std Dev 2.816
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

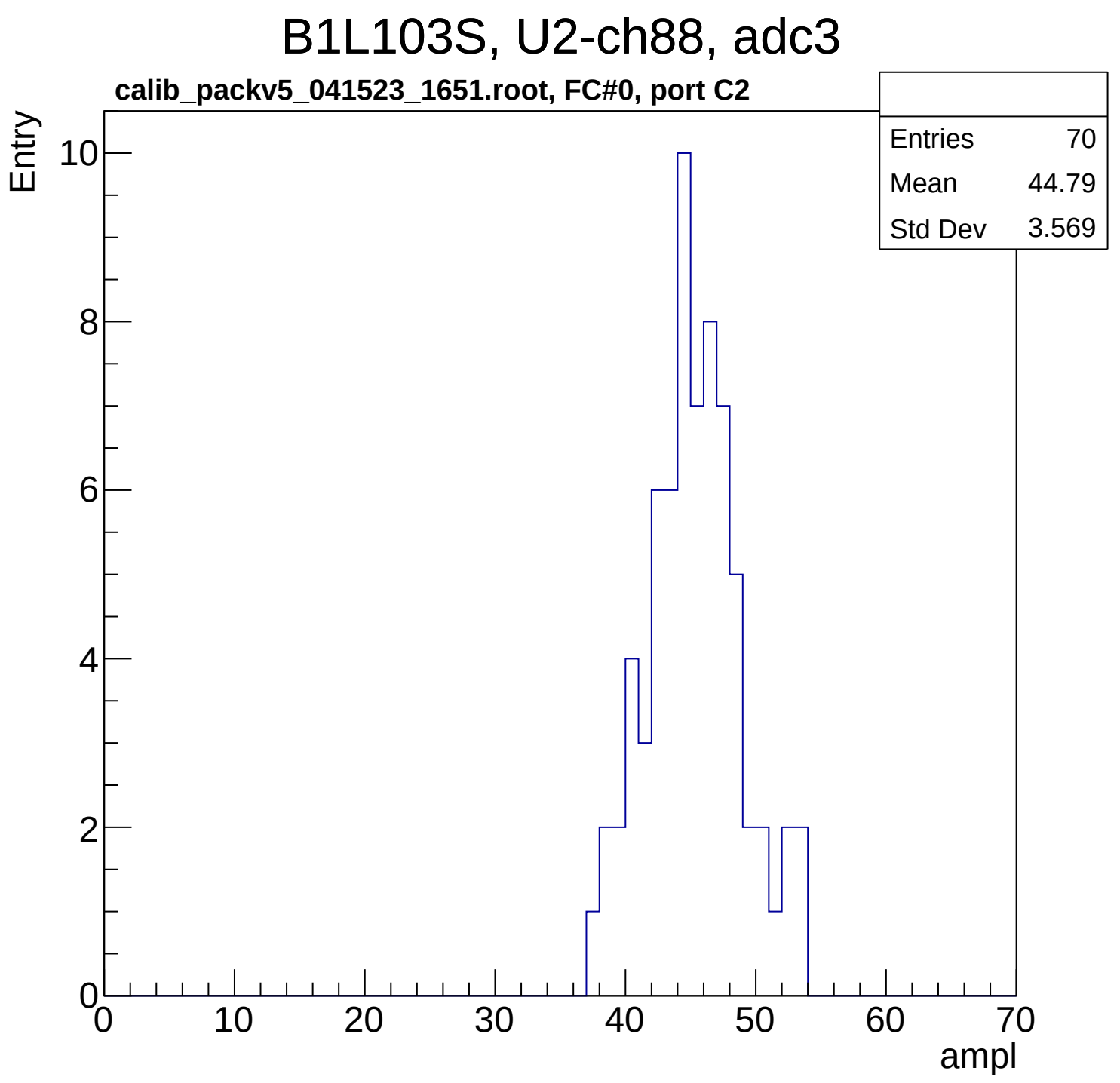

B1L103S, U2-ch87, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 57
Std Dev 15.9
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

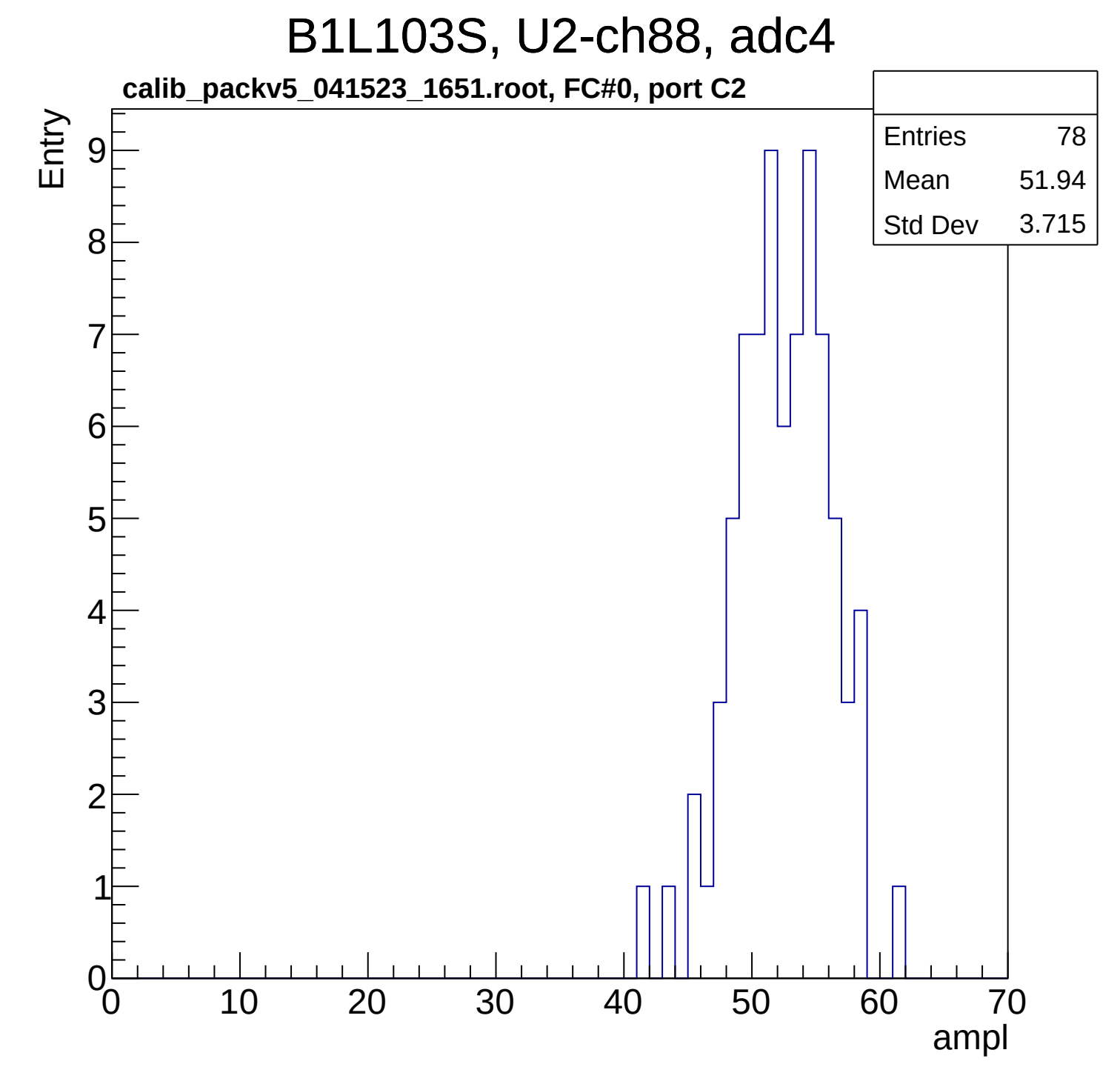

B1L103S, U2-ch87, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

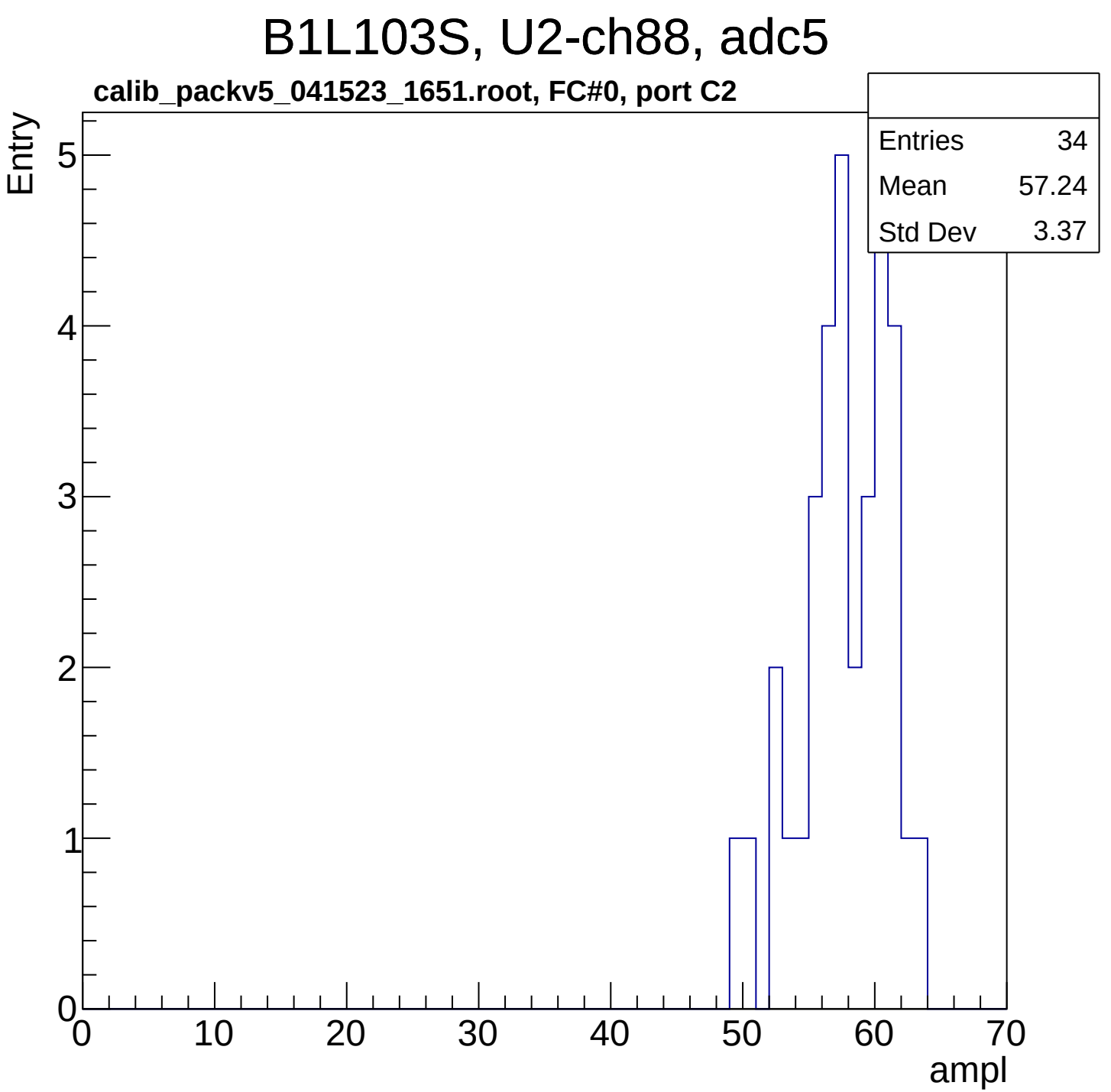

B1L103S, U2-ch88, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 22.74
Std Dev 10.87
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

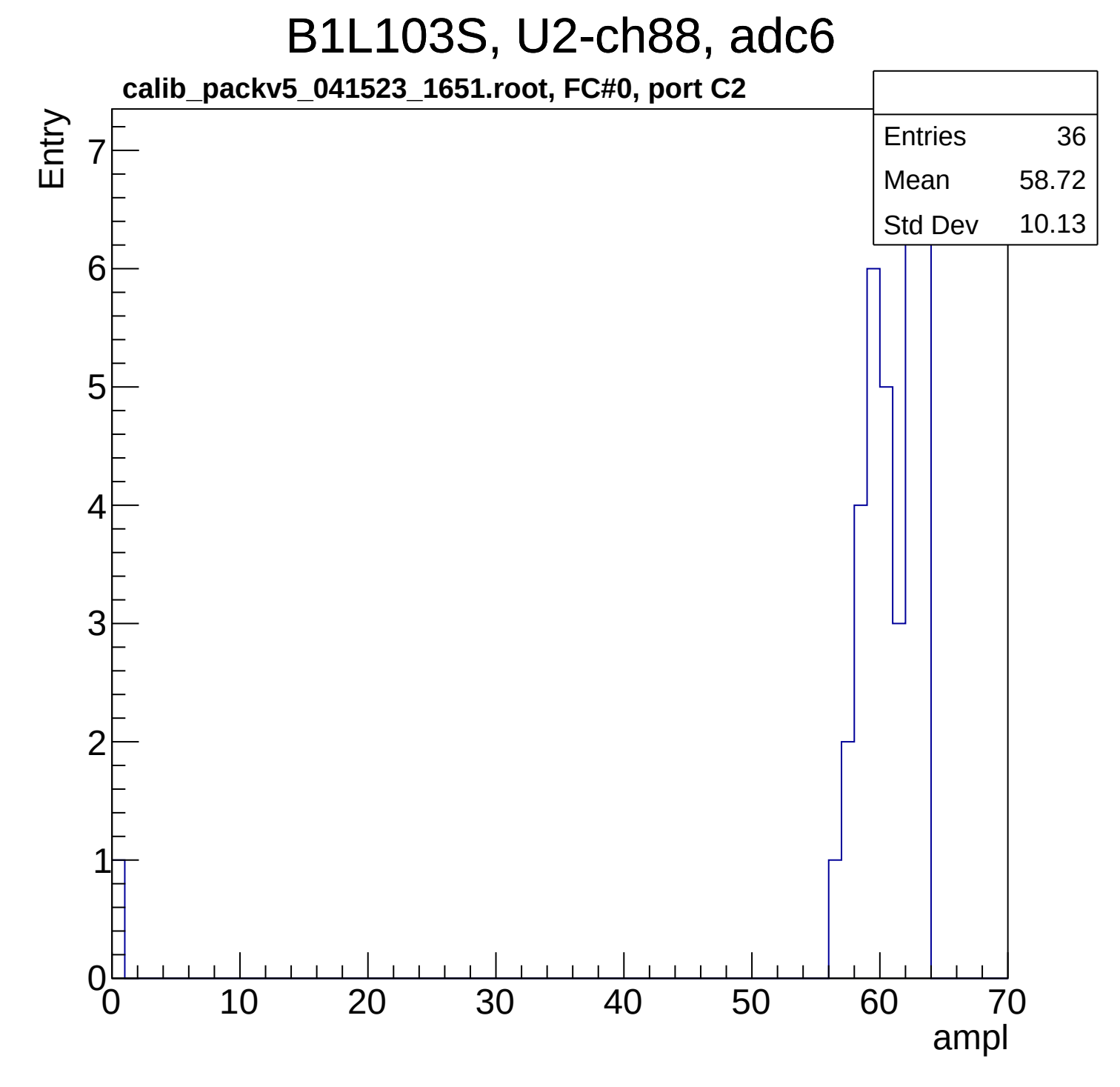

B1L103S, U2-ch88, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 29.54
Std Dev 10.61
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

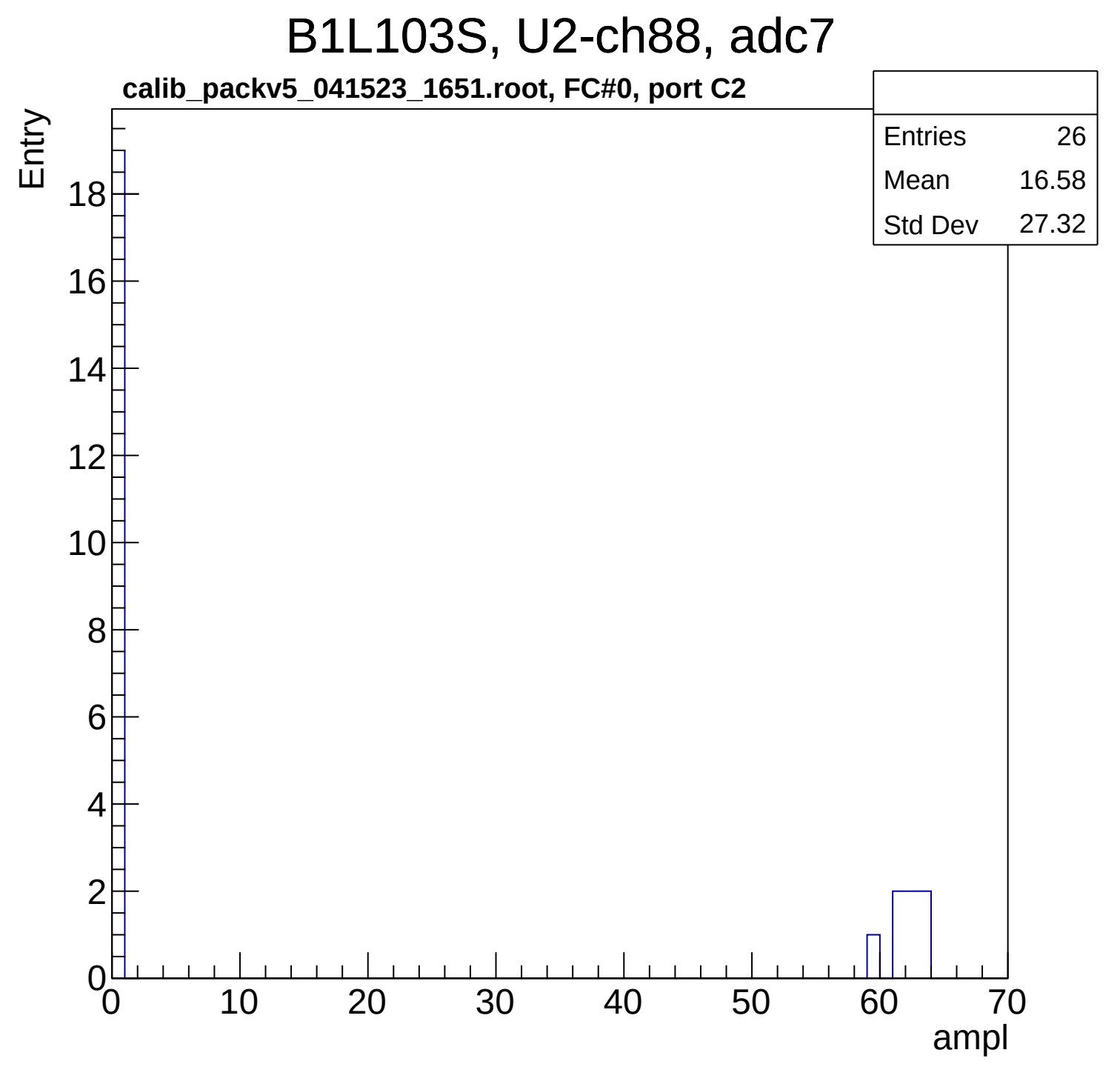

B1L103S, U2-ch88, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 34.59
Std Dev 12.54
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

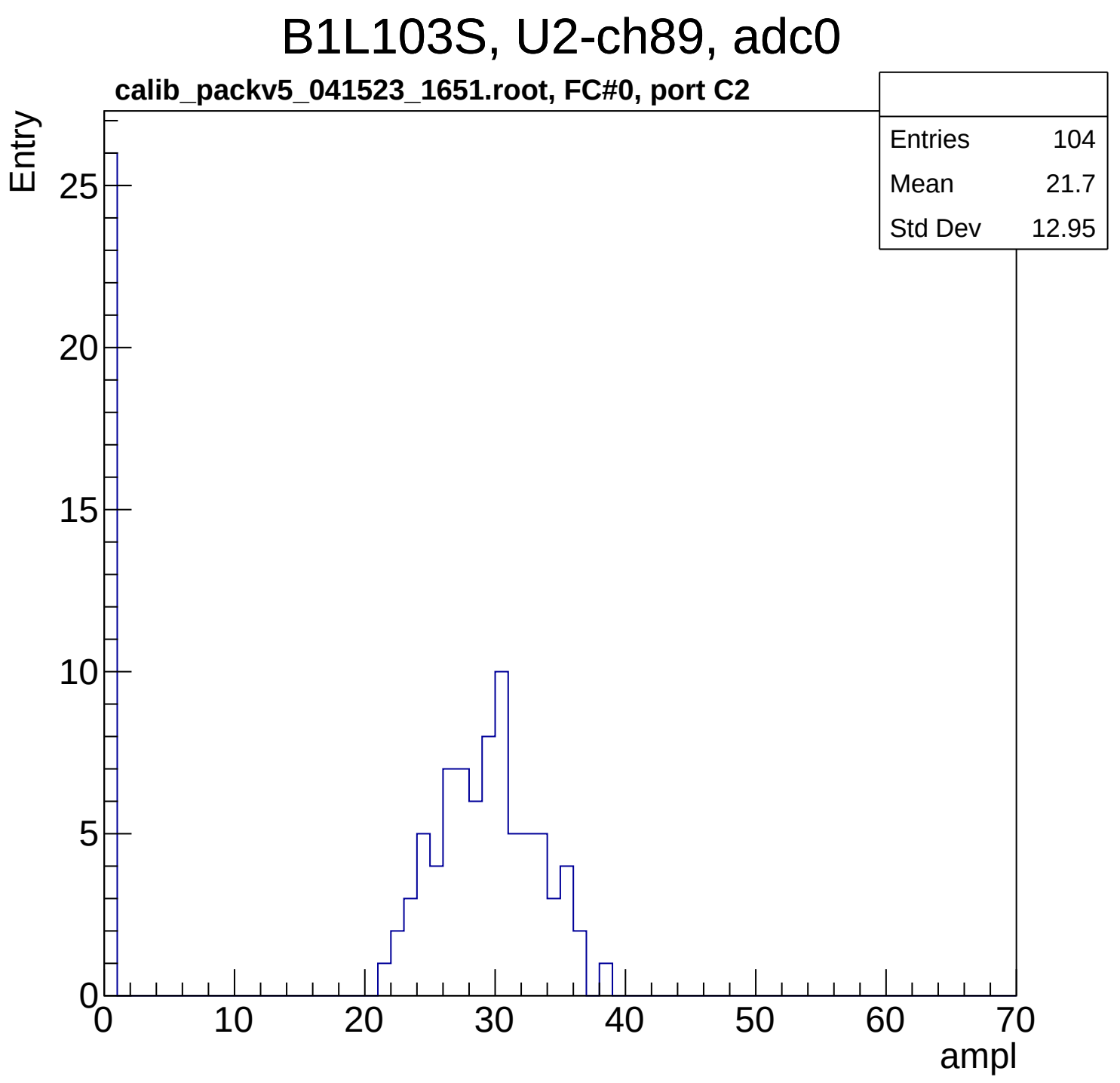

B1L103S, U2-ch88, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 44.79
Std Dev 3.569
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

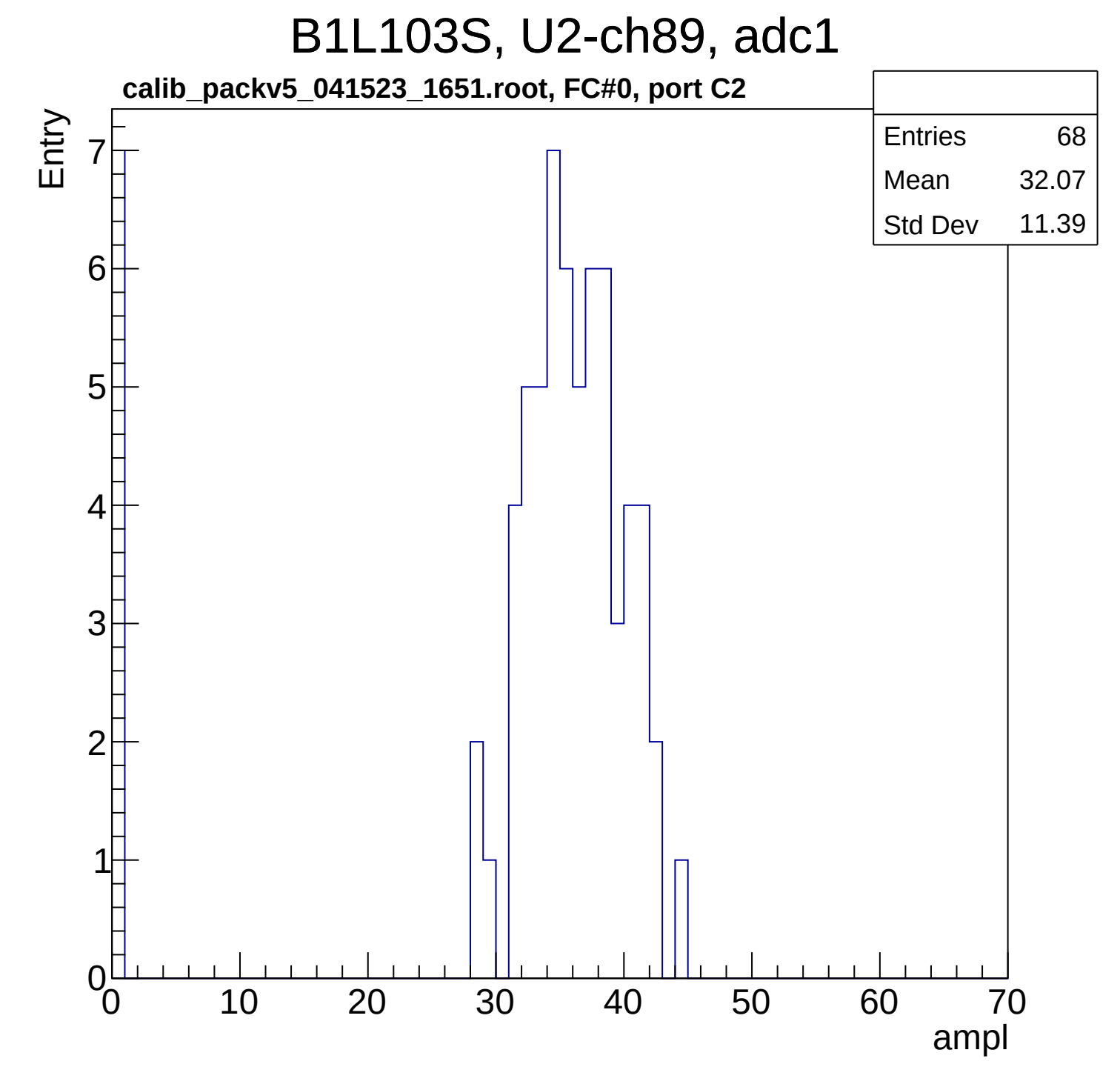

B1L103S, U2-ch88, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 51.94
Std Dev 3.715
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

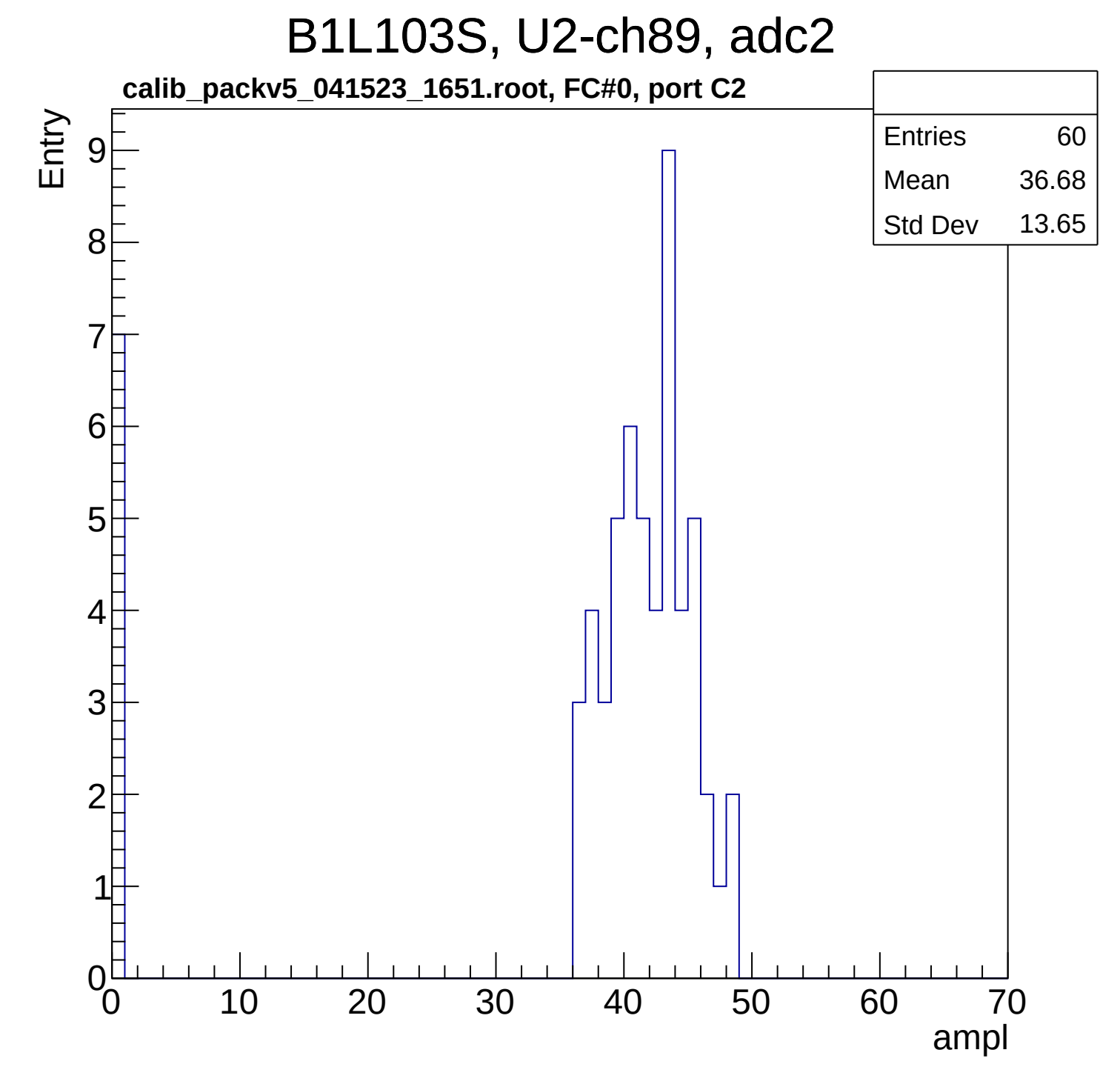

B1L103S, U2-ch88, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 57.24
Std Dev 3.37
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

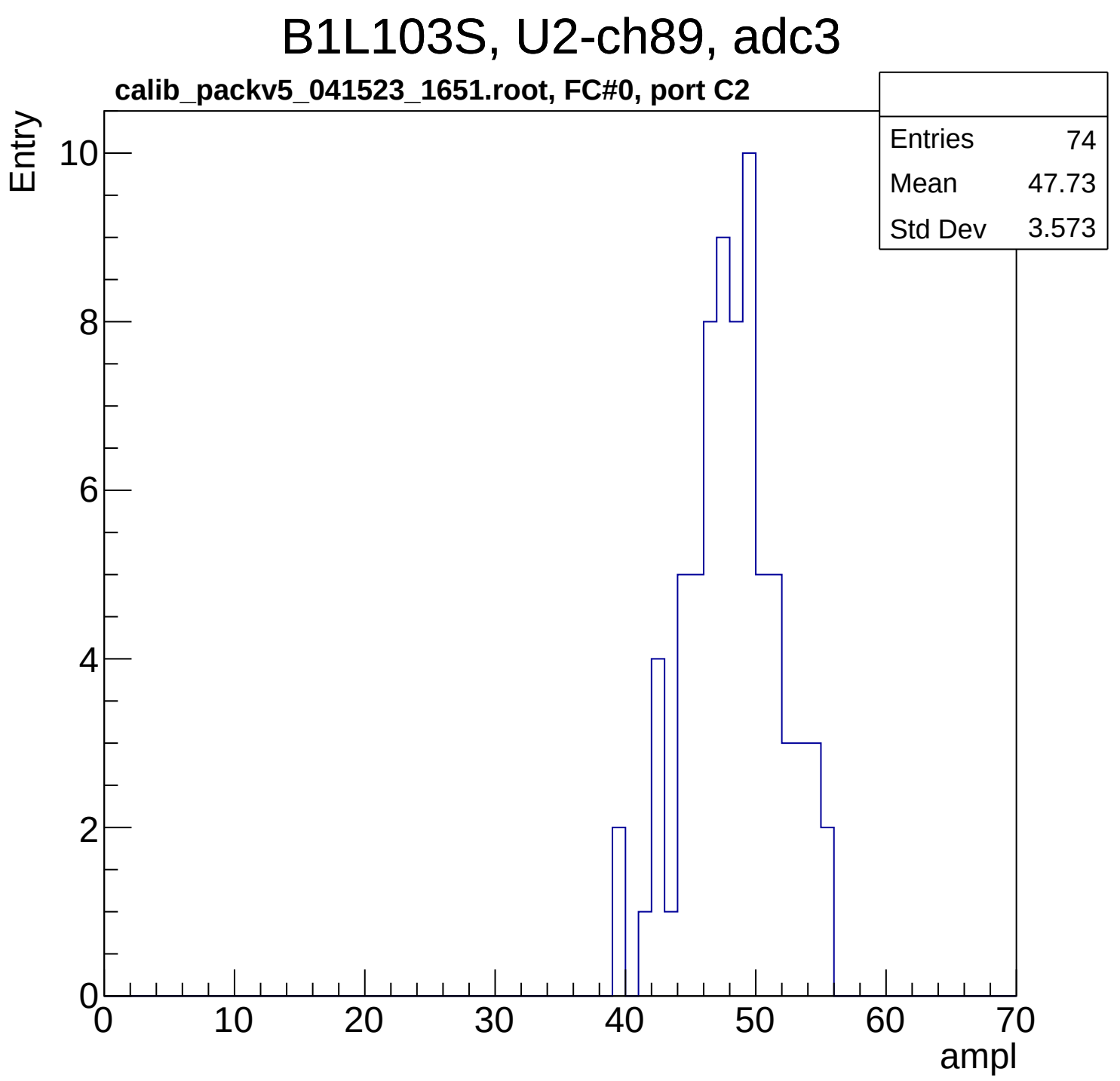

B1L103S, U2-ch88, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 58.72
Std Dev 10.13
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

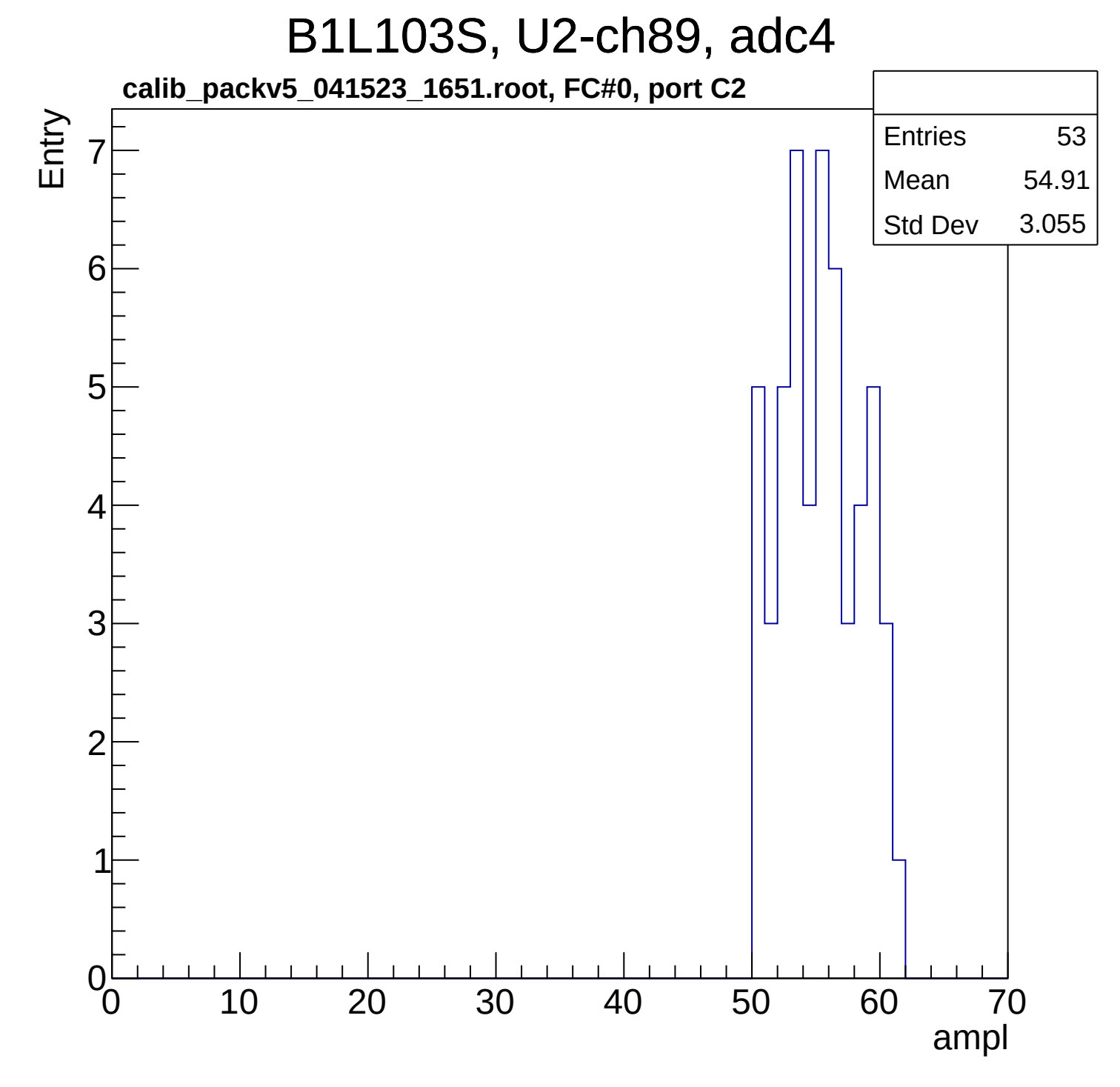

B1L103S, U2-ch88, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 16.58
Std Dev 27.32
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

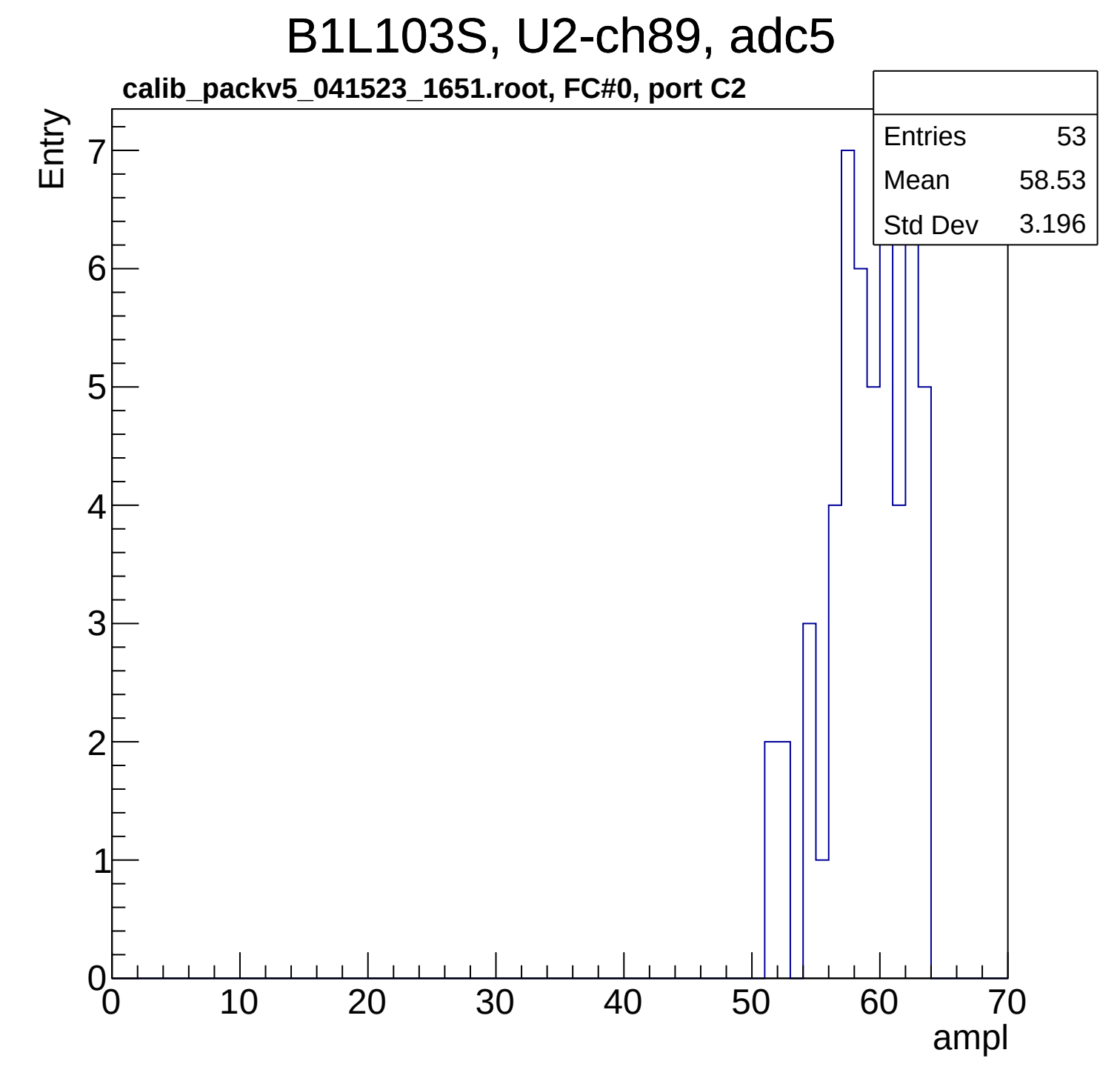

B1L103S, U2-ch89, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 21.7
Std Dev 12.95
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl

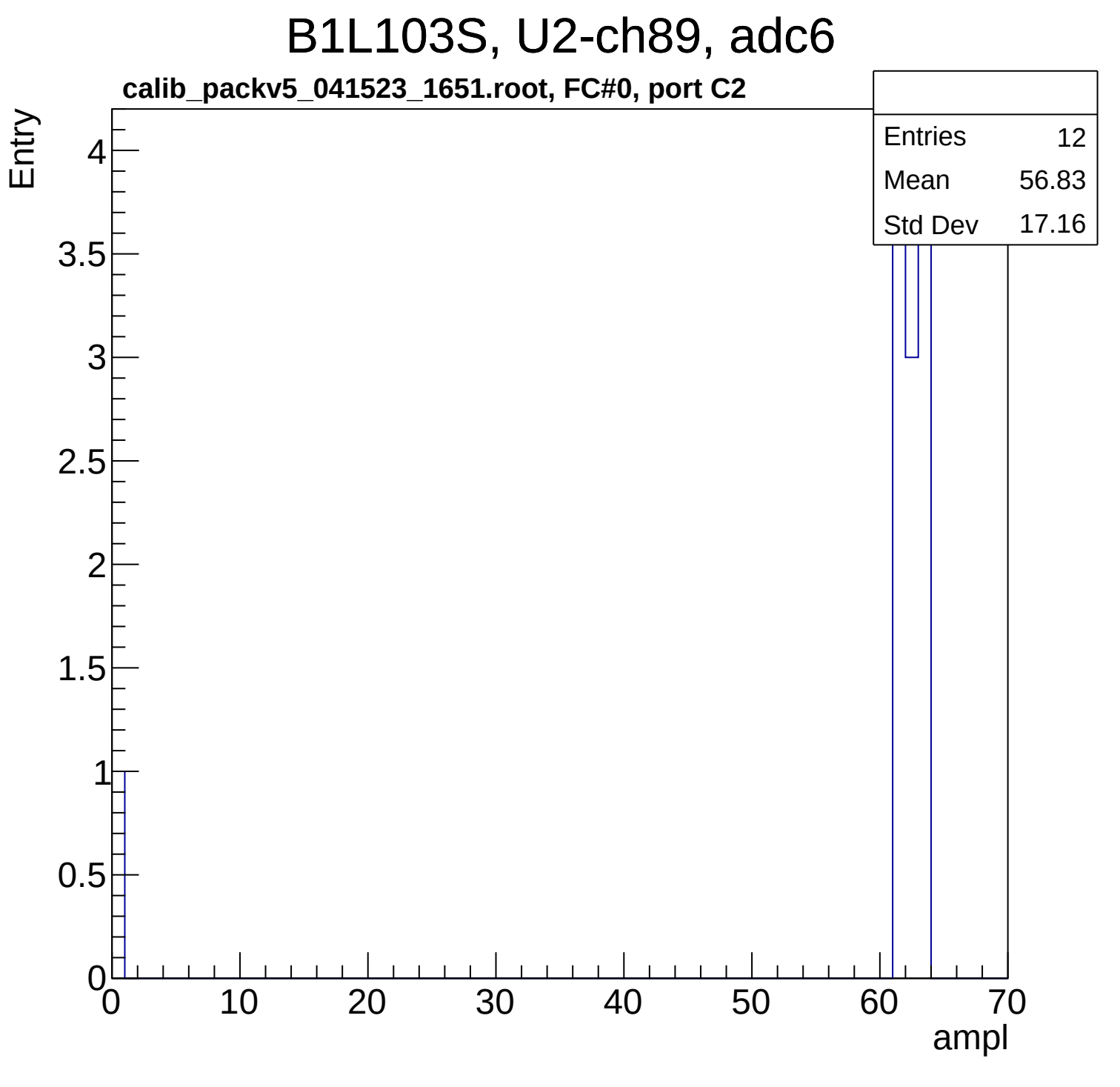

B1L103S, U2-ch89, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 32.07
Std Dev 11.39
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

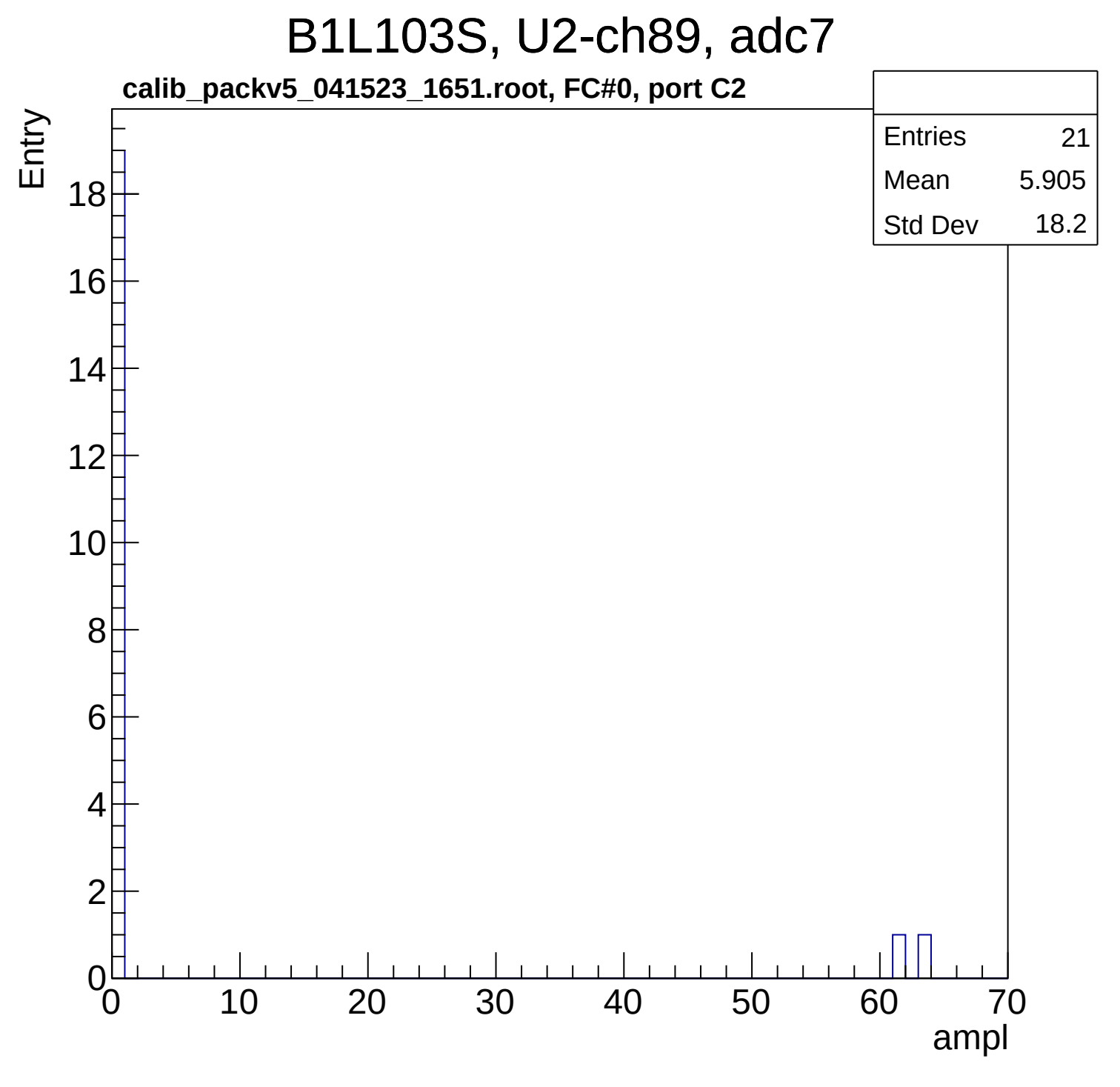

B1L103S, U2-ch89, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 36.68
Std Dev 13.65
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

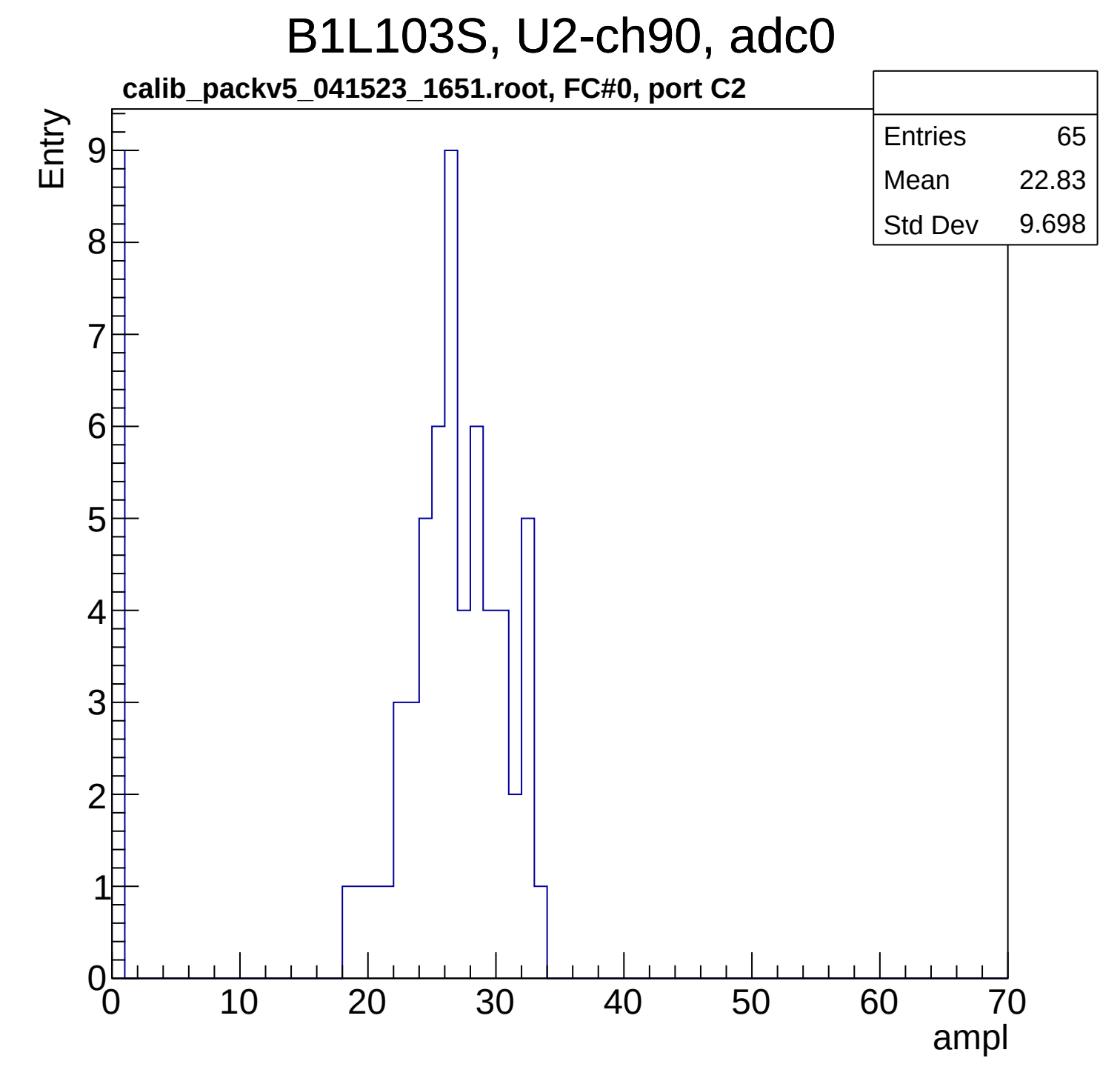

B1L103S, U2-ch89, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 47.73
Std Dev 3.573
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

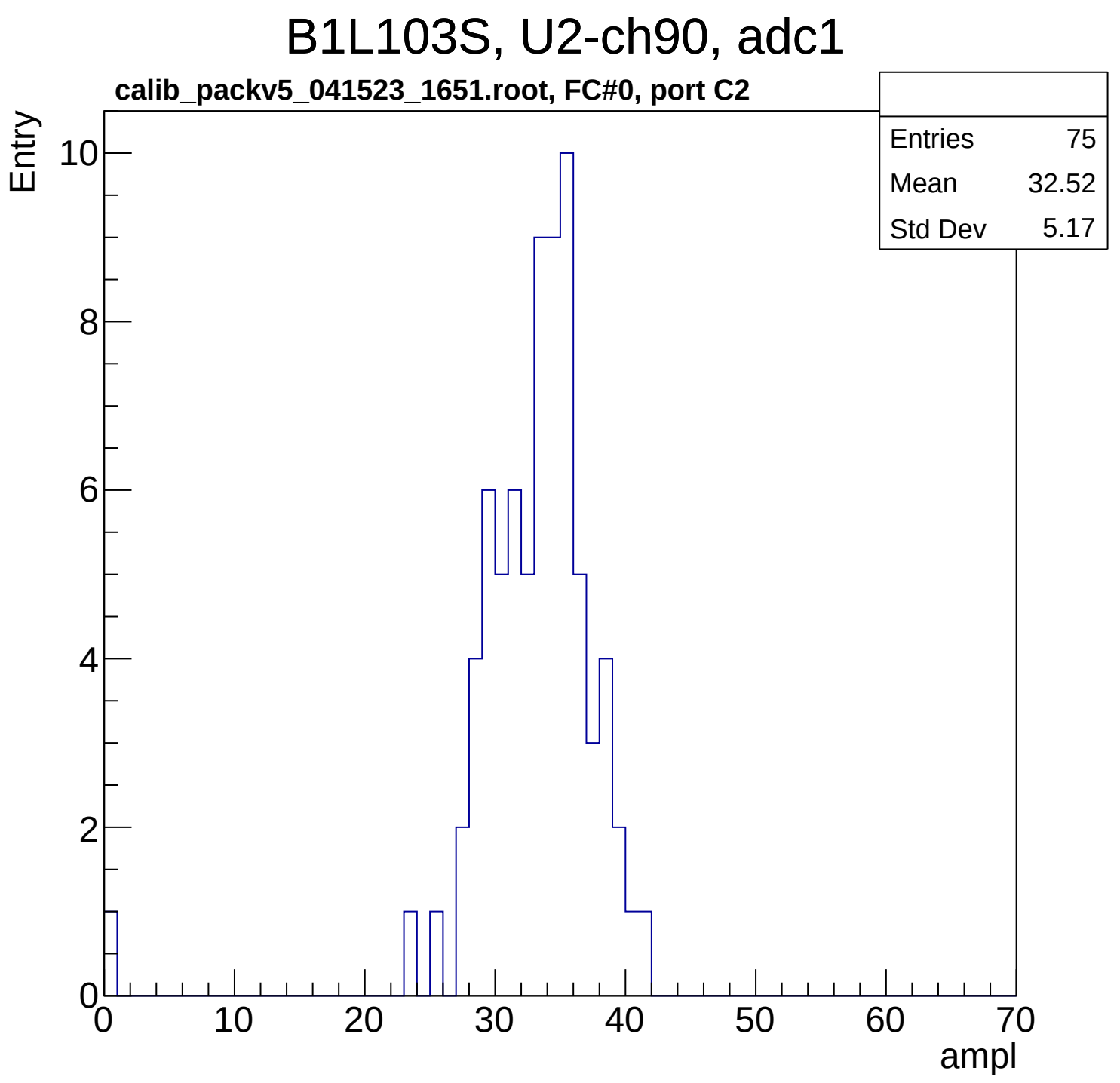

B1L103S, U2-ch89, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 54.91
Std Dev 3.055
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

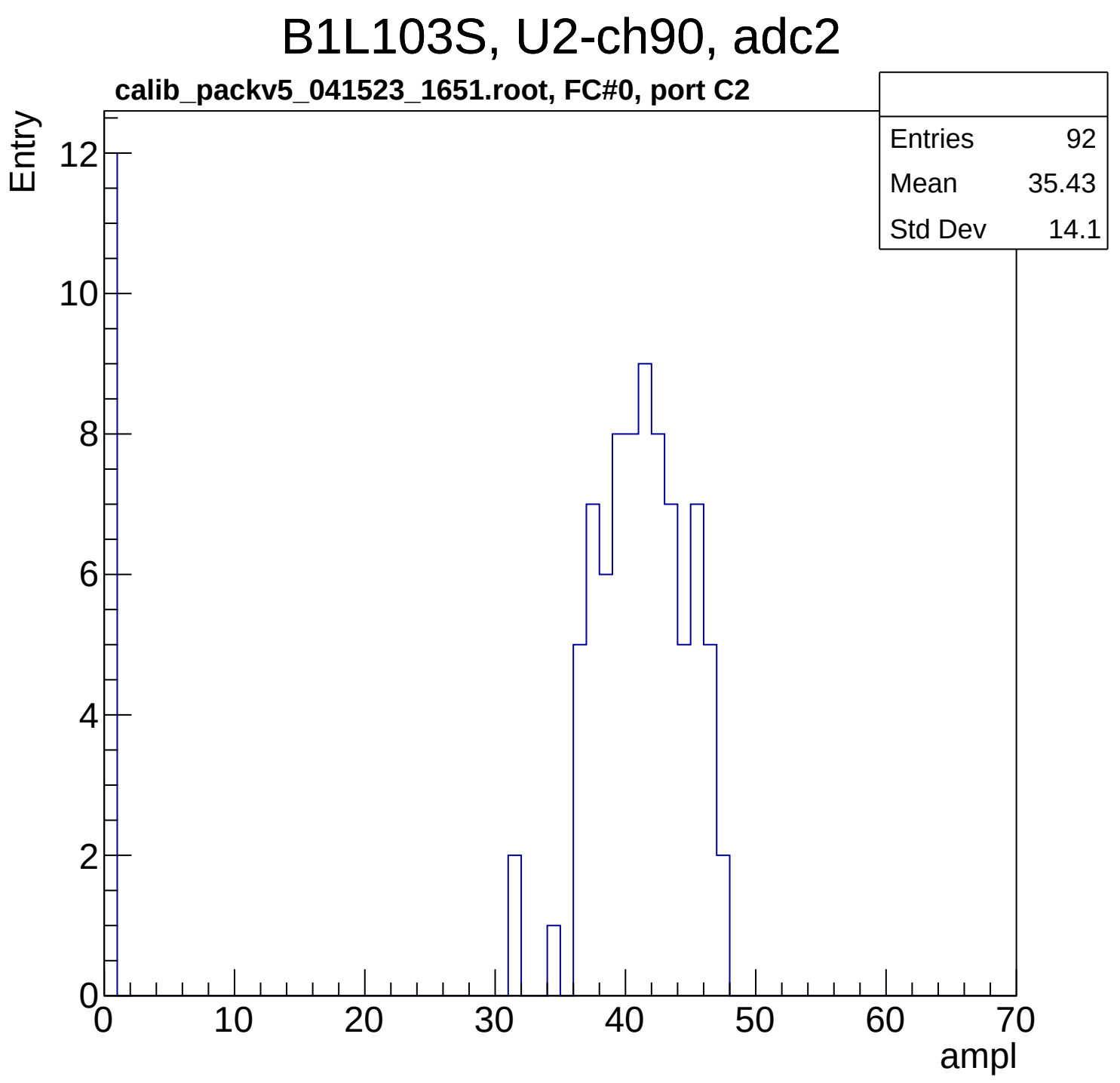

B1L103S, U2-ch89, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.53
Std Dev 3.196
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

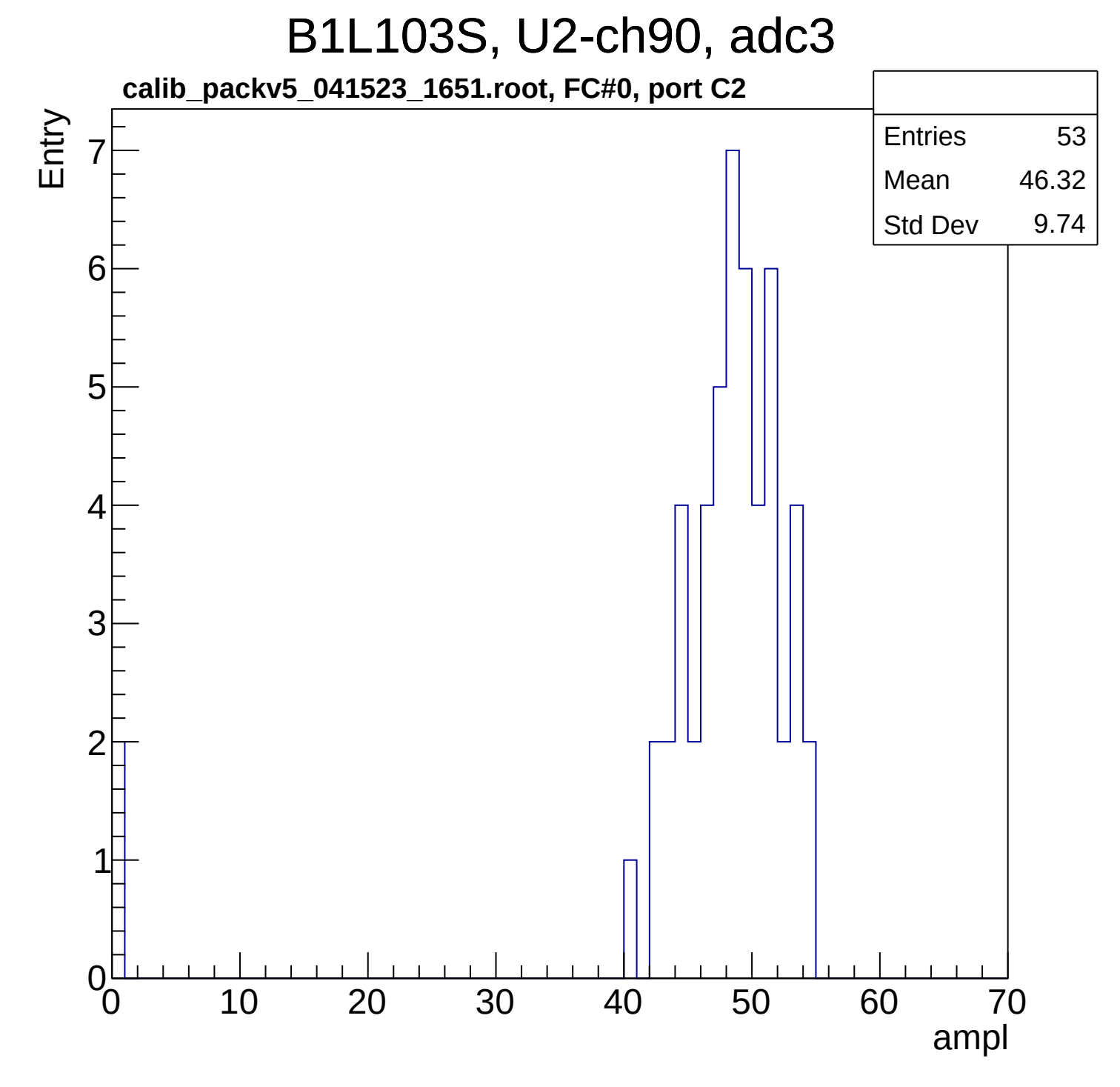

B1L103S, U2-ch89, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.83
Std Dev 17.16
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

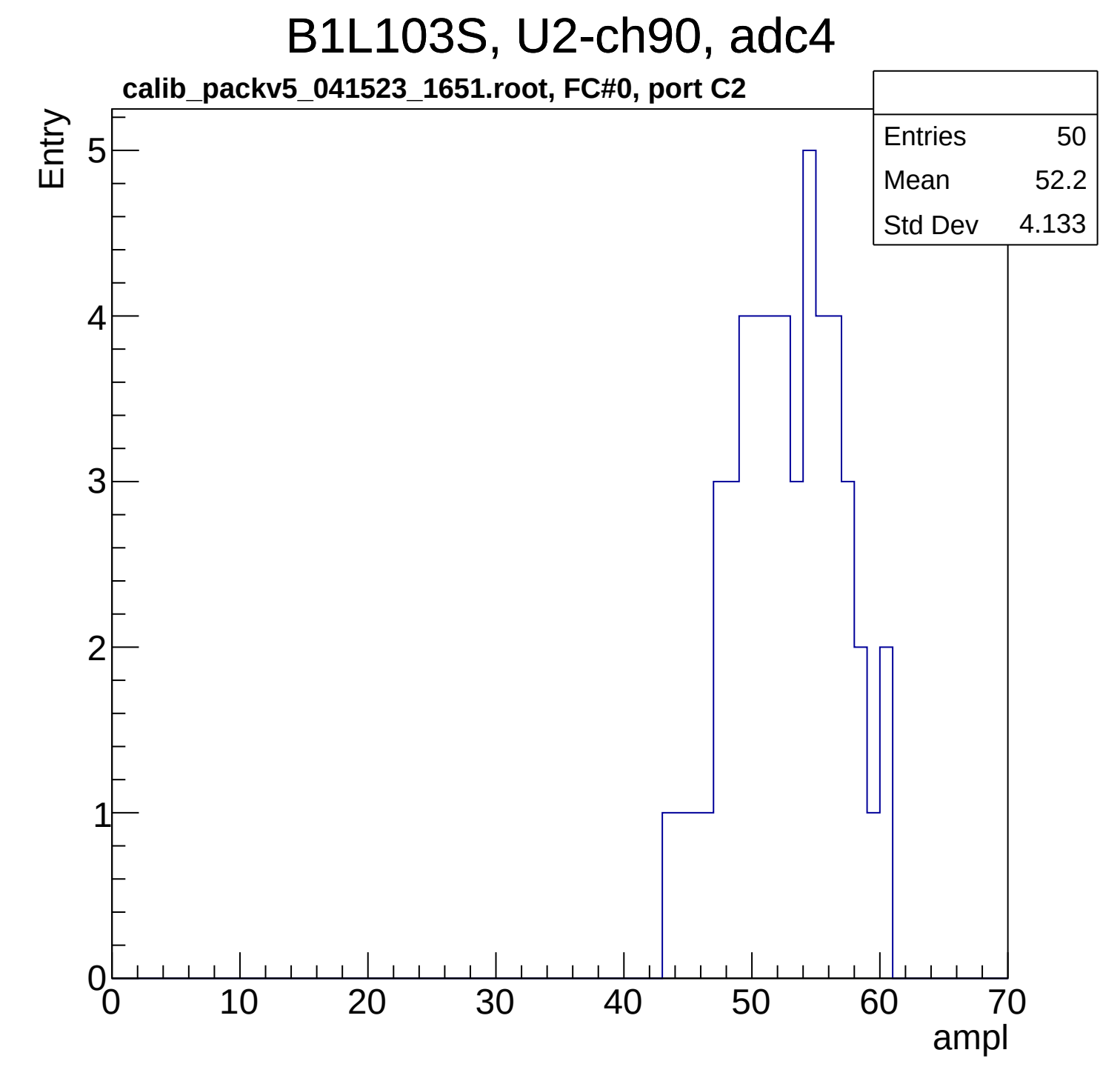

B1L103S, U2-ch89, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.905
Std Dev 18.2
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

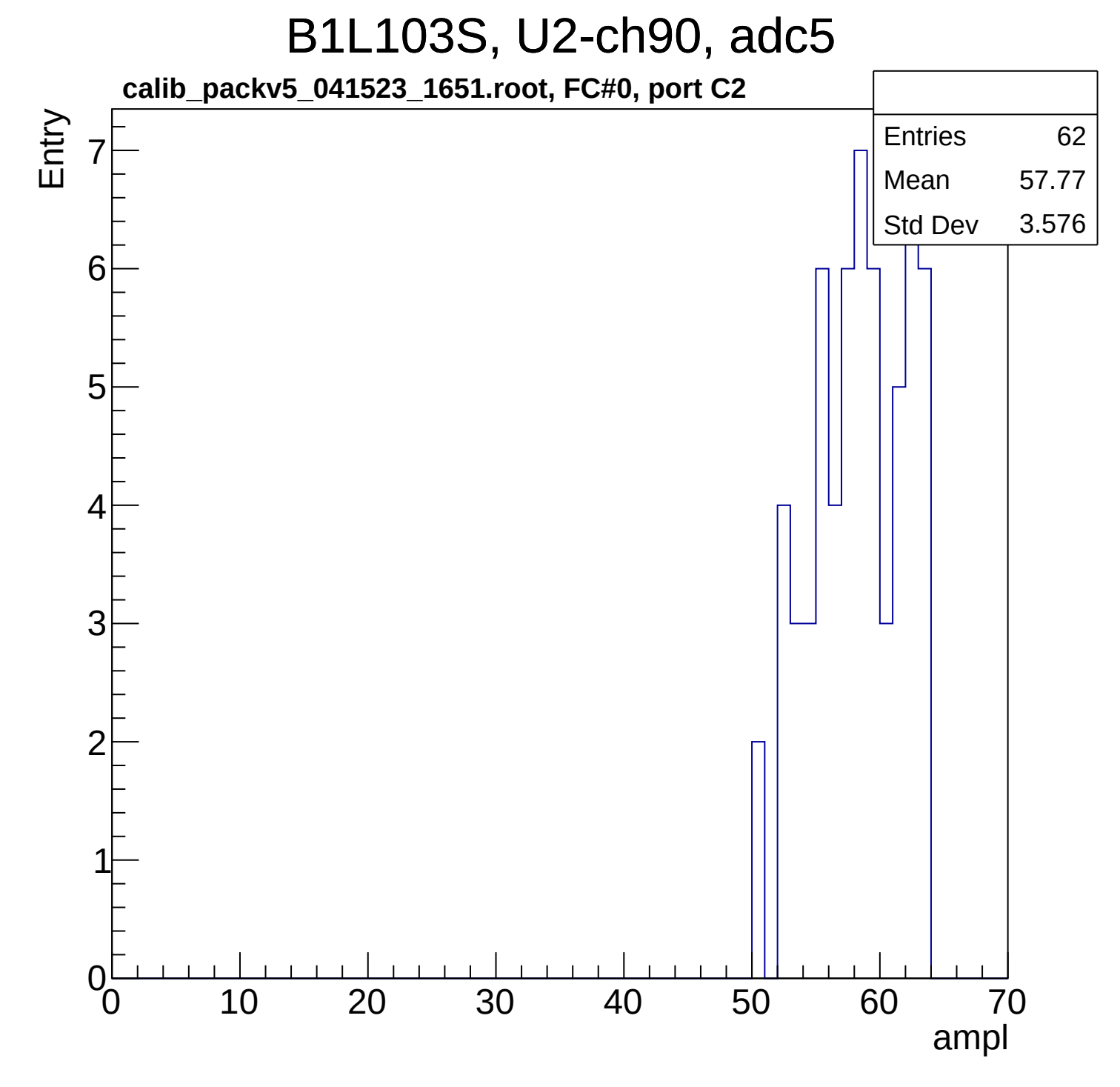

B1L103S, U2-ch90, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 22.83
Std Dev 9.698
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

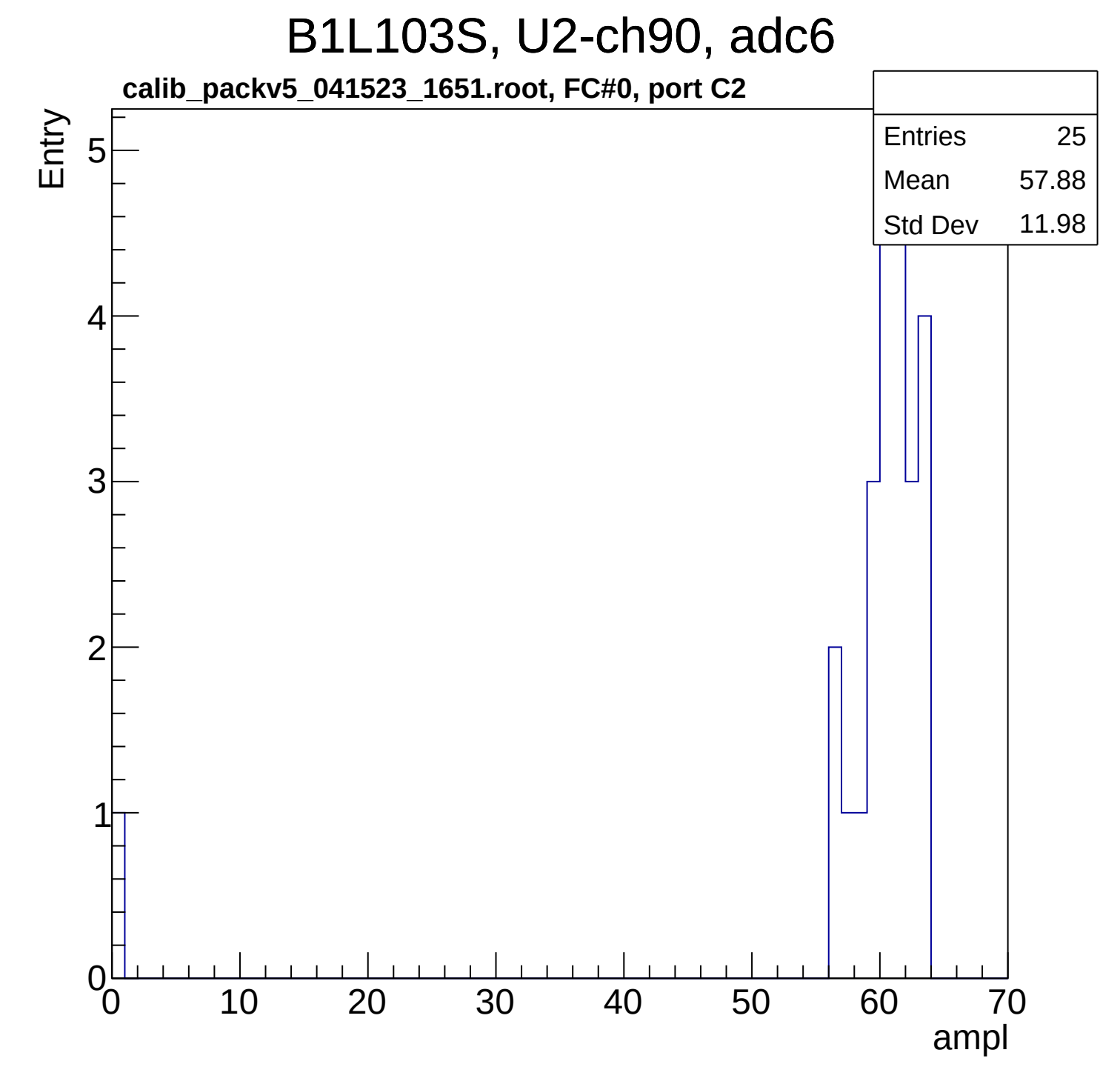

B1L103S, U2-ch90, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 32.52
Std Dev 5.17
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

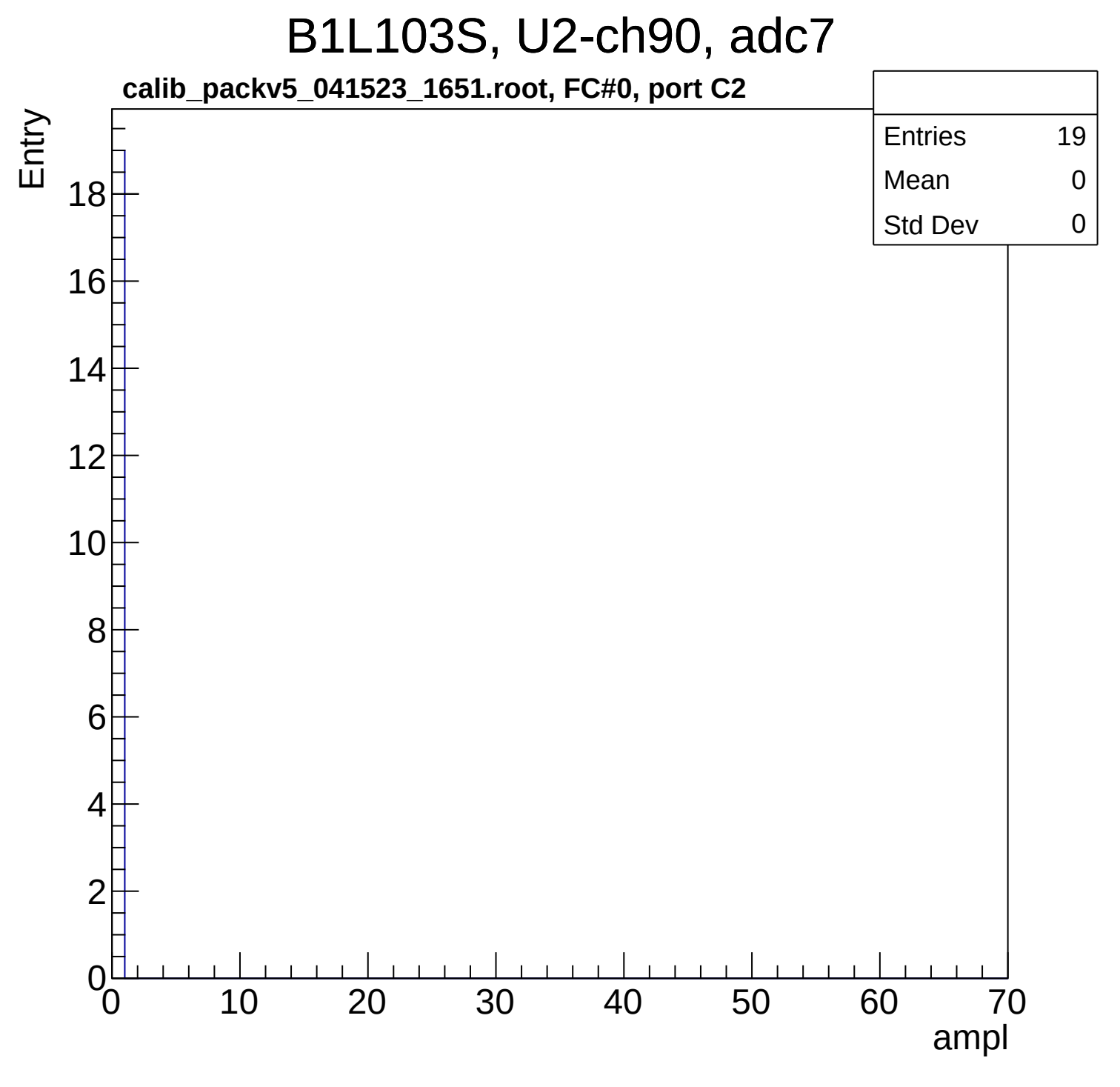

B1L103S, U2-ch90, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 35.43
Std Dev 14.1
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

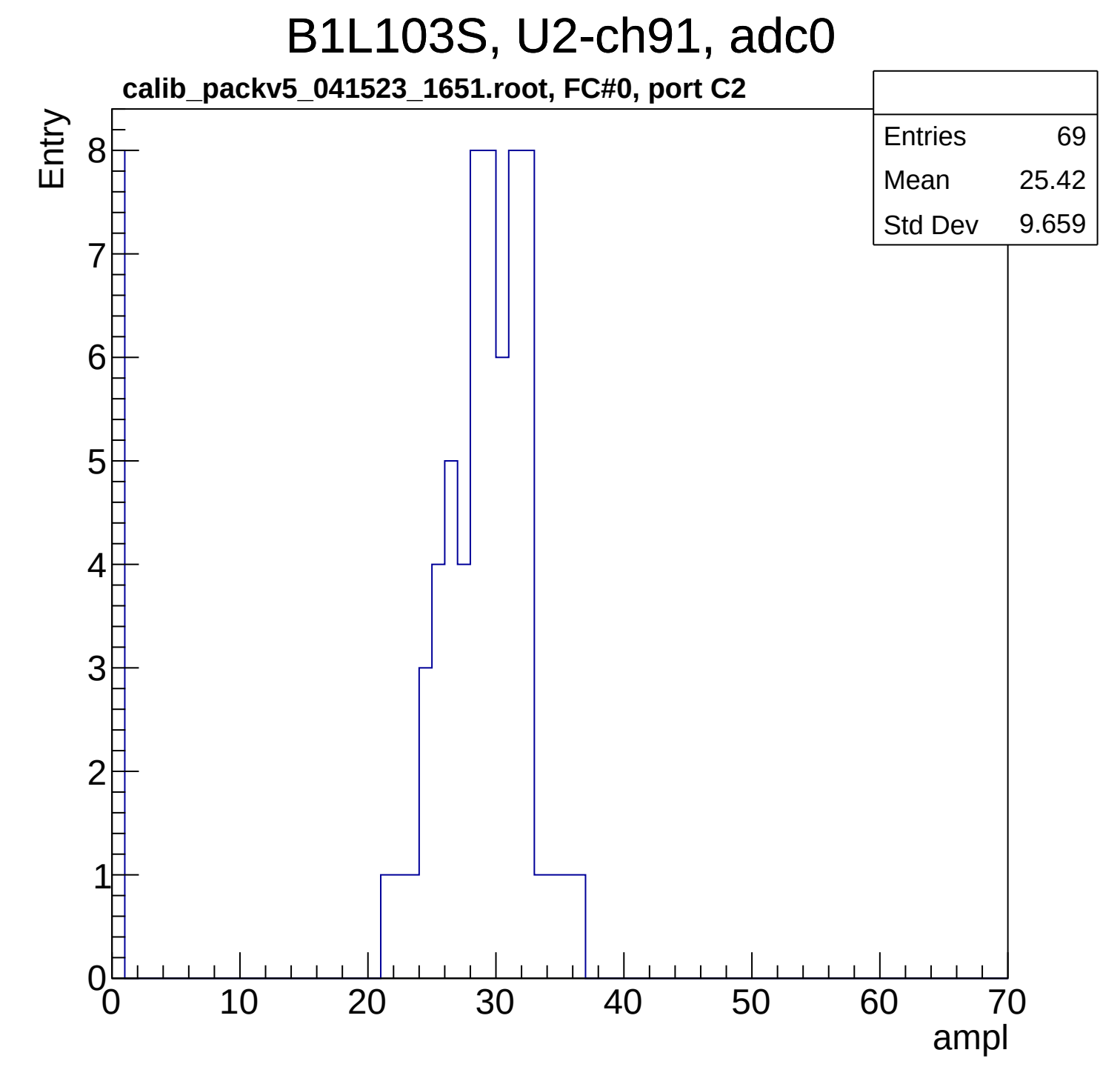

B1L103S, U2-ch90, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 46.32
Std Dev 9.74
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

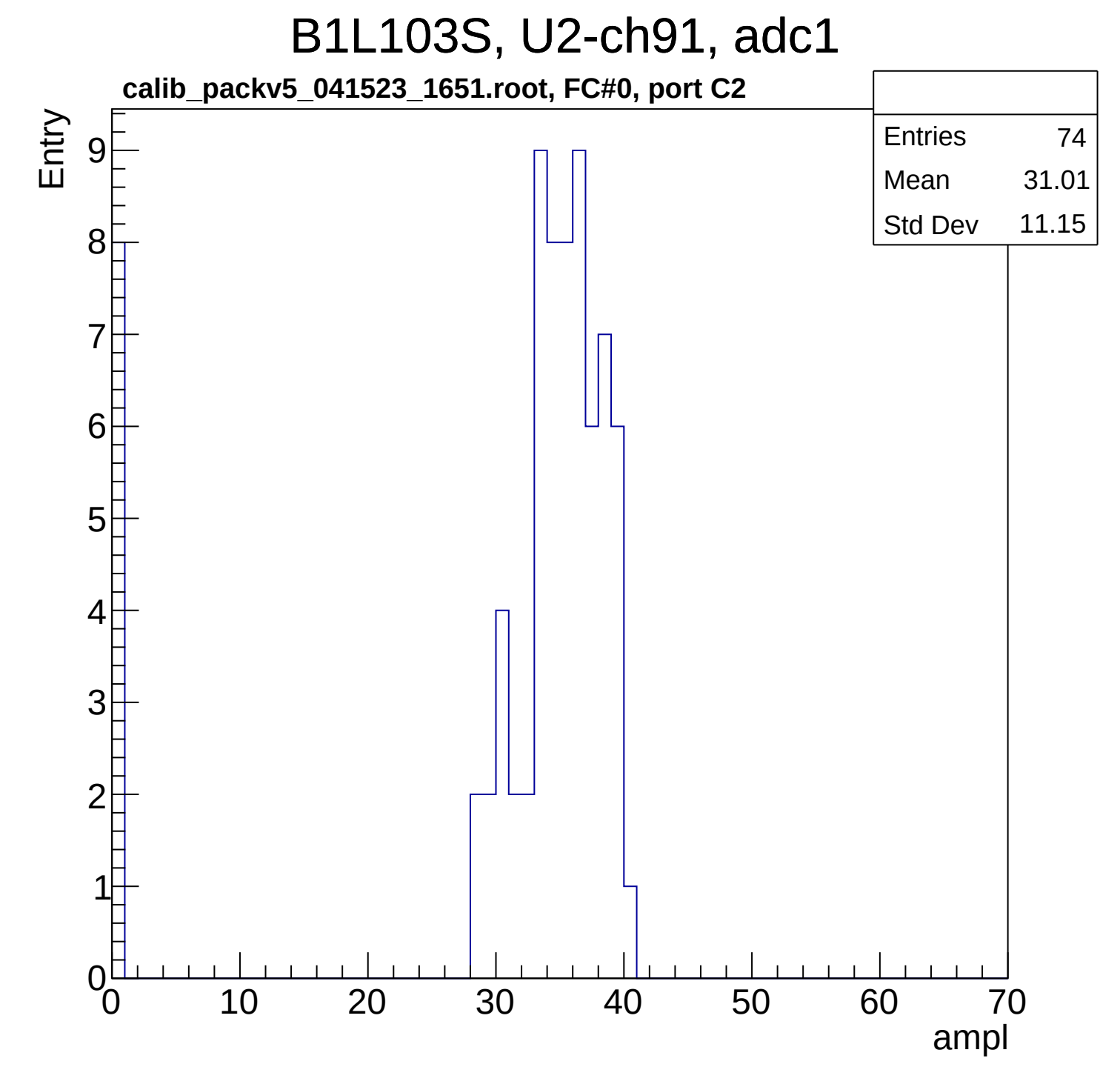

B1L103S, U2-ch90, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 52.2
Std Dev 4.133
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

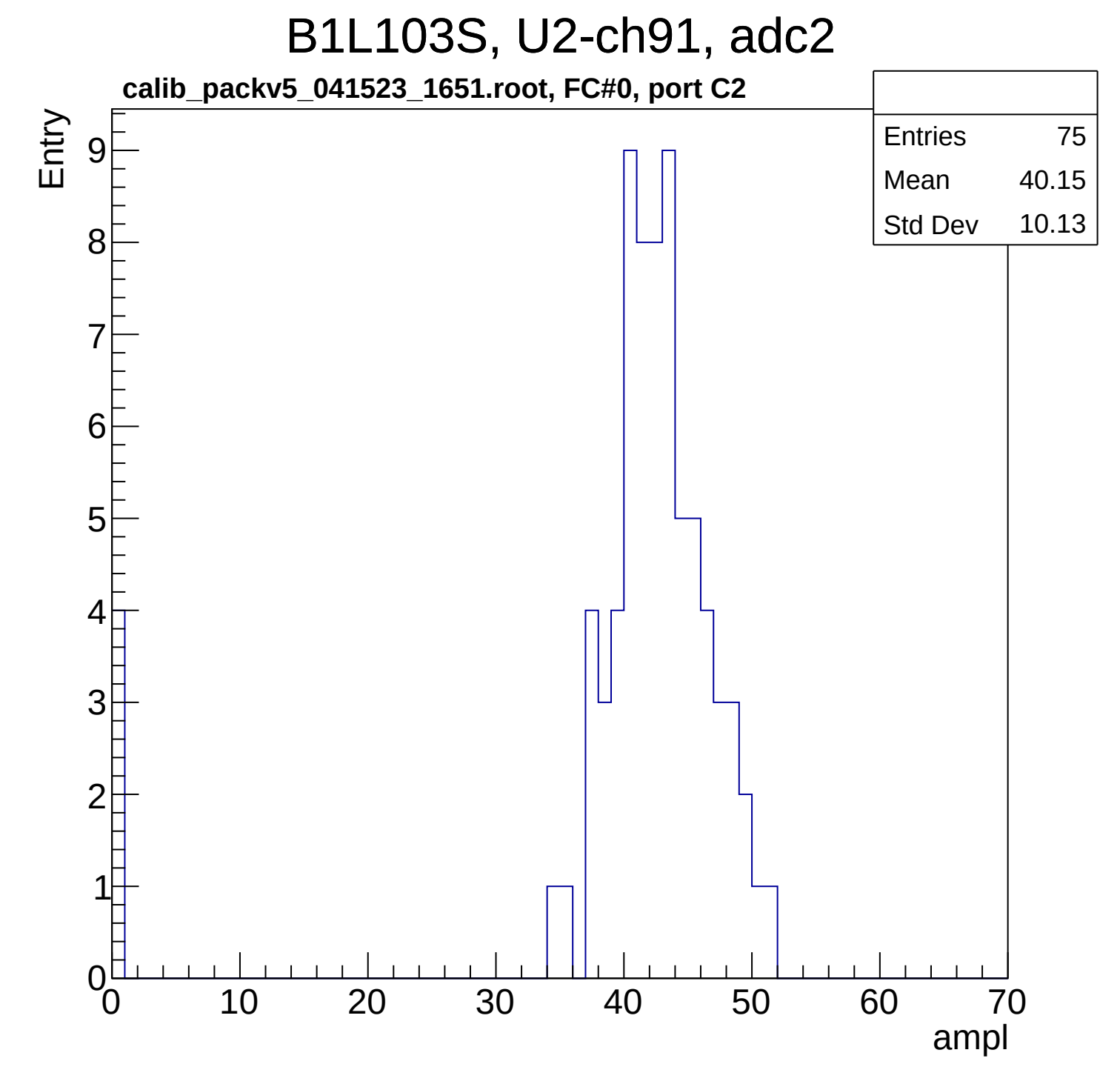

B1L103S, U2-ch90, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 57.77
Std Dev 3.576
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

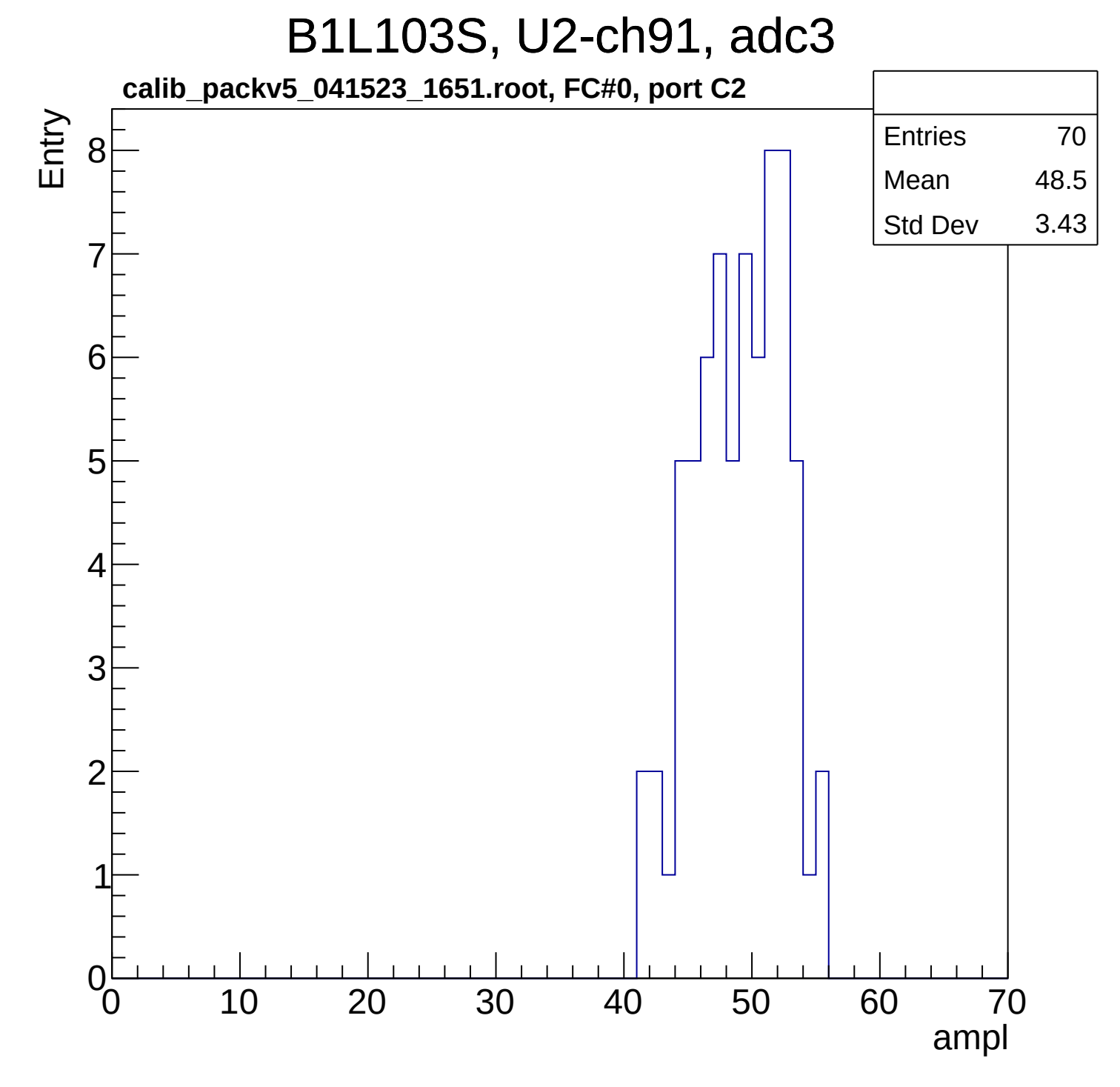

B1L103S, U2-ch90, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 25
Mean 57.88
Std Dev 11.98
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

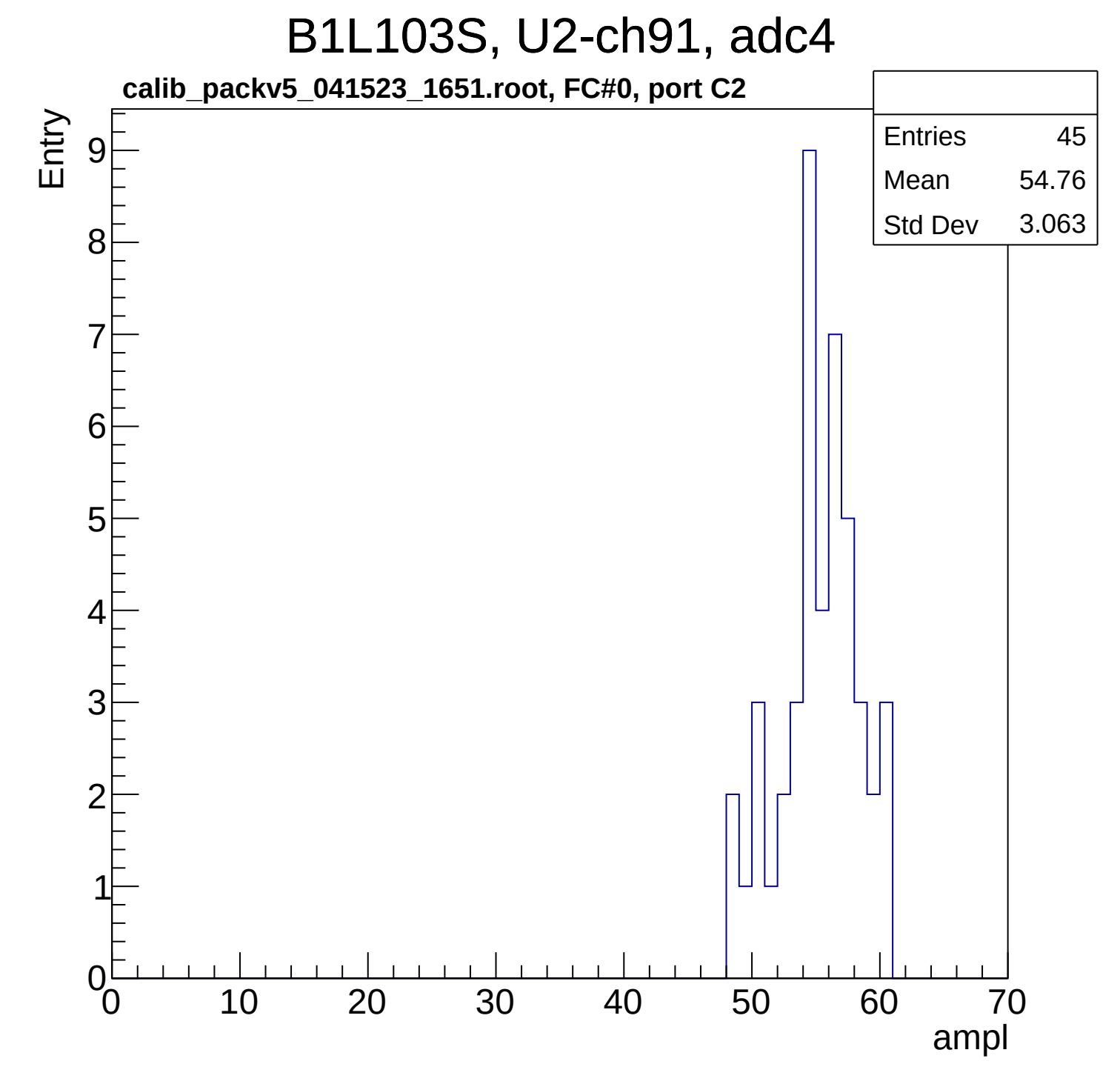

B1L103S, U2-ch90, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

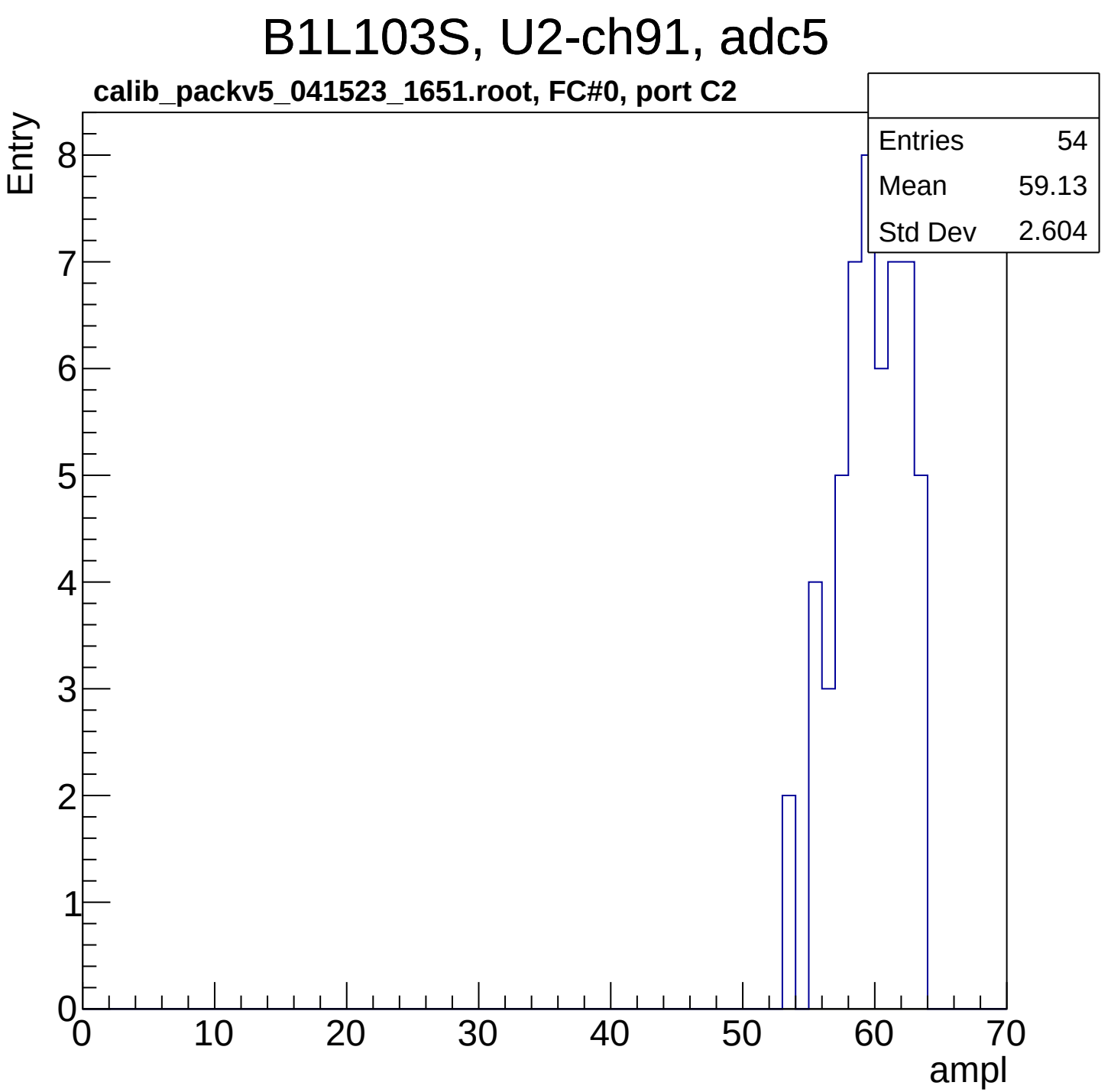

B1L103S, U2-ch91, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 25.42
Std Dev 9.659
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

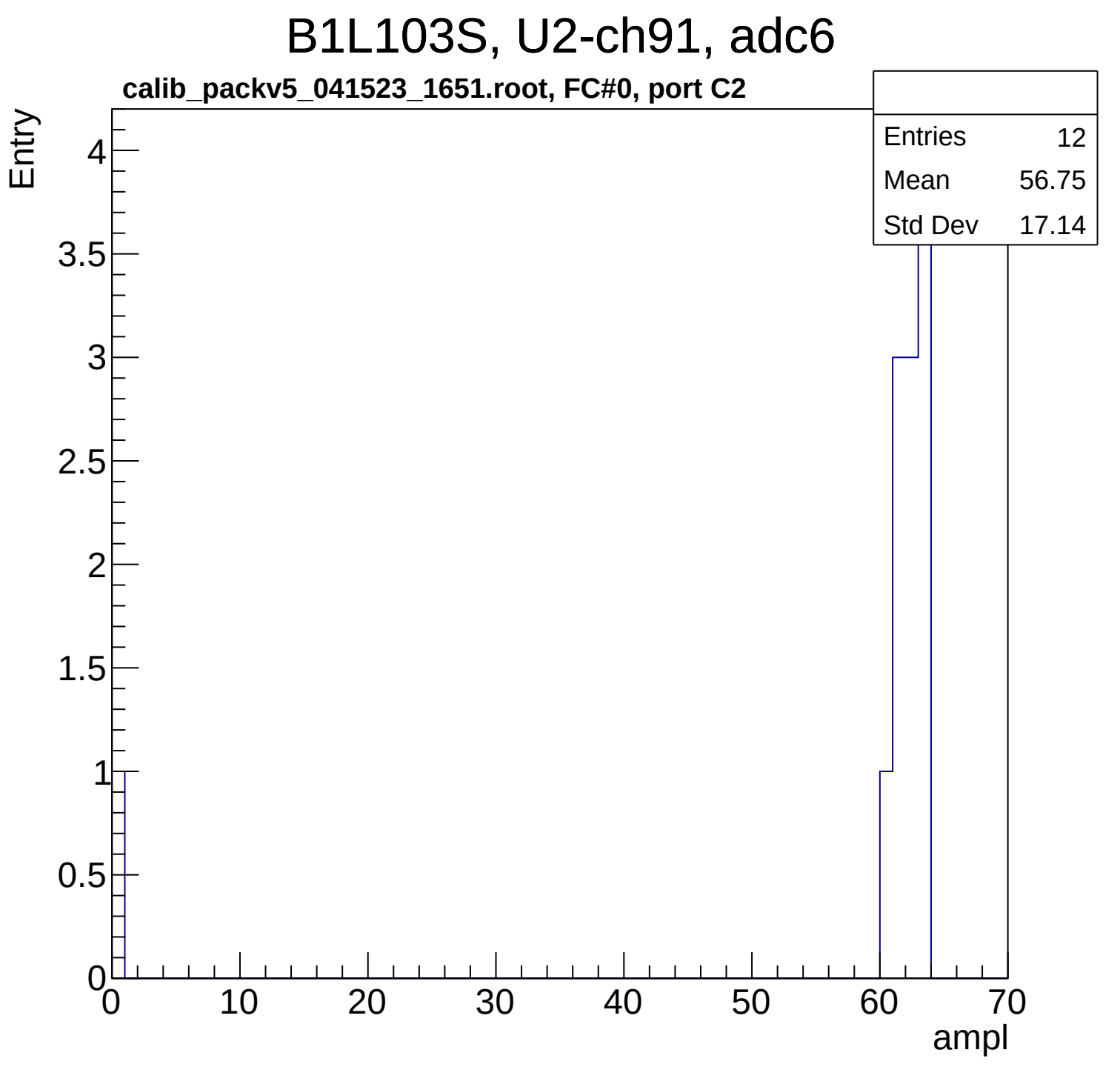

B1L103S, U2-ch91, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 31.01
Std Dev 11.15
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

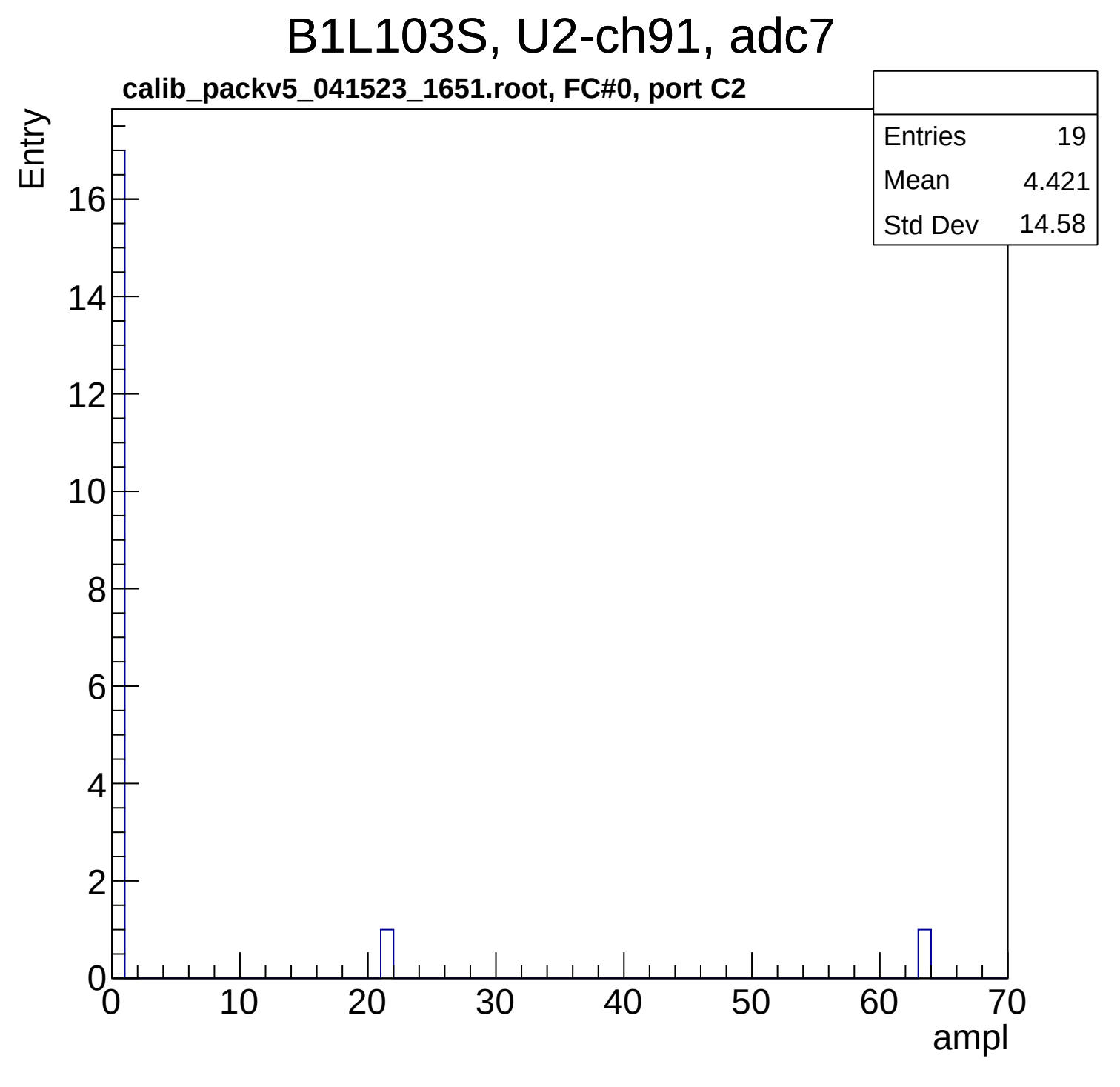

B1L103S, U2-ch91, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 40.15
Std Dev 10.13
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

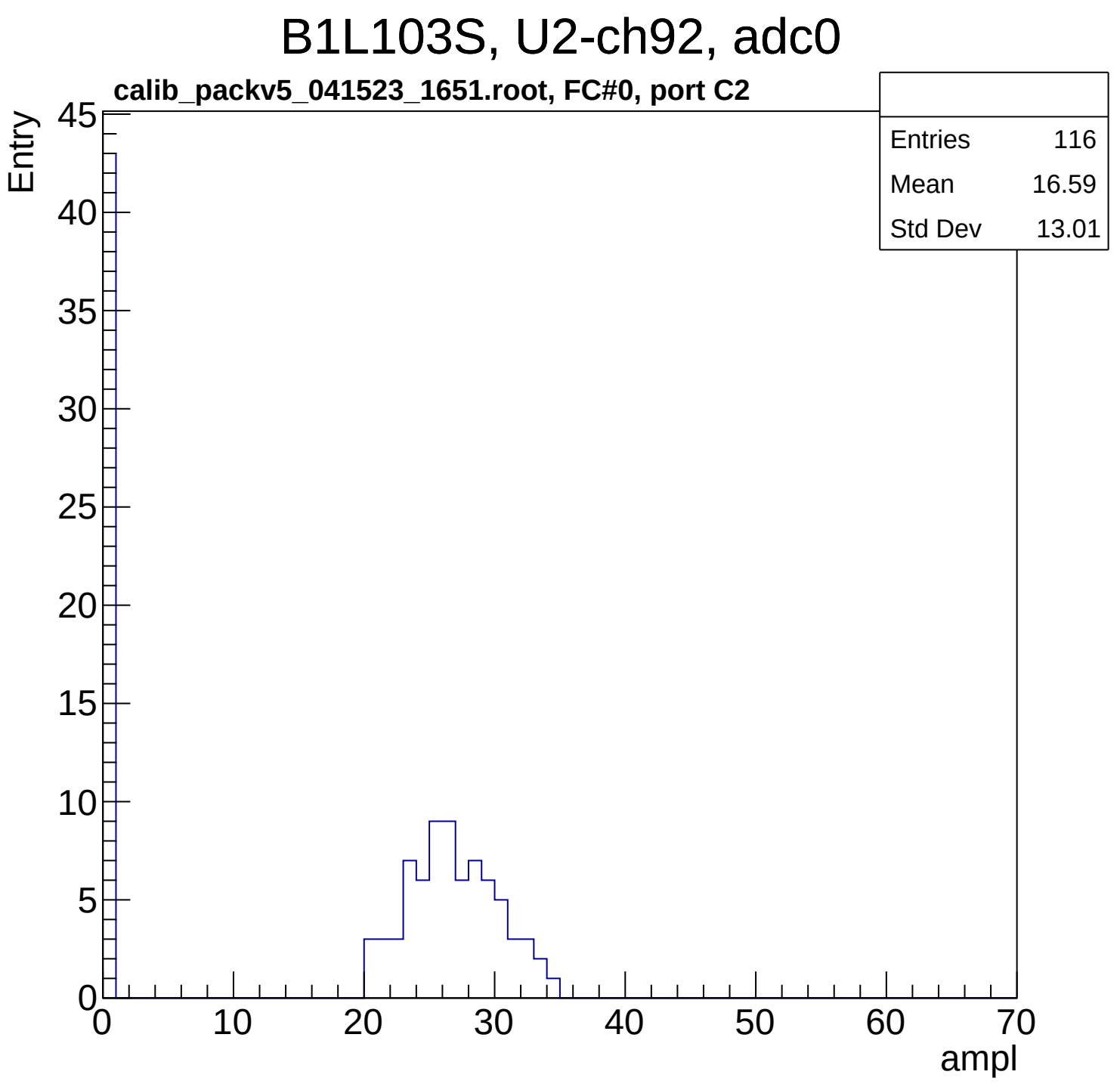

B1L103S, U2-ch91, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 48.5
Std Dev 3.43
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

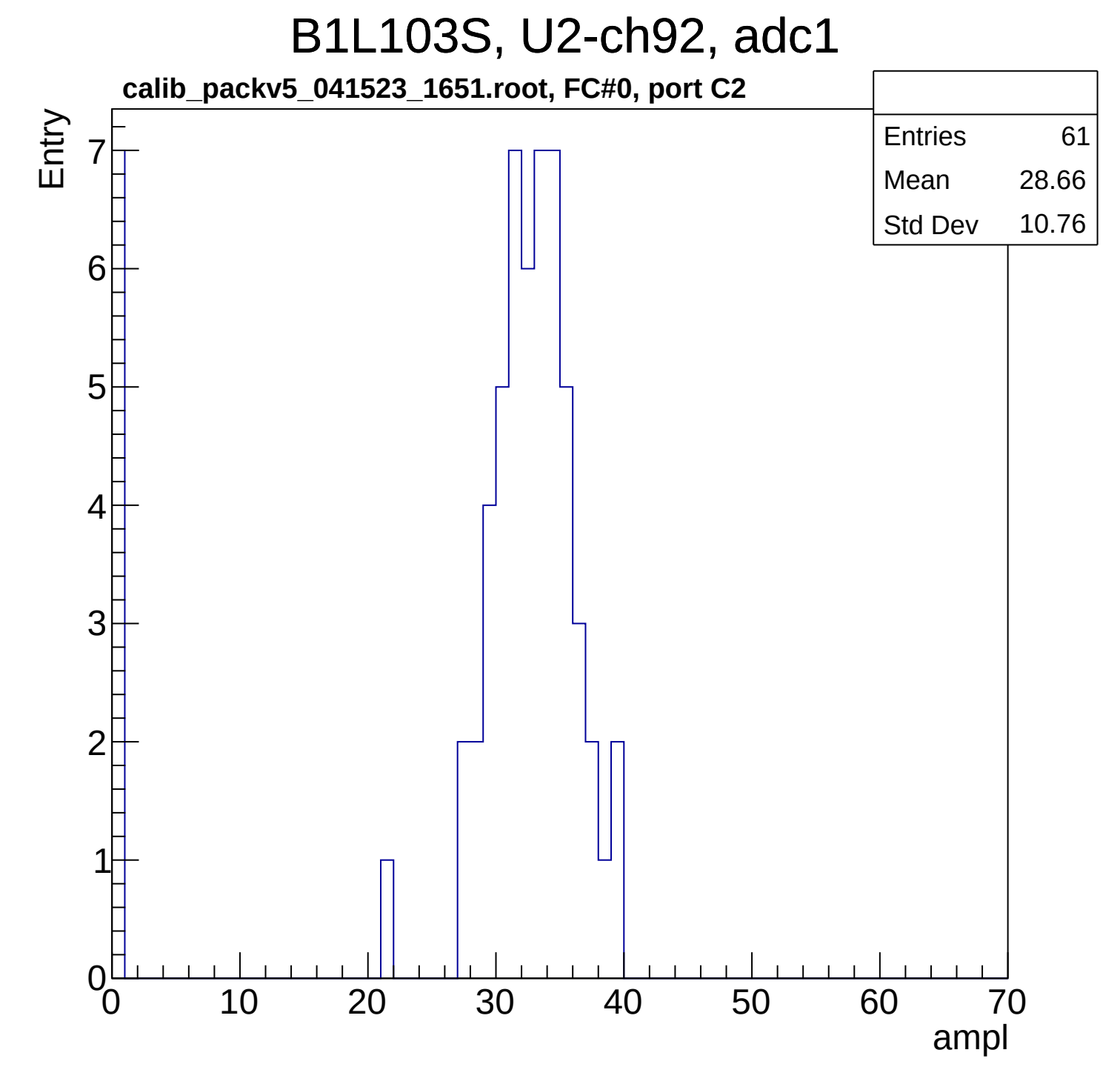

B1L103S, U2-ch91, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 54.76
Std Dev 3.063
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

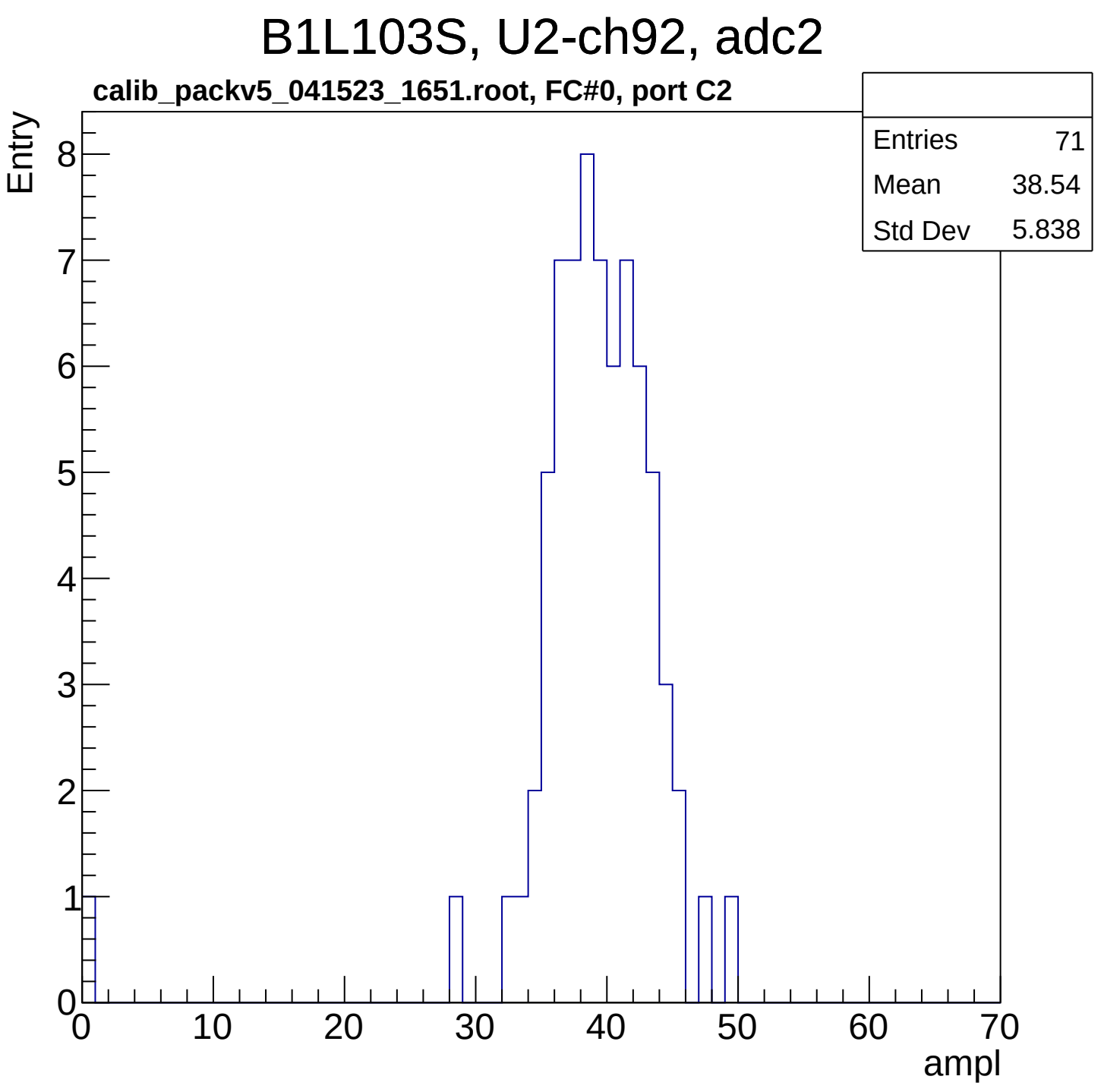

B1L103S, U2-ch91, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 59.13
Std Dev 2.604
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

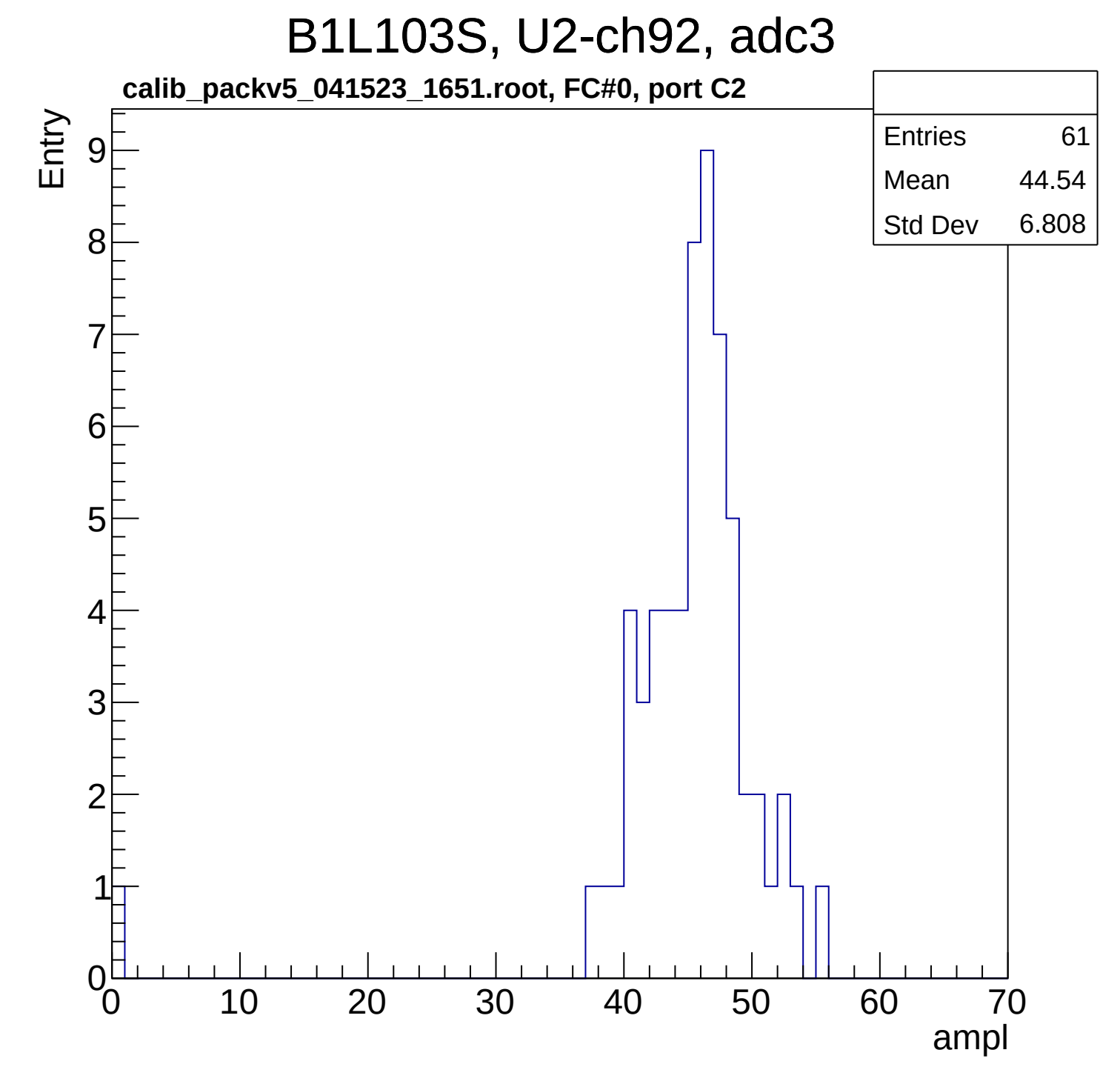

B1L103S, U2-ch91, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.75
Std Dev 17.14
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

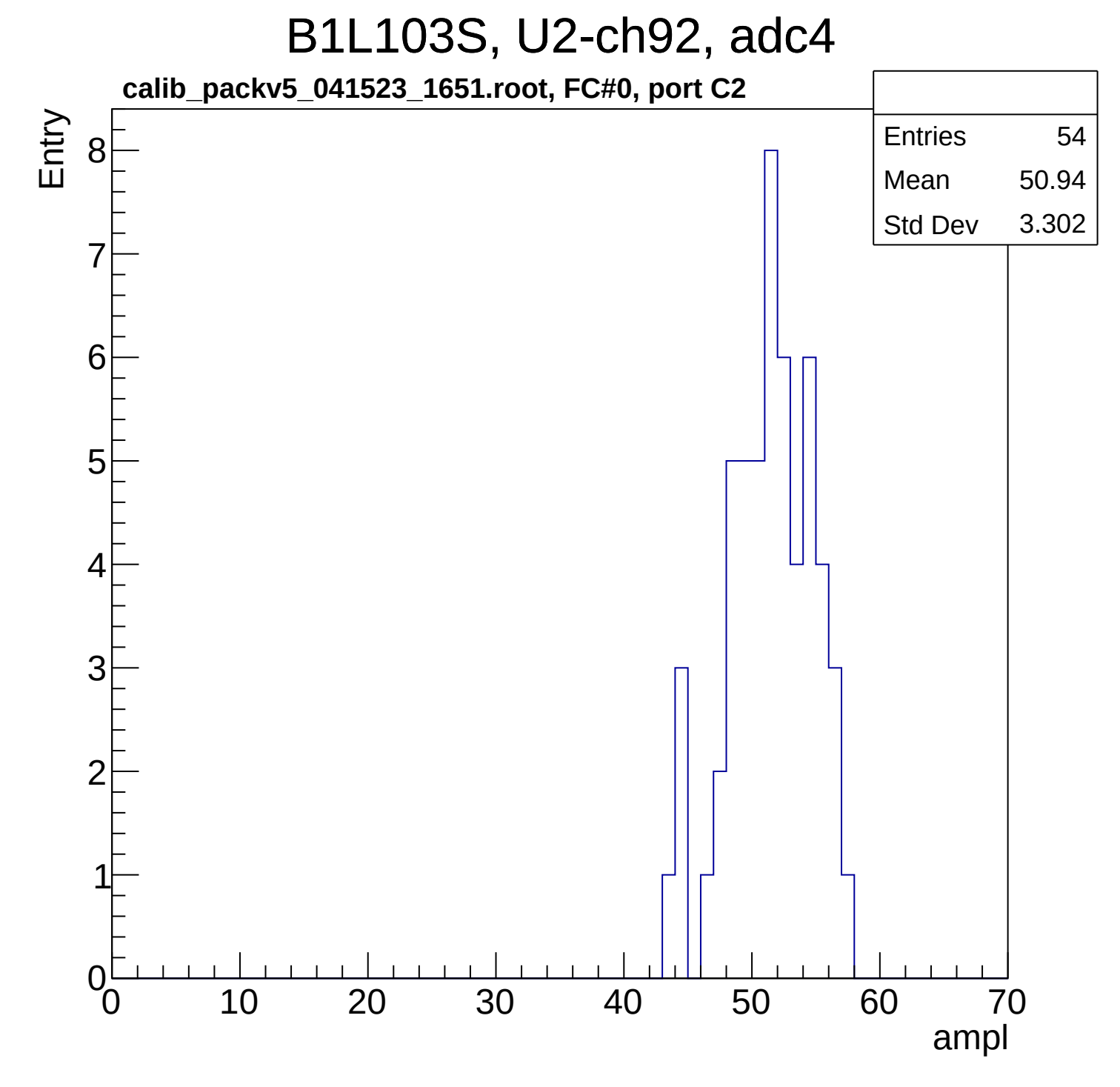

B1L103S, U2-ch91, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 4.421
Std Dev 14.58
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

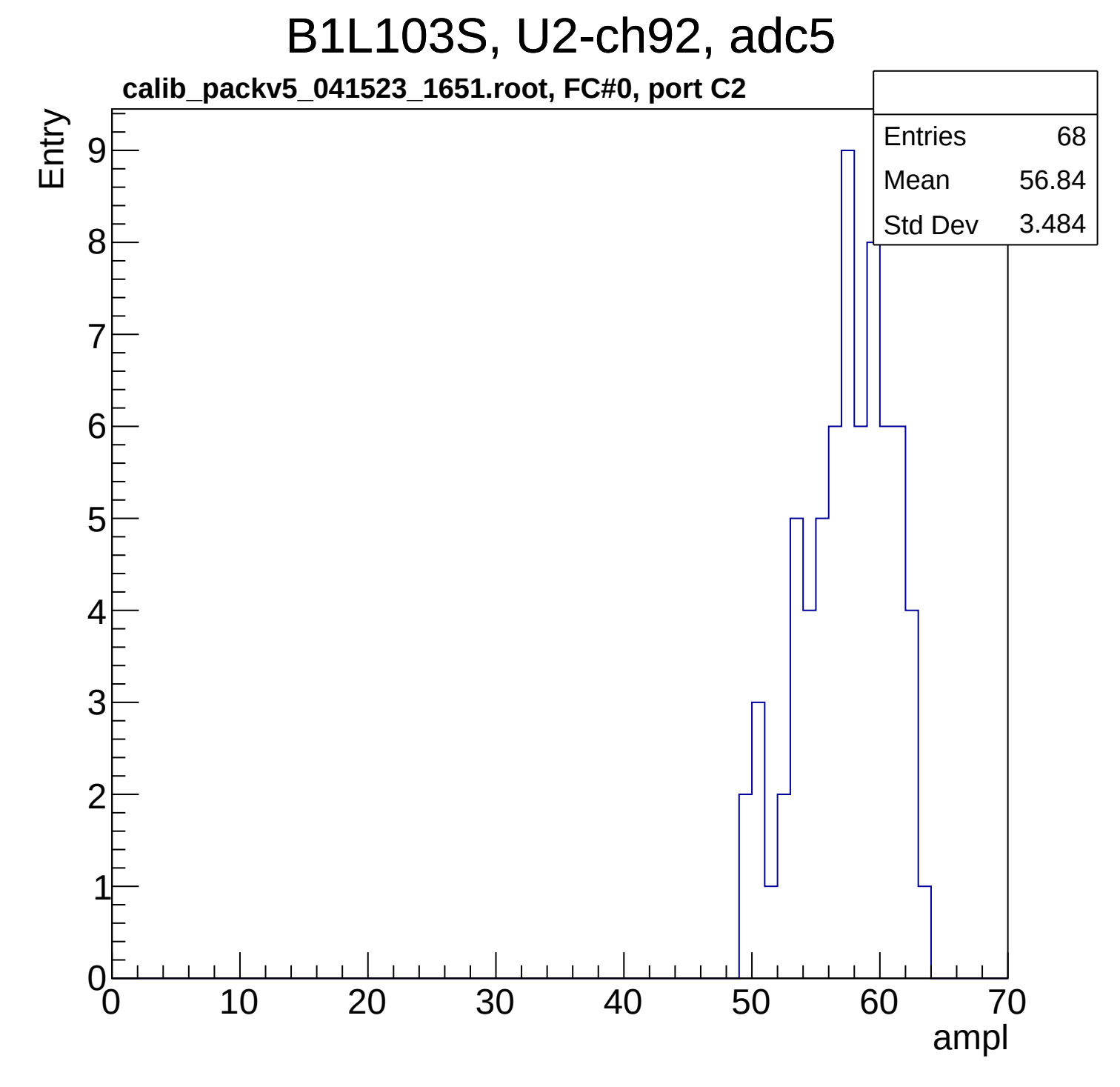

B1L103S, U2-ch92, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 116
Mean 16.59
Std Dev 13.01
Entry
ampl
0
5
10
15
20
25
30
35
40
45
0
10
20
30
40
50
60
70

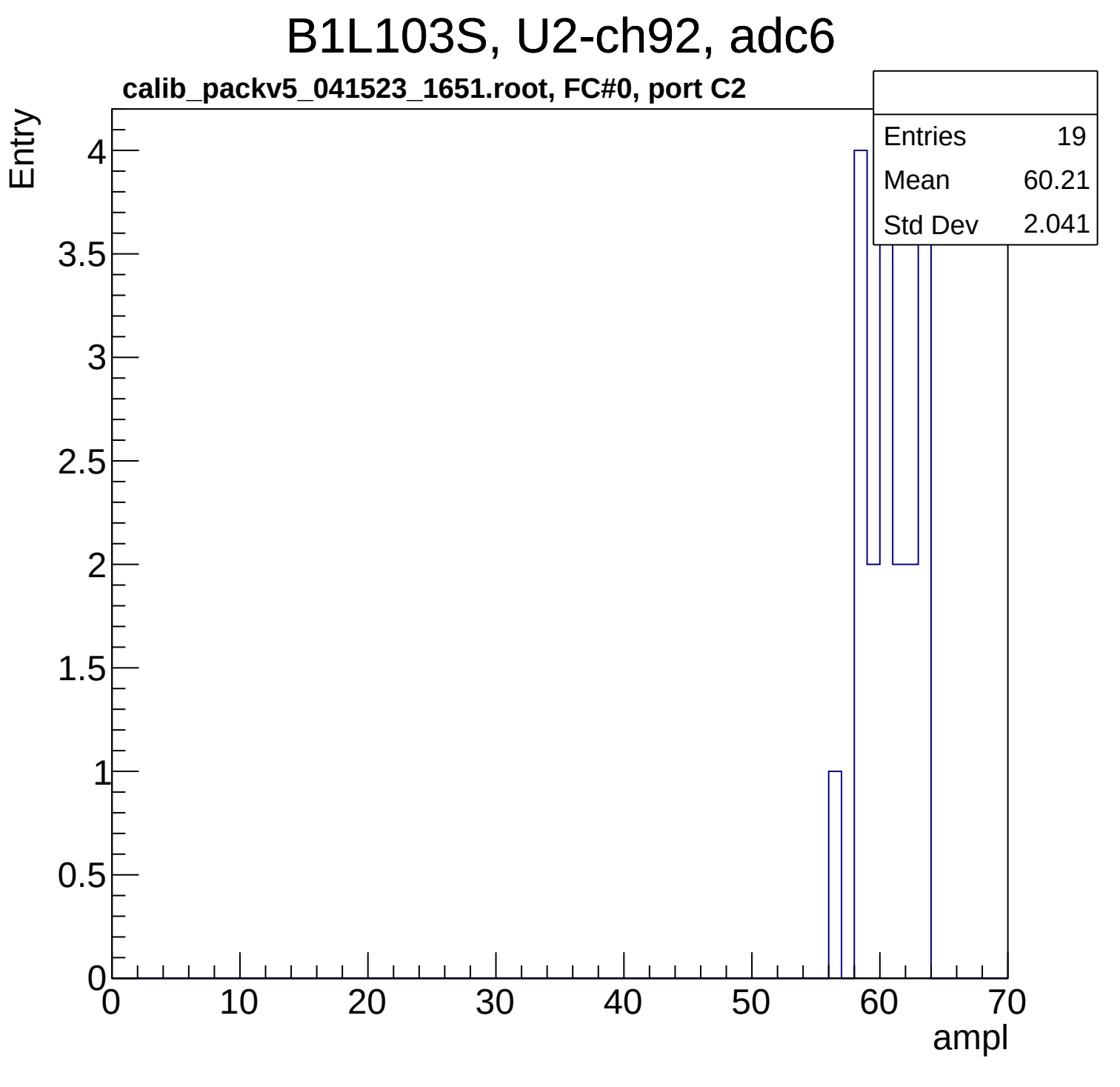

B1L103S, U2-ch92, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 28.66
Std Dev 10.76
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

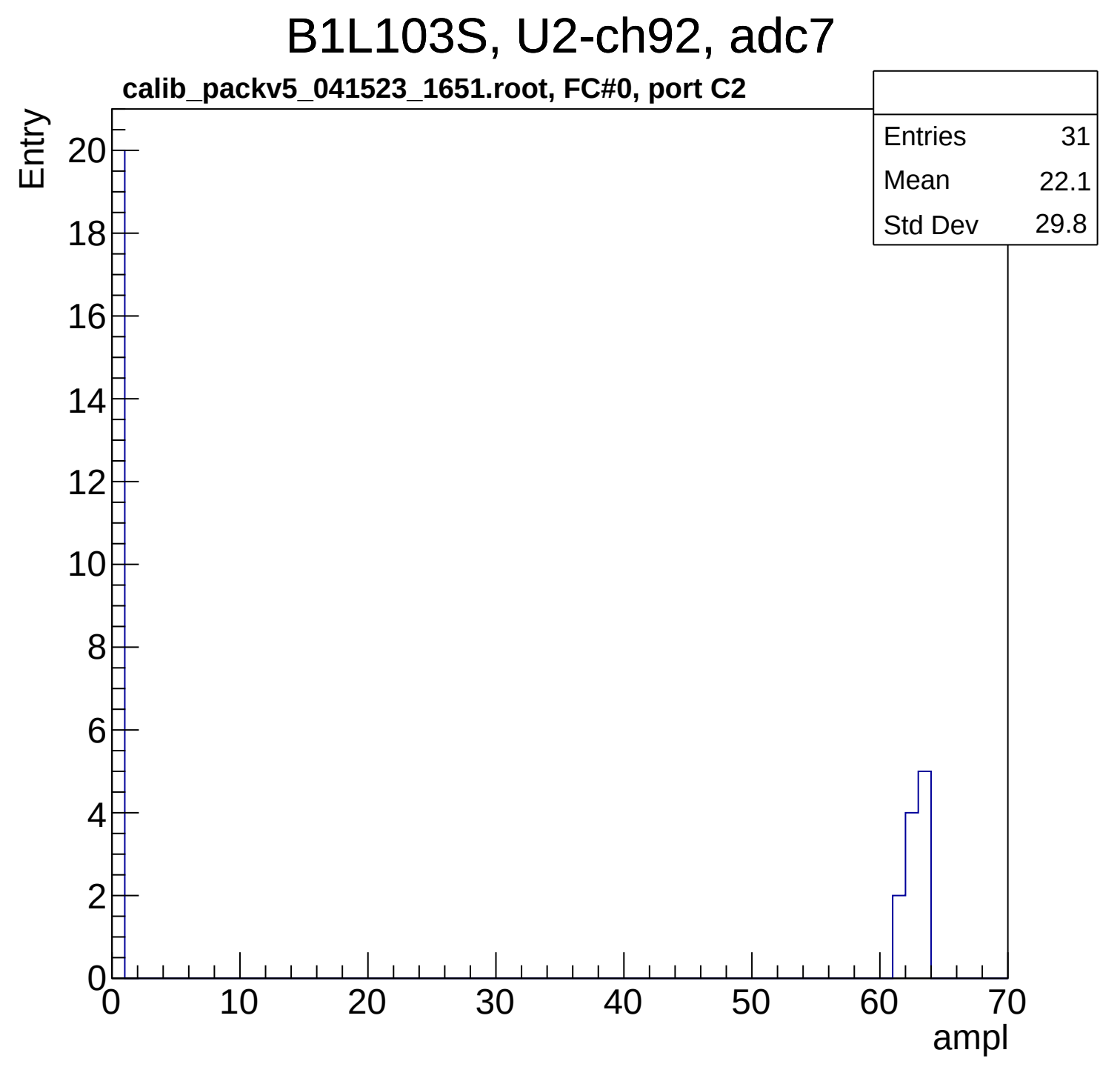

B1L103S, U2-ch92, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 38.54
Std Dev 5.838
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

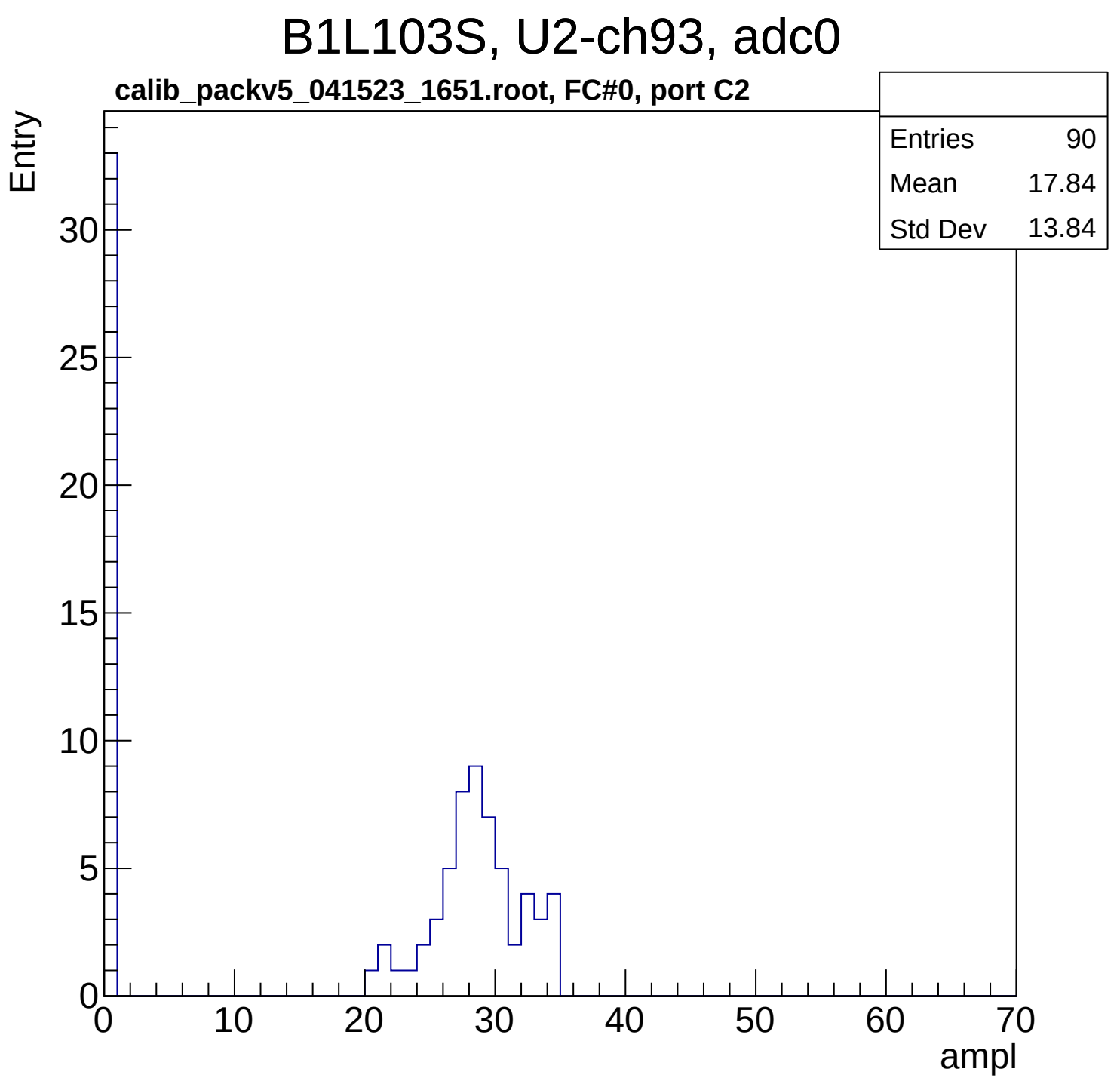

B1L103S, U2-ch92, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 44.54
Std Dev 6.808
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

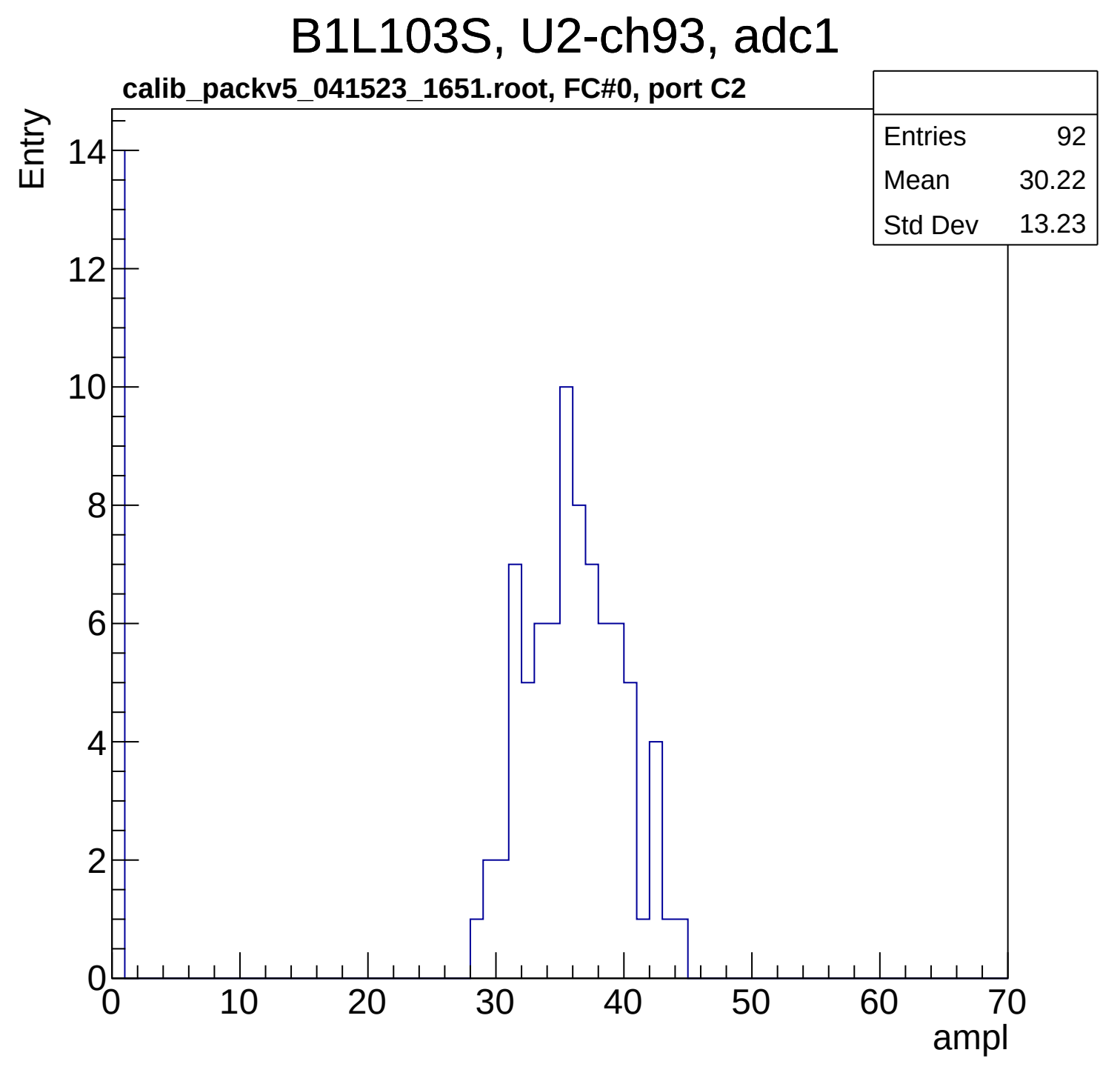

B1L103S, U2-ch92, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 50.94
Std Dev 3.302
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

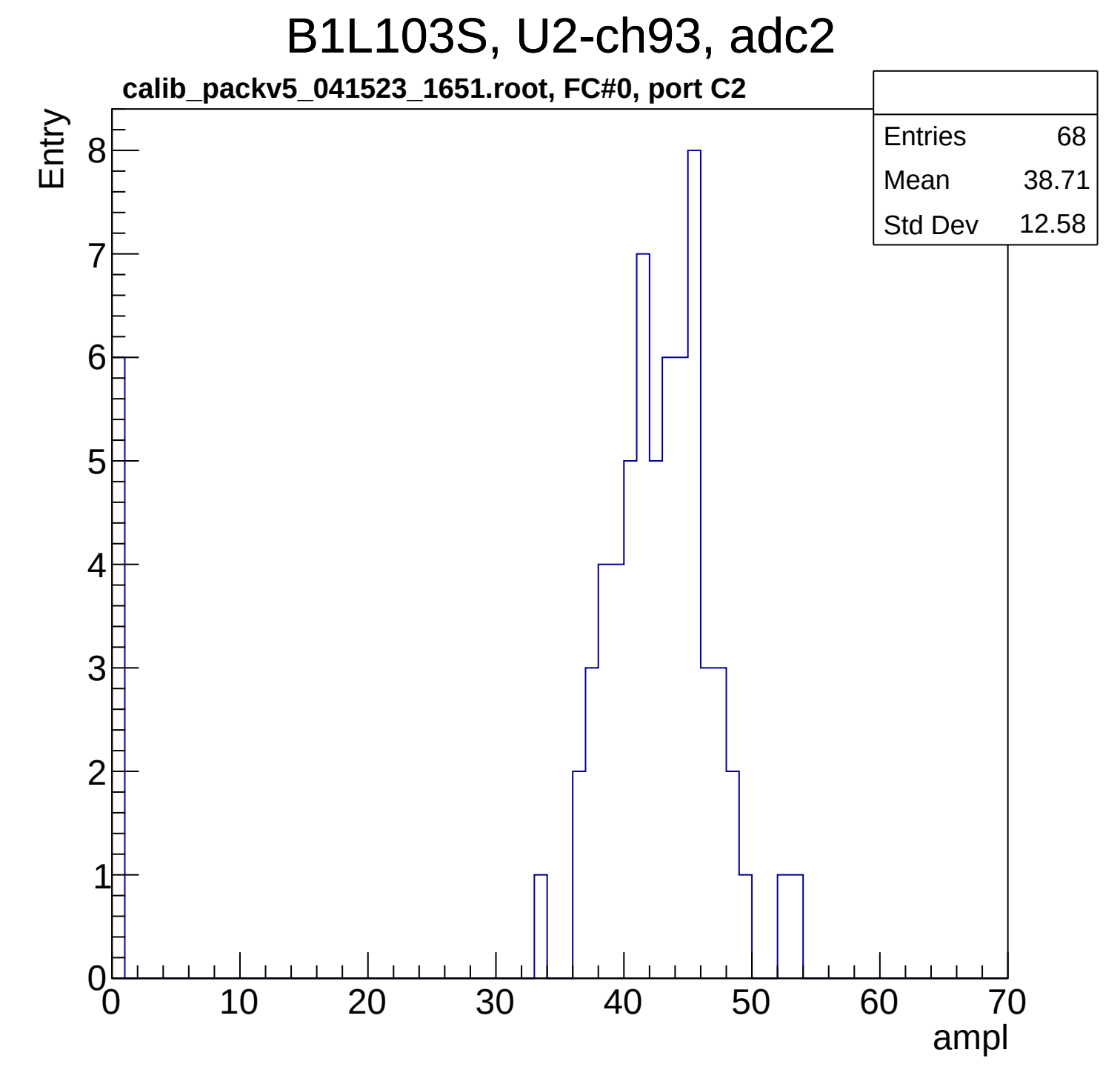

B1L103S, U2-ch92, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 56.84
Std Dev 3.484
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

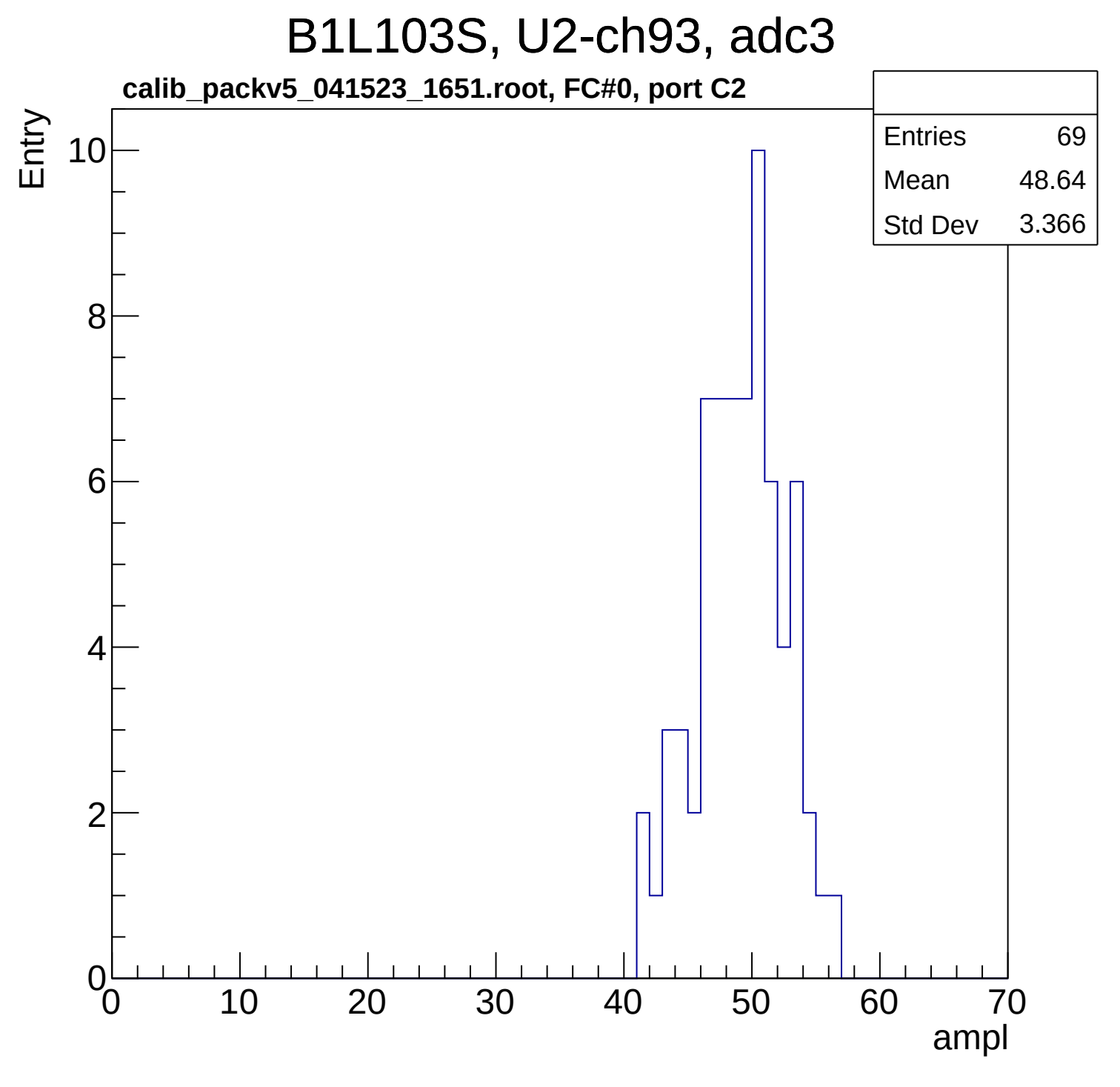

B1L103S, U2-ch92, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 60.21
Std Dev 2.041
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

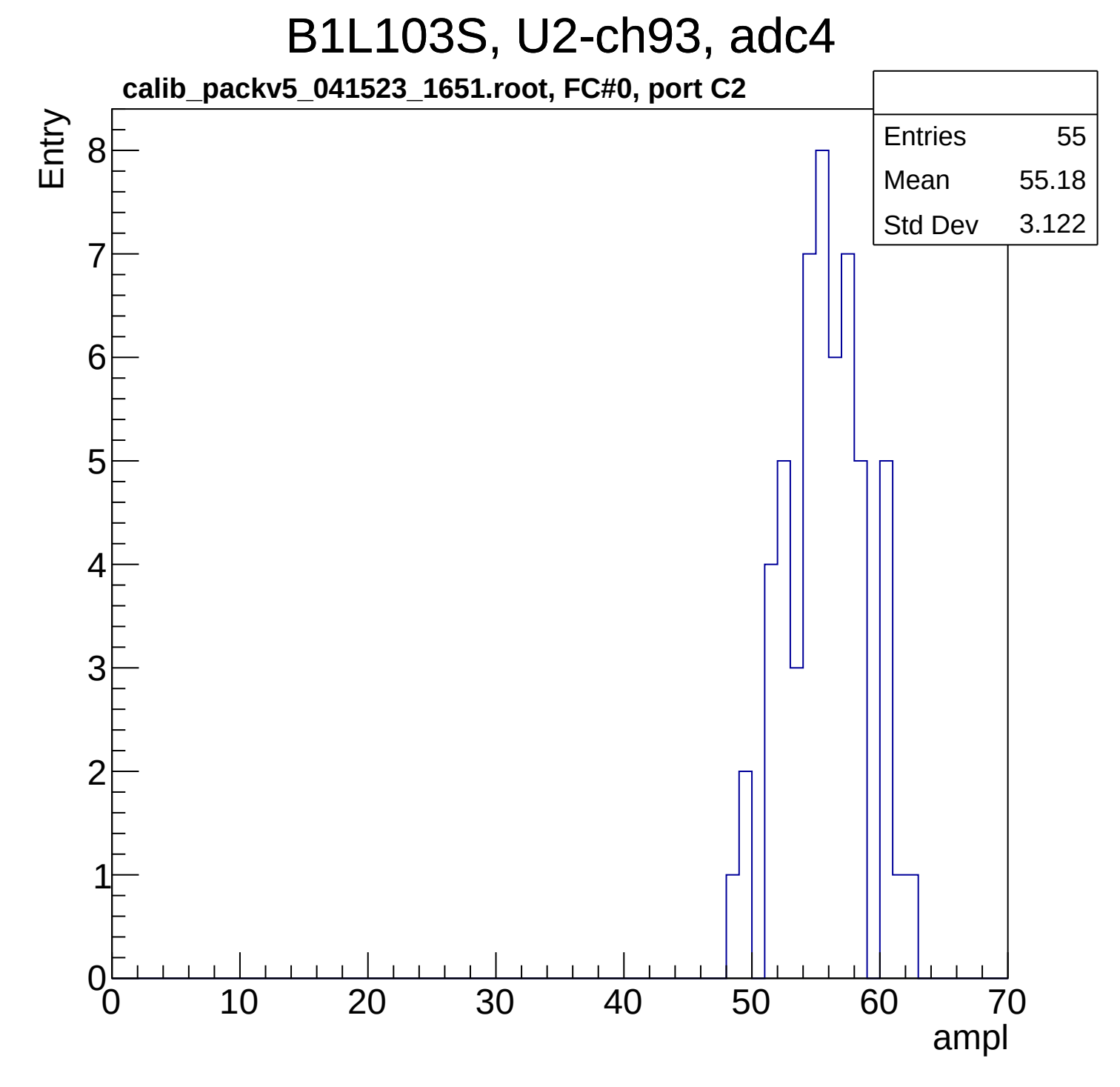

B1L103S, U2-ch92, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 22.1
Std Dev 29.8
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl

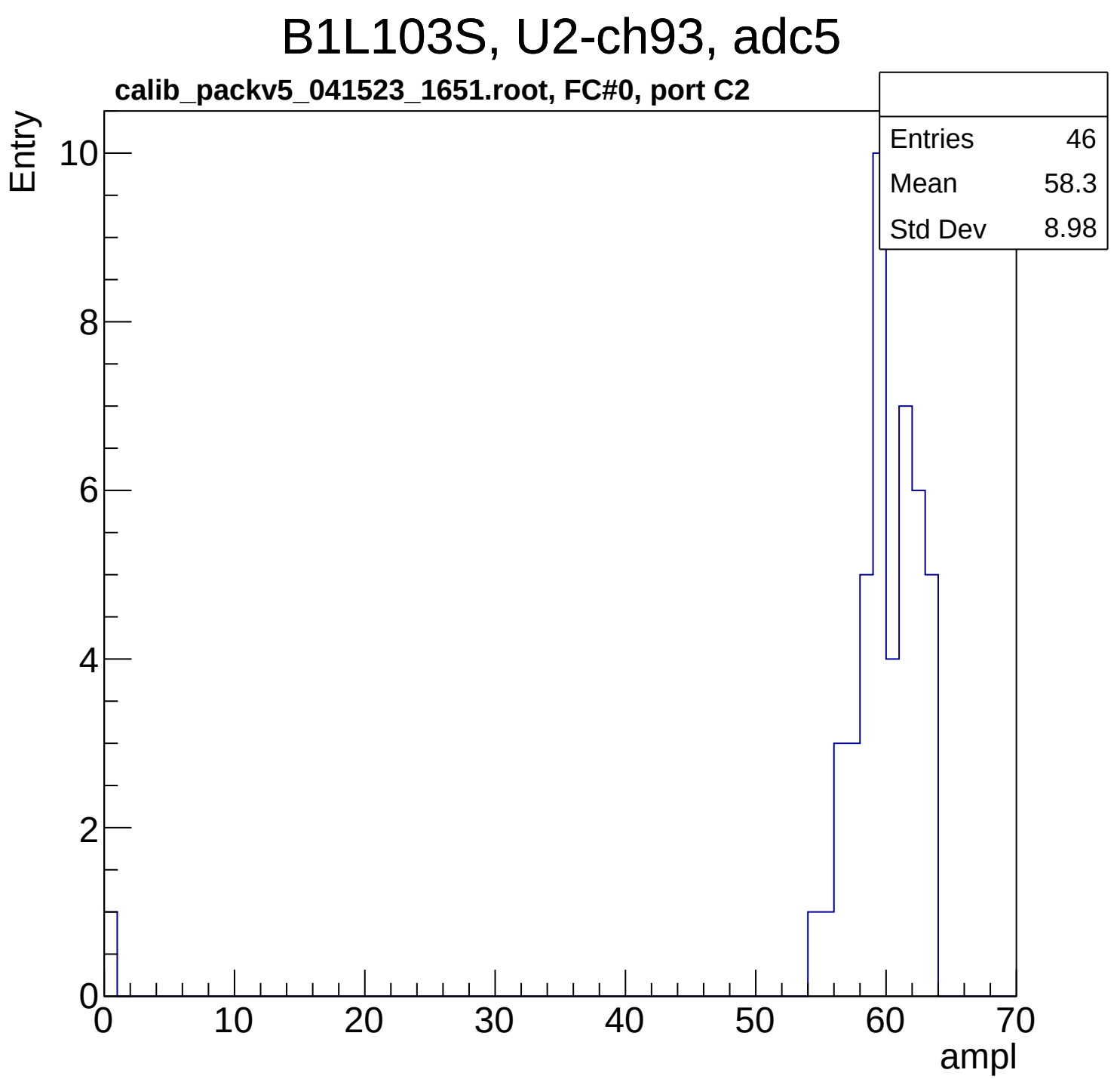

B1L103S, U2-ch93, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 17.84
Std Dev 13.84
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl

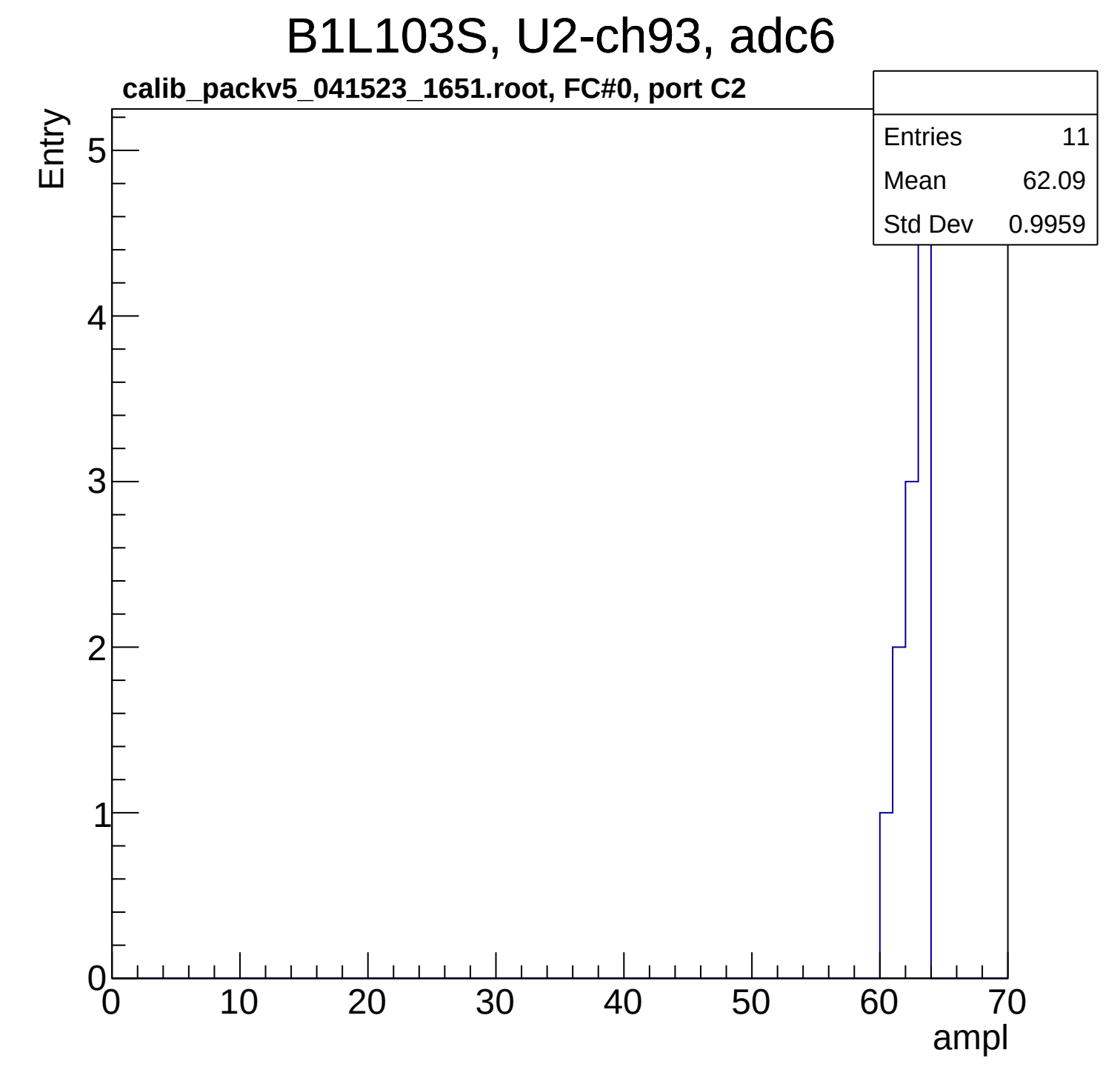

B1L103S, U2-ch93, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 30.22
Std Dev 13.23
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

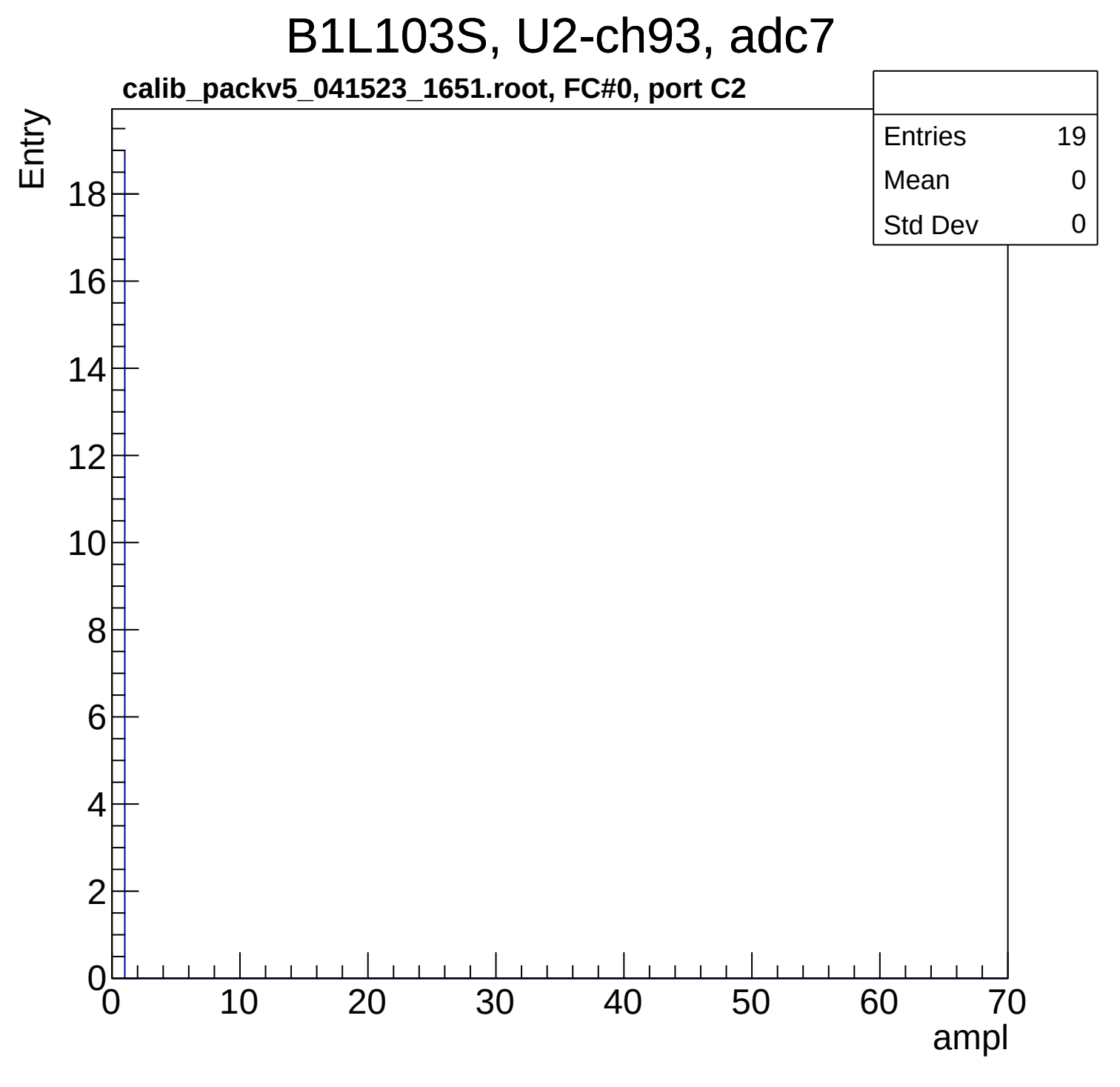

B1L103S, U2-ch93, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 38.71
Std Dev 12.58
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

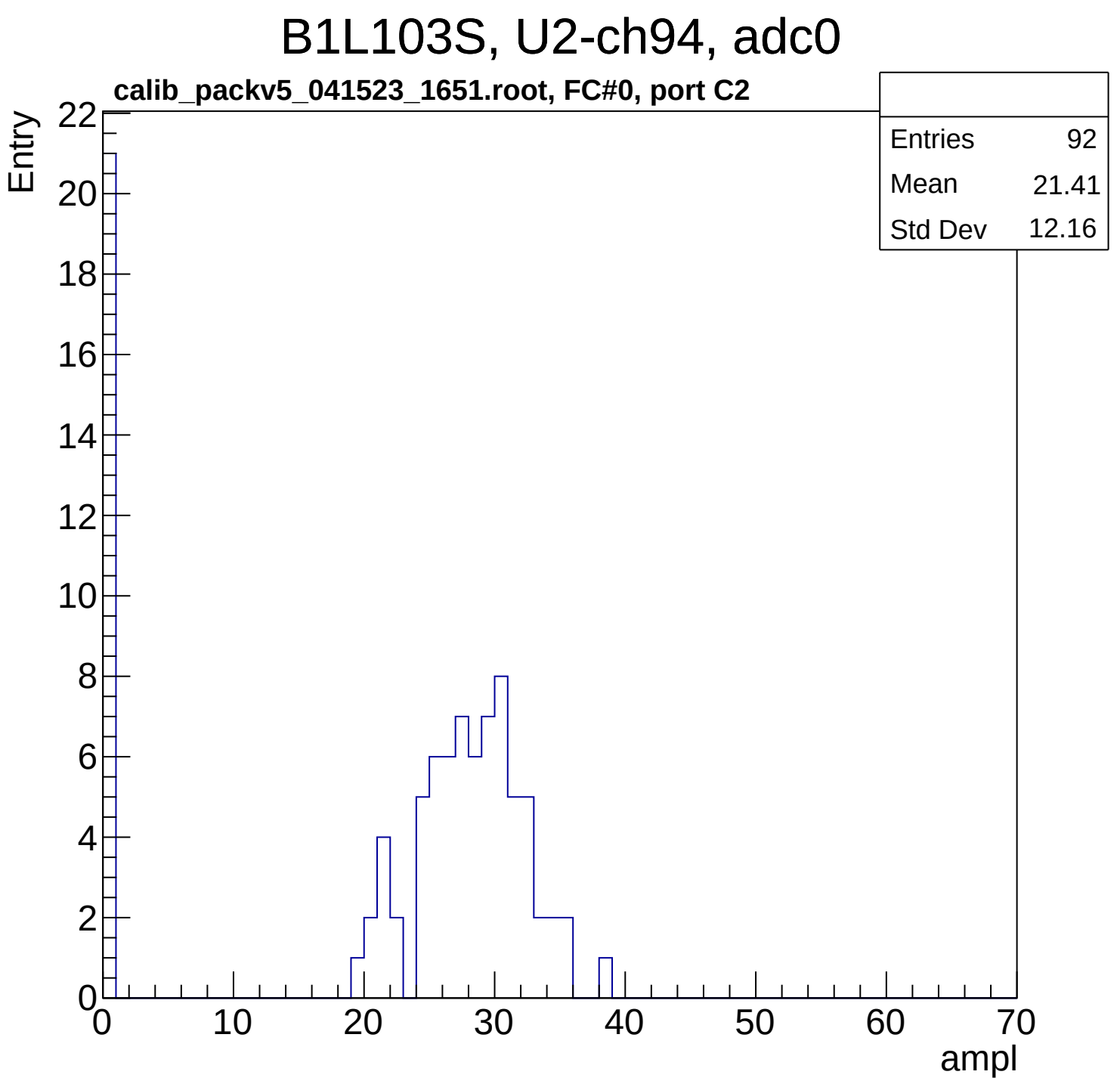

B1L103S, U2-ch93, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 48.64
Std Dev 3.366
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

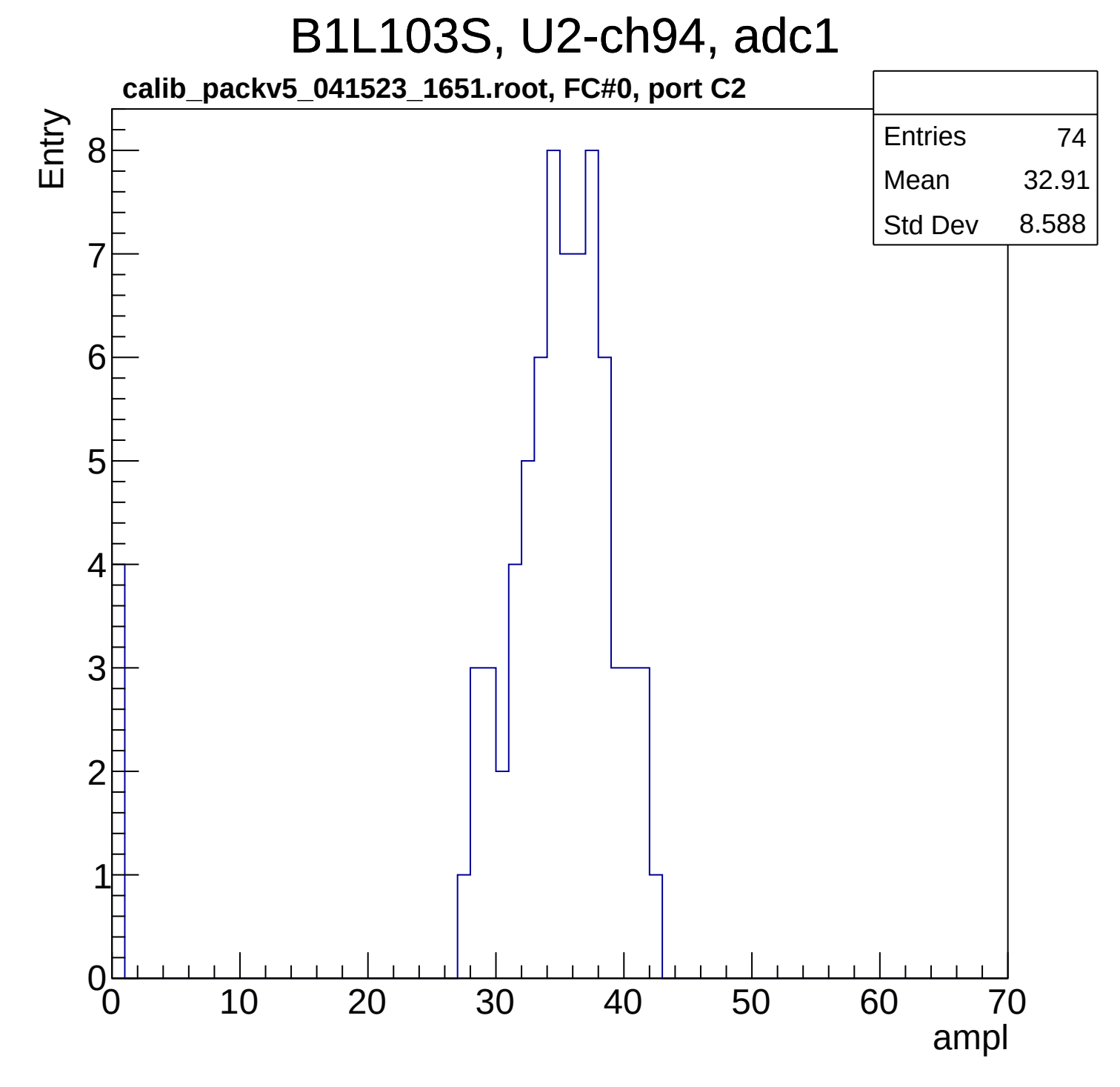

B1L103S, U2-ch93, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 55.18
Std Dev 3.122
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

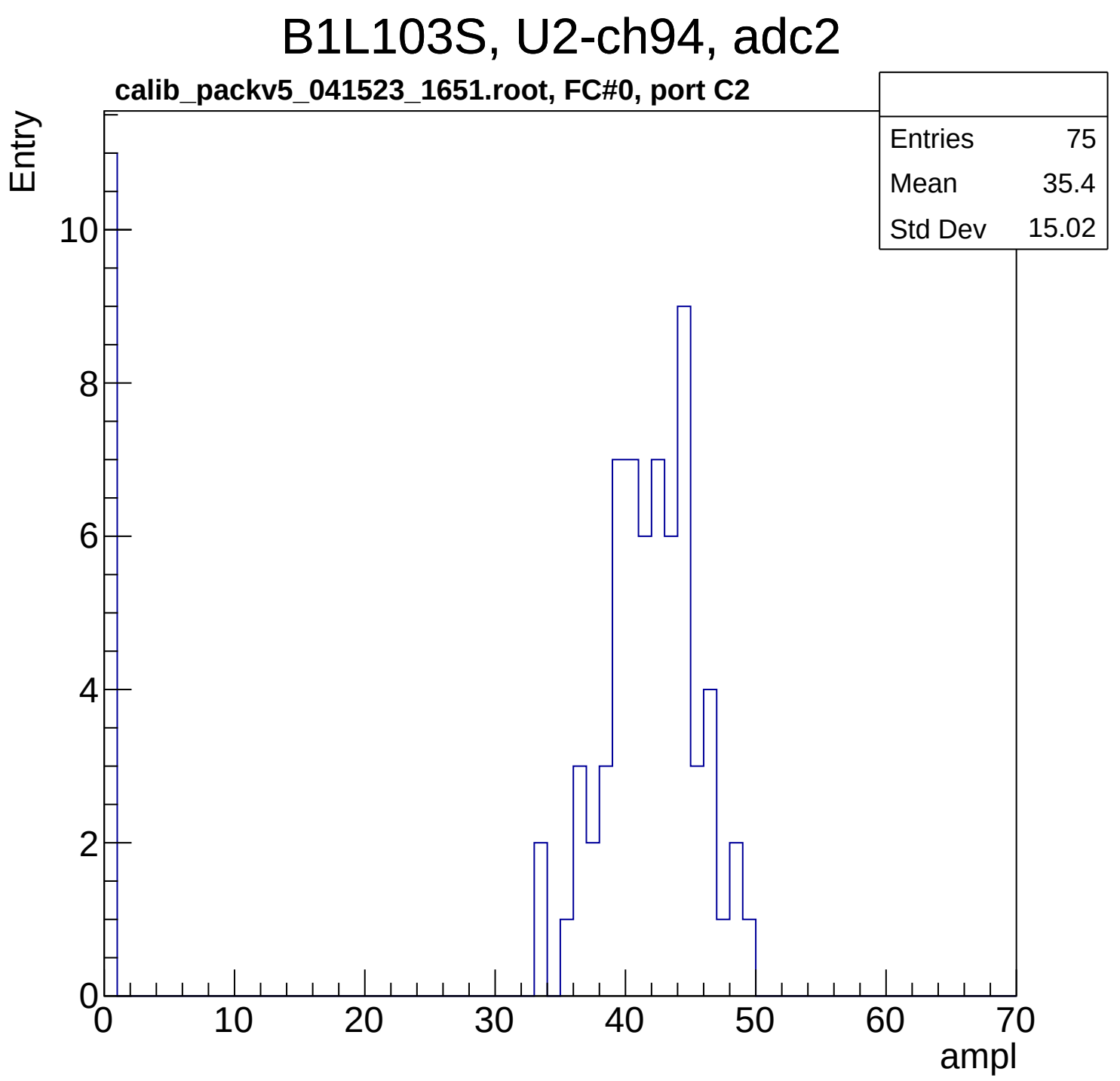

B1L103S, U2-ch93, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.3
Std Dev 8.98
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

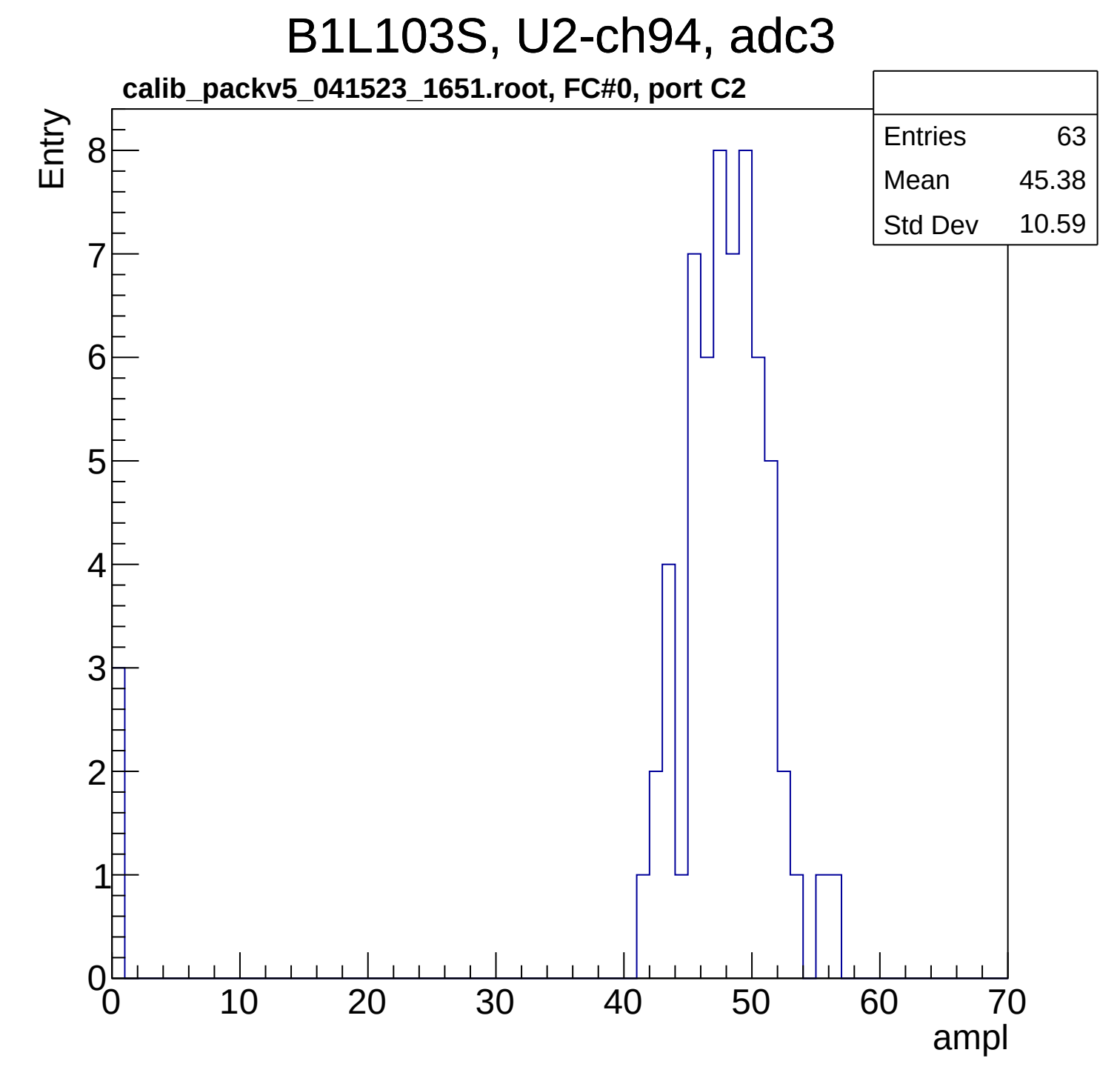

B1L103S, U2-ch93, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 62.09
Std Dev 0.9959
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

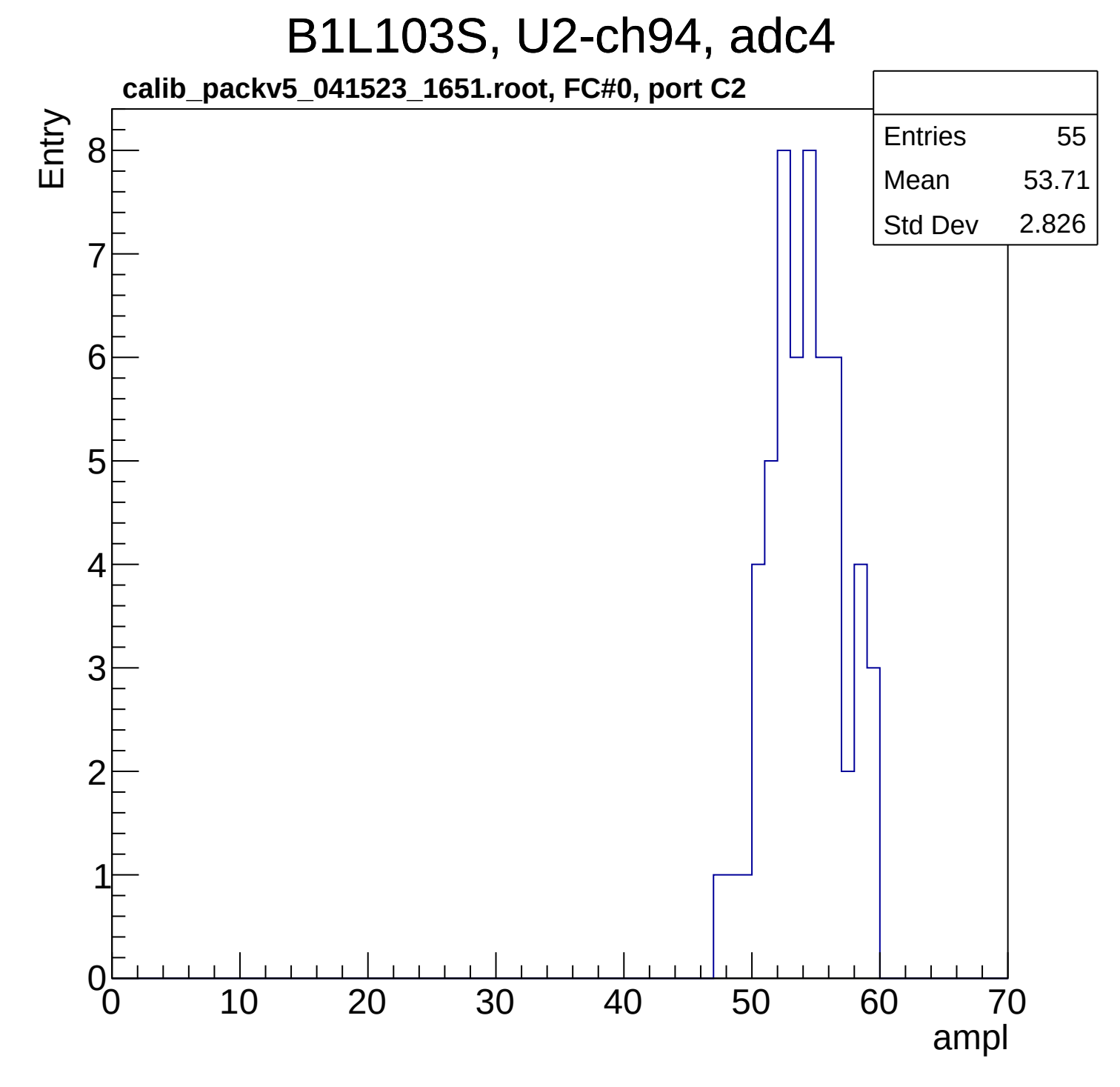

B1L103S, U2-ch93, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

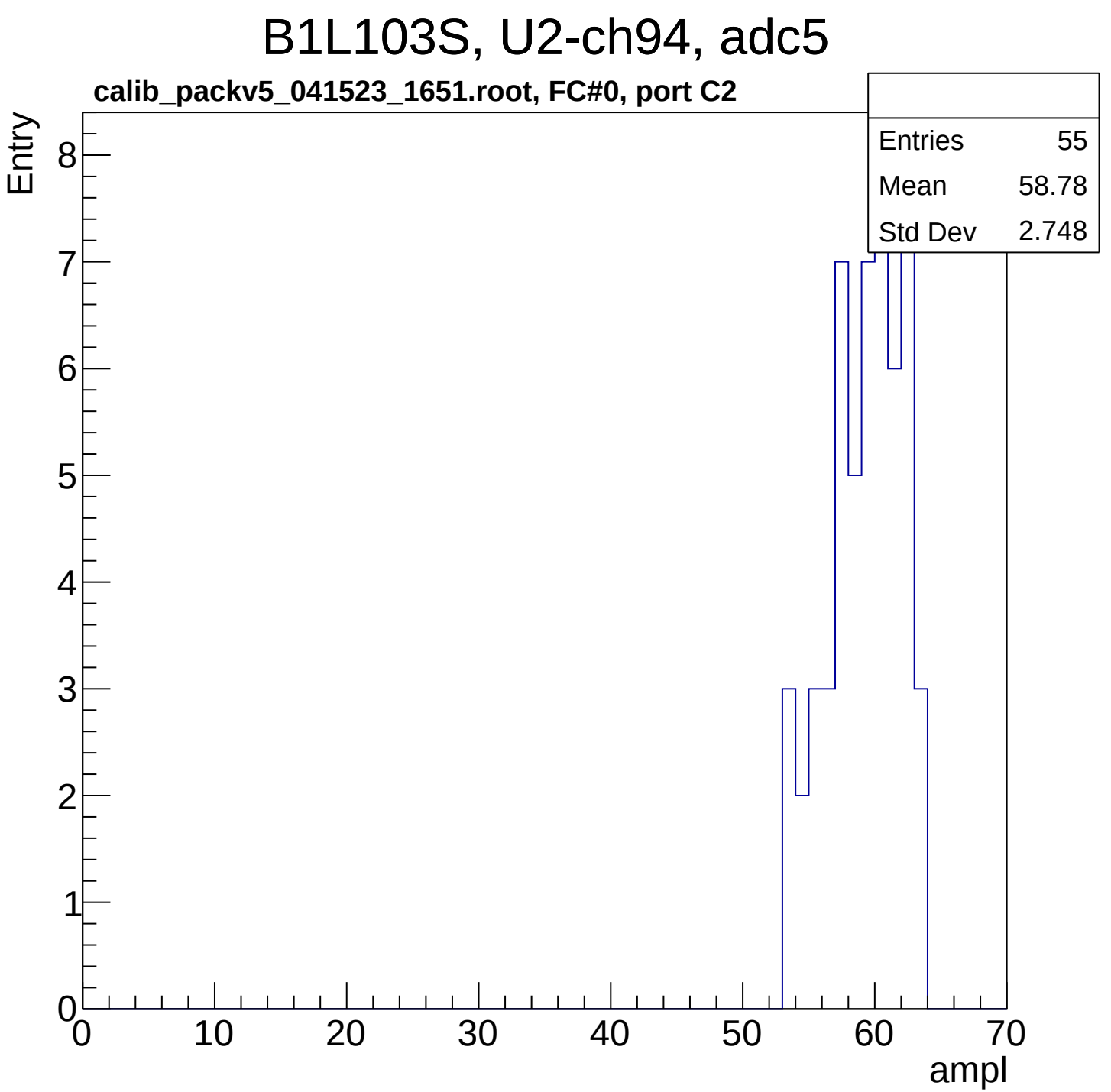

B1L103S, U2-ch94, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 21.41
Std Dev 12.16
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70

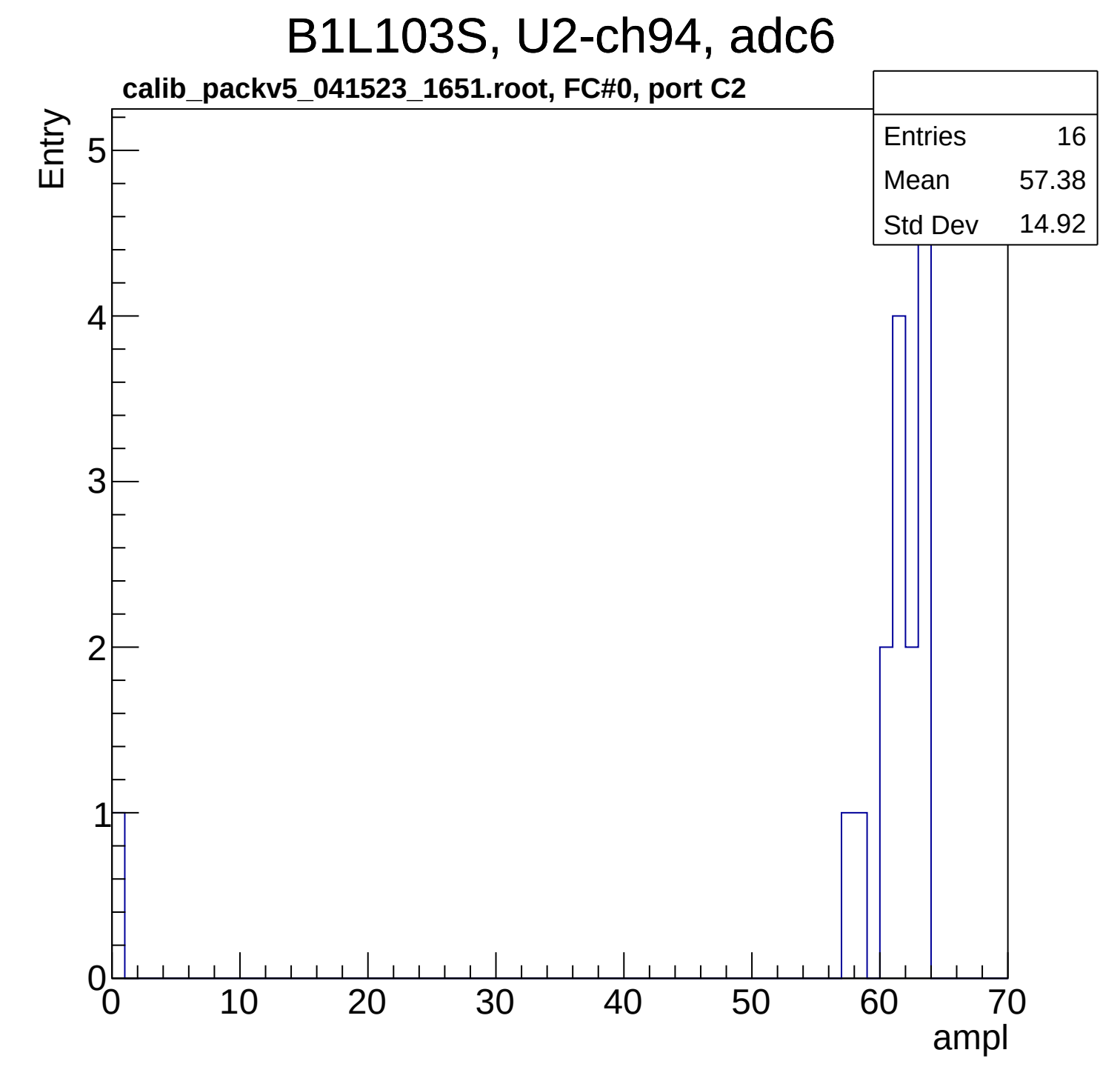

B1L103S, U2-ch94, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 32.91
Std Dev 8.588
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

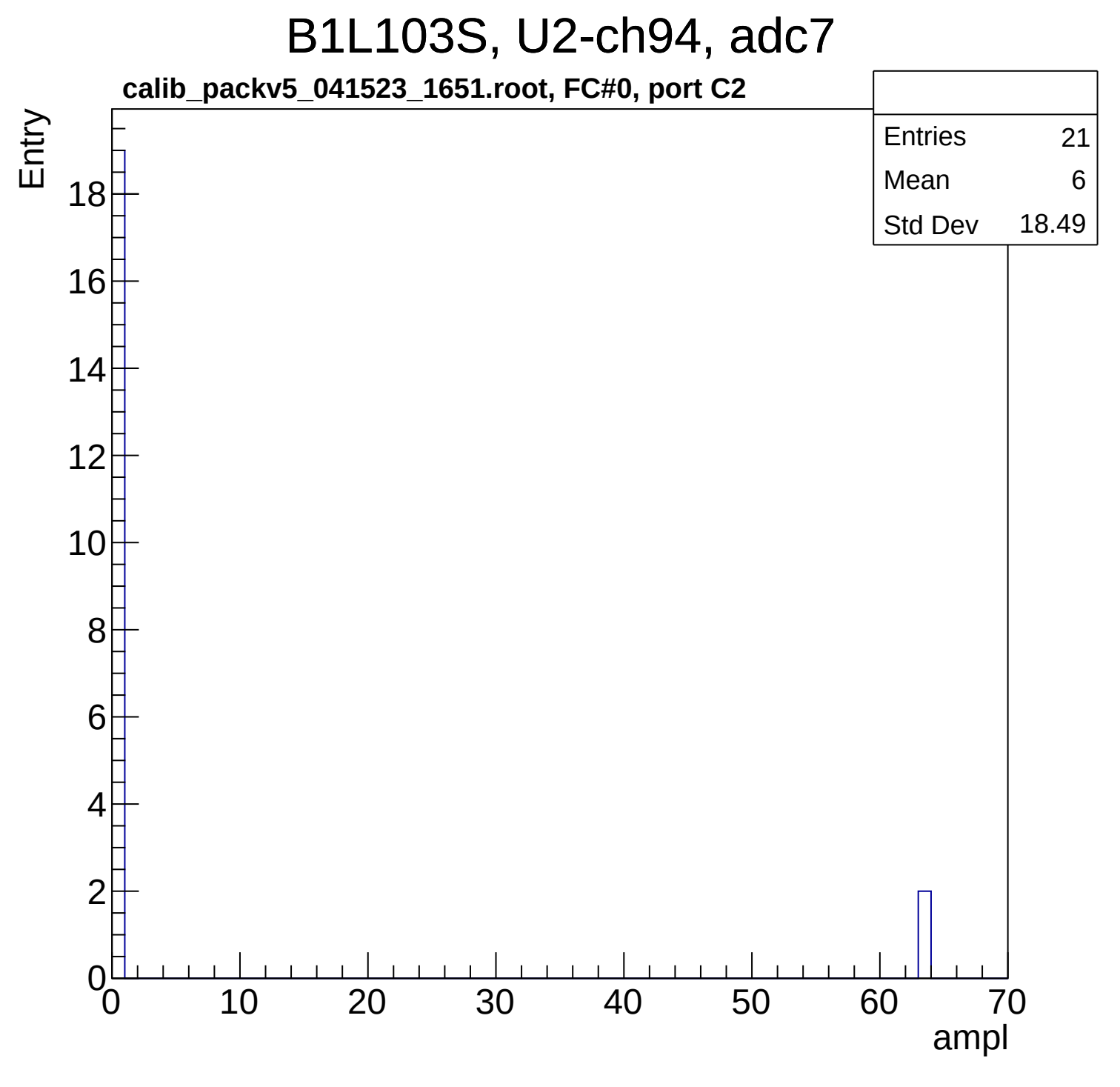

B1L103S, U2-ch94, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 35.4
Std Dev 15.02
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

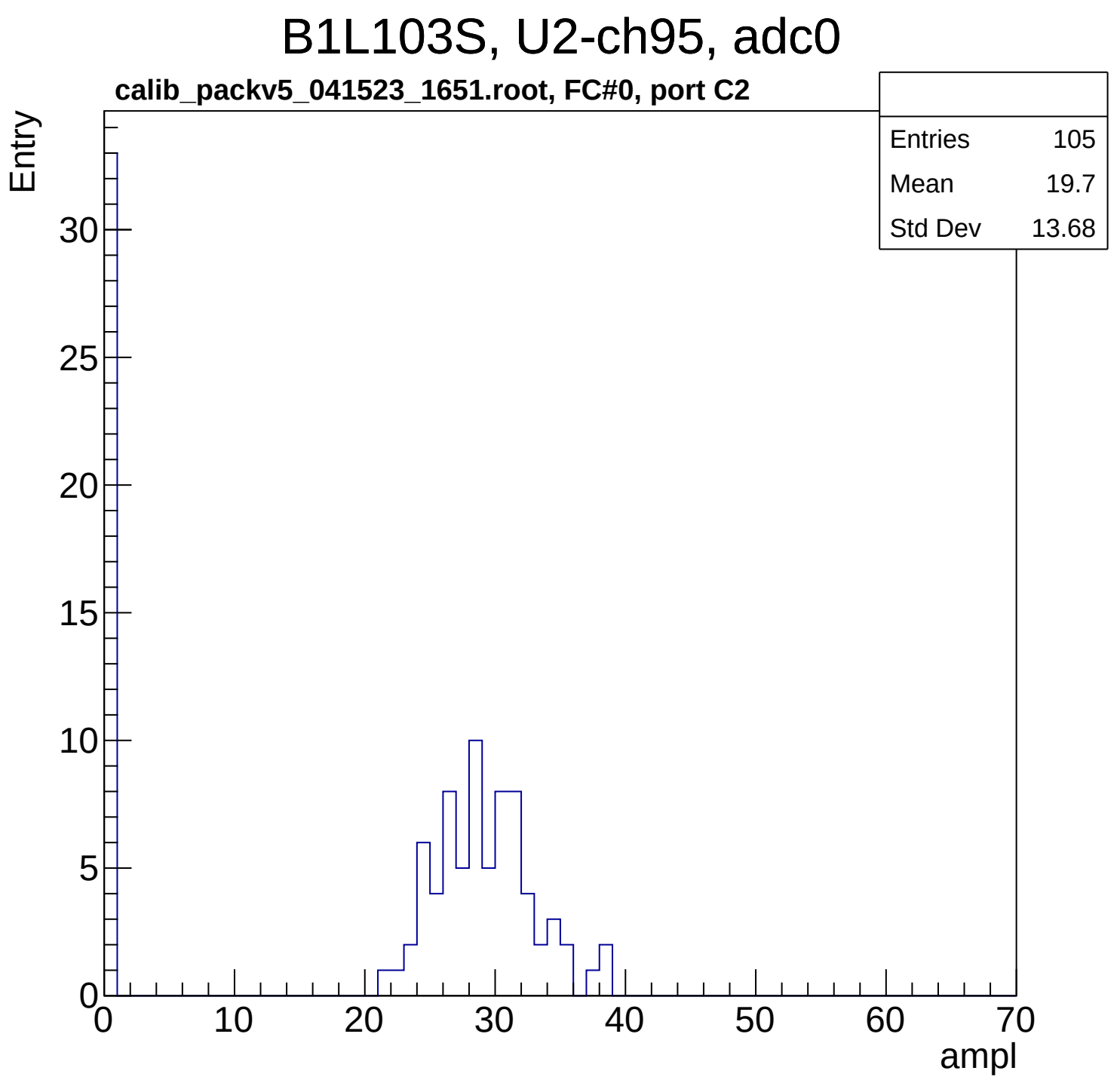

B1L103S, U2-ch94, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 45.38
Std Dev 10.59
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

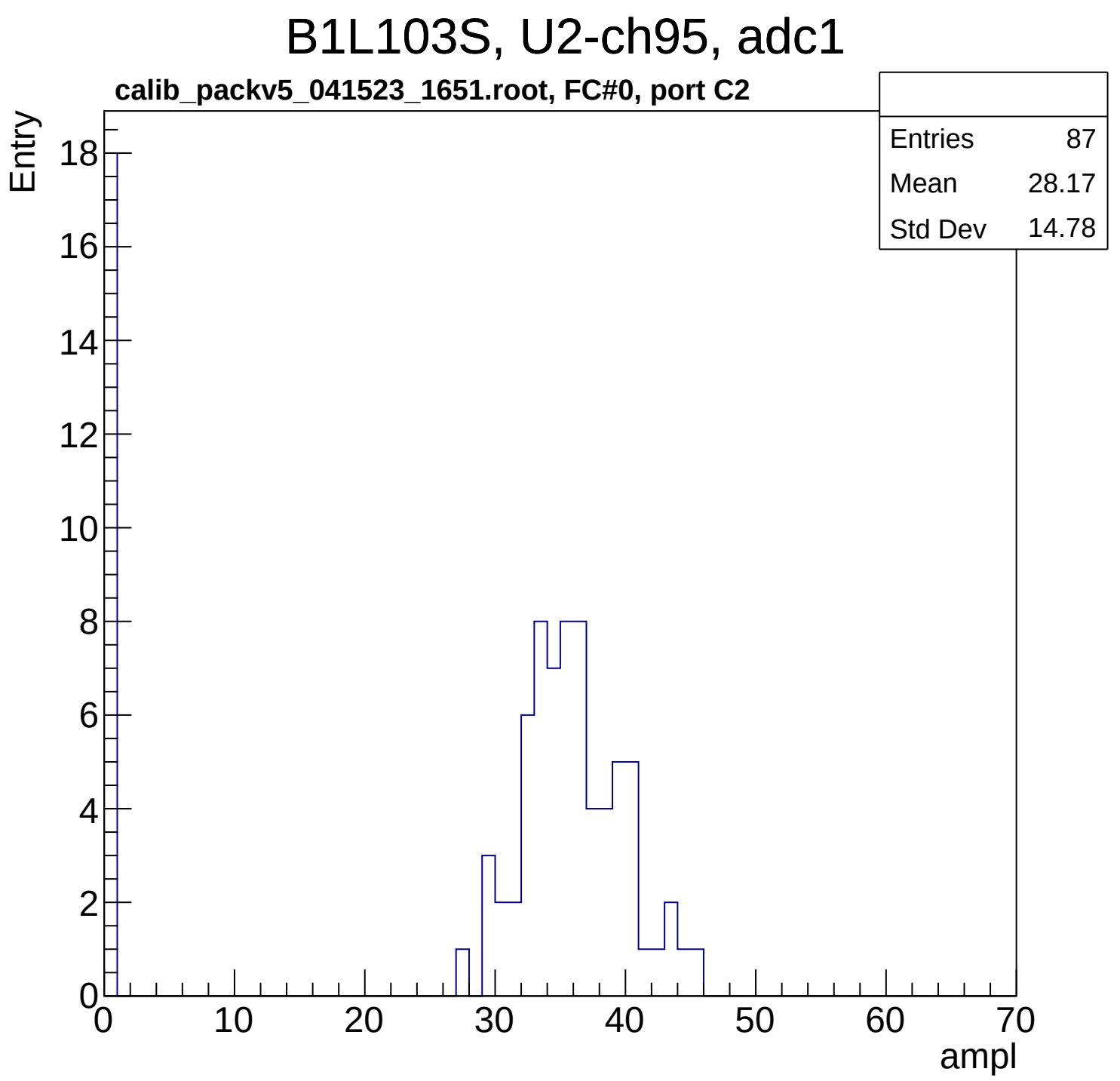

B1L103S, U2-ch94, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 53.71
Std Dev 2.826
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

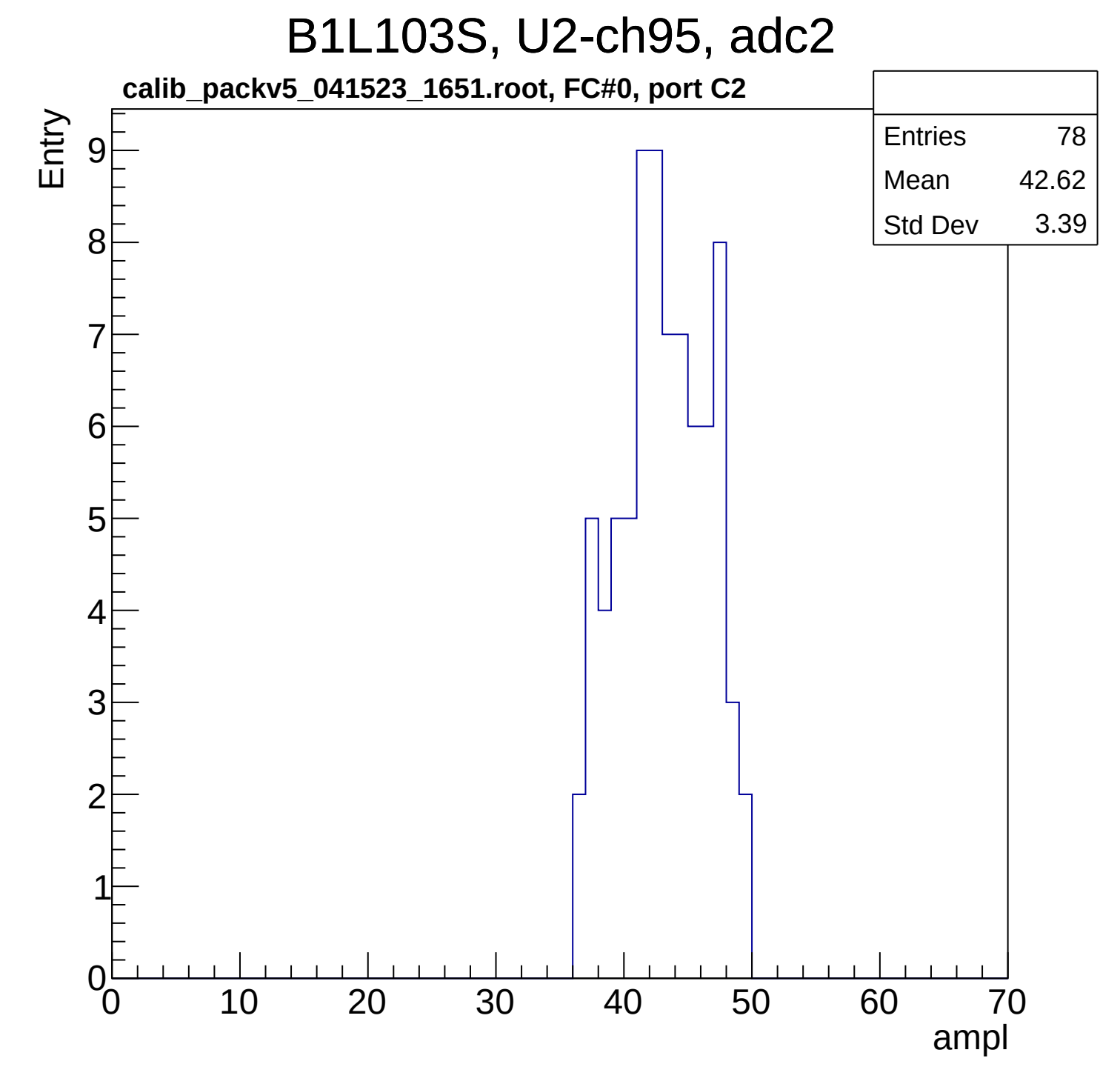

B1L103S, U2-ch94, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.78
Std Dev 2.748
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

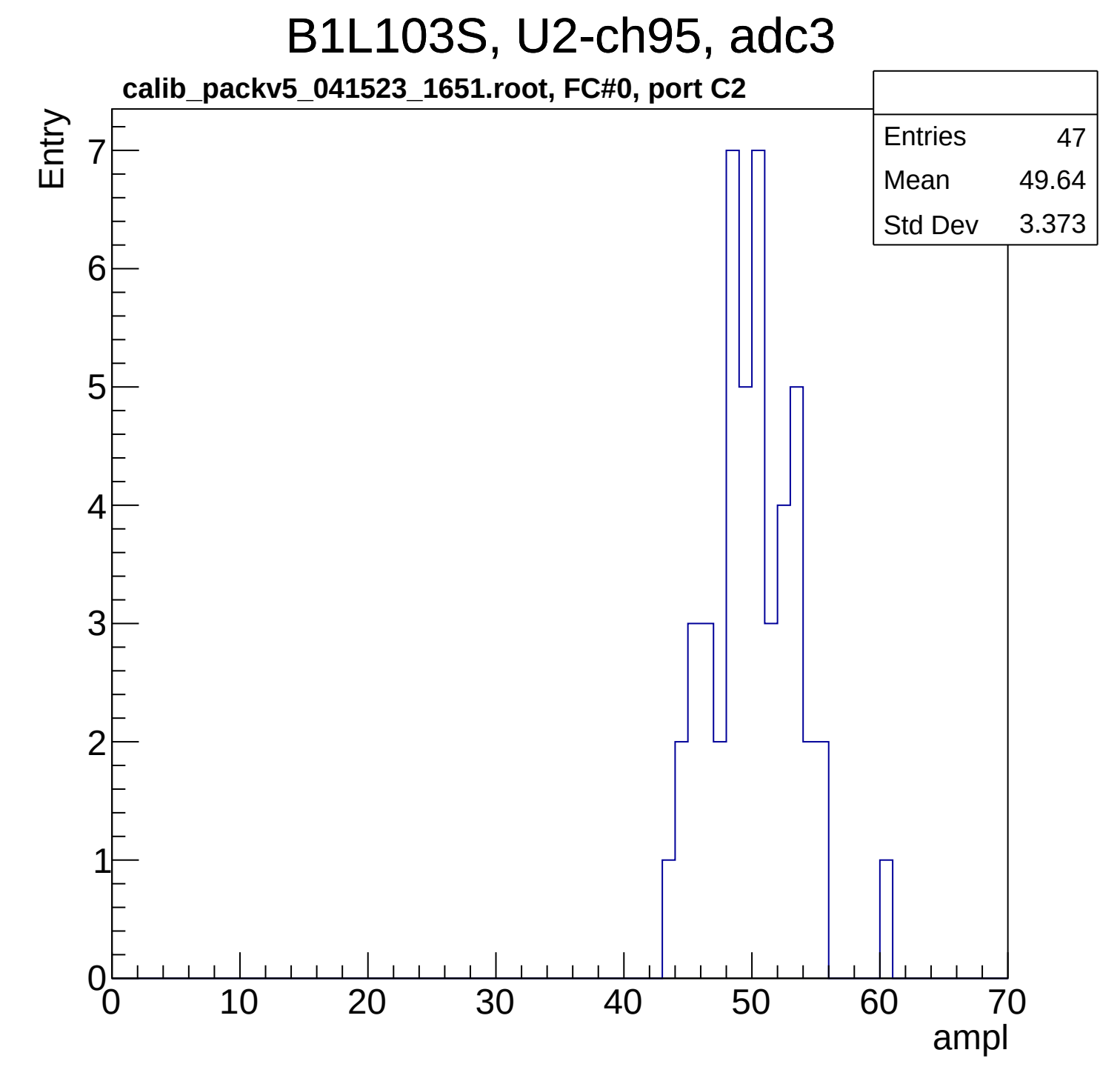

B1L103S, U2-ch94, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.38
Std Dev 14.92
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

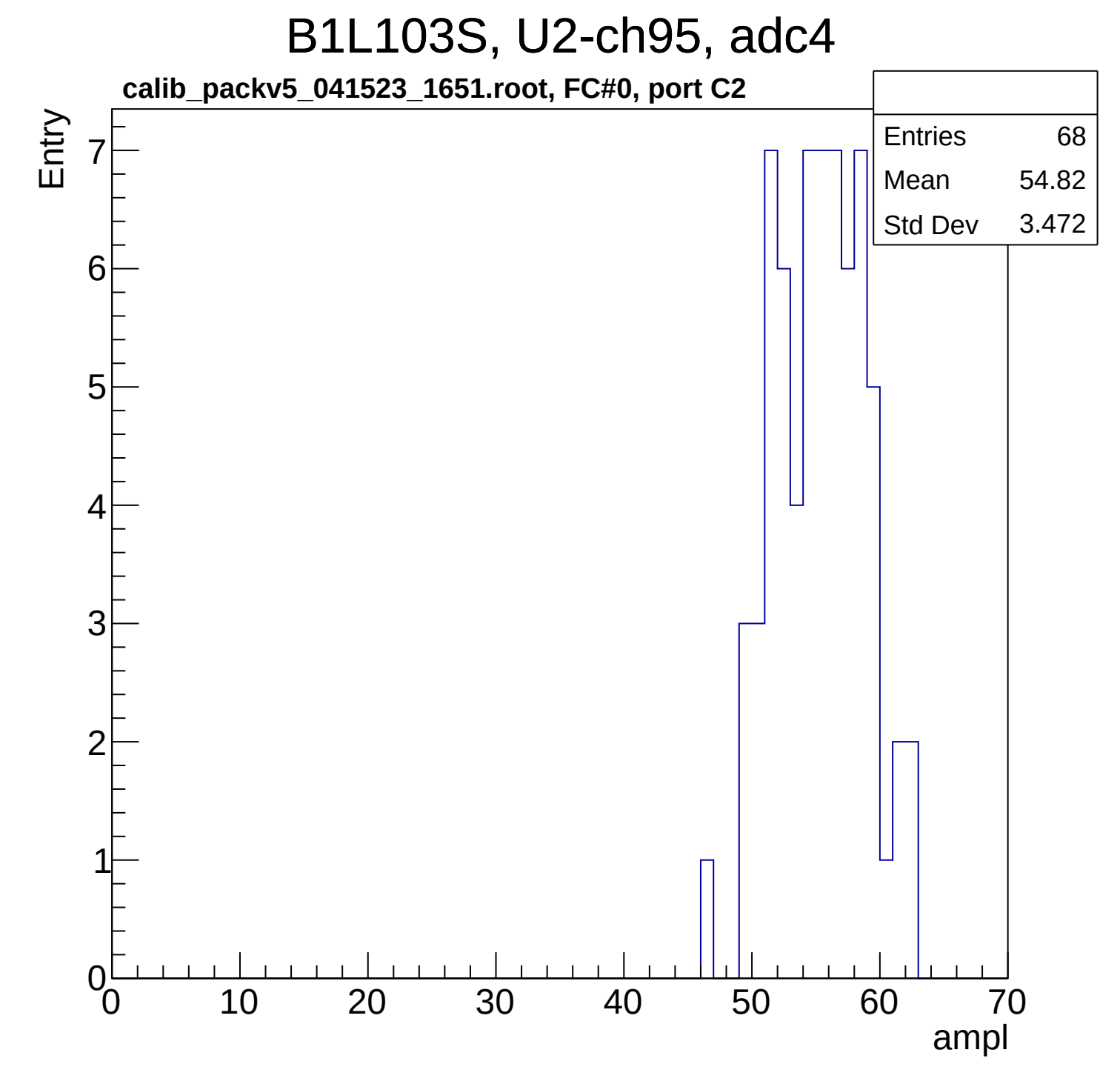

B1L103S, U2-ch94, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

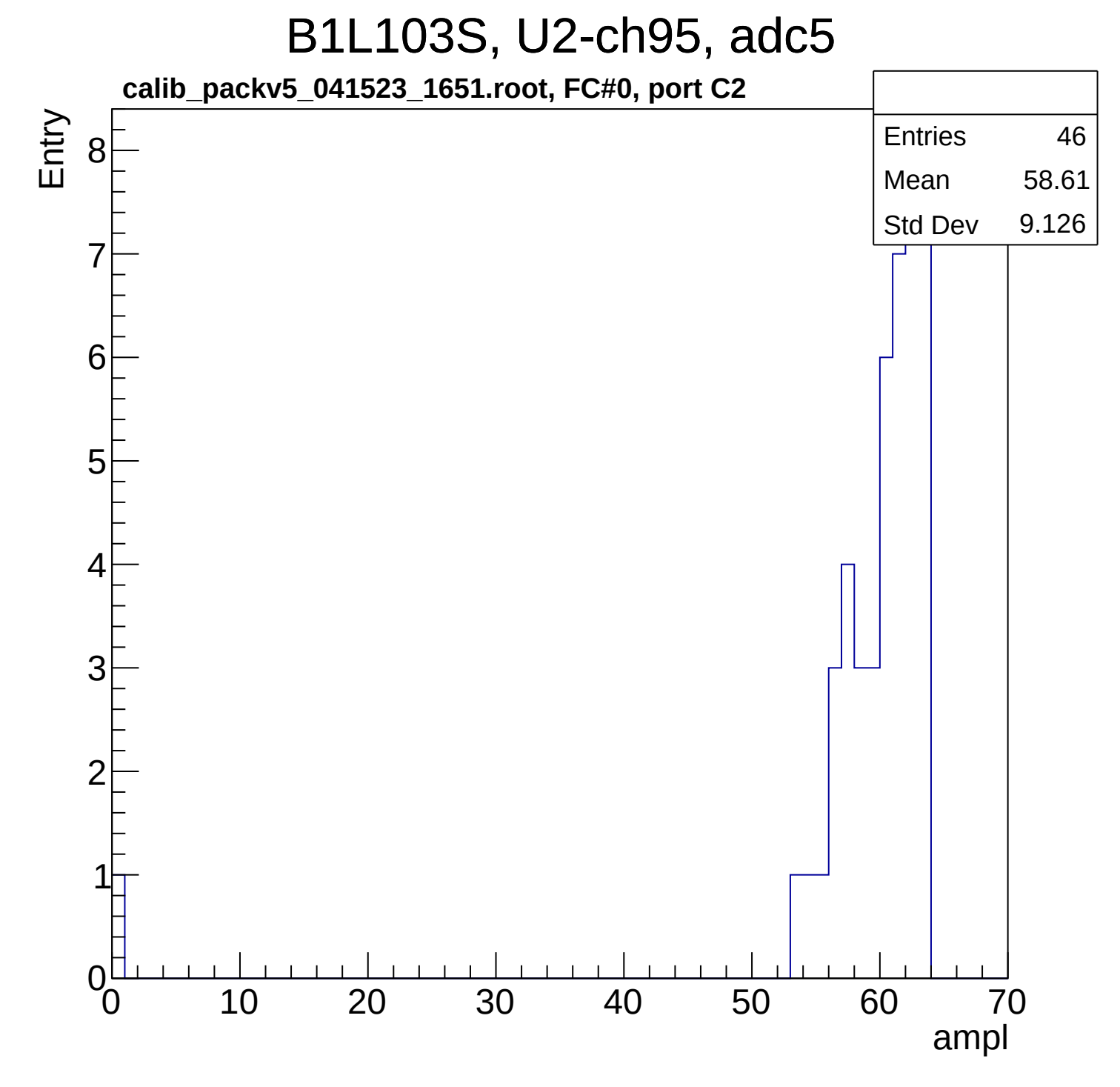

B1L103S, U2-ch95, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 105
Mean 19.7
Std Dev 13.68
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl

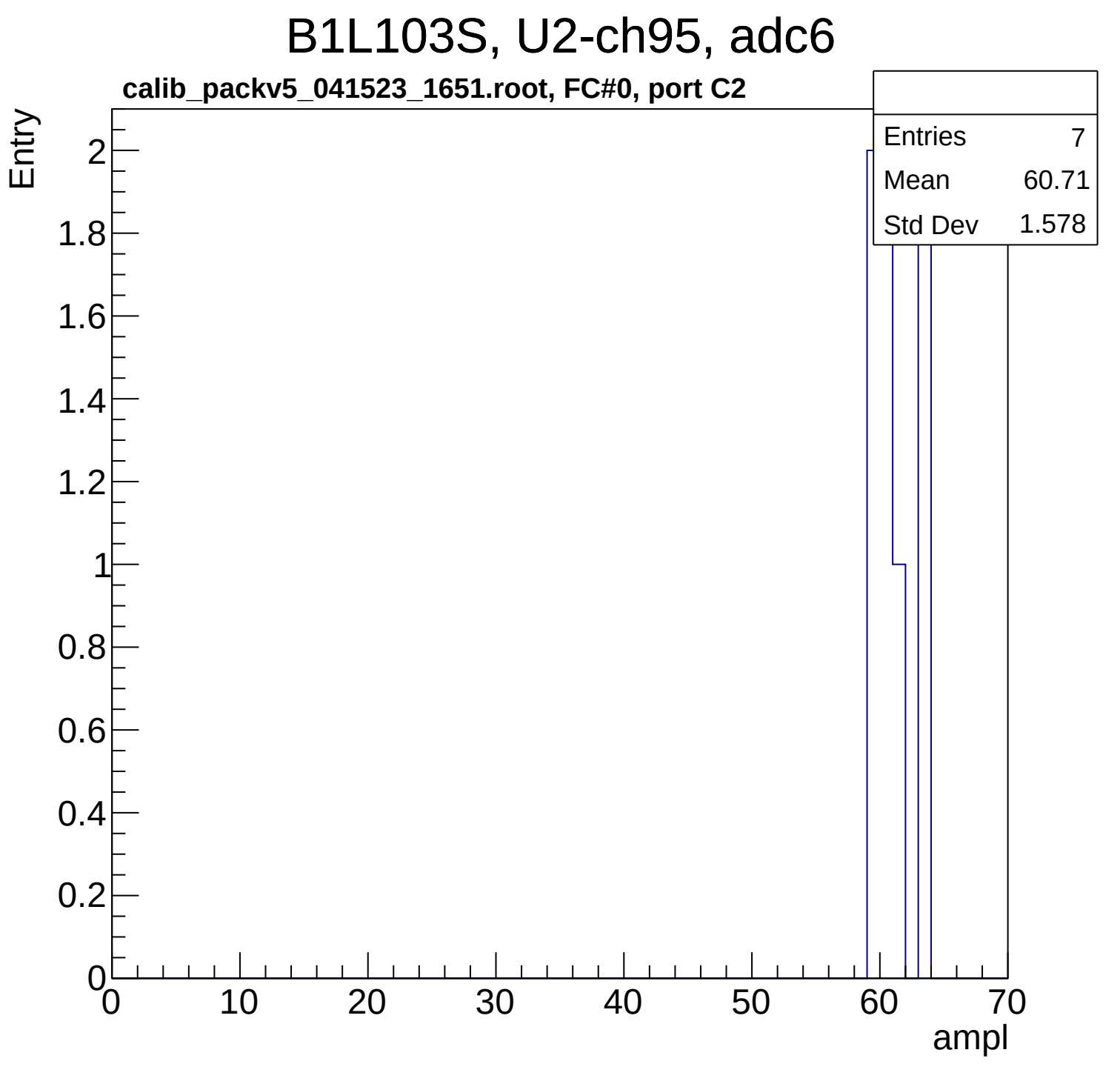

B1L103S, U2-ch95, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 28.17
Std Dev 14.78
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

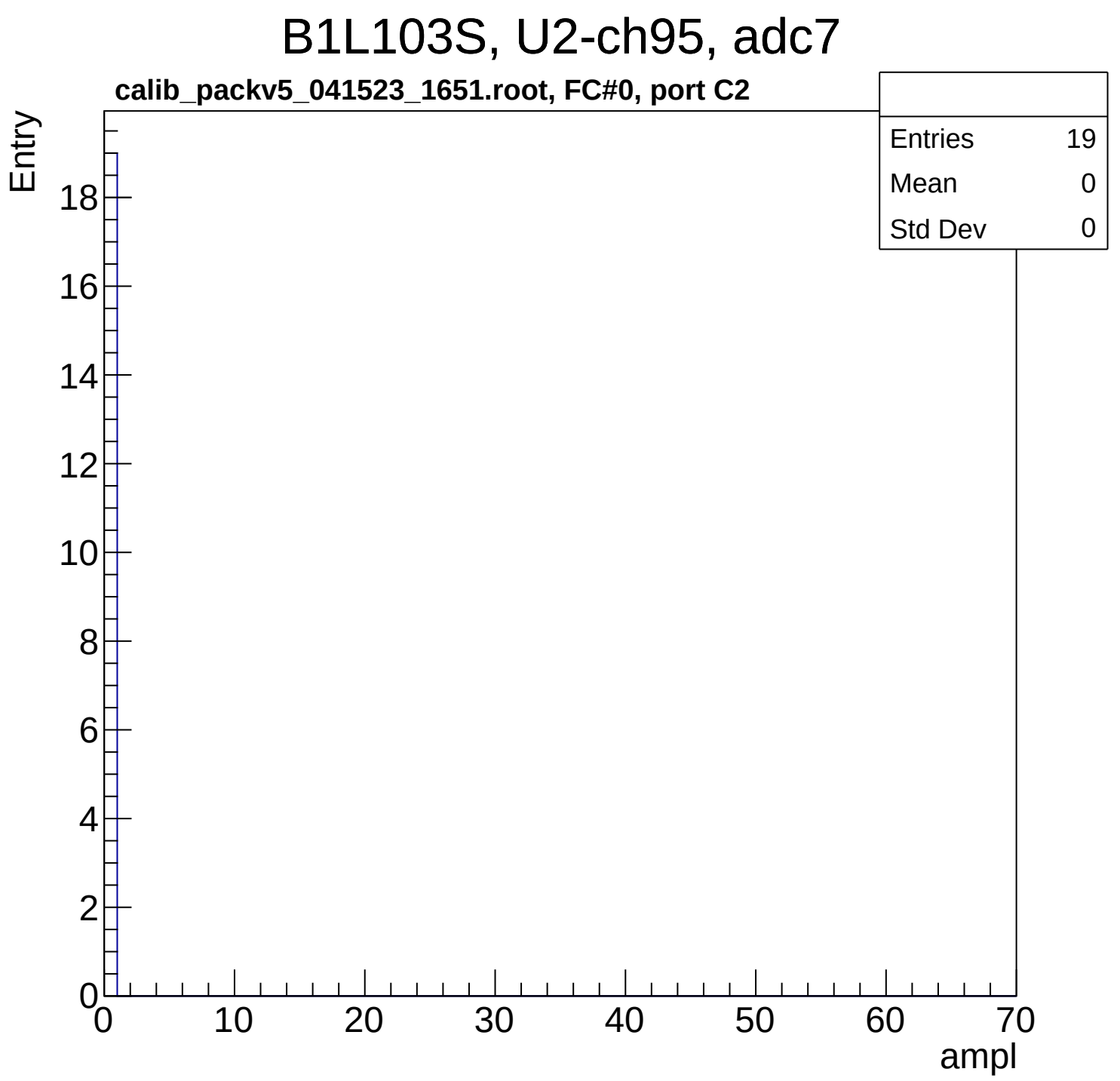

B1L103S, U2-ch95, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 42.62
Std Dev 3.39
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

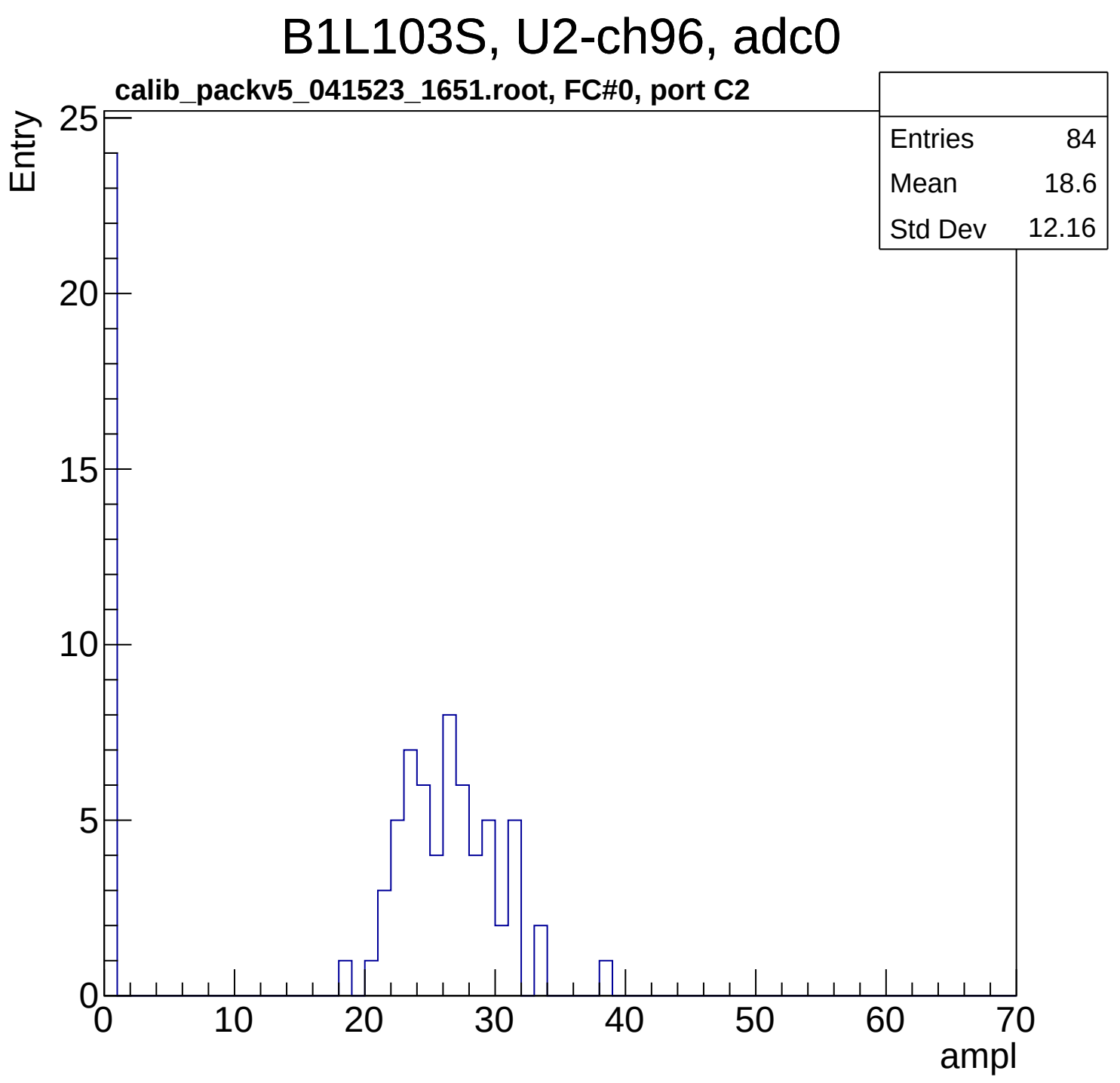

B1L103S, U2-ch95, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 49.64
Std Dev 3.373
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

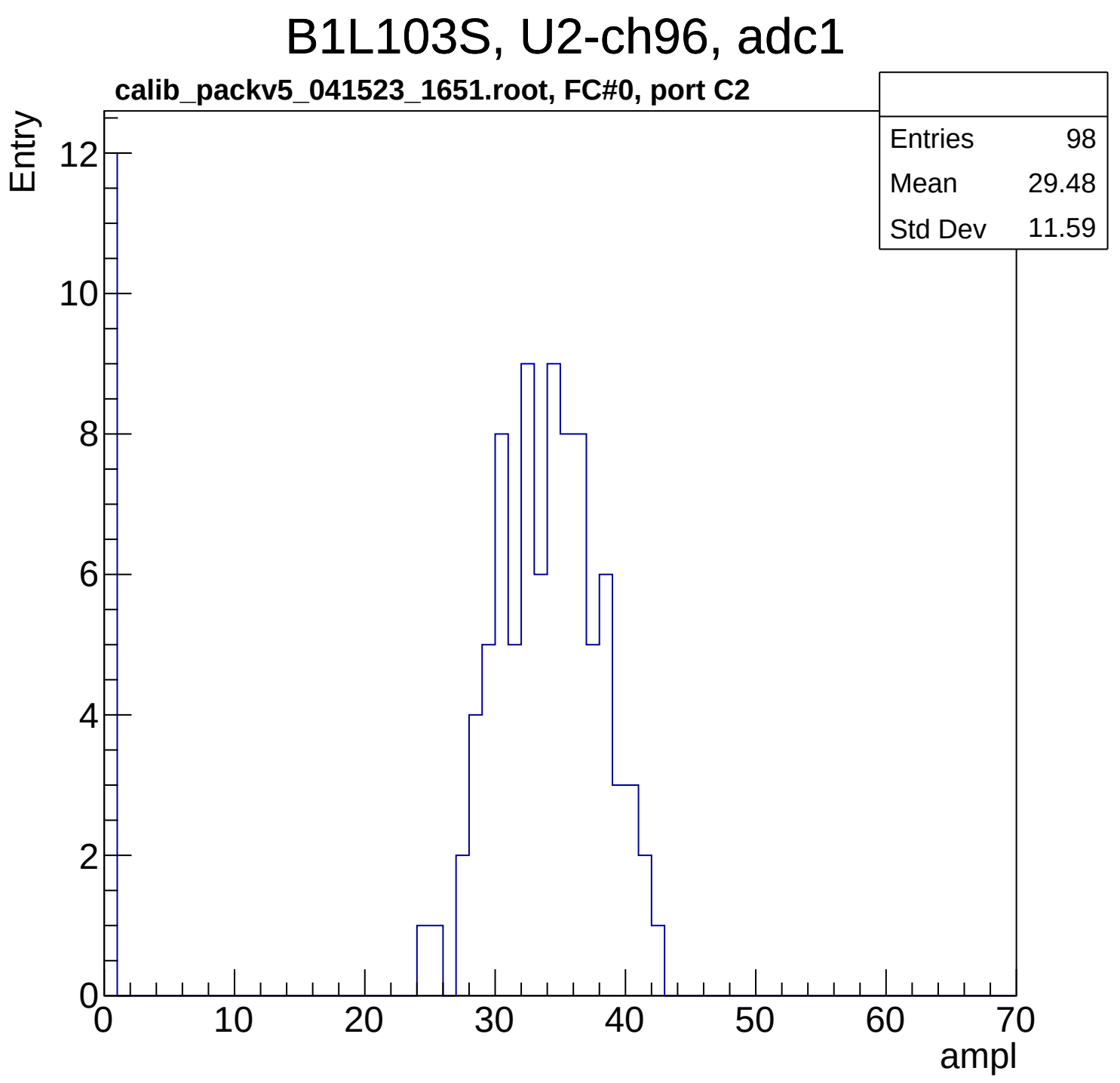

B1L103S, U2-ch95, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 54.82
Std Dev 3.472
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

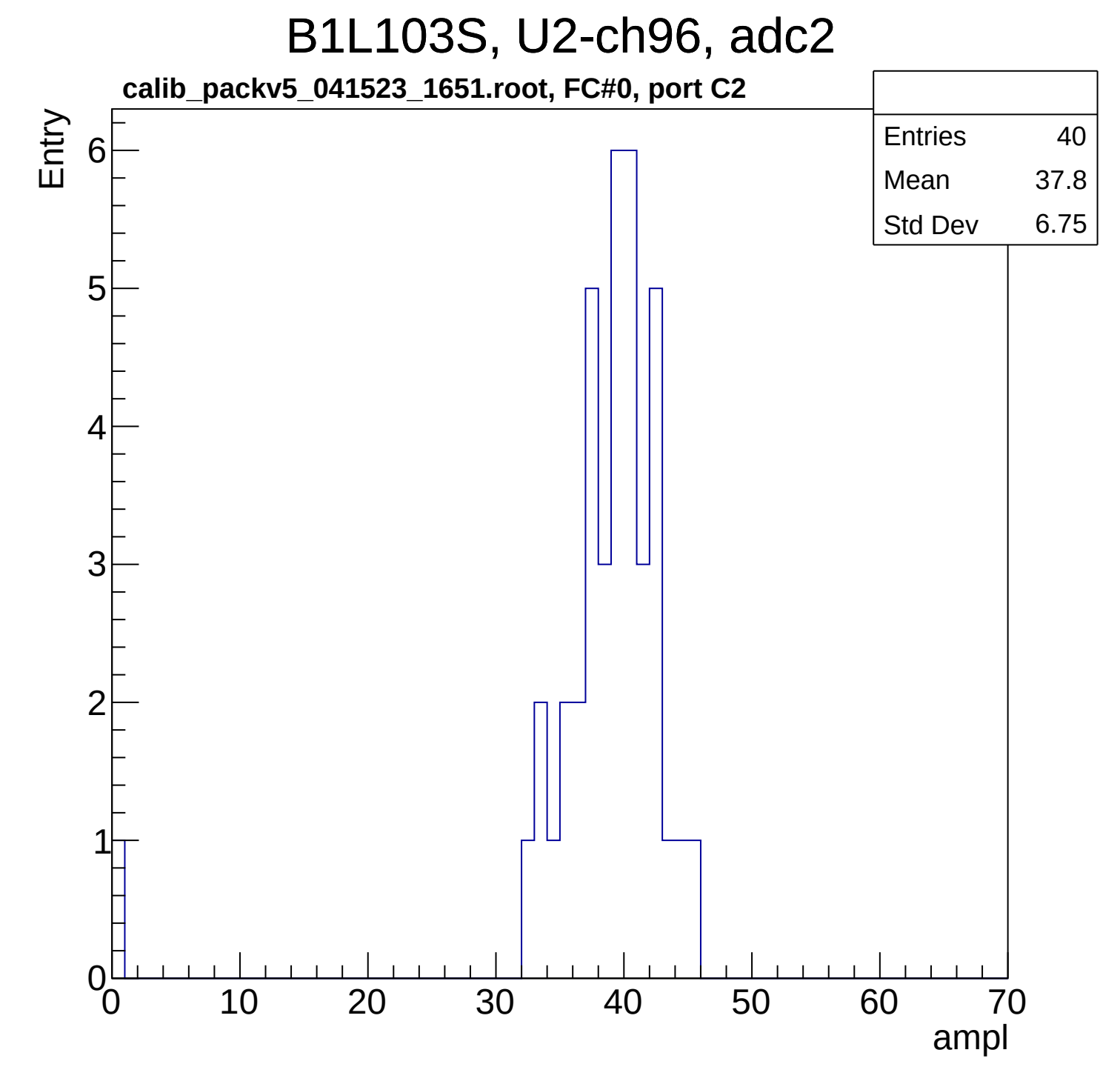

B1L103S, U2-ch95, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.61
Std Dev 9.126
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

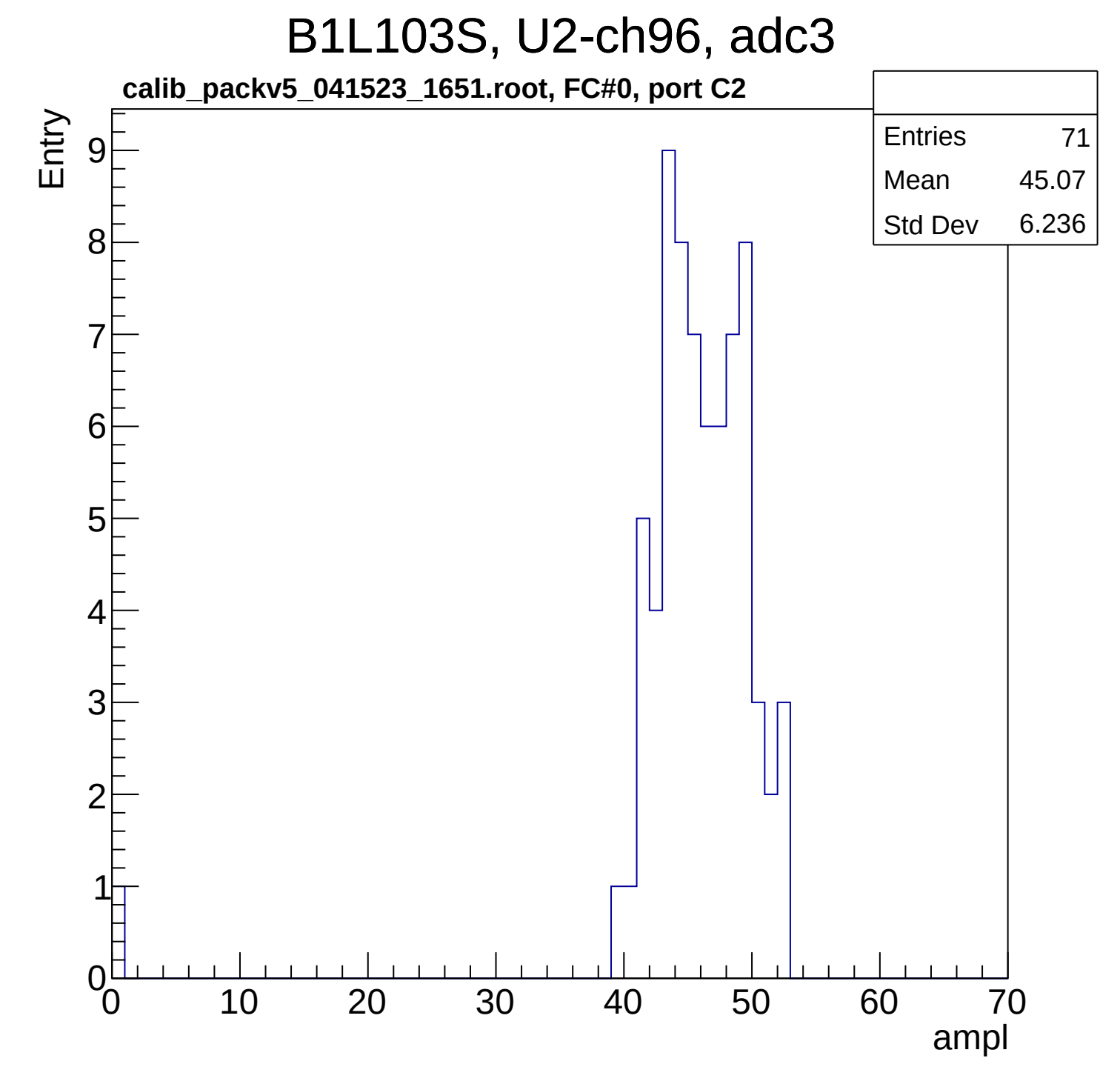

B1L103S, U2-ch95, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 60.71
Std Dev 1.578
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

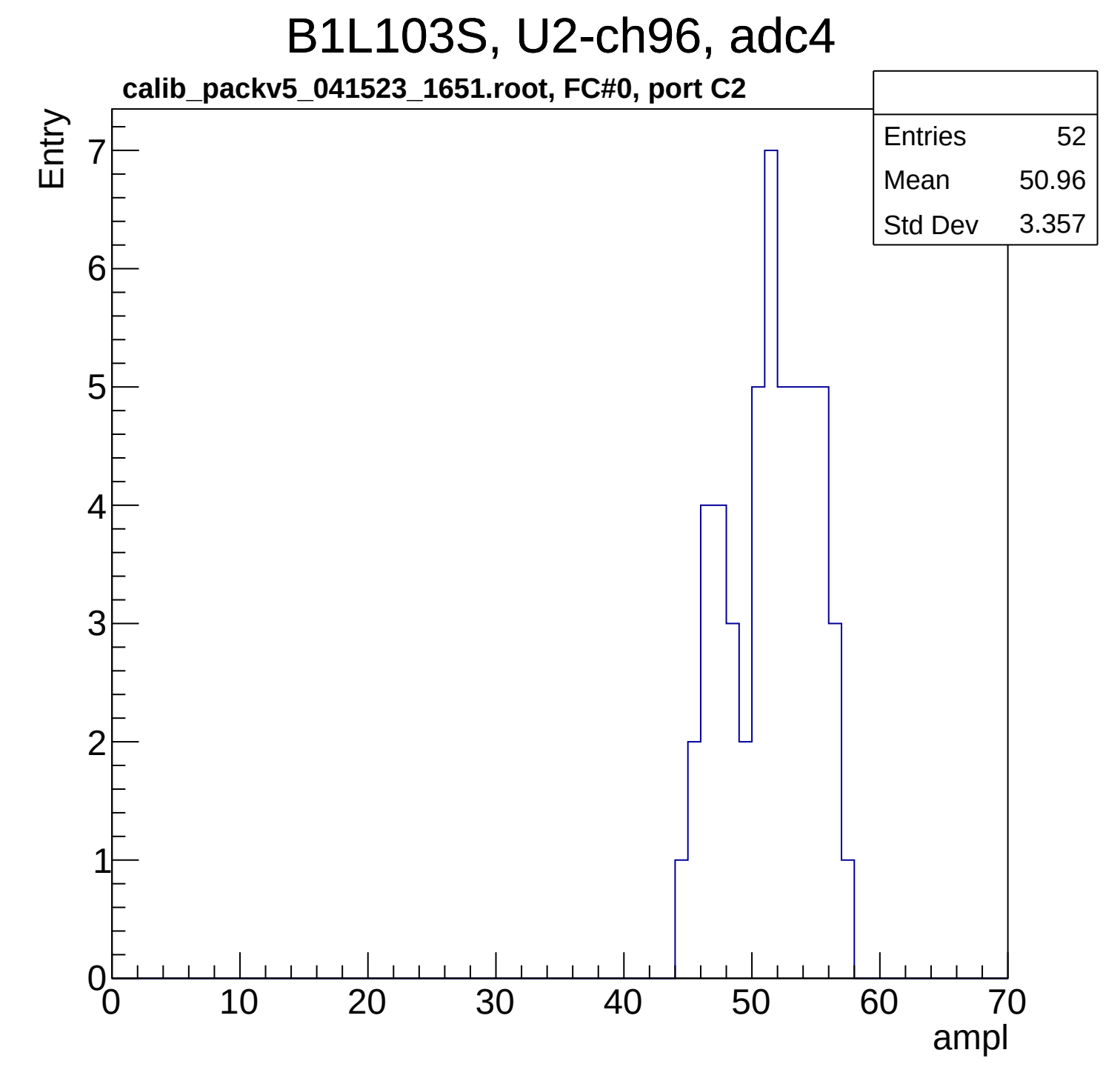

B1L103S, U2-ch95, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

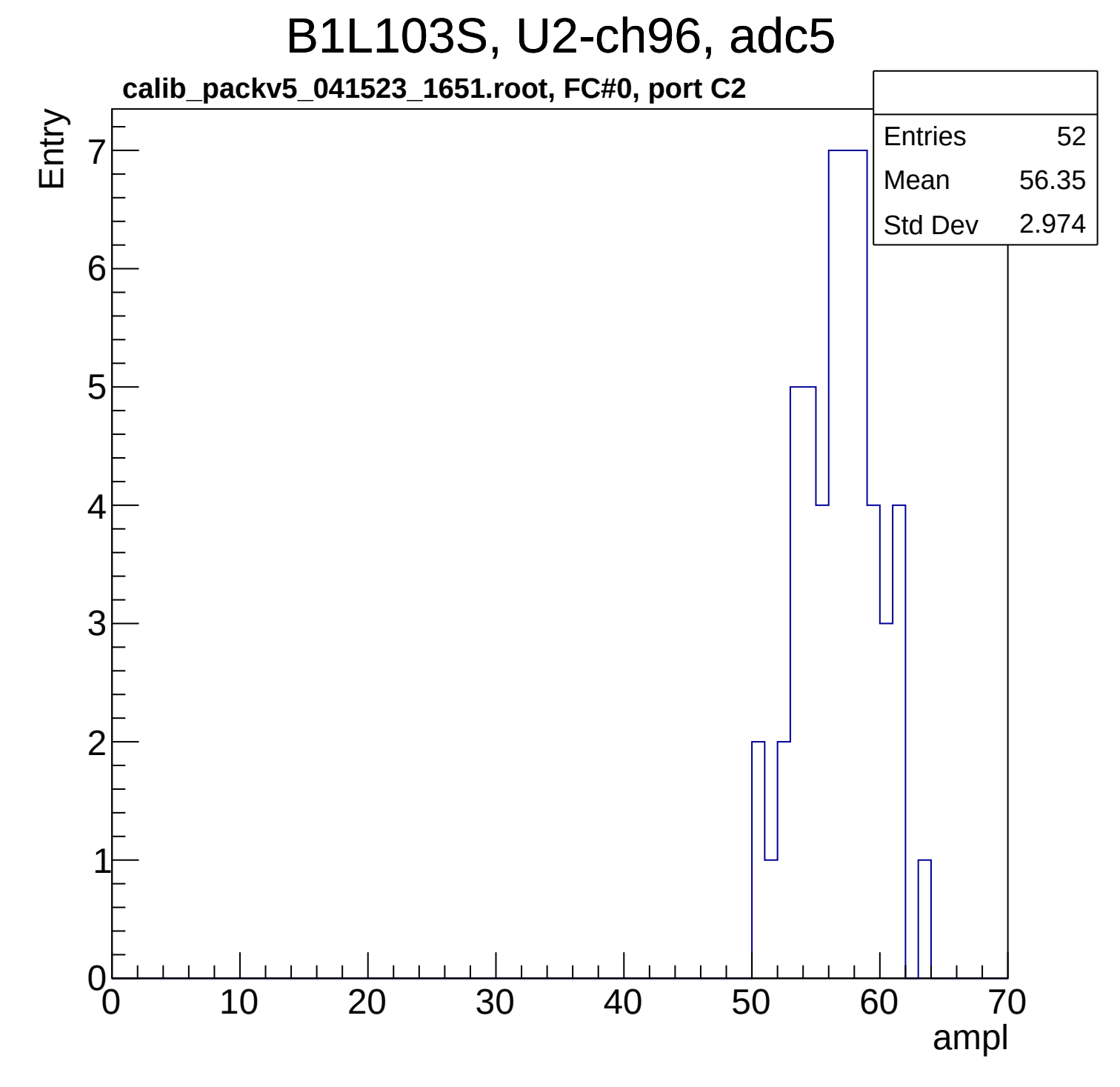

B1L103S, U2-ch96, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 18.6
Std Dev 12.16
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl

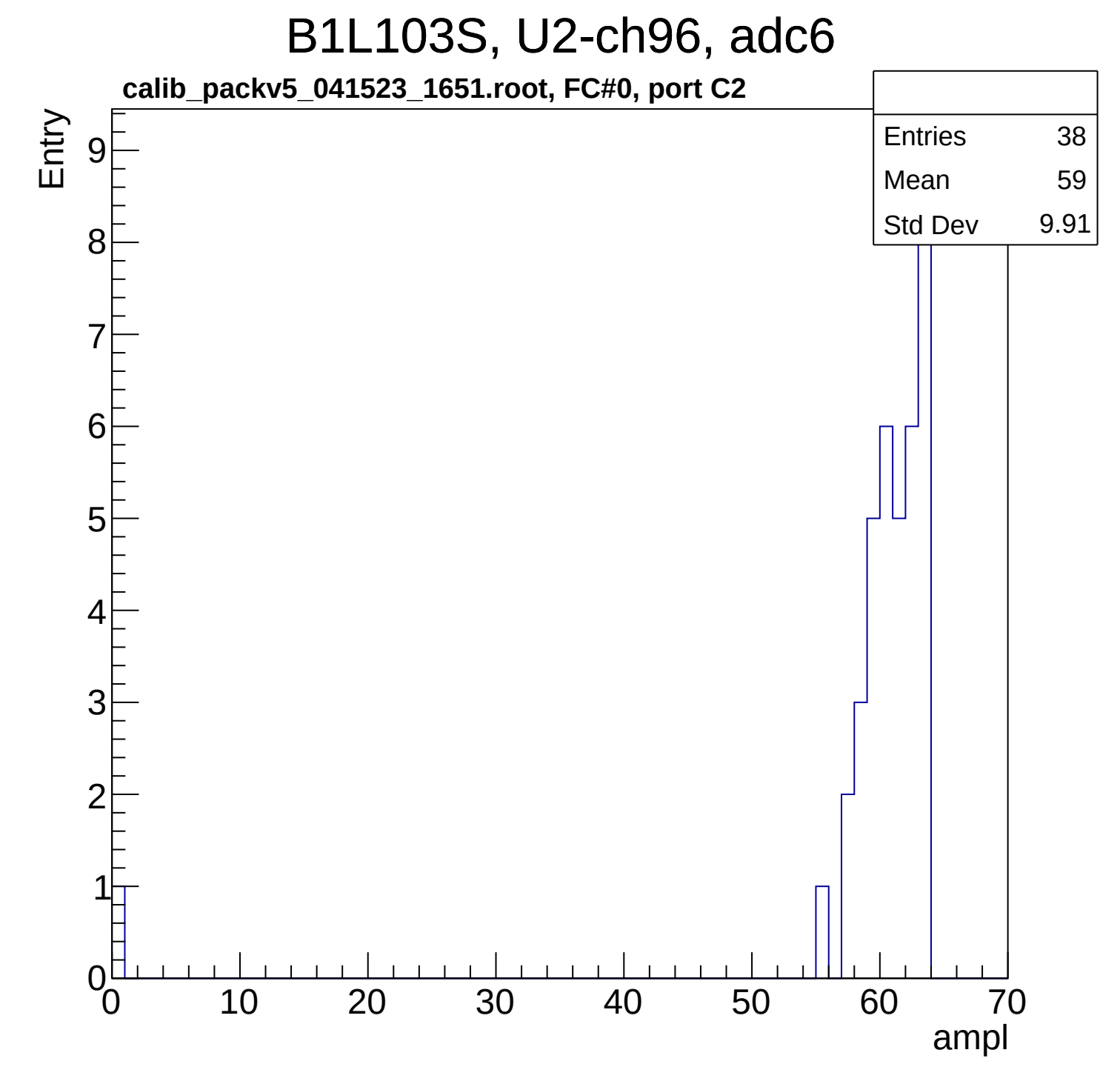

B1L103S, U2-ch96, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 29.48
Std Dev 11.59
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

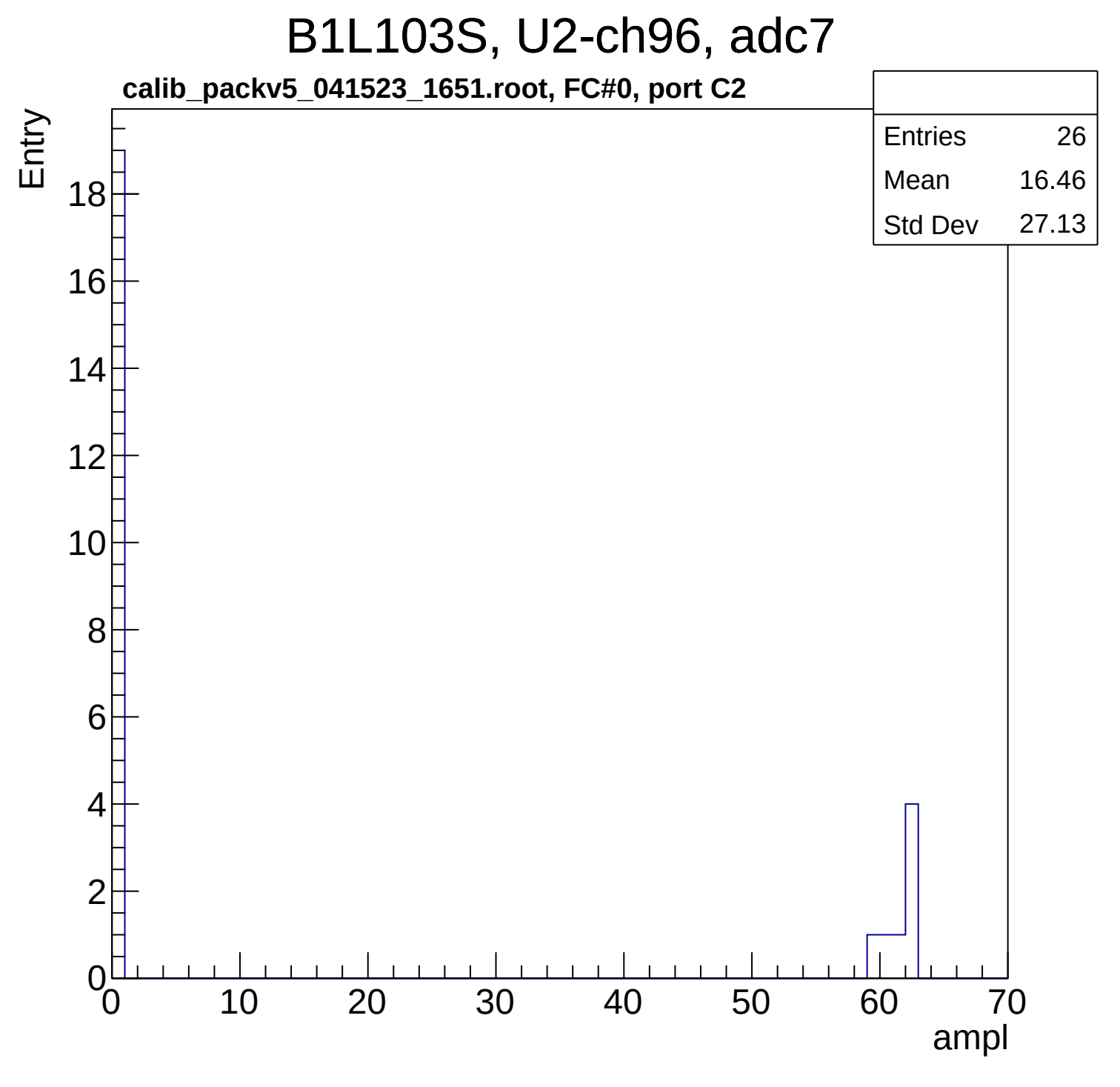

B1L103S, U2-ch96, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 37.8
Std Dev 6.75
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

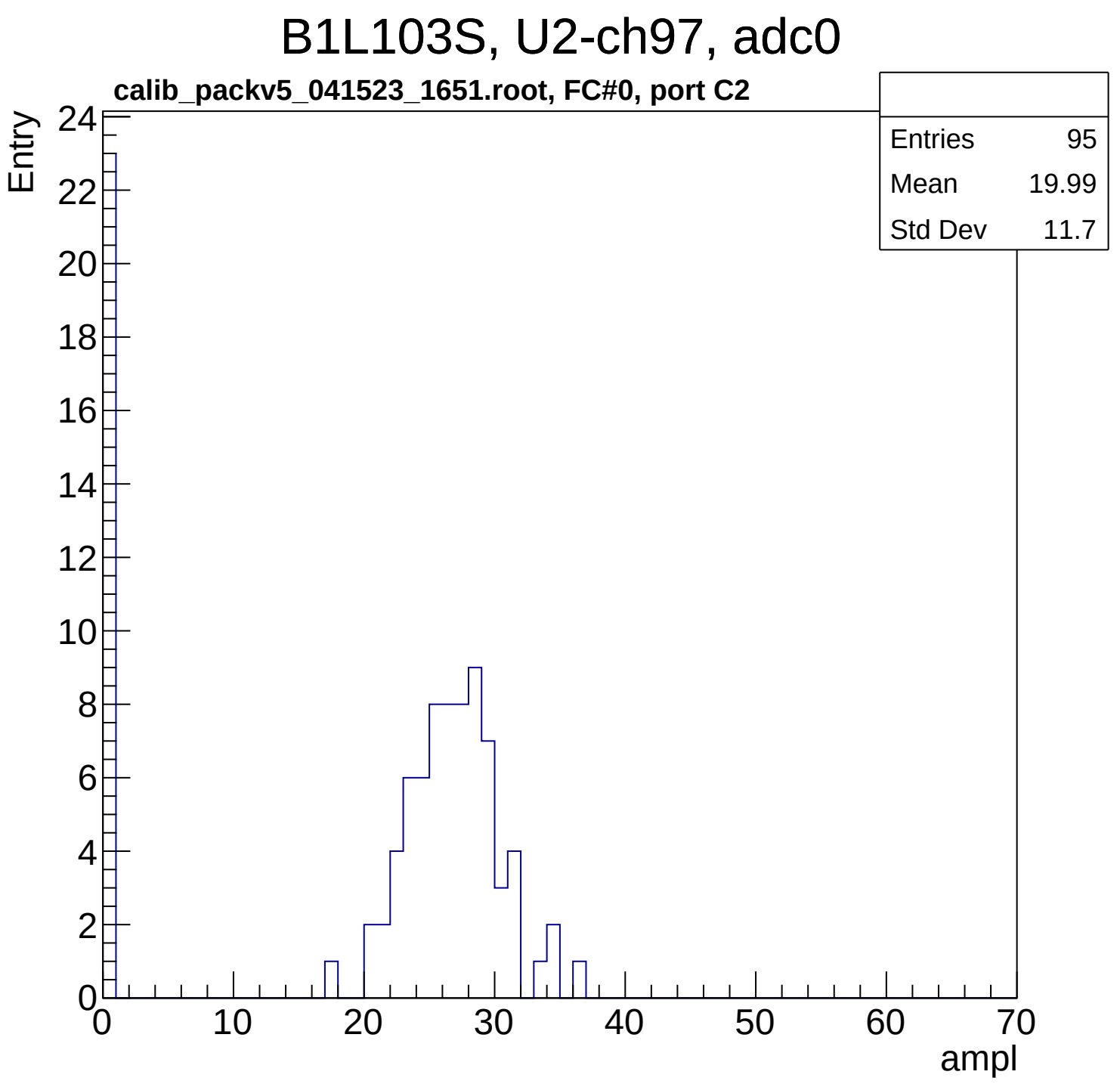

B1L103S, U2-ch96, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 45.07
Std Dev 6.236
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

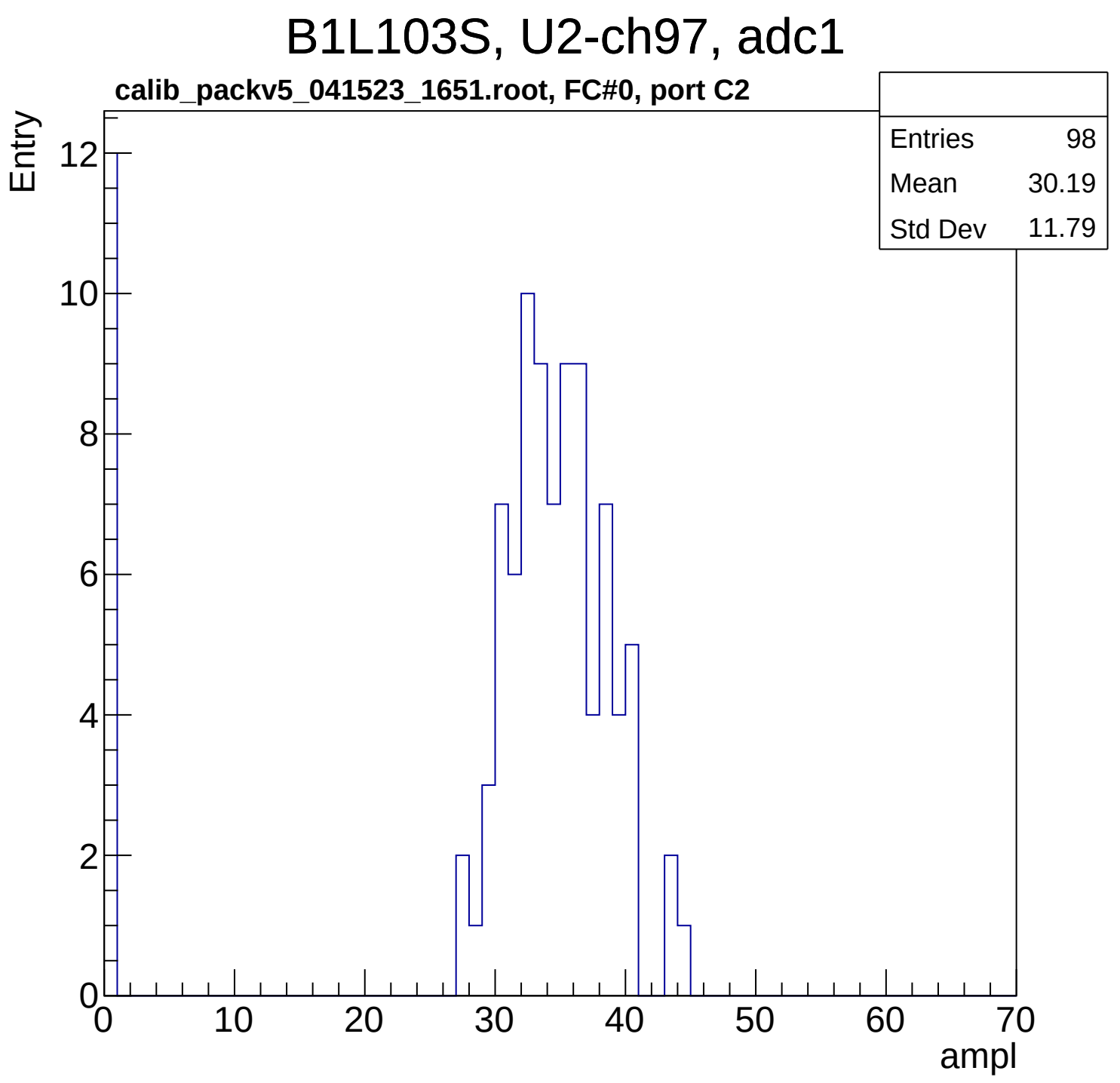

B1L103S, U2-ch96, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 50.96
Std Dev 3.357
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

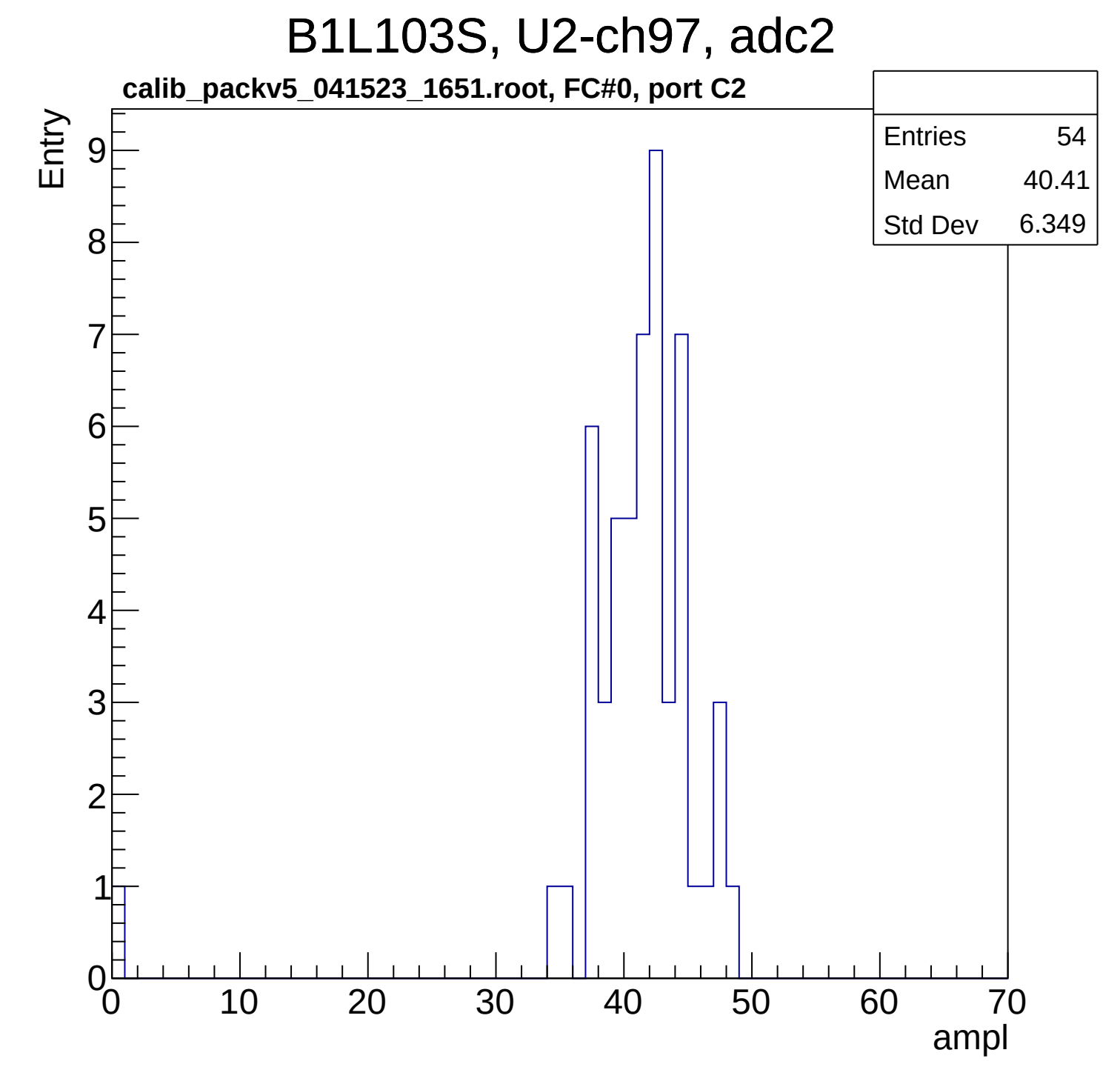

B1L103S, U2-ch96, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 56.35
Std Dev 2.974
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

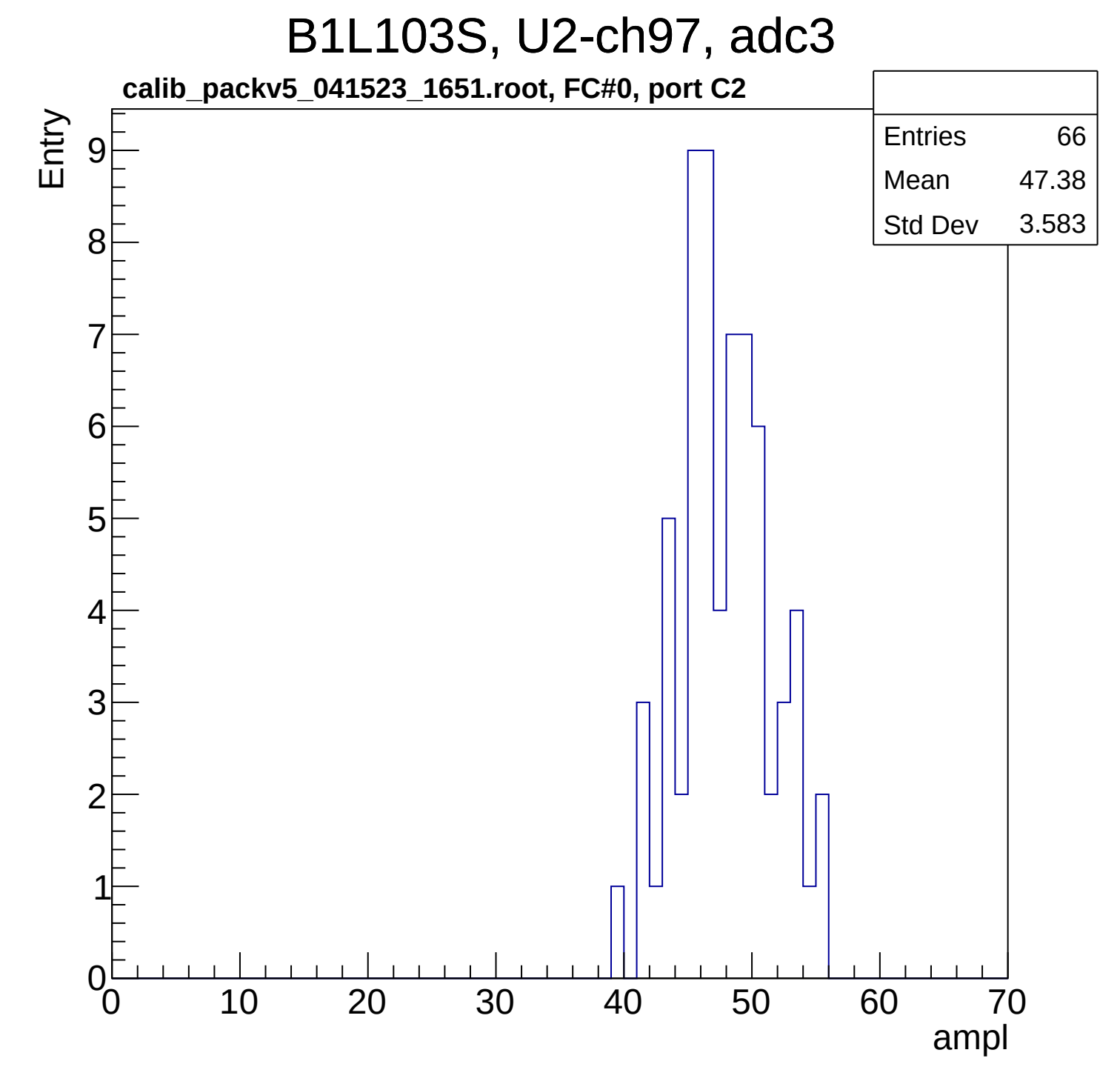

B1L103S, U2-ch96, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 59
Std Dev 9.91
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

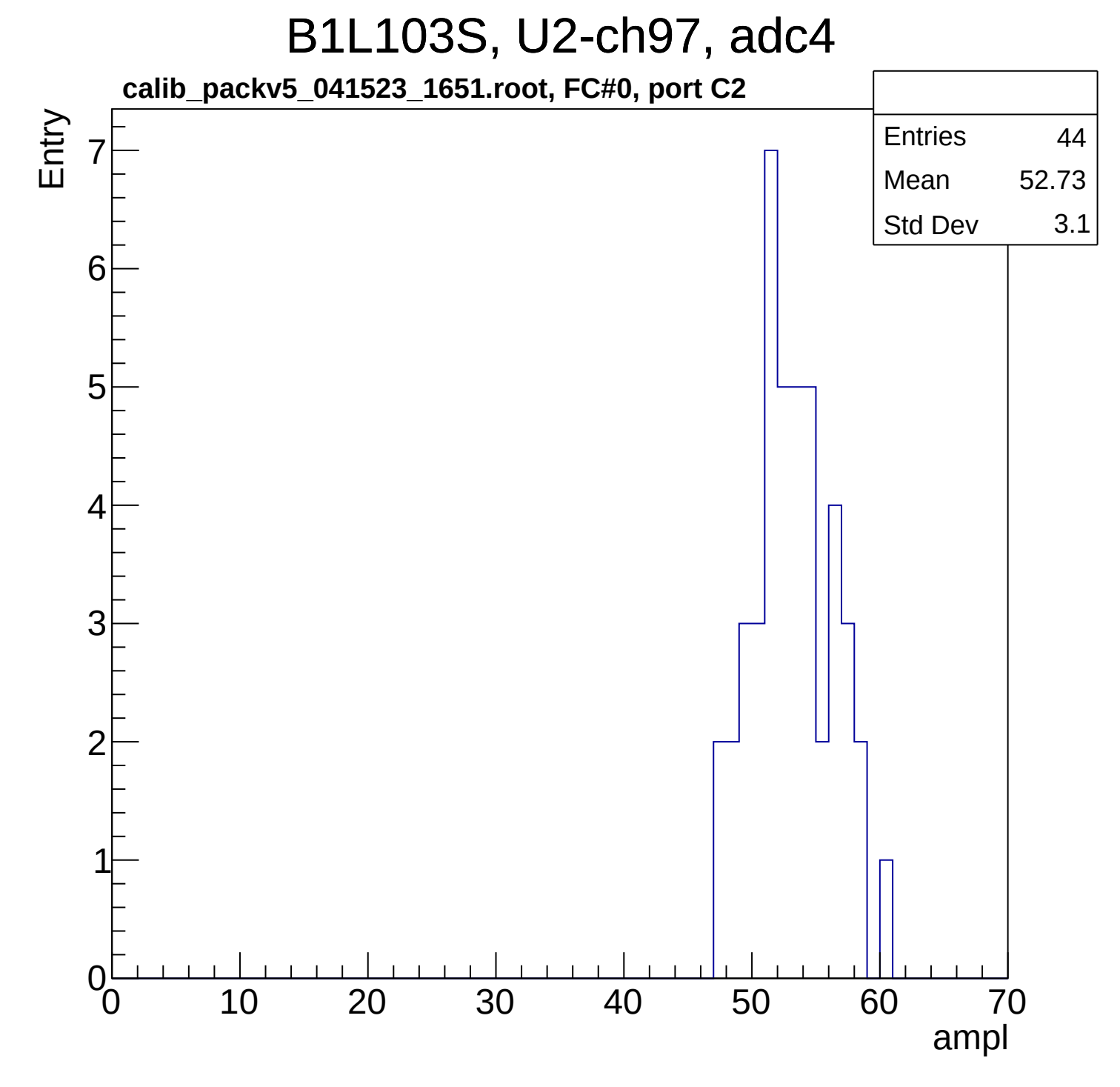

B1L103S, U2-ch96, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 16.46
Std Dev 27.13
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

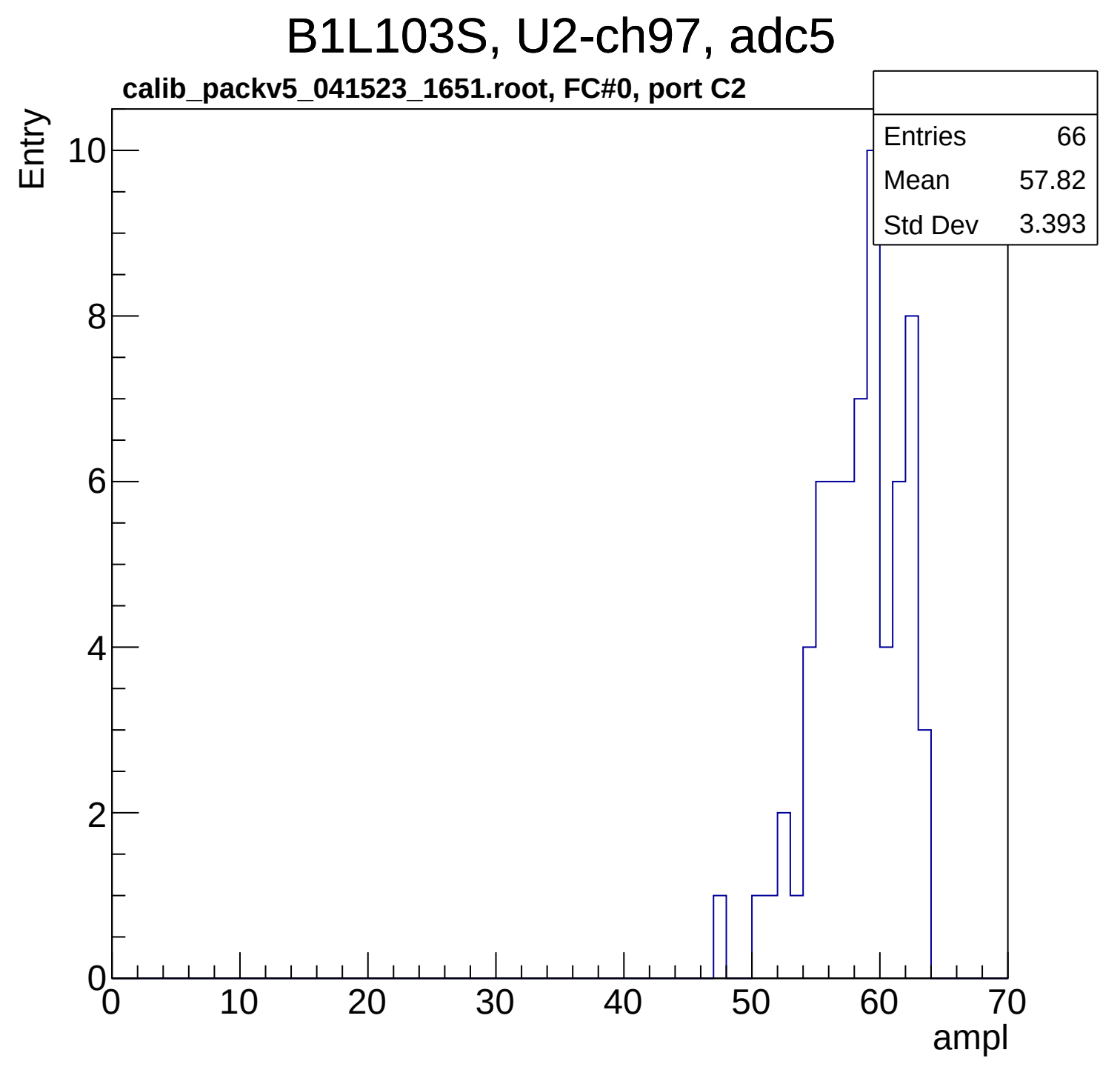

B1L103S, U2-ch97, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 19.99
Std Dev 11.7
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70

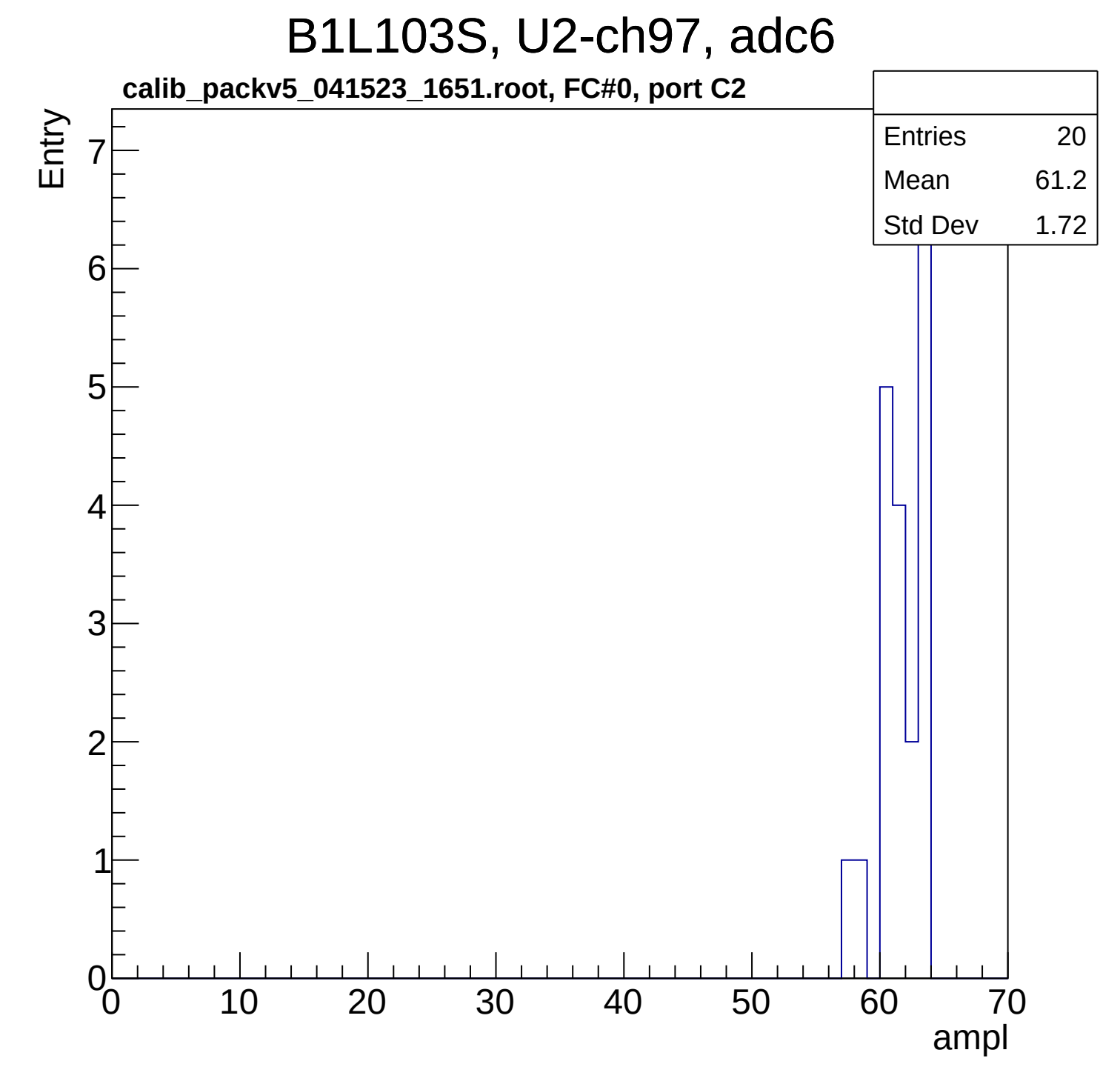

B1L103S, U2-ch97, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 30.19
Std Dev 11.79
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

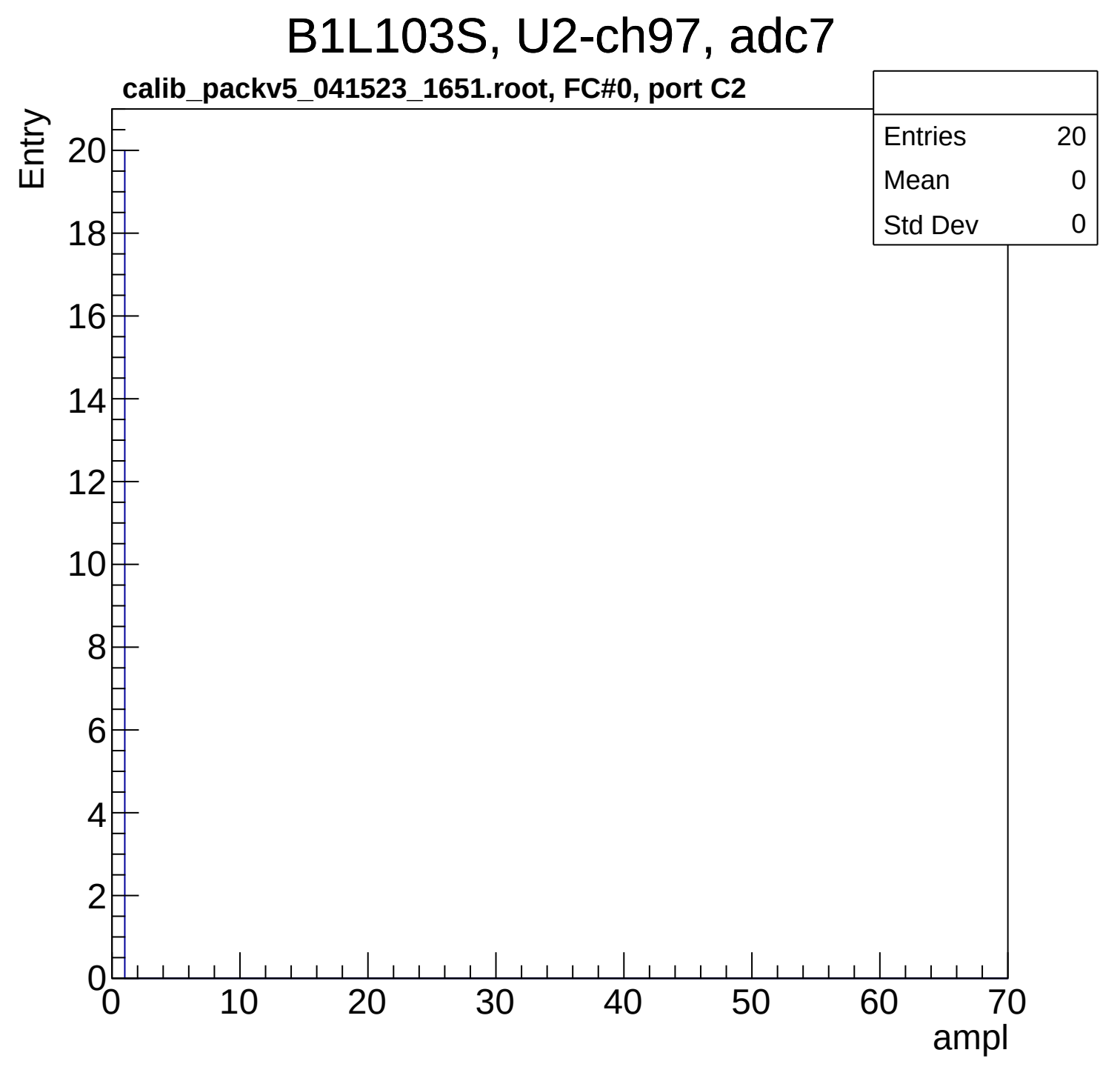

B1L103S, U2-ch97, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 40.41
Std Dev 6.349
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

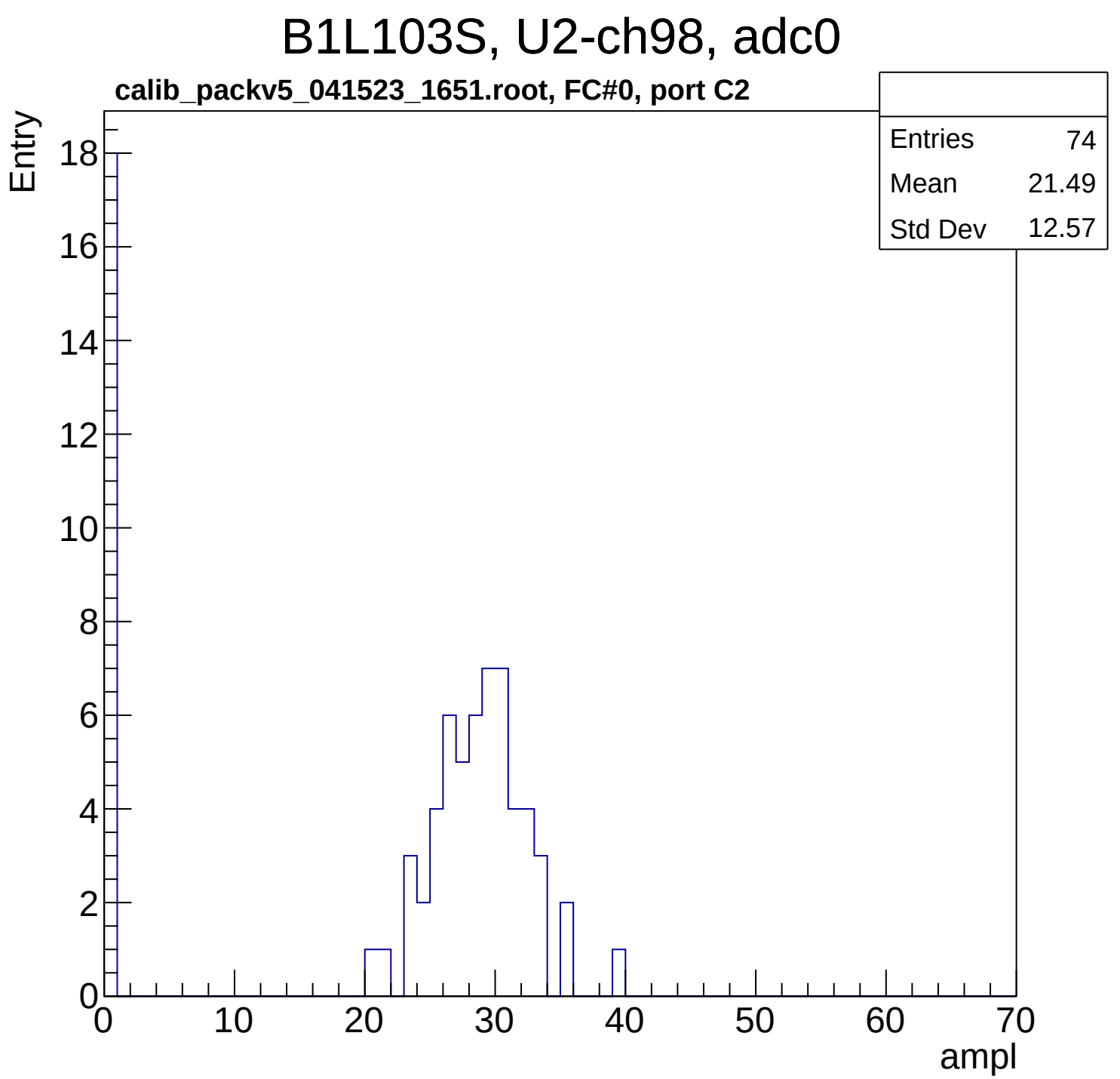

B1L103S, U2-ch97, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 47.38
Std Dev 3.583
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

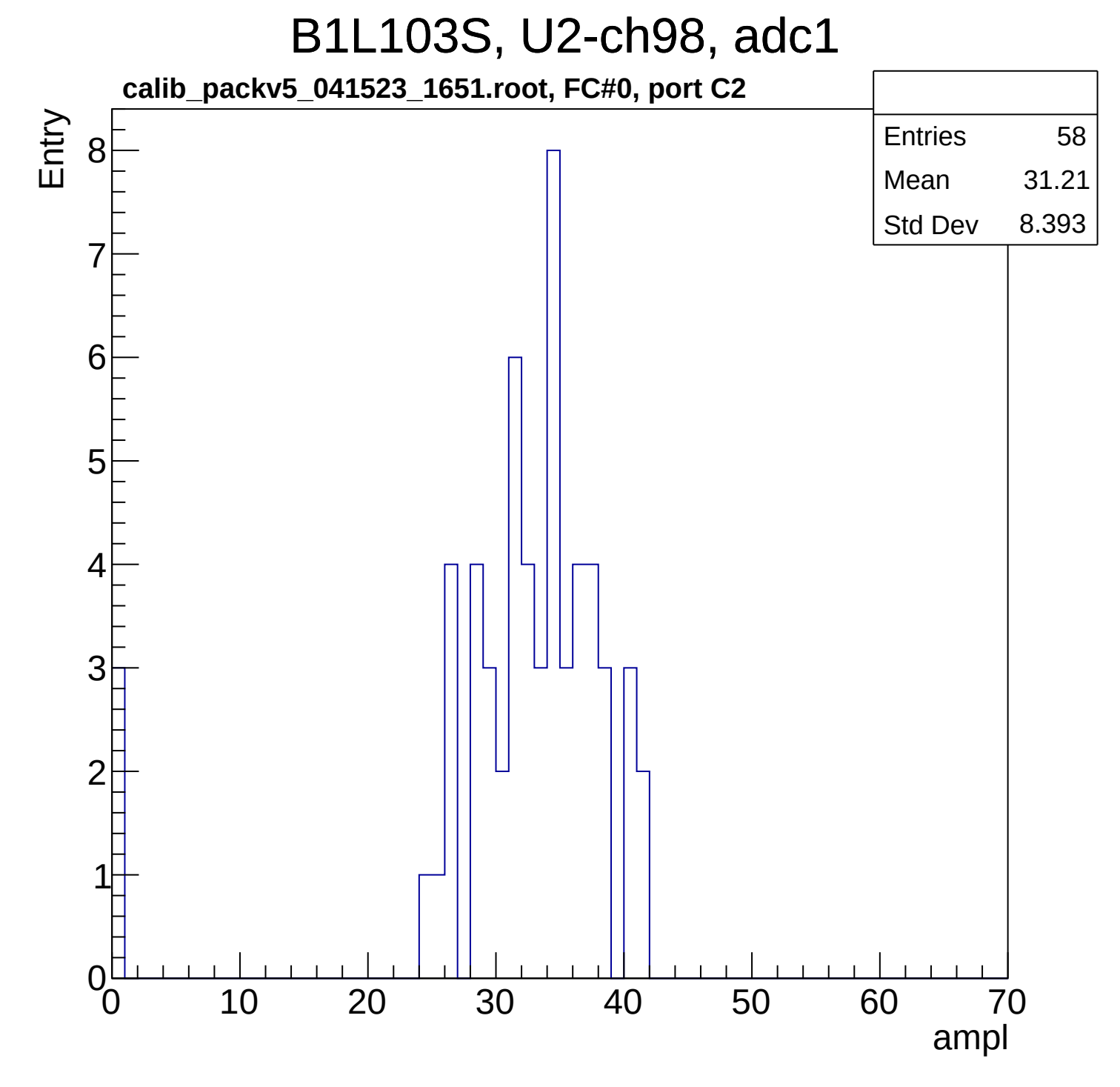

B1L103S, U2-ch97, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 52.73
Std Dev 3.1
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

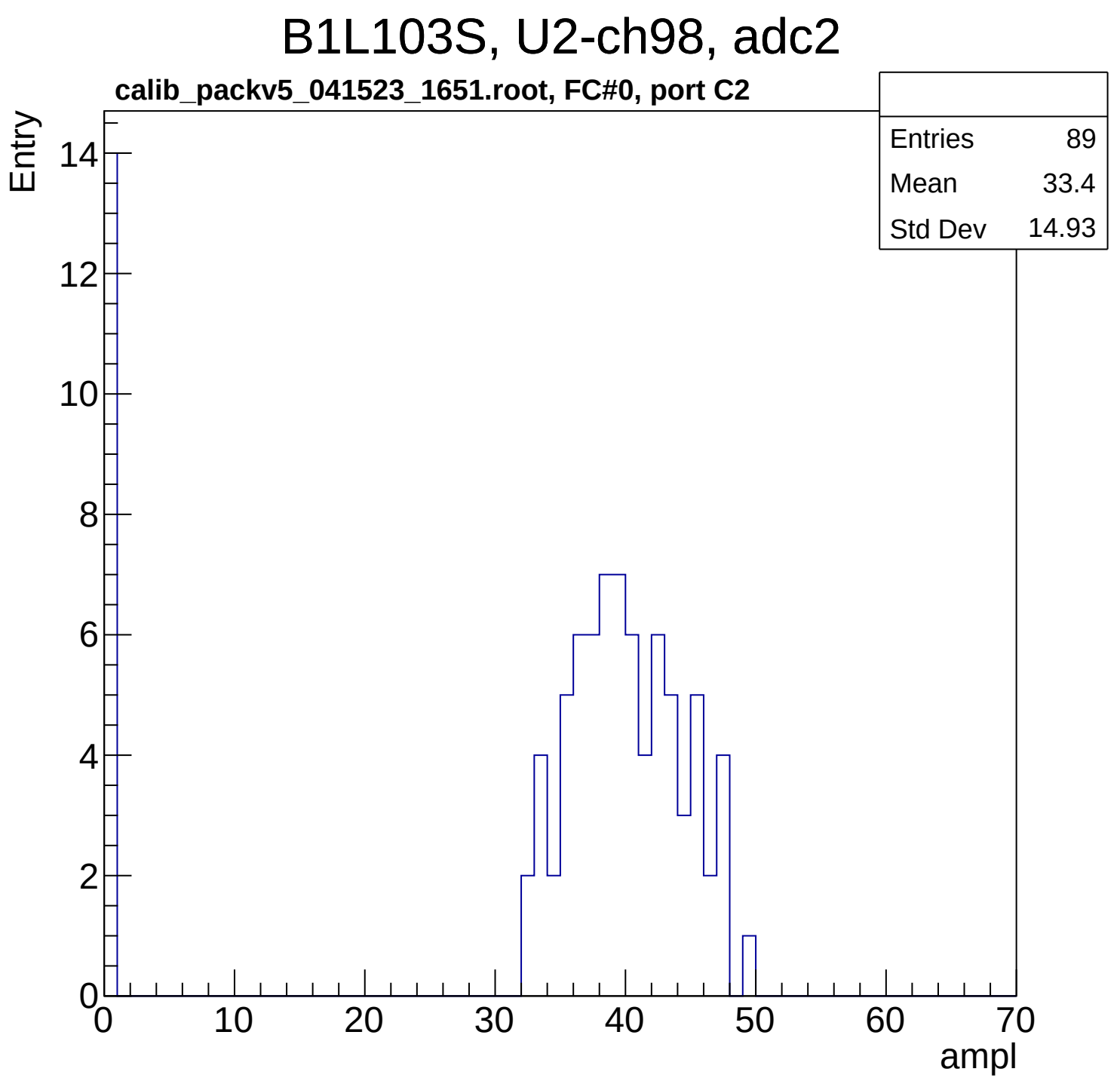

B1L103S, U2-ch97, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 57.82
Std Dev 3.393
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

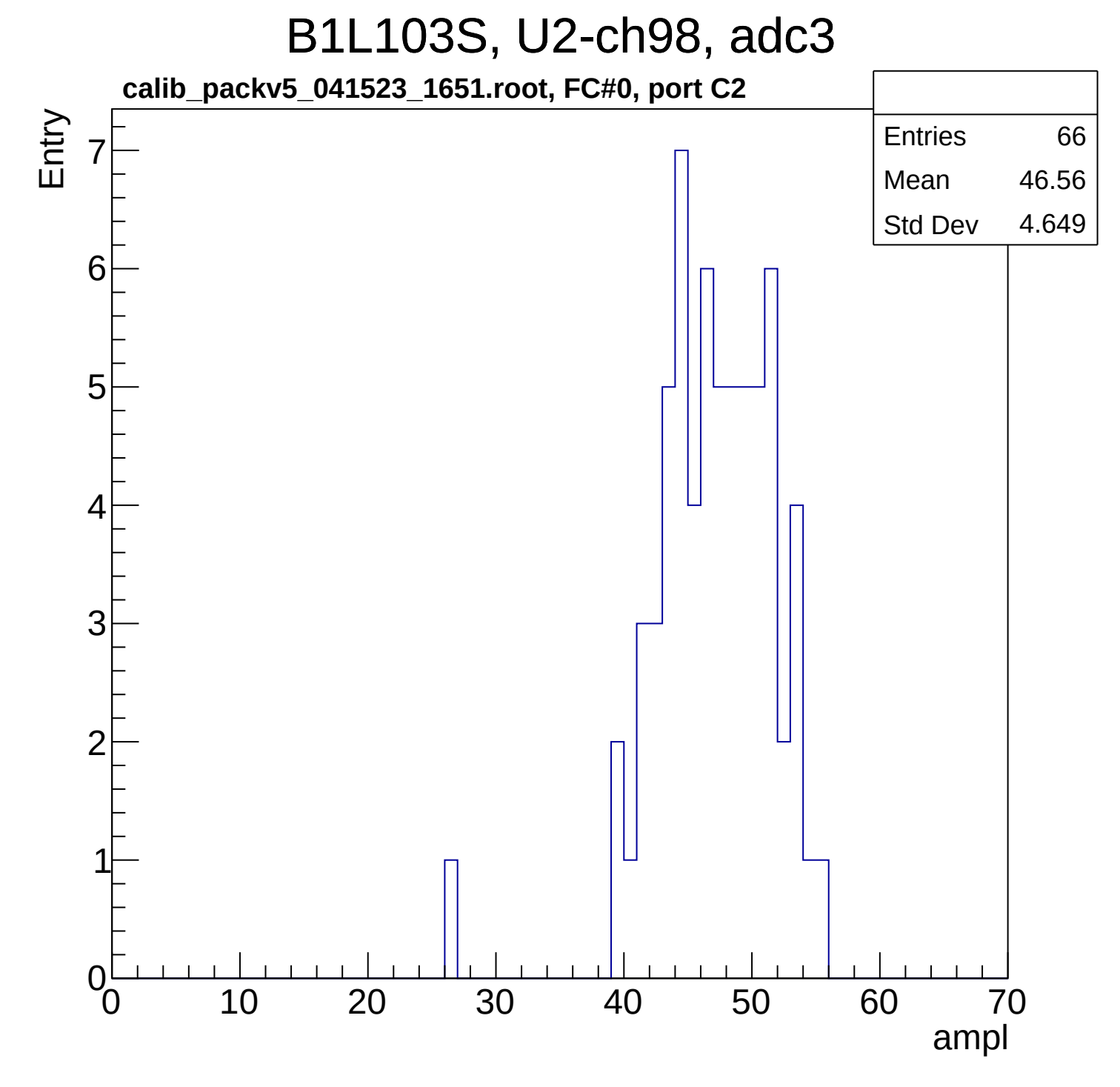

B1L103S, U2-ch97, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 61.2
Std Dev 1.72
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

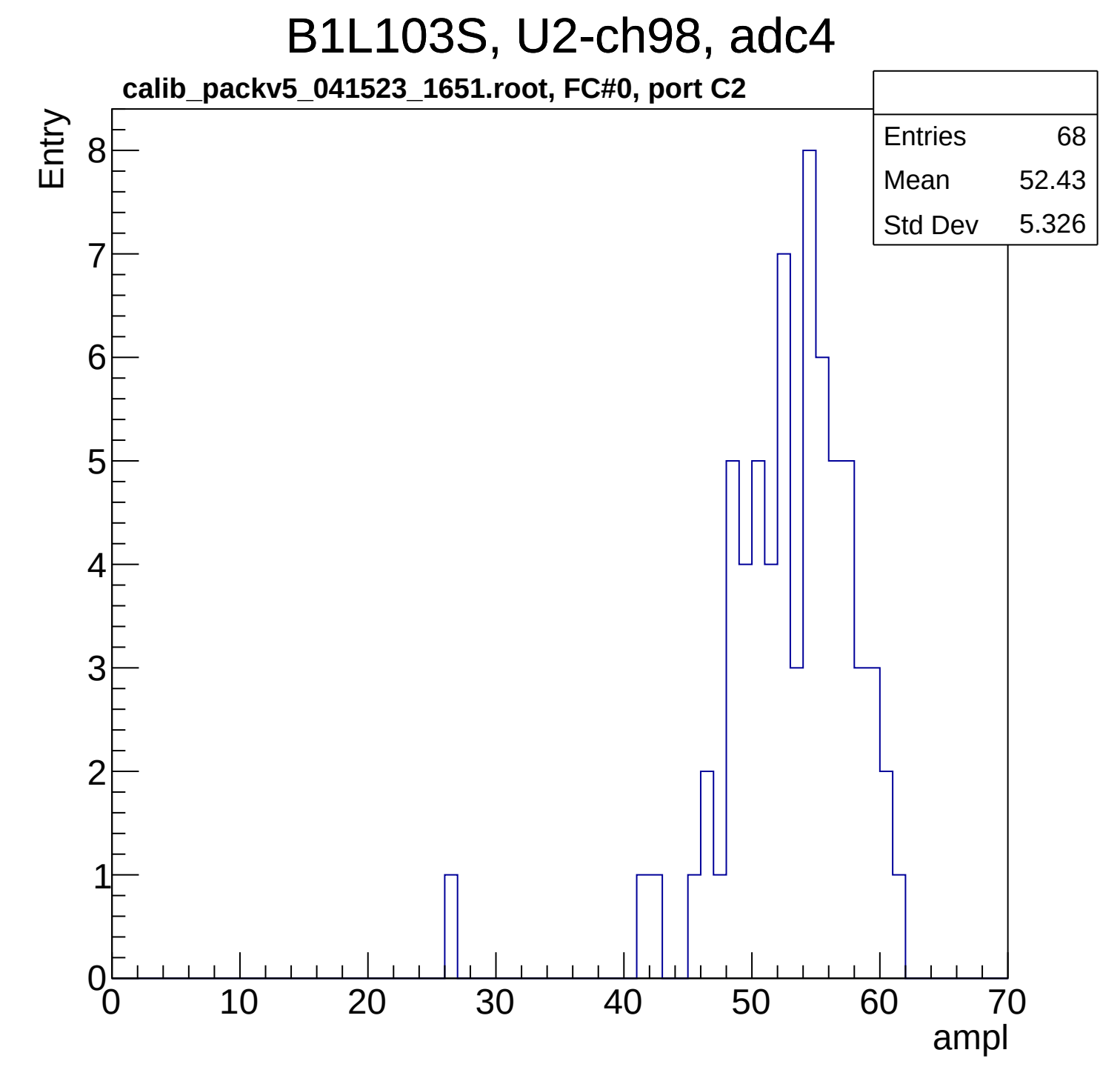

B1L103S, U2-ch97, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl

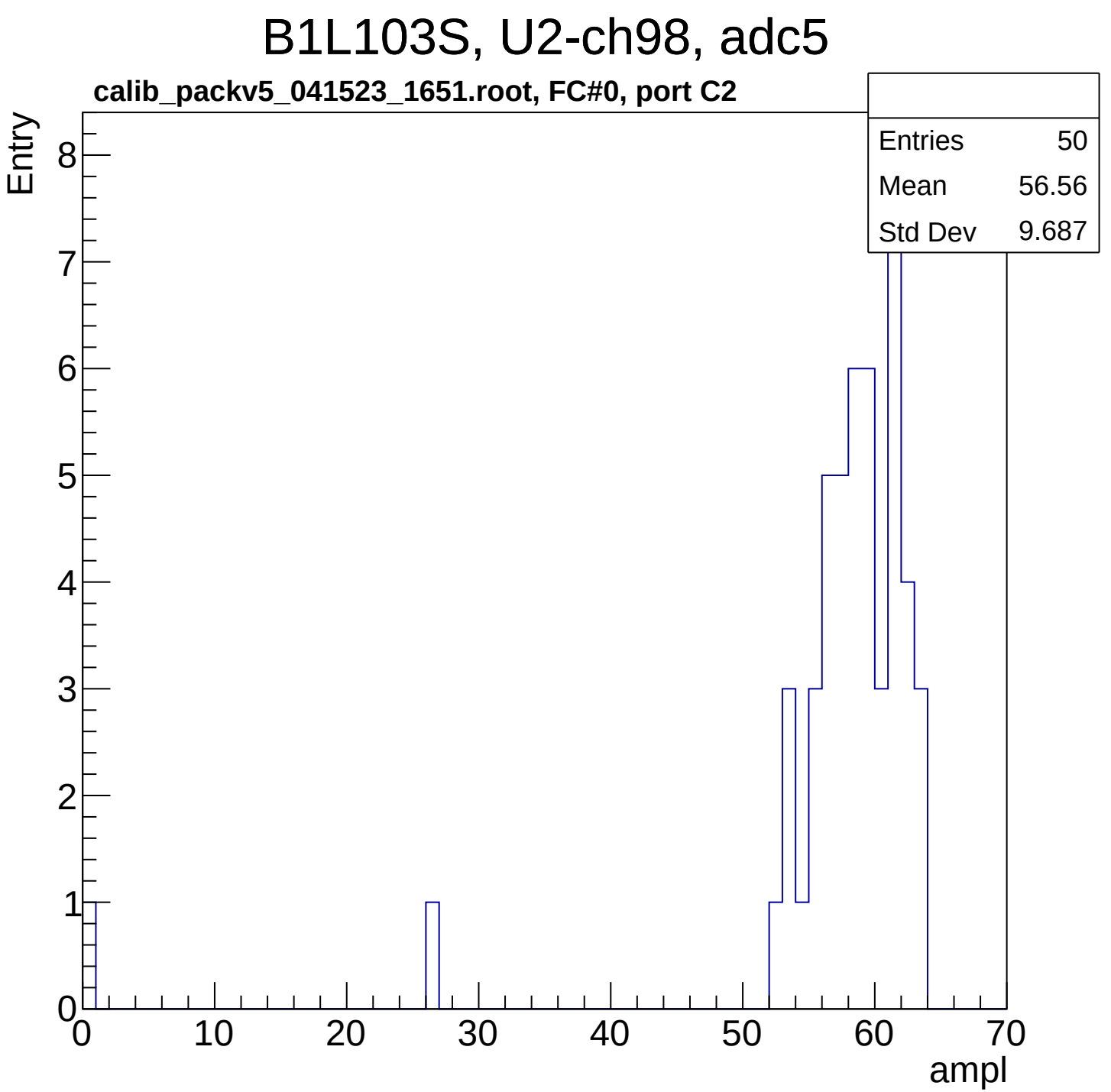

B1L103S, U2-ch98, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 21.49
Std Dev 12.57
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

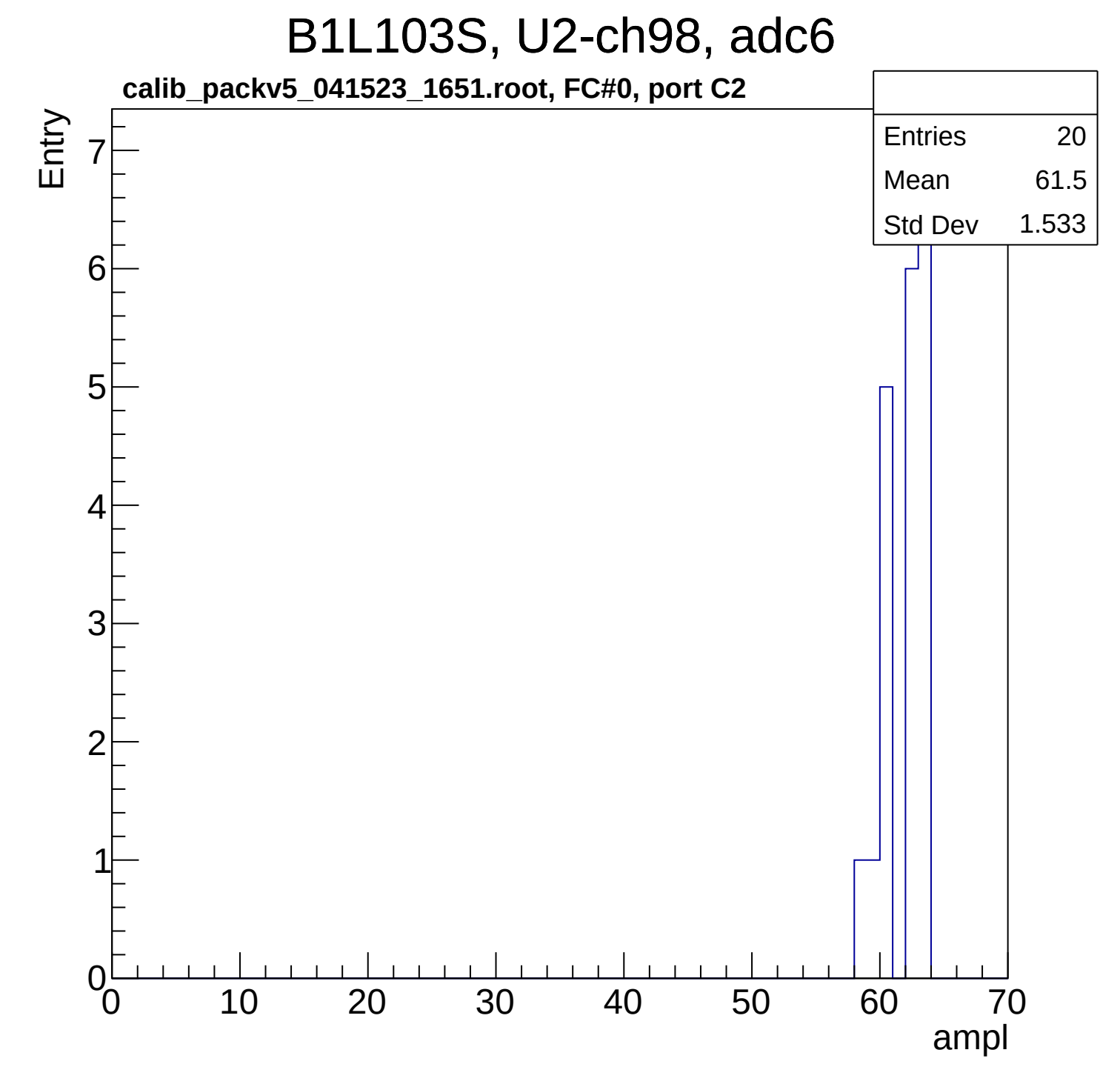

B1L103S, U2-ch98, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 31.21
Std Dev 8.393
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

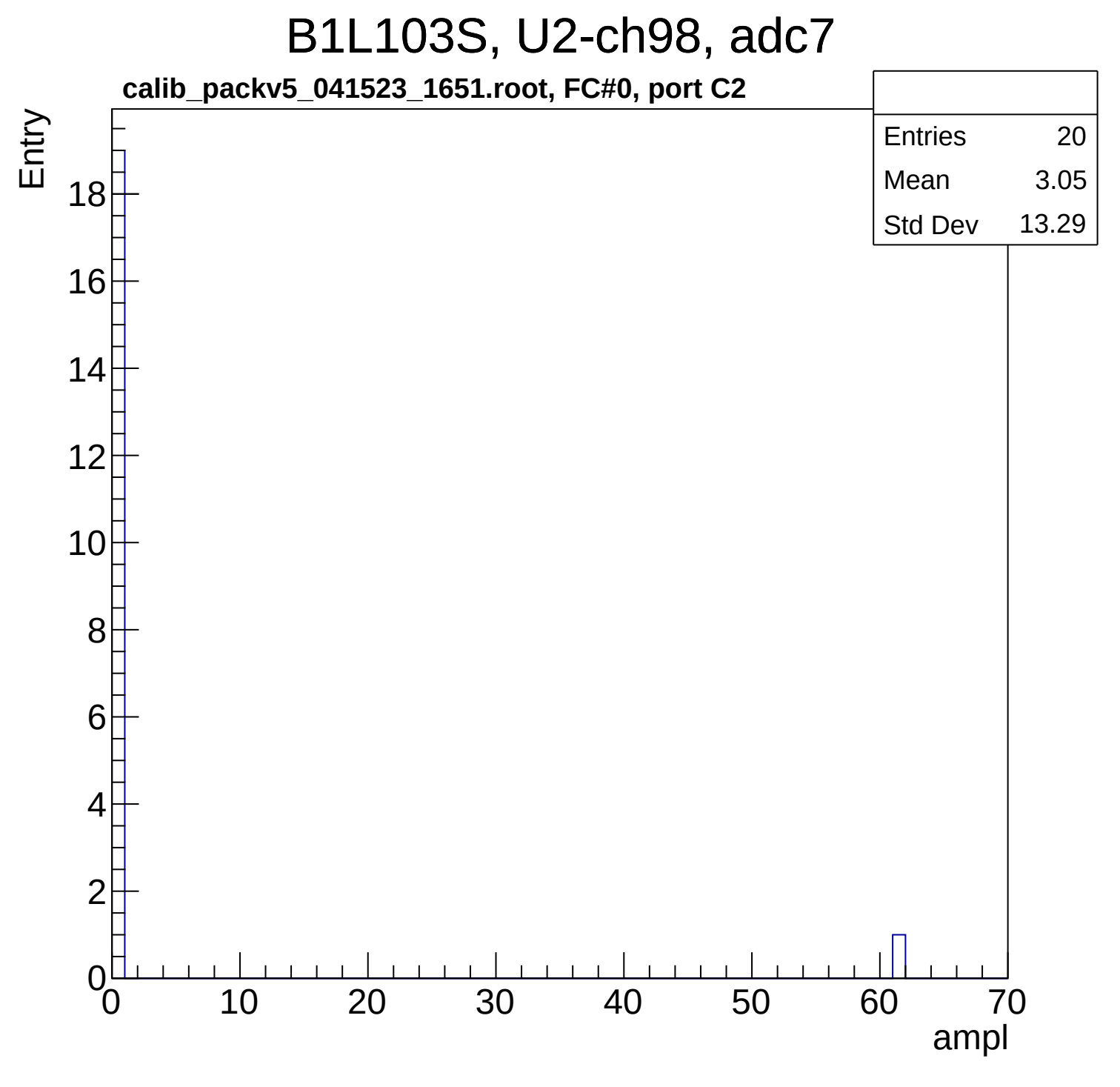

B1L103S, U2-ch98, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 33.4
Std Dev 14.93
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

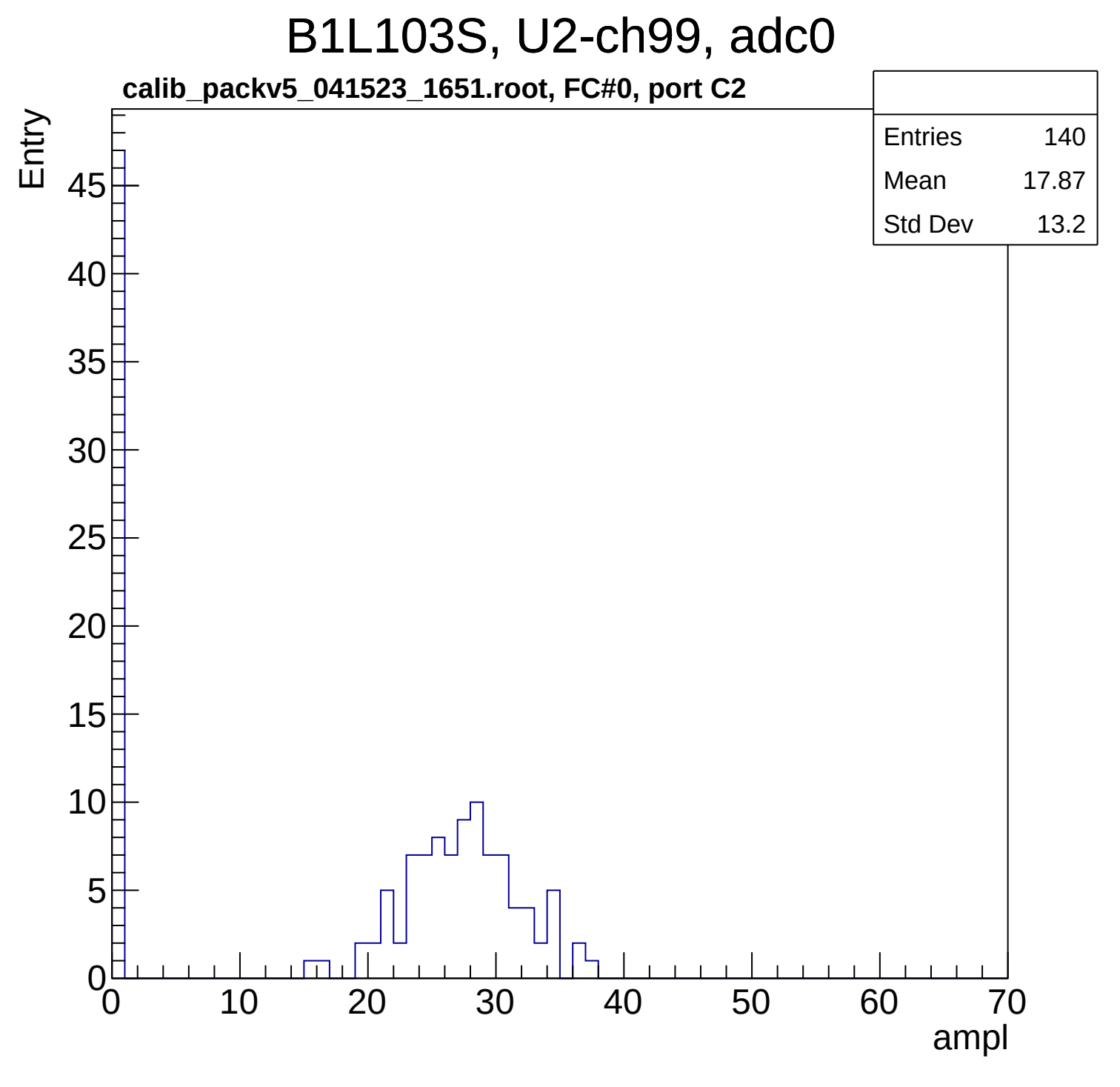

B1L103S, U2-ch98, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 46.56
Std Dev 4.649
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

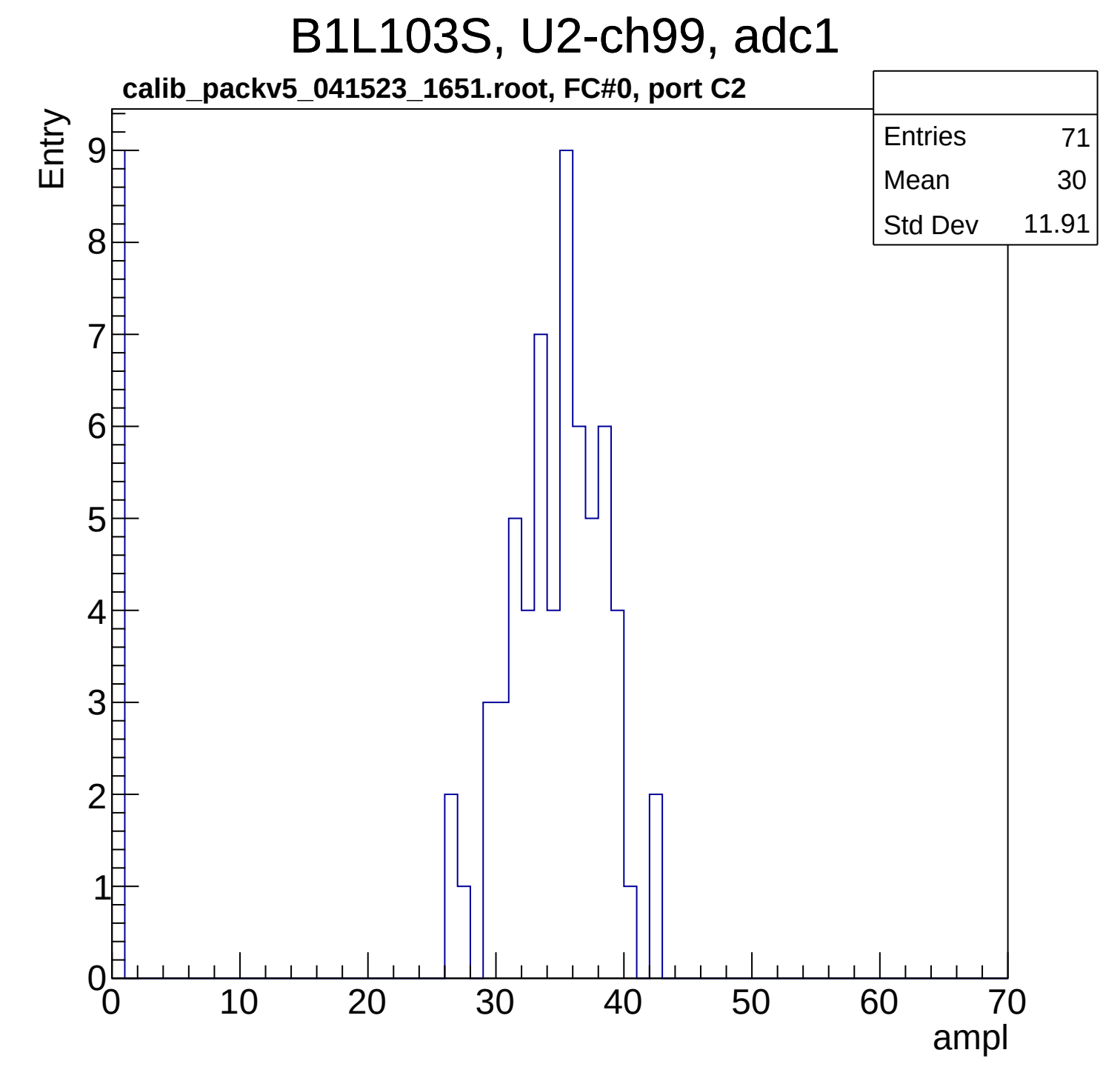

B1L103S, U2-ch98, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 52.43
Std Dev 5.326
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

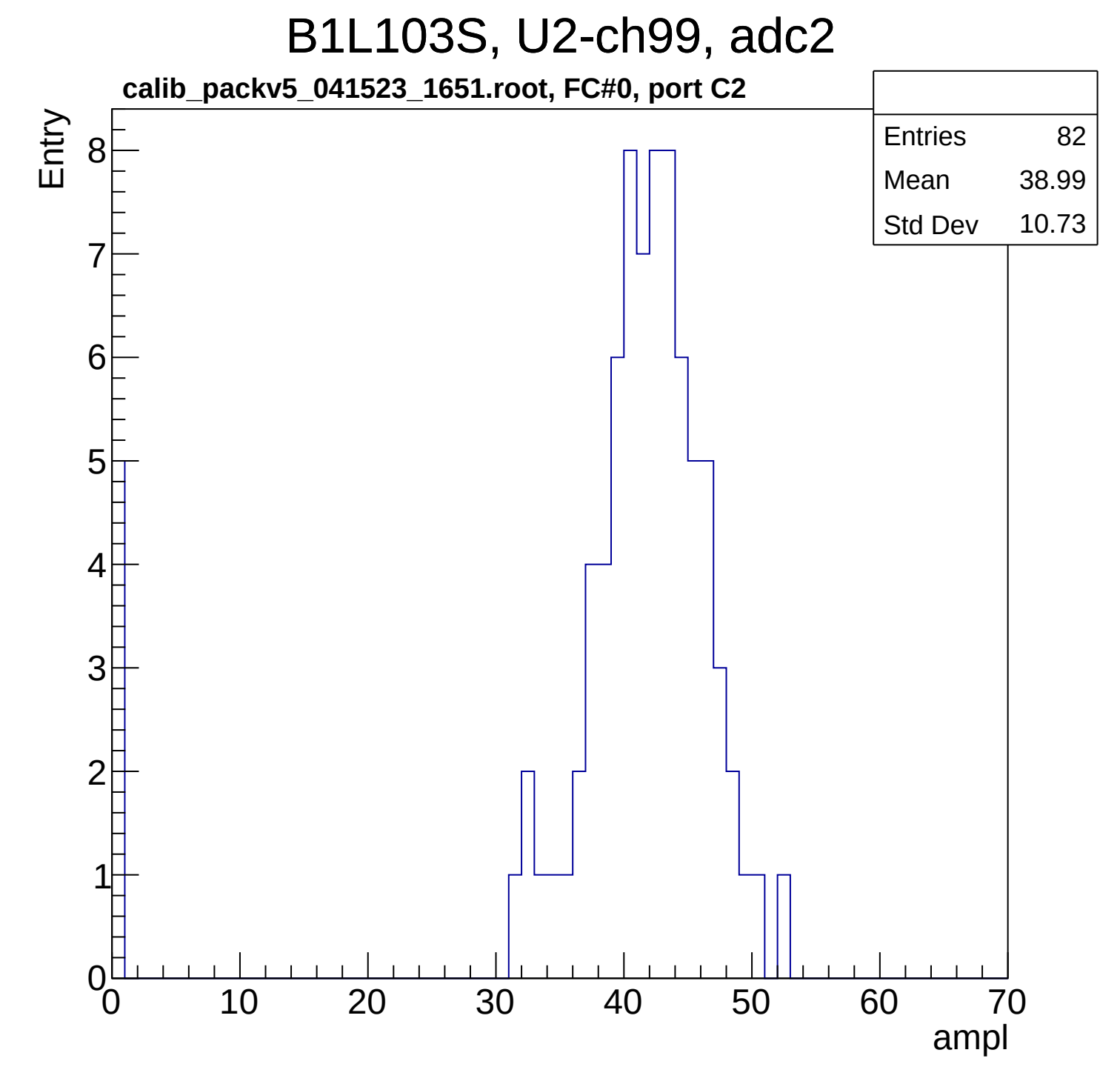

B1L103S, U2-ch98, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 56.56
Std Dev 9.687
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

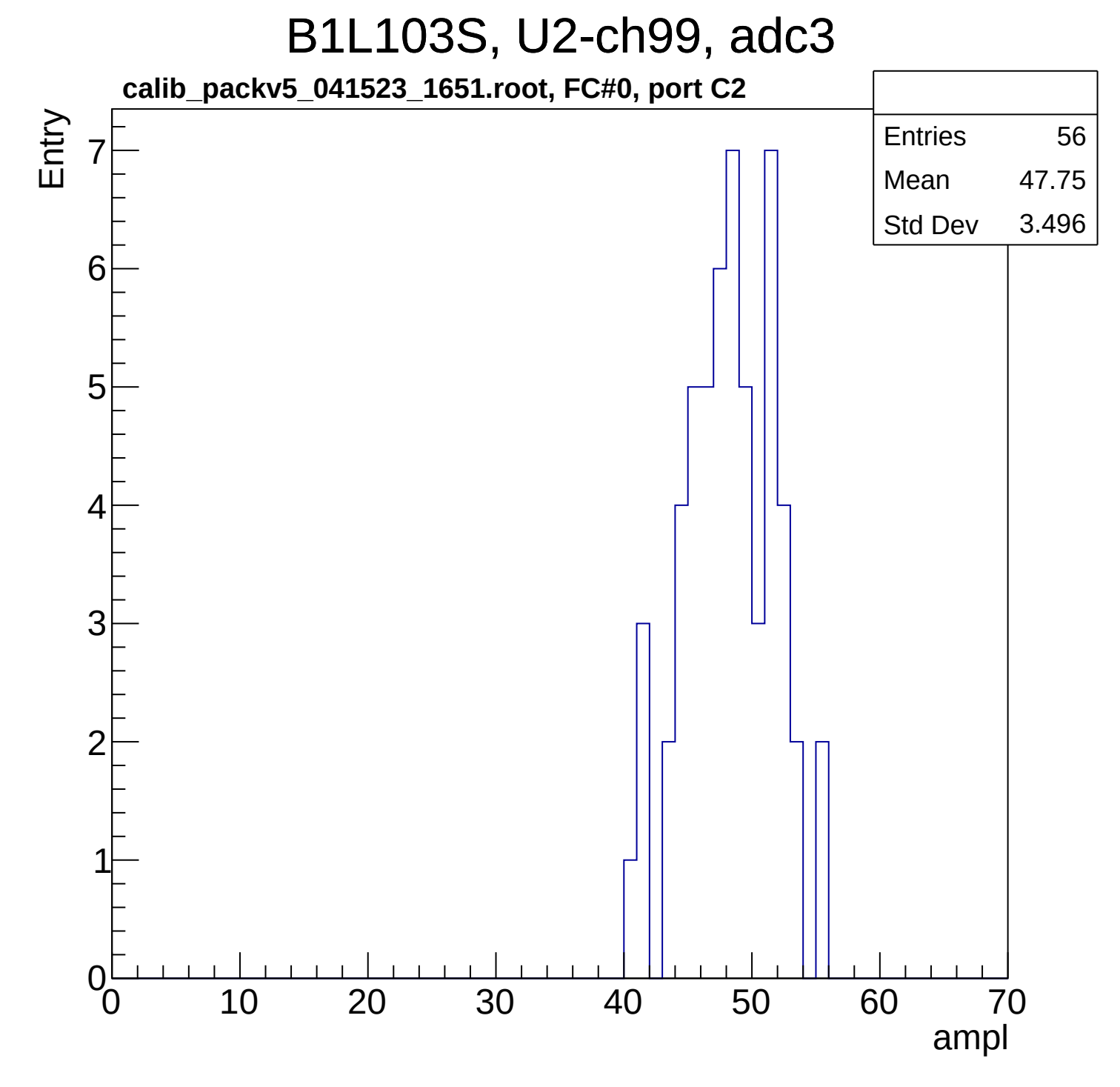

B1L103S, U2-ch98, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 61.5
Std Dev 1.533
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

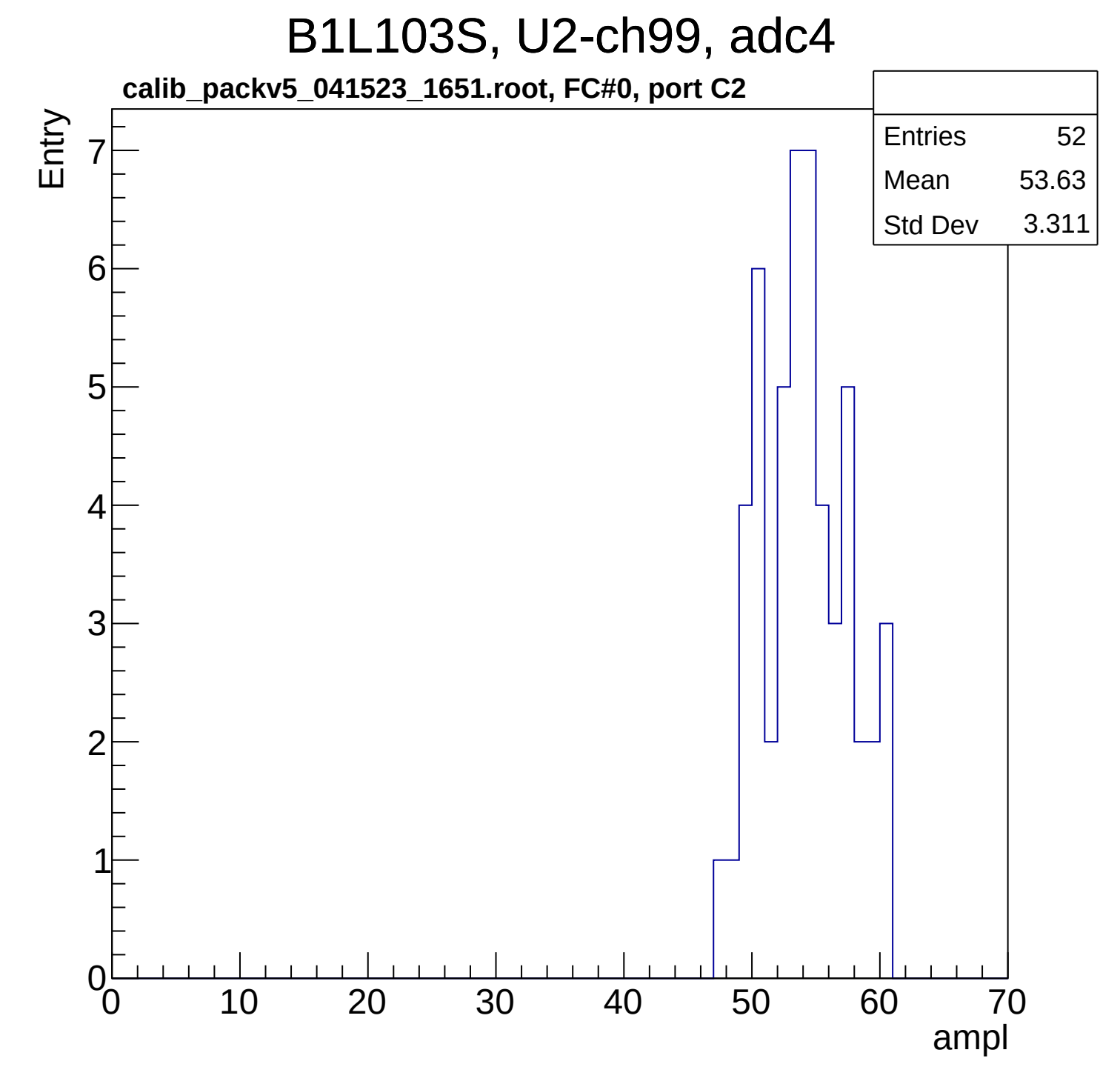

B1L103S, U2-ch98, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

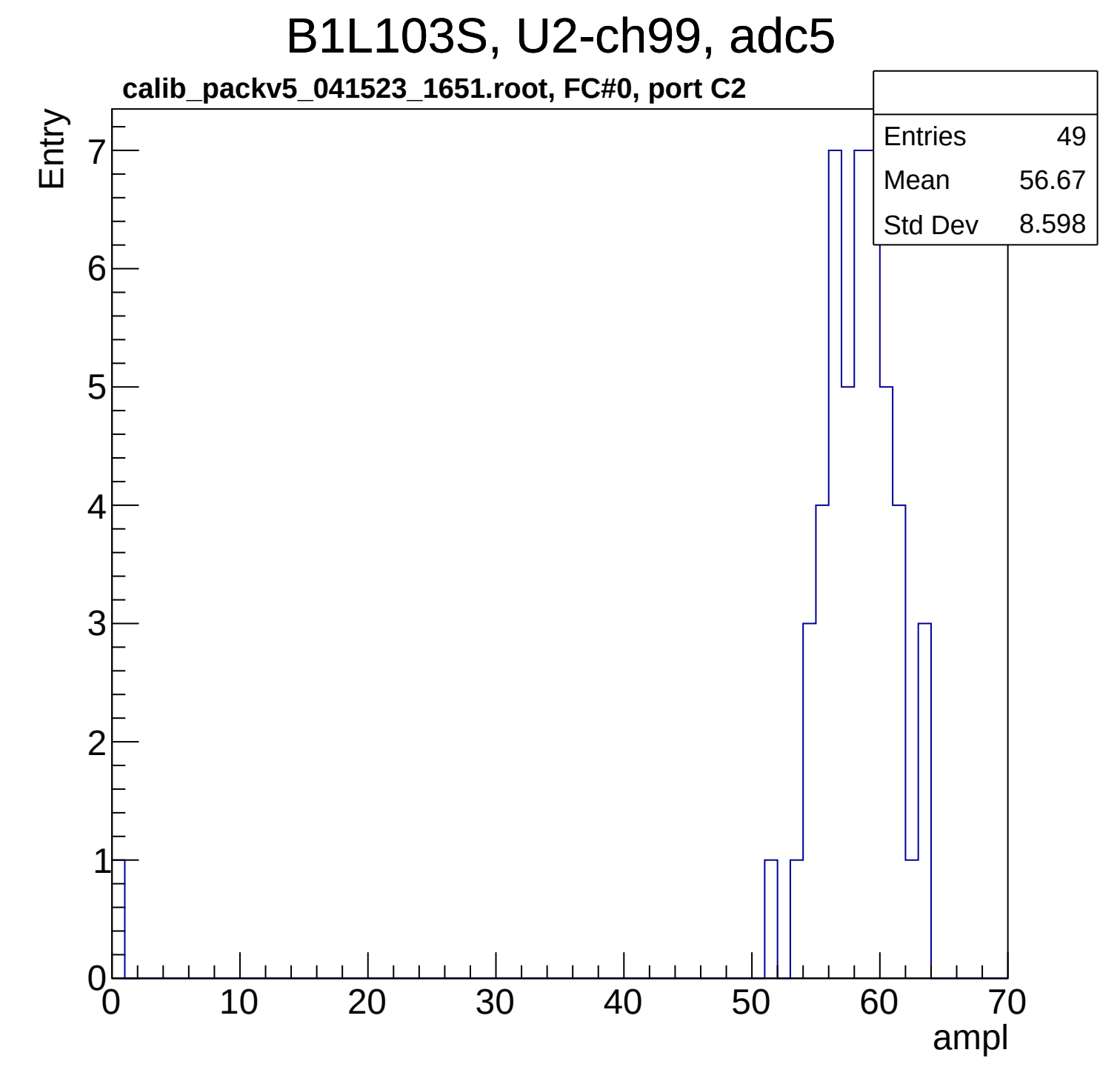

B1L103S, U2-ch99, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 140
Mean 17.87
Std Dev 13.2
Entry
0
5
10
15
20
25
30
35
40
45
0
10
20
30
40
50
60
70
ampl

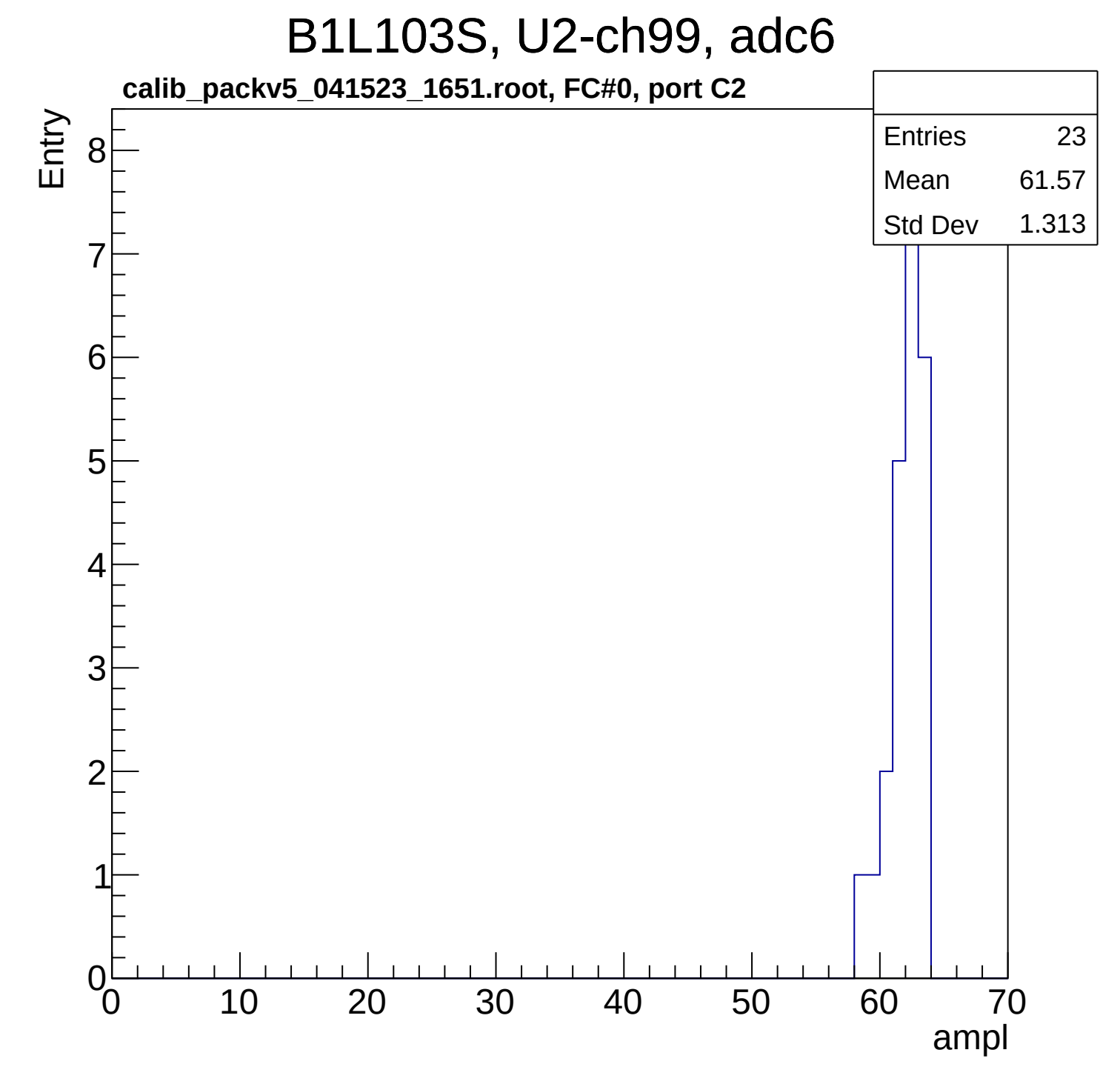

B1L103S, U2-ch99, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 30
Std Dev 11.91
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

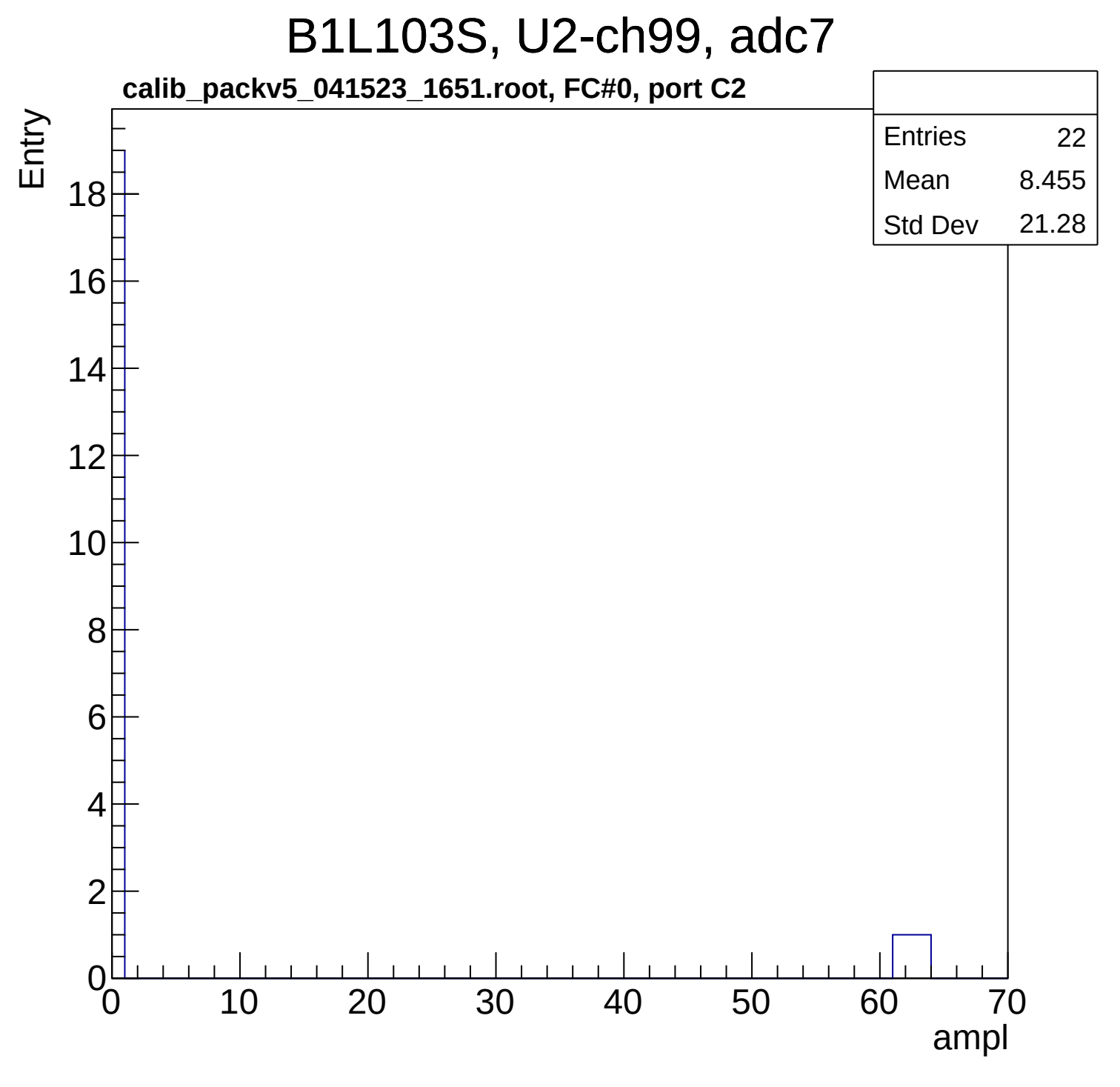

B1L103S, U2-ch99, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 38.99
Std Dev 10.73
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

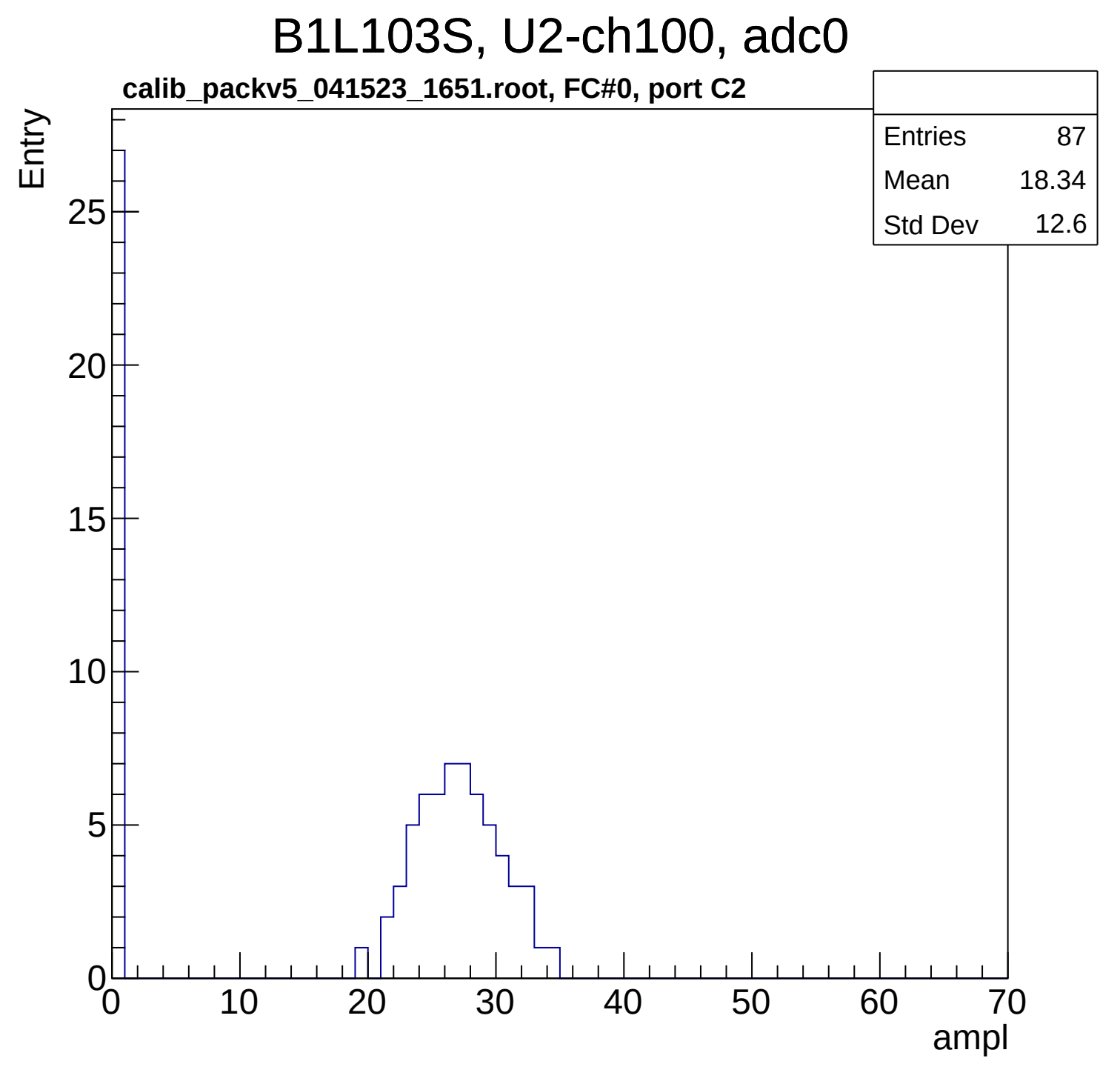

B1L103S, U2-ch99, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 47.75
Std Dev 3.496
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

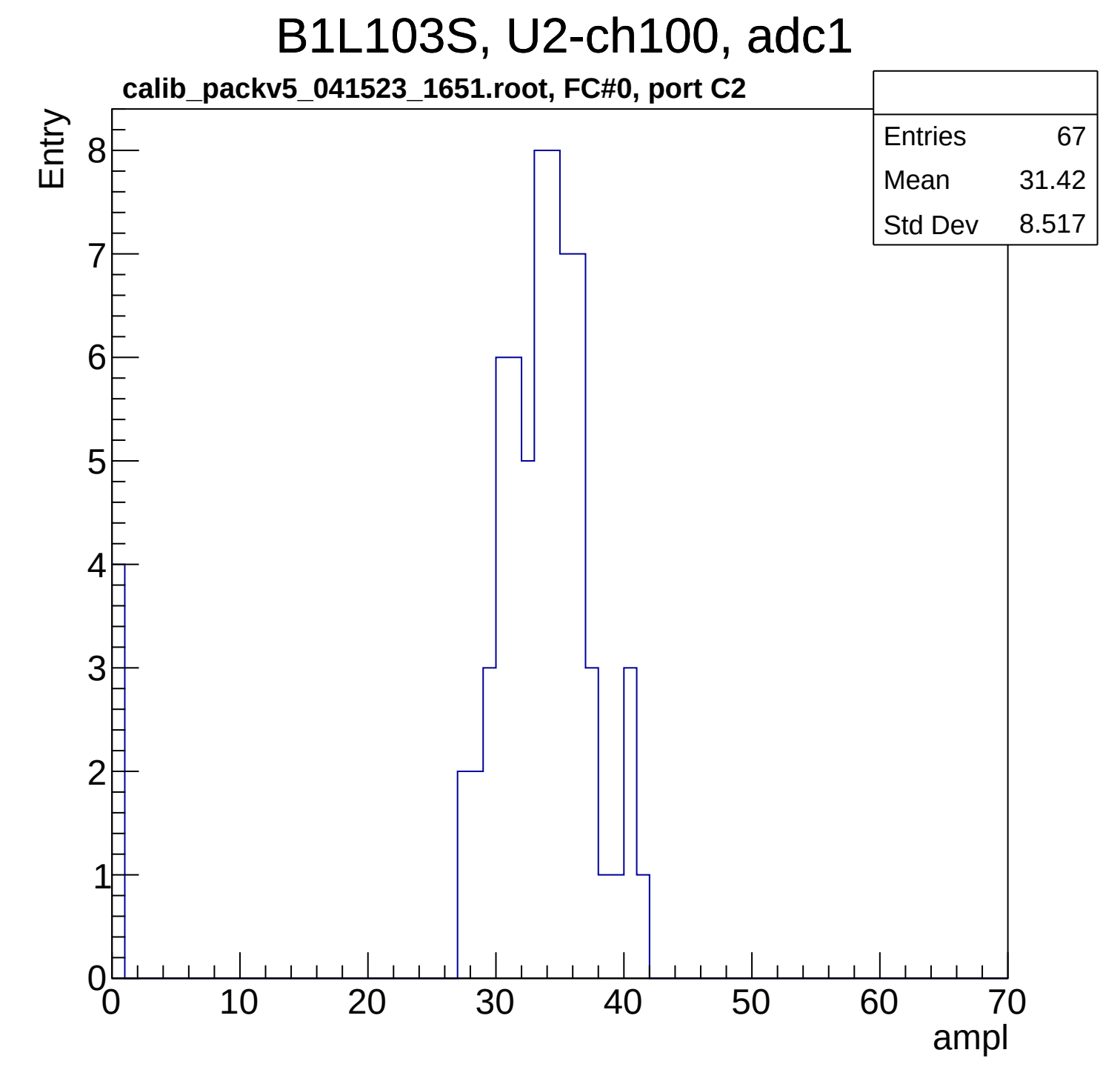

B1L103S, U2-ch99, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 53.63
Std Dev 3.311
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

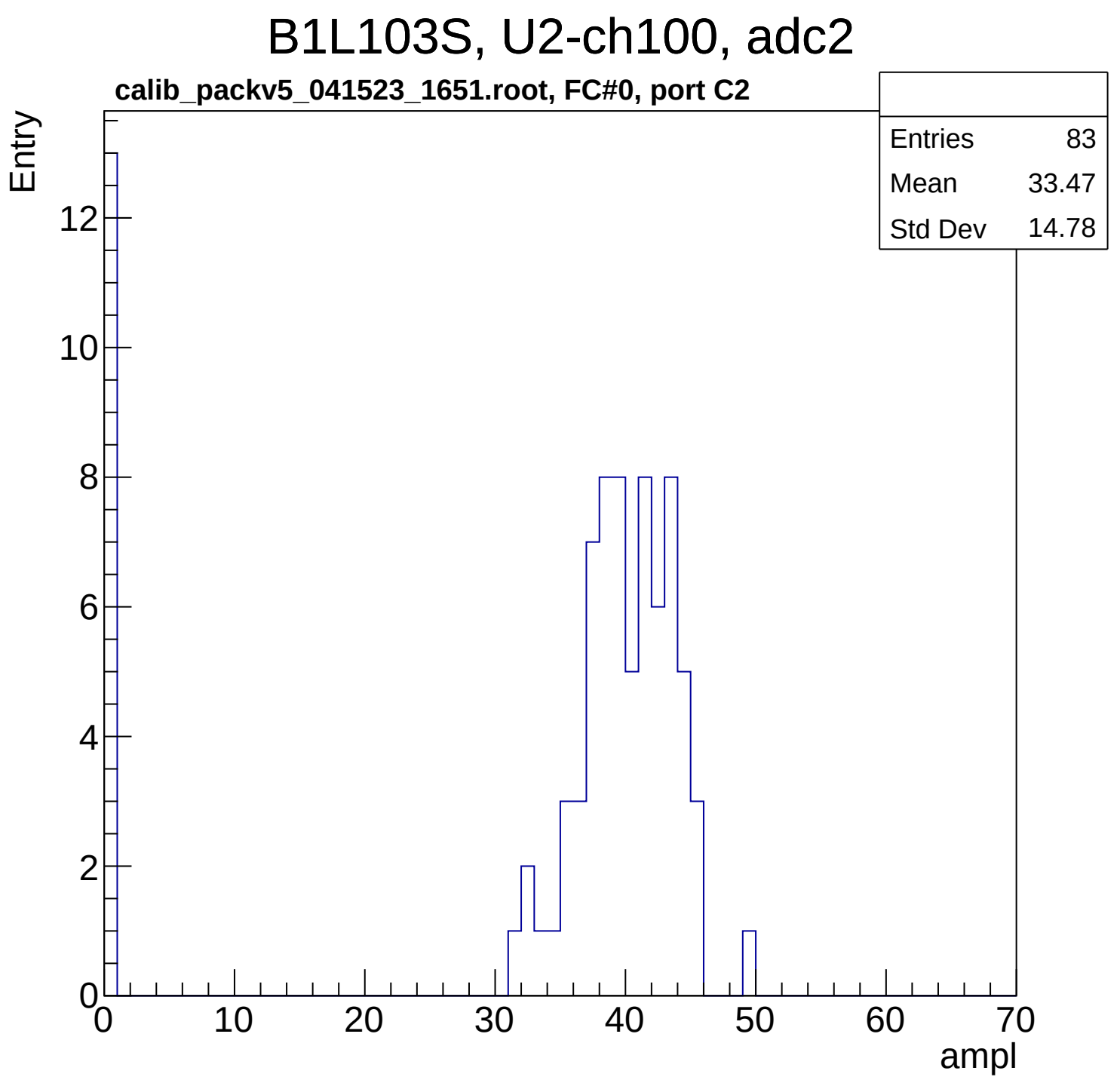

B1L103S, U2-ch99, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 56.67
Std Dev 8.598
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

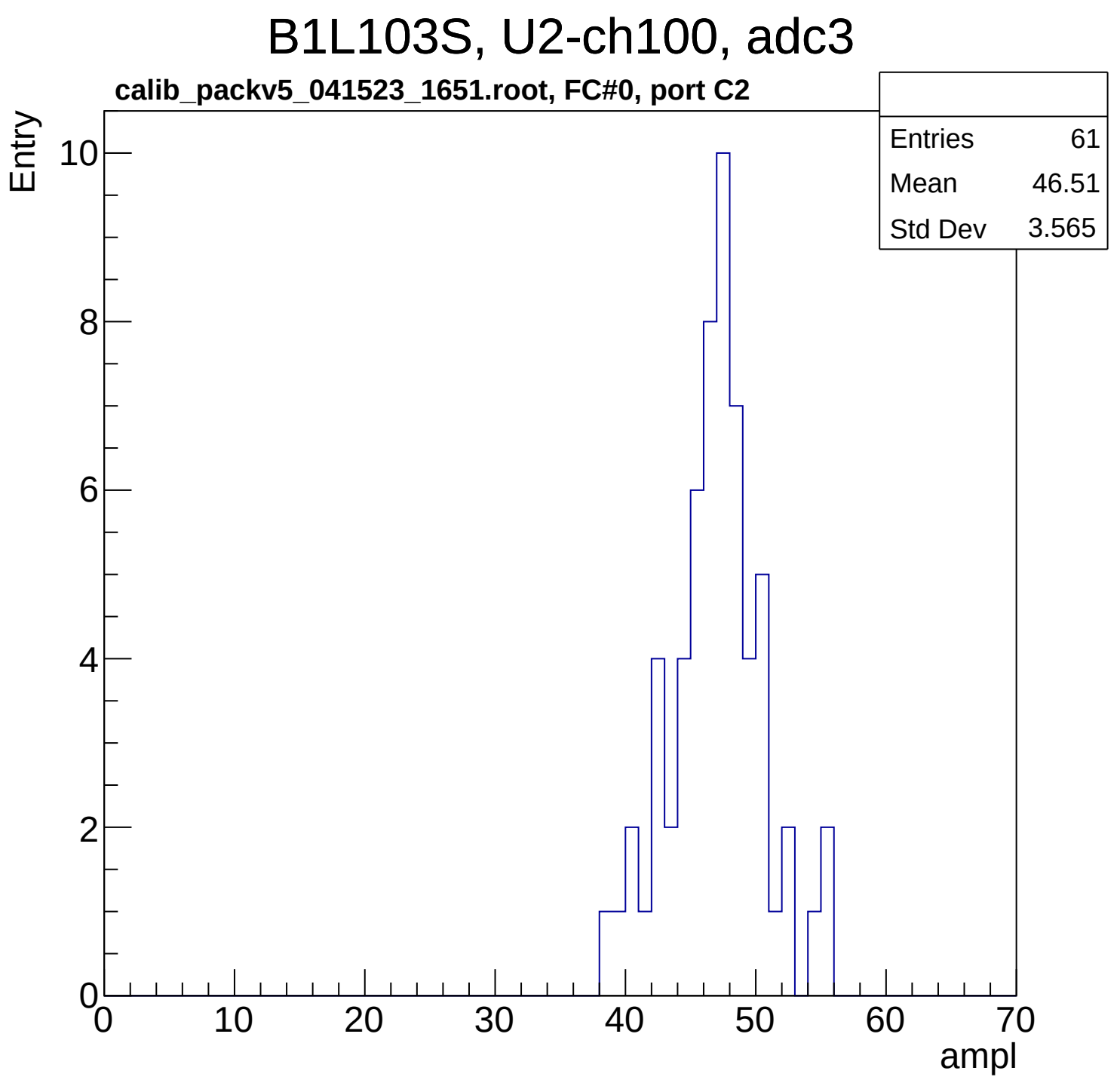

B1L103S, U2-ch99, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 61.57
Std Dev 1.313
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

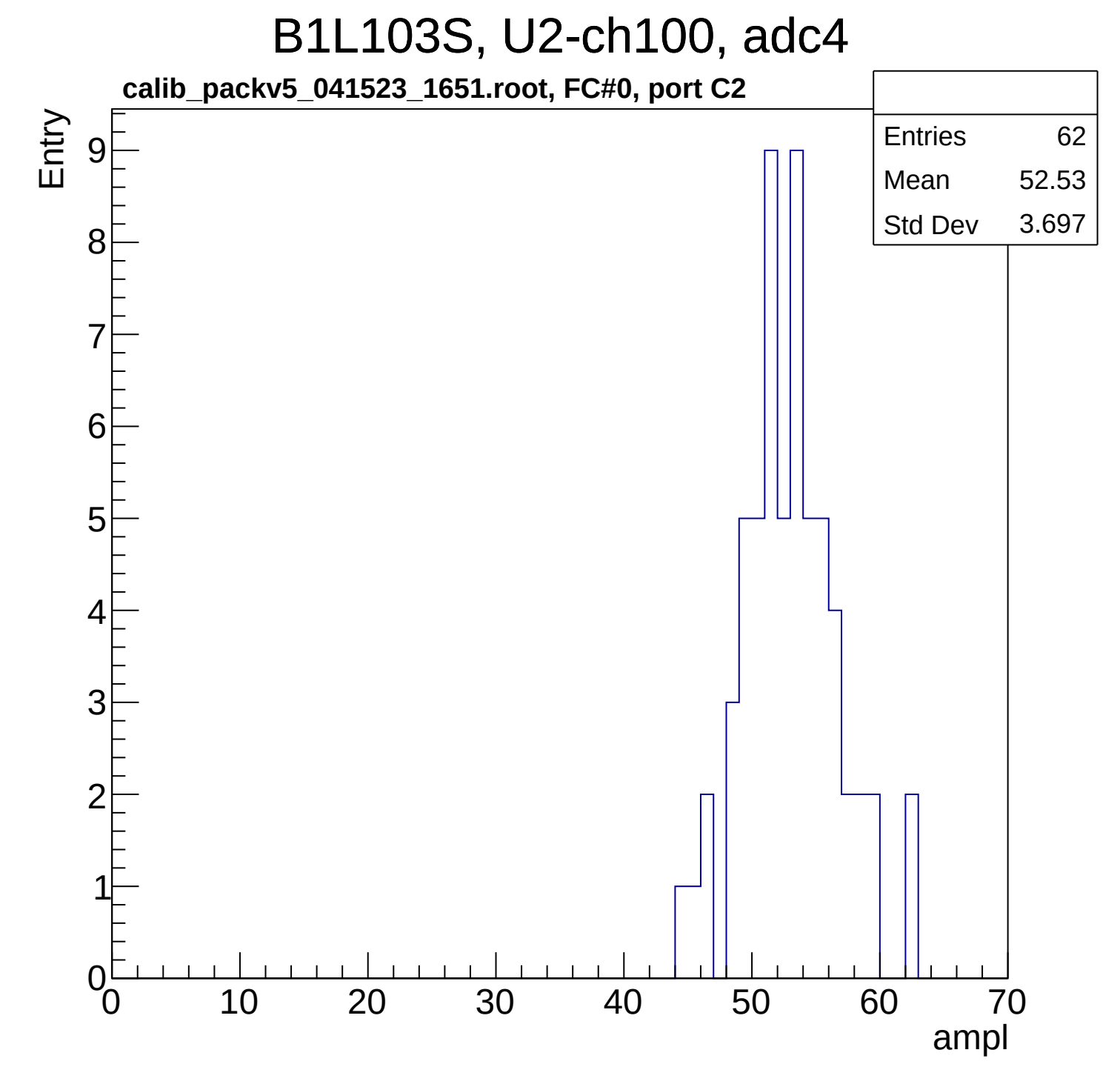

B1L103S, U2-ch99, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.455
Std Dev 21.28
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

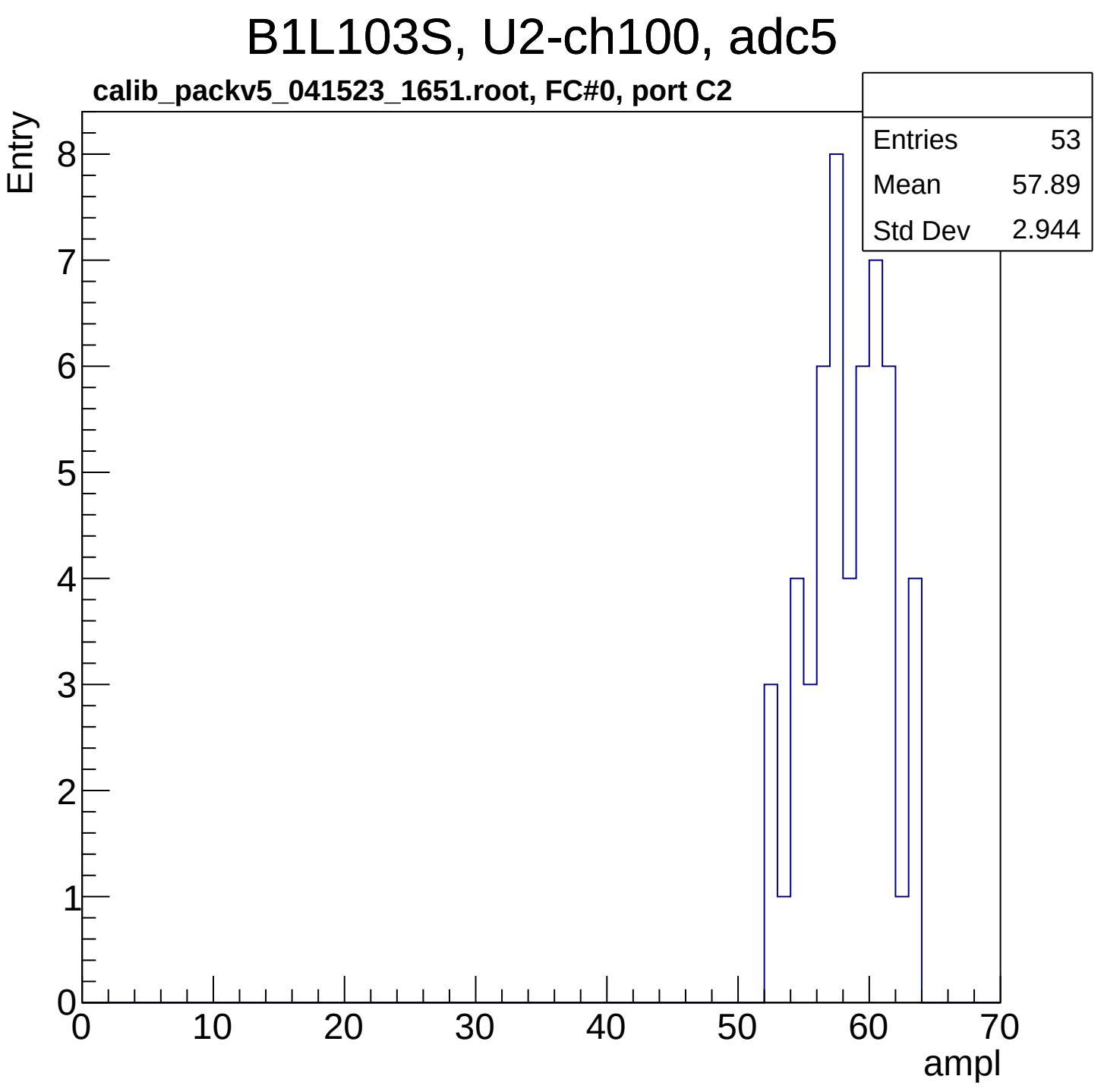

B1L103S, U2-ch100, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 18.34
Std Dev 12.6
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl

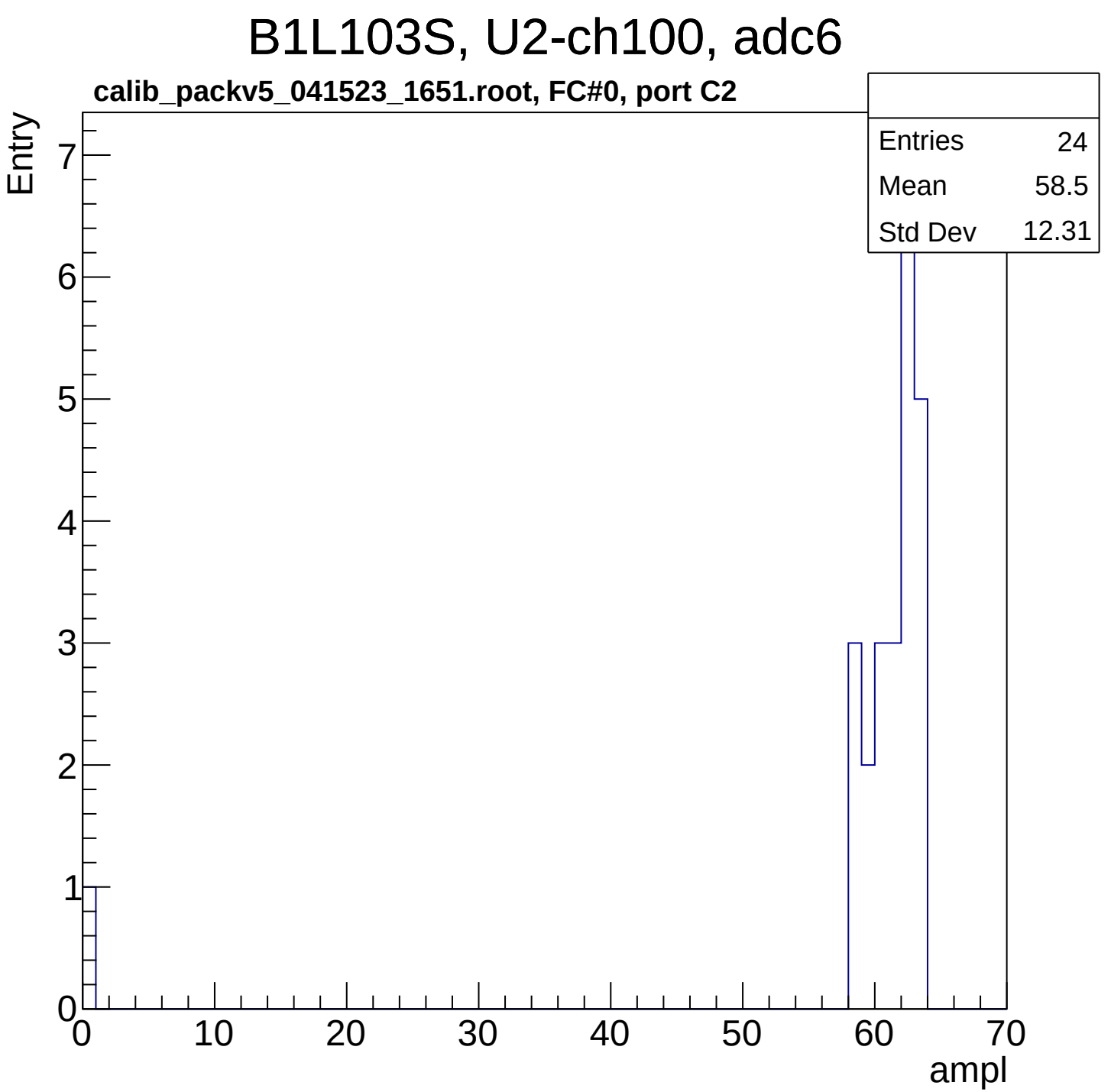

B1L103S, U2-ch100, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 31.42
Std Dev 8.517
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

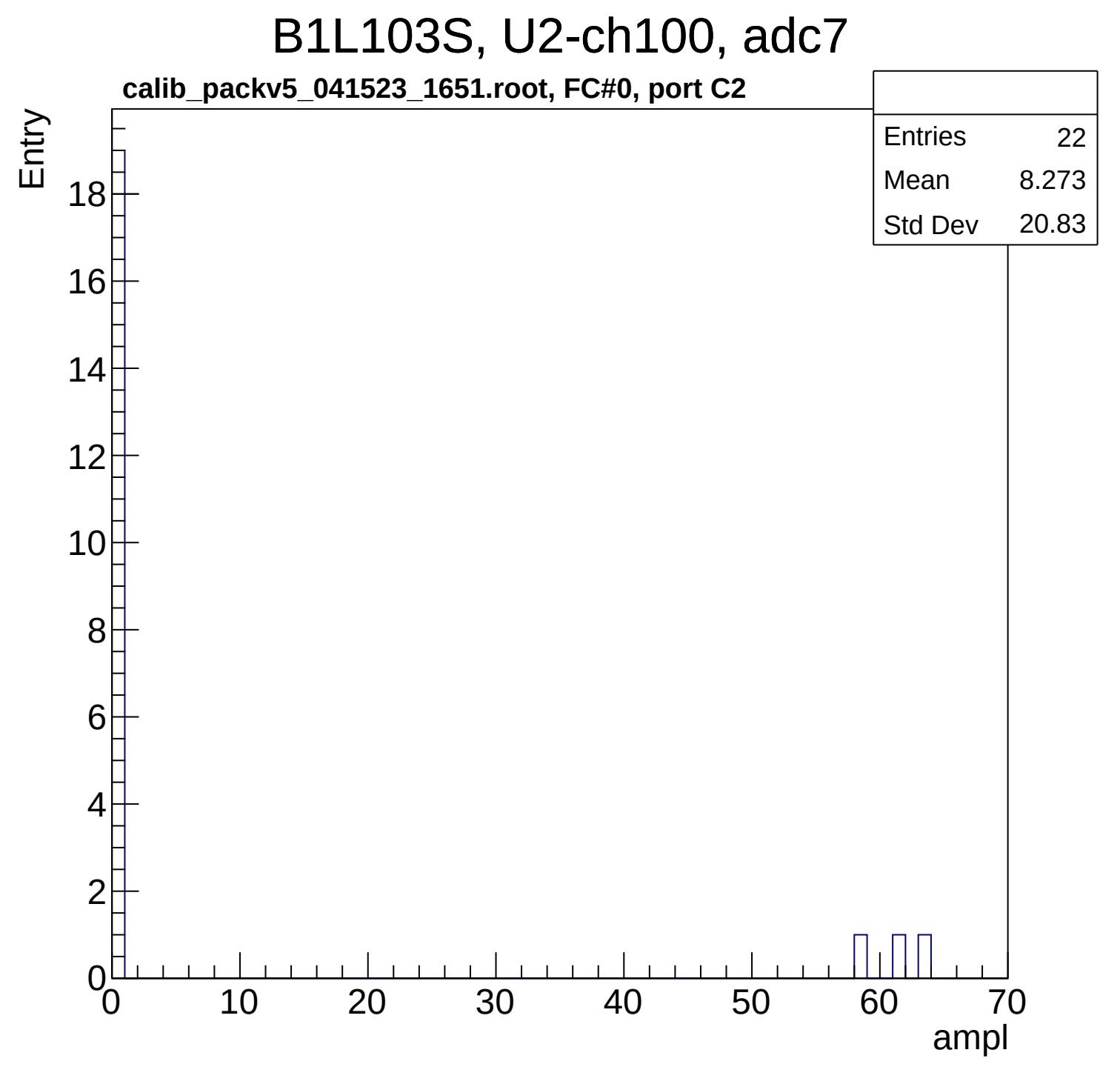

B1L103S, U2-ch100, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 33.47
Std Dev 14.78
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

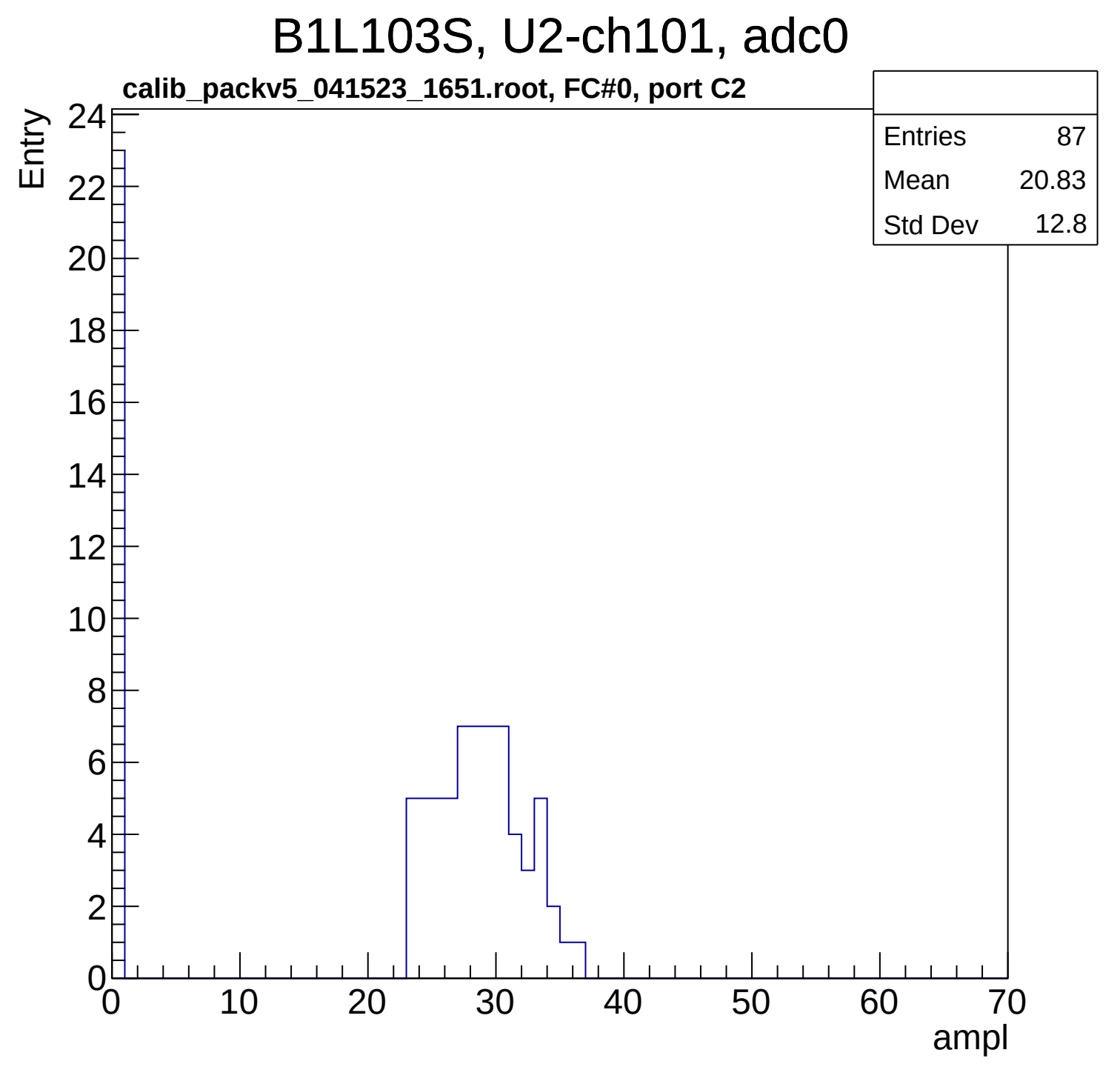

B1L103S, U2-ch100, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 46.51
Std Dev 3.565
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

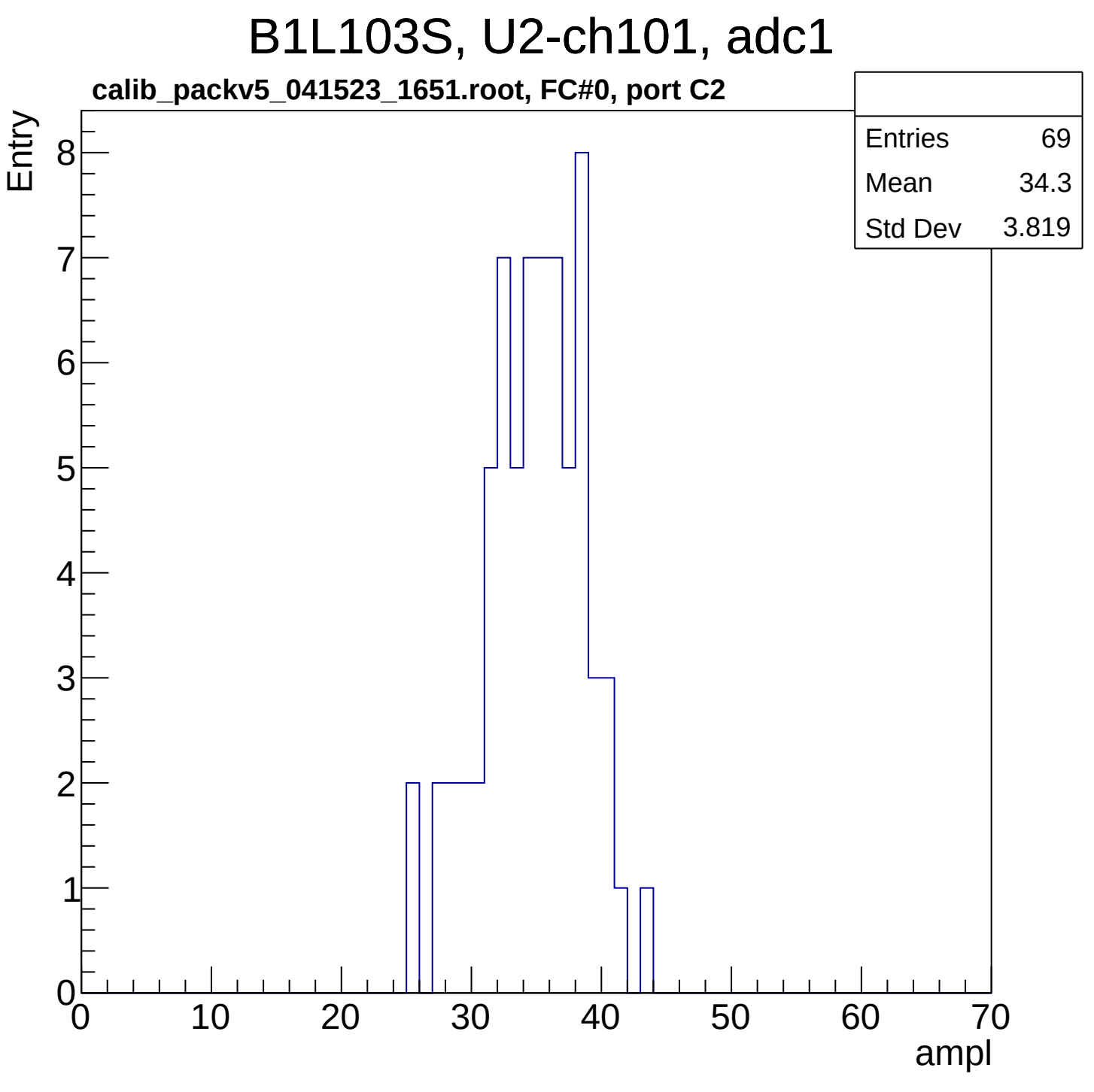

B1L103S, U2-ch100, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 52.53
Std Dev 3.697
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

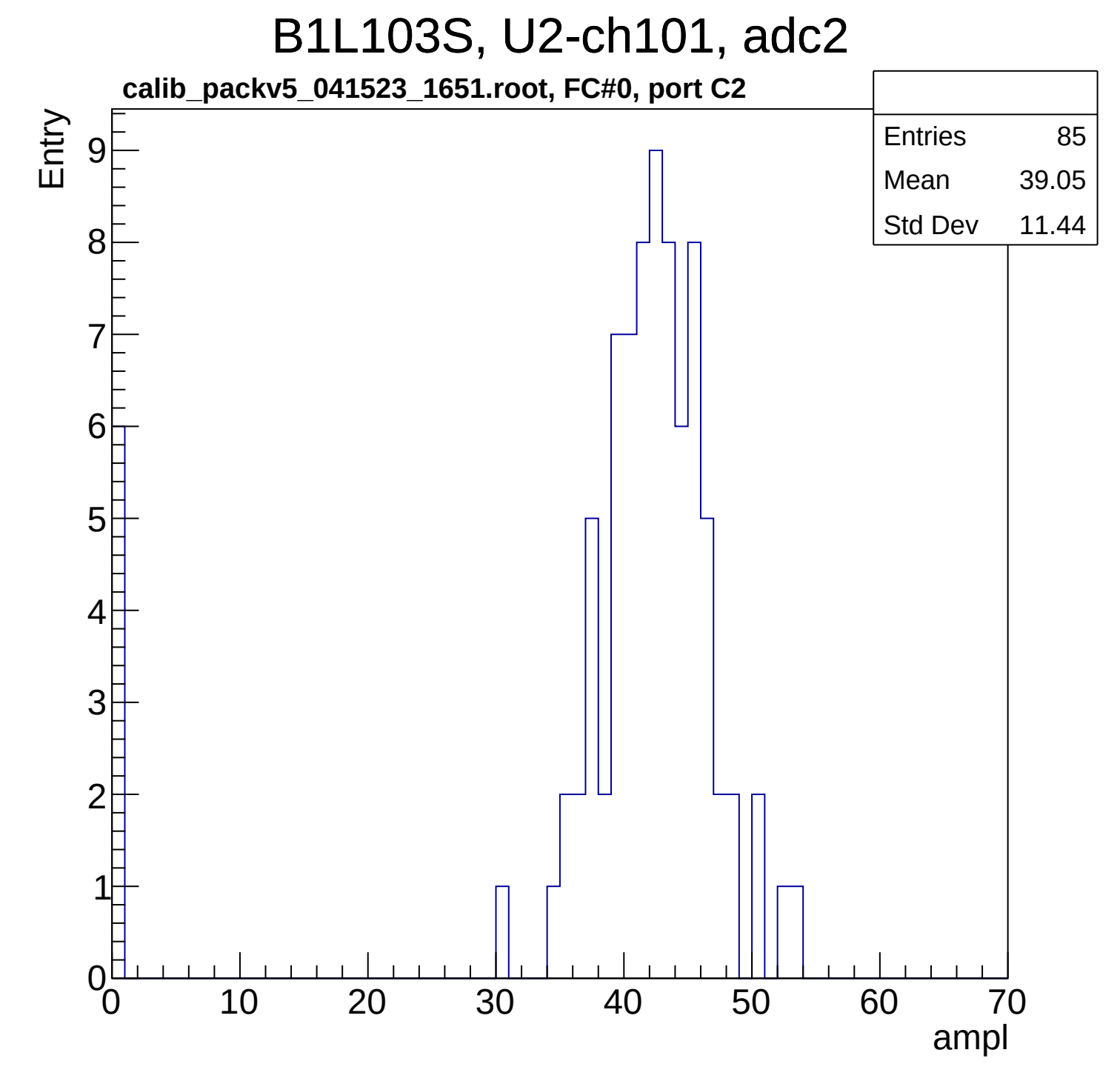

B1L103S, U2-ch100, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 57.89
Std Dev 2.944
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

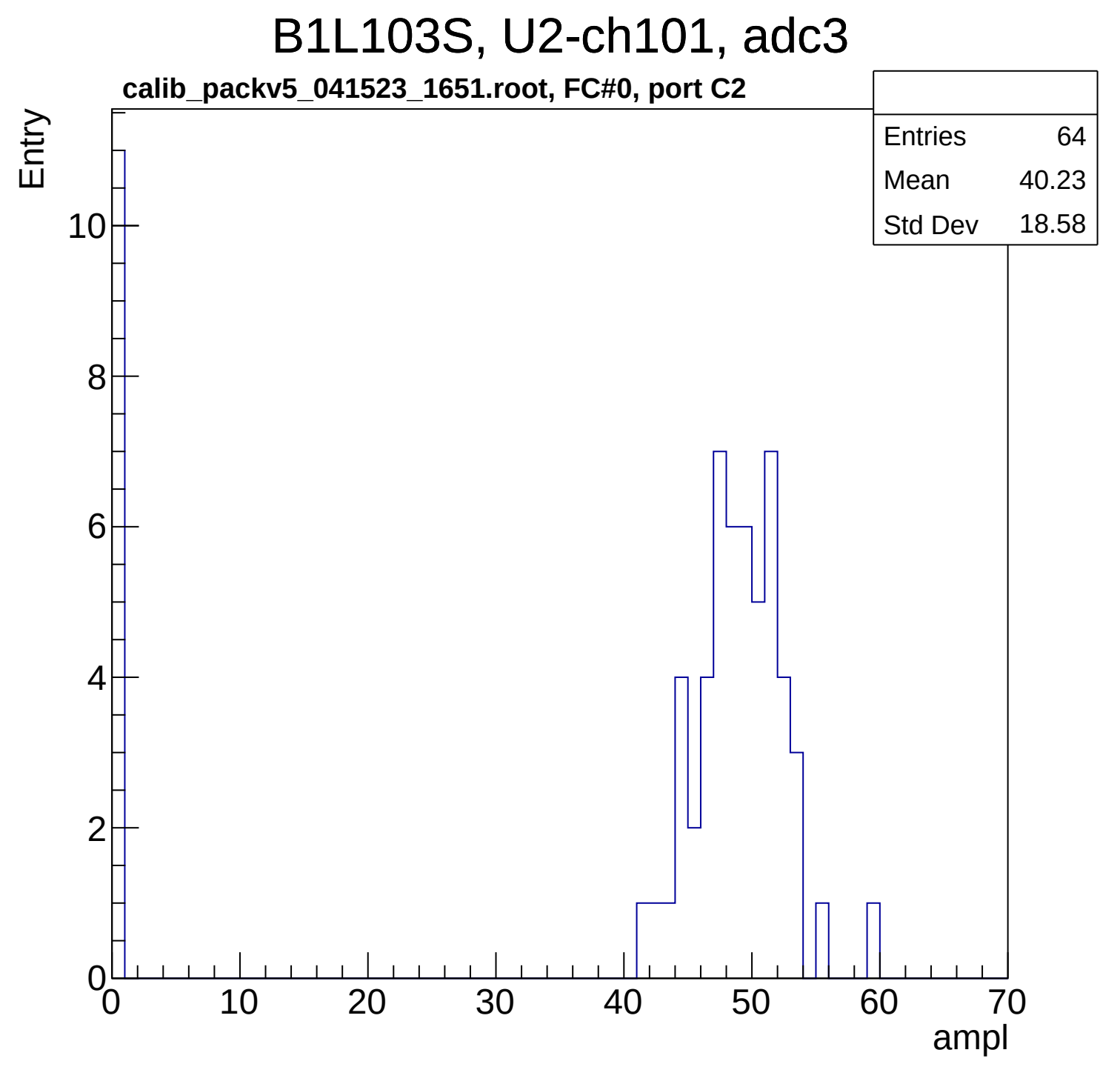

B1L103S, U2-ch100, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 58.5
Std Dev 12.31
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

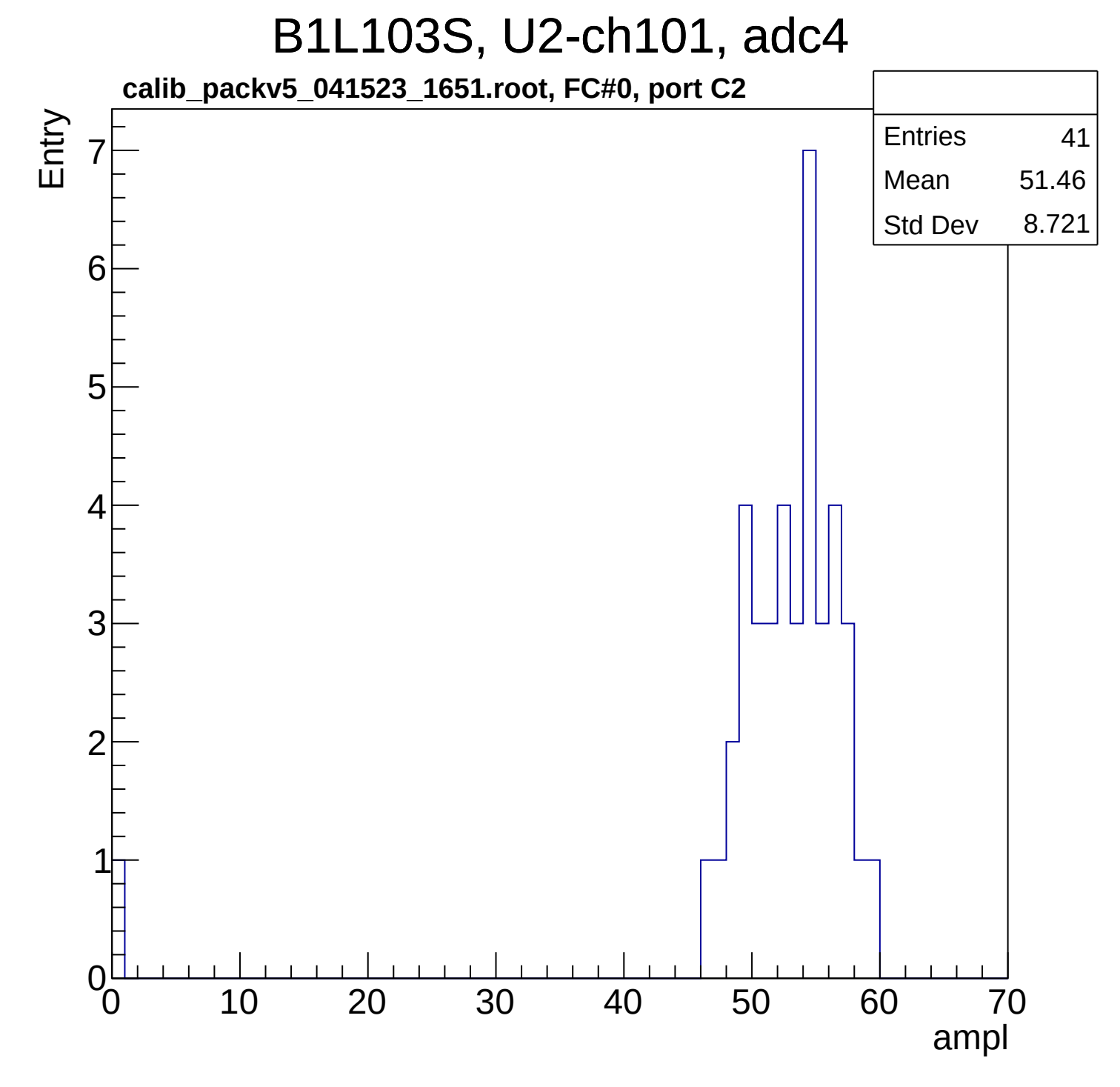

B1L103S, U2-ch100, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.273
Std Dev 20.83
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

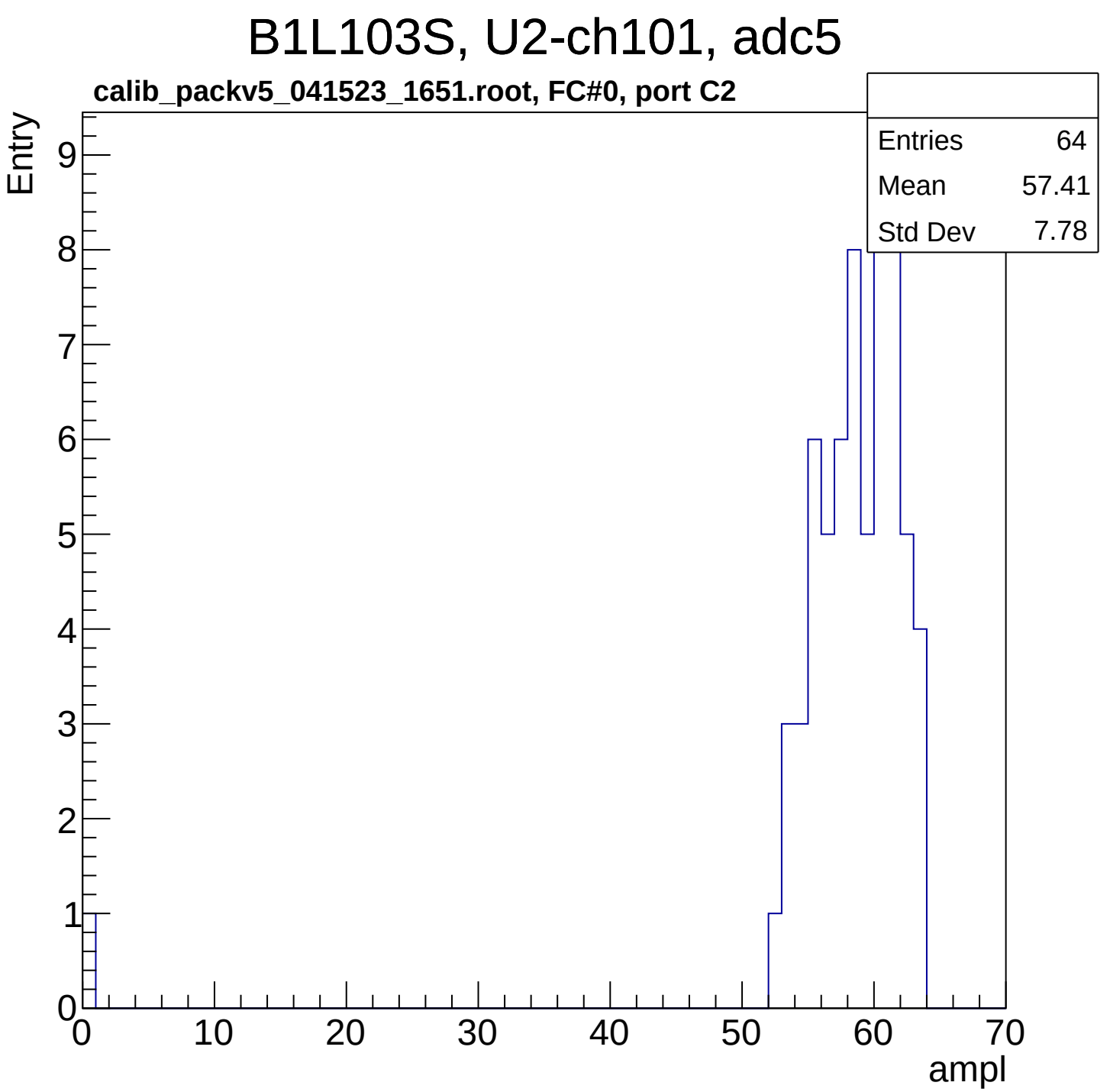

B1L103S, U2-ch101, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 20.83
Std Dev 12.8
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70

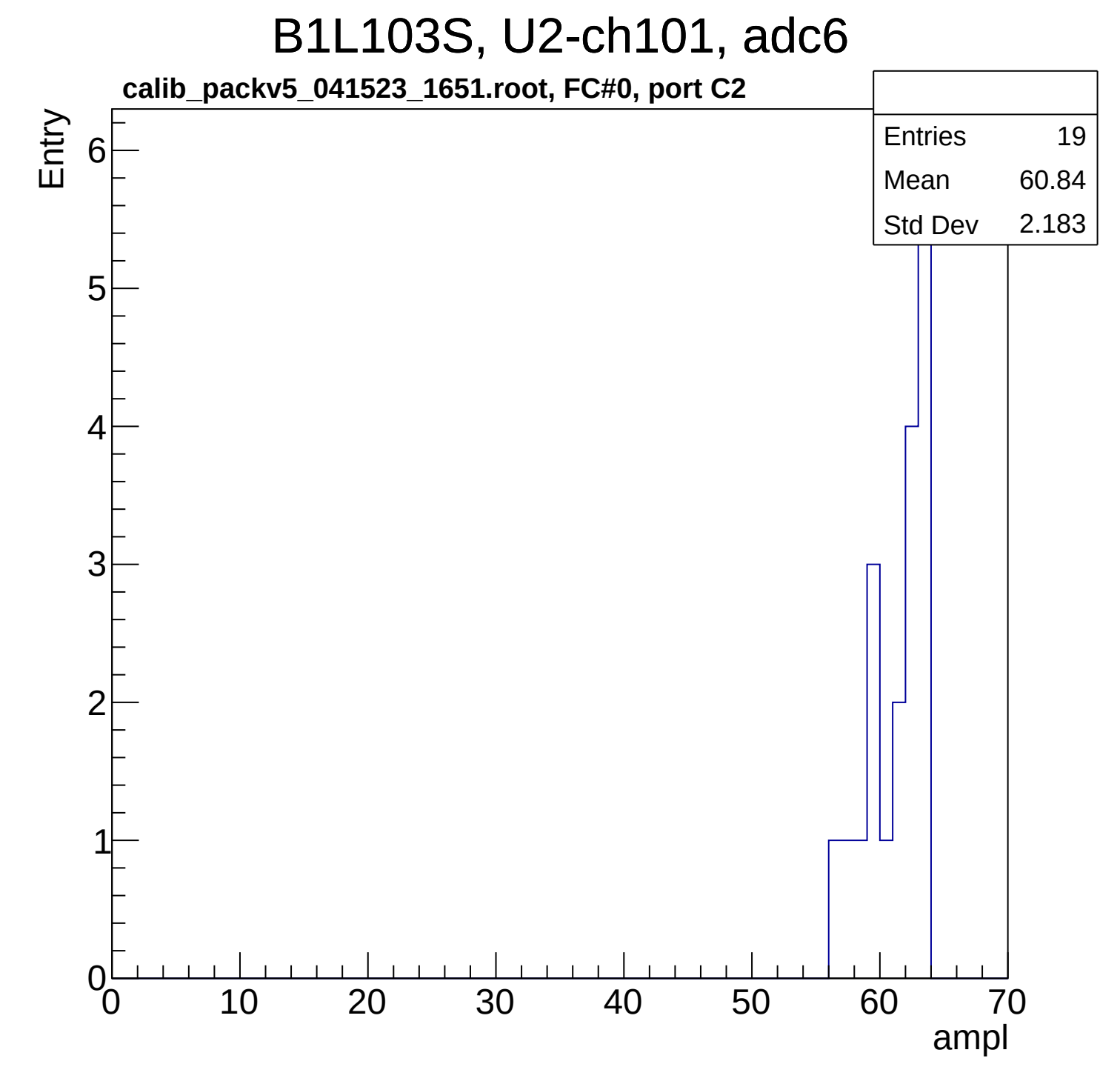

B1L103S, U2-ch101, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 34.3
Std Dev 3.819
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

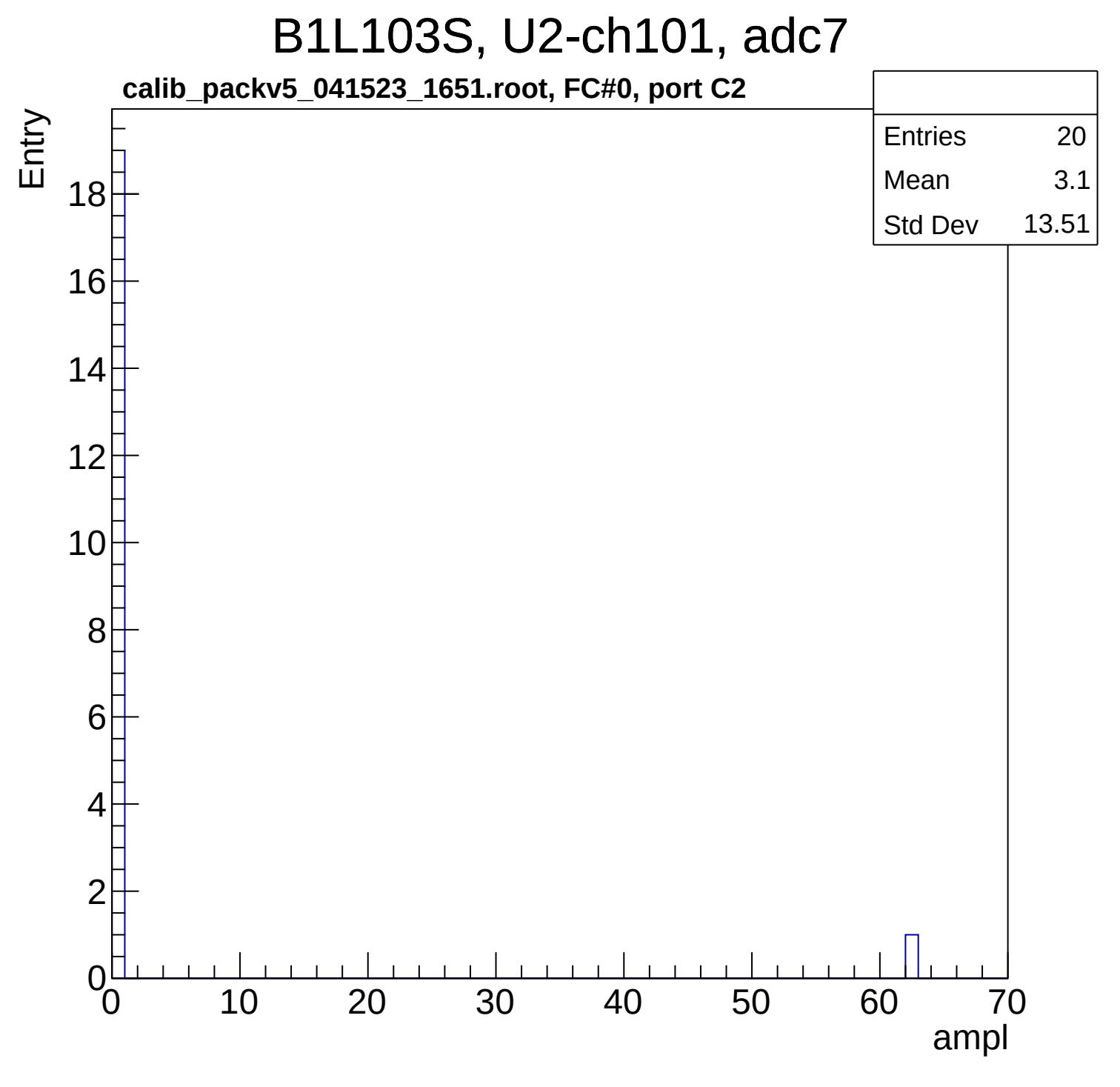

B1L103S, U2-ch101, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 39.05
Std Dev 11.44
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

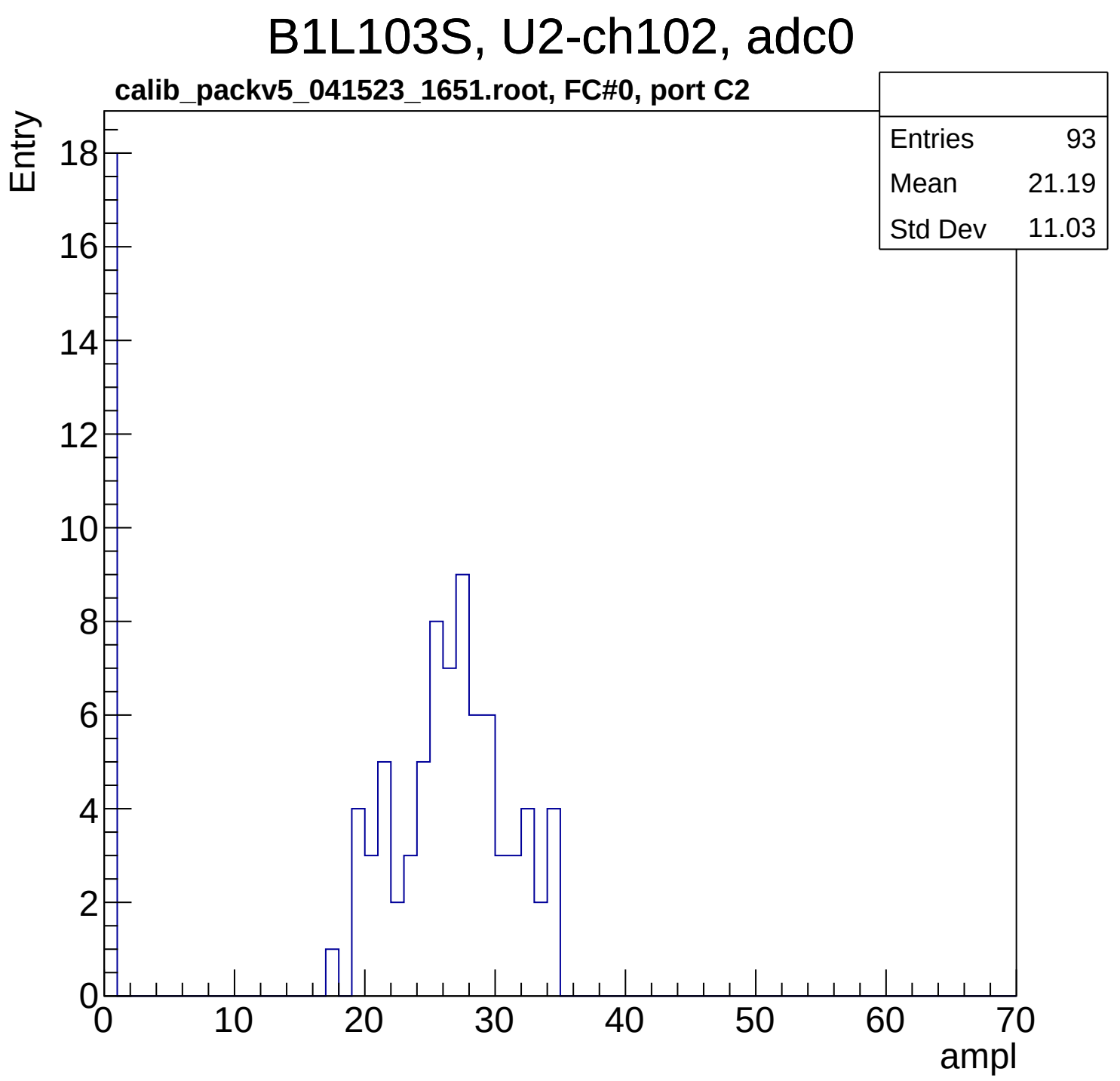

B1L103S, U2-ch101, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 40.23
Std Dev 18.58
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

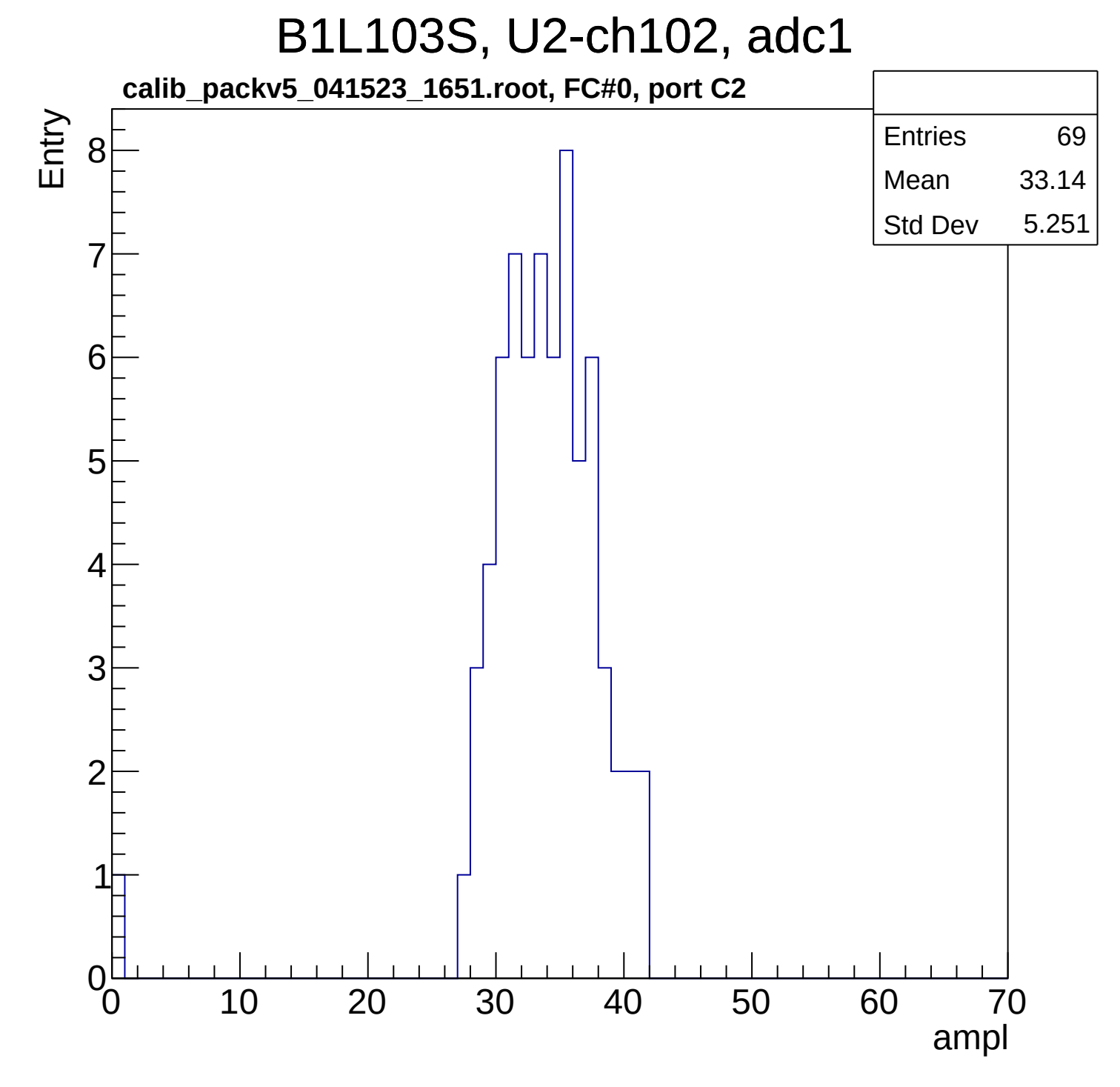

B1L103S, U2-ch101, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 51.46
Std Dev 8.721
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

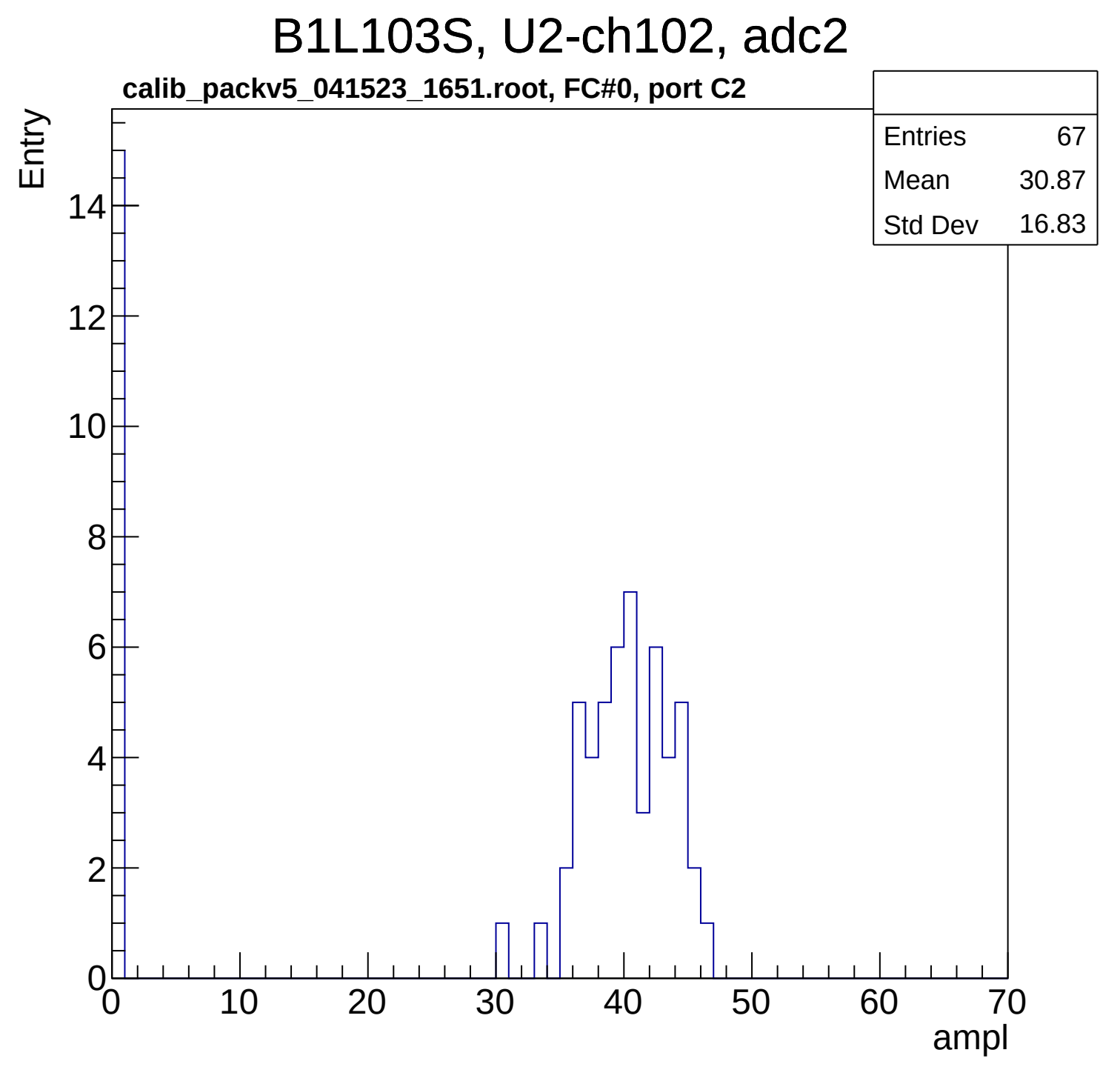

B1L103S, U2-ch101, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 57.41
Std Dev 7.78
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

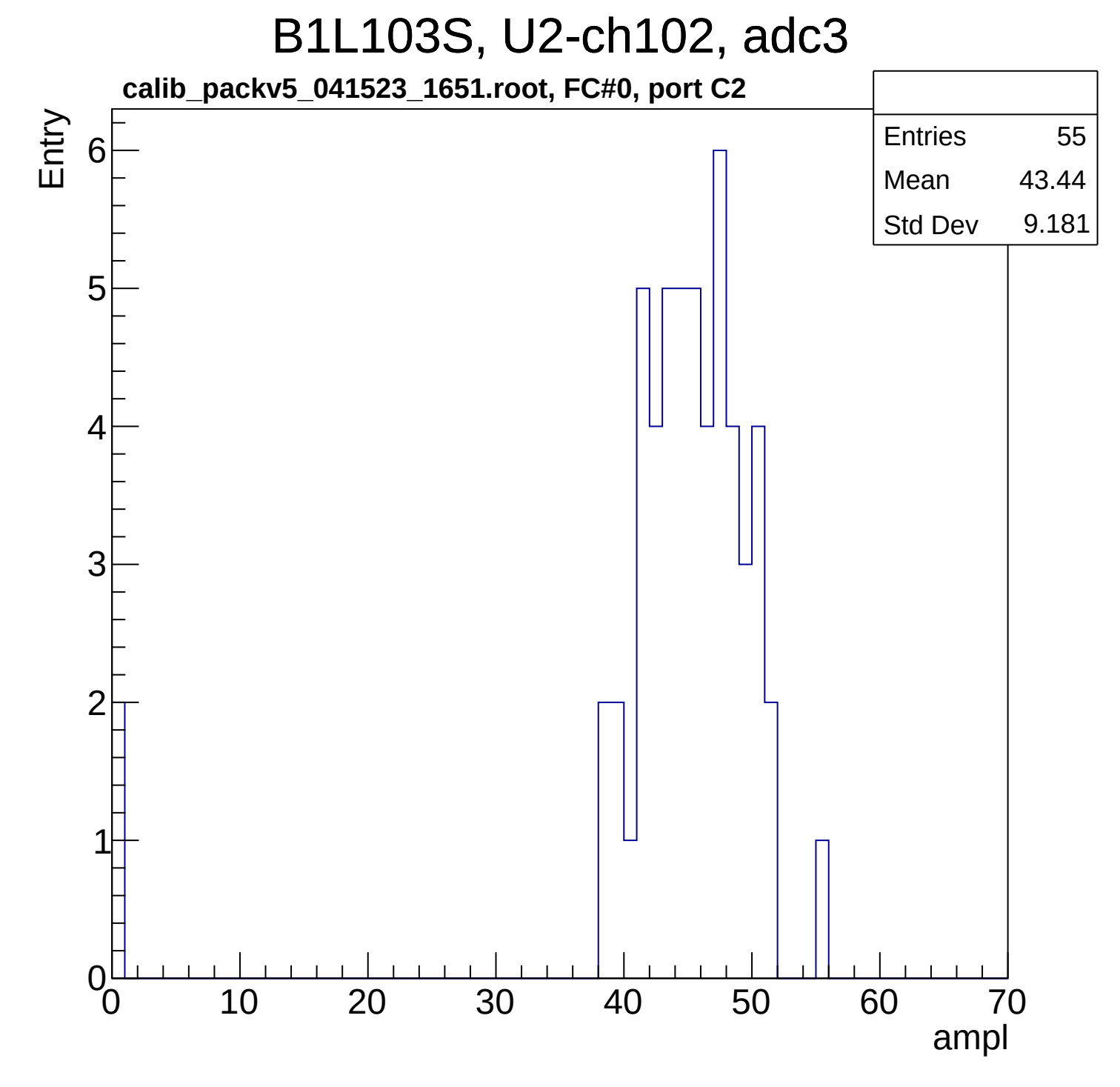

B1L103S, U2-ch101, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 60.84
Std Dev 2.183
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

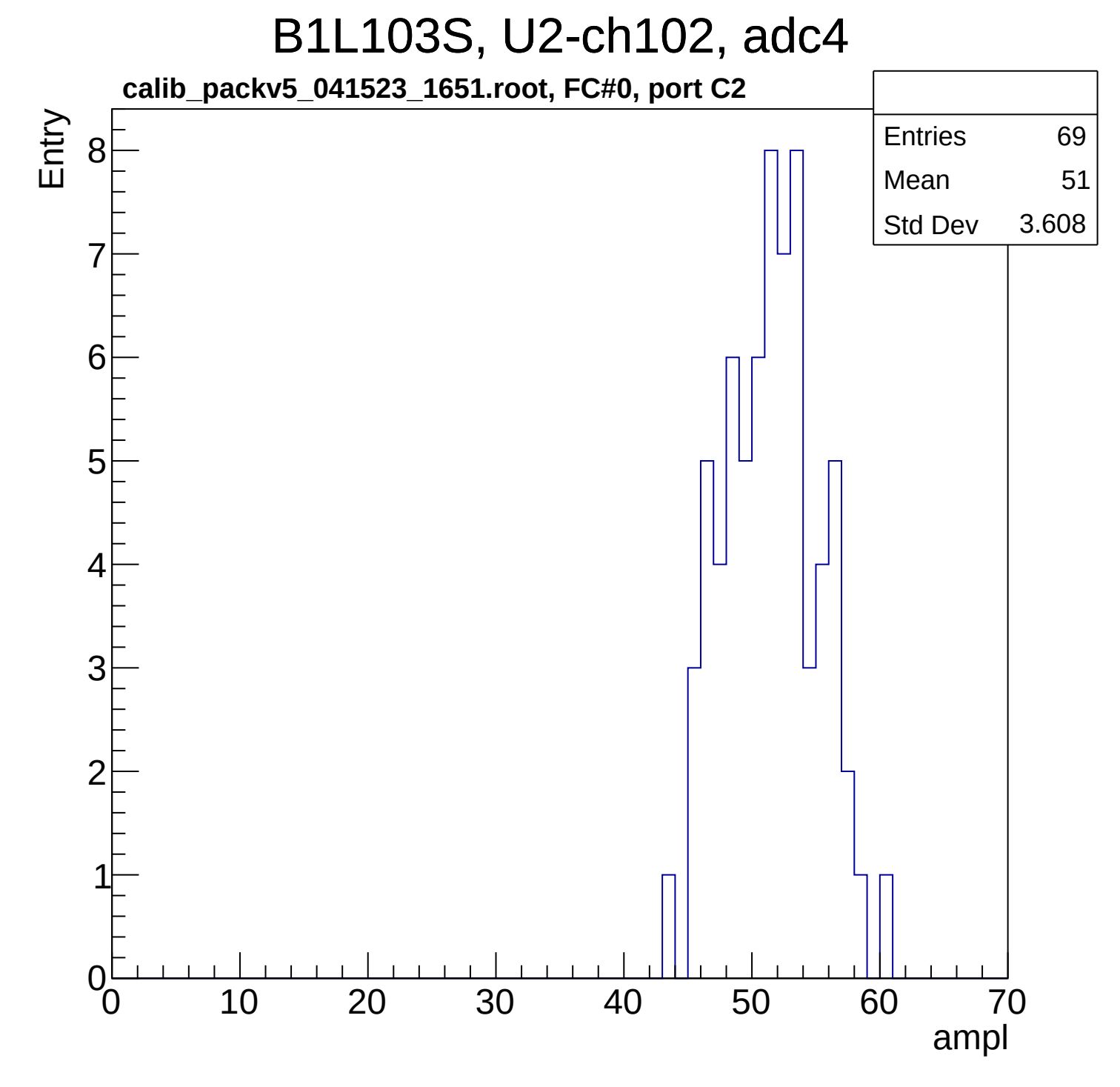

B1L103S, U2-ch101, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

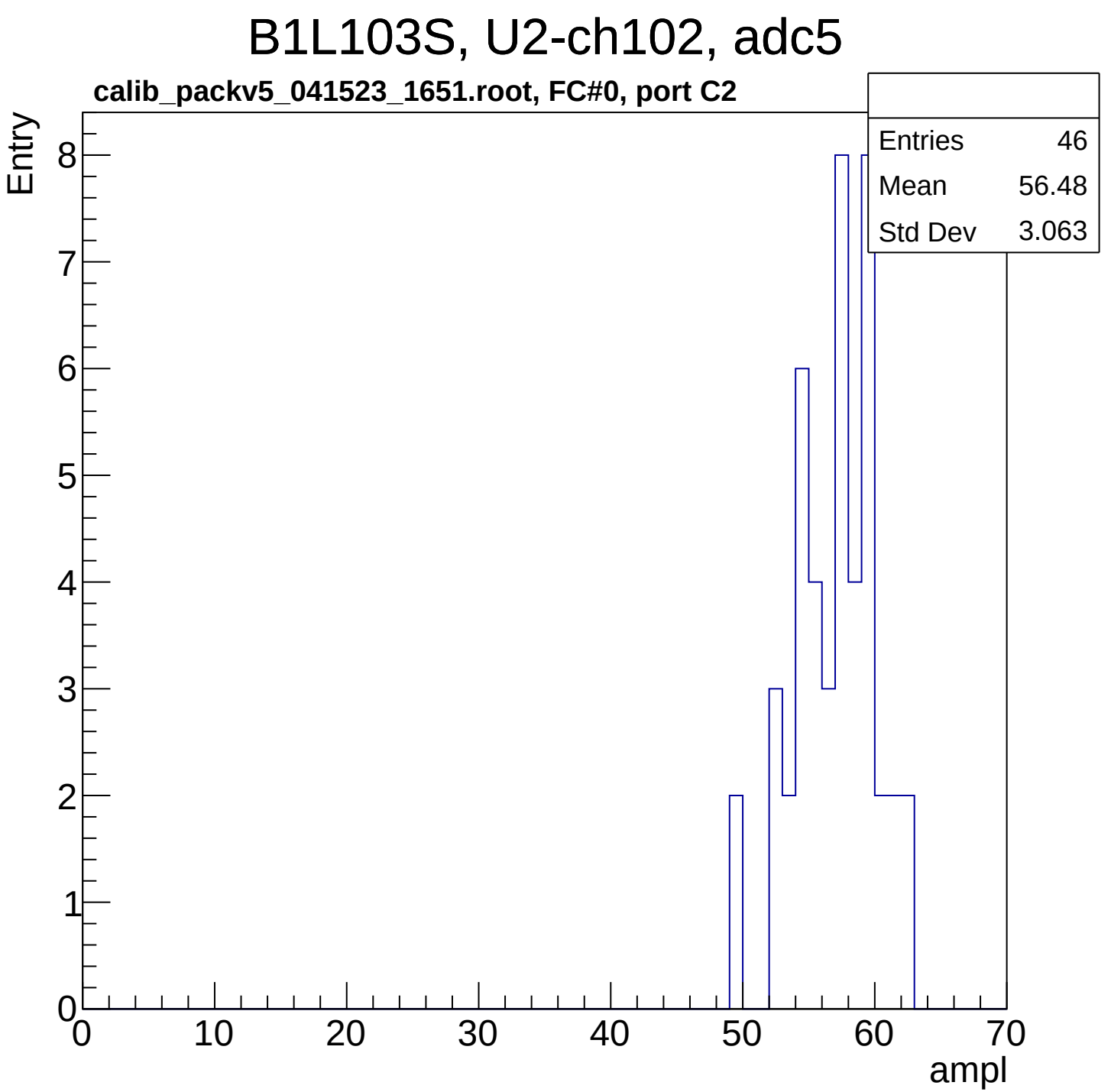

B1L103S, U2-ch102, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 21.19
Std Dev 11.03
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

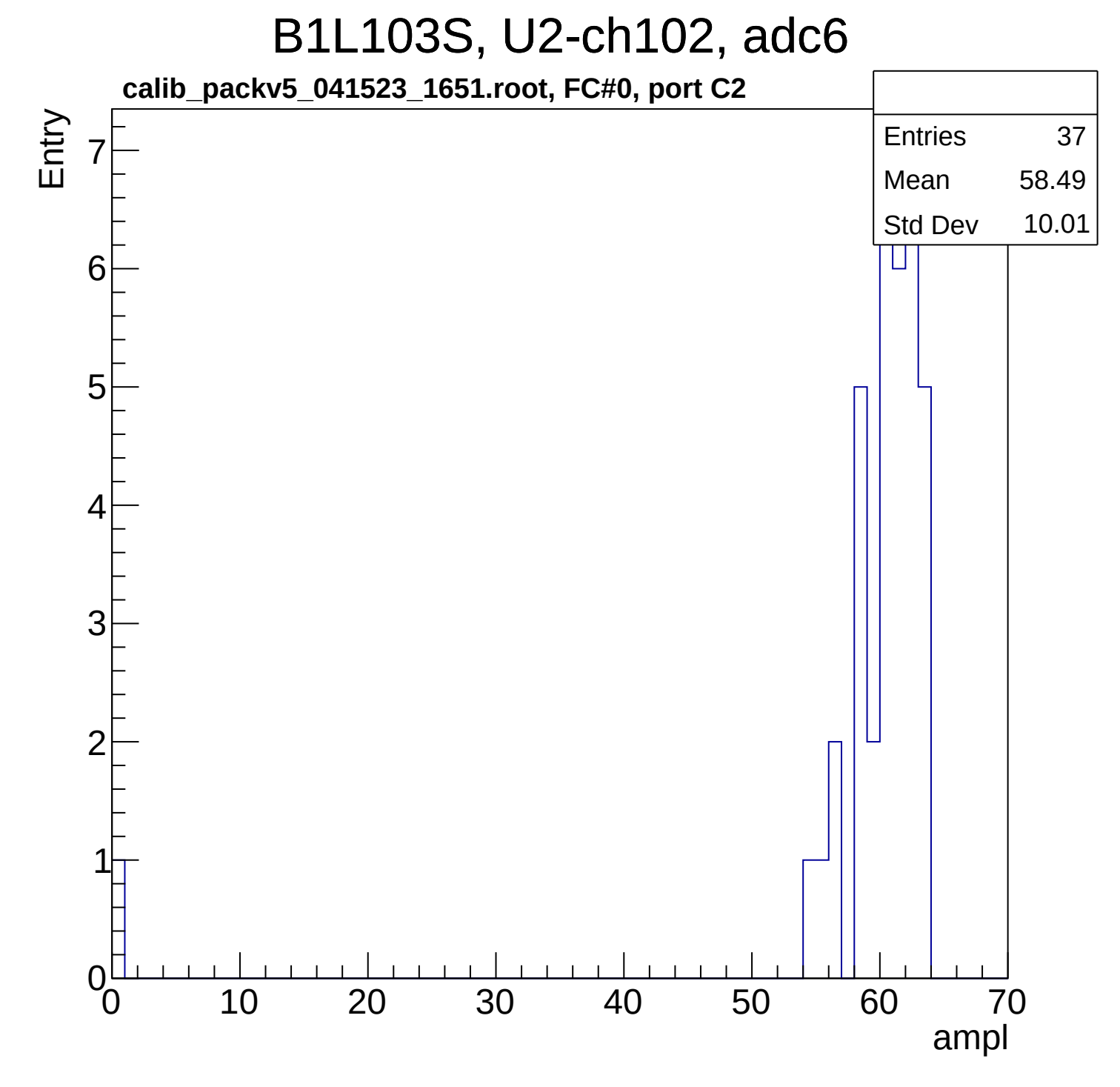

B1L103S, U2-ch102, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 33.14
Std Dev 5.251
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

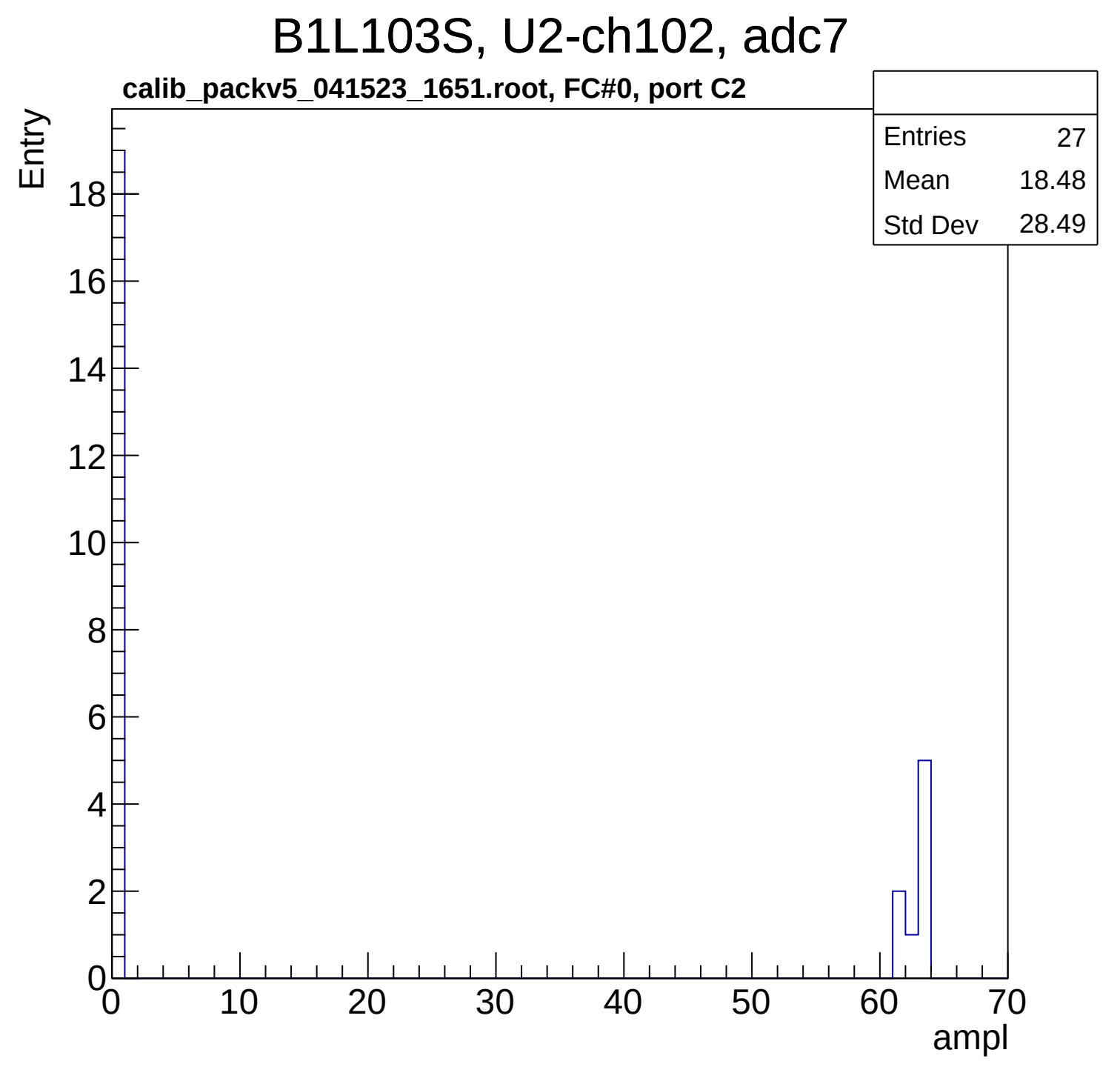

B1L103S, U2-ch102, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 30.87
Std Dev 16.83
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

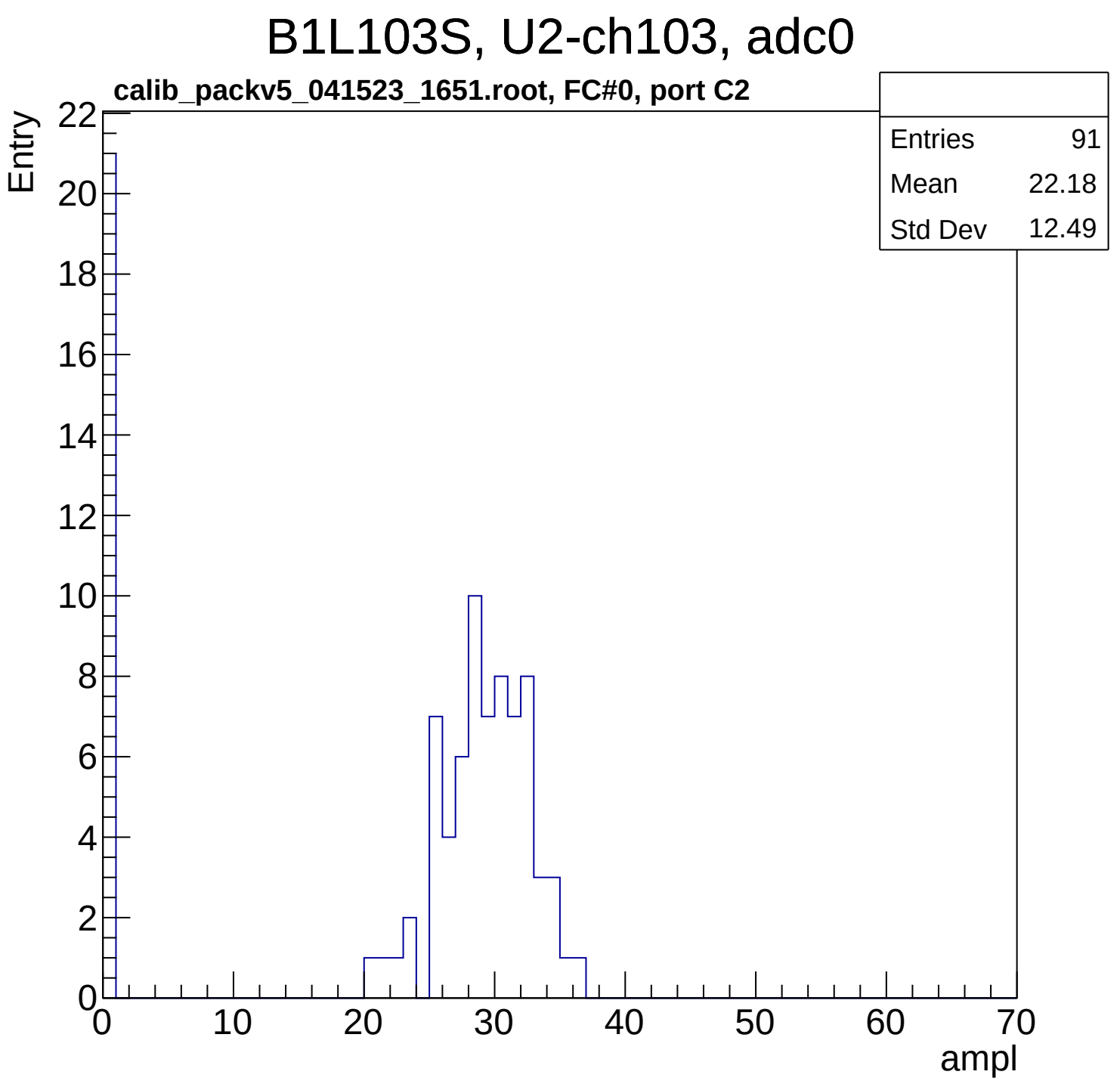

B1L103S, U2-ch102, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 43.44
Std Dev 9.181
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

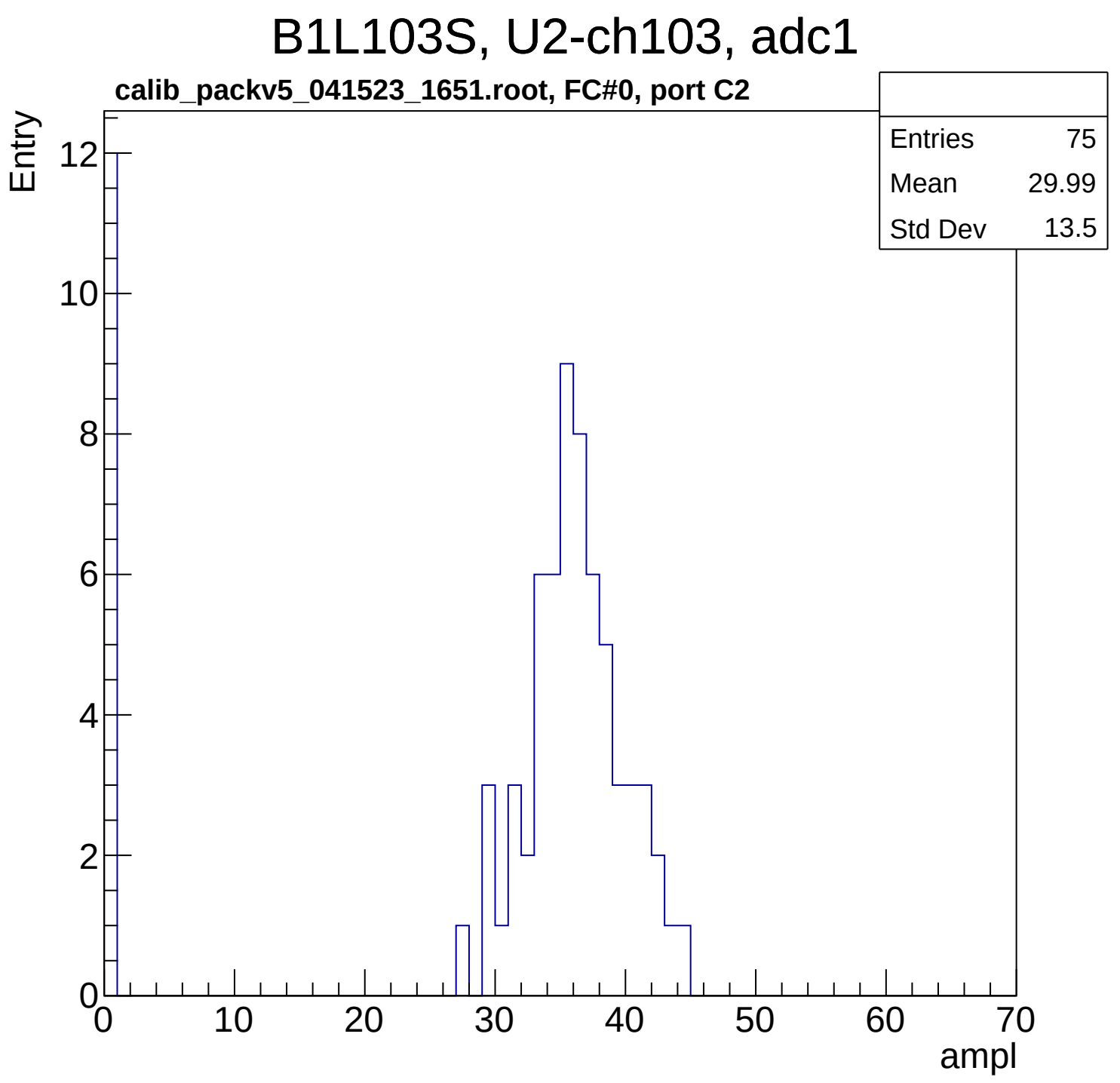

B1L103S, U2-ch102, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 51
Std Dev 3.608
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

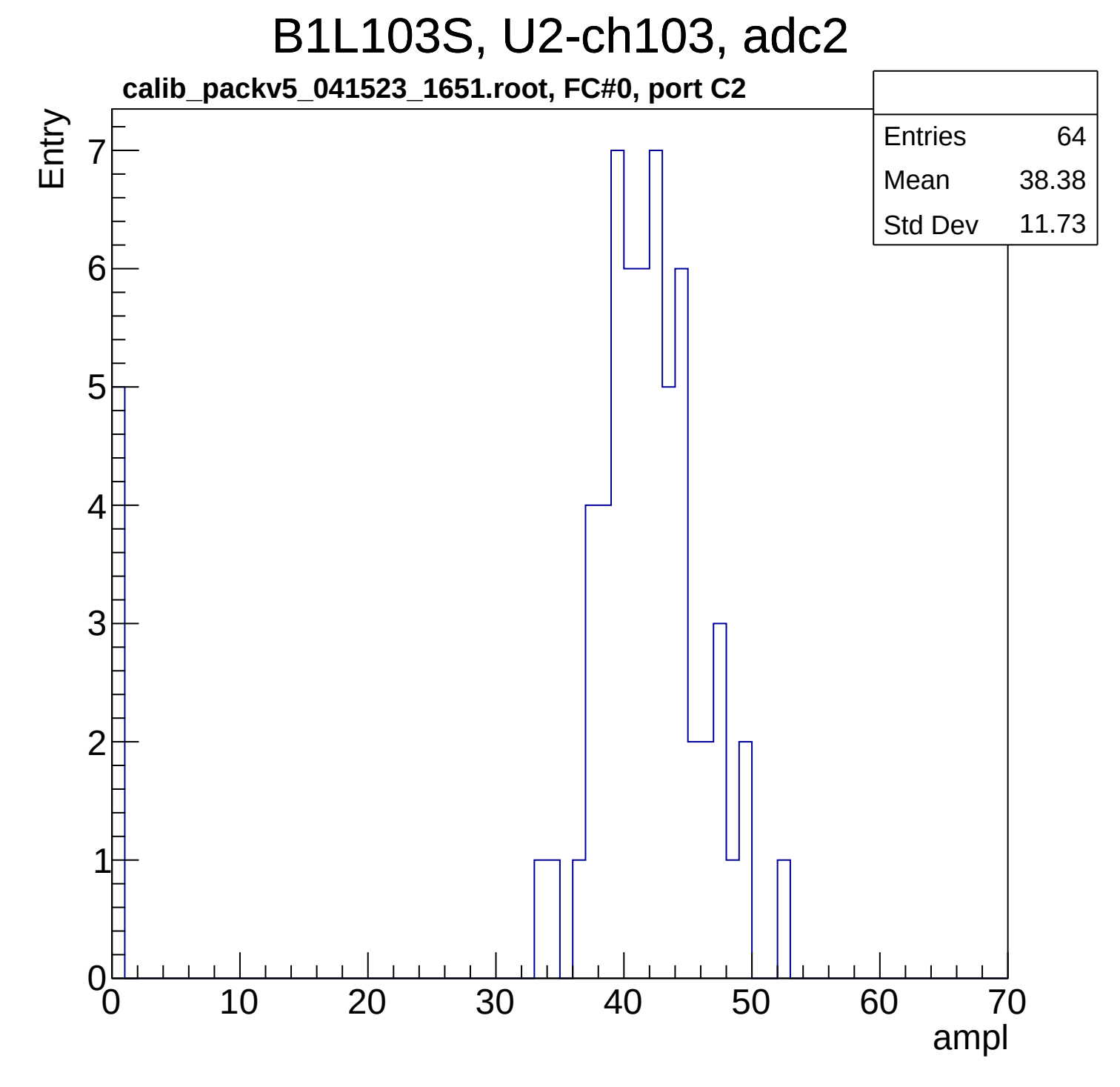

B1L103S, U2-ch102, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 56.48
Std Dev 3.063
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

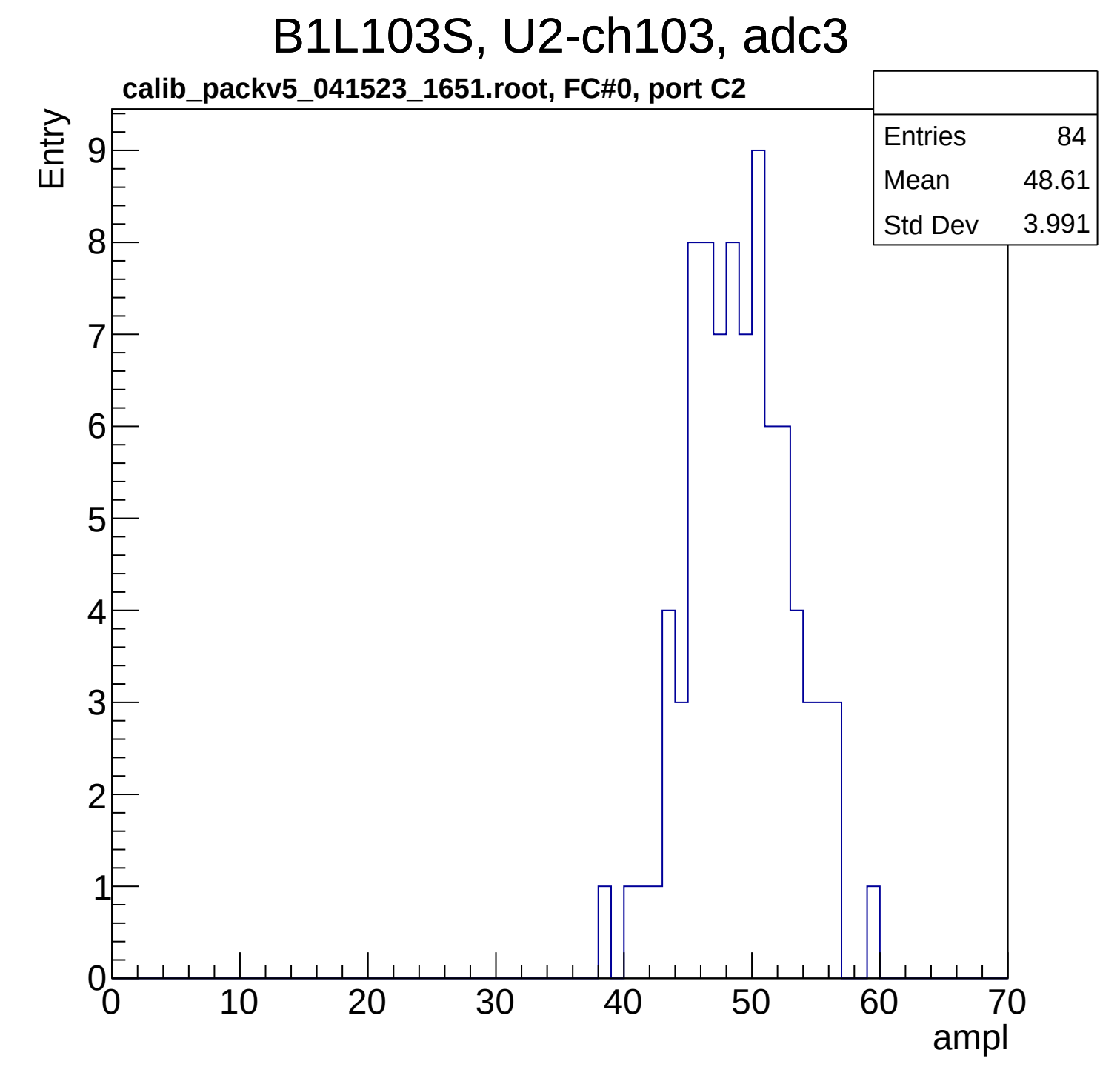

B1L103S, U2-ch102, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 58.49
Std Dev 10.01
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

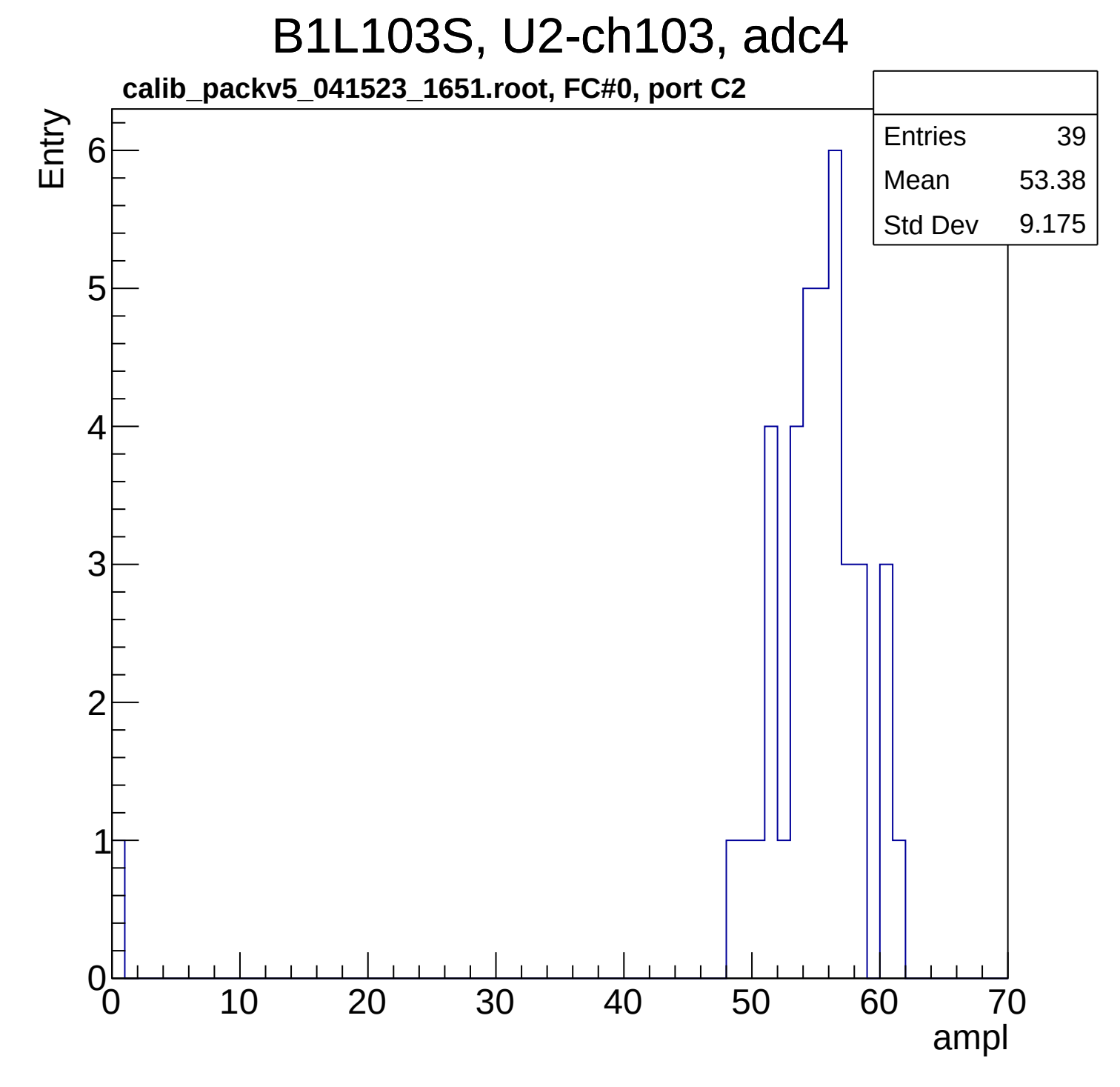

B1L103S, U2-ch102, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 18.48
Std Dev 28.49
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

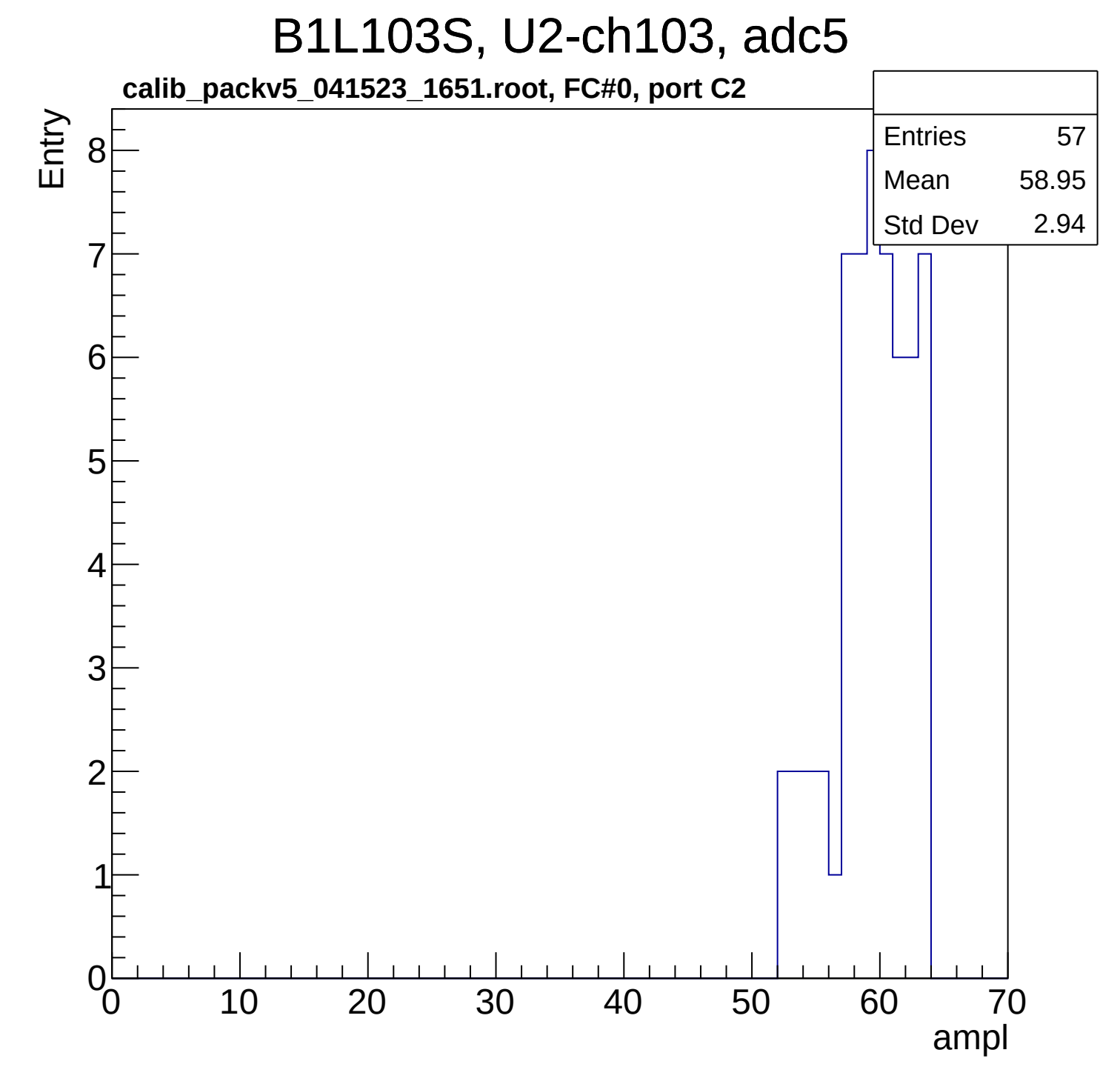

B1L103S, U2-ch103, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 22.18
Std Dev 12.49
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70

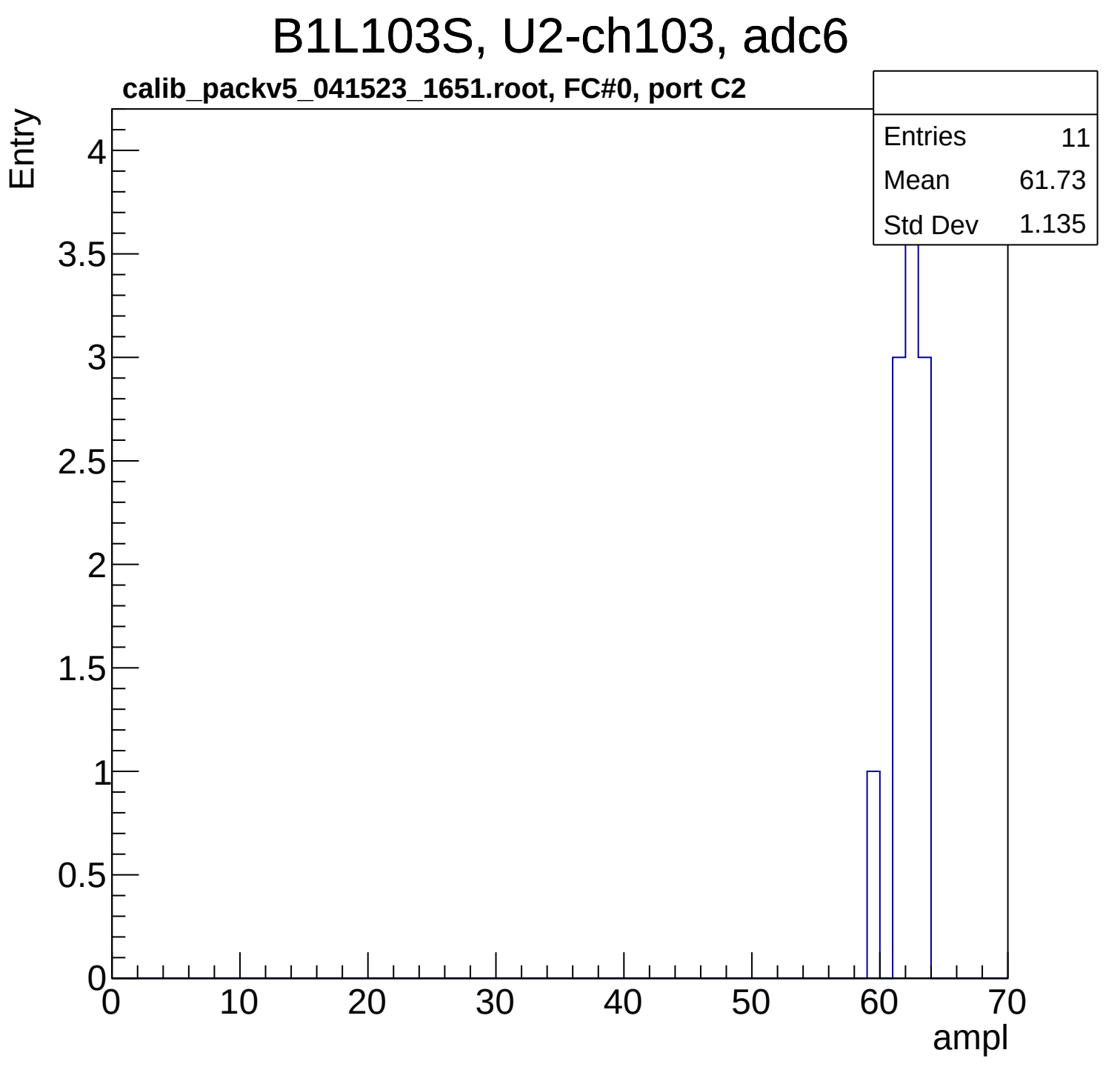

B1L103S, U2-ch103, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 29.99
Std Dev 13.5
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

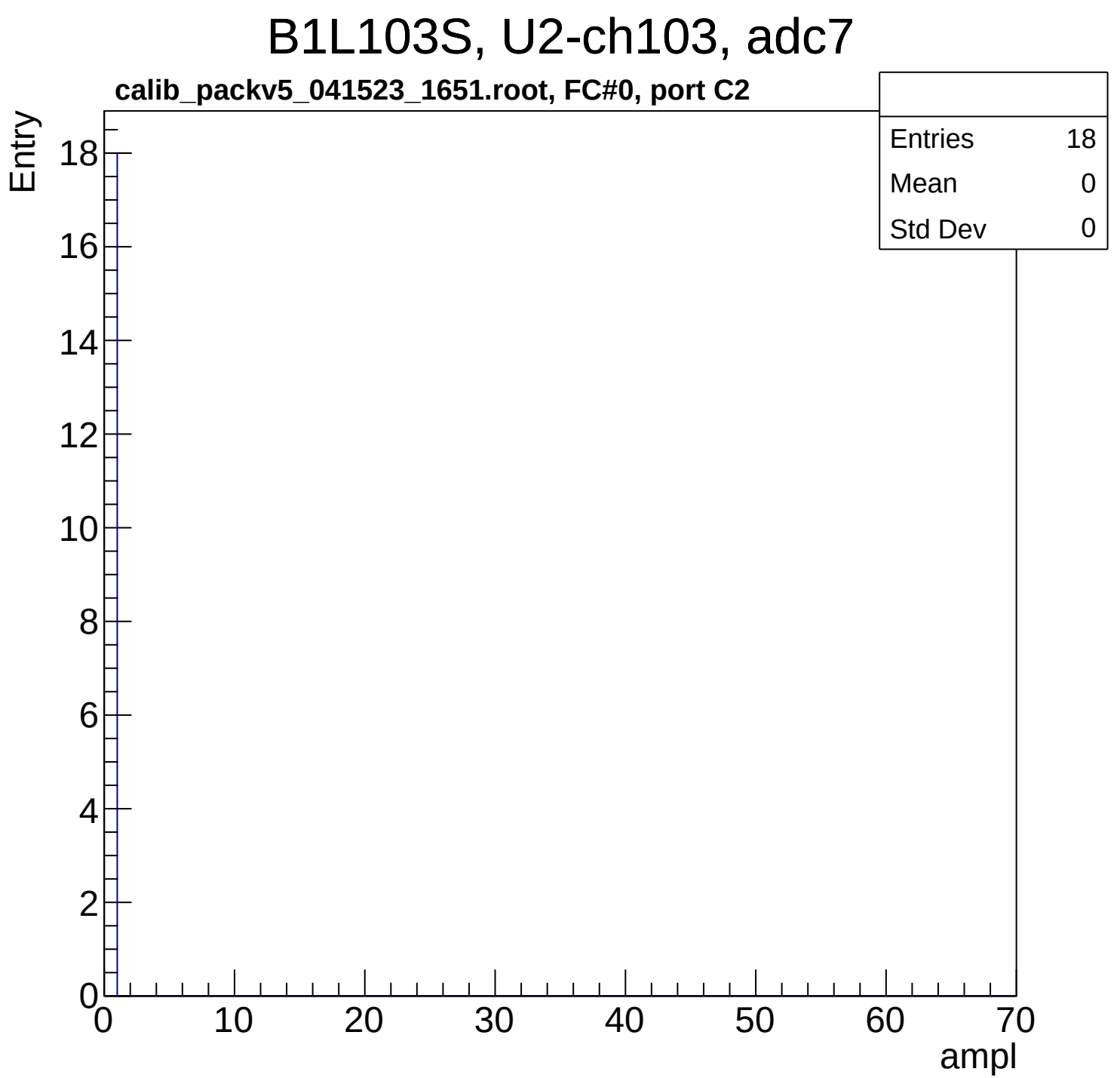

B1L103S, U2-ch103, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 38.38
Std Dev 11.73
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

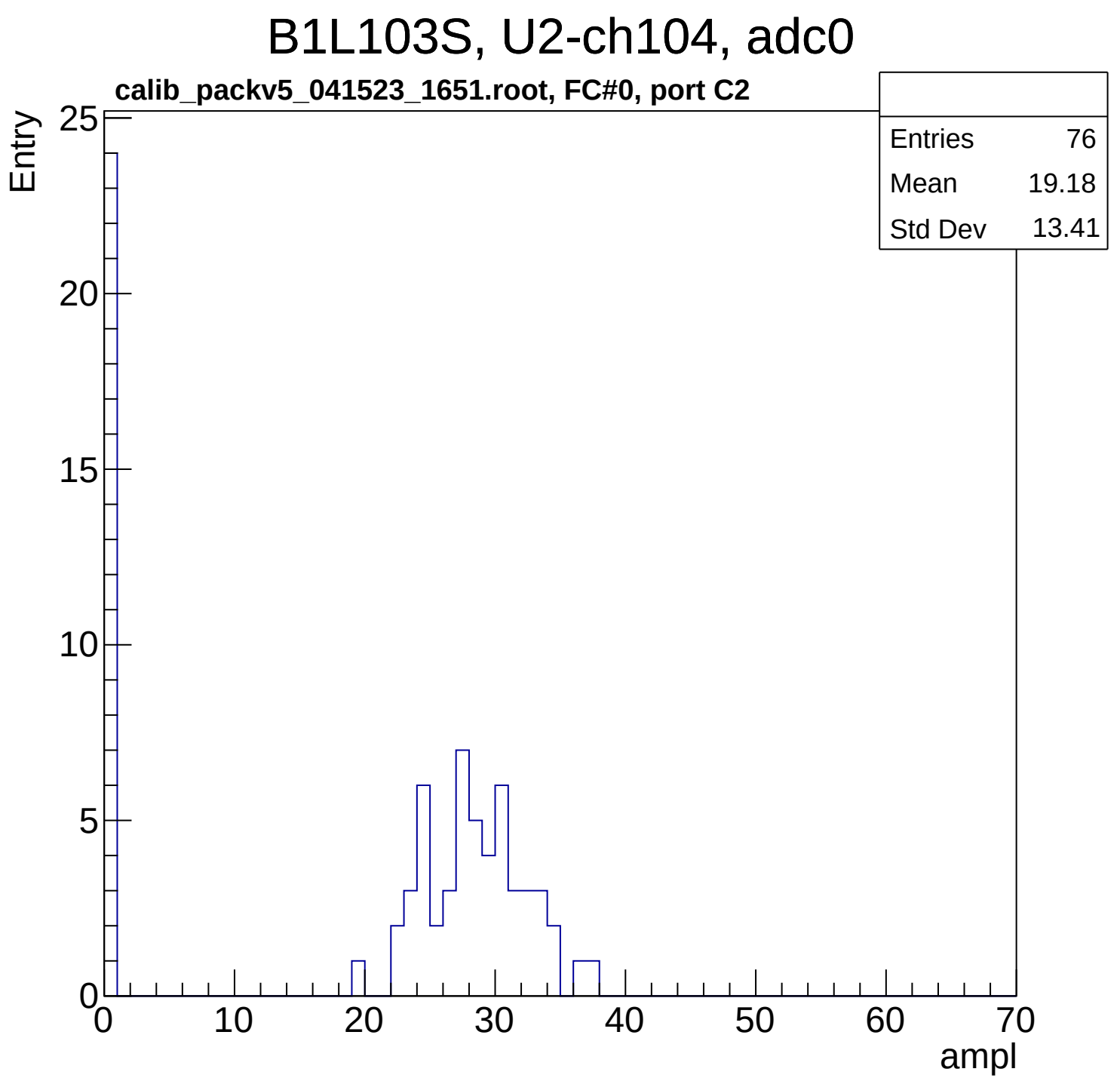

B1L103S, U2-ch103, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 48.61
Std Dev 3.991
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

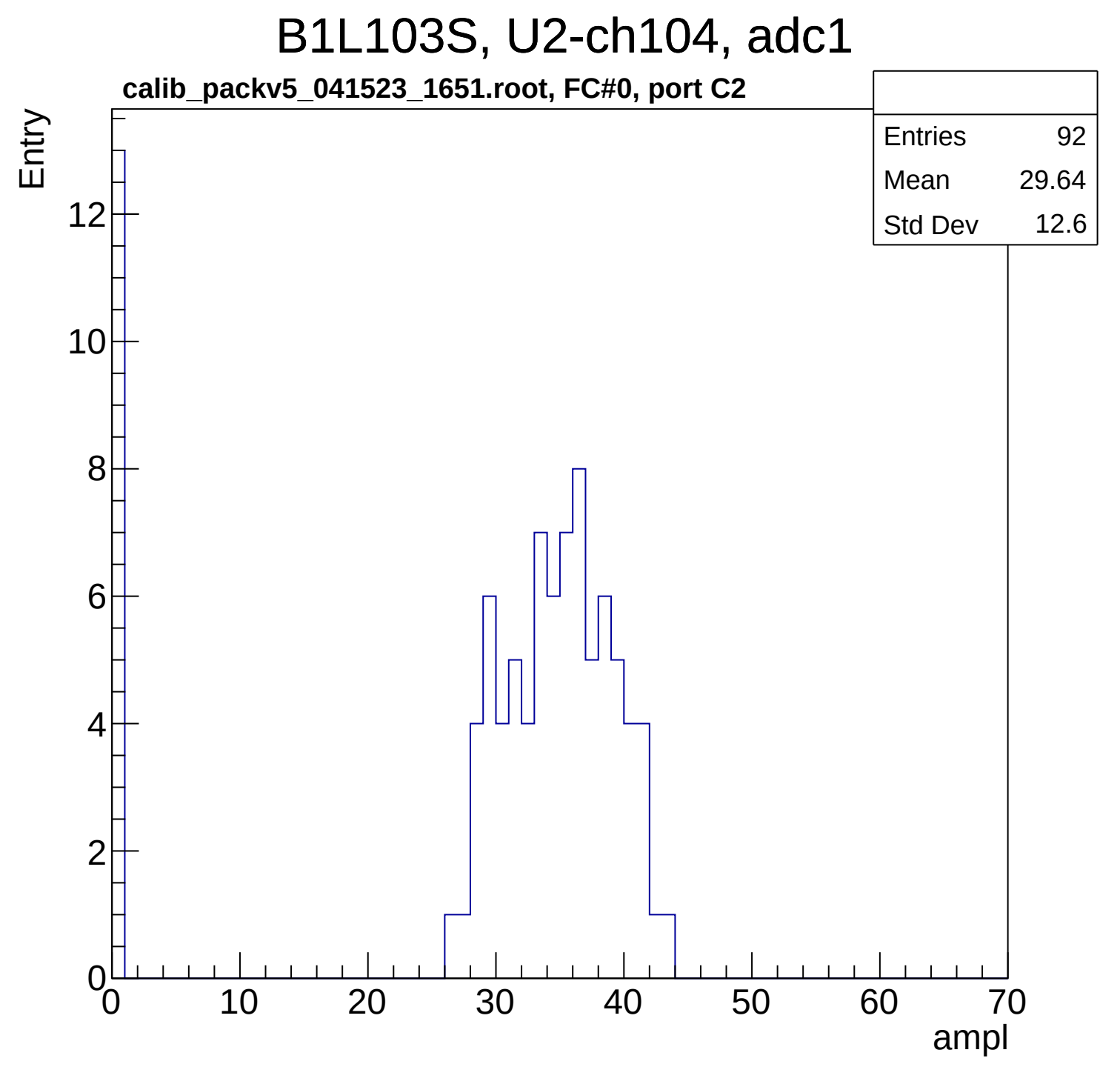

B1L103S, U2-ch103, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 53.38
Std Dev 9.175
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

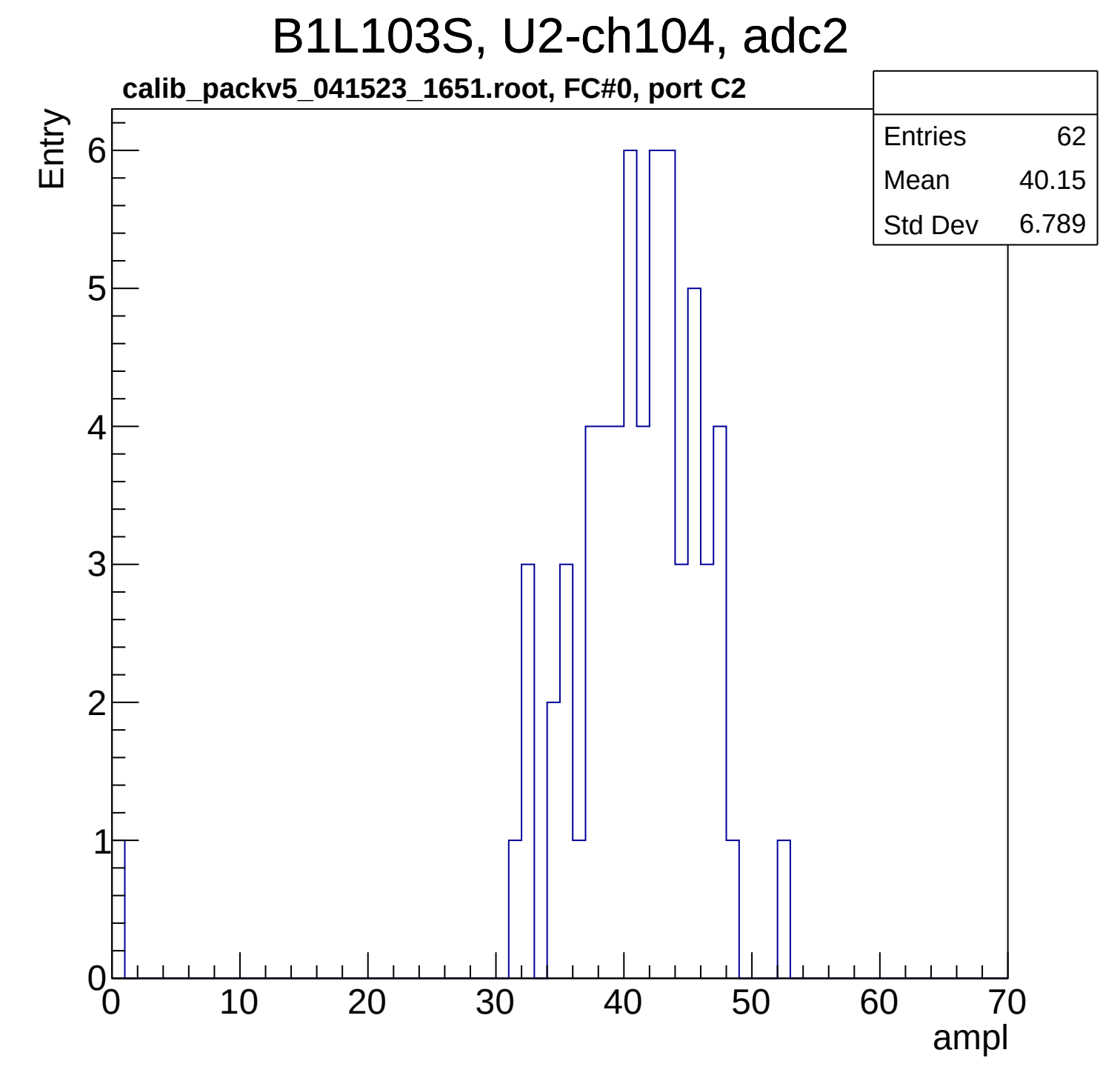

B1L103S, U2-ch103, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.95
Std Dev 2.94
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

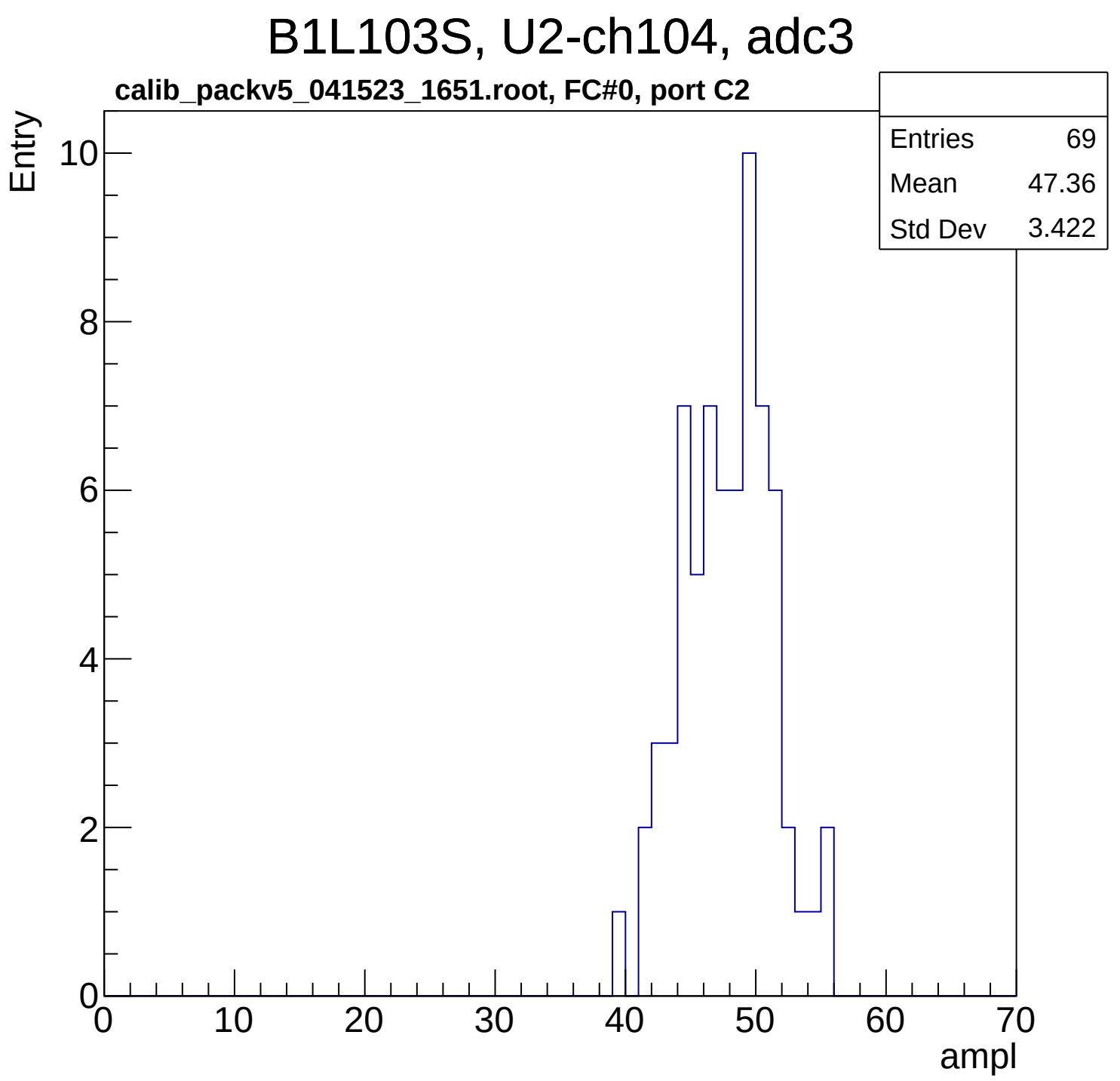

B1L103S, U2-ch103, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 61.73
Std Dev 1.135
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

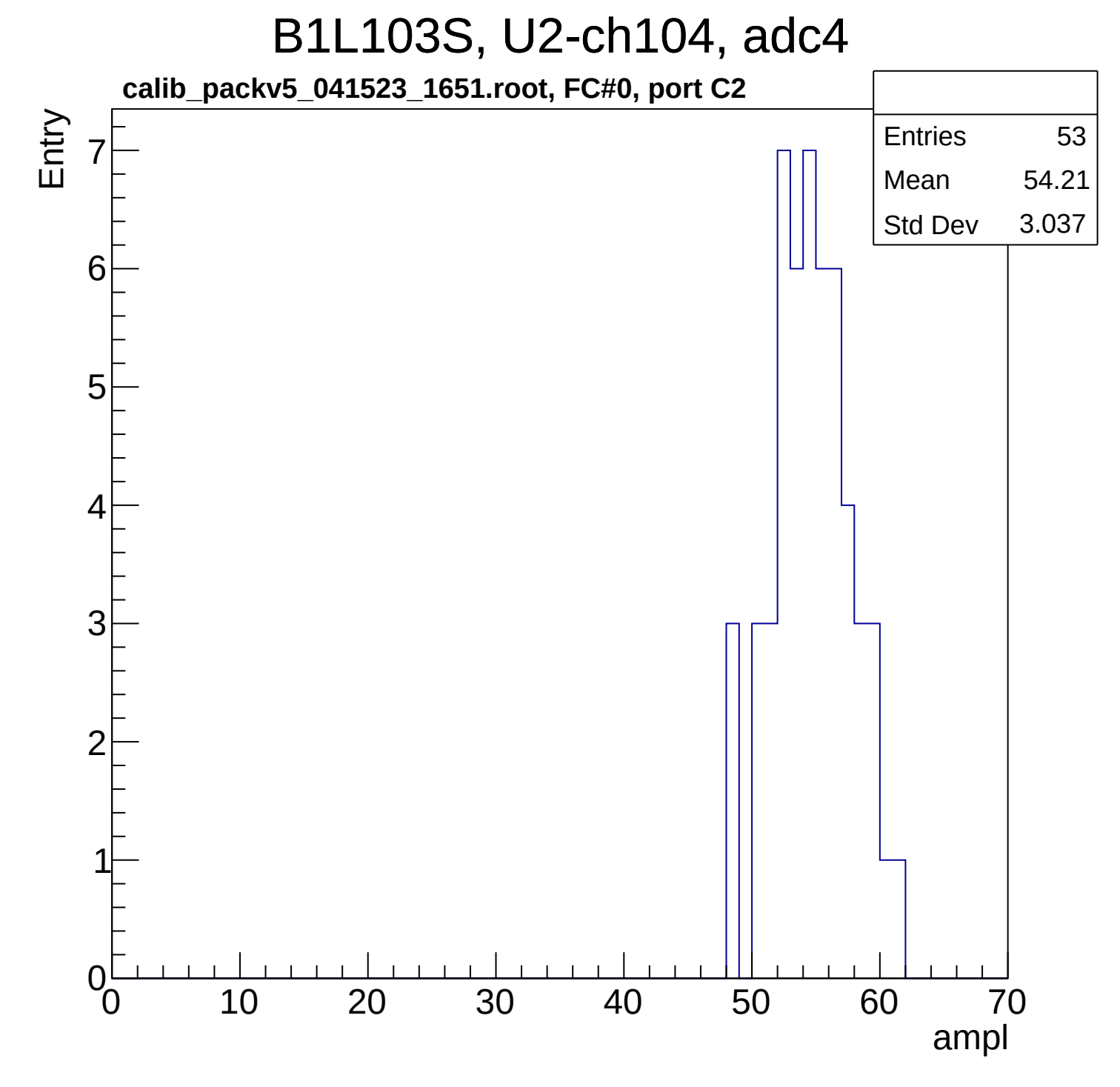

B1L103S, U2-ch103, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

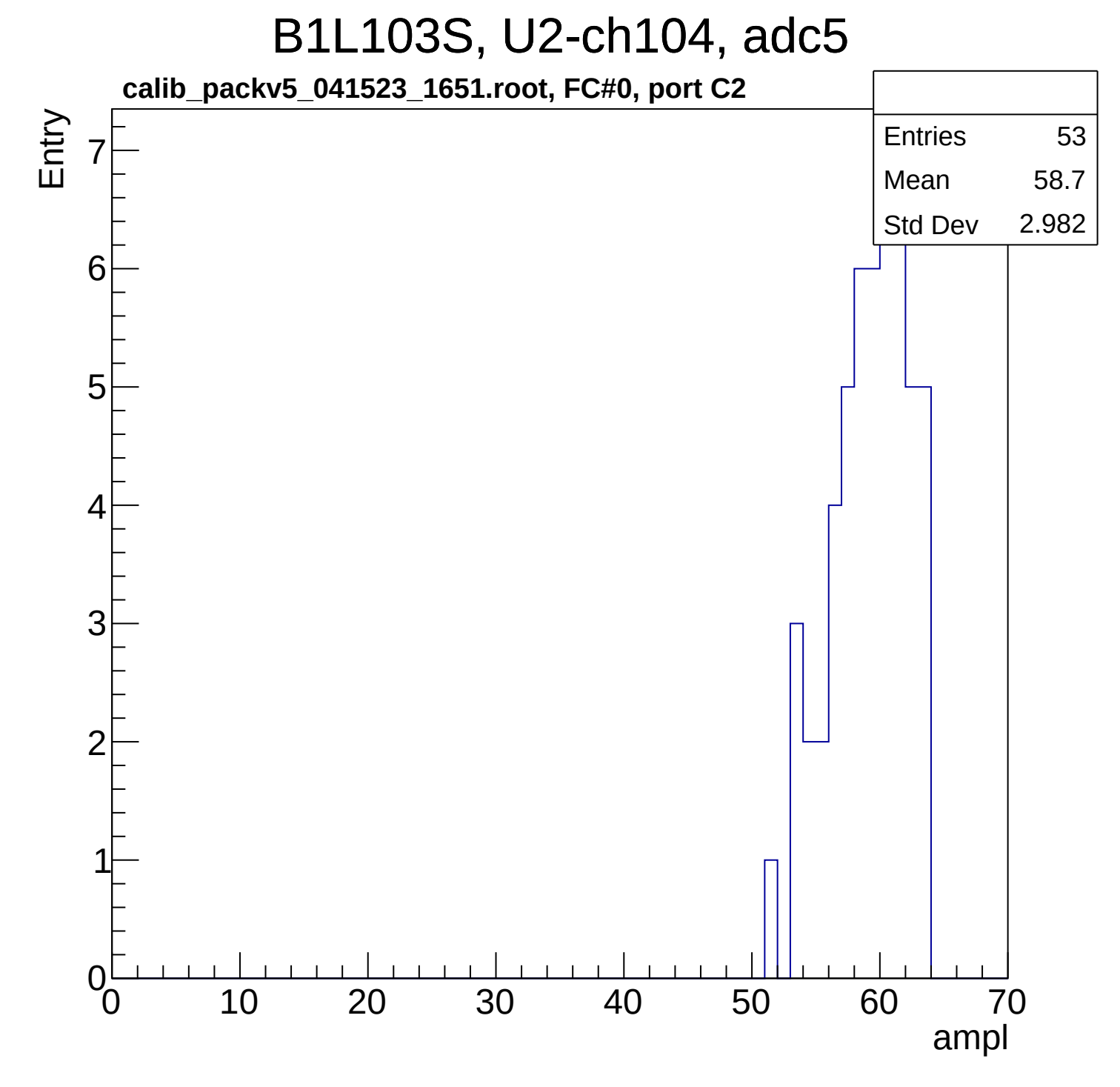

B1L103S, U2-ch104, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 19.18
Std Dev 13.41
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70

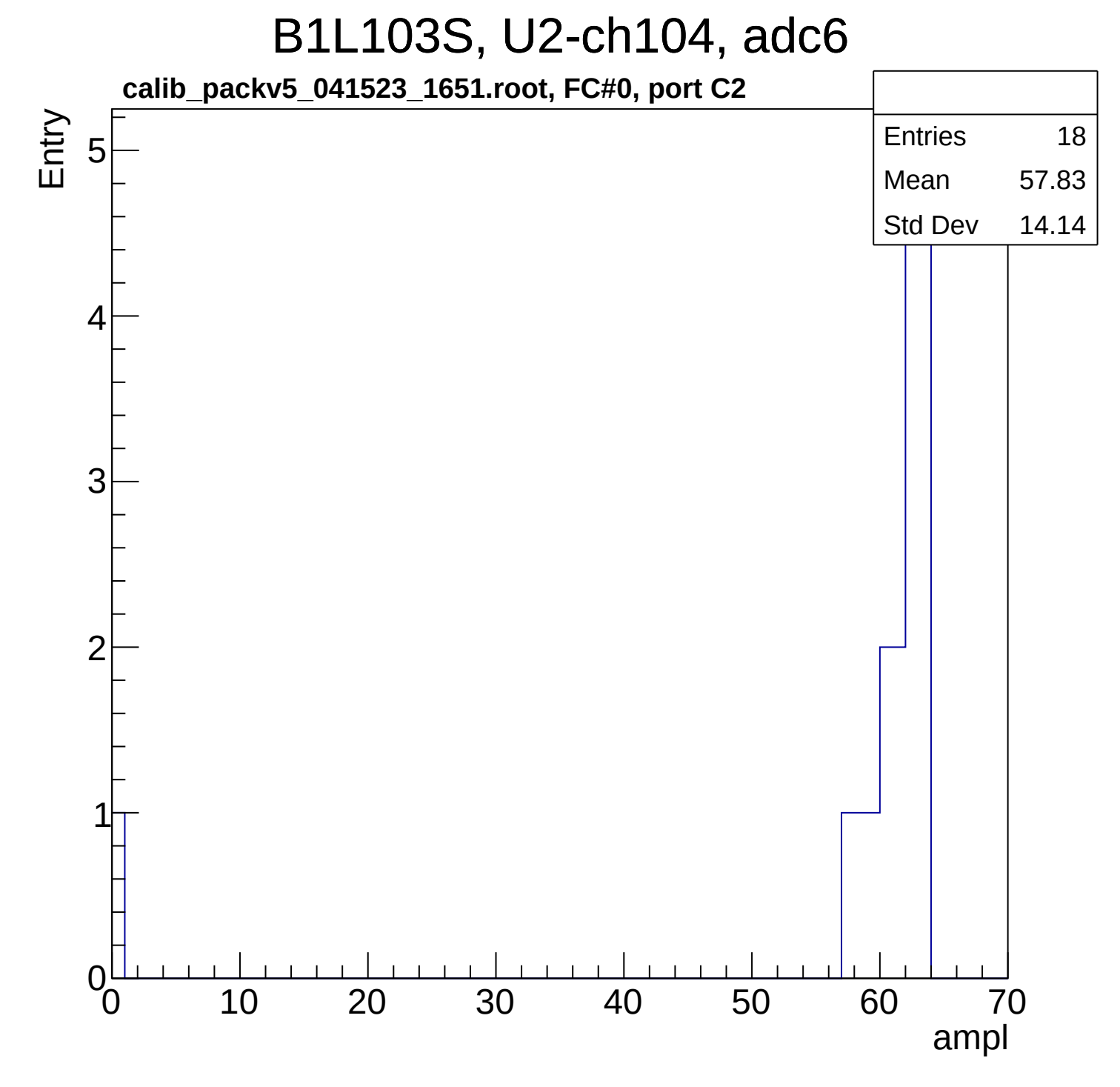

B1L103S, U2-ch104, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 29.64
Std Dev 12.6
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

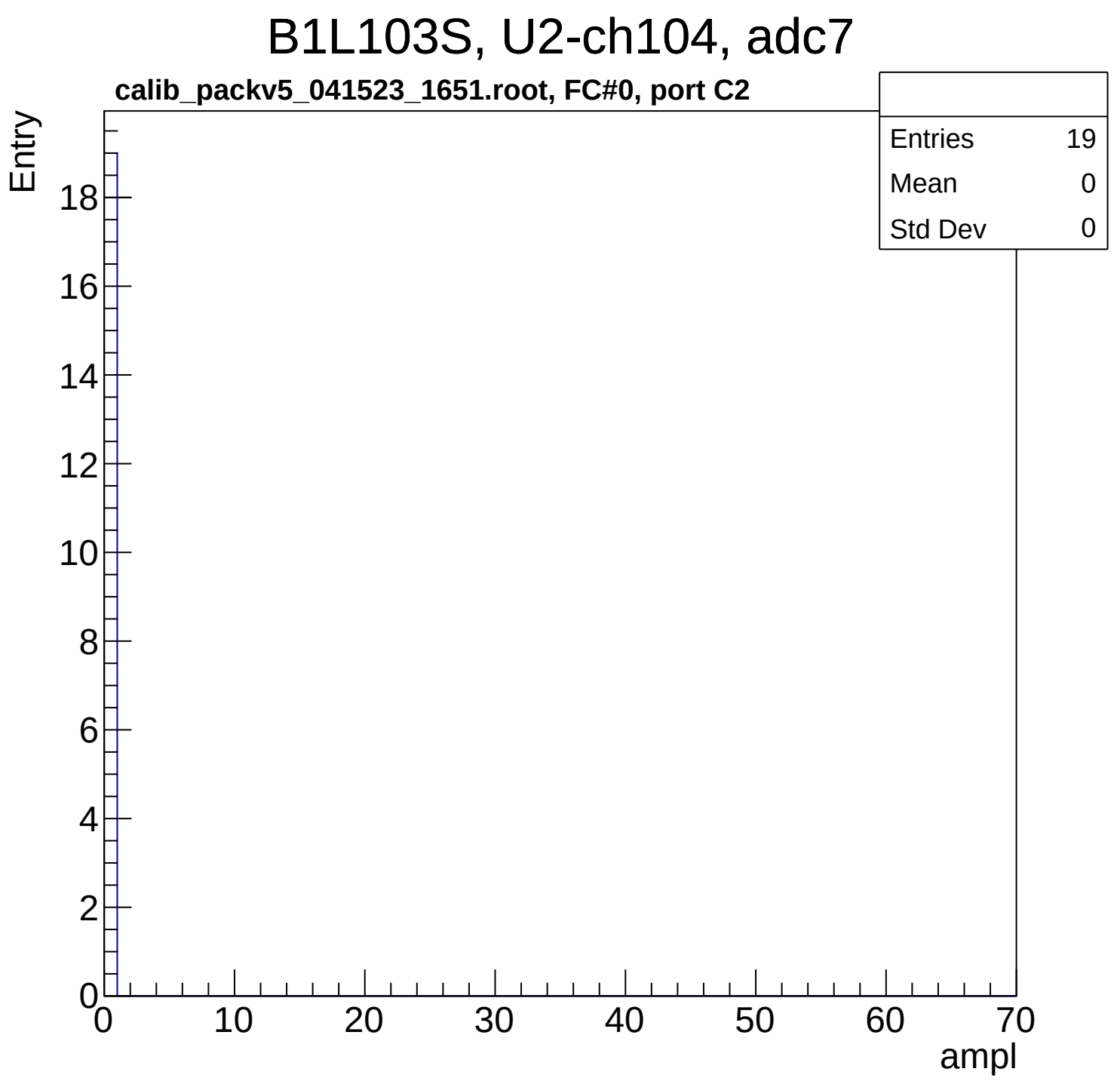

B1L103S, U2-ch104, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 40.15
Std Dev 6.789
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

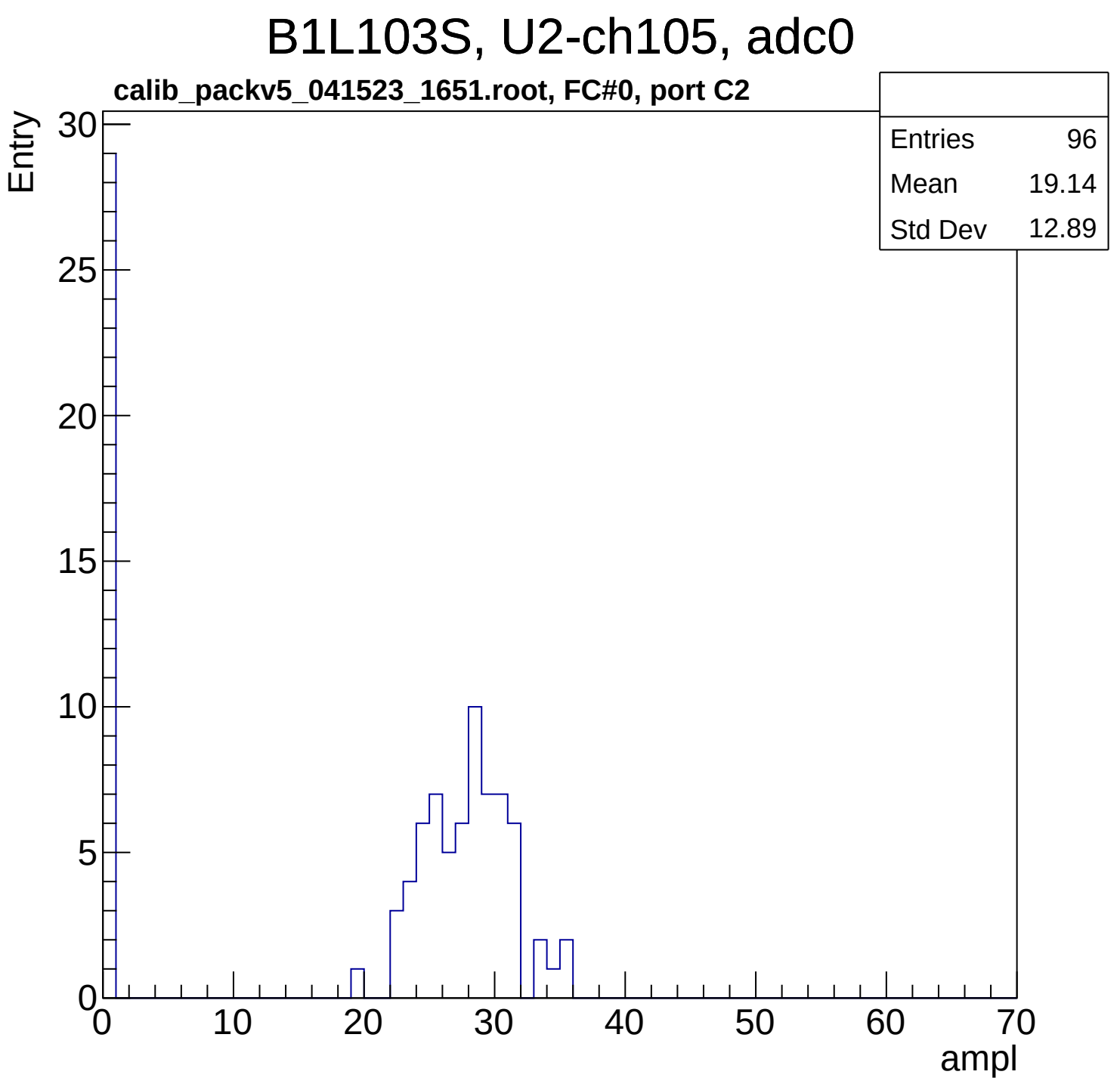

B1L103S, U2-ch104, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 47.36
Std Dev 3.422
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

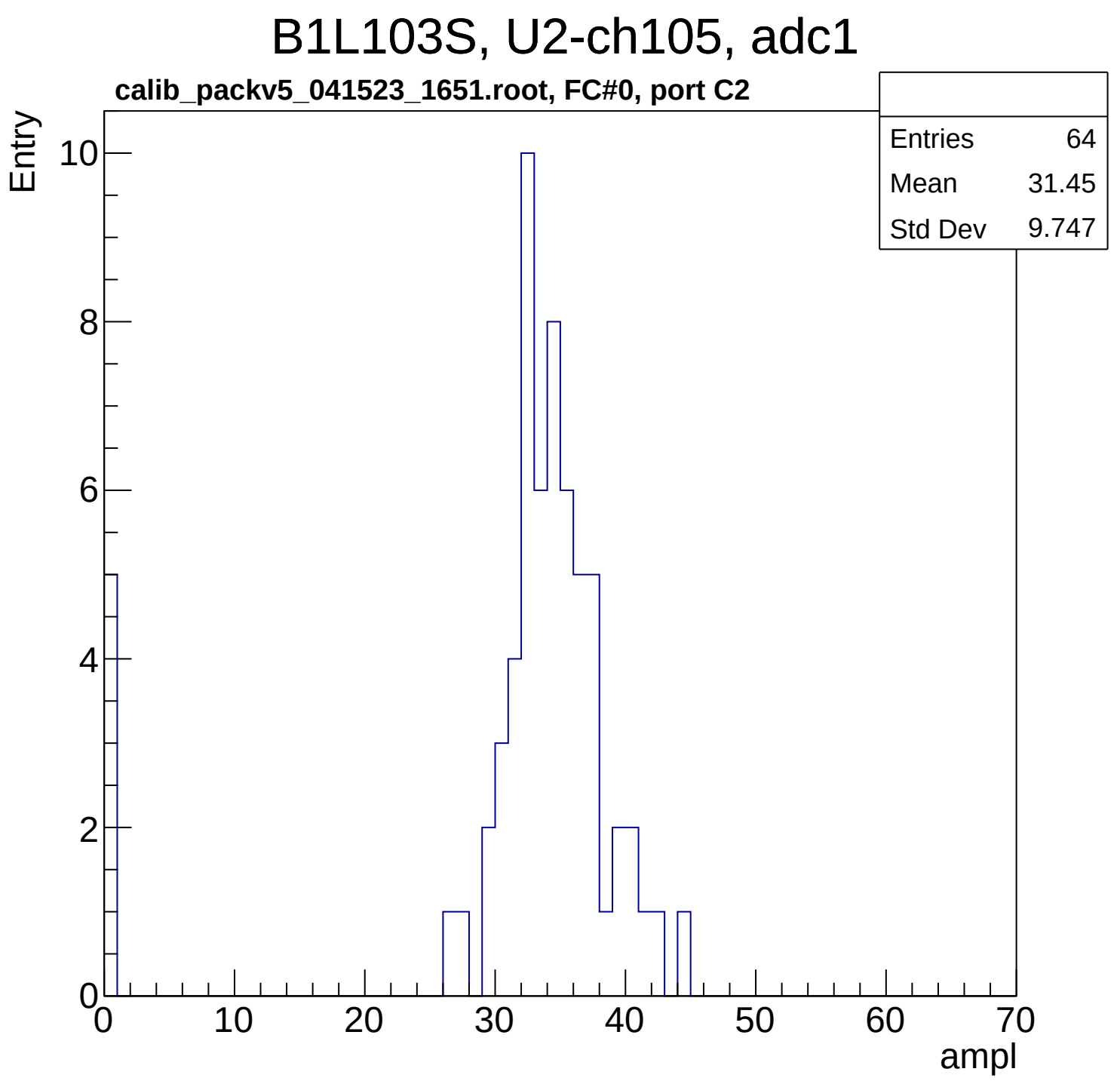

B1L103S, U2-ch104, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 54.21
Std Dev 3.037
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

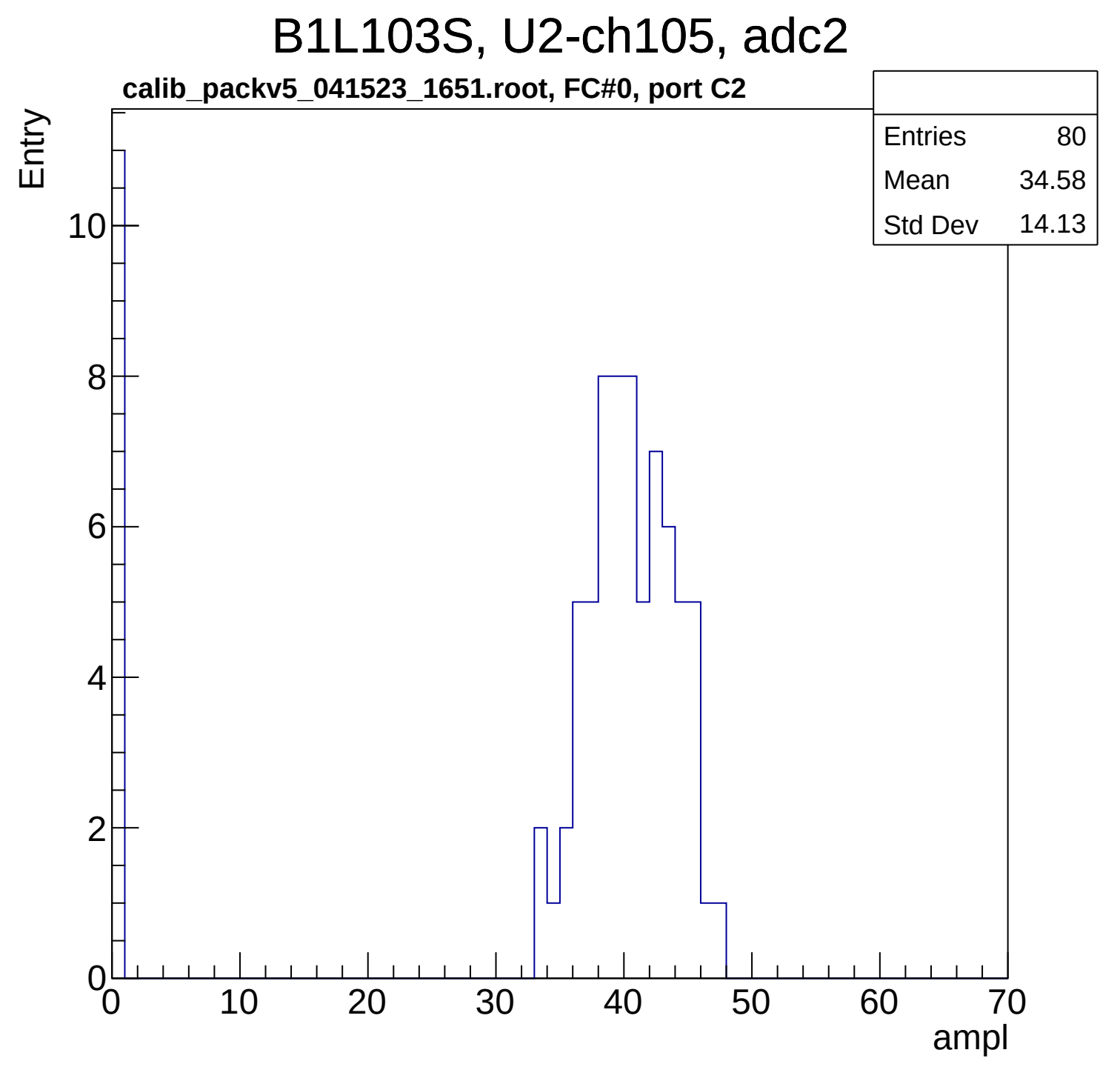

B1L103S, U2-ch104, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 58.7
Std Dev 2.982
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

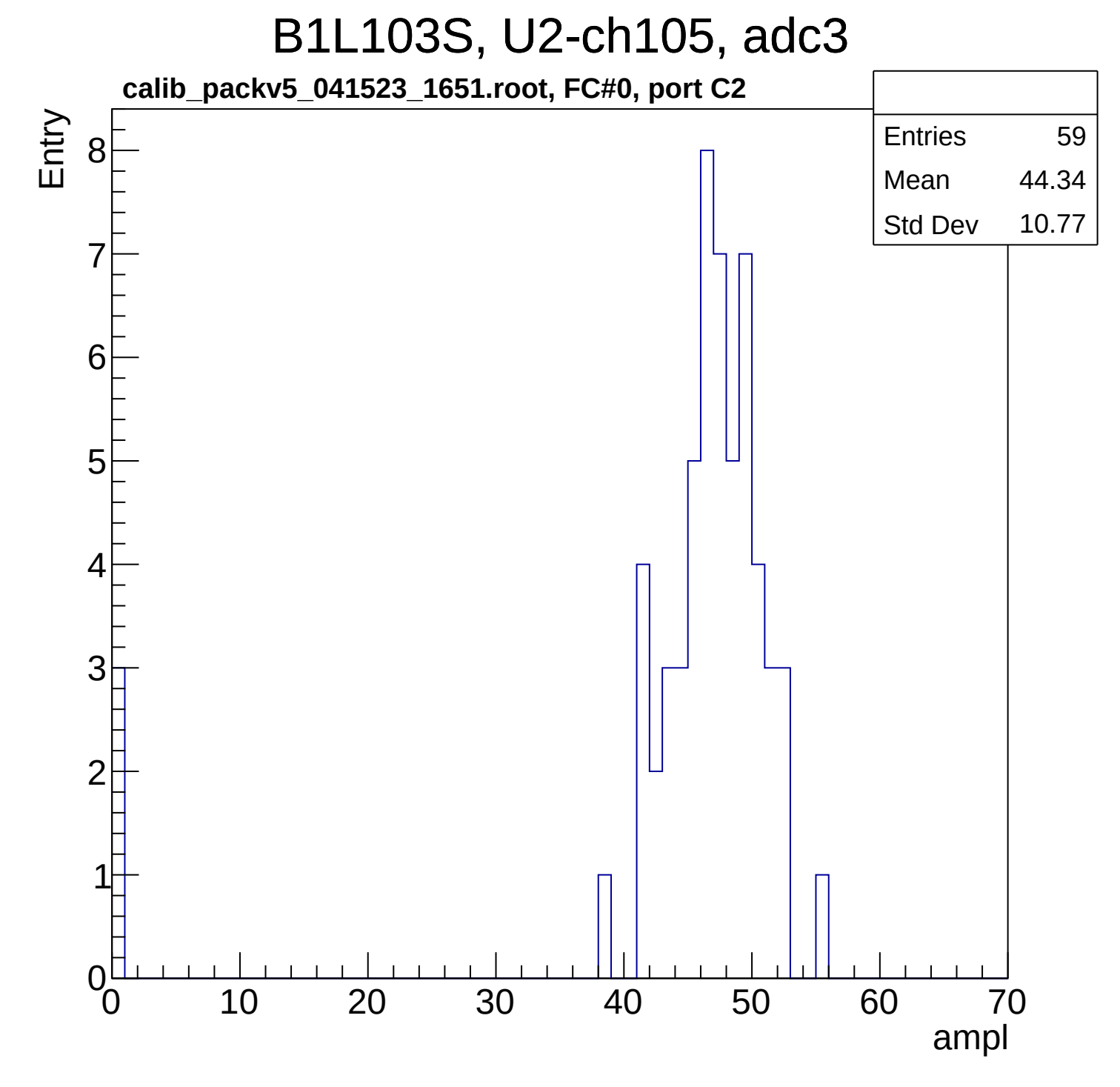

B1L103S, U2-ch104, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 57.83
Std Dev 14.14
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

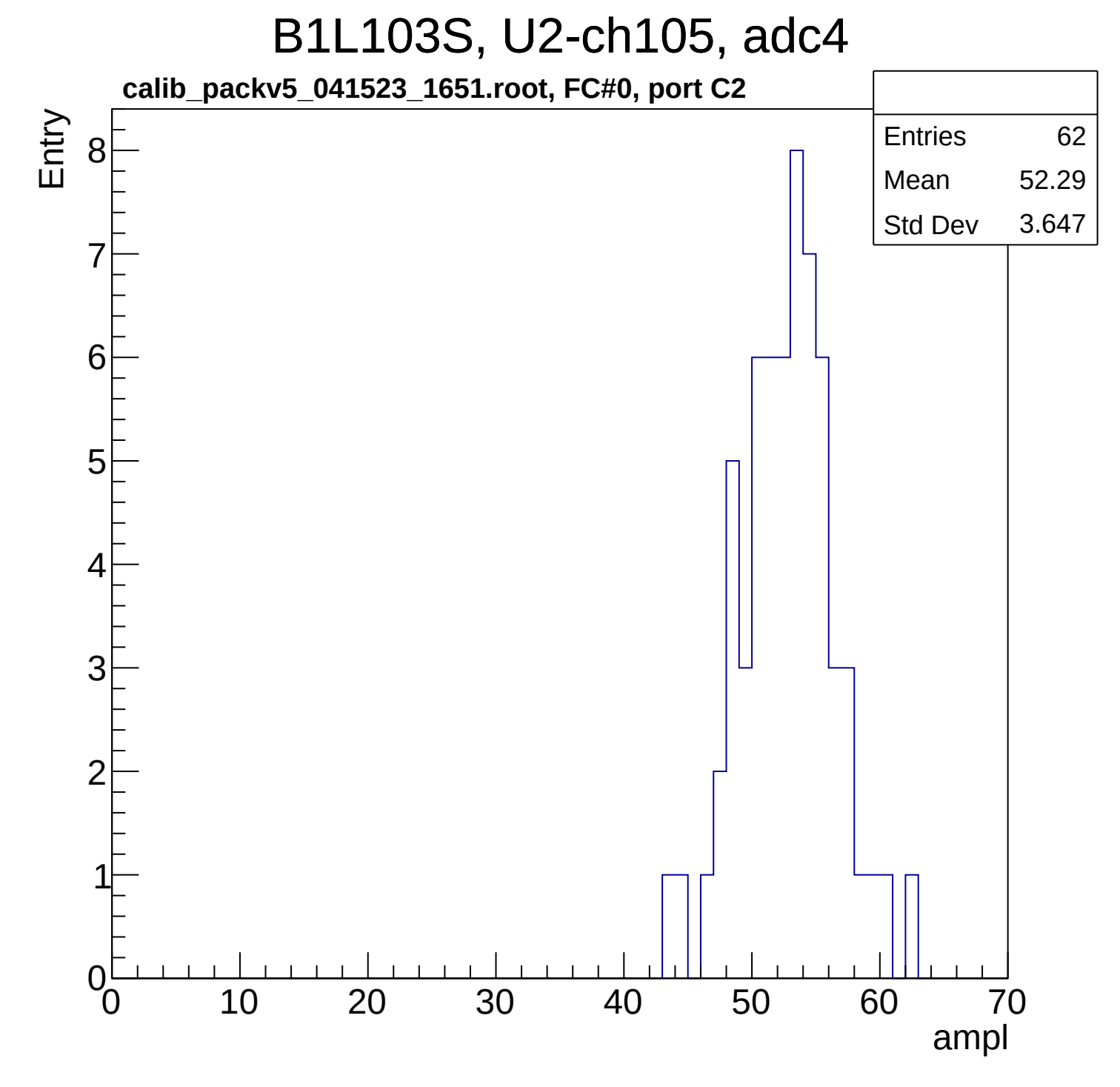

B1L103S, U2-ch104, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

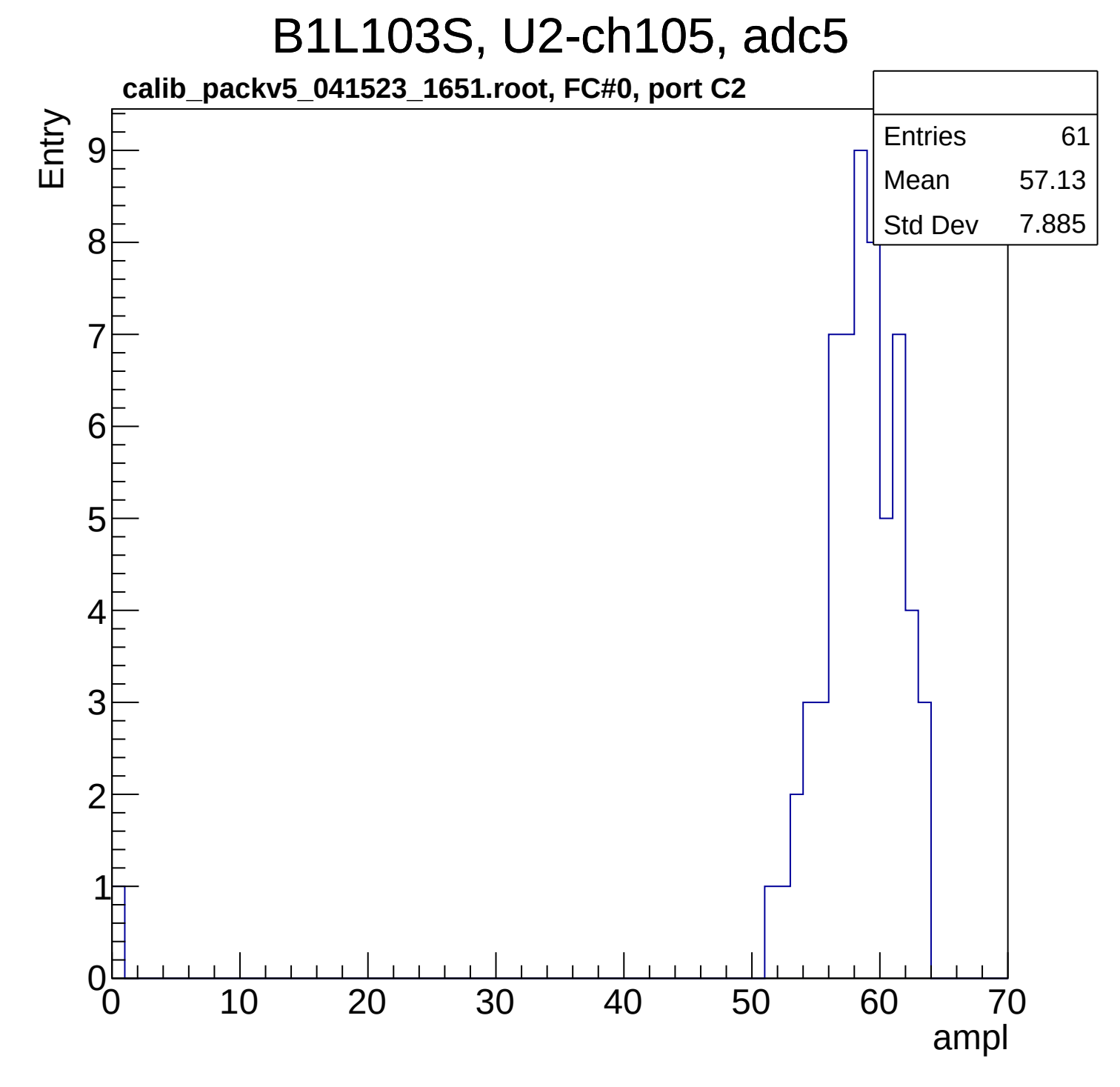

B1L103S, U2-ch105, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 19.14
Std Dev 12.89
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70

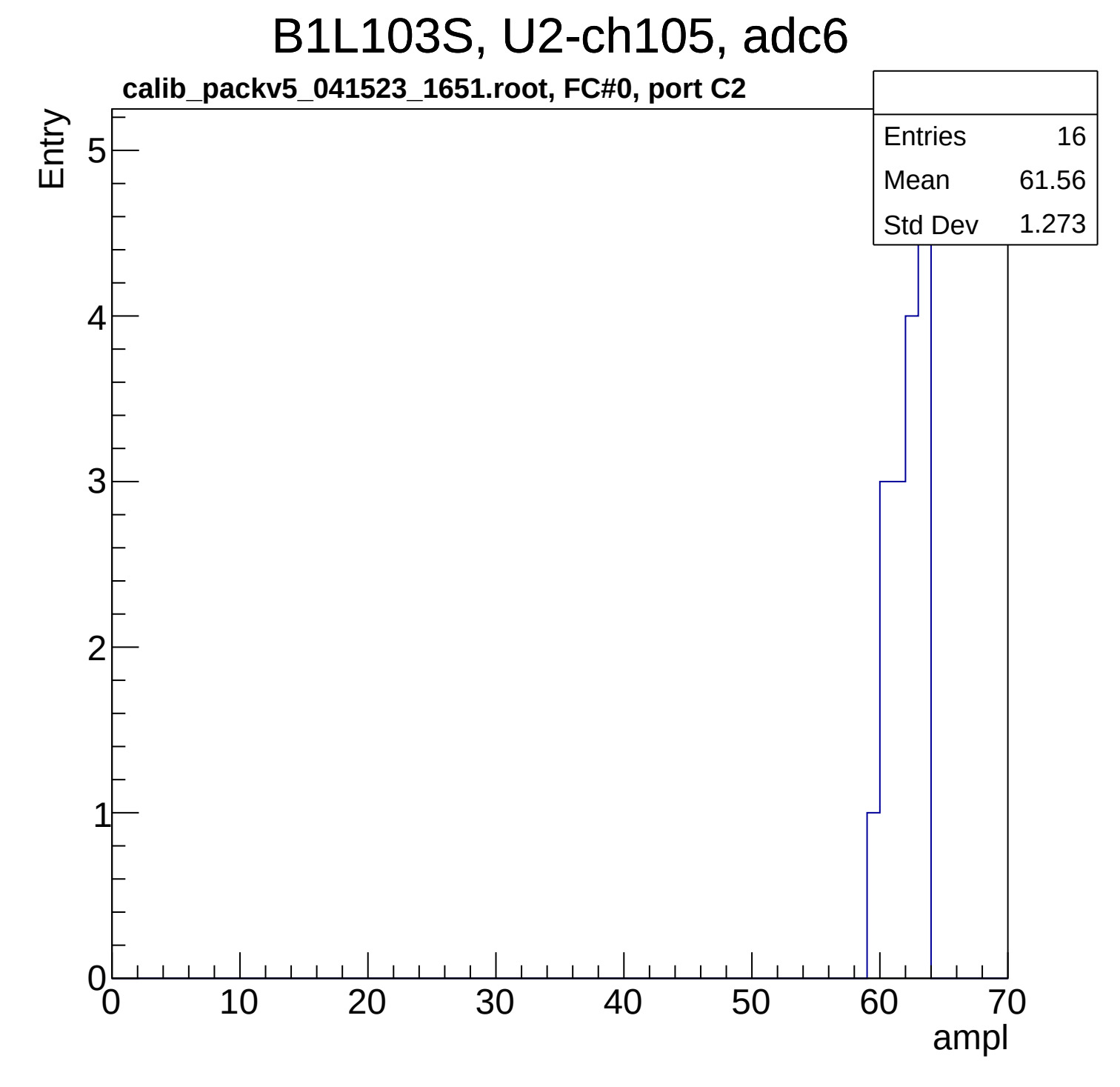

B1L103S, U2-ch105, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 31.45
Std Dev 9.747
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

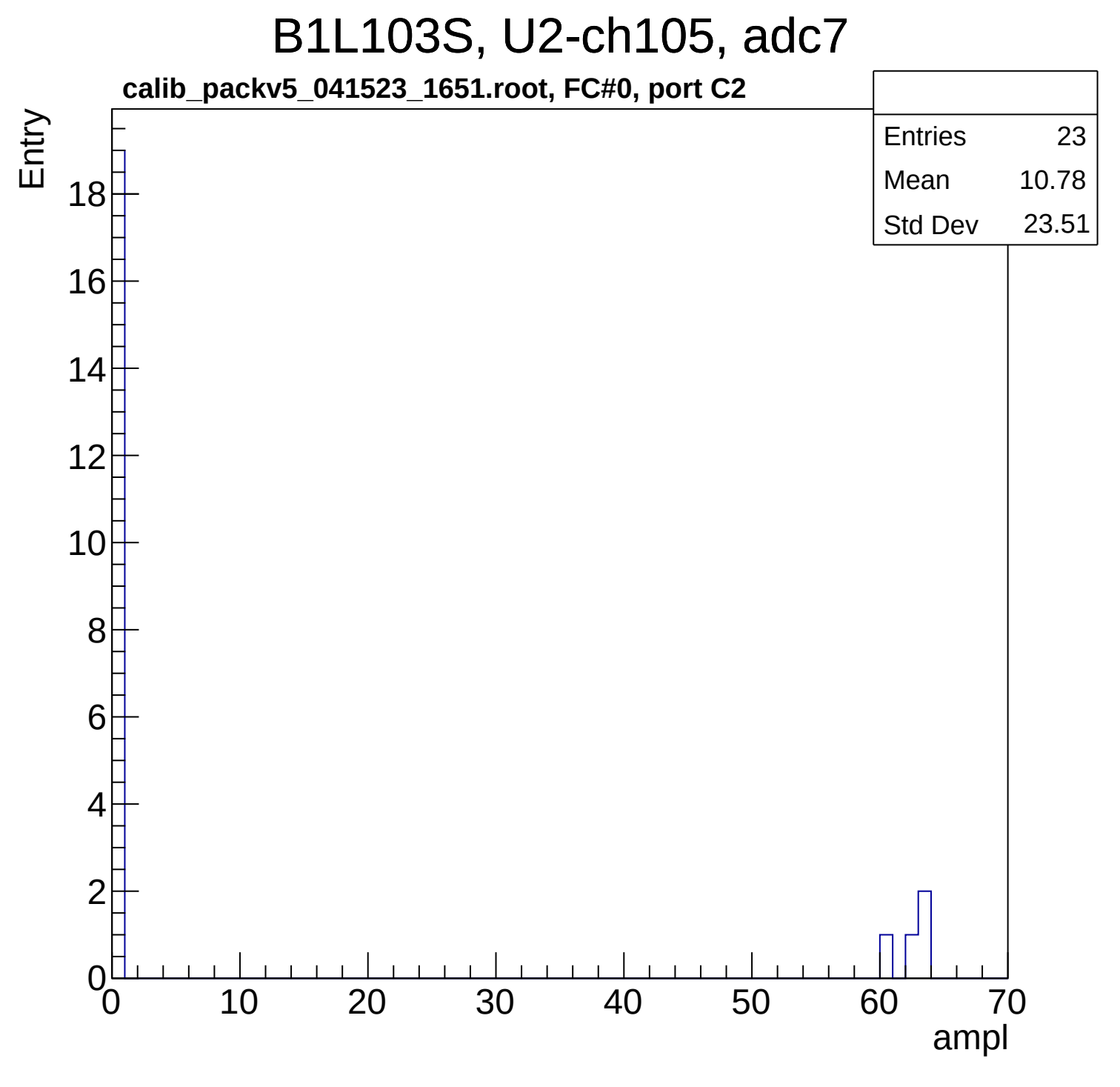

B1L103S, U2-ch105, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 34.58
Std Dev 14.13
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

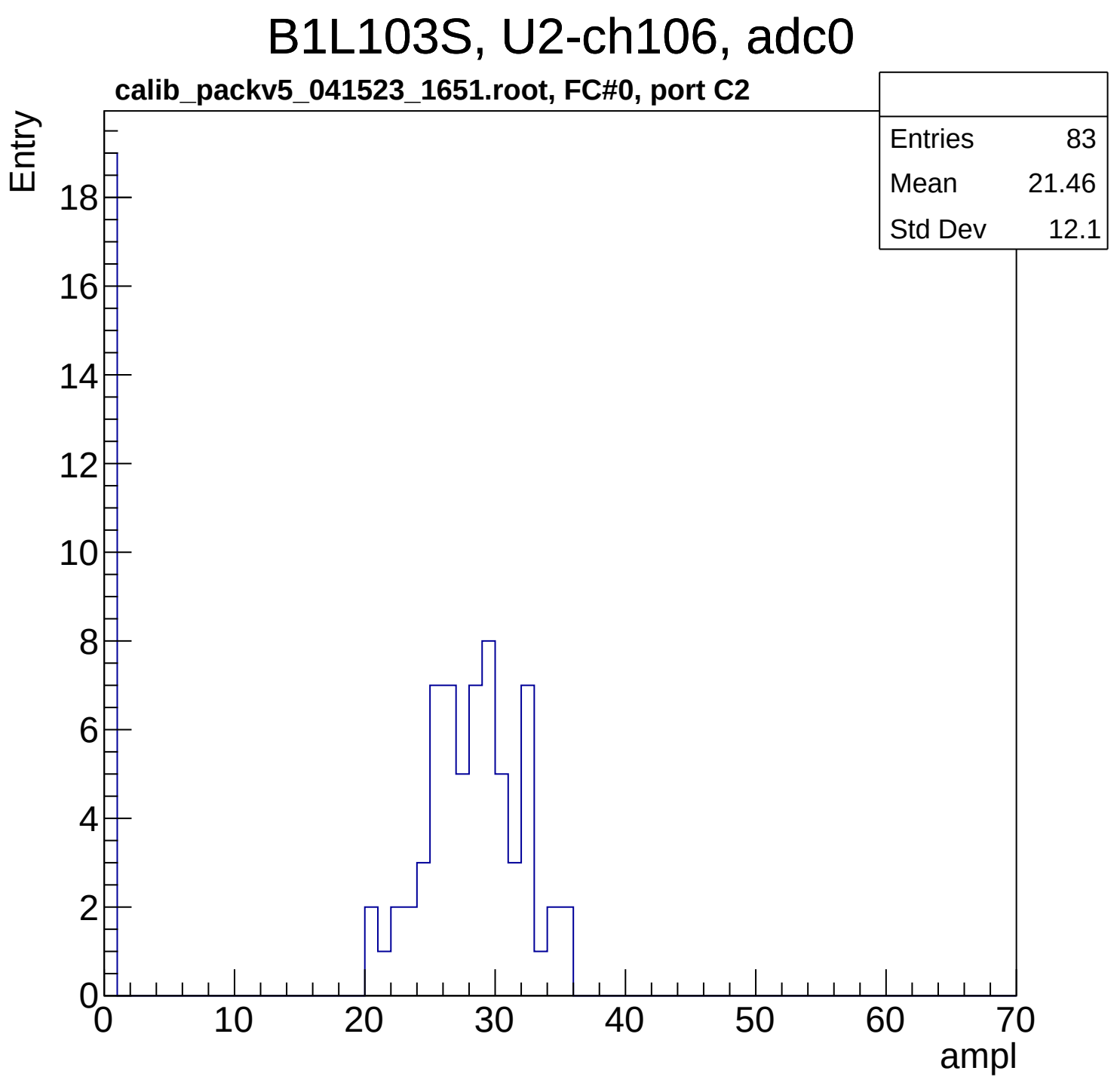

B1L103S, U2-ch105, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 44.34
Std Dev 10.77
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

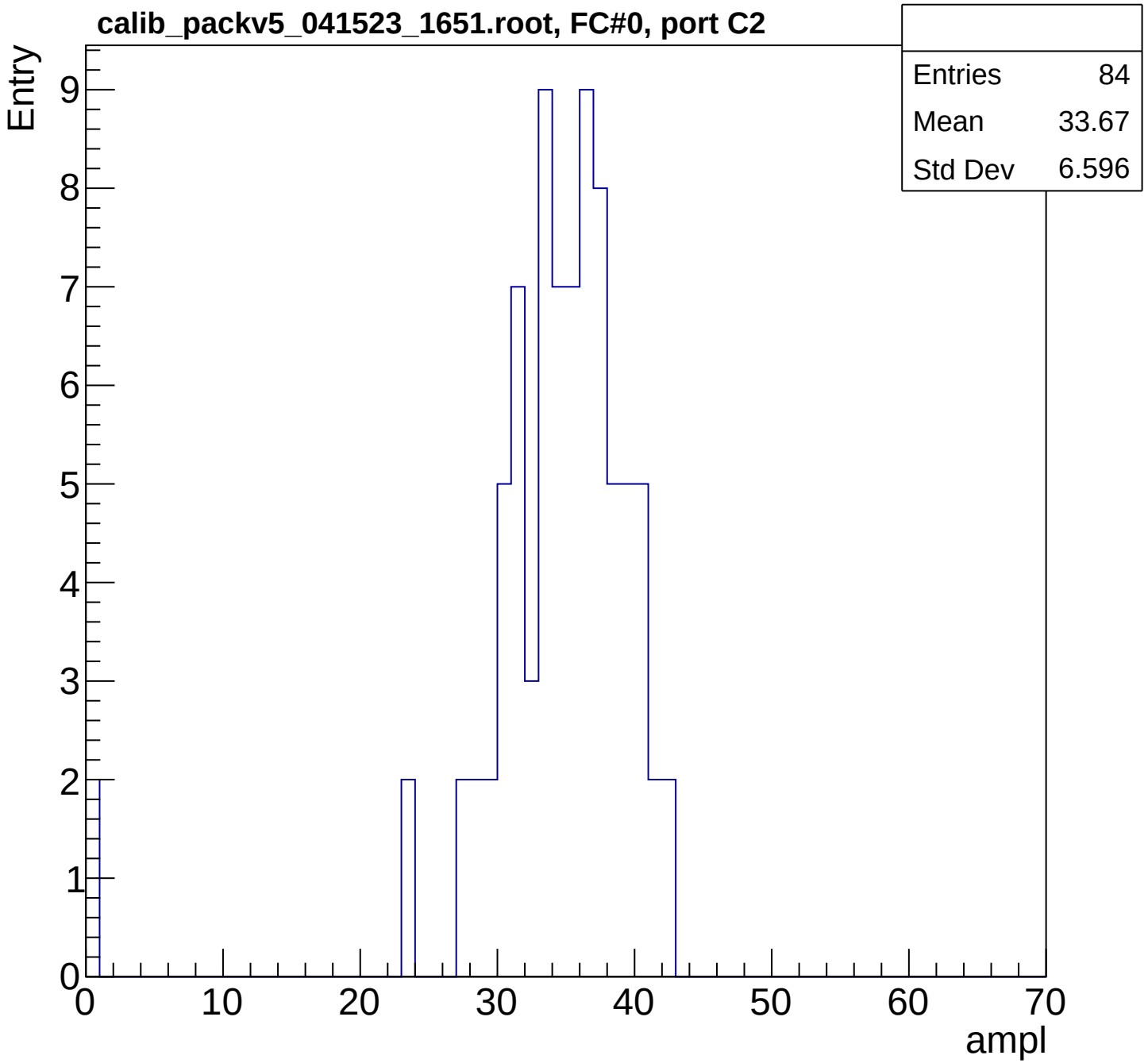

B1L103S, U2-ch105, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 52.29
Std Dev 3.647
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

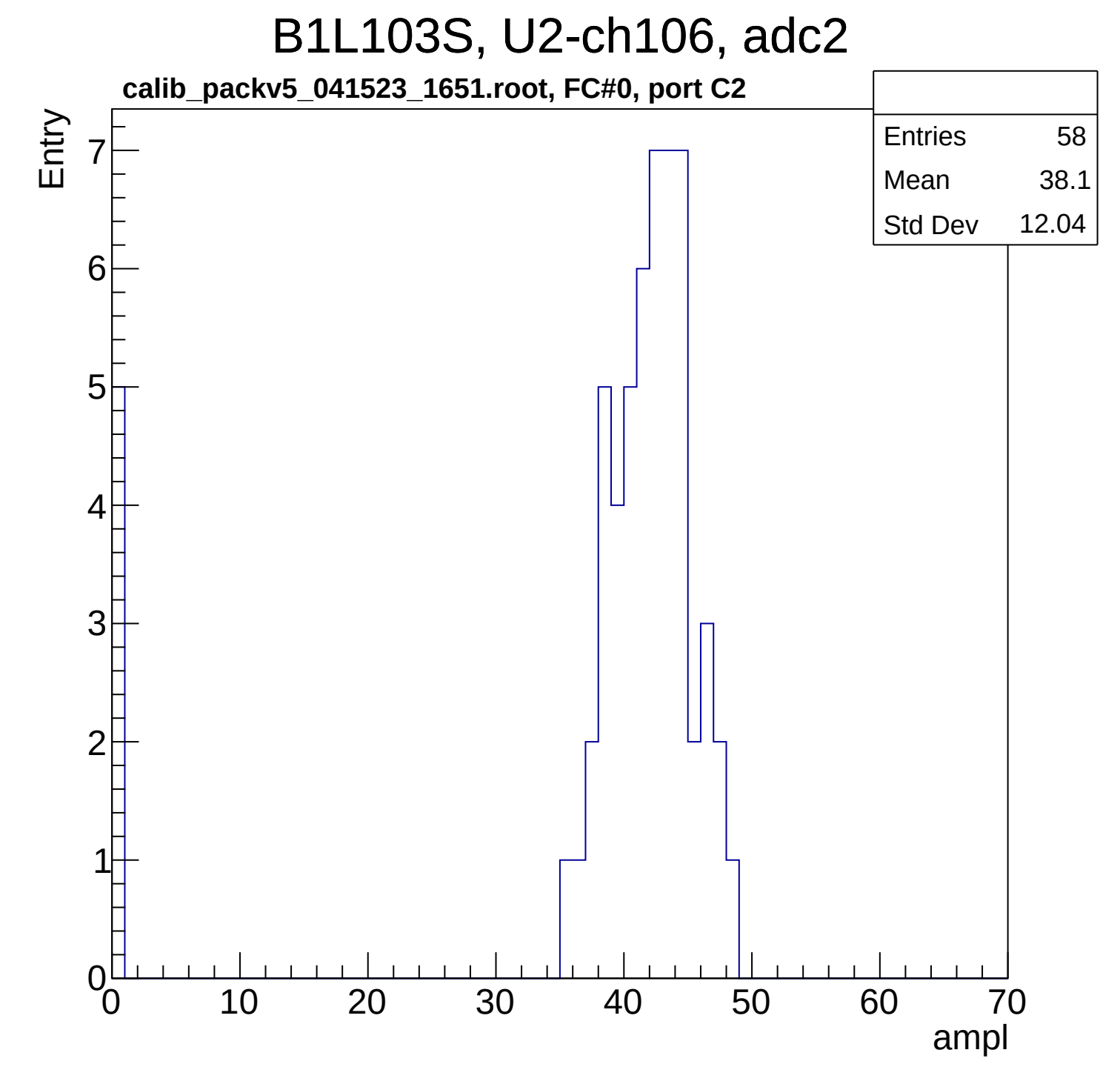

B1L103S, U2-ch105, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 57.13
Std Dev 7.885
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

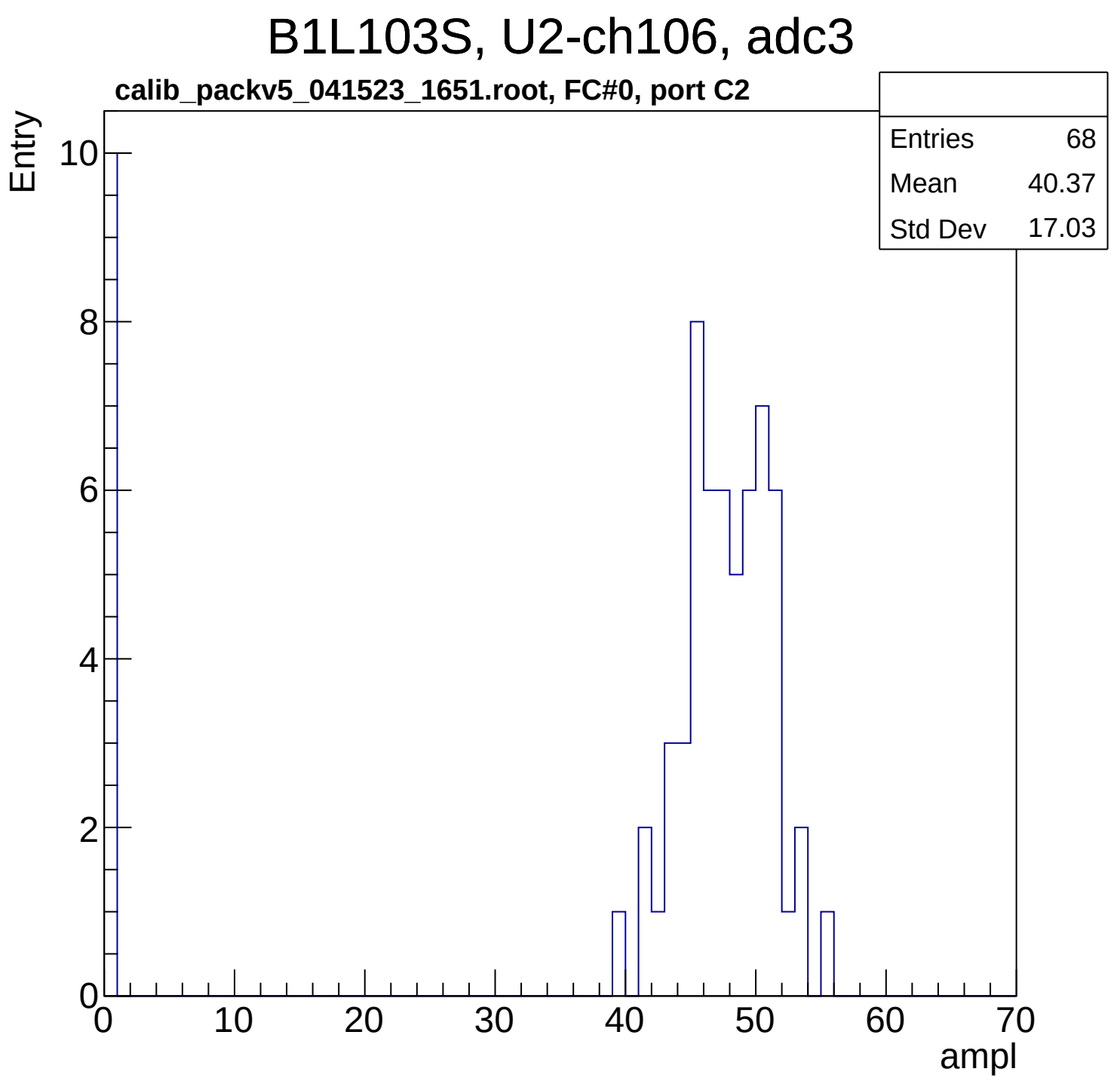

B1L103S, U2-ch105, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 61.56
Std Dev 1.273
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

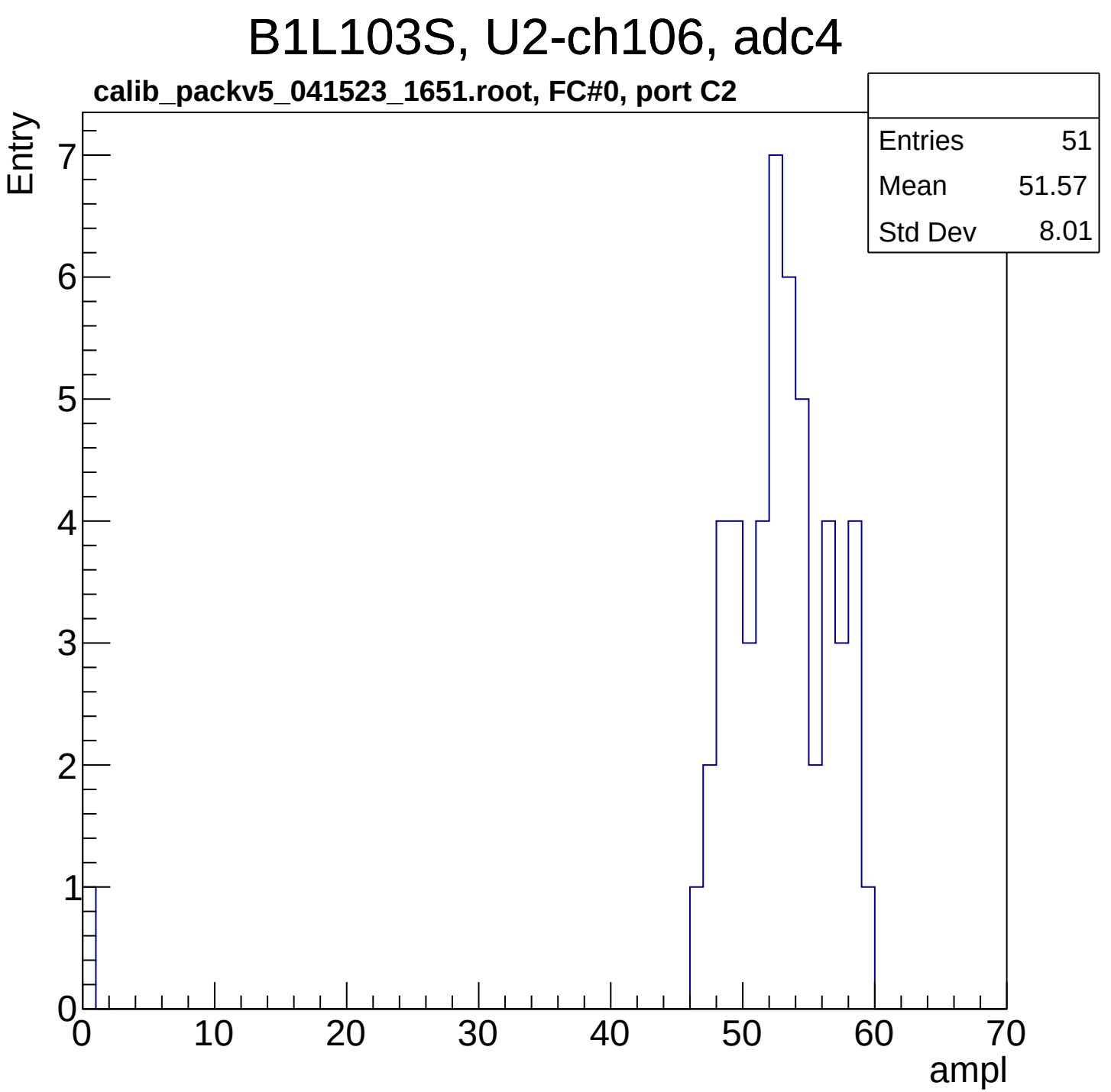

B1L103S, U2-ch105, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.78
Std Dev 23.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

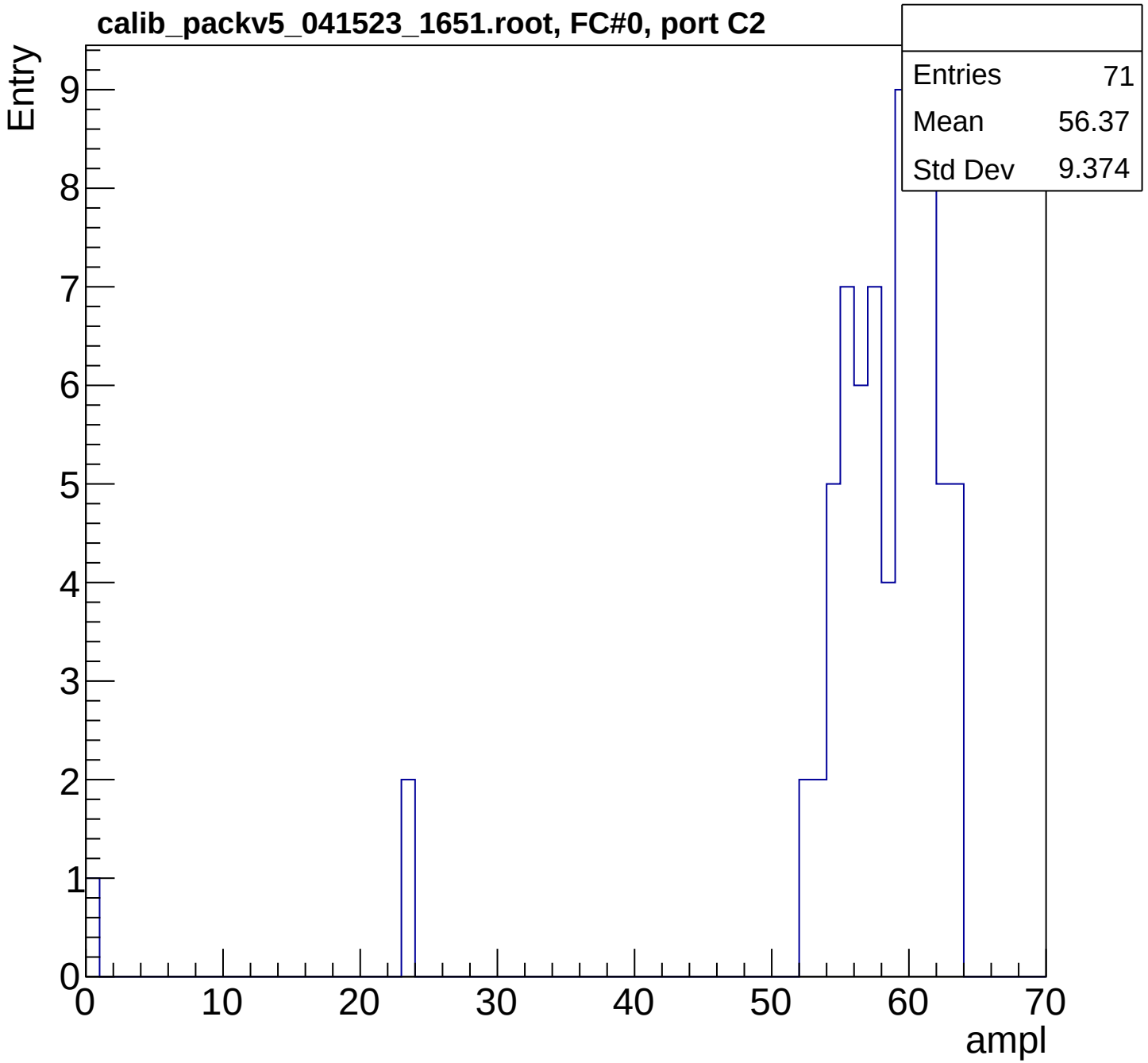

B1L103S, U2-ch106, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 21.46
Std Dev 12.1
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

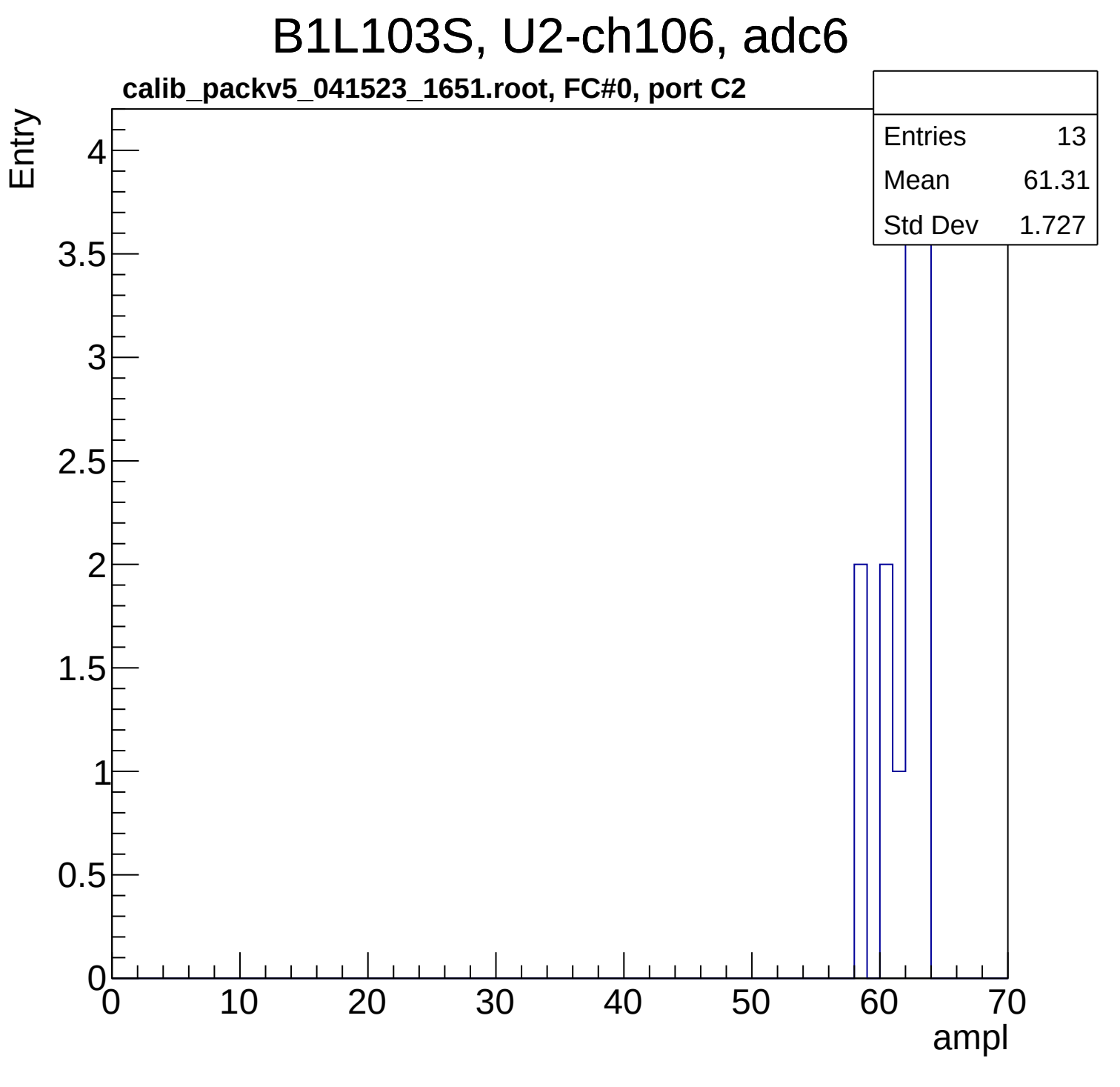

B1L103S, U2-ch106, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 33.67
Std Dev 6.596
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

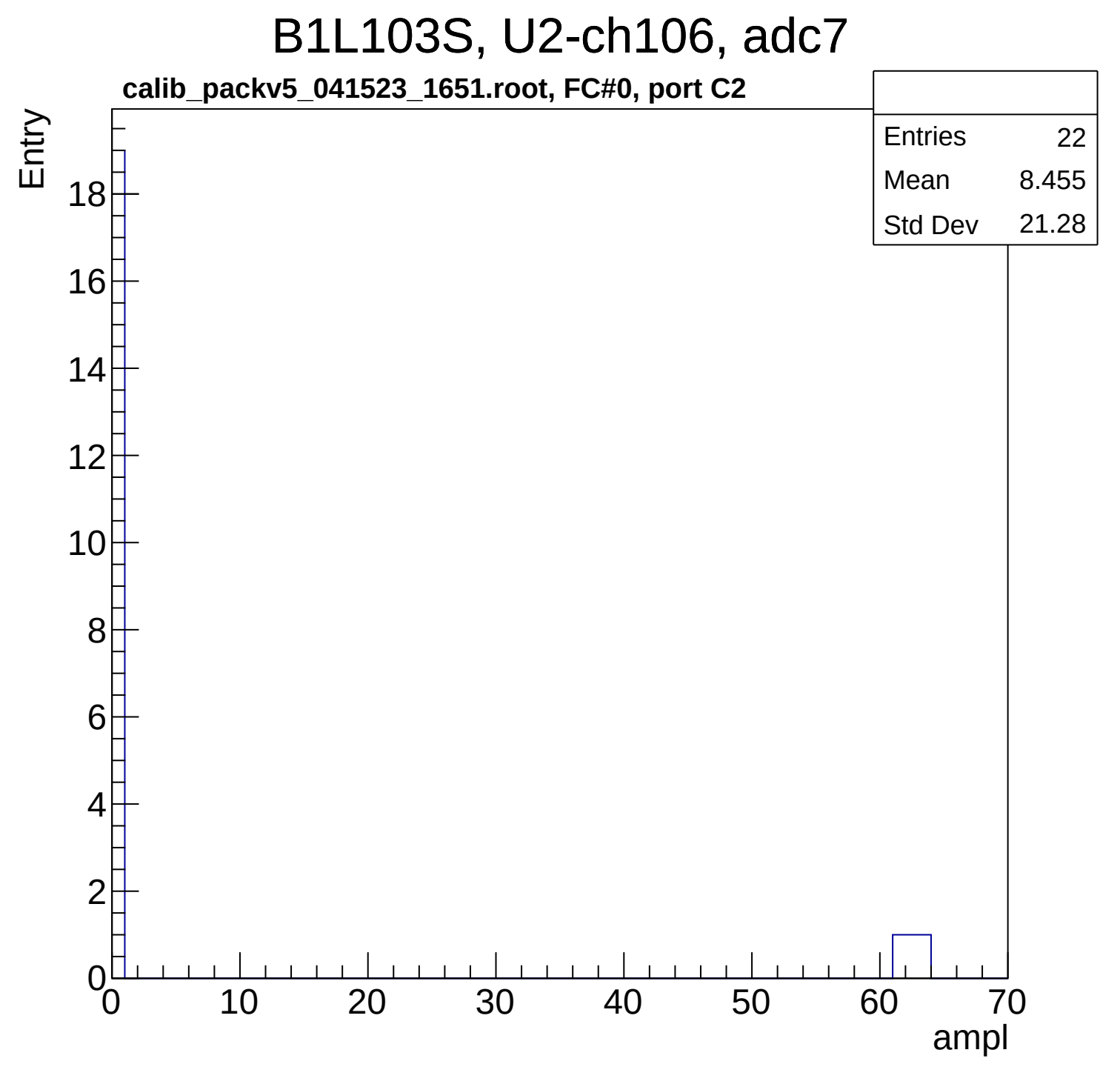

B1L103S, U2-ch106, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 38.1
Std Dev 12.04
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

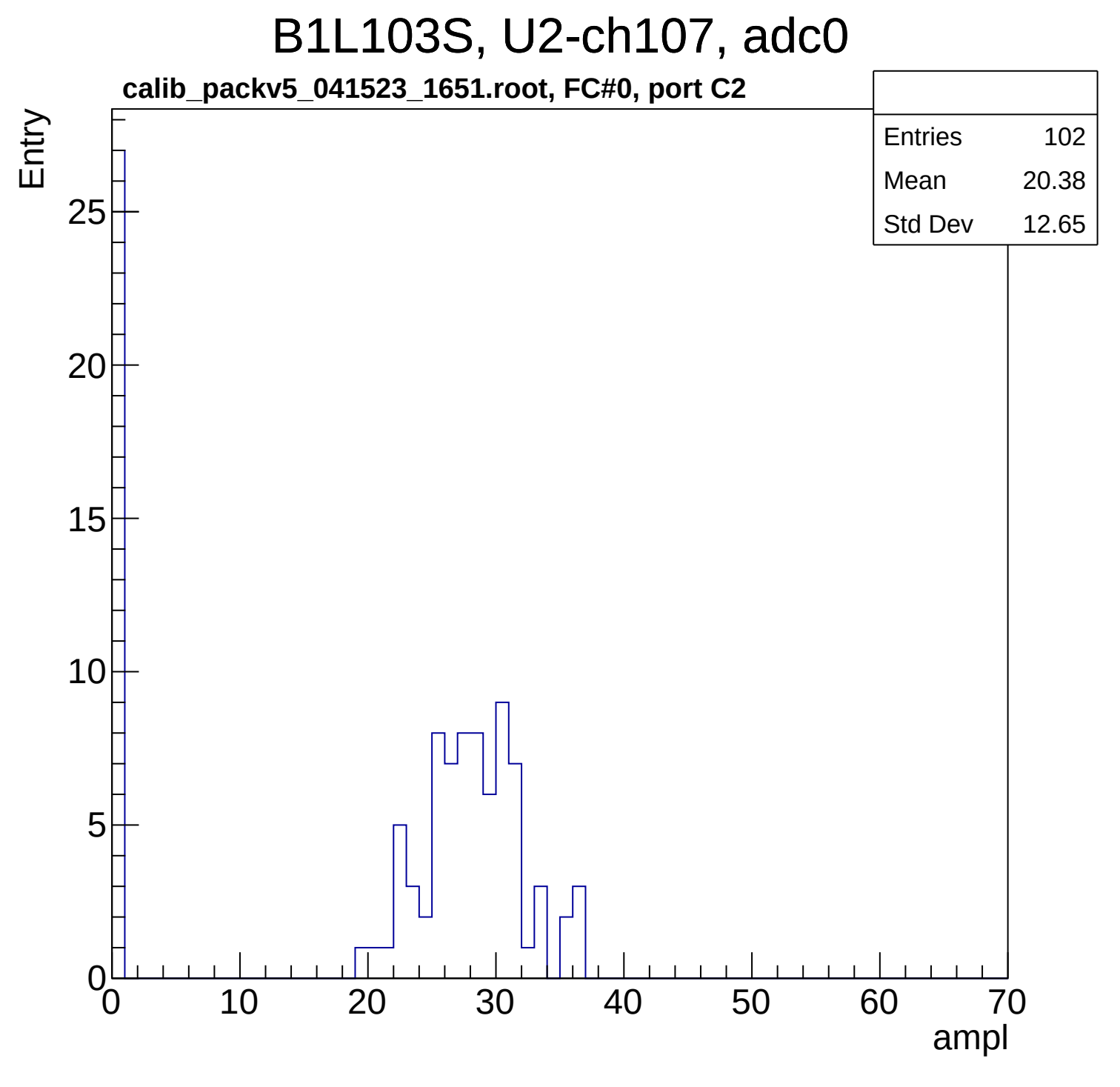

B1L103S, U2-ch106, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 40.37
Std Dev 17.03
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

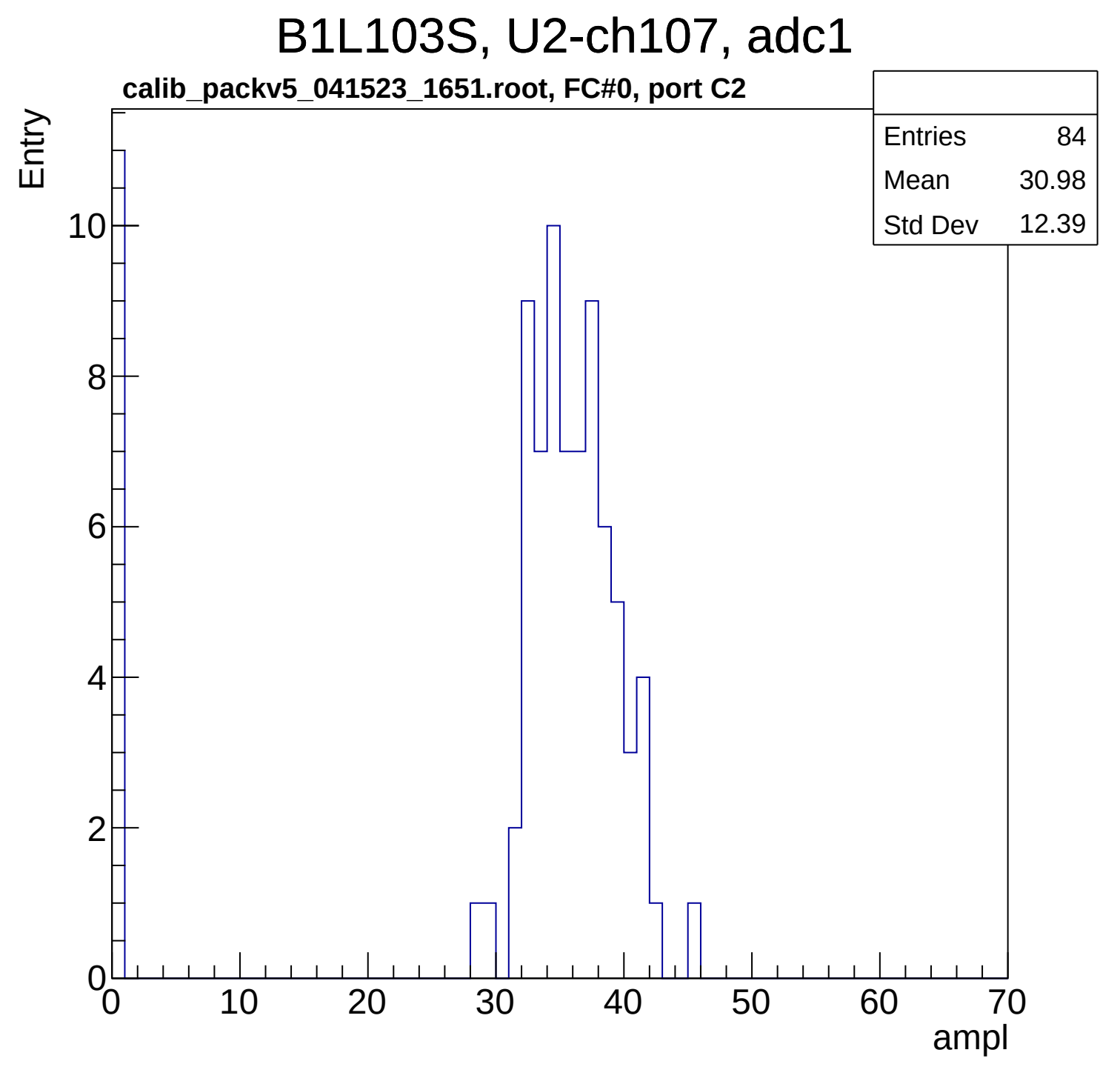

B1L103S, U2-ch106, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 51.57
Std Dev 8.01
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

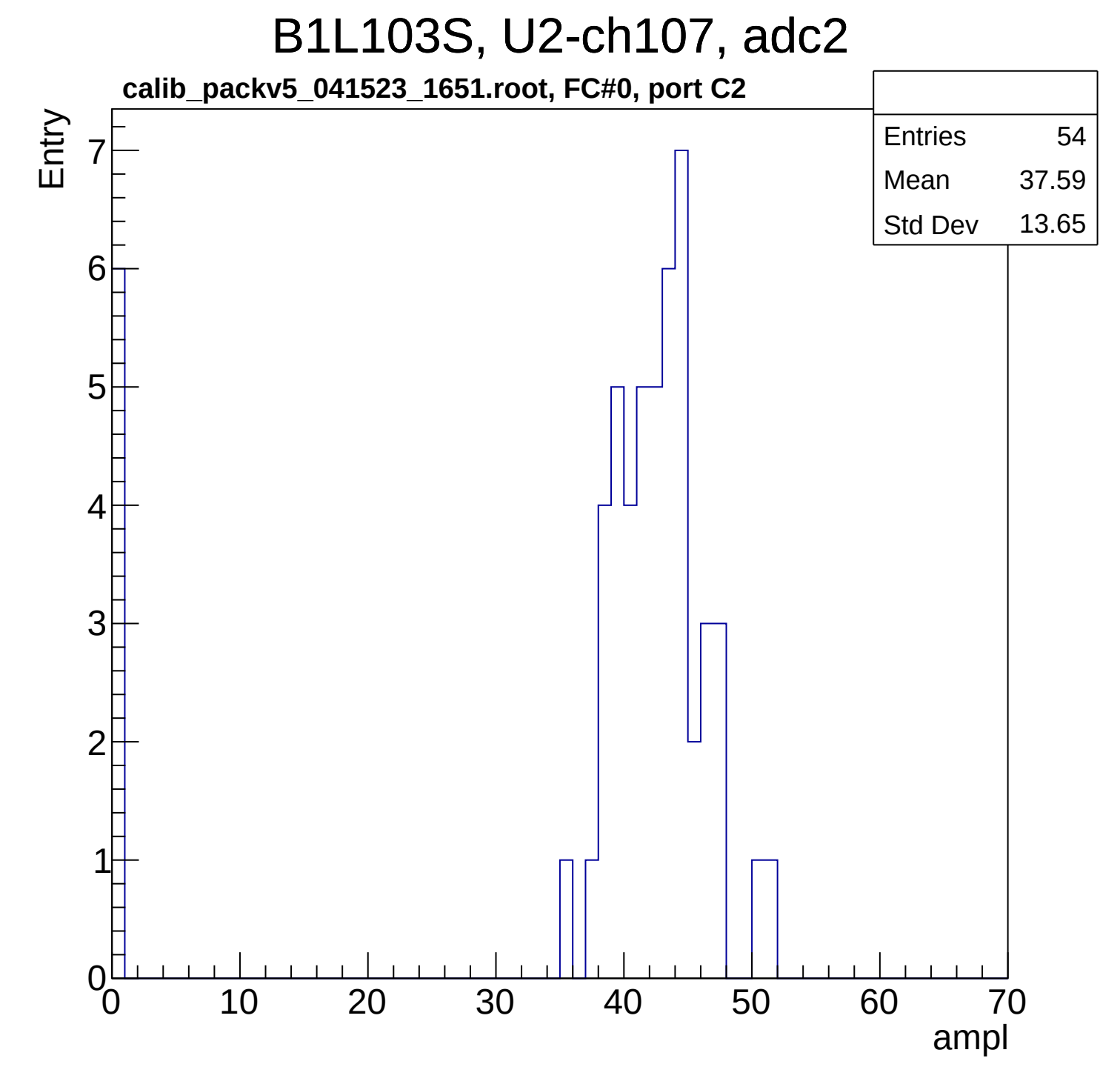

B1L103S, U2-ch106, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 56.37
Std Dev 9.374
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

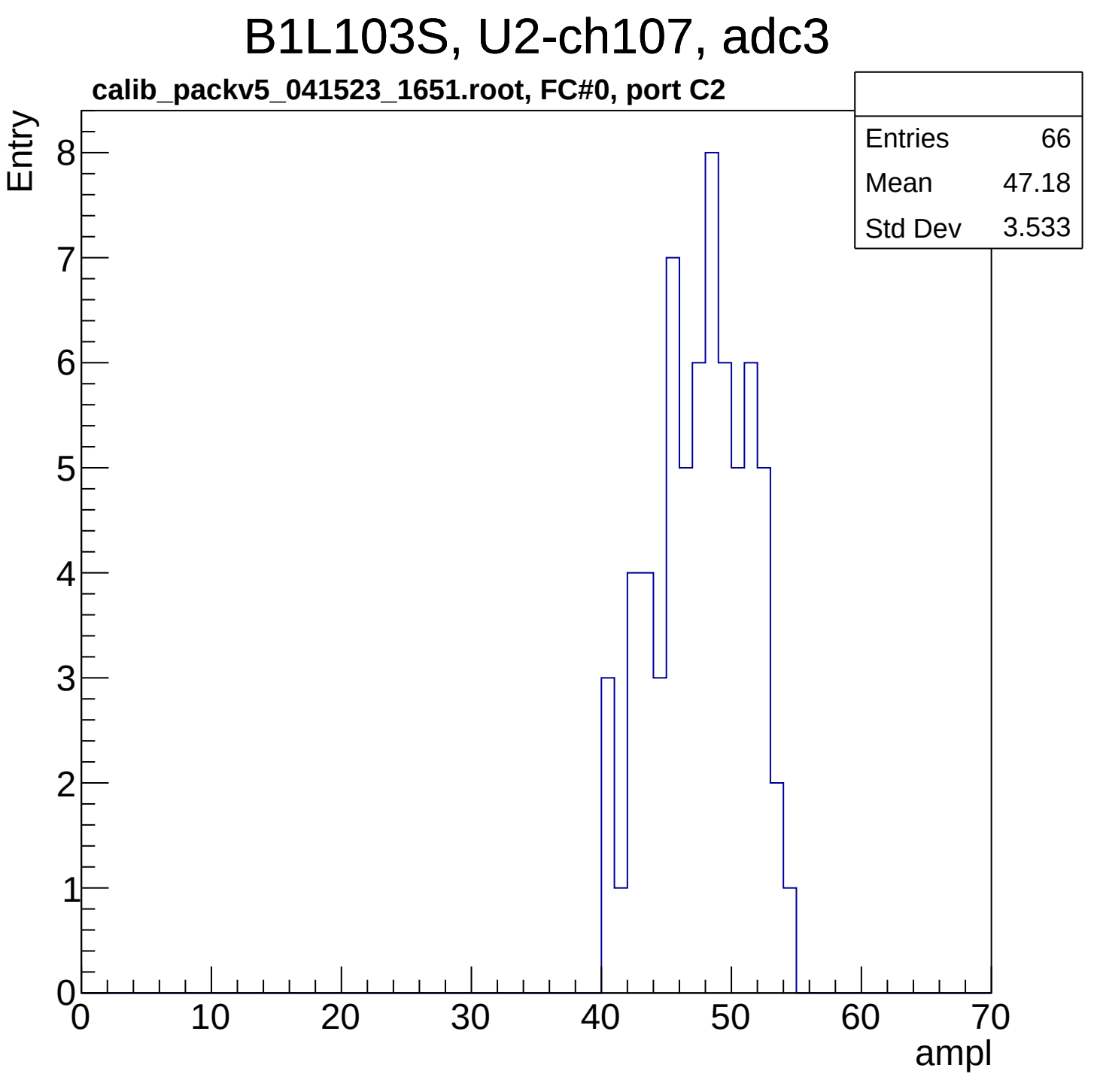

B1L103S, U2-ch106, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.31
Std Dev 1.727
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

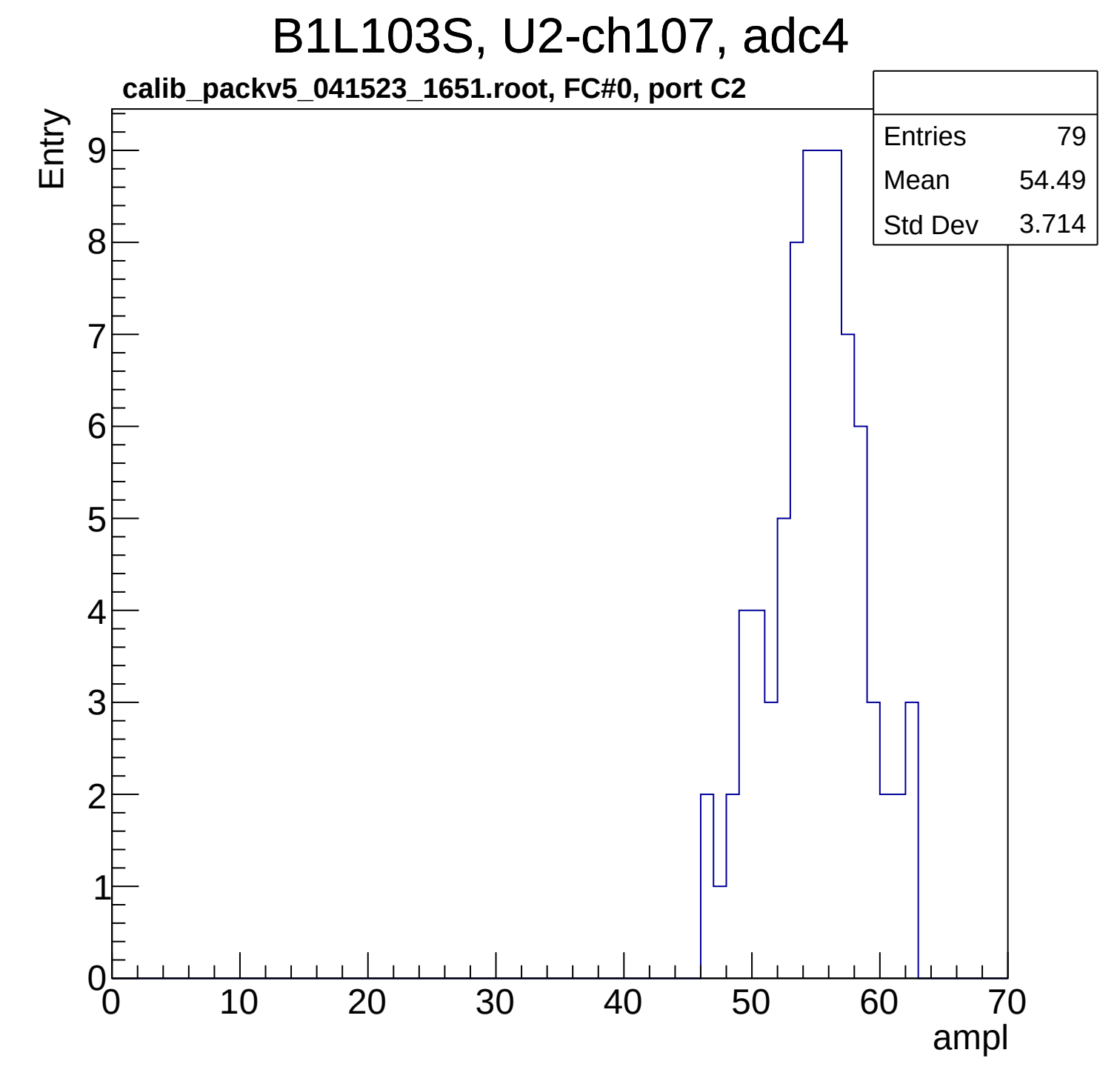

B1L103S, U2-ch106, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.455
Std Dev 21.28
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

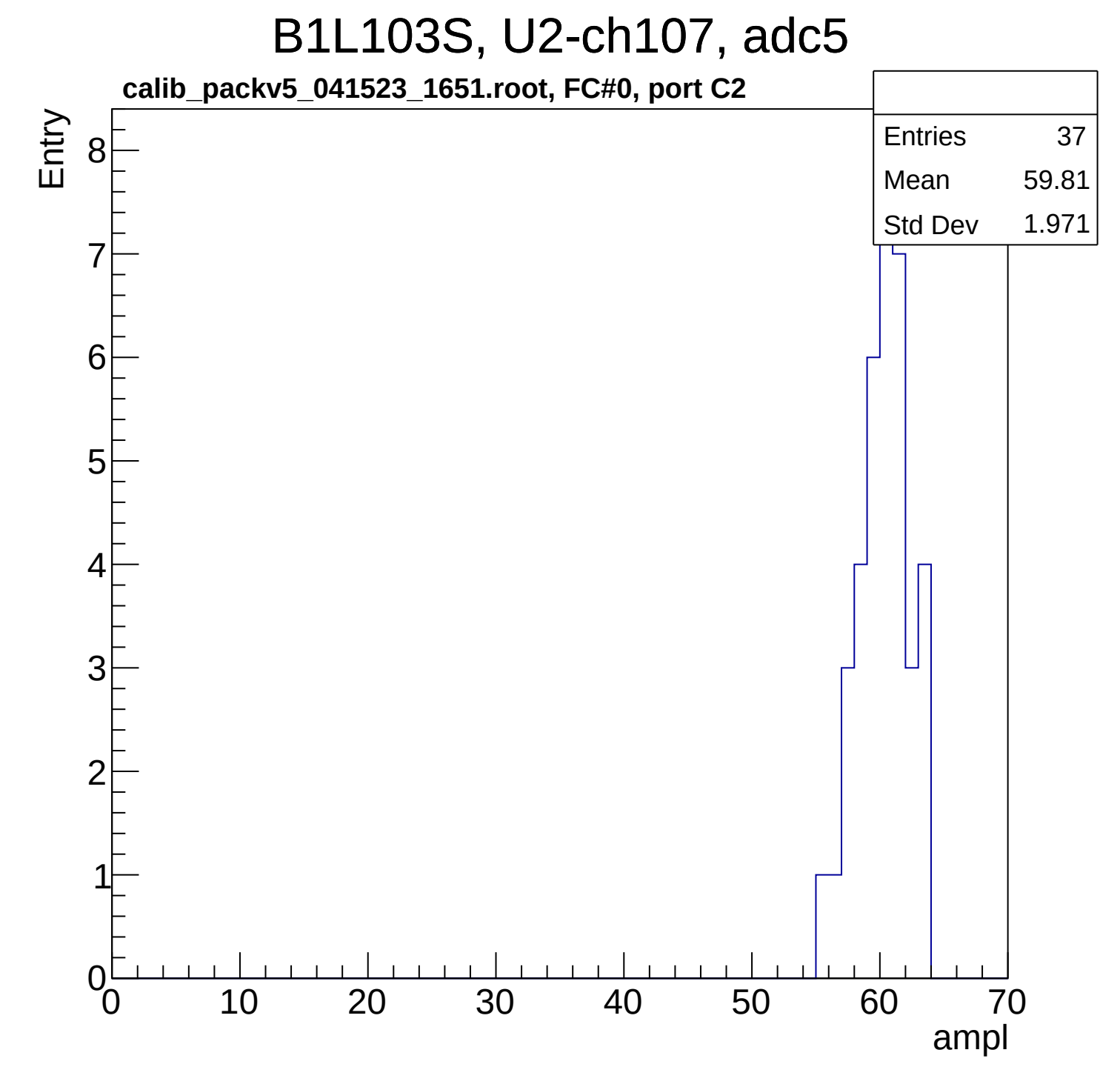

B1L103S, U2-ch107, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 20.38
Std Dev 12.65
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl

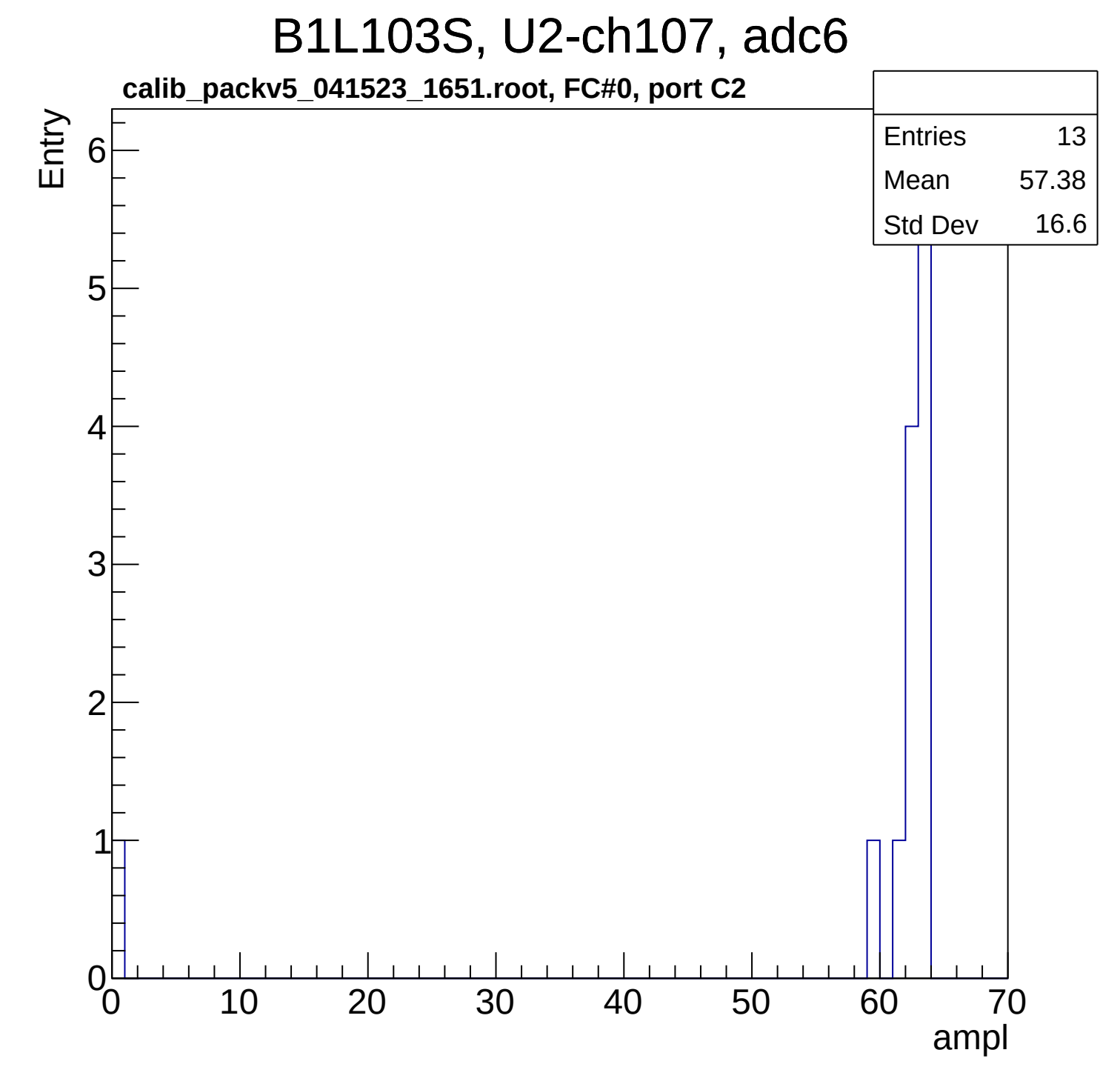

B1L103S, U2-ch107, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 30.98
Std Dev 12.39
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

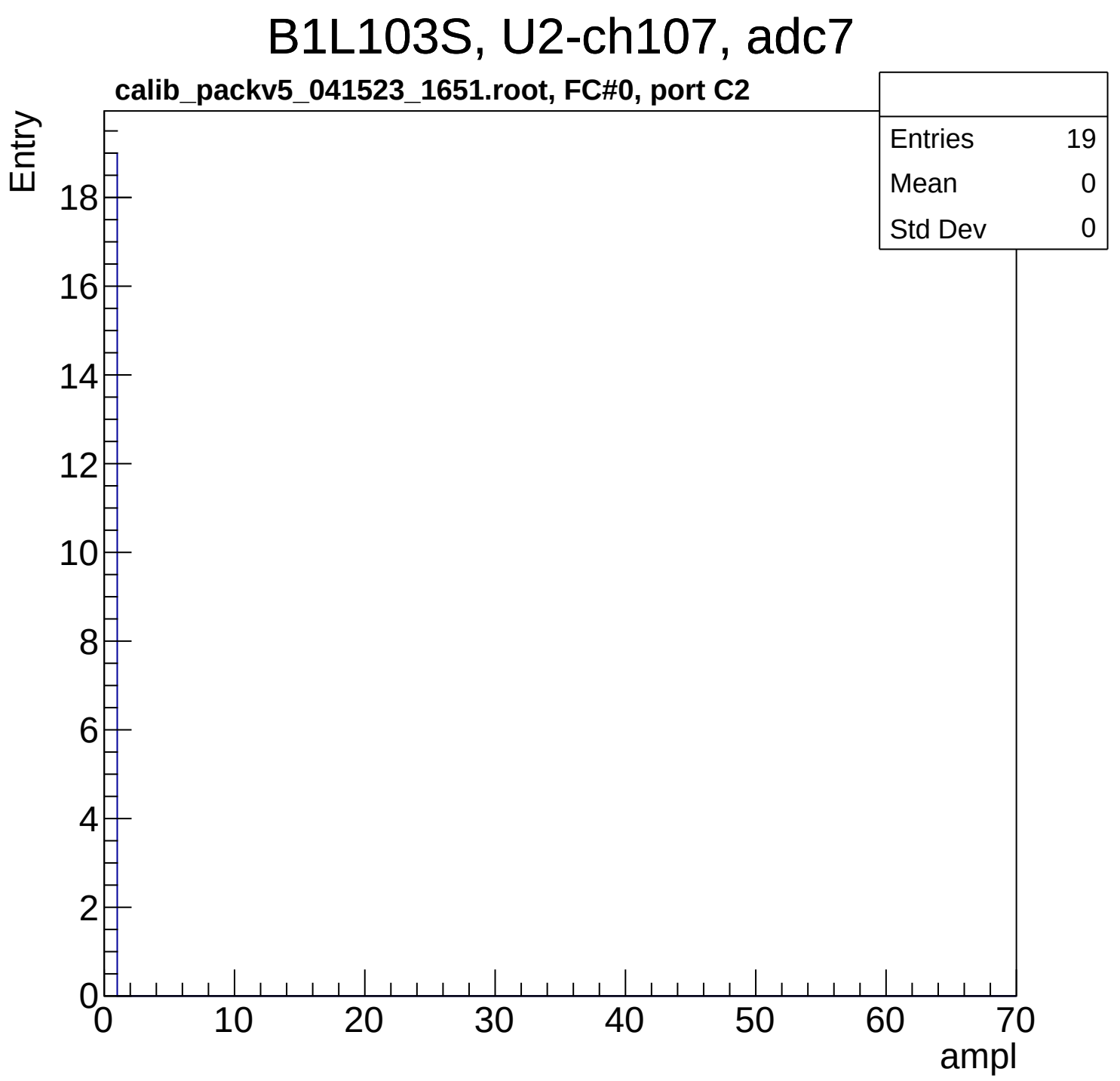

B1L103S, U2-ch107, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 37.59
Std Dev 13.65
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

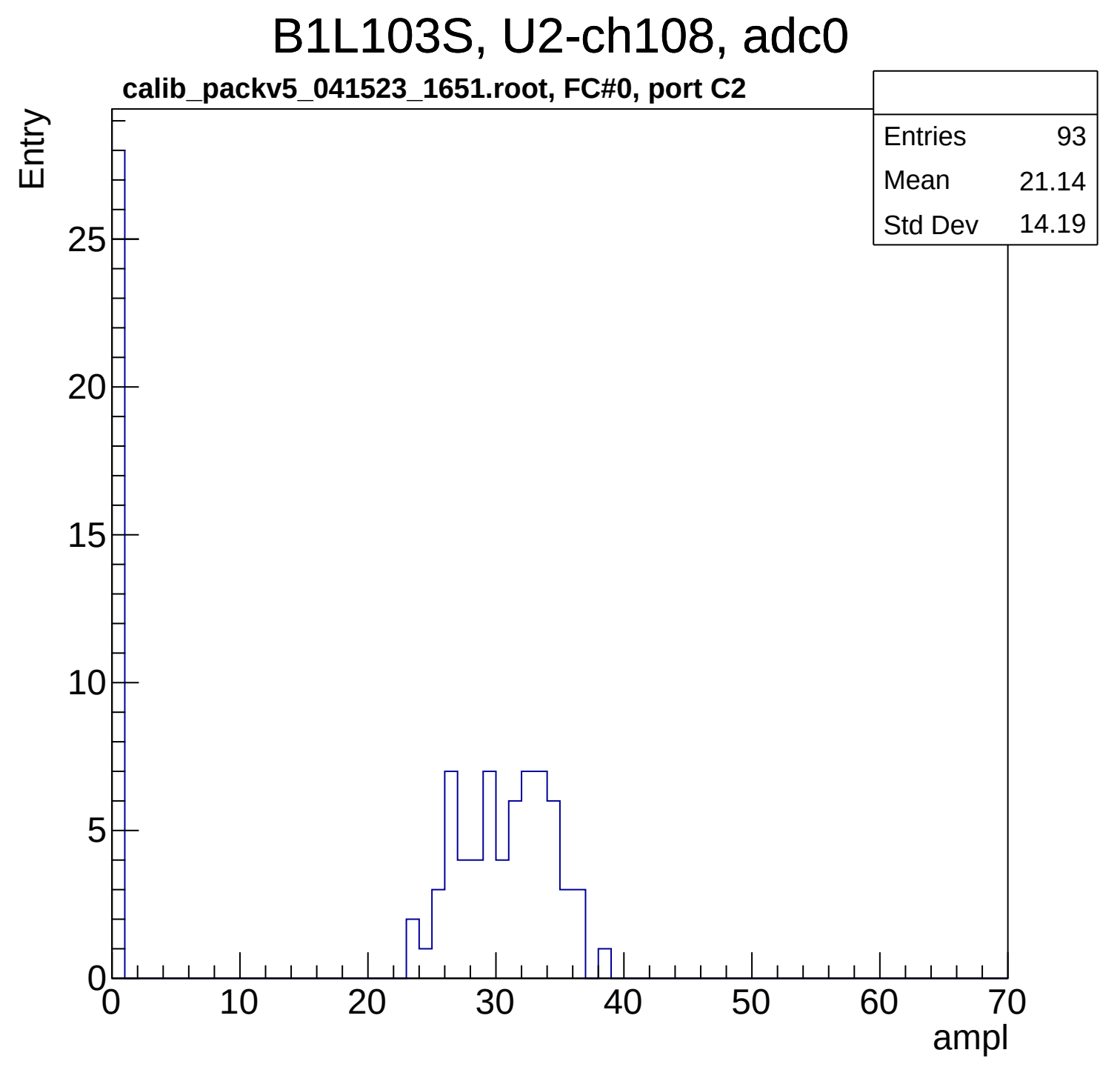

B1L103S, U2-ch107, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 47.18
Std Dev 3.533
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

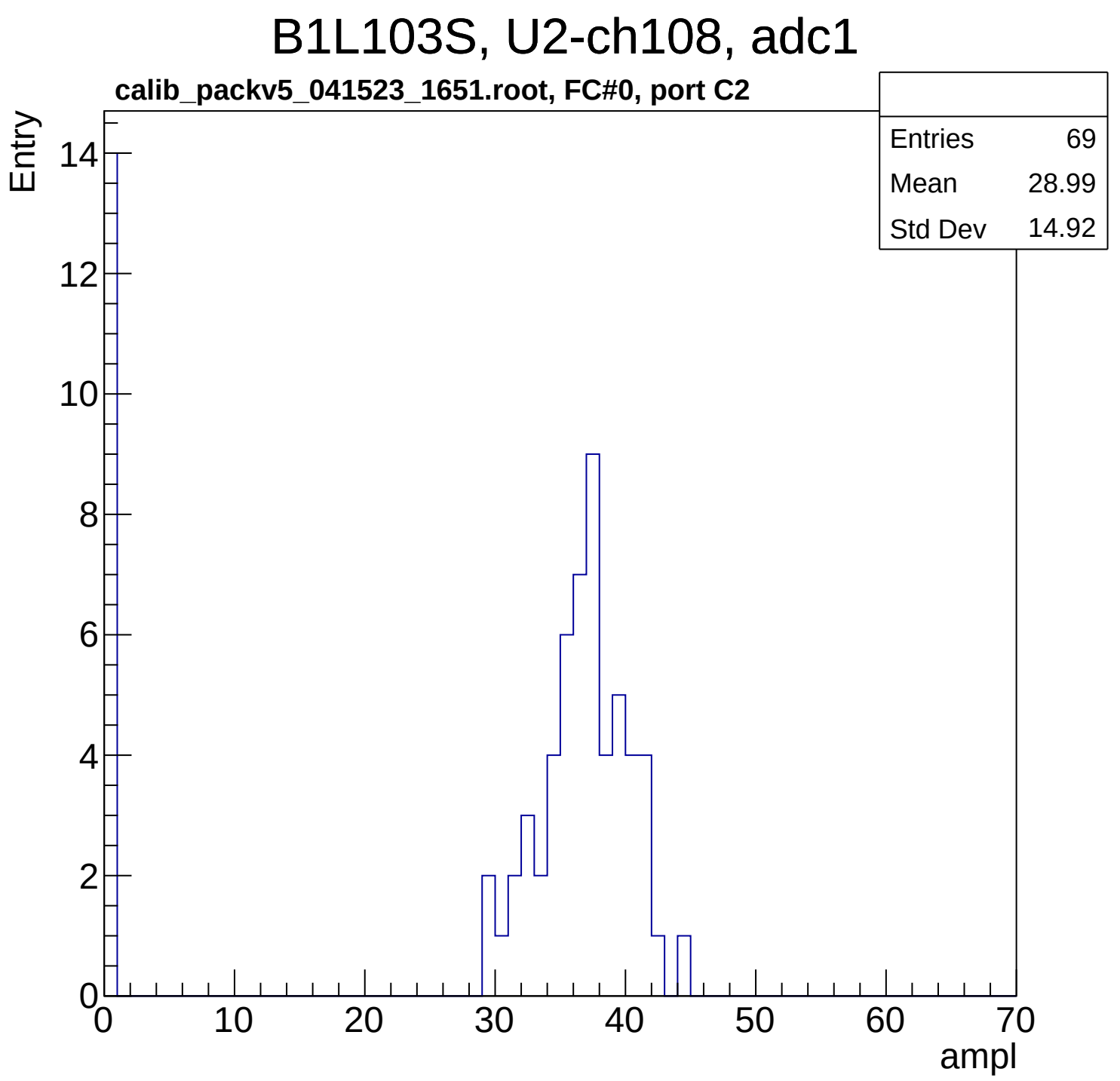

B1L103S, U2-ch107, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 54.49
Std Dev 3.714
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

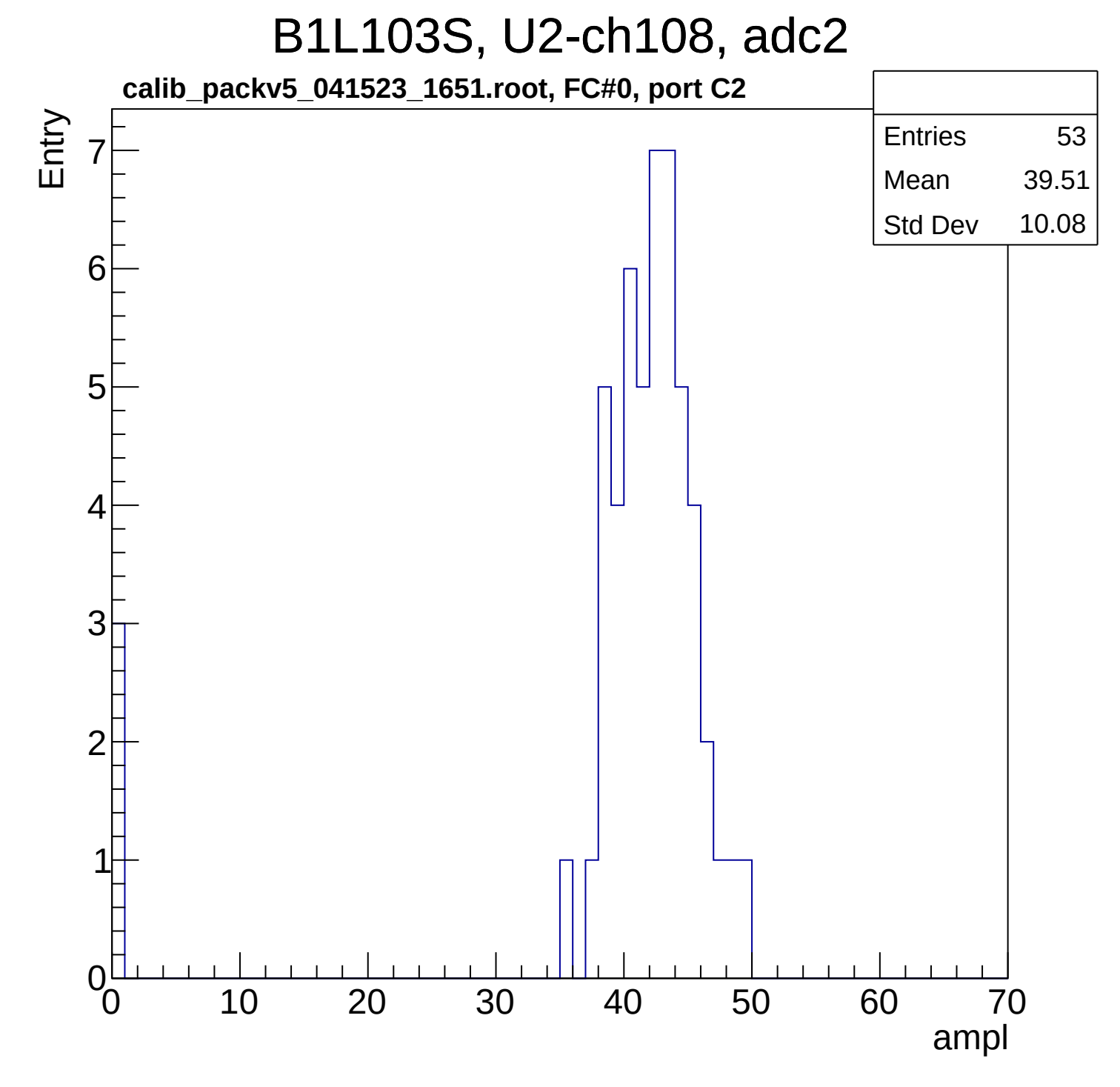

B1L103S, U2-ch107, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 59.81
Std Dev 1.971
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

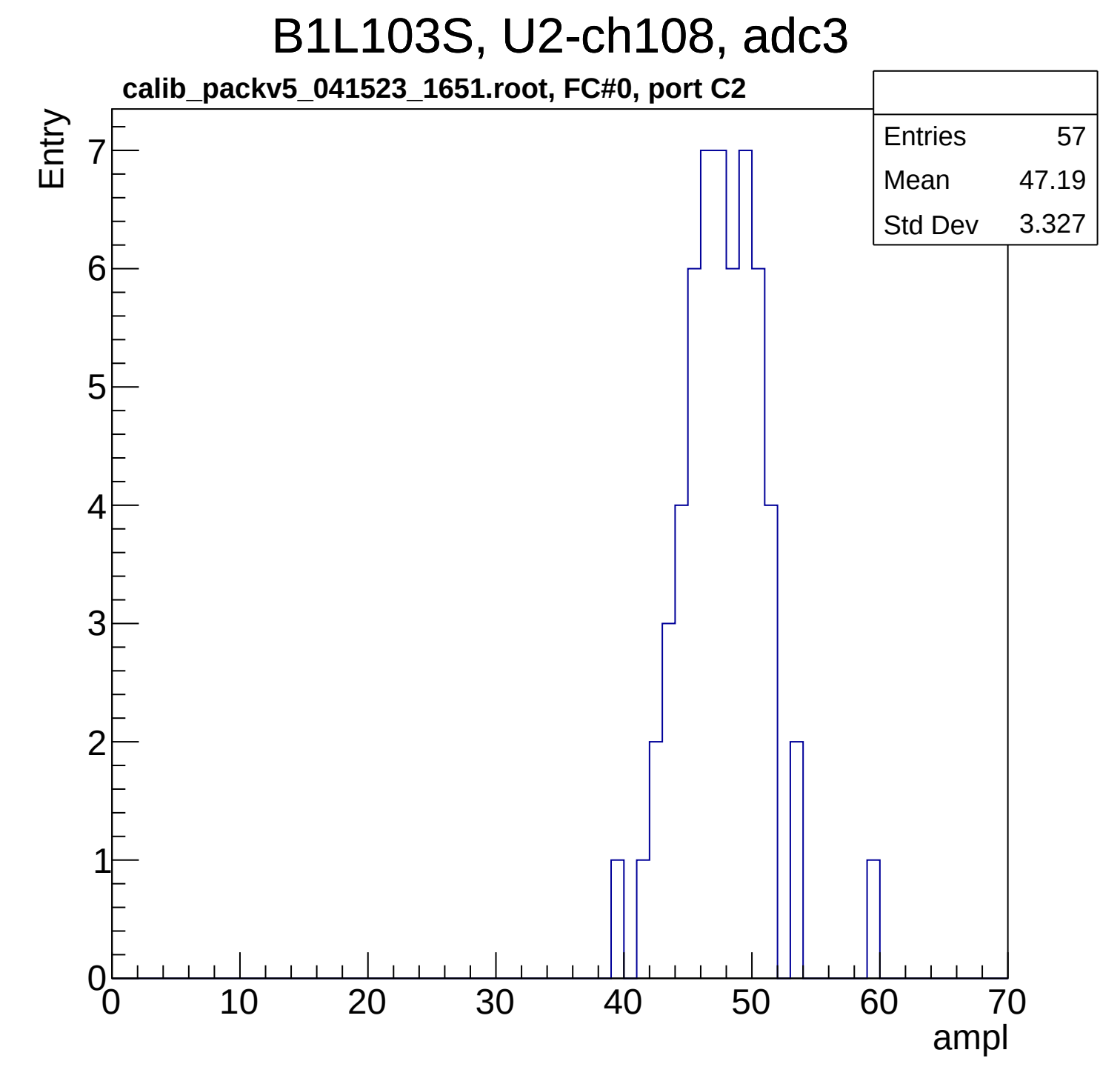

B1L103S, U2-ch107, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 57.38
Std Dev 16.6
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

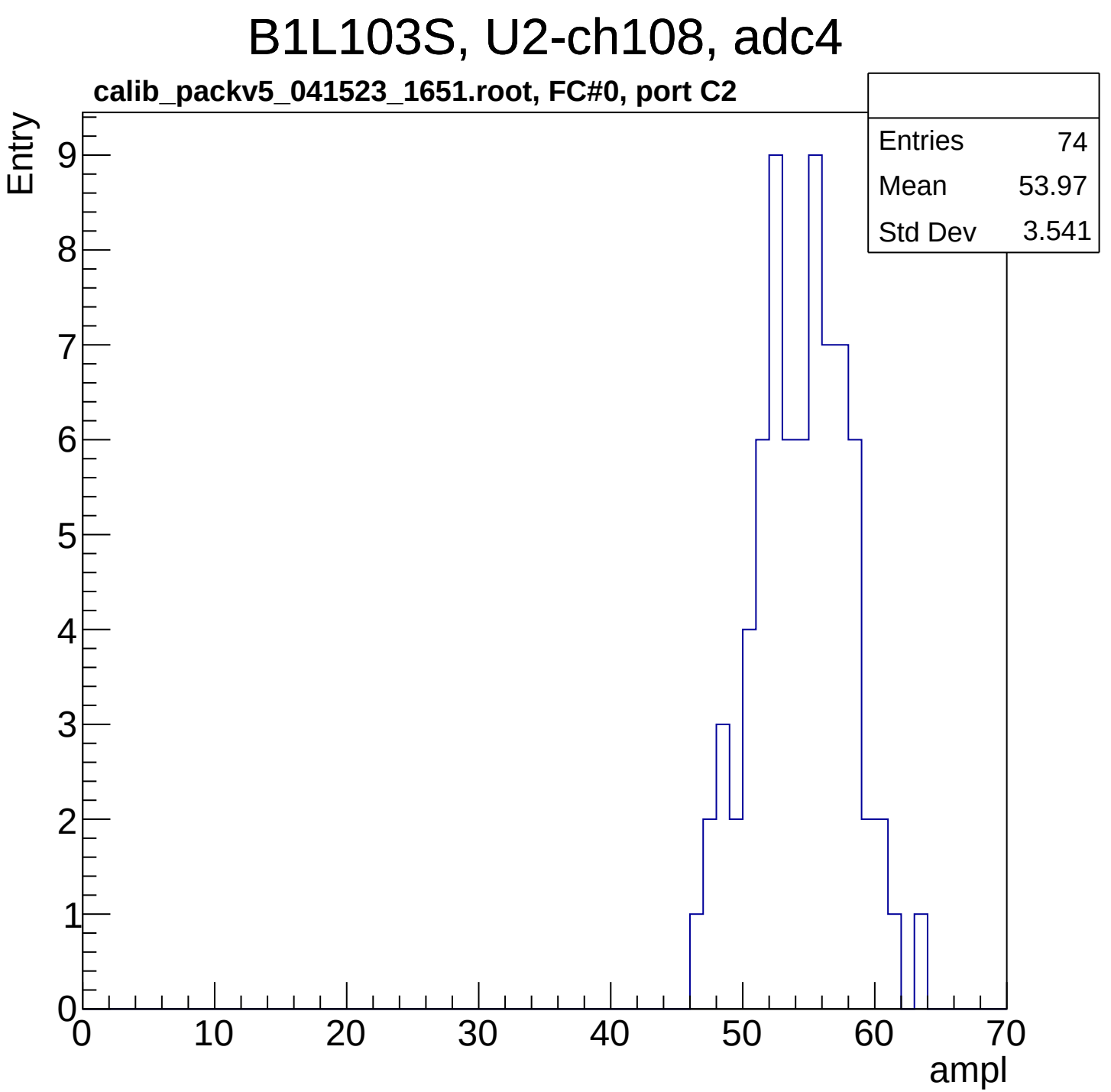

B1L103S, U2-ch107, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

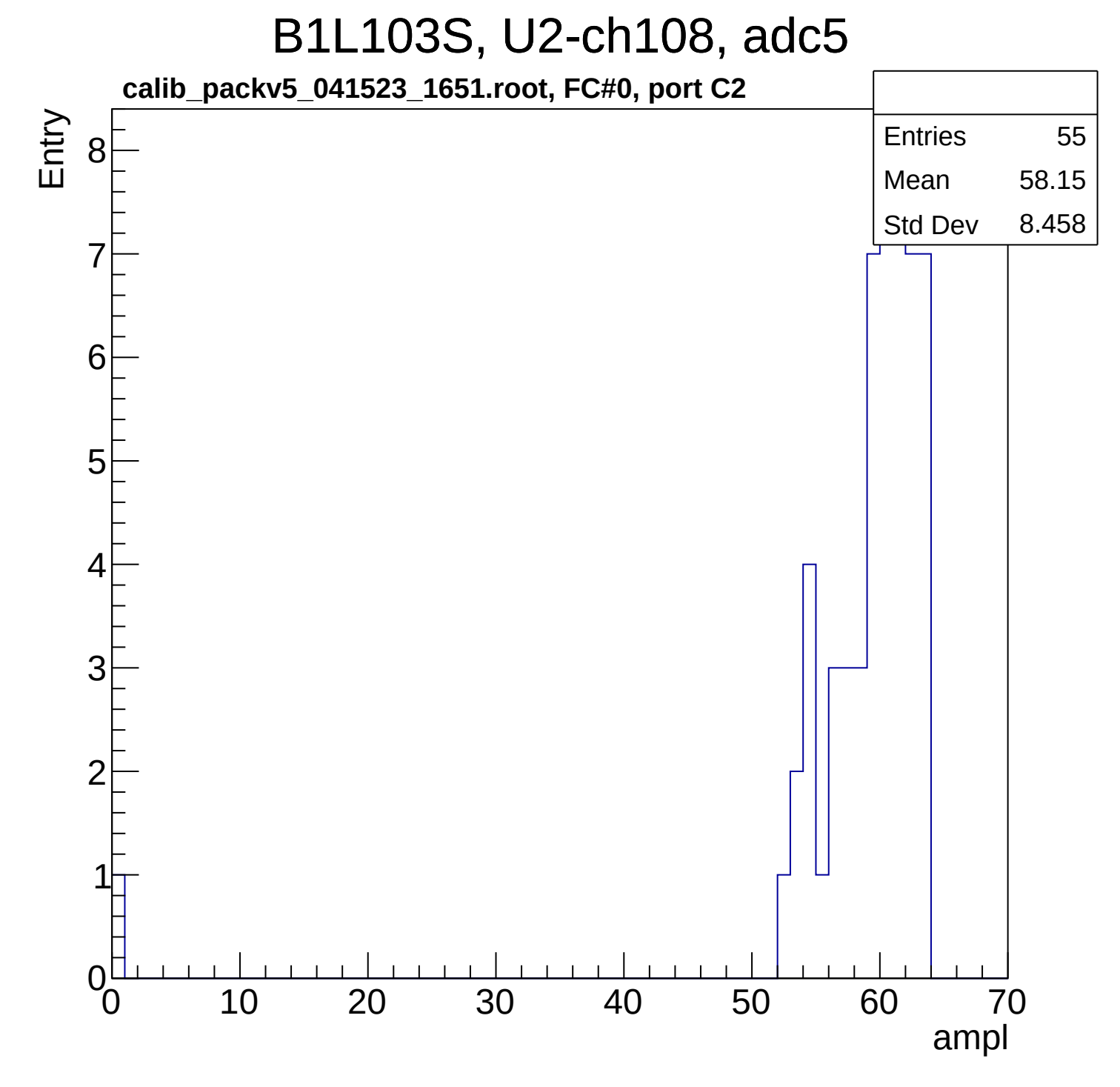

B1L103S, U2-ch108, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 21.14
Std Dev 14.19
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl

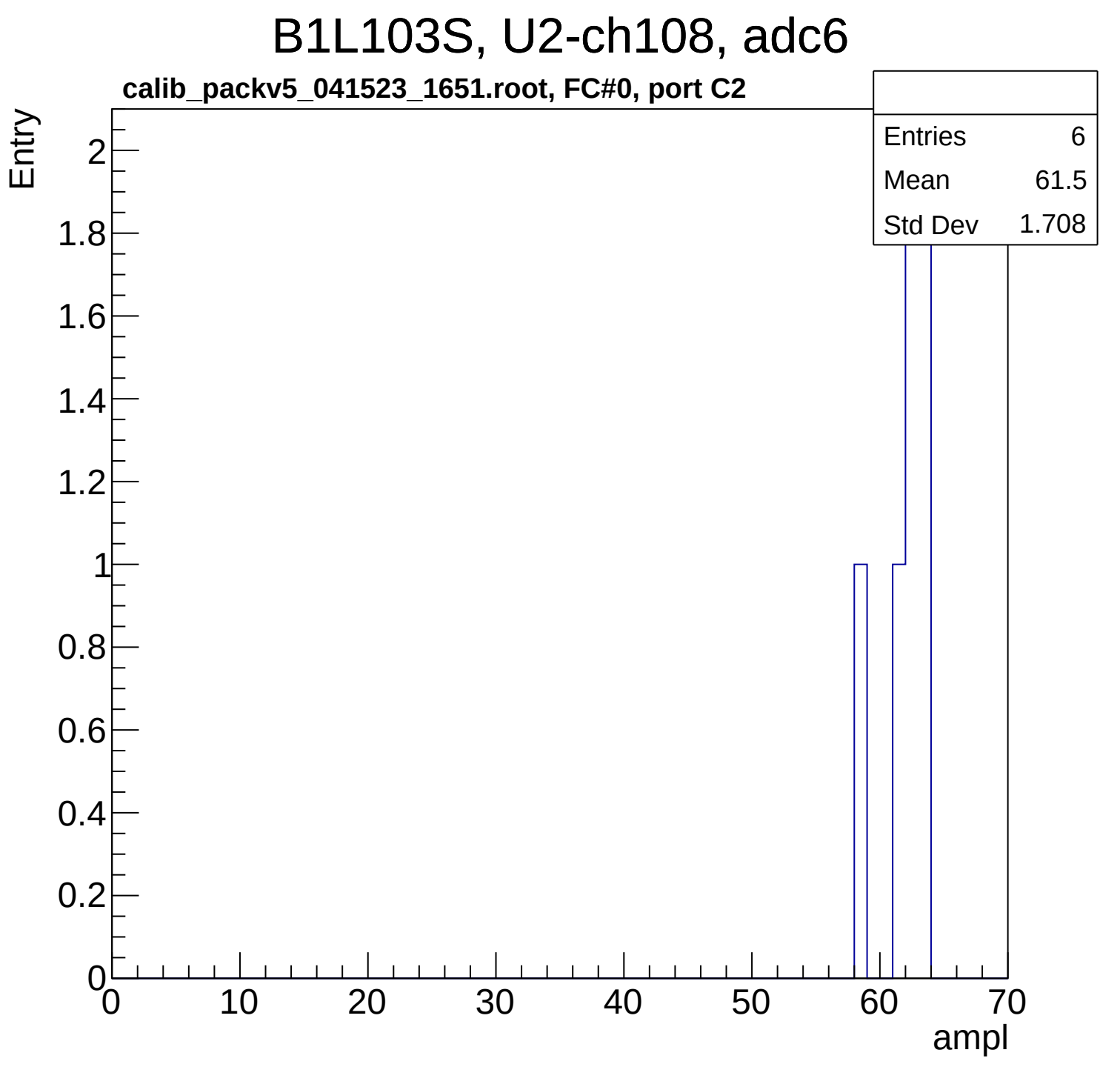

B1L103S, U2-ch108, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 28.99
Std Dev 14.92
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

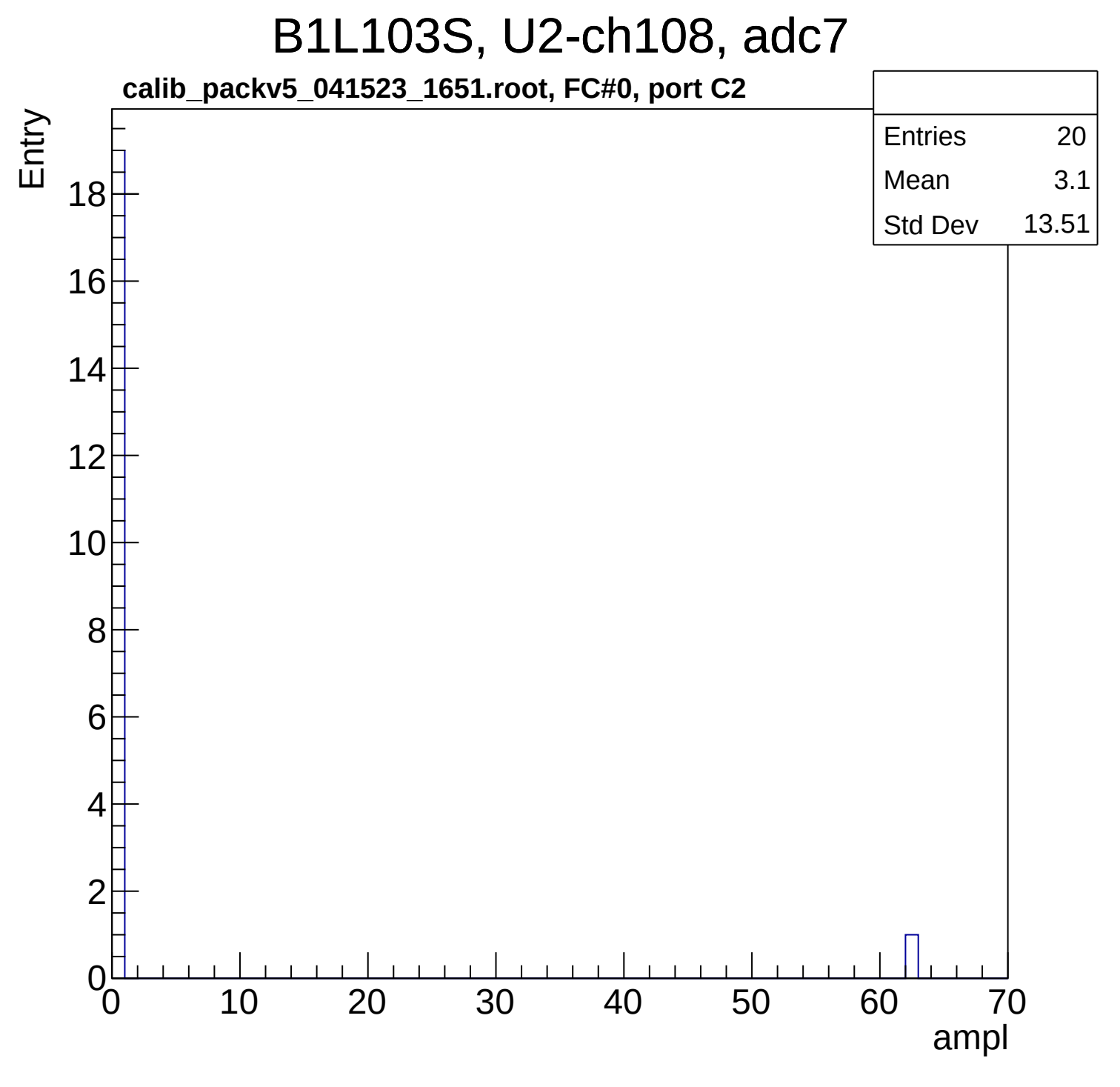

B1L103S, U2-ch108, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 39.51
Std Dev 10.08
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

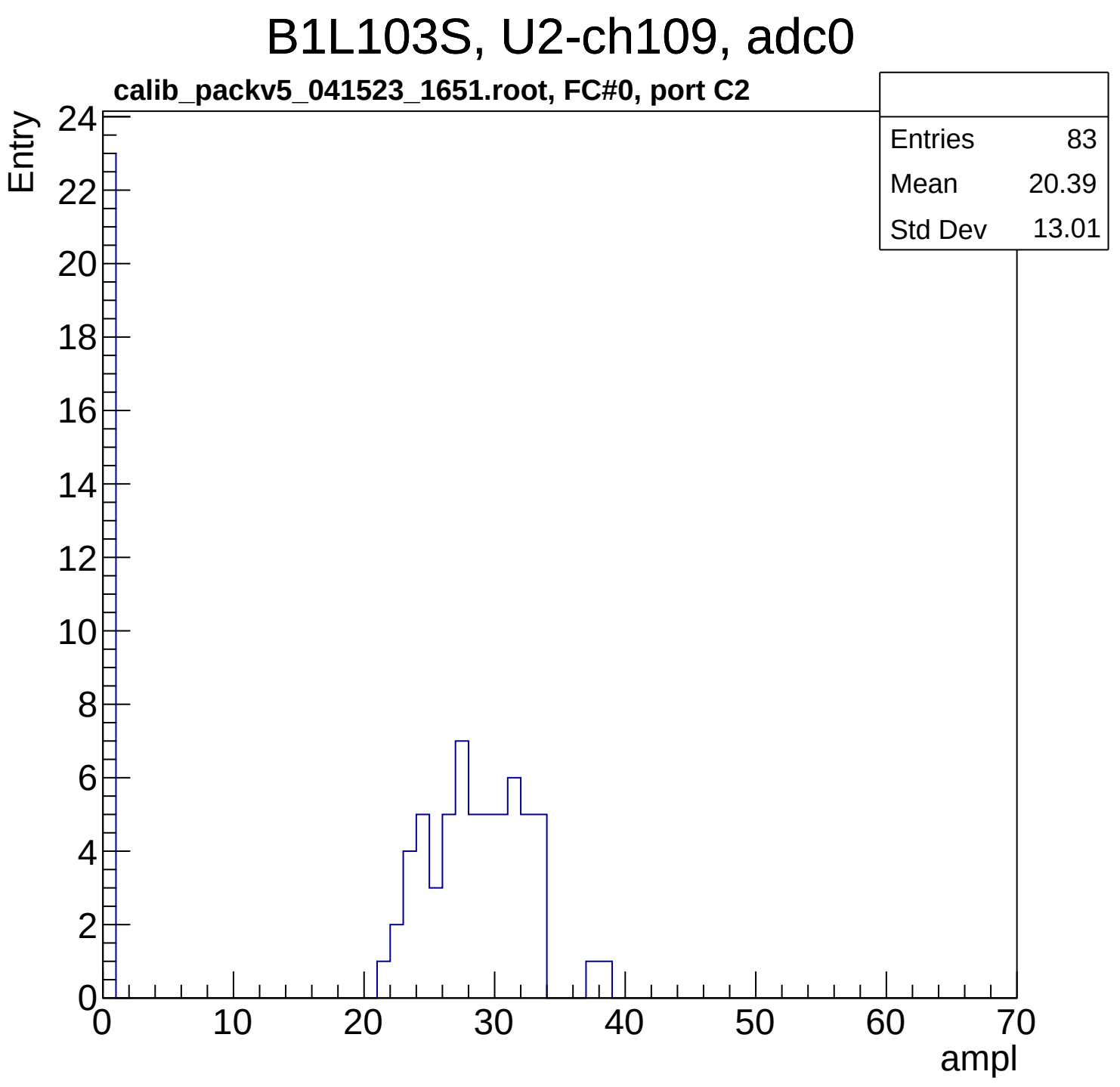

B1L103S, U2-ch108, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 47.19
Std Dev 3.327
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

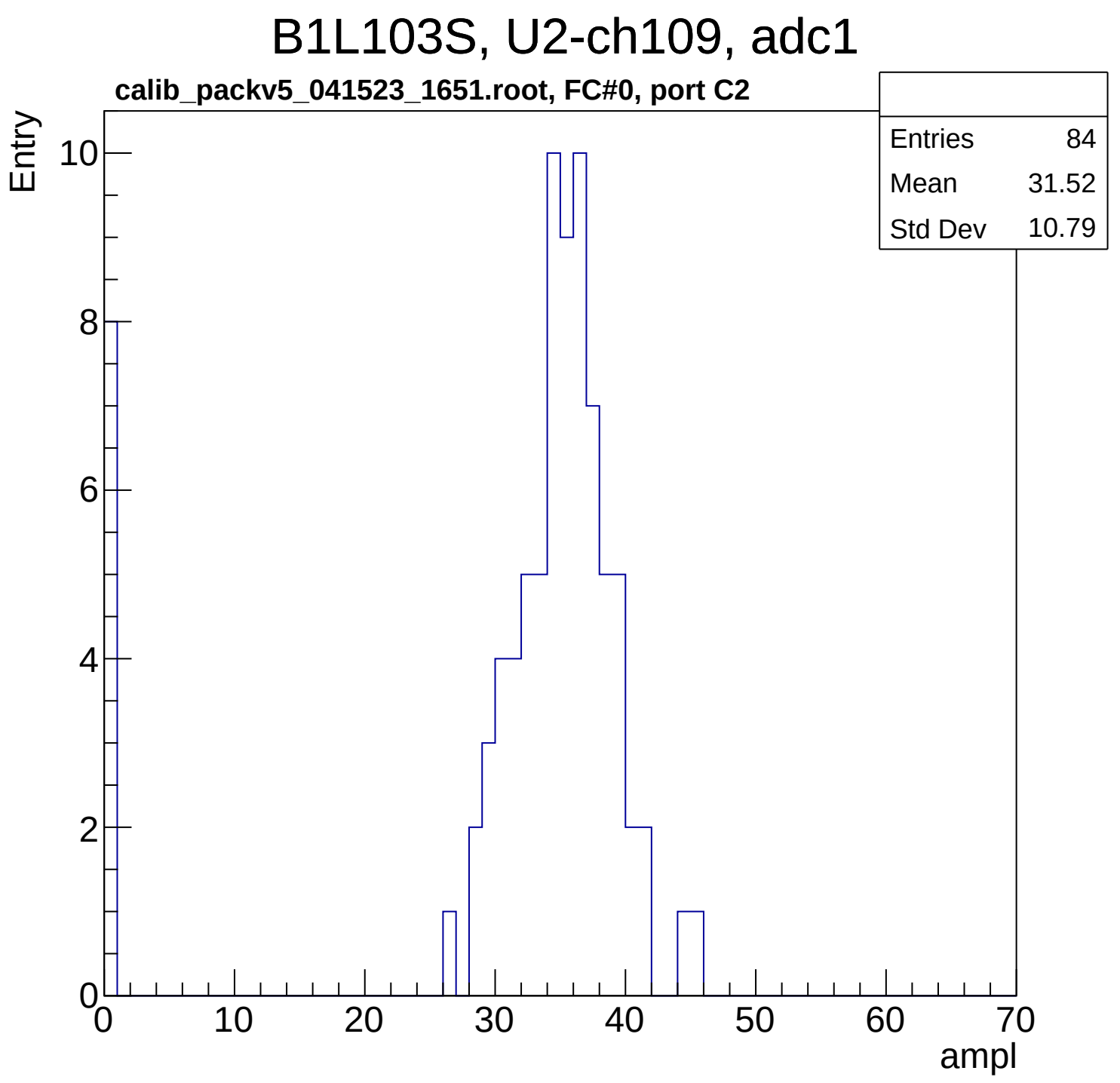

B1L103S, U2-ch108, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 53.97
Std Dev 3.541
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

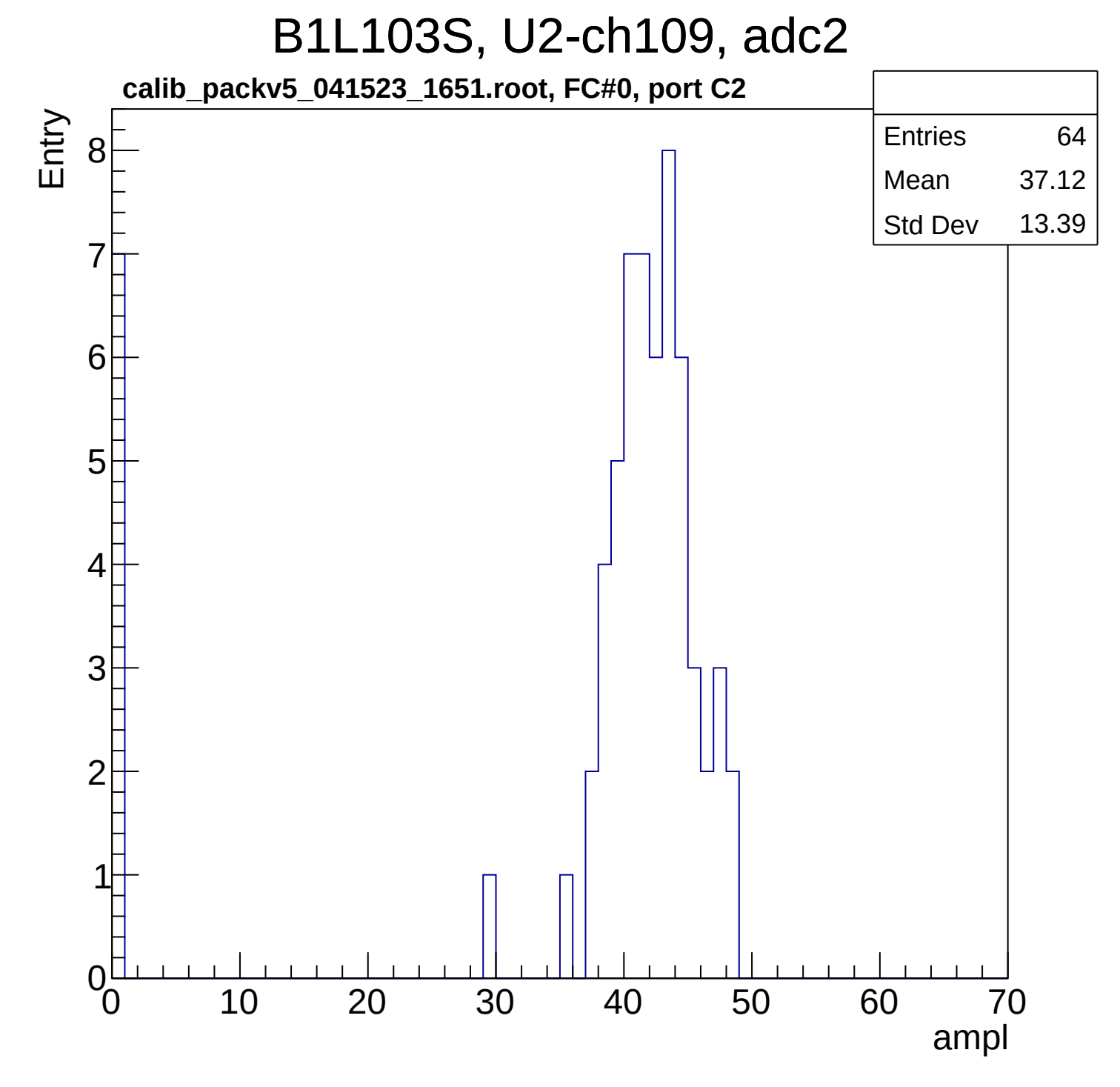

B1L103S, U2-ch108, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.15
Std Dev 8.458
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

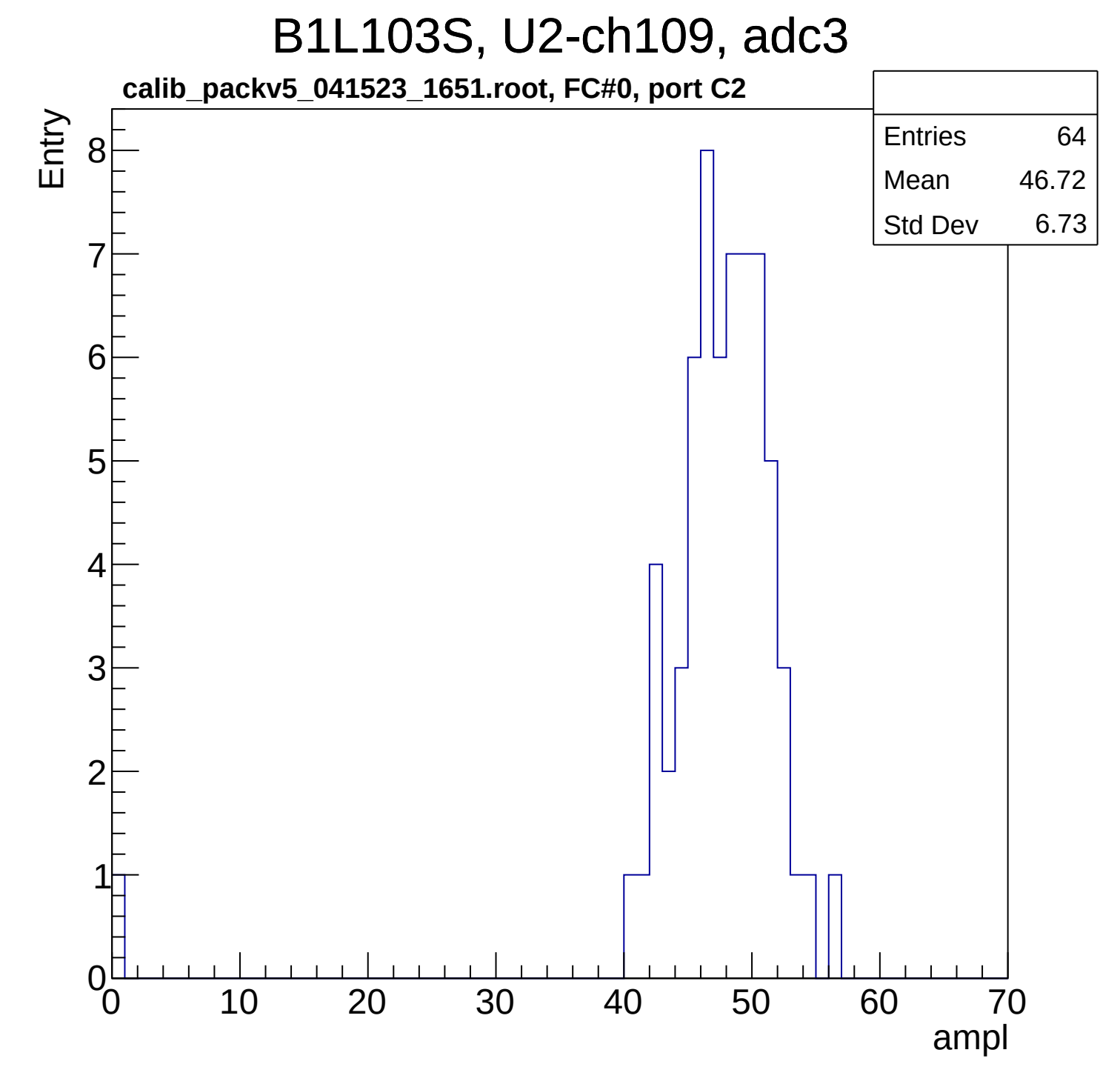

B1L103S, U2-ch108, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.5
Std Dev 1.708
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

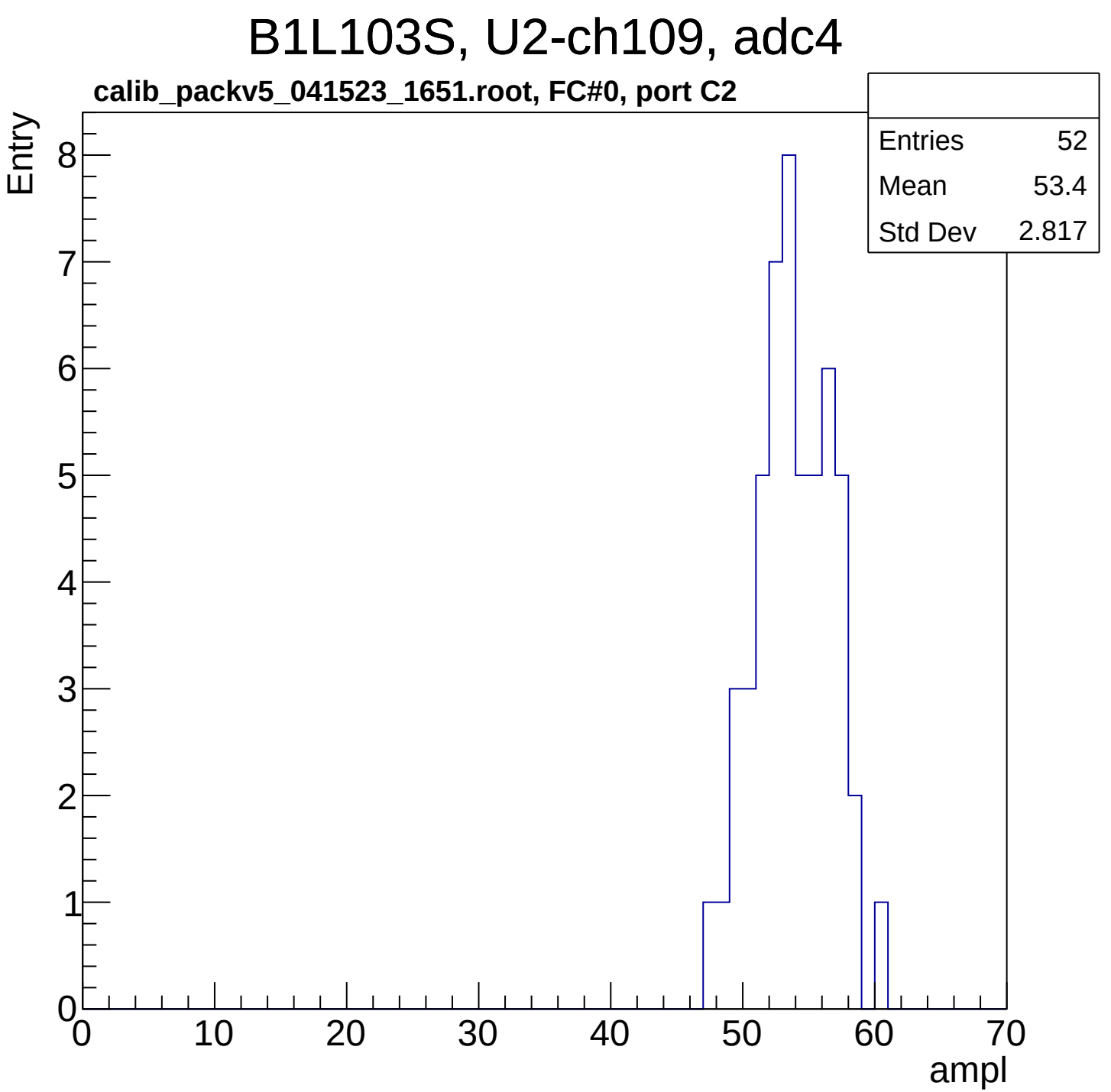

B1L103S, U2-ch108, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

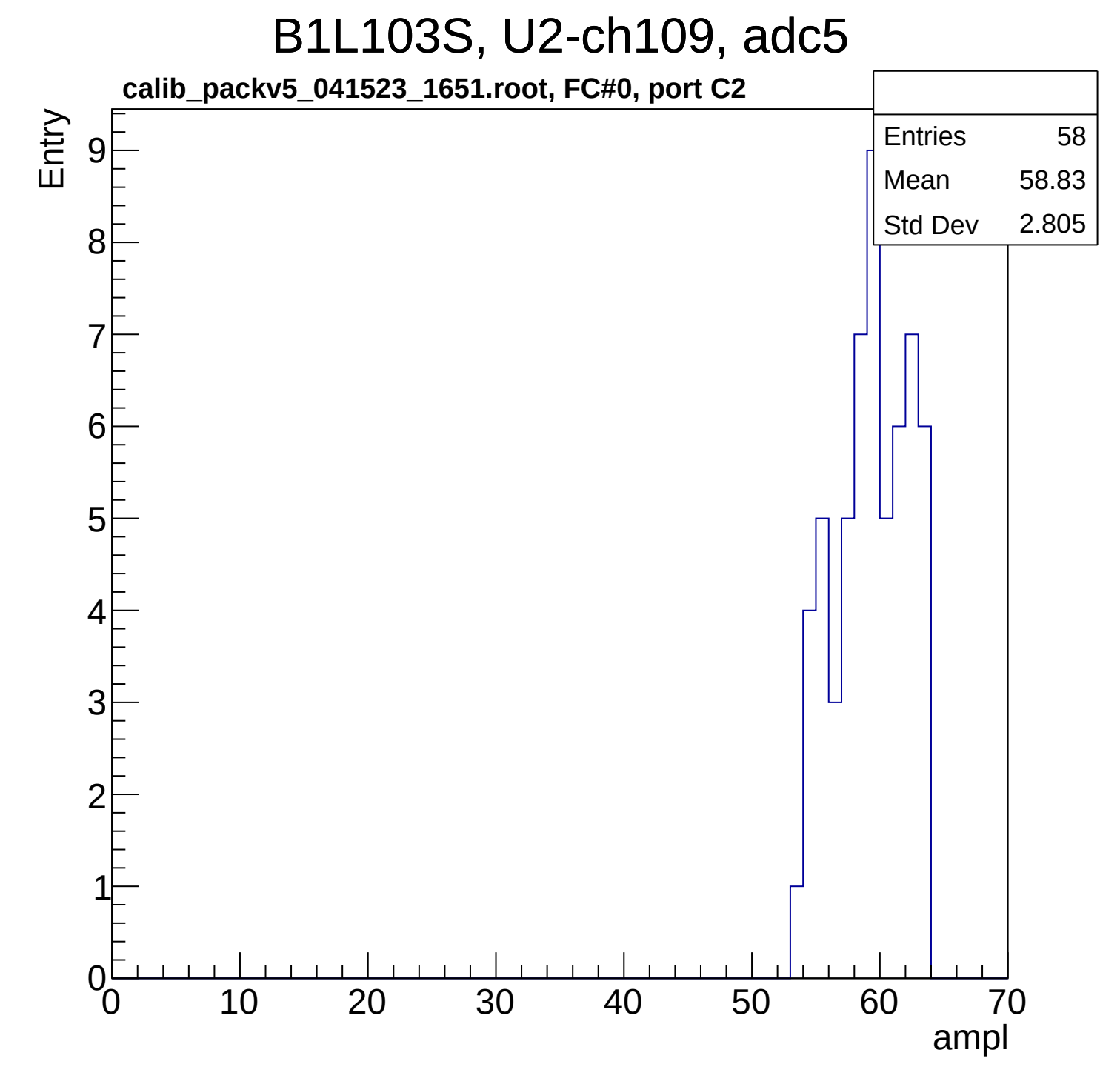

B1L103S, U2-ch109, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 20.39
Std Dev 13.01
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70

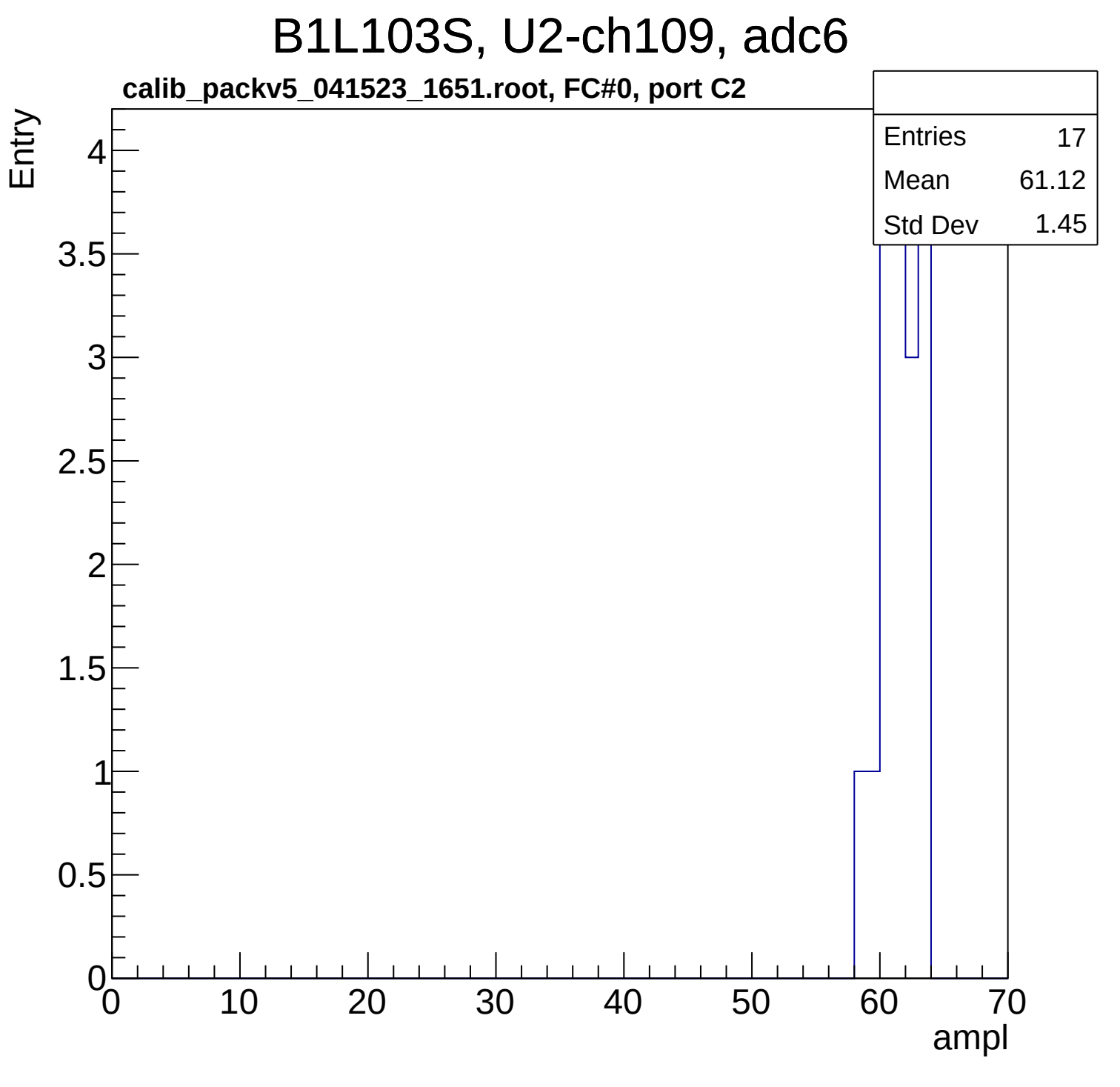

B1L103S, U2-ch109, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 31.52
Std Dev 10.79
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

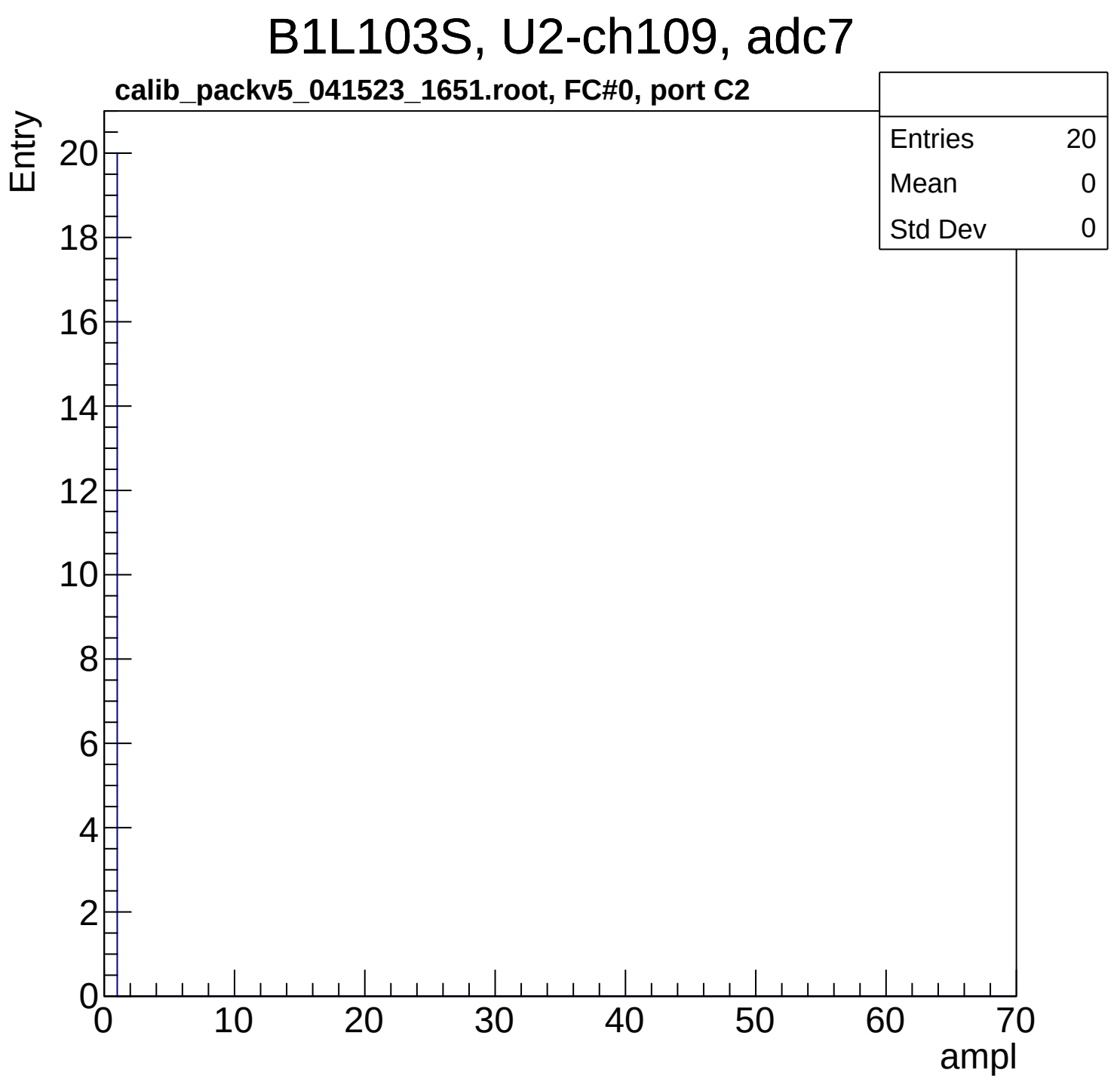

B1L103S, U2-ch109, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 37.12
Std Dev 13.39
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

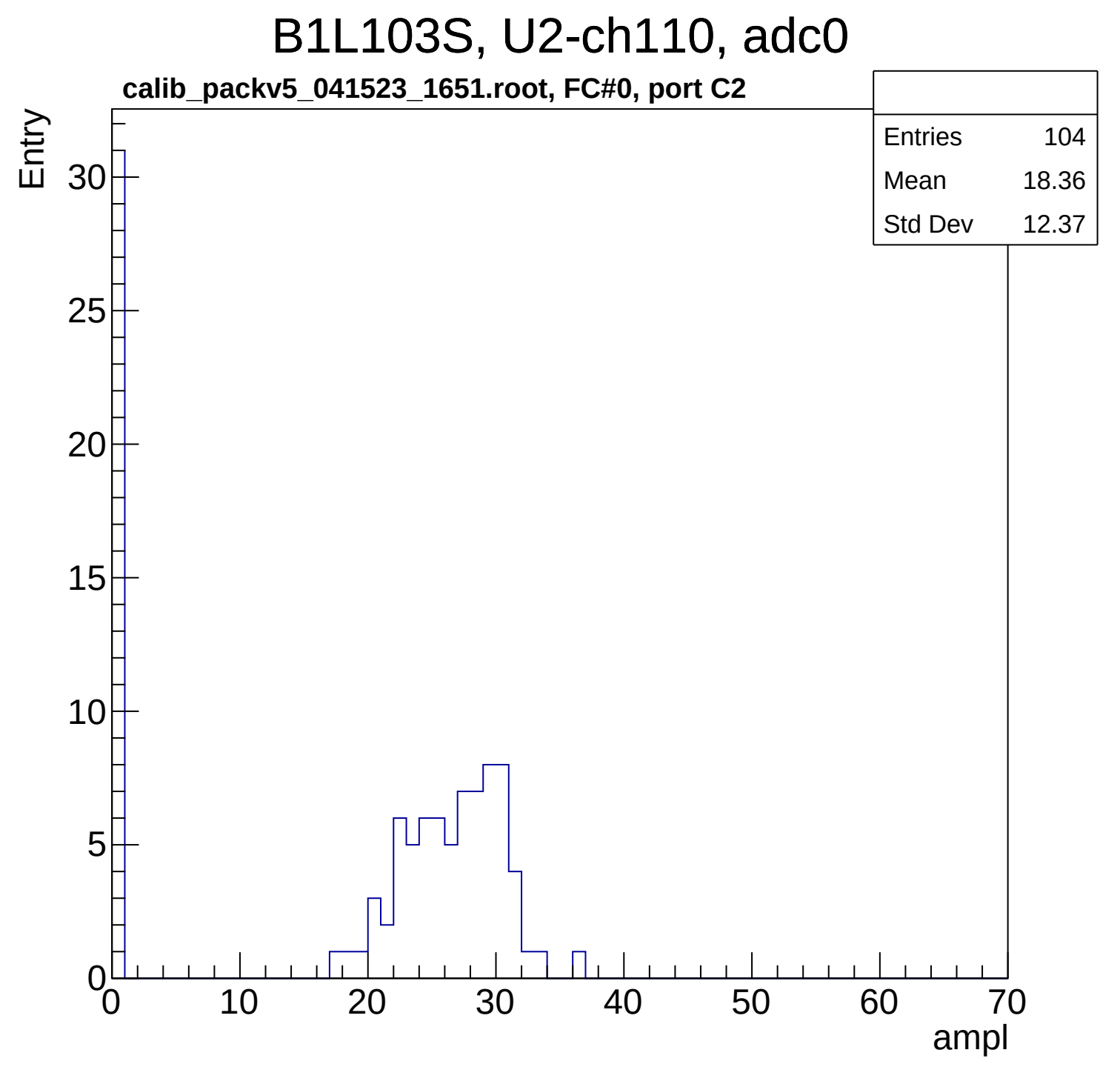

B1L103S, U2-ch109, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 46.72
Std Dev 6.73
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

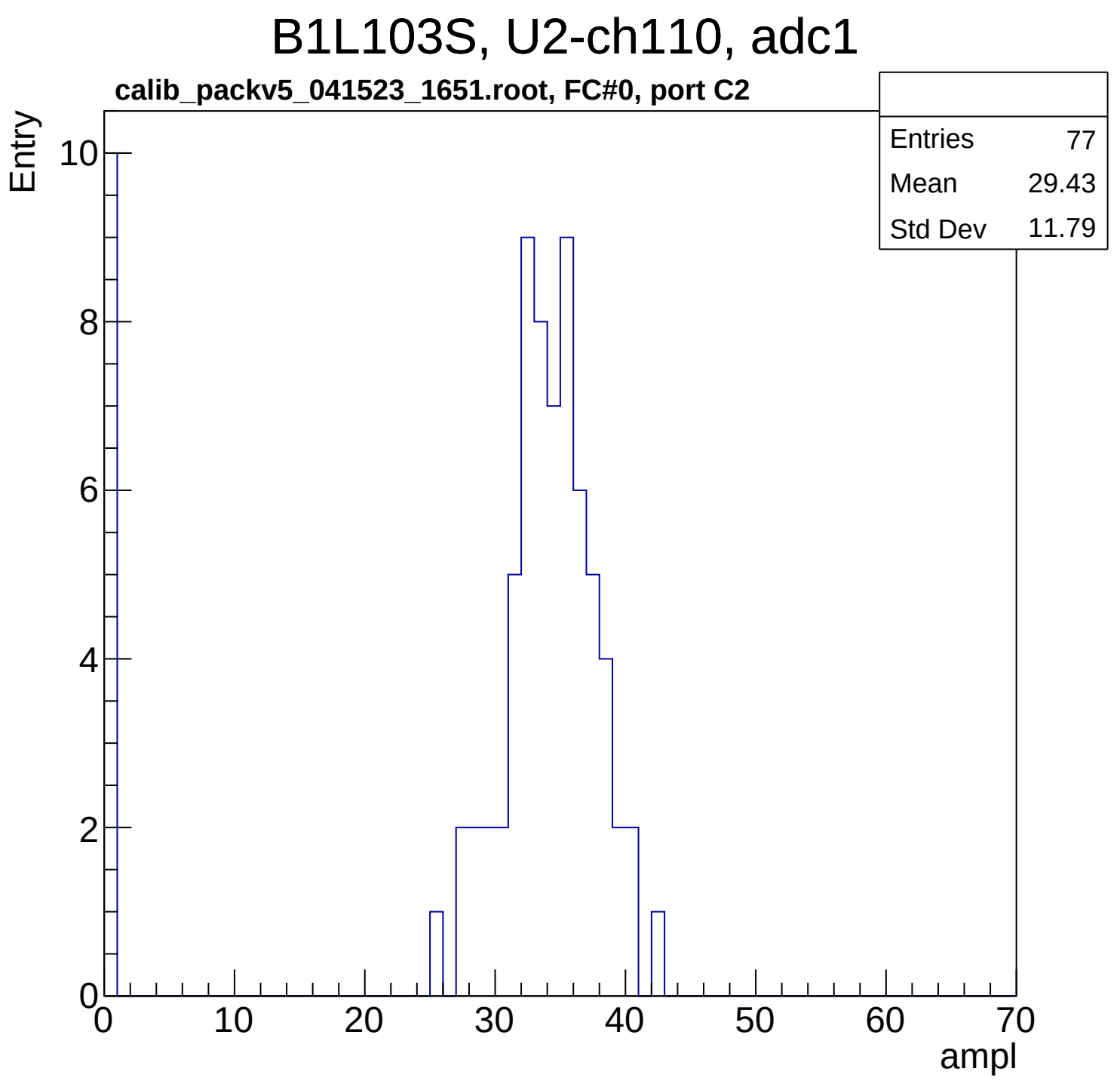

B1L103S, U2-ch109, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 53.4
Std Dev 2.817
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

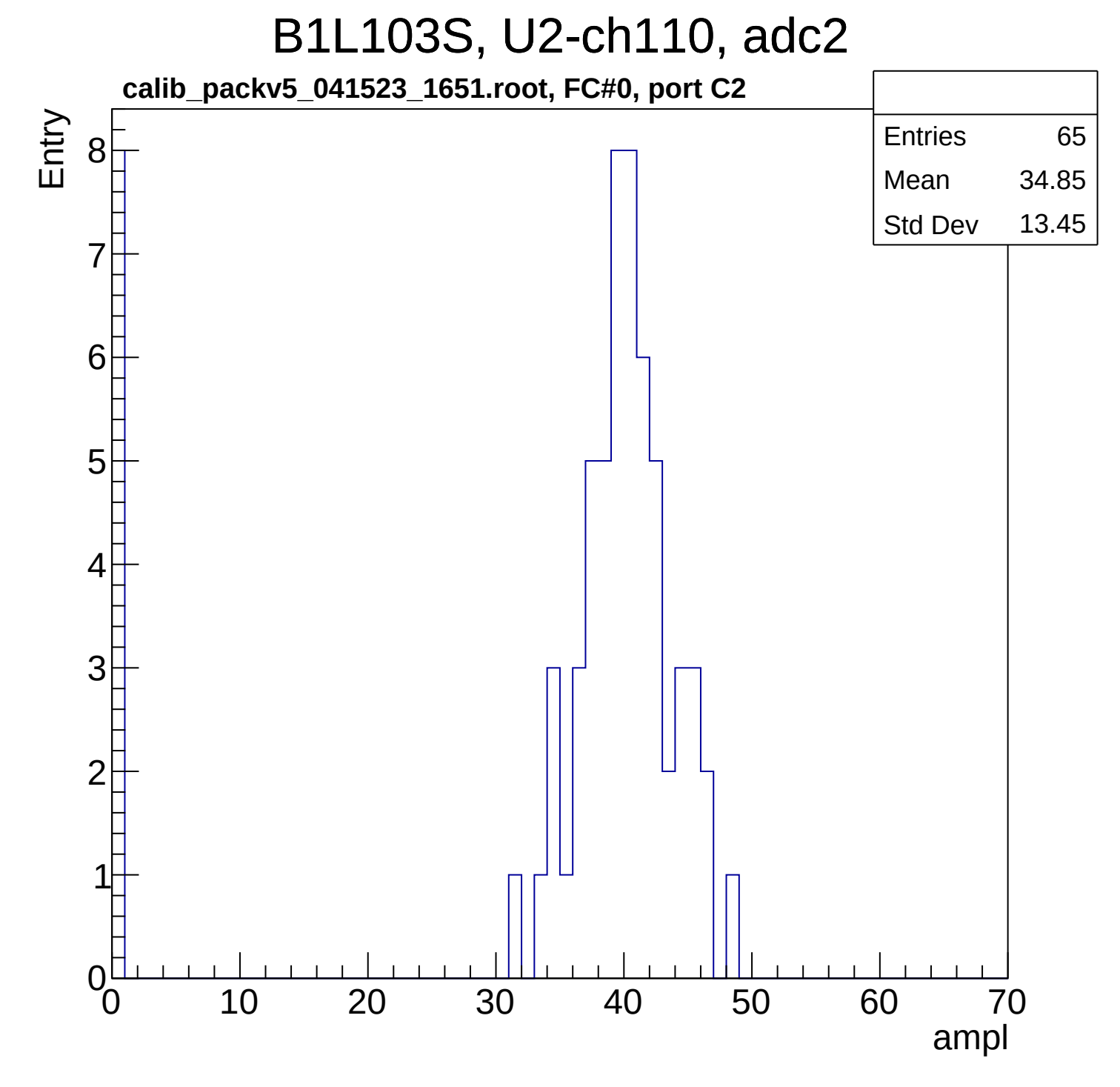

B1L103S, U2-ch109, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.83
Std Dev 2.805
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

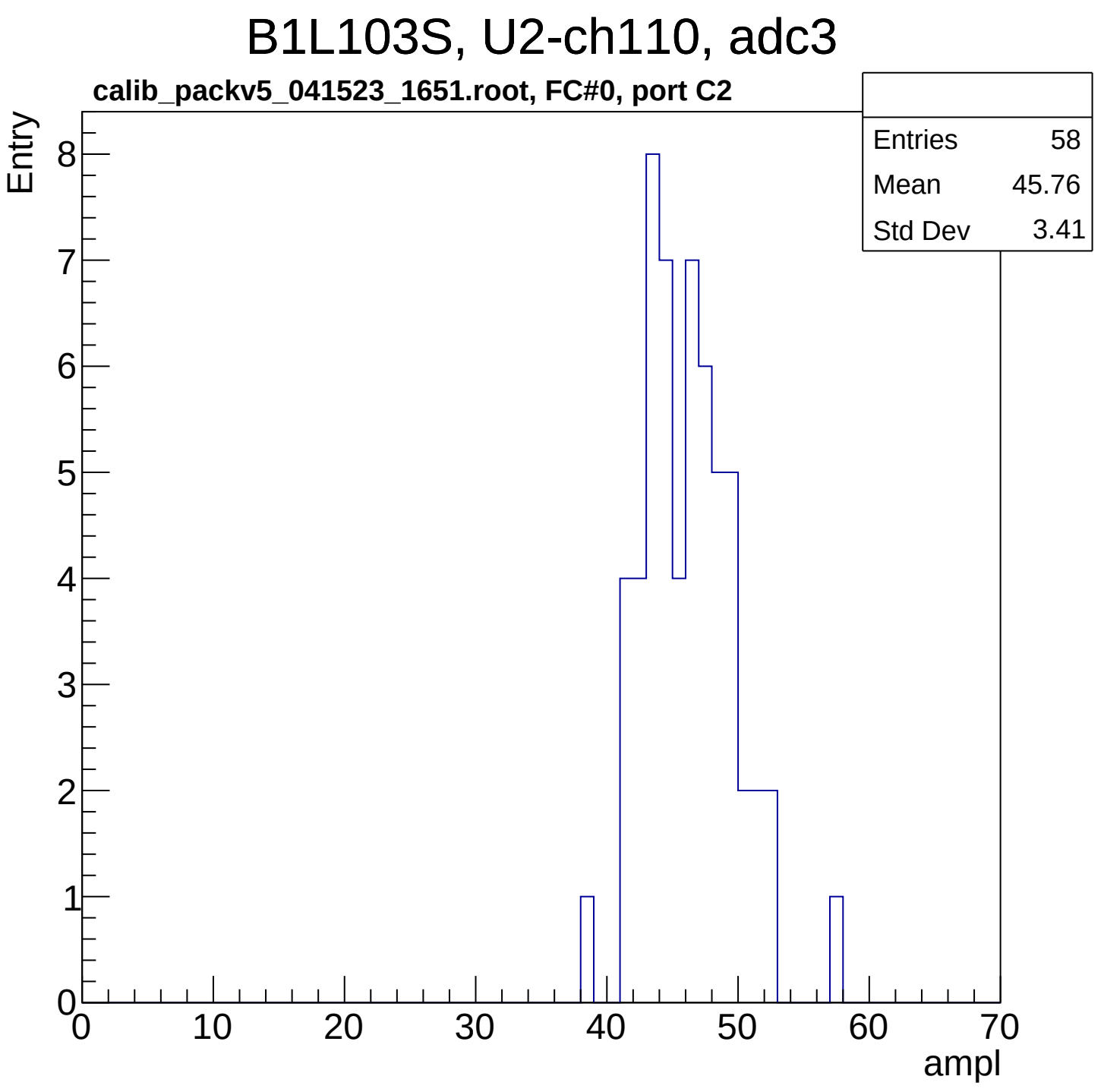

B1L103S, U2-ch109, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 17
Mean 61.12
Std Dev 1.45
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

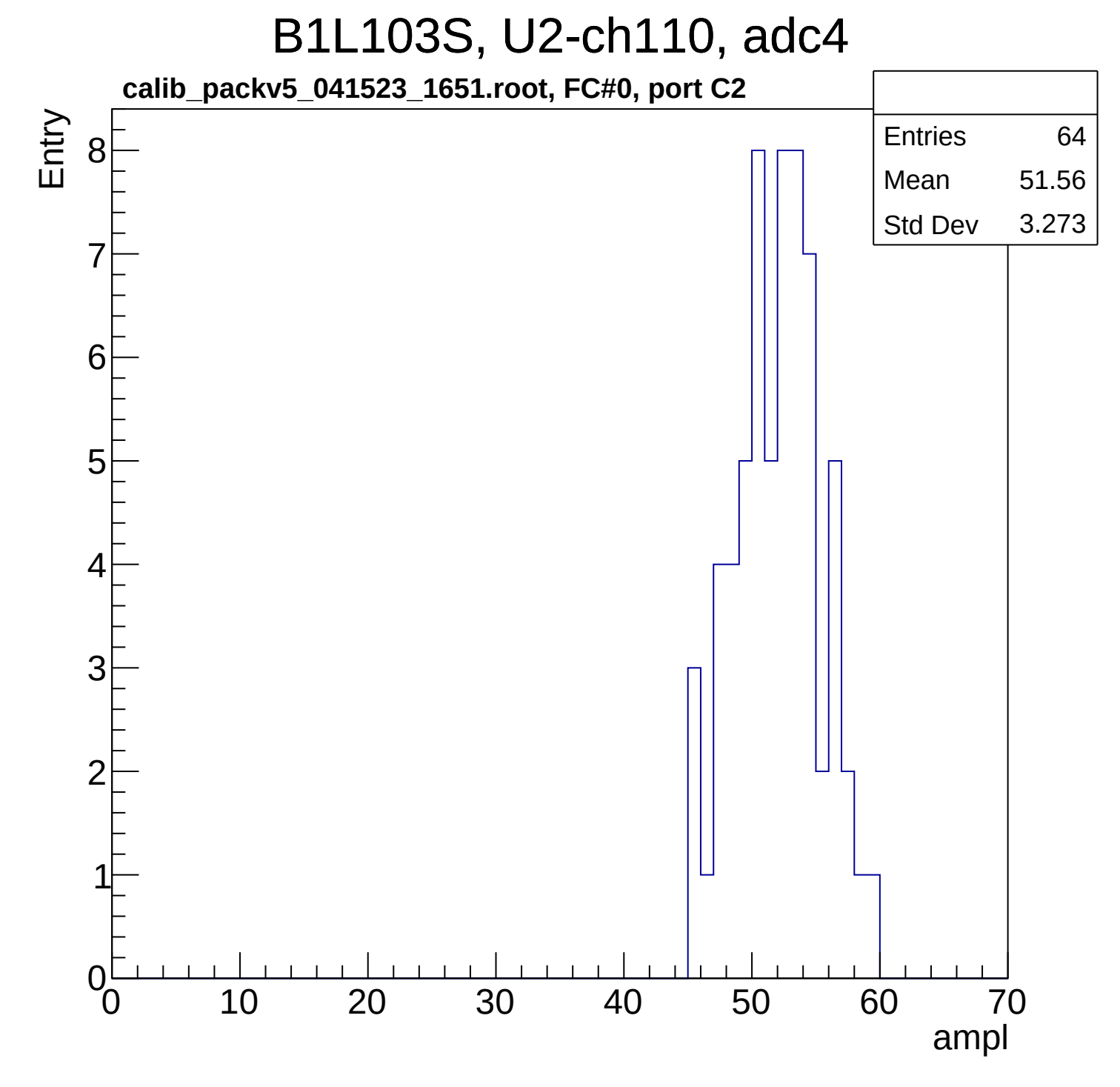

B1L103S, U2-ch109, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl

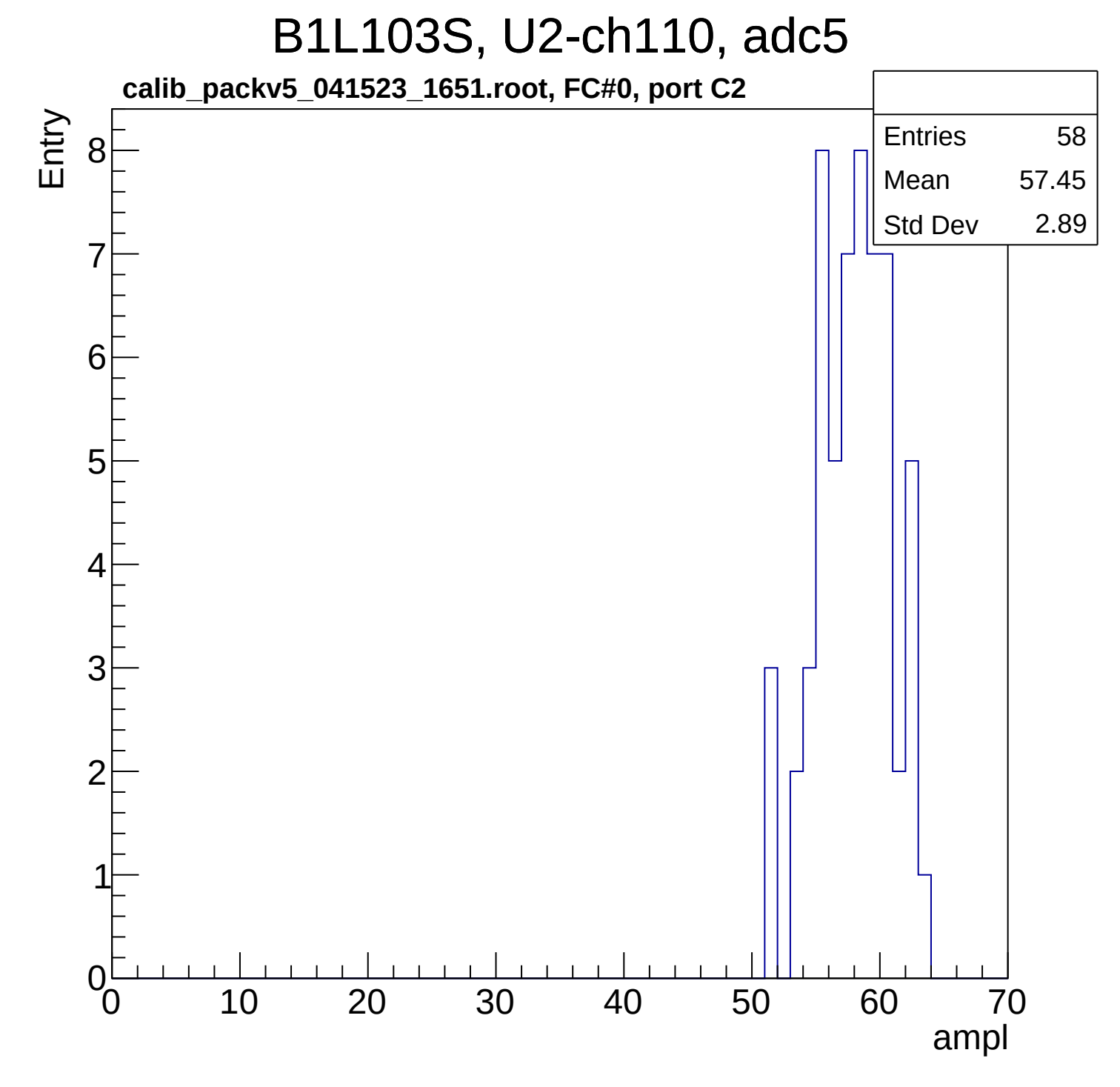

B1L103S, U2-ch110, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 18.36
Std Dev 12.37
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl

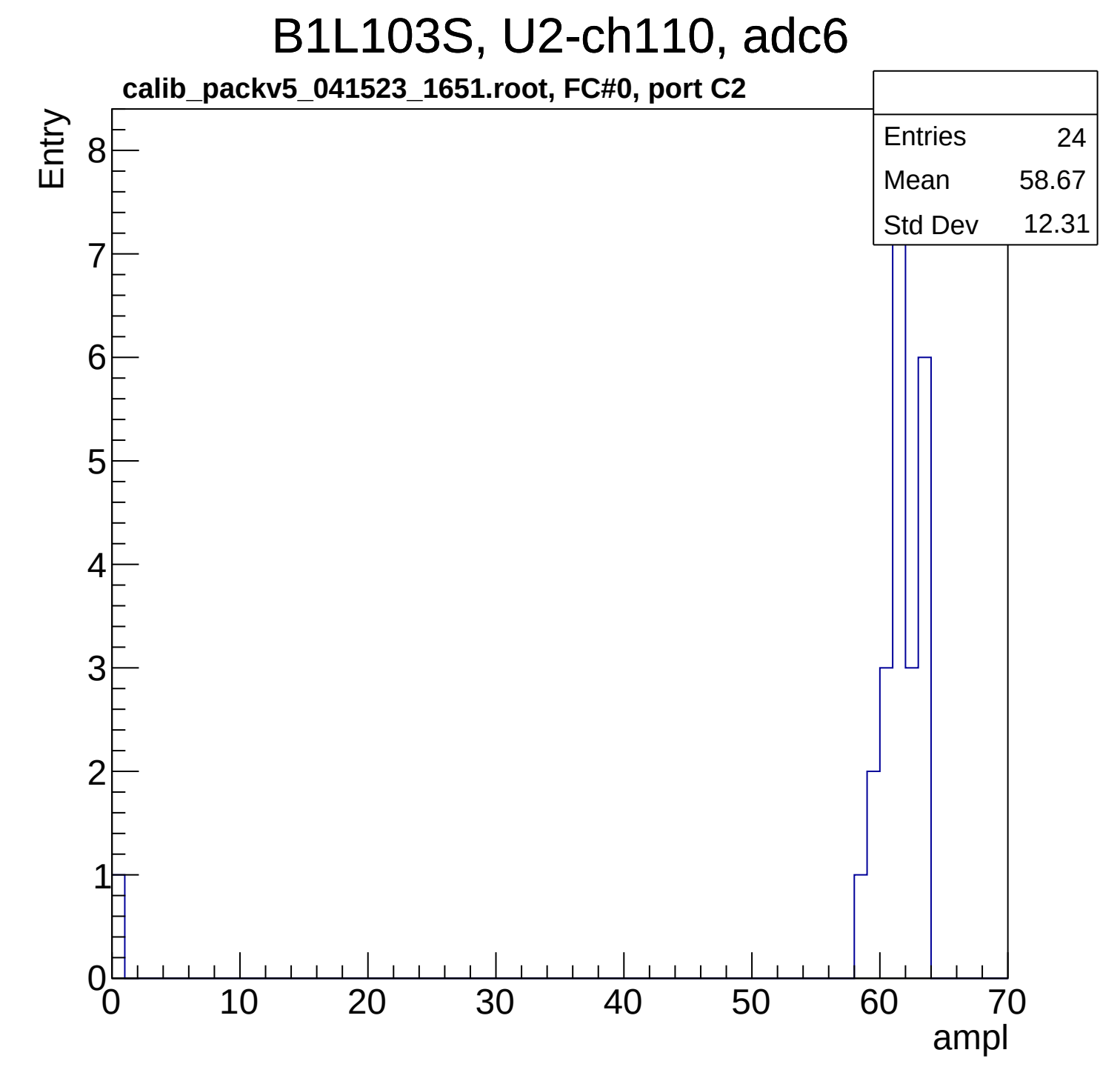

B1L103S, U2-ch110, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 29.43
Std Dev 11.79
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

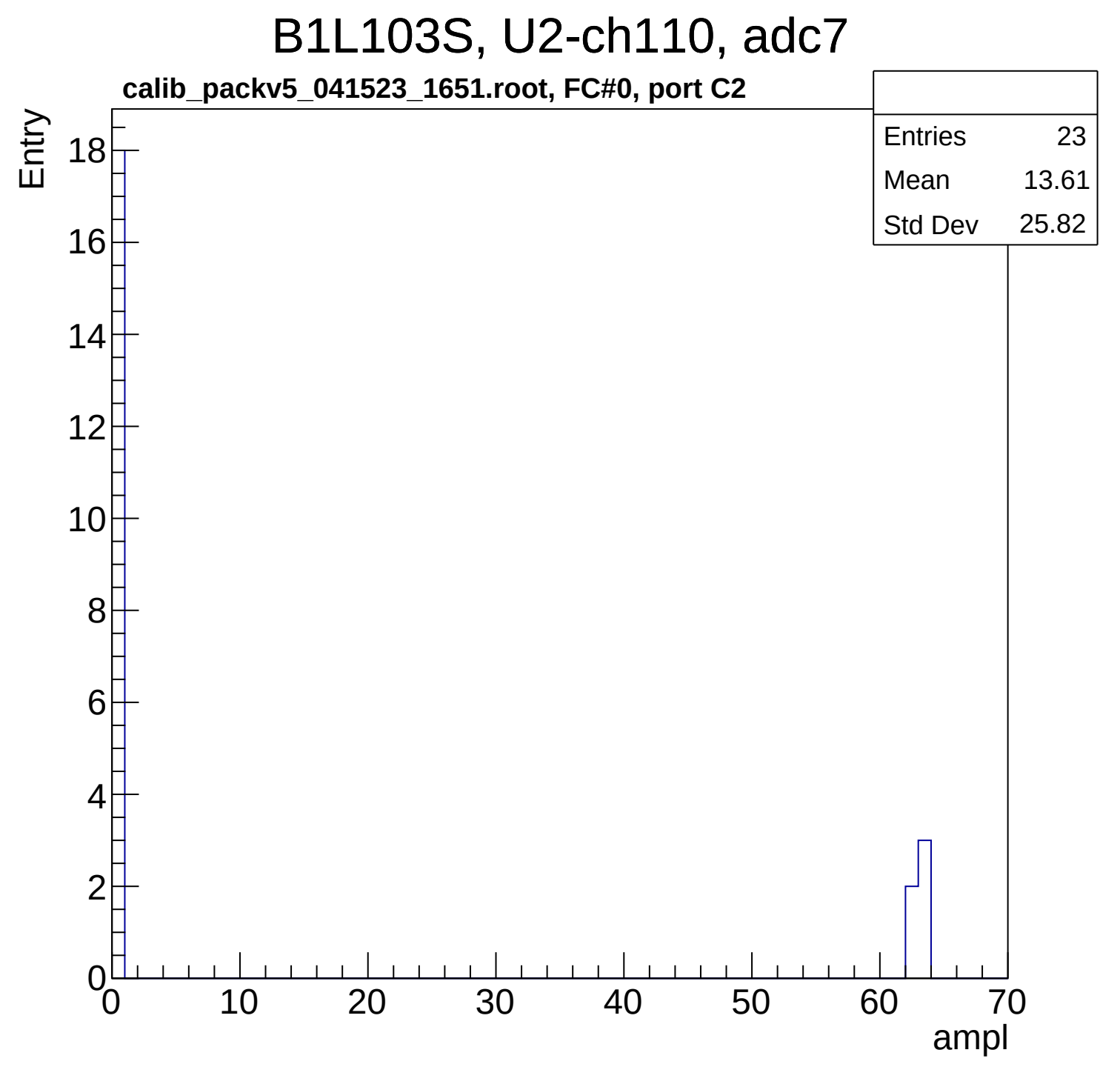

B1L103S, U2-ch110, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 34.85
Std Dev 13.45
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

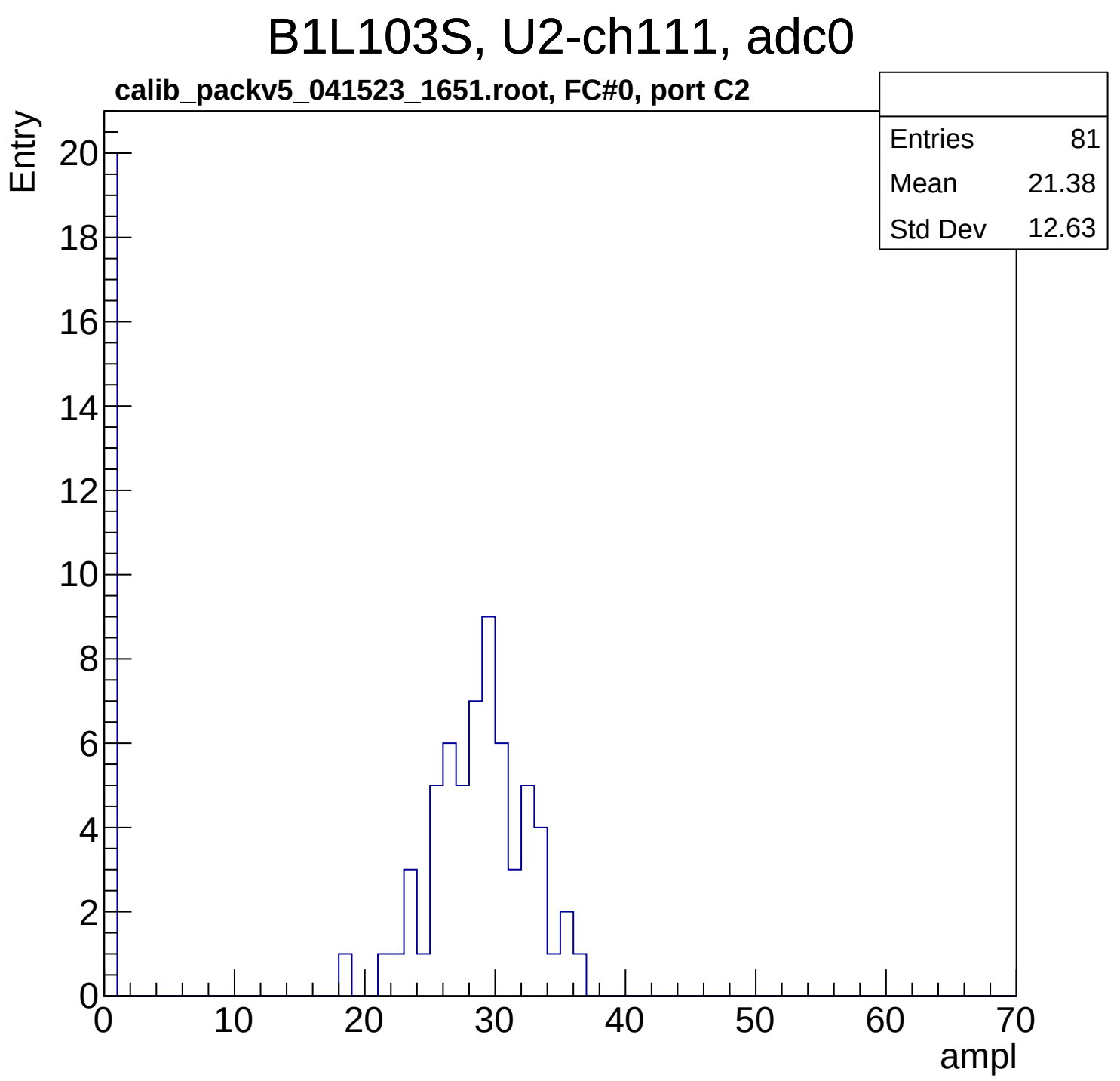

B1L103S, U2-ch110, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 45.76
Std Dev 3.41
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

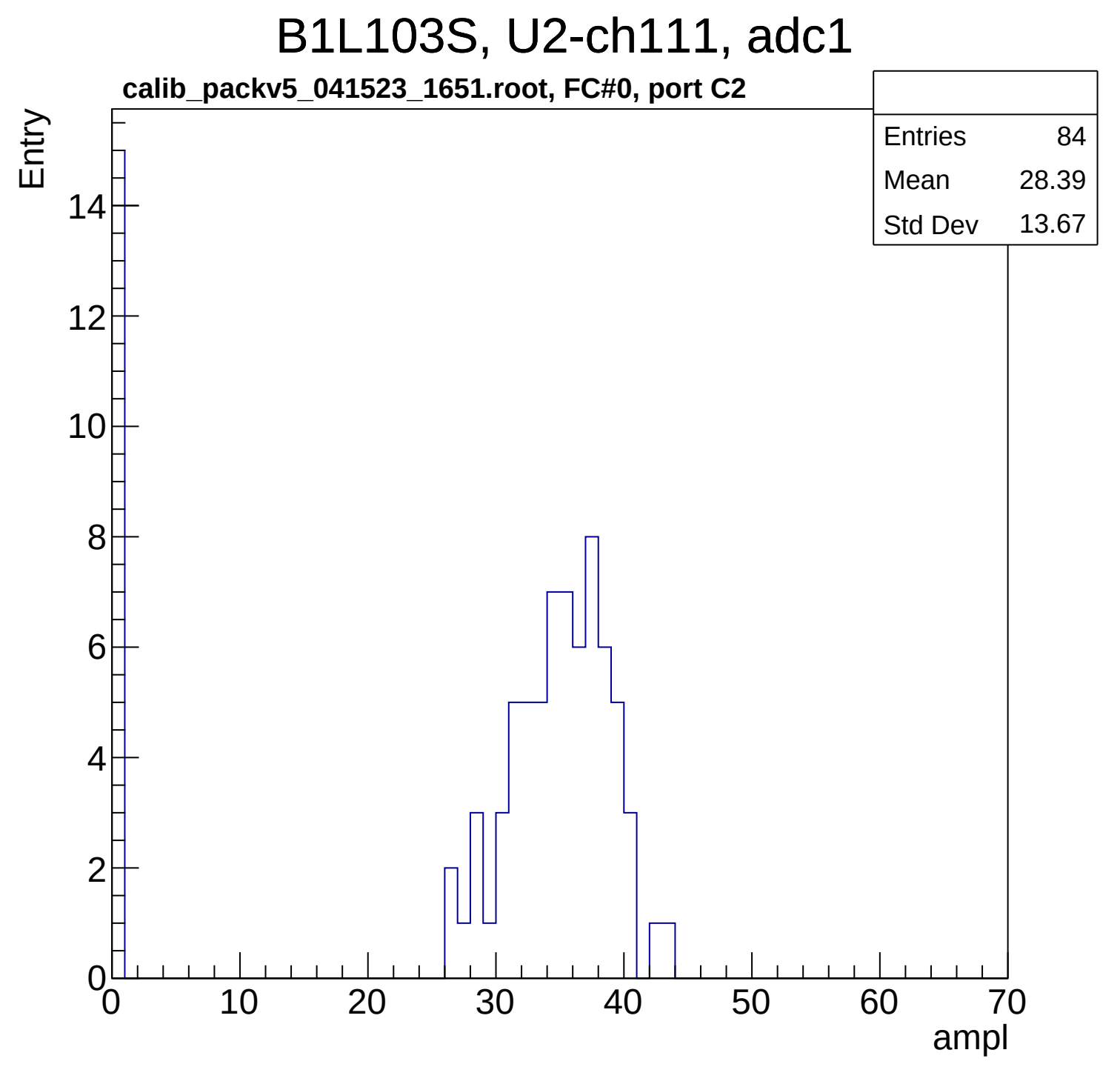

B1L103S, U2-ch110, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 51.56
Std Dev 3.273
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

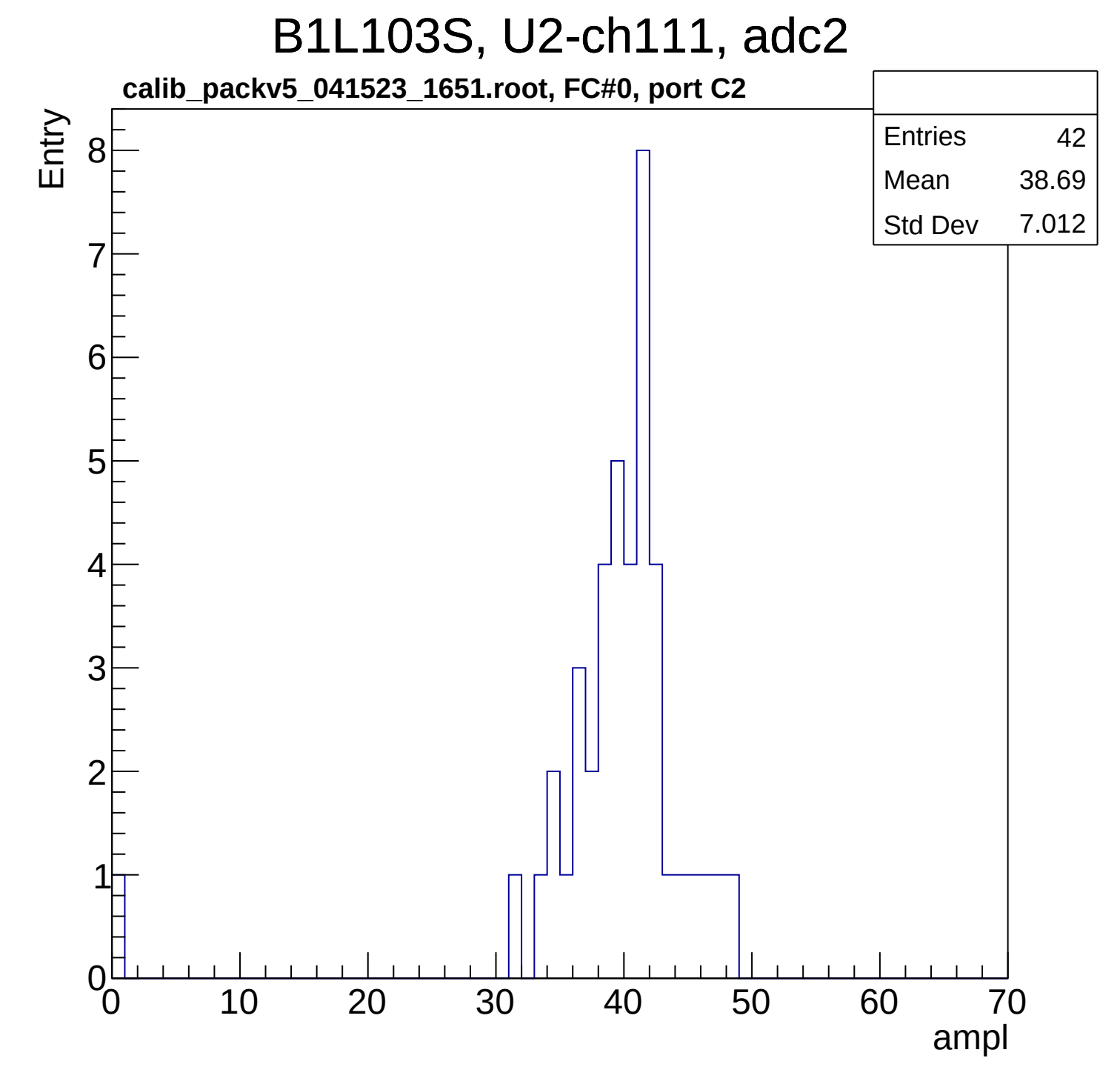

B1L103S, U2-ch110, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 57.45
Std Dev 2.89
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

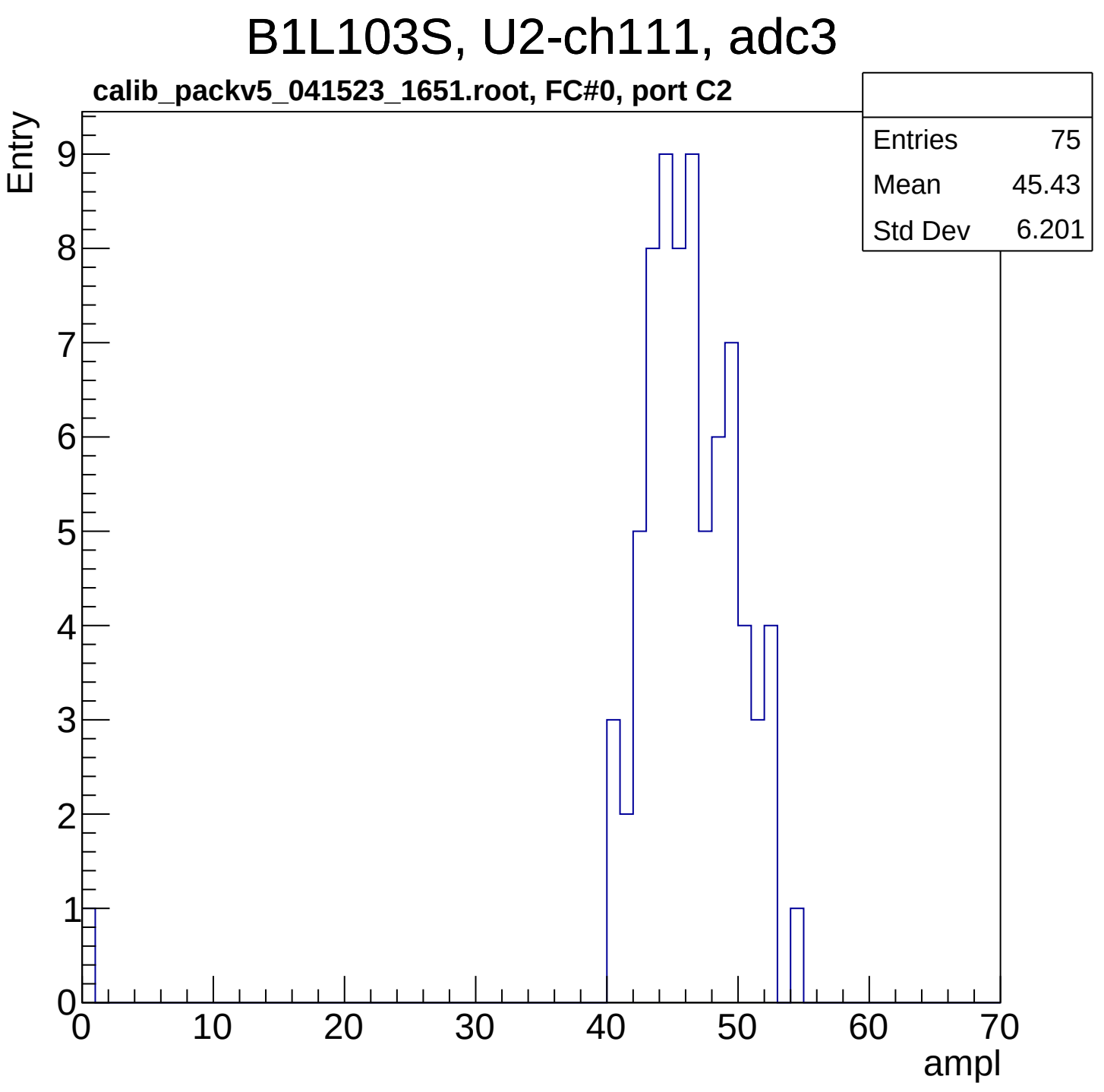

B1L103S, U2-ch110, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 58.67
Std Dev 12.31
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

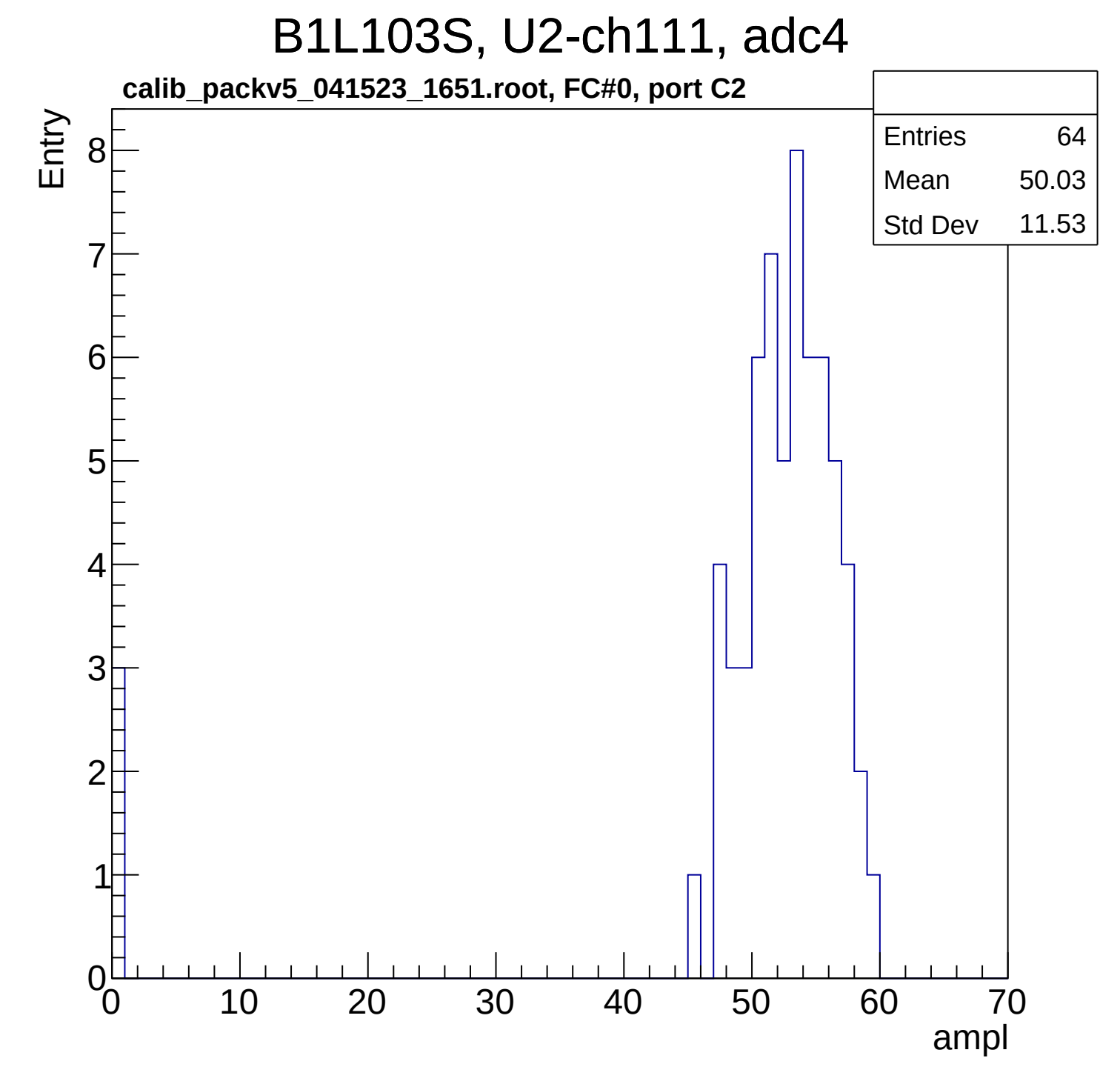

B1L103S, U2-ch110, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 13.61
Std Dev 25.82
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

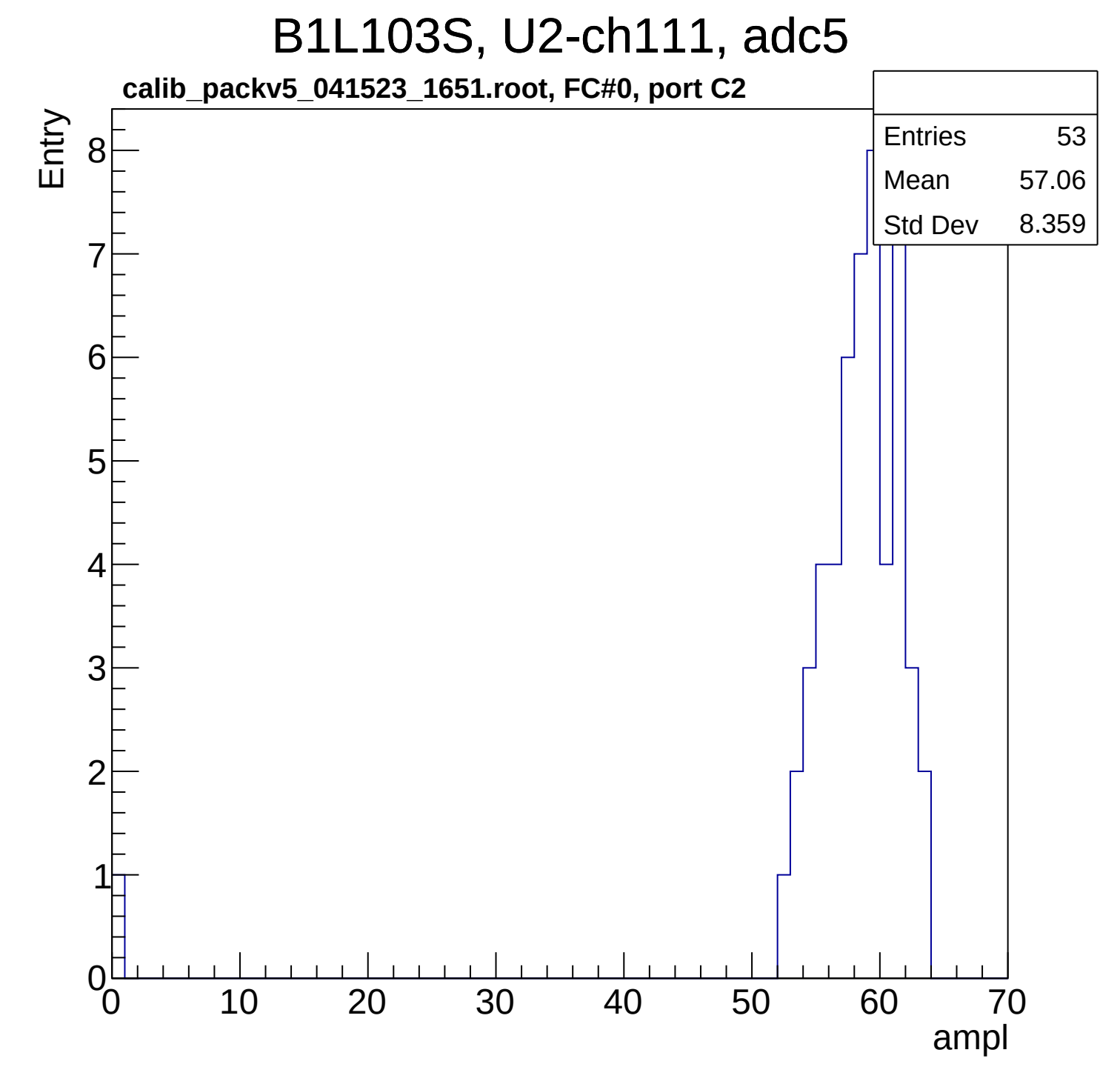

B1L103S, U2-ch111, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 21.38
Std Dev 12.63
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl

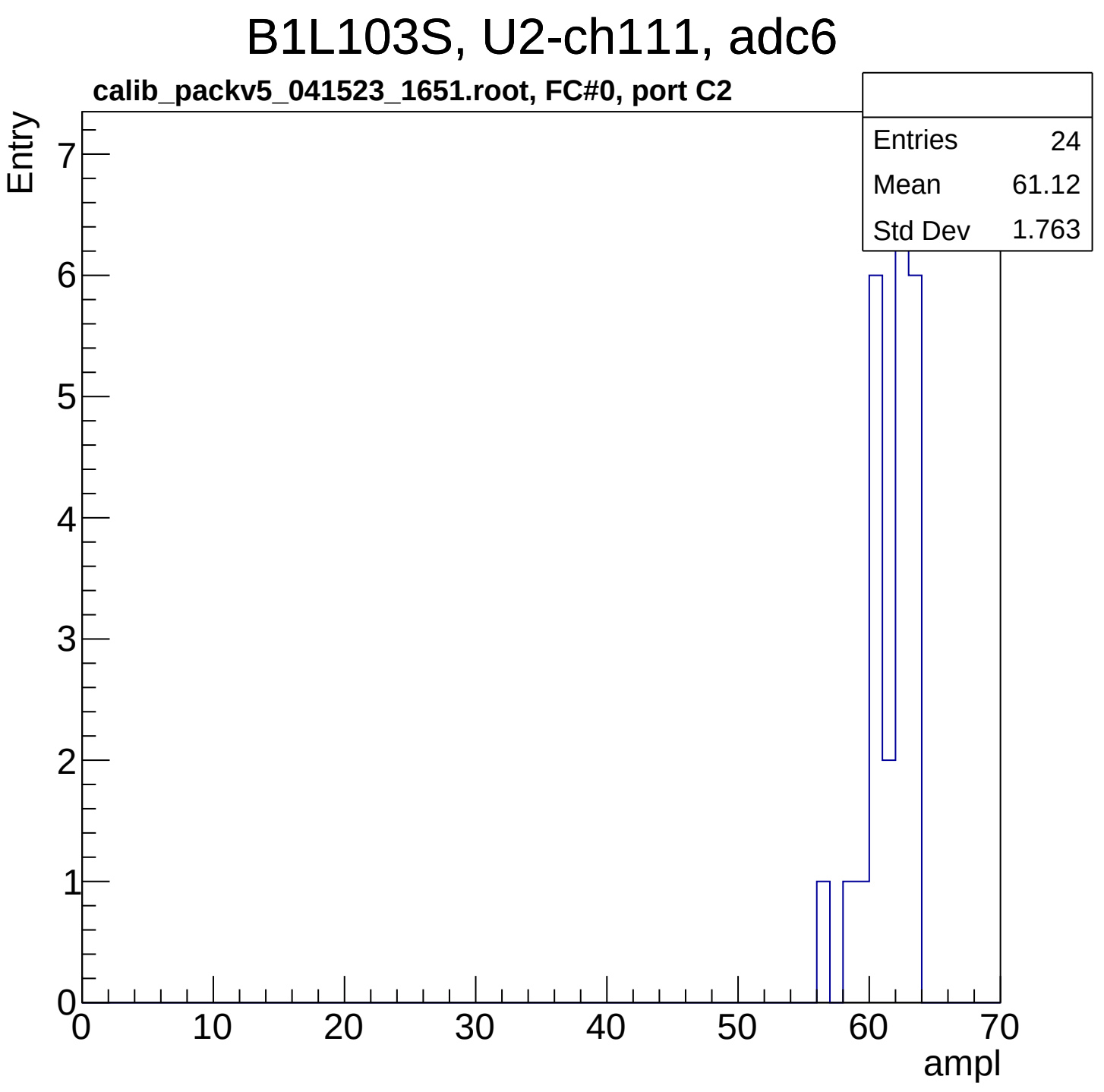

B1L103S, U2-ch111, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 28.39
Std Dev 13.67
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

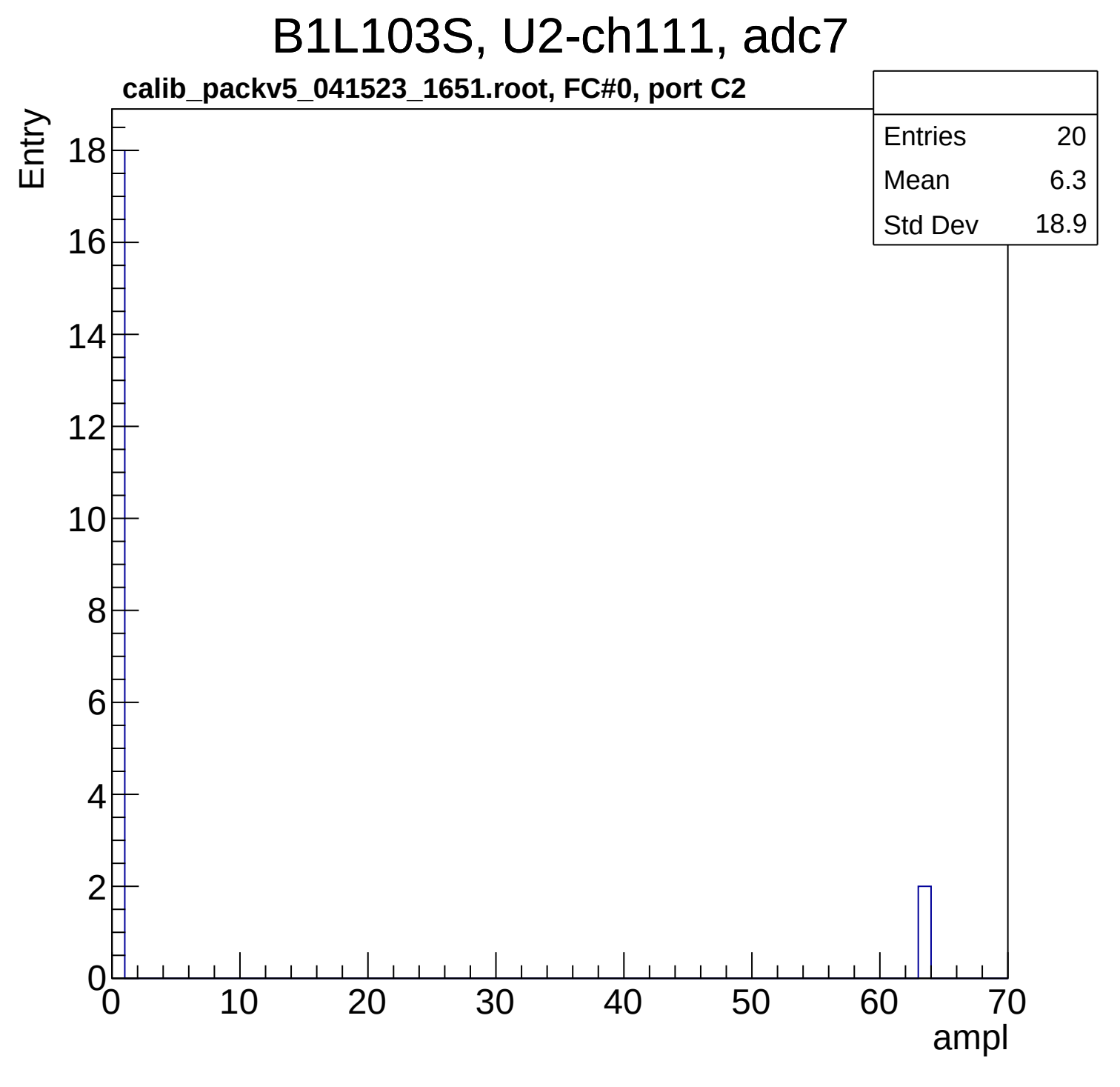

B1L103S, U2-ch111, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 38.69
Std Dev 7.012
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

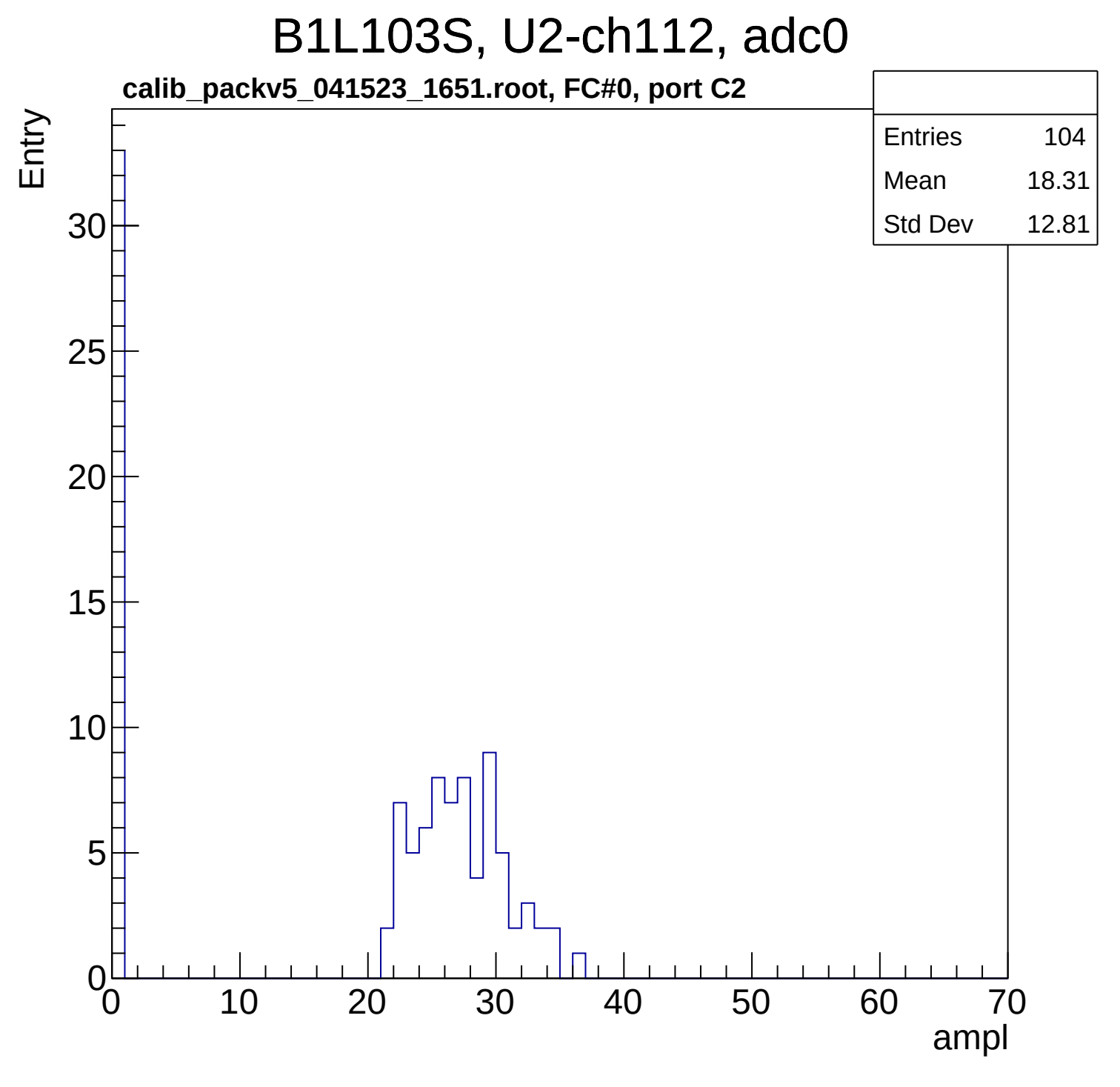

B1L103S, U2-ch111, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 45.43
Std Dev 6.201
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

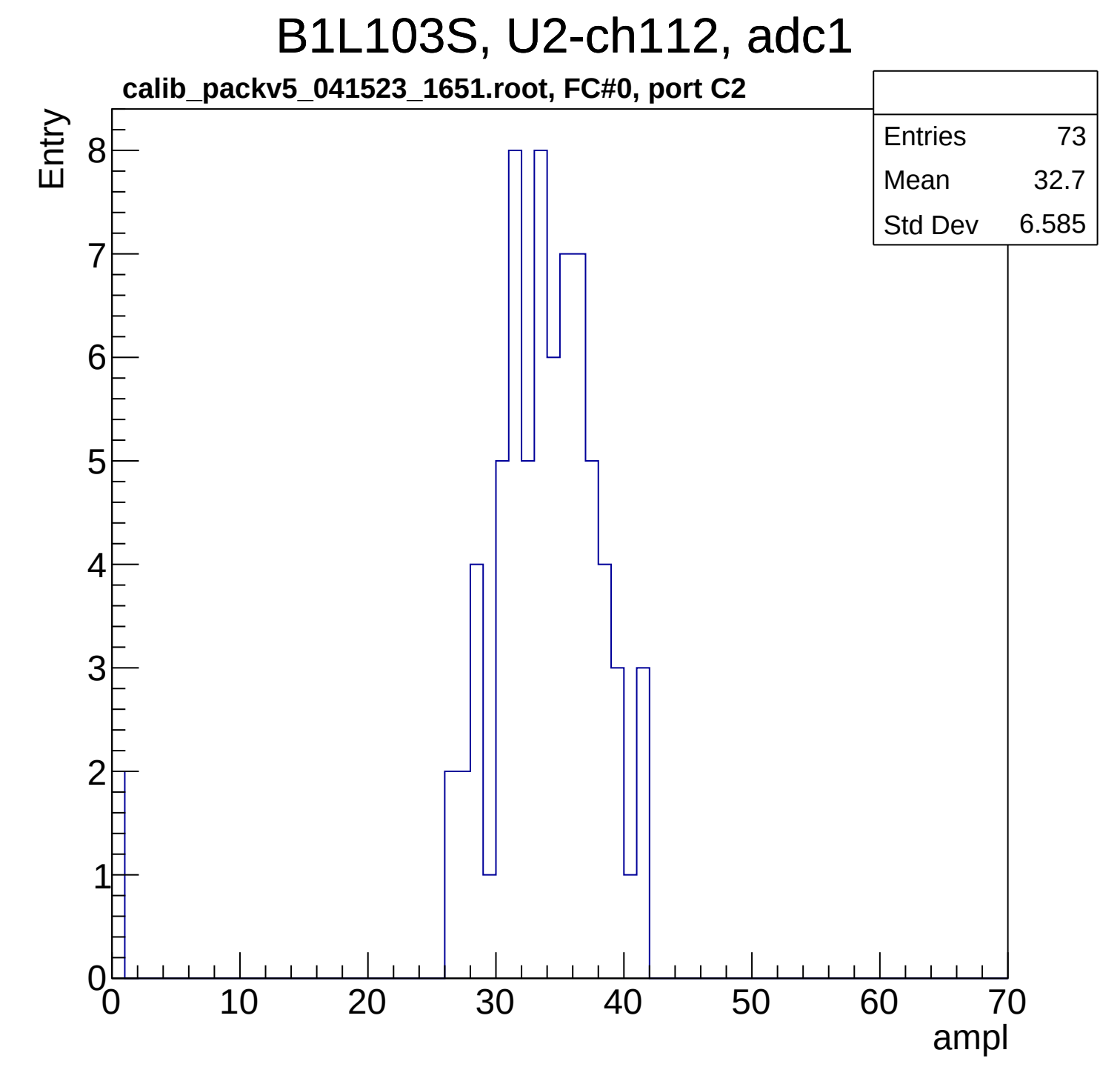

B1L103S, U2-ch111, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 50.03
Std Dev 11.53
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

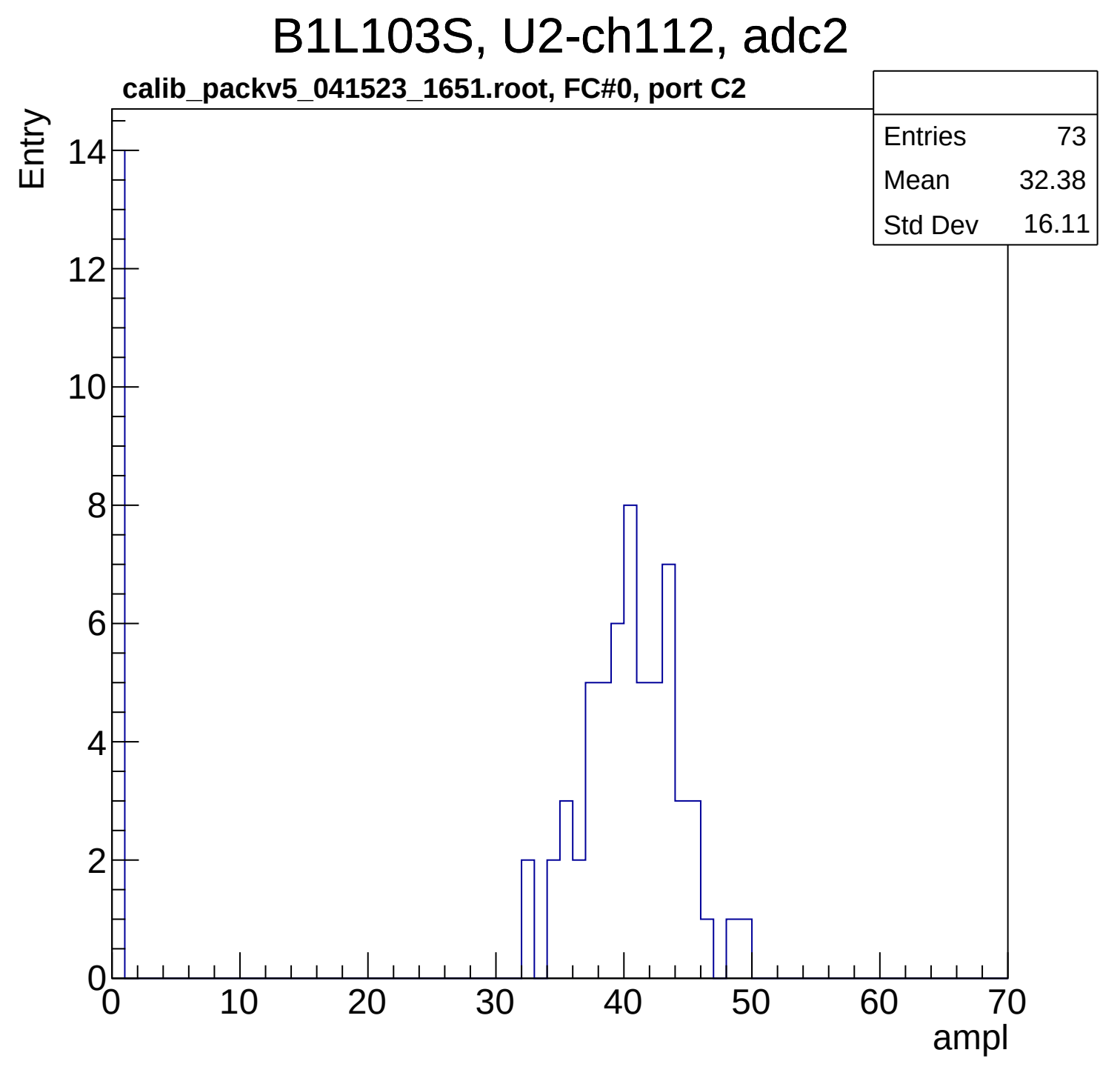

B1L103S, U2-ch111, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 57.06
Std Dev 8.359
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

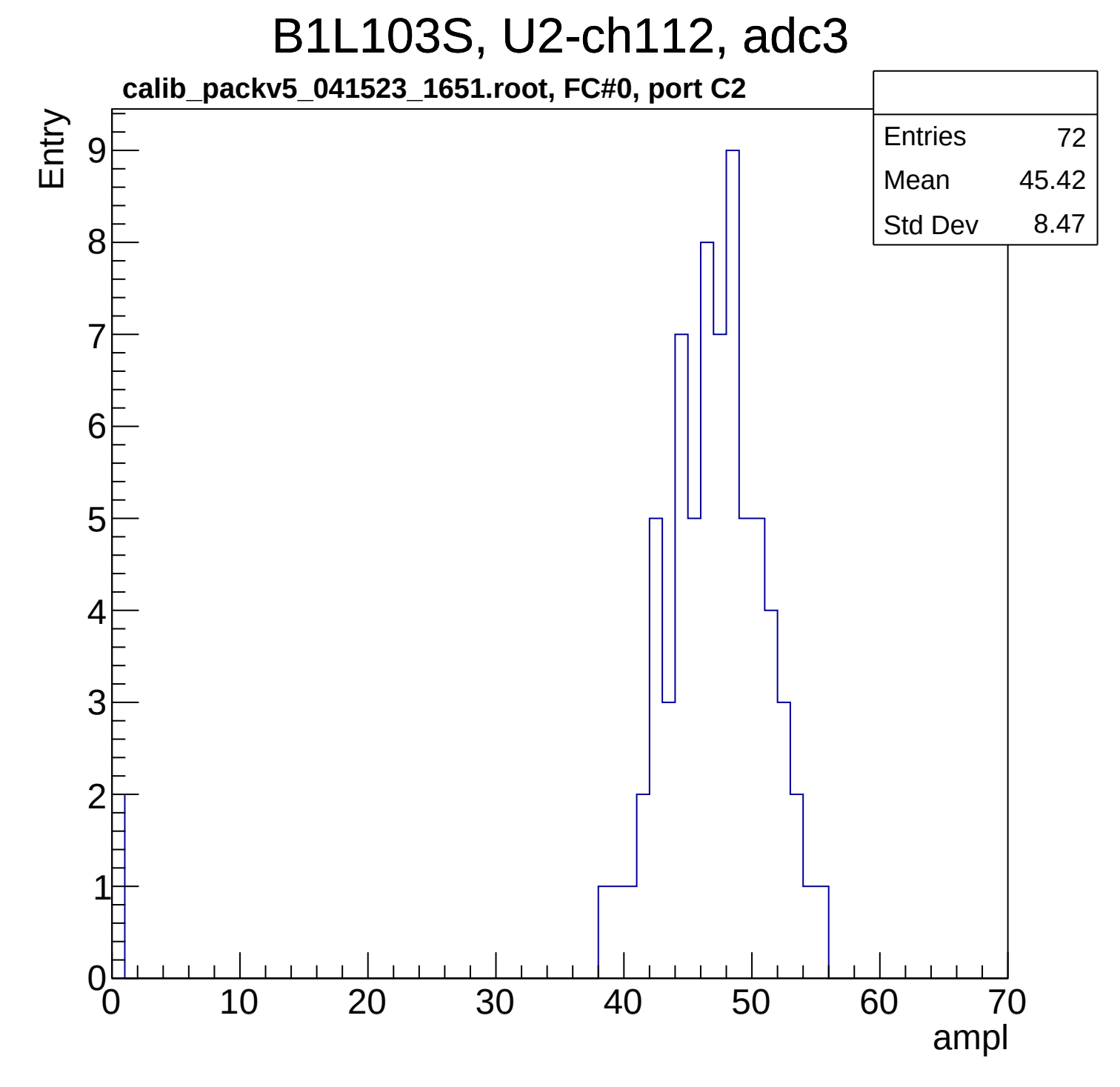

B1L103S, U2-ch111, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 61.12
Std Dev 1.763
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

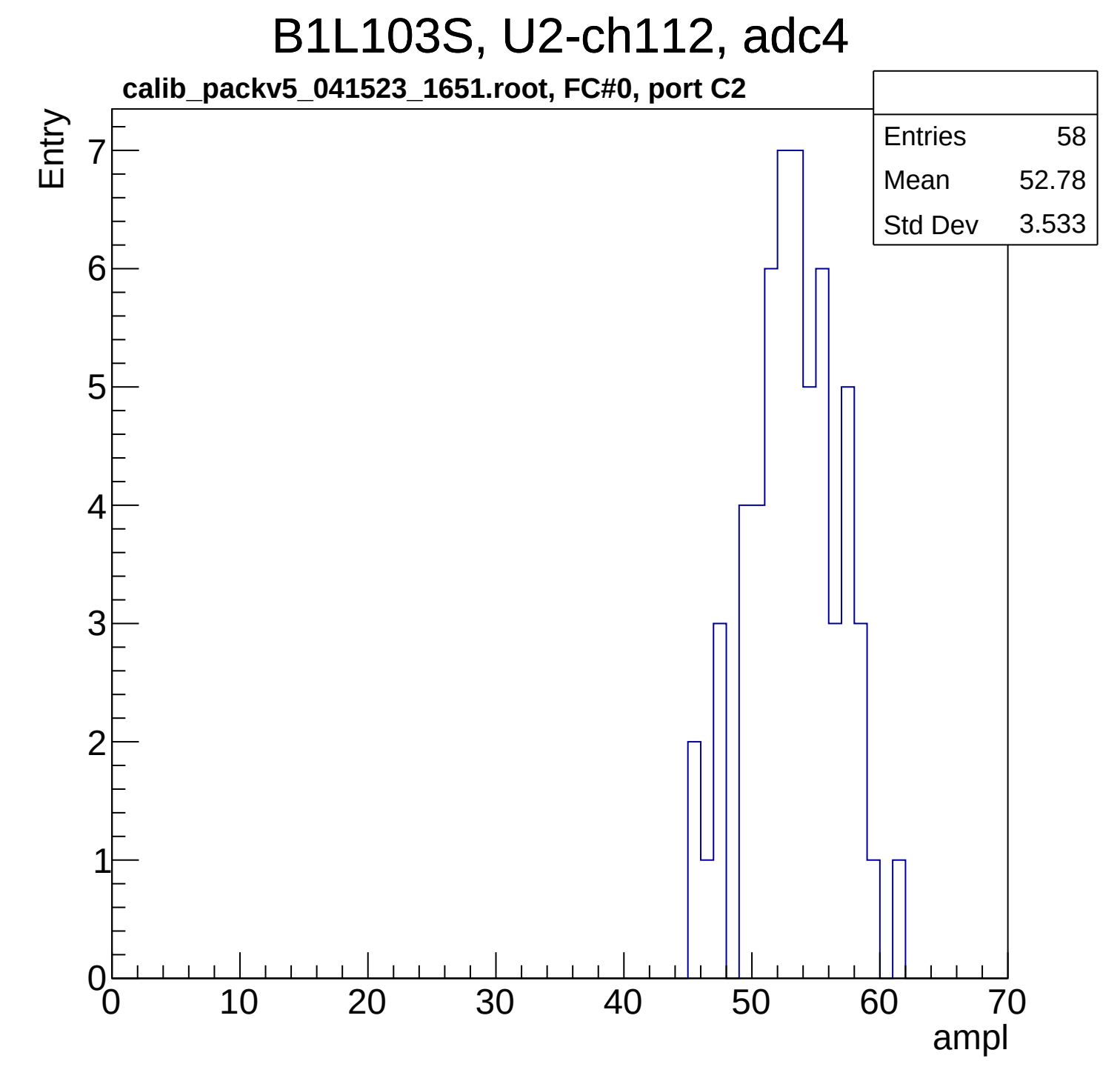

B1L103S, U2-ch111, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.3
Std Dev 18.9
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

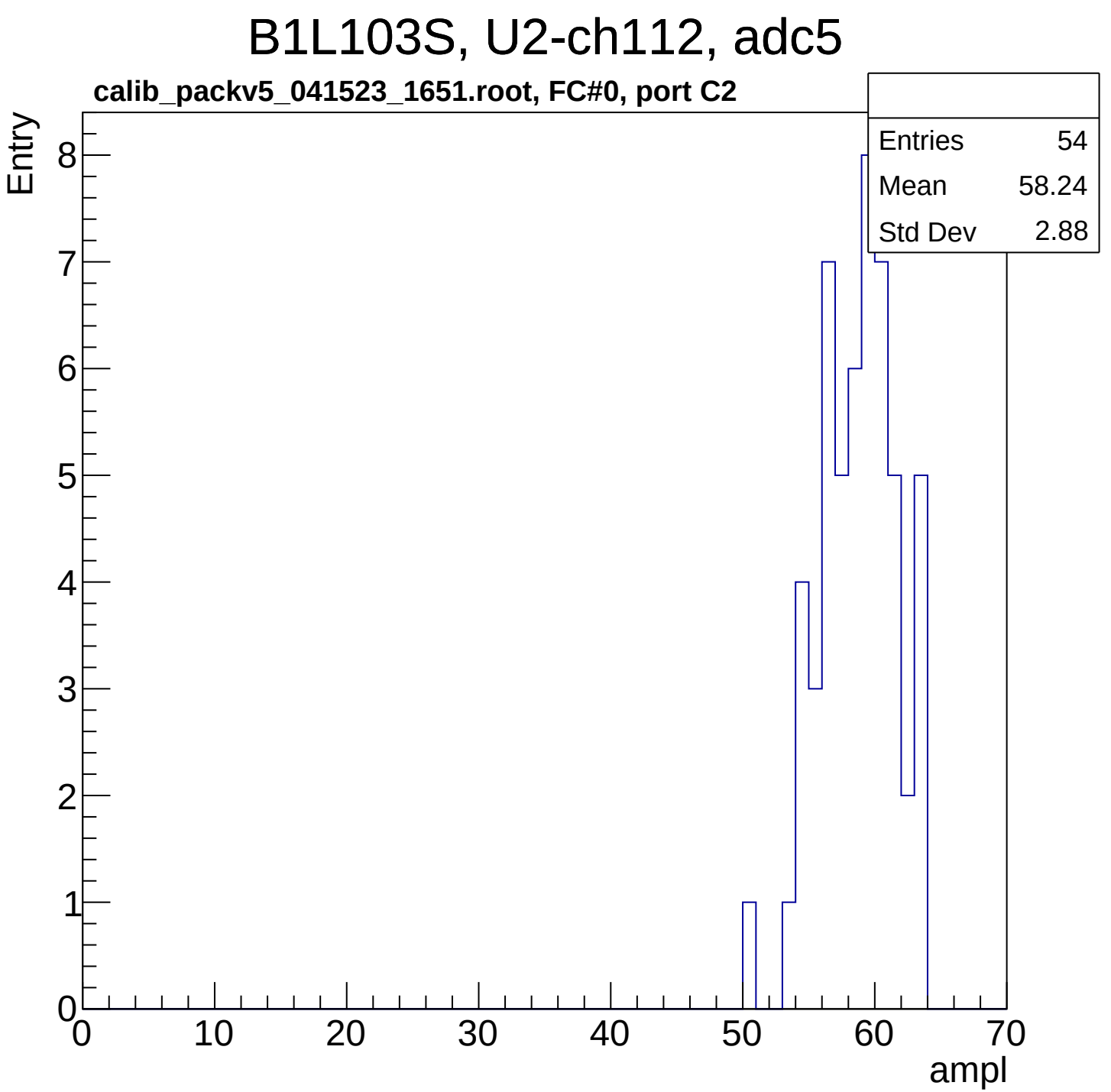

B1L103S, U2-ch112, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 18.31
Std Dev 12.81
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl

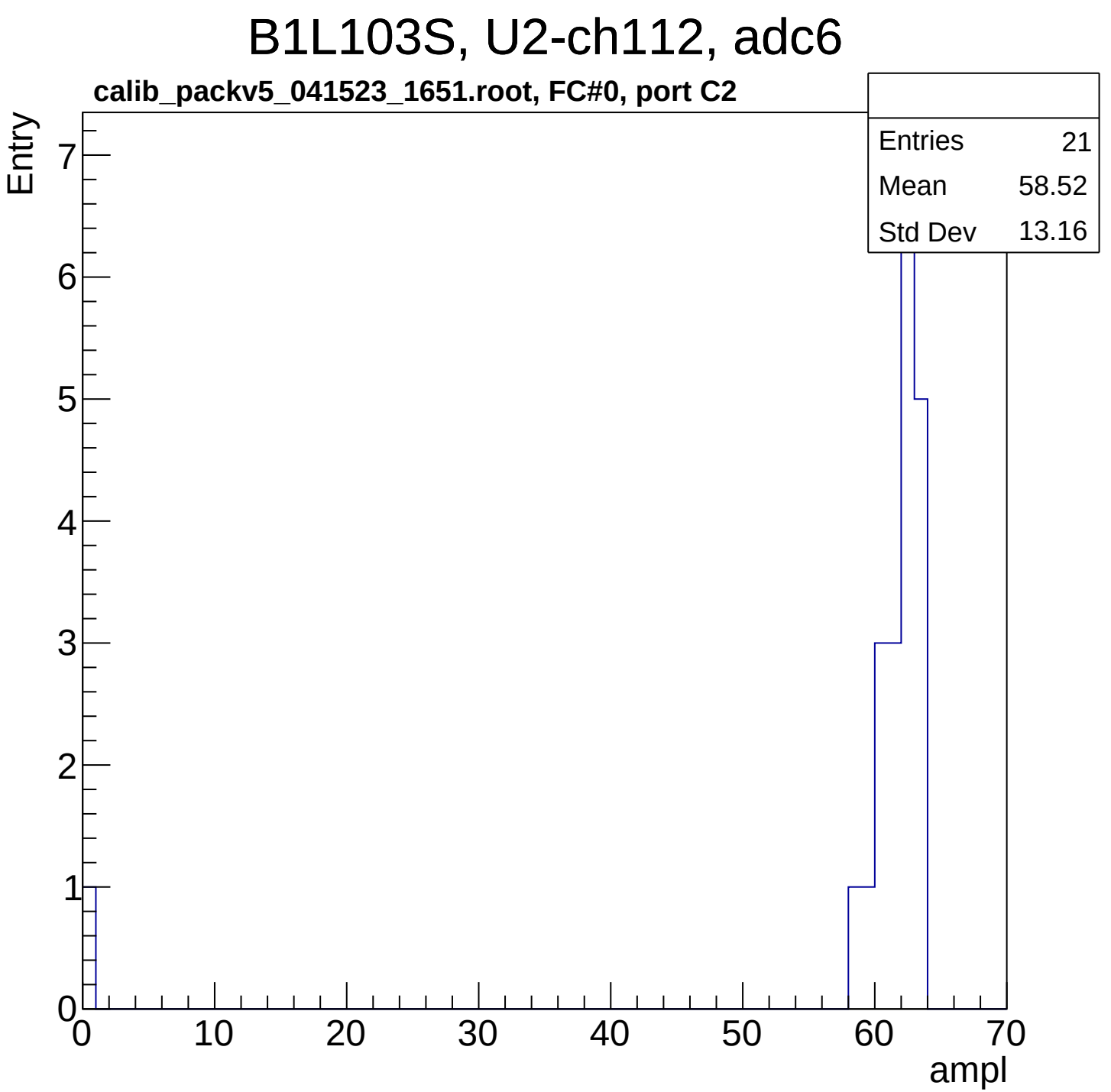

B1L103S, U2-ch112, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 32.7
Std Dev 6.585
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

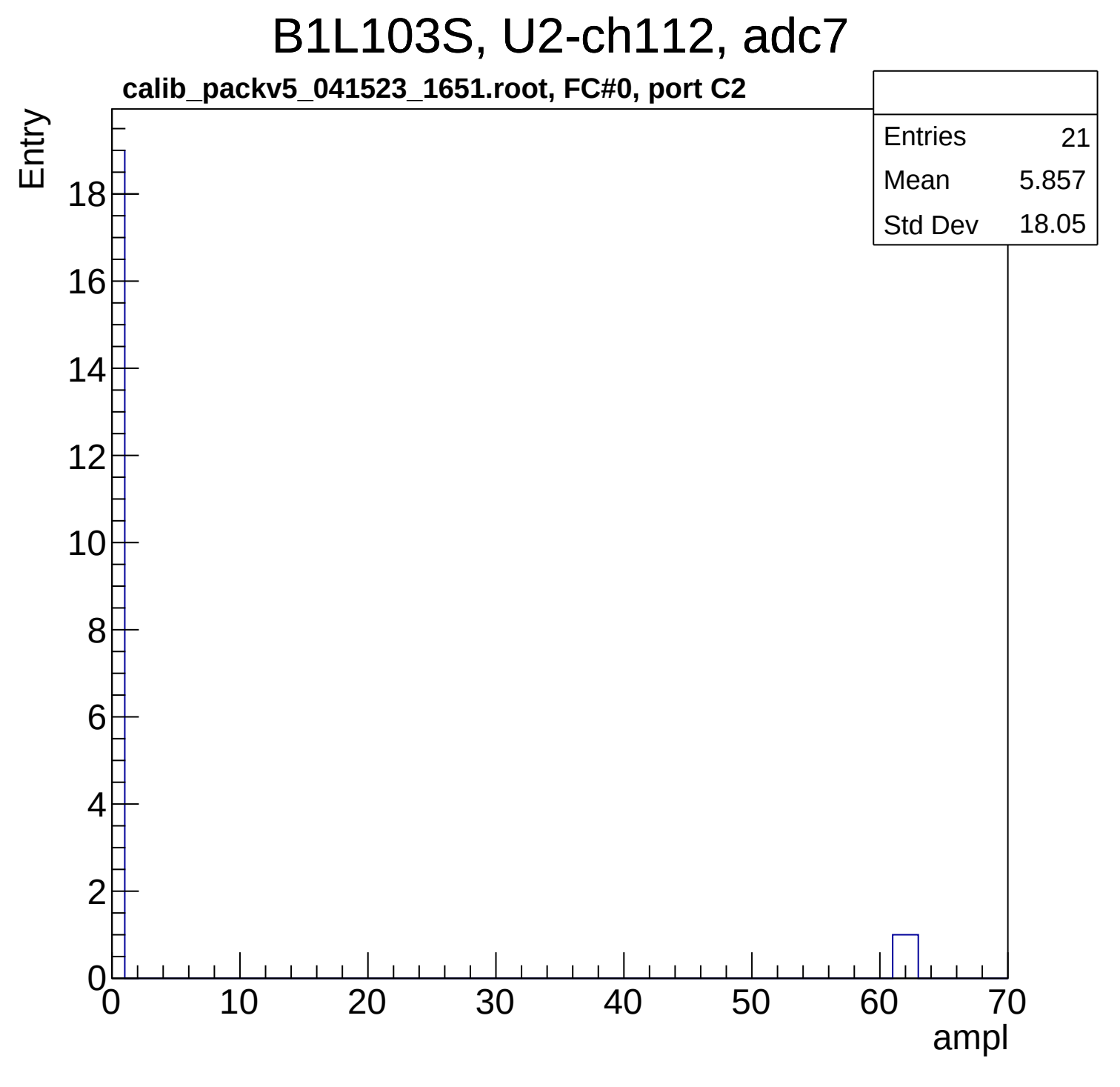

B1L103S, U2-ch112, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 32.38
Std Dev 16.11
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

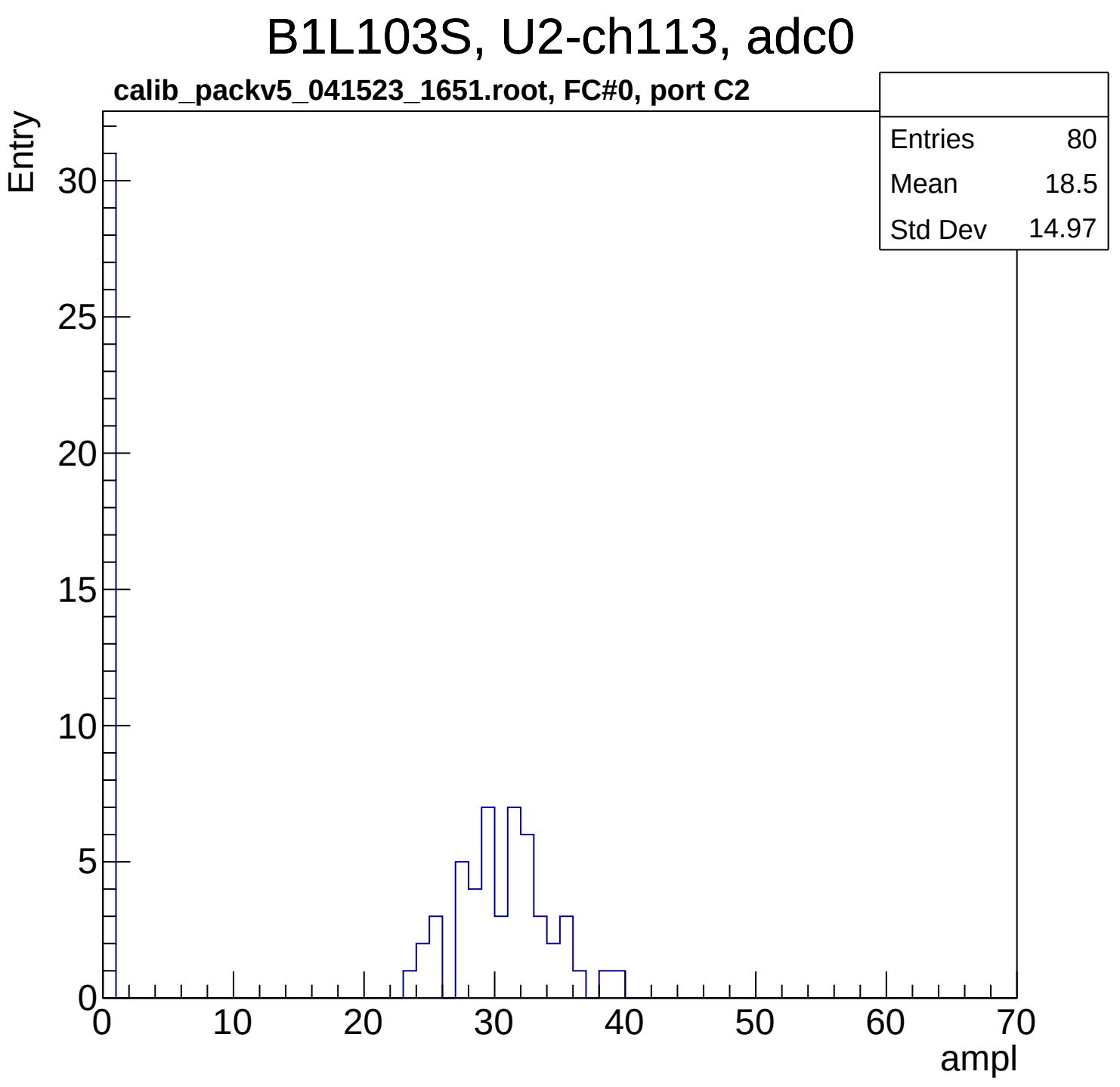

B1L103S, U2-ch112, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 45.42
Std Dev 8.47
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

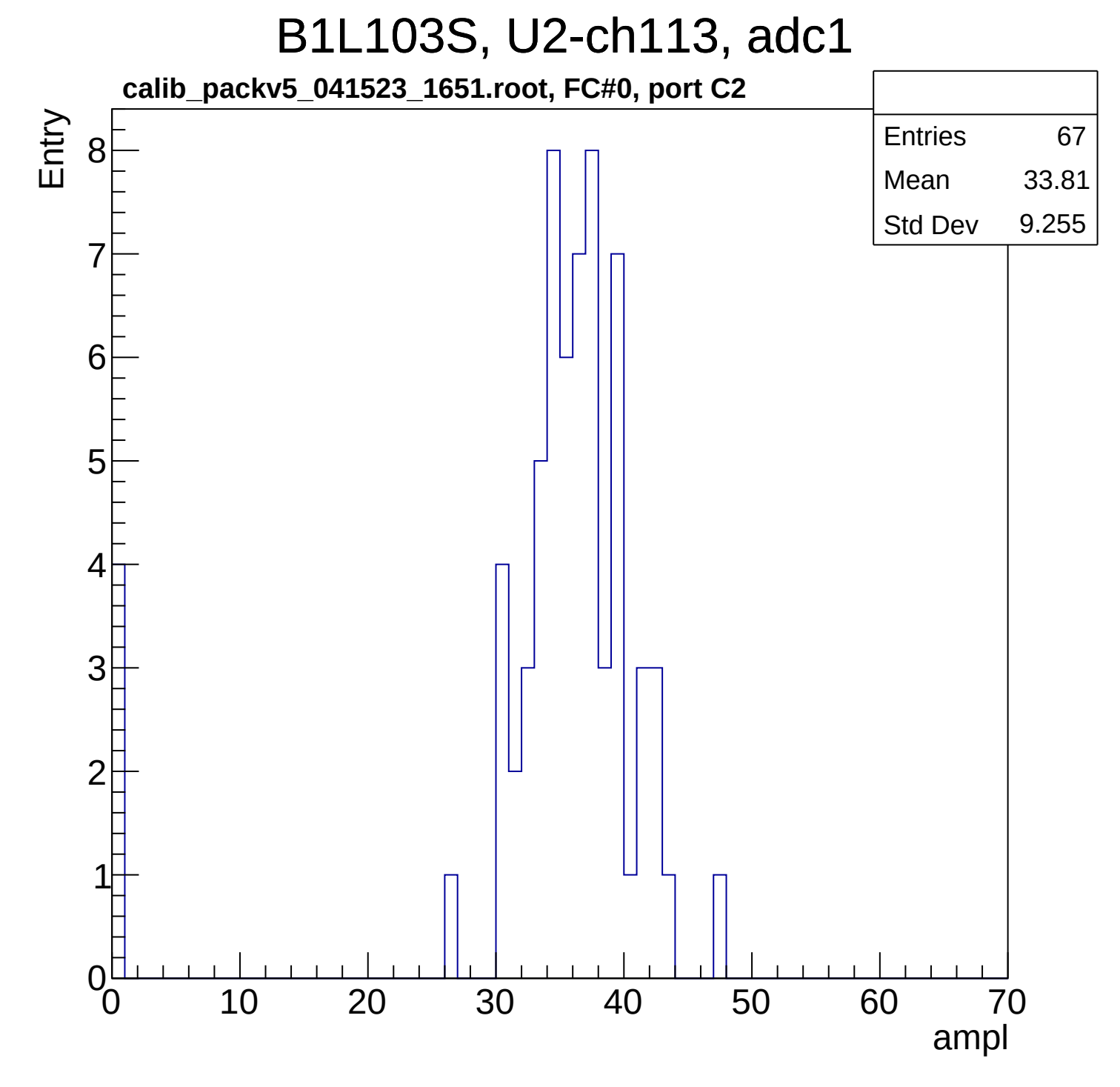

B1L103S, U2-ch112, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 52.78
Std Dev 3.533
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

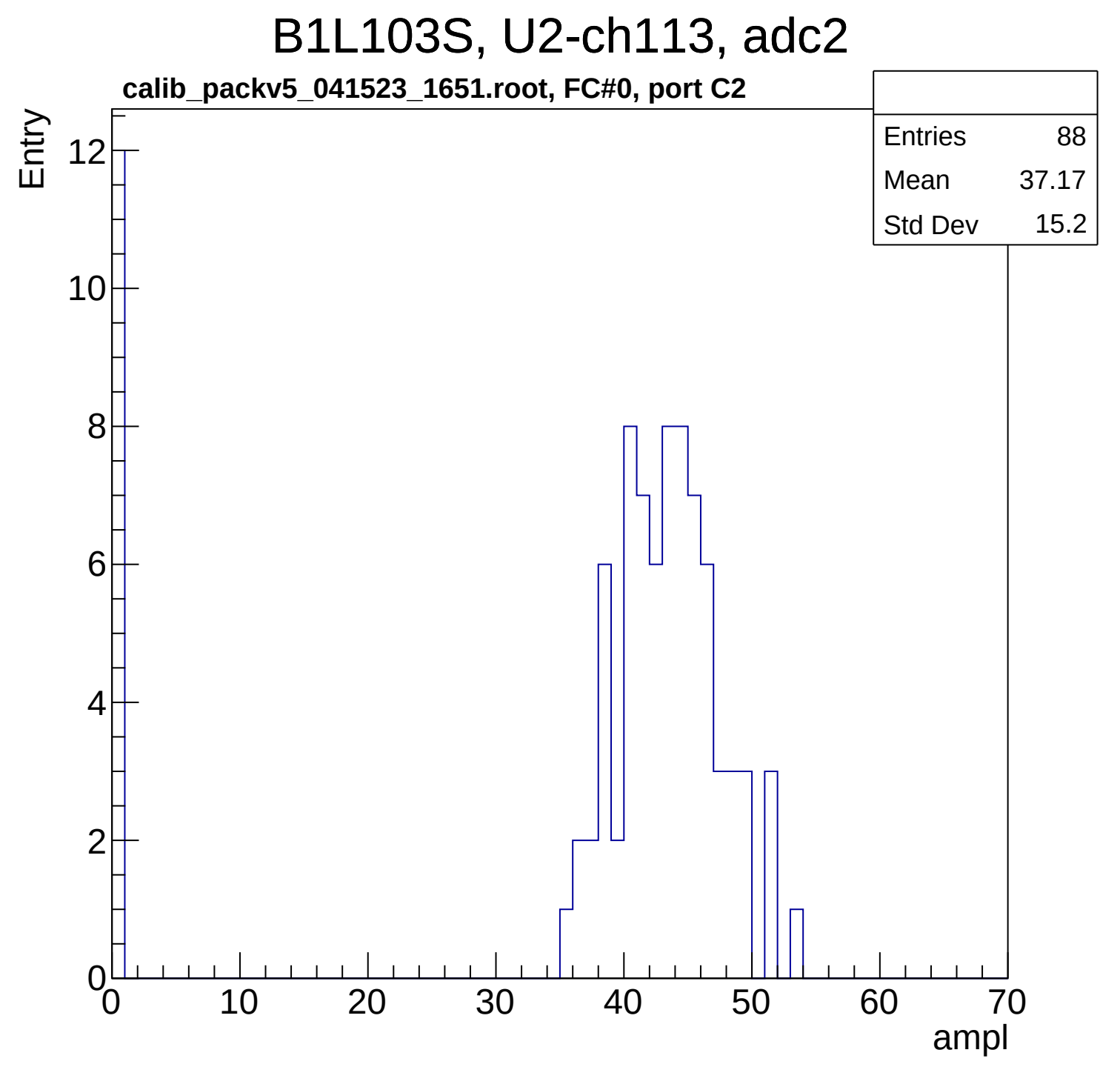

B1L103S, U2-ch112, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.24
Std Dev 2.88
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

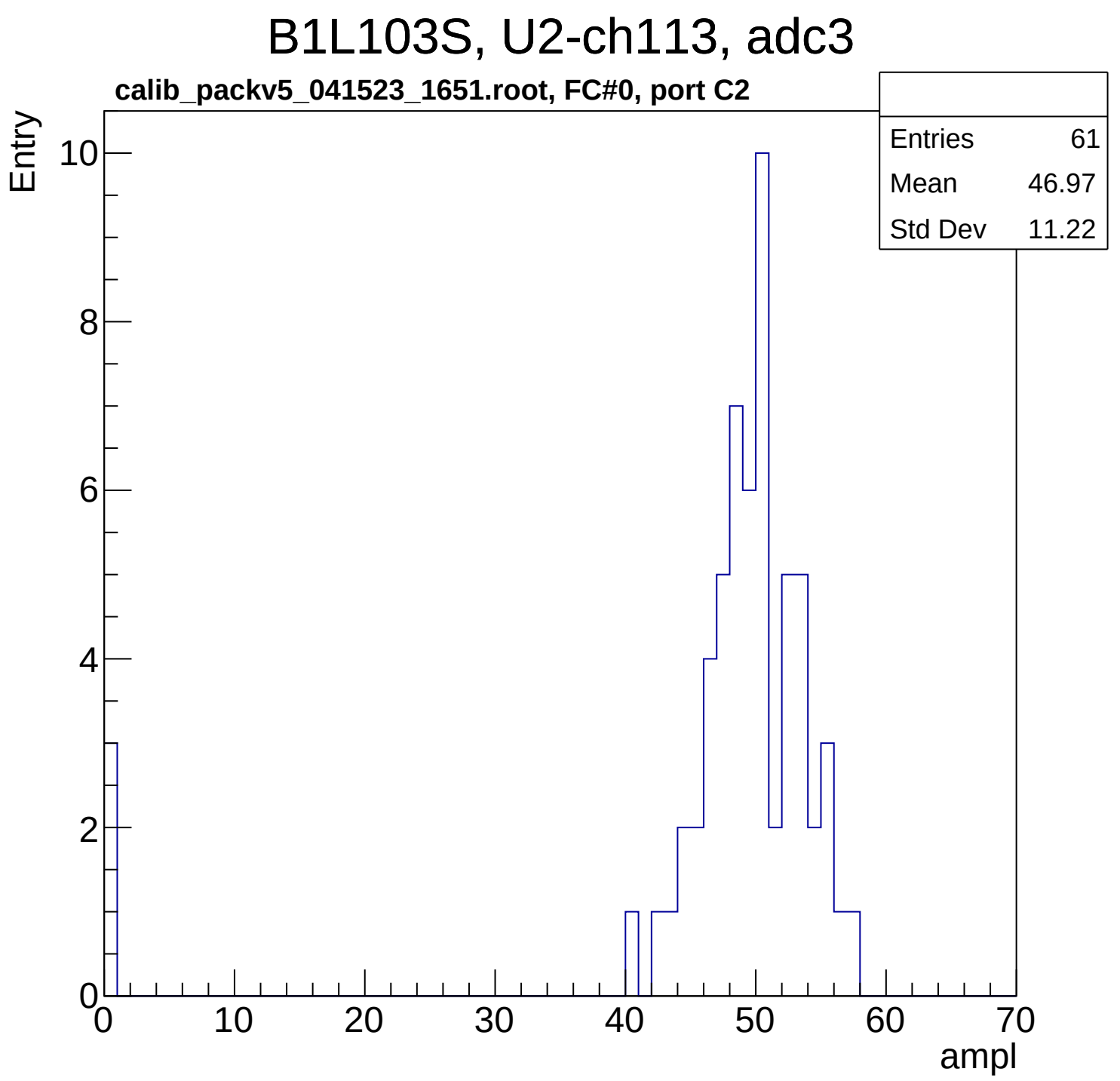

B1L103S, U2-ch112, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 58.52
Std Dev 13.16
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

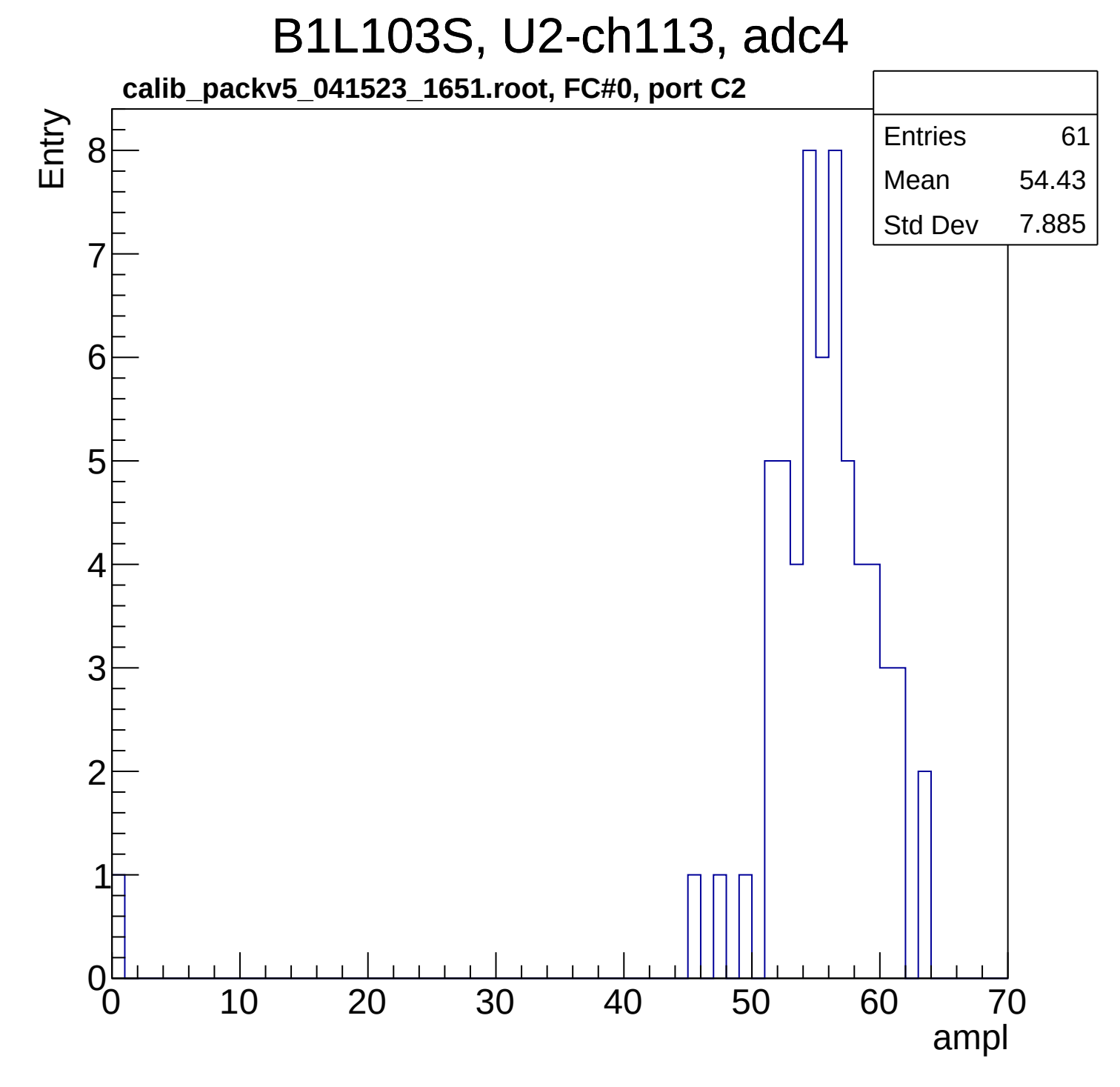

B1L103S, U2-ch112, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.857
Std Dev 18.05
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

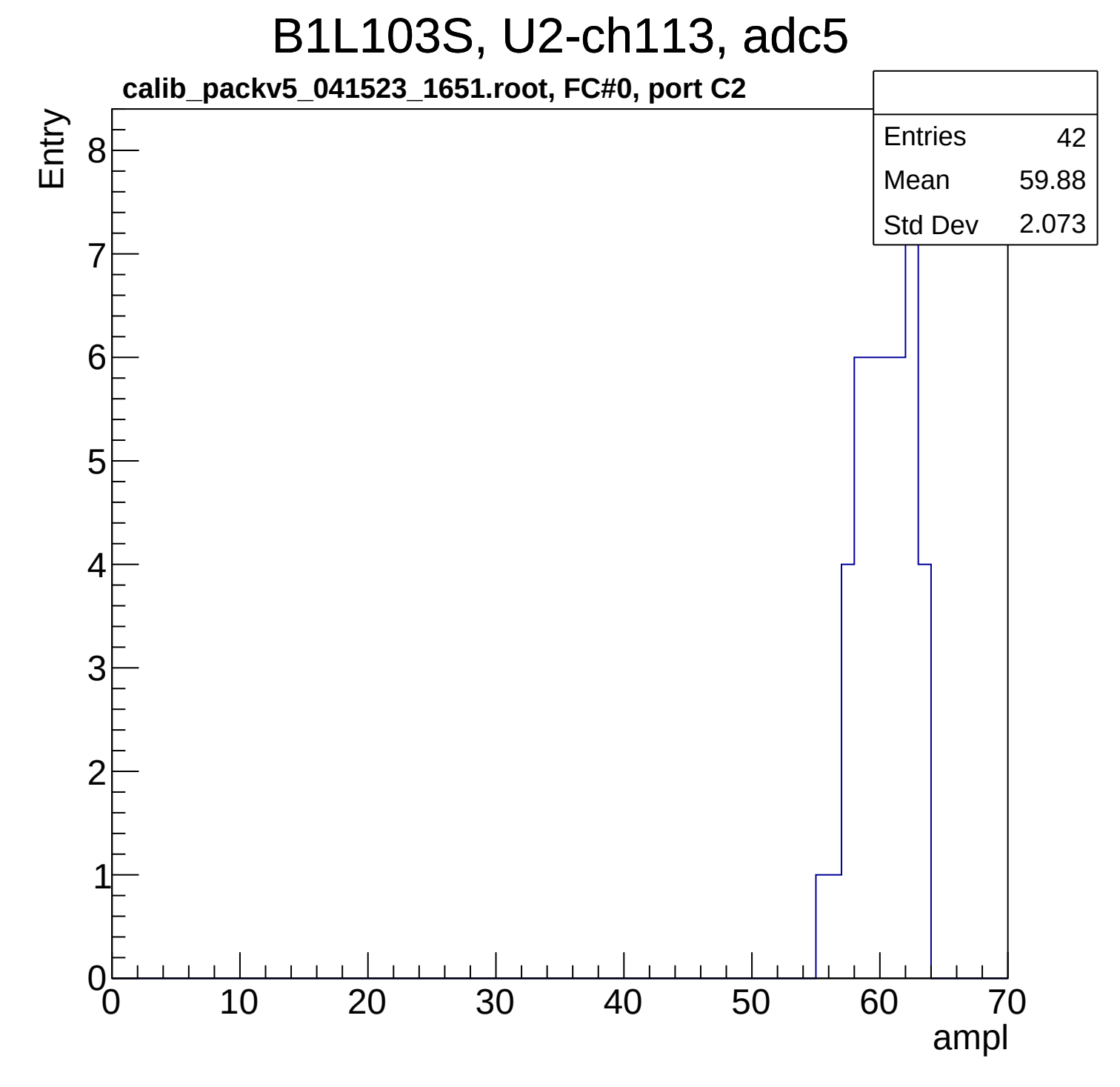

B1L103S, U2-ch113, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 18.5
Std Dev 14.97
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl

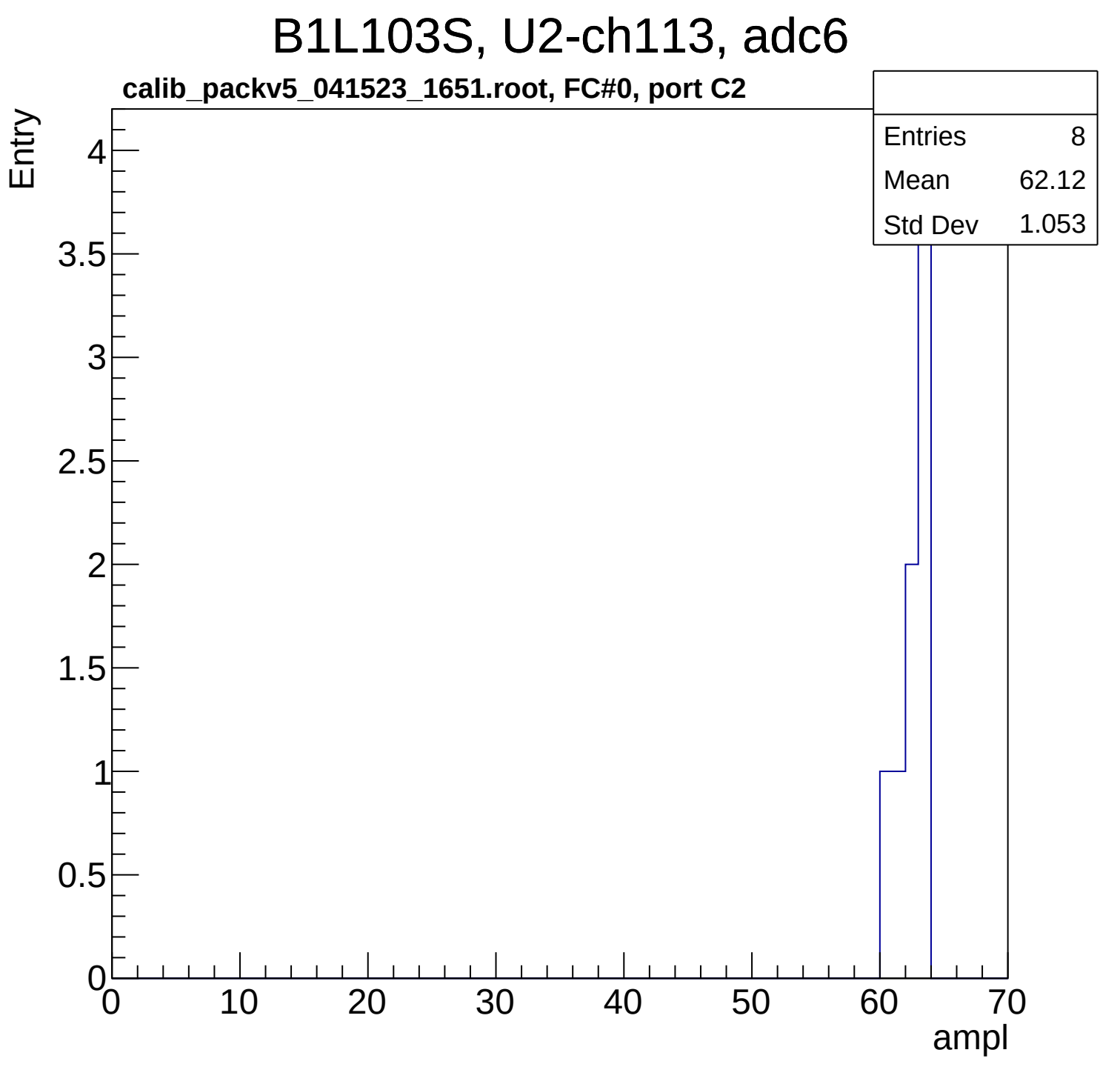

B1L103S, U2-ch113, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 33.81
Std Dev 9.255
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

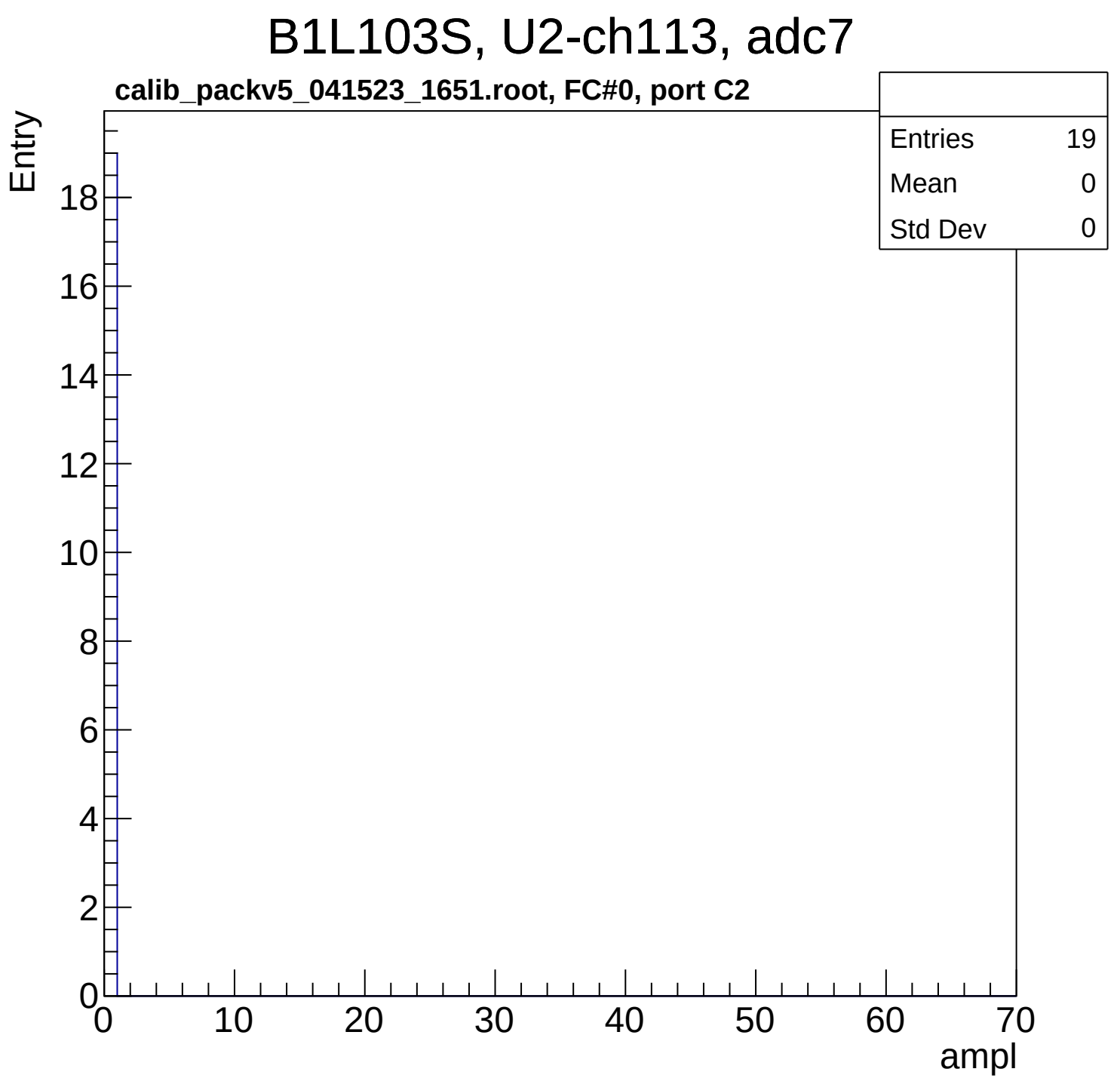

B1L103S, U2-ch113, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 37.17
Std Dev 15.2
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

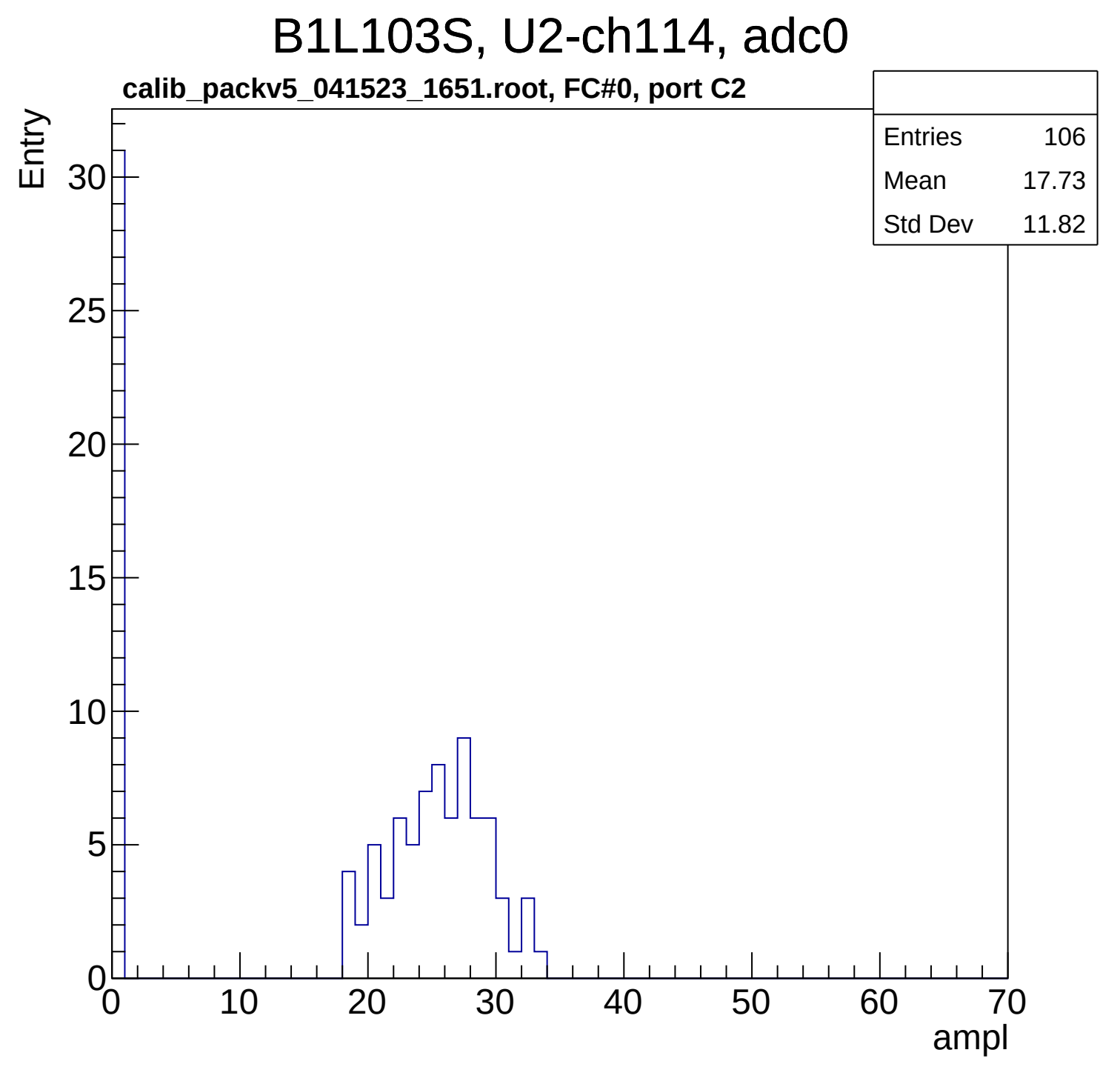

B1L103S, U2-ch113, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 46.97
Std Dev 11.22
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

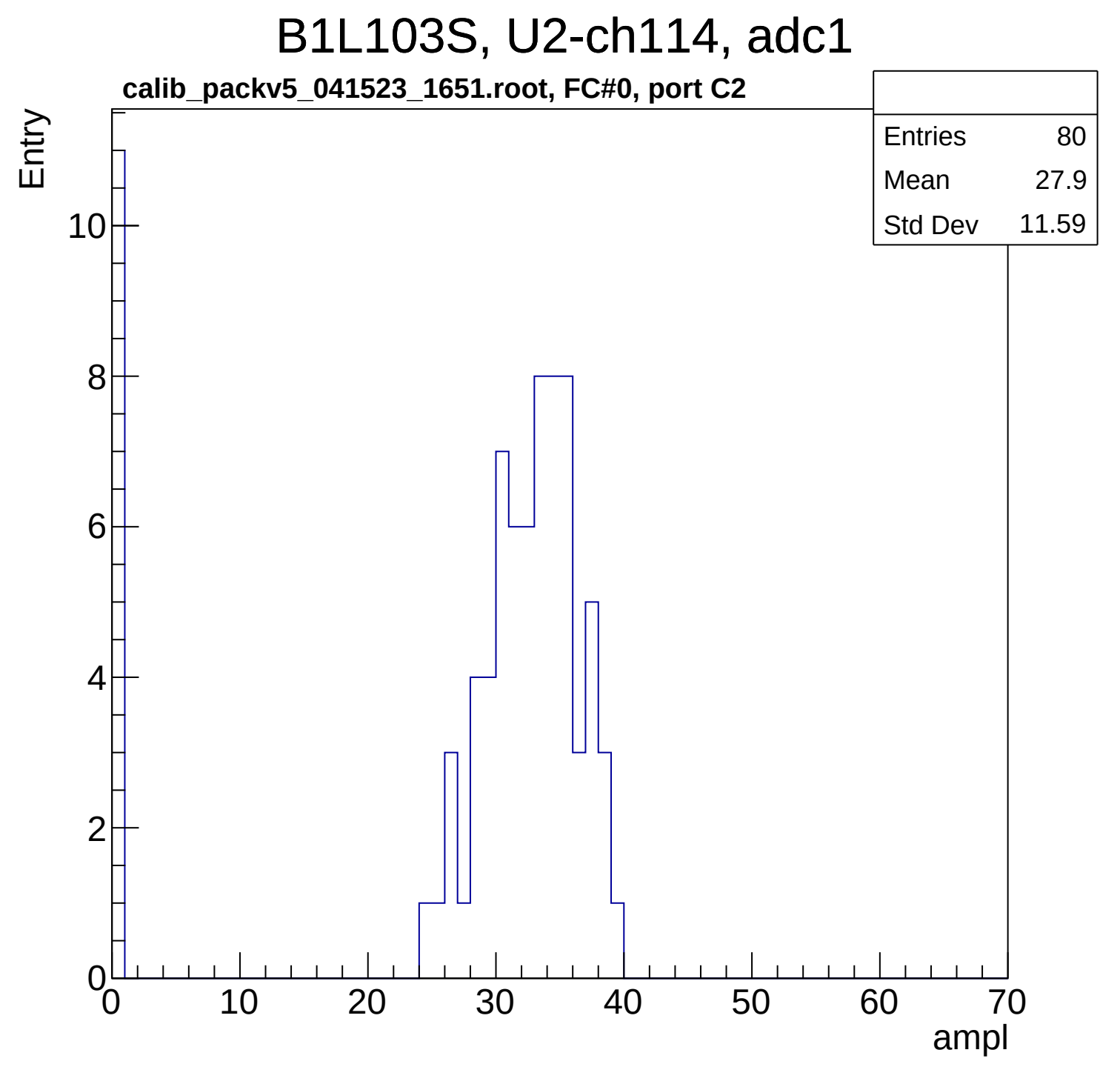

B1L103S, U2-ch113, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 54.43
Std Dev 7.885
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

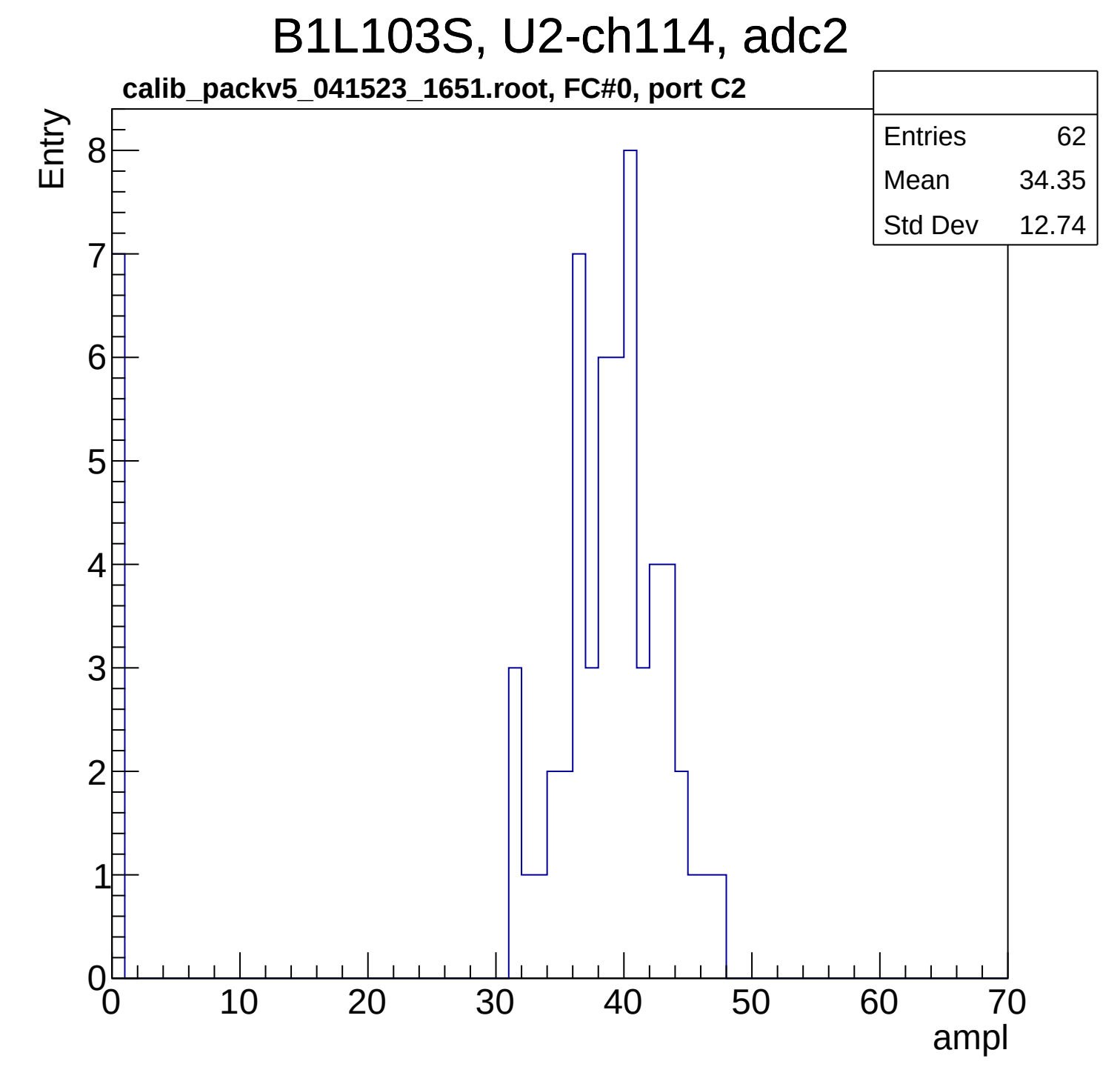

B1L103S, U2-ch113, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 59.88
Std Dev 2.073
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

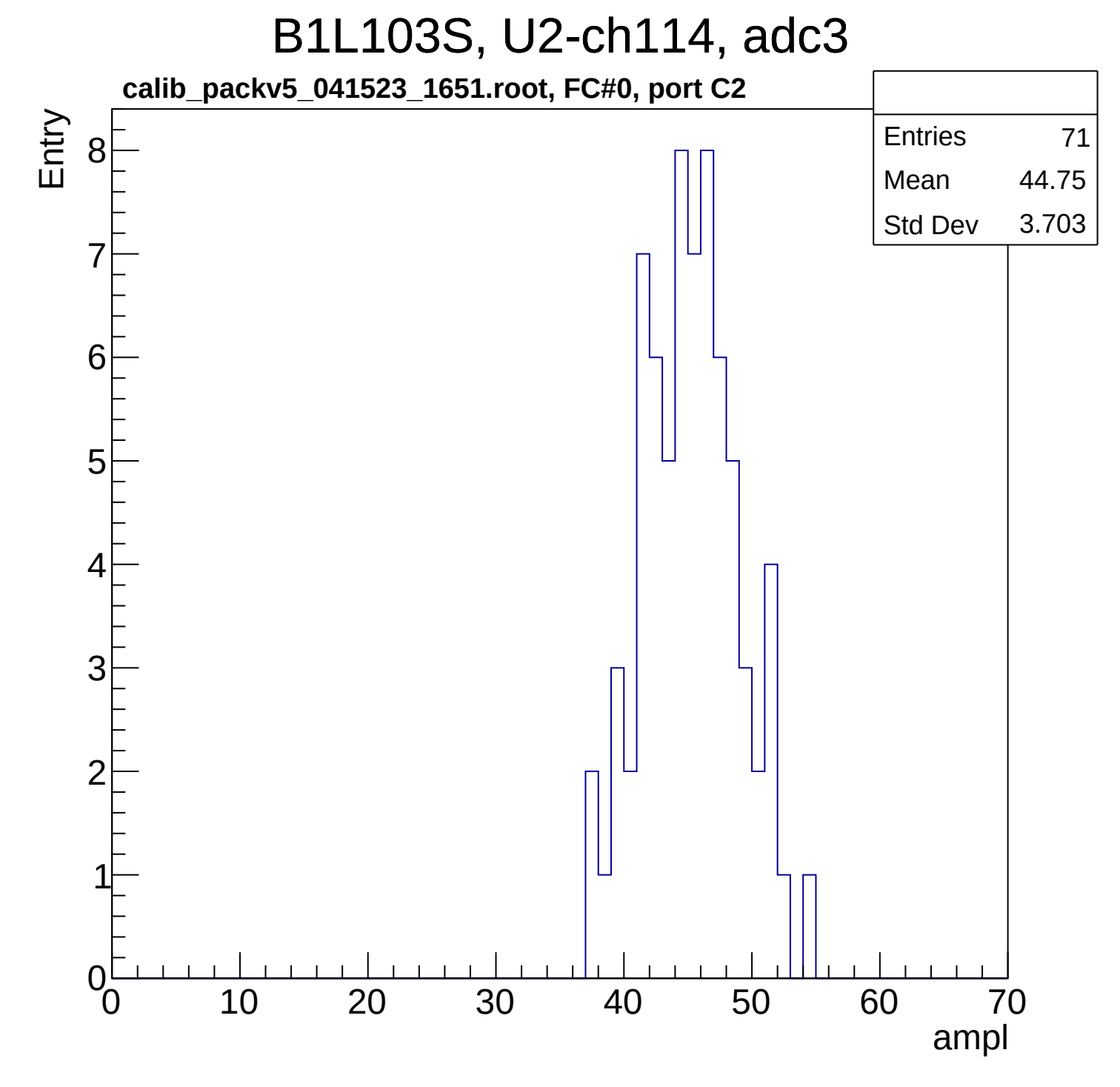

B1L103S, U2-ch113, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62.12
Std Dev 1.053
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

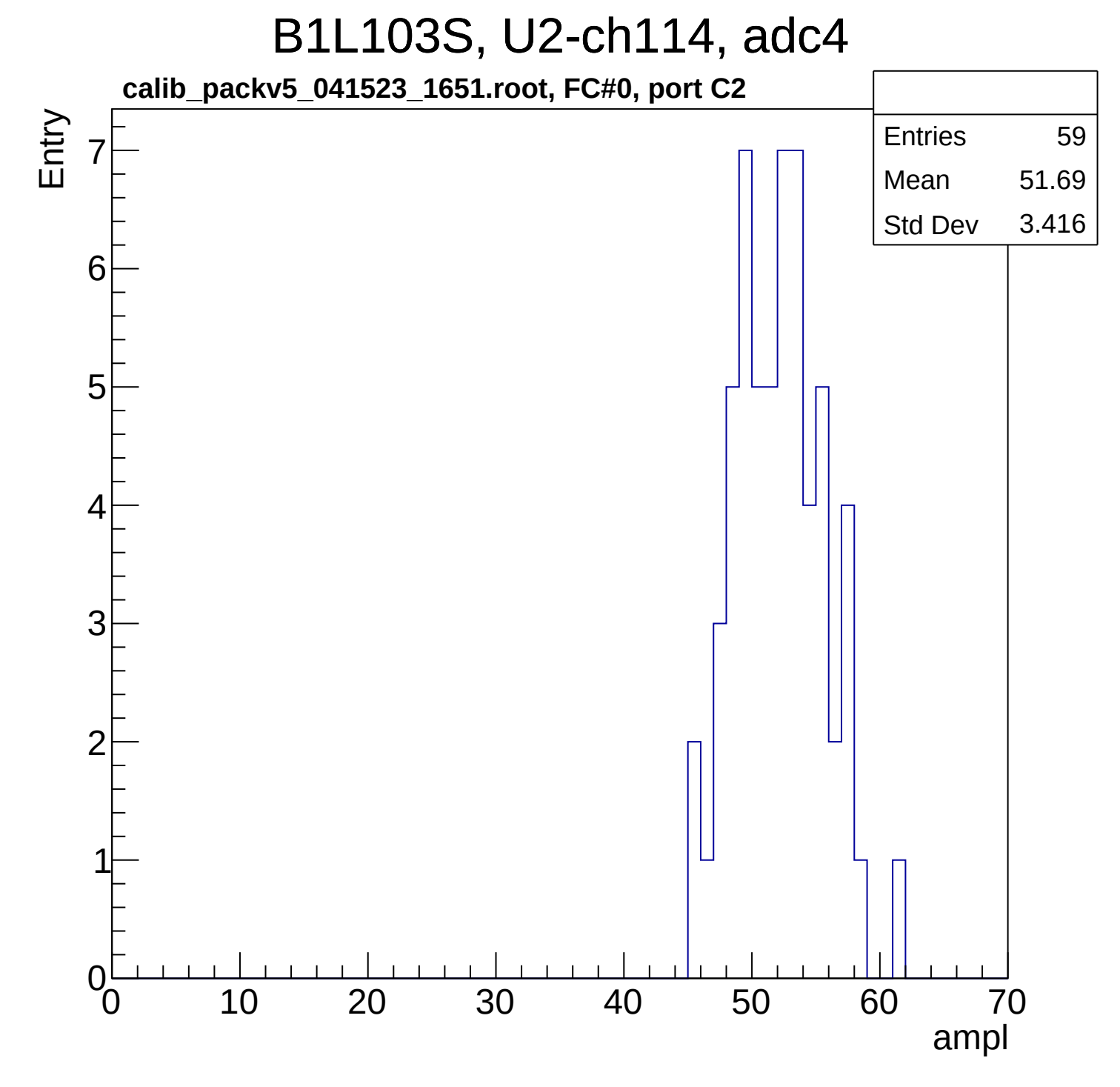

B1L103S, U2-ch113, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

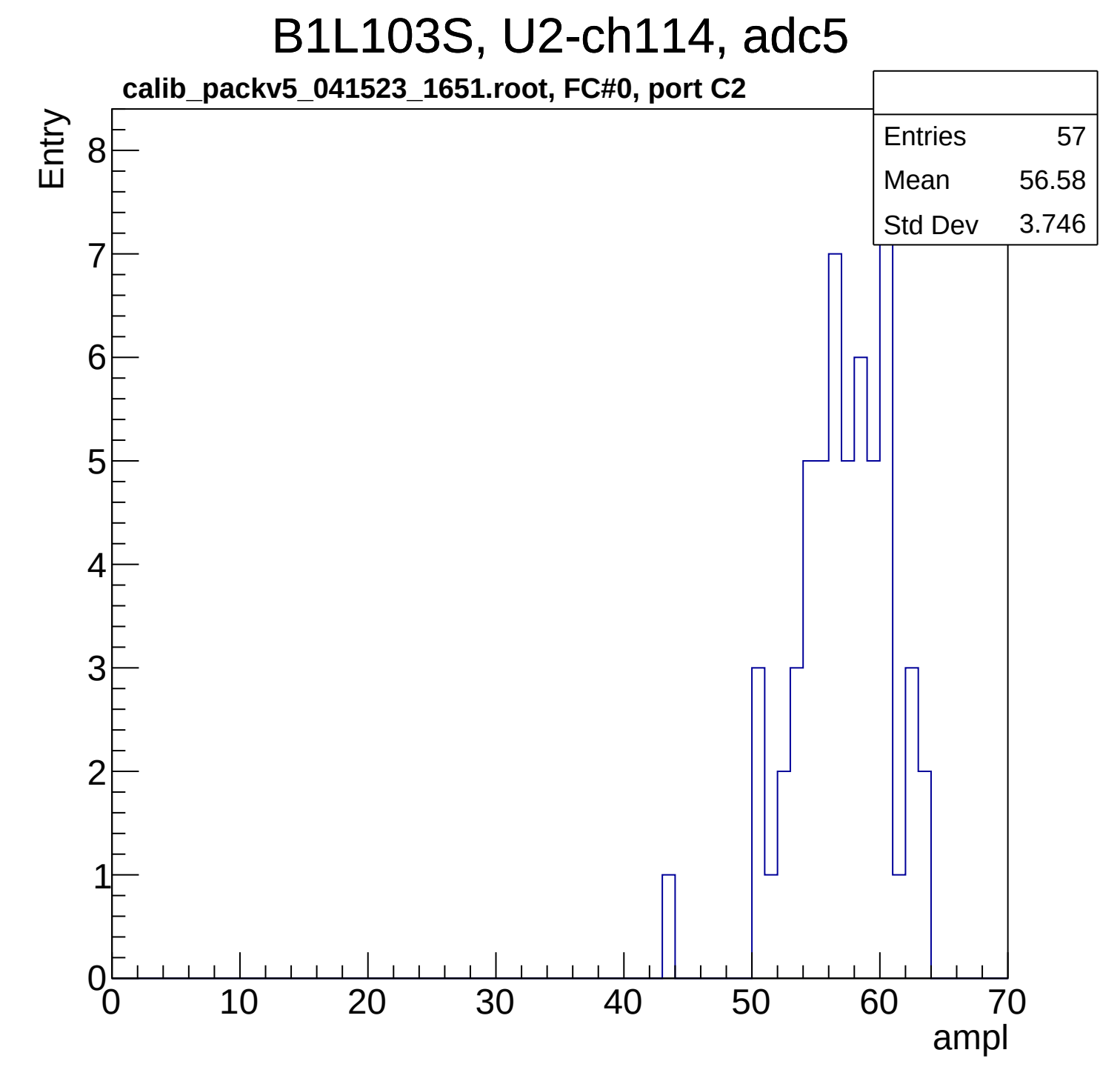

B1L103S, U2-ch114, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 106
Mean 17.73
Std Dev 11.82
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl

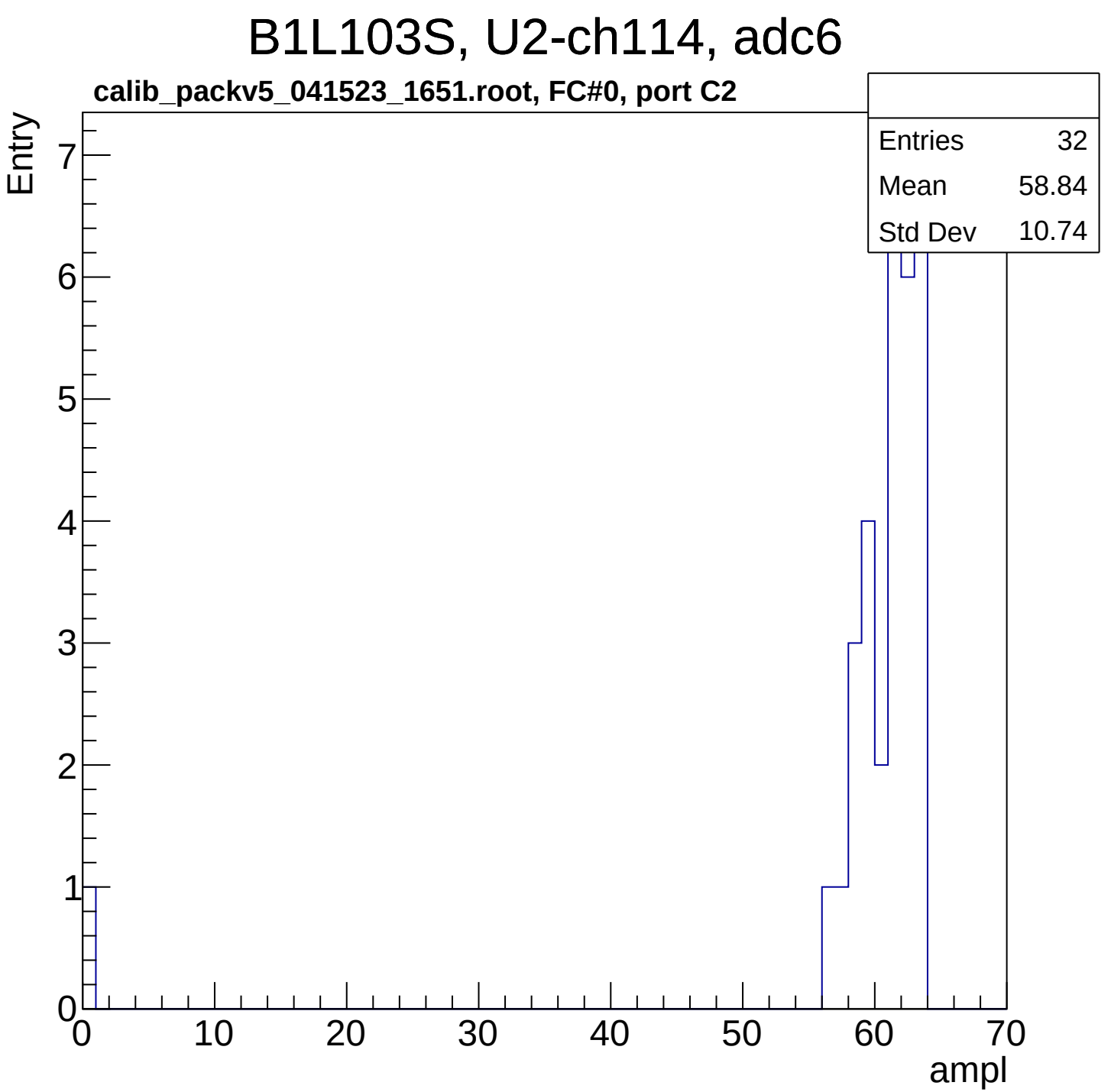

B1L103S, U2-ch114, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 27.9
Std Dev 11.59
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

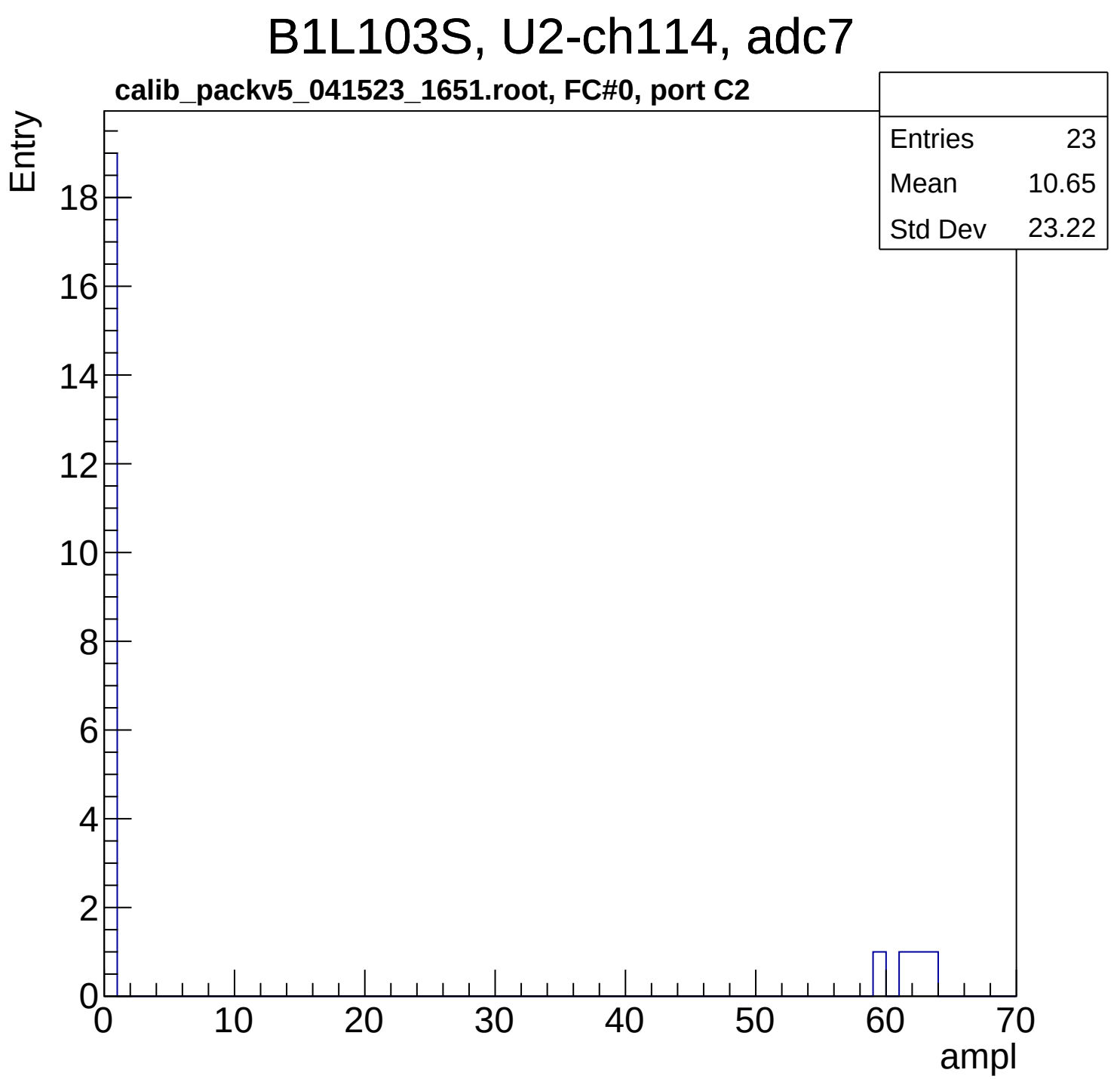

B1L103S, U2-ch114, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 34.35
Std Dev 12.74
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

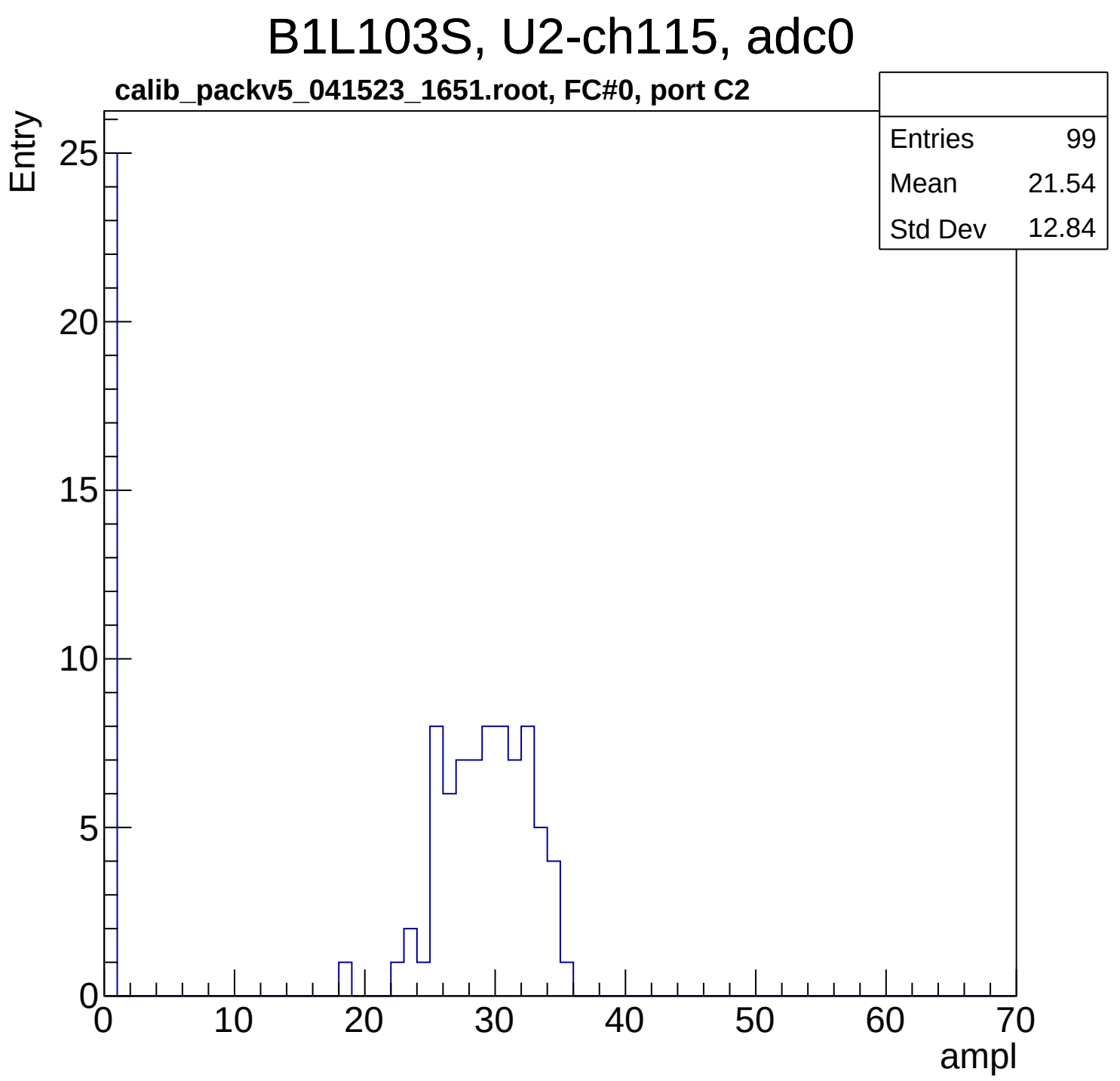

B1L103S, U2-ch114, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 44.75
Std Dev 3.703
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

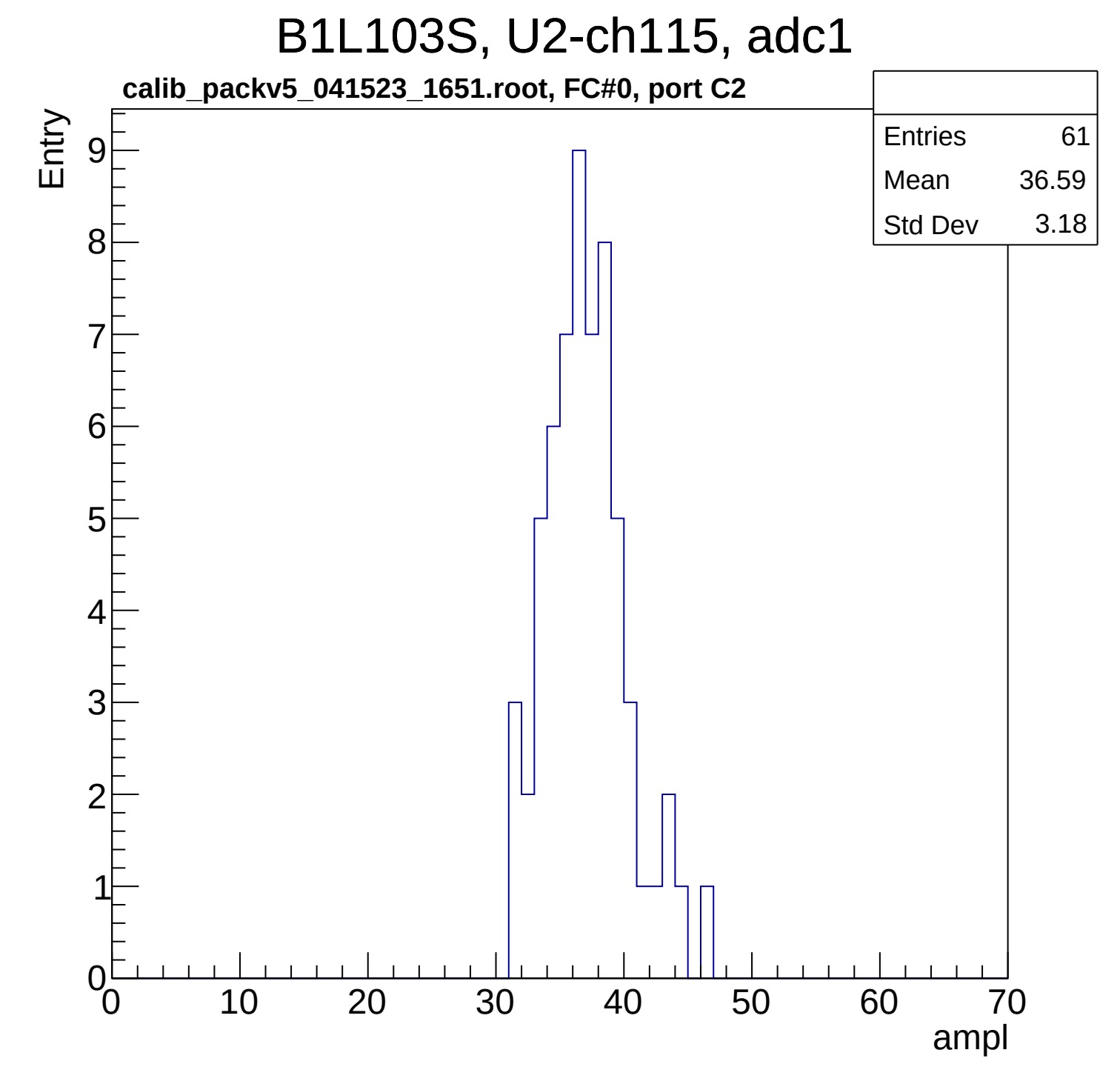

B1L103S, U2-ch114, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 51.69
Std Dev 3.416
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

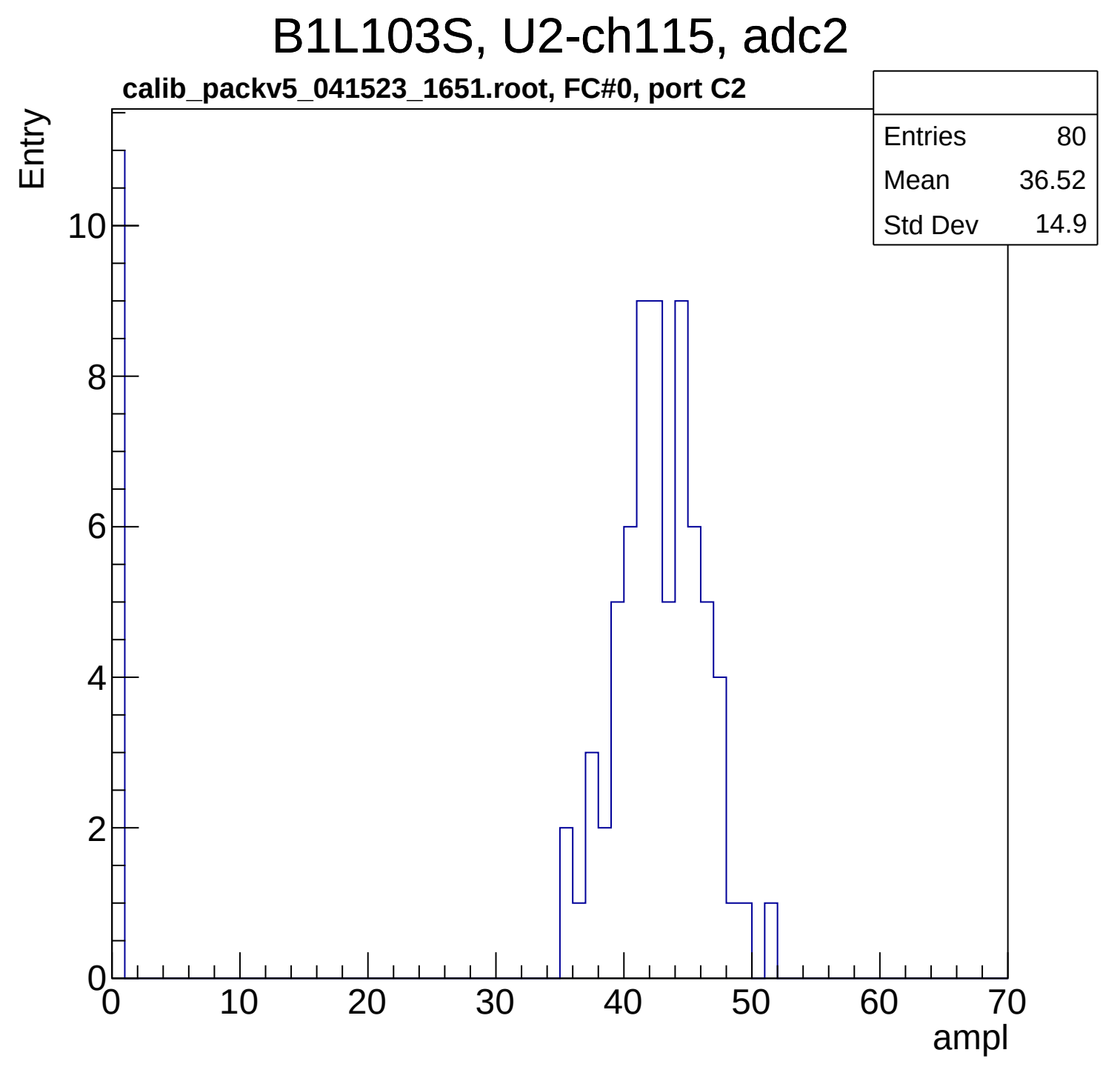

B1L103S, U2-ch114, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 56.58
Std Dev 3.746
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

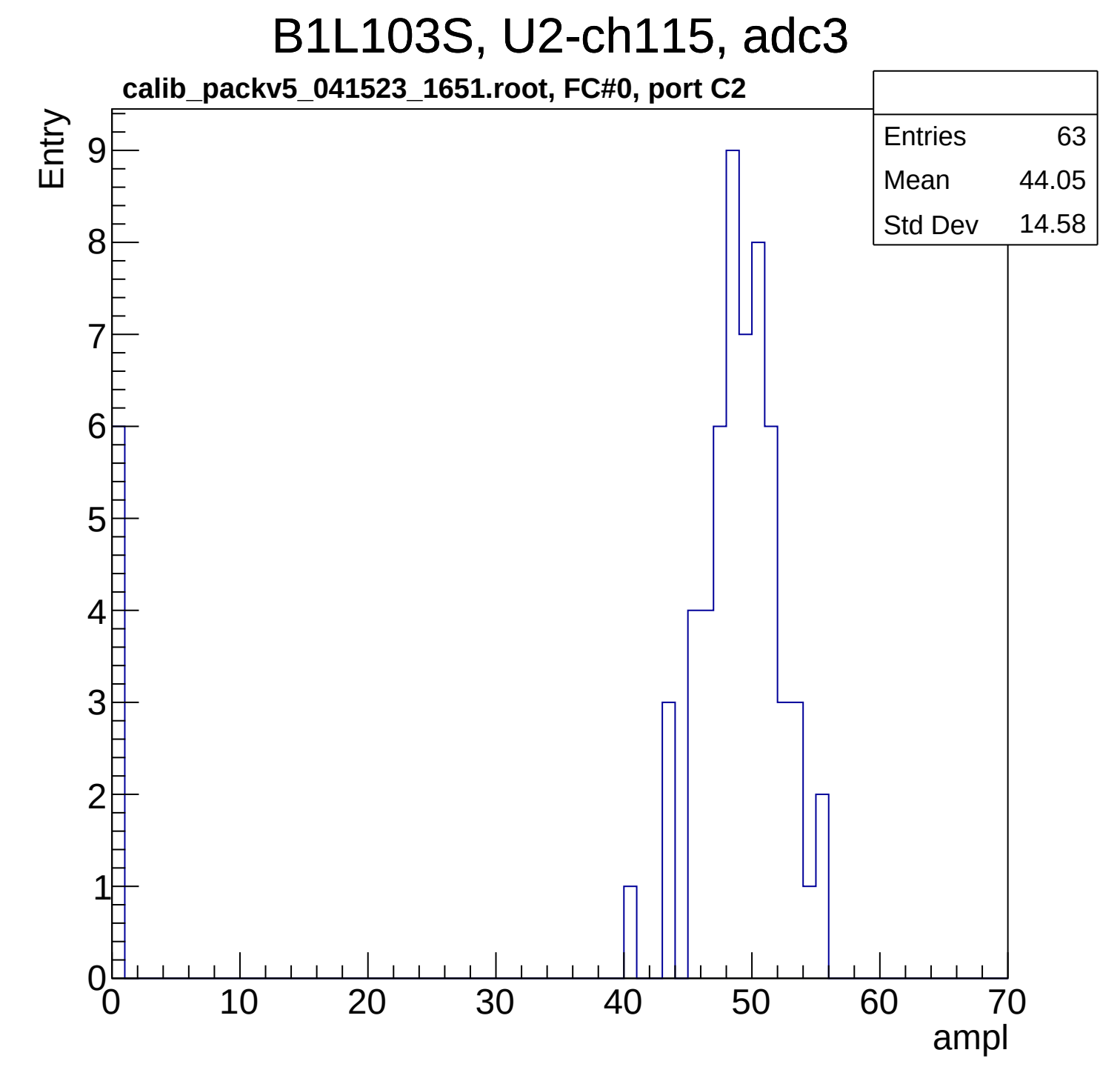

B1L103S, U2-ch114, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 58.84
Std Dev 10.74
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

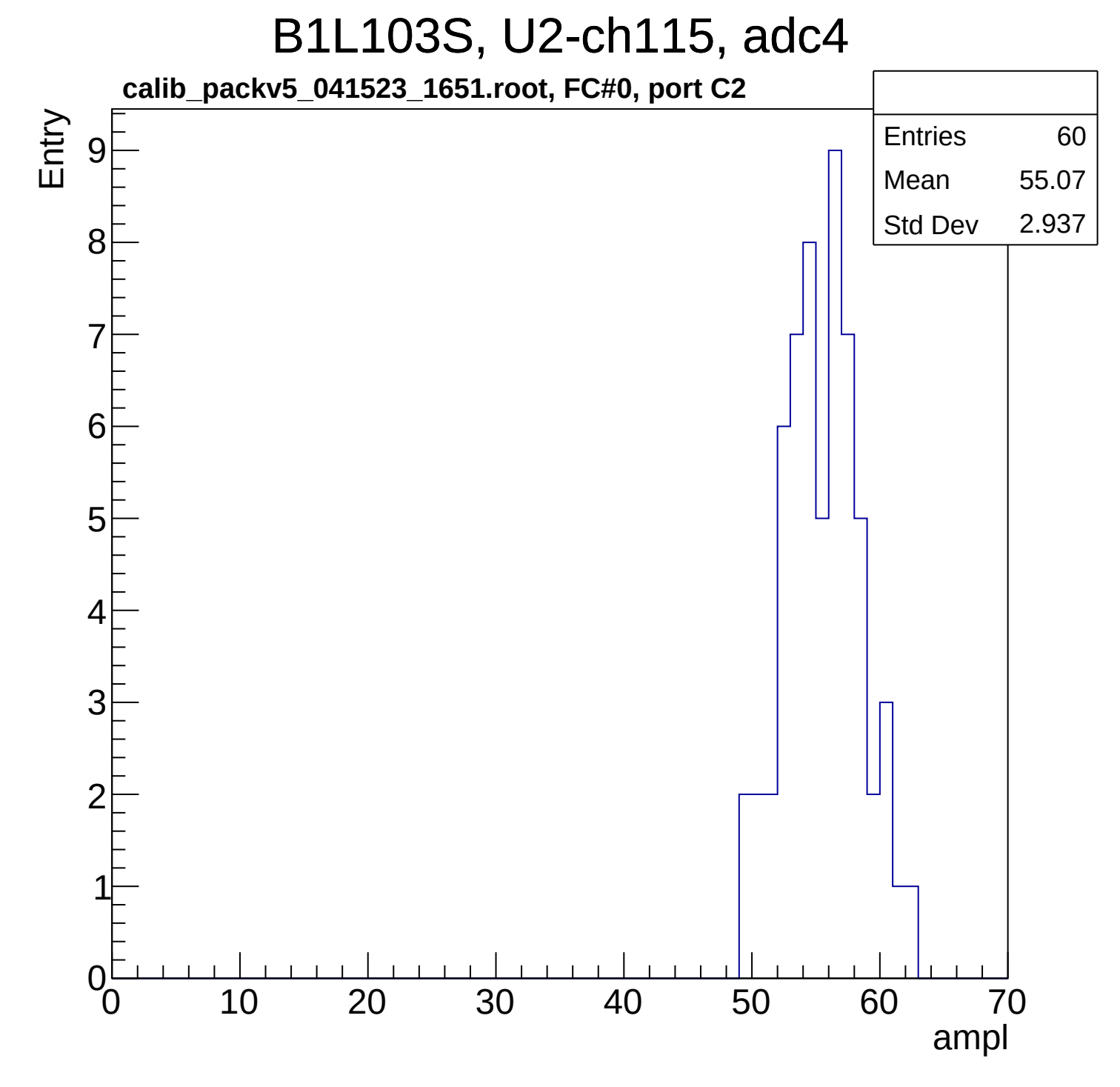

B1L103S, U2-ch114, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 23
Mean 10.65
Std Dev 23.22
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

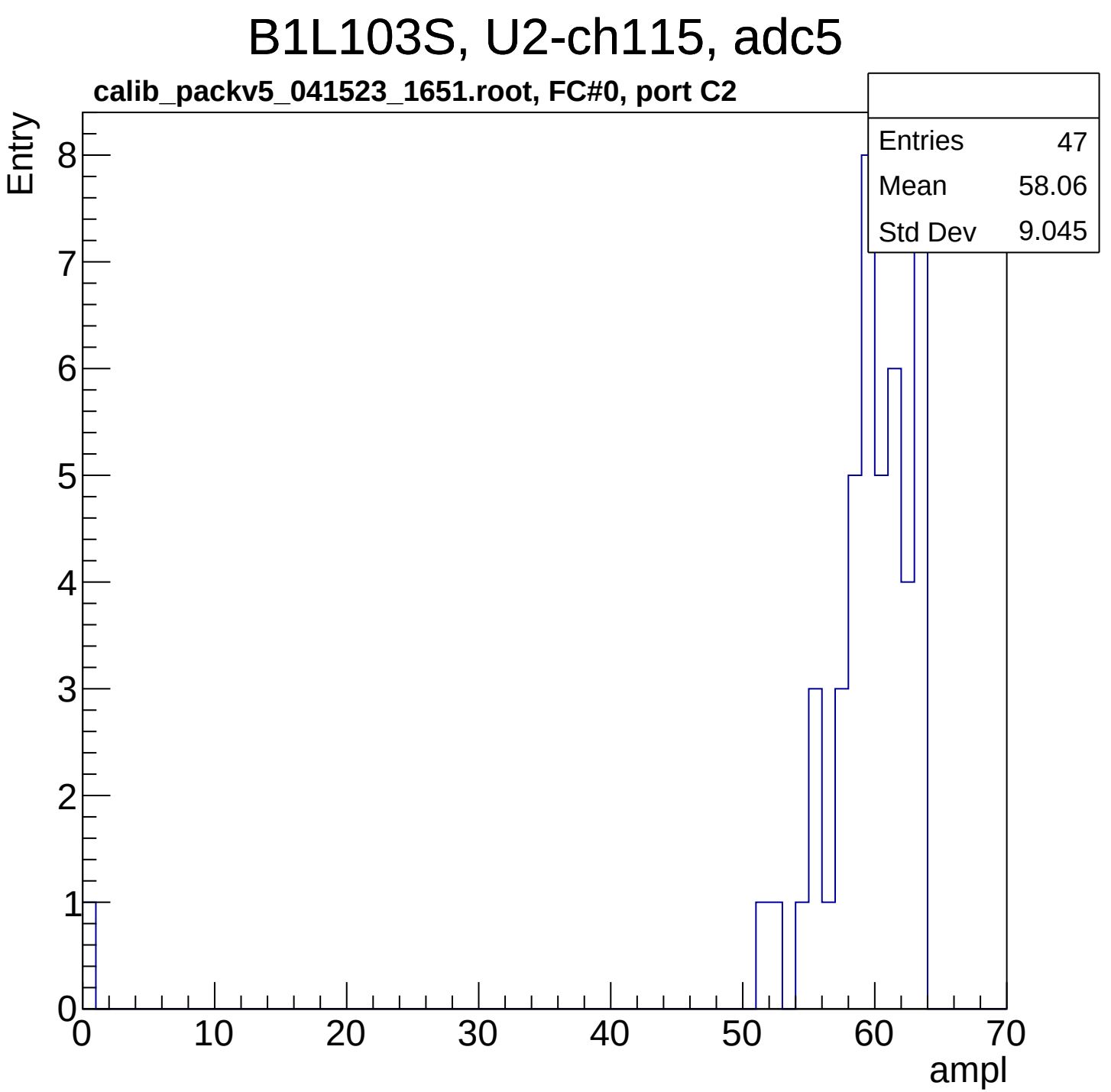

B1L103S, U2-ch115, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 21.54
Std Dev 12.84
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl

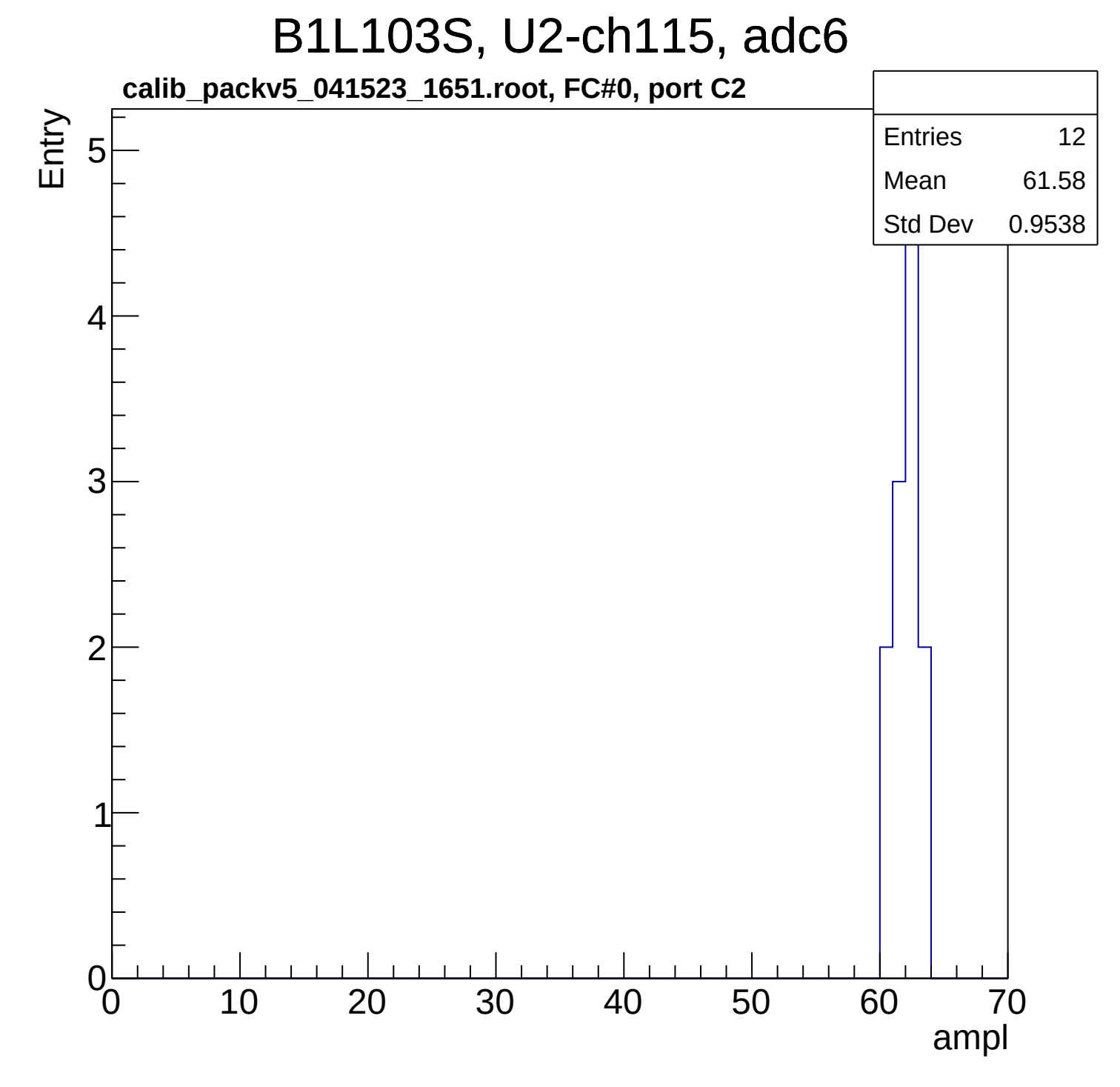

B1L103S, U2-ch115, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 36.59
Std Dev 3.18
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

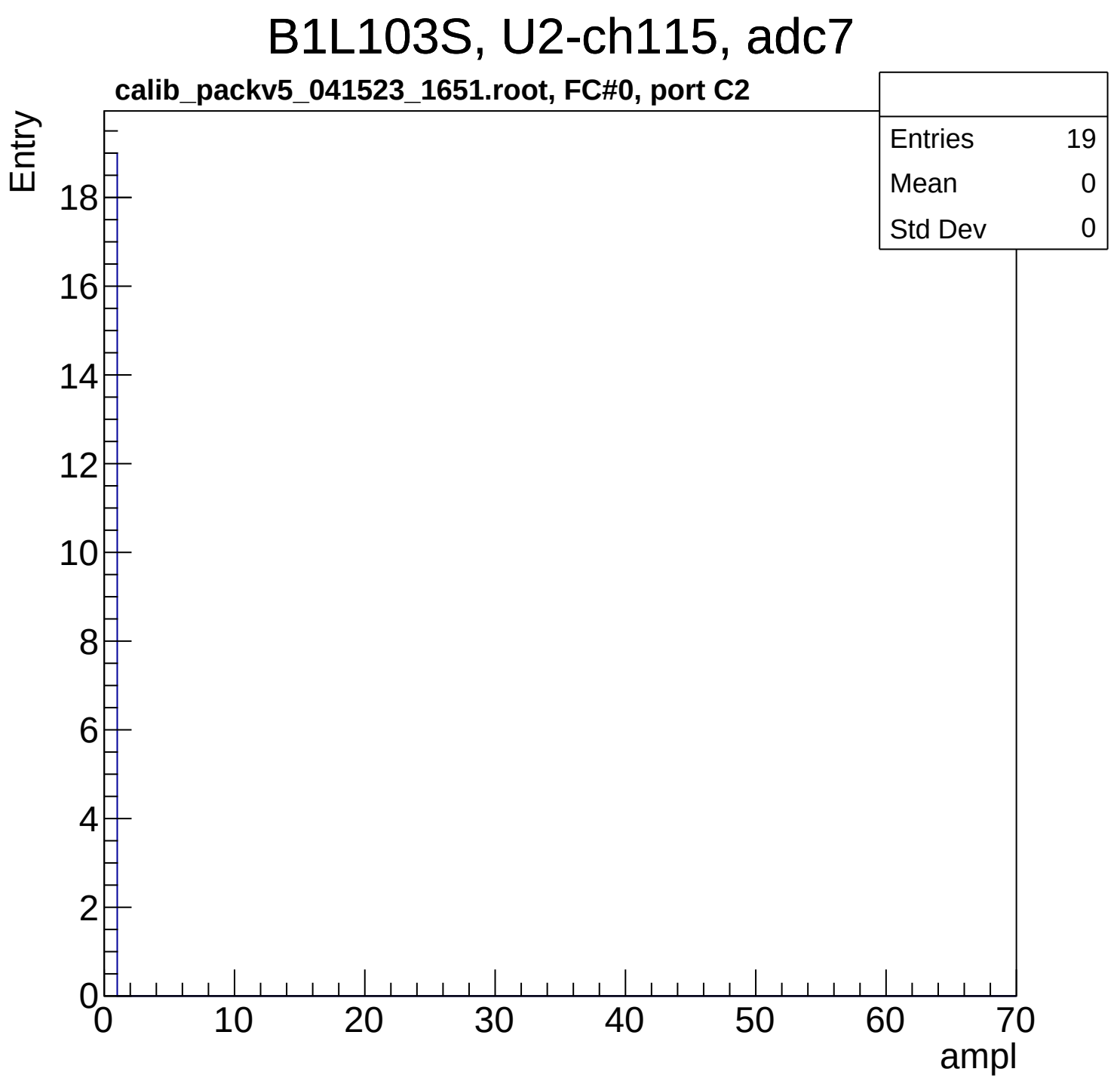

B1L103S, U2-ch115, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 36.52
Std Dev 14.9
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

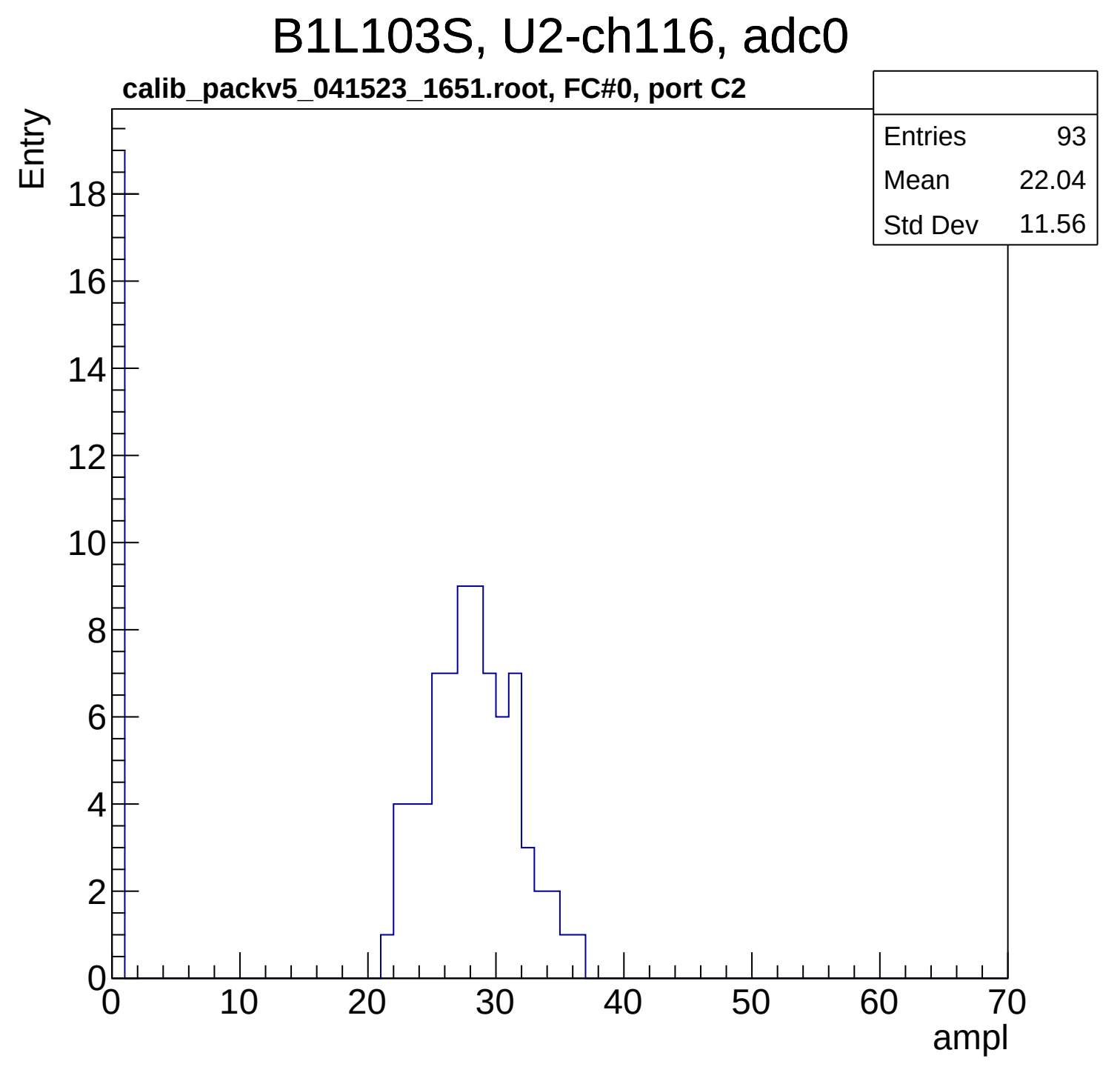

B1L103S, U2-ch115, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 44.05
Std Dev 14.58
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

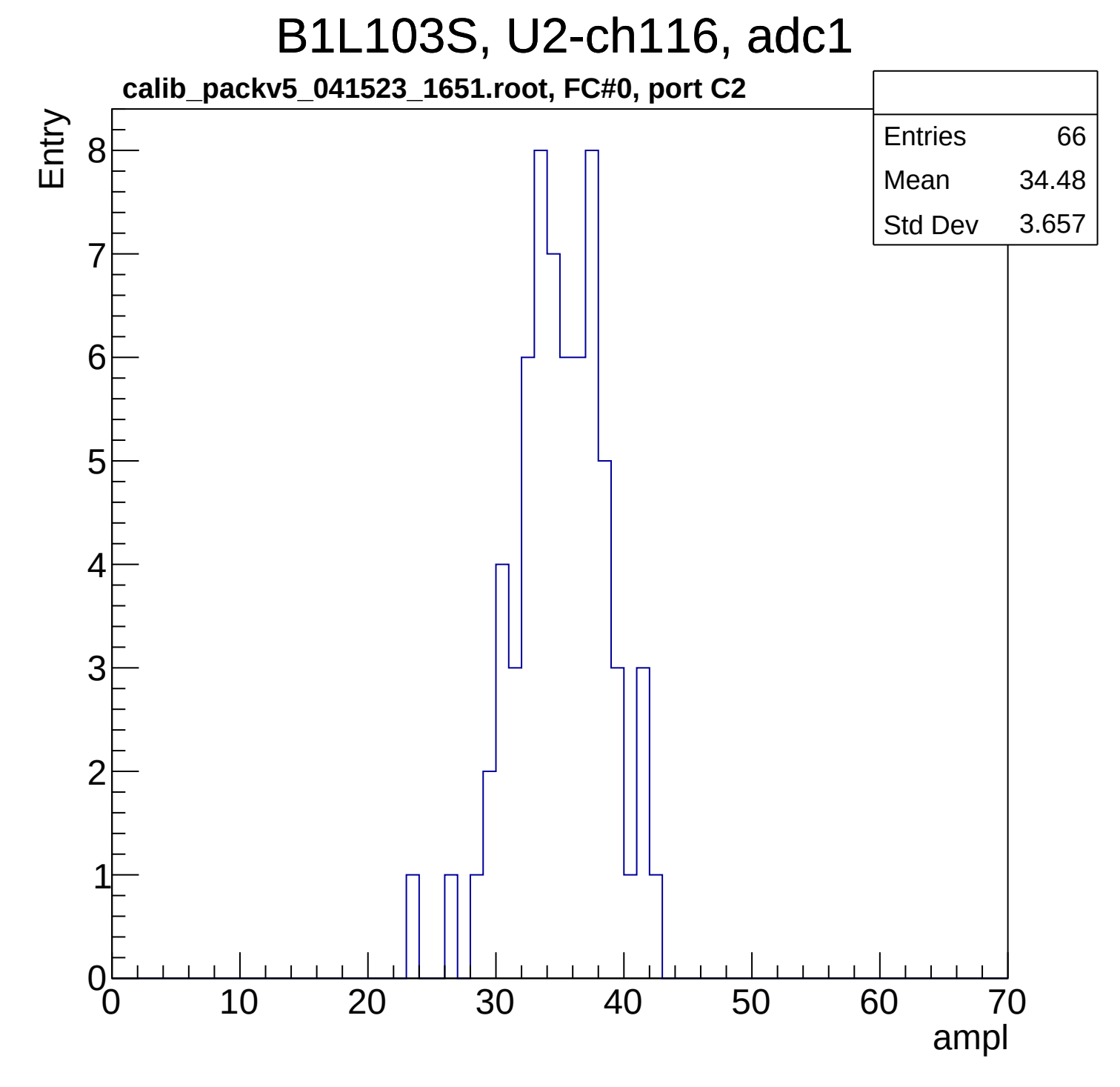

B1L103S, U2-ch115, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 55.07
Std Dev 2.937
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

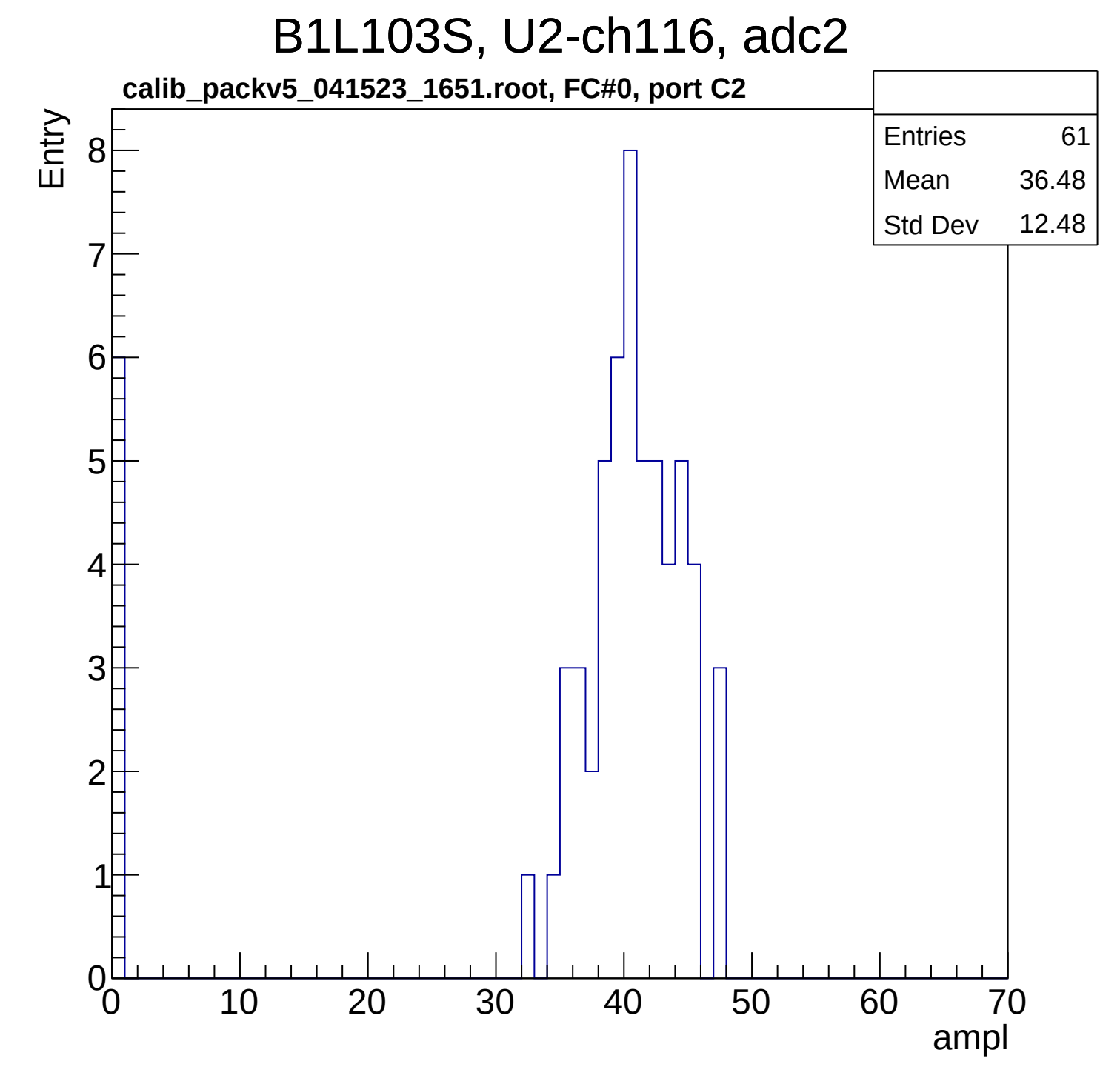

B1L103S, U2-ch115, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.06
Std Dev 9.045
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

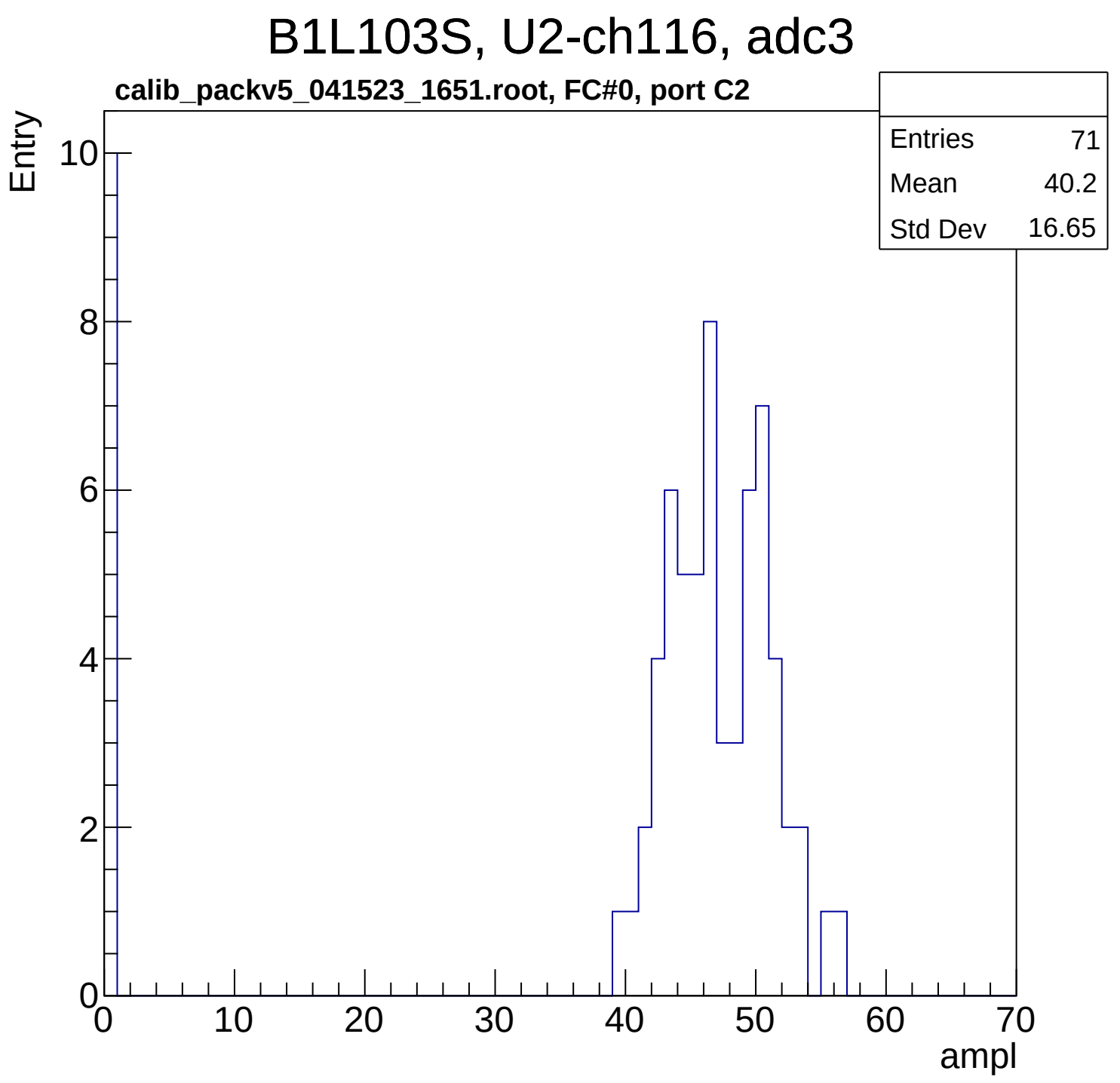

B1L103S, U2-ch115, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.58
Std Dev 0.9538
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

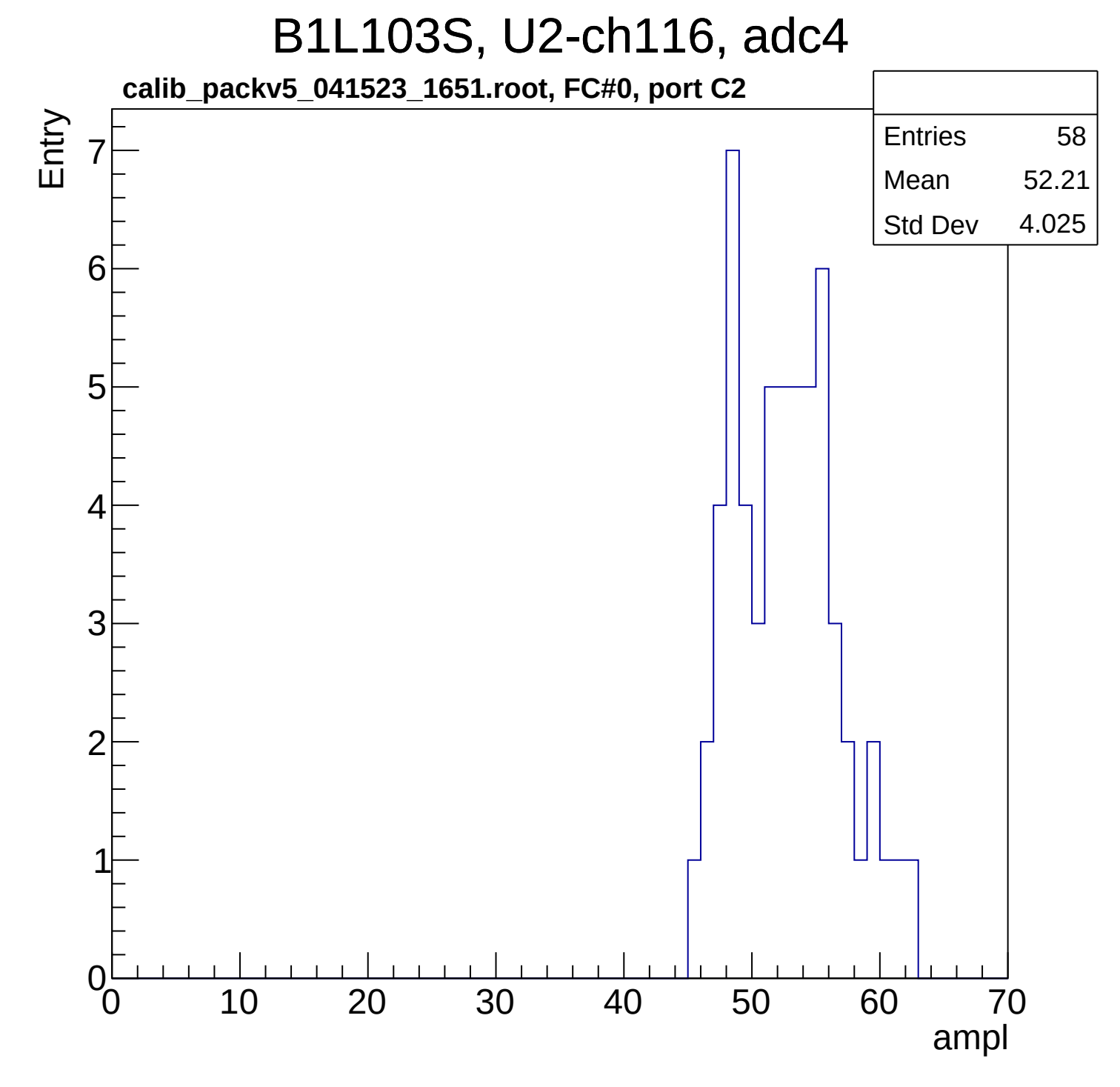

B1L103S, U2-ch115, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

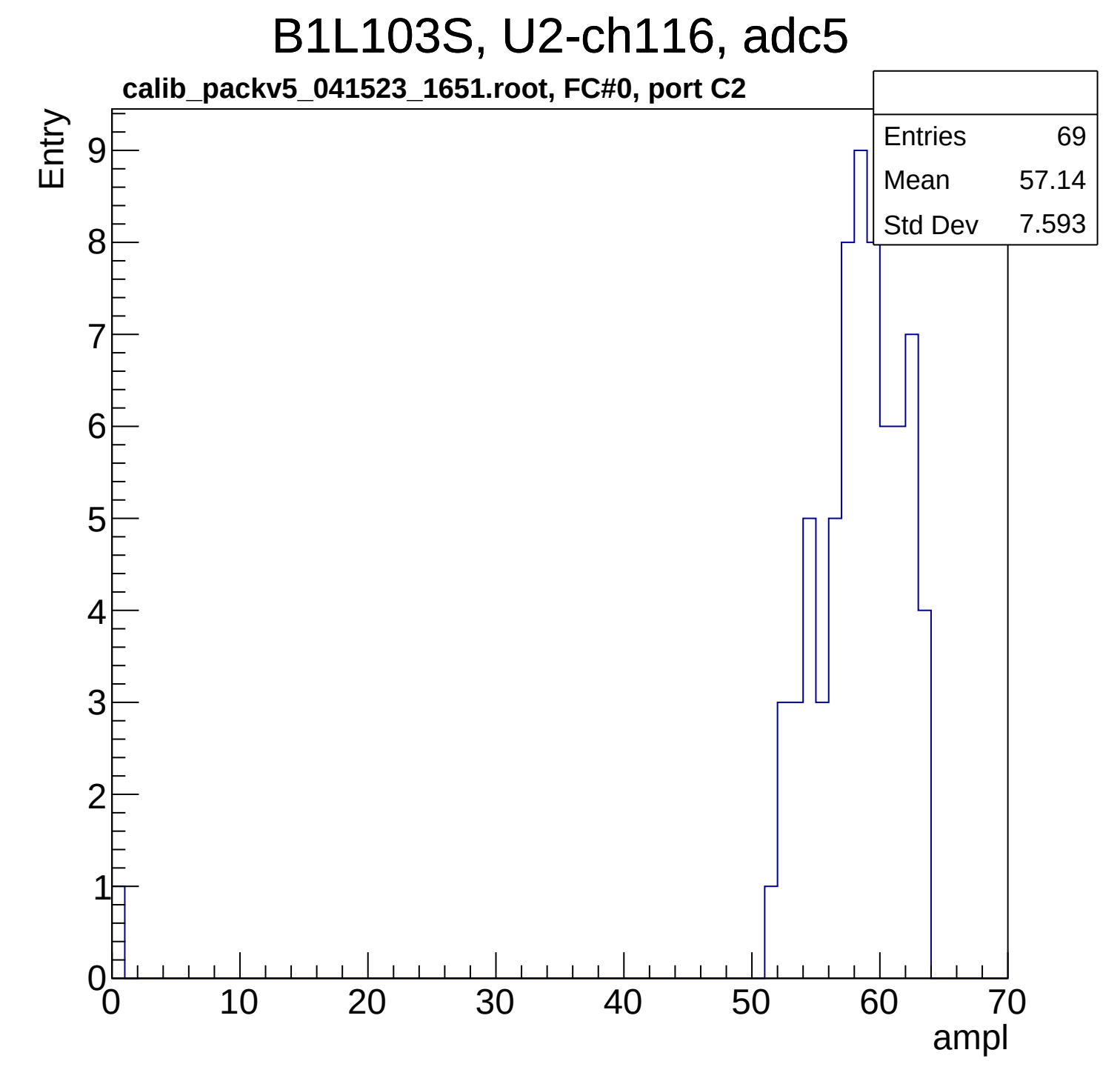

B1L103S, U2-ch116, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 22.04
Std Dev 11.56
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

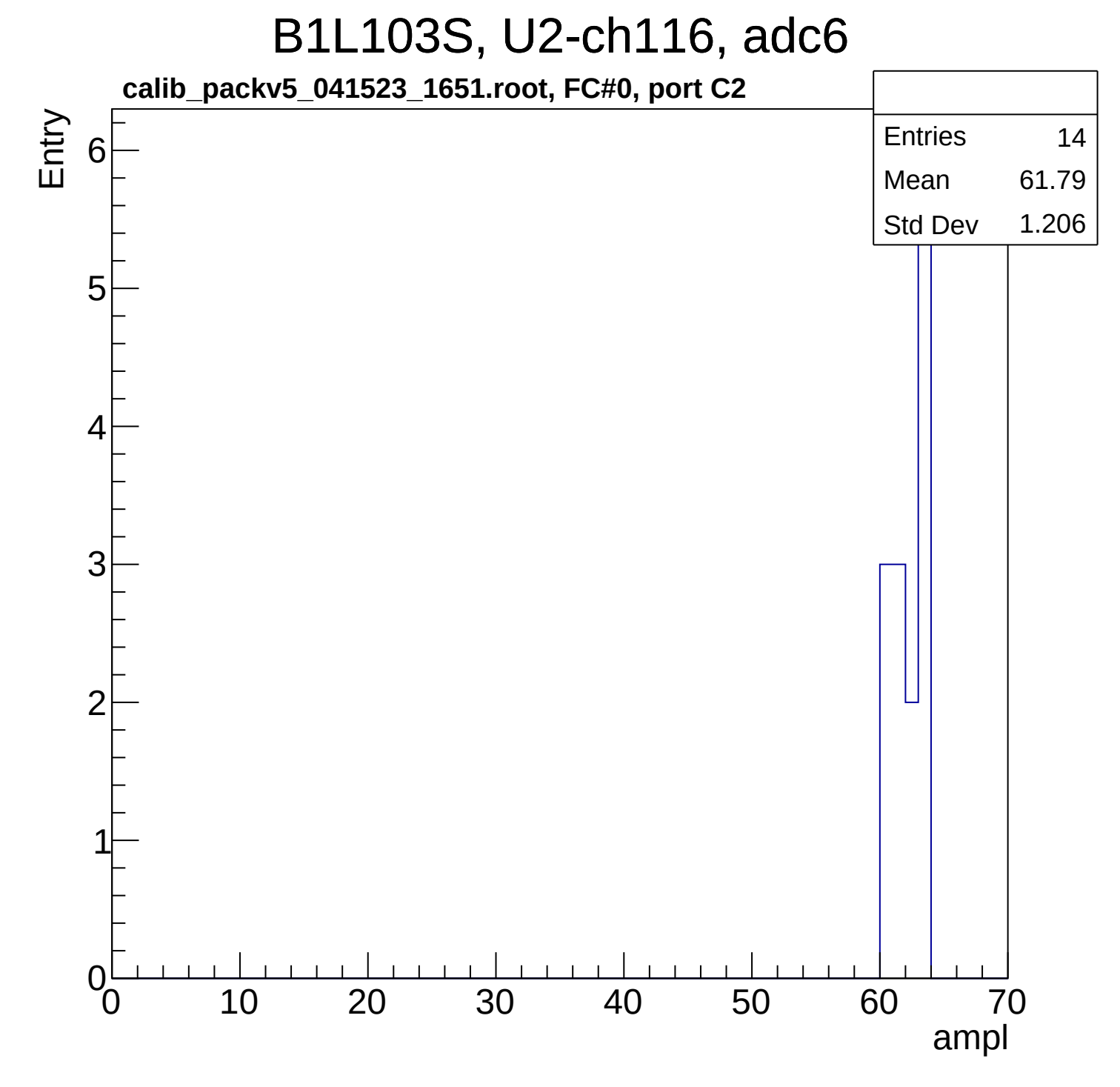

B1L103S, U2-ch116, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 34.48
Std Dev 3.657
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

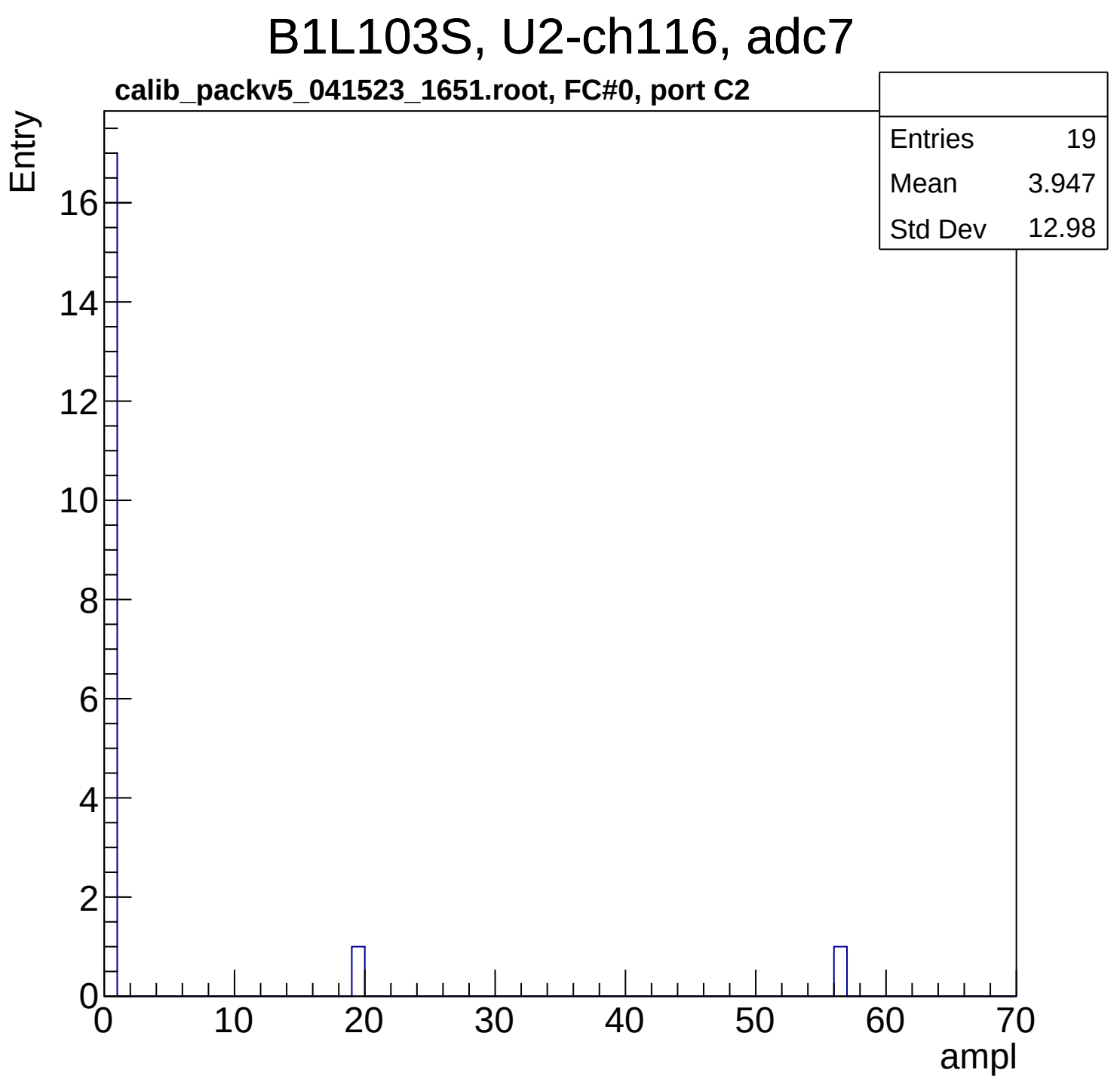

B1L103S, U2-ch116, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 36.48
Std Dev 12.48
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

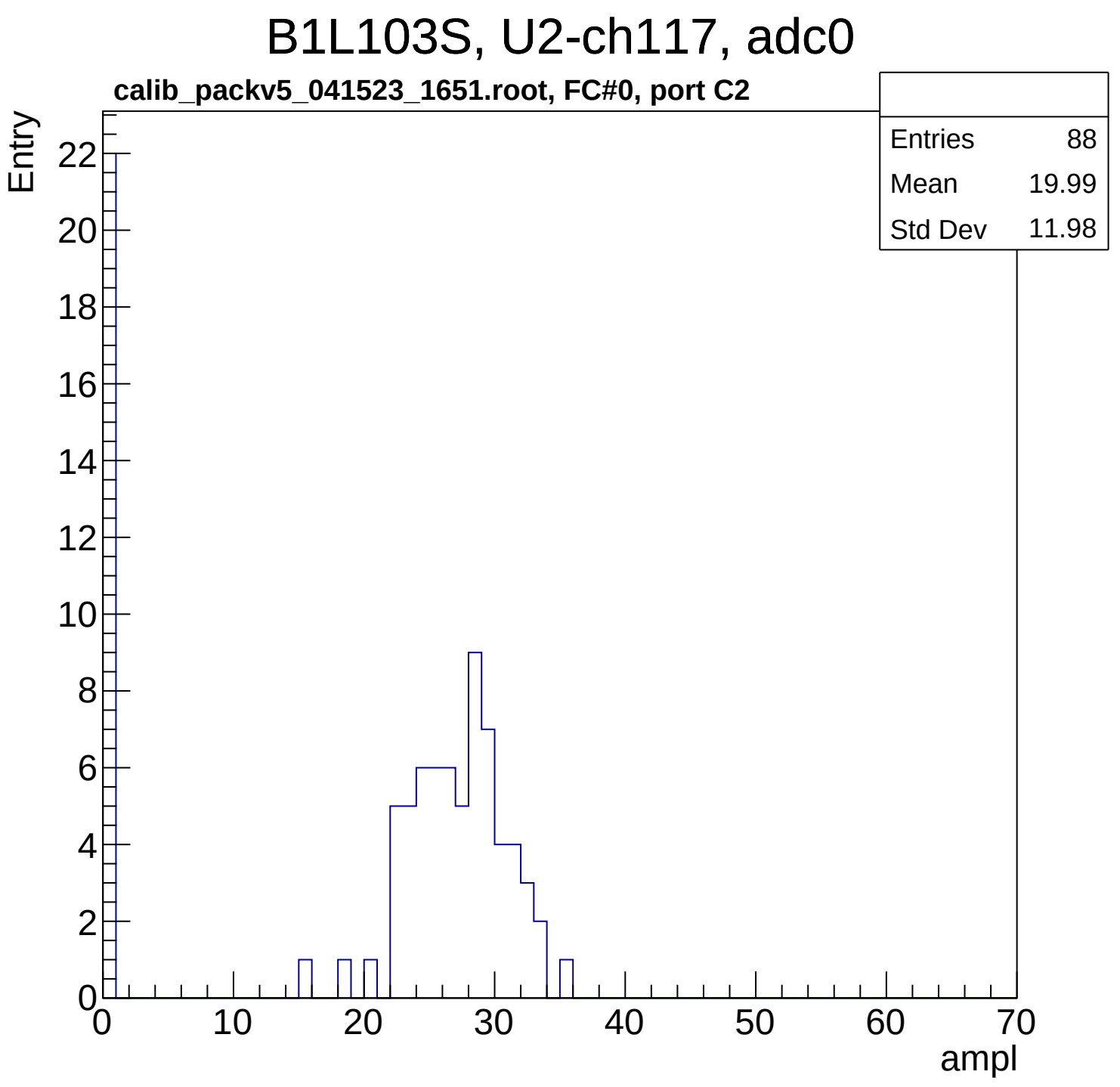

B1L103S, U2-ch116, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 40.2
Std Dev 16.65
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

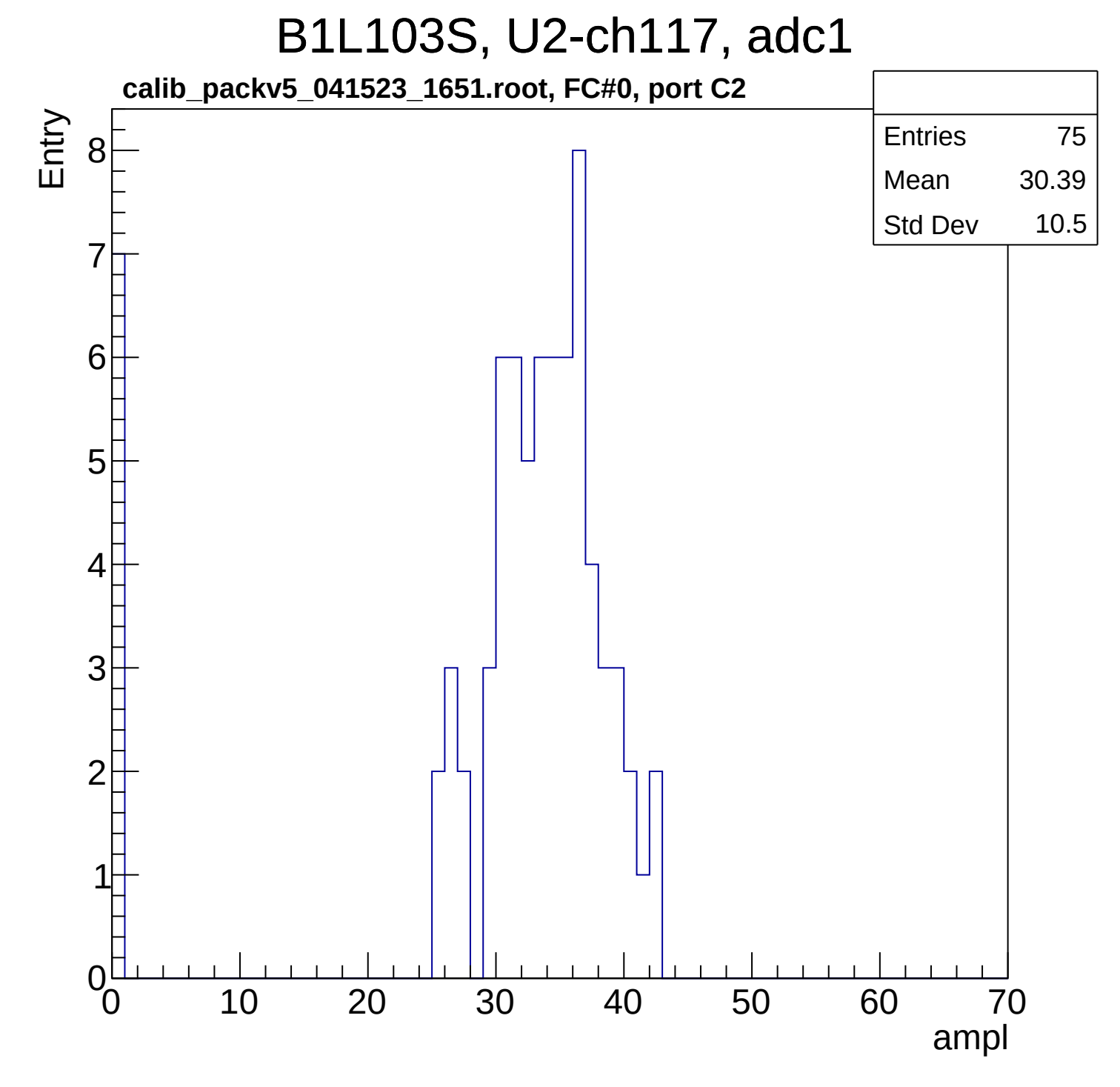

B1L103S, U2-ch116, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 52.21
Std Dev 4.025
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

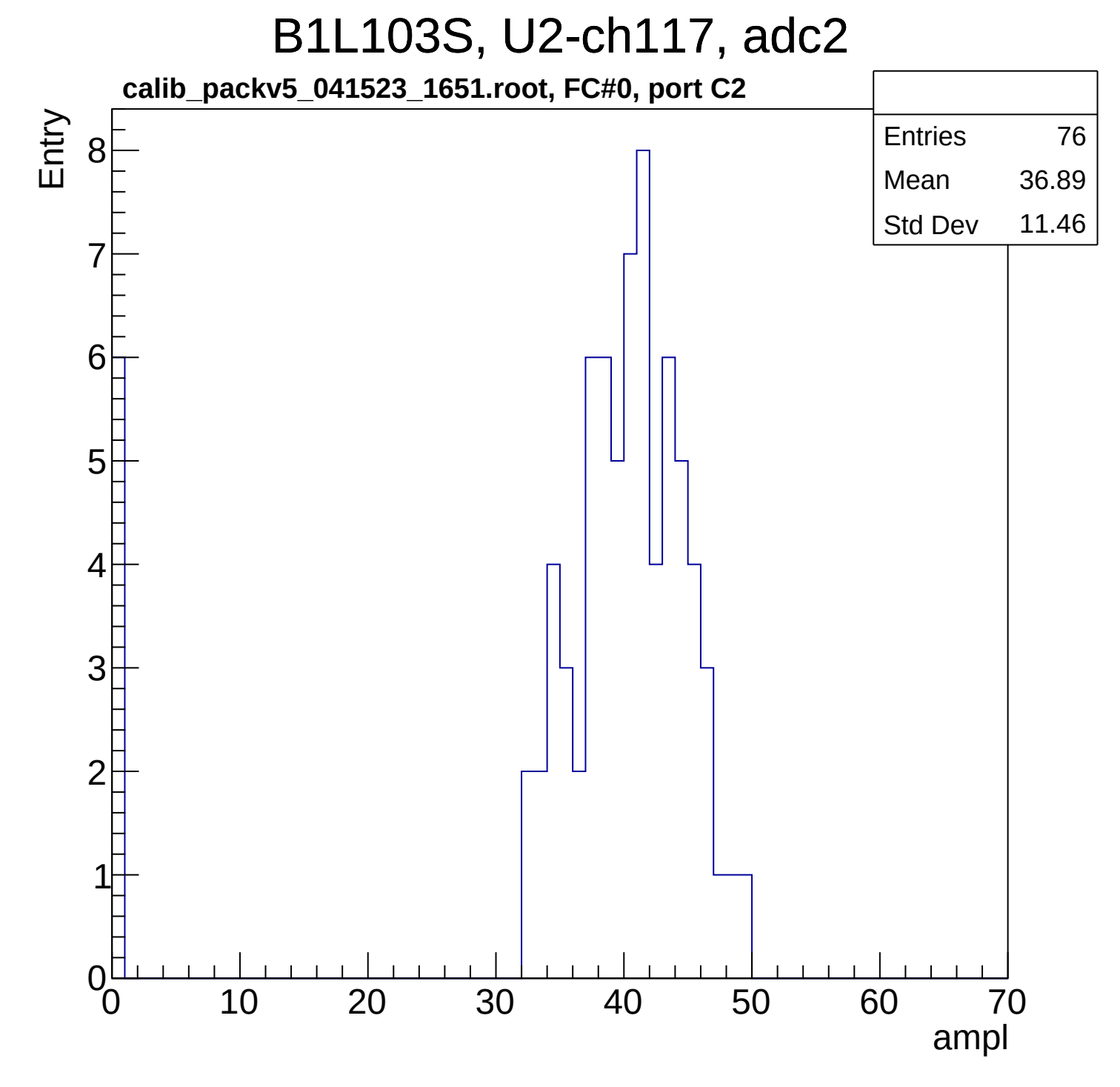

B1L103S, U2-ch116, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 57.14
Std Dev 7.593
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

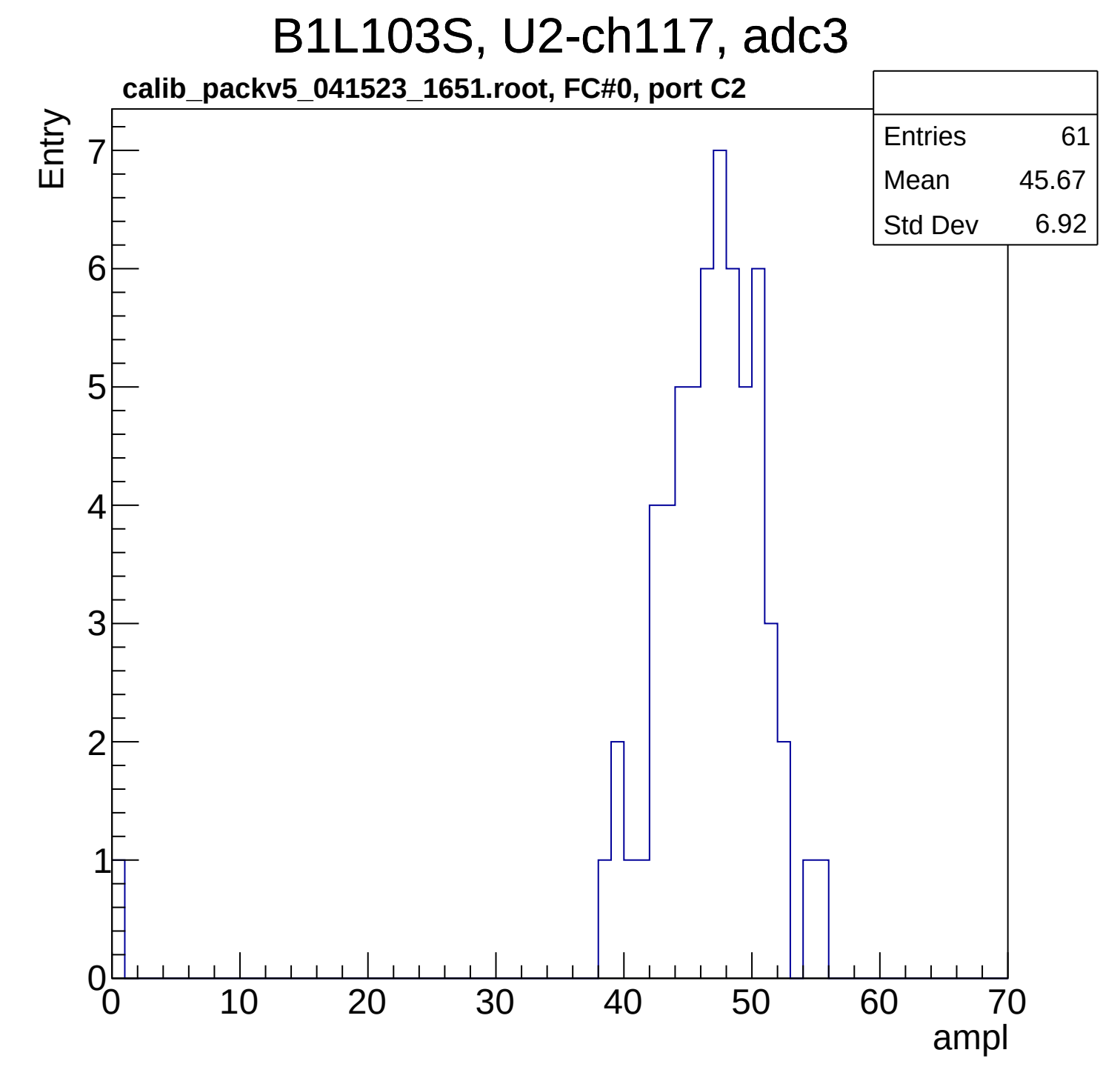

B1L103S, U2-ch116, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 61.79
Std Dev 1.206
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

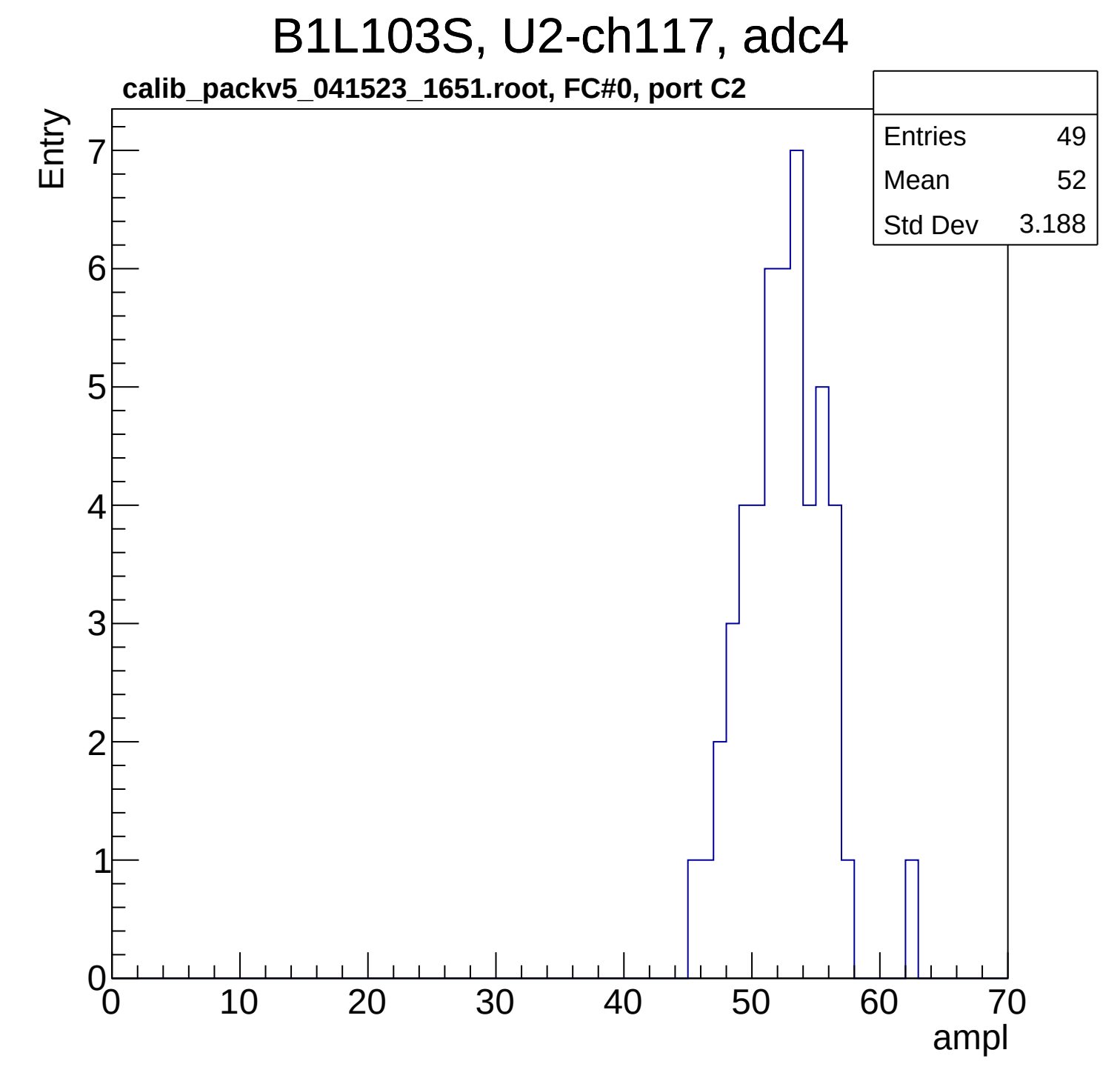

B1L103S, U2-ch116, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.947
Std Dev 12.98
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

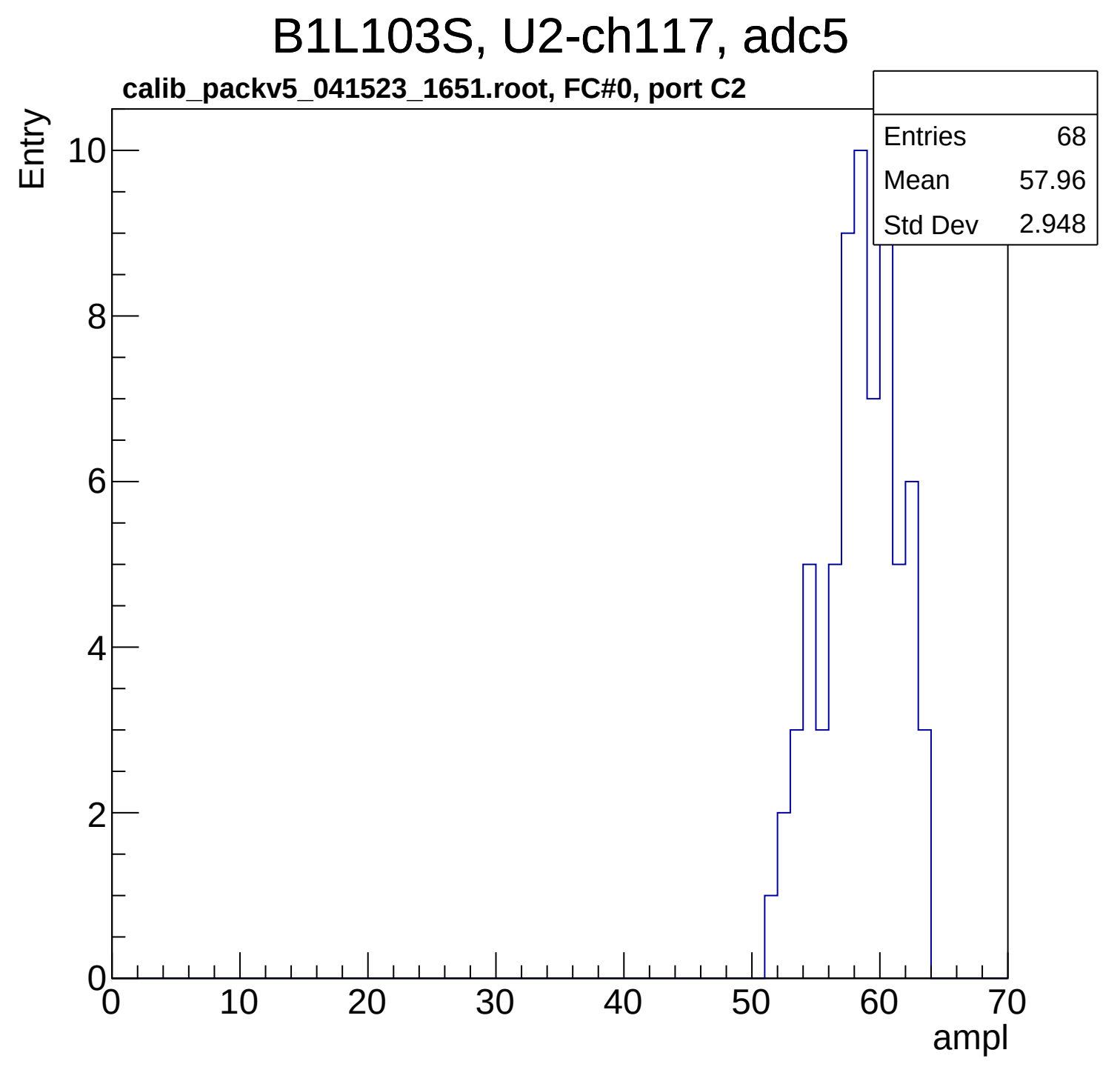

B1L103S, U2-ch117, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 19.99
Std Dev 11.98
Entry
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70
ampl

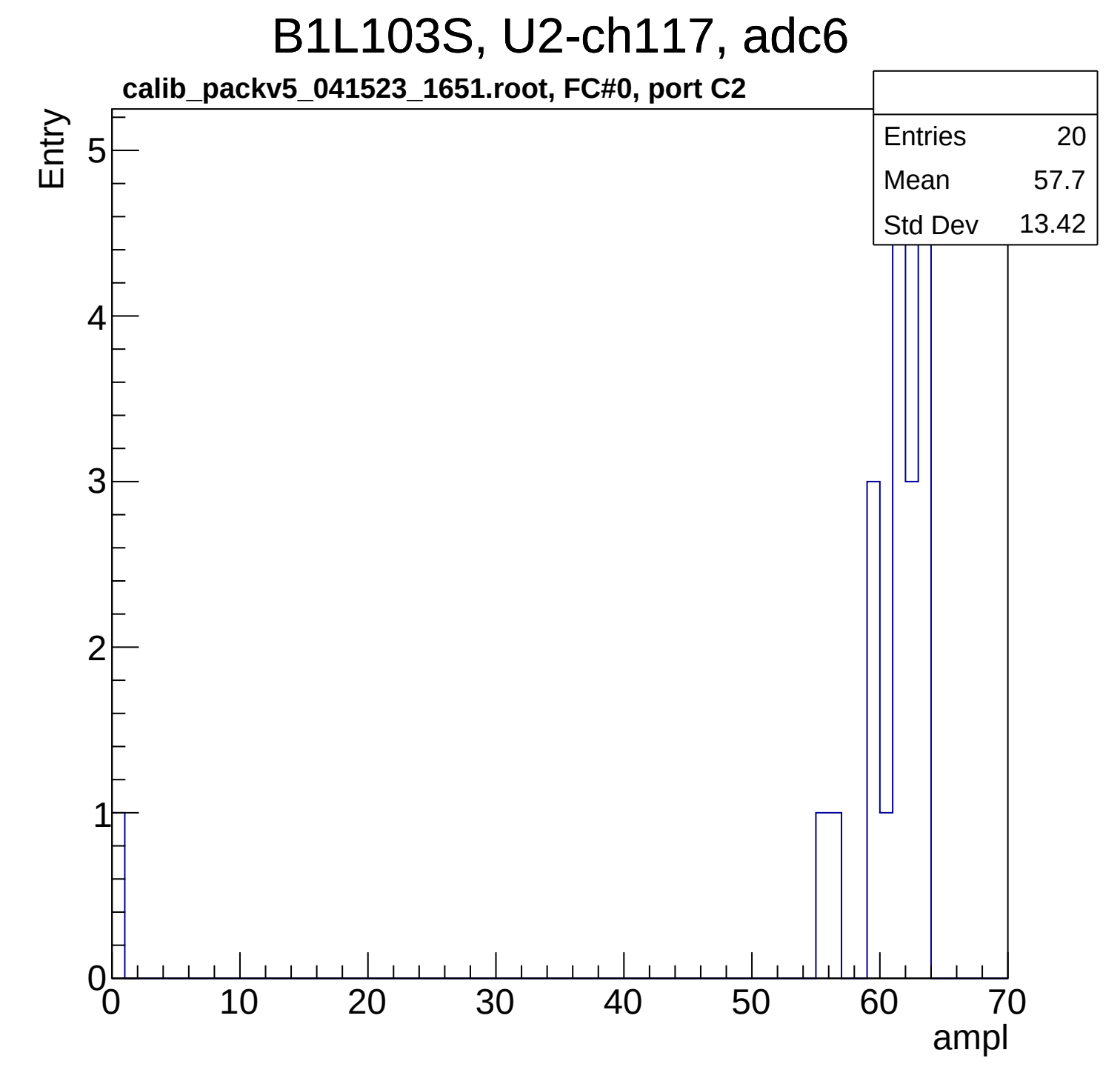

B1L103S, U2-ch117, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 30.39
Std Dev 10.5
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

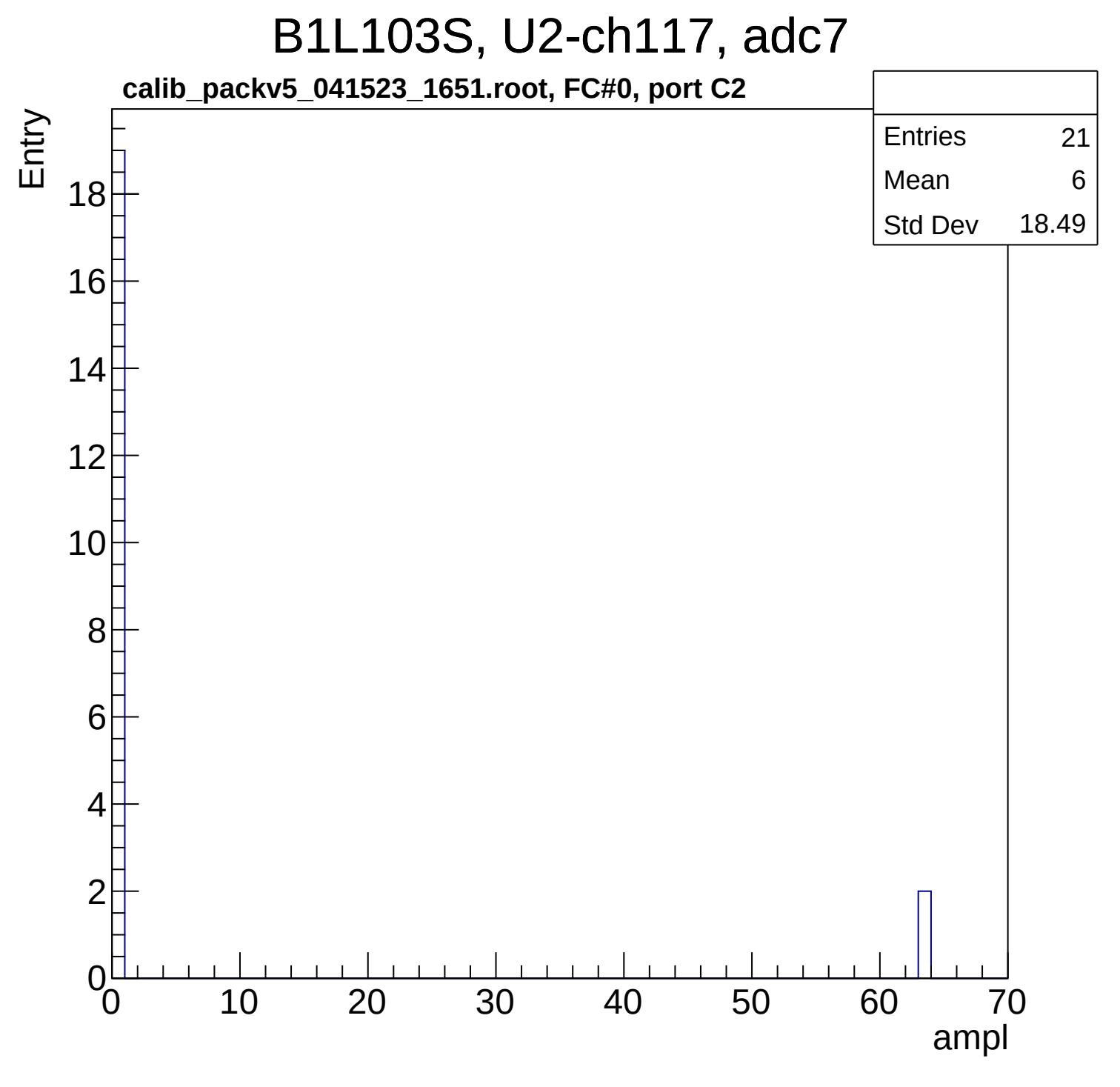

B1L103S, U2-ch117, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 36.89
Std Dev 11.46
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

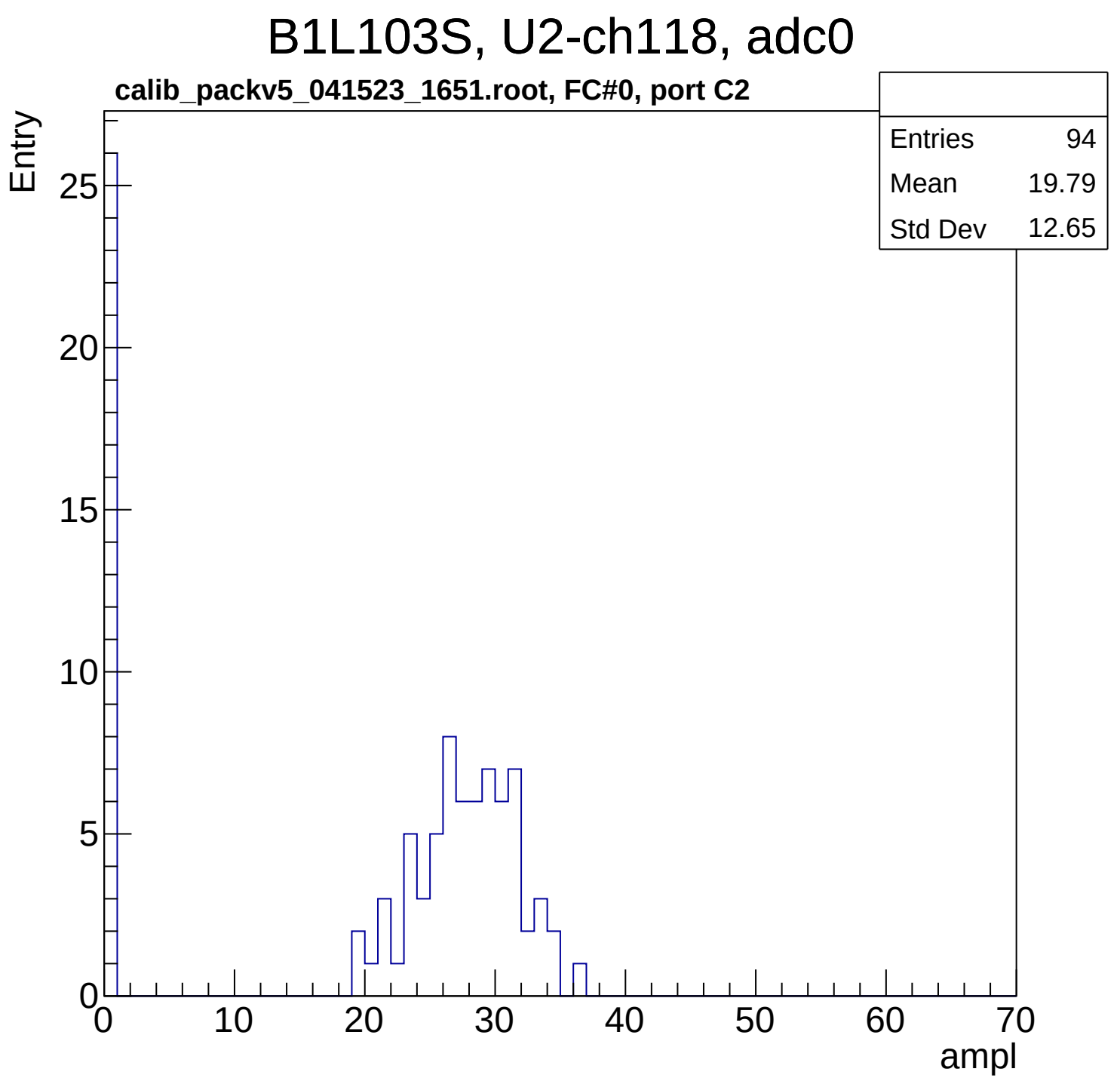

B1L103S, U2-ch117, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 45.67
Std Dev 6.92
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

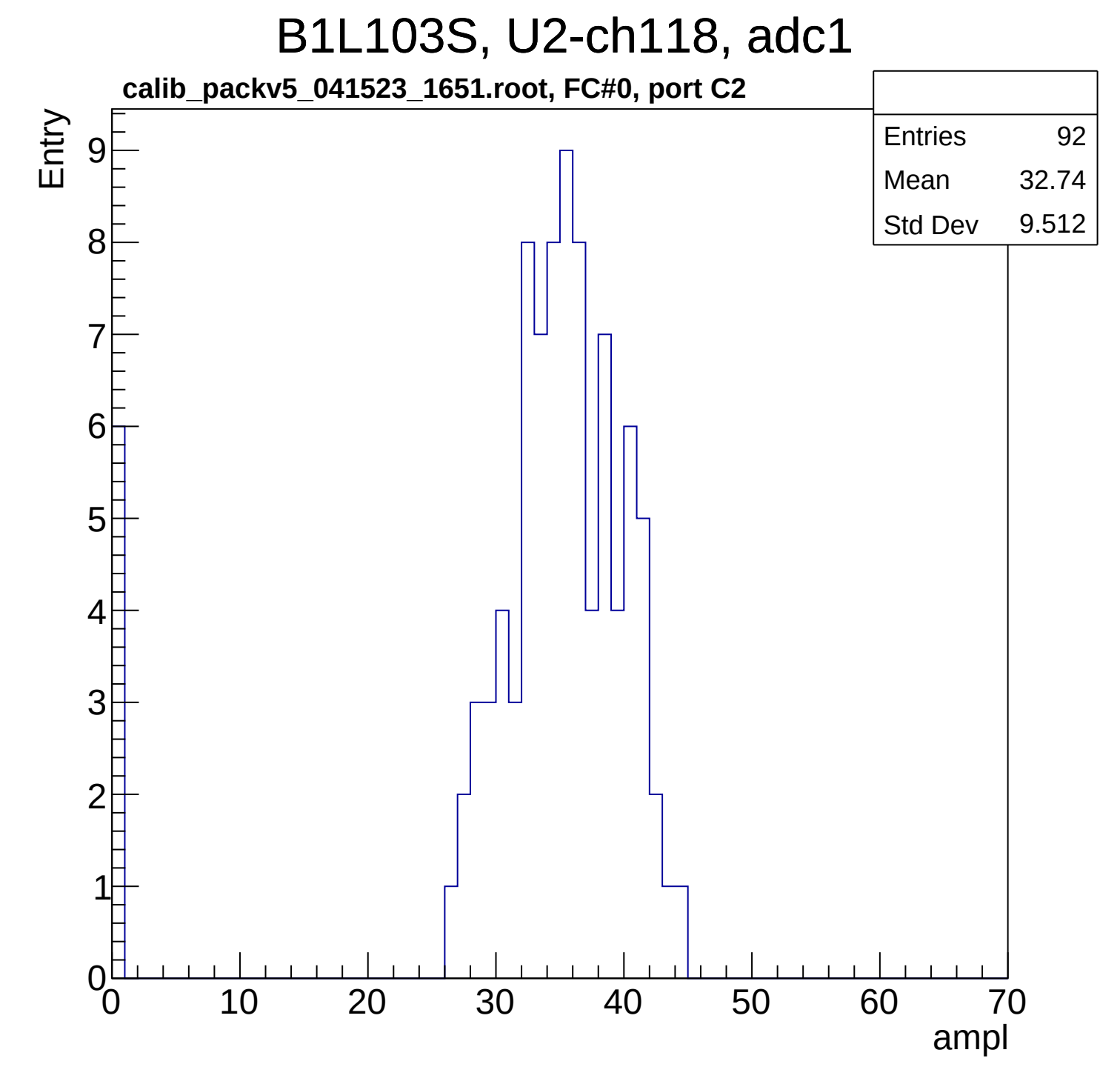

B1L103S, U2-ch117, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 52
Std Dev 3.188
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

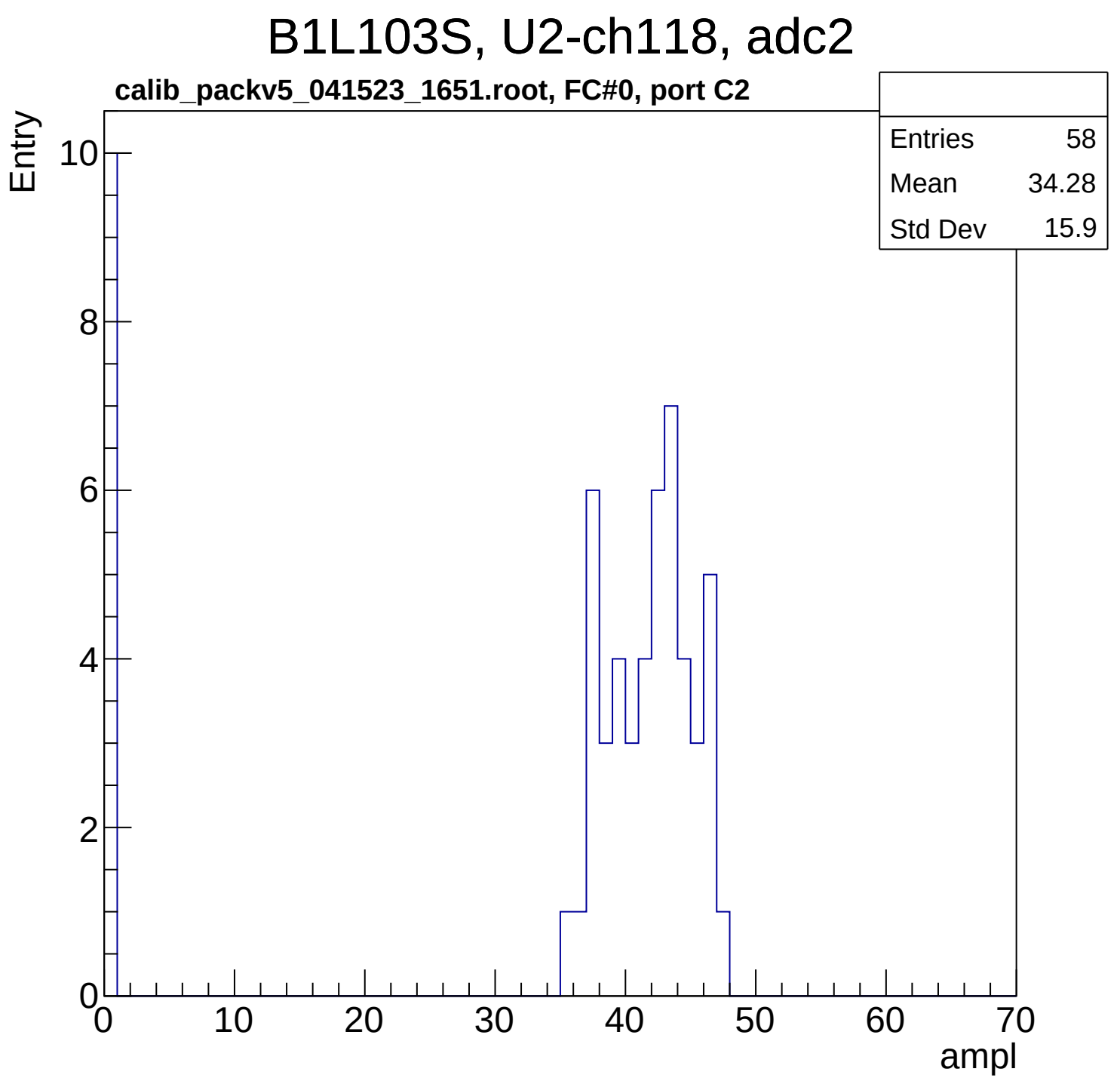

B1L103S, U2-ch117, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 57.96
Std Dev 2.948
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

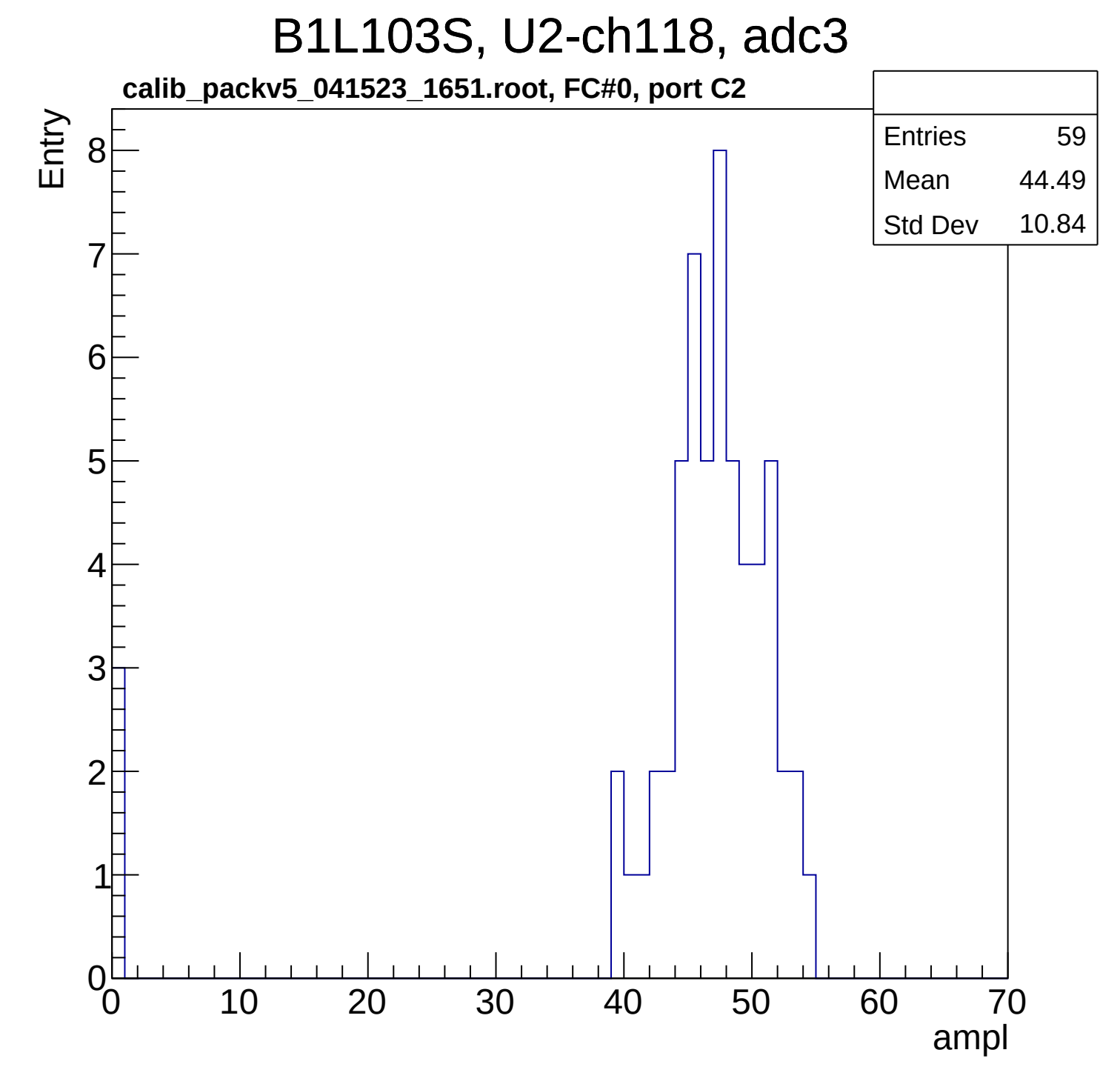

B1L103S, U2-ch117, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 57.7
Std Dev 13.42
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

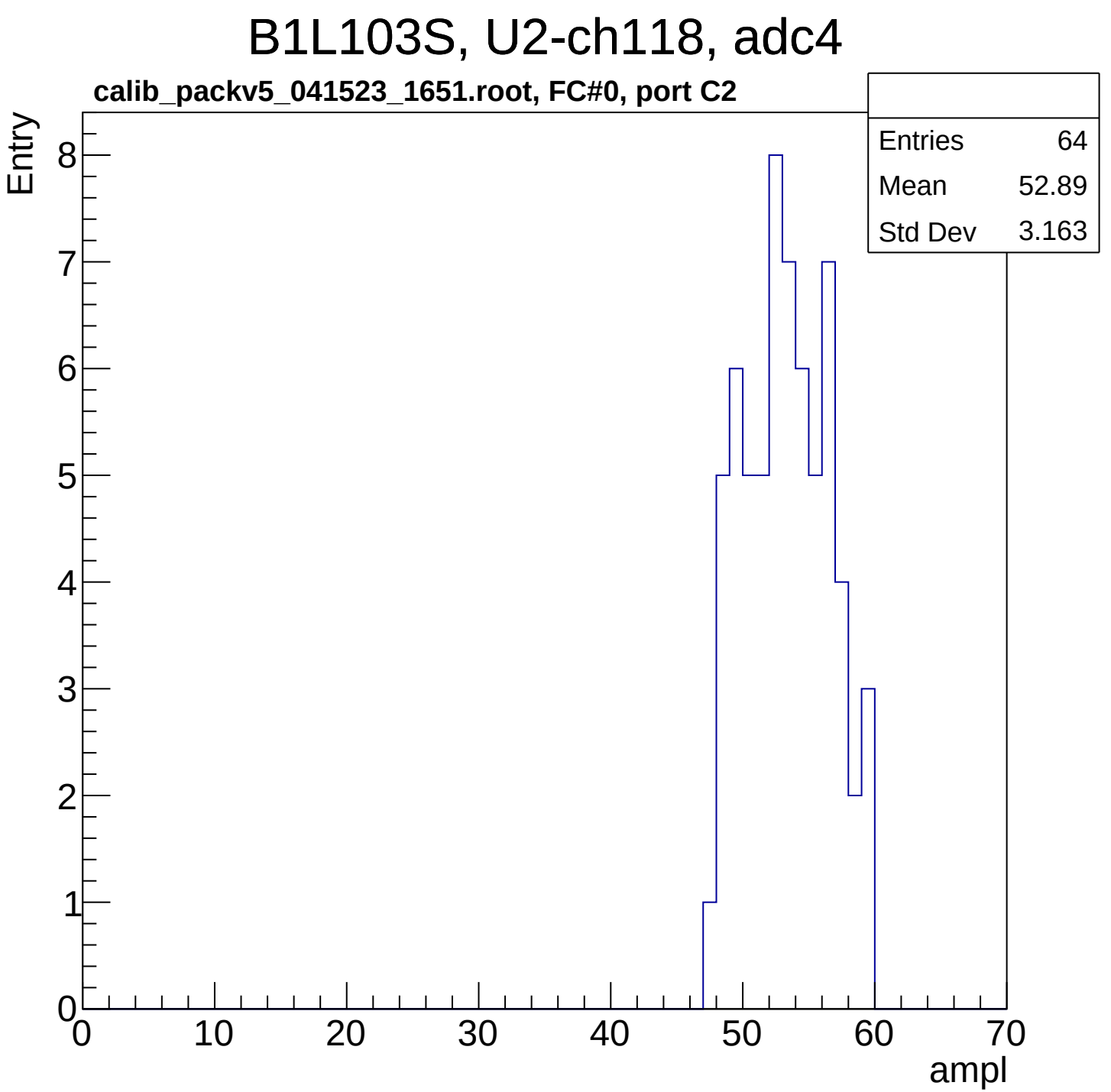

B1L103S, U2-ch117, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 6
Std Dev 18.49
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

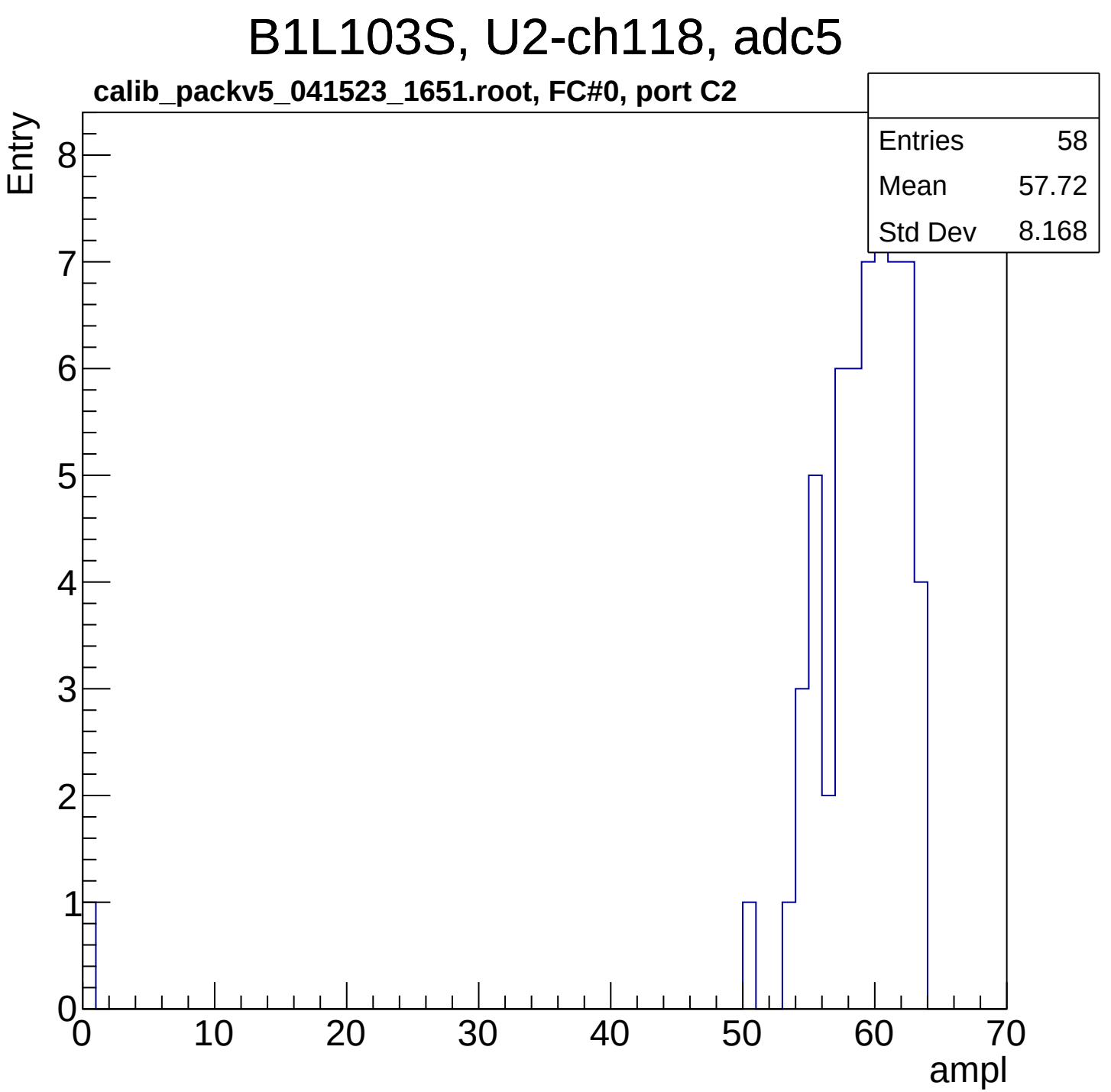

B1L103S, U2-ch118, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 19.79
Std Dev 12.65
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl

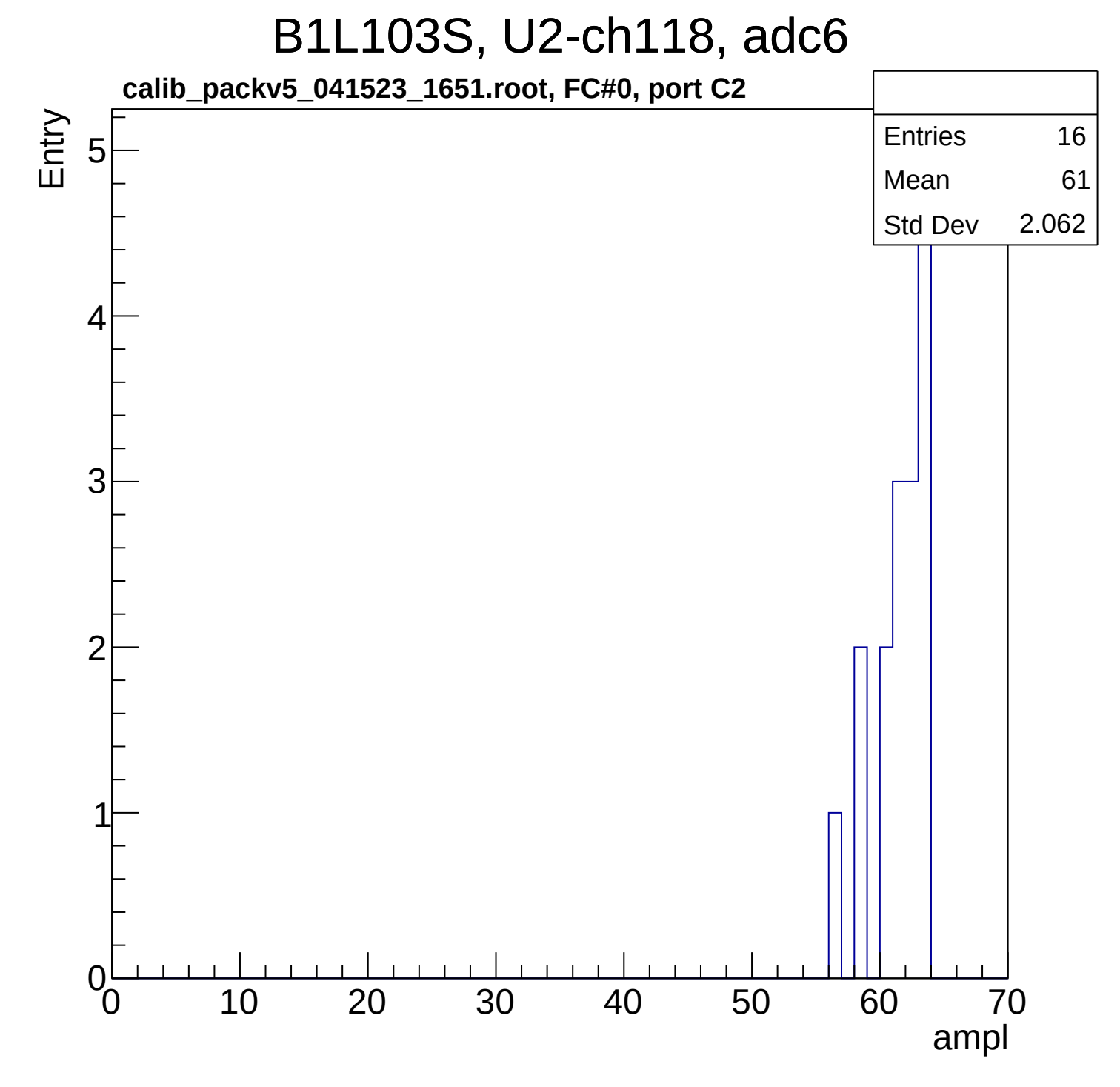

B1L103S, U2-ch118, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 32.74
Std Dev 9.512
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

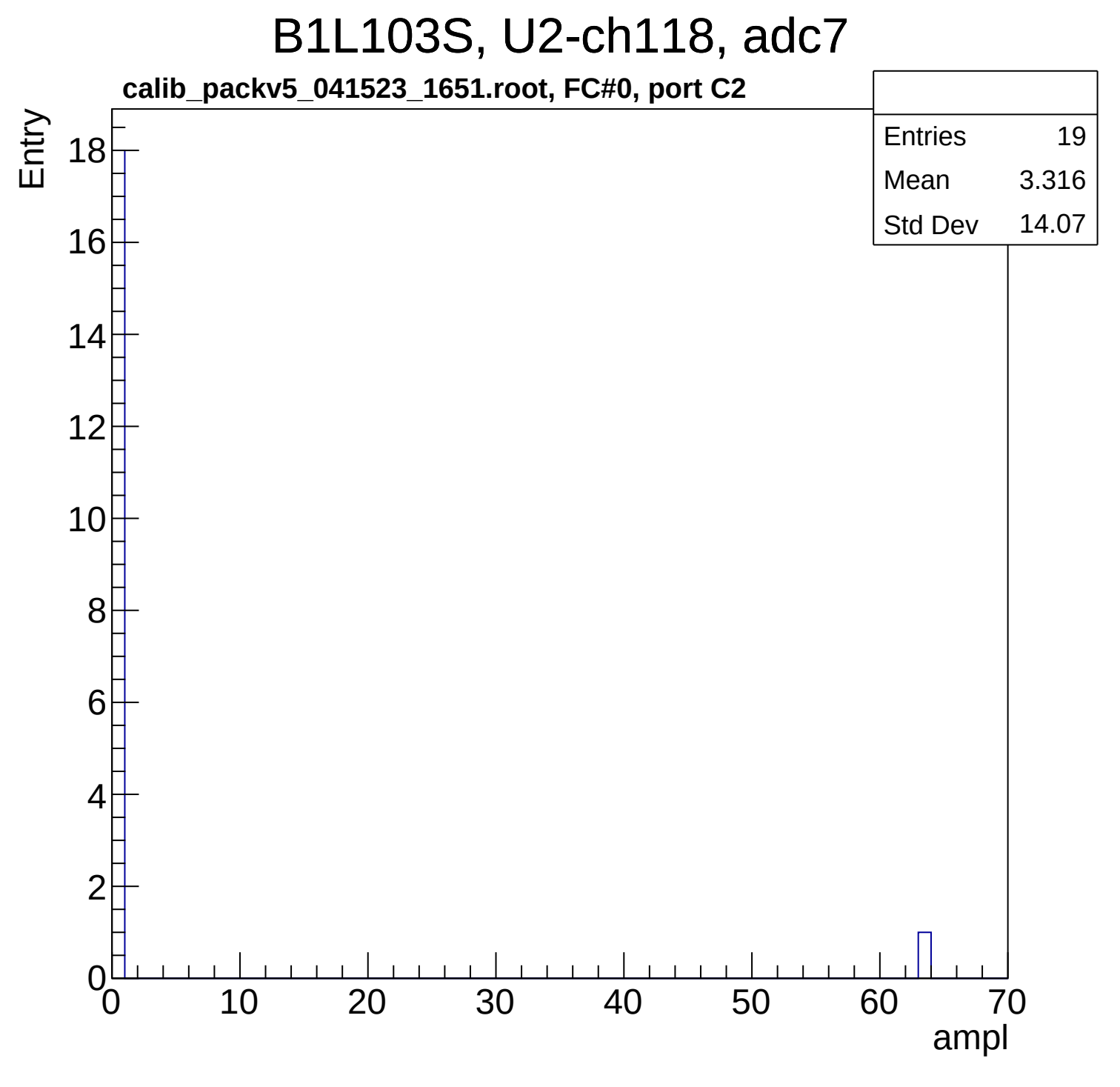

B1L103S, U2-ch118, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 34.28
Std Dev 15.9
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

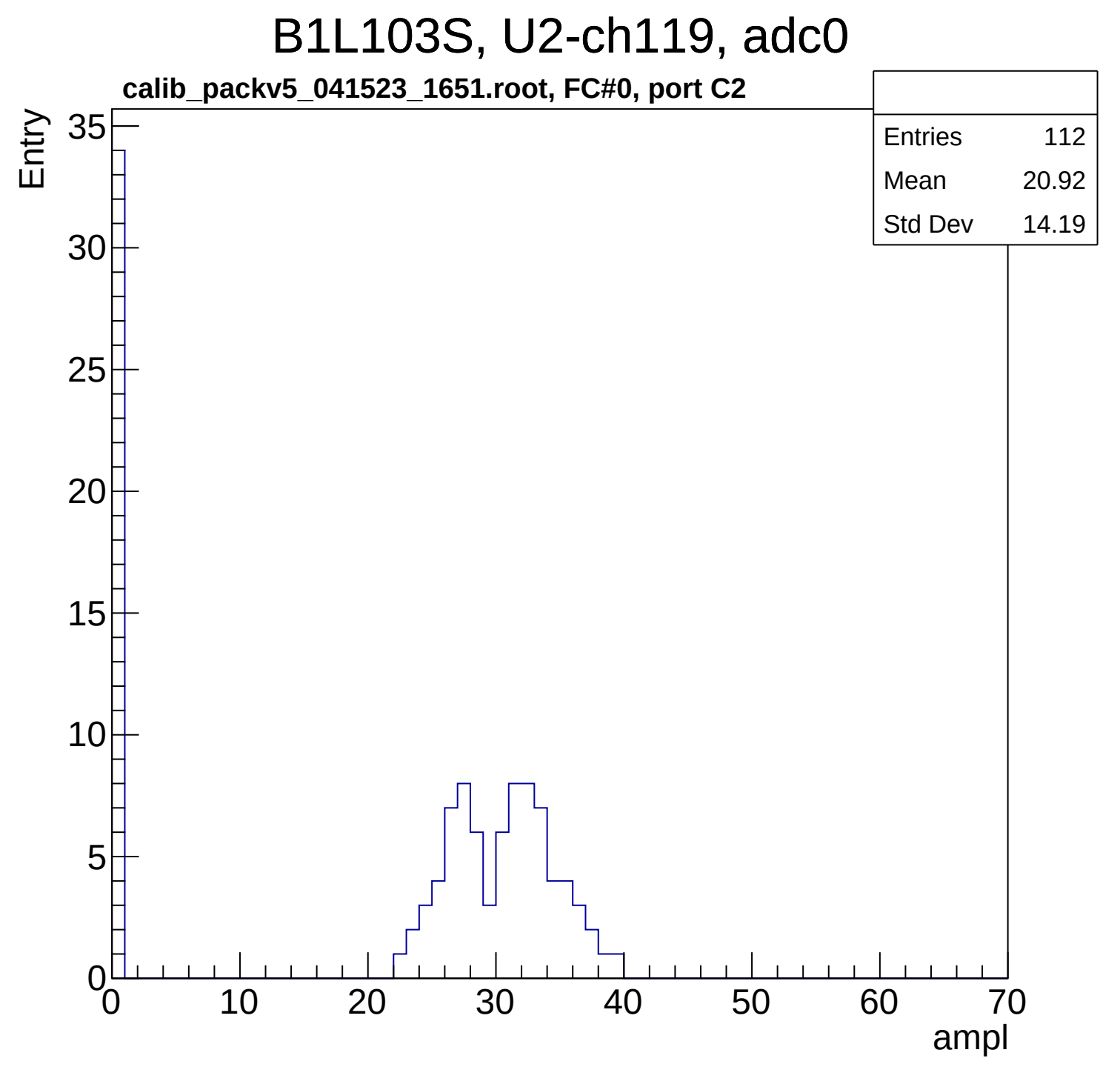

B1L103S, U2-ch118, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 44.49
Std Dev 10.84
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

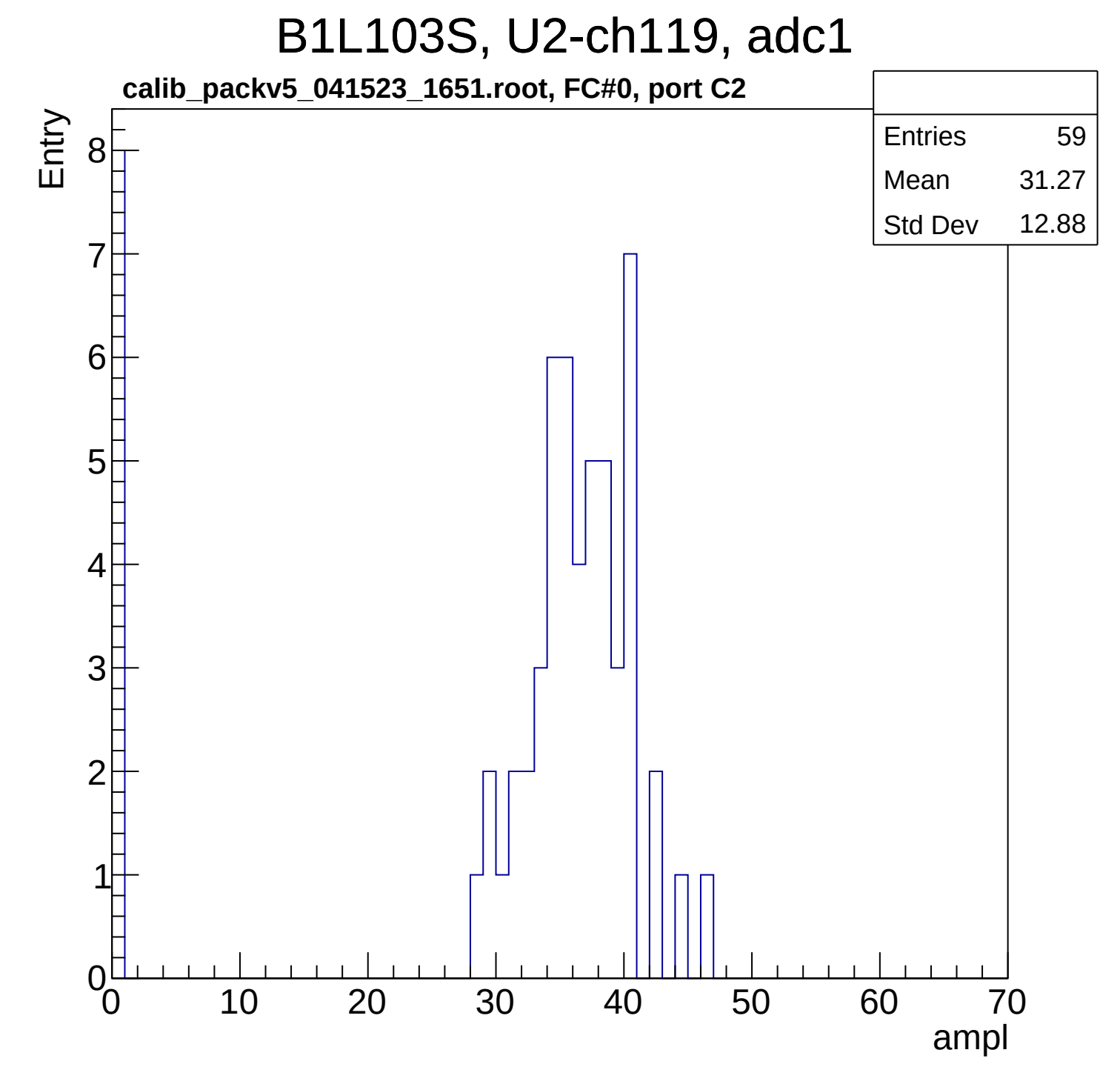

B1L103S, U2-ch118, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 52.89
Std Dev 3.163
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

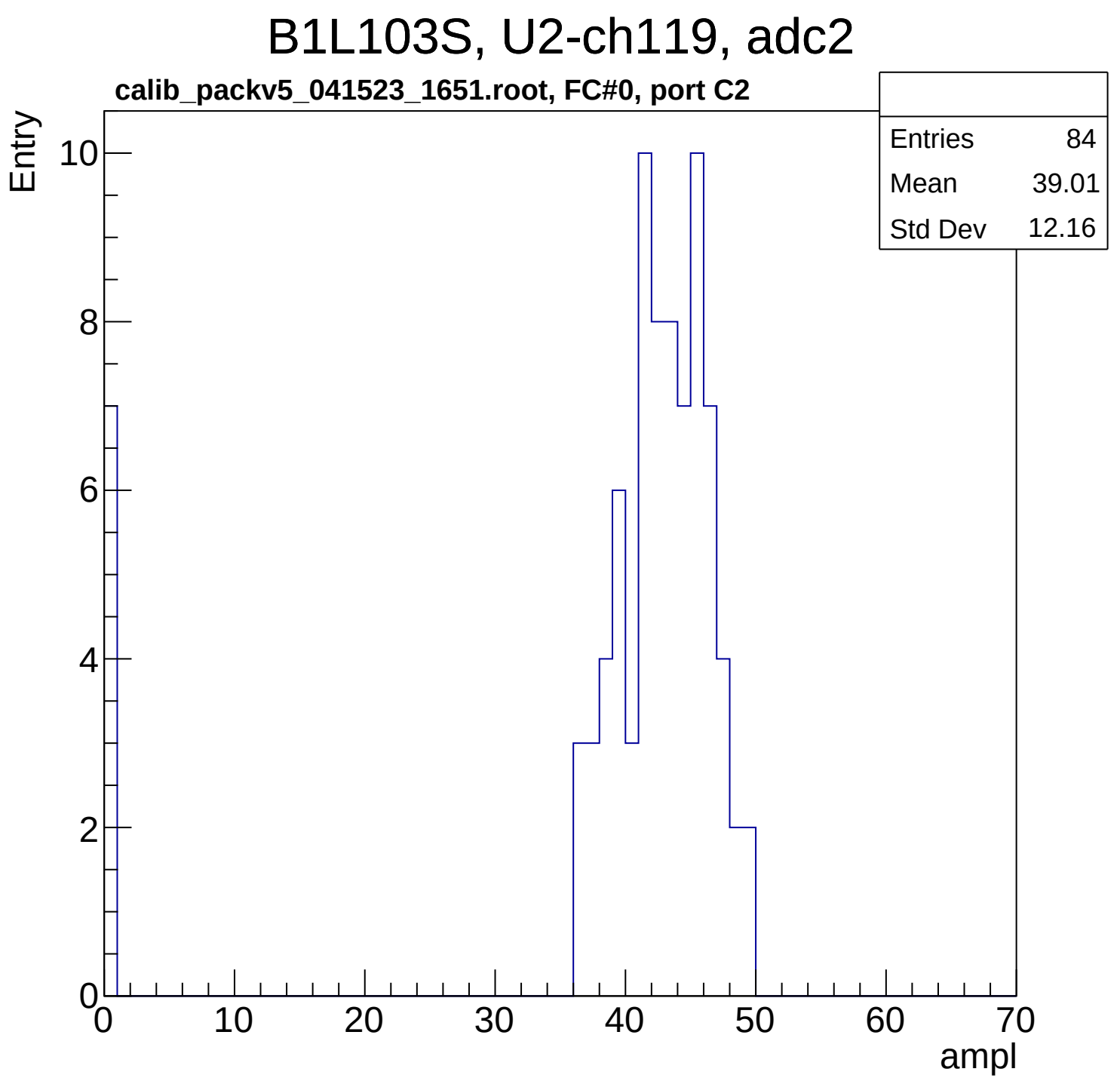

B1L103S, U2-ch118, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 57.72
Std Dev 8.168
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

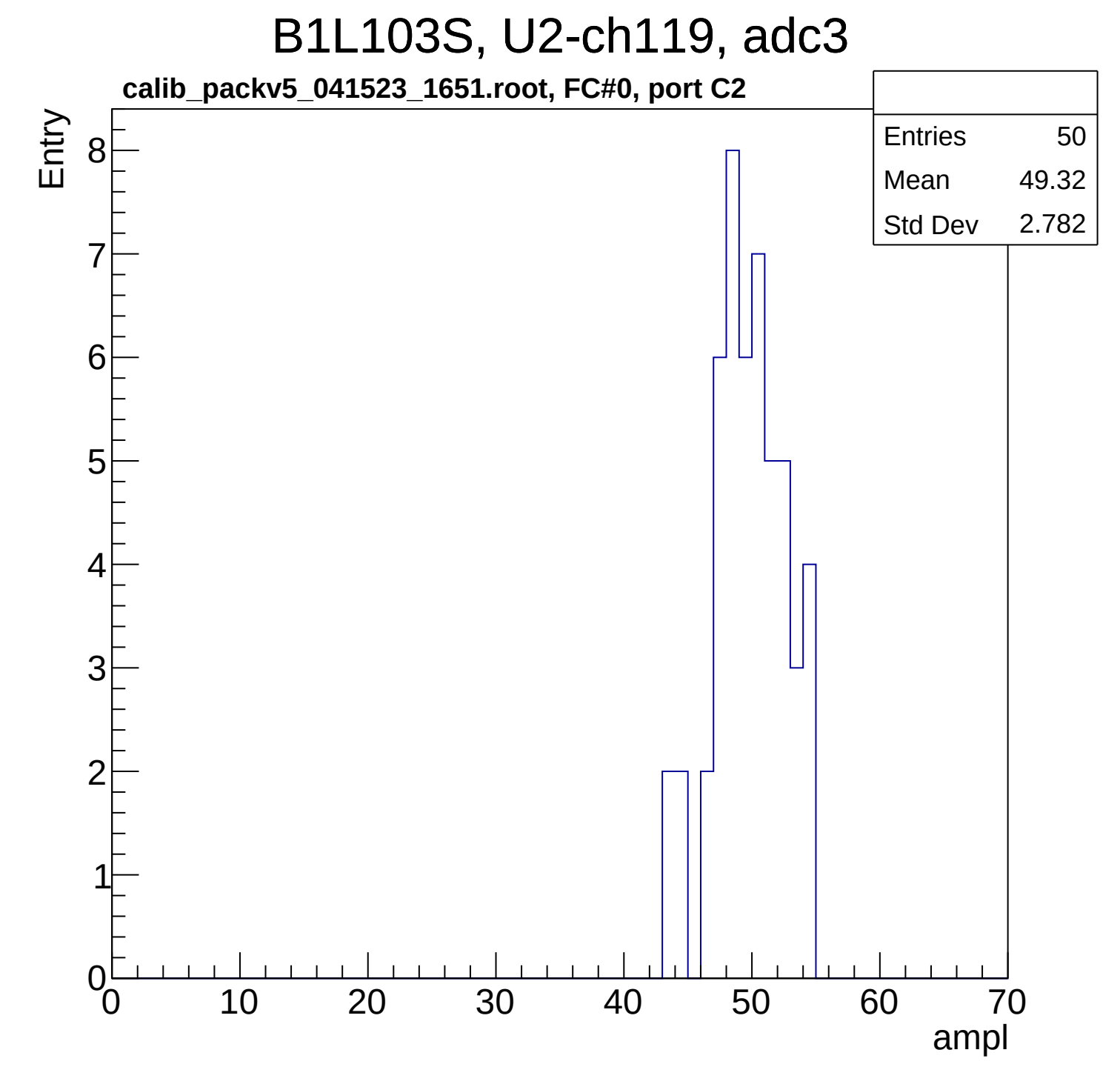

B1L103S, U2-ch118, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 61
Std Dev 2.062
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

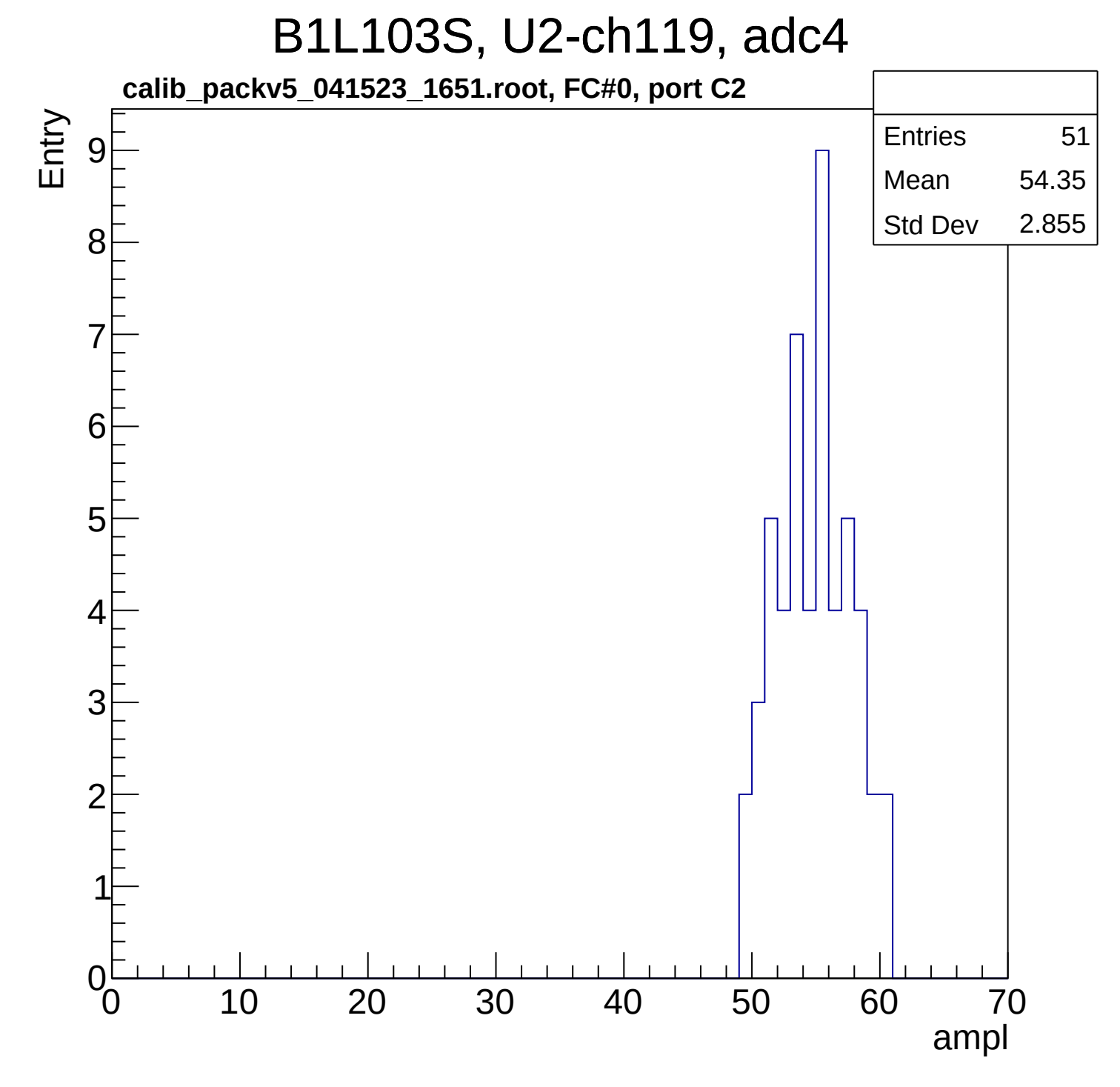

B1L103S, U2-ch118, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

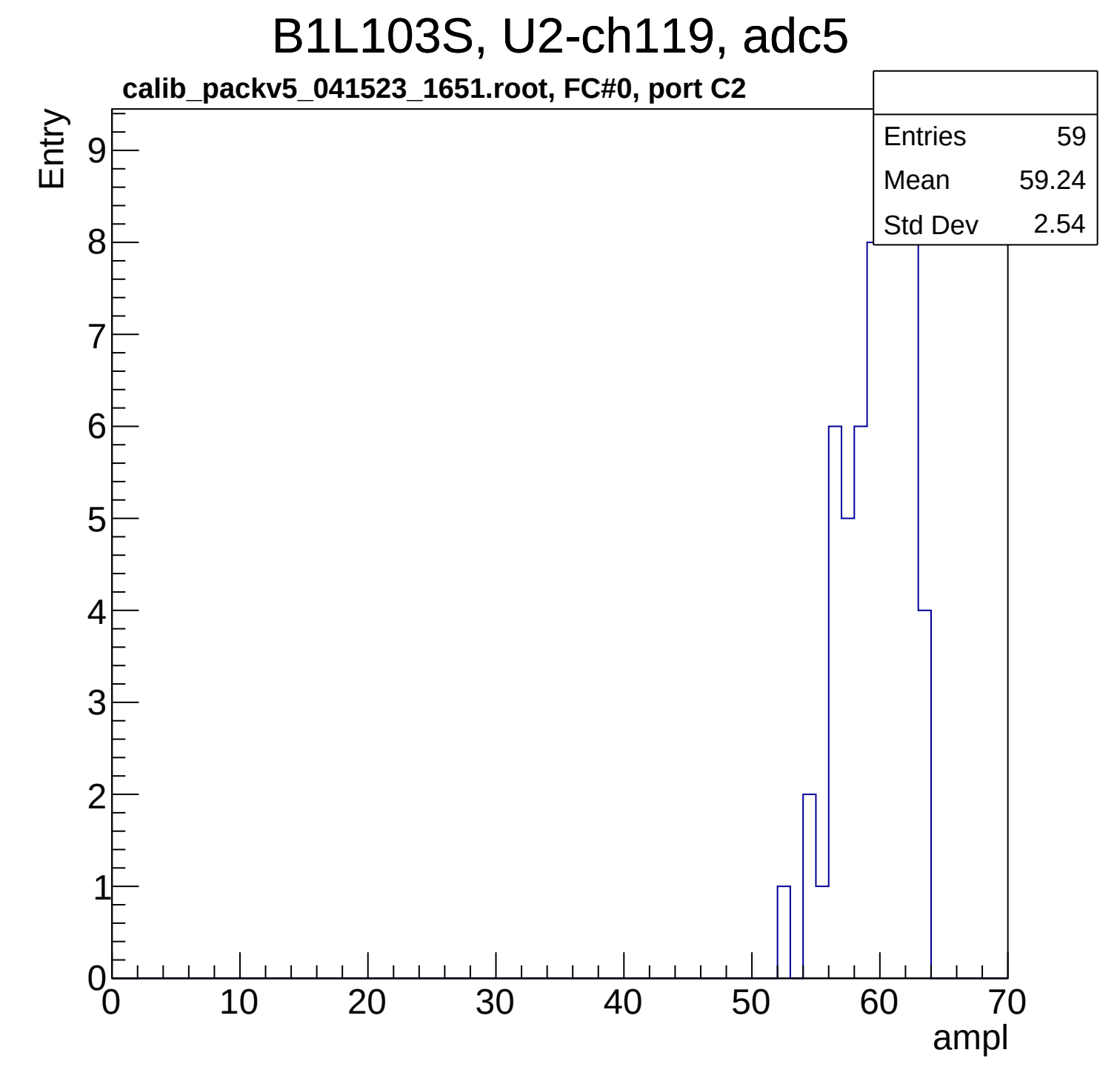

B1L103S, U2-ch119, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 112
Mean 20.92
Std Dev 14.19
Entry
ampl
0
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70

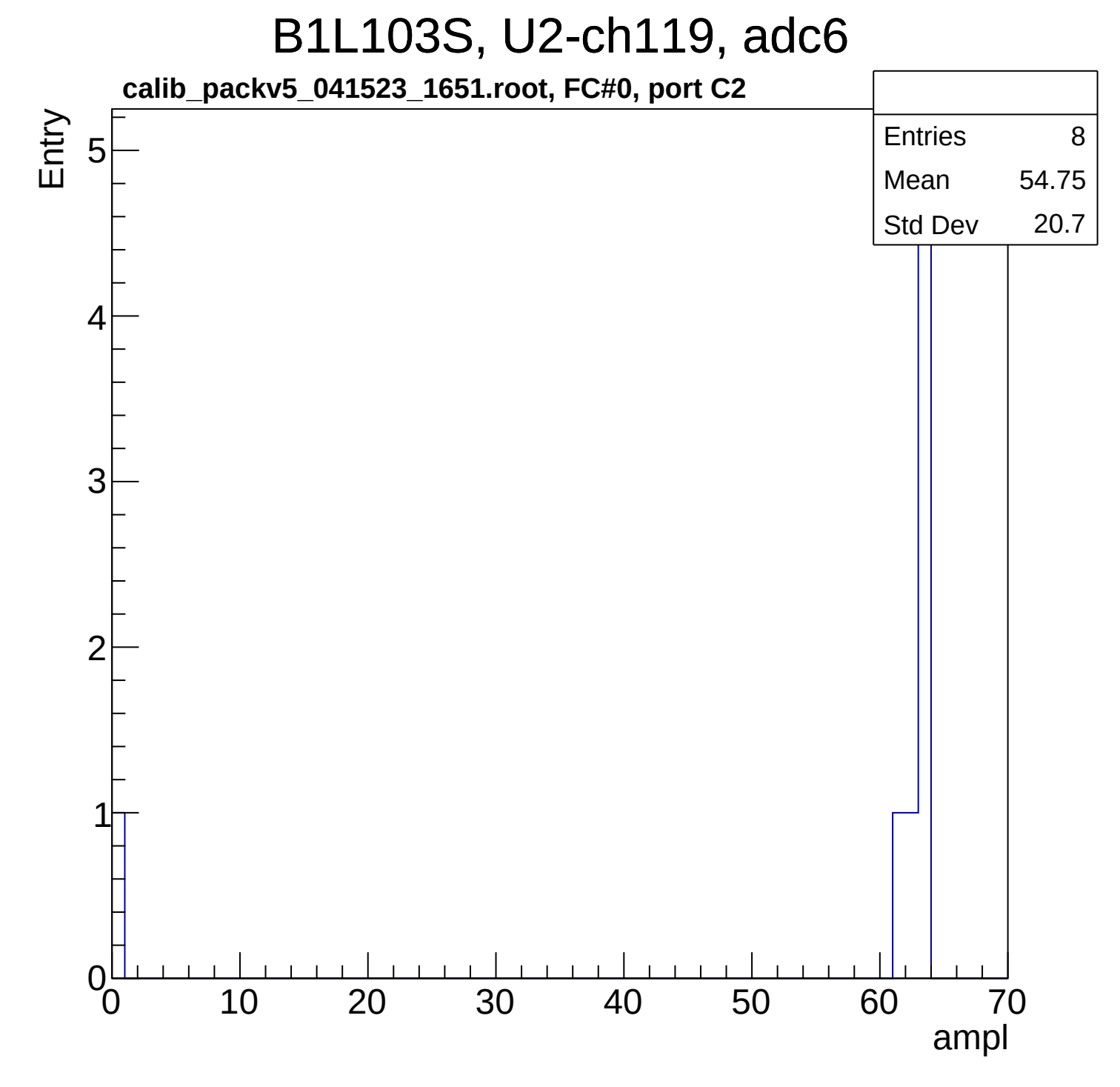

B1L103S, U2-ch119, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 31.27
Std Dev 12.88
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

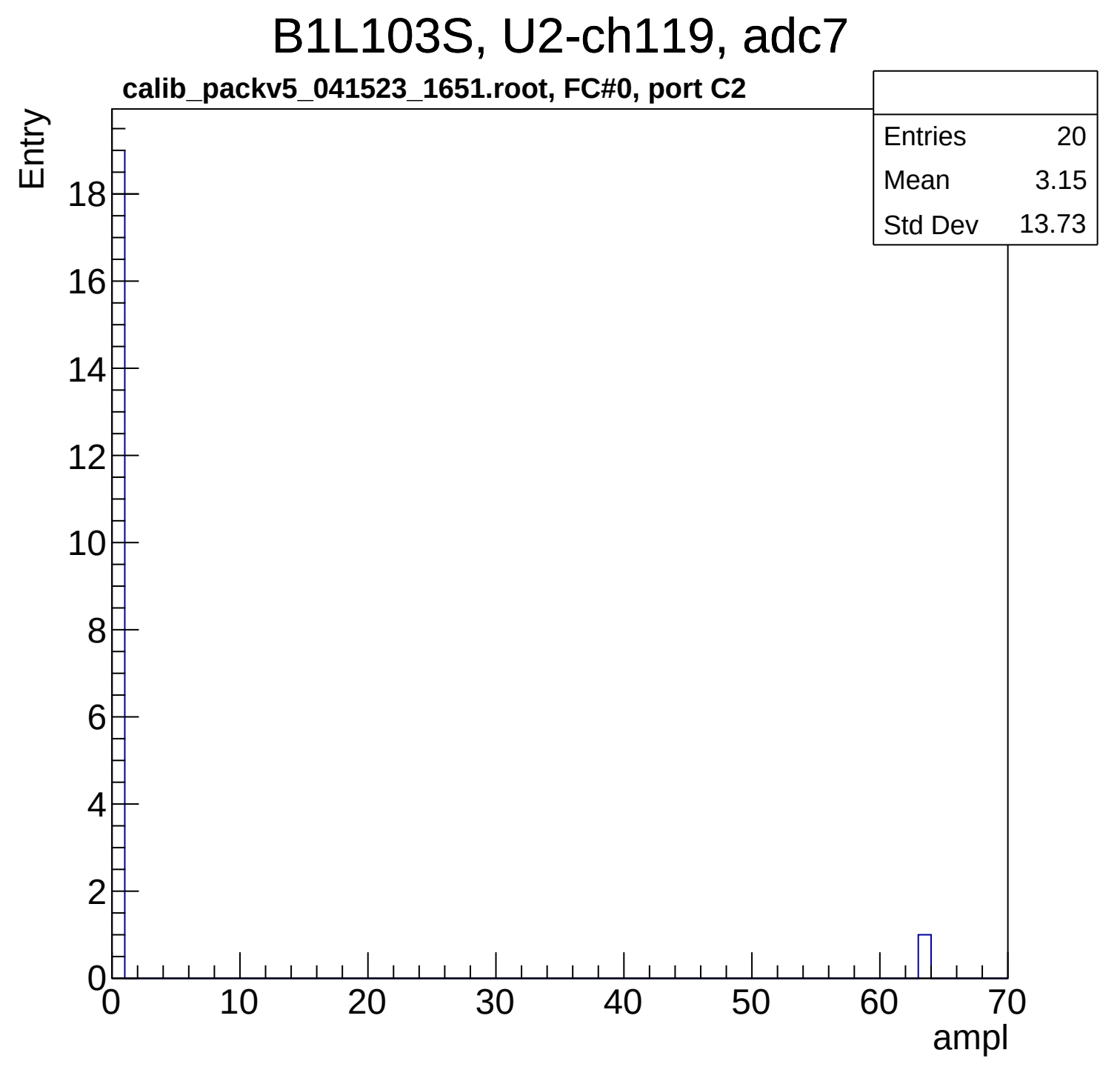

B1L103S, U2-ch119, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 39.01
Std Dev 12.16
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

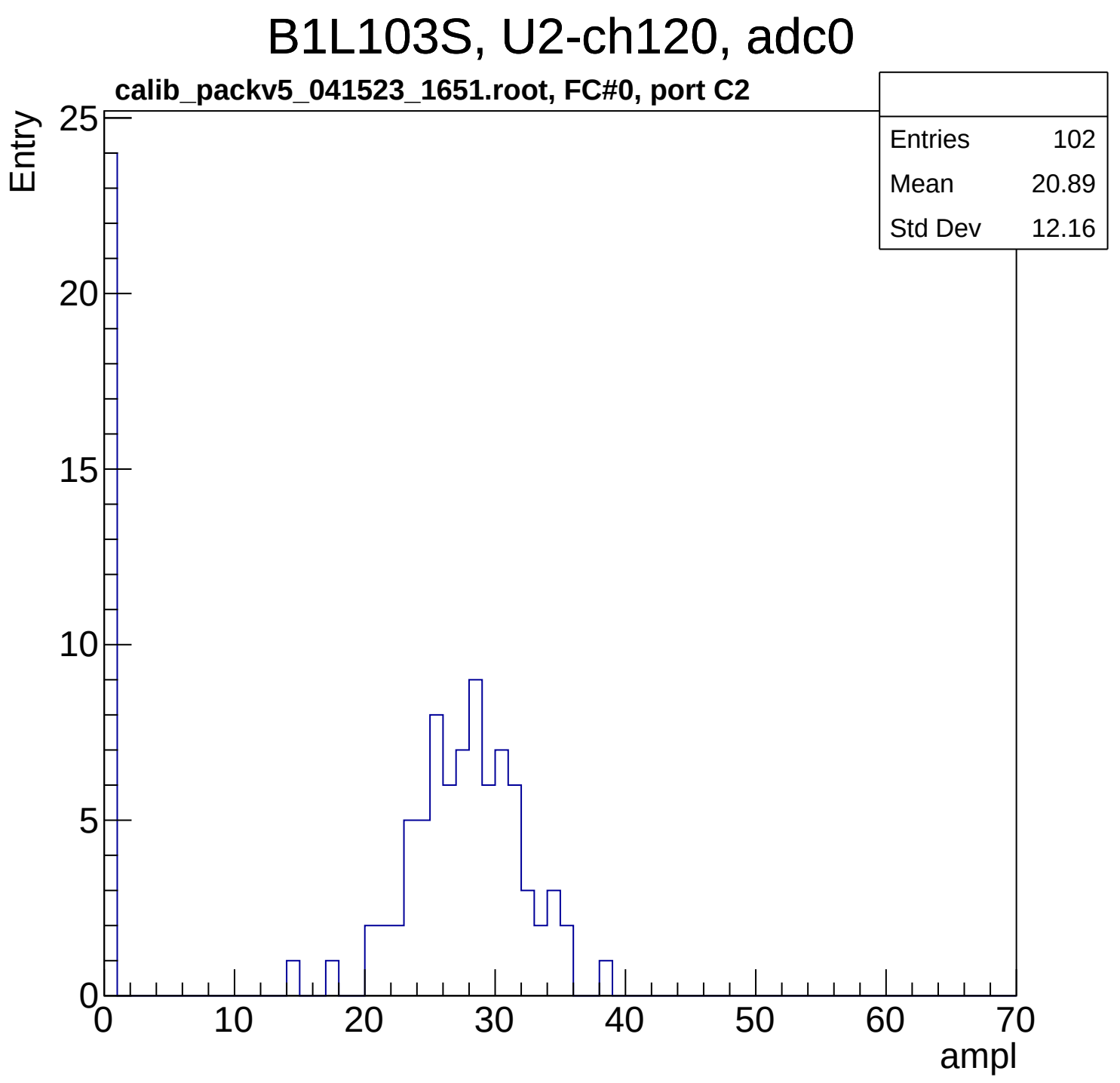

B1L103S, U2-ch119, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 49.32
Std Dev 2.782
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

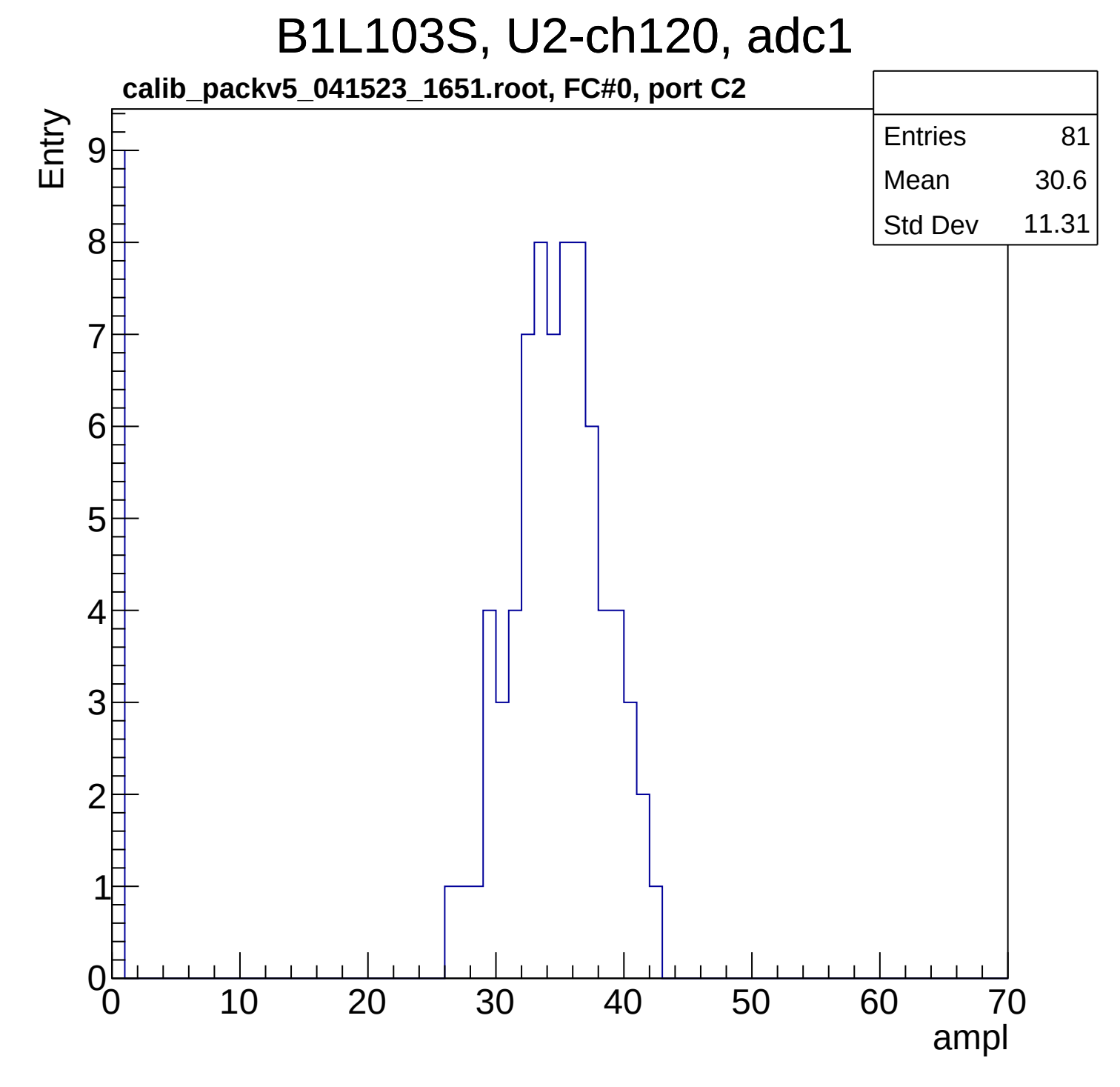

B1L103S, U2-ch119, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 54.35
Std Dev 2.855
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

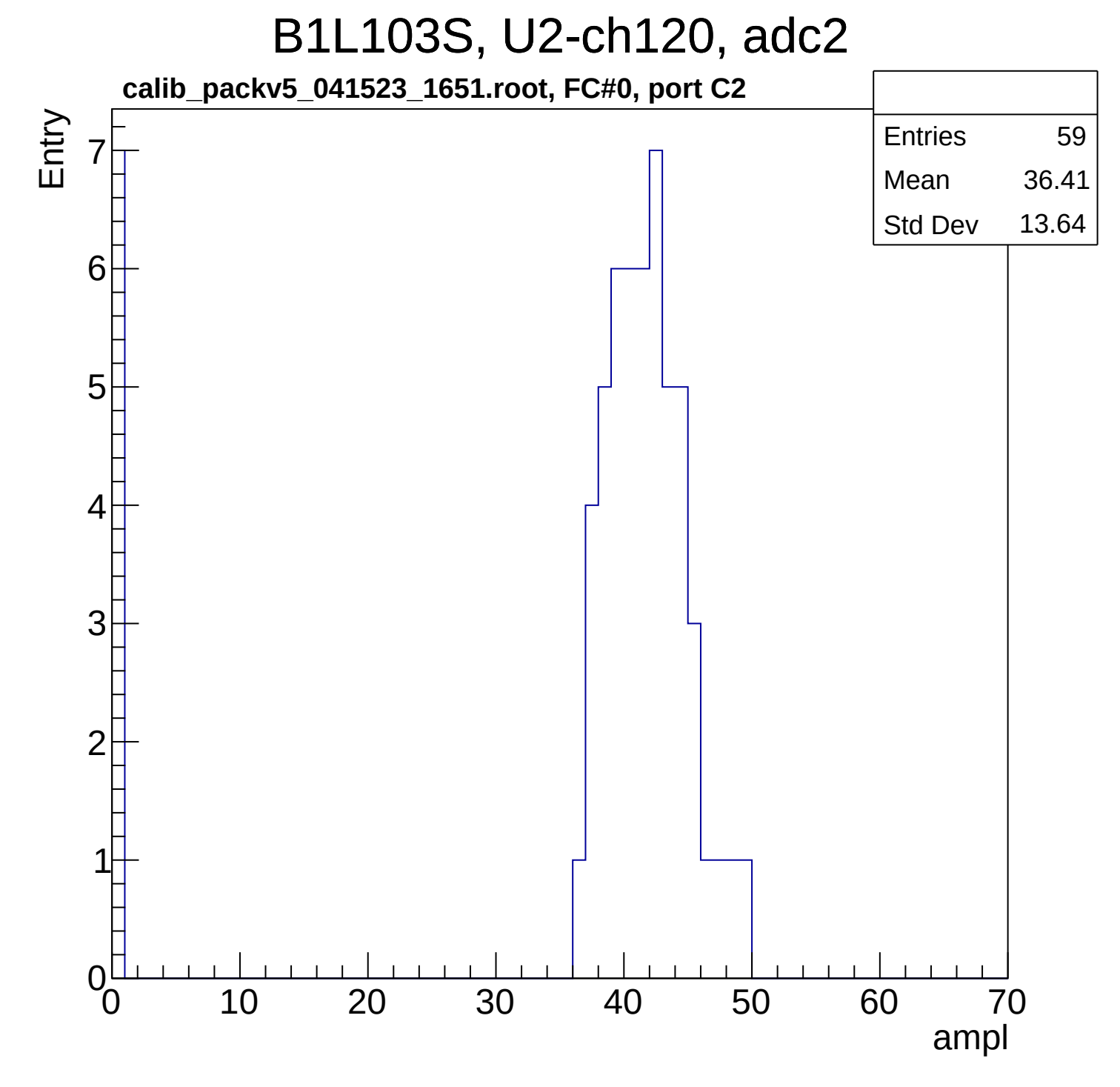

B1L103S, U2-ch119, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 59.24
Std Dev 2.54
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

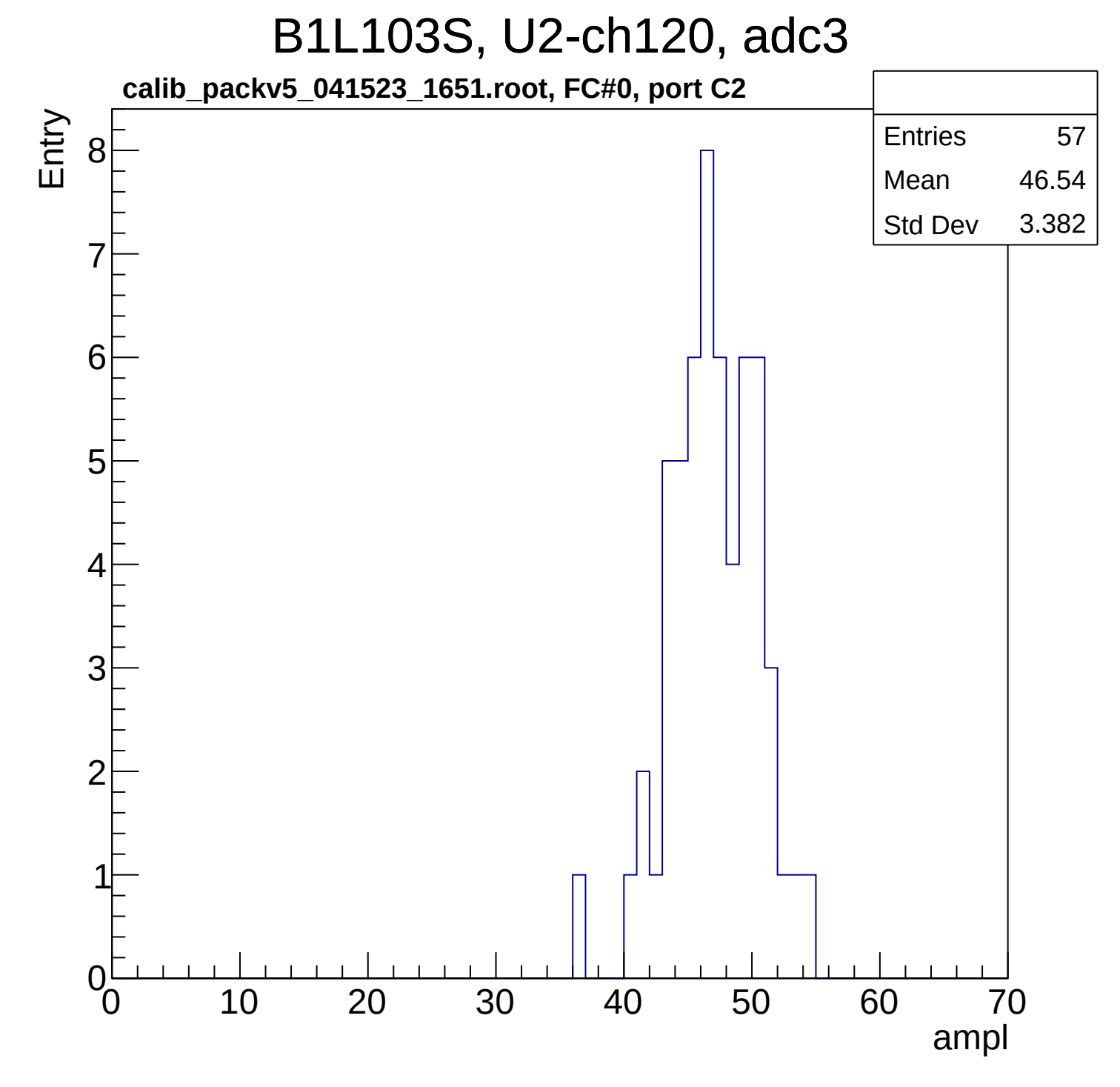

B1L103S, U2-ch119, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 54.75
Std Dev 20.7
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

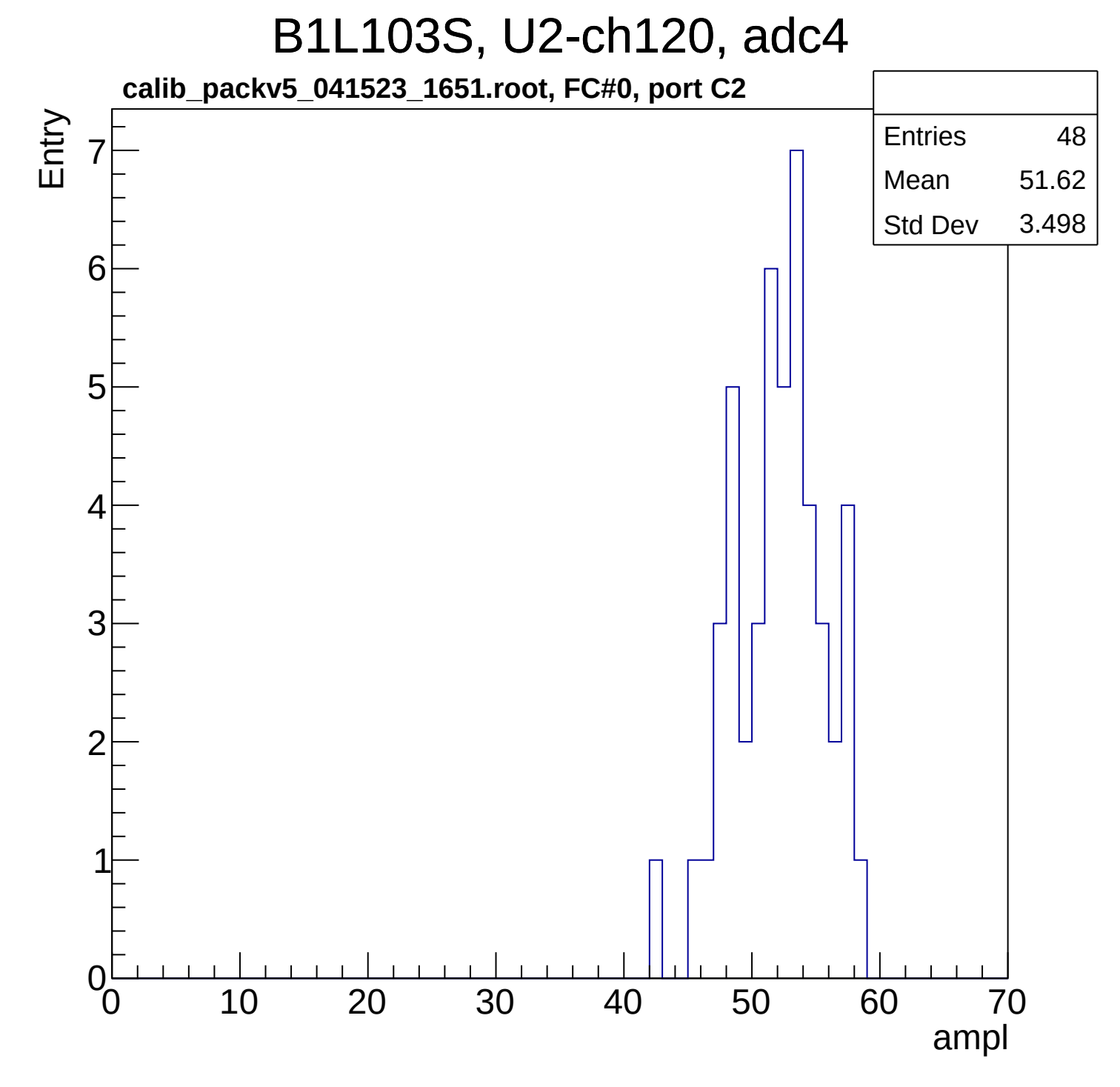

B1L103S, U2-ch119, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

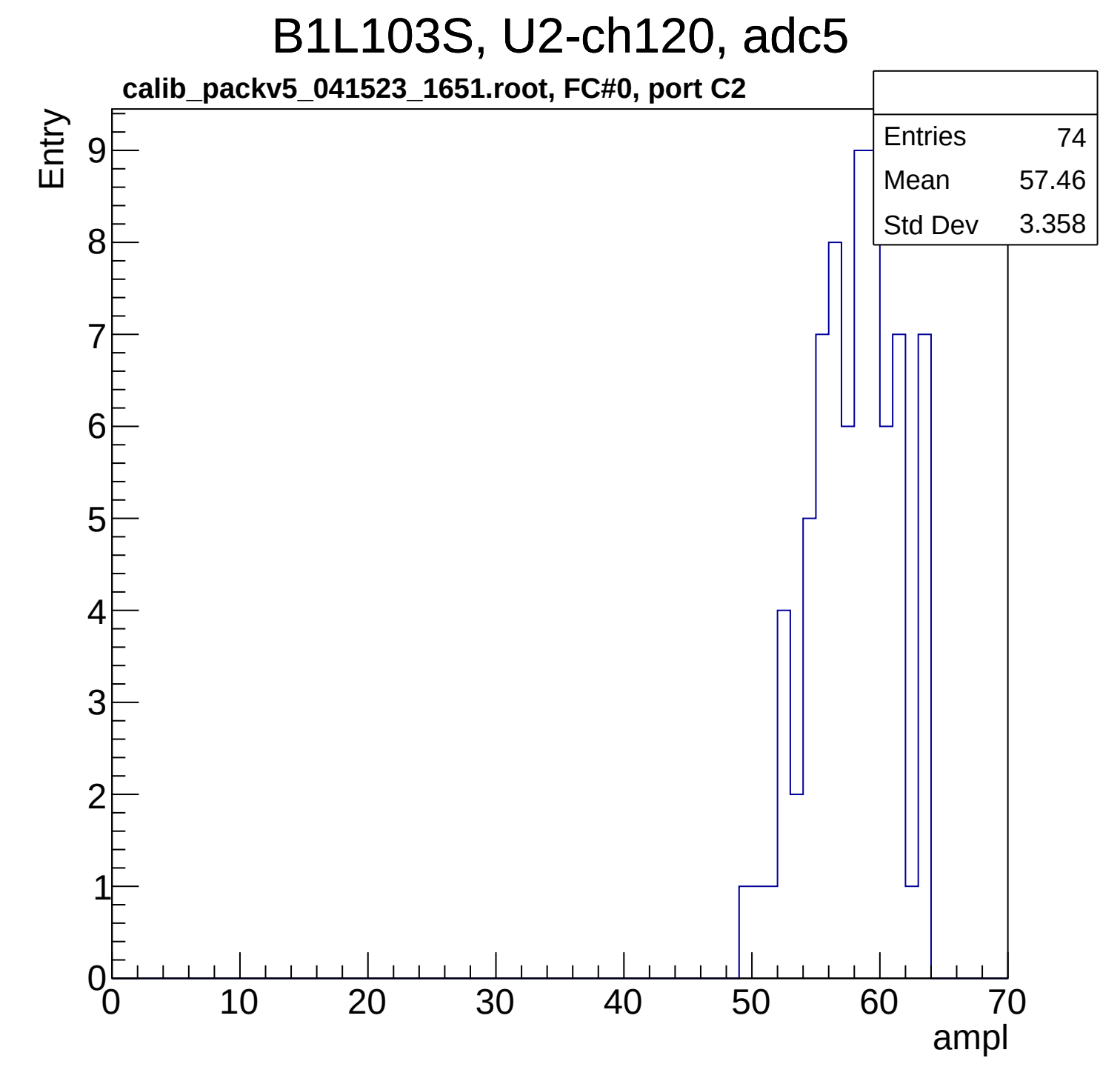

B1L103S, U2-ch120, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 20.89
Std Dev 12.16
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70

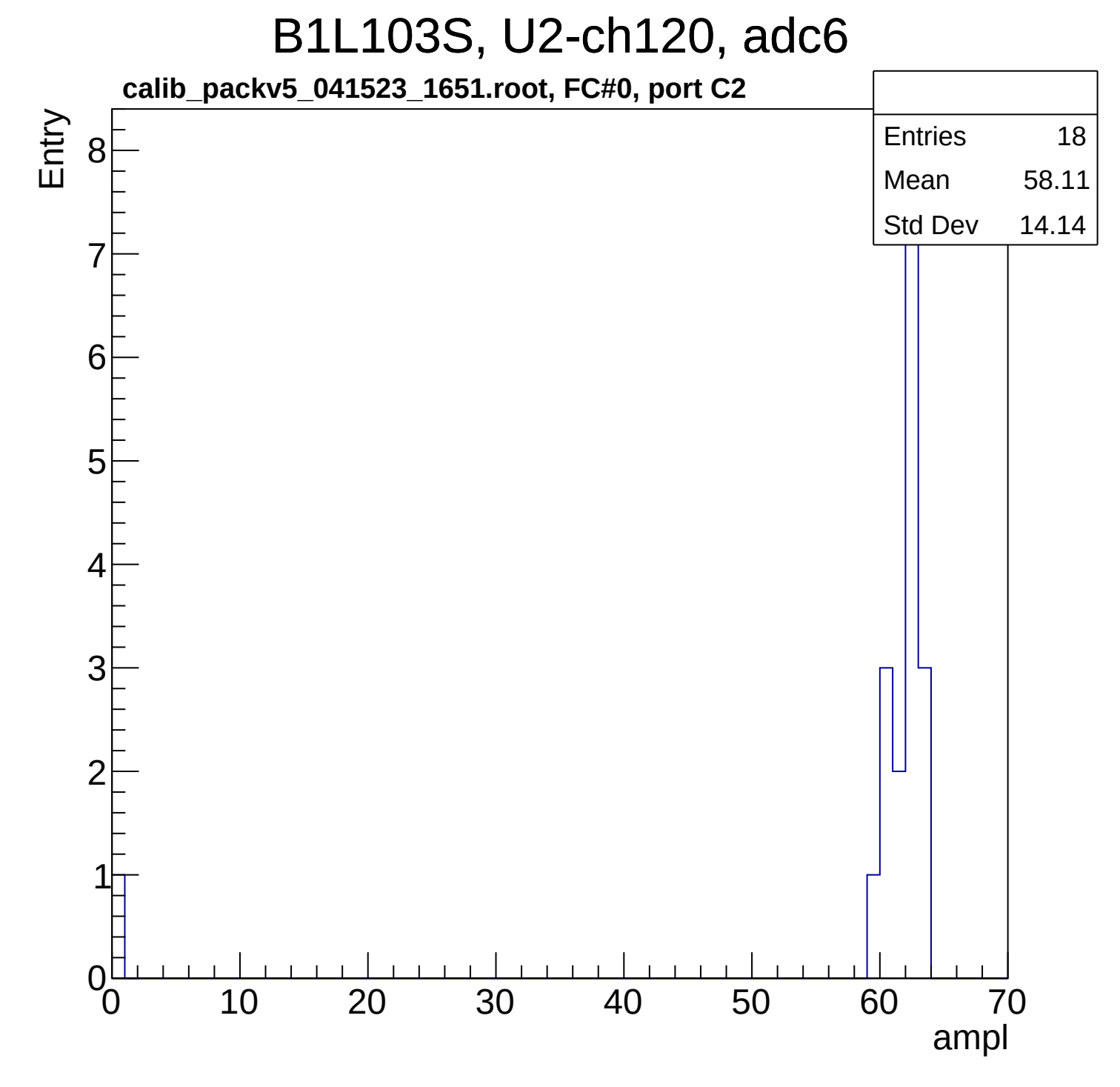

B1L103S, U2-ch120, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 30.6
Std Dev 11.31
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

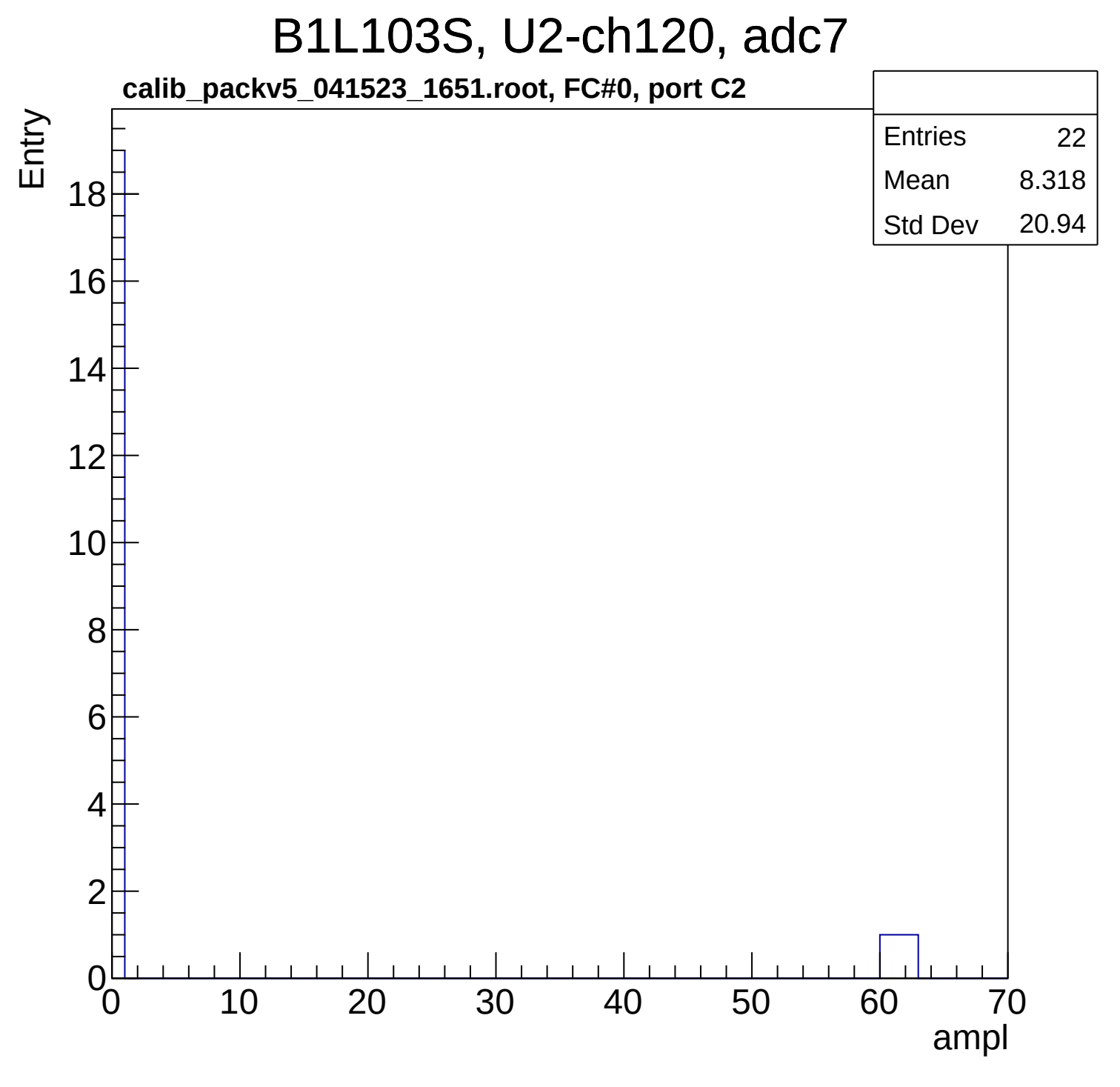

B1L103S, U2-ch120, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 36.41
Std Dev 13.64
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

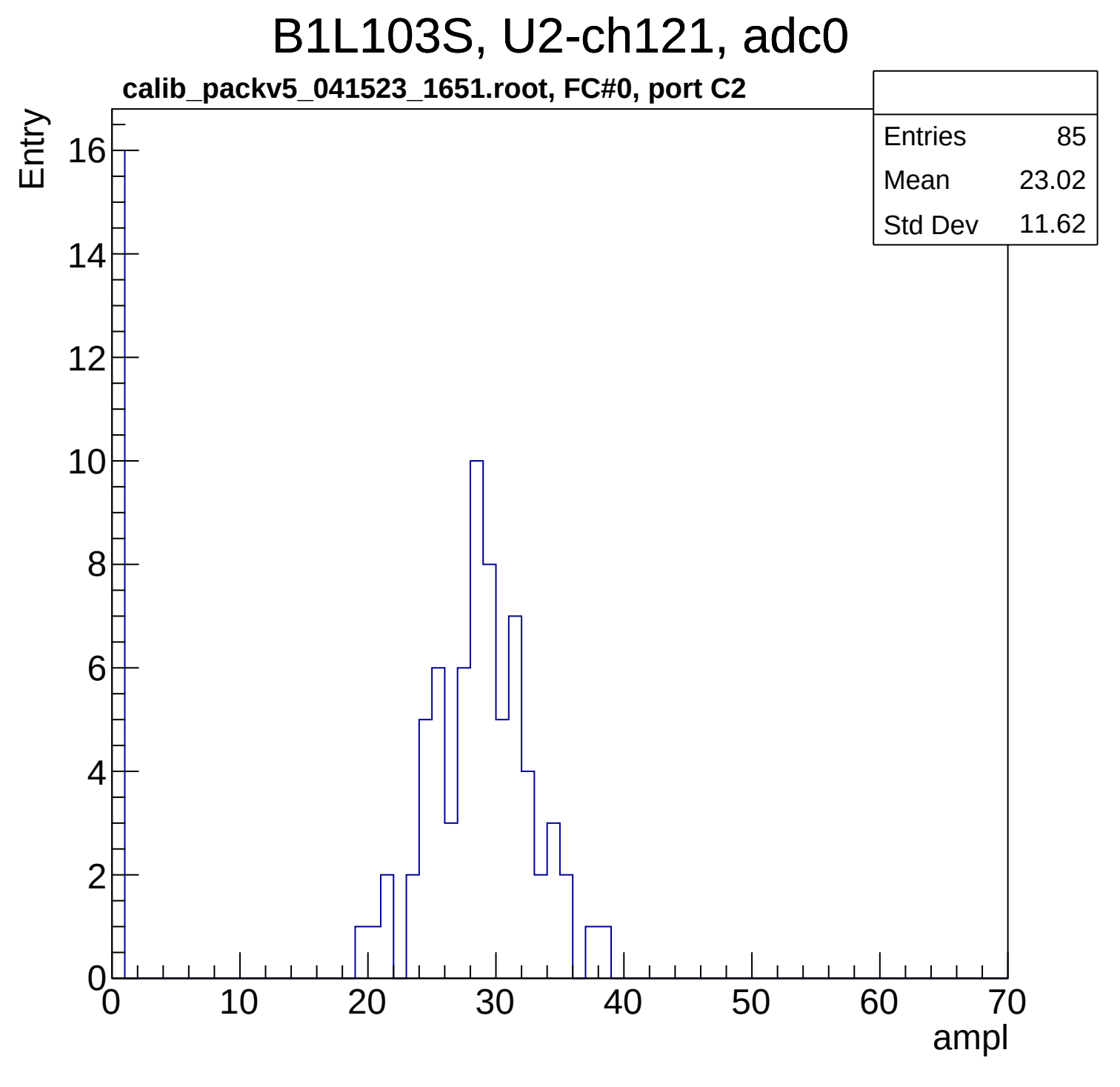

B1L103S, U2-ch120, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 46.54
Std Dev 3.382
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

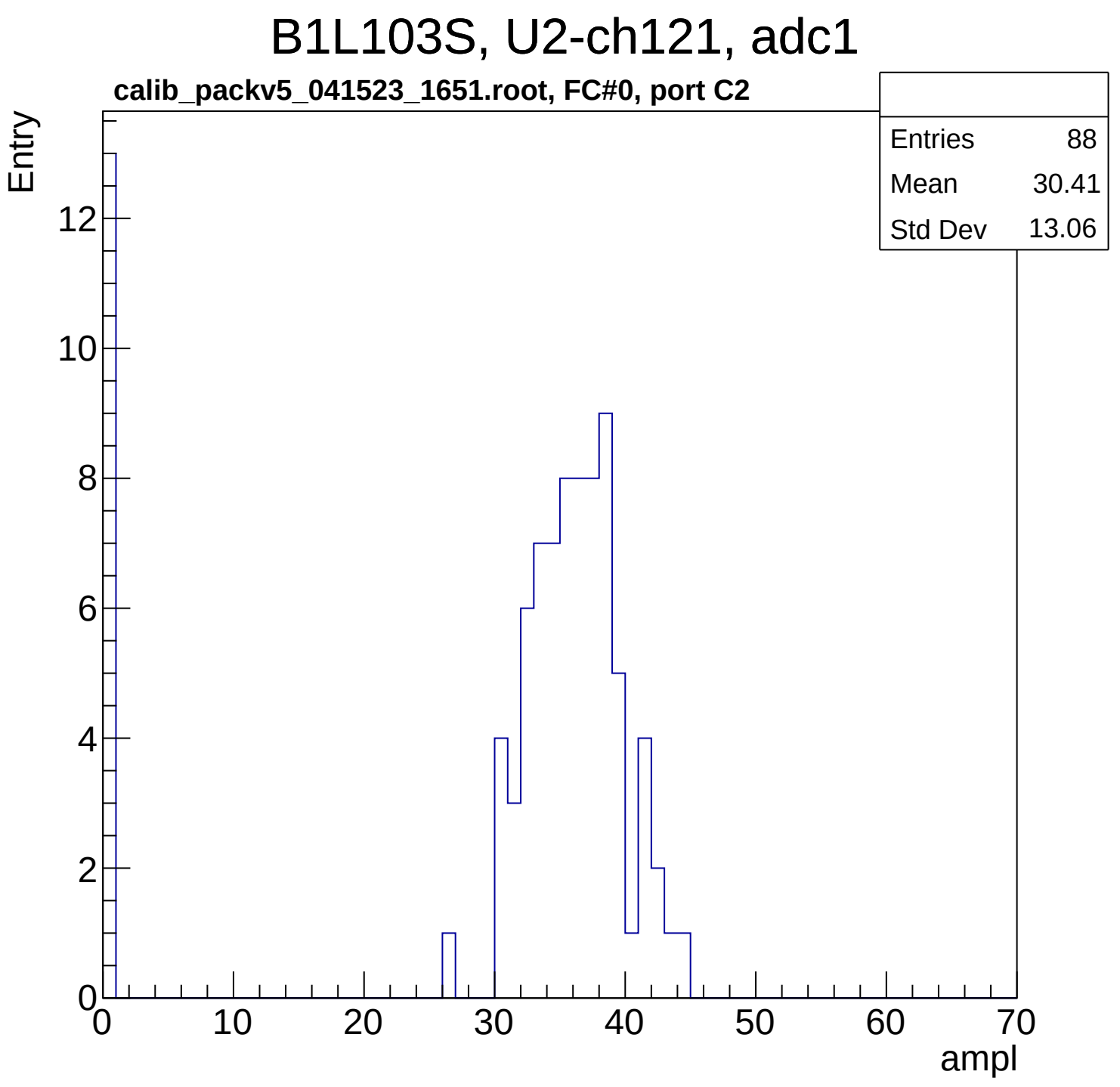

B1L103S, U2-ch120, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 51.62
Std Dev 3.498
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

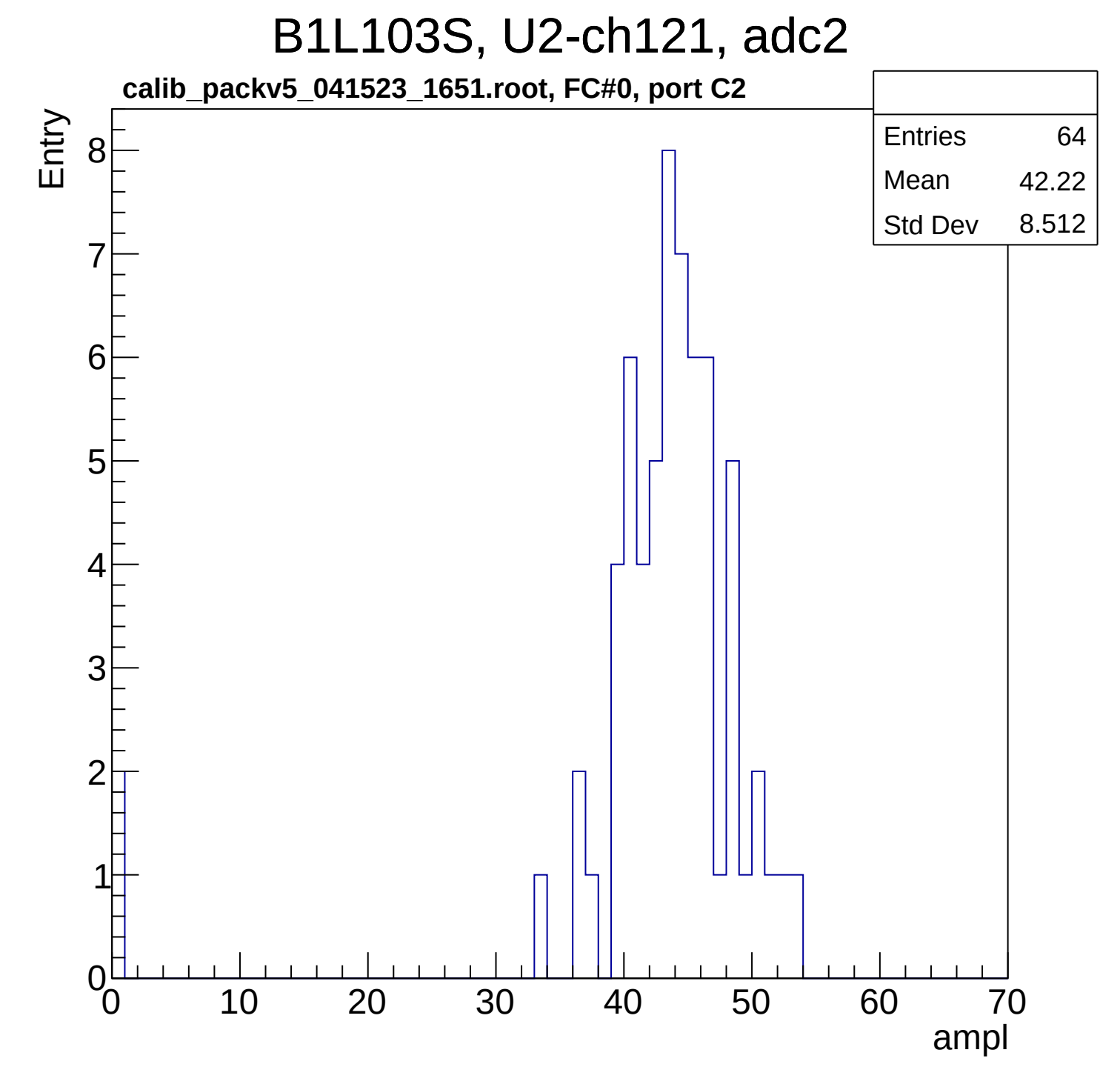

B1L103S, U2-ch120, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 57.46
Std Dev 3.358
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

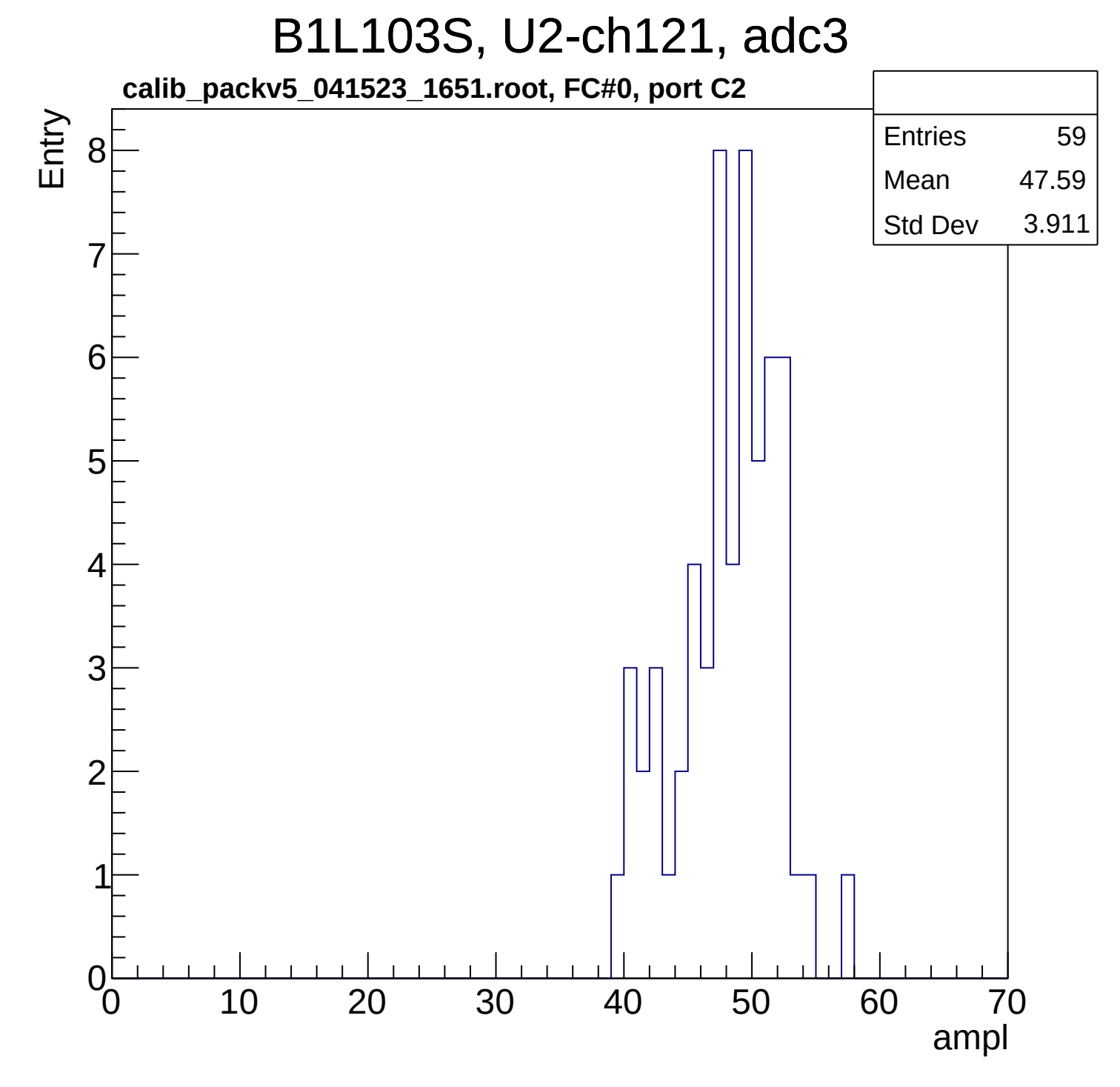

B1L103S, U2-ch120, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 58.11
Std Dev 14.14
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

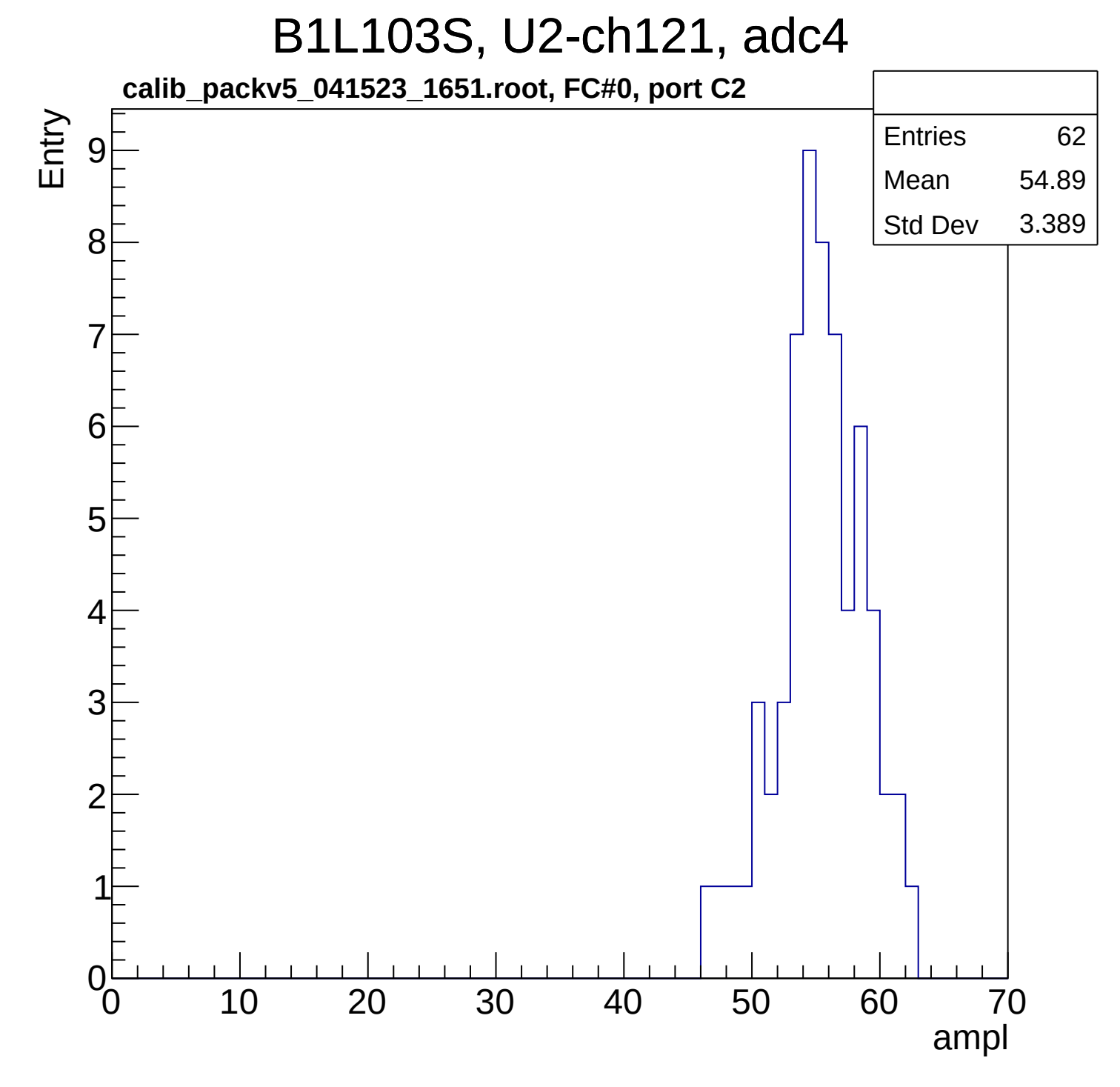

B1L103S, U2-ch120, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.318
Std Dev 20.94
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

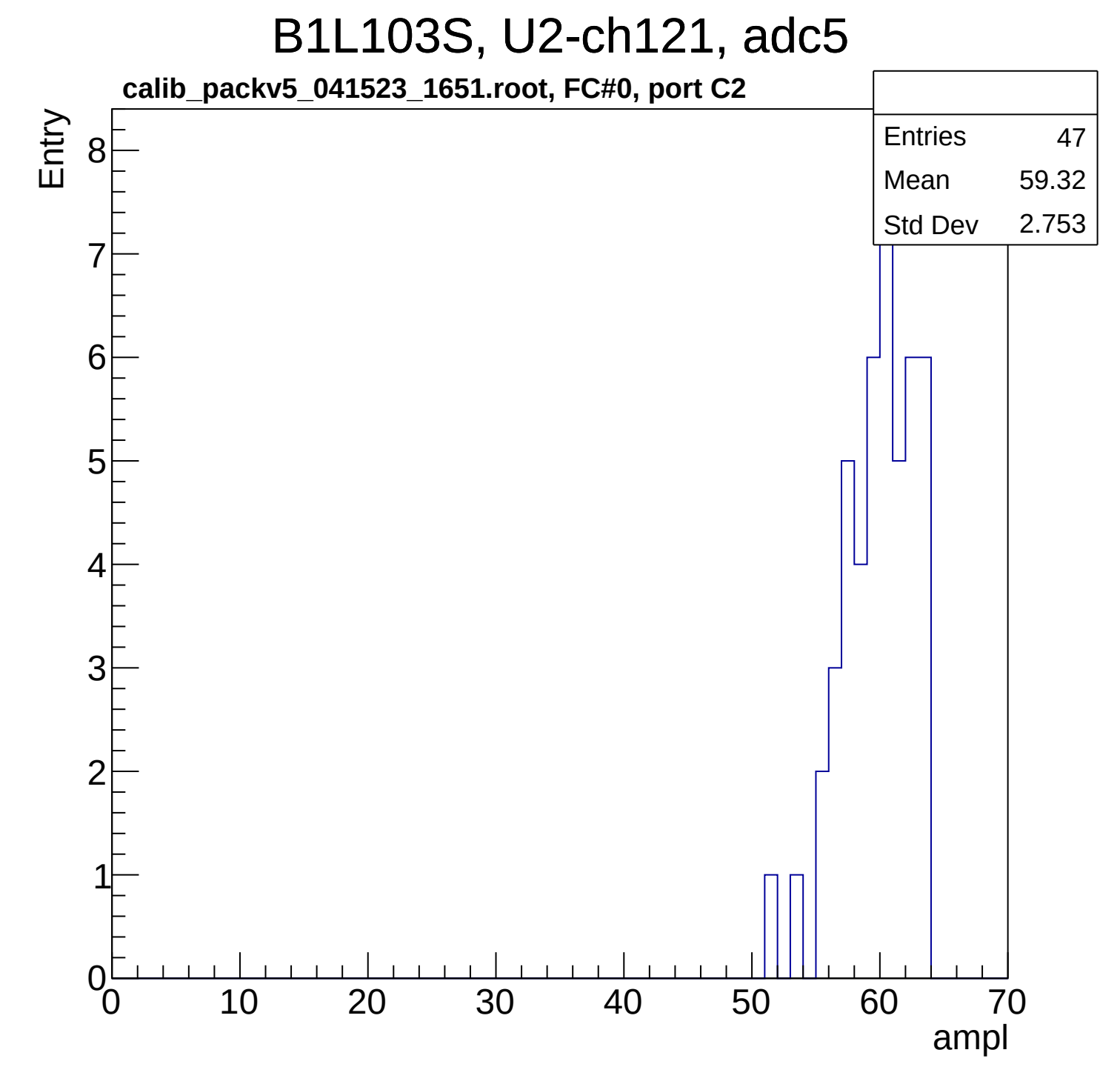

B1L103S, U2-ch121, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 23.02
Std Dev 11.62
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

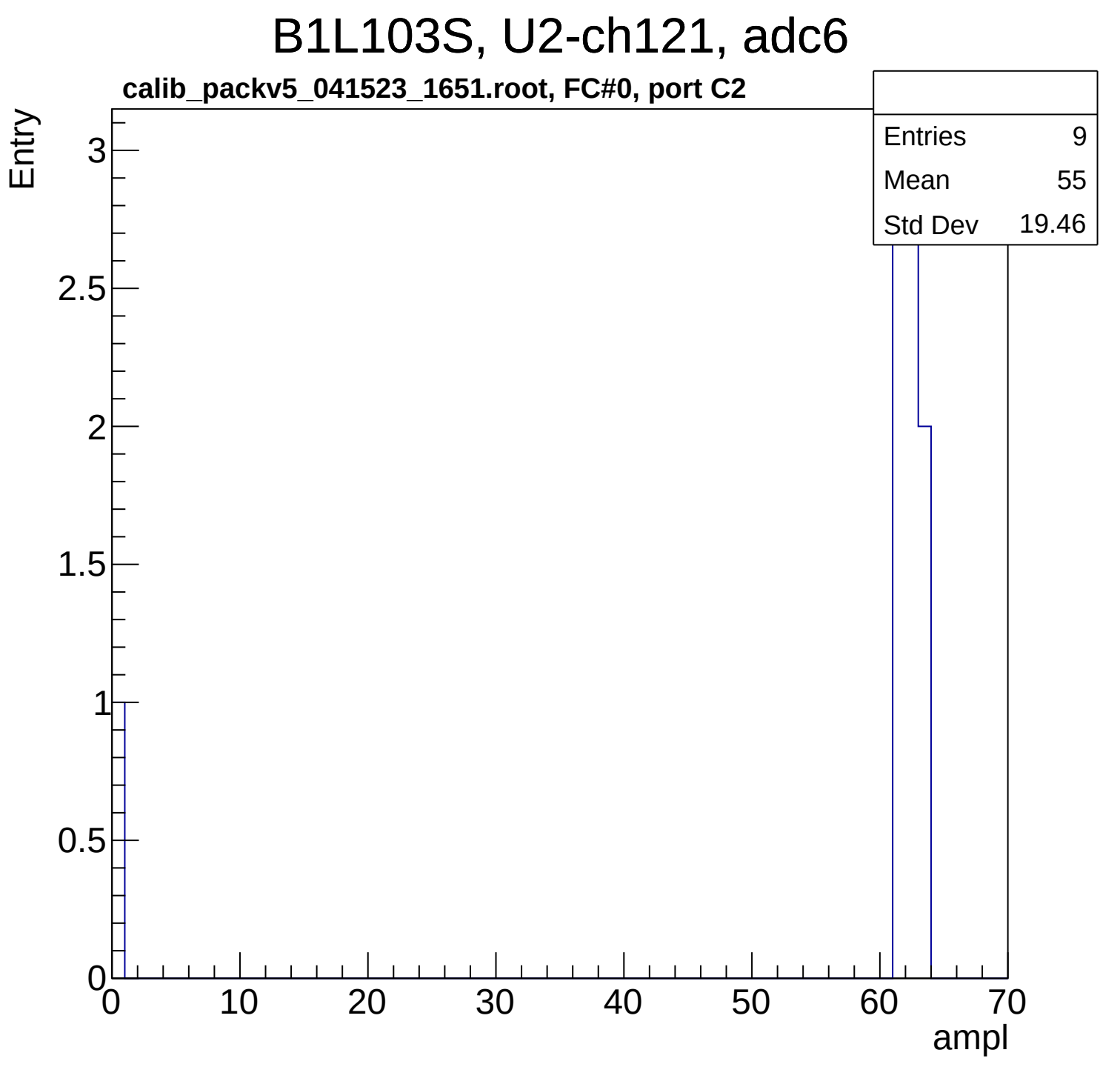

B1L103S, U2-ch121, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 30.41
Std Dev 13.06
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl

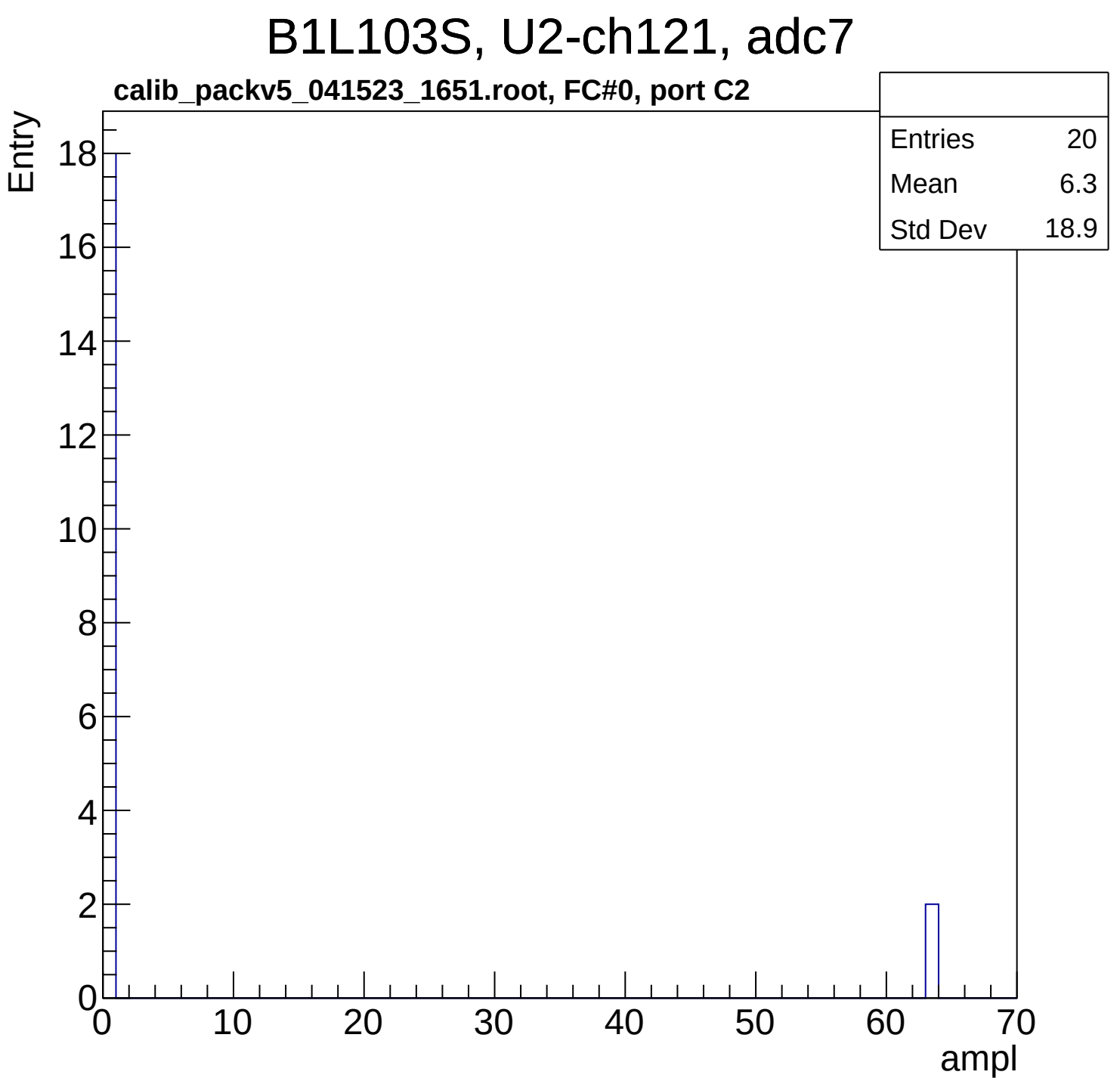

B1L103S, U2-ch121, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 42.22
Std Dev 8.512
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

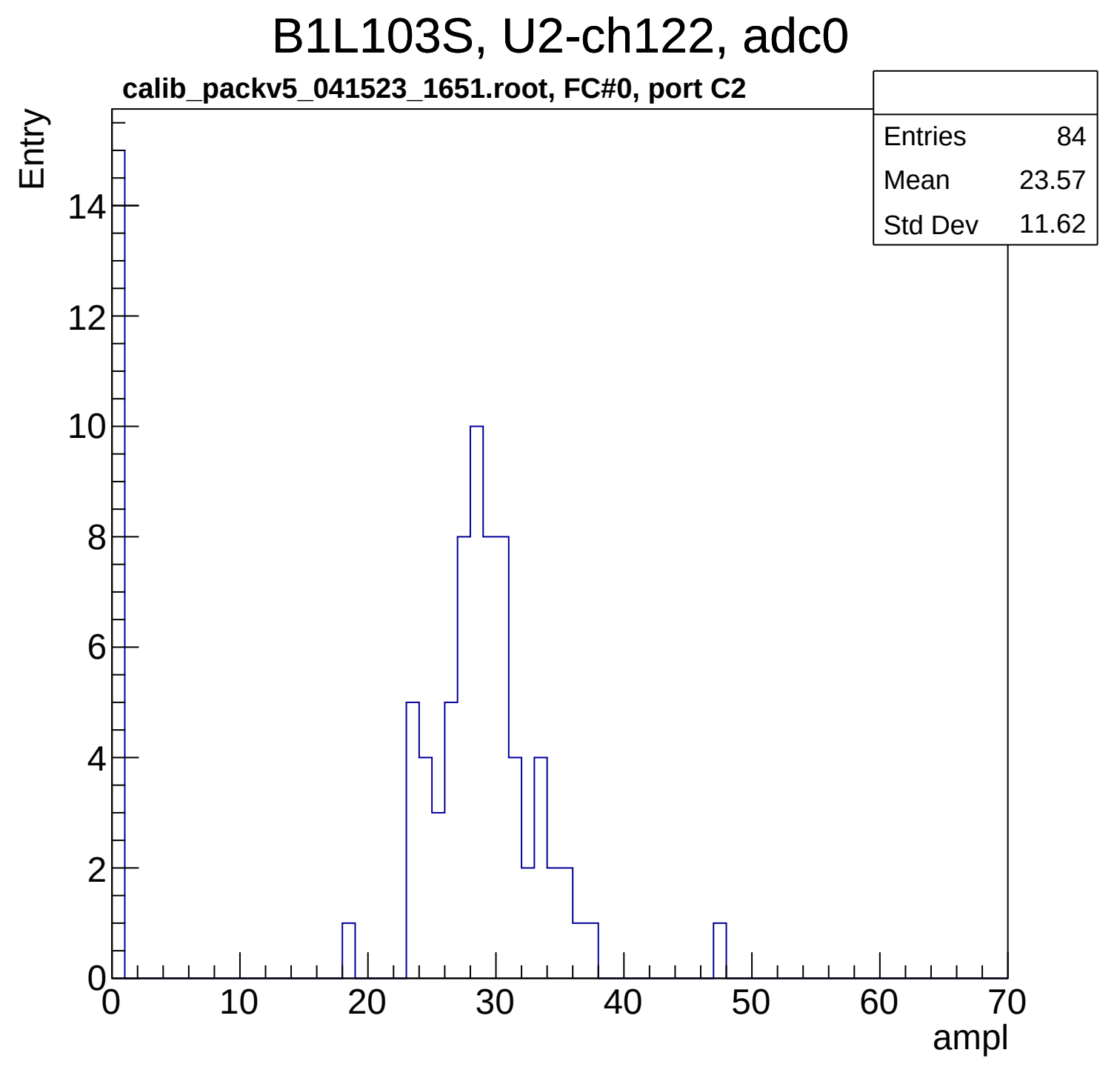

B1L103S, U2-ch121, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 47.59
Std Dev 3.911
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

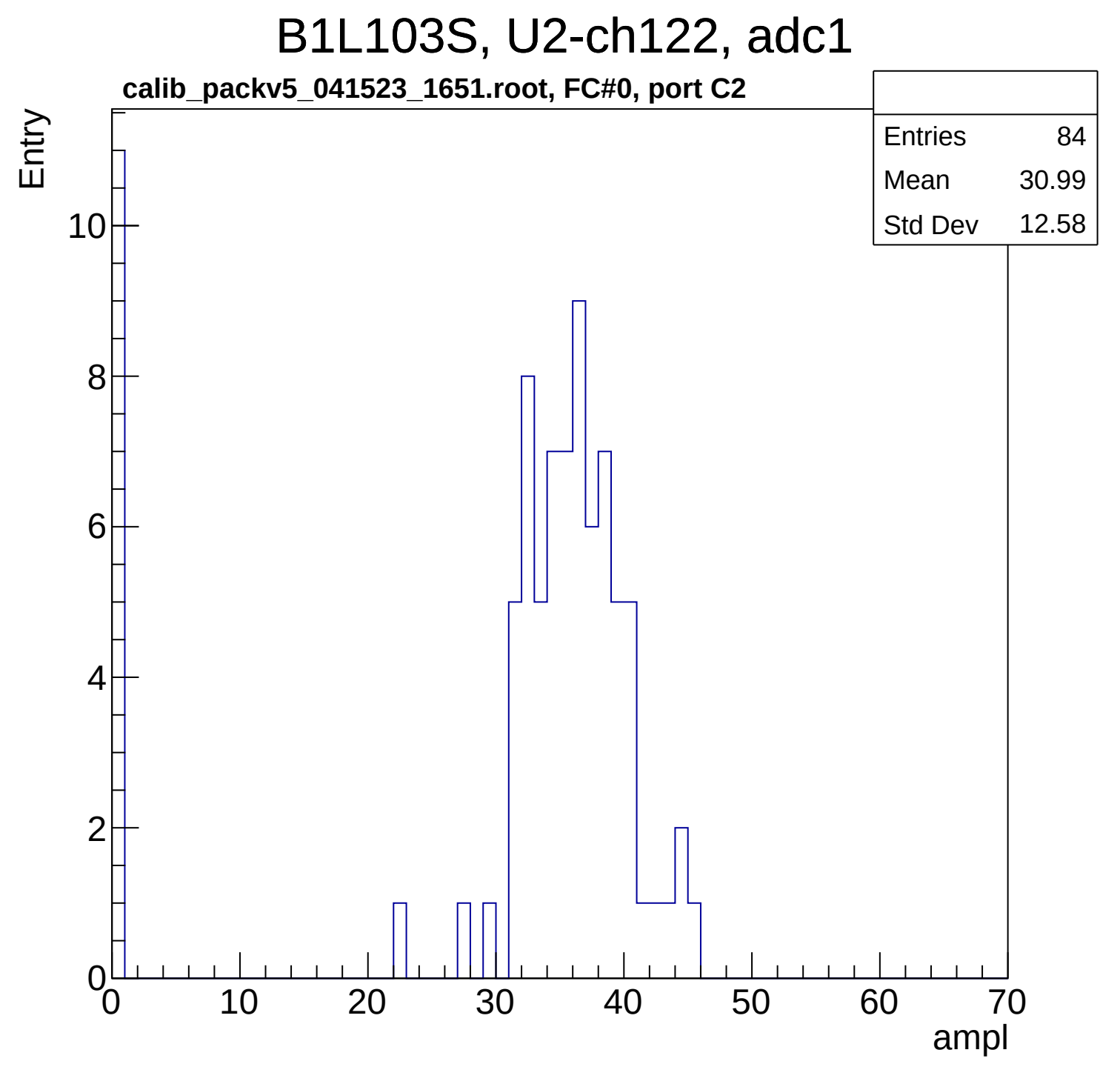

B1L103S, U2-ch121, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 54.89
Std Dev 3.389
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

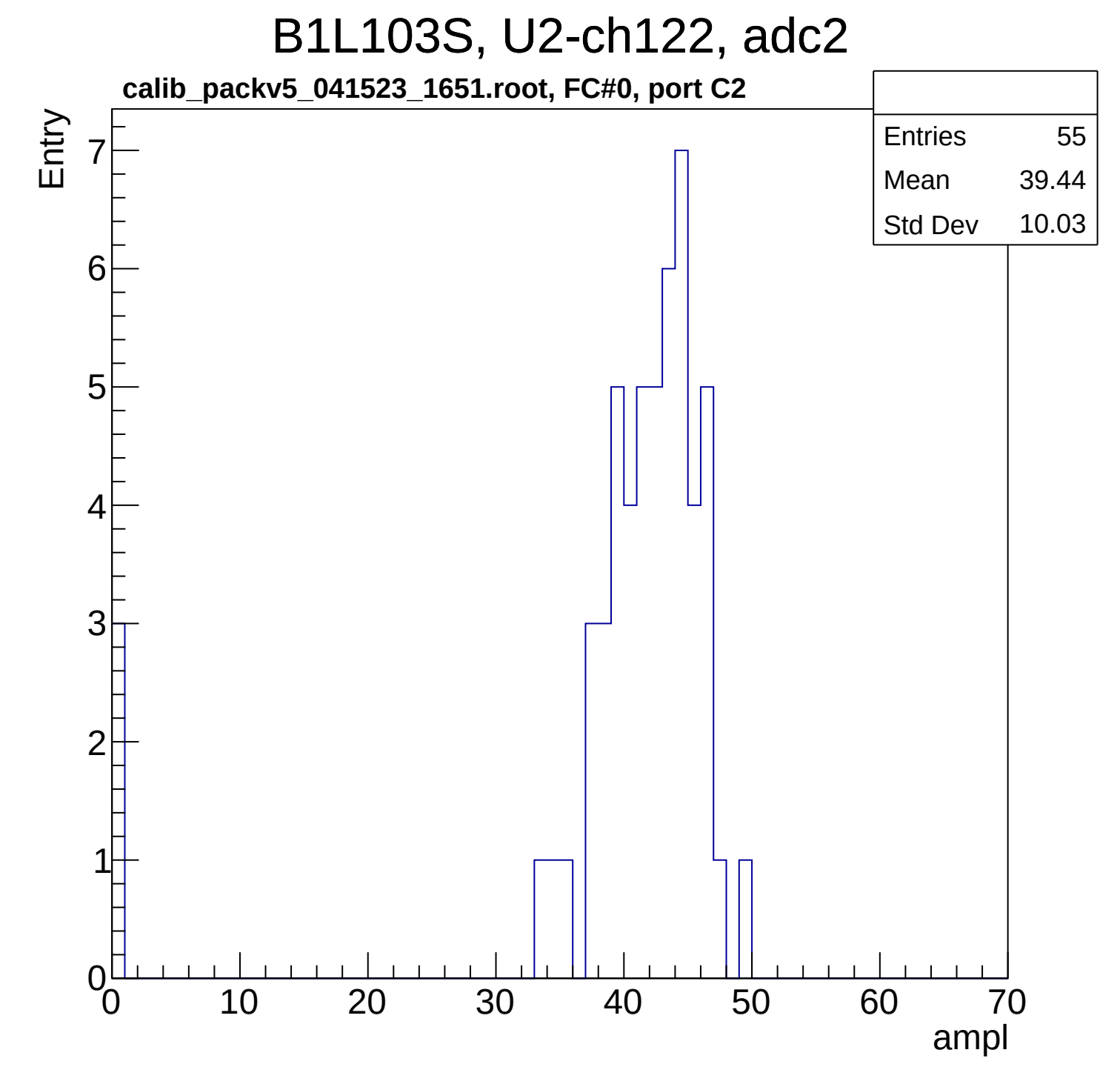

B1L103S, U2-ch121, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 59.32
Std Dev 2.753
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

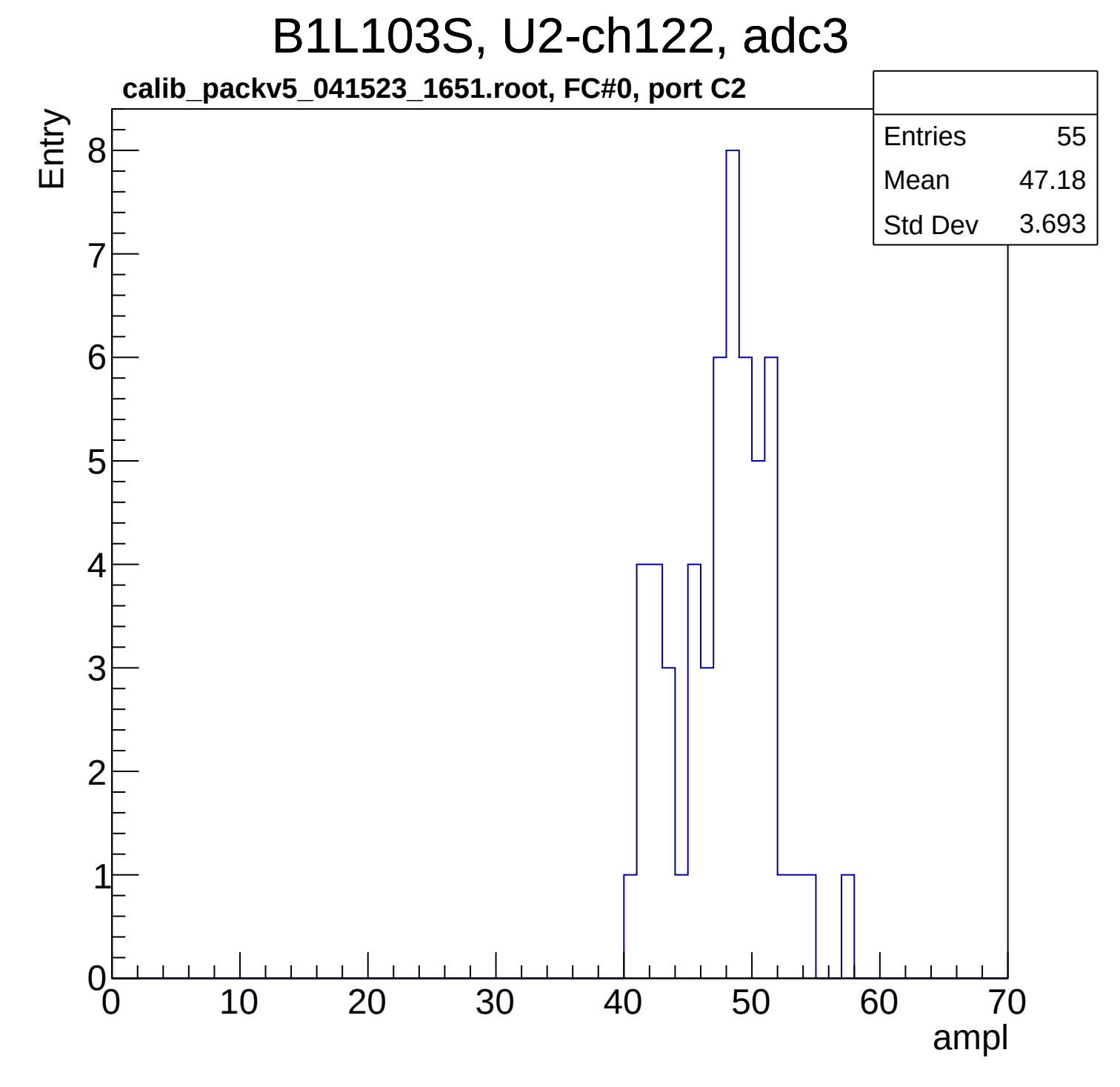

B1L103S, U2-ch121, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 55
Std Dev 19.46
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

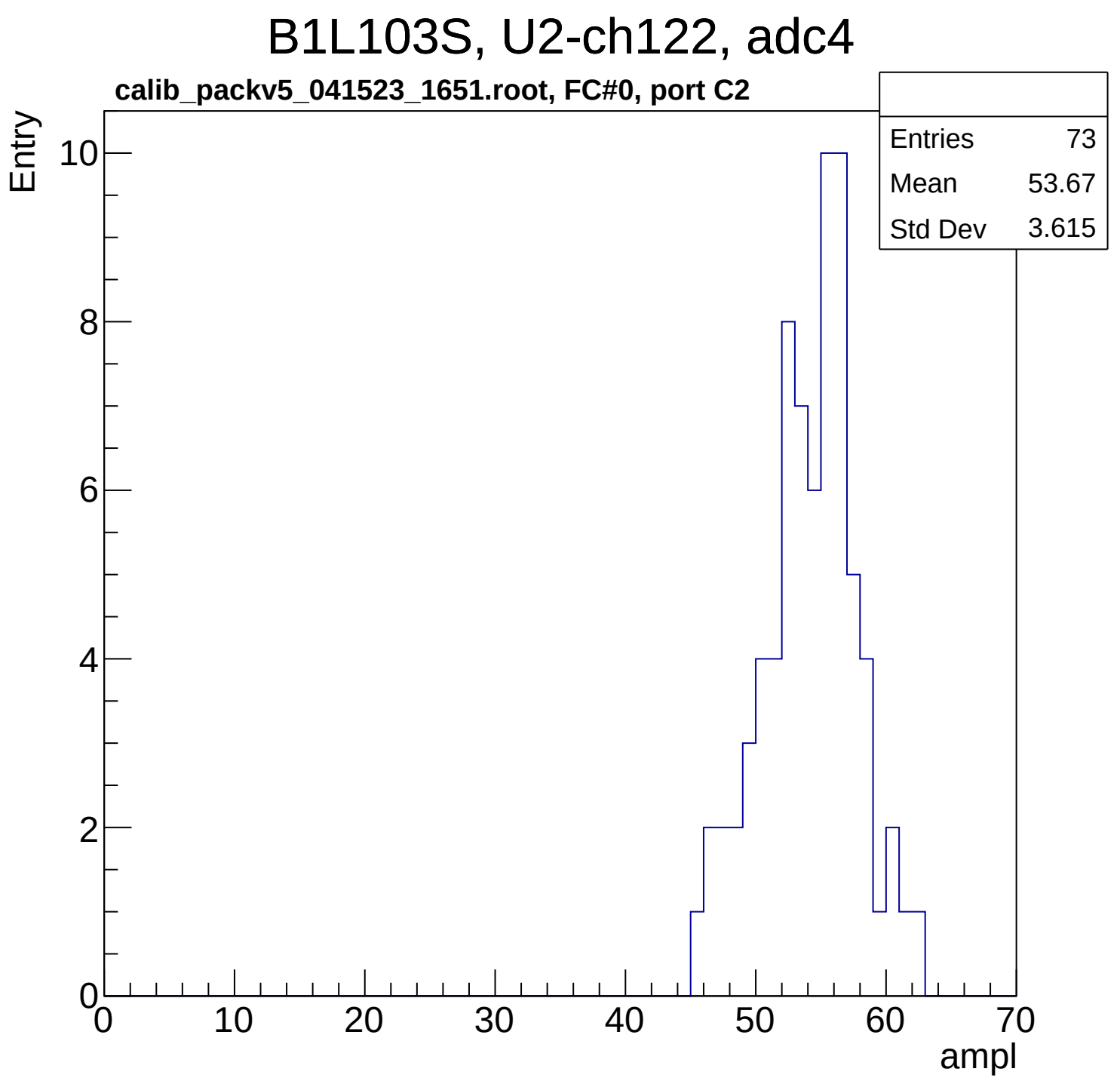

B1L103S, U2-ch121, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.3
Std Dev 18.9
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

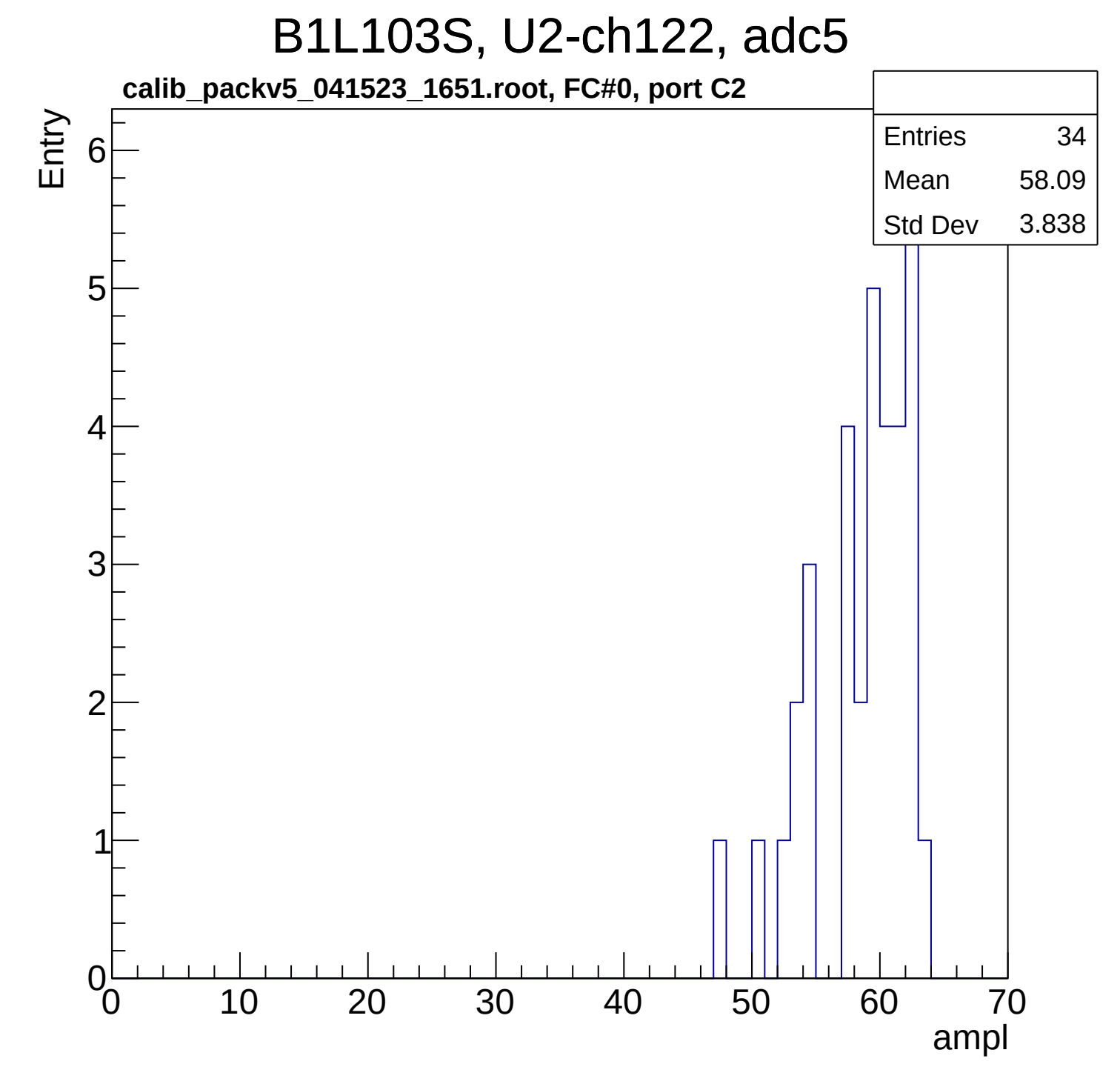

B1L103S, U2-ch122, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 23.57
Std Dev 11.62
Entry
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70
ampl

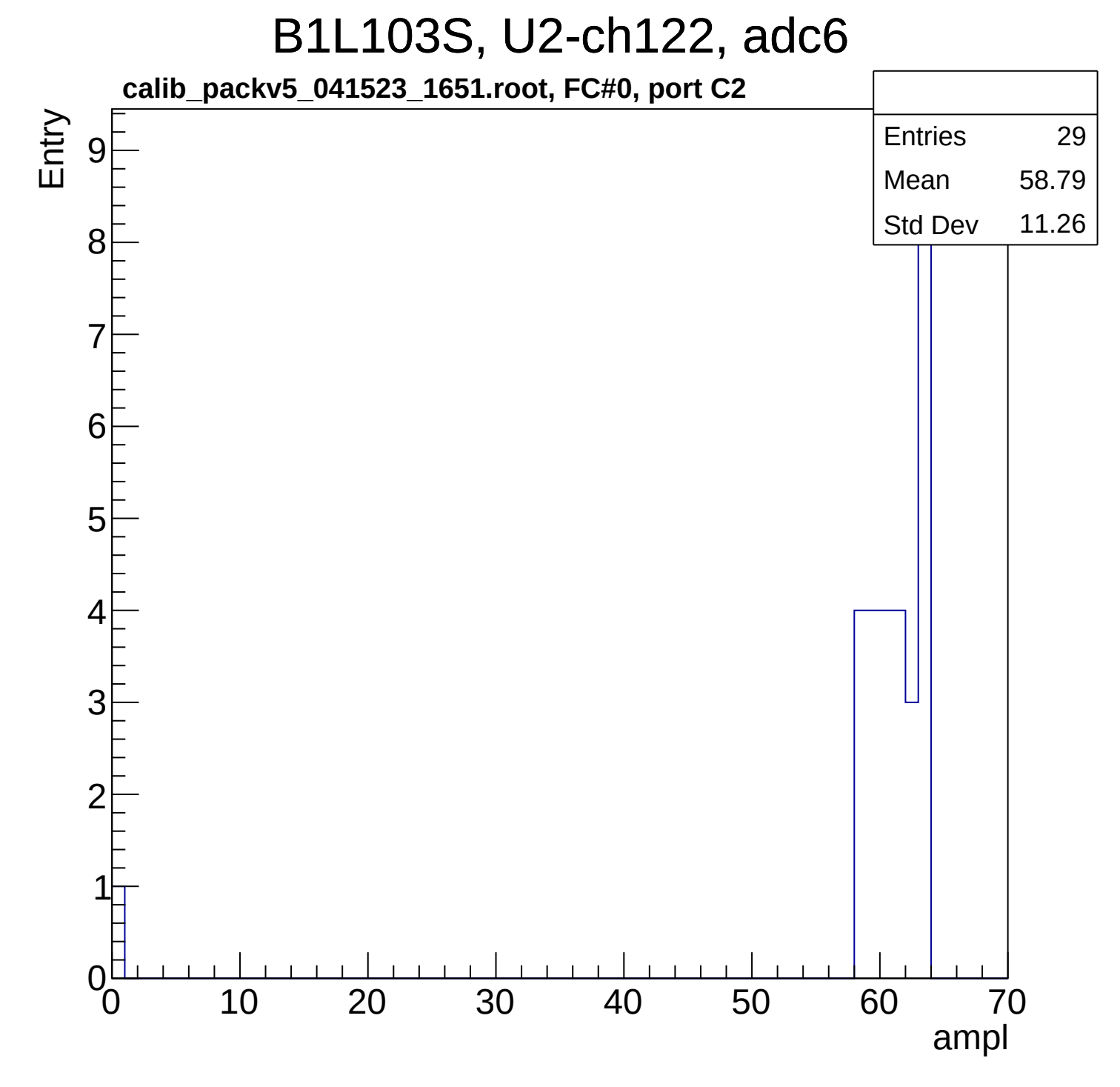

B1L103S, U2-ch122, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 30.99
Std Dev 12.58
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

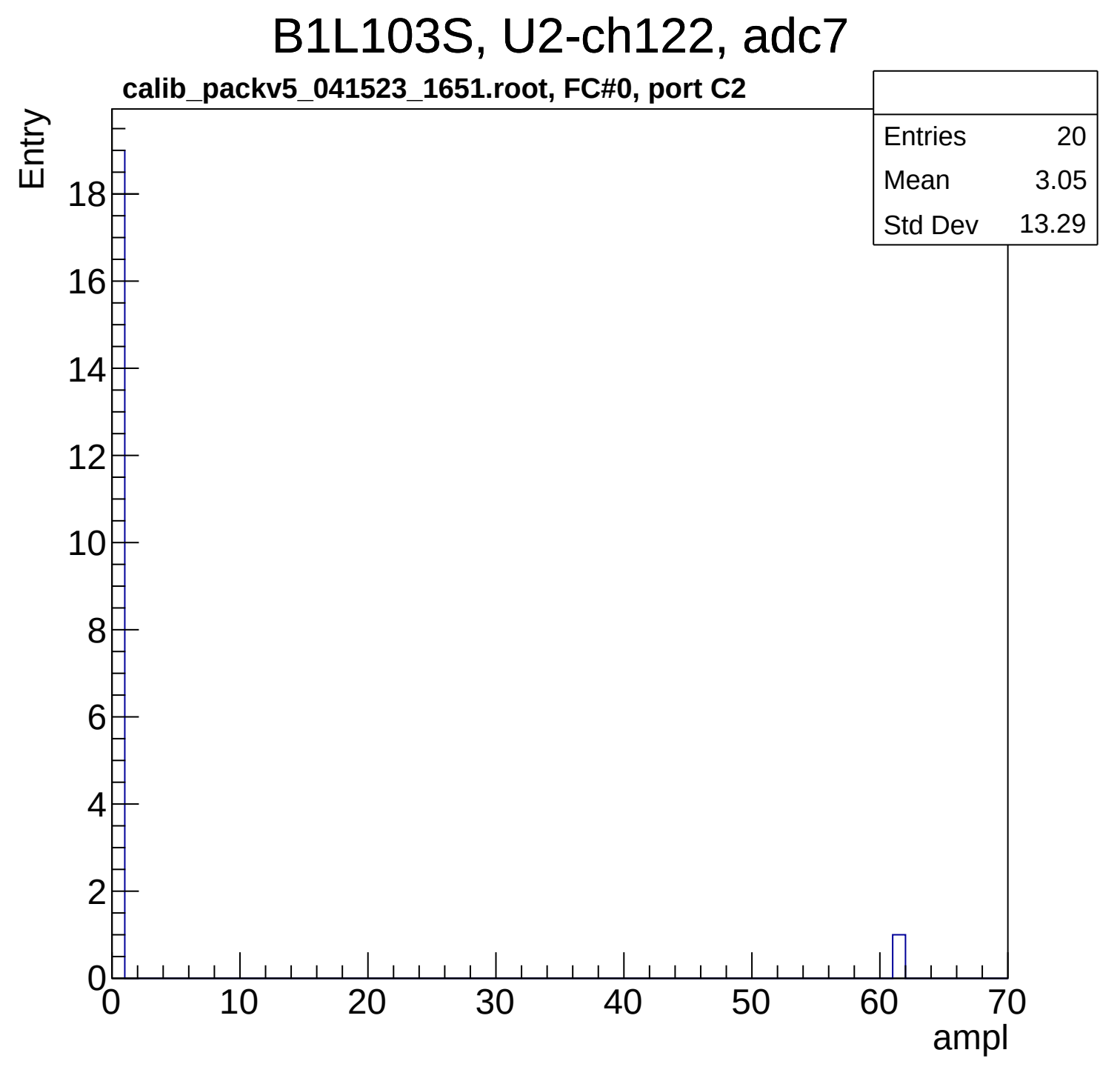

B1L103S, U2-ch122, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 39.44
Std Dev 10.03
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

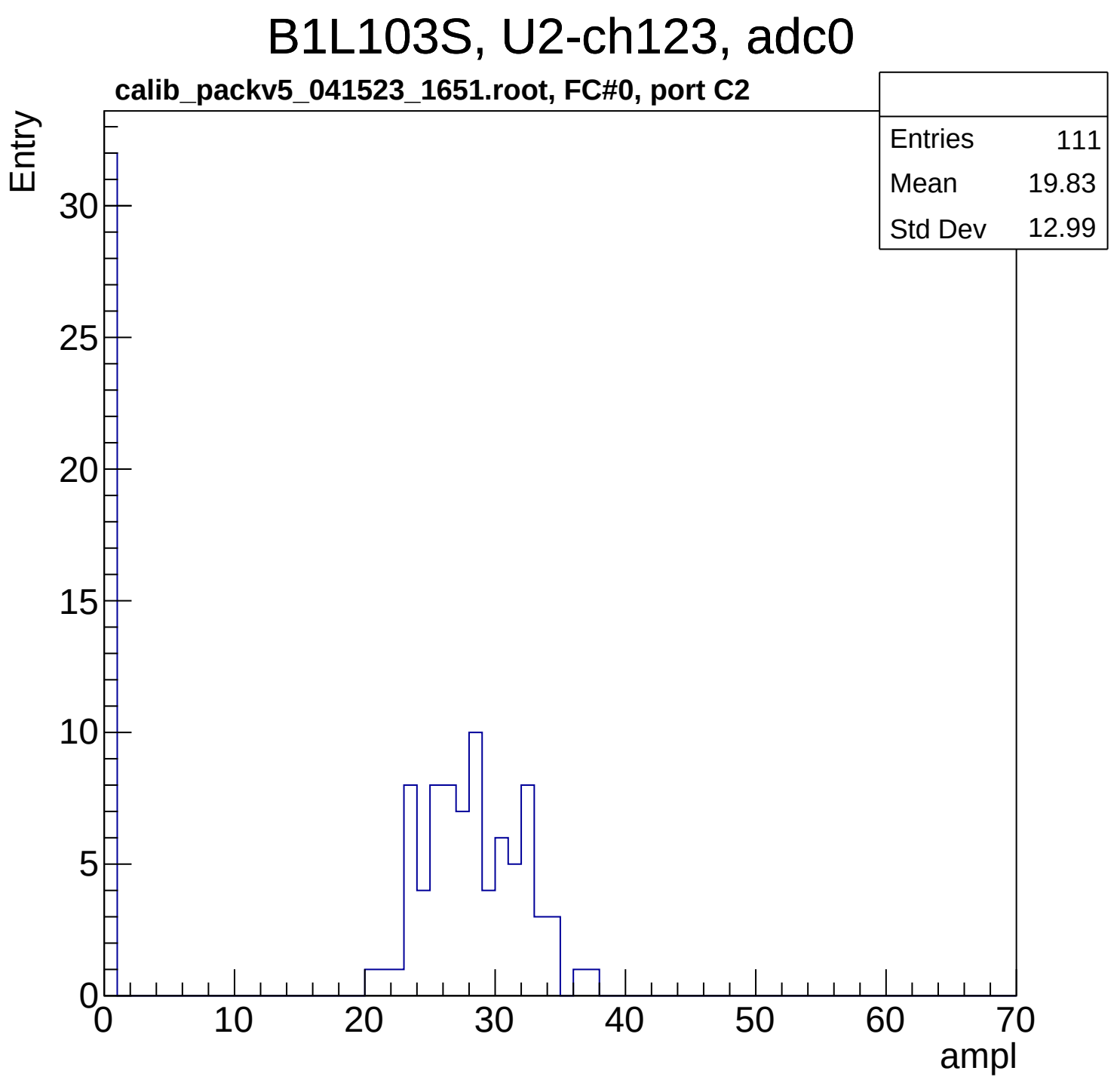

B1L103S, U2-ch122, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 47.18
Std Dev 3.693
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

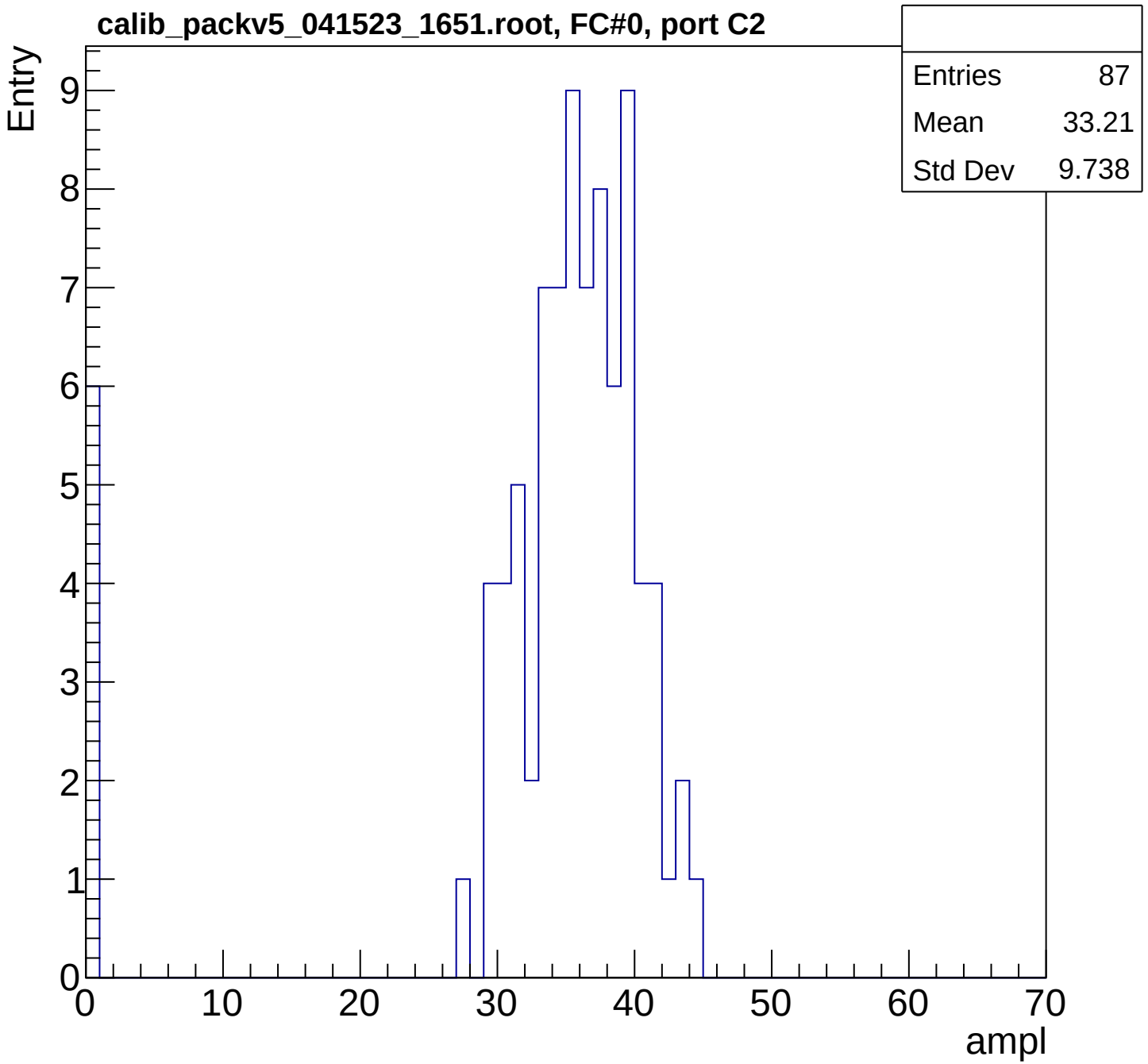

B1L103S, U2-ch122, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 53.67
Std Dev 3.615
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

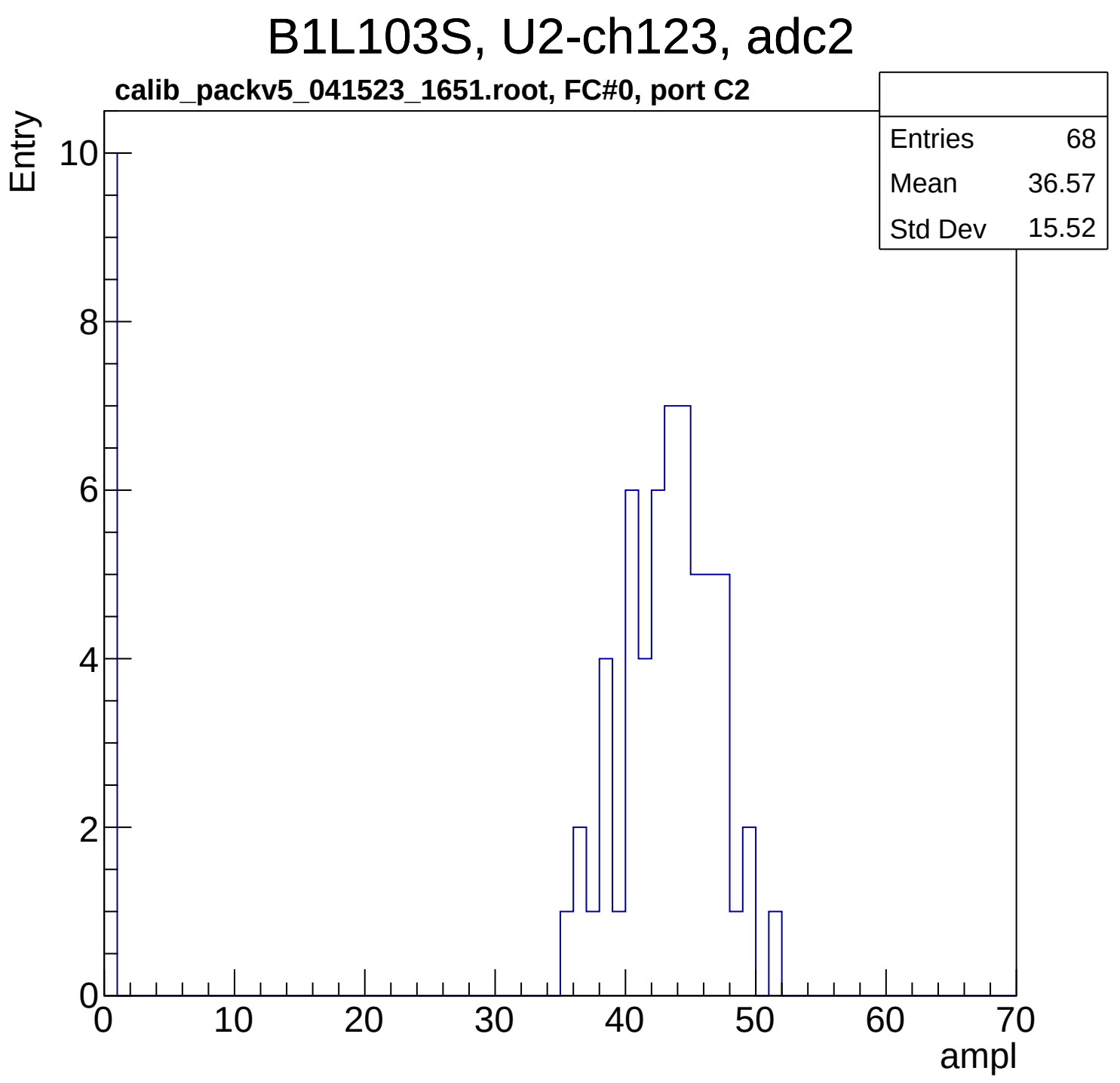

B1L103S, U2-ch122, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 58.09
Std Dev 3.838
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

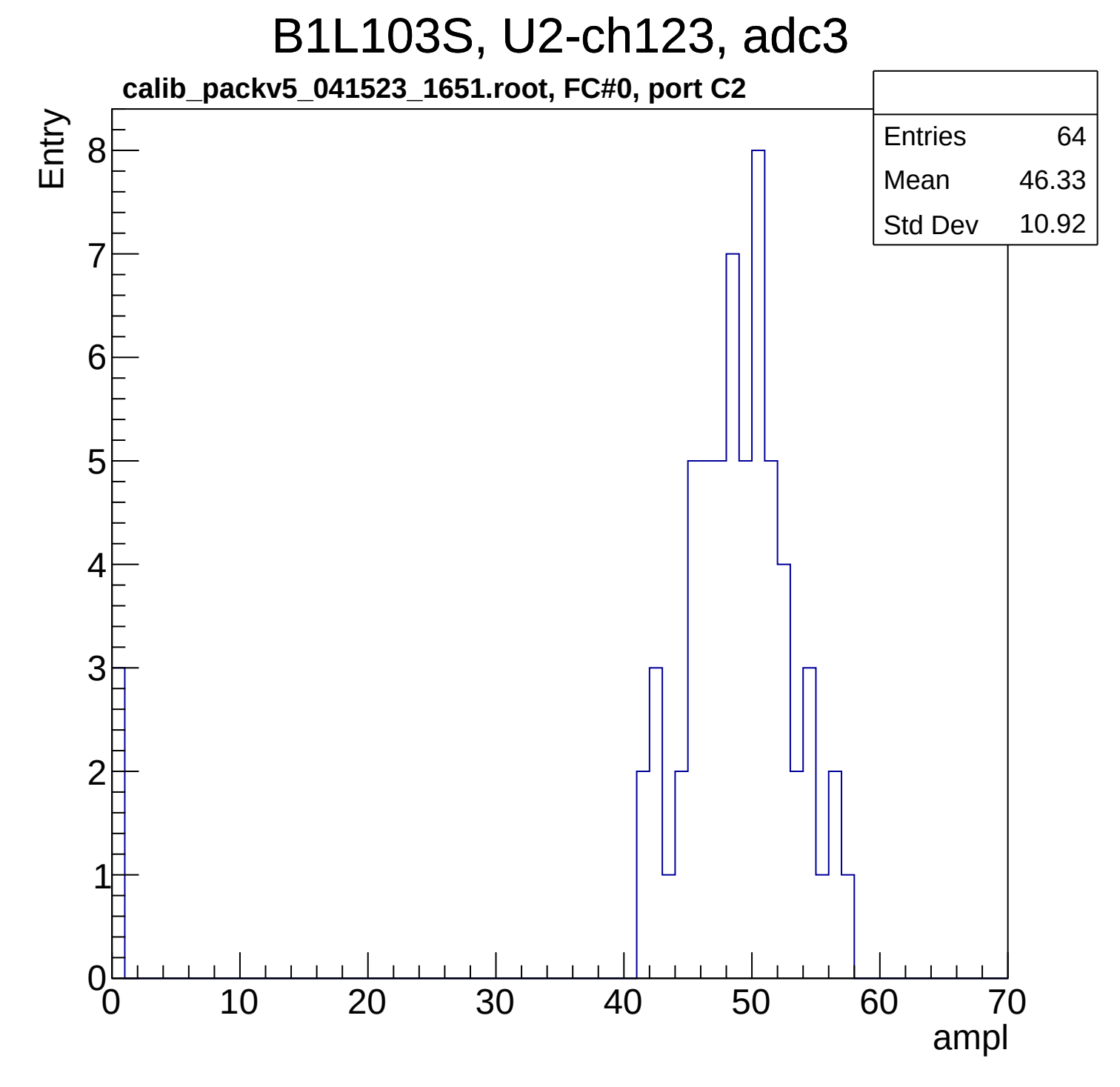

B1L103S, U2-ch122, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 29
Mean 58.79
Std Dev 11.26
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

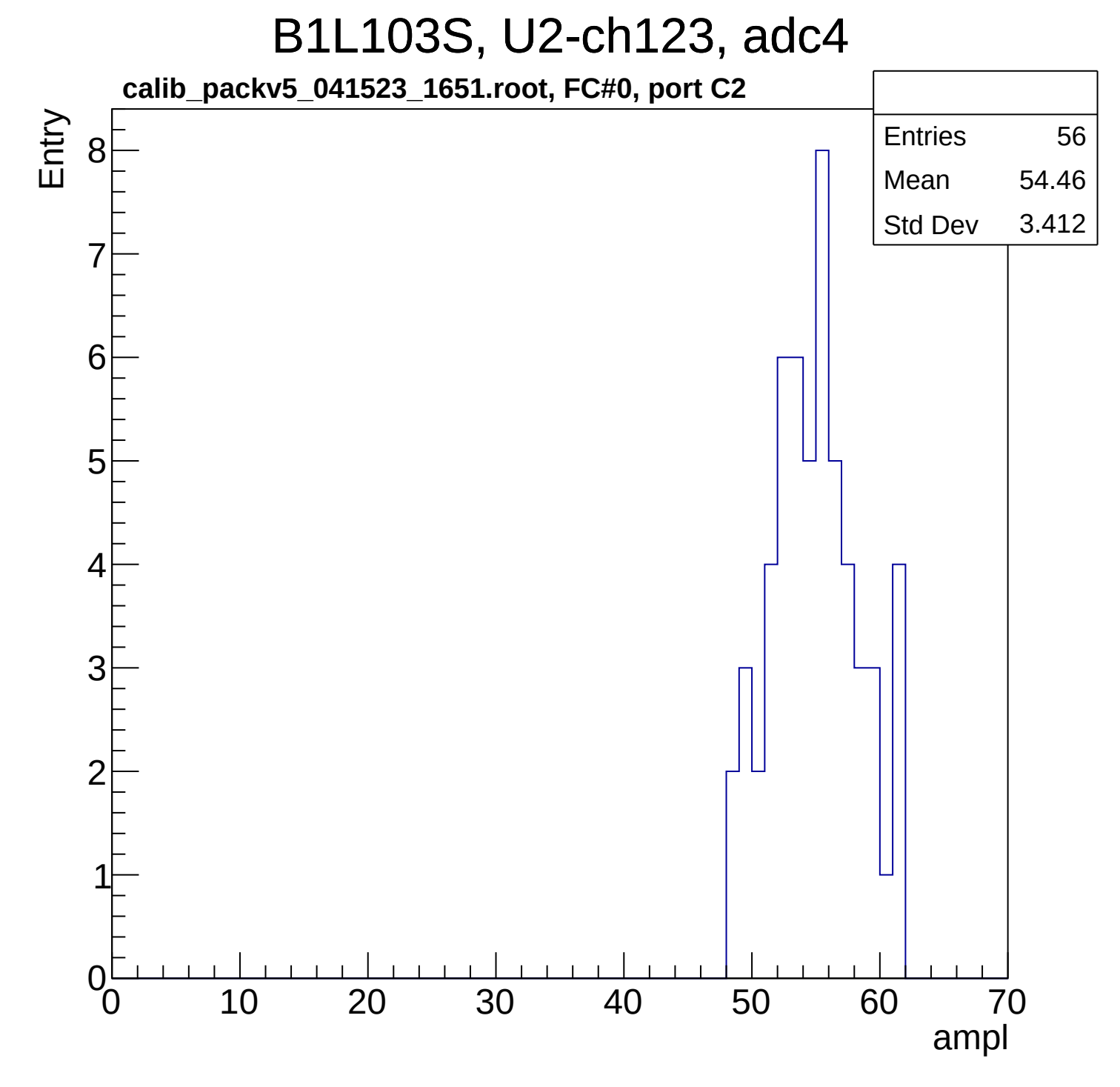

B1L103S, U2-ch122, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.05
Std Dev 13.29
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

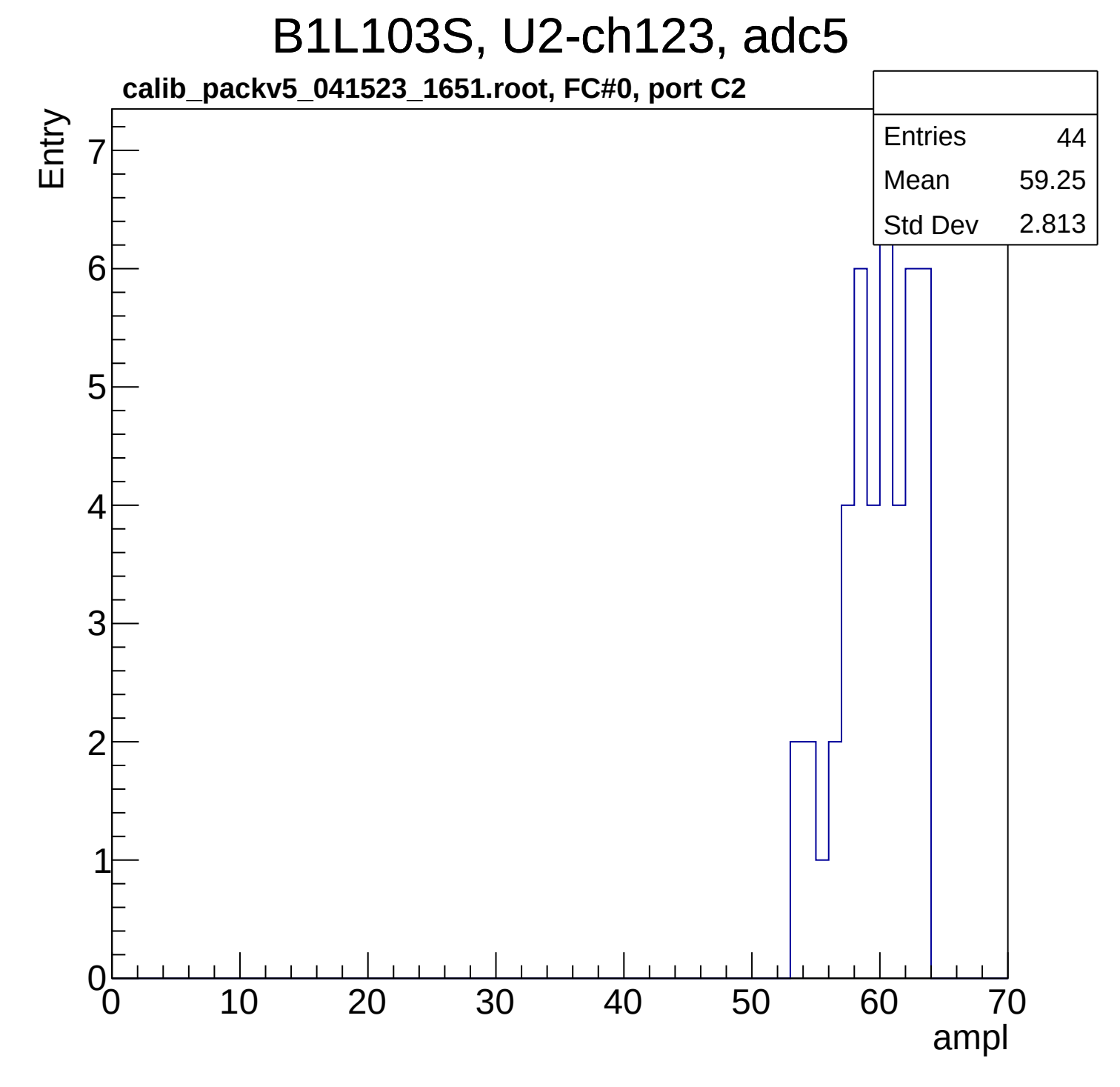

B1L103S, U2-ch123, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 111
Mean 19.83
Std Dev 12.99
Entry
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70
ampl

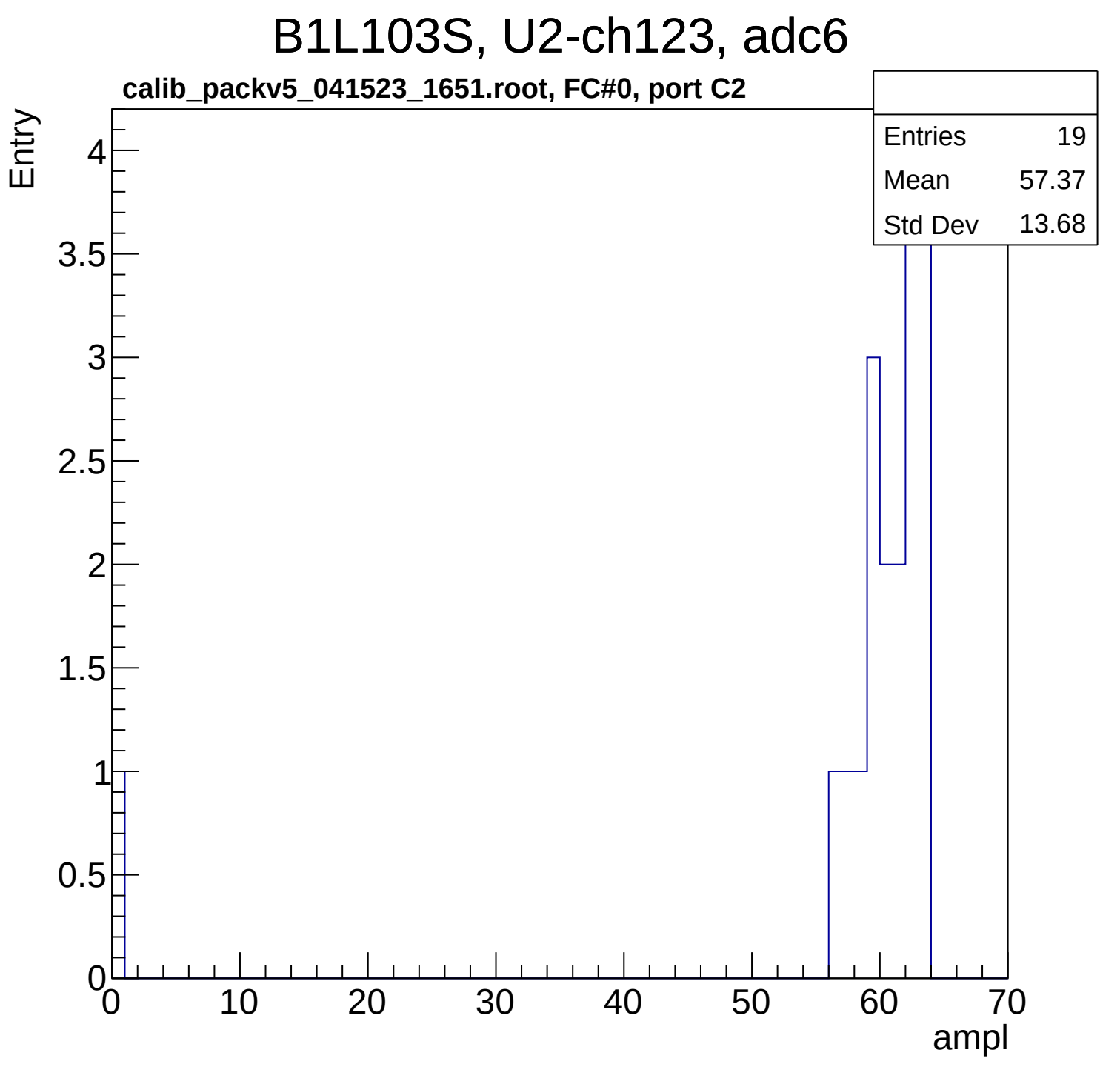

B1L103S, U2-ch123, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 33.21
Std Dev 9.738
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

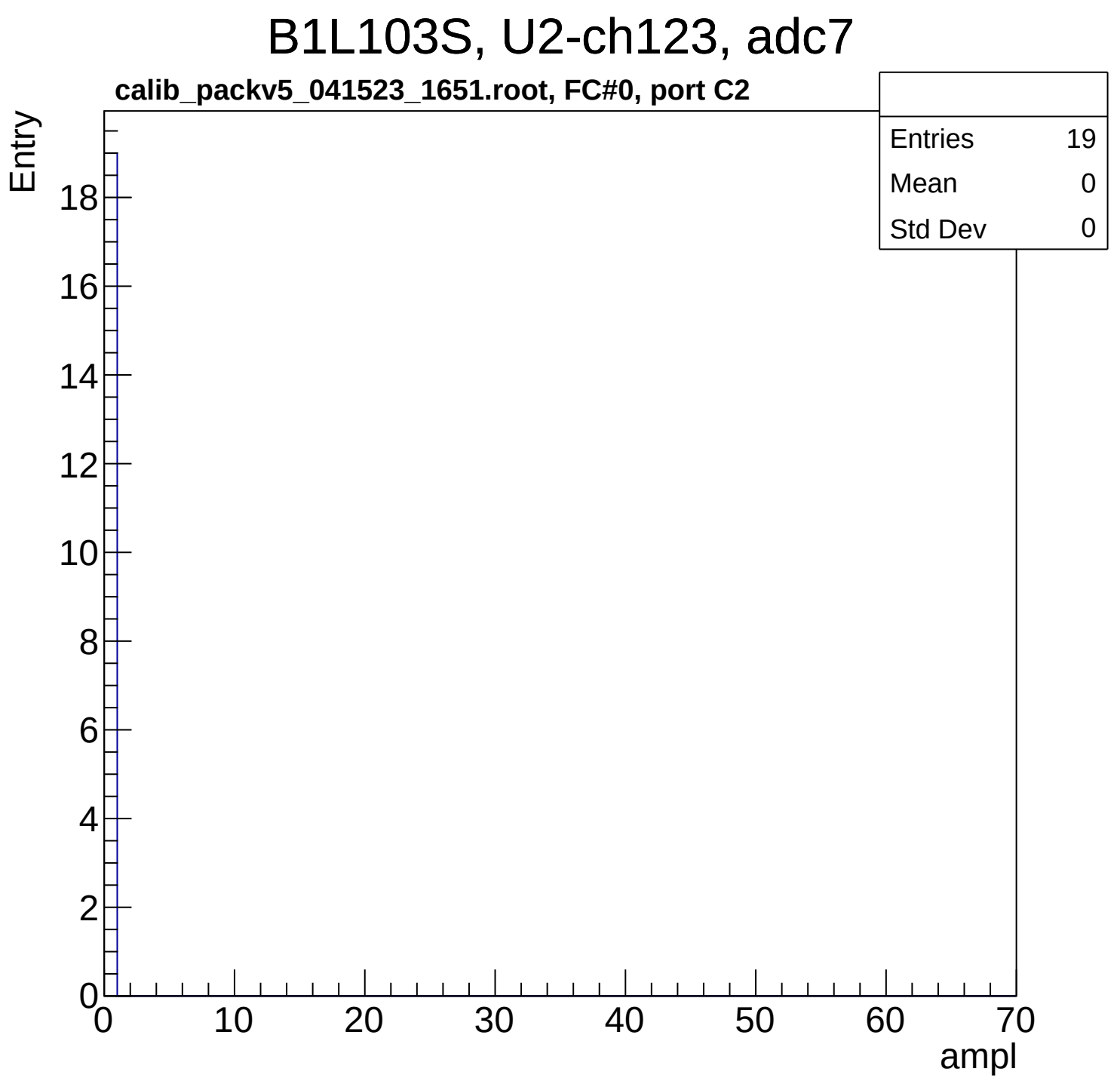

B1L103S, U2-ch123, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 36.57
Std Dev 15.52
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

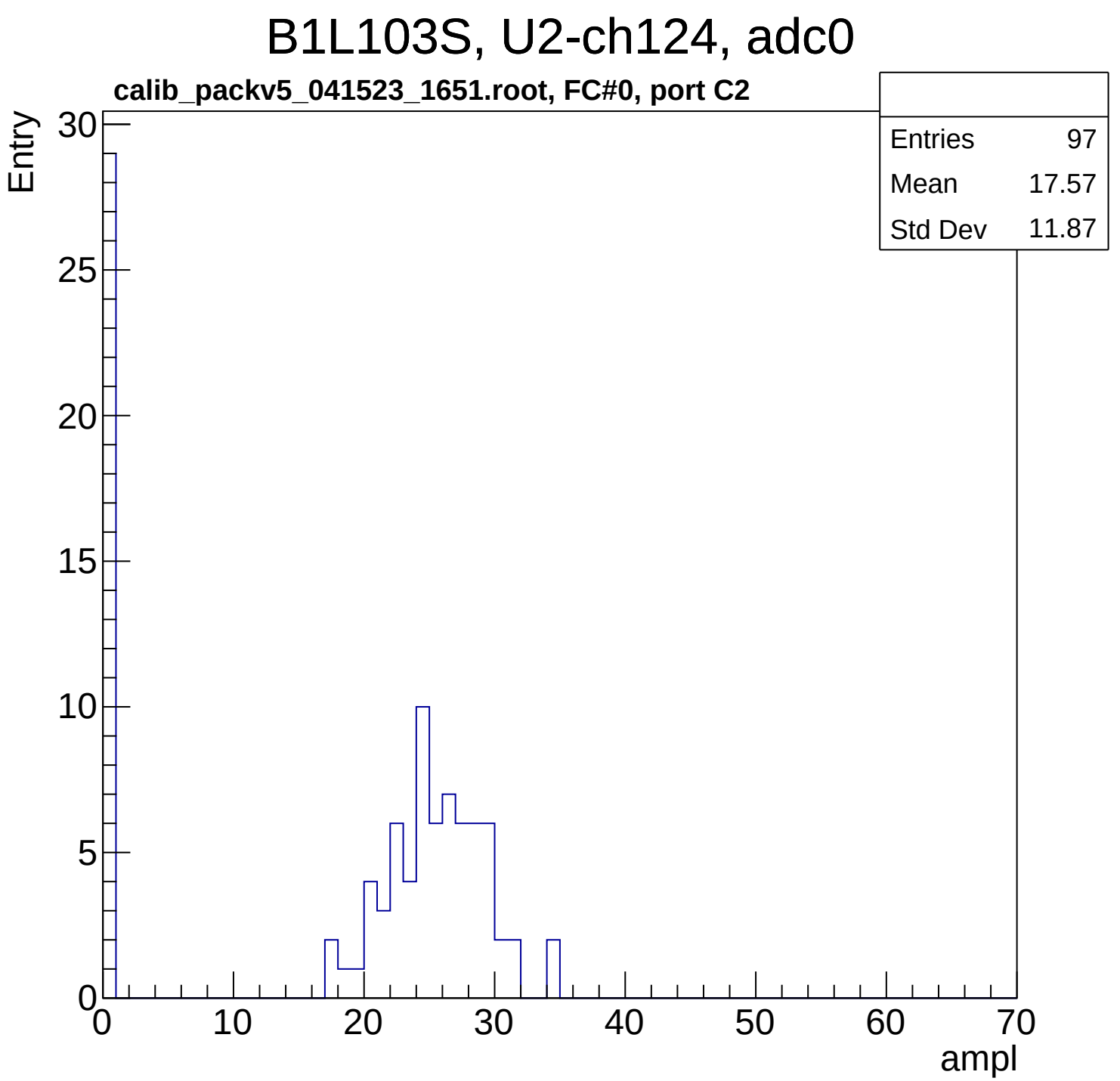

B1L103S, U2-ch123, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 46.33
Std Dev 10.92
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

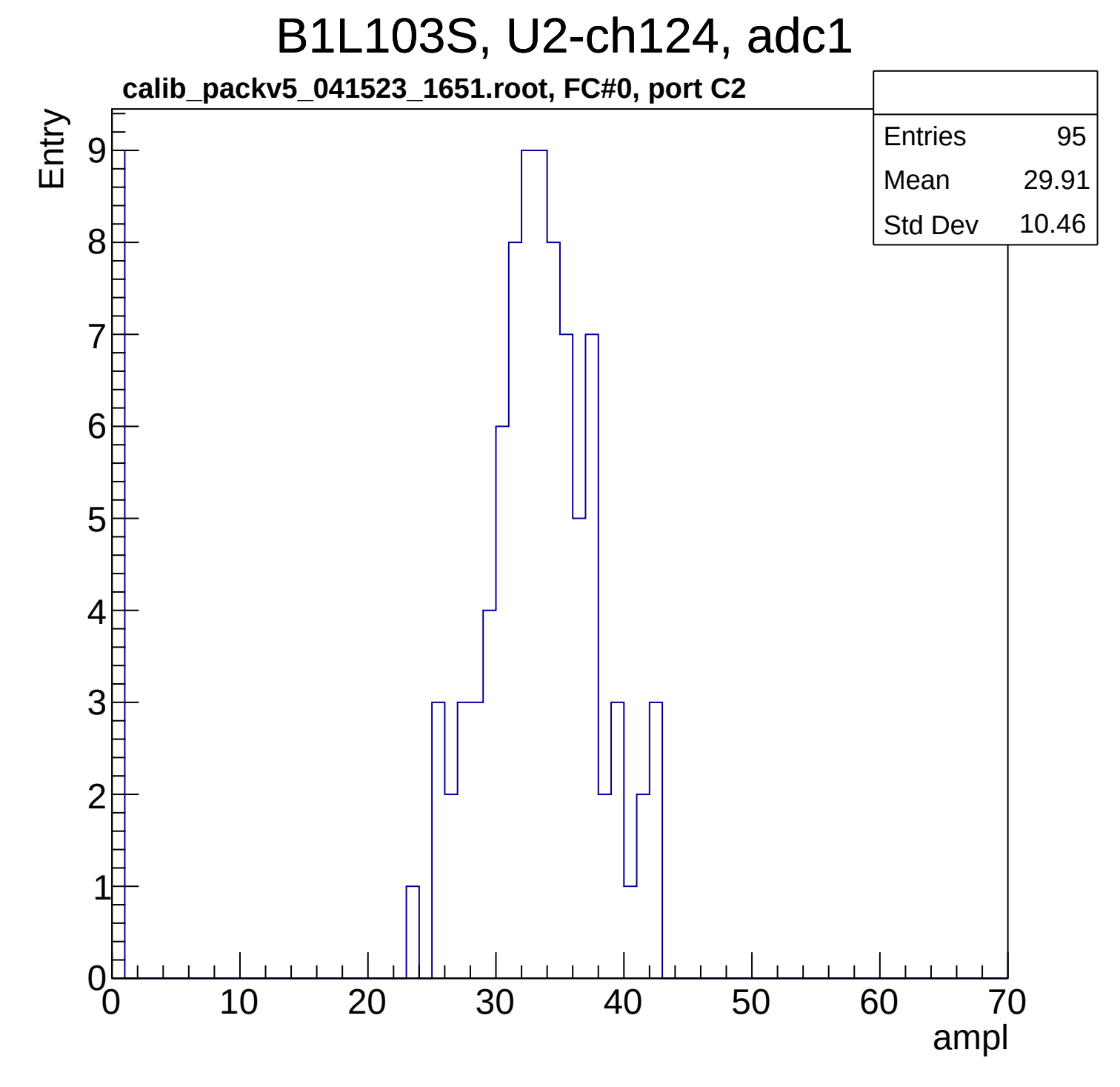

B1L103S, U2-ch123, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 54.46
Std Dev 3.412
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

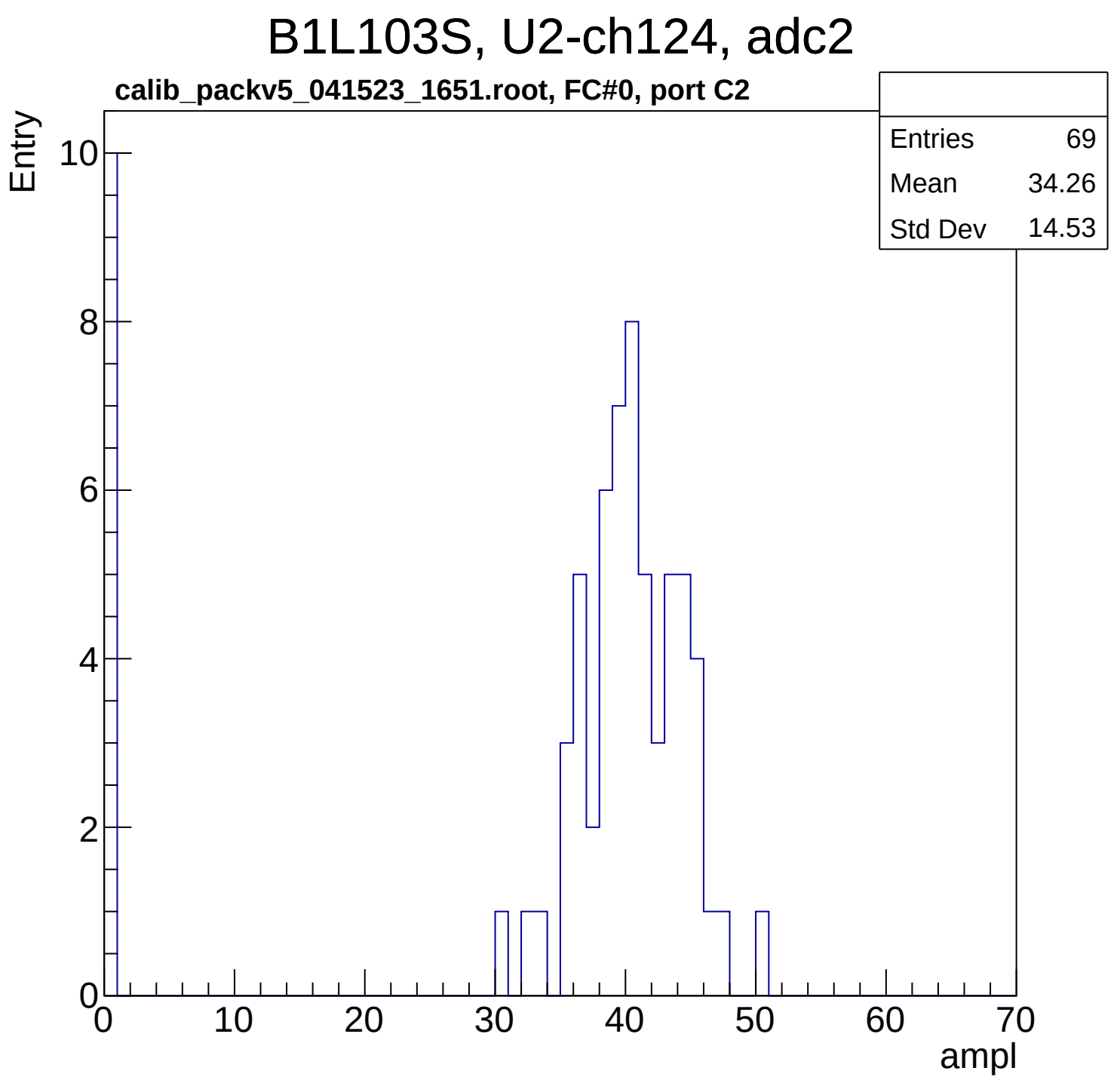

B1L103S, U2-ch123, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 59.25
Std Dev 2.813
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

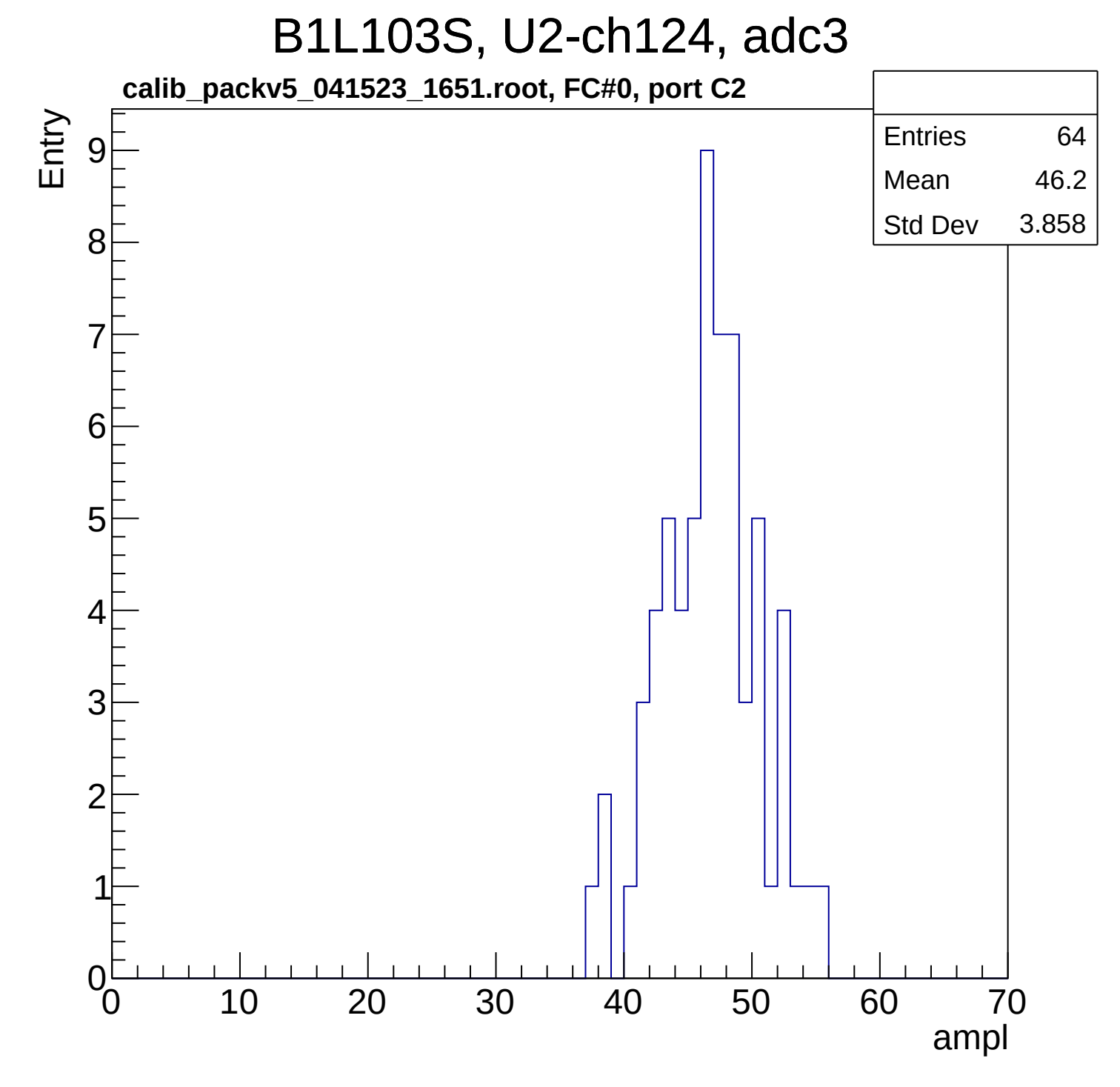

B1L103S, U2-ch123, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 57.37
Std Dev 13.68
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

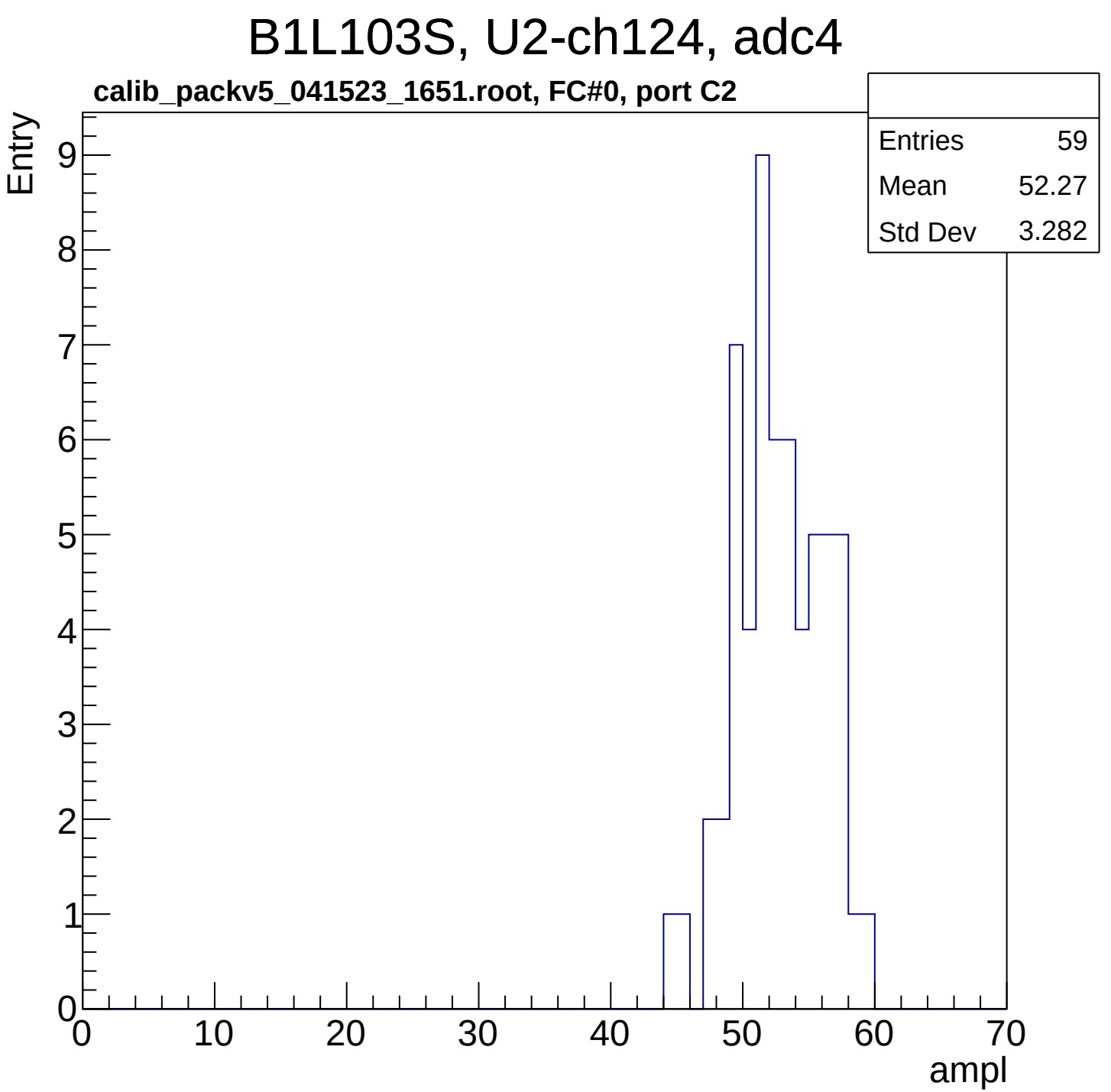

B1L103S, U2-ch123, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

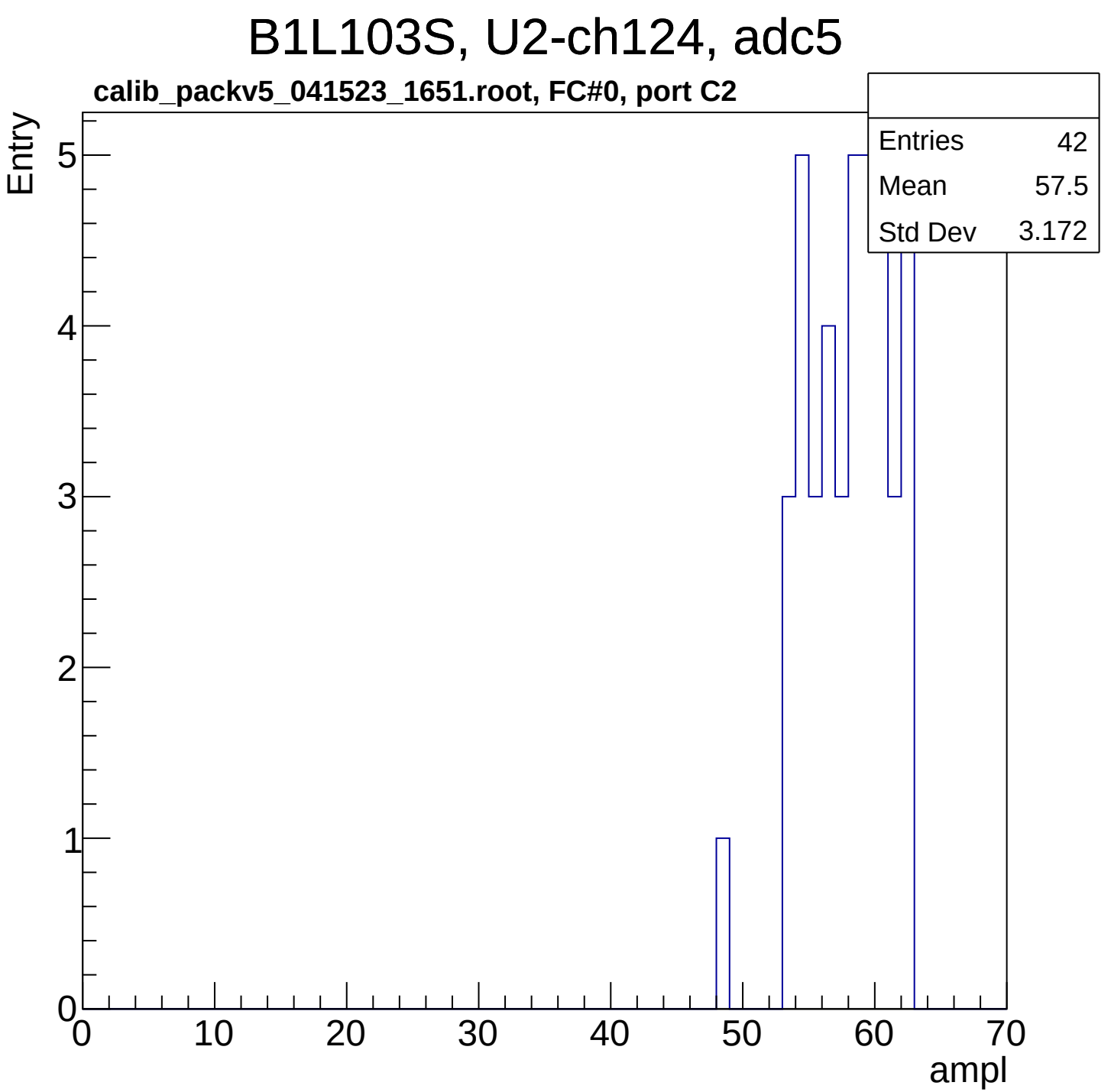

B1L103S, U2-ch124, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 17.57
Std Dev 11.87
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70

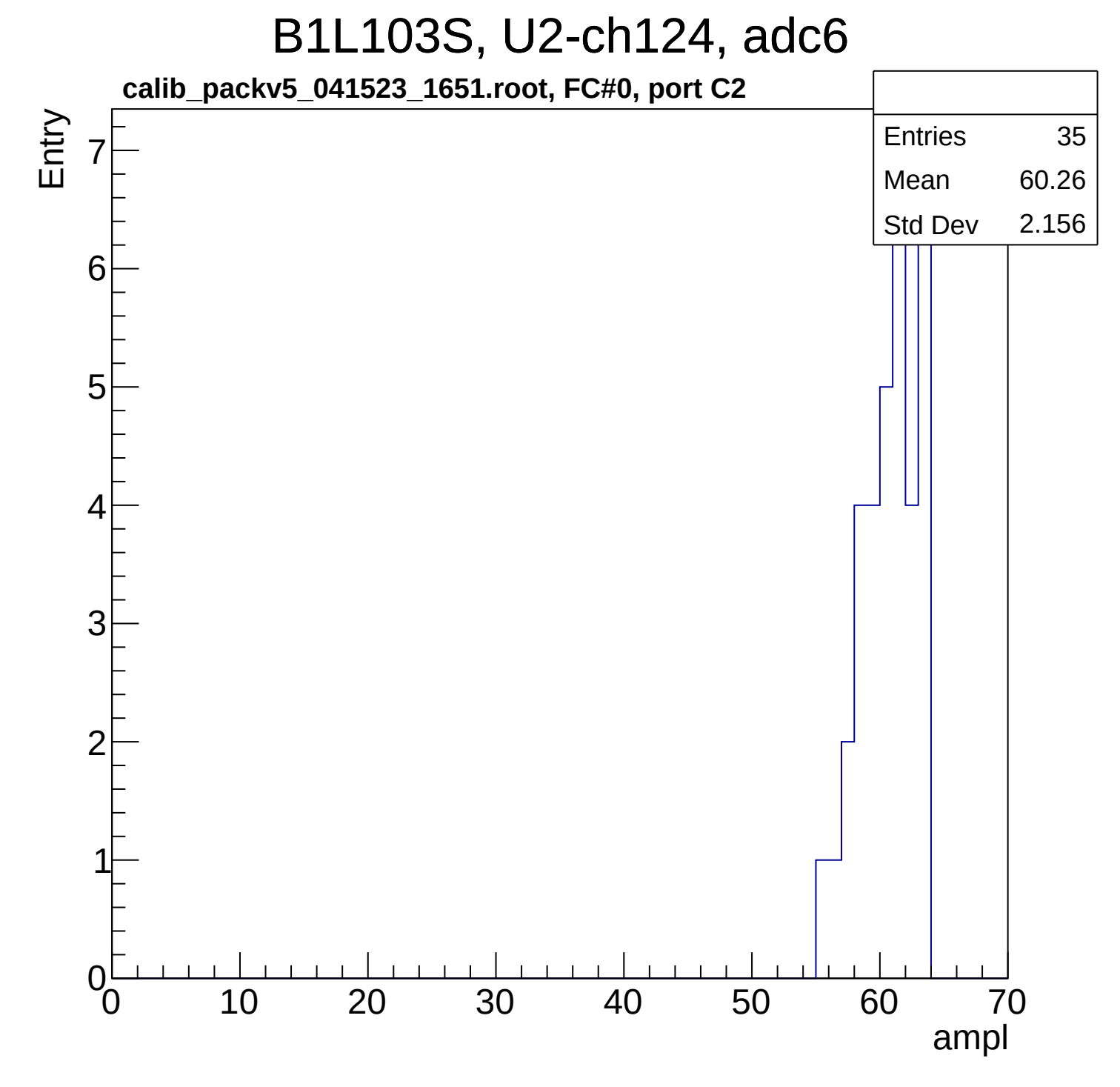

B1L103S, U2-ch124, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 29.91
Std Dev 10.46
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

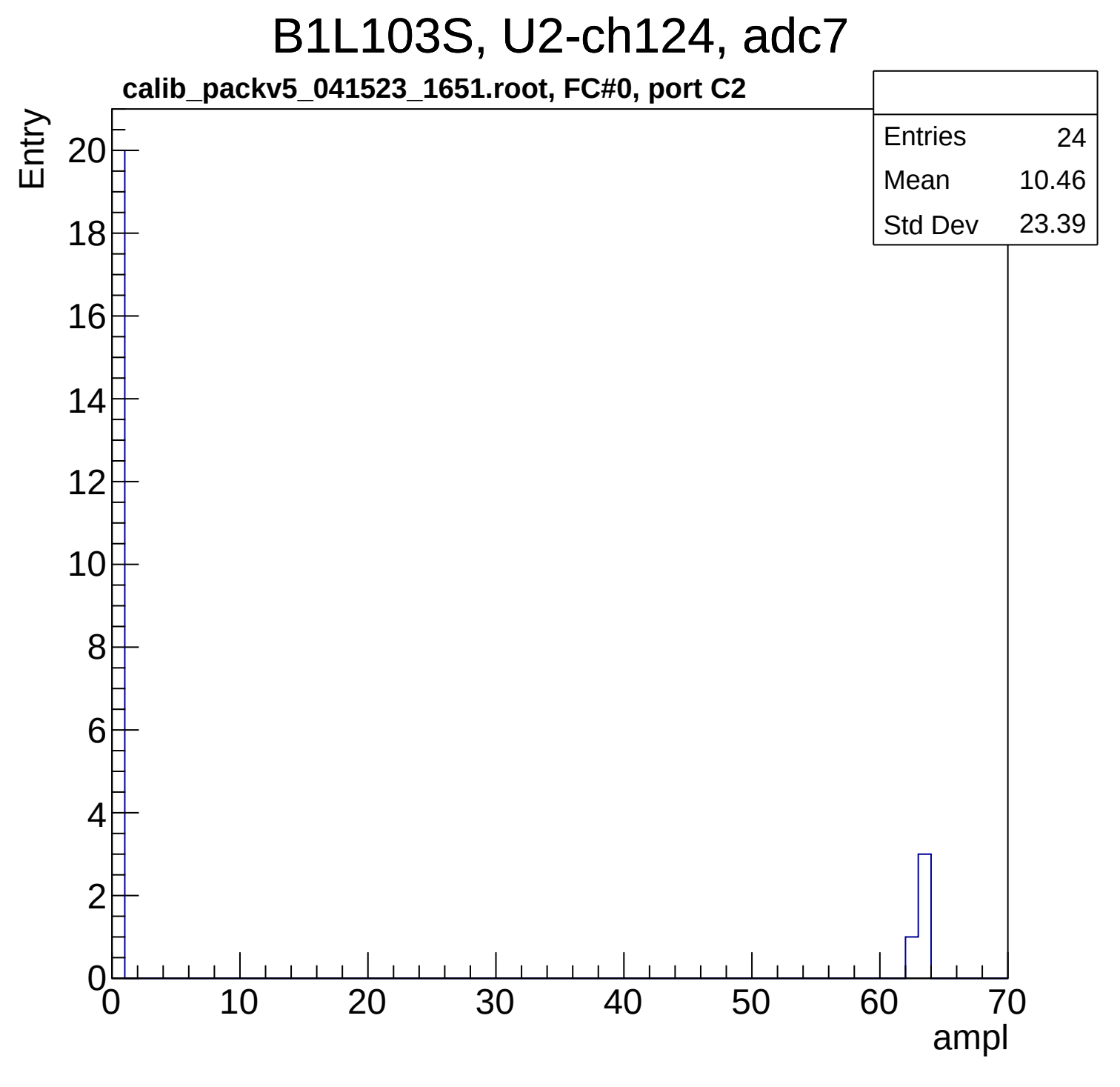

B1L103S, U2-ch124, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 34.26
Std Dev 14.53
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

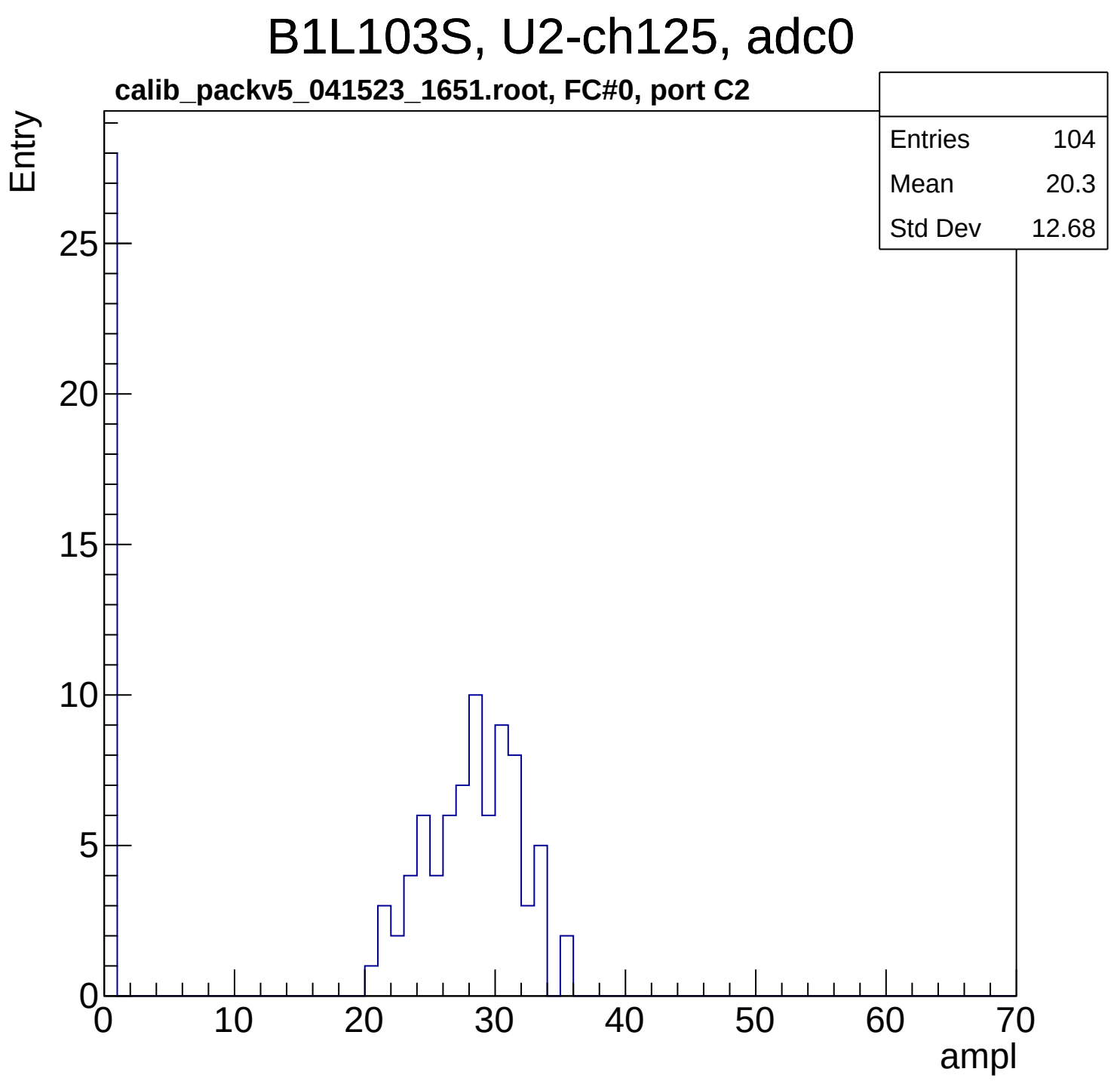

B1L103S, U2-ch124, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 46.2
Std Dev 3.858
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

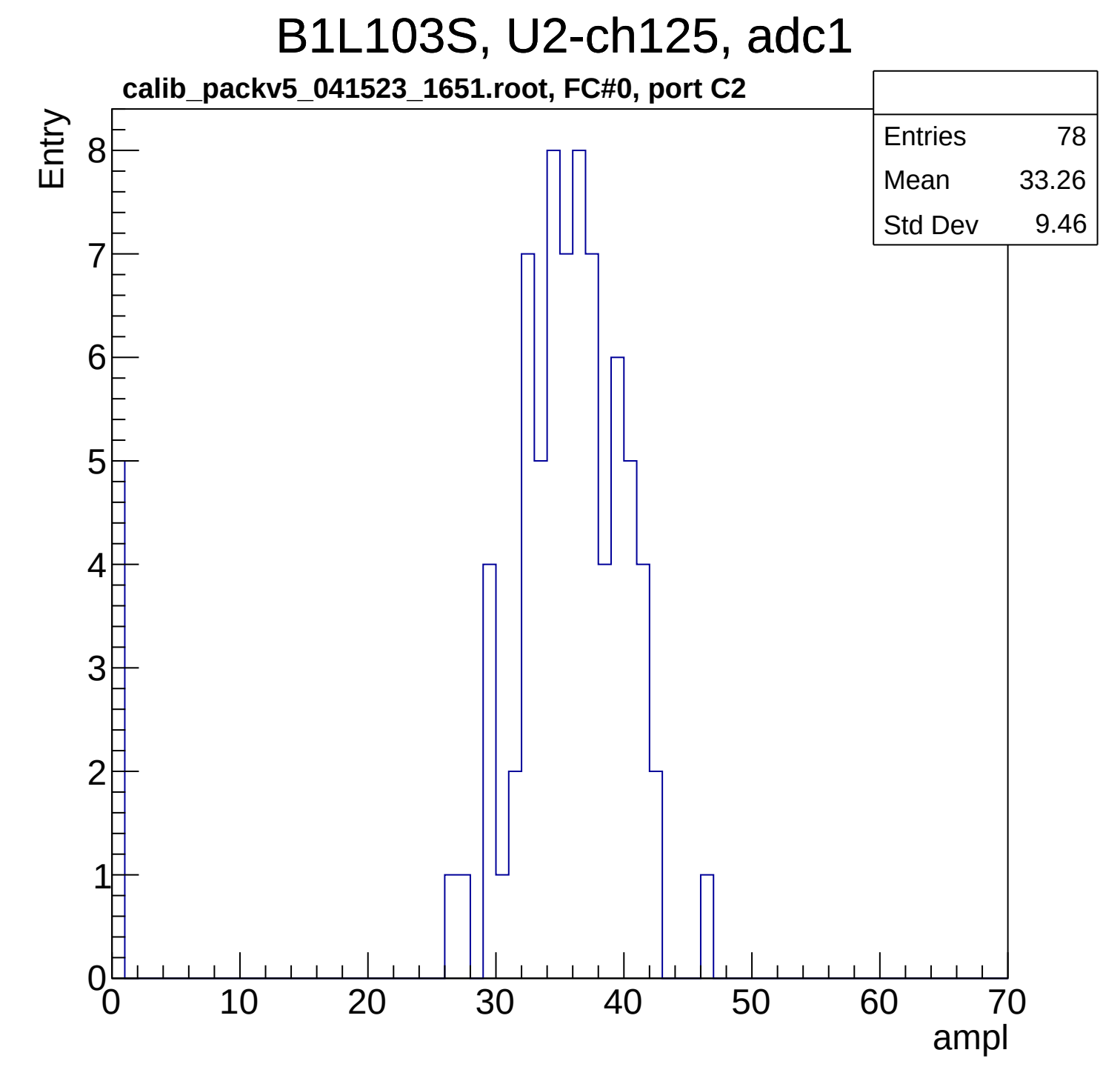

B1L103S, U2-ch124, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 52.27
Std Dev 3.282
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

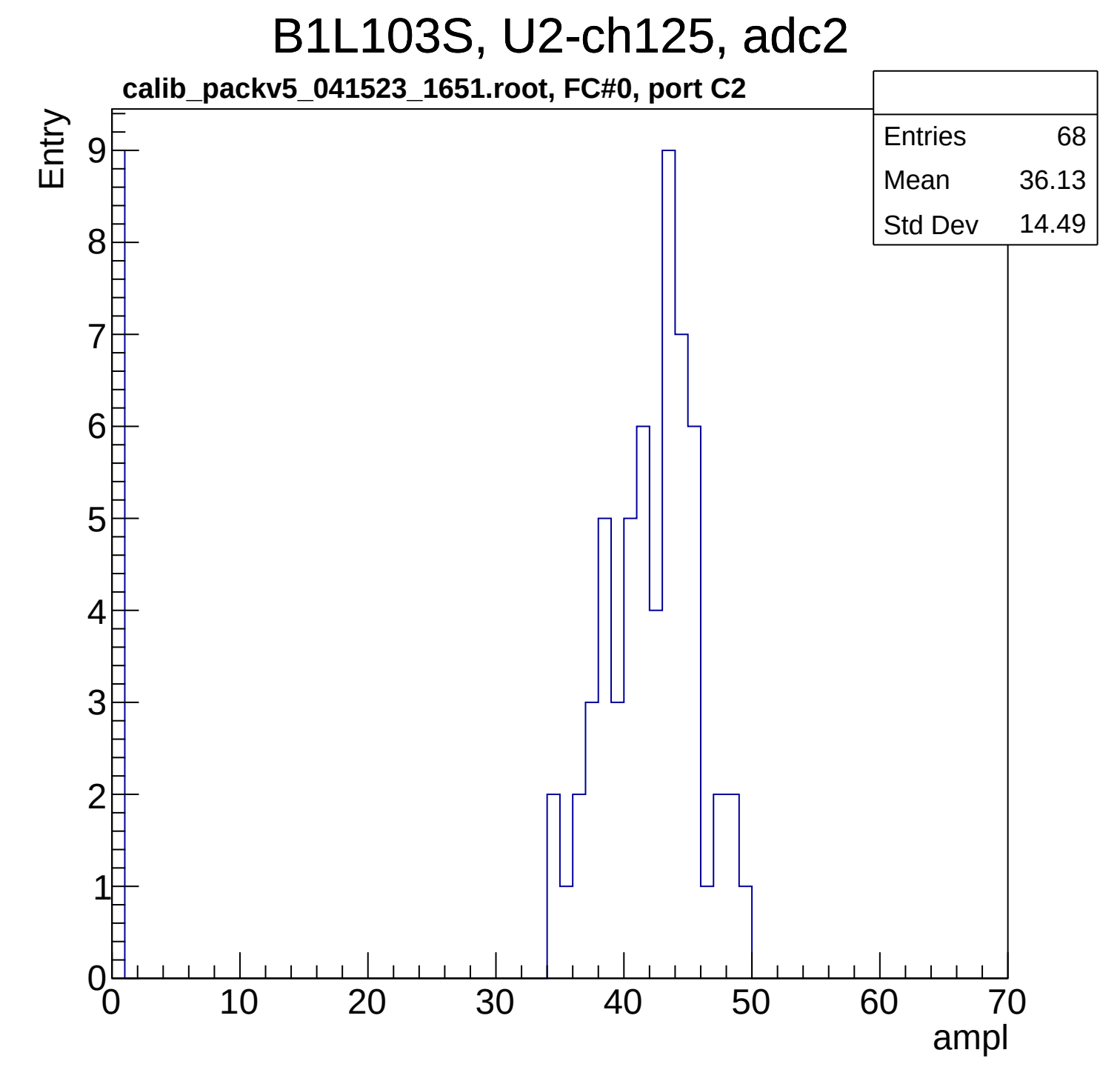

B1L103S, U2-ch124, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 57.5
Std Dev 3.172
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

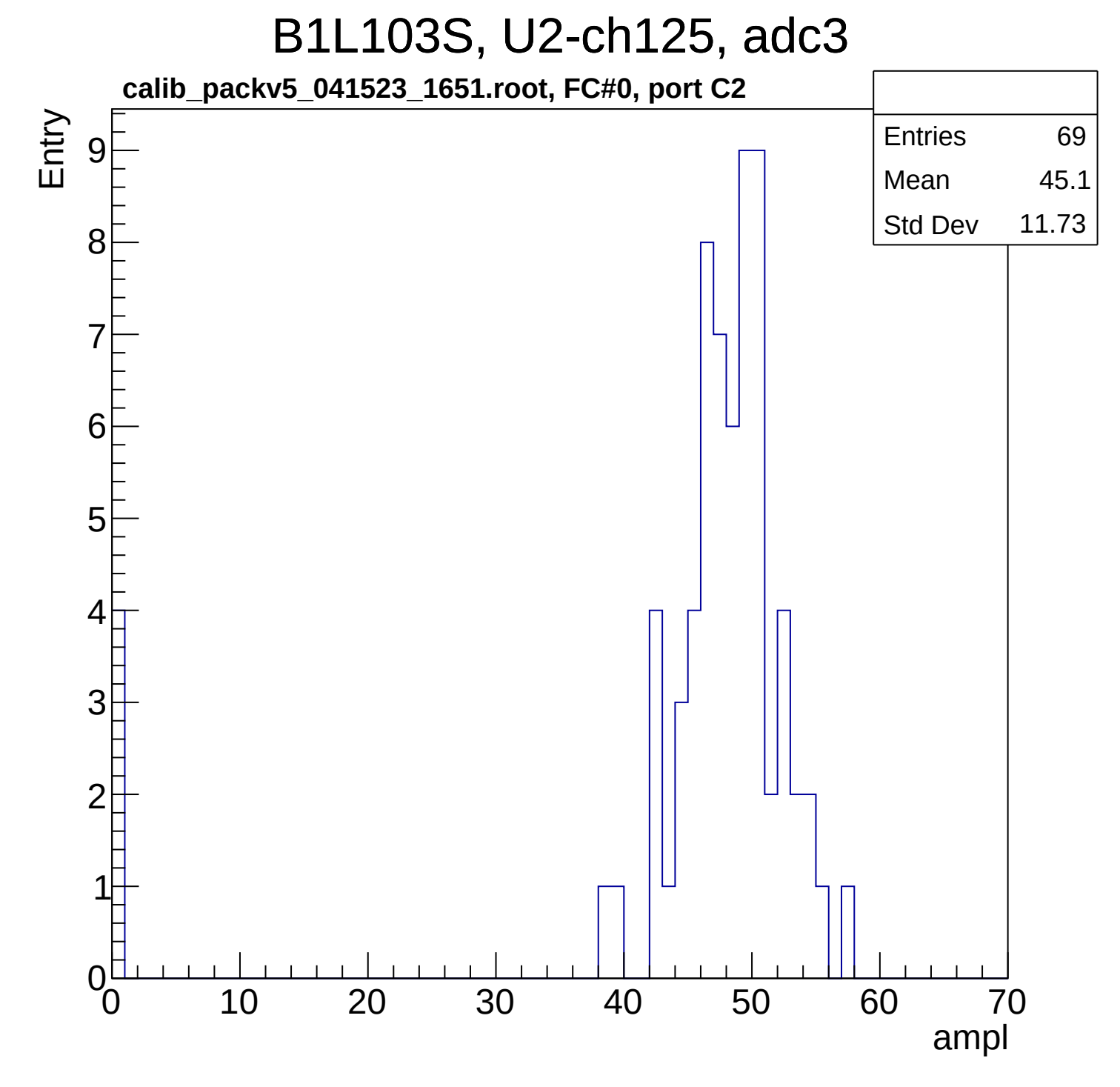

B1L103S, U2-ch124, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 60.26
Std Dev 2.156
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

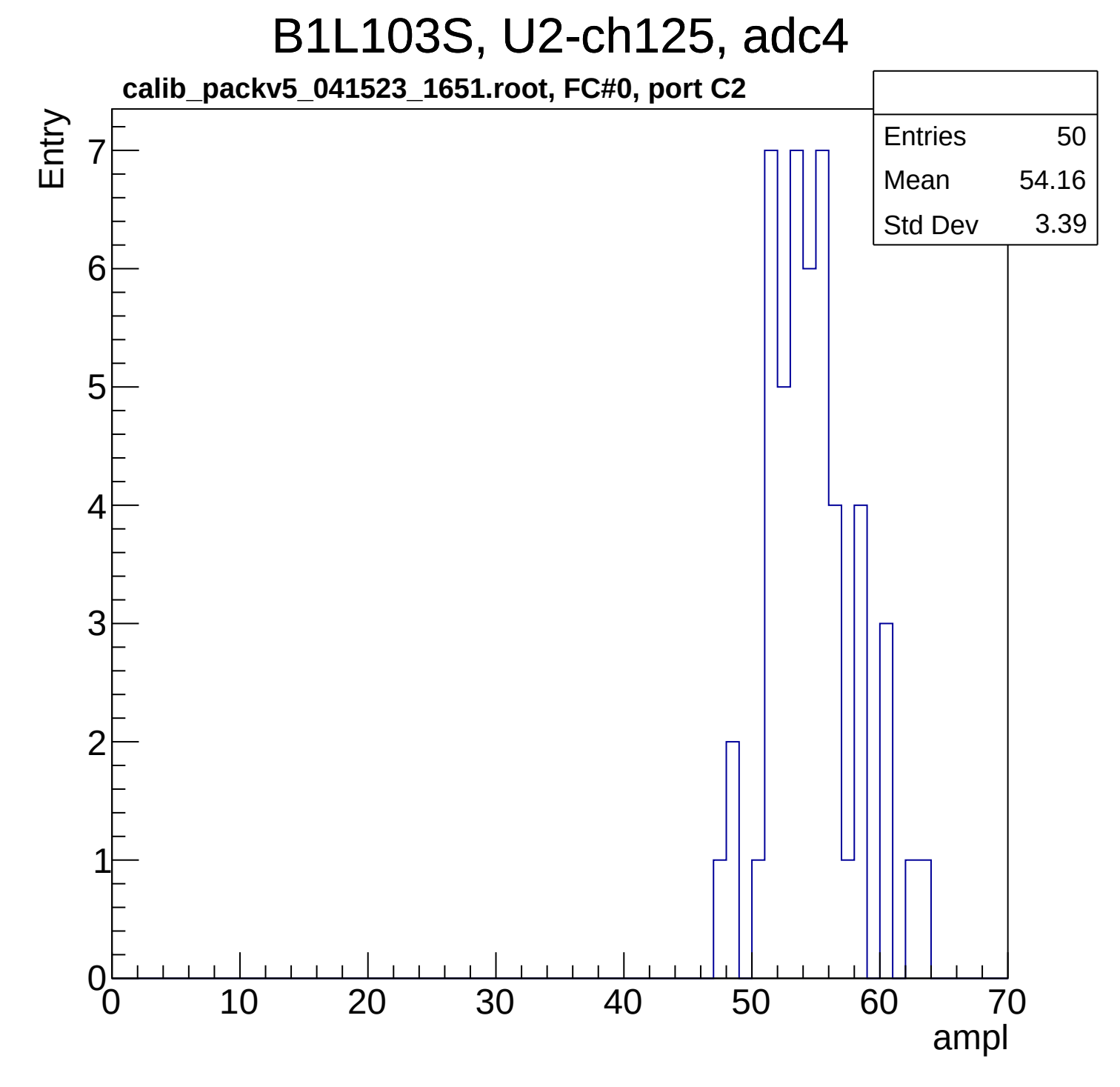

B1L103S, U2-ch124, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 10.46
Std Dev 23.39
Entry
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
50
60
70
ampl

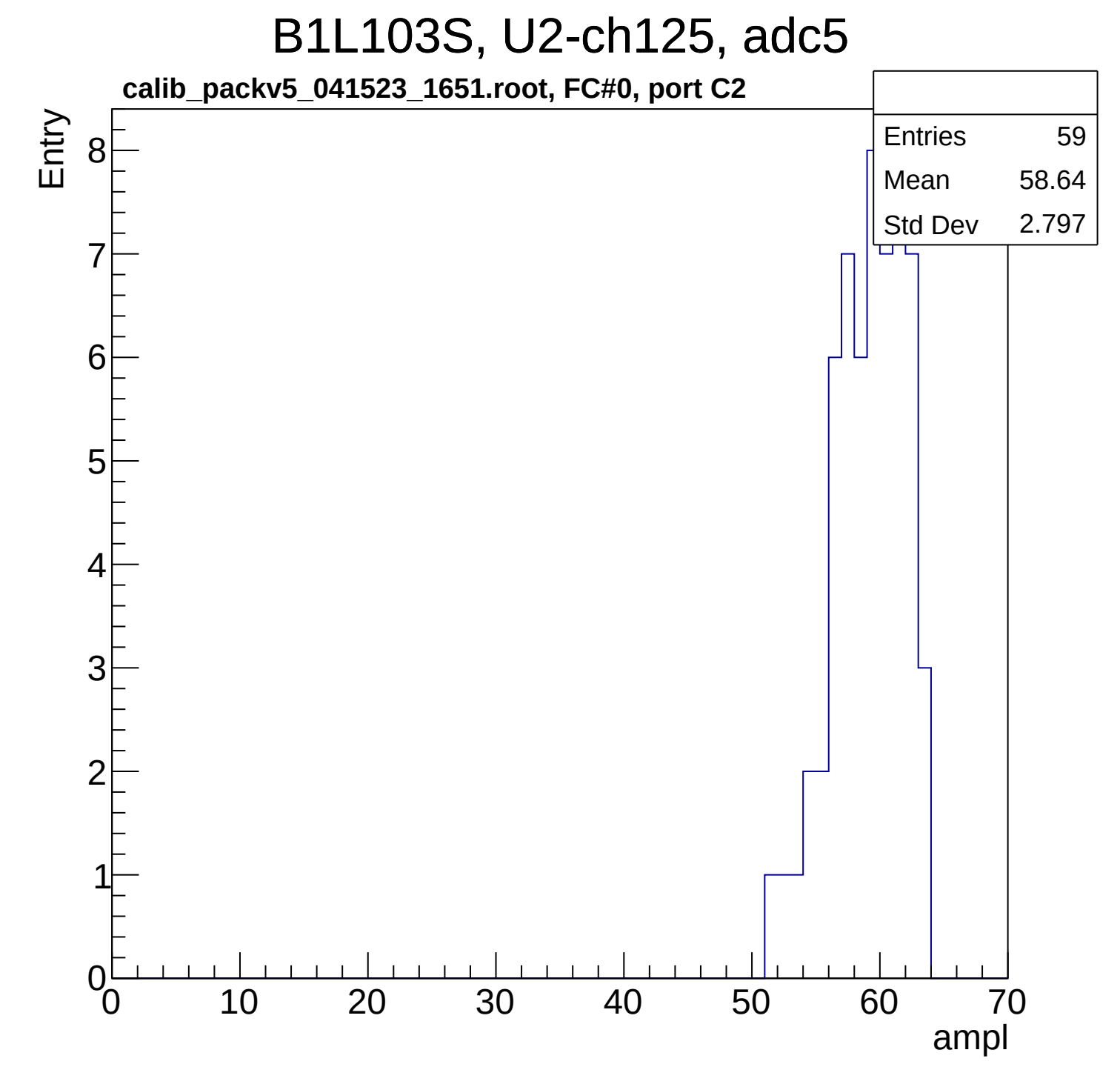

B1L103S, U2-ch125, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 20.3
Std Dev 12.68
Entry
0
5
10
15
20
25
0
10
20
30
40
50
60
70
ampl

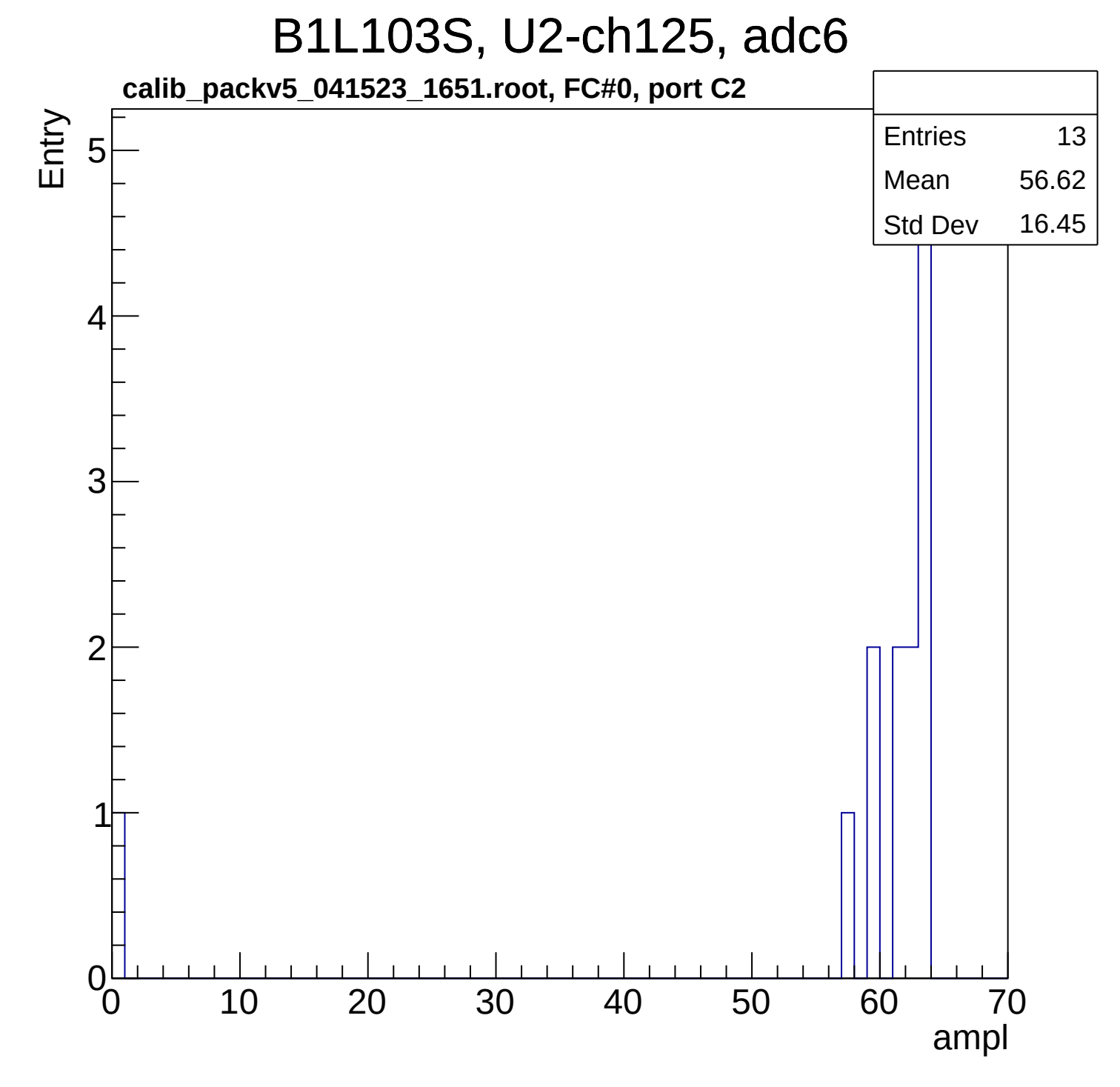

B1L103S, U2-ch125, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 33.26
Std Dev 9.46
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

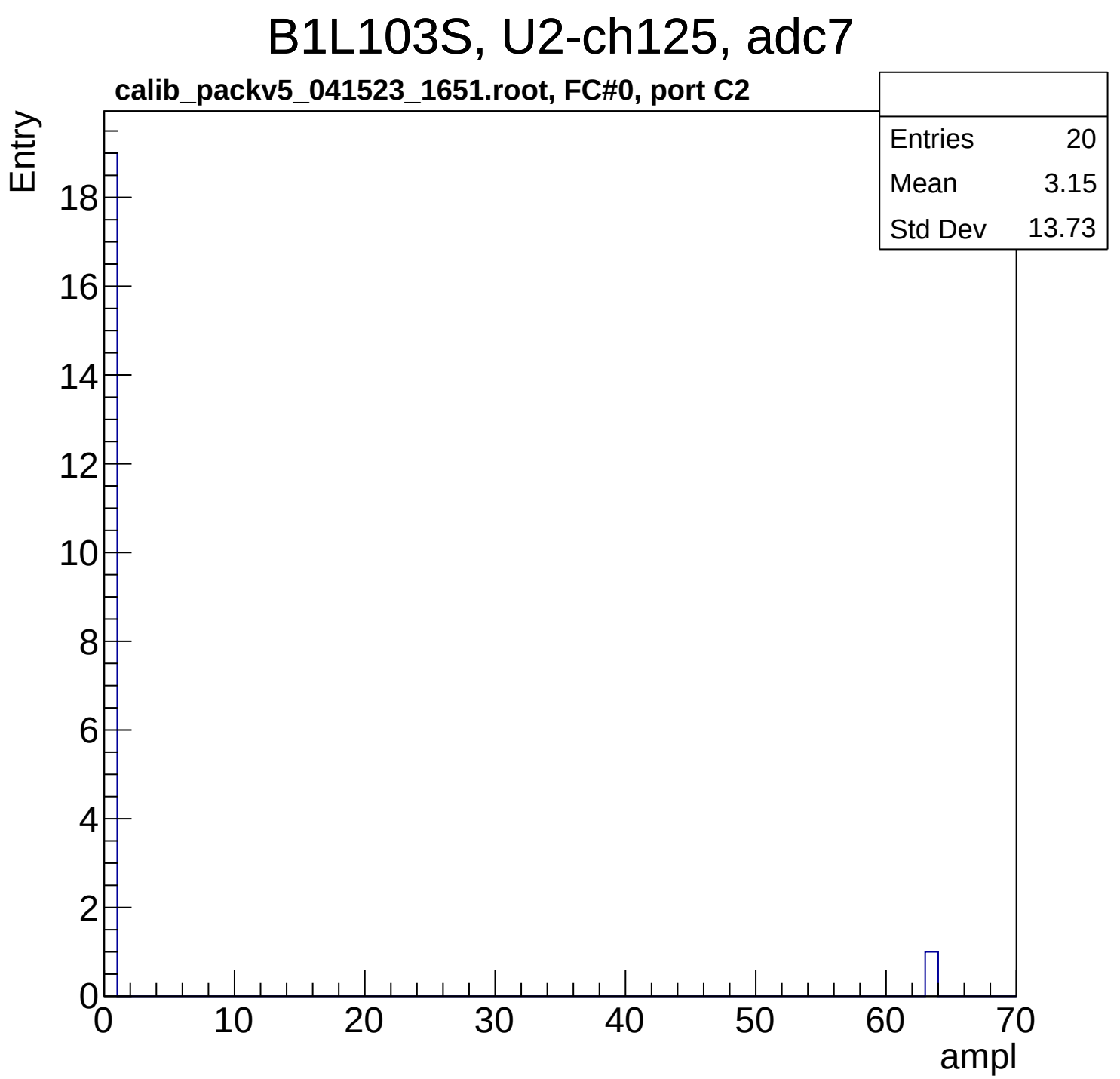

B1L103S, U2-ch125, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 36.13
Std Dev 14.49
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

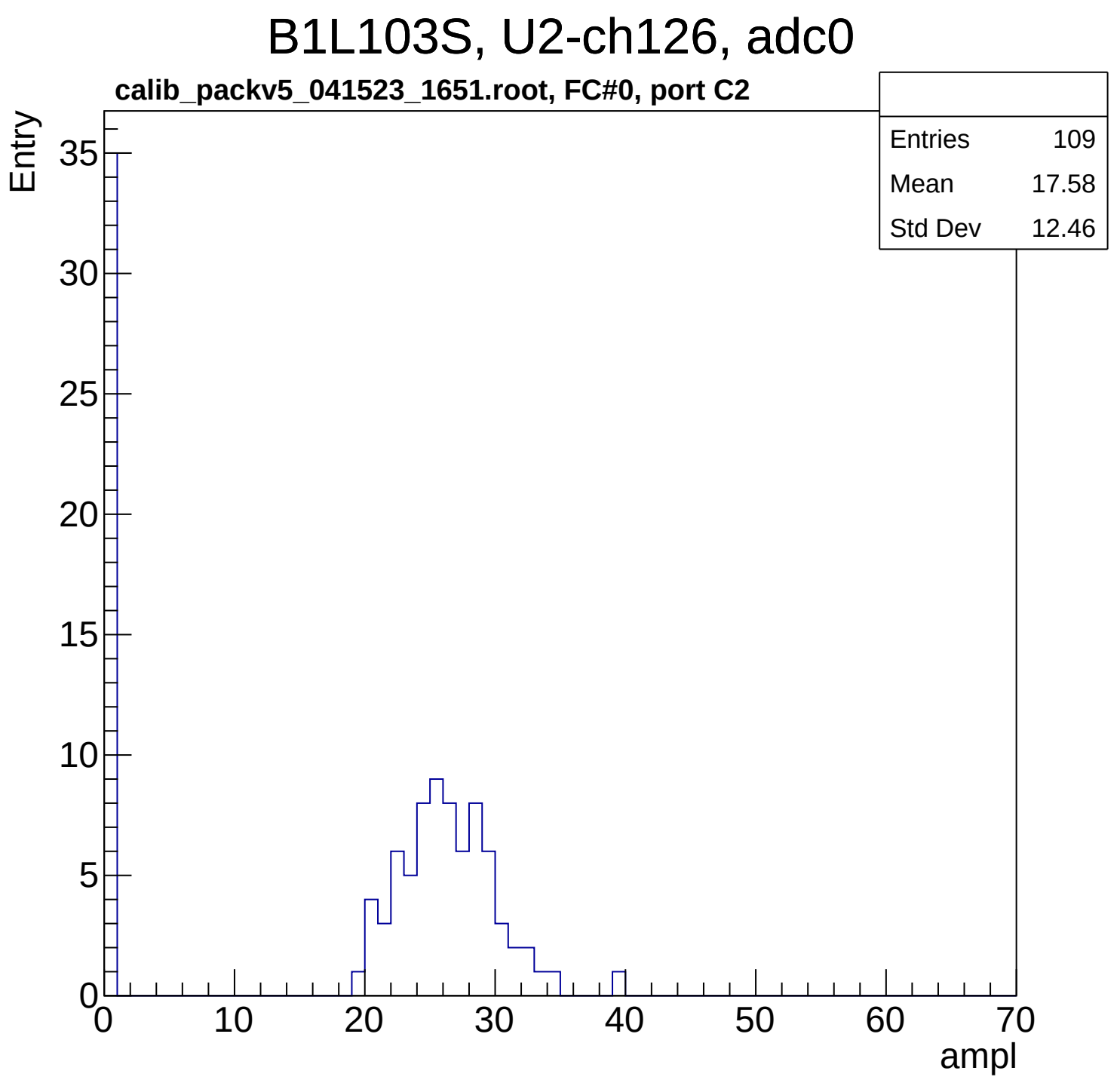

B1L103S, U2-ch125, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 45.1
Std Dev 11.73
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

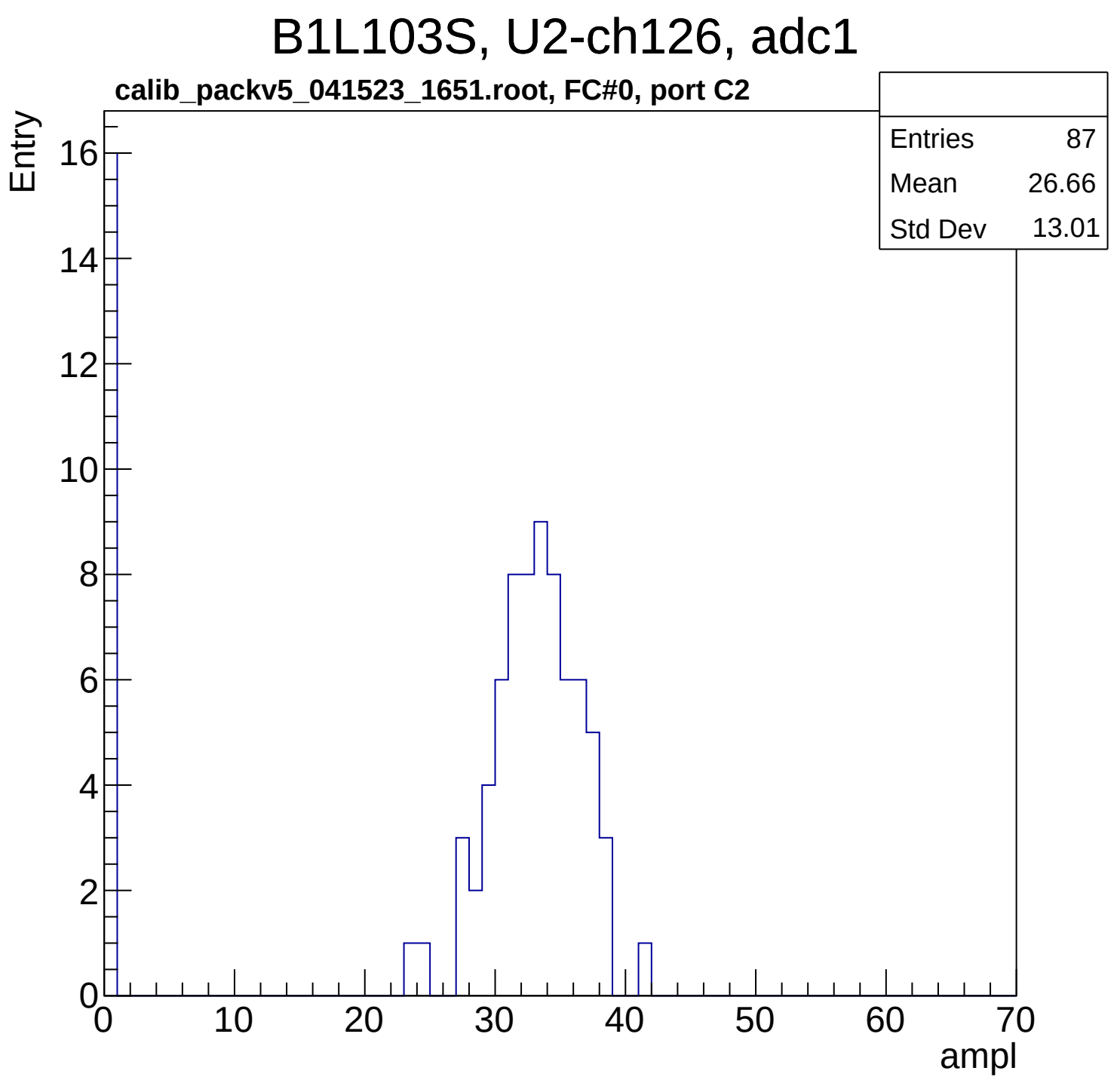

B1L103S, U2-ch125, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 54.16
Std Dev 3.39
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

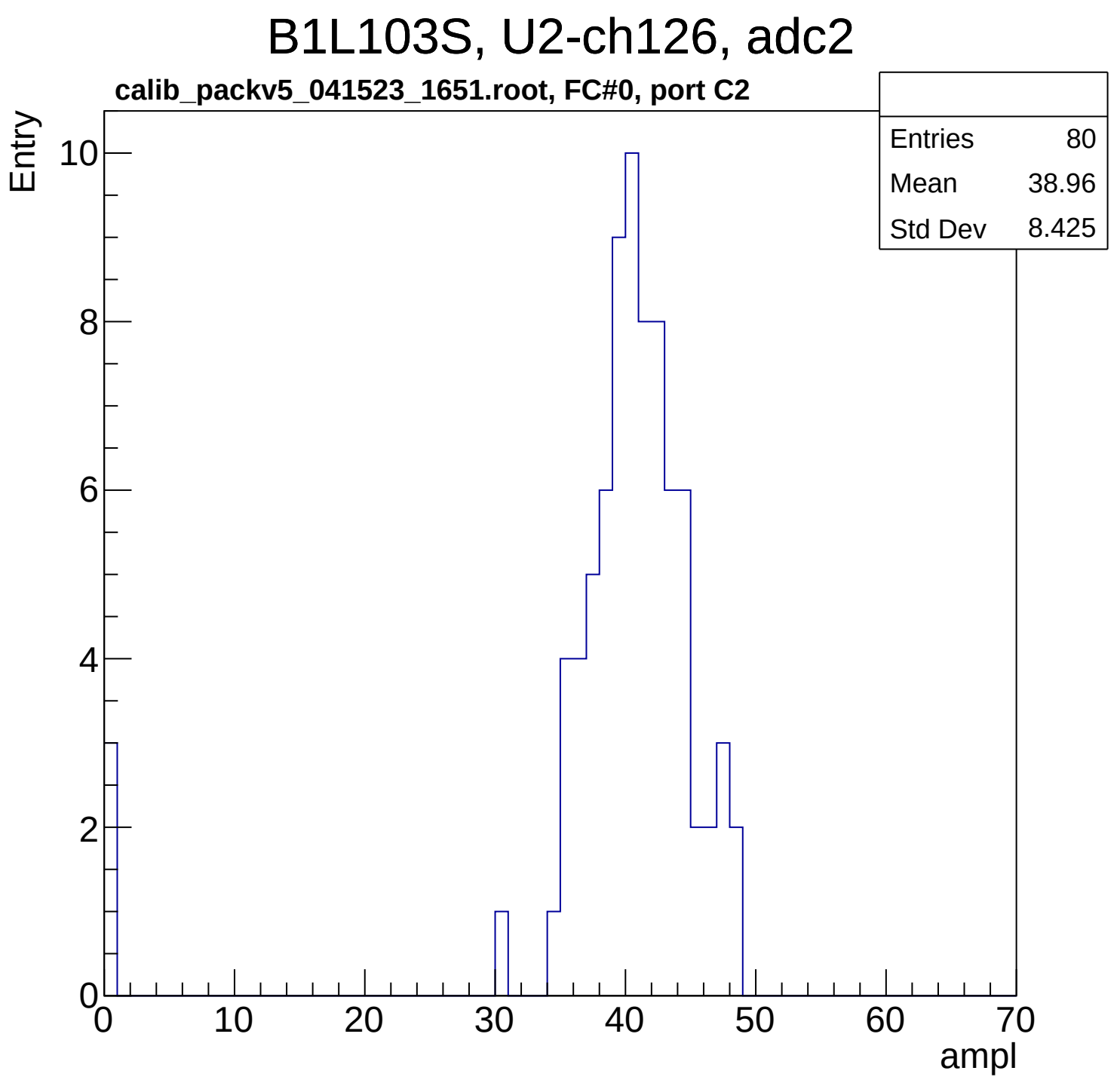

B1L103S, U2-ch125, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 58.64
Std Dev 2.797
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

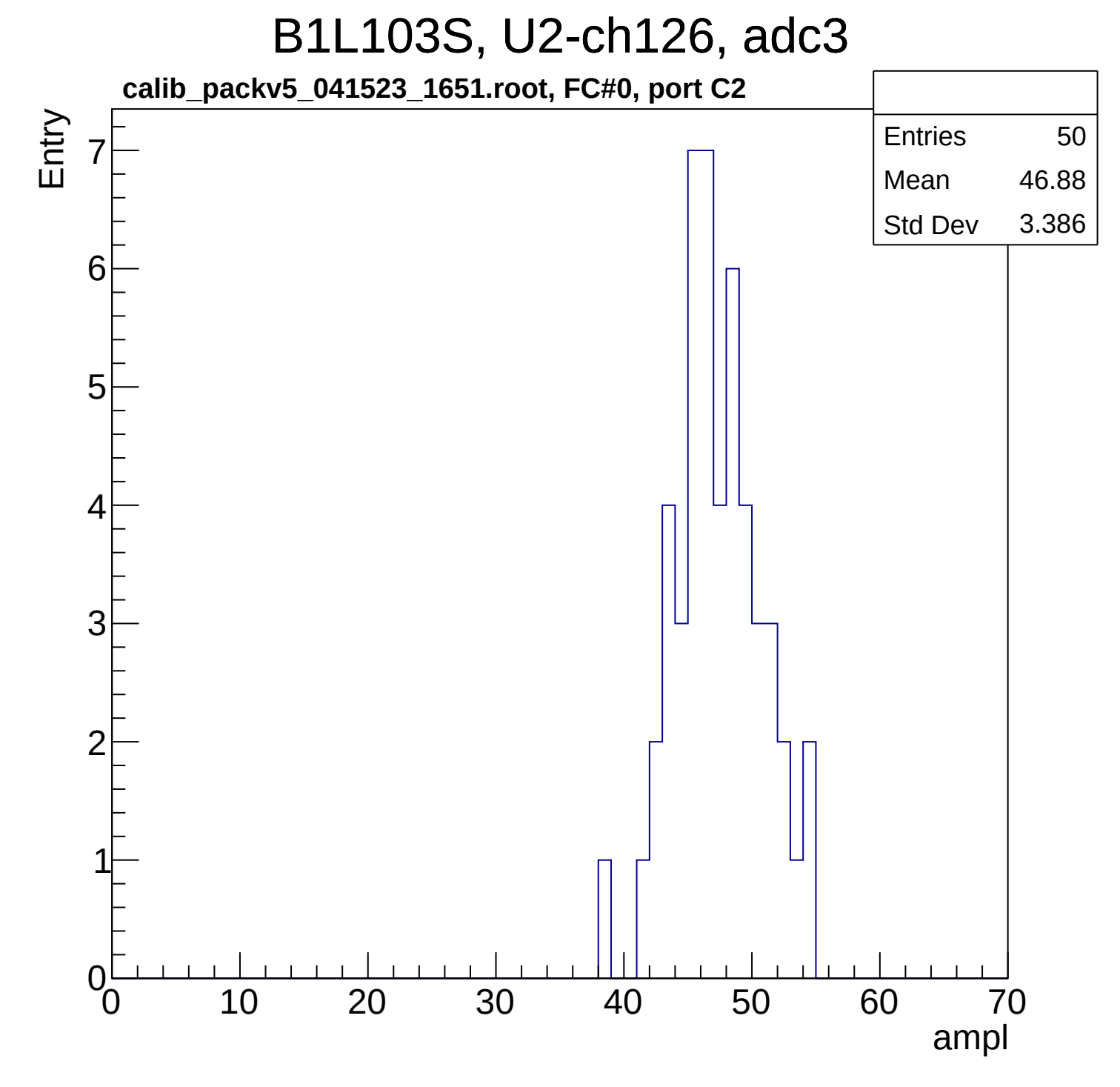

B1L103S, U2-ch125, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 56.62
Std Dev 16.45
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

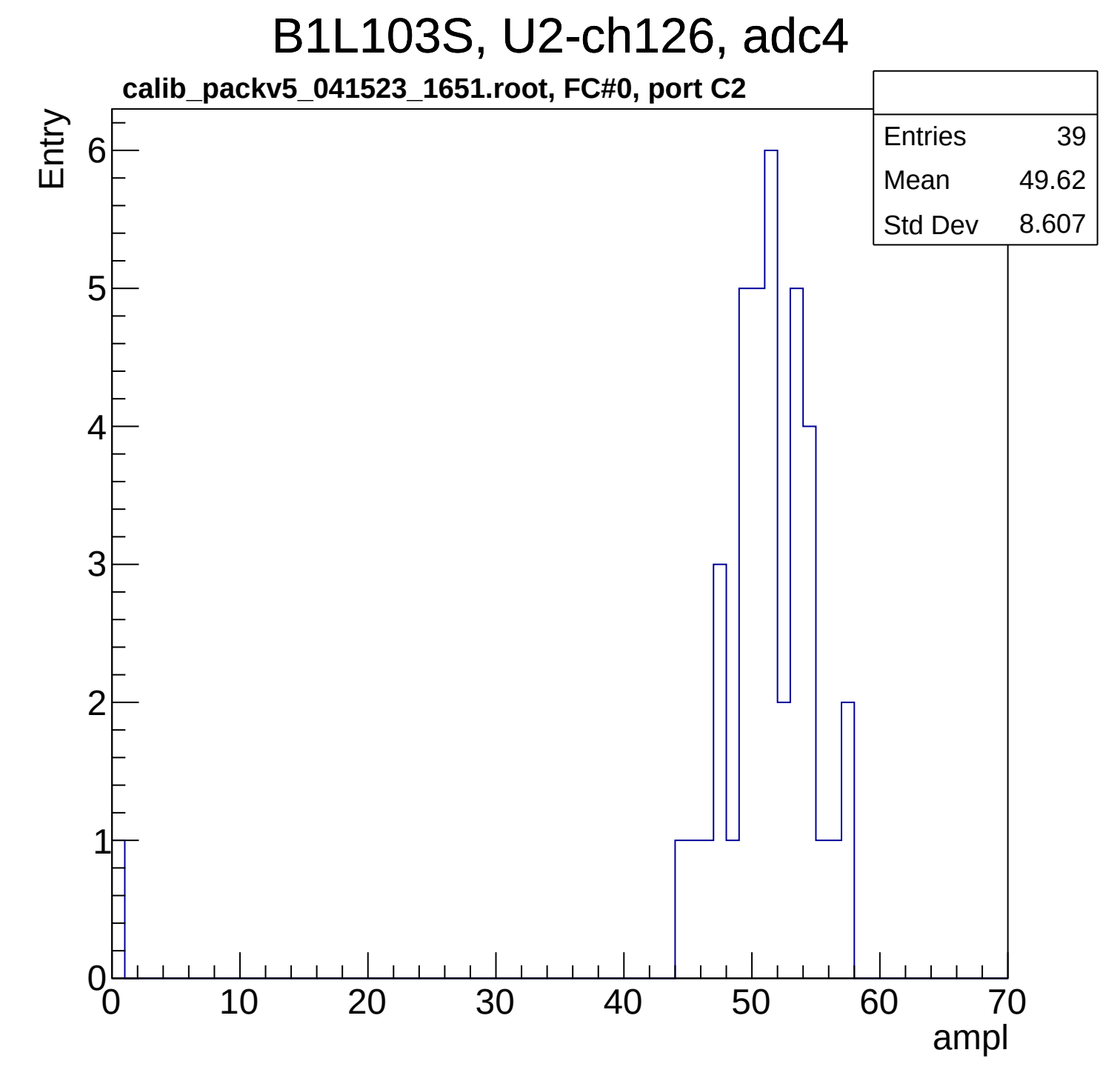

B1L103S, U2-ch125, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

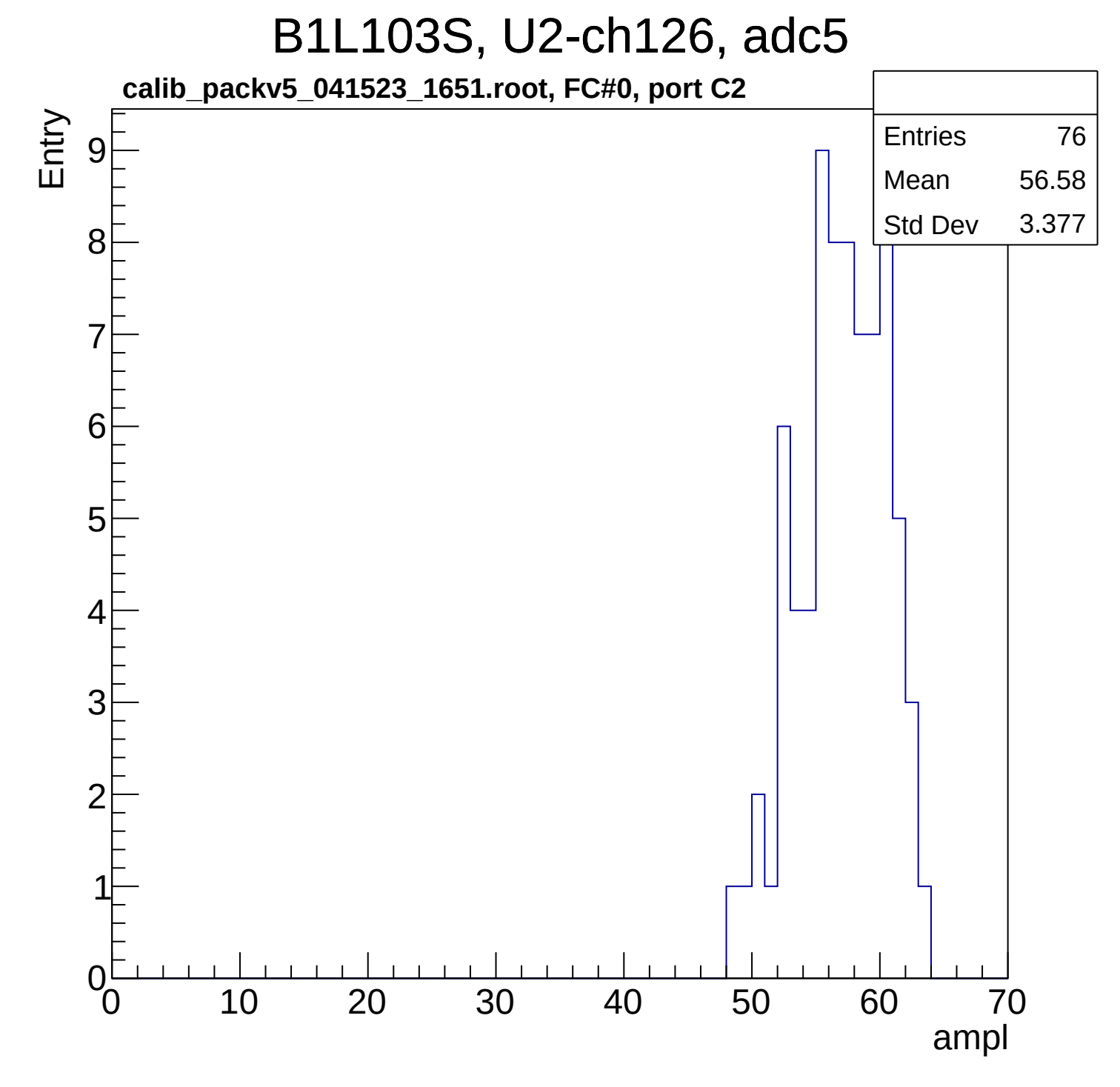

B1L103S, U2-ch126, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 109
Mean 17.58
Std Dev 12.46
Entry
0
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70
ampl

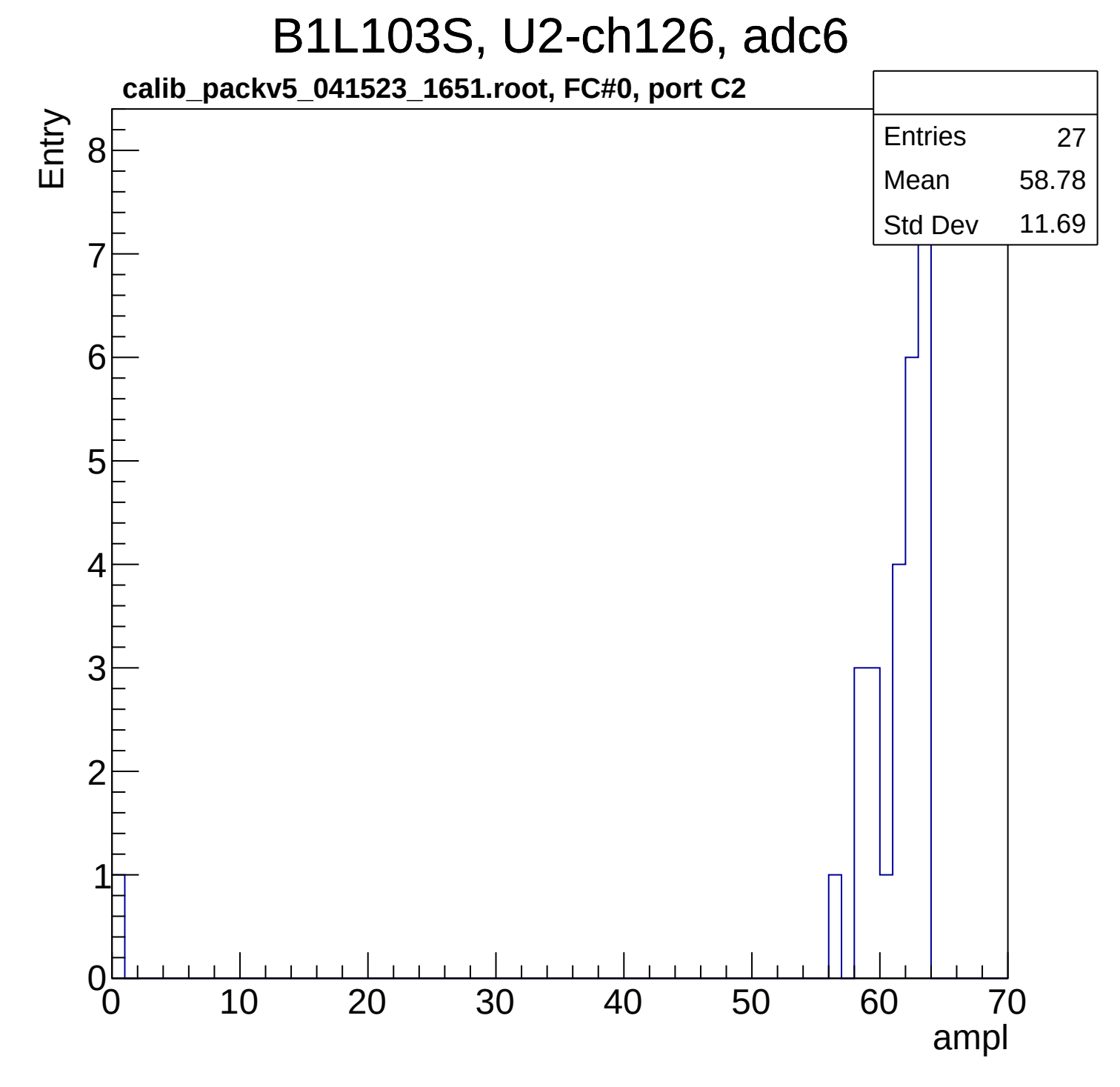

B1L103S, U2-ch126, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 26.66
Std Dev 13.01
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

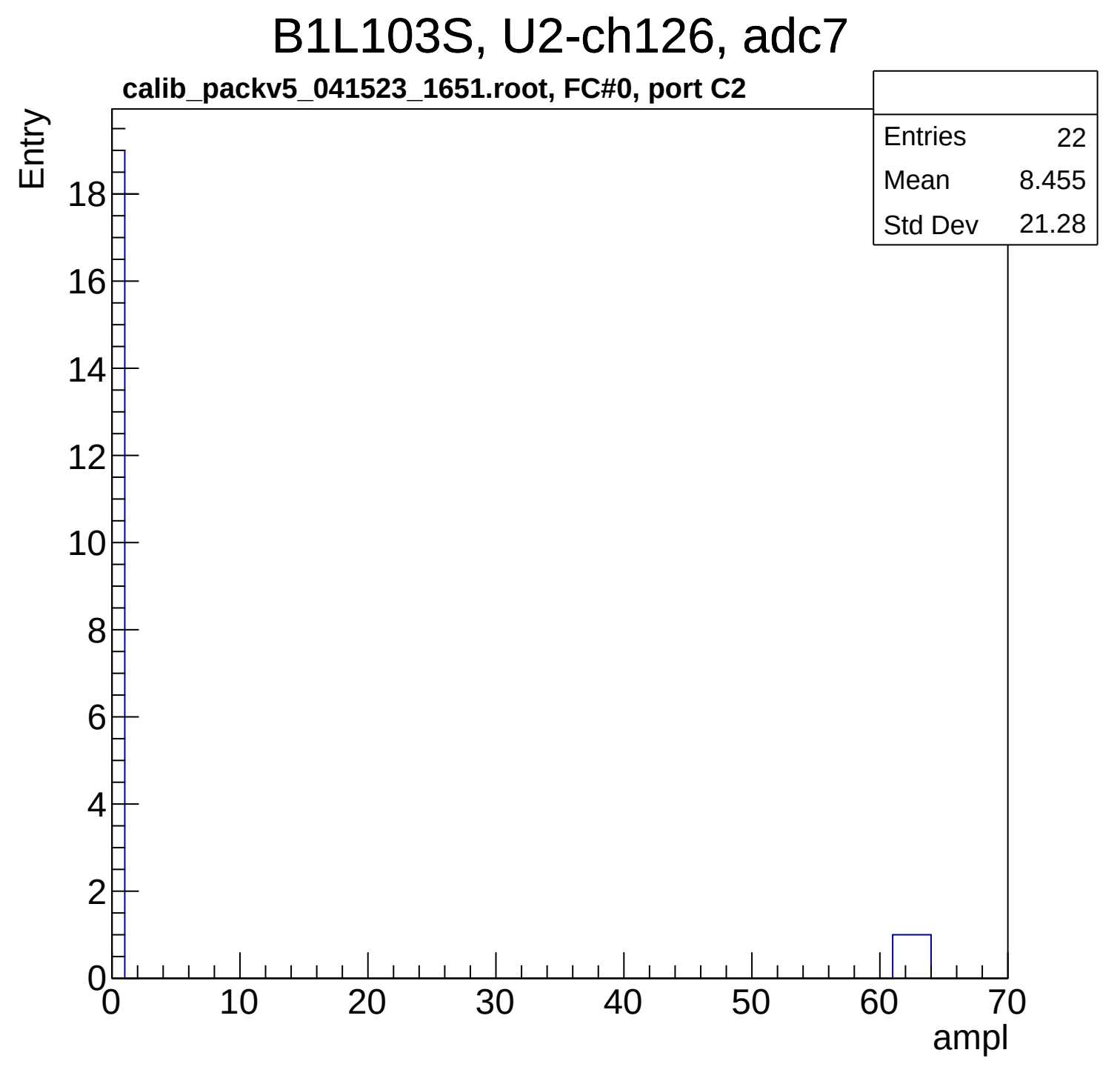

B1L103S, U2-ch126, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 38.96
Std Dev 8.425
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

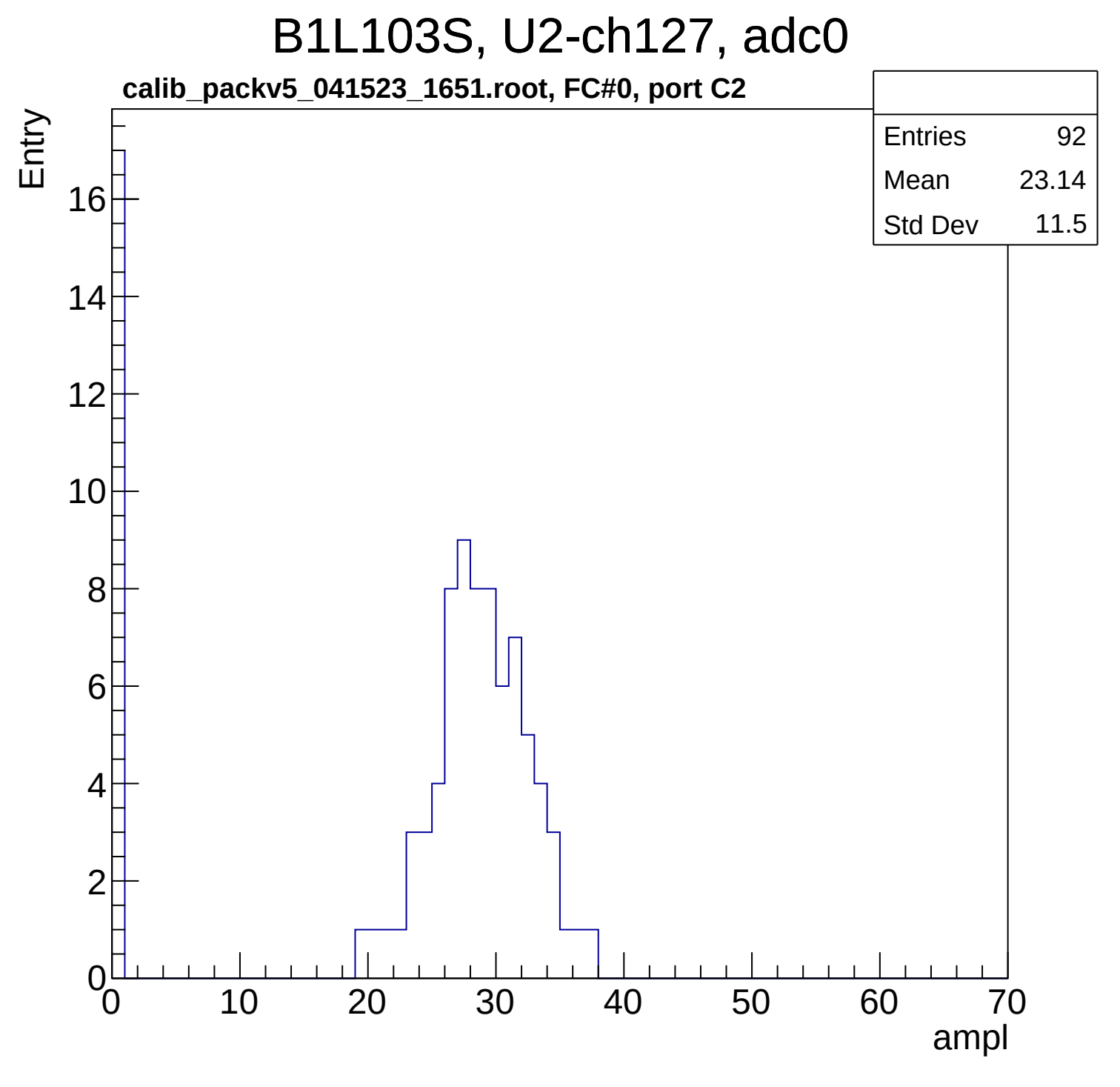

B1L103S, U2-ch126, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 46.88
Std Dev 3.386
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

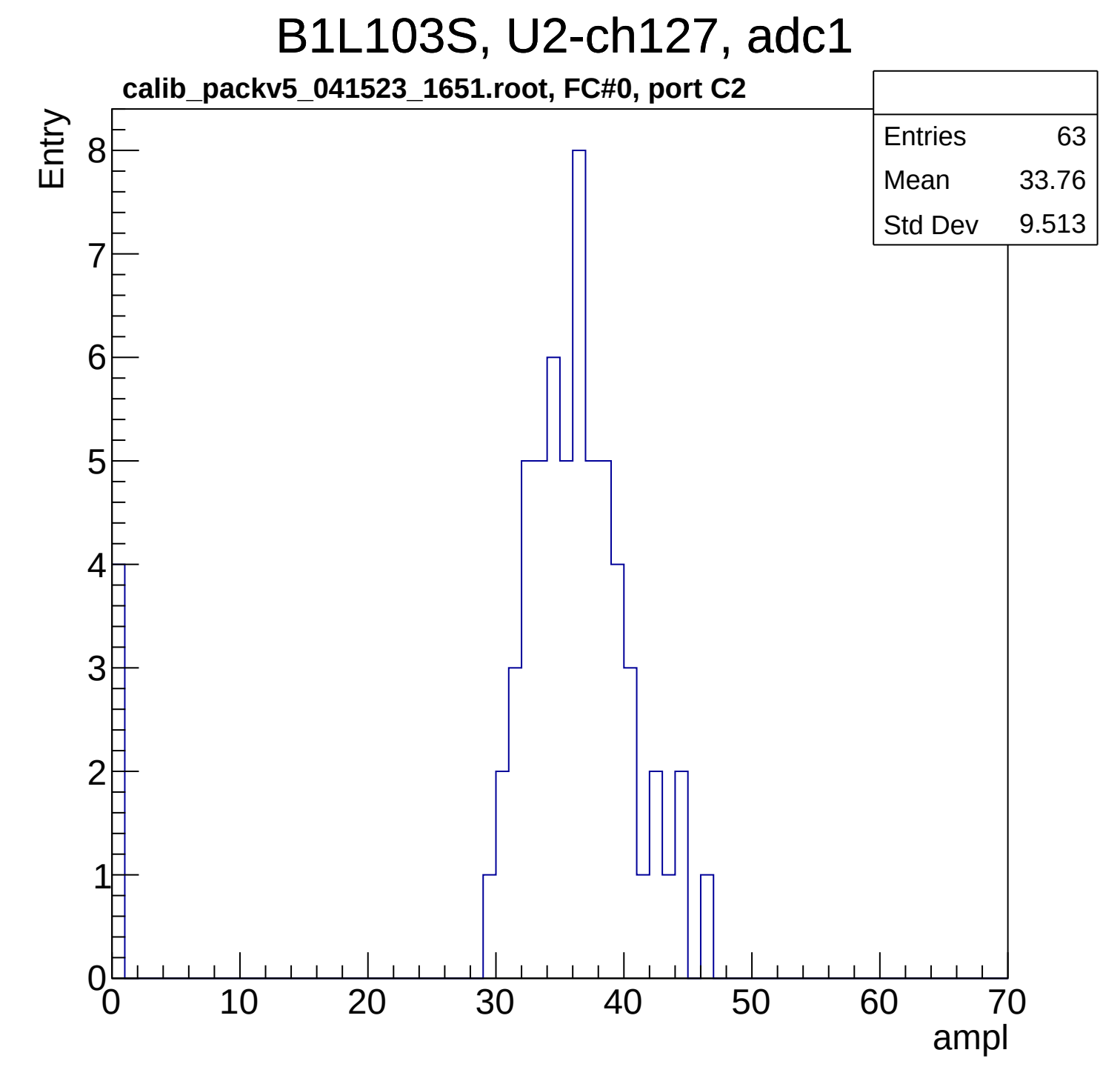

B1L103S, U2-ch126, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 49.62
Std Dev 8.607
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

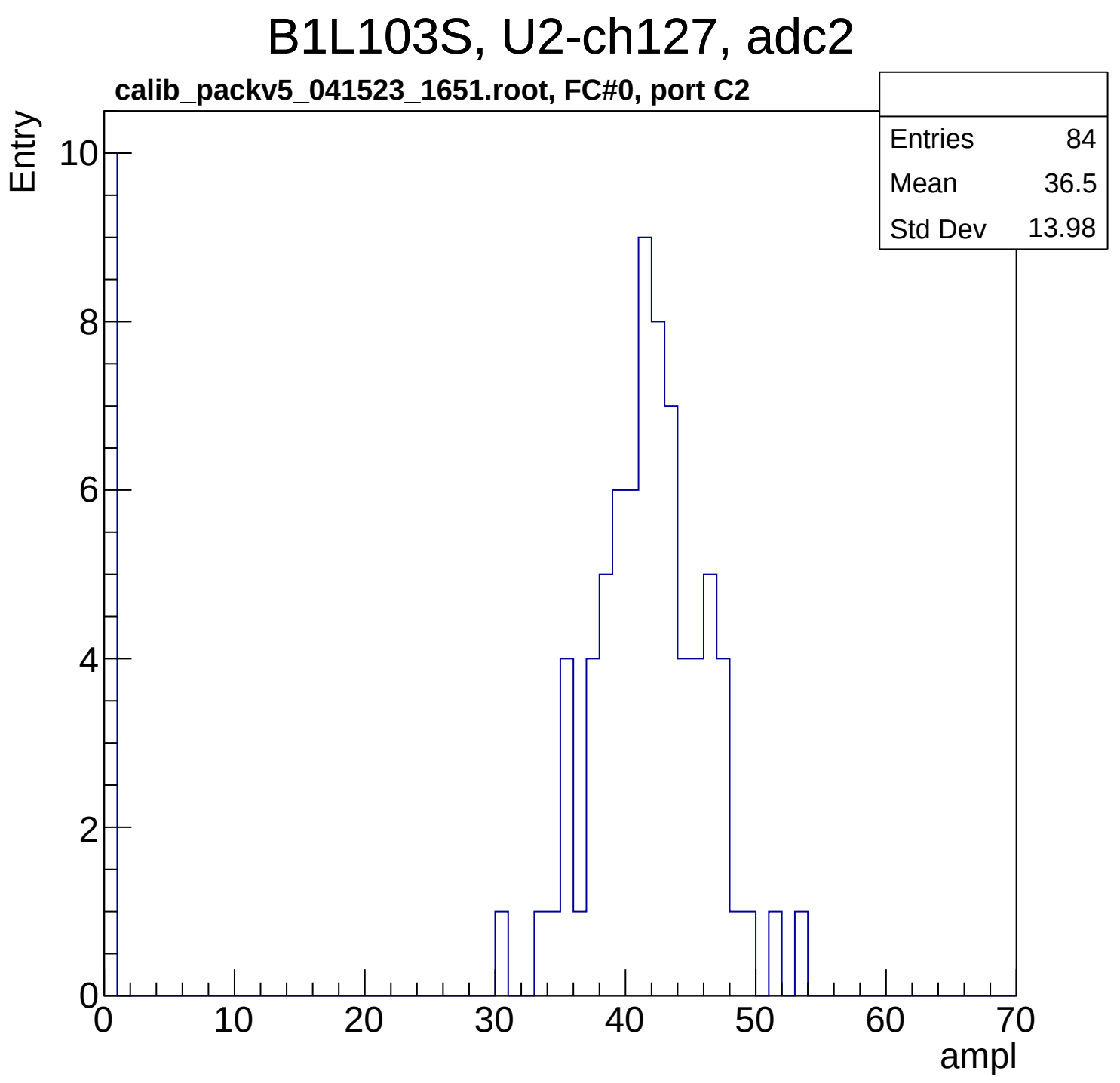

B1L103S, U2-ch126, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 56.58
Std Dev 3.377
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

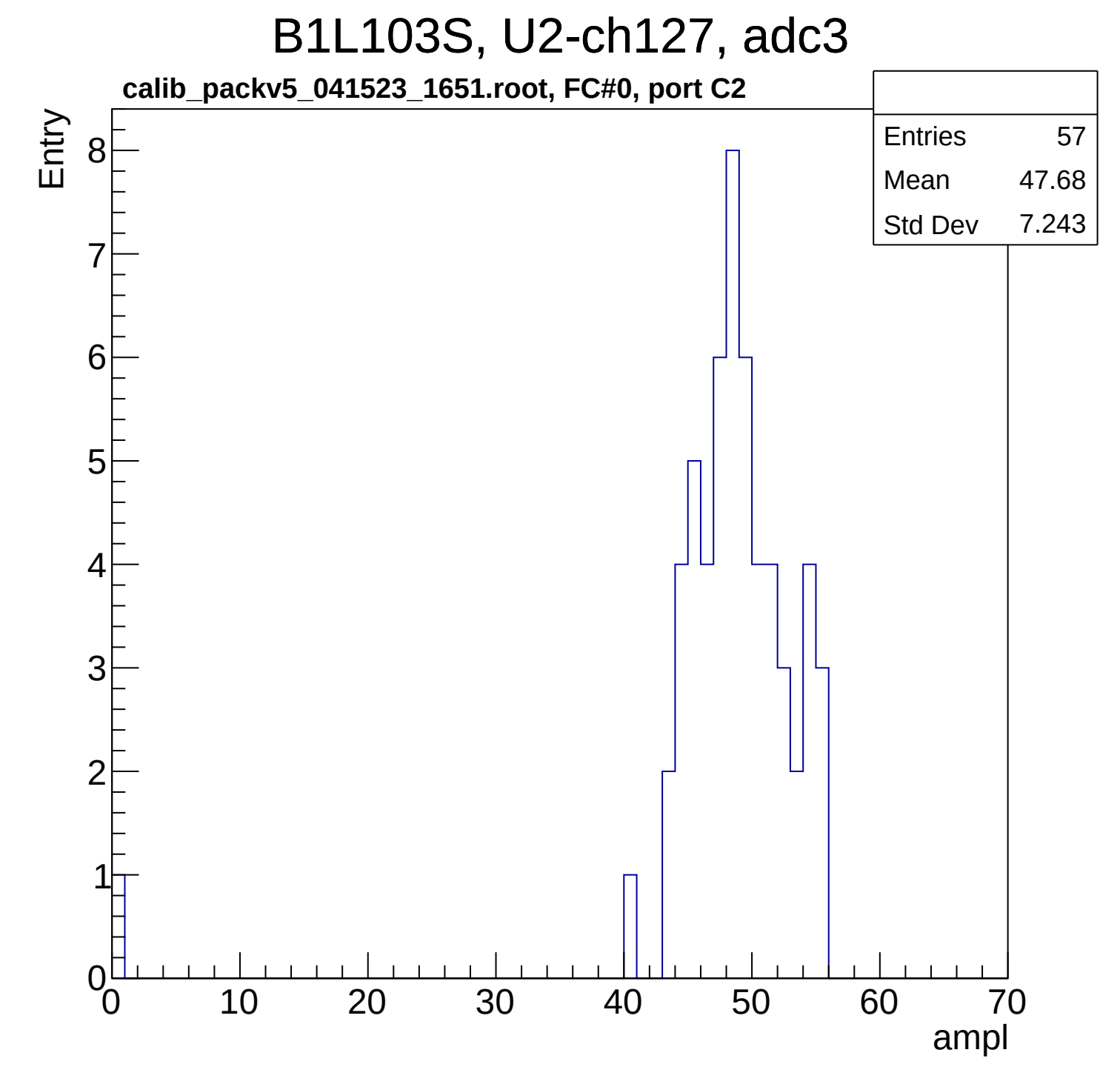

B1L103S, U2-ch126, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 58.78
Std Dev 11.69
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

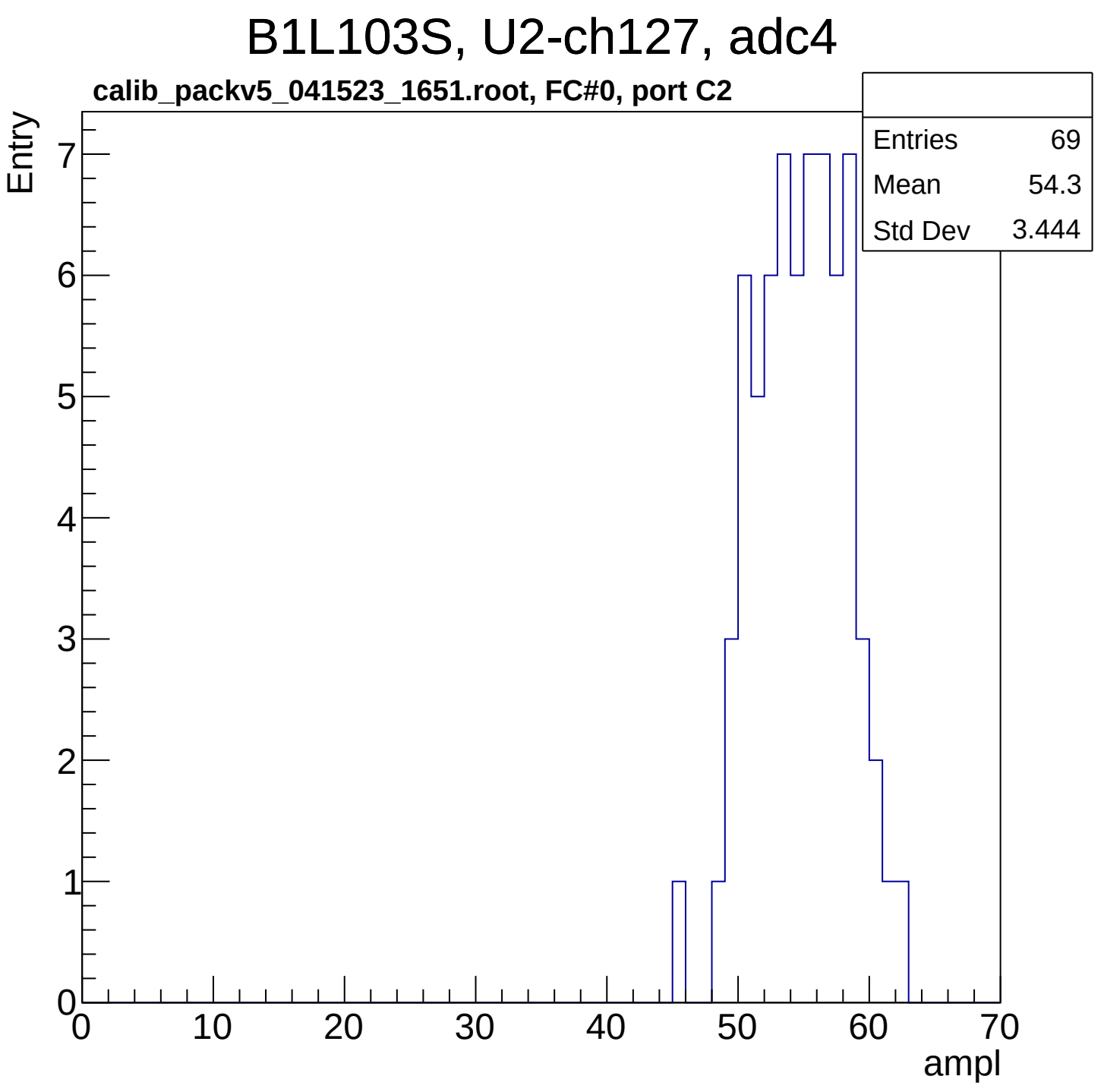

B1L103S, U2-ch126, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 8.455
Std Dev 21.28
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

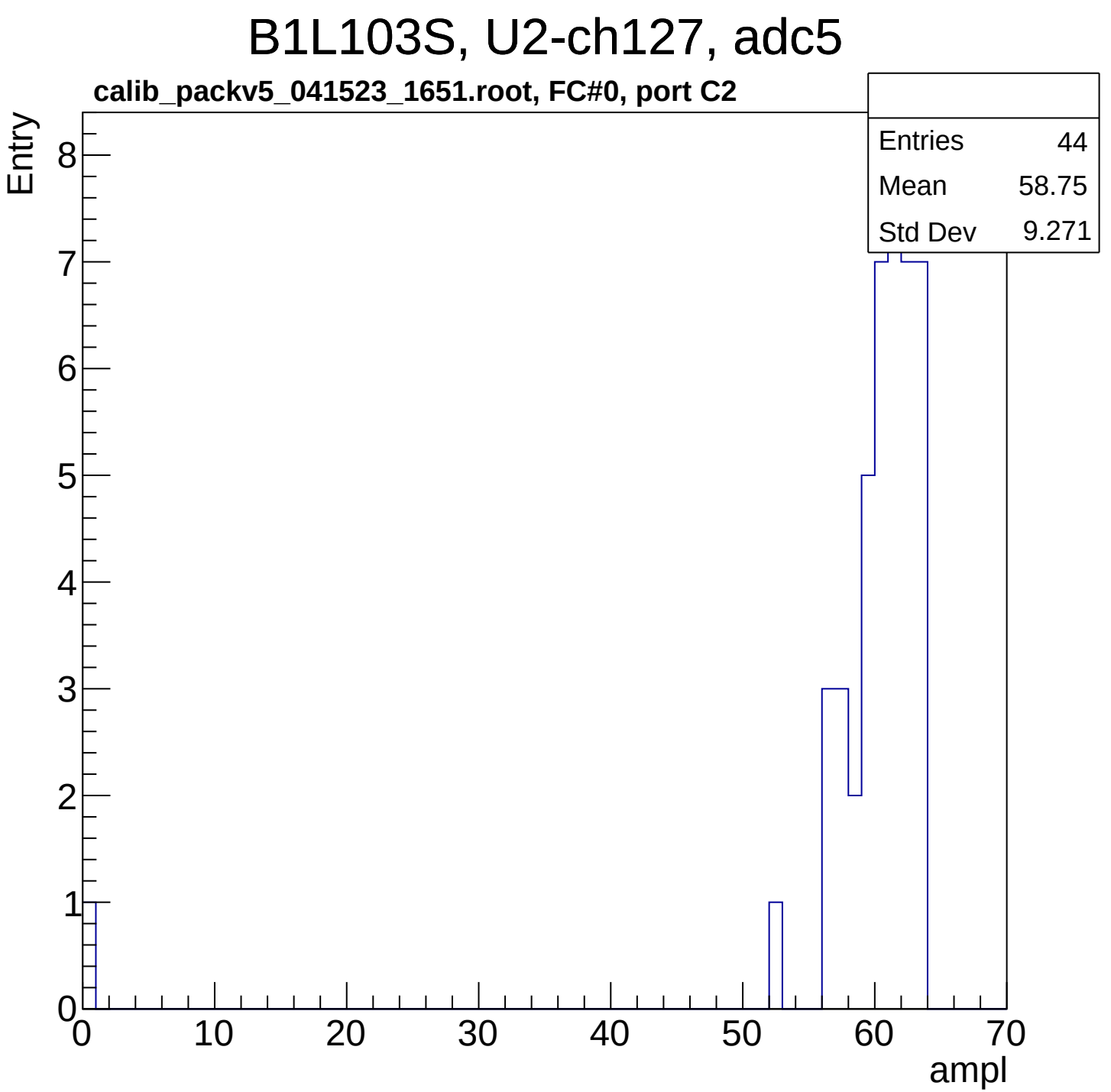

B1L103S, U2-ch127, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 23.14
Std Dev 11.5
Entry
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl

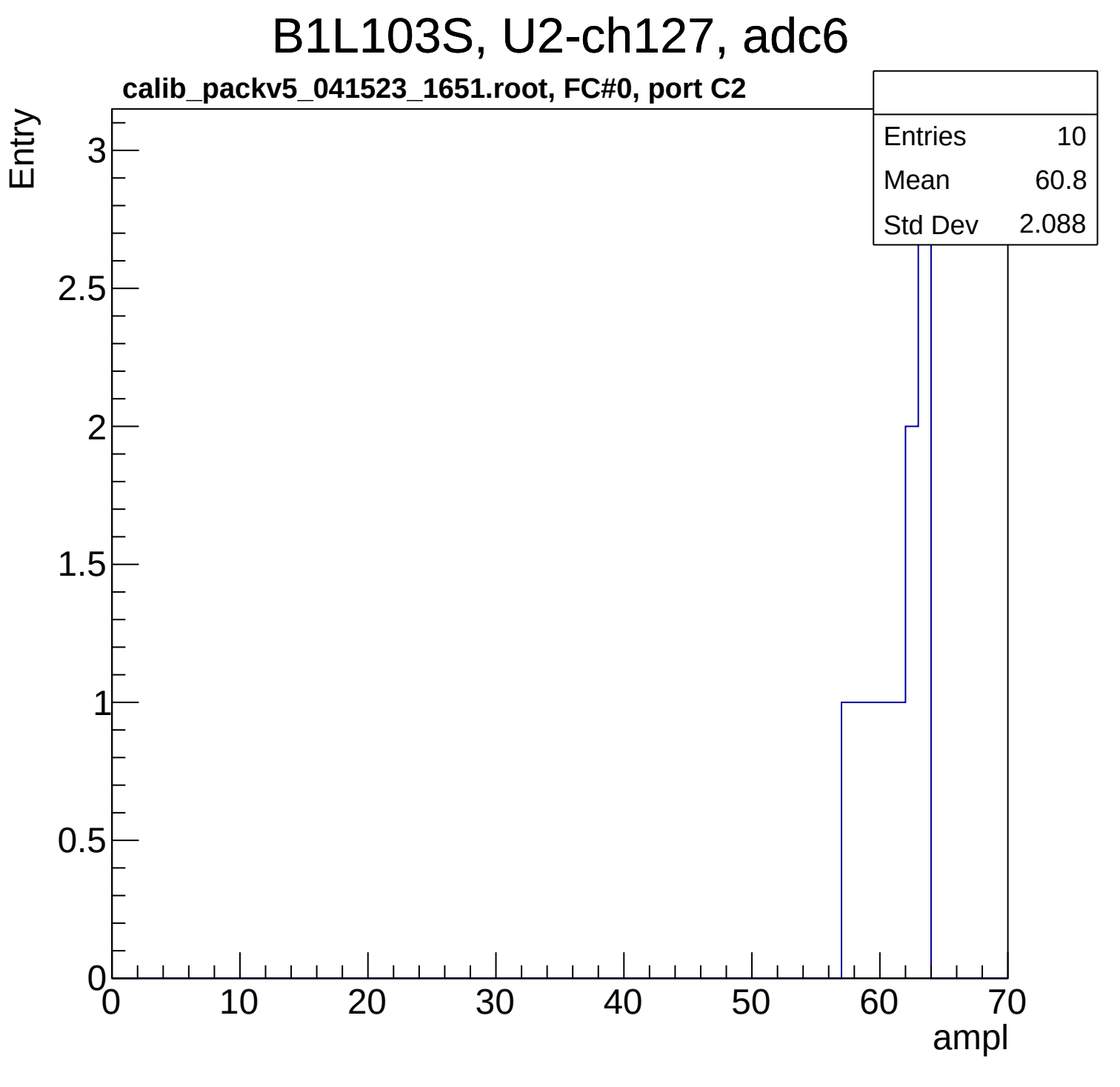

B1L103S, U2-ch127, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 33.76
Std Dev 9.513
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

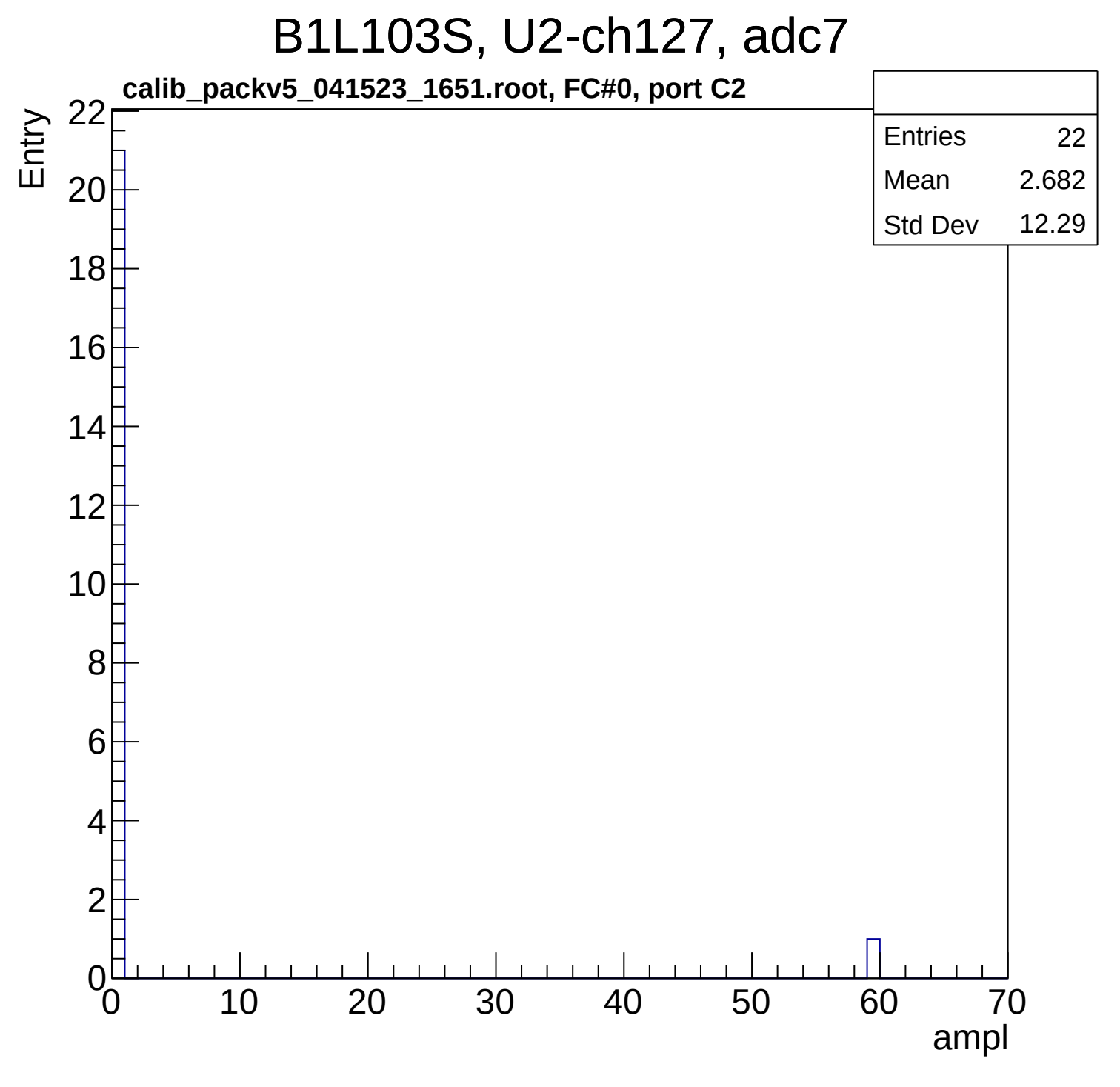

B1L103S, U2-ch127, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 36.5
Std Dev 13.98
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

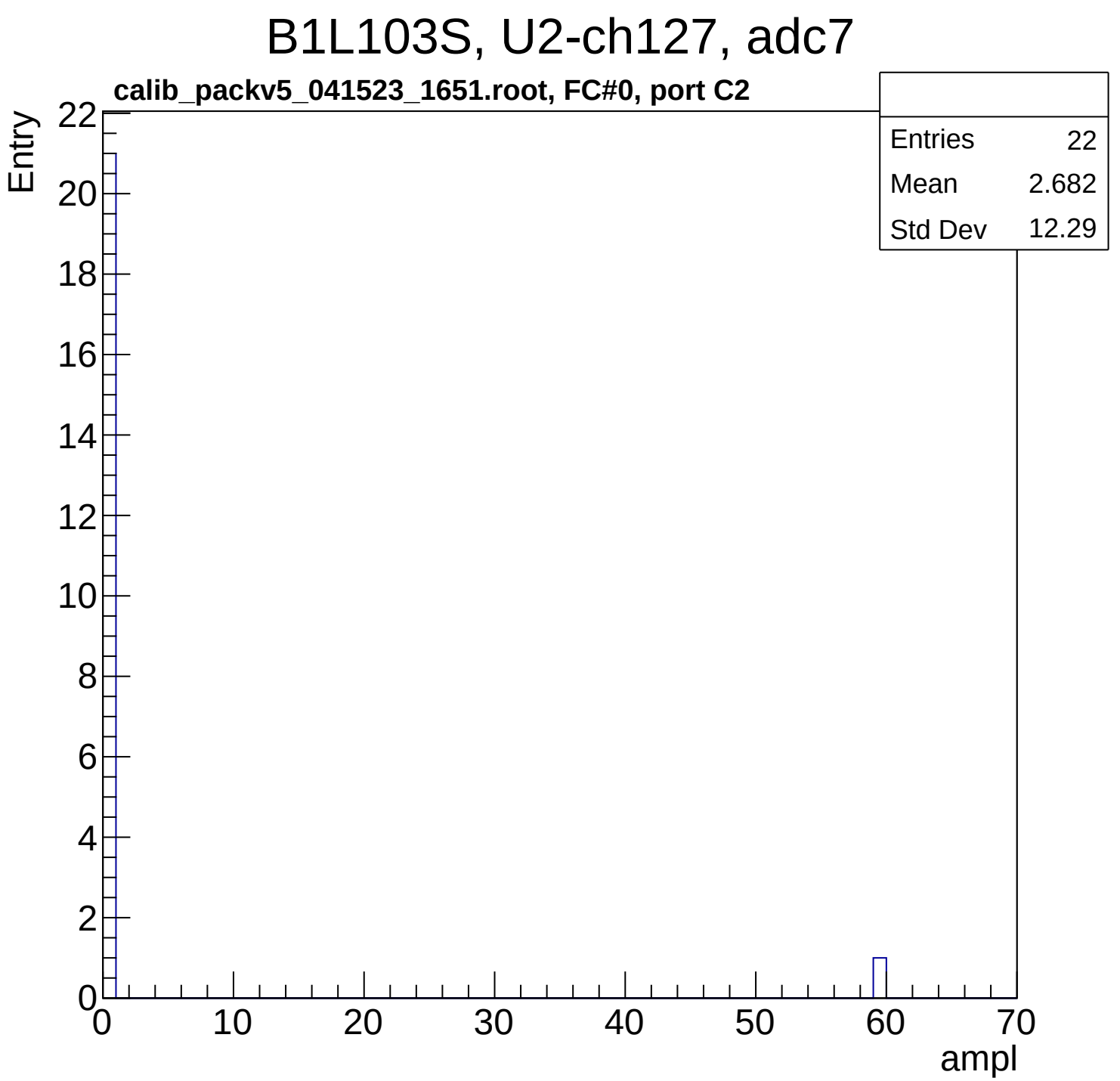

B1L103S, U2-ch127, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 47.68
Std Dev 7.243
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U2-ch127, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 54.3
Std Dev 3.444
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U2-ch127, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 58.75
Std Dev 9.271
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U2-ch127, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 60.8
Std Dev 2.088
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U2-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 2.682
Std Dev 12.29
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U2-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 2.682
Std Dev 12.29
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70