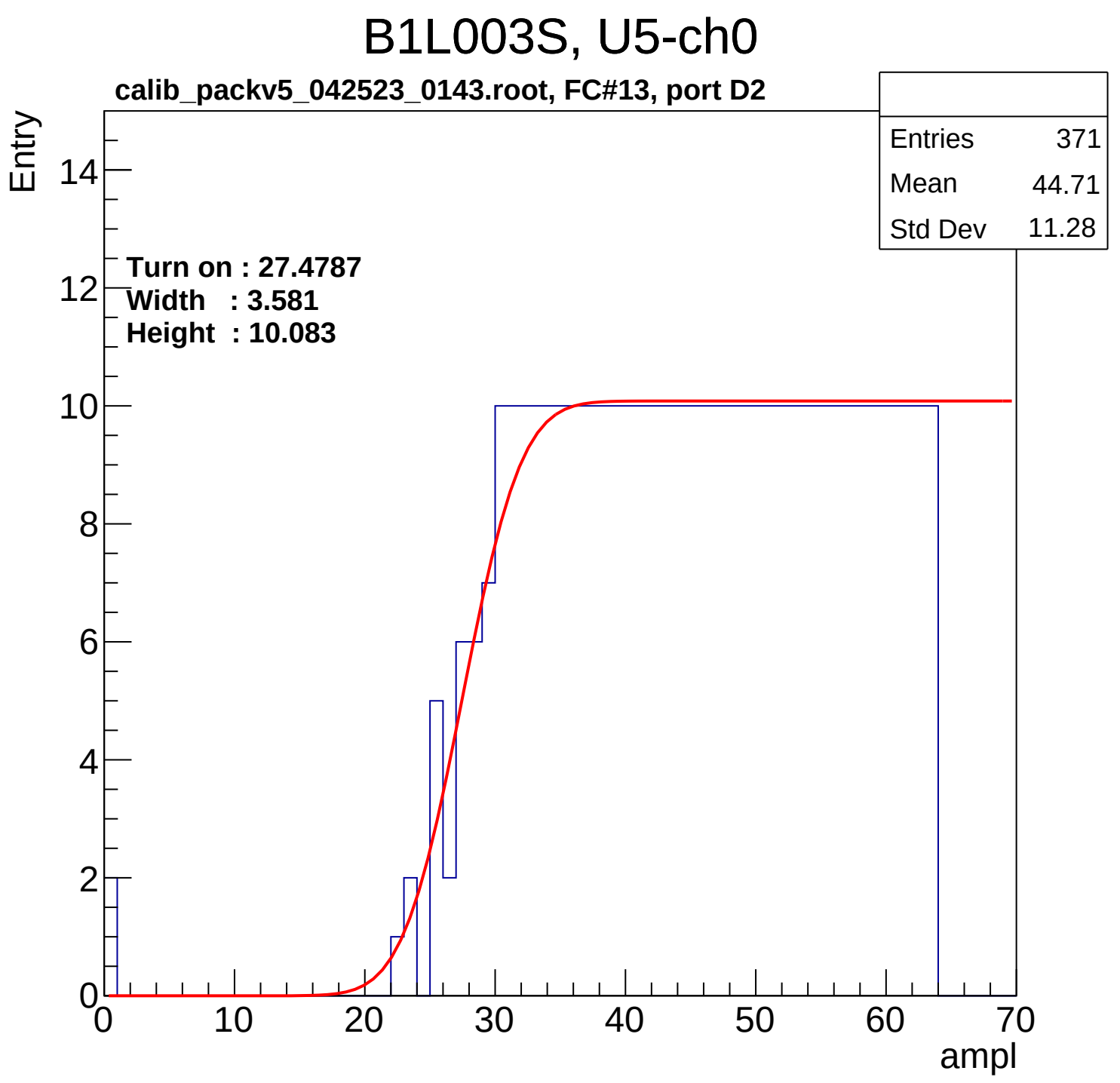
B1L003S, U5-ch0
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.71
Std Dev 11.28
Turn on : 27.4787
Width : 3.581
Height : 10.083
Entry
ampl
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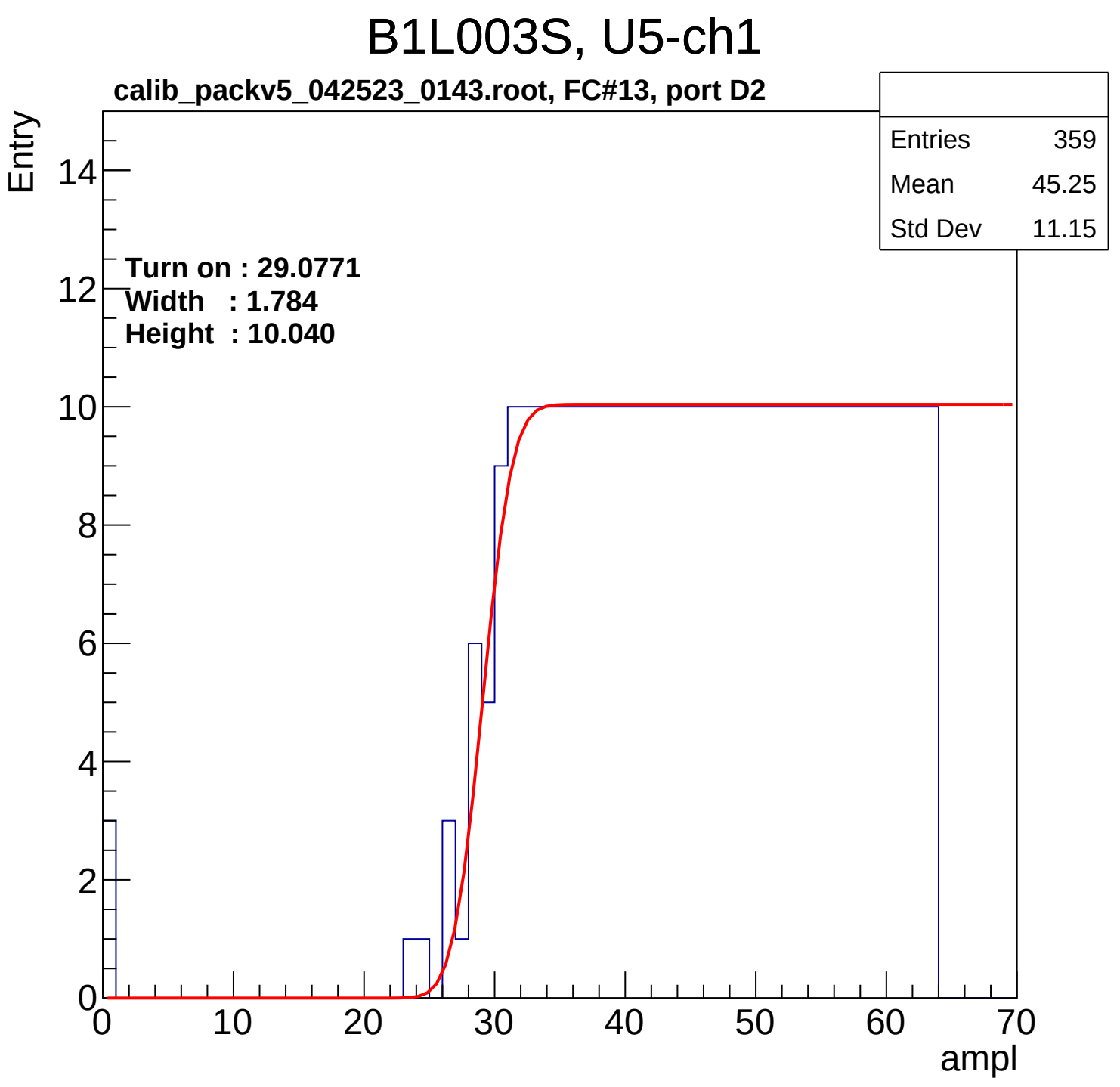
B1L003S, U5-ch1
calib_packv5_042523_0143.root, FC#13, port D2
Entries 359
Mean 45.25
Std Dev 11.15
Turn on : 29.0771
Width : 1.784
Height : 10.040
Entry
ampl
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2
4
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0
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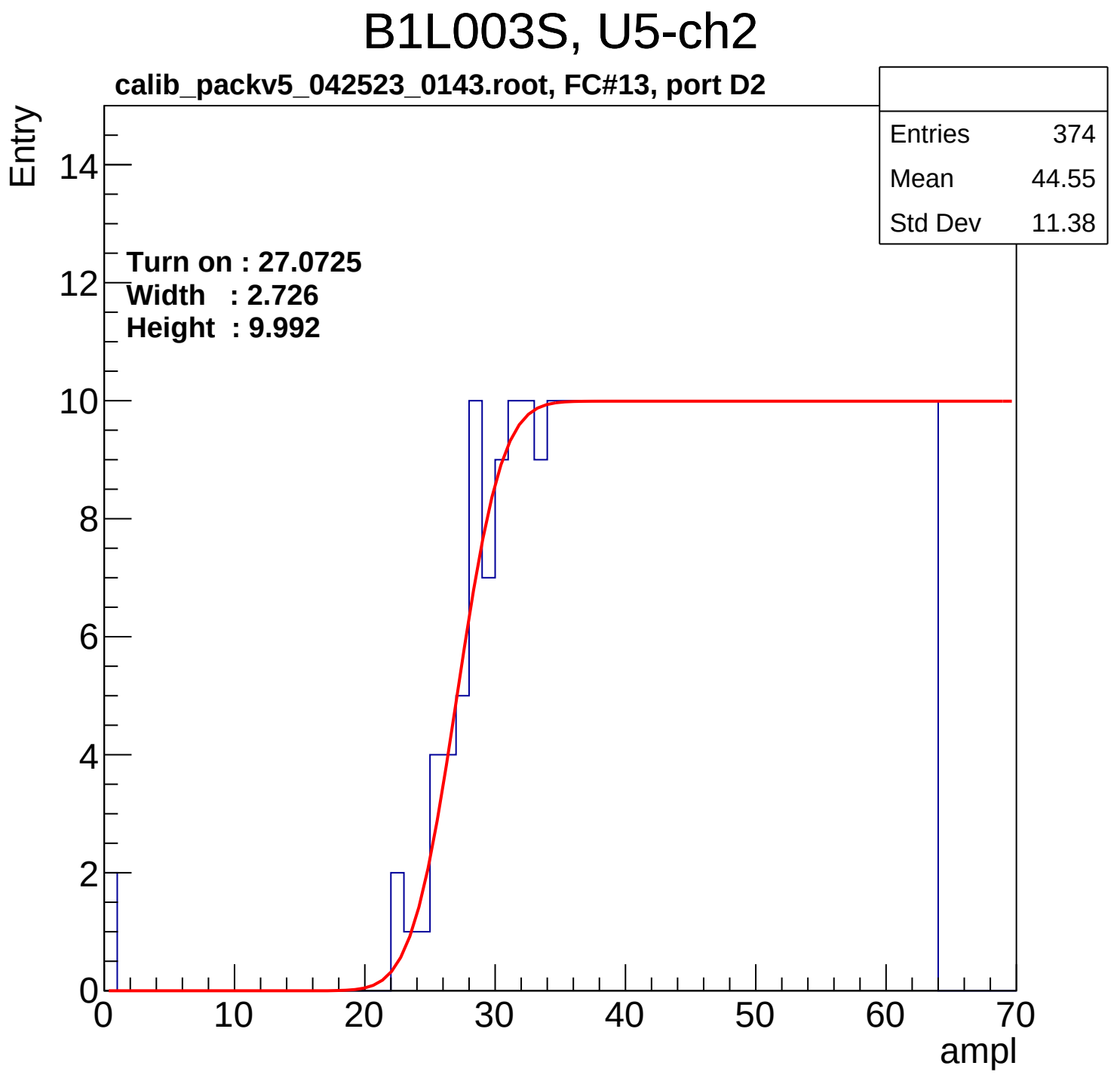
B1L003S, U5-ch2
calib_packv5_042523_0143.root, FC#13, port D2
Entries 374
Mean 44.55
Std Dev 11.38
Turn on : 27.0725
Width : 2.726
Height : 9.992
Entry
ampl
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2
4
6
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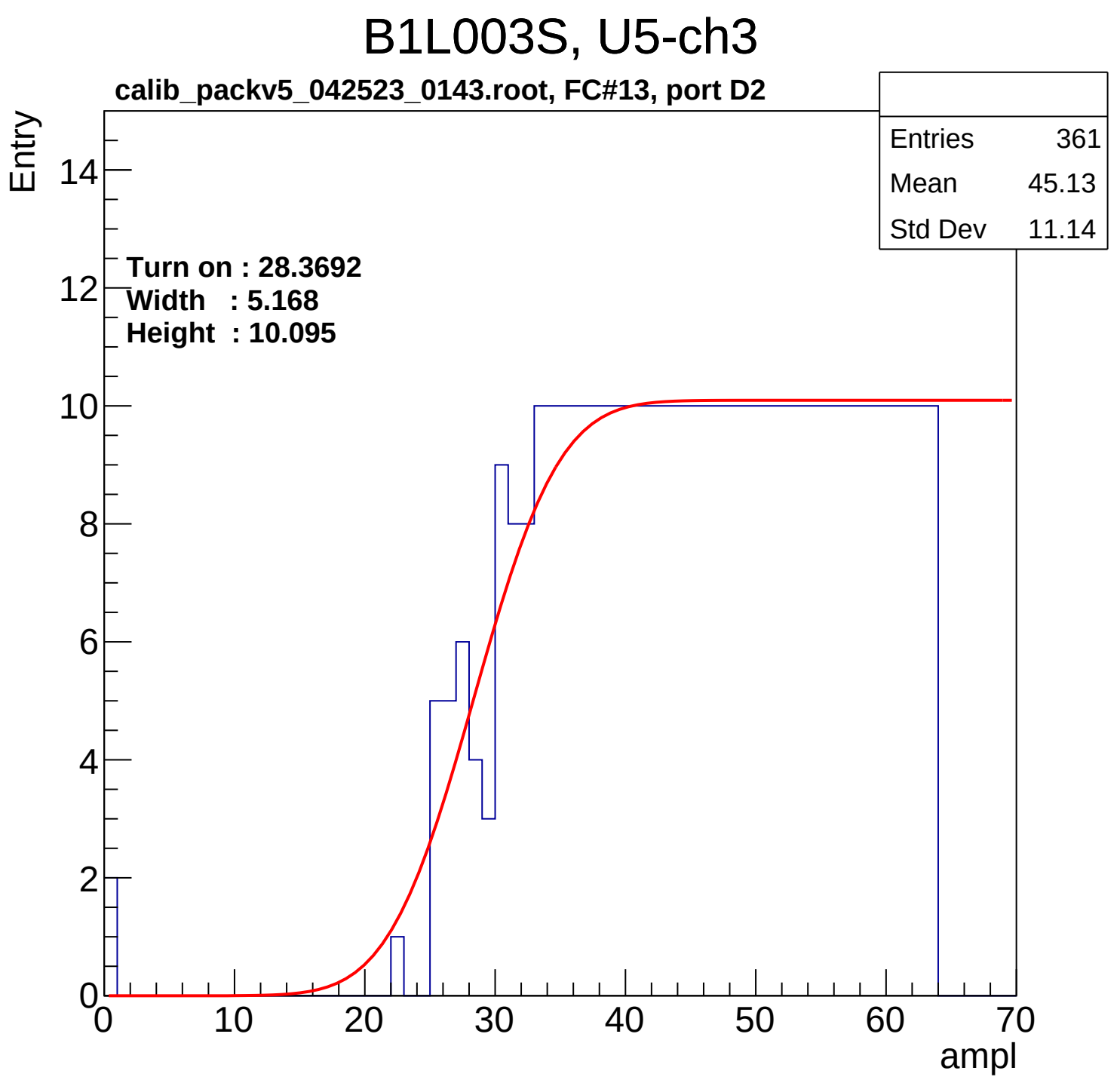
B1L003S, U5-ch3
calib_packv5_042523_0143.root, FC#13, port D2
Entries 361
Mean 45.13
Std Dev 11.14
Turn on : 28.3692
Width : 5.168
Height : 10.095
Entry
ampl
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2
4
6
8
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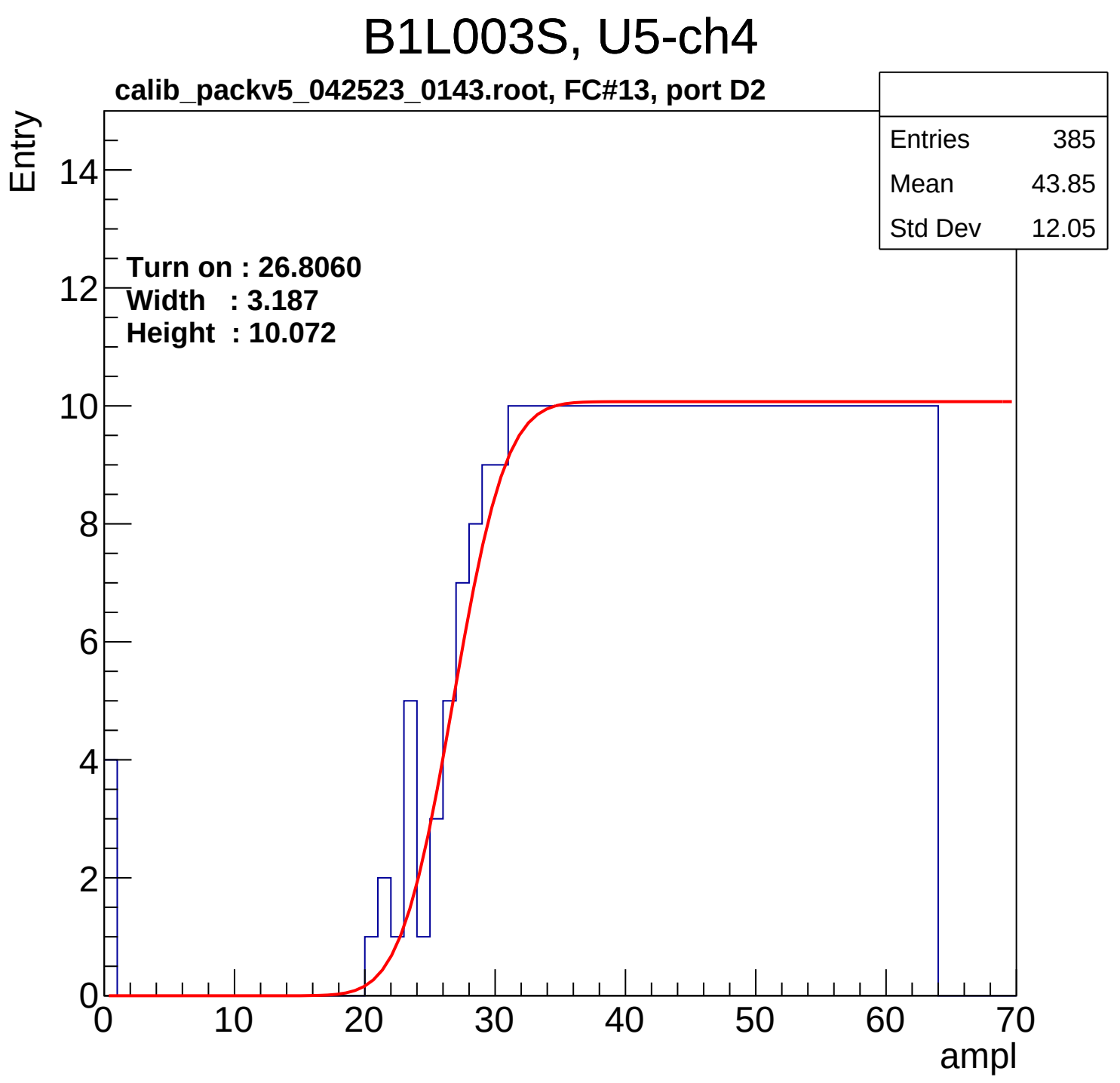
B1L003S, U5-ch4
calib_packv5_042523_0143.root, FC#13, port D2
Entries 385
Mean 43.85
Std Dev 12.05
Turn on : 26.8060
Width : 3.187
Height : 10.072
Entry
ampl
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4
6
8
10
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0
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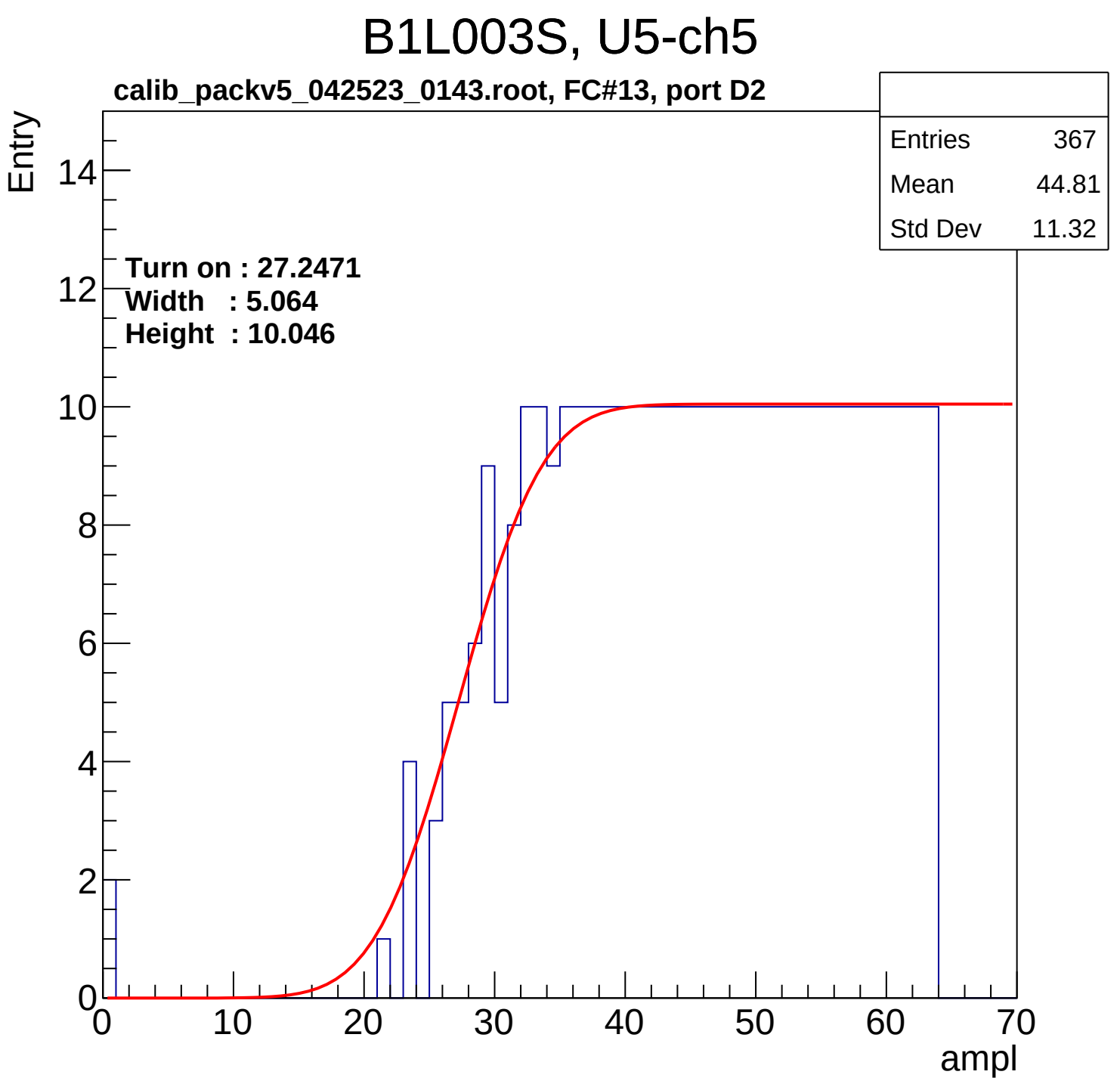
B1L003S, U5-ch5
calib_packv5_042523_0143.root, FC#13, port D2
Entries 367
Mean 44.81
Std Dev 11.32
Turn on : 27.2471
Width : 5.064
Height : 10.046
Entry
ampl
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2
4
6
8
10
12
14
0
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60
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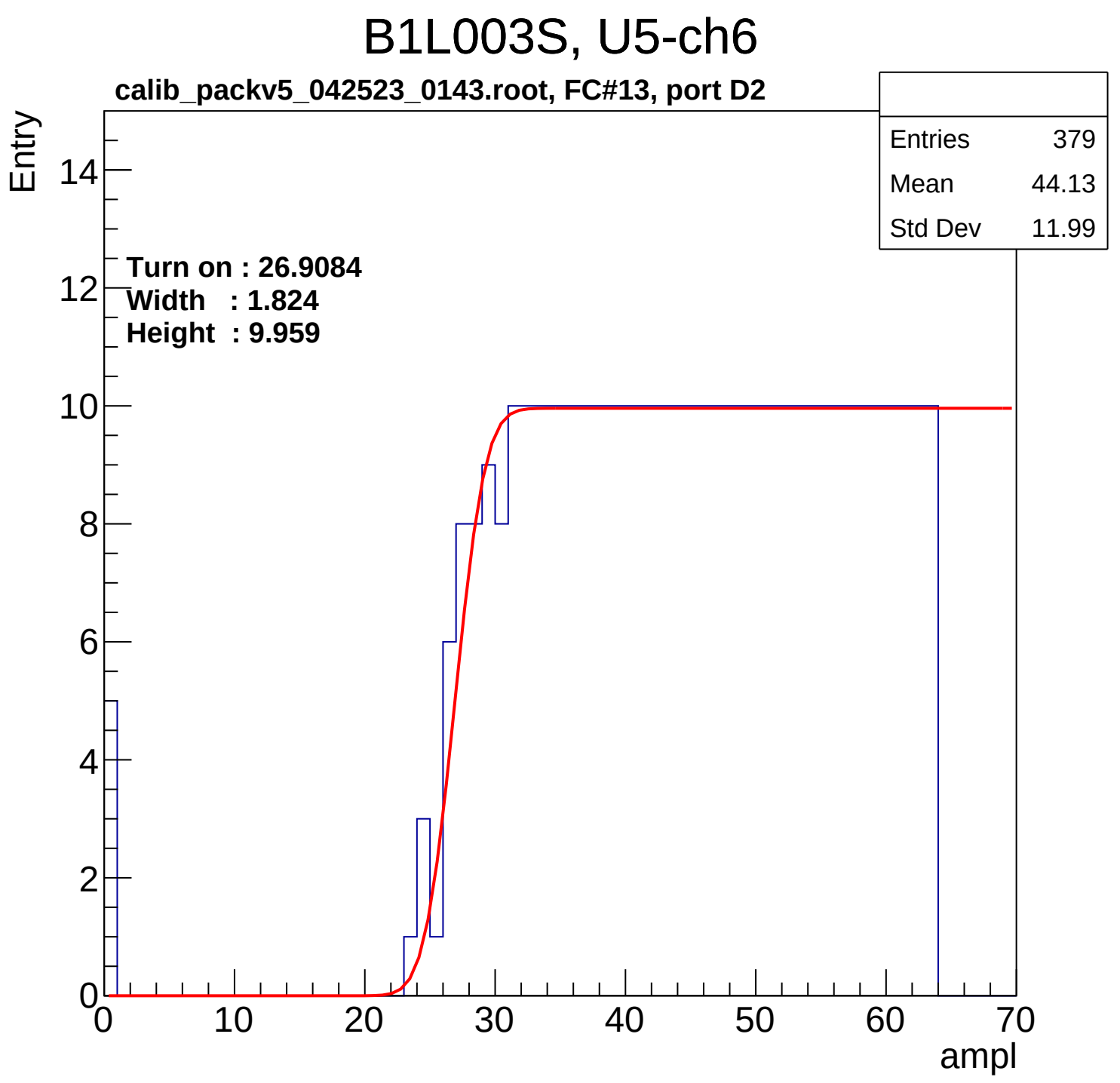
B1L003S, U5-ch6
calib_packv5_042523_0143.root, FC#13, port D2
Entries 379
Mean 44.13
Std Dev 11.99
Turn on : 26.9084
Width : 1.824
Height : 9.959
Entry
ampl
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2
4
6
8
10
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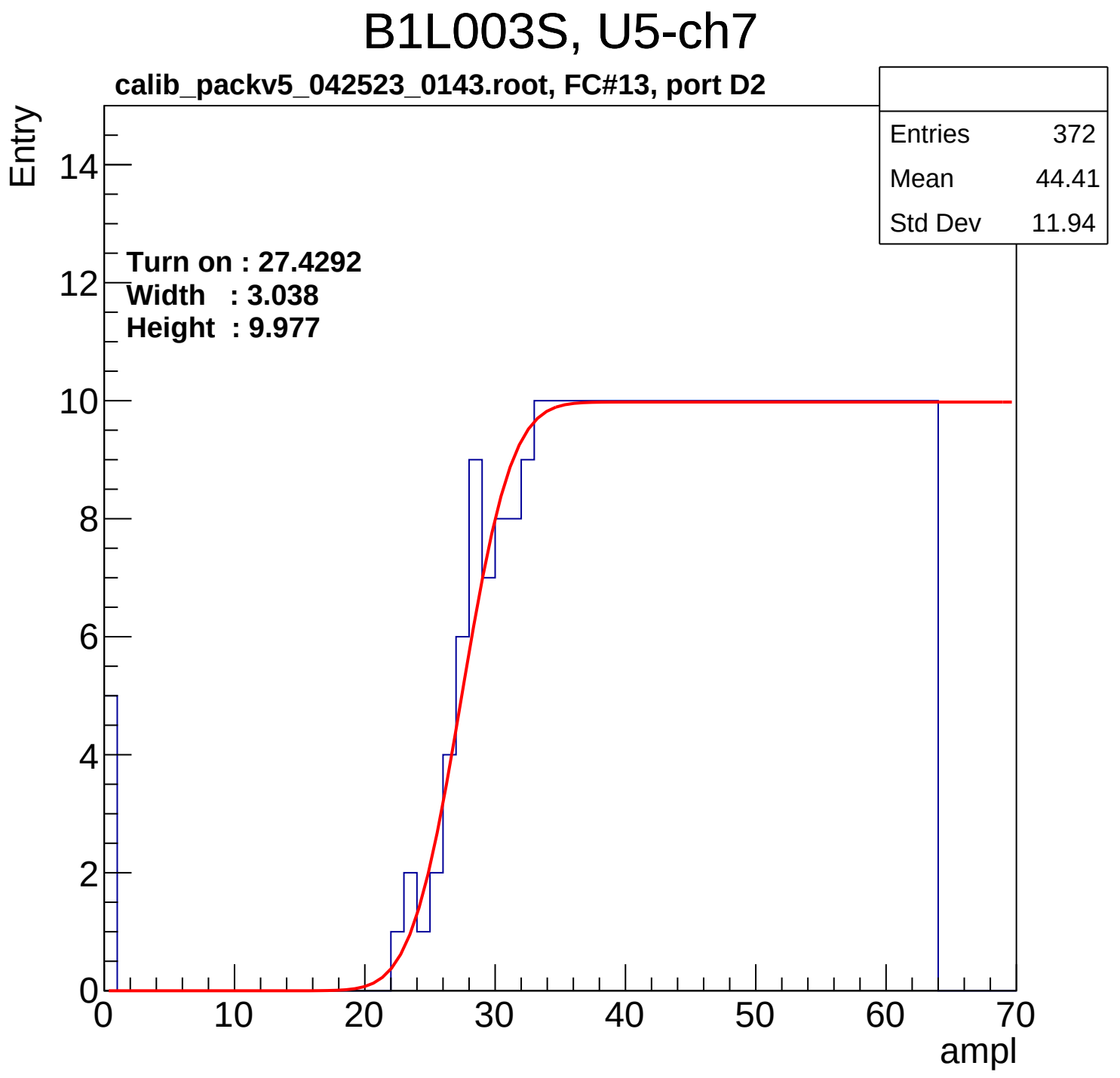
B1L003S, U5-ch7
calib_packv5_042523_0143.root, FC#13, port D2
Entries 372
Mean 44.41
Std Dev 11.94
Turn on : 27.4292
Width : 3.038
Height : 9.977
Entry
ampl
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2
4
6
8
10
12
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0
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60
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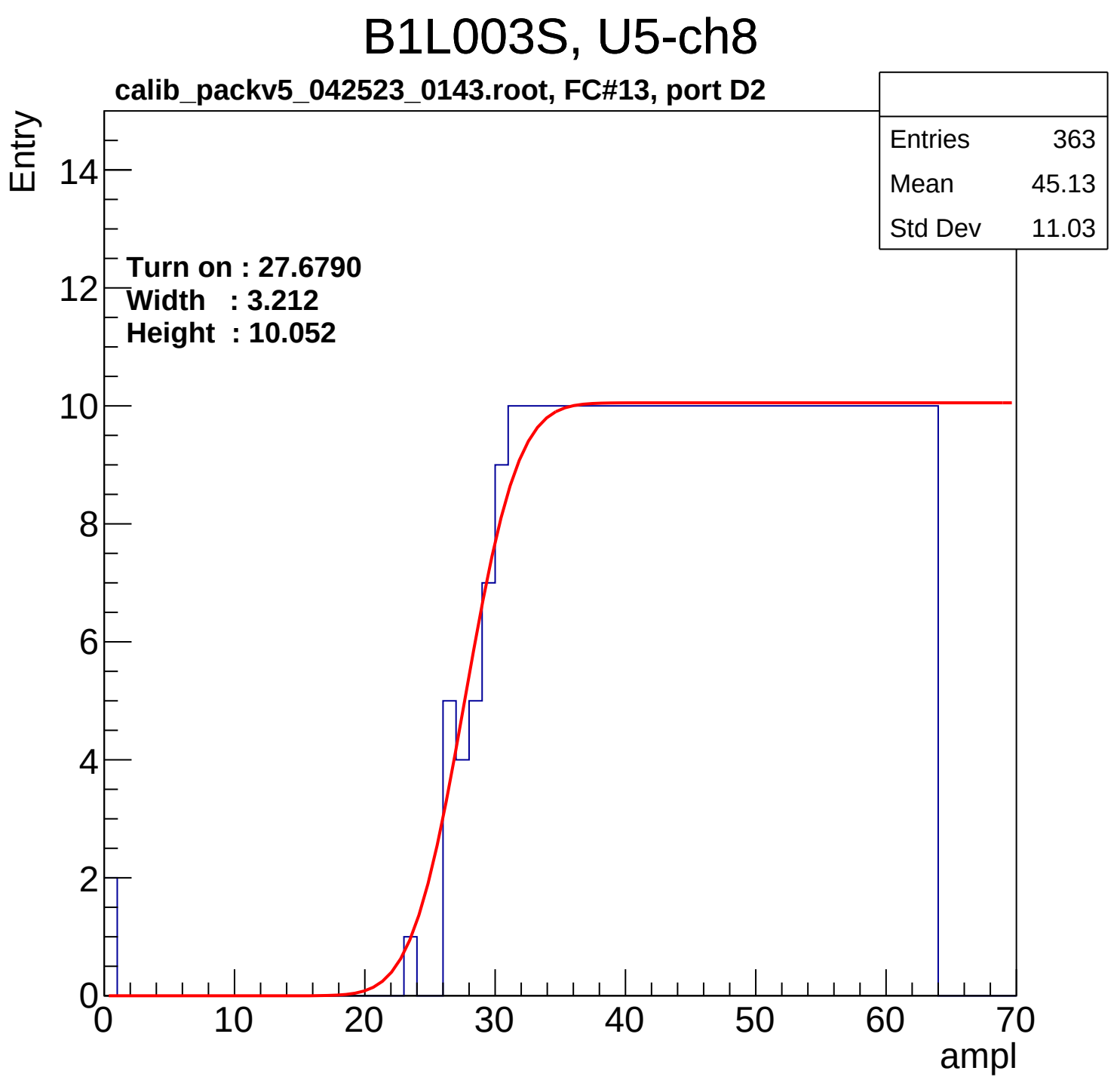
B1L003S, U5-ch8
calib_packv5_042523_0143.root, FC#13, port D2
Entries 363
Mean 45.13
Std Dev 11.03
Turn on : 27.6790
Width : 3.212
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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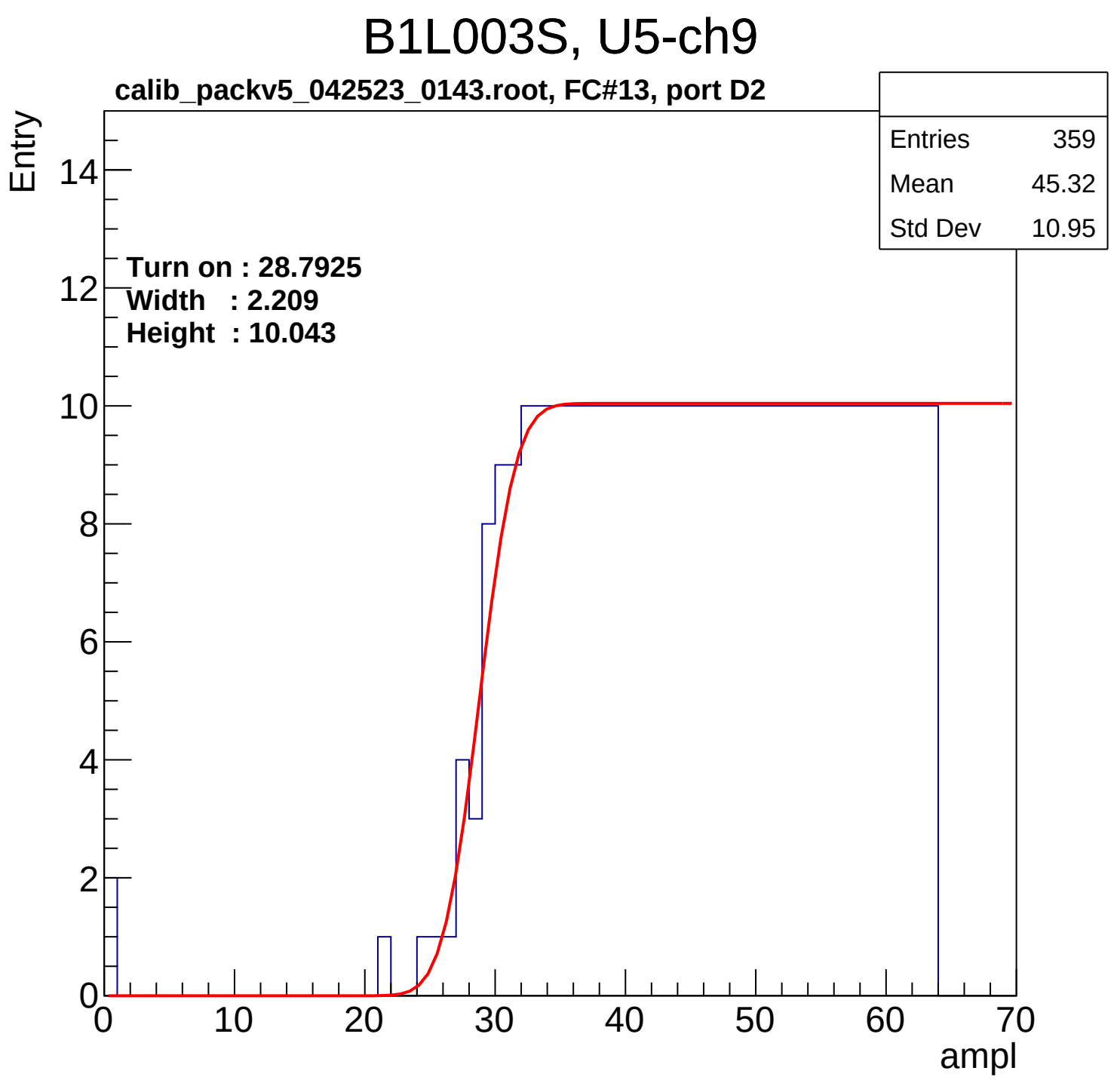
B1L003S, U5-ch9
calib_packv5_042523_0143.root, FC#13, port D2
Entries 359
Mean 45.32
Std Dev 10.95
Turn on : 28.7925
Width : 2.209
Height : 10.043
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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60
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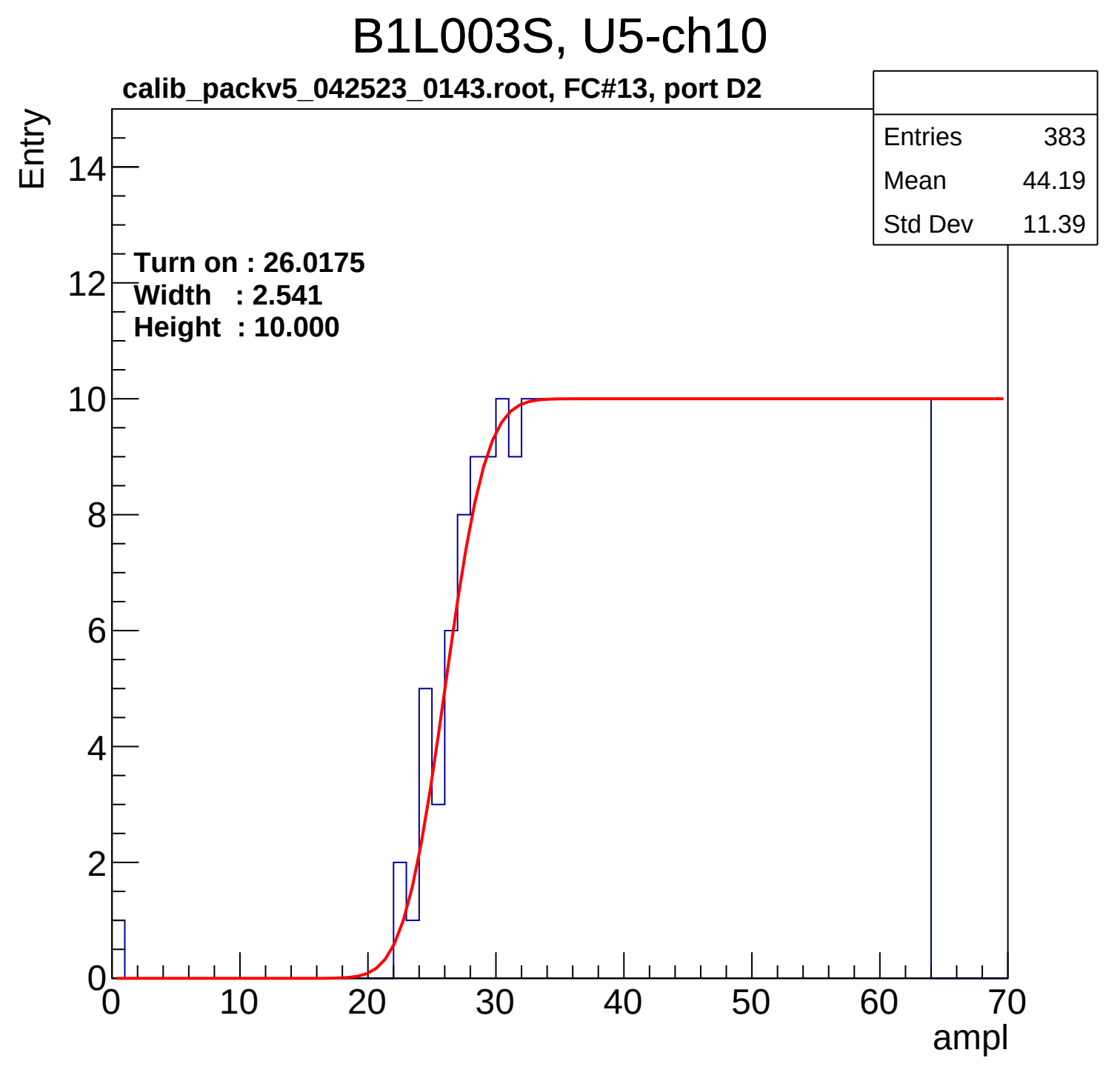
B1L003S, U5-ch10
calib_packv5_042523_0143.root, FC#13, port D2
Entries 383
Mean 44.19
Std Dev 11.39
Turn on : 26.0175
Width : 2.541
Height : 10.000
Entry
ampl
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2
4
6
8
10
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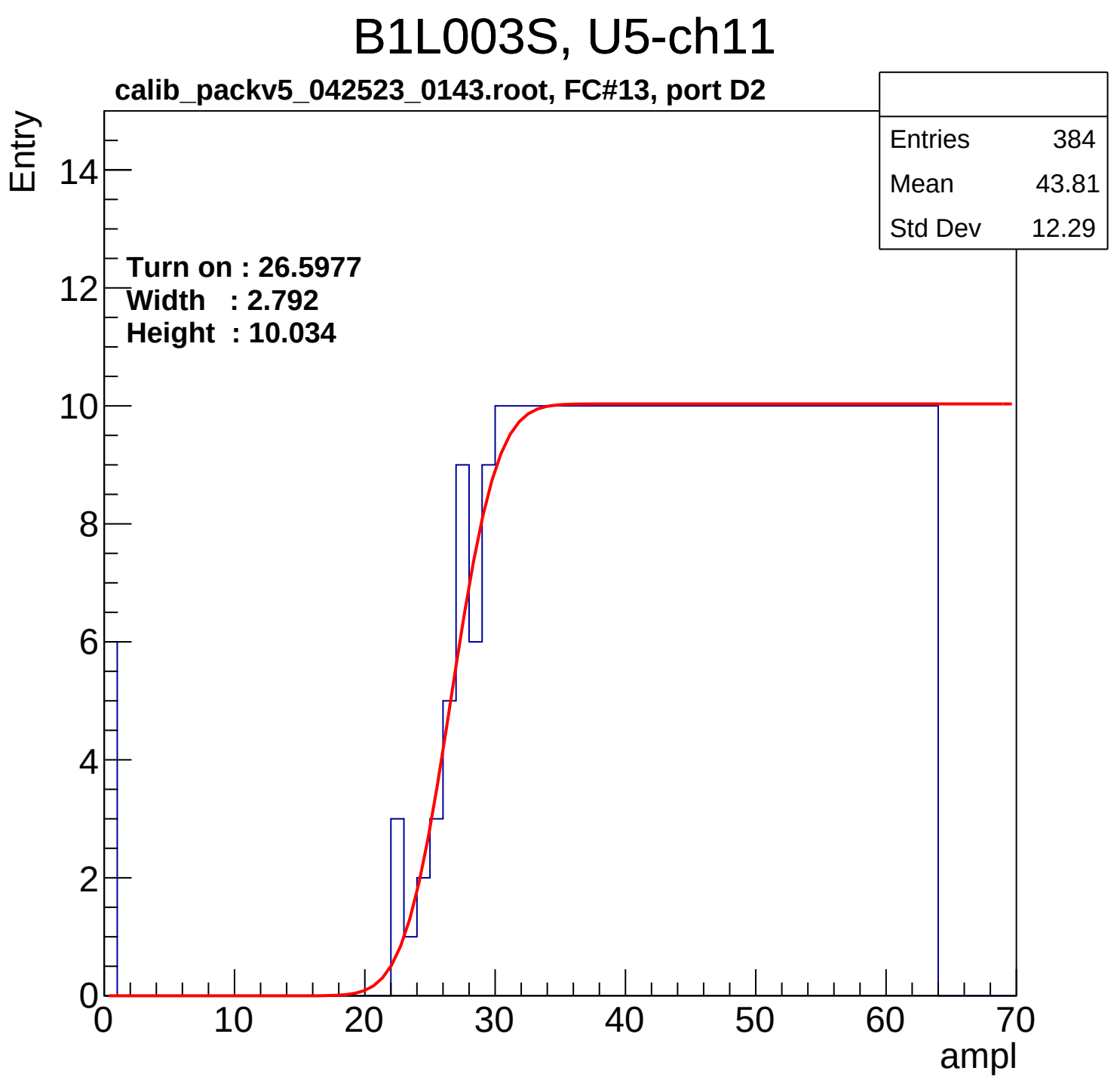
B1L003S, U5-ch11
calib_packv5_042523_0143.root, FC#13, port D2
Entries 384
Mean 43.81
Std Dev 12.29
Turn on : 26.5977
Width : 2.792
Height : 10.034
Entry
ampl
0
2
4
6
8
10
12
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60
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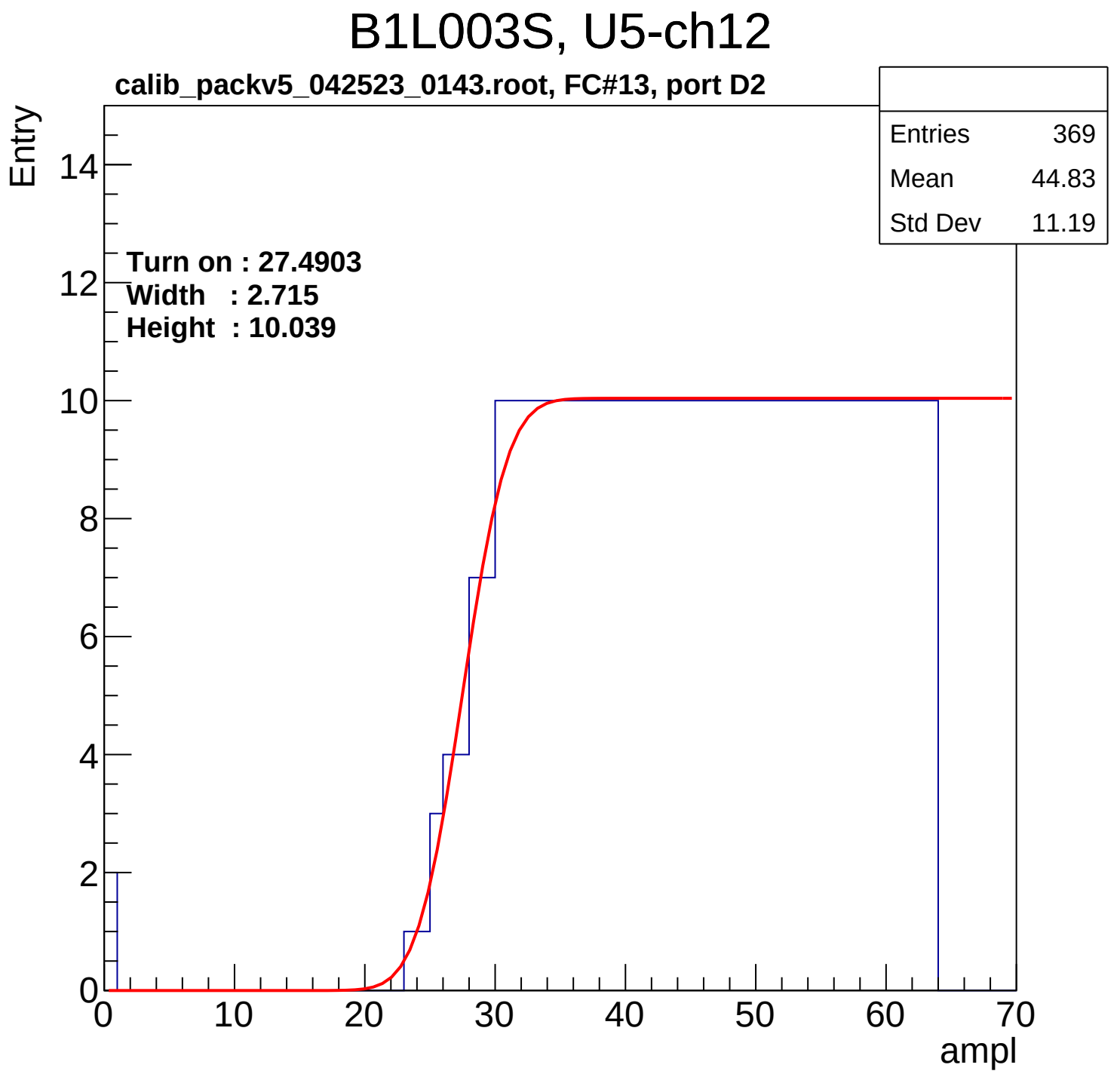
B1L003S, U5-ch12
calib_packv5_042523_0143.root, FC#13, port D2
Entries 369
Mean 44.83
Std Dev 11.19
Turn on : 27.4903
Width : 2.715
Height : 10.039
Entry
ampl
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2
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6
8
10
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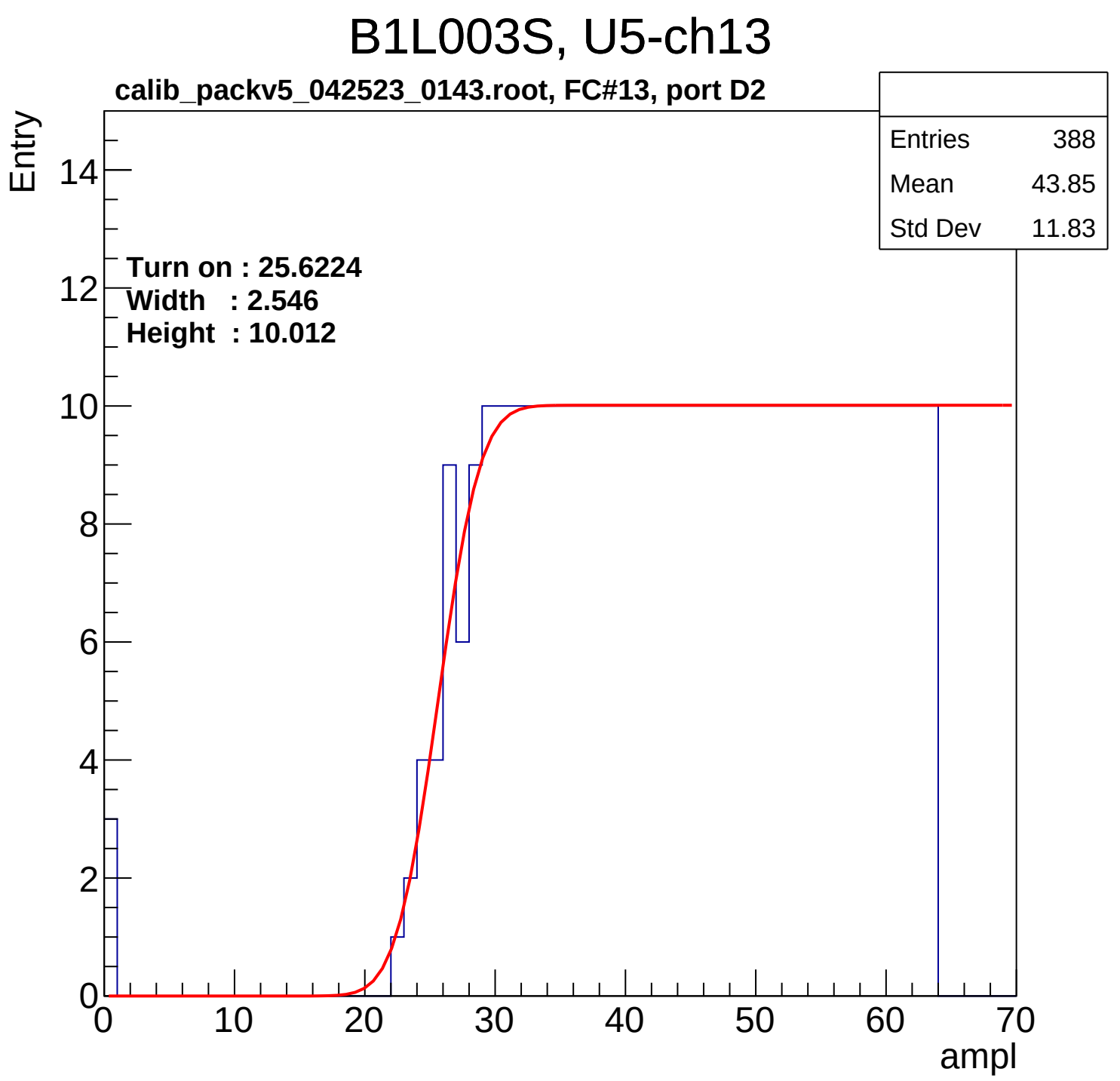
B1L003S, U5-ch13
calib_packv5_042523_0143.root, FC#13, port D2
Entries 388
Mean 43.85
Std Dev 11.83
Turn on : 25.6224
Width : 2.546
Height : 10.012
Entry
ampl
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2
4
6
8
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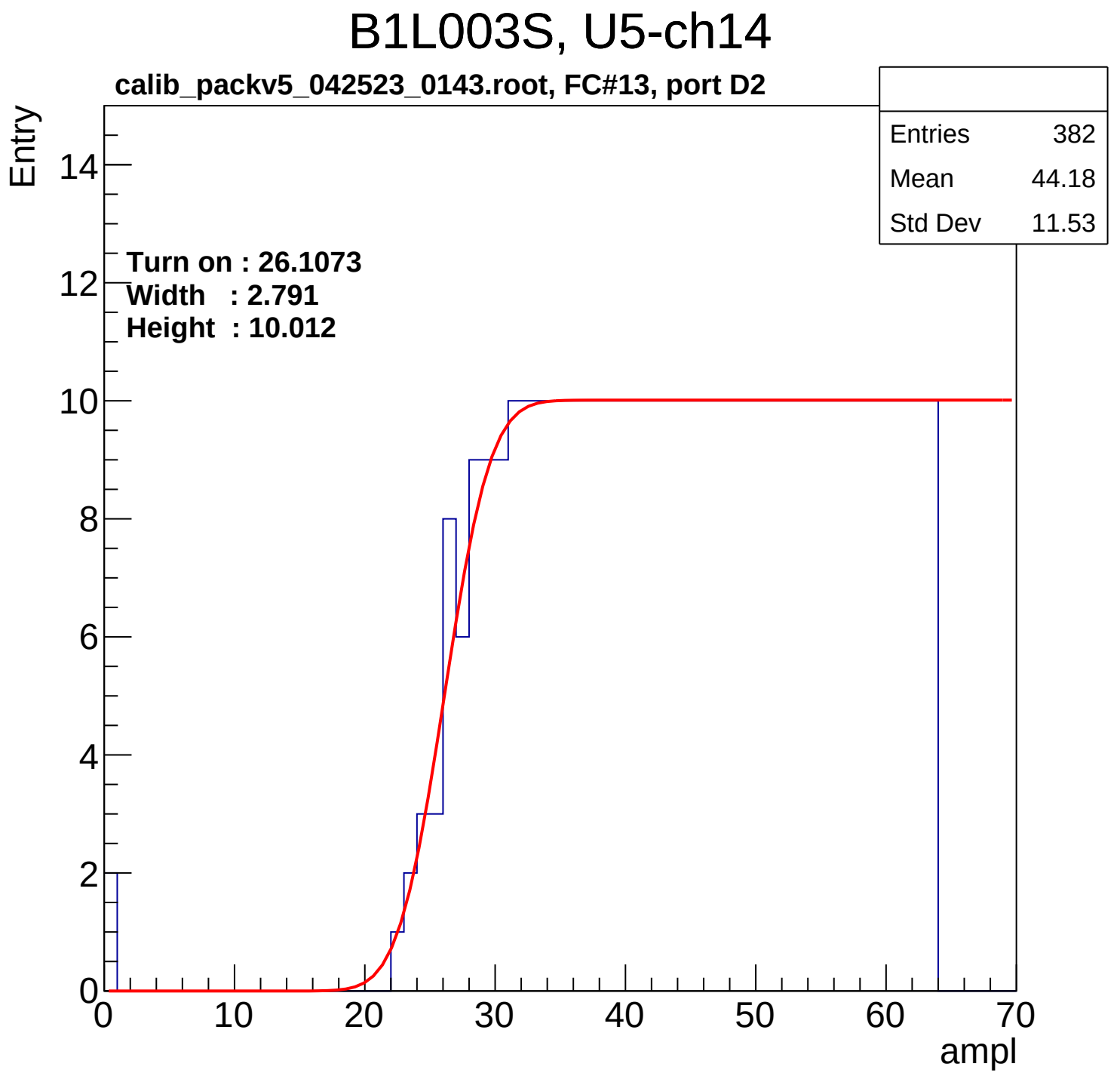
B1L003S, U5-ch14
calib_packv5_042523_0143.root, FC#13, port D2
Entries 382
Mean 44.18
Std Dev 11.53
Turn on : 26.1073
Width : 2.791
Height : 10.012
Entry
ampl
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8
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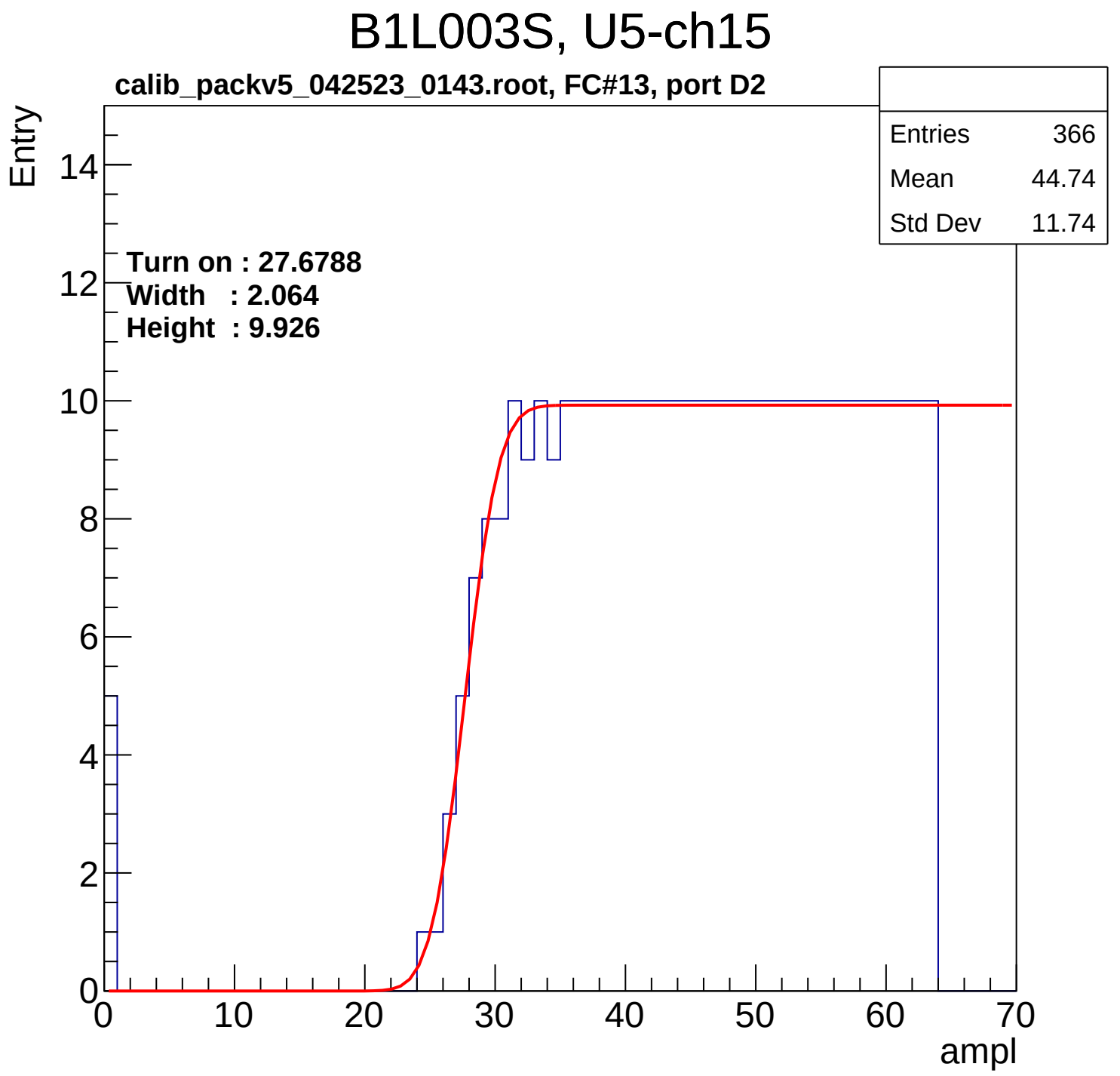
B1L003S, U5-ch15
calib_packv5_042523_0143.root, FC#13, port D2
Entries 366
Mean 44.74
Std Dev 11.74
Turn on : 27.6788
Width : 2.064
Height : 9.926
Entry
ampl
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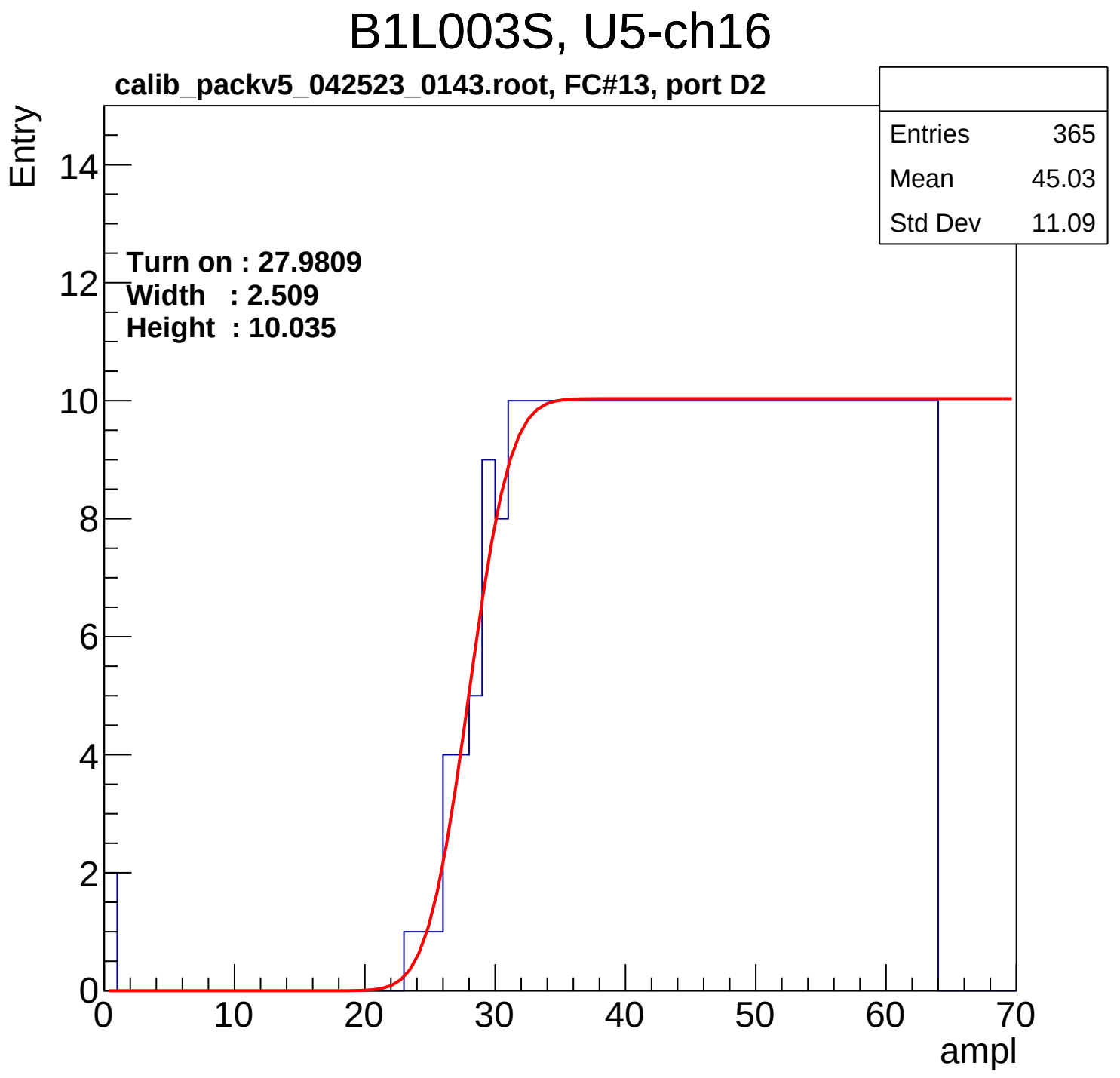
B1L003S, U5-ch16
calib_packv5_042523_0143.root, FC#13, port D2
Entries 365
Mean 45.03
Std Dev 11.09
Turn on : 27.9809
Width : 2.509
Height : 10.035
Entry
ampl
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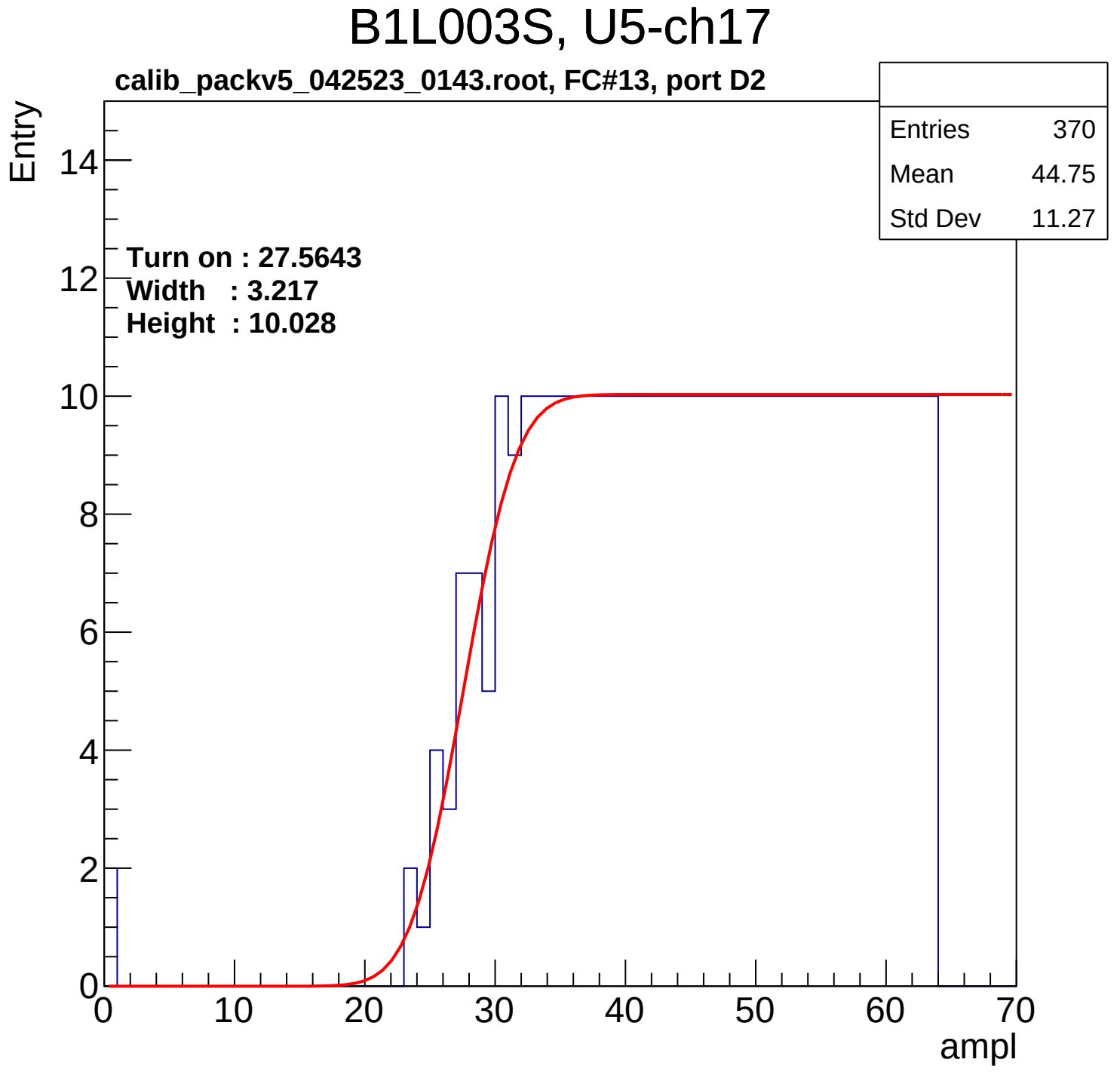
B1L003S, U5-ch17
calib_packv5_042523_0143.root, FC#13, port D2
Entries 370
Mean 44.75
Std Dev 11.27
Turn on : 27.5643
Width : 3.217
Height : 10.028
Entry
ampl
0
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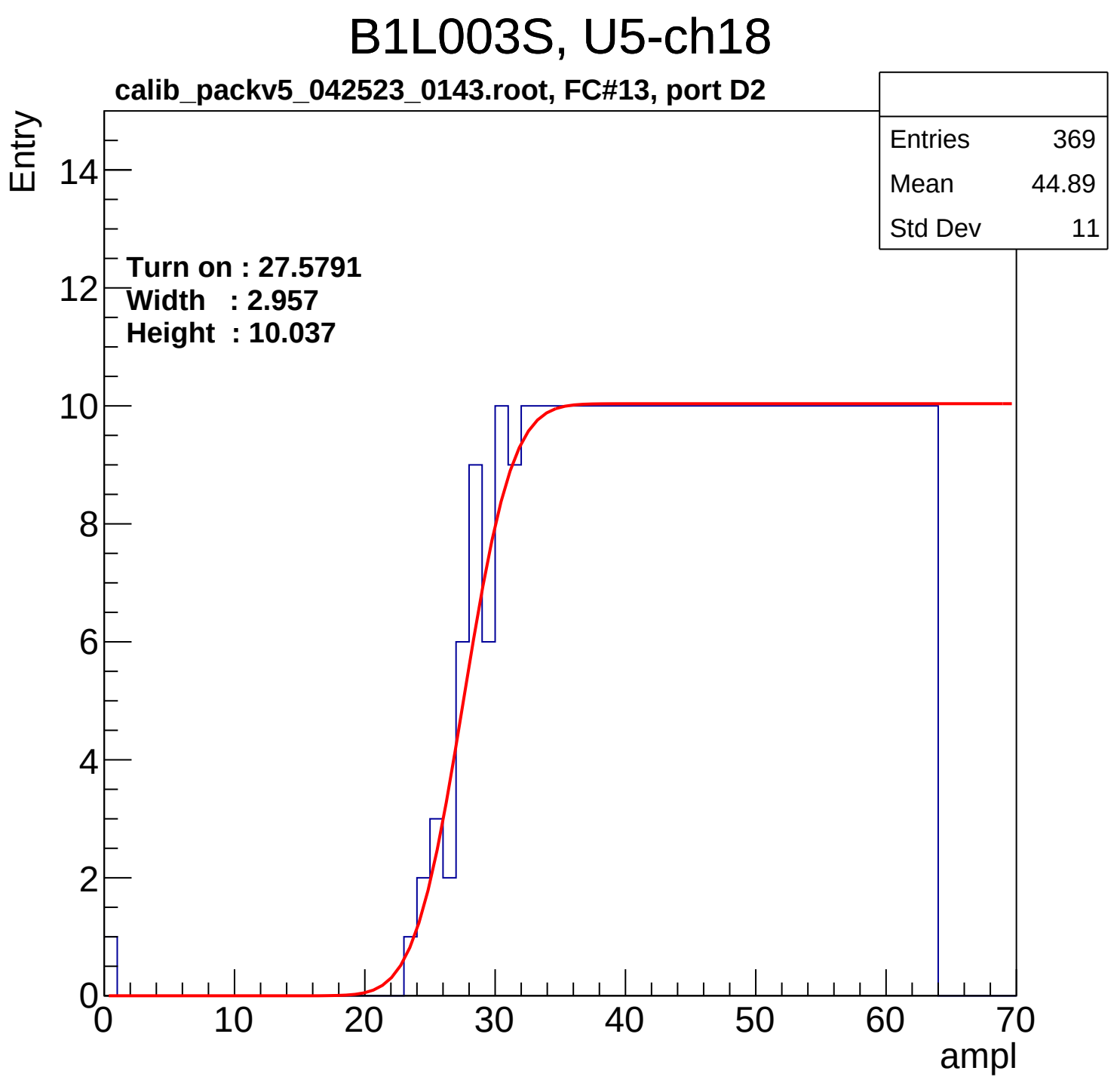
B1L003S, U5-ch18
calib_packv5_042523_0143.root, FC#13, port D2
Entries 369
Mean 44.89
Std Dev 11
Turn on : 27.5791
Width : 2.957
Height : 10.037
Entry
ampl
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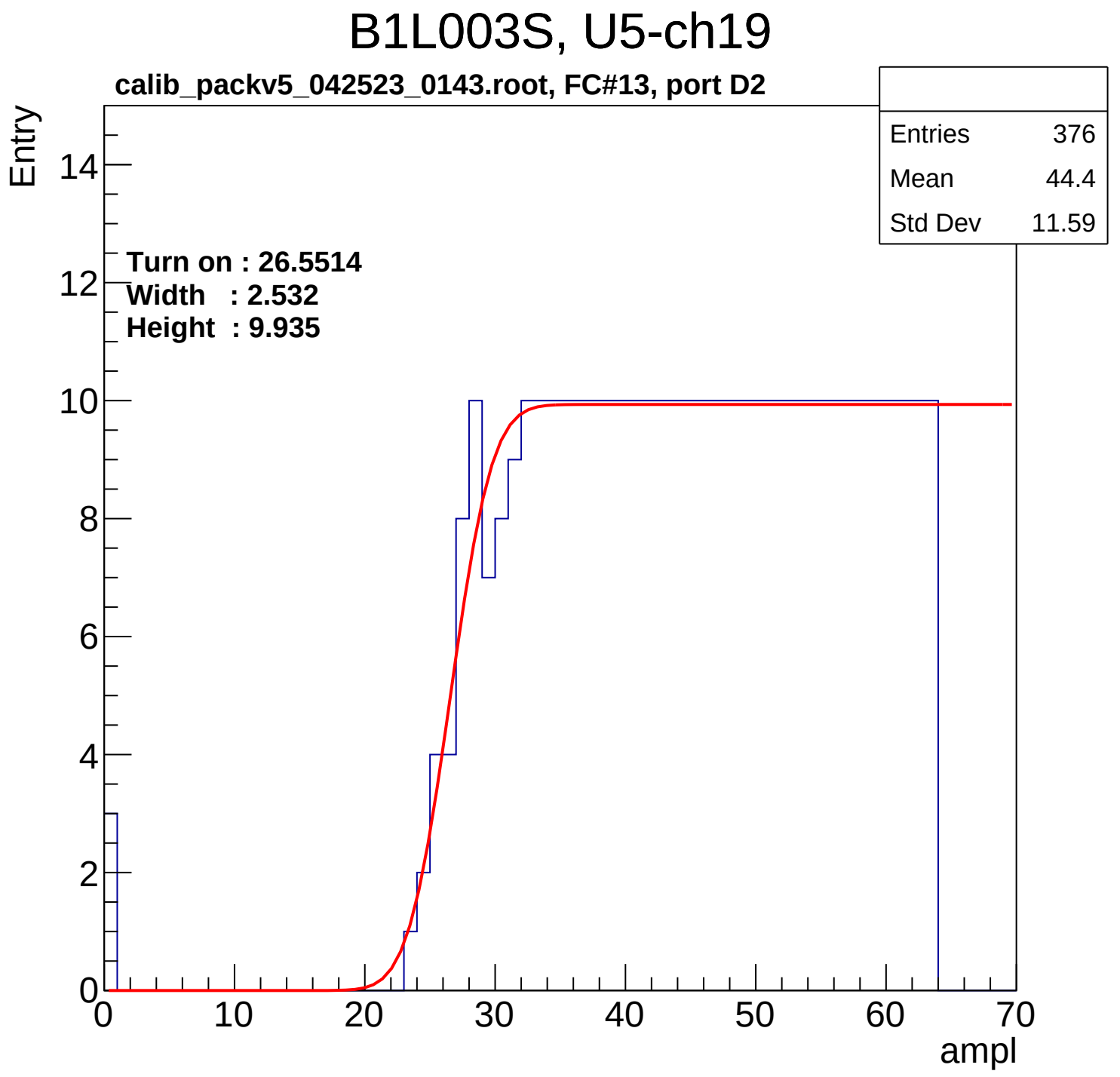
B1L003S, U5-ch19
calib_packv5_042523_0143.root, FC#13, port D2
Entries 376
Mean 44.4
Std Dev 11.59
Turn on : 26.5514
Width : 2.532
Height : 9.935
Entry
ampl
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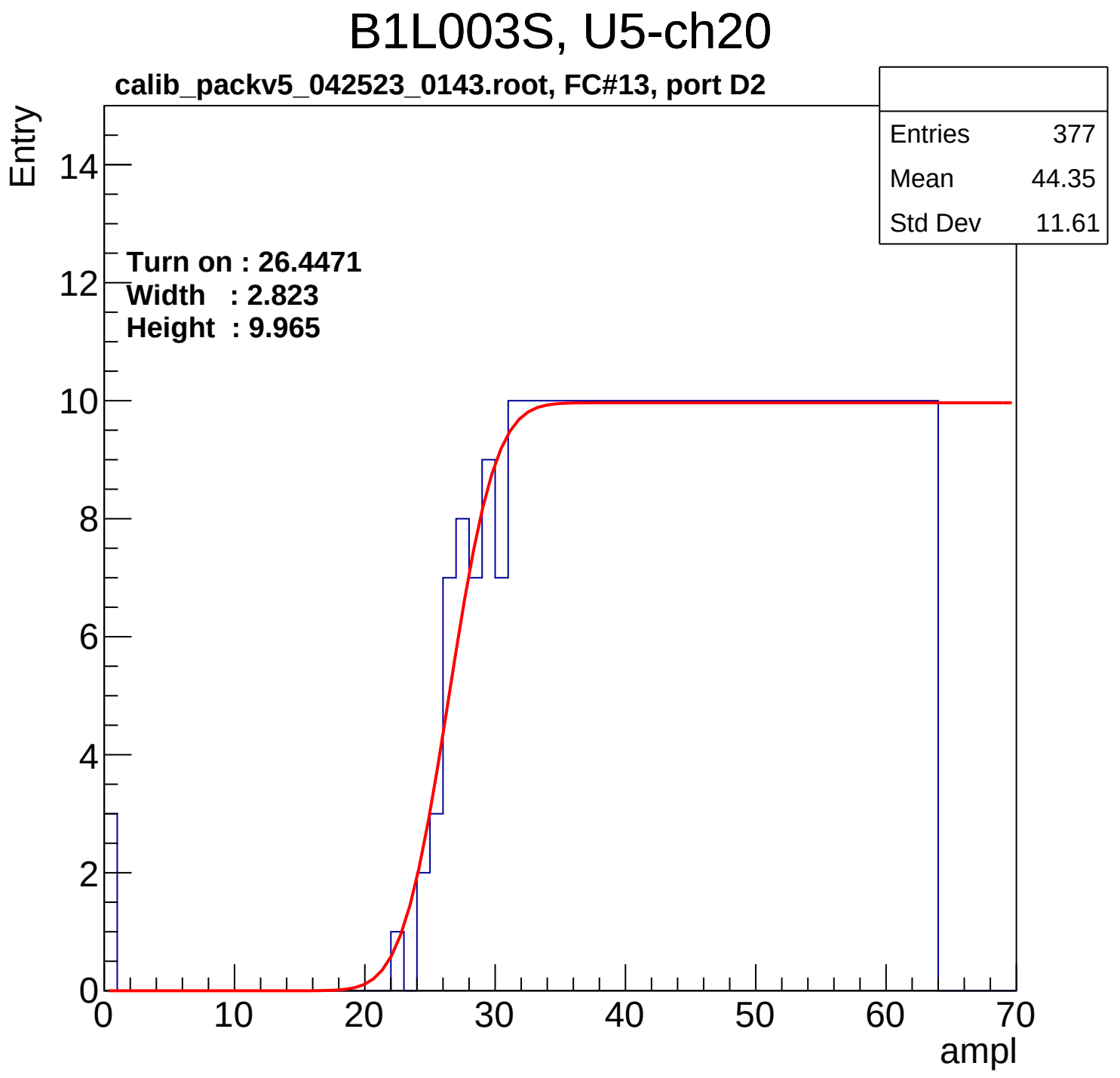
B1L003S, U5-ch20
calib_packv5_042523_0143.root, FC#13, port D2
Entries 377
Mean 44.35
Std Dev 11.61
Turn on : 26.4471
Width : 2.823
Height : 9.965
Entry
ampl
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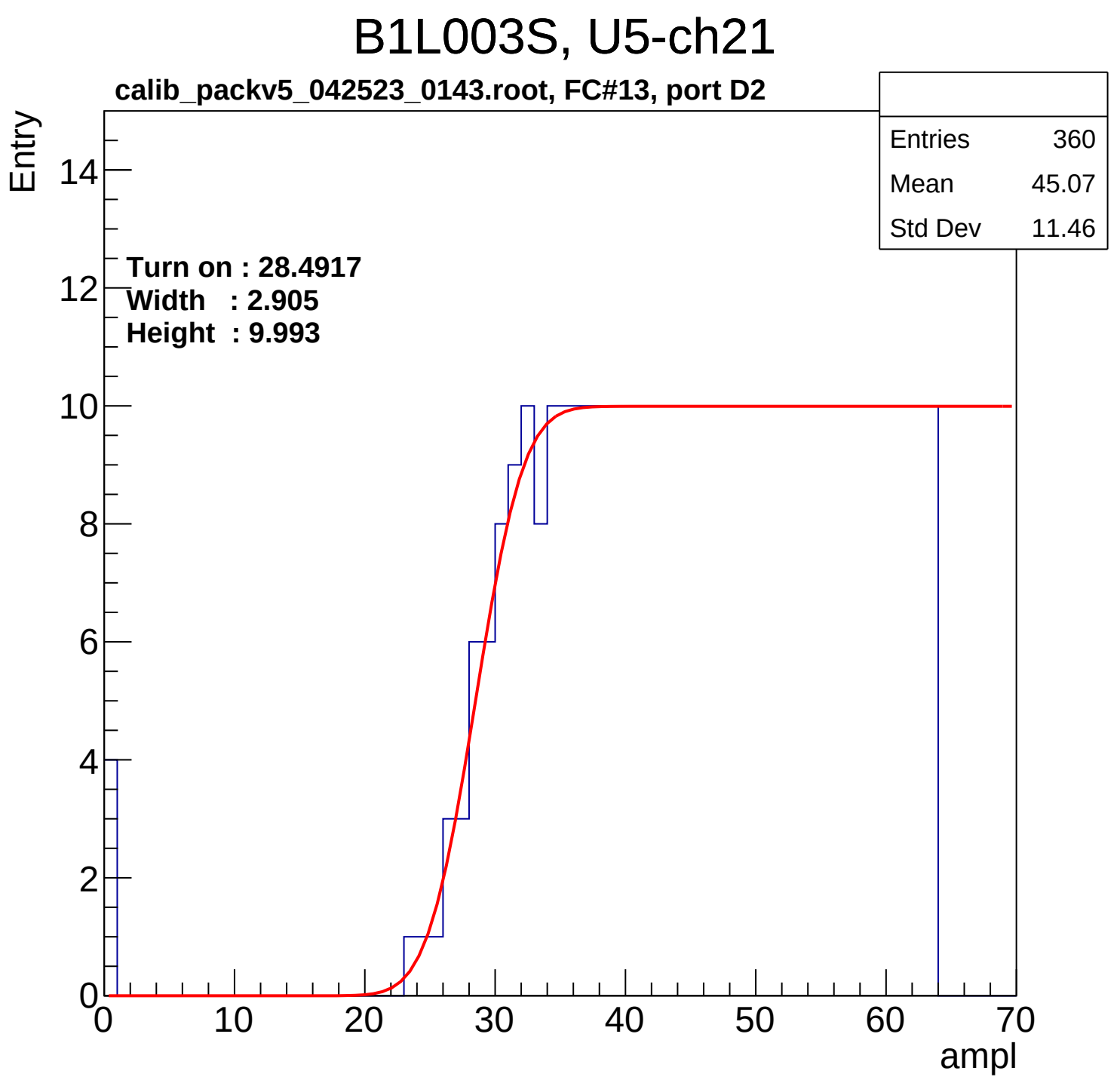
B1L003S, U5-ch21
calib_packv5_042523_0143.root, FC#13, port D2
Entries 360
Mean 45.07
Std Dev 11.46
Turn on : 28.4917
Width : 2.905
Height : 9.993
Entry
ampl
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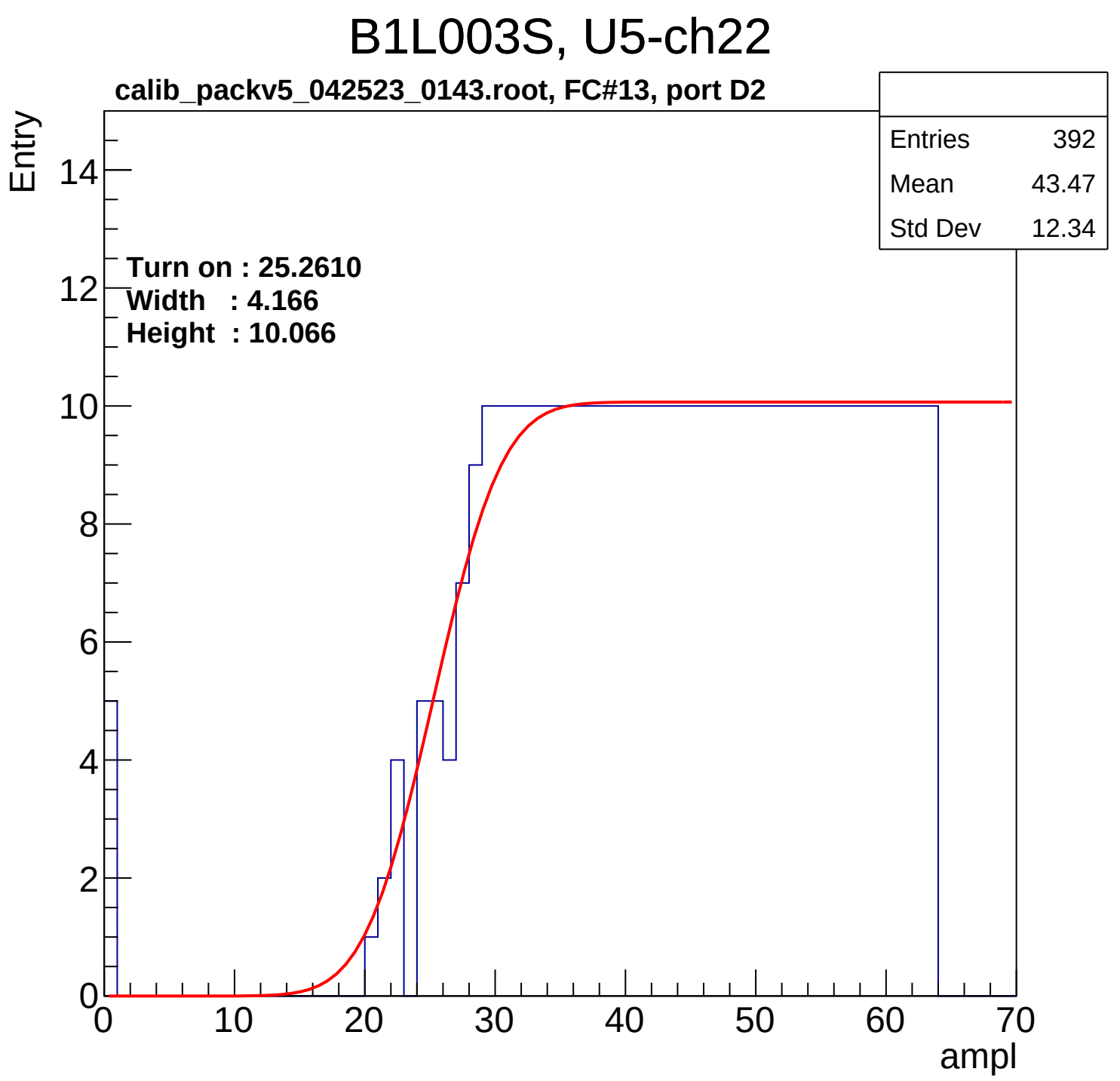
B1L003S, U5-ch22
calib_packv5_042523_0143.root, FC#13, port D2
Entries 392
Mean 43.47
Std Dev 12.34
Turn on : 25.2610
Width : 4.166
Height : 10.066
Entry
ampl
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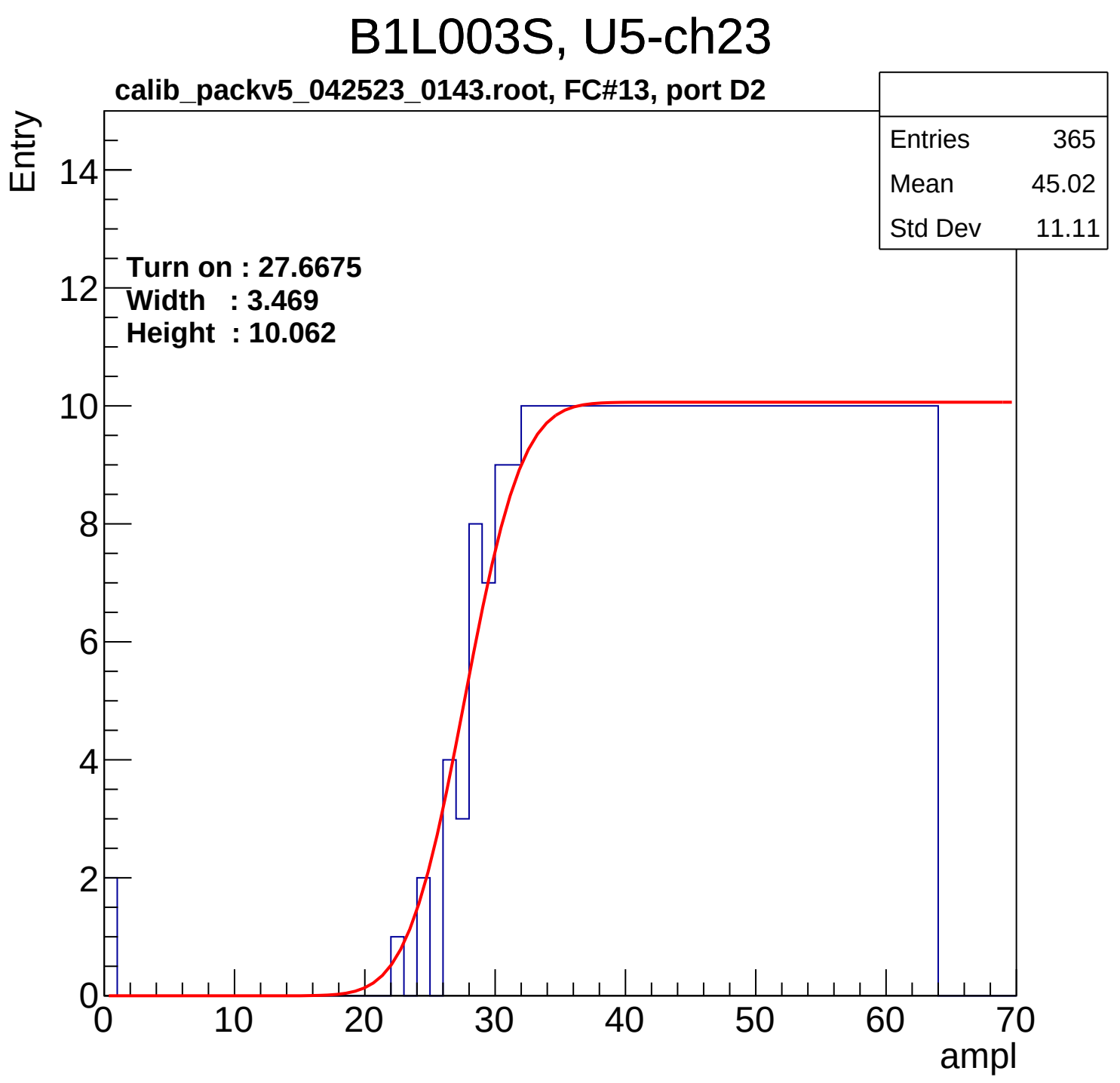
B1L003S, U5-ch23
calib_packv5_042523_0143.root, FC#13, port D2
Entries 365
Mean 45.02
Std Dev 11.11
Turn on : 27.6675
Width : 3.469
Height : 10.062
Entry
ampl
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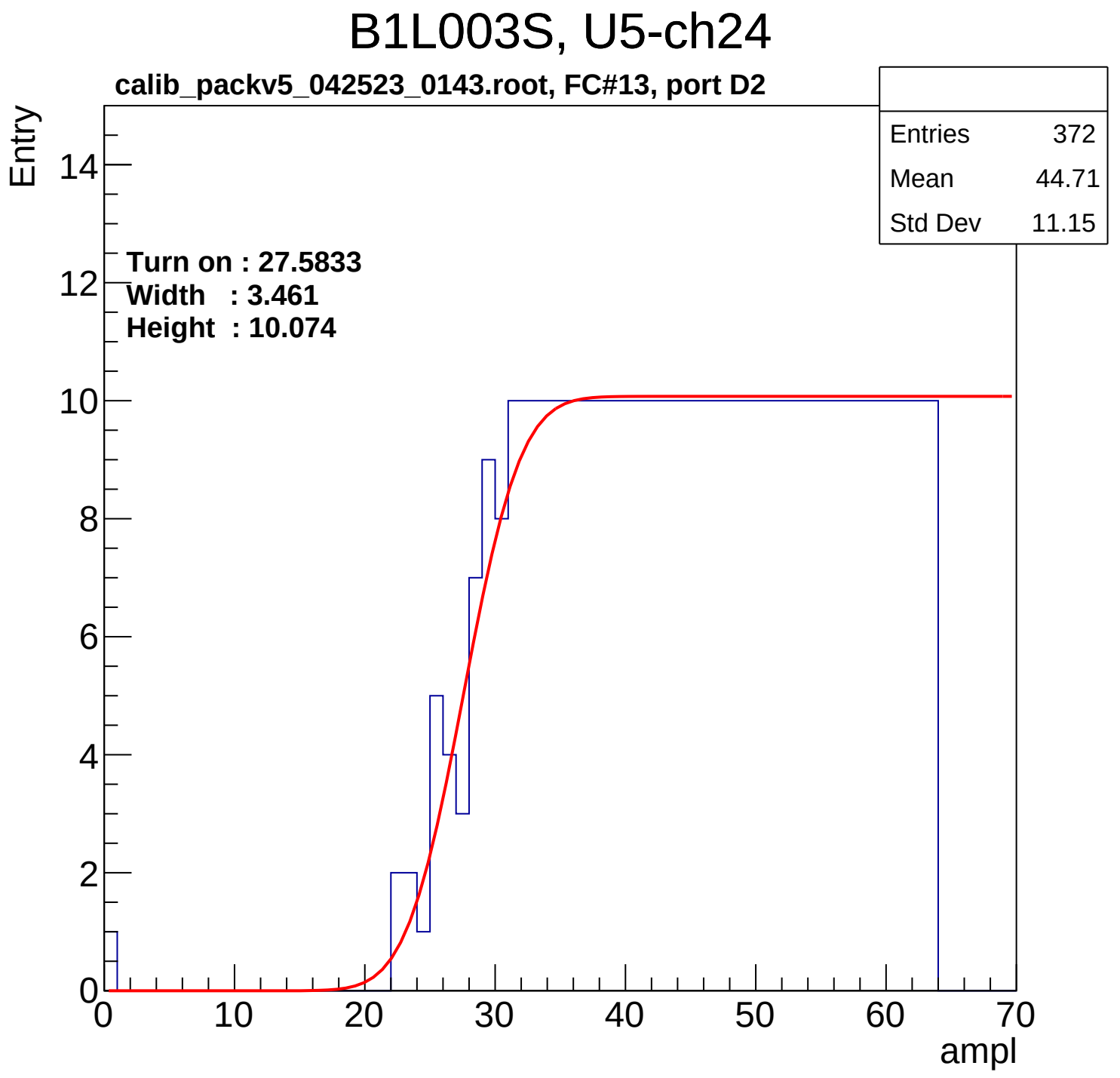
B1L003S, U5-ch24
calib_packv5_042523_0143.root, FC#13, port D2
Entries 372
Mean 44.71
Std Dev 11.15
Turn on : 27.5833
Width : 3.461
Height : 10.074
Entry
ampl
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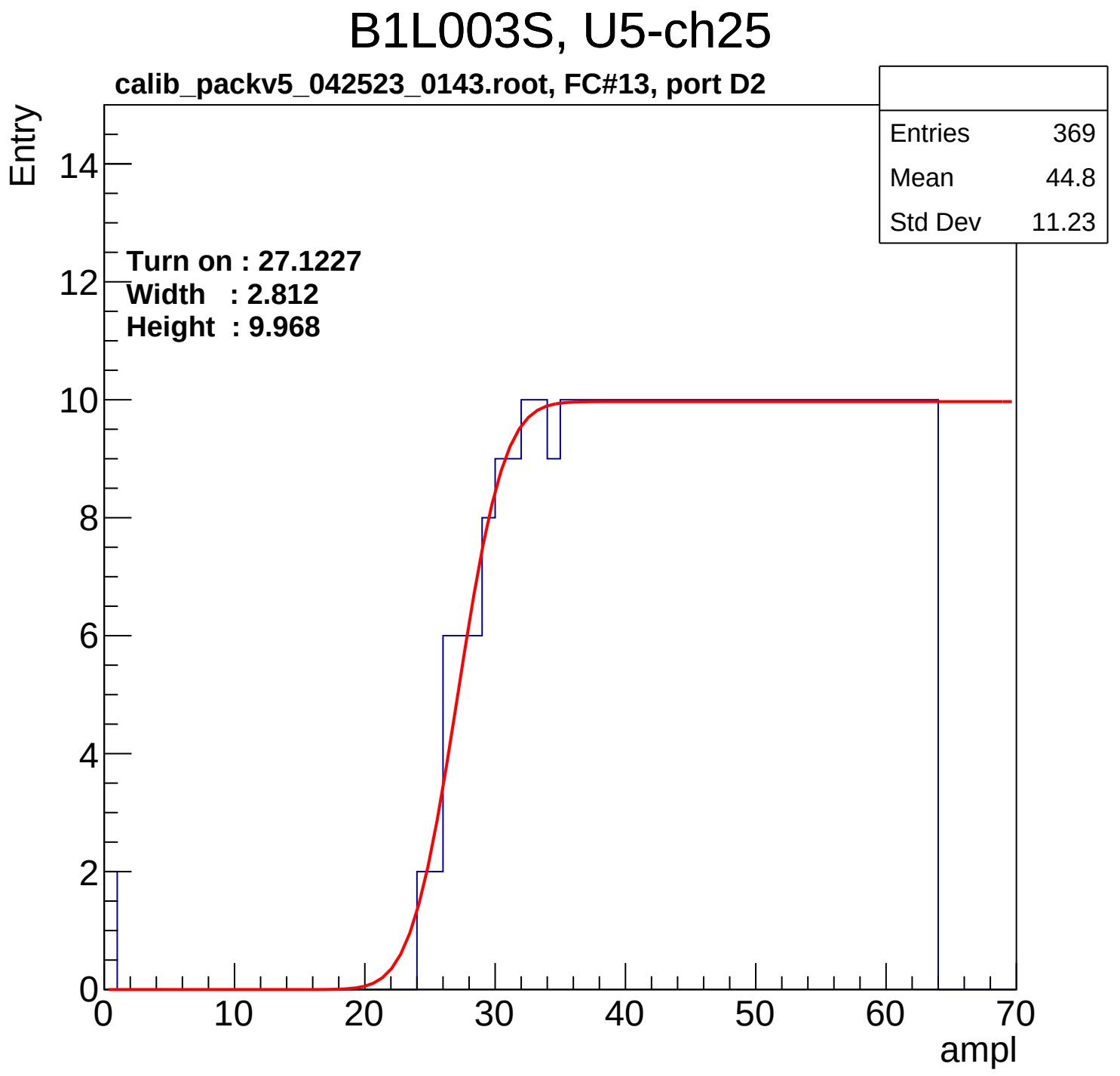
B1L003S, U5-ch25
calib_packv5_042523_0143.root, FC#13, port D2
Entries 369
Mean 44.8
Std Dev 11.23
Turn on : 27.1227
Width : 2.812
Height : 9.968
Entry
ampl
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6
8
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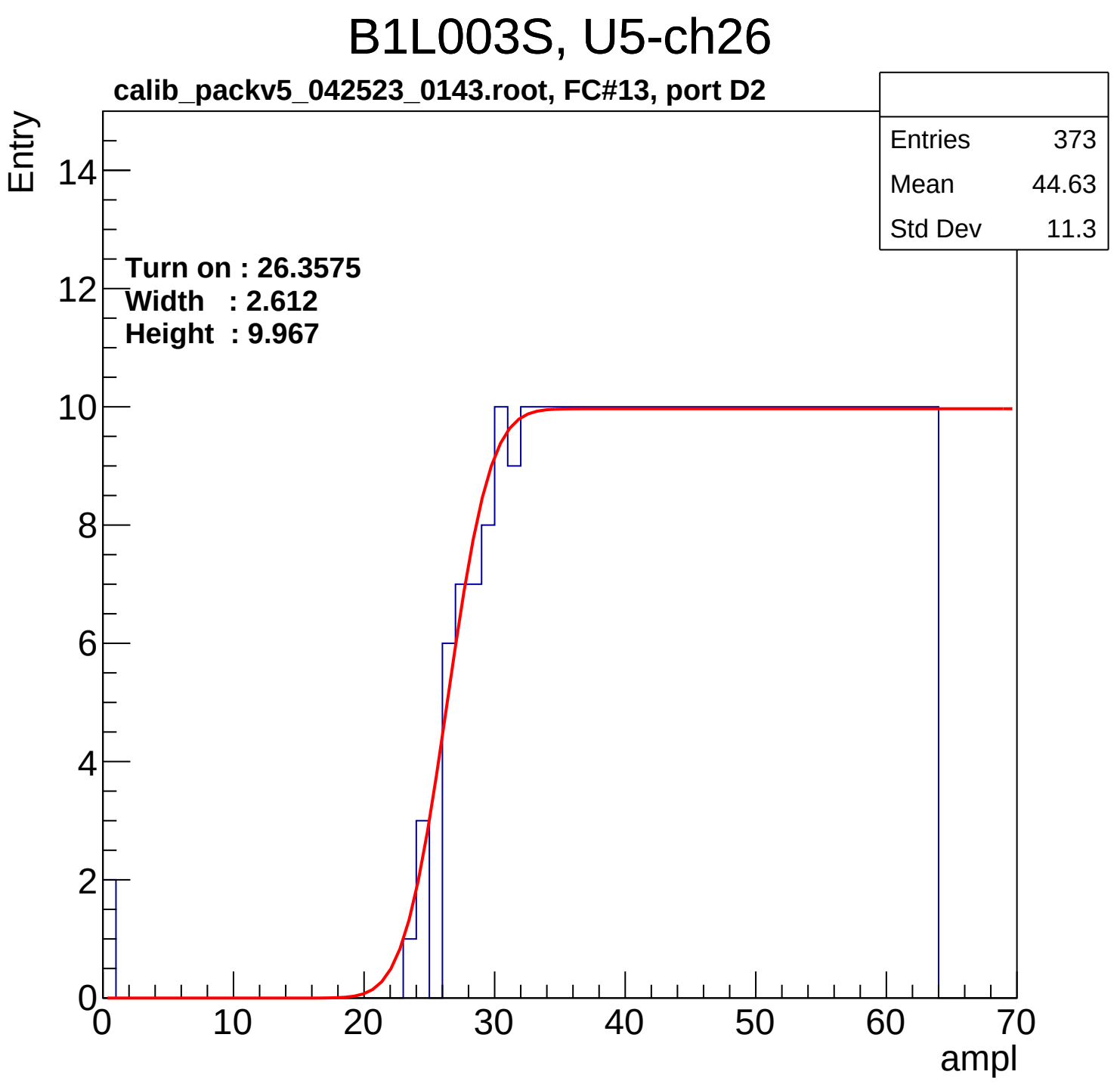
B1L003S, U5-ch26
calib_packv5_042523_0143.root, FC#13, port D2
Entries 373
Mean 44.63
Std Dev 11.3
Turn on : 26.3575
Width : 2.612
Height : 9.967
Entry
ampl
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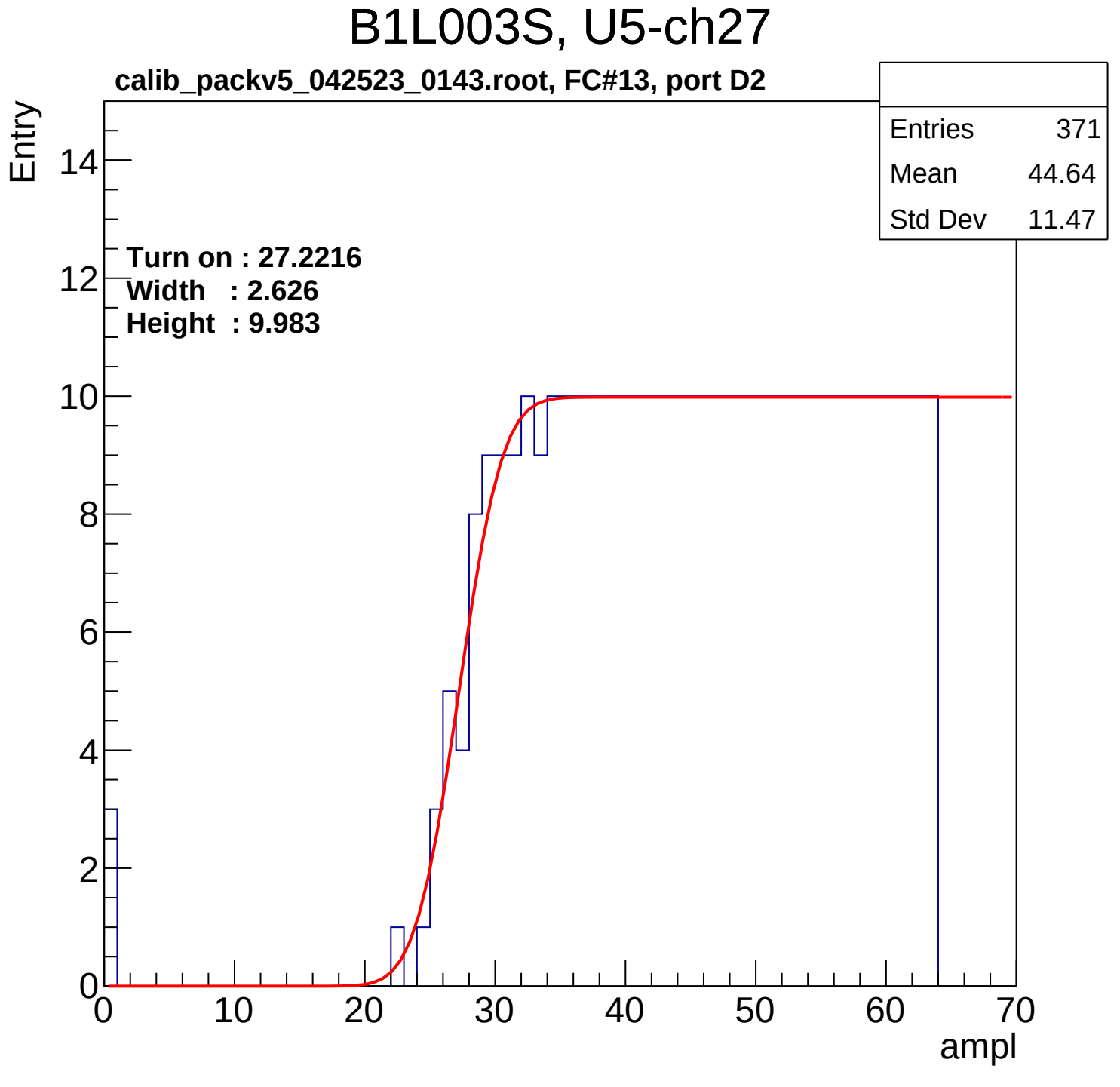
B1L003S, U5-ch27
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.64
Std Dev 11.47
Turn on : 27.2216
Width : 2.626
Height : 9.983
Entry
ampl
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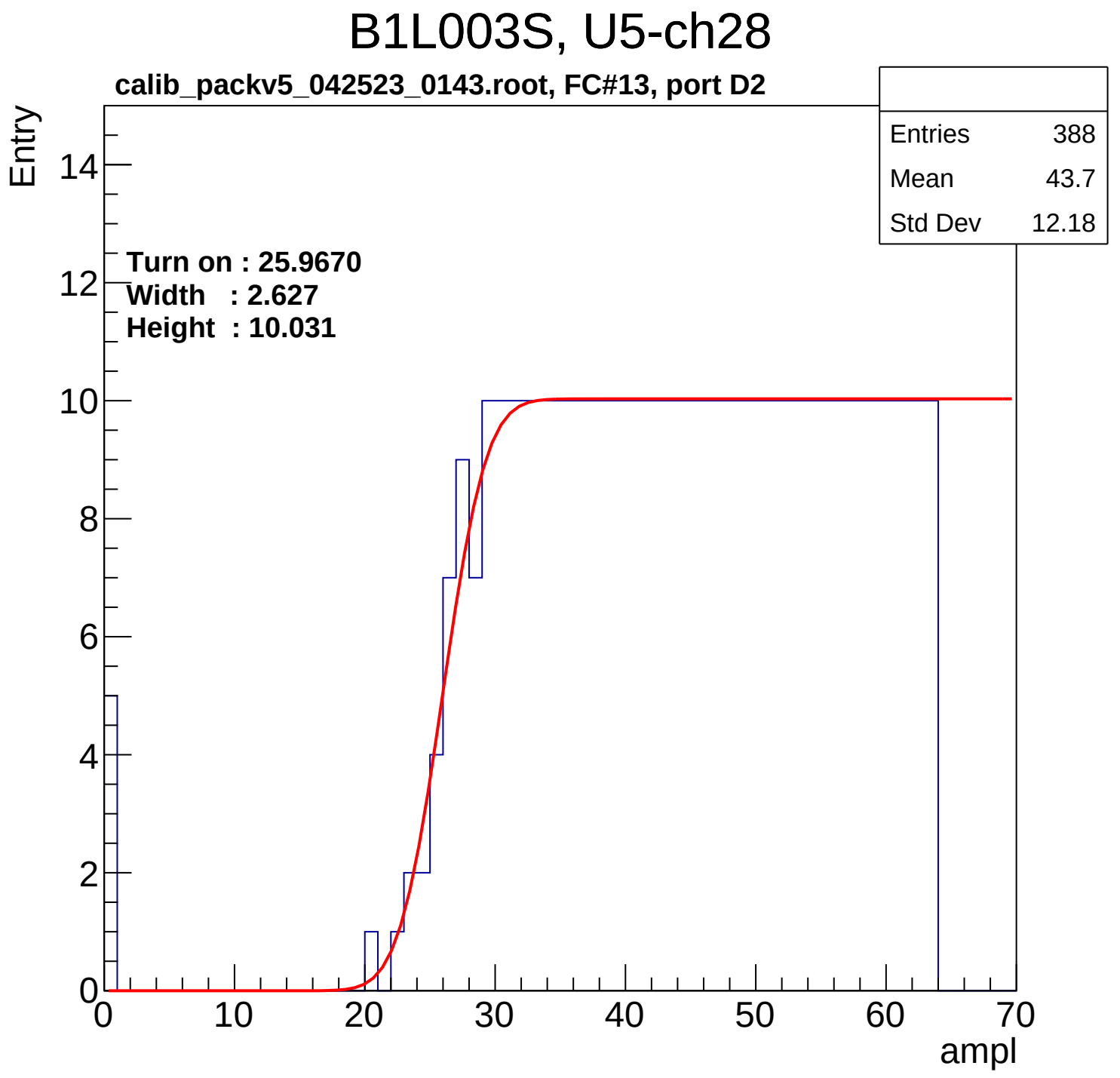
B1L003S, U5-ch28
calib_packv5_042523_0143.root, FC#13, port D2
Entries 388
Mean 43.7
Std Dev 12.18
Turn on : 25.9670
Width : 2.627
Height : 10.031
Entry
ampl
0
2
4
6
8
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12
14
0
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20
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40
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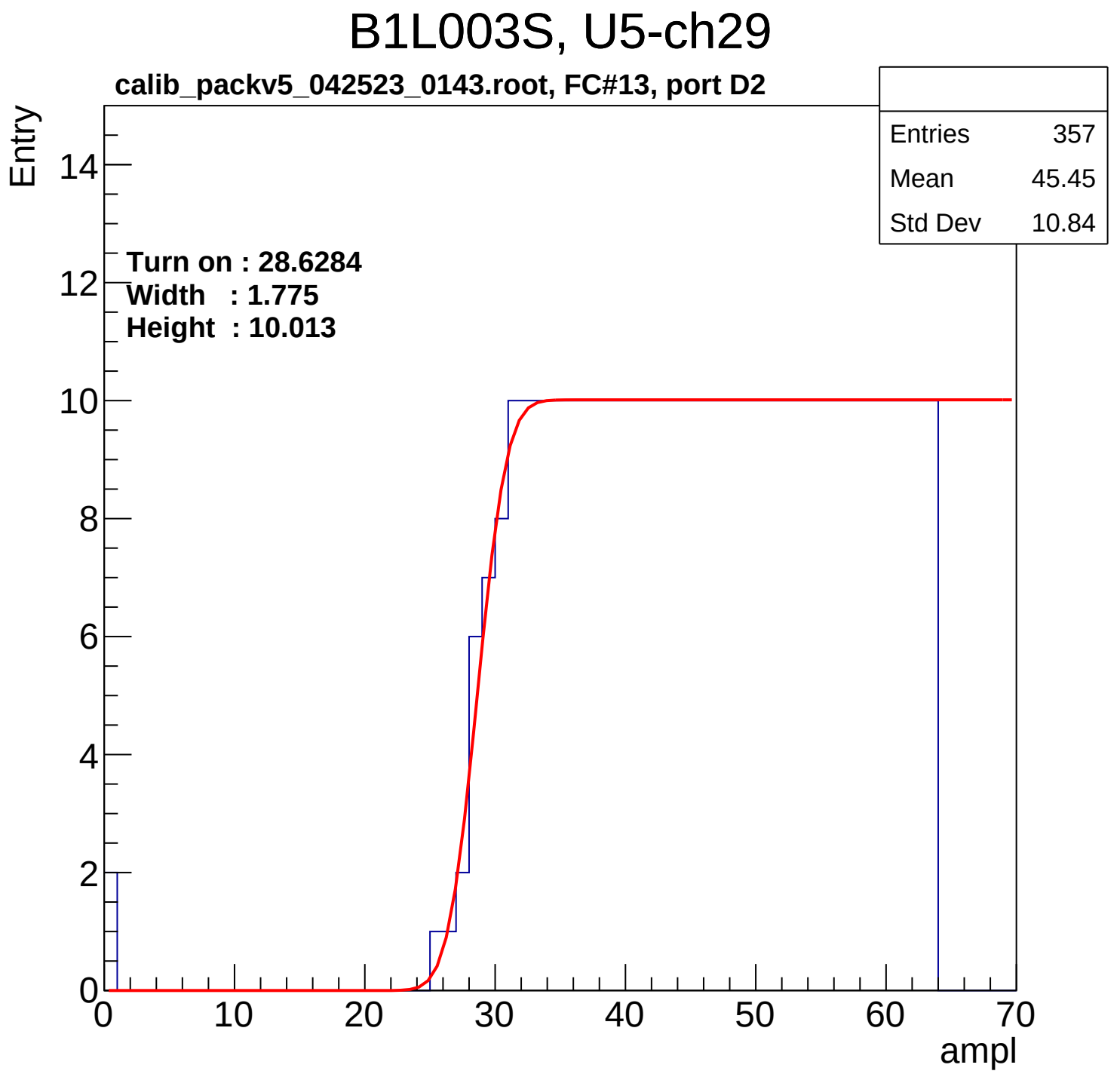
B1L003S, U5-ch29
calib_packv5_042523_0143.root, FC#13, port D2
Entries 357
Mean 45.45
Std Dev 10.84
Turn on : 28.6284
Width : 1.775
Height : 10.013
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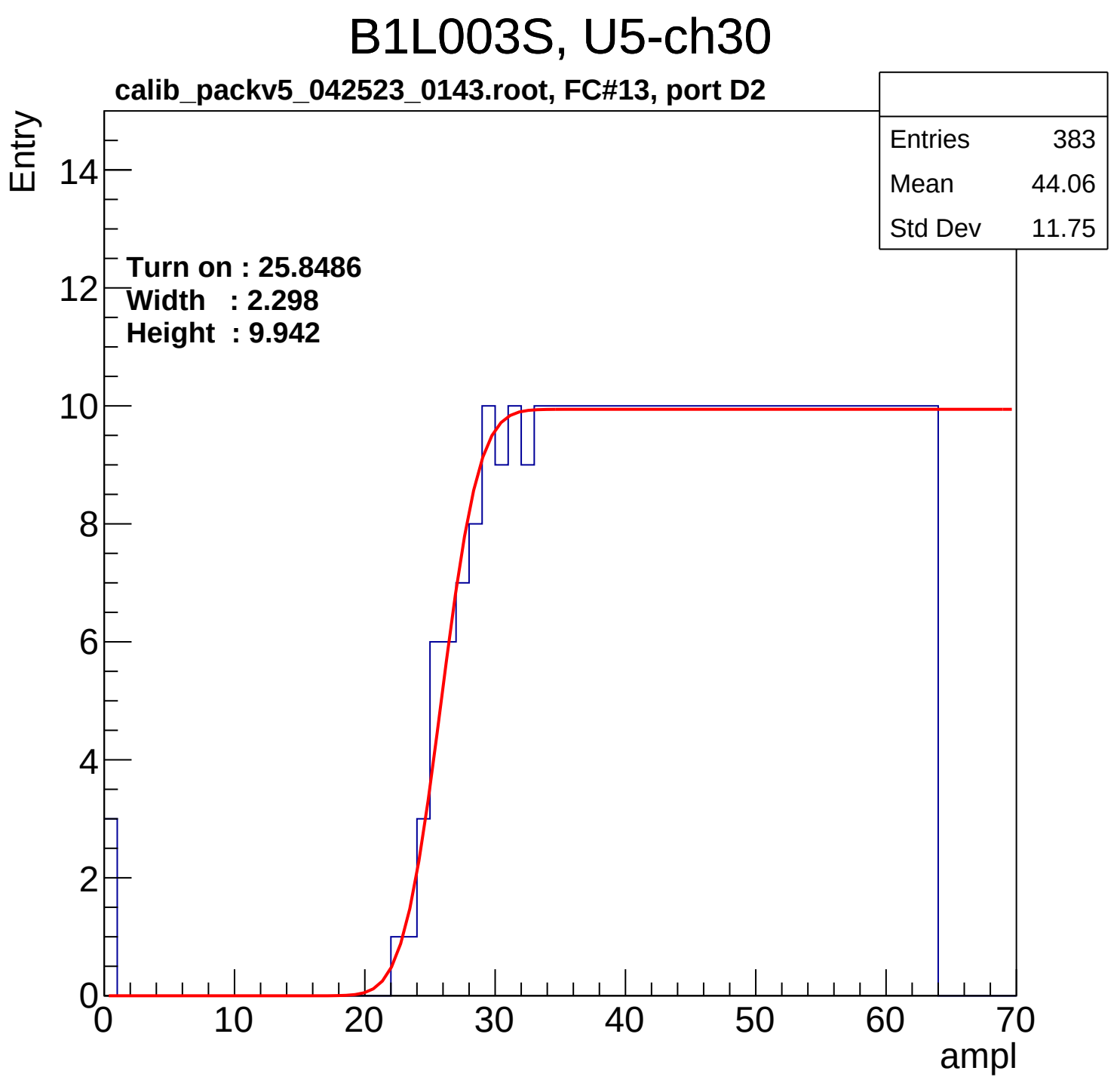
B1L003S, U5-ch30
calib_packv5_042523_0143.root, FC#13, port D2
Entries 383
Mean 44.06
Std Dev 11.75
Turn on : 25.8486
Width : 2.298
Height : 9.942
Entry
ampl
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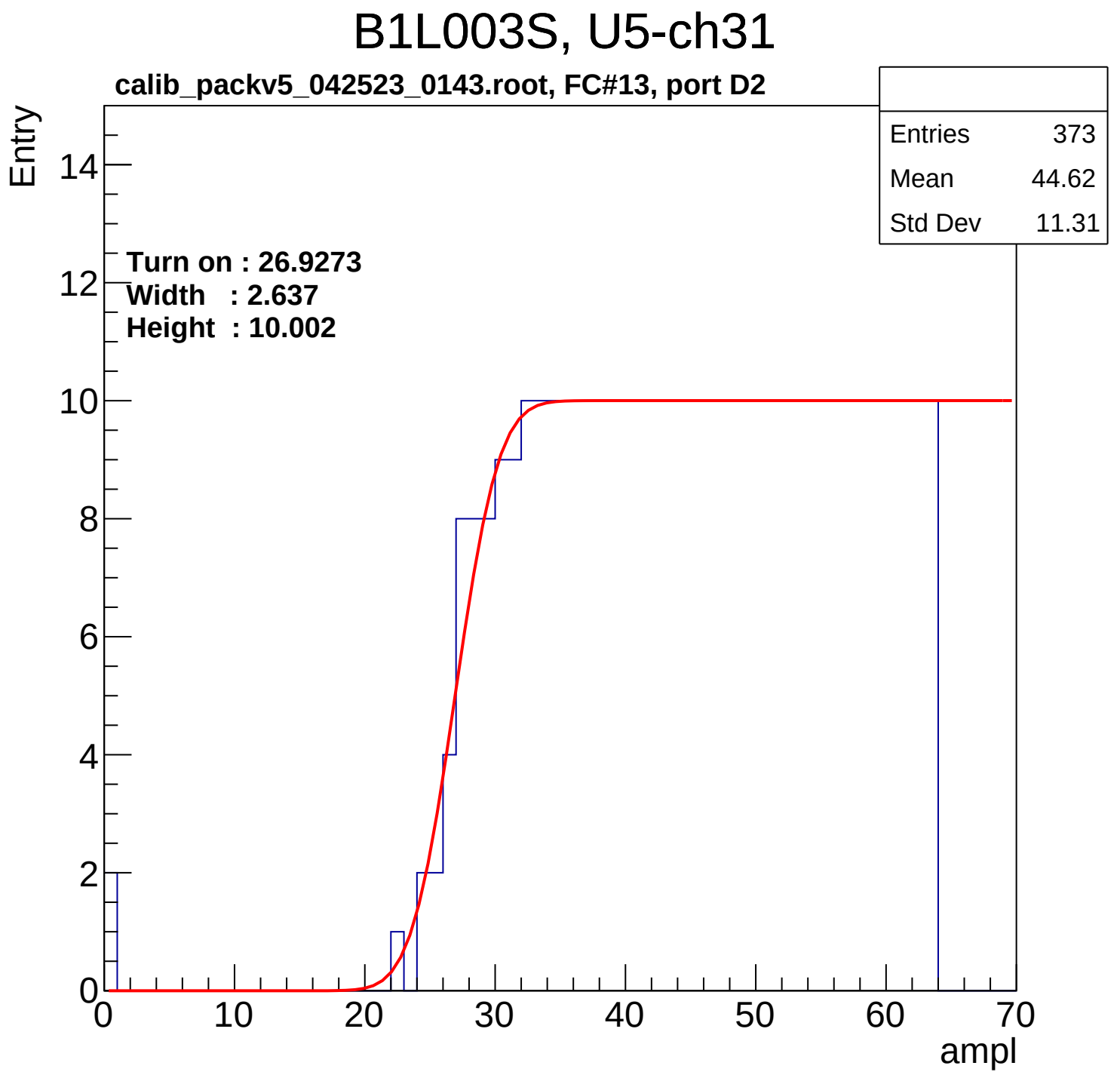
B1L003S, U5-ch31
calib_packv5_042523_0143.root, FC#13, port D2
Entries 373
Mean 44.62
Std Dev 11.31
Turn on : 26.9273
Width : 2.637
Height : 10.002
Entry
ampl
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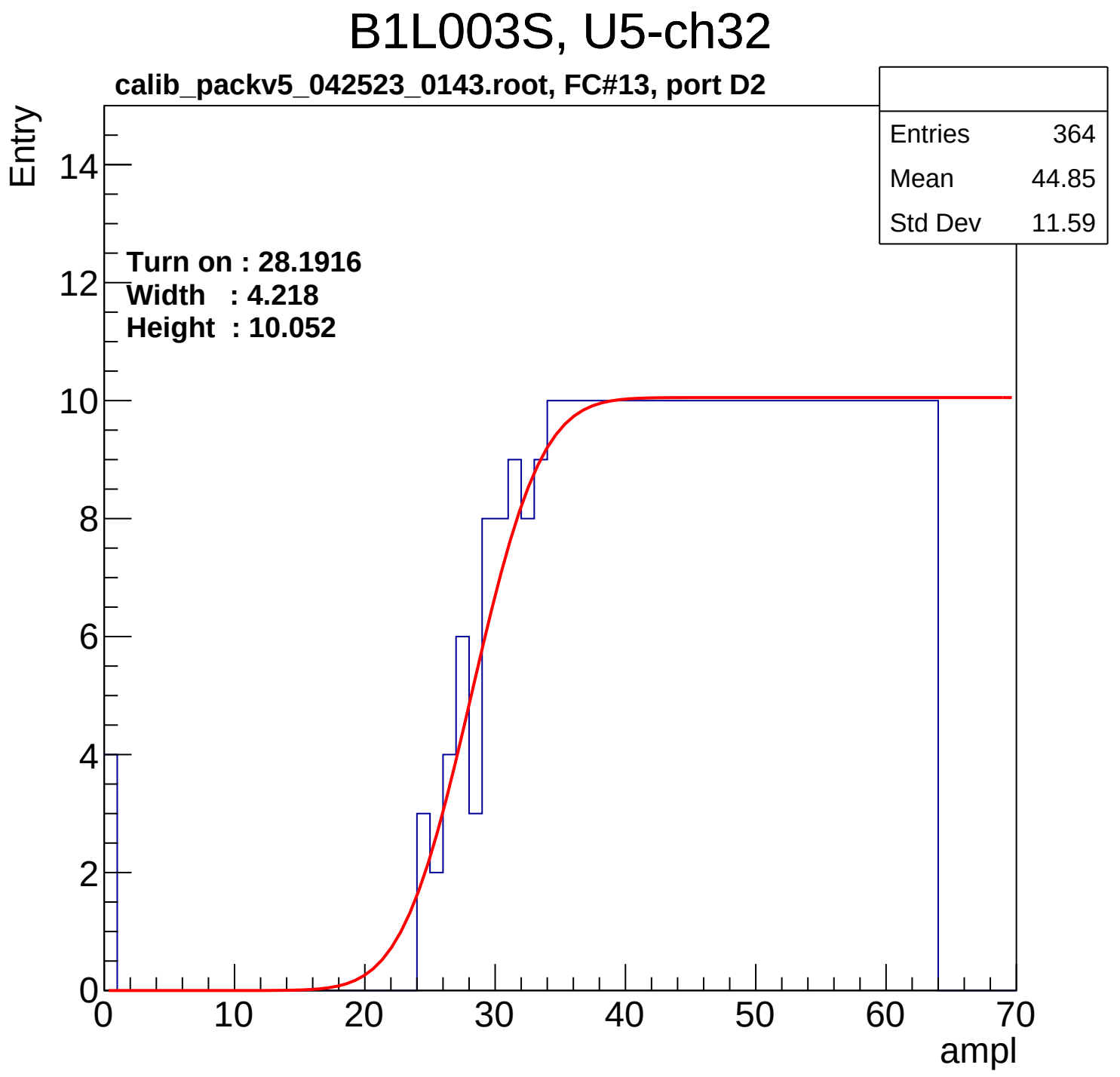
B1L003S, U5-ch32
calib_packv5_042523_0143.root, FC#13, port D2
Entries 364
Mean 44.85
Std Dev 11.59
Turn on : 28.1916
Width : 4.218
Height : 10.052
Entry
ampl
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4
6
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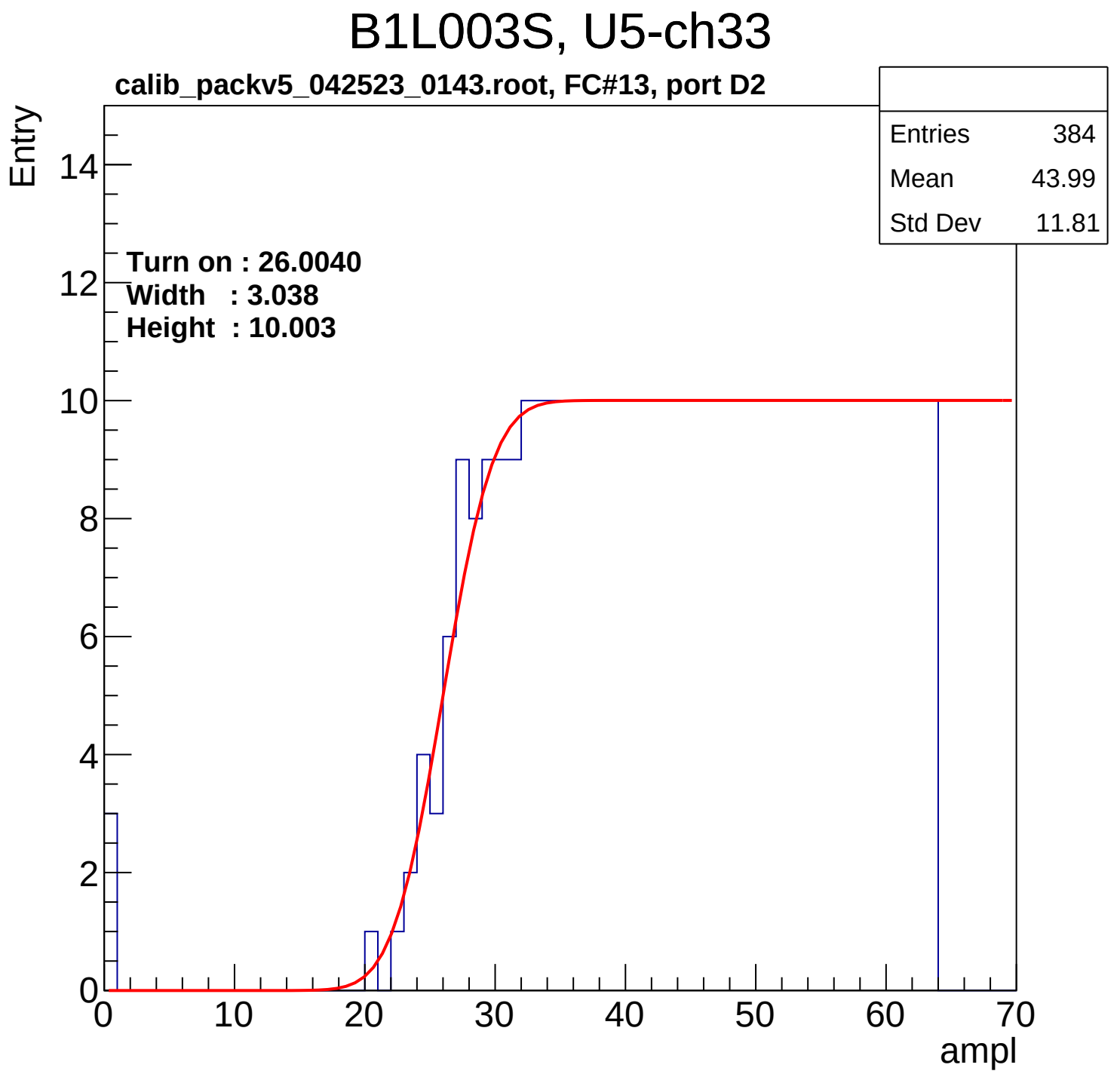
B1L003S, U5-ch33
calib_packv5_042523_0143.root, FC#13, port D2
Entries 384
Mean 43.99
Std Dev 11.81
Turn on : 26.0040
Width : 3.038
Height : 10.003
Entry
ampl
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6
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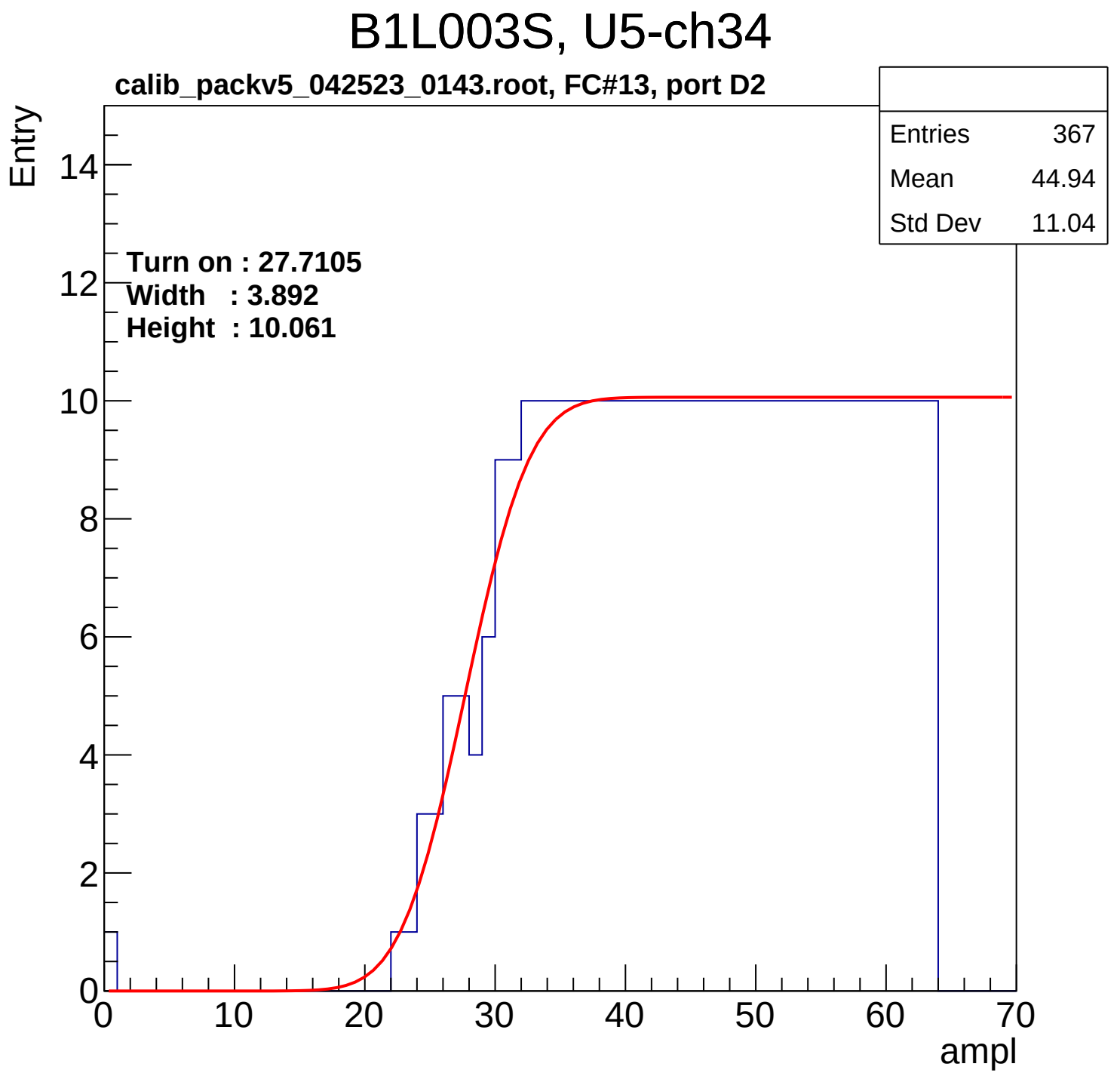
B1L003S, U5-ch34
calib_packv5_042523_0143.root, FC#13, port D2
Entries 367
Mean 44.94
Std Dev 11.04
Turn on : 27.7105
Width : 3.892
Height : 10.061
Entry
ampl
0
2
4
6
8
10
12
14
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60
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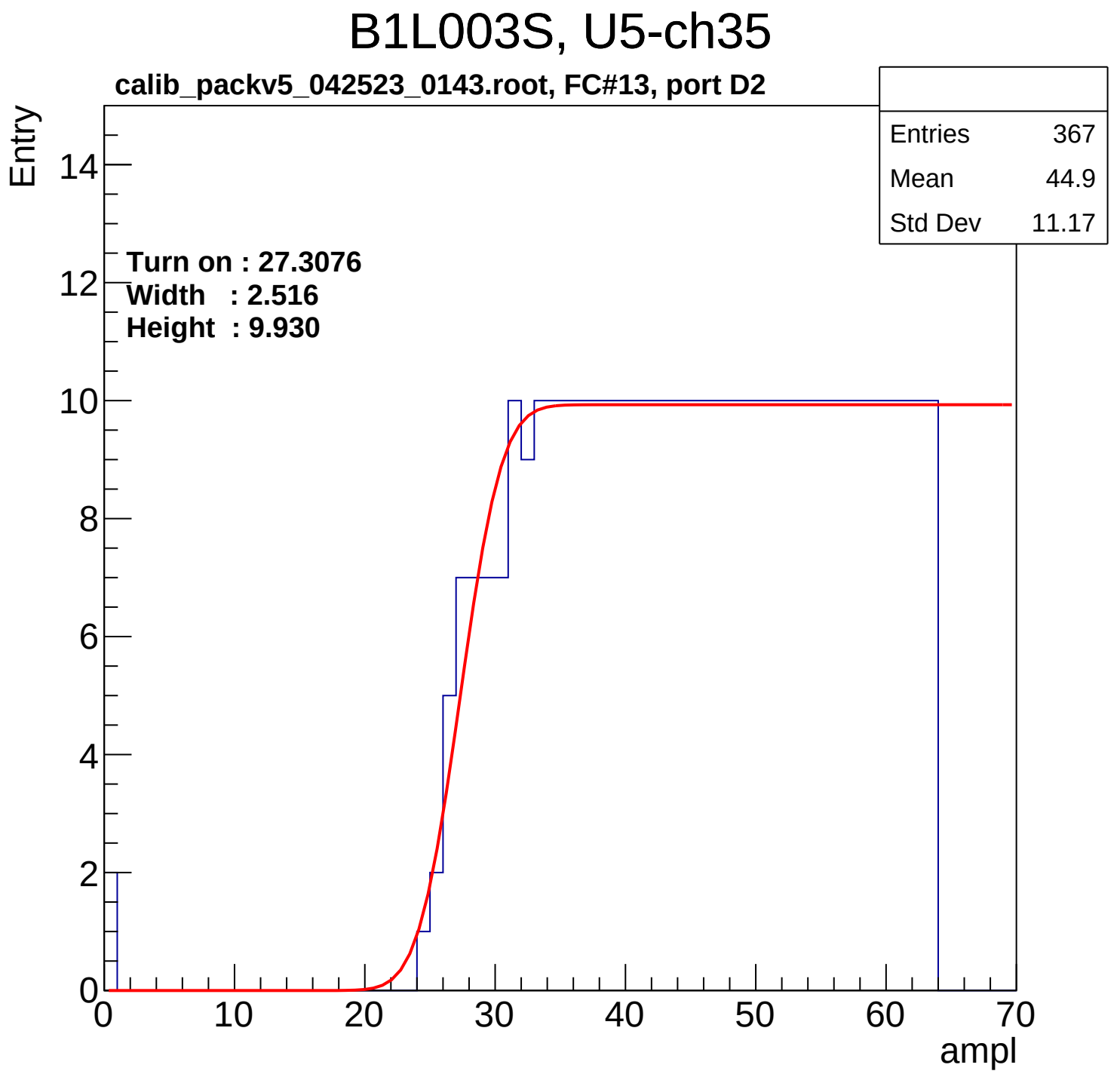
B1L003S, U5-ch35
calib_packv5_042523_0143.root, FC#13, port D2
Entries 367
Mean 44.9
Std Dev 11.17
Turn on : 27.3076
Width : 2.516
Height : 9.930
Entry
ampl
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2
4
6
8
10
12
14
0
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60
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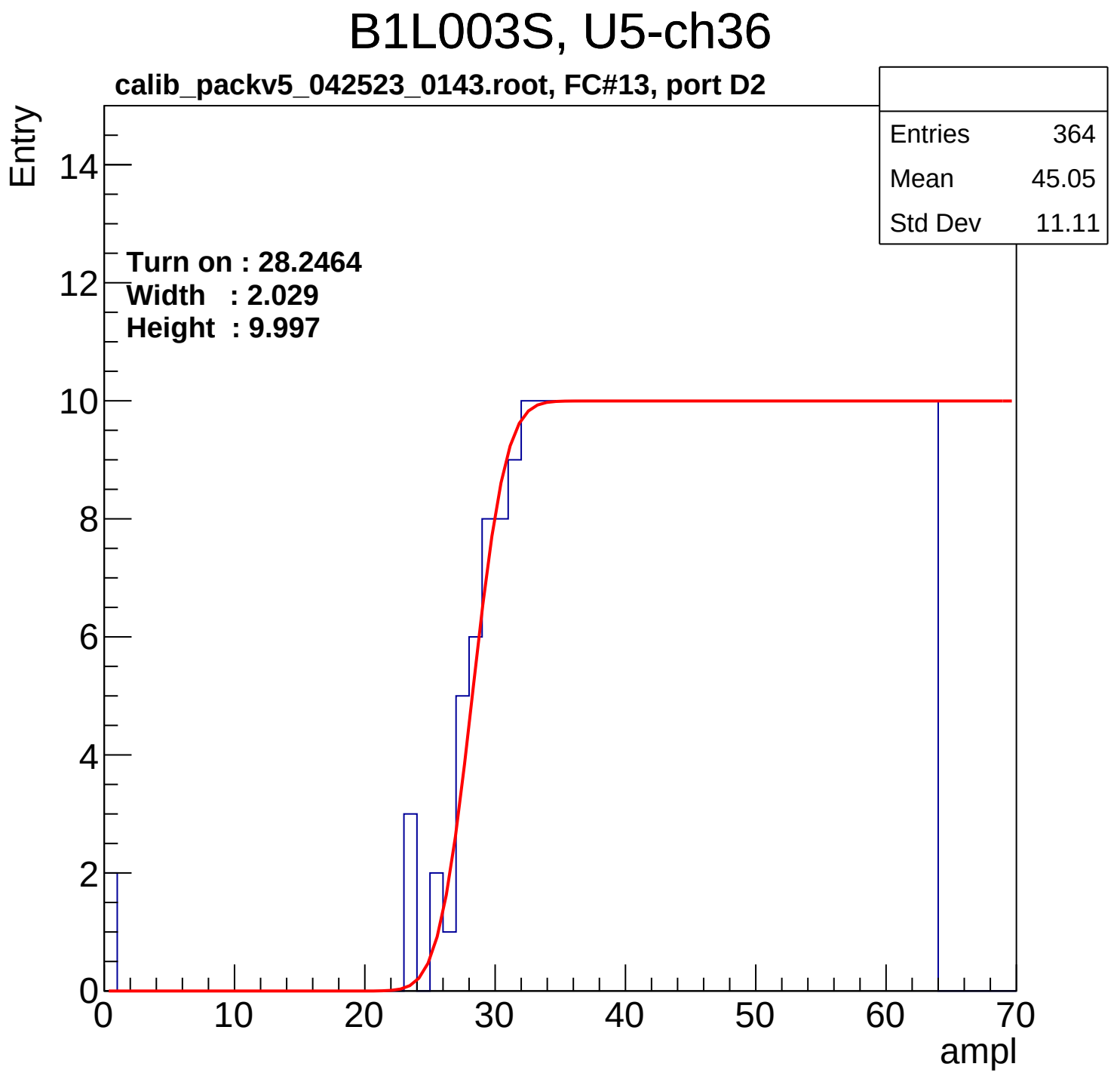
B1L003S, U5-ch36
calib_packv5_042523_0143.root, FC#13, port D2
Entries 364
Mean 45.05
Std Dev 11.11
Turn on : 28.2464
Width : 2.029
Height : 9.997
Entry
ampl
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2
4
6
8
10
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0
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60
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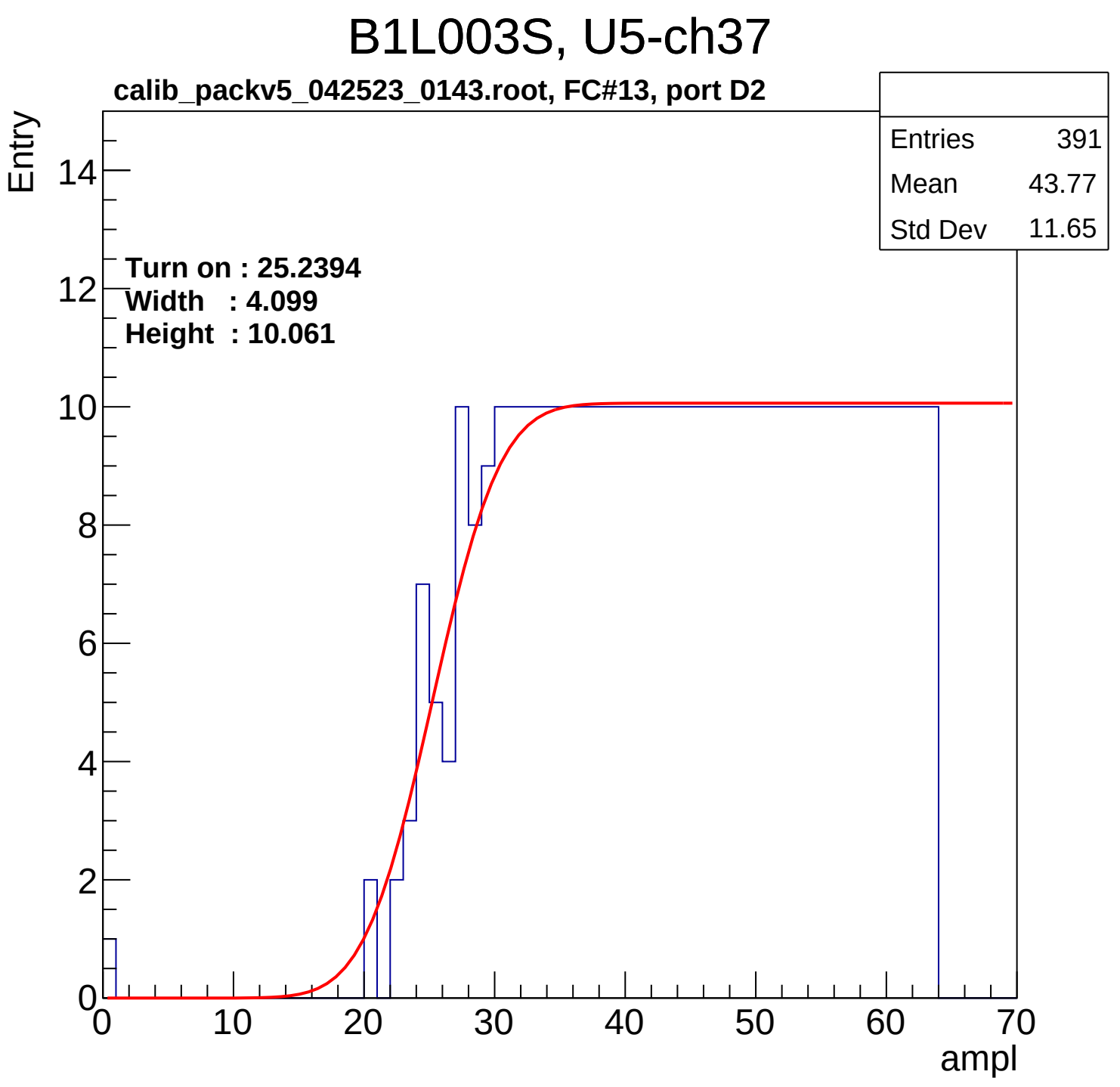
B1L003S, U5-ch37
calib_packv5_042523_0143.root, FC#13, port D2
Entries 391
Mean 43.77
Std Dev 11.65
Turn on : 25.2394
Width : 4.099
Height : 10.061
Entry
ampl
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4
6
8
10
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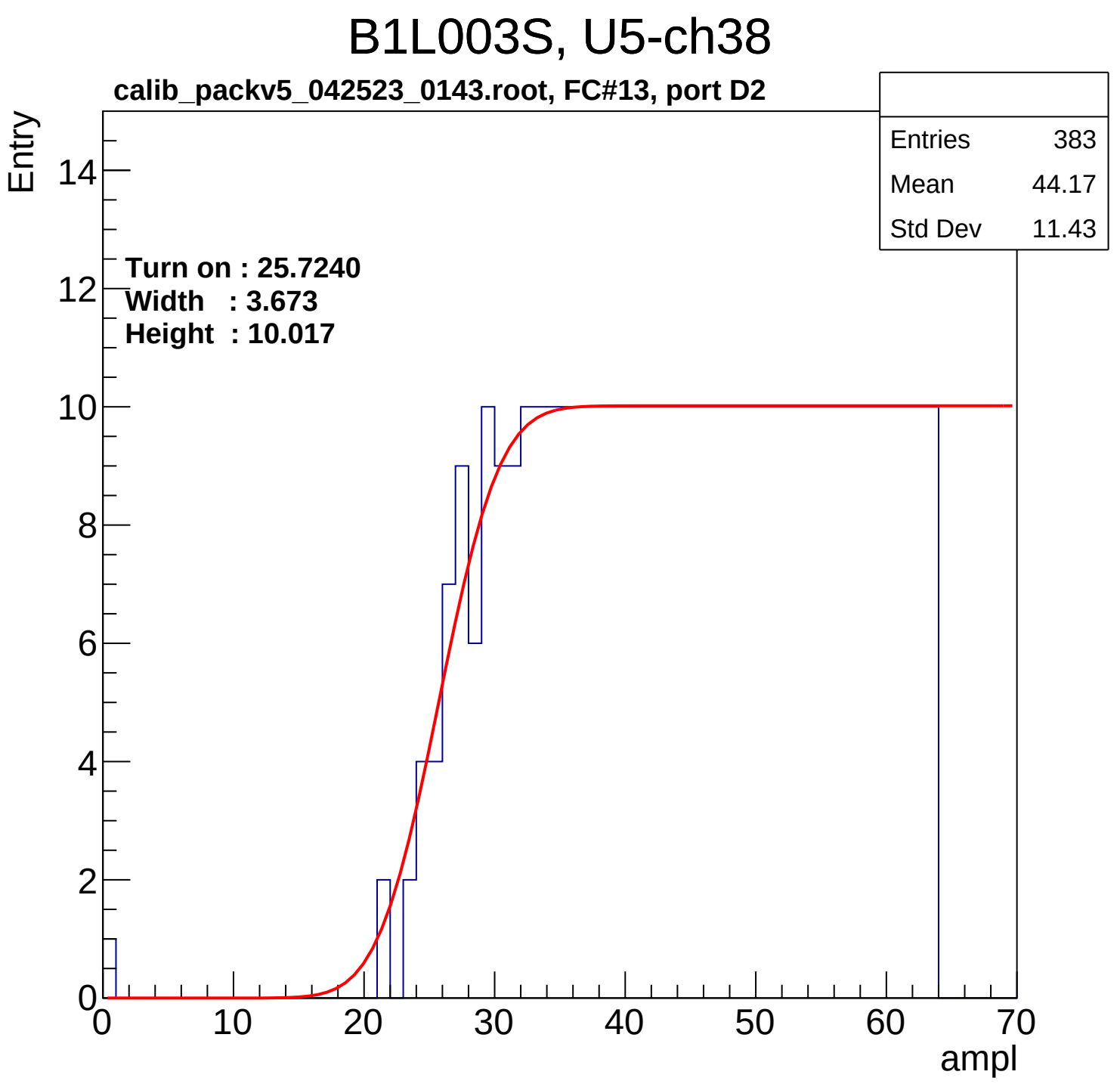
B1L003S, U5-ch38
calib_packv5_042523_0143.root, FC#13, port D2
Entries 383
Mean 44.17
Std Dev 11.43
Turn on : 25.7240
Width : 3.673
Height : 10.017
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
50
60
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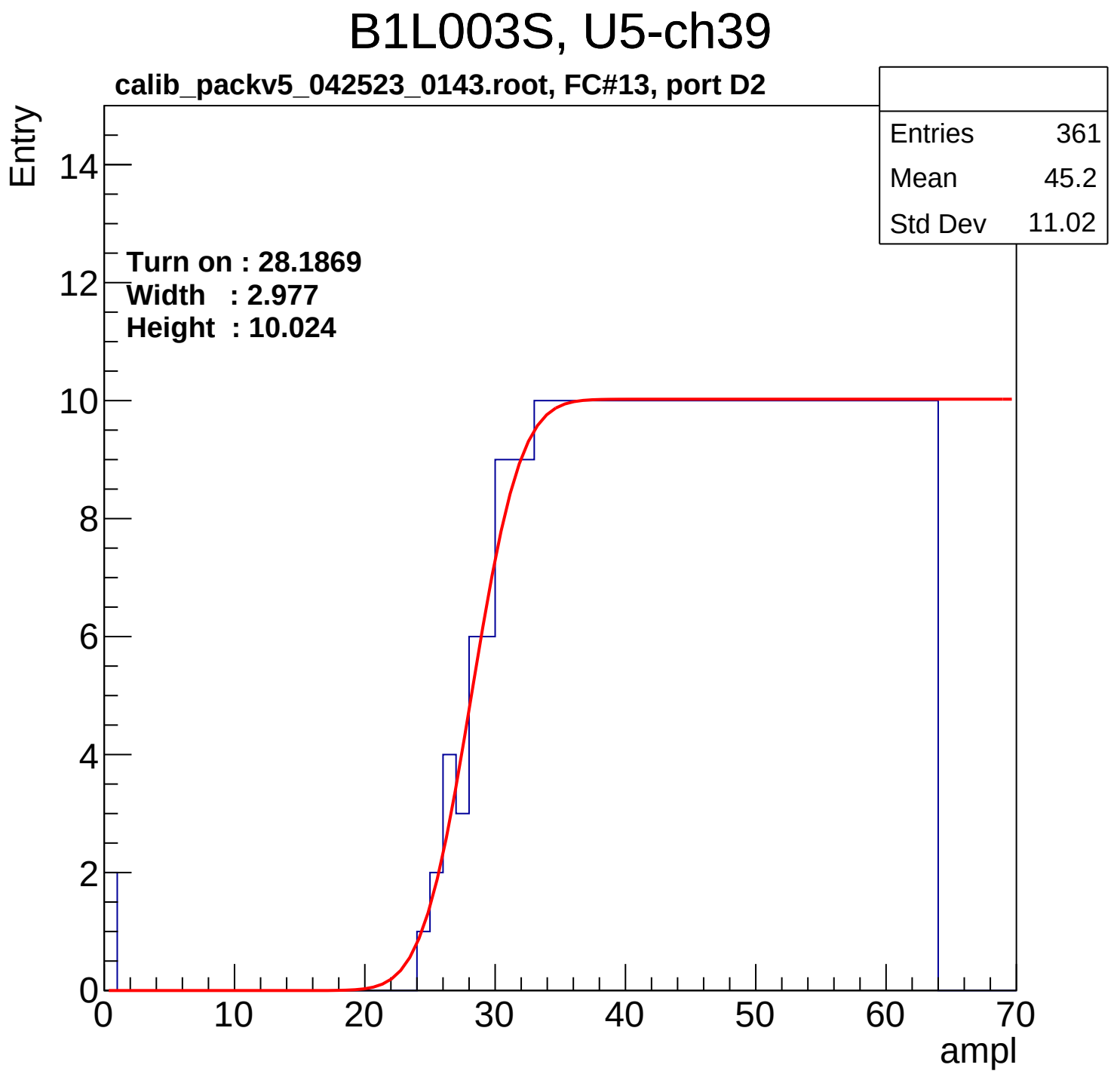
B1L003S, U5-ch39
calib_packv5_042523_0143.root, FC#13, port D2
Entries 361
Mean 45.2
Std Dev 11.02
Turn on : 28.1869
Width : 2.977
Height : 10.024
Entry
ampl
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6
8
10
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0
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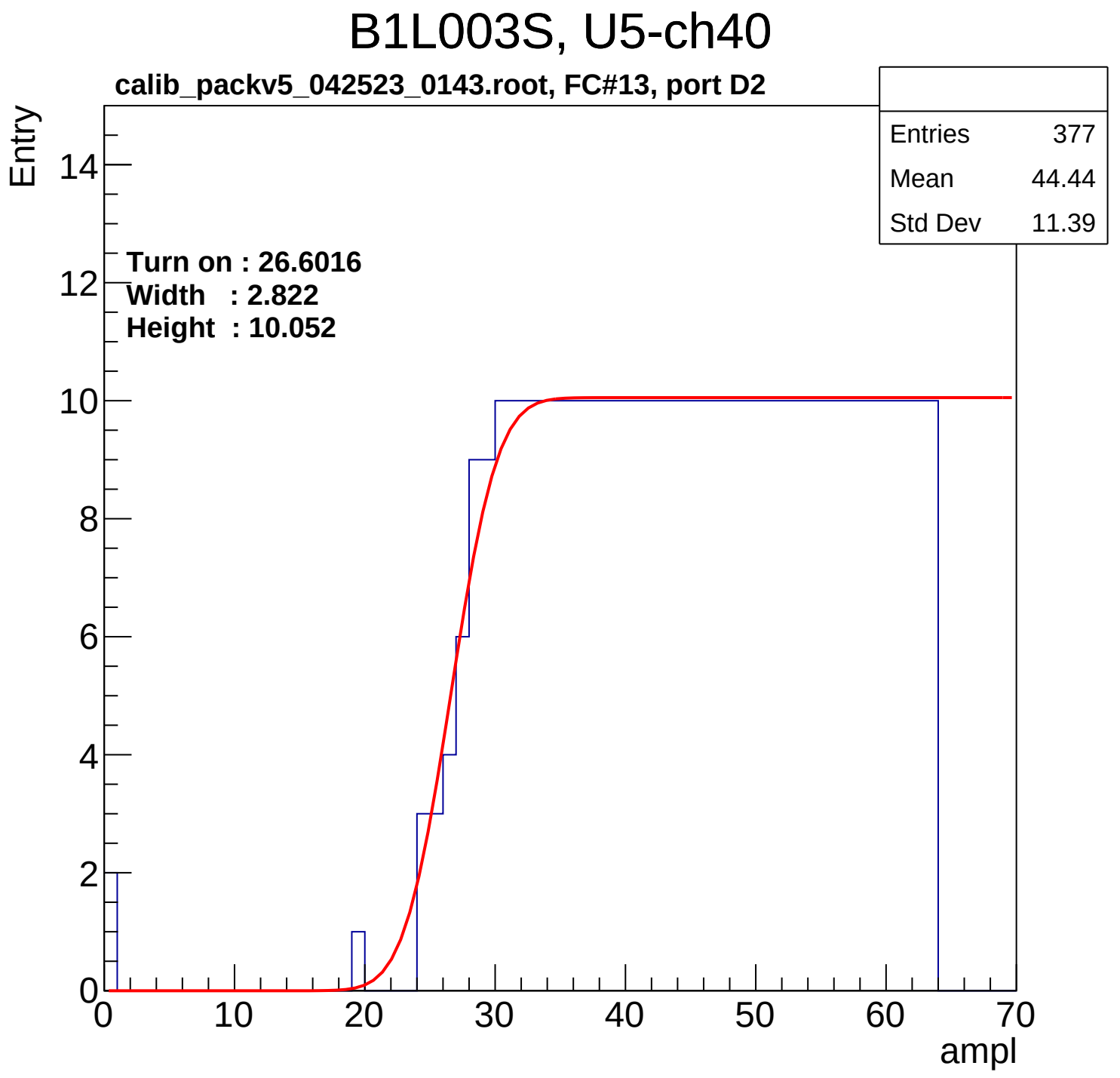
B1L003S, U5-ch40
calib_packv5_042523_0143.root, FC#13, port D2
Entries 377
Mean 44.44
Std Dev 11.39
Turn on : 26.6016
Width : 2.822
Height : 10.052
Entry
ampl
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2
4
6
8
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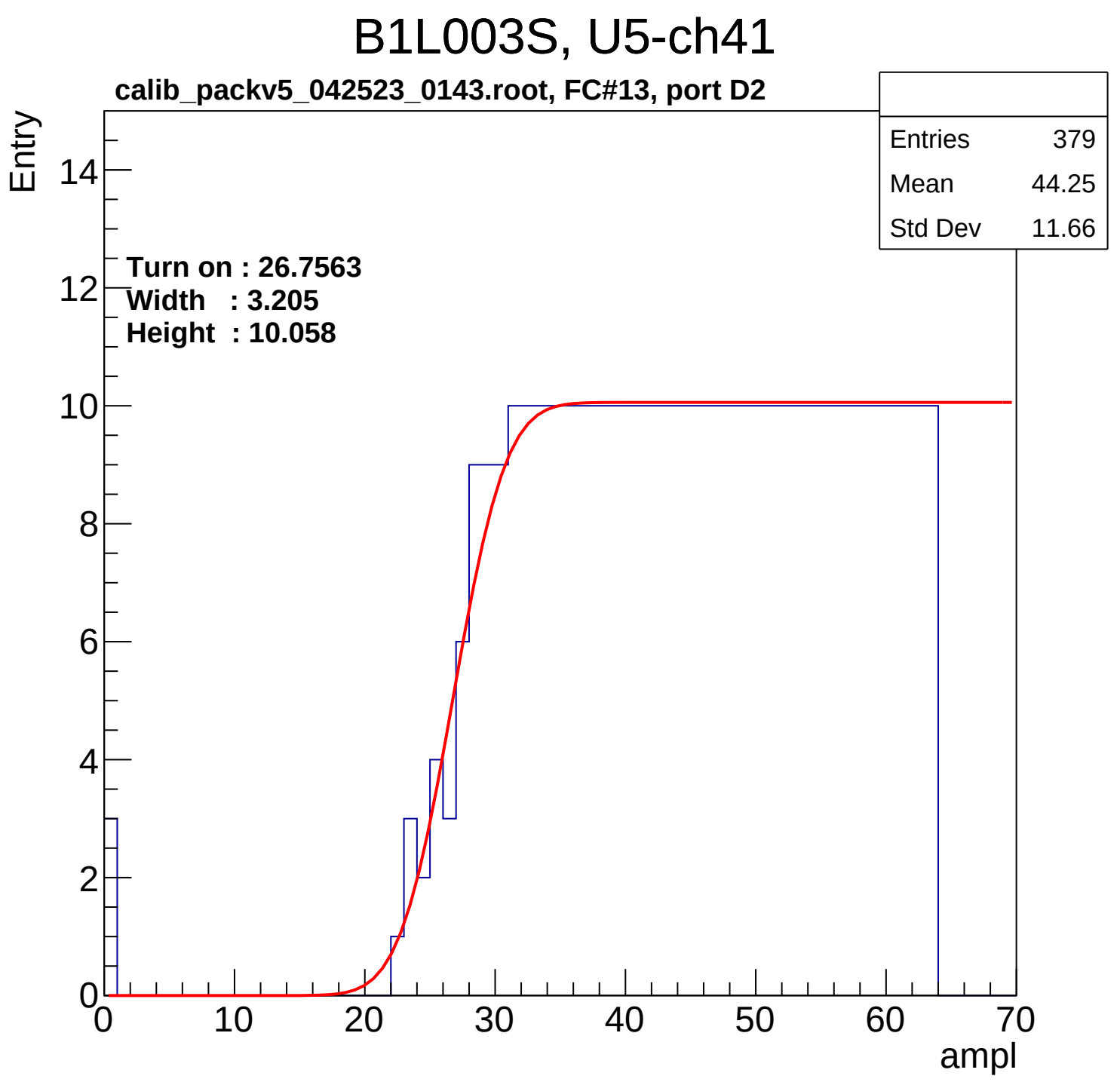
B1L003S, U5-ch41
calib_packv5_042523_0143.root, FC#13, port D2
Entries 379
Mean 44.25
Std Dev 11.66
Turn on : 26.7563
Width : 3.205
Height : 10.058
Entry
ampl
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6
8
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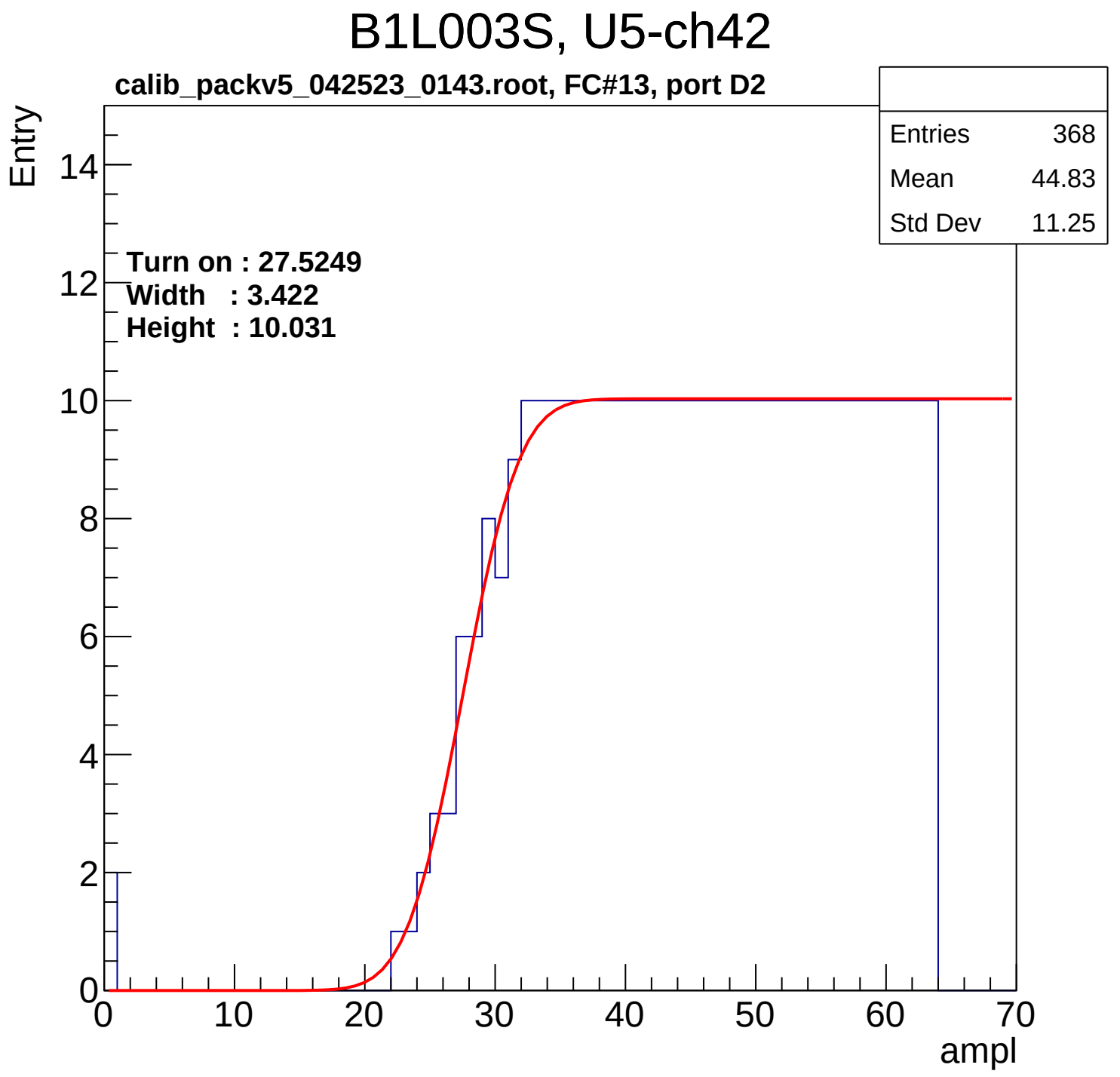
B1L003S, U5-ch42
calib_packv5_042523_0143.root, FC#13, port D2
Entries 368
Mean 44.83
Std Dev 11.25
Turn on : 27.5249
Width : 3.422
Height : 10.031
Entry
ampl
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4
6
8
10
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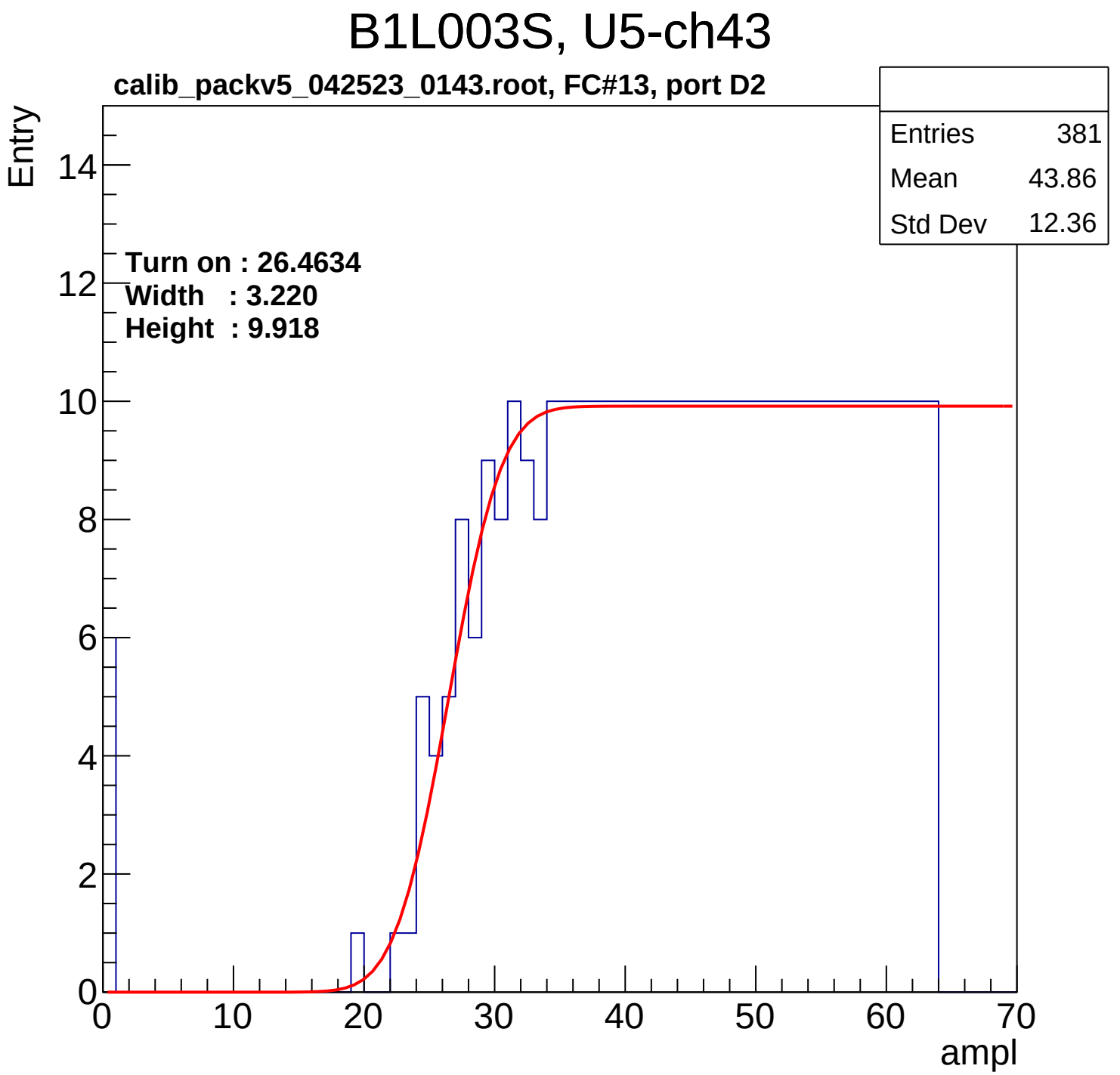
B1L003S, U5-ch43
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 43.86
Std Dev 12.36
Turn on : 26.4634
Width : 3.220
Height : 9.918
Entry
ampl
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6
8
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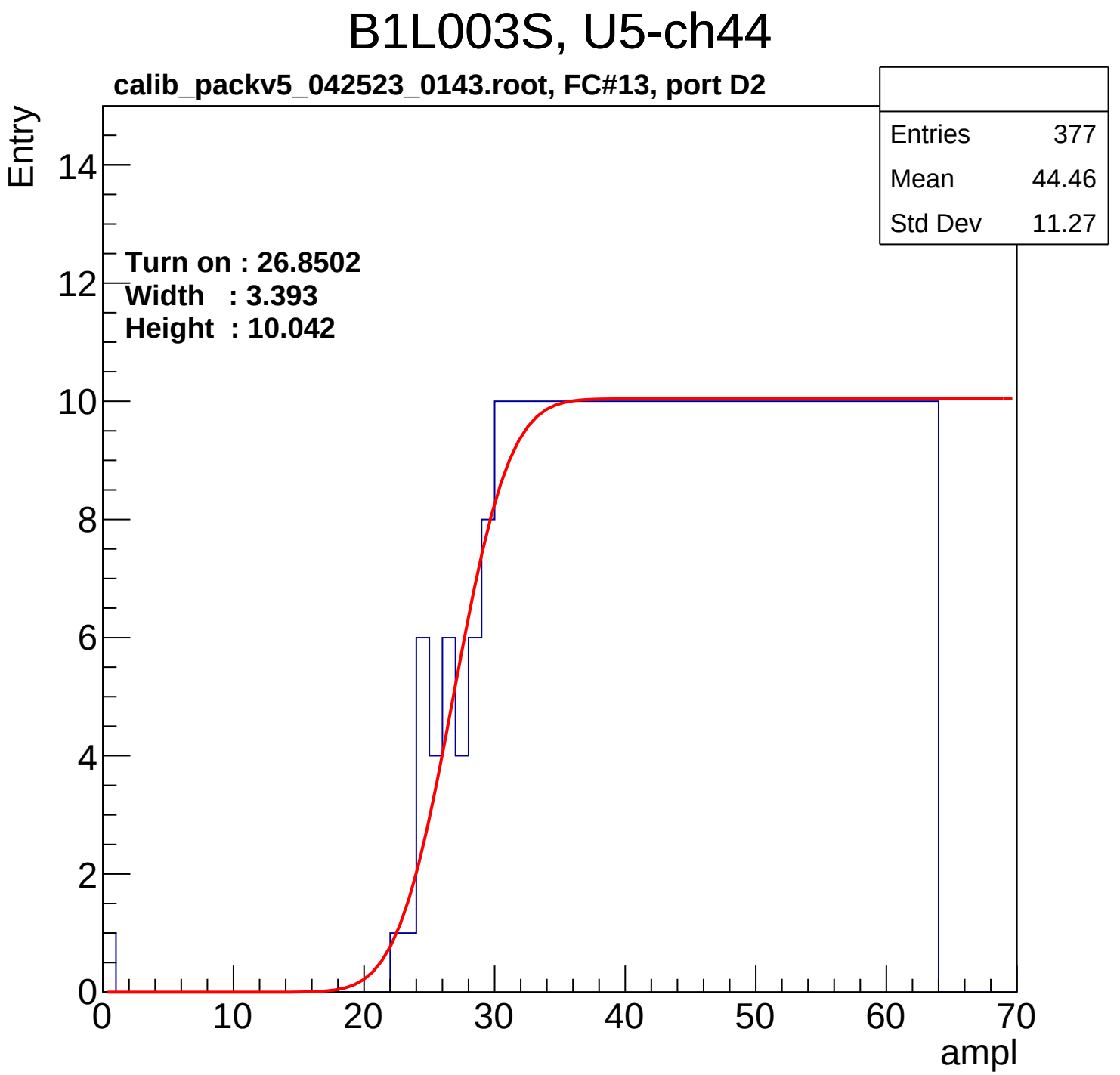
B1L003S, U5-ch44
calib_packv5_042523_0143.root, FC#13, port D2
Entries 377
Mean 44.46
Std Dev 11.27
Turn on : 26.8502
Width : 3.393
Height : 10.042
Entry
ampl
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4
6
8
10
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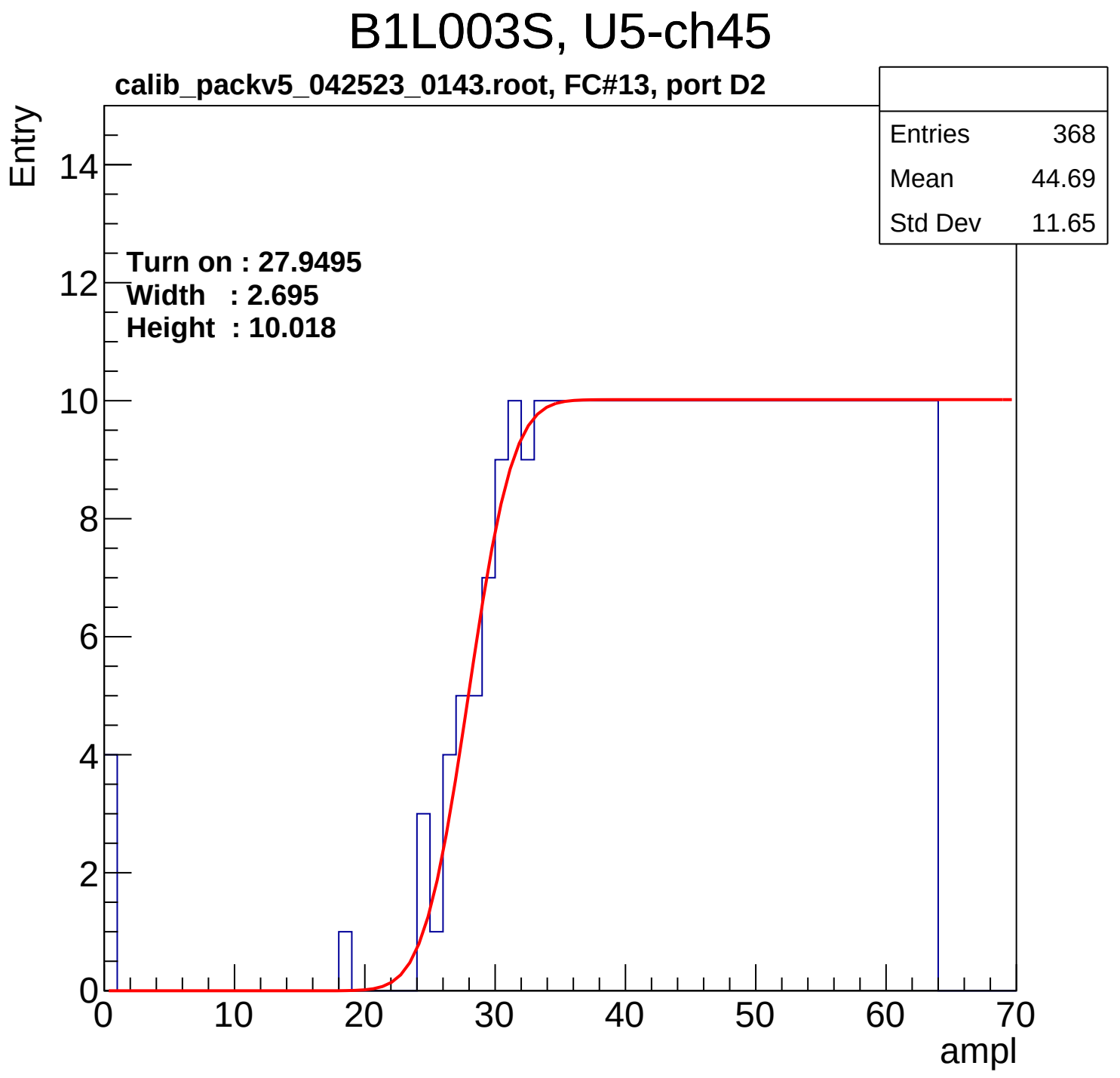
B1L003S, U5-ch45
calib_packv5_042523_0143.root, FC#13, port D2
Entries 368
Mean 44.69
Std Dev 11.65
Turn on : 27.9495
Width : 2.695
Height : 10.018
Entry
ampl
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8
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0
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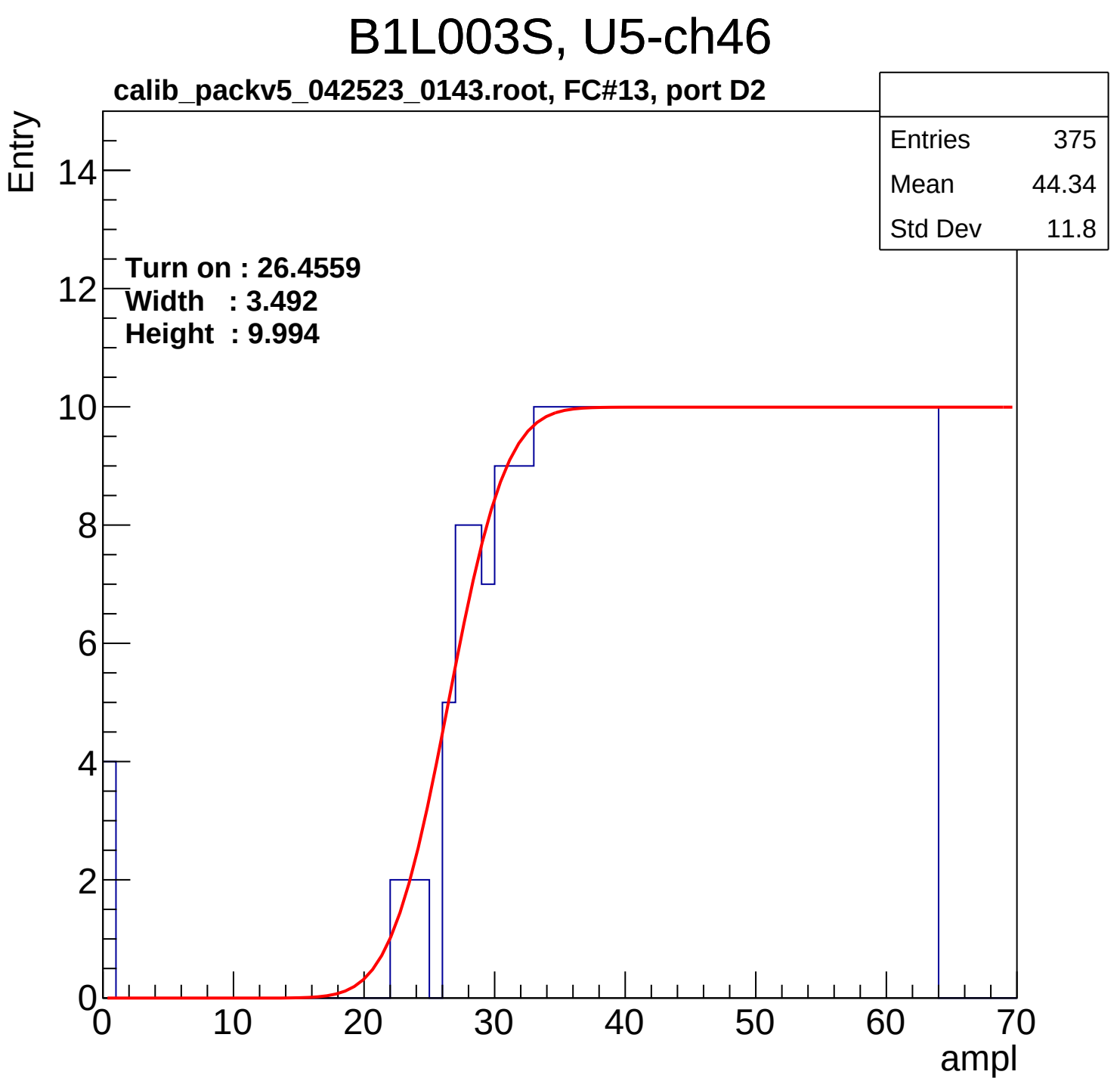
B1L003S, U5-ch46
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.34
Std Dev 11.8
Turn on : 26.4559
Width : 3.492
Height : 9.994
Entry
ampl
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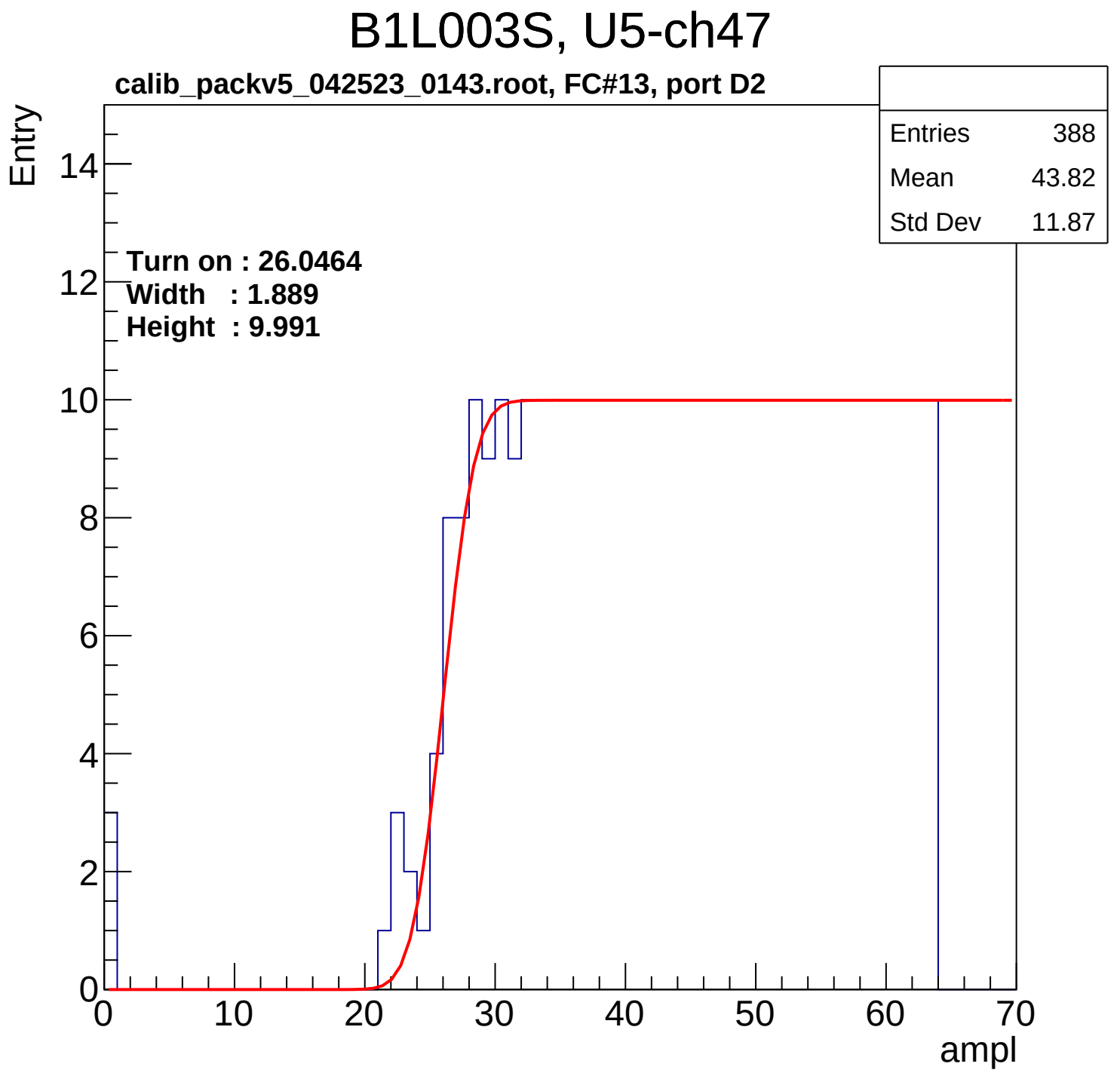
B1L003S, U5-ch47
calib_packv5_042523_0143.root, FC#13, port D2
Entries 388
Mean 43.82
Std Dev 11.87
Turn on : 26.0464
Width : 1.889
Height : 9.991
Entry
ampl
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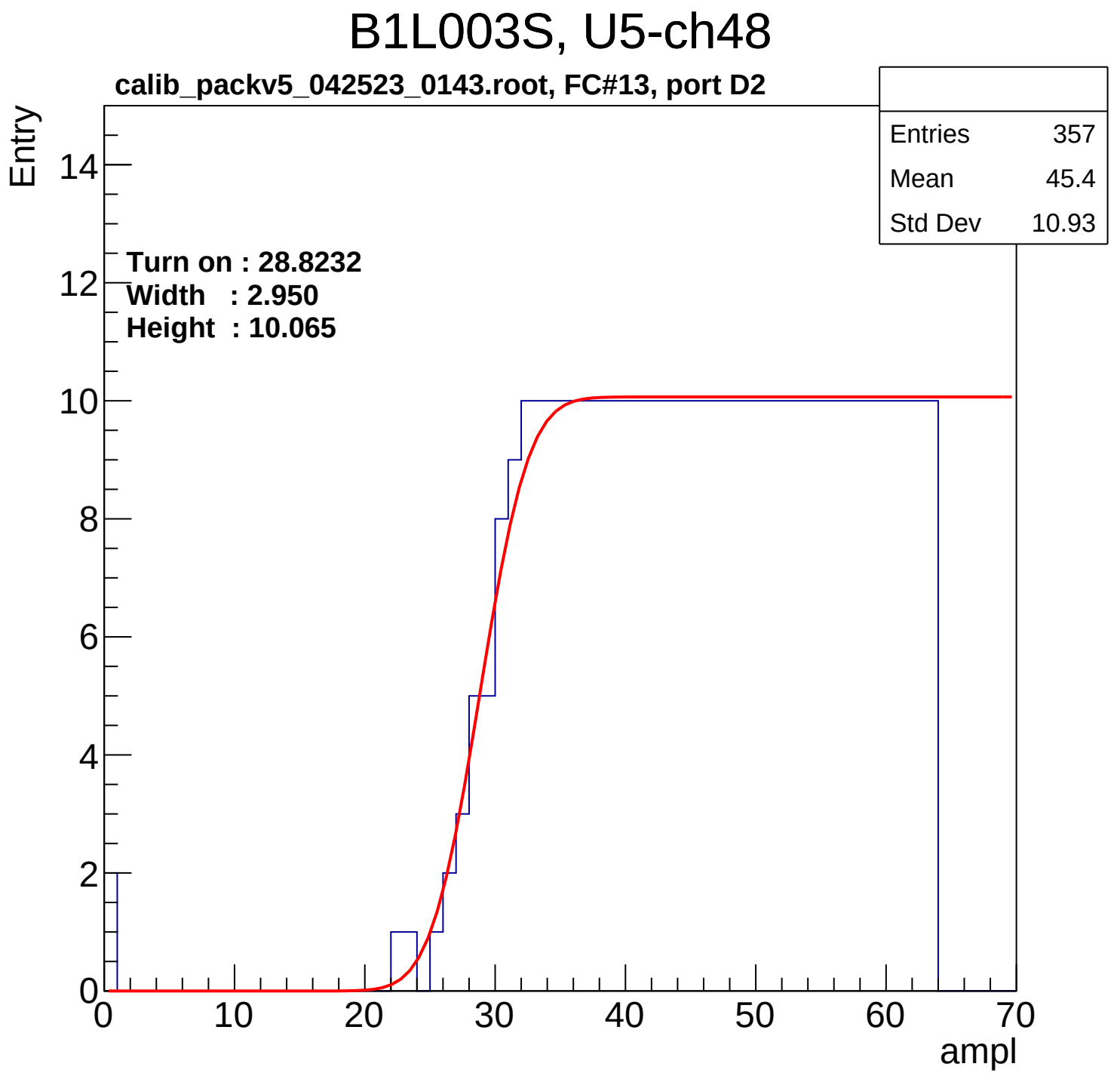
B1L003S, U5-ch48
calib_packv5_042523_0143.root, FC#13, port D2
Entries 357
Mean 45.4
Std Dev 10.93
Turn on : 28.8232
Width : 2.950
Height : 10.065
Entry
ampl
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6
8
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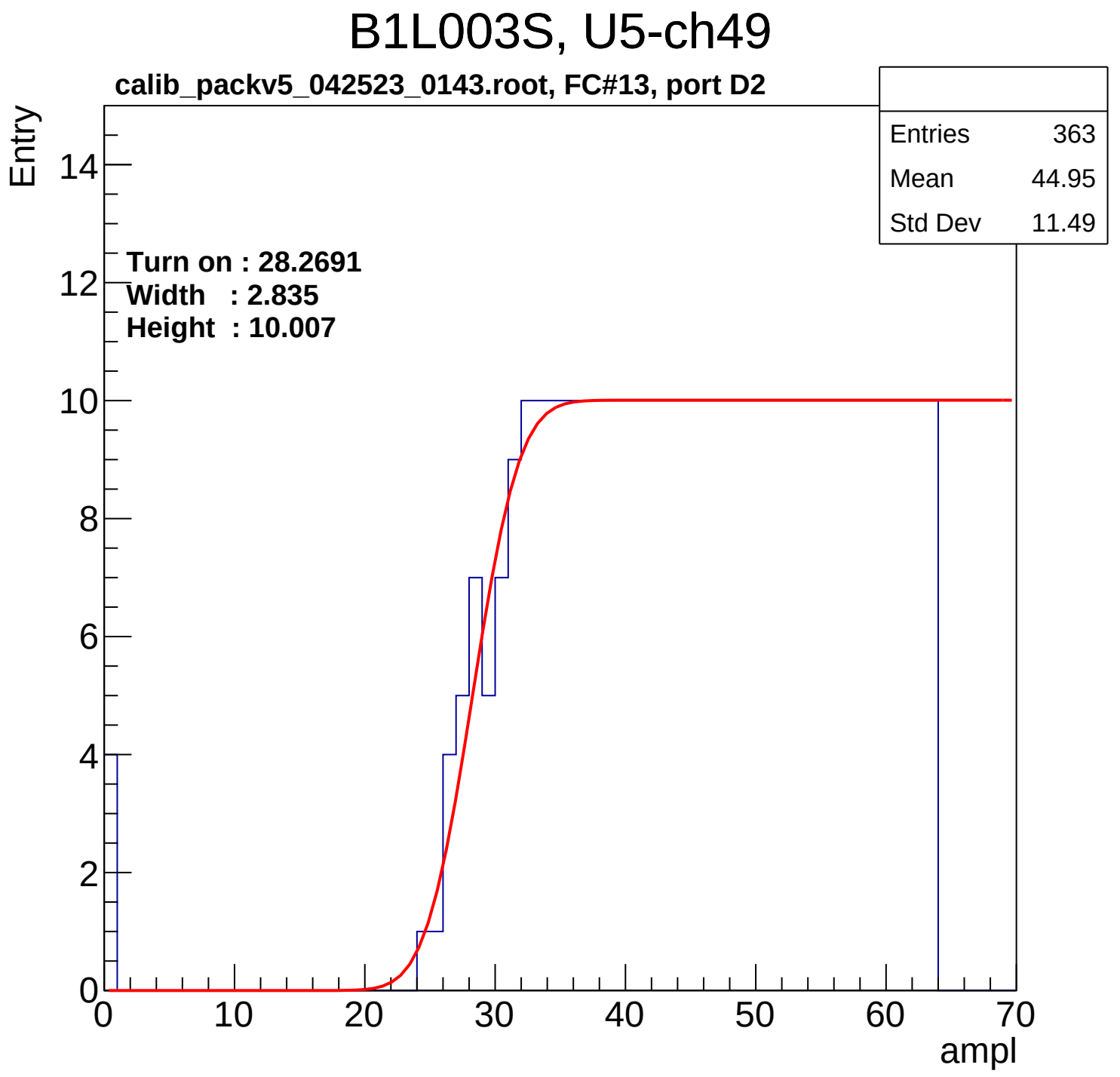
B1L003S, U5-ch49
calib_packv5_042523_0143.root, FC#13, port D2
Entries 363
Mean 44.95
Std Dev 11.49
Turn on : 28.2691
Width : 2.835
Height : 10.007
Entry
ampl
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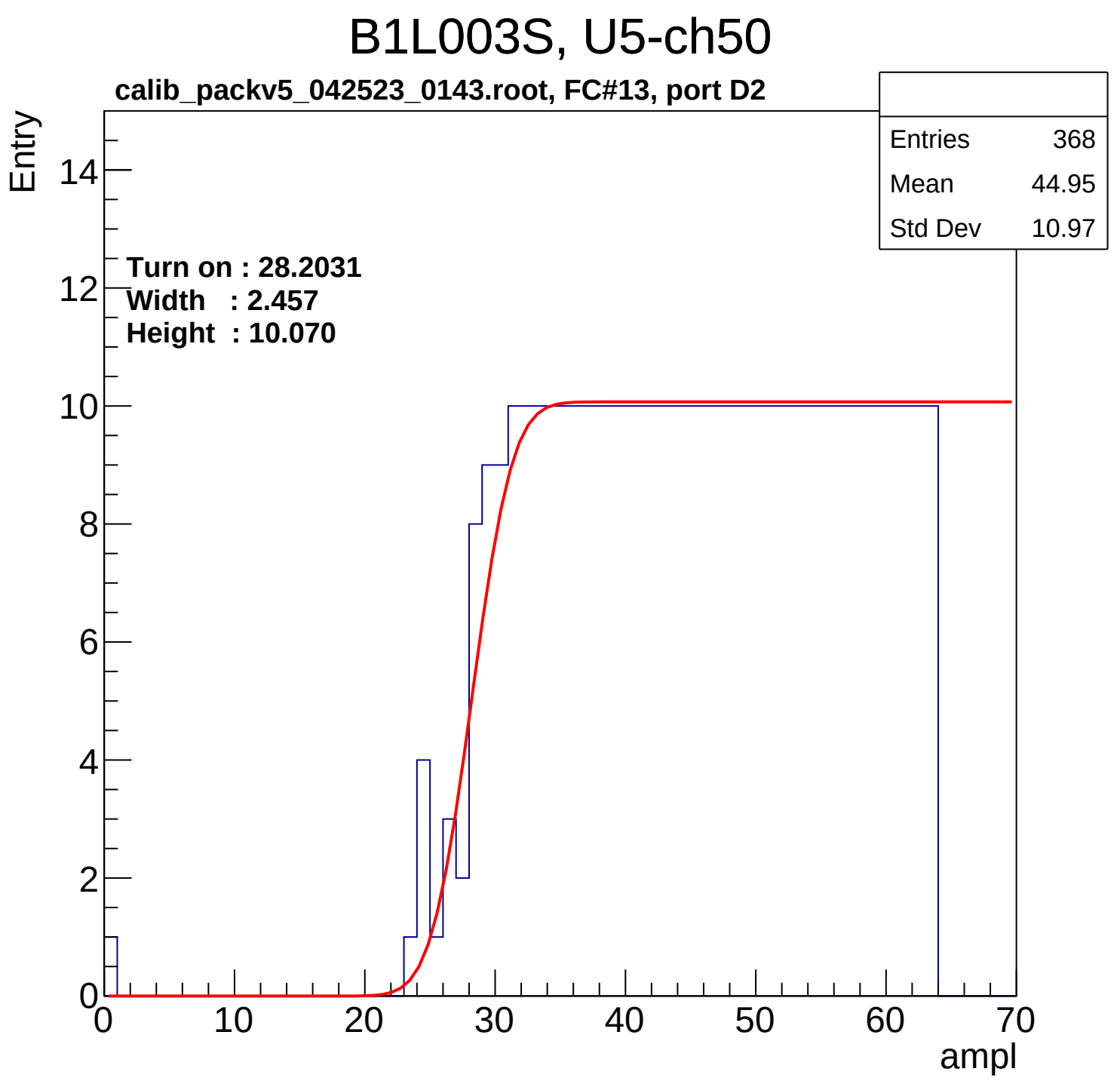
B1L003S, U5-ch50
calib_packv5_042523_0143.root, FC#13, port D2
Entries 368
Mean 44.95
Std Dev 10.97
Turn on : 28.2031
Width : 2.457
Height : 10.070
Entry
ampl
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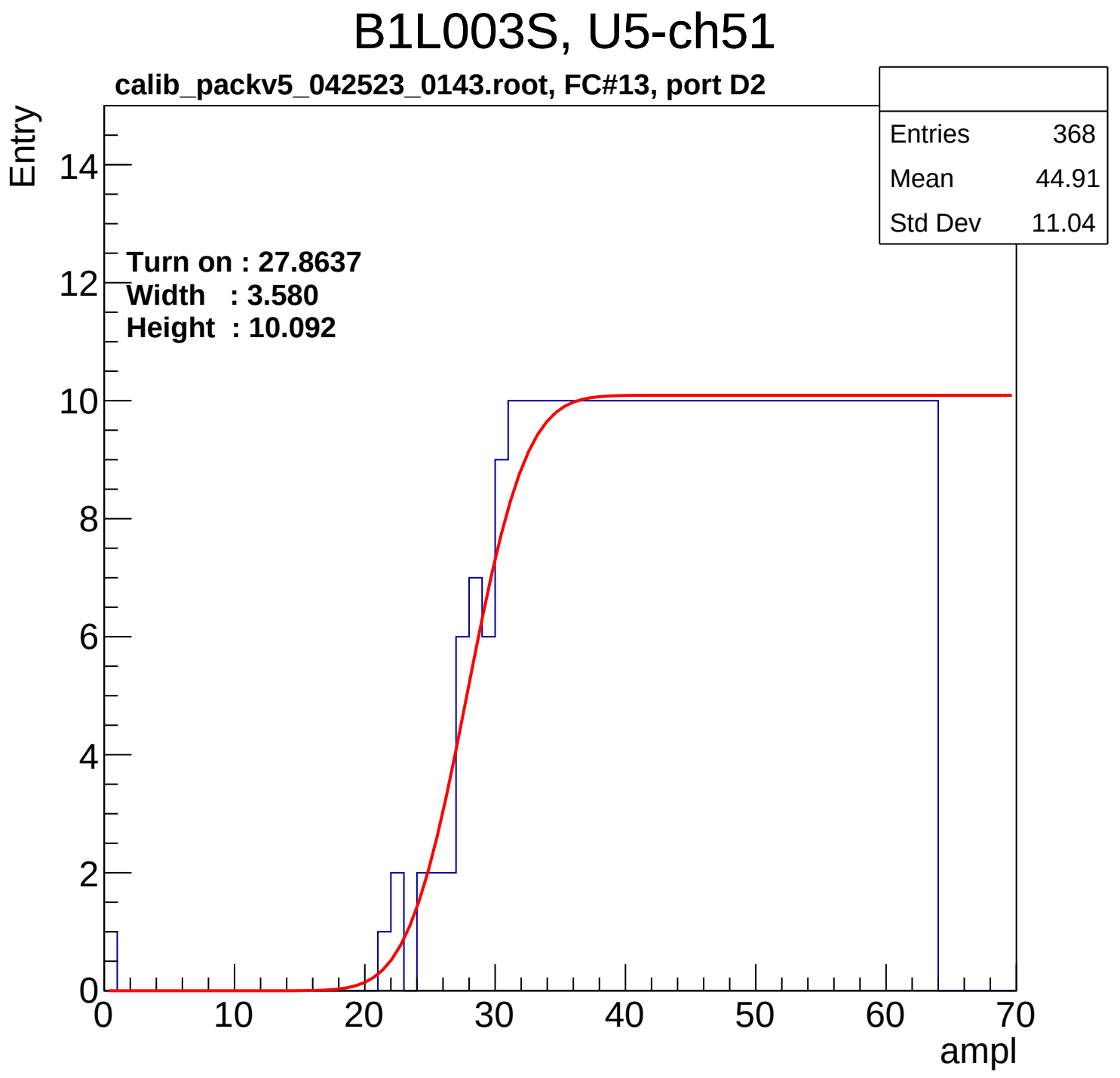
B1L003S, U5-ch51
calib_packv5_042523_0143.root, FC#13, port D2
Entries 368
Mean 44.91
Std Dev 11.04
Turn on : 27.8637
Width : 3.580
Height : 10.092
Entry
ampl
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2
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6
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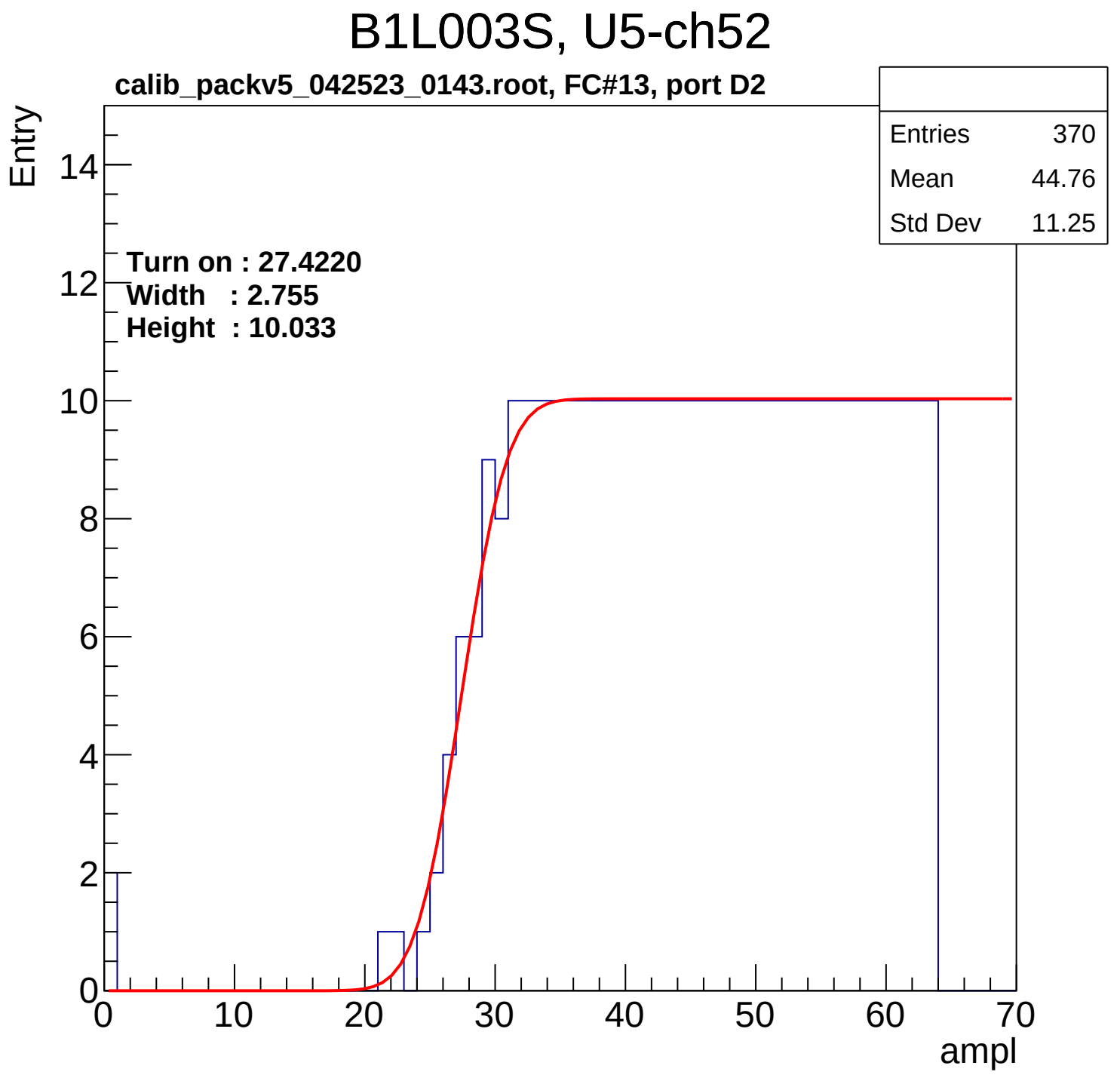
B1L003S, U5-ch52
calib_packv5_042523_0143.root, FC#13, port D2
Entries 370
Mean 44.76
Std Dev 11.25
Turn on : 27.4220
Width : 2.755
Height : 10.033
Entry
ampl
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4
6
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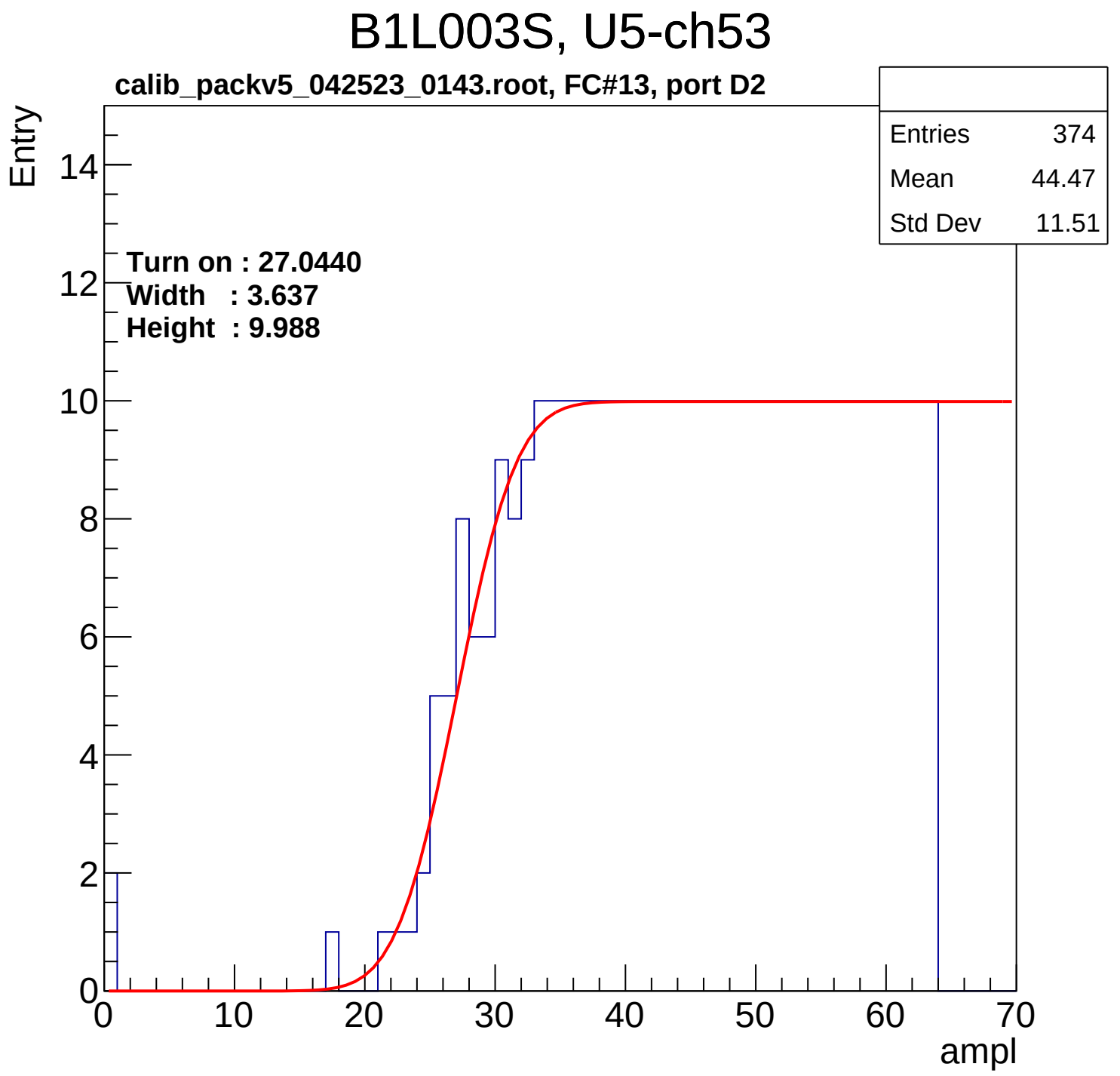
B1L003S, U5-ch53
calib_packv5_042523_0143.root, FC#13, port D2
Entries 374
Mean 44.47
Std Dev 11.51
Turn on : 27.0440
Width : 3.637
Height : 9.988
Entry
ampl
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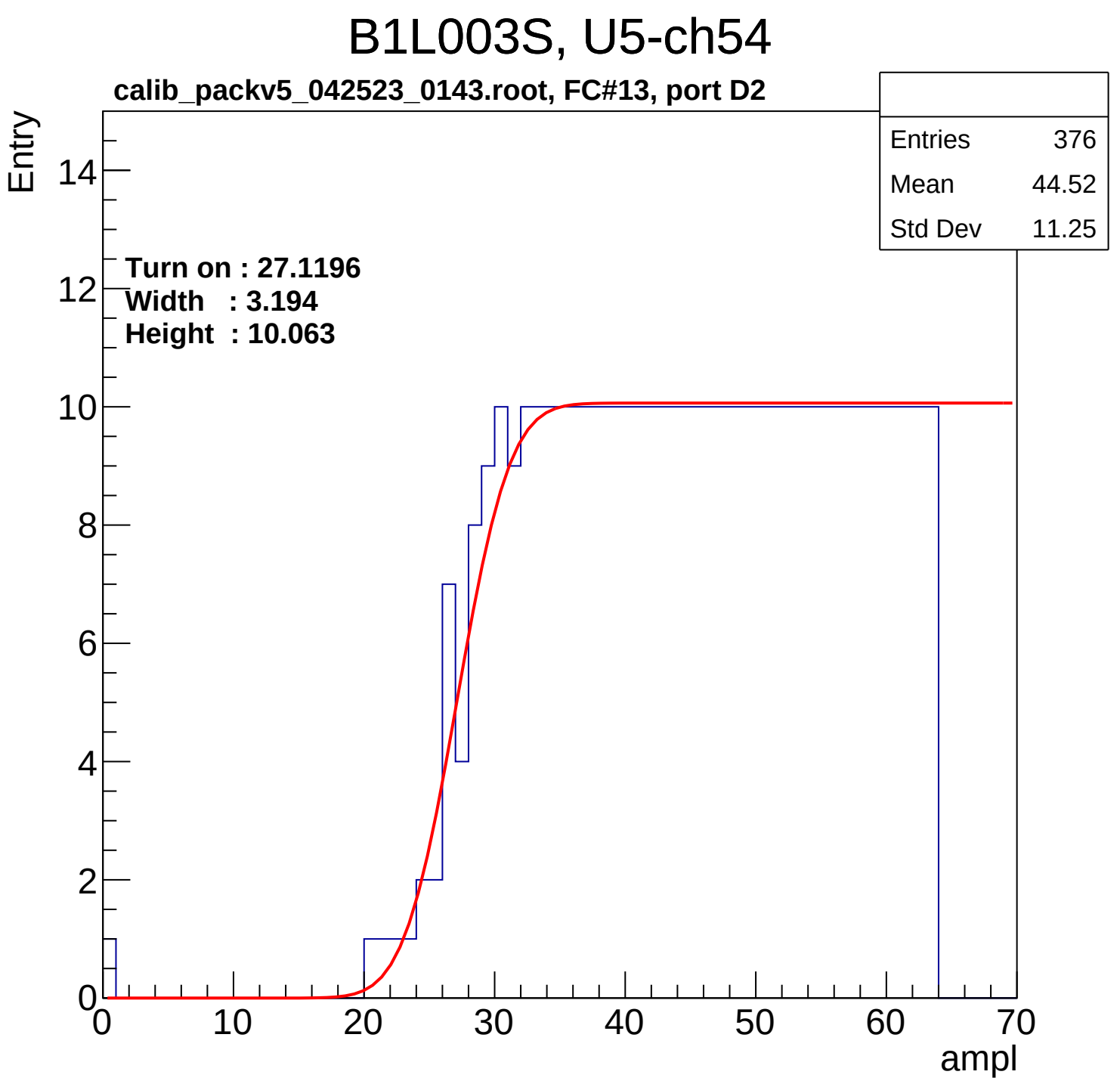
B1L003S, U5-ch54
calib_packv5_042523_0143.root, FC#13, port D2
Entries 376
Mean 44.52
Std Dev 11.25
Turn on : 27.1196
Width : 3.194
Height : 10.063
Entry
ampl
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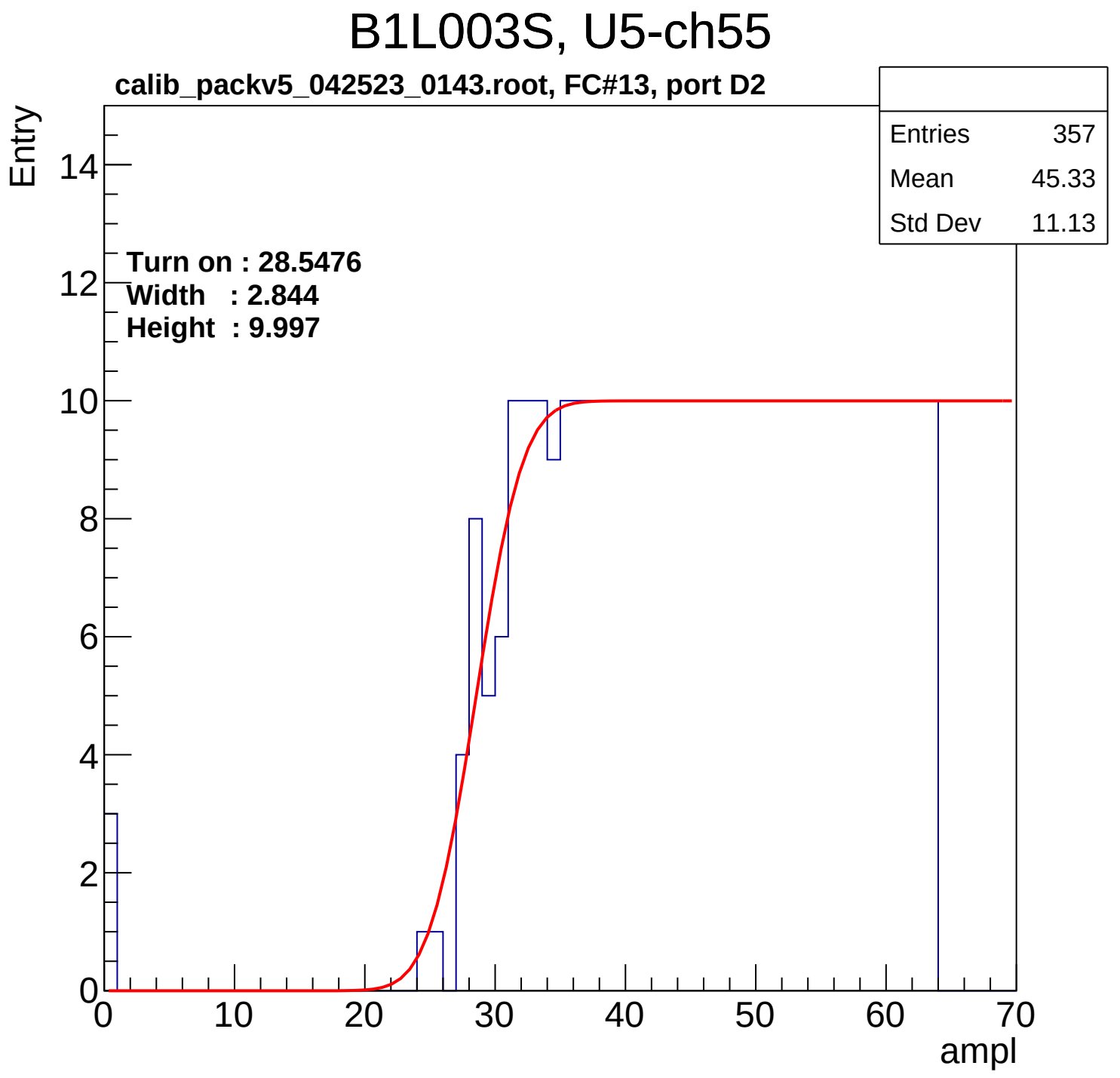
B1L003S, U5-ch55
calib_packv5_042523_0143.root, FC#13, port D2
Entries 357
Mean 45.33
Std Dev 11.13
Turn on : 28.5476
Width : 2.844
Height : 9.997
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ampl
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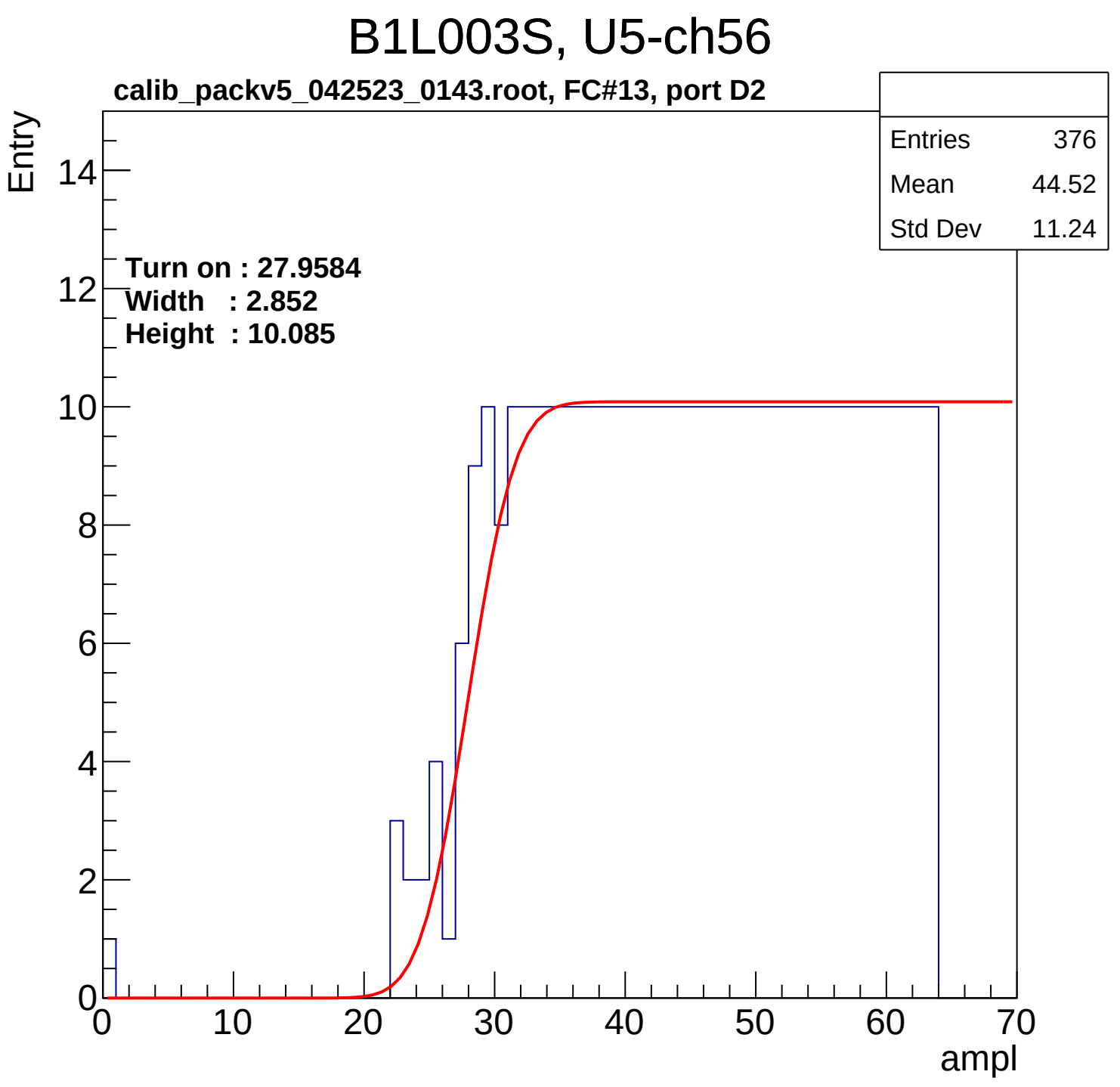
B1L003S, U5-ch56
calib_packv5_042523_0143.root, FC#13, port D2
Entries 376
Mean 44.52
Std Dev 11.24
Turn on : 27.9584
Width : 2.852
Height : 10.085
Entry
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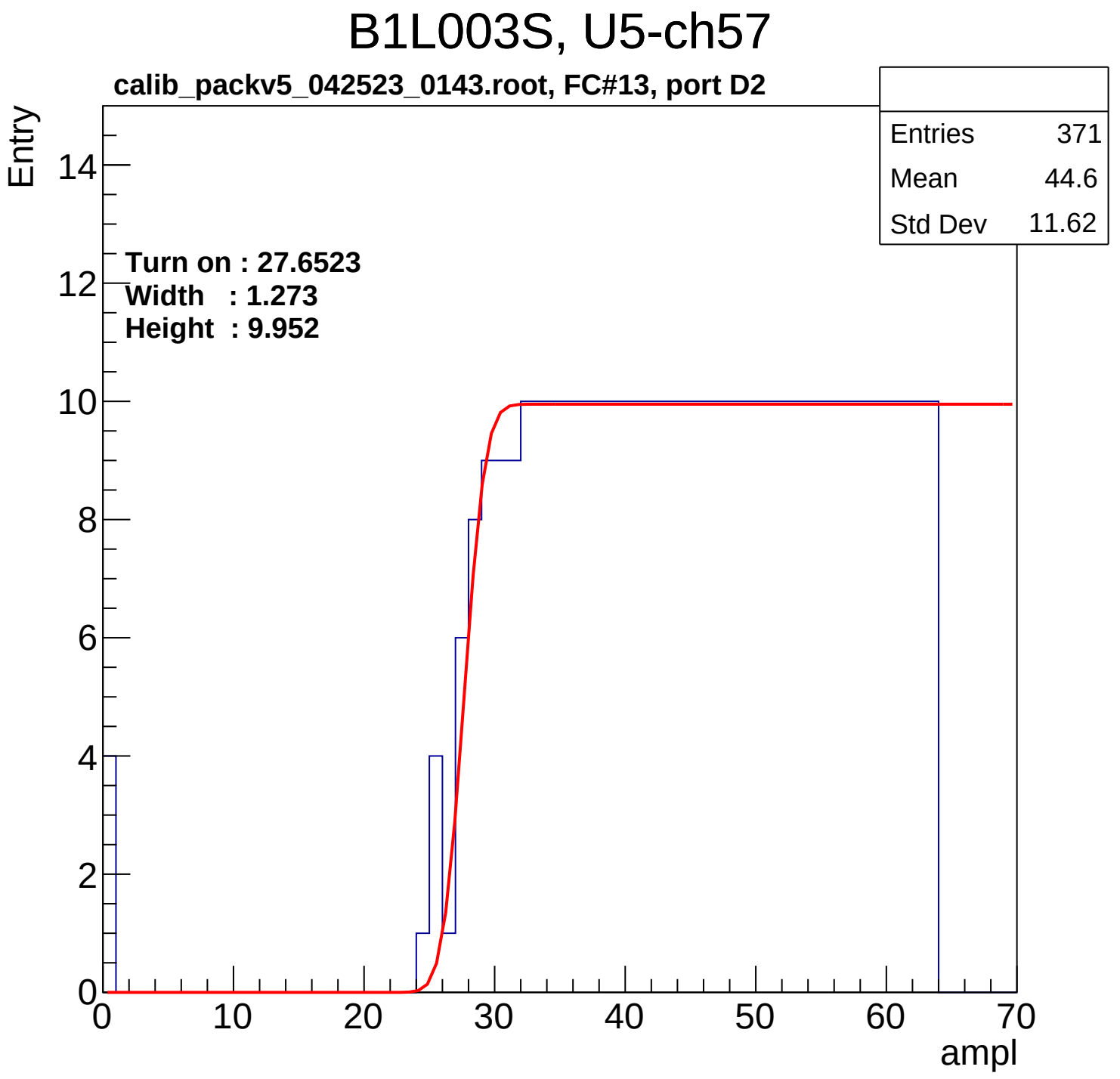
B1L003S, U5-ch57
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.6
Std Dev 11.62
Turn on : 27.6523
Width : 1.273
Height : 9.952
Entry
ampl
0
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4
6
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12
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20
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40
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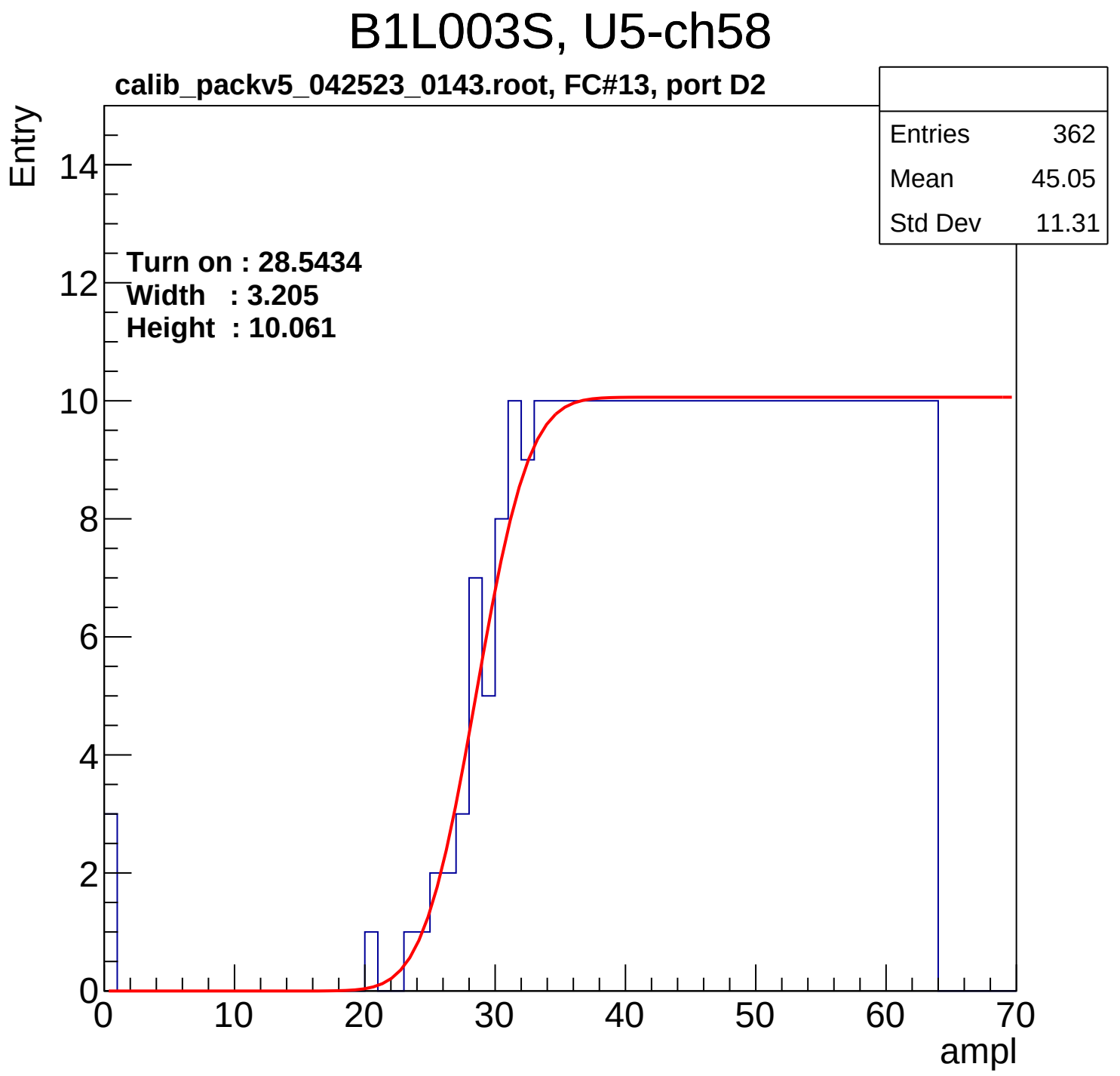
B1L003S, U5-ch58
calib_packv5_042523_0143.root, FC#13, port D2
Entries 362
Mean 45.05
Std Dev 11.31
Turn on : 28.5434
Width : 3.205
Height : 10.061
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ampl
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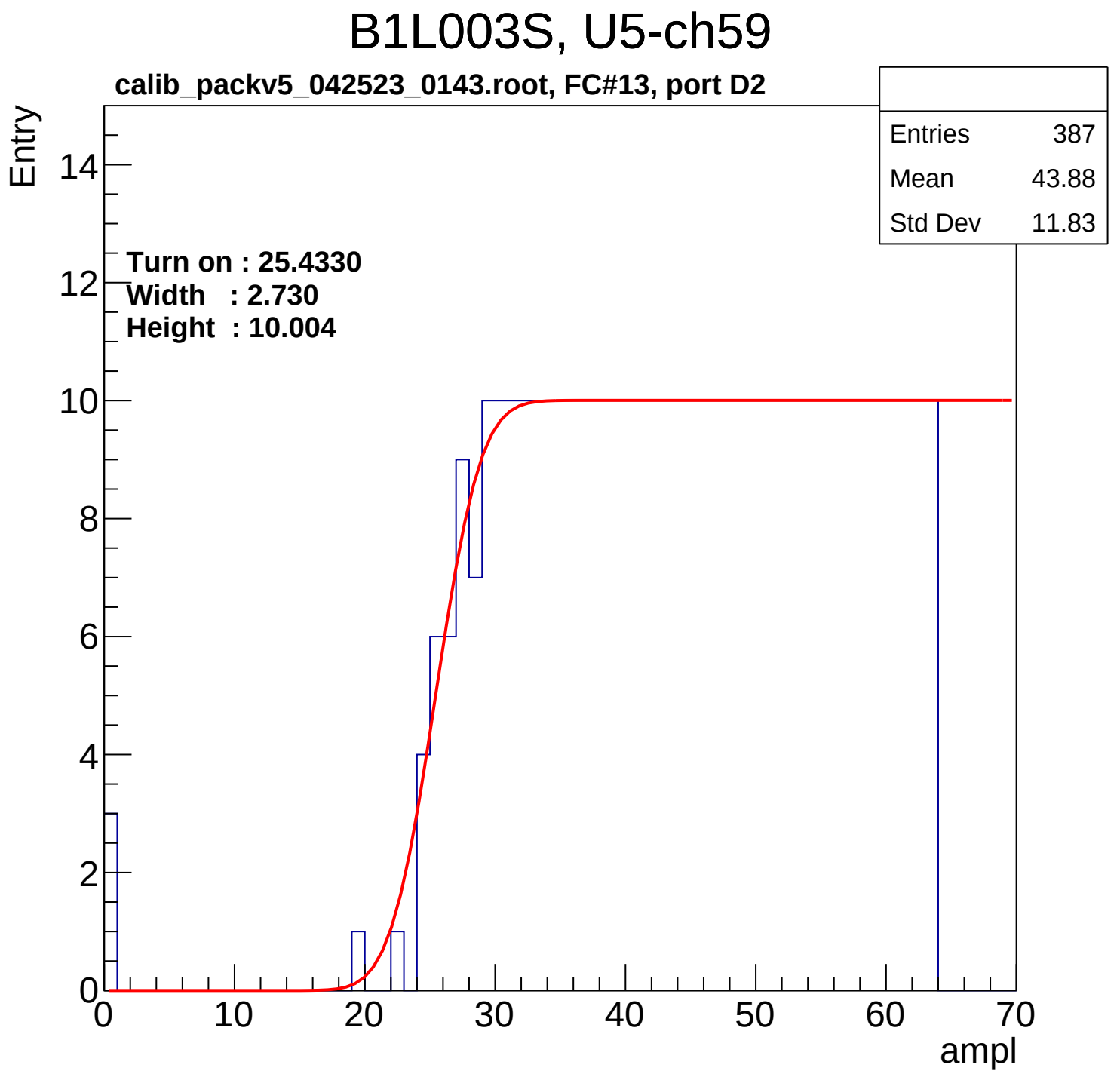
B1L003S, U5-ch59
calib_packv5_042523_0143.root, FC#13, port D2
Entries 387
Mean 43.88
Std Dev 11.83
Turn on : 25.4330
Width : 2.730
Height : 10.004
Entry
ampl
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2
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6
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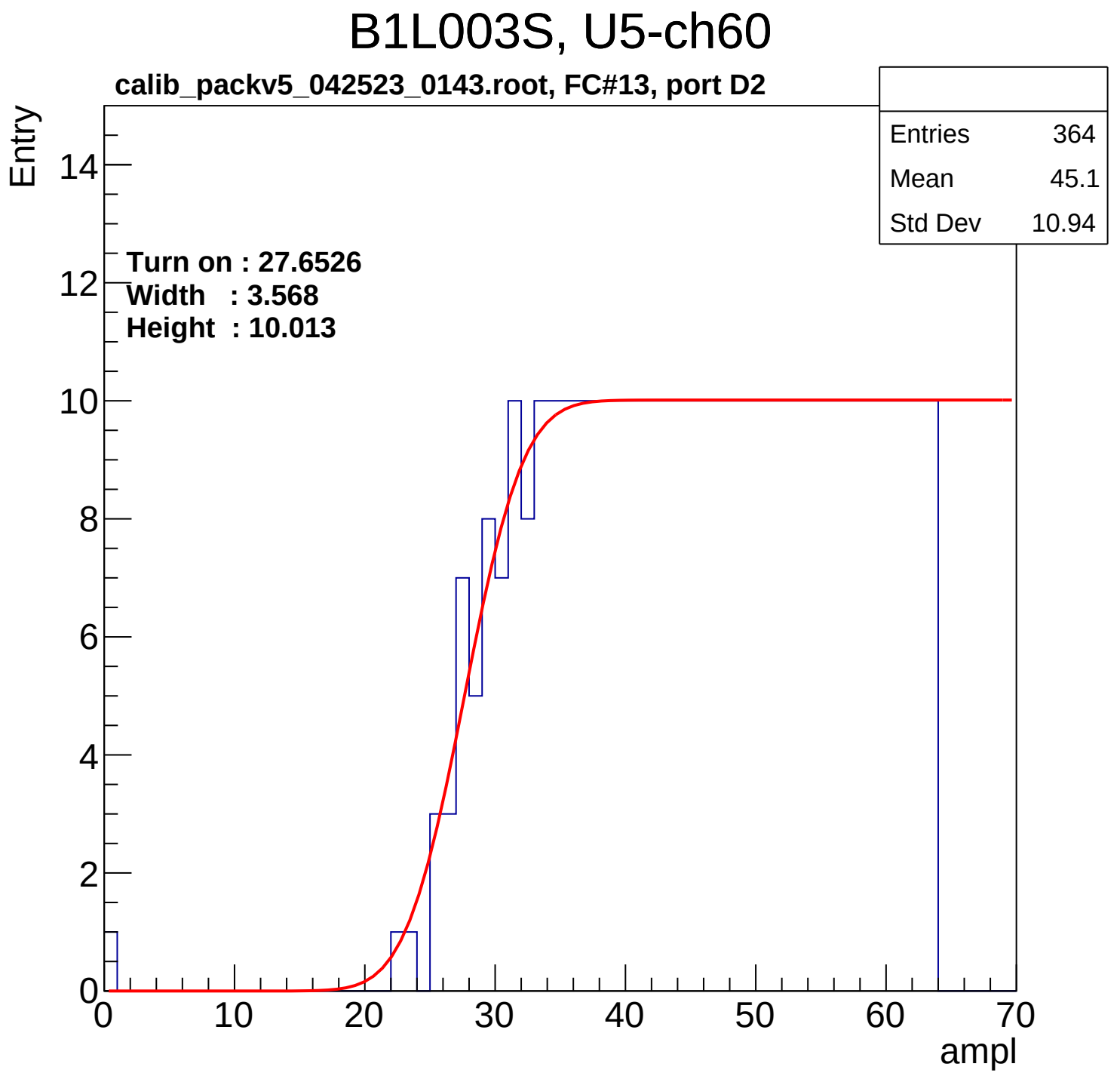
B1L003S, U5-ch60
calib_packv5_042523_0143.root, FC#13, port D2
Entries 364
Mean 45.1
Std Dev 10.94
Turn on : 27.6526
Width : 3.568
Height : 10.013
Entry
ampl
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2
4
6
8
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0
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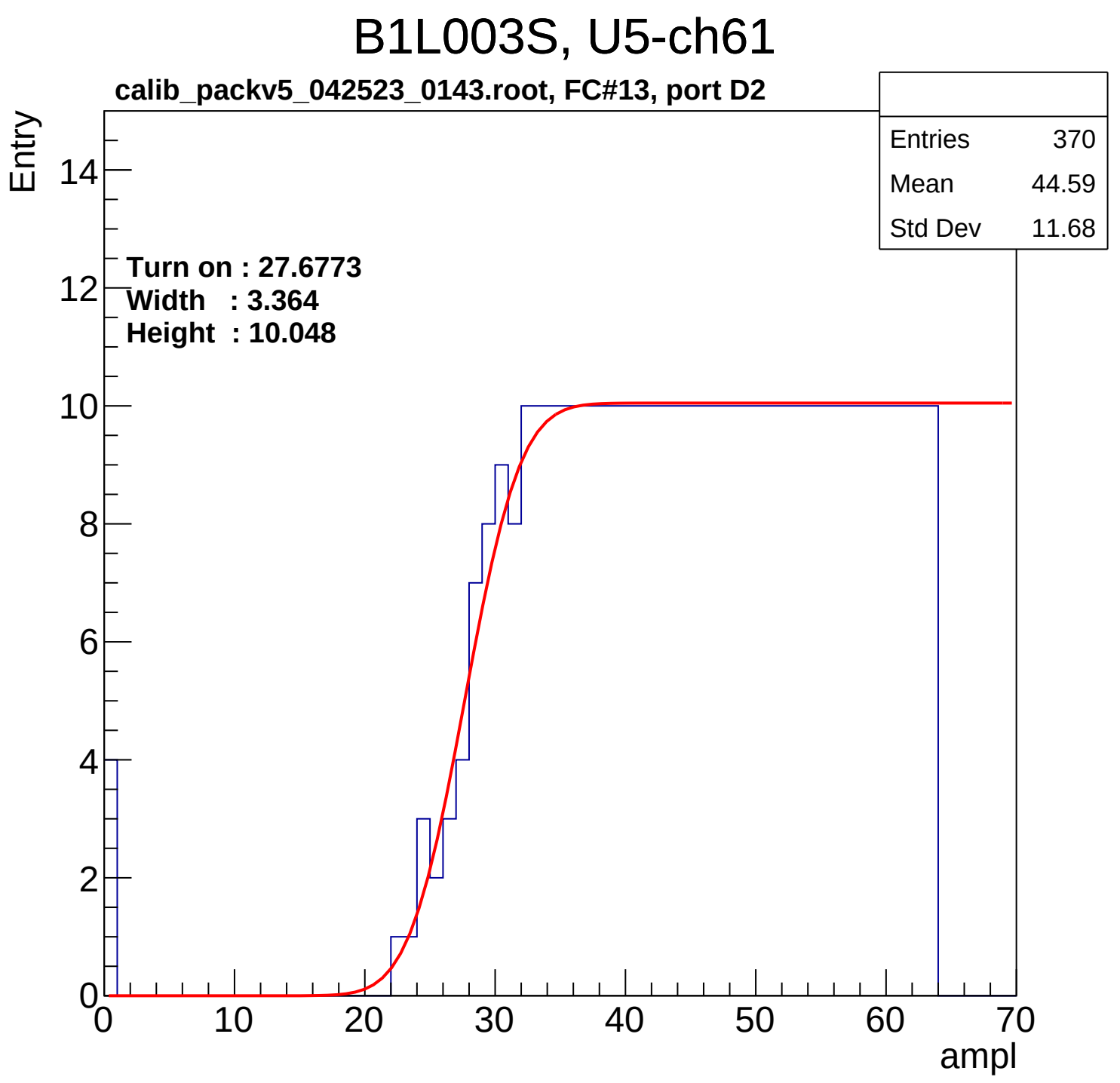
B1L003S, U5-ch61
calib_packv5_042523_0143.root, FC#13, port D2
Entries 370
Mean 44.59
Std Dev 11.68
Turn on : 27.6773
Width : 3.364
Height : 10.048
Entry
ampl
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4
6
8
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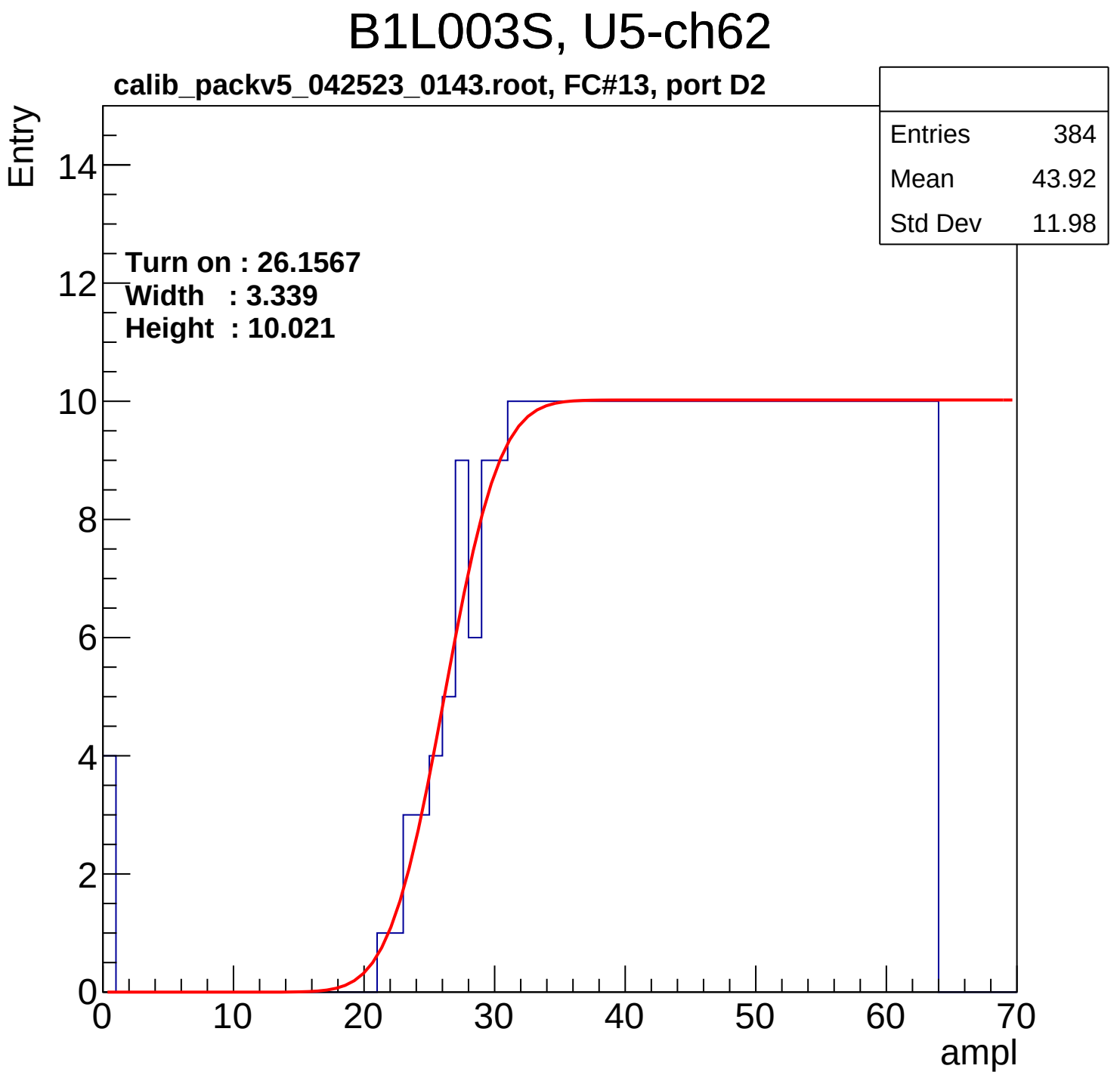
B1L003S, U5-ch62
calib_packv5_042523_0143.root, FC#13, port D2
Entries 384
Mean 43.92
Std Dev 11.98
Turn on : 26.1567
Width : 3.339
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
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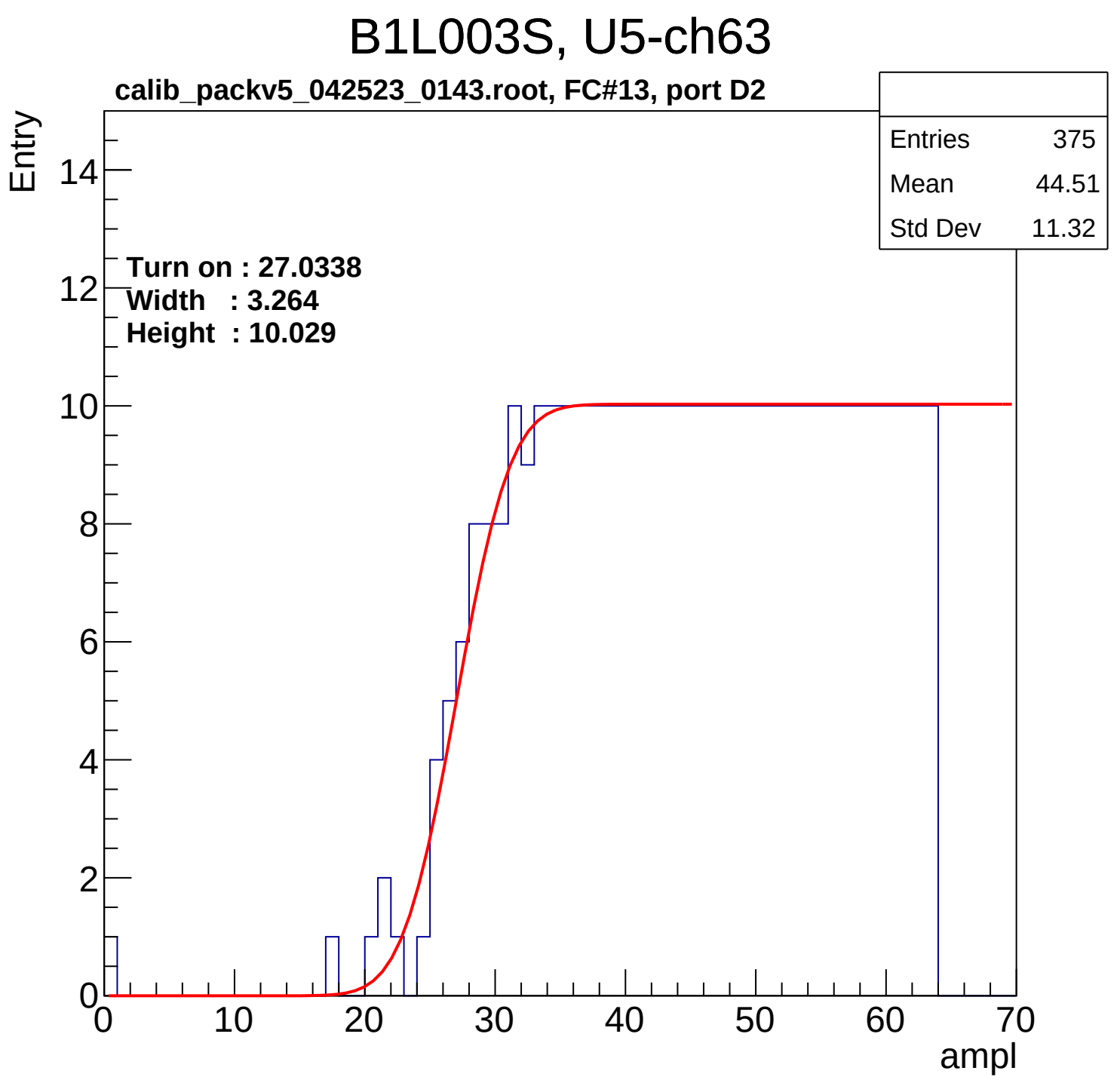
B1L003S, U5-ch63
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.51
Std Dev 11.32
Turn on : 27.0338
Width : 3.264
Height : 10.029
Entry
ampl
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6
8
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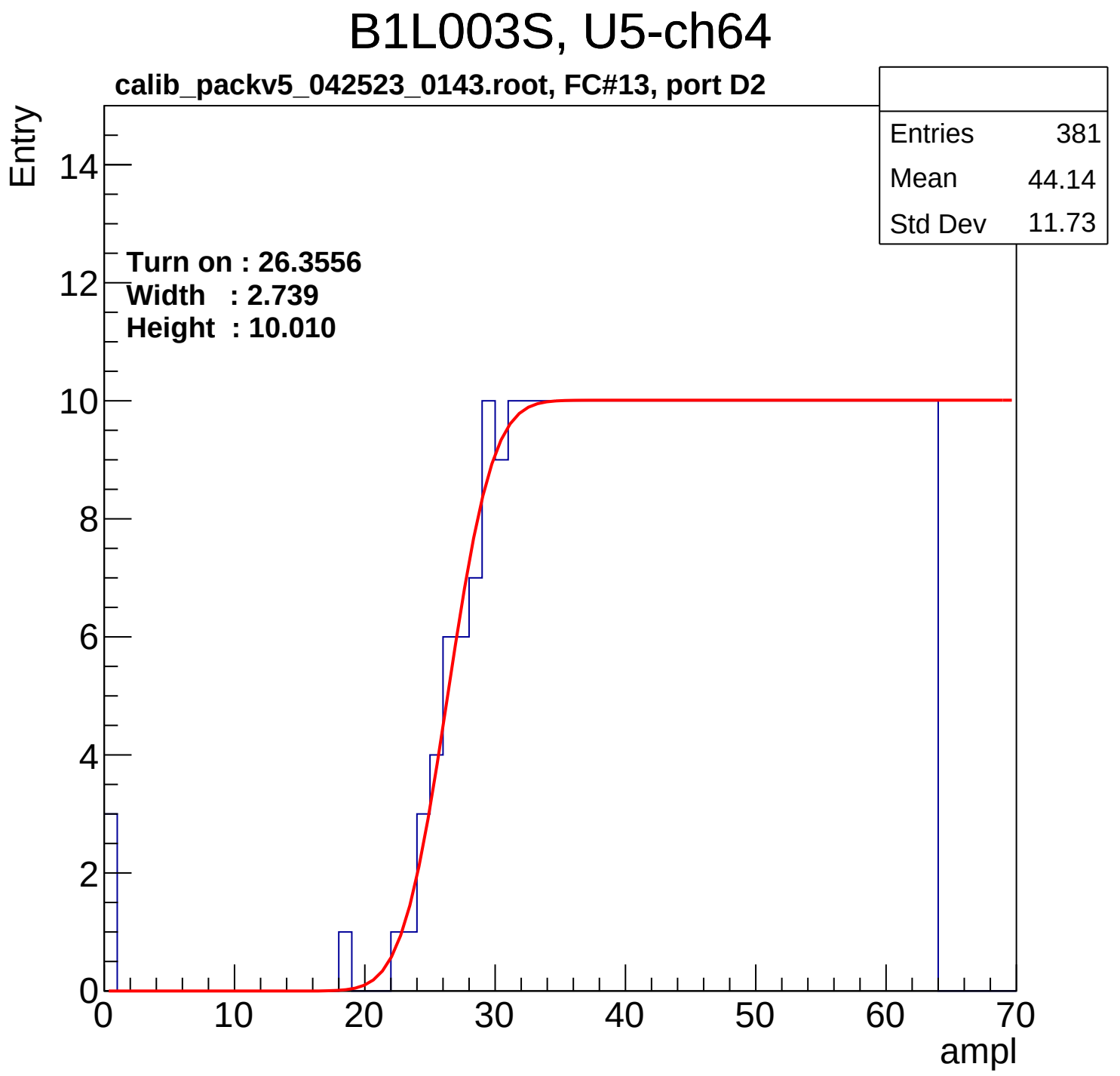
B1L003S, U5-ch64
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 44.14
Std Dev 11.73
Turn on : 26.3556
Width : 2.739
Height : 10.010
Entry
ampl
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2
4
6
8
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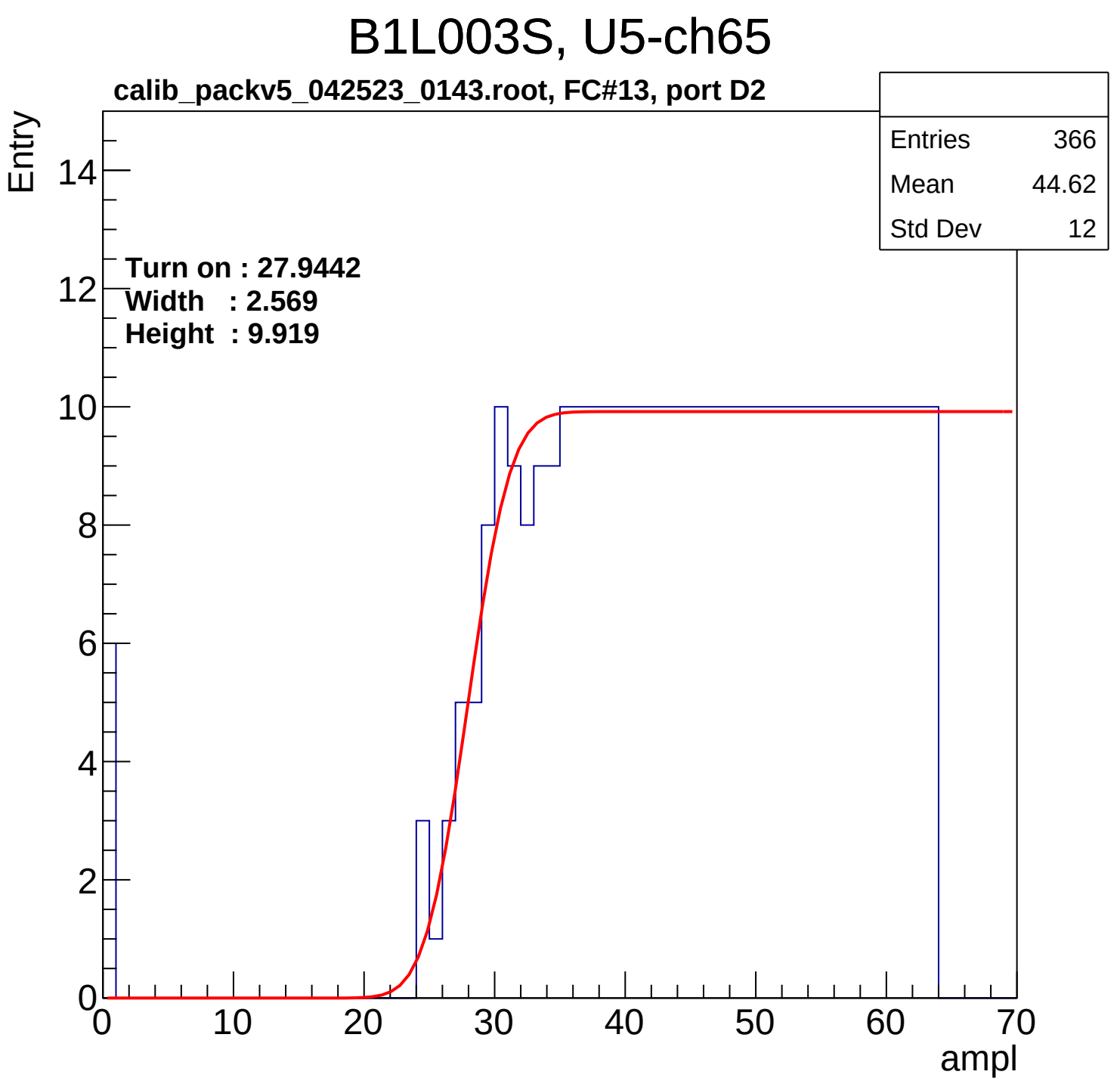
B1L003S, U5-ch65
calib_packv5_042523_0143.root, FC#13, port D2
Entries 366
Mean 44.62
Std Dev 12
Turn on : 27.9442
Width : 2.569
Height : 9.919
Entry
ampl
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2
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6
8
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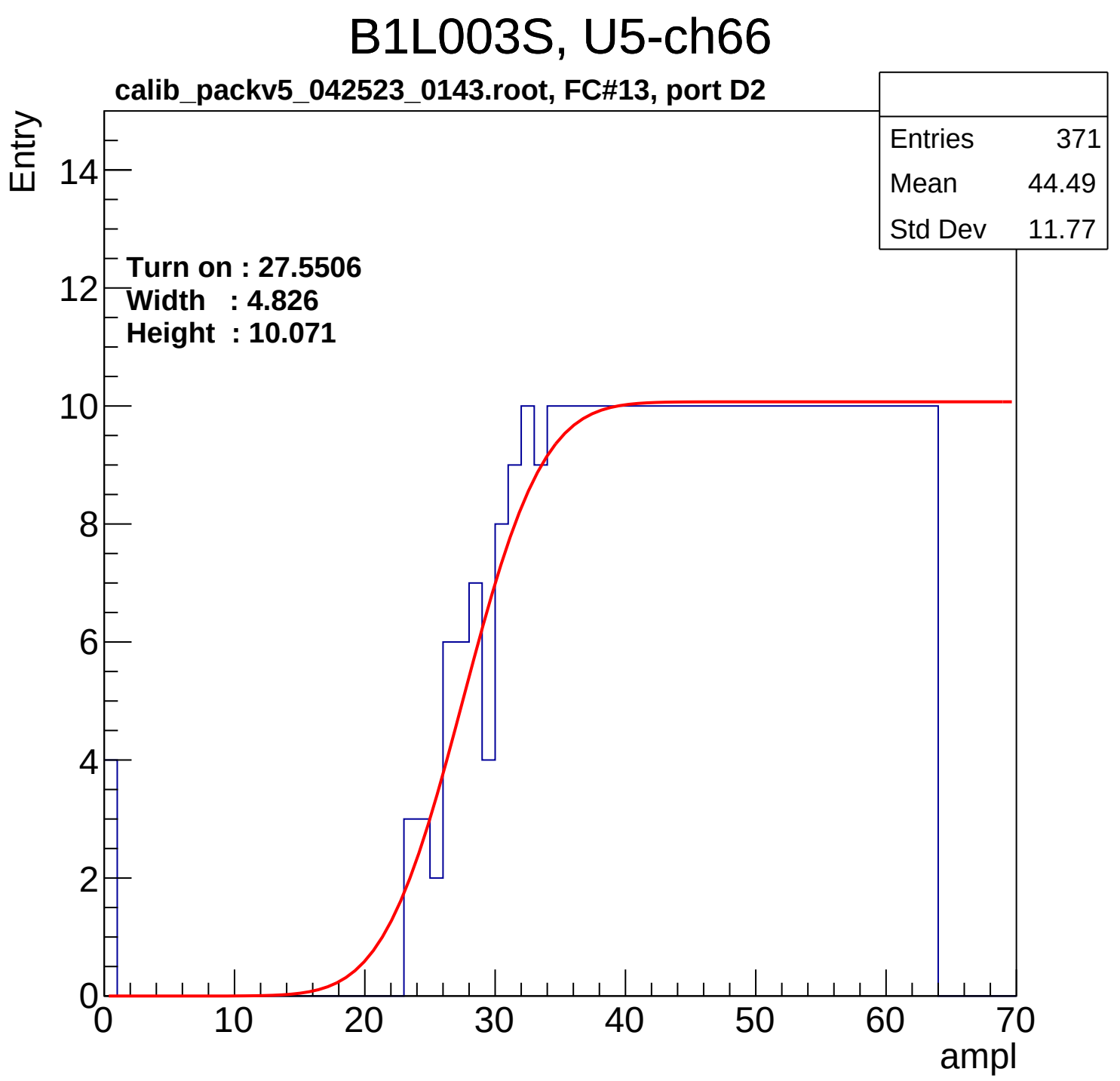
B1L003S, U5-ch66
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.49
Std Dev 11.77
Turn on : 27.5506
Width : 4.826
Height : 10.071
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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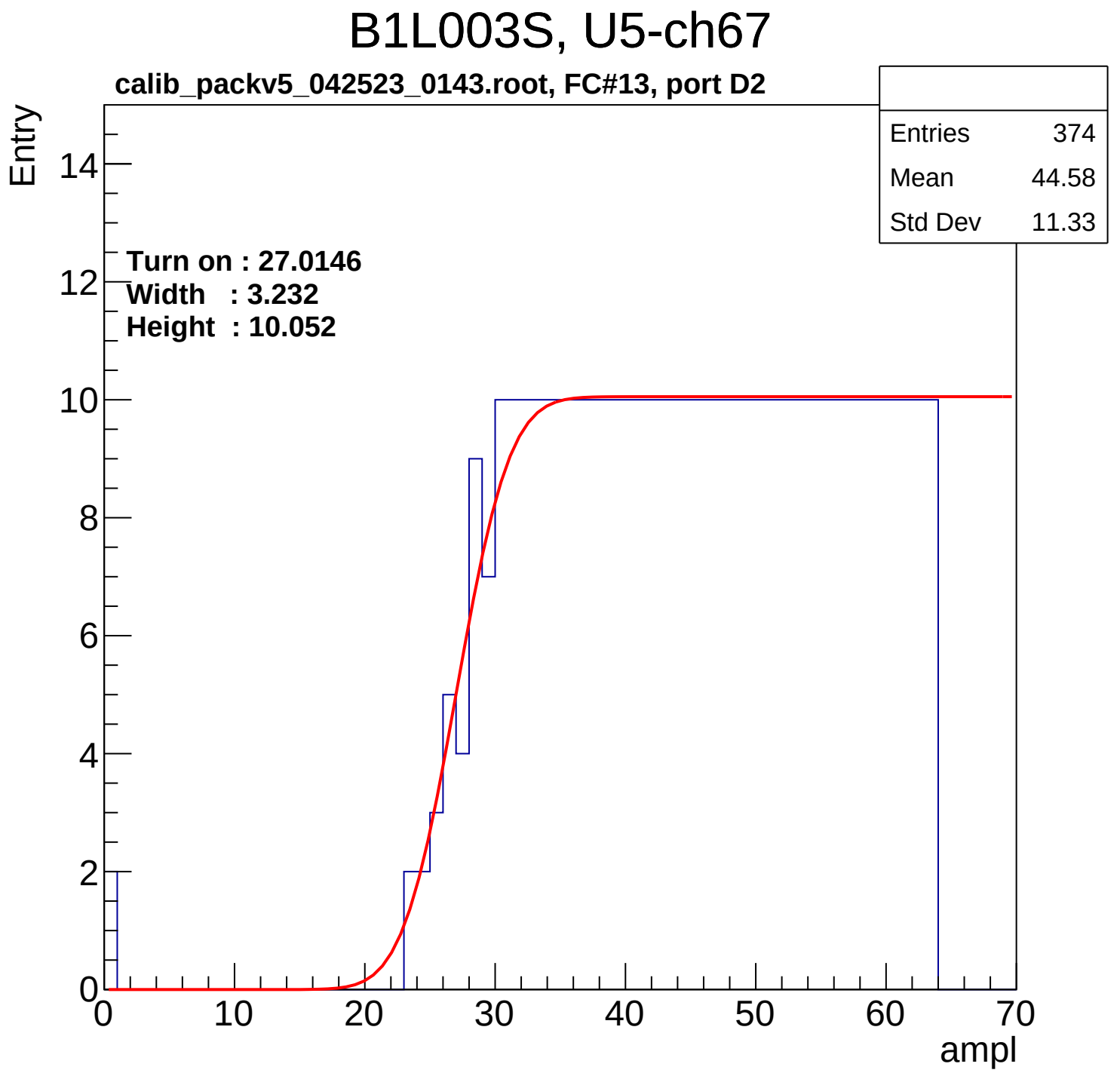
B1L003S, U5-ch67
calib_packv5_042523_0143.root, FC#13, port D2
Entries 374
Mean 44.58
Std Dev 11.33
Turn on : 27.0146
Width : 3.232
Height : 10.052
Entry
ampl
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4
6
8
10
12
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0
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60
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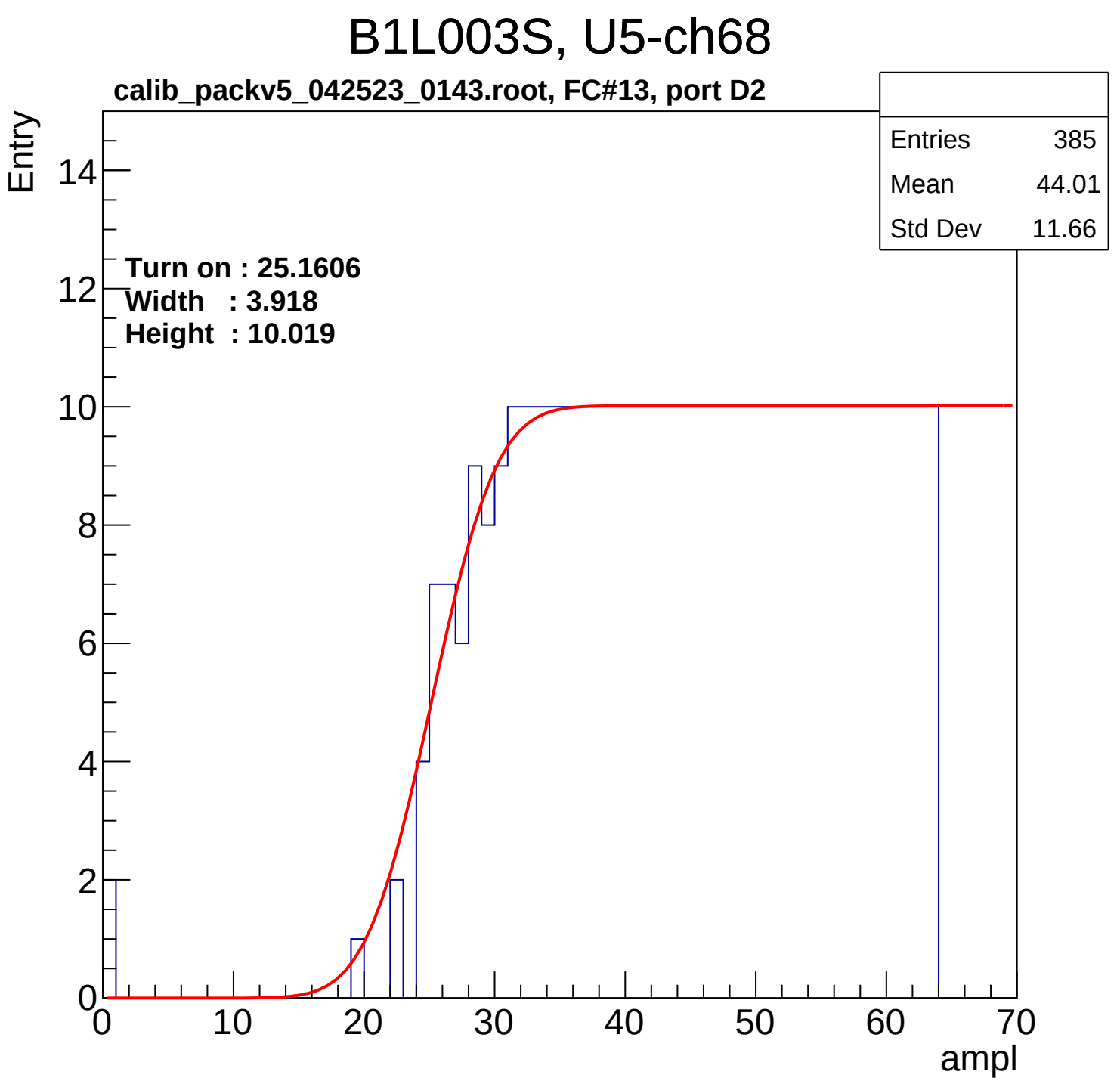
B1L003S, U5-ch68
calib_packv5_042523_0143.root, FC#13, port D2
Entries 385
Mean 44.01
Std Dev 11.66
Turn on : 25.1606
Width : 3.918
Height : 10.019
Entry
ampl
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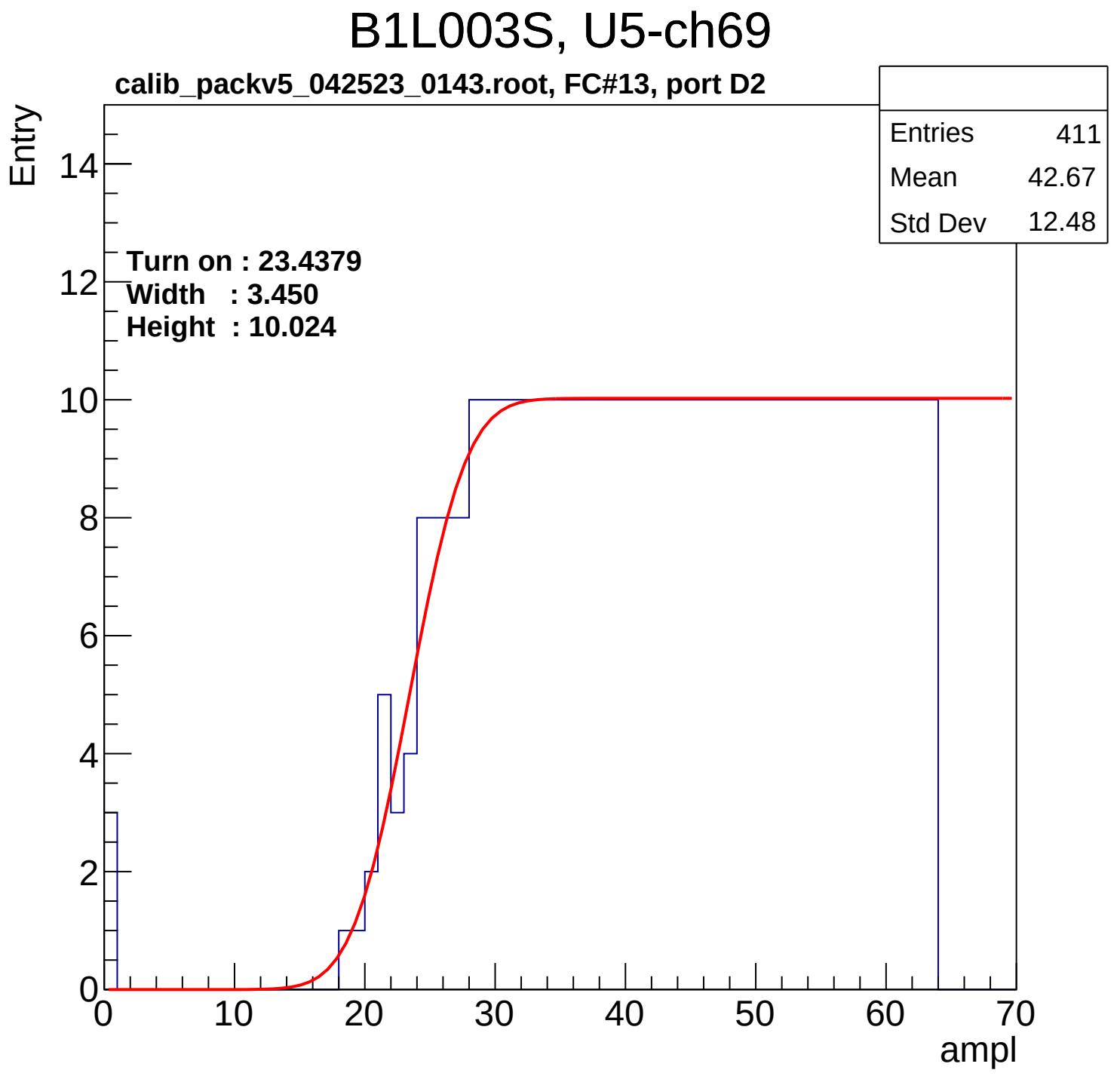
B1L003S, U5-ch69
calib_packv5_042523_0143.root, FC#13, port D2
Entries 411
Mean 42.67
Std Dev 12.48
Turn on : 23.4379
Width : 3.450
Height : 10.024
Entry
ampl
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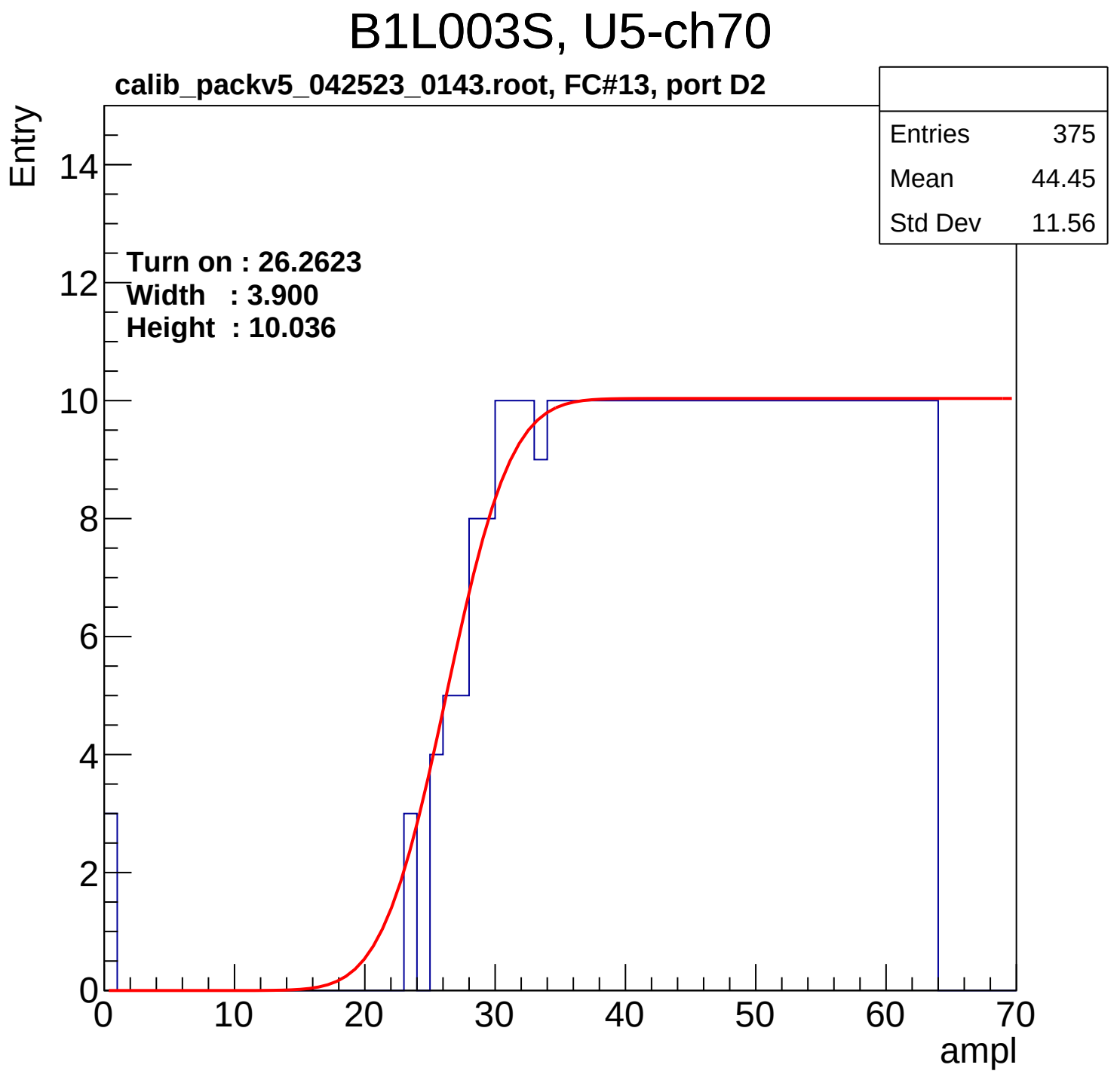
B1L003S, U5-ch70
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.45
Std Dev 11.56
Turn on : 26.2623
Width : 3.900
Height : 10.036
Entry
ampl
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6
8
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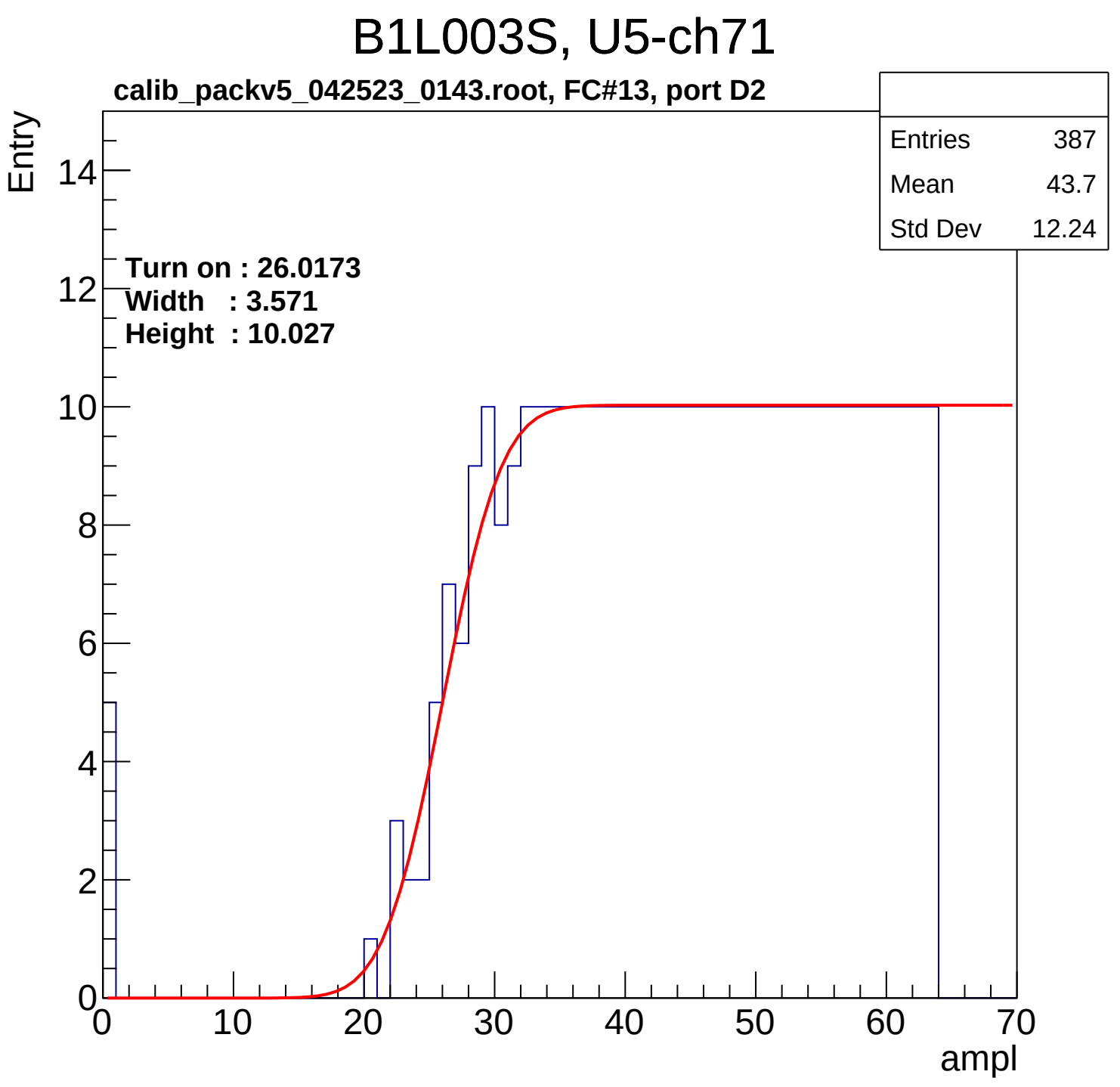
B1L003S, U5-ch71
calib_packv5_042523_0143.root, FC#13, port D2
Entries 387
Mean 43.7
Std Dev 12.24
Turn on : 26.0173
Width : 3.571
Height : 10.027
Entry
ampl
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8
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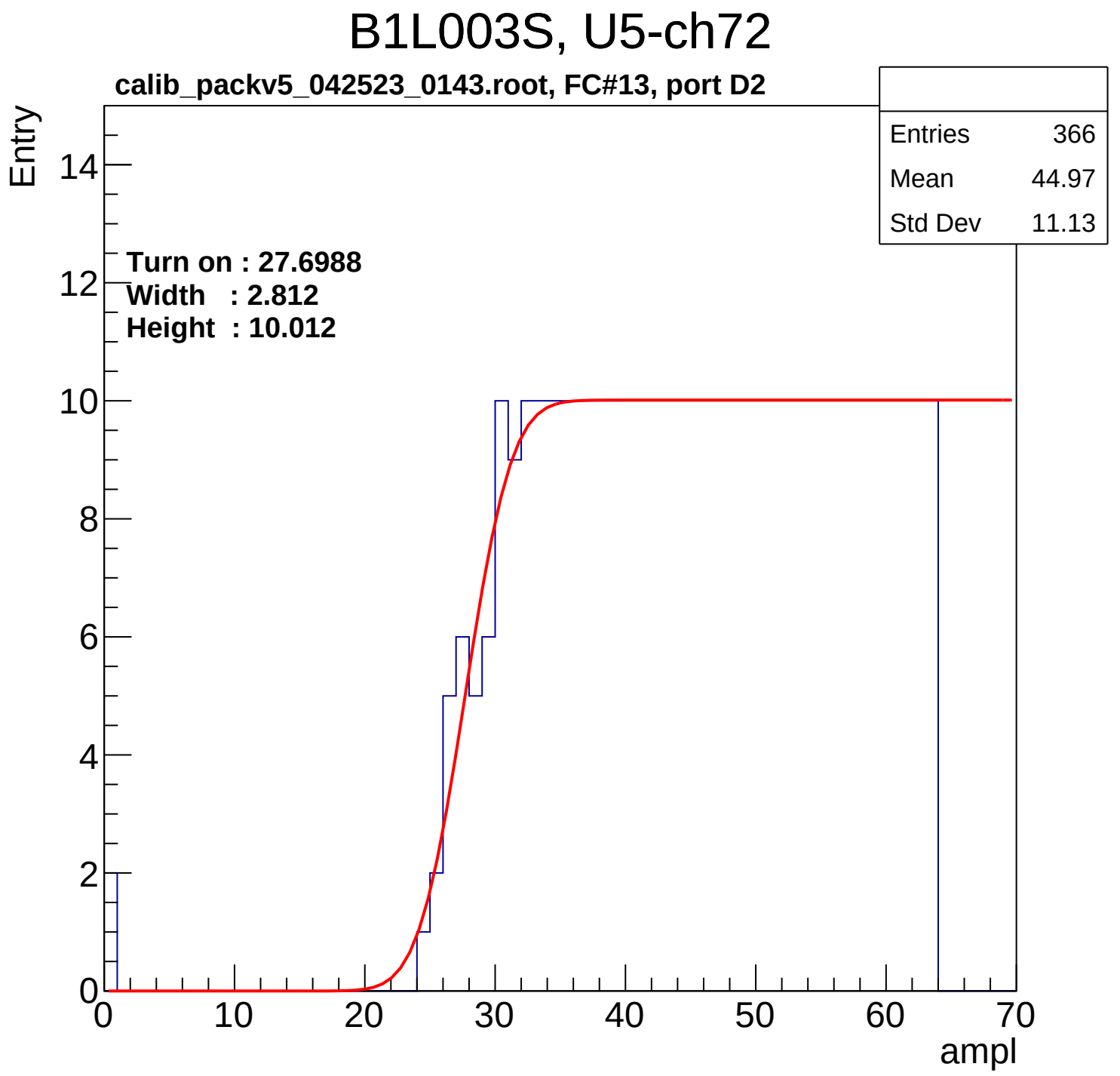
B1L003S, U5-ch72
calib_packv5_042523_0143.root, FC#13, port D2
Entries 366
Mean 44.97
Std Dev 11.13
Turn on : 27.6988
Width : 2.812
Height : 10.012
Entry
ampl
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4
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8
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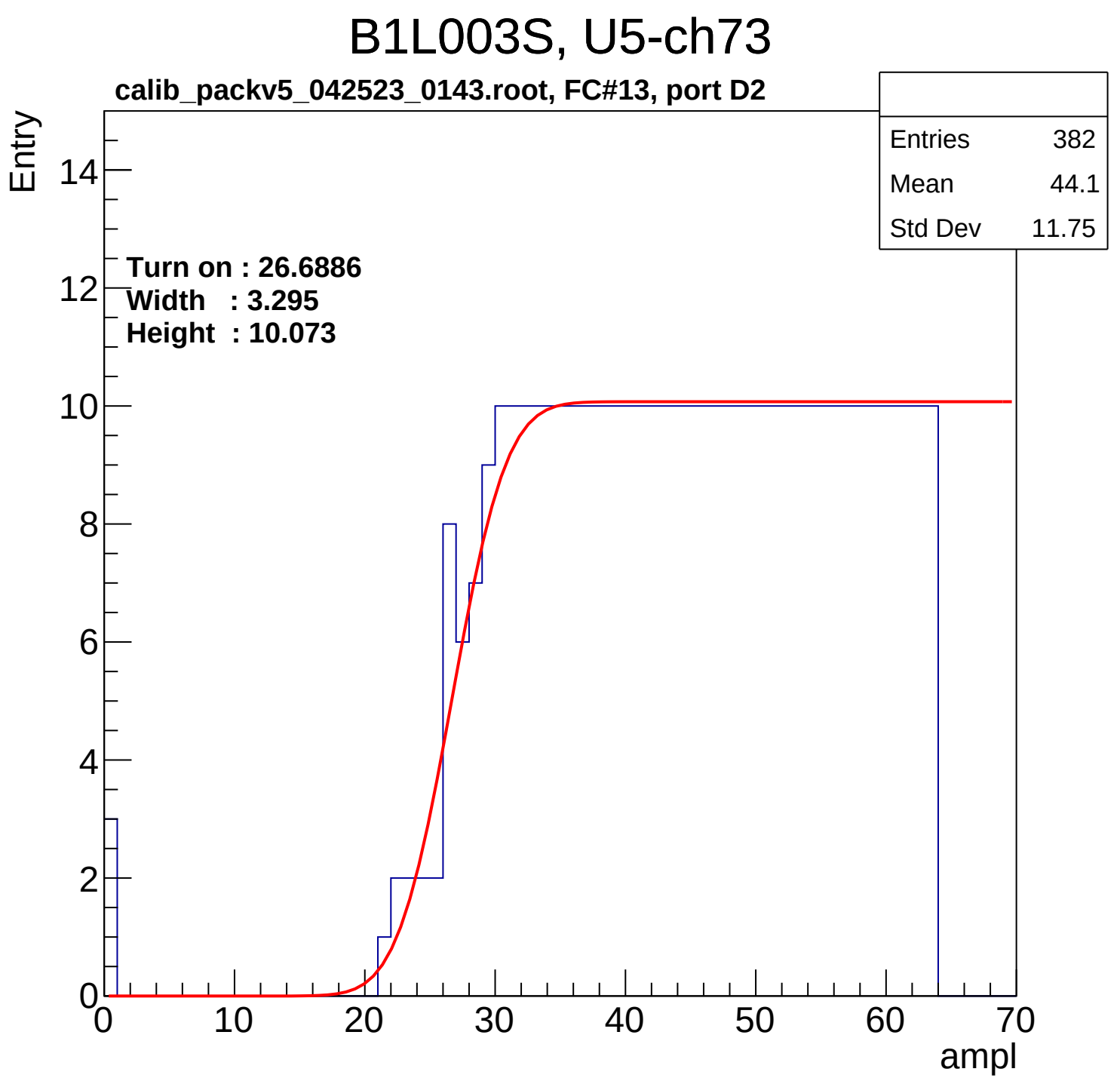
B1L003S, U5-ch73
calib_packv5_042523_0143.root, FC#13, port D2
Entries 382
Mean 44.1
Std Dev 11.75
Turn on : 26.6886
Width : 3.295
Height : 10.073
Entry
ampl
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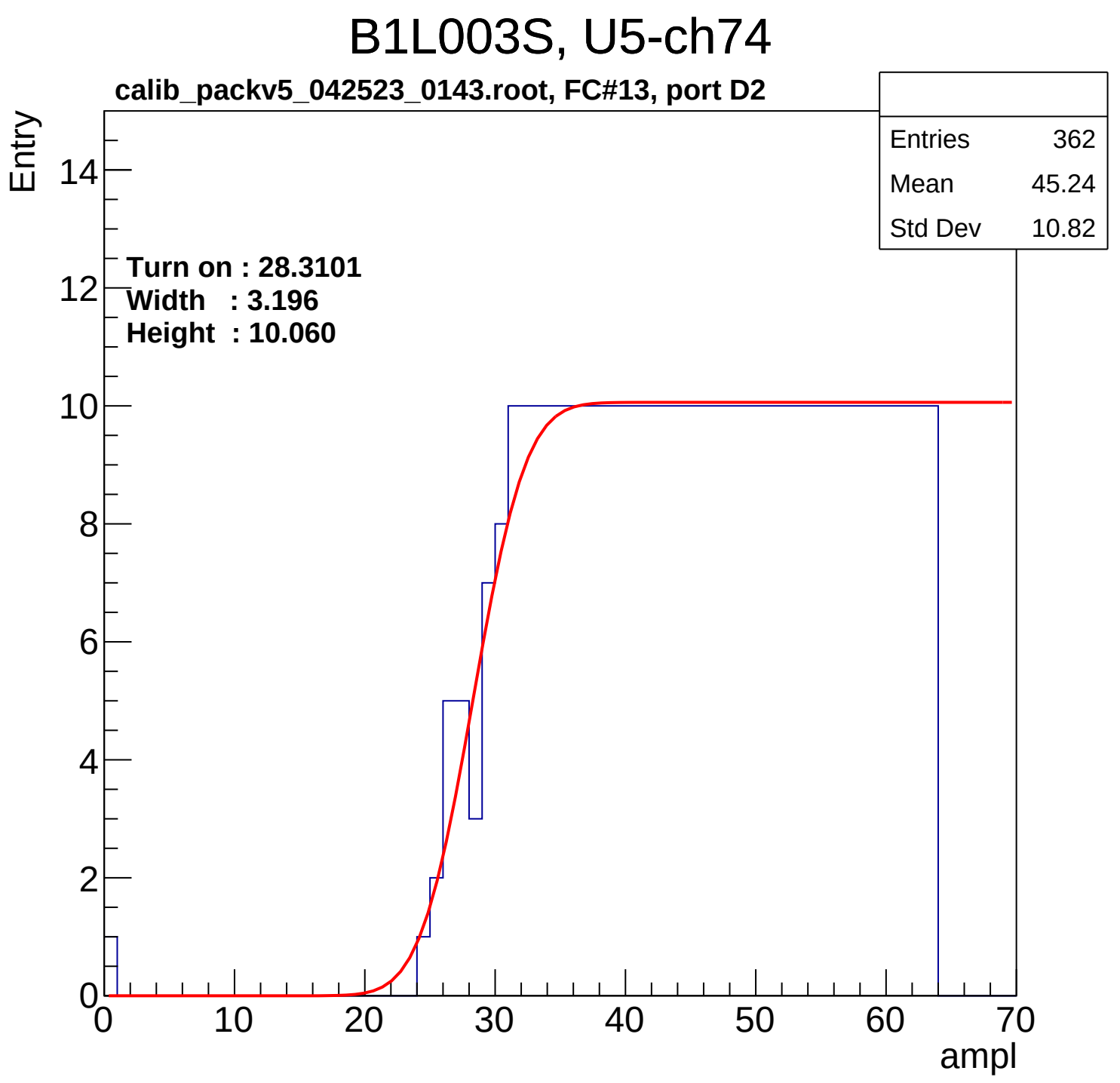
B1L003S, U5-ch74
calib_packv5_042523_0143.root, FC#13, port D2
Entries 362
Mean 45.24
Std Dev 10.82
Turn on : 28.3101
Width : 3.196
Height : 10.060
Entry
ampl
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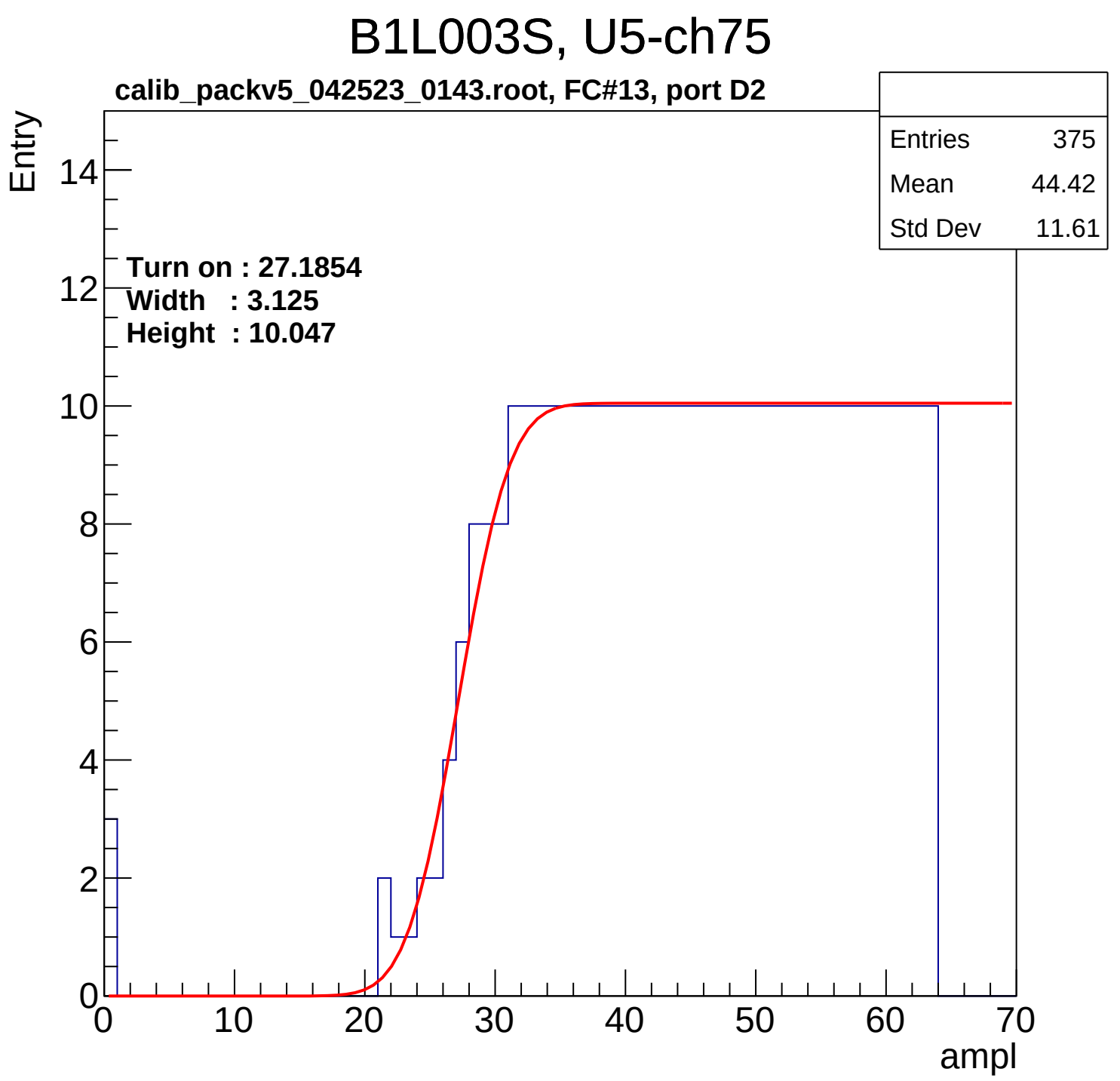
B1L003S, U5-ch75
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.42
Std Dev 11.61
Turn on : 27.1854
Width : 3.125
Height : 10.047
Entry
ampl
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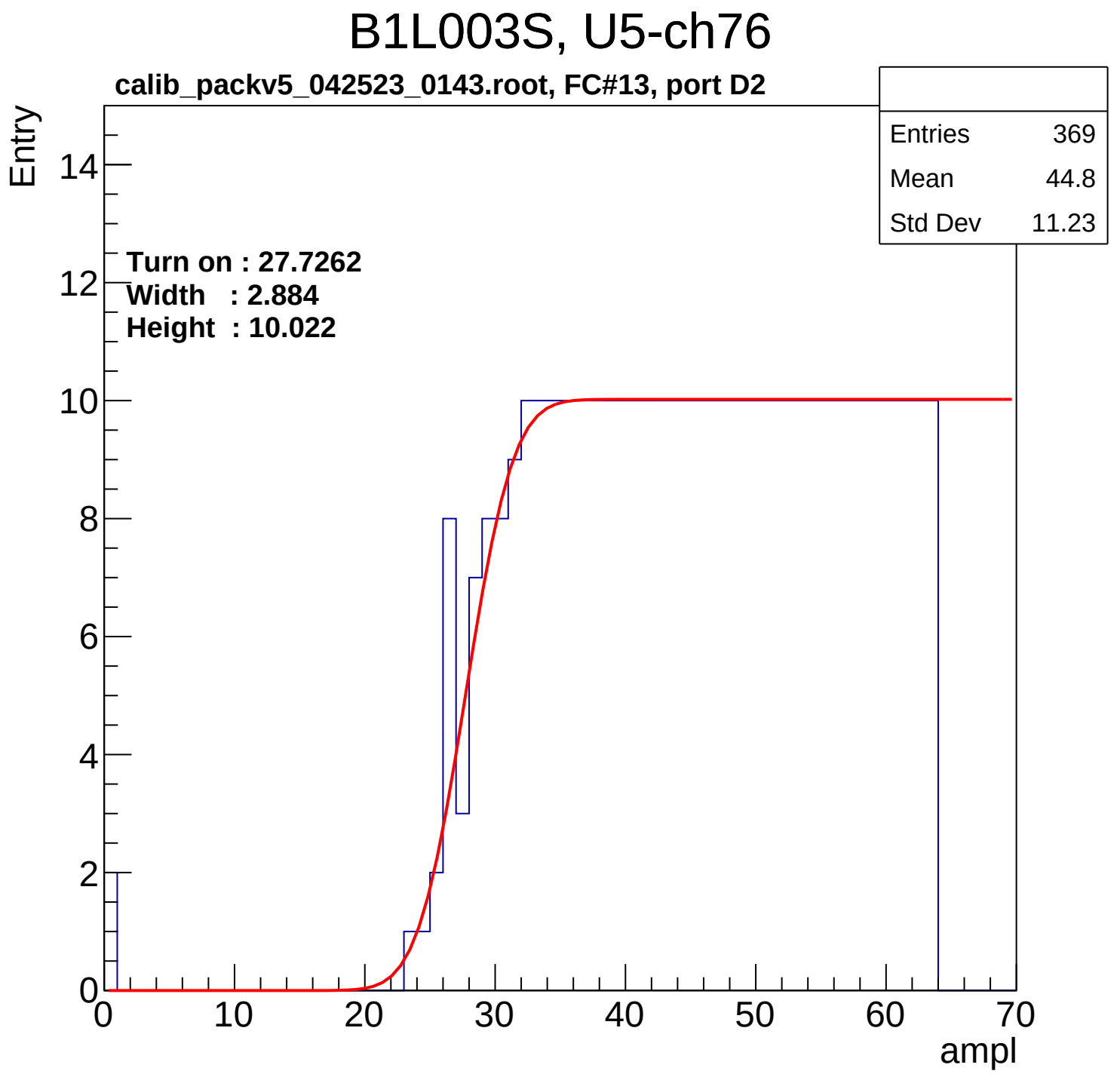
B1L003S, U5-ch76
calib_packv5_042523_0143.root, FC#13, port D2
Entries 369
Mean 44.8
Std Dev 11.23
Turn on : 27.7262
Width : 2.884
Height : 10.022
Entry
ampl
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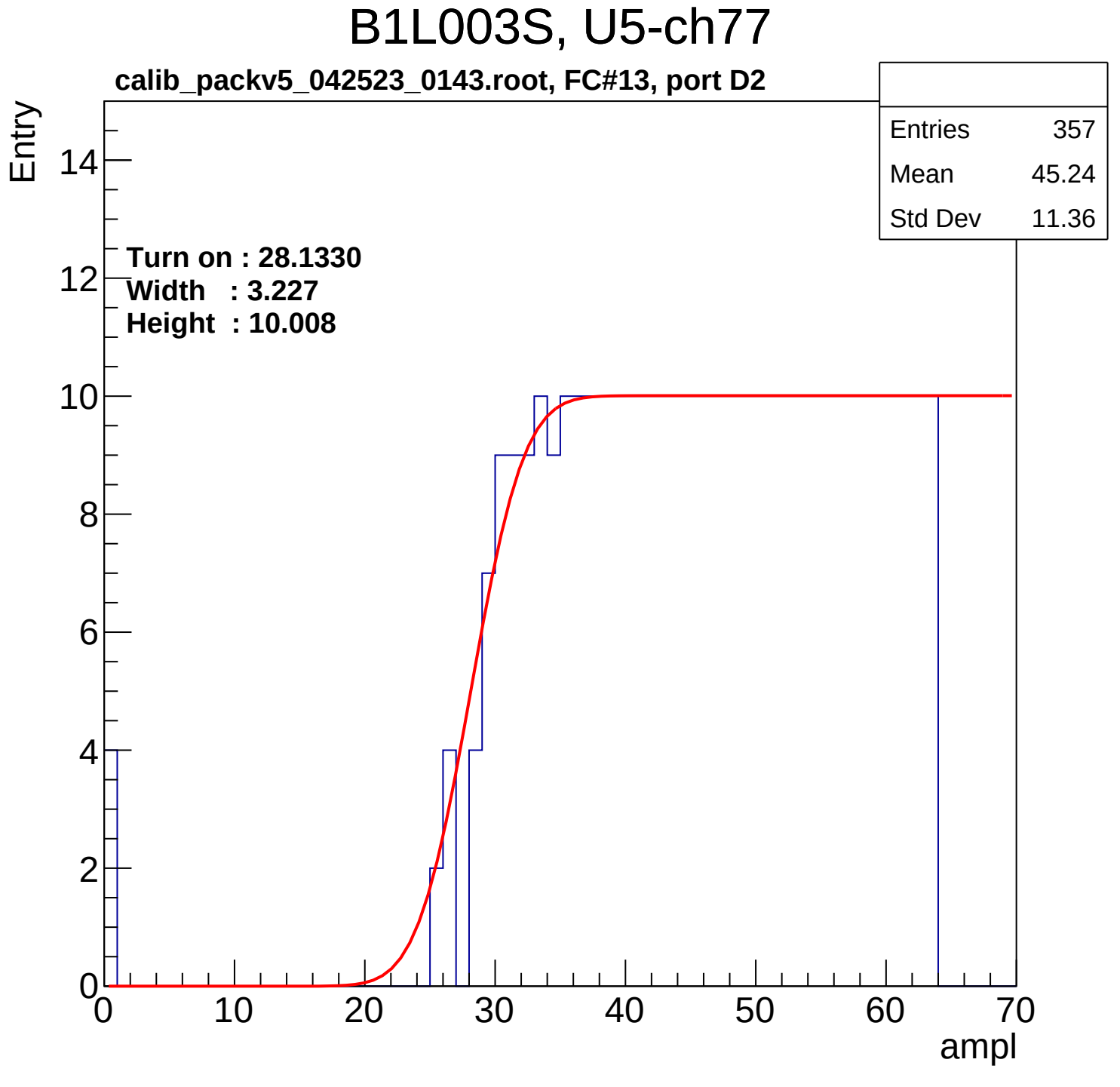
B1L003S, U5-ch77
calib_packv5_042523_0143.root, FC#13, port D2
Entries 357
Mean 45.24
Std Dev 11.36
Turn on : 28.1330
Width : 3.227
Height : 10.008
Entry
ampl
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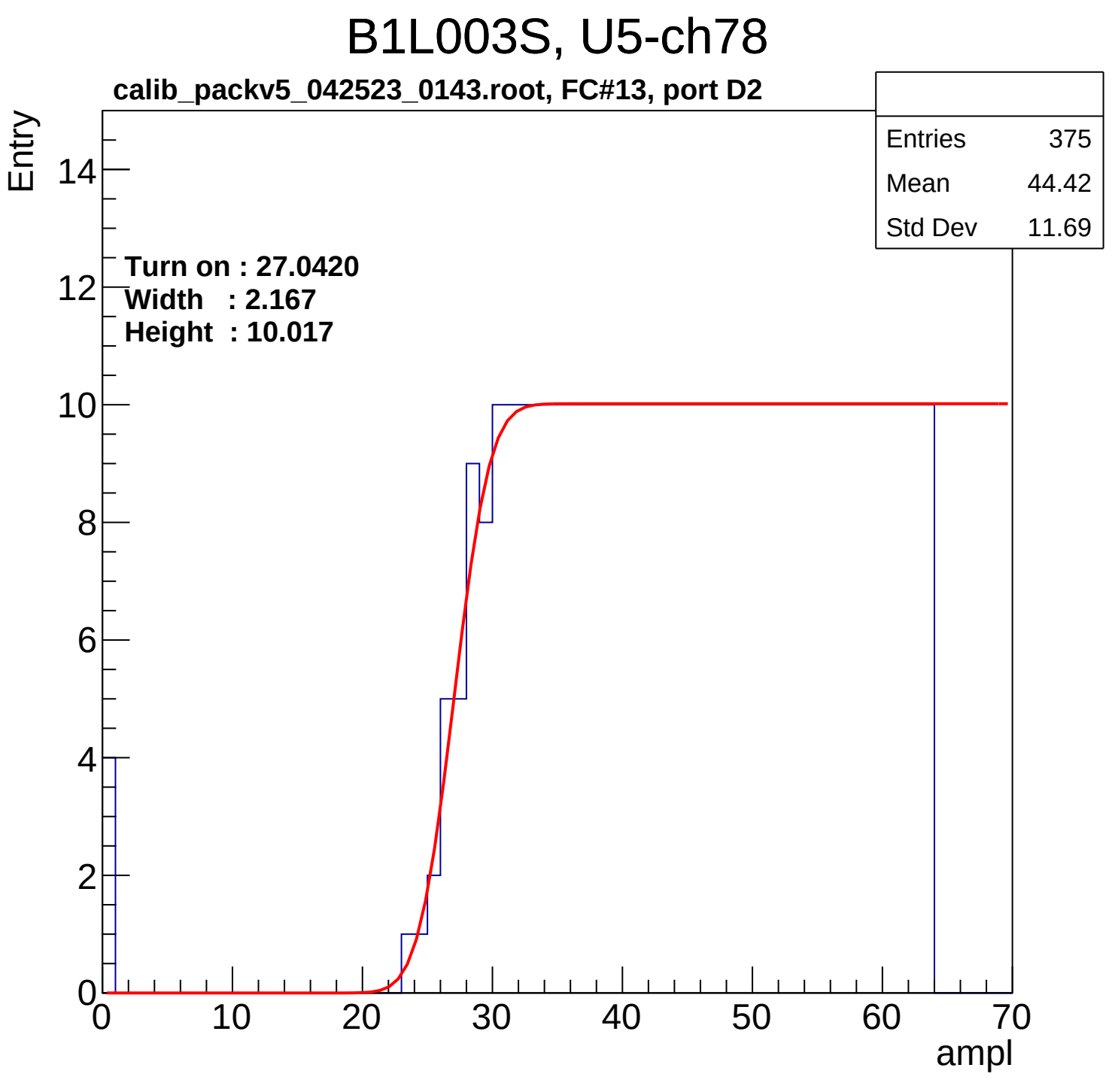
B1L003S, U5-ch78
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.42
Std Dev 11.69
Turn on : 27.0420
Width : 2.167
Height : 10.017
Entry
ampl
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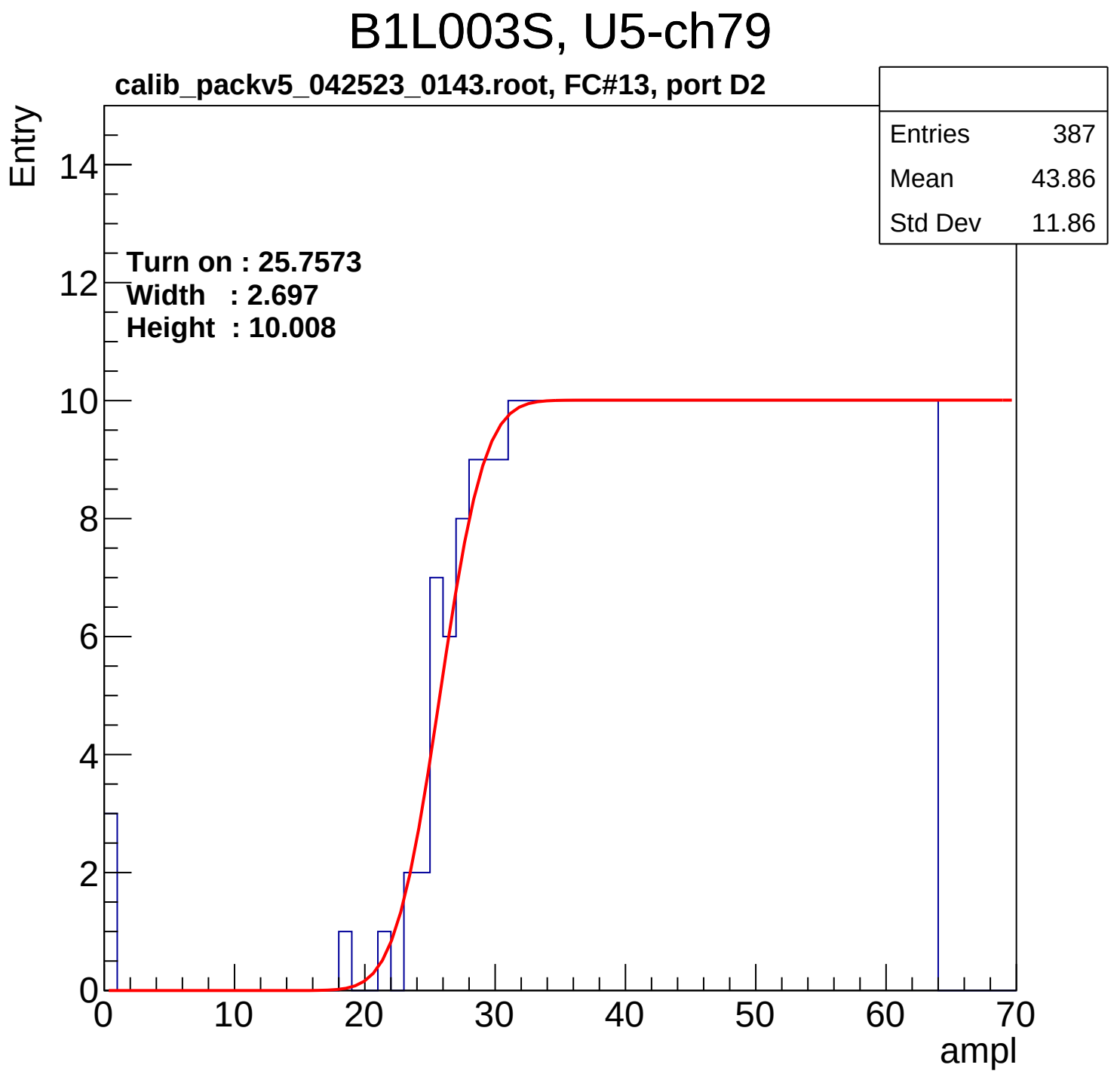
B1L003S, U5-ch79
calib_packv5_042523_0143.root, FC#13, port D2
Entries 387
Mean 43.86
Std Dev 11.86
Turn on : 25.7573
Width : 2.697
Height : 10.008
Entry
ampl
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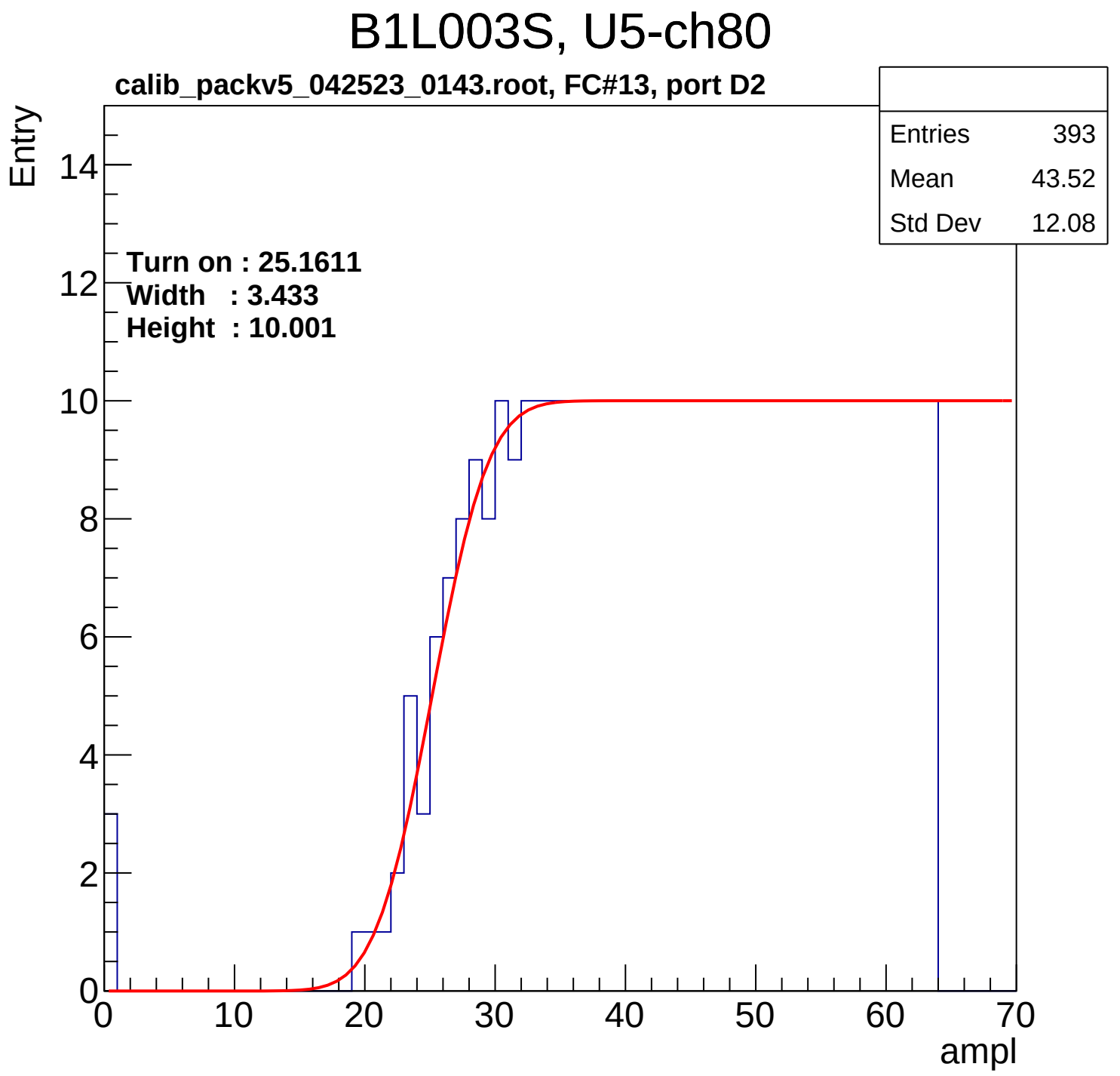
B1L003S, U5-ch80
calib_packv5_042523_0143.root, FC#13, port D2
Entries 393
Mean 43.52
Std Dev 12.08
Turn on : 25.1611
Width : 3.433
Height : 10.001
Entry
ampl
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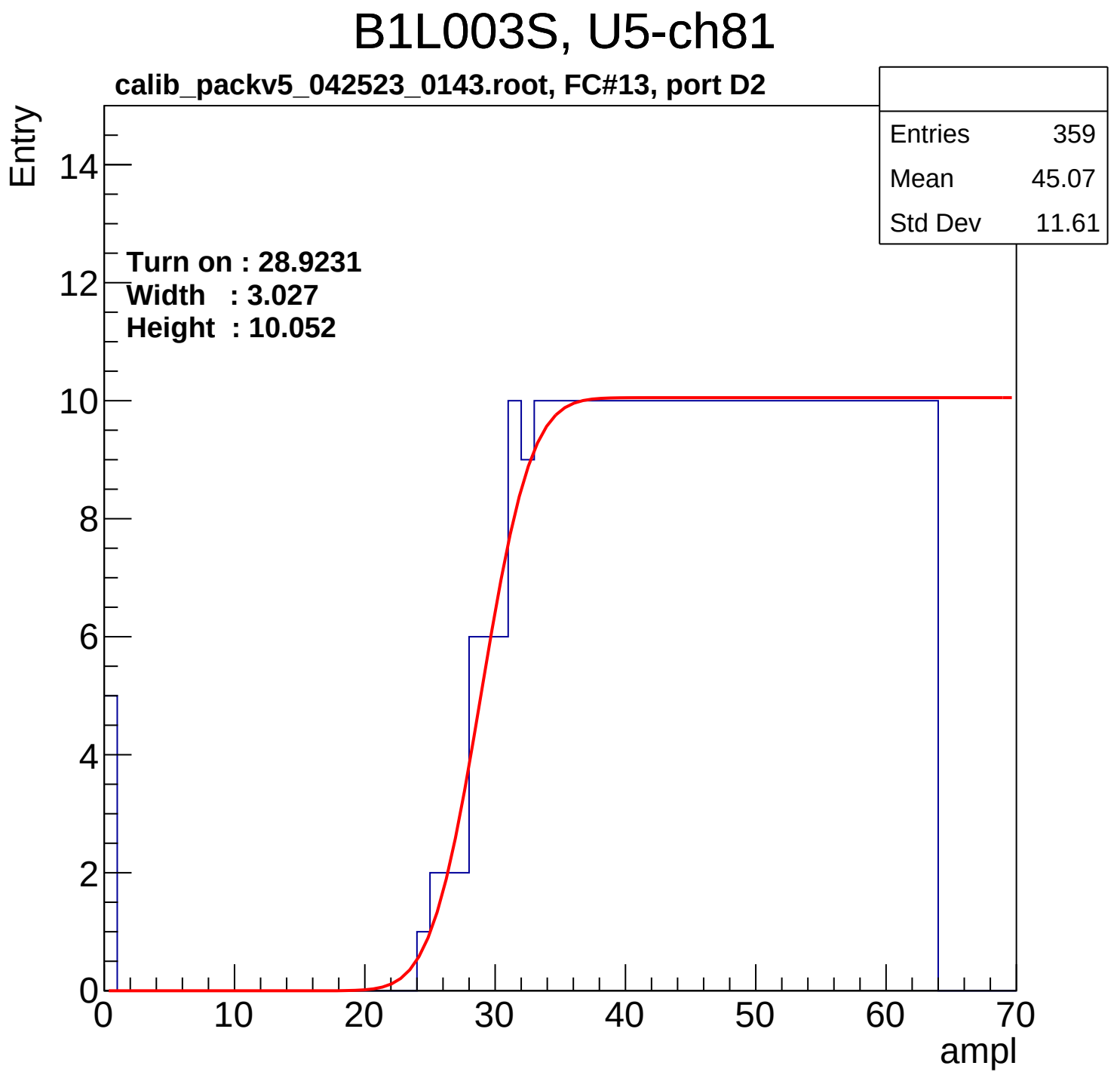
B1L003S, U5-ch81
calib_packv5_042523_0143.root, FC#13, port D2
Entries 359
Mean 45.07
Std Dev 11.61
Turn on : 28.9231
Width : 3.027
Height : 10.052
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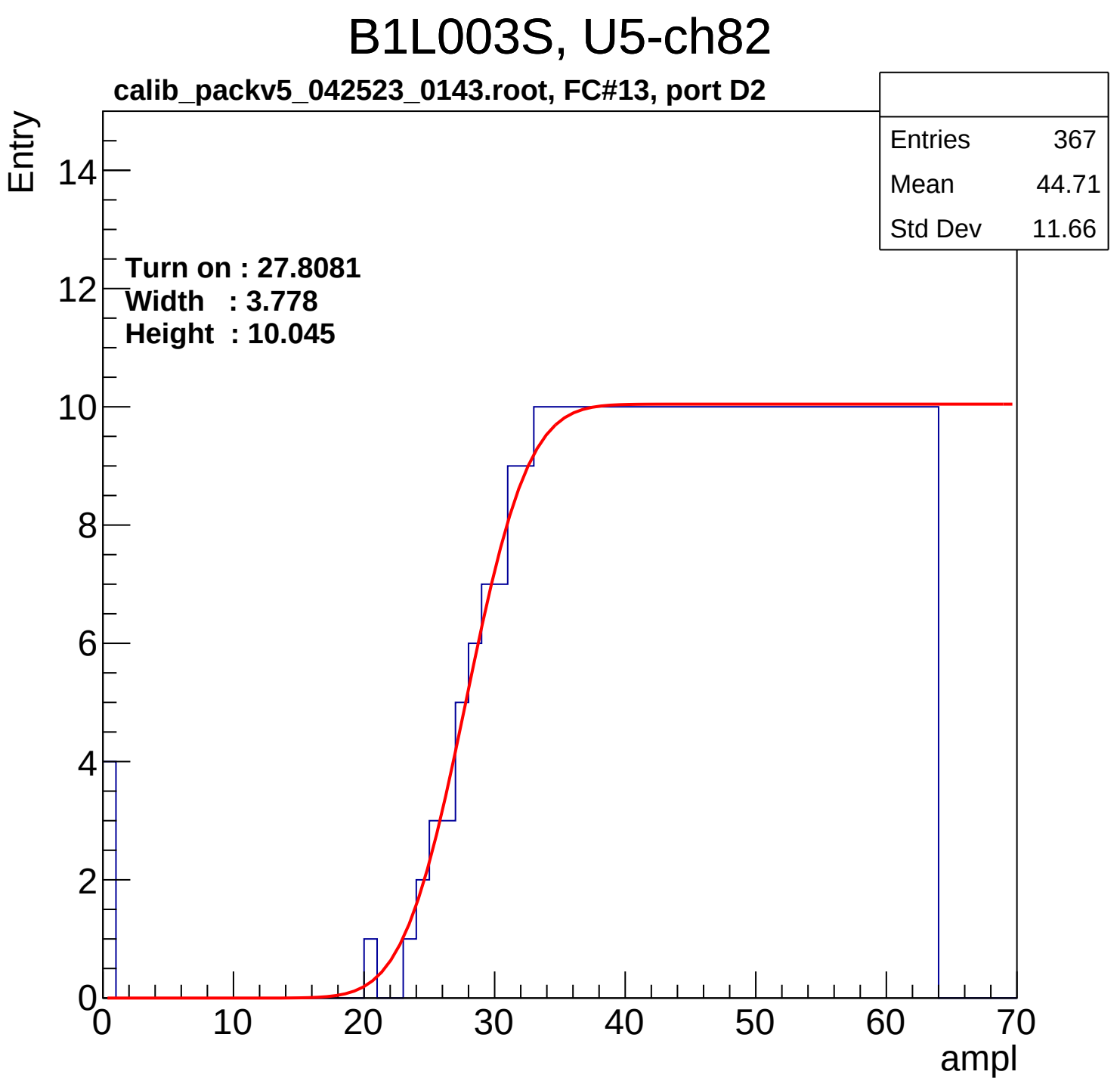
B1L003S, U5-ch82
calib_packv5_042523_0143.root, FC#13, port D2
Entries 367
Mean 44.71
Std Dev 11.66
Turn on : 27.8081
Width : 3.778
Height : 10.045
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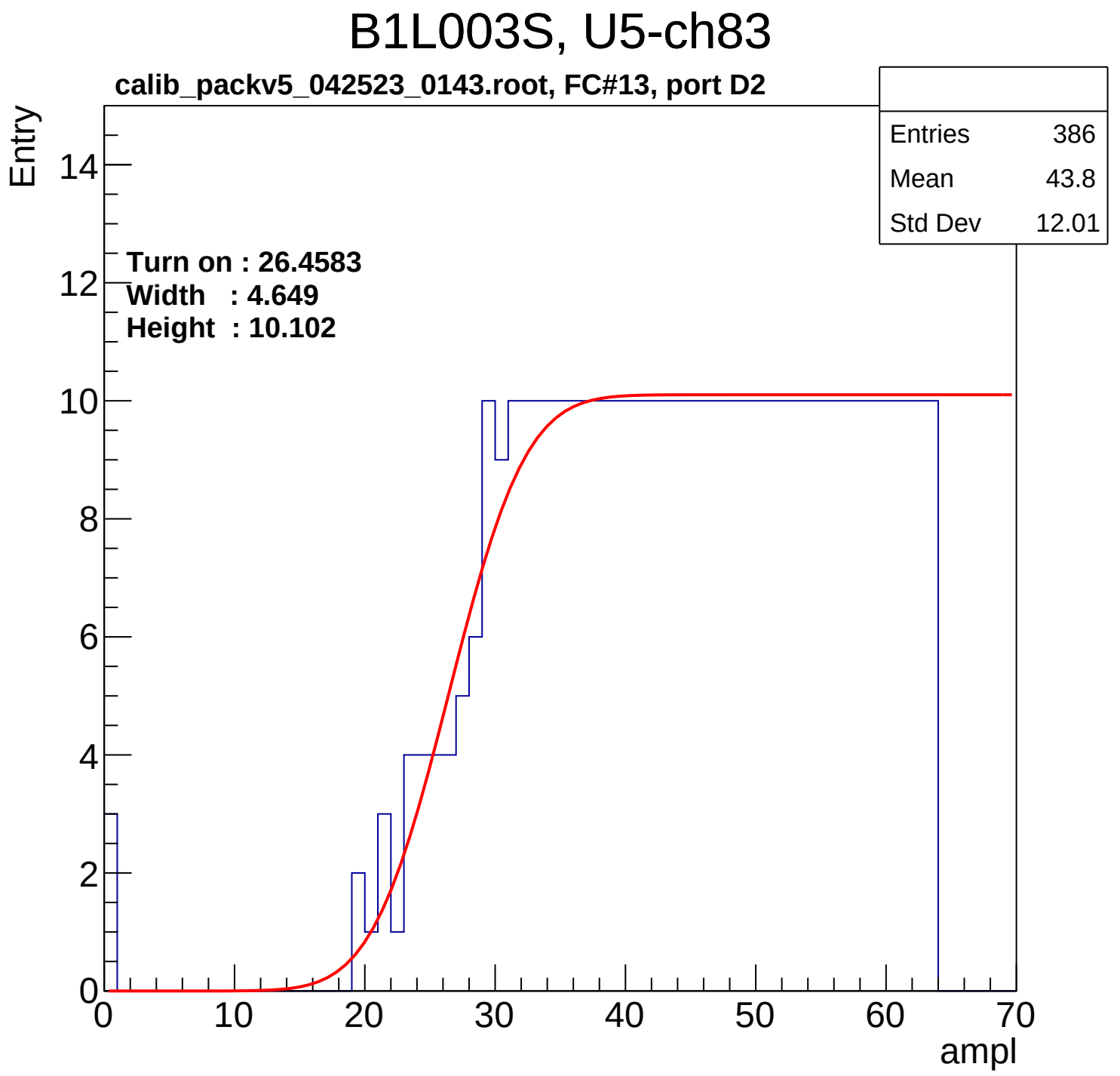
B1L003S, U5-ch83
calib_packv5_042523_0143.root, FC#13, port D2
Entries 386
Mean 43.8
Std Dev 12.01
Turn on : 26.4583
Width : 4.649
Height : 10.102
Entry
ampl
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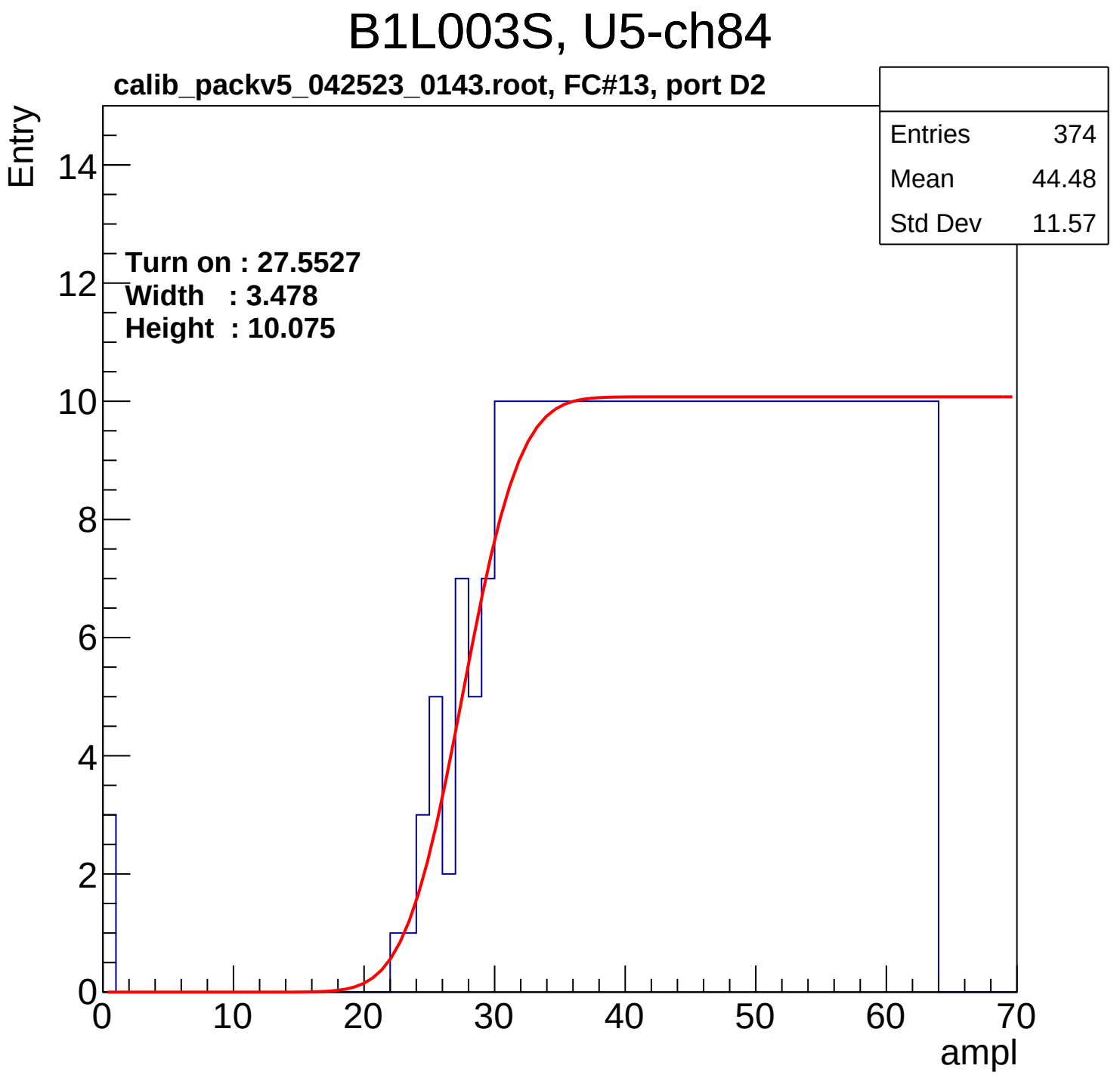
B1L003S, U5-ch84
calib_packv5_042523_0143.root, FC#13, port D2
Entries 374
Mean 44.48
Std Dev 11.57
Turn on : 27.5527
Width : 3.478
Height : 10.075
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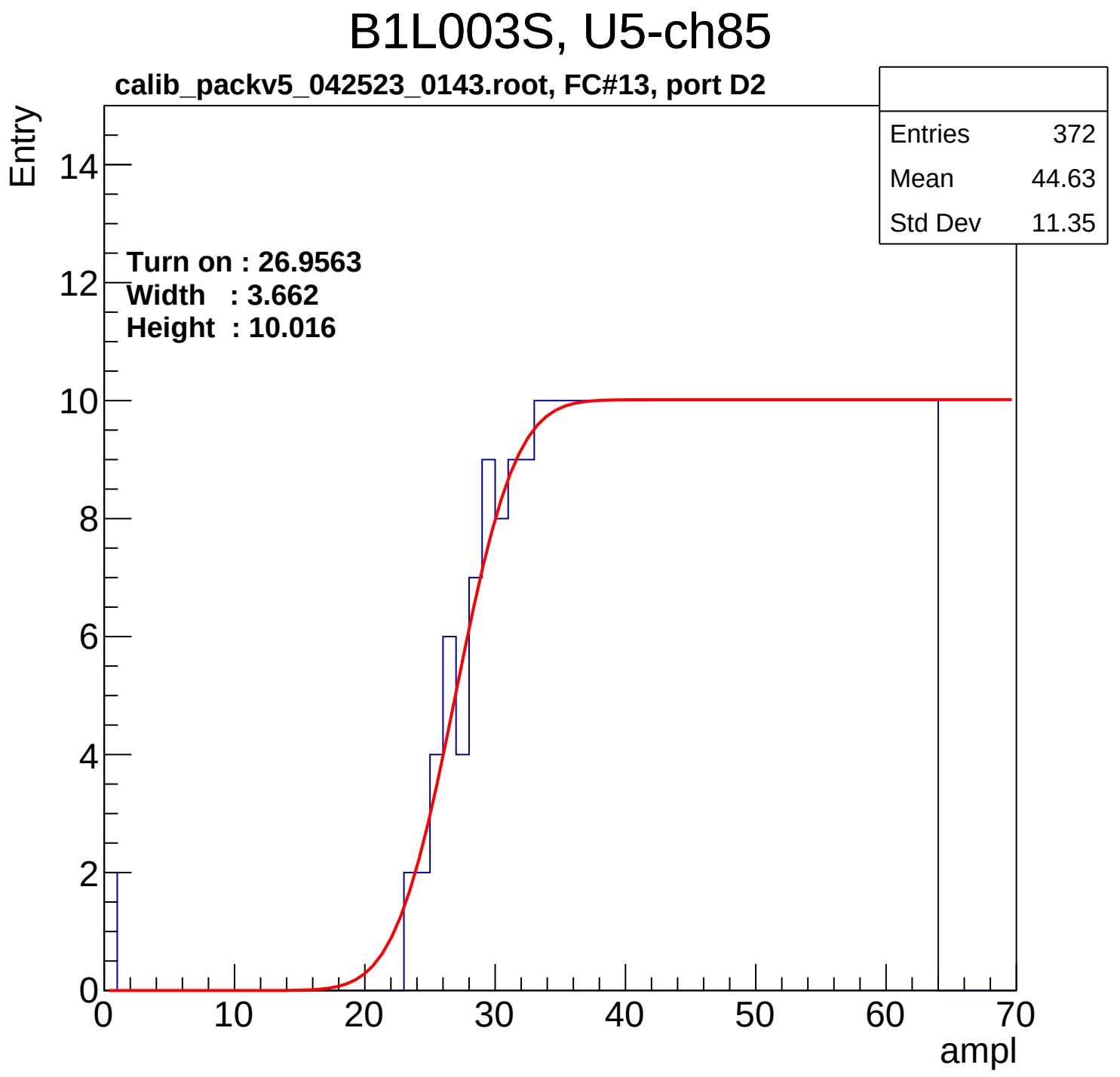
B1L003S, U5-ch85
calib_packv5_042523_0143.root, FC#13, port D2
Entries 372
Mean 44.63
Std Dev 11.35
Turn on : 26.9563
Width : 3.662
Height : 10.016
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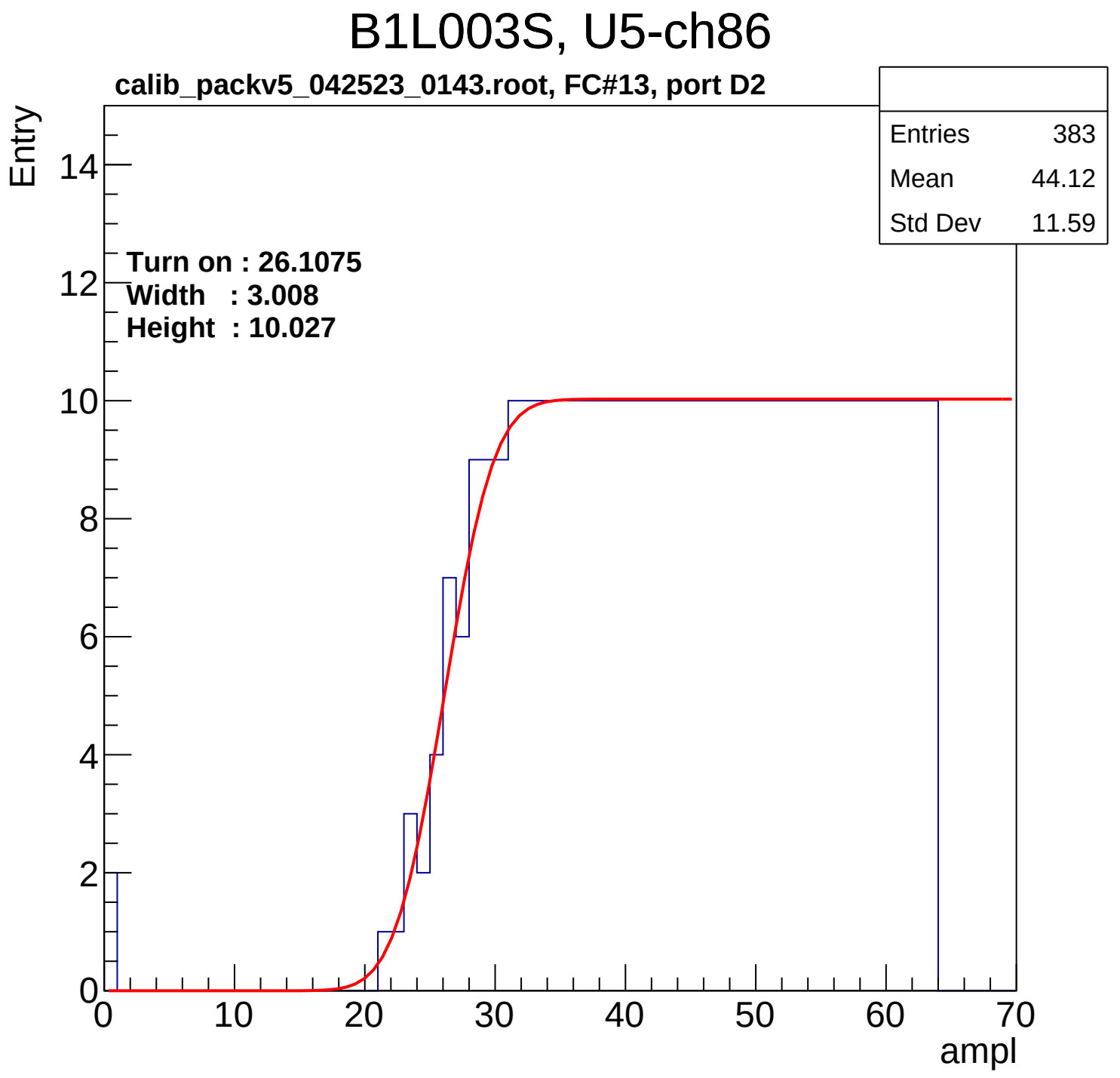
B1L003S, U5-ch86
calib_packv5_042523_0143.root, FC#13, port D2
Entries 383
Mean 44.12
Std Dev 11.59
Turn on : 26.1075
Width : 3.008
Height : 10.027
Entry
ampl
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20
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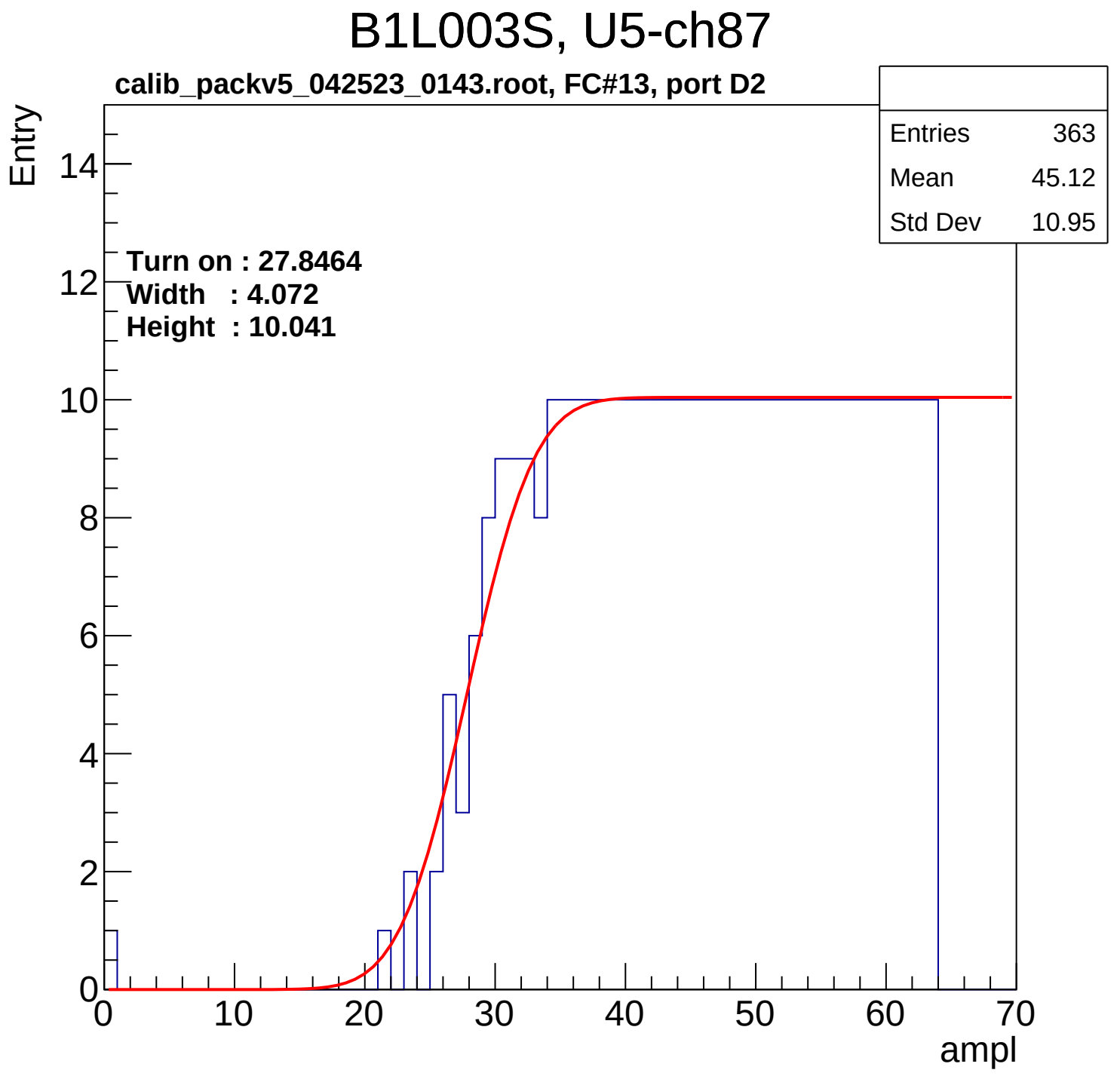
B1L003S, U5-ch87
calib_packv5_042523_0143.root, FC#13, port D2
Entries 363
Mean 45.12
Std Dev 10.95
Turn on : 27.8464
Width : 4.072
Height : 10.041
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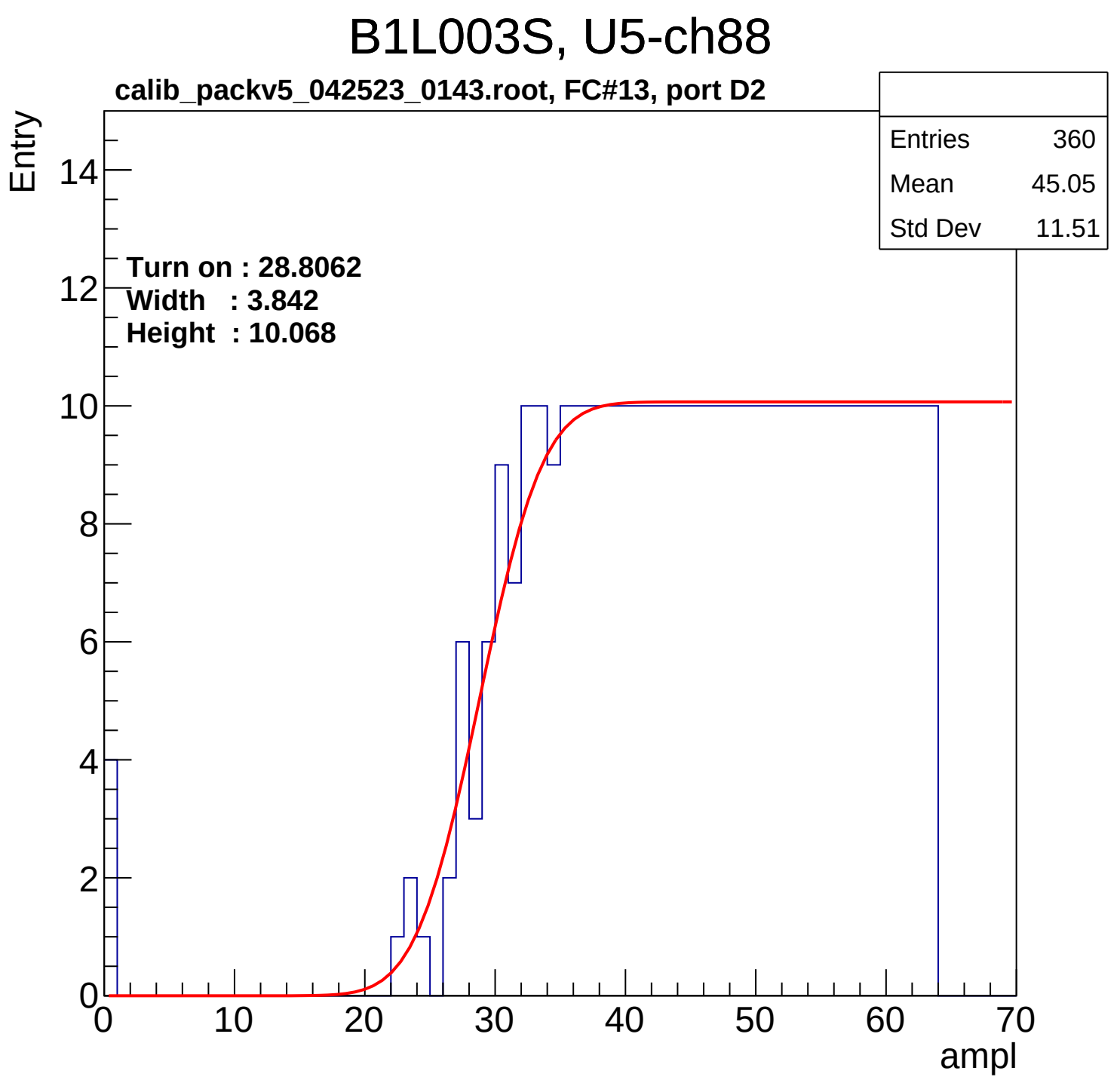
B1L003S, U5-ch88
calib_packv5_042523_0143.root, FC#13, port D2
Entries 360
Mean 45.05
Std Dev 11.51
Turn on : 28.8062
Width : 3.842
Height : 10.068
Entry
ampl
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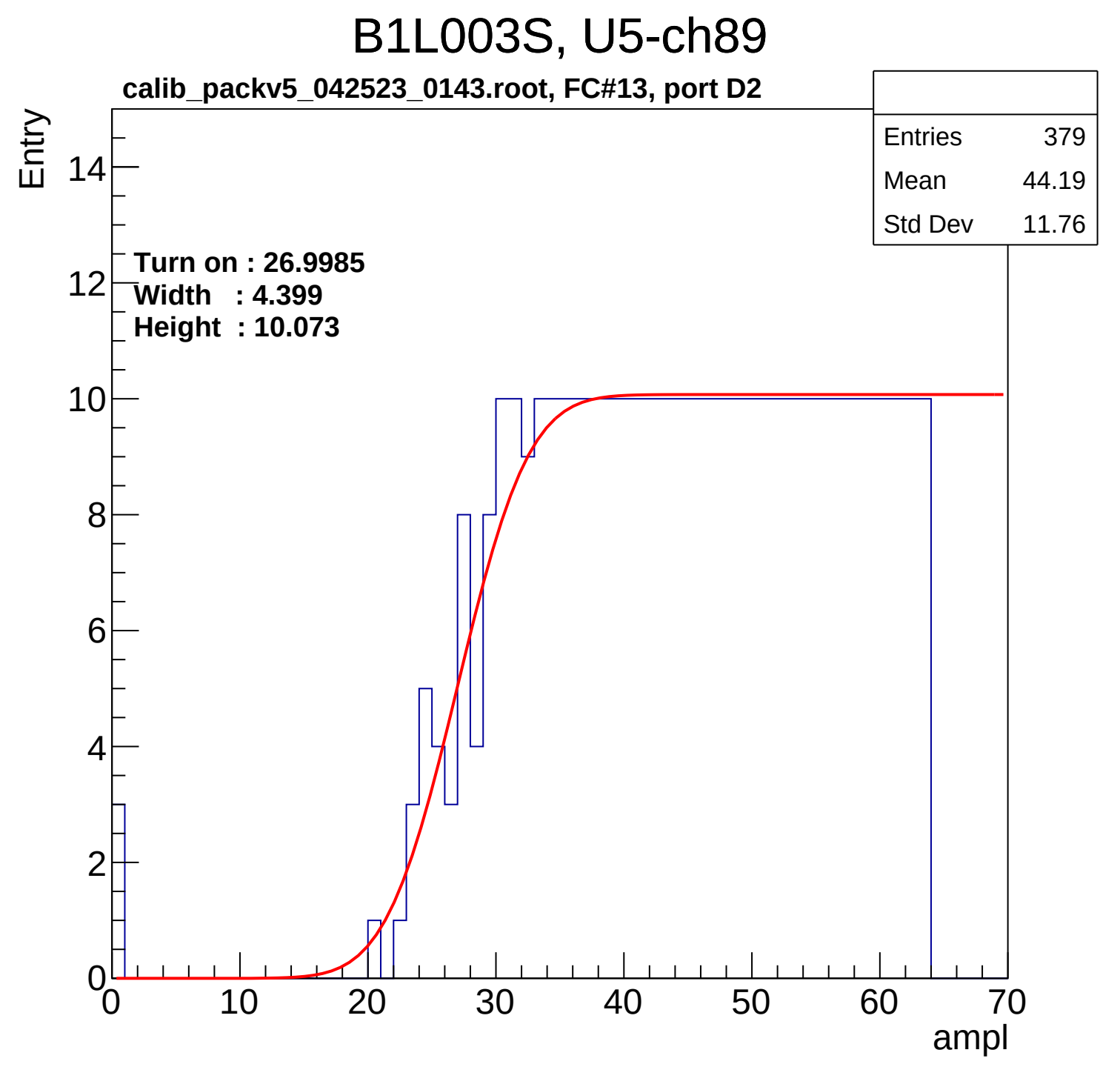
B1L003S, U5-ch89
calib_packv5_042523_0143.root, FC#13, port D2
Entries 379
Mean 44.19
Std Dev 11.76
Turn on : 26.9985
Width : 4.399
Height : 10.073
Entry
ampl
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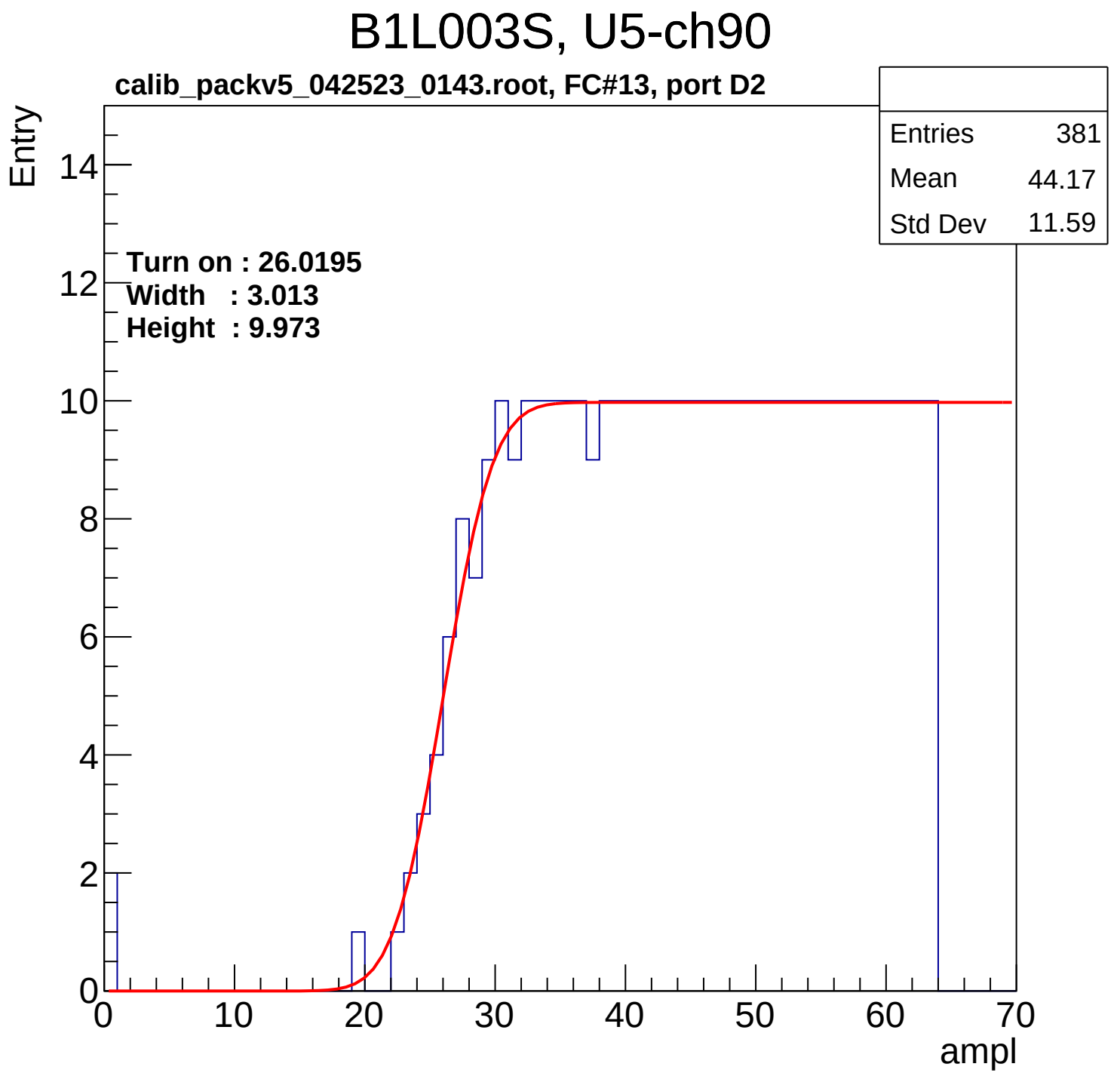
B1L003S, U5-ch90
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 44.17
Std Dev 11.59
Turn on : 26.0195
Width : 3.013
Height : 9.973
Entry
ampl
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4
6
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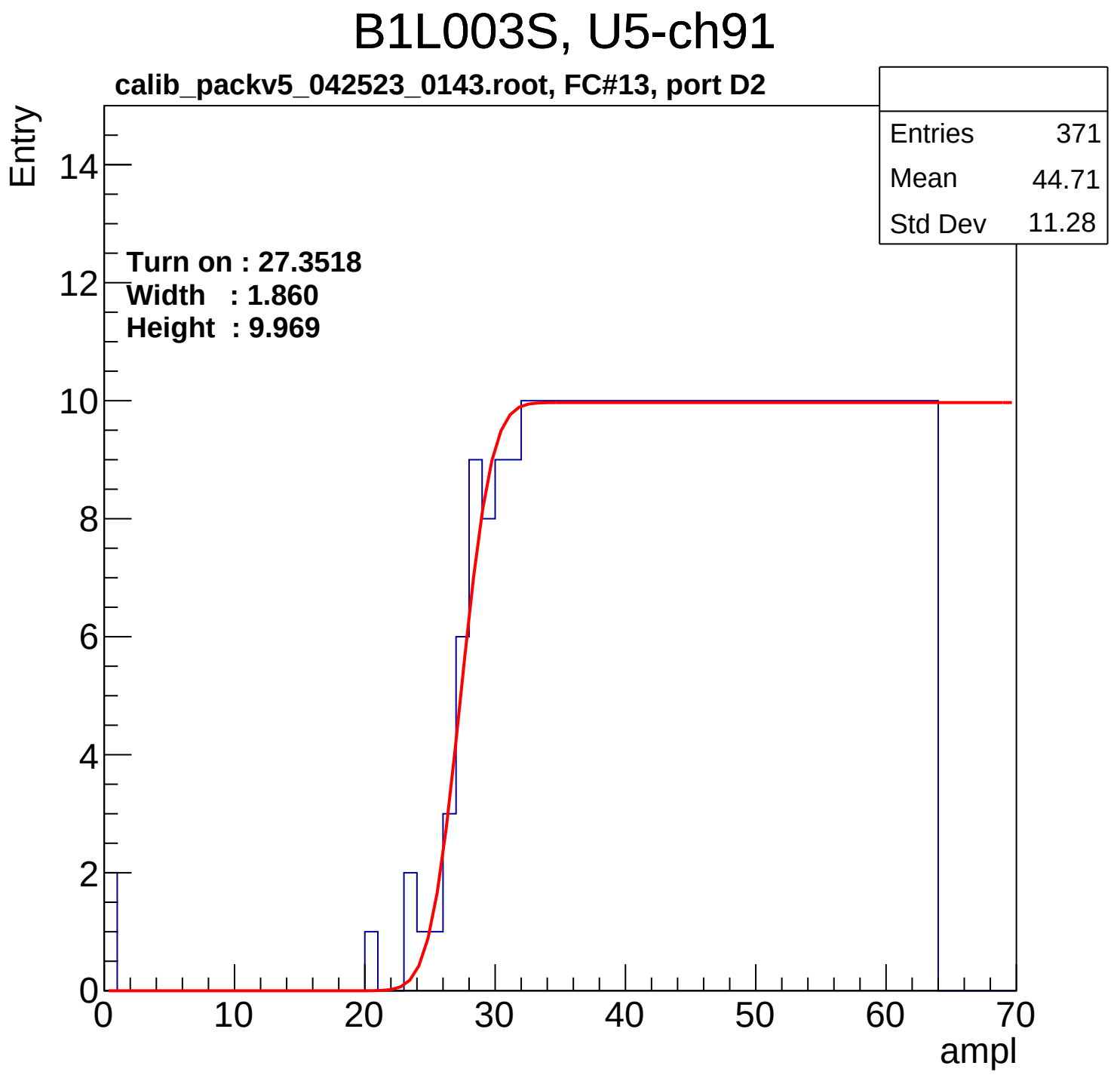
B1L003S, U5-ch91
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.71
Std Dev 11.28
Turn on : 27.3518
Width : 1.860
Height : 9.969
Entry
ampl
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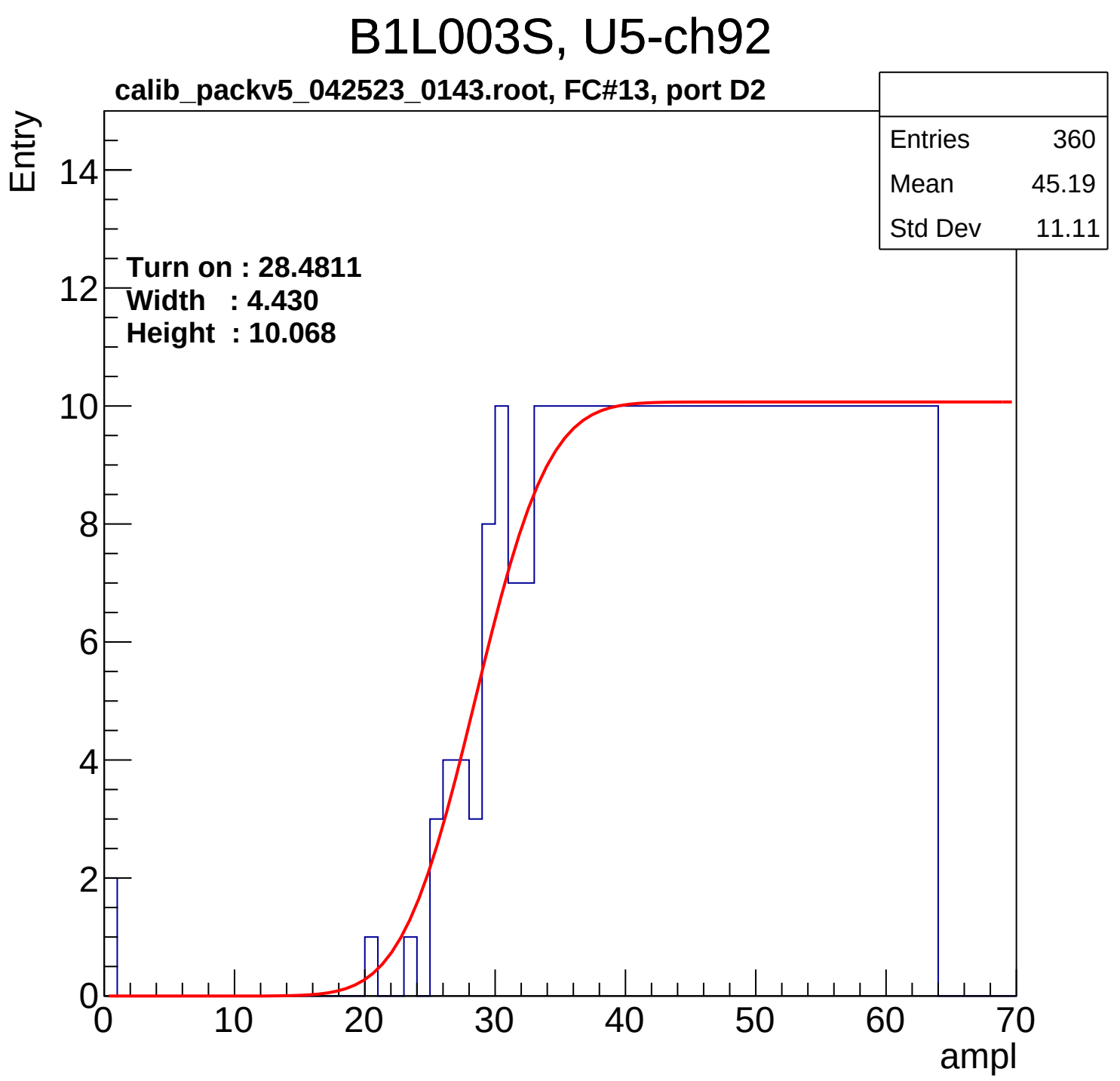
B1L003S, U5-ch92
calib_packv5_042523_0143.root, FC#13, port D2
Entries 360
Mean 45.19
Std Dev 11.11
Turn on : 28.4811
Width : 4.430
Height : 10.068
Entry
ampl
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6
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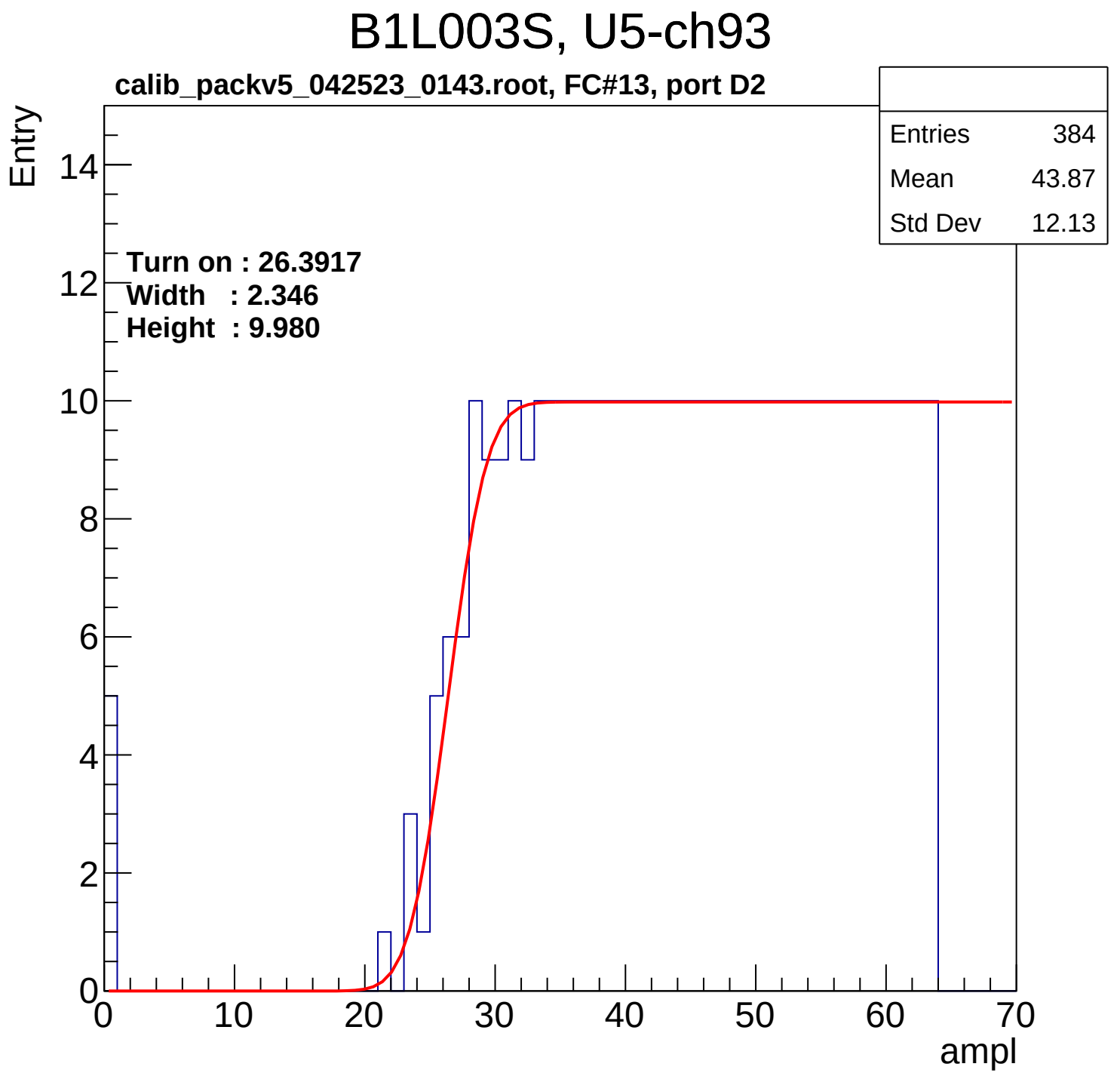
B1L003S, U5-ch93
calib_packv5_042523_0143.root, FC#13, port D2
Entries 384
Mean 43.87
Std Dev 12.13
Turn on : 26.3917
Width : 2.346
Height : 9.980
Entry
ampl
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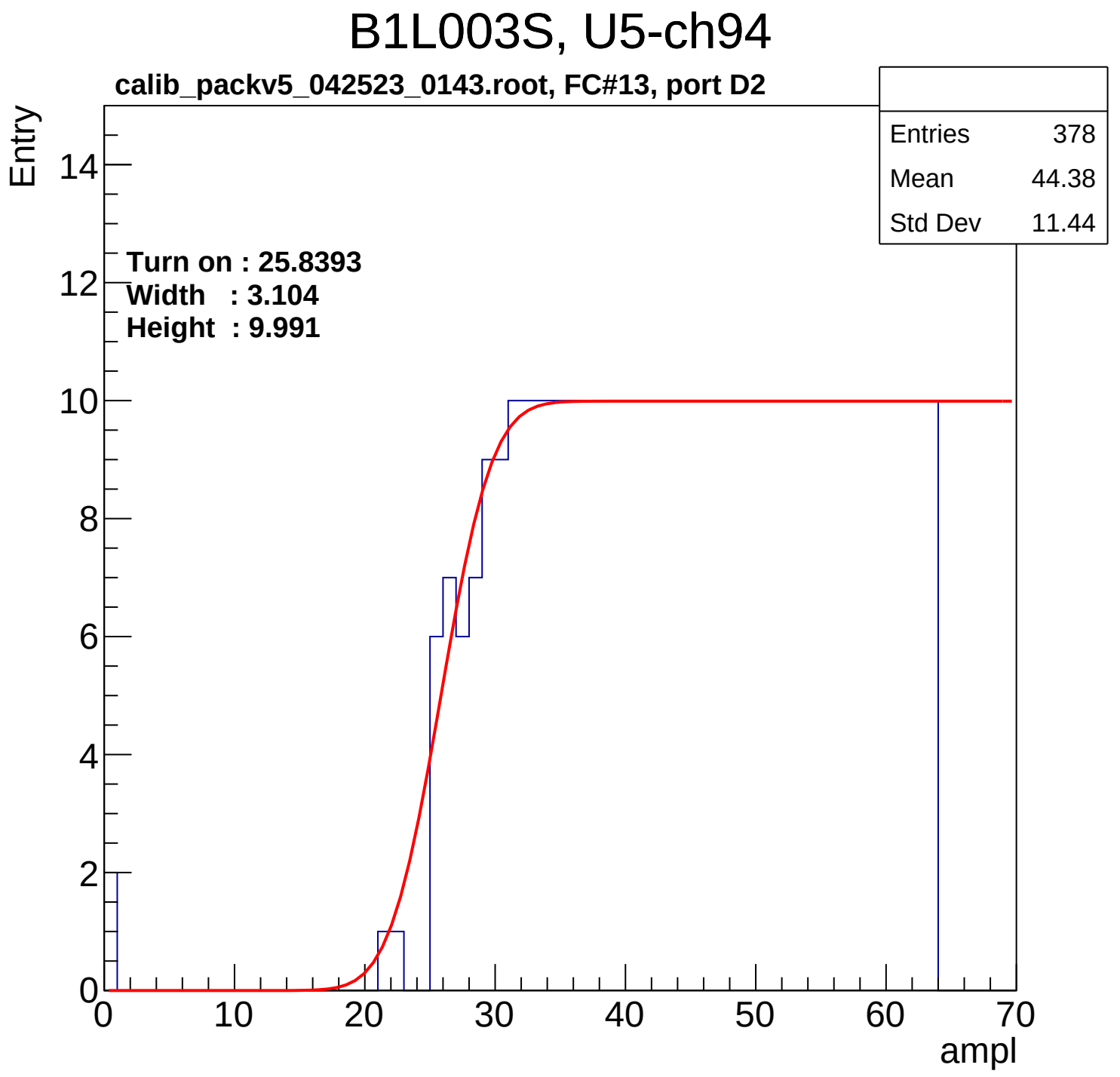
B1L003S, U5-ch94
calib_packv5_042523_0143.root, FC#13, port D2
Entries 378
Mean 44.38
Std Dev 11.44
Turn on : 25.8393
Width : 3.104
Height : 9.991
Entry
ampl
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6
8
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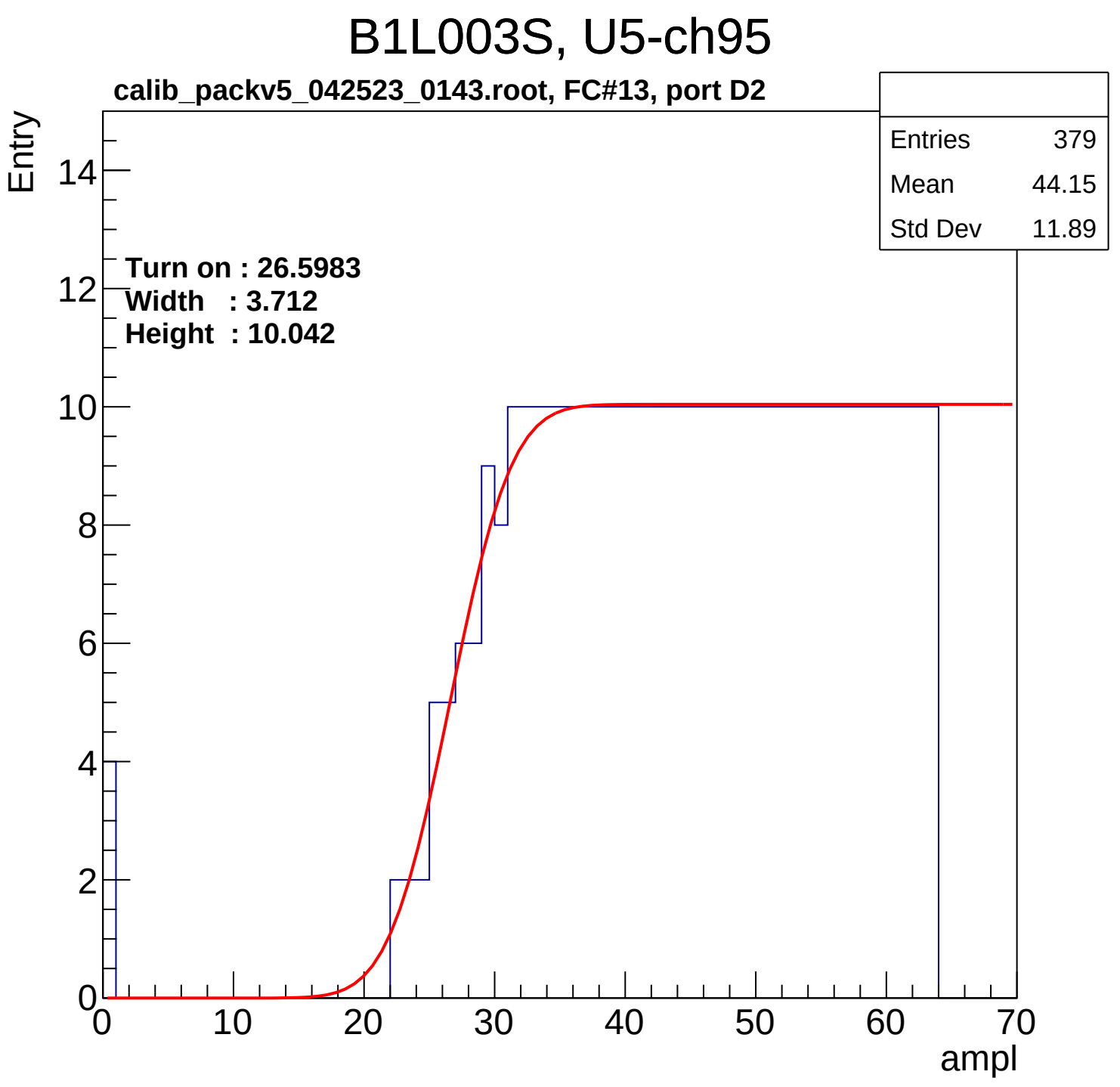
B1L003S, U5-ch95
calib_packv5_042523_0143.root, FC#13, port D2
Entries 379
Mean 44.15
Std Dev 11.89
Turn on : 26.5983
Width : 3.712
Height : 10.042
Entry
ampl
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6
8
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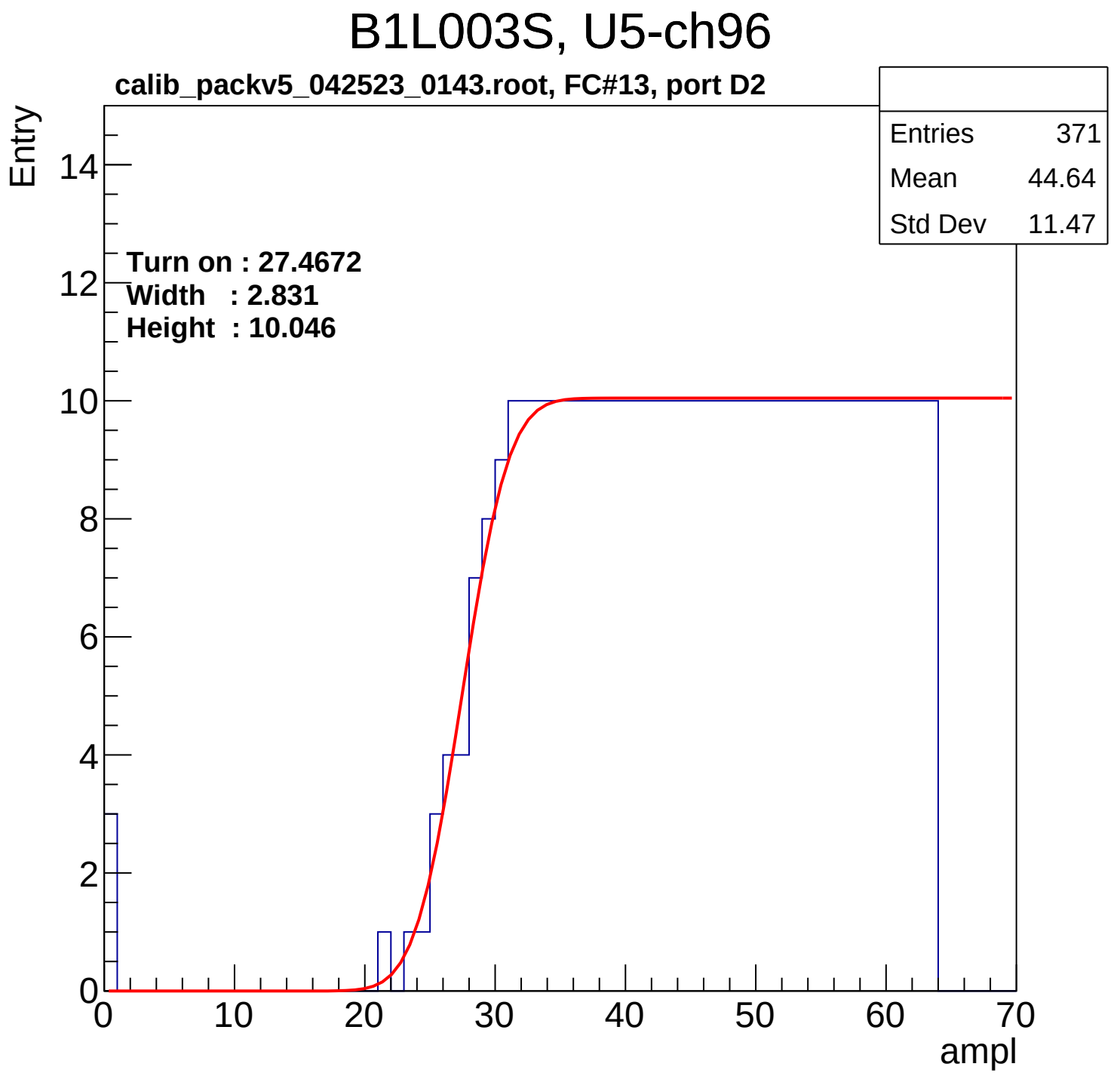
B1L003S, U5-ch96
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.64
Std Dev 11.47
Turn on : 27.4672
Width : 2.831
Height : 10.046
Entry
ampl
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6
8
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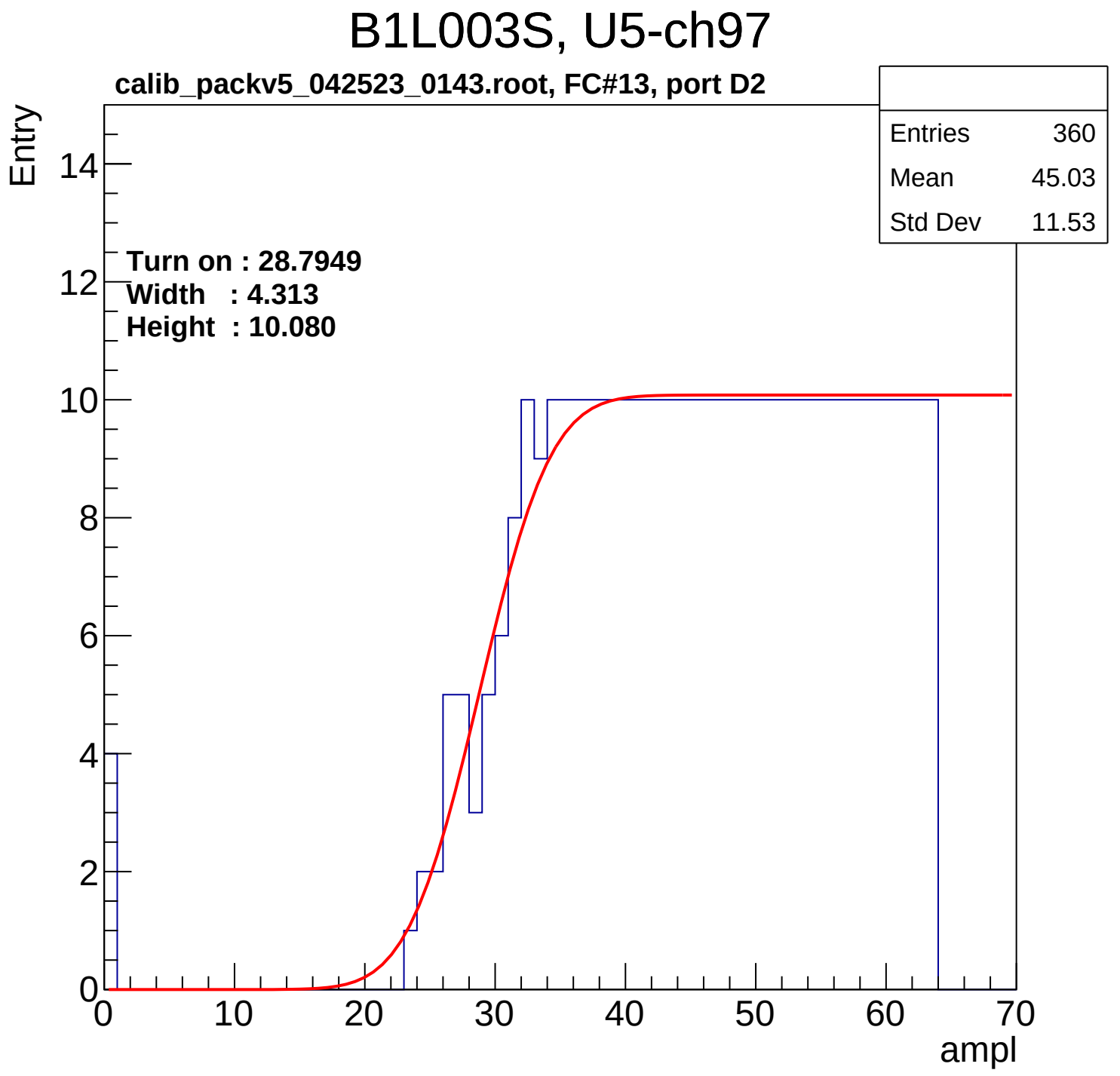
B1L003S, U5-ch97
calib_packv5_042523_0143.root, FC#13, port D2
Entries 360
Mean 45.03
Std Dev 11.53
Turn on : 28.7949
Width : 4.313
Height : 10.080
Entry
ampl
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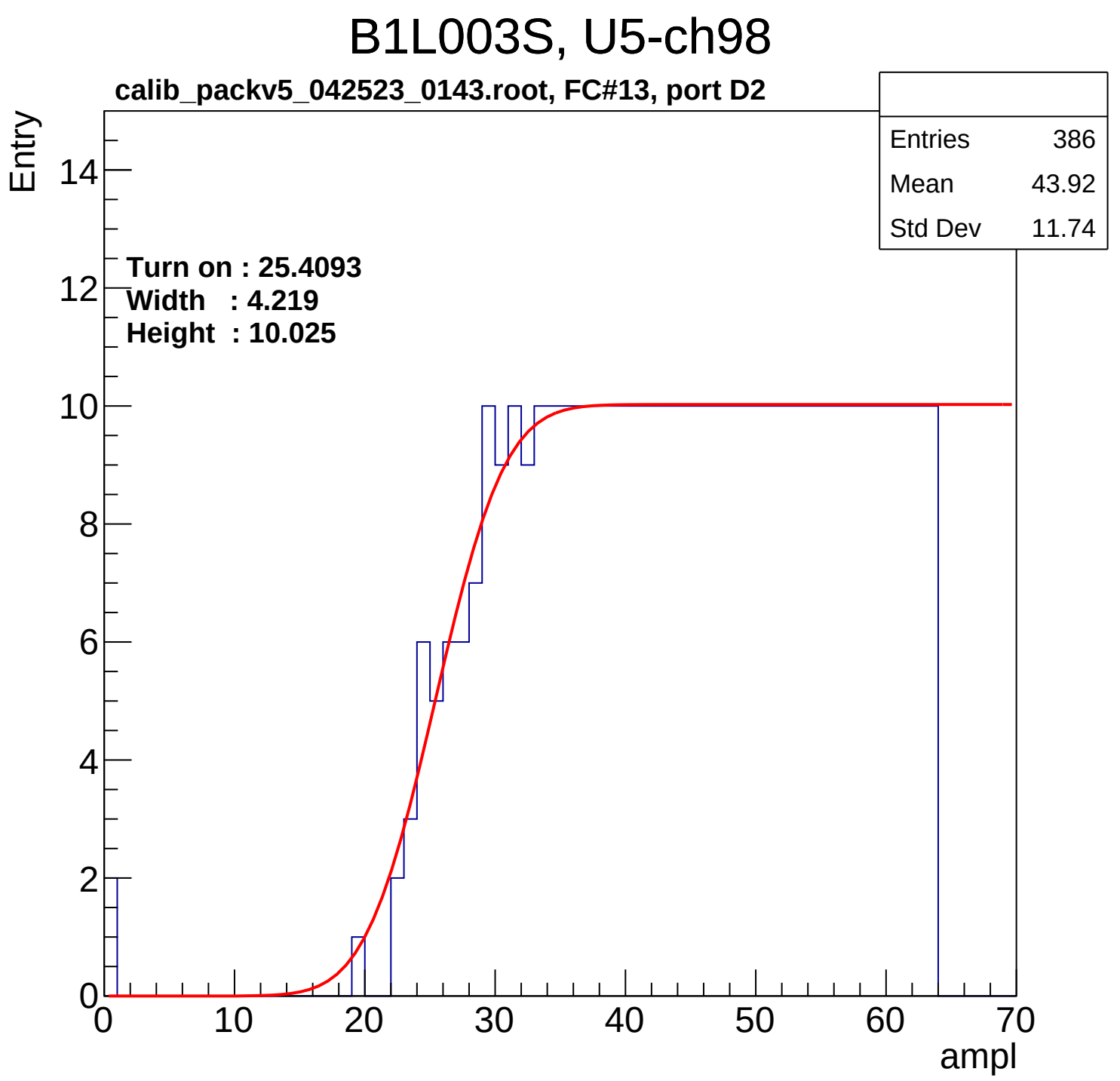
B1L003S, U5-ch98
calib_packv5_042523_0143.root, FC#13, port D2
Entries 386
Mean 43.92
Std Dev 11.74
Turn on : 25.4093
Width : 4.219
Height : 10.025
Entry
ampl
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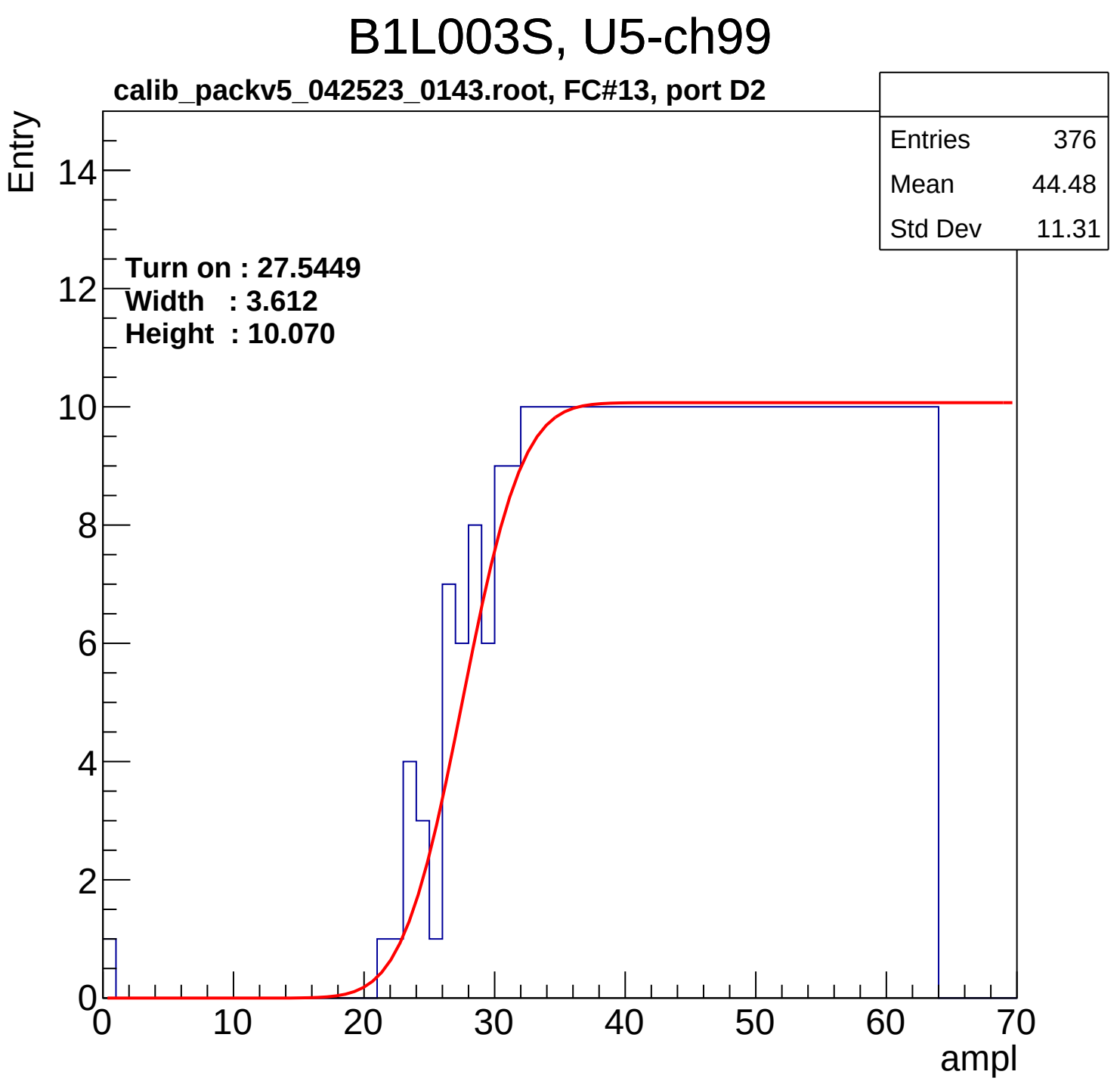
B1L003S, U5-ch99
calib_packv5_042523_0143.root, FC#13, port D2
Entries 376
Mean 44.48
Std Dev 11.31
Turn on : 27.5449
Width : 3.612
Height : 10.070
Entry
ampl
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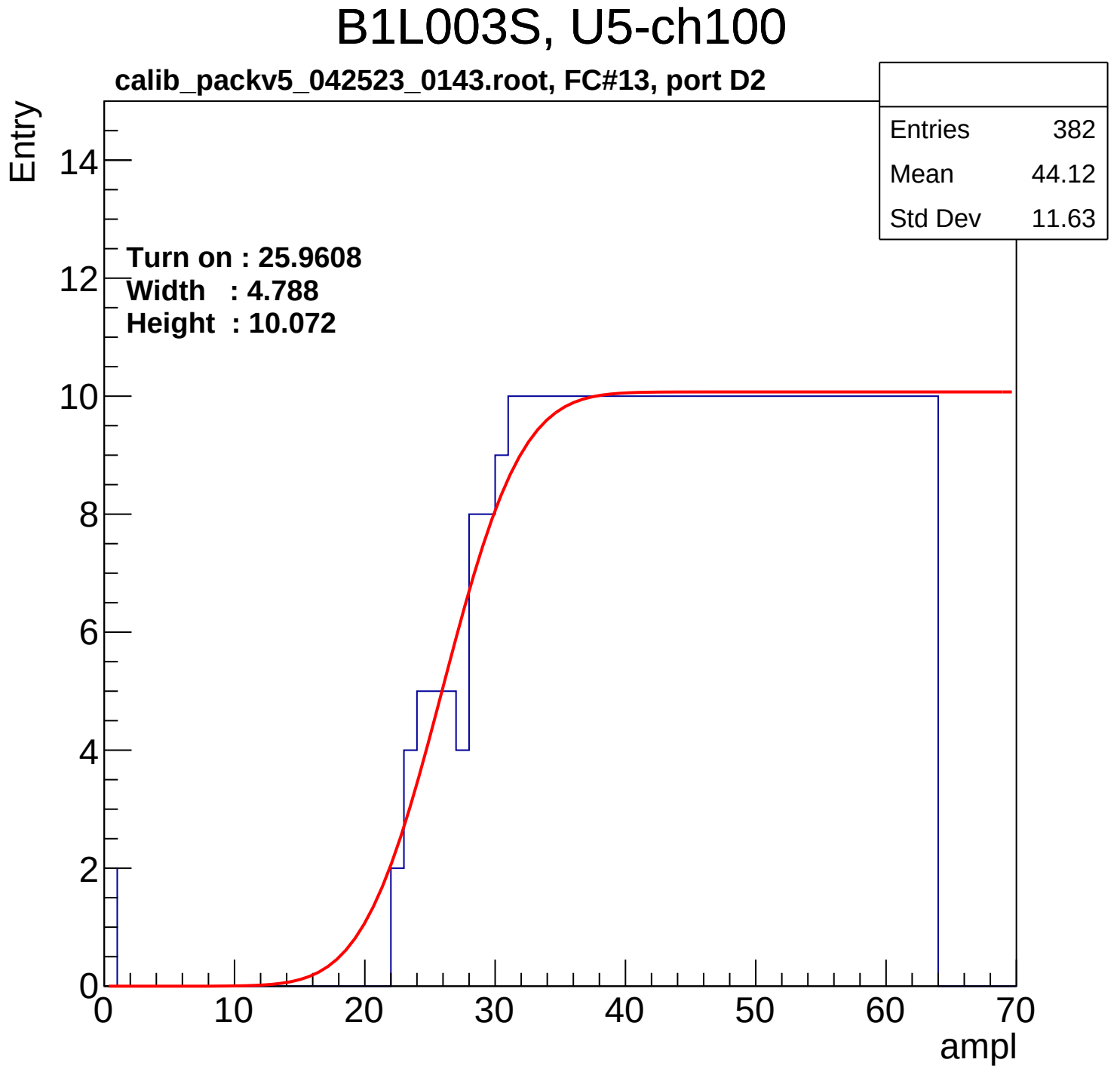
B1L003S, U5-ch100
calib_packv5_042523_0143.root, FC#13, port D2
Entries 382
Mean 44.12
Std Dev 11.63
Turn on : 25.9608
Width : 4.788
Height : 10.072
Entry
ampl
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6
8
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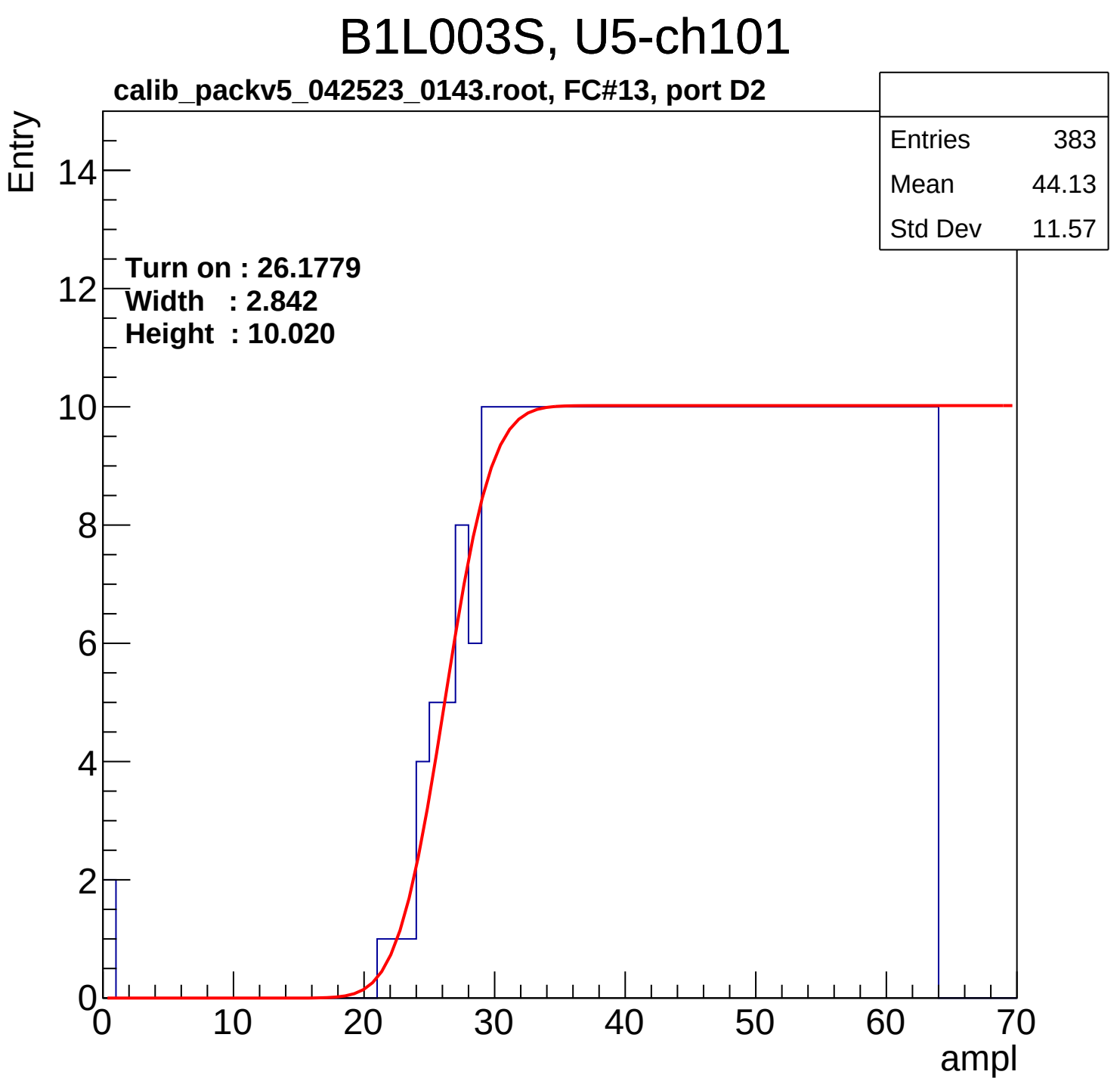
B1L003S, U5-ch101
calib_packv5_042523_0143.root, FC#13, port D2
Entries 383
Mean 44.13
Std Dev 11.57
Turn on : 26.1779
Width : 2.842
Height : 10.020
Entry
ampl
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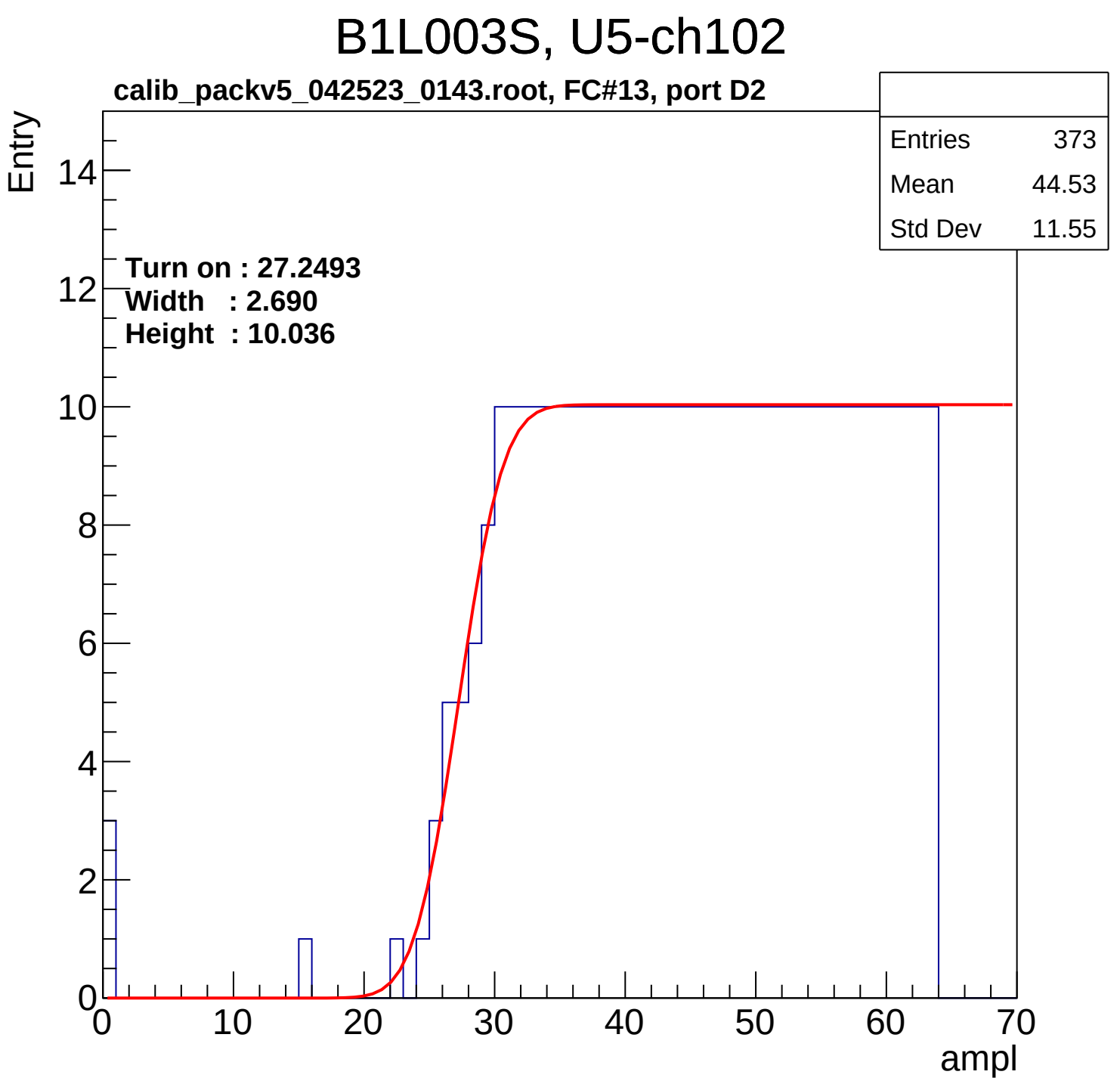
B1L003S, U5-ch102
calib_packv5_042523_0143.root, FC#13, port D2
Entries 373
Mean 44.53
Std Dev 11.55
Turn on : 27.2493
Width : 2.690
Height : 10.036
Entry
ampl
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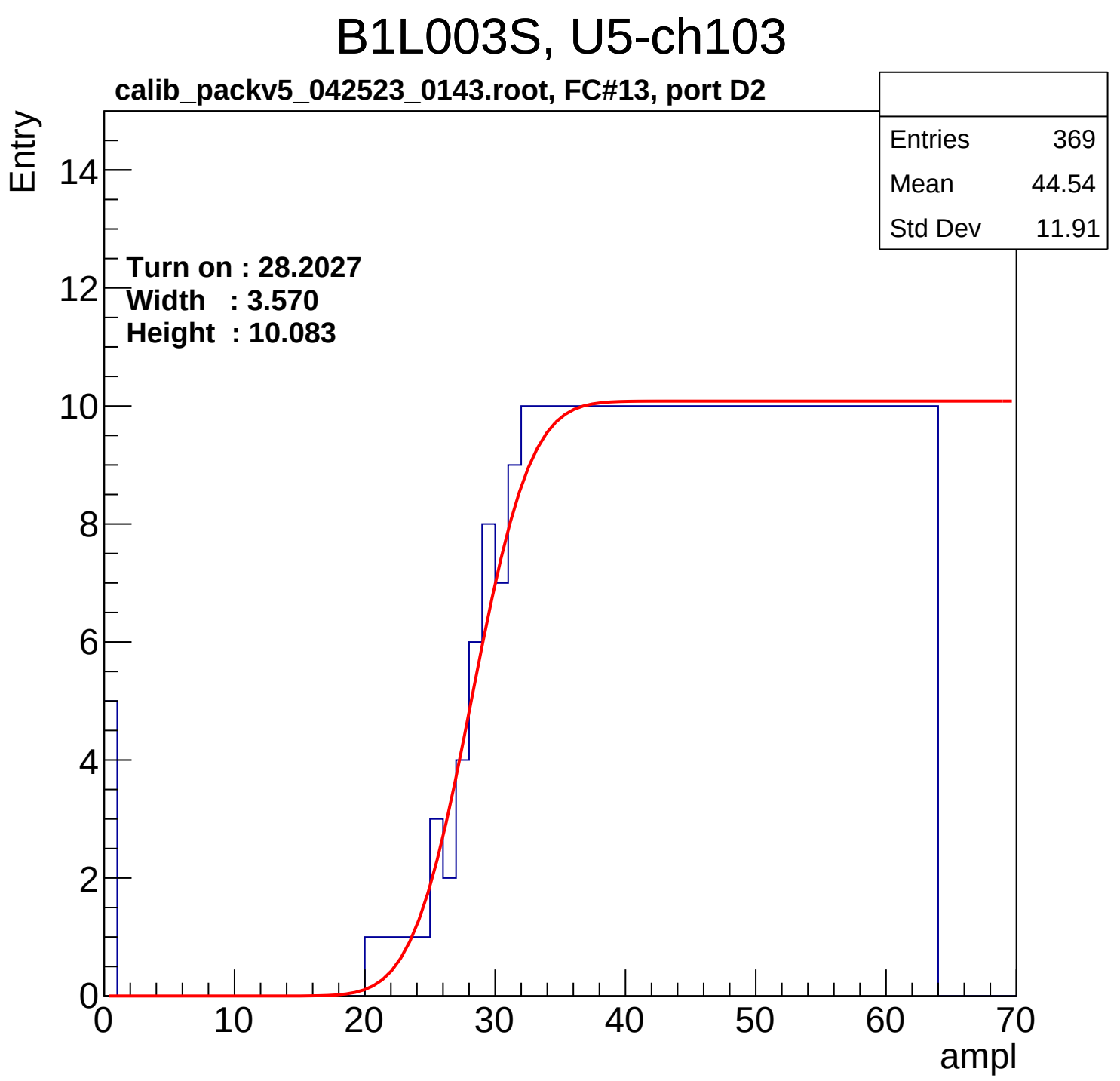
B1L003S, U5-ch103
calib_packv5_042523_0143.root, FC#13, port D2
Entries 369
Mean 44.54
Std Dev 11.91
Turn on : 28.2027
Width : 3.570
Height : 10.083
Entry
ampl
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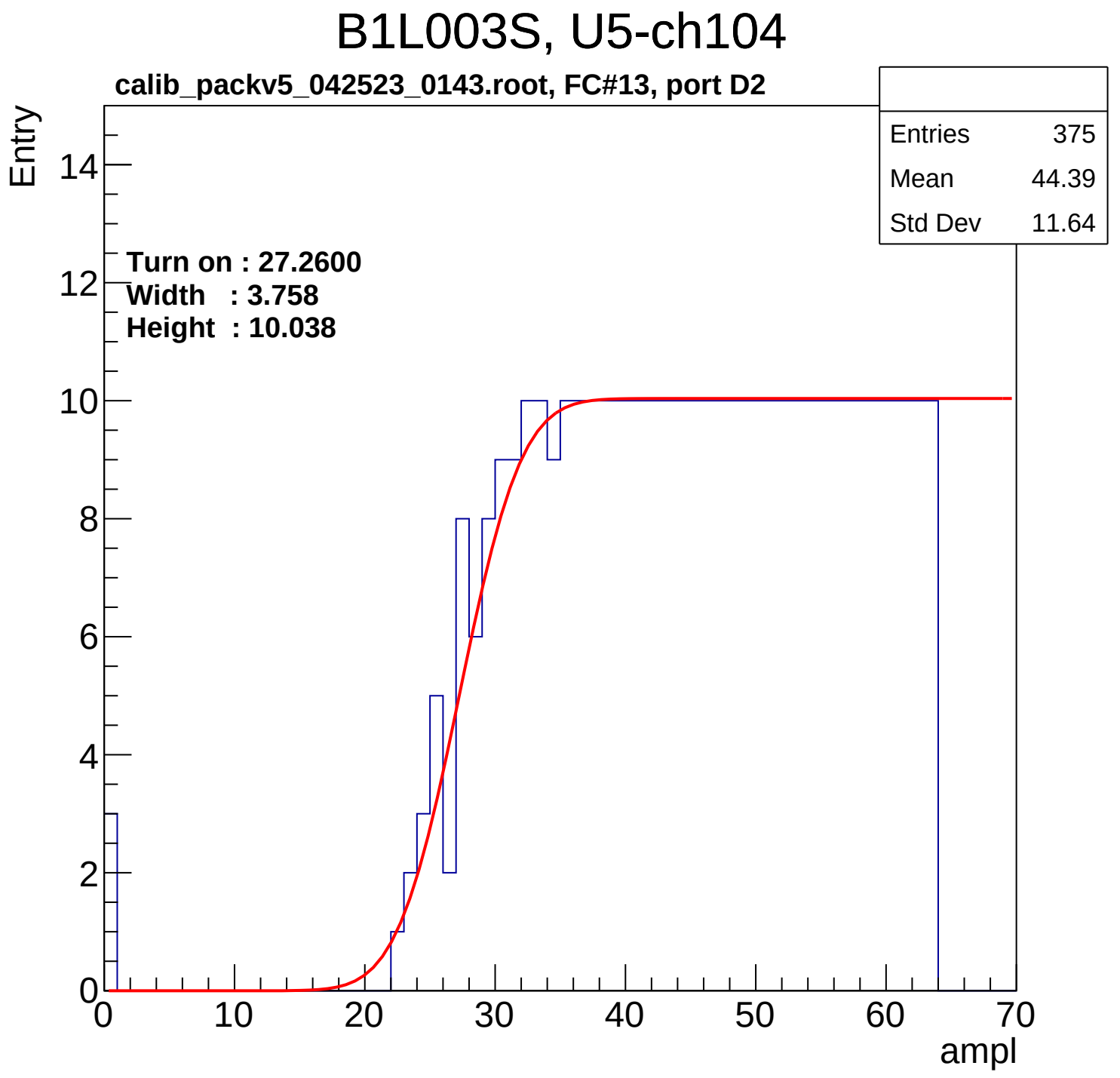
B1L003S, U5-ch104
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.39
Std Dev 11.64
Turn on : 27.2600
Width : 3.758
Height : 10.038
Entry
ampl
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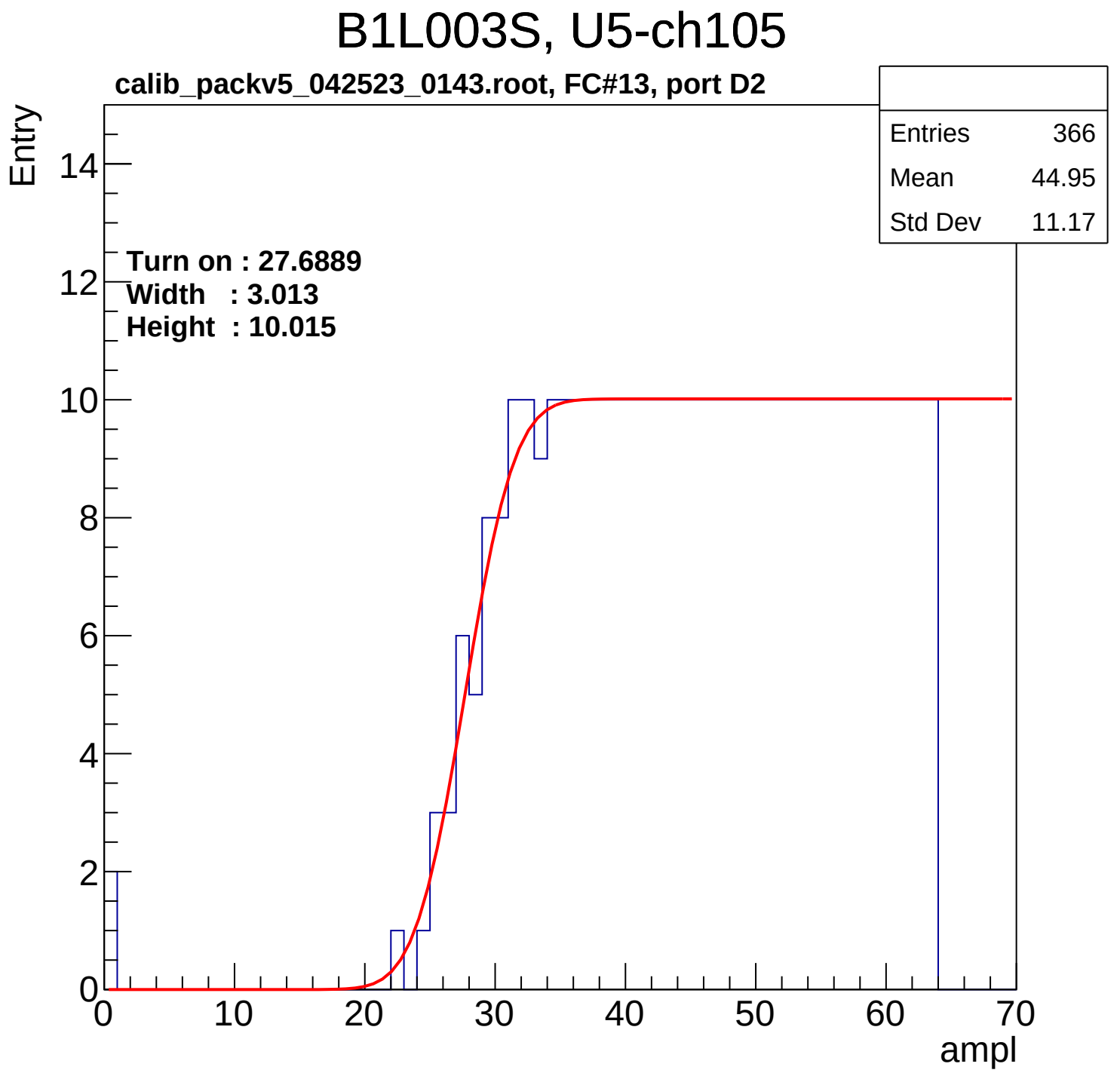
B1L003S, U5-ch105
calib_packv5_042523_0143.root, FC#13, port D2
Entries 366
Mean 44.95
Std Dev 11.17
Turn on : 27.6889
Width : 3.013
Height : 10.015
Entry
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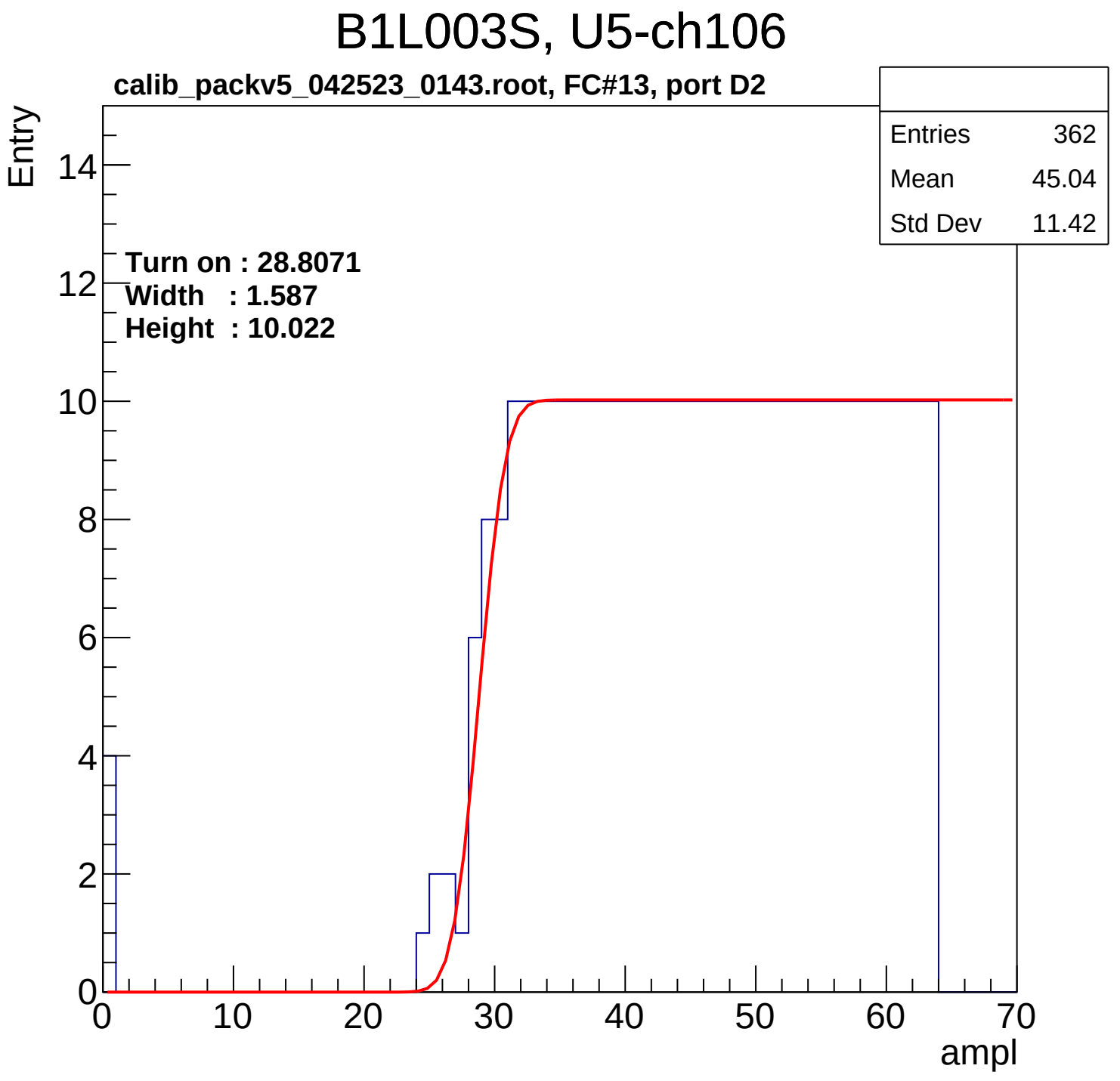
B1L003S, U5-ch106
calib_packv5_042523_0143.root, FC#13, port D2
Entries 362
Mean 45.04
Std Dev 11.42
Turn on : 28.8071
Width : 1.587
Height : 10.022
Entry
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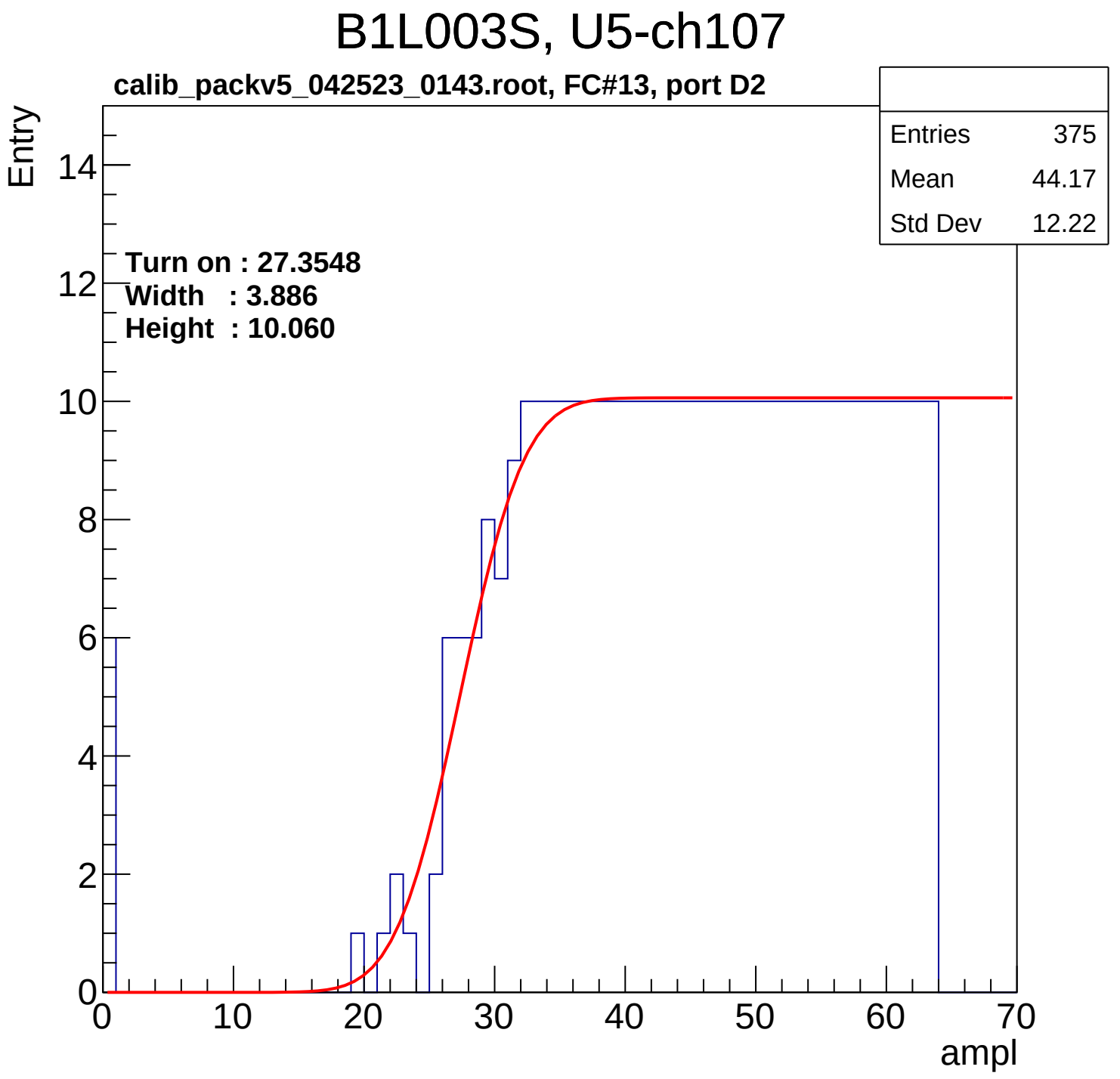
B1L003S, U5-ch107
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.17
Std Dev 12.22
Turn on : 27.3548
Width : 3.886
Height : 10.060
Entry
ampl
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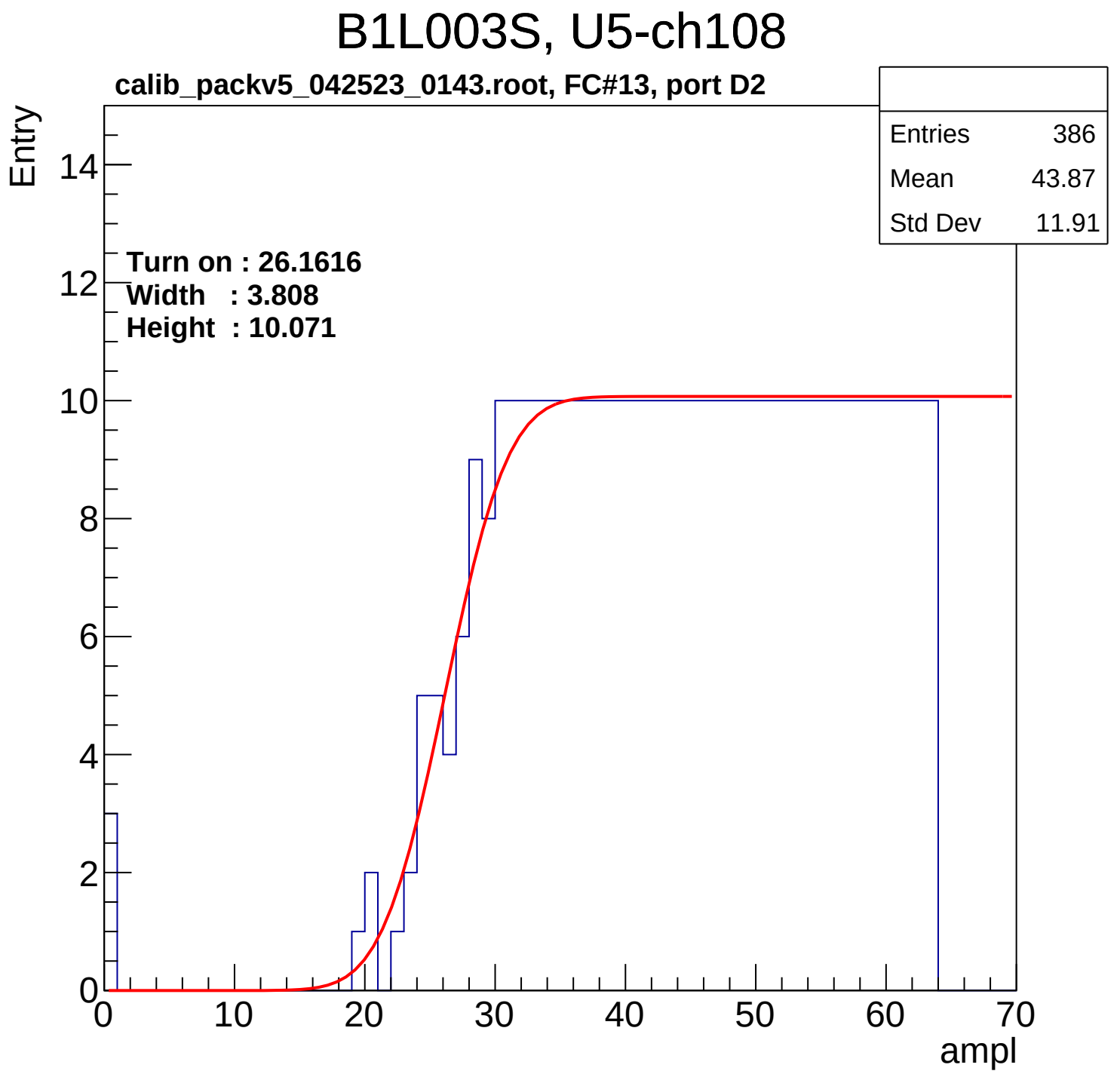
B1L003S, U5-ch108
calib_packv5_042523_0143.root, FC#13, port D2
Entries 386
Mean 43.87
Std Dev 11.91
Turn on : 26.1616
Width : 3.808
Height : 10.071
Entry
ampl
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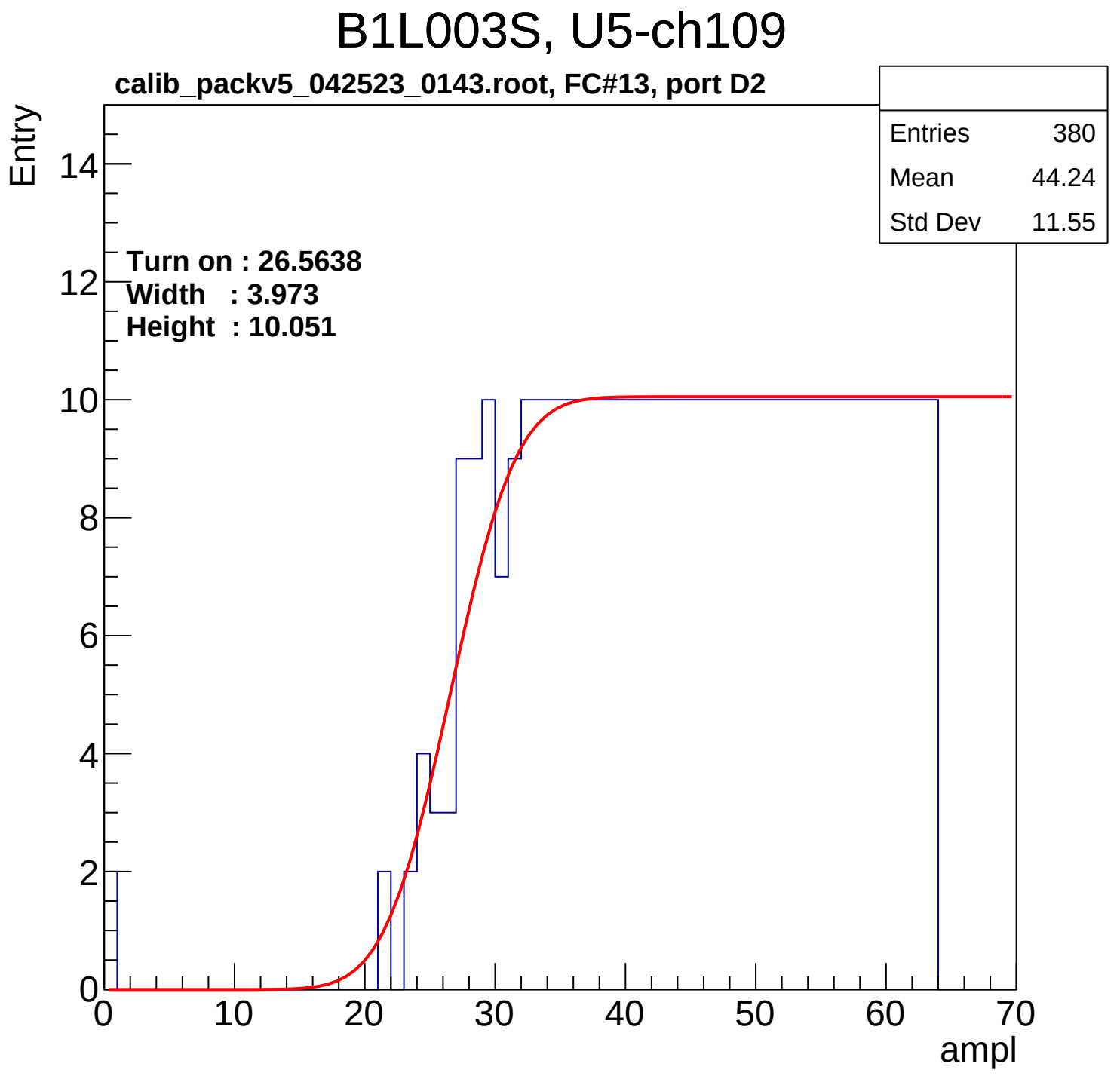
B1L003S, U5-ch109
calib_packv5_042523_0143.root, FC#13, port D2
Entries 380
Mean 44.24
Std Dev 11.55
Turn on : 26.5638
Width : 3.973
Height : 10.051
Entry
ampl
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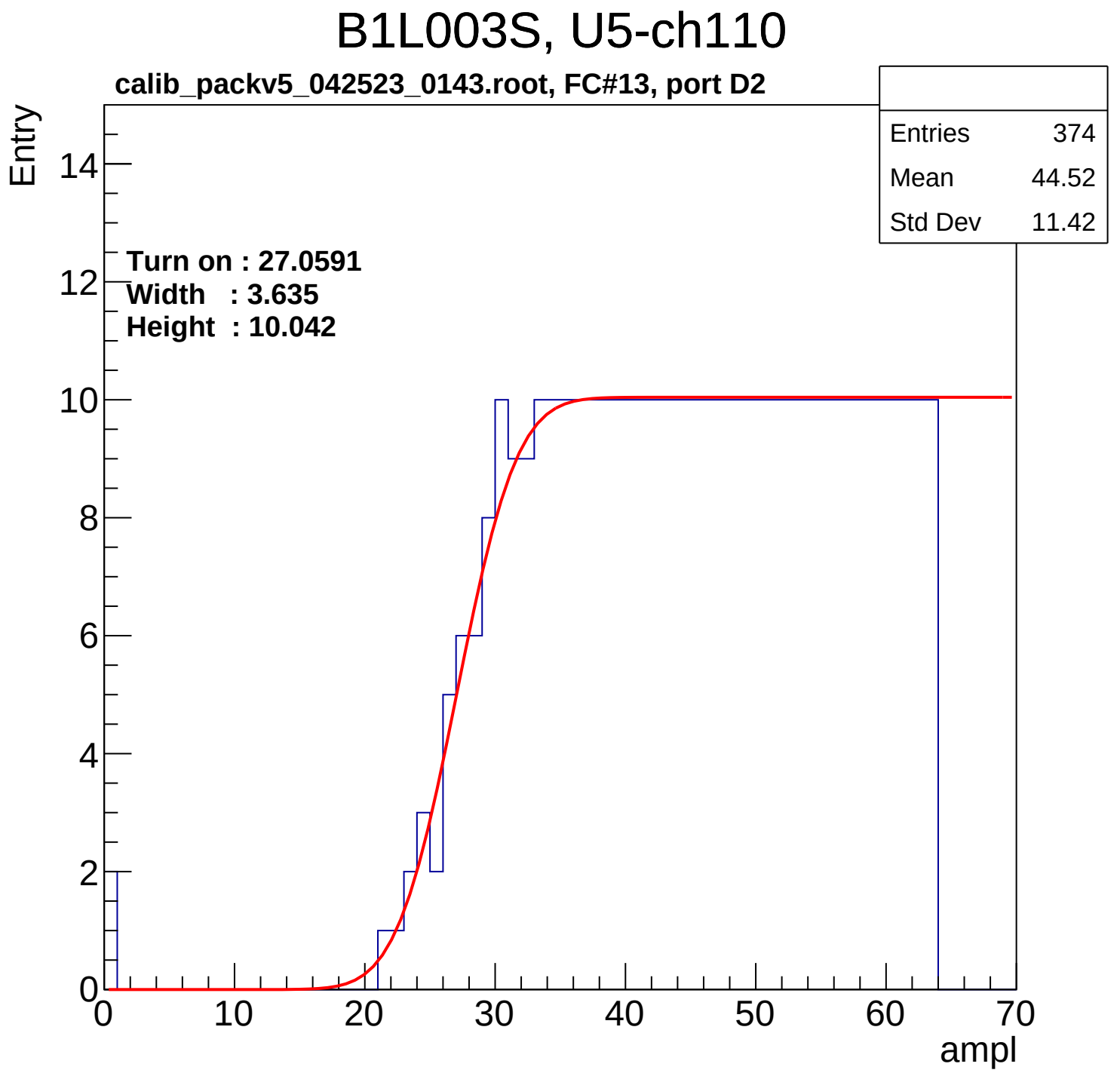
B1L003S, U5-ch110
calib_packv5_042523_0143.root, FC#13, port D2
Entries 374
Mean 44.52
Std Dev 11.42
Turn on : 27.0591
Width : 3.635
Height : 10.042
Entry
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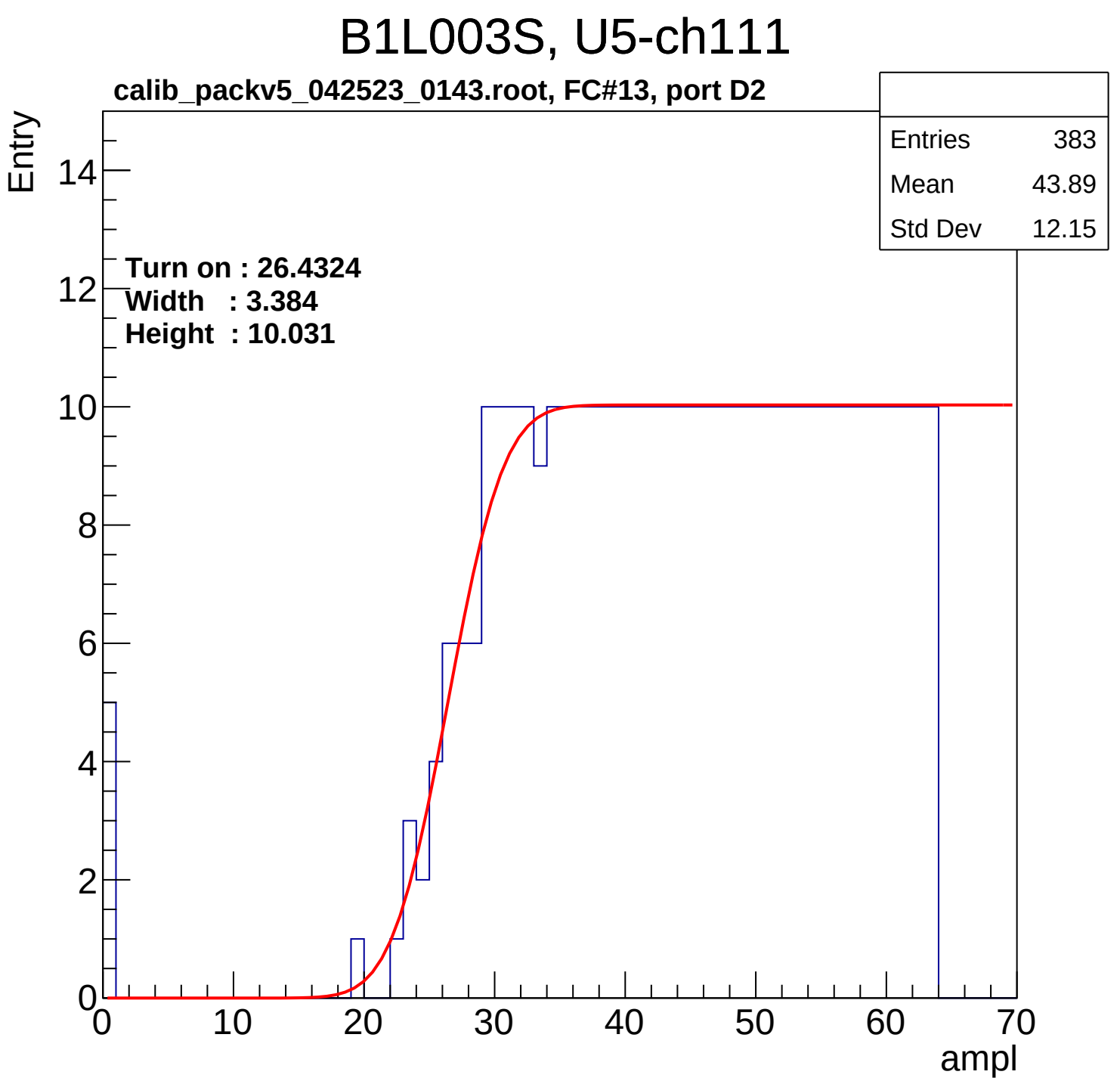
B1L003S, U5-ch111
calib_packv5_042523_0143.root, FC#13, port D2
Entries 383
Mean 43.89
Std Dev 12.15
Turn on : 26.4324
Width : 3.384
Height : 10.031
Entry
ampl
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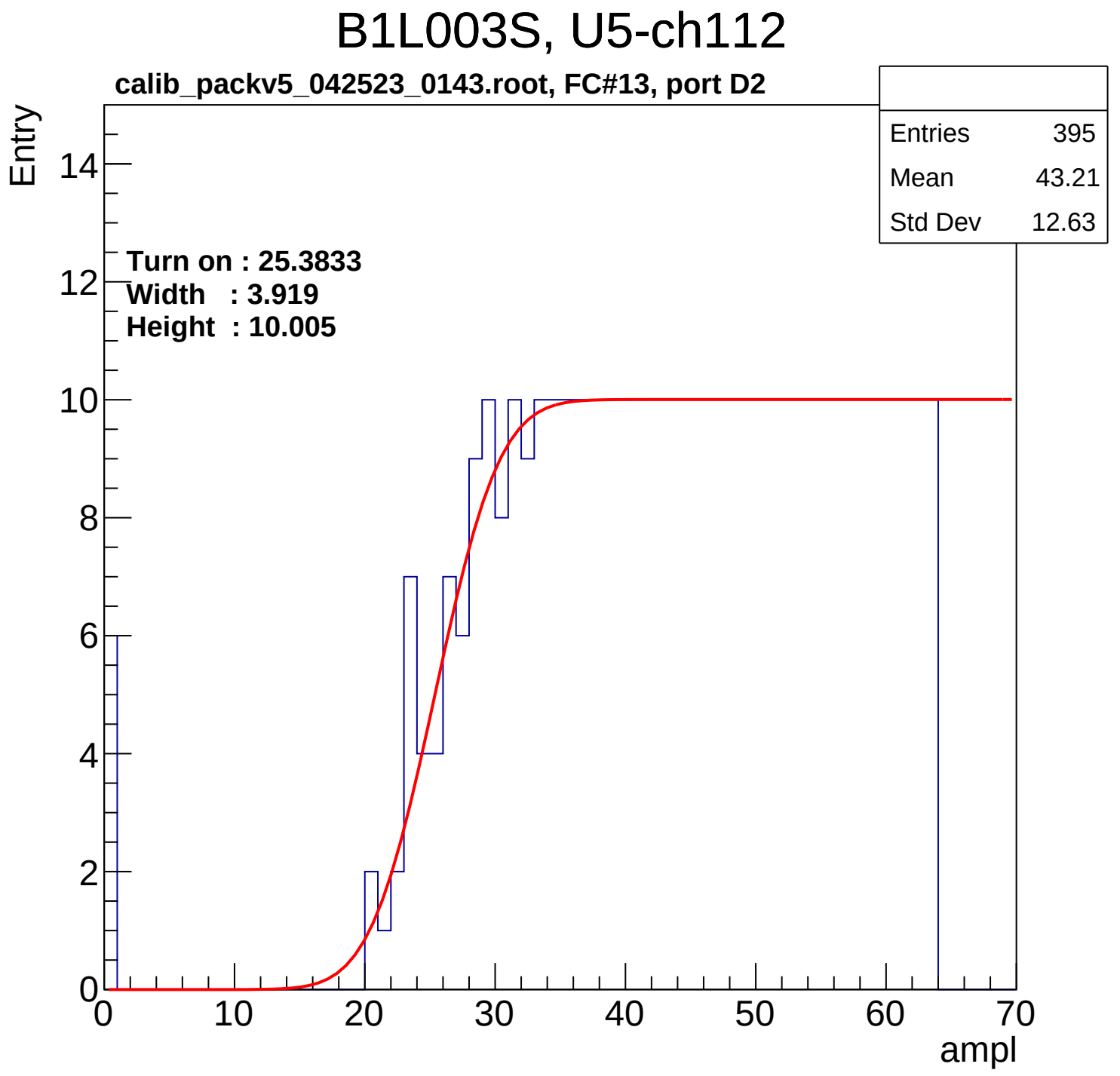
B1L003S, U5-ch112
calib_packv5_042523_0143.root, FC#13, port D2
Entries 395
Mean 43.21
Std Dev 12.63
Turn on : 25.3833
Width : 3.919
Height : 10.005
Entry
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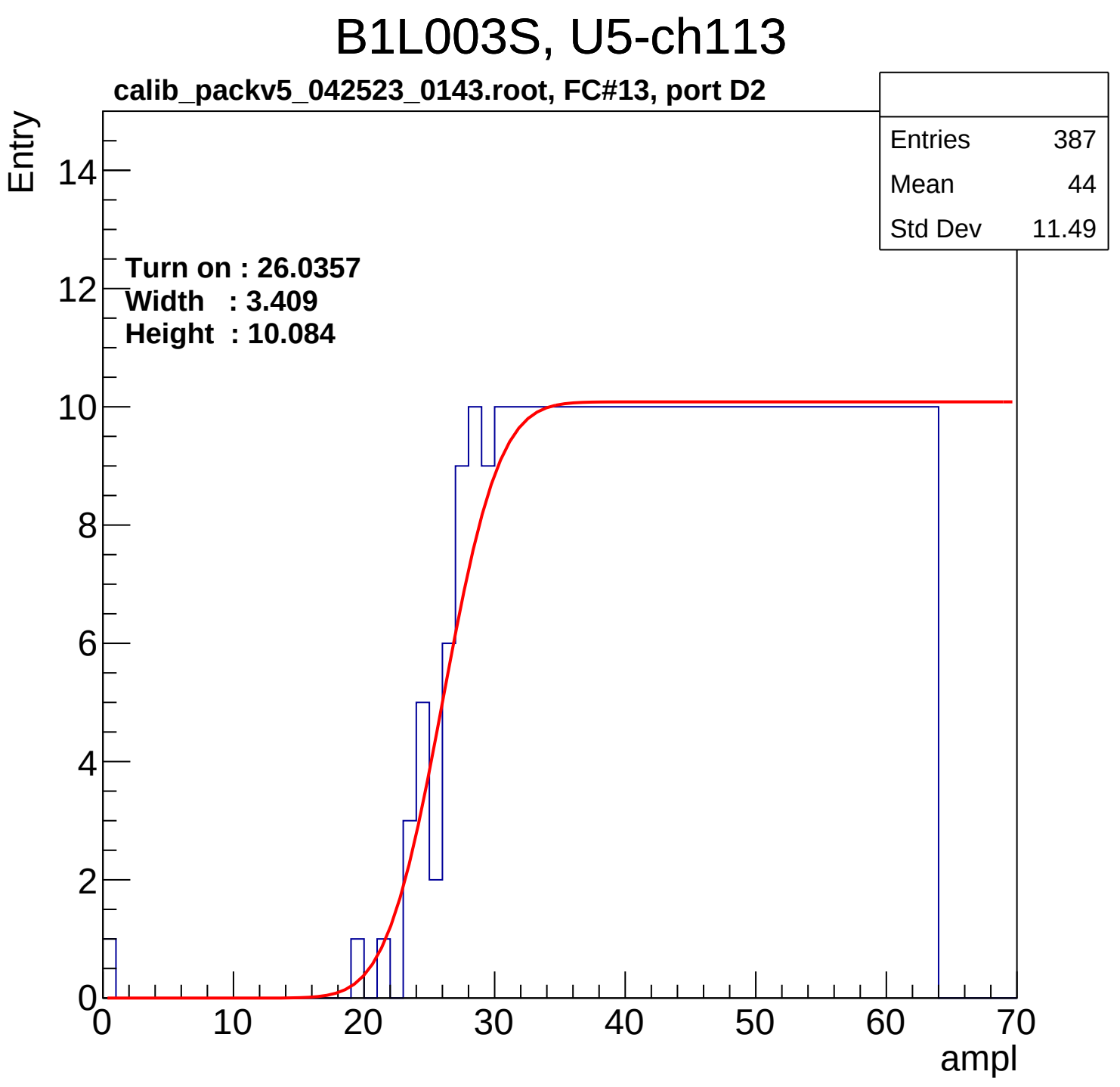
B1L003S, U5-ch113
calib_packv5_042523_0143.root, FC#13, port D2
Entries 387
Mean 44
Std Dev 11.49
Turn on : 26.0357
Width : 3.409
Height : 10.084
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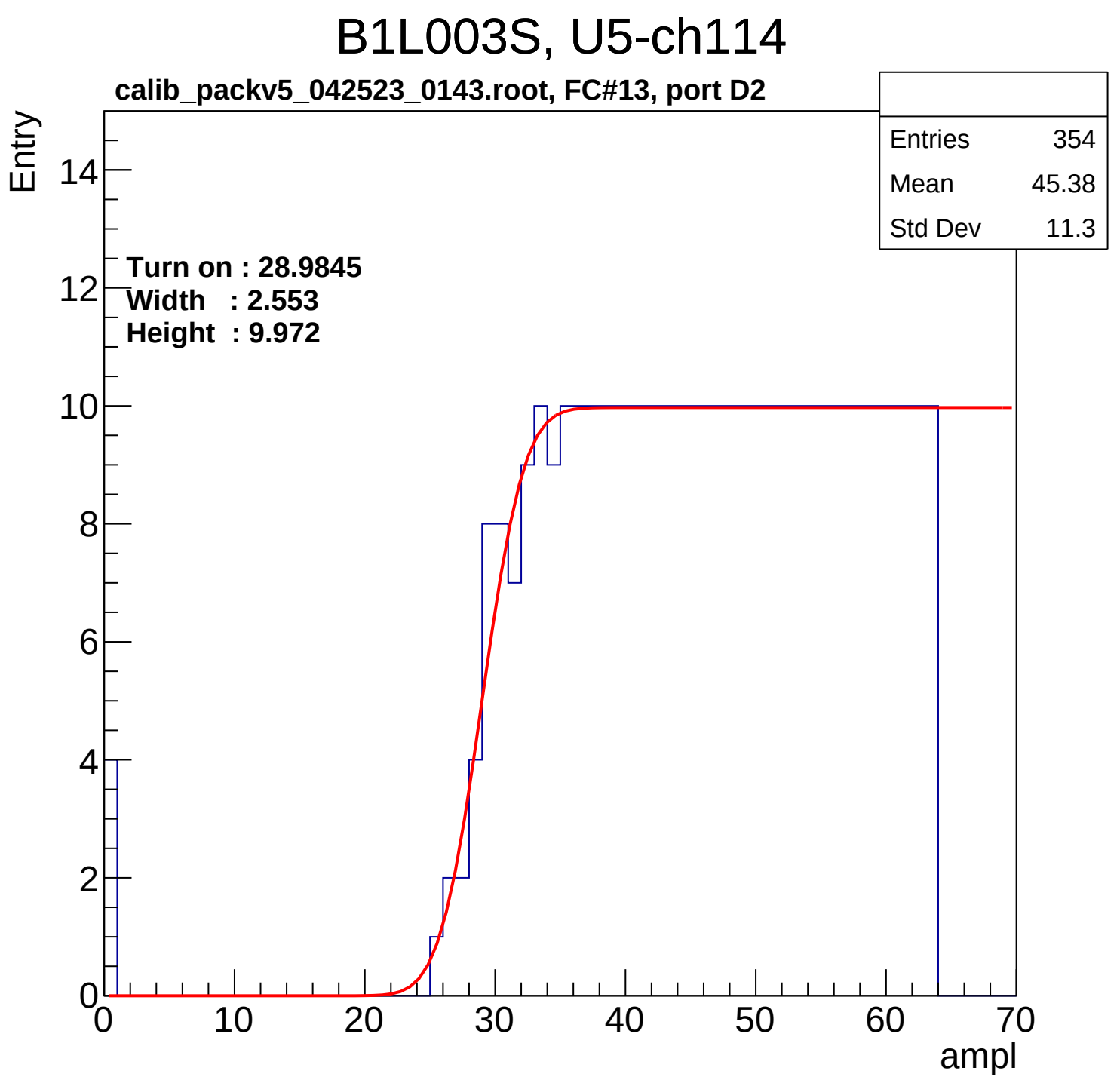
B1L003S, U5-ch114
calib_packv5_042523_0143.root, FC#13, port D2
Entries 354
Mean 45.38
Std Dev 11.3
Turn on : 28.9845
Width : 2.553
Height : 9.972
Entry
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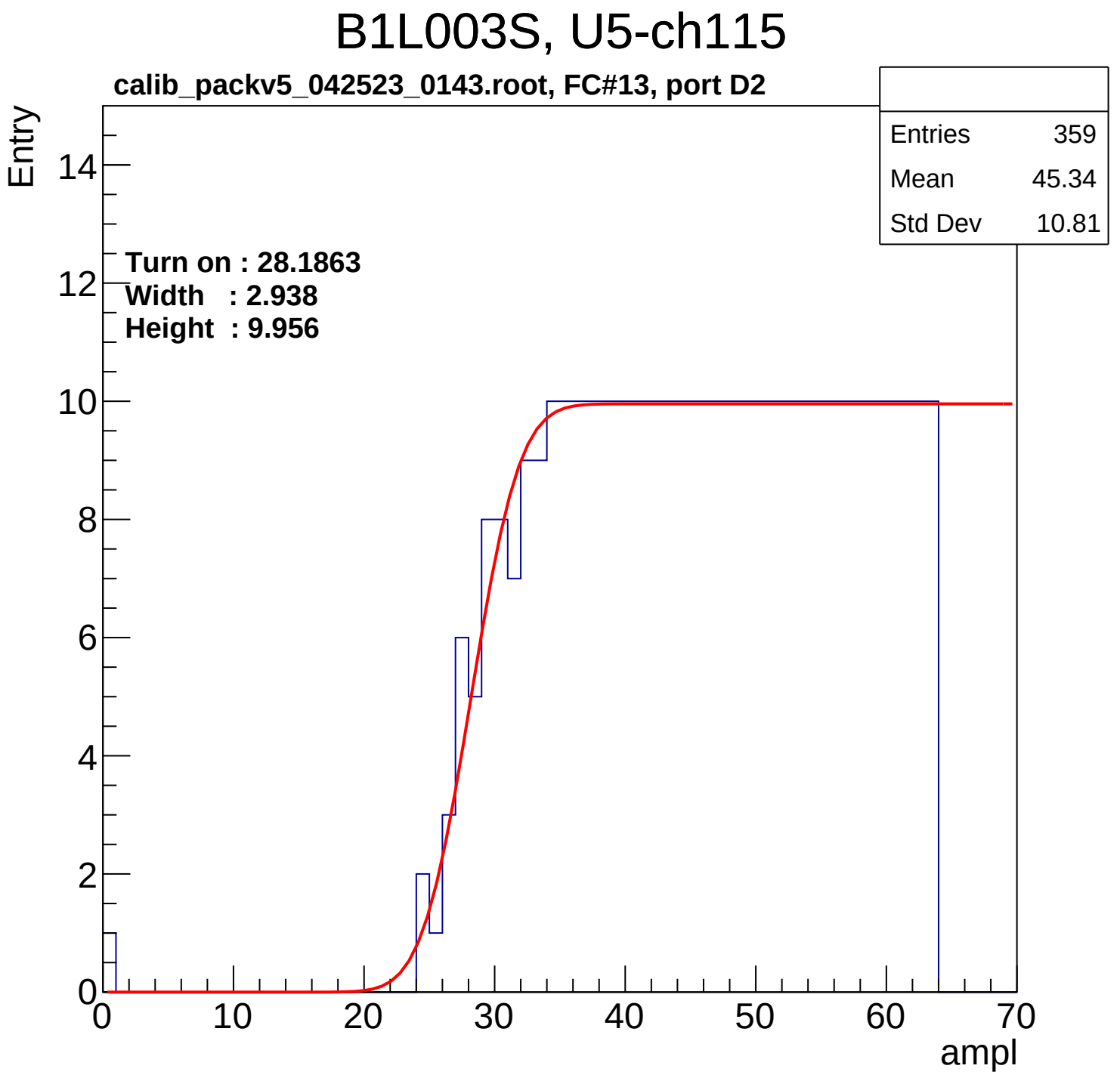
B1L003S, U5-ch115
calib_packv5_042523_0143.root, FC#13, port D2
Entries 359
Mean 45.34
Std Dev 10.81
Turn on : 28.1863
Width : 2.938
Height : 9.956
Entry
ampl
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4
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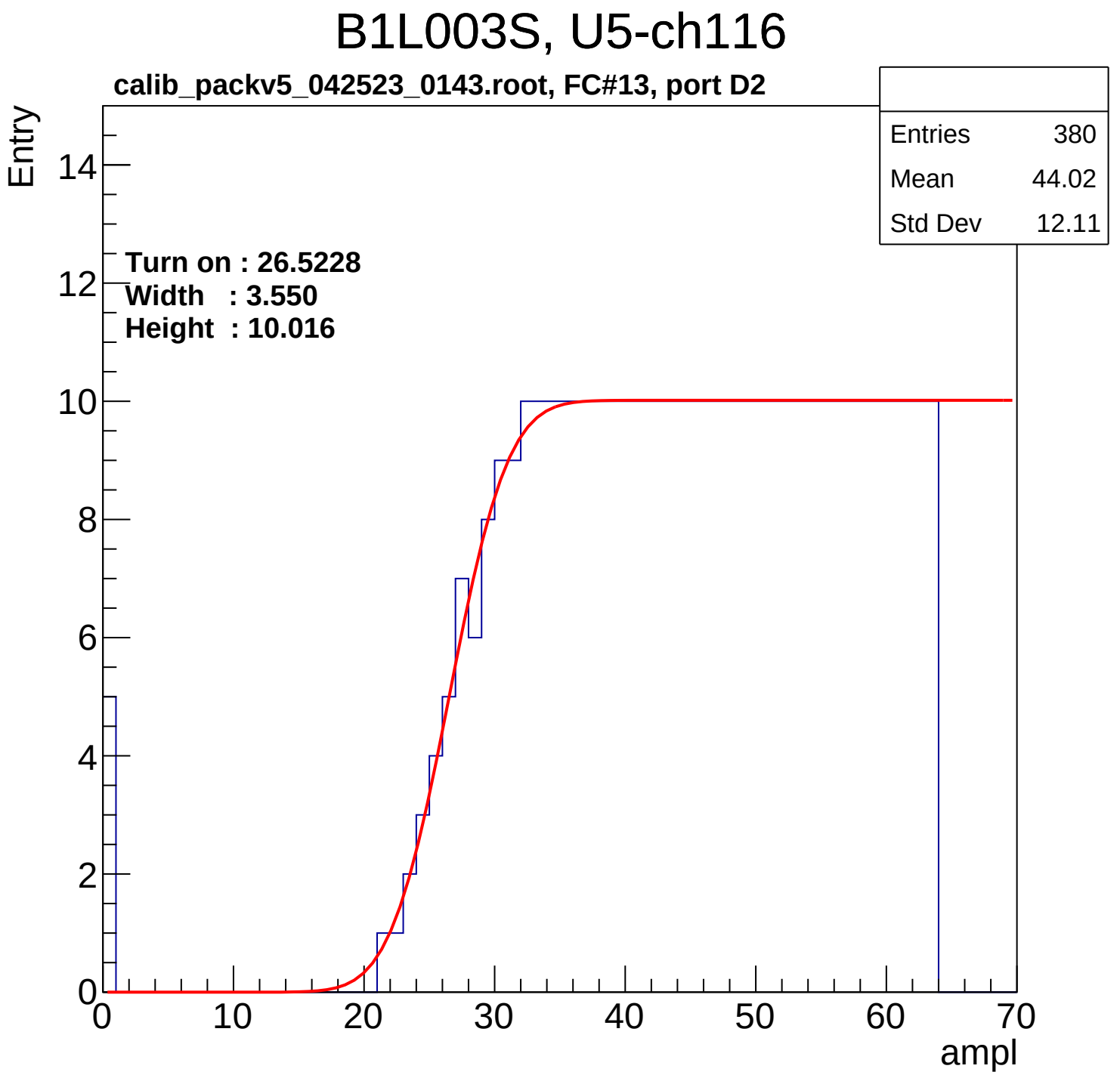
B1L003S, U5-ch116
calib_packv5_042523_0143.root, FC#13, port D2
Entries 380
Mean 44.02
Std Dev 12.11
Turn on : 26.5228
Width : 3.550
Height : 10.016
Entry
ampl
0
2
4
6
8
10
12
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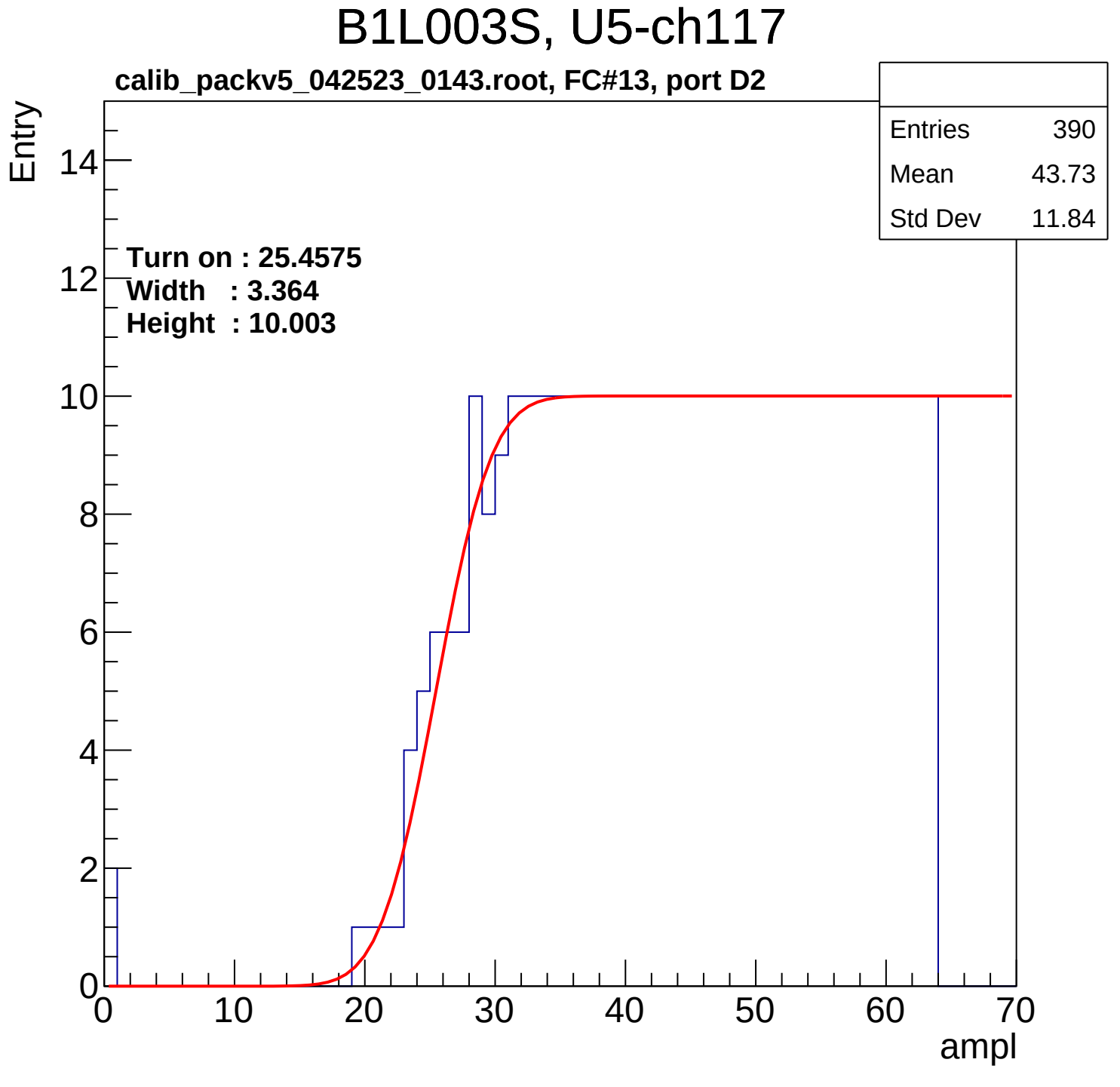
B1L003S, U5-ch117
calib_packv5_042523_0143.root, FC#13, port D2
Entries 390
Mean 43.73
Std Dev 11.84
Turn on : 25.4575
Width : 3.364
Height : 10.003
Entry
ampl
0
2
4
6
8
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12
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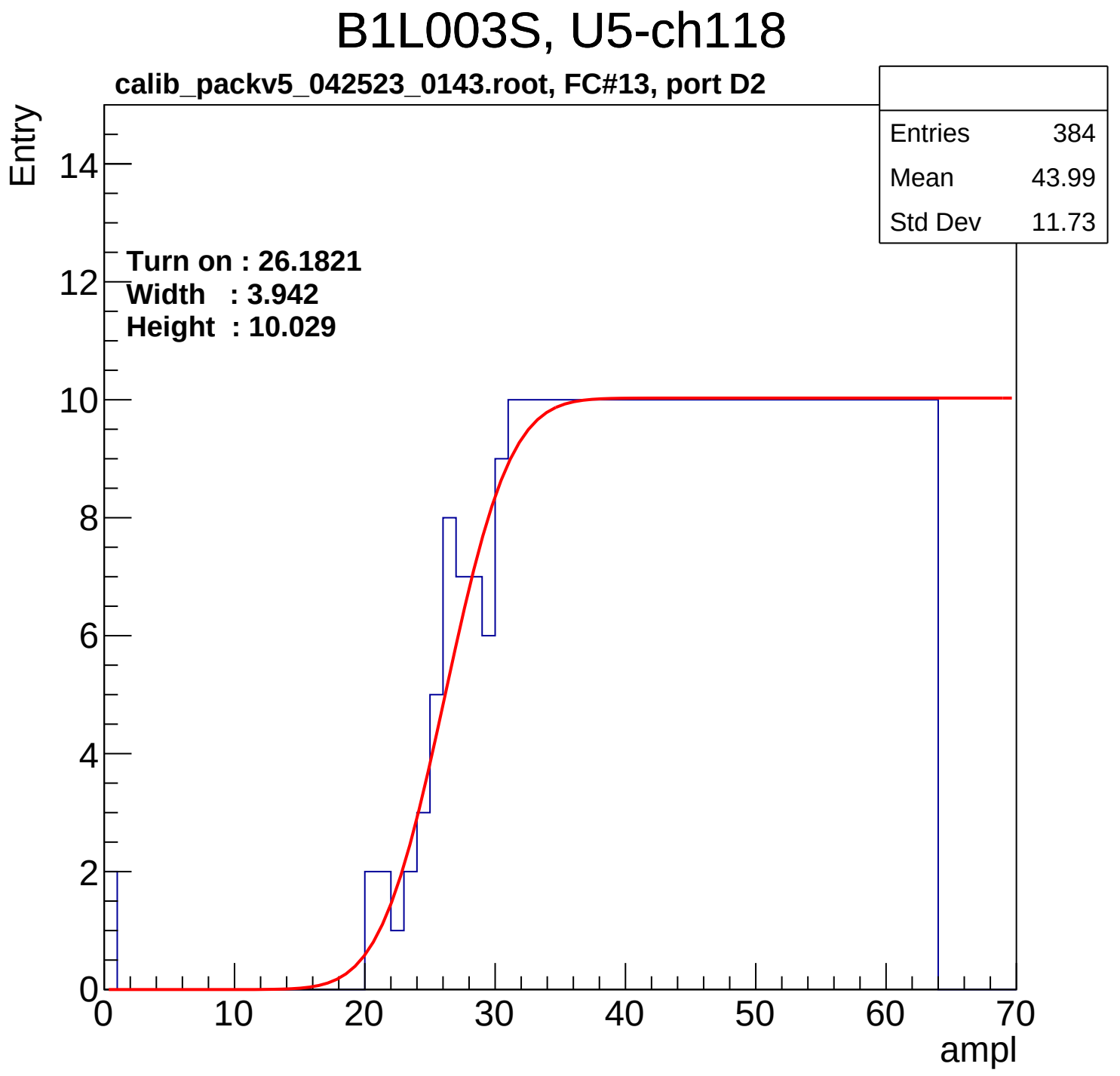
B1L003S, U5-ch118
calib_packv5_042523_0143.root, FC#13, port D2
Entries 384
Mean 43.99
Std Dev 11.73
Turn on : 26.1821
Width : 3.942
Height : 10.029
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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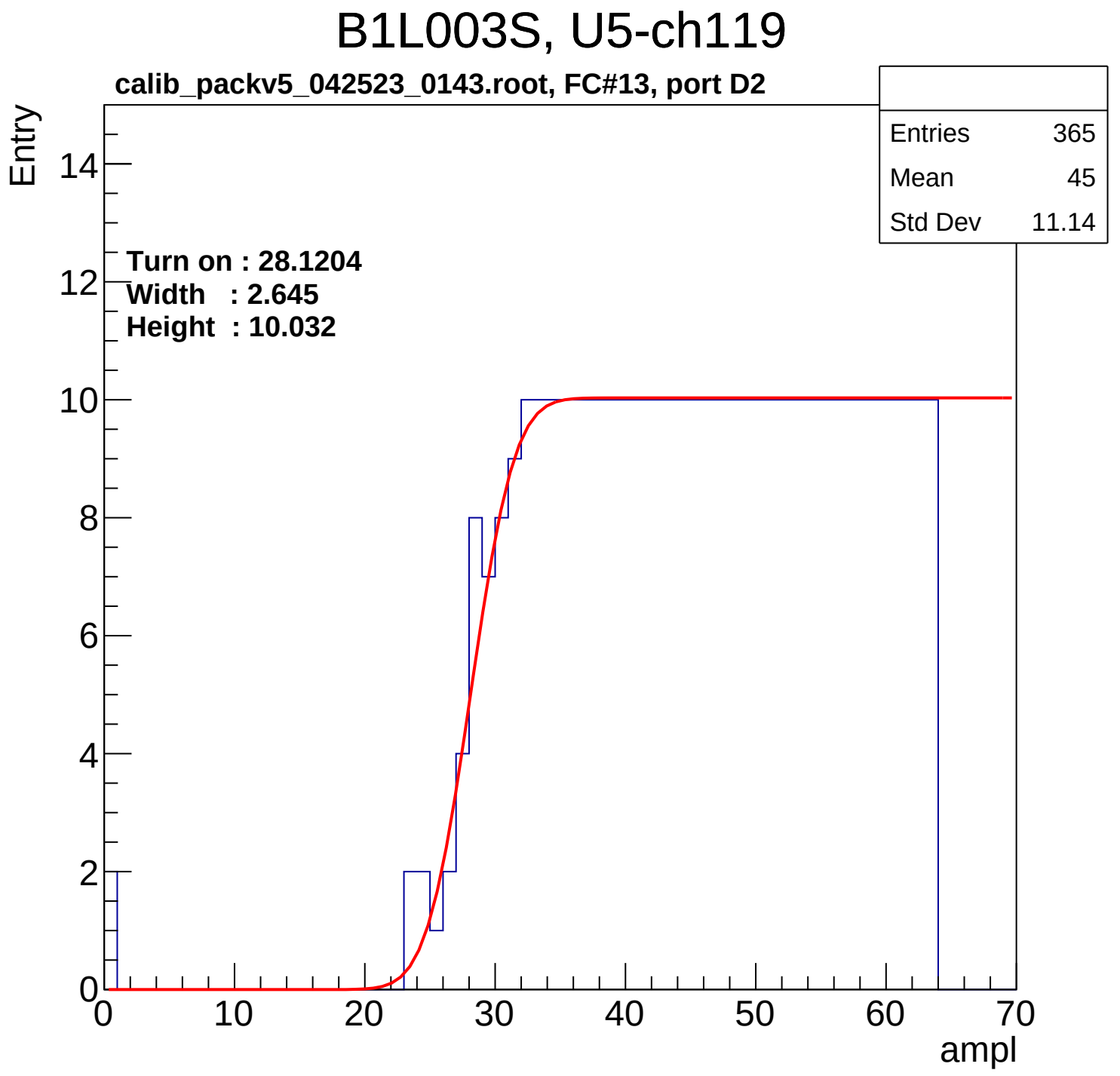
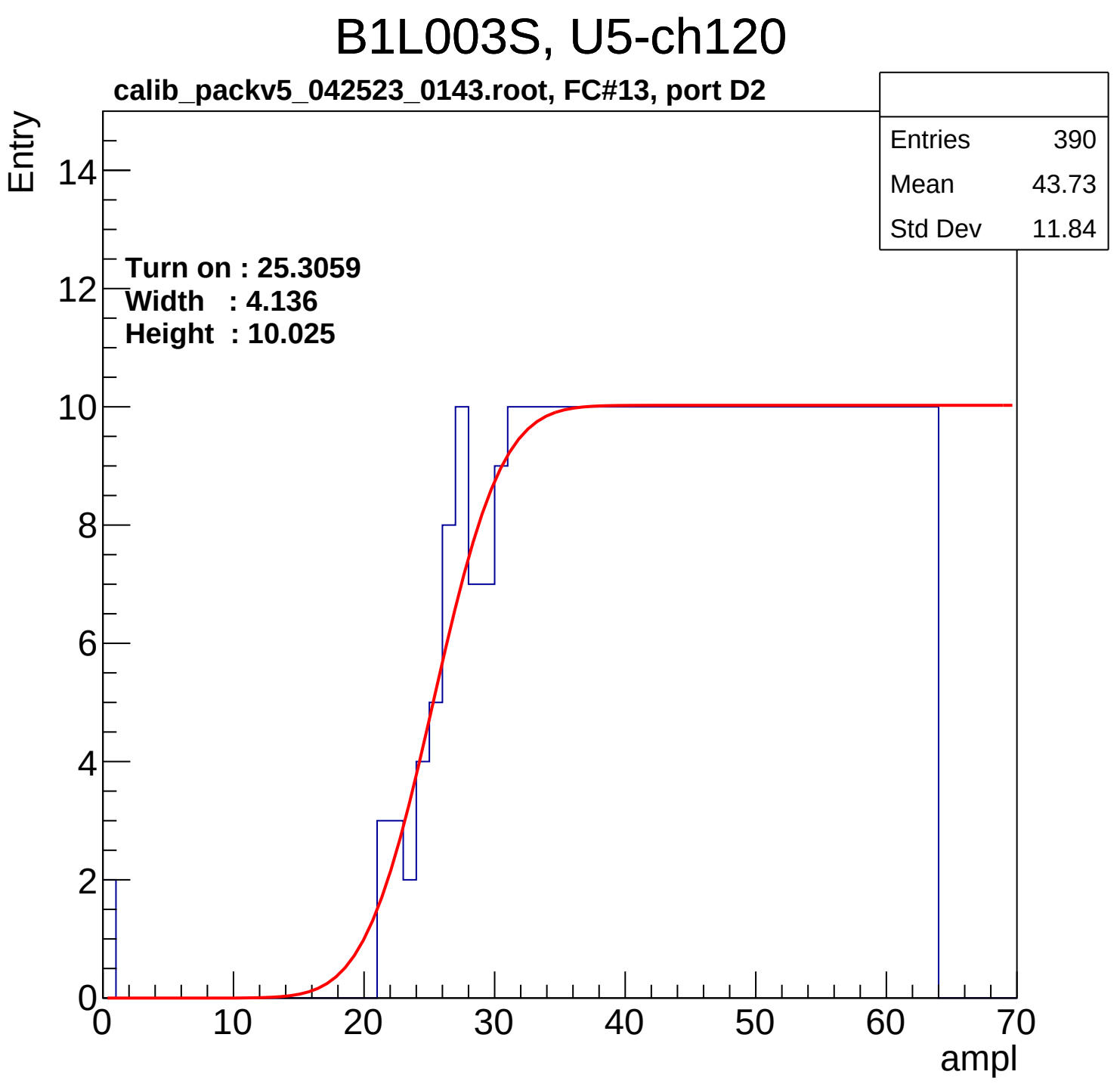

B1L003S, U5-ch119
calib_packv5_042523_0143.root, FC#13, port D2
Entries 365
Mean 45
Std Dev 11.14
Turn on : 28.1204
Width : 2.645
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U5-ch120
calib_packv5_042523_0143.root, FC#13, port D2
Entries 390
Mean 43.73
Std Dev 11.84
Turn on : 25.3059
Width : 4.136
Height : 10.025
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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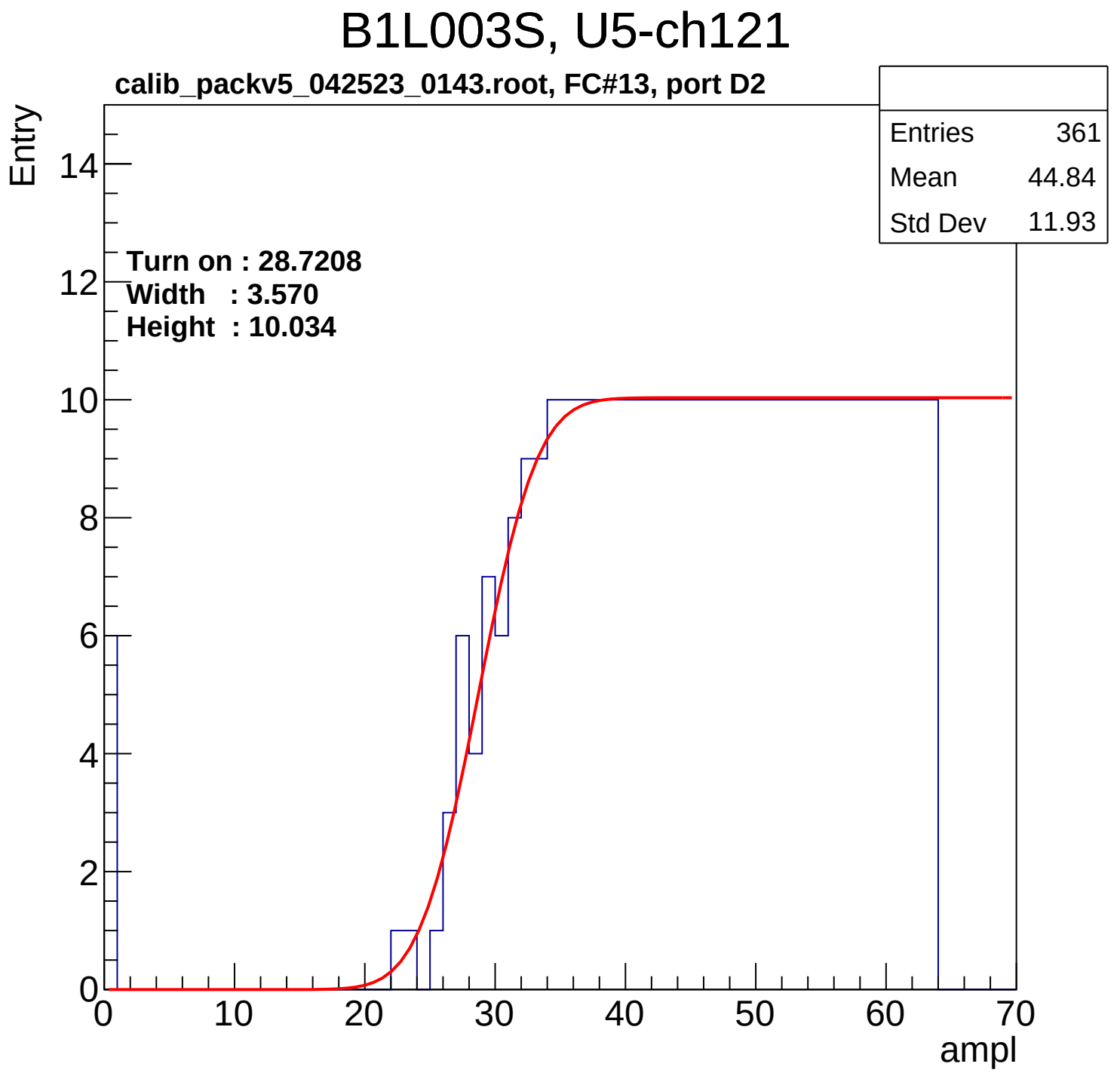
B1L003S, U5-ch121
calib_packv5_042523_0143.root, FC#13, port D2
Entries 361
Mean 44.84
Std Dev 11.93
Turn on : 28.7208
Width : 3.570
Height : 10.034
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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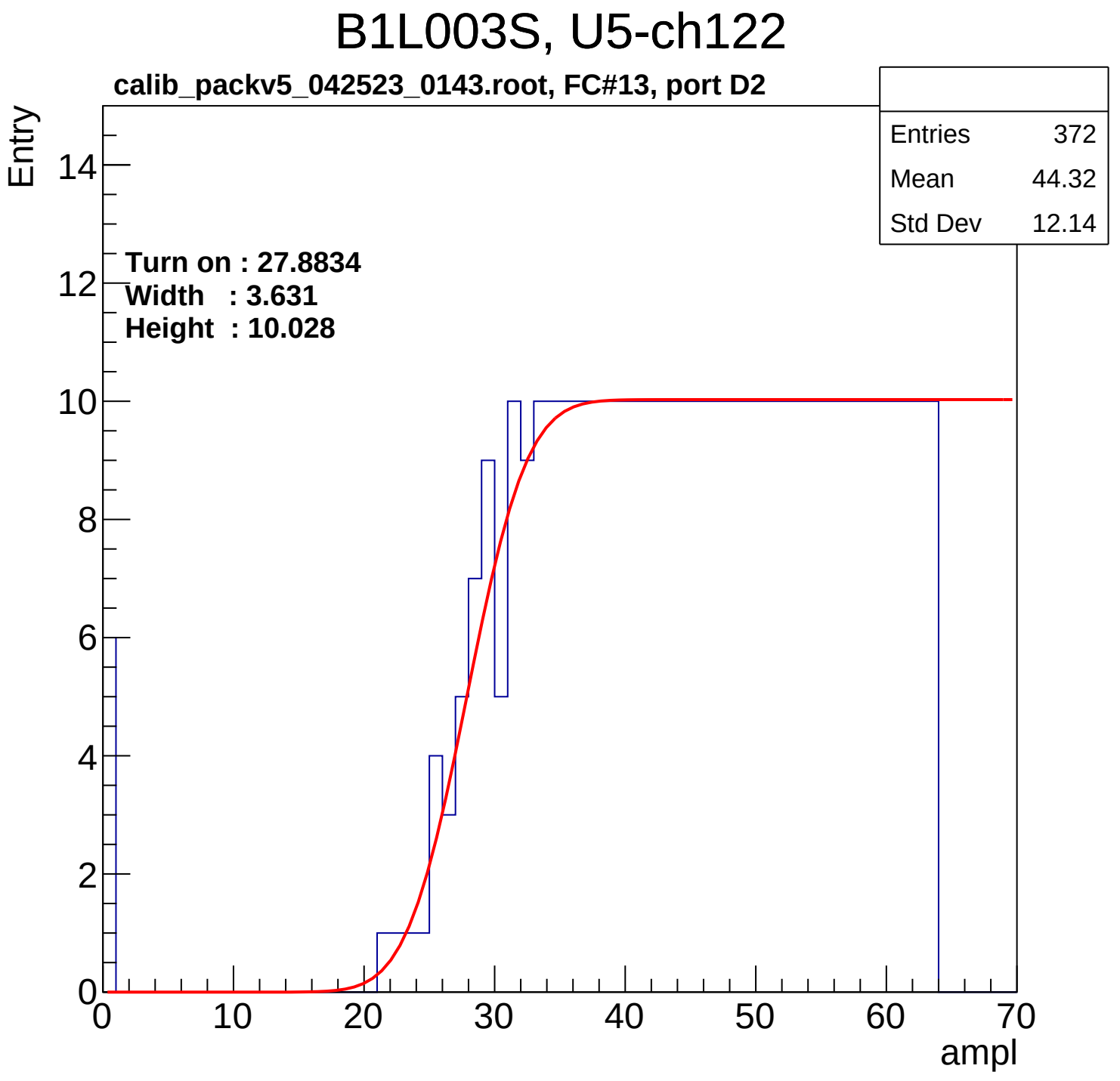
B1L003S, U5-ch122
calib_packv5_042523_0143.root, FC#13, port D2
Entries 372
Mean 44.32
Std Dev 12.14
Turn on : 27.8834
Width : 3.631
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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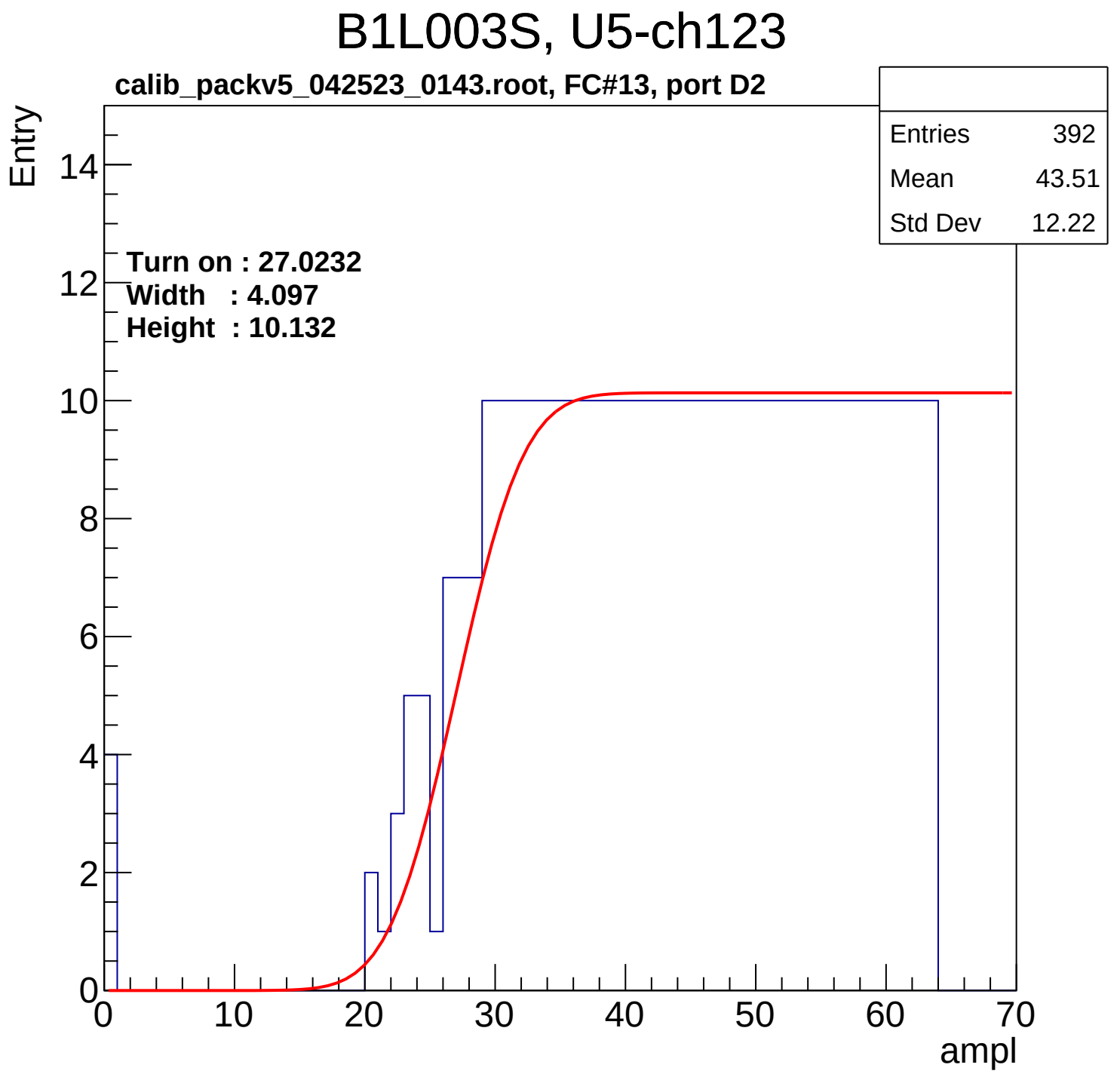
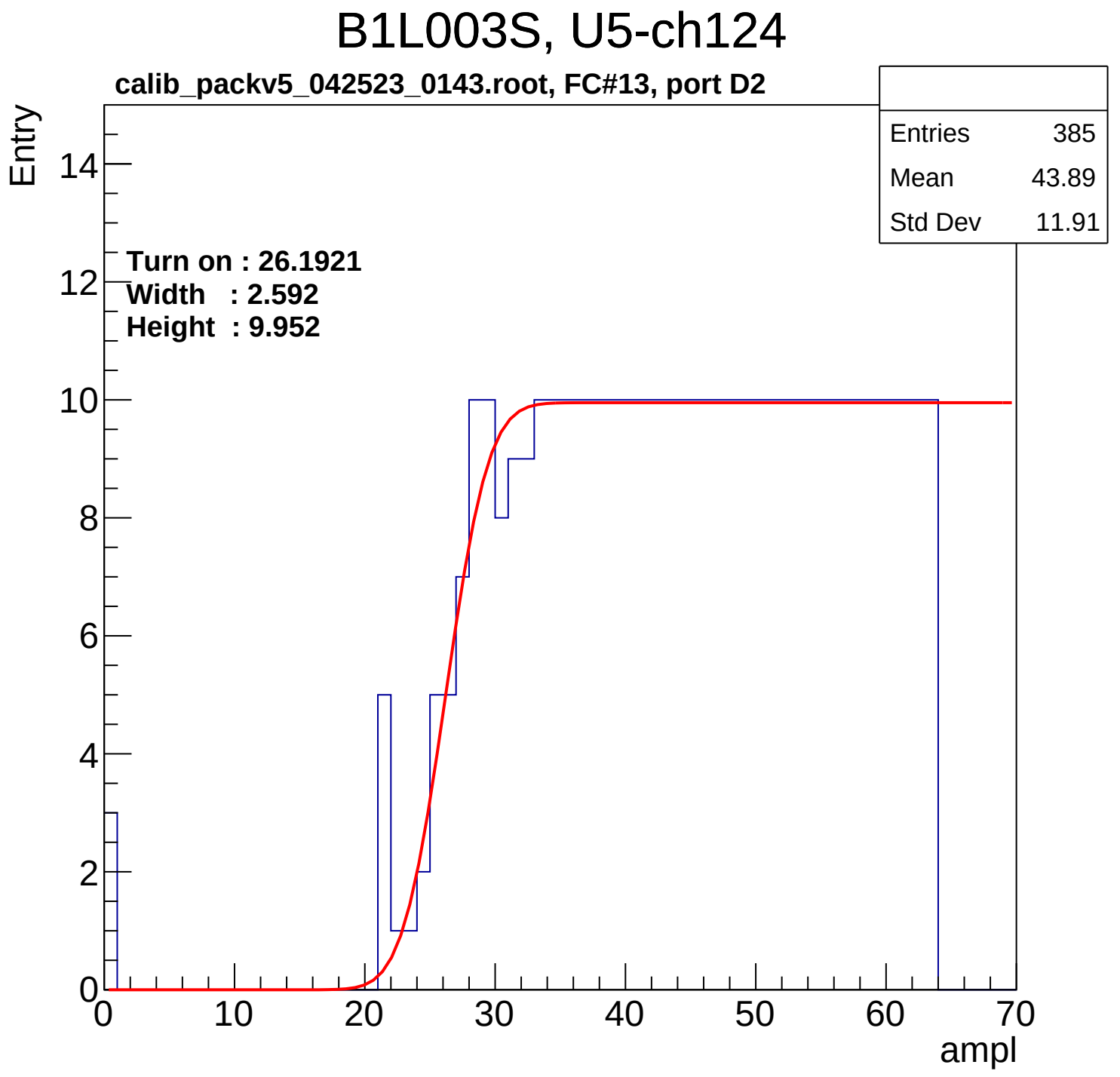

B1L003S, U5-ch123
calib_packv5_042523_0143.root, FC#13, port D2
Entries 392
Mean 43.51
Std Dev 12.22
Turn on : 27.0232
Width : 4.097
Height : 10.132
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U5-ch124
calib_packv5_042523_0143.root, FC#13, port D2
Entries 385
Mean 43.89
Std Dev 11.91
Turn on : 26.1921
Width : 2.592
Height : 9.952
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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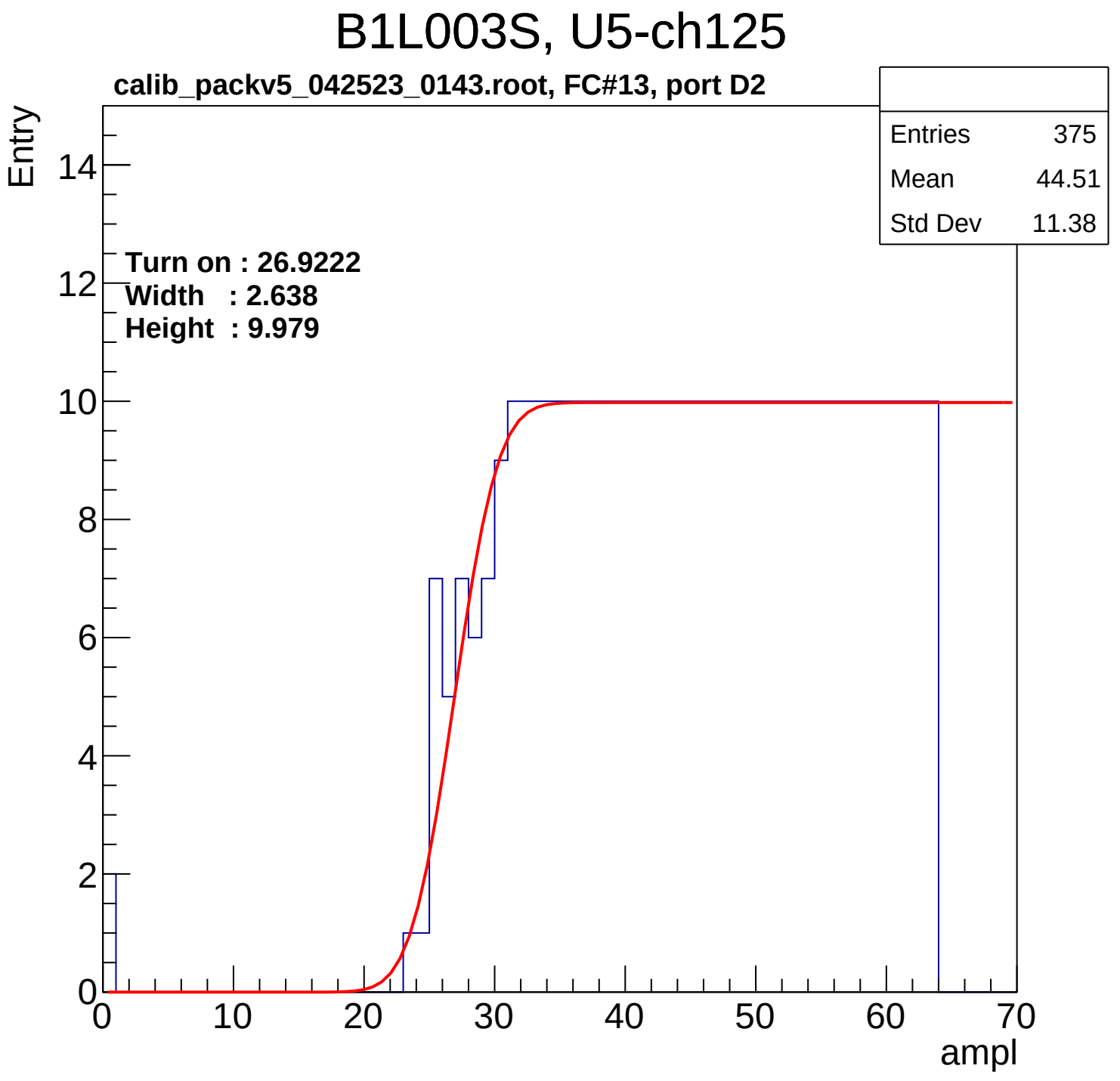
B1L003S, U5-ch125
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.51
Std Dev 11.38
Turn on : 26.9222
Width : 2.638
Height : 9.979
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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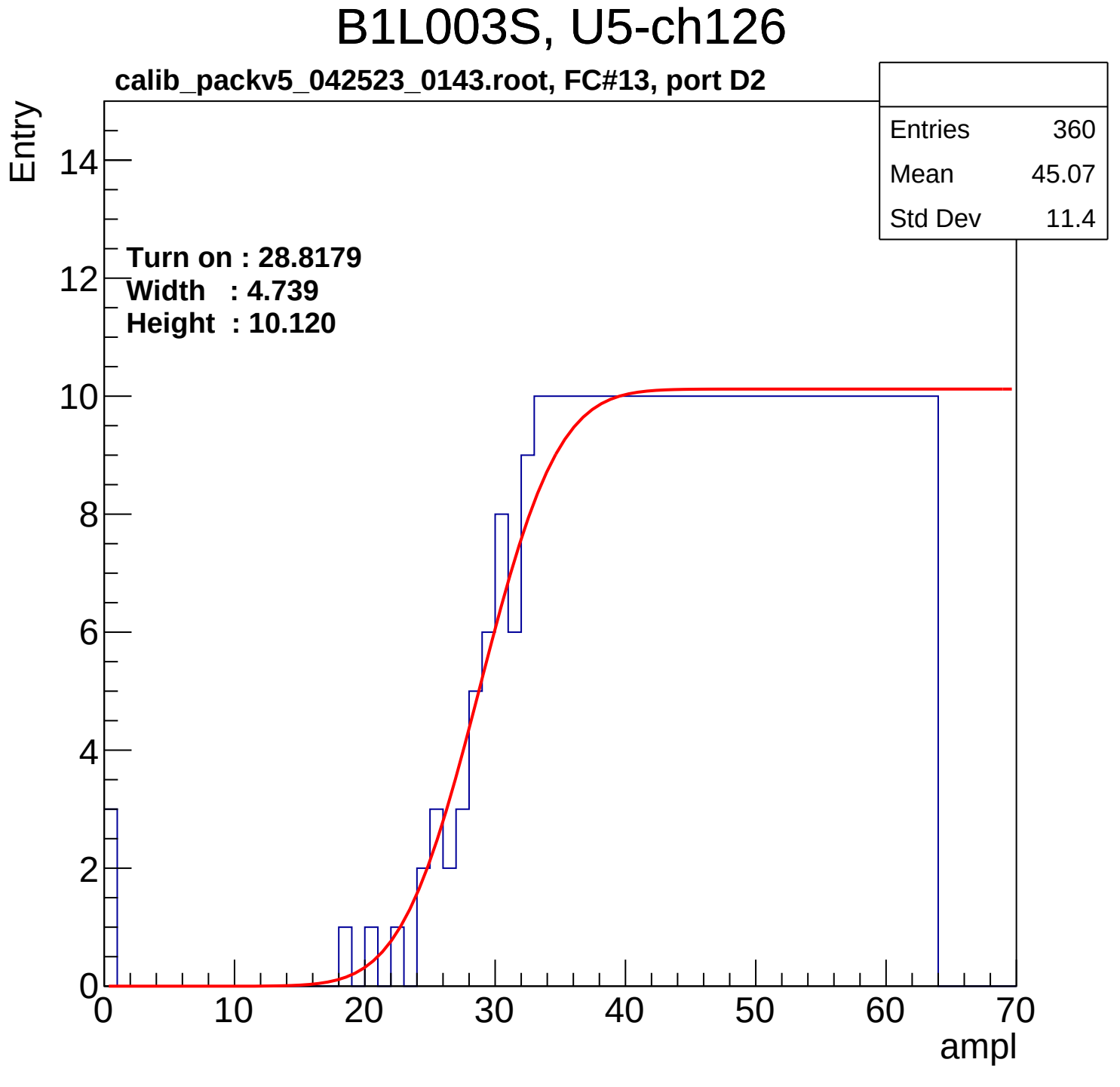
B1L003S, U5-ch126
calib_packv5_042523_0143.root, FC#13, port D2
Entries 360
Mean 45.07
Std Dev 11.4
Turn on : 28.8179
Width : 4.739
Height : 10.120
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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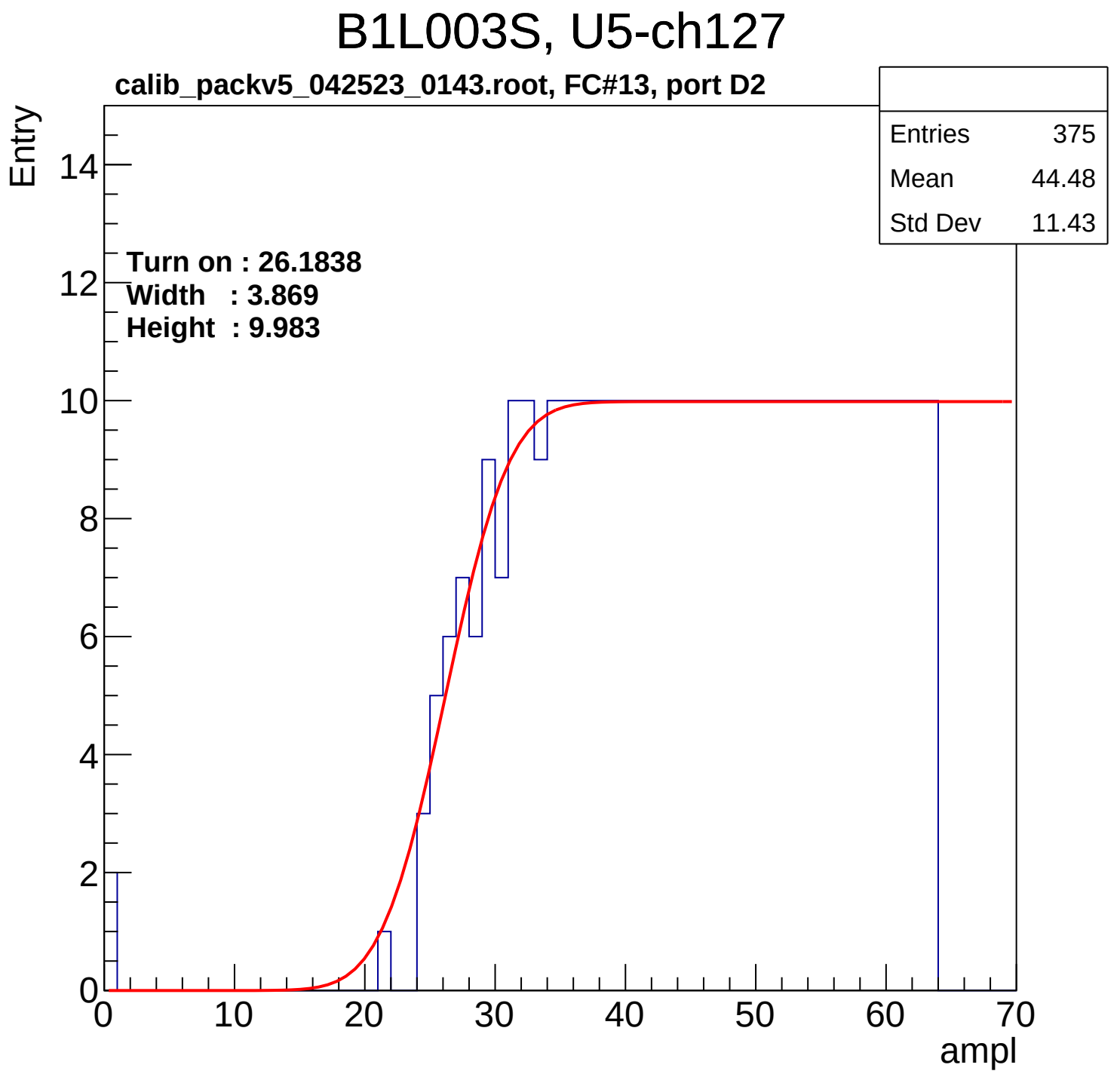
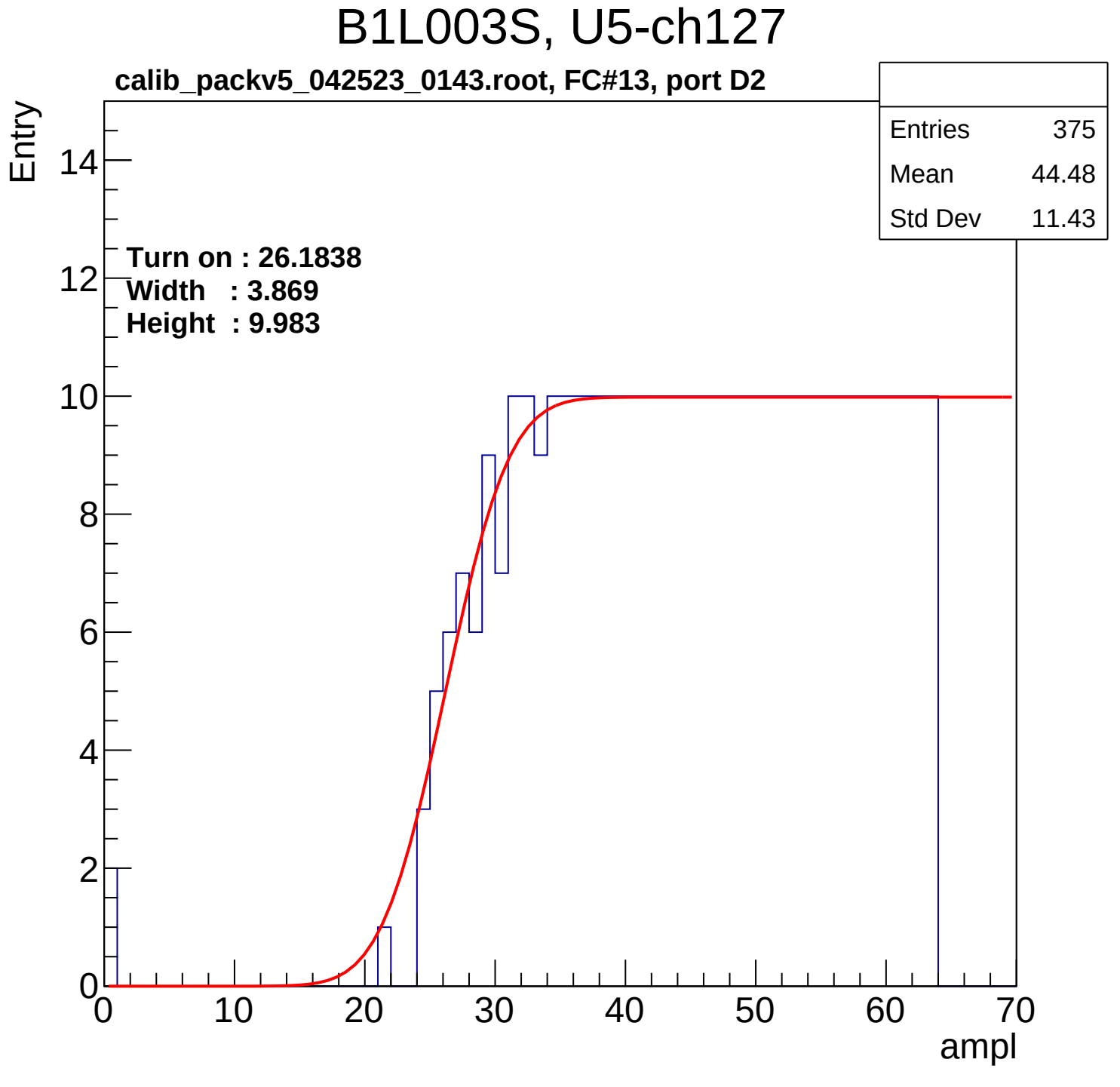

B1L003S, U5-ch127
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.48
Std Dev 11.43
Turn on : 26.1838
Width : 3.869
Height : 9.983
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U5-ch127
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.48
Std Dev 11.43
Turn on : 26.1838
Width : 3.869
Height : 9.983
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70