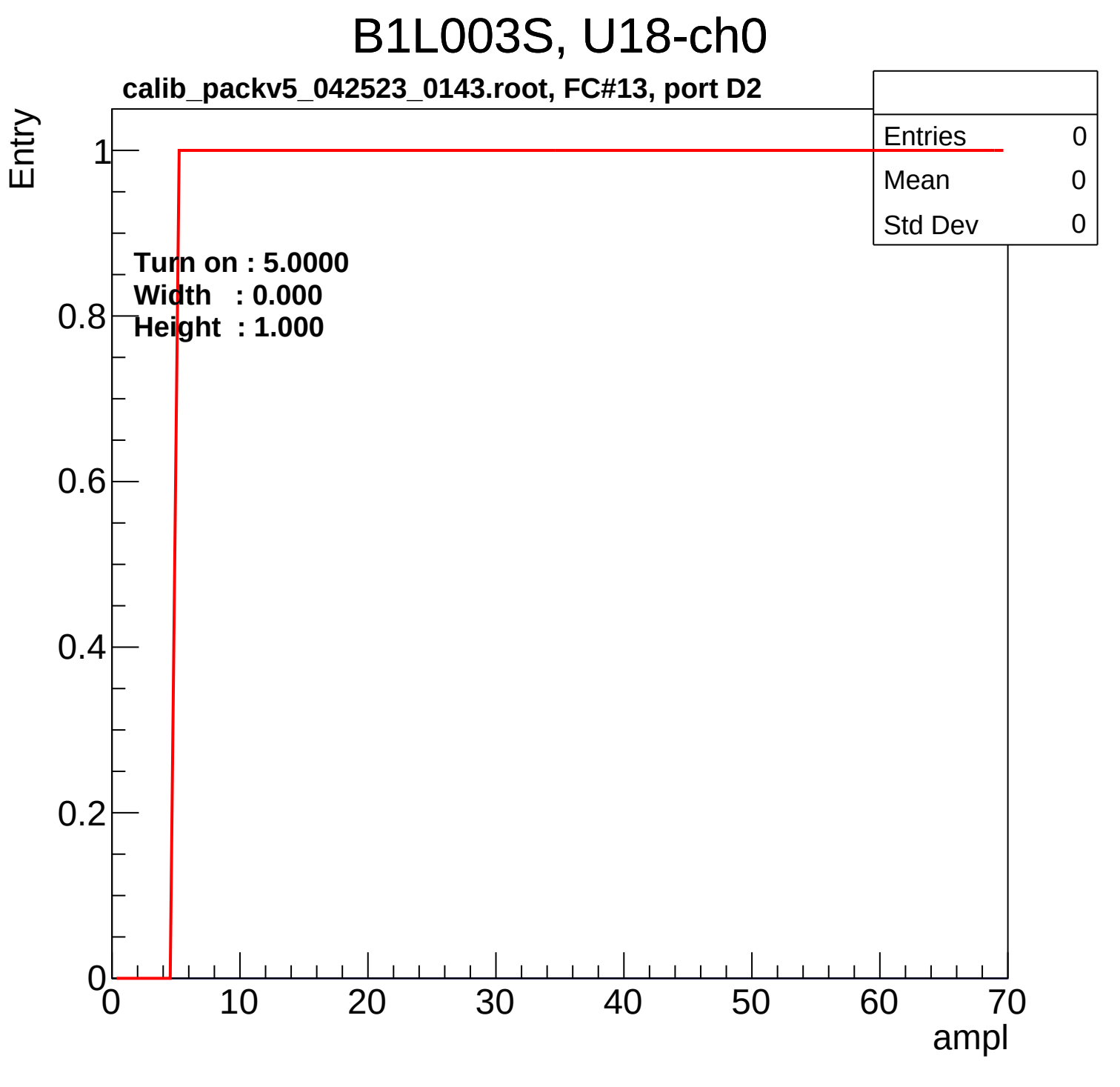
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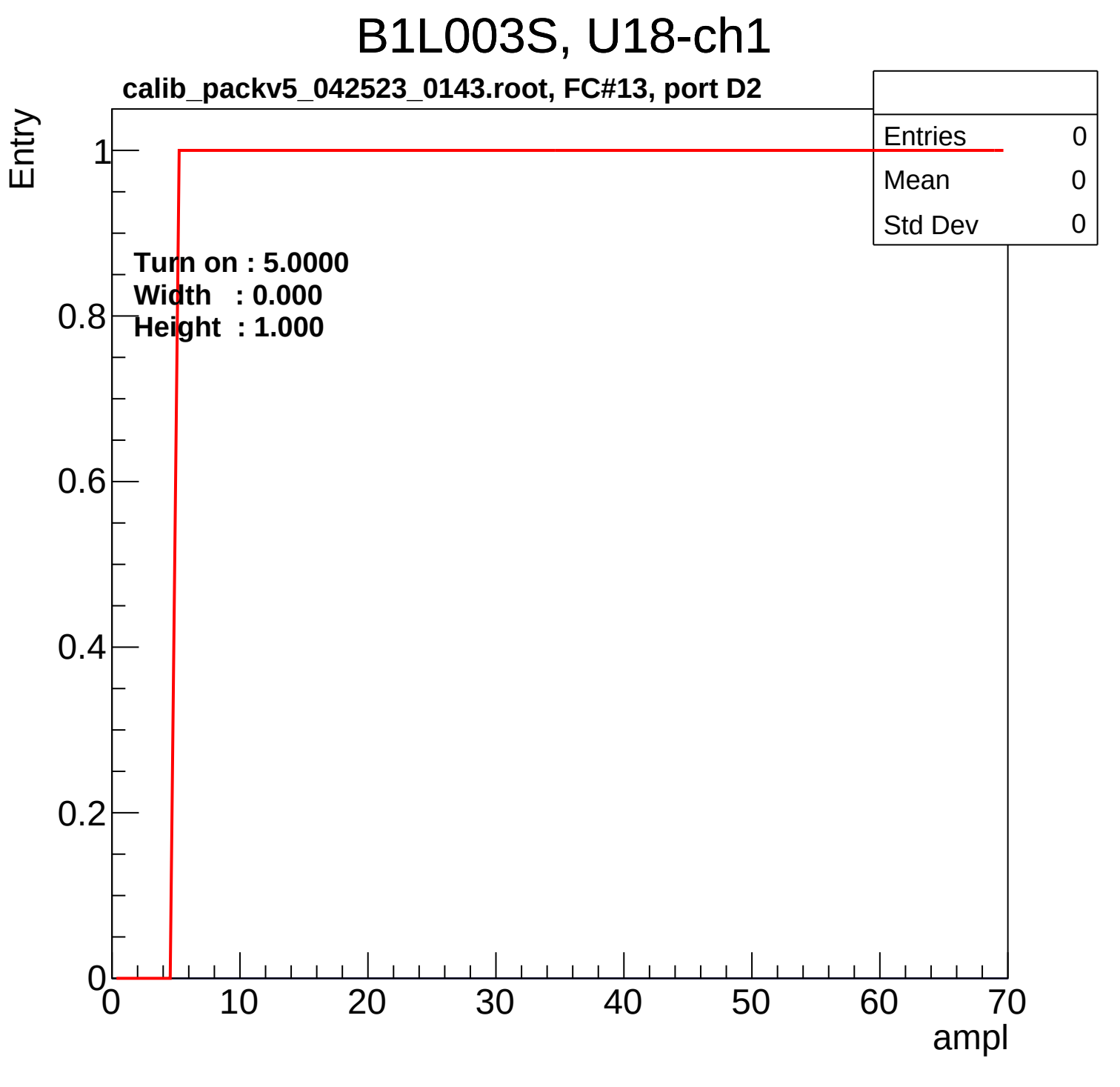
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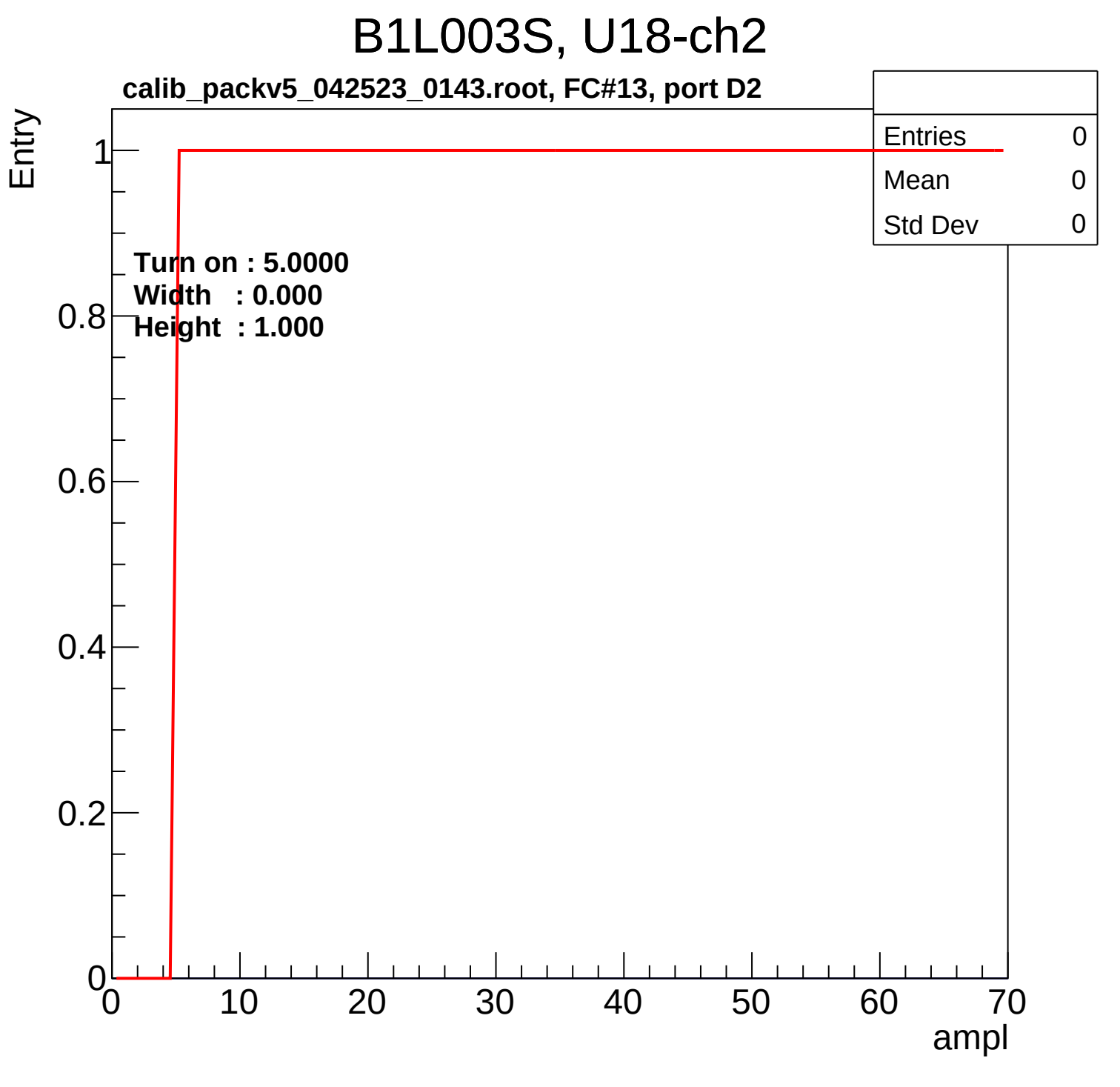
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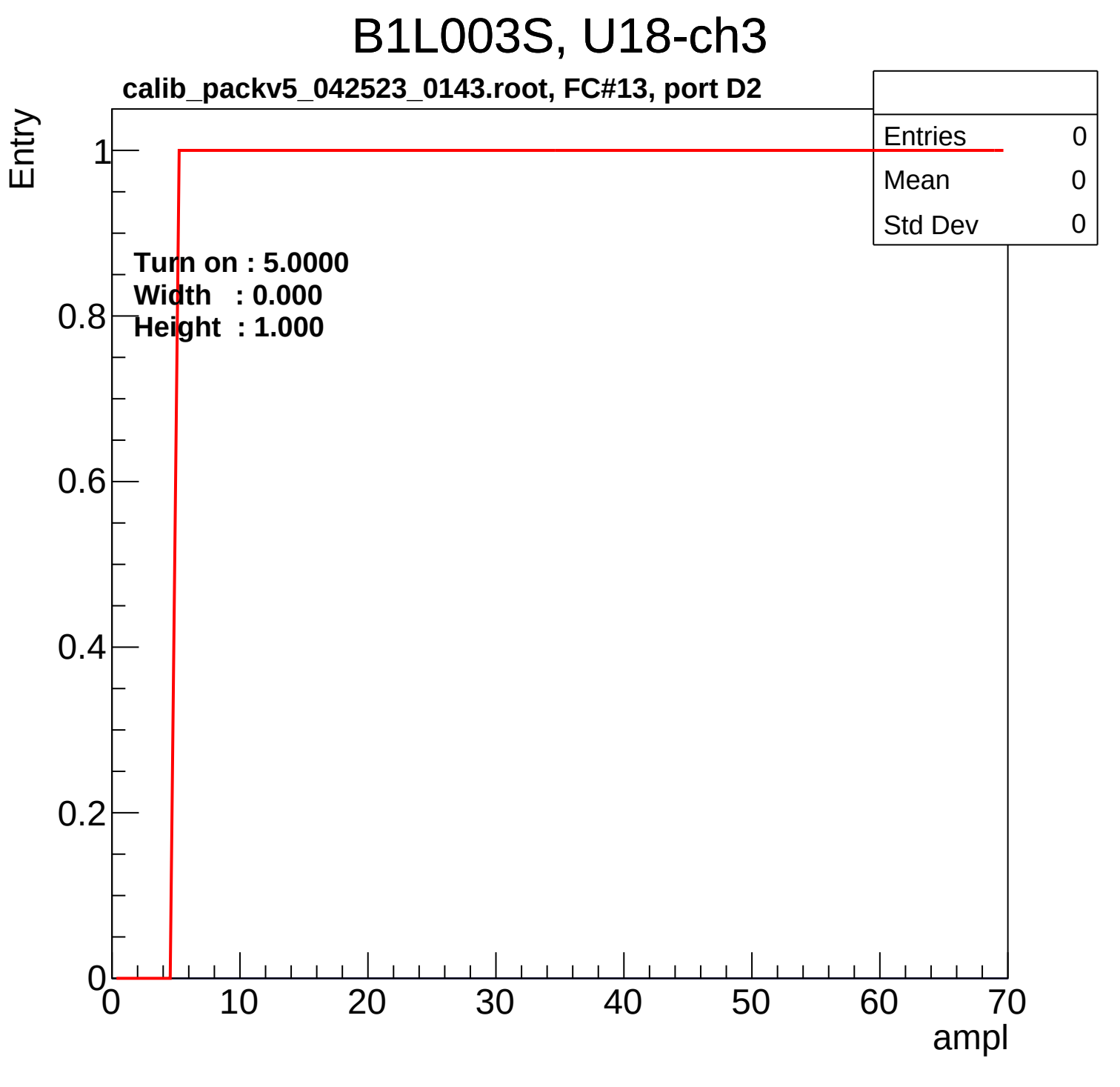
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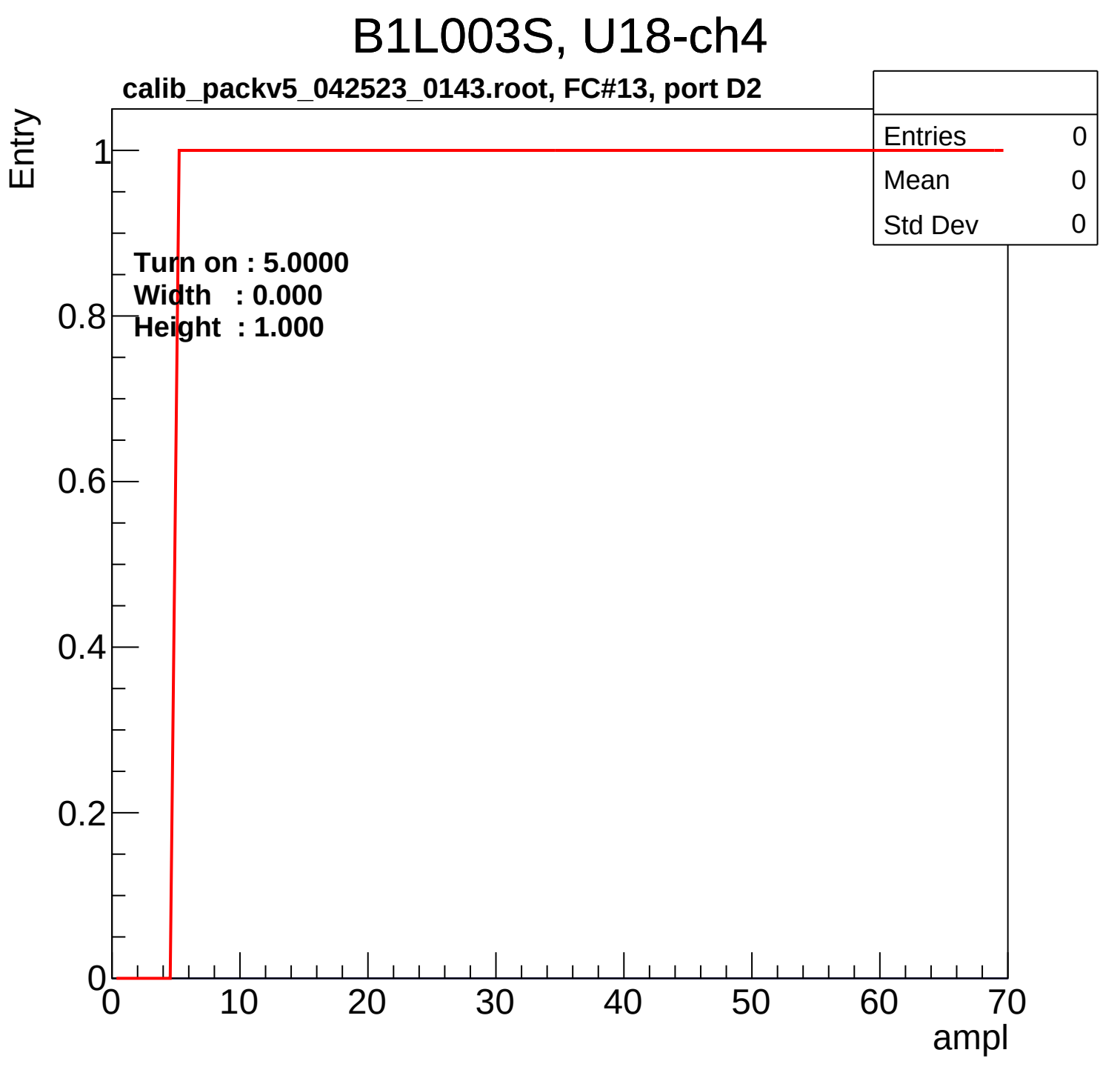
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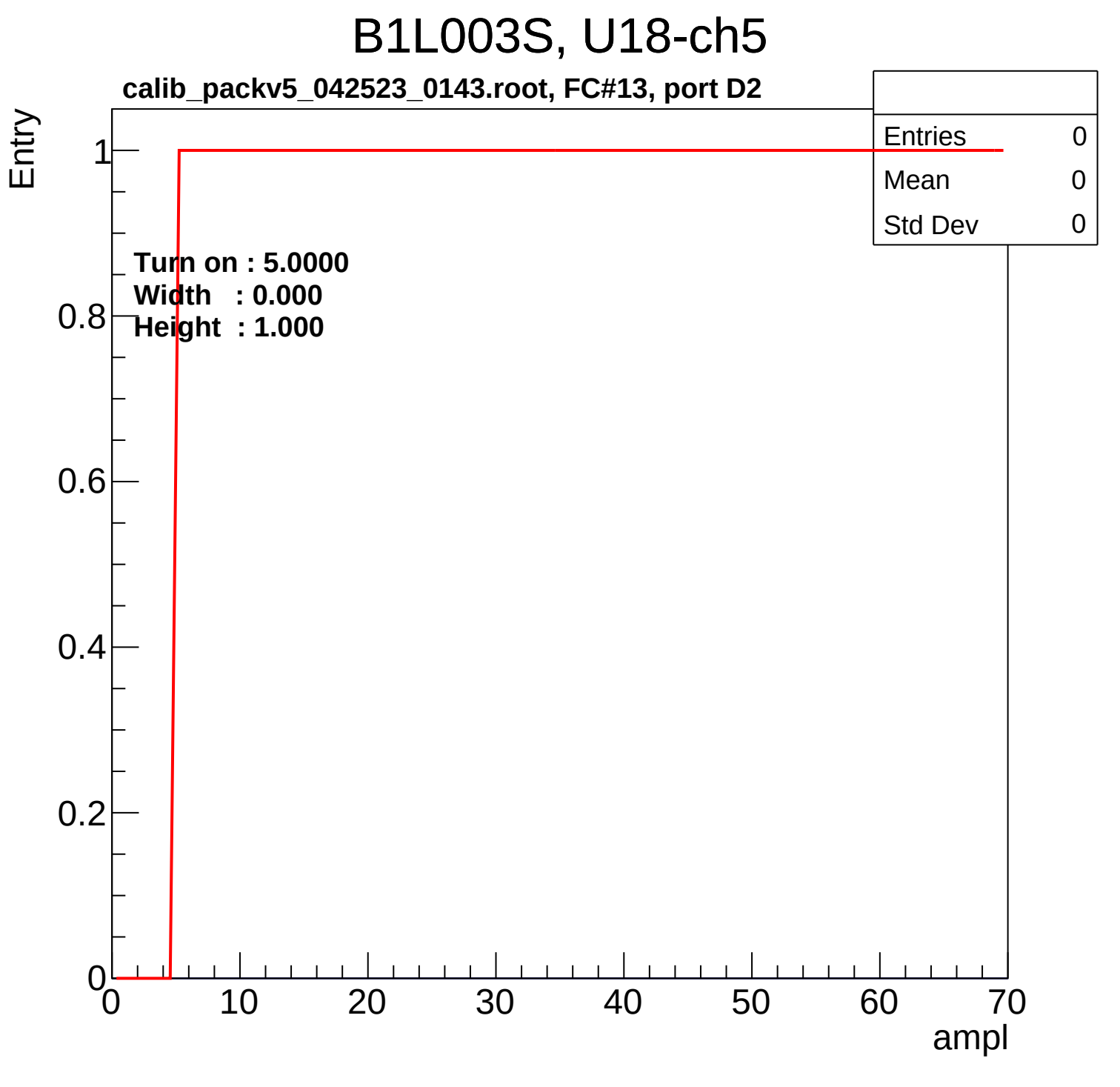
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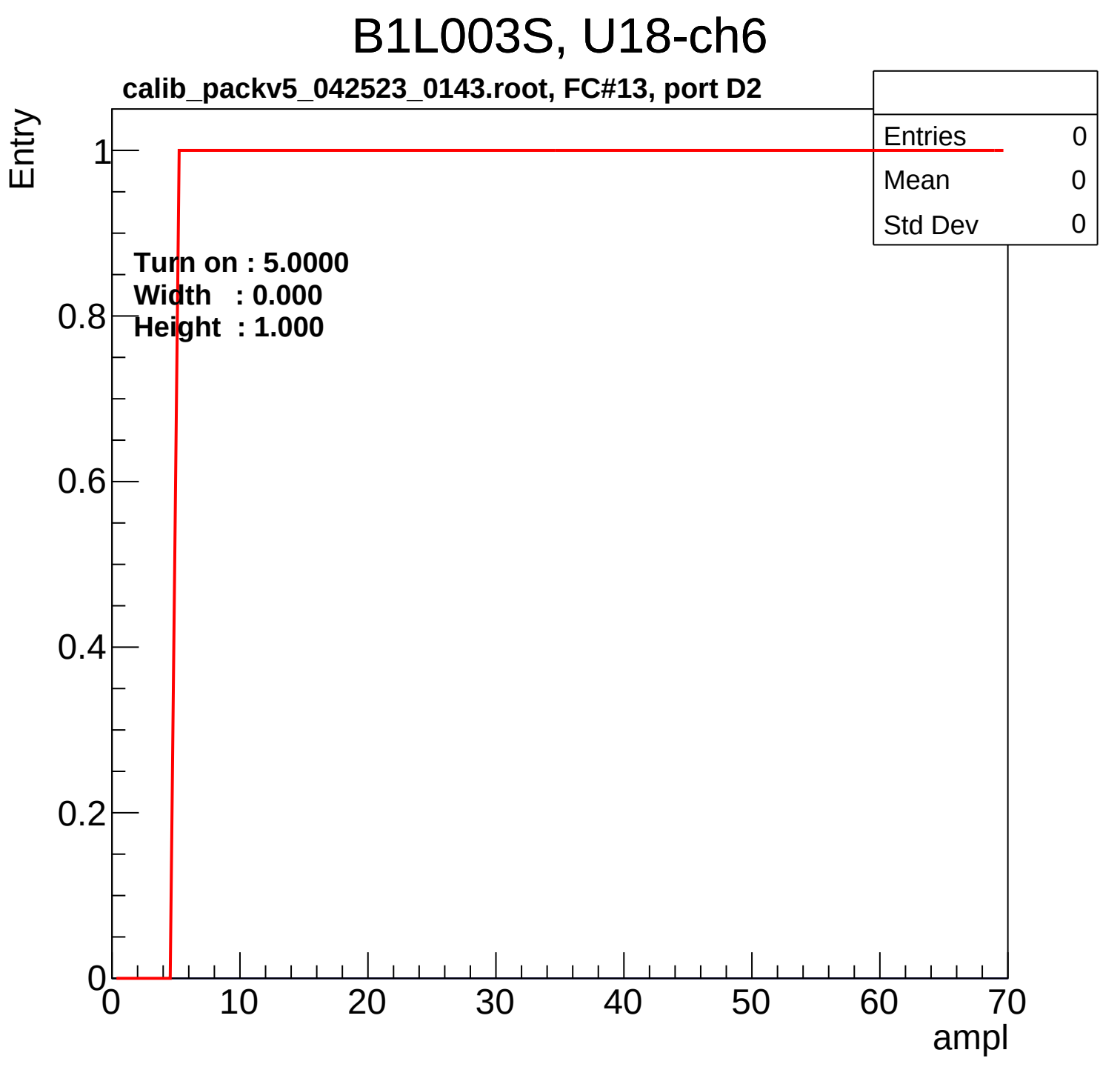
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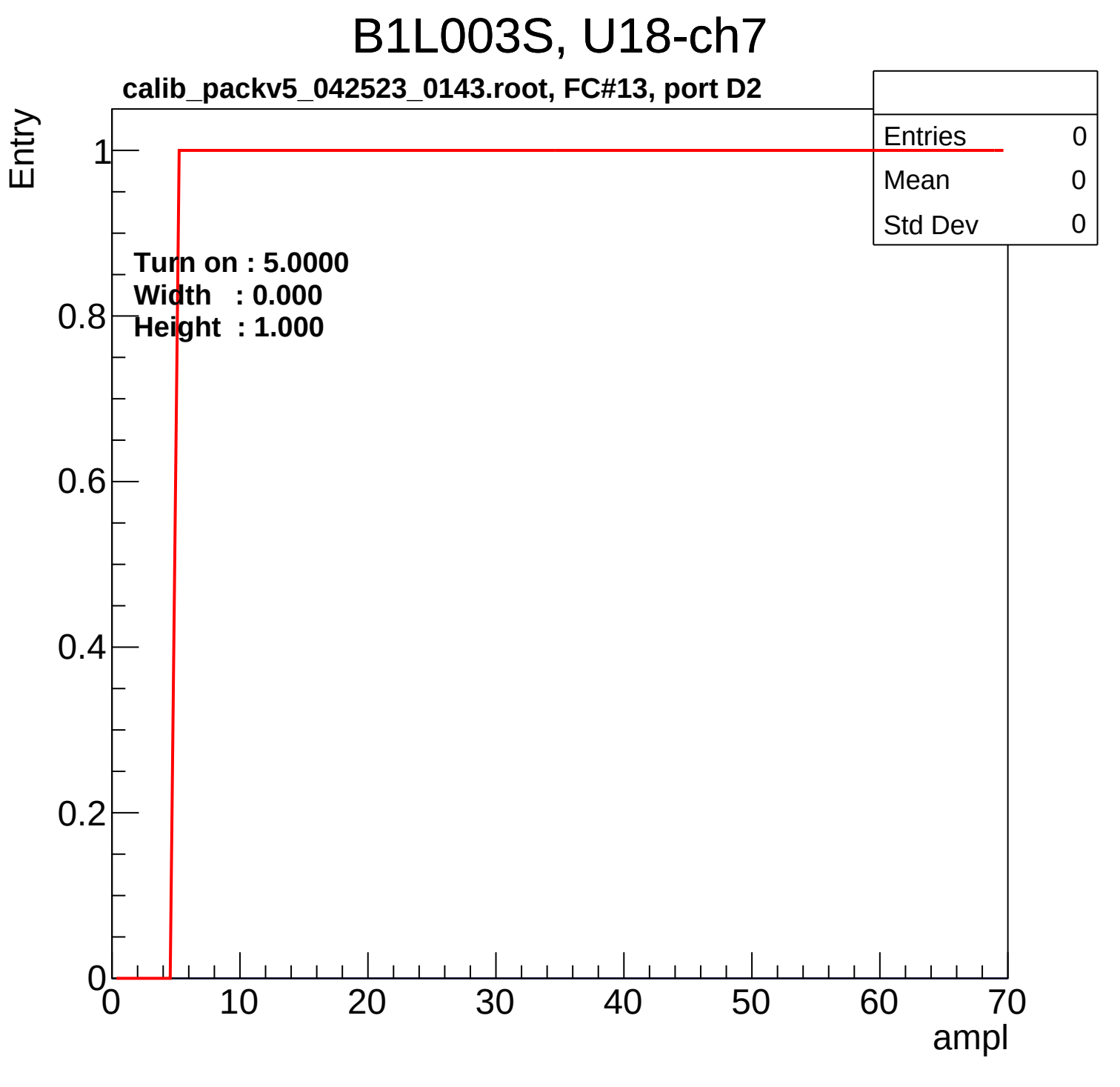
B1L003S, U18-ch7
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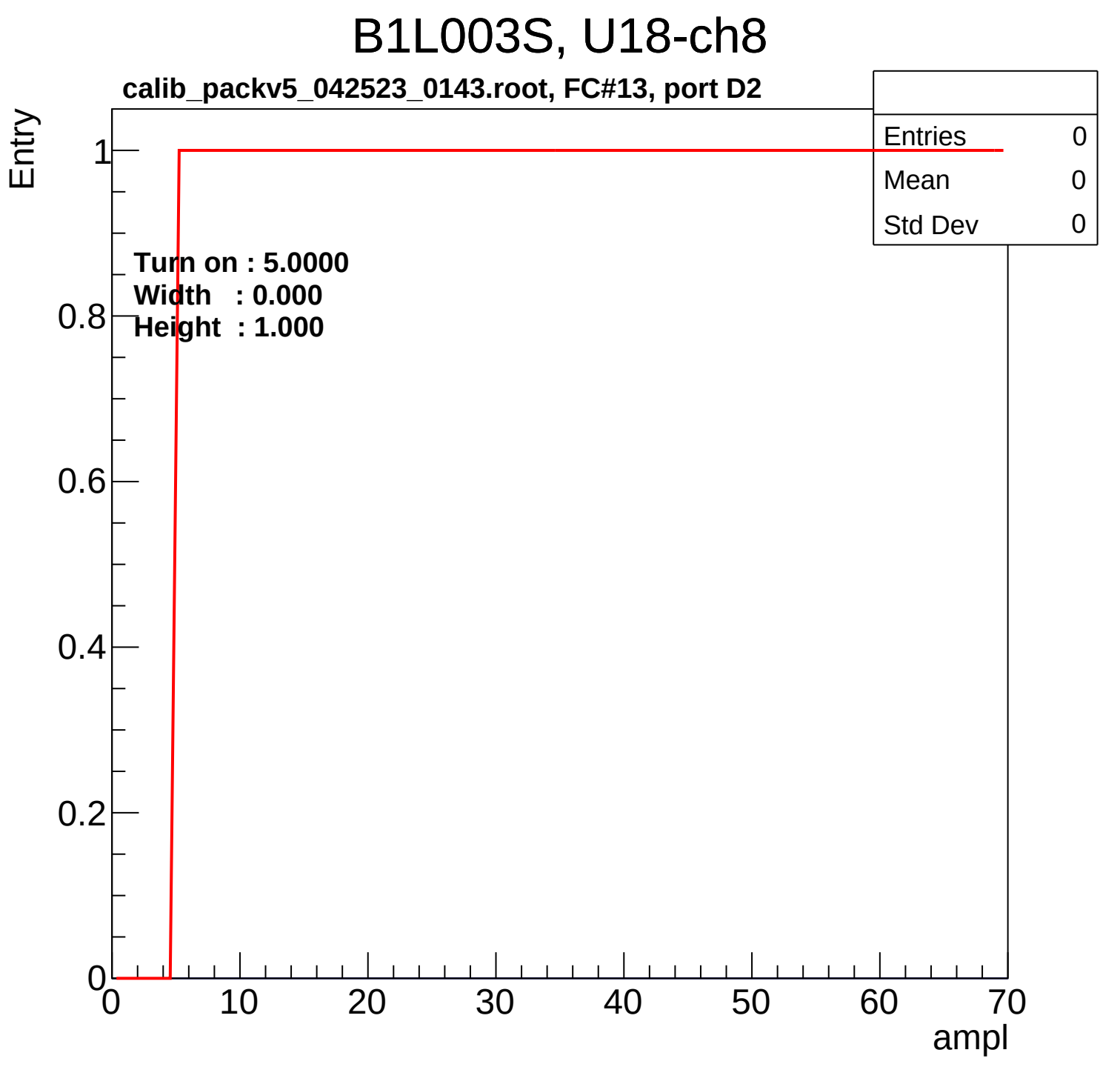
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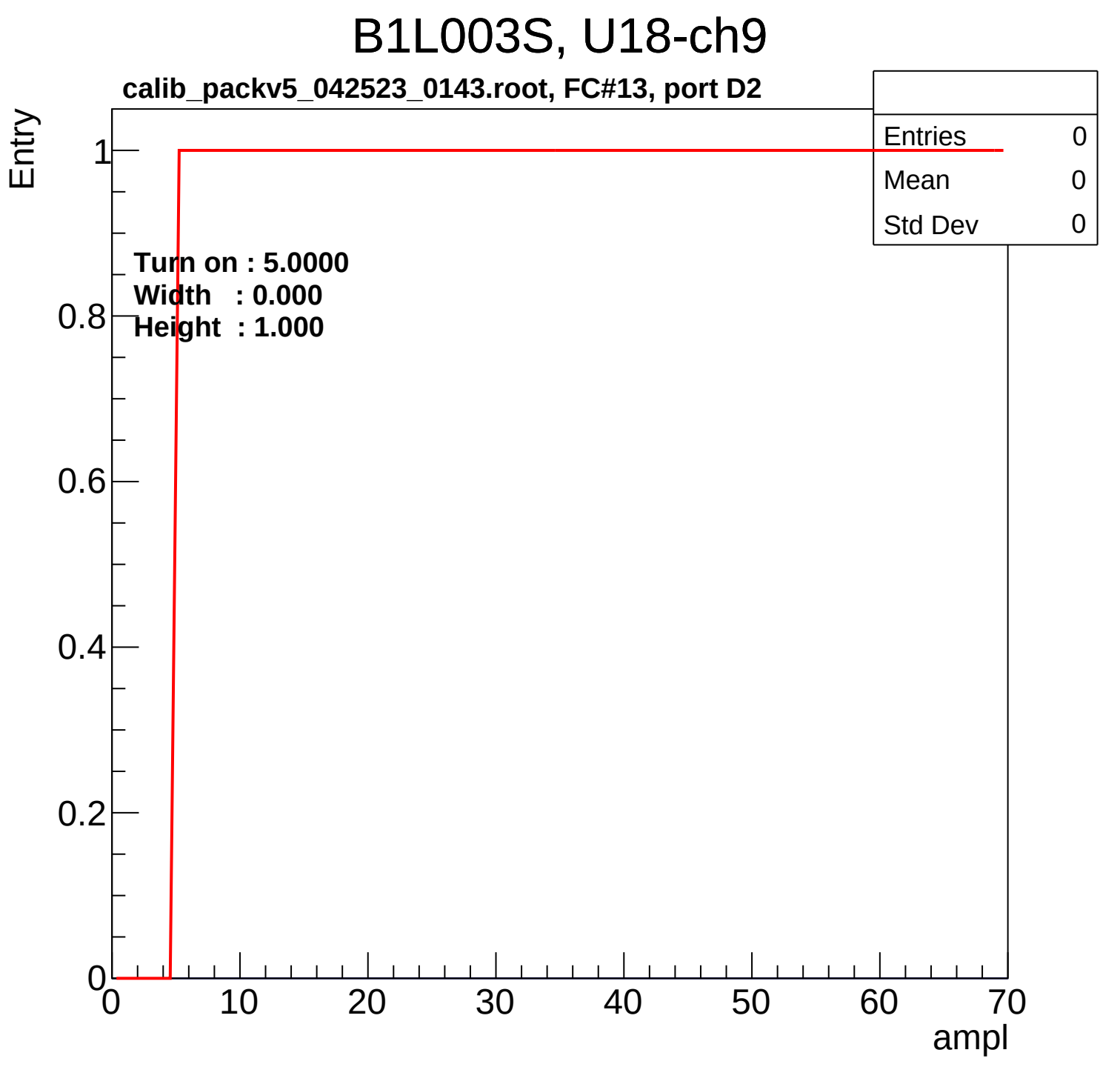
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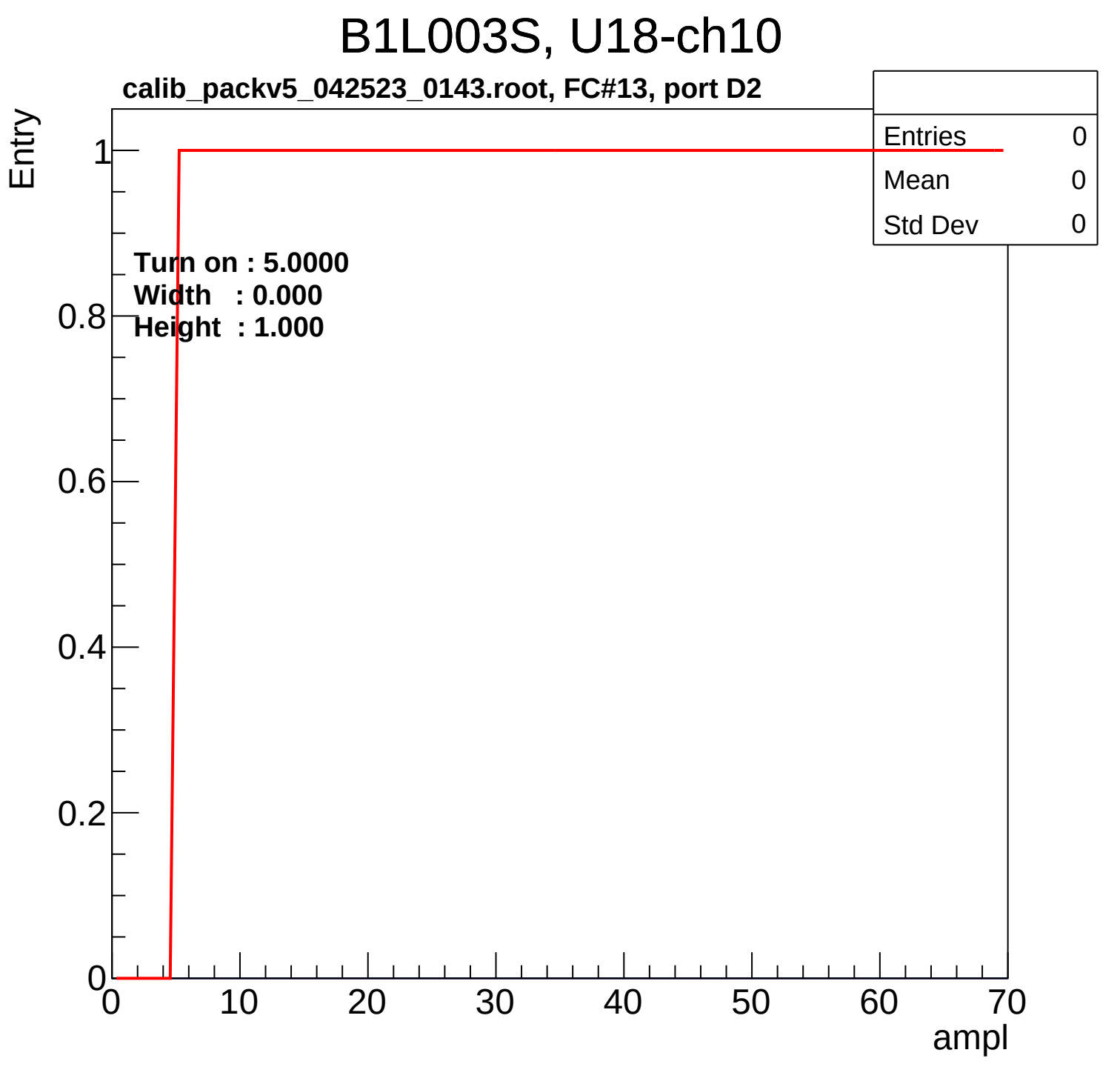
ampl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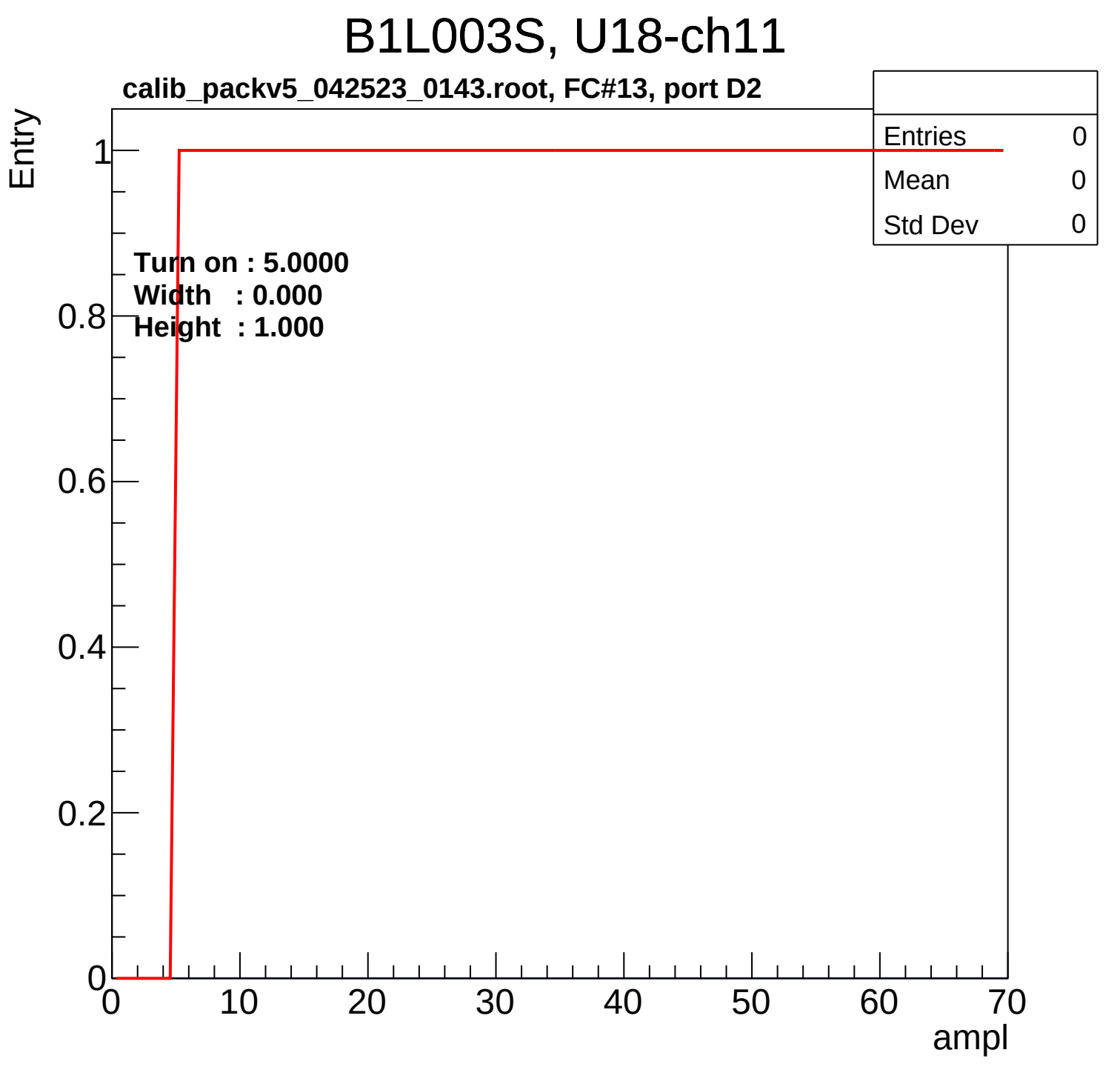
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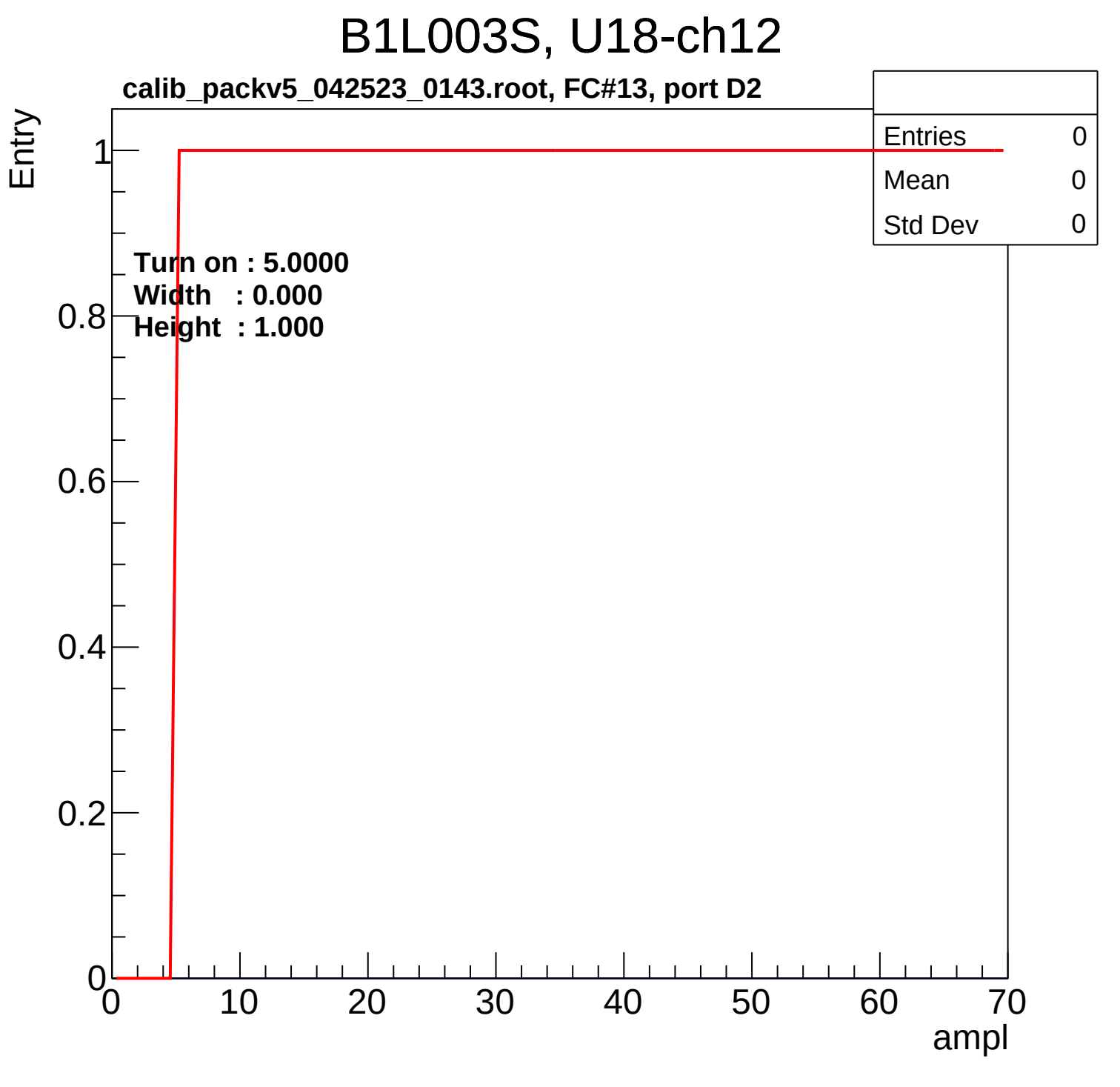
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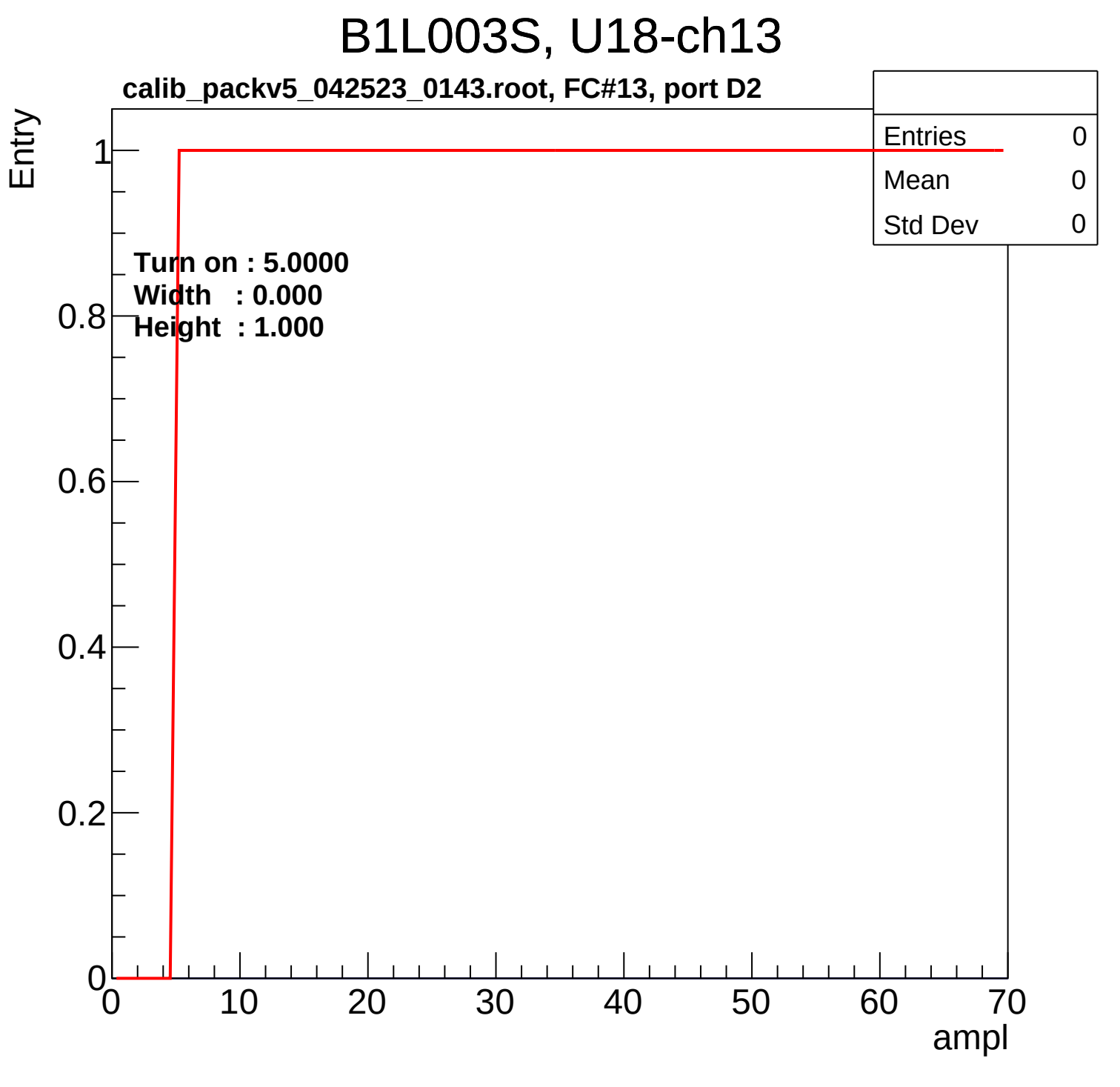
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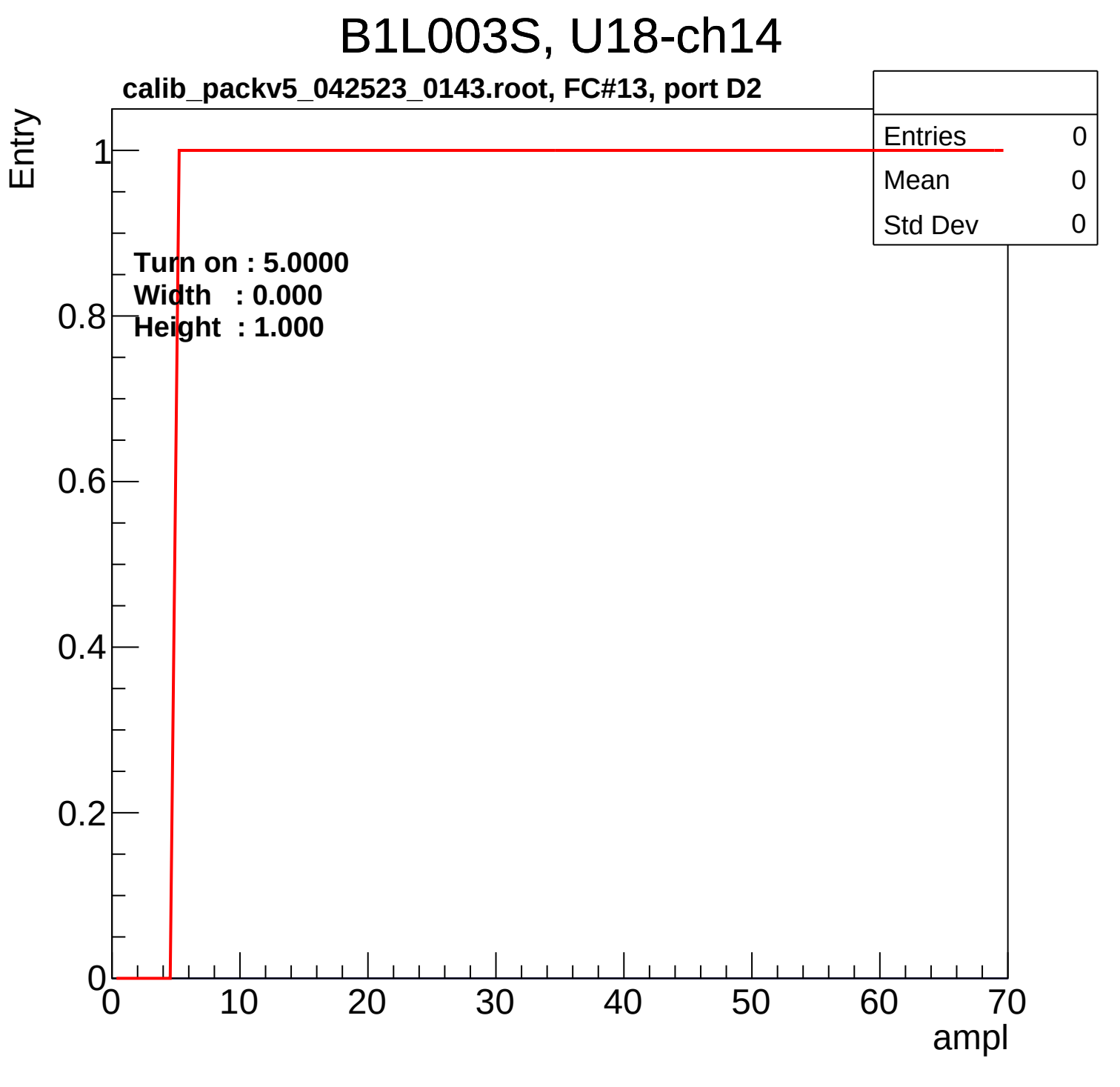
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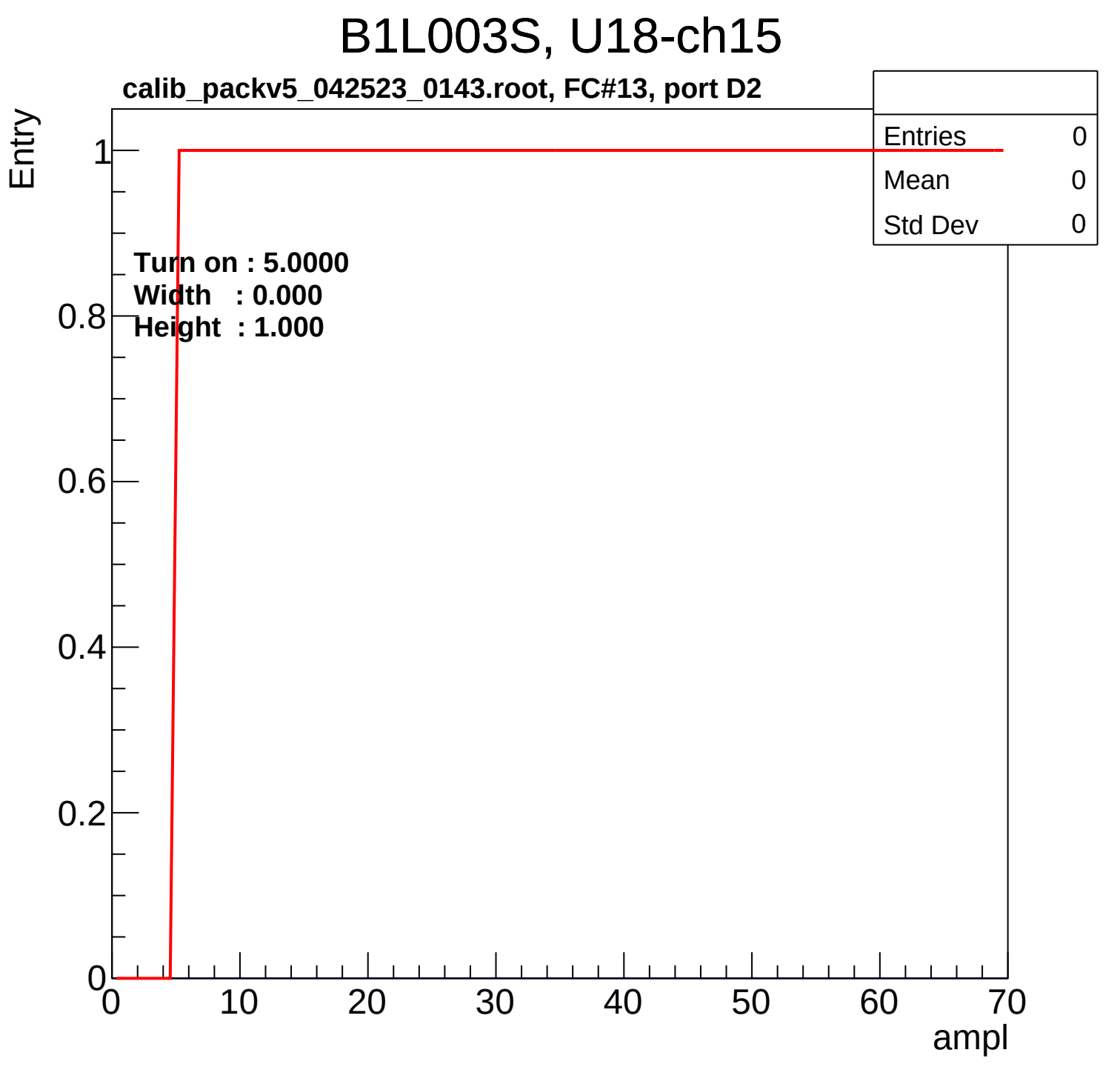
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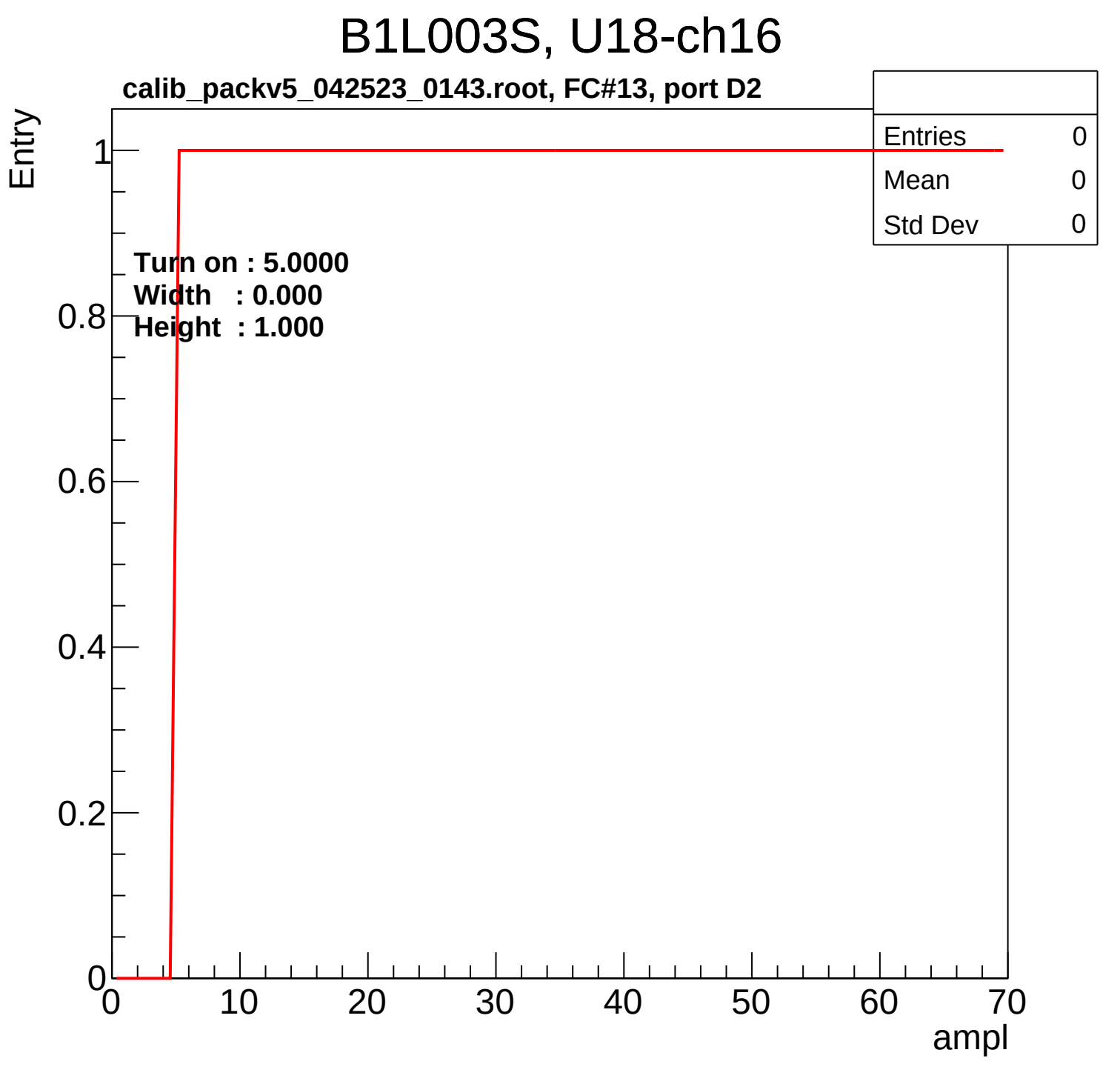
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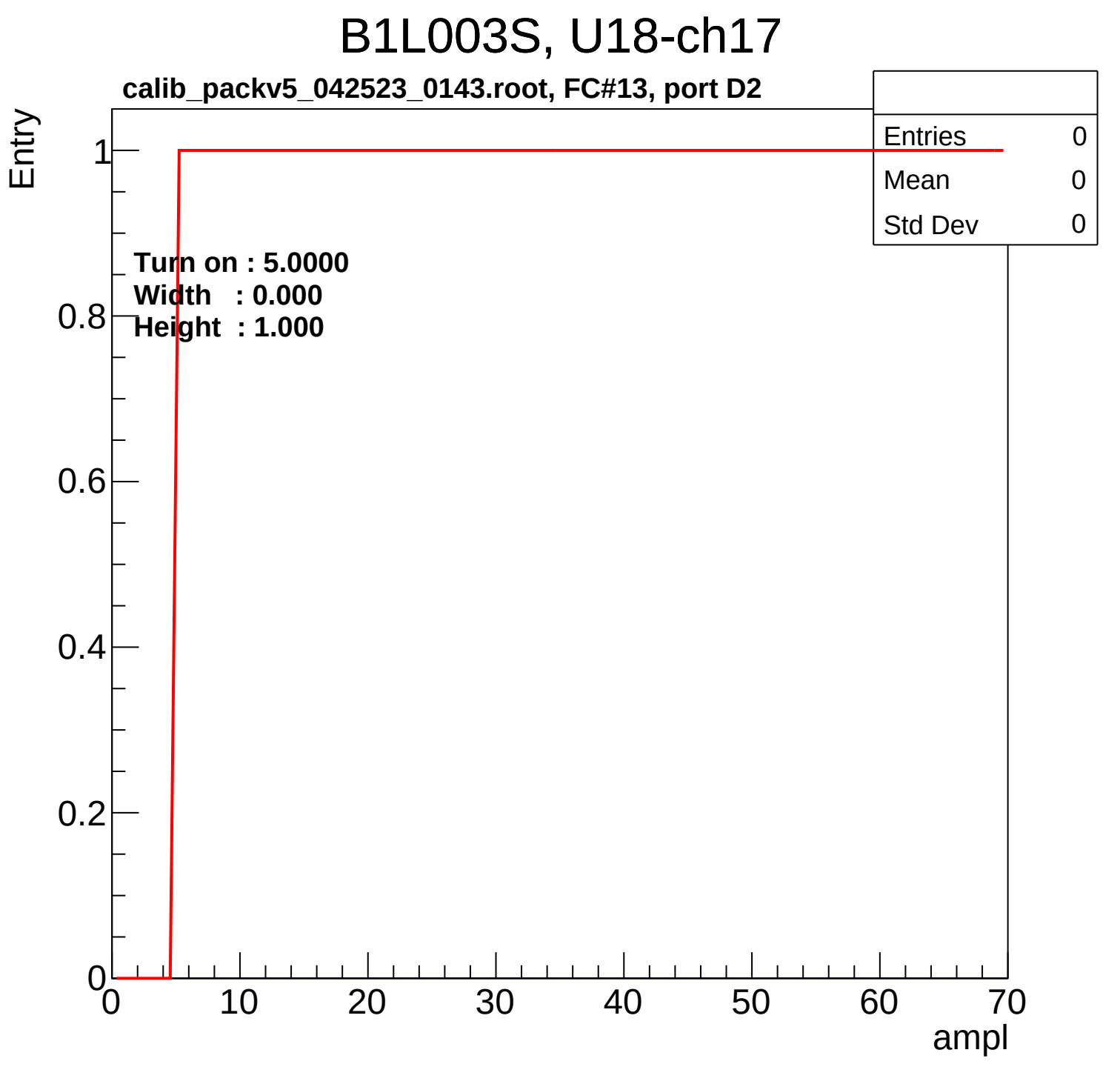
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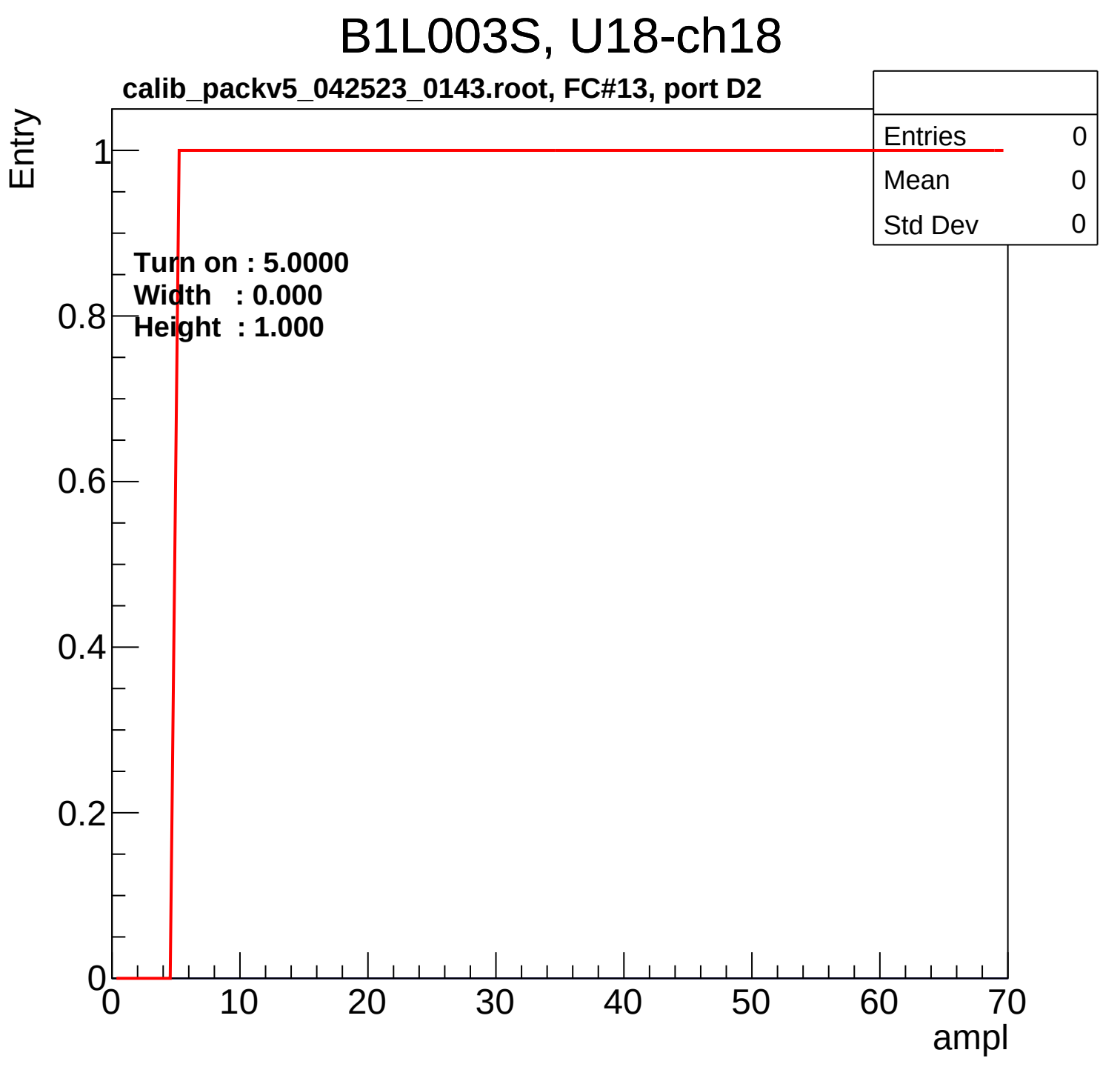
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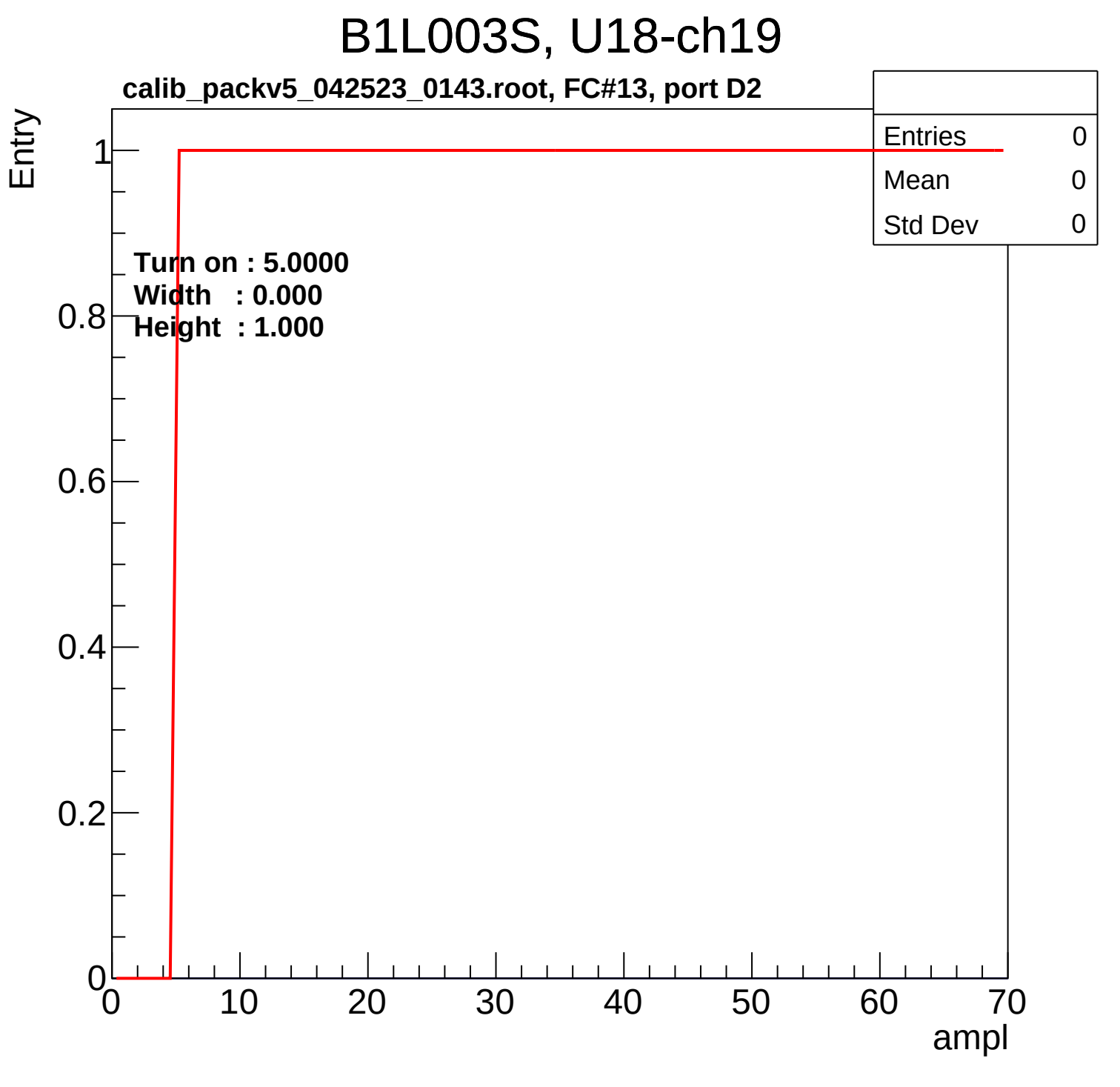
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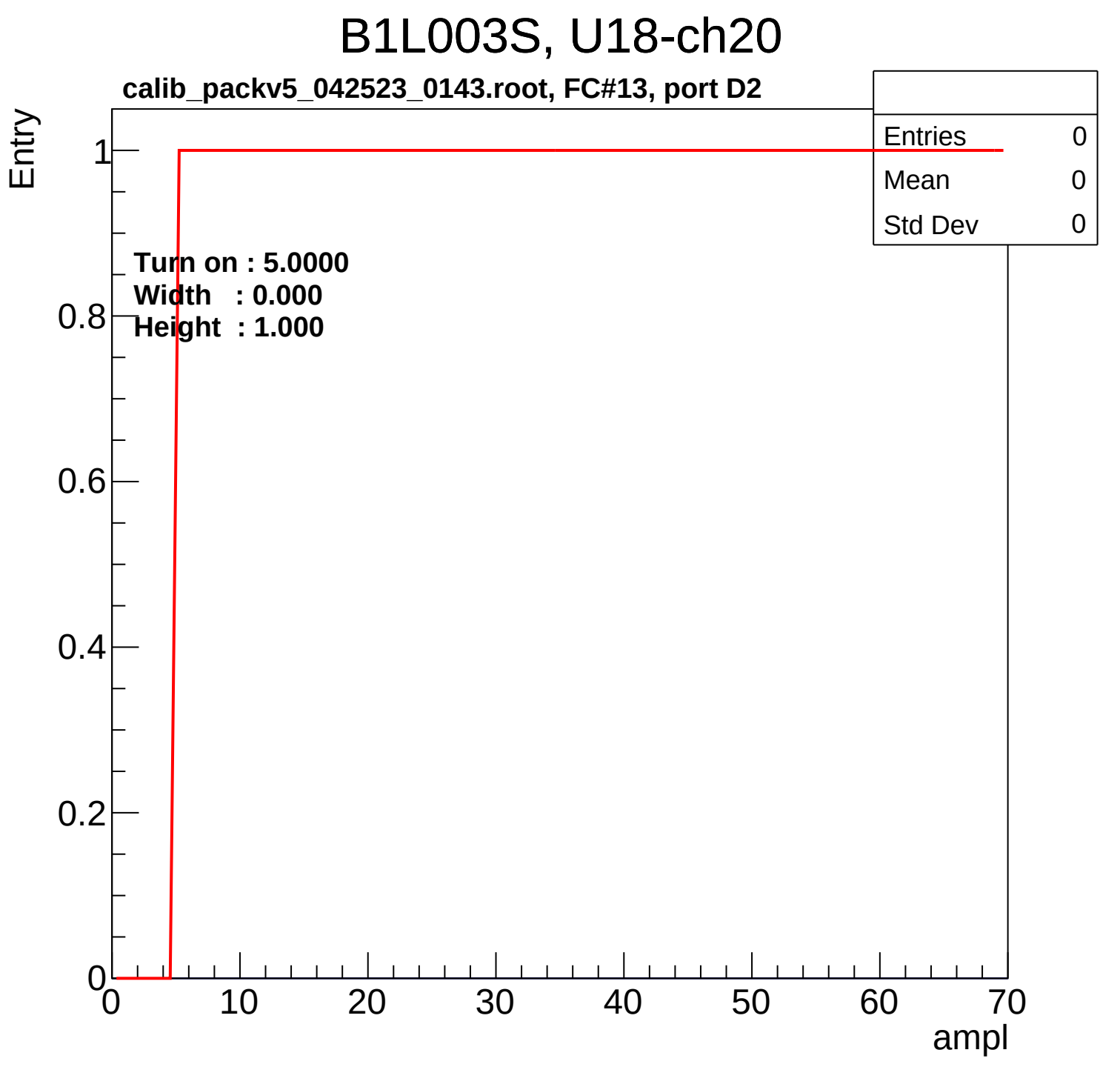
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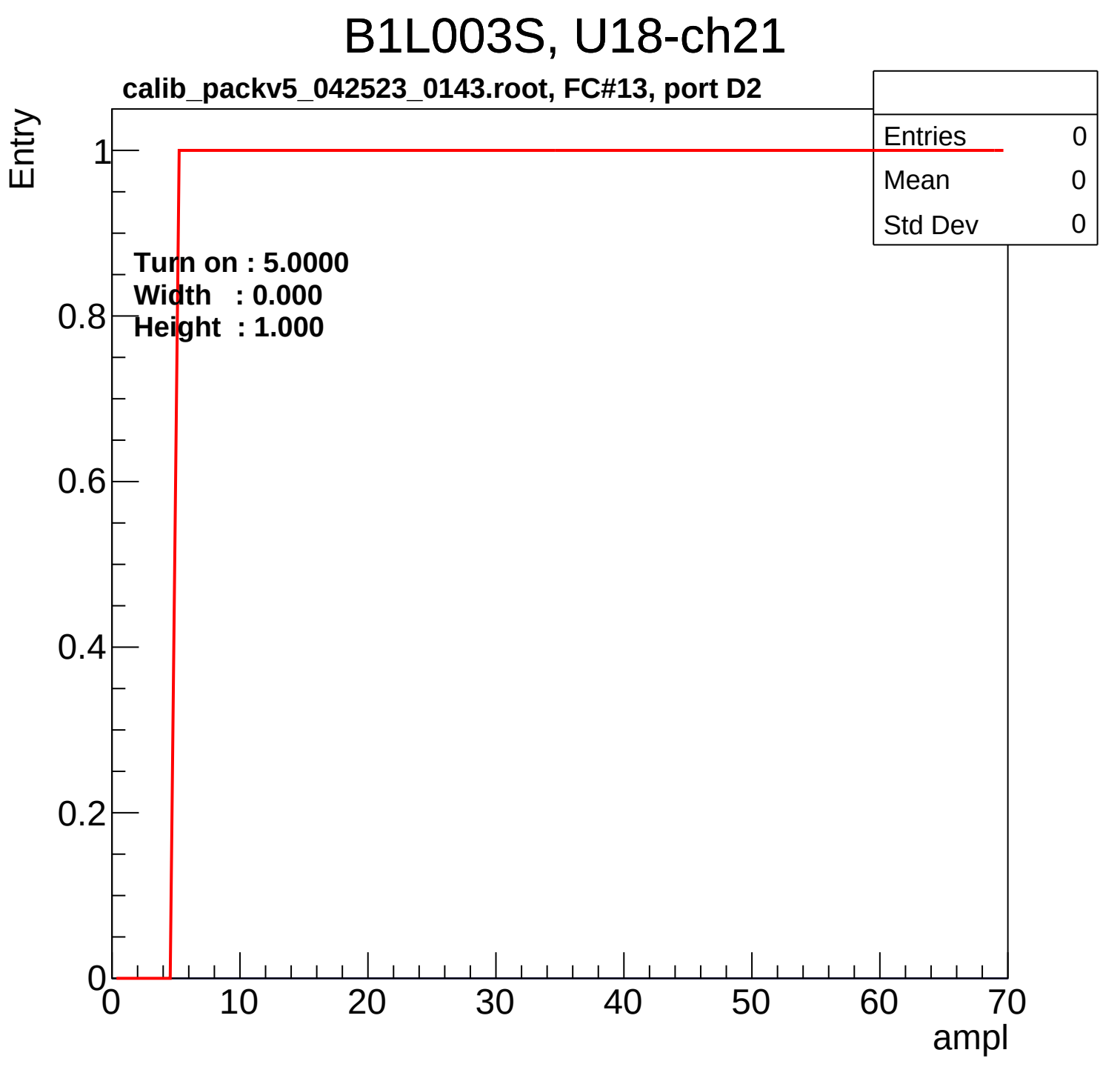
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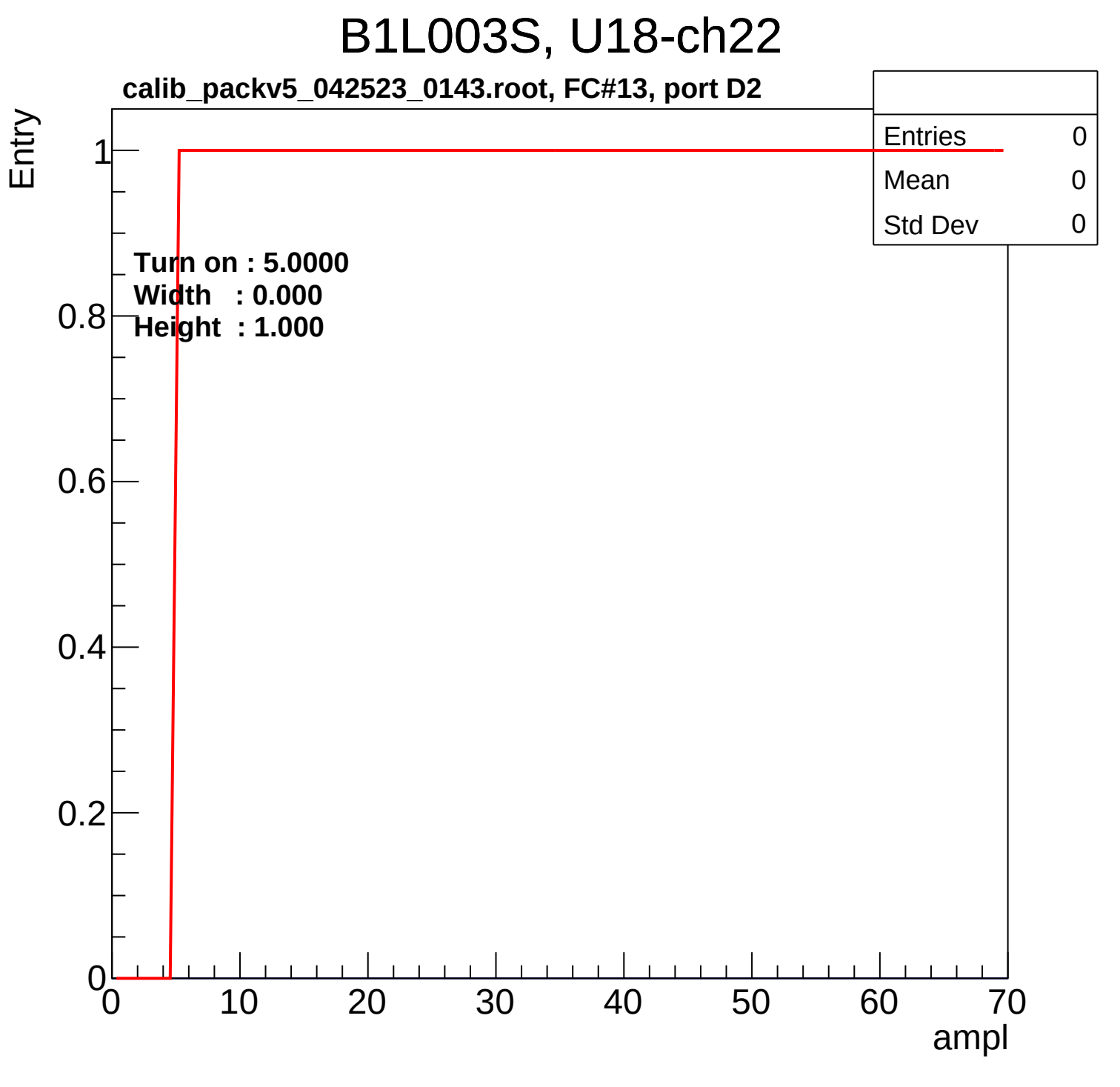
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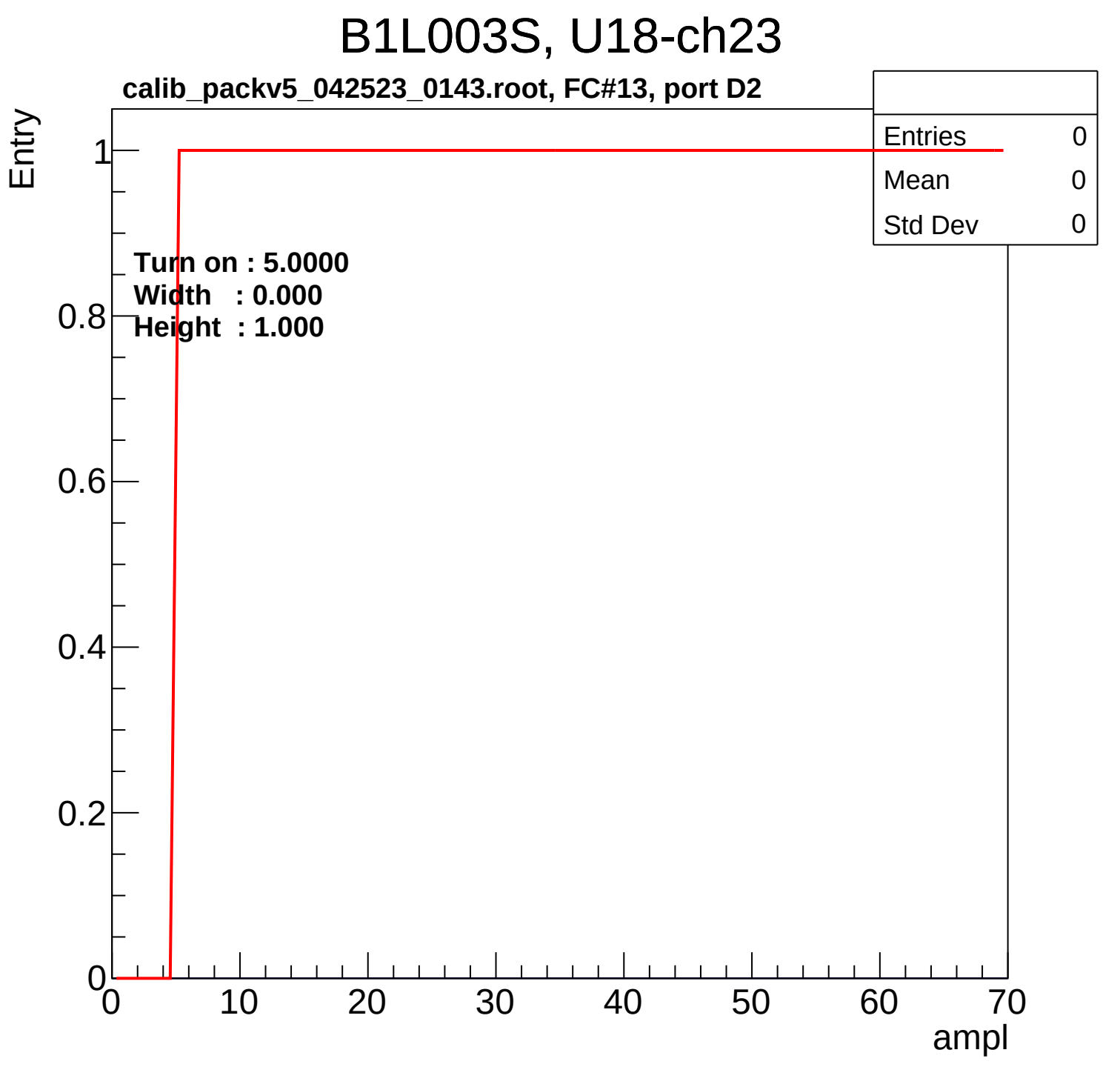
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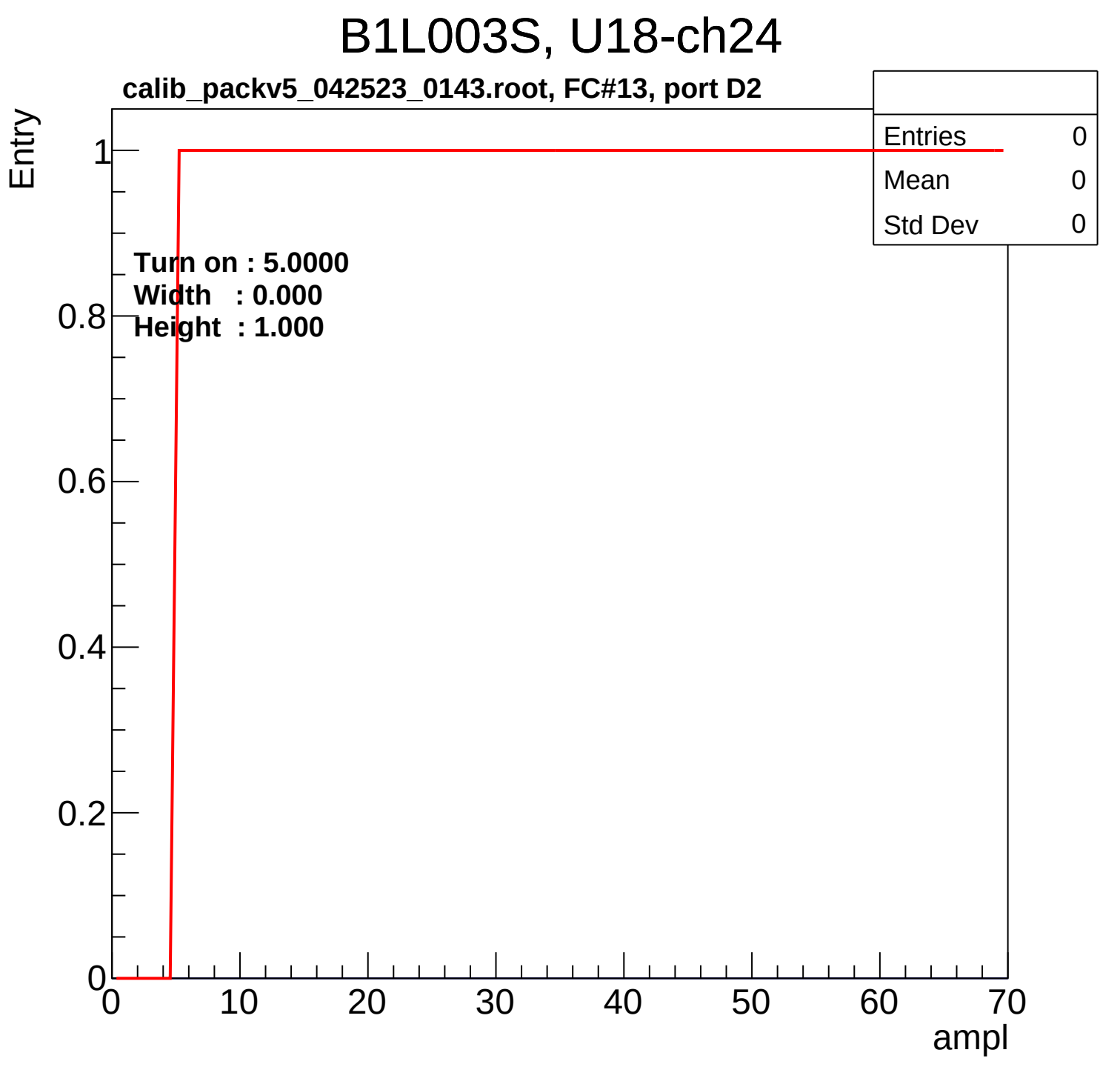
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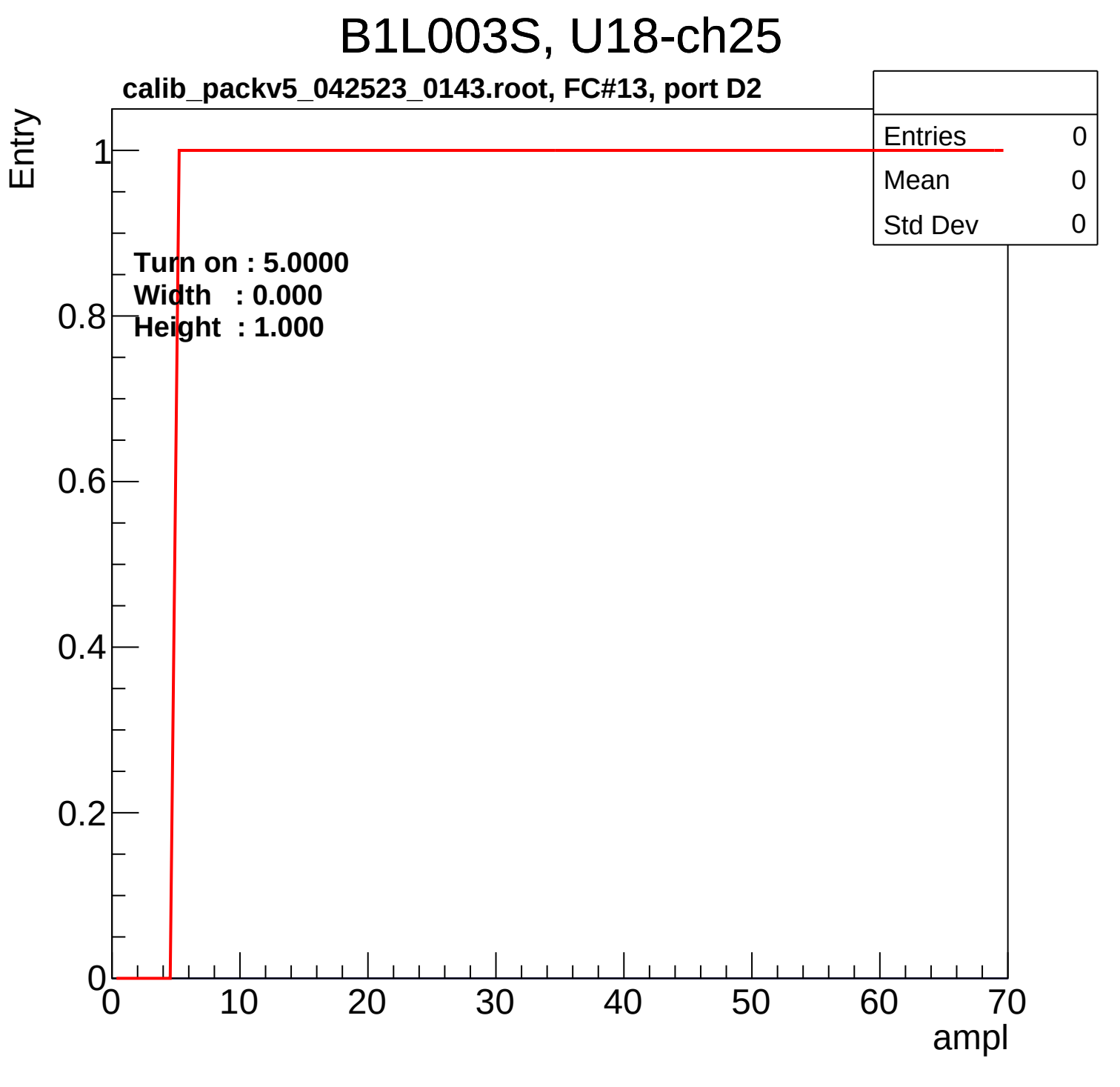
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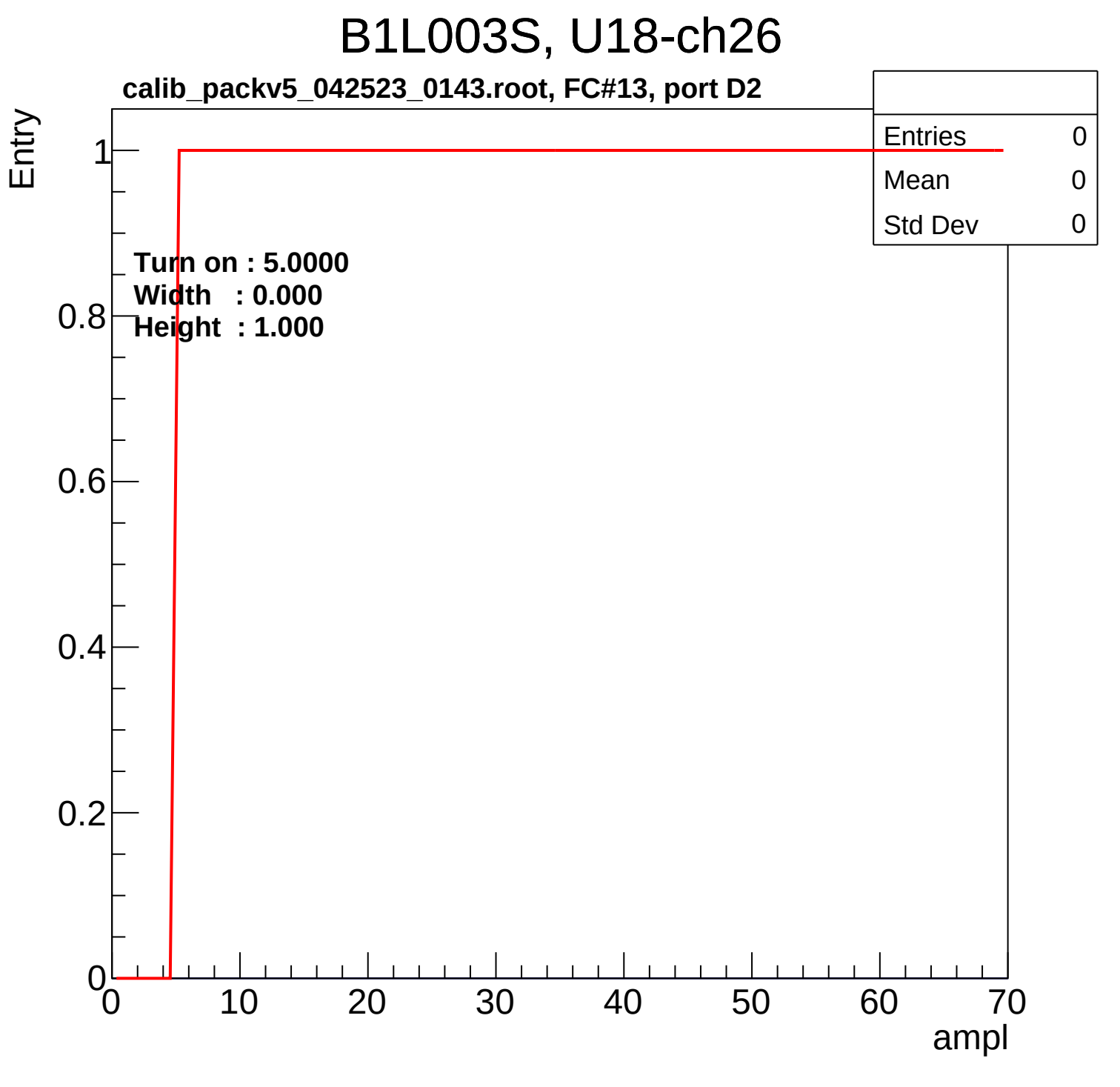
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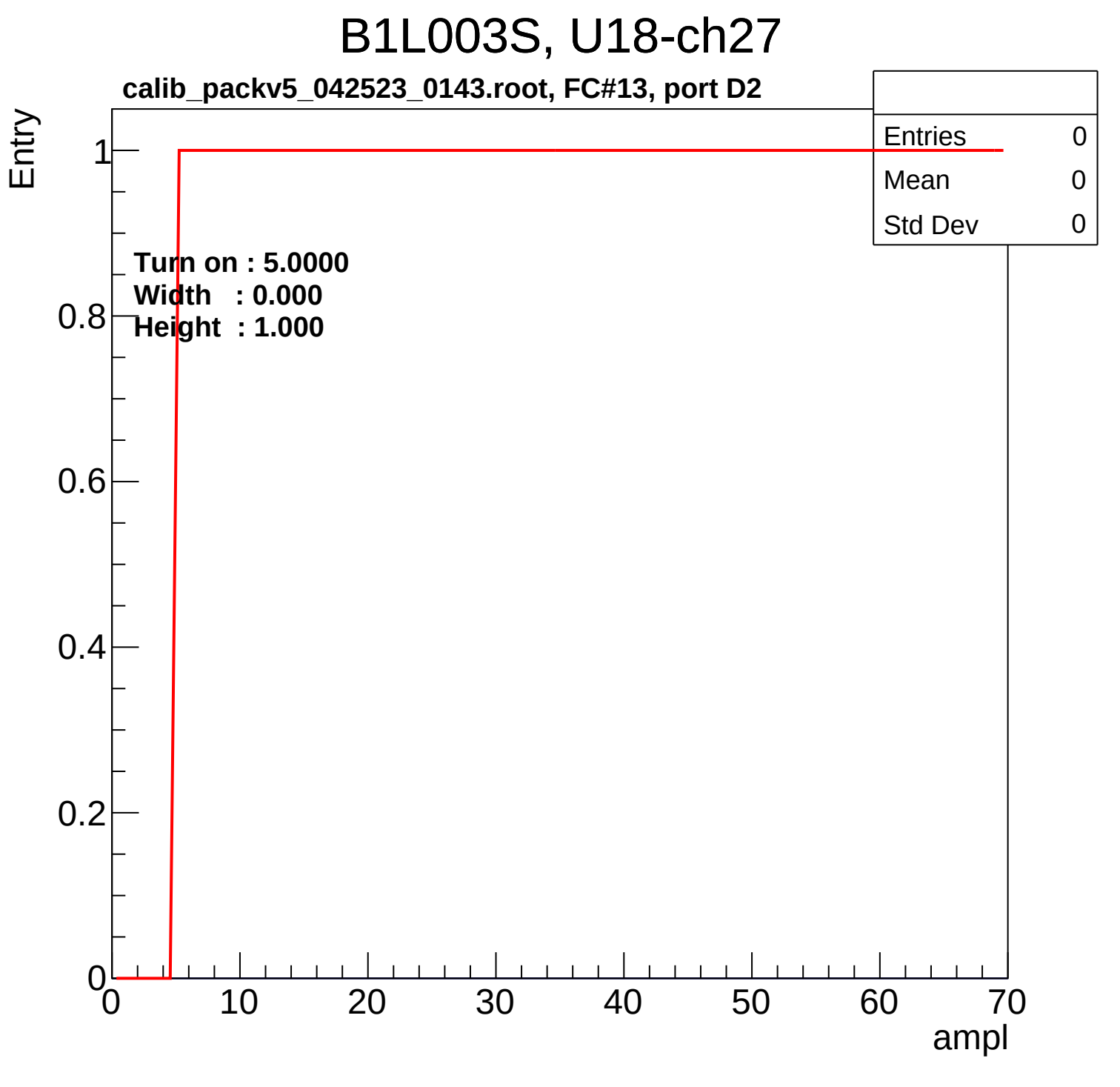
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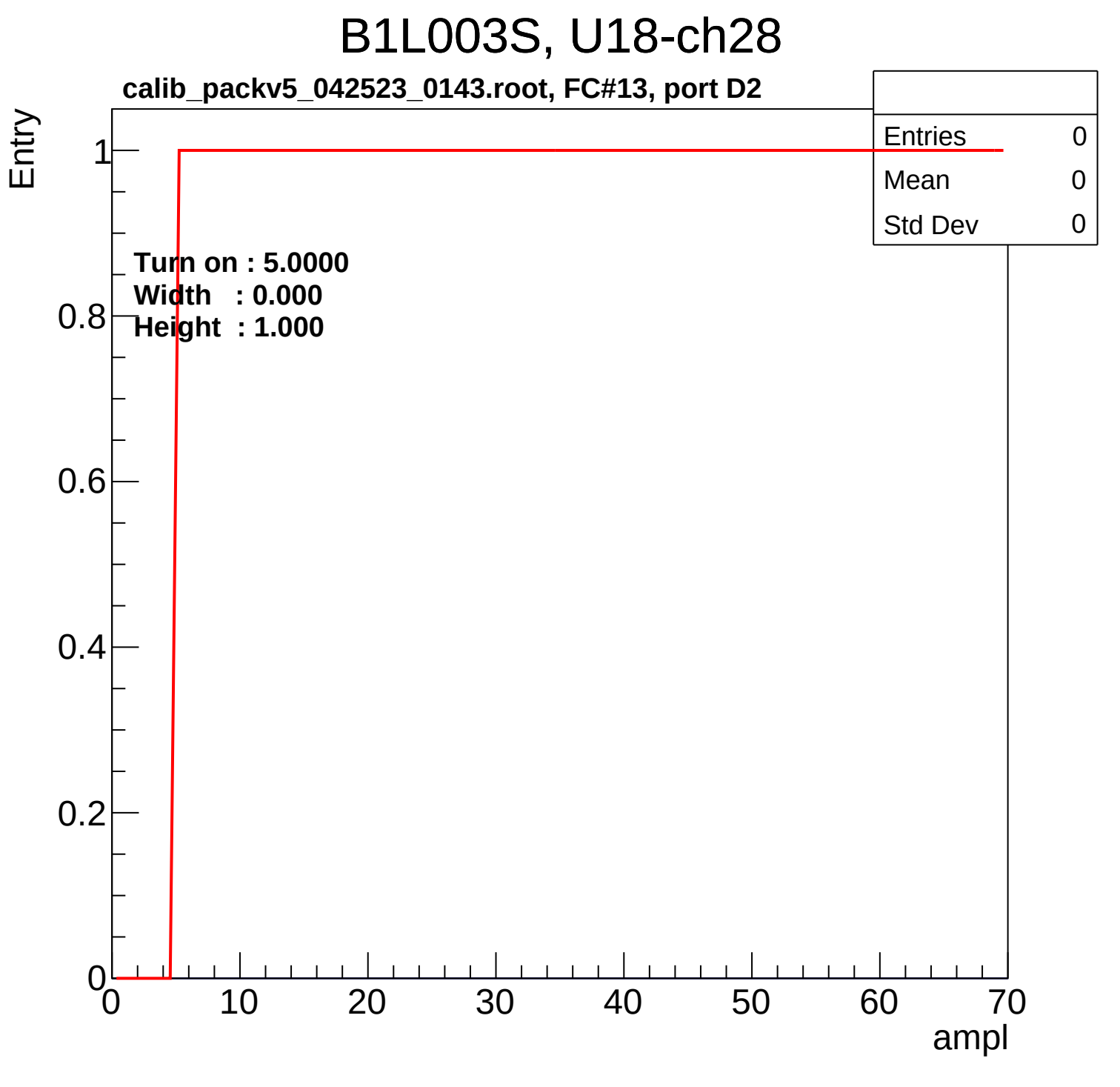
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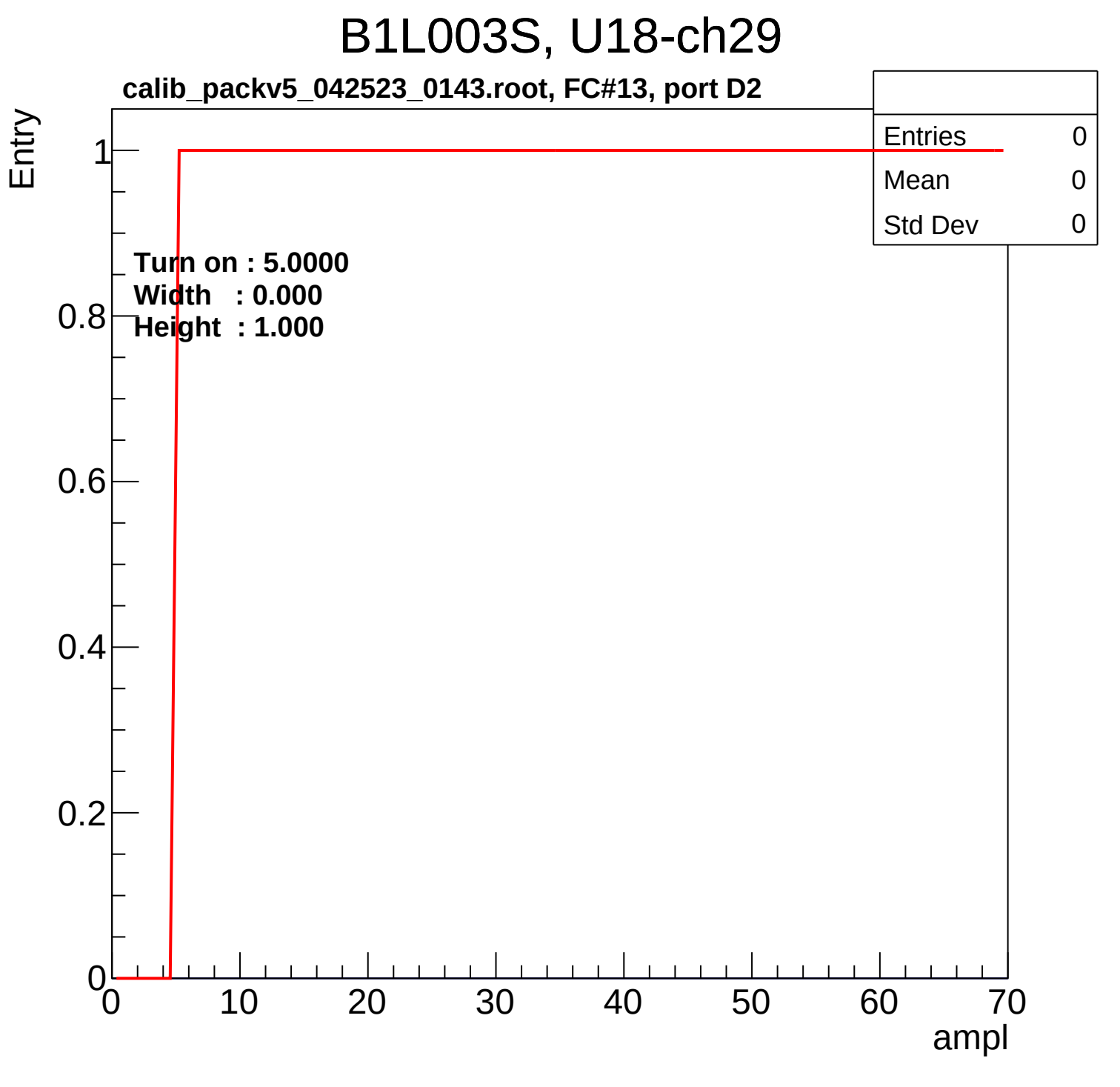
B1L003S, U18-ch29
calib_packv5_042523_0143.root, FC#13, port D2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
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0.6
0.4
0.2
0
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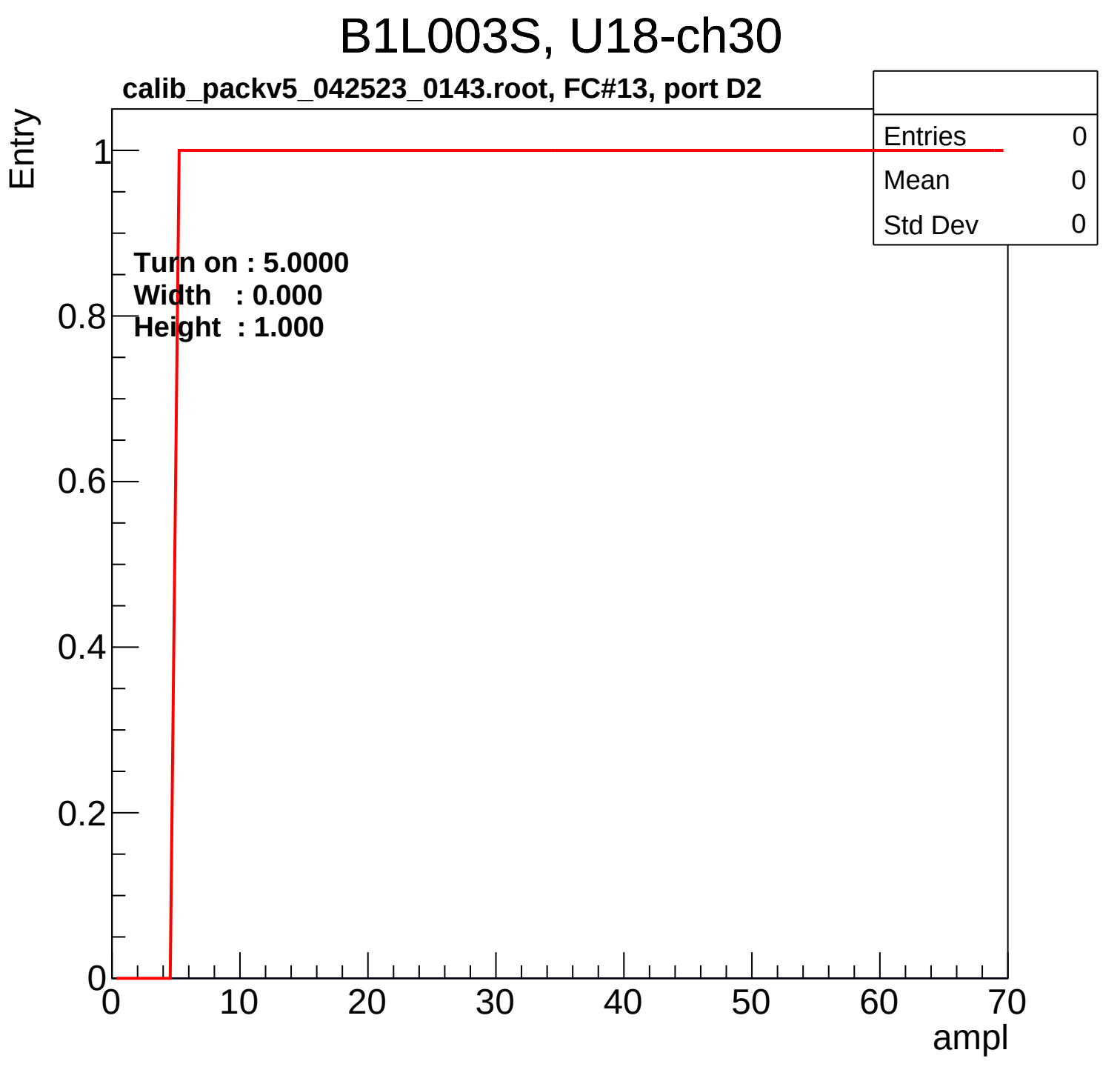
70
ampl


B1L003S, U18-ch30
calib_packv5_042523_0143.root, FC#13, port D2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.6
0.4
0.2
0
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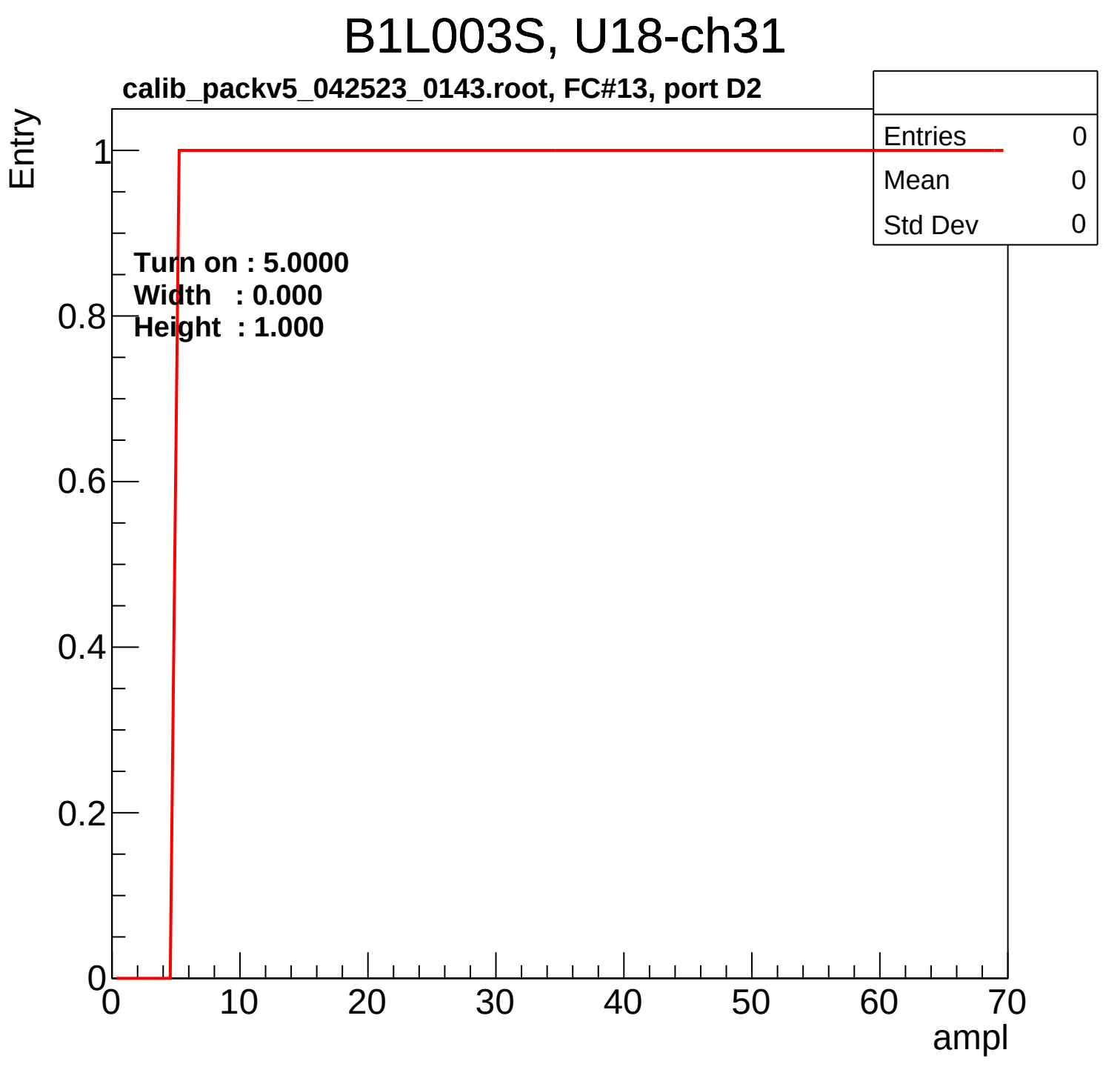
70
ampl


B1L003S, U18-ch31
calib_packv5_042523_0143.root, FC#13, port D2
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
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0.8
0.6
0.4
0.2
0
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10
20
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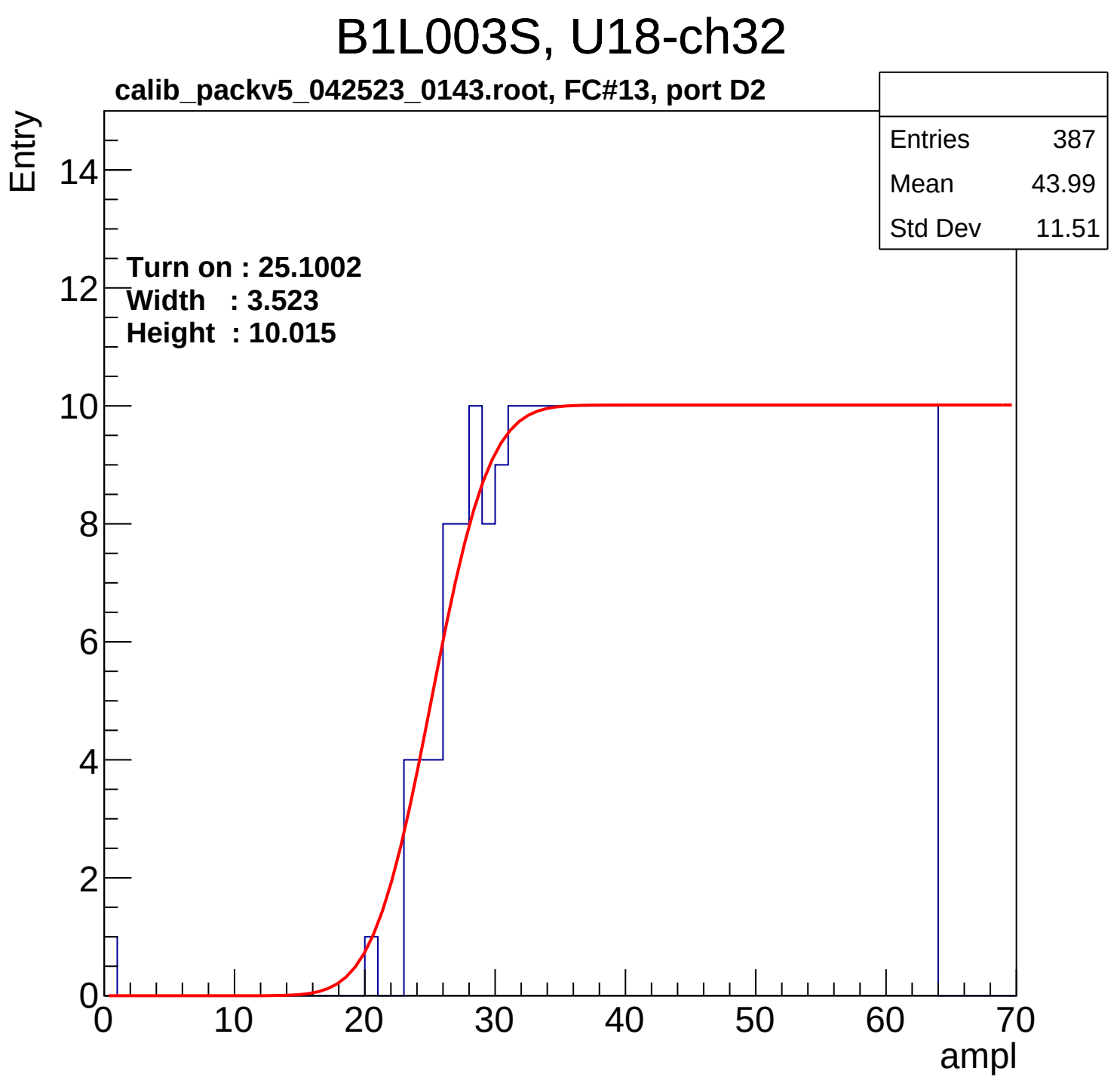
50
60
70
ampl


B1L003S, U18-ch32
calib_packv5_042523_0143.root, FC#13, port D2
Entries 387
Mean 43.99
Std Dev 11.51
Turn on : 25.1002
Width : 3.523
Height : 10.015
Entry
ampl
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2
4
6
8
10
12
14
0
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60
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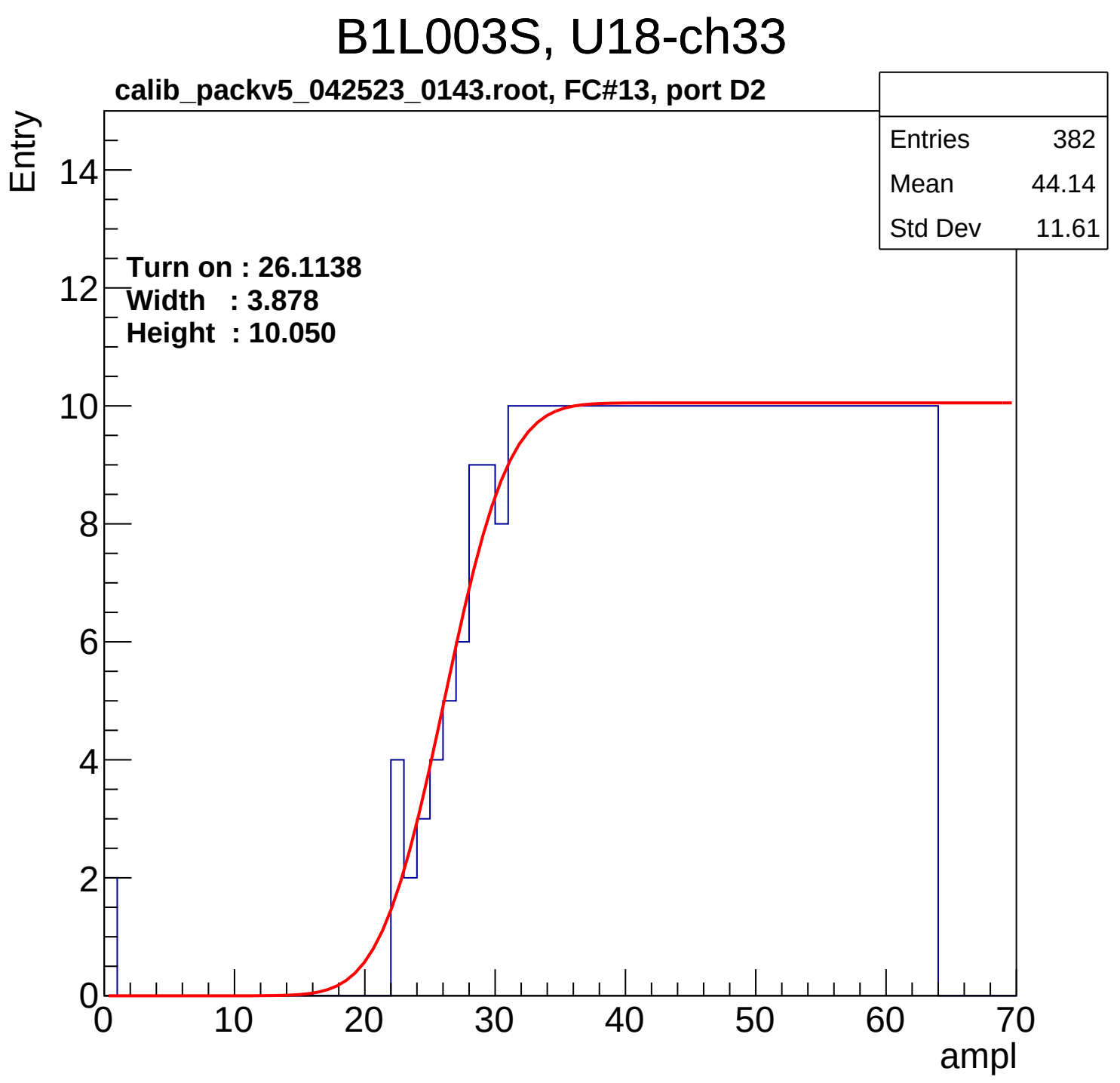
B1L003S, U18-ch33
calib_packv5_042523_0143.root, FC#13, port D2
Entries 382
Mean 44.14
Std Dev 11.61
Turn on : 26.1138
Width : 3.878
Height : 10.050
Entry
ampl
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2
4
6
8
10
12
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0
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60
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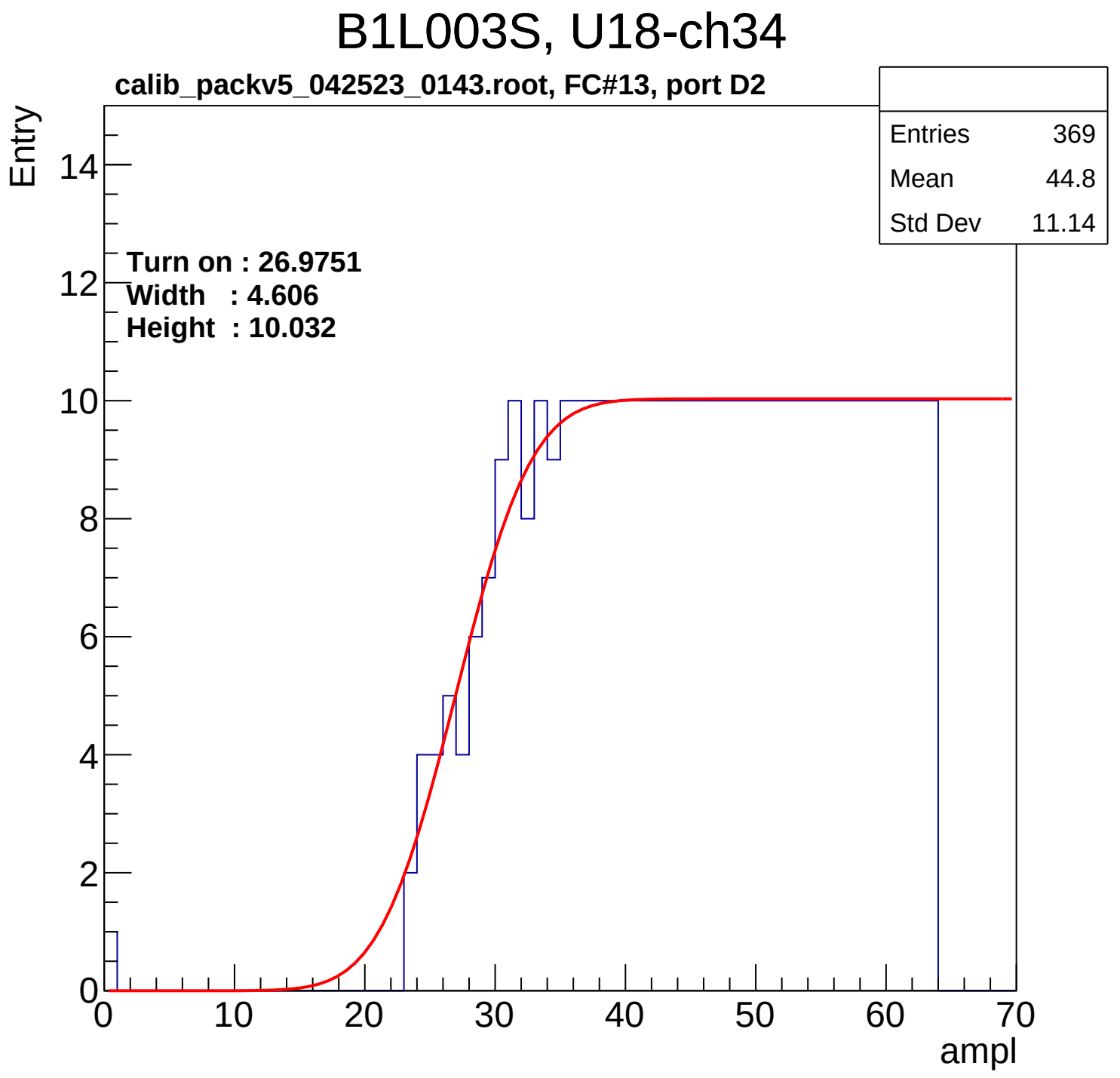
B1L003S, U18-ch34
calib_packv5_042523_0143.root, FC#13, port D2
Entries 369
Mean 44.8
Std Dev 11.14
Turn on : 26.9751
Width : 4.606
Height : 10.032
Entry
ampl
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2
4
6
8
10
12
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0
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40
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60
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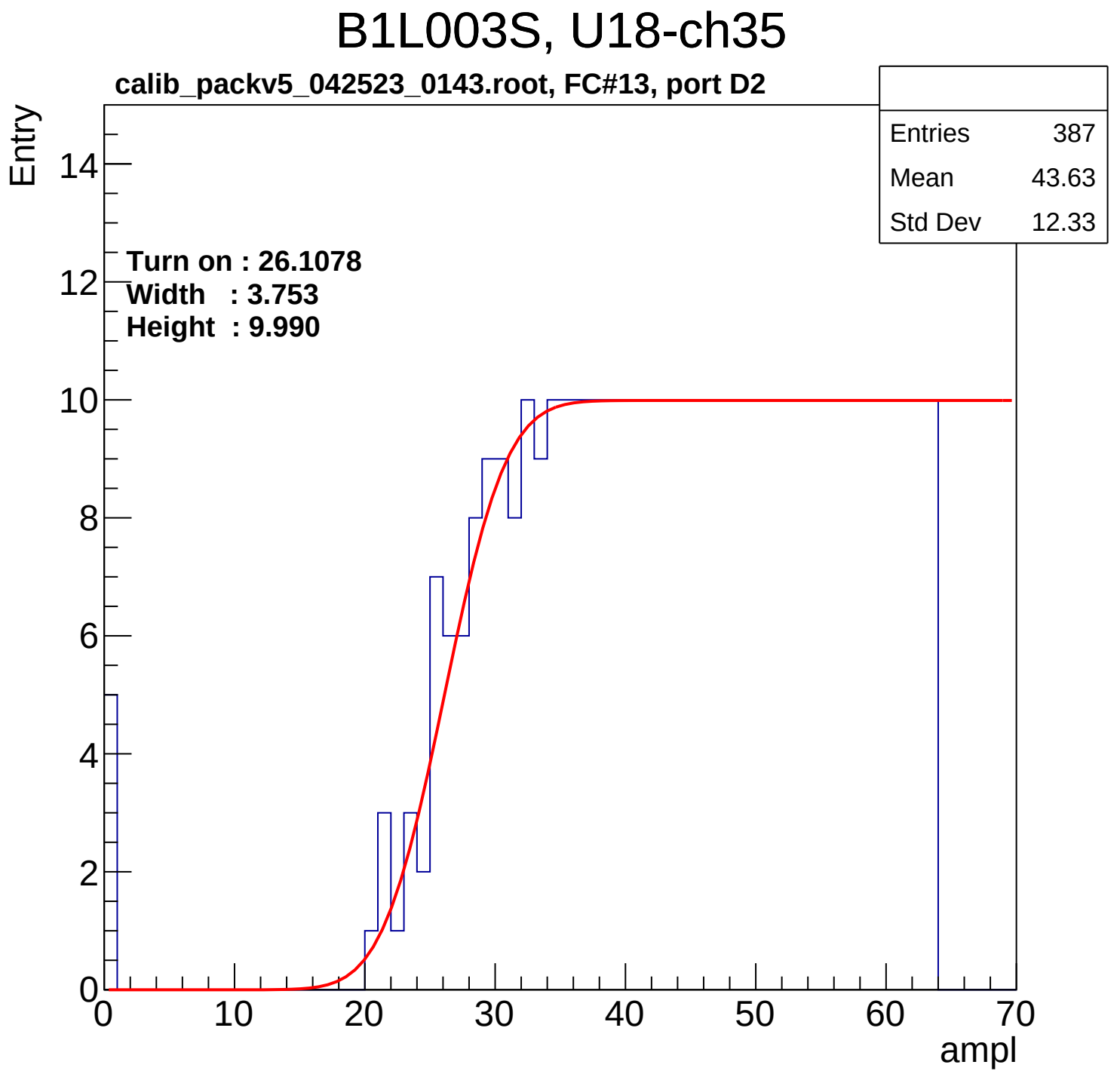
B1L003S, U18-ch35
calib_packv5_042523_0143.root, FC#13, port D2
Entries 387
Mean 43.63
Std Dev 12.33
Turn on : 26.1078
Width : 3.753
Height : 9.990
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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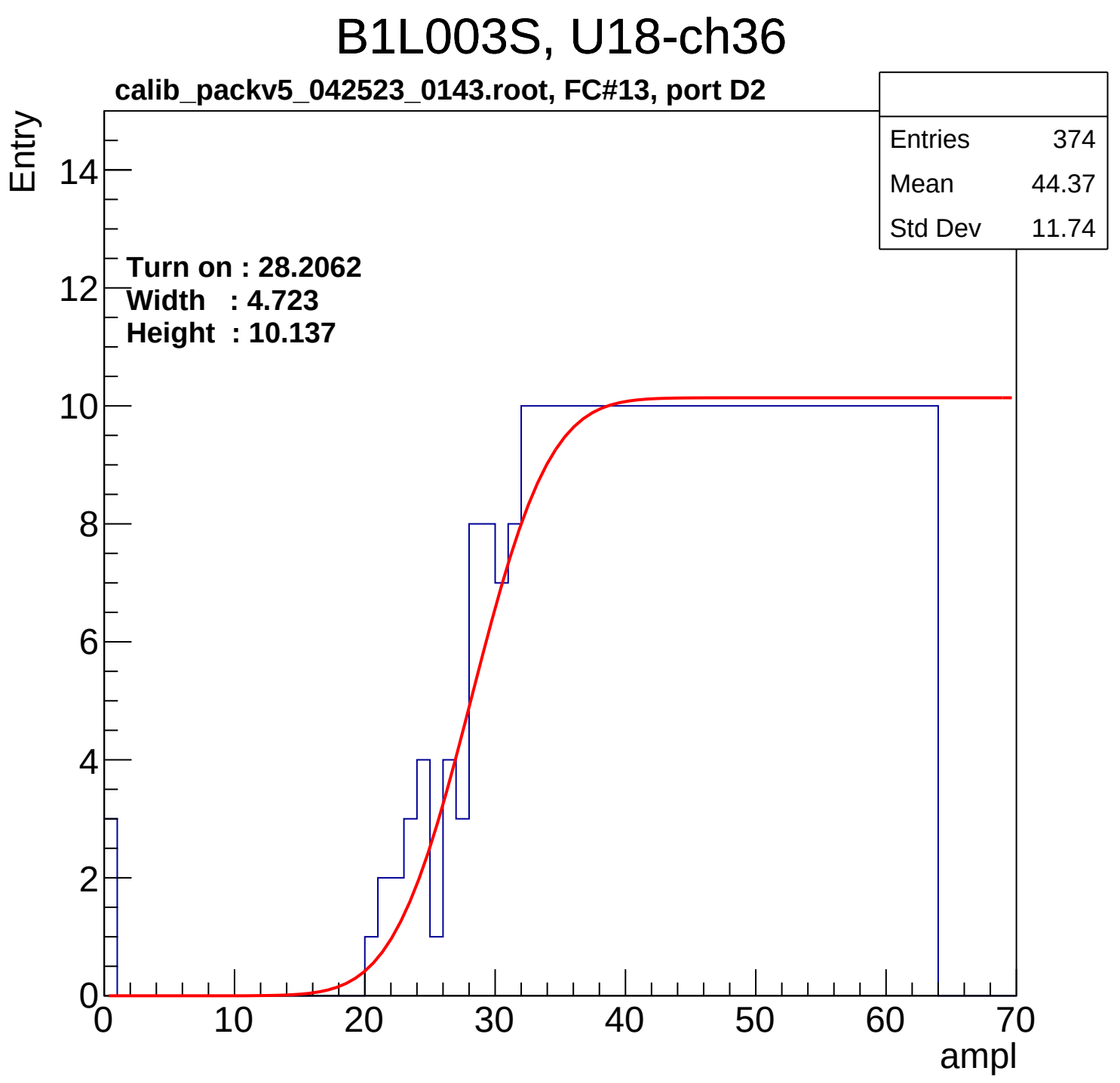
B1L003S, U18-ch36
calib_packv5_042523_0143.root, FC#13, port D2
Entries 374
Mean 44.37
Std Dev 11.74
Turn on : 28.2062
Width : 4.723
Height : 10.137
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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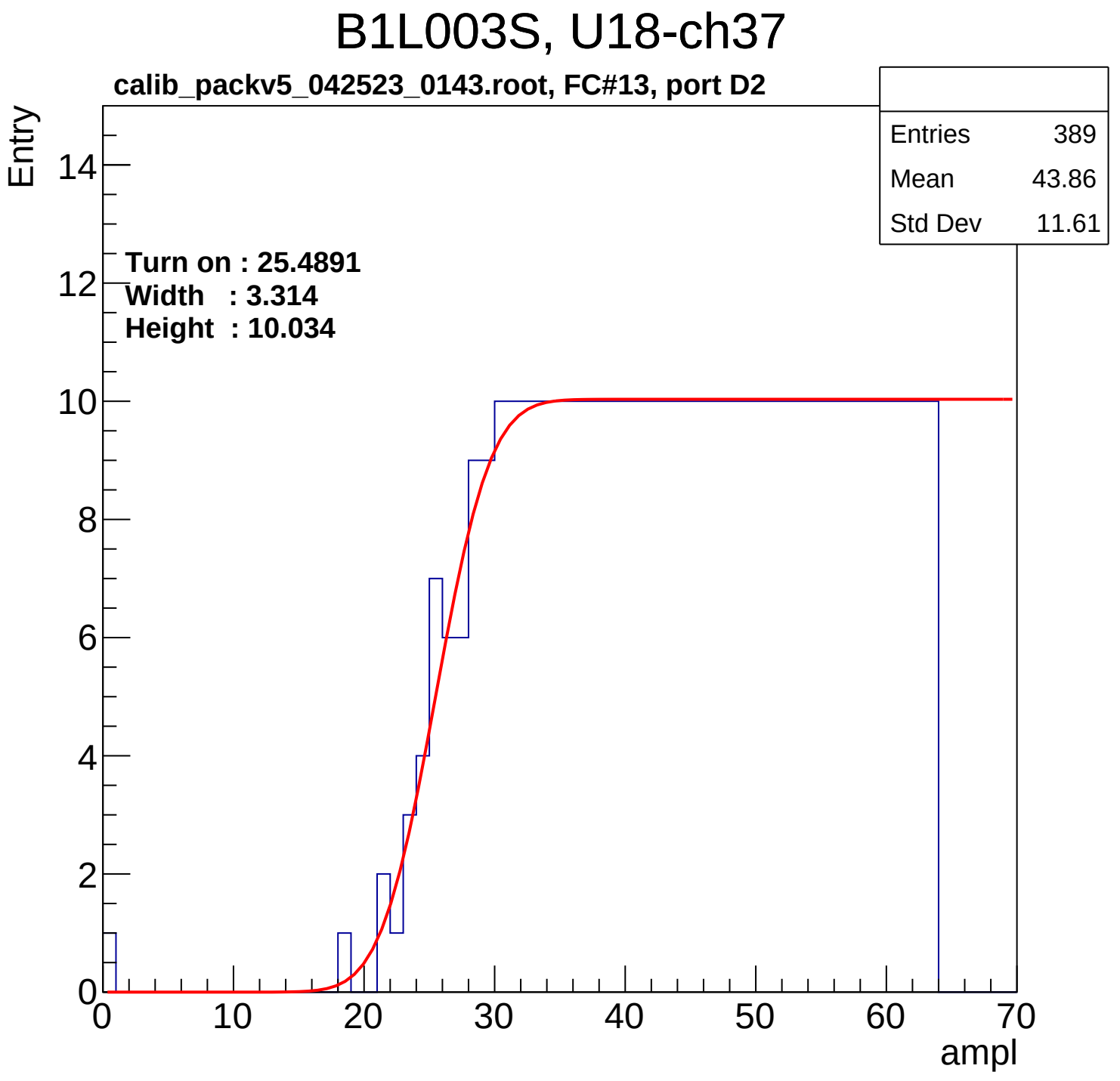
40
50
60
70


B1L003S, U18-ch37
calib_packv5_042523_0143.root, FC#13, port D2
Entries 389
Mean 43.86
Std Dev 11.61
Turn on : 25.4891
Width : 3.314
Height : 10.034
Entry
ampl
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2
4
6
8
10
12
14
0
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40
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60
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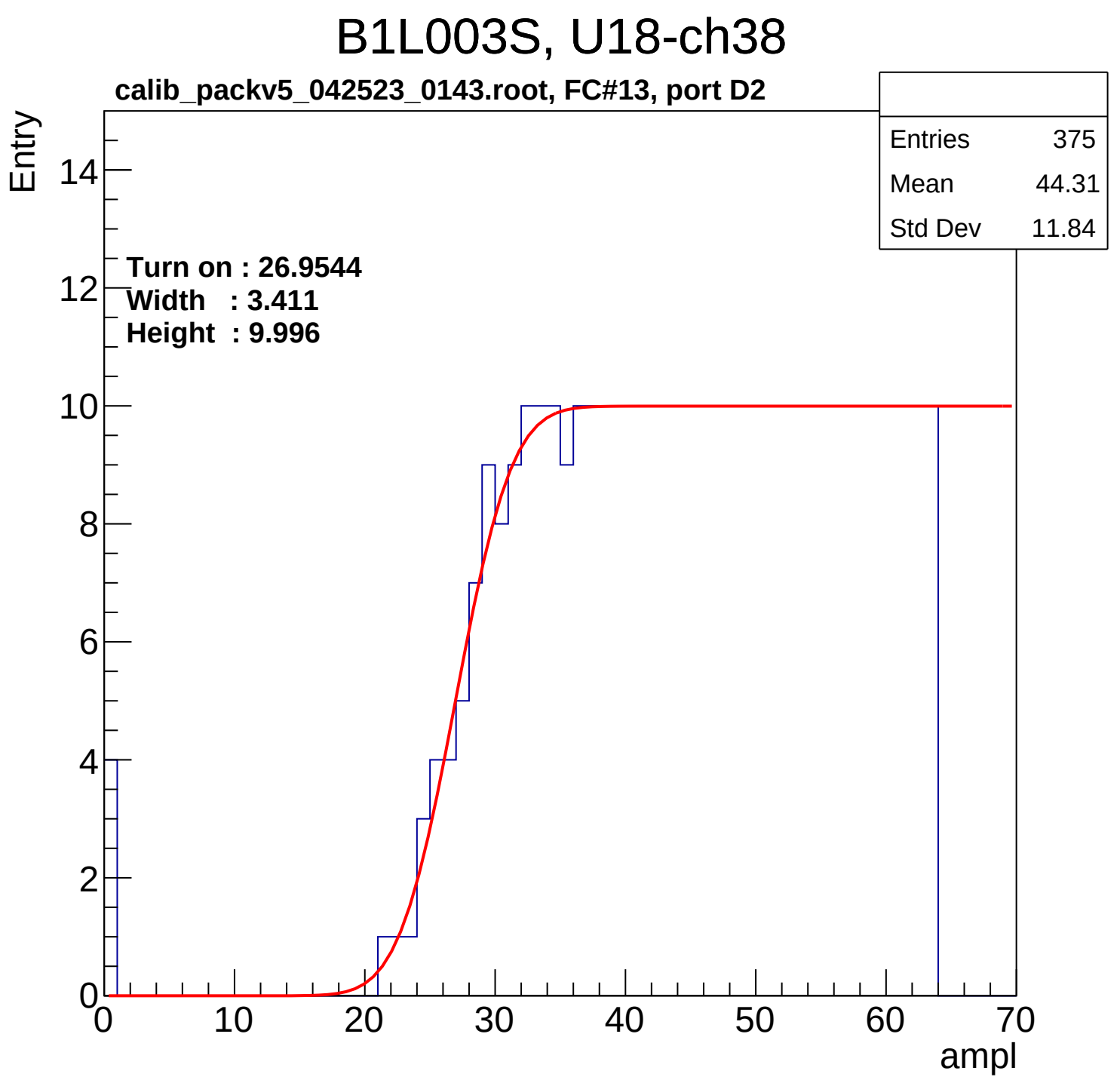
B1L003S, U18-ch38
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.31
Std Dev 11.84
Turn on : 26.9544
Width : 3.411
Height : 9.996
Entry
ampl
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2
4
6
8
10
12
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0
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60
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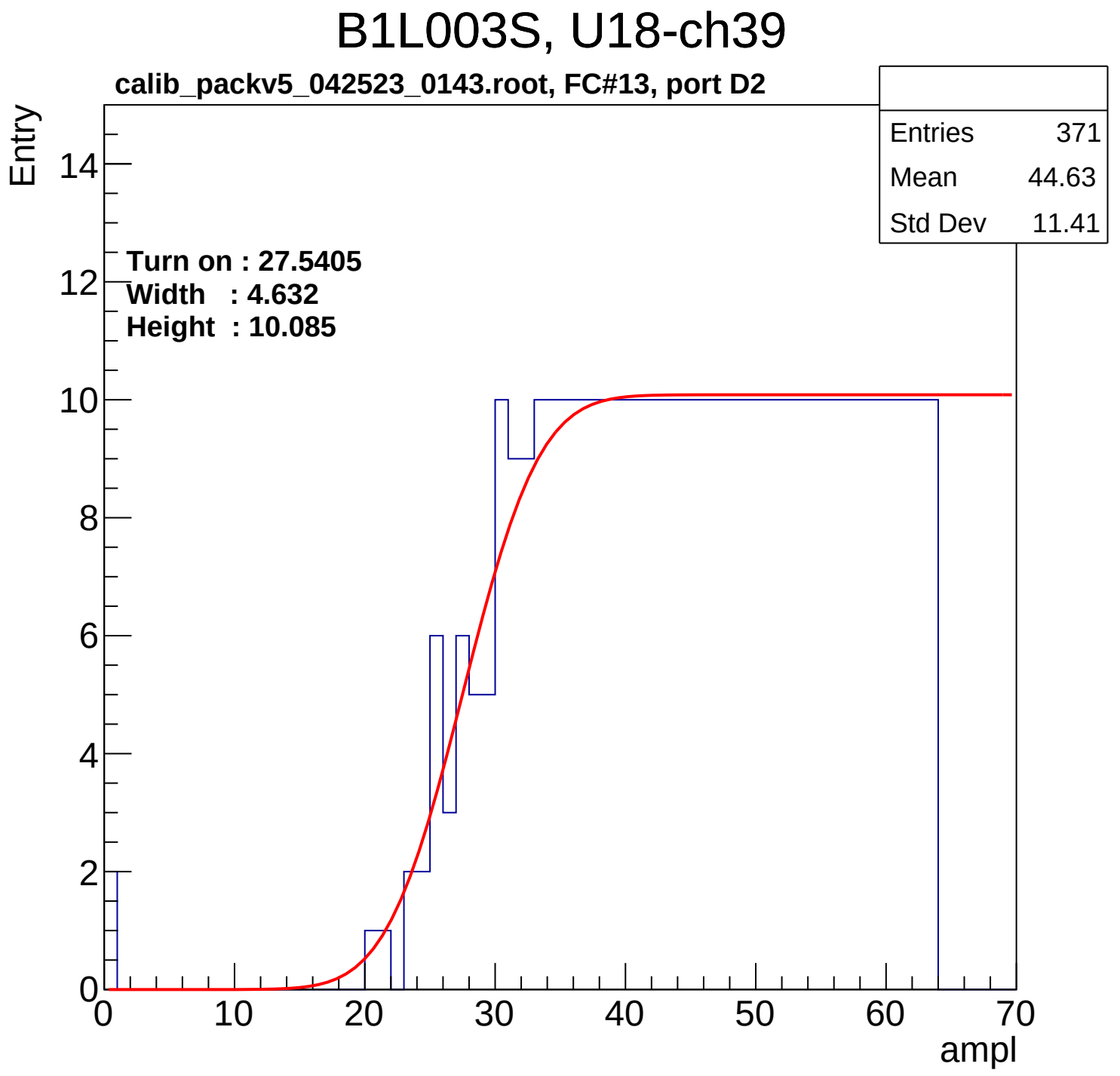
B1L003S, U18-ch39
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.63
Std Dev 11.41
Turn on : 27.5405
Width : 4.632
Height : 10.085
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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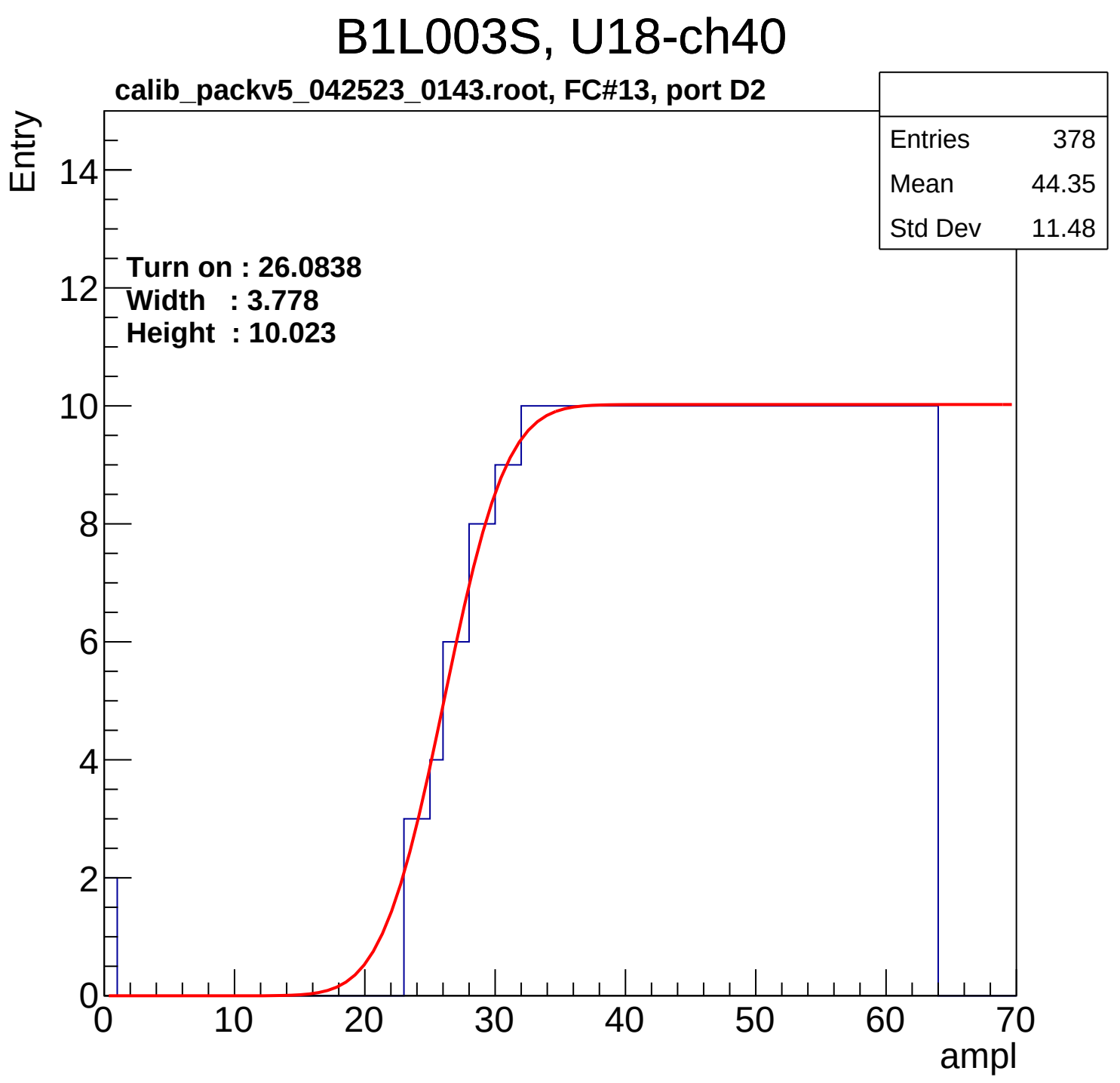
B1L003S, U18-ch40
calib_packv5_042523_0143.root, FC#13, port D2
Entries 378
Mean 44.35
Std Dev 11.48
Turn on : 26.0838
Width : 3.778
Height : 10.023
Entry
ampl
0
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4
6
8
10
12
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0
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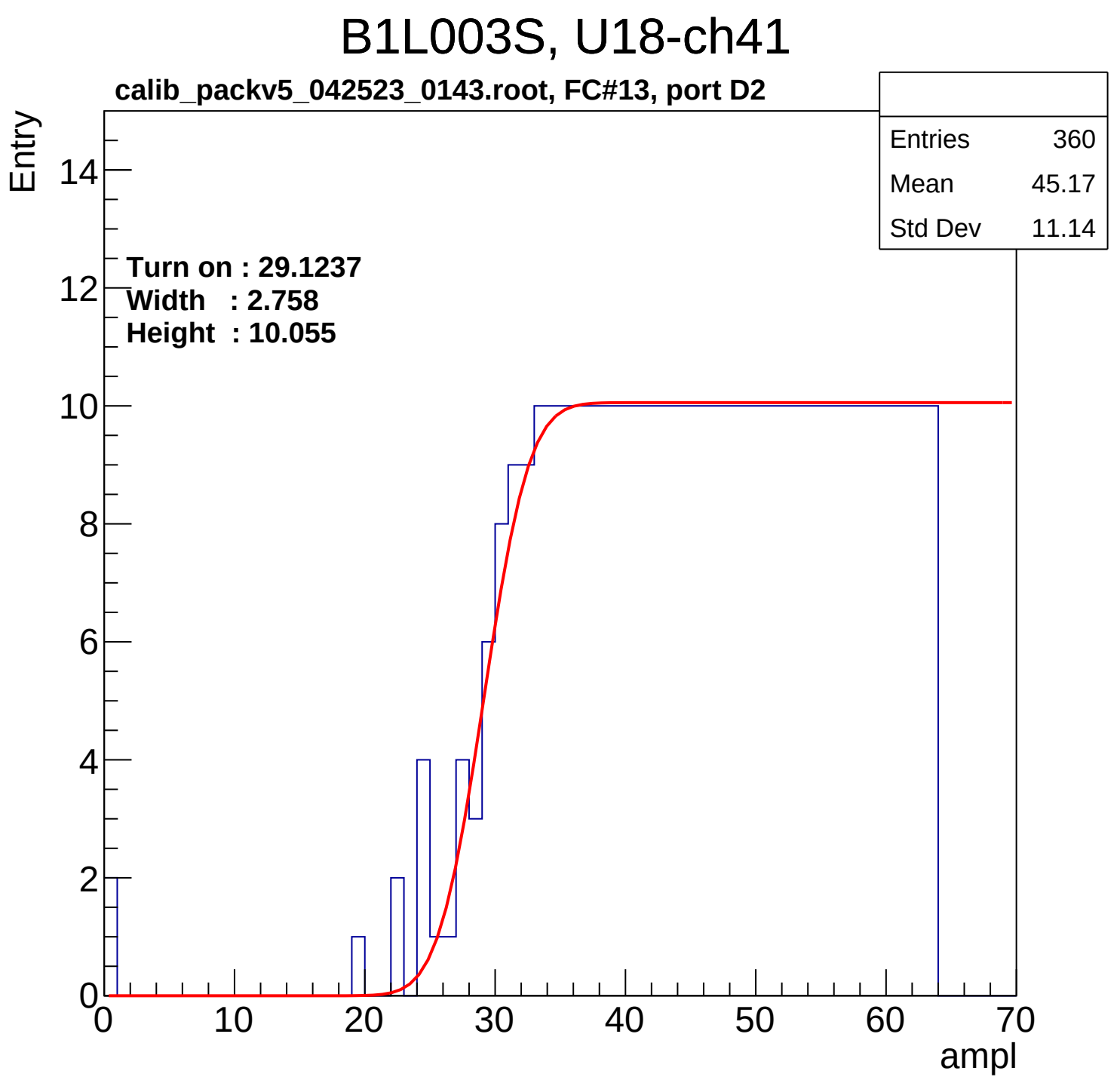
B1L003S, U18-ch41
calib_packv5_042523_0143.root, FC#13, port D2
Entries 360
Mean 45.17
Std Dev 11.14
Turn on : 29.1237
Width : 2.758
Height : 10.055
Entry
ampl
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2
4
6
8
10
12
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0
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60
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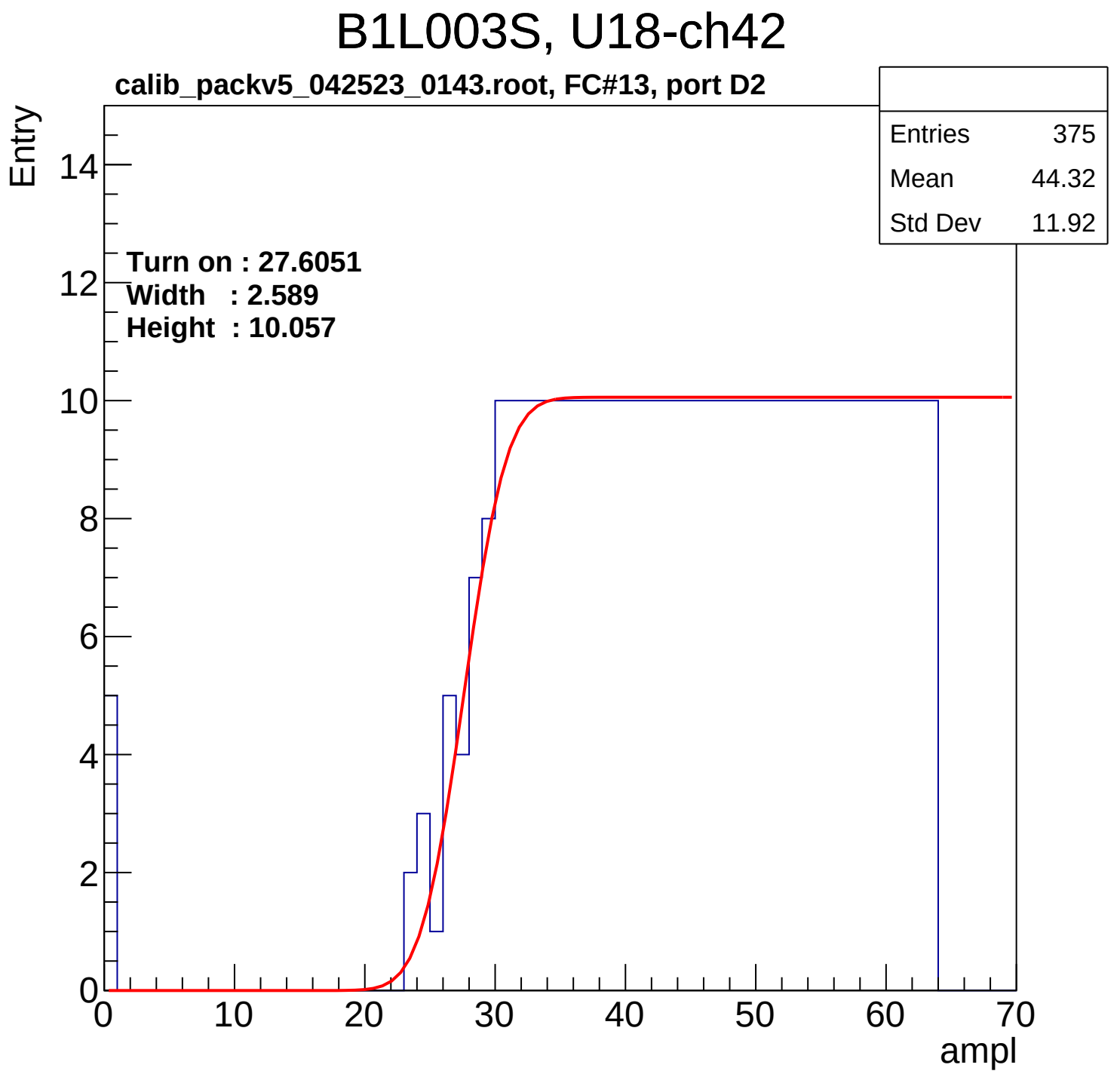
B1L003S, U18-ch42
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.32
Std Dev 11.92
Turn on : 27.6051
Width : 2.589
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
14
0
10
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40
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60
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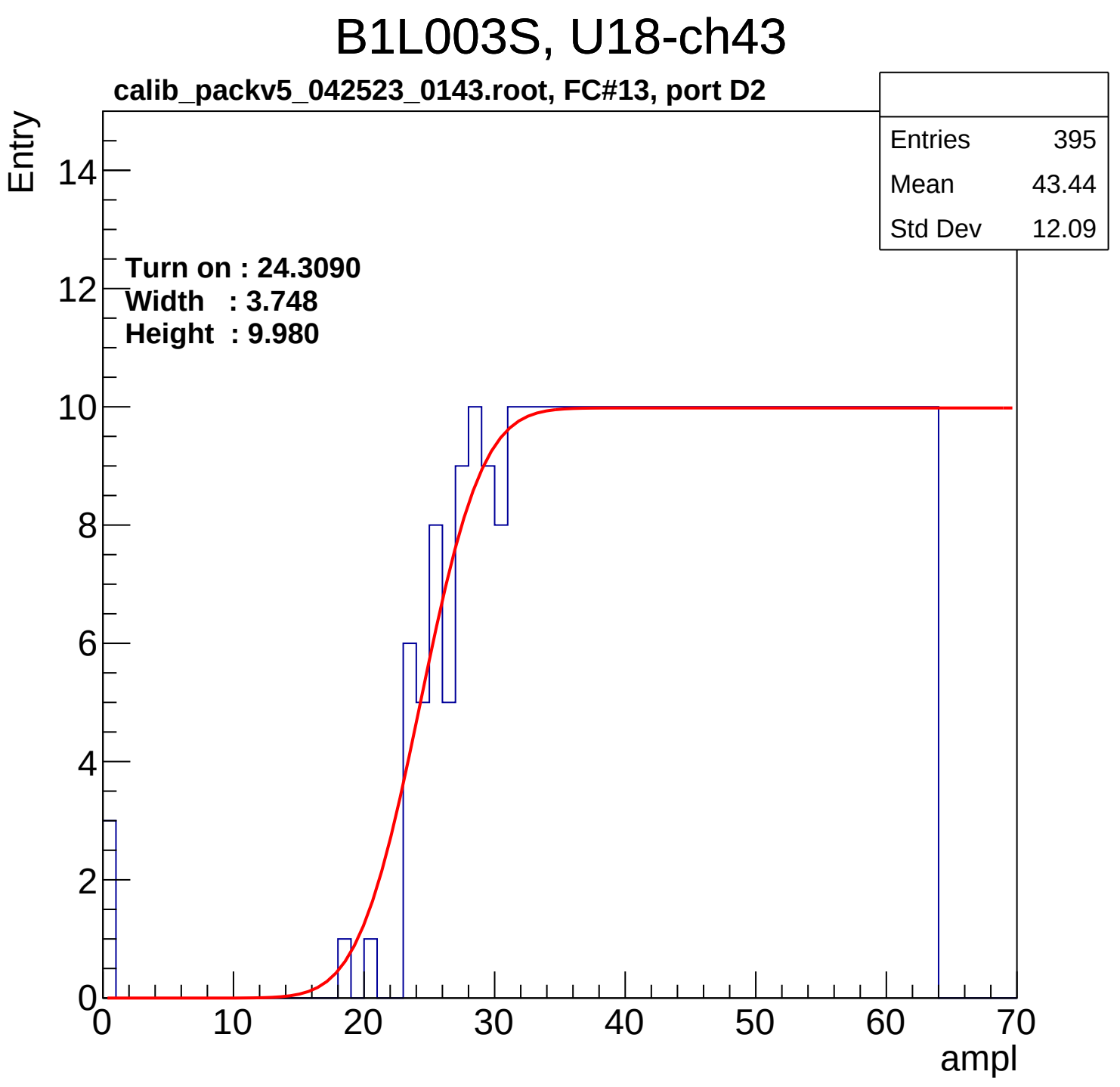
B1L003S, U18-ch43
calib_packv5_042523_0143.root, FC#13, port D2
Entries 395
Mean 43.44
Std Dev 12.09
Turn on : 24.3090
Width : 3.748
Height : 9.980
Entry
ampl
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2
4
6
8
10
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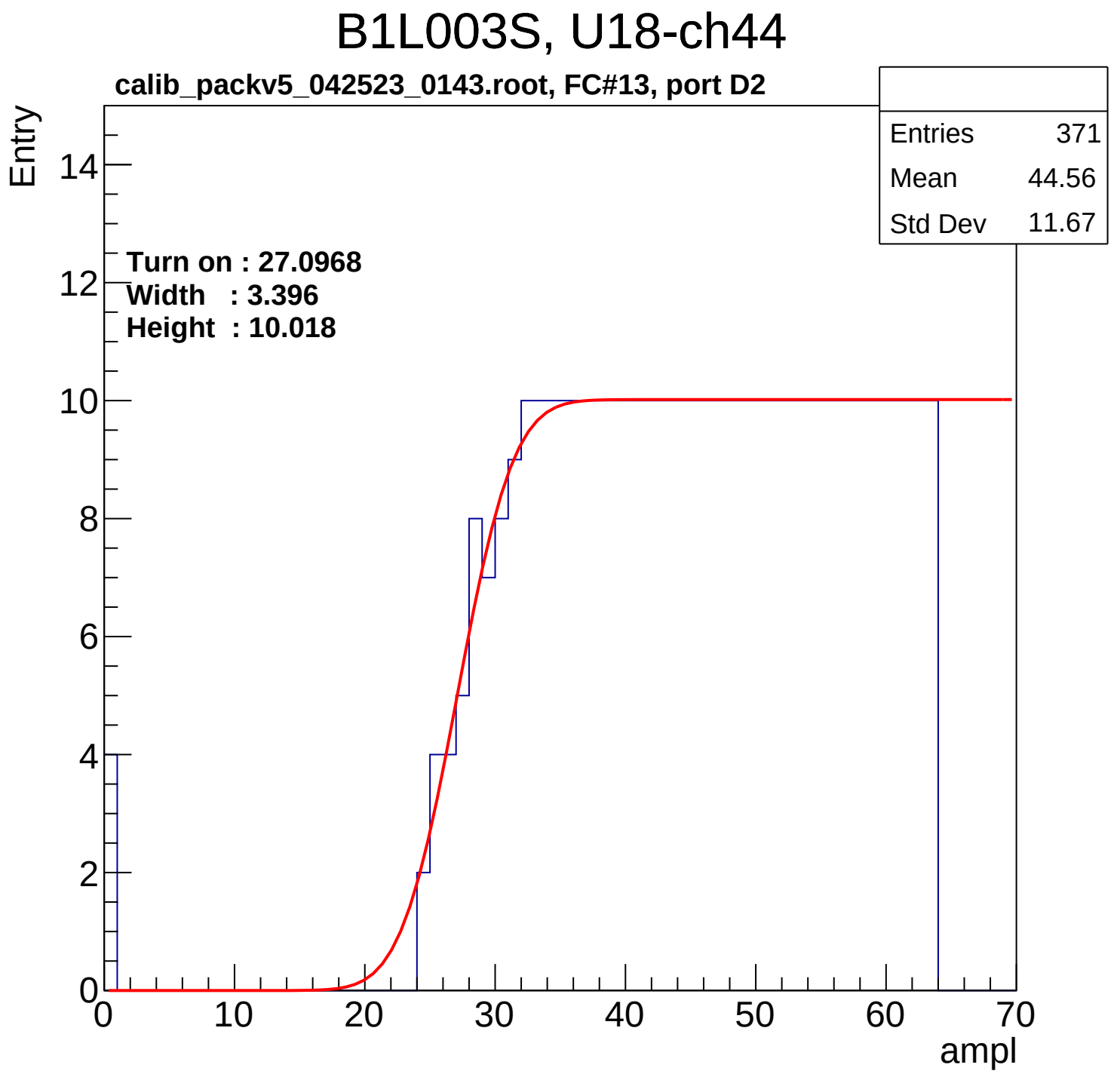
B1L003S, U18-ch44
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.56
Std Dev 11.67
Turn on : 27.0968
Width : 3.396
Height : 10.018
Entry
ampl
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8
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0
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60
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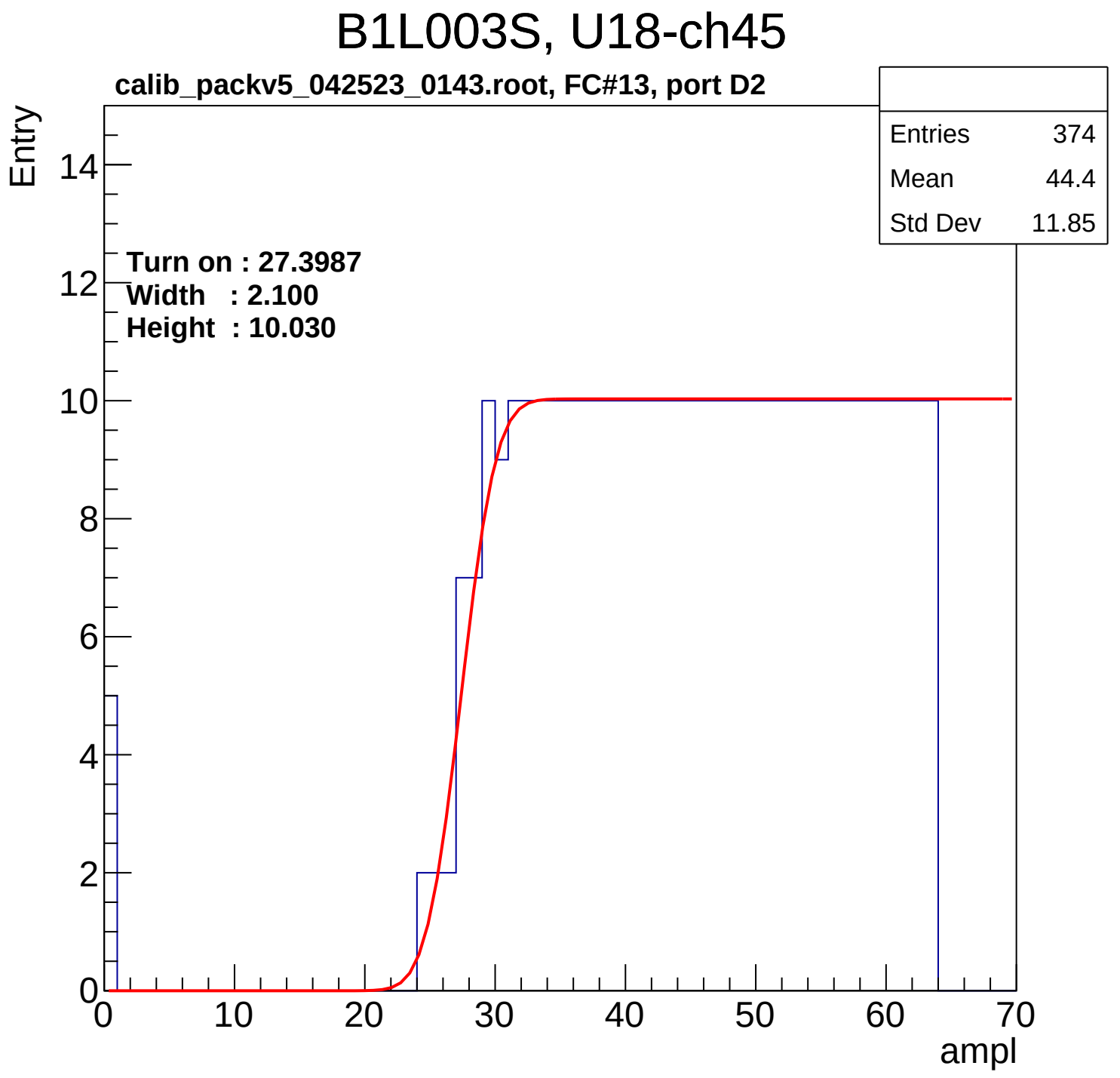
B1L003S, U18-ch45
calib_packv5_042523_0143.root, FC#13, port D2
Entries 374
Mean 44.4
Std Dev 11.85
Turn on : 27.3987
Width : 2.100
Height : 10.030
Entry
ampl
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2
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6
8
10
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0
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60
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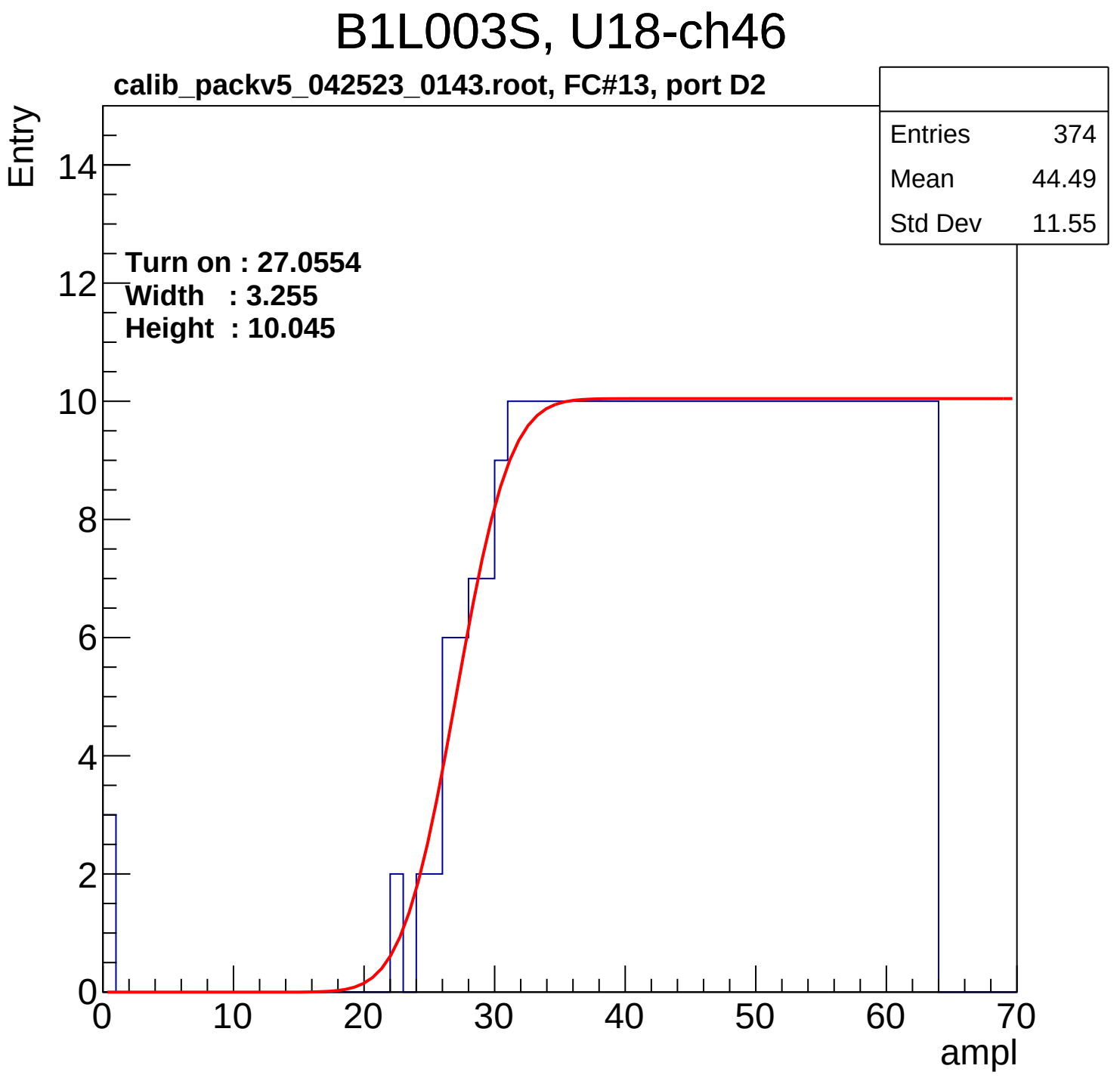
B1L003S, U18-ch46
calib_packv5_042523_0143.root, FC#13, port D2
Entries 374
Mean 44.49
Std Dev 11.55
Turn on : 27.0554
Width : 3.255
Height : 10.045
Entry
ampl
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4
6
8
10
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0
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60
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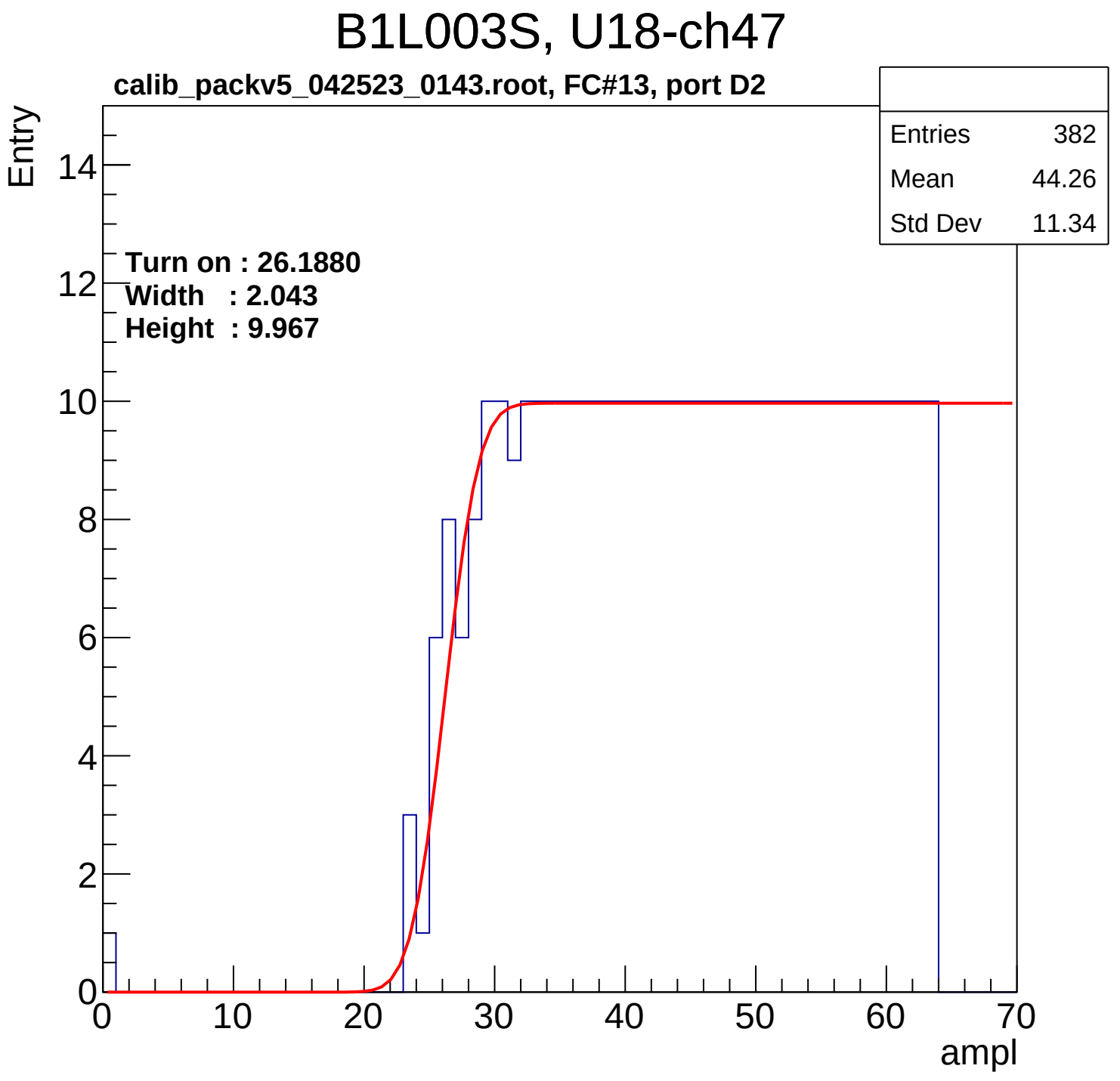
B1L003S, U18-ch47
calib_packv5_042523_0143.root, FC#13, port D2
Entries 382
Mean 44.26
Std Dev 11.34
Turn on : 26.1880
Width : 2.043
Height : 9.967
Entry
ampl
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2
4
6
8
10
12
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0
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60
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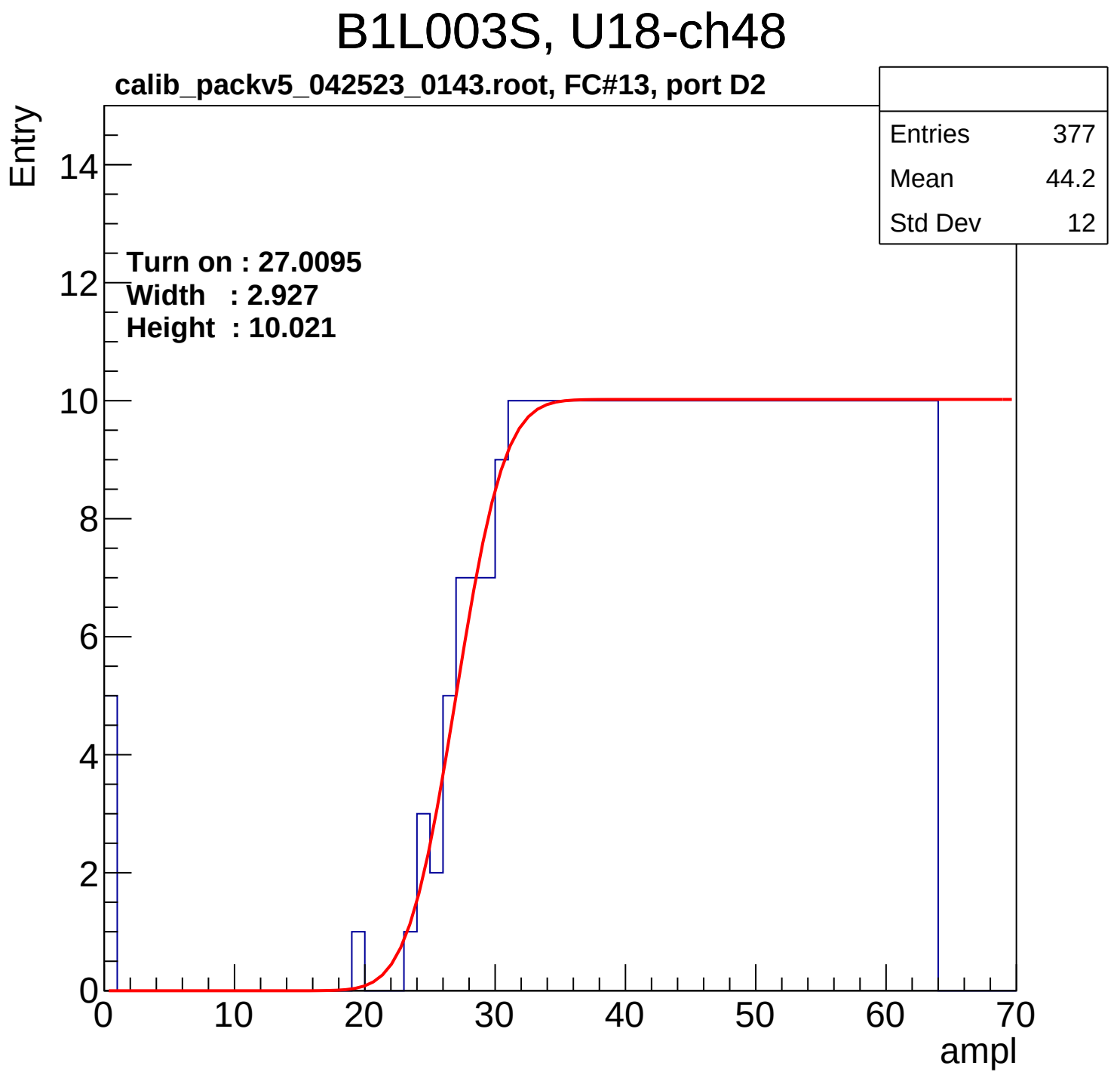
B1L003S, U18-ch48
calib_packv5_042523_0143.root, FC#13, port D2
Entries 377
Mean 44.2
Std Dev 12
Turn on : 27.0095
Width : 2.927
Height : 10.021
Entry
ampl
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4
6
8
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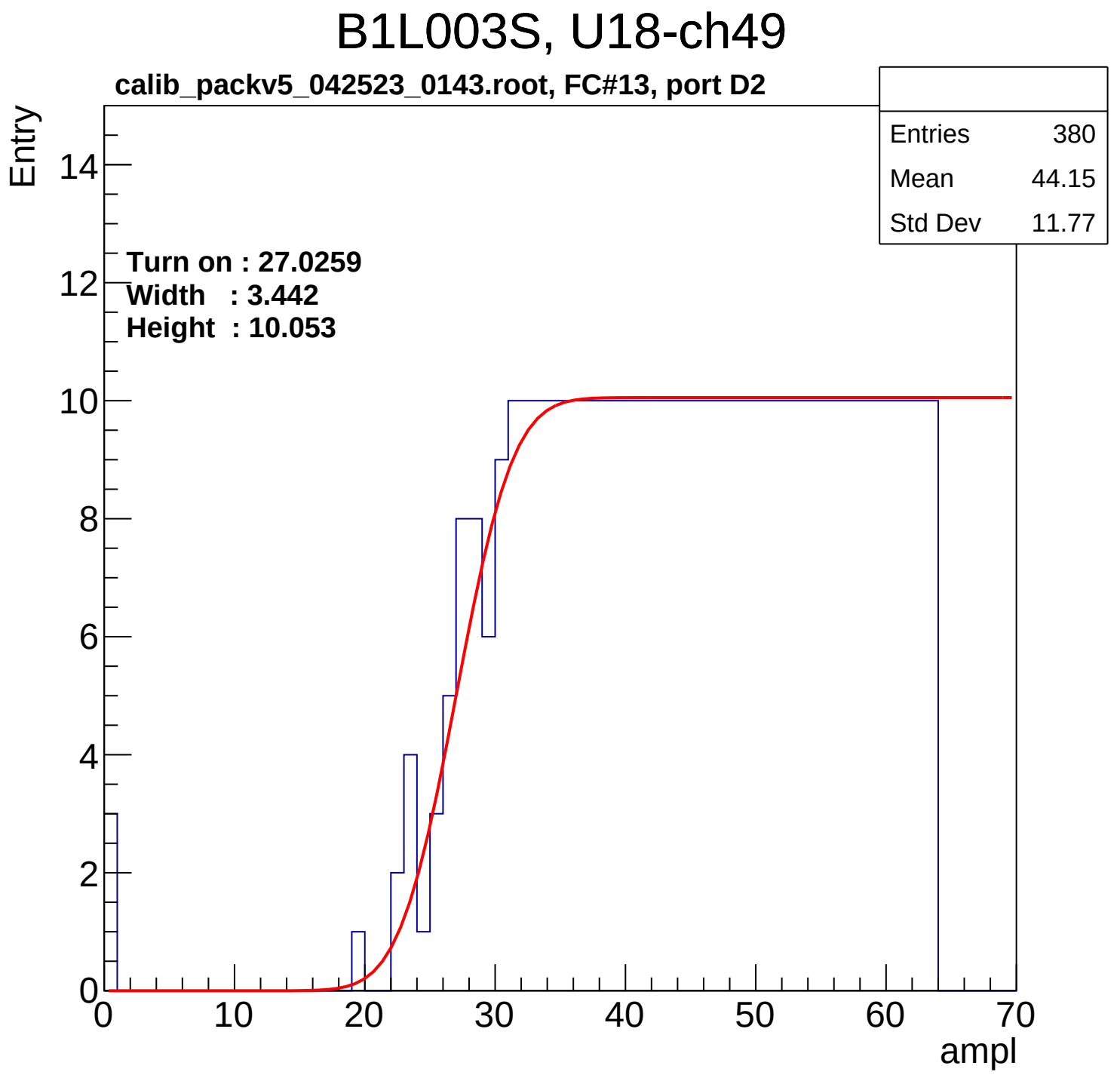
B1L003S, U18-ch49
calib_packv5_042523_0143.root, FC#13, port D2
Entries 380
Mean 44.15
Std Dev 11.77
Turn on : 27.0259
Width : 3.442
Height : 10.053
Entry
ampl
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2
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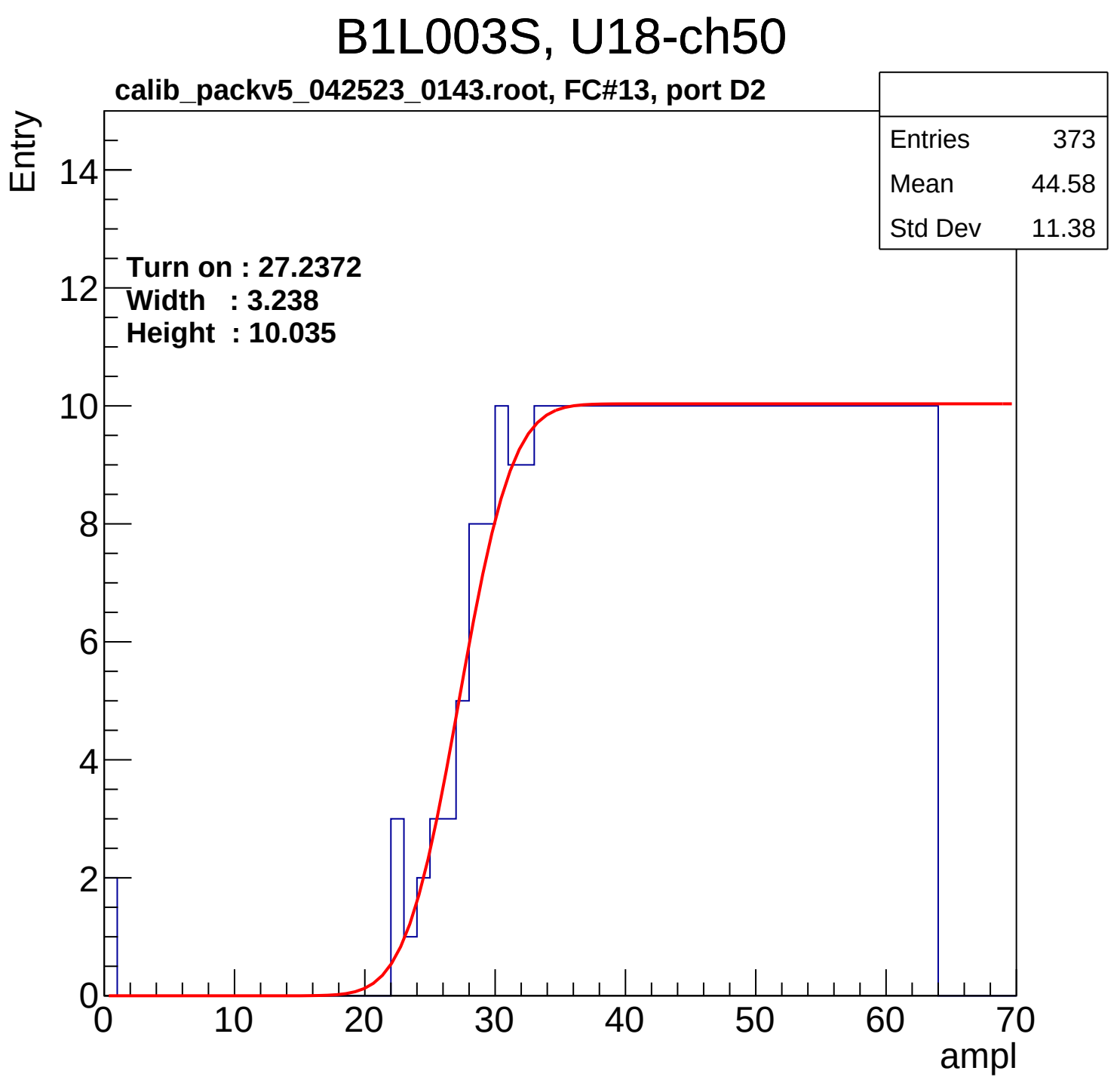
B1L003S, U18-ch50
calib_packv5_042523_0143.root, FC#13, port D2
Entries 373
Mean 44.58
Std Dev 11.38
Turn on : 27.2372
Width : 3.238
Height : 10.035
Entry
ampl
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6
8
10
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0
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60
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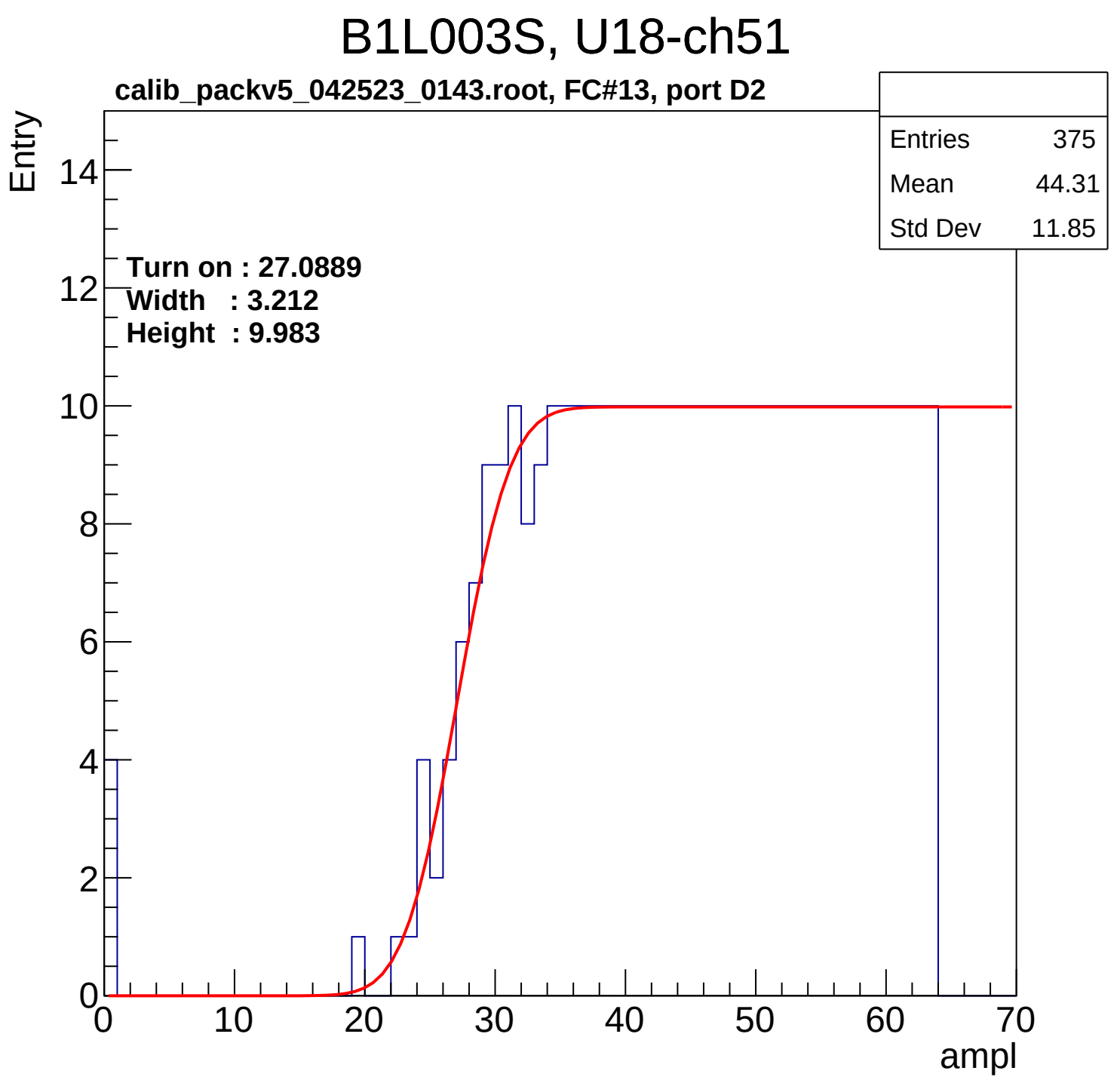
B1L003S, U18-ch51
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.31
Std Dev 11.85
Turn on : 27.0889
Width : 3.212
Height : 9.983
Entry
ampl
0
2
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6
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60
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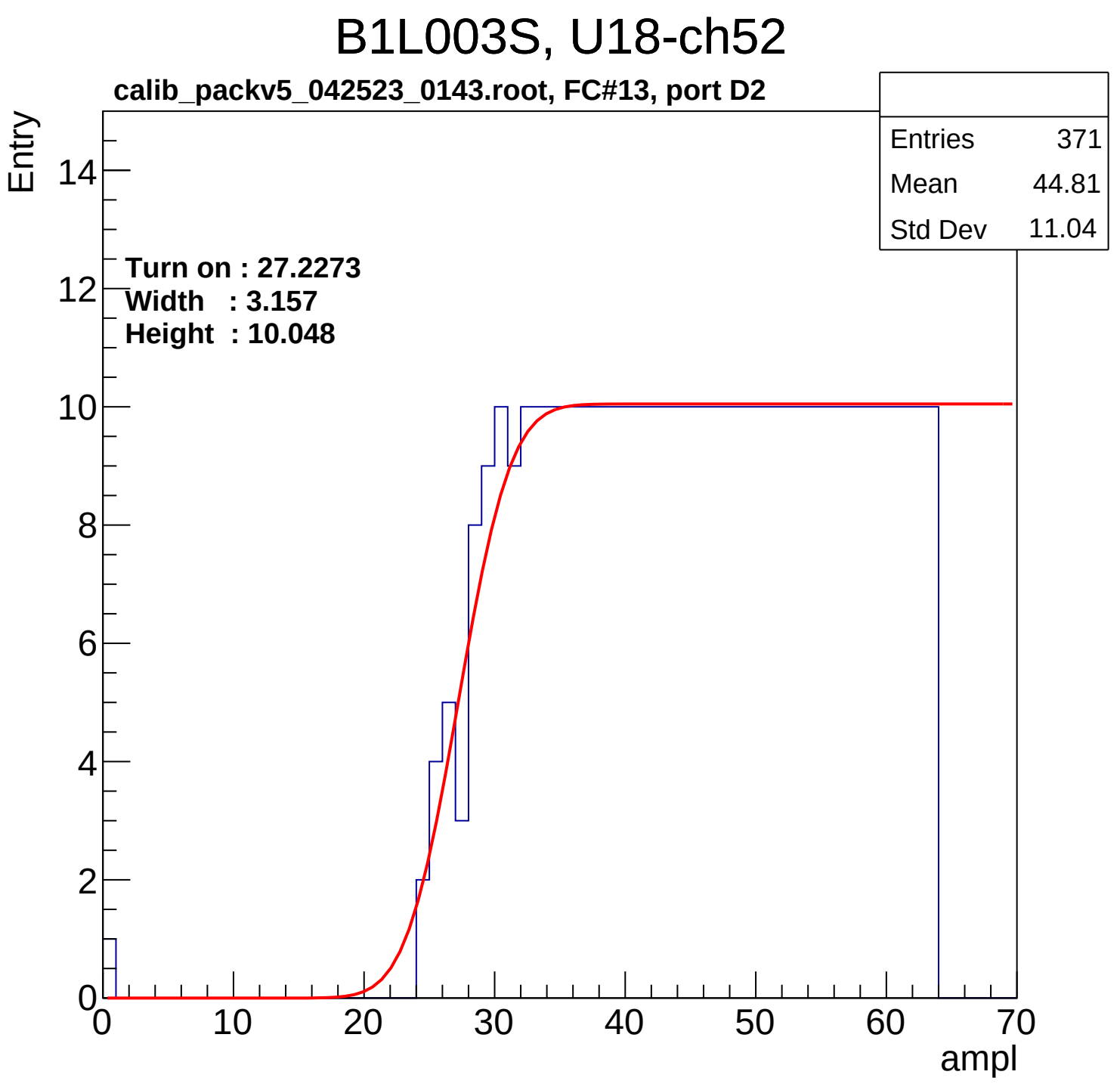
B1L003S, U18-ch52
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.81
Std Dev 11.04
Turn on : 27.2273
Width : 3.157
Height : 10.048
Entry
ampl
0
2
4
6
8
10
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0
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60
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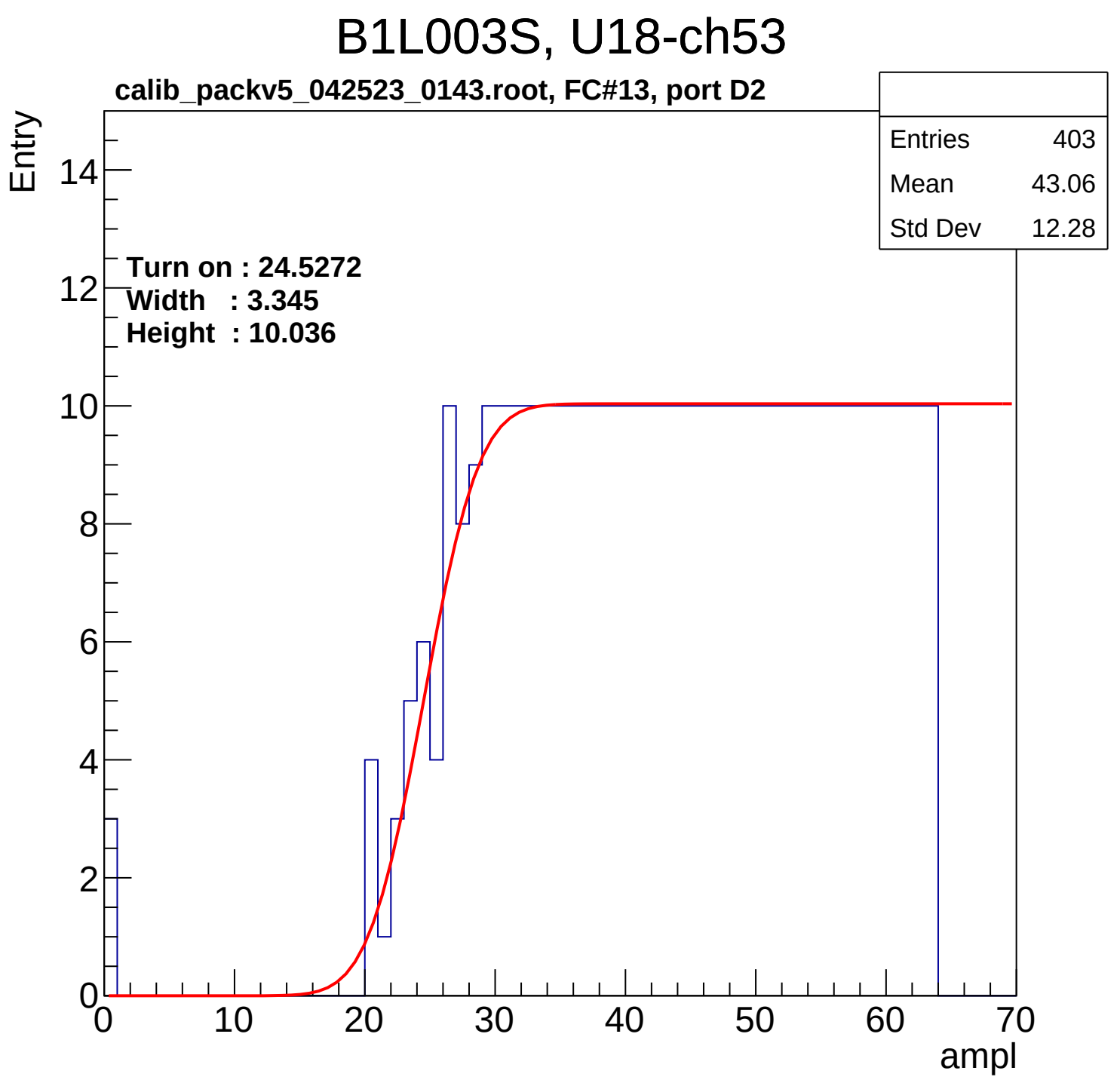
B1L003S, U18-ch53
calib_packv5_042523_0143.root, FC#13, port D2
Entries 403
Mean 43.06
Std Dev 12.28
Turn on : 24.5272
Width : 3.345
Height : 10.036
Entry
ampl
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2
4
6
8
10
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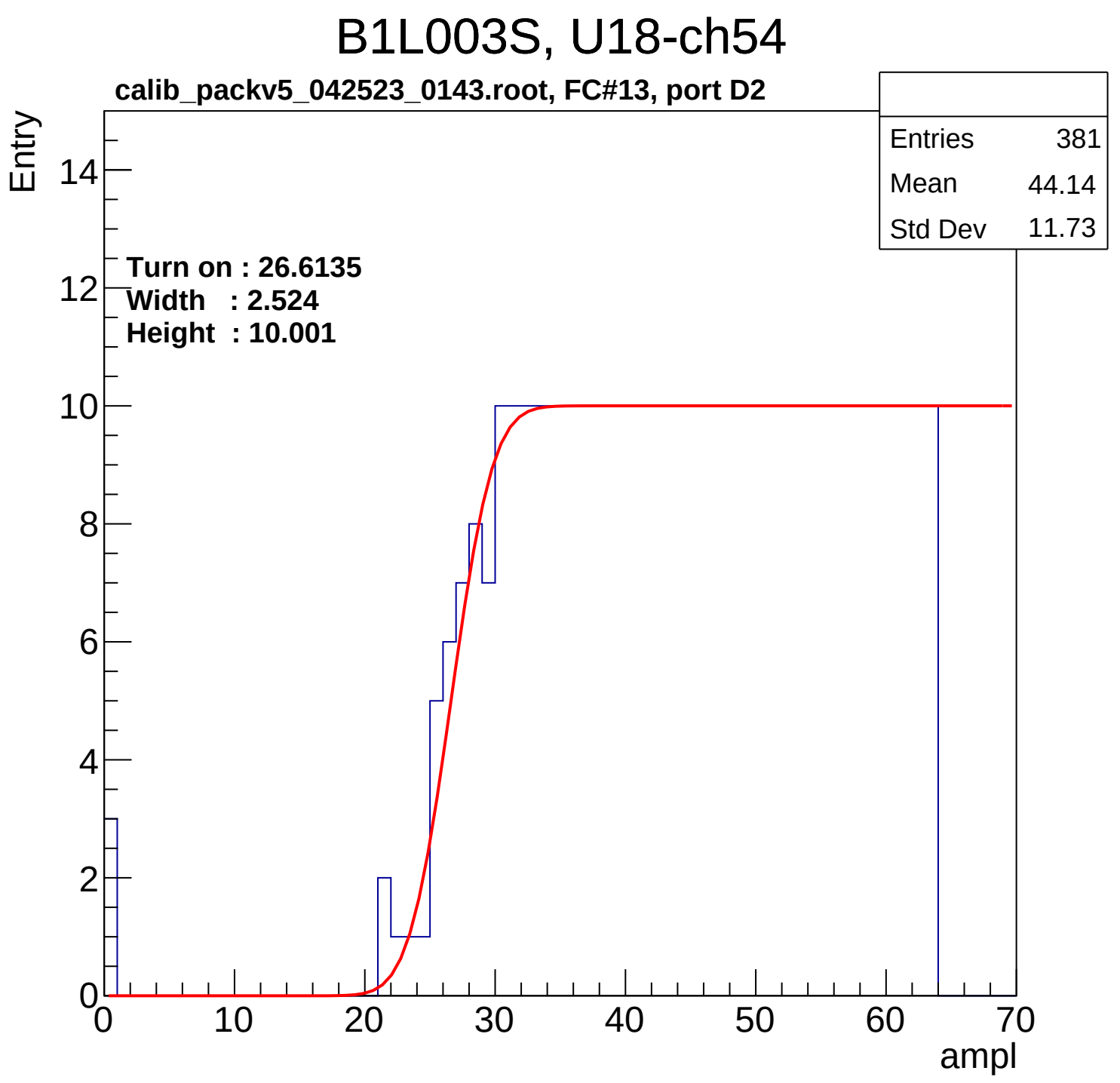
B1L003S, U18-ch54
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 44.14
Std Dev 11.73
Turn on : 26.6135
Width : 2.524
Height : 10.001
Entry
ampl
0
2
4
6
8
10
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0
10
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60
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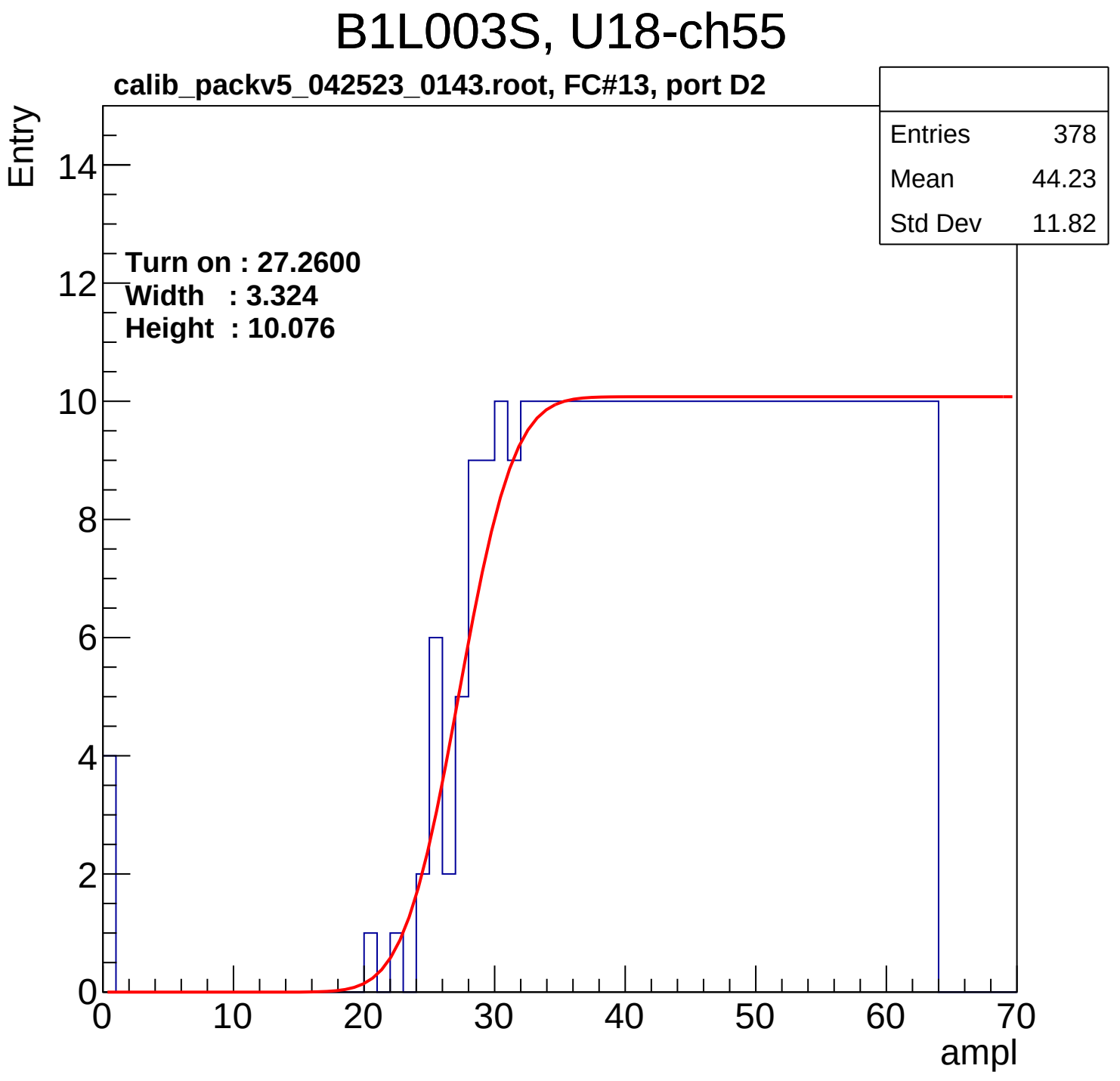
B1L003S, U18-ch55
calib_packv5_042523_0143.root, FC#13, port D2
Entries 378
Mean 44.23
Std Dev 11.82
Turn on : 27.2600
Width : 3.324
Height : 10.076
Entry
ampl
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2
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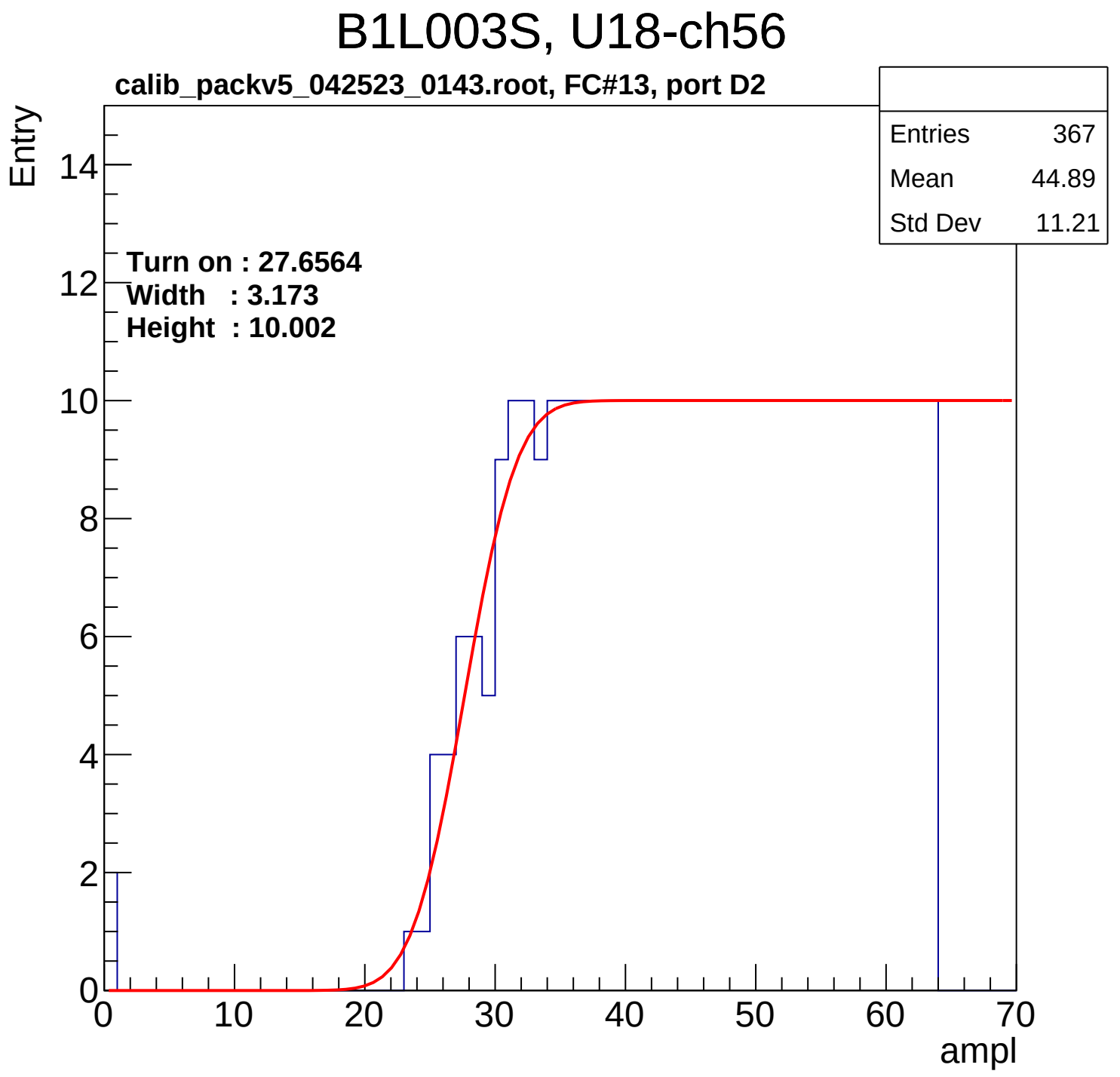
B1L003S, U18-ch56
calib_packv5_042523_0143.root, FC#13, port D2
Entries 367
Mean 44.89
Std Dev 11.21
Turn on : 27.6564
Width : 3.173
Height : 10.002
Entry
ampl
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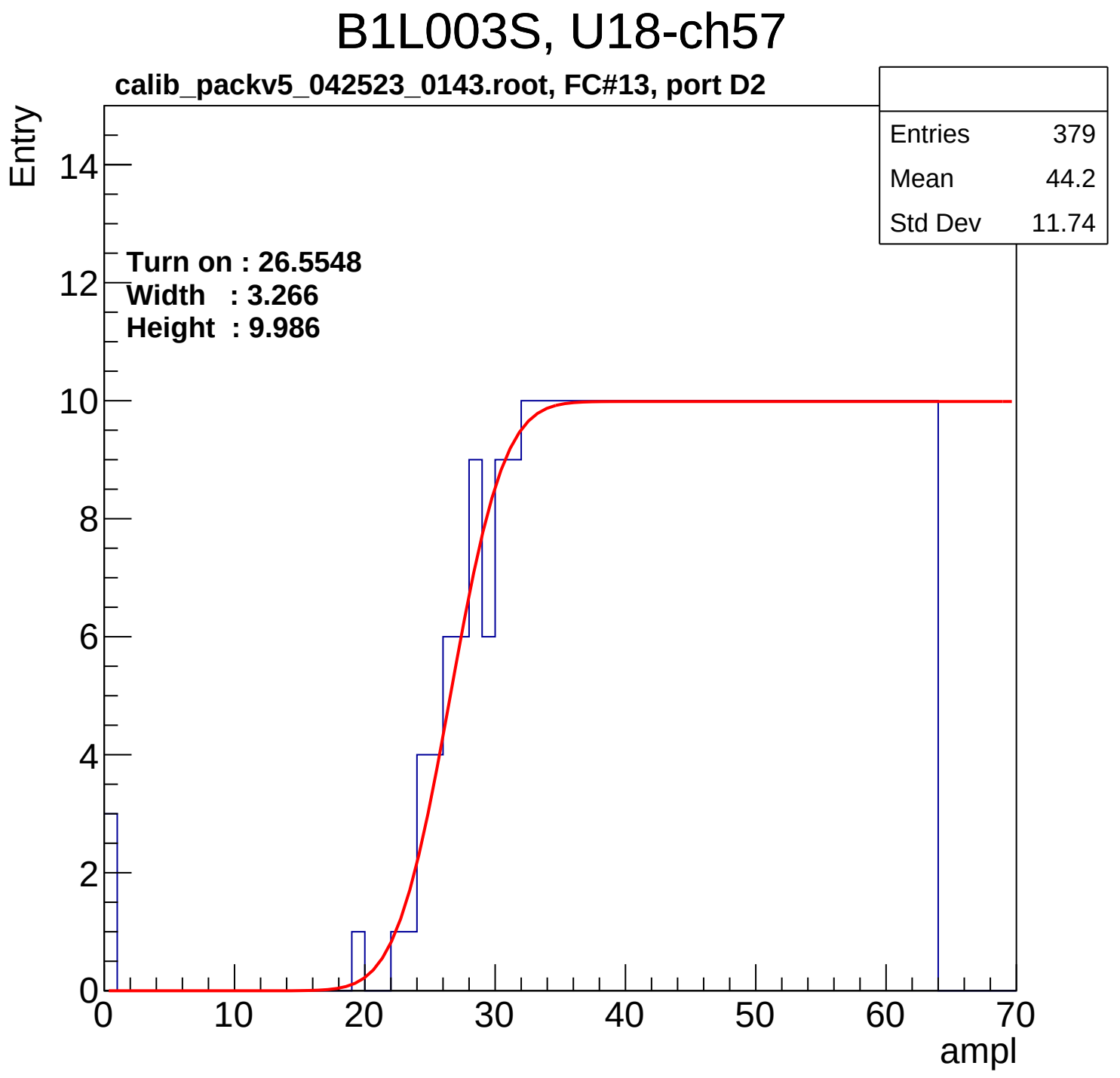
B1L003S, U18-ch57
calib_packv5_042523_0143.root, FC#13, port D2
Entries 379
Mean 44.2
Std Dev 11.74
Turn on : 26.5548
Width : 3.266
Height : 9.986
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
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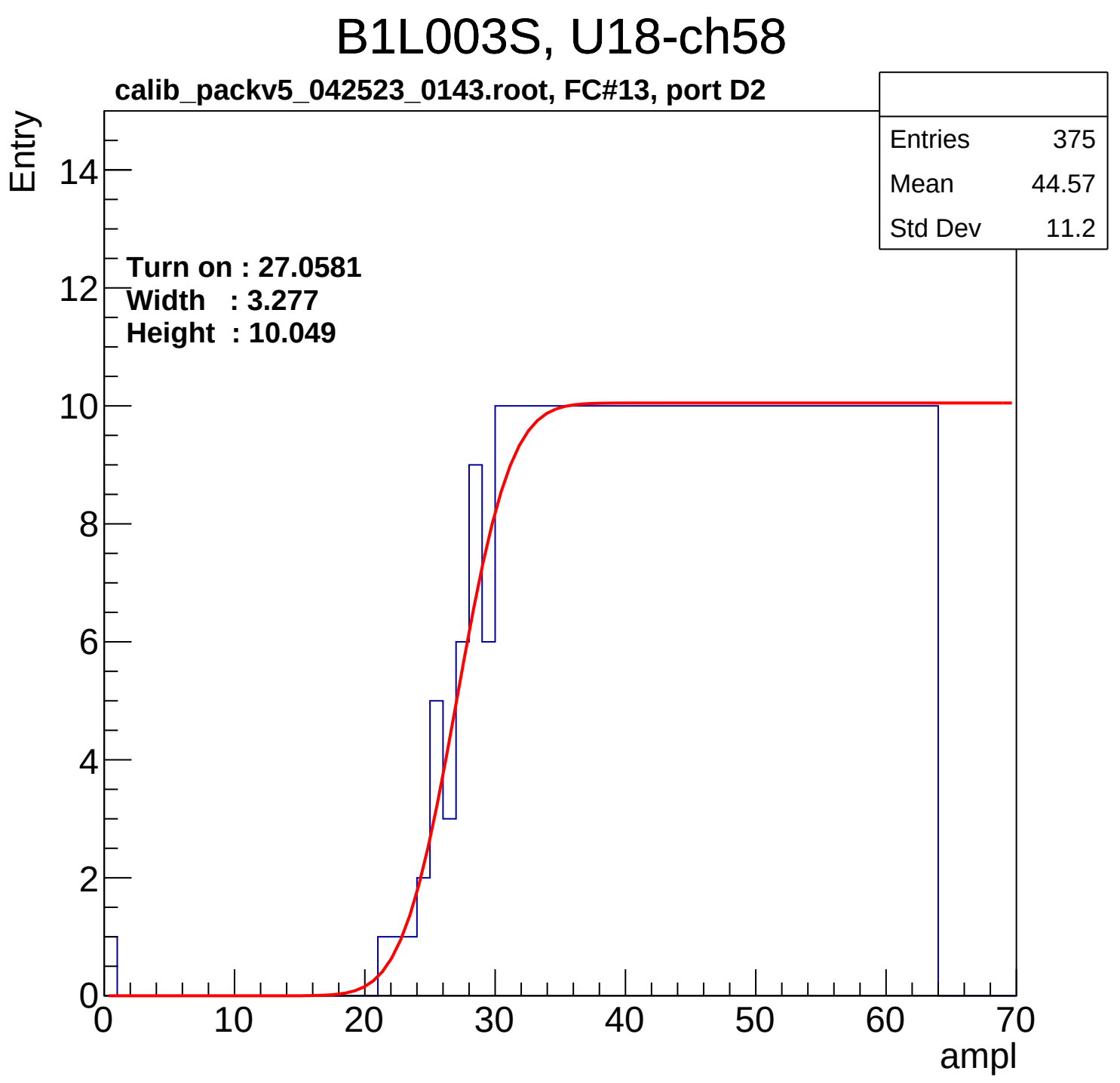
B1L003S, U18-ch58
calib_packv5_042523_0143.root, FC#13, port D2
Entries 375
Mean 44.57
Std Dev 11.2
Turn on : 27.0581
Width : 3.277
Height : 10.049
Entry
ampl
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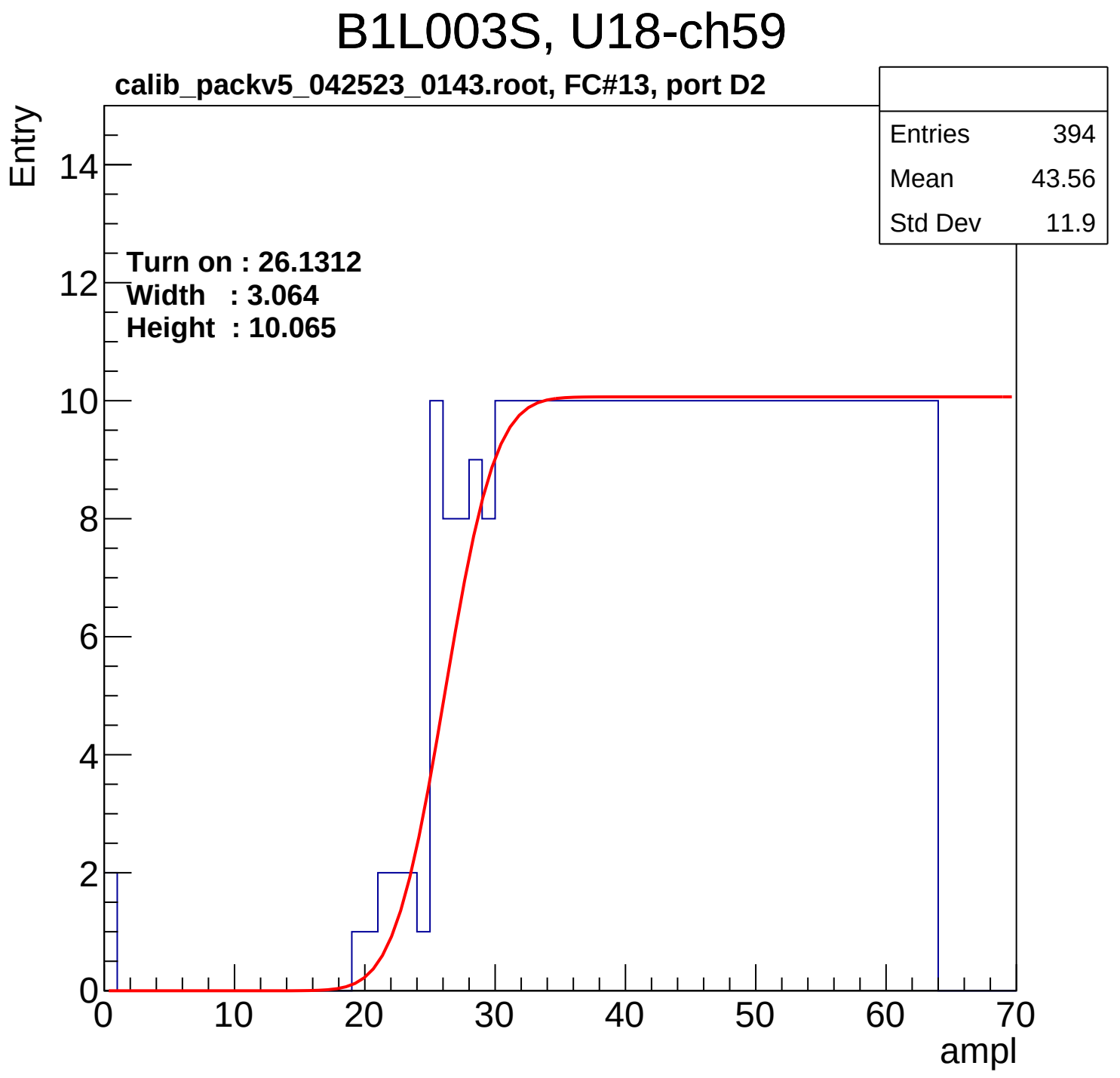
B1L003S, U18-ch59
calib_packv5_042523_0143.root, FC#13, port D2
Entries 394
Mean 43.56
Std Dev 11.9
Turn on : 26.1312
Width : 3.064
Height : 10.065
Entry
ampl
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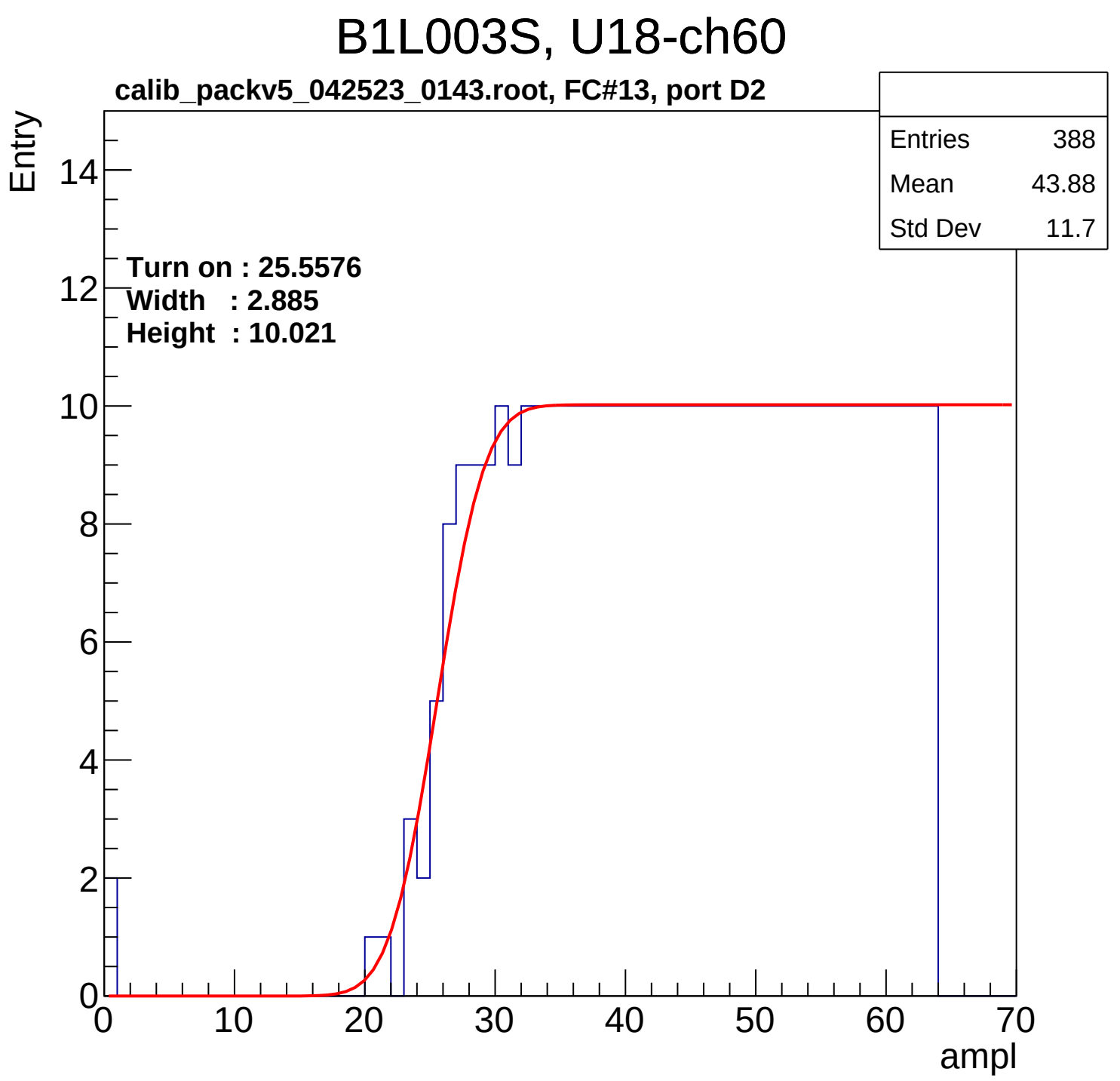
B1L003S, U18-ch60
calib_packv5_042523_0143.root, FC#13, port D2
Entries 388
Mean 43.88
Std Dev 11.7
Turn on : 25.5576
Width : 2.885
Height : 10.021
Entry
ampl
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2
4
6
8
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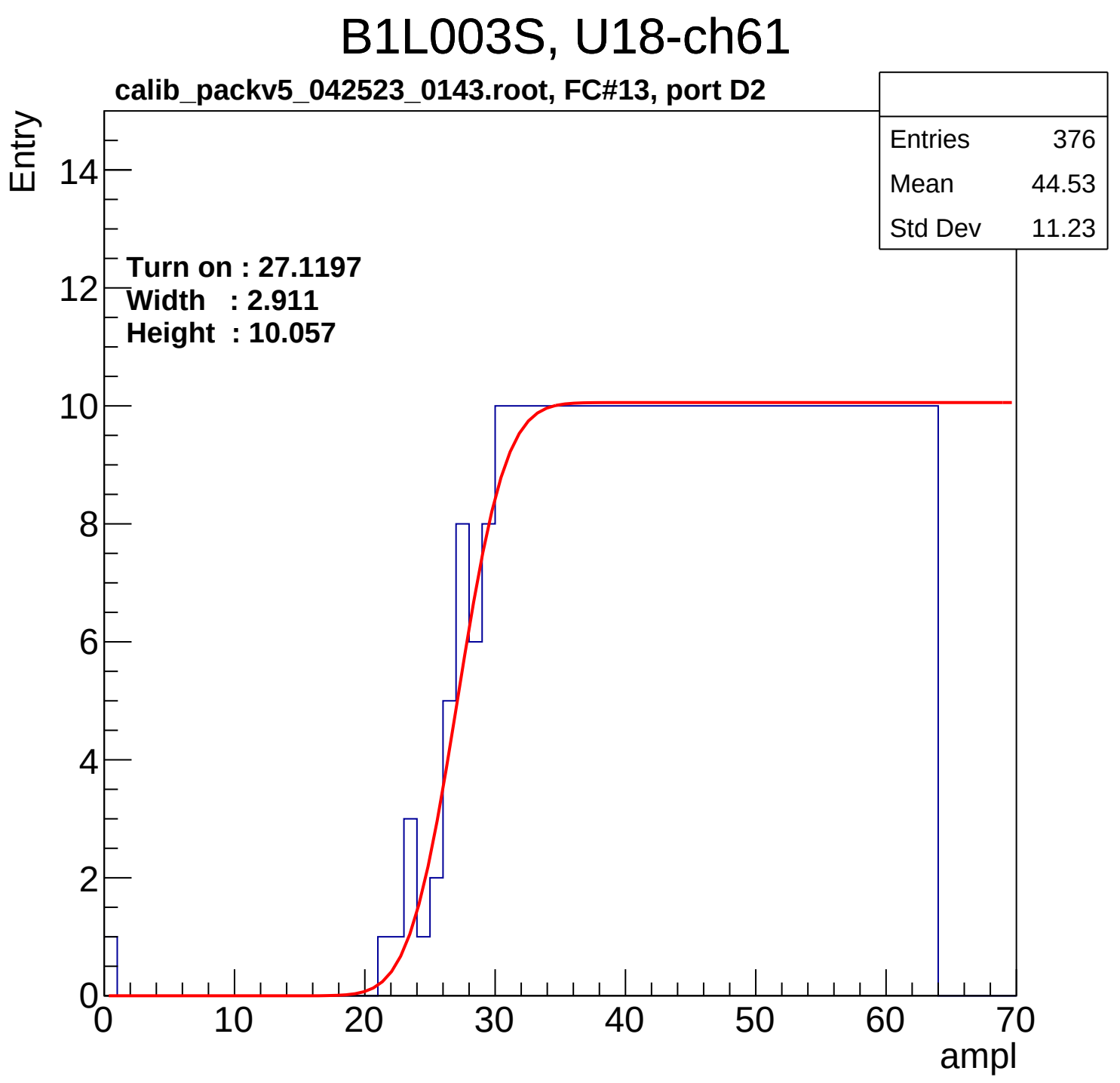
B1L003S, U18-ch61
calib_packv5_042523_0143.root, FC#13, port D2
Entries 376
Mean 44.53
Std Dev 11.23
Turn on : 27.1197
Width : 2.911
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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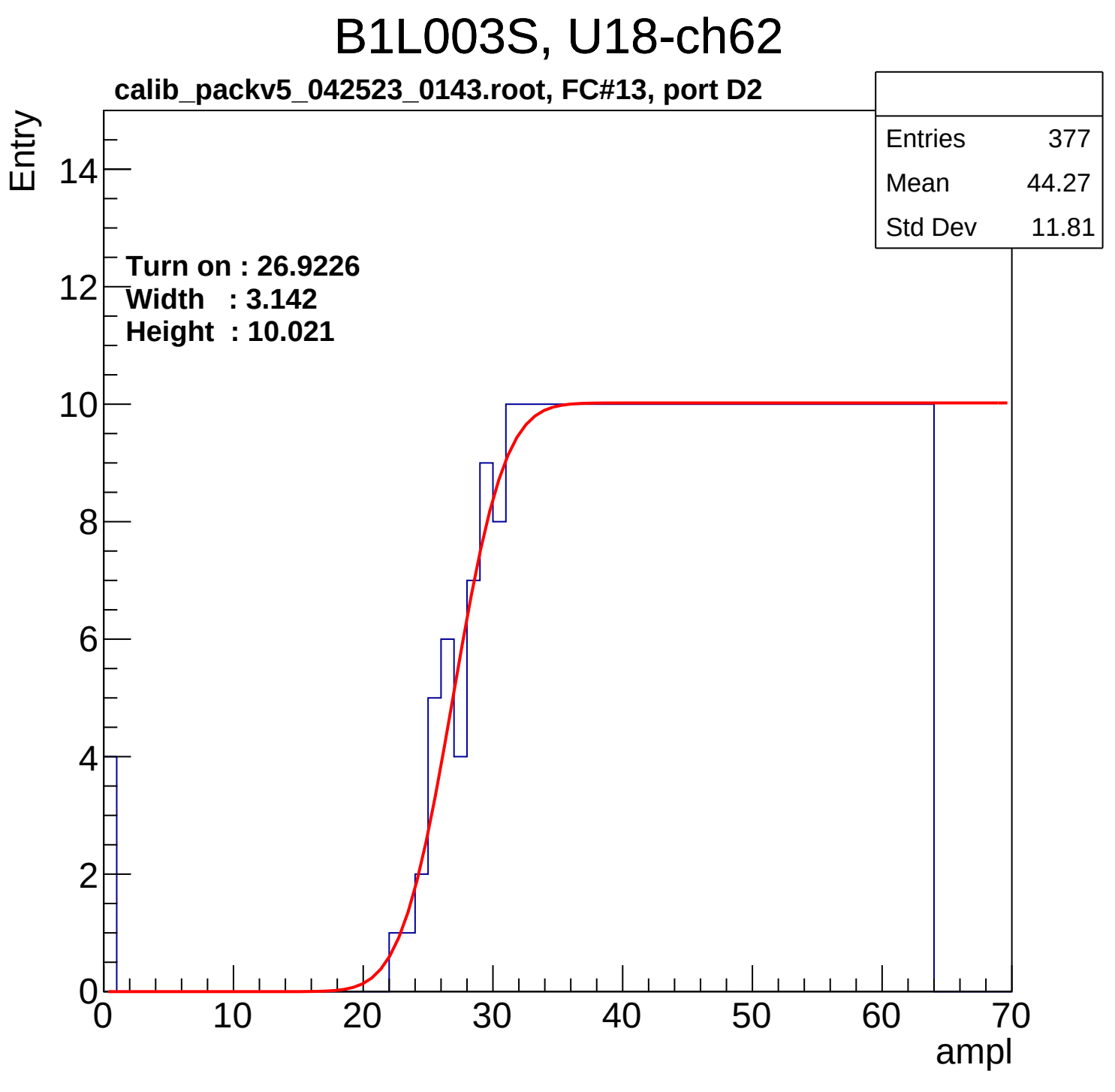
B1L003S, U18-ch62
calib_packv5_042523_0143.root, FC#13, port D2
Entries 377
Mean 44.27
Std Dev 11.81
Turn on : 26.9226
Width : 3.142
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
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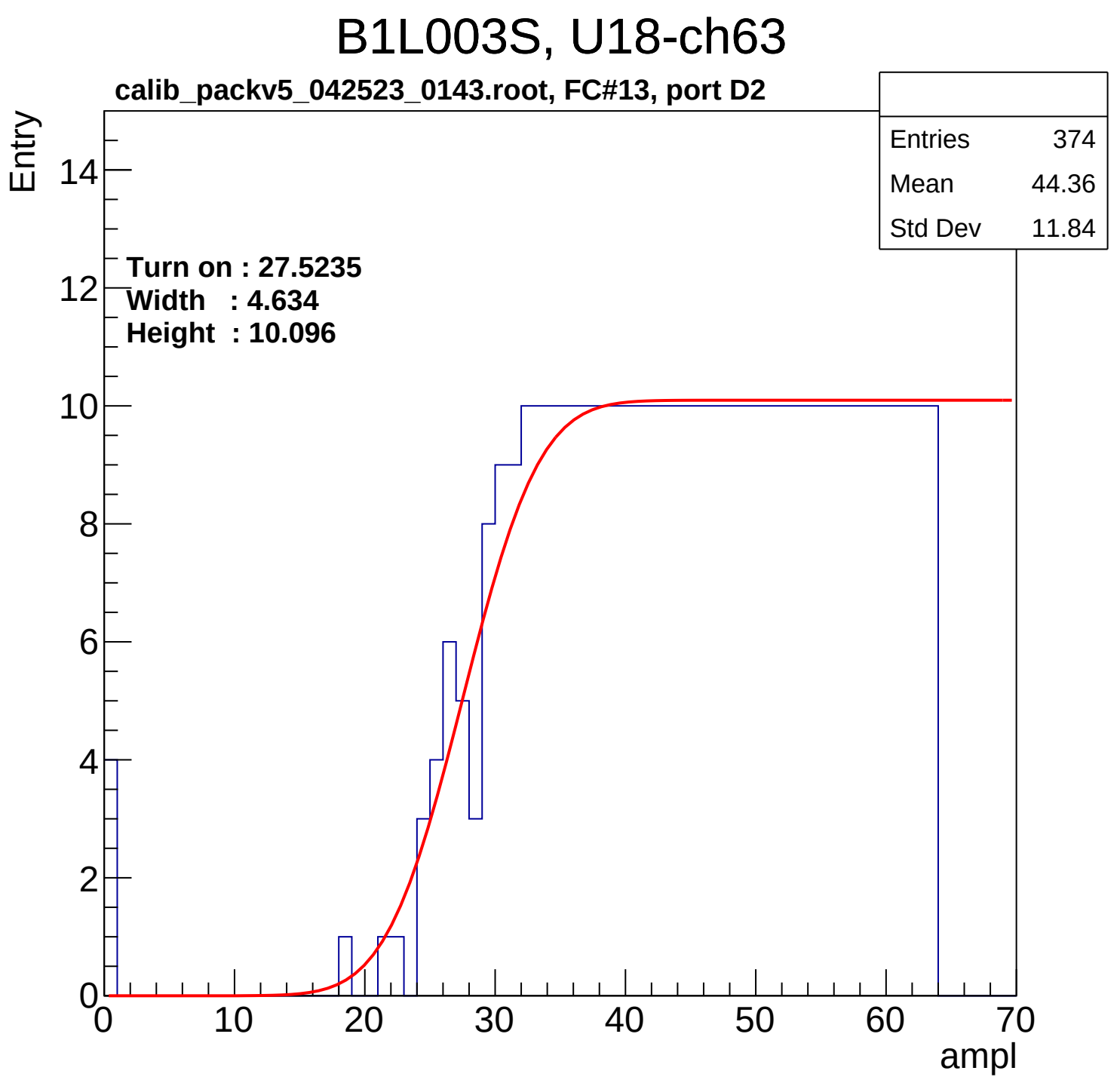
B1L003S, U18-ch63
calib_packv5_042523_0143.root, FC#13, port D2
Entries 374
Mean 44.36
Std Dev 11.84
Turn on : 27.5235
Width : 4.634
Height : 10.096
Entry
ampl
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2
4
6
8
10
12
14
0
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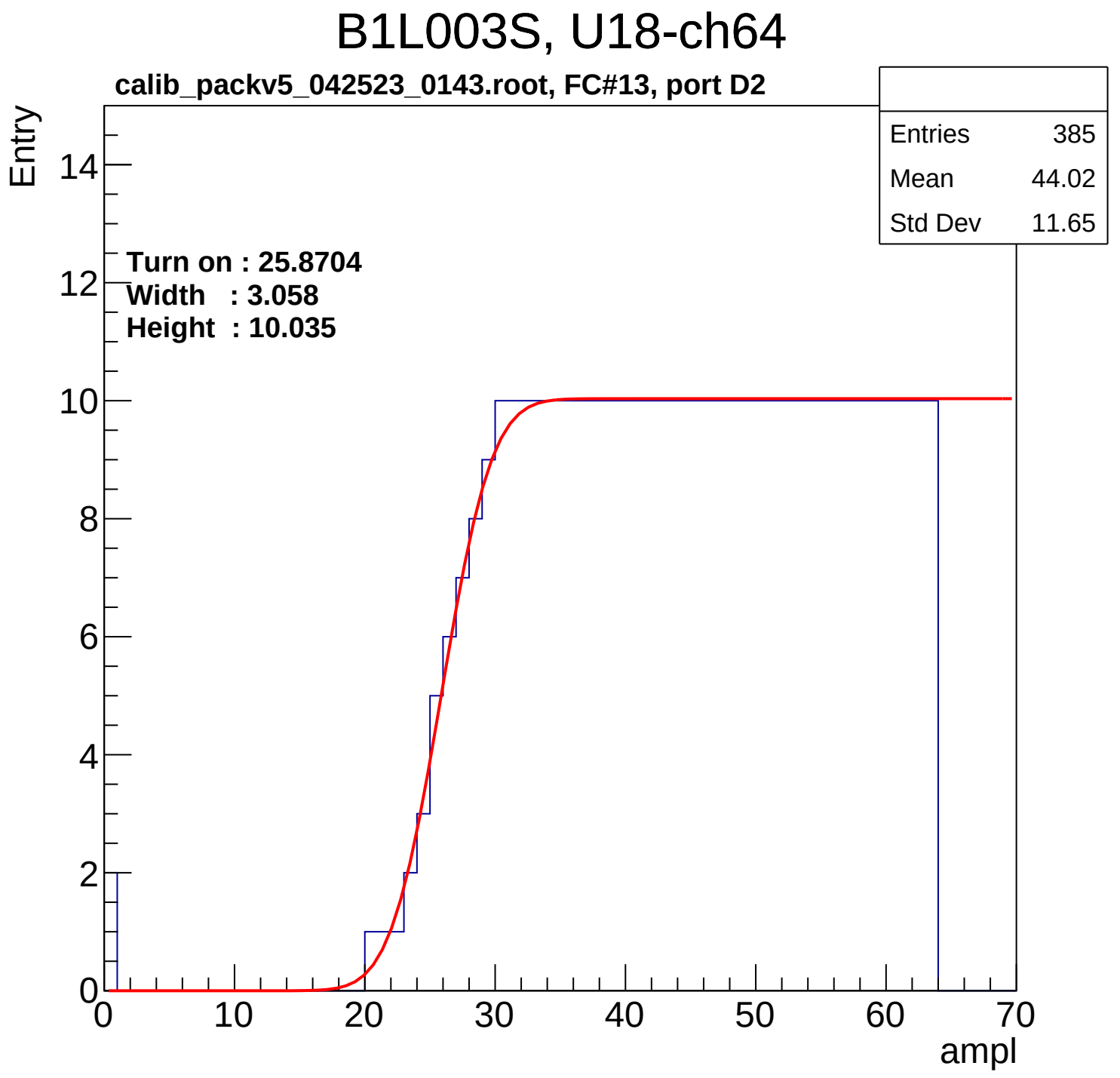
B1L003S, U18-ch64
calib_packv5_042523_0143.root, FC#13, port D2
Entries 385
Mean 44.02
Std Dev 11.65
Turn on : 25.8704
Width : 3.058
Height : 10.035
Entry
ampl
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8
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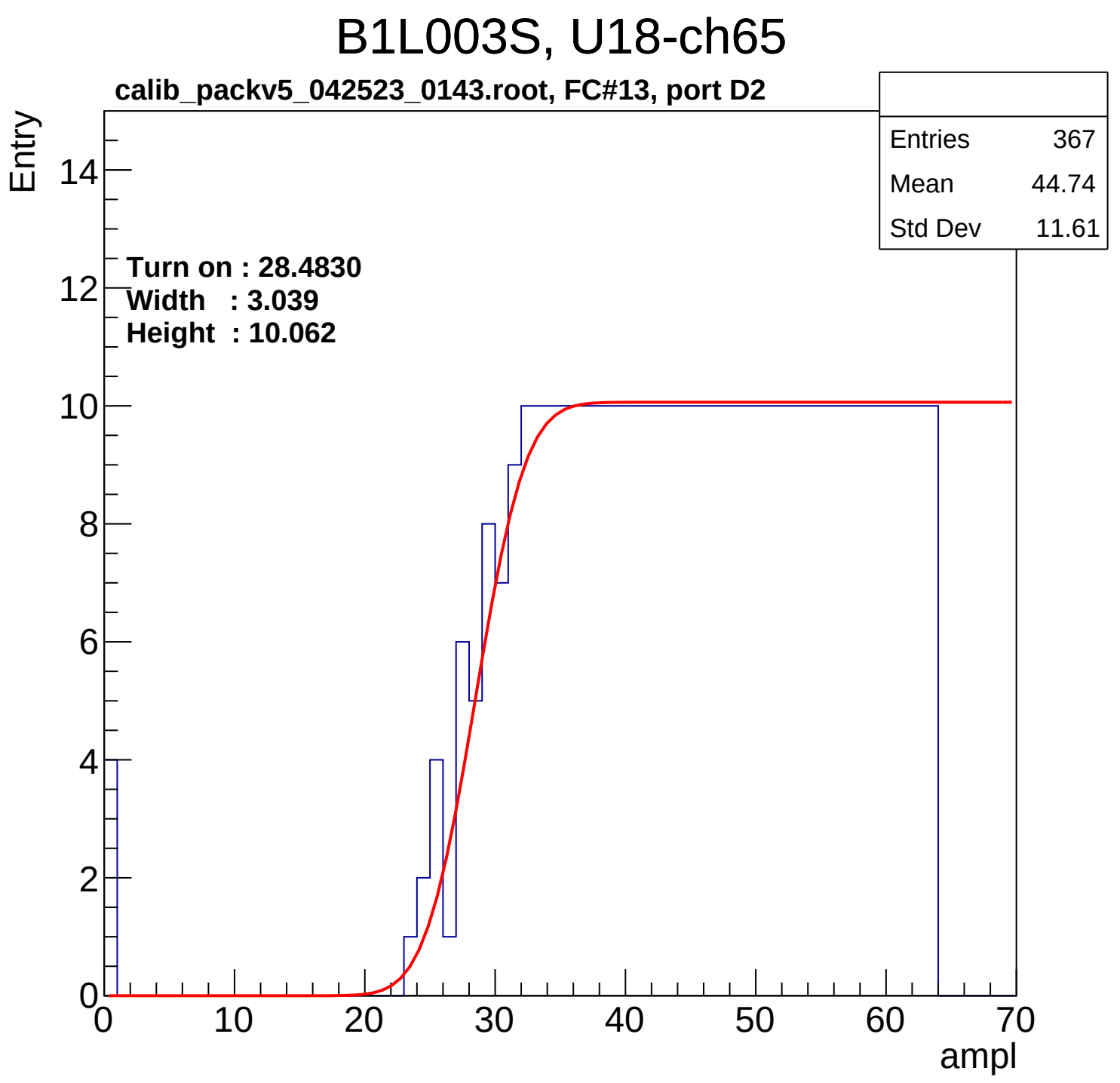
B1L003S, U18-ch65
calib_packv5_042523_0143.root, FC#13, port D2
Entries 367
Mean 44.74
Std Dev 11.61
Turn on : 28.4830
Width : 3.039
Height : 10.062
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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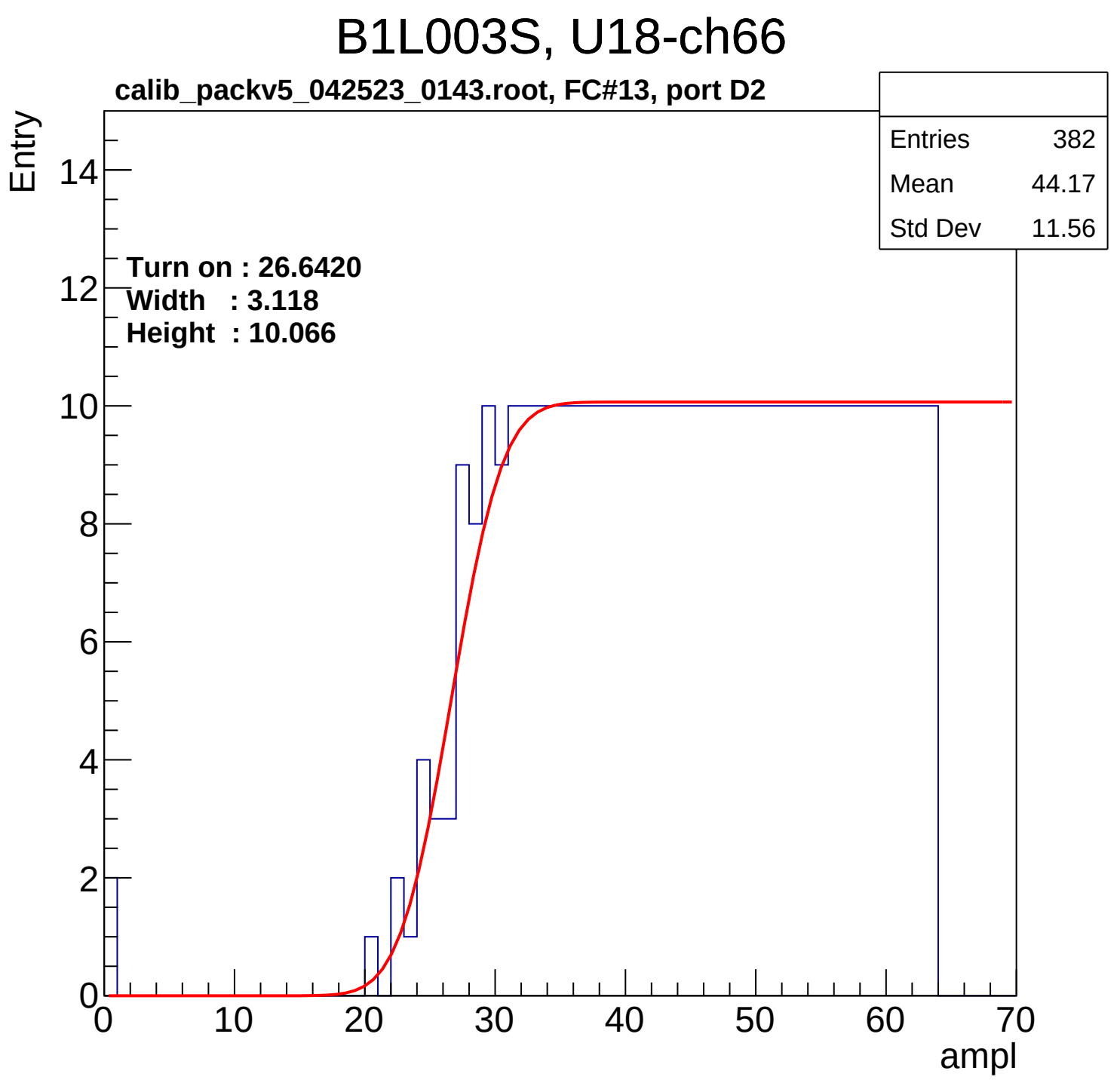
B1L003S, U18-ch66
calib_packv5_042523_0143.root, FC#13, port D2
Entries 382
Mean 44.17
Std Dev 11.56
Turn on : 26.6420
Width : 3.118
Height : 10.066
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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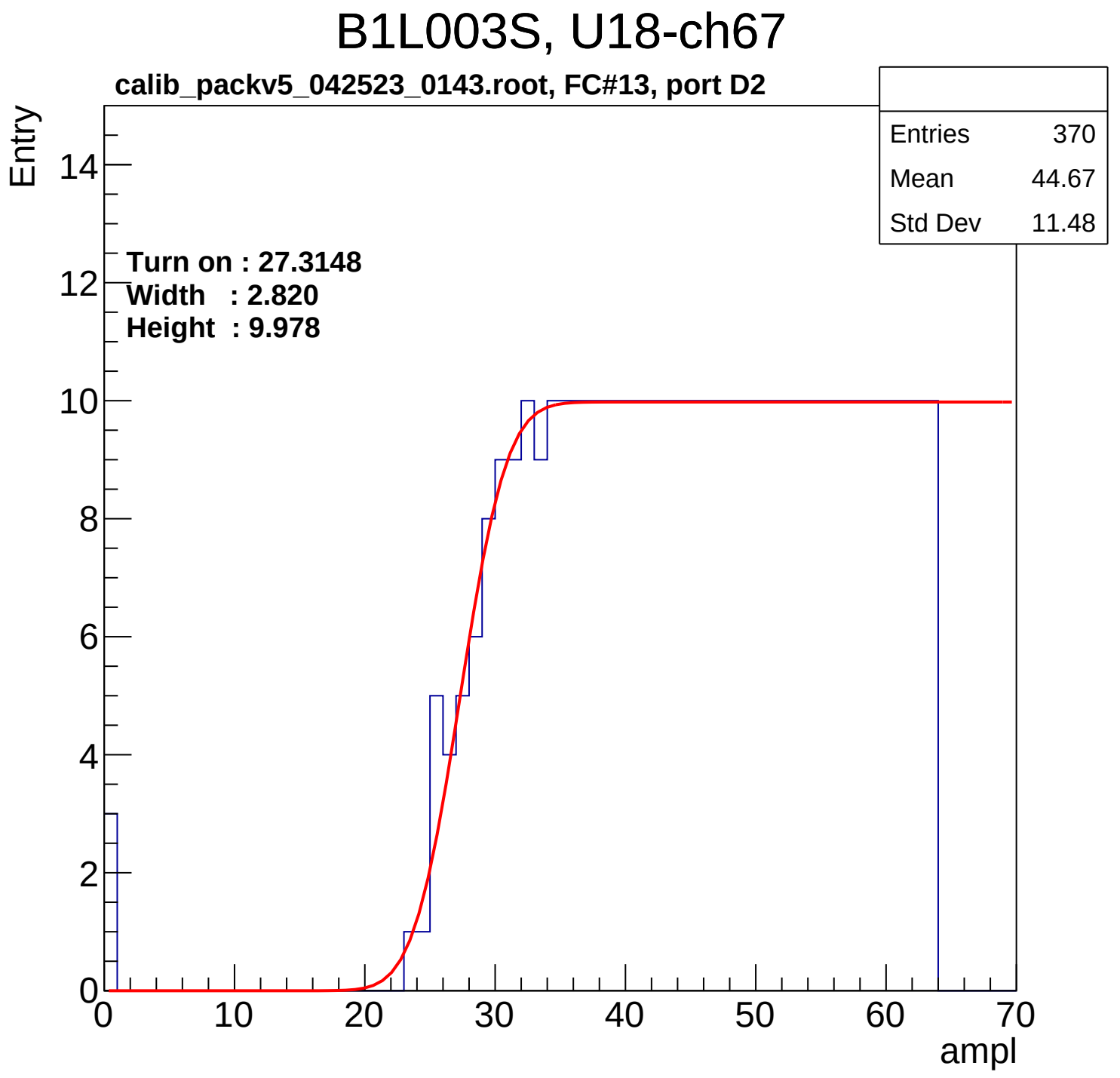
B1L003S, U18-ch67
calib_packv5_042523_0143.root, FC#13, port D2
Entries 370
Mean 44.67
Std Dev 11.48
Turn on : 27.3148
Width : 2.820
Height : 9.978
Entry
ampl
0
2
4
6
8
10
12
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0
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20
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60
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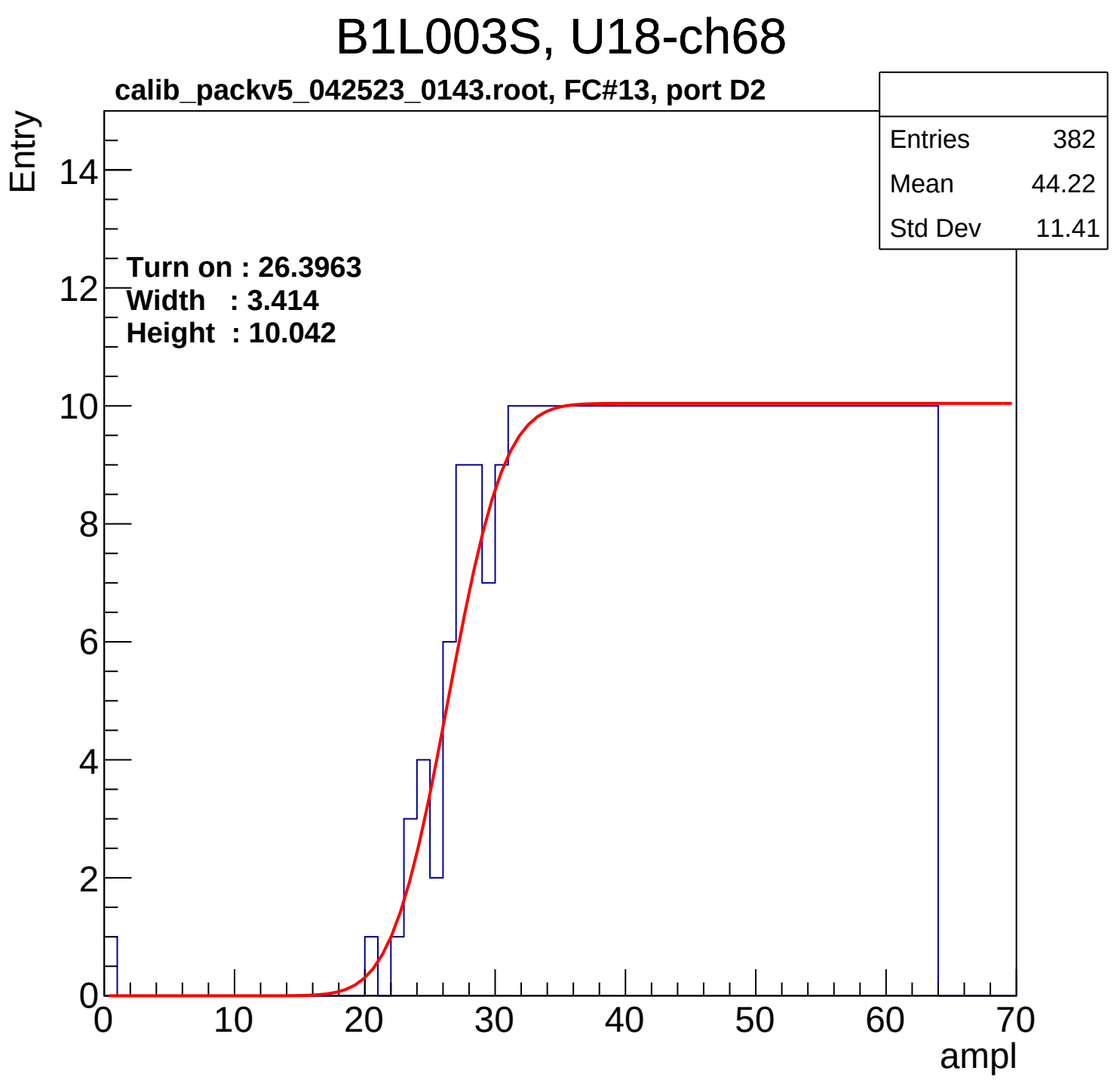
B1L003S, U18-ch68
calib_packv5_042523_0143.root, FC#13, port D2
Entries 382
Mean 44.22
Std Dev 11.41
Turn on : 26.3963
Width : 3.414
Height : 10.042
Entry
ampl
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6
8
10
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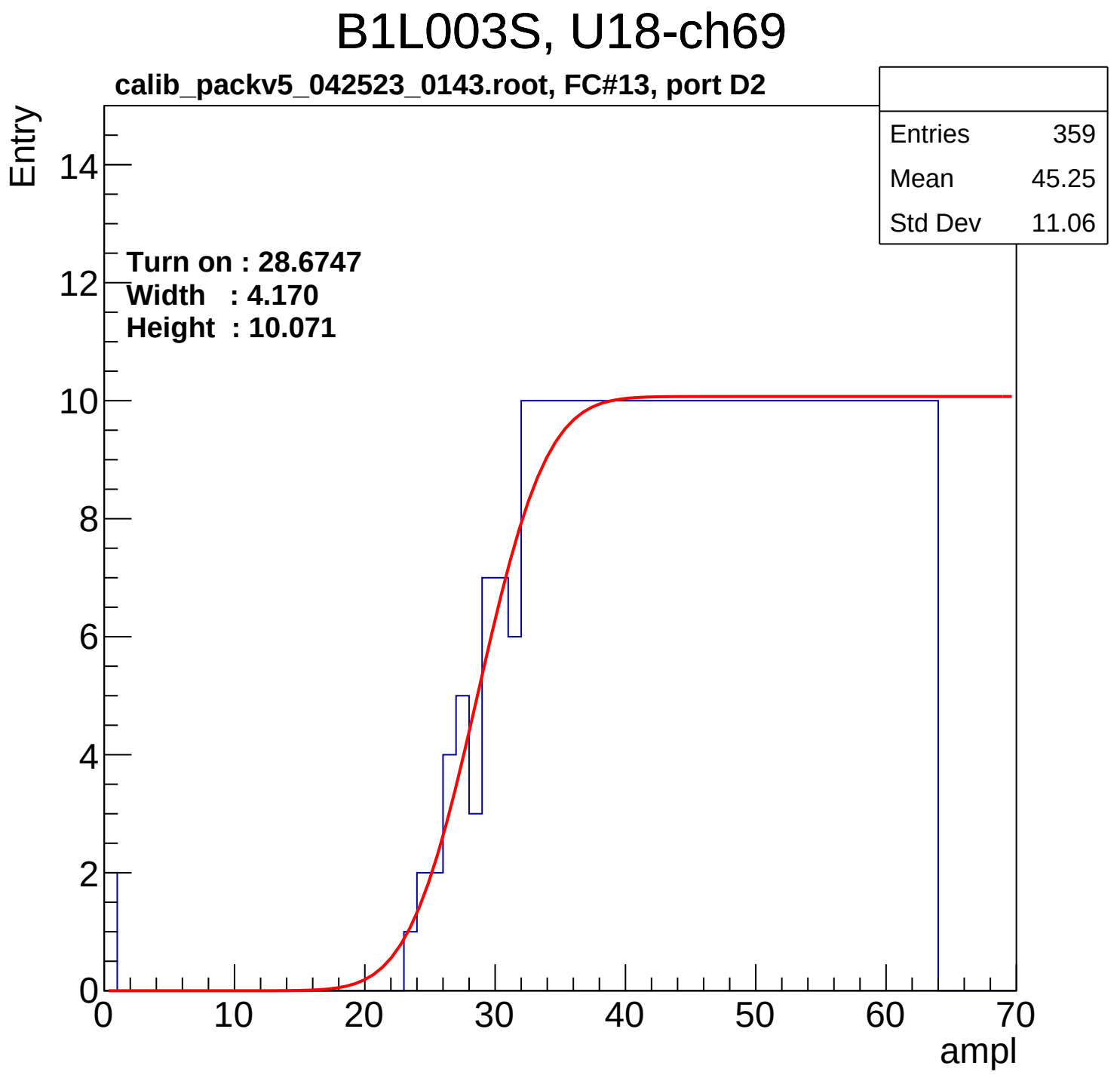
B1L003S, U18-ch69
calib_packv5_042523_0143.root, FC#13, port D2
Entries 359
Mean 45.25
Std Dev 11.06
Turn on : 28.6747
Width : 4.170
Height : 10.071
Entry
ampl
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8
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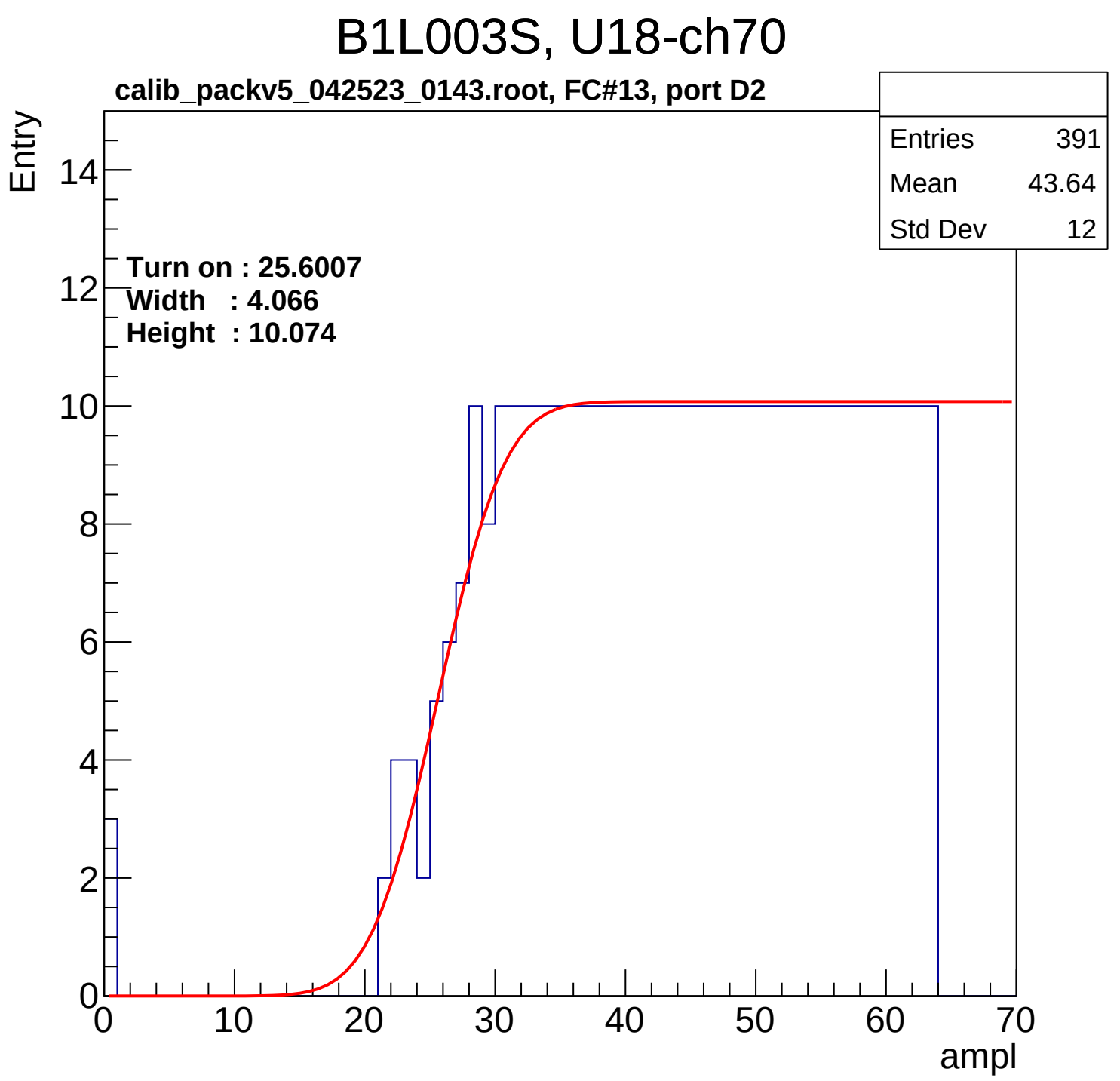
B1L003S, U18-ch70
calib_packv5_042523_0143.root, FC#13, port D2
Entries 391
Mean 43.64
Std Dev 12
Turn on : 25.6007
Width : 4.066
Height : 10.074
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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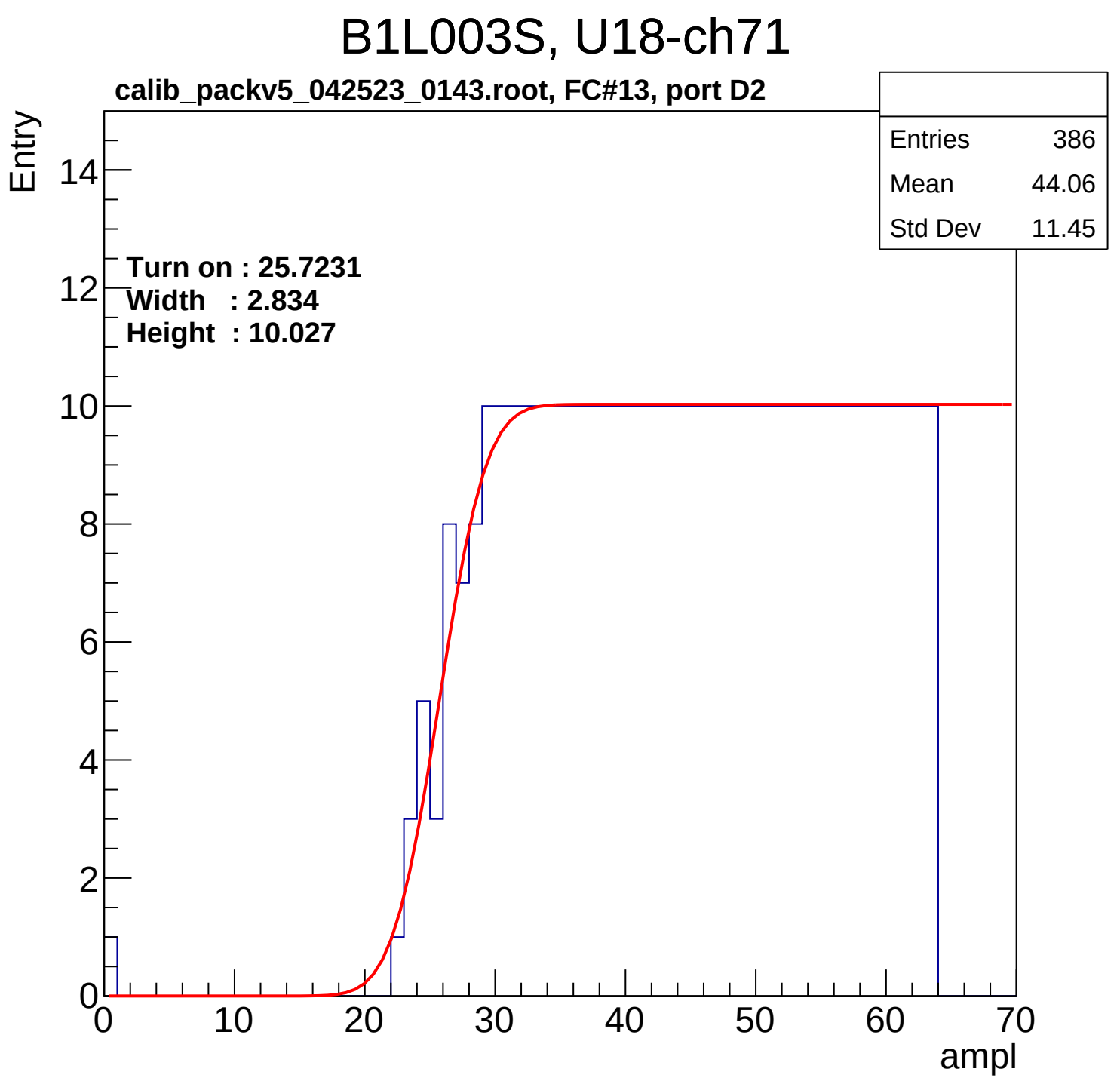
B1L003S, U18-ch71
calib_packv5_042523_0143.root, FC#13, port D2
Entries 386
Mean 44.06
Std Dev 11.45
Turn on : 25.7231
Width : 2.834
Height : 10.027
Entry
ampl
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2
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6
8
10
12
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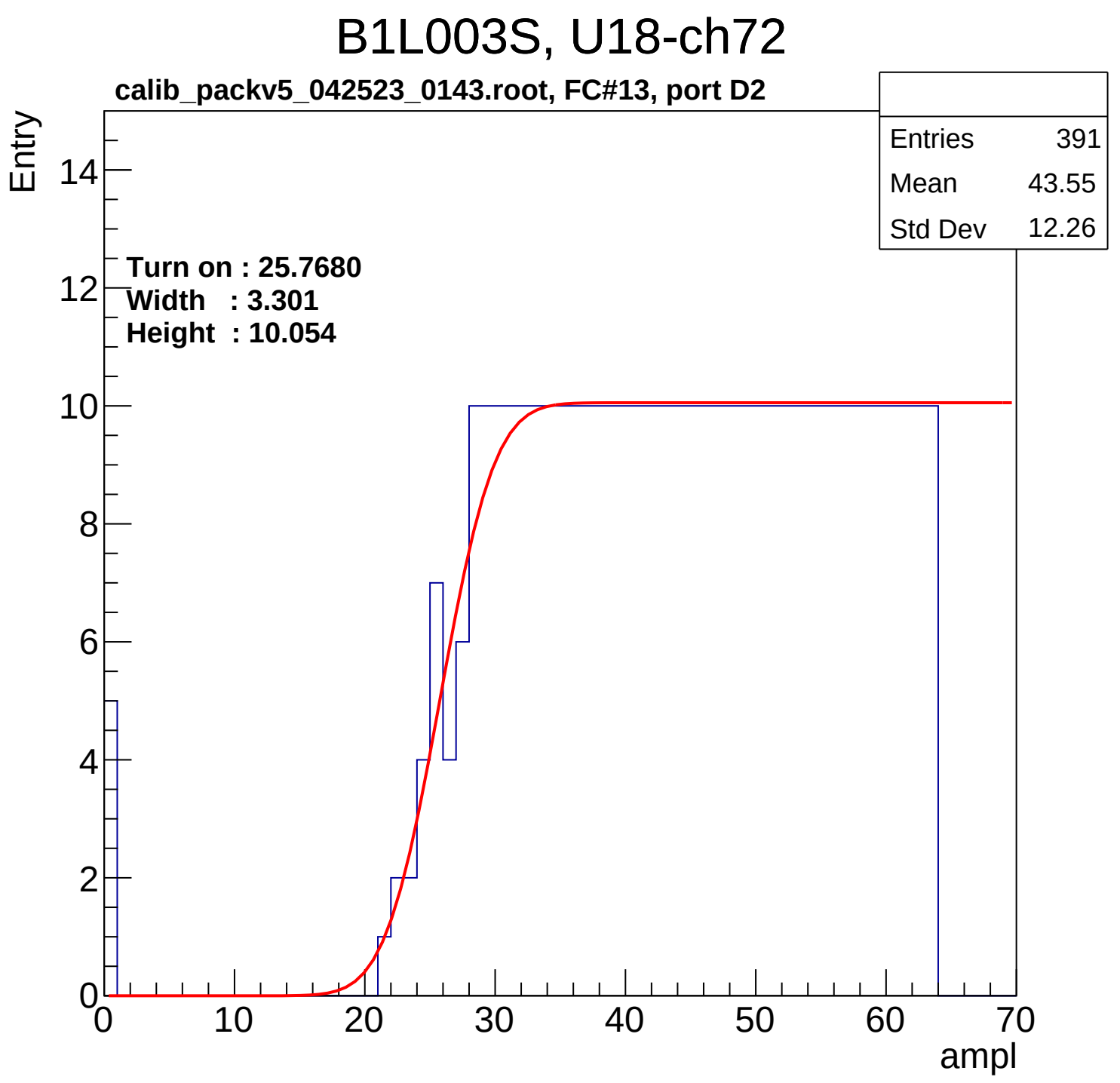
B1L003S, U18-ch72
calib_packv5_042523_0143.root, FC#13, port D2
Entries 391
Mean 43.55
Std Dev 12.26
Turn on : 25.7680
Width : 3.301
Height : 10.054
Entry
ampl
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8
10
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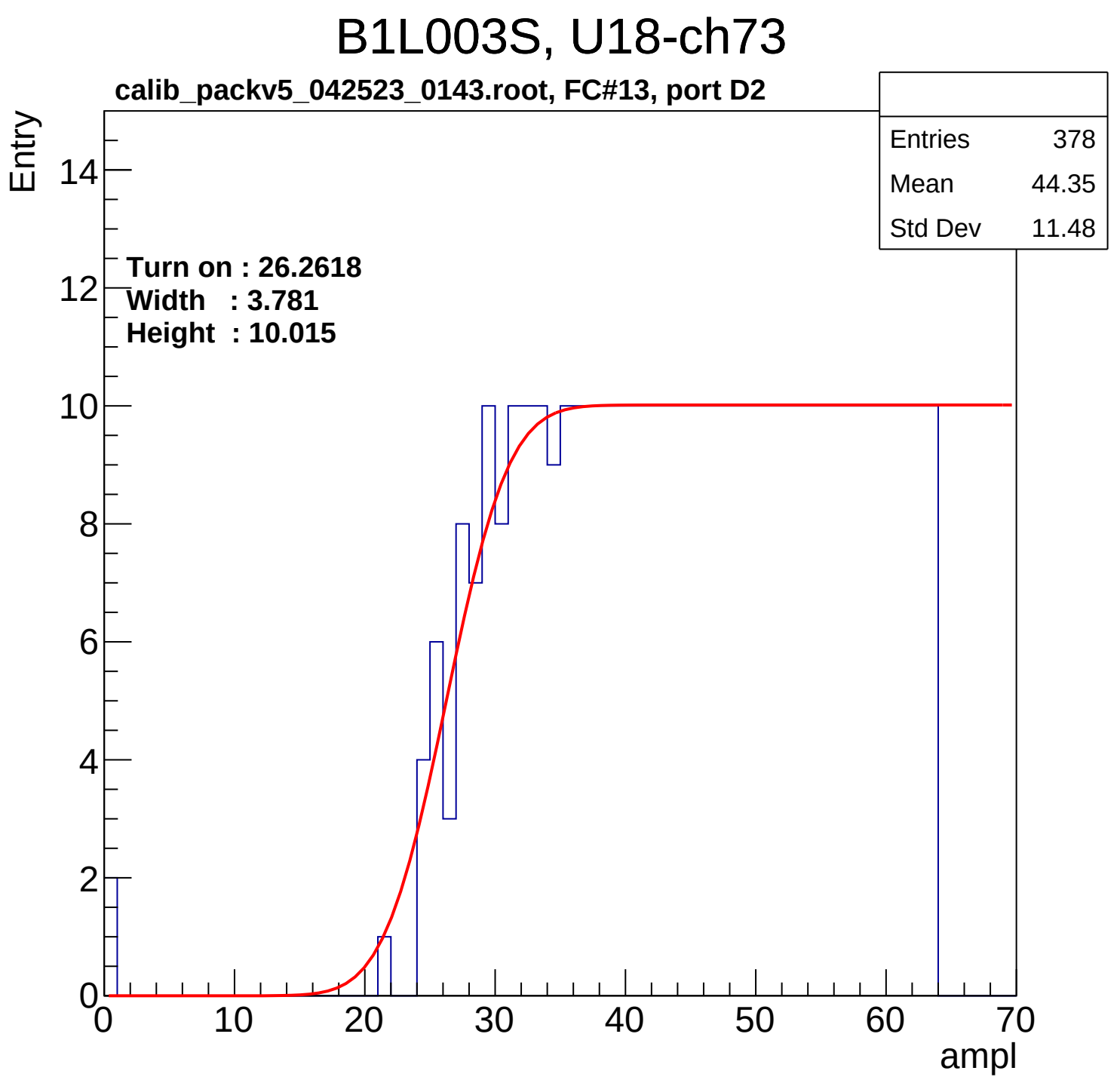
B1L003S, U18-ch73
calib_packv5_042523_0143.root, FC#13, port D2
Entries 378
Mean 44.35
Std Dev 11.48
Turn on : 26.2618
Width : 3.781
Height : 10.015
Entry
ampl
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10
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0
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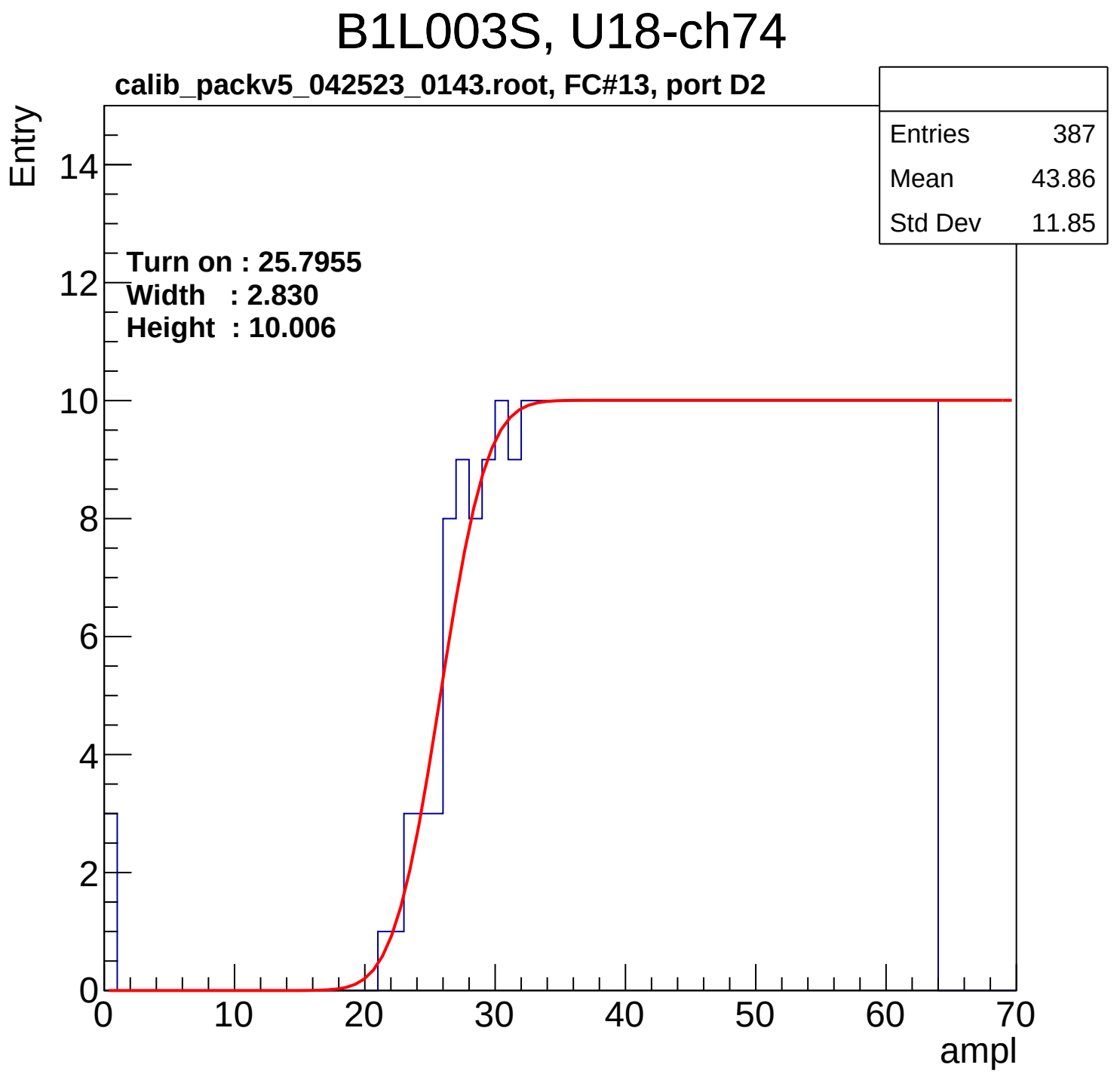
B1L003S, U18-ch74
calib_packv5_042523_0143.root, FC#13, port D2
Entries 387
Mean 43.86
Std Dev 11.85
Turn on : 25.7955
Width : 2.830
Height : 10.006
Entry
ampl
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8
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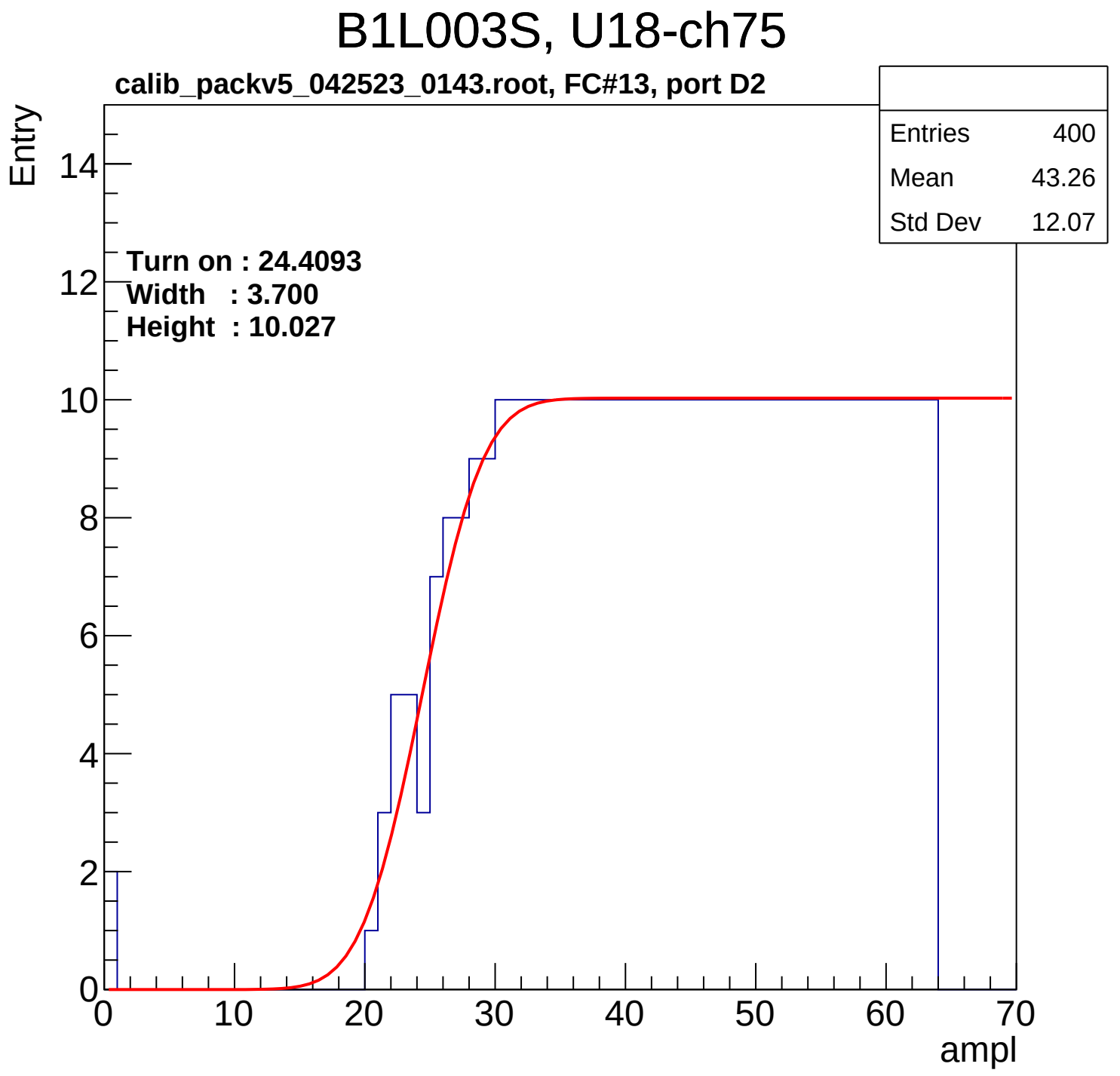
B1L003S, U18-ch75
calib_packv5_042523_0143.root, FC#13, port D2
Entries 400
Mean 43.26
Std Dev 12.07
Turn on : 24.4093
Width : 3.700
Height : 10.027
Entry
ampl
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8
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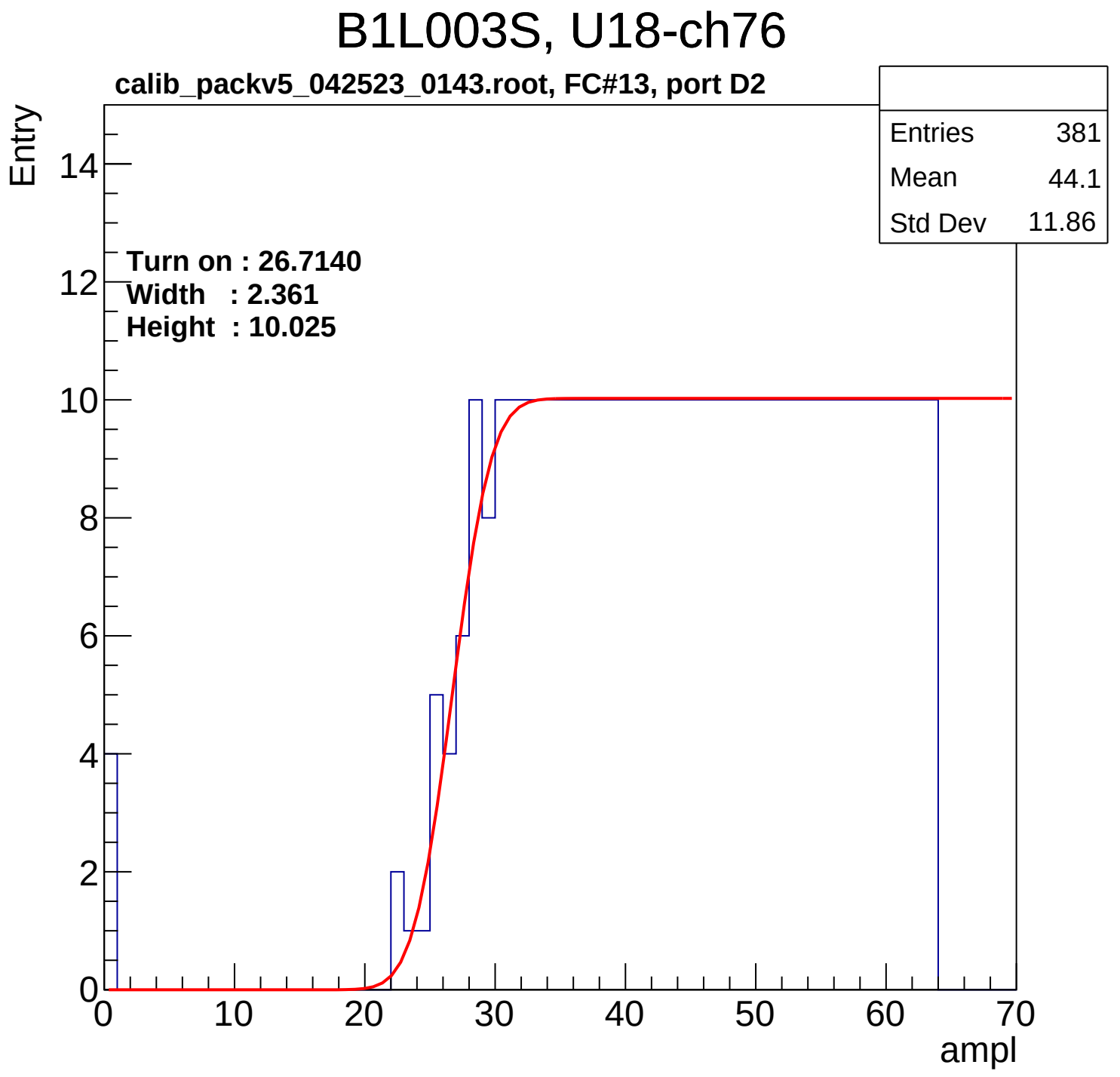
B1L003S, U18-ch76
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 44.1
Std Dev 11.86
Turn on : 26.7140
Width : 2.361
Height : 10.025
Entry
ampl
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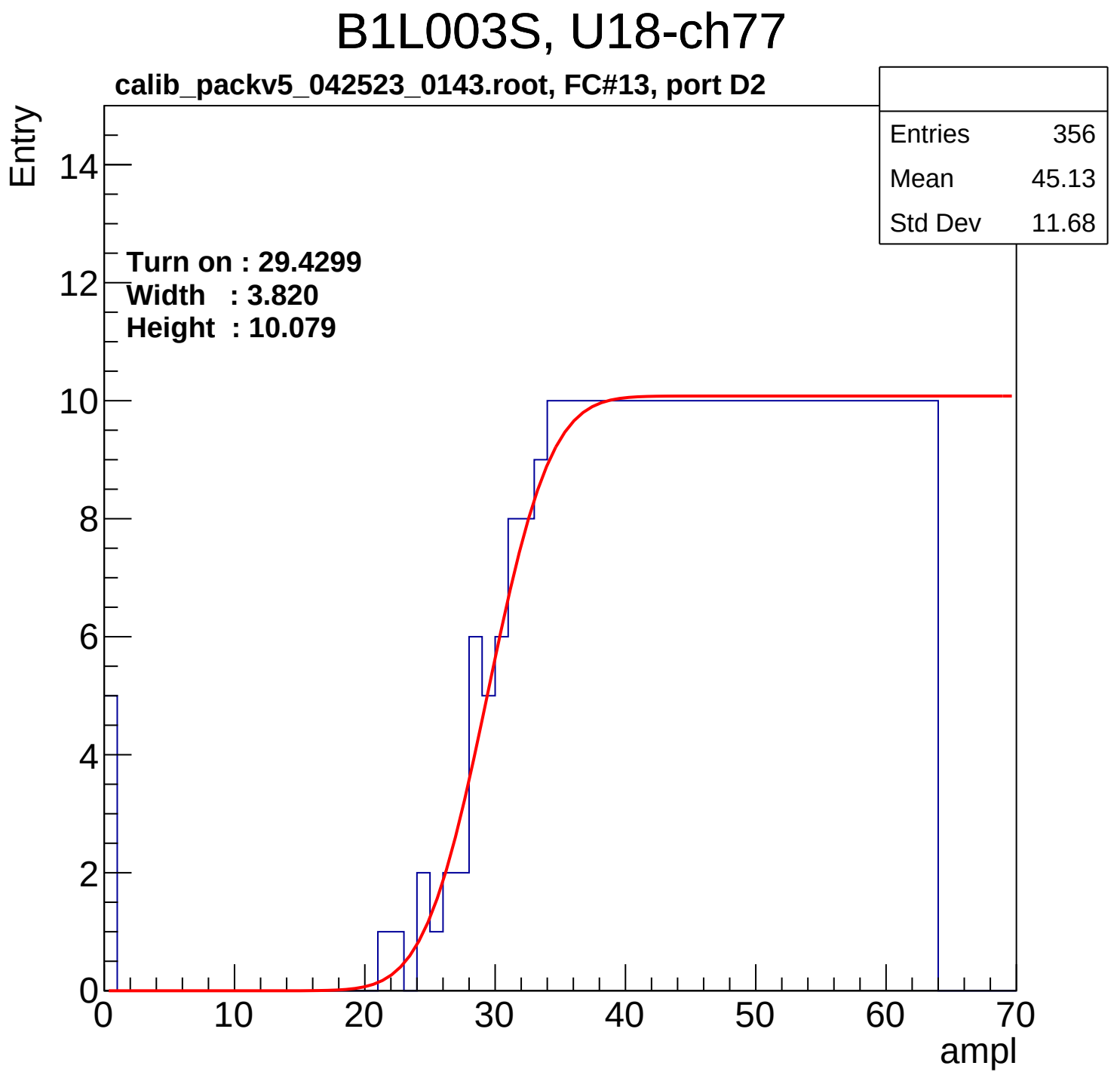
B1L003S, U18-ch77
calib_packv5_042523_0143.root, FC#13, port D2
Entries 356
Mean 45.13
Std Dev 11.68
Turn on : 29.4299
Width : 3.820
Height : 10.079
Entry
ampl
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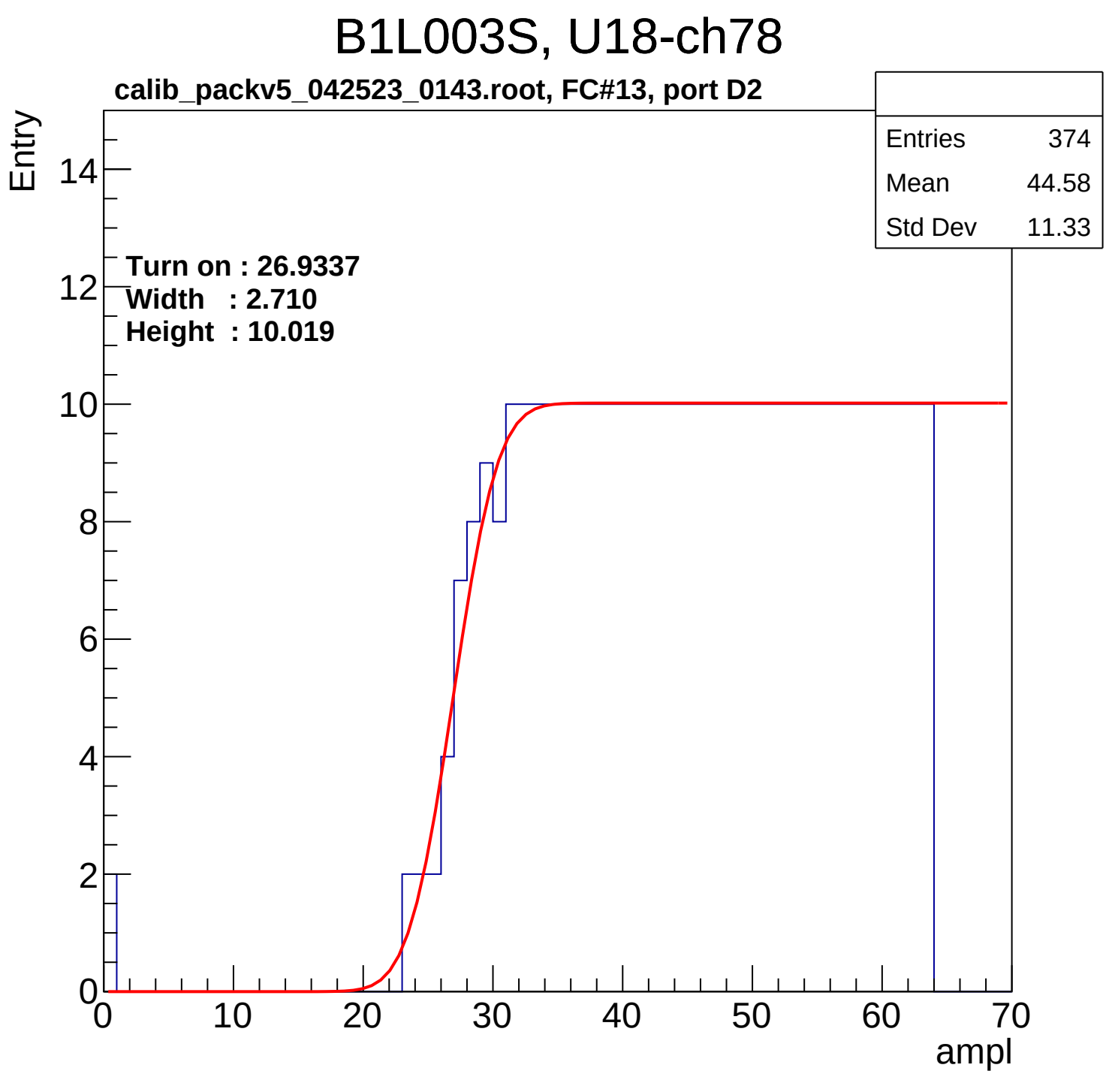
B1L003S, U18-ch78
calib_packv5_042523_0143.root, FC#13, port D2
Entries 374
Mean 44.58
Std Dev 11.33
Turn on : 26.9337
Width : 2.710
Height : 10.019
Entry
ampl
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2
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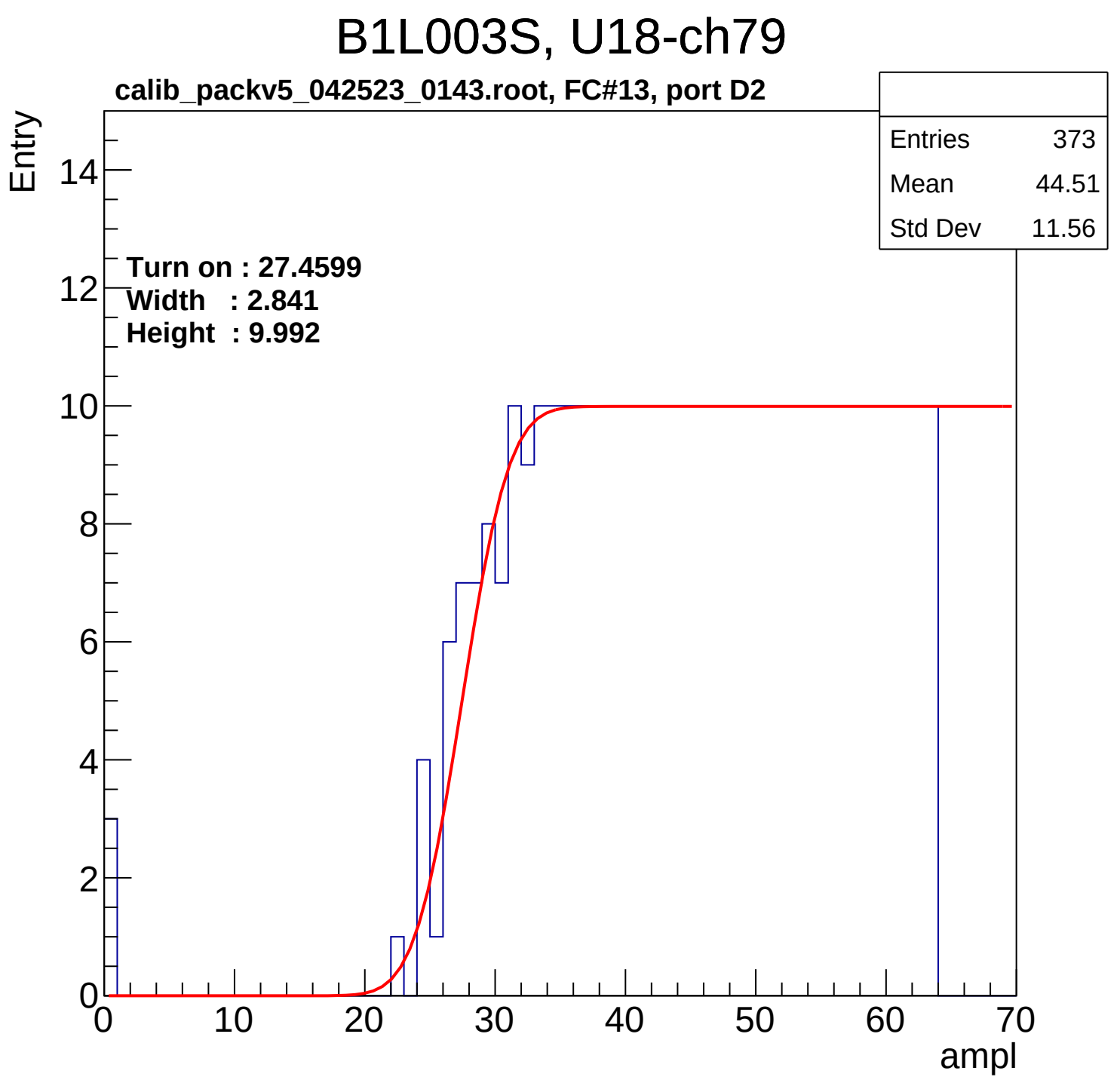
B1L003S, U18-ch79
calib_packv5_042523_0143.root, FC#13, port D2
Entries 373
Mean 44.51
Std Dev 11.56
Turn on : 27.4599
Width : 2.841
Height : 9.992
Entry
ampl
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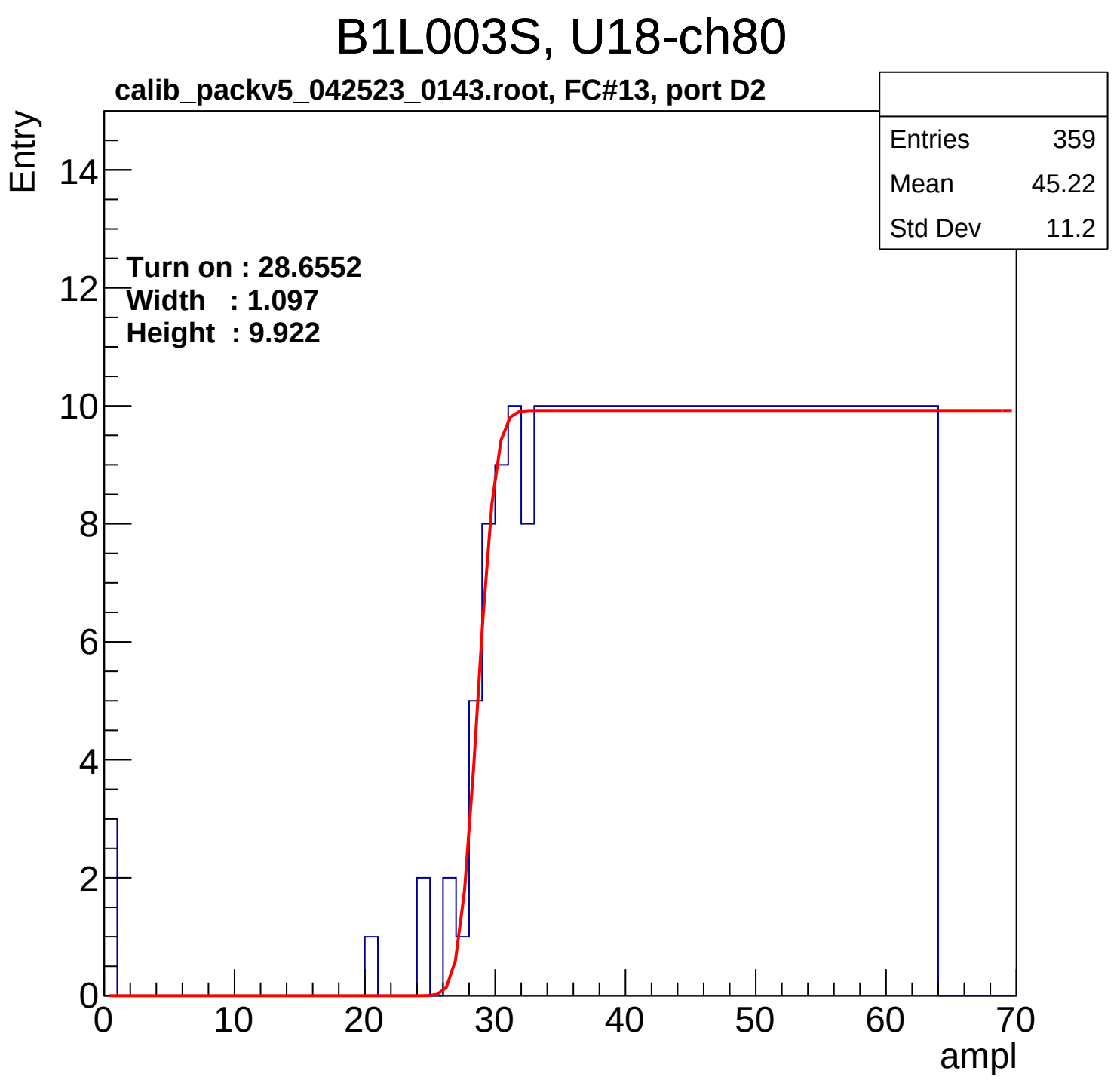
B1L003S, U18-ch80
calib_packv5_042523_0143.root, FC#13, port D2
Entries 359
Mean 45.22
Std Dev 11.2
Turn on : 28.6552
Width : 1.097
Height : 9.922
Entry
ampl
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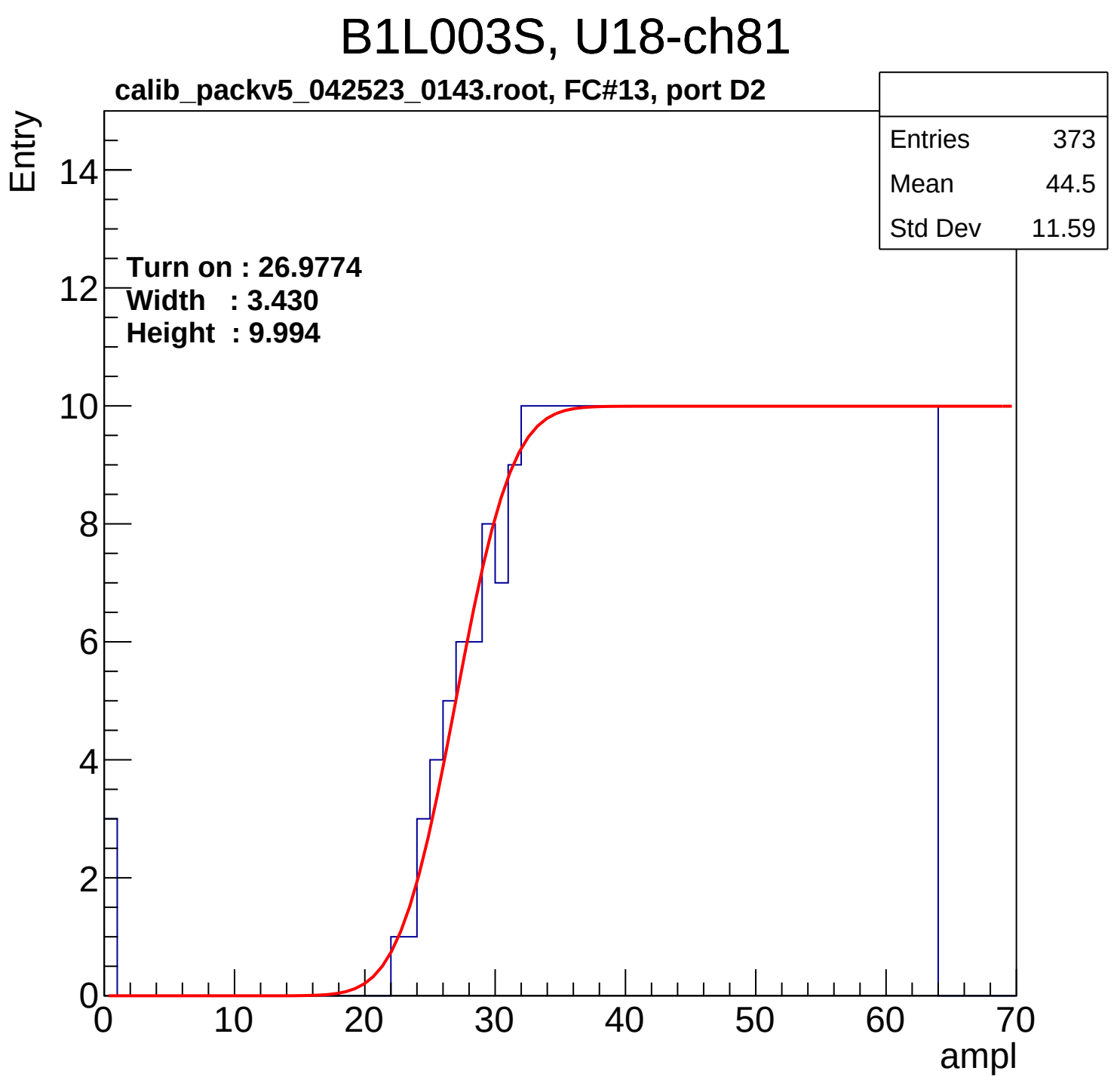
B1L003S, U18-ch81
calib_packv5_042523_0143.root, FC#13, port D2
Entries 373
Mean 44.5
Std Dev 11.59
Turn on : 26.9774
Width : 3.430
Height : 9.994
Entry
ampl
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8
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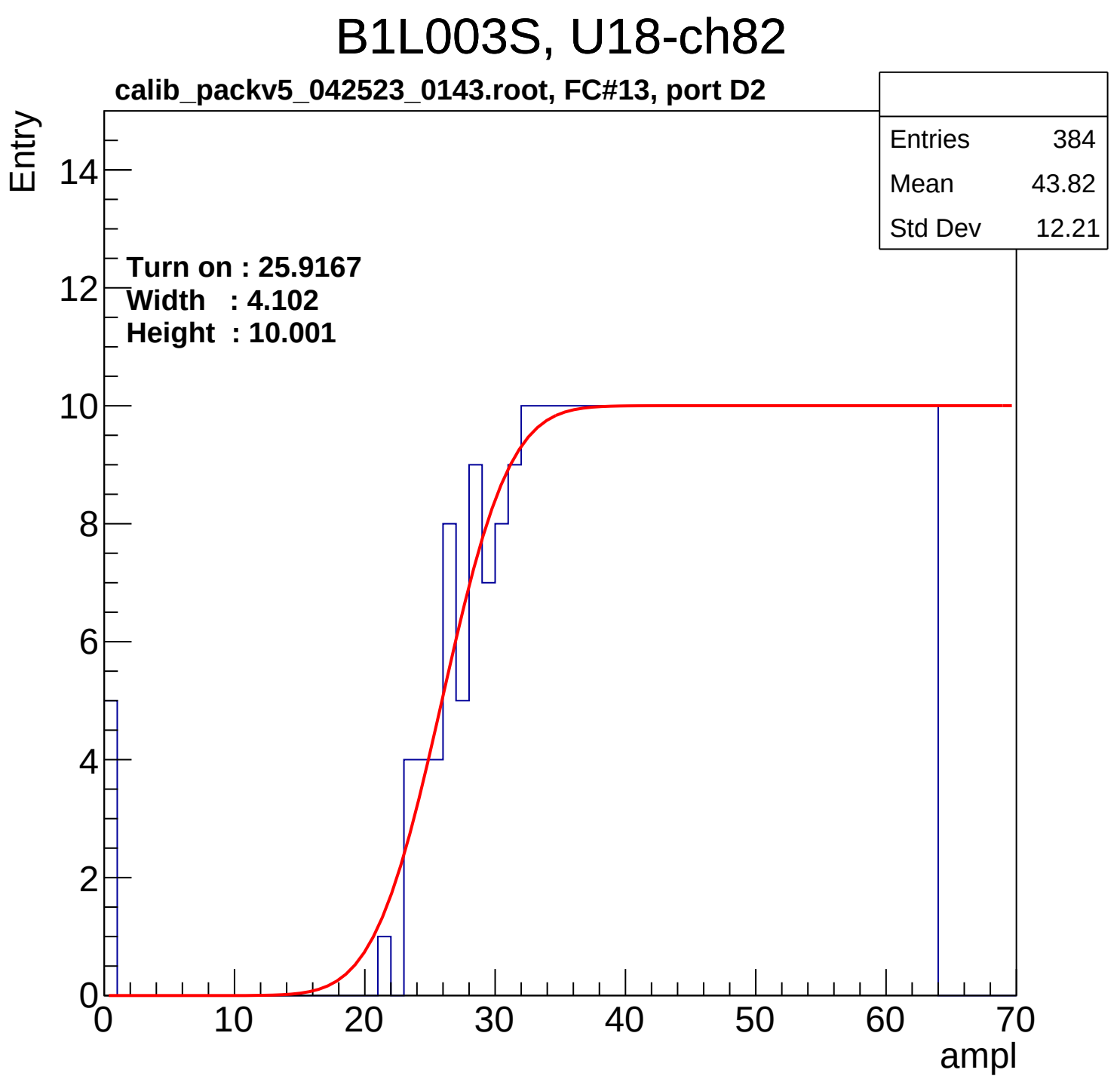
B1L003S, U18-ch82
calib_packv5_042523_0143.root, FC#13, port D2
Entries 384
Mean 43.82
Std Dev 12.21
Turn on : 25.9167
Width : 4.102
Height : 10.001
Entry
ampl
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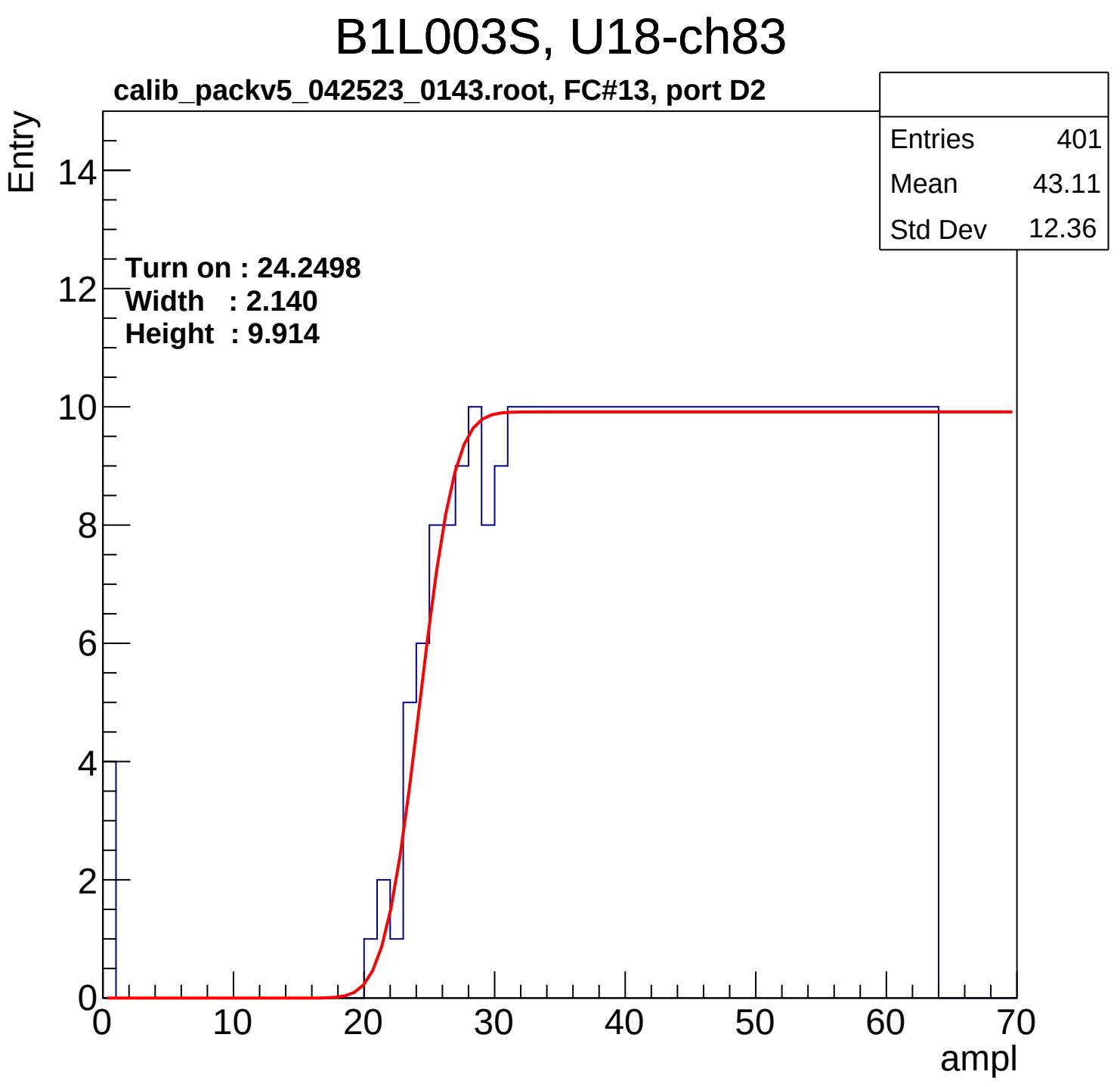
B1L003S, U18-ch83
calib_packv5_042523_0143.root, FC#13, port D2
Entries 401
Mean 43.11
Std Dev 12.36
Turn on : 24.2498
Width : 2.140
Height : 9.914
Entry
ampl
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6
8
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60
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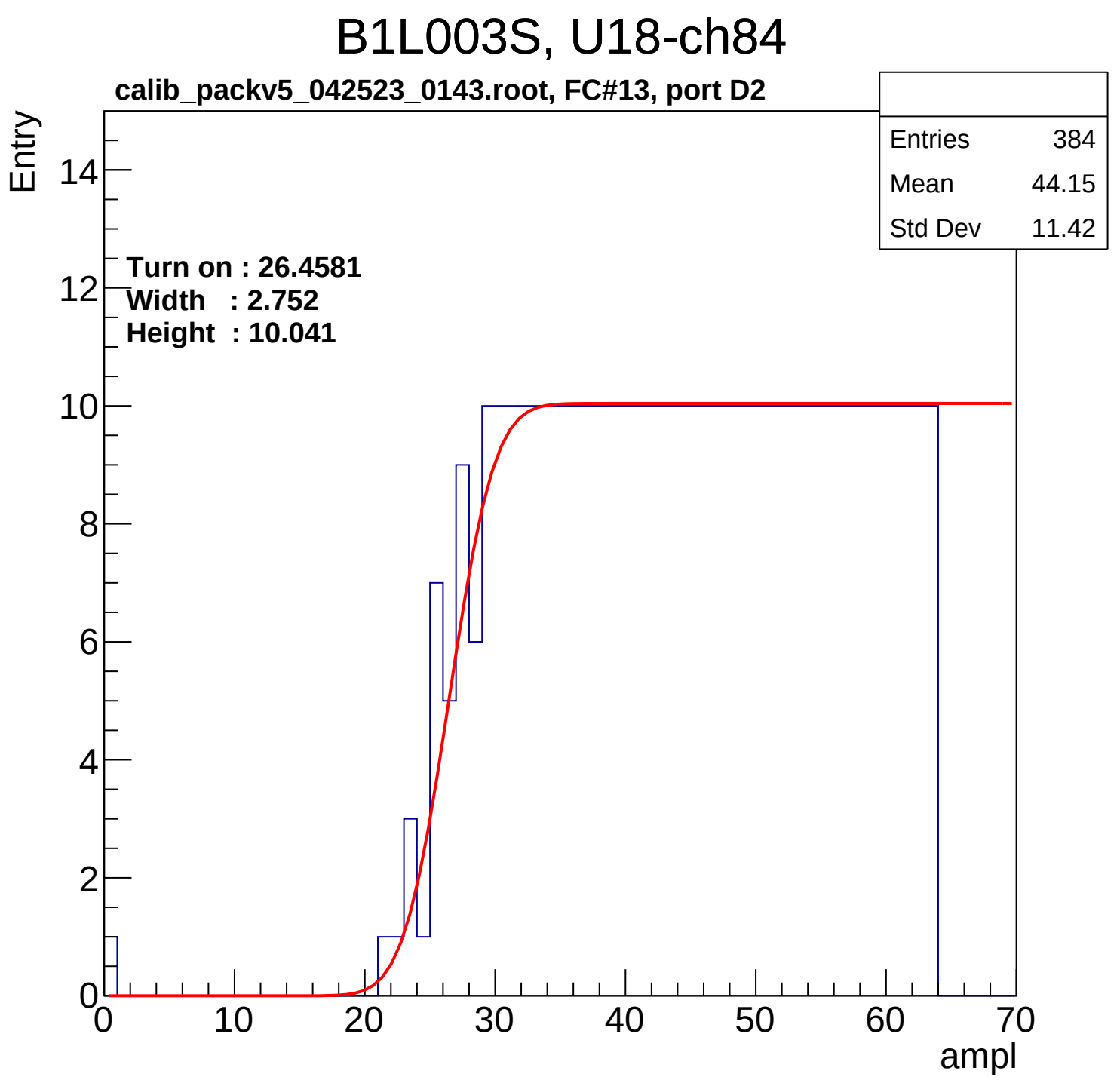
B1L003S, U18-ch84
calib_packv5_042523_0143.root, FC#13, port D2
Entries 384
Mean 44.15
Std Dev 11.42
Turn on : 26.4581
Width : 2.752
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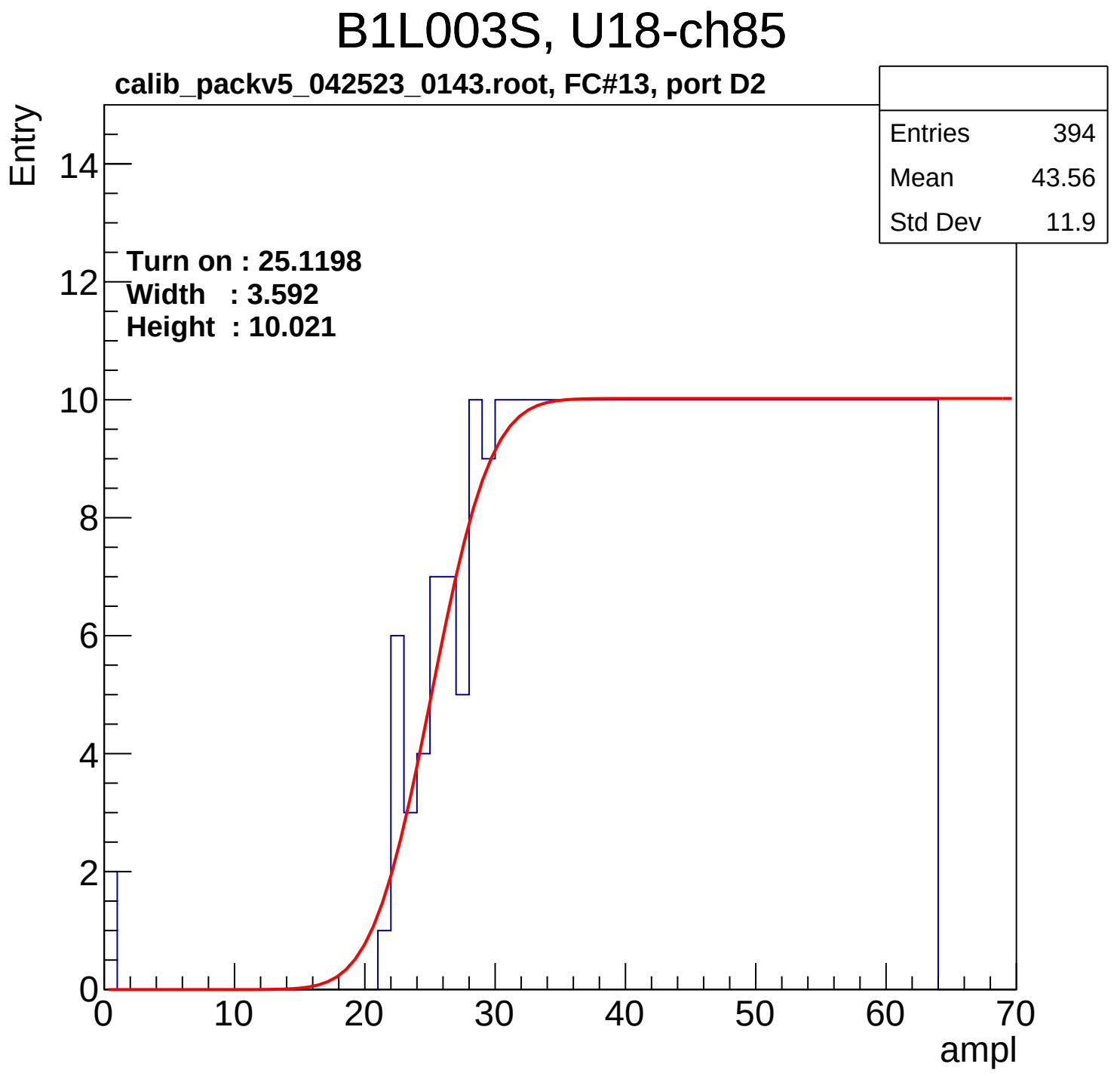
B1L003S, U18-ch85
calib_packv5_042523_0143.root, FC#13, port D2
Entries 394
Mean 43.56
Std Dev 11.9
Turn on : 25.1198
Width : 3.592
Height : 10.021
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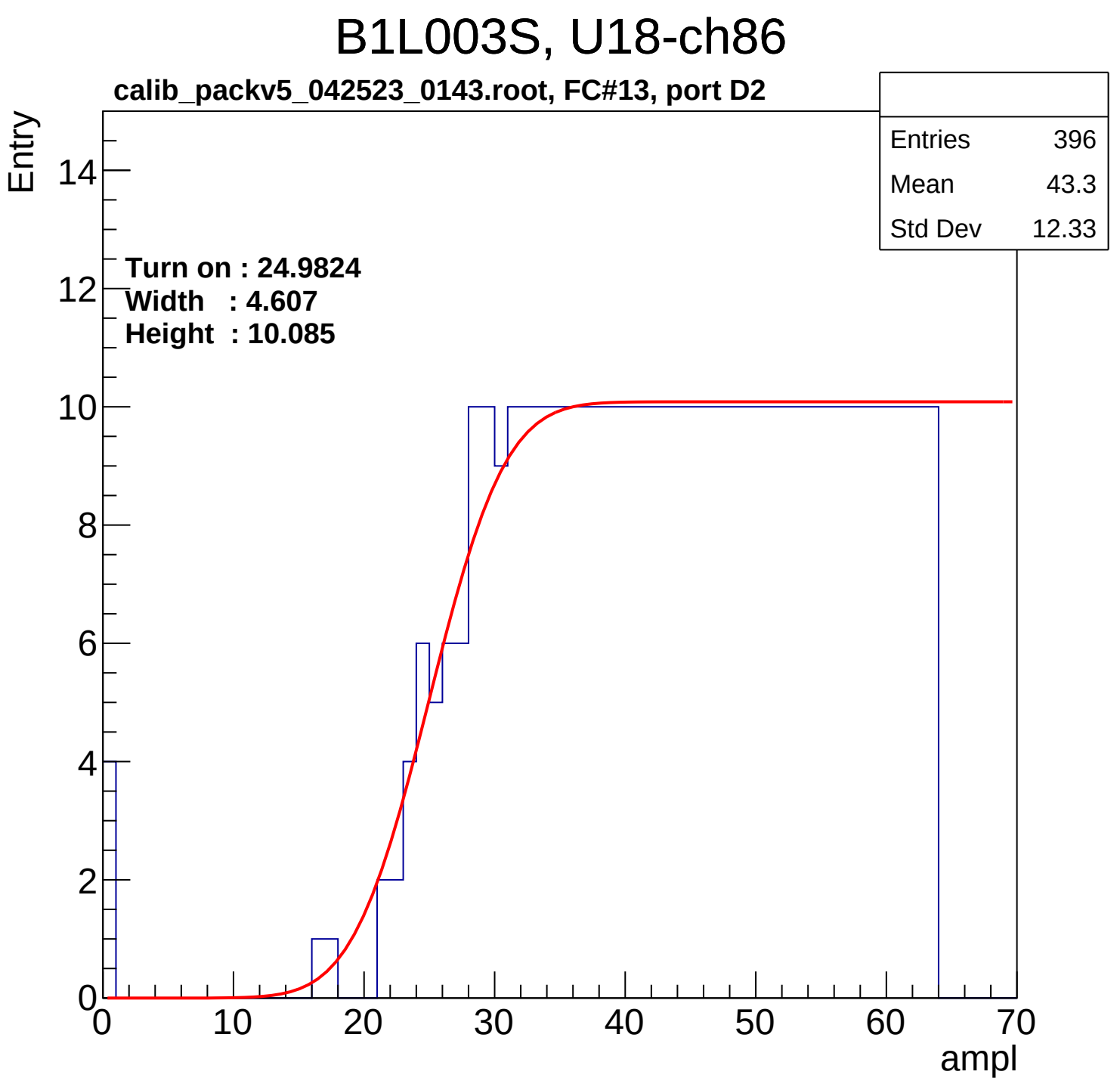
B1L003S, U18-ch86
calib_packv5_042523_0143.root, FC#13, port D2
Entries 396
Mean 43.3
Std Dev 12.33
Turn on : 24.9824
Width : 4.607
Height : 10.085
Entry
ampl
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4
6
8
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12
14
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40
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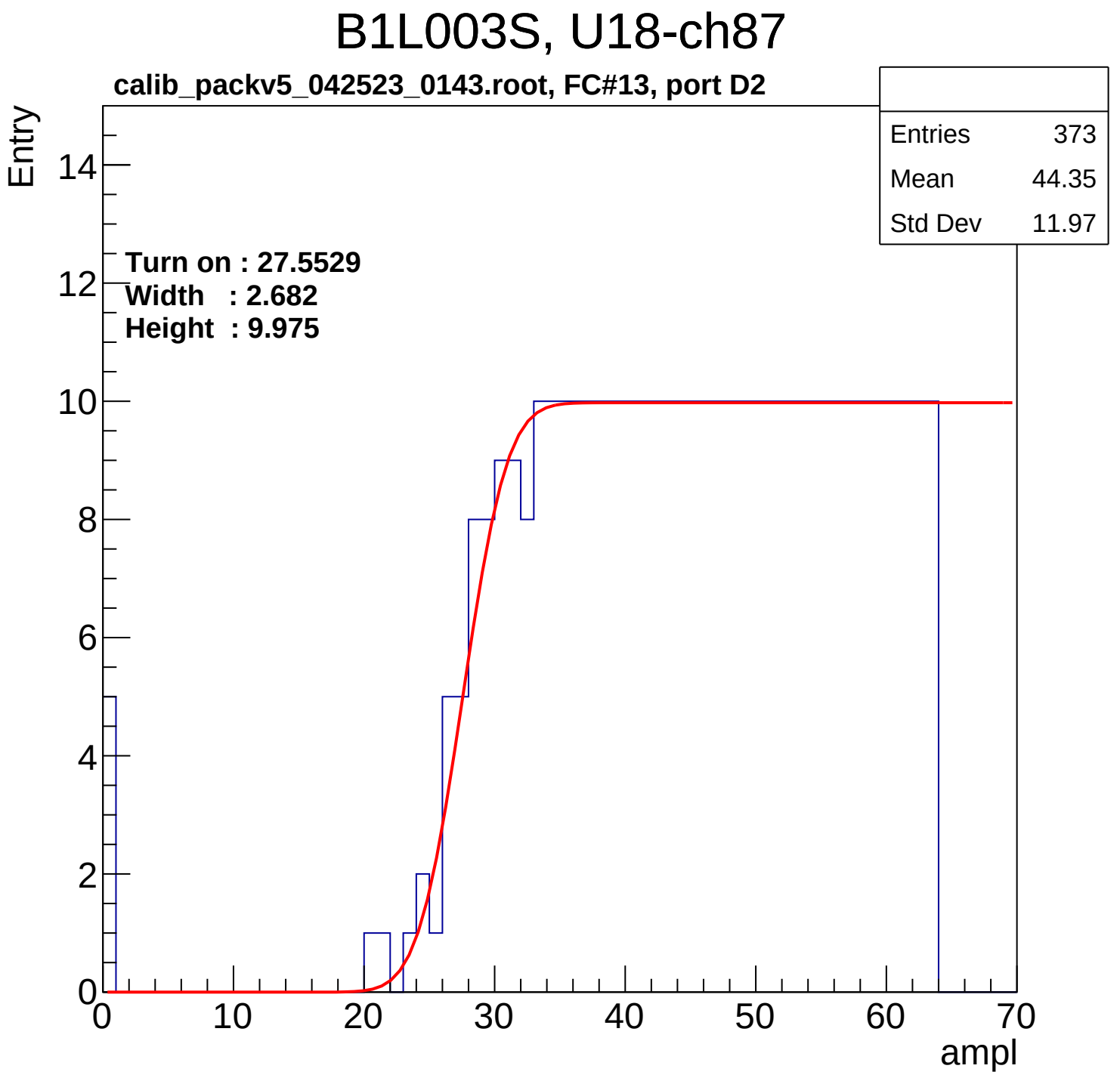
B1L003S, U18-ch87
calib_packv5_042523_0143.root, FC#13, port D2
Entries 373
Mean 44.35
Std Dev 11.97
Turn on : 27.5529
Width : 2.682
Height : 9.975
Entry
ampl
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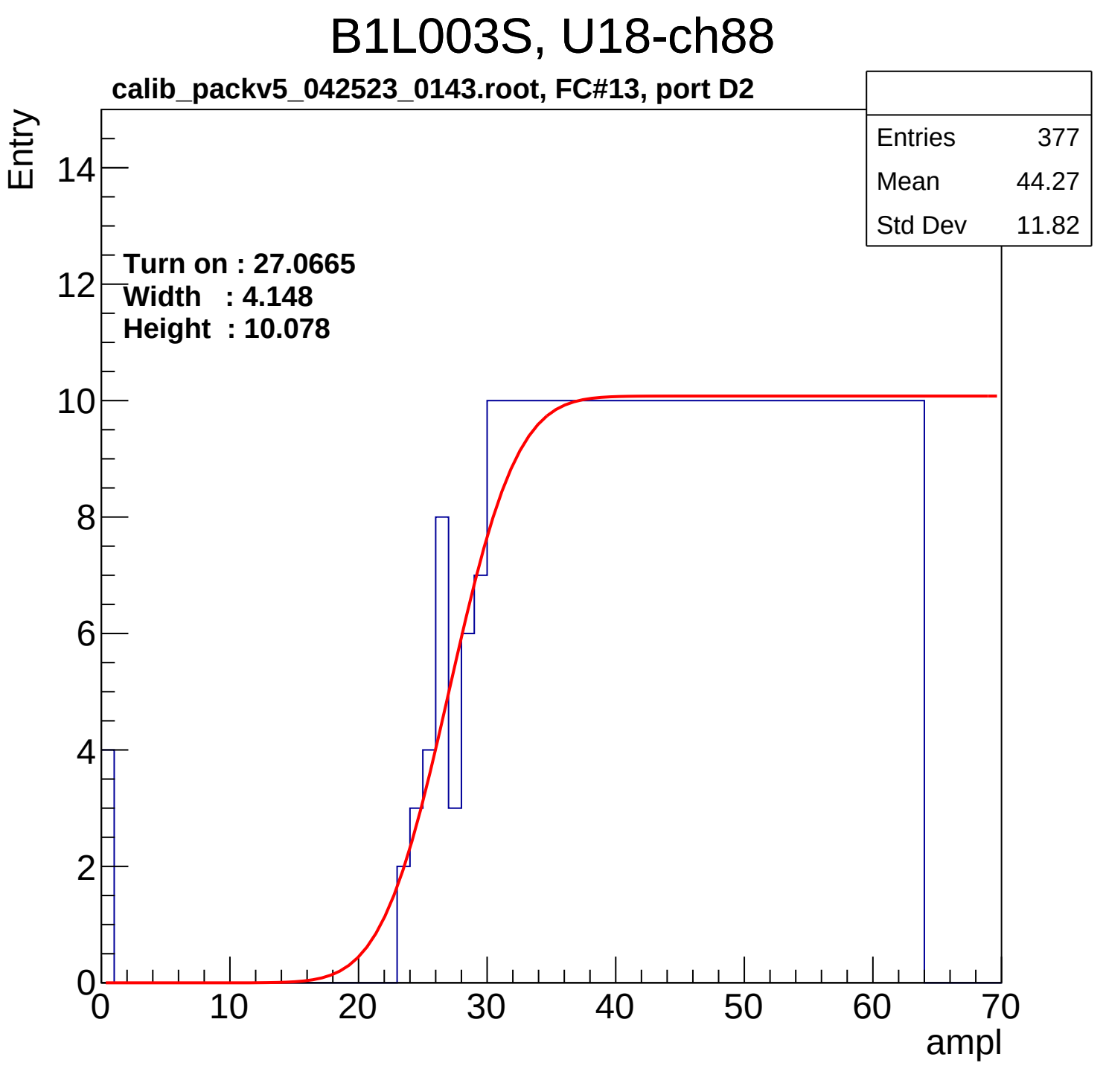
B1L003S, U18-ch88
calib_packv5_042523_0143.root, FC#13, port D2
Entries 377
Mean 44.27
Std Dev 11.82
Turn on : 27.0665
Width : 4.148
Height : 10.078
Entry
ampl
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2
4
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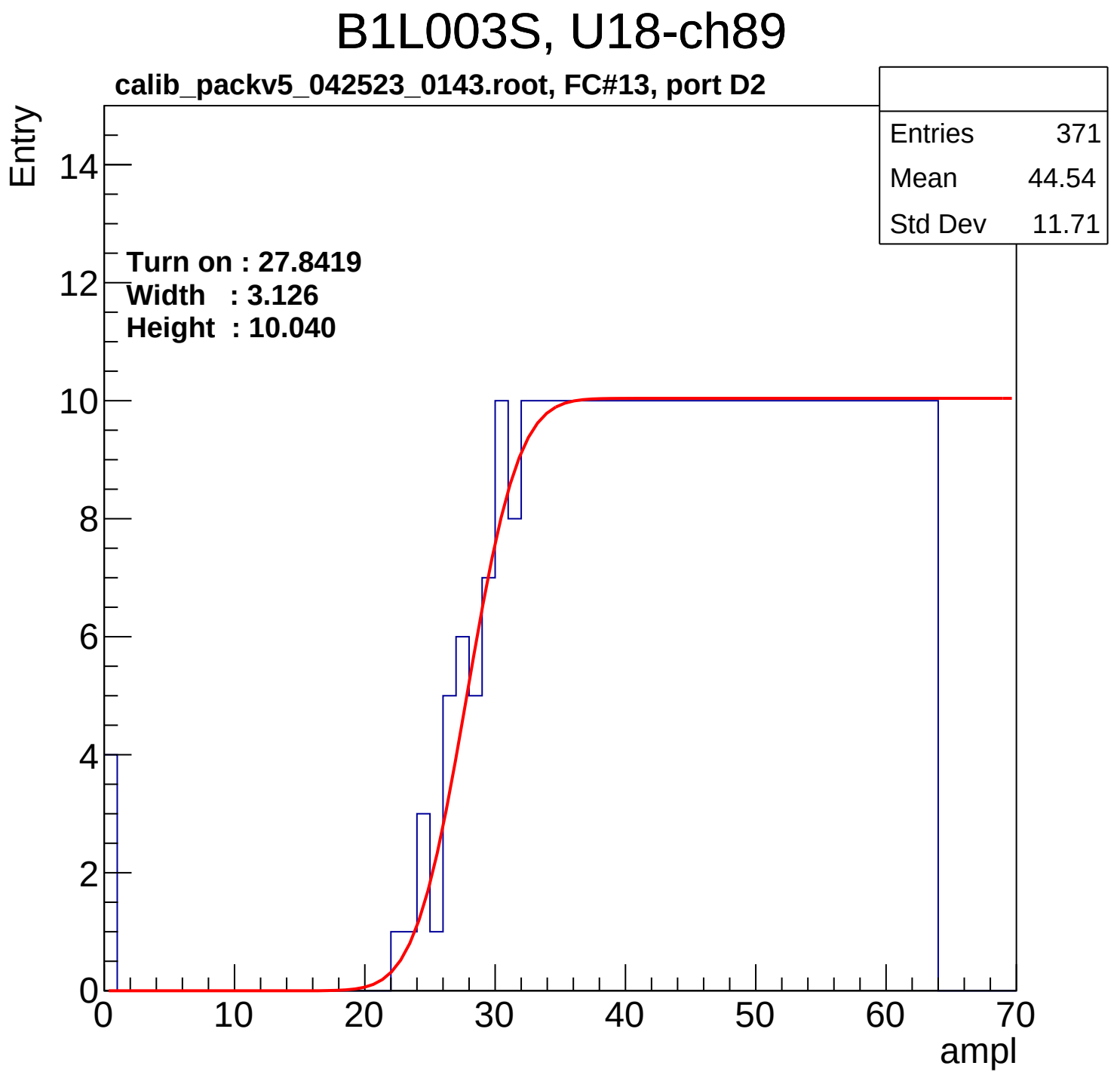
B1L003S, U18-ch89
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.54
Std Dev 11.71
Turn on : 27.8419
Width : 3.126
Height : 10.040
Entry
ampl
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2
4
6
8
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12
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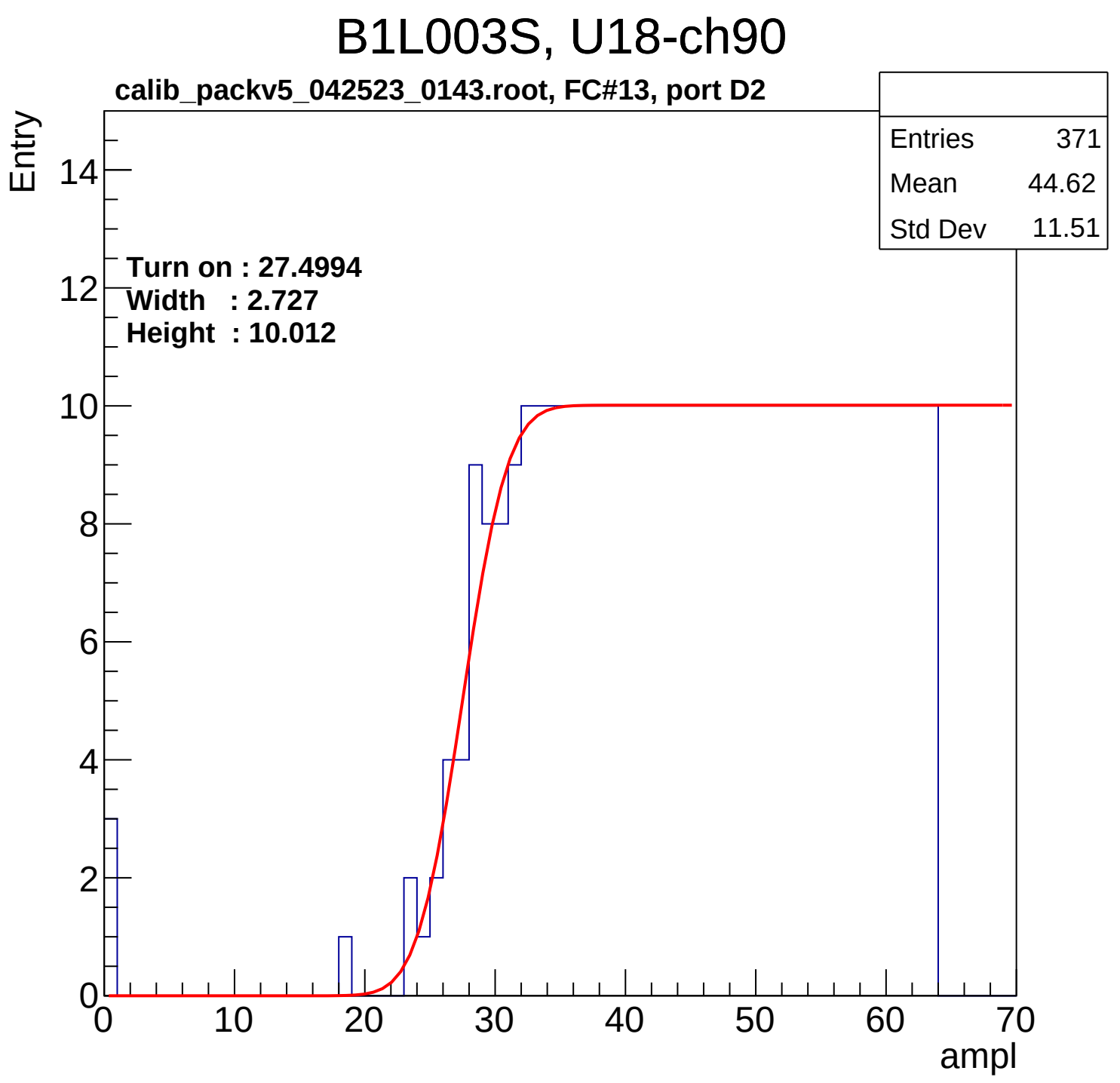
B1L003S, U18-ch90
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.62
Std Dev 11.51
Turn on : 27.4994
Width : 2.727
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
14
0
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60
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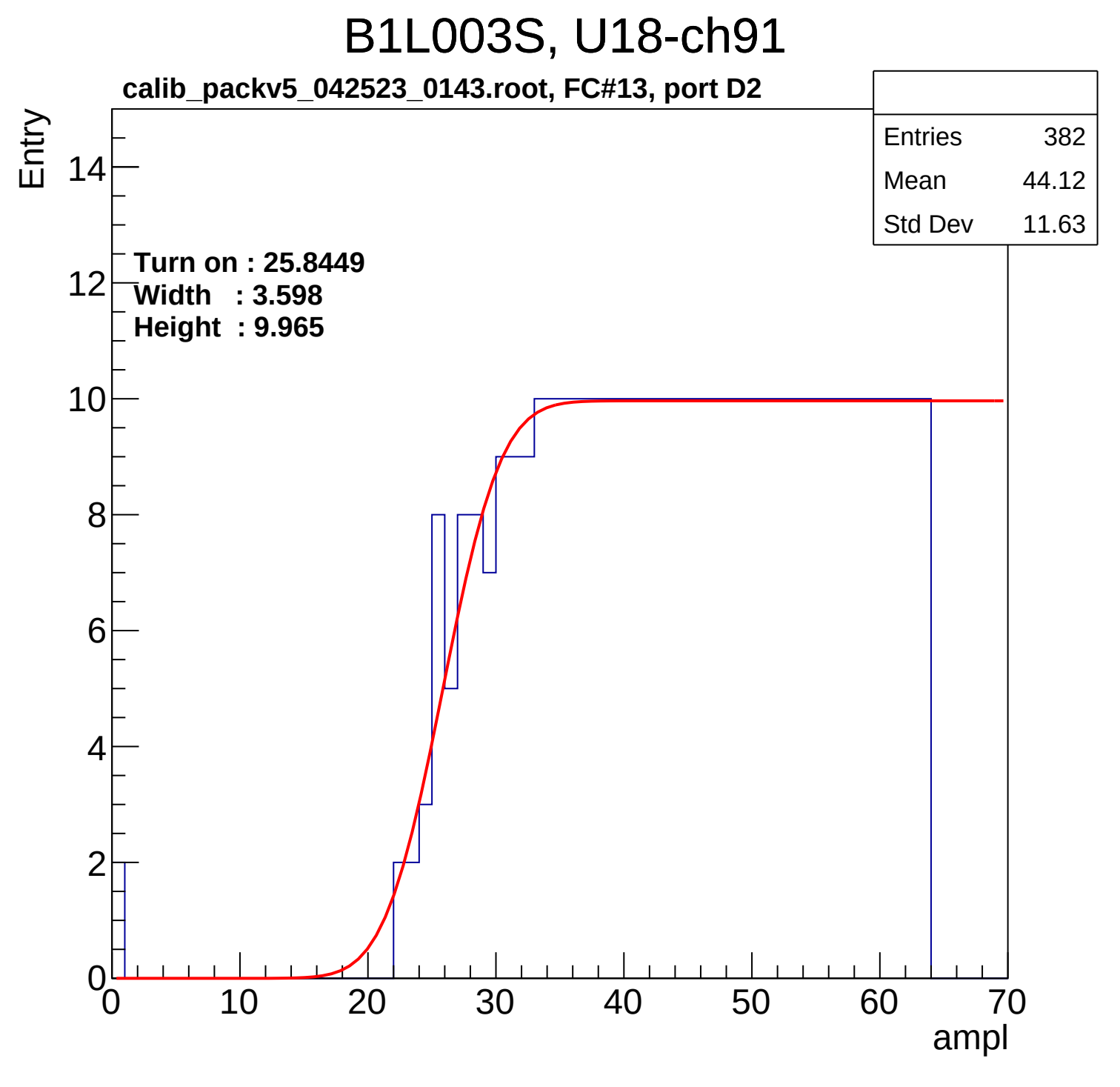
B1L003S, U18-ch91
calib_packv5_042523_0143.root, FC#13, port D2
Entries 382
Mean 44.12
Std Dev 11.63
Turn on : 25.8449
Width : 3.598
Height : 9.965
Entry
ampl
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2
4
6
8
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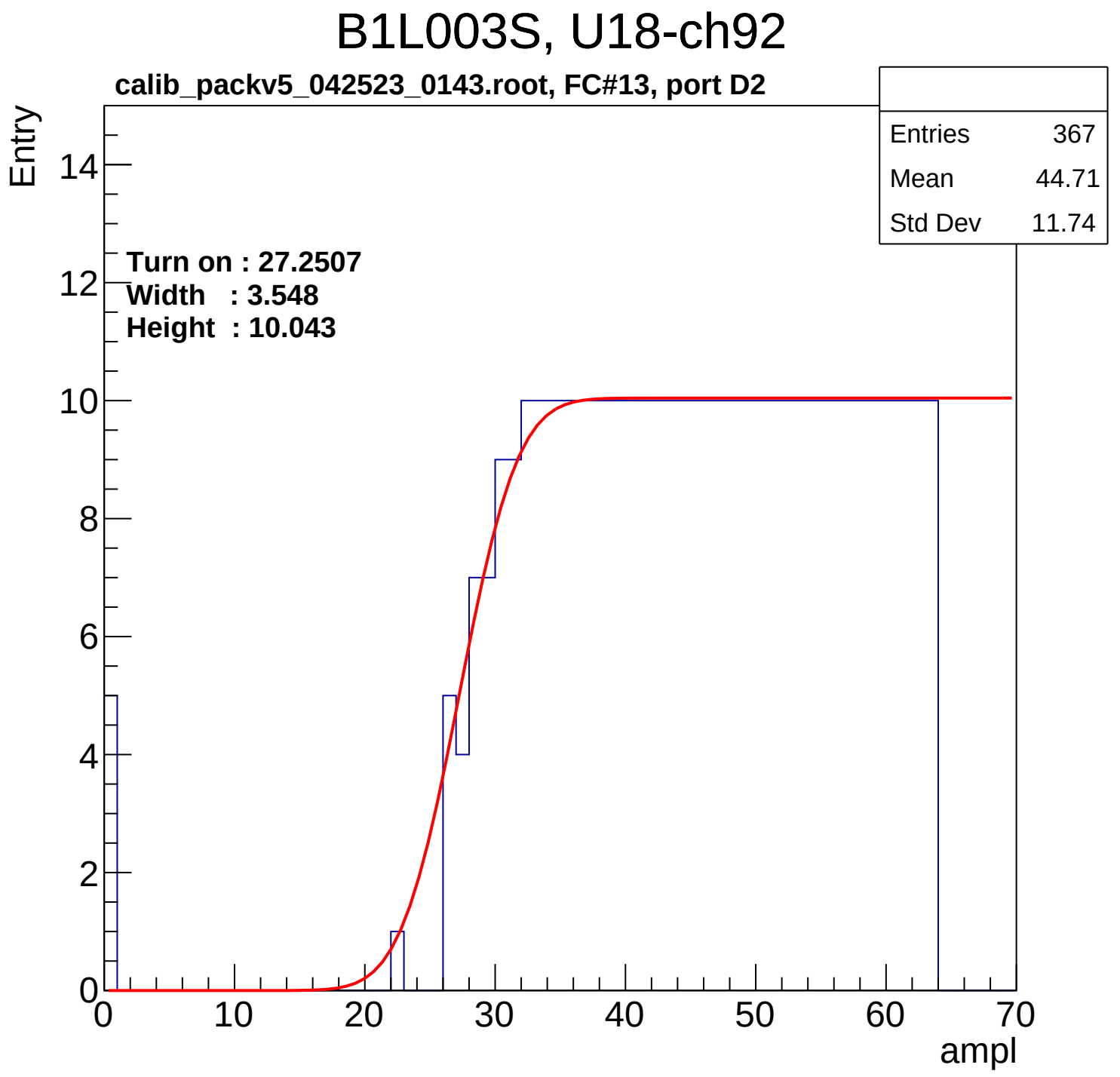
B1L003S, U18-ch92
calib_packv5_042523_0143.root, FC#13, port D2
Entries 367
Mean 44.71
Std Dev 11.74
Turn on : 27.2507
Width : 3.548
Height : 10.043
Entry
ampl
0
2
4
6
8
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12
14
0
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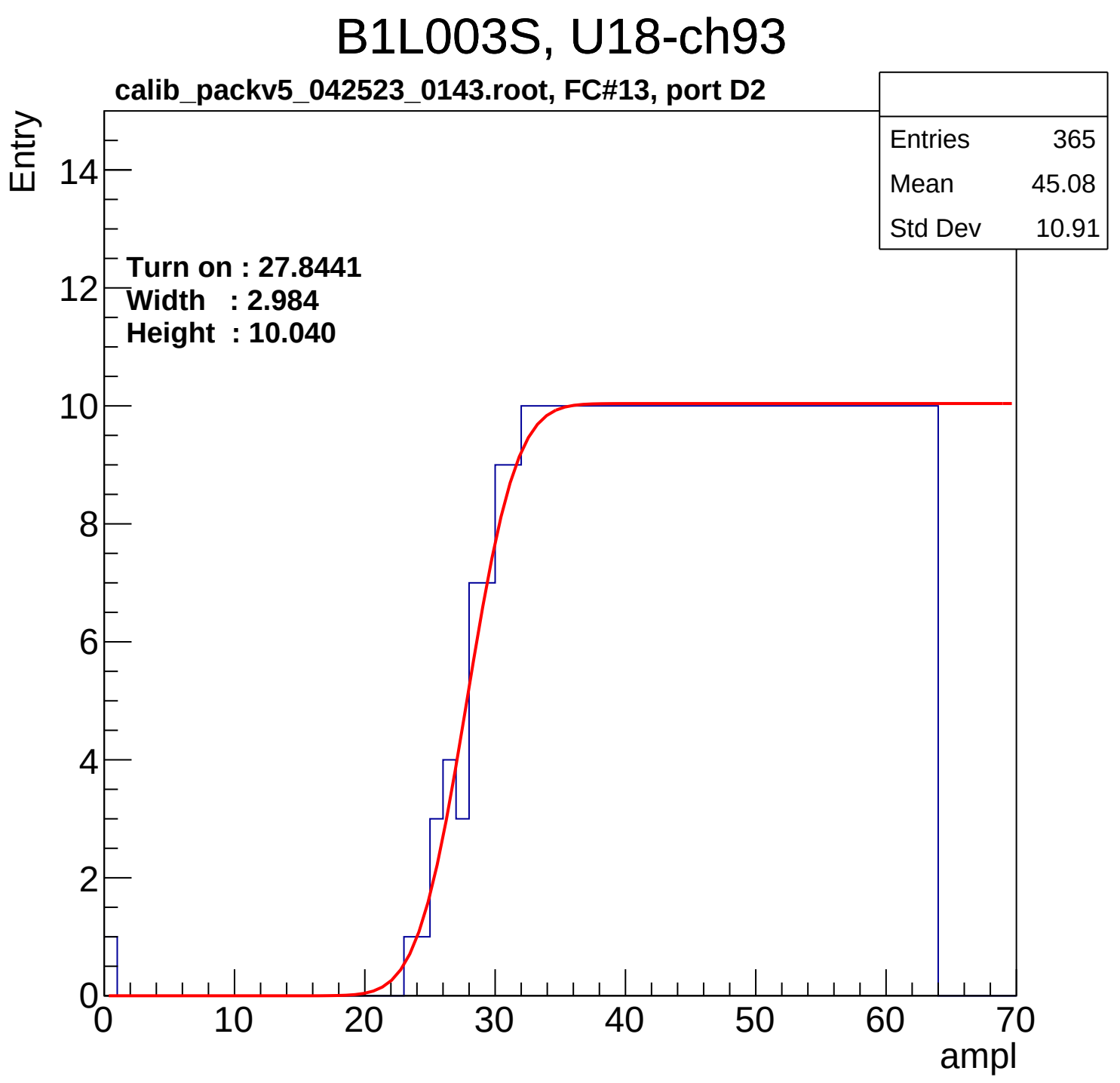
B1L003S, U18-ch93
calib_packv5_042523_0143.root, FC#13, port D2
Entries 365
Mean 45.08
Std Dev 10.91
Turn on : 27.8441
Width : 2.984
Height : 10.040
Entry
ampl
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2
4
6
8
10
12
14
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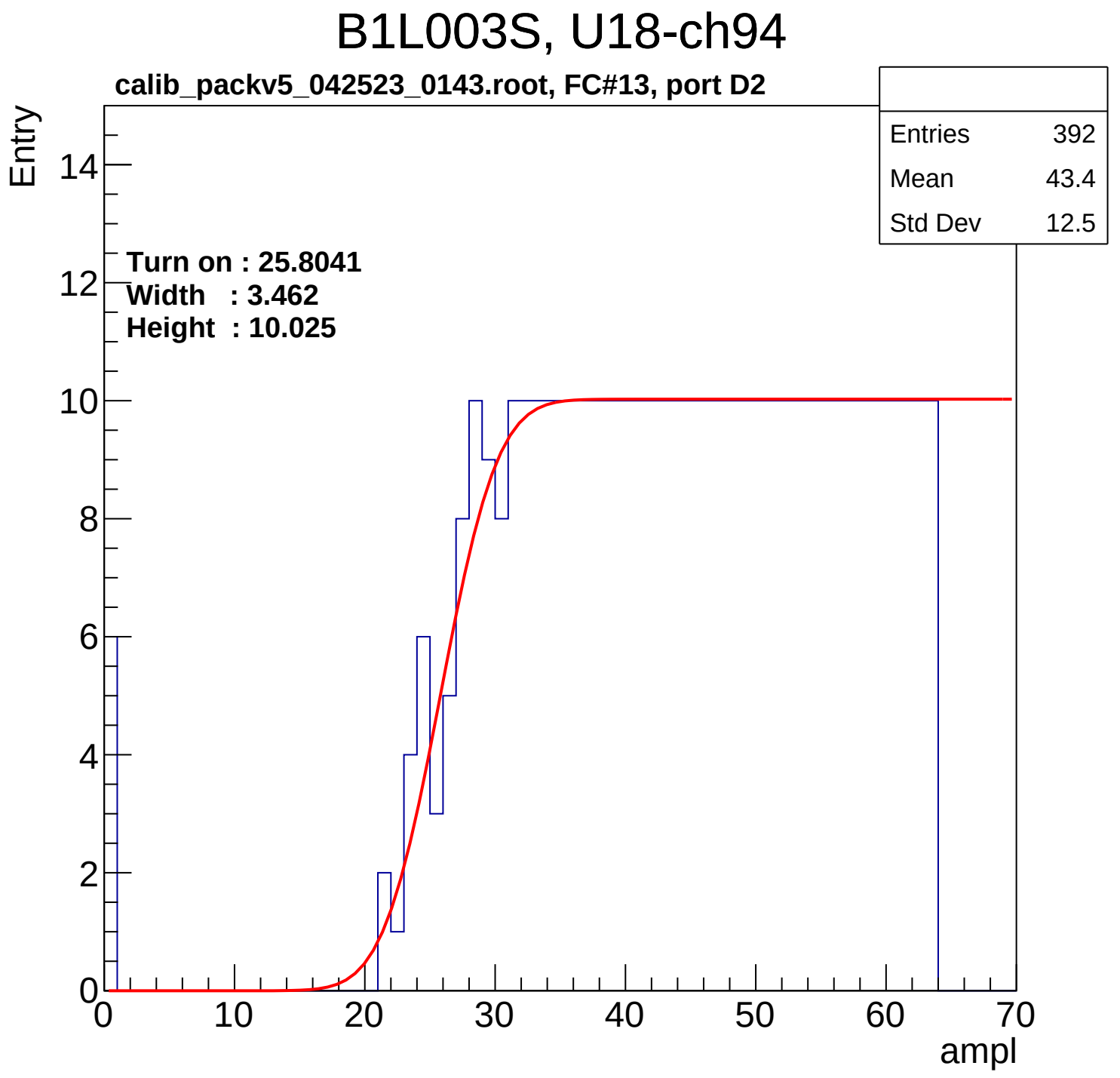
B1L003S, U18-ch94
calib_packv5_042523_0143.root, FC#13, port D2
Entries 392
Mean 43.4
Std Dev 12.5
Turn on : 25.8041
Width : 3.462
Height : 10.025
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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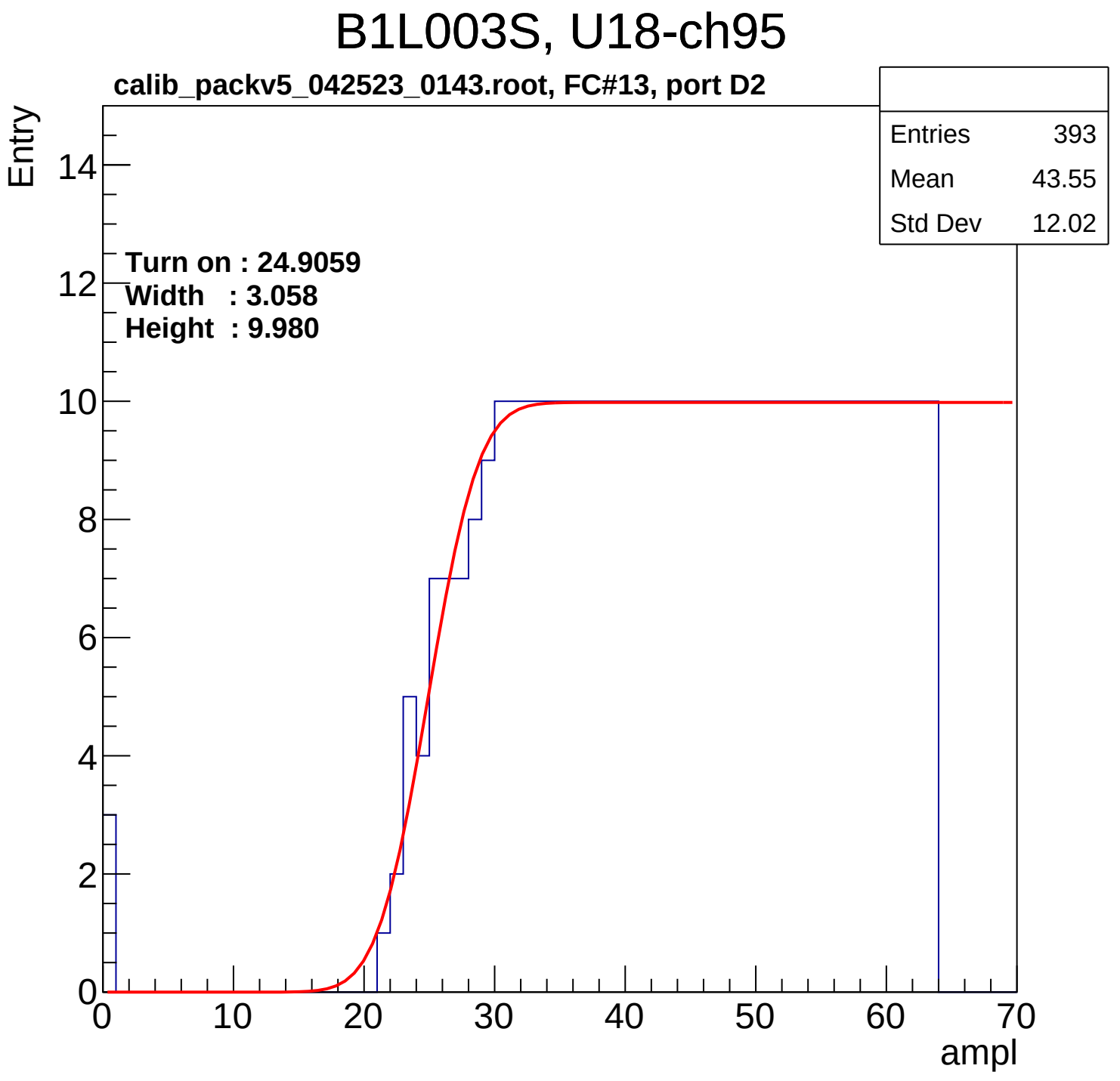
B1L003S, U18-ch95
calib_packv5_042523_0143.root, FC#13, port D2
Entries 393
Mean 43.55
Std Dev 12.02
Turn on : 24.9059
Width : 3.058
Height : 9.980
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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60
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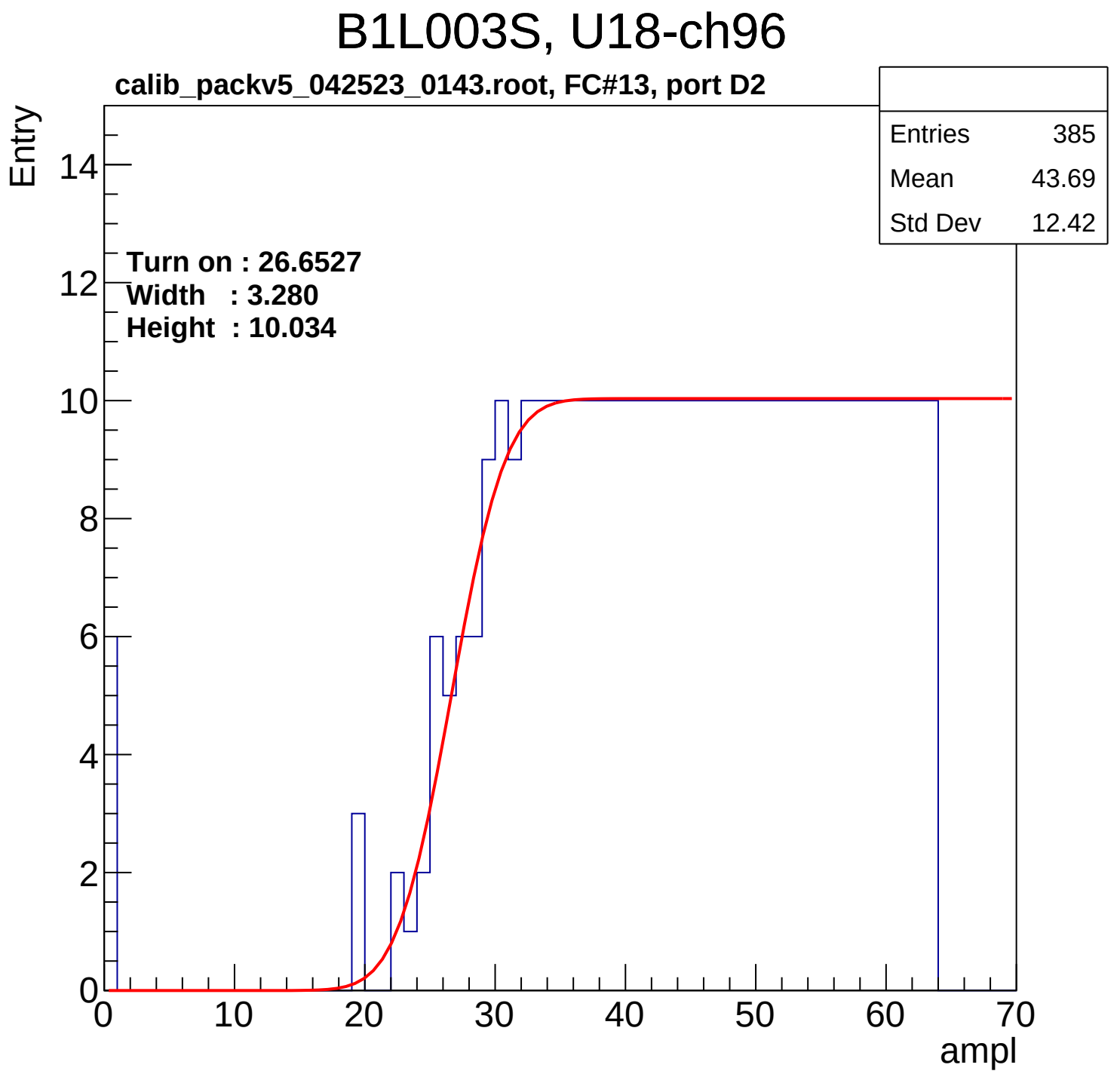
B1L003S, U18-ch96
calib_packv5_042523_0143.root, FC#13, port D2
Entries 385
Mean 43.69
Std Dev 12.42
Turn on : 26.6527
Width : 3.280
Height : 10.034
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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40
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60
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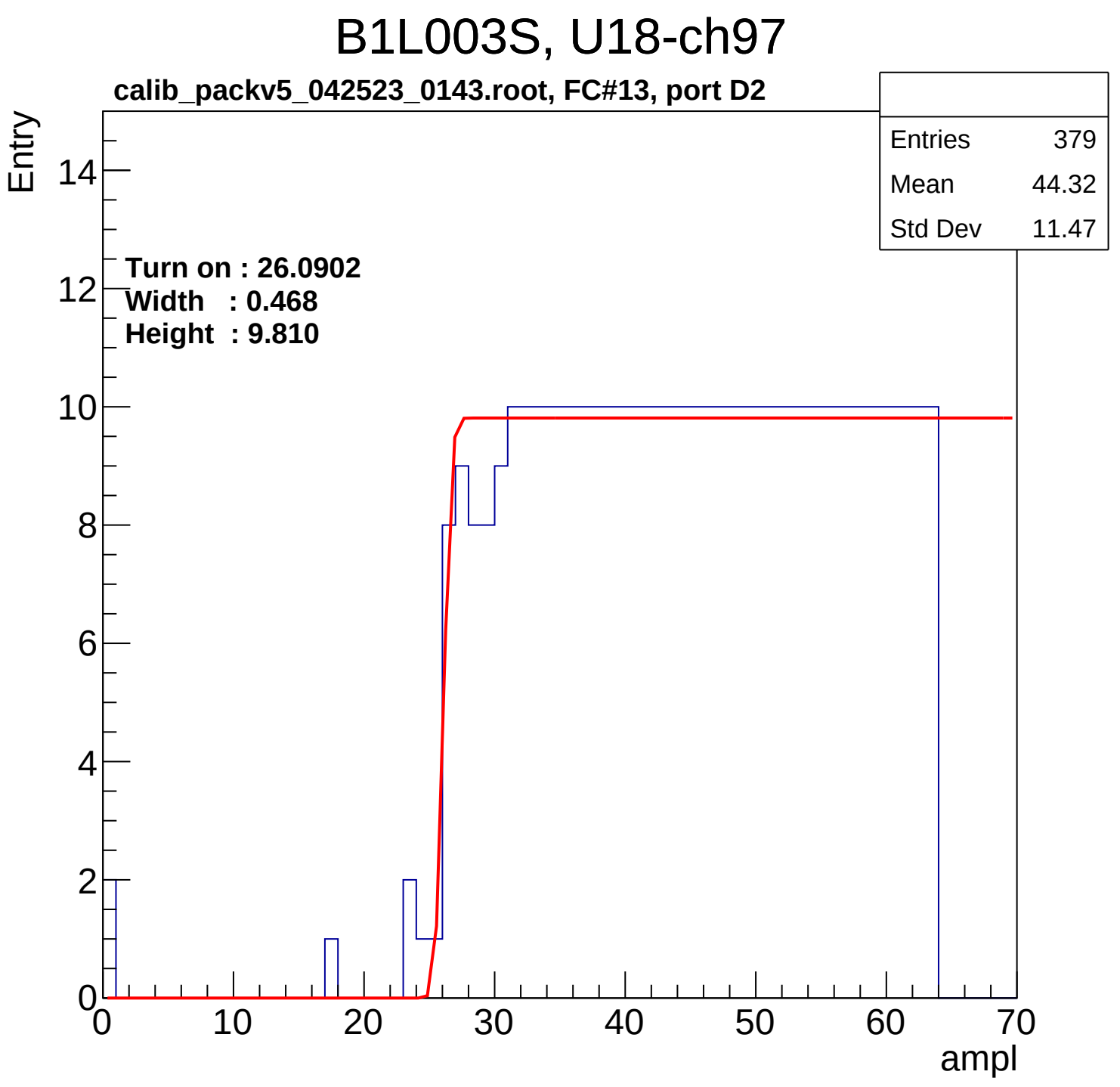
B1L003S, U18-ch97
calib_packv5_042523_0143.root, FC#13, port D2
Entries 379
Mean 44.32
Std Dev 11.47
Turn on : 26.0902
Width : 0.468
Height : 9.810
Entry
ampl
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2
4
6
8
10
12
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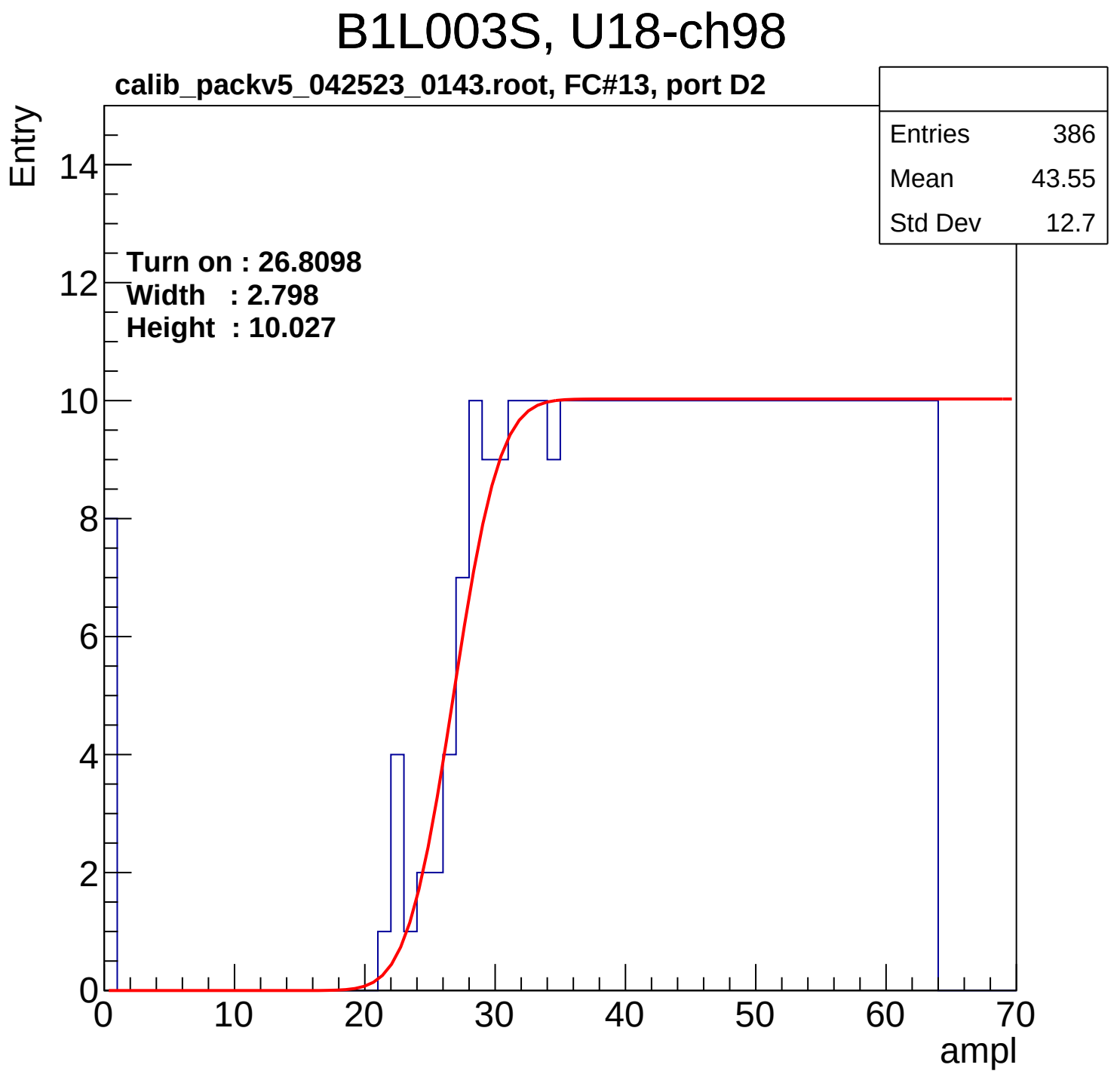
B1L003S, U18-ch98
calib_packv5_042523_0143.root, FC#13, port D2
Entries 386
Mean 43.55
Std Dev 12.7
Turn on : 26.8098
Width : 2.798
Height : 10.027
Entry
ampl
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2
4
6
8
10
12
14
0
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20
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60
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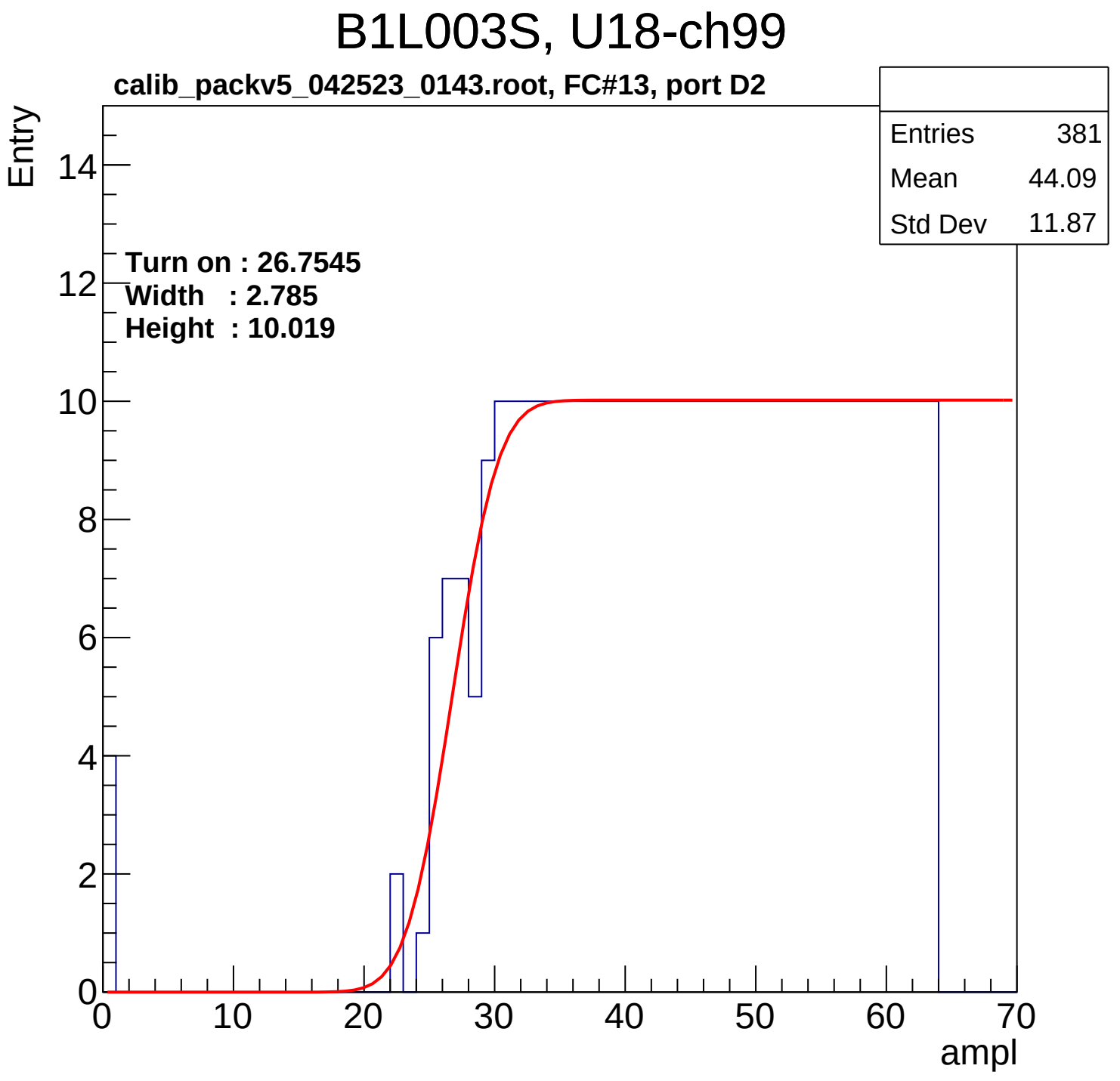
B1L003S, U18-ch99
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 44.09
Std Dev 11.87
Turn on : 26.7545
Width : 2.785
Height : 10.019
Entry
ampl
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4
6
8
10
12
14
0
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20
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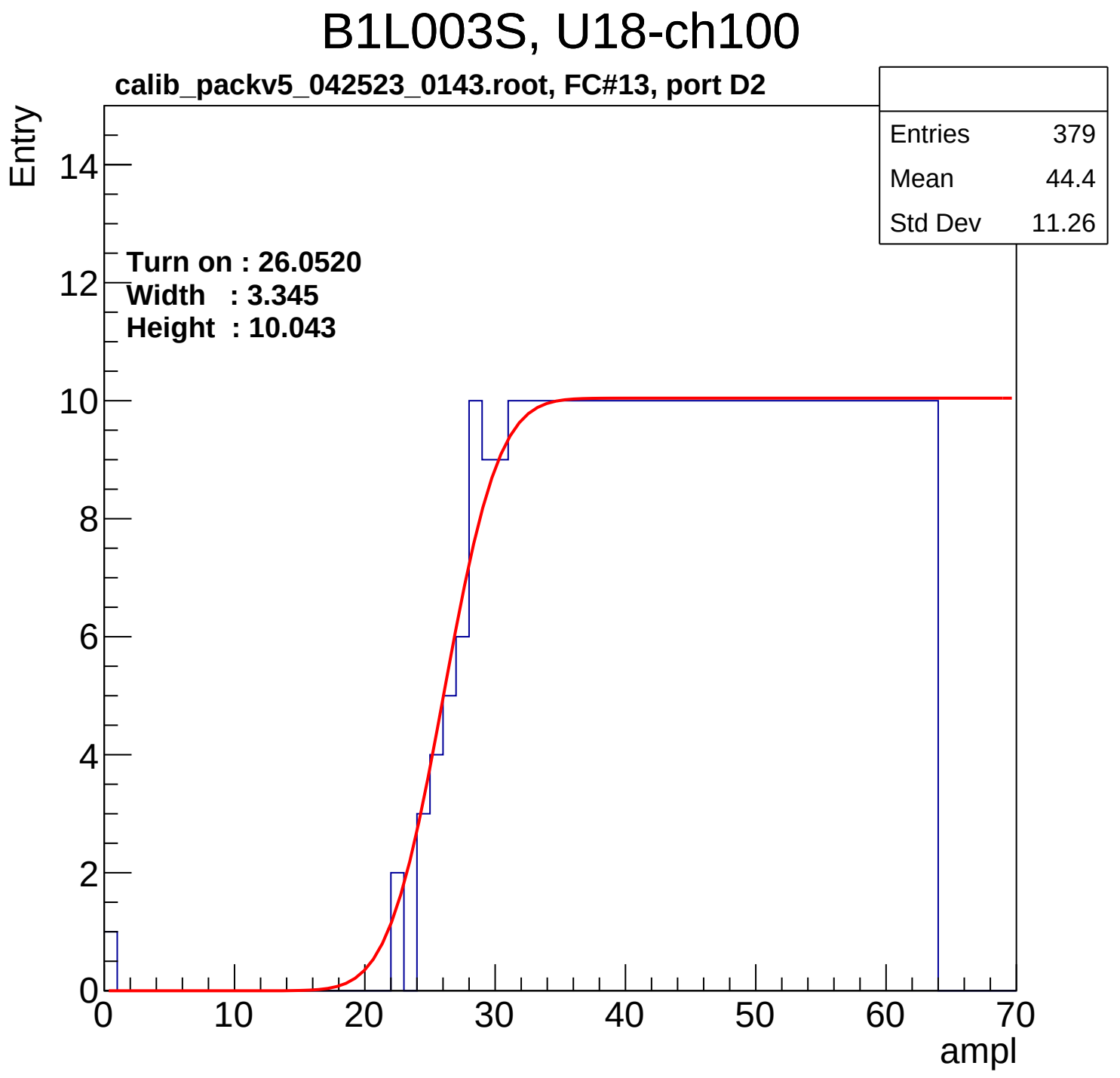
B1L003S, U18-ch100
calib_packv5_042523_0143.root, FC#13, port D2
Entries 379
Mean 44.4
Std Dev 11.26
Turn on : 26.0520
Width : 3.345
Height : 10.043
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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60
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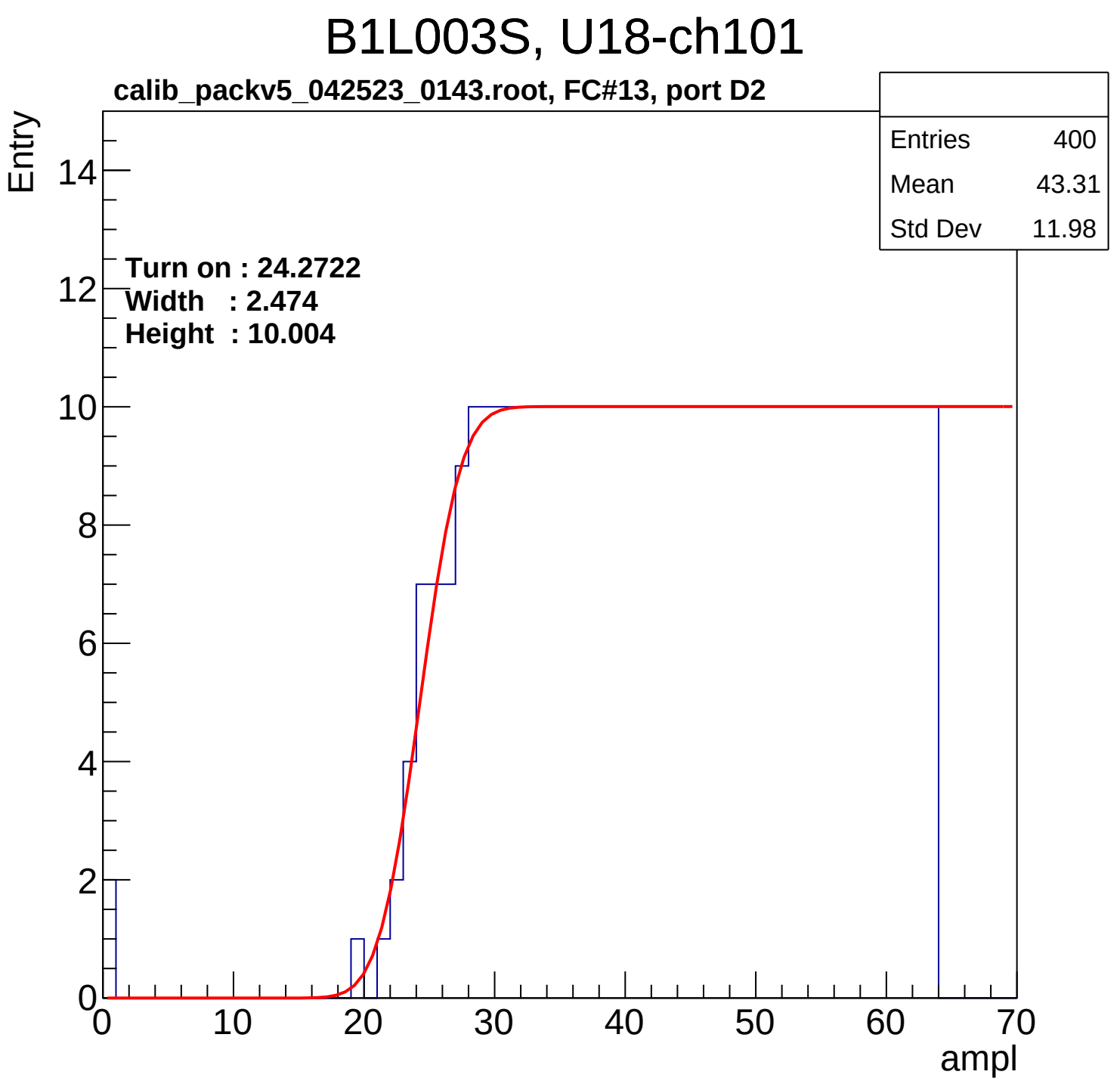
B1L003S, U18-ch101
calib_packv5_042523_0143.root, FC#13, port D2
Entries 400
Mean 43.31
Std Dev 11.98
Turn on : 24.2722
Width : 2.474
Height : 10.004
Entry
ampl
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4
6
8
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12
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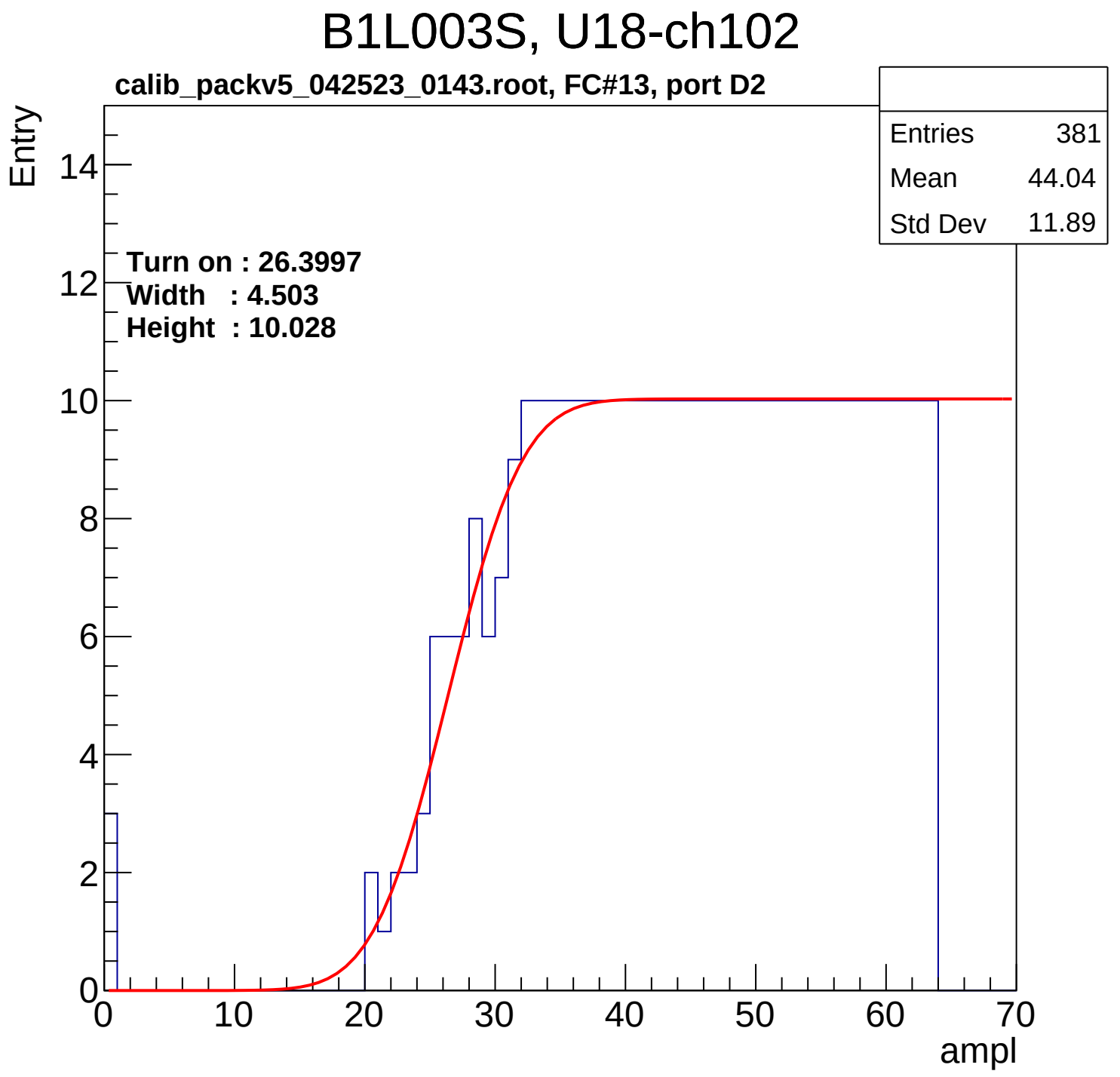
B1L003S, U18-ch102
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 44.04
Std Dev 11.89
Turn on : 26.3997
Width : 4.503
Height : 10.028
Entry
ampl
0
2
4
6
8
10
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0
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60
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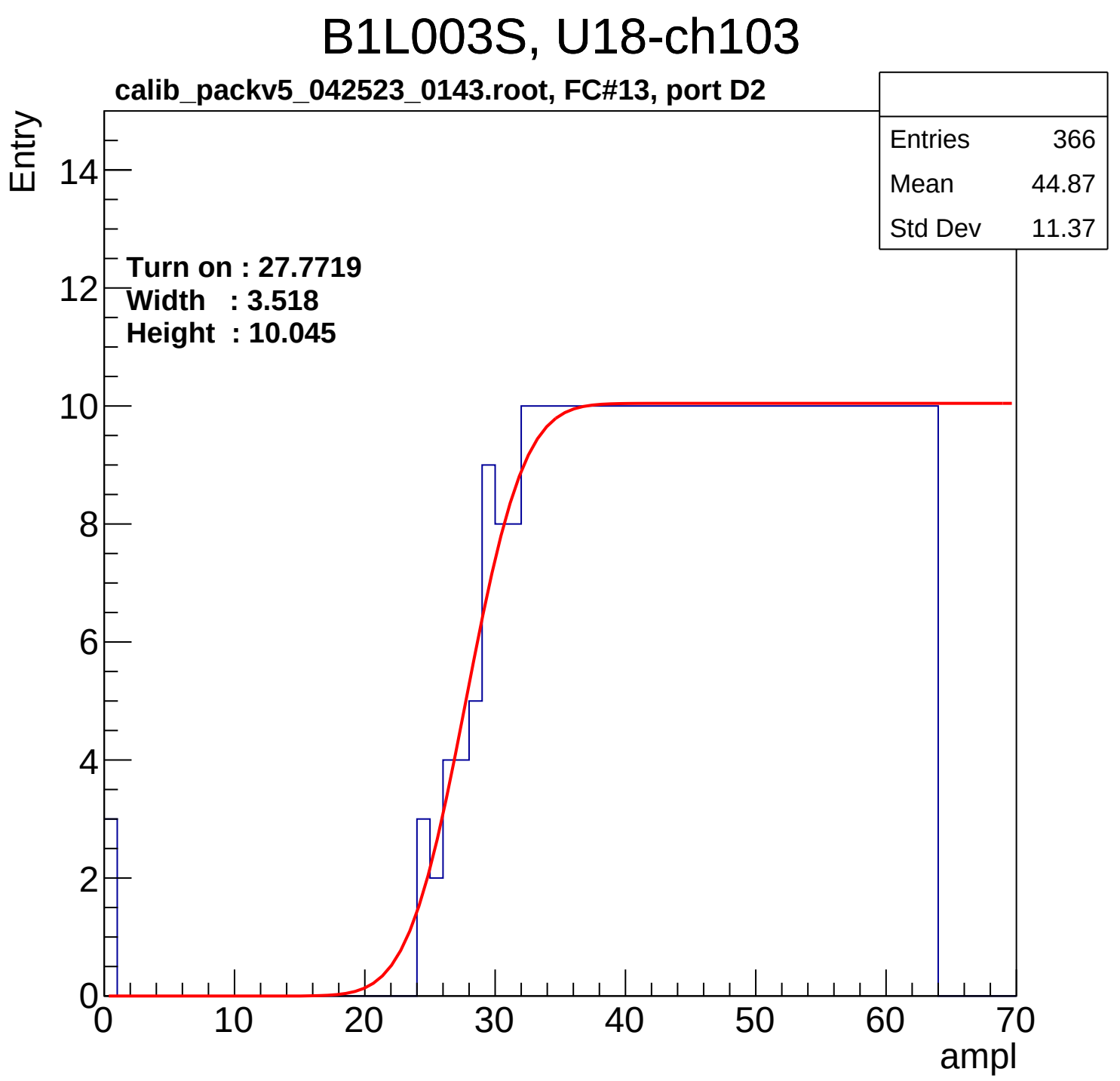
B1L003S, U18-ch103
calib_packv5_042523_0143.root, FC#13, port D2
Entries 366
Mean 44.87
Std Dev 11.37
Turn on : 27.7719
Width : 3.518
Height : 10.045
Entry
ampl
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4
6
8
10
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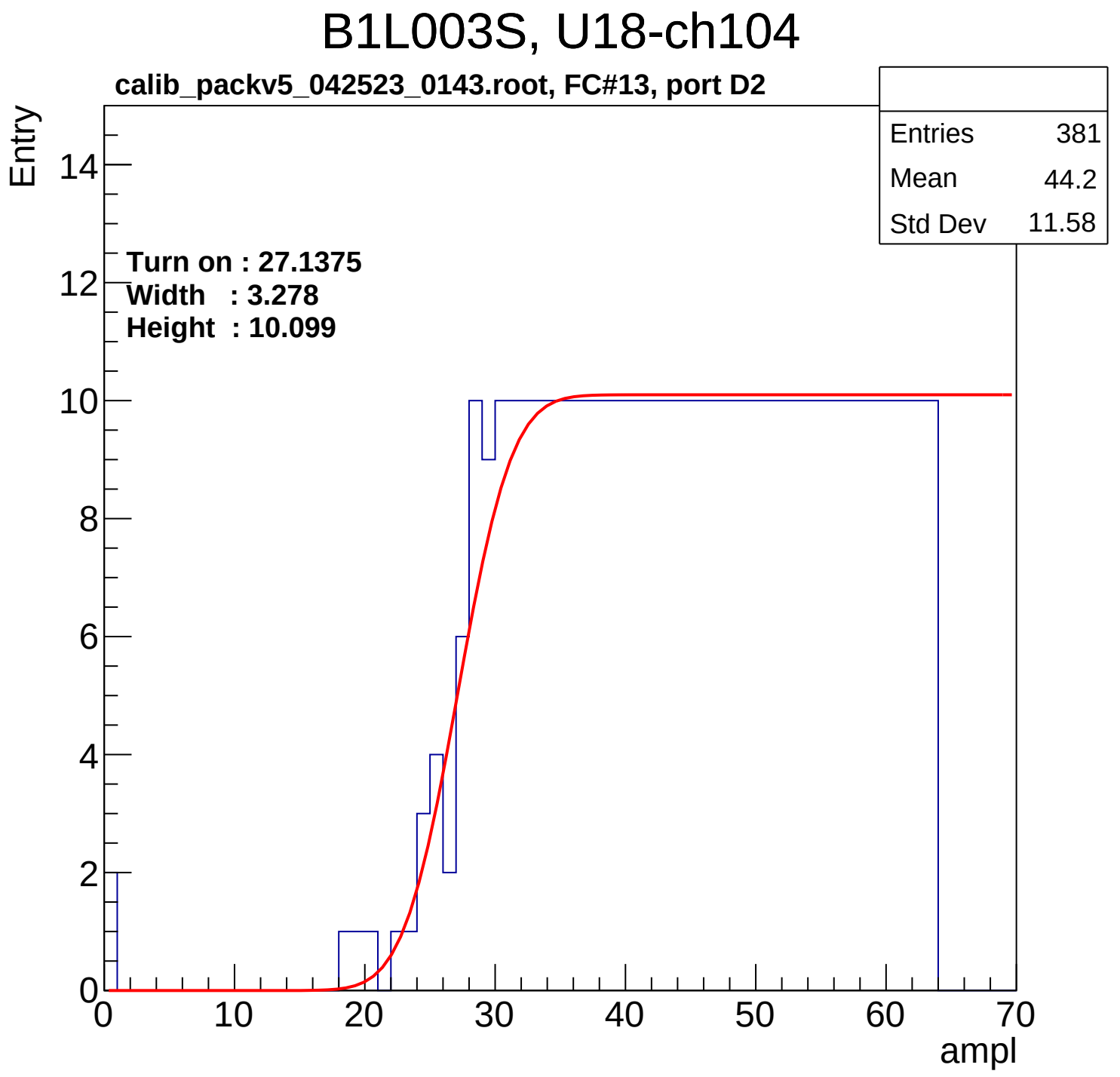
B1L003S, U18-ch104
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 44.2
Std Dev 11.58
Turn on : 27.1375
Width : 3.278
Height : 10.099
Entry
ampl
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2
4
6
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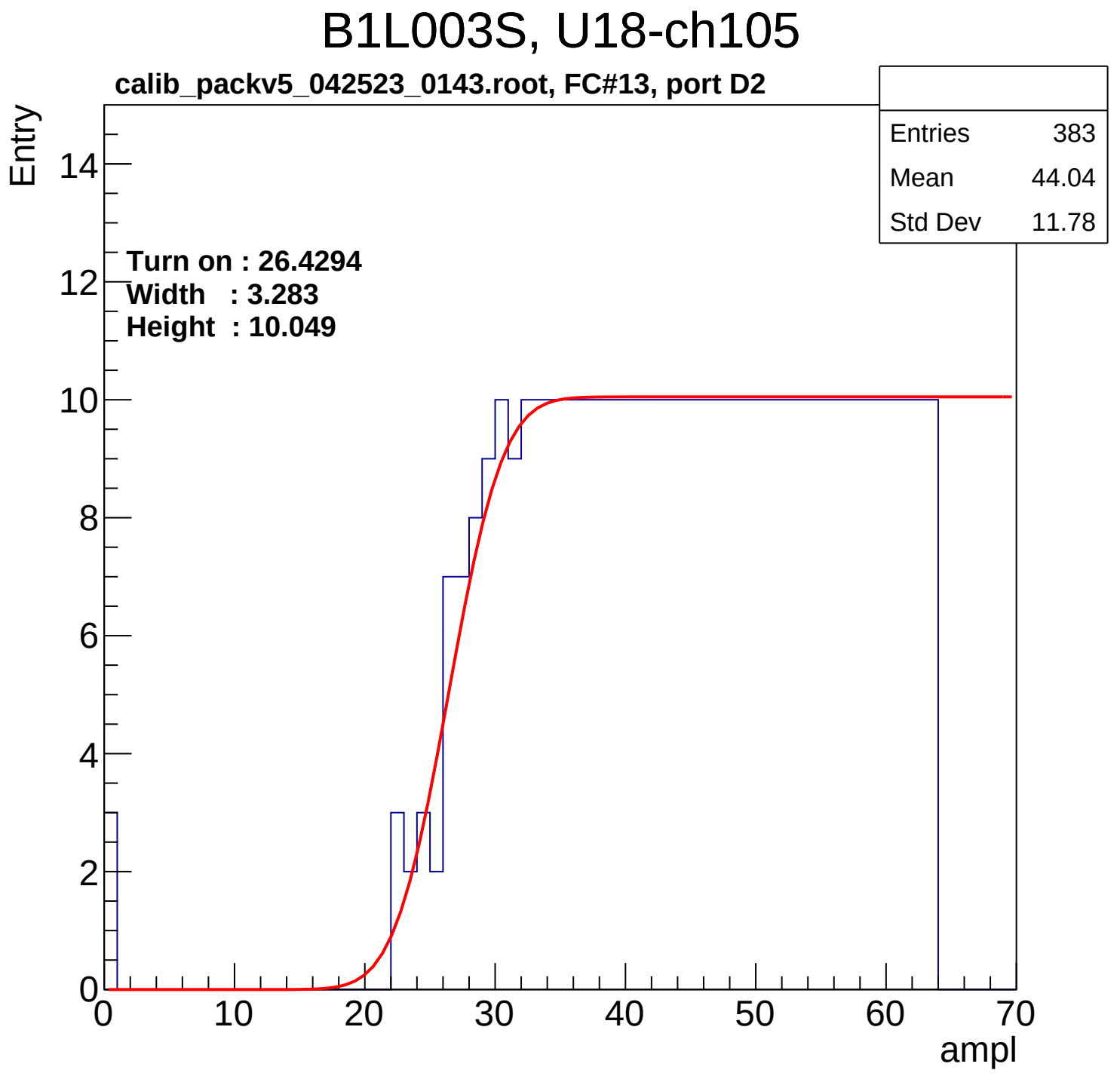
B1L003S, U18-ch105
calib_packv5_042523_0143.root, FC#13, port D2
Entries 383
Mean 44.04
Std Dev 11.78
Turn on : 26.4294
Width : 3.283
Height : 10.049
Entry
ampl
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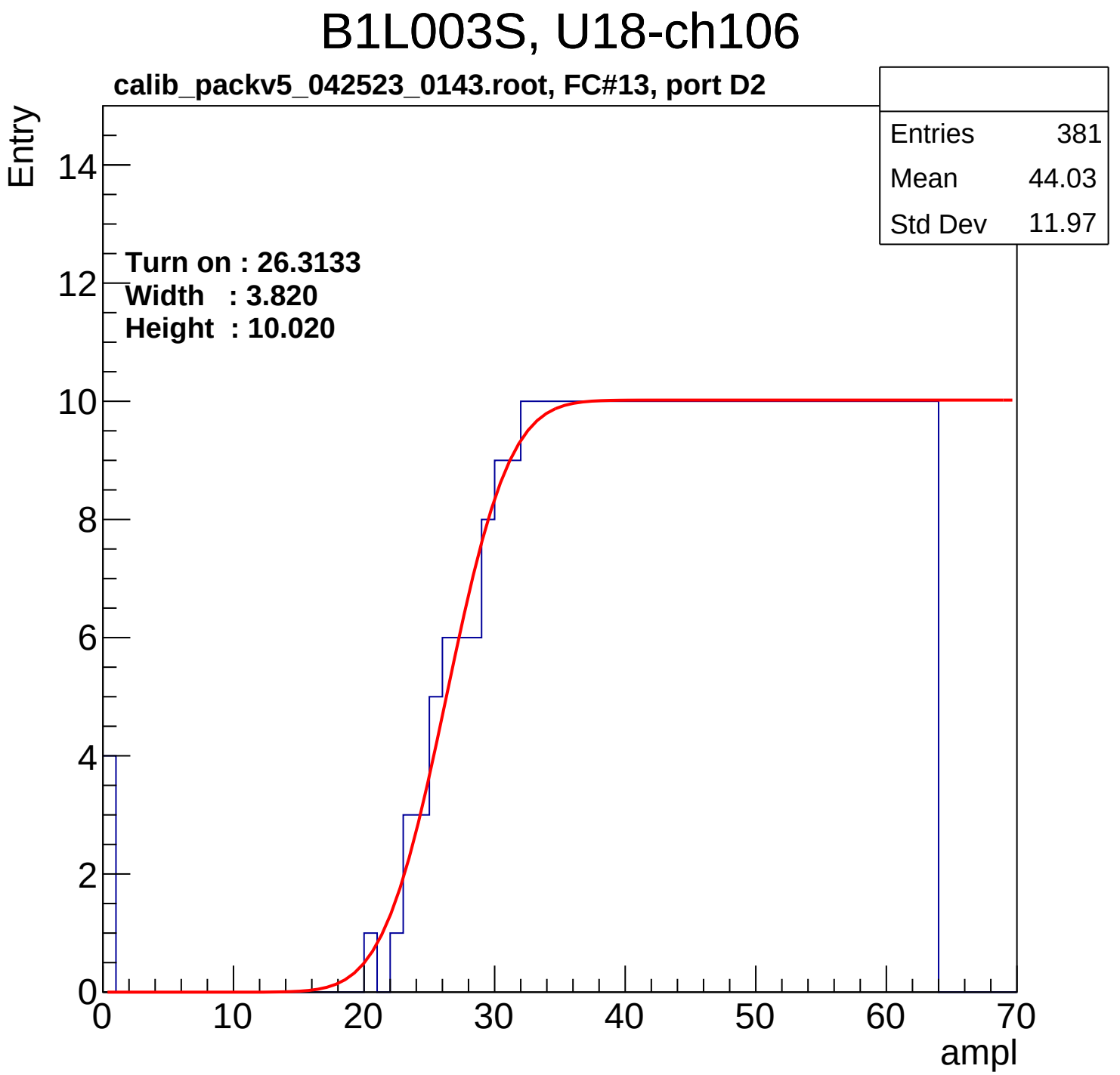
B1L003S, U18-ch106
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 44.03
Std Dev 11.97
Turn on : 26.3133
Width : 3.820
Height : 10.020
Entry
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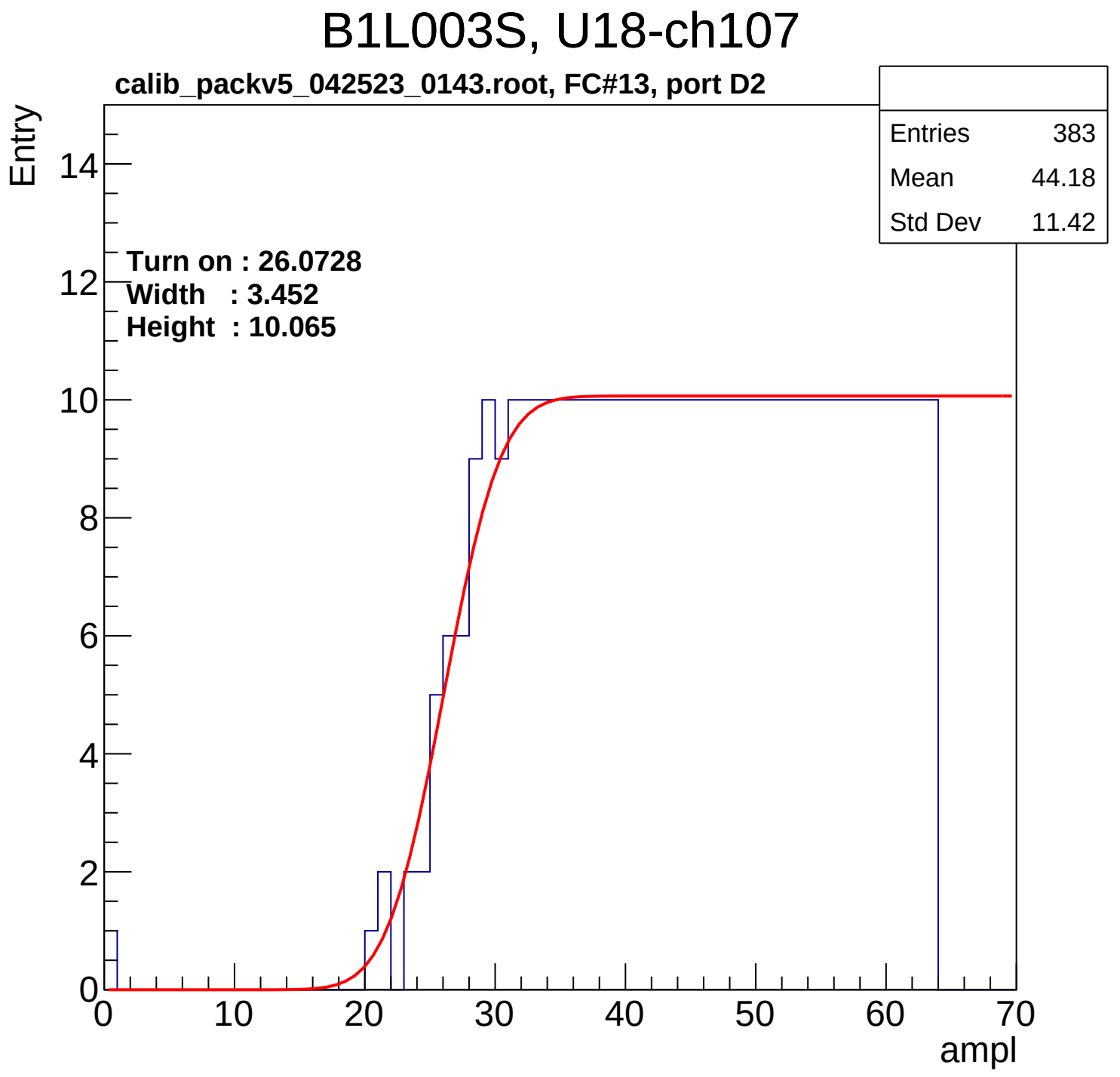
B1L003S, U18-ch107
calib_packv5_042523_0143.root, FC#13, port D2
Entries 383
Mean 44.18
Std Dev 11.42
Turn on : 26.0728
Width : 3.452
Height : 10.065
Entry
ampl
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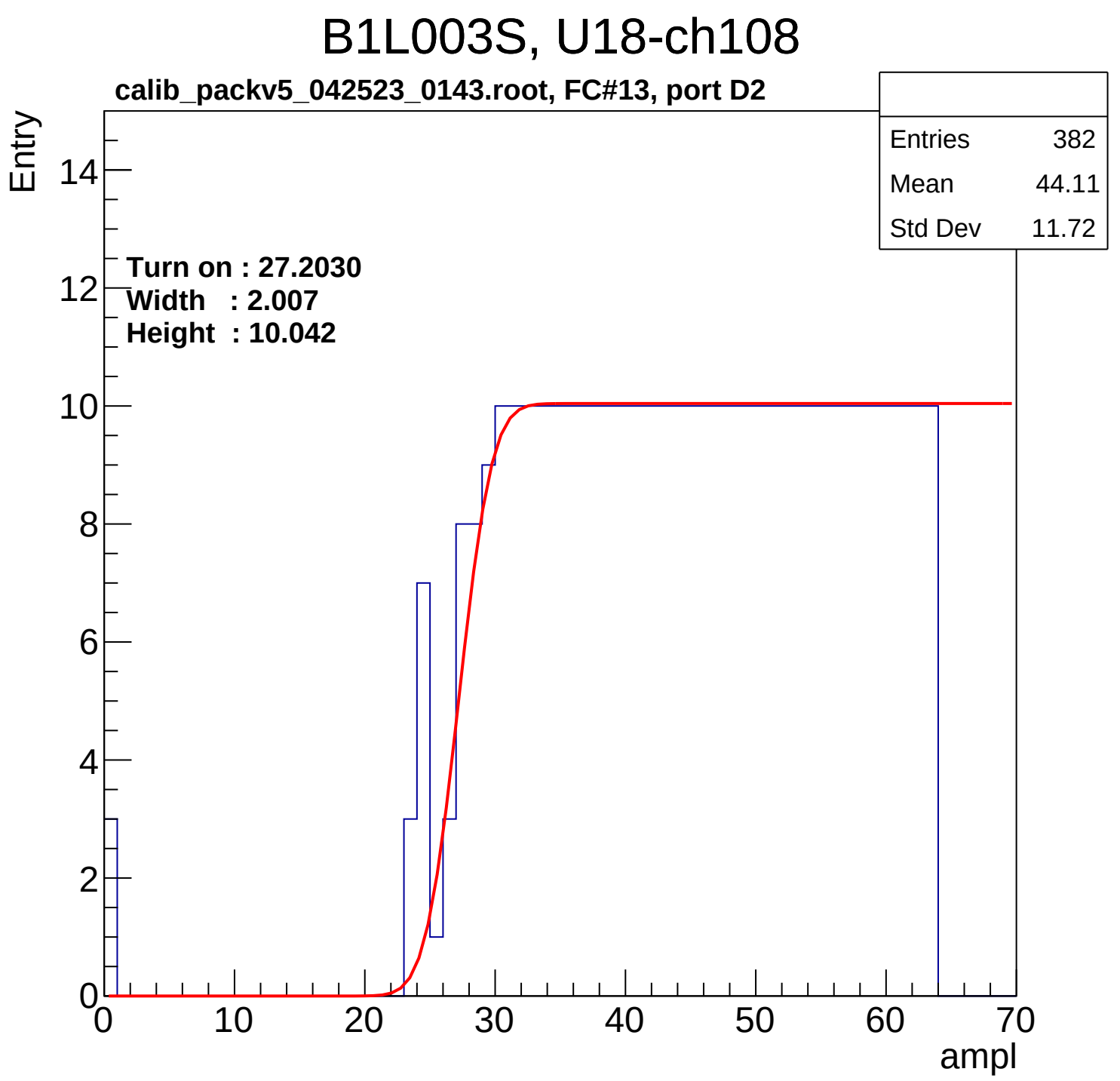
B1L003S, U18-ch108
calib_packv5_042523_0143.root, FC#13, port D2
Entries 382
Mean 44.11
Std Dev 11.72
Turn on : 27.2030
Width : 2.007
Height : 10.042
Entry
ampl
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2
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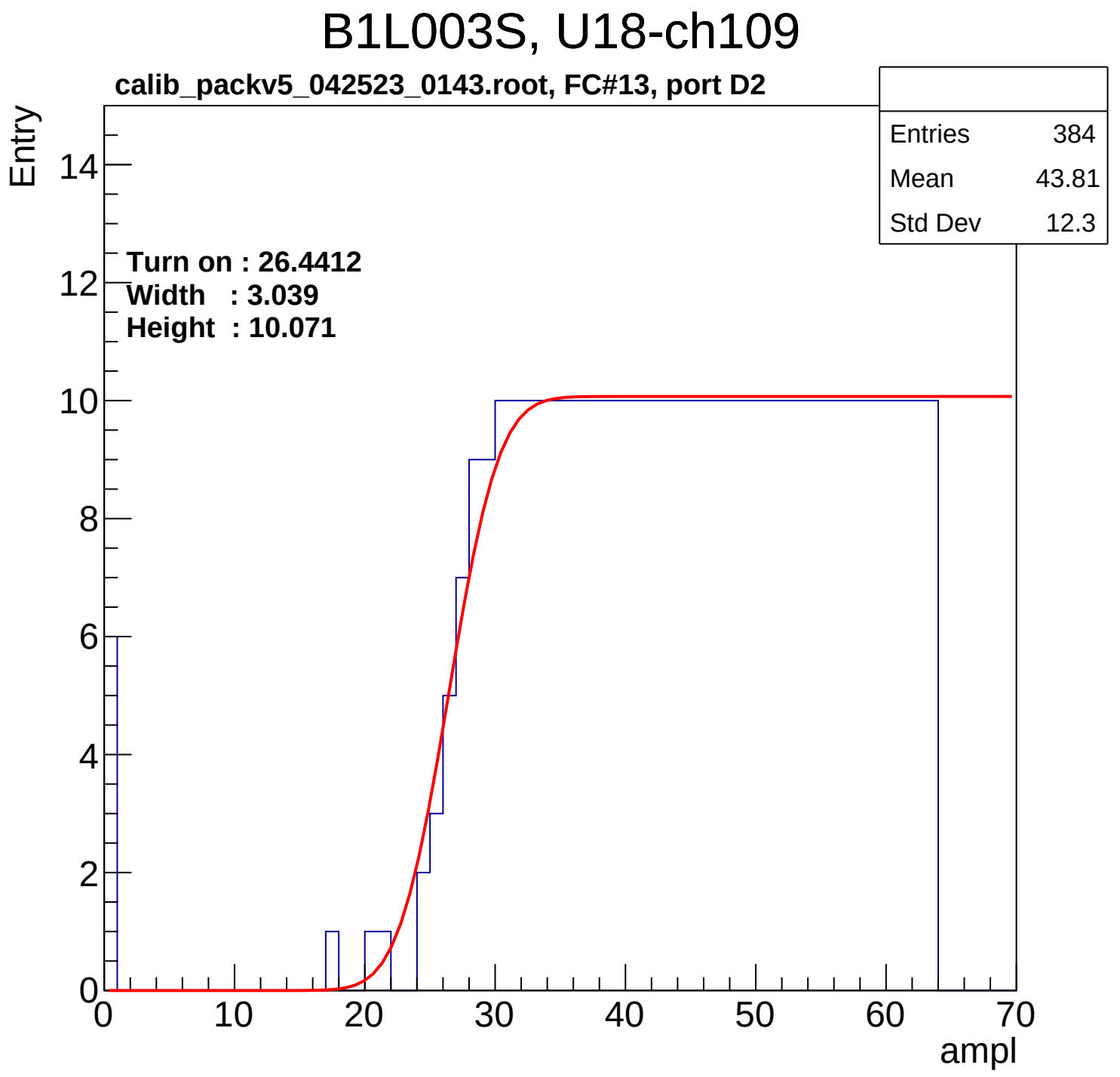
B1L003S, U18-ch109
calib_packv5_042523_0143.root, FC#13, port D2
Entries 384
Mean 43.81
Std Dev 12.3
Turn on : 26.4412
Width : 3.039
Height : 10.071
Entry
ampl
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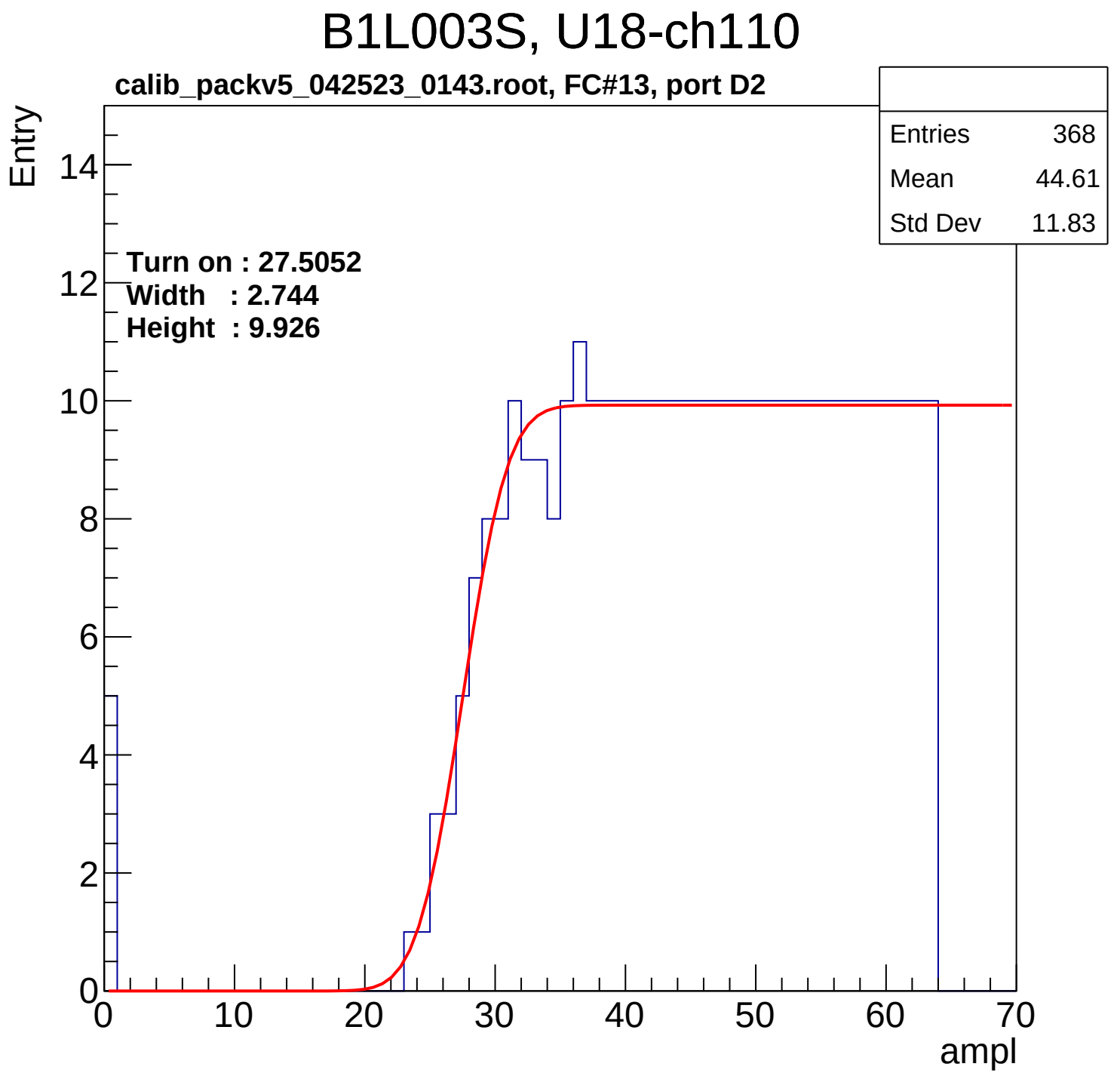
B1L003S, U18-ch110
calib_packv5_042523_0143.root, FC#13, port D2
Entries 368
Mean 44.61
Std Dev 11.83
Turn on : 27.5052
Width : 2.744
Height : 9.926
Entry
ampl
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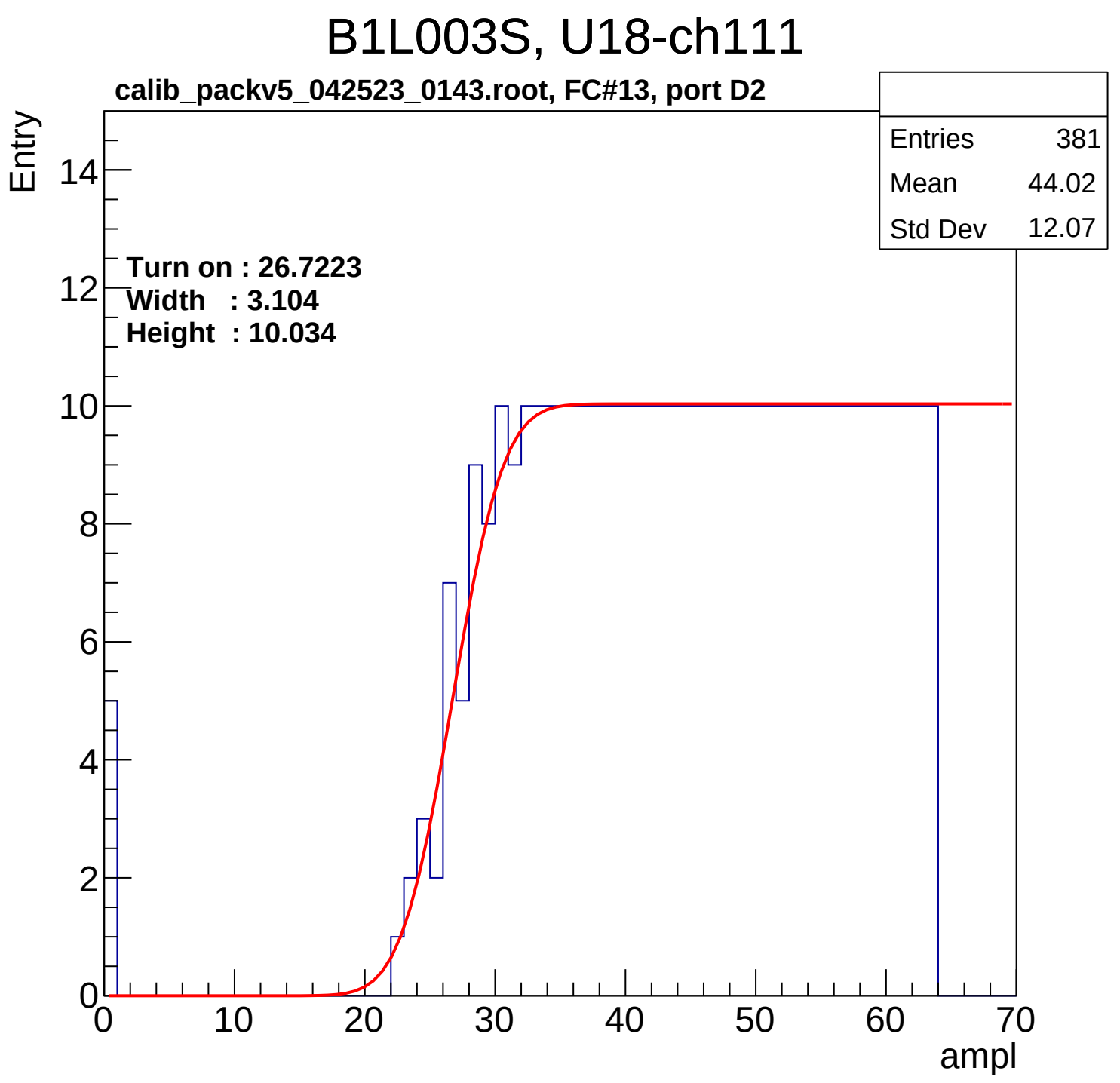
B1L003S, U18-ch111
calib_packv5_042523_0143.root, FC#13, port D2
Entries 381
Mean 44.02
Std Dev 12.07
Turn on : 26.7223
Width : 3.104
Height : 10.034
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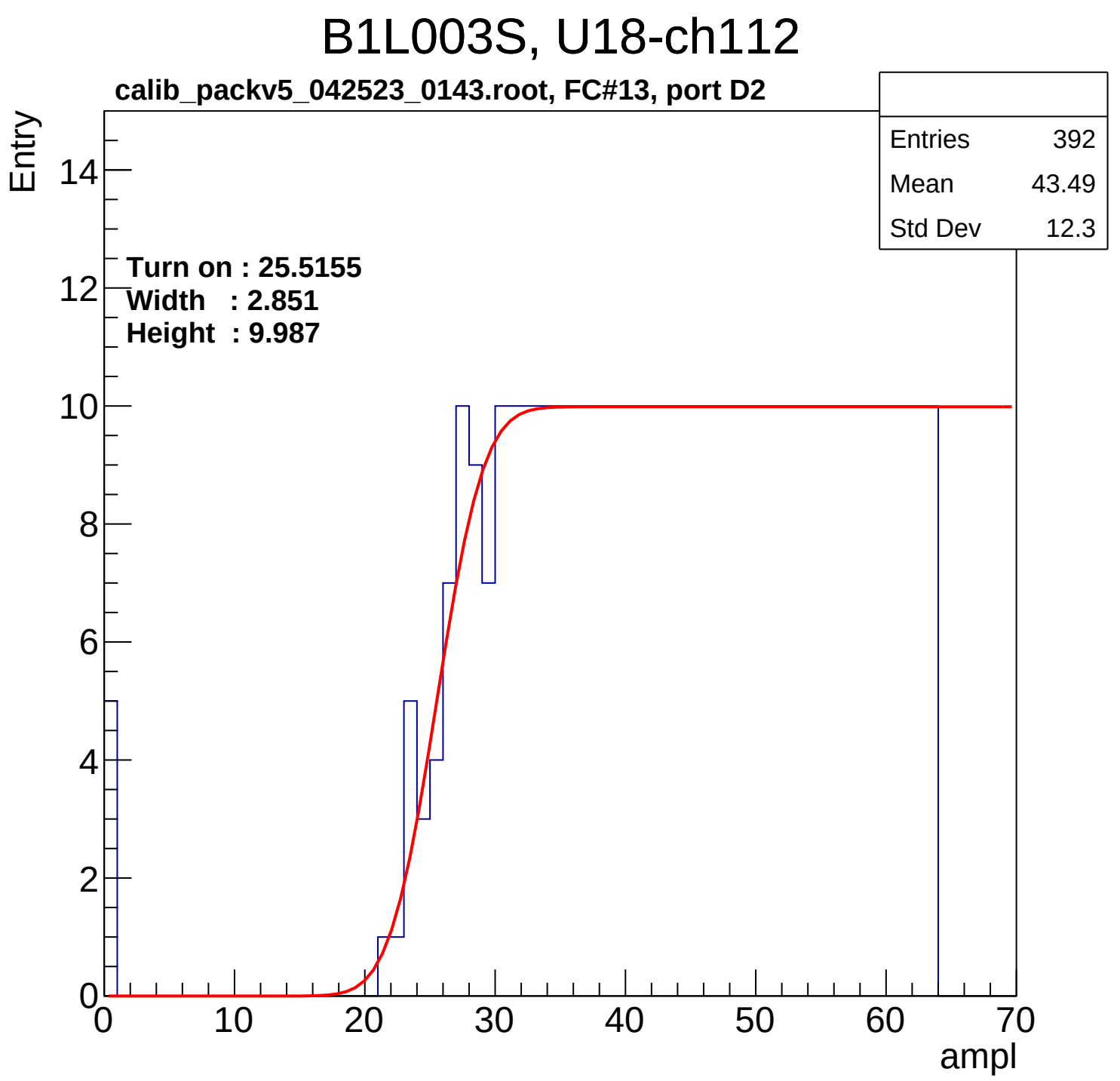
B1L003S, U18-ch112
calib_packv5_042523_0143.root, FC#13, port D2
Entries 392
Mean 43.49
Std Dev 12.3
Turn on : 25.5155
Width : 2.851
Height : 9.987
Entry
ampl
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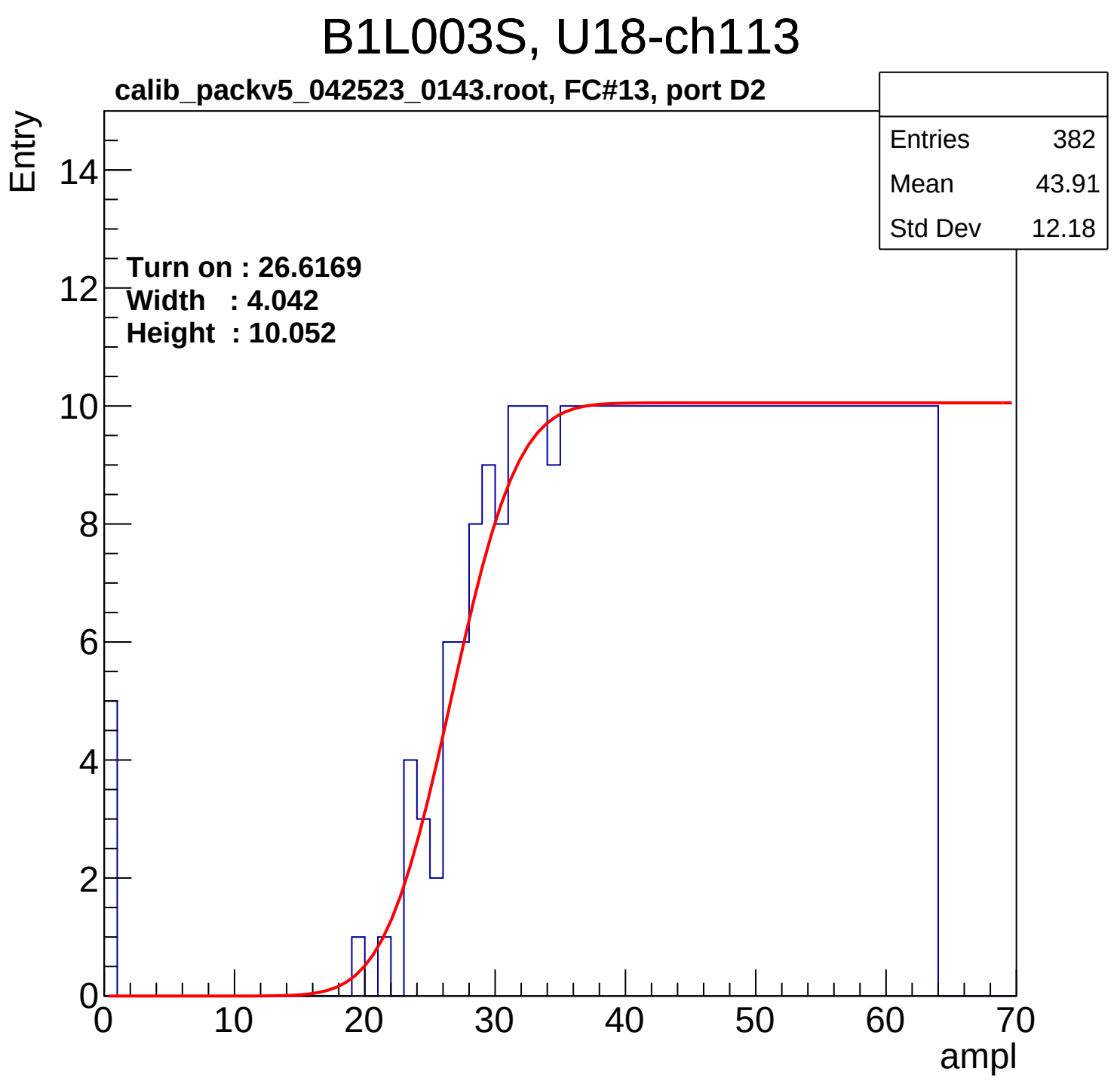
B1L003S, U18-ch113
calib_packv5_042523_0143.root, FC#13, port D2
Entries 382
Mean 43.91
Std Dev 12.18
Turn on : 26.6169
Width : 4.042
Height : 10.052
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ampl
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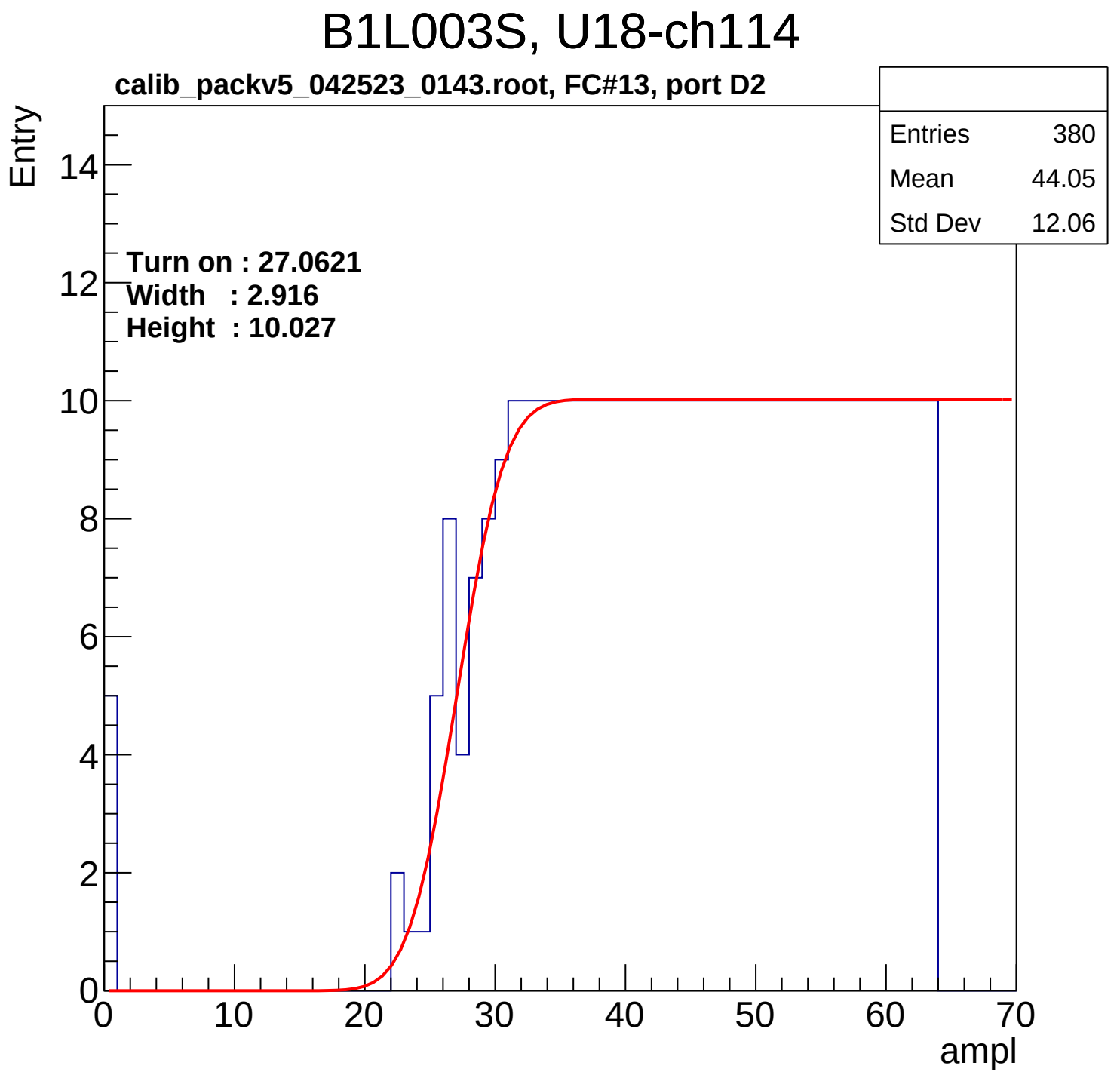
B1L003S, U18-ch114
calib_packv5_042523_0143.root, FC#13, port D2
Entries 380
Mean 44.05
Std Dev 12.06
Turn on : 27.0621
Width : 2.916
Height : 10.027
Entry
ampl
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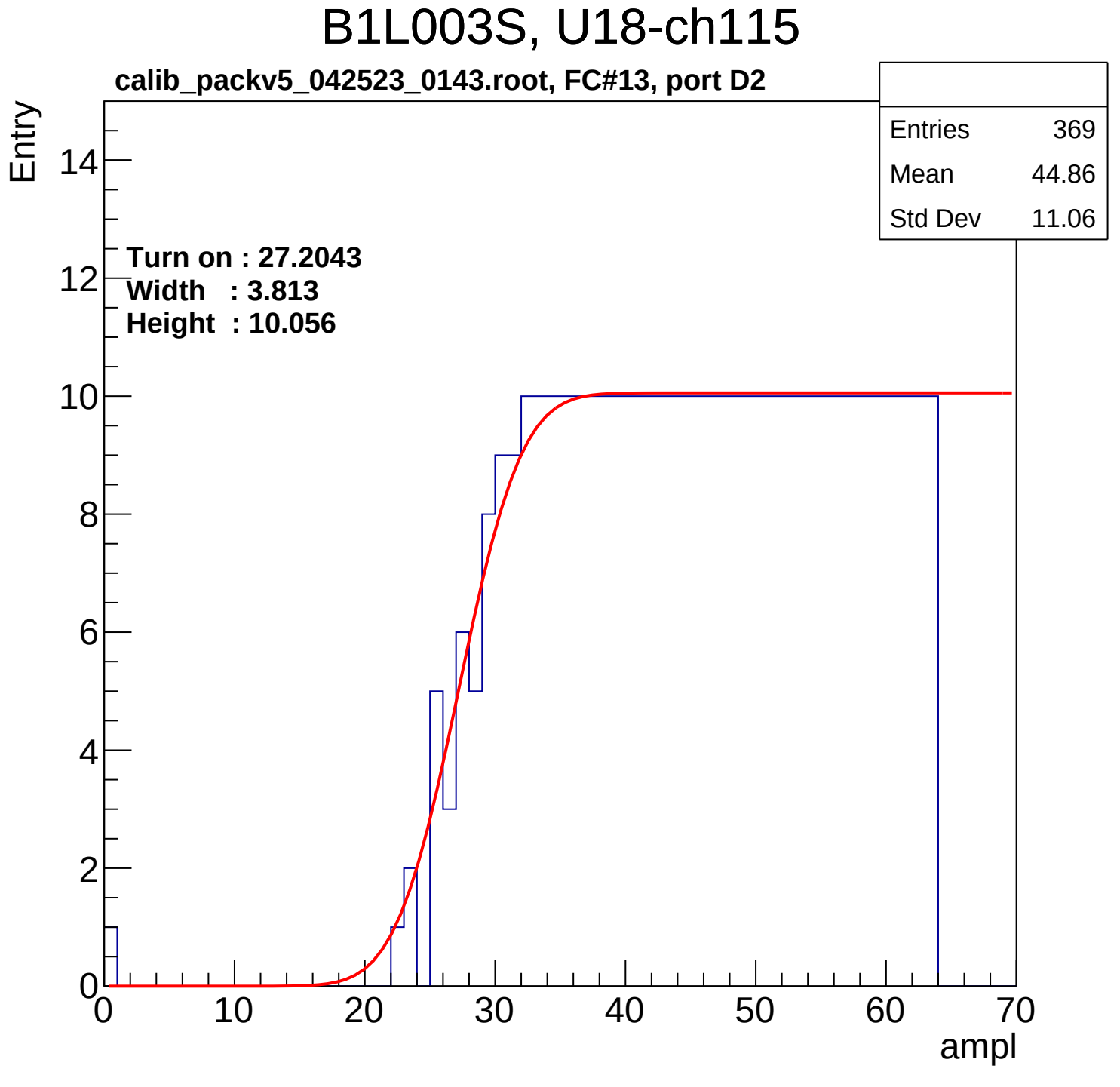
B1L003S, U18-ch115
calib_packv5_042523_0143.root, FC#13, port D2
Entries 369
Mean 44.86
Std Dev 11.06
Turn on : 27.2043
Width : 3.813
Height : 10.056
Entry
ampl
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4
6
8
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12
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20
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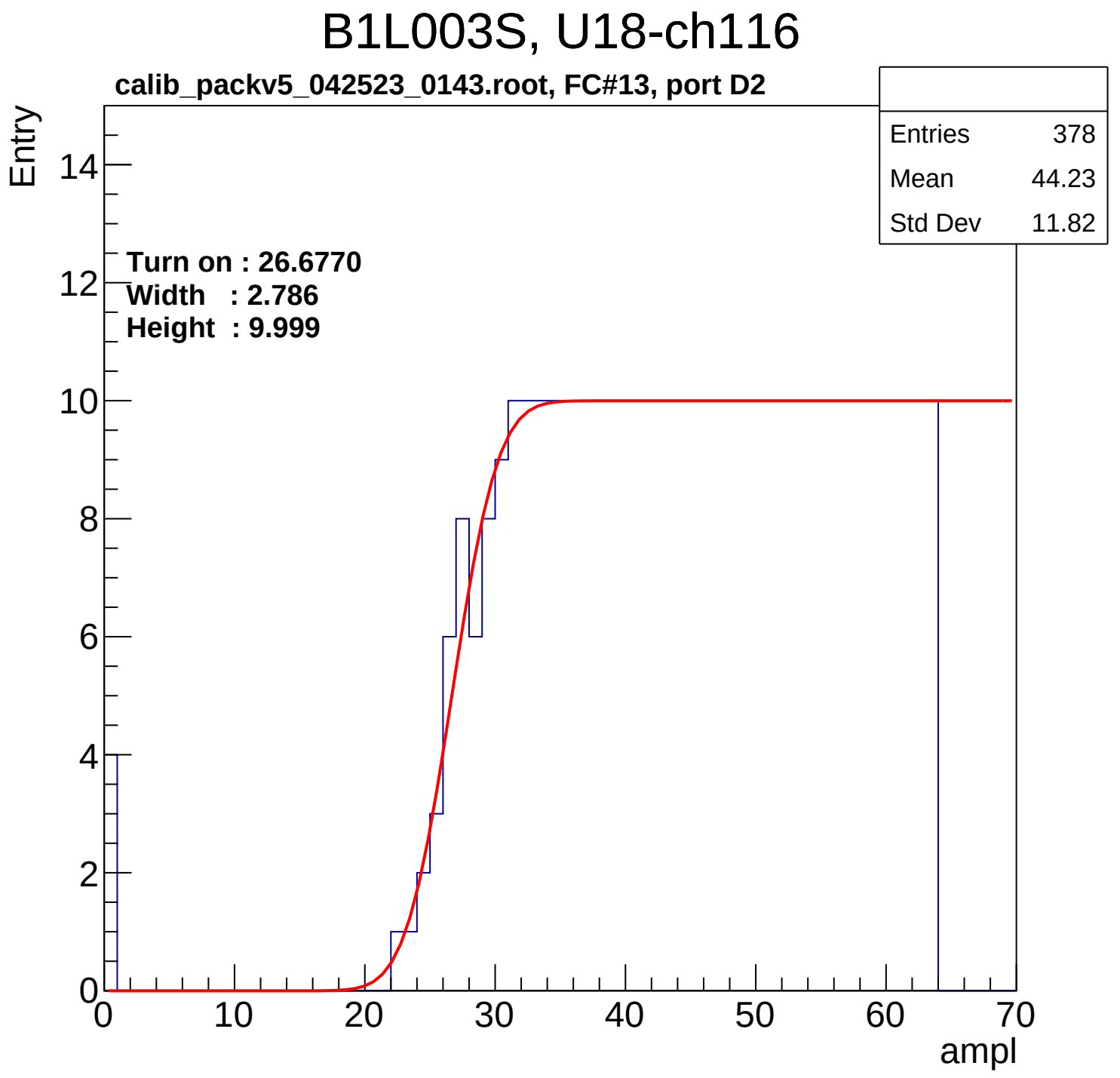
B1L003S, U18-ch116
calib_packv5_042523_0143.root, FC#13, port D2
Entries 378
Mean 44.23
Std Dev 11.82
Turn on : 26.6770
Width : 2.786
Height : 9.999
Entry
ampl
0
2
4
6
8
10
12
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0
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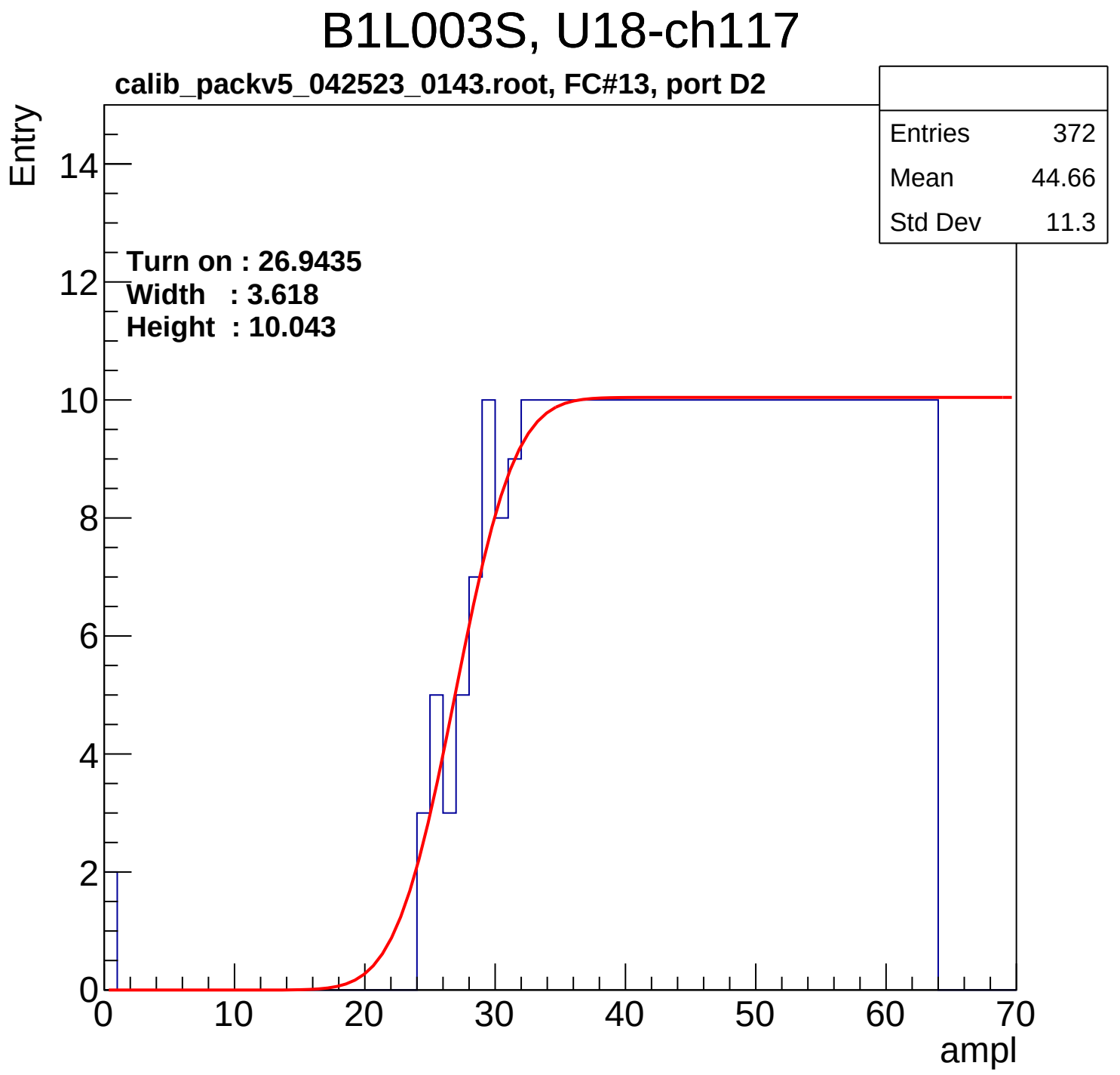
B1L003S, U18-ch117
calib_packv5_042523_0143.root, FC#13, port D2
Entries 372
Mean 44.66
Std Dev 11.3
Turn on : 26.9435
Width : 3.618
Height : 10.043
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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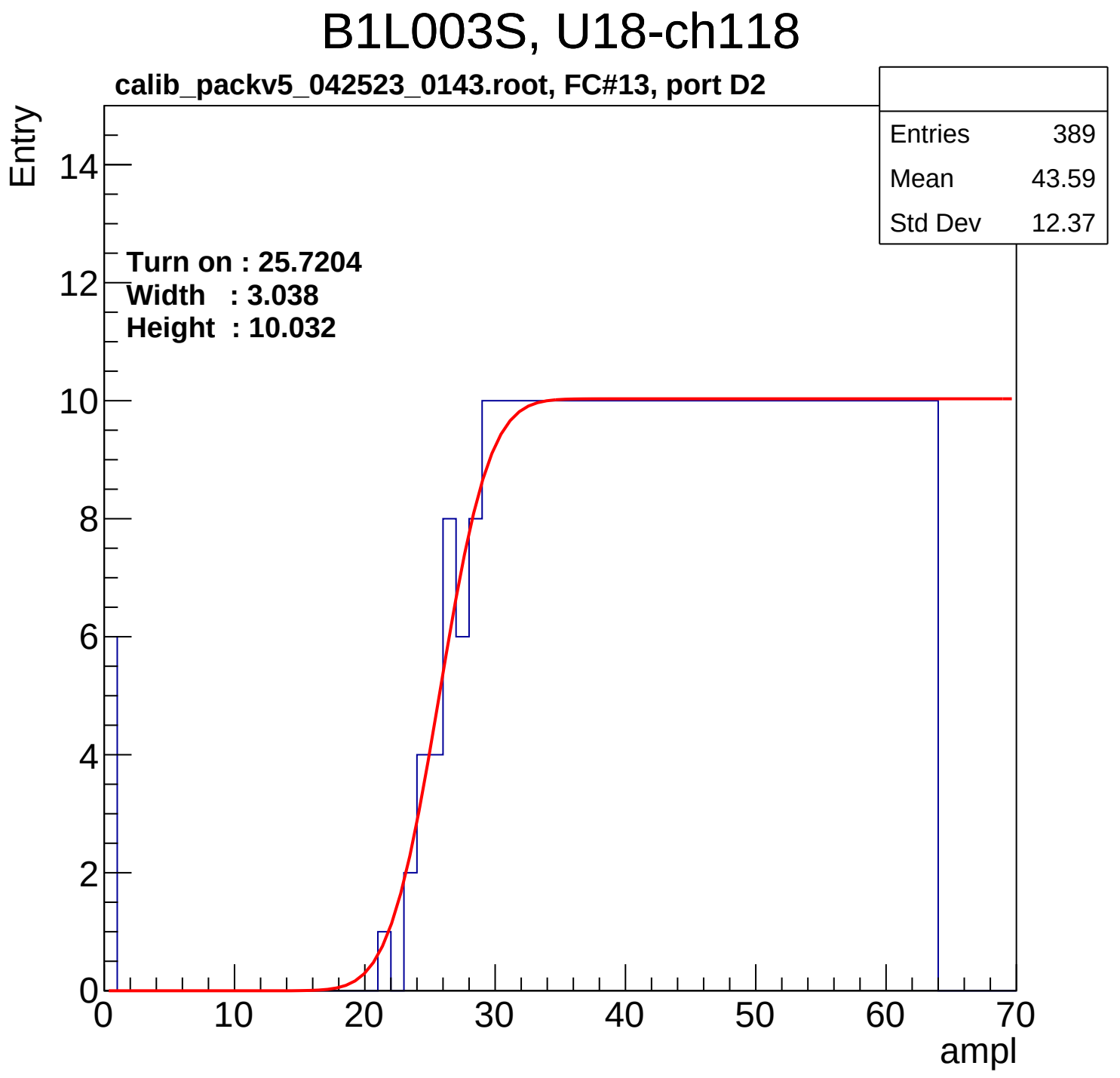
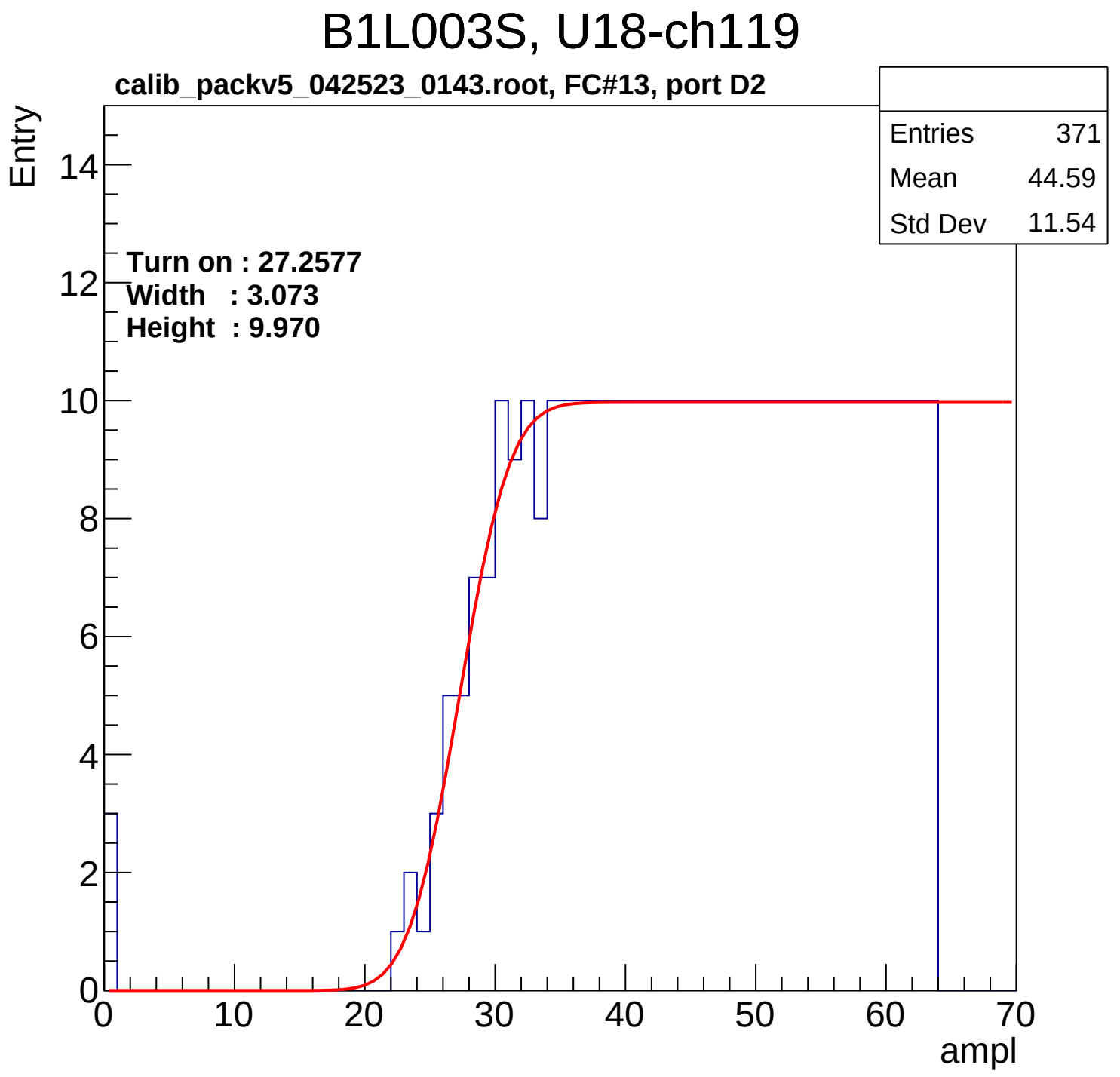
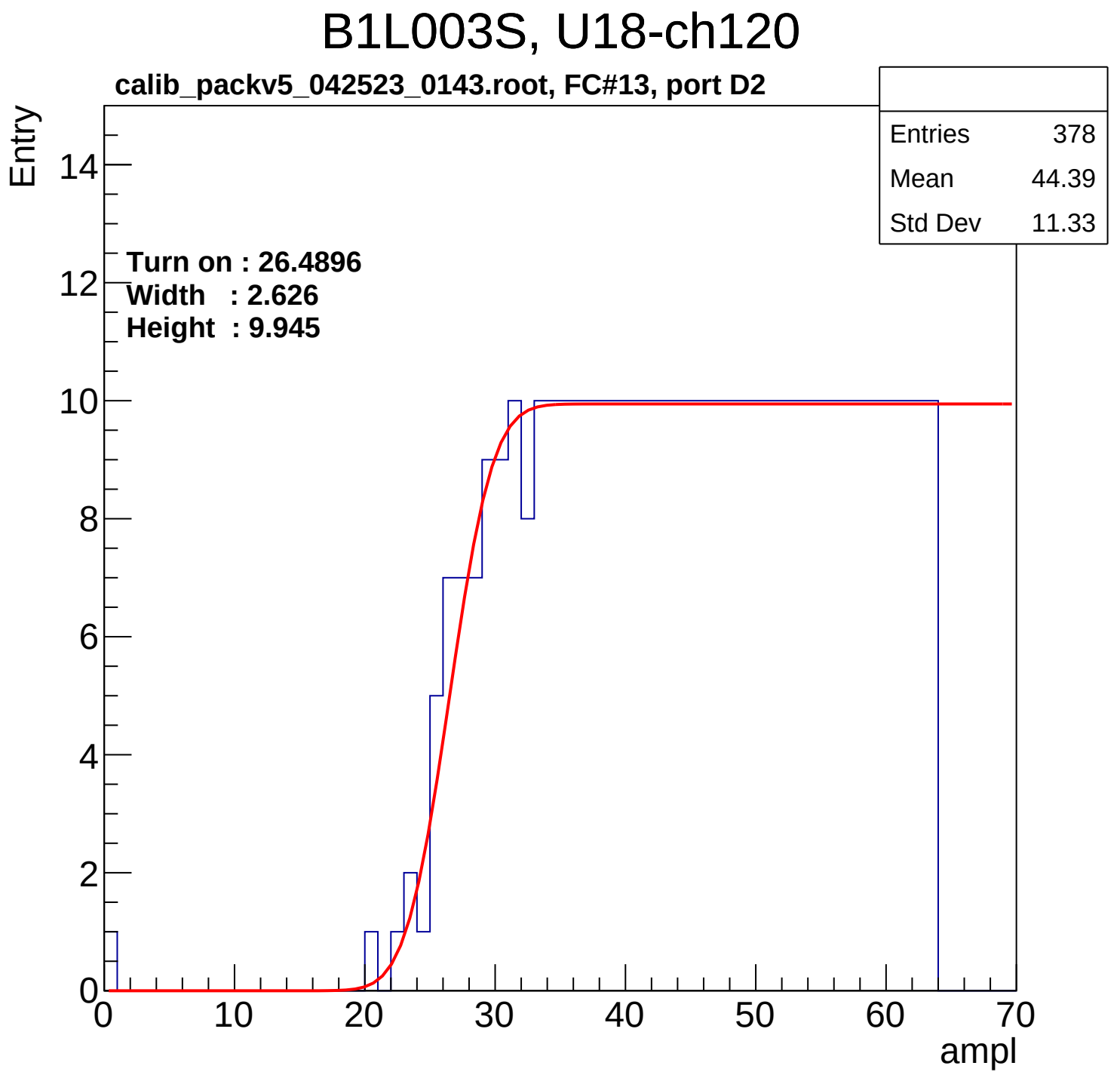
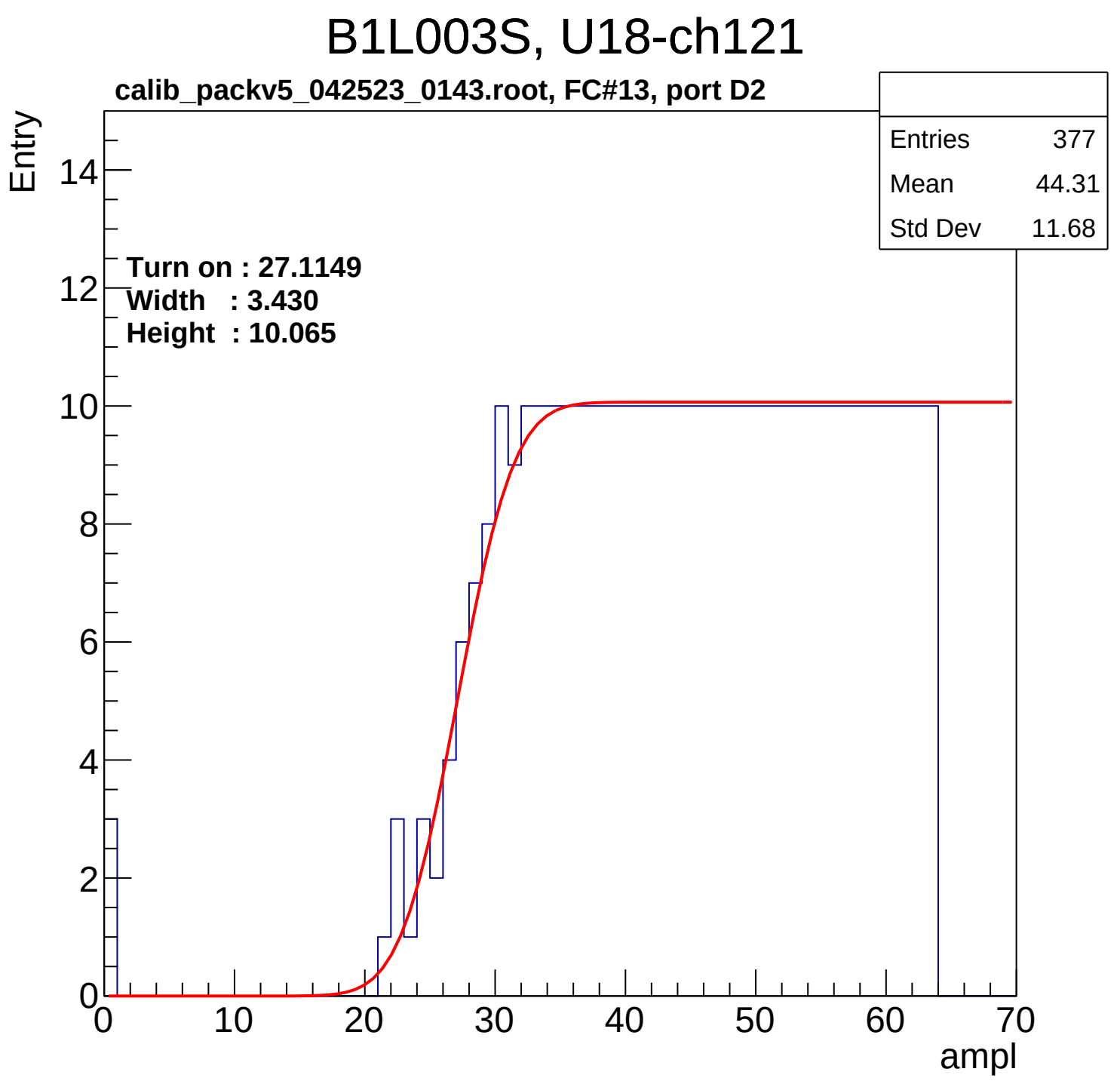
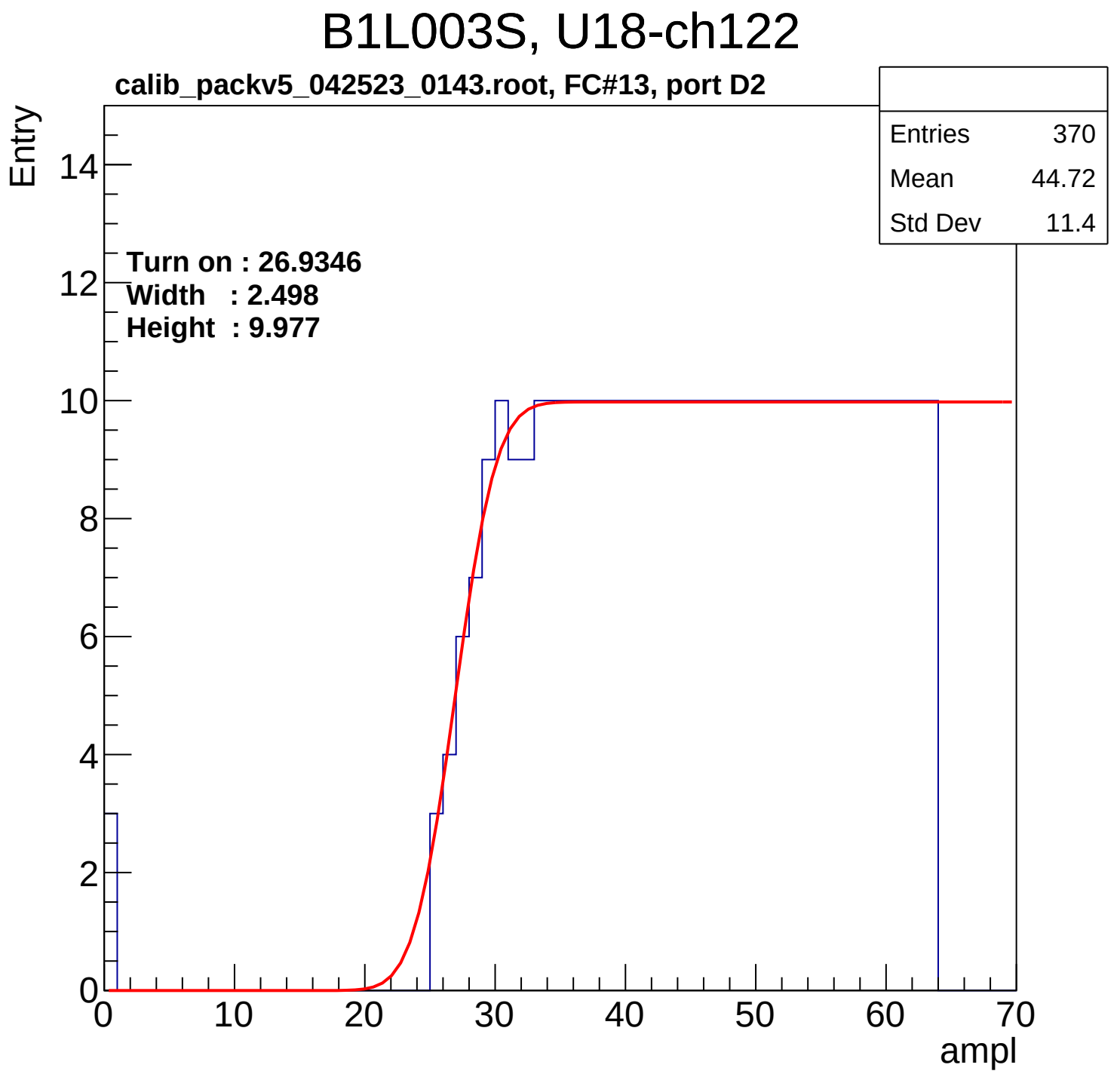
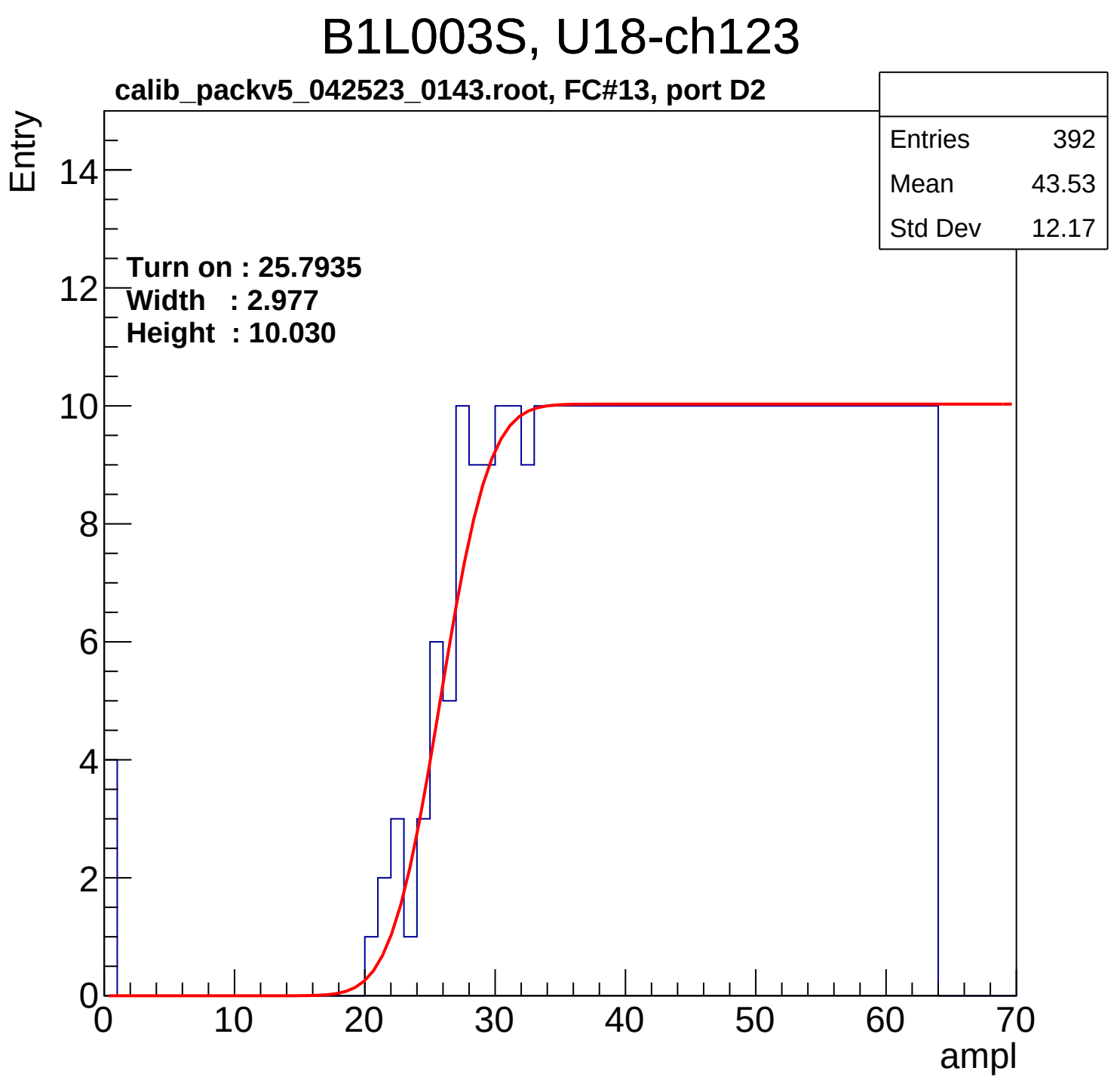

B1L003S, U18-ch118
calib_packv5_042523_0143.root, FC#13, port D2
Entries 389
Mean 43.59
Std Dev 12.37
Turn on : 25.7204
Width : 3.038
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

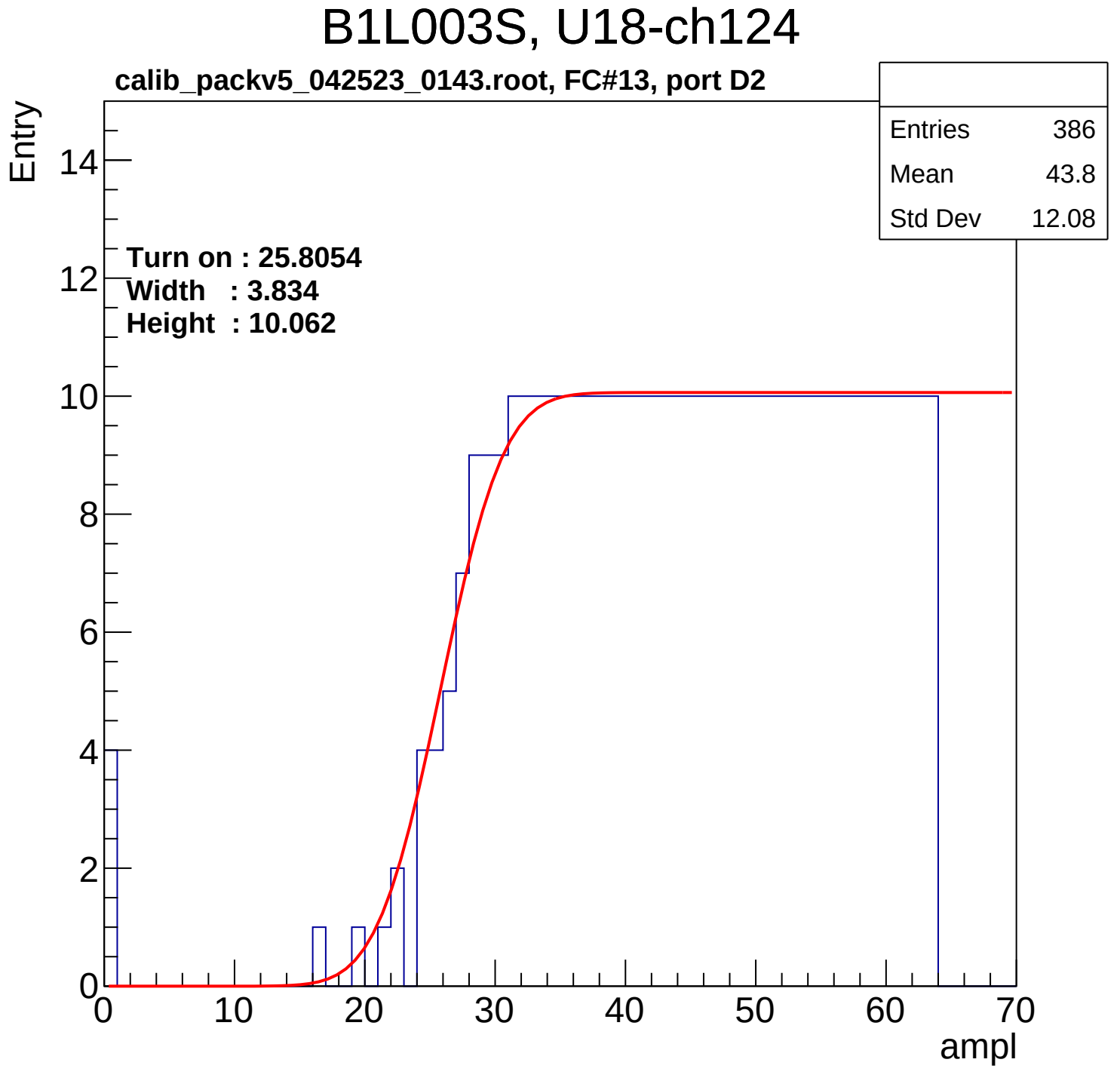

B1L003S, U18-ch119
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.59
Std Dev 11.54
Turn on : 27.2577
Width : 3.073
Height : 9.970
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

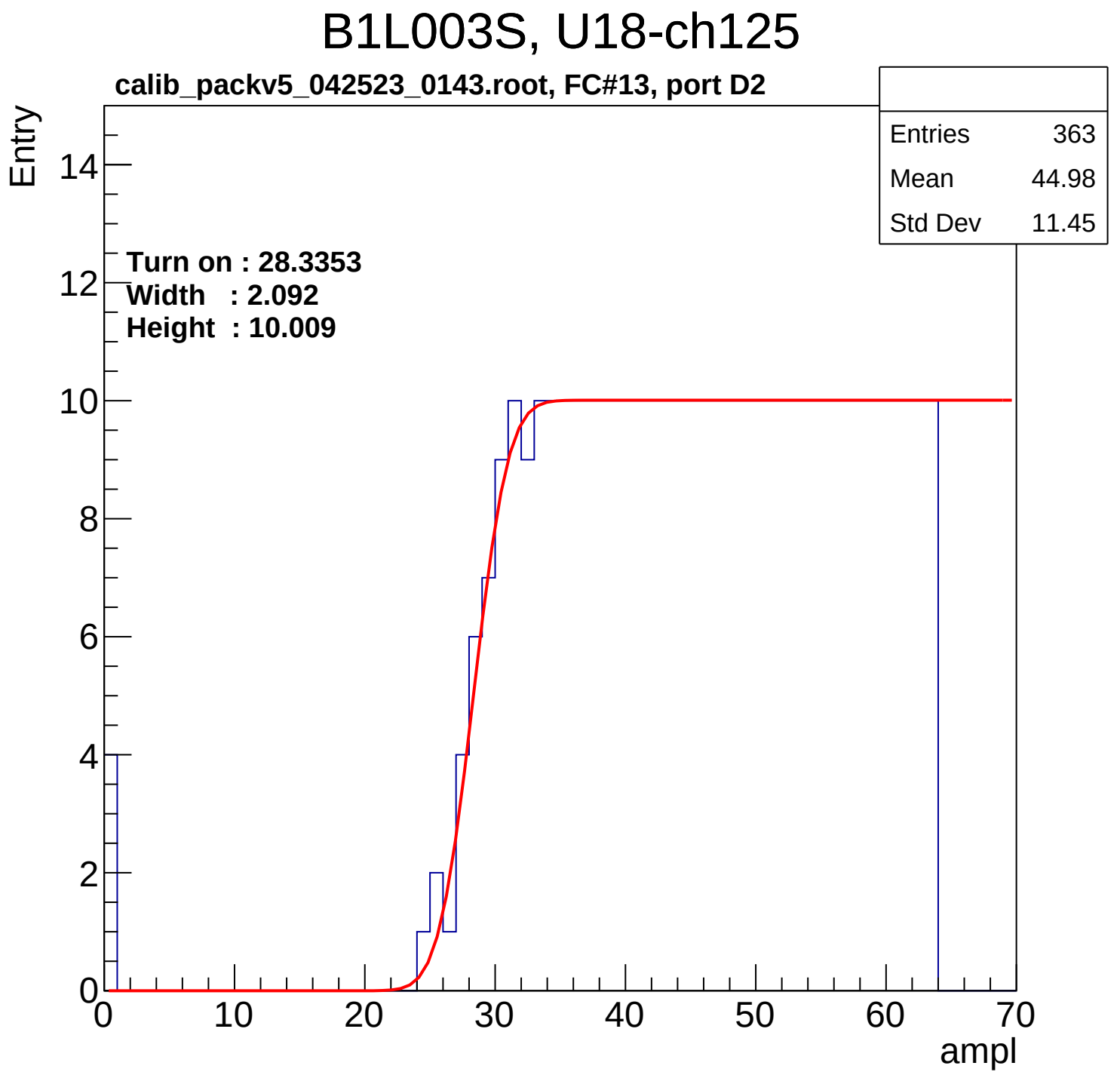

B1L003S, U18-ch120
calib_packv5_042523_0143.root, FC#13, port D2
Entries 378
Mean 44.39
Std Dev 11.33
Turn on : 26.4896
Width : 2.626
Height : 9.945
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

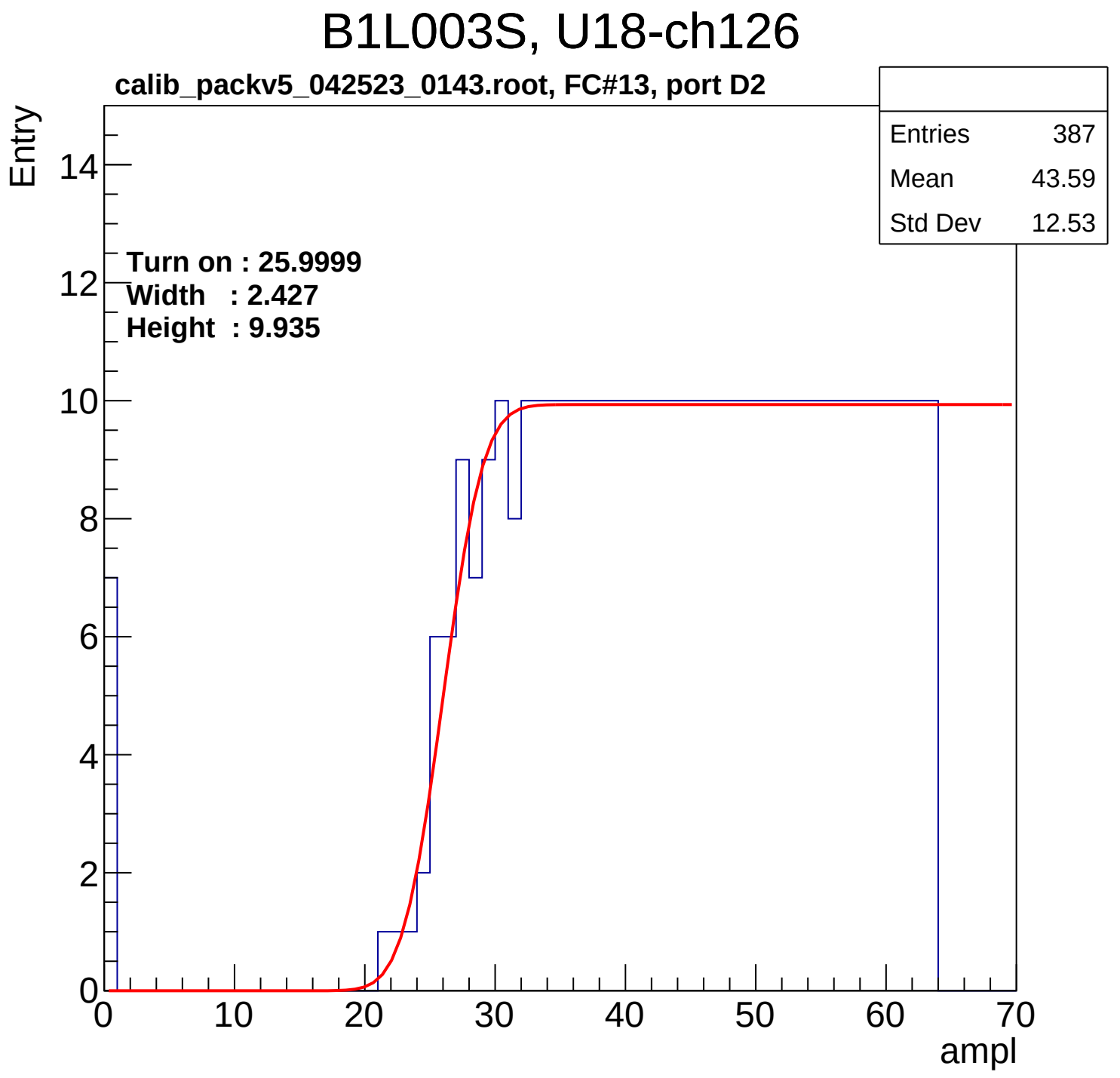

B1L003S, U18-ch121
calib_packv5_042523_0143.root, FC#13, port D2
Entries 377
Mean 44.31
Std Dev 11.68
Turn on : 27.1149
Width : 3.430
Height : 10.065
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U18-ch122
calib_packv5_042523_0143.root, FC#13, port D2
Entries 370
Mean 44.72
Std Dev 11.4
Turn on : 26.9346
Width : 2.498
Height : 9.977
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U18-ch123
calib_packv5_042523_0143.root, FC#13, port D2
Entries 392
Mean 43.53
Std Dev 12.17
Turn on : 25.7935
Width : 2.977
Height : 10.030
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U18-ch124
calib_packv5_042523_0143.root, FC#13, port D2
Entries 386
Mean 43.8
Std Dev 12.08
Turn on : 25.8054
Width : 3.834
Height : 10.062
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U18-ch125
calib_packv5_042523_0143.root, FC#13, port D2
Entries 363
Mean 44.98
Std Dev 11.45
Turn on : 28.3353
Width : 2.092
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U18-ch126
calib_packv5_042523_0143.root, FC#13, port D2
Entries 387
Mean 43.59
Std Dev 12.53
Turn on : 25.9999
Width : 2.427
Height : 9.935
Entry
ampl
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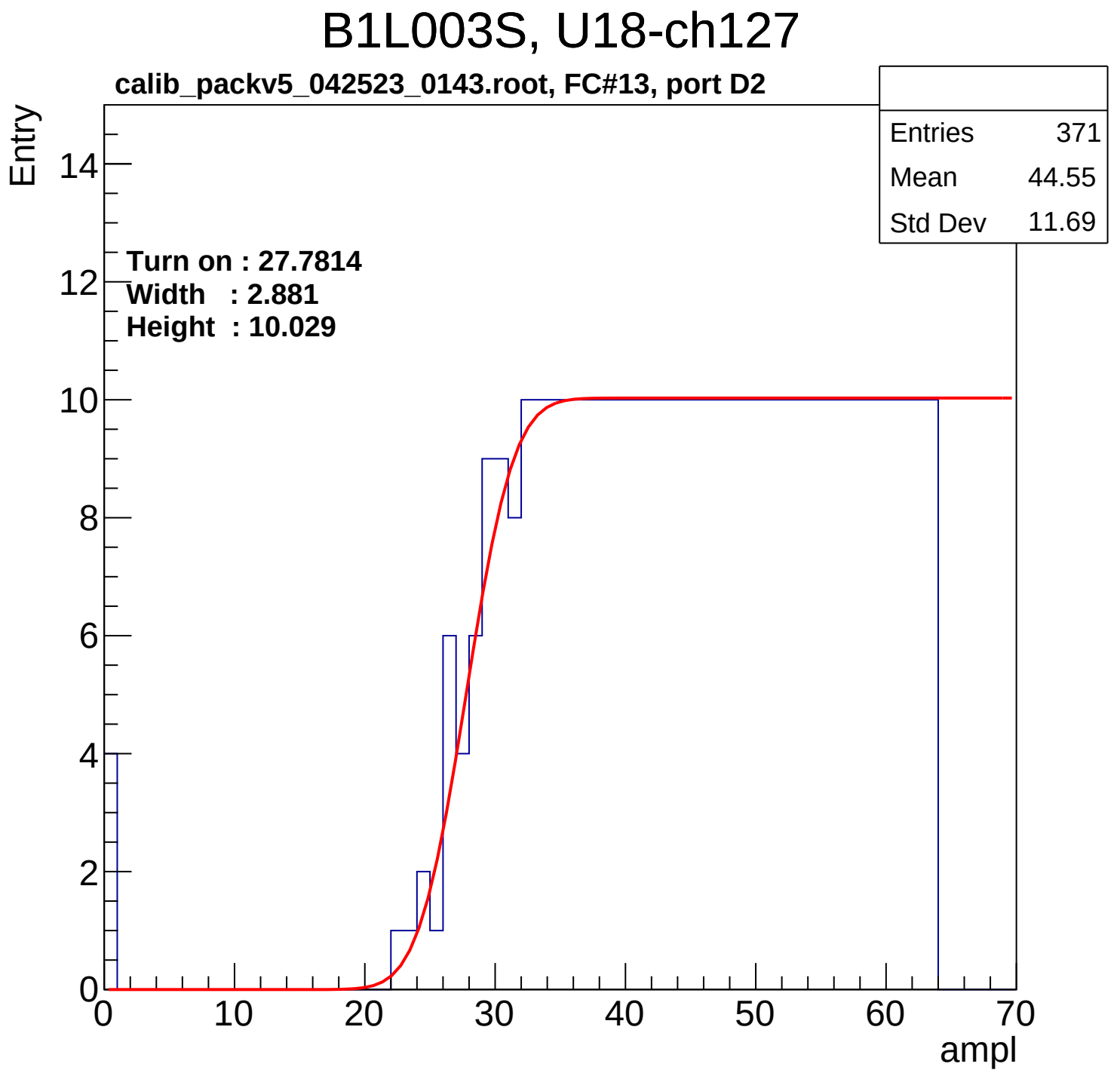
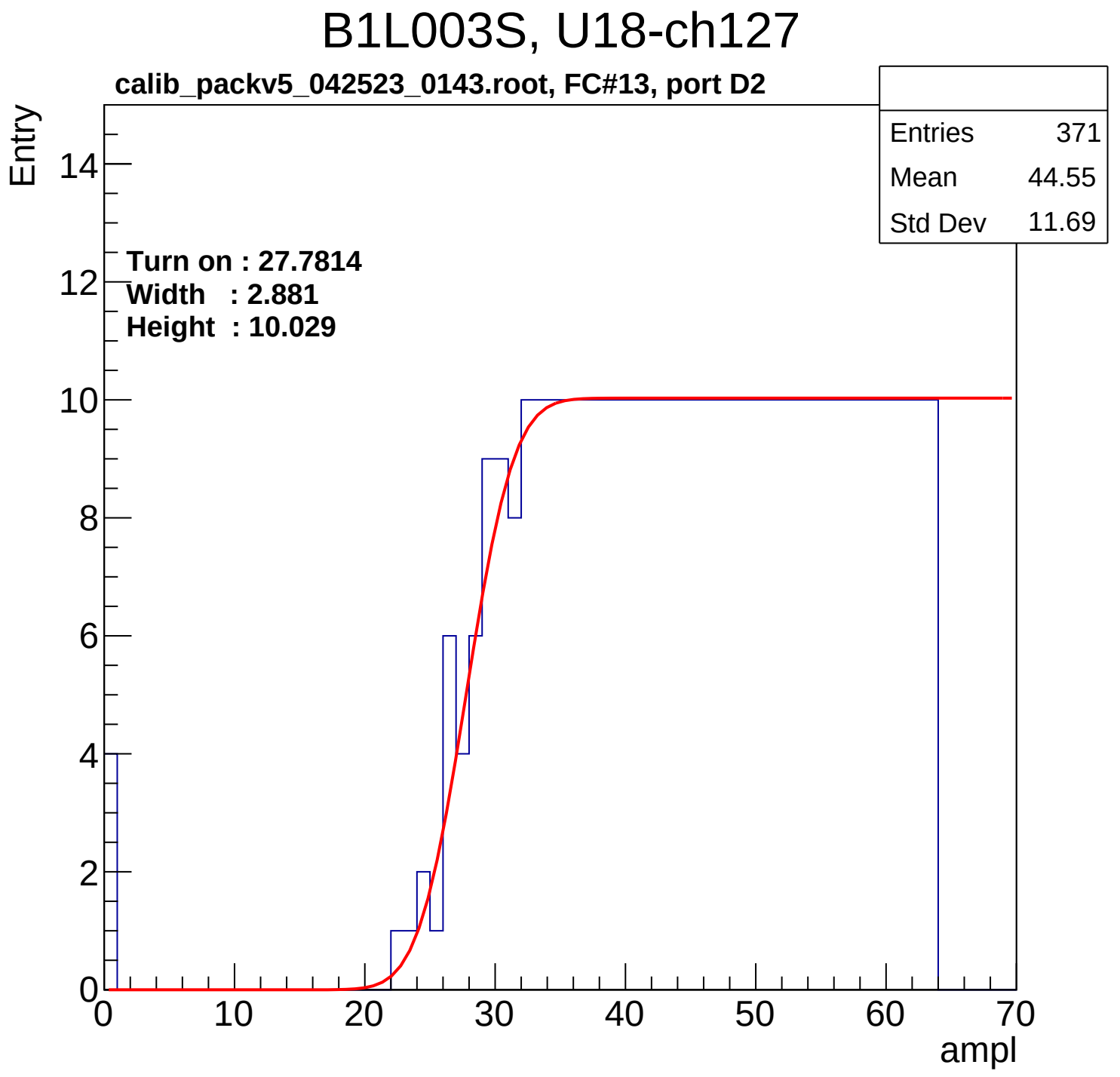
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U18-ch127
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.55
Std Dev 11.69
Turn on : 27.7814
Width : 2.881
Height : 10.029
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L003S, U18-ch127
calib_packv5_042523_0143.root, FC#13, port D2
Entries 371
Mean 44.55
Std Dev 11.69
Turn on : 27.7814
Width : 2.881
Height : 10.029
Entry
ampl
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2
4
6
8
10
12
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0
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20
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