

B1L103S, U21-ch0

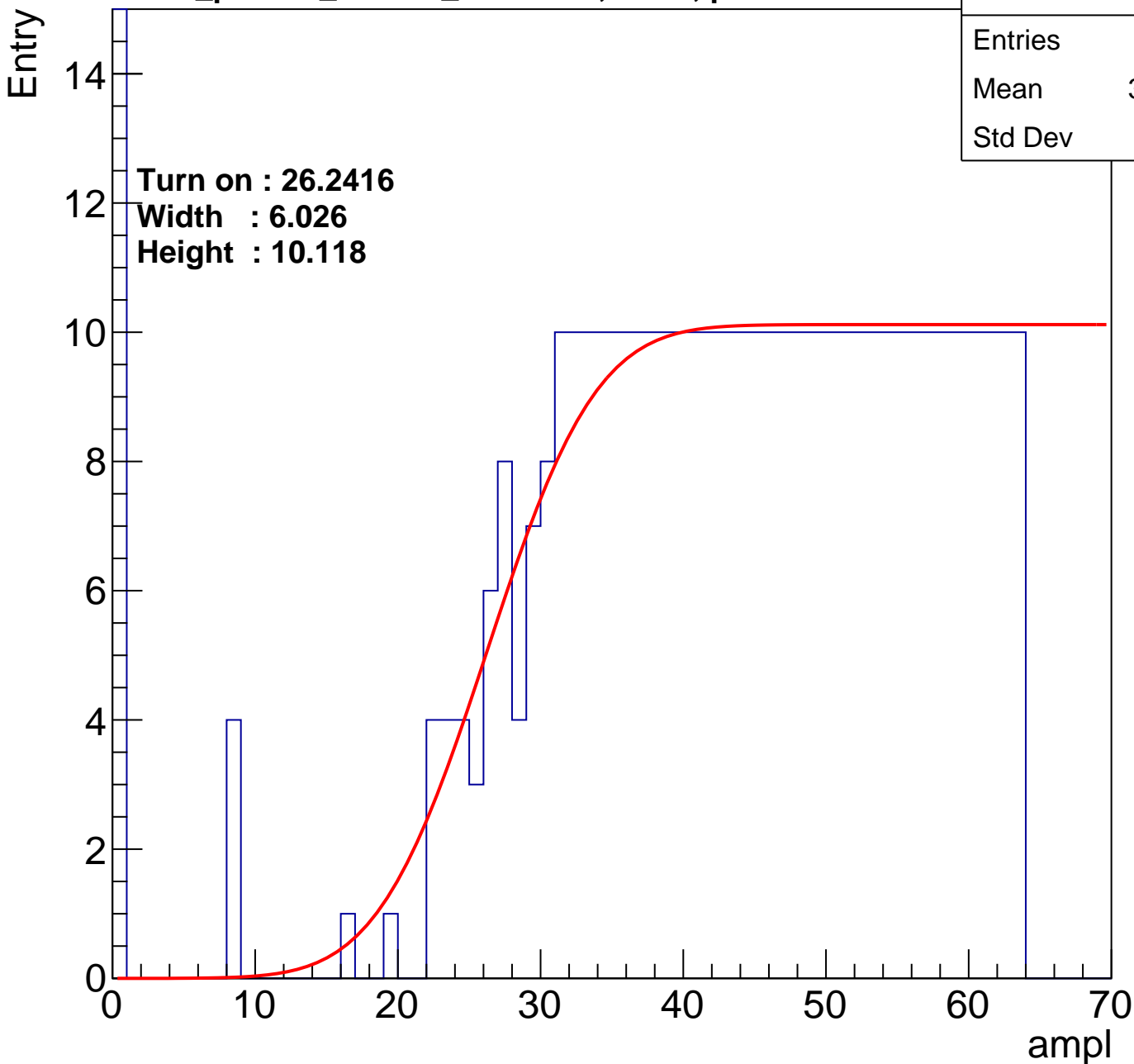
calib_packv5_041523_1651.root, FC#0, port C2

Entries	448
Mean	37.62
Std Dev	18.9

Turn on : 26.2416

Width : 6.026

Height : 10.118



B1L103S, U21-ch1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	39.79
Std Dev	17.39

Turn on : 26.2852

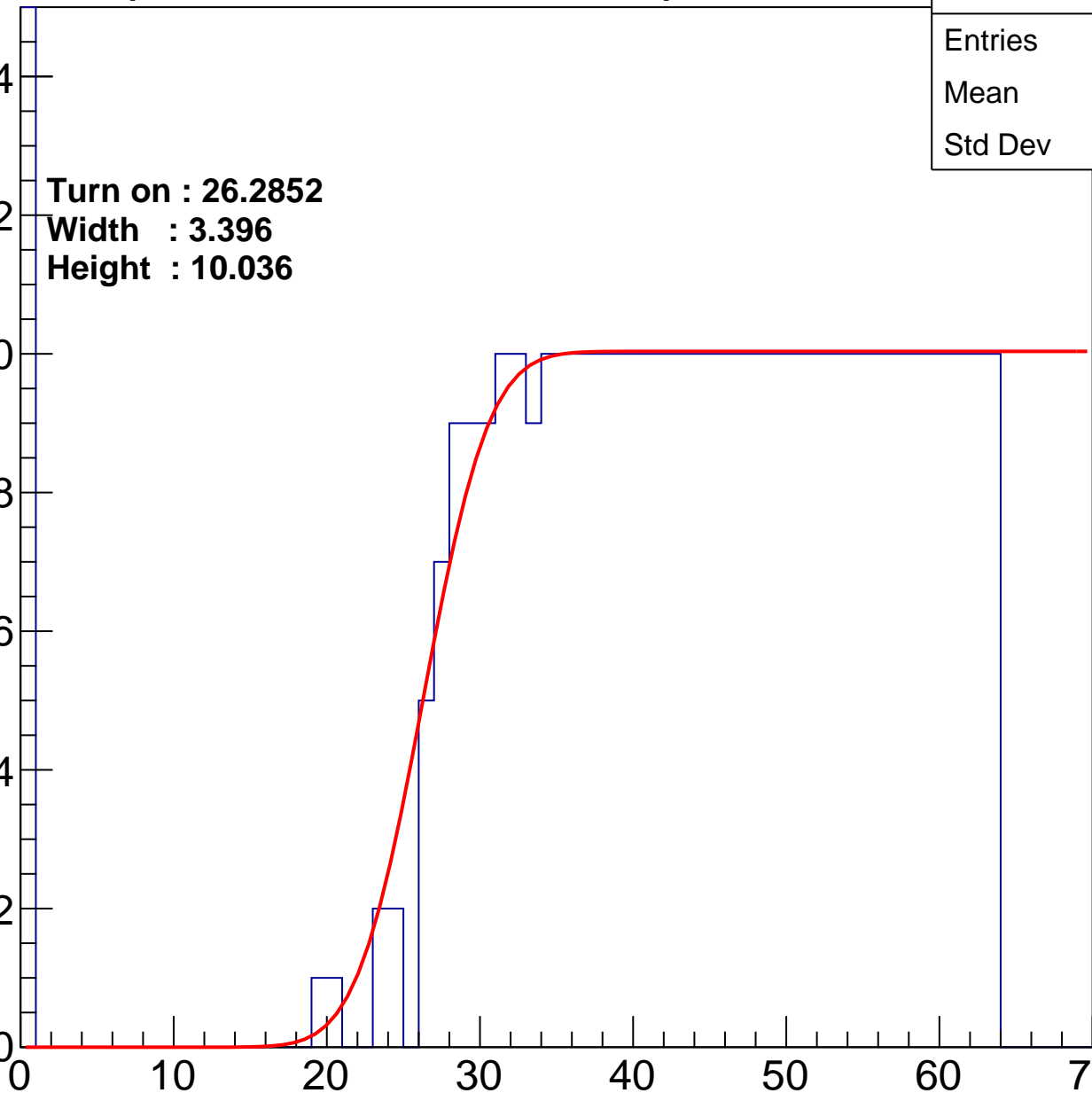
Width : 3.396

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	460
Mean	38.42
Std Dev	17.29

Turn on : 23.0868

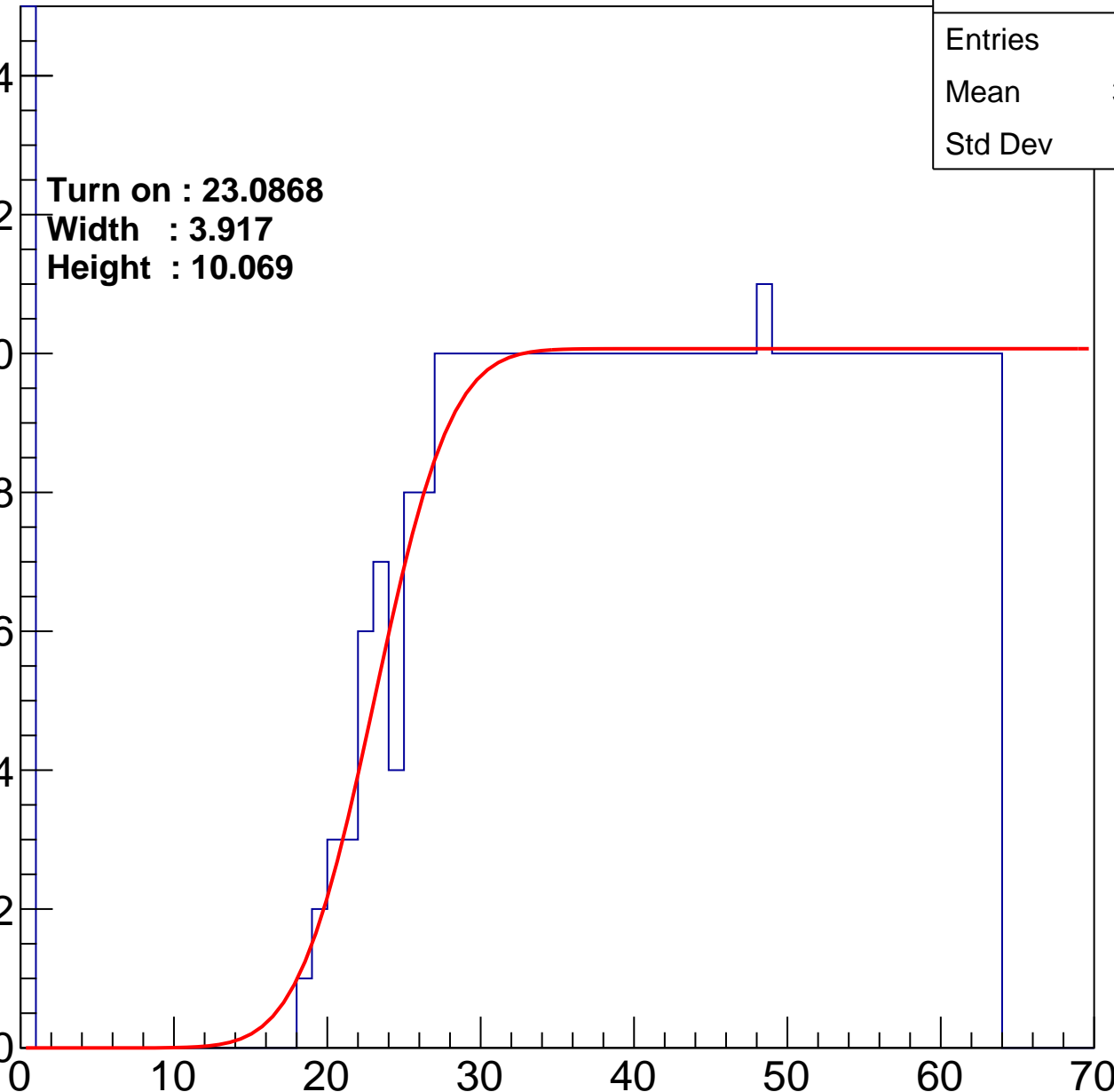
Width : 3.917

Height : 10.069

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	39.98
Std Dev	17.1

Turn on : 26.4835

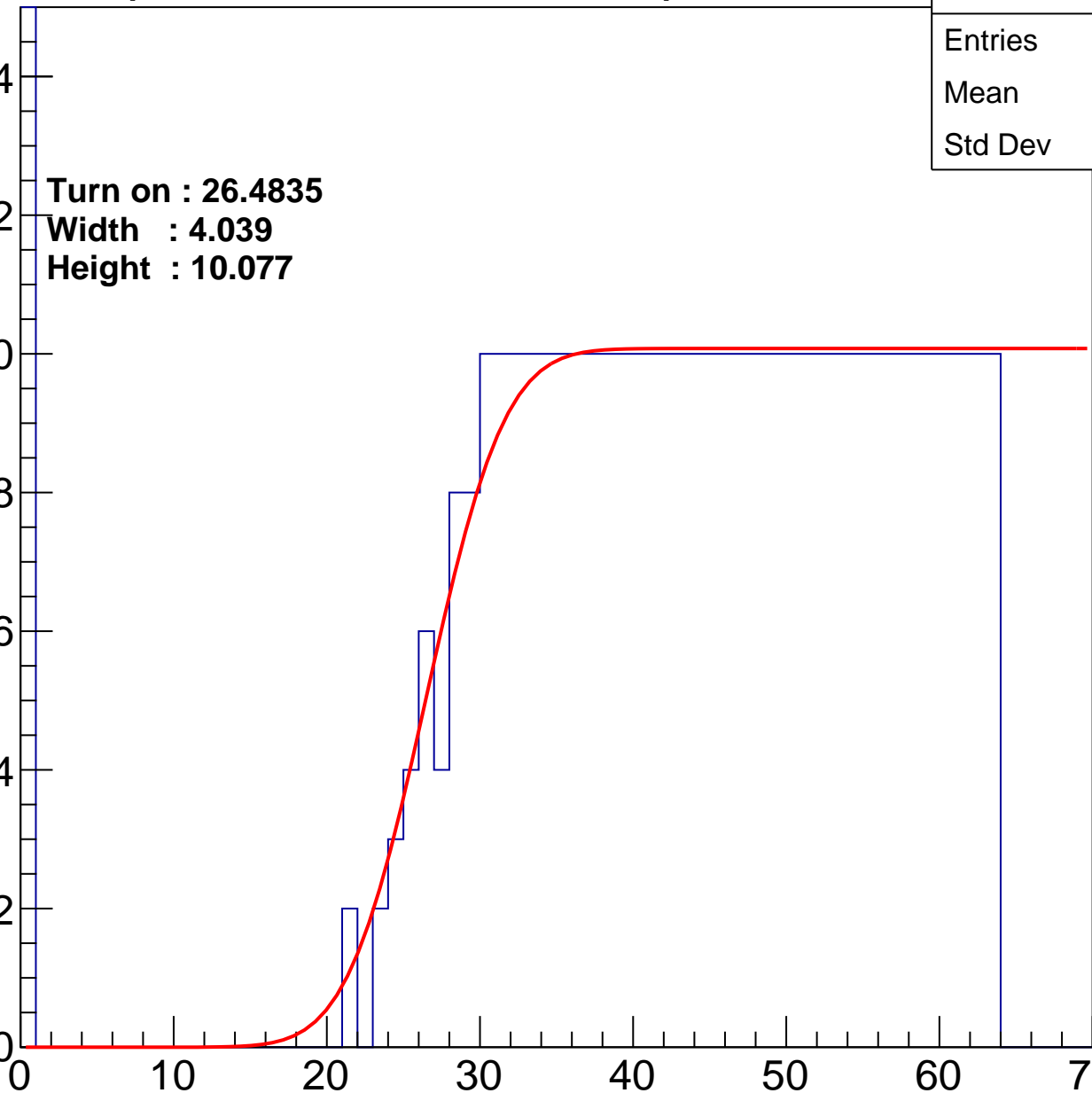
Width : 4.039

Height : 10.077

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	39.8
Std Dev	17.41

Turn on : 26.9804

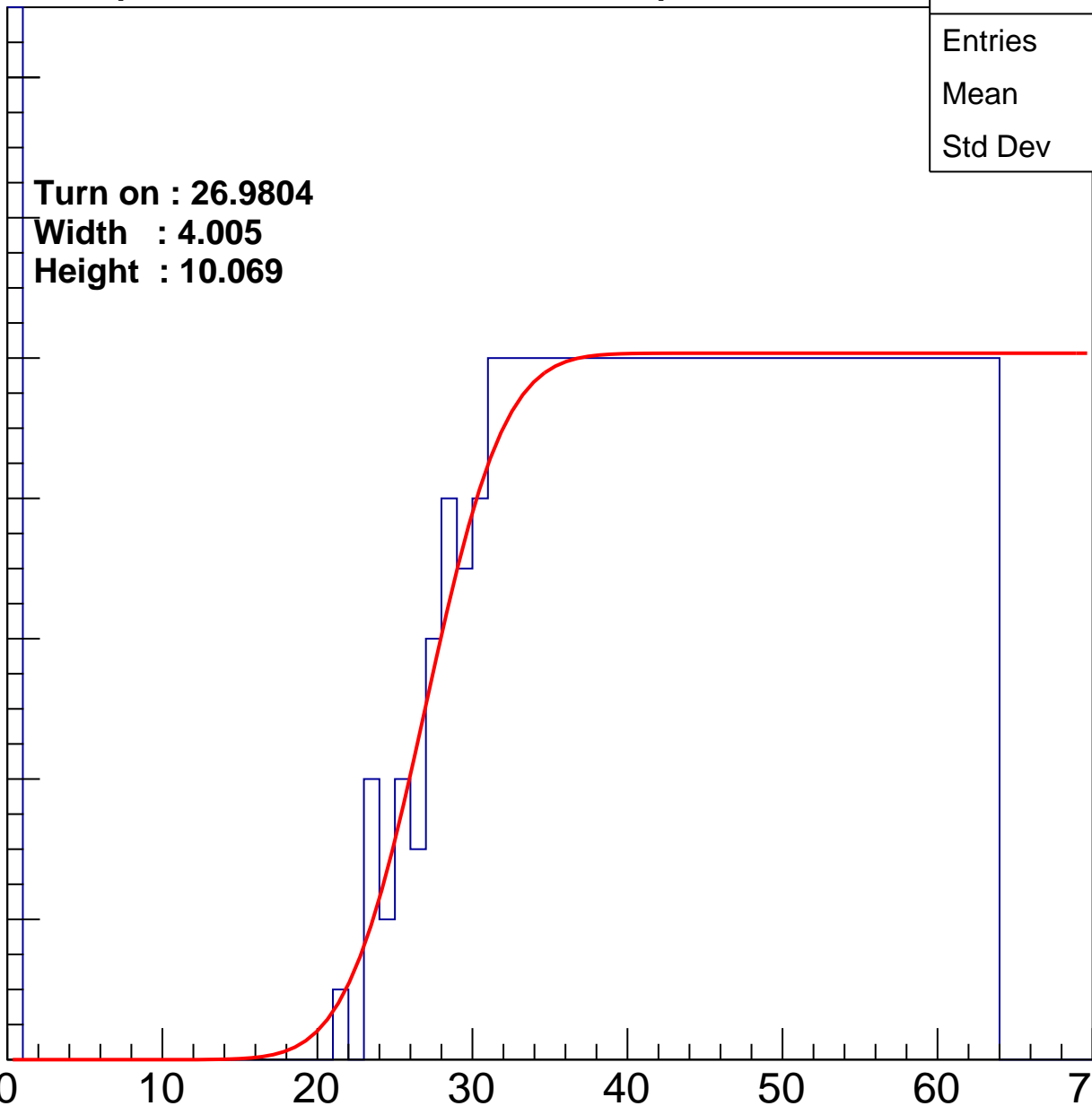
Width : 4.005

Height : 10.069

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch5

calib_packv5_041523_1651.root, FC#0, port C2

Entries	448
Mean	38.47
Std Dev	17.95

Turn on : 24.6711

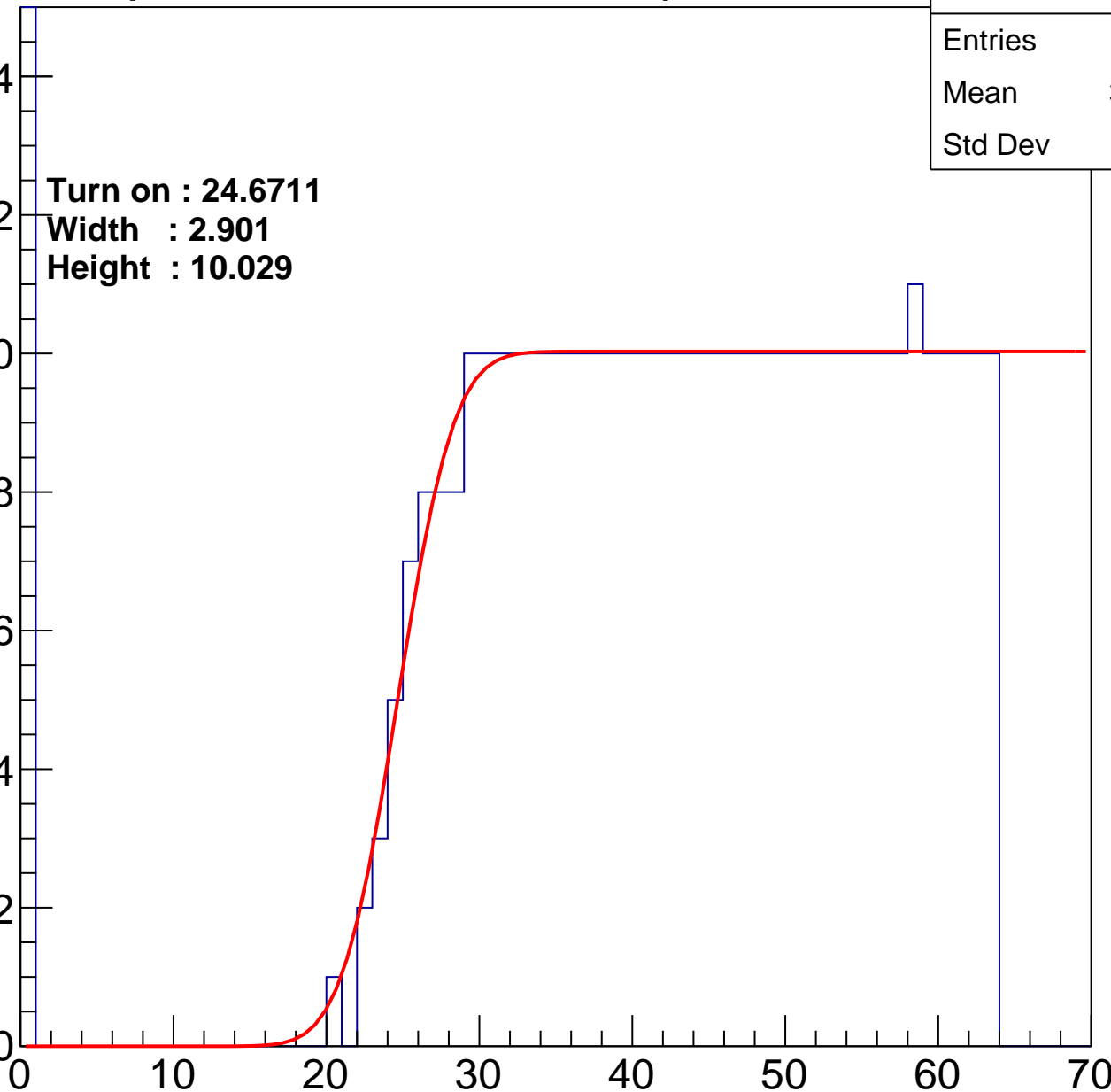
Width : 2.901

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch6

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	39.33
Std Dev	17.88

Turn on : 27.0727

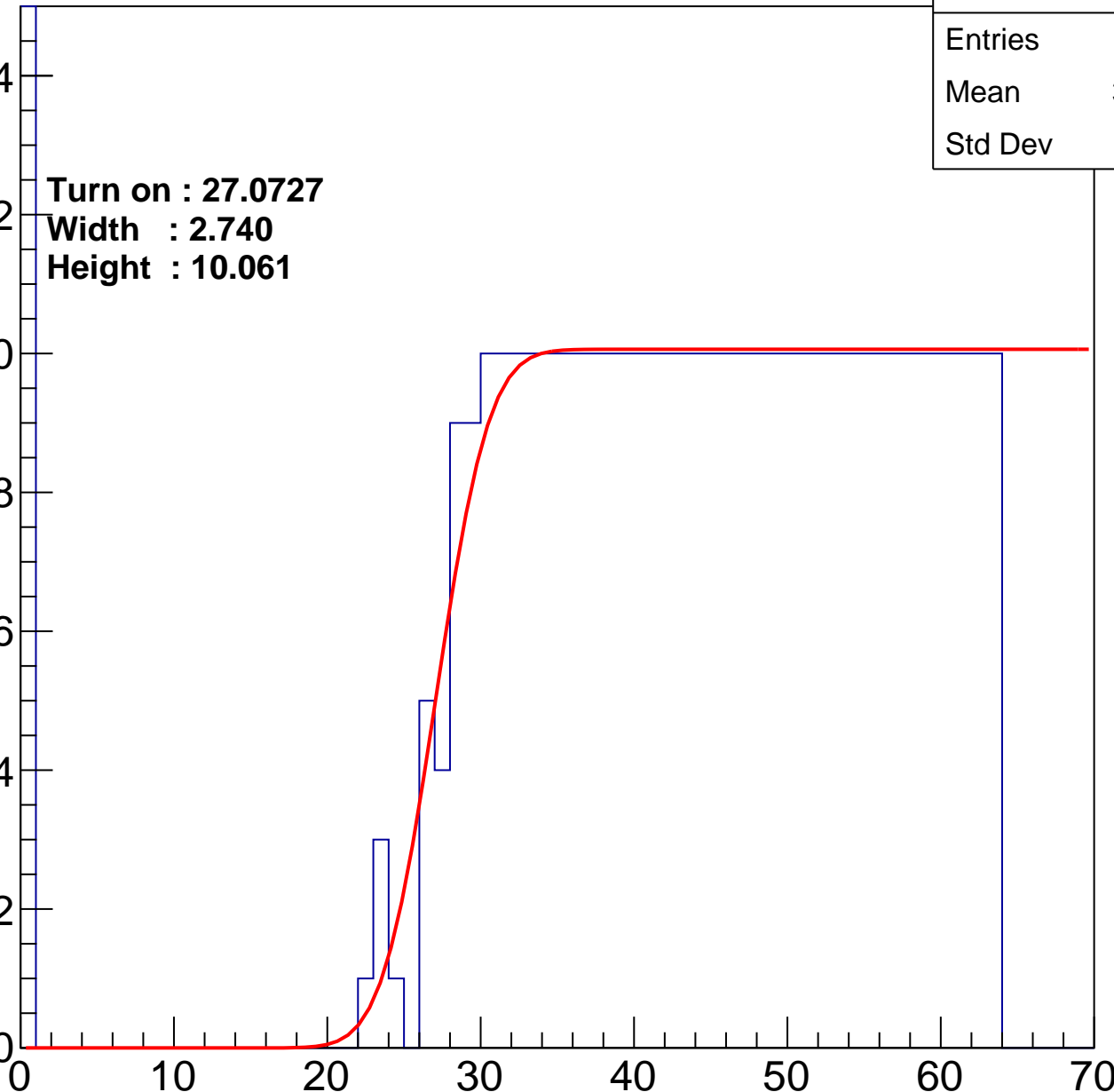
Width : 2.740

Height : 10.061

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	407
Mean	40.63
Std Dev	16.86

Turn on : 27.2841

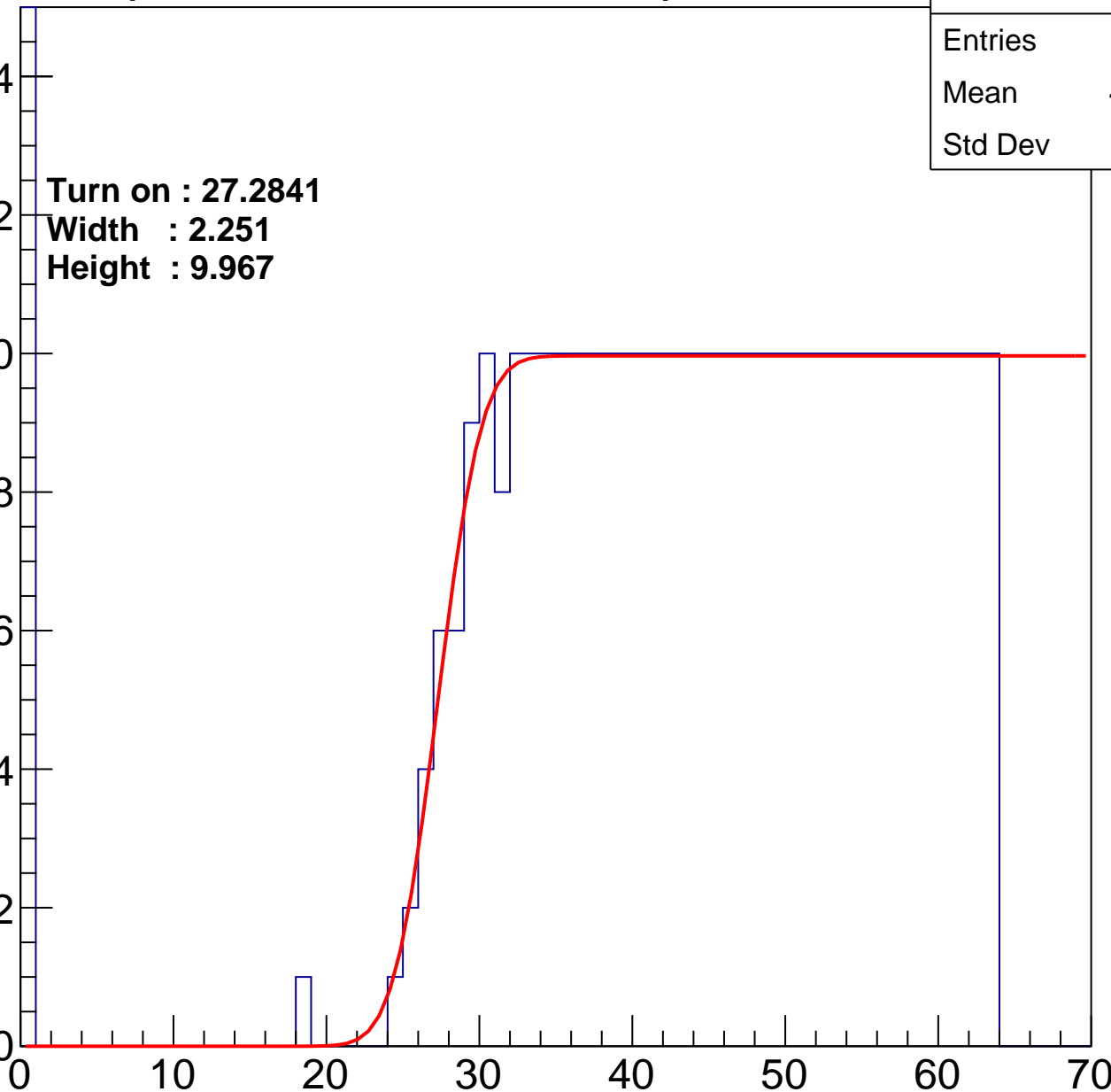
Width : 2.251

Height : 9.967

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch8

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	38.83
Std Dev	17.95

Turn on : 26.0102

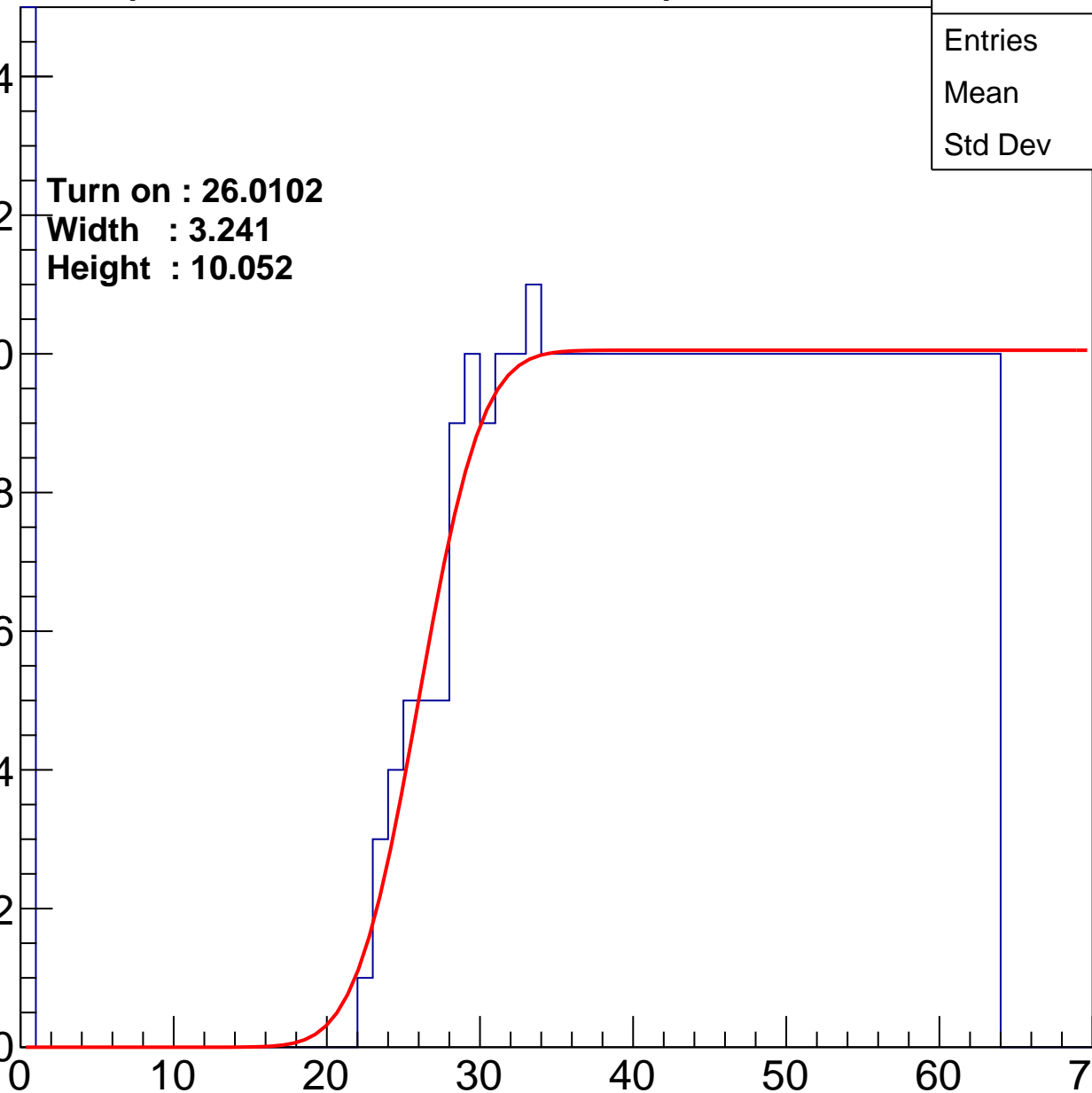
Width : 3.241

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch9

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	39.29
Std Dev	17.37

Turn on : 25.3271

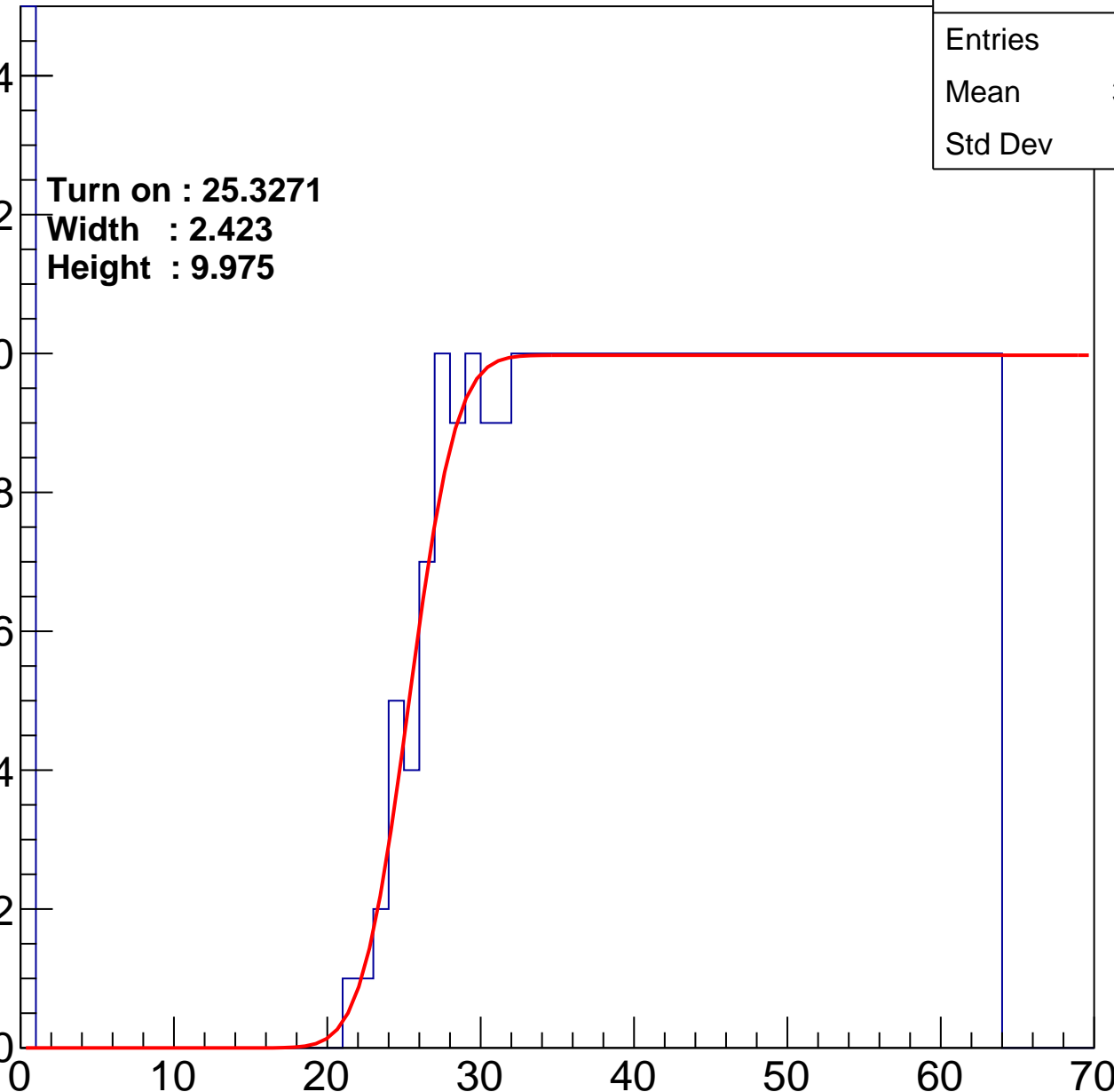
Width : 2.423

Height : 9.975

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch10

calib_packv5_041523_1651.root, FC#0, port C2

Entries	415
Mean	40.02
Std Dev	17.33

Turn on : 27.3665

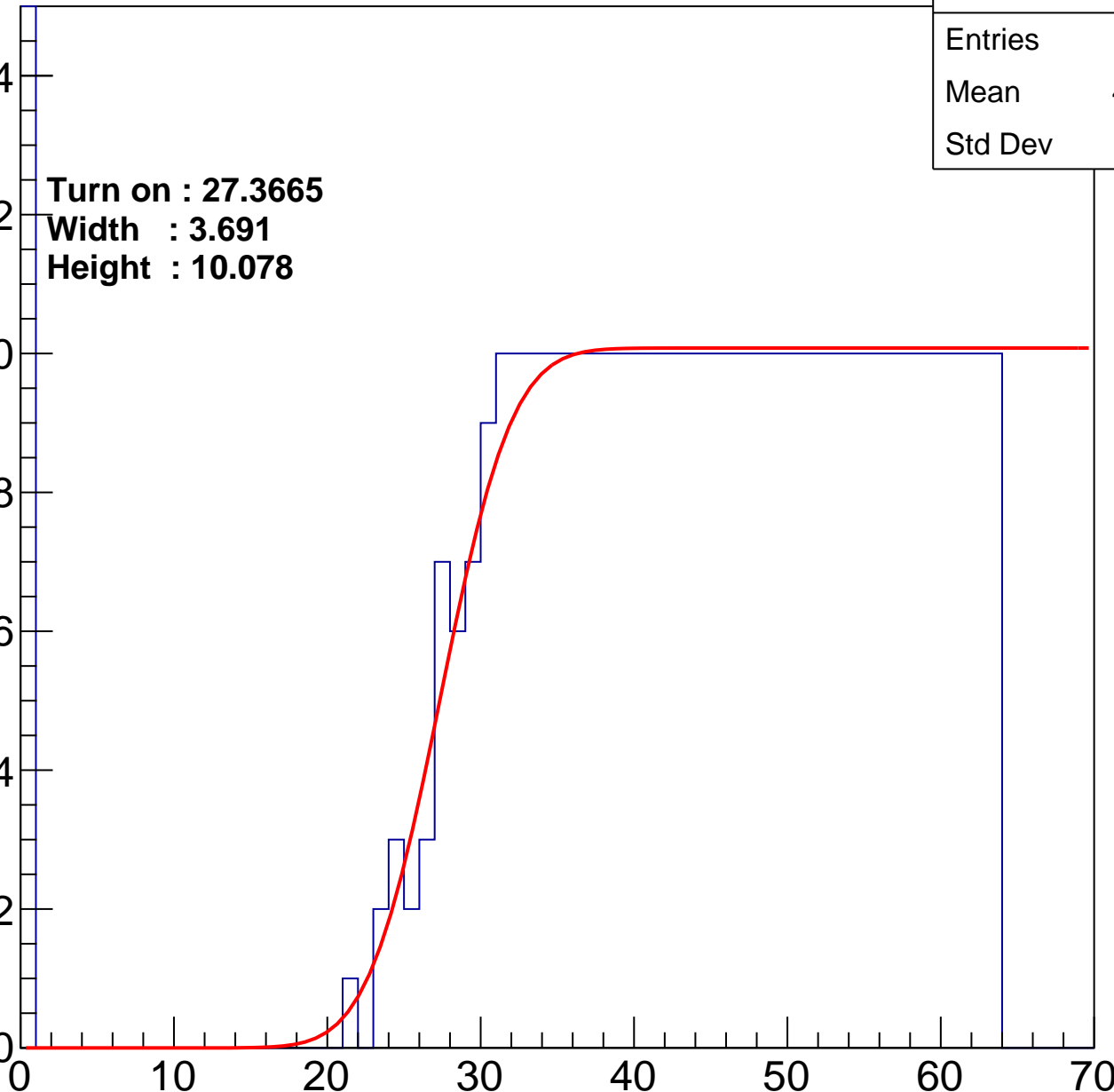
Width : 3.691

Height : 10.078

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch11

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	38.9
Std Dev	18.52

Turn on : 27.5231

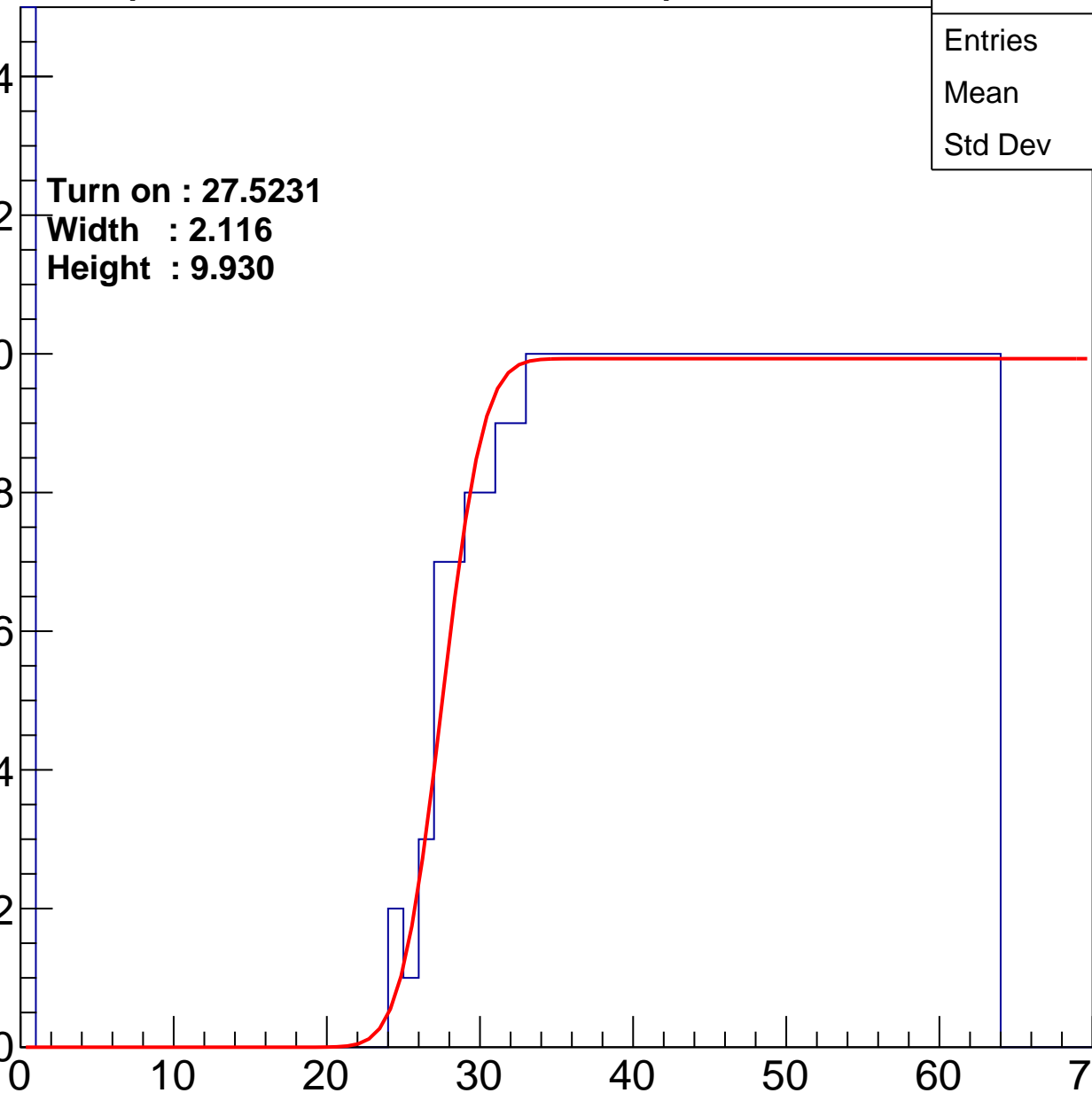
Width : 2.116

Height : 9.930

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch12

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	40.38
Std Dev	16.59

Turn on : 26.1587

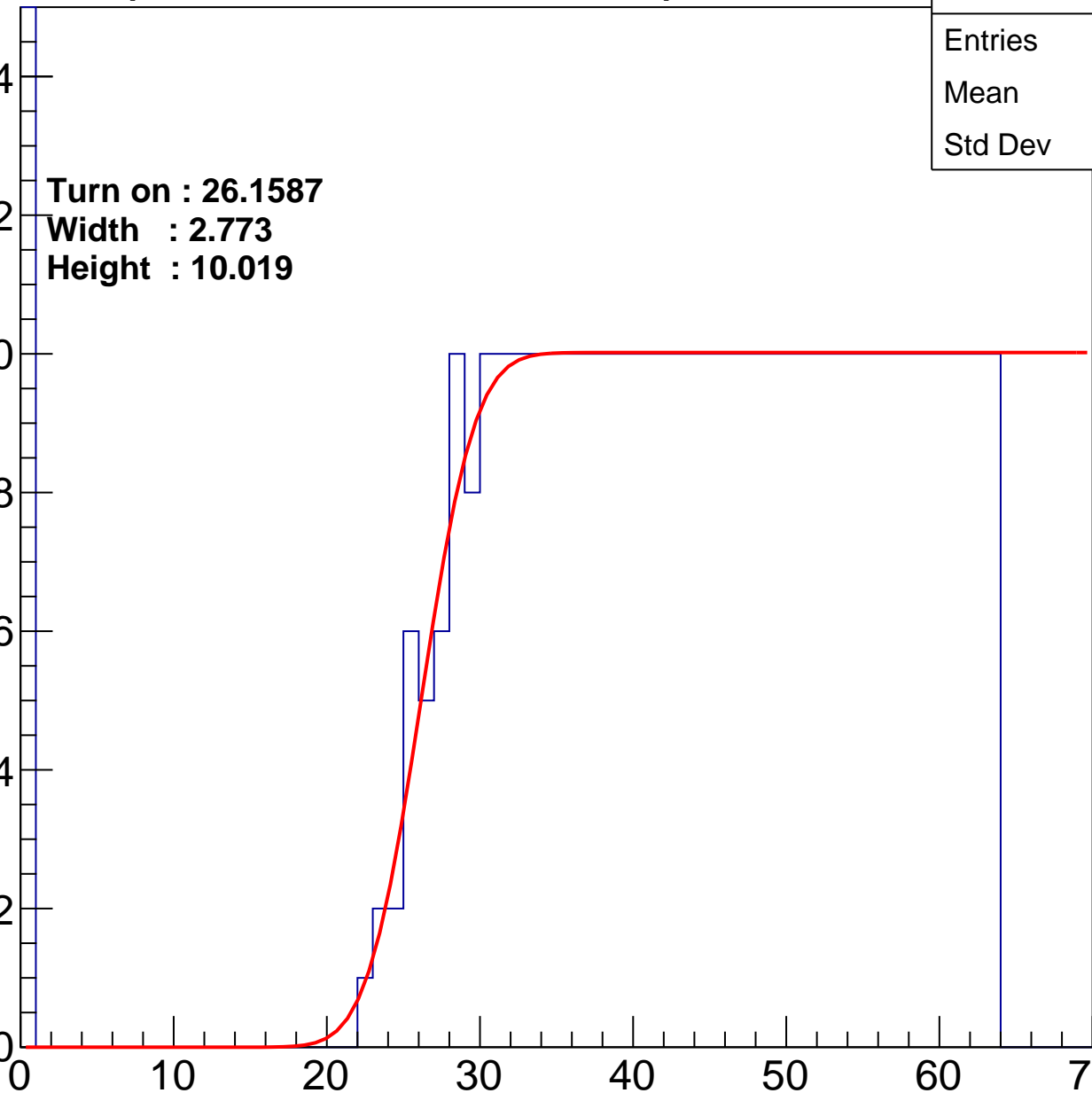
Width : 2.773

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch13

calib_packv5_041523_1651.root, FC#0, port C2

Entries	391
Mean	40.74
Std Dev	17.64

Turn on : 30.0236

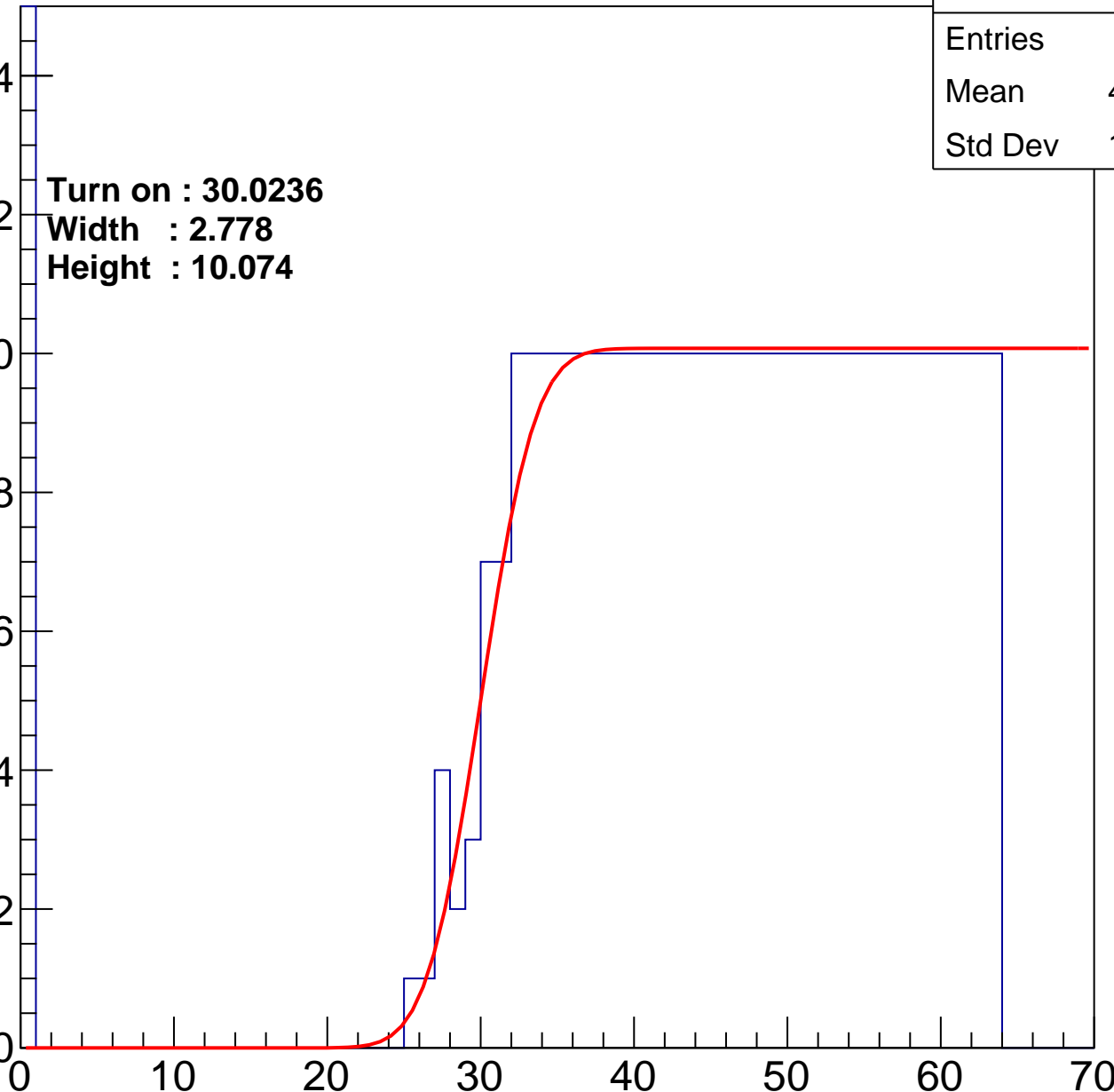
Width : 2.778

Height : 10.074

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch14

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	40.58
Std Dev	15.91

Turn on : 24.2759

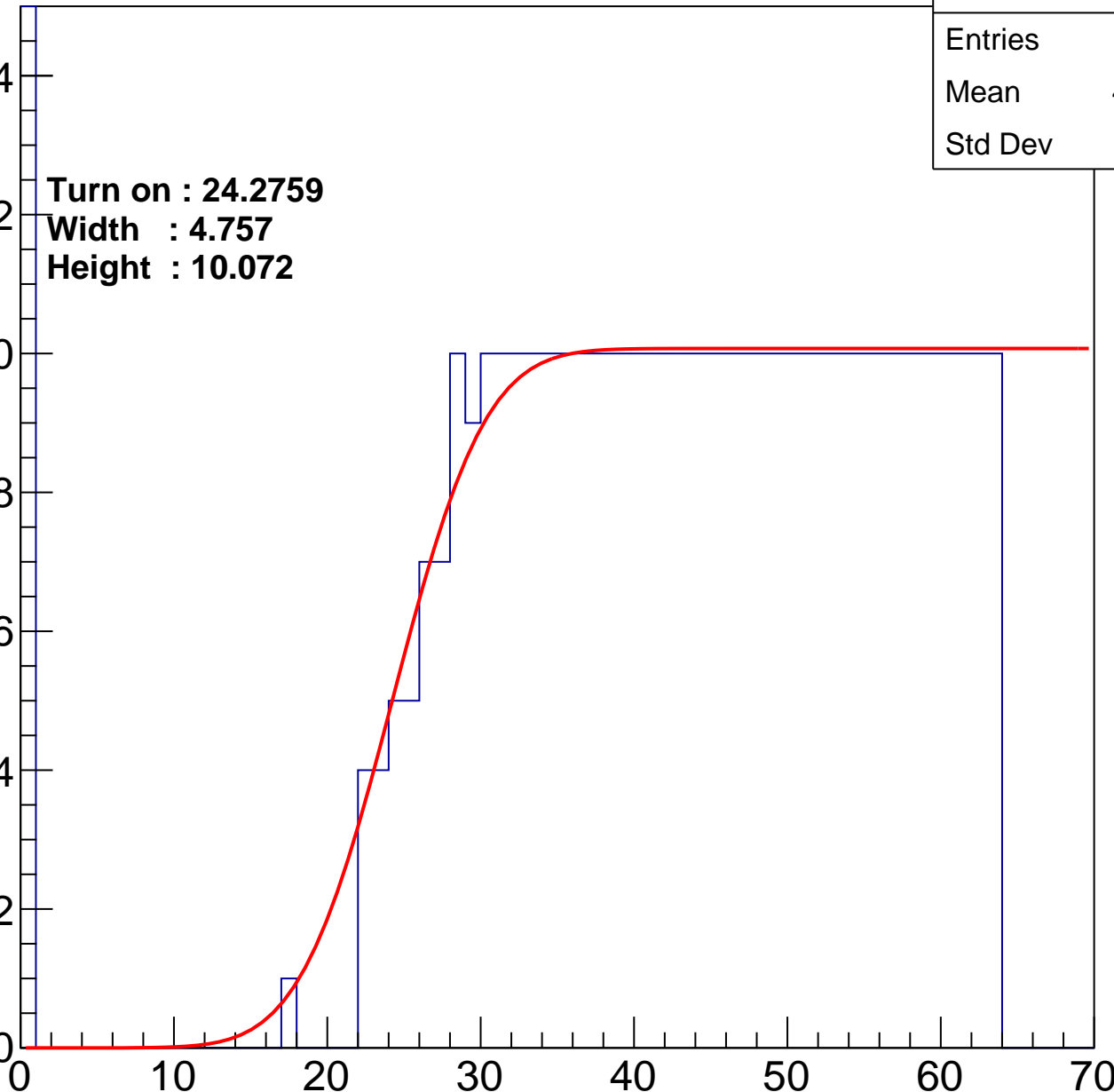
Width : 4.757

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch15

calib_packv5_041523_1651.root, FC#0, port C2

Entries	422
Mean	39.6
Std Dev	17.55

Turn on : 26.3857

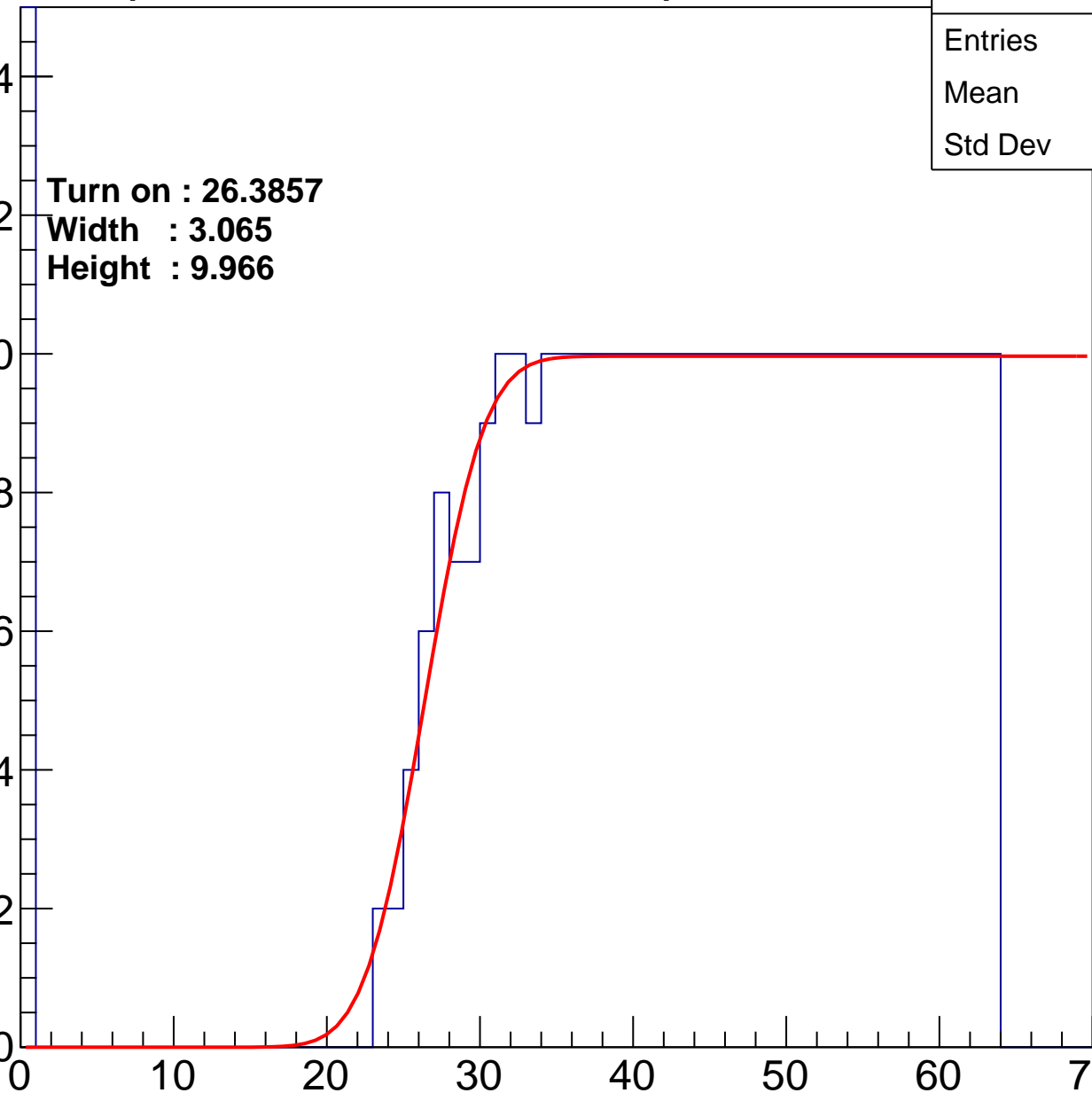
Width : 3.065

Height : 9.966

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch16

calib_packv5_041523_1651.root, FC#0, port C2

Entries	455
Mean	38.47
Std Dev	17.59

Turn on : 25.0097

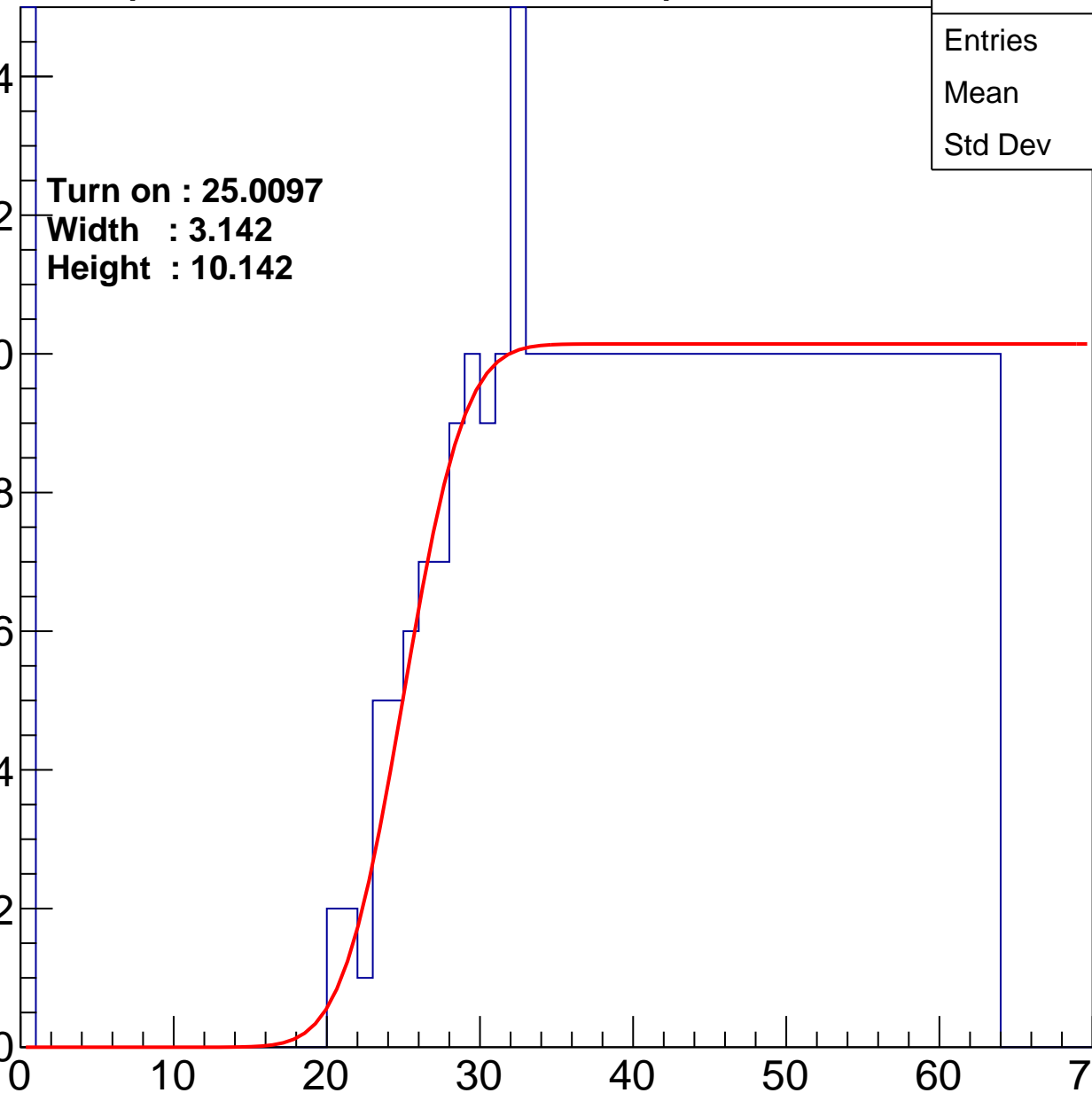
Width : 3.142

Height : 10.142

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch17

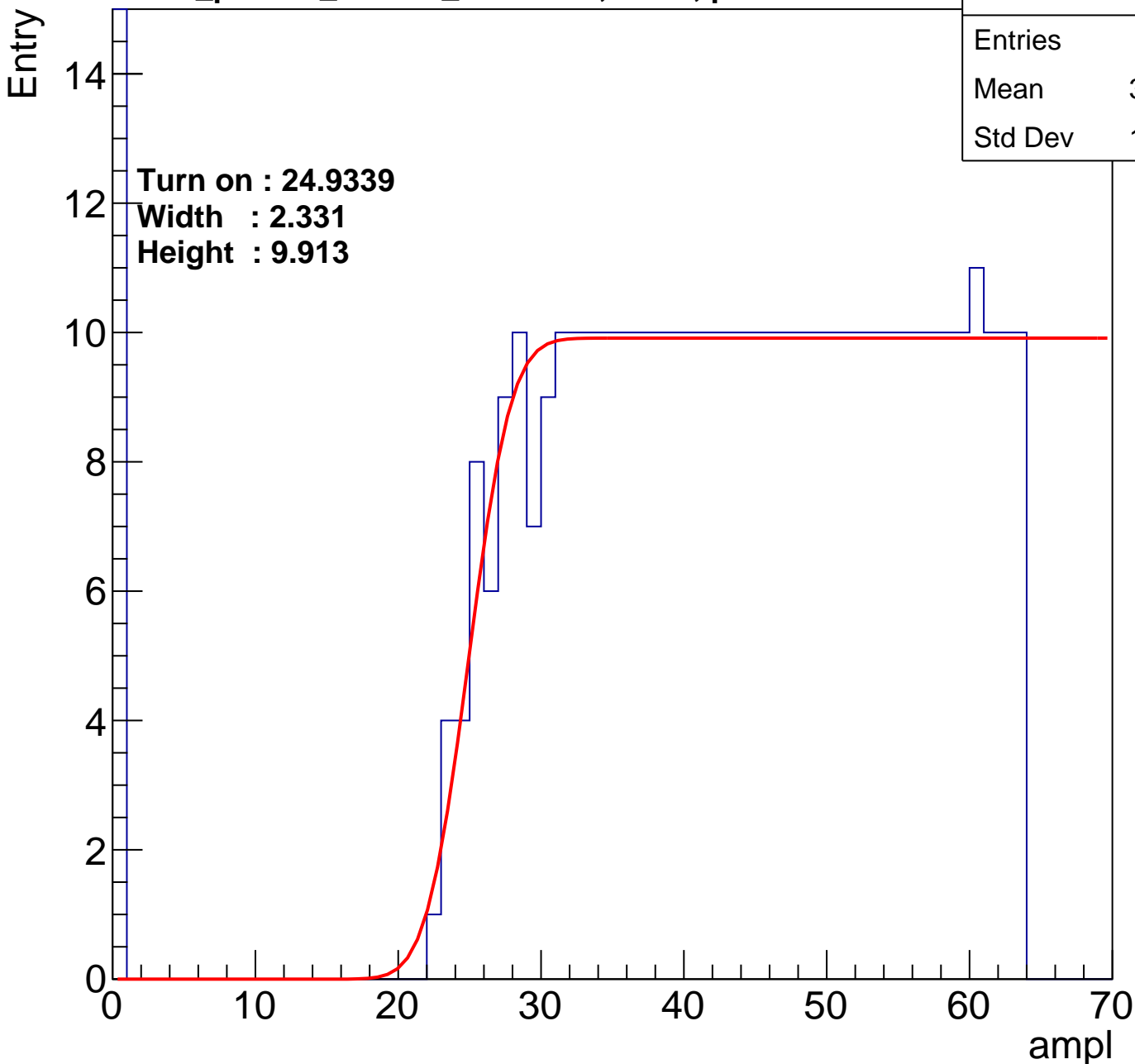
calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	39.38
Std Dev	17.29

Turn on : 24.9339

Width : 2.331

Height : 9.913



B1L103S, U21-ch18

calib_packv5_041523_1651.root, FC#0, port C2

Entries	415
Mean	39.87
Std Dev	17.53

Turn on : 27.0699

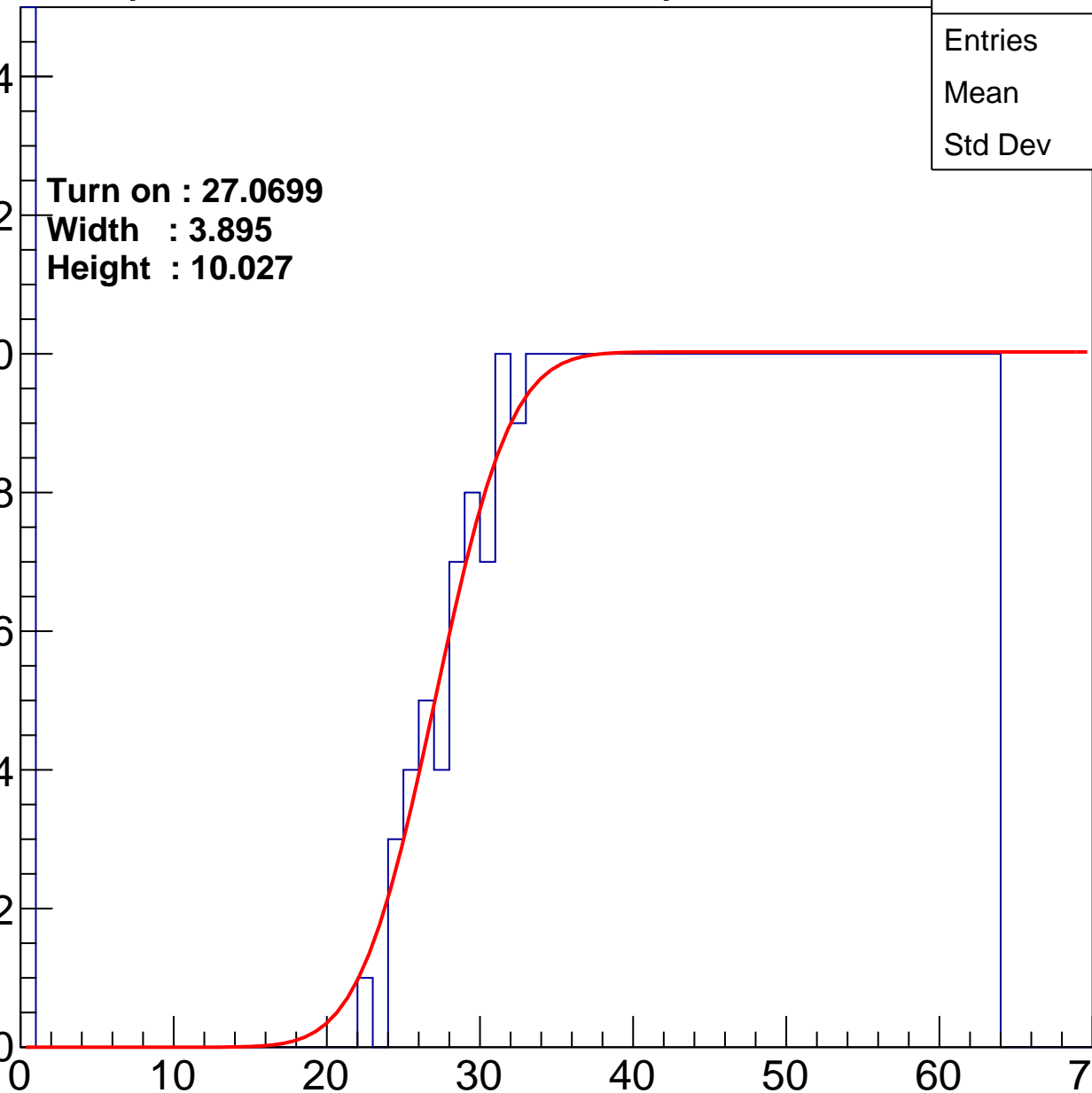
Width : 3.895

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch19

calib_packv5_041523_1651.root, FC#0, port C2

Entries	448
Mean	38.35
Std Dev	18.01

Turn on : 24.9893

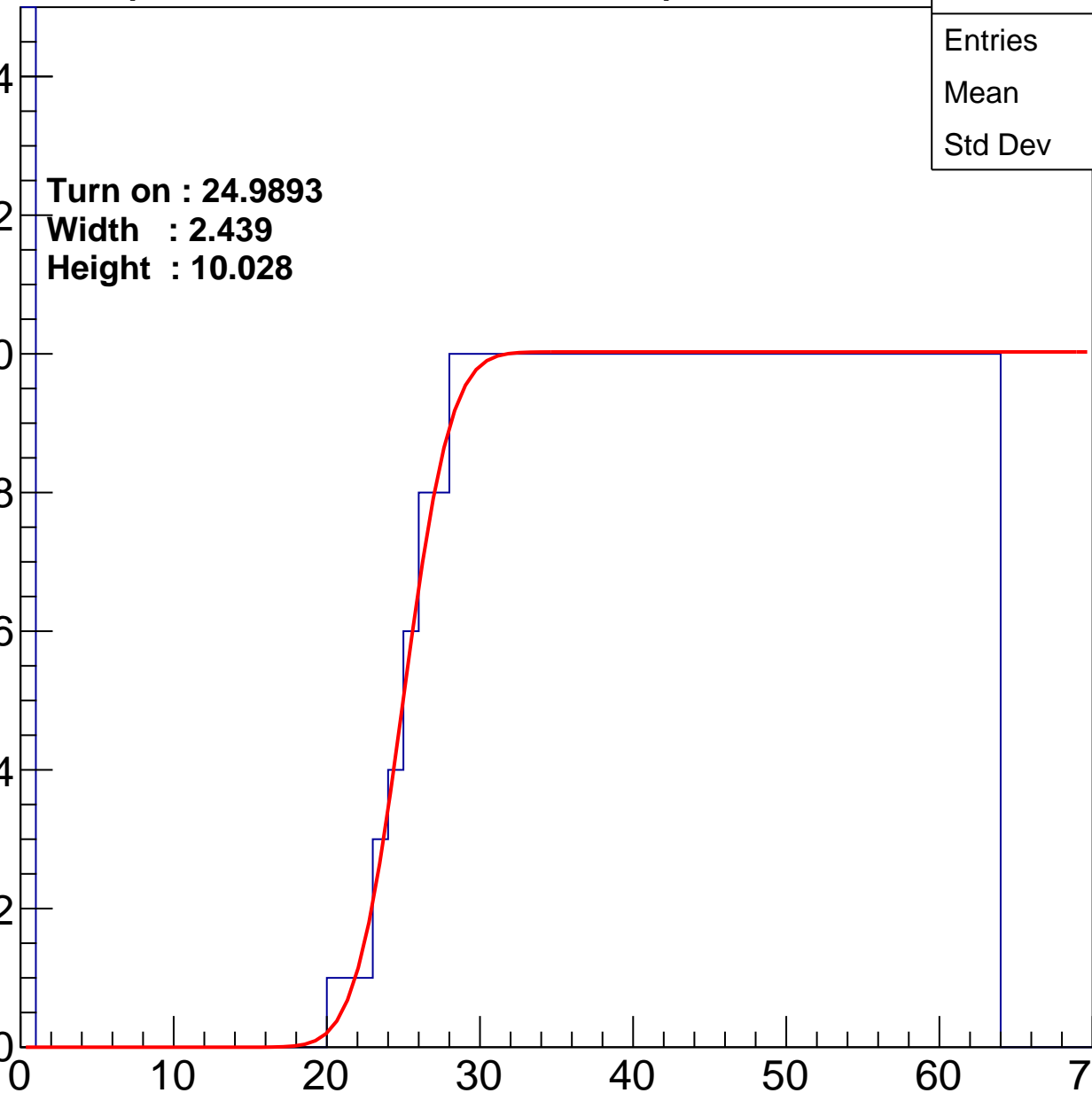
Width : 2.439

Height : 10.028

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch20

calib_packv5_041523_1651.root, FC#0, port C2

Entries	410
Mean	40.45
Std Dev	16.96

Turn on : 28.2006

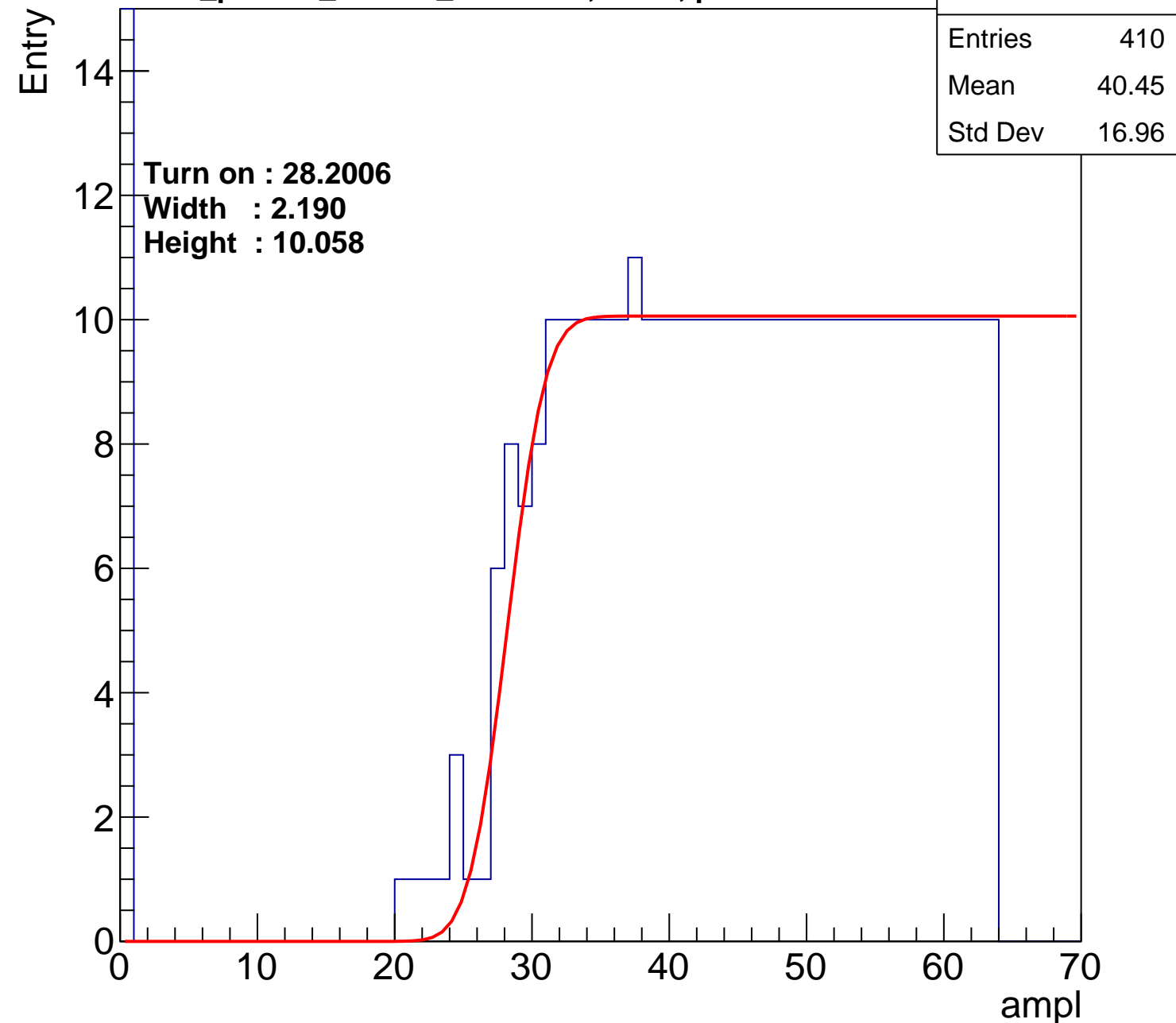
Width : 2.190

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch21

calib_packv5_041523_1651.root, FC#0, port C2

Entries	417
Mean	39.59
Std Dev	17.87

Turn on : 28.3046

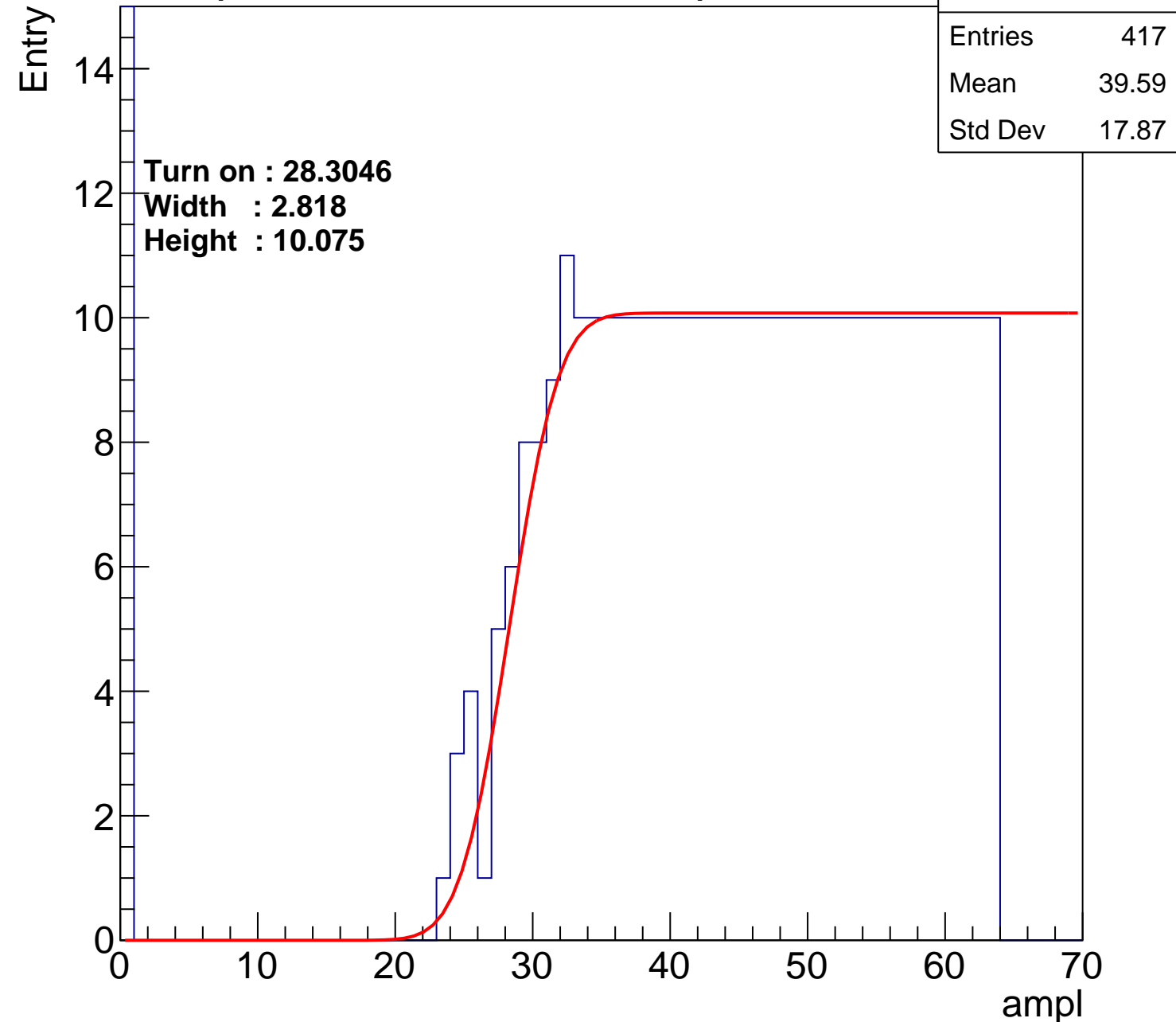
Width : 2.818

Height : 10.075

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch22

calib_packv5_041523_1651.root, FC#0, port C2

Entries	453
Mean	37.94
Std Dev	18.36

Turn on : 25.2360

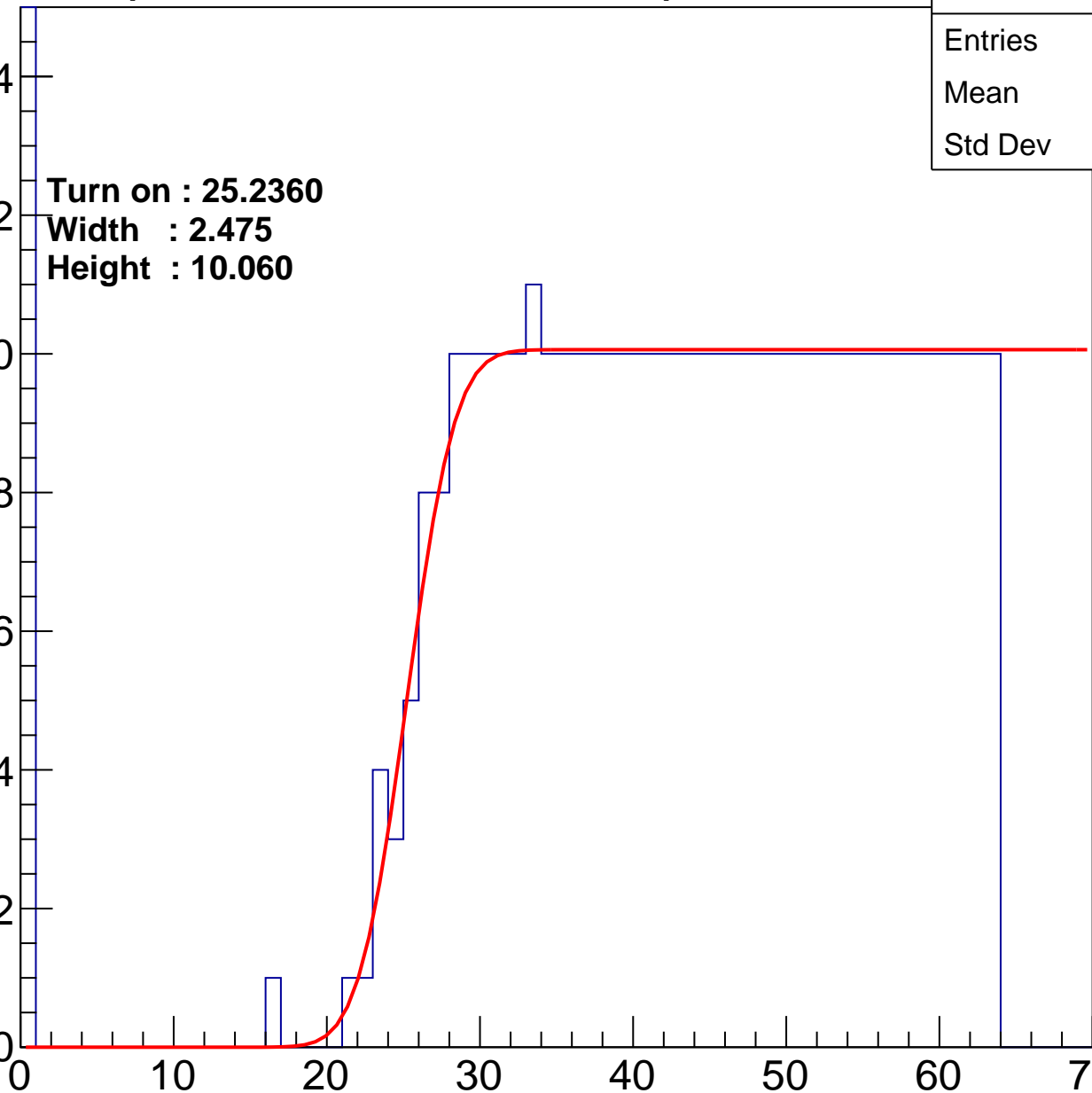
Width : 2.475

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch23

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	40.09
Std Dev	16.69

Turn on : 25.8516

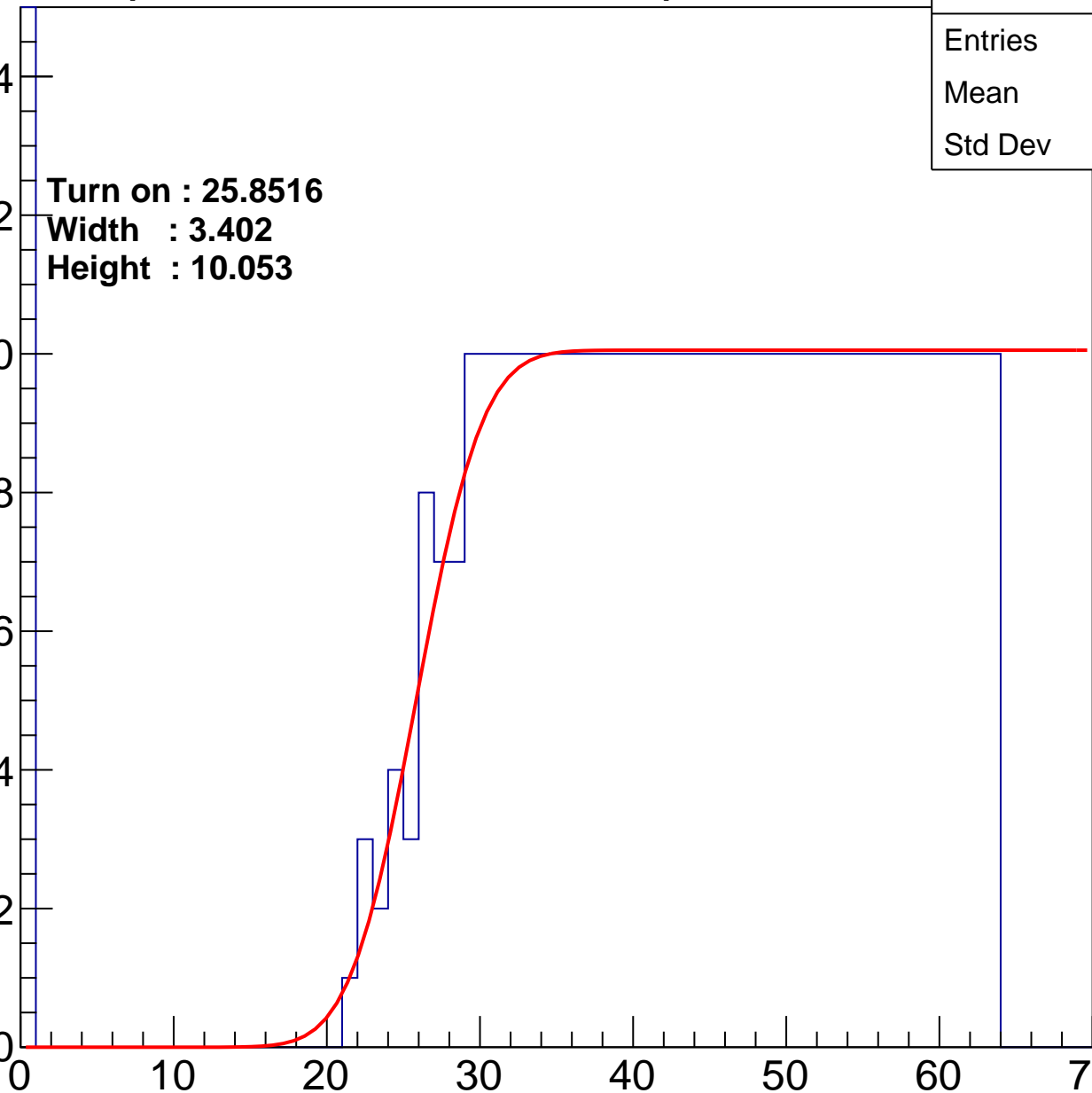
Width : 3.402

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch24

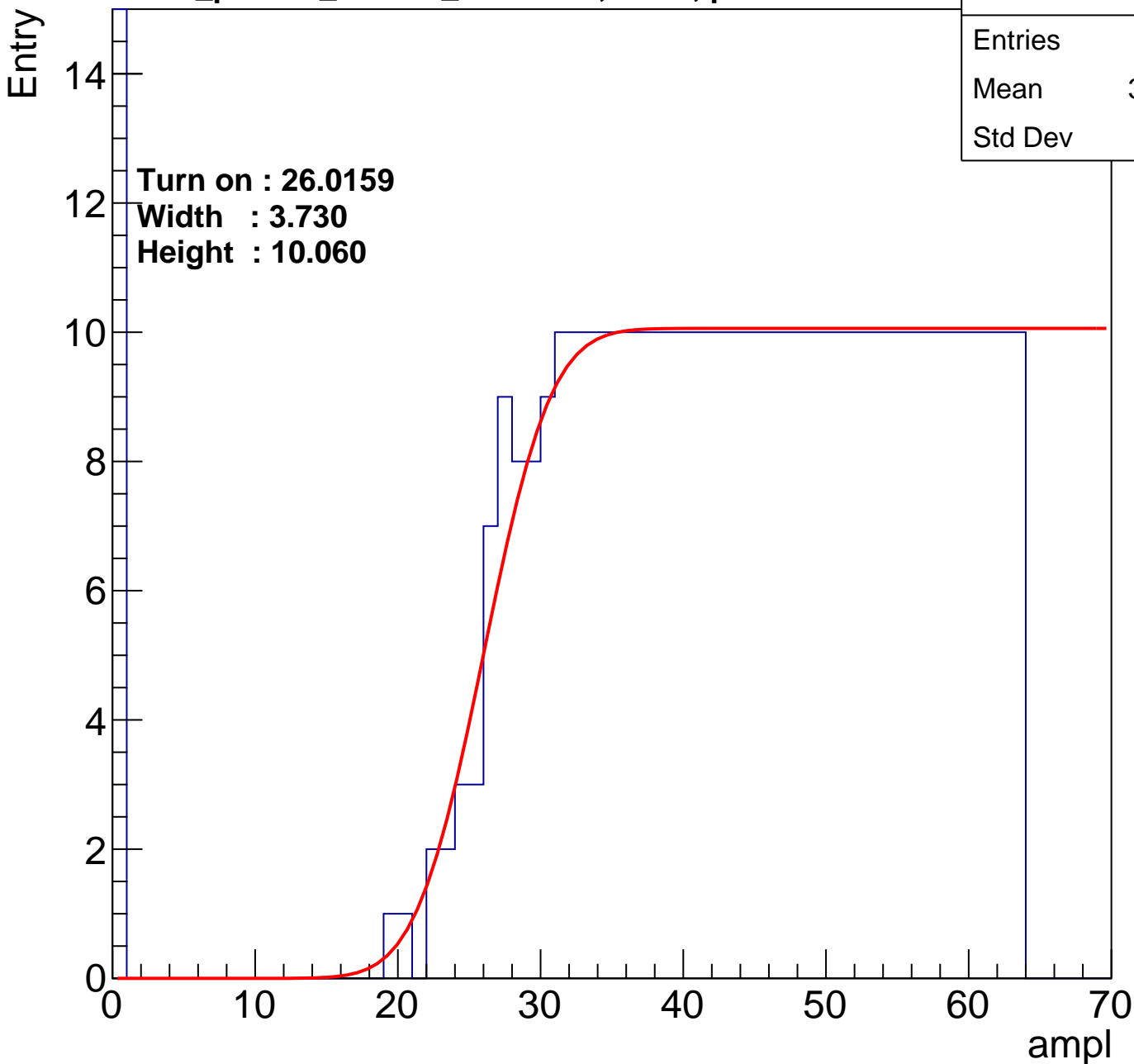
calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	39.95
Std Dev	16.9

Turn on : 26.0159

Width : 3.730

Height : 10.060



B1L103S, U21-ch25

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	38.44
Std Dev	18.89

Turn on : 27.4126

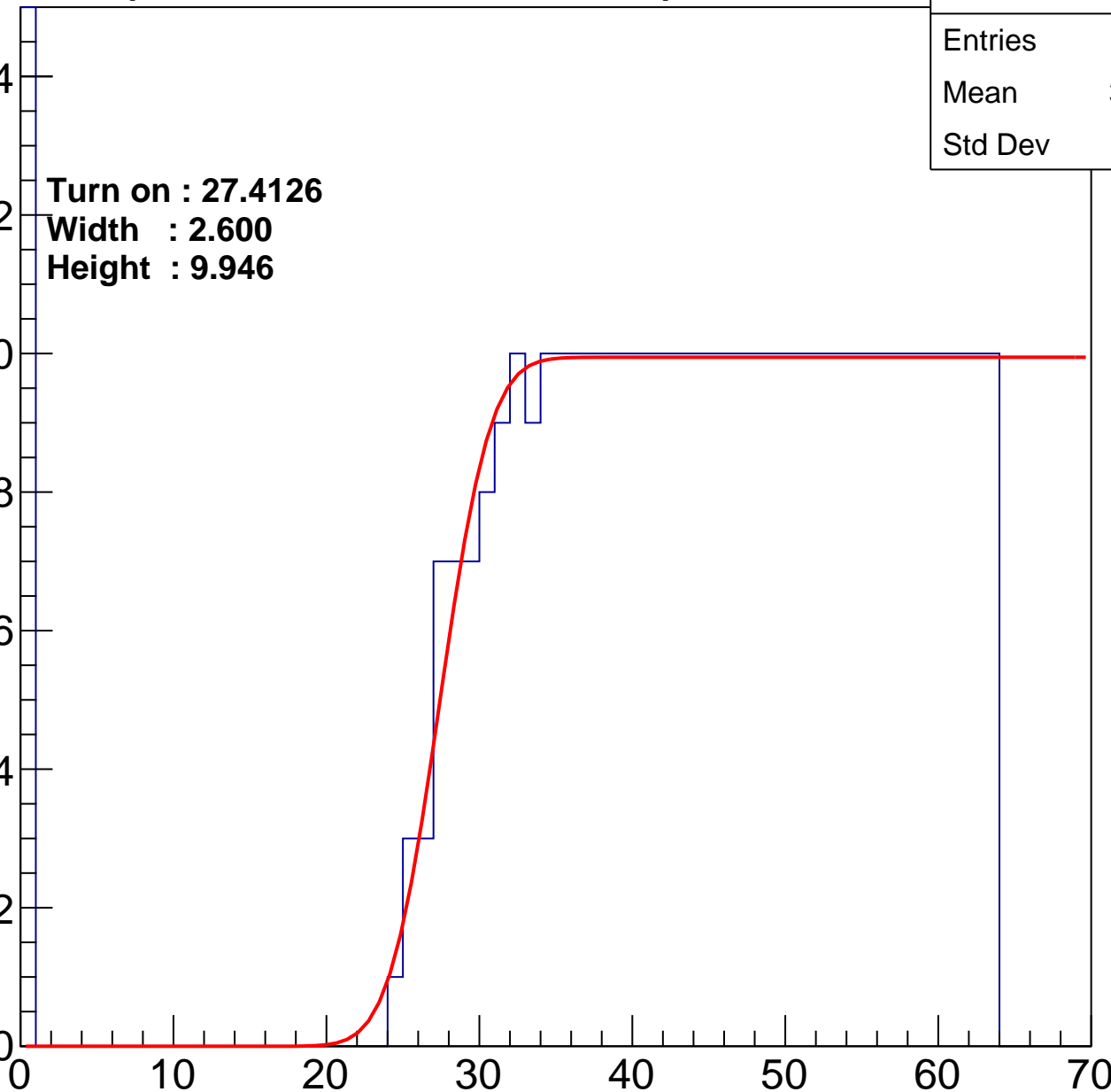
Width : 2.600

Height : 9.946

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch26

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	39.05
Std Dev	17.94

Turn on : 25.7956

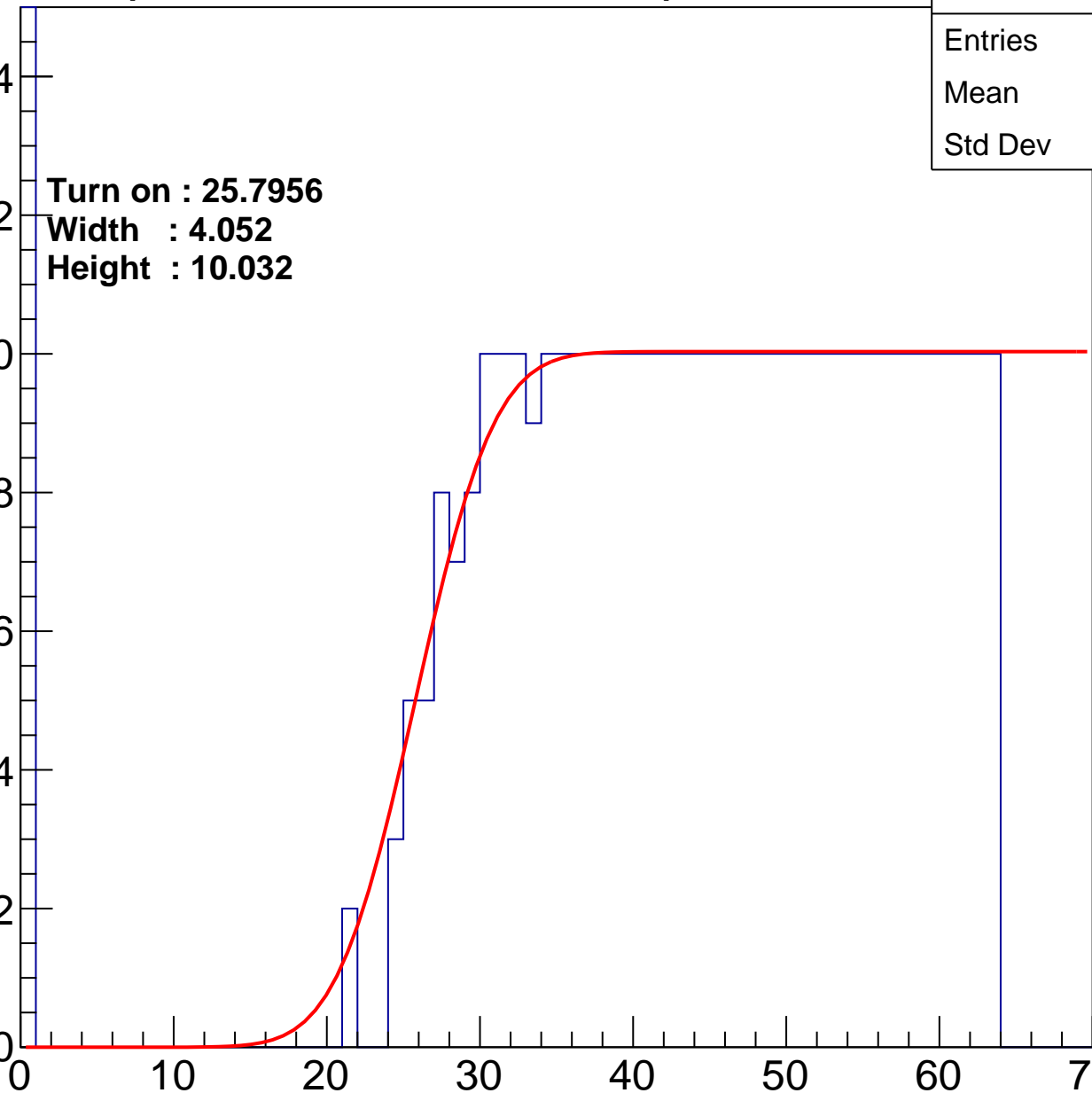
Width : 4.052

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch27

calib_packv5_041523_1651.root, FC#0, port C2

Entries	404
Mean	40.73
Std Dev	16.87

Turn on : 27.5416

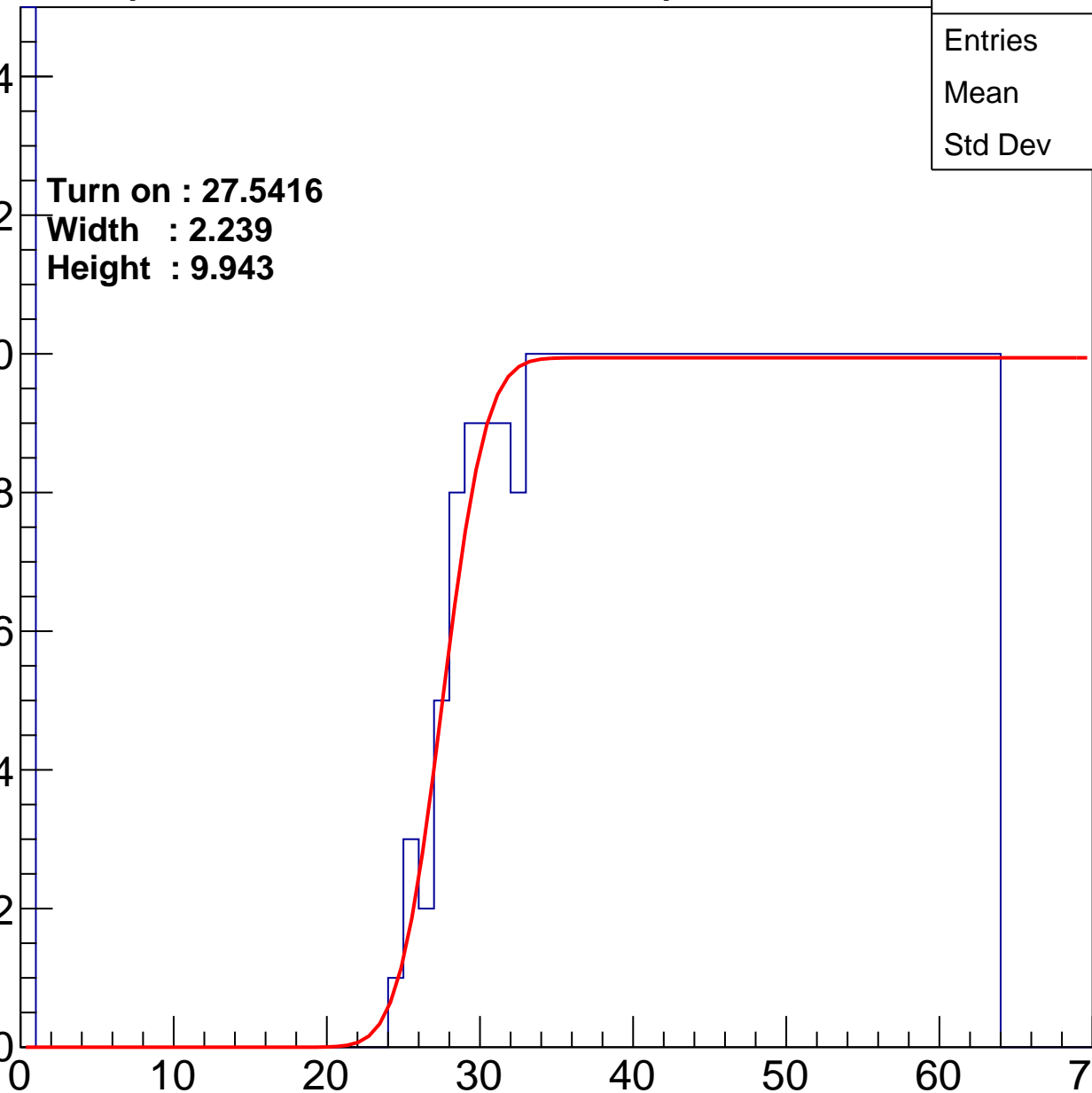
Width : 2.239

Height : 9.943

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch28

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	39.16
Std Dev	17.56

Turn on : 25.9418

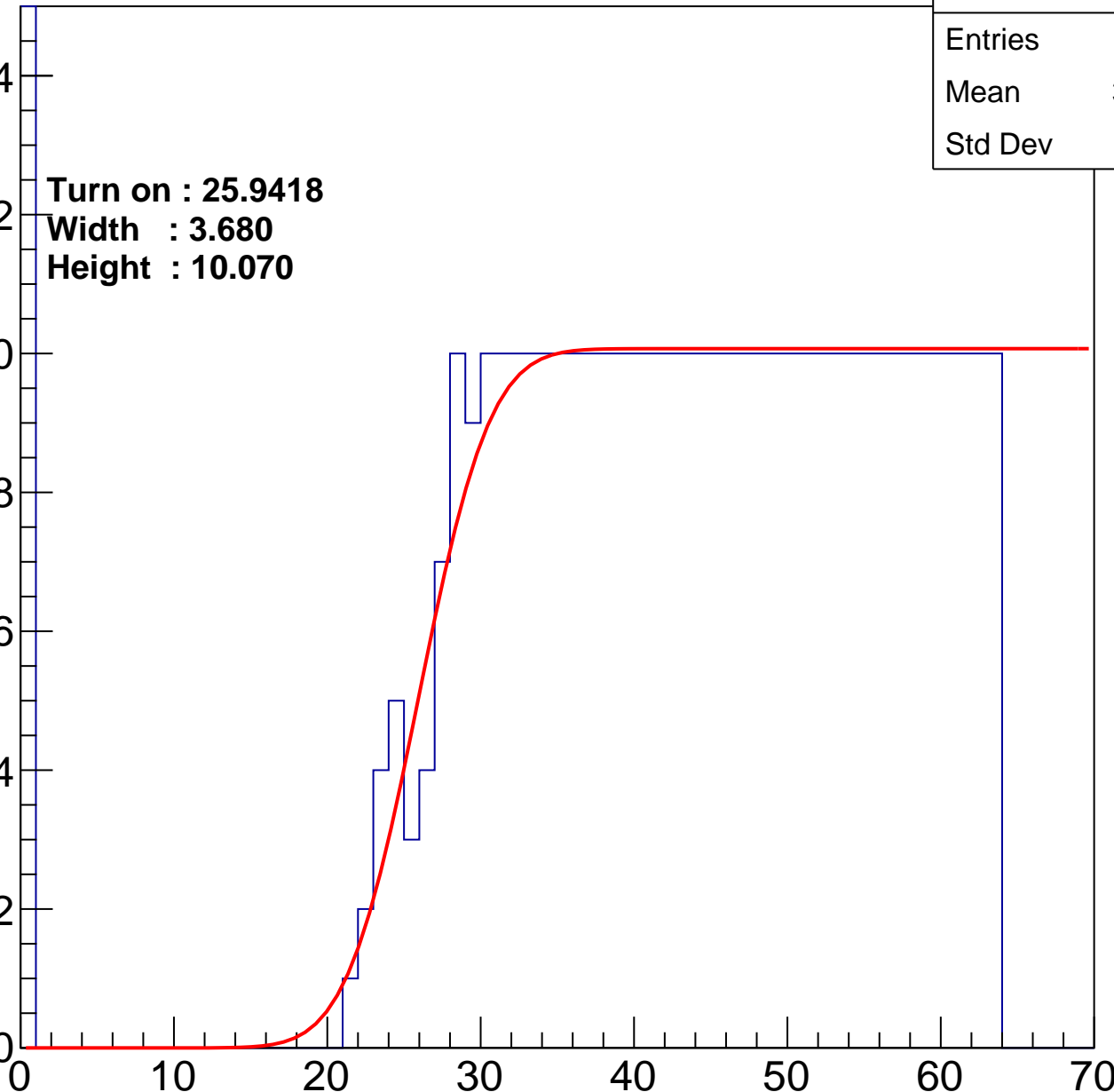
Width : 3.680

Height : 10.070

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch29

calib_packv5_041523_1651.root, FC#0, port C2

Entries	425
Mean	40.07
Std Dev	16.66

Turn on : 25.6178

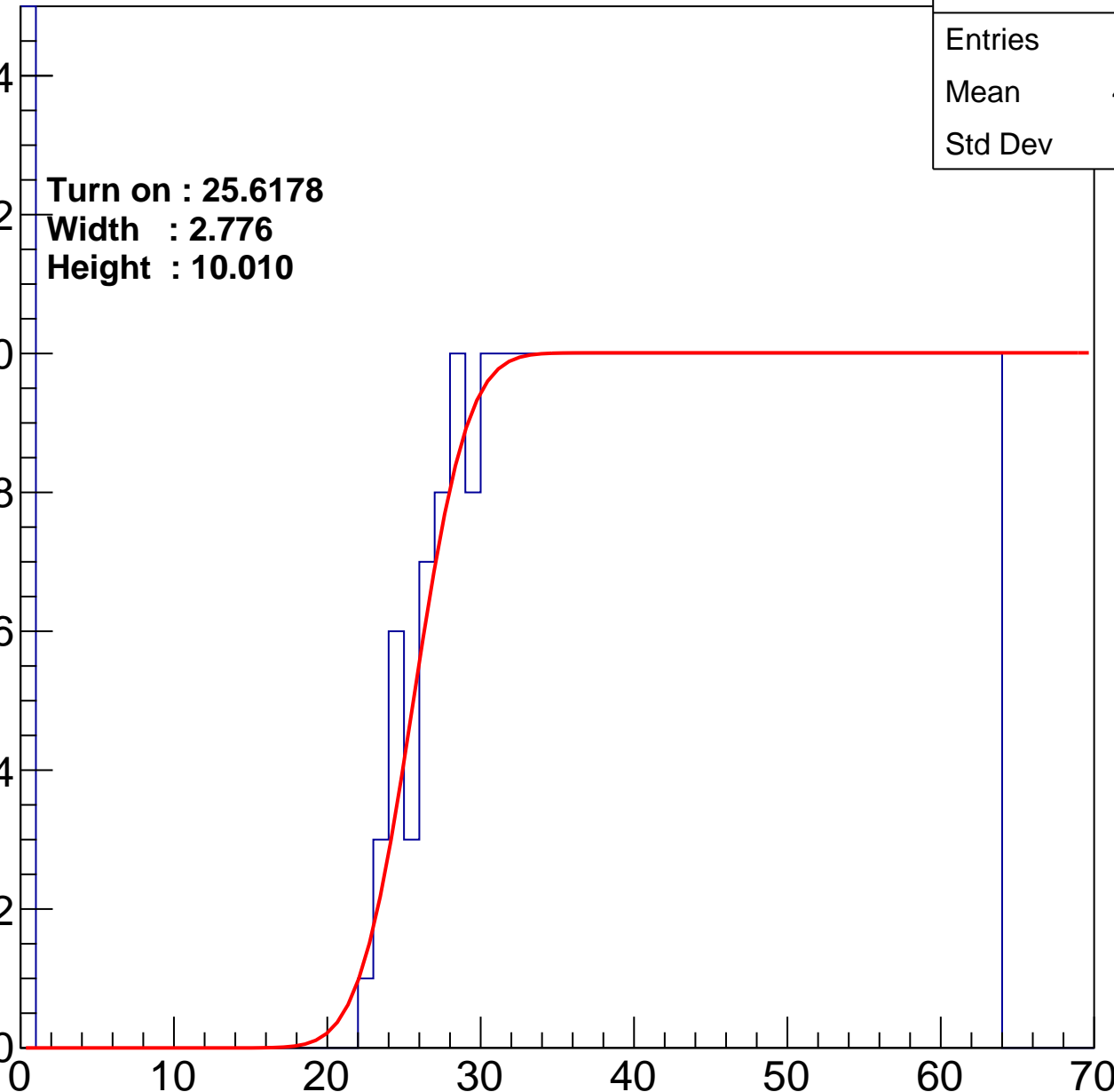
Width : 2.776

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch30

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	38.78
Std Dev	17.69

Turn on : 25.5577

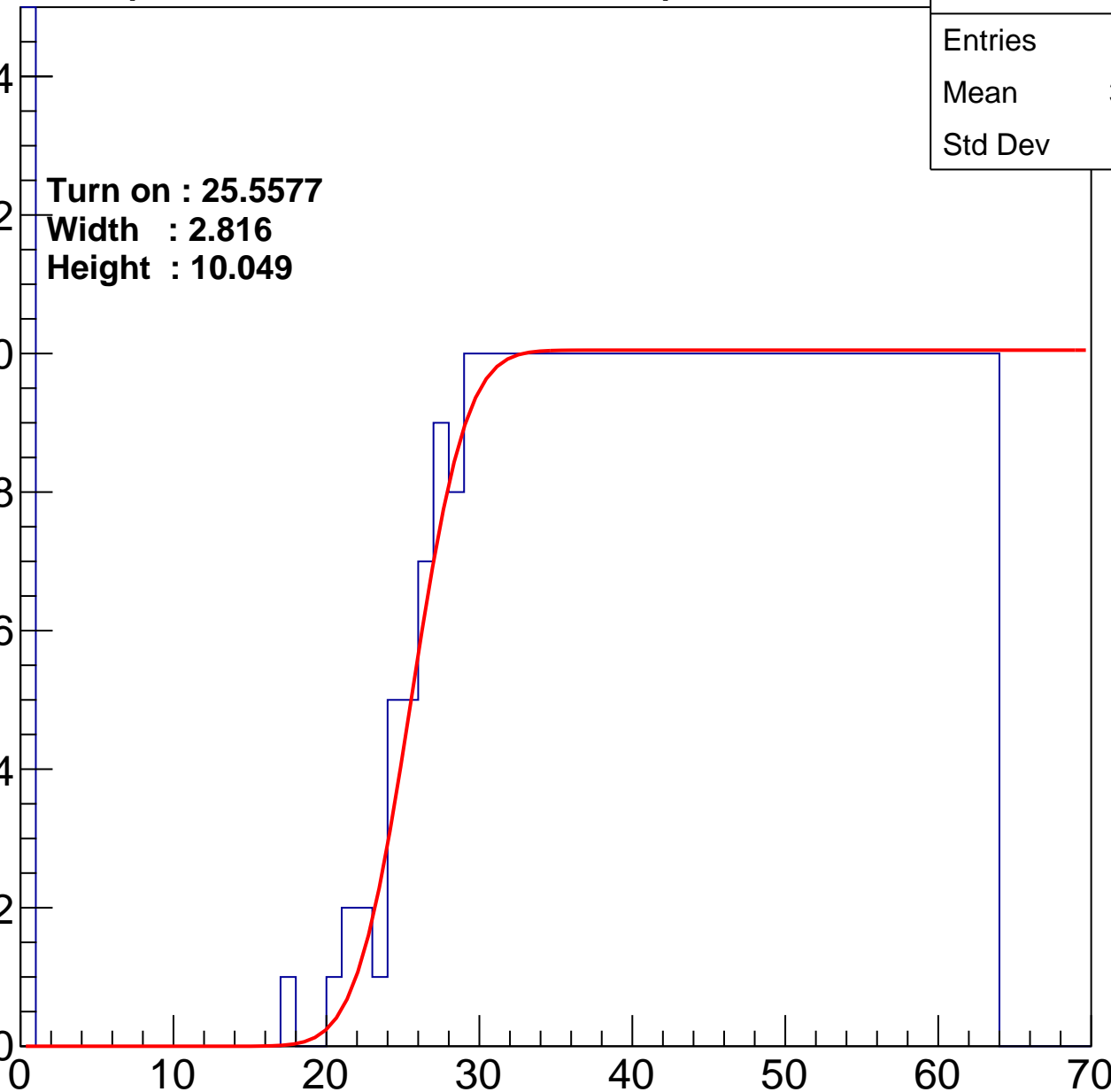
Width : 2.816

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch31

calib_packv5_041523_1651.root, FC#0, port C2

Entries	411
Mean	39.79
Std Dev	17.92

Turn on : 27.9853

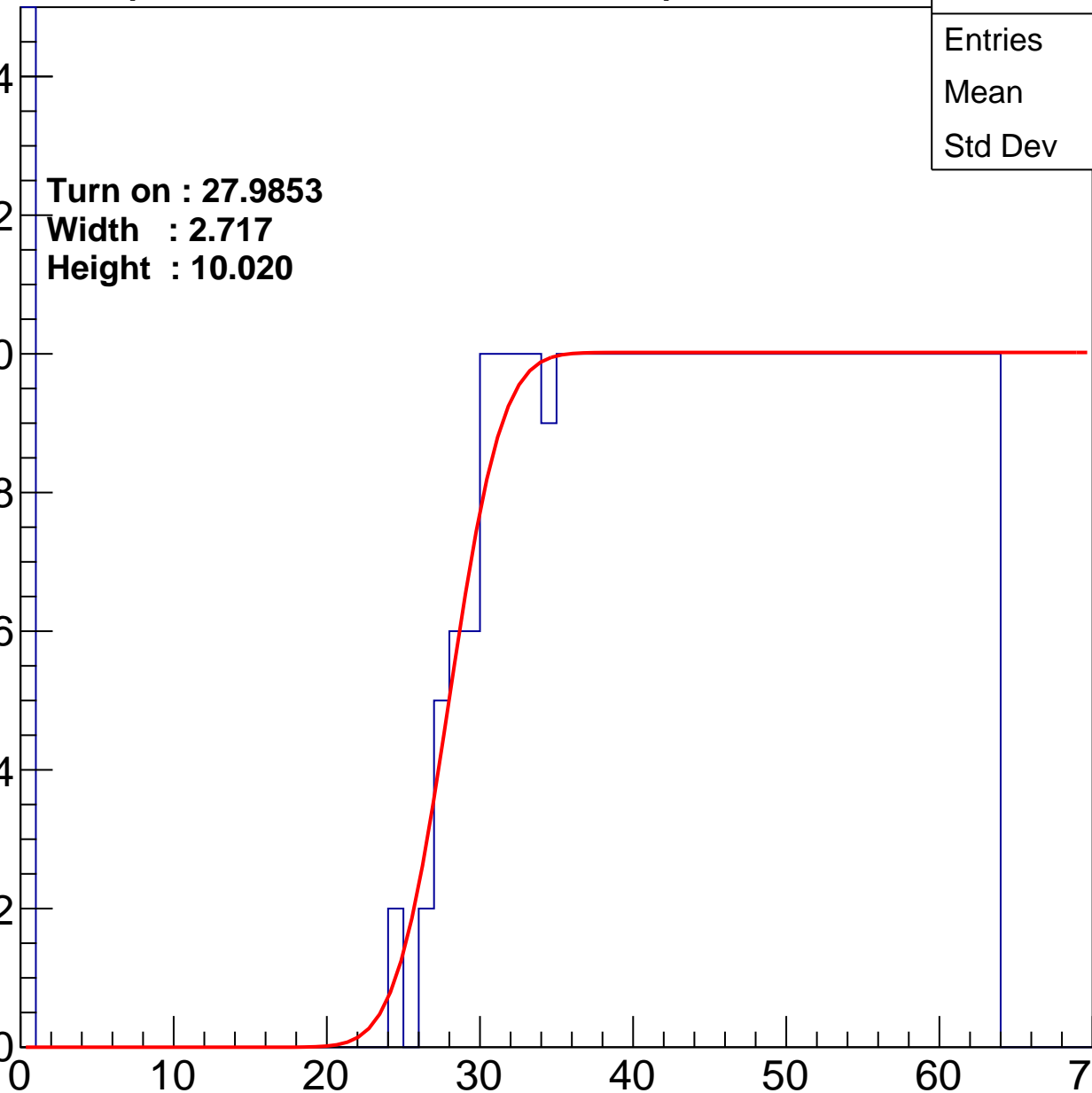
Width : 2.717

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch32

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	39.05
Std Dev	17.41

Turn on : 25.0707

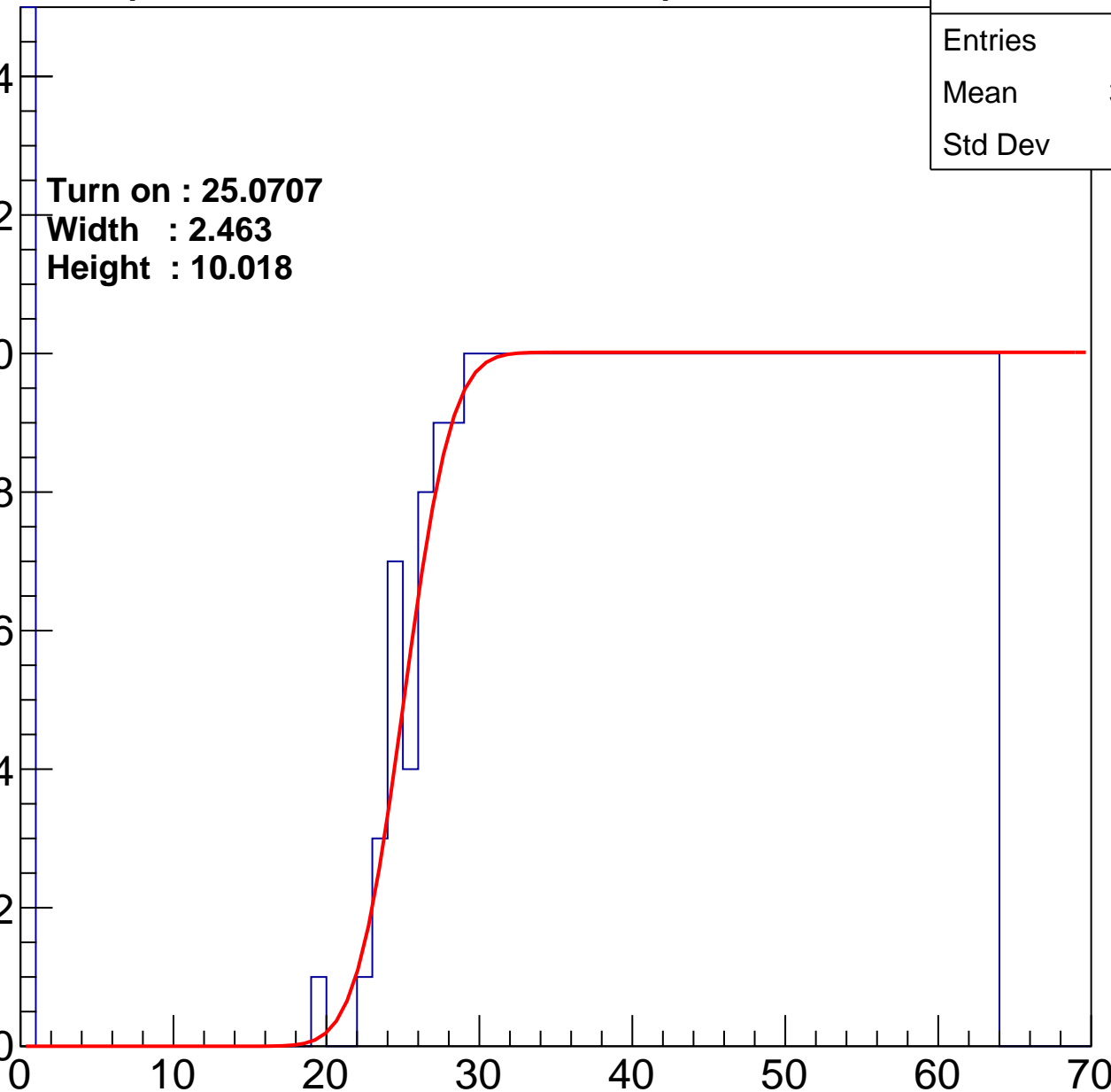
Width : 2.463

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch33

calib_packv5_041523_1651.root, FC#0, port C2

Entries	421
Mean	40.32
Std Dev	16.5

Turn on : 26.7105

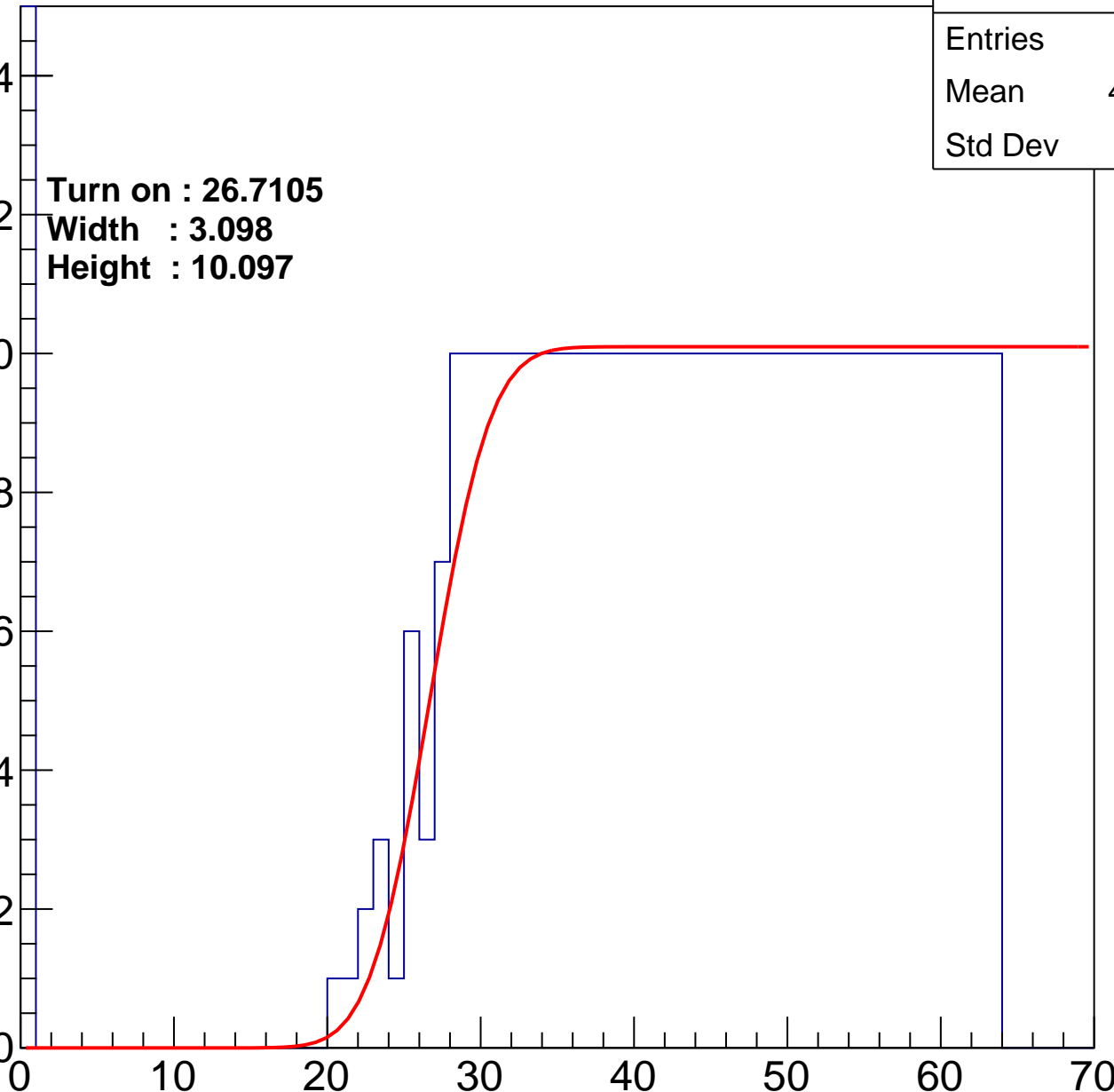
Width : 3.098

Height : 10.097

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch34

calib_packv5_041523_1651.root, FC#0, port C2

Entries	456
Mean	38.85
Std Dev	16.88

Turn on : 22.4767

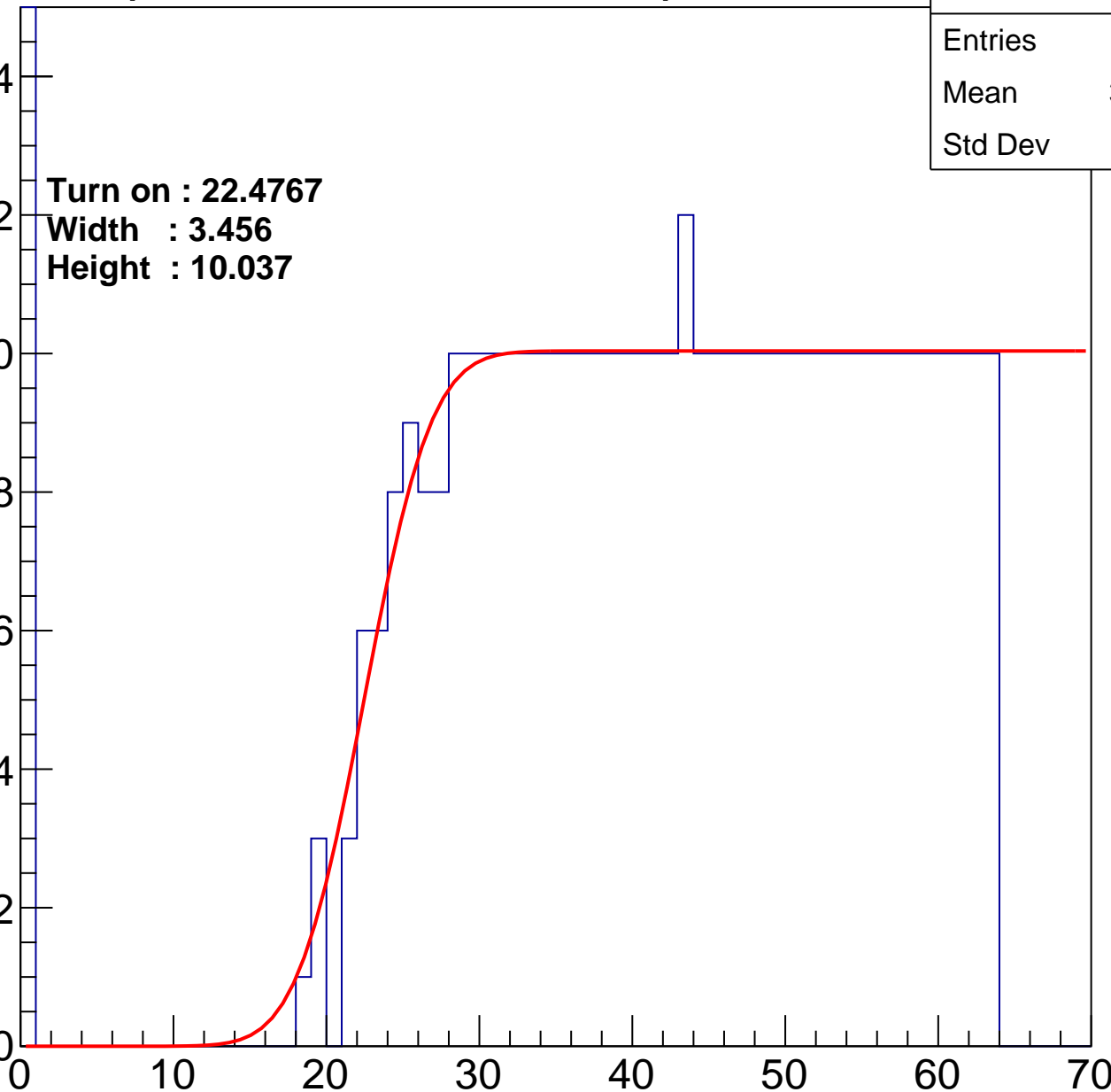
Width : 3.456

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch35

calib_packv5_041523_1651.root, FC#0, port C2

Entries	410
Mean	39.97
Std Dev	17.72

Turn on : 27.7458

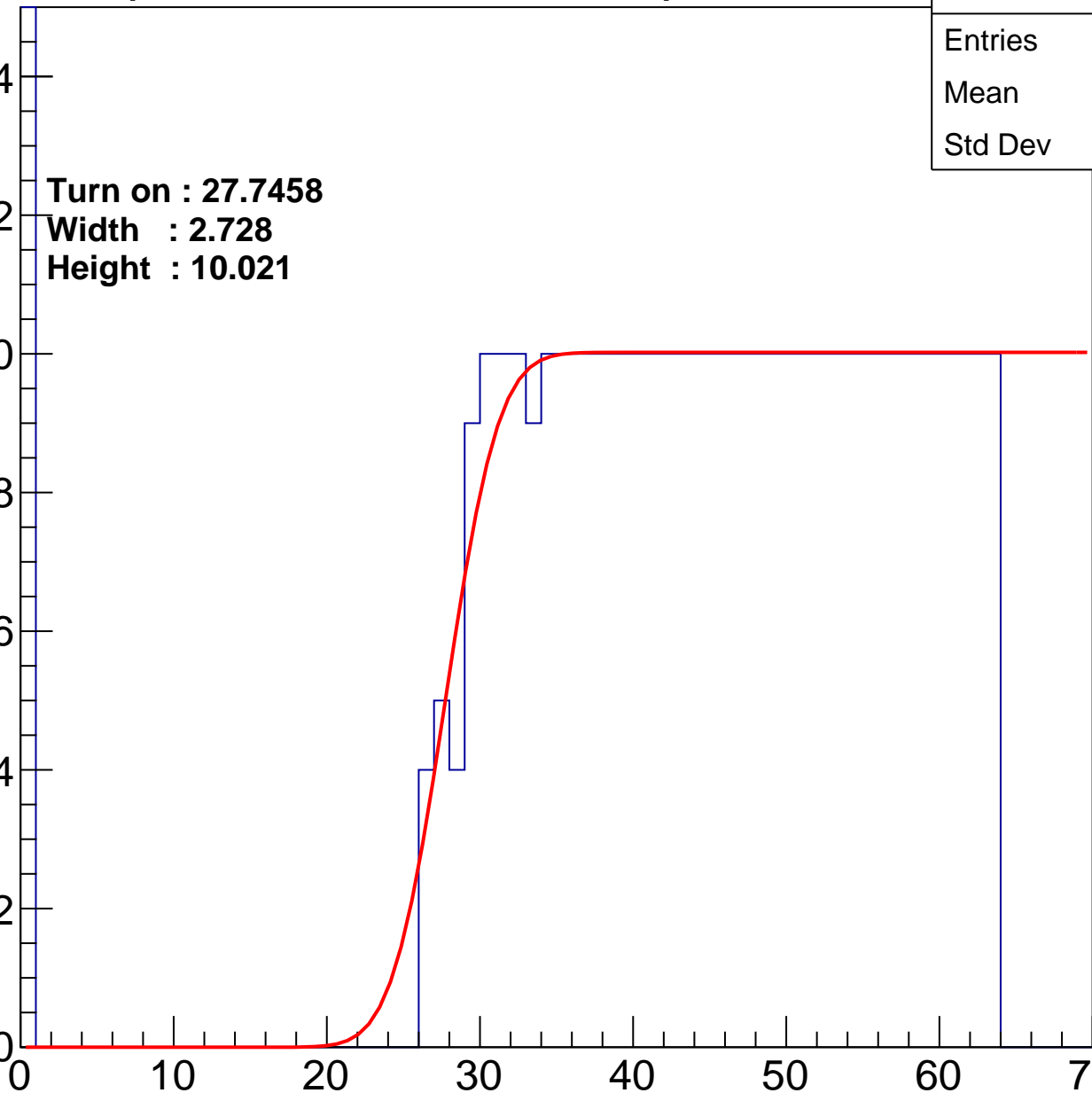
Width : 2.728

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch36

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	39.35
Std Dev	16.78

Turn on : 23.7496

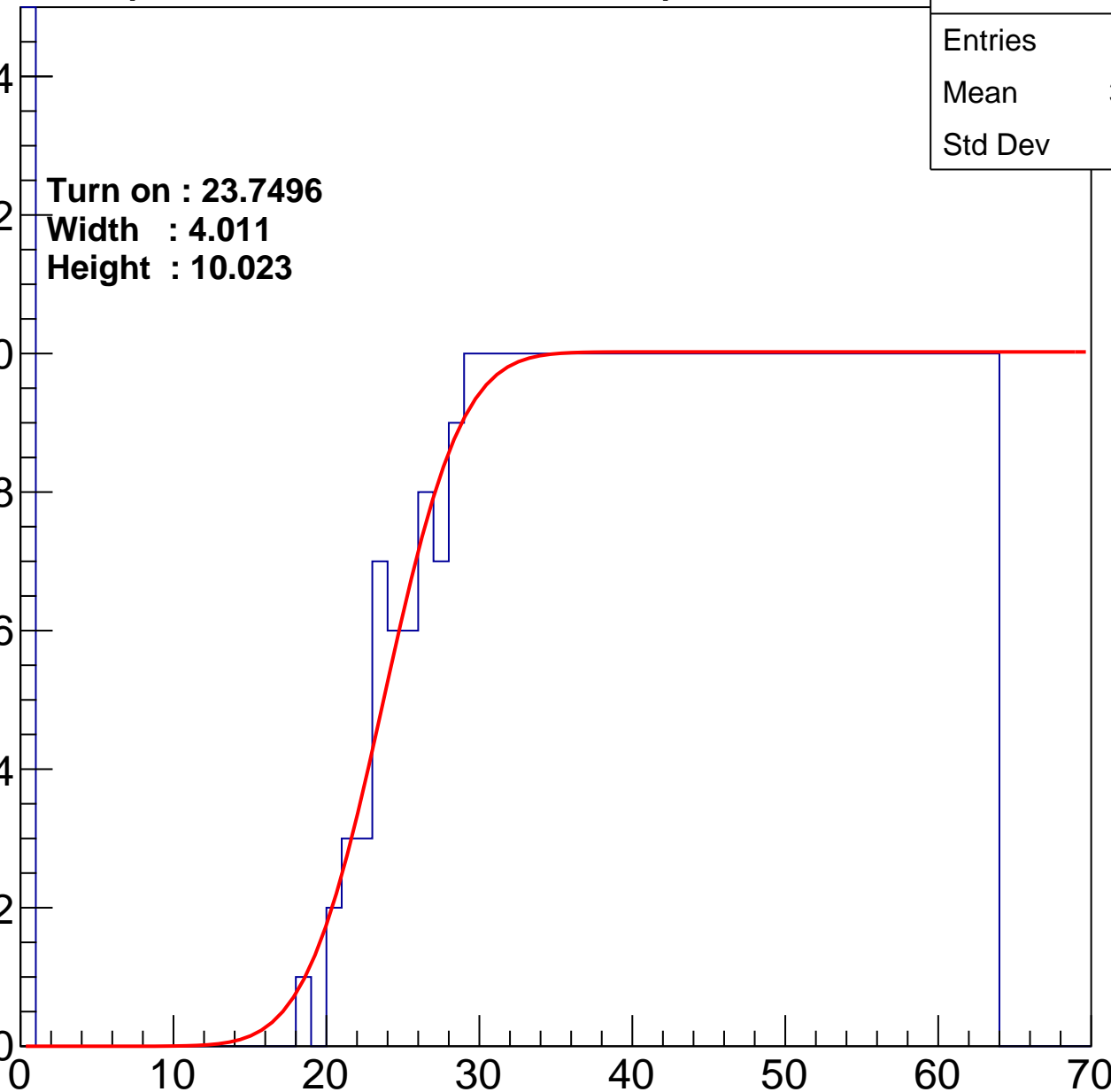
Width : 4.011

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch37

calib_packv5_041523_1651.root, FC#0, port C2

Entries	410
Mean	39.78
Std Dev	18.03

Turn on : 28.8128

Width : 3.140

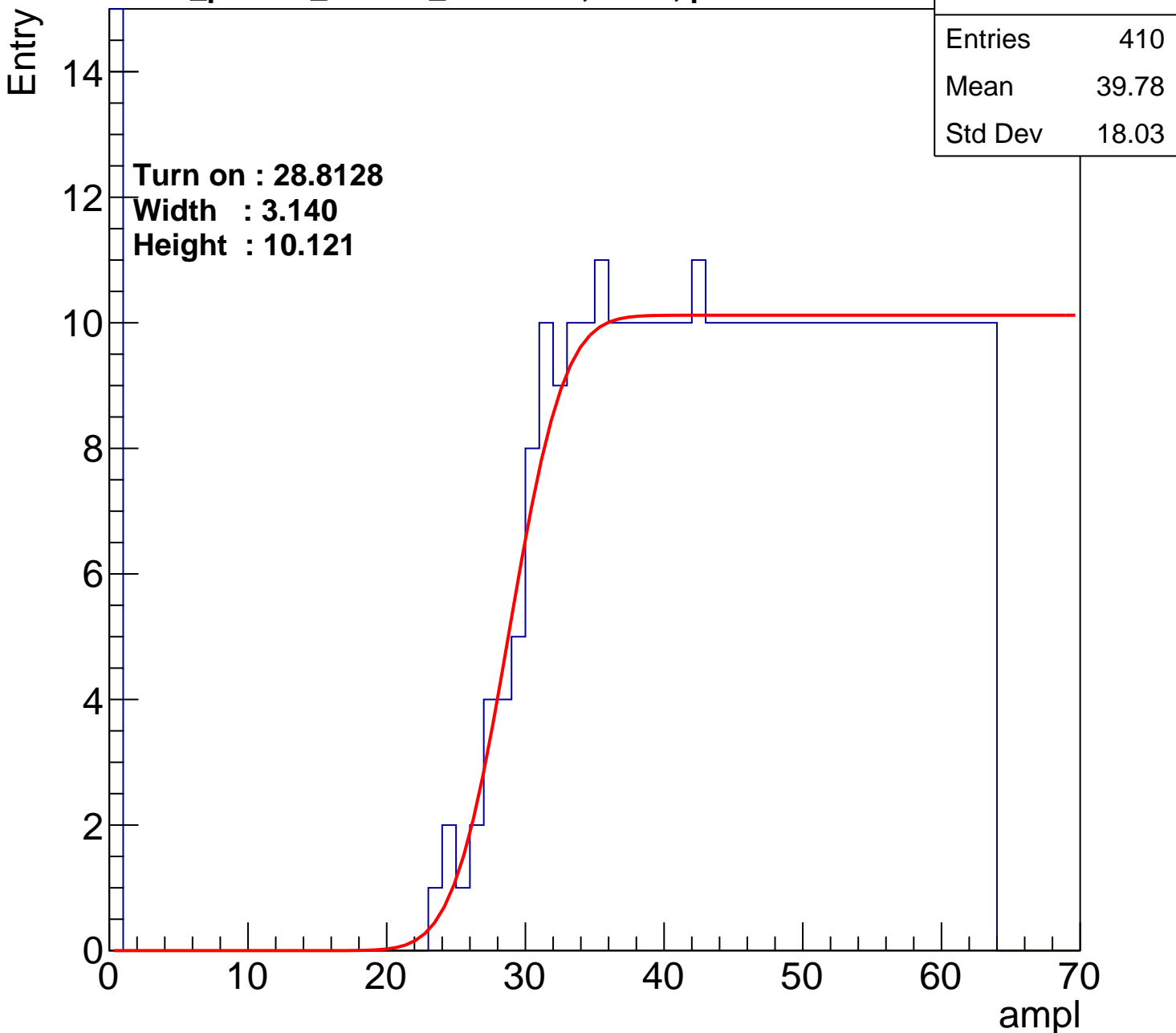
Height : 10.121

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U21-ch38

calib_packv5_041523_1651.root, FC#0, port C2

Entries	457
Mean	38.49
Std Dev	17.29

Turn on : 22.9728

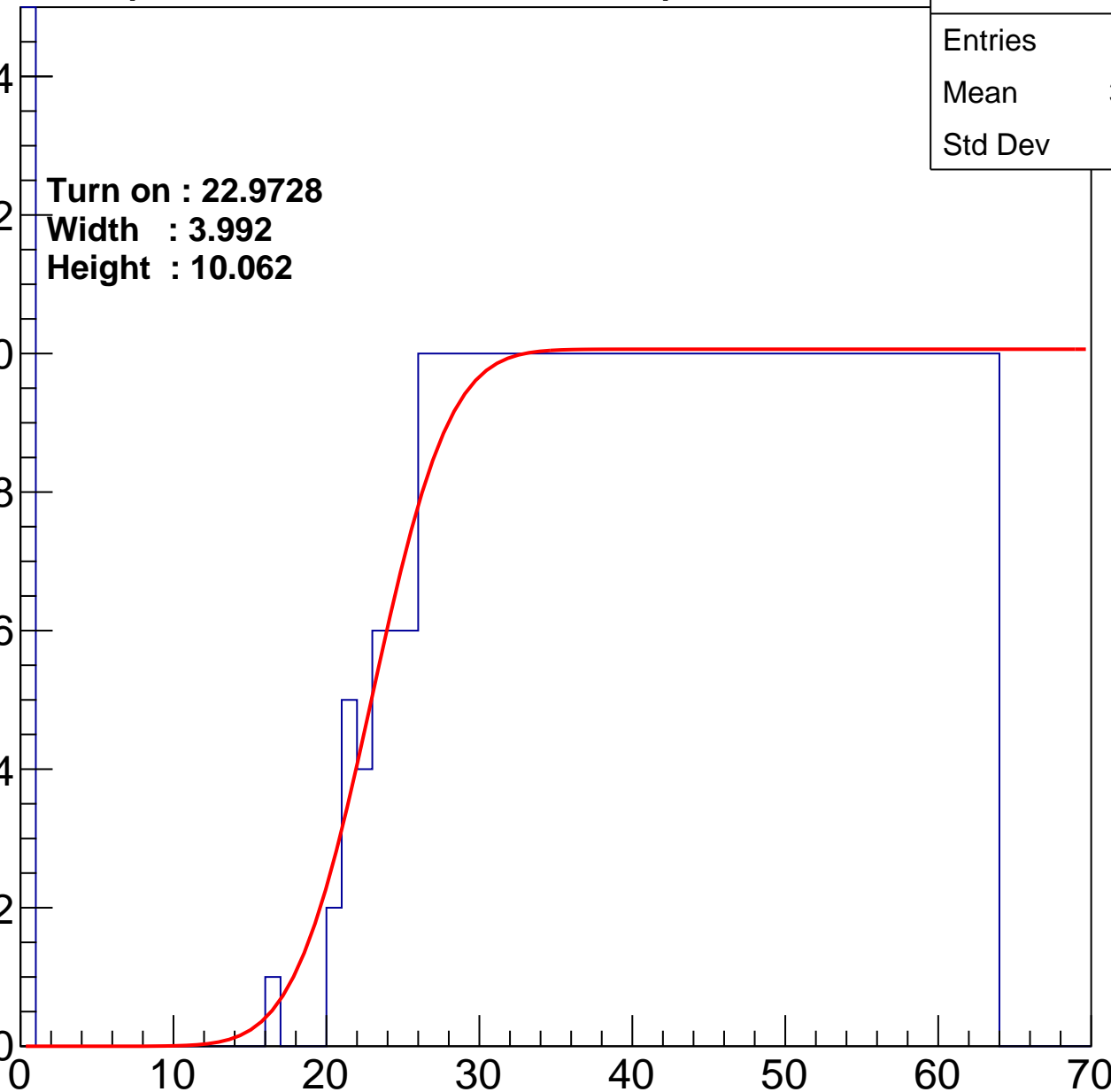
Width : 3.992

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch39

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	38.95
Std Dev	17.63

Turn on : 25.4058

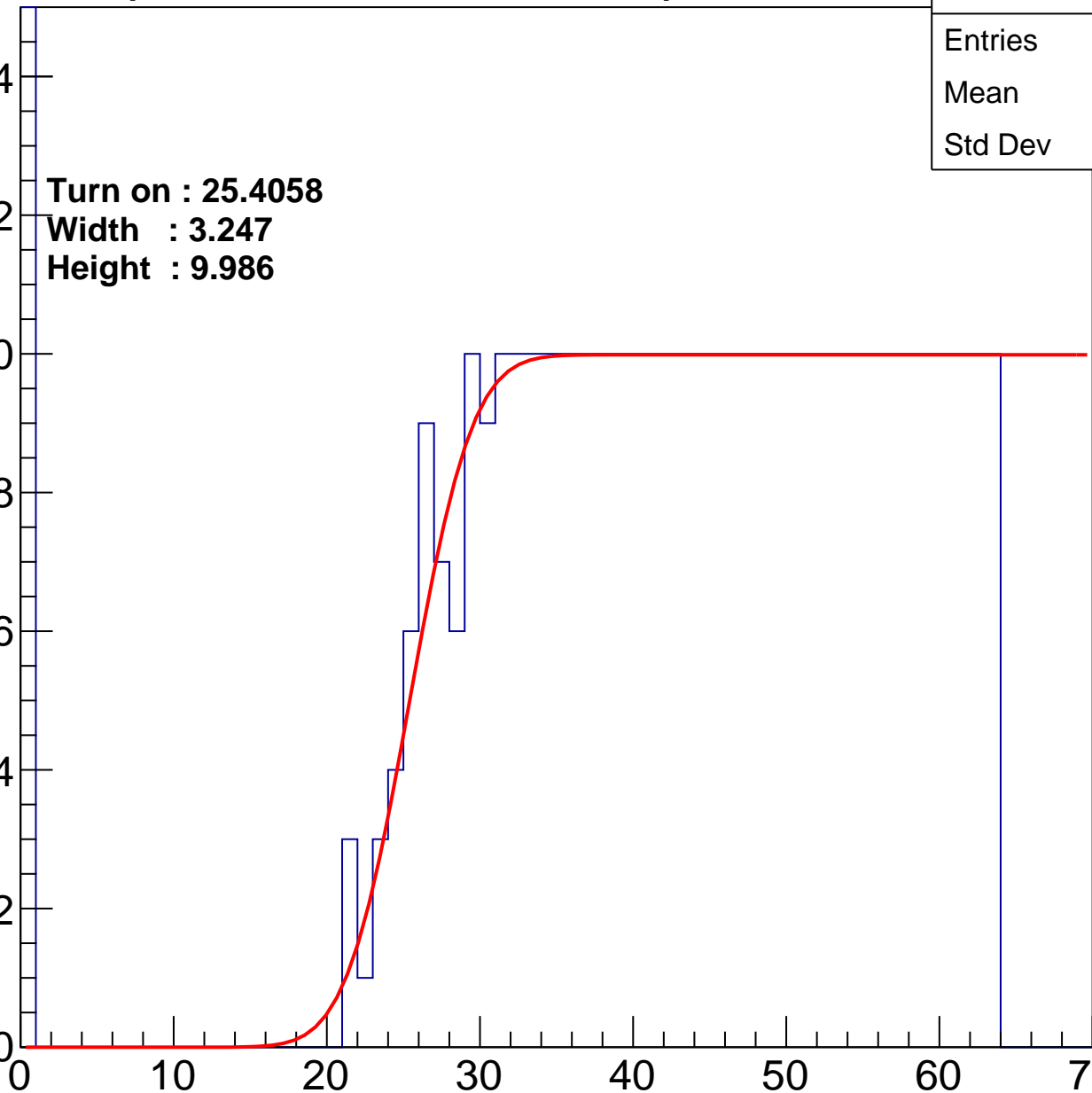
Width : 3.247

Height : 9.986

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch40

calib_packv5_041523_1651.root, FC#0, port C2

Entries	441
Mean	39.35
Std Dev	17.17

Turn on : 24.9023

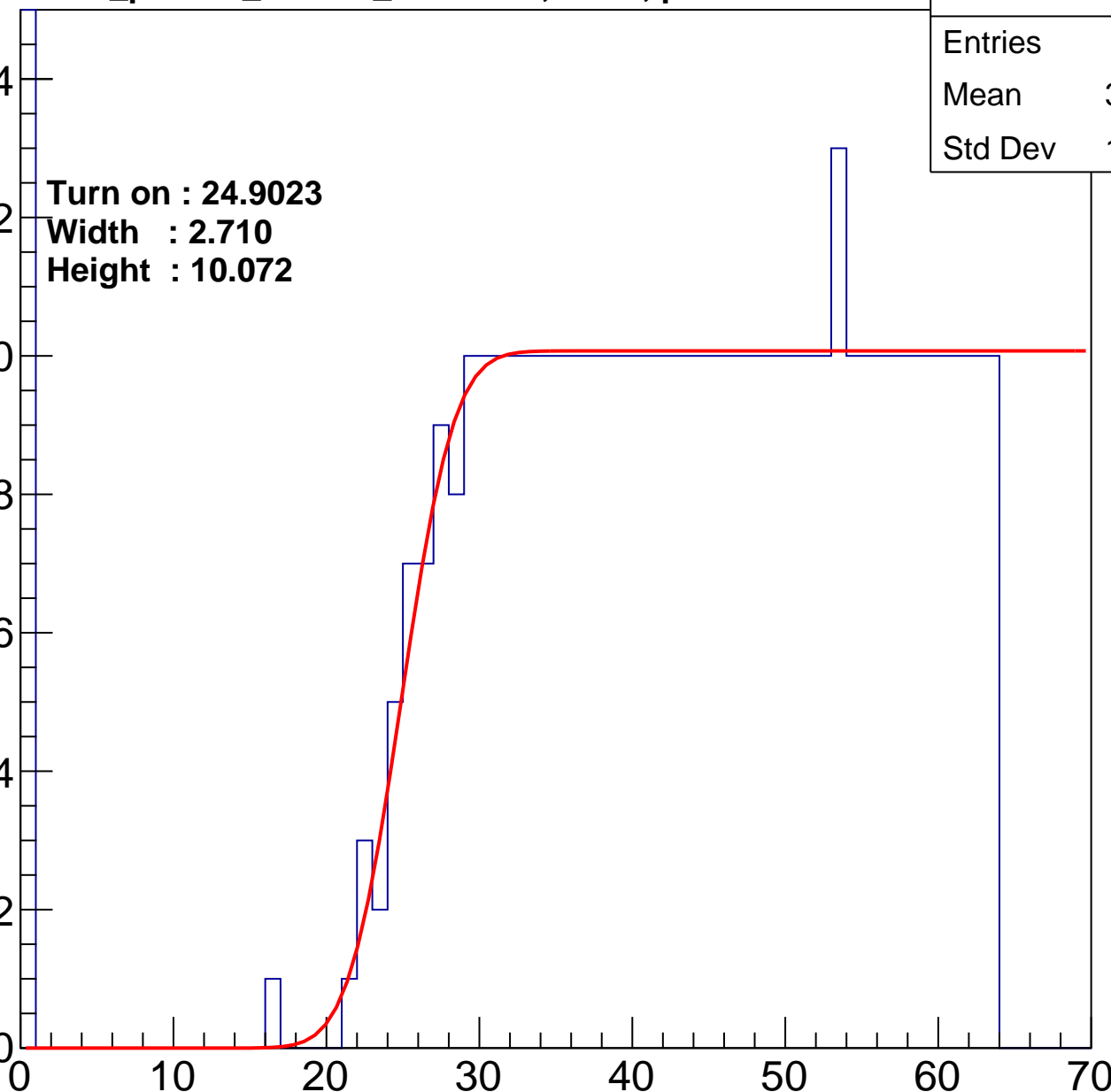
Width : 2.710

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch41

calib_packv5_041523_1651.root, FC#0, port C2

Entries	413
Mean	40.64
Std Dev	16.72

Turn on : 26.6274

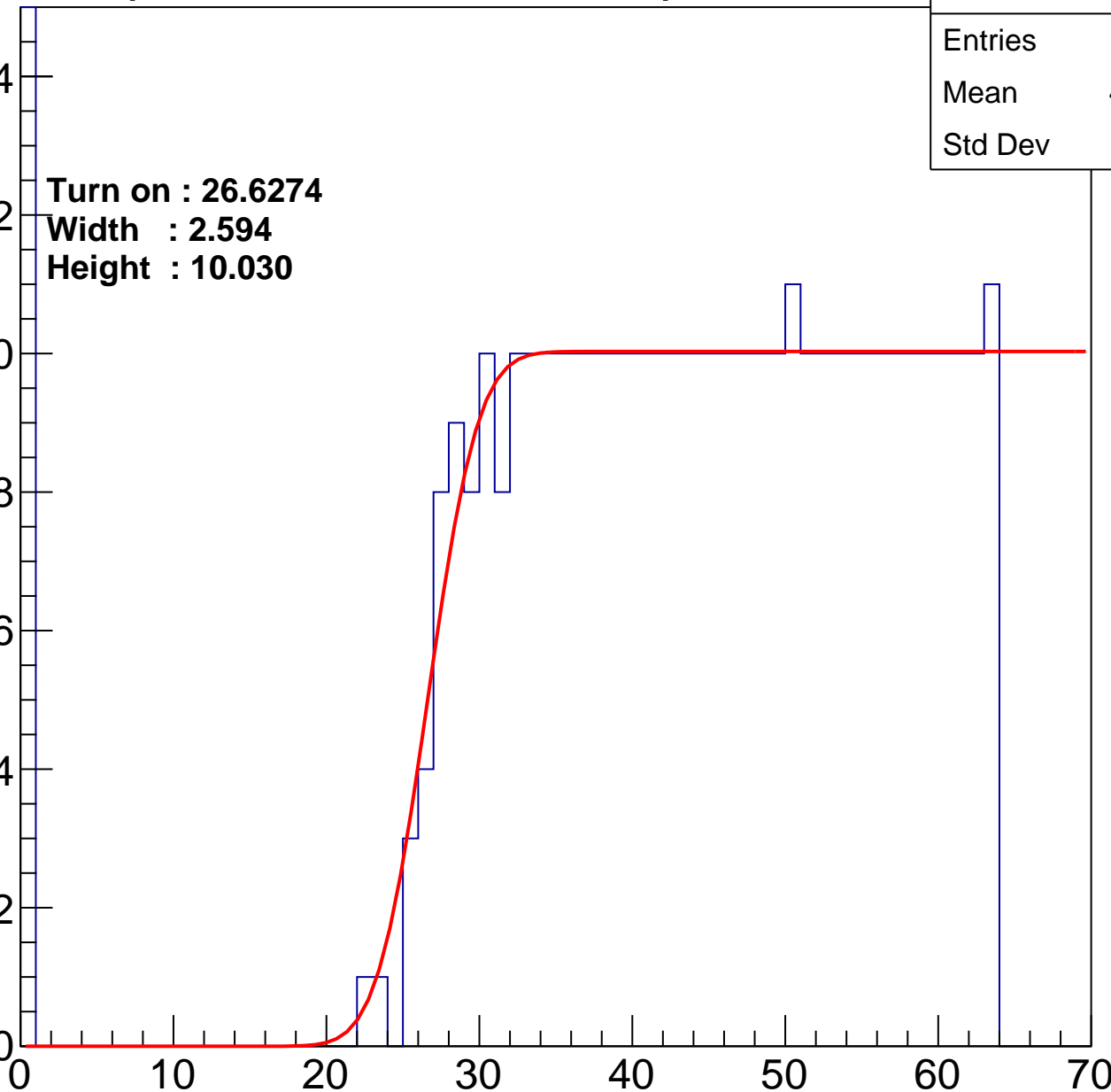
Width : 2.594

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch42

calib_packv5_041523_1651.root, FC#0, port C2

Entries	451
Mean	38.67
Std Dev	17.34

Turn on : 23.7532

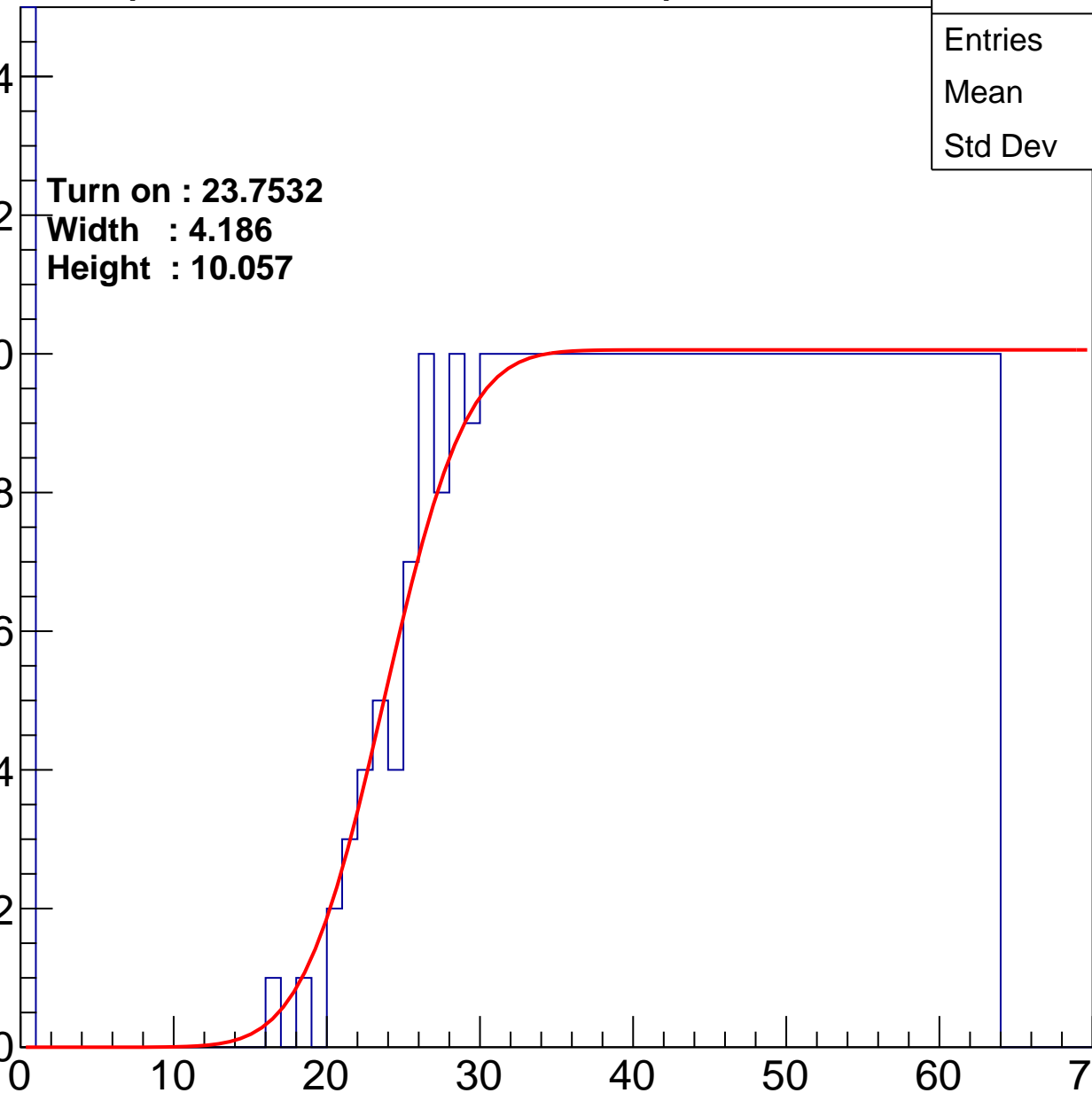
Width : 4.186

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch43

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	38.87
Std Dev	17.98

Turn on : 26.0820

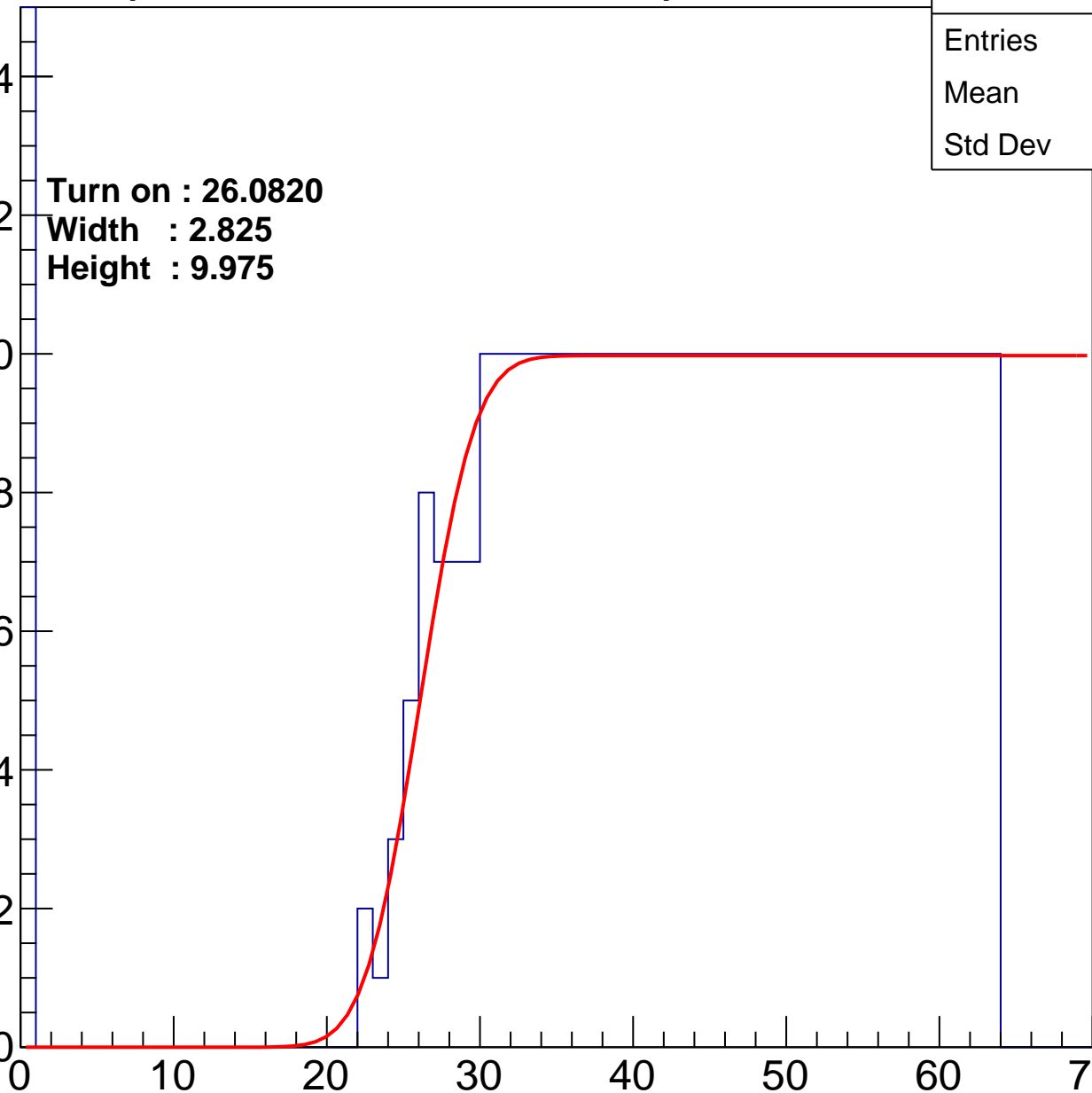
Width : 2.825

Height : 9.975

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch44

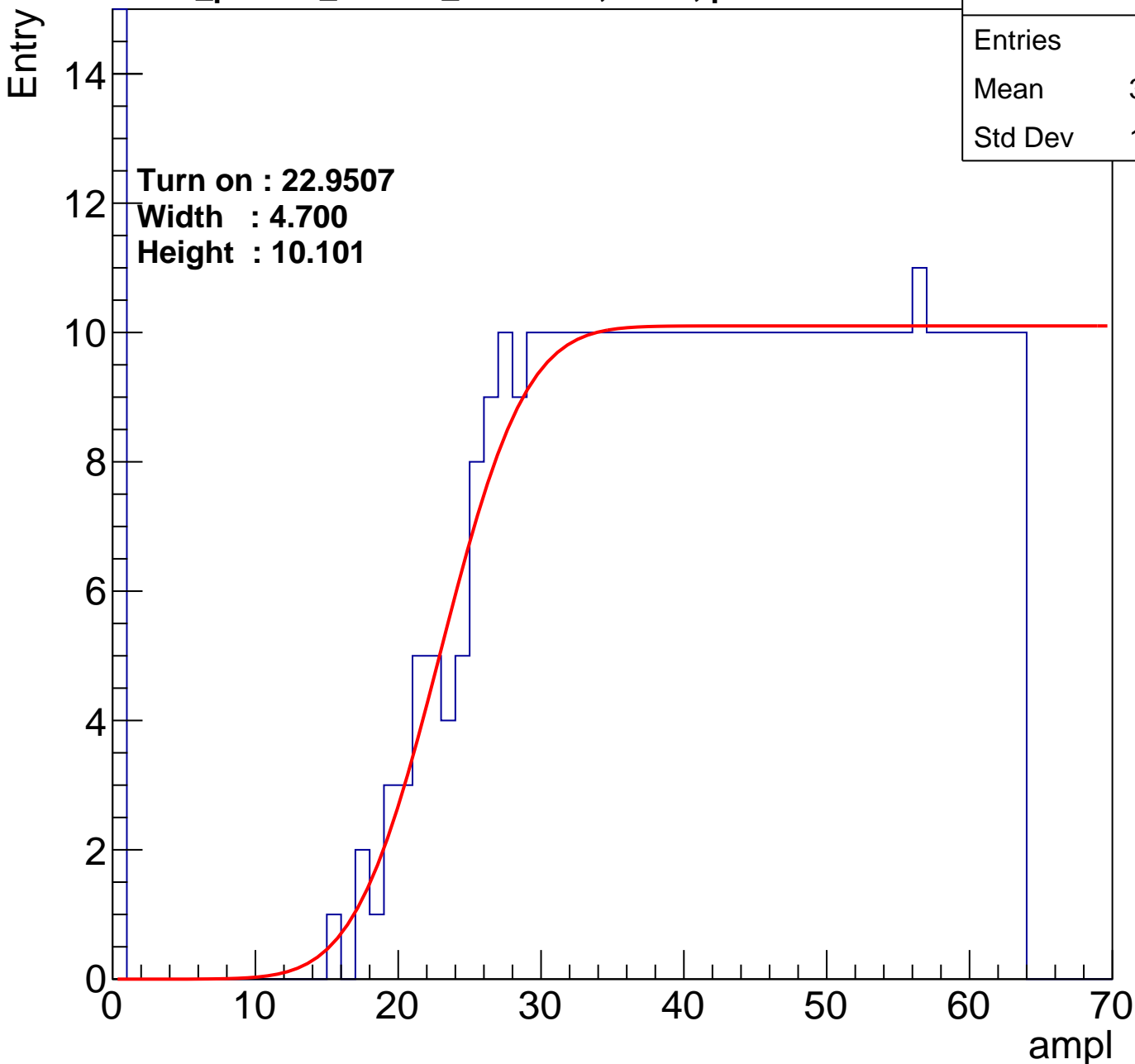
calib_packv5_041523_1651.root, FC#0, port C2

Entries	460
Mean	38.53
Std Dev	17.14

Turn on : 22.9507

Width : 4.700

Height : 10.101



B1L103S, U21-ch45

calib_packv5_041523_1651.root, FC#0, port C2

Entries	425
Mean	39.7
Std Dev	17.38

Turn on : 26.7347

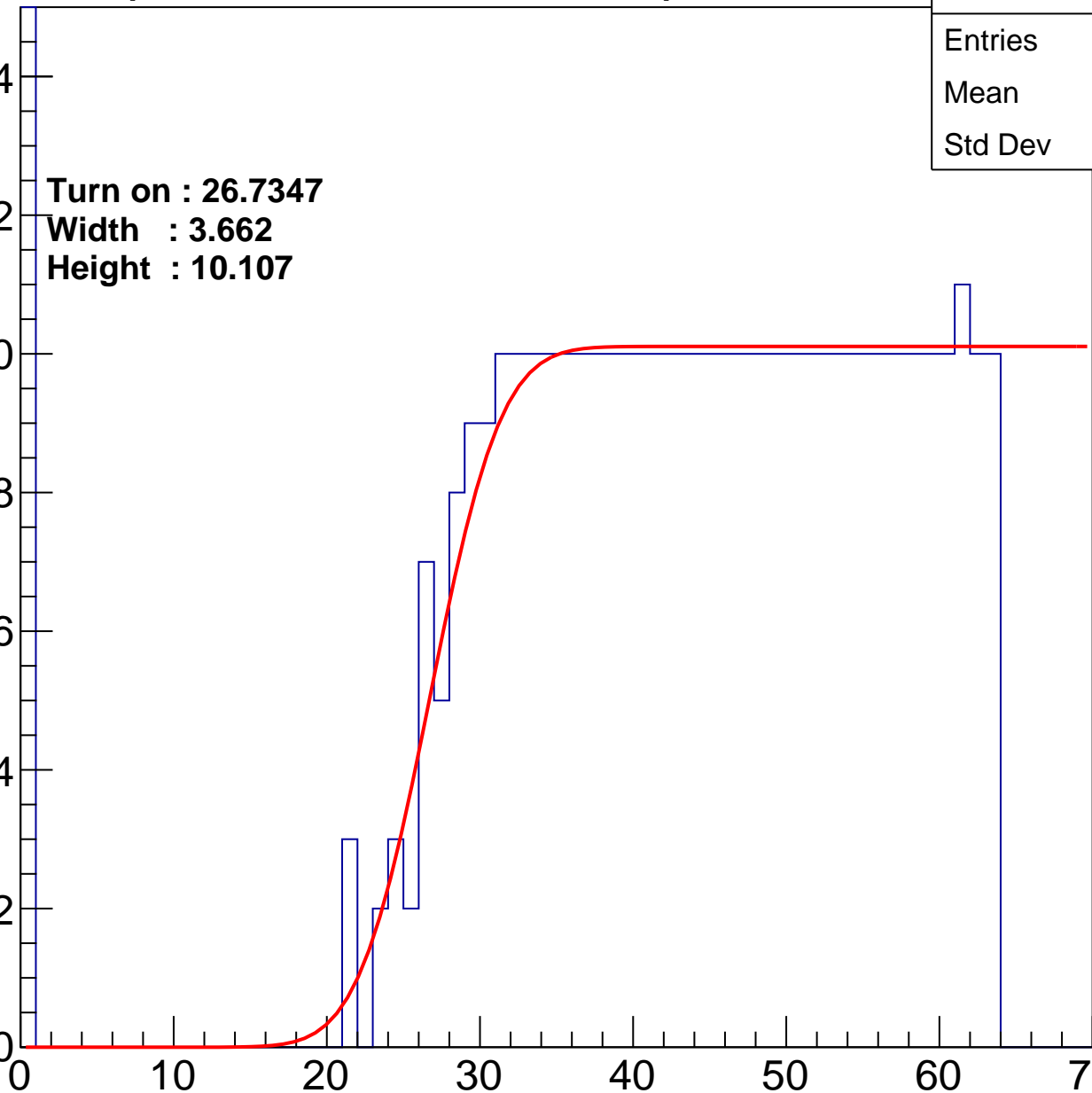
Width : 3.662

Height : 10.107

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch46

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	39.86
Std Dev	16.63

Turn on : 24.9169

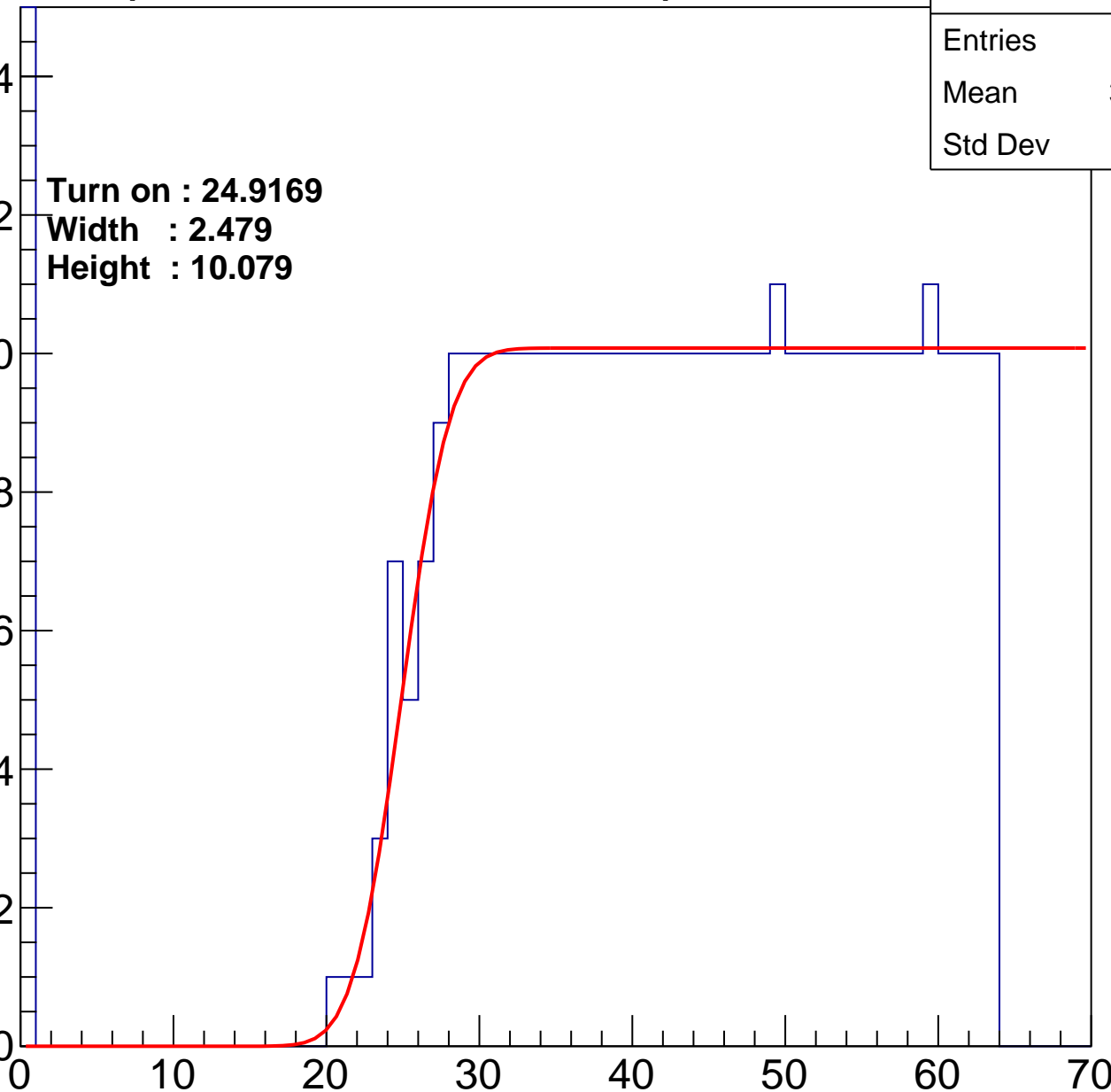
Width : 2.479

Height : 10.079

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch47

calib_packv5_041523_1651.root, FC#0, port C2

Entries	411
Mean	40.89
Std Dev	16.39

Turn on : 27.1299

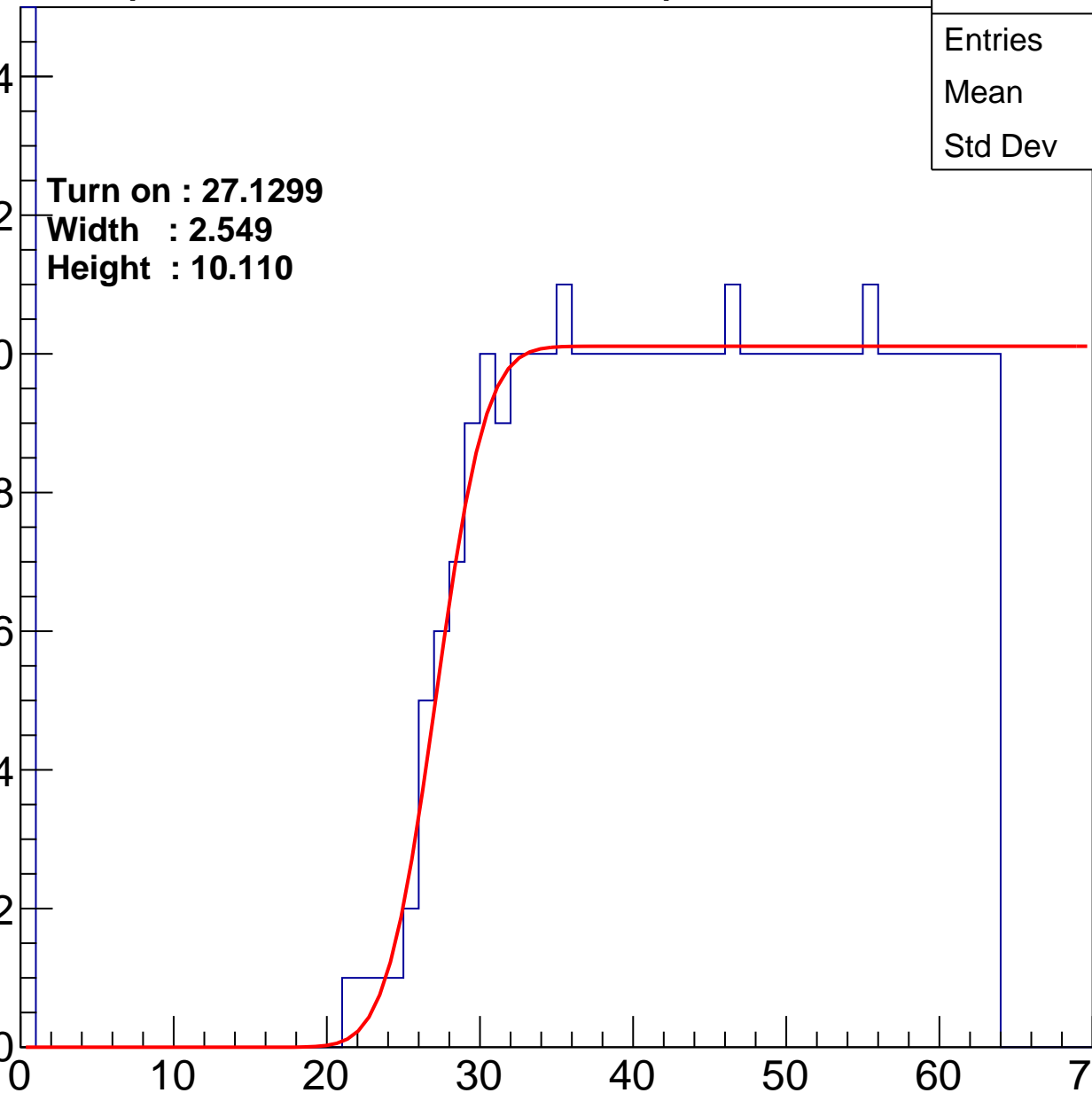
Width : 2.549

Height : 10.110

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch48

calib_packv5_041523_1651.root, FC#0, port C2

Entries	450
Mean	38.66
Std Dev	17.44

Turn on : 23.5249

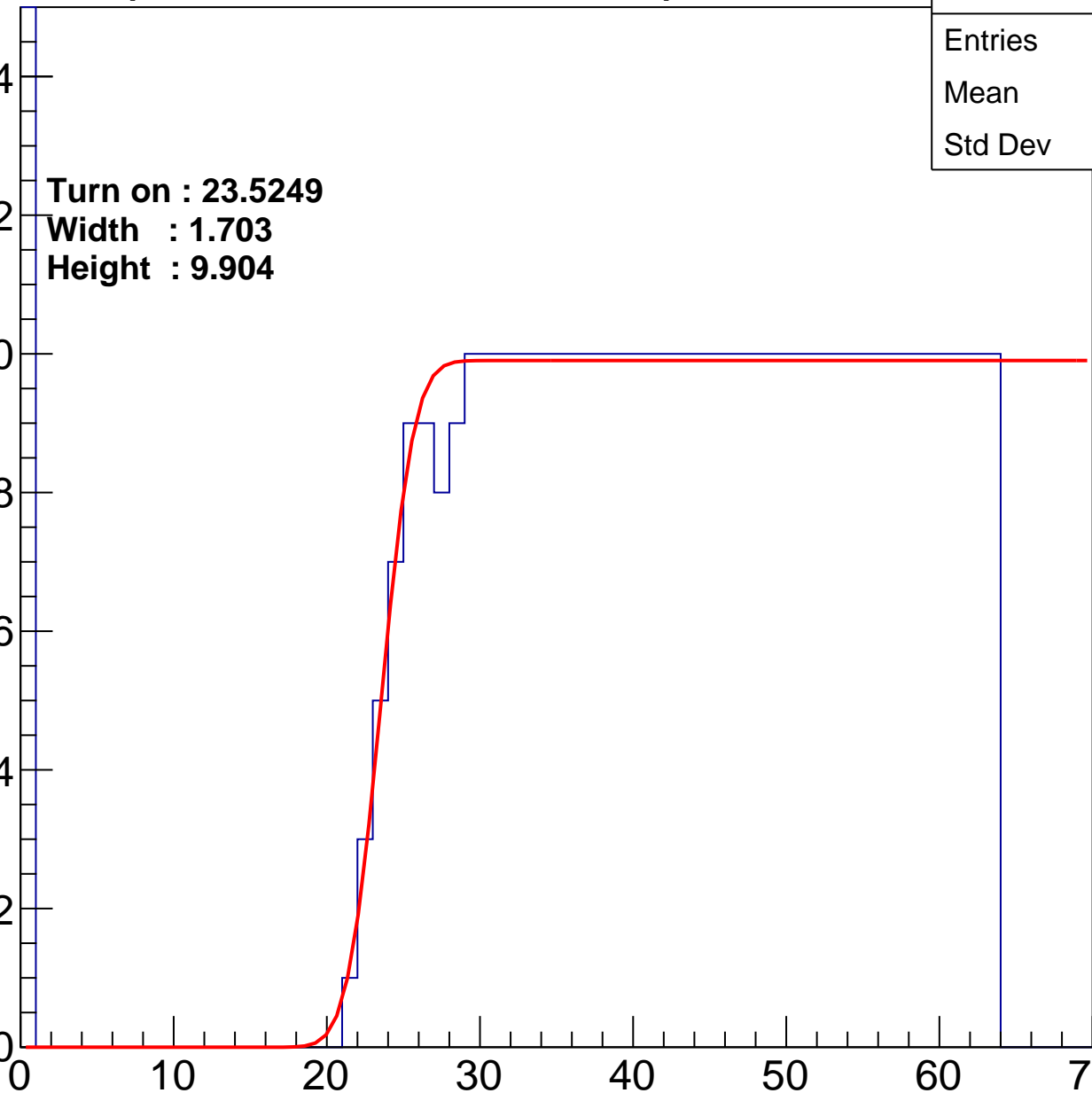
Width : 1.703

Height : 9.904

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch49

calib_packv5_041523_1651.root, FC#0, port C2

Entries	427
Mean	39.21
Std Dev	17.87

Turn on : 26.5772

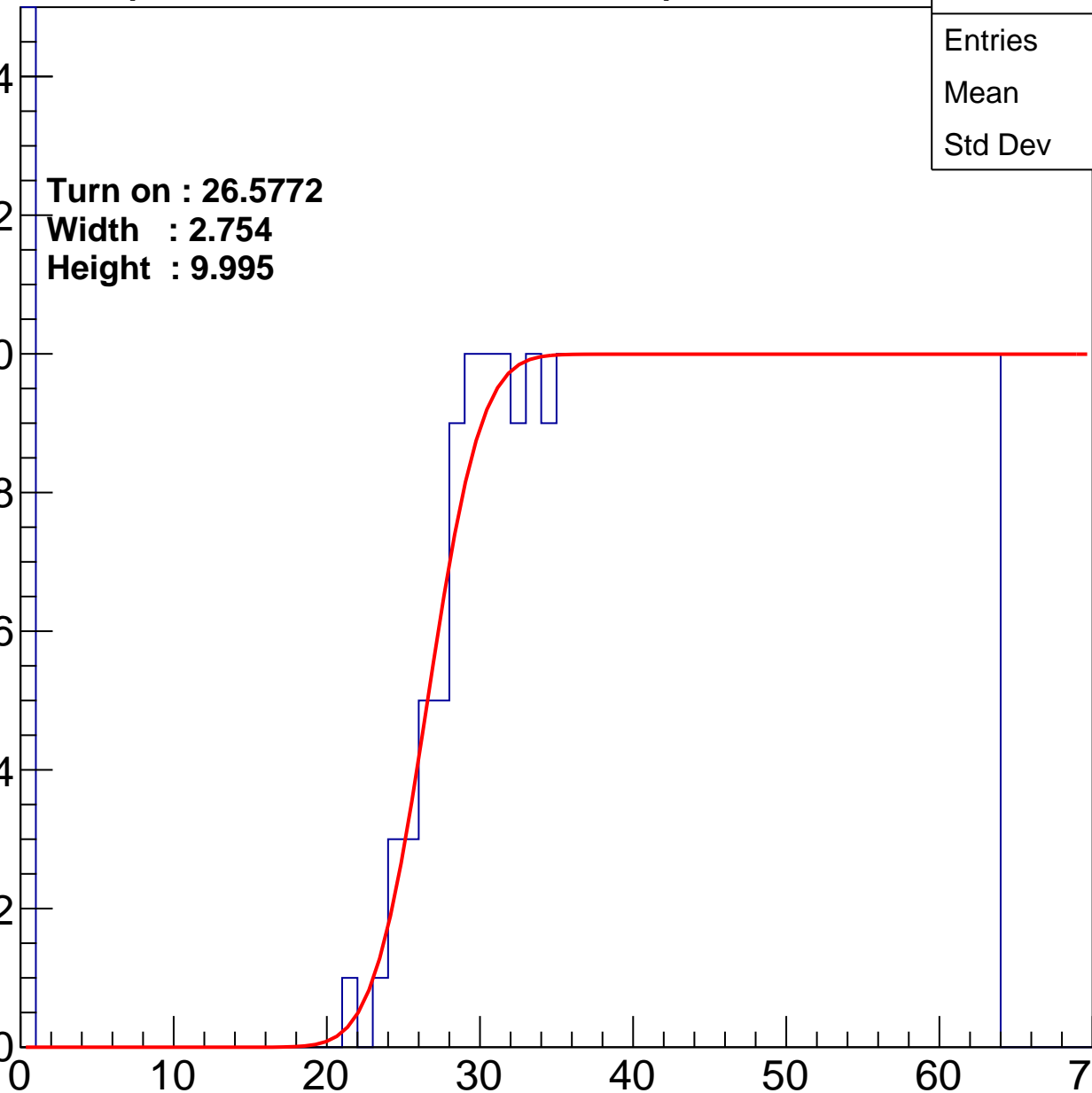
Width : 2.754

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch50

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	39.05
Std Dev	17.31

Turn on : 24.7091

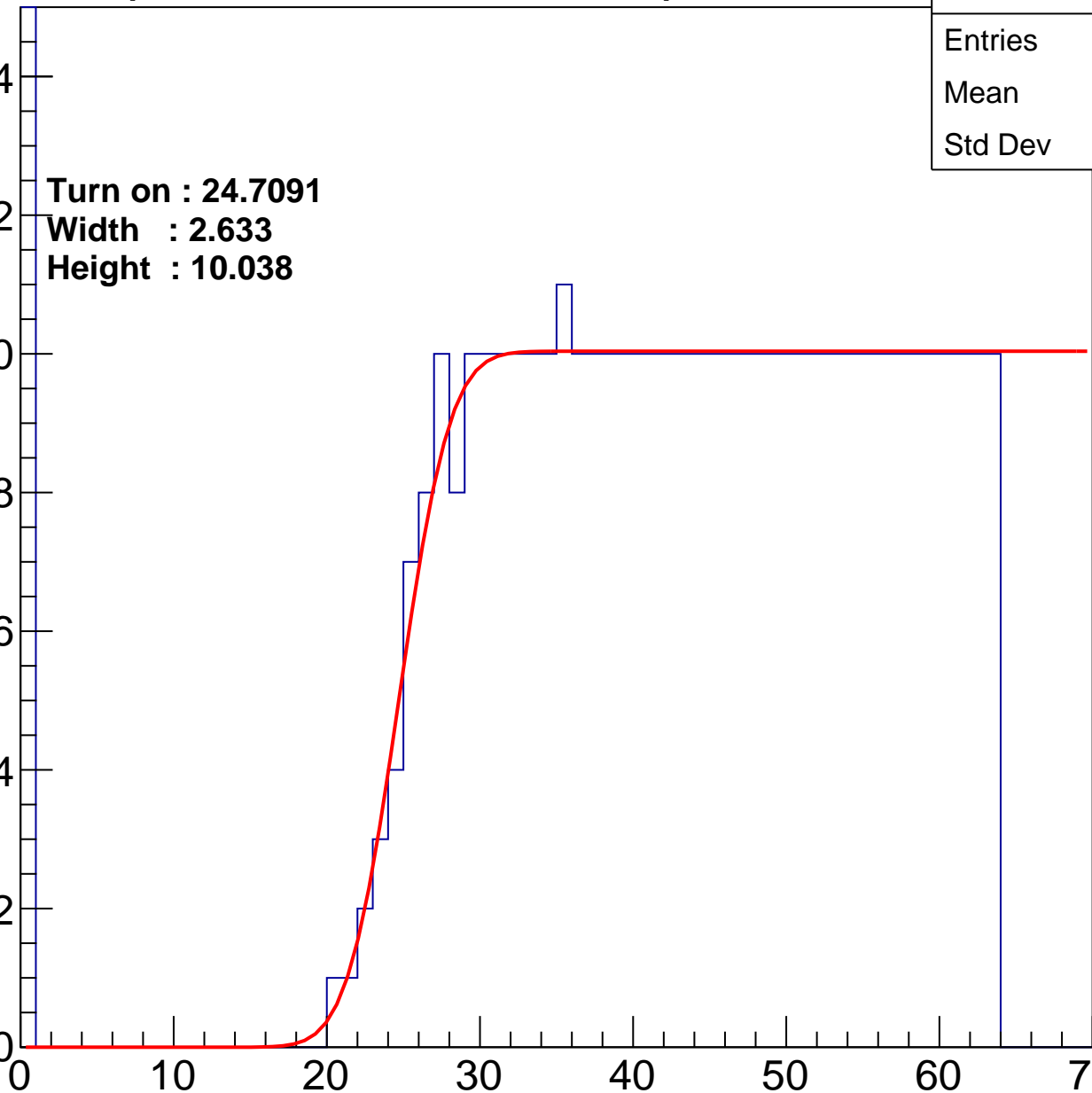
Width : 2.633

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch51

calib_packv5_041523_1651.root, FC#0, port C2

Entries	400
Mean	41.1
Std Dev	16.59

Turn on : 28.5258

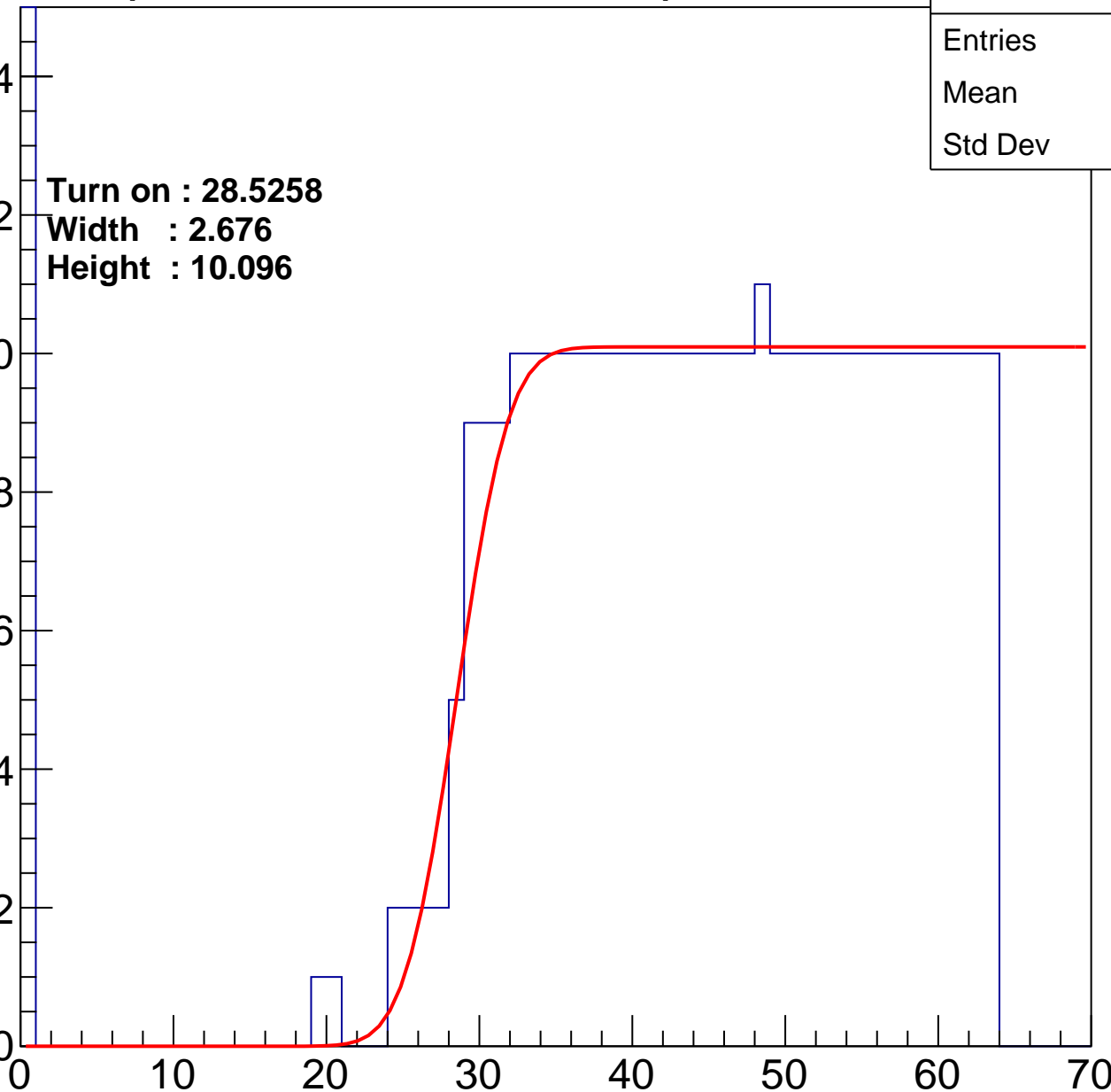
Width : 2.676

Height : 10.096

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch52

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	39.18
Std Dev	17.26

Turn on : 24.9569

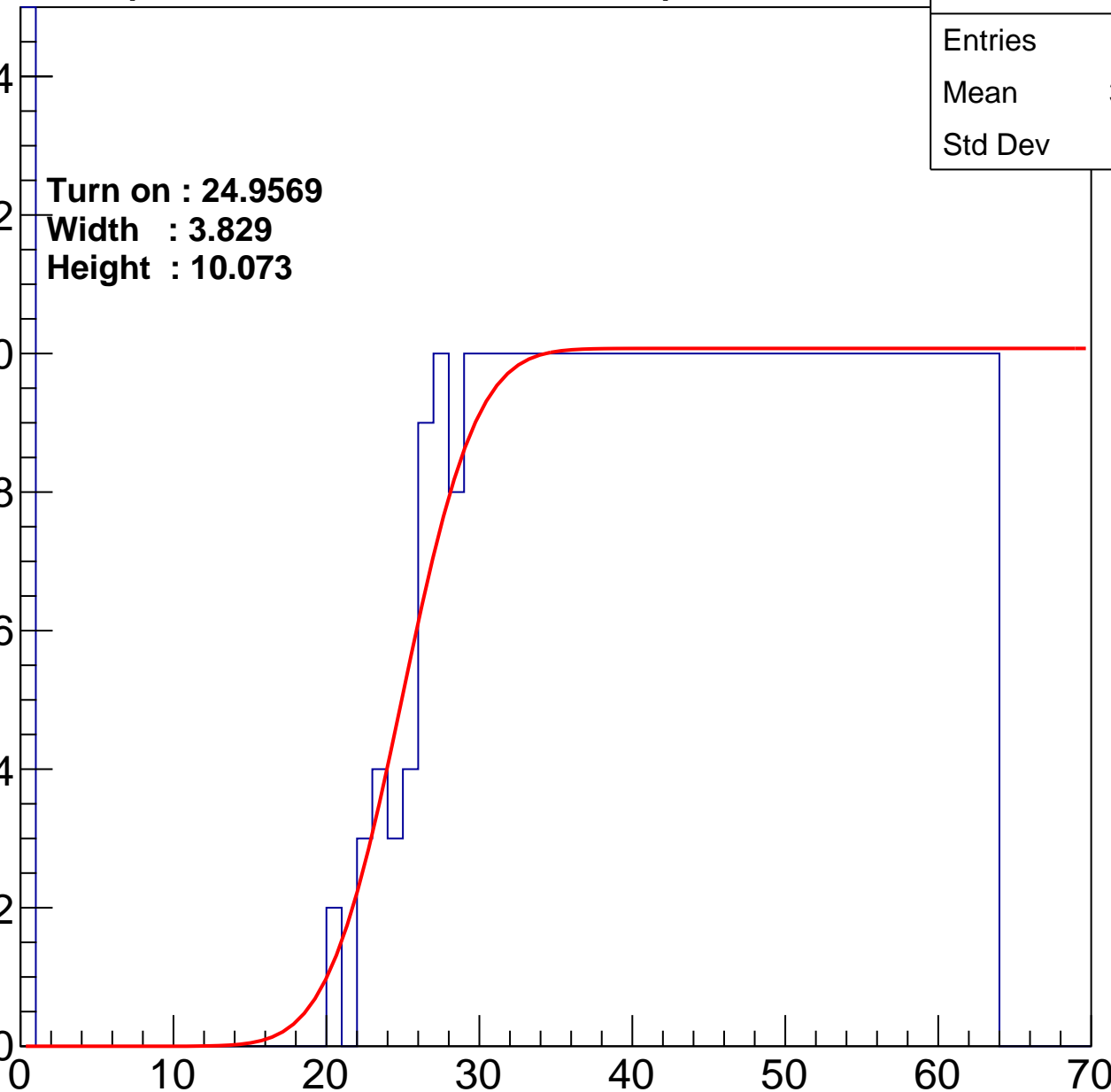
Width : 3.829

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch53

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	38.75
Std Dev	17.98

Turn on : 25.7464

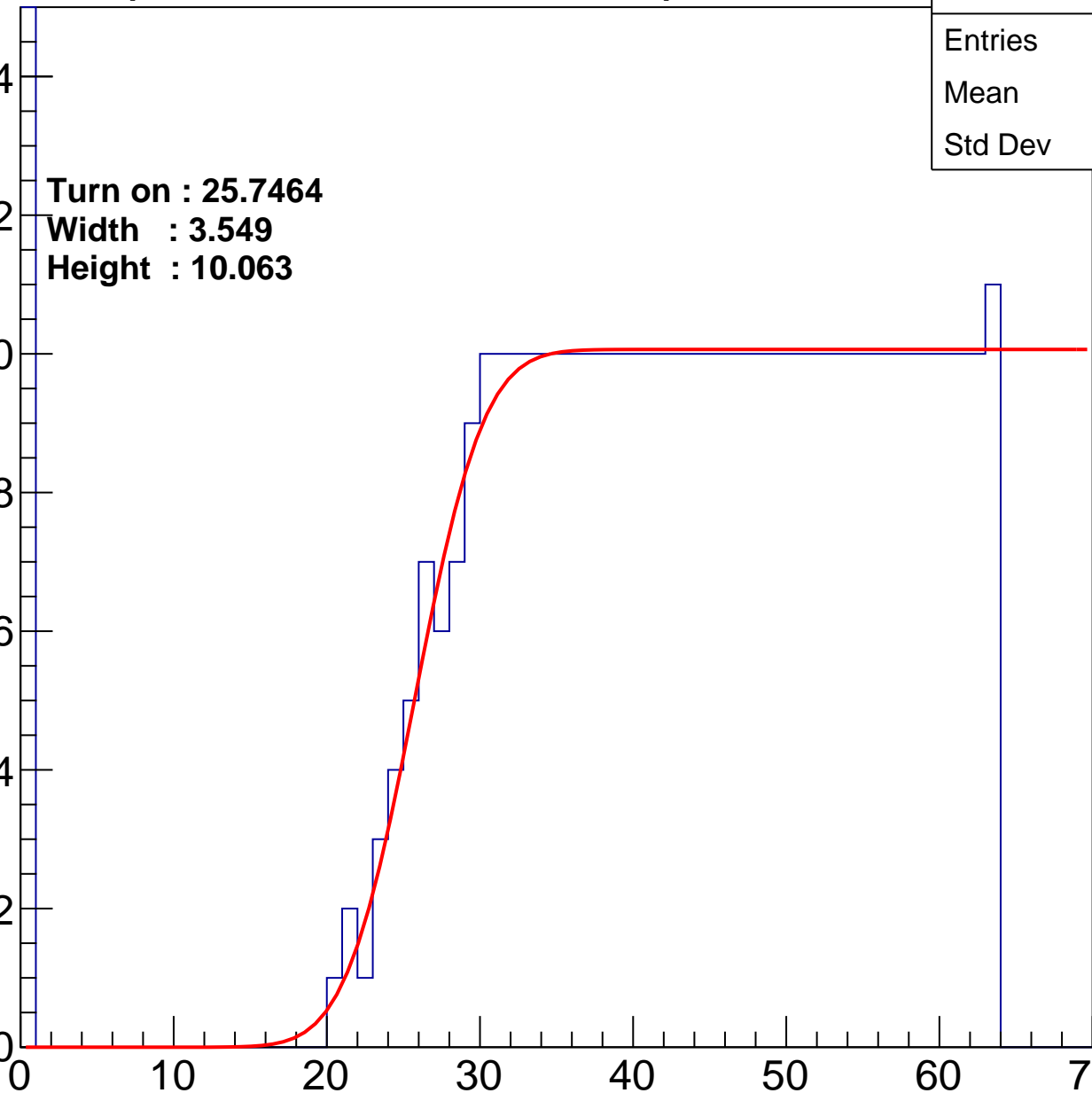
Width : 3.549

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch54

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.8
Std Dev	16.88

Turn on : 25.4764

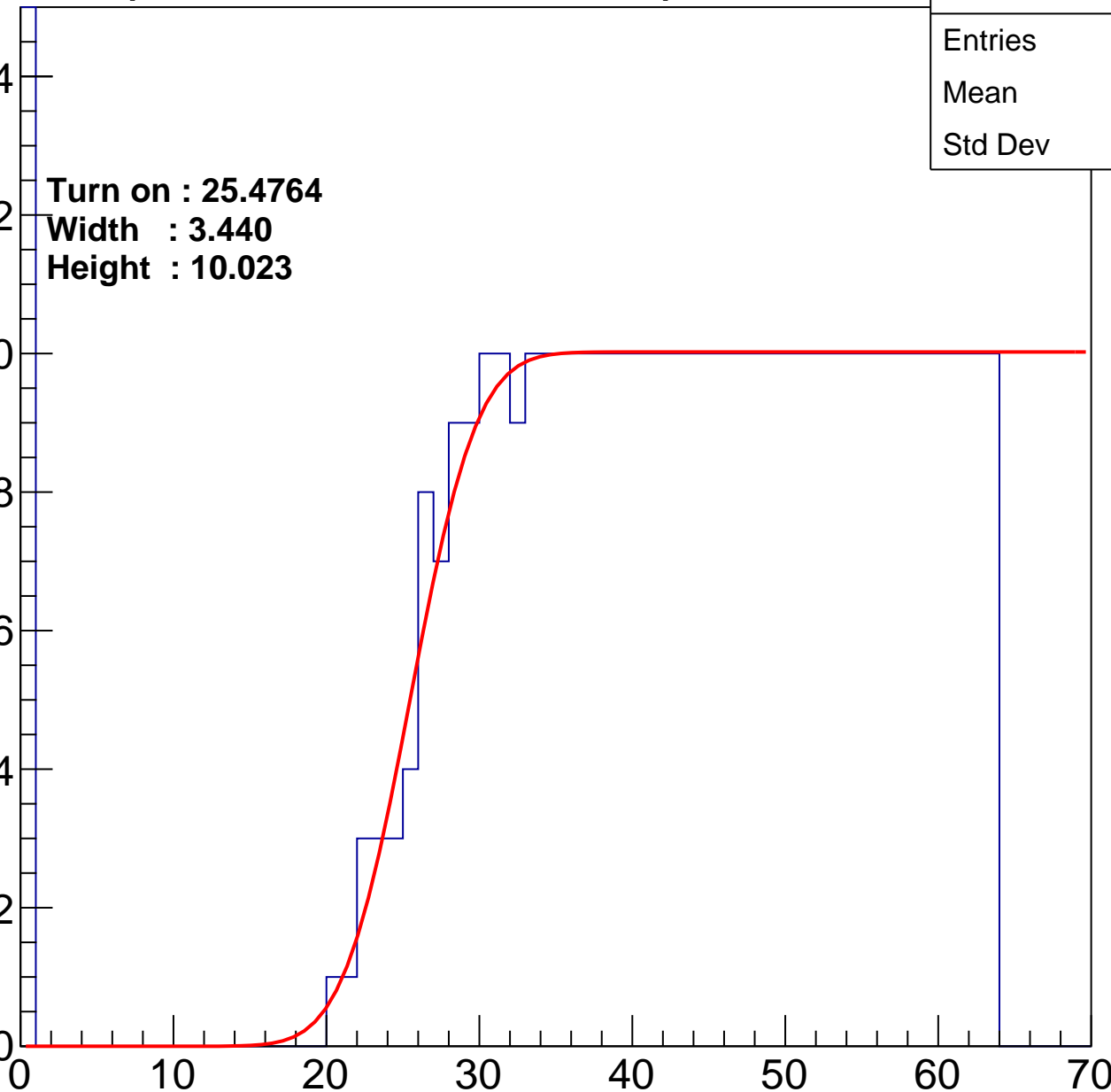
Width : 3.440

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch55

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	38.99
Std Dev	18.31

Turn on : 27.3637

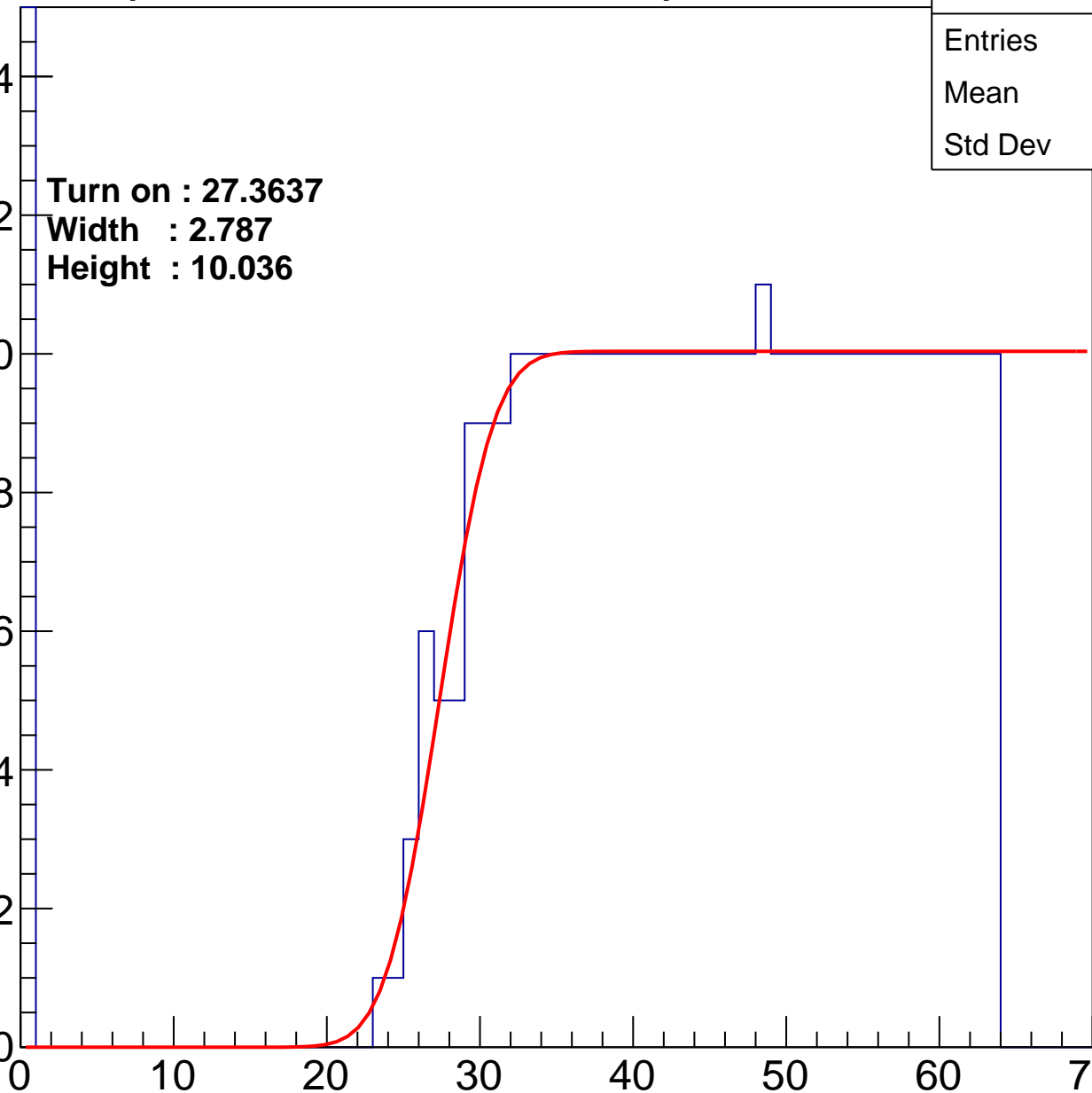
Width : 2.787

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch56

calib_packv5_041523_1651.root, FC#0, port C2

Entries	461
Mean	38.08
Std Dev	17.71

Turn on : 23.2671

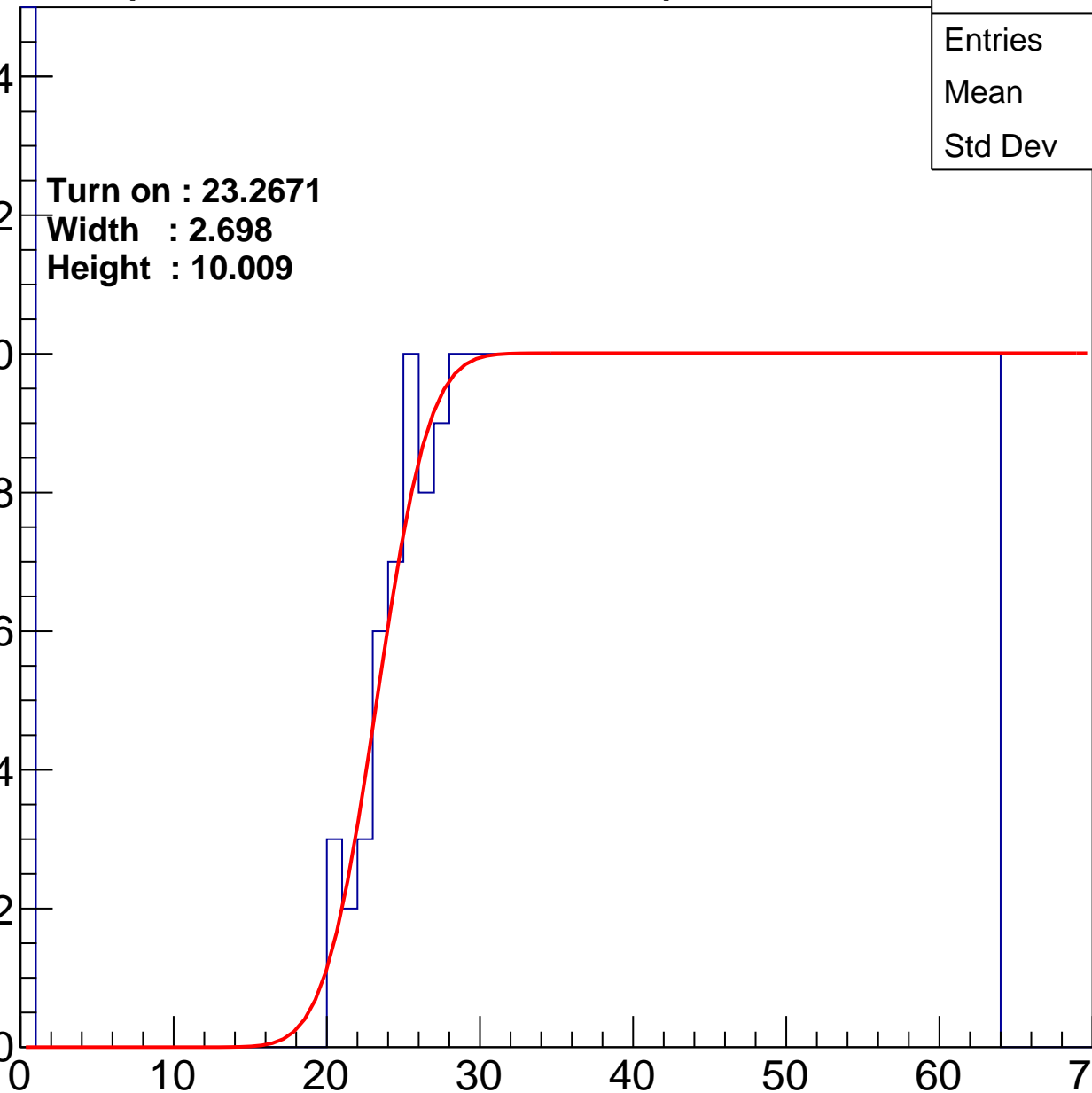
Width : 2.698

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch57

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.33
Std Dev	17.75

Turn on : 26.7281

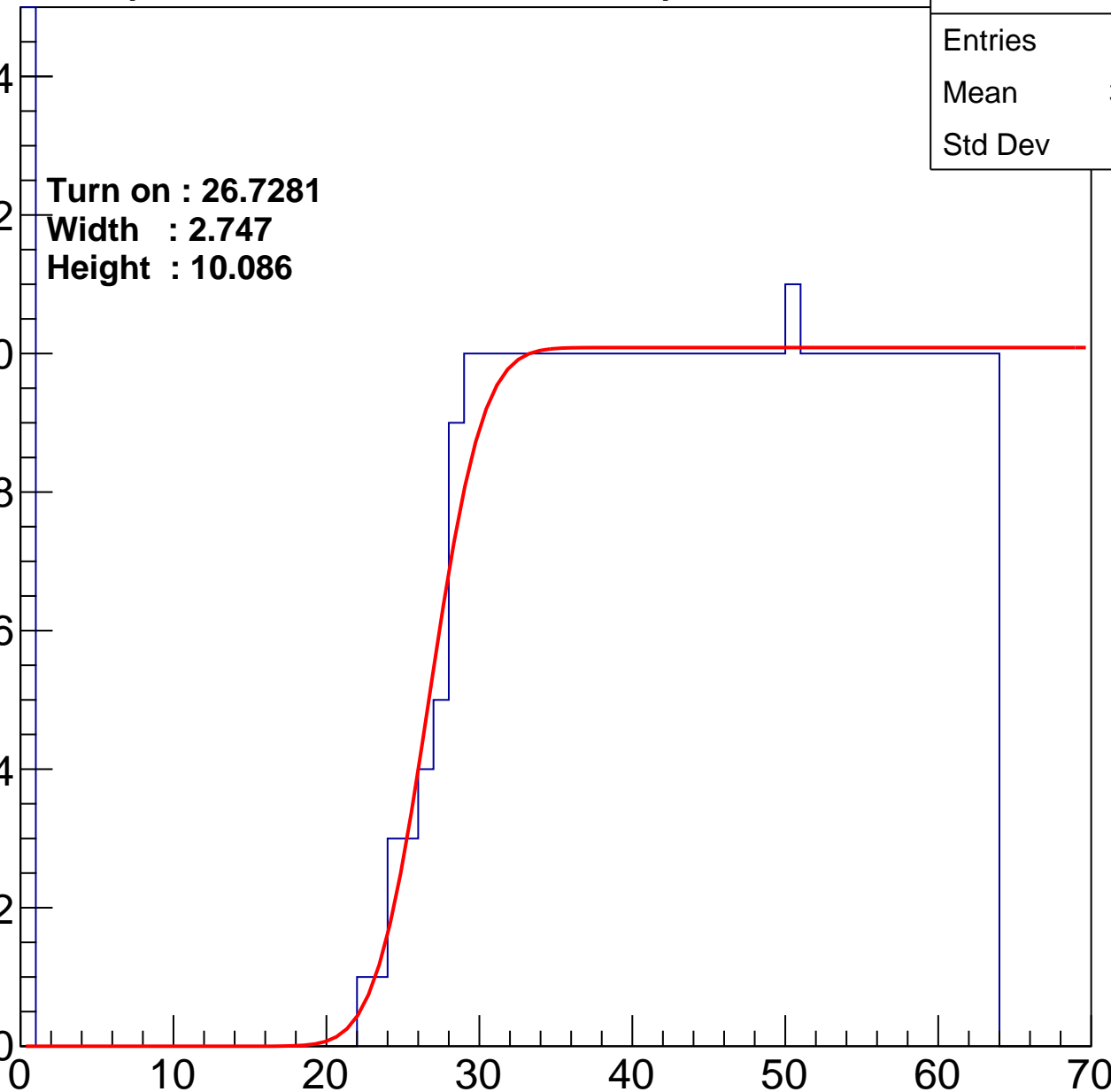
Width : 2.747

Height : 10.086

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch58

calib_packv5_041523_1651.root, FC#0, port C2

Entries	448
Mean	38.81
Std Dev	17.31

Turn on : 24.0135

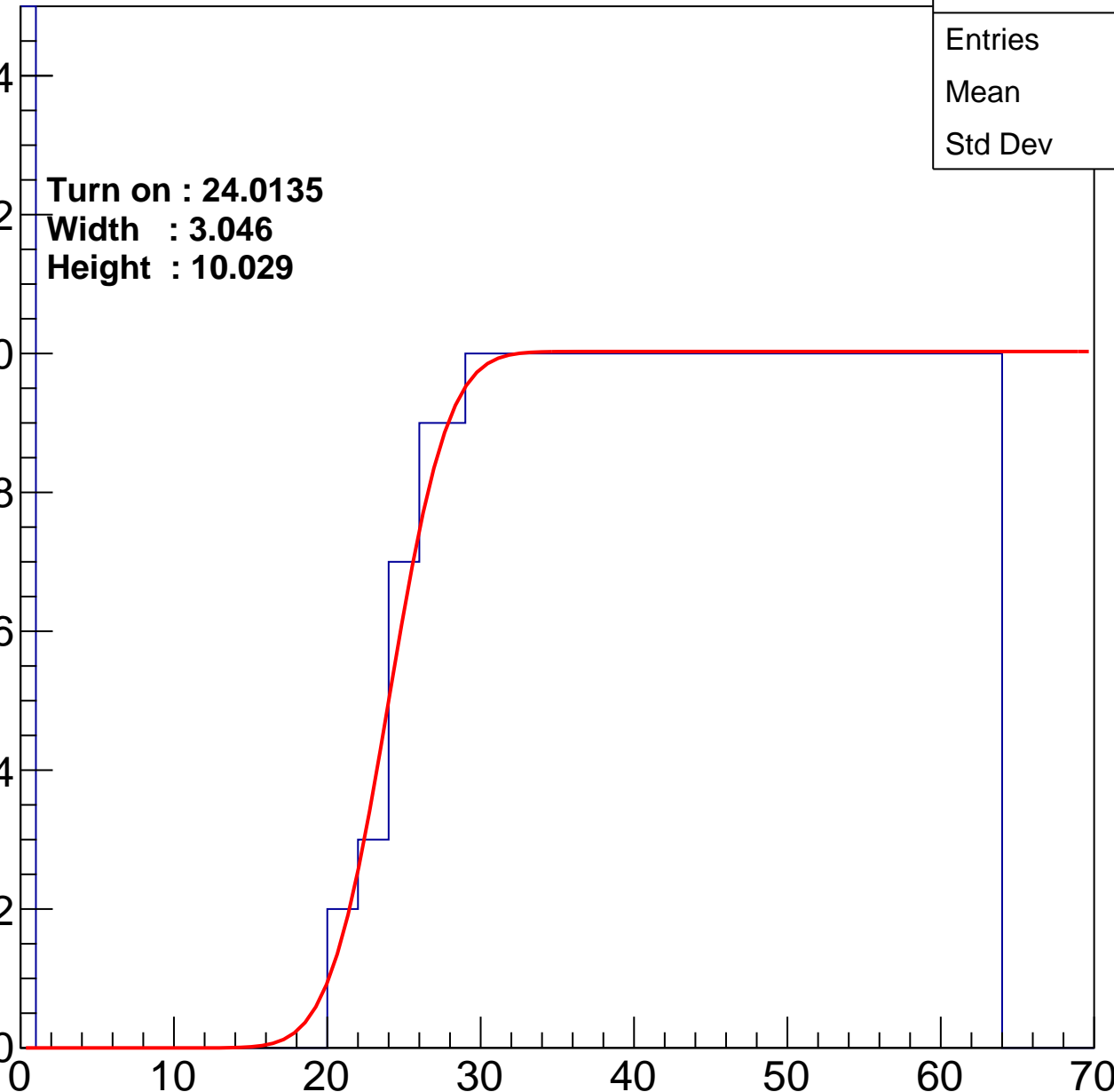
Width : 3.046

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch59

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.21
Std Dev	17.79

Turn on : 26.7619

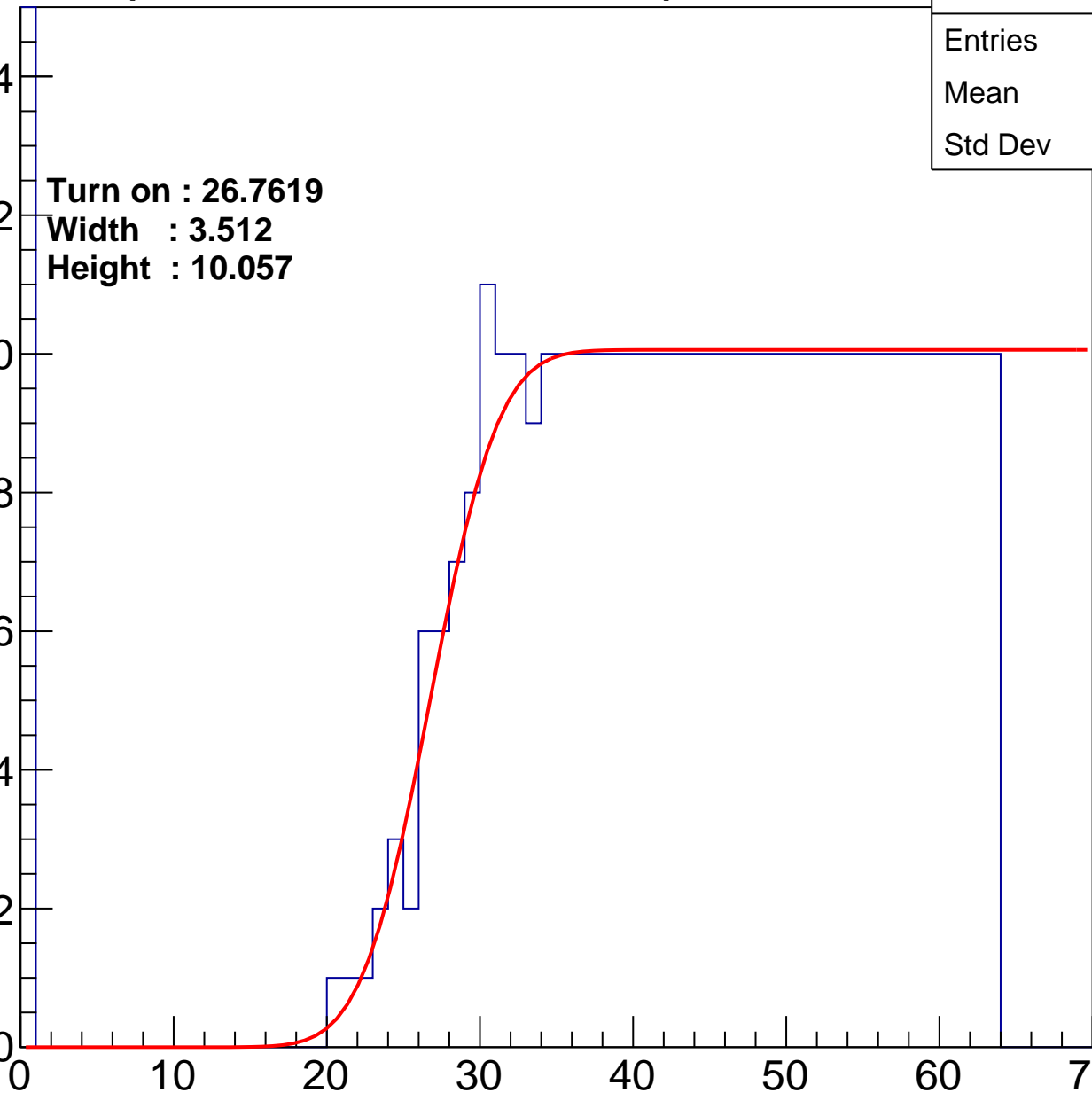
Width : 3.512

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch60

calib_packv5_041523_1651.root, FC#0, port C2

Entries	448
Mean	38.72
Std Dev	17.56

Turn on : 24.5804

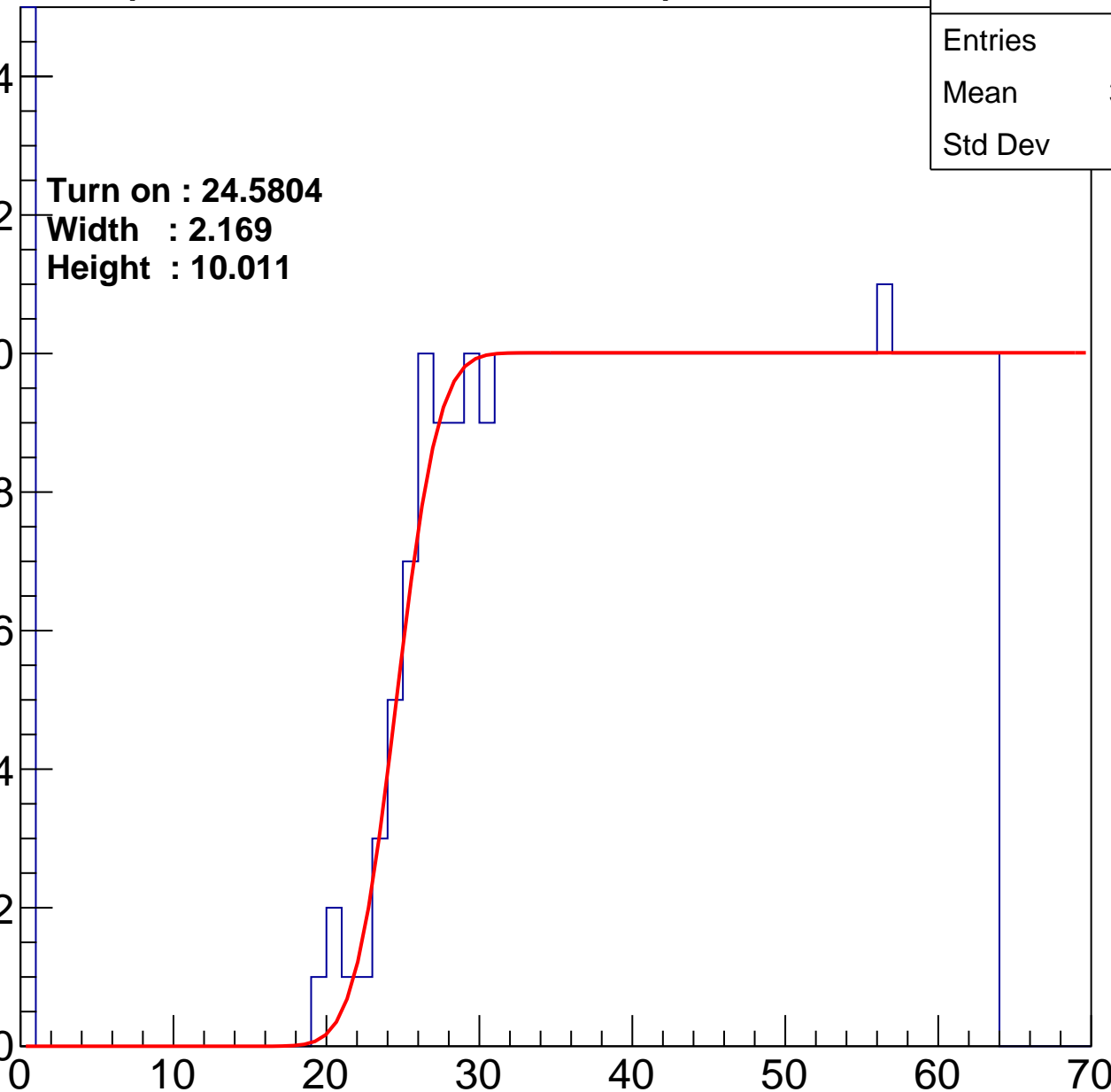
Width : 2.169

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch61

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	39.47
Std Dev	17.53

Turn on : 25.9684

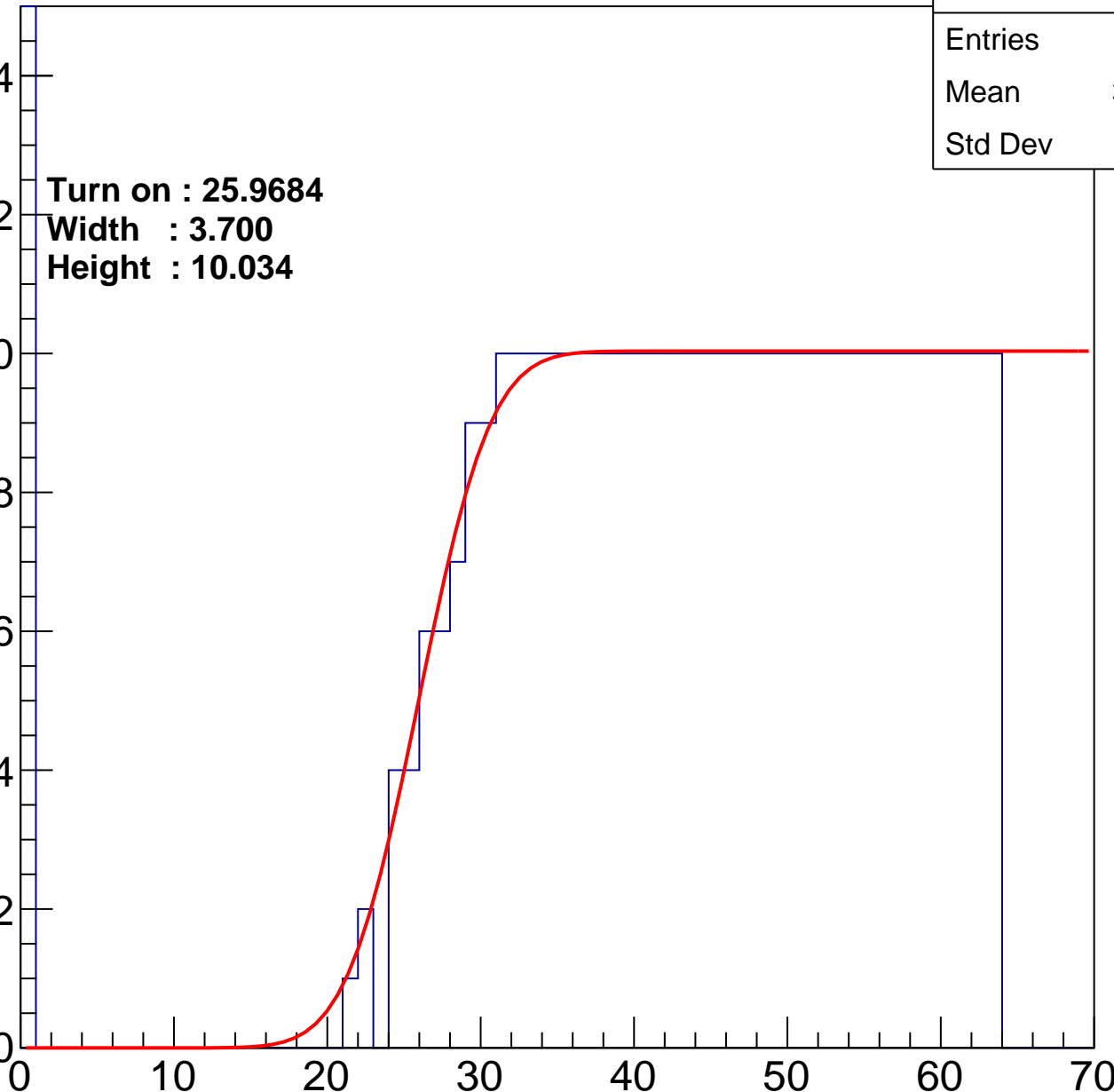
Width : 3.700

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch62

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.79
Std Dev	16.94

Turn on : 25.5801

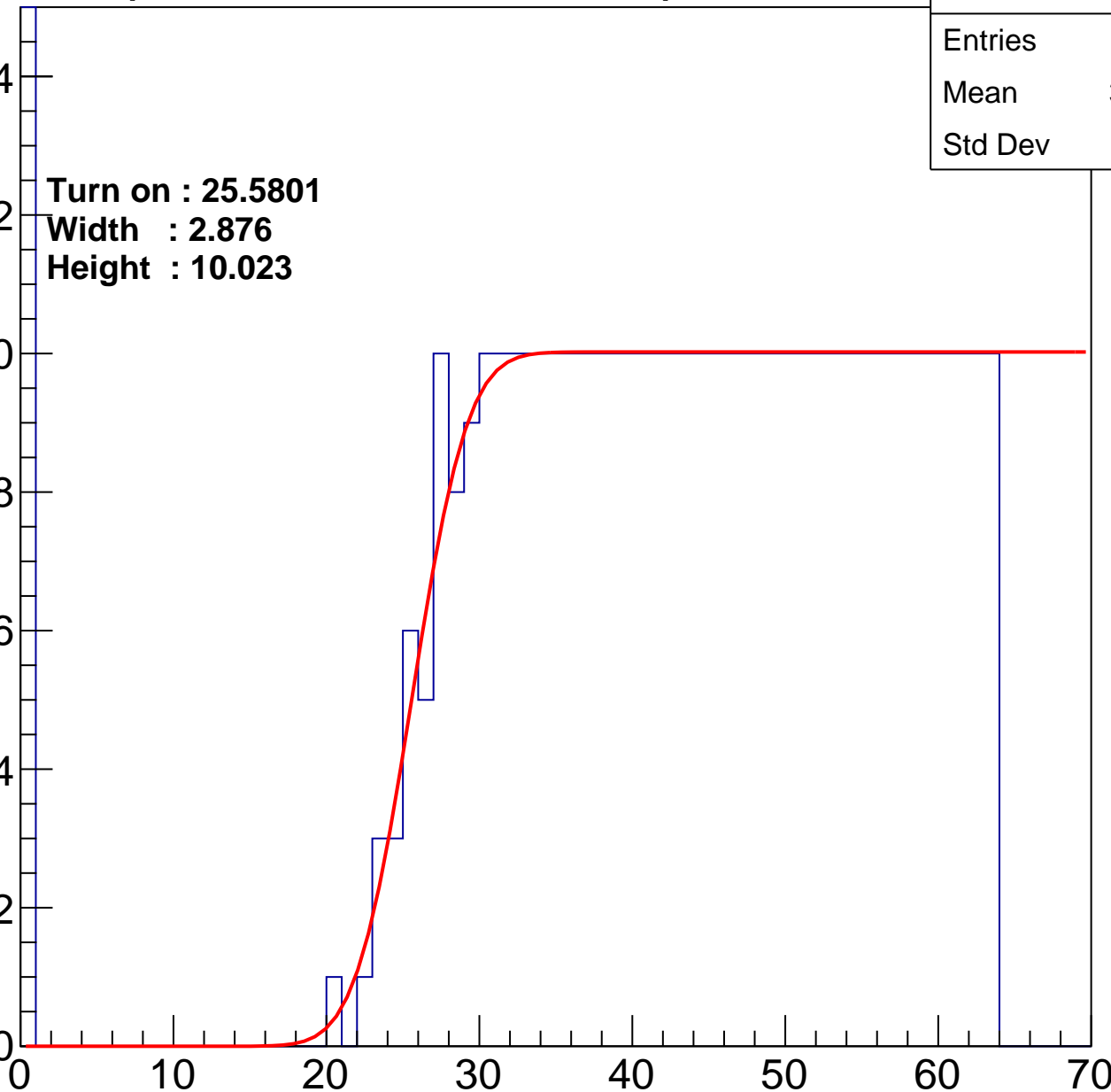
Width : 2.876

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch63

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	40.02
Std Dev	17.13

Turn on : 26.8043

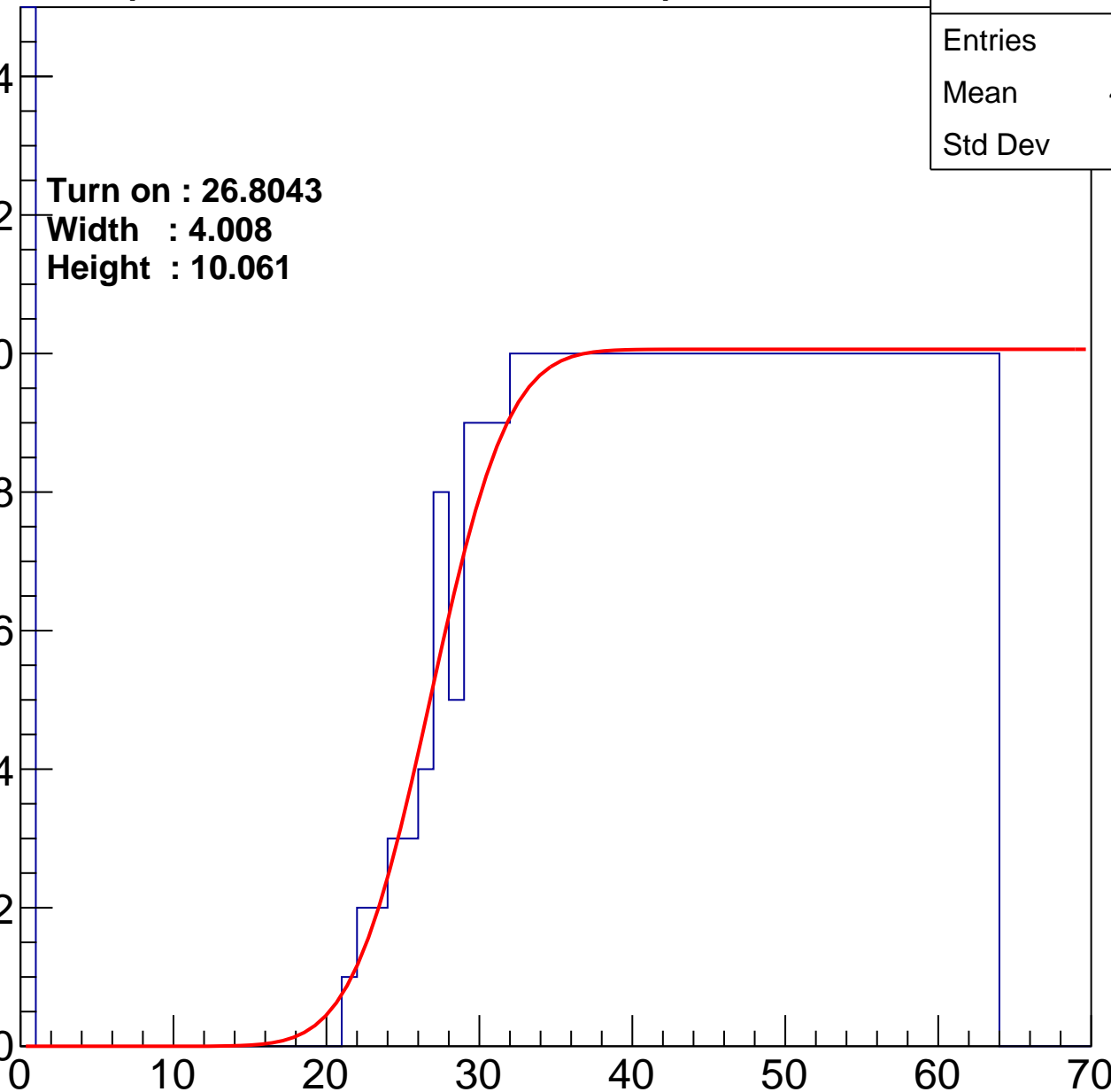
Width : 4.008

Height : 10.061

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch64

calib_packv5_041523_1651.root, FC#0, port C2

Entries	457
Mean	38.12
Std Dev	17.84

Turn on : 23.6583

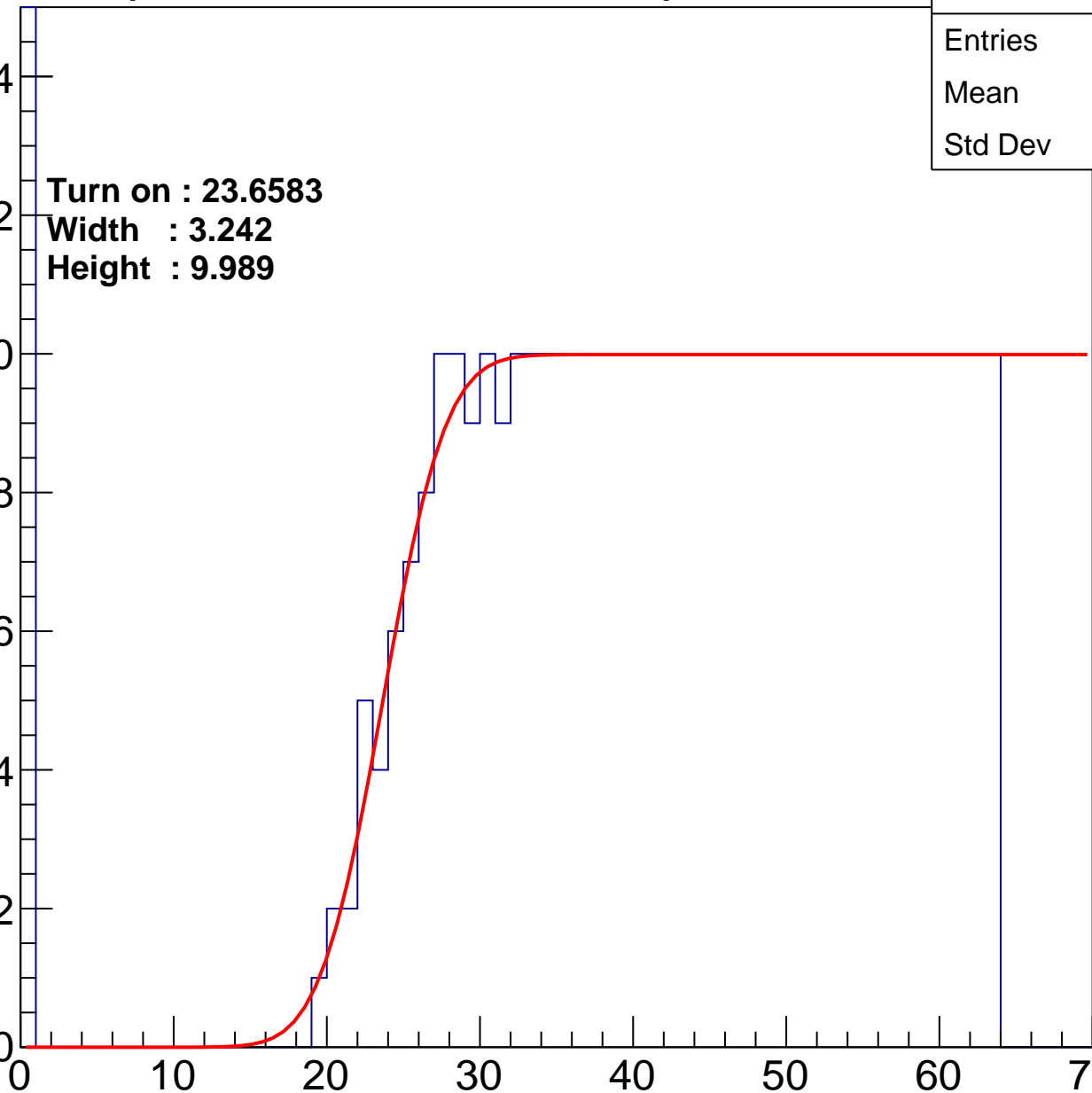
Width : 3.242

Height : 9.989

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch65

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	40.14
Std Dev	16.9

Turn on : 26.1815

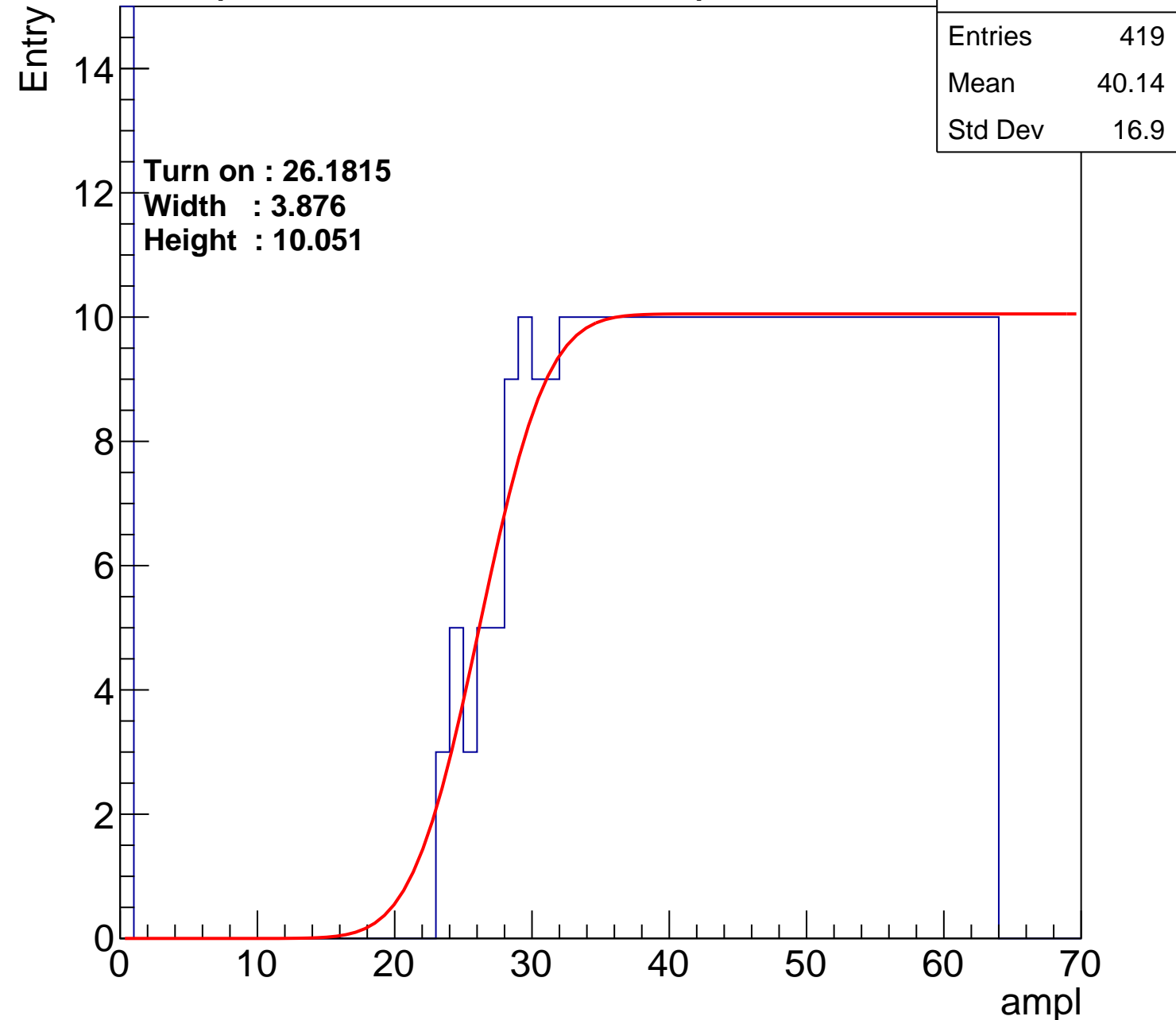
Width : 3.876

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch66

calib_packv5_041523_1651.root, FC#0, port C2

Entries	444
Mean	39.14
Std Dev	17.1

Turn on : 24.2128

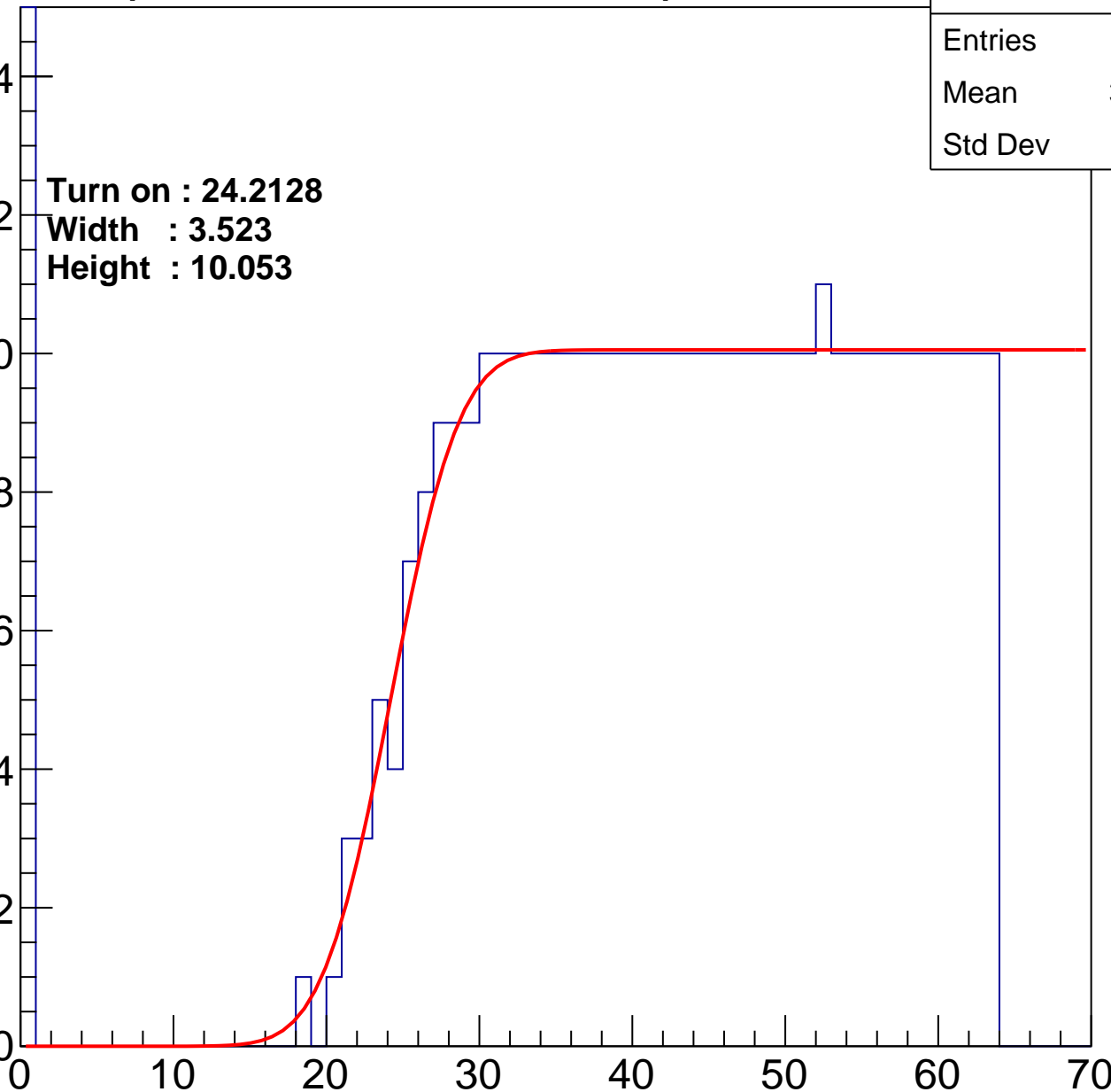
Width : 3.523

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch67

calib_packv5_041523_1651.root, FC#0, port C2

Entries	412
Mean	40.5
Std Dev	16.74

Turn on : 26.7952

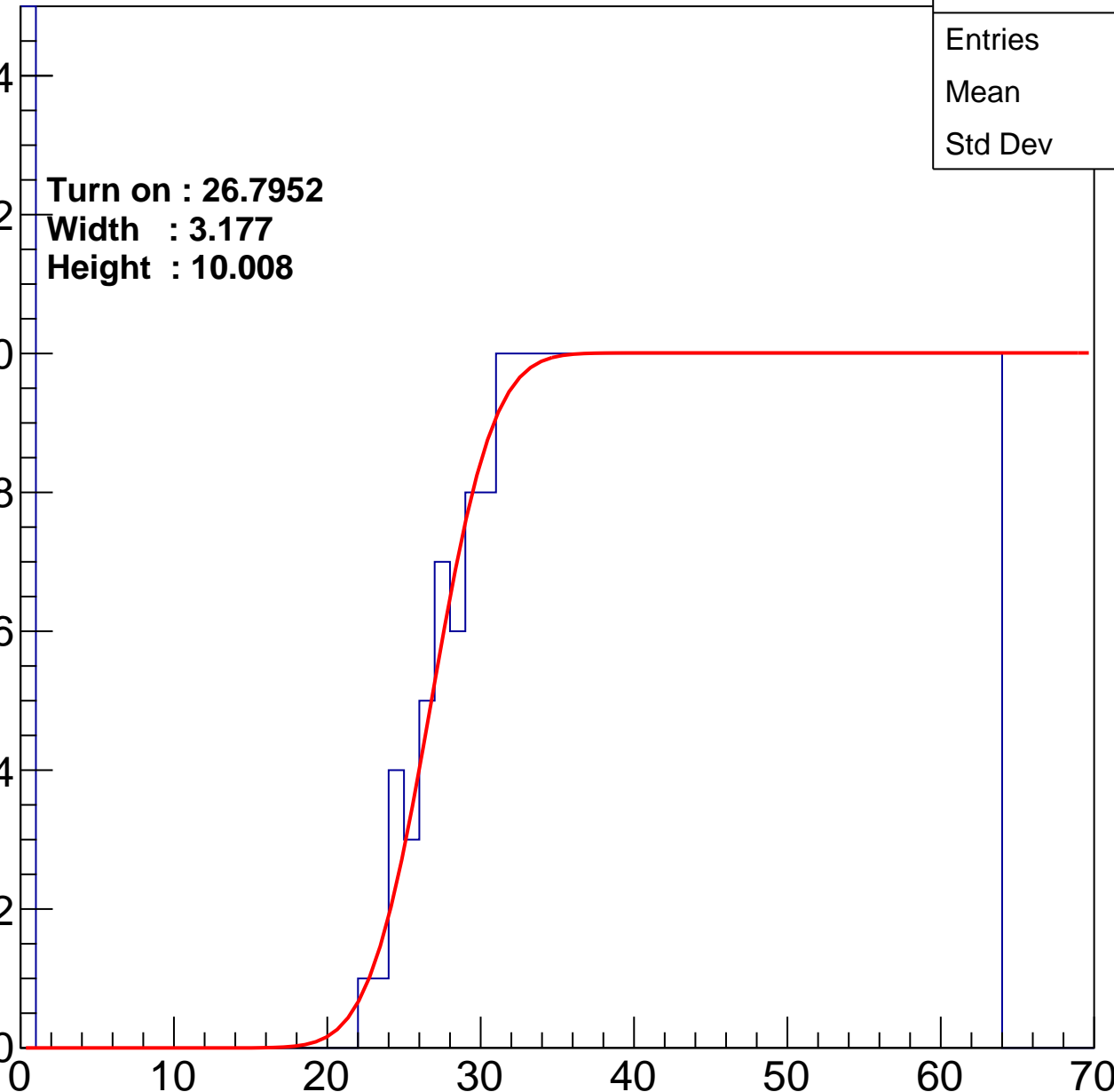
Width : 3.177

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch68

calib_packv5_041523_1651.root, FC#0, port C2

Entries	421
Mean	40.05
Std Dev	17.01

Turn on : 26.2395

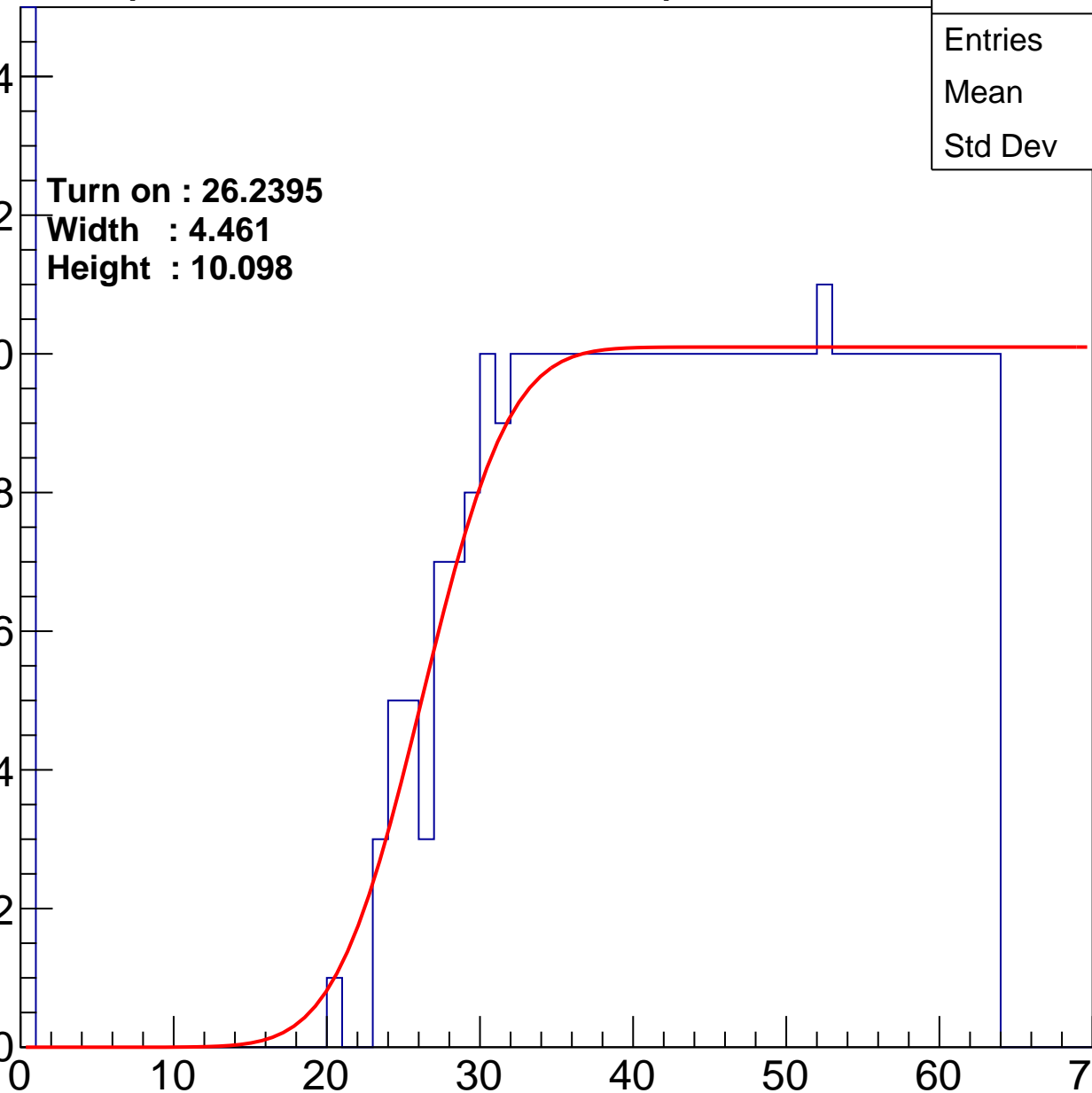
Width : 4.461

Height : 10.098

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch69

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	40.2
Std Dev	17.21

Turn on : 26.9847

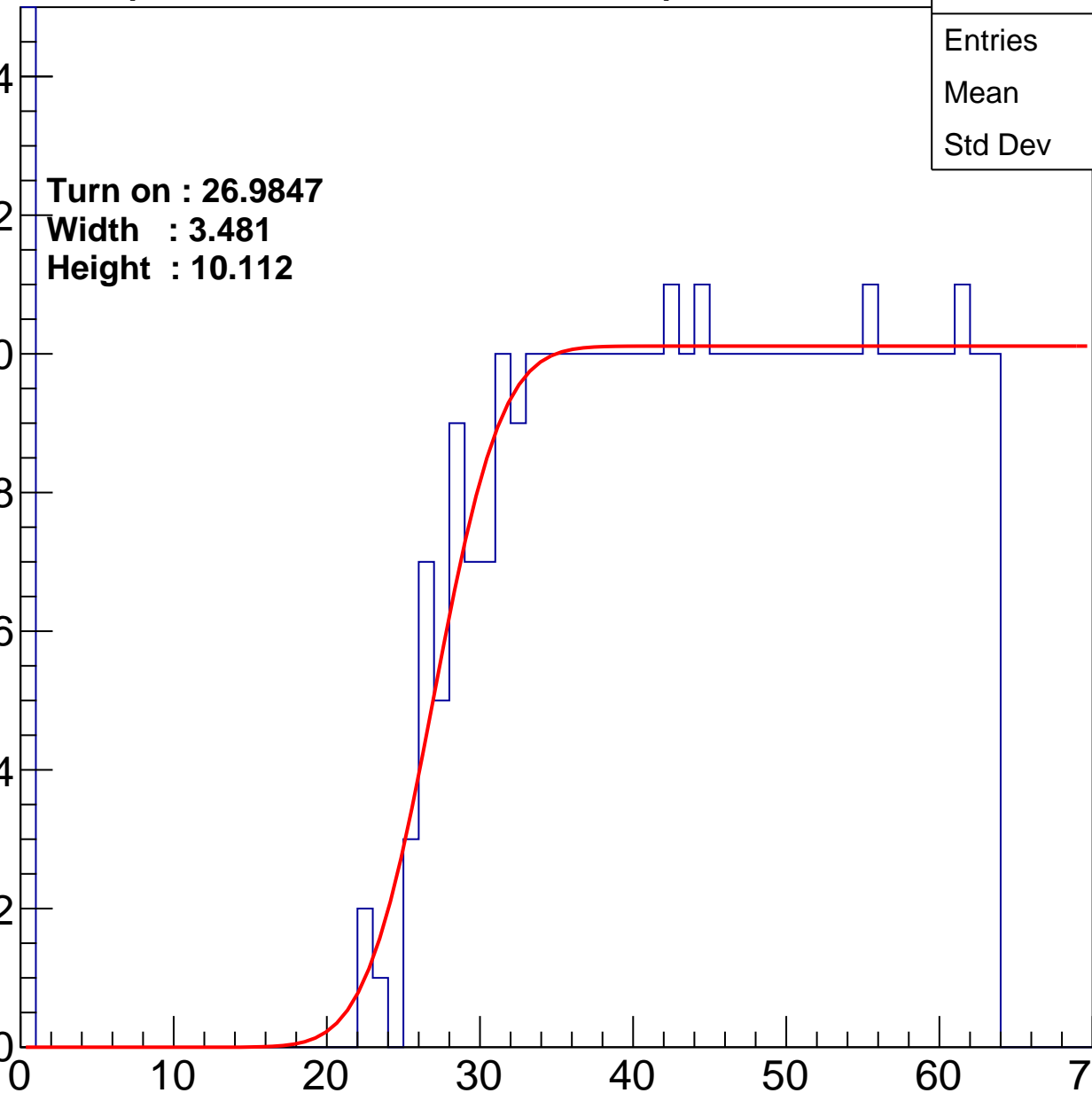
Width : 3.481

Height : 10.112

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch70

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	38.9
Std Dev	17.72

Turn on : 25.3783

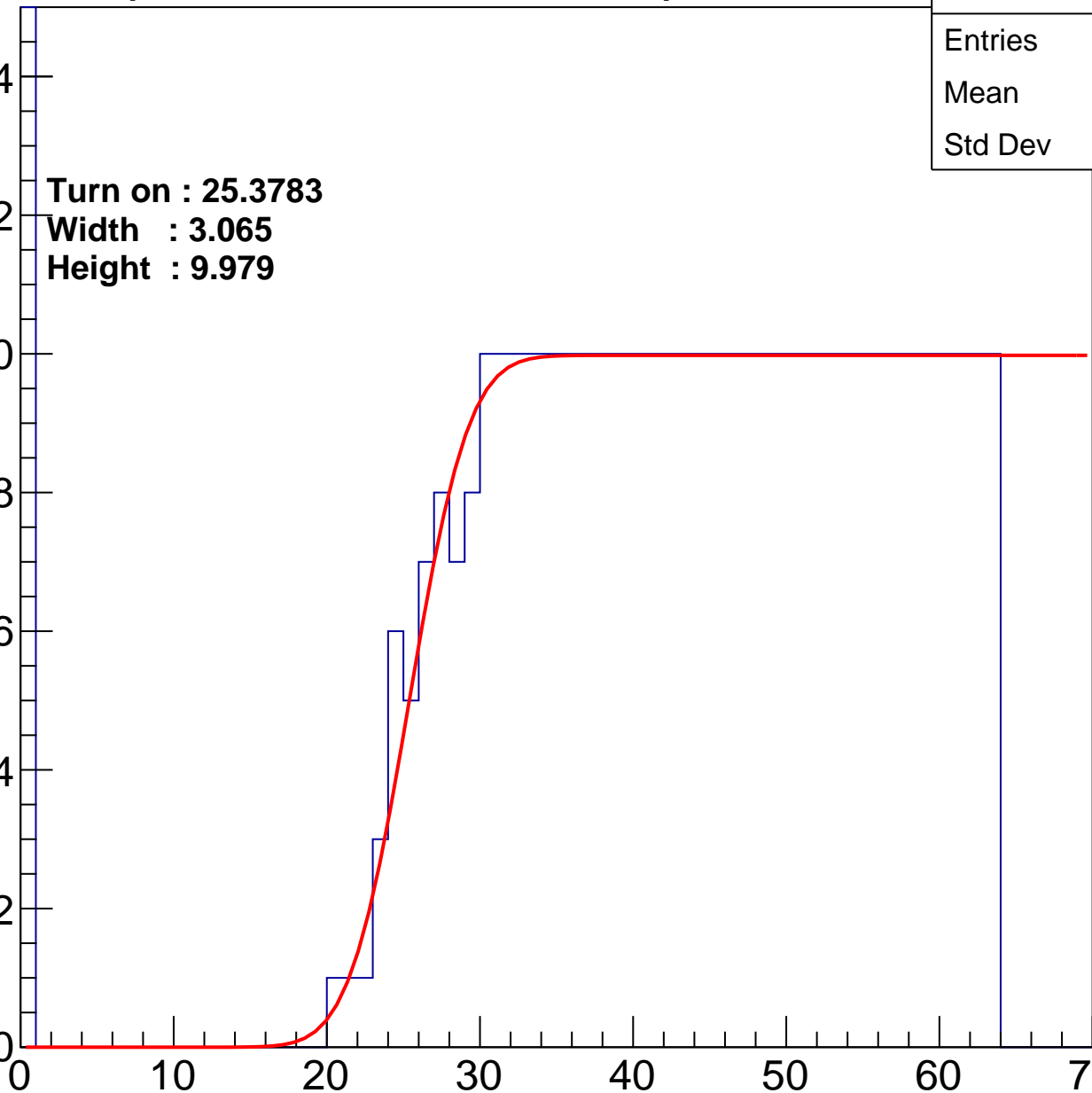
Width : 3.065

Height : 9.979

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch71

calib_packv5_041523_1651.root, FC#0, port C2

Entries	425
Mean	39.54
Std Dev	17.51

Turn on : 26.2785

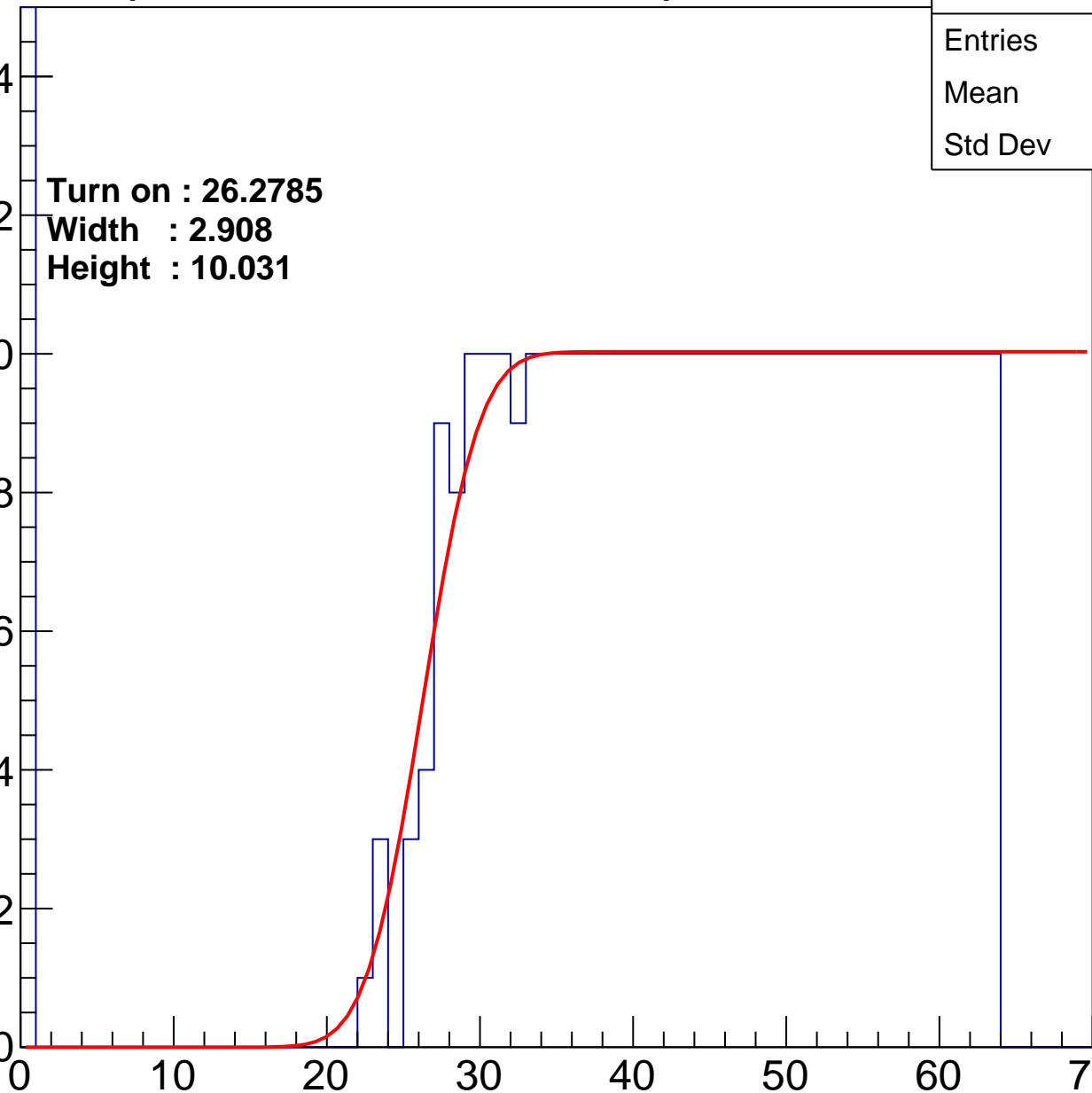
Width : 2.908

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch72

calib_packv5_041523_1651.root, FC#0, port C2

Entries	436
Mean	38.27
Std Dev	18.71

Turn on : 26.5946

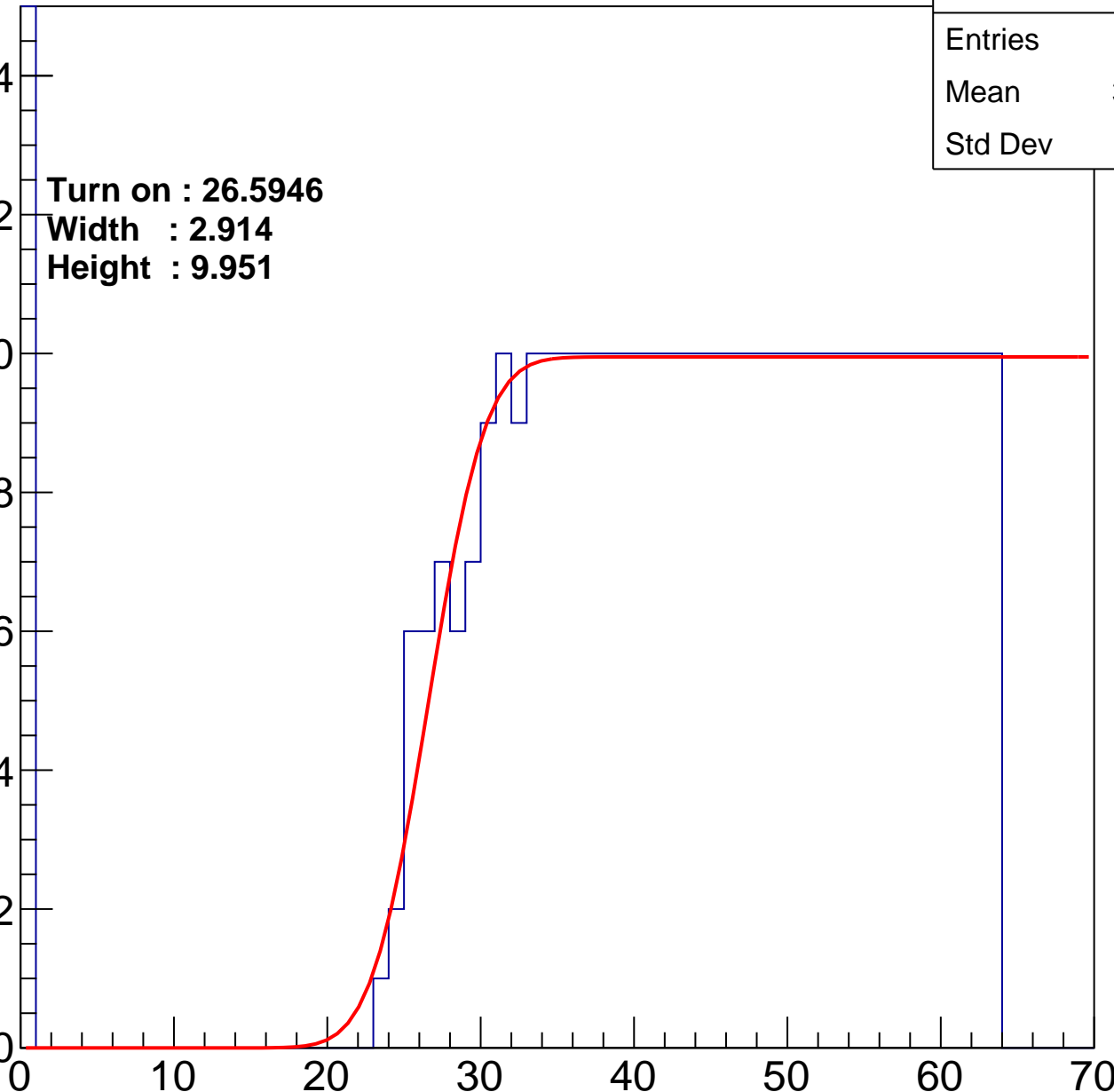
Width : 2.914

Height : 9.951

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch73

calib_packv5_041523_1651.root, FC#0, port C2

Entries	409
Mean	41.09
Std Dev	16.09

Turn on : 26.8662

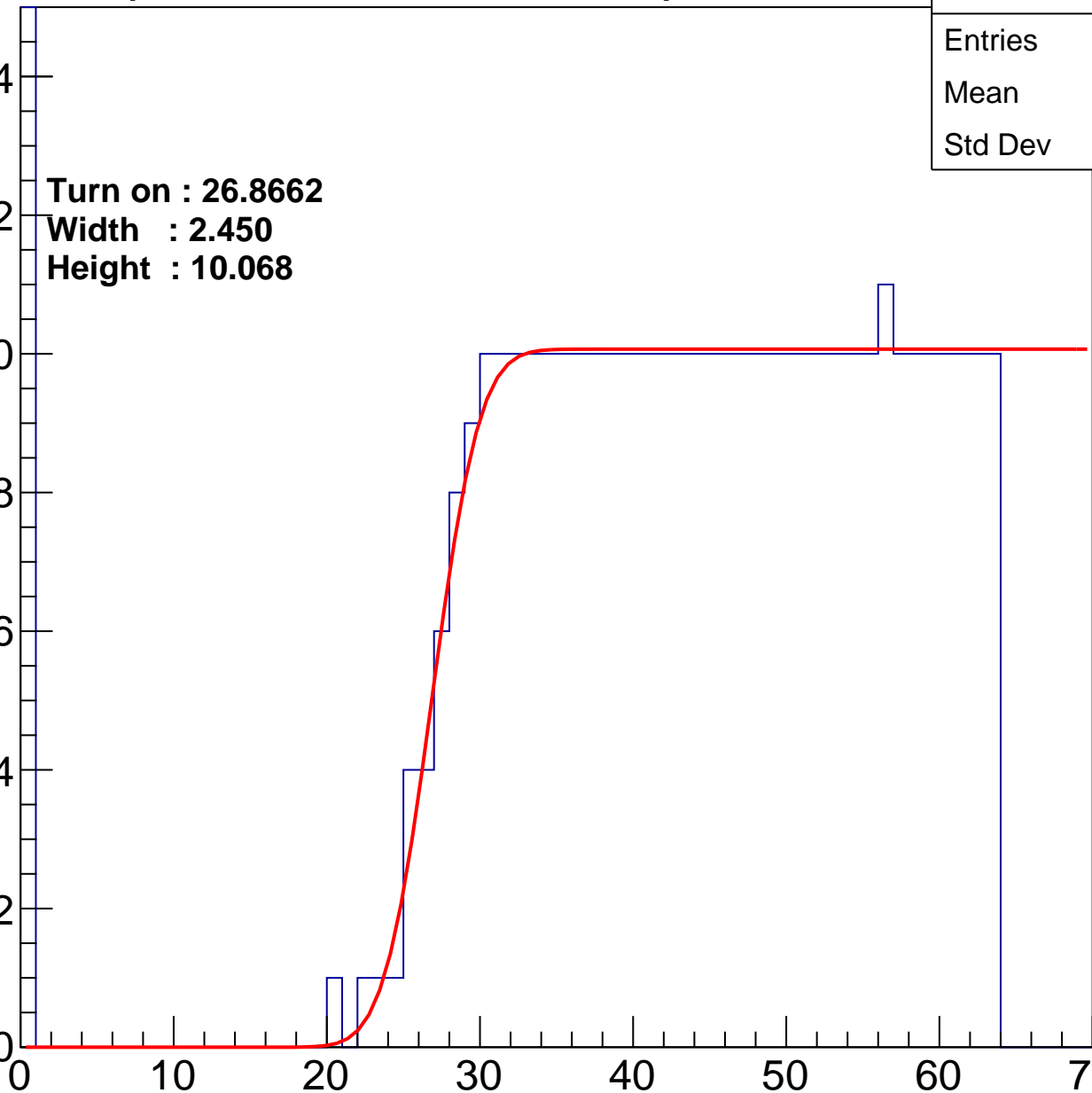
Width : 2.450

Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch74

calib_packv5_041523_1651.root, FC#0, port C2

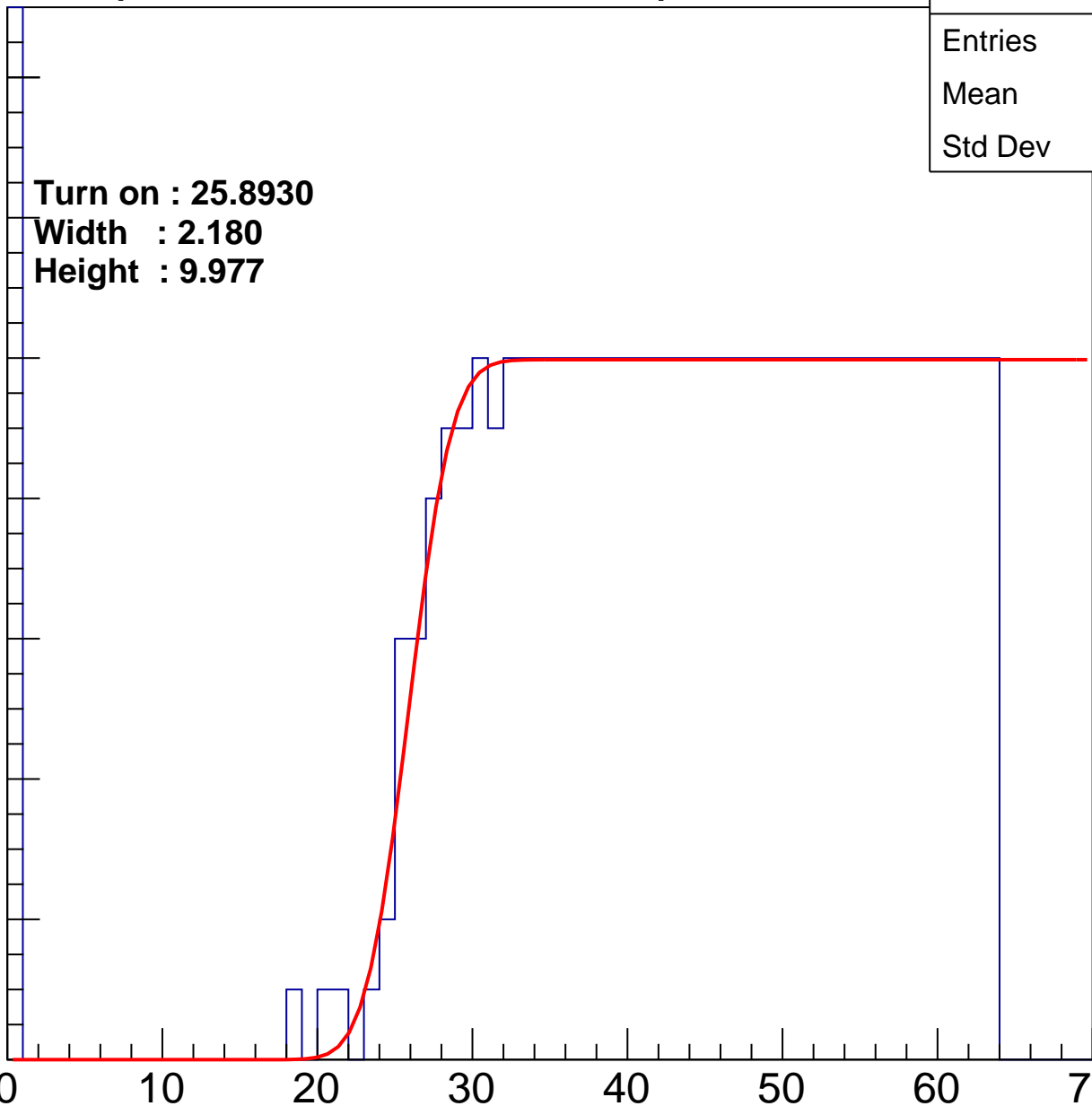
Entry

14
12
10
8
6
4
2
0

Turn on : 25.8930
Width : 2.180
Height : 9.977

Entries	437
Mean	38.77
Std Dev	17.97

ampl



B1L103S, U21-ch75

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	39.33
Std Dev	17.48

Turn on : 26.3977

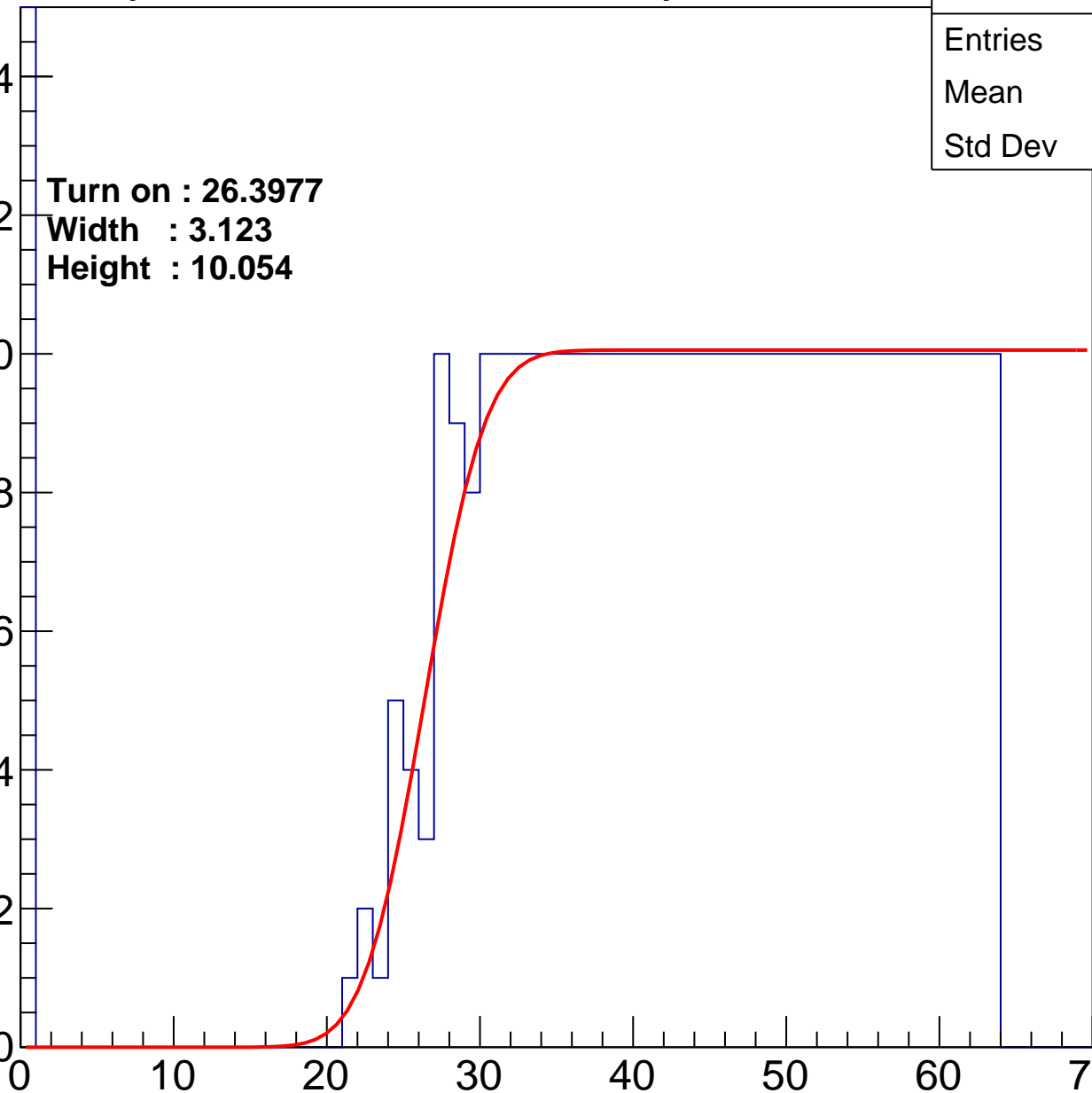
Width : 3.123

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch76

calib_packv5_041523_1651.root, FC#0, port C2

Entries	449
Mean	38.77
Std Dev	17.31

Turn on : 23.8687

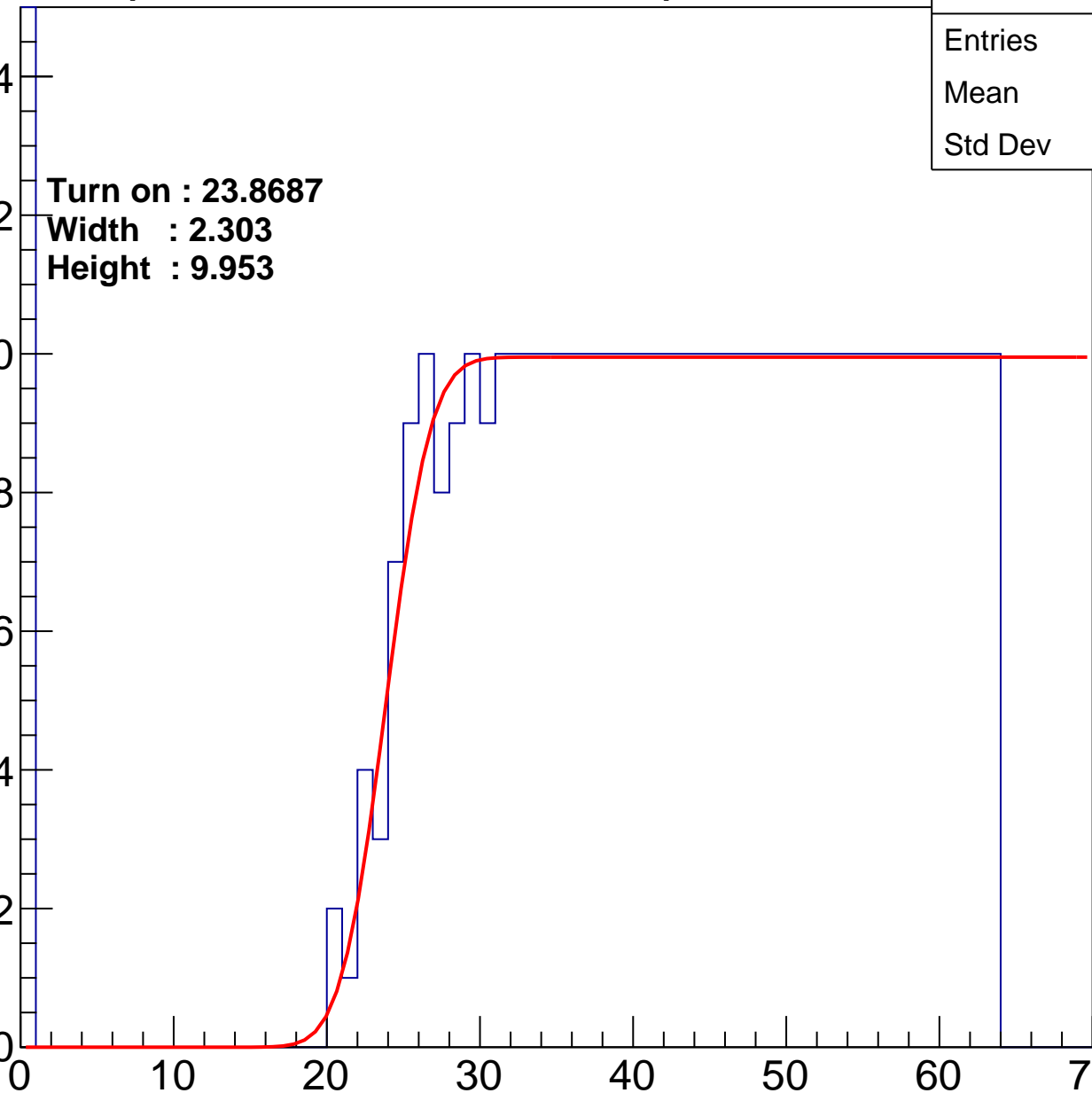
Width : 2.303

Height : 9.953

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch77

calib_packv5_041523_1651.root, FC#0, port C2

Entries	444
Mean	37.85
Std Dev	19.01

Turn on : 26.8403

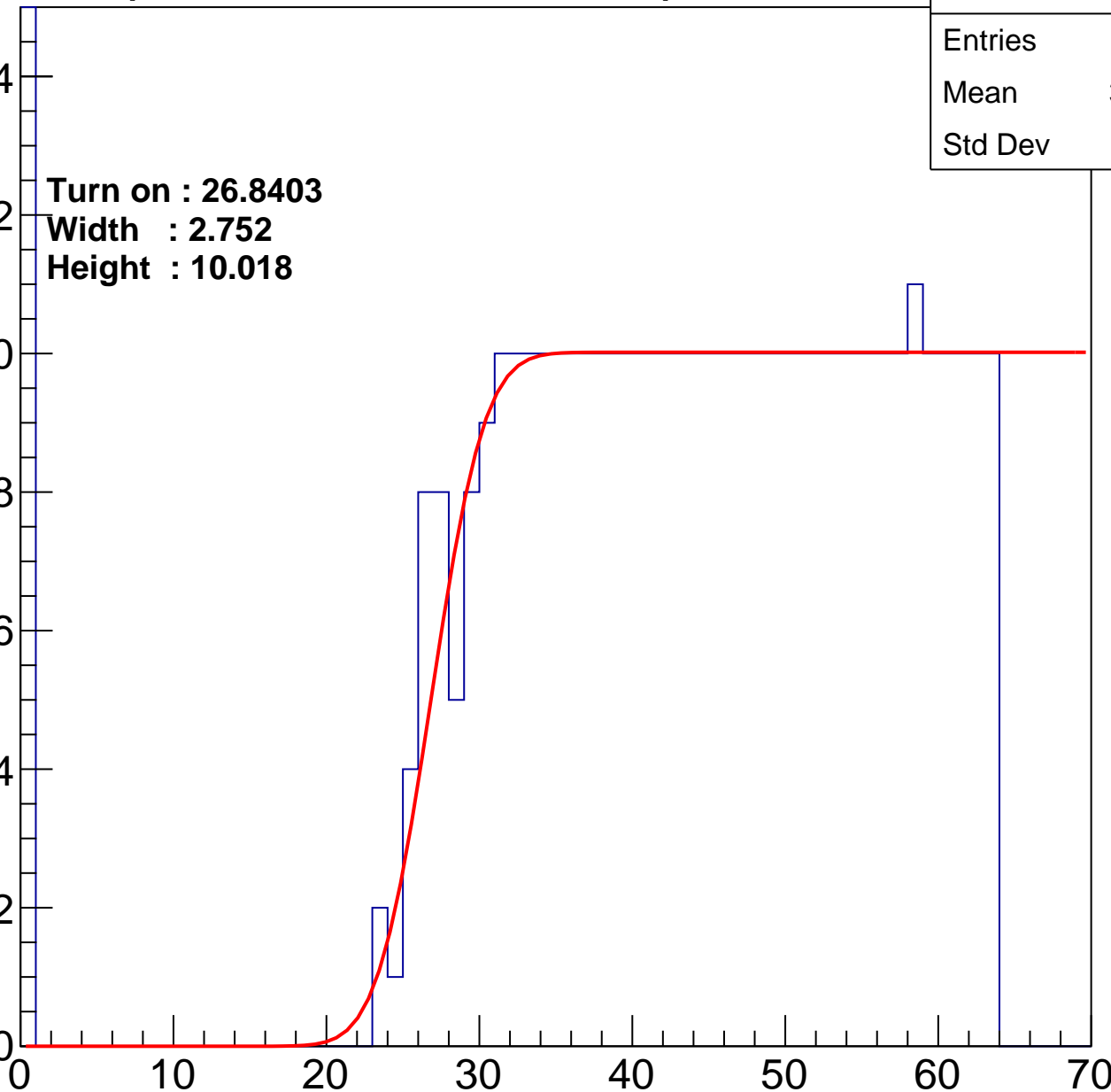
Width : 2.752

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch78

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	38.87
Std Dev	17.5

Turn on : 24.9184

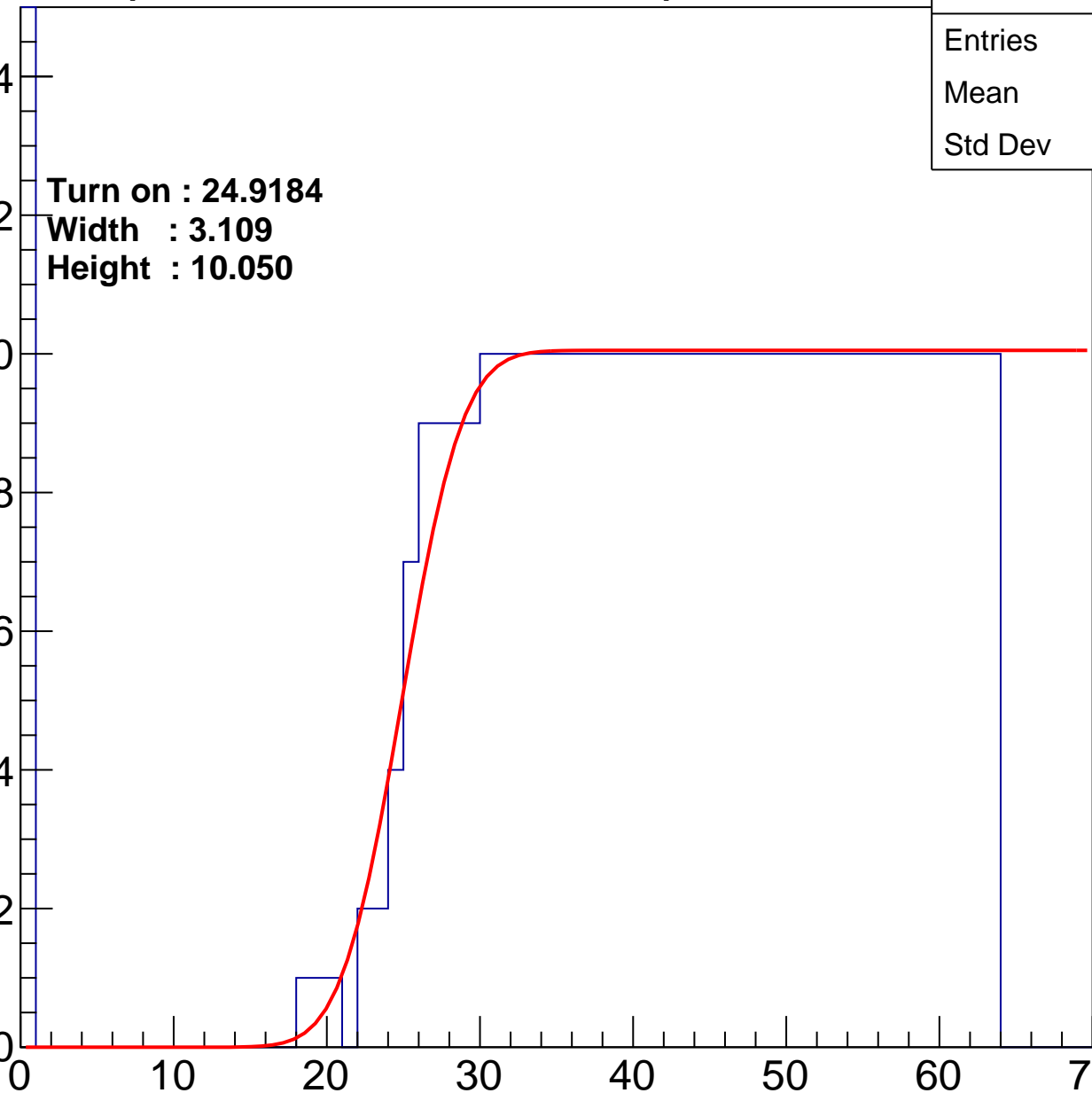
Width : 3.109

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch79

calib_packv5_041523_1651.root, FC#0, port C2

Entries	412
Mean	40.13
Std Dev	17.46

Turn on : 27.6582

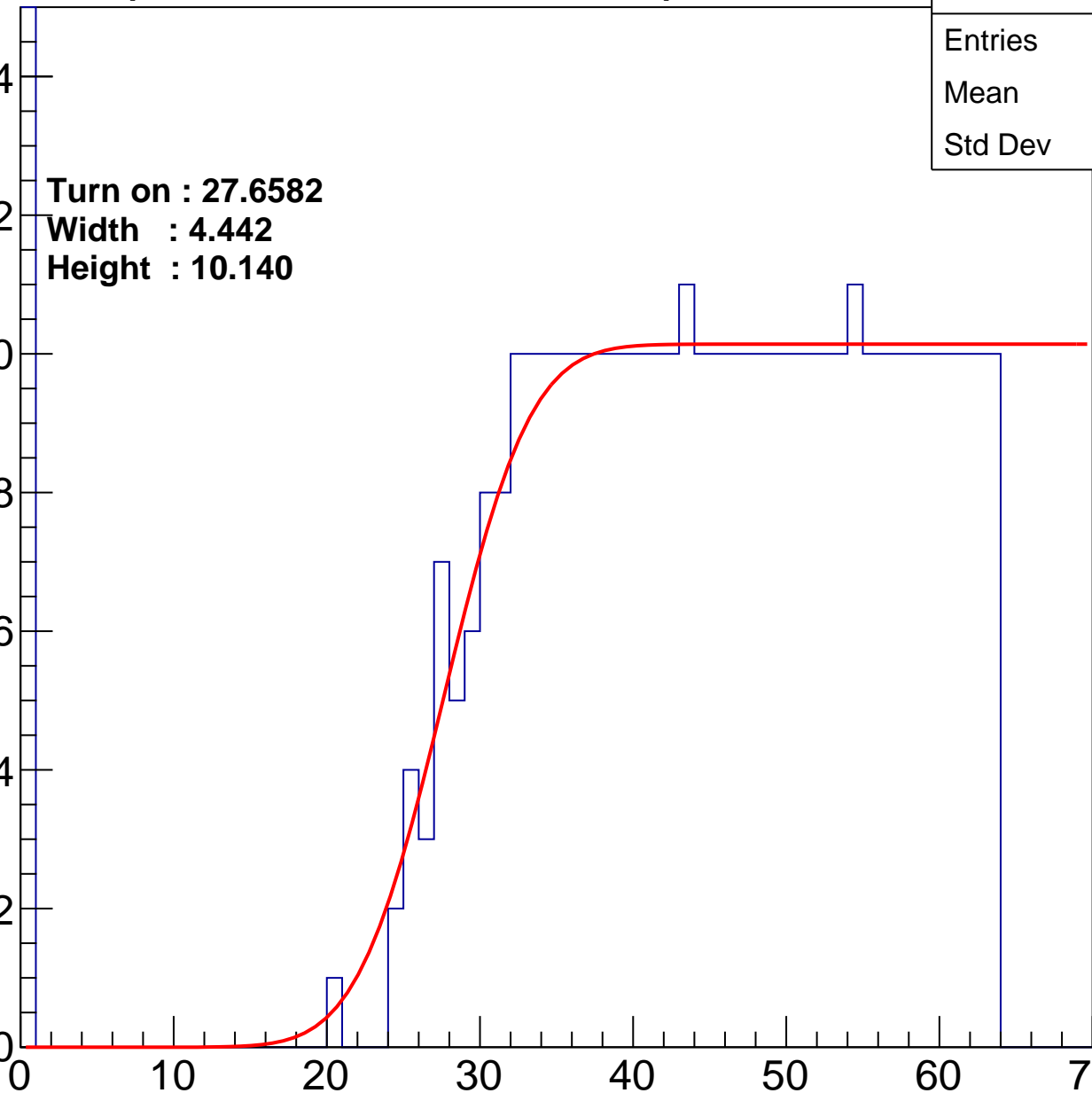
Width : 4.442

Height : 10.140

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch80

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	39.33
Std Dev	17.11

Turn on : 24.7388

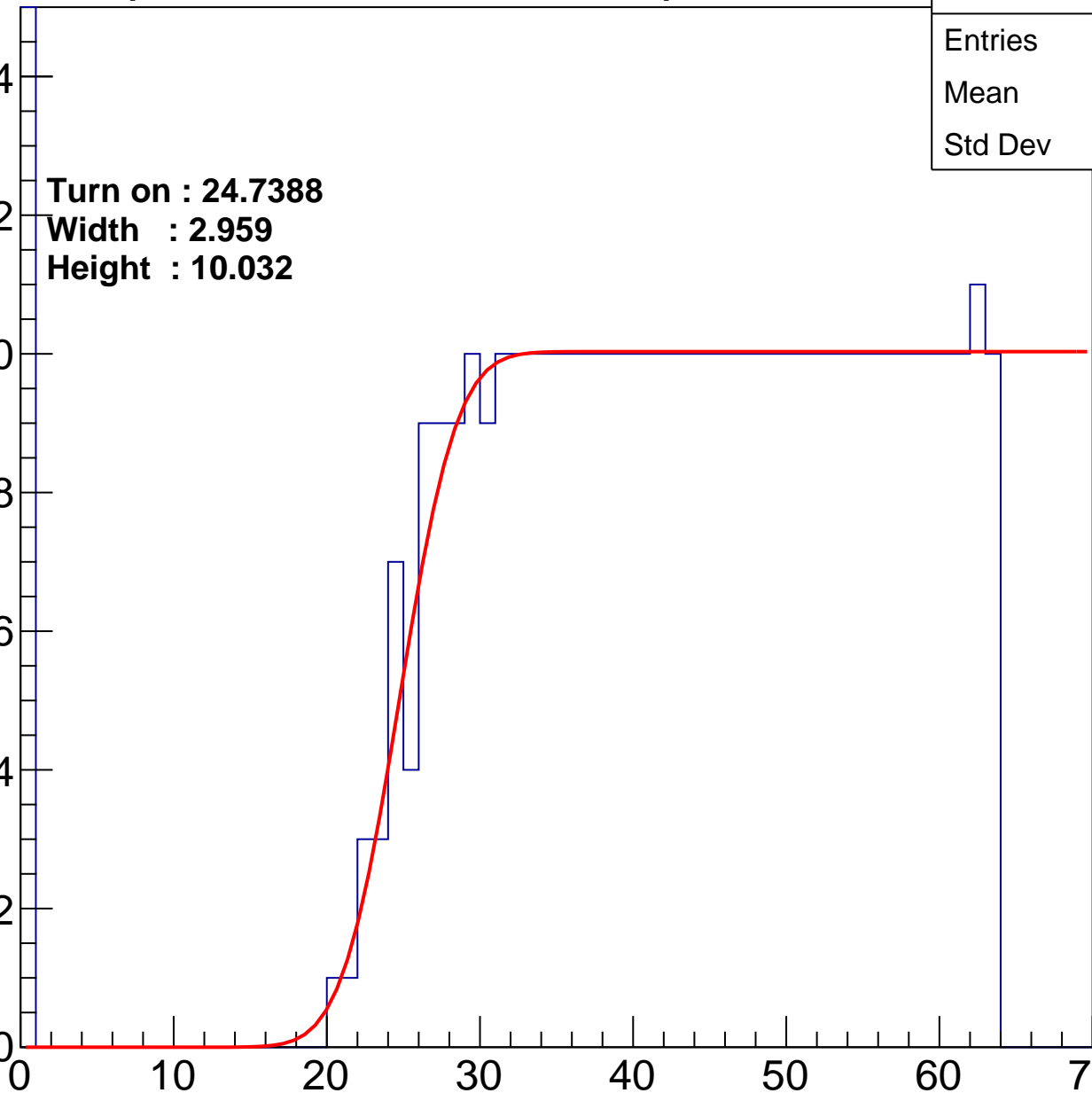
Width : 2.959

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch81

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.81
Std Dev	16.85

Turn on : 25.4656

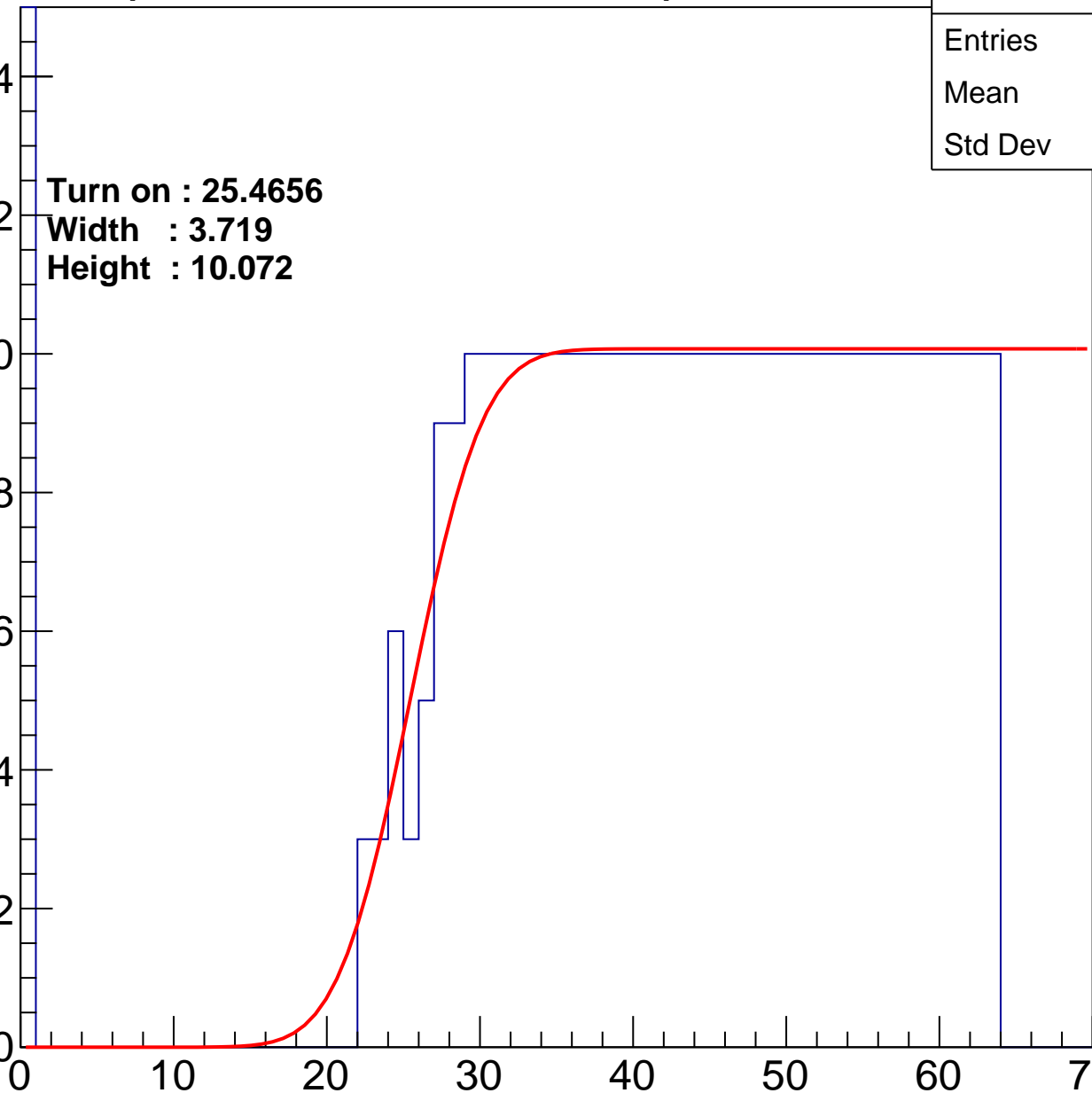
Width : 3.719

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch82

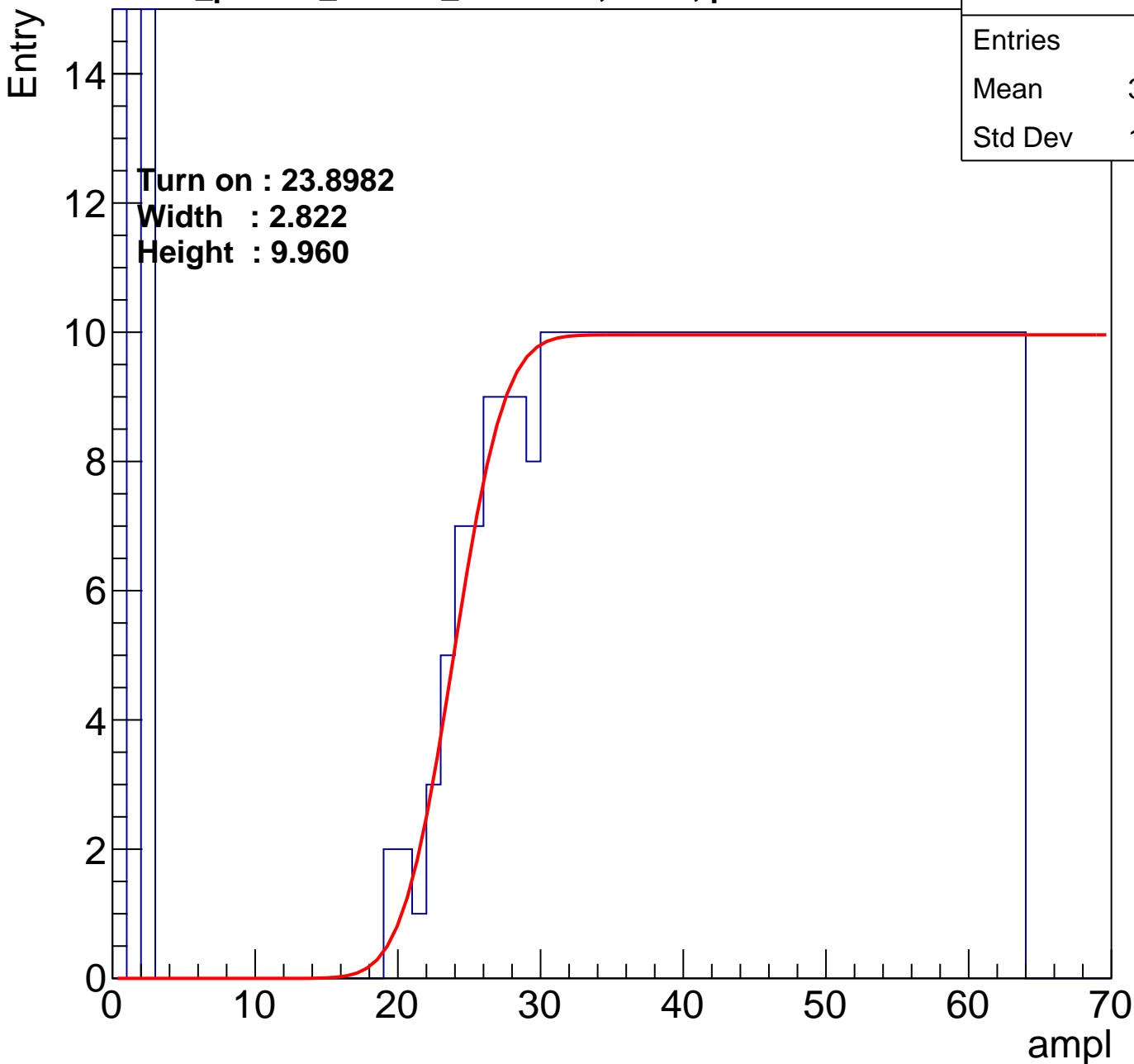
calib_packv5_041523_1651.root, FC#0, port C2

Entries	503
Mean	34.84
Std Dev	19.86

Turn on : 23.8982

Width : 2.822

Height : 9.960



B1L103S, U21-ch83

calib_packv5_041523_1651.root, FC#0, port C2

Entries	421
Mean	39.43
Std Dev	17.91

Turn on : 27.2537

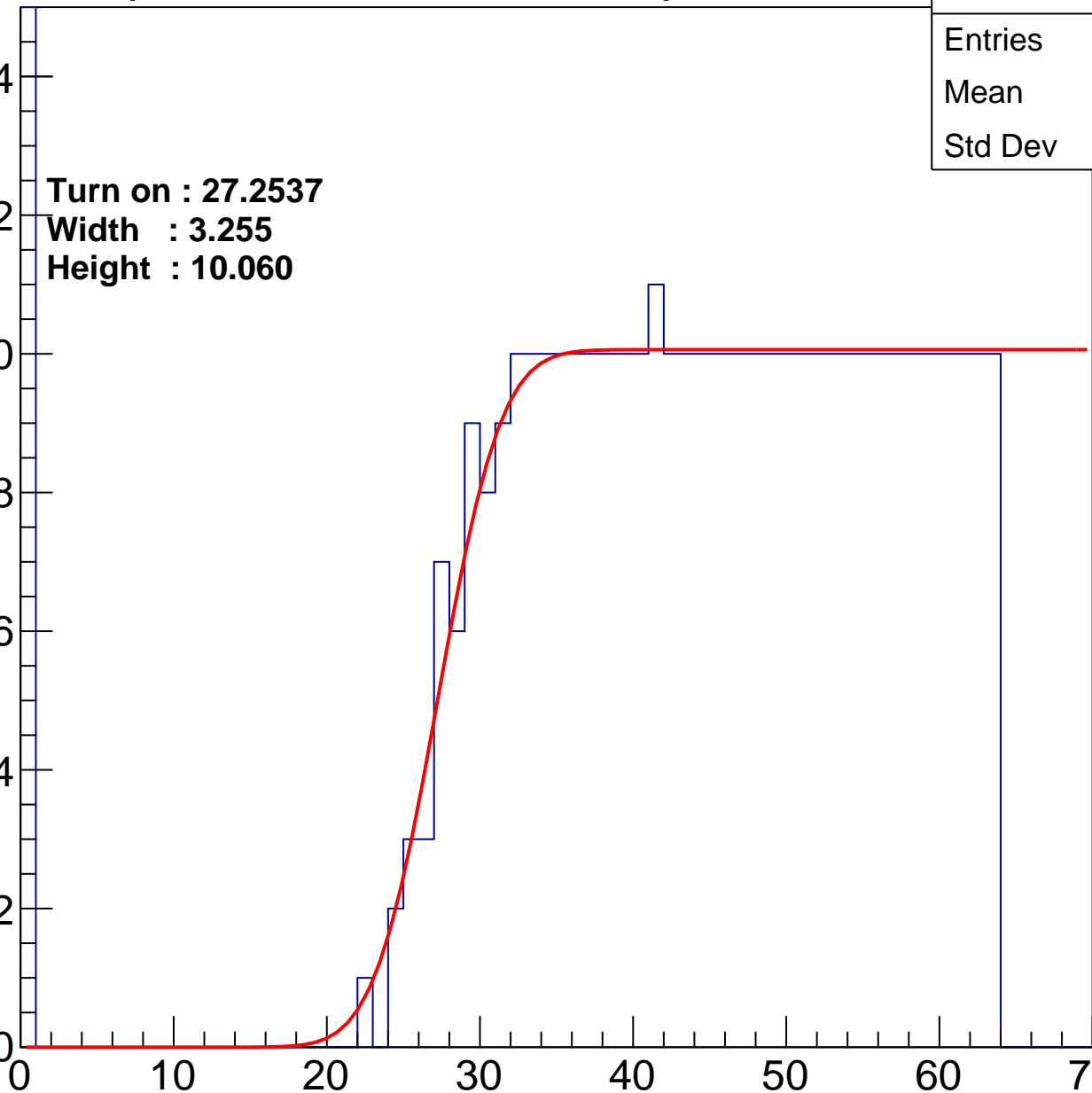
Width : 3.255

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch84

calib_packv5_041523_1651.root, FC#0, port C2

Entries	461
Mean	38.67
Std Dev	16.73

Turn on : 22.3862

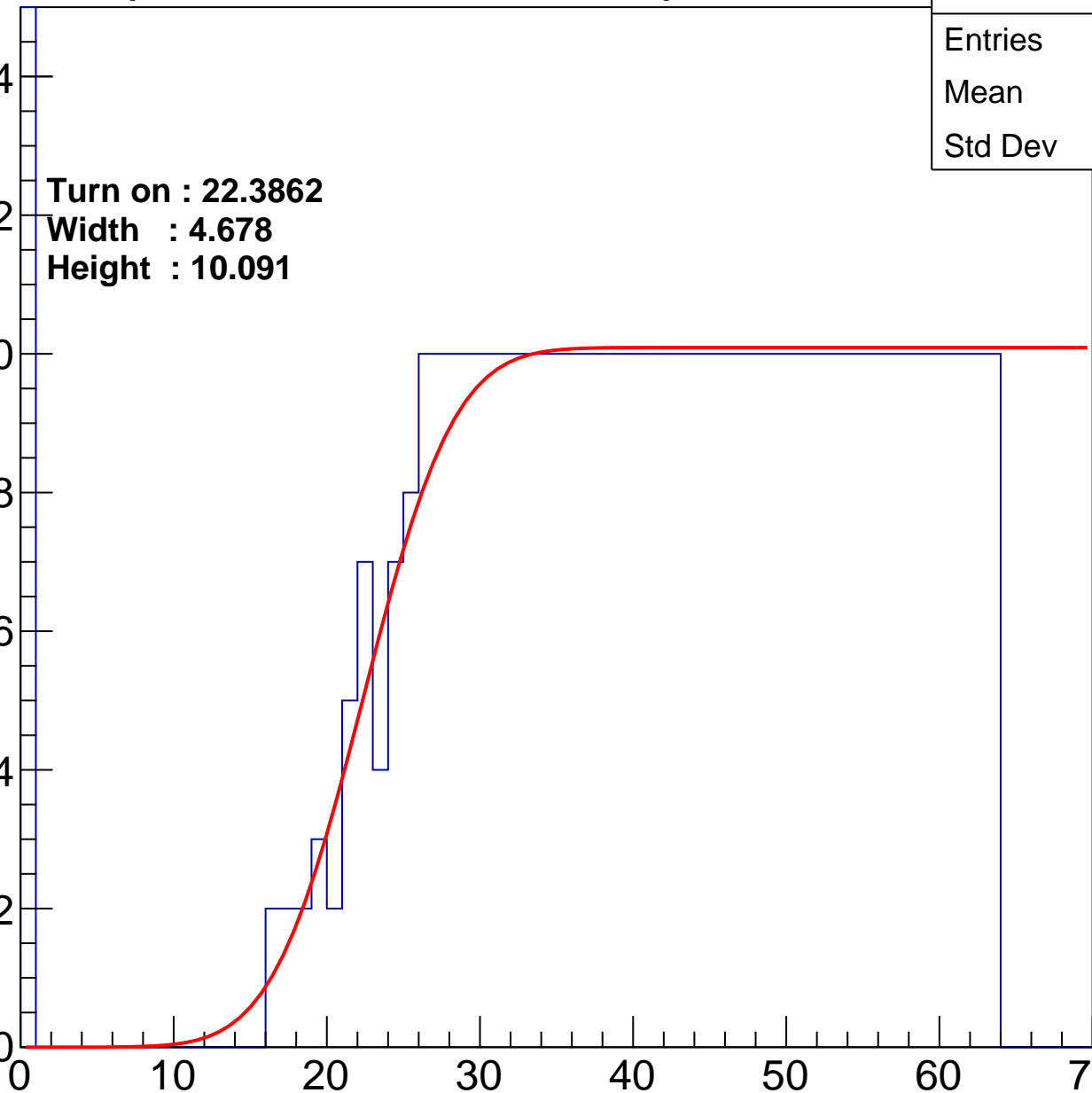
Width : 4.678

Height : 10.091

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch85

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	39.06
Std Dev	17.86

Turn on : 26.2629

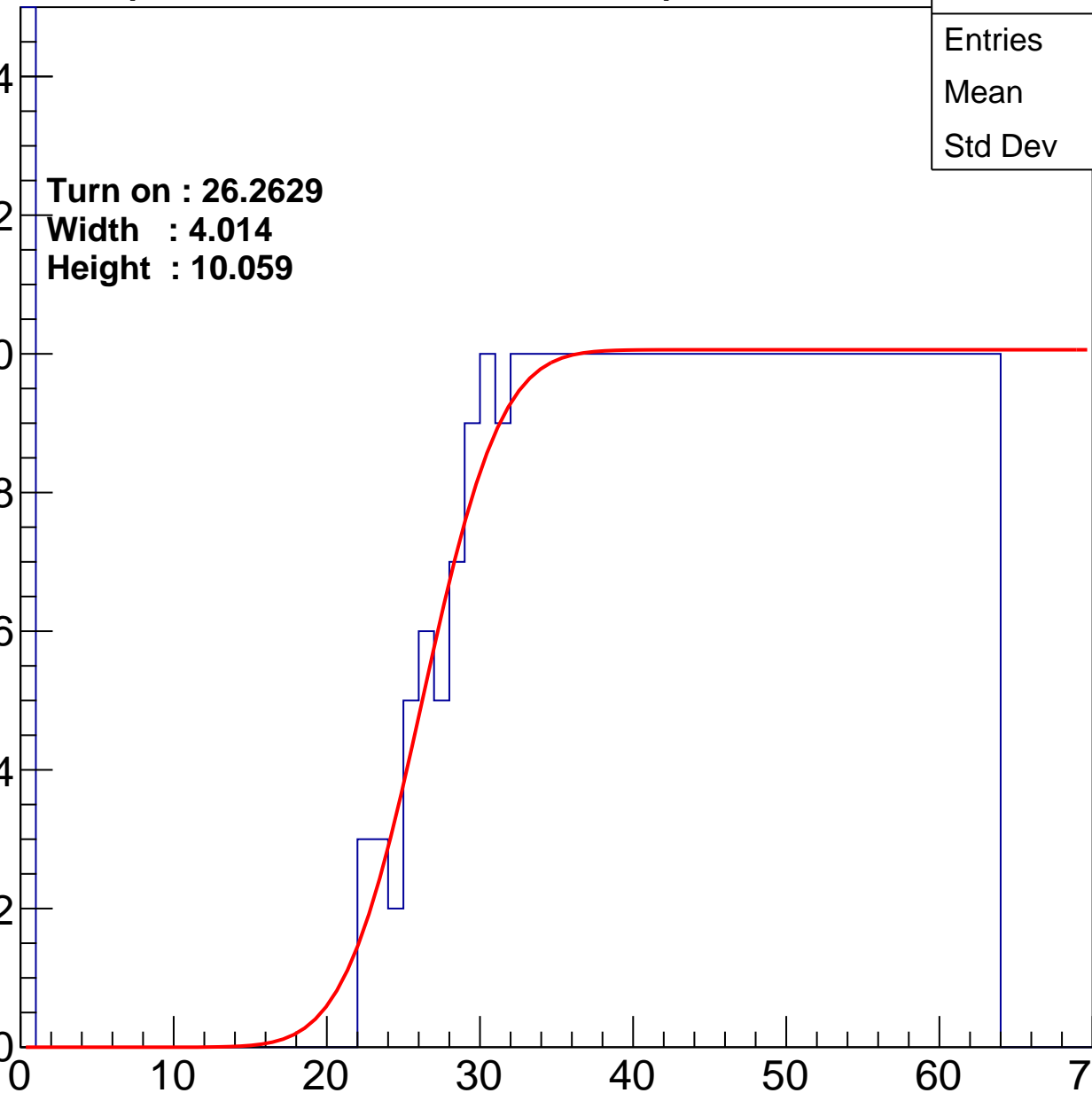
Width : 4.014

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch86

calib_packv5_041523_1651.root, FC#0, port C2

Entries	461
Mean	37.71
Std Dev	18.25

Turn on : 23.9801

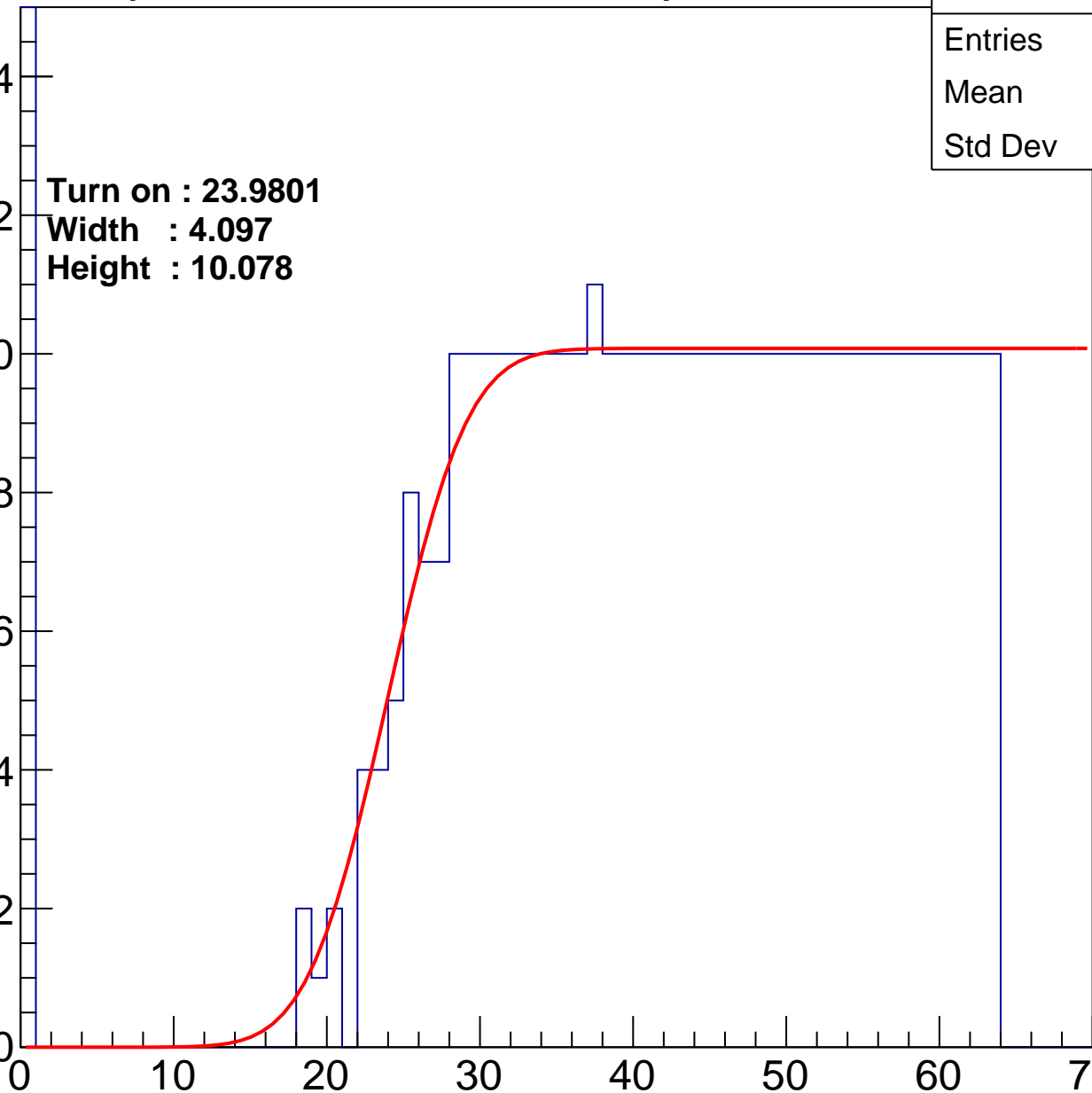
Width : 4.097

Height : 10.078

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch87

calib_packv5_041523_1651.root, FC#0, port C2

Entries	466
Mean	37.97
Std Dev	17.58

Turn on : 22.6403

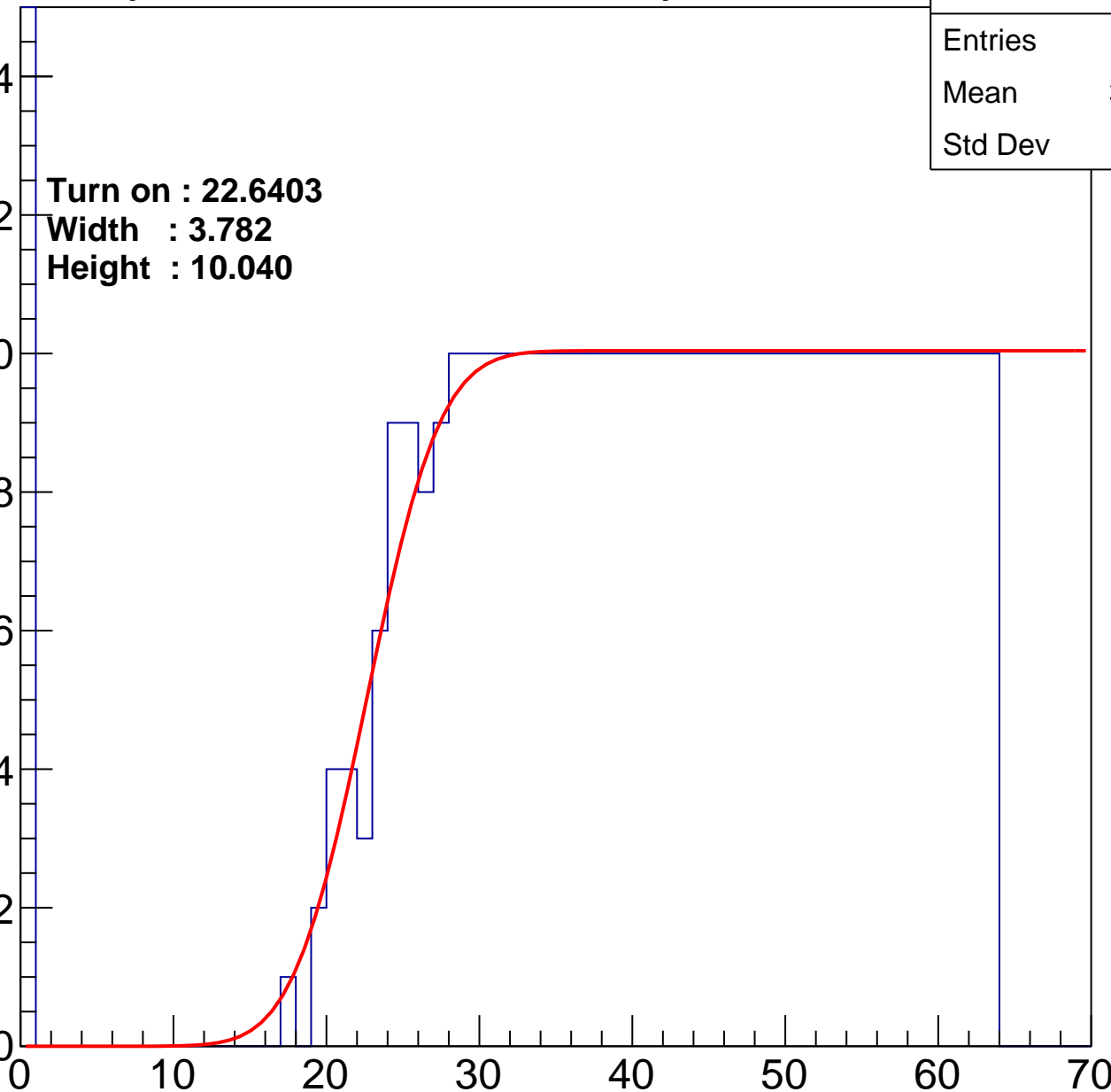
Width : 3.782

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch88

calib_packv5_041523_1651.root, FC#0, port C2

Entries	451
Mean	38.06
Std Dev	18.37

Turn on : 25.2484

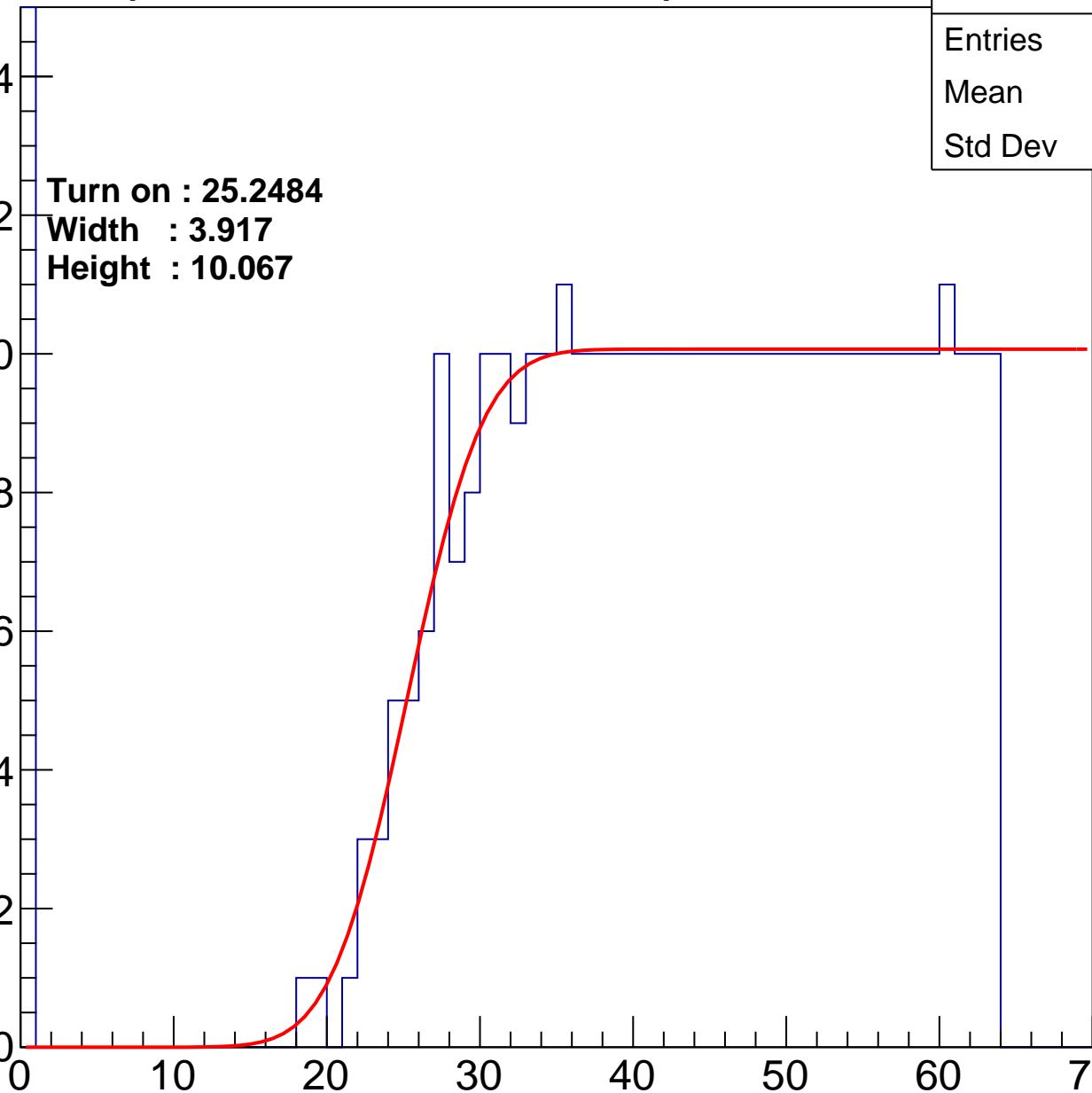
Width : 3.917

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch89

calib_packv5_041523_1651.root, FC#0, port C2

Entries	456
Mean	38.17
Std Dev	18.01

Turn on : 24.0219

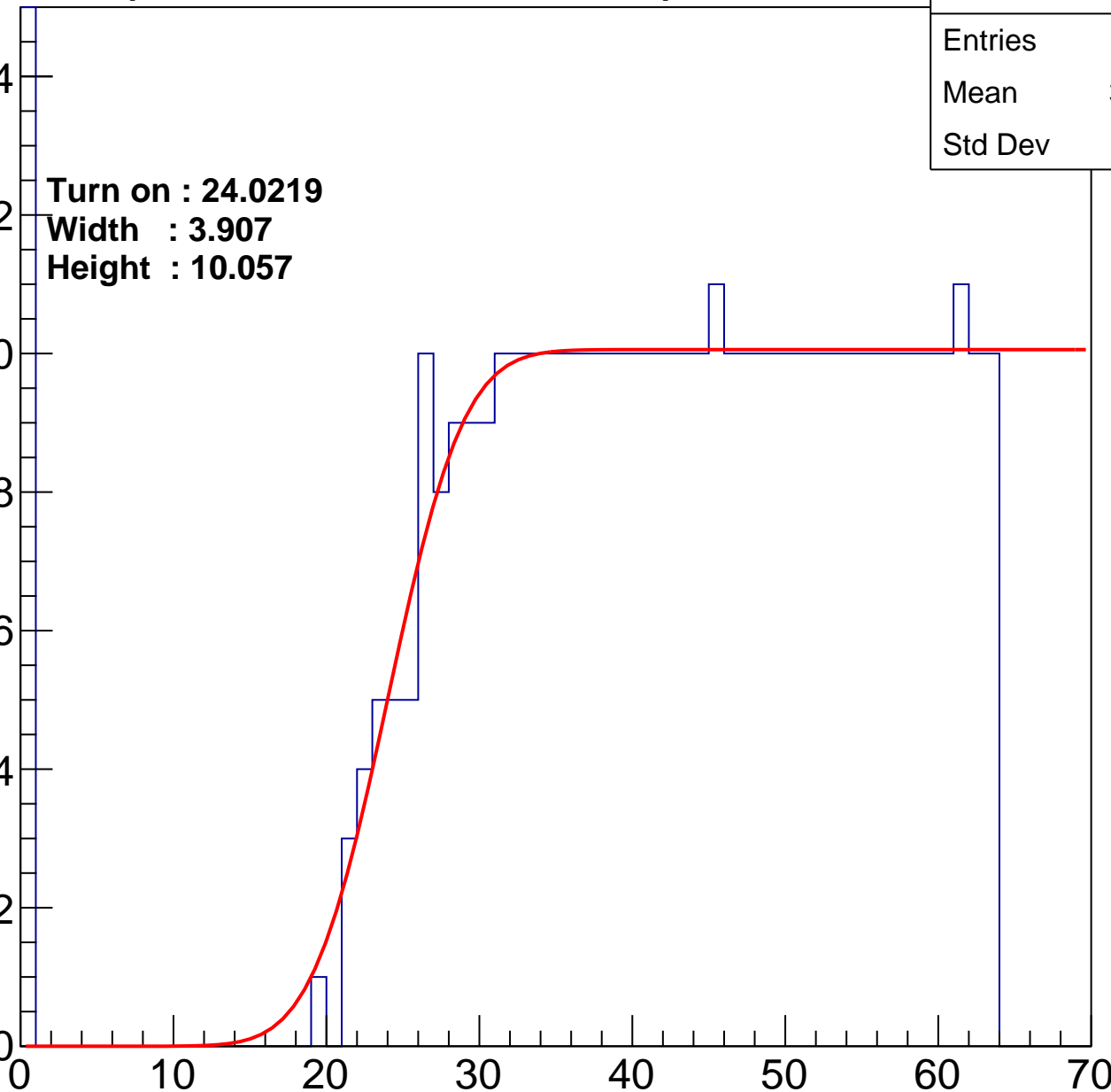
Width : 3.907

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch90

calib_packv5_041523_1651.root, FC#0, port C2

Entries	469
Mean	37.83
Std Dev	17.61

Turn on : 23.2049

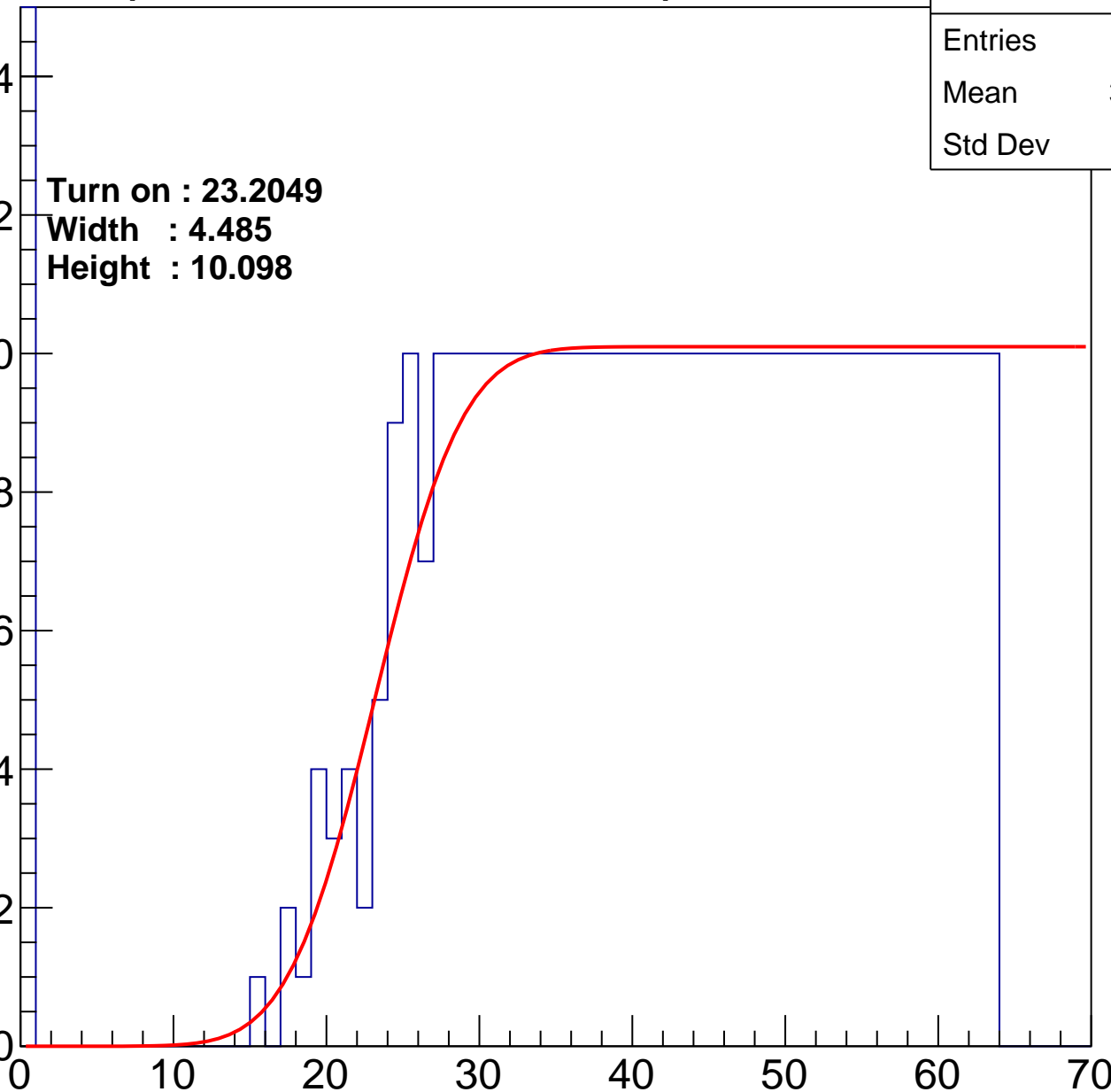
Width : 4.485

Height : 10.098

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch91

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	39.91
Std Dev	16.87

Turn on : 25.8955

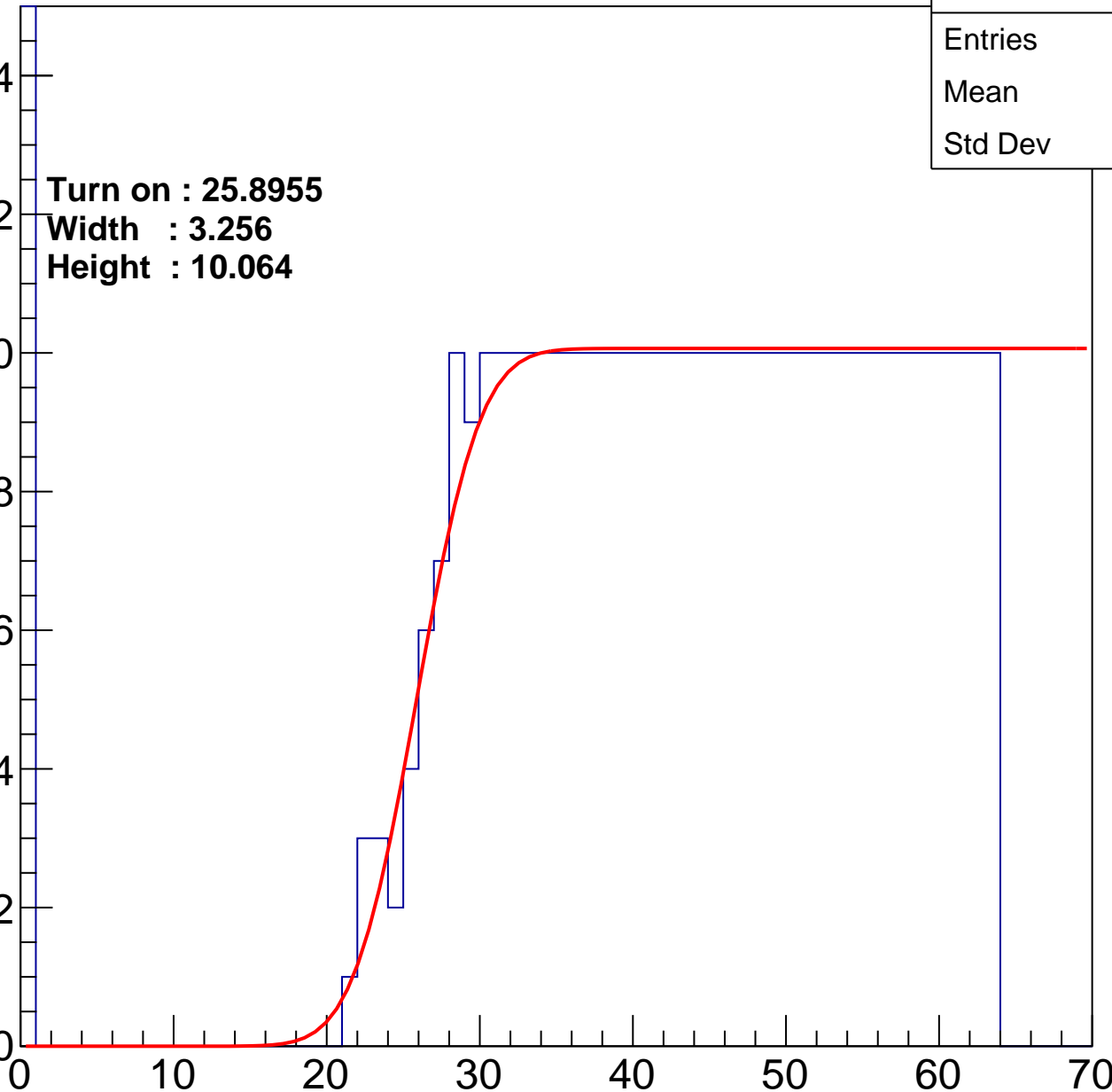
Width : 3.256

Height : 10.064

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch92

calib_packv5_041523_1651.root, FC#0, port C2

Entries	454
Mean	38.55
Std Dev	17.44

Turn on : 23.5659

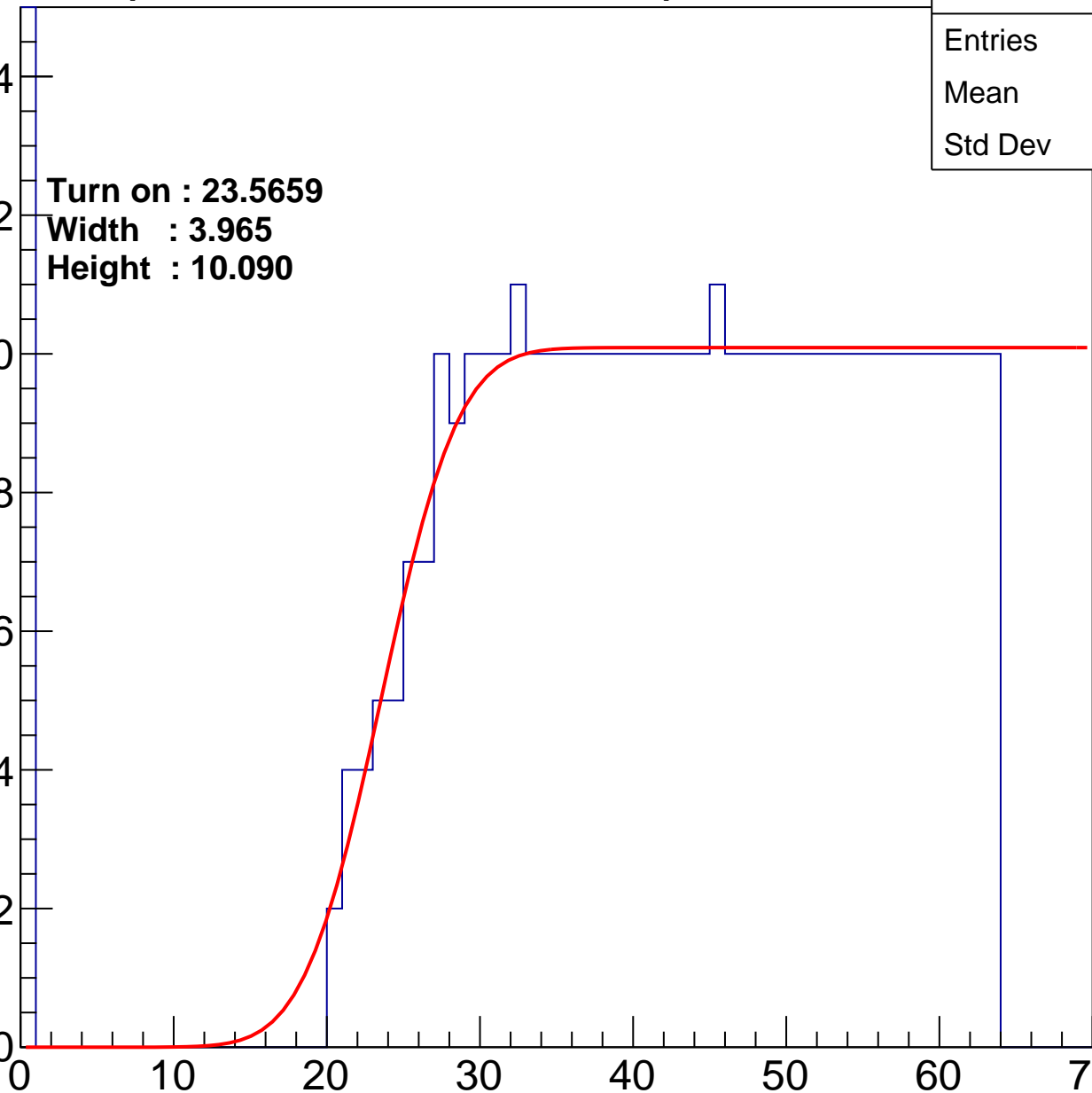
Width : 3.965

Height : 10.090

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch93

calib_packv5_041523_1651.root, FC#0, port C2

Entries	466
Mean	37.56
Std Dev	18.19

Turn on : 23.4201

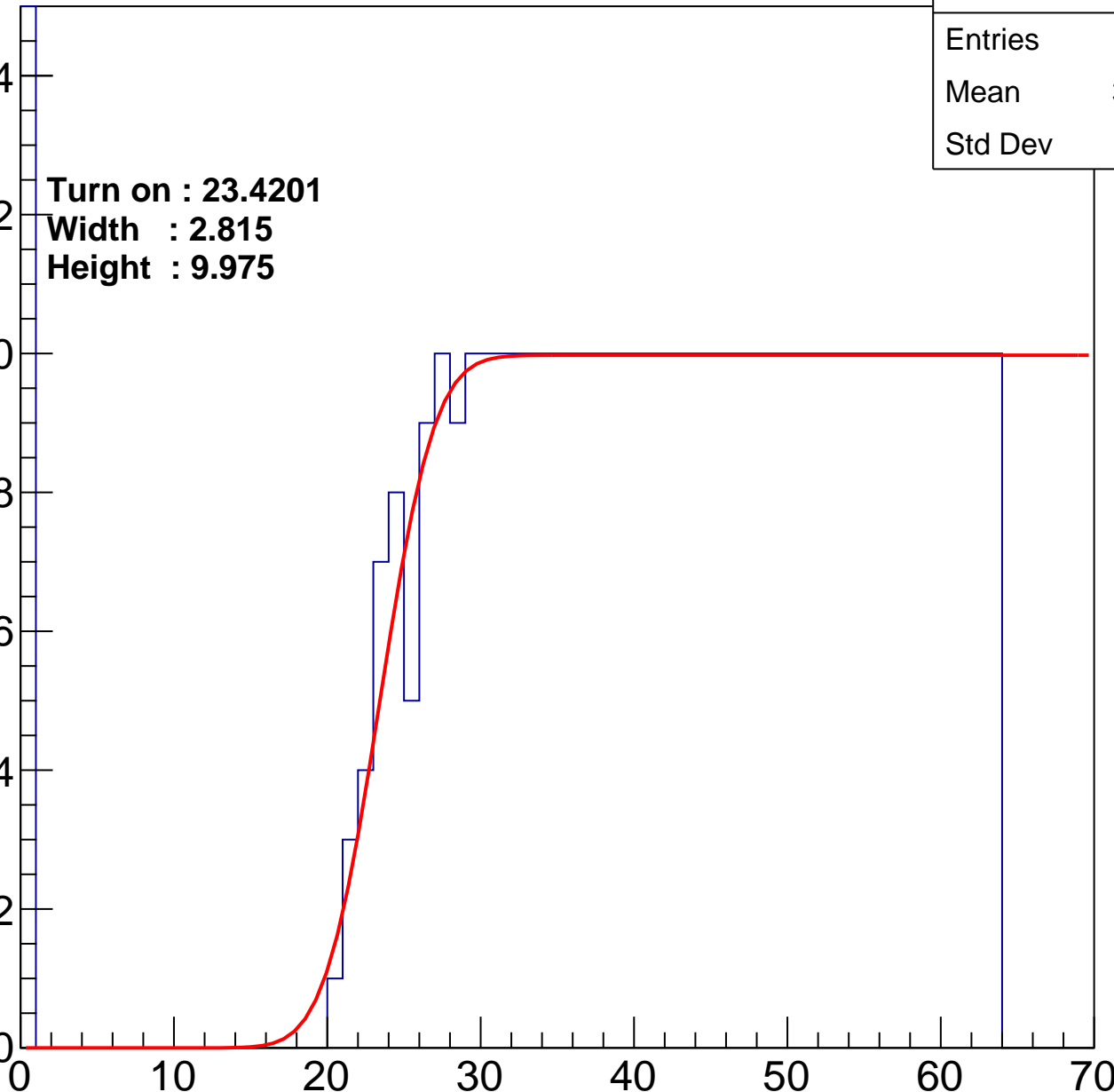
Width : 2.815

Height : 9.975

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch94

calib_packv5_041523_1651.root, FC#0, port C2

Entries	461
Mean	37.81
Std Dev	18.06

Turn on : 23.2941

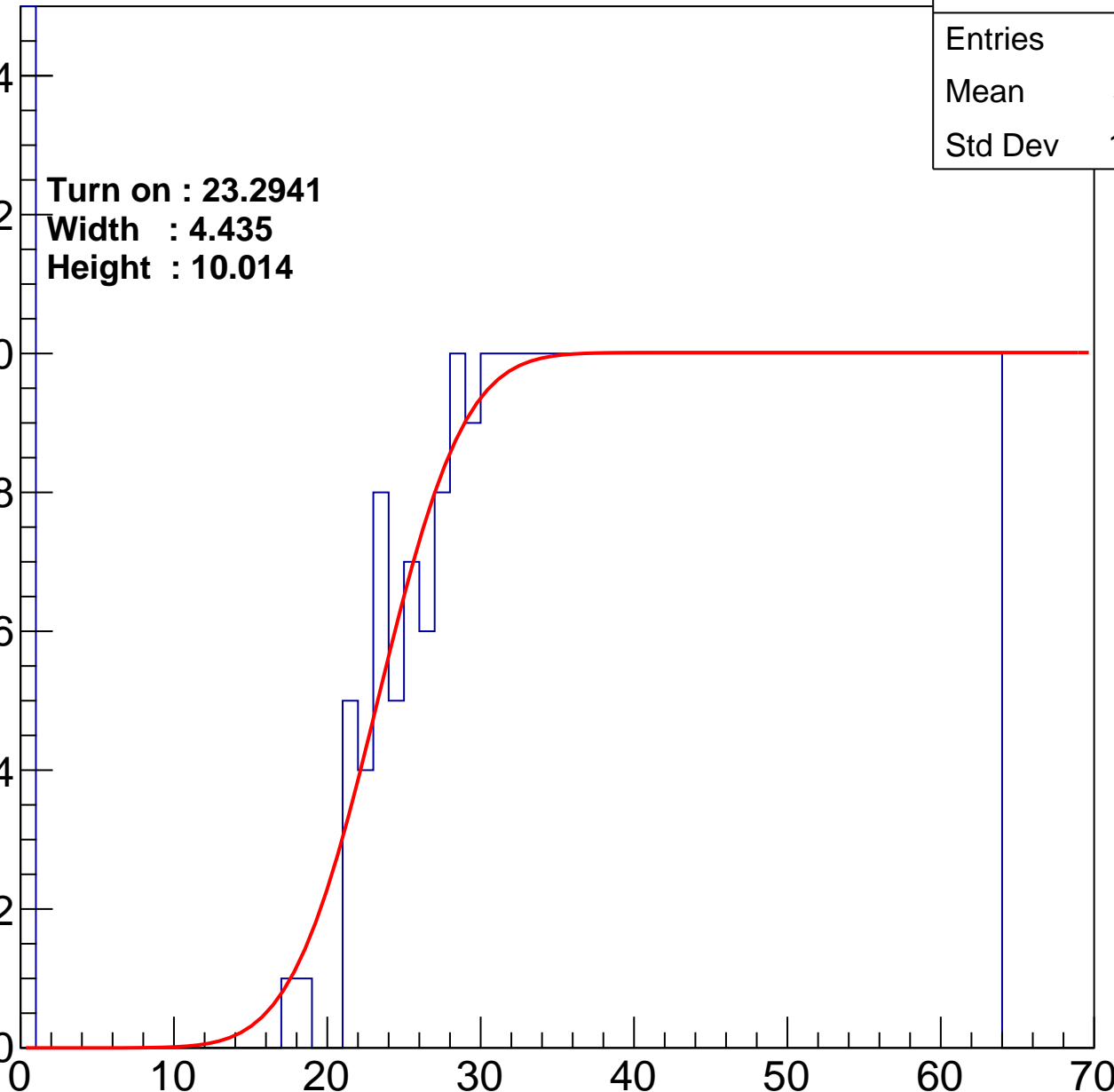
Width : 4.435

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch95

calib_packv5_041523_1651.root, FC#0, port C2

Entries	454
Mean	37.3
Std Dev	19.11

Turn on : 25.8562

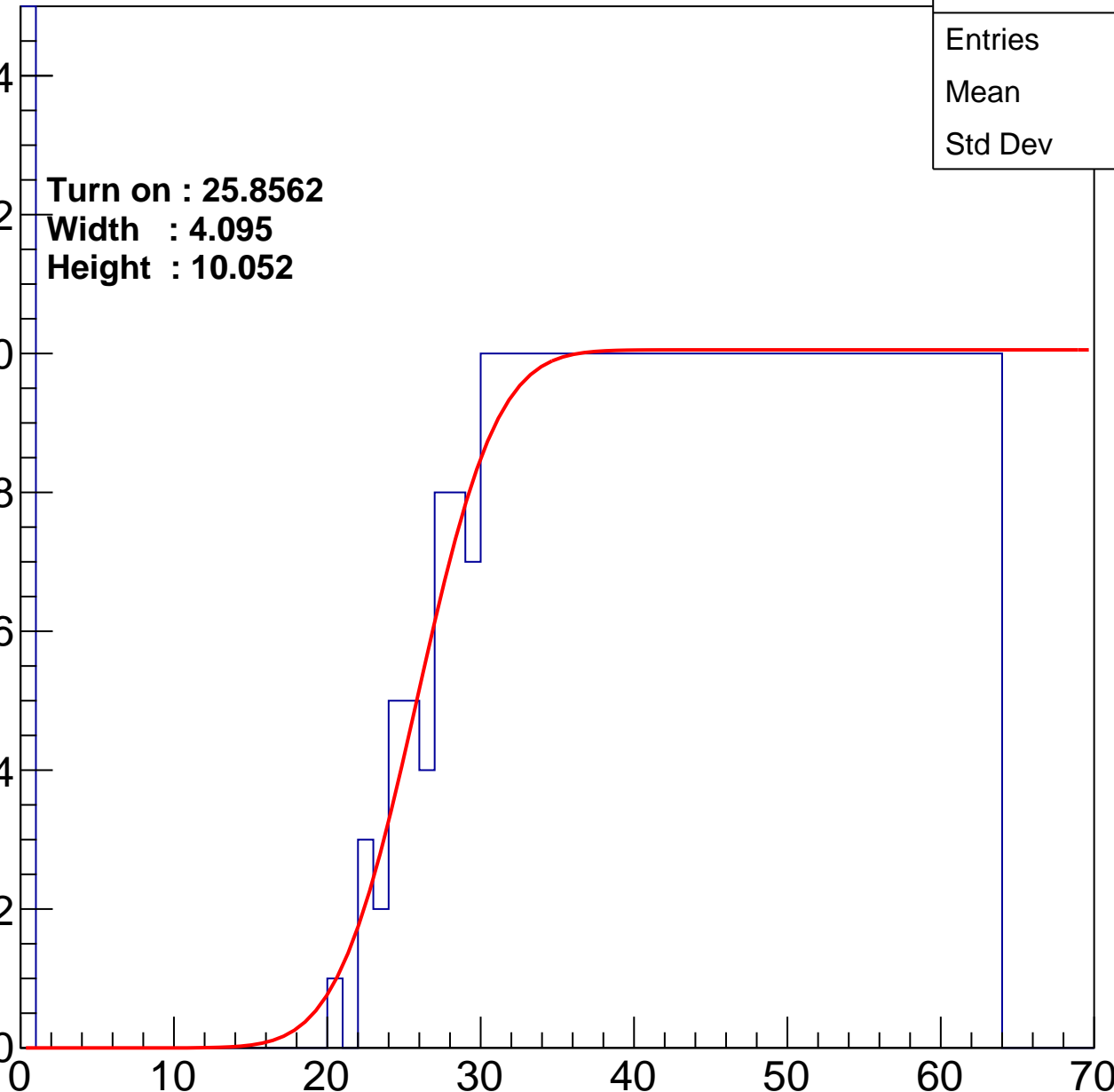
Width : 4.095

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch96

calib_packv5_041523_1651.root, FC#0, port C2

Entries	456
Mean	38.77
Std Dev	16.95

Turn on : 22.8856

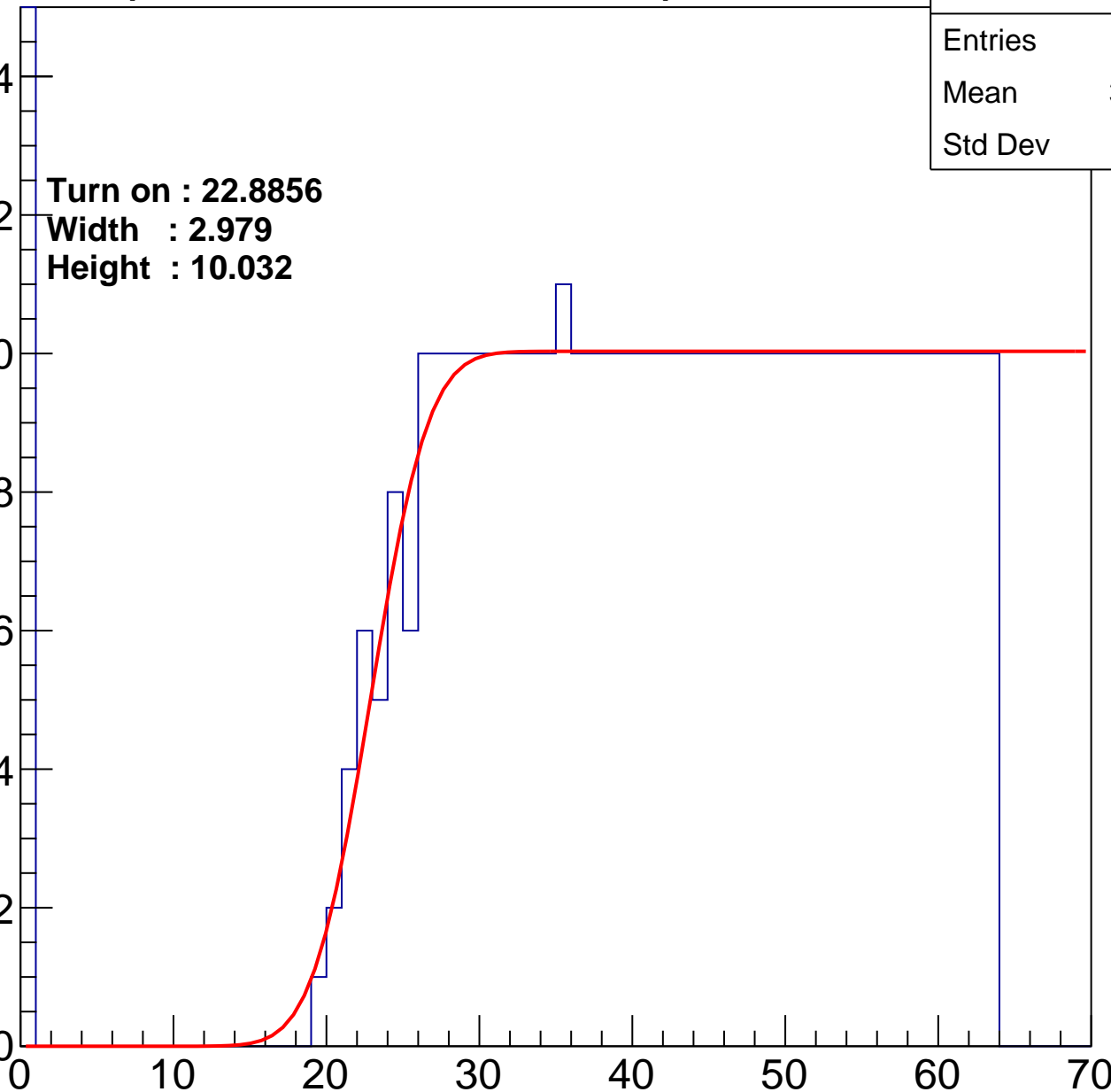
Width : 2.979

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch97

calib_packv5_041523_1651.root, FC#0, port C2

Entries	447
Mean	38.68
Std Dev	17.53

Turn on : 24.7345

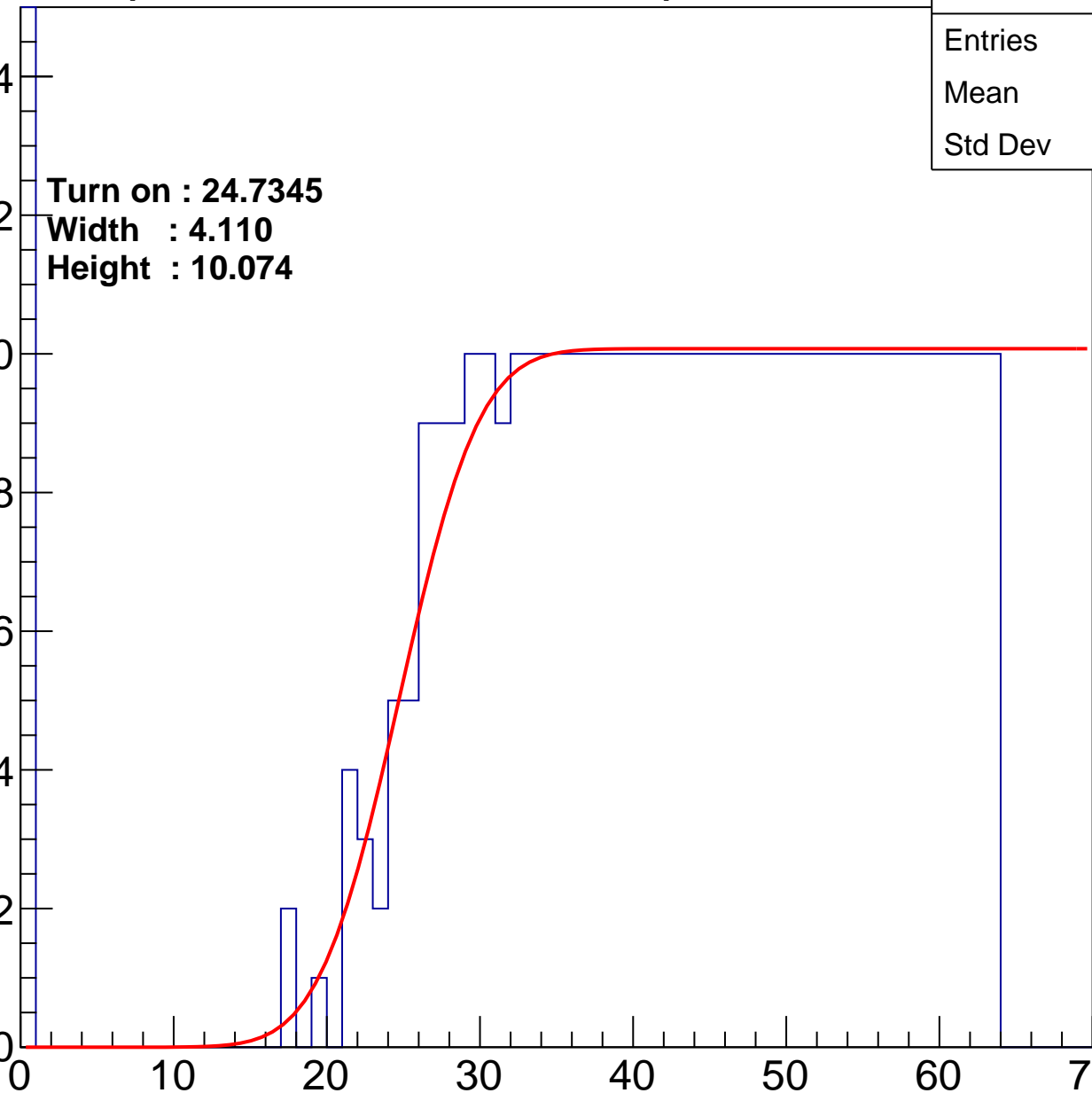
Width : 4.110

Height : 10.074

Entry

14
12
10
8
6
4
2
0

ampl

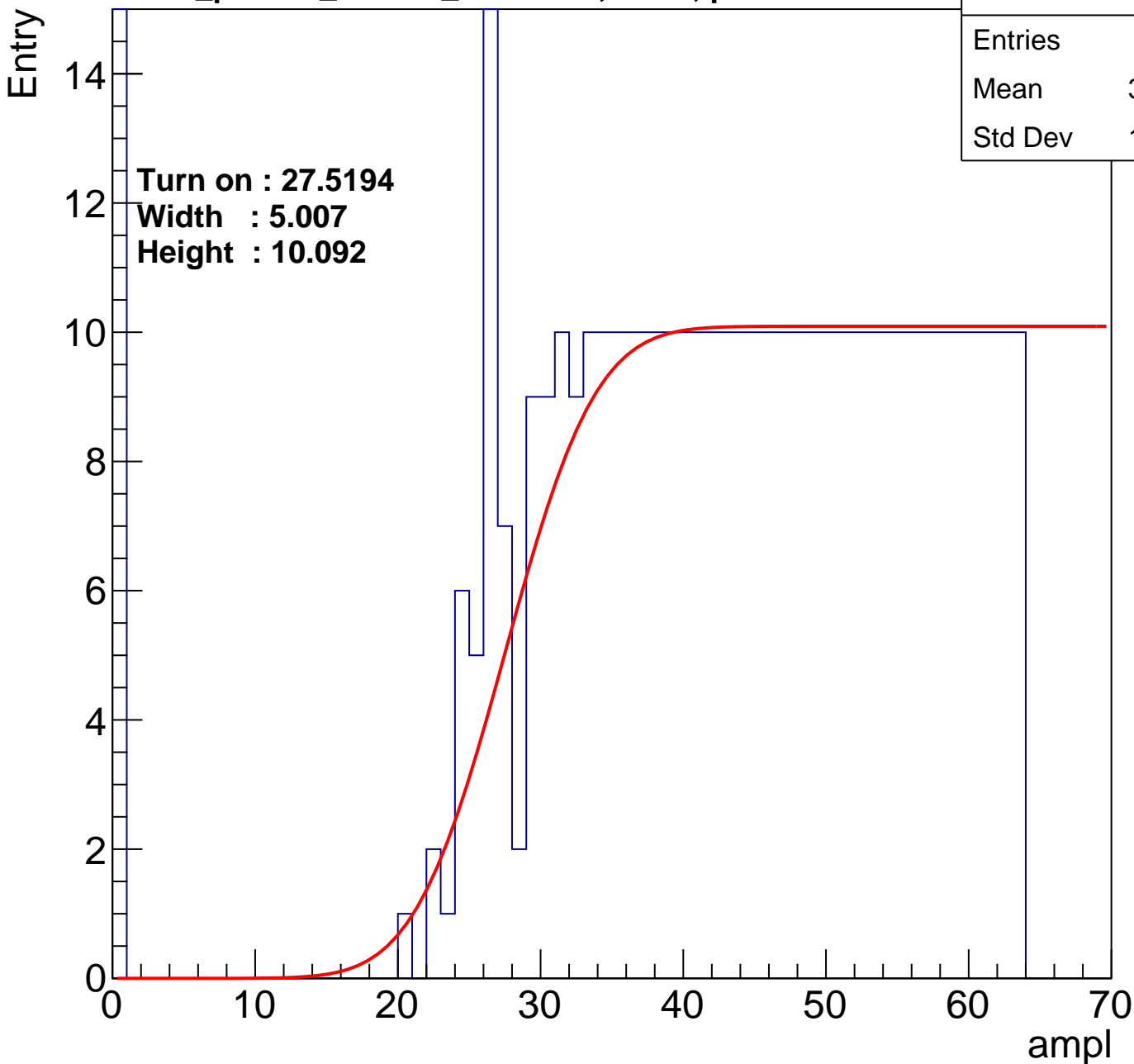


B1L103S, U21-ch98

calib_packv5_041523_1651.root, FC#0, port C2

Entries	450
Mean	38.24
Std Dev	18.02

Turn on : 27.5194
Width : 5.007
Height : 10.092



B1L103S, U21-ch99

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	39.24
Std Dev	17.27

Turn on : 25.2892

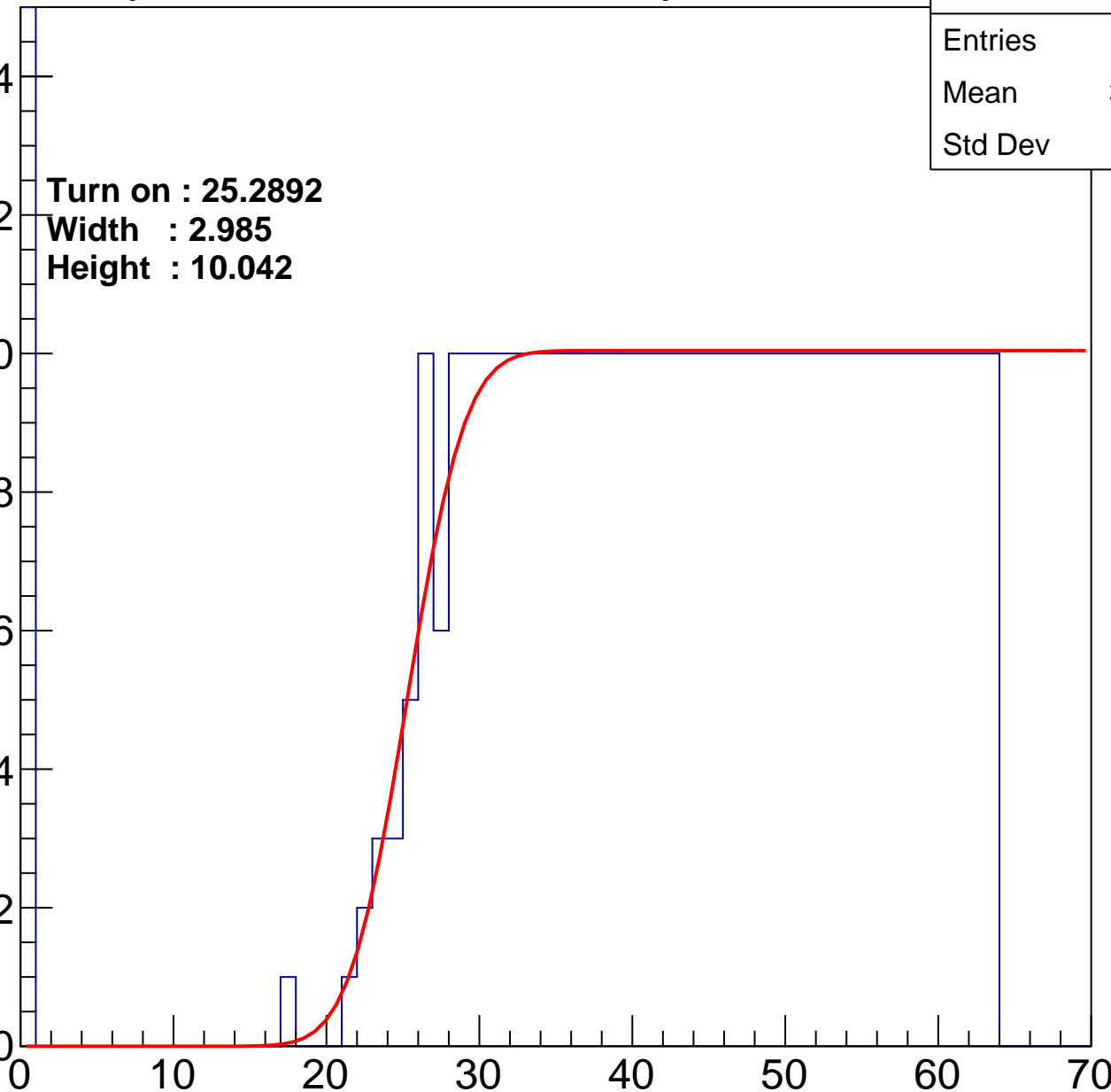
Width : 2.985

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch100

calib_packv5_041523_1651.root, FC#0, port C2

Entries	457
Mean	38.3
Std Dev	17.62

Turn on : 23.4949

Width : 4.158

Height : 10.057

Entry

14

12

10

8

6

4

2

0

0

10

20

30

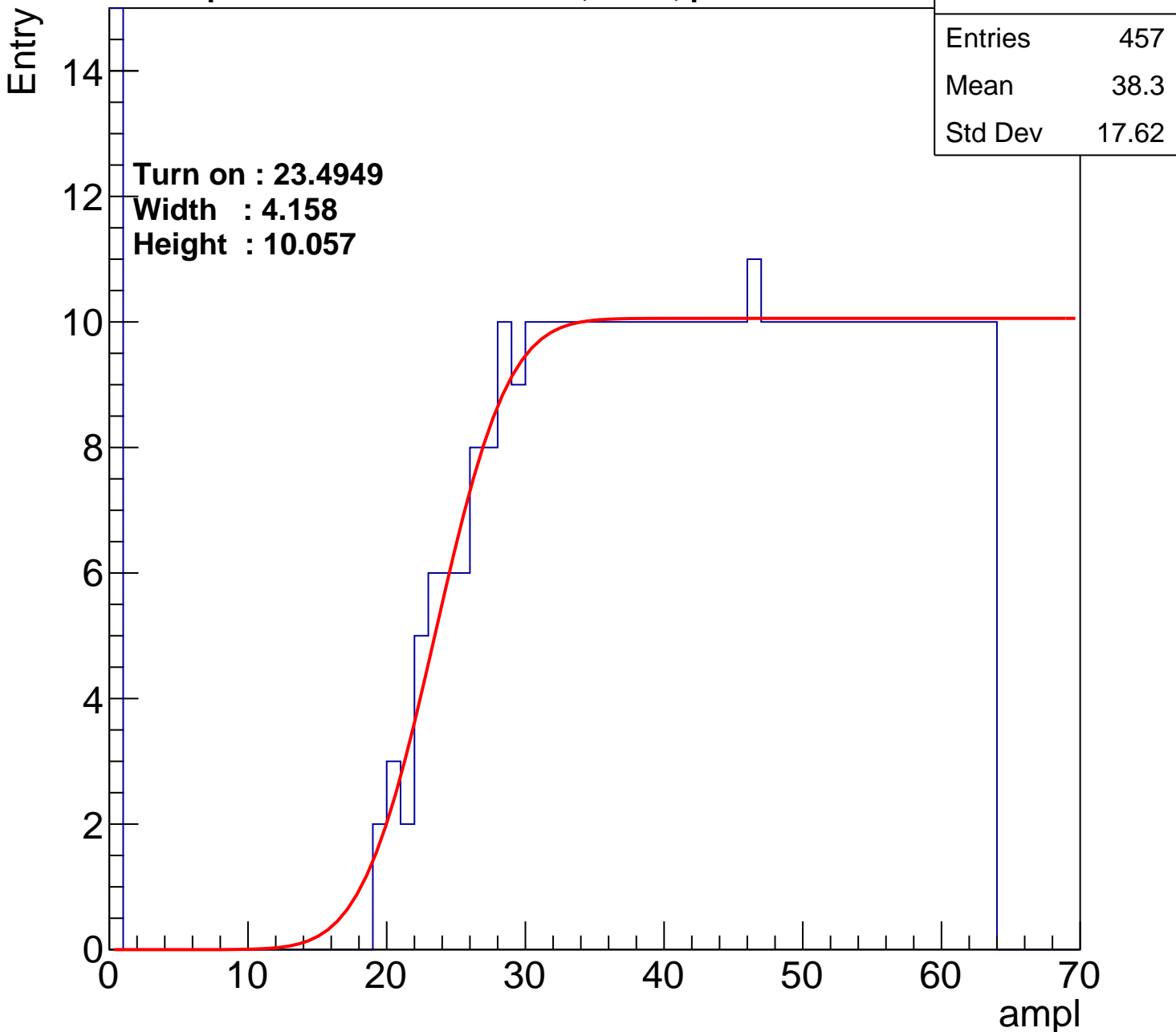
40

50

60

70

ampl



B1L103S, U21-ch101

calib_packv5_041523_1651.root, FC#0, port C2

Entries	447
Mean	38.36
Std Dev	17.99

Turn on : 24.7136

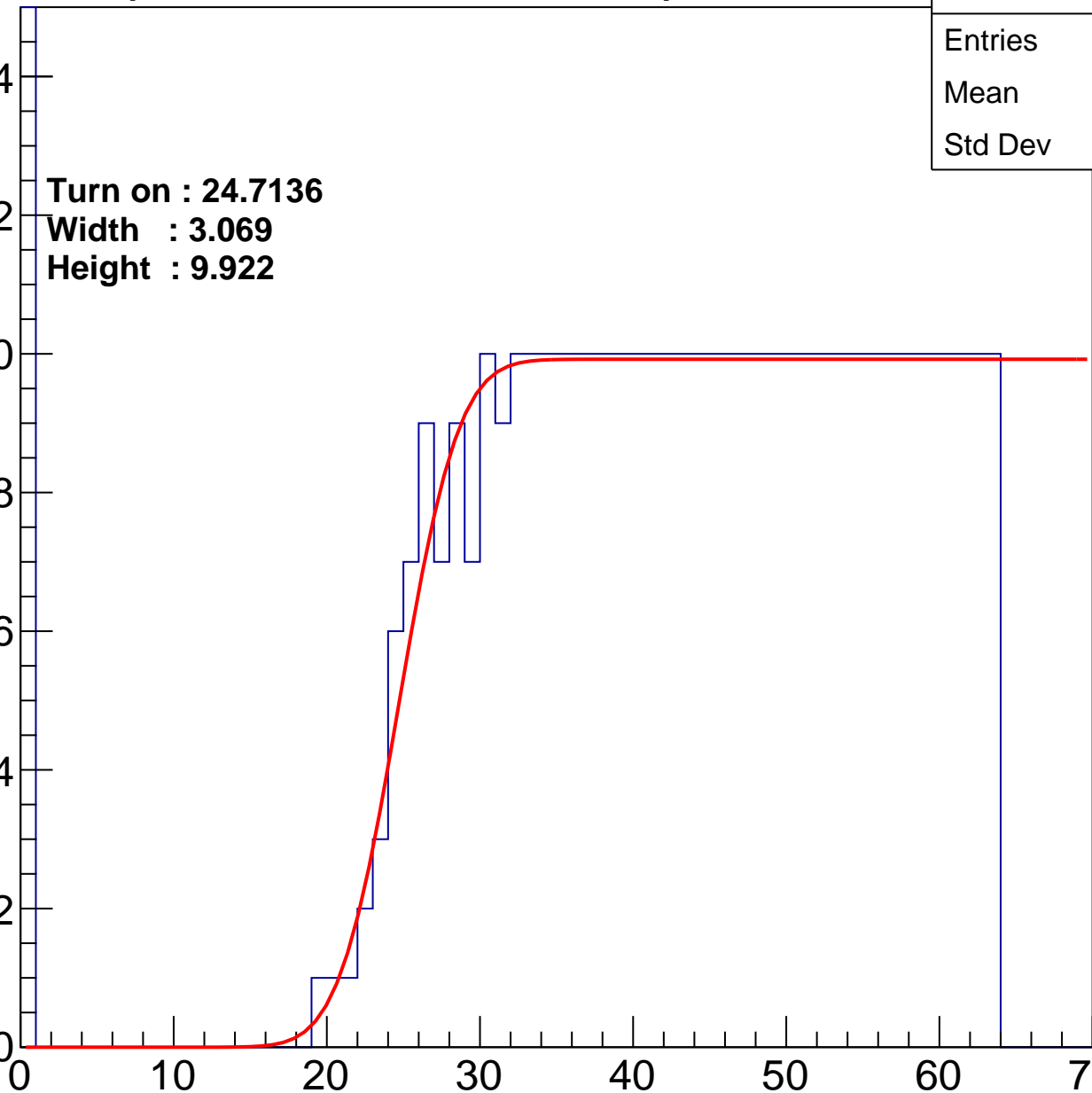
Width : 3.069

Height : 9.922

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch102

calib_packv5_041523_1651.root, FC#0, port C2

Entries	455
Mean	38.26
Std Dev	17.72

Turn on : 24.0602

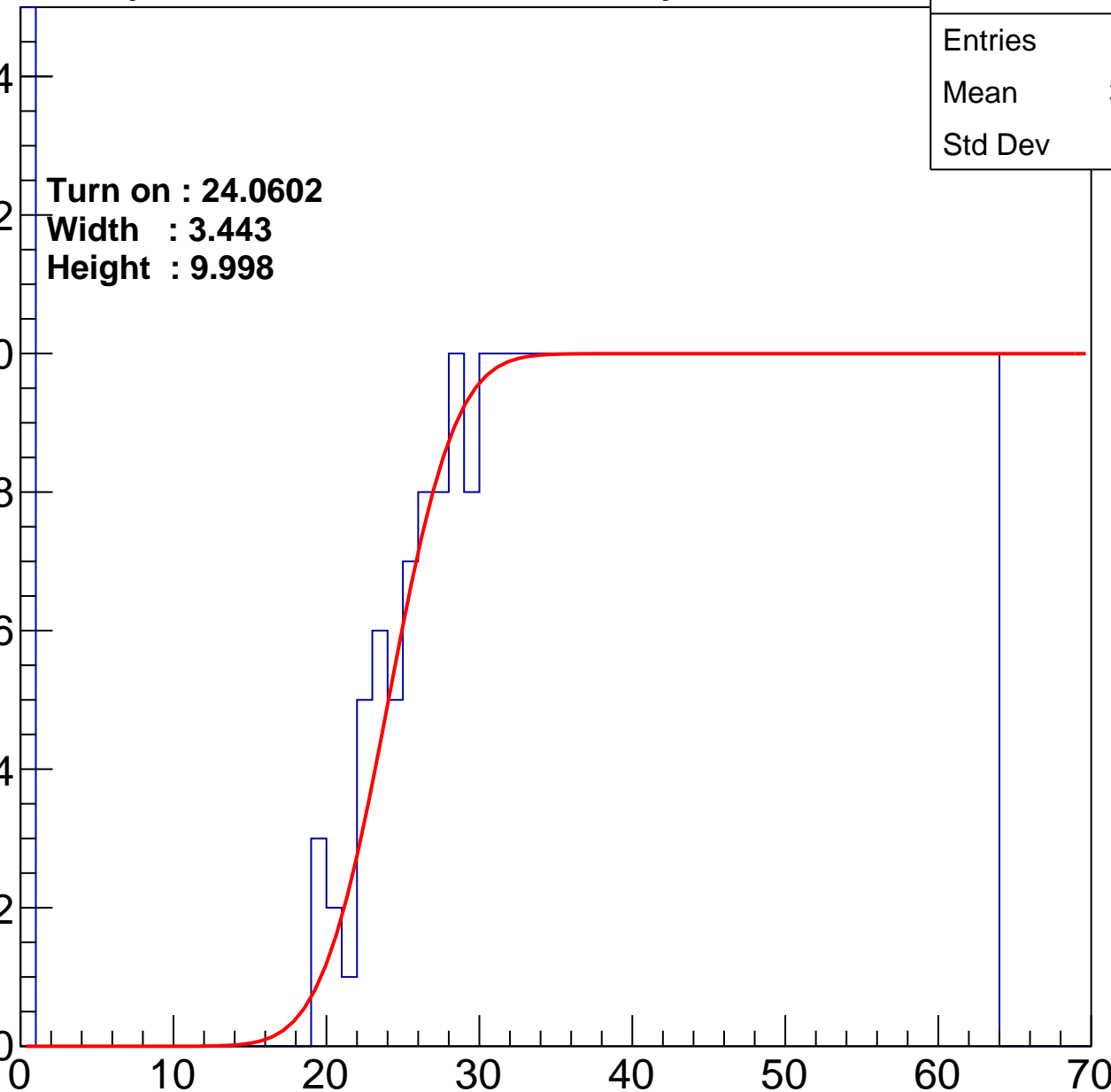
Width : 3.443

Height : 9.998

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch103

calib_packv5_041523_1651.root, FC#0, port C2

Entries	450
Mean	38.5
Std Dev	17.65

Turn on : 24.0160

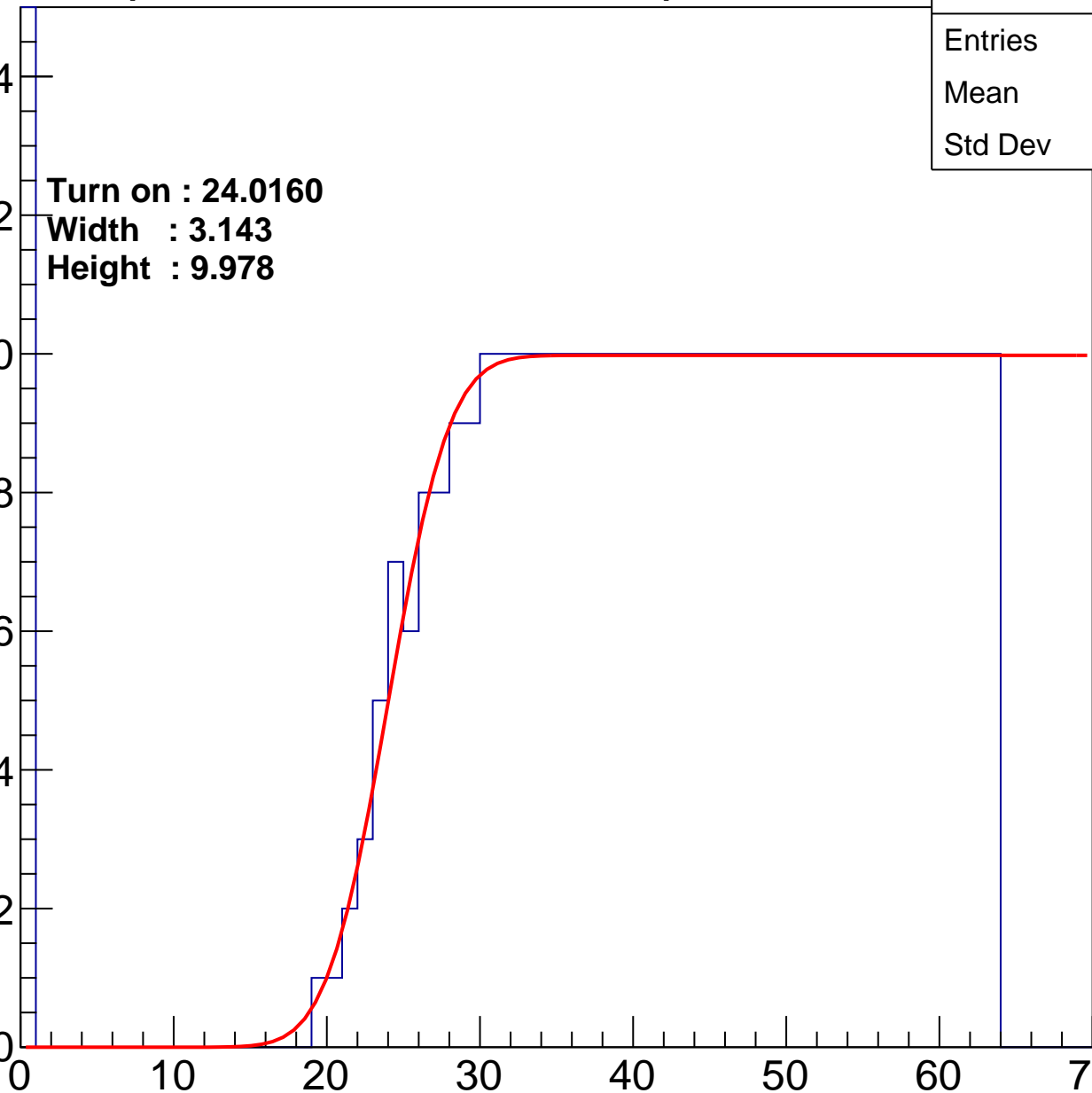
Width : 3.143

Height : 9.978

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch104

calib_packv5_041523_1651.root, FC#0, port C2

Entries	451
Mean	38.6
Std Dev	17.47

Turn on : 24.1253

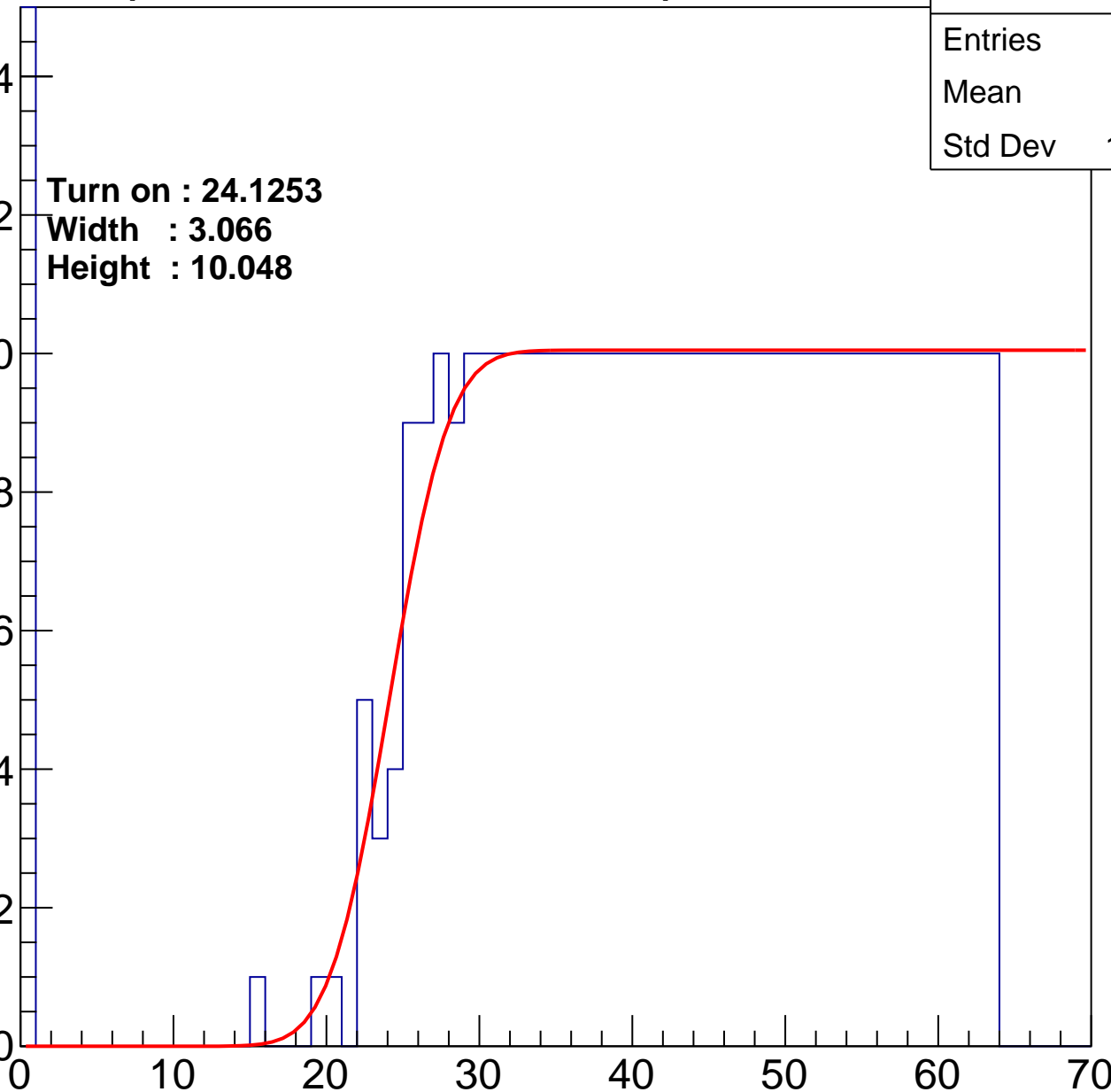
Width : 3.066

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch105

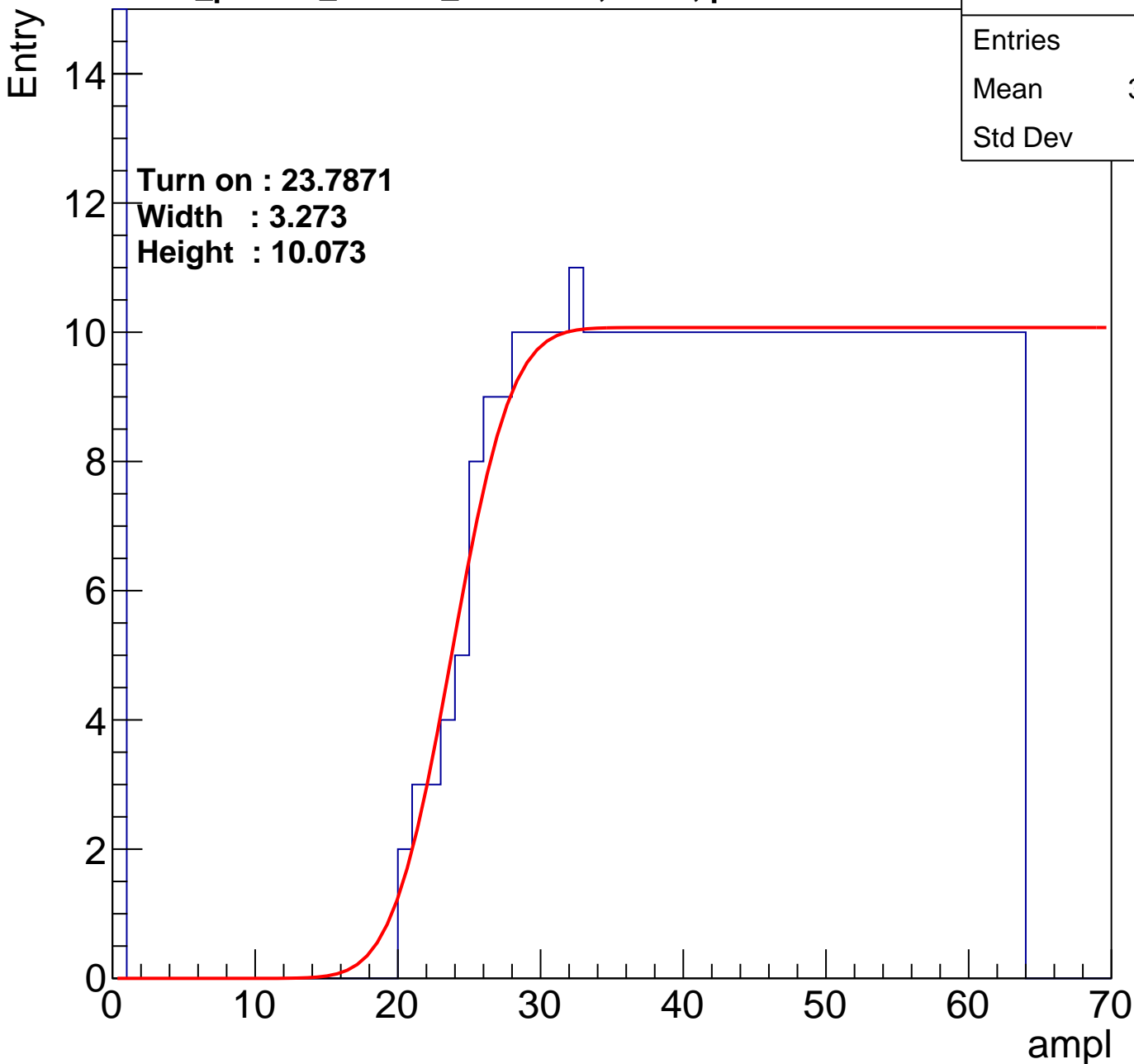
calib_packv5_041523_1651.root, FC#0, port C2

Entries	464
Mean	37.65
Std Dev	18.2

Turn on : 23.7871

Width : 3.273

Height : 10.073



B1L103S, U21-ch106

calib_packv5_041523_1651.root, FC#0, port C2

Entries	480
Mean	37.36
Std Dev	17.74

Turn on : 21.4908

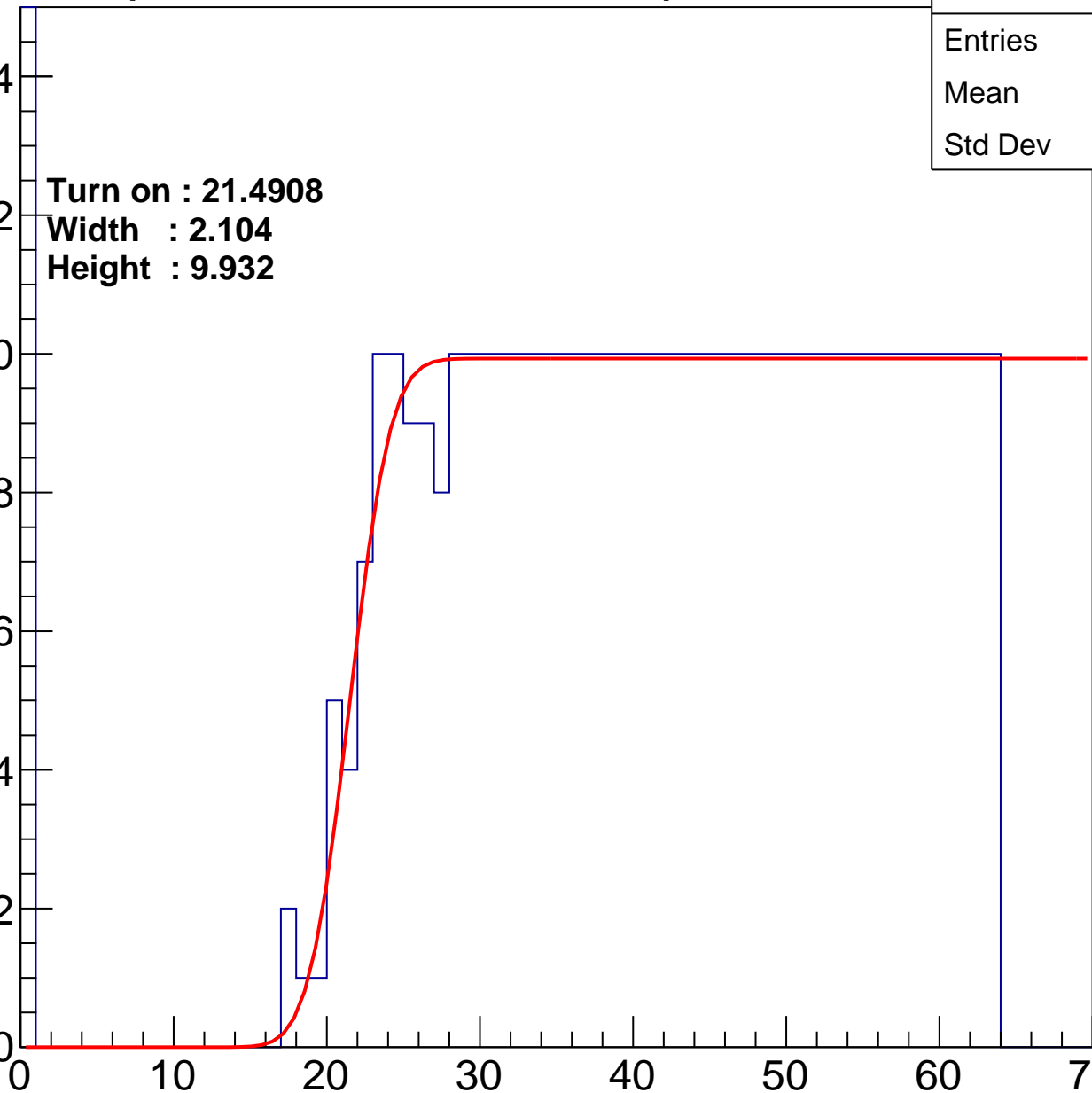
Width : 2.104

Height : 9.932

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch107

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	39.03
Std Dev	17.74

Turn on : 25.7938

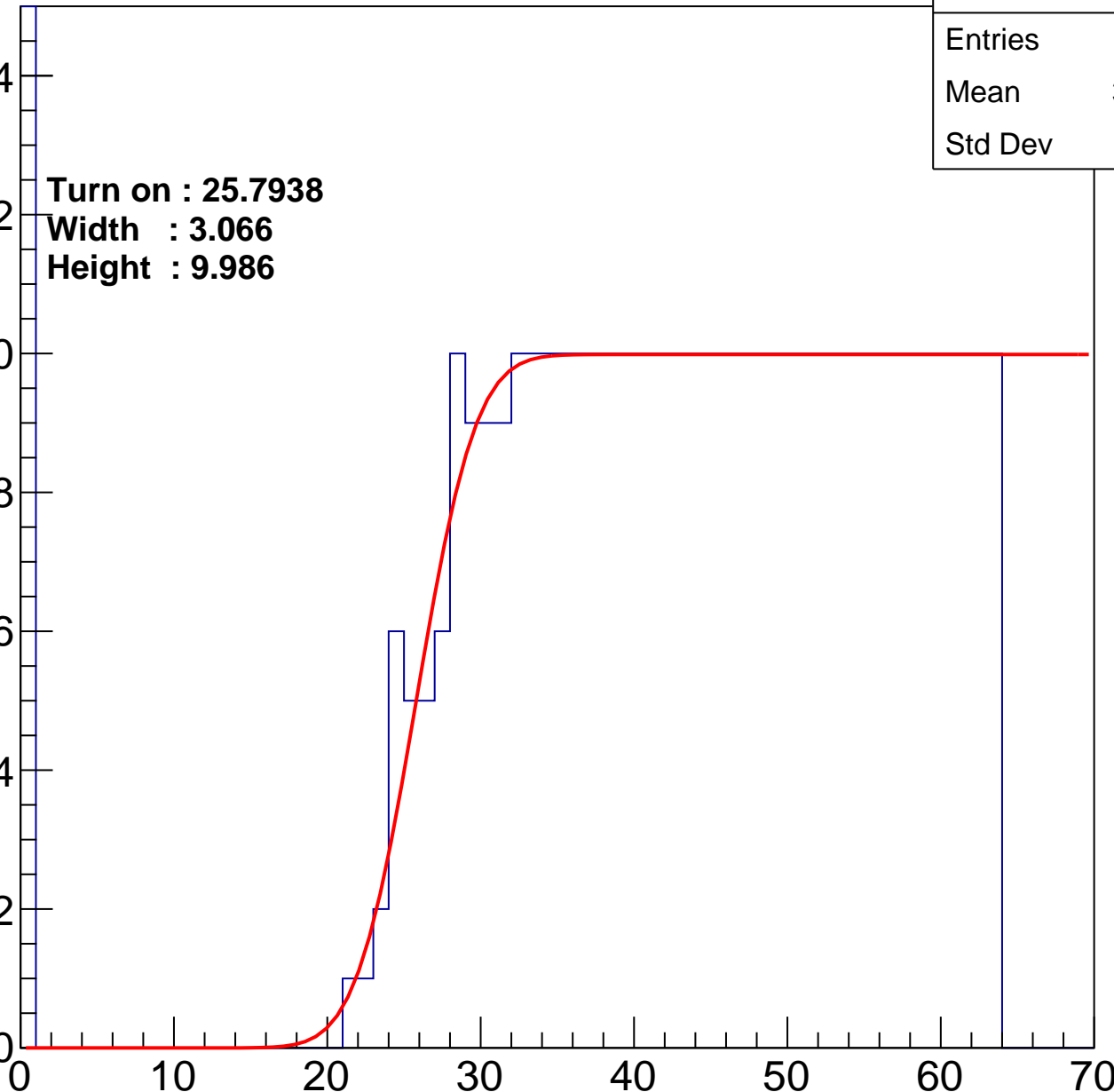
Width : 3.066

Height : 9.986

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch108

calib_packv5_041523_1651.root, FC#0, port C2

Entries	460
Mean	38.15
Std Dev	17.66

Turn on : 23.4957

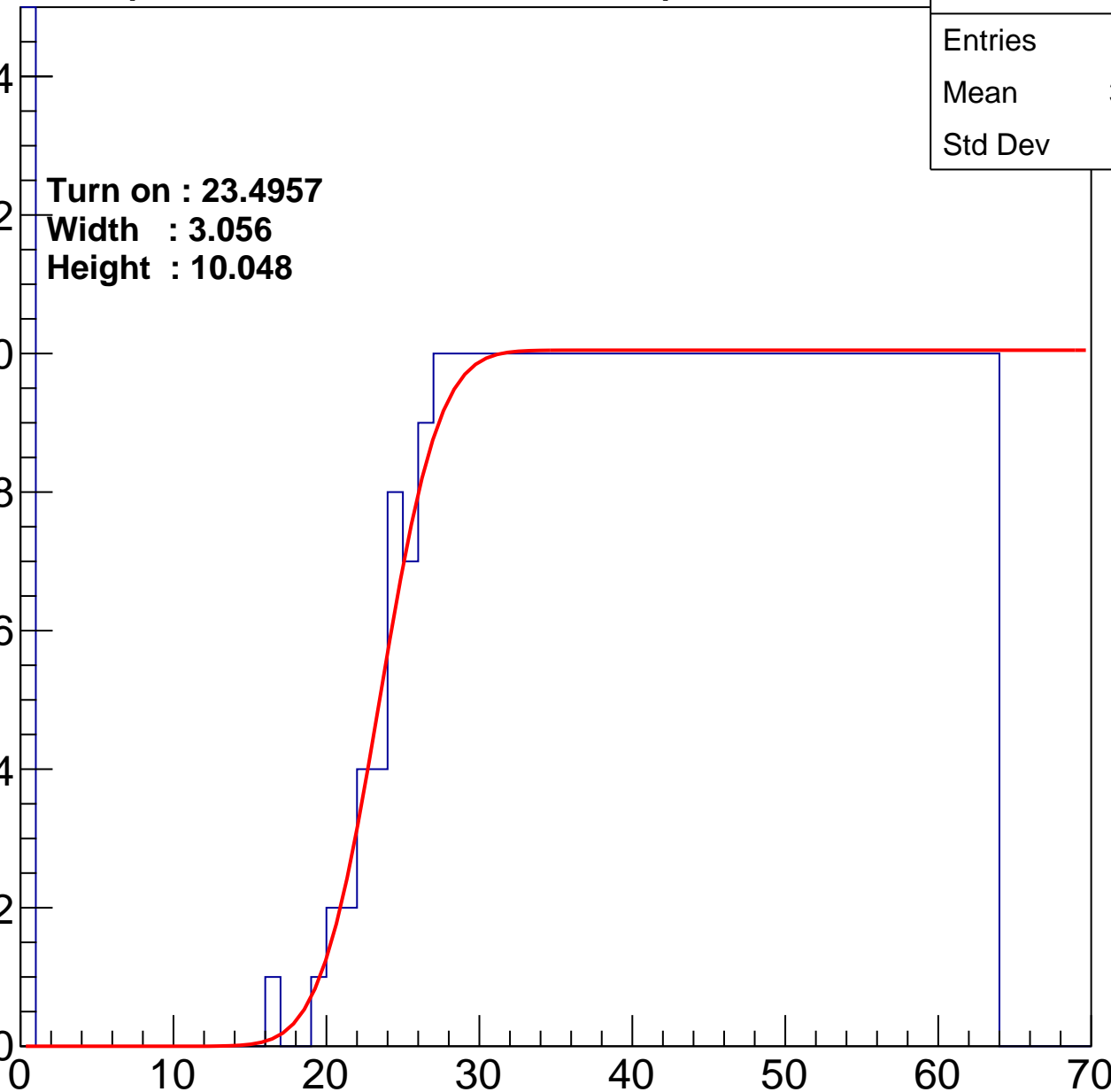
Width : 3.056

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch109

calib_packv5_041523_1651.root, FC#0, port C2

Entries	427
Mean	39.96
Std Dev	16.7

Turn on : 25.4870

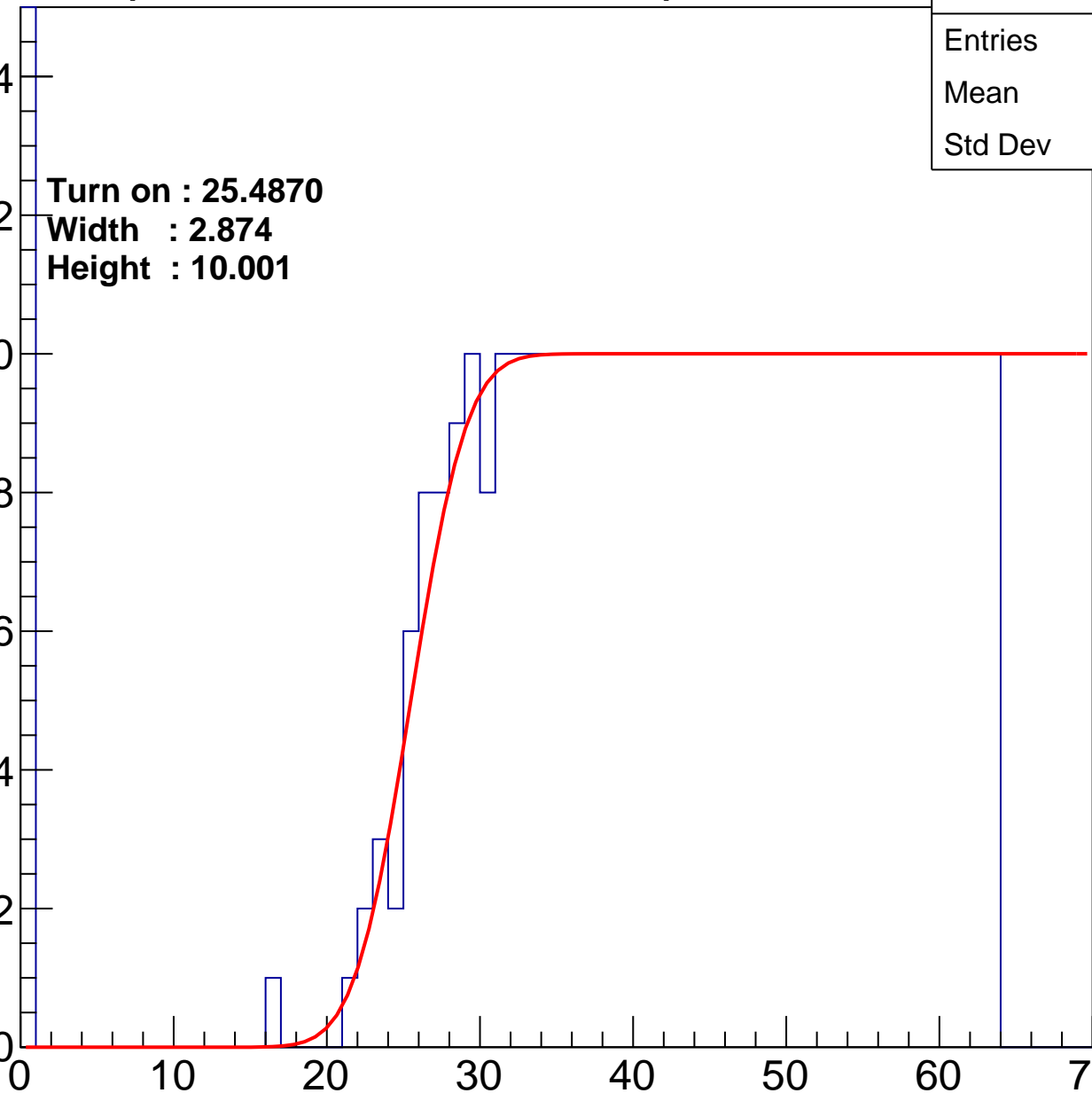
Width : 2.874

Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch110

calib_packv5_041523_1651.root, FC#0, port C2

Entries	470
Mean	37.49
Std Dev	18.07

Turn on : 23.2392

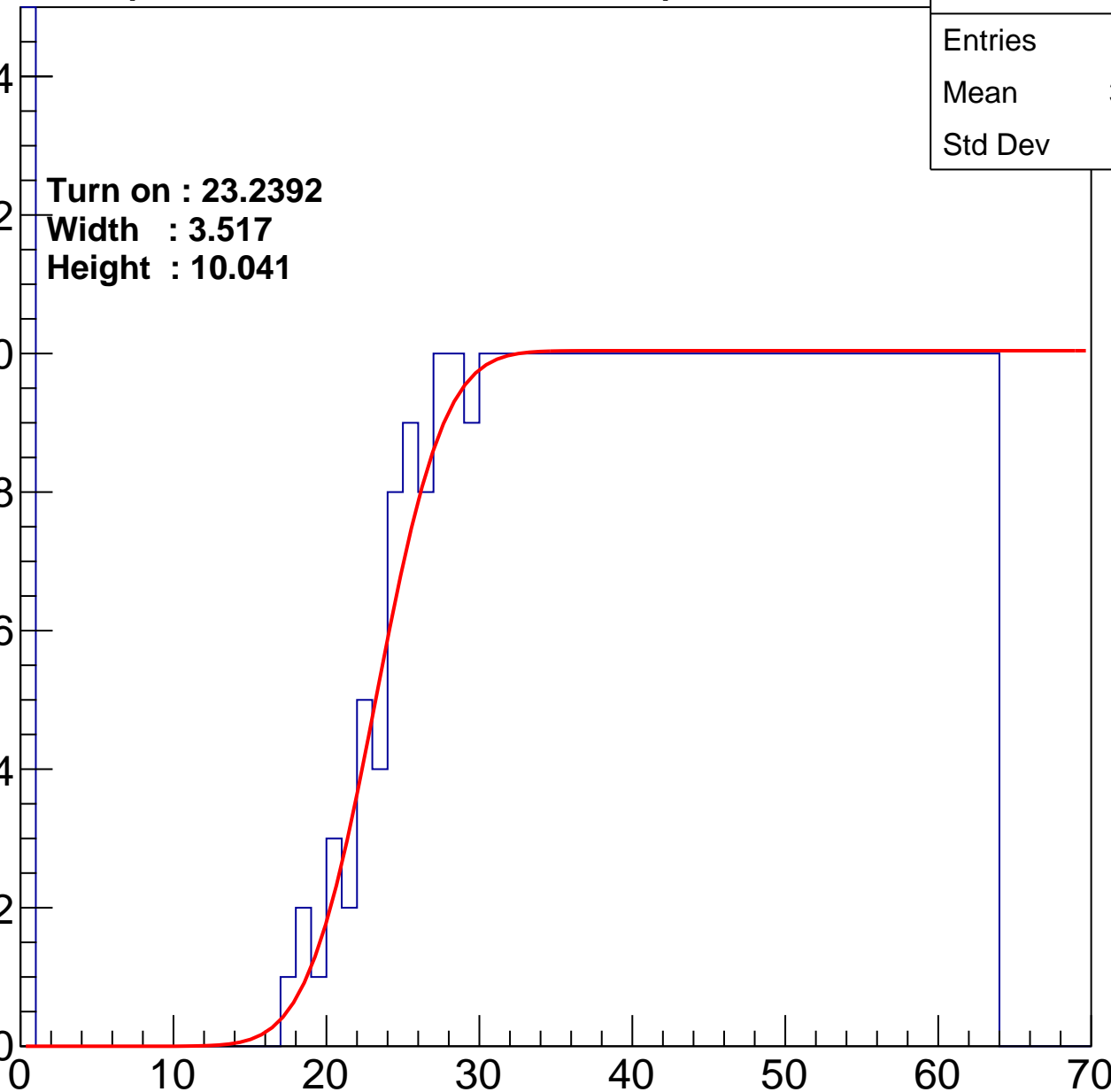
Width : 3.517

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch111

calib_packv5_041523_1651.root, FC#0, port C2

Entries	415
Mean	40.15
Std Dev	17.13

Turn on : 26.7819

Width : 2.983

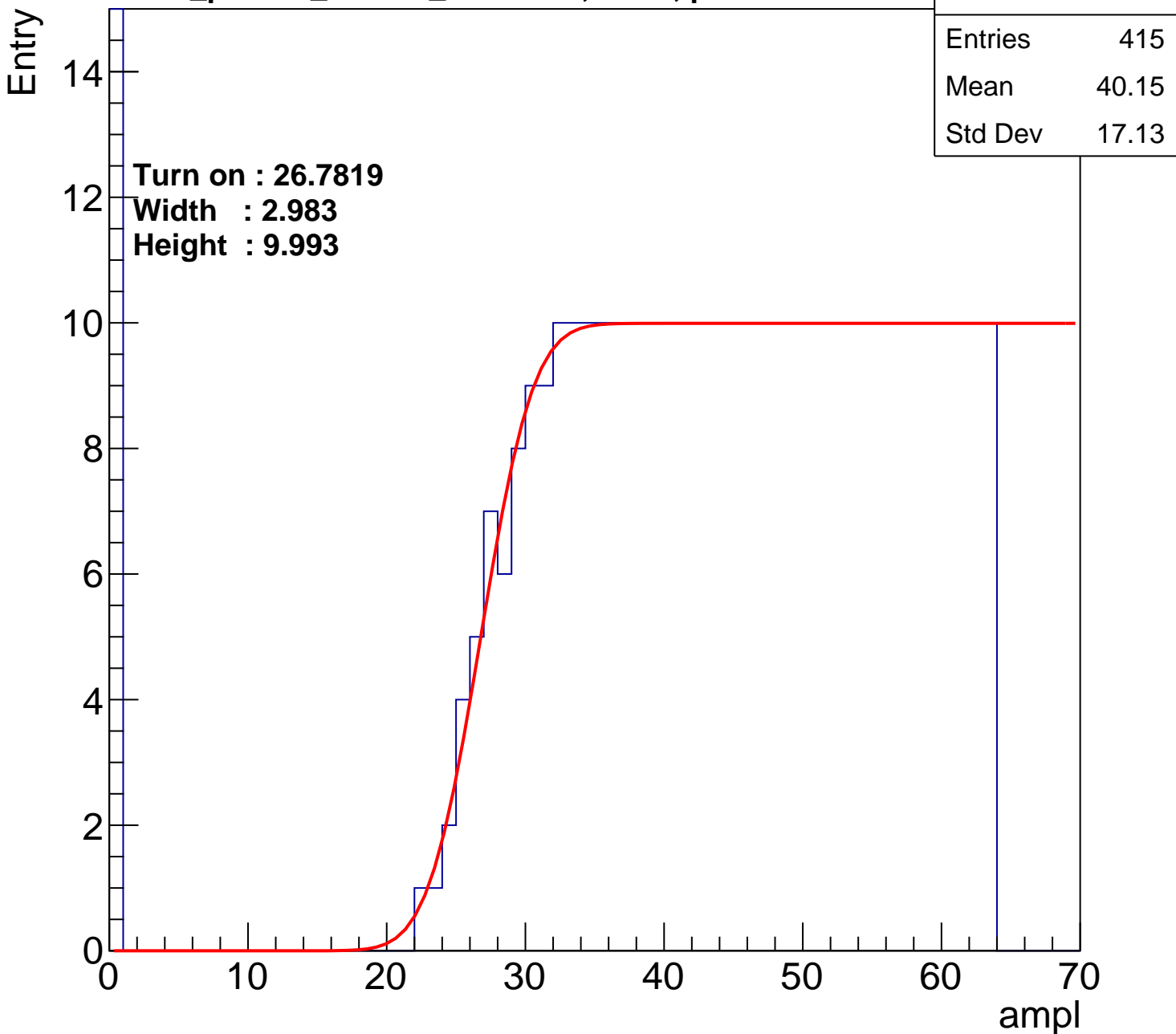
Height : 9.993

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U21-ch112

calib_packv5_041523_1651.root, FC#0, port C2

Entries	452
Mean	38.54
Std Dev	17.74

Turn on : 24.8974

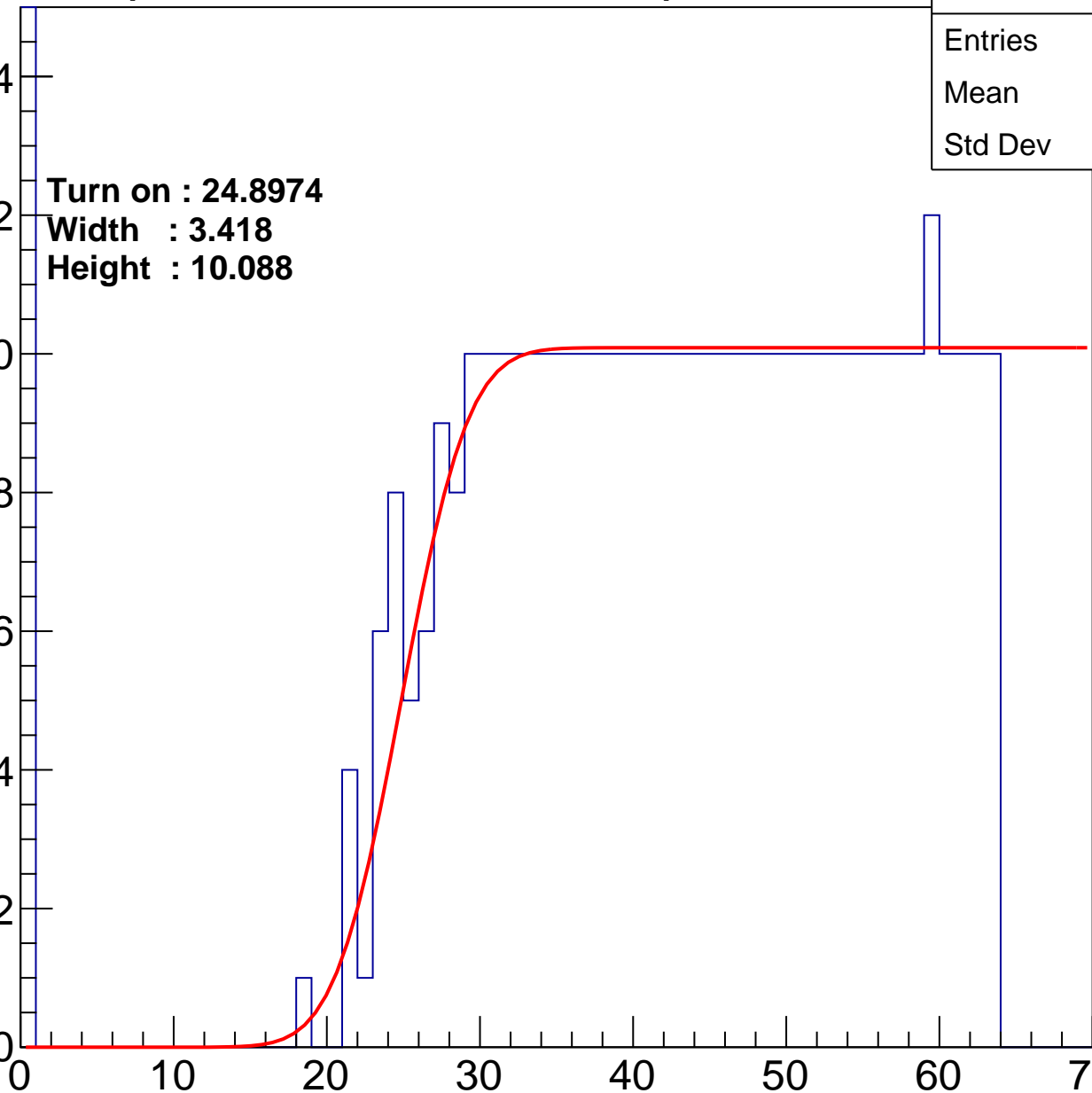
Width : 3.418

Height : 10.088

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch113

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.76
Std Dev	16.93

Turn on : 25.9420

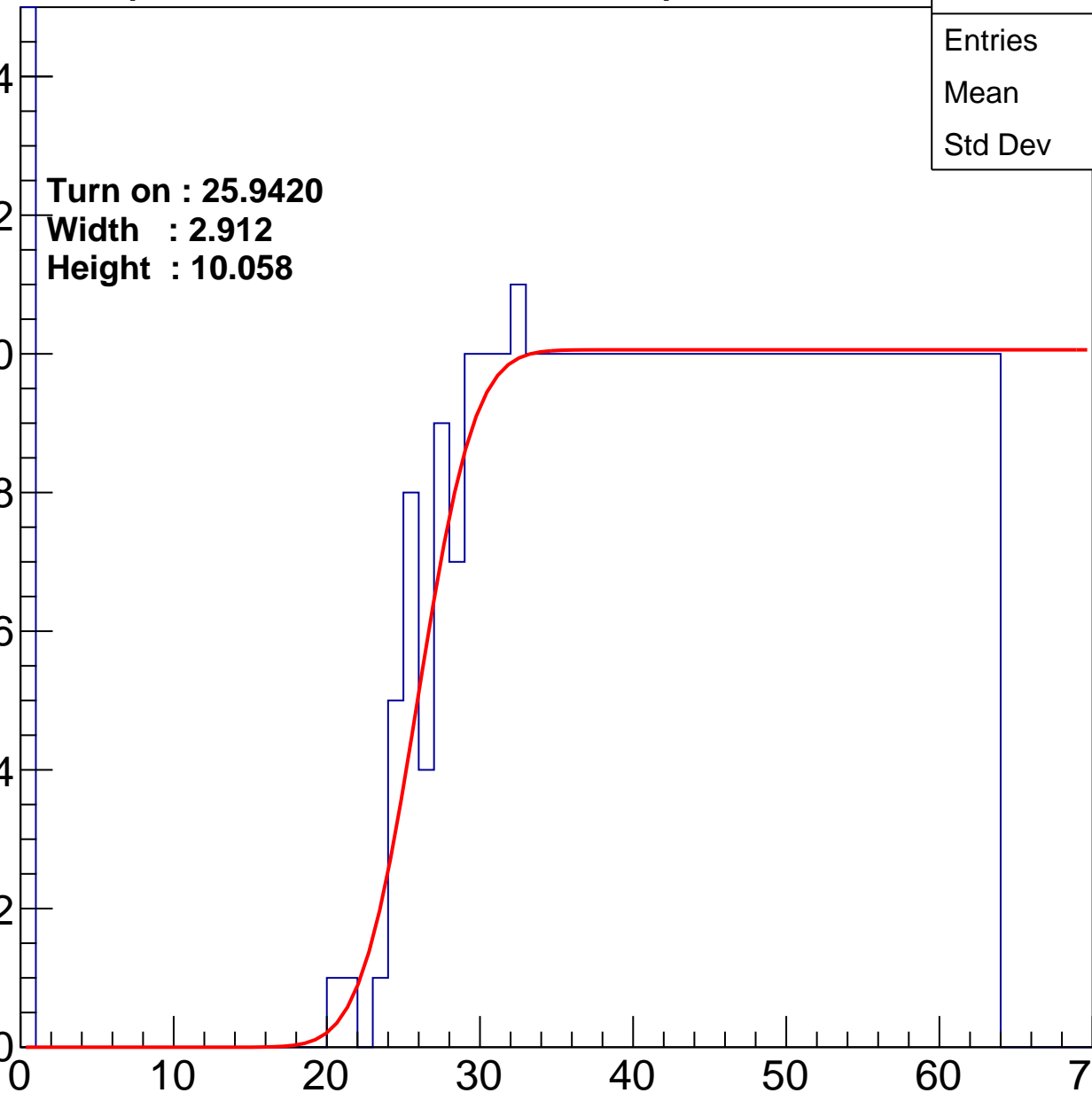
Width : 2.912

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch114

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	38.96
Std Dev	17.42

Turn on : 24.6793

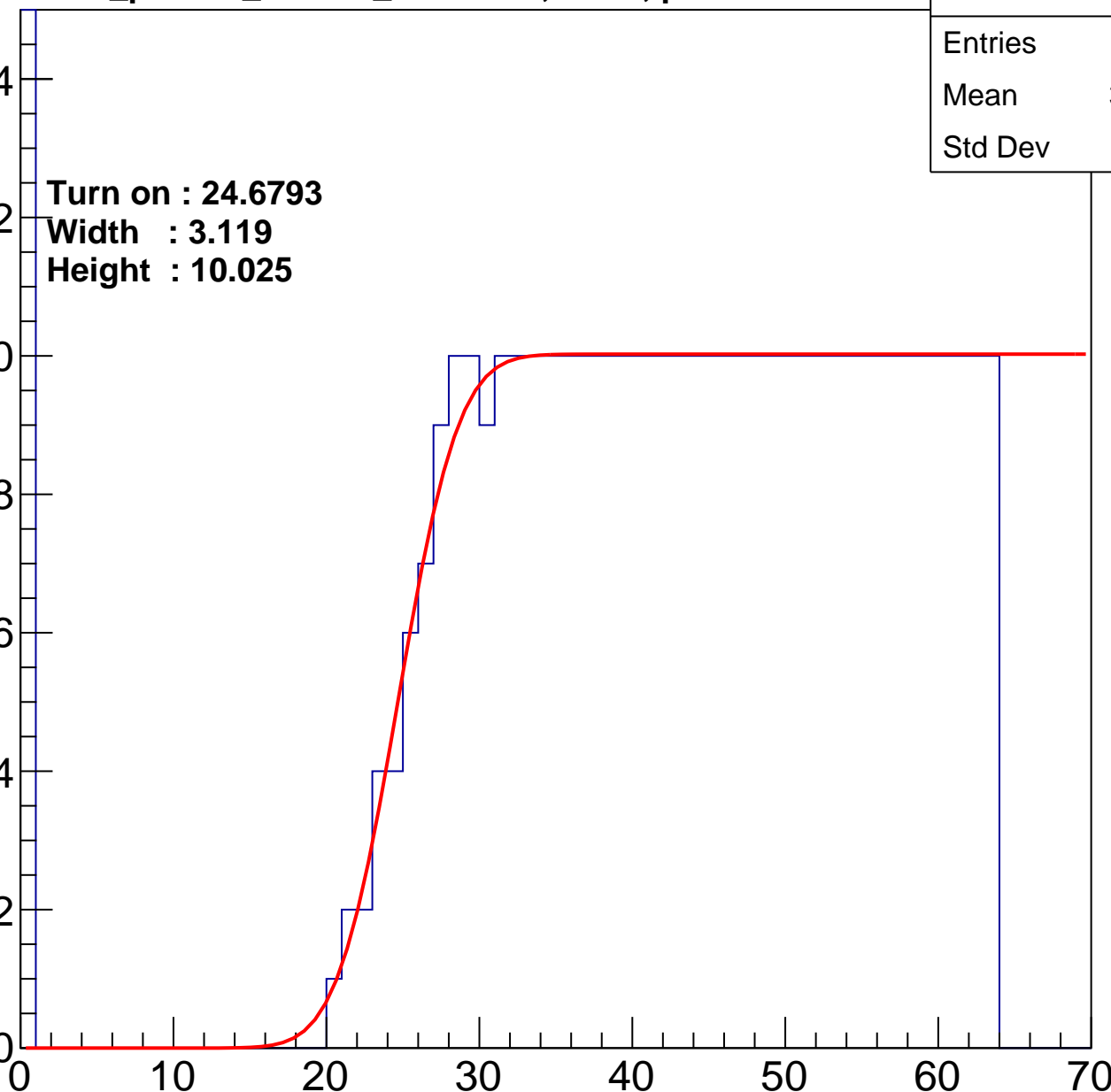
Width : 3.119

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch115

calib_packv5_041523_1651.root, FC#0, port C2

Entries	453
Mean	38.12
Std Dev	18.04

Turn on : 24.6983

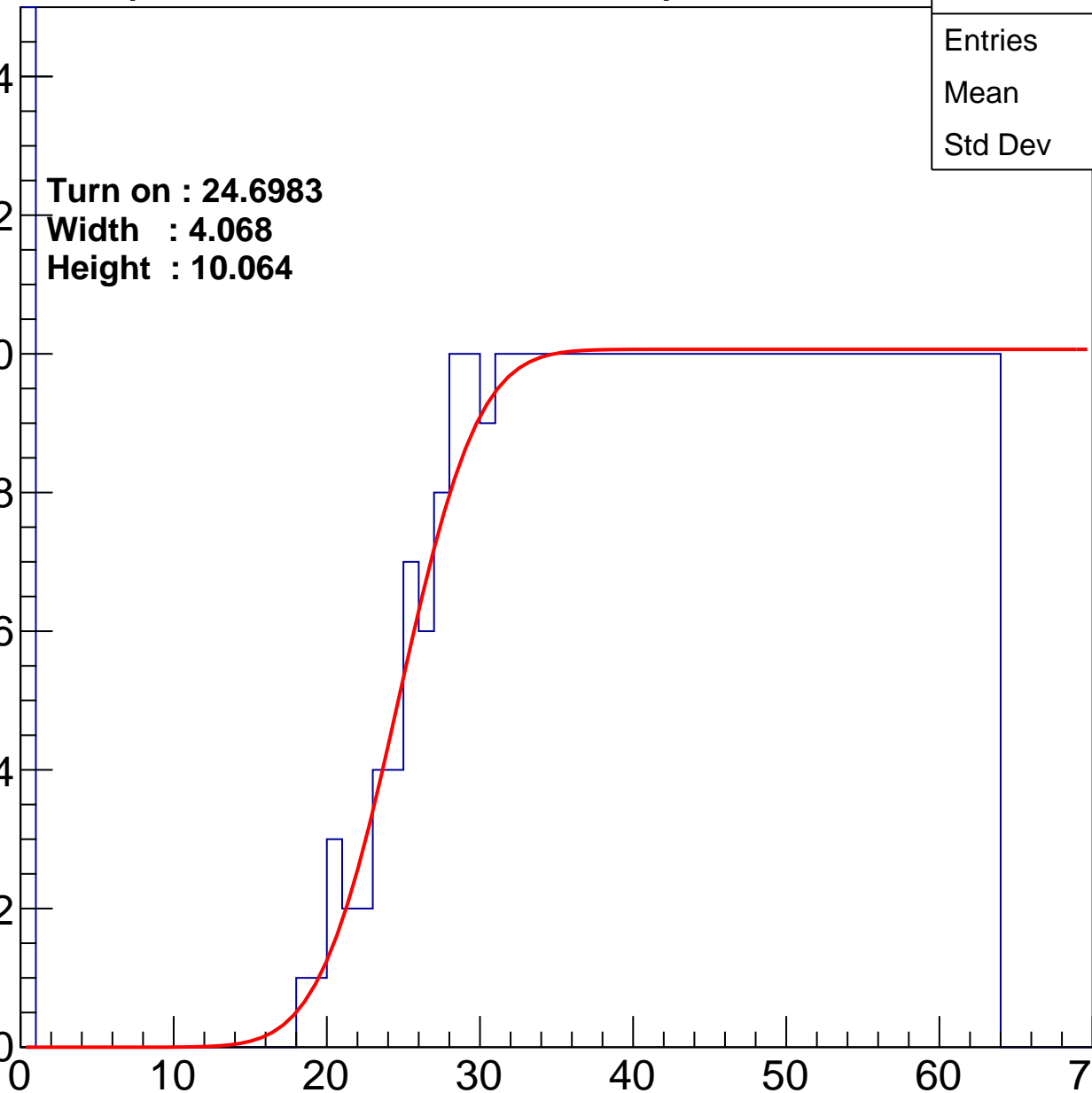
Width : 4.068

Height : 10.064

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch116

calib_packv5_041523_1651.root, FC#0, port C2

Entries	464
Mean	38.36
Std Dev	17.11

Turn on : 22.3892

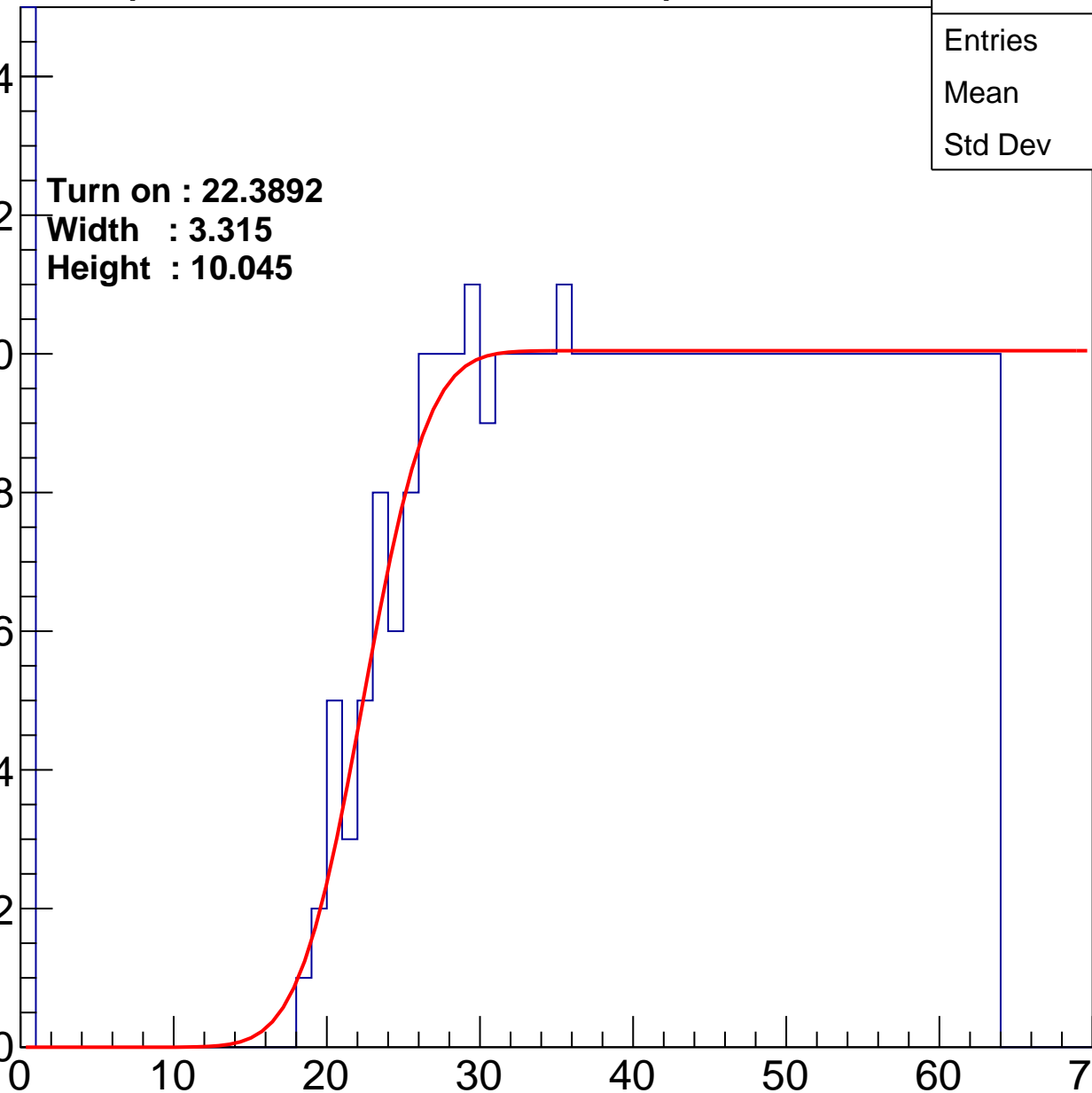
Width : 3.315

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch117

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	39.23
Std Dev	17.6

Turn on : 25.8654

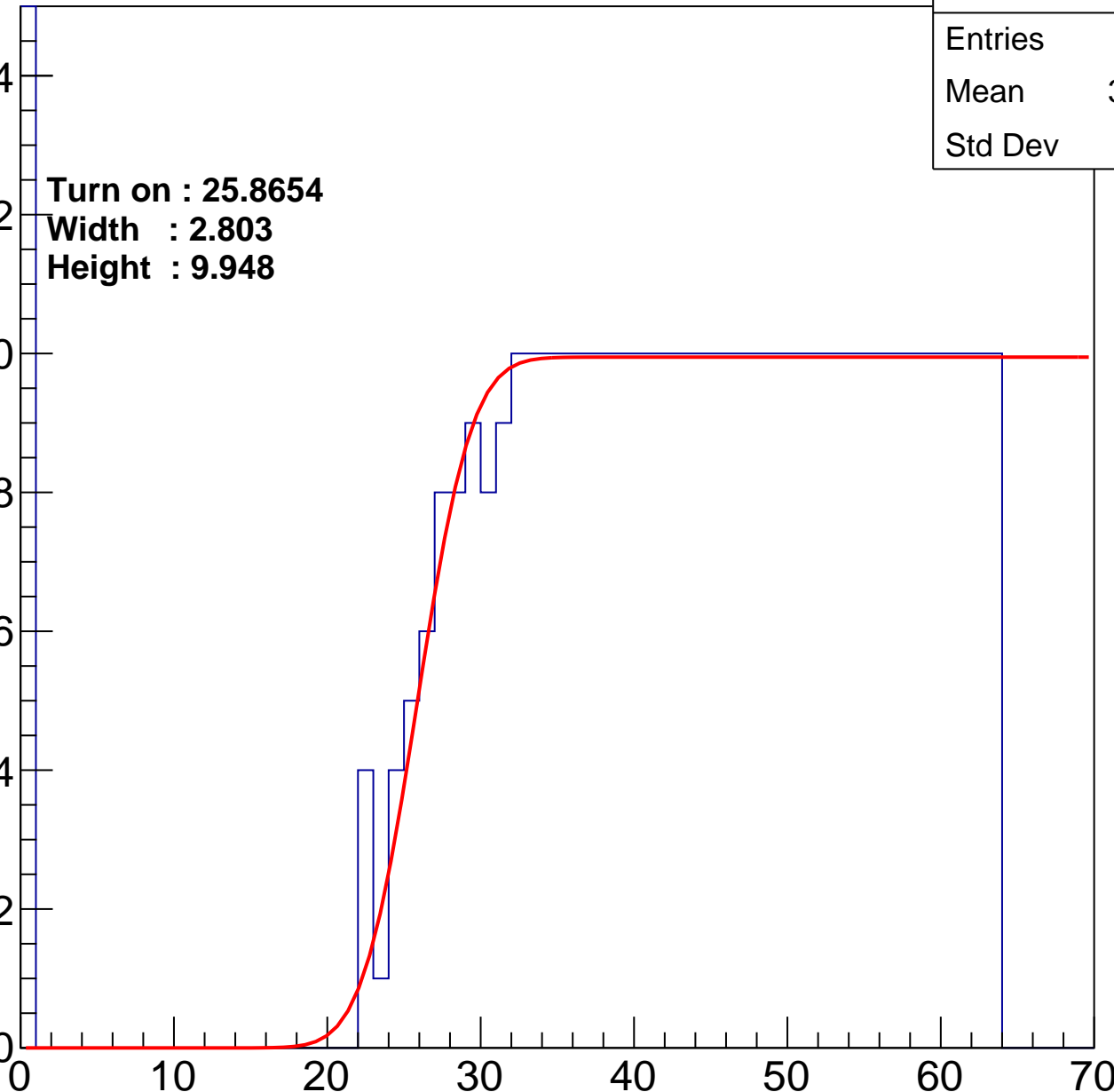
Width : 2.803

Height : 9.948

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch118

calib_packv5_041523_1651.root, FC#0, port C2

Entries	493
Mean	36.16
Std Dev	18.78

Turn on : 22.6155

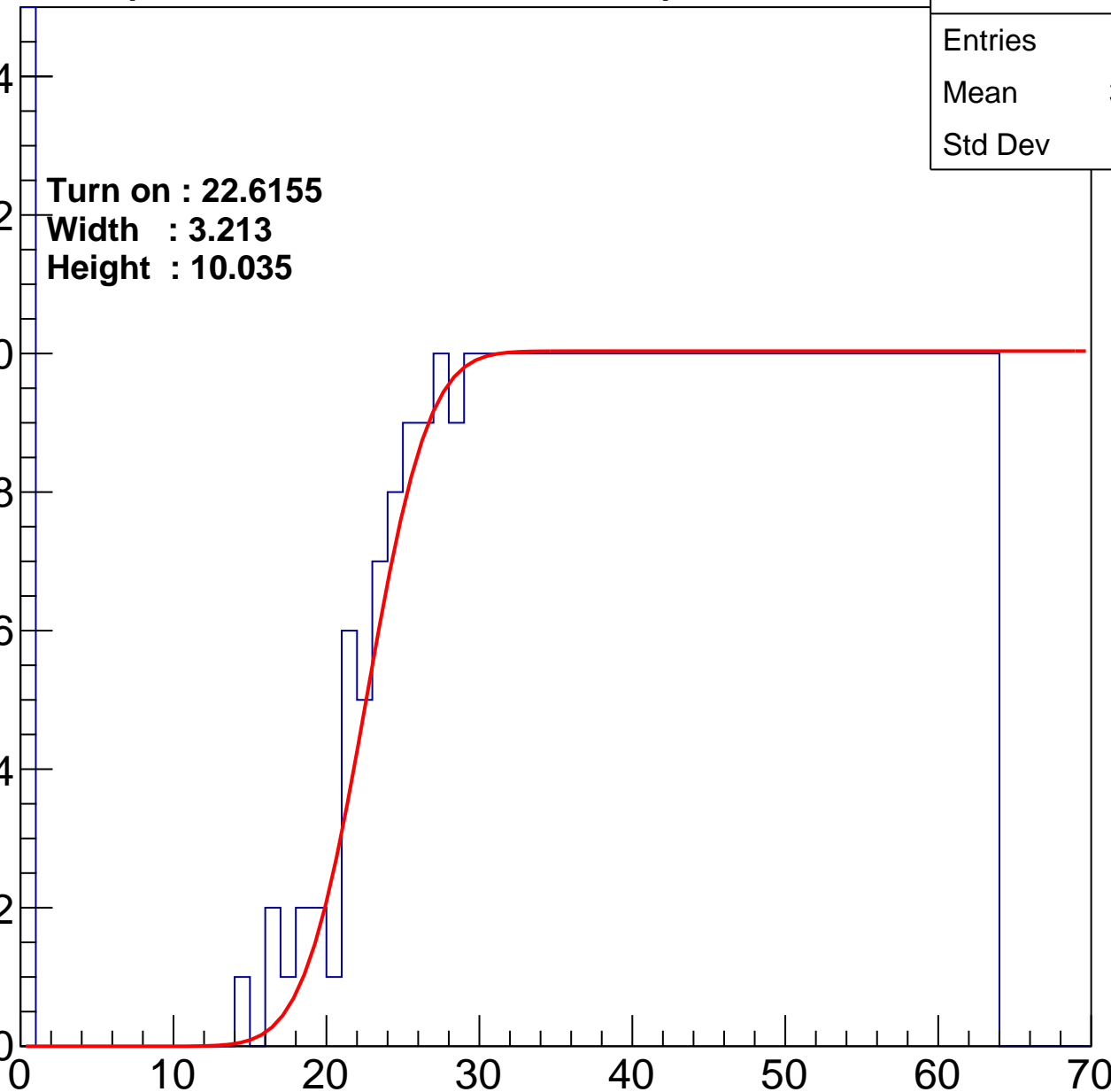
Width : 3.213

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch119

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	37.87
Std Dev	18.96

Turn on : 26.5595

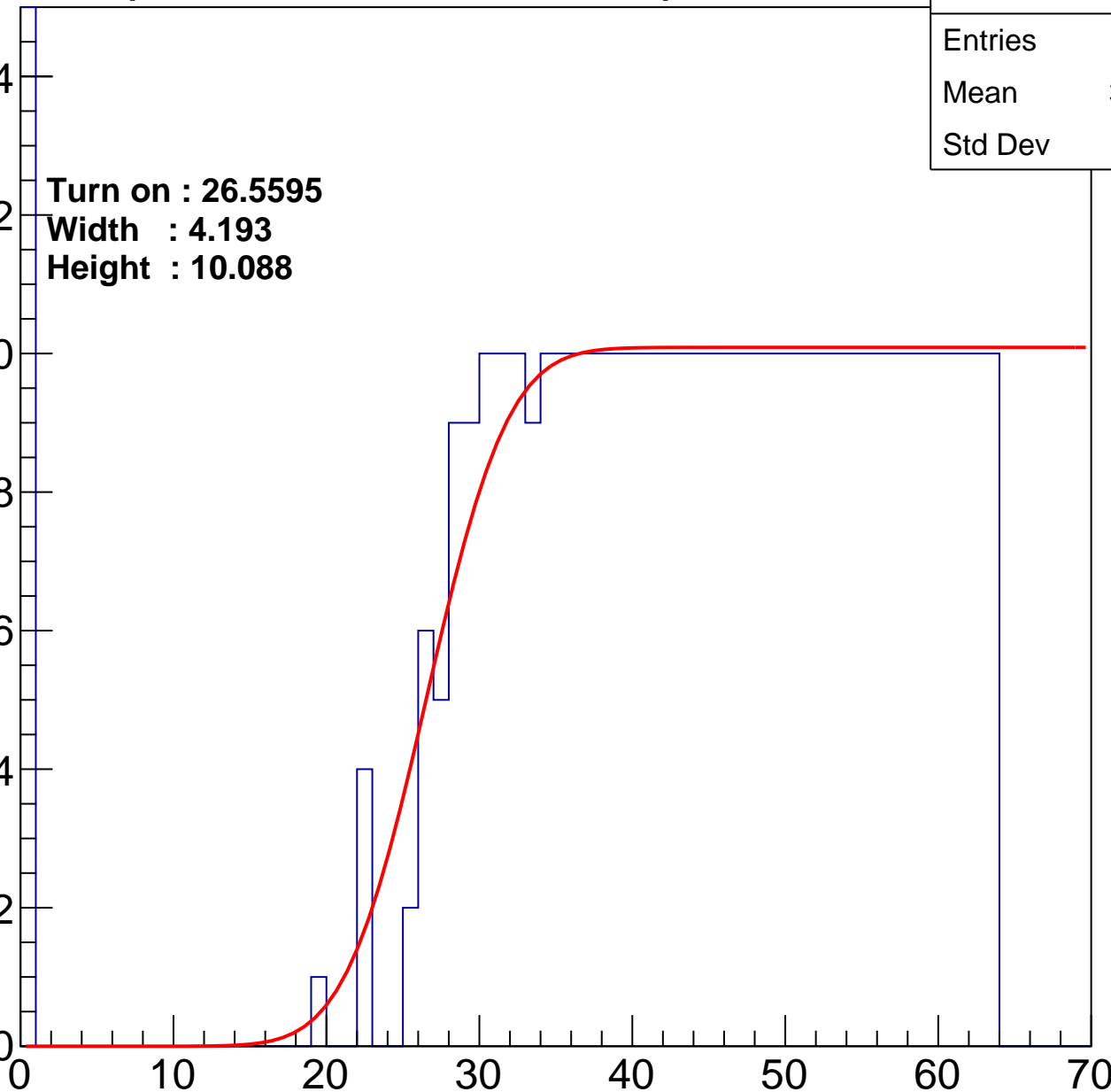
Width : 4.193

Height : 10.088

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch120

calib_packv5_041523_1651.root, FC#0, port C2

Entries	485
Mean	36.91
Std Dev	18.08

Turn on : 21.1536

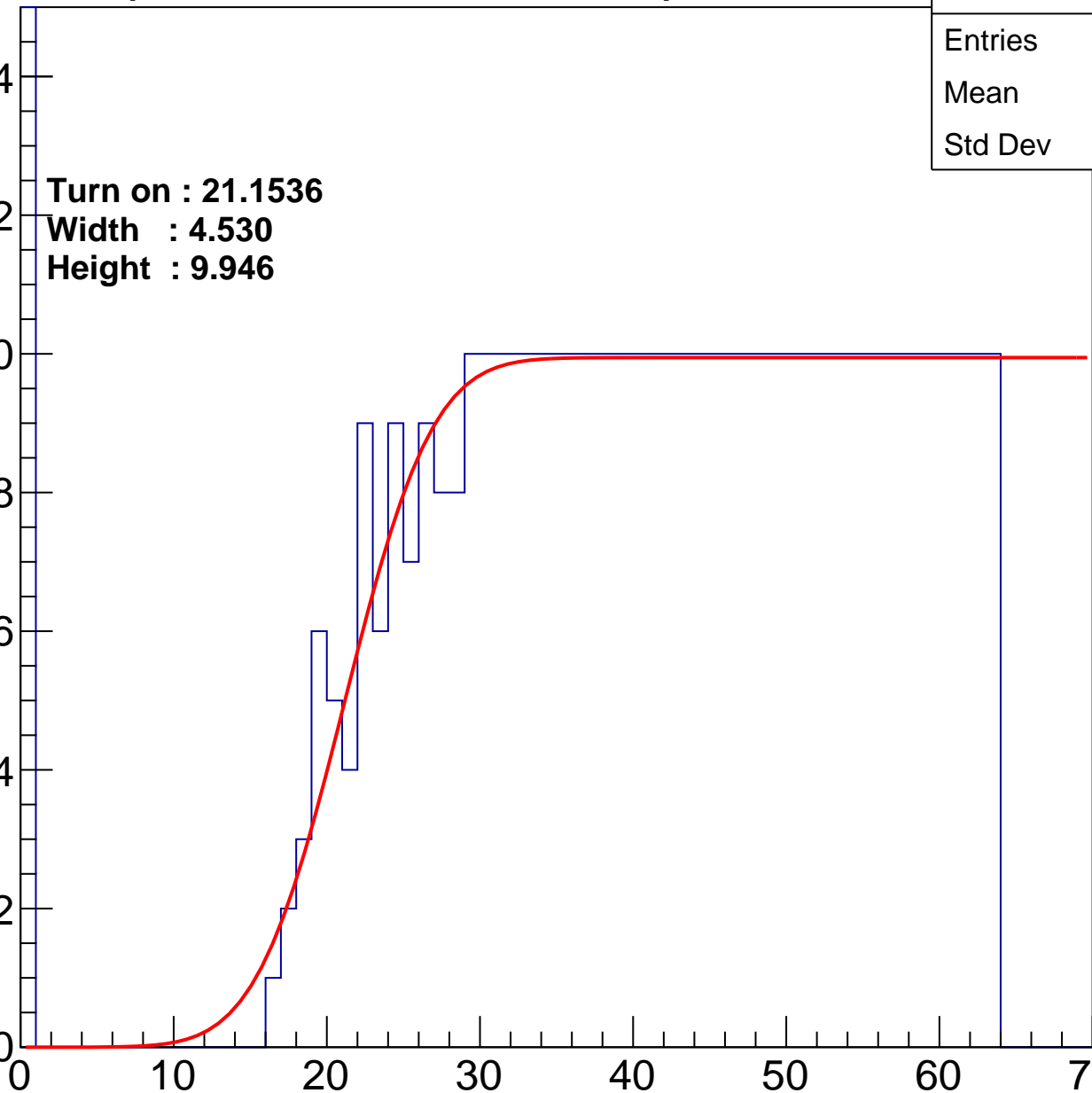
Width : 4.530

Height : 9.946

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch121

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	38.52
Std Dev	18.1

Turn on : 25.2939

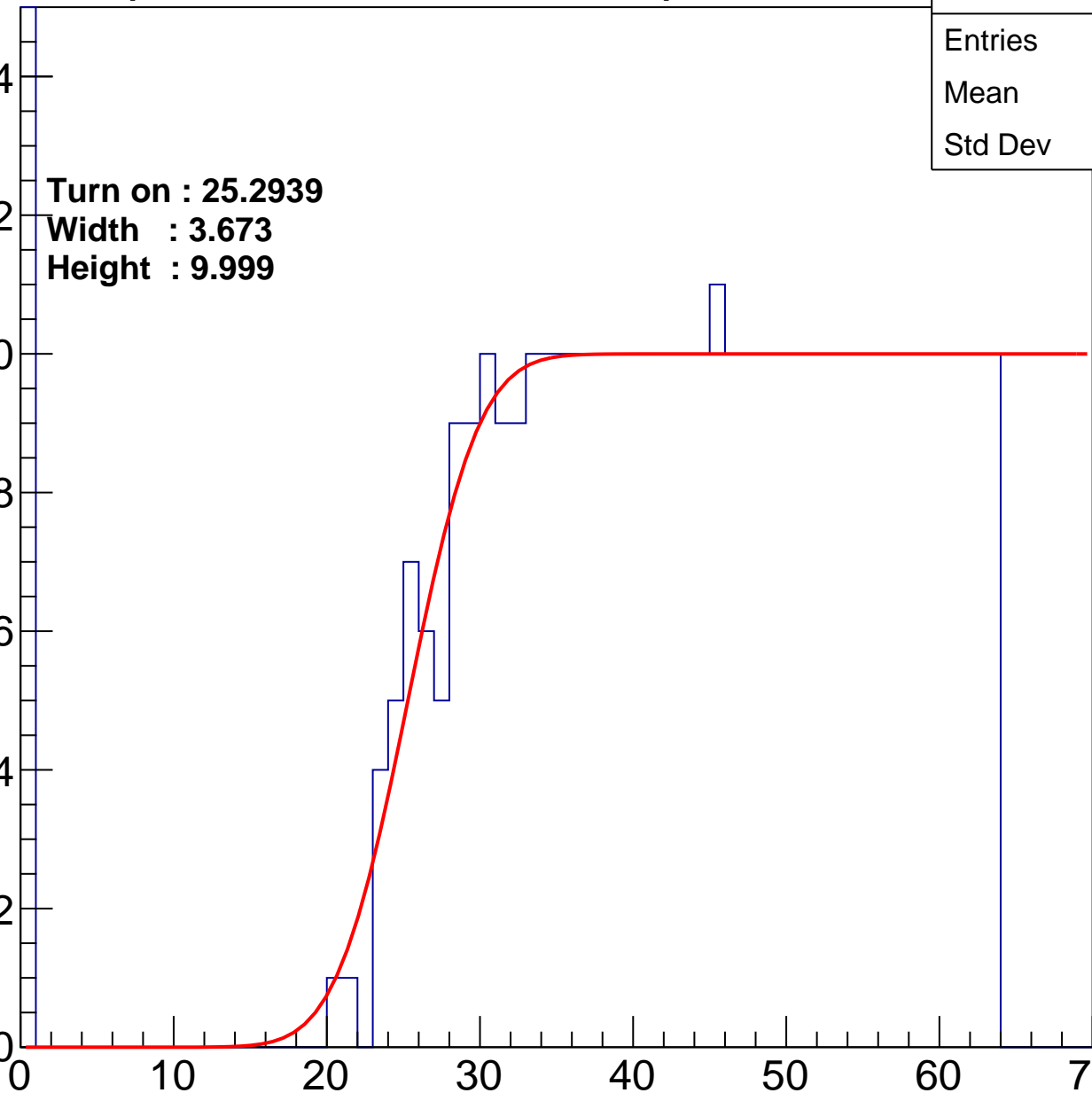
Width : 3.673

Height : 9.999

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch122

calib_packv5_041523_1651.root, FC#0, port C2

Entries	448
Mean	38.35
Std Dev	18.04

Turn on : 24.9912

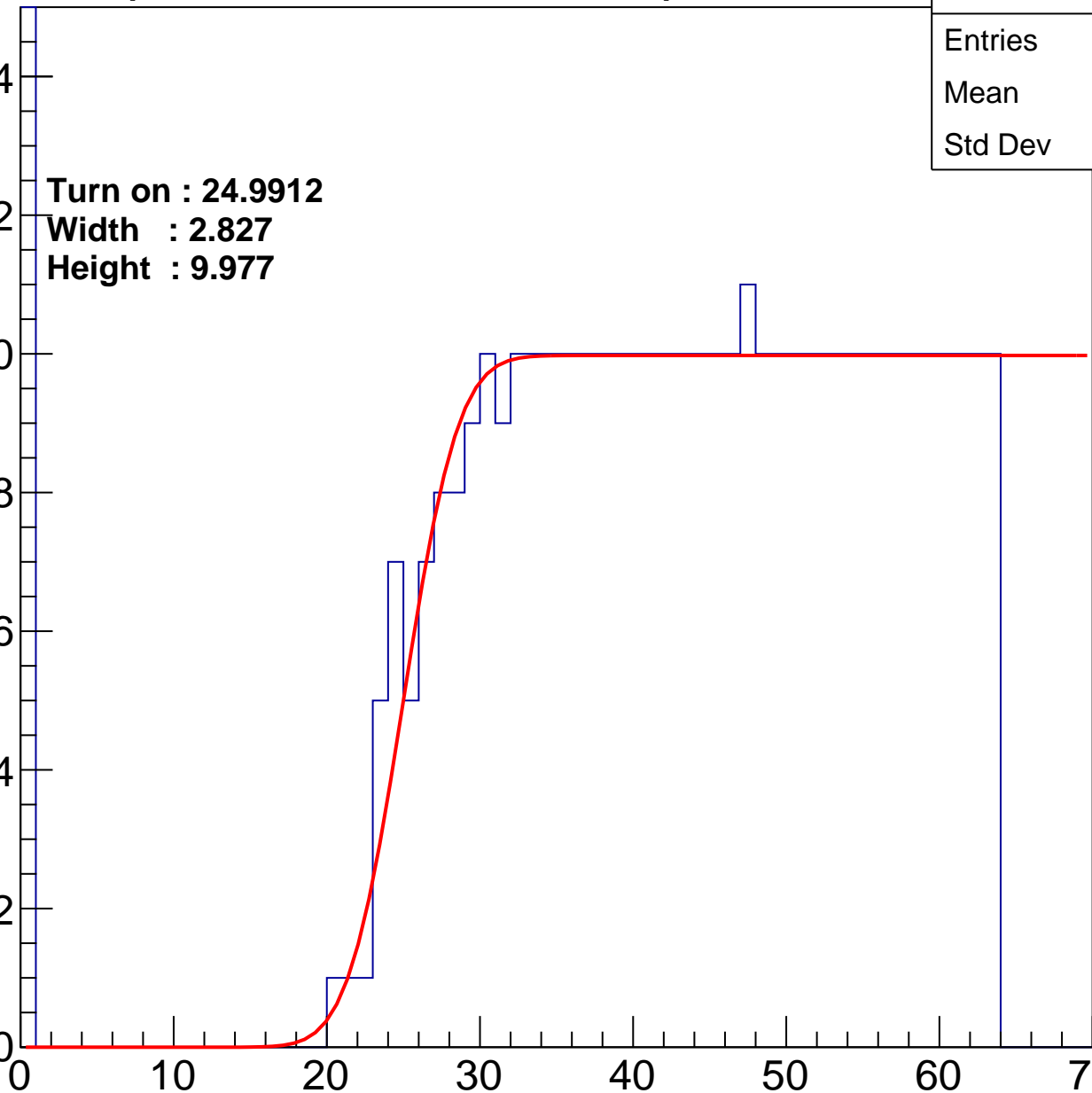
Width : 2.827

Height : 9.977

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch123

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	39.07
Std Dev	17.67

Turn on : 25.9520

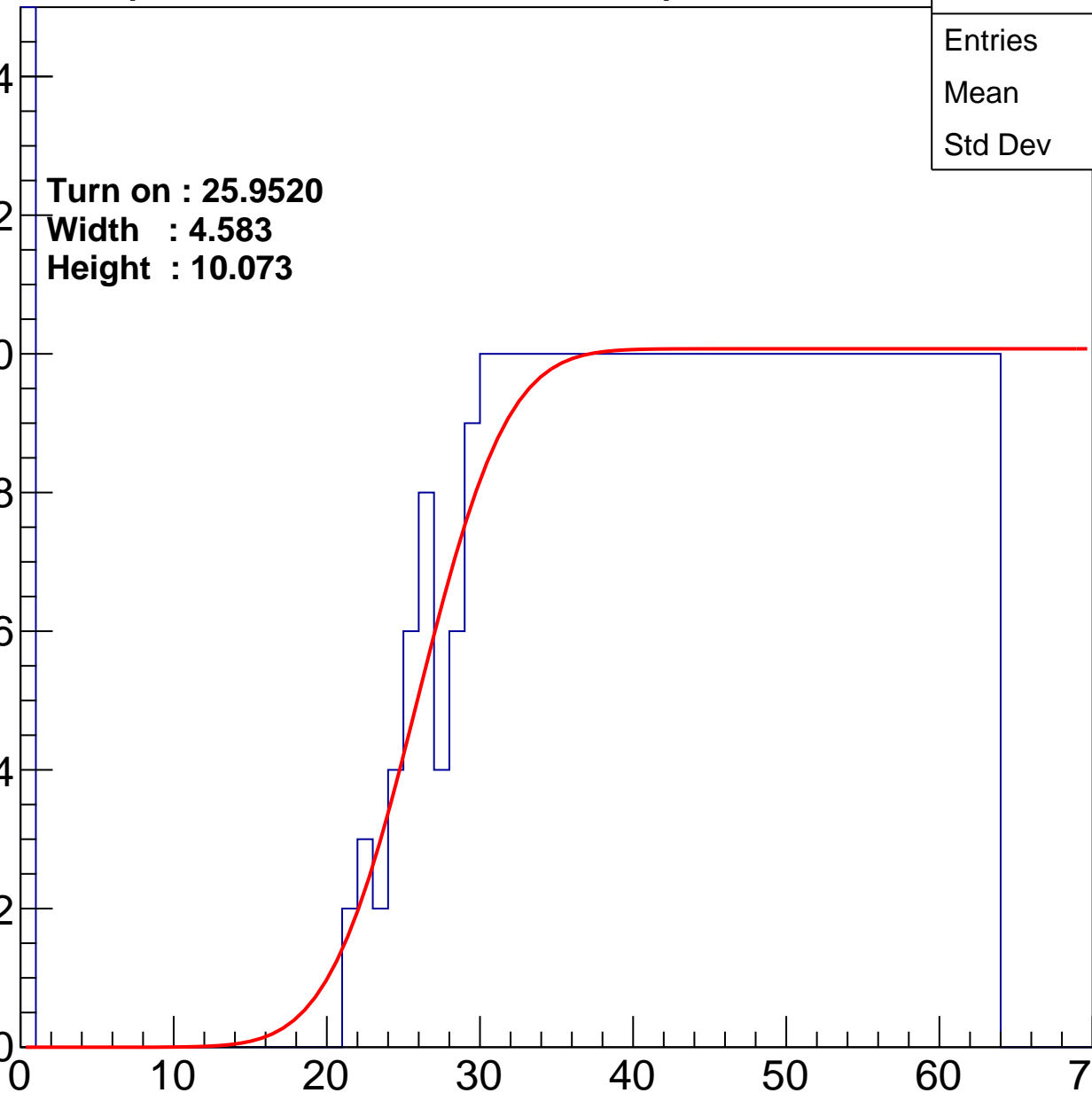
Width : 4.583

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch124

calib_packv5_041523_1651.root, FC#0, port C2

Entries	451
Mean	38.61
Std Dev	17.39

Turn on : 23.5704

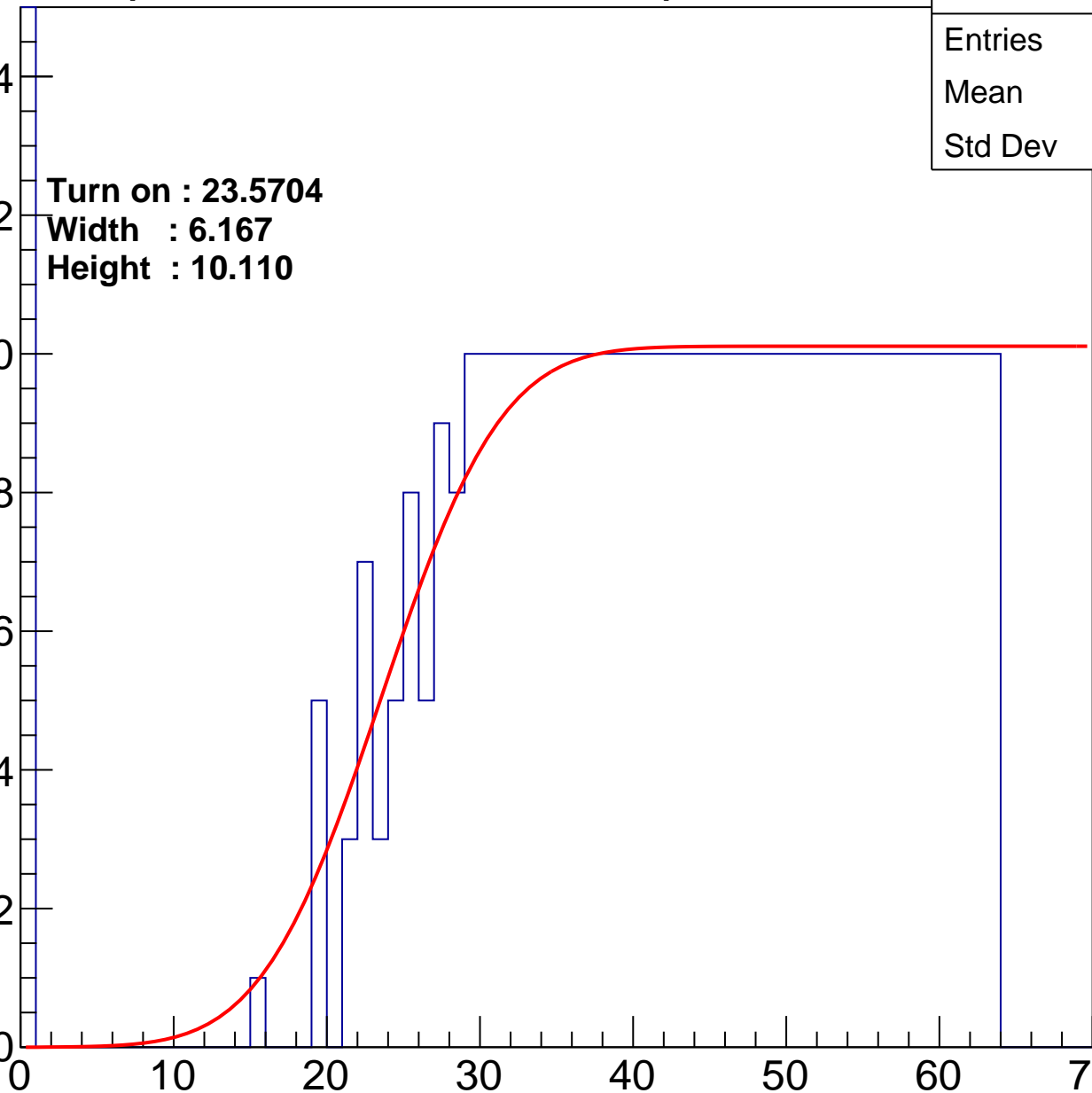
Width : 6.167

Height : 10.110

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch125

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	39.22
Std Dev	17.19

Turn on : 25.0517

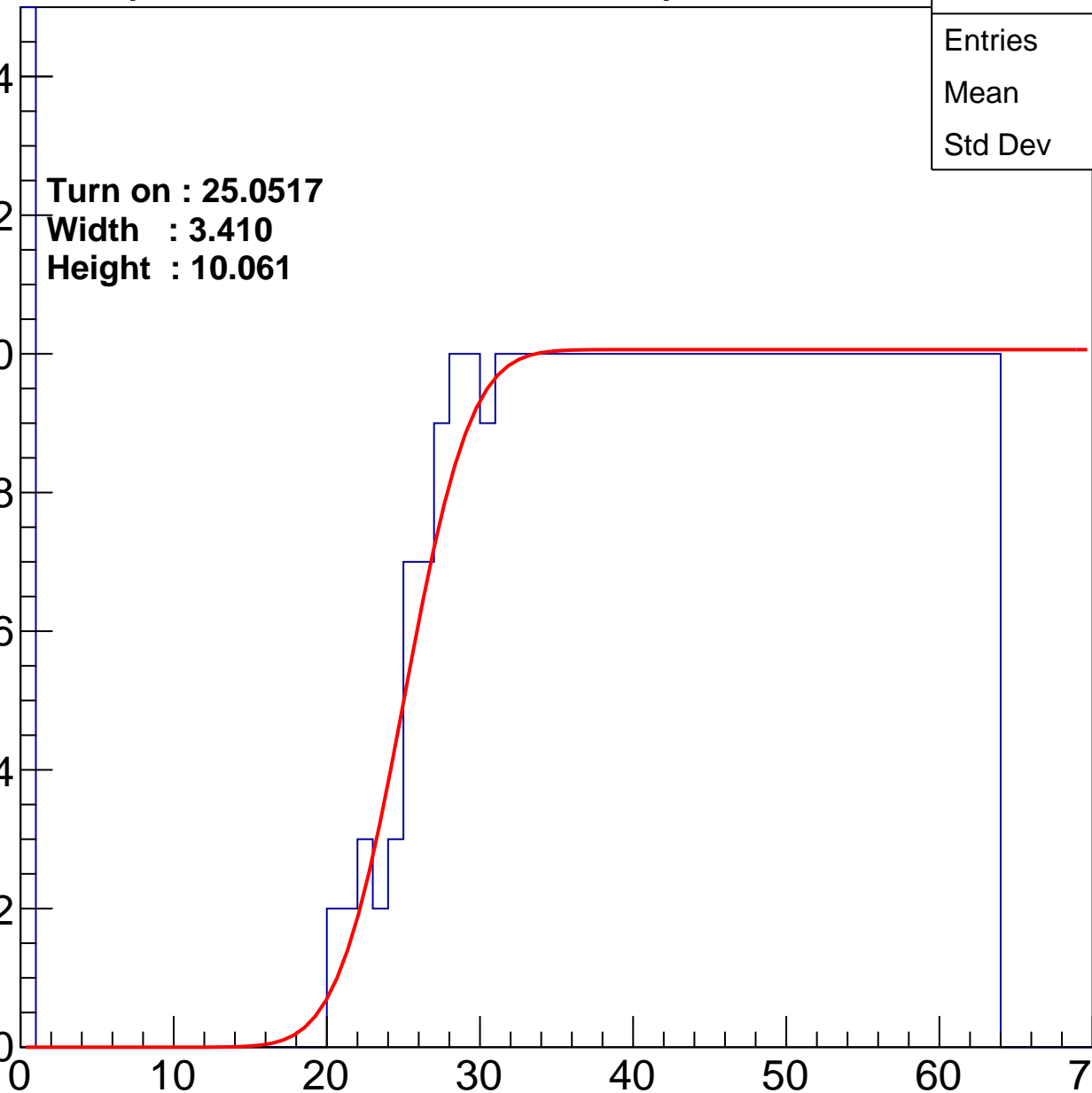
Width : 3.410

Height : 10.061

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch126

calib_packv5_041523_1651.root, FC#0, port C2

Entries	472
Mean	37.82
Std Dev	17.44

Turn on : 22.5457

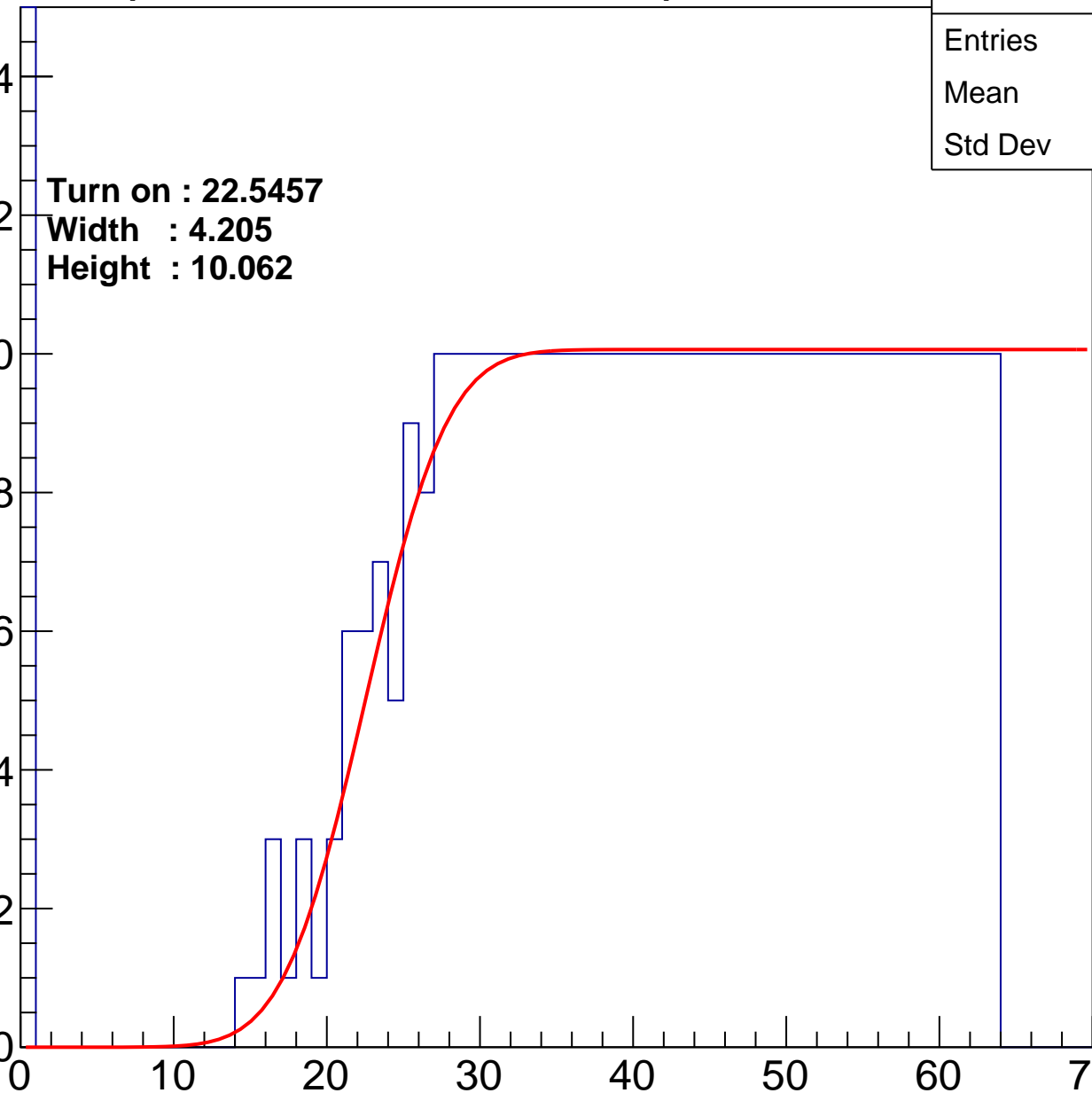
Width : 4.205

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch127

calib_packv5_041523_1651.root, FC#0, port C2

Entries	463
Mean	37.33
Std Dev	18.65

Turn on : 23.9426

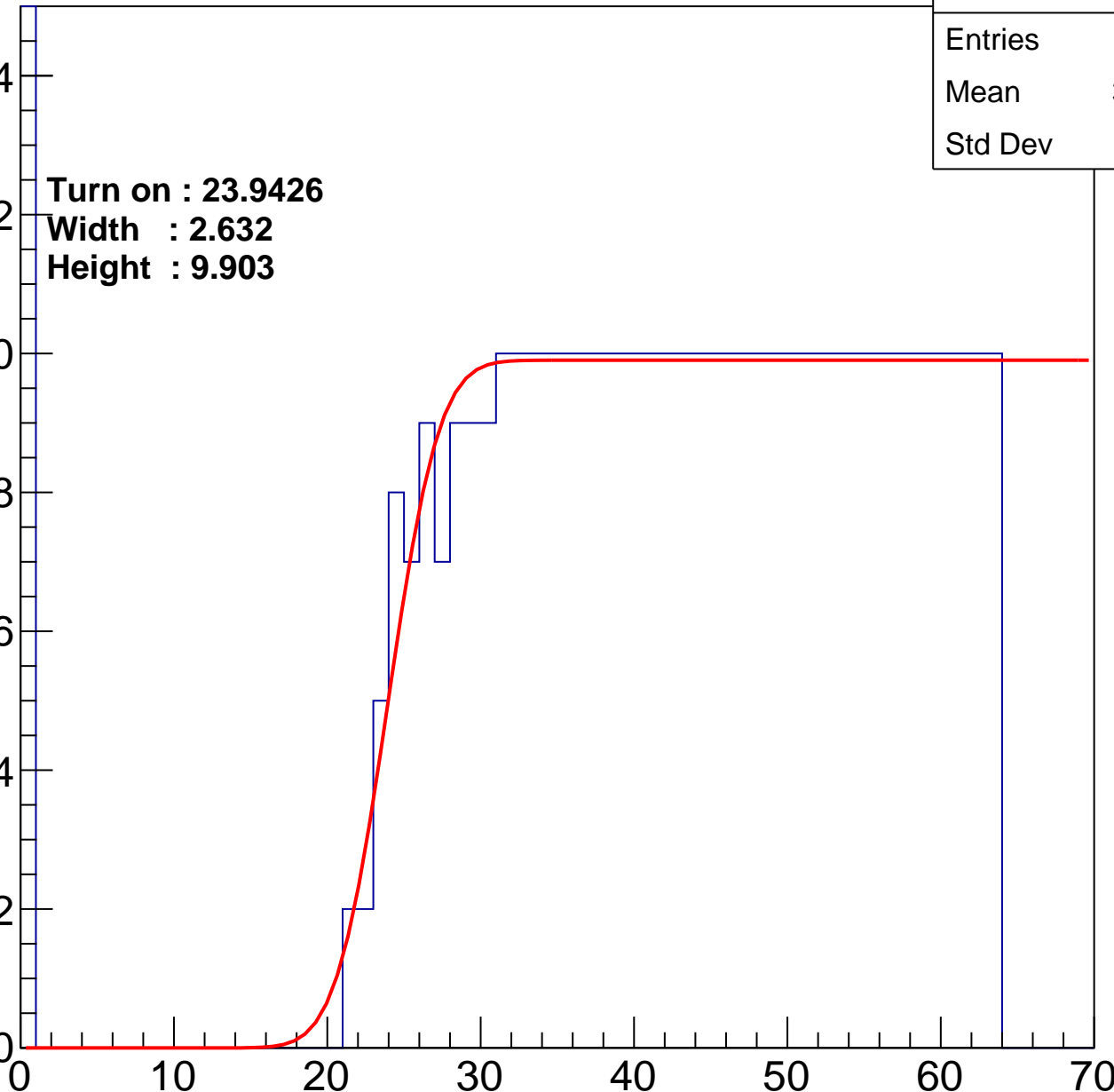
Width : 2.632

Height : 9.903

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U21-ch127

calib_packv5_041523_1651.root, FC#0, port C2

Entries	463
Mean	37.33
Std Dev	18.65

Turn on : 23.9426

Width : 2.632

Height : 9.903

Entry

14
12
10
8
6
4
2
0

ampl

