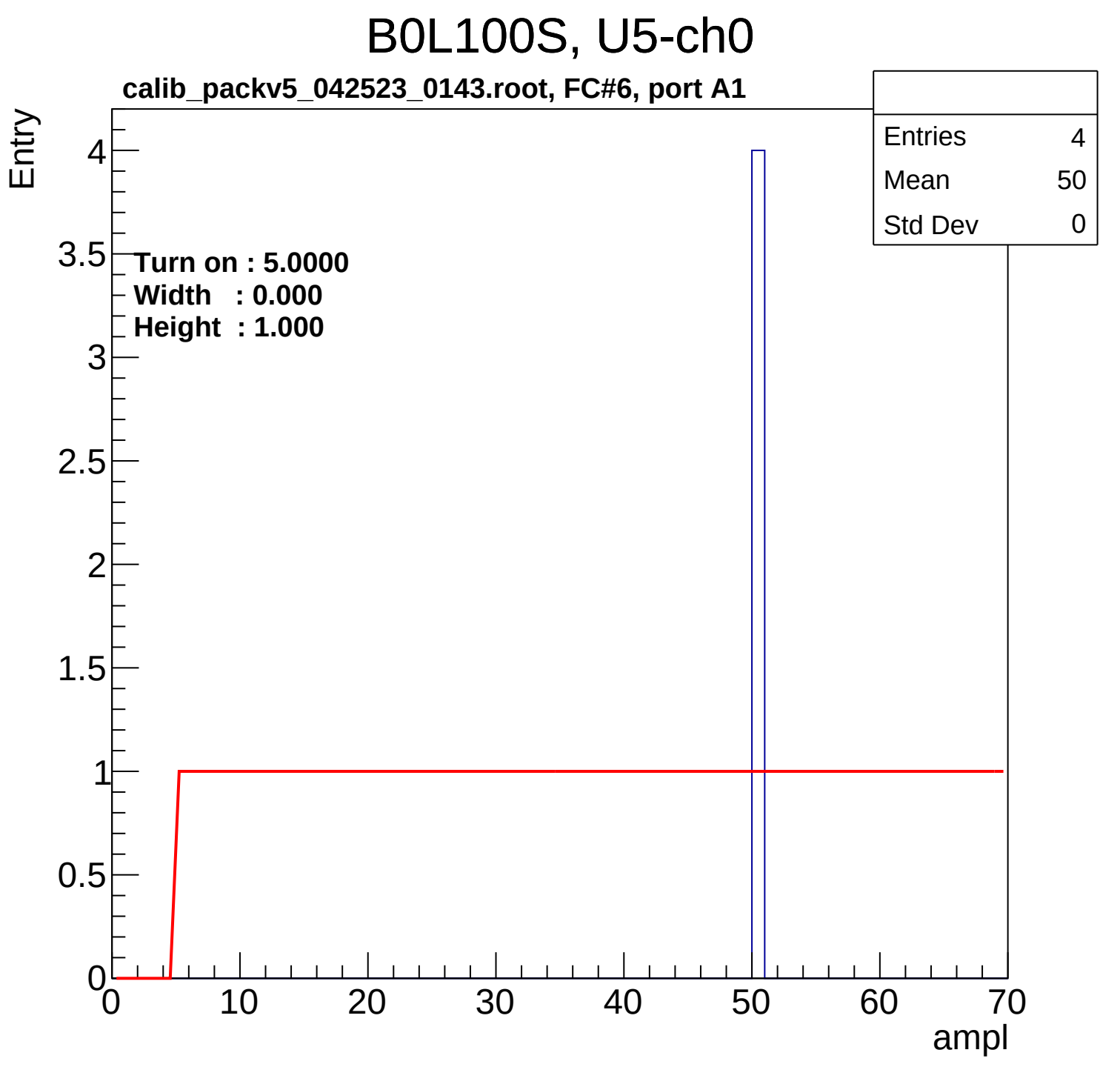
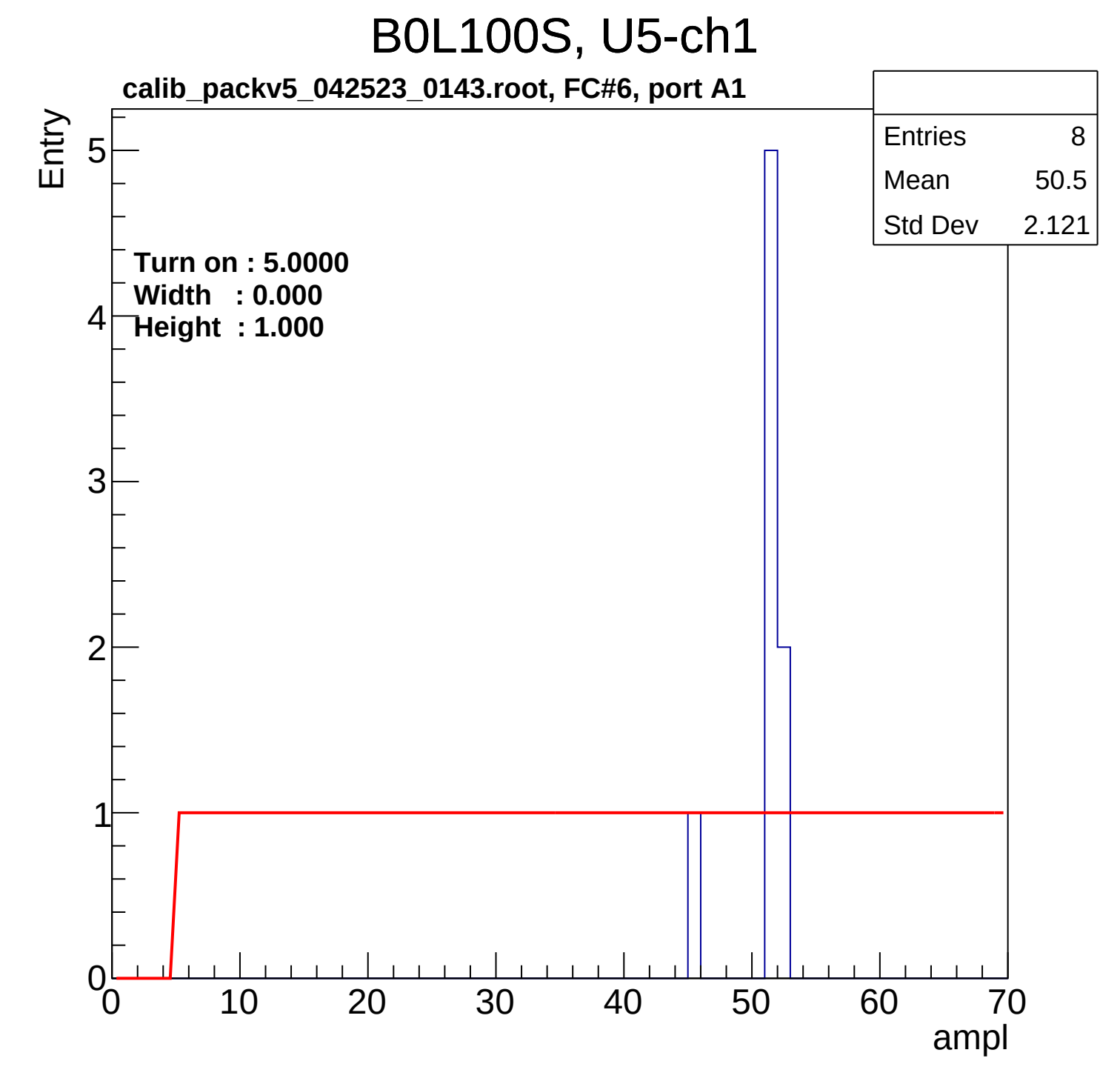
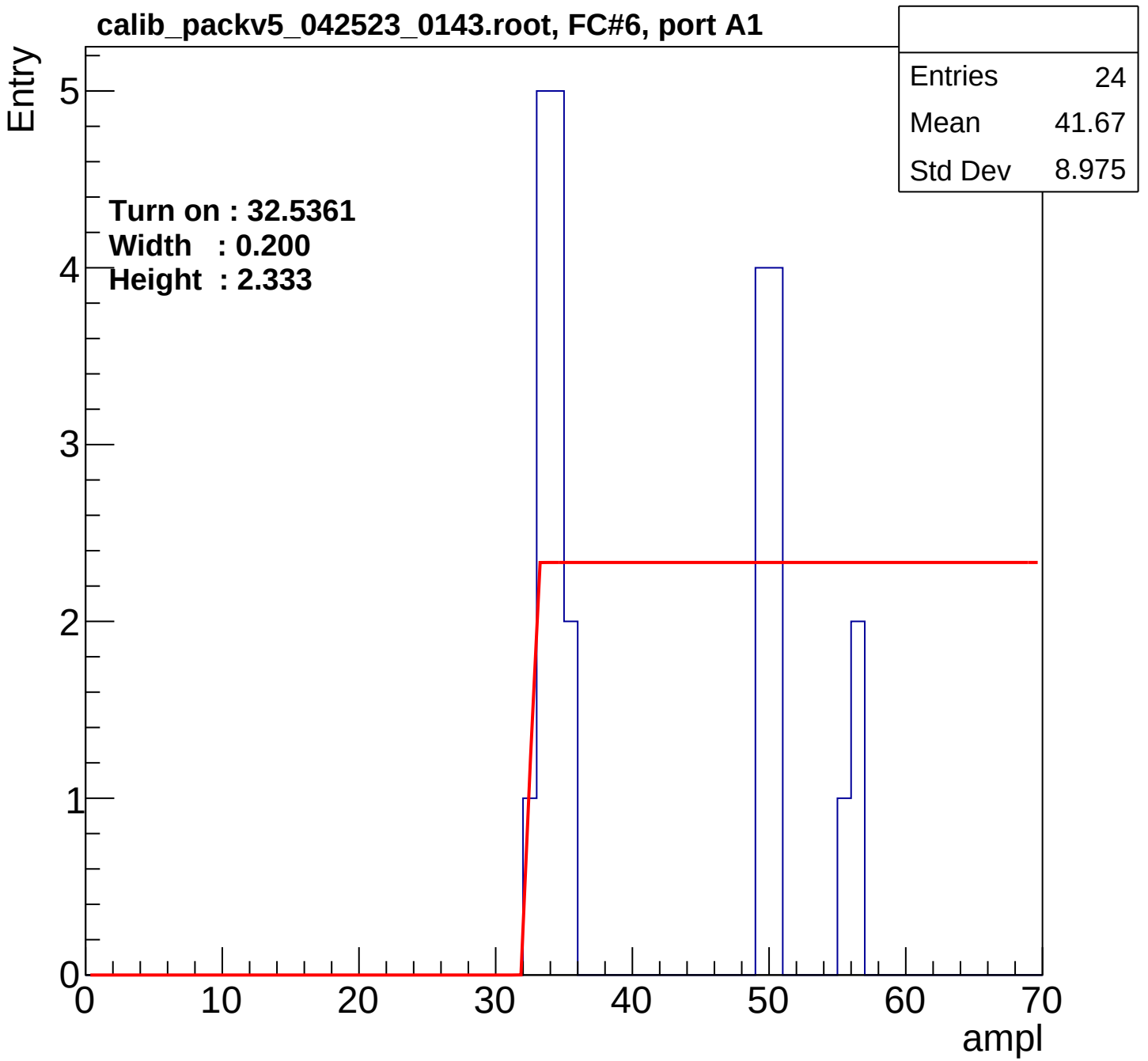
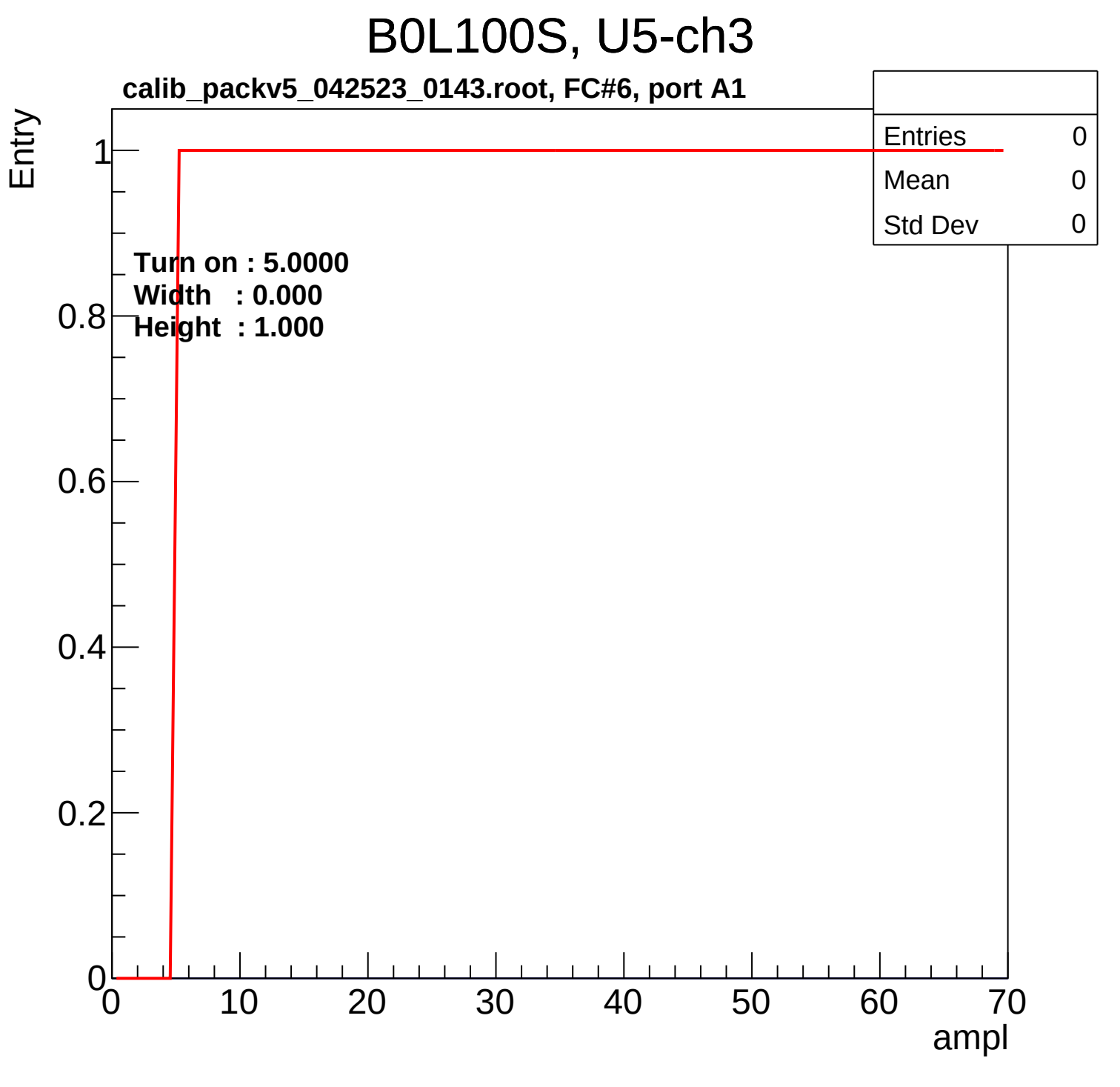
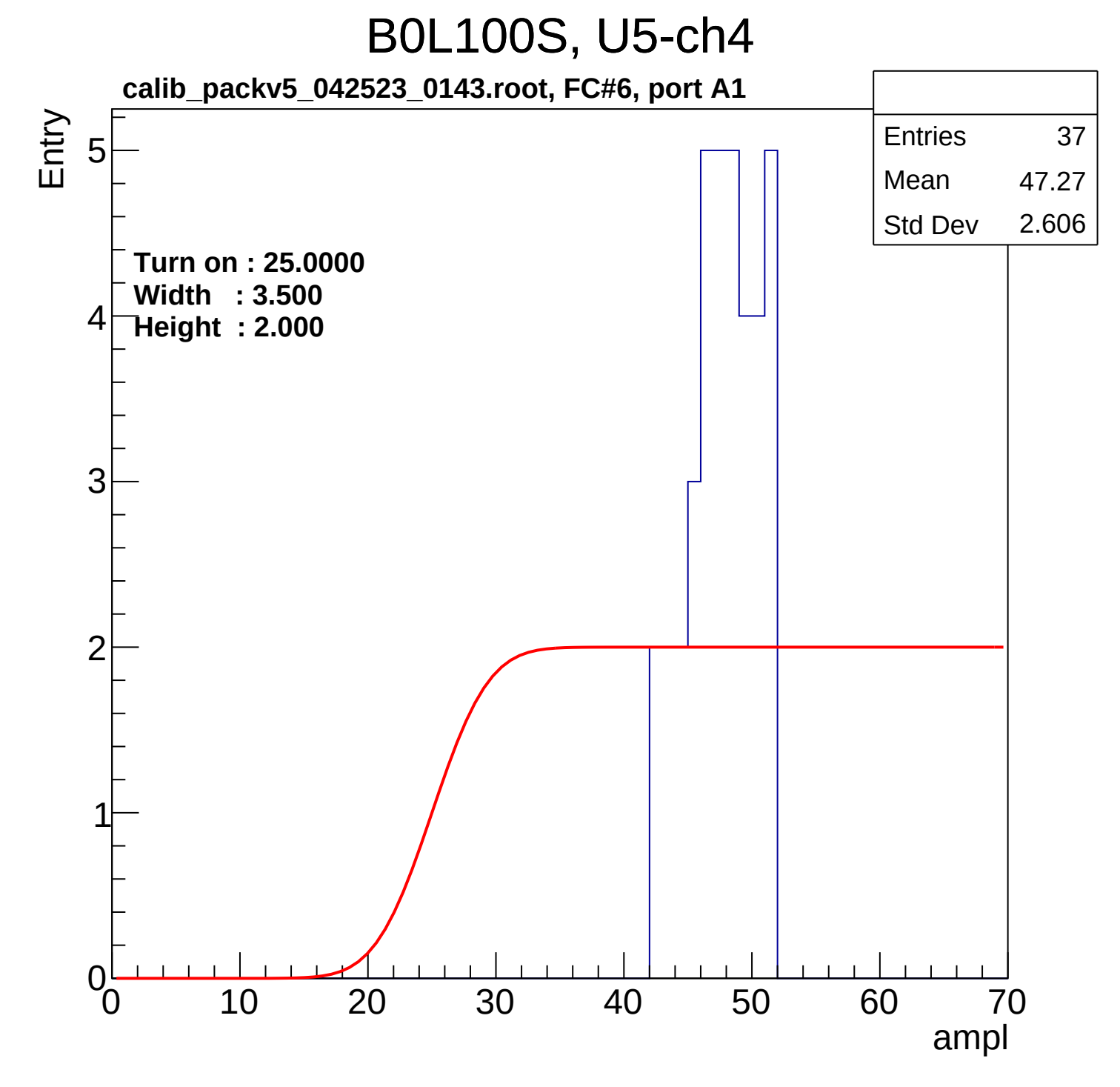
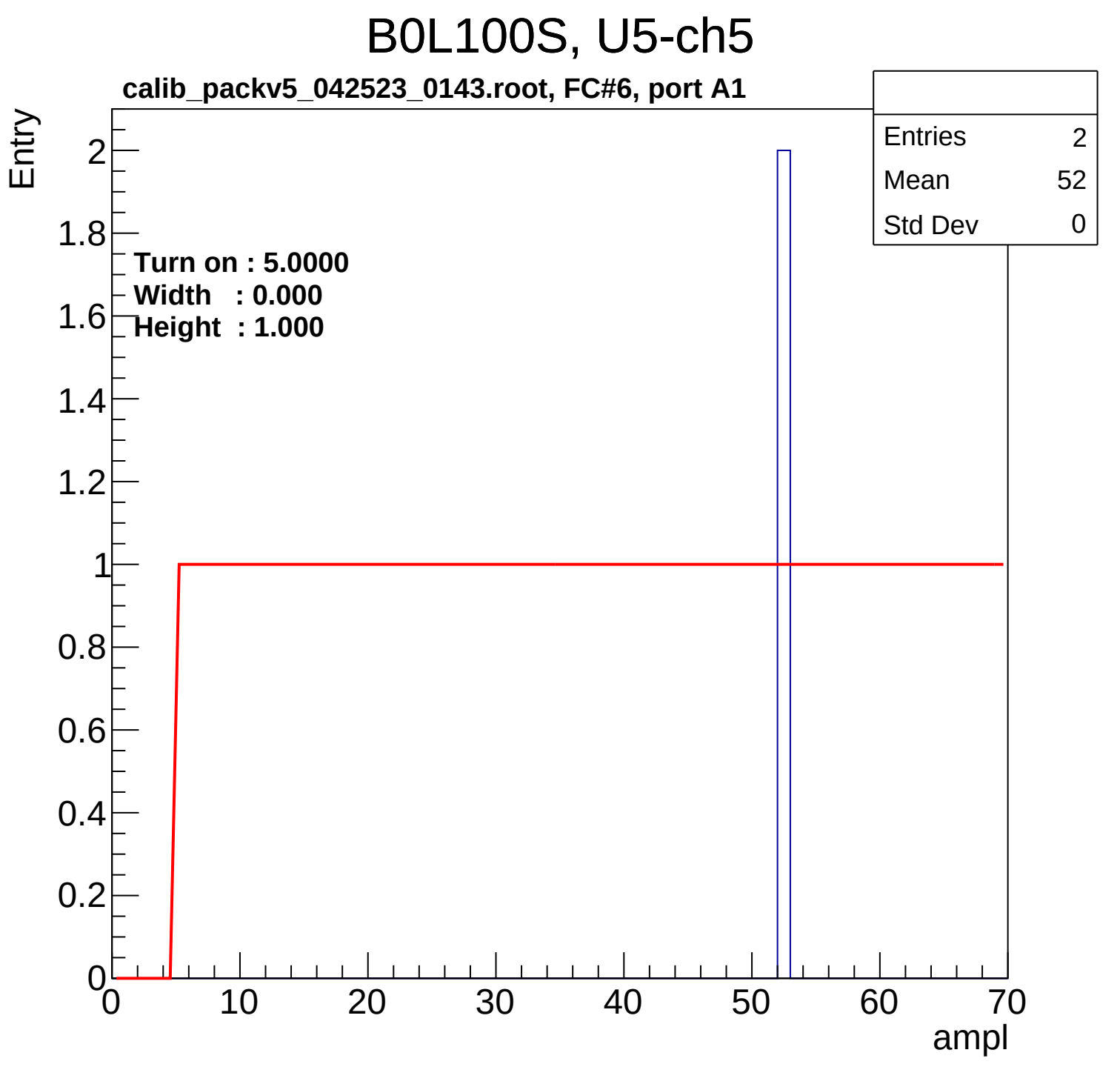

B0L100S, U5-ch0
calib_packv5_042523_0143.root, FC#6, port A1
Entries 4
Mean 50
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

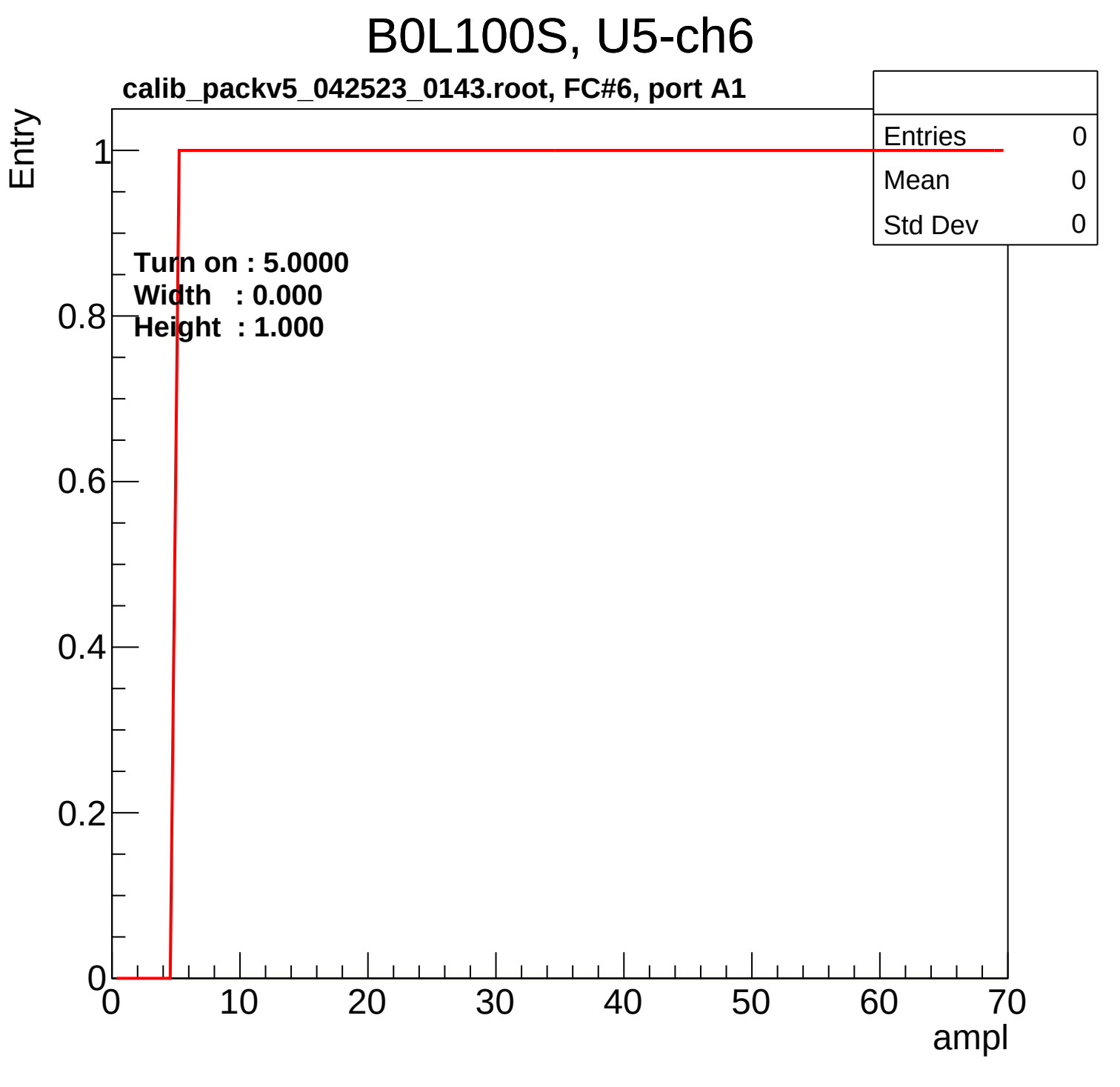

B0L100S, U5-ch1
calib_packv5_042523_0143.root, FC#6, port A1
Entries 8
Mean 50.5
Std Dev 2.121
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

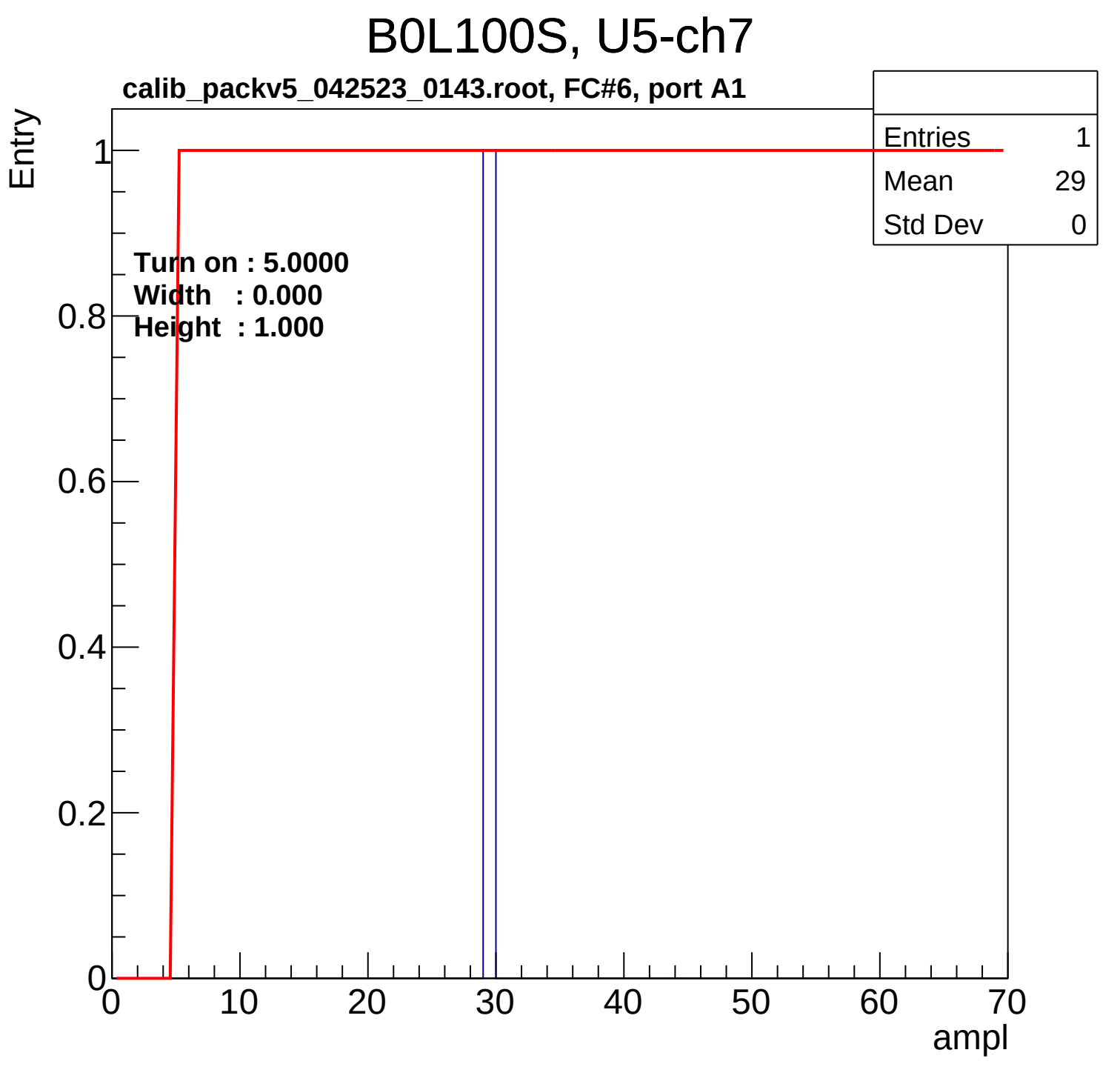

B0L100S, U5-ch2
calib_packv5_042523_0143.root, FC#6, port A1
Entries 24
Mean 41.67
Std Dev 8.975
Turn on : 32.5361
Width : 0.200
Height : 2.333
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

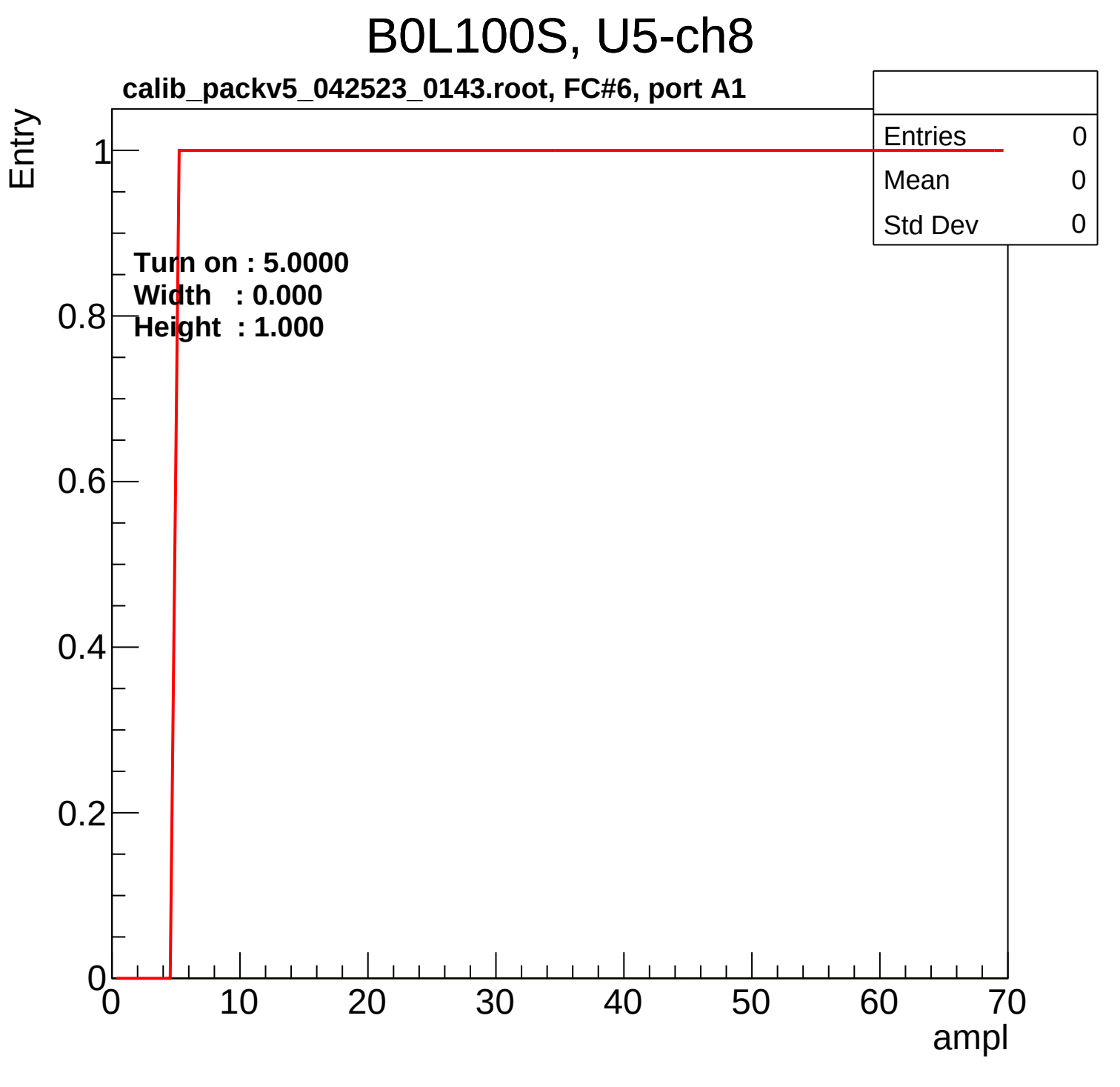

B0L100S, U5-ch3
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

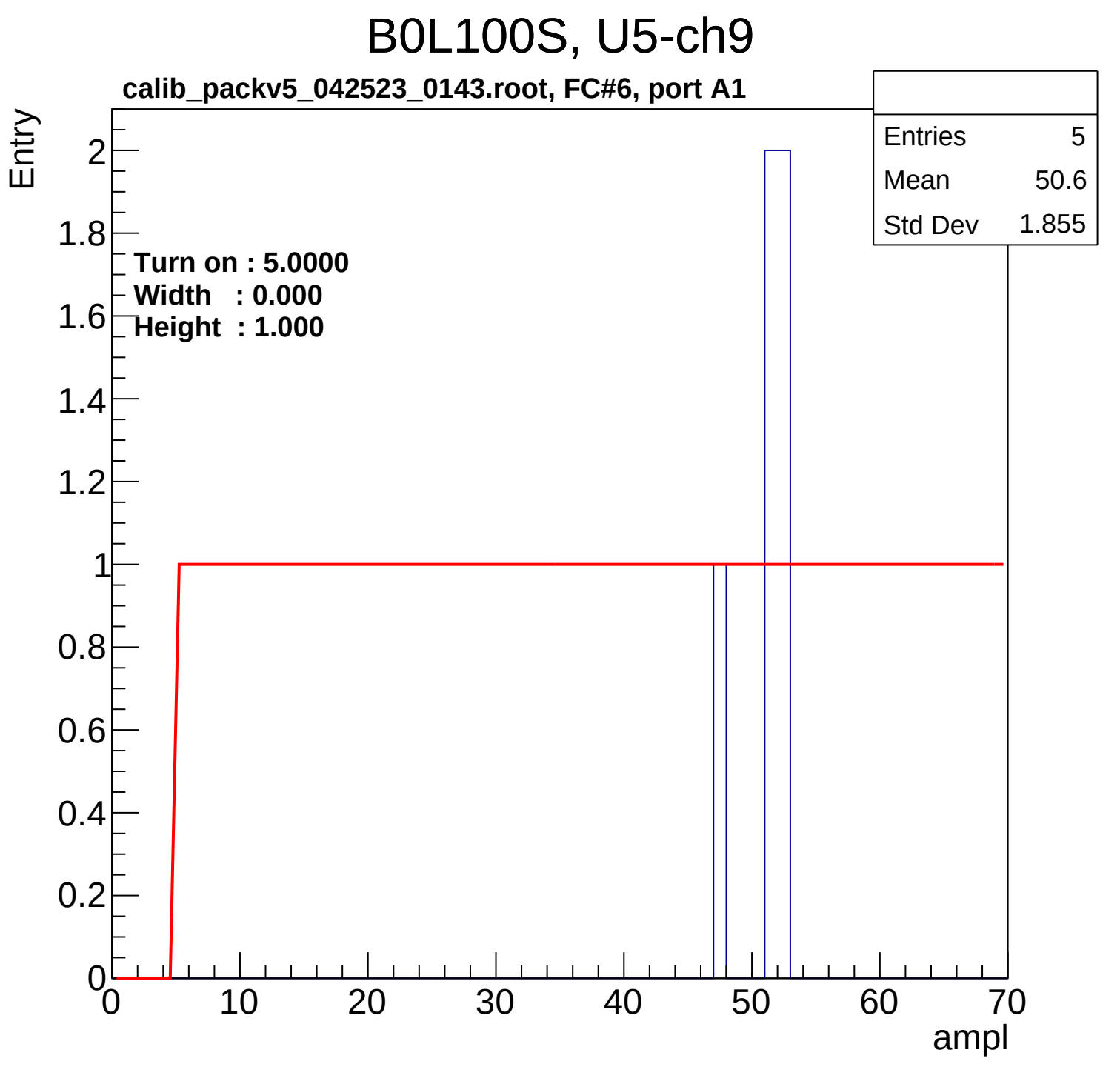

B0L100S, U5-ch4
calib_packv5_042523_0143.root, FC#6, port A1
Entries 37
Mean 47.27
Std Dev 2.606
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

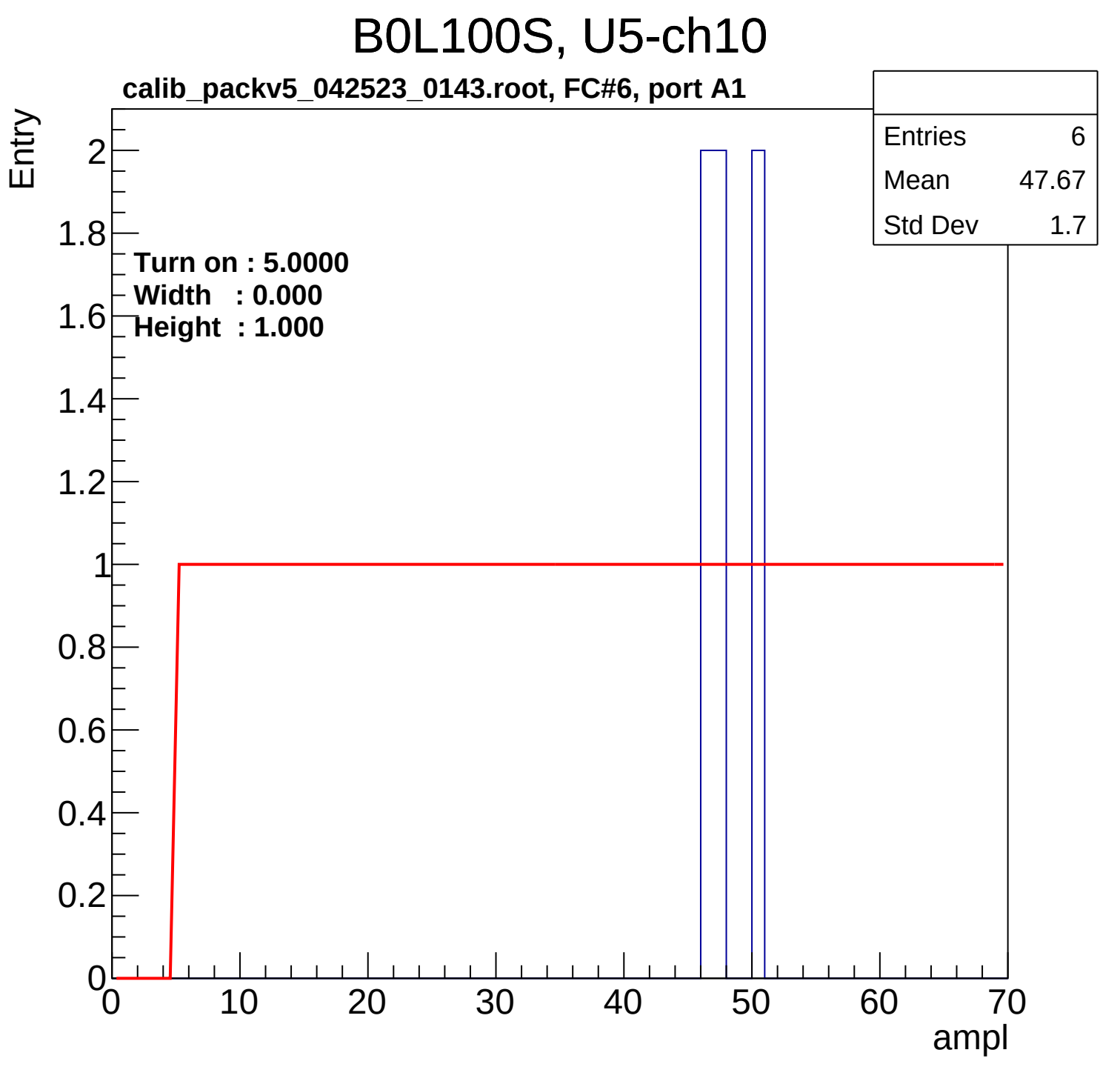

B0L100S, U5-ch5
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 52
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

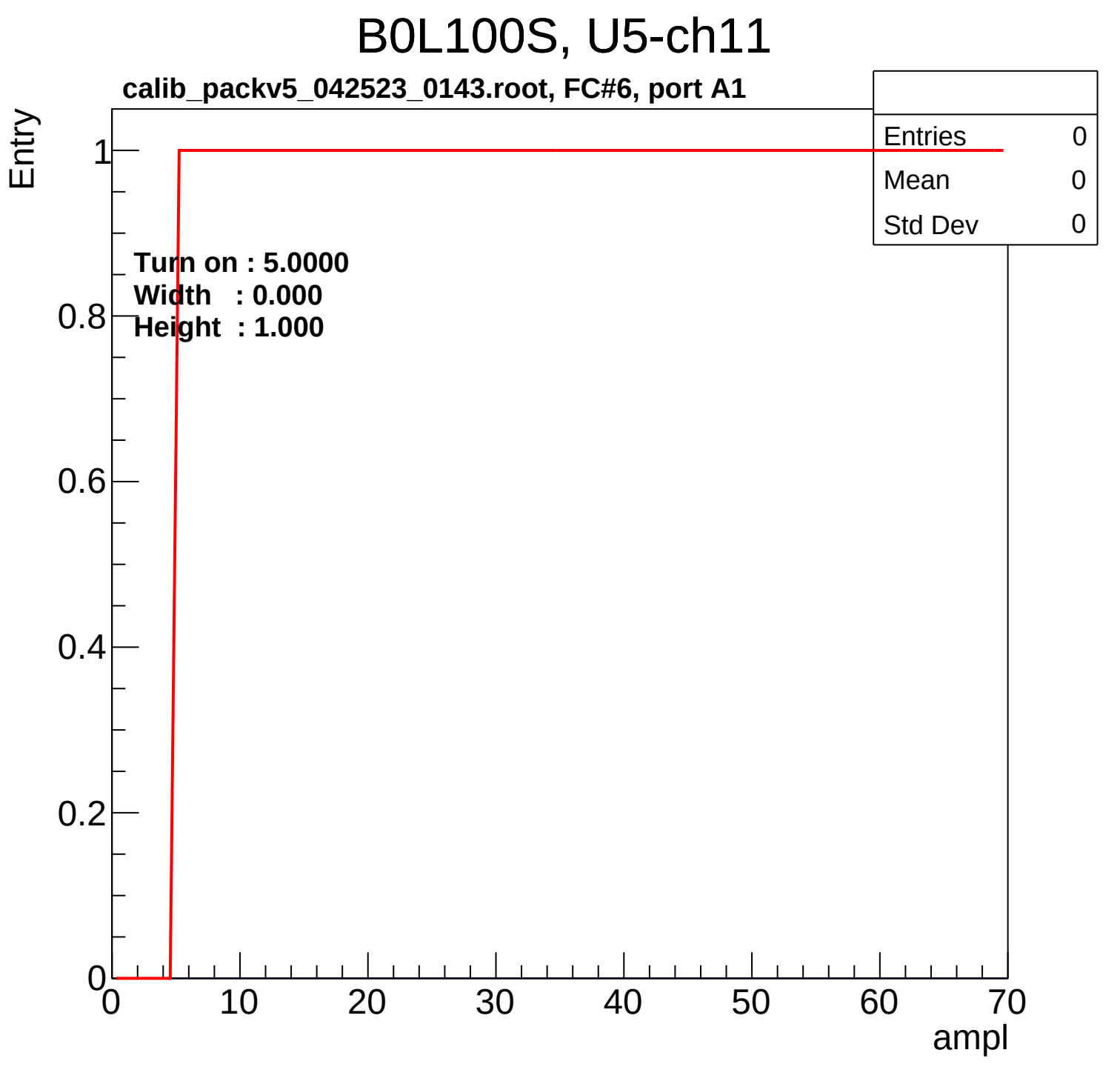

B0L100S, U5-ch6
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

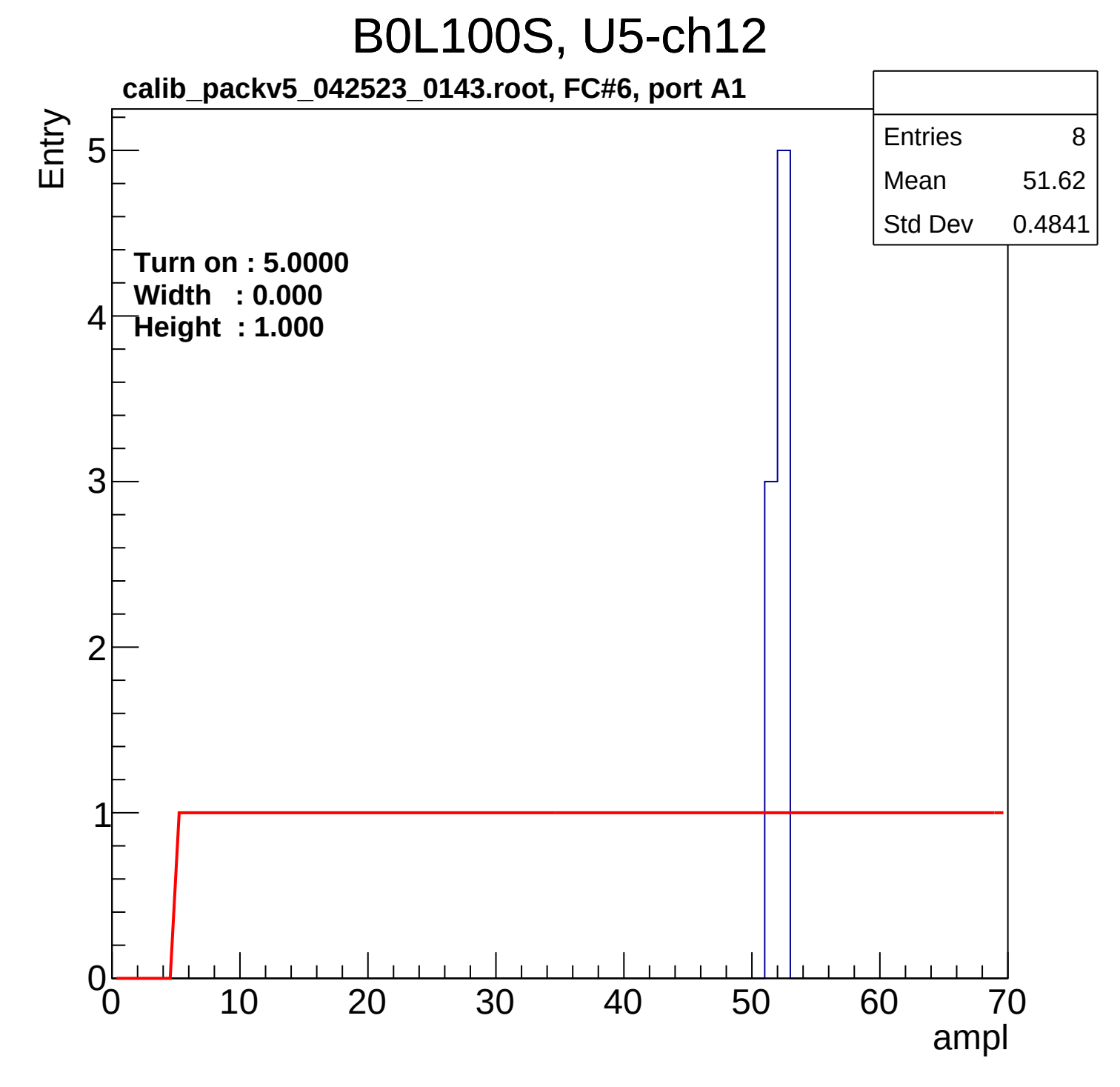

B0L100S, U5-ch7
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 29
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

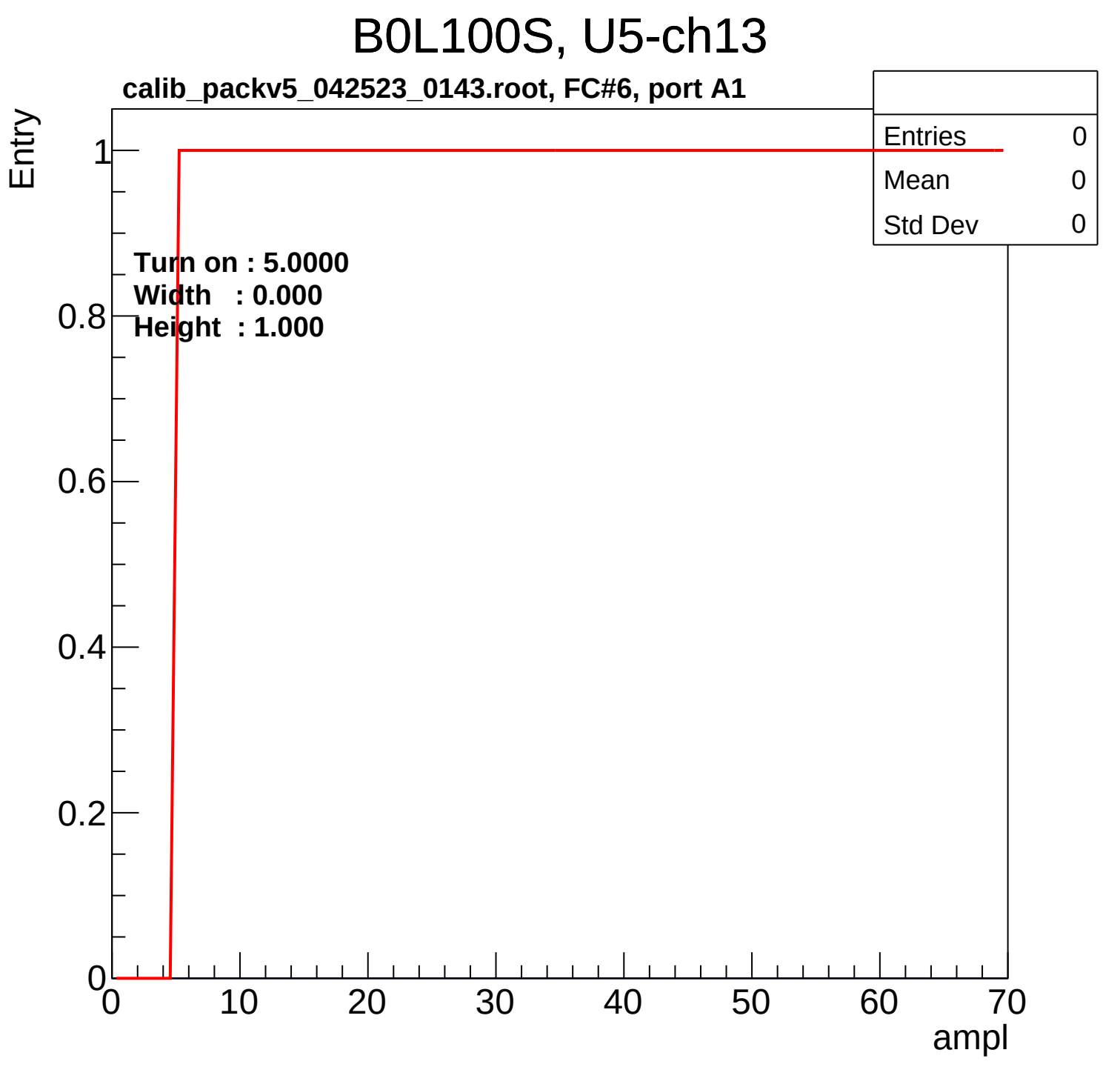

B0L100S, U5-ch8
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

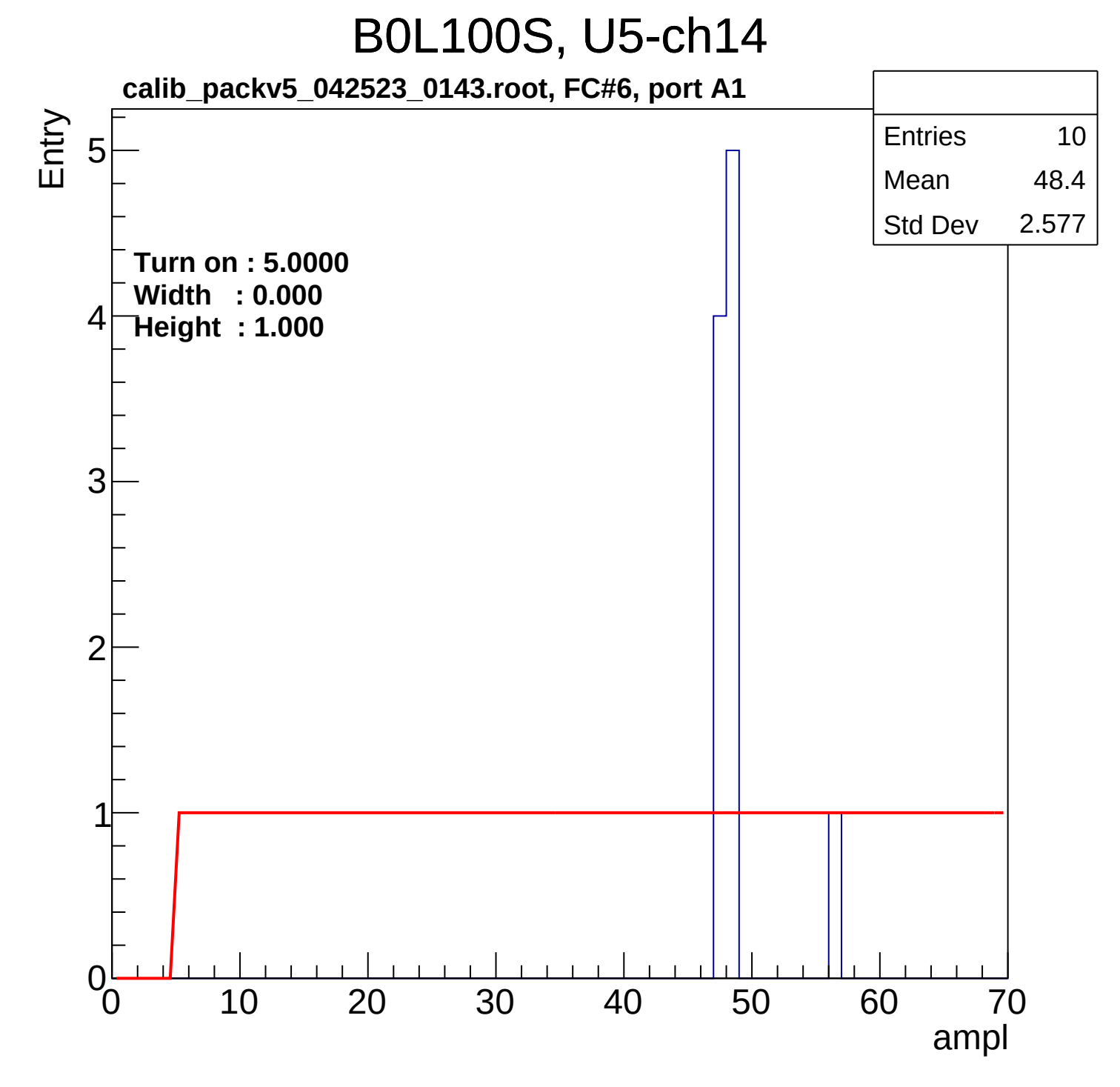

B0L100S, U5-ch9
calib_packv5_042523_0143.root, FC#6, port A1
Entries 5
Mean 50.6
Std Dev 1.855
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

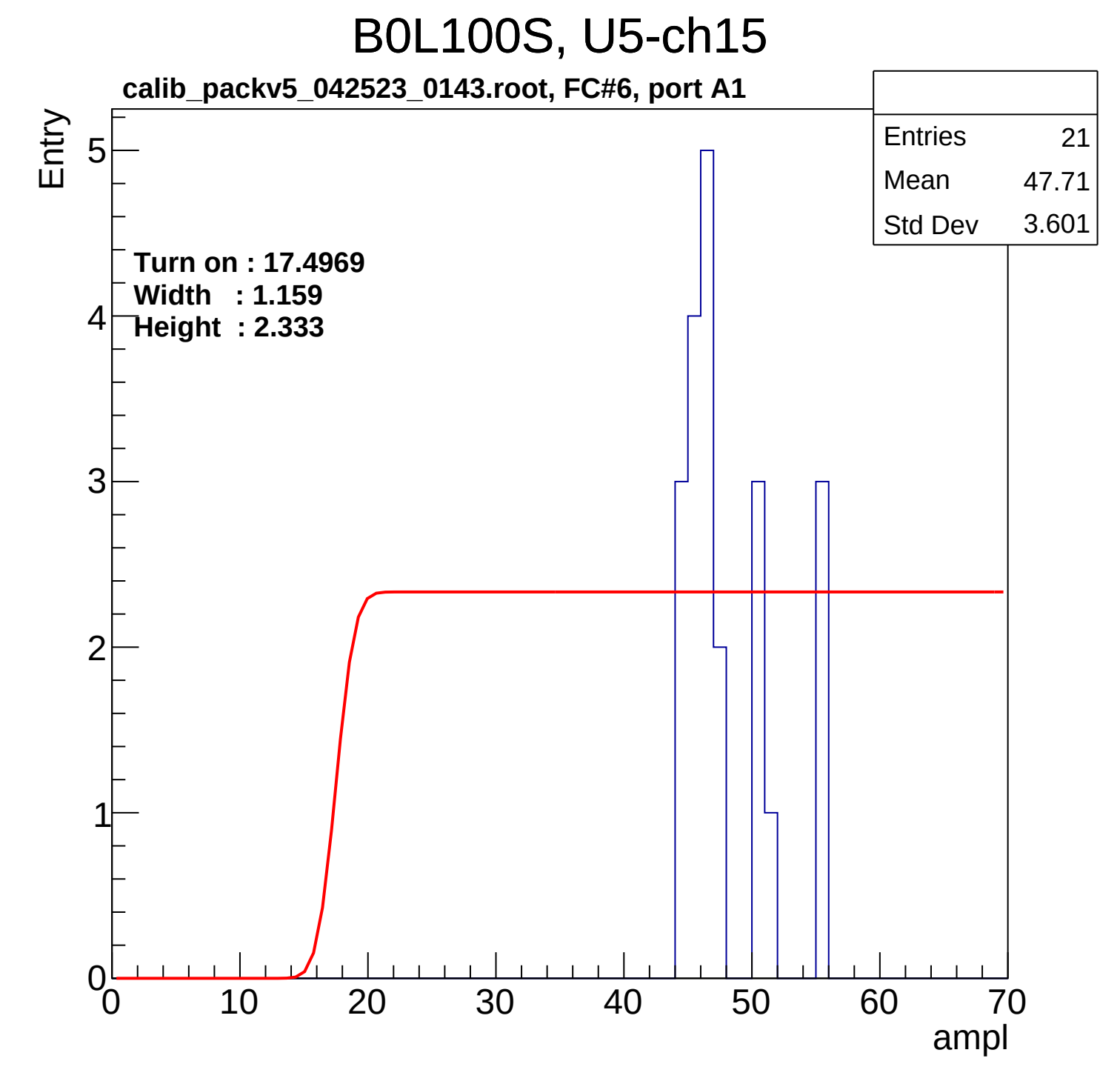

B0L100S, U5-ch10
calib_packv5_042523_0143.root, FC#6, port A1
Entries 6
Mean 47.67
Std Dev 1.7
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

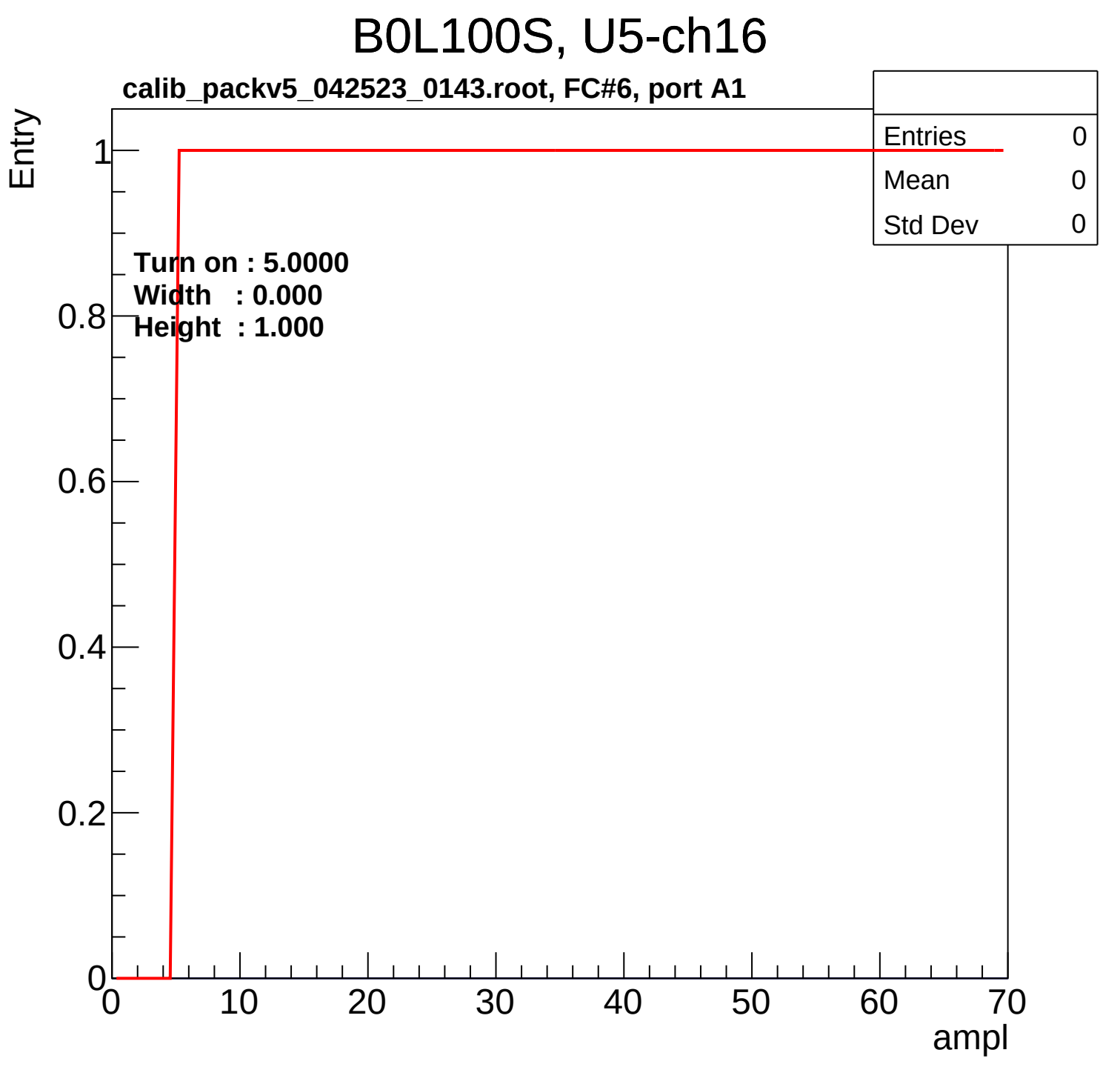

B0L100S, U5-ch11
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

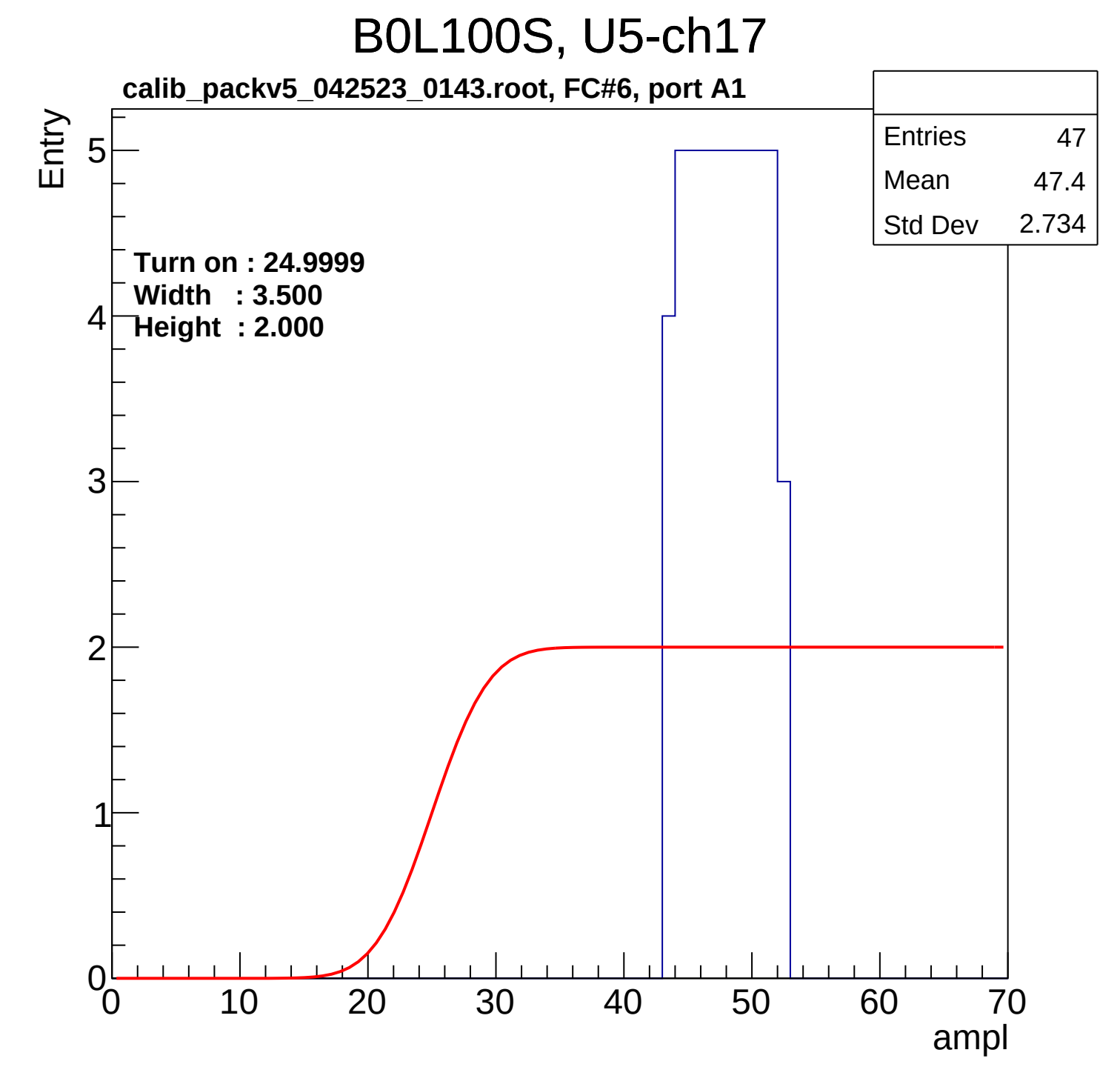

B0L100S, U5-ch12
calib_packv5_042523_0143.root, FC#6, port A1
Entries 8
Mean 51.62
Std Dev 0.4841
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

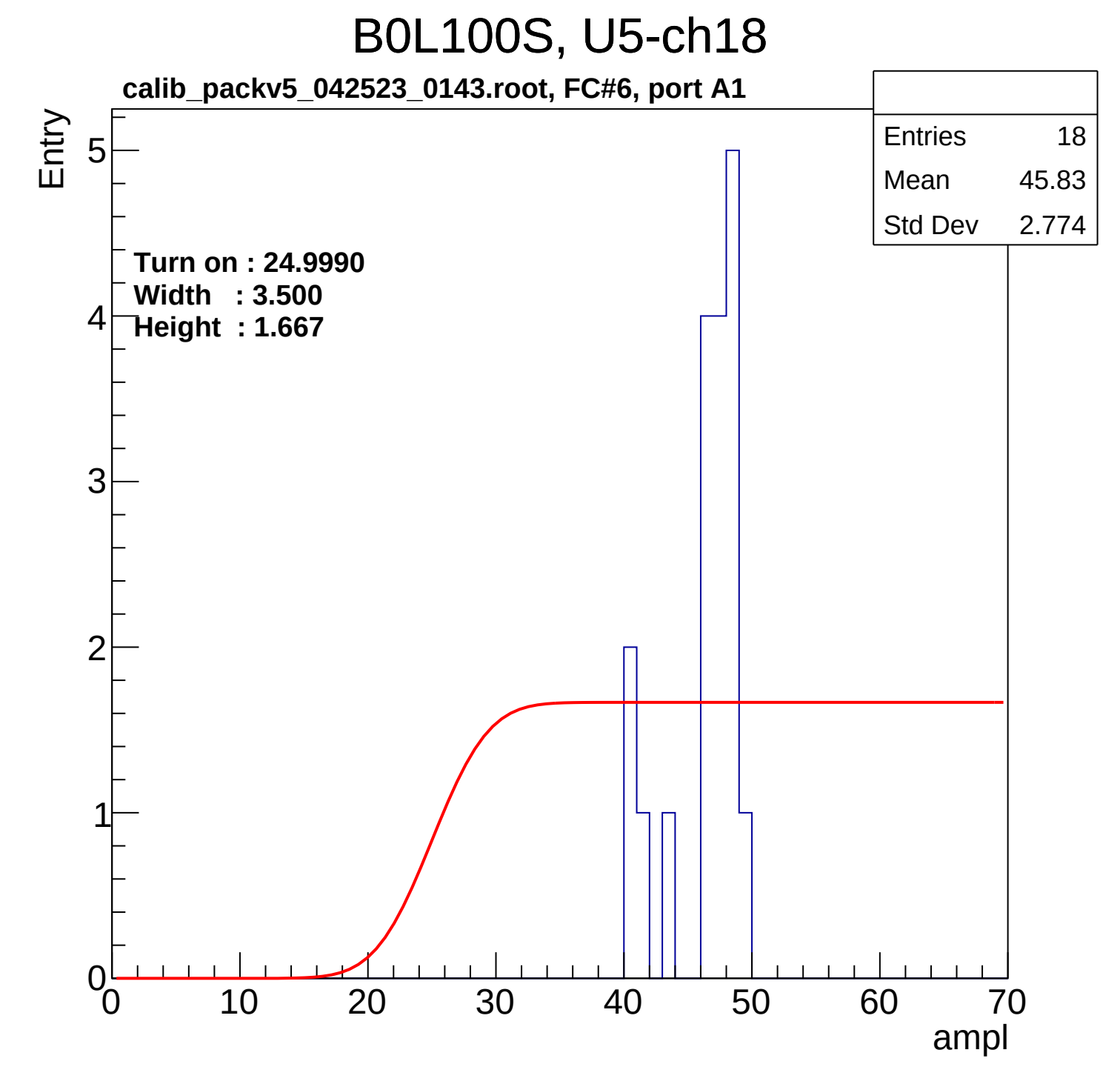

B0L100S, U5-ch13
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

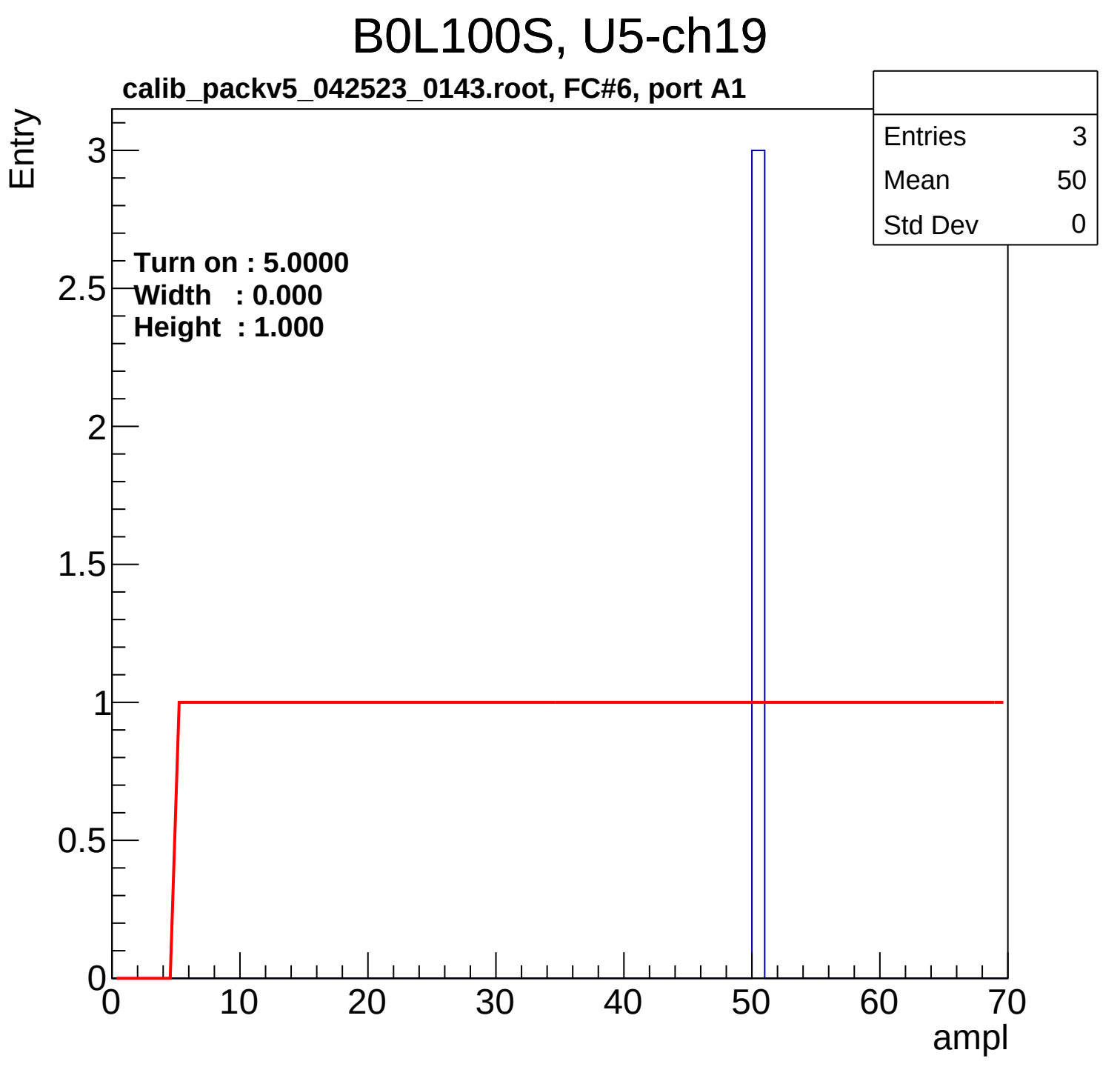

B0L100S, U5-ch14
calib_packv5_042523_0143.root, FC#6, port A1
Entries 10
Mean 48.4
Std Dev 2.577
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

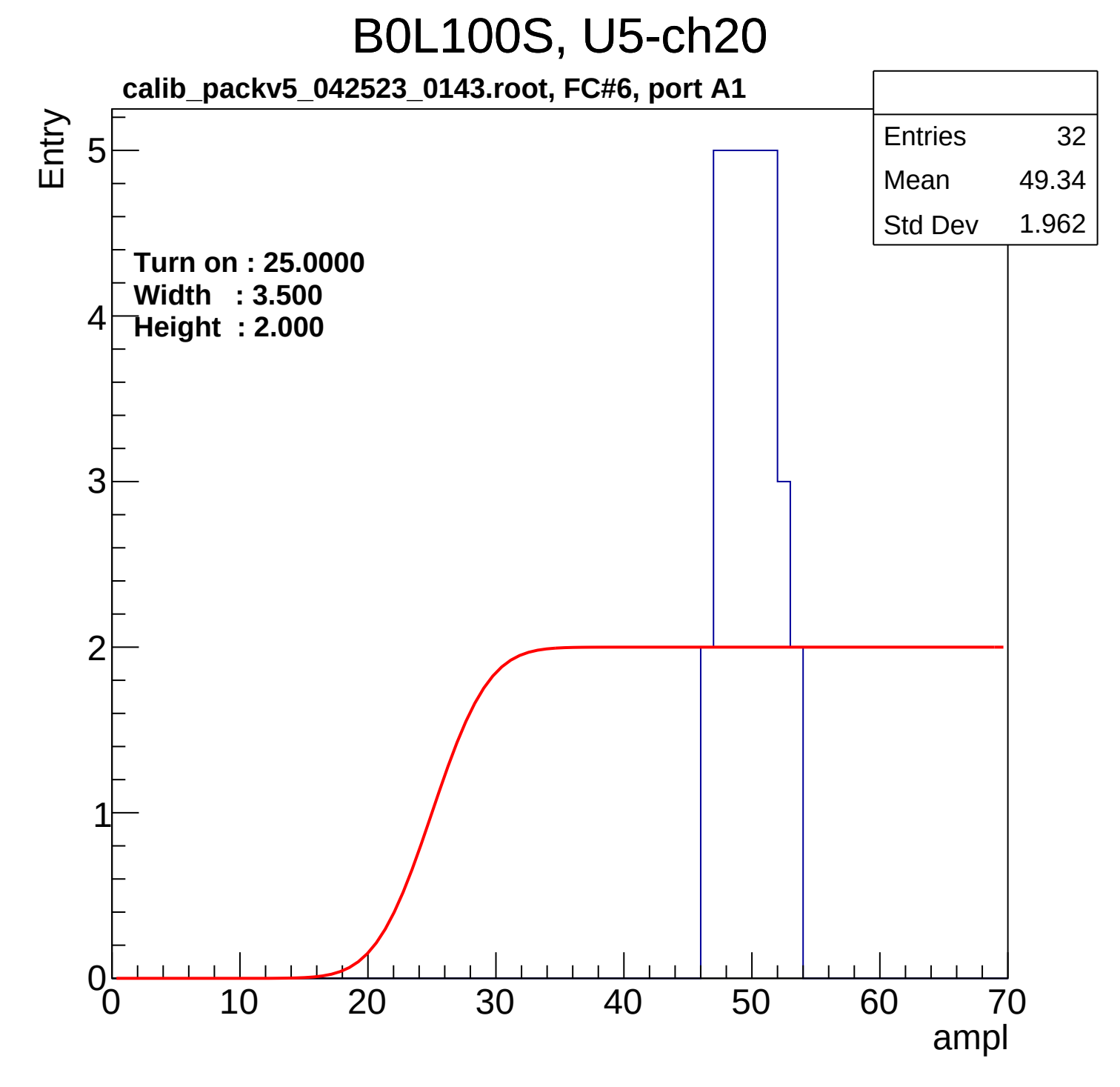

B0L100S, U5-ch15
calib_packv5_042523_0143.root, FC#6, port A1
Entries 21
Mean 47.71
Std Dev 3.601
Turn on : 17.4969
Width : 1.159
Height : 2.333
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

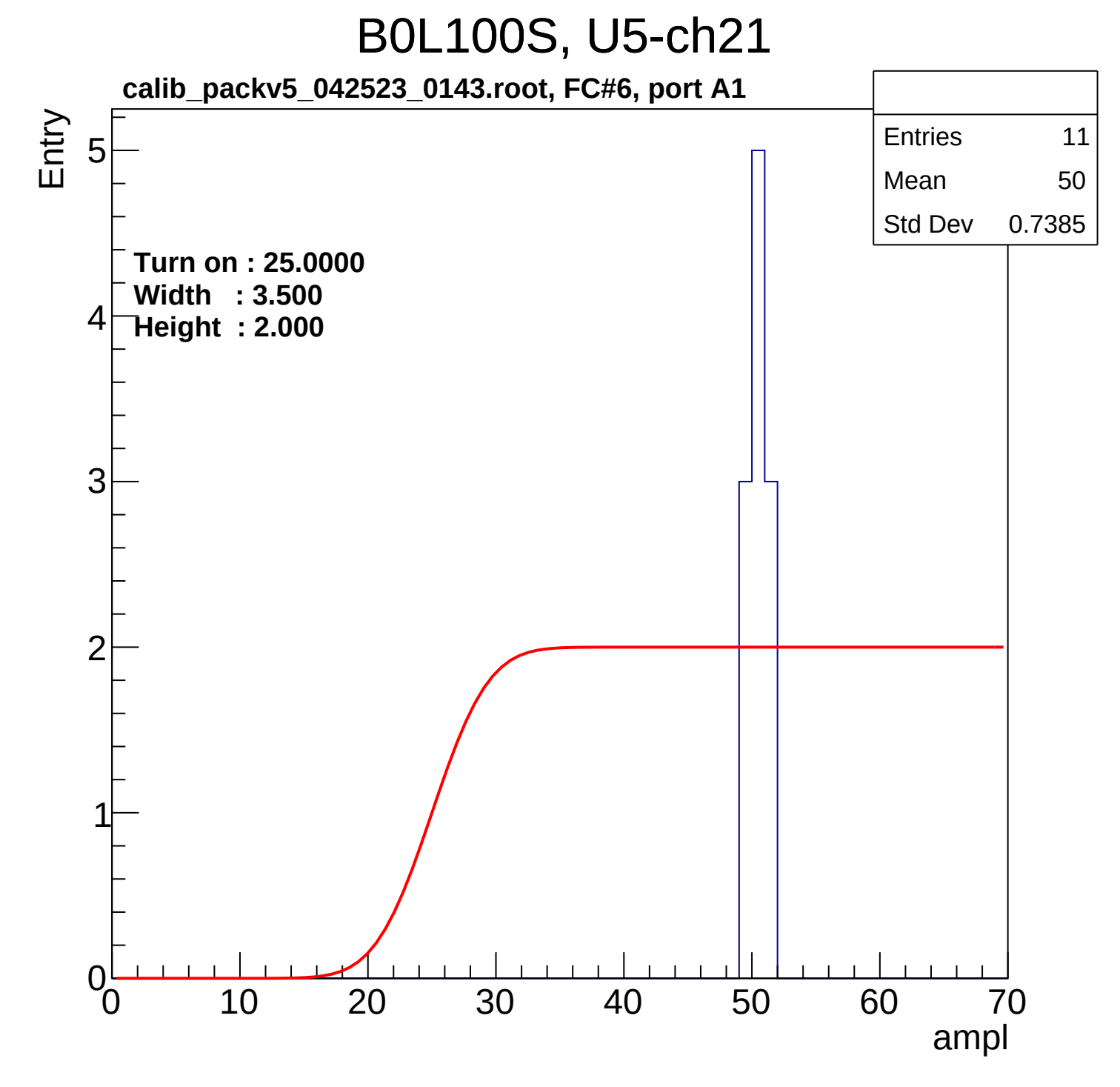

B0L100S, U5-ch16
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

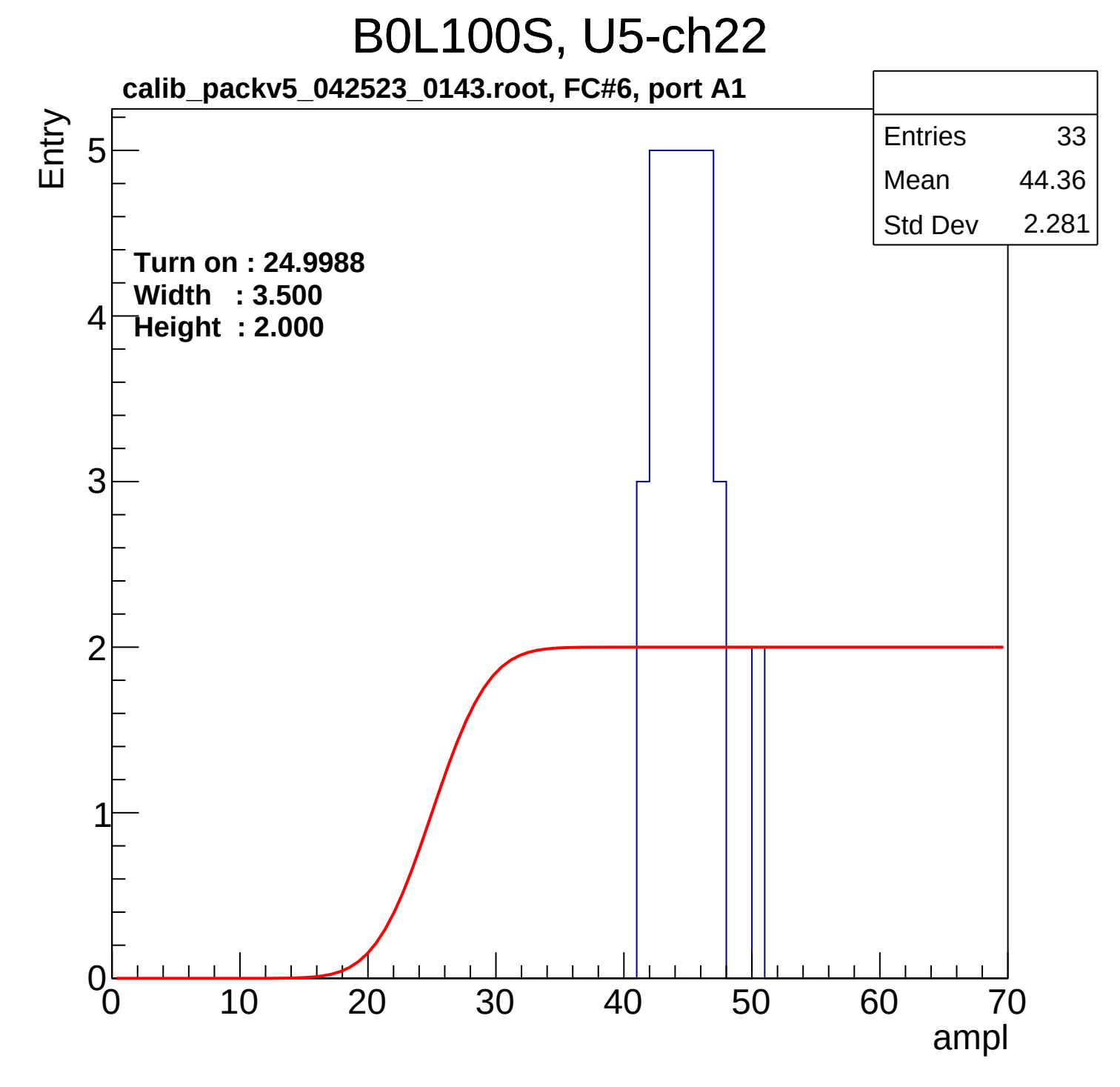

B0L100S, U5-ch17
calib_packv5_042523_0143.root, FC#6, port A1
Entries 47
Mean 47.4
Std Dev 2.734
Turn on : 24.9999
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

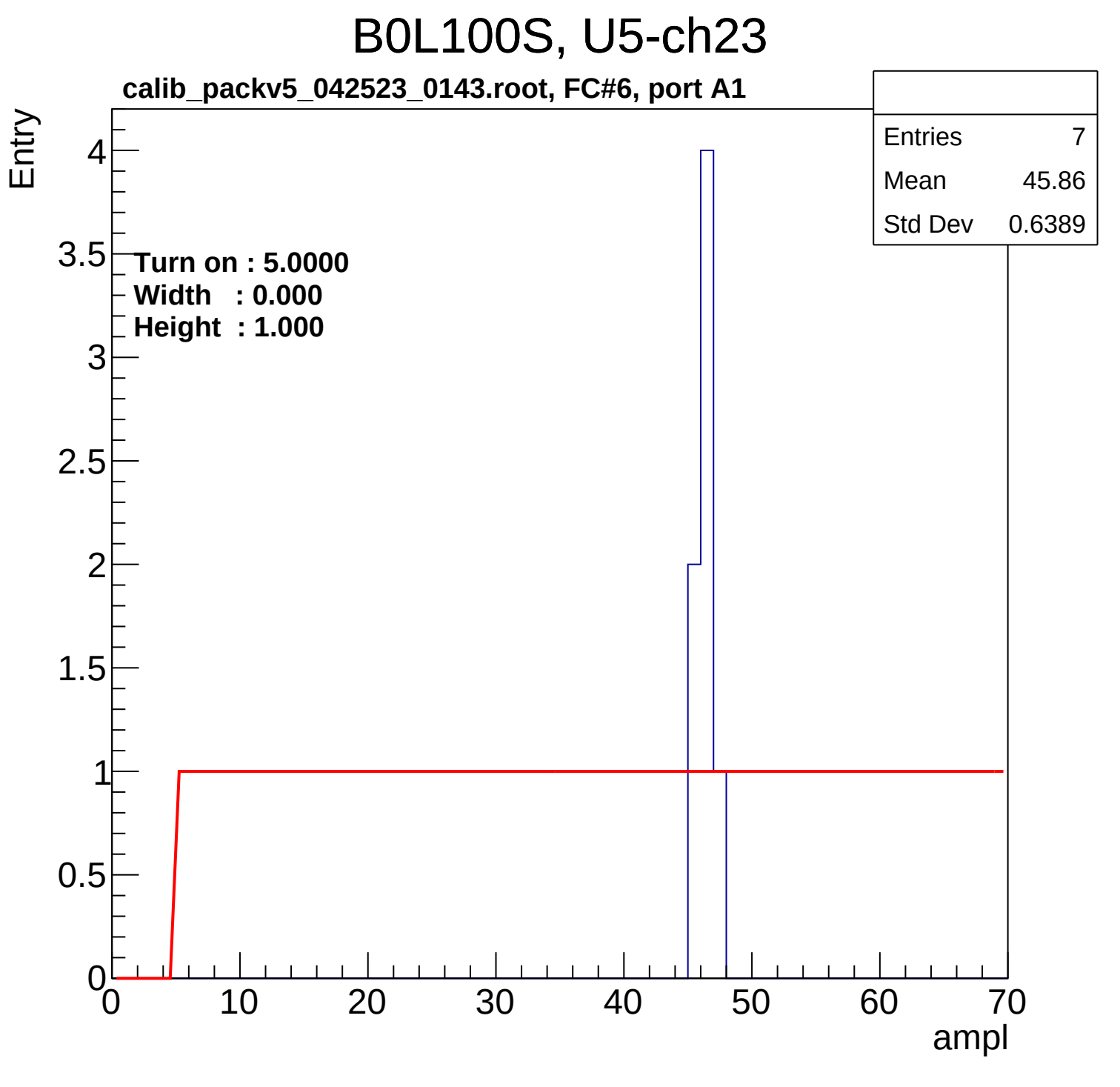

B0L100S, U5-ch18
calib_packv5_042523_0143.root, FC#6, port A1
Entries 18
Mean 45.83
Std Dev 2.774
Turn on : 24.9990
Width : 3.500
Height : 1.667
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

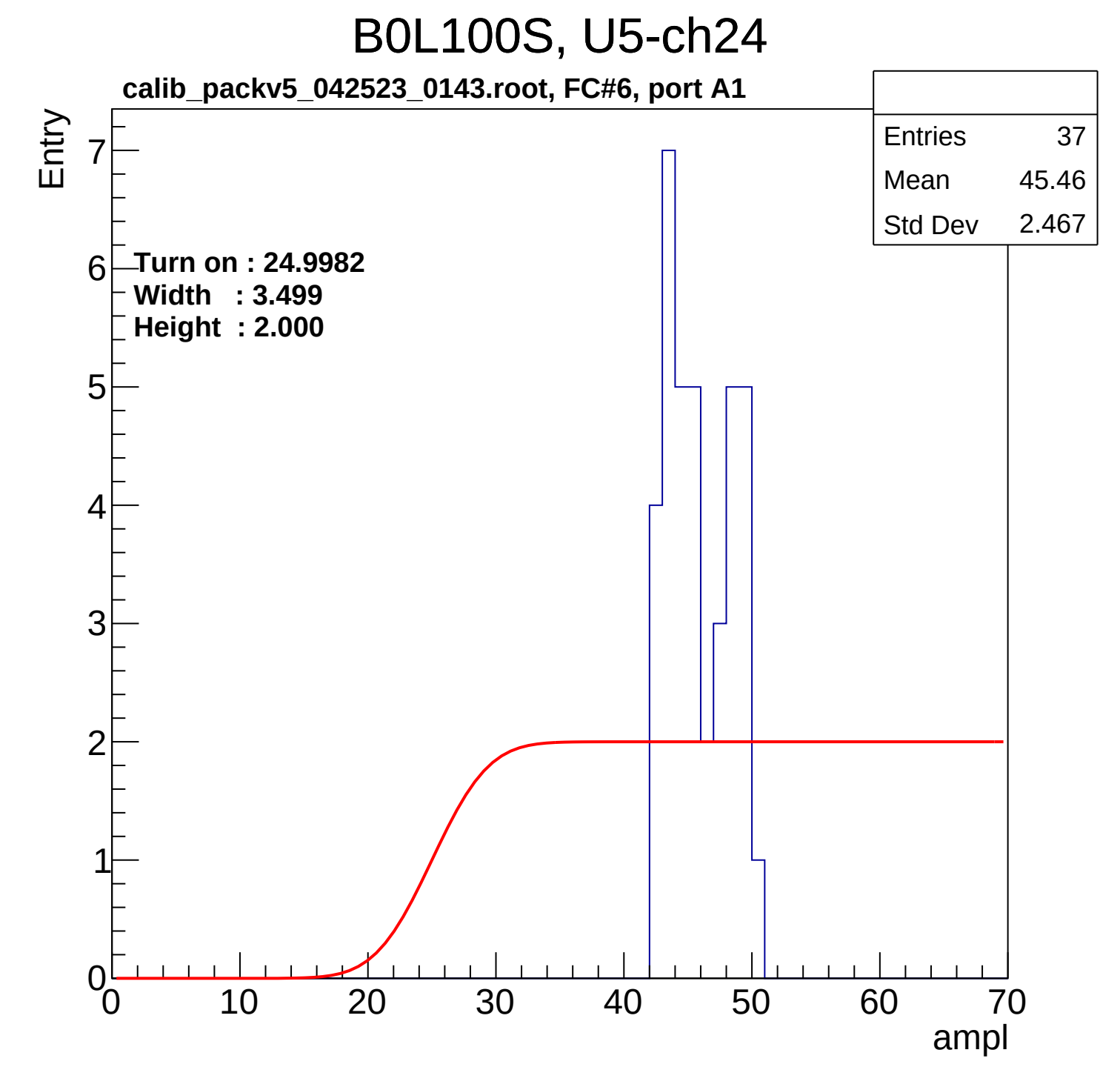

B0L100S, U5-ch19
calib_packv5_042523_0143.root, FC#6, port A1
Entries 3
Mean 50
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

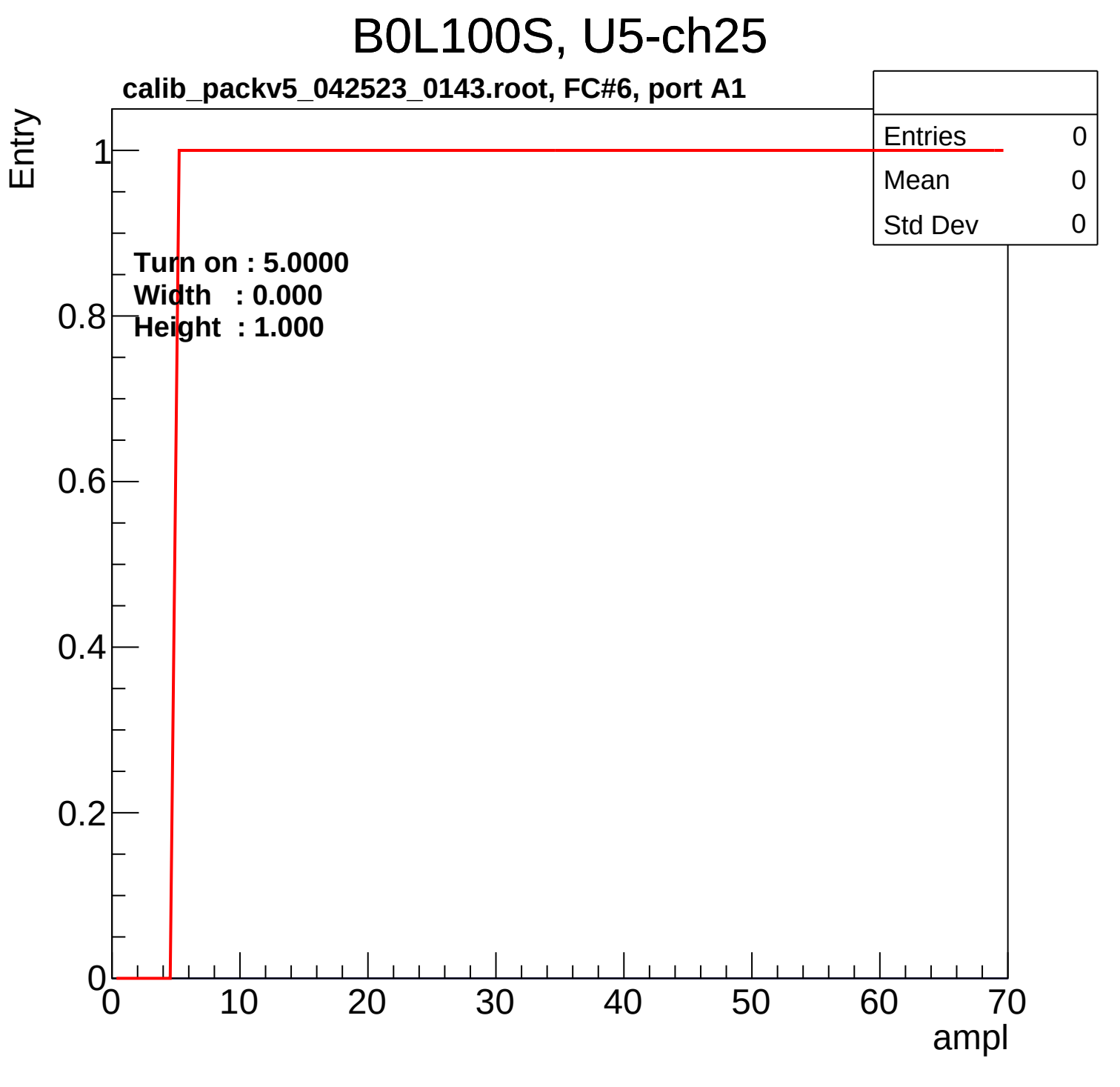

B0L100S, U5-ch20
calib_packv5_042523_0143.root, FC#6, port A1
Entries 32
Mean 49.34
Std Dev 1.962
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

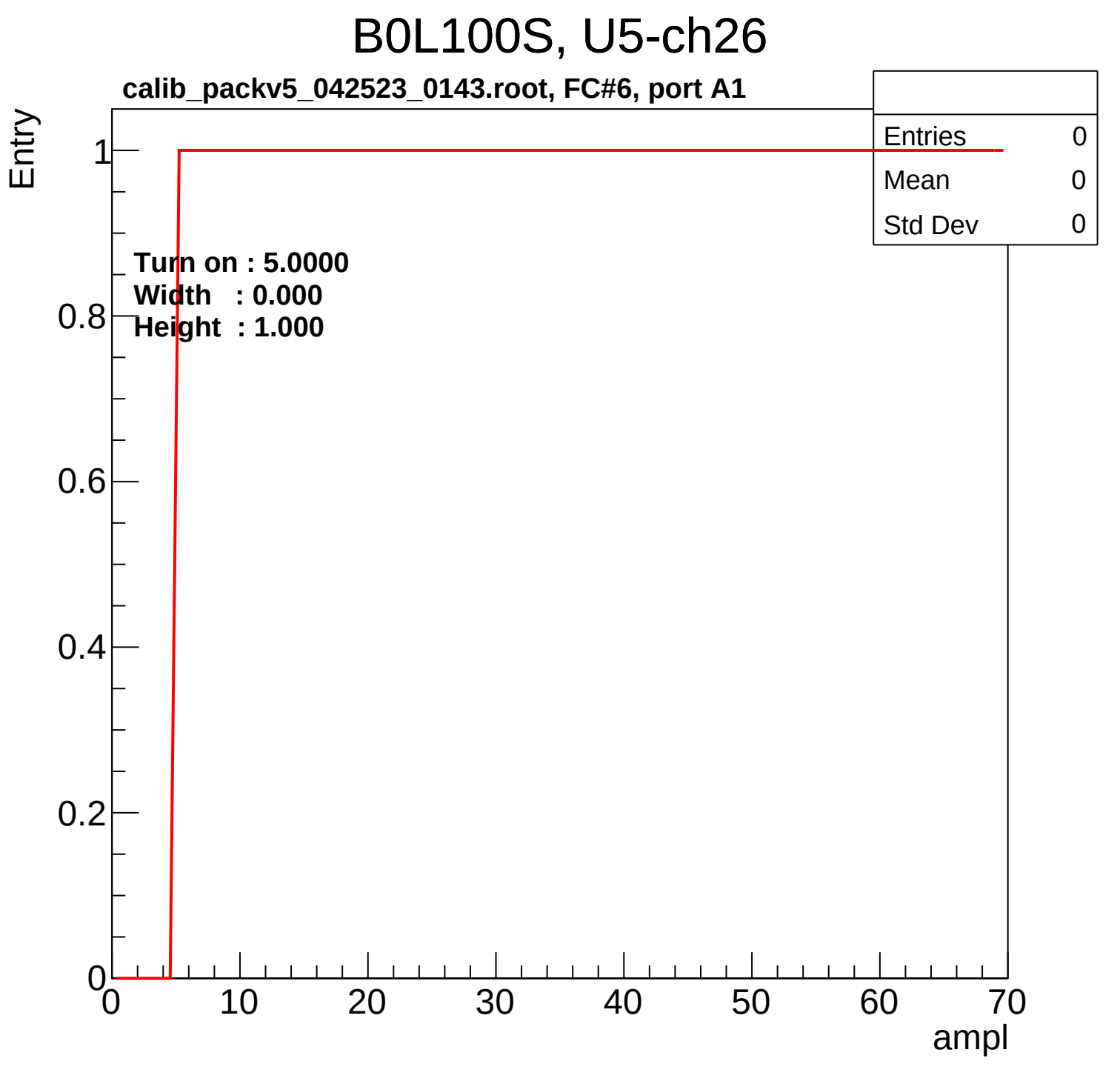

B0L100S, U5-ch21
calib_packv5_042523_0143.root, FC#6, port A1
Entries 11
Mean 50
Std Dev 0.7385
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

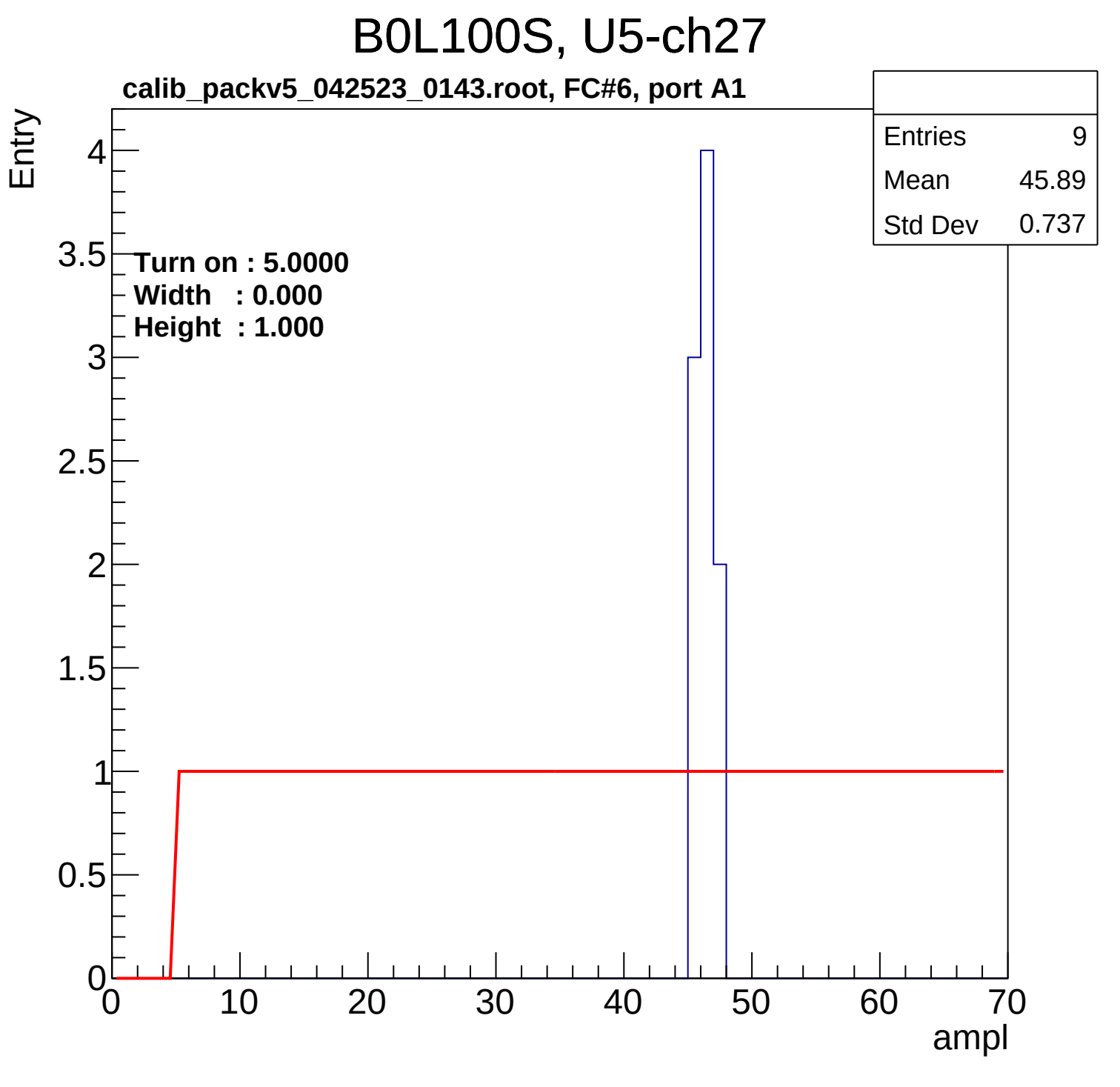

B0L100S, U5-ch22
calib_packv5_042523_0143.root, FC#6, port A1
Entries 33
Mean 44.36
Std Dev 2.281
Turn on : 24.9988
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

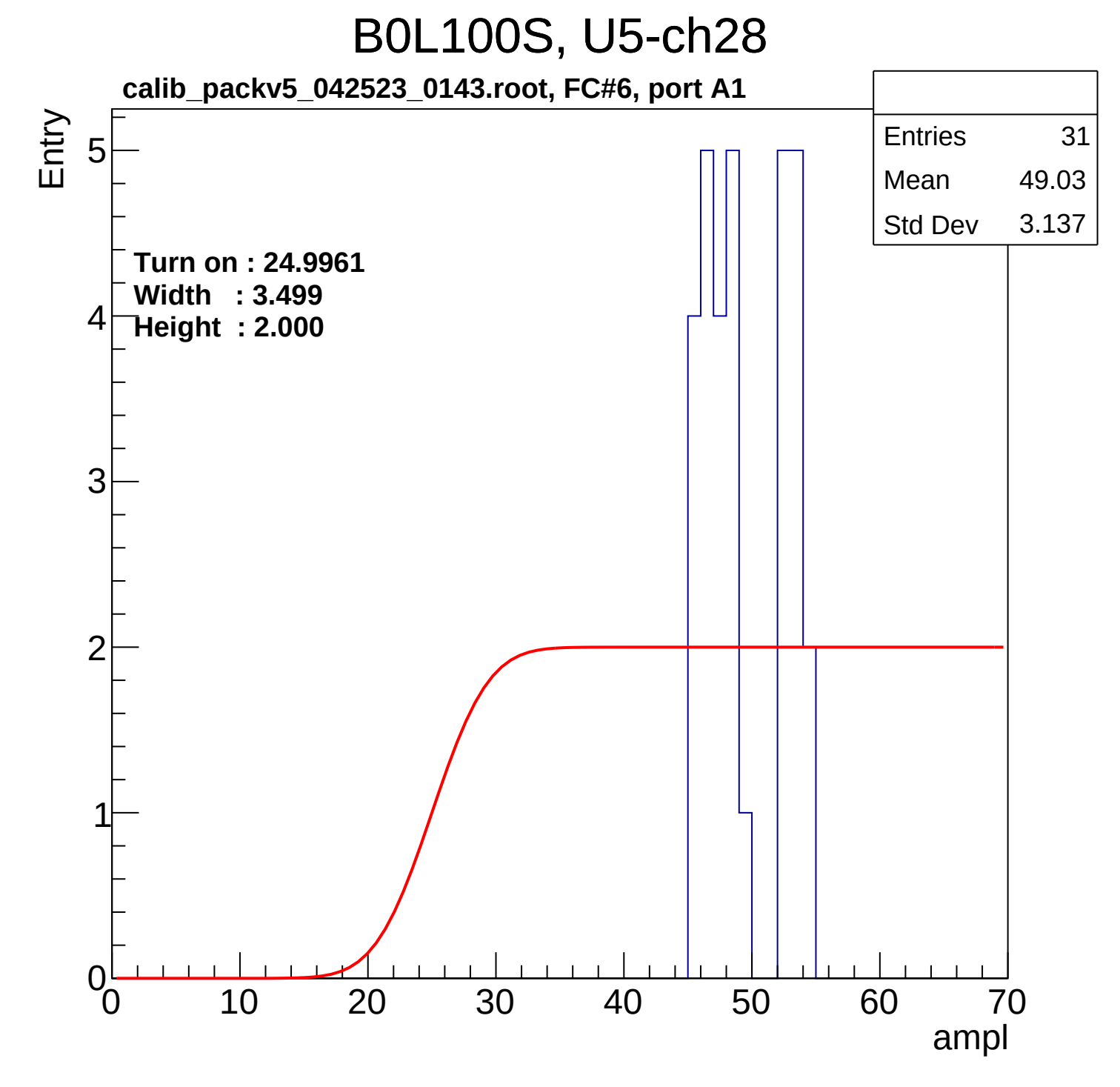

B0L100S, U5-ch23
calib_packv5_042523_0143.root, FC#6, port A1
Entries 7
Mean 45.86
Std Dev 0.6389
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

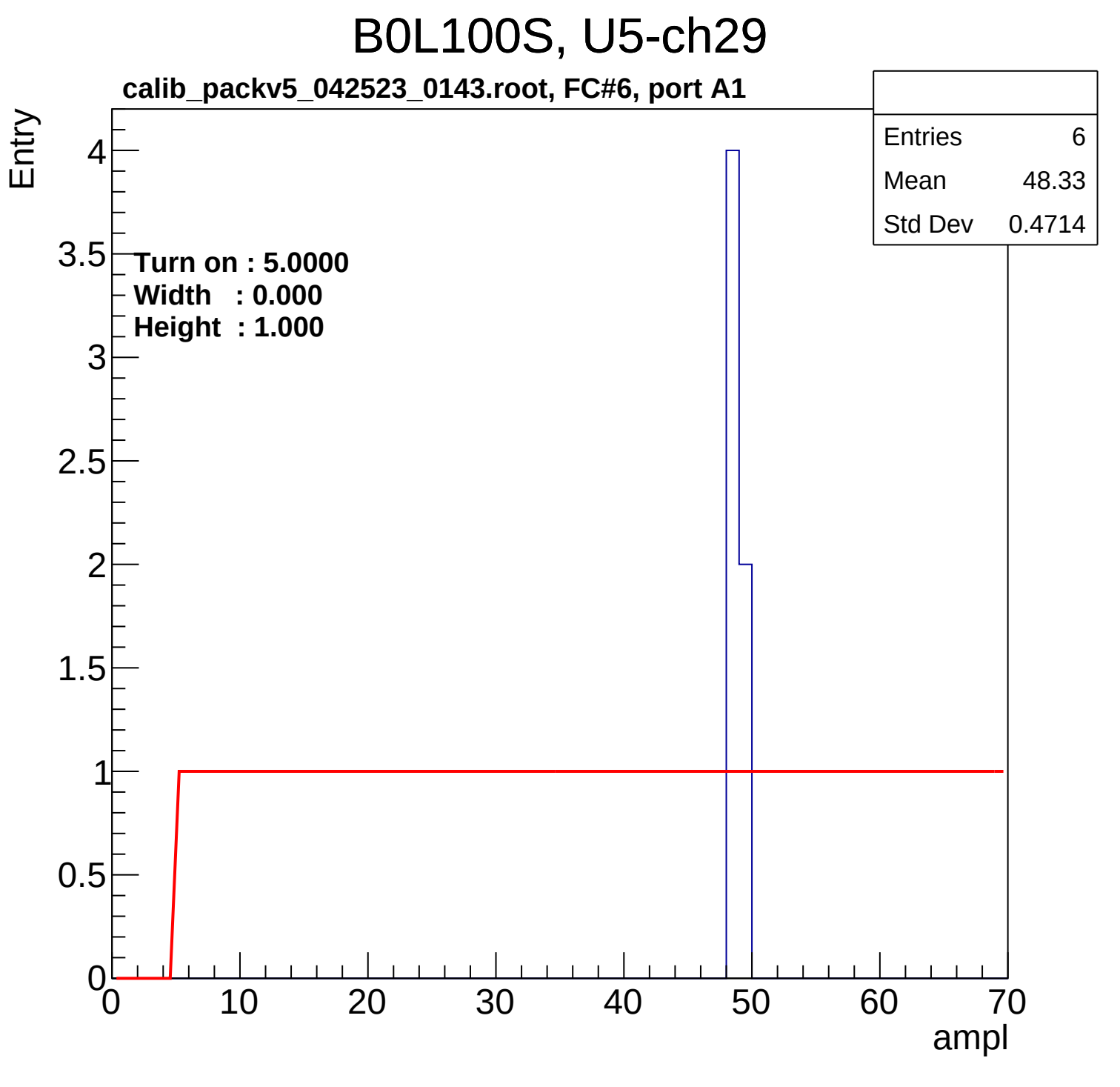

B0L100S, U5-ch24
calib_packv5_042523_0143.root, FC#6, port A1
Entries 37
Mean 45.46
Std Dev 2.467
Turn on : 24.9982
Width : 3.499
Height : 2.000
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

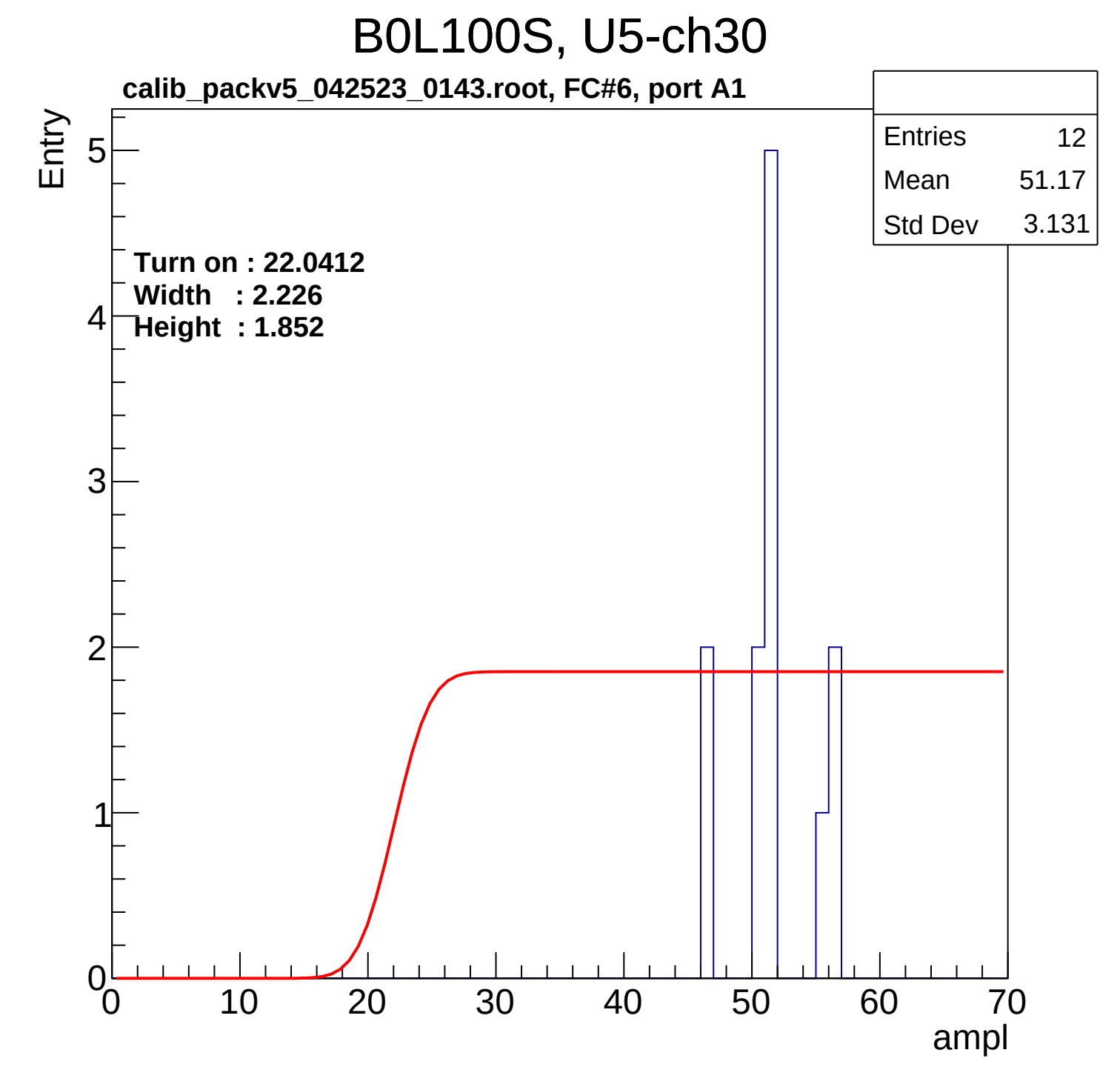

B0L100S, U5-ch25
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

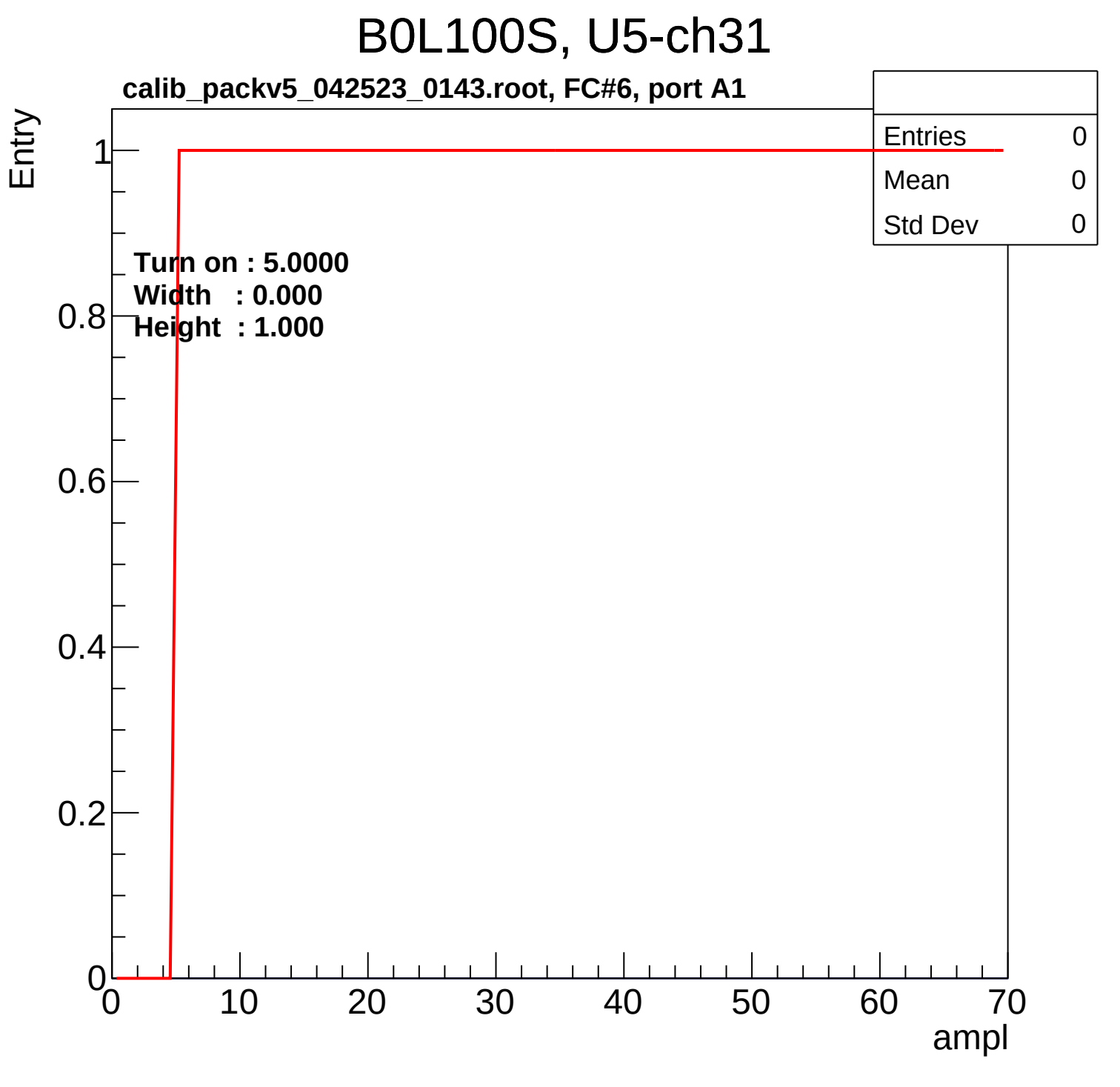

B0L100S, U5-ch26
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

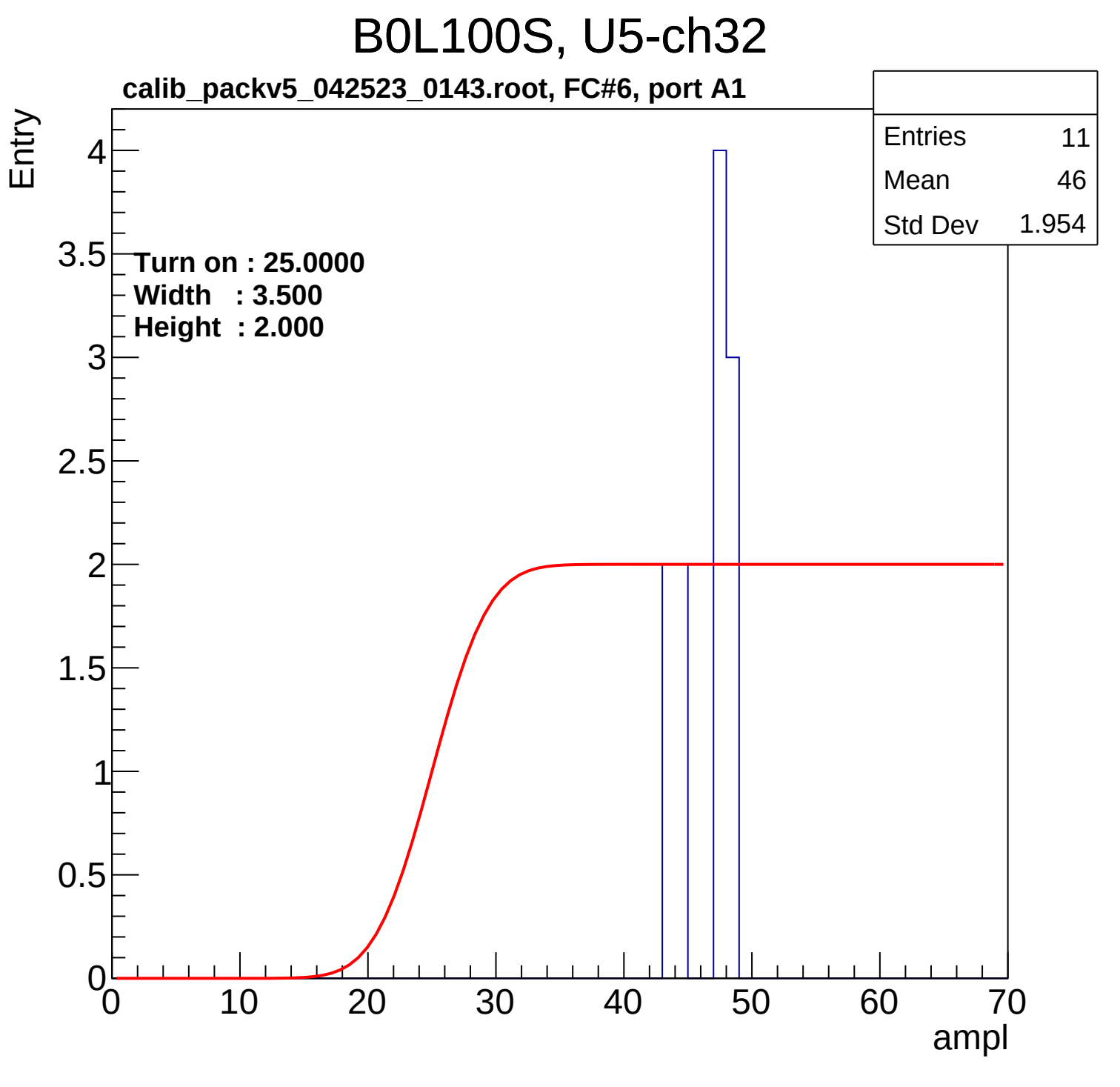

B0L100S, U5-ch27
calib_packv5_042523_0143.root, FC#6, port A1
Entries 9
Mean 45.89
Std Dev 0.737
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

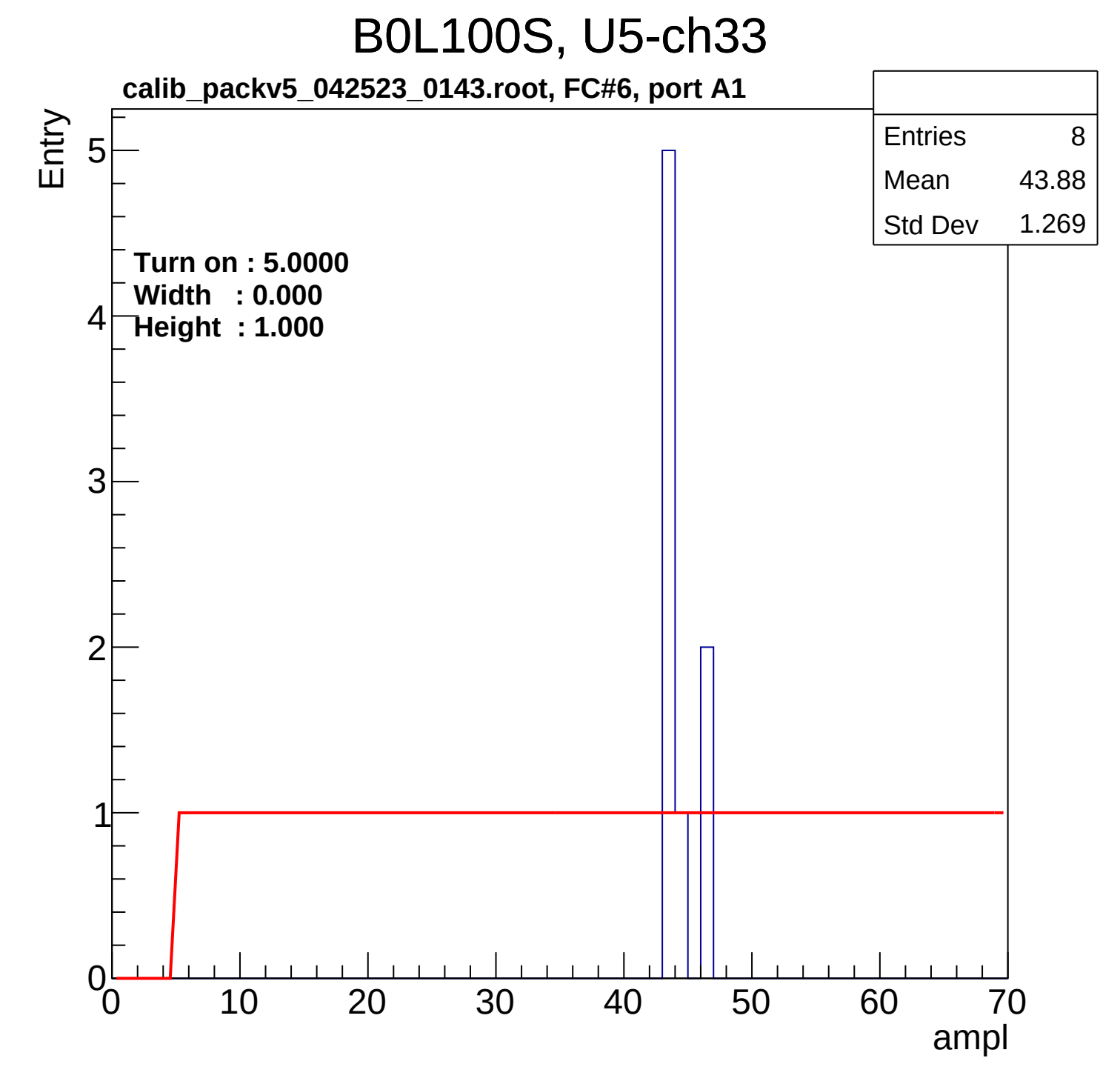

B0L100S, U5-ch28
calib_packv5_042523_0143.root, FC#6, port A1
Entries 31
Mean 49.03
Std Dev 3.137
Turn on : 24.9961
Width : 3.499
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

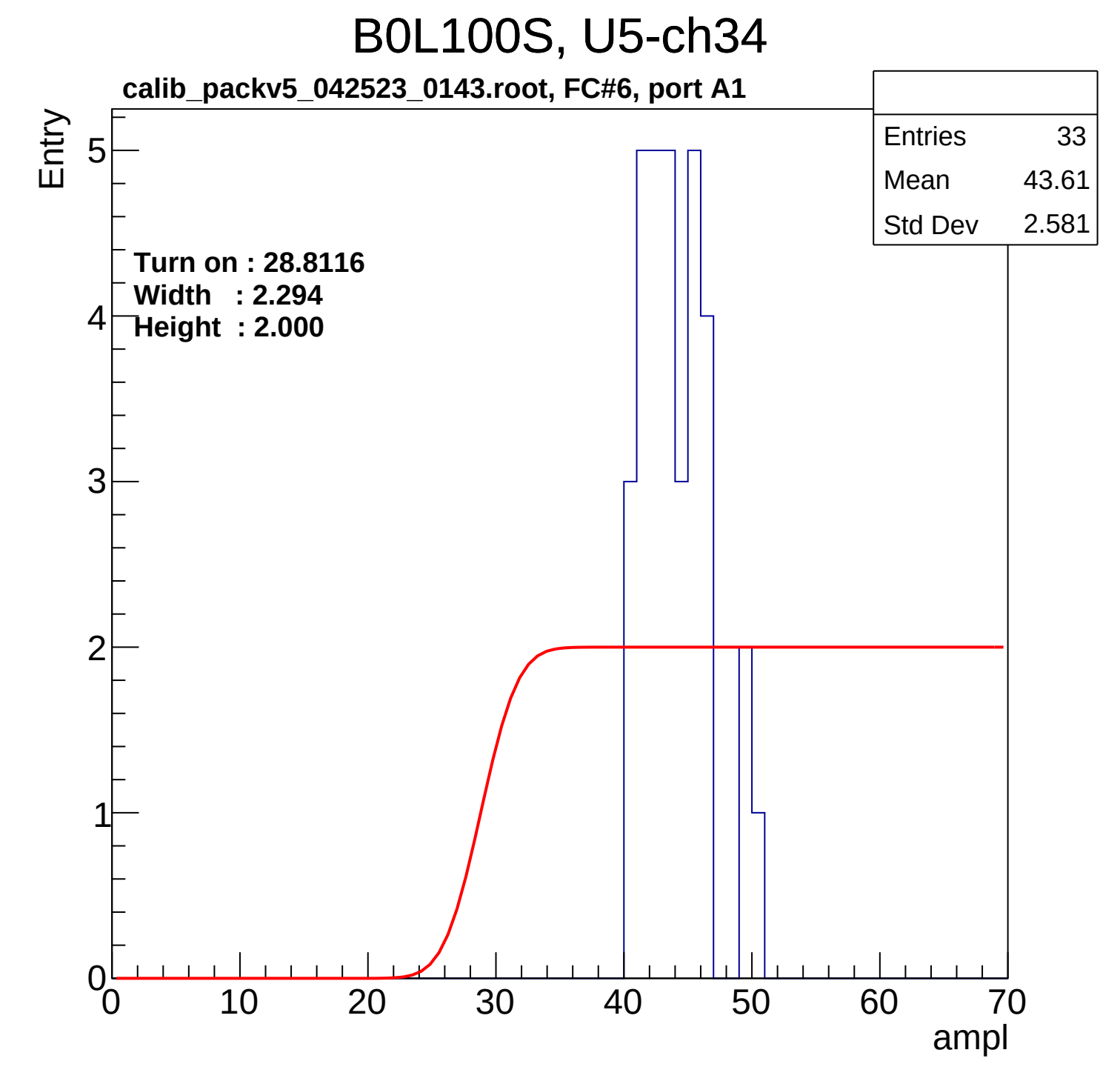

B0L100S, U5-ch29
calib_packv5_042523_0143.root, FC#6, port A1
Entries 6
Mean 48.33
Std Dev 0.4714
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

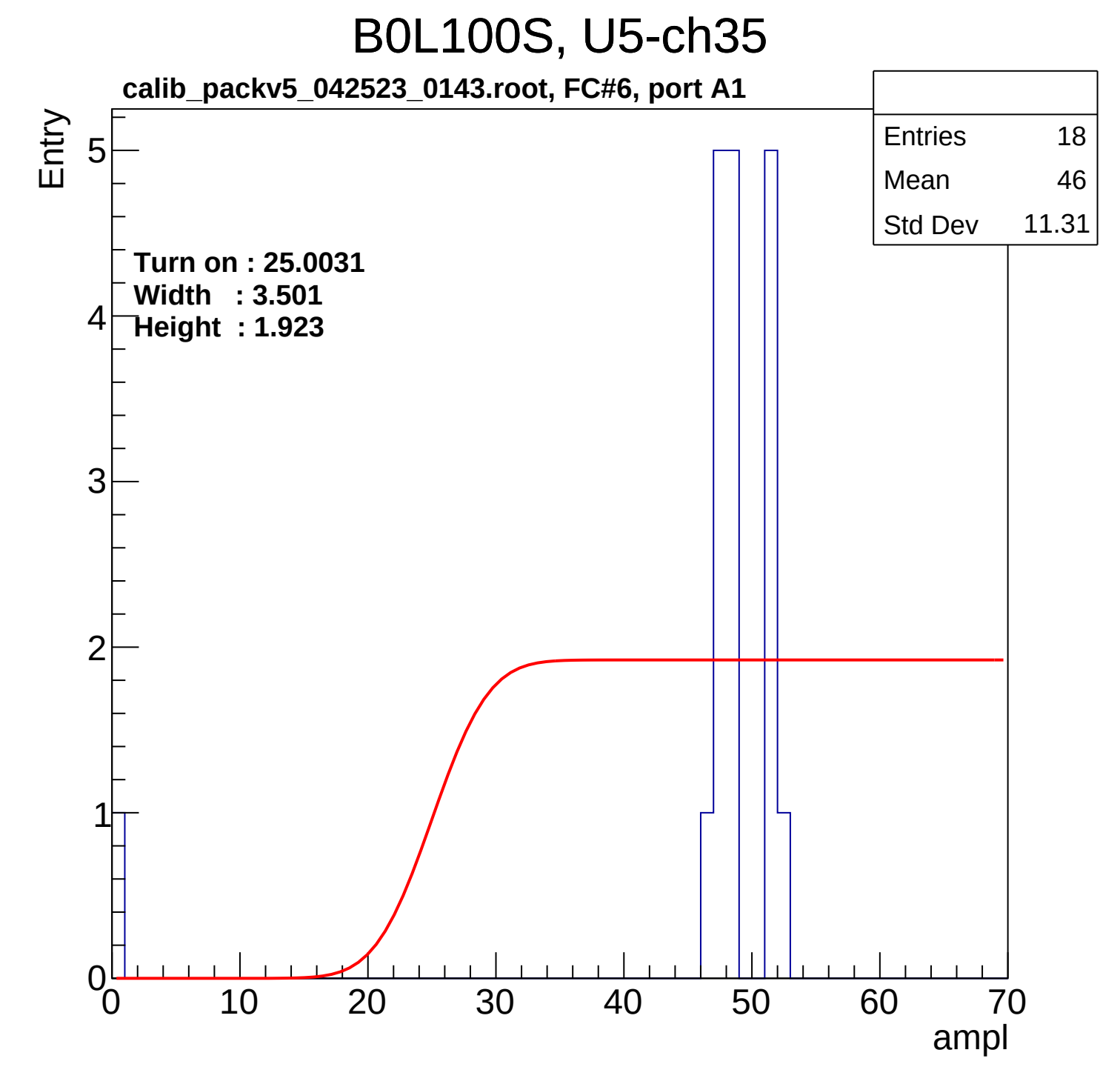

B0L100S, U5-ch30
calib_packv5_042523_0143.root, FC#6, port A1
Entries 12
Mean 51.17
Std Dev 3.131
Turn on : 22.0412
Width : 2.226
Height : 1.852
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

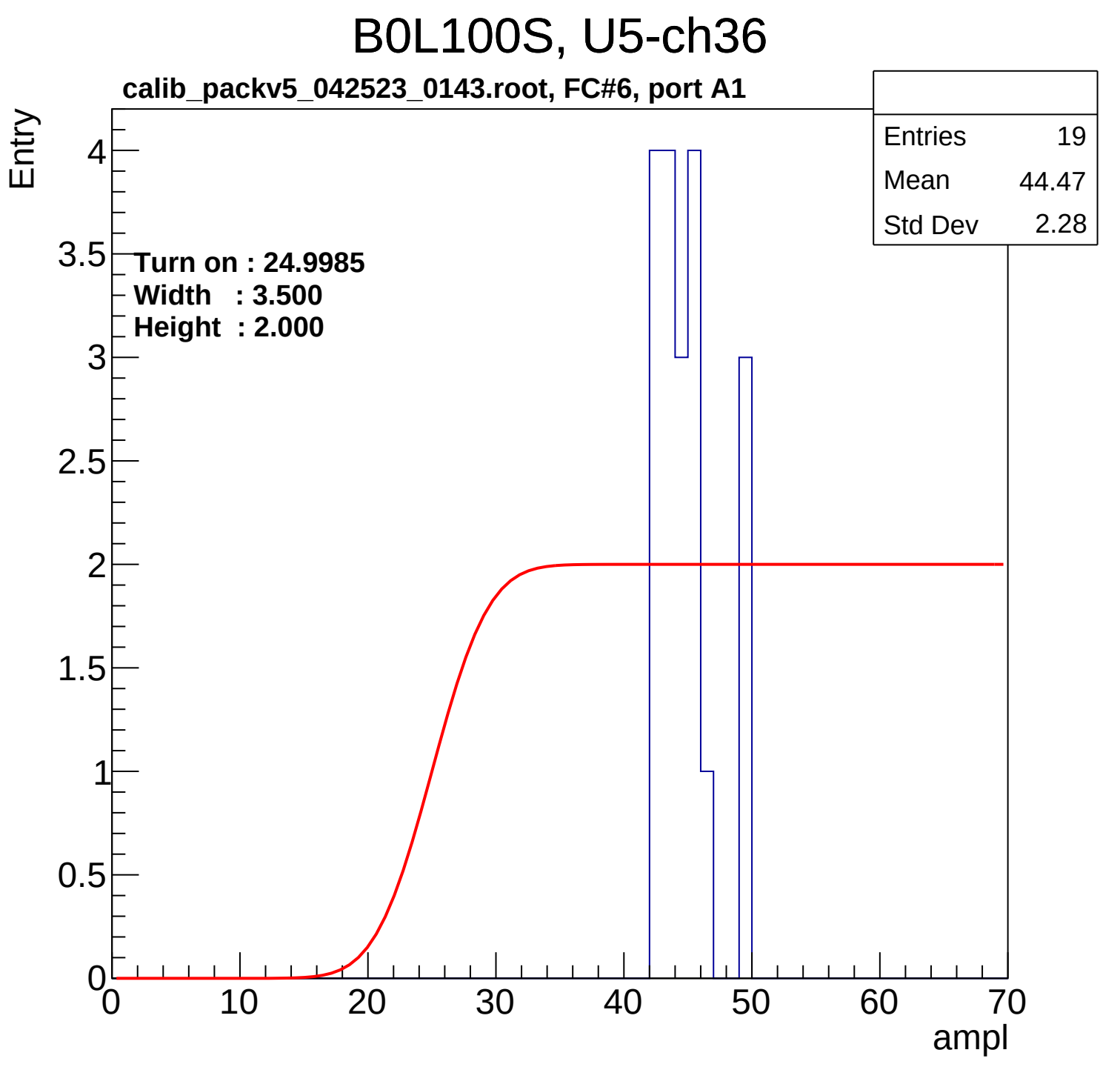

B0L100S, U5-ch31
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

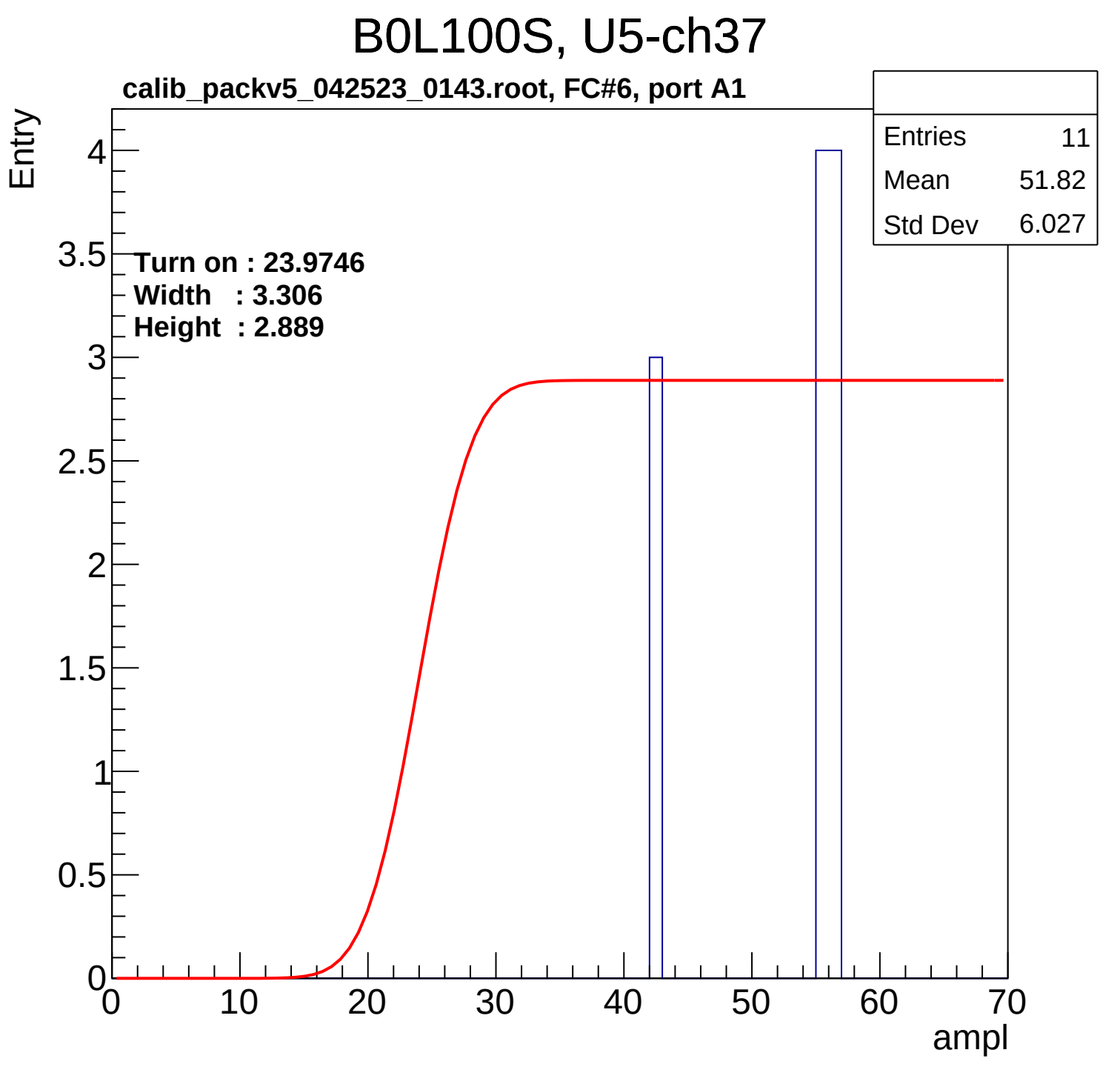

B0L100S, U5-ch32
calib_packv5_042523_0143.root, FC#6, port A1
Entries 11
Mean 46
Std Dev 1.954
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

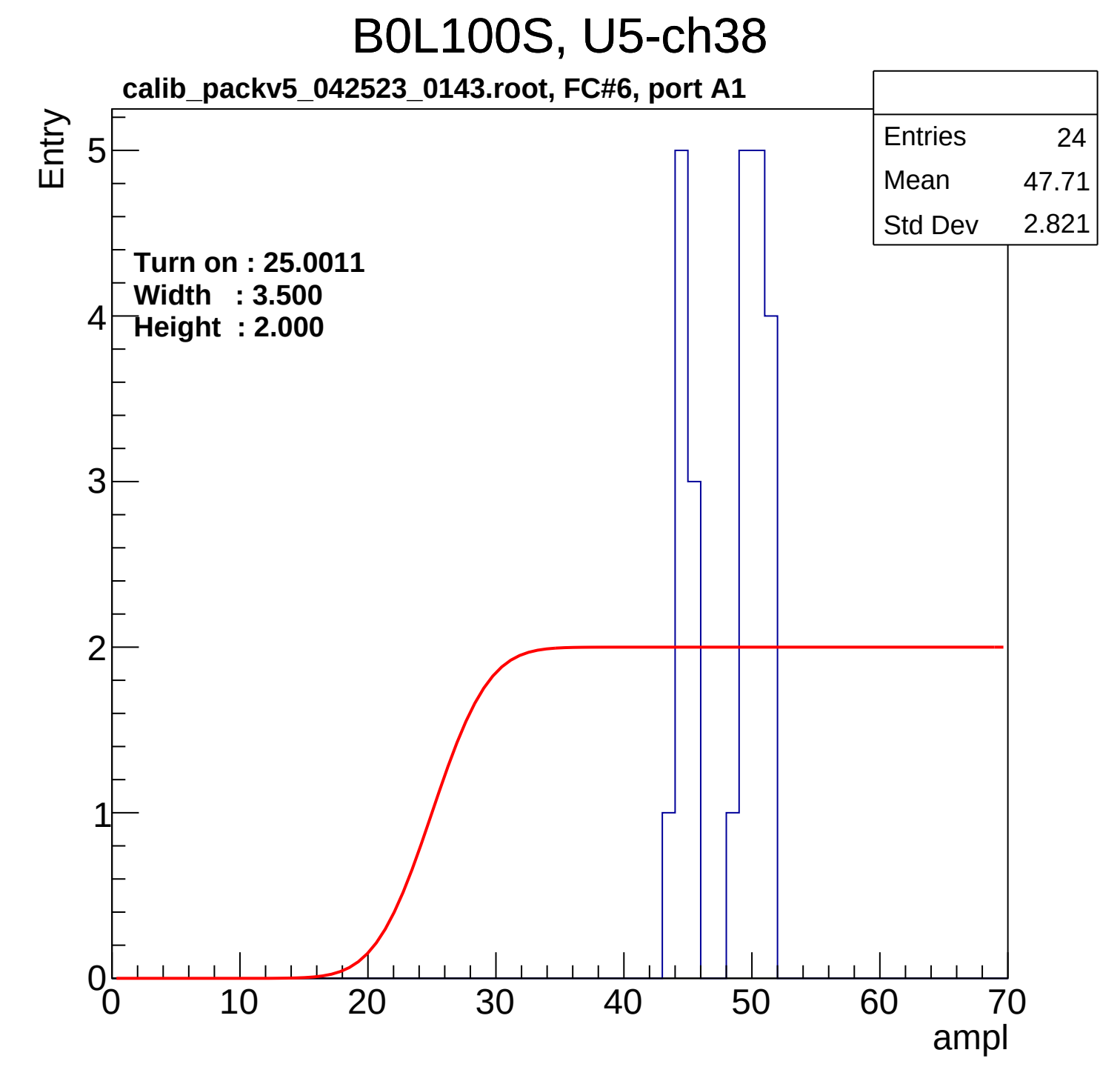

B0L100S, U5-ch33
calib_packv5_042523_0143.root, FC#6, port A1
Entries 8
Mean 43.88
Std Dev 1.269
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

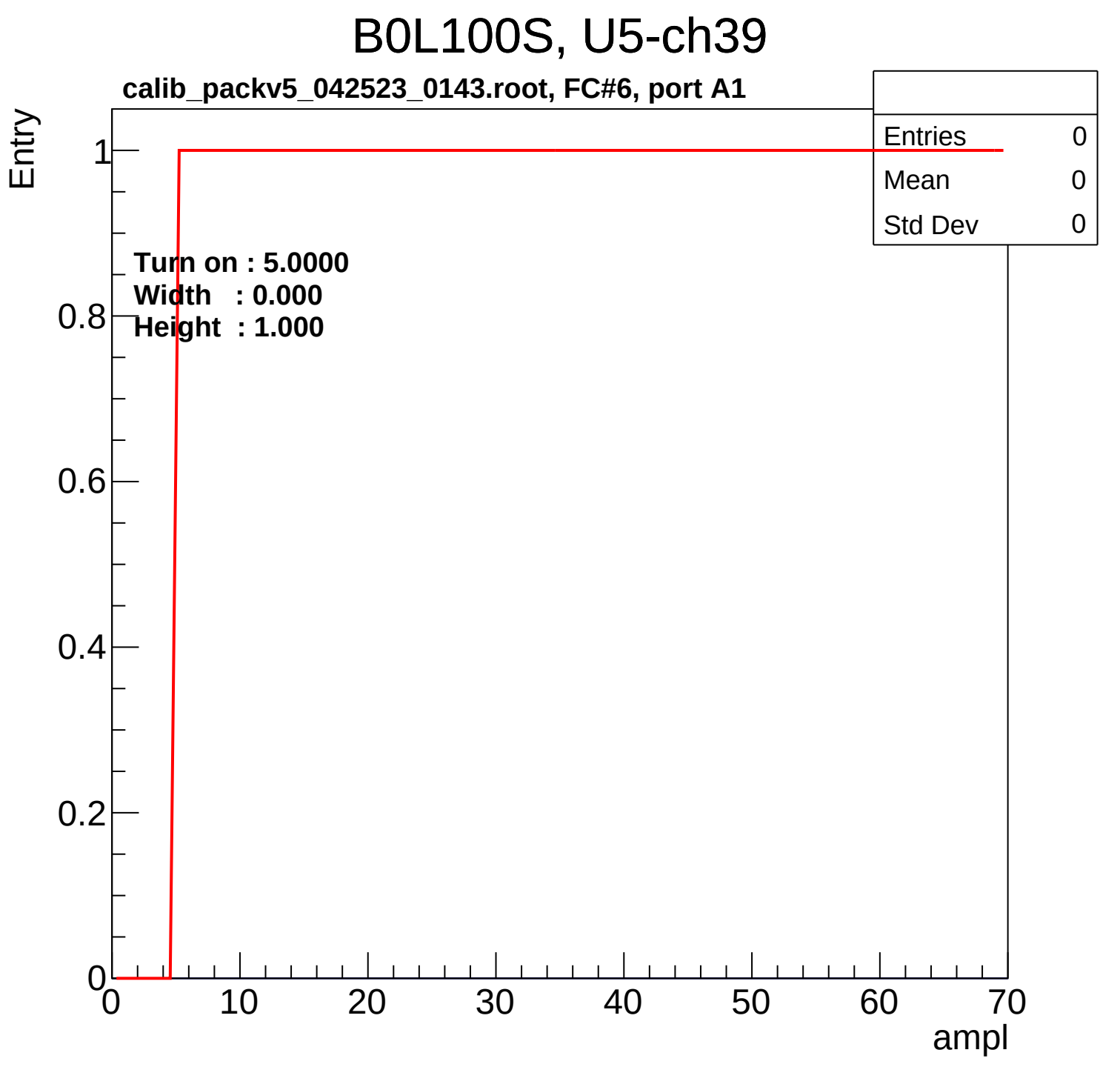

B0L100S, U5-ch34
calib_packv5_042523_0143.root, FC#6, port A1
Entries 33
Mean 43.61
Std Dev 2.581
Turn on : 28.8116
Width : 2.294
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

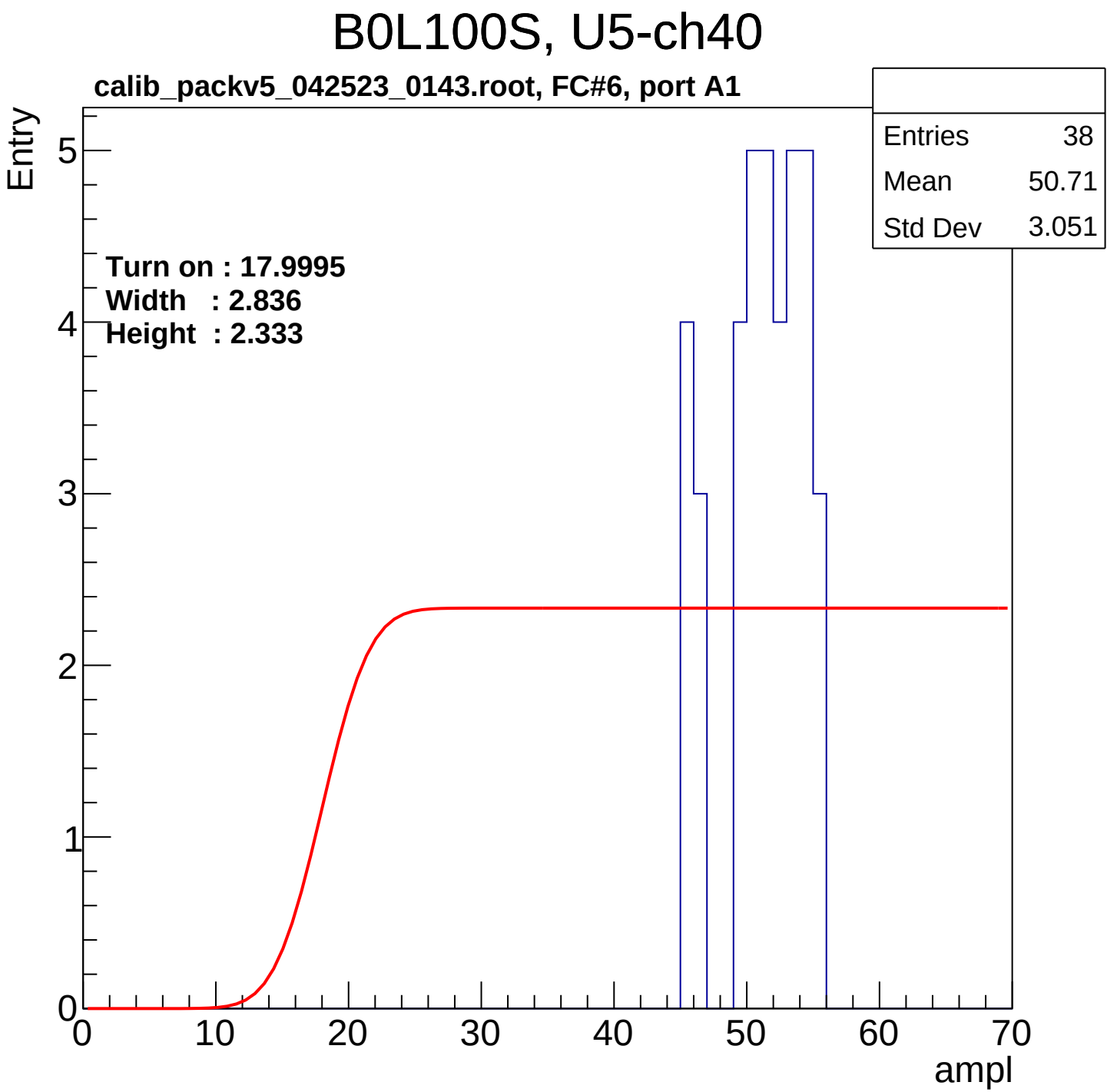

B0L100S, U5-ch35
calib_packv5_042523_0143.root, FC#6, port A1
Entries 18
Mean 46
Std Dev 11.31
Turn on : 25.0031
Width : 3.501
Height : 1.923
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

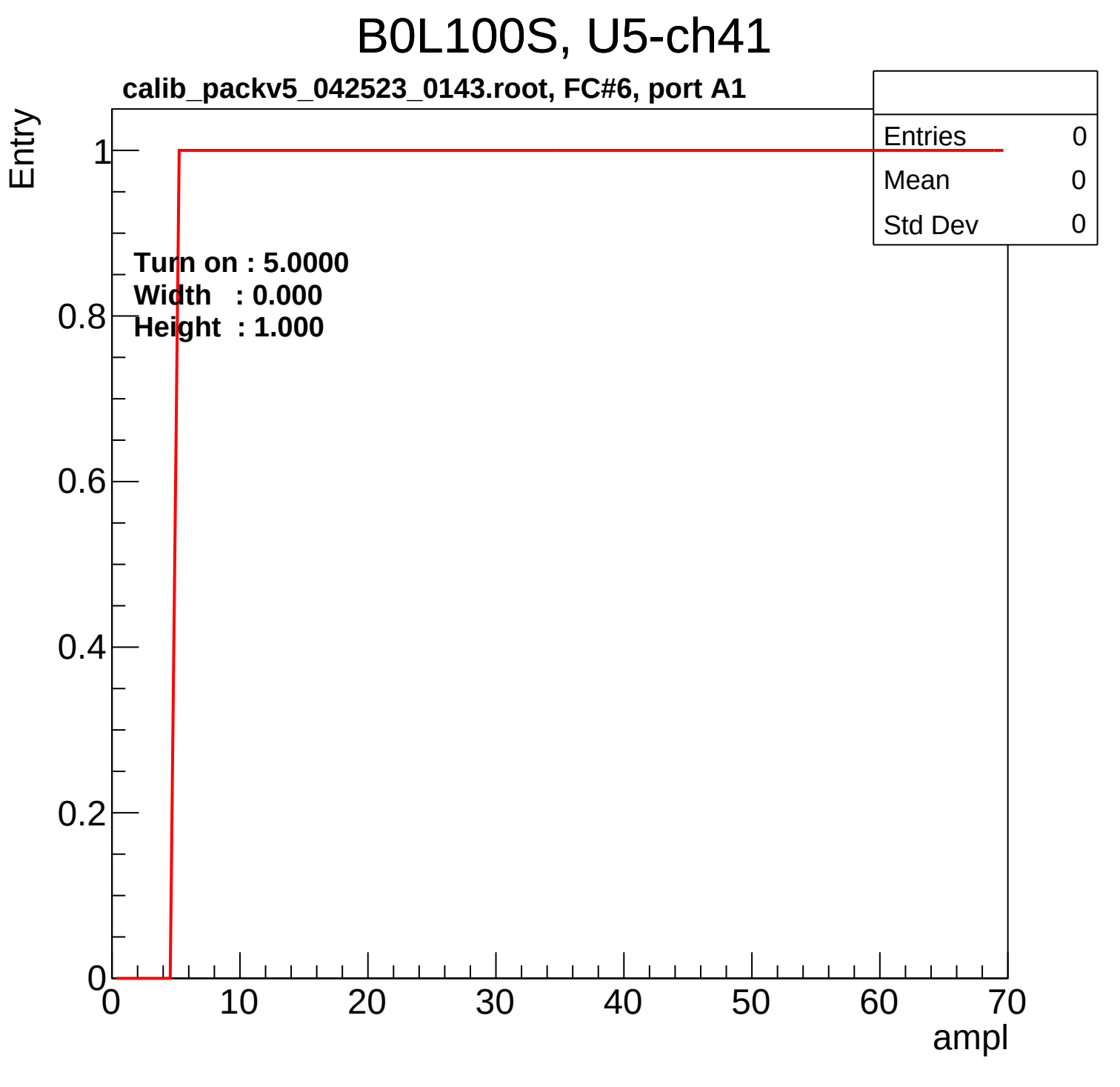

B0L100S, U5-ch36
calib_packv5_042523_0143.root, FC#6, port A1
Entries 19
Mean 44.47
Std Dev 2.28
Turn on : 24.9985
Width : 3.500
Height : 2.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

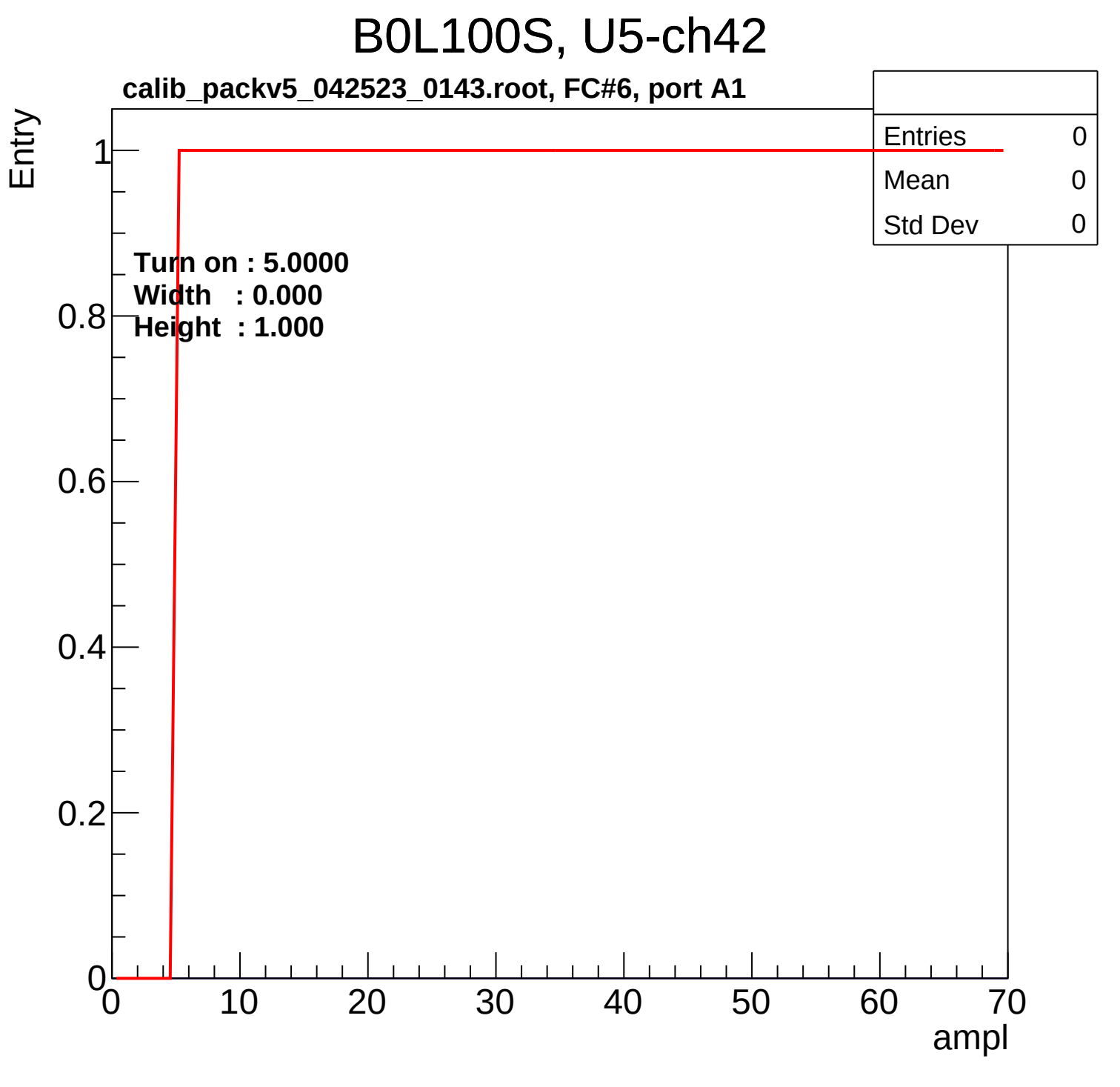

B0L100S, U5-ch37
calib_packv5_042523_0143.root, FC#6, port A1
Entries 11
Mean 51.82
Std Dev 6.027
Turn on : 23.9746
Width : 3.306
Height : 2.889
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

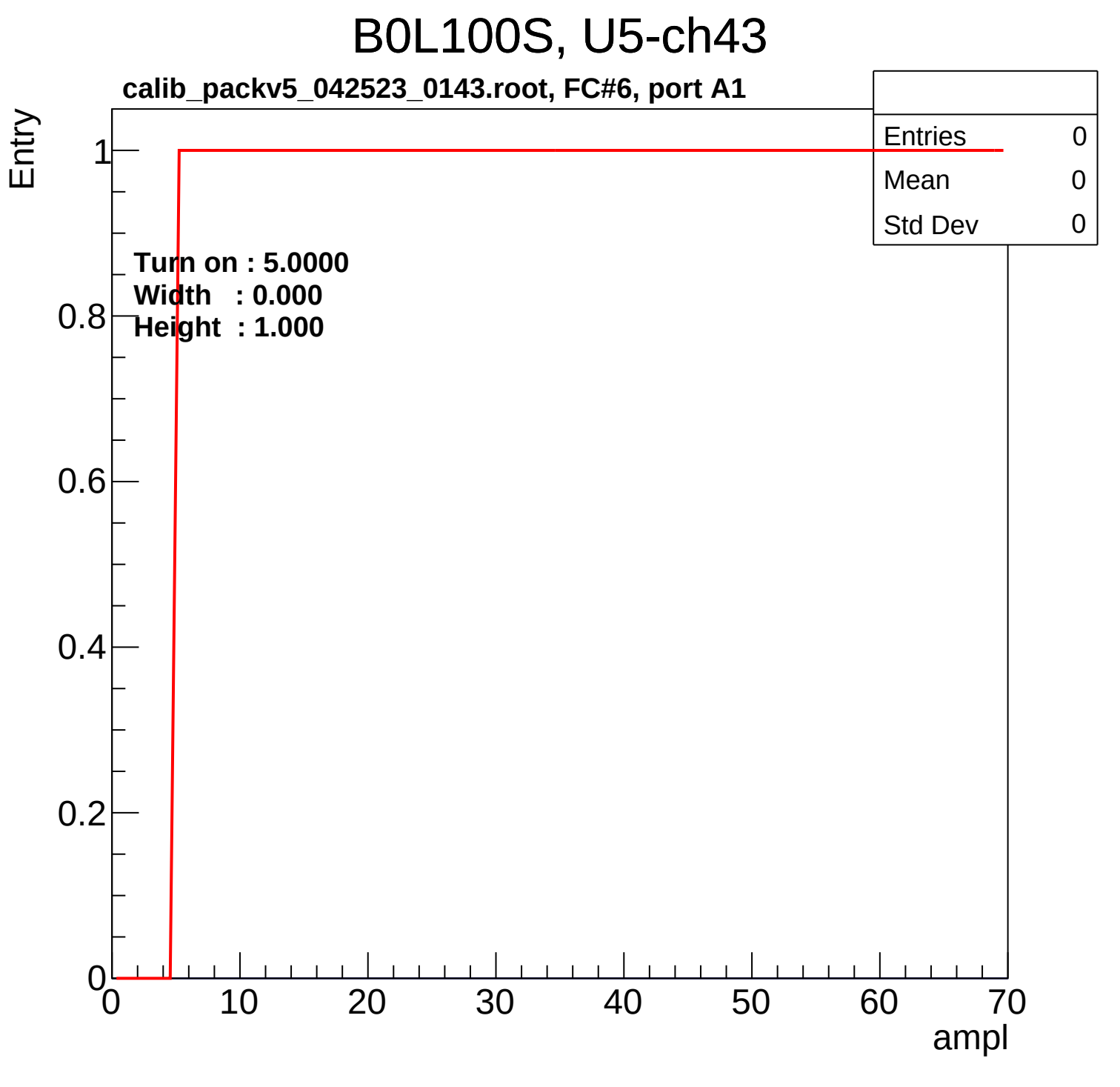

B0L100S, U5-ch38
calib_packv5_042523_0143.root, FC#6, port A1
Entries 24
Mean 47.71
Std Dev 2.821
Turn on : 25.0011
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

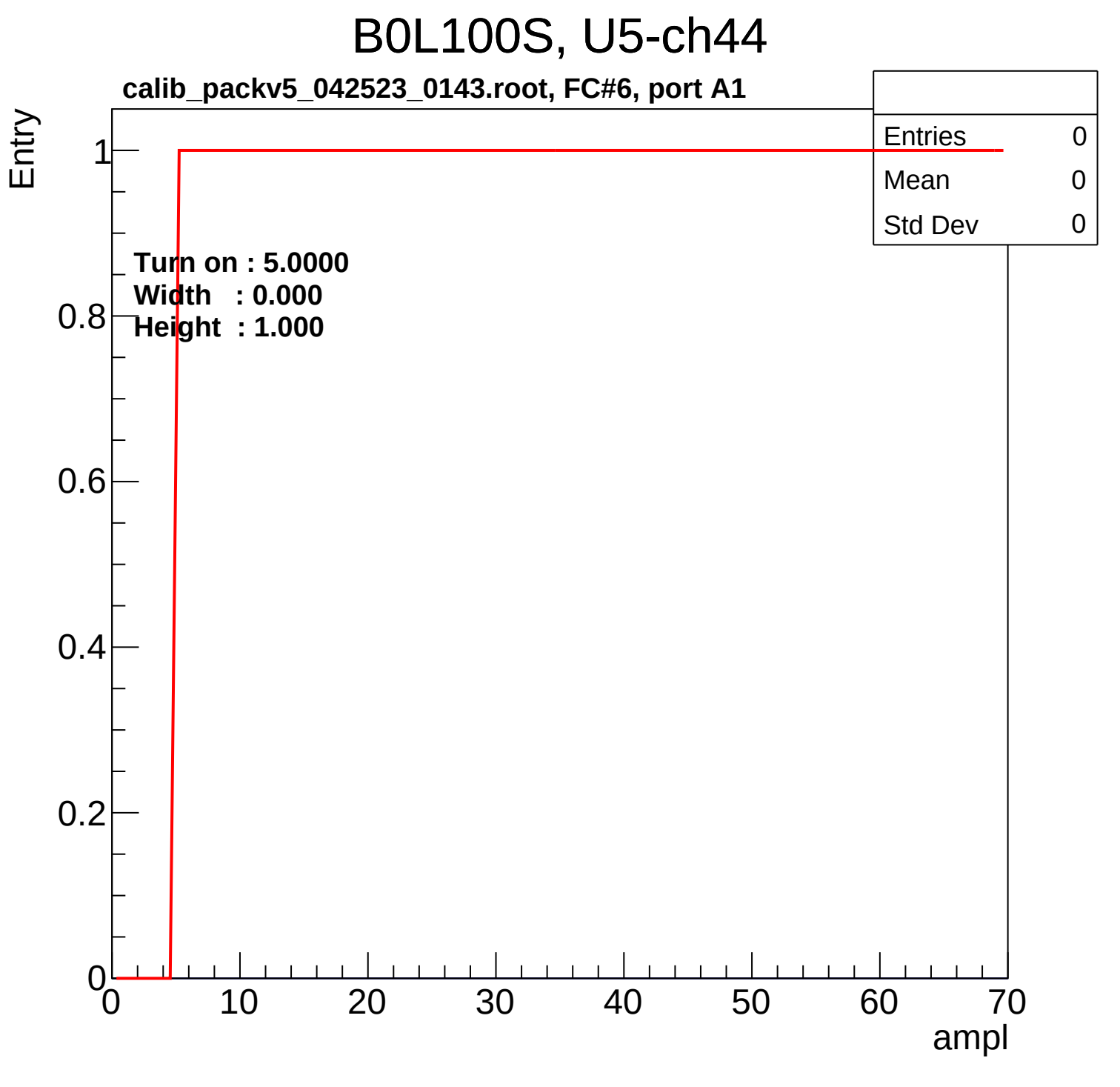

B0L100S, U5-ch39
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

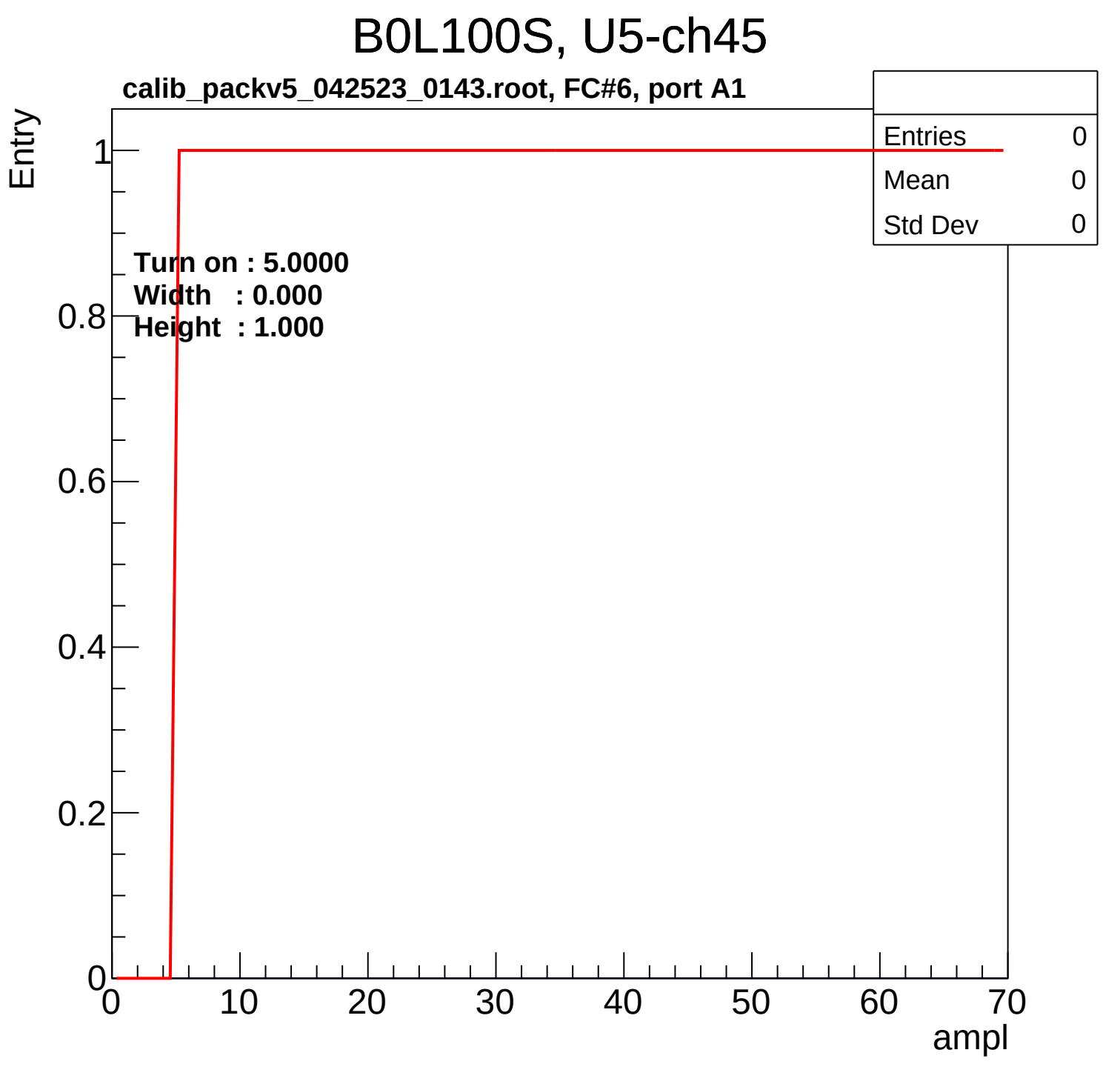

B0L100S, U5-ch40
calib_packv5_042523_0143.root, FC#6, port A1
Entries 38
Mean 50.71
Std Dev 3.051
Turn on : 17.9995
Width : 2.836
Height : 2.333
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

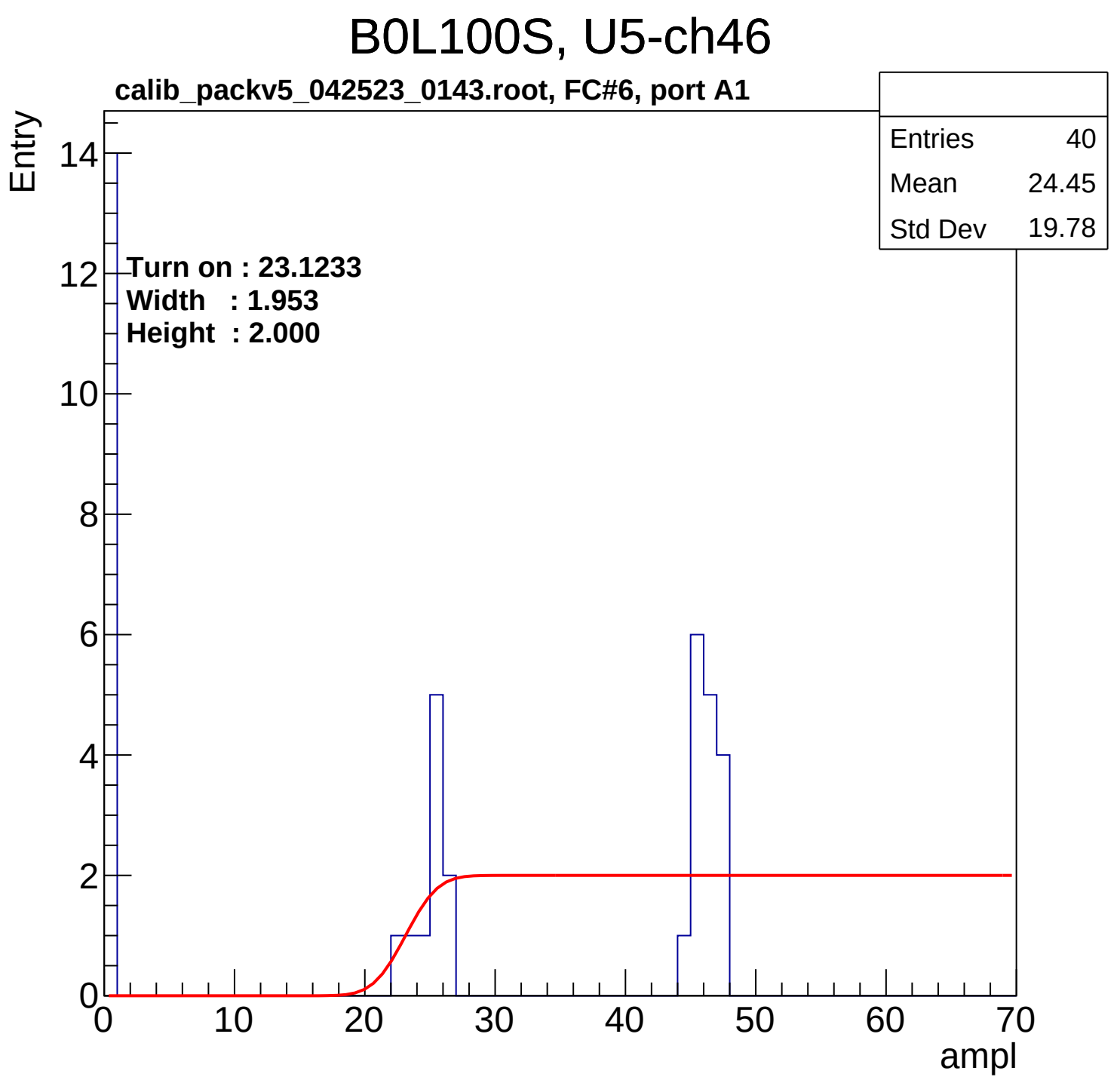

B0L100S, U5-ch41
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

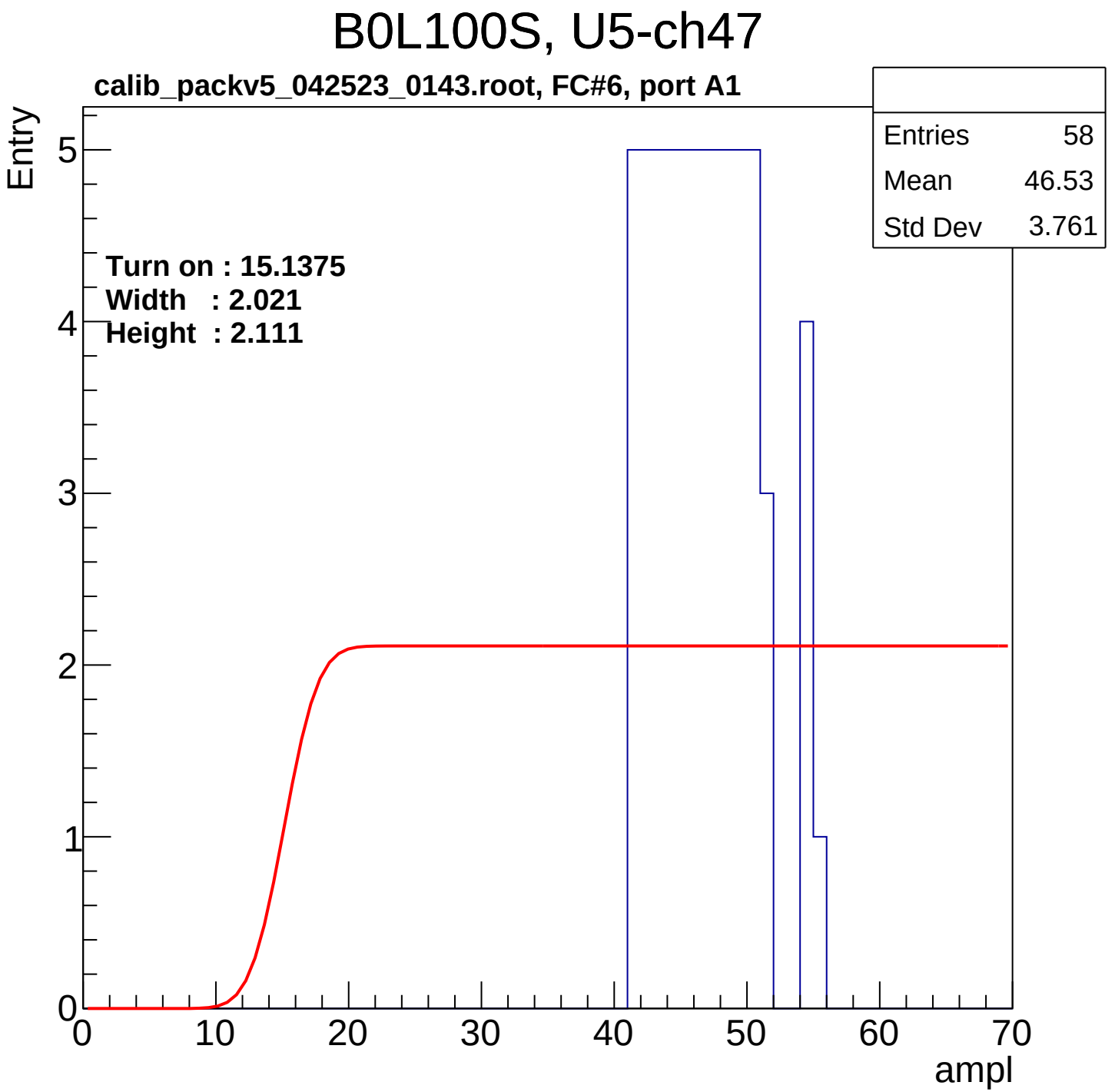

B0L100S, U5-ch42
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

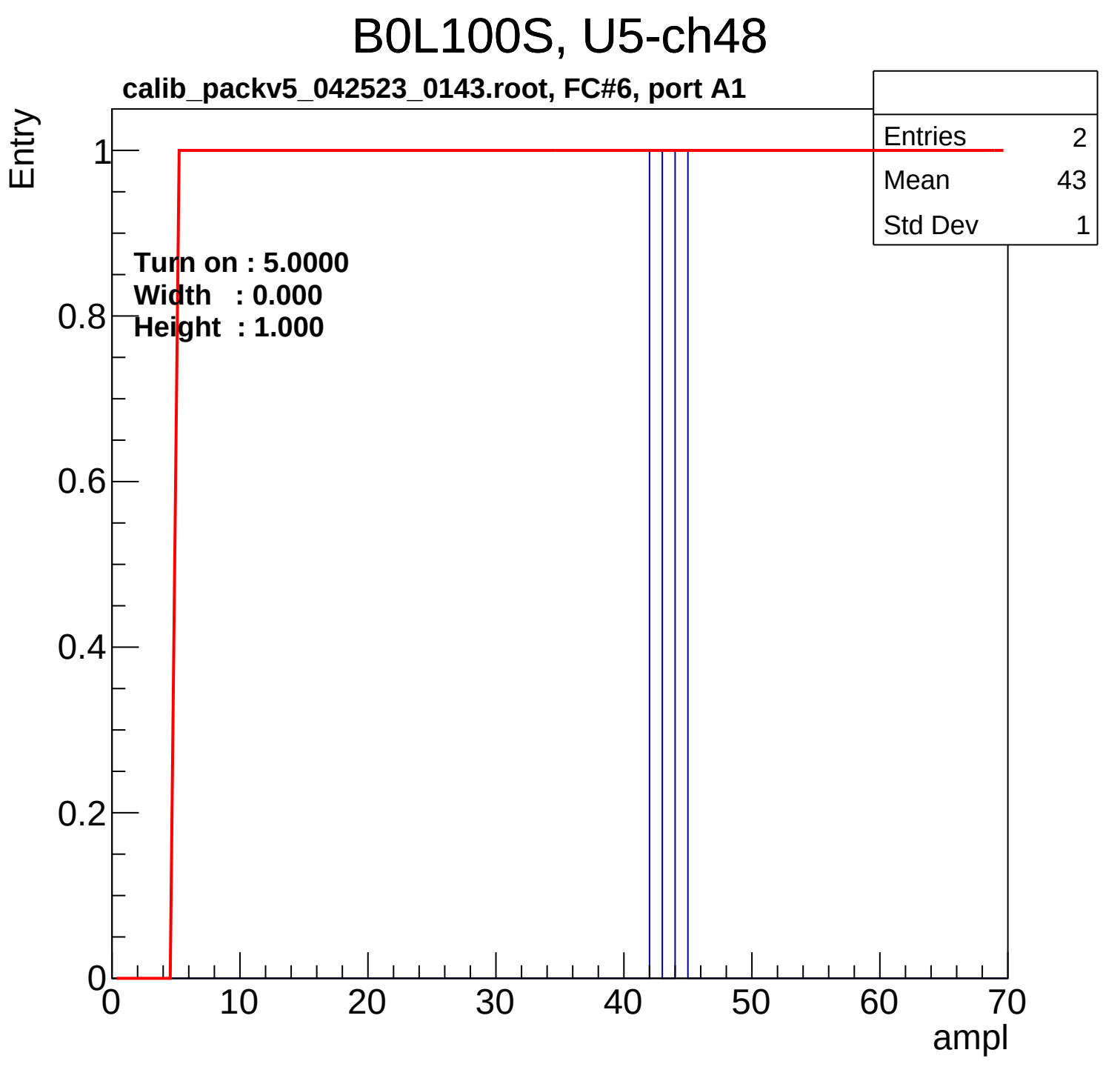

B0L100S, U5-ch43
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

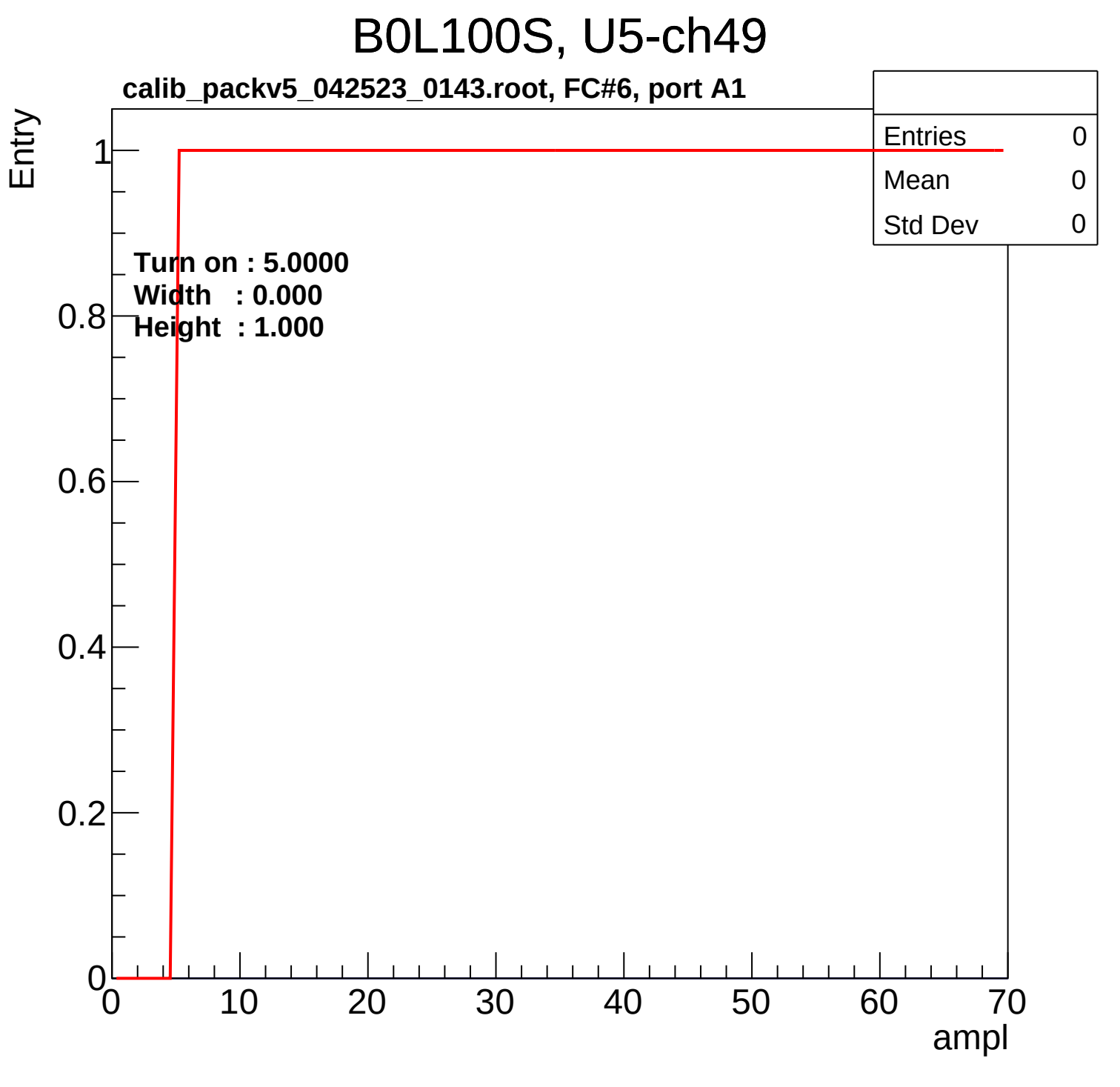

B0L100S, U5-ch44
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

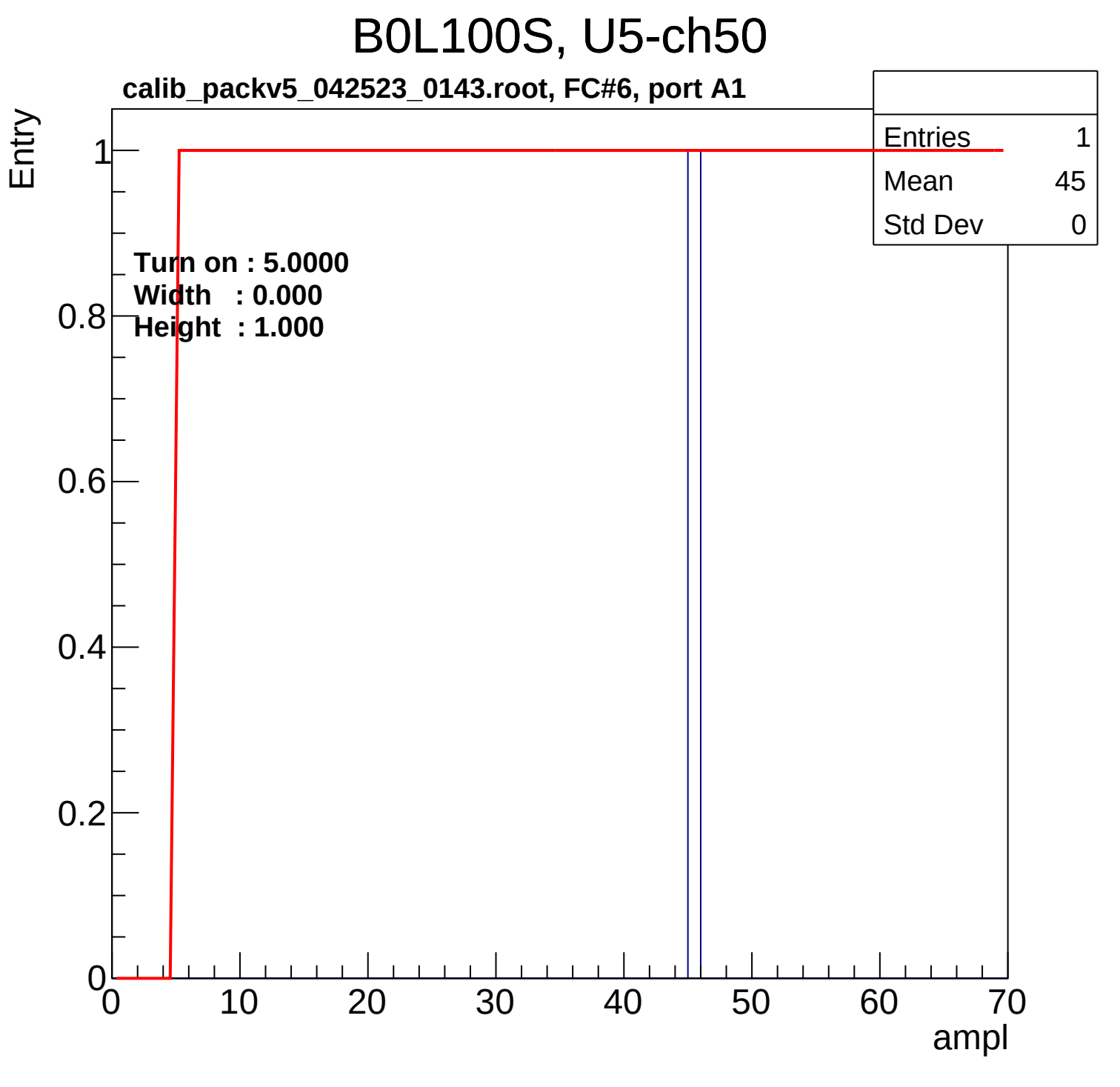

B0L100S, U5-ch45
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

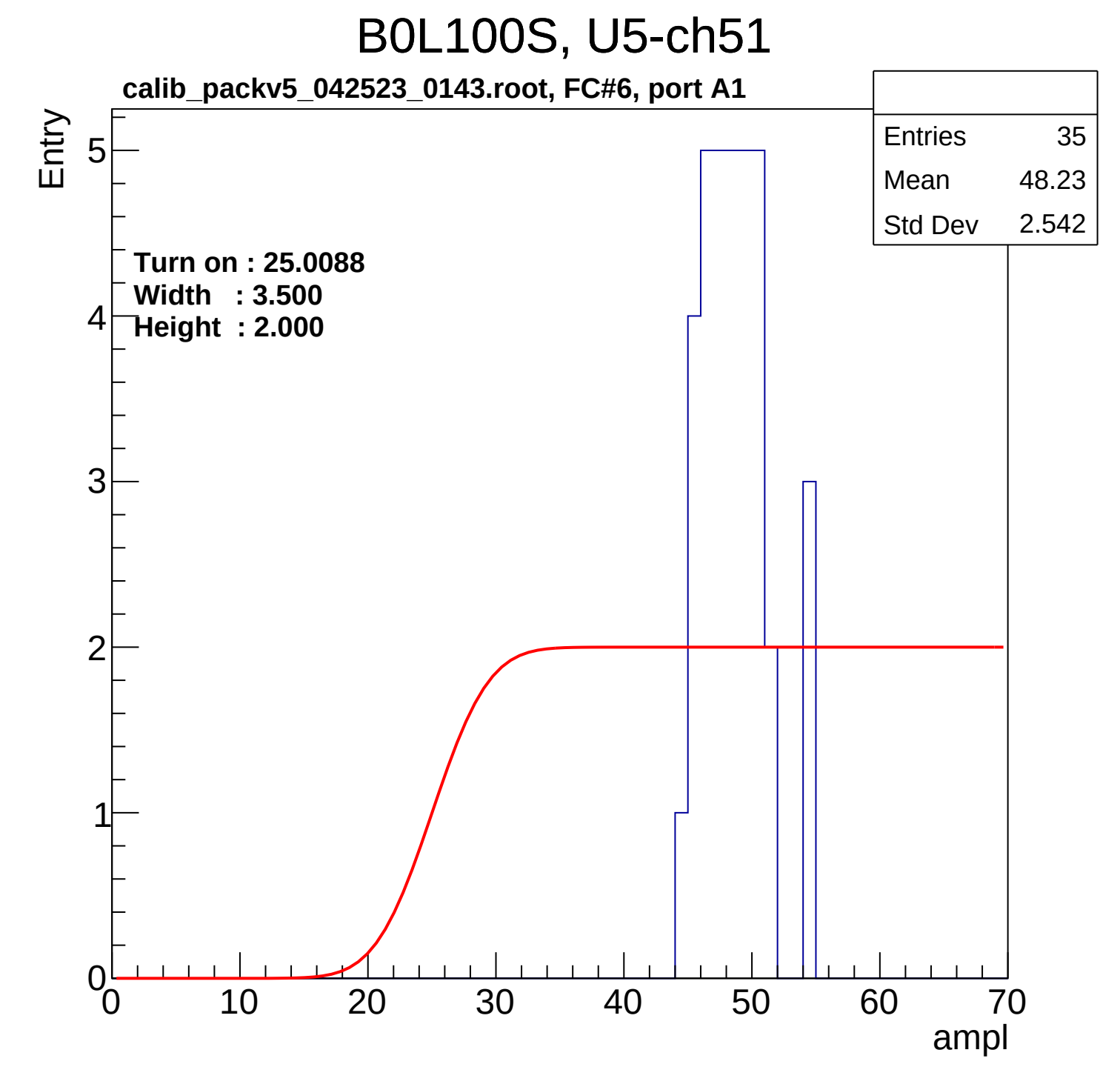

B0L100S, U5-ch46
calib_packv5_042523_0143.root, FC#6, port A1
Entries 40
Mean 24.45
Std Dev 19.78
Turn on : 23.1233
Width : 1.953
Height : 2.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

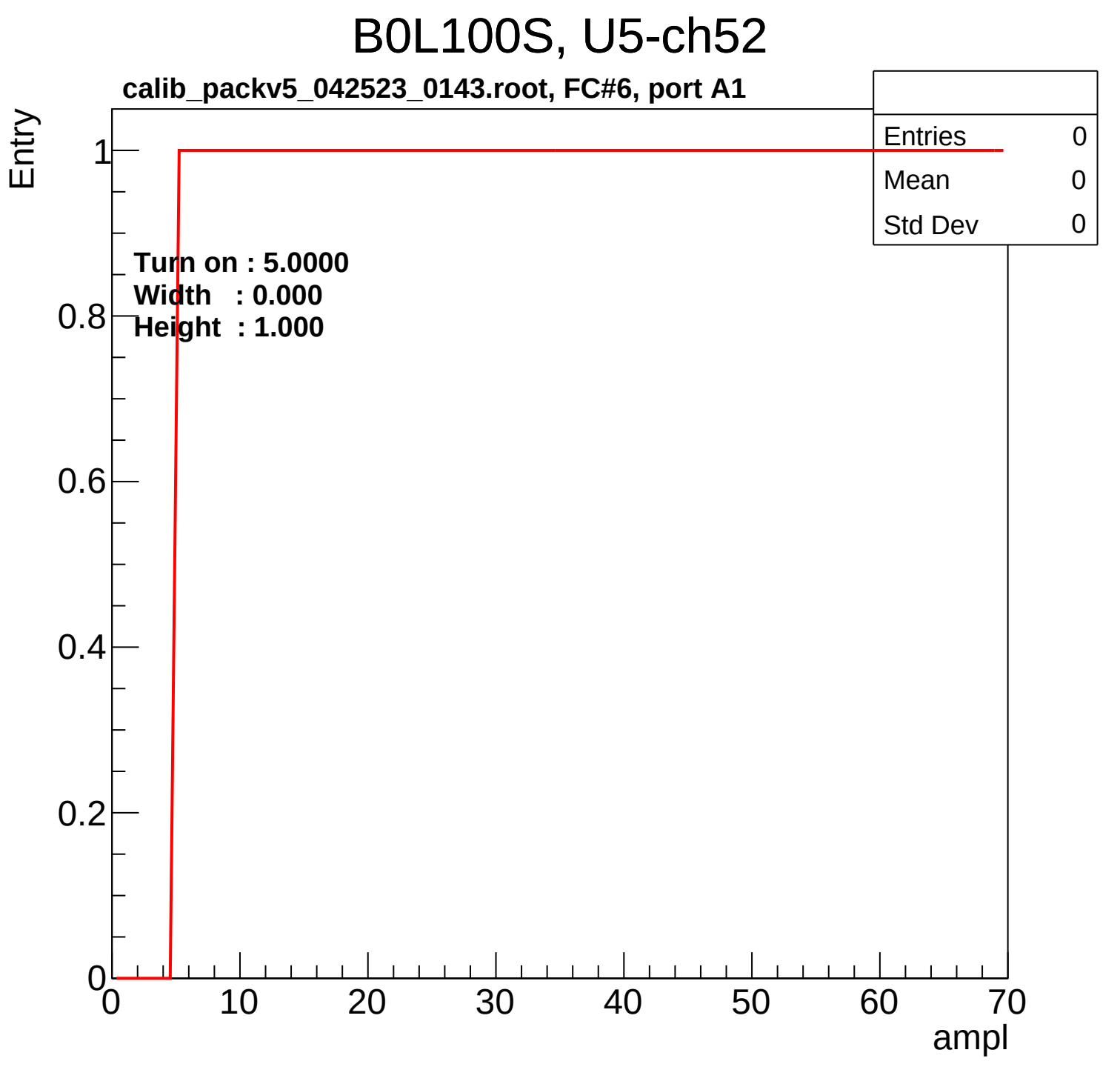

B0L100S, U5-ch47
calib_packv5_042523_0143.root, FC#6, port A1
Entries 58
Mean 46.53
Std Dev 3.761
Turn on : 15.1375
Width : 2.021
Height : 2.111
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

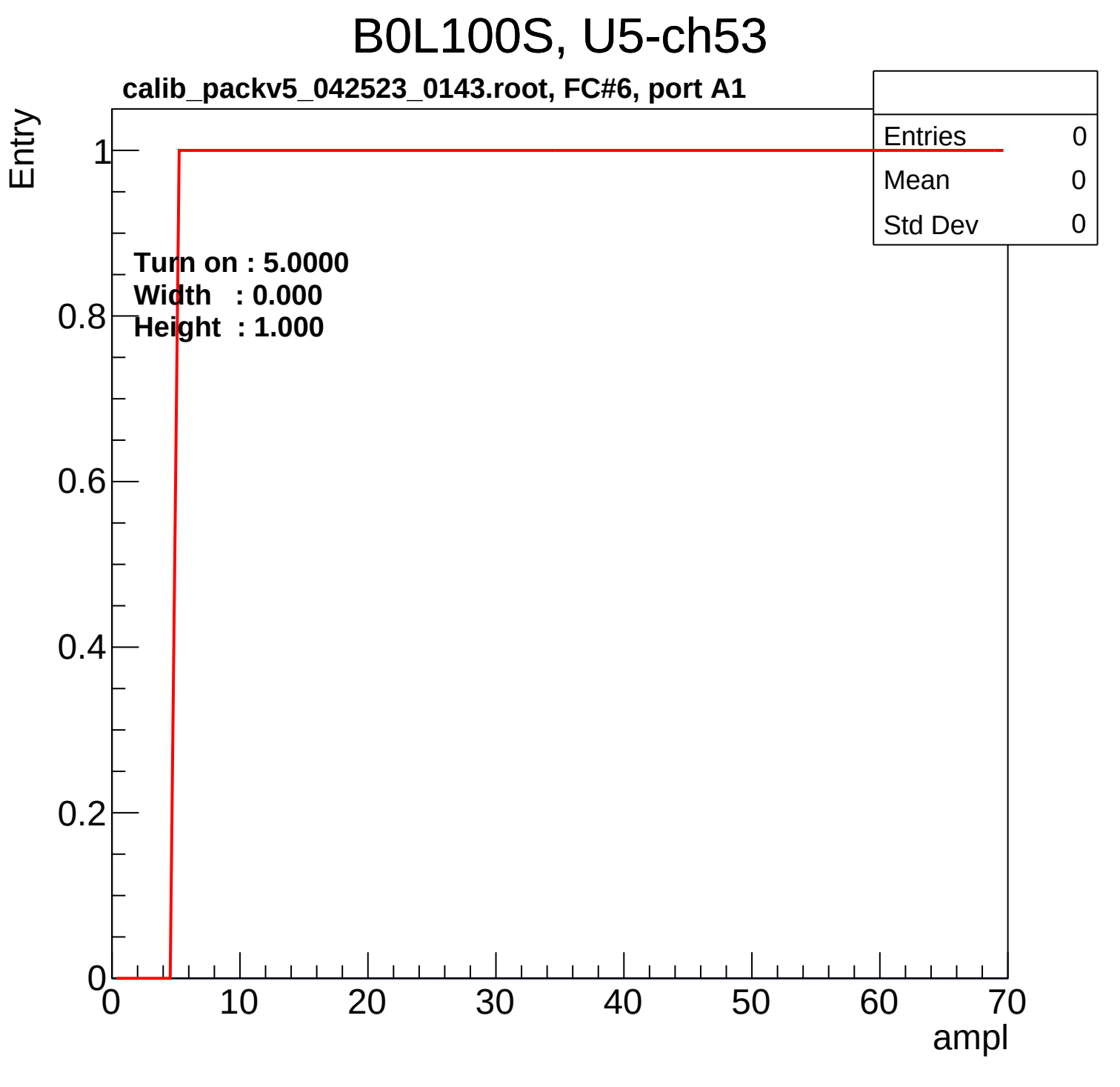

B0L100S, U5-ch48
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 43
Std Dev 1
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

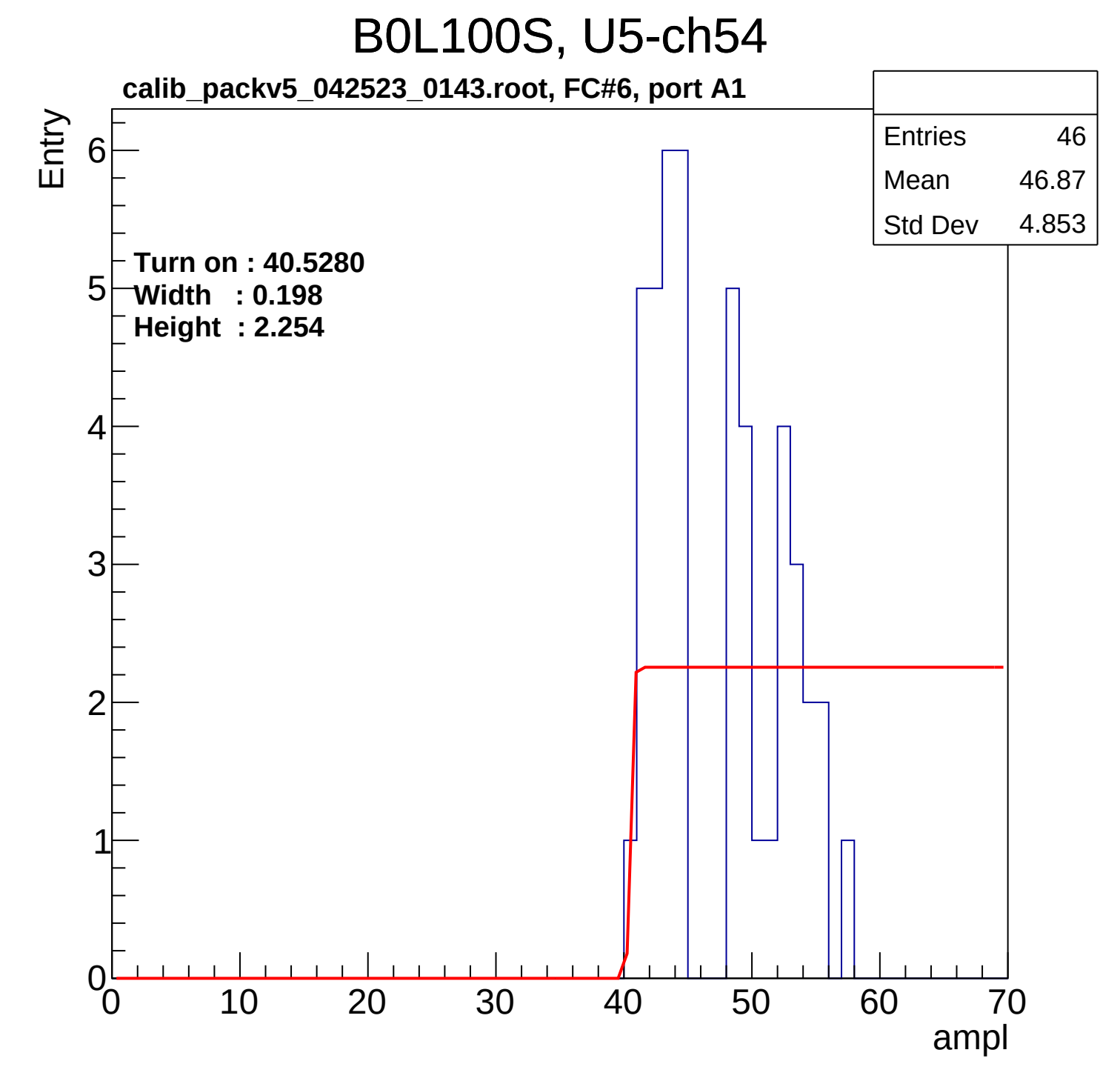

B0L100S, U5-ch49
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

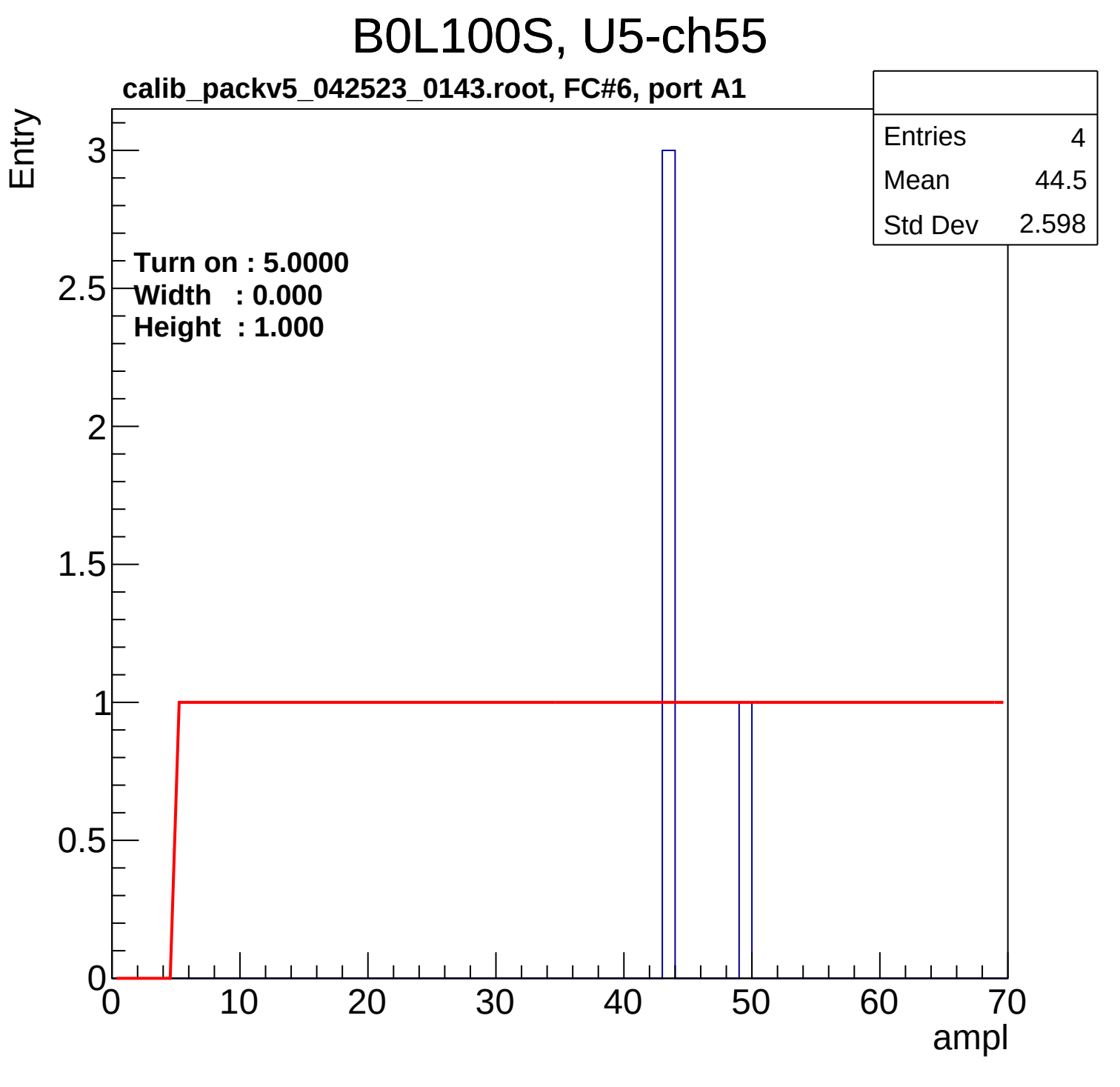

B0L100S, U5-ch50
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 45
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

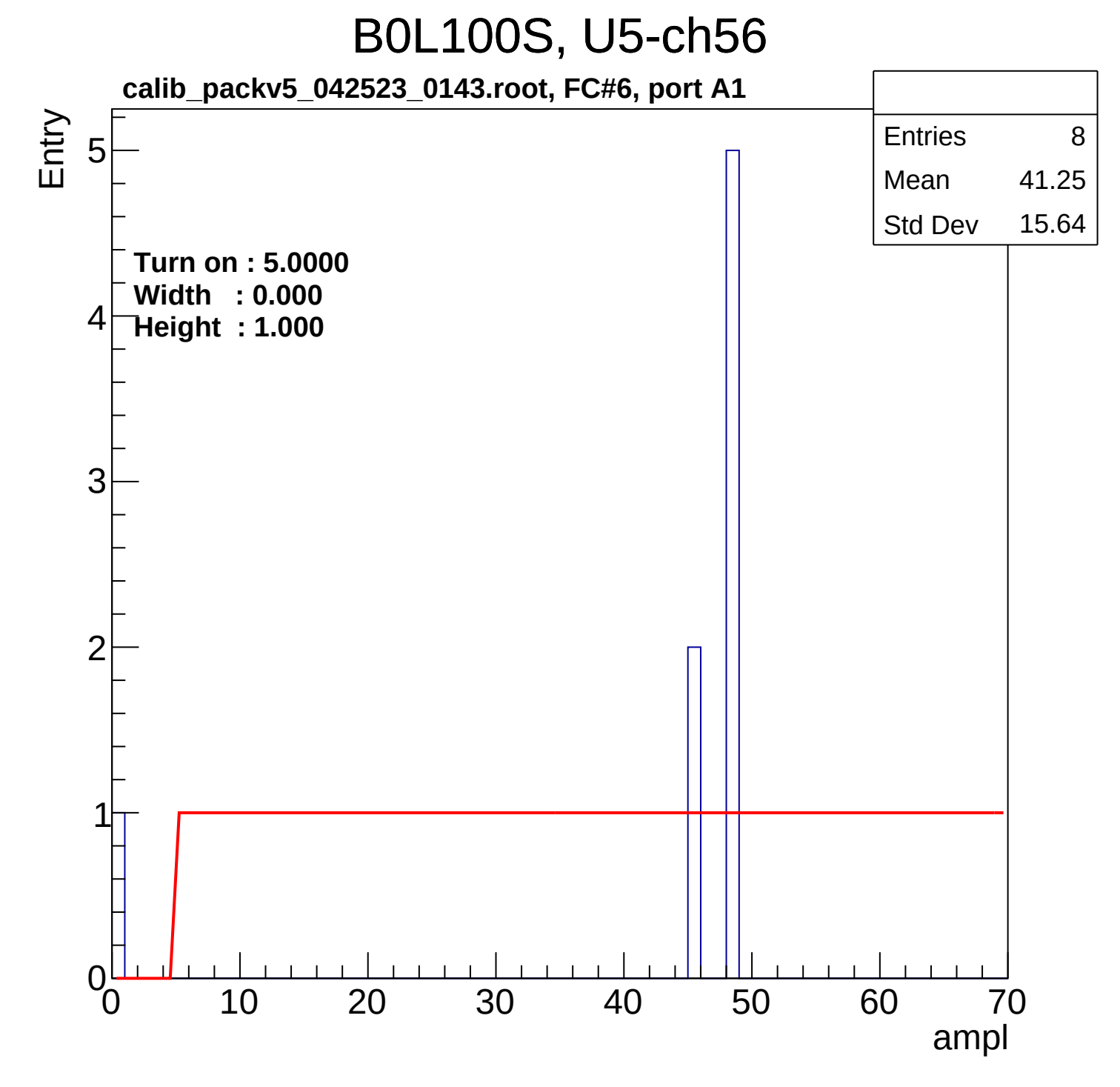

B0L100S, U5-ch51
calib_packv5_042523_0143.root, FC#6, port A1
Entries 35
Mean 48.23
Std Dev 2.542
Turn on : 25.0088
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

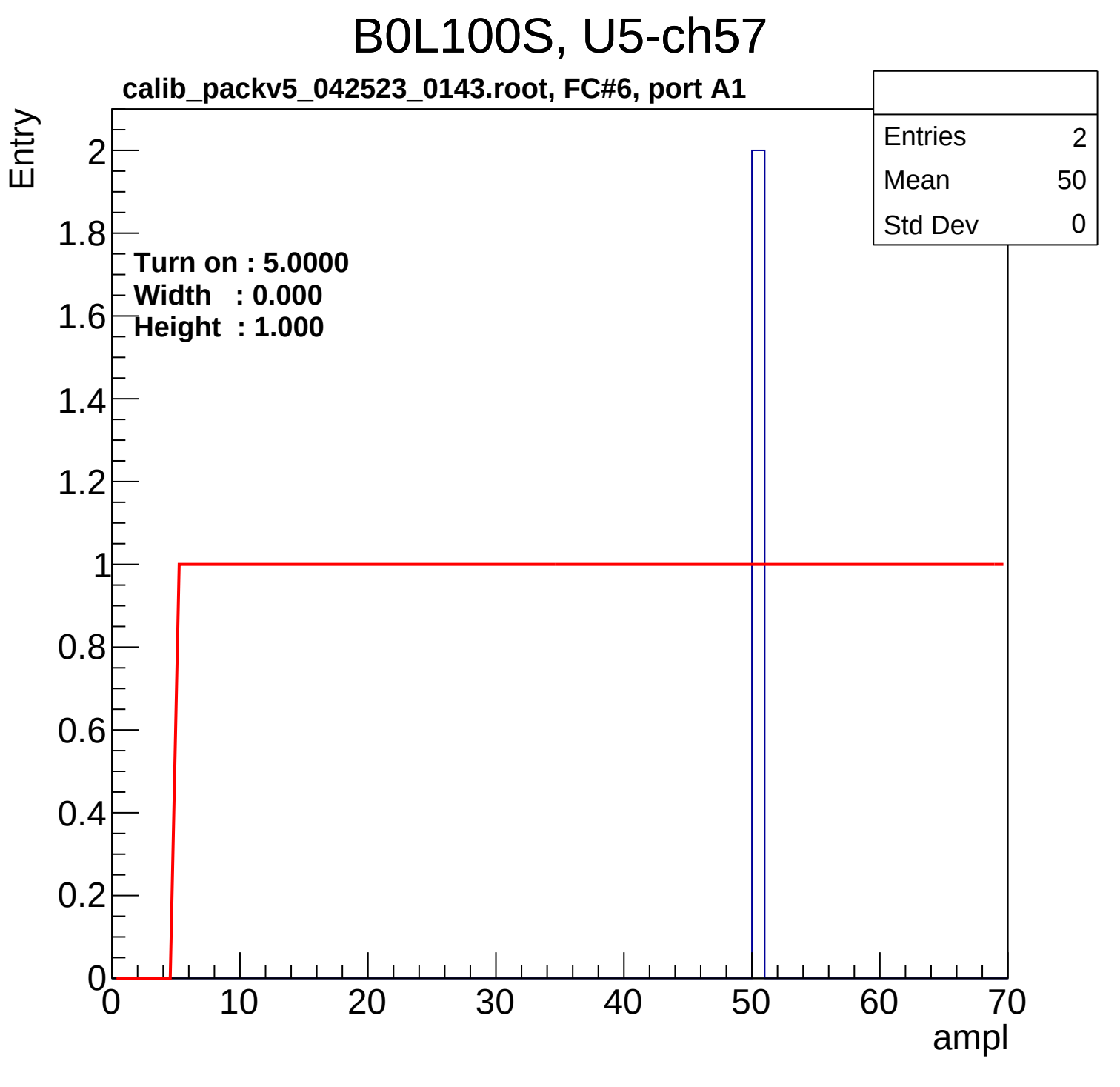

B0L100S, U5-ch52
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

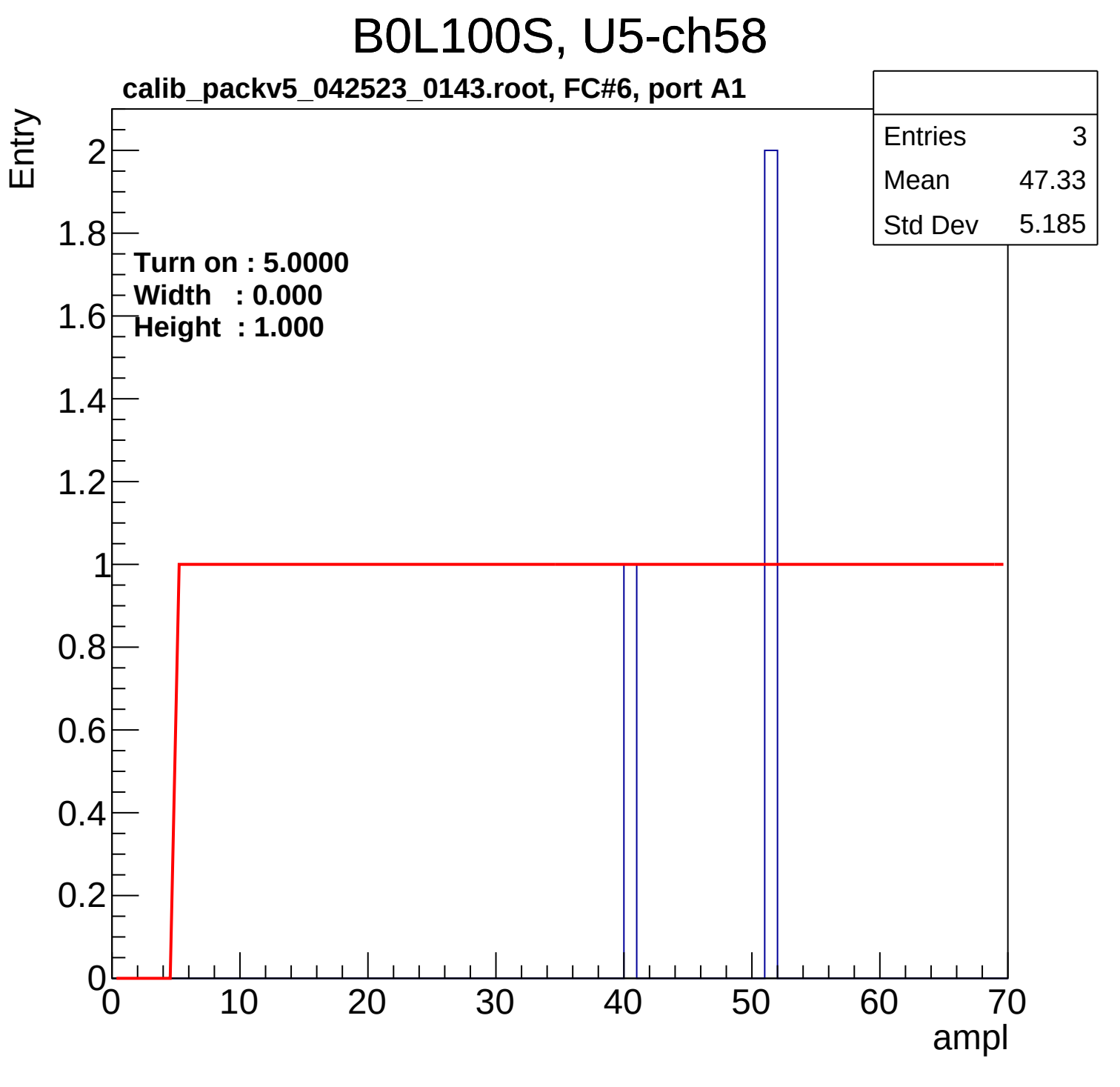

B0L100S, U5-ch53
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

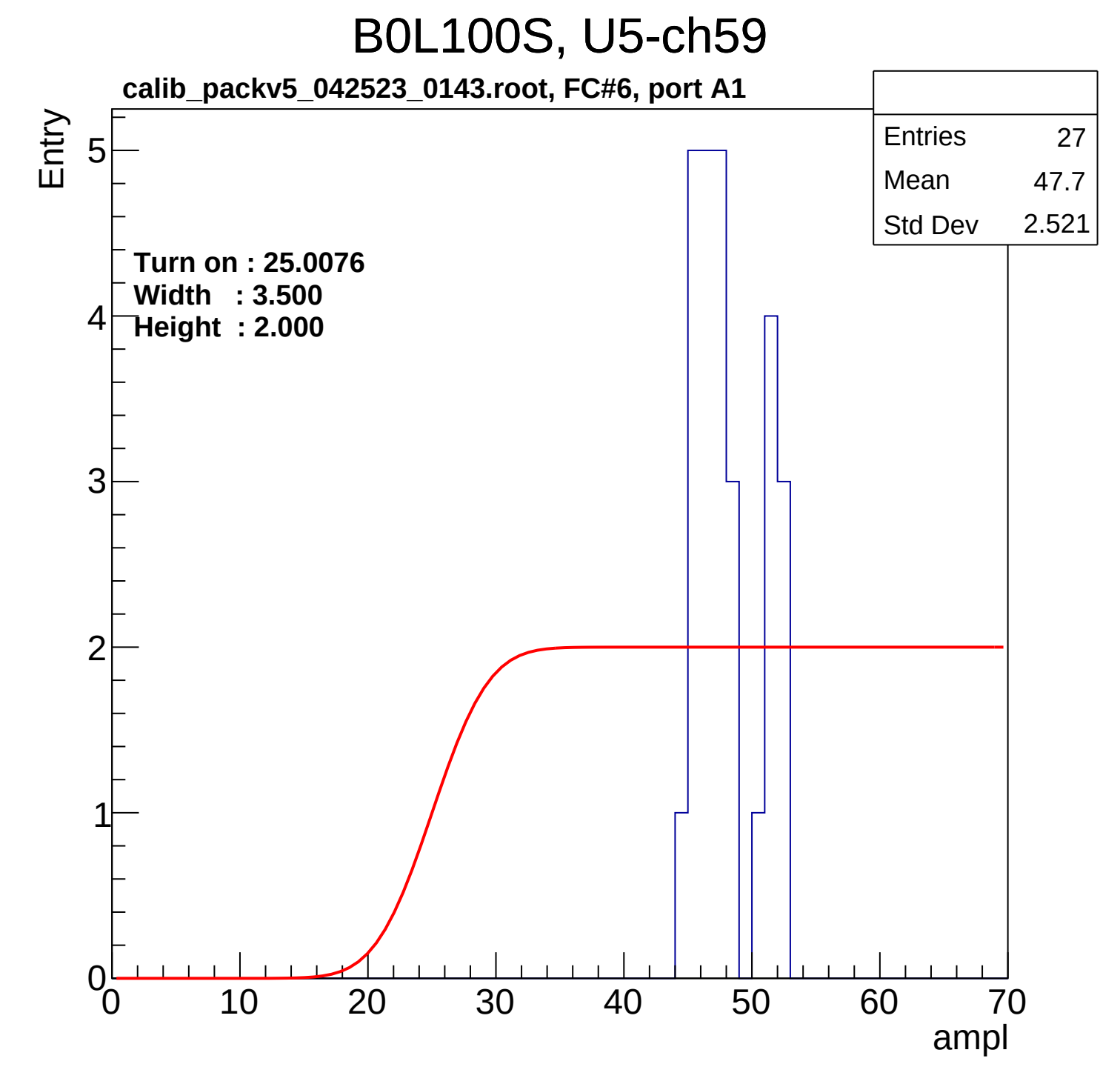

B0L100S, U5-ch54
calib_packv5_042523_0143.root, FC#6, port A1
Entries 46
Mean 46.87
Std Dev 4.853
Turn on : 40.5280
Width : 0.198
Height : 2.254
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

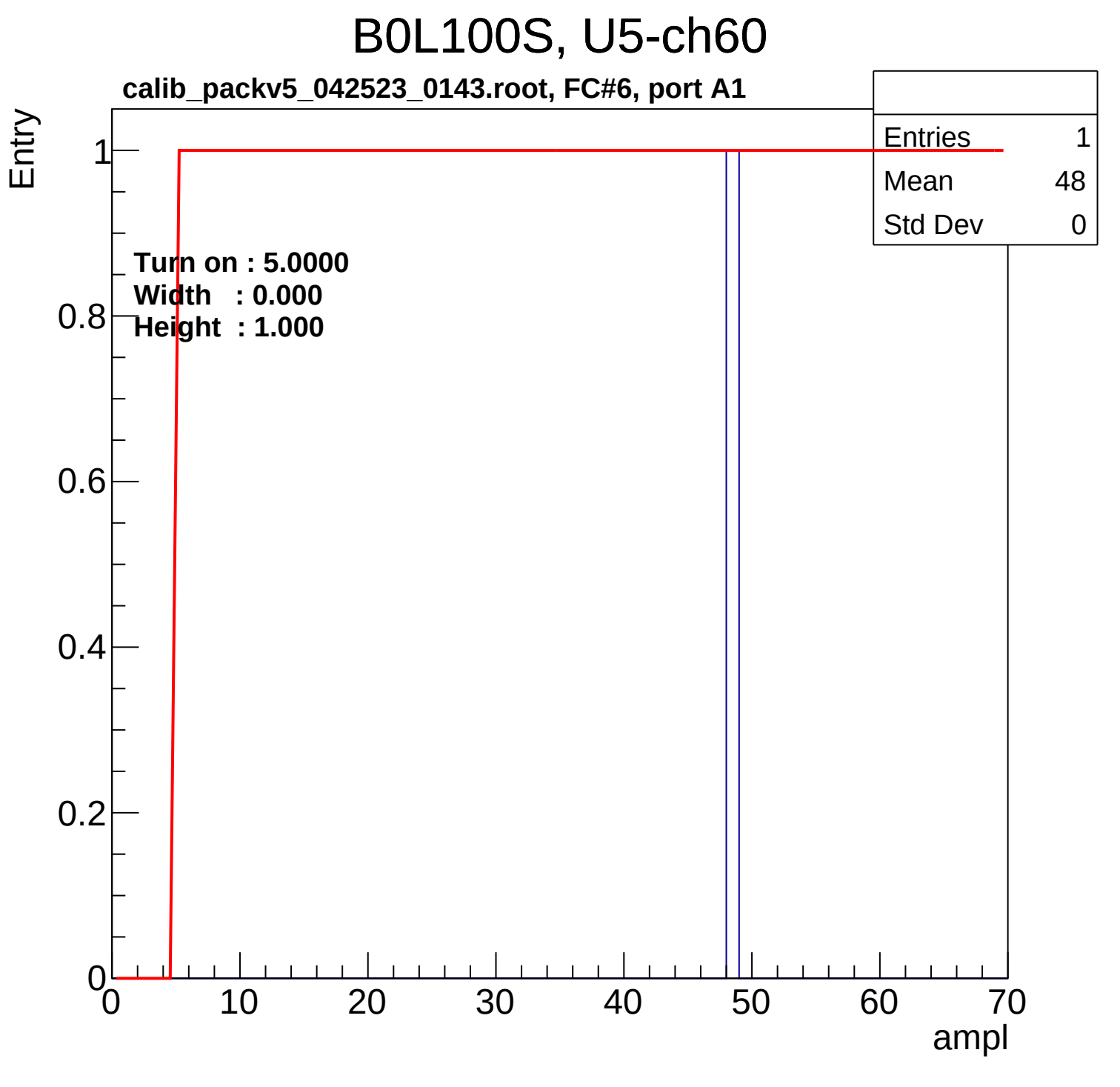

B0L100S, U5-ch55
calib_packv5_042523_0143.root, FC#6, port A1
Entries 4
Mean 44.5
Std Dev 2.598
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

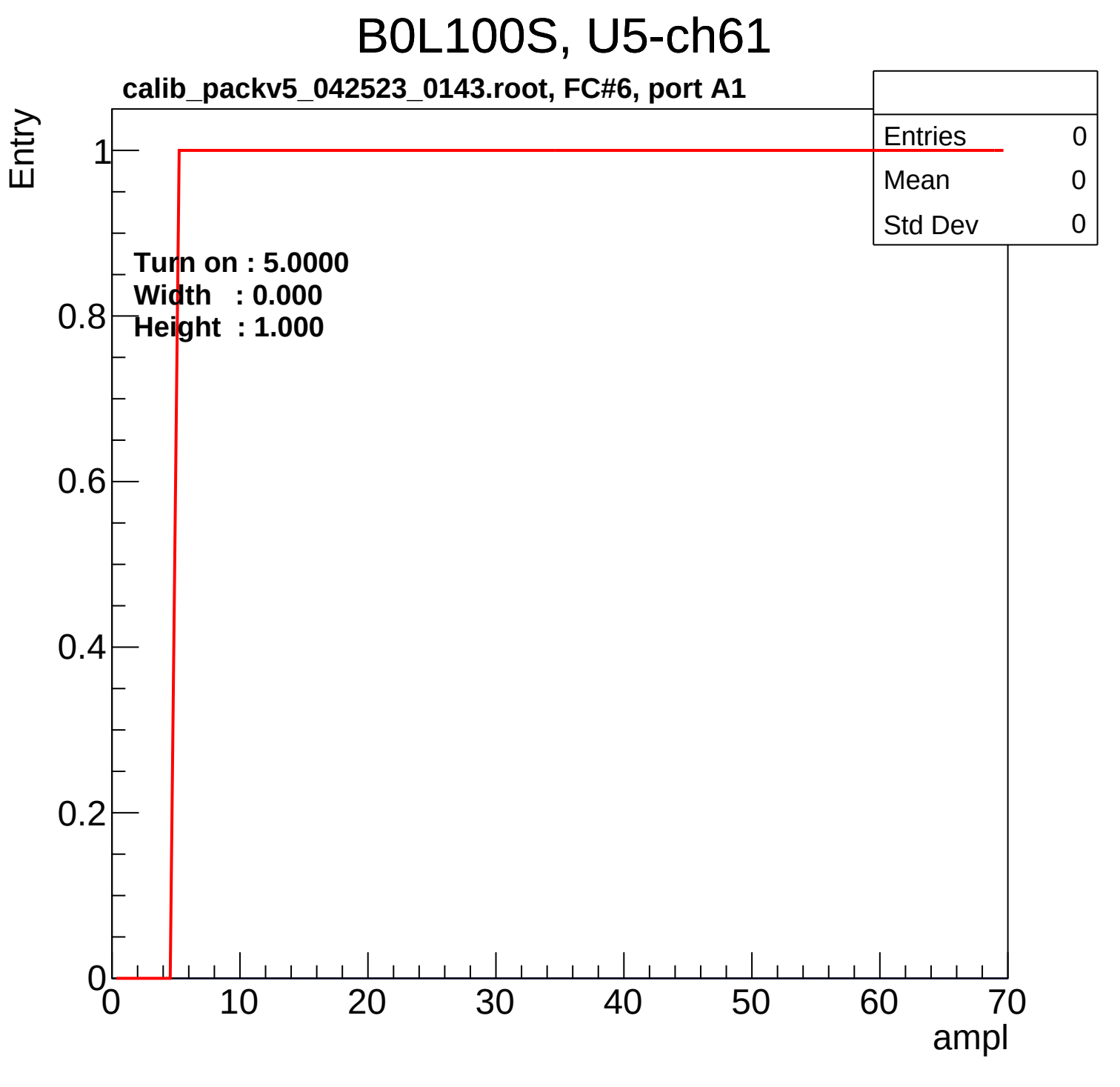

B0L100S, U5-ch56
calib_packv5_042523_0143.root, FC#6, port A1
Entries 8
Mean 41.25
Std Dev 15.64
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

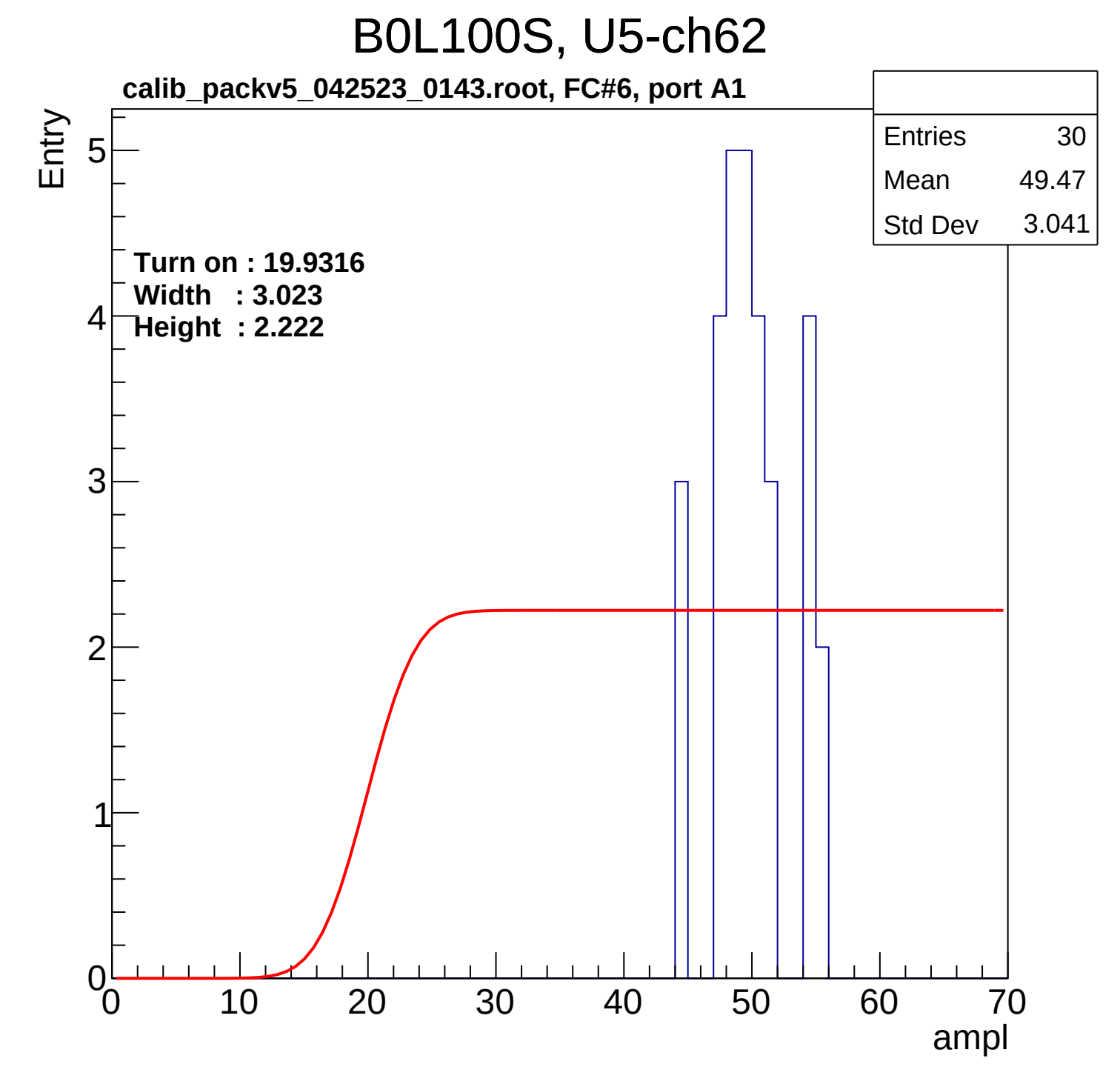

B0L100S, U5-ch57
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 50
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

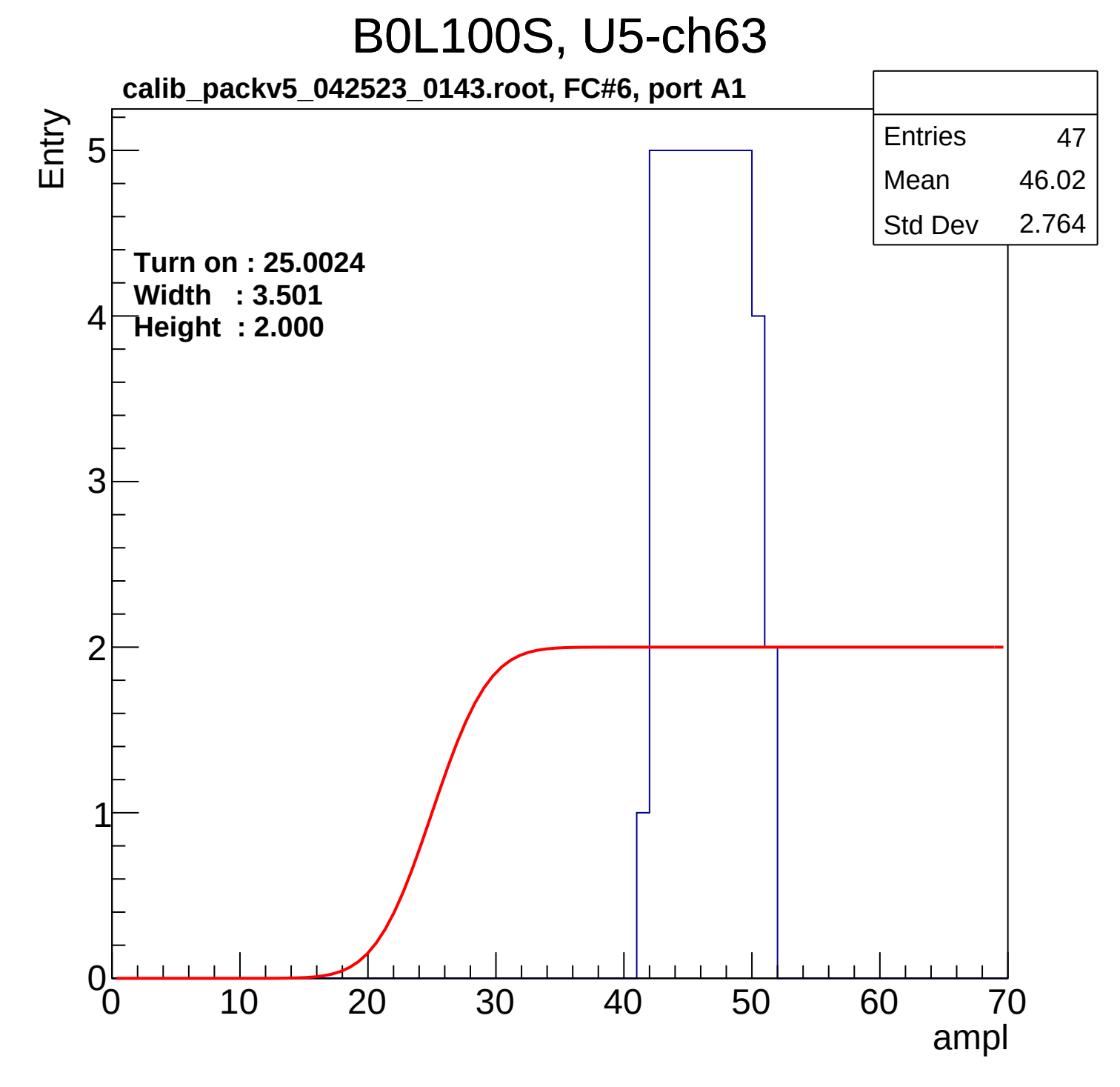

B0L100S, U5-ch58
calib_packv5_042523_0143.root, FC#6, port A1
Entries 3
Mean 47.33
Std Dev 5.185
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

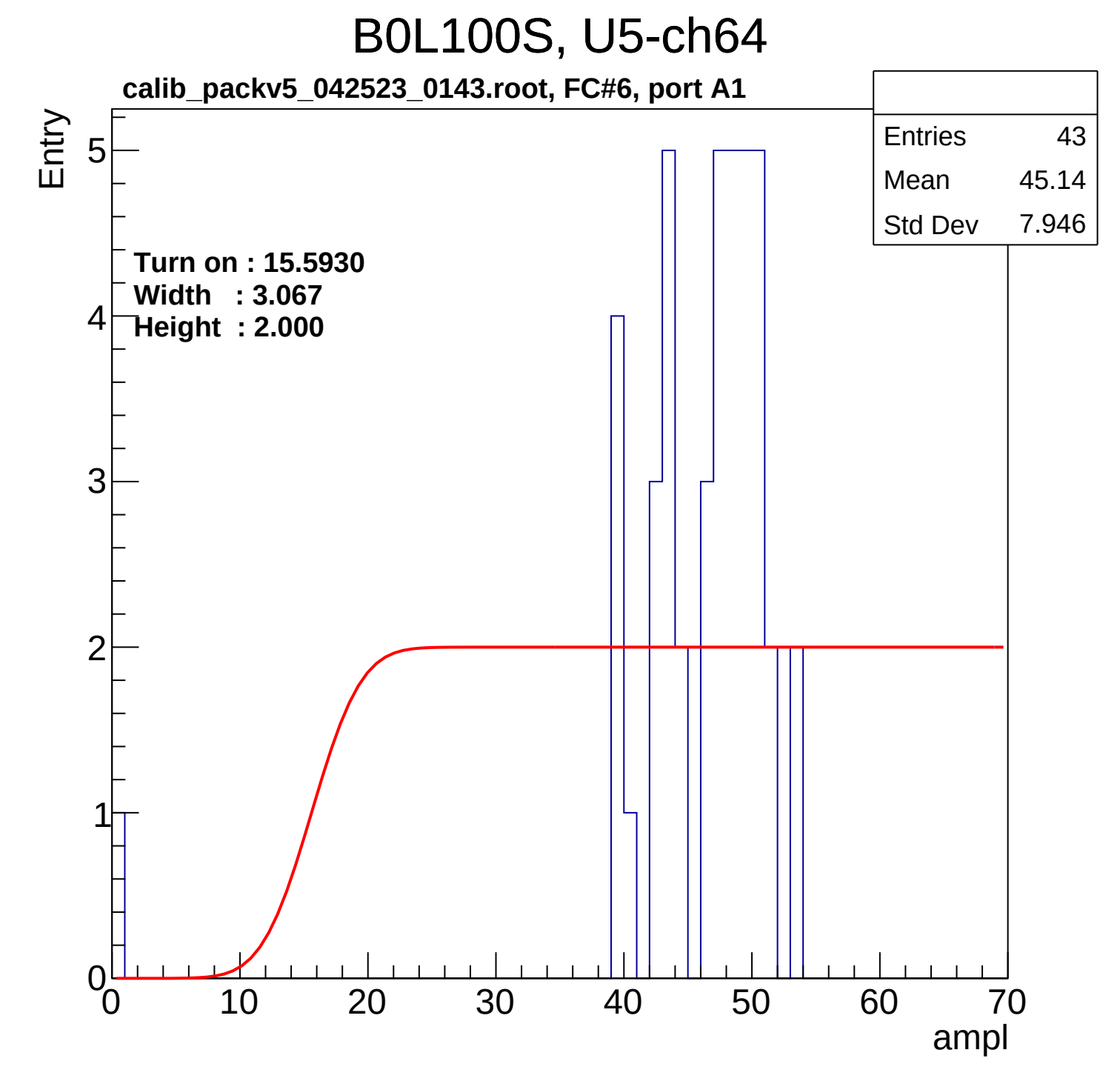

B0L100S, U5-ch59
calib_packv5_042523_0143.root, FC#6, port A1
Entries 27
Mean 47.7
Std Dev 2.521
Turn on : 25.0076
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

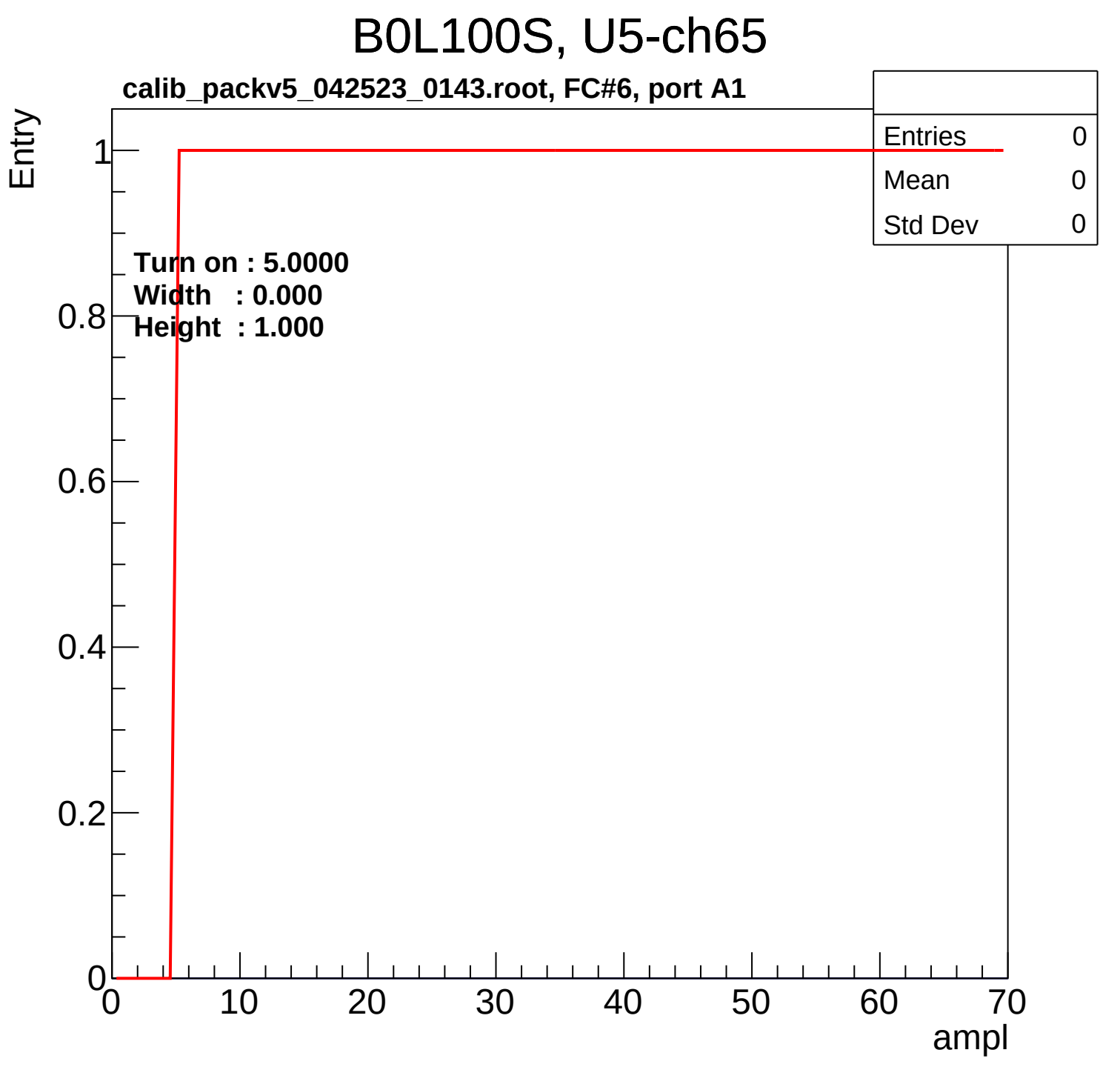

B0L100S, U5-ch60
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 48
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

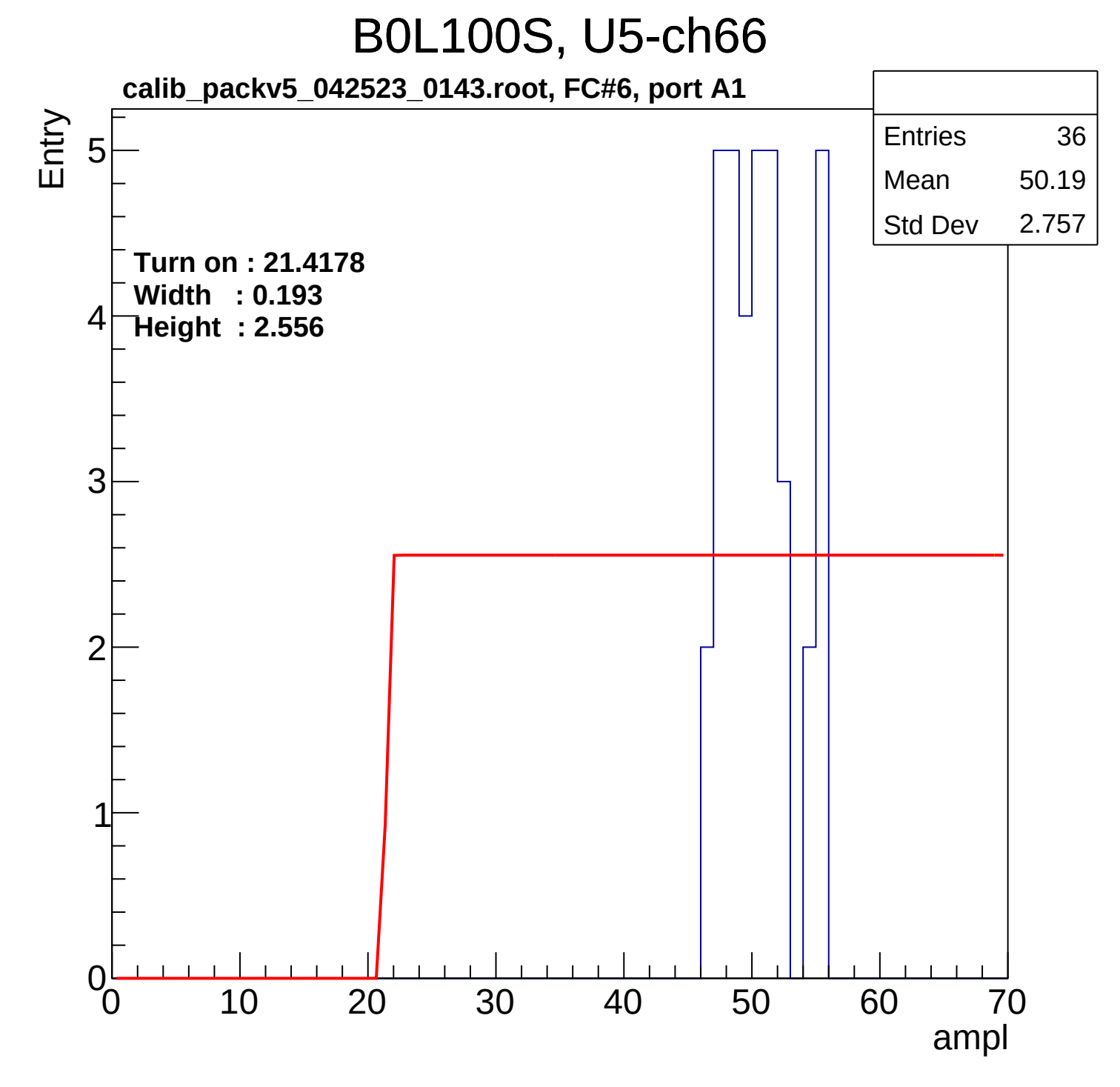

B0L100S, U5-ch61
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

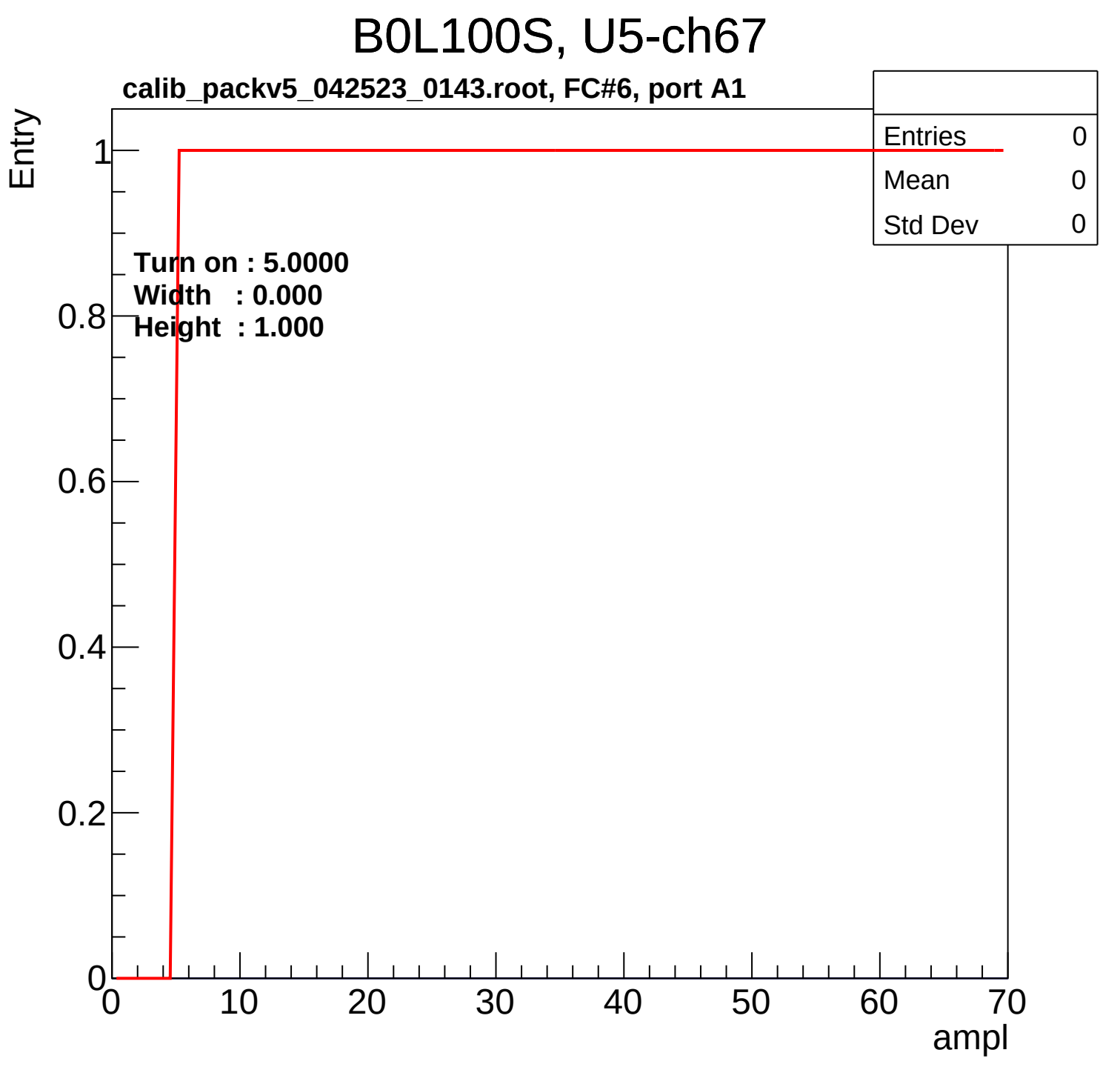

B0L100S, U5-ch62
calib_packv5_042523_0143.root, FC#6, port A1
Entries 30
Mean 49.47
Std Dev 3.041
Turn on : 19.9316
Width : 3.023
Height : 2.222
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

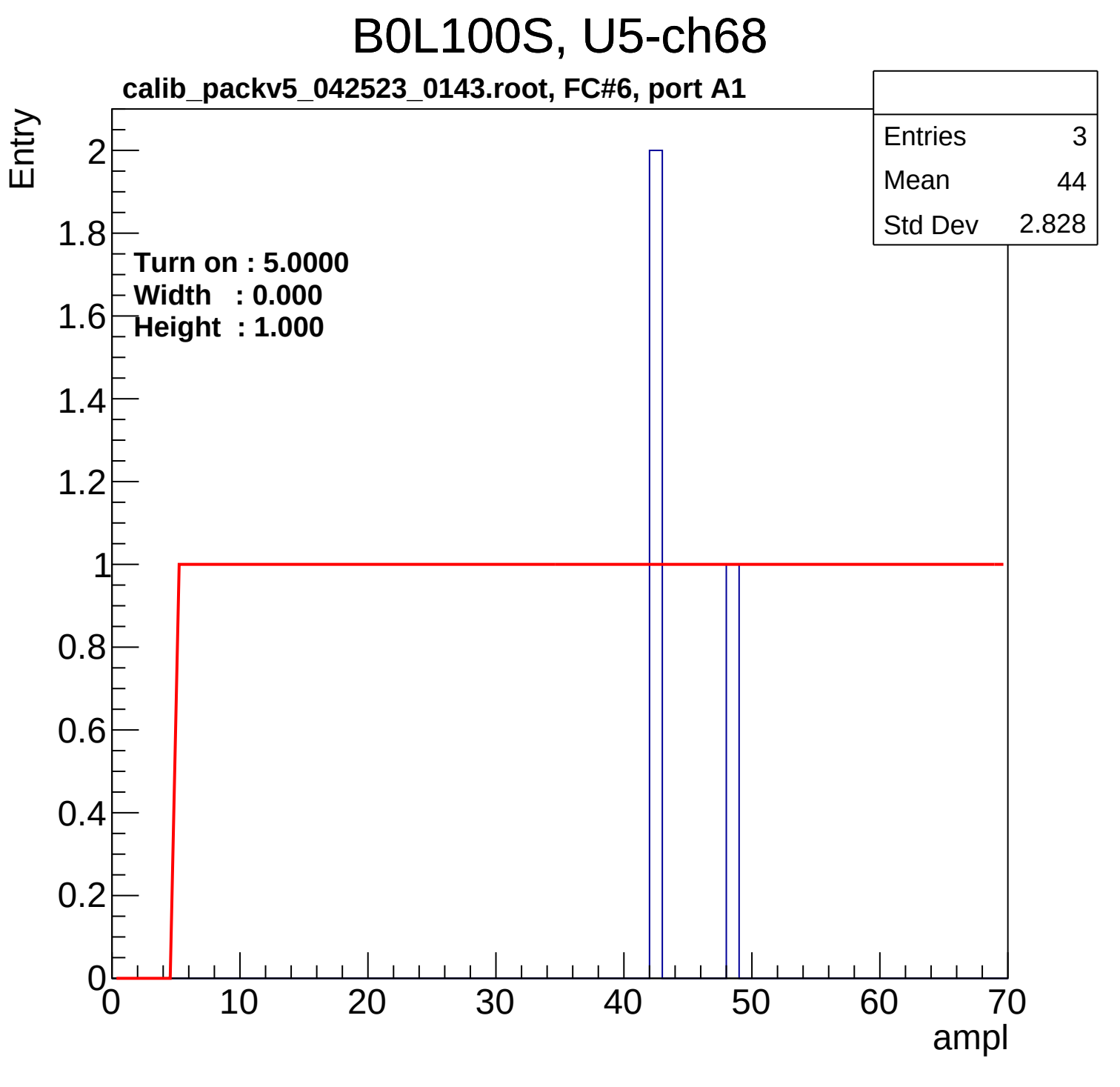

B0L100S, U5-ch63
calib_packv5_042523_0143.root, FC#6, port A1
Entries 47
Mean 46.02
Std Dev 2.764
Turn on : 25.0024
Width : 3.501
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

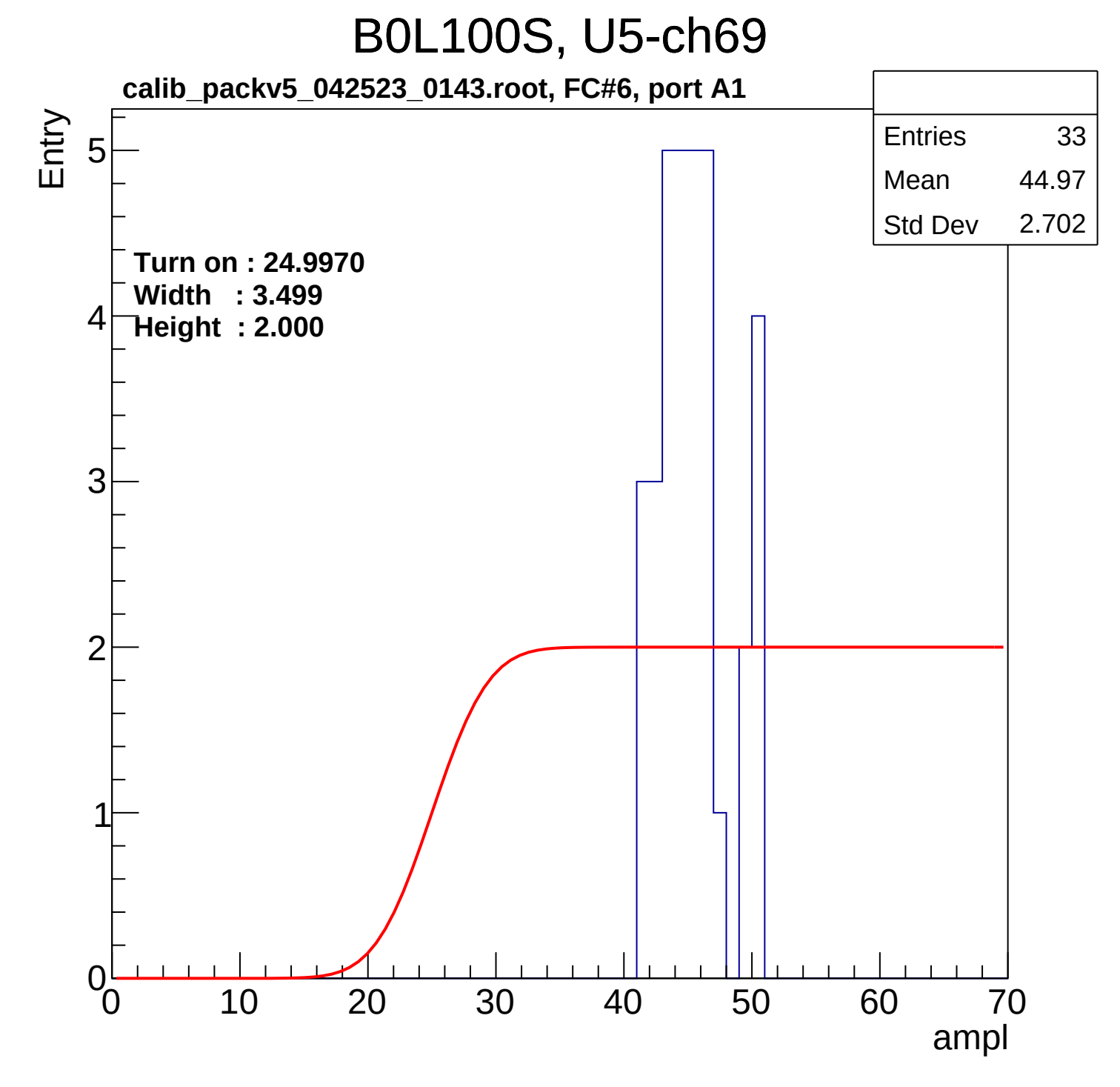

B0L100S, U5-ch64
calib_packv5_042523_0143.root, FC#6, port A1
Entries 43
Mean 45.14
Std Dev 7.946
Turn on : 15.5930
Width : 3.067
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

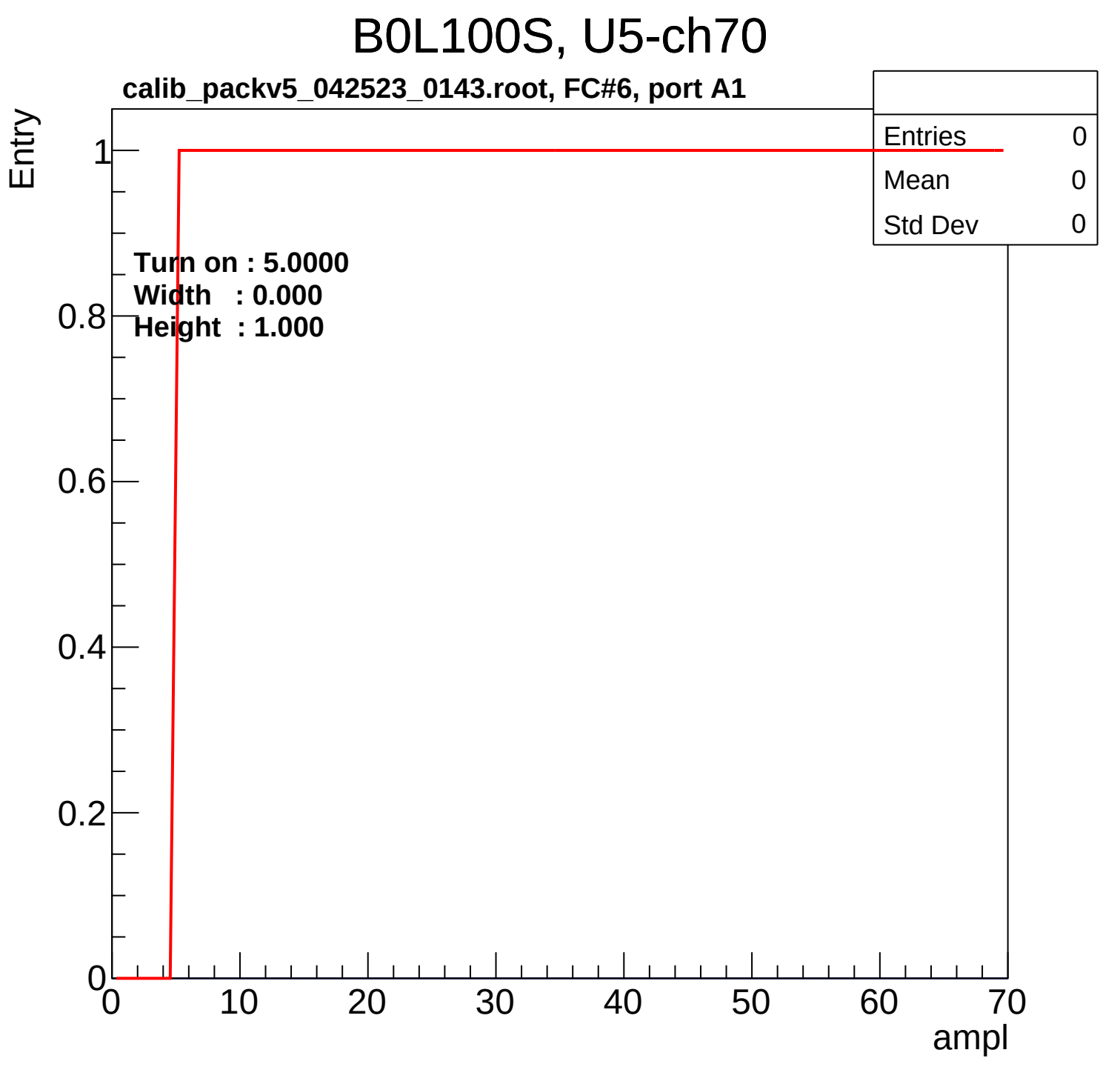

B0L100S, U5-ch65
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

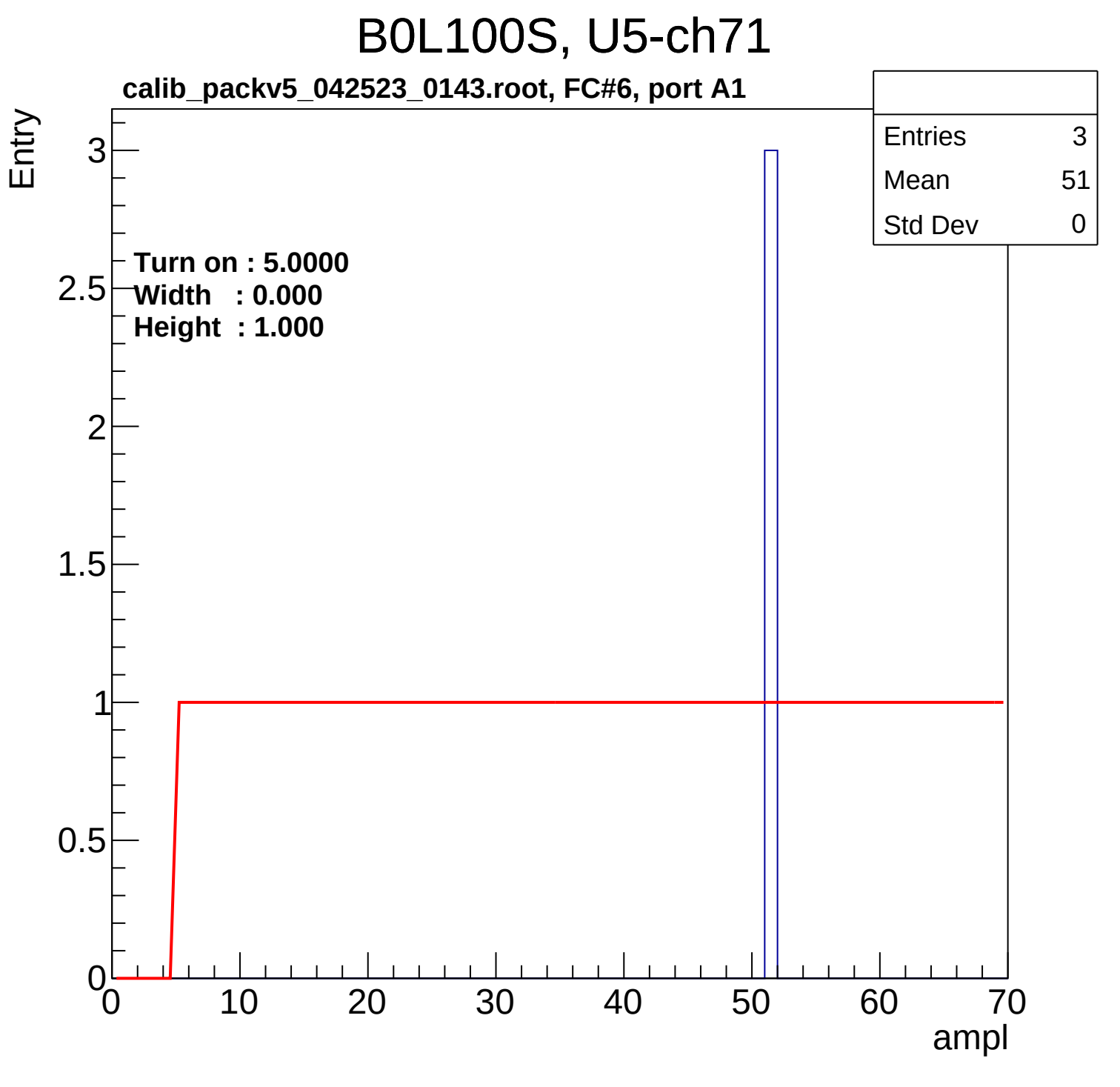

B0L100S, U5-ch66
calib_packv5_042523_0143.root, FC#6, port A1
Entries 36
Mean 50.19
Std Dev 2.757
Turn on : 21.4178
Width : 0.193
Height : 2.556
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

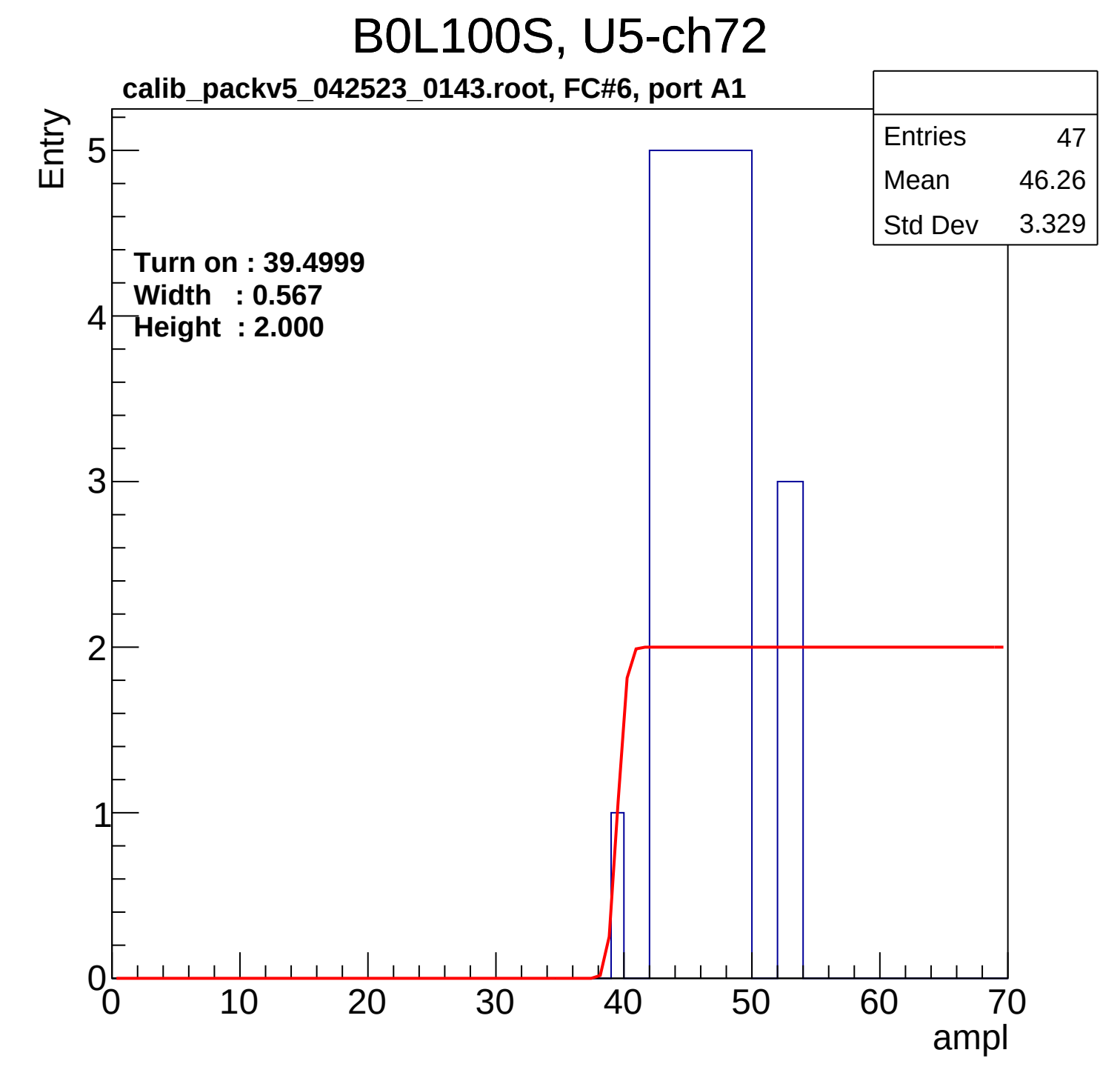

B0L100S, U5-ch67
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

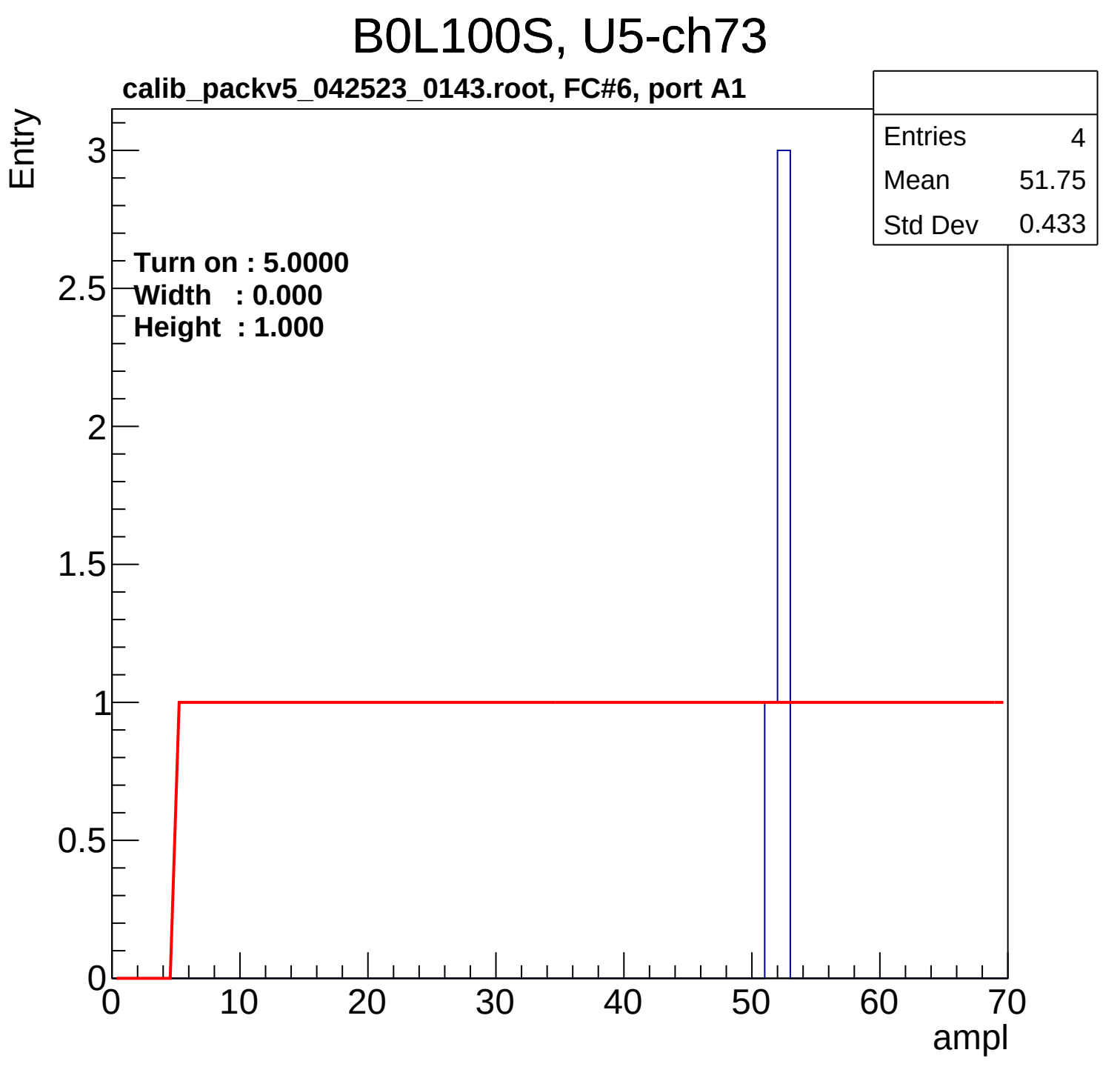

B0L100S, U5-ch68
calib_packv5_042523_0143.root, FC#6, port A1
Entries 3
Mean 44
Std Dev 2.828
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

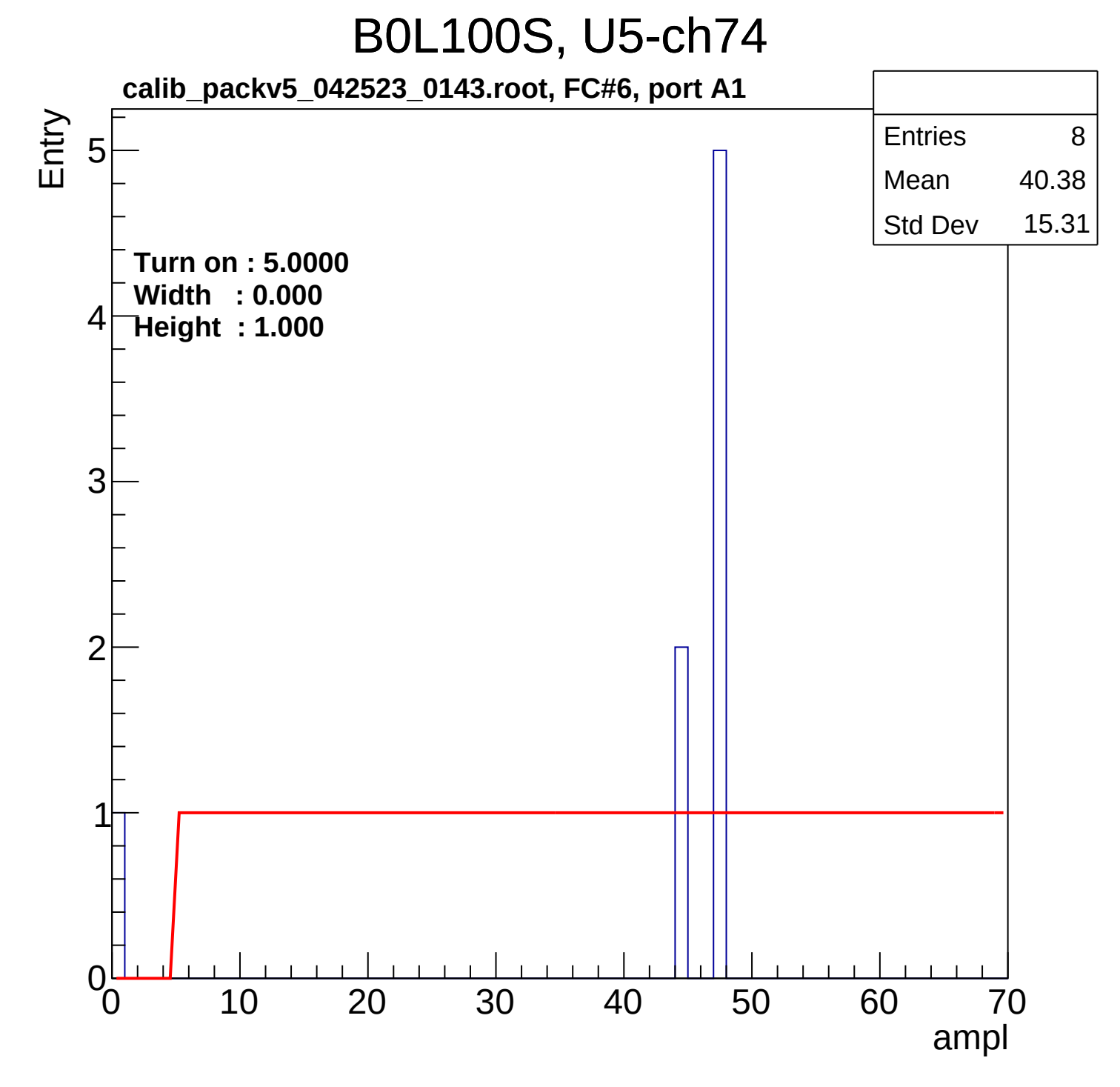

B0L100S, U5-ch69
calib_packv5_042523_0143.root, FC#6, port A1
Entries 33
Mean 44.97
Std Dev 2.702
Turn on : 24.9970
Width : 3.499
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

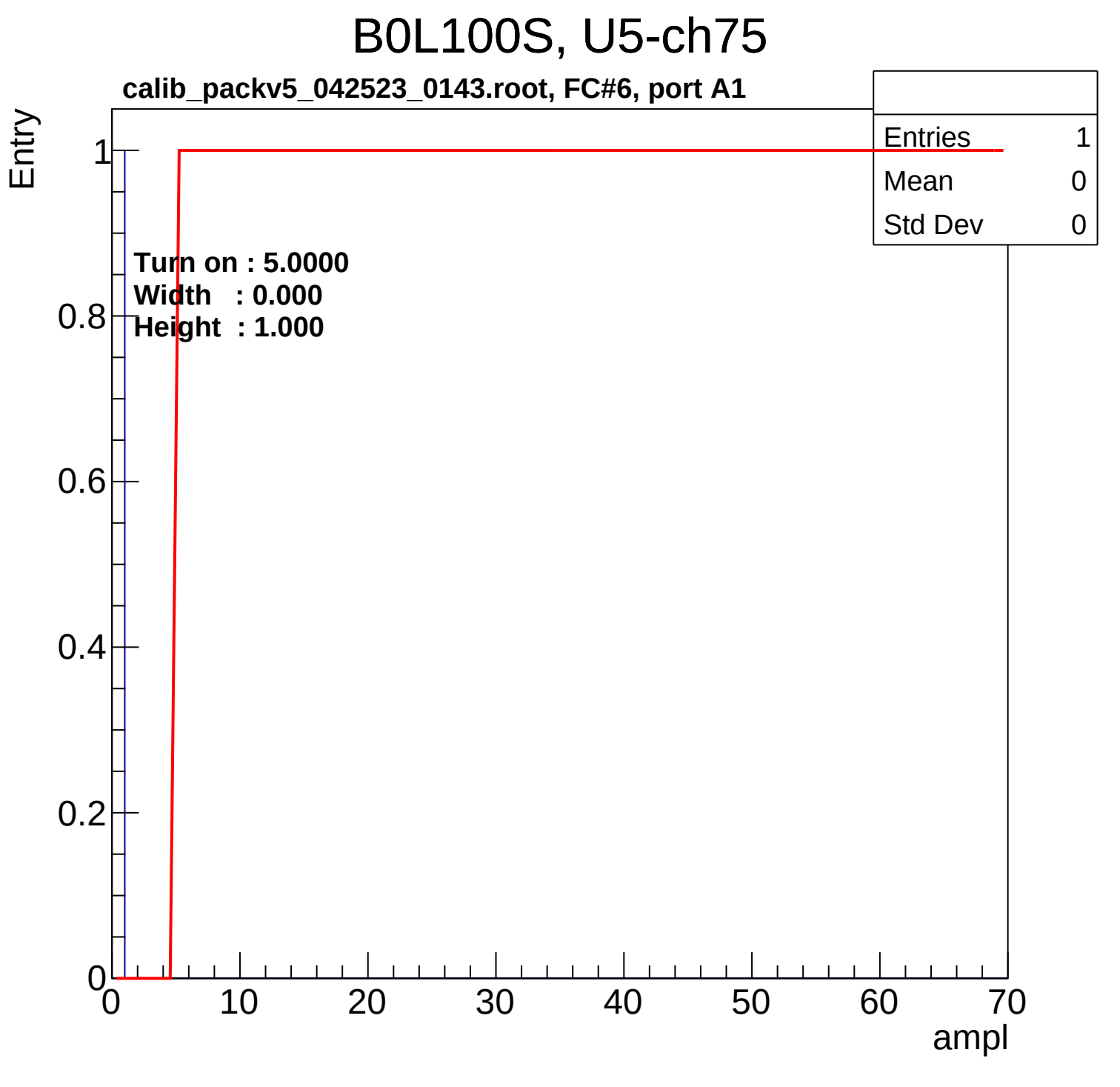

B0L100S, U5-ch70
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

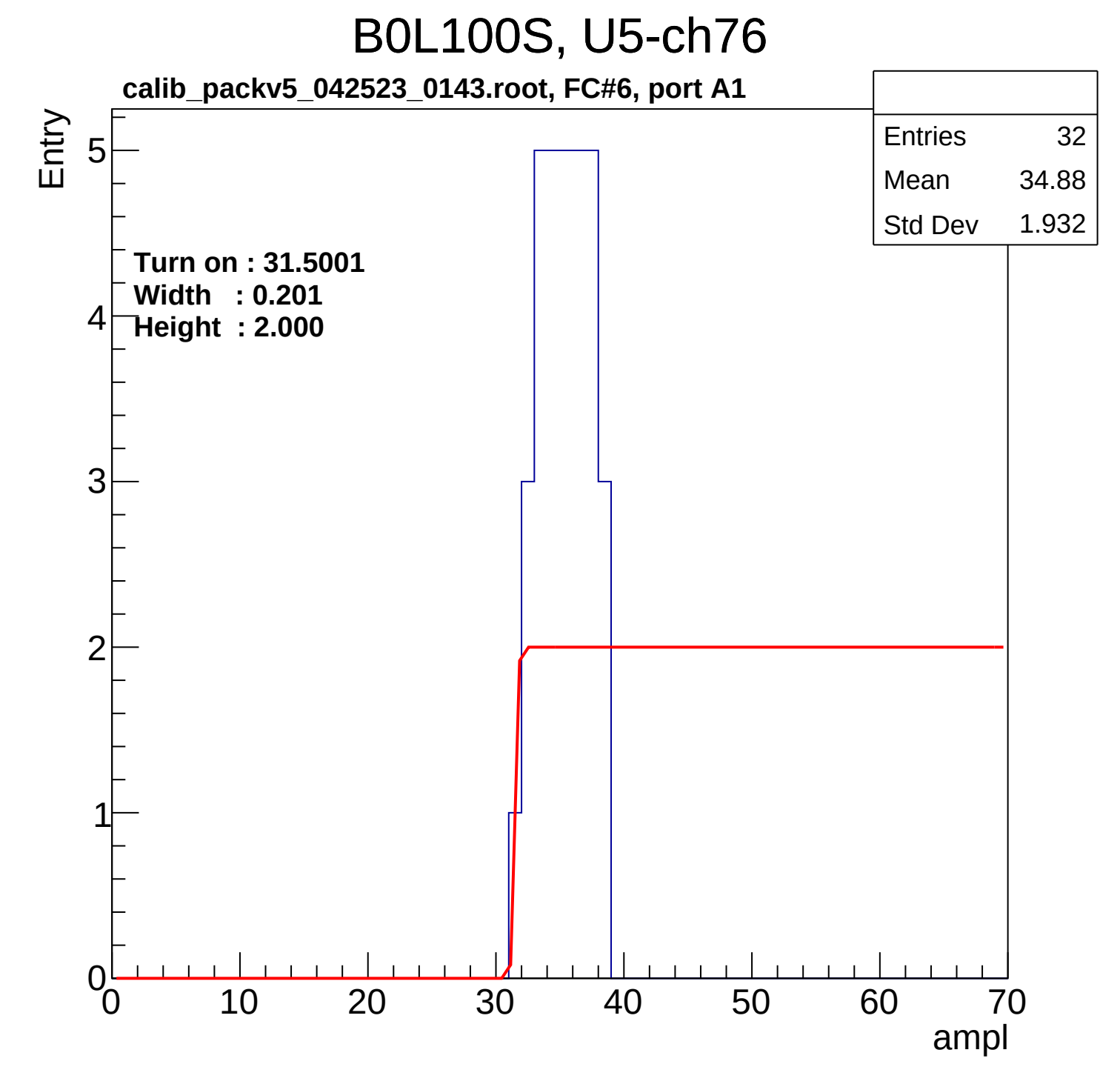

B0L100S, U5-ch71
calib_packv5_042523_0143.root, FC#6, port A1
Entries 3
Mean 51
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

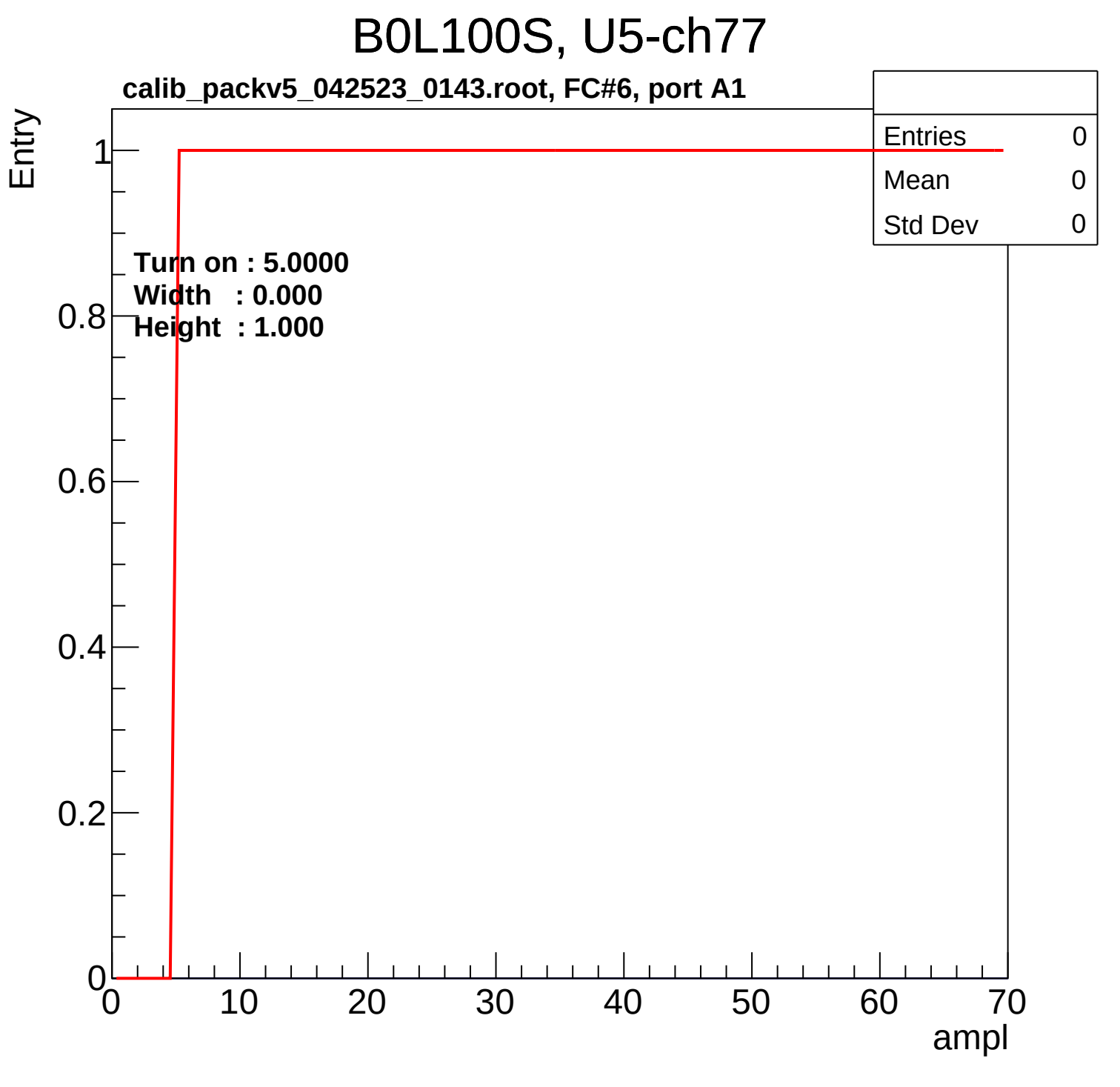

B0L100S, U5-ch72
calib_packv5_042523_0143.root, FC#6, port A1
Entries 47
Mean 46.26
Std Dev 3.329
Turn on : 39.4999
Width : 0.567
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

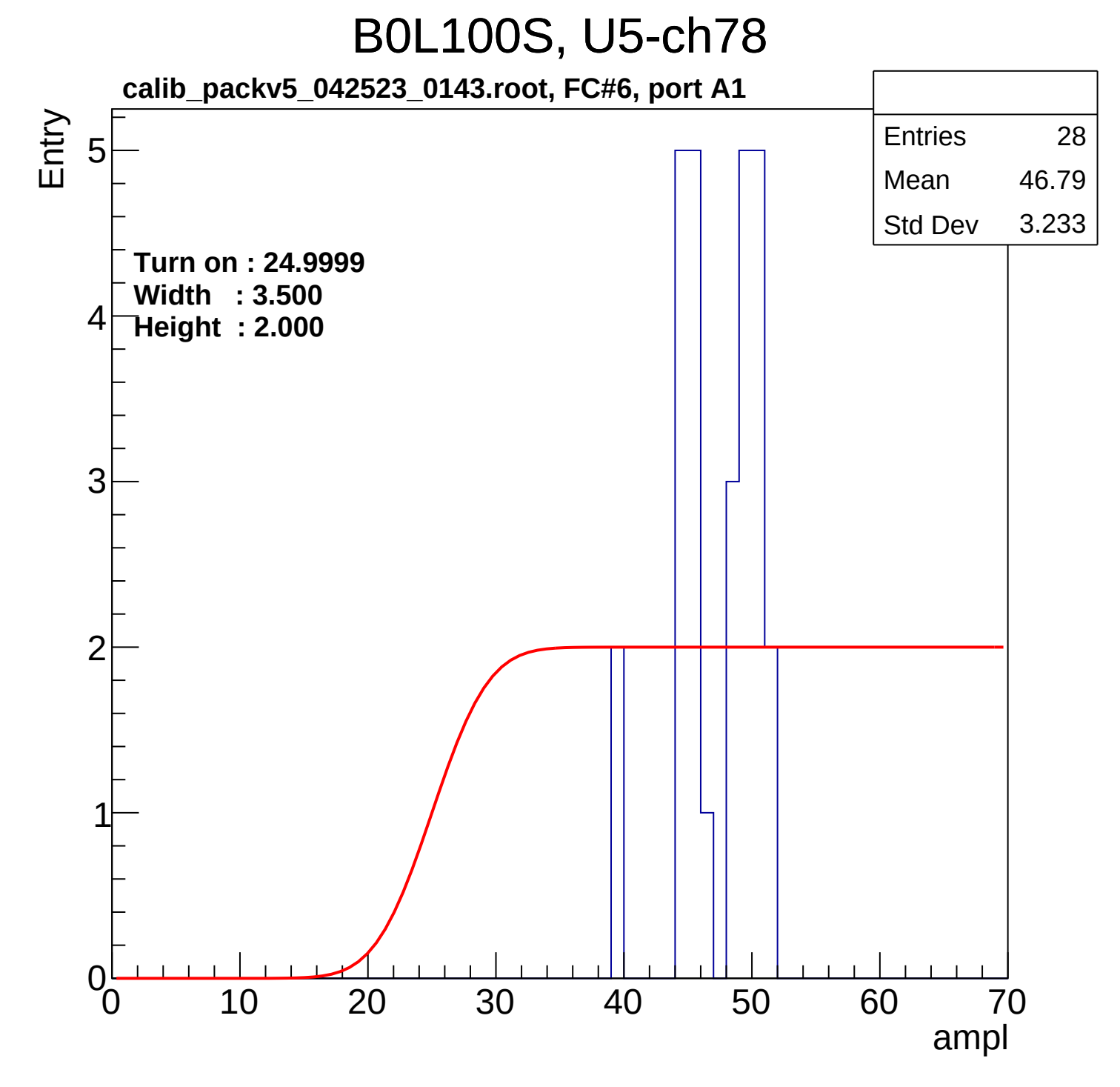

B0L100S, U5-ch73
calib_packv5_042523_0143.root, FC#6, port A1
Entries 4
Mean 51.75
Std Dev 0.433
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

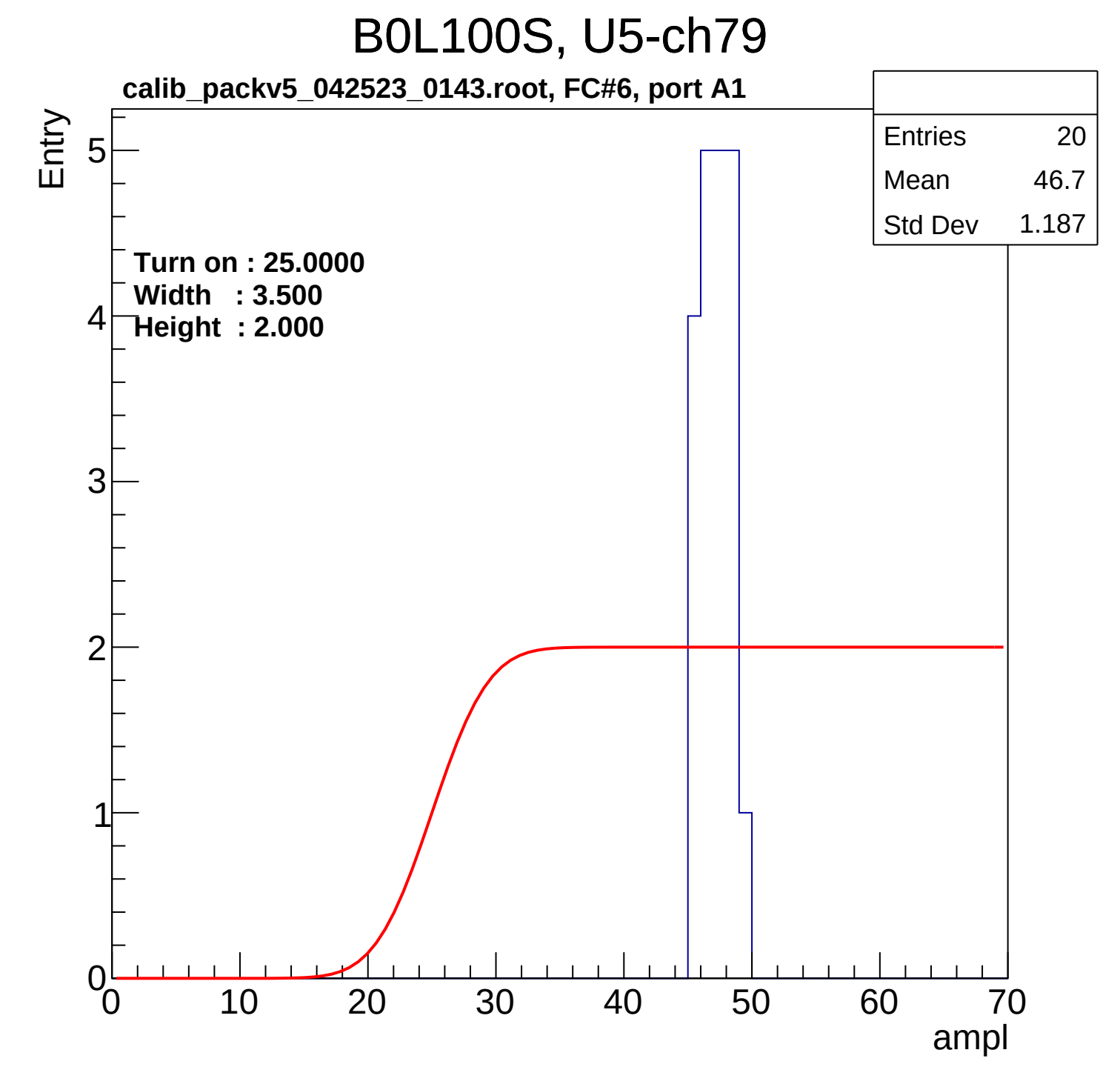

B0L100S, U5-ch74
calib_packv5_042523_0143.root, FC#6, port A1
Entries 8
Mean 40.38
Std Dev 15.31
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

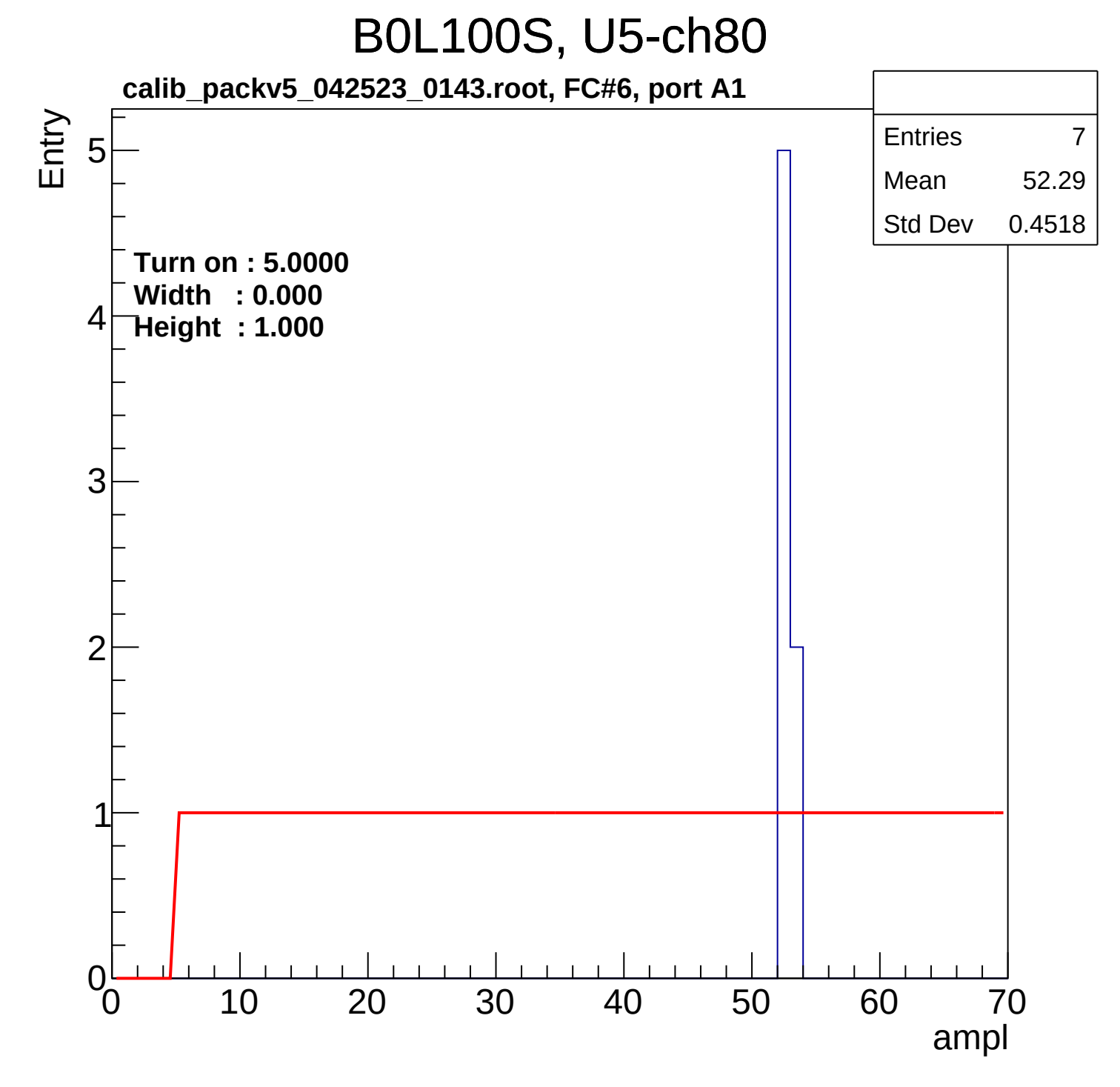

B0L100S, U5-ch75
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

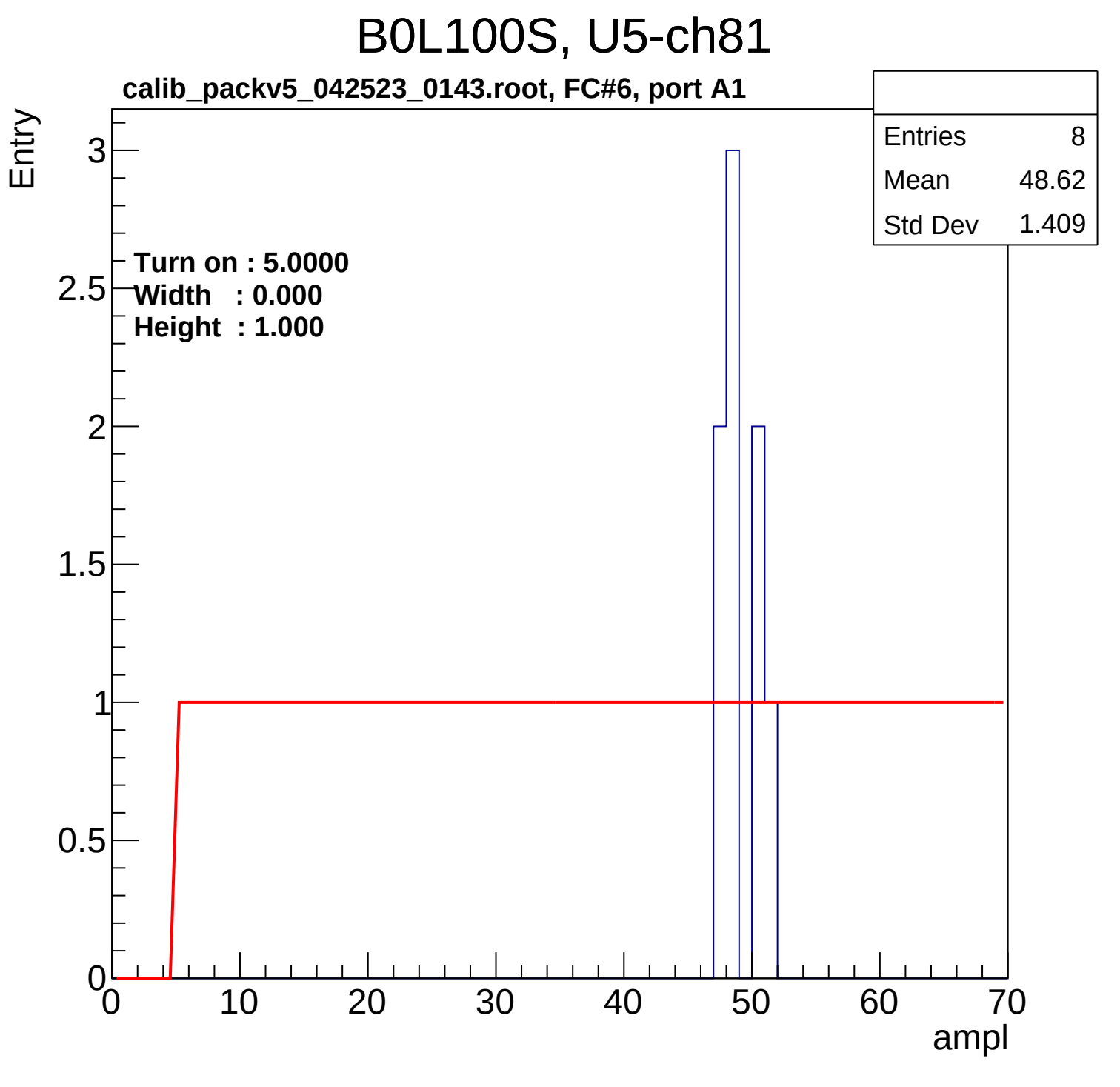

B0L100S, U5-ch76
calib_packv5_042523_0143.root, FC#6, port A1
Entries 32
Mean 34.88
Std Dev 1.932
Turn on : 31.5001
Width : 0.201
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

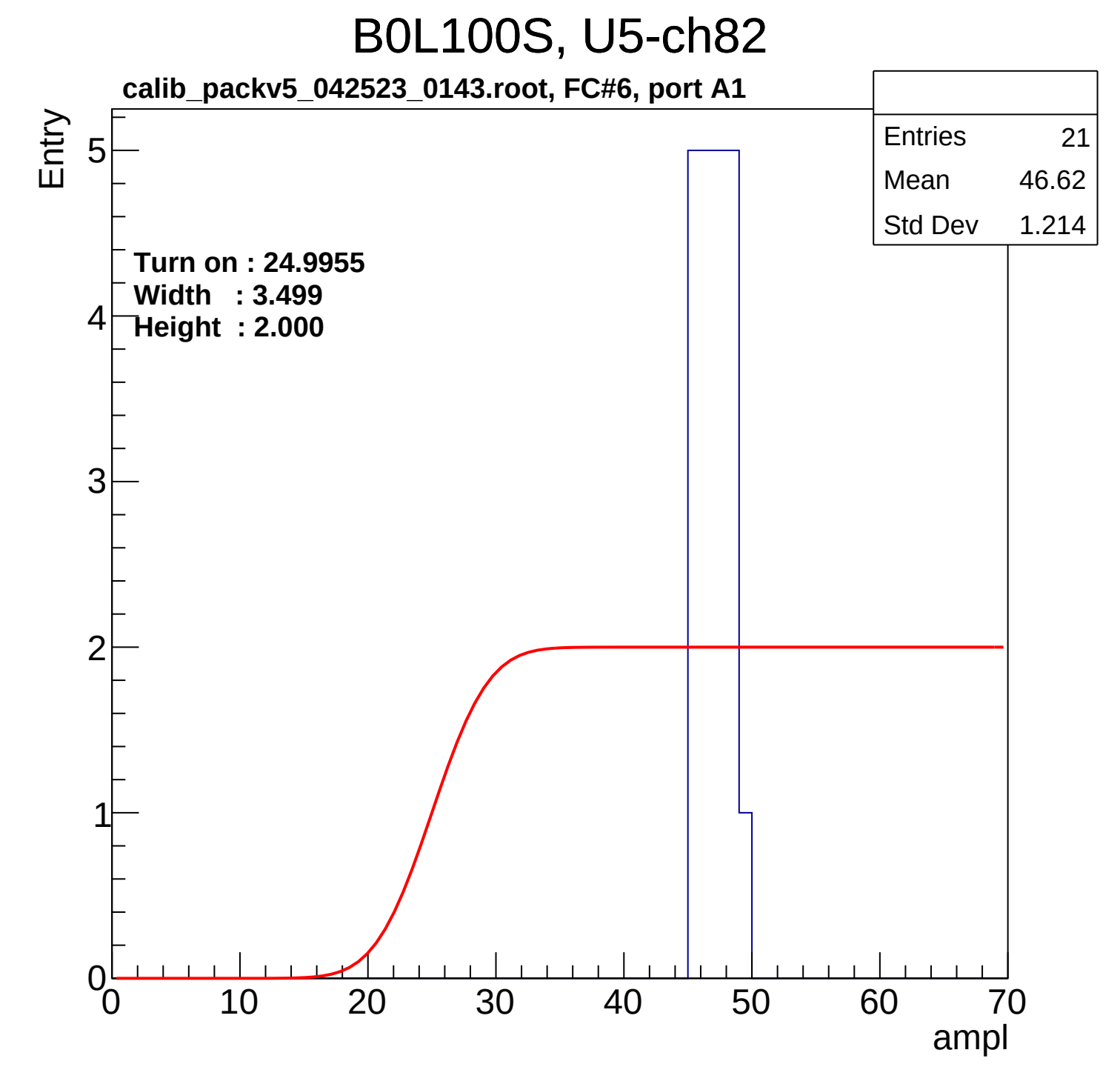

B0L100S, U5-ch77
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

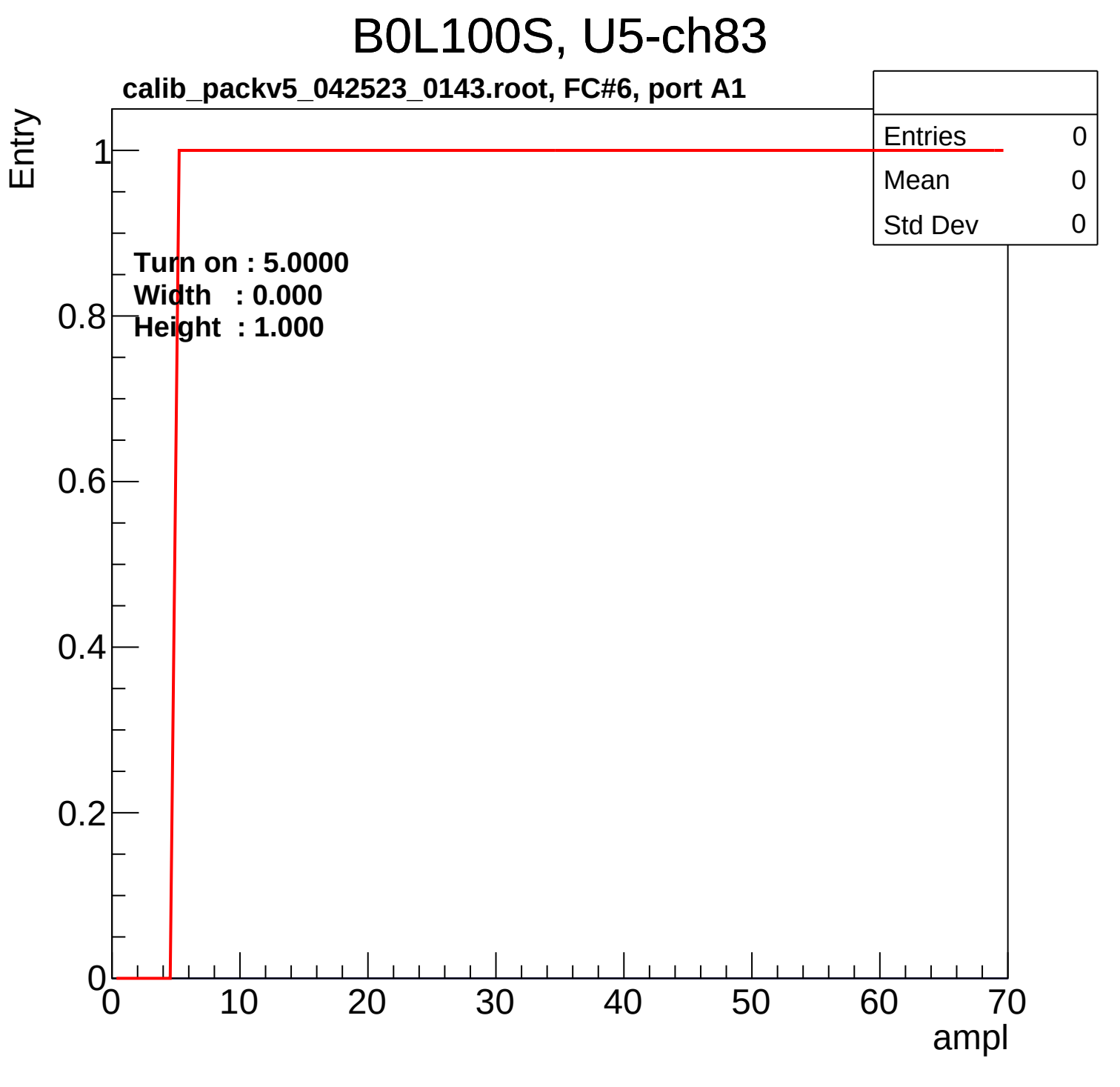

B0L100S, U5-ch78
calib_packv5_042523_0143.root, FC#6, port A1
Entries 28
Mean 46.79
Std Dev 3.233
Turn on : 24.9999
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

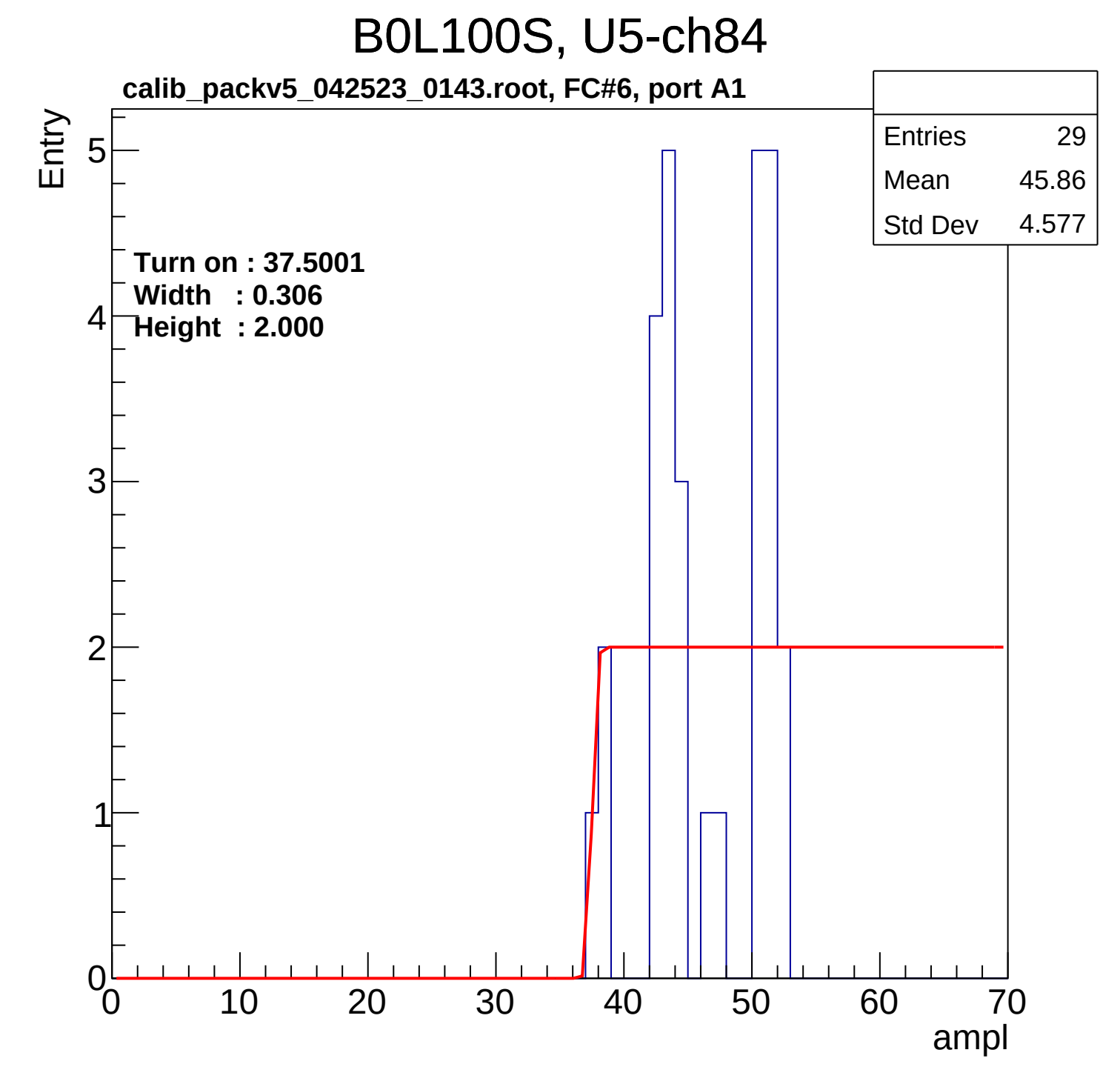

B0L100S, U5-ch79
calib_packv5_042523_0143.root, FC#6, port A1
Entries 20
Mean 46.7
Std Dev 1.187
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

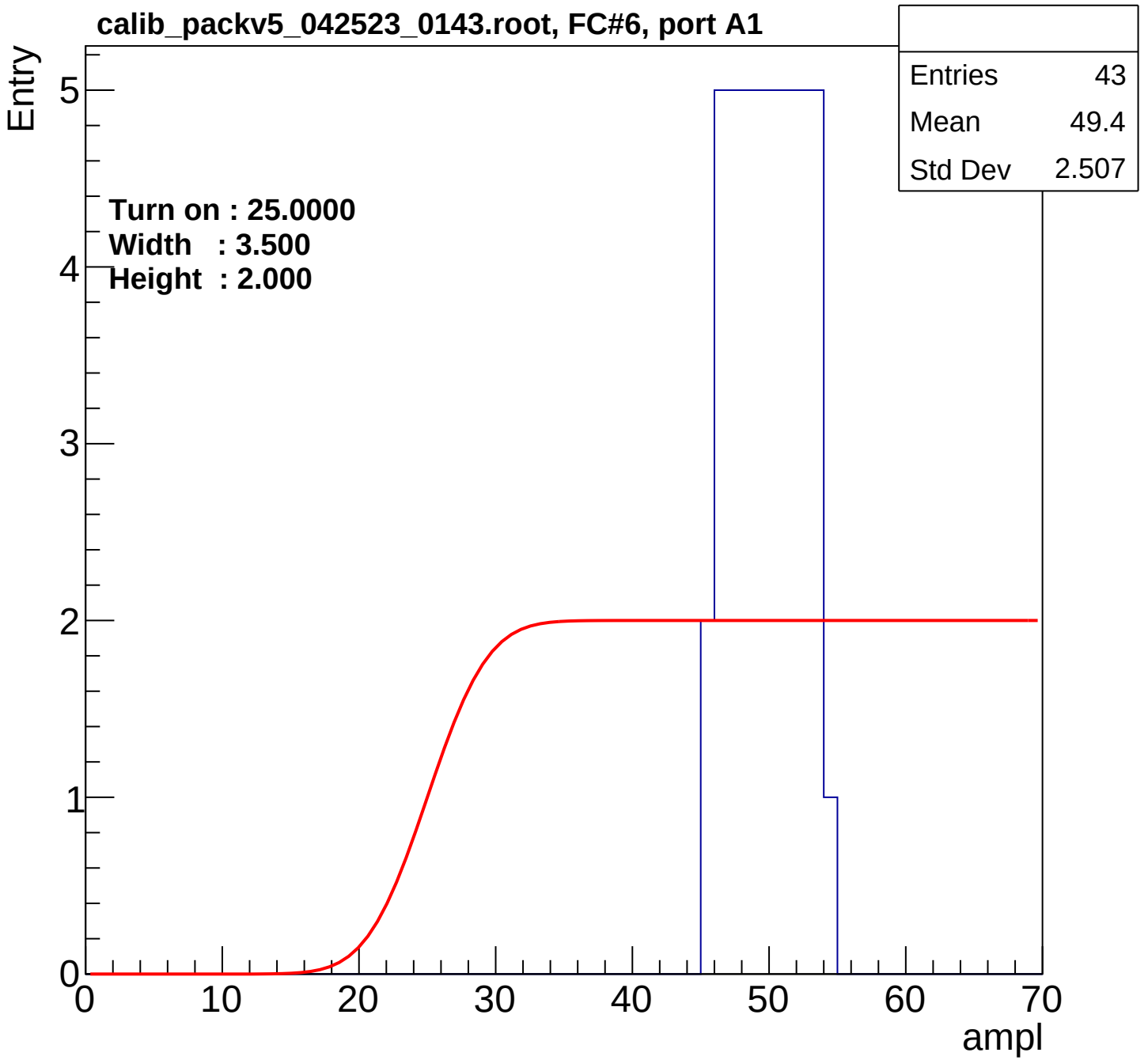

B0L100S, U5-ch80
calib_packv5_042523_0143.root, FC#6, port A1
Entries 7
Mean 52.29
Std Dev 0.4518
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

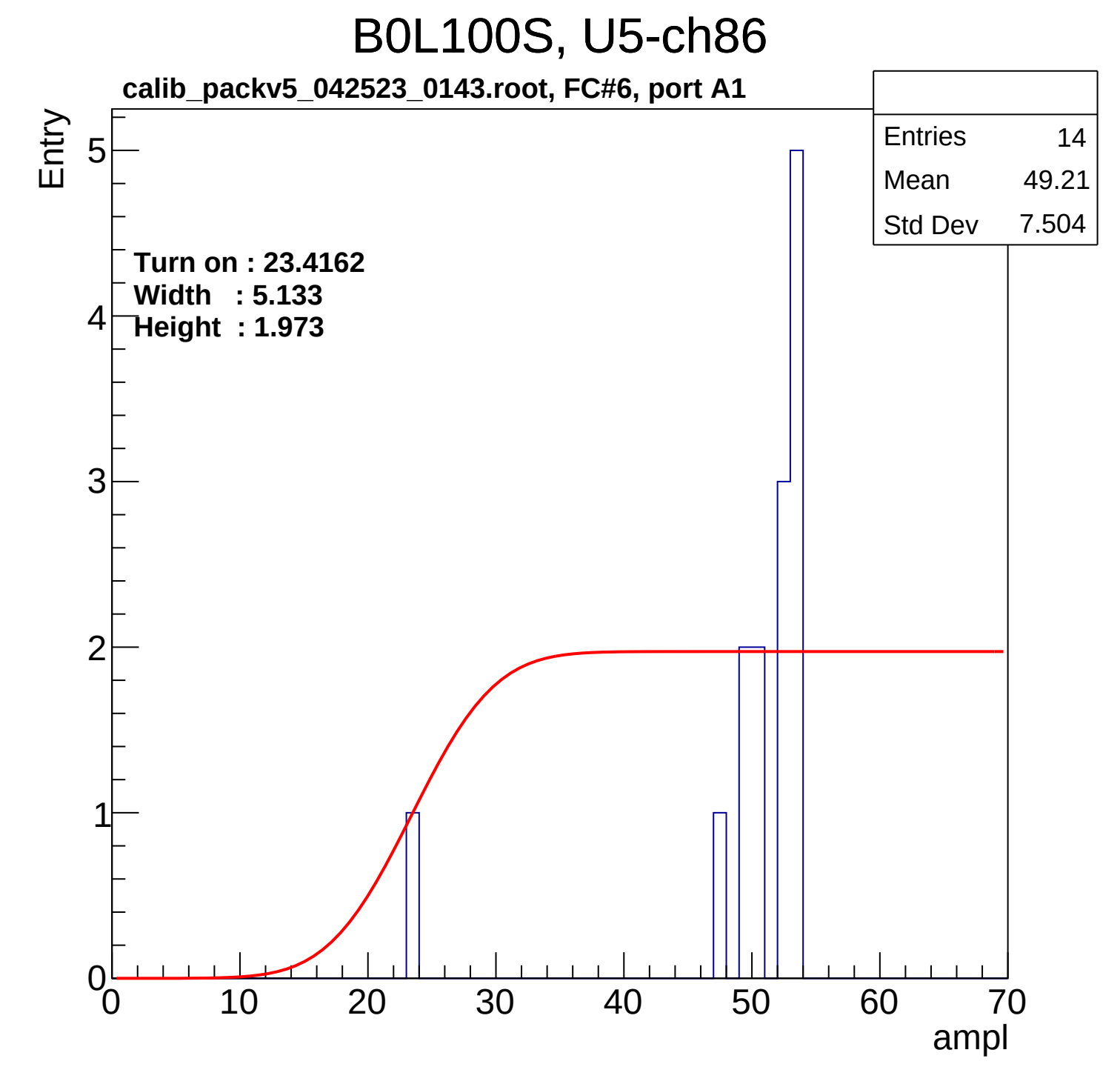

B0L100S, U5-ch81
calib_packv5_042523_0143.root, FC#6, port A1
Entries 8
Mean 48.62
Std Dev 1.409
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

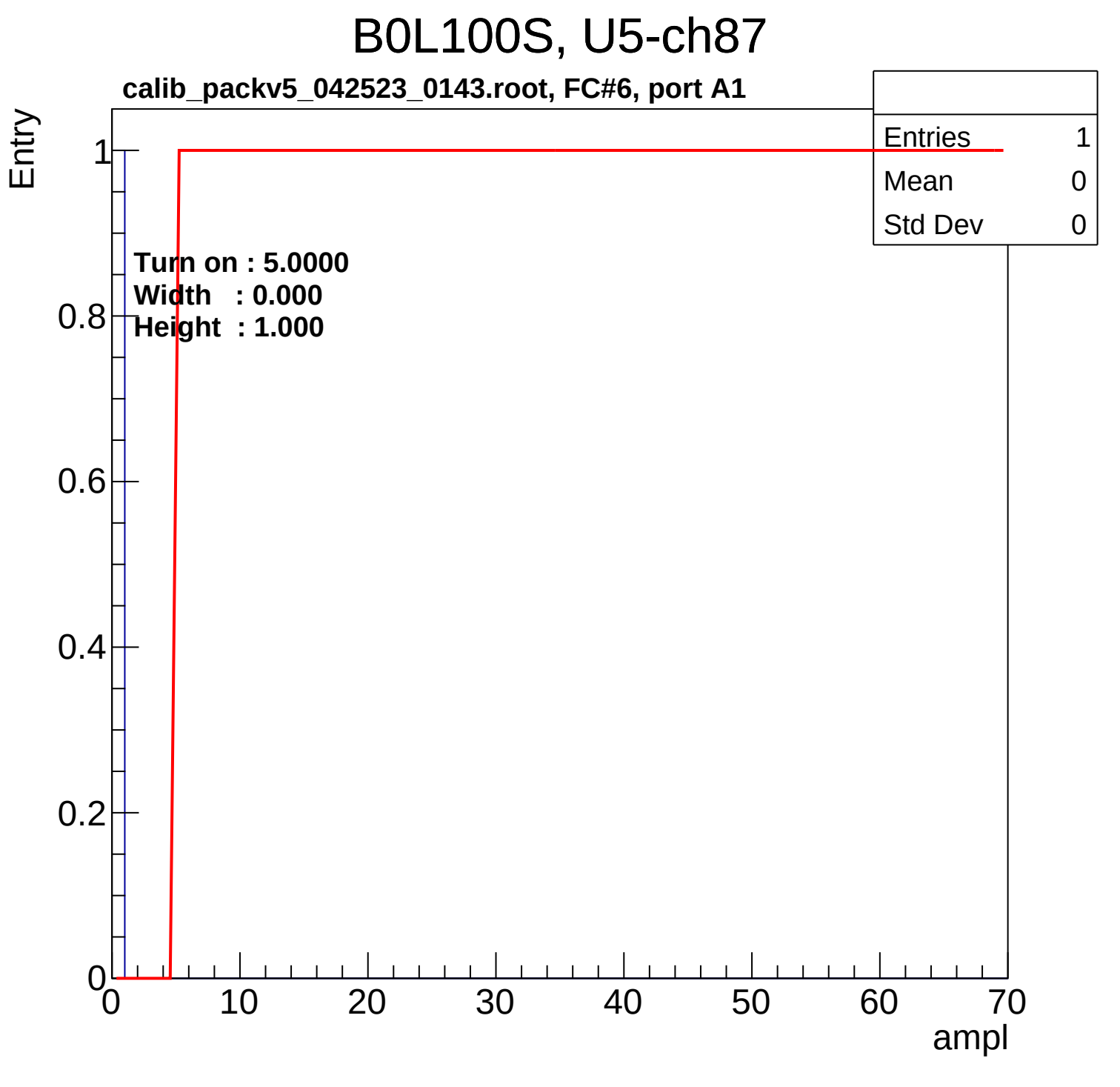

B0L100S, U5-ch82
calib_packv5_042523_0143.root, FC#6, port A1
Entries 21
Mean 46.62
Std Dev 1.214
Turn on : 24.9955
Width : 3.499
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

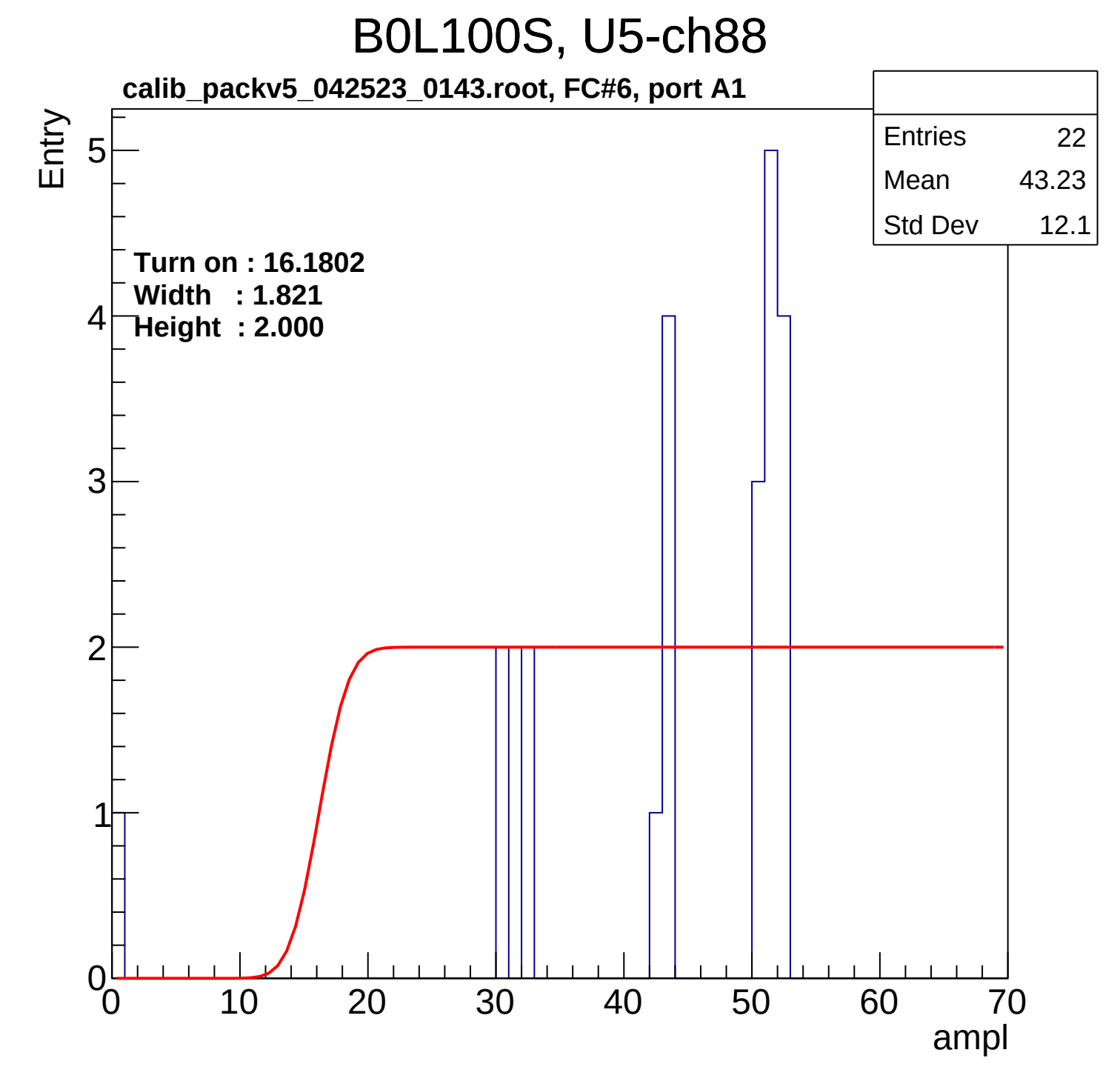

B0L100S, U5-ch83
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

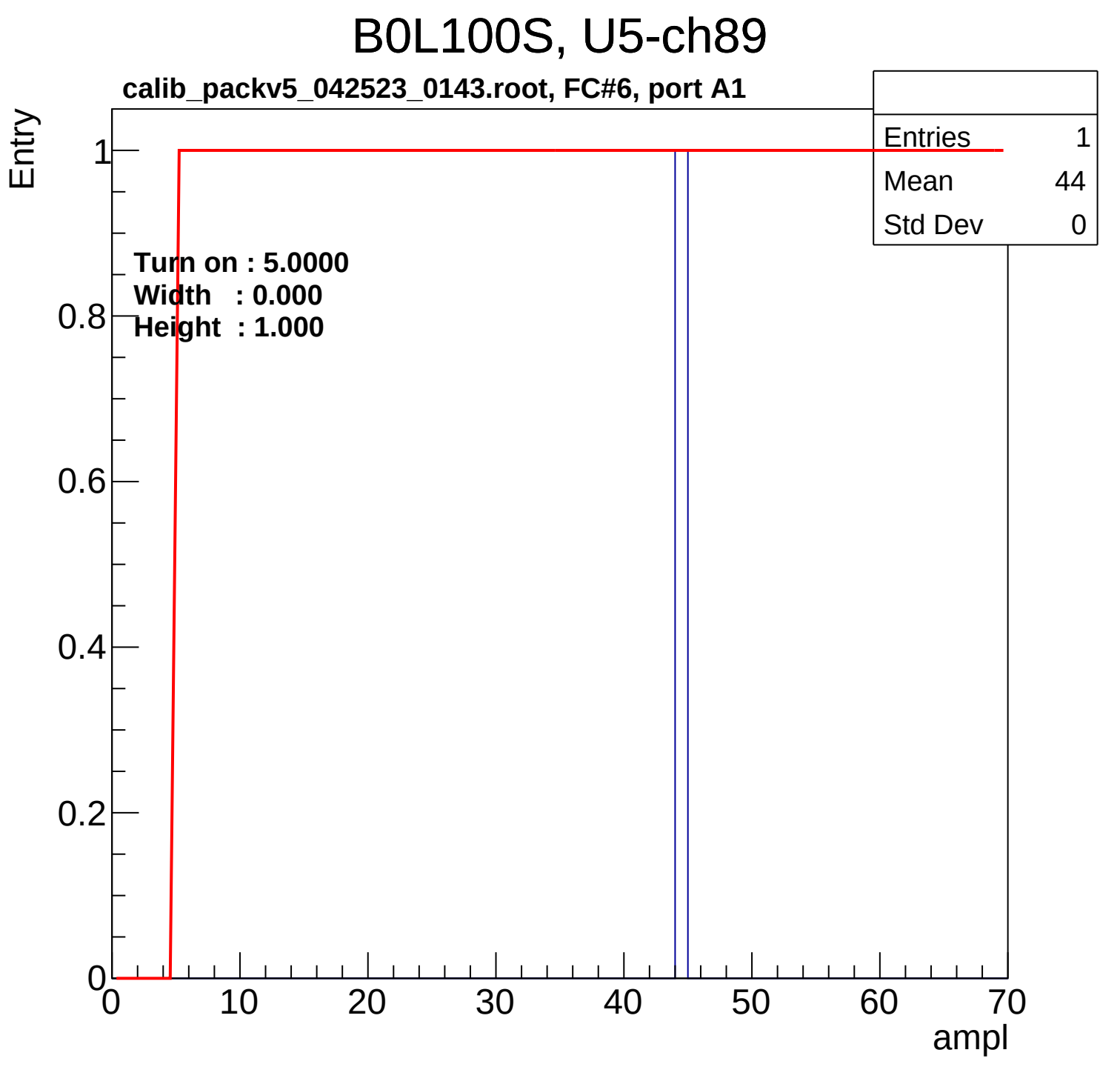

B0L100S, U5-ch84
calib_packv5_042523_0143.root, FC#6, port A1
Entries 29
Mean 45.86
Std Dev 4.577
Turn on : 37.5001
Width : 0.306
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

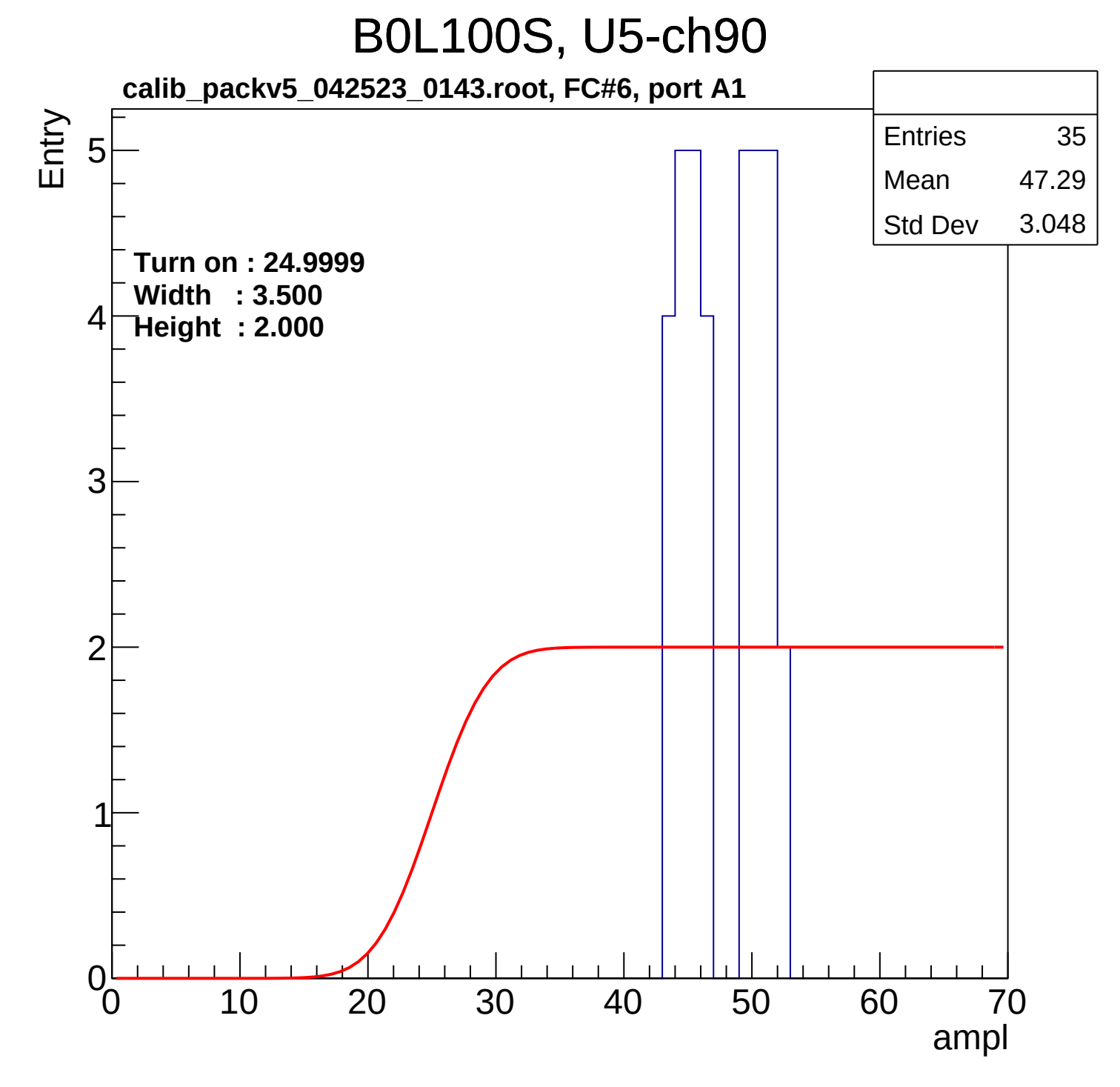

B0L100S, U5-ch85
calib_packv5_042523_0143.root, FC#6, port A1
Entries 43
Mean 49.4
Std Dev 2.507
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

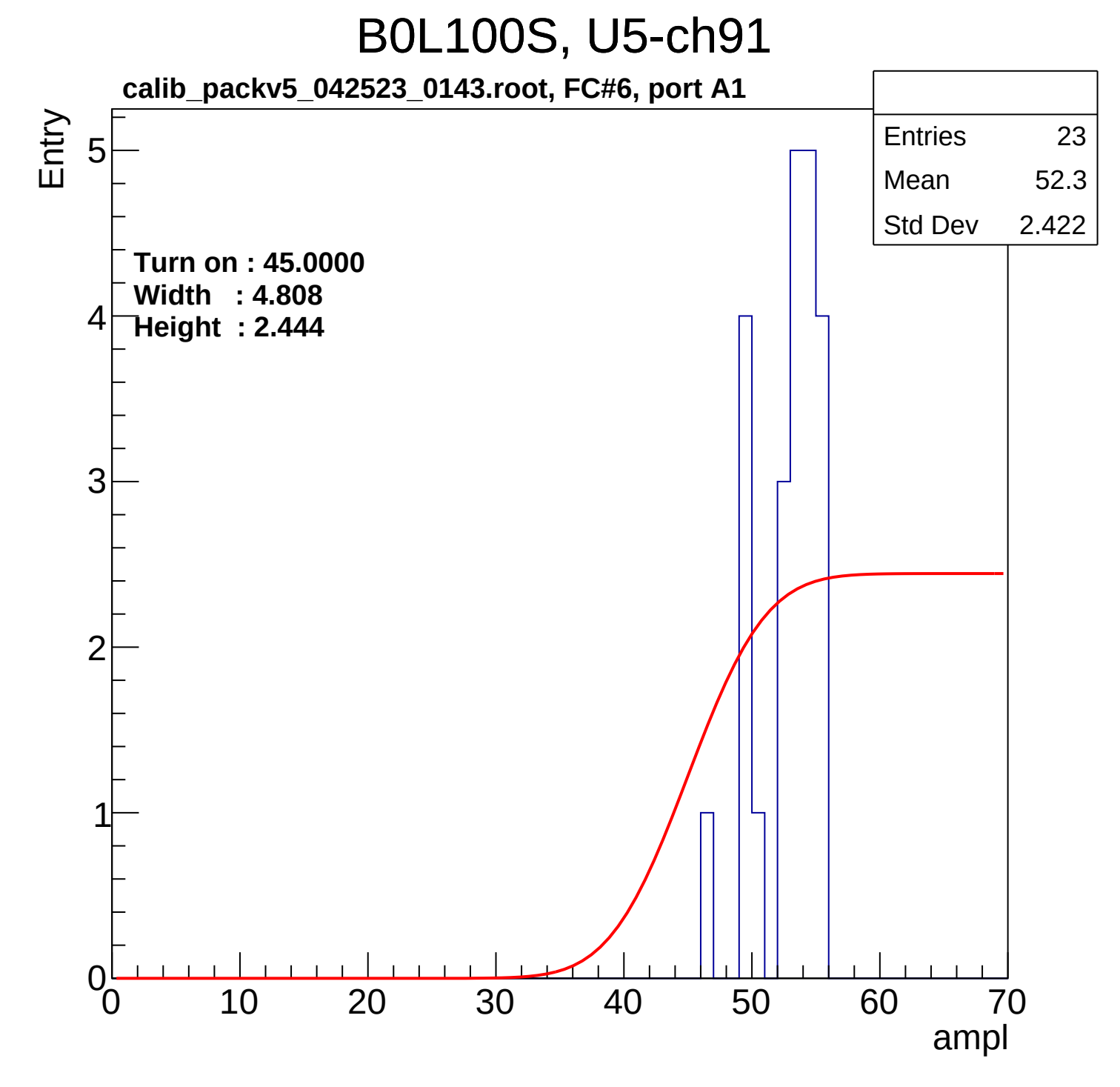

B0L100S, U5-ch86
calib_packv5_042523_0143.root, FC#6, port A1
Entries 14
Mean 49.21
Std Dev 7.504
Turn on : 23.4162
Width : 5.133
Height : 1.973
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

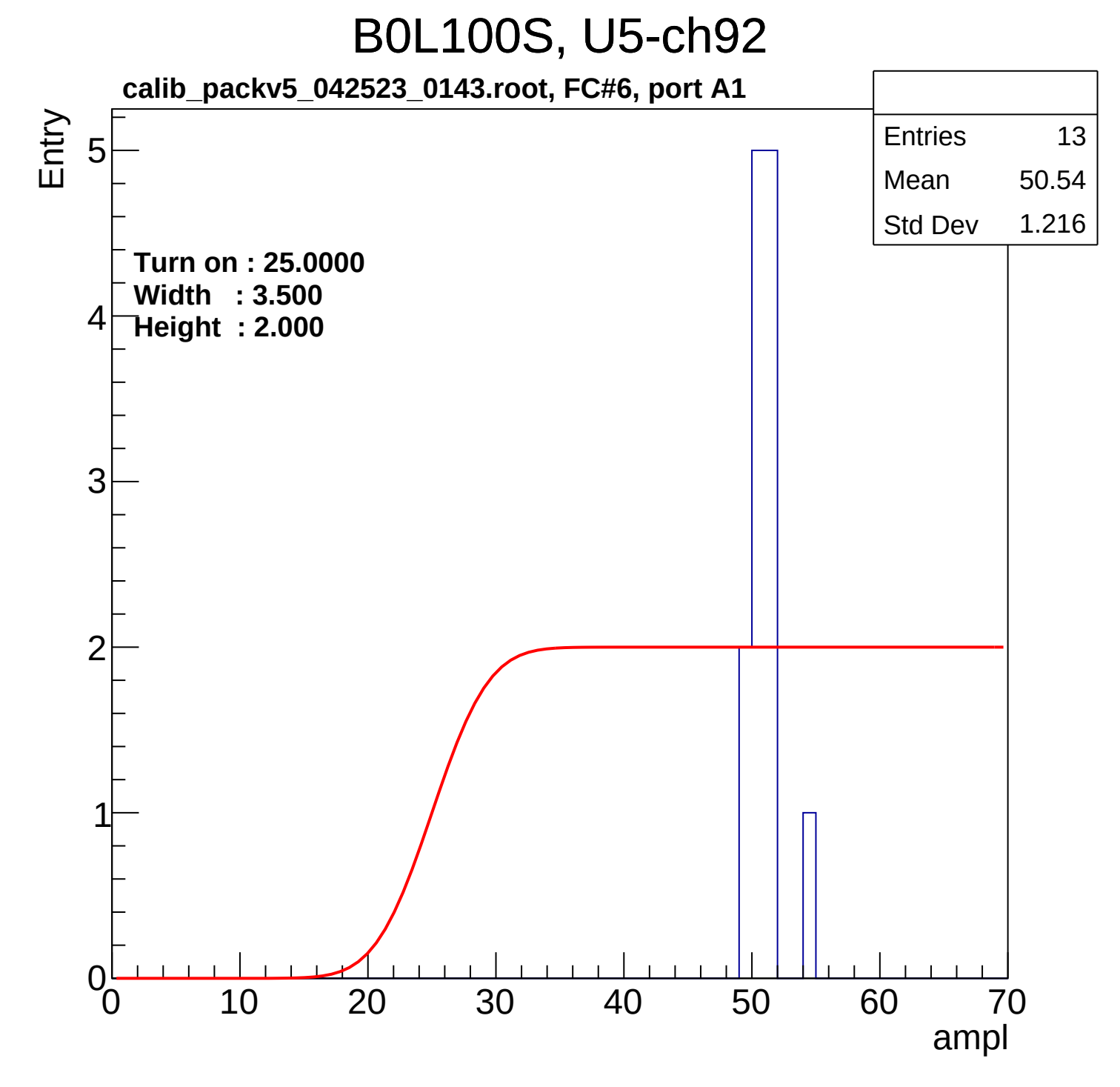

B0L100S, U5-ch87
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

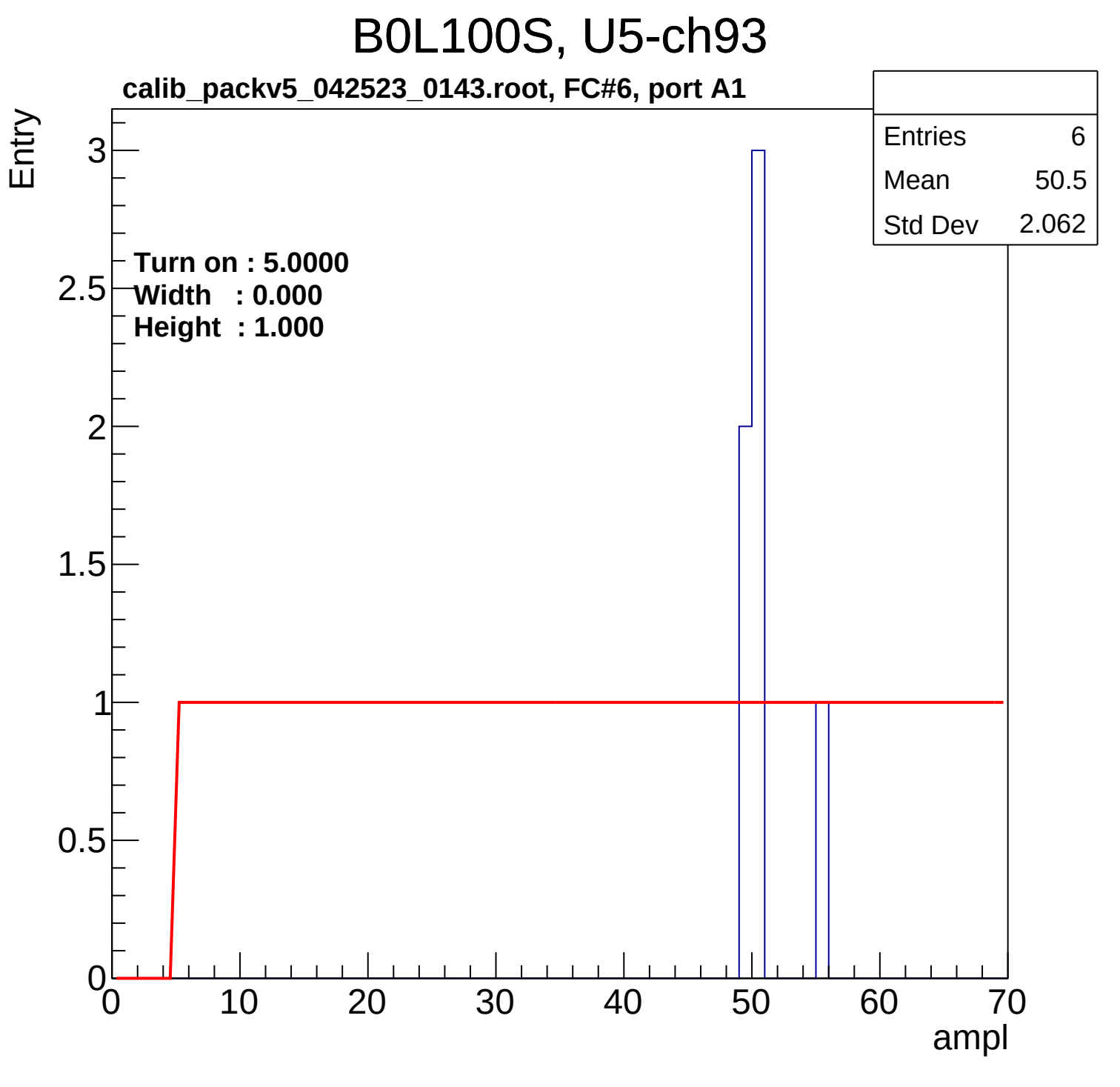

B0L100S, U5-ch88
calib_packv5_042523_0143.root, FC#6, port A1
Entries 22
Mean 43.23
Std Dev 12.1
Turn on : 16.1802
Width : 1.821
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

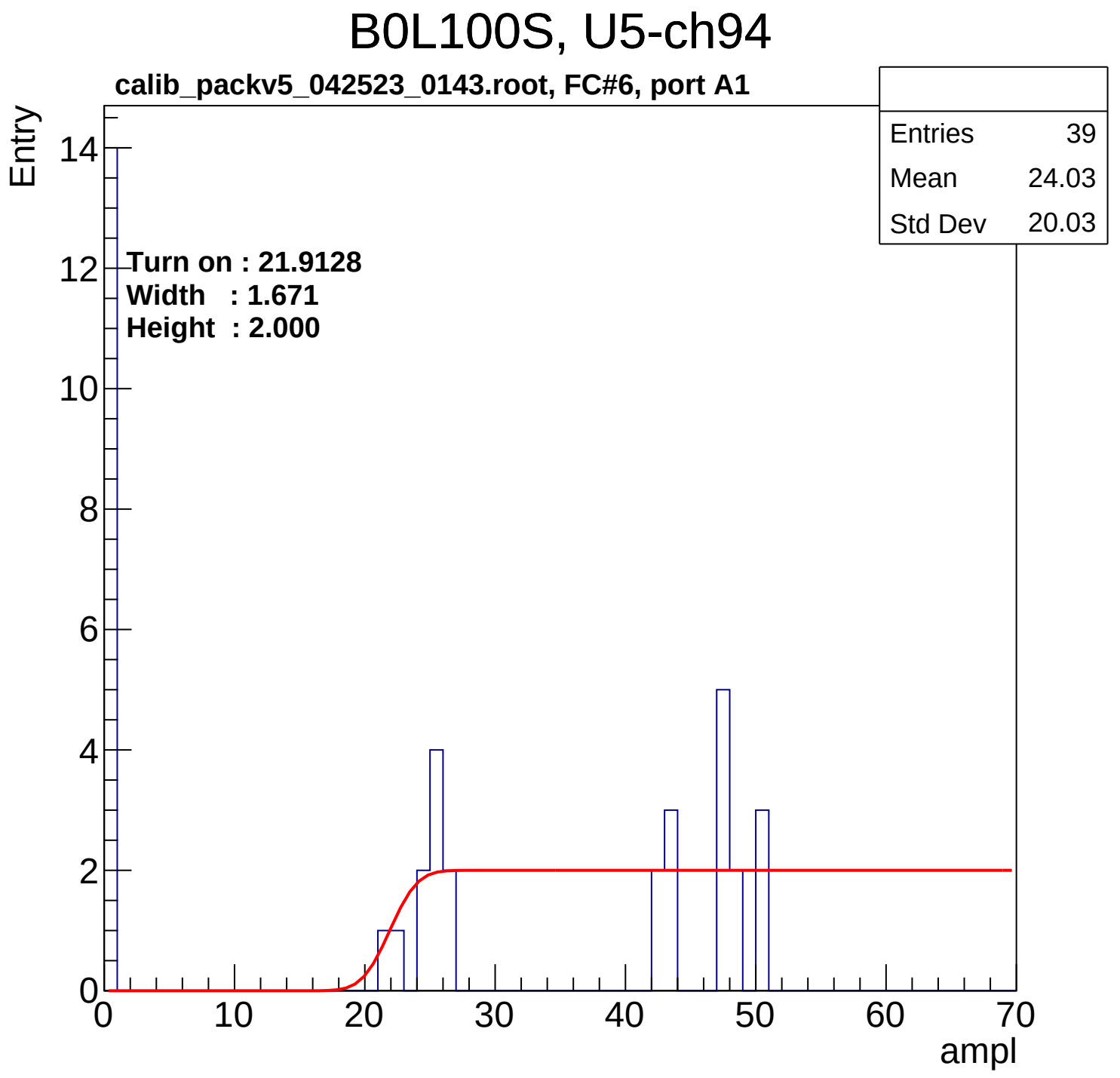

B0L100S, U5-ch89
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 44
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

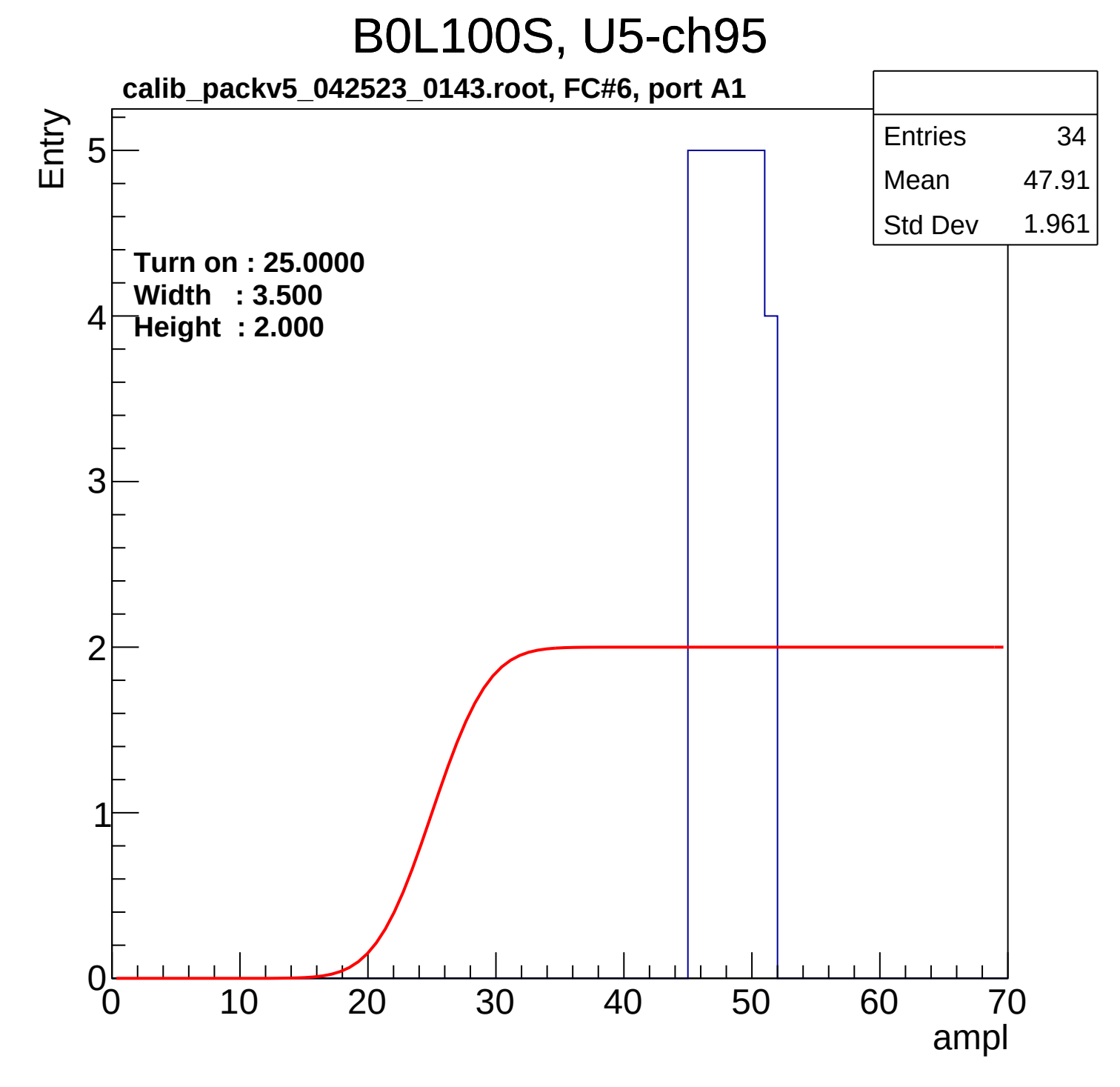

B0L100S, U5-ch90
calib_packv5_042523_0143.root, FC#6, port A1
Entries 35
Mean 47.29
Std Dev 3.048
Turn on : 24.9999
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

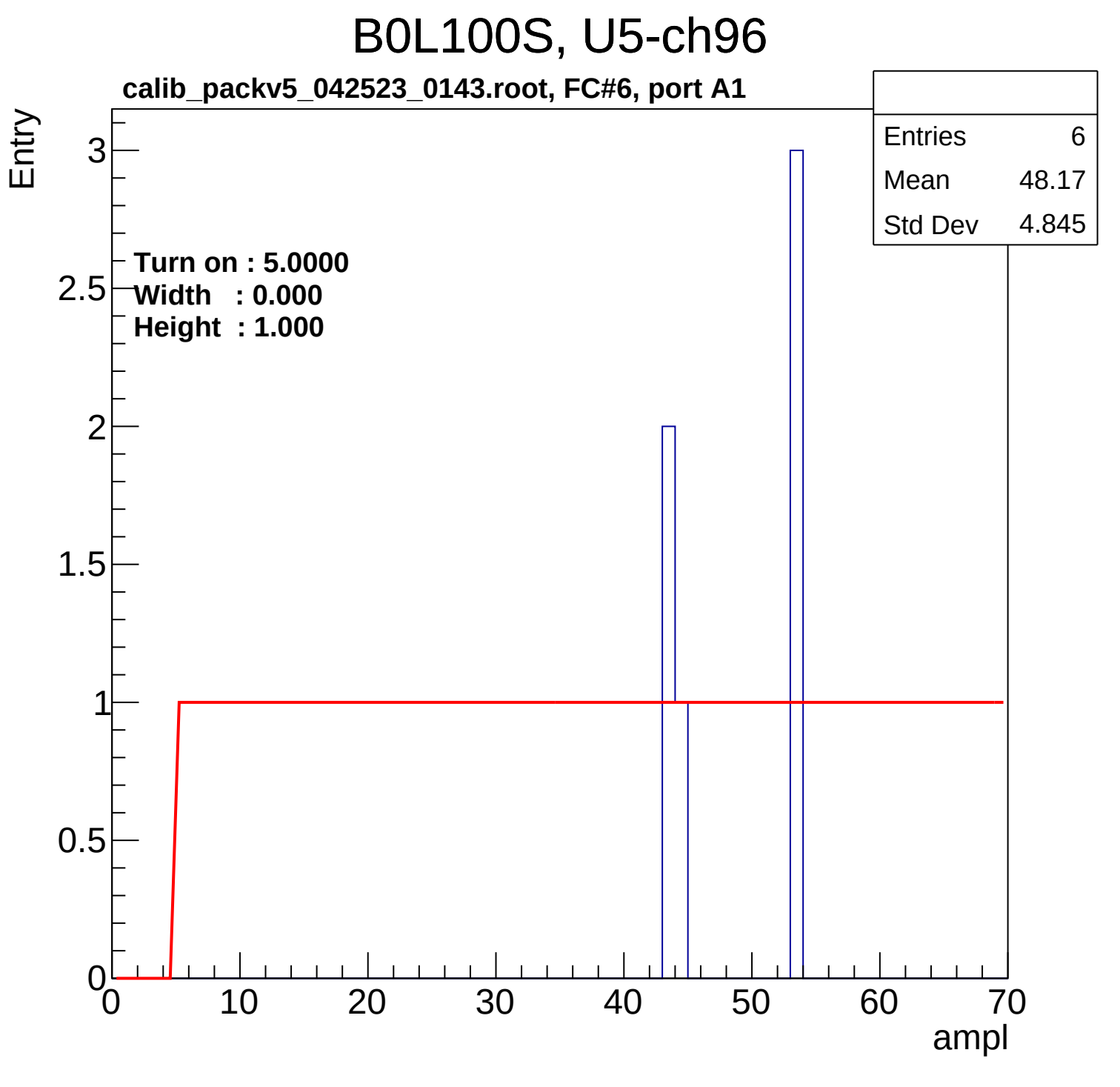

B0L100S, U5-ch91
calib_packv5_042523_0143.root, FC#6, port A1
Entries 23
Mean 52.3
Std Dev 2.422
Turn on : 45.0000
Width : 4.808
Height : 2.444
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

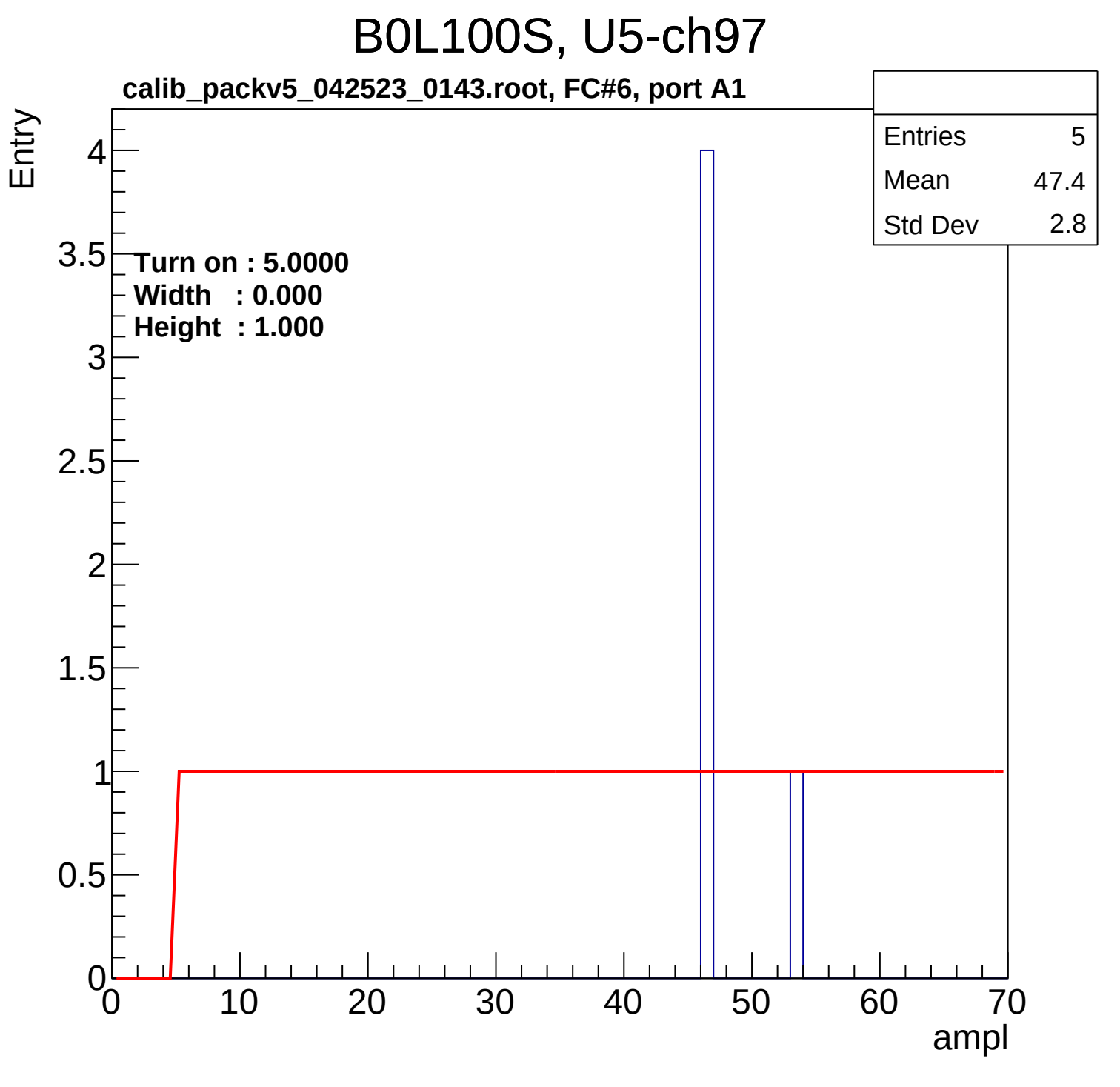

B0L100S, U5-ch92
calib_packv5_042523_0143.root, FC#6, port A1
Entries 13
Mean 50.54
Std Dev 1.216
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

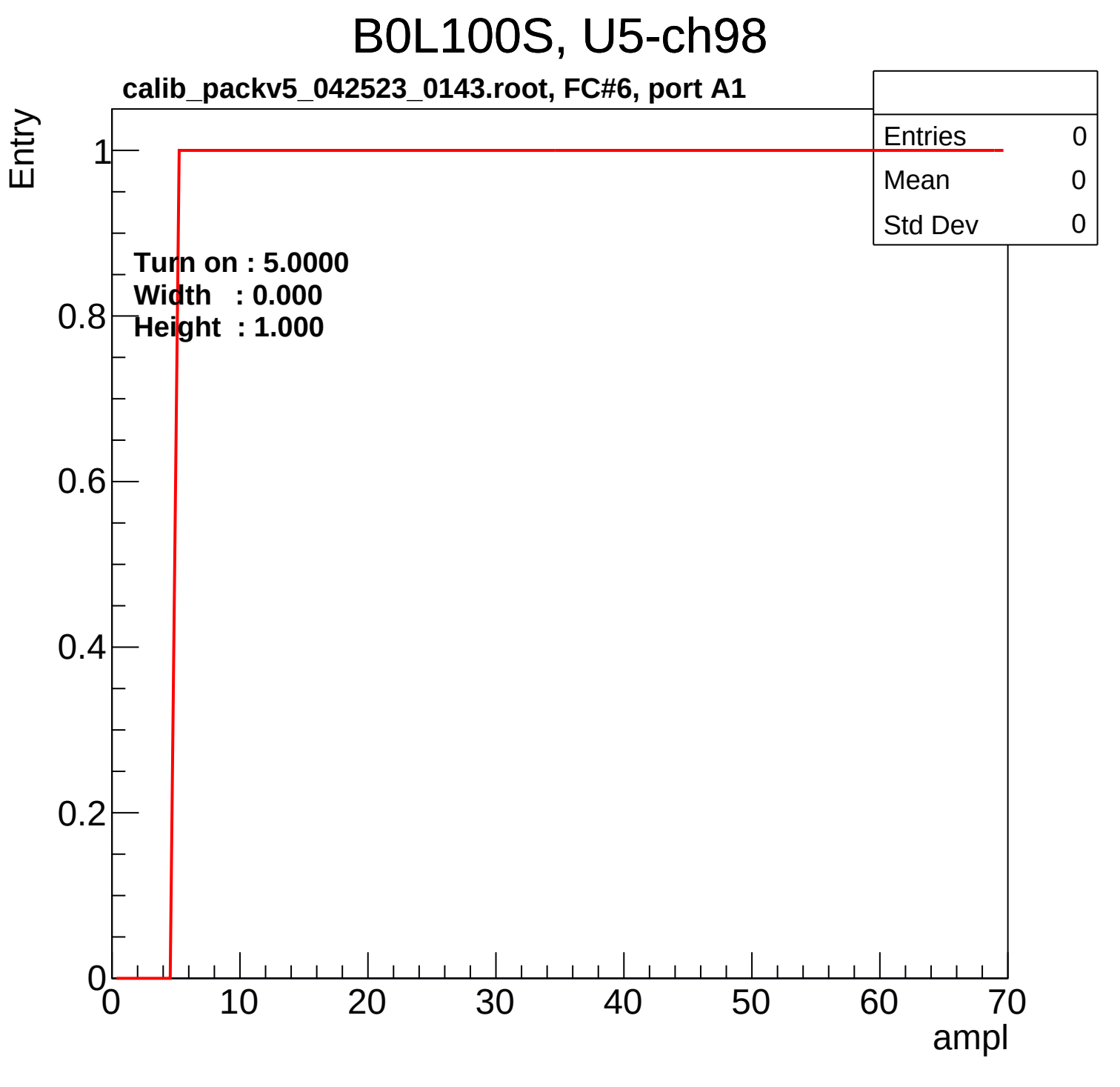

B0L100S, U5-ch93
calib_packv5_042523_0143.root, FC#6, port A1
Entries 6
Mean 50.5
Std Dev 2.062
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

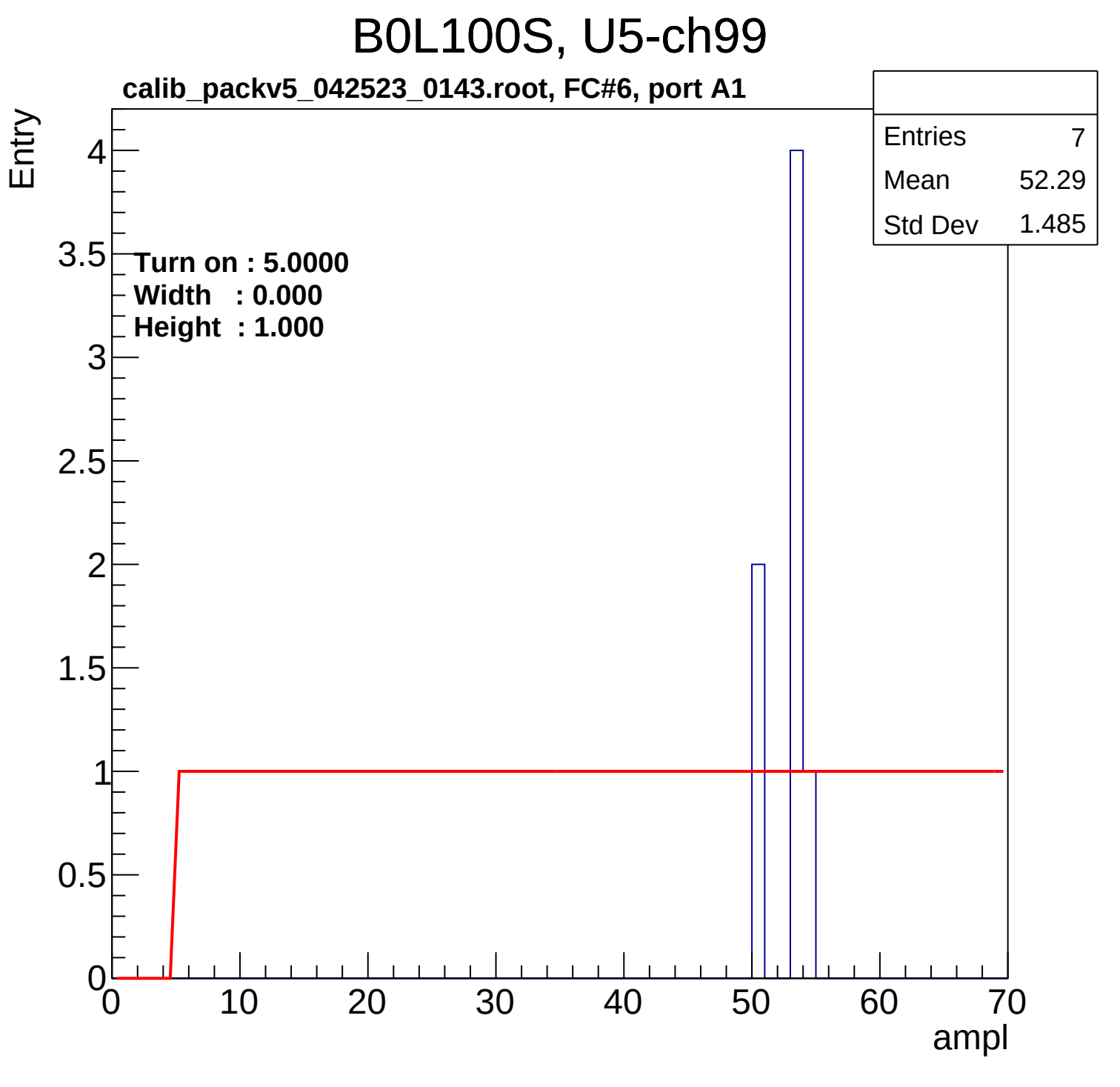

B0L100S, U5-ch94
calib_packv5_042523_0143.root, FC#6, port A1
Entries 39
Mean 24.03
Std Dev 20.03
Turn on : 21.9128
Width : 1.671
Height : 2.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

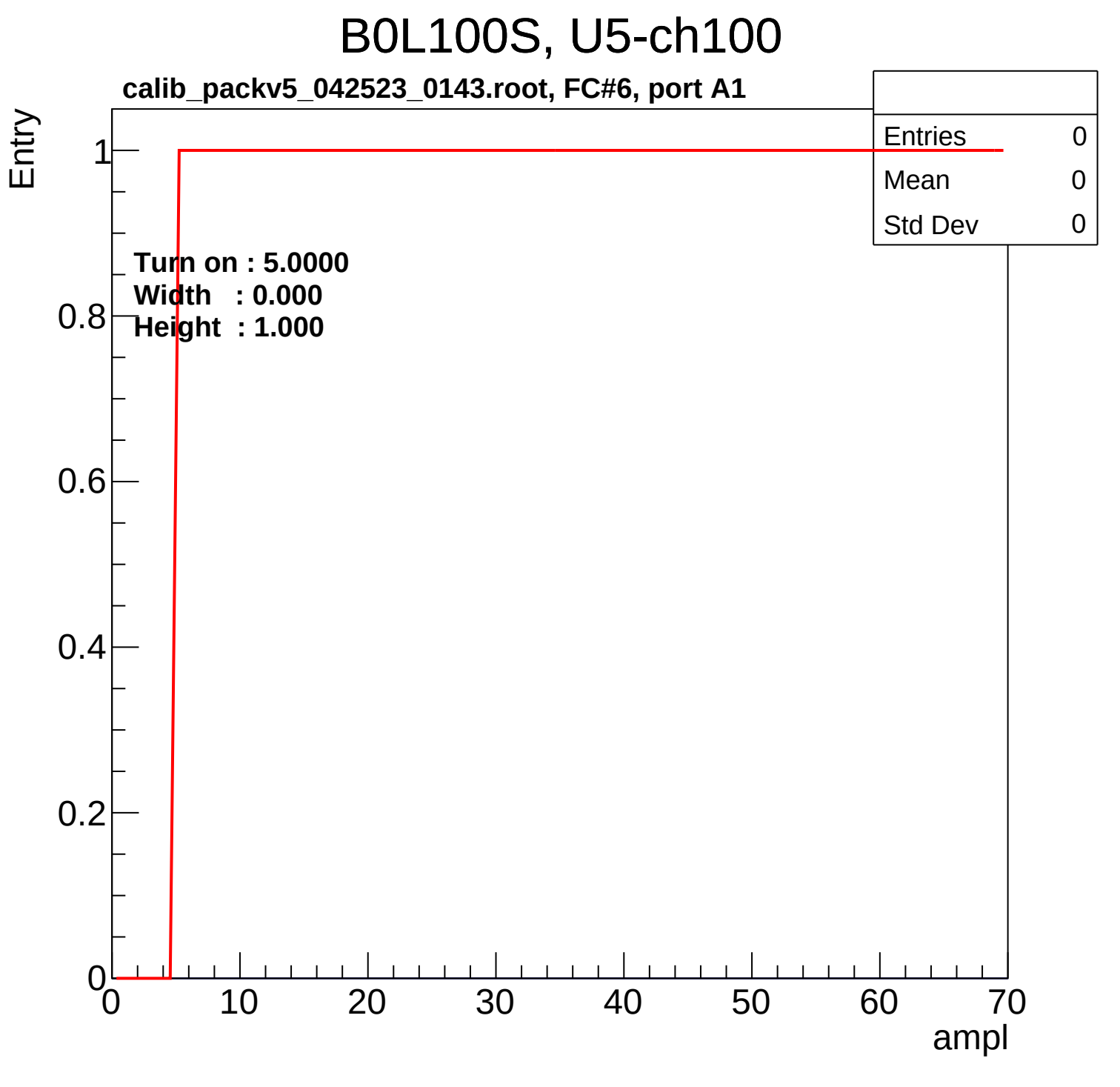

B0L100S, U5-ch95
calib_packv5_042523_0143.root, FC#6, port A1
Entries 34
Mean 47.91
Std Dev 1.961
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

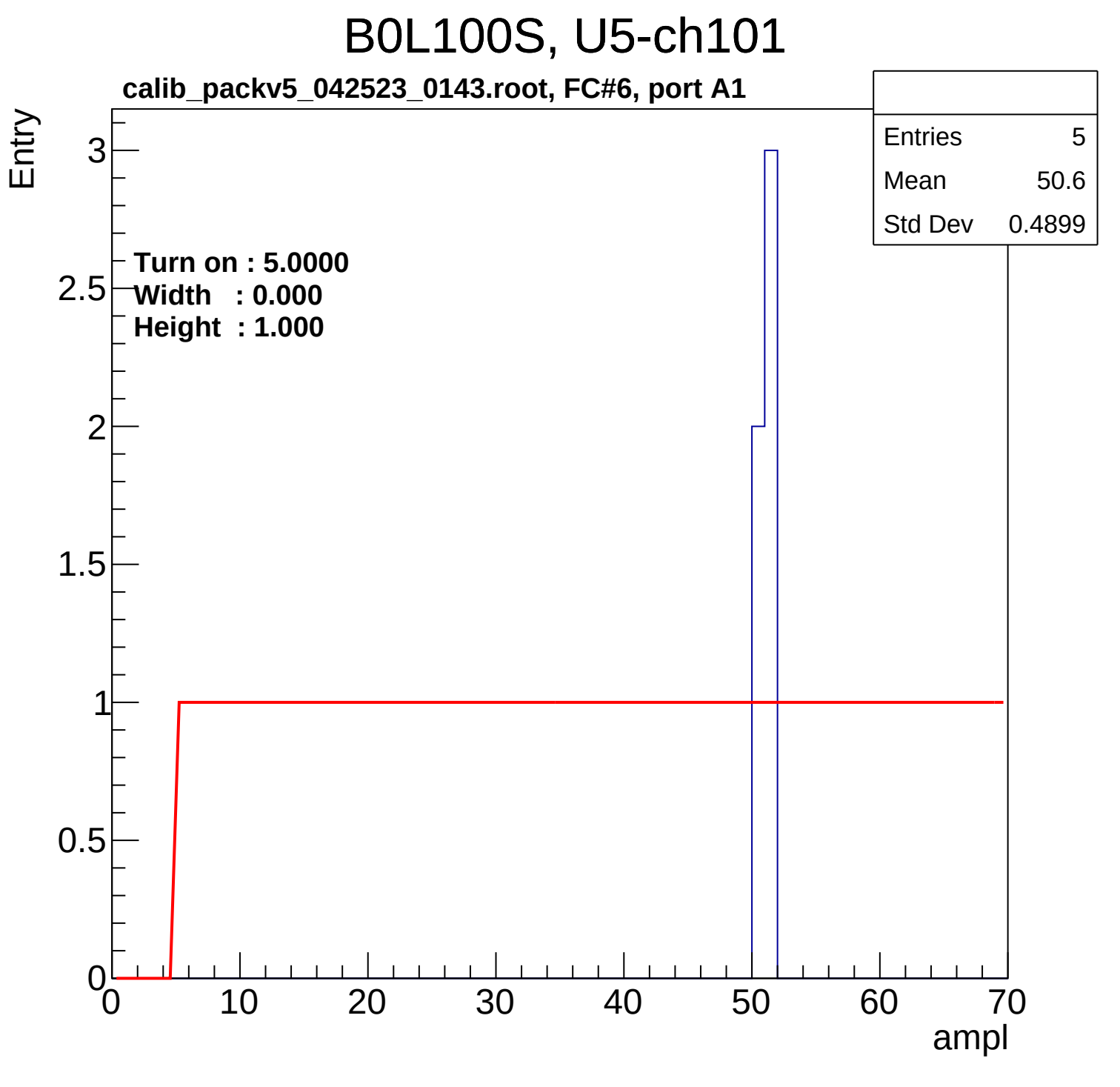

B0L100S, U5-ch96
calib_packv5_042523_0143.root, FC#6, port A1
Entries 6
Mean 48.17
Std Dev 4.845
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

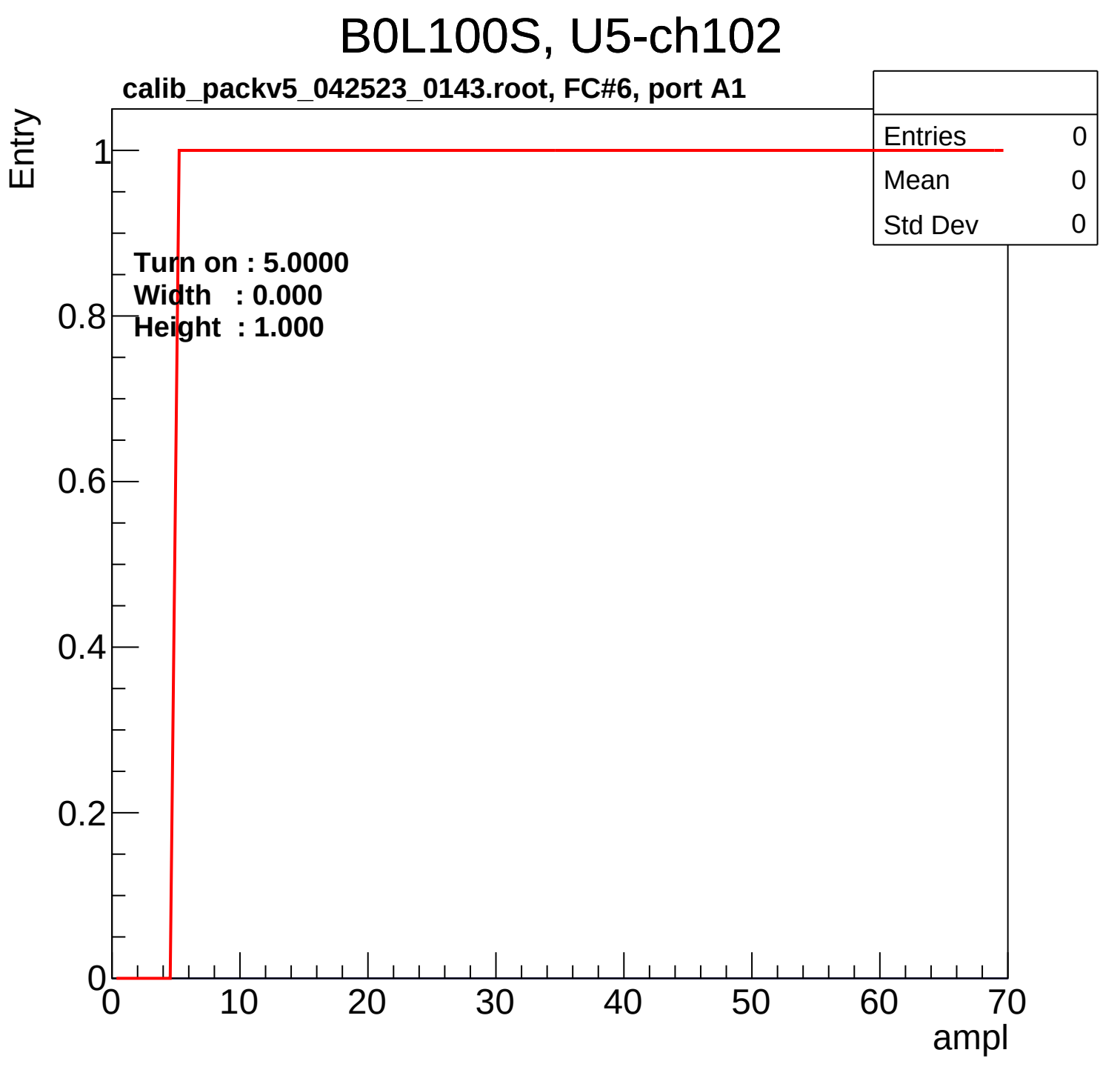

B0L100S, U5-ch97
calib_packv5_042523_0143.root, FC#6, port A1
Entries 5
Mean 47.4
Std Dev 2.8
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

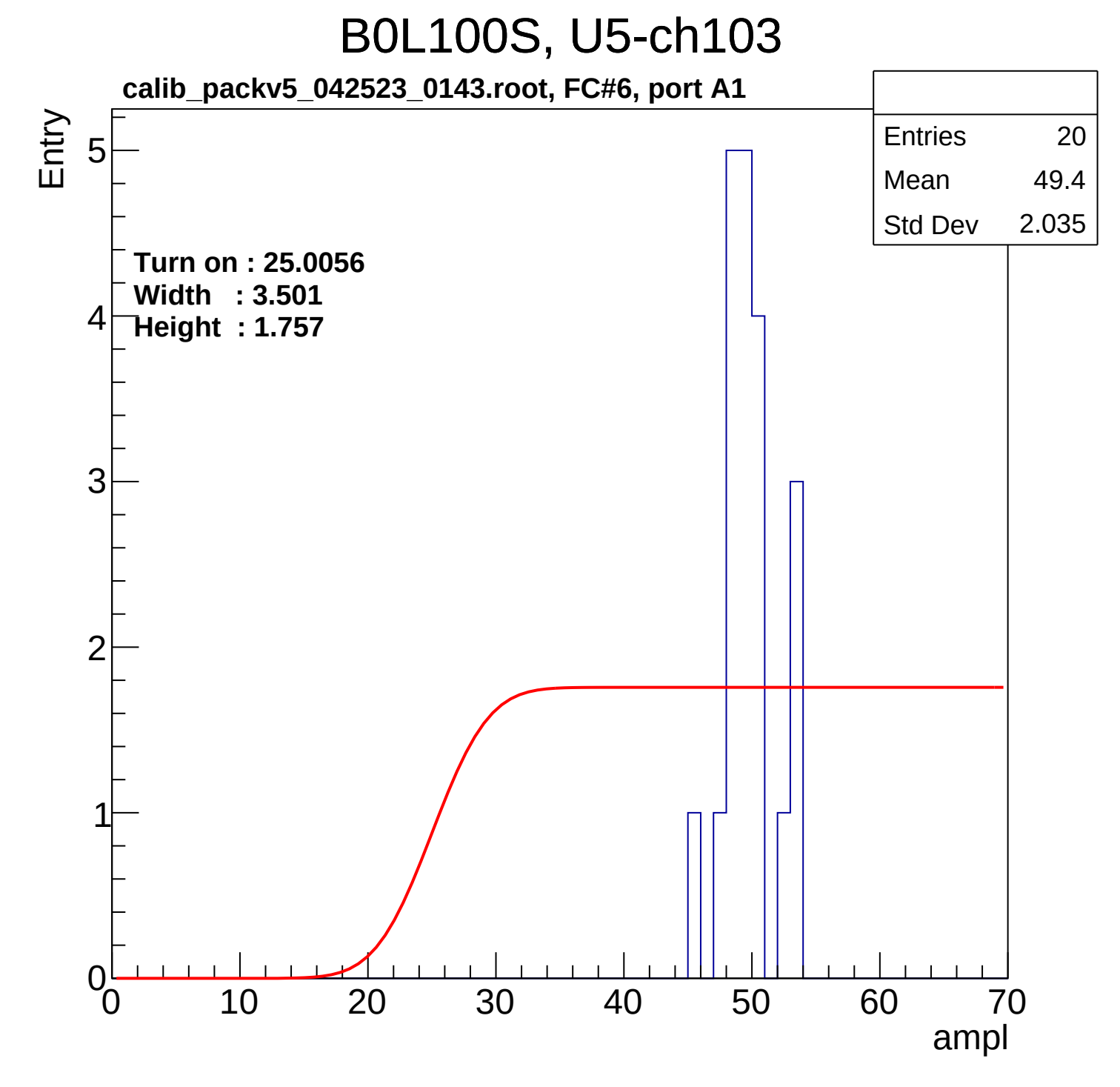

B0L100S, U5-ch98
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

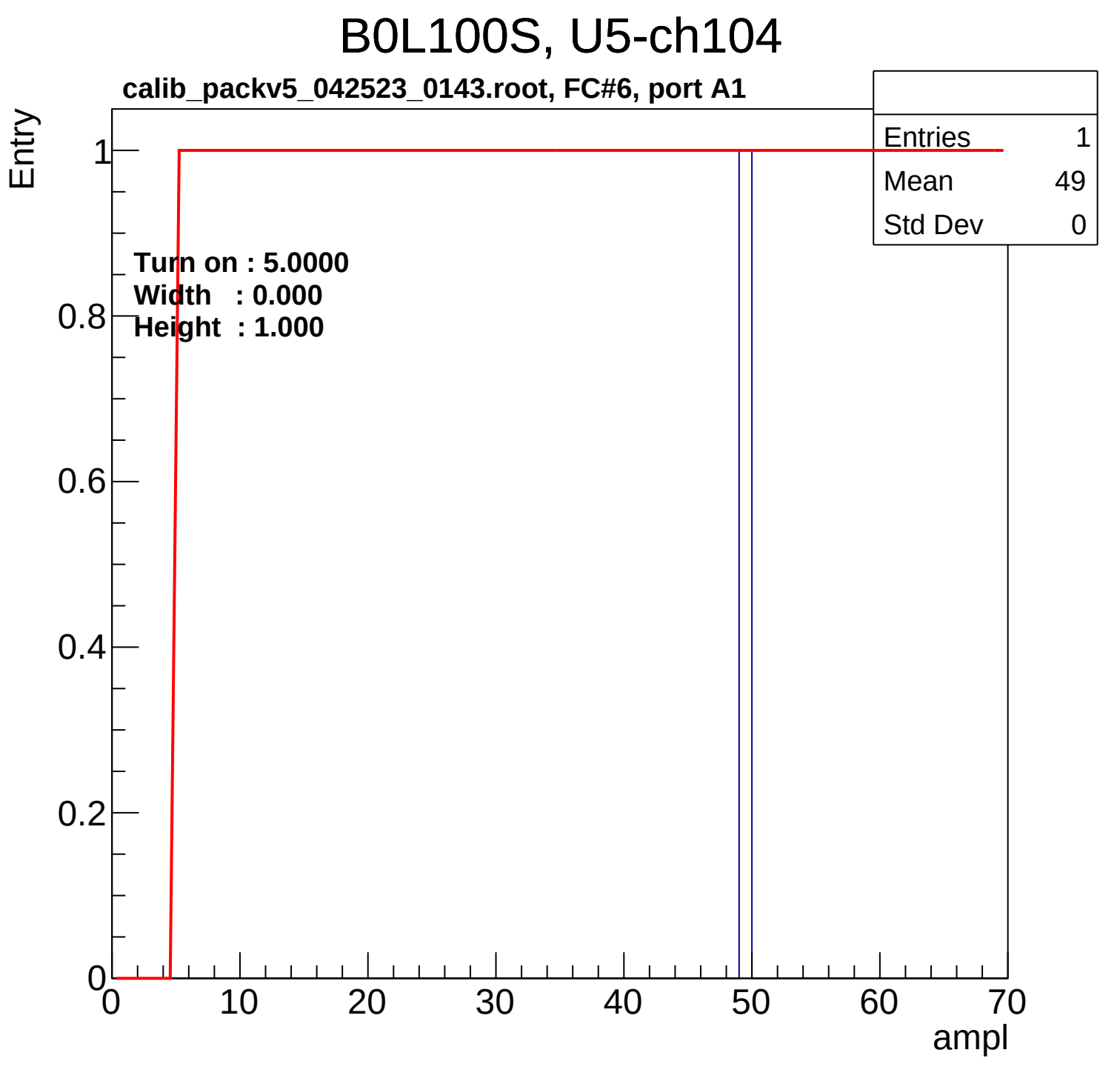

B0L100S, U5-ch99
calib_packv5_042523_0143.root, FC#6, port A1
Entries 7
Mean 52.29
Std Dev 1.485
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

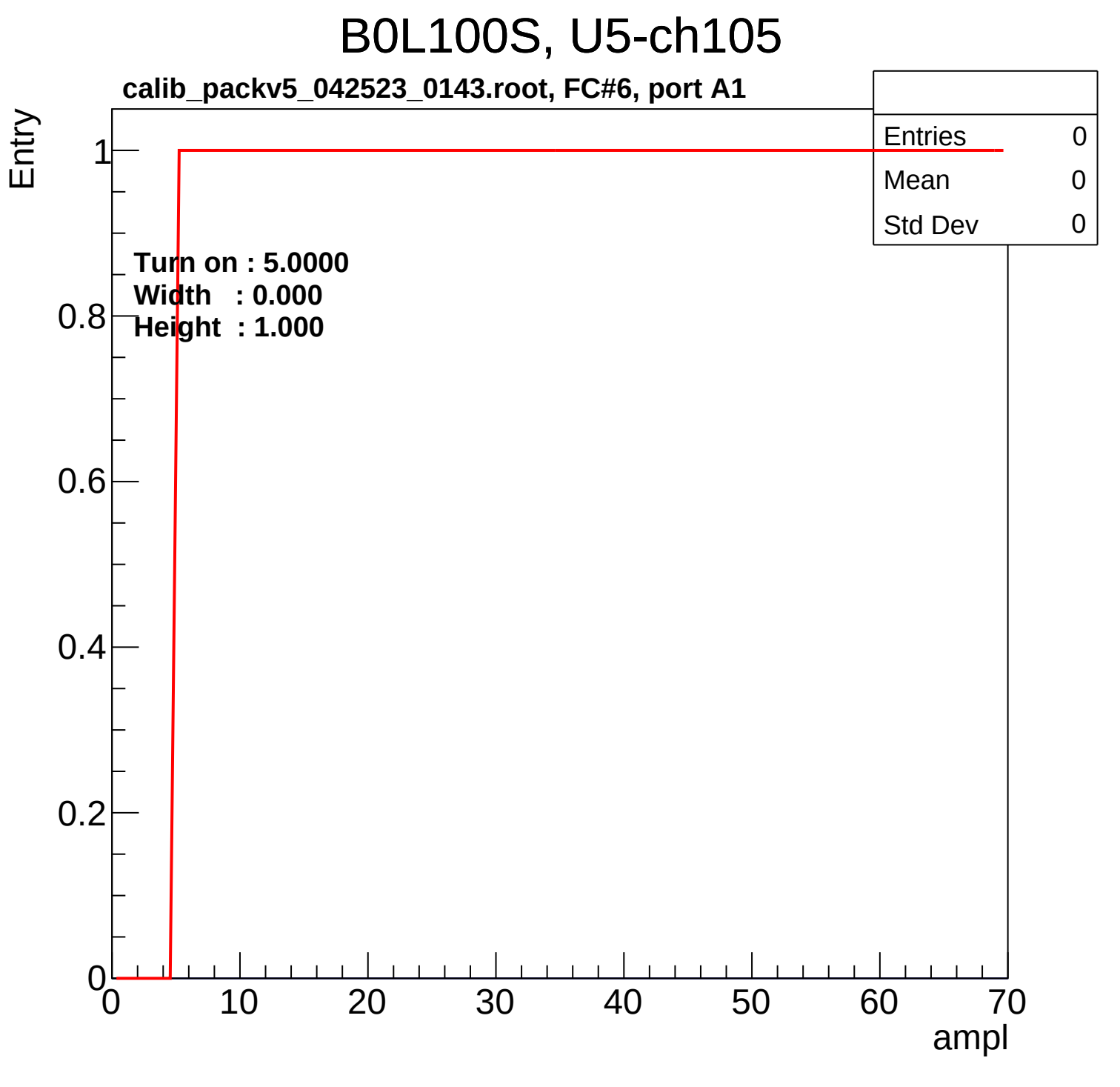

B0L100S, U5-ch100
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

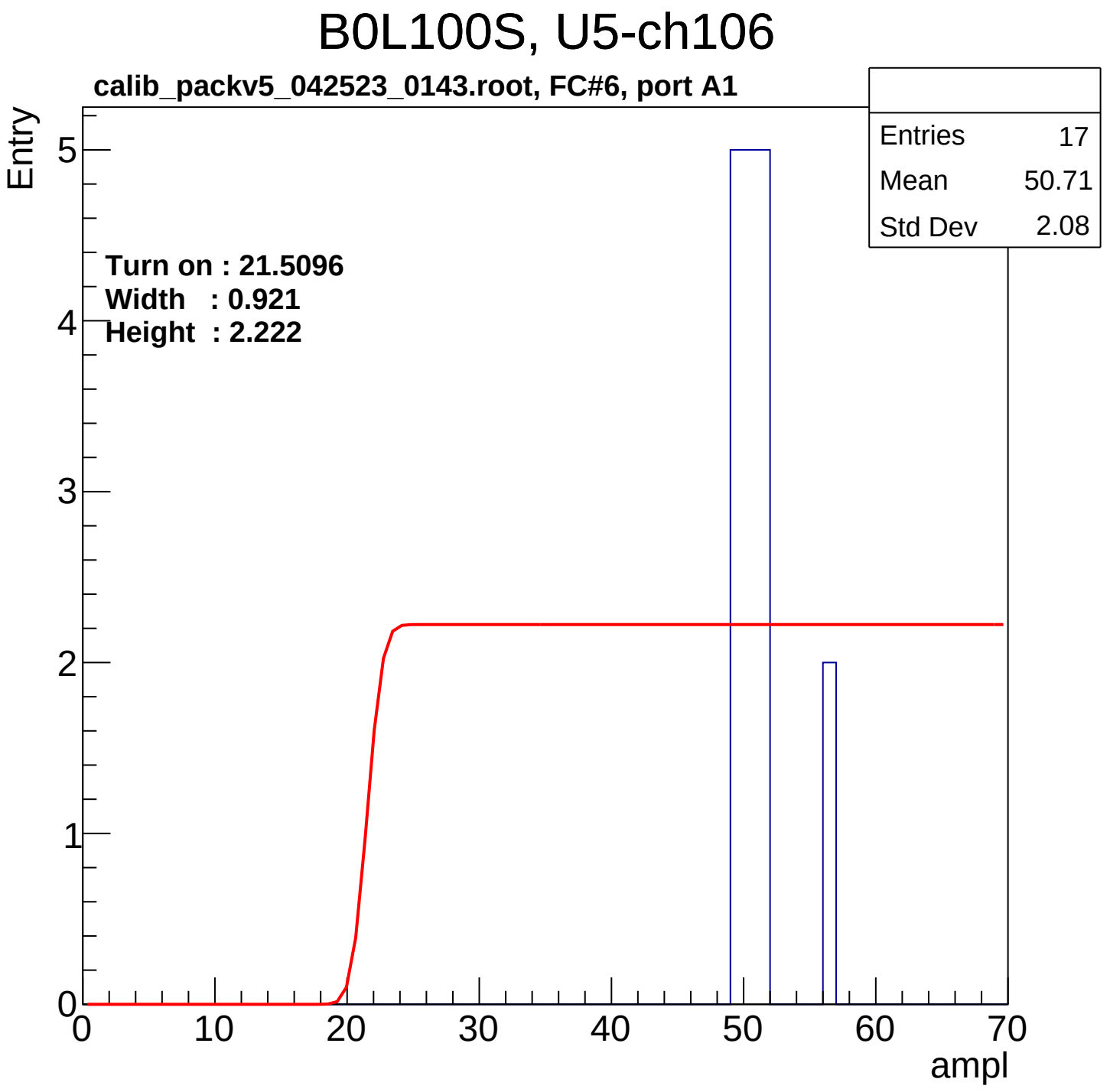

B0L100S, U5-ch101
calib_packv5_042523_0143.root, FC#6, port A1
Entries 5
Mean 50.6
Std Dev 0.4899
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

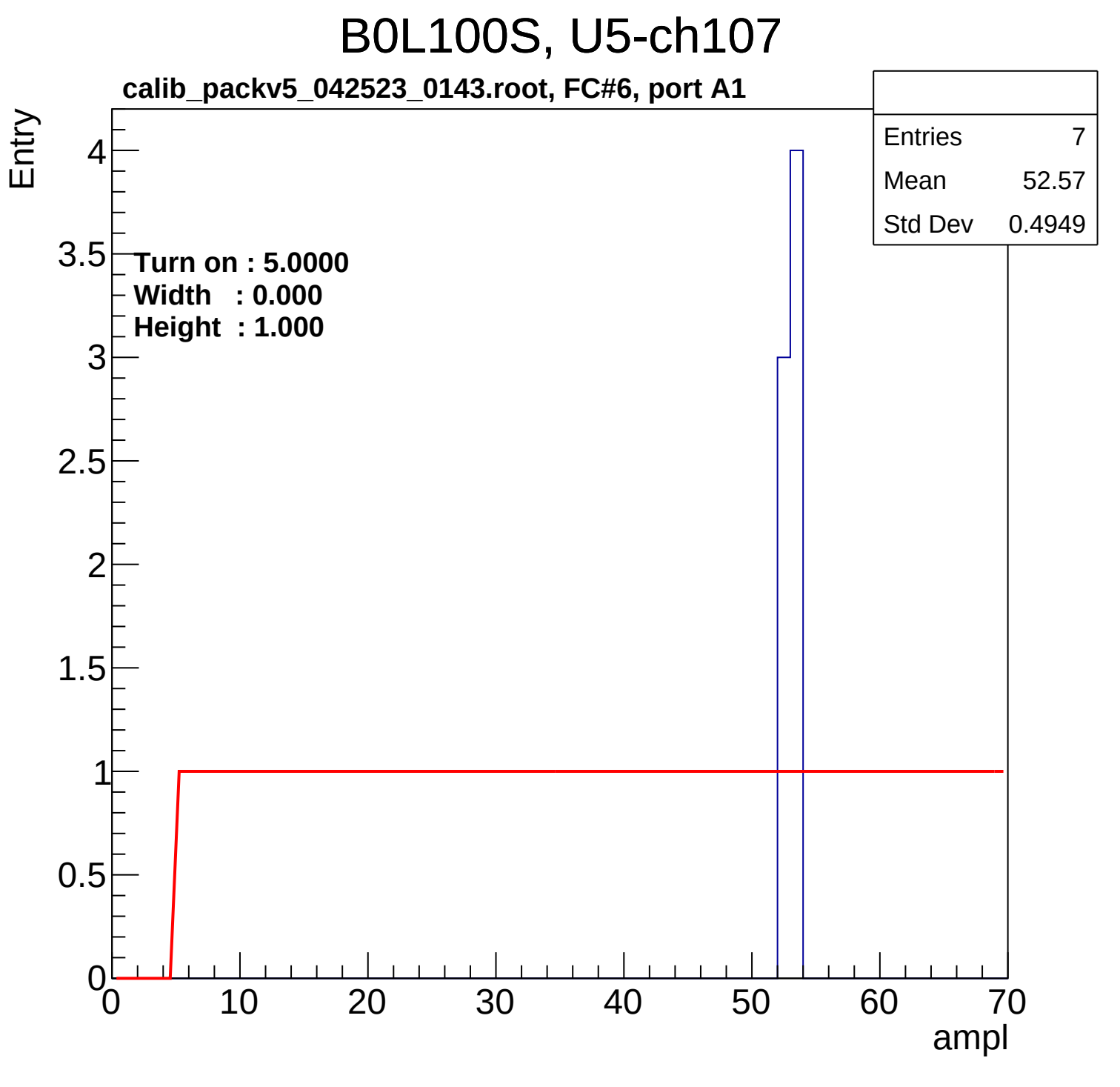

B0L100S, U5-ch102
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

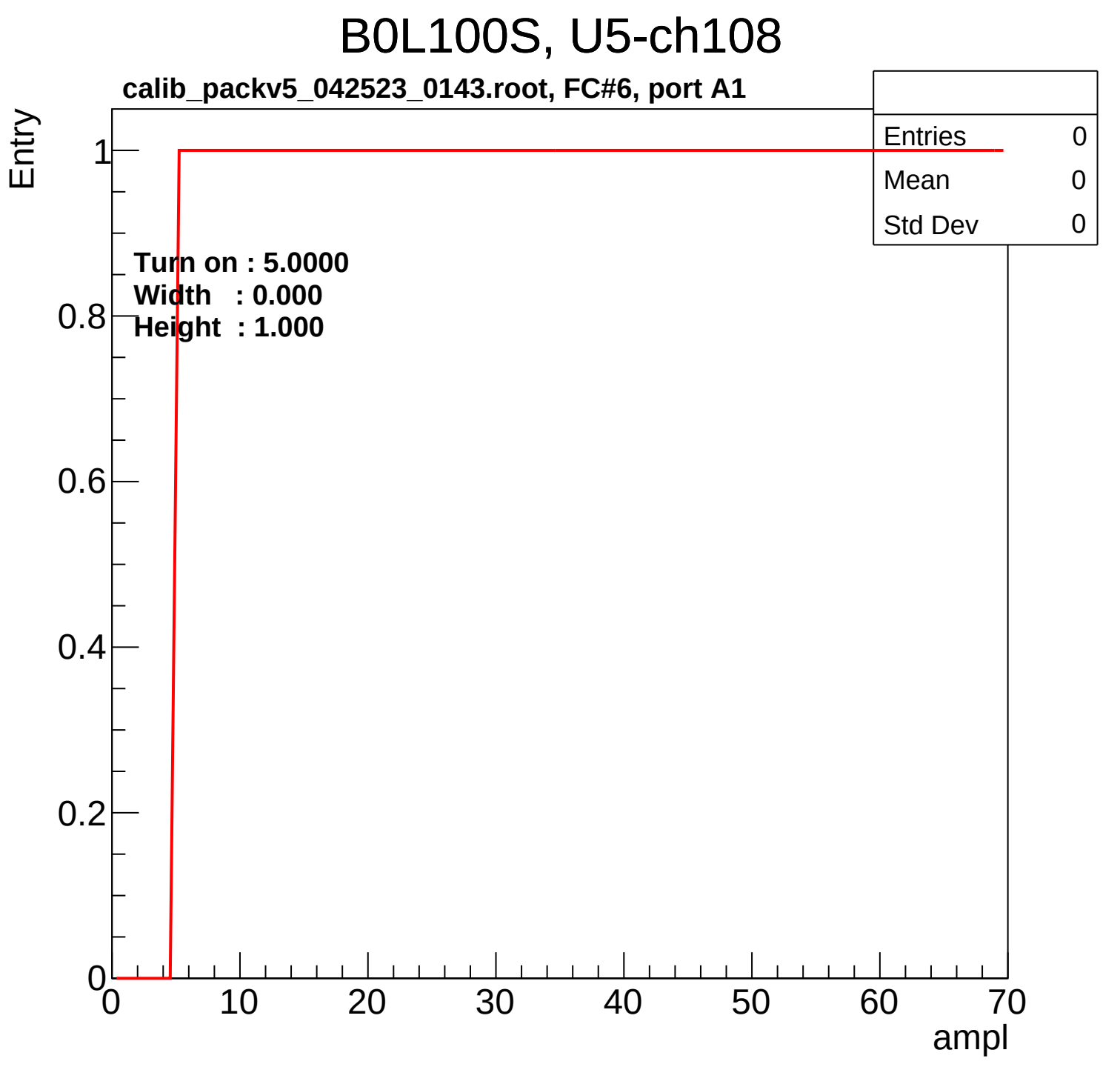

B0L100S, U5-ch103
calib_packv5_042523_0143.root, FC#6, port A1
Entries 20
Mean 49.4
Std Dev 2.035
Turn on : 25.0056
Width : 3.501
Height : 1.757
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

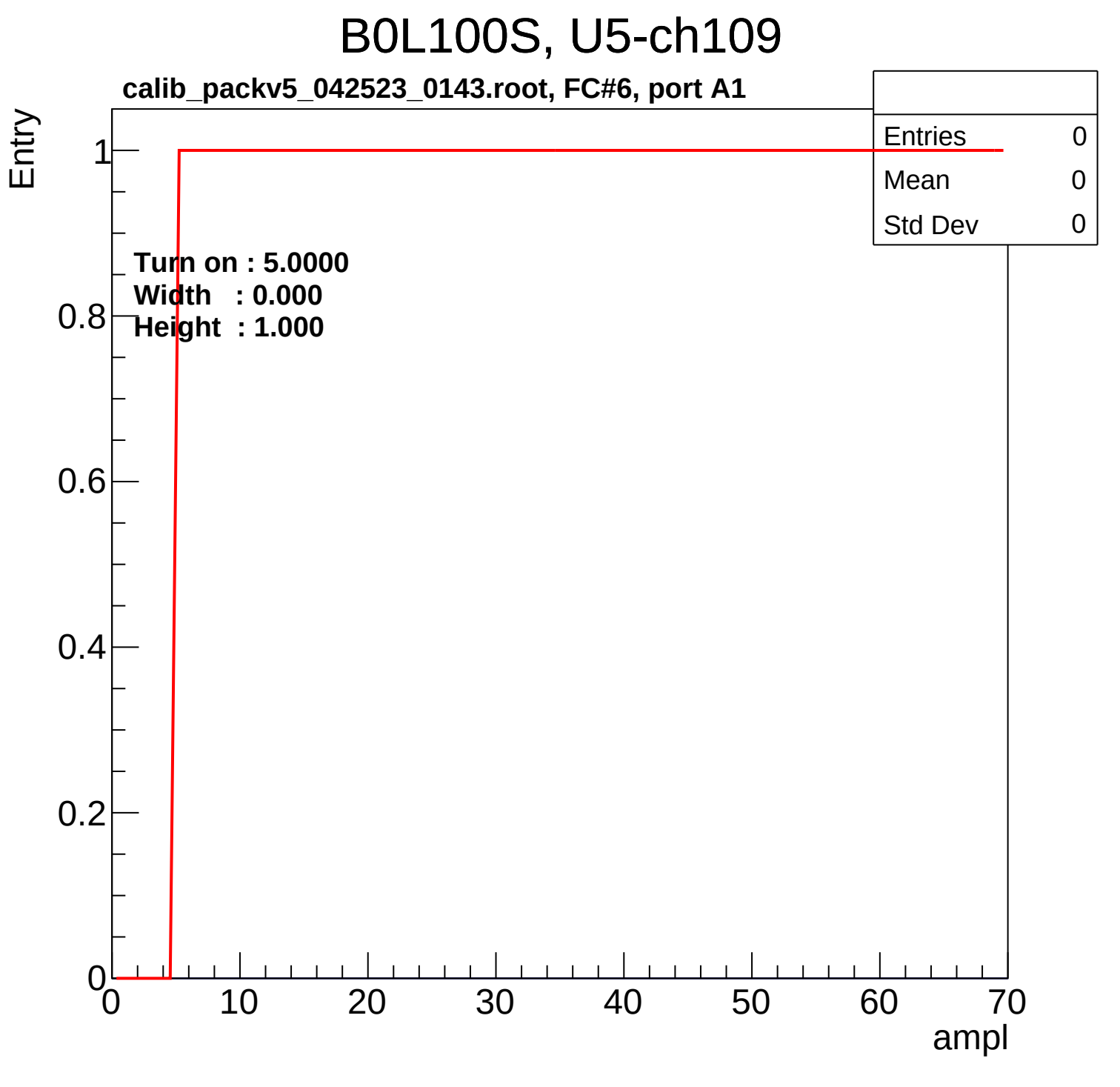

B0L100S, U5-ch104
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 49
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

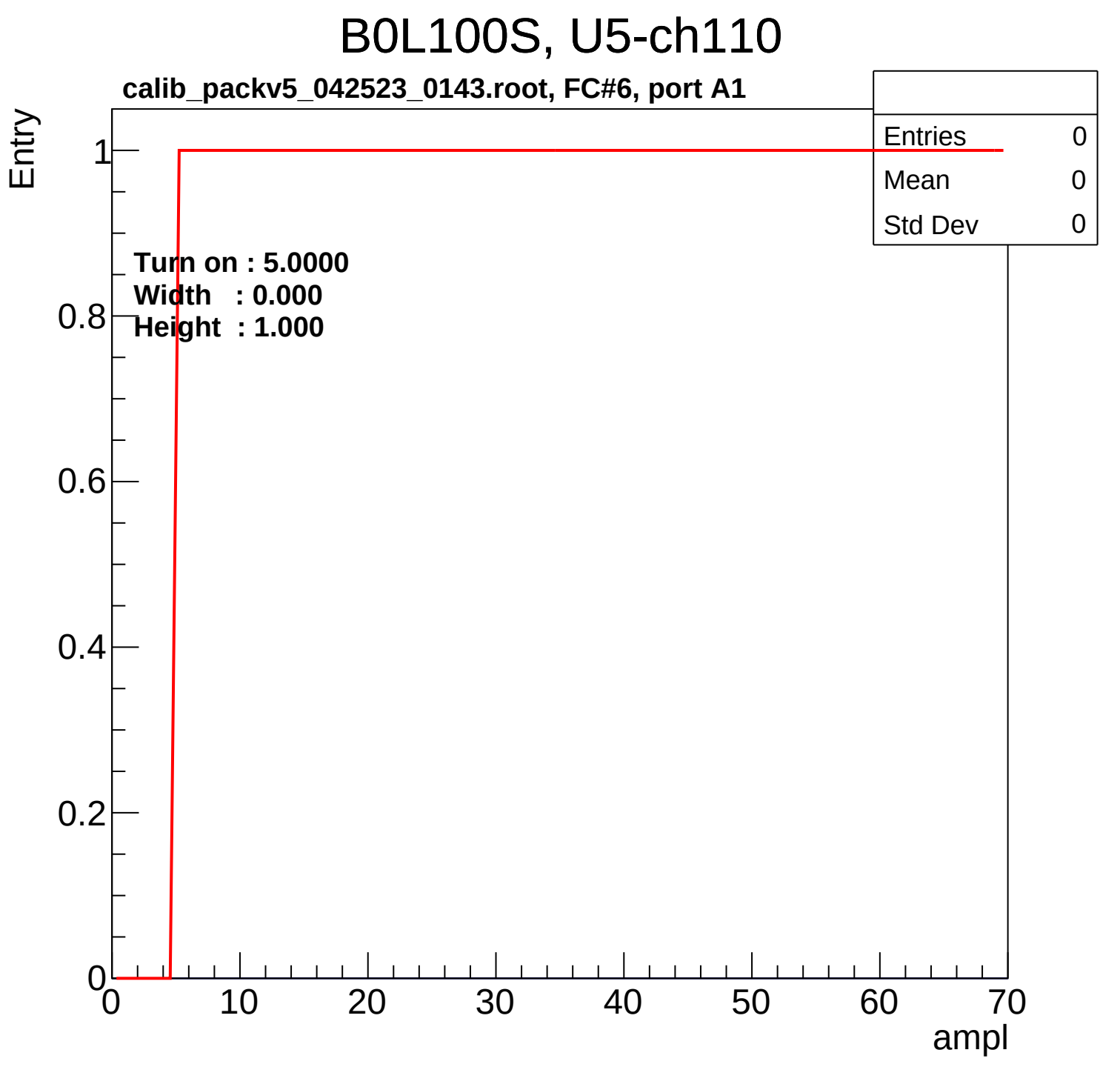

B0L100S, U5-ch105
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

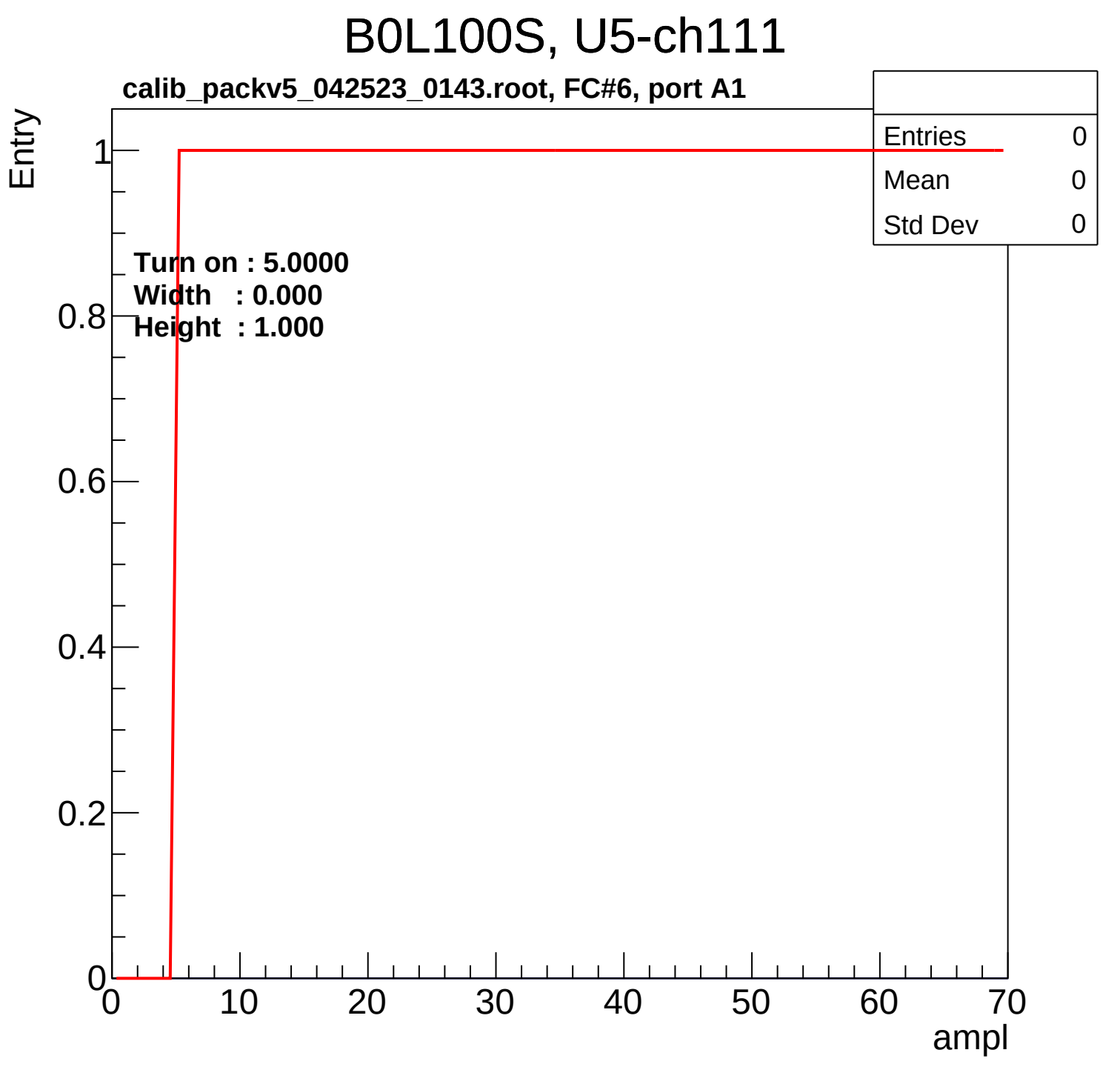

B0L100S, U5-ch106
calib_packv5_042523_0143.root, FC#6, port A1
Entries 17
Mean 50.71
Std Dev 2.08
Turn on : 21.5096
Width : 0.921
Height : 2.222
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

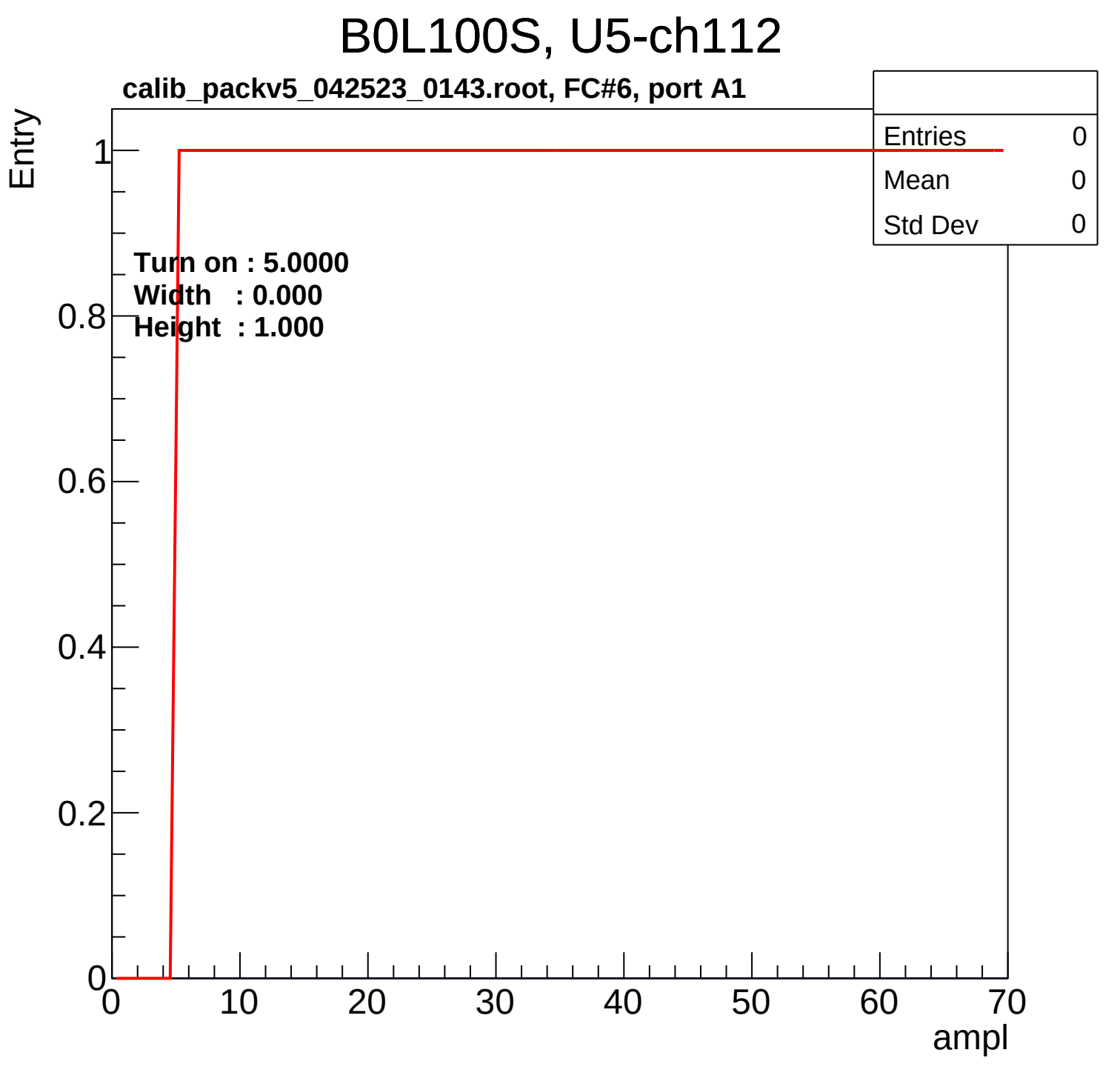

B0L100S, U5-ch107
calib_packv5_042523_0143.root, FC#6, port A1
Entries 7
Mean 52.57
Std Dev 0.4949
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

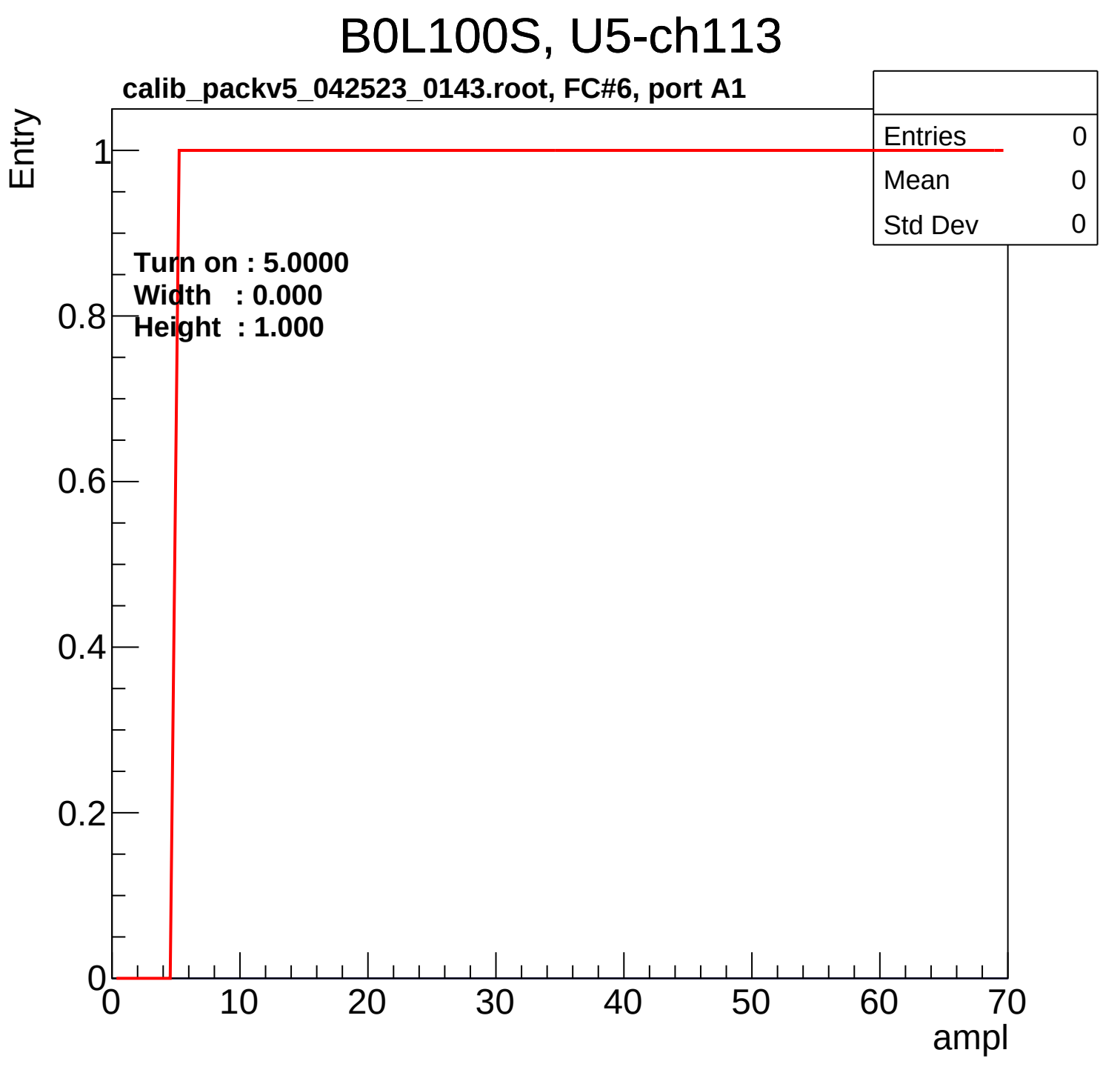

B0L100S, U5-ch108
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

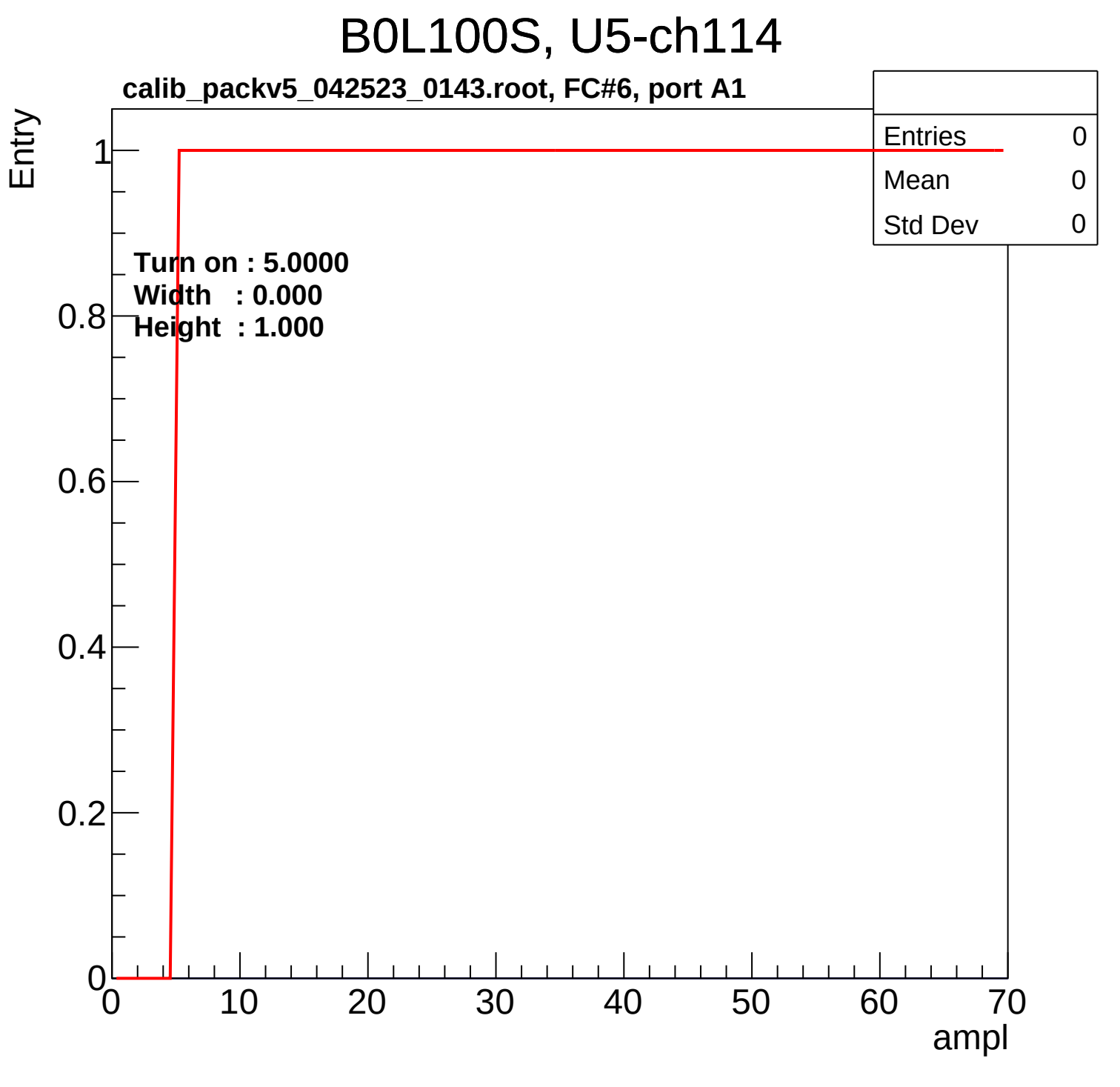

B0L100S, U5-ch109
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

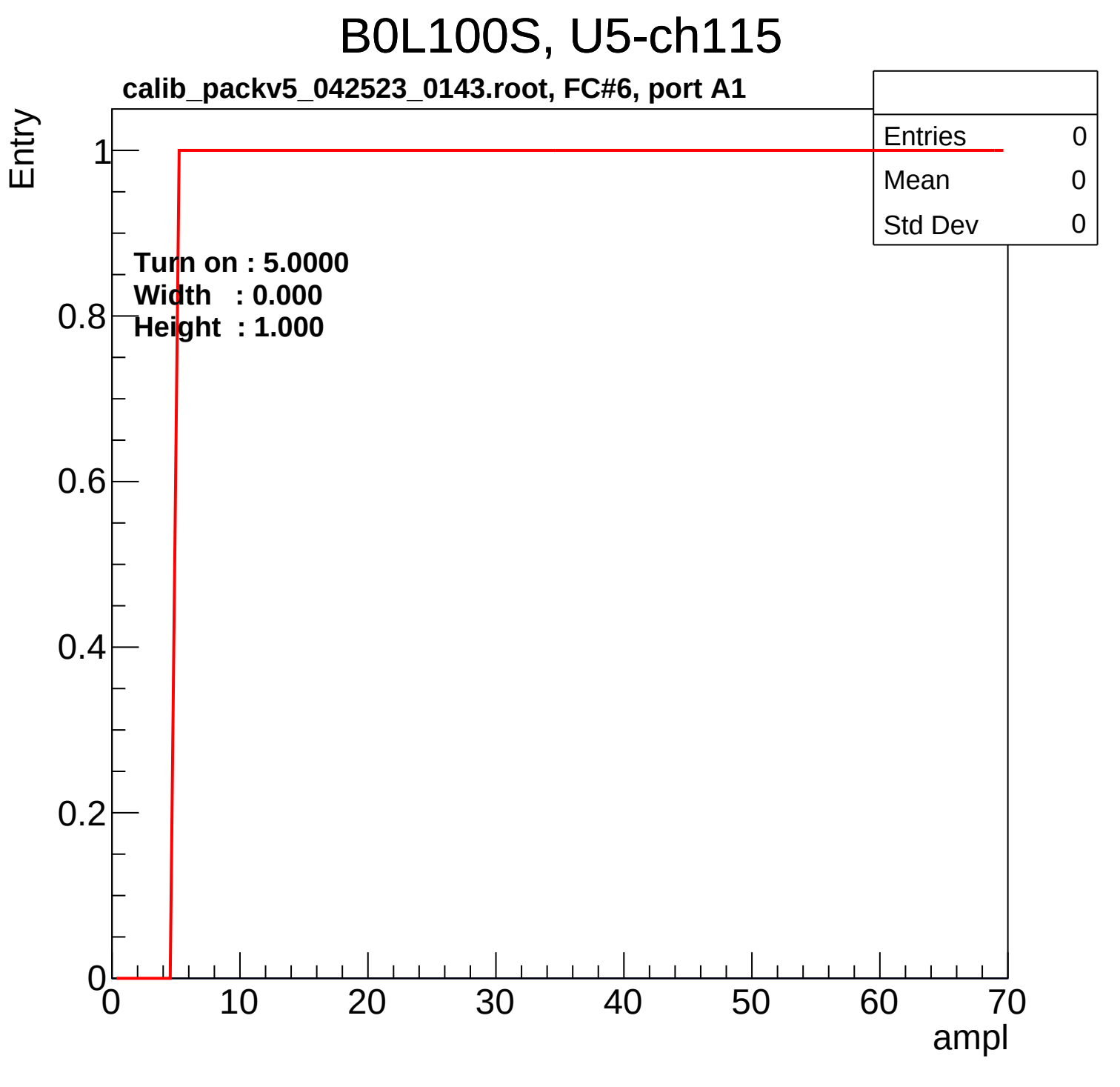

B0L100S, U5-ch110
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

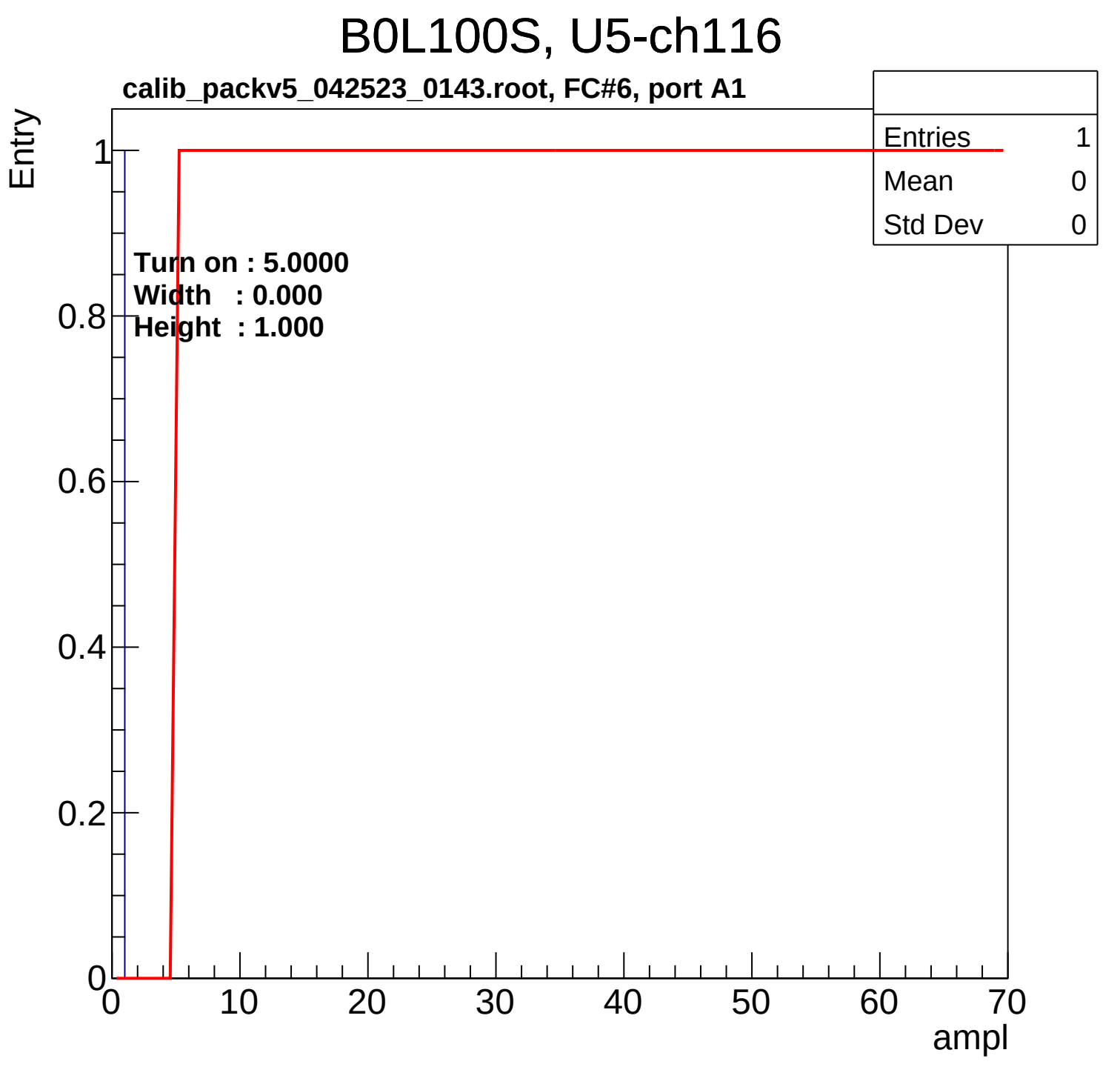

B0L100S, U5-ch111
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

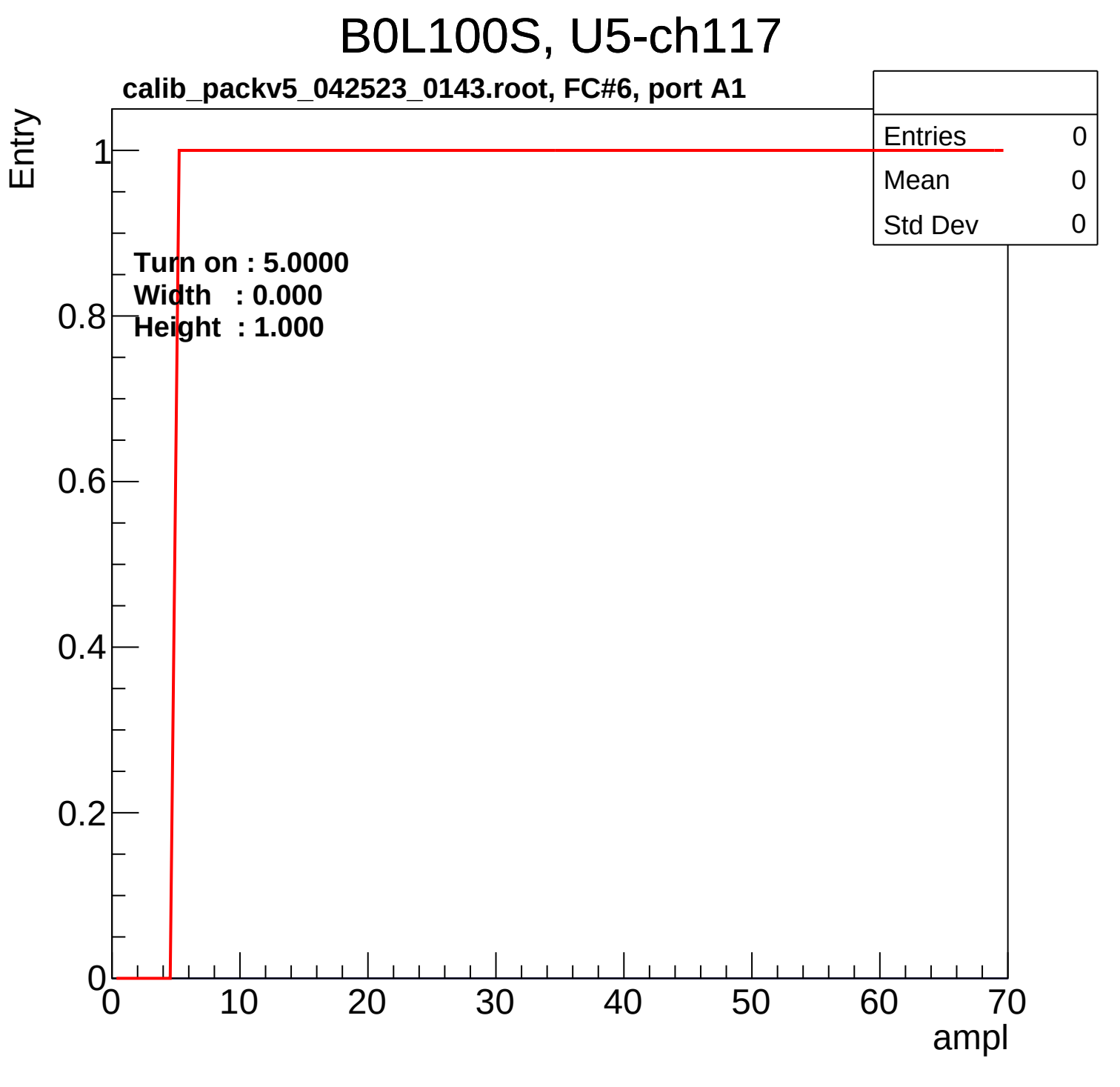

B0L100S, U5-ch112
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

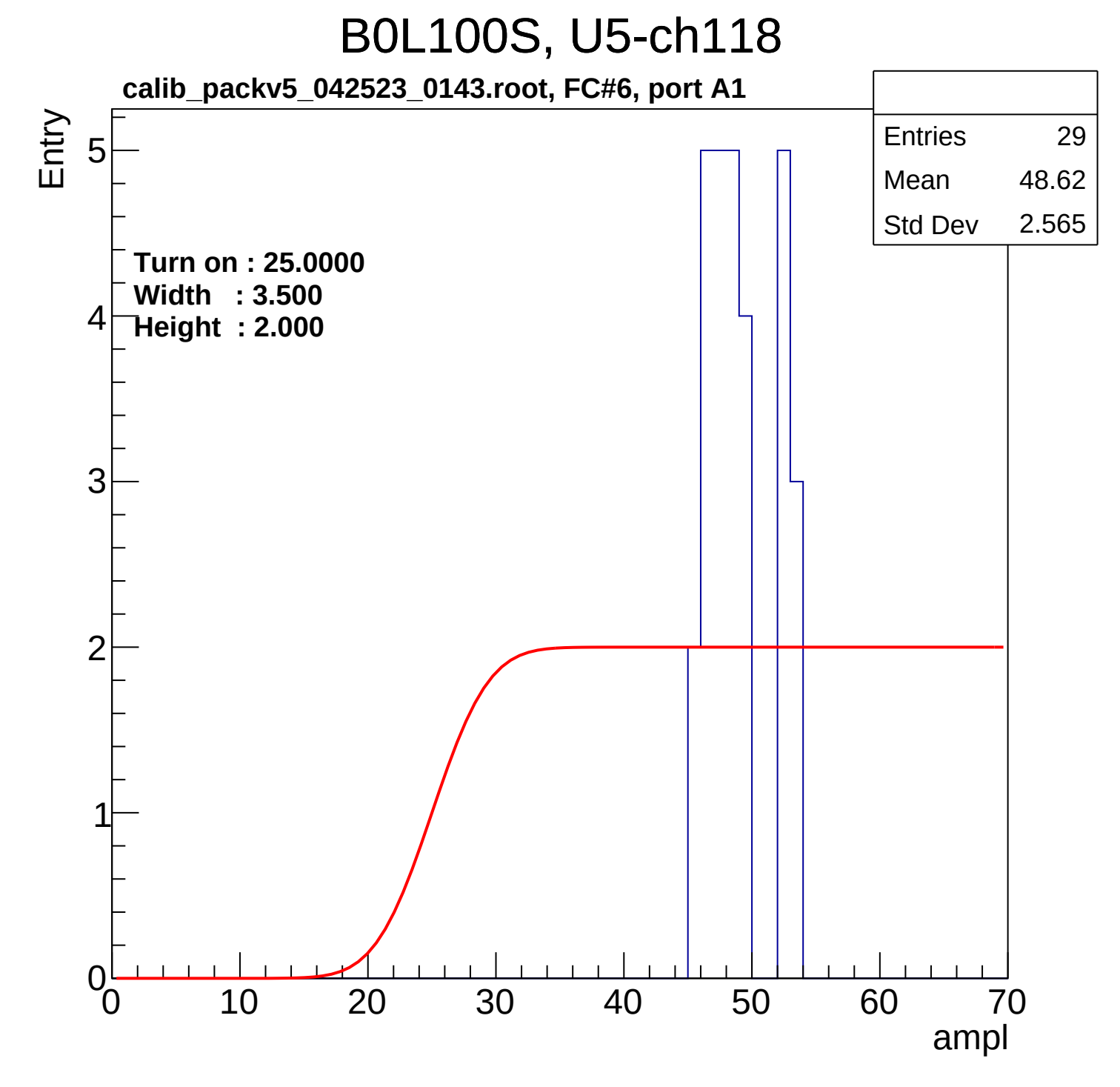

B0L100S, U5-ch113
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

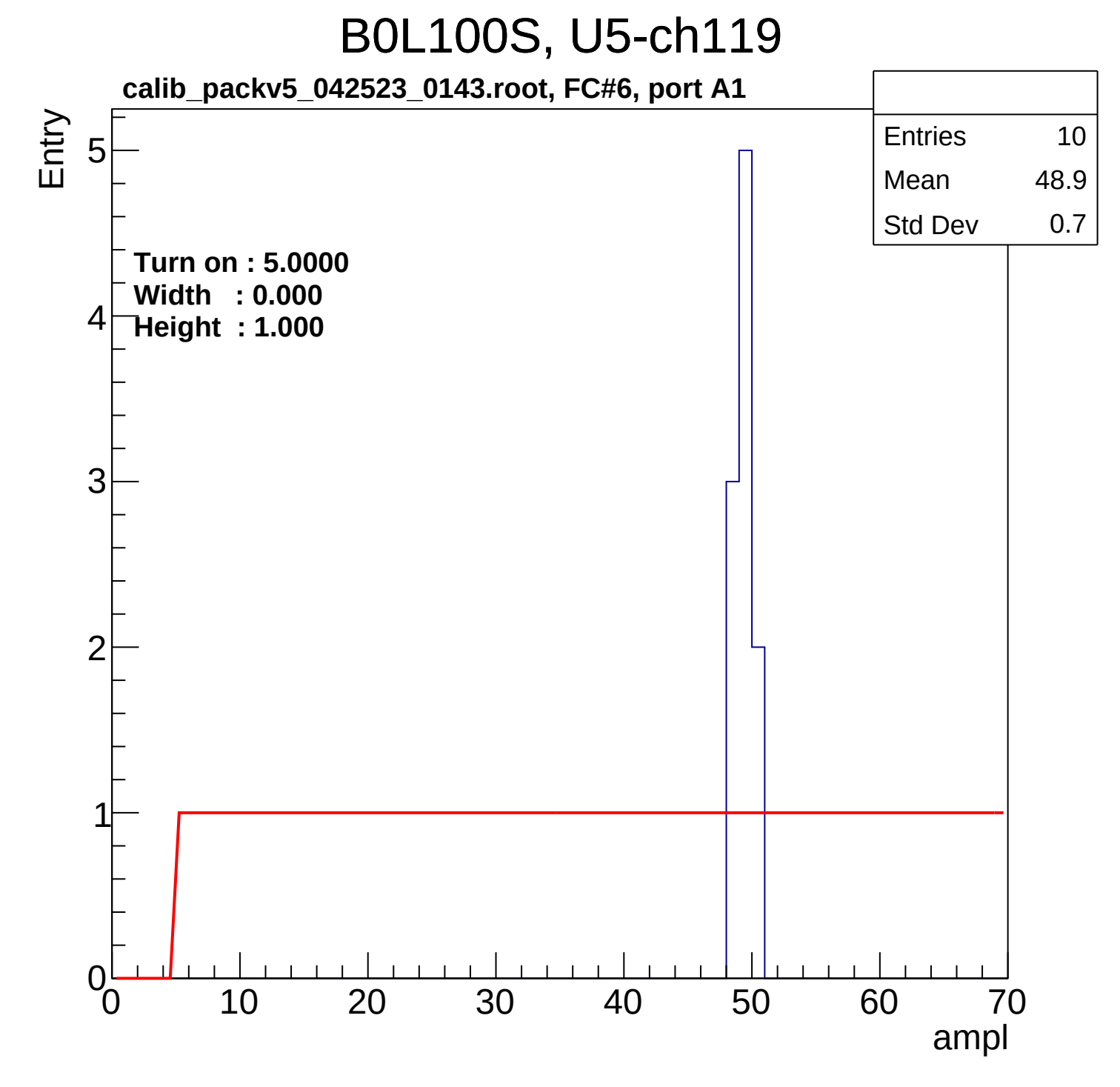

B0L100S, U5-ch114
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

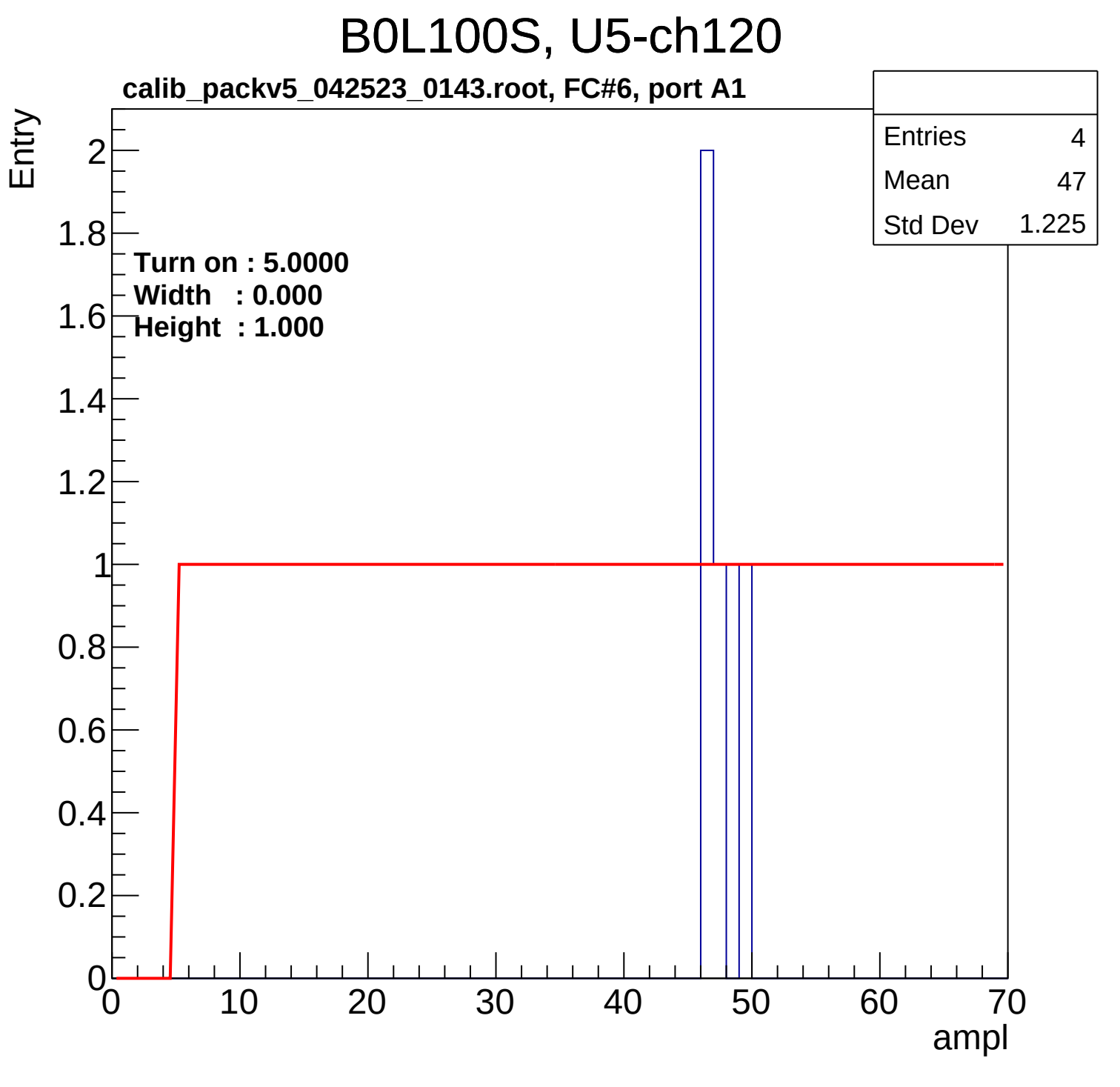

B0L100S, U5-ch115
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

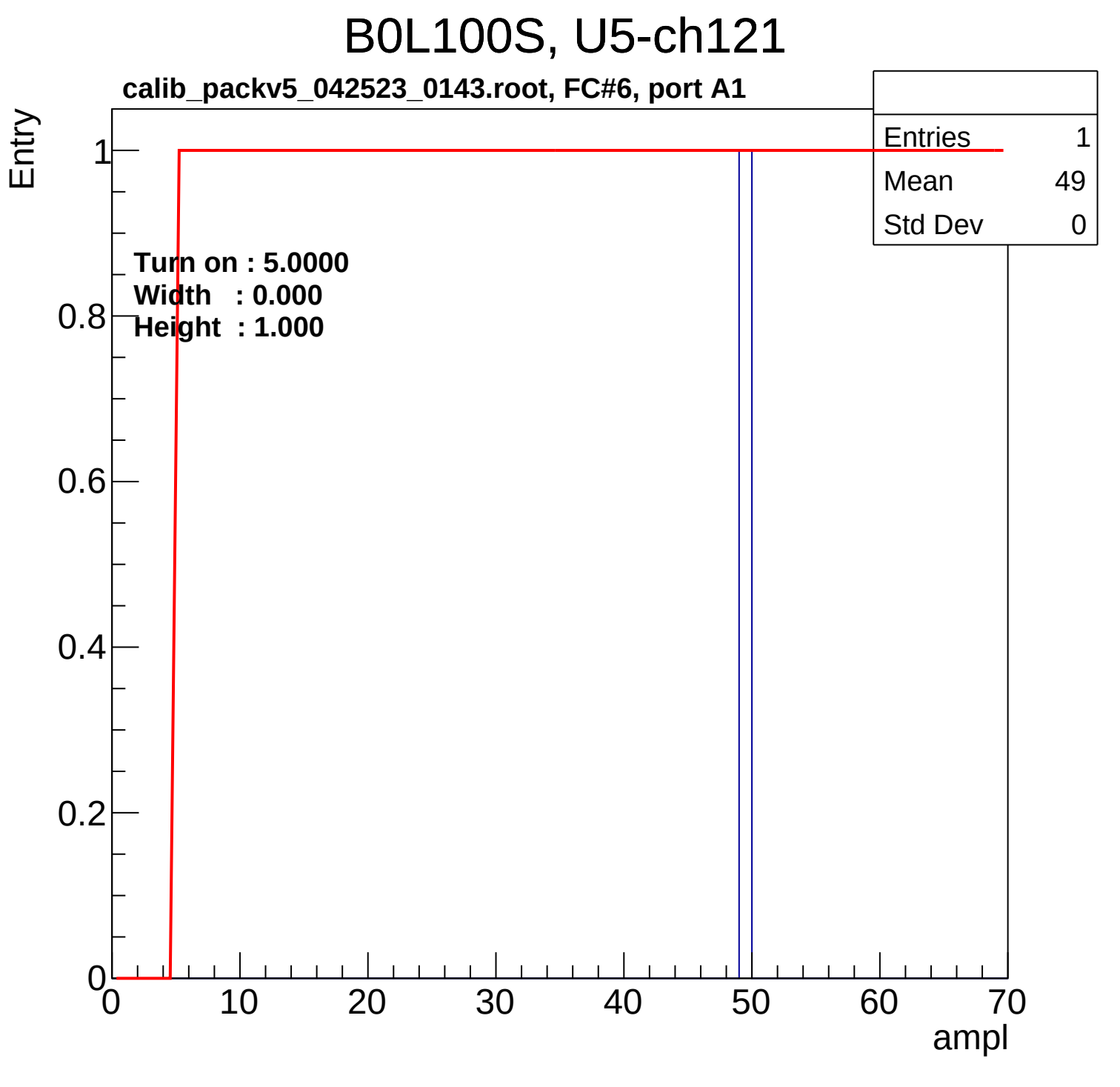

B0L100S, U5-ch116
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

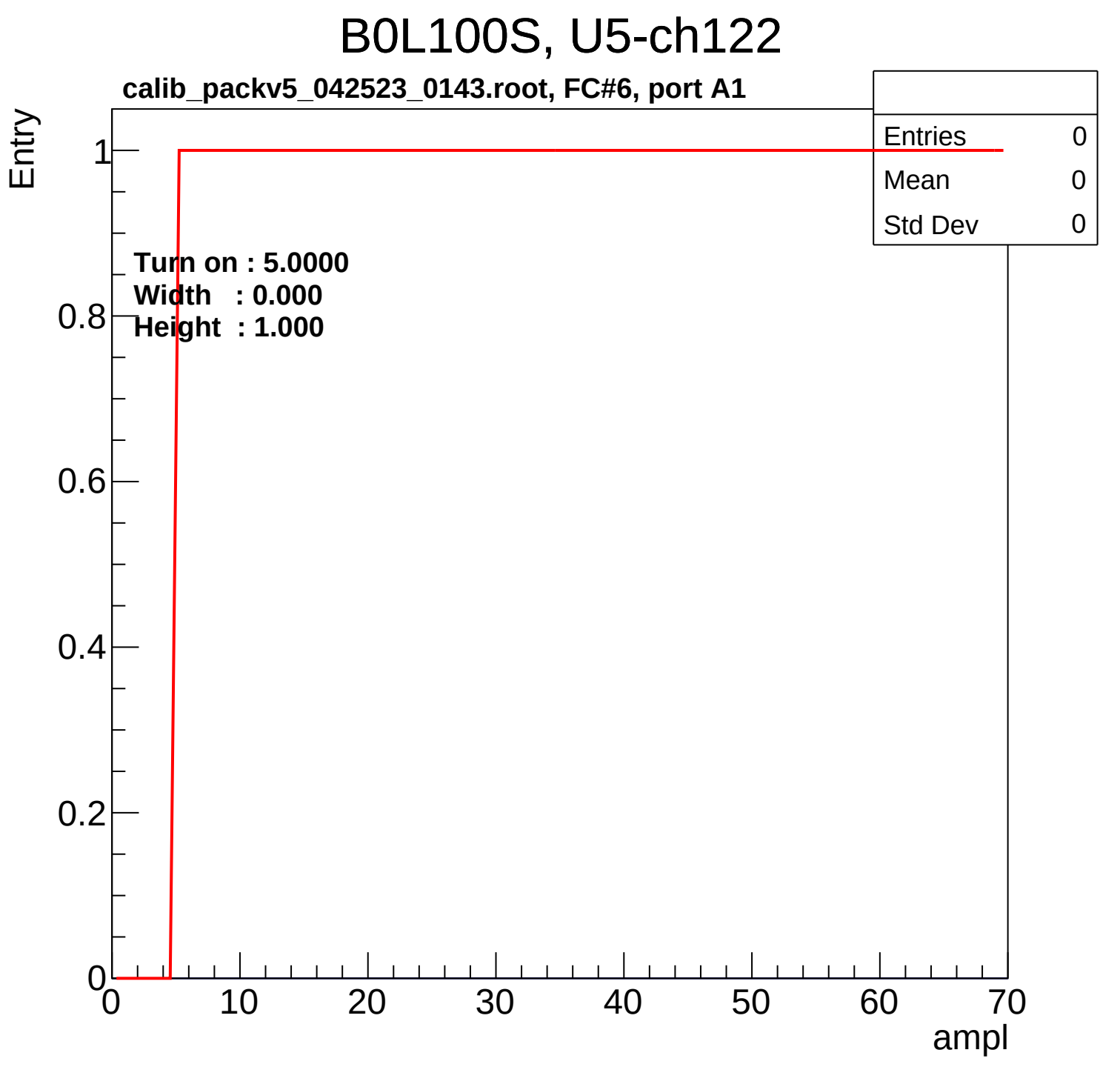

B0L100S, U5-ch117
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

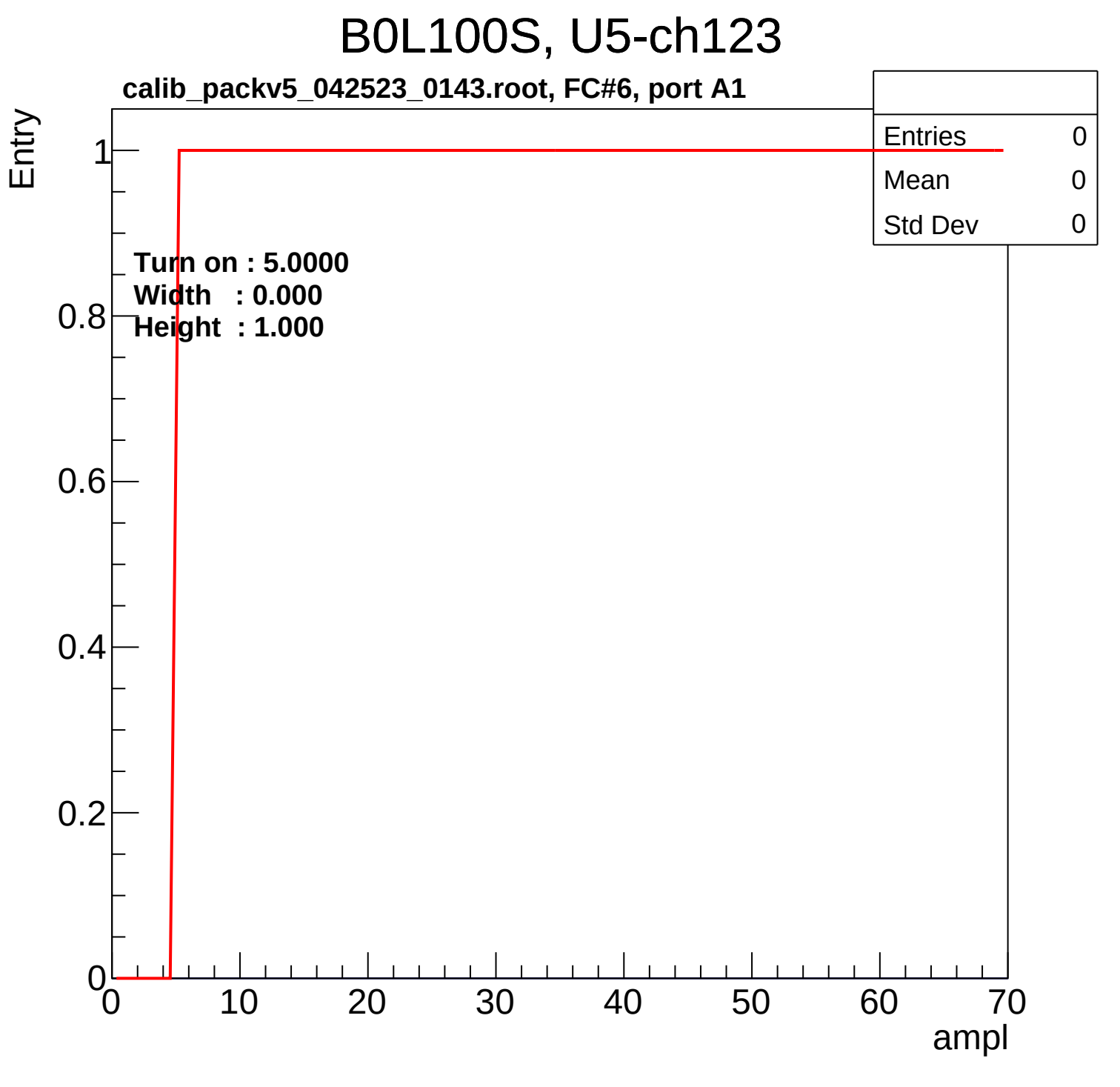

B0L100S, U5-ch118
calib_packv5_042523_0143.root, FC#6, port A1
Entries 29
Mean 48.62
Std Dev 2.565
Turn on : 25.0000
Width : 3.500
Height : 2.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

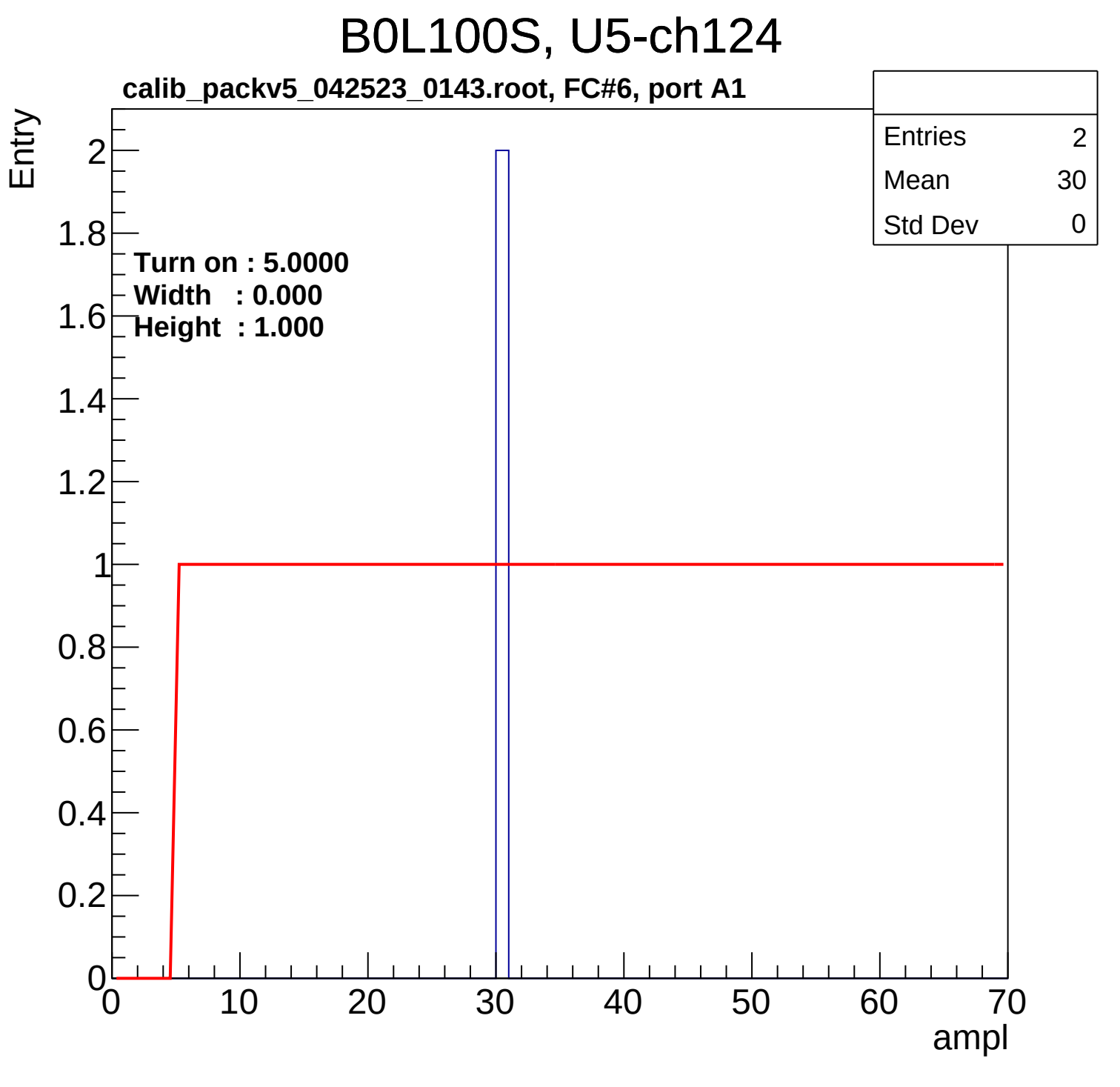

B0L100S, U5-ch119
calib_packv5_042523_0143.root, FC#6, port A1
Entries 10
Mean 48.9
Std Dev 0.7
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

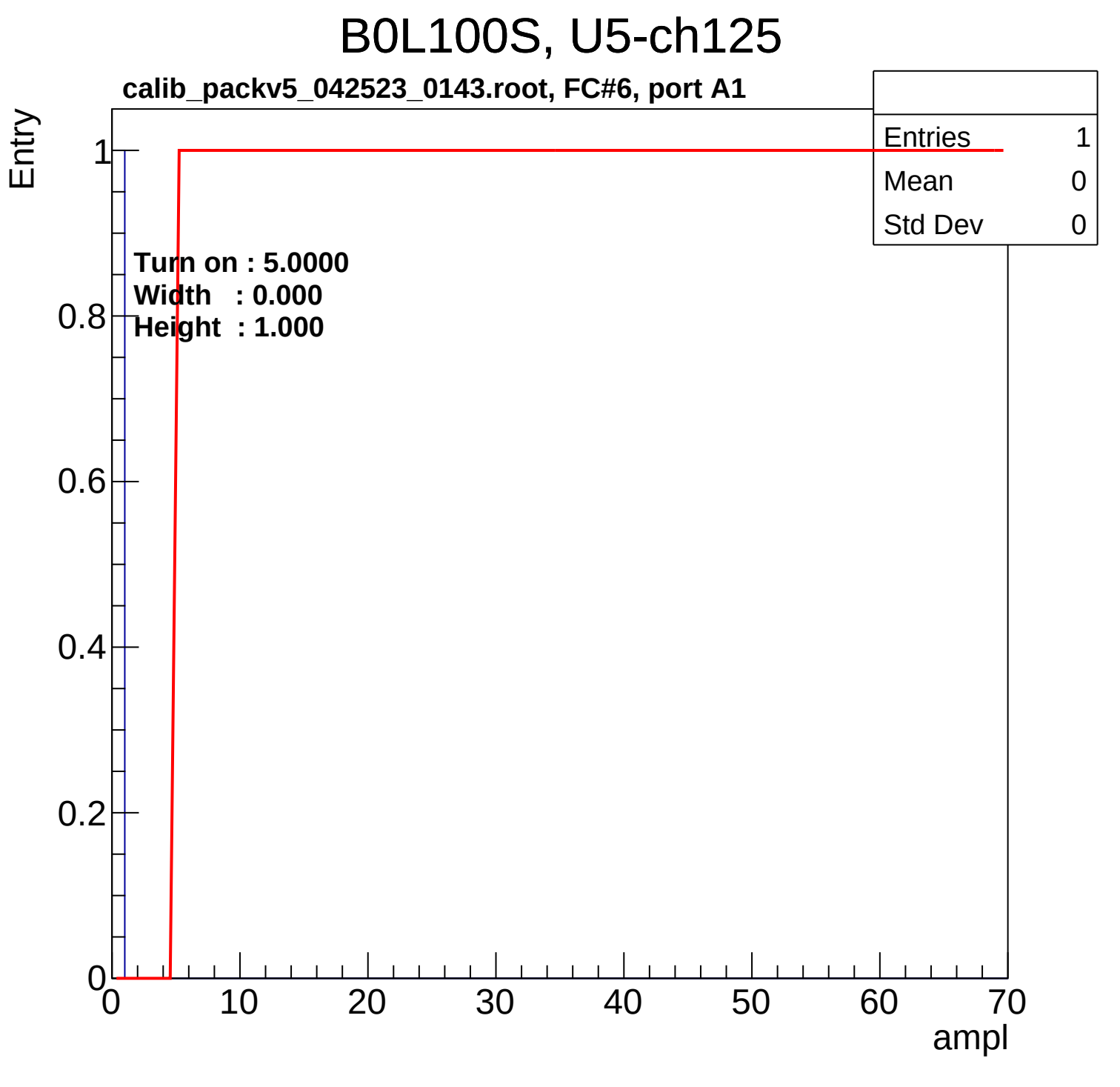

B0L100S, U5-ch120
calib_packv5_042523_0143.root, FC#6, port A1
Entries 4
Mean 47
Std Dev 1.225
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

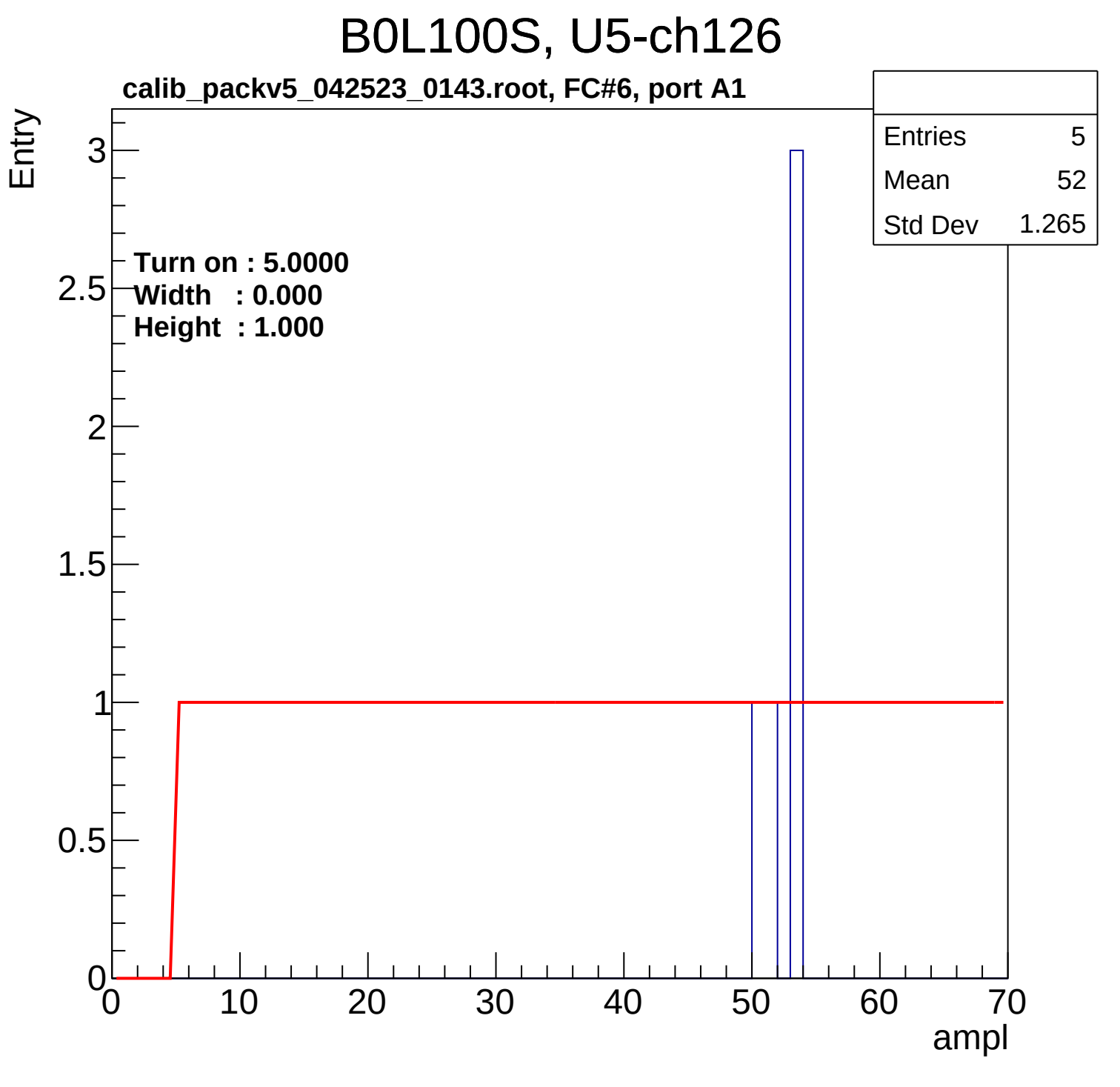

B0L100S, U5-ch121
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 49
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

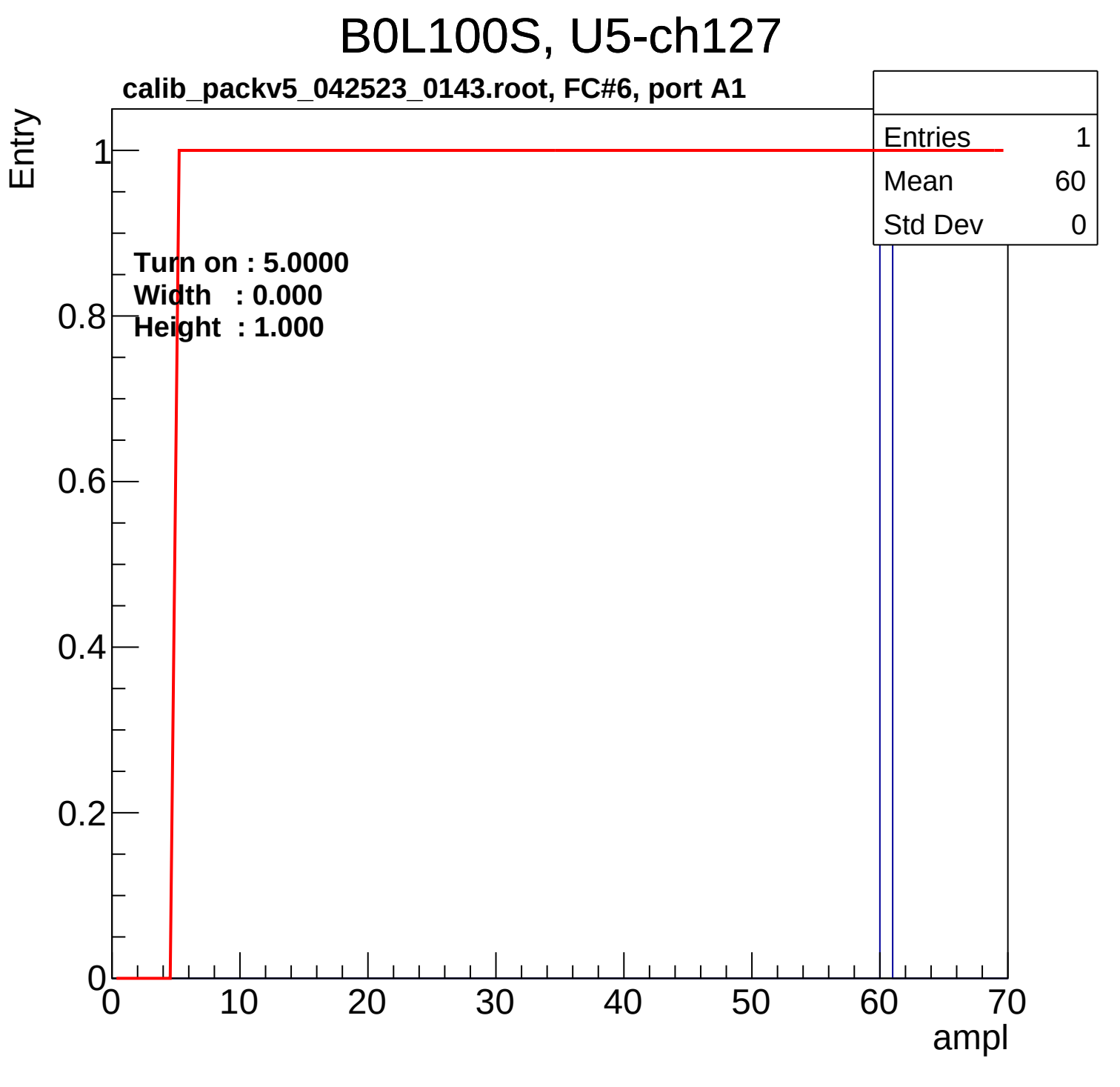

B0L100S, U5-ch122
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

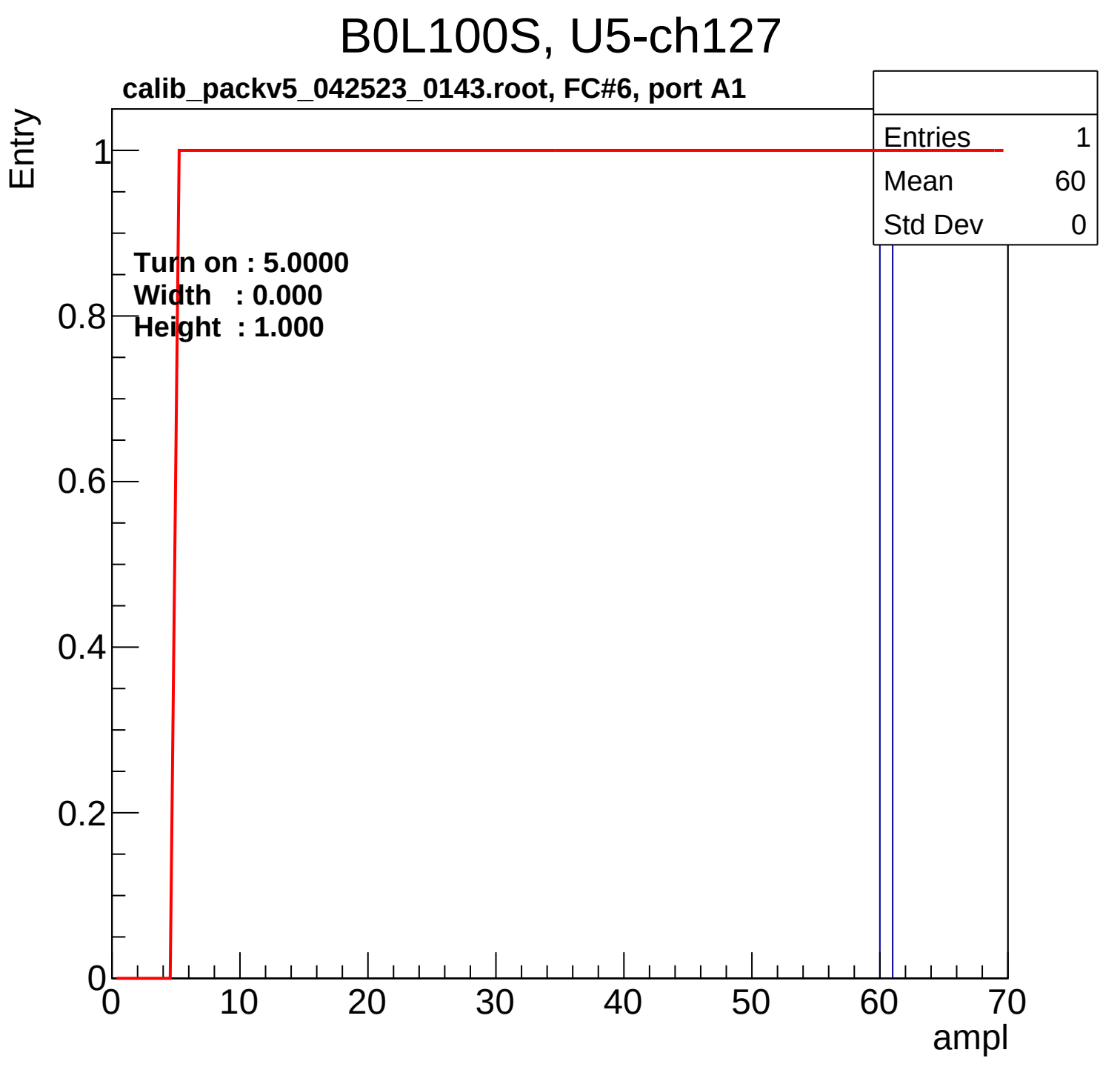

B0L100S, U5-ch123
calib_packv5_042523_0143.root, FC#6, port A1
Entries 0
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U5-ch124
calib_packv5_042523_0143.root, FC#6, port A1
Entries 2
Mean 30
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B0L100S, U5-ch125
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 0
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B0L100S, U5-ch126
calib_packv5_042523_0143.root, FC#6, port A1
Entries 5
Mean 52
Std Dev 1.265
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B0L100S, U5-ch127
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 60
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B0L100S, U5-ch127
calib_packv5_042523_0143.root, FC#6, port A1
Entries 1
Mean 60
Std Dev 0
Turn on : 5.0000
Width : 0.000
Height : 1.000
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70