



# B0L001S, U24-ch0

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	364
Mean	45.14
Std Dev	10.87

Turn on : 27.9391

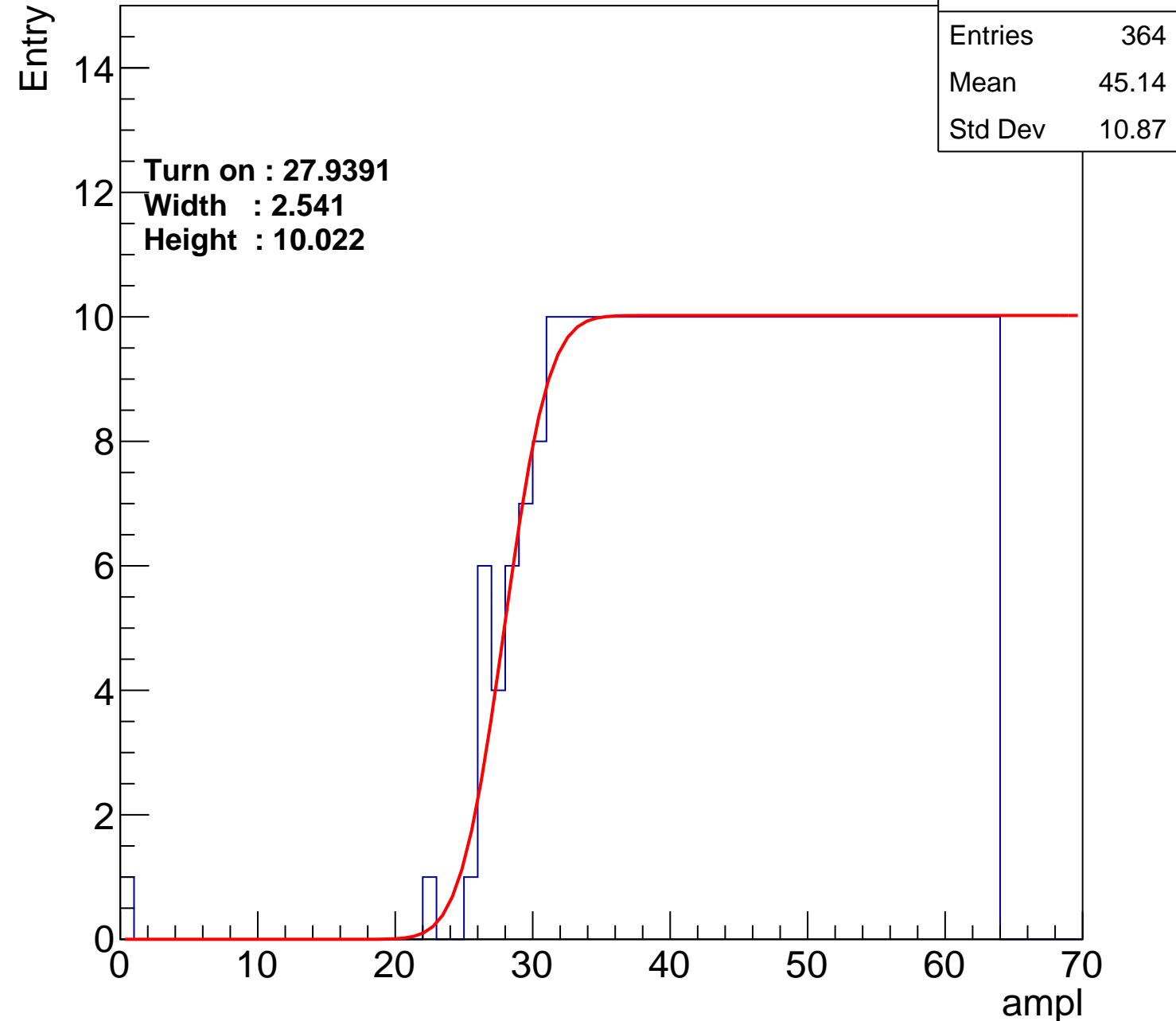
Width : 2.541

Height : 10.022

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch1

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	368
Mean	44.94
Std Dev	10.98

**Turn on : 27.4575**

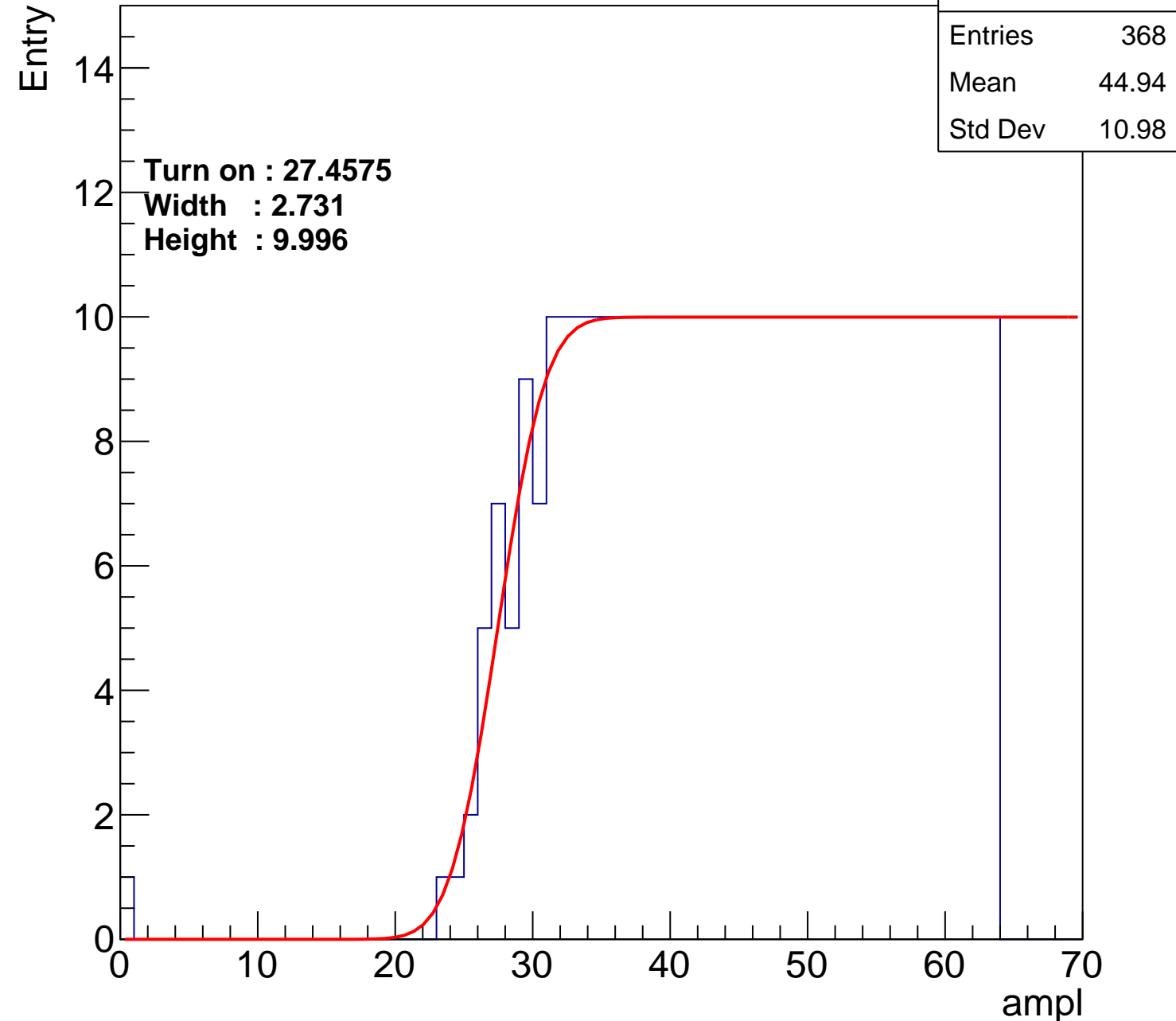
**Width : 2.731**

**Height : 9.996**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch2

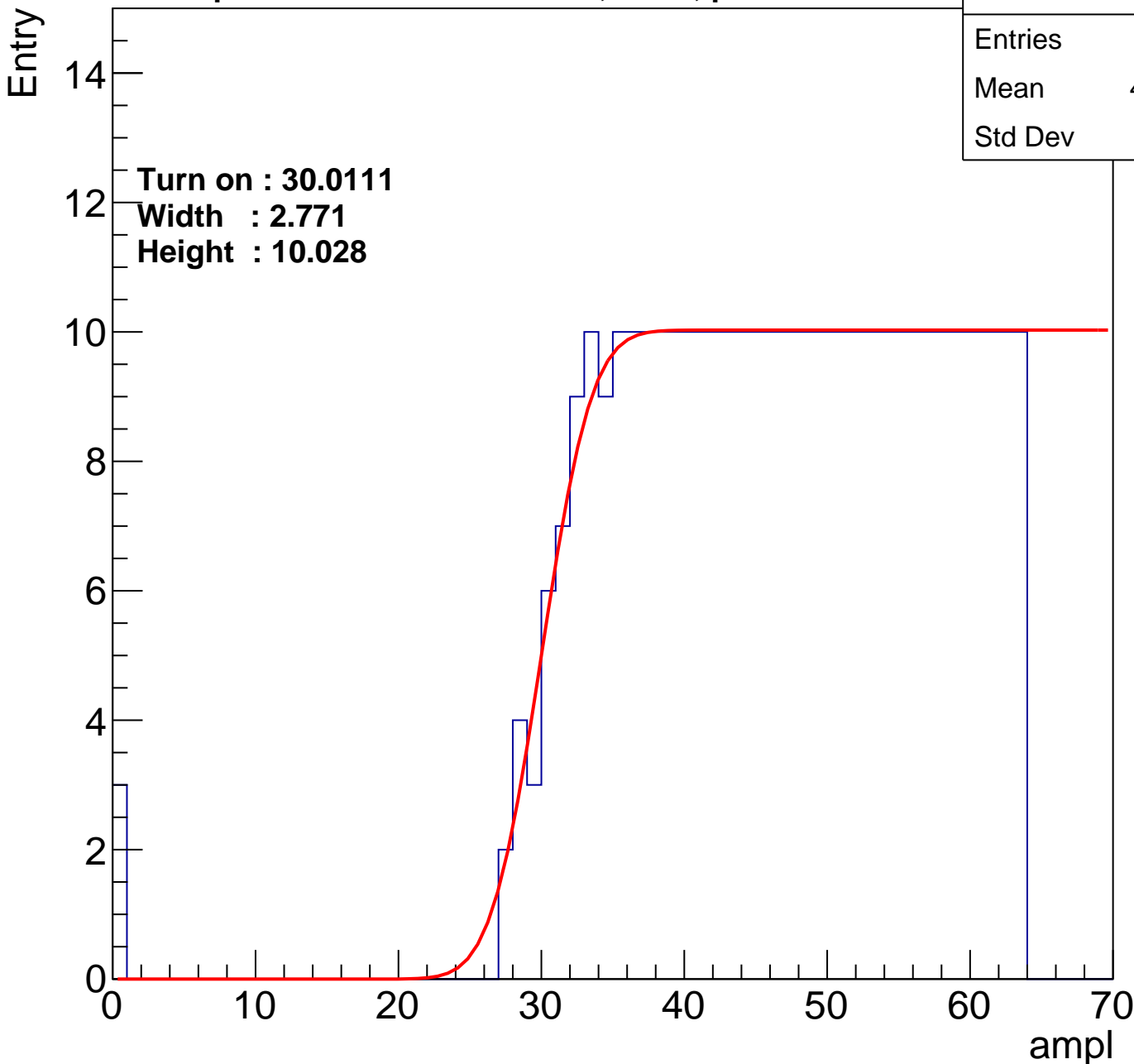
**calib\_packv5\_042523\_0143.root, FC#9, port A1**

**Turn on : 30.0111**

**Width : 2.771**

**Height : 10.028**

Entries	343
Mean	46.02
Std Dev	10.8



# B0L001S, U24-ch3

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	357
Mean	45.22
Std Dev	11.4

Turn on : 29.2184

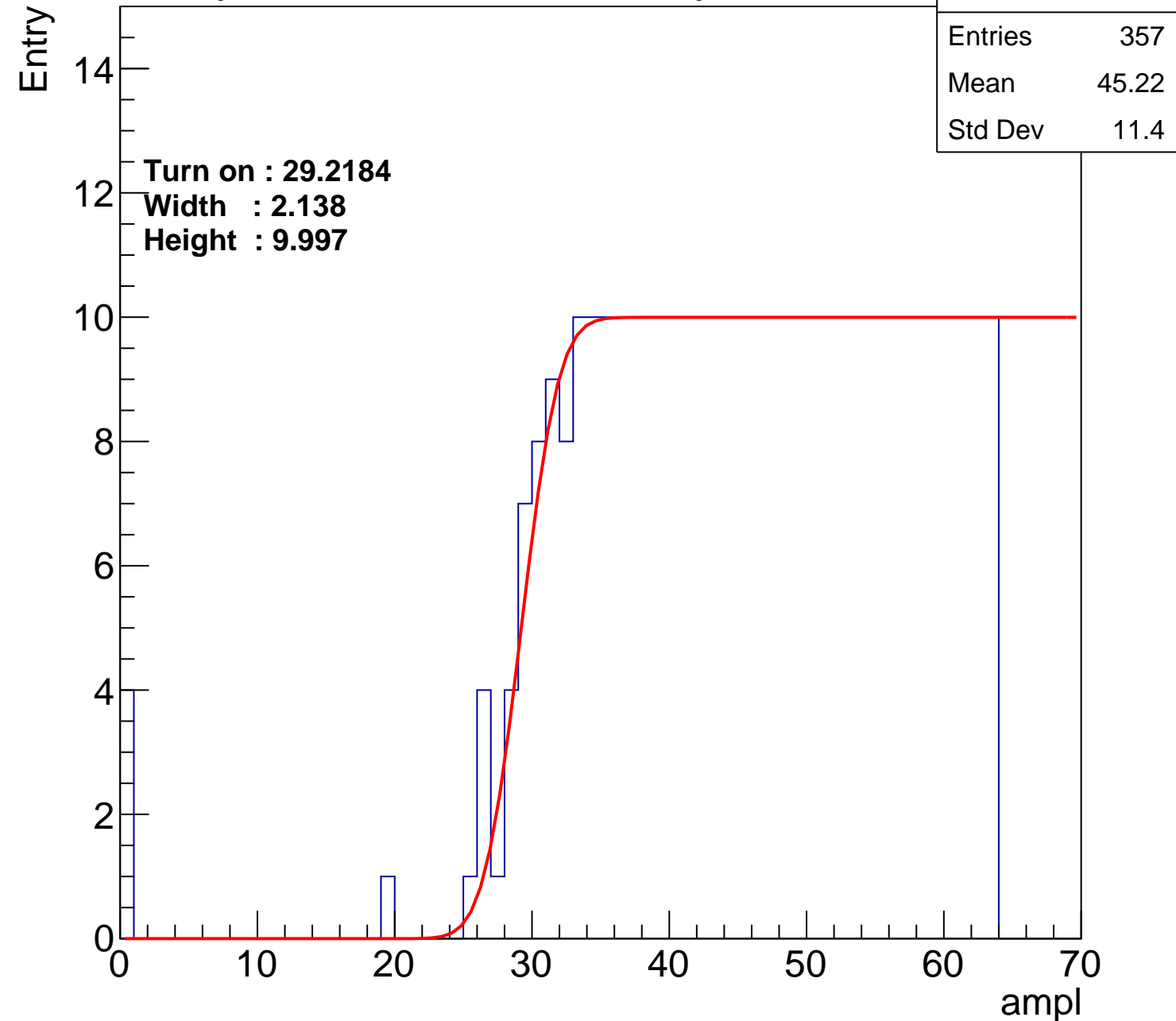
Width : 2.138

Height : 9.997

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch4

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	373
Mean	44.63
Std Dev	11.3

Turn on : 26.8239

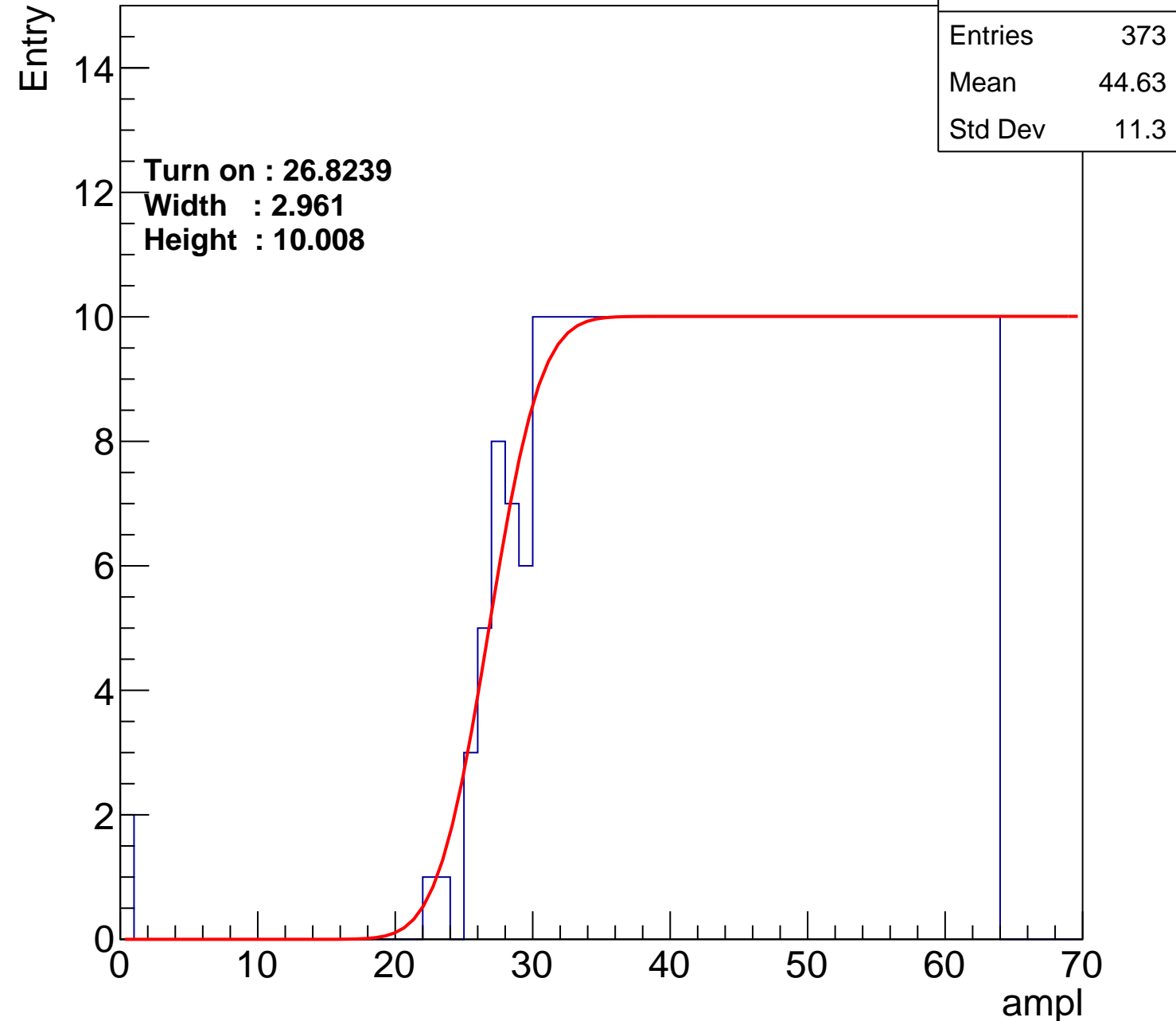
Width : 2.961

Height : 10.008

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch5

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	359
Mean	45.32
Std Dev	10.95

**Turn on : 28.7483**

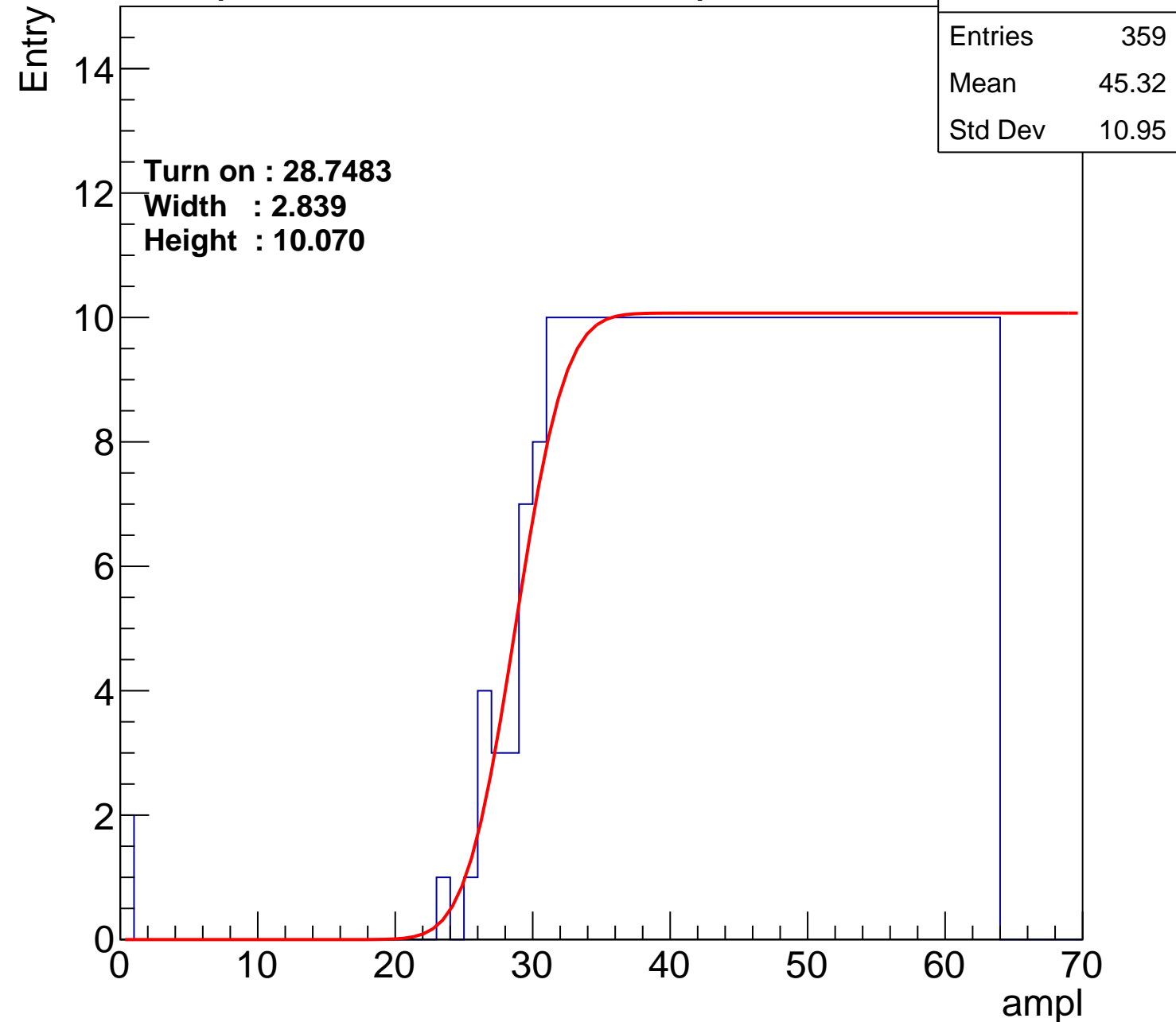
**Width : 2.839**

**Height : 10.070**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch6

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	361
Mean	45.17
Std Dev	11.06

**Turn on : 27.9349**

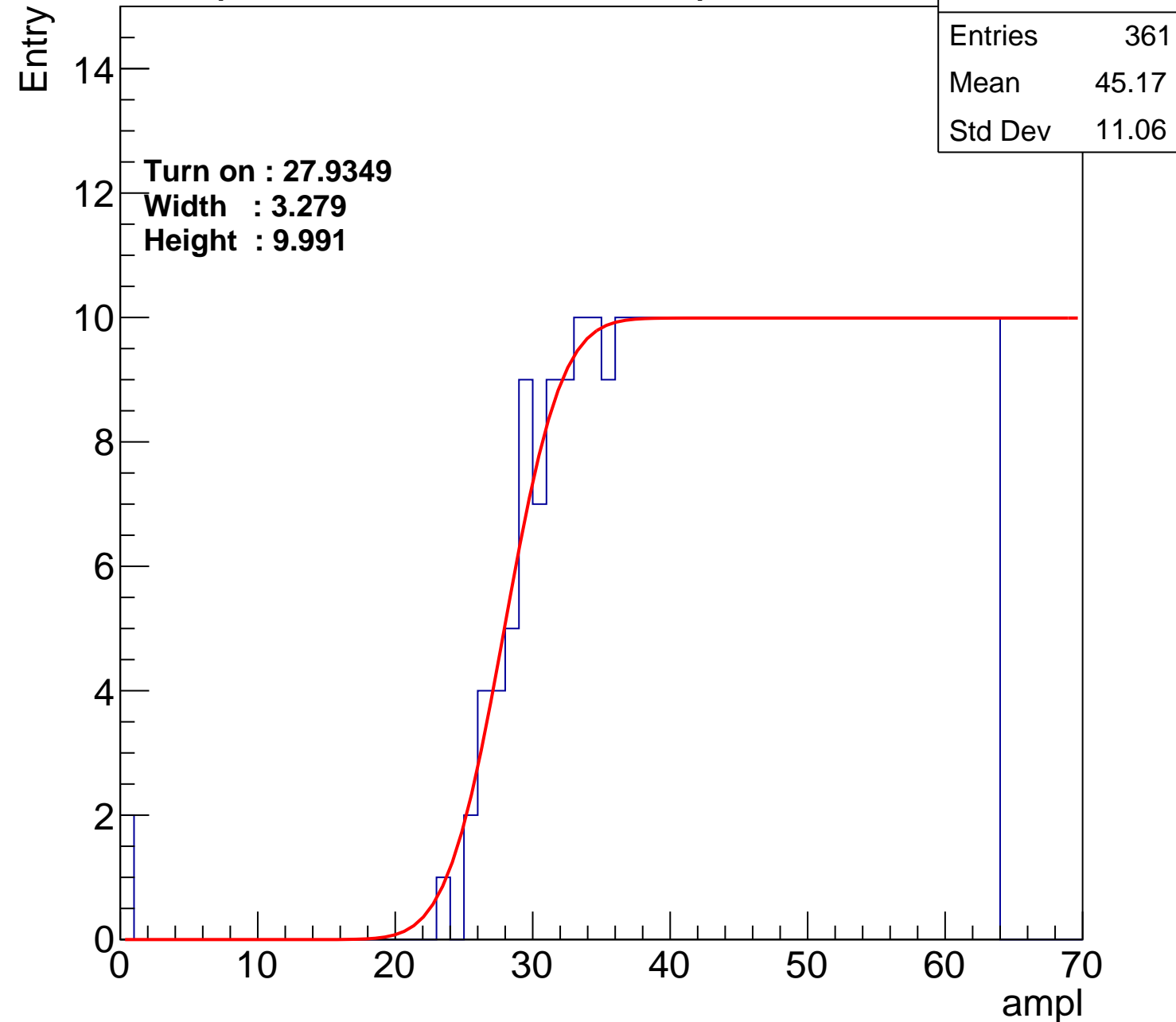
**Width : 3.279**

**Height : 9.991**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U24-ch7

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	350
Mean	45.56
Std Dev	11.24

**Turn on : 29.7363**

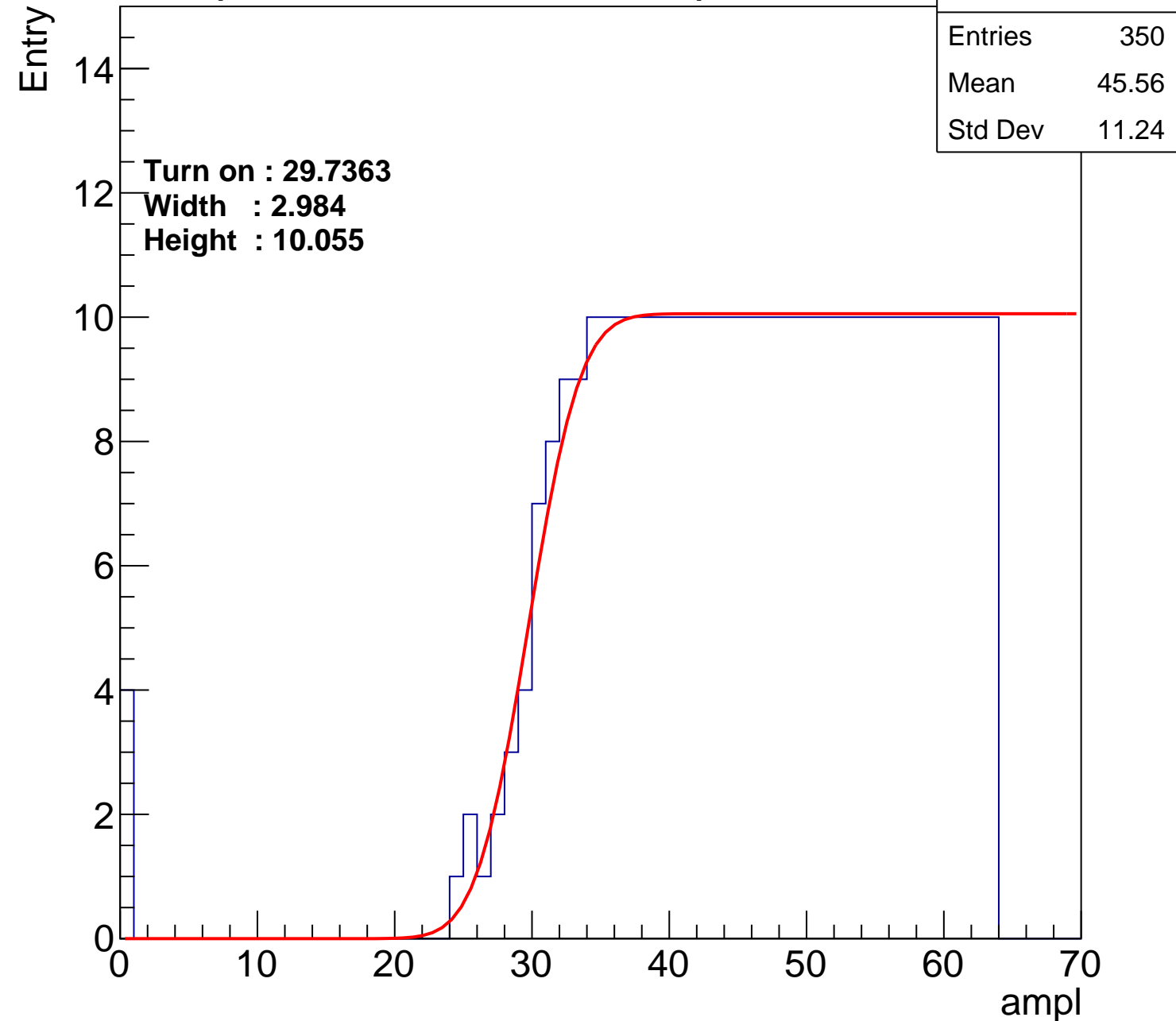
**Width : 2.984**

**Height : 10.055**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch8

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	350
Mean	45.65
Std Dev	11

Turn on : 29.5711

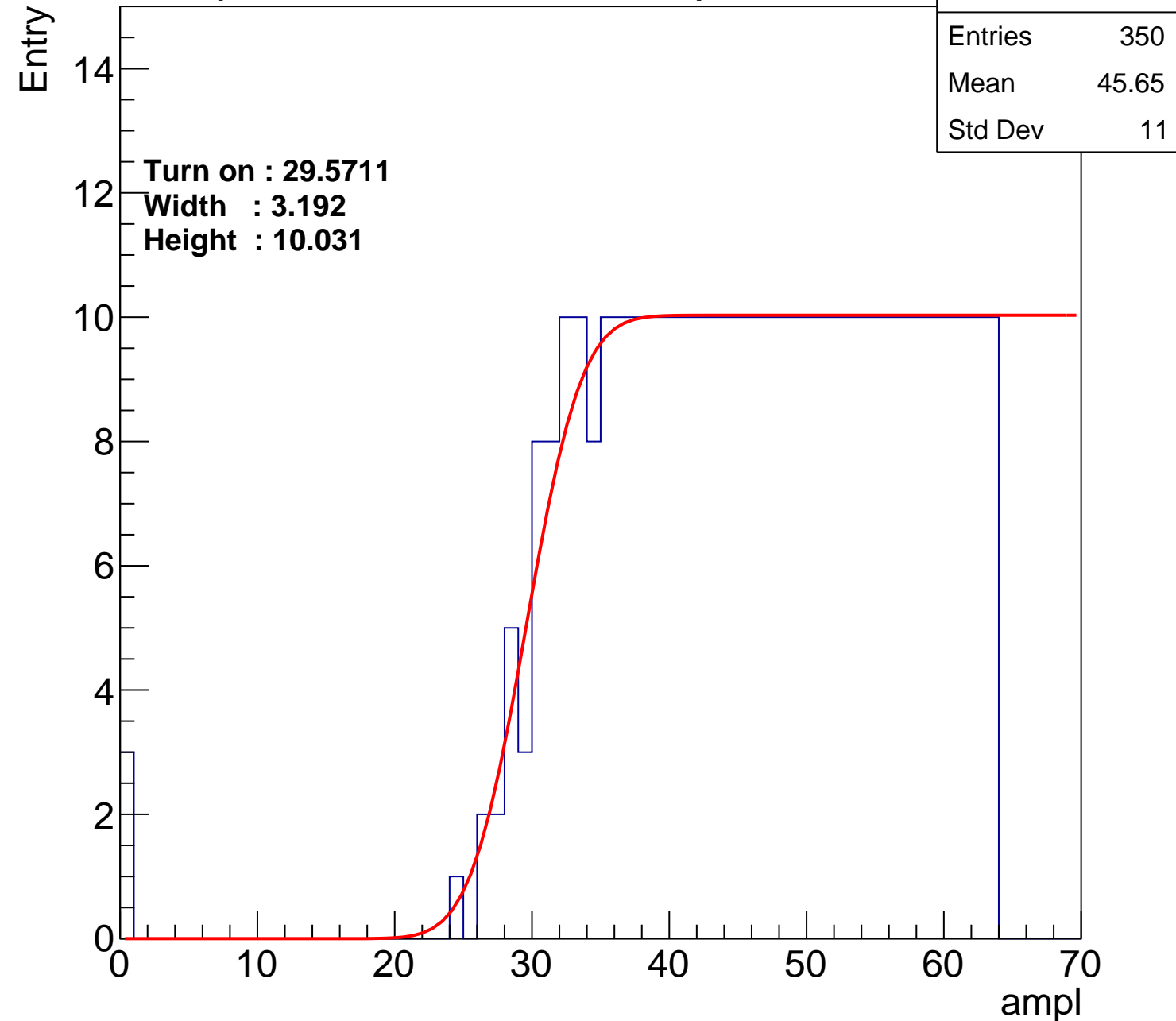
Width : 3.192

Height : 10.031

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch9

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	364
Mean	45.12
Std Dev	10.91

**Turn on : 27.9927**

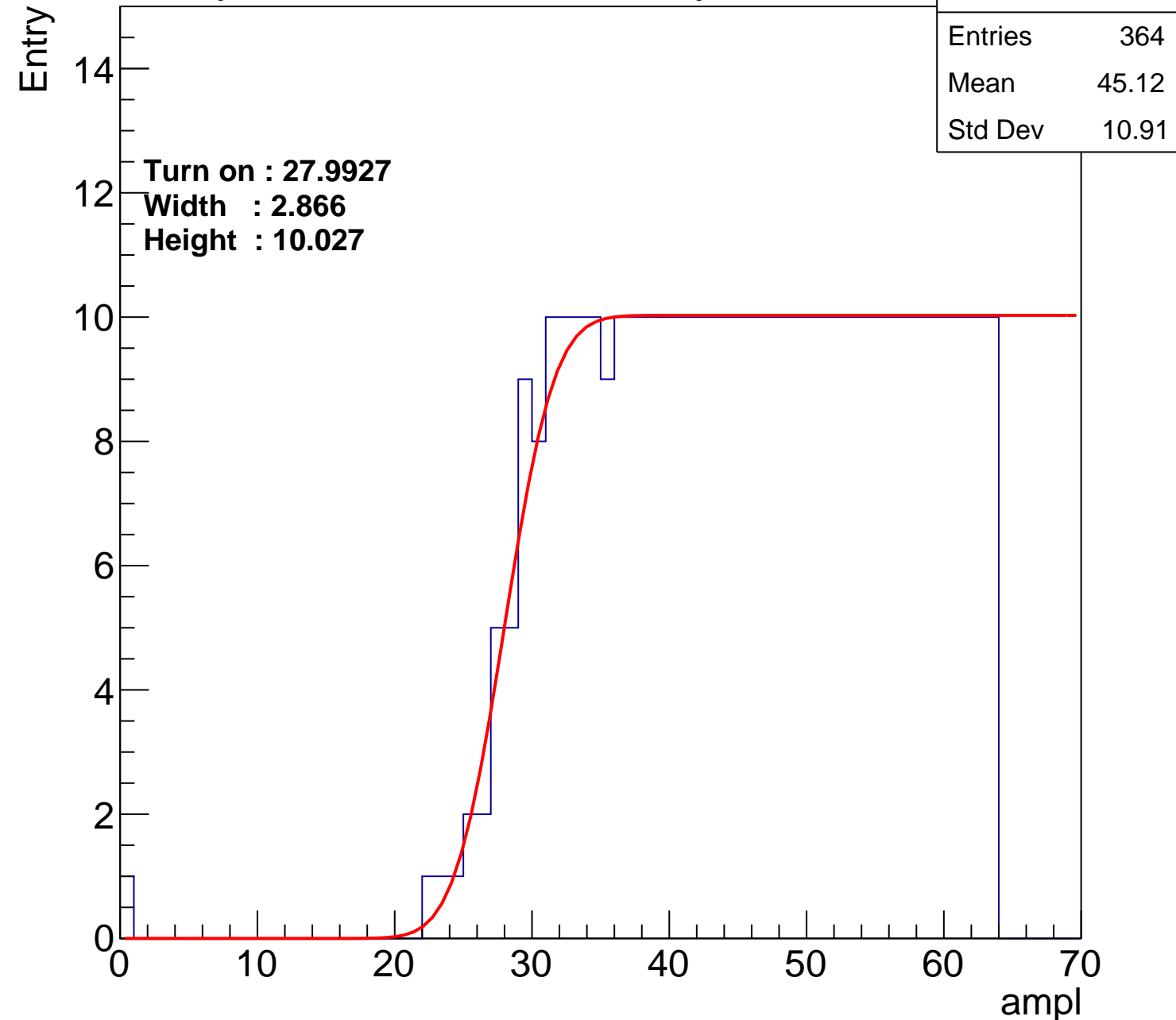
**Width : 2.866**

**Height : 10.027**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch10

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	356
Mean	45.47
Std Dev	10.87

Turn on : 28.9714

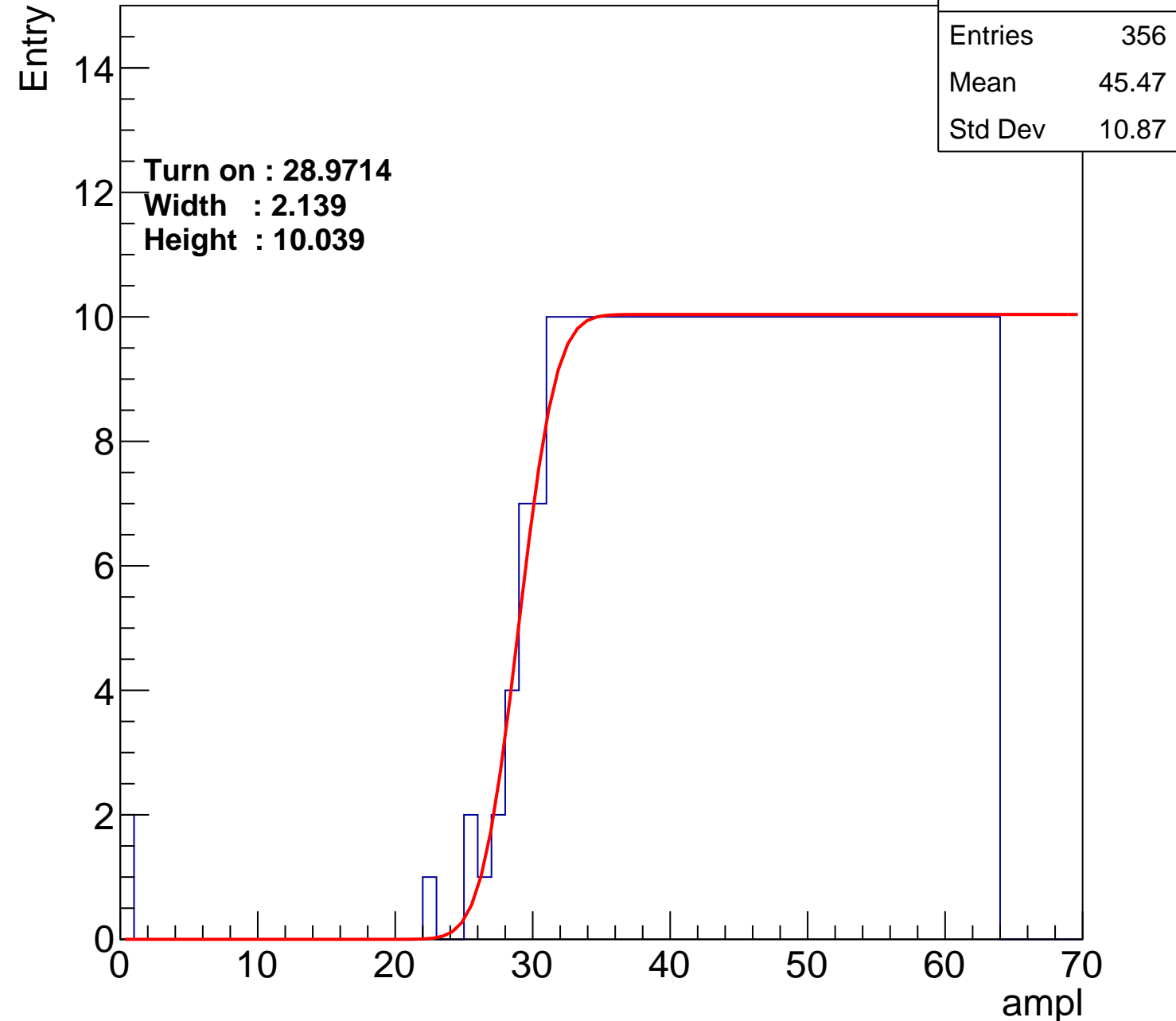
Width : 2.139

Height : 10.039

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch11

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	349
Mean	45.75
Std Dev	10.8

Turn on : 29.2386

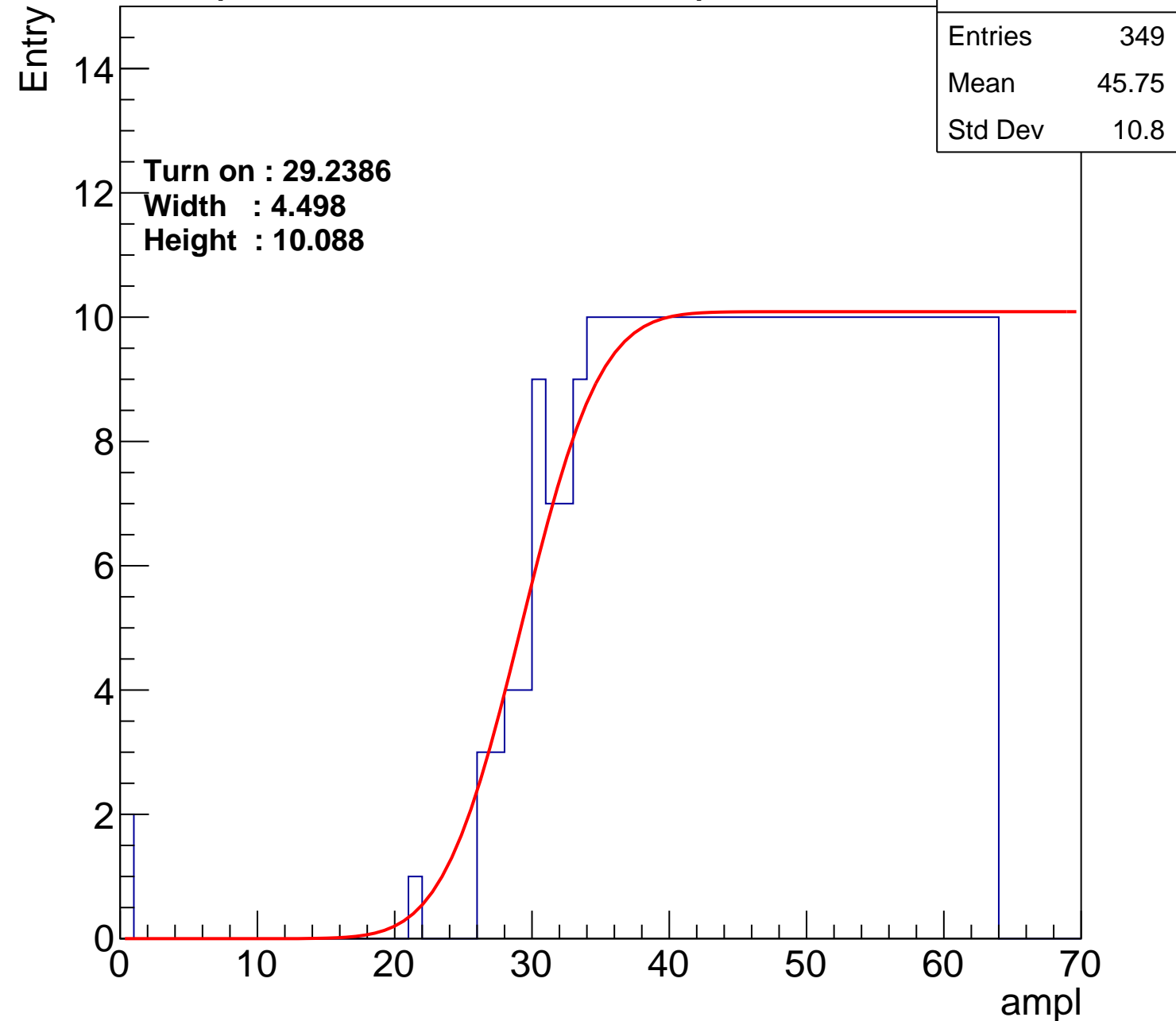
Width : 4.498

Height : 10.088

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch12

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	355
Mean	45.43
Std Dev	11.08

Turn on : 28.5855

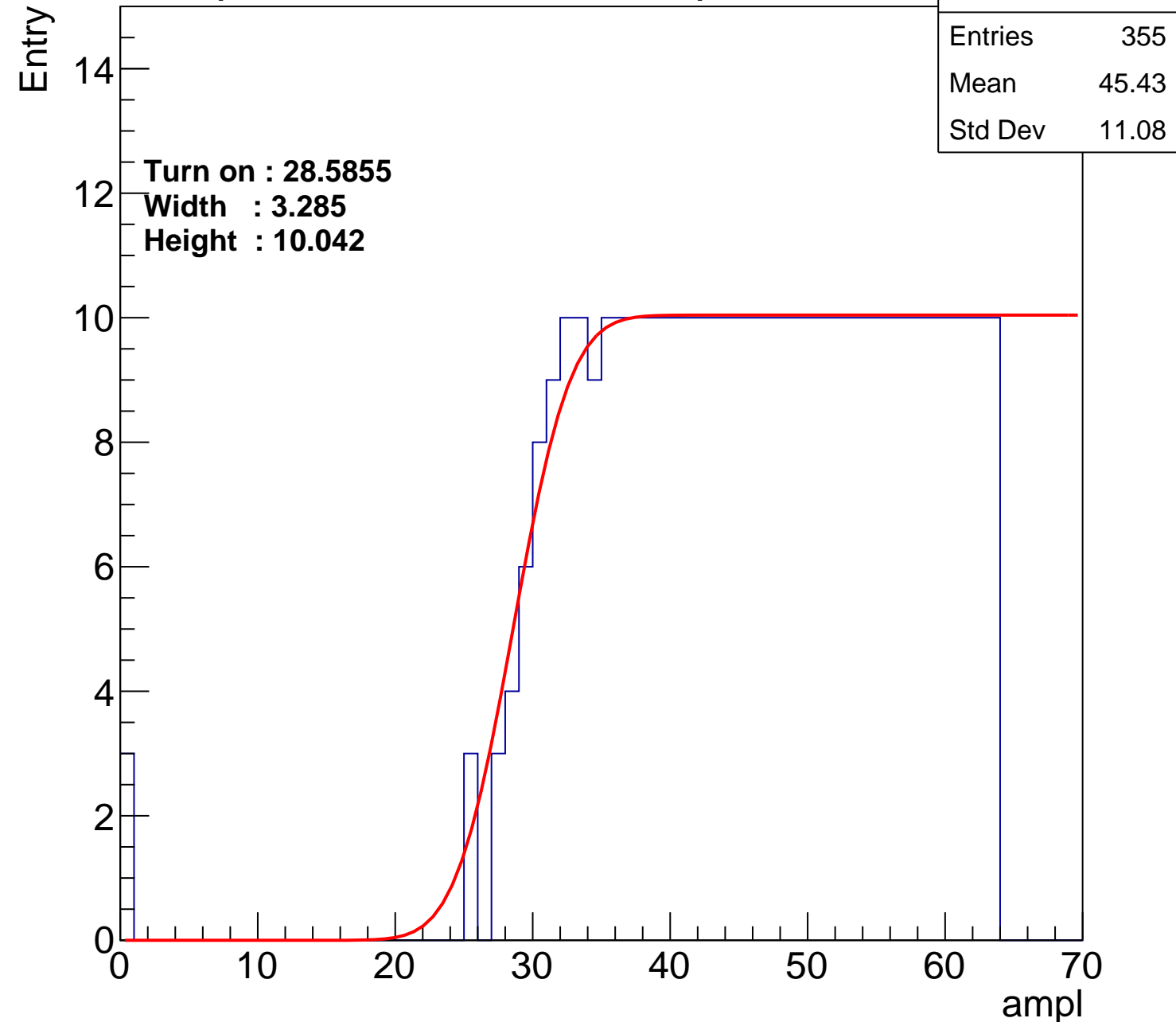
Width : 3.285

Height : 10.042

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



**calib\_packv5\_042523\_0143.root, FC#9, port A1**

Entries	353
Mean	45.54
Std Dev	11.01

Std Dev	11.01
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**Height : 9.943**



# B0L001S, U24-ch14

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	376
Mean	44.55
Std Dev	11.2

Turn on : 26.9488

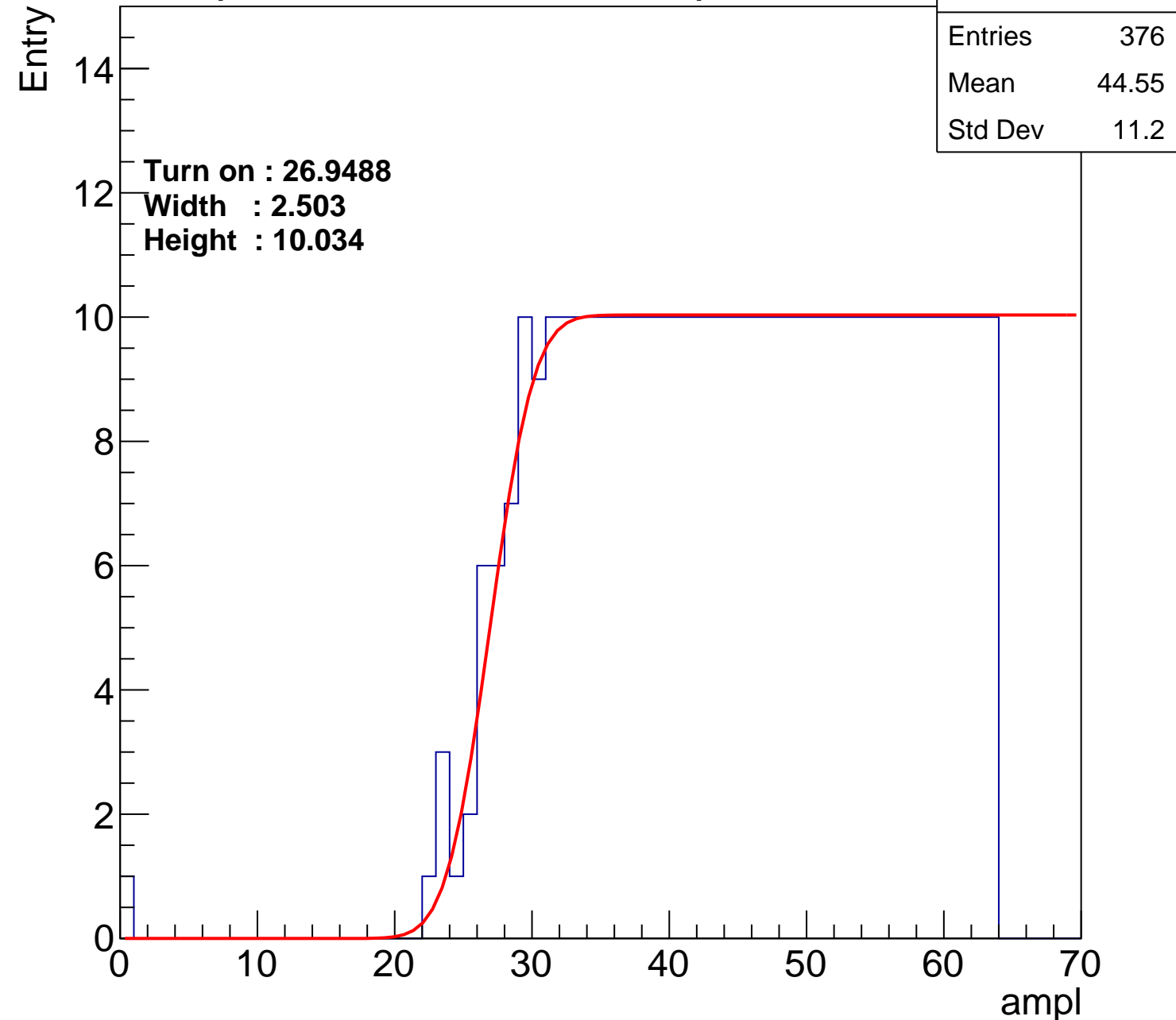
Width : 2.503

Height : 10.034

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U24-ch15

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	373
Mean	44.51
Std Dev	11.57

Turn on : 27.3924

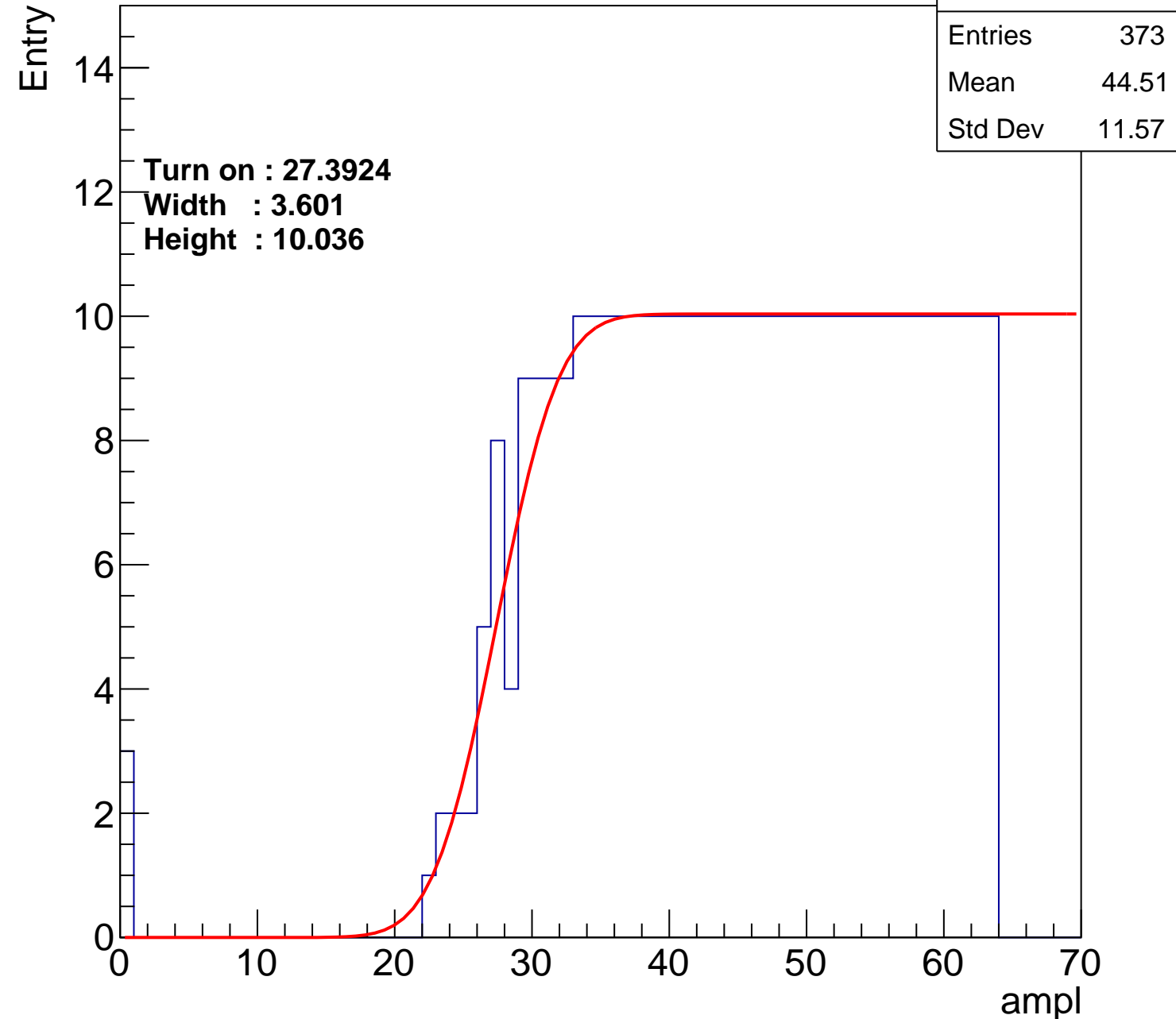
Width : 3.601

Height : 10.036

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch16

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	363
Mean	45.13
Std Dev	11.04

**Turn on : 28.3943**

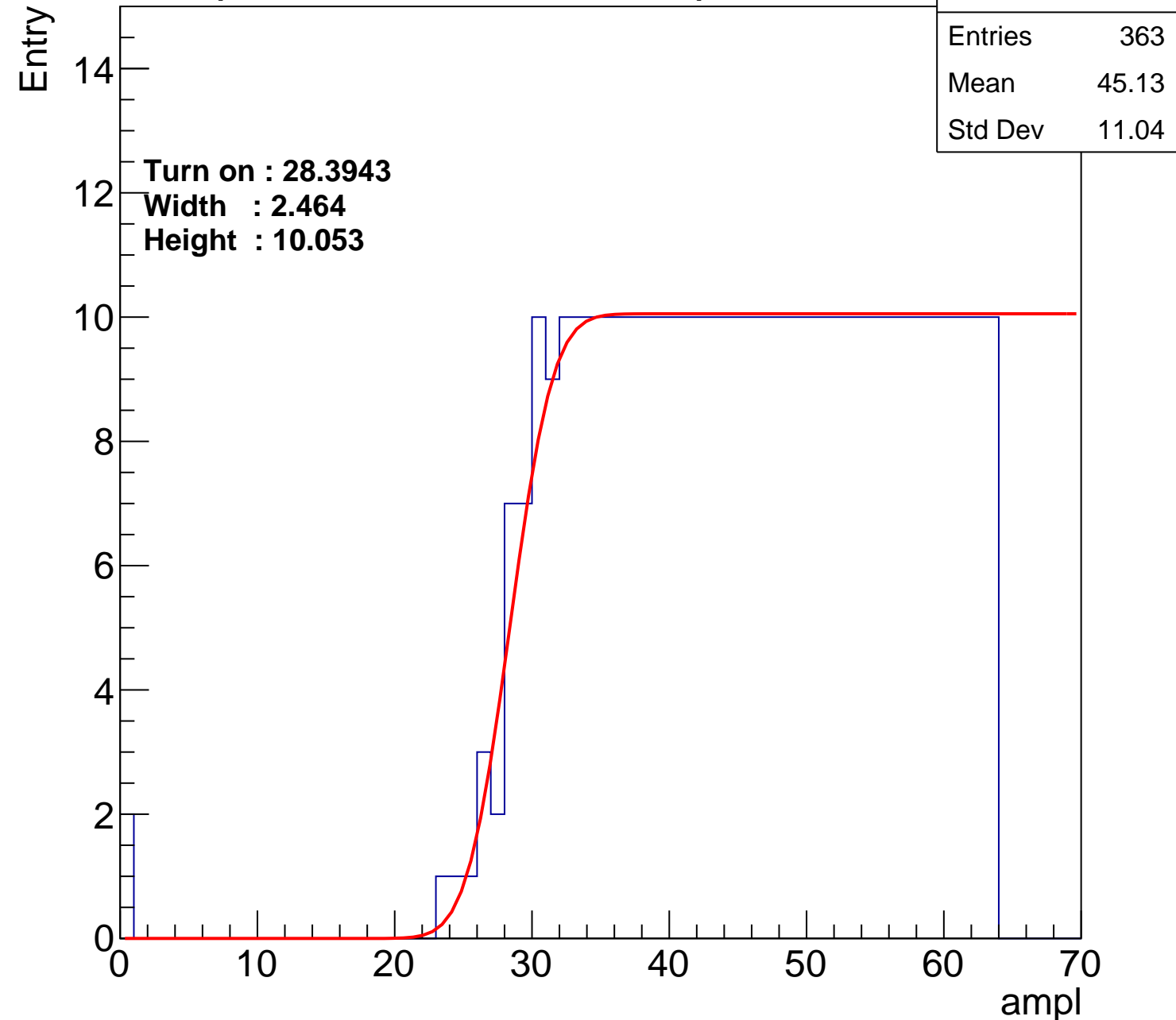
**Width : 2.464**

**Height : 10.053**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch17

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	373
Mean	44.55
Std Dev	11.51

Turn on : 26.9273

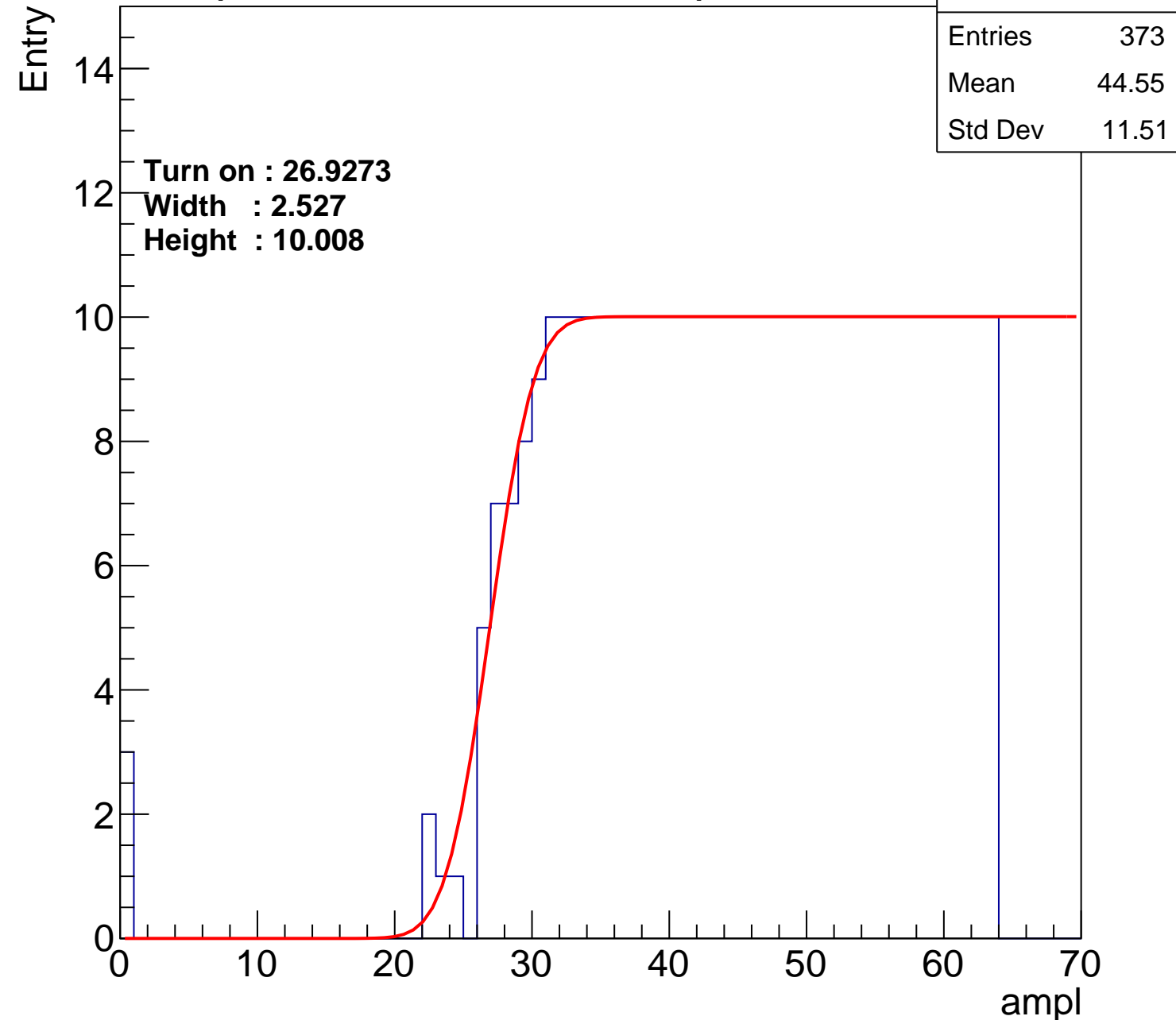
Width : 2.527

Height : 10.008

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch18

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	361
Mean	45.23
Std Dev	10.97

Turn on : 27.9926

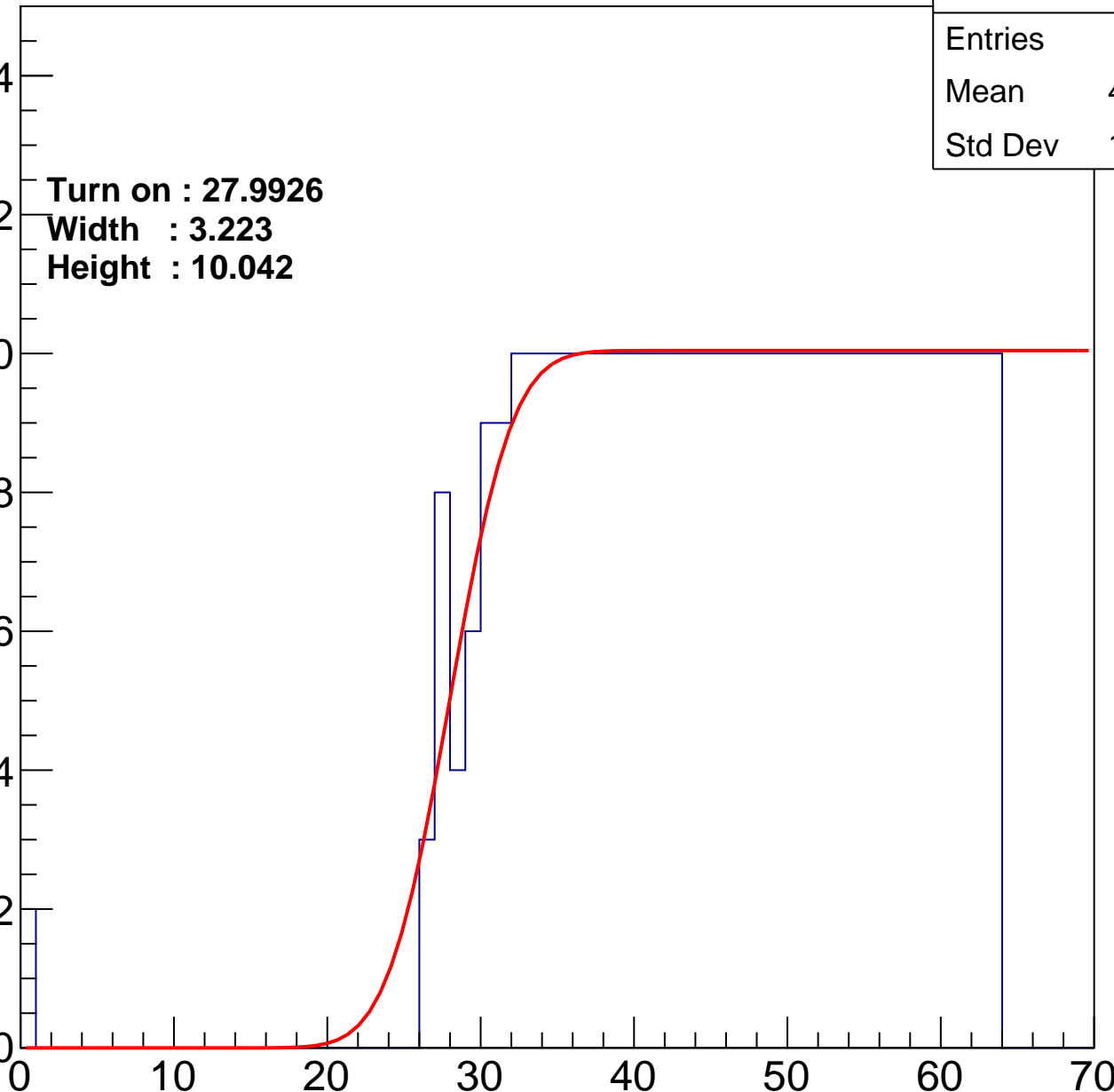
Width : 3.223

Height : 10.042

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch19

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	355
Mean	45.33
Std Dev	11.33

Turn on : 29.7386

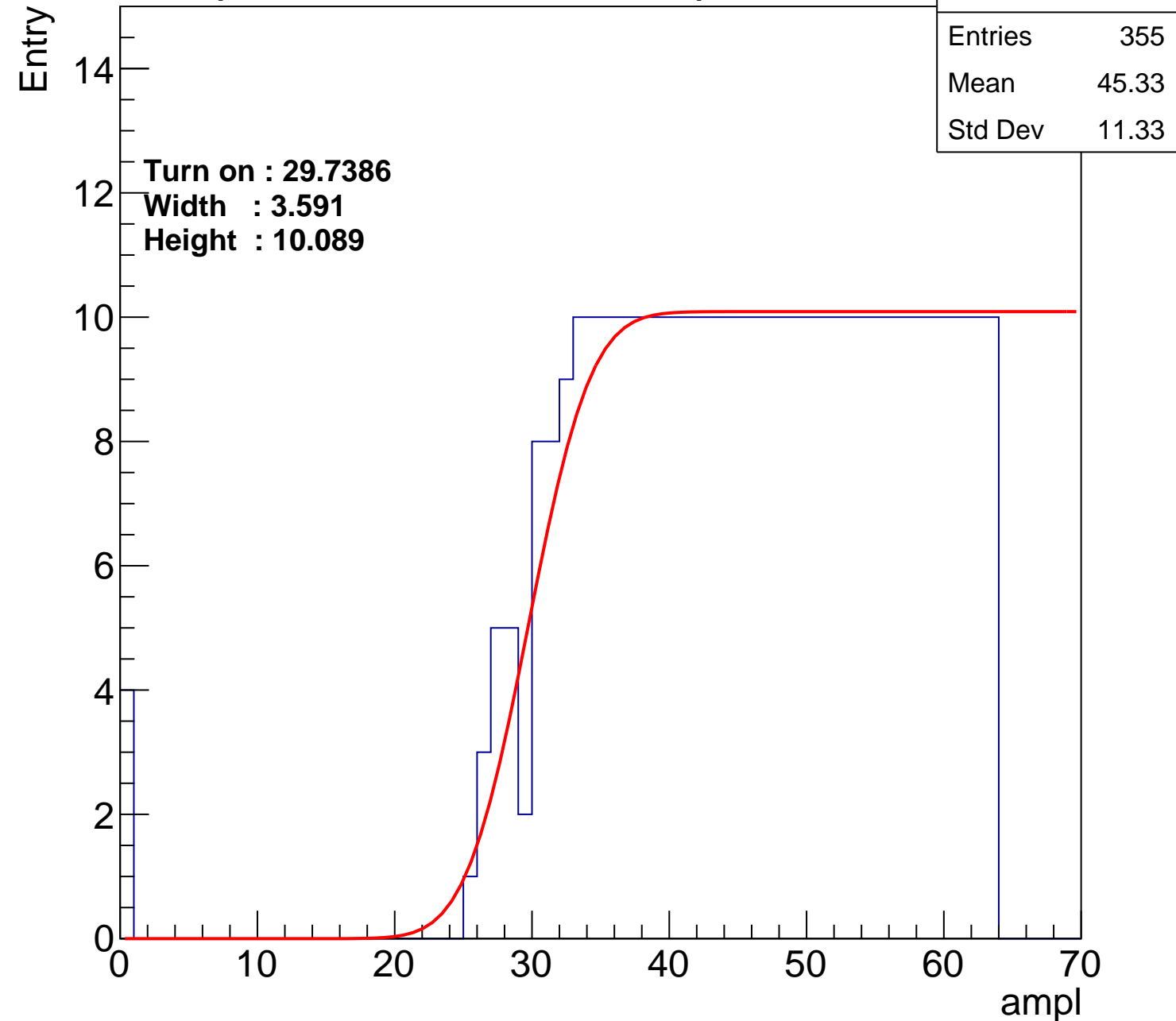
Width : 3.591

Height : 10.089

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch20

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	359
Mean	45.29
Std Dev	11

**Turn on : 28.9620**

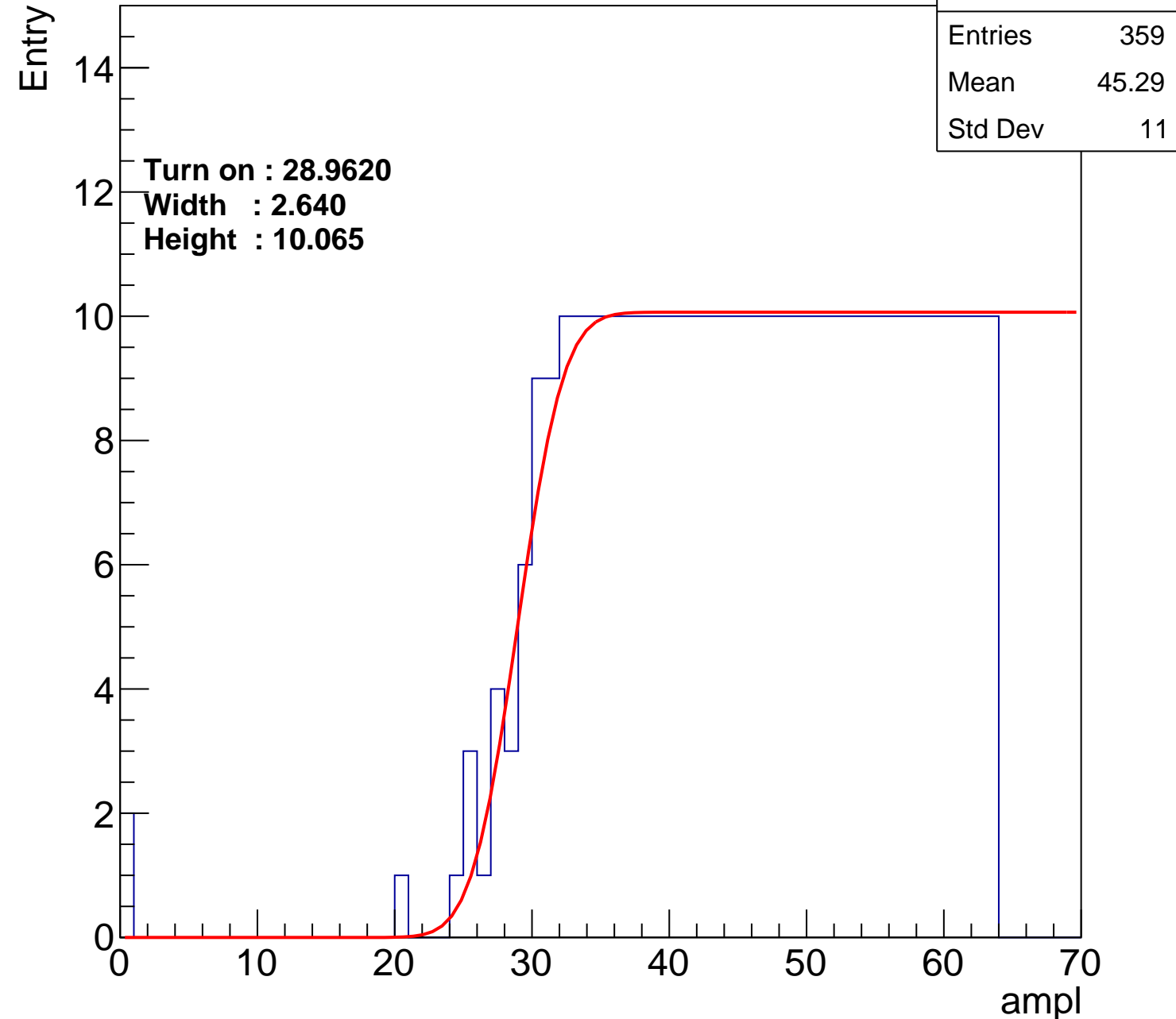
**Width : 2.640**

**Height : 10.065**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch21

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	363
Mean	44.94
Std Dev	11.51

Turn on : 28.3436

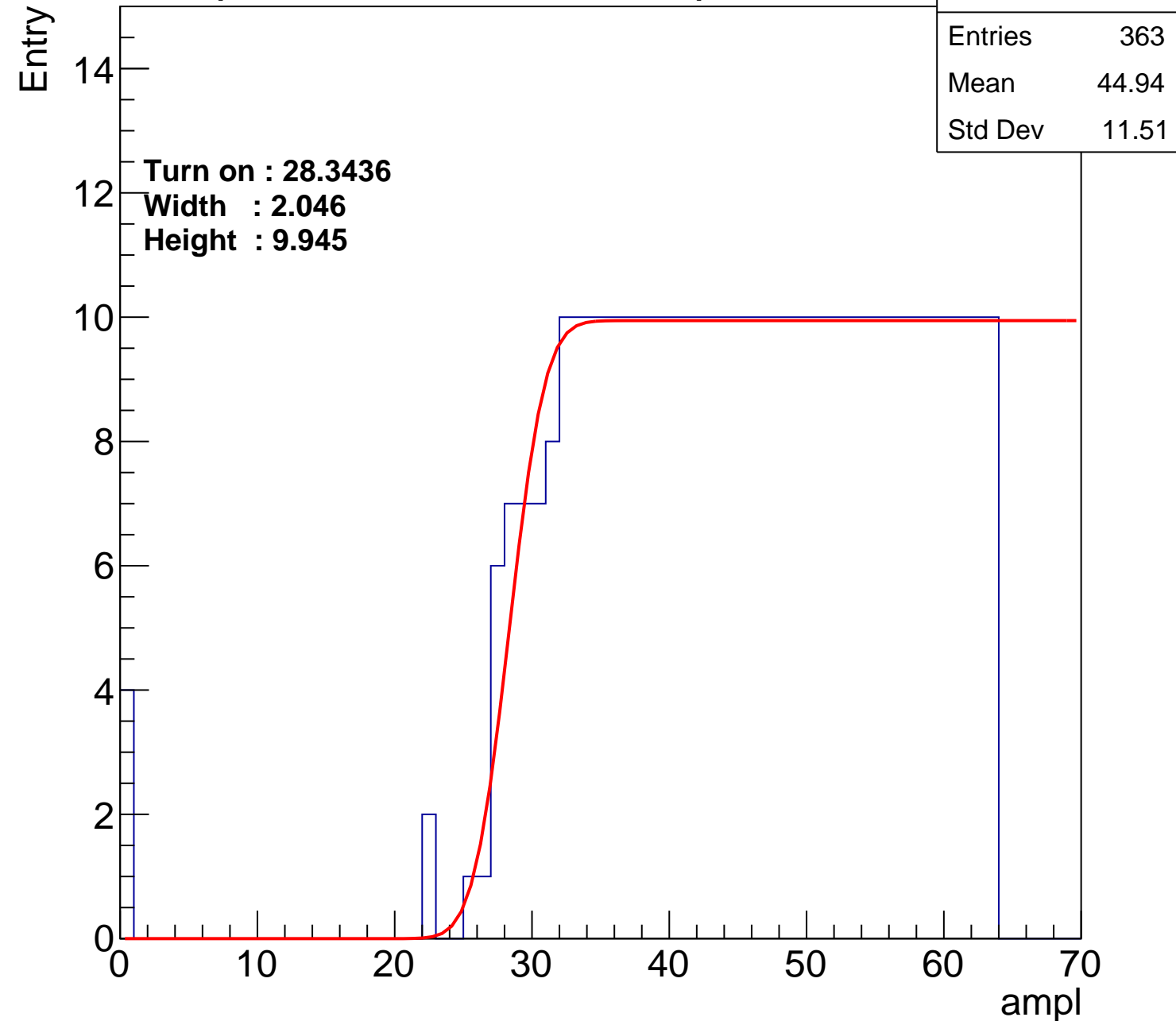
Width : 2.046

Height : 9.945

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch22

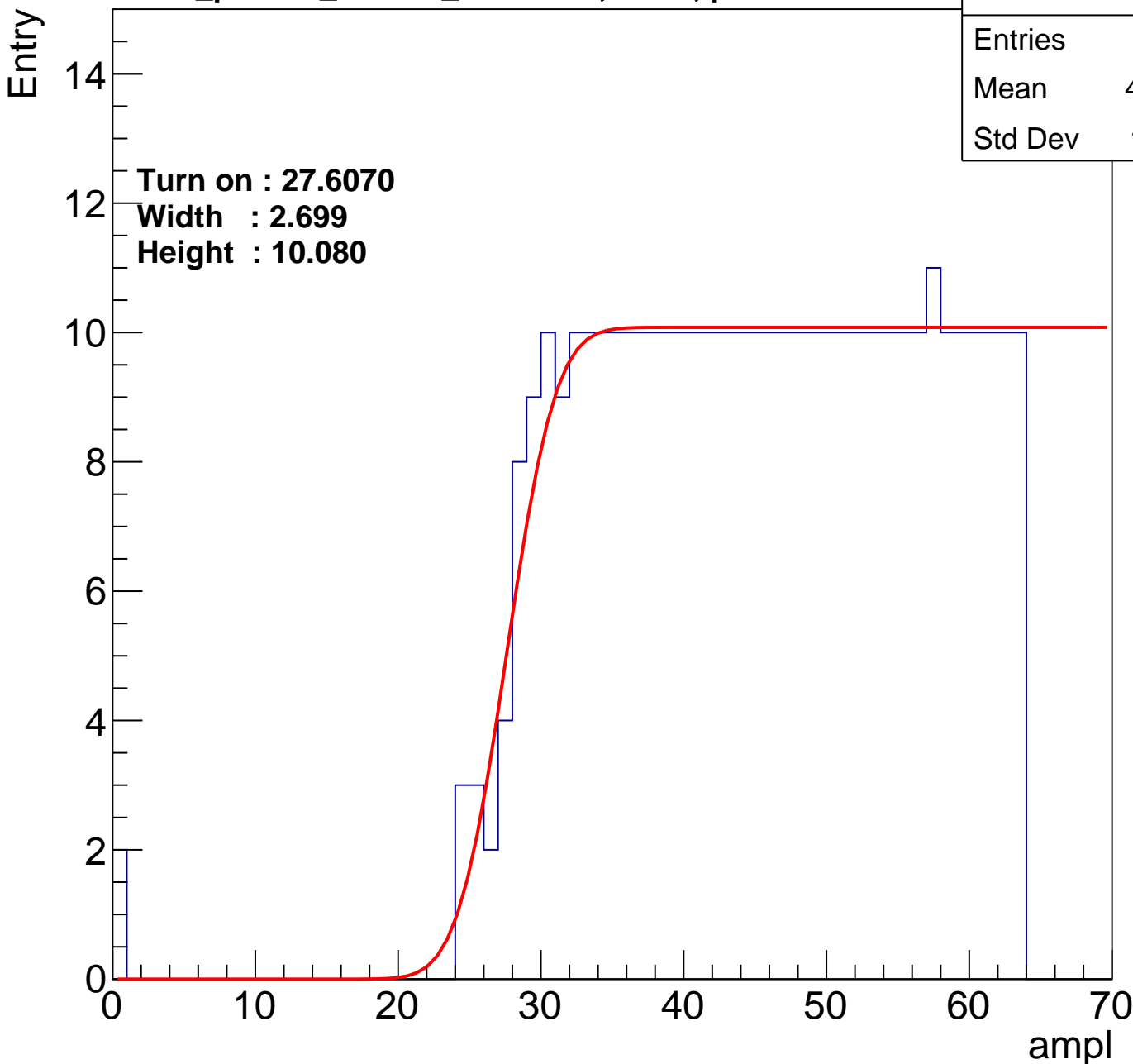
**calib\_packv5\_042523\_0143.root, FC#9, port A1**

Entries	371
Mean	44.82
Std Dev	11.21

**Turn on : 27.6070**

**Width : 2.699**

**Height : 10.080**





# B0L001S, U24-ch23

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	381
Mean	44.25
Std Dev	11.48

Turn on : 26.0538

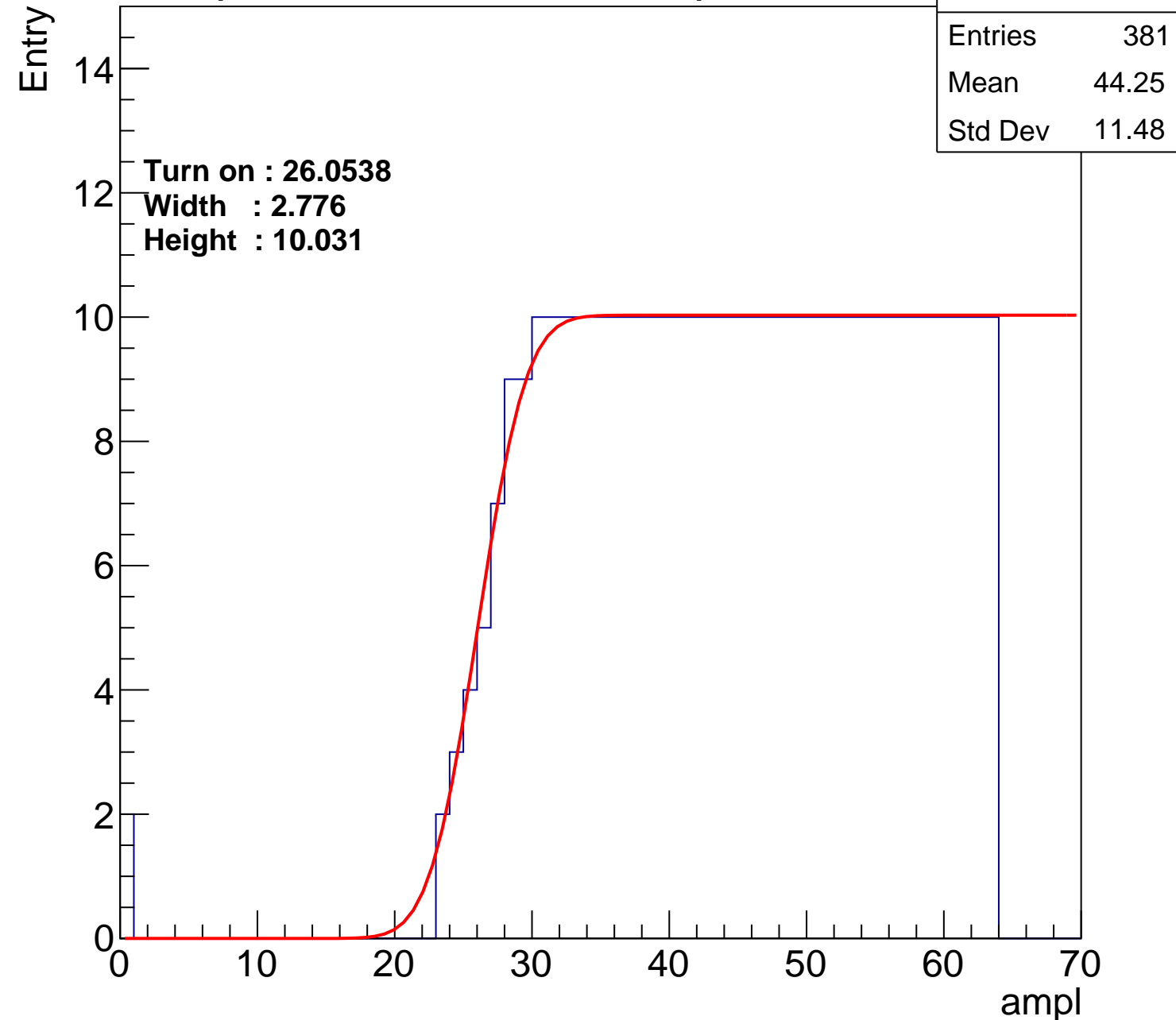
Width : 2.776

Height : 10.031

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch24

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	370
Mean	44.82
Std Dev	11.38

Turn on : 27.5424

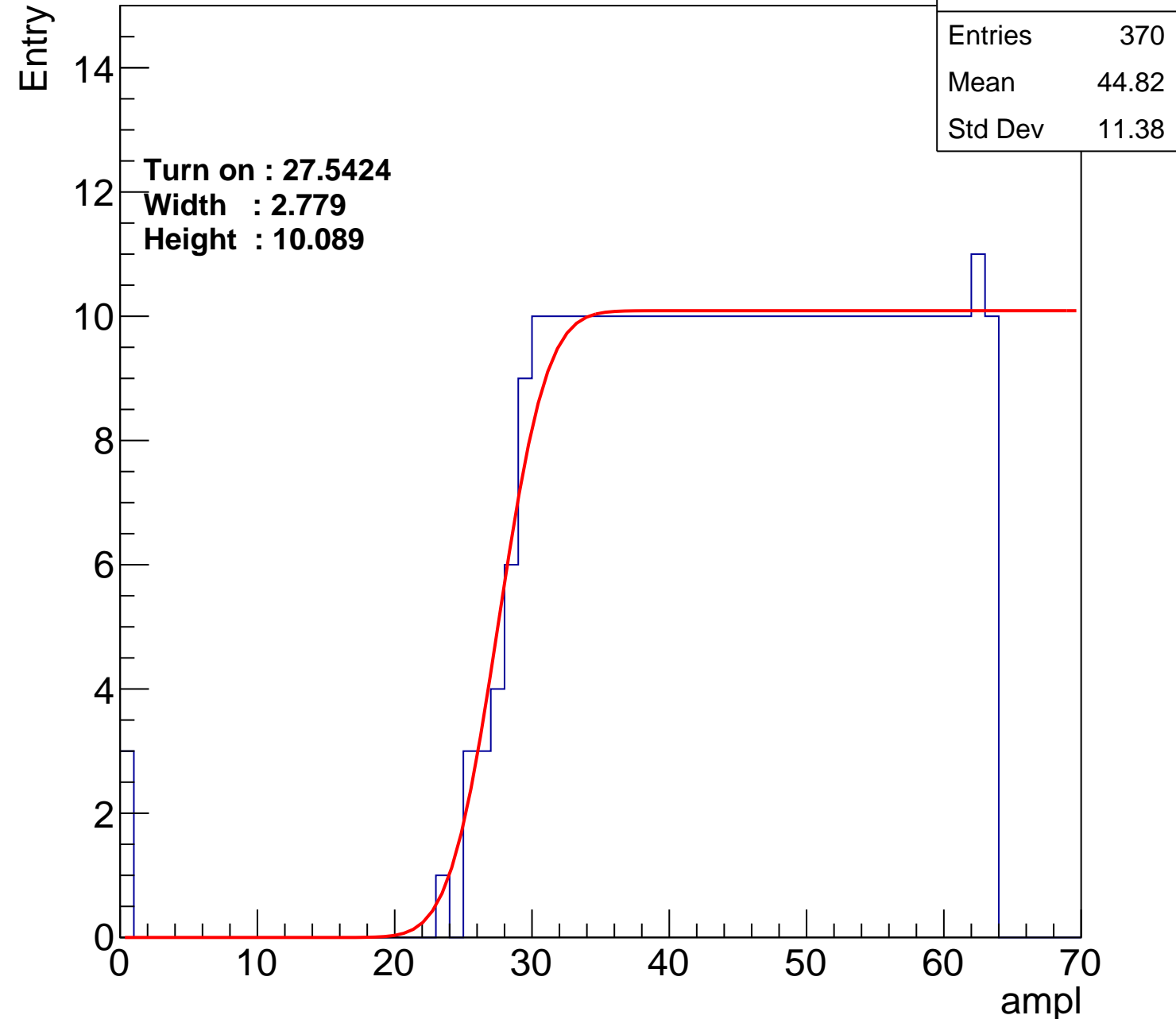
Width : 2.779

Height : 10.089

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch25

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	362
Mean	45.28
Std Dev	10.75

Turn on : 28.0652

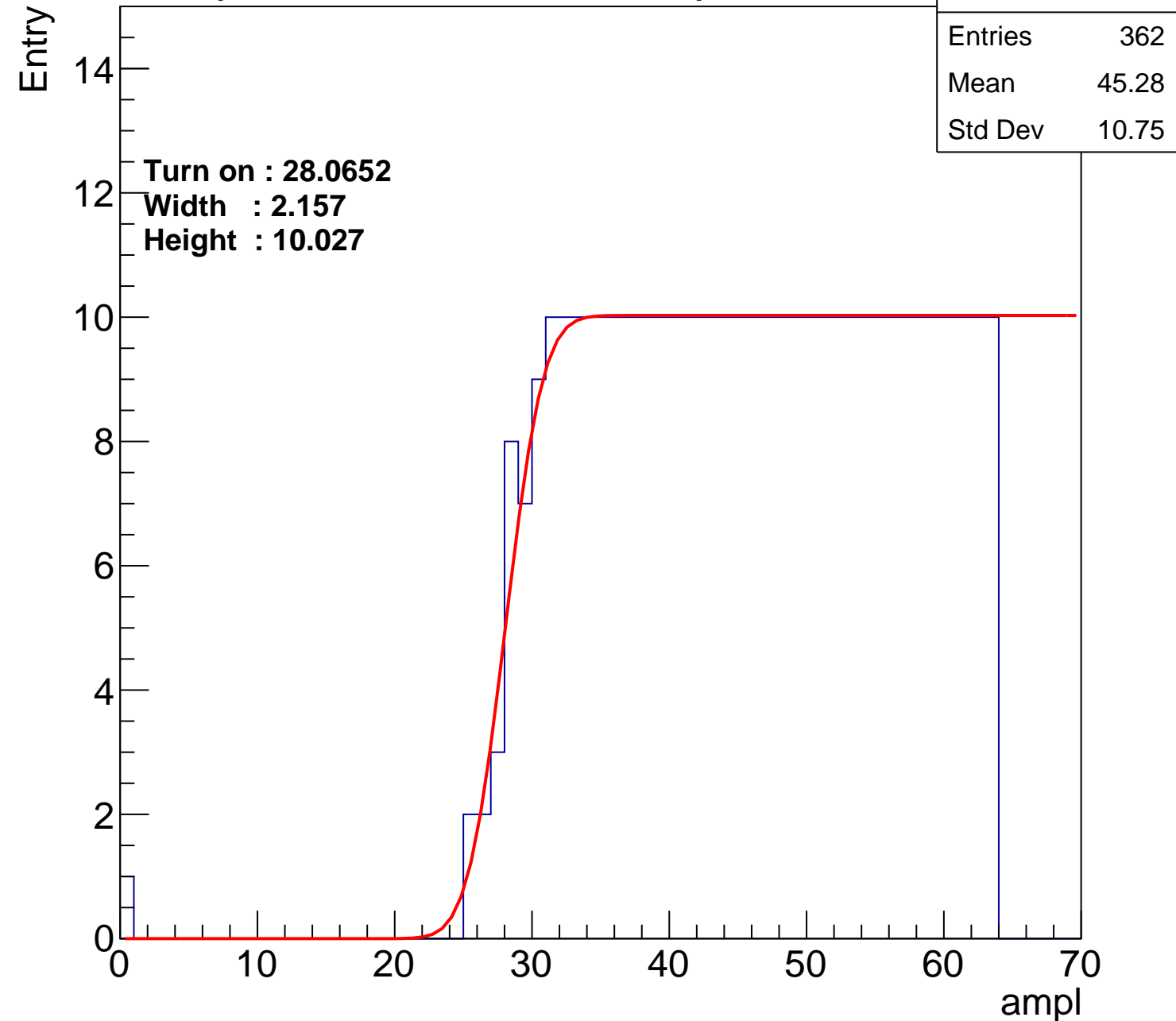
Width : 2.157

Height : 10.027

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch26

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	362
Mean	45.11
Std Dev	11.29

**Turn on : 28.6367**

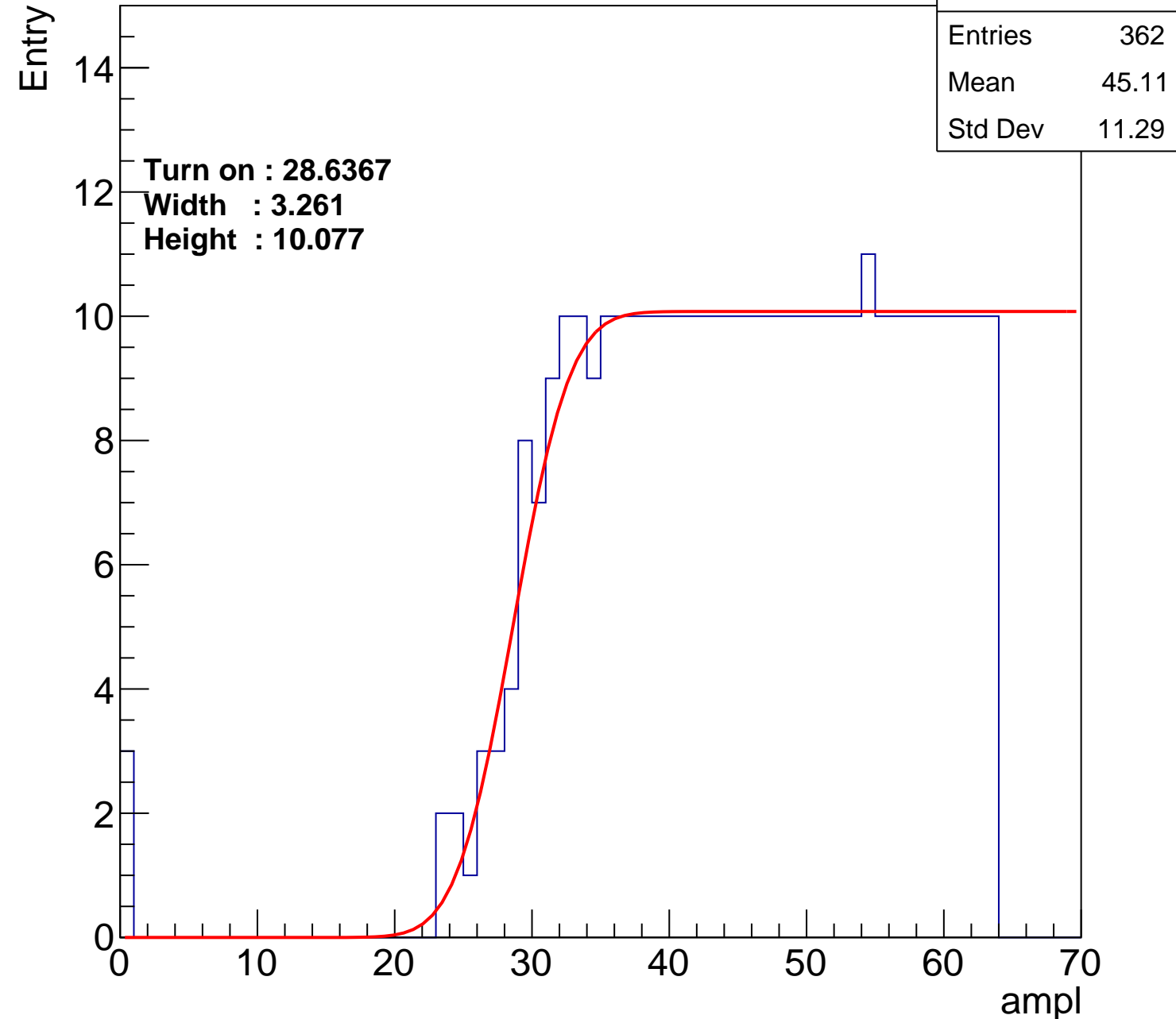
**Width : 3.261**

**Height : 10.077**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch27

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	351
Mean	45.71
Std Dev	10.76

Turn on : 29.5221

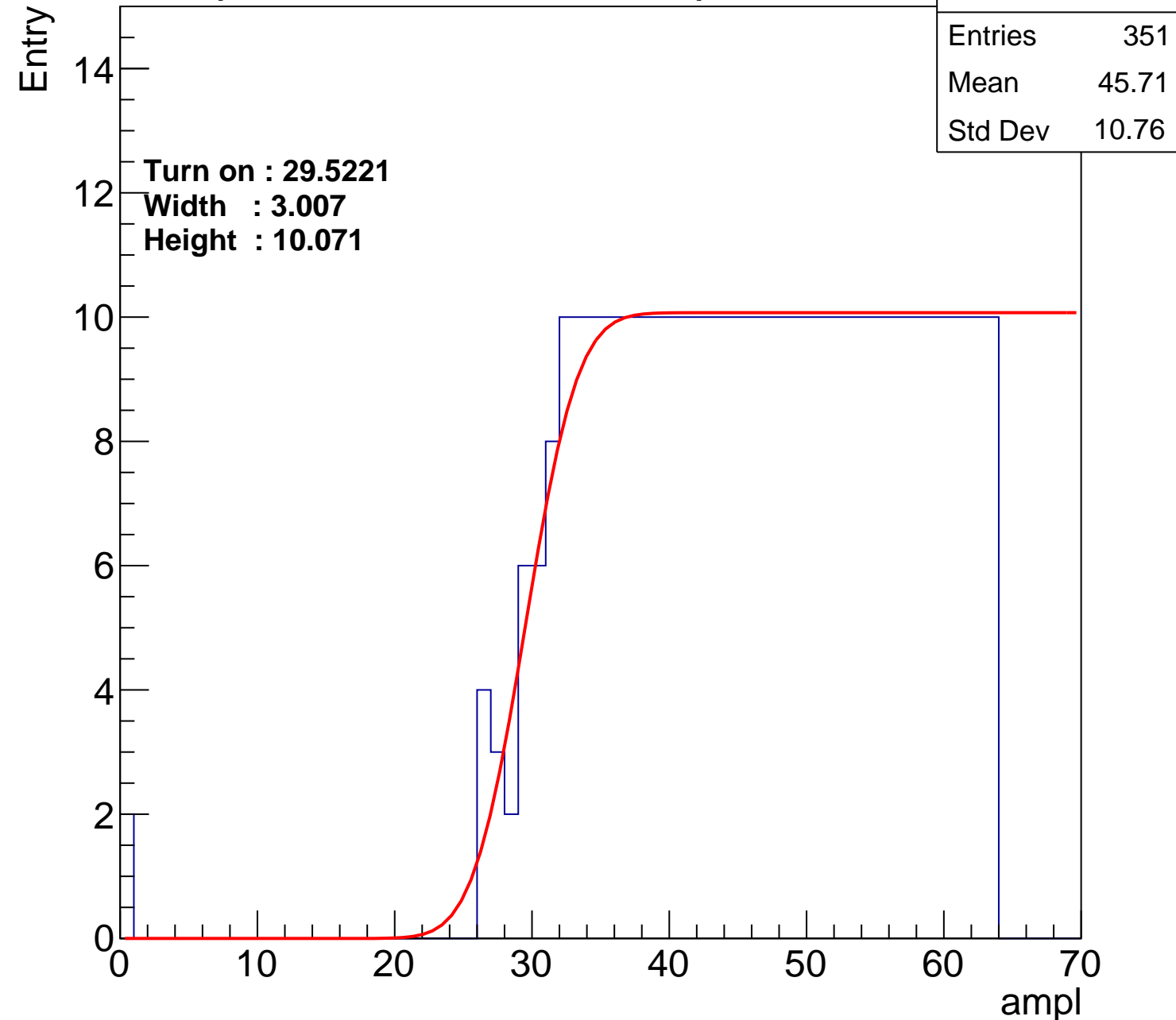
Width : 3.007

Height : 10.071

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch28

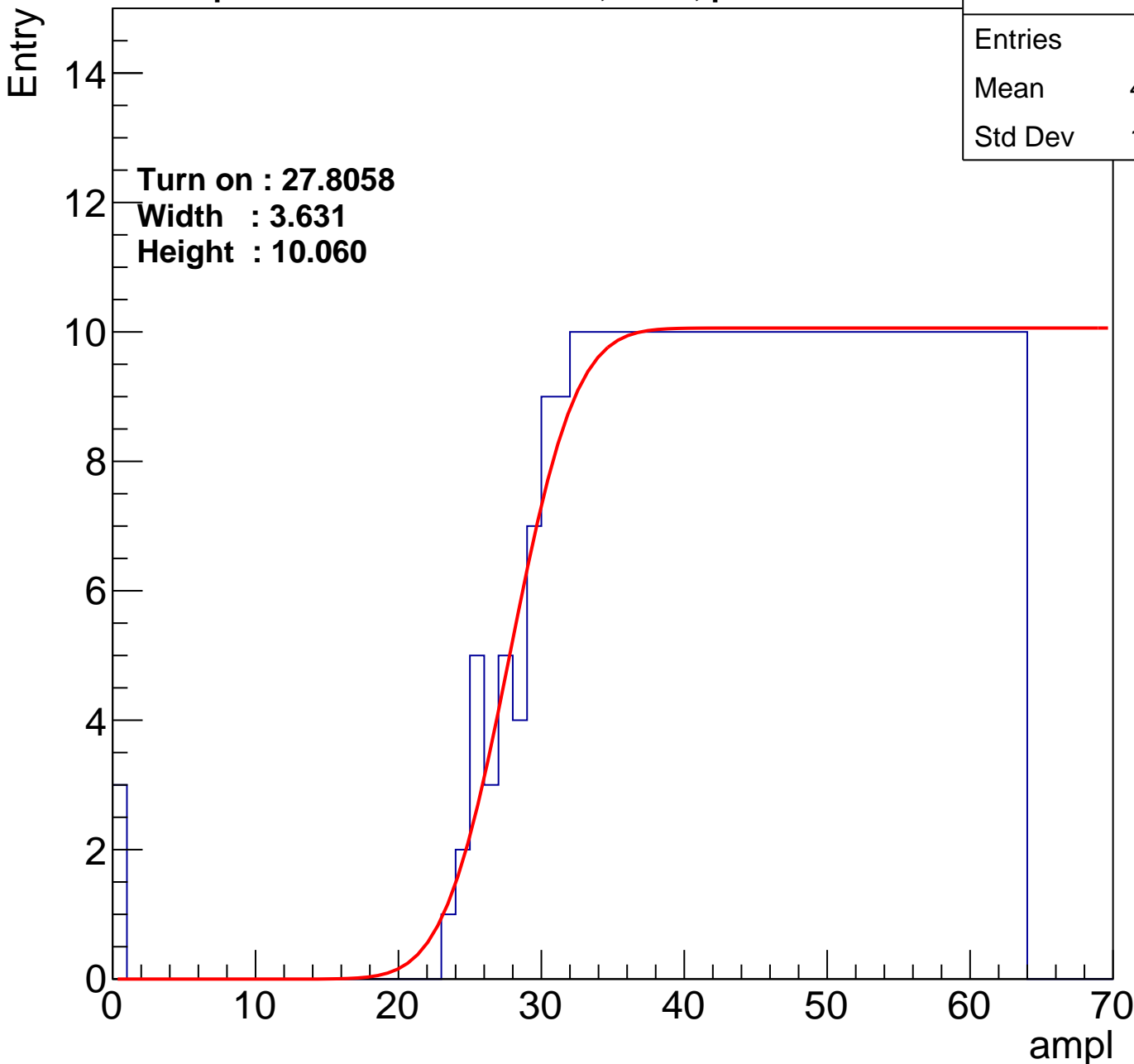
**calib\_packv5\_042523\_0143.root, FC#9, port A1**

Entries	368
Mean	44.76
Std Dev	11.44

**Turn on : 27.8058**

**Width : 3.631**

**Height : 10.060**



# B0L001S, U24-ch29

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	339
Mean	46.28
Std Dev	10.49

Turn on : 30.3635

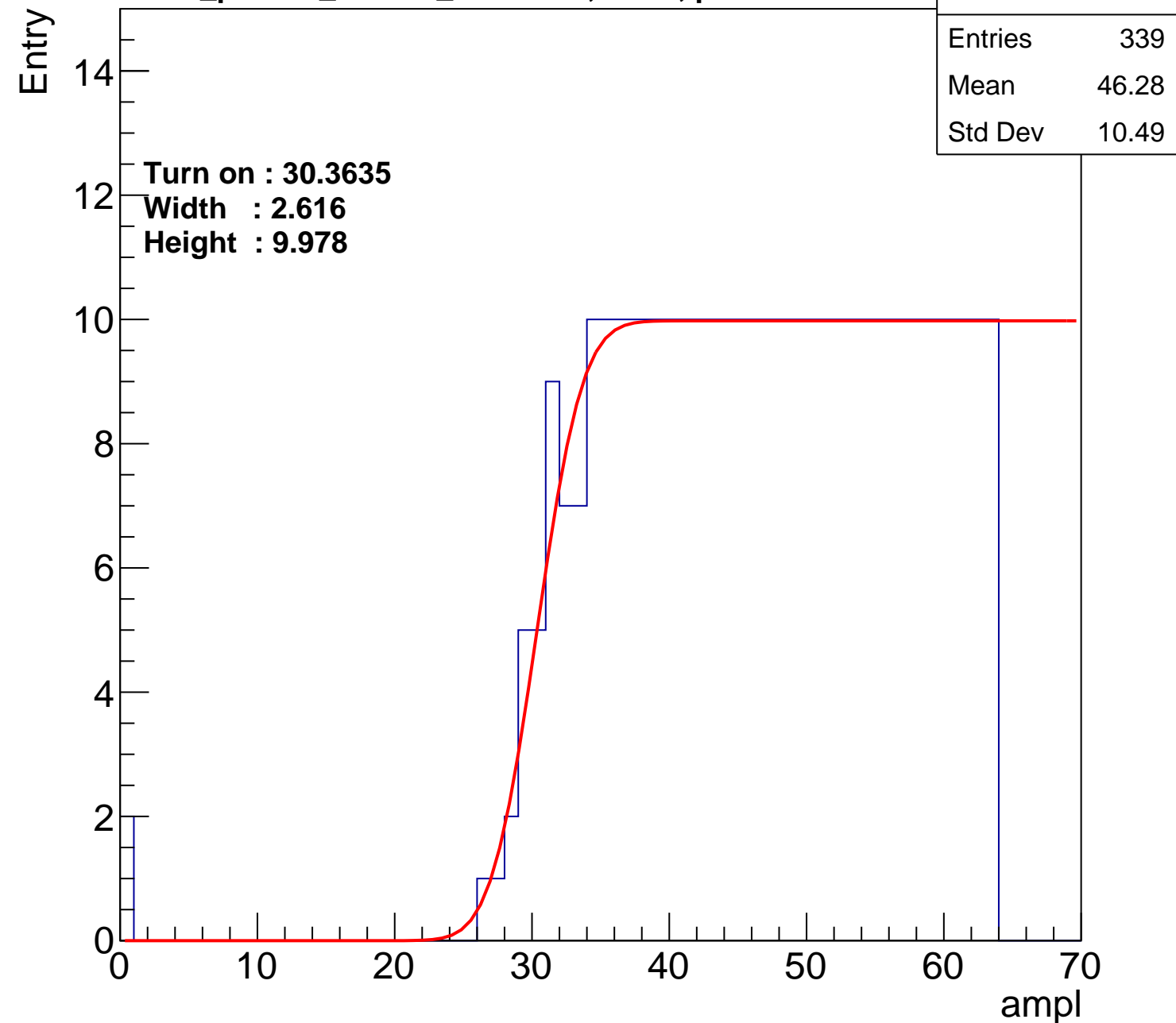
Width : 2.616

Height : 9.978

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch30

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	384
Mean	43.8
Std Dev	12.3

**Turn on : 26.2535**

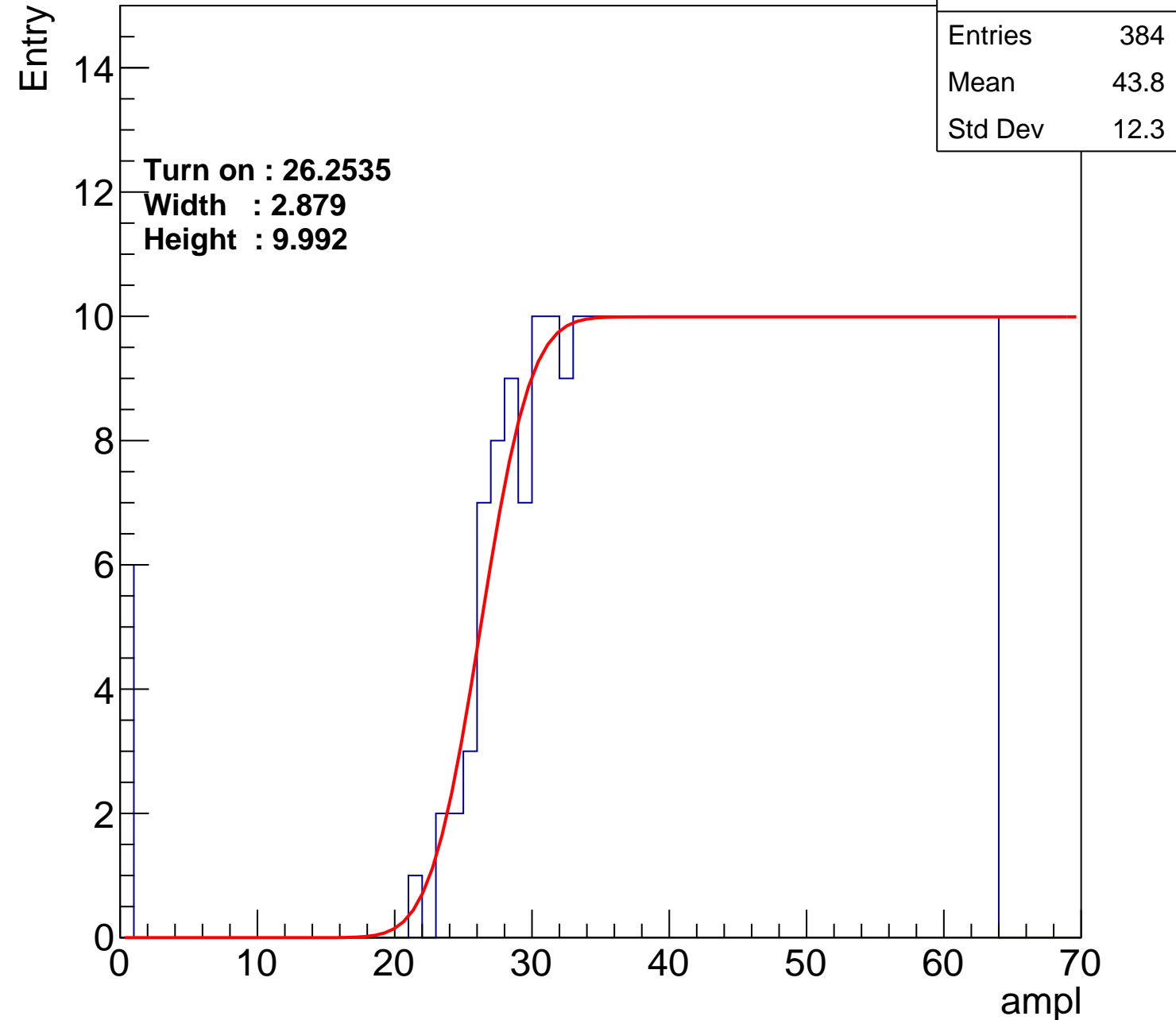
**Width : 2.879**

**Height : 9.992**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U24-ch31

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	351
Mean	45.58
Std Dev	11.07

Turn on : 29.5192

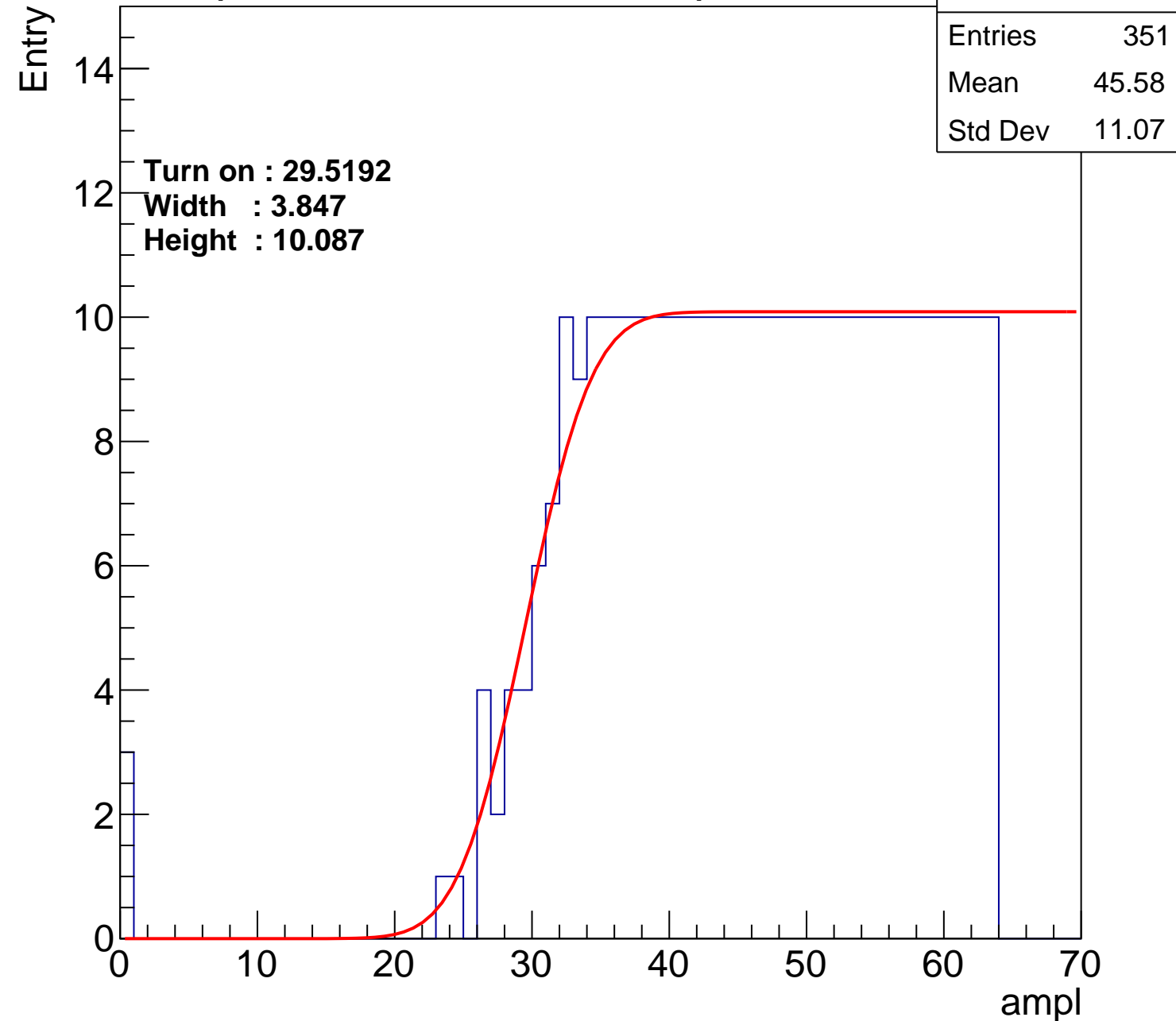
Width : 3.847

Height : 10.087

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch32

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	373
Mean	44.39
Std Dev	11.91

Turn on : 27.0481

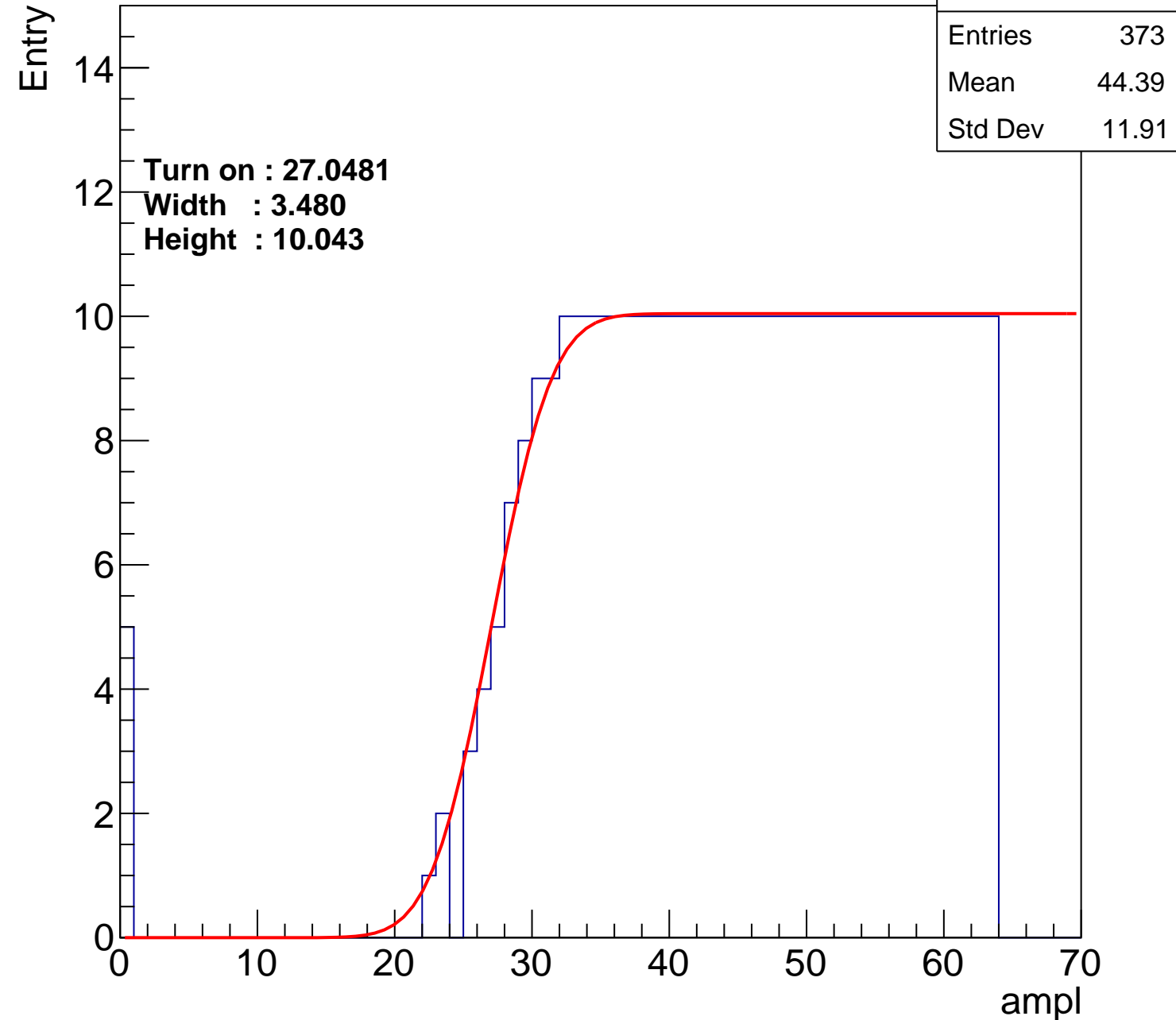
Width : 3.480

Height : 10.043

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch33

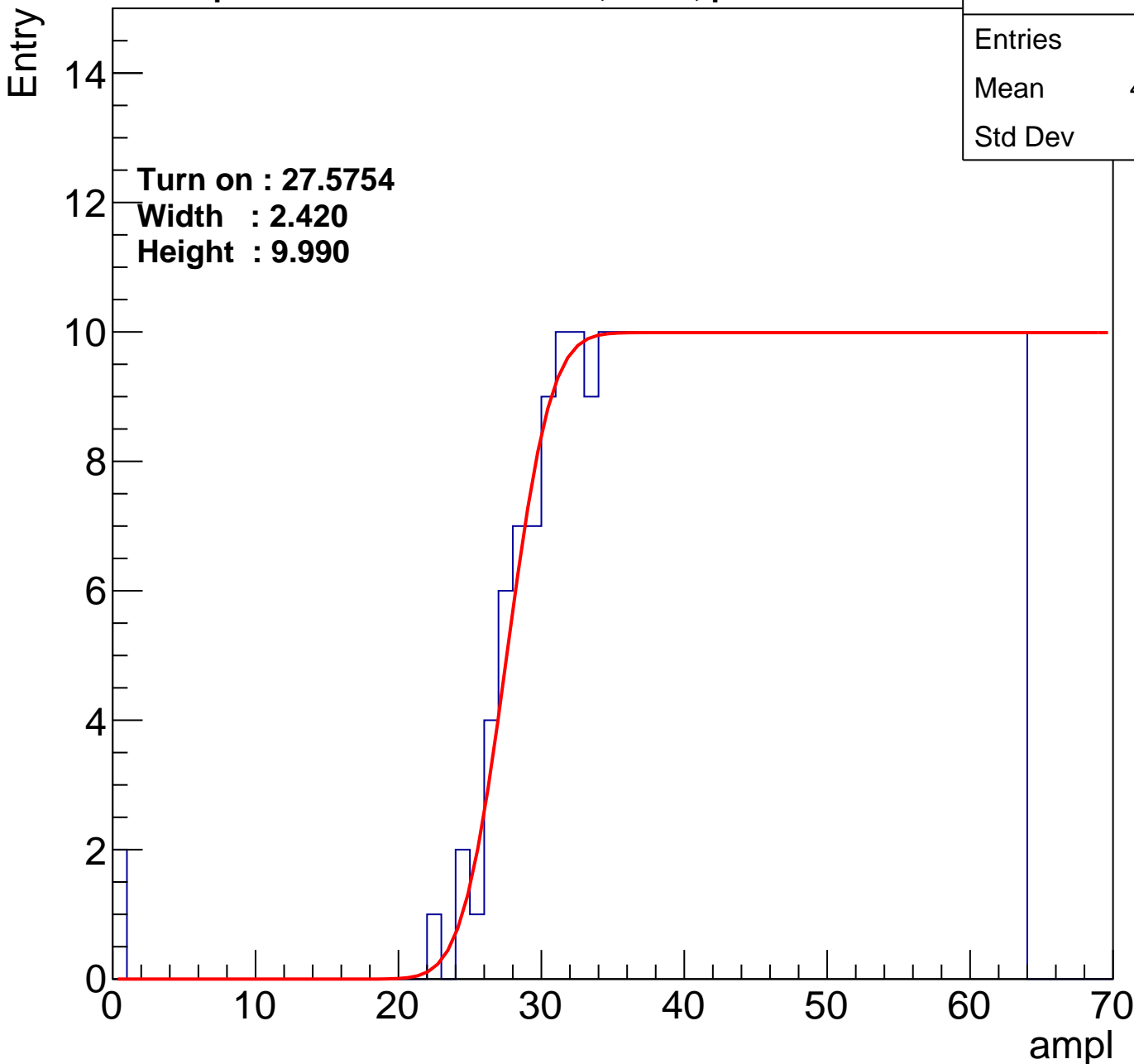
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	368
Mean	44.86
Std Dev	11.2

Turn on : 27.5754

Width : 2.420

Height : 9.990



# B0L001S, U24-ch34

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	368
Mean	44.92
Std Dev	11.01

Turn on : 27.5826

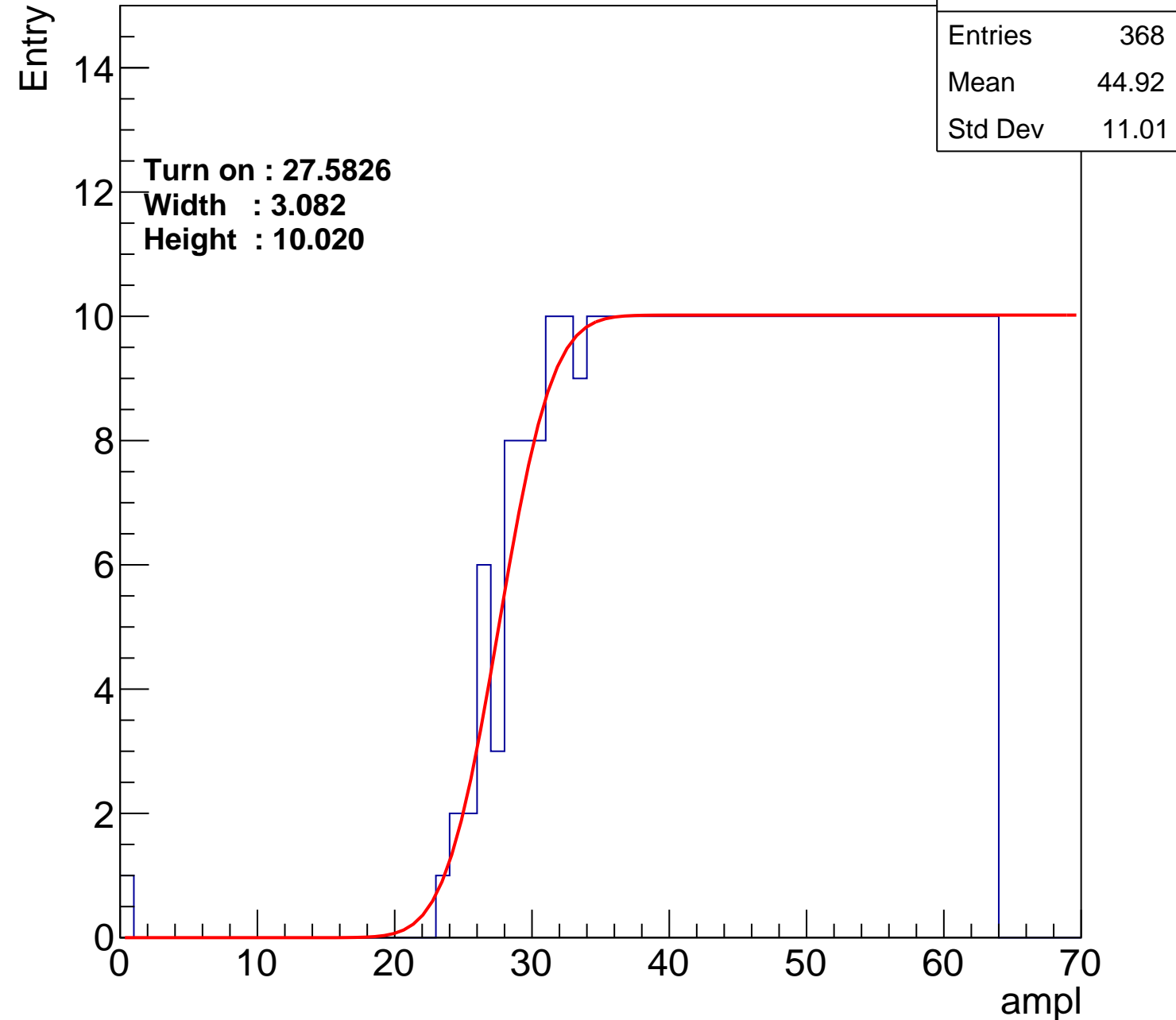
Width : 3.082

Height : 10.020

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch35

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	364
Mean	45.04
Std Dev	11.27

Turn on : 28.4104

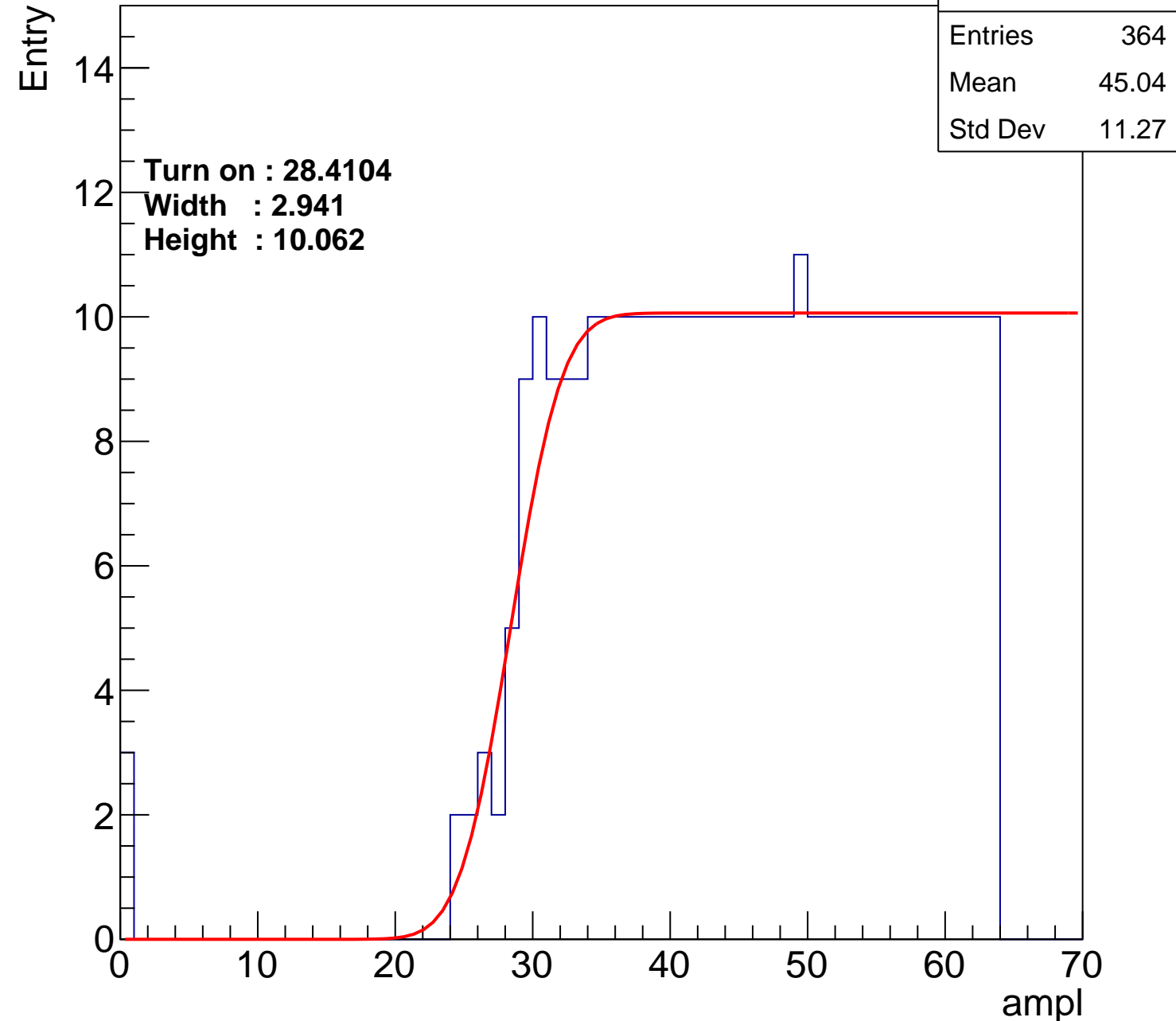
Width : 2.941

Height : 10.062

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch36

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	341
Mean	46.23
Std Dev	10.34

**Turn on : 30.2033**

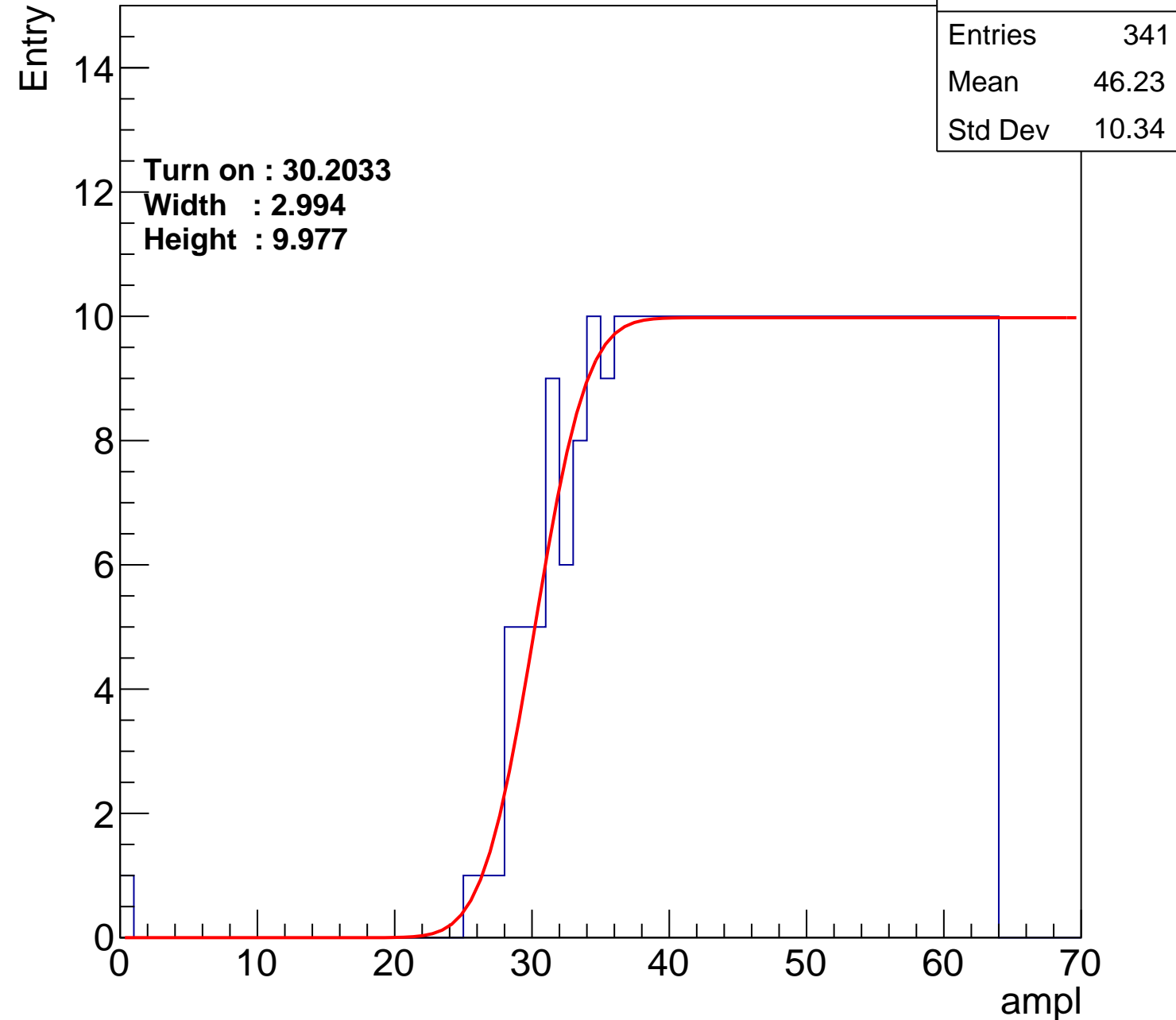
**Width : 2.994**

**Height : 9.977**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch37

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	350
Mean	45.78
Std Dev	10.69

Turn on : 28.7656

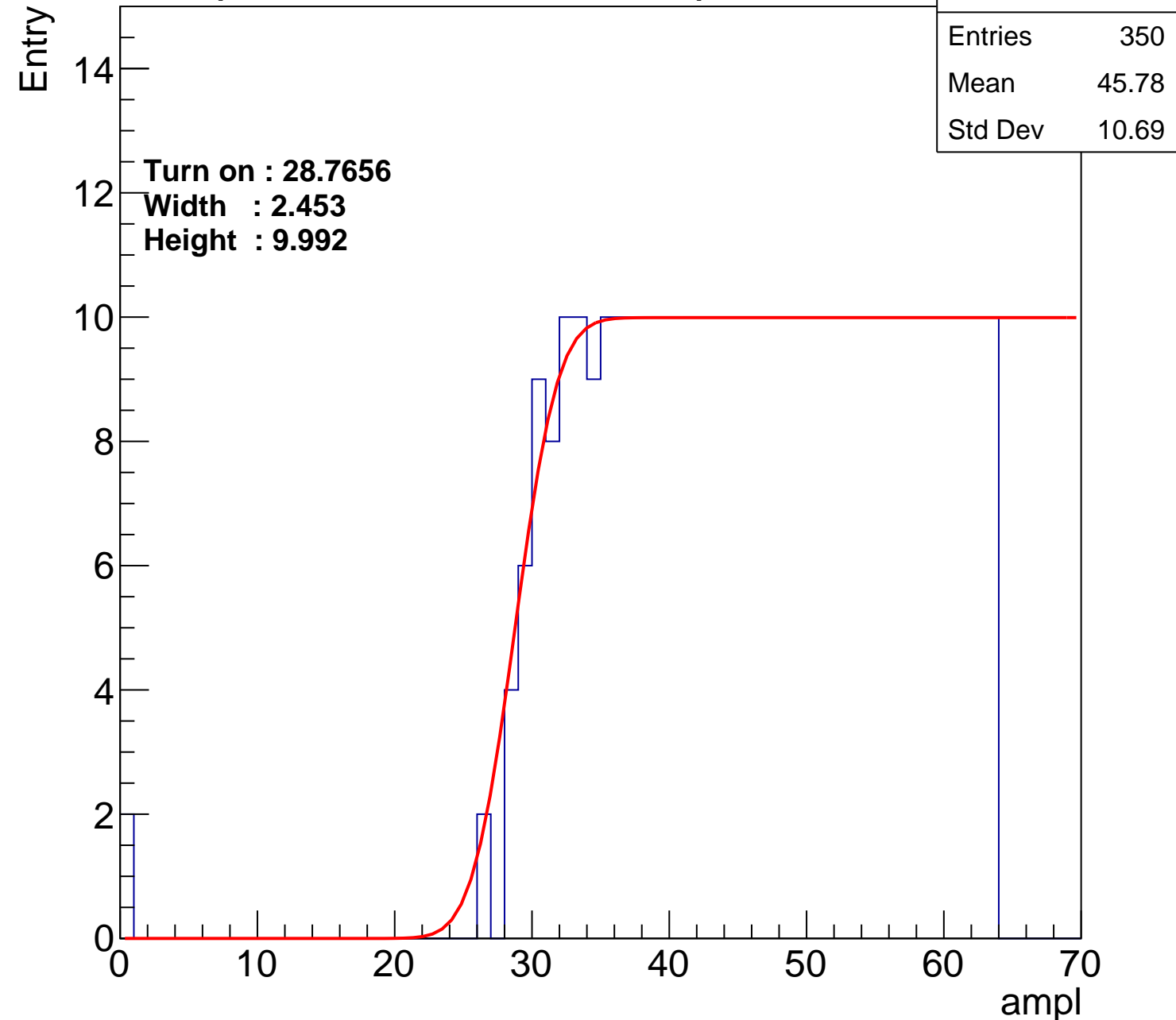
Width : 2.453

Height : 9.992

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



**calib\_packv5\_042523\_0143.root, FC#9, port A1**

Entries	395
Mean	43.5
Std Dev	12.01

Std Dev	12.01
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**Height : 10.034**

**Height : 10.034**





# B0L001S, U24-ch39

calib\_packv5\_042523\_0143.root, FC#9, port A1

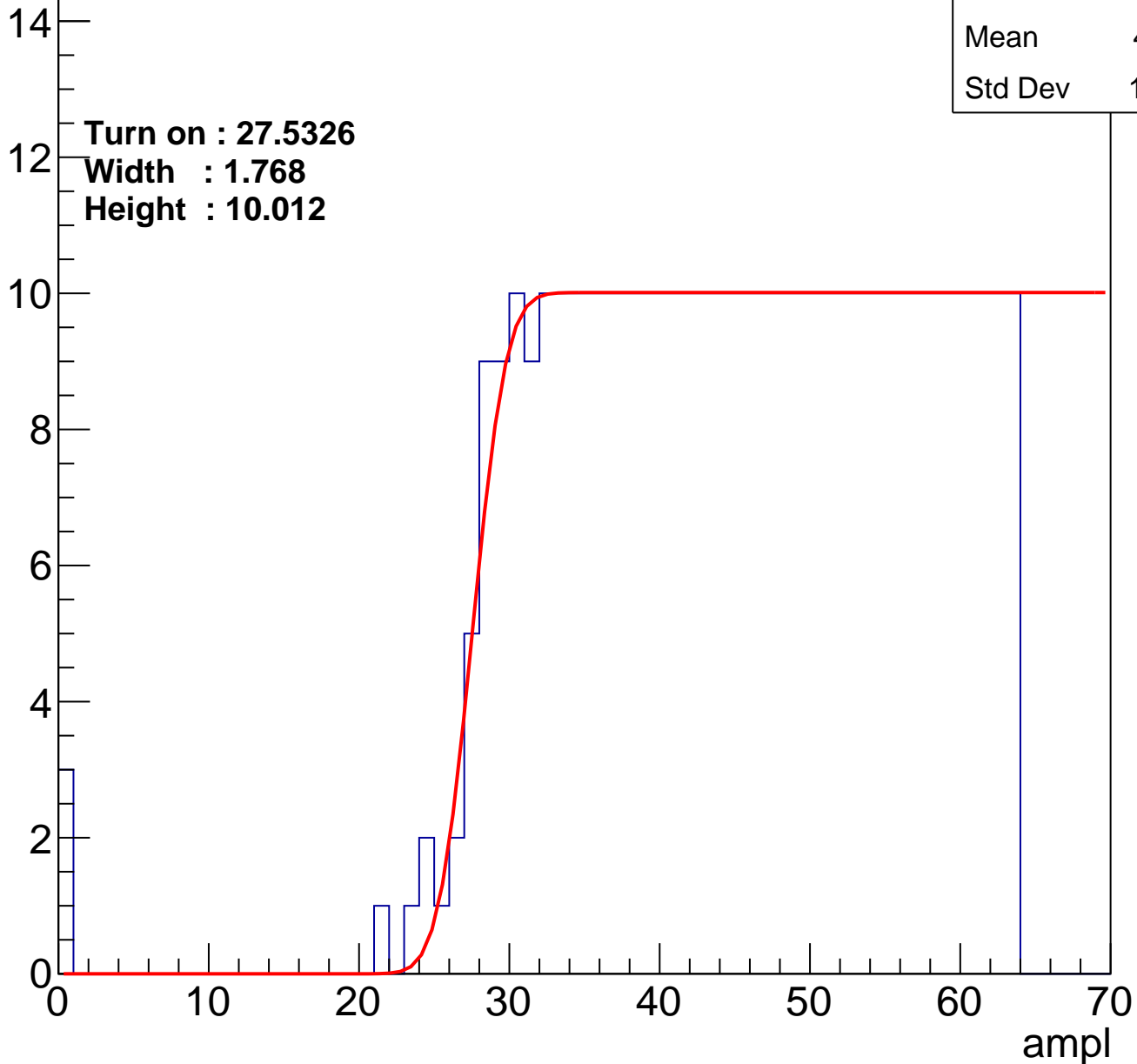
Entries	372
Mean	44.61
Std Dev	11.47

Turn on : 27.5326

Width : 1.768

Height : 10.012

Entry



# B0L001S, U24-ch40

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	343
Mean	45.94
Std Dev	10.92

Turn on : 30.2468

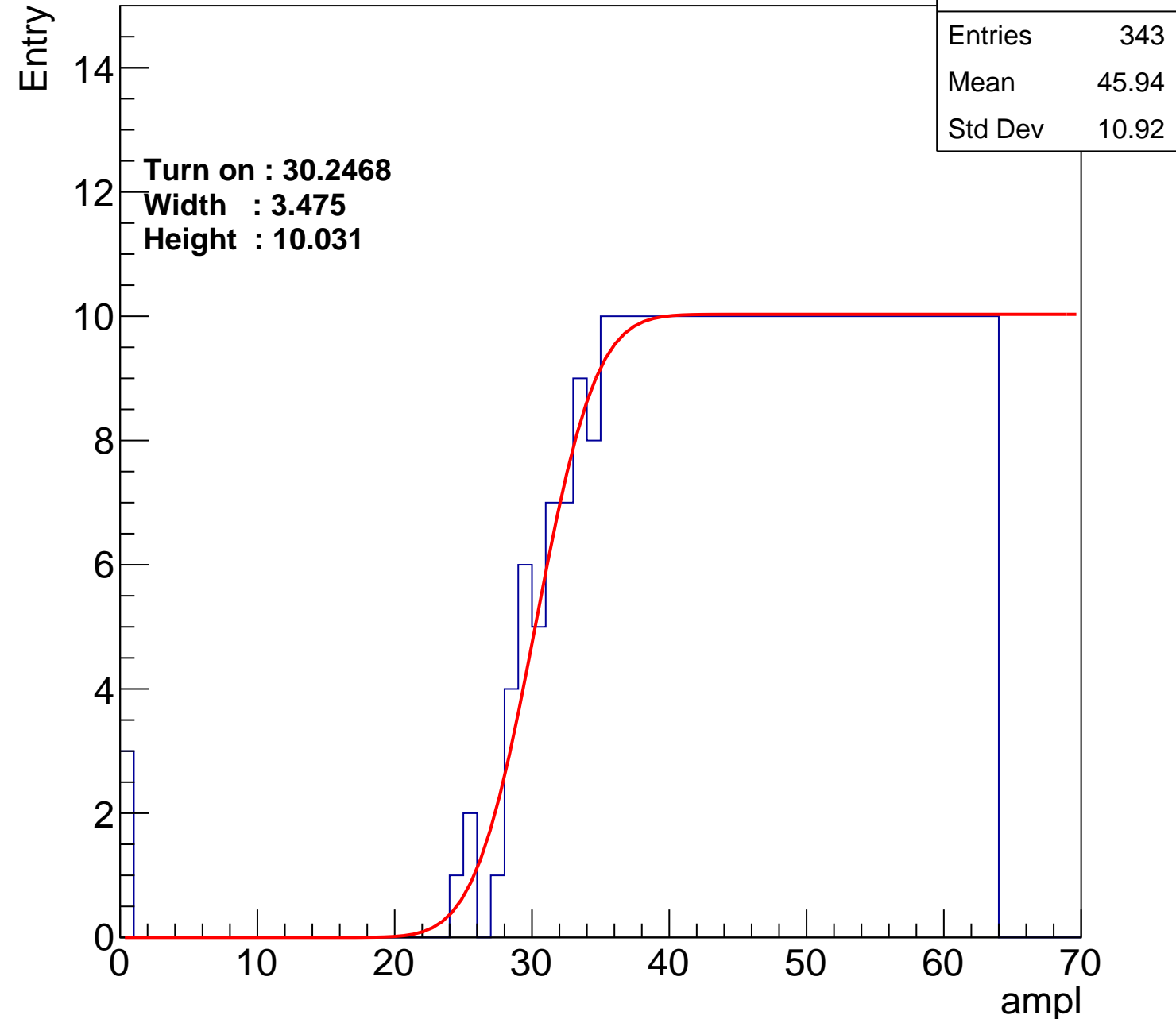
Width : 3.475

Height : 10.031

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch41

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	361
Mean	45.28
Std Dev	10.8

Turn on : 28.3198

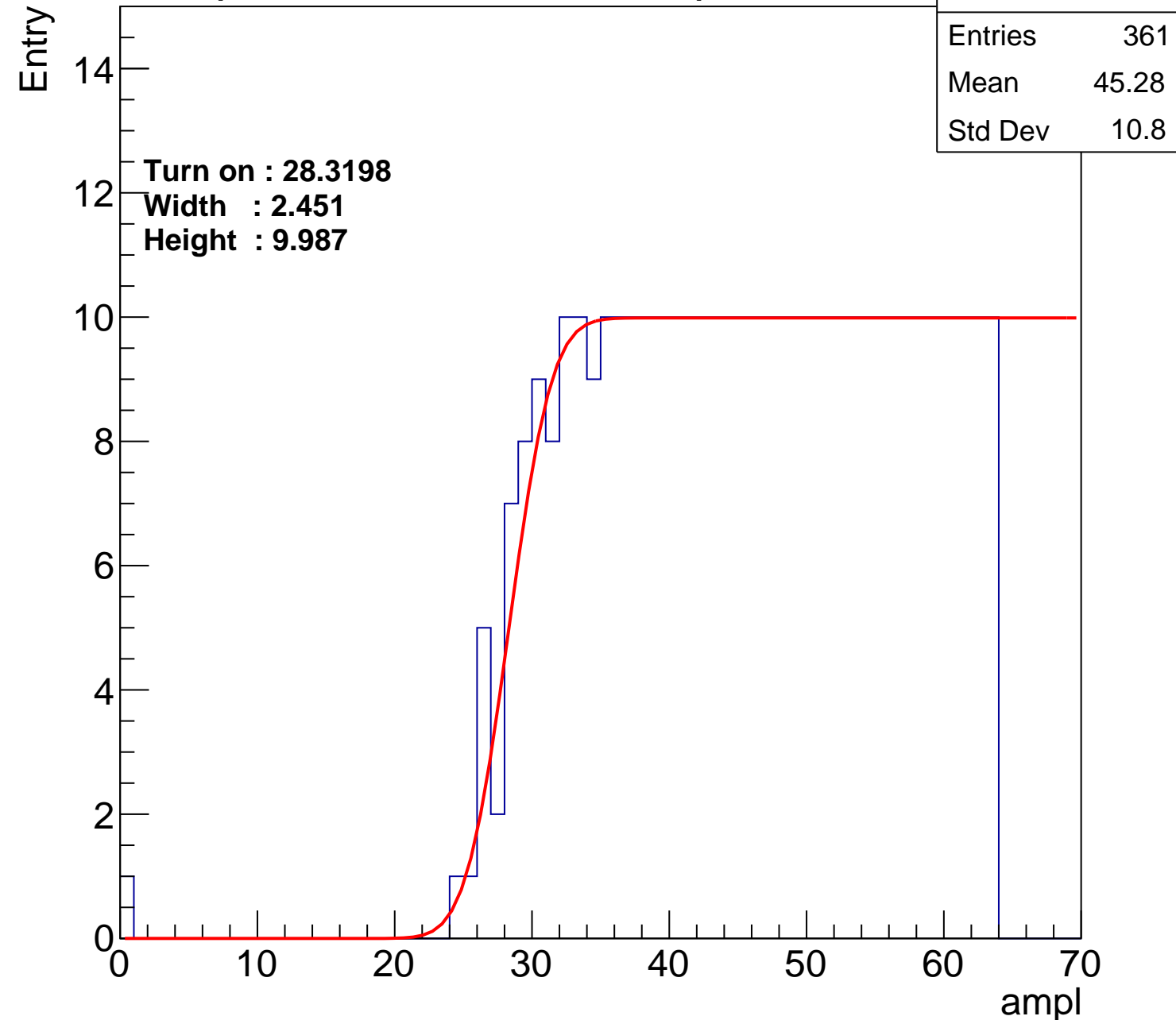
Width : 2.451

Height : 9.987

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch42

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	377
Mean	44.42
Std Dev	11.42

Turn on : 26.7710

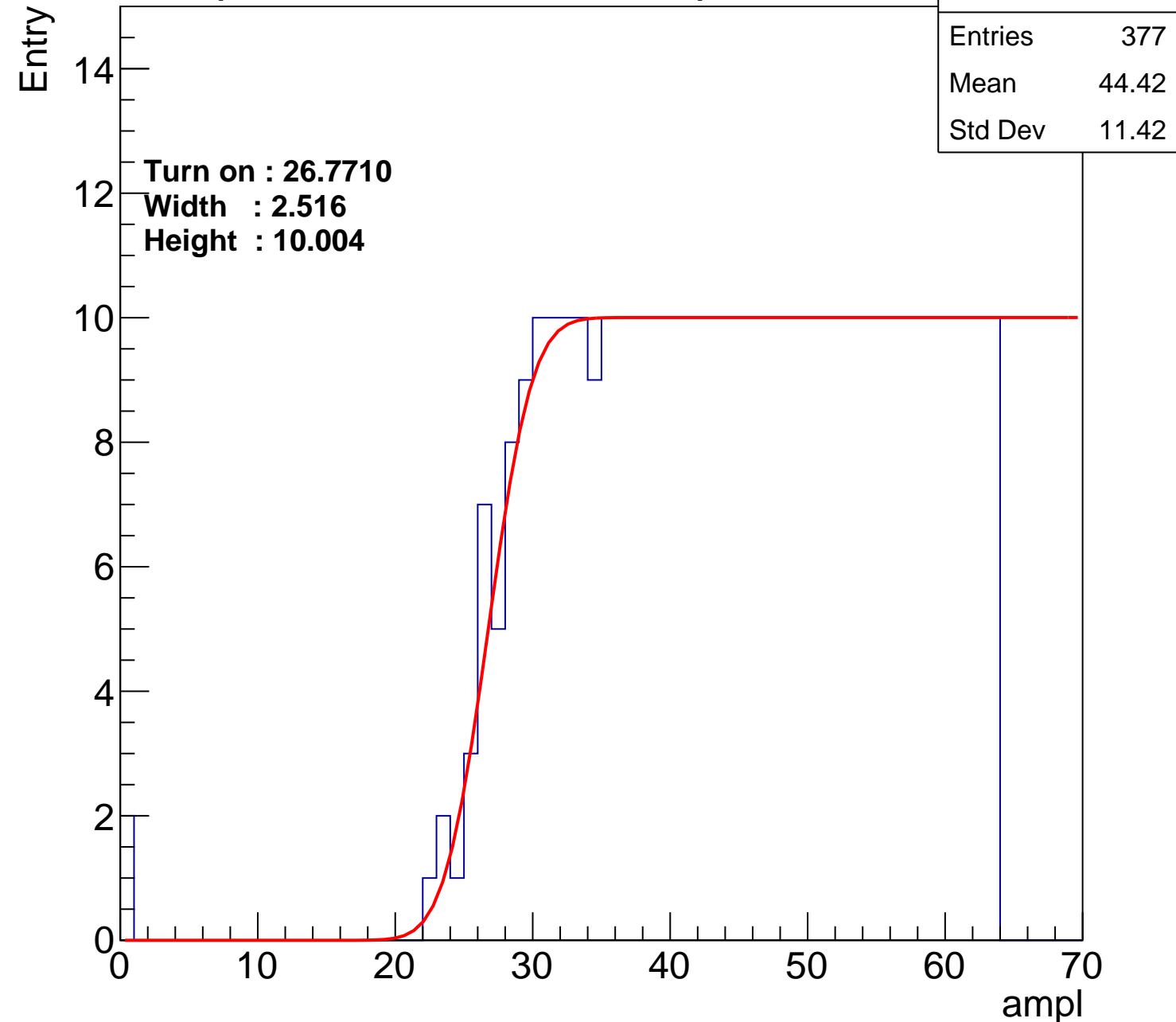
Width : 2.516

Height : 10.004

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch43

calib\_packv5\_042523\_0143.root, FC#9, port A1

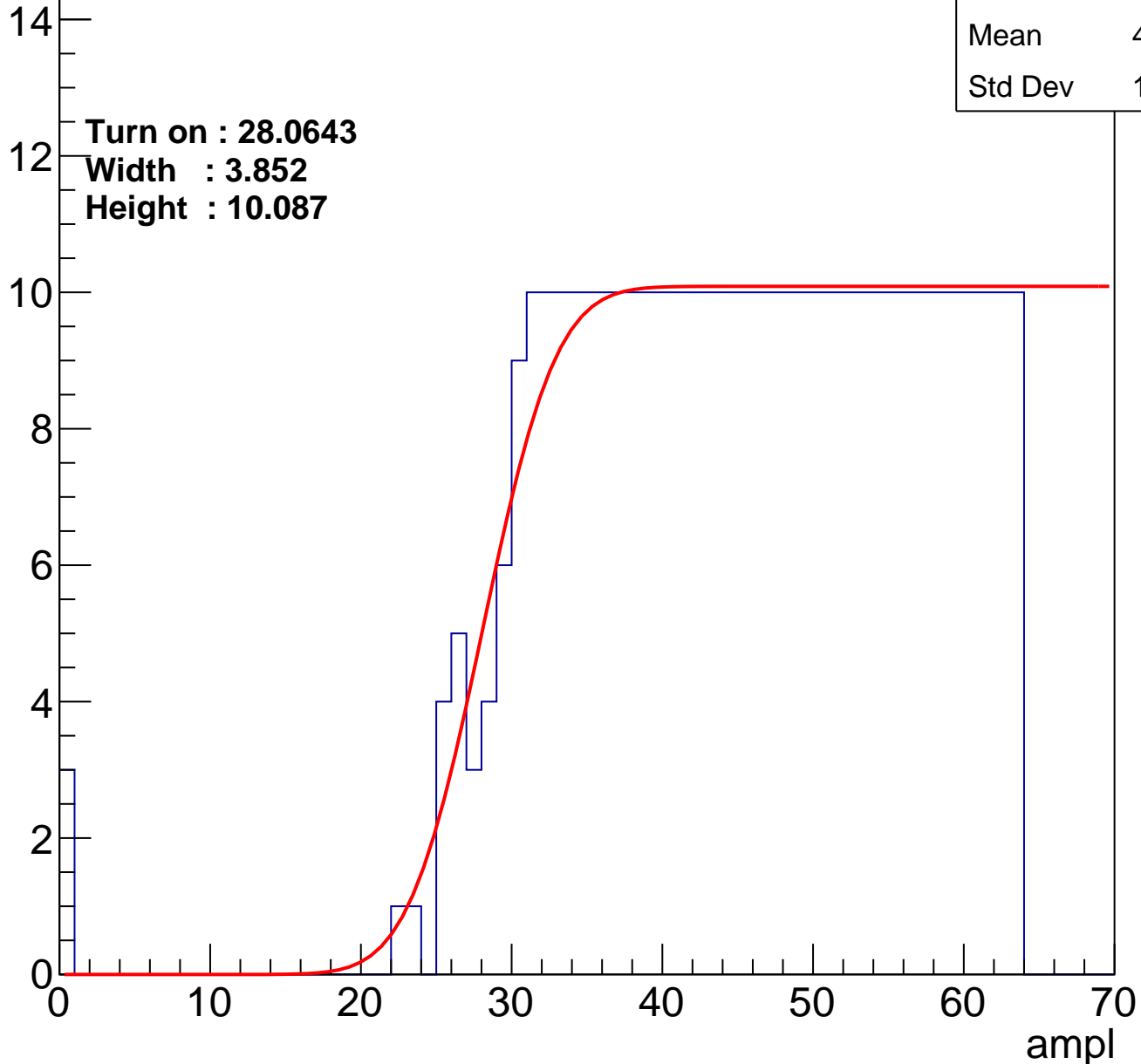
Entries	366
Mean	44.87
Std Dev	11.38

**Turn on : 28.0643**

**Width : 3.852**

**Height : 10.087**

Entry



# B0L001S, U24-ch44

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	361
Mean	45.25
Std Dev	11.19

Turn on : 28.5047

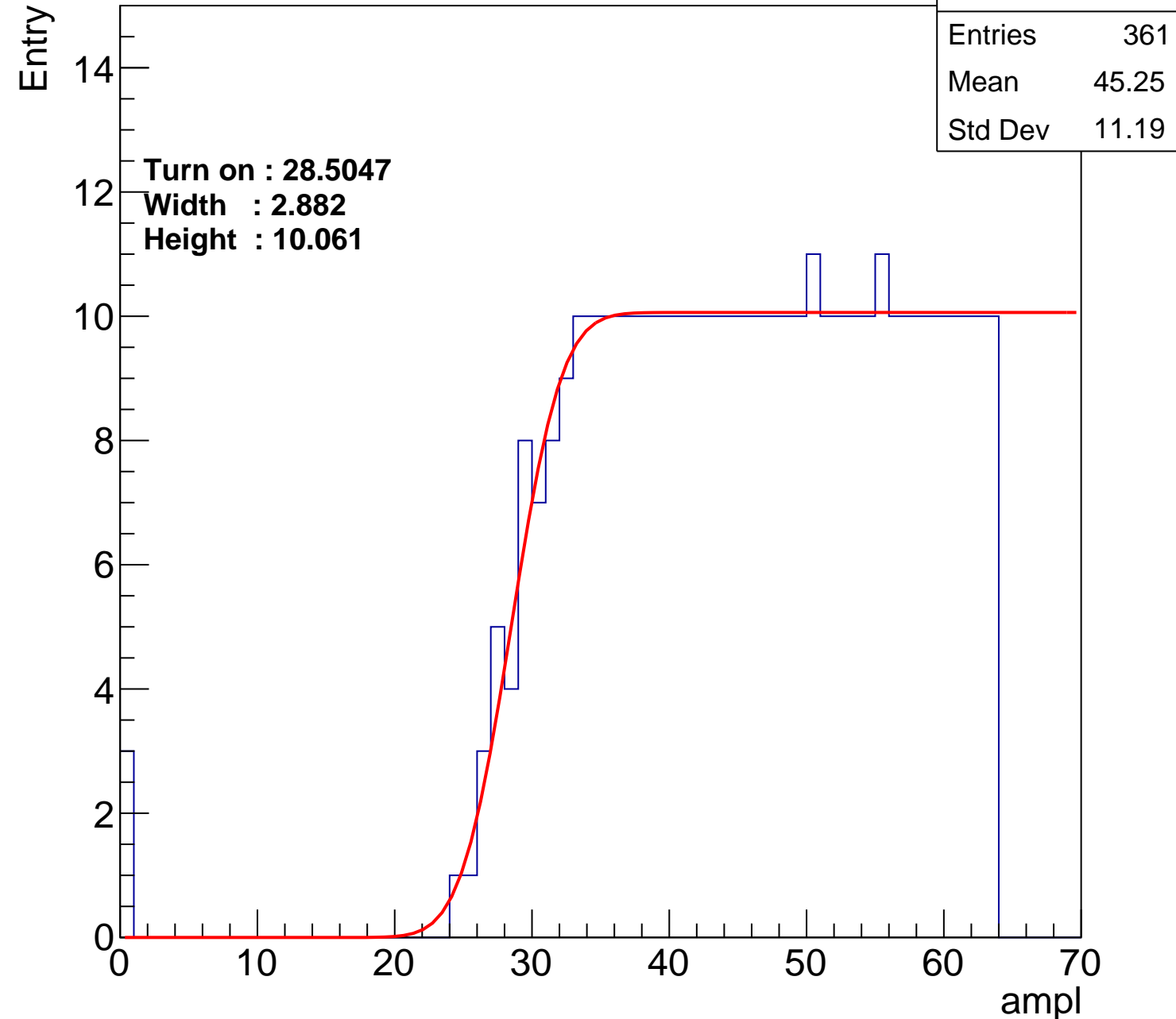
Width : 2.882

Height : 10.061

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch45

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	376
Mean	44.3
Std Dev	11.81

Turn on : 26.8928

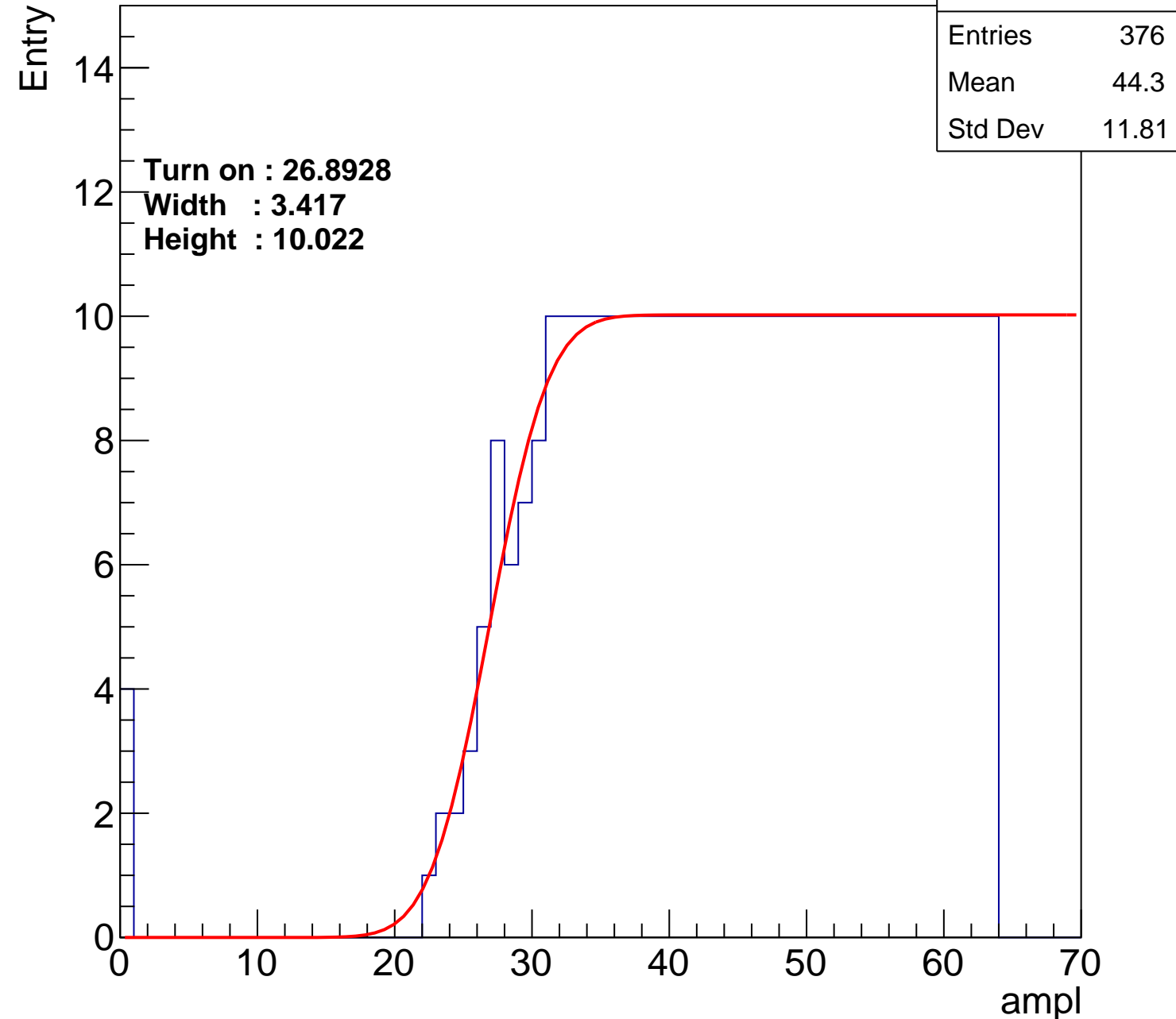
Width : 3.417

Height : 10.022

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch46

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	357
Mean	45.44
Std Dev	10.77

Turn on : 28.5600

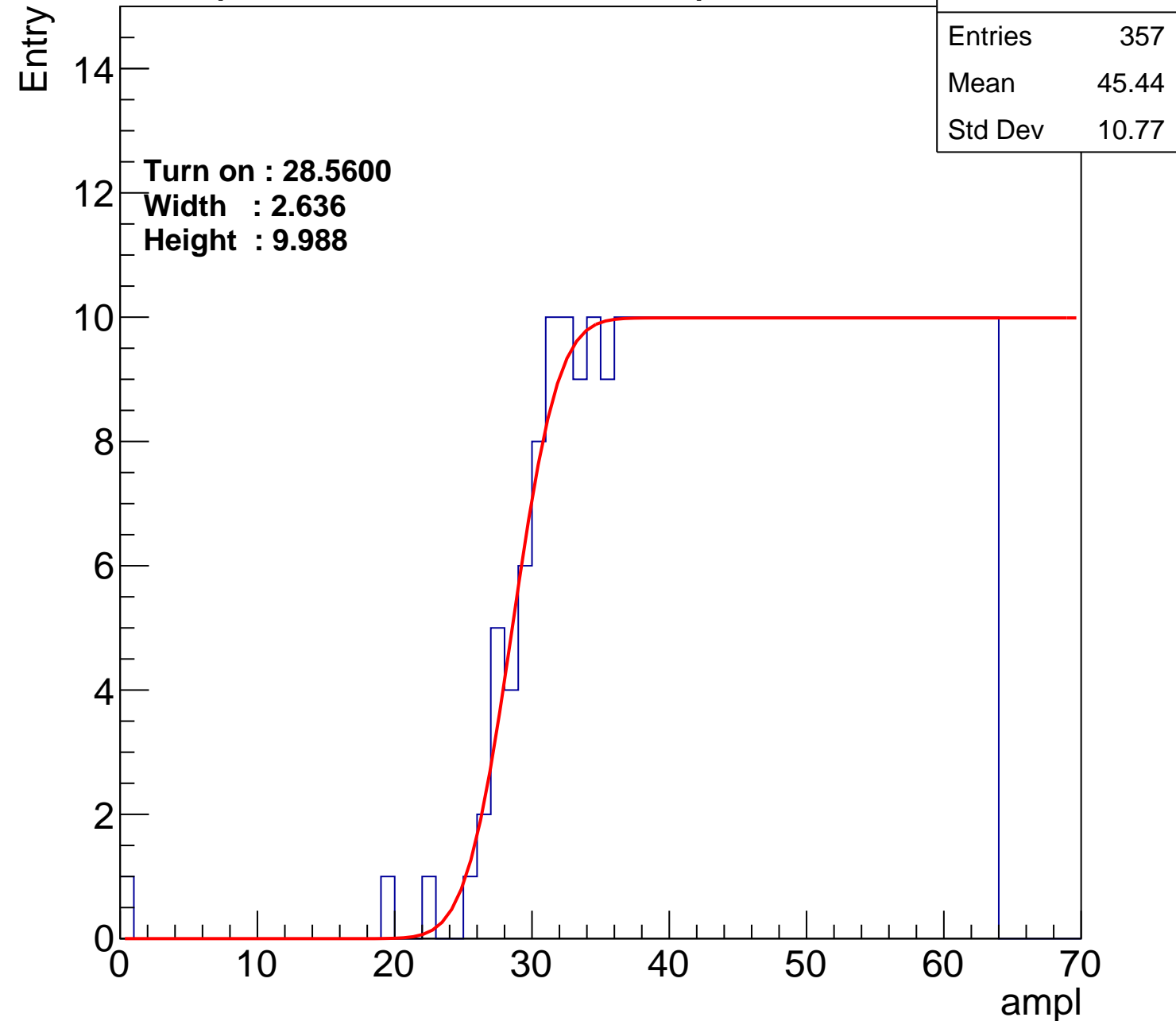
Width : 2.636

Height : 9.988

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U24-ch47

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	347
Mean	45.8
Std Dev	10.92

**Turn on : 29.6704**

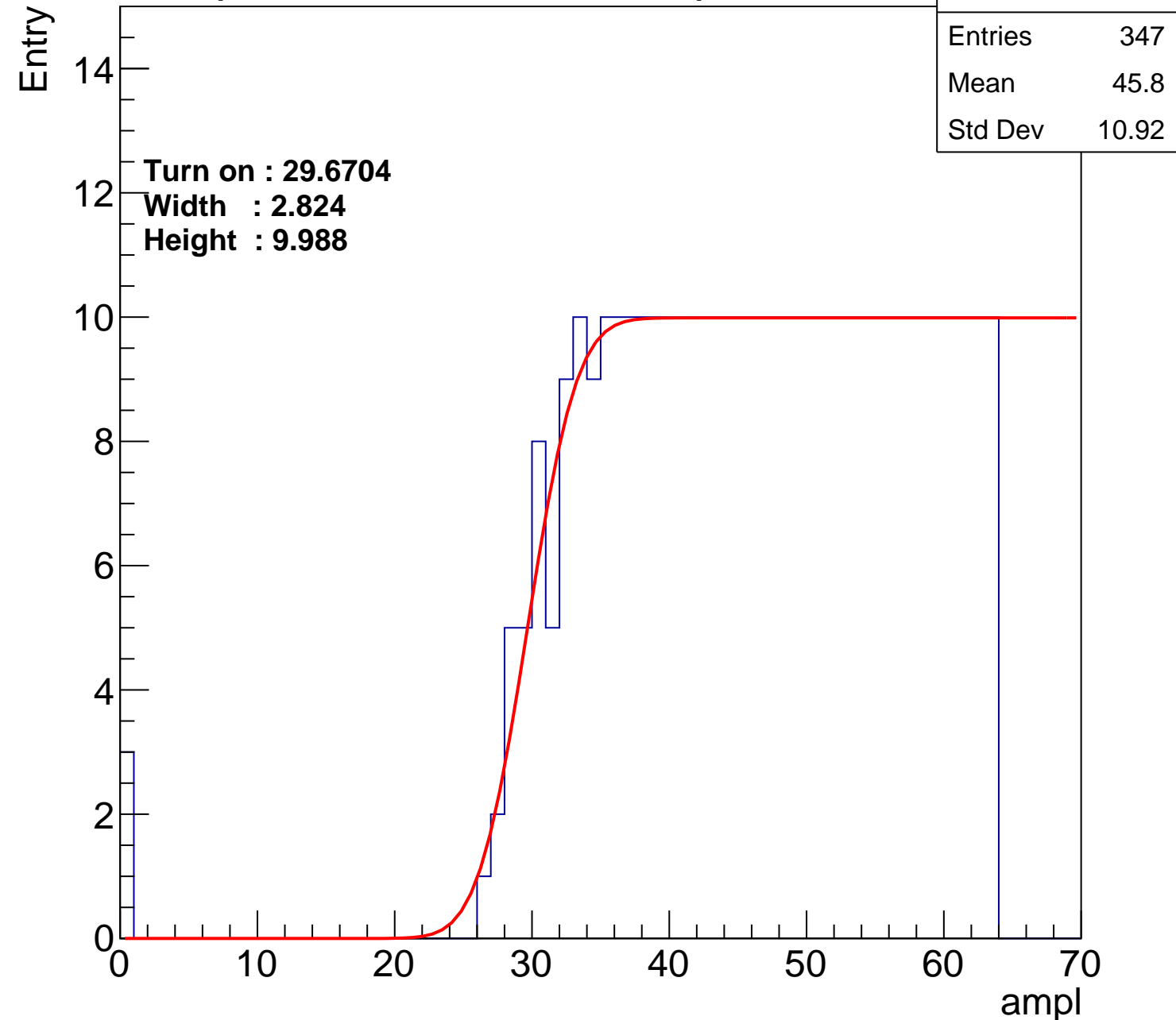
**Width : 2.824**

**Height : 9.988**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch48

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	354
Mean	45.33
Std Dev	11.39

**Turn on : 28.9169**

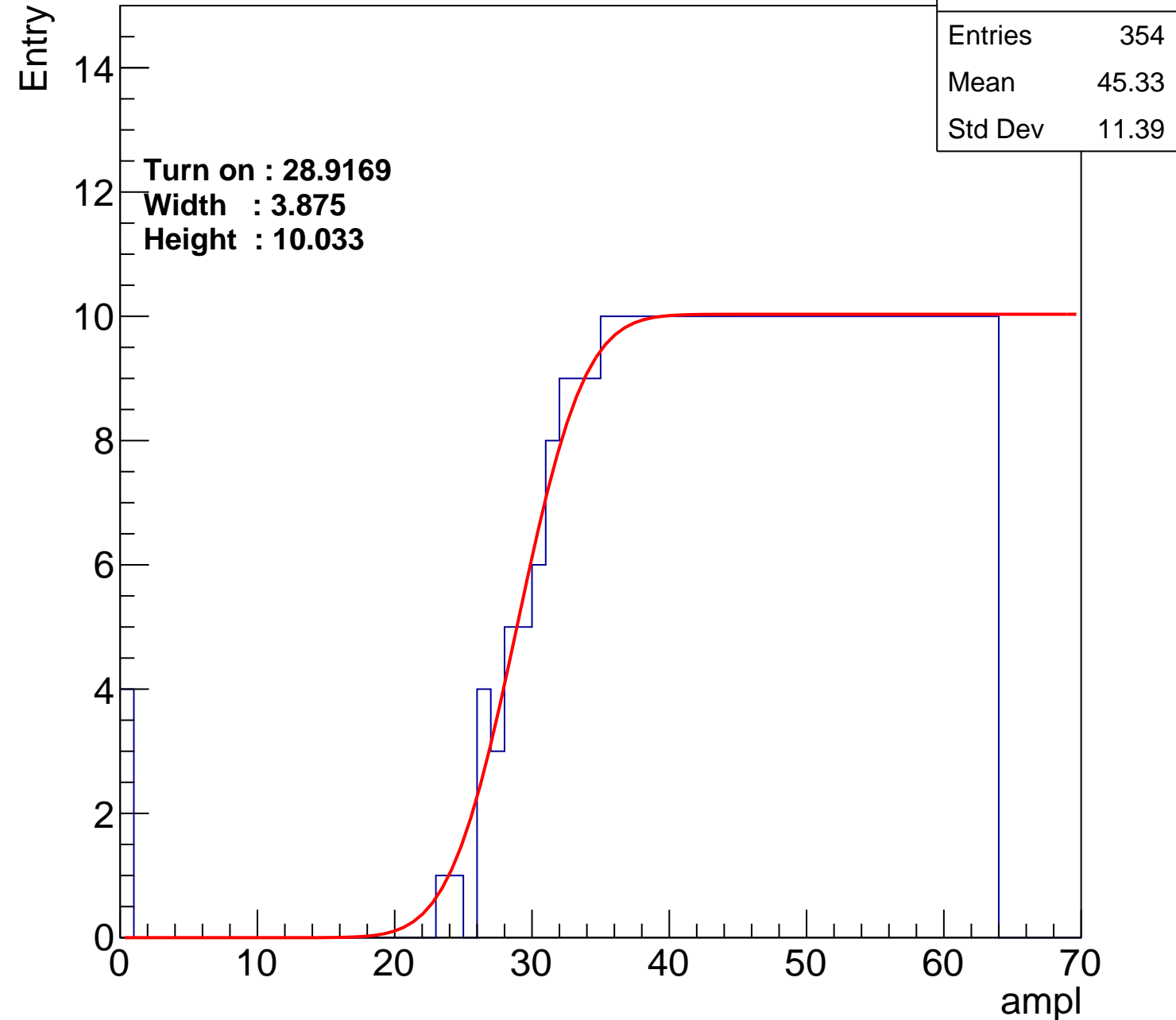
**Width : 3.875**

**Height : 10.033**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch49

calib\_packv5\_042523\_0143.root, FC#9, port A1

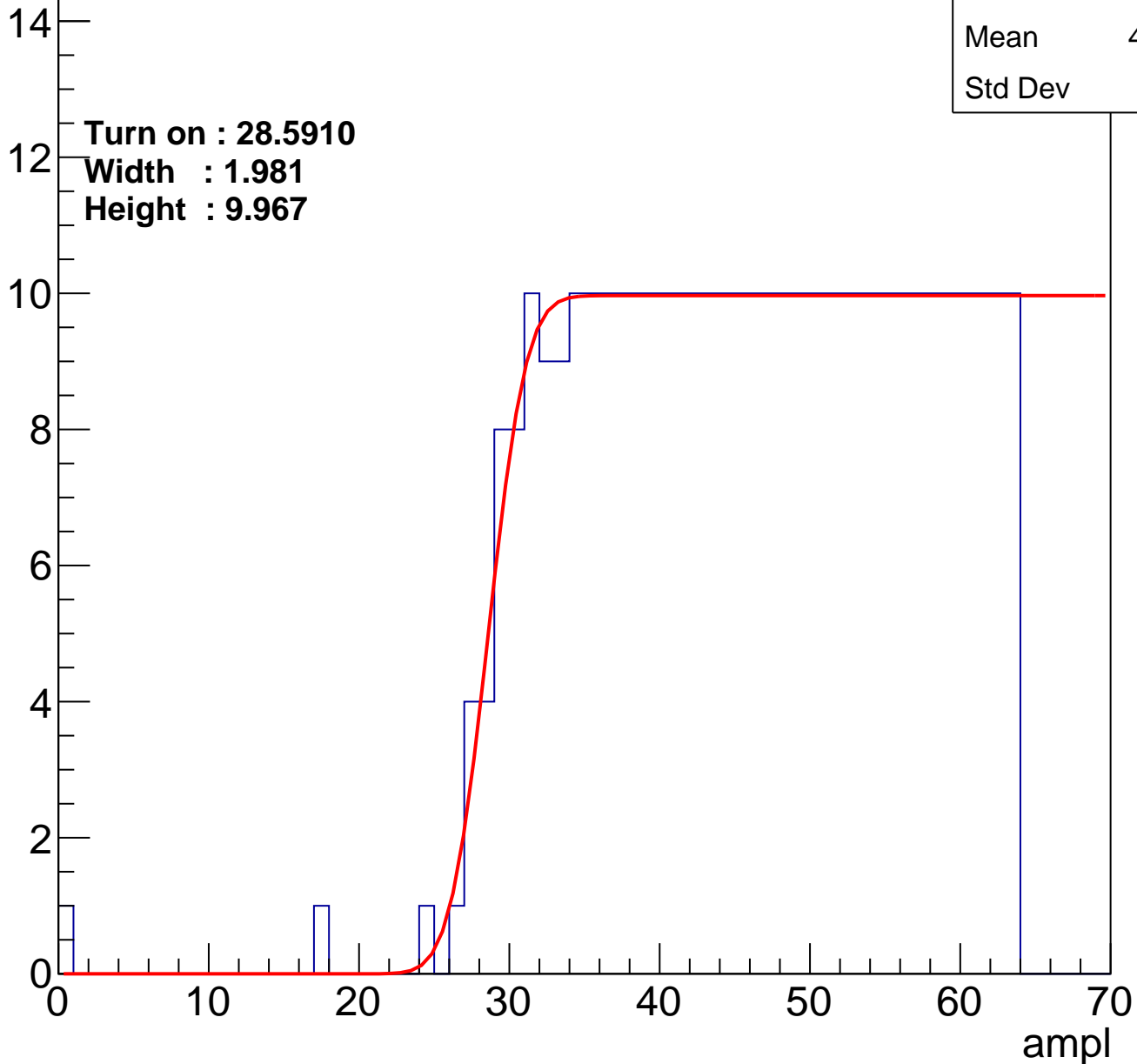
Entries	356
Mean	45.52
Std Dev	10.7

Turn on : 28.5910

Width : 1.981

Height : 9.967

Entry



# B0L001S, U24-ch50

calib\_packv5\_042523\_0143.root, FC#9, port A1

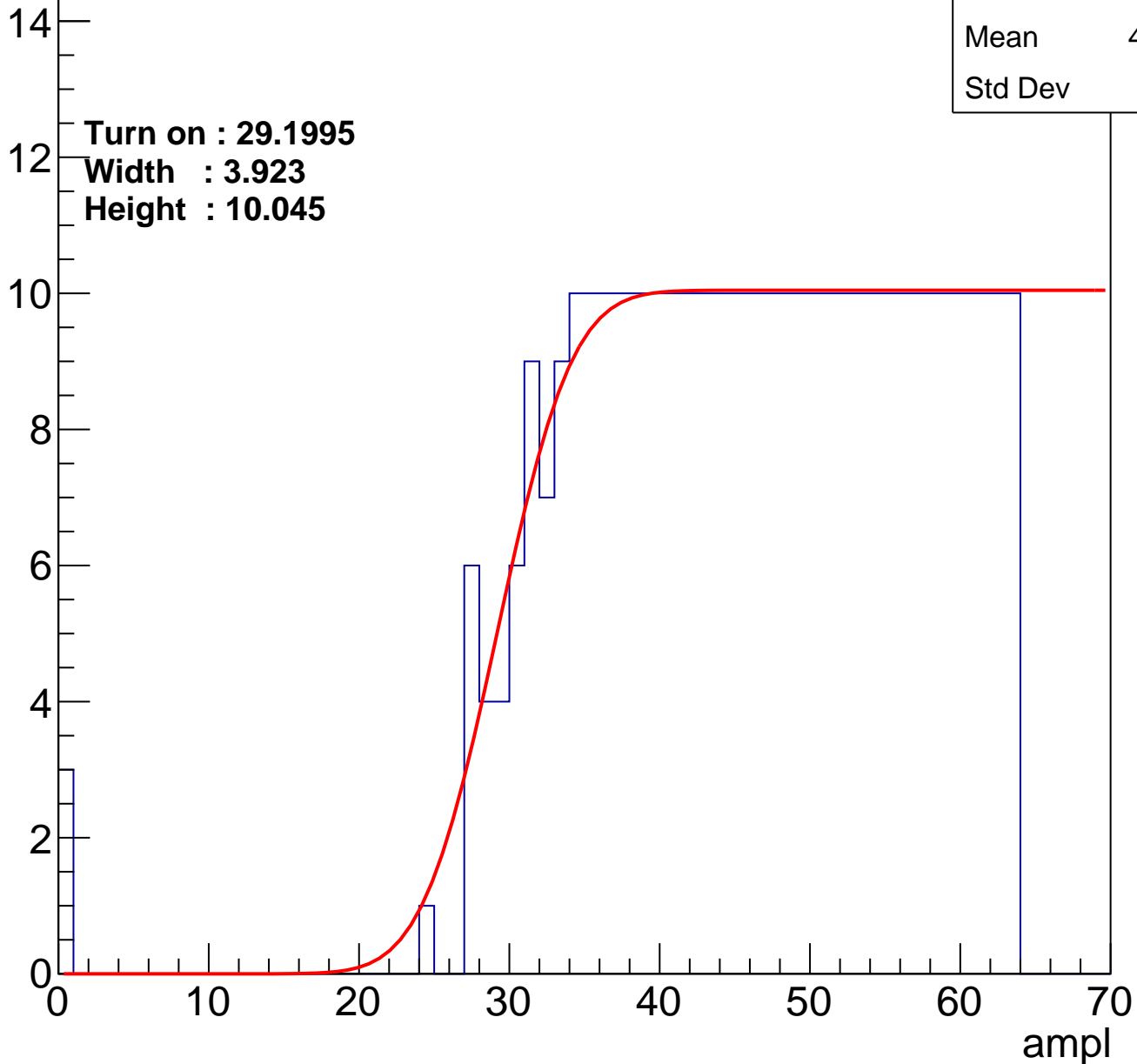
Entries	349
Mean	45.68
Std Dev	11

Turn on : 29.1995

Width : 3.923

Height : 10.045

Entry



# B0L001S, U24-ch51

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	367
Mean	44.67
Std Dev	11.81

Turn on : 27.8256

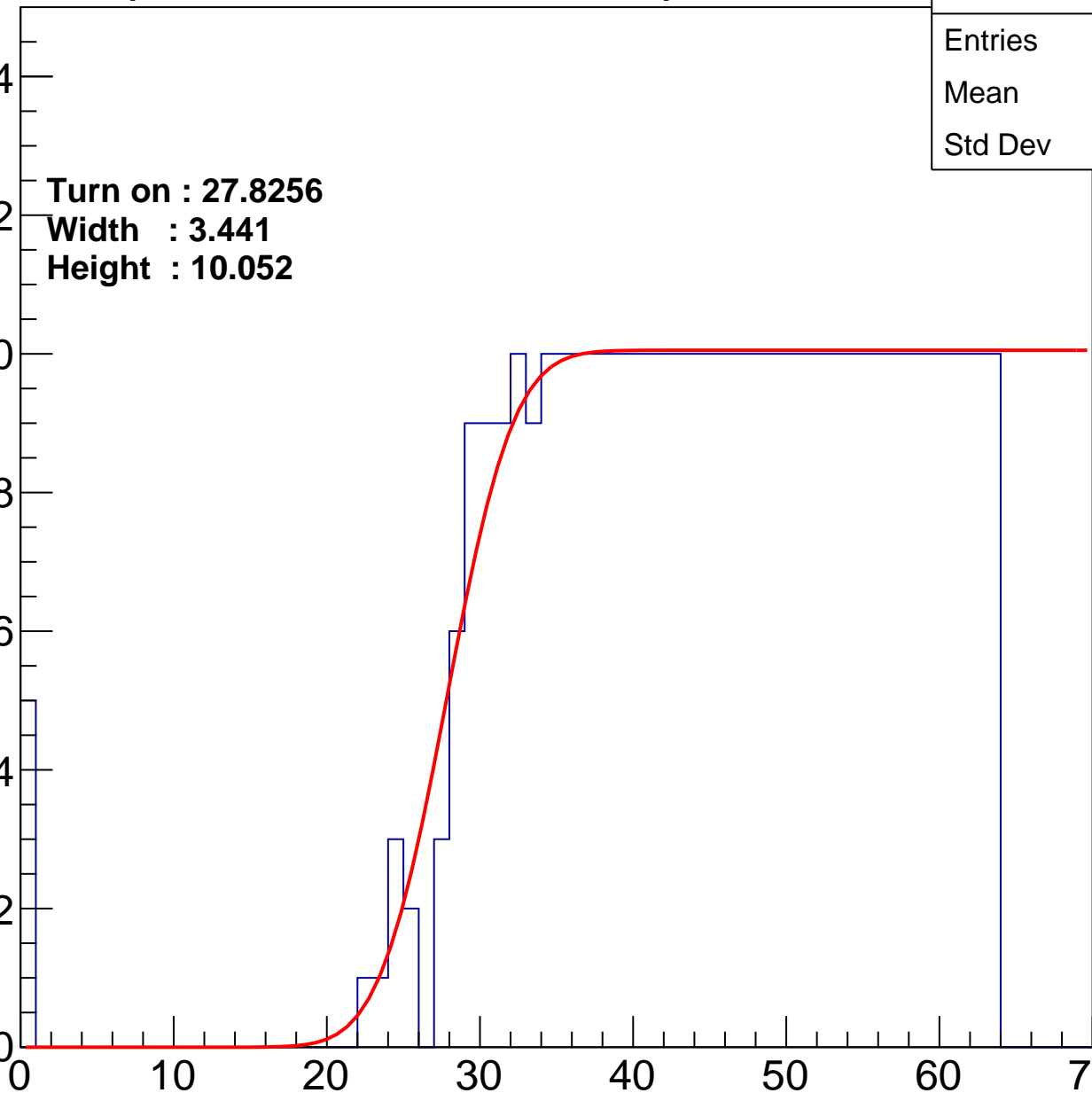
Width : 3.441

Height : 10.052

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch52

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	356
Mean	45.33
Std Dev	11.18

**Turn on : 28.8183**

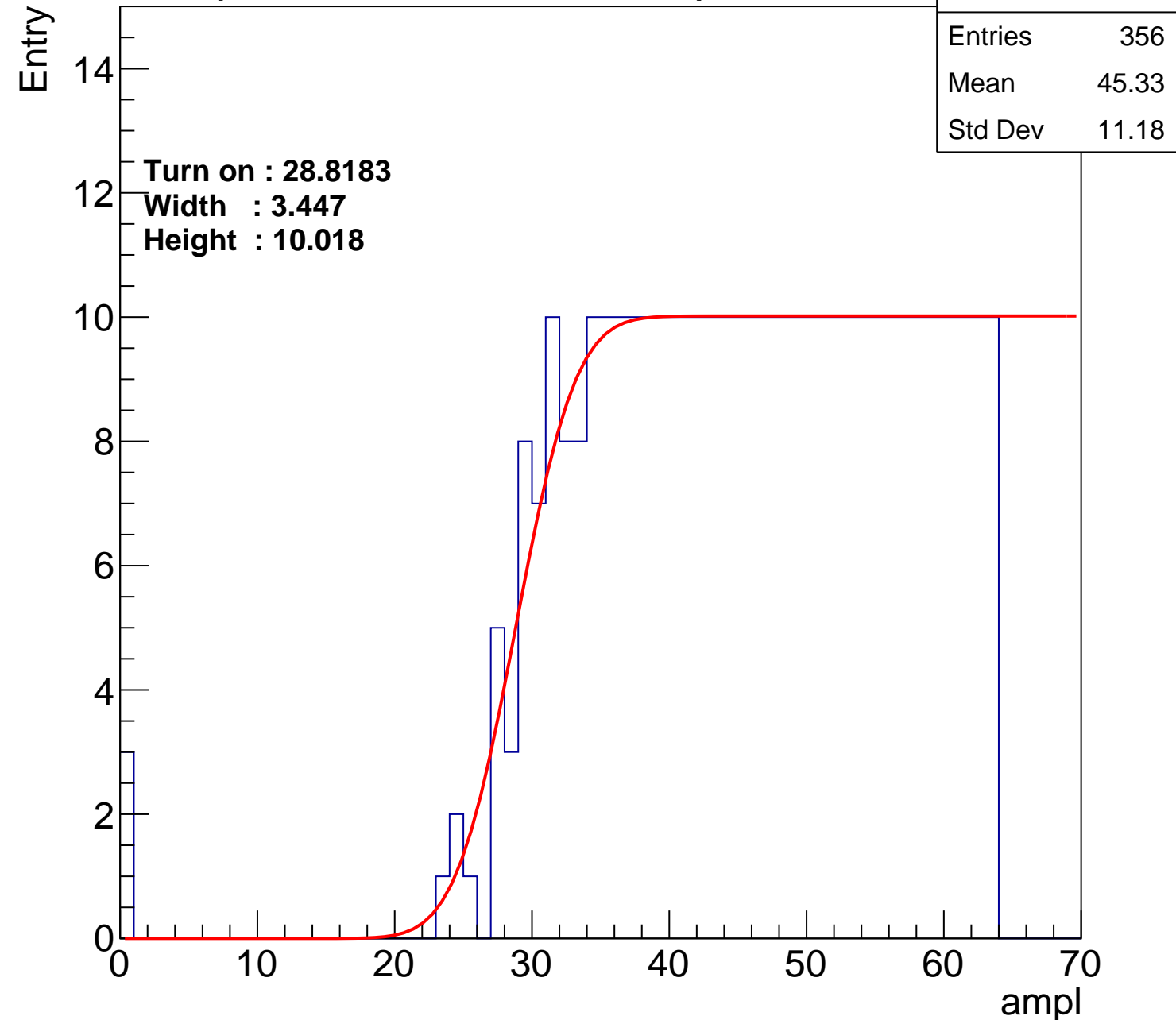
**Width : 3.447**

**Height : 10.018**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch53

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	363
Mean	44.9
Std Dev	11.66

**Turn on : 28.3741**

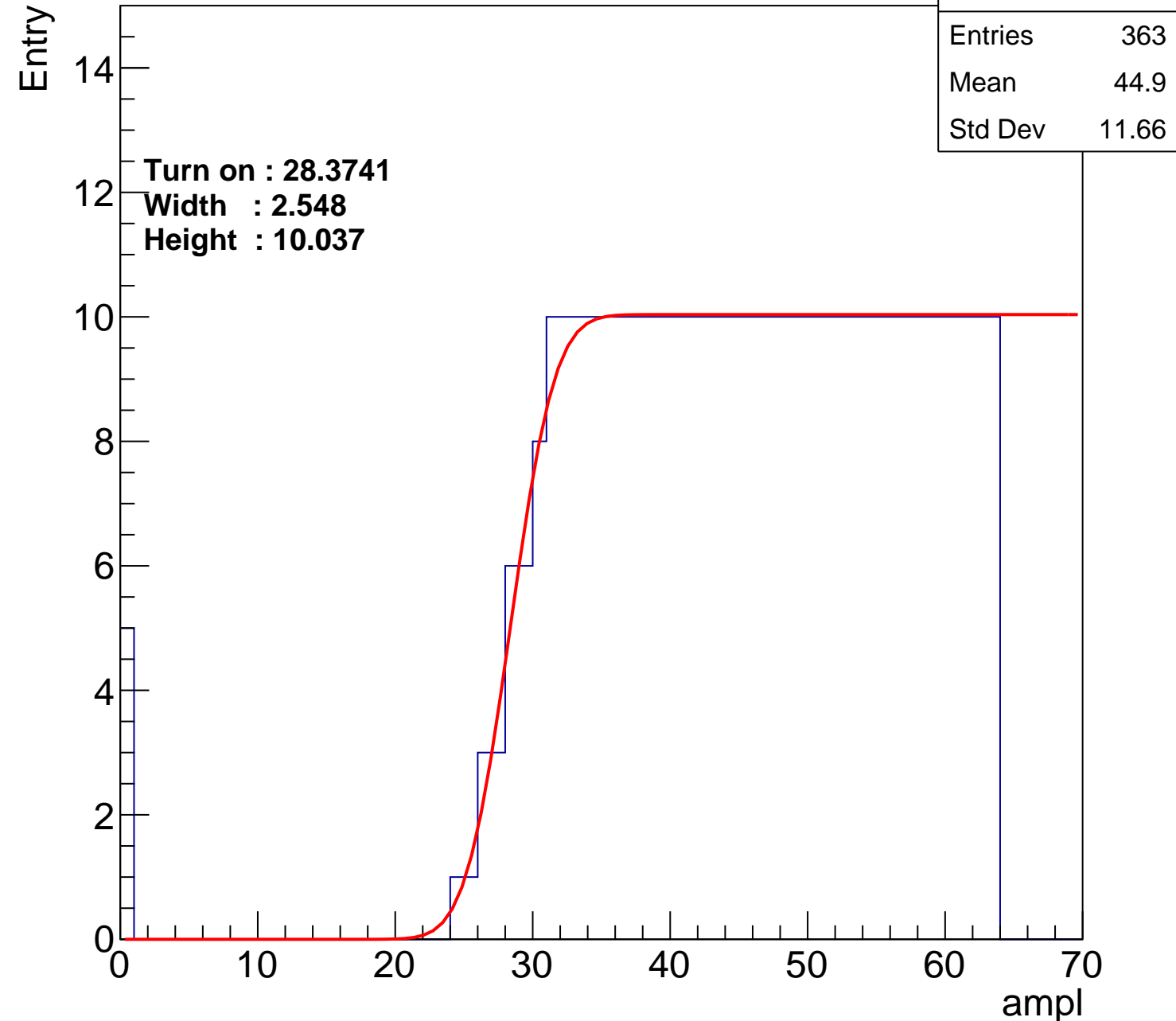
**Width : 2.548**

**Height : 10.037**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch54

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	368
Mean	44.79
Std Dev	11.39

Turn on : 27.1956

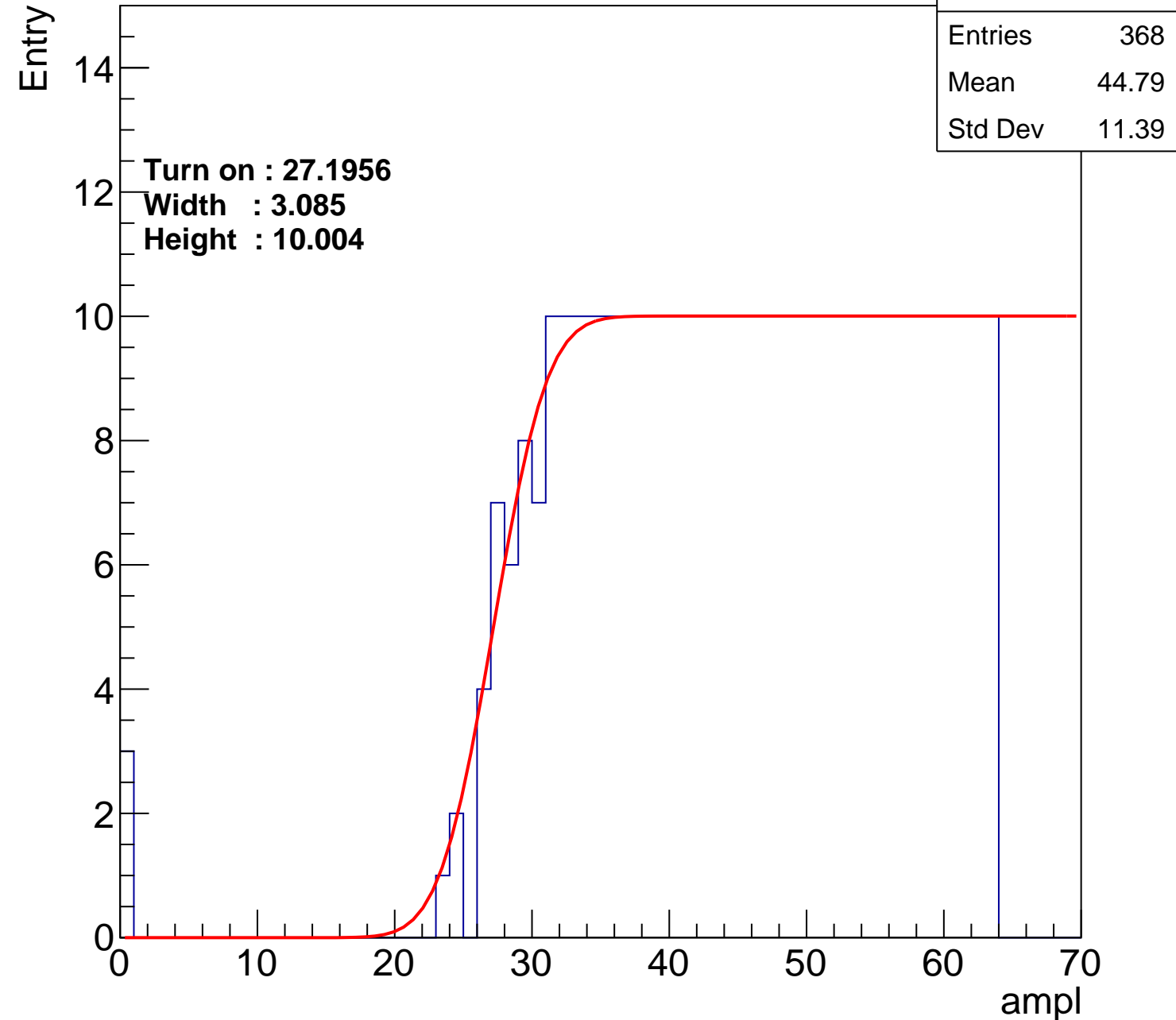
Width : 3.085

Height : 10.004

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U24-ch55

calib\_packv5\_042523\_0143.root, FC#9, port A1

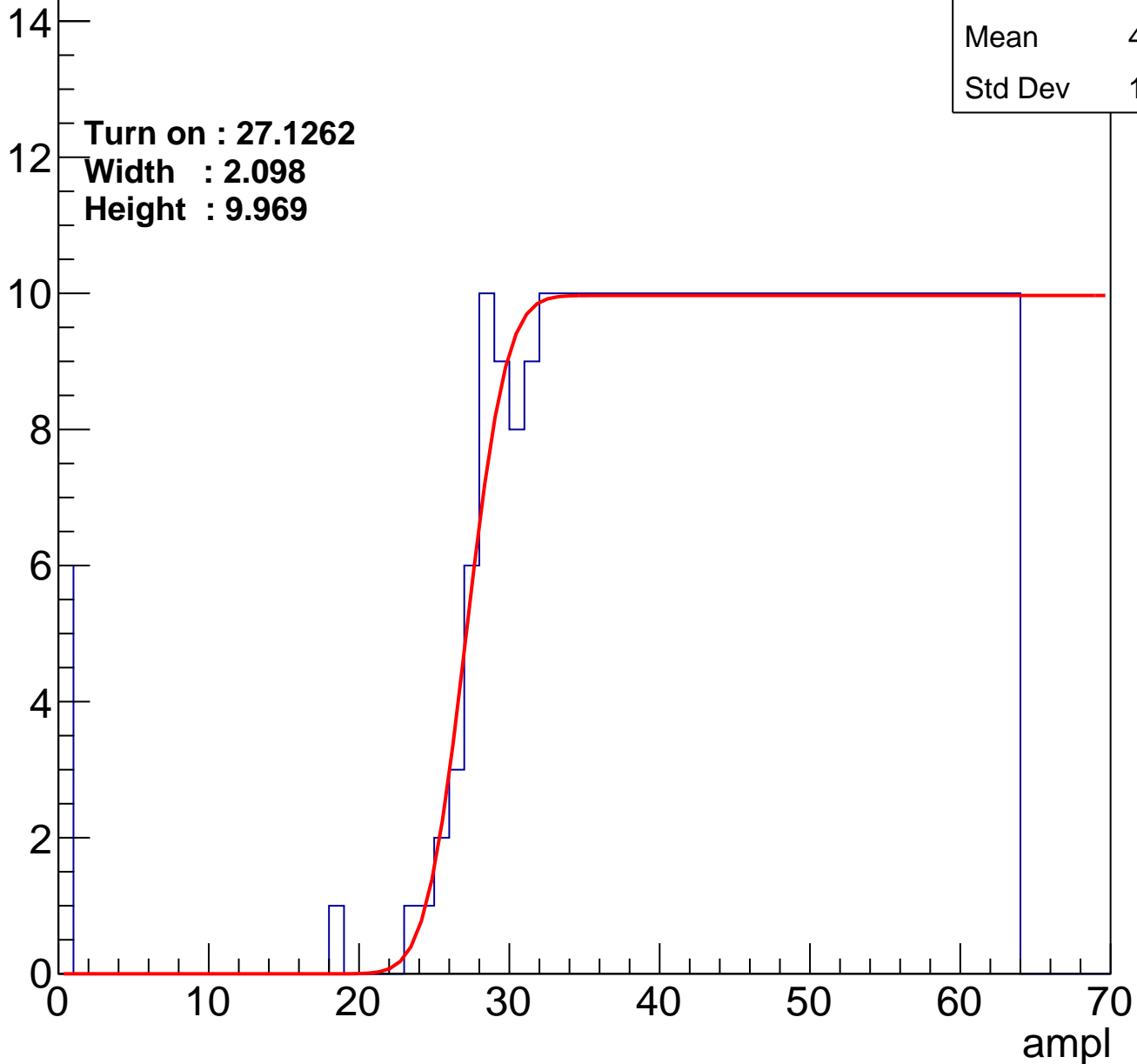
Entries	376
Mean	44.19
Std Dev	12.14

Turn on : 27.1262

Width : 2.098

Height : 9.969

Entry



# B0L001S, U24-ch56

calib\_packv5\_042523\_0143.root, FC#9, port A1

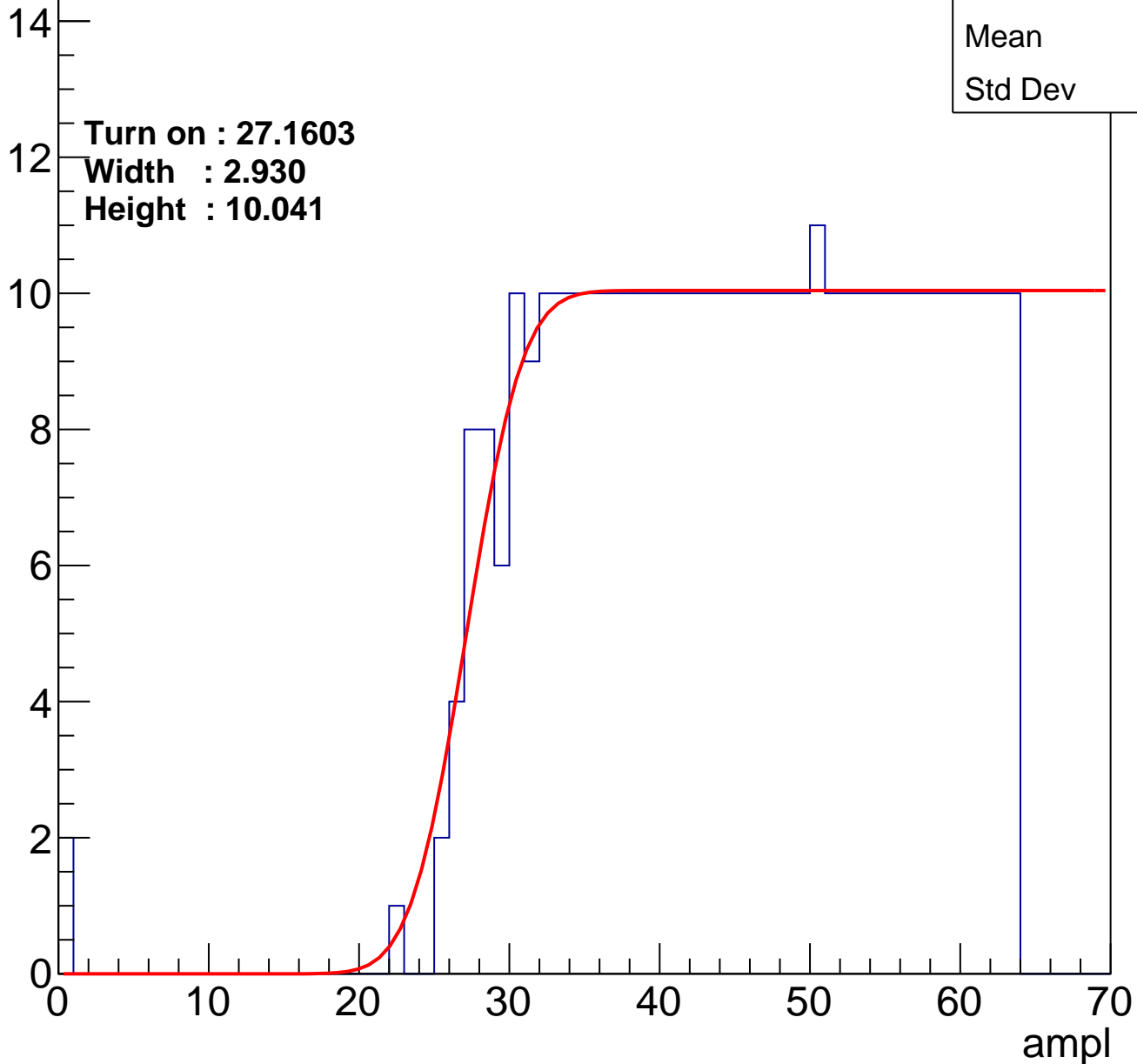
Entries	371
Mean	44.8
Std Dev	11.2

Turn on : 27.1603

Width : 2.930

Height : 10.041

Entry



# B0L001S, U24-ch57

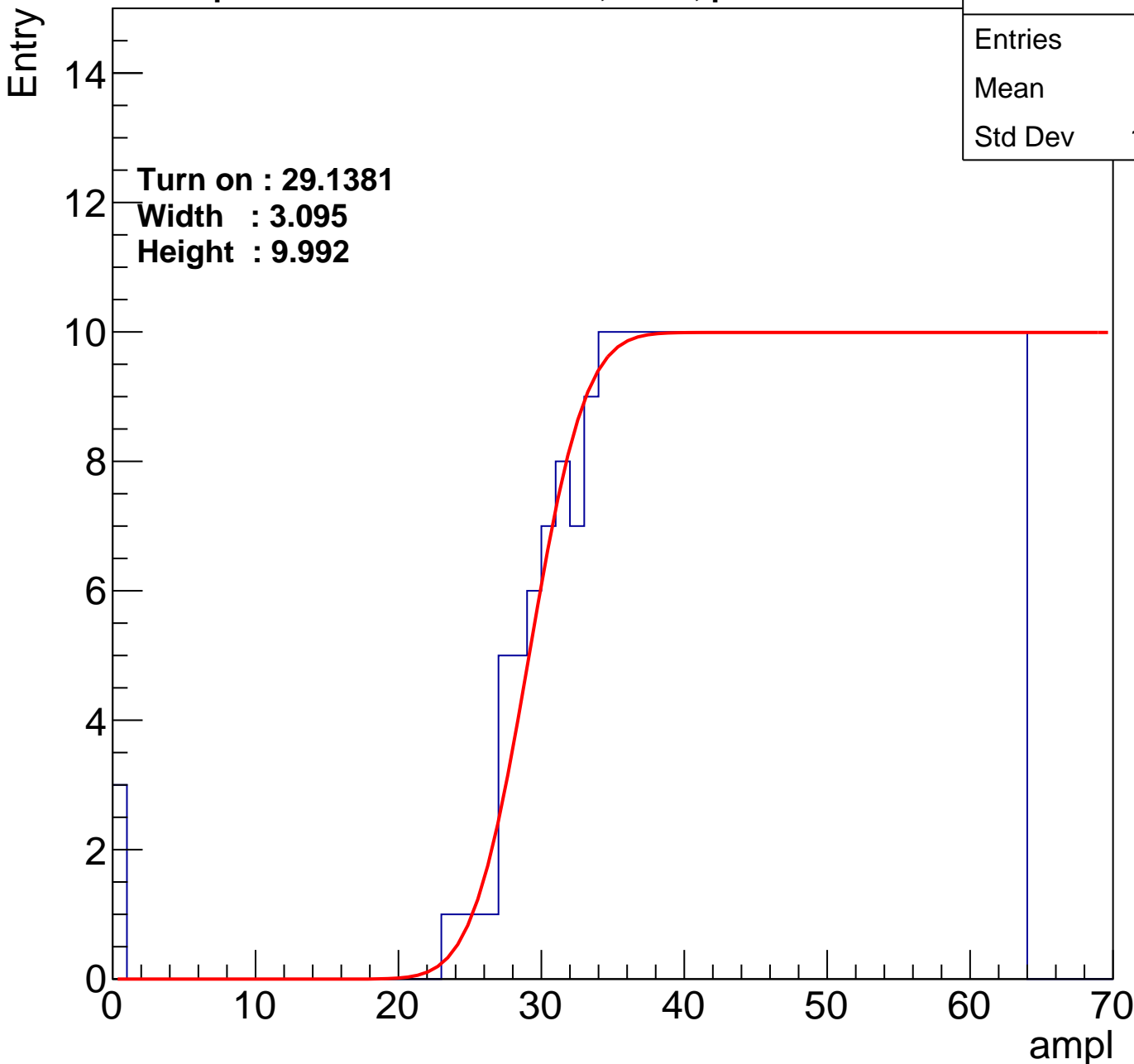
calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	354
Mean	45.41
Std Dev	11.16

Turn on : 29.1381

Width : 3.095

Height : 9.992



**calib\_packv5\_042523\_0143.root, FC#9, port A1**

Entries	362
Mean	45.13
Std Dev	11.08

Std Dev	11.08
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**Height : 9.998**

0

60

0

# B0L001S, U24-ch59

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	353
Mean	45.12
Std Dev	12.12

Turn on : 29.4576

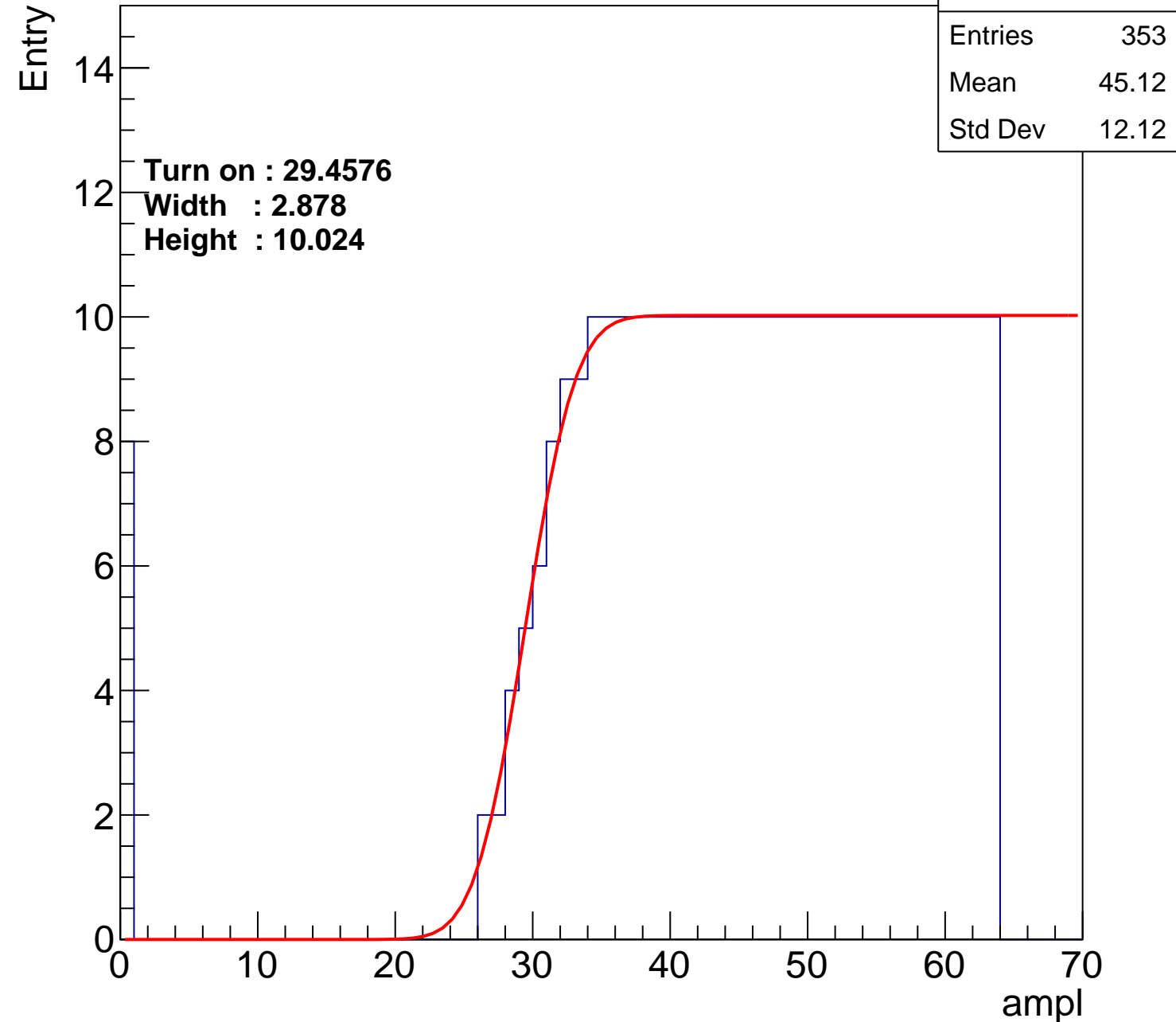
Width : 2.878

Height : 10.024

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch60

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	365
Mean	44.99
Std Dev	11.16

**Turn on : 28.2536**

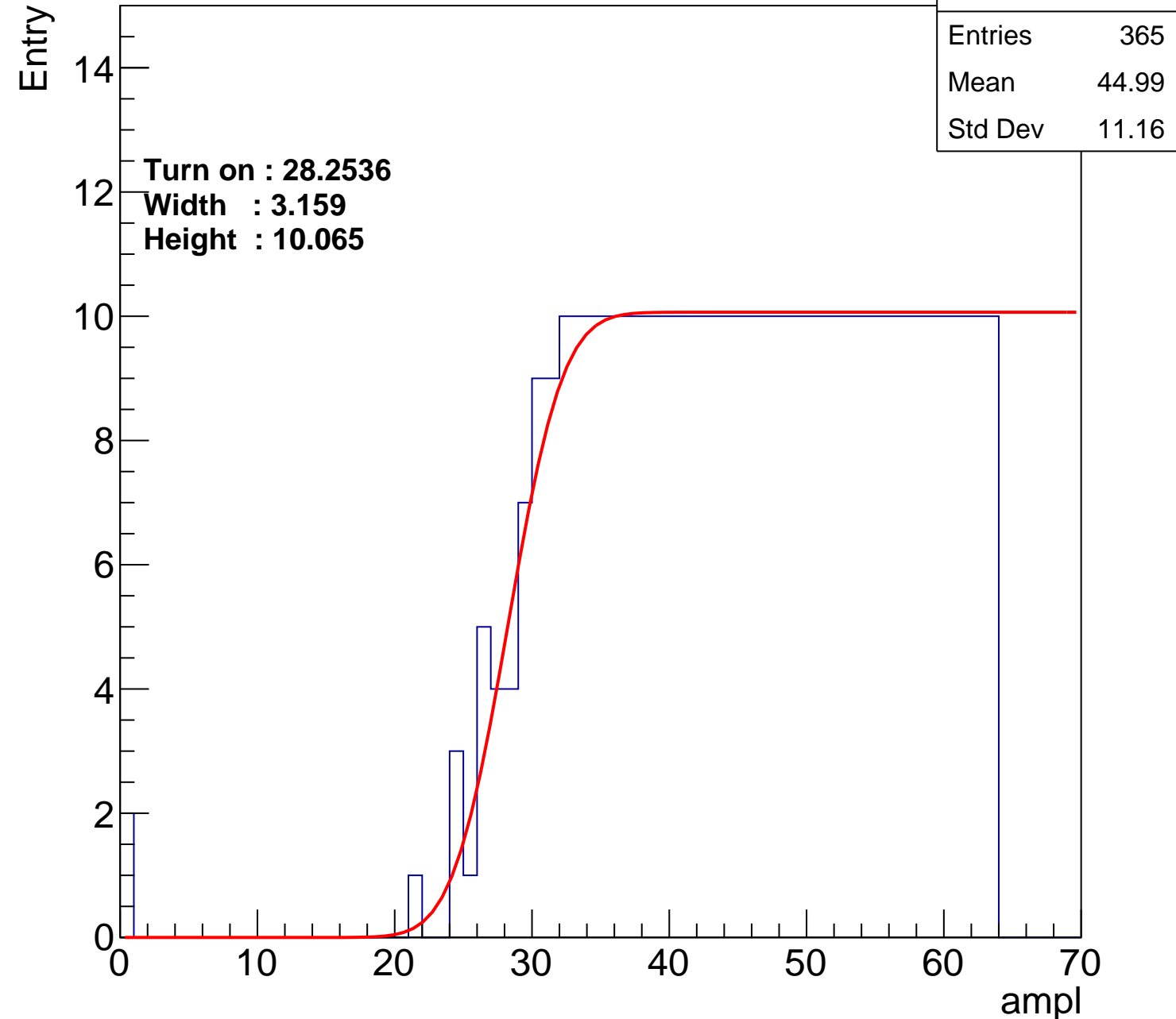
**Width : 3.159**

**Height : 10.065**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch61

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	352
Mean	45.54
Std Dev	11.07

Turn on : 29.3134

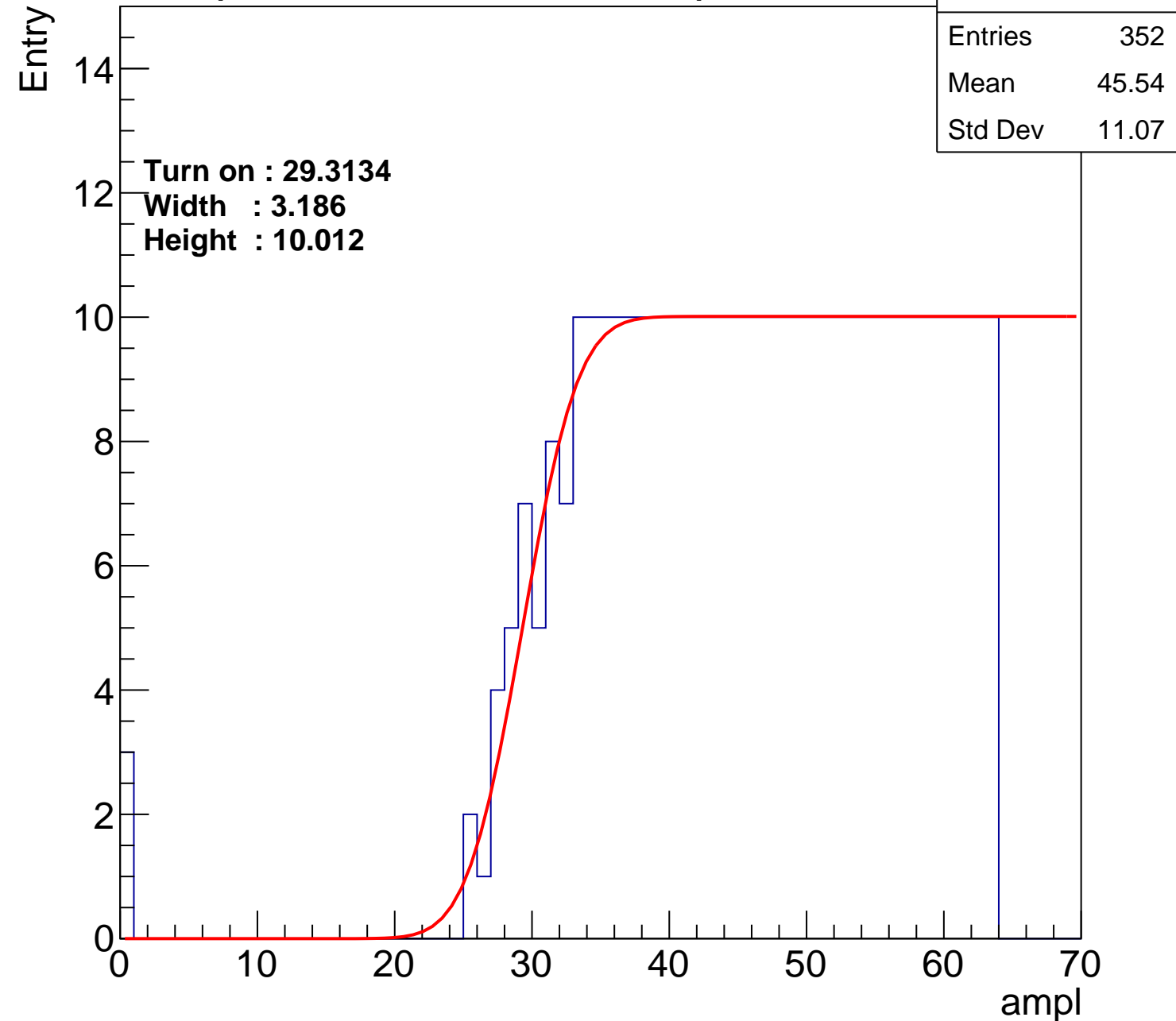
Width : 3.186

Height : 10.012

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch62

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	384
Mean	44.06
Std Dev	11.63

**Turn on : 25.2855**

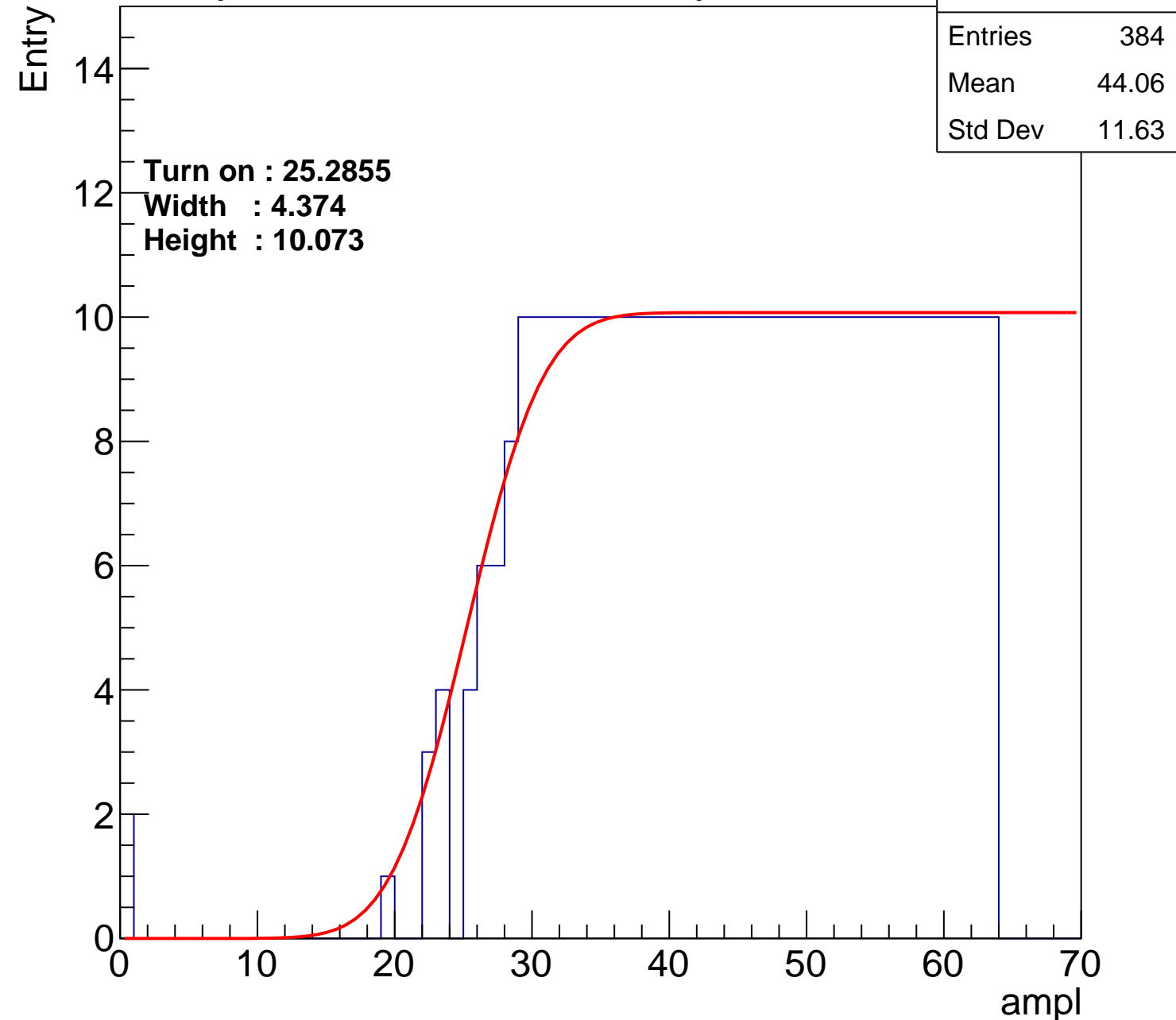
**Width : 4.374**

**Height : 10.073**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U24-ch63

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	359
Mean	45.28
Std Dev	11

Turn on : 28.1549

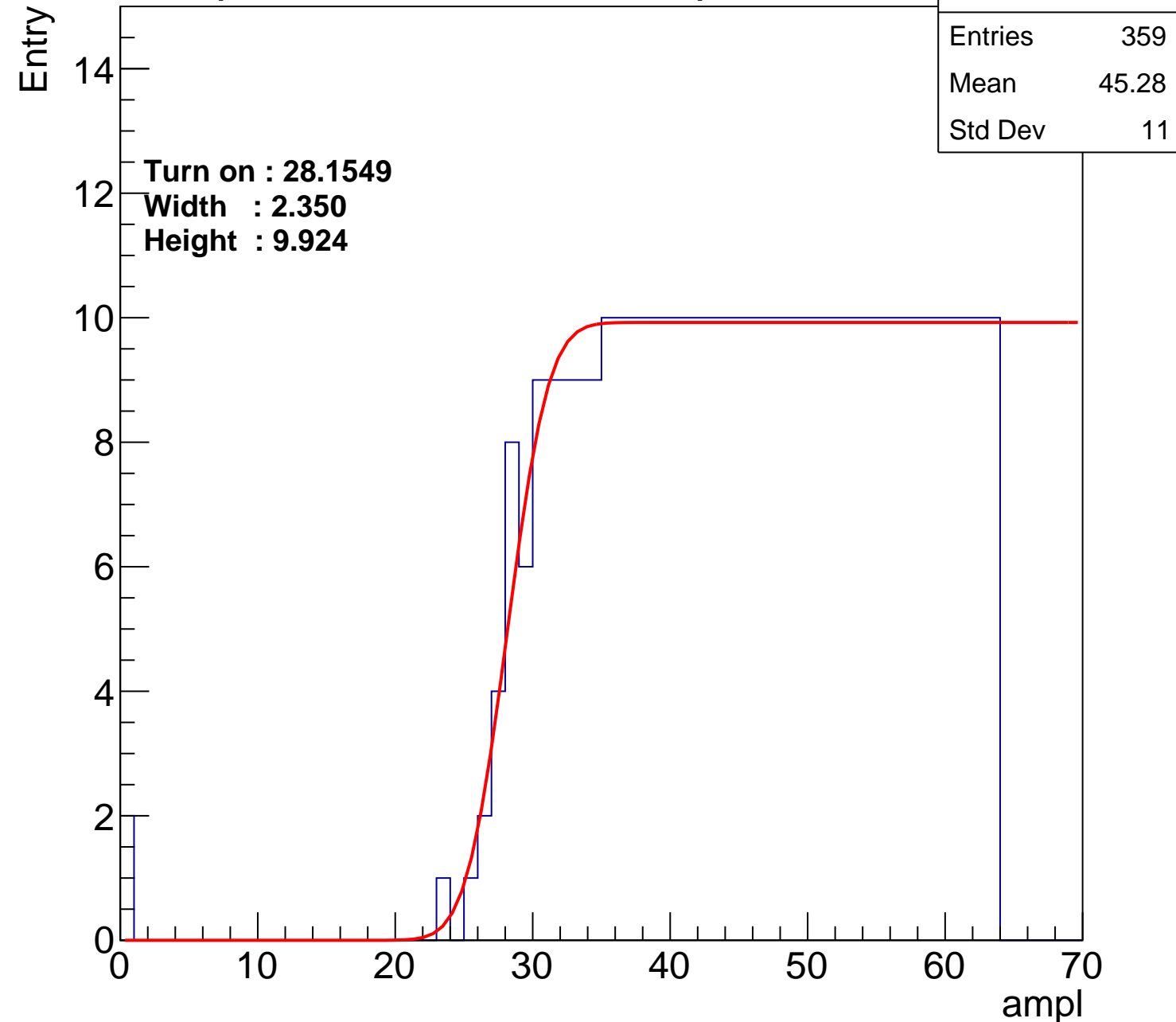
Width : 2.350

Height : 9.924

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch64

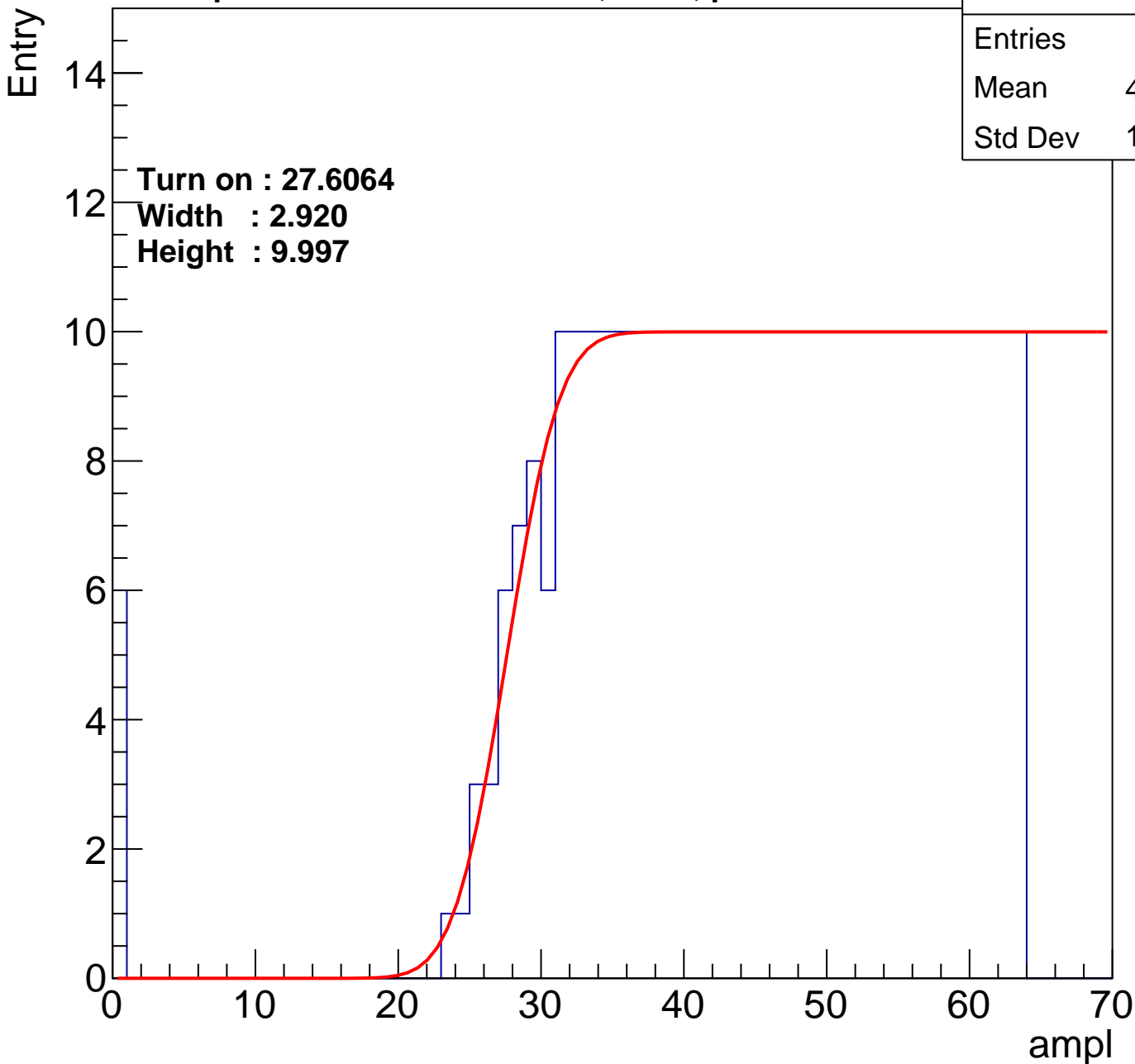
**calib\_packv5\_042523\_0143.root, FC#9, port A1**

Entries	371
Mean	44.42
Std Dev	12.05

**Turn on : 27.6064**

**Width : 2.920**

**Height : 9.997**



# B0L001S, U24-ch65

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	364
Mean	45.22
Std Dev	11.07

Turn on : 28.2057

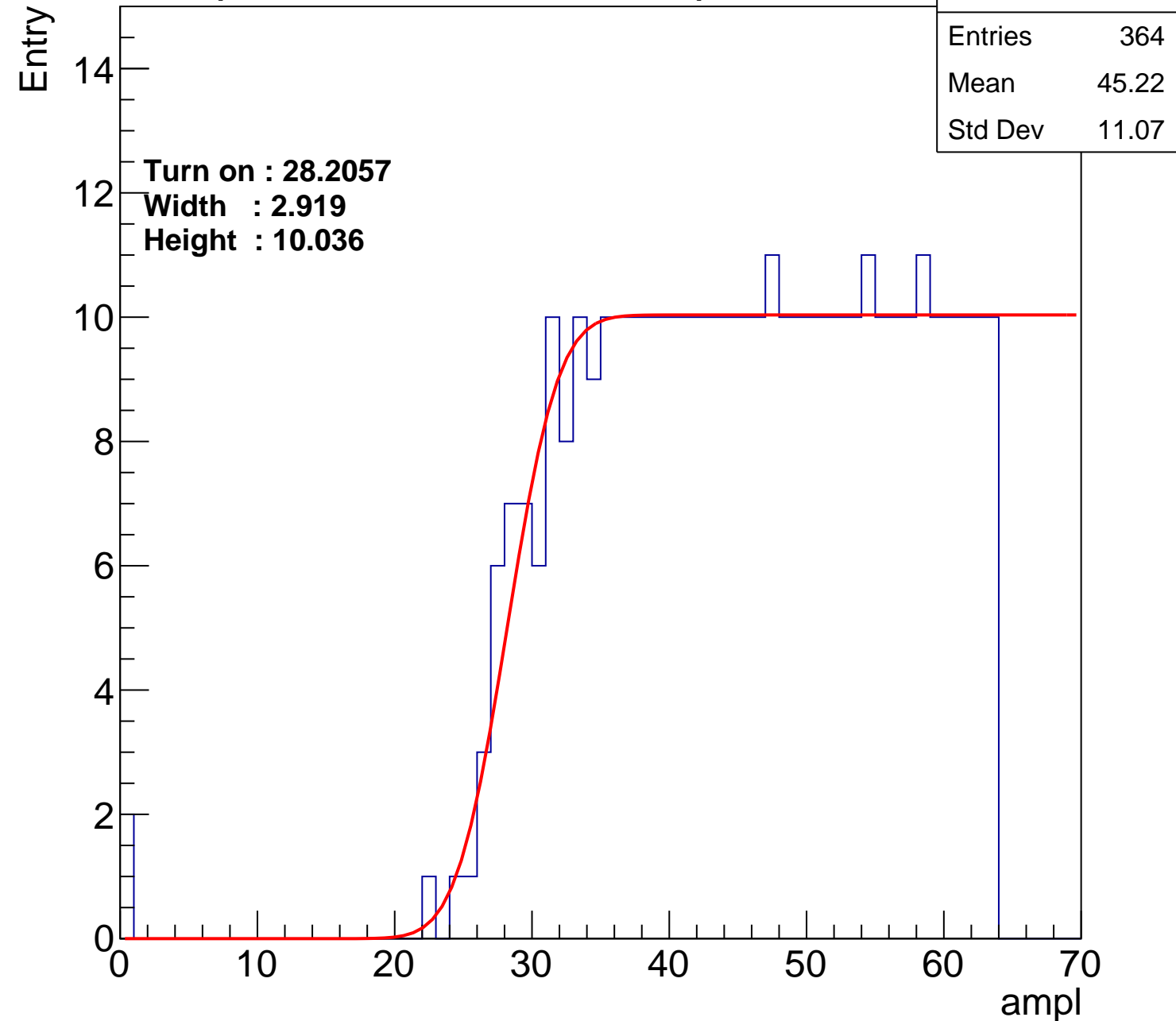
Width : 2.919

Height : 10.036

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch66

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	371
Mean	44.65
Std Dev	11.47

**Turn on : 26.9805**

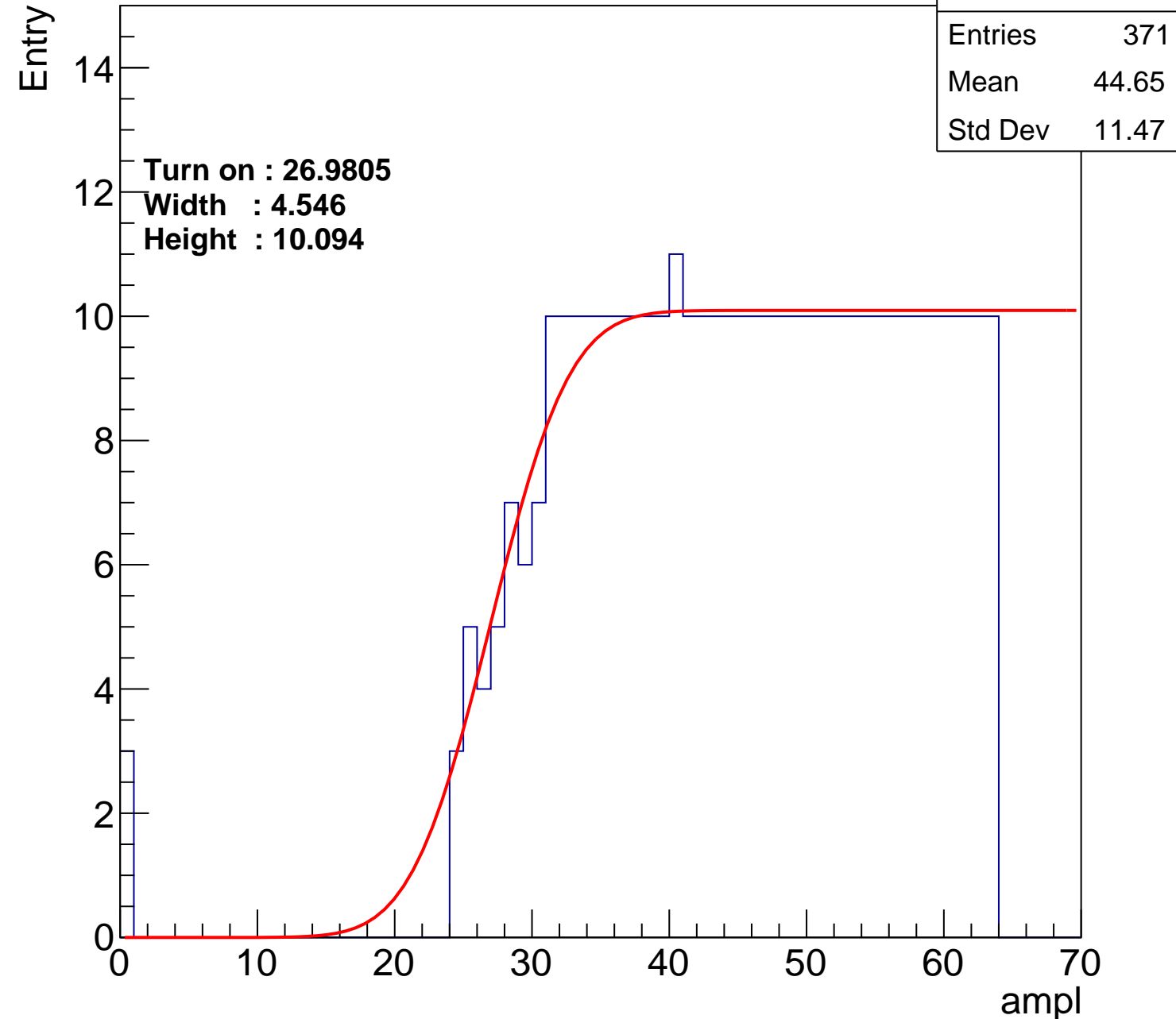
**Width : 4.546**

**Height : 10.094**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch67

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	354
Mean	45.44
Std Dev	11.13

Turn on : 29.2070

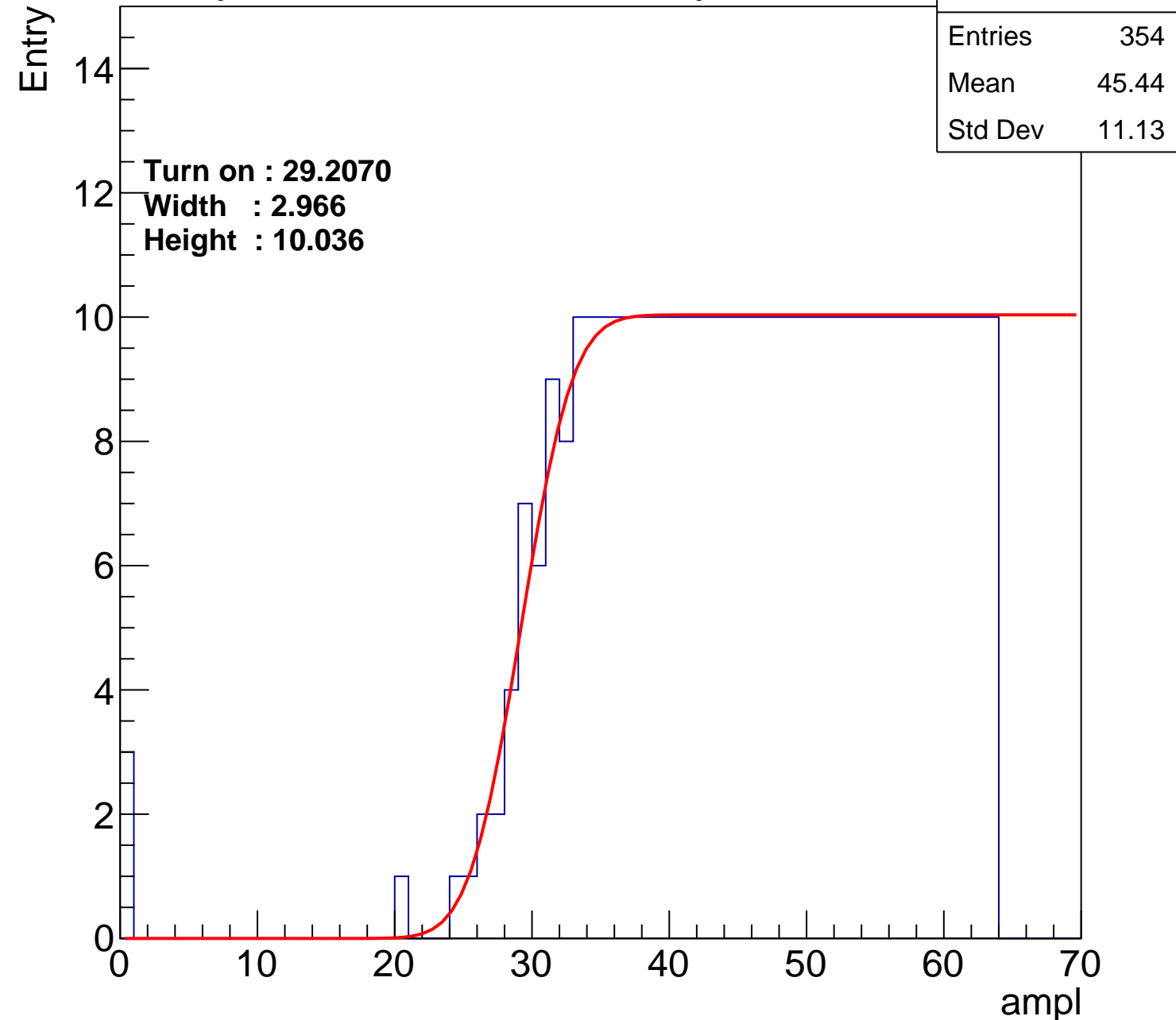
Width : 2.966

Height : 10.036

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch68

calib\_packv5\_042523\_0143.root, FC#9, port A1

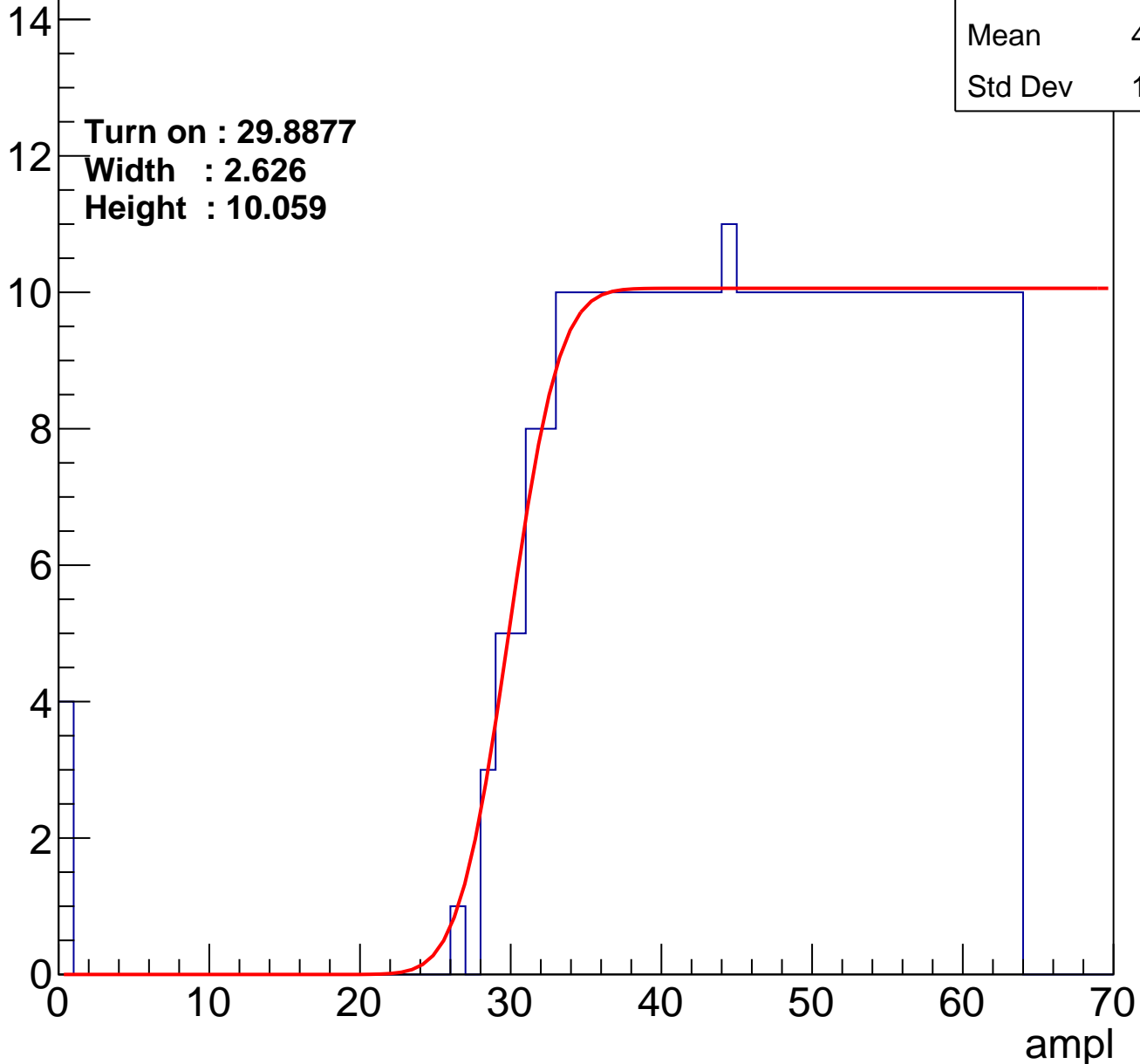
Entries	345
Mean	45.89
Std Dev	11.03

**Turn on : 29.8877**

**Width : 2.626**

**Height : 10.059**

Entry



# B0L001S, U24-ch69

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	357
Mean	45.45
Std Dev	10.74

Turn on : 28.8330

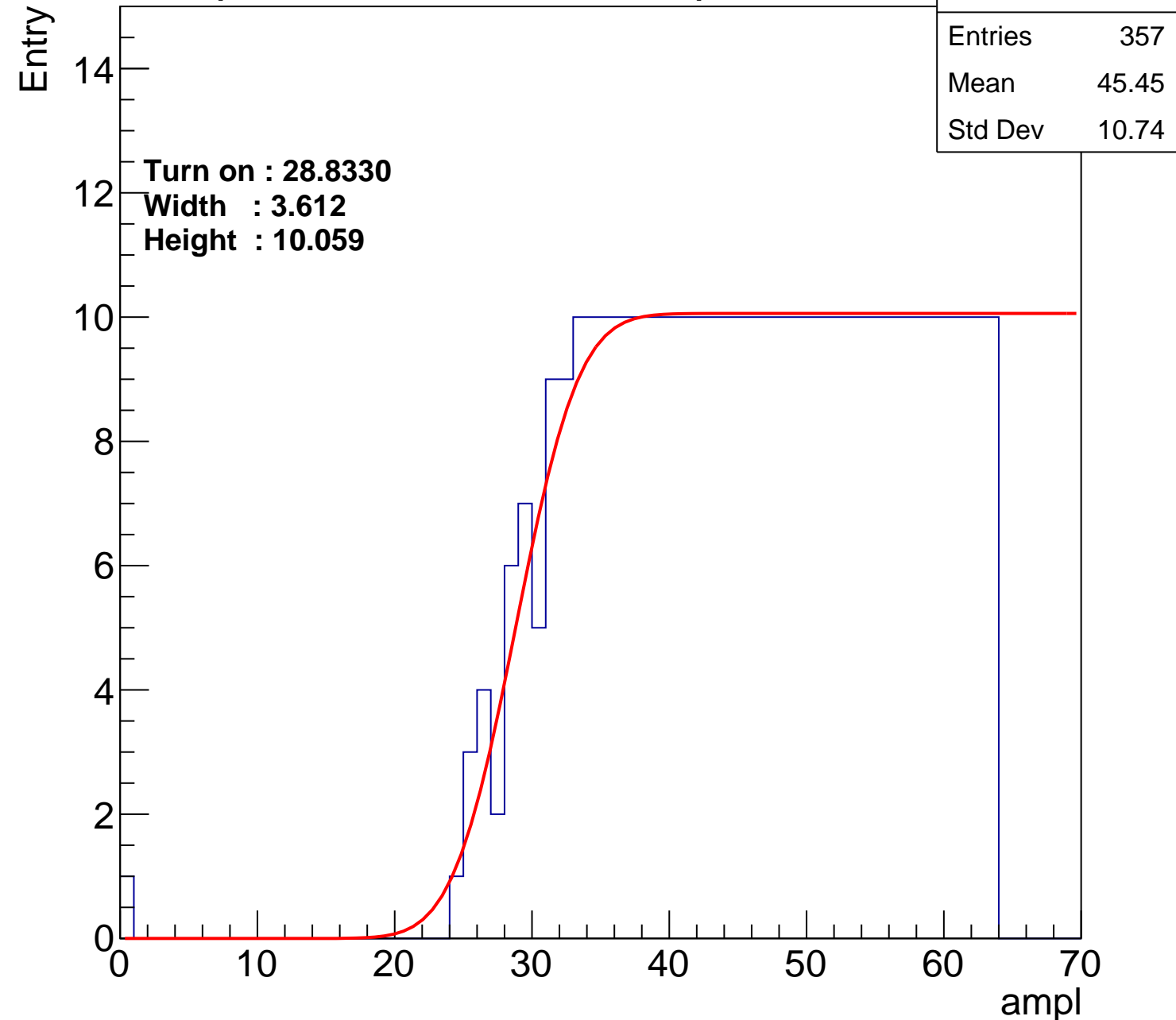
Width : 3.612

Height : 10.059

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch70

calib\_packv5\_042523\_0143.root, FC#9, port A1

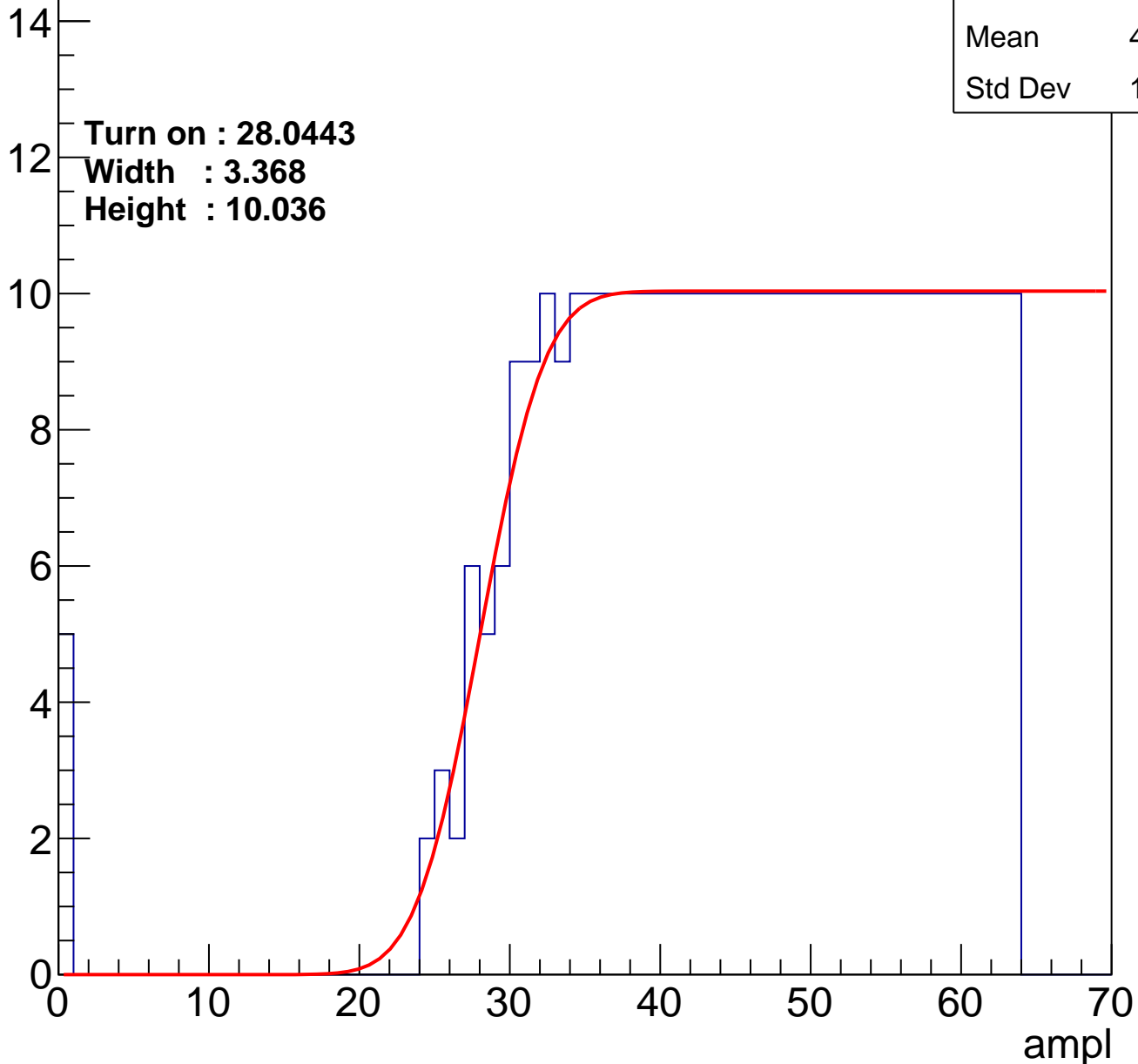
Entries	366
Mean	44.72
Std Dev	11.78

Turn on : 28.0443

Width : 3.368

Height : 10.036

Entry





# B0L001S, U24-ch71

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	374
Mean	44.44
Std Dev	11.71

Turn on : 27.2423

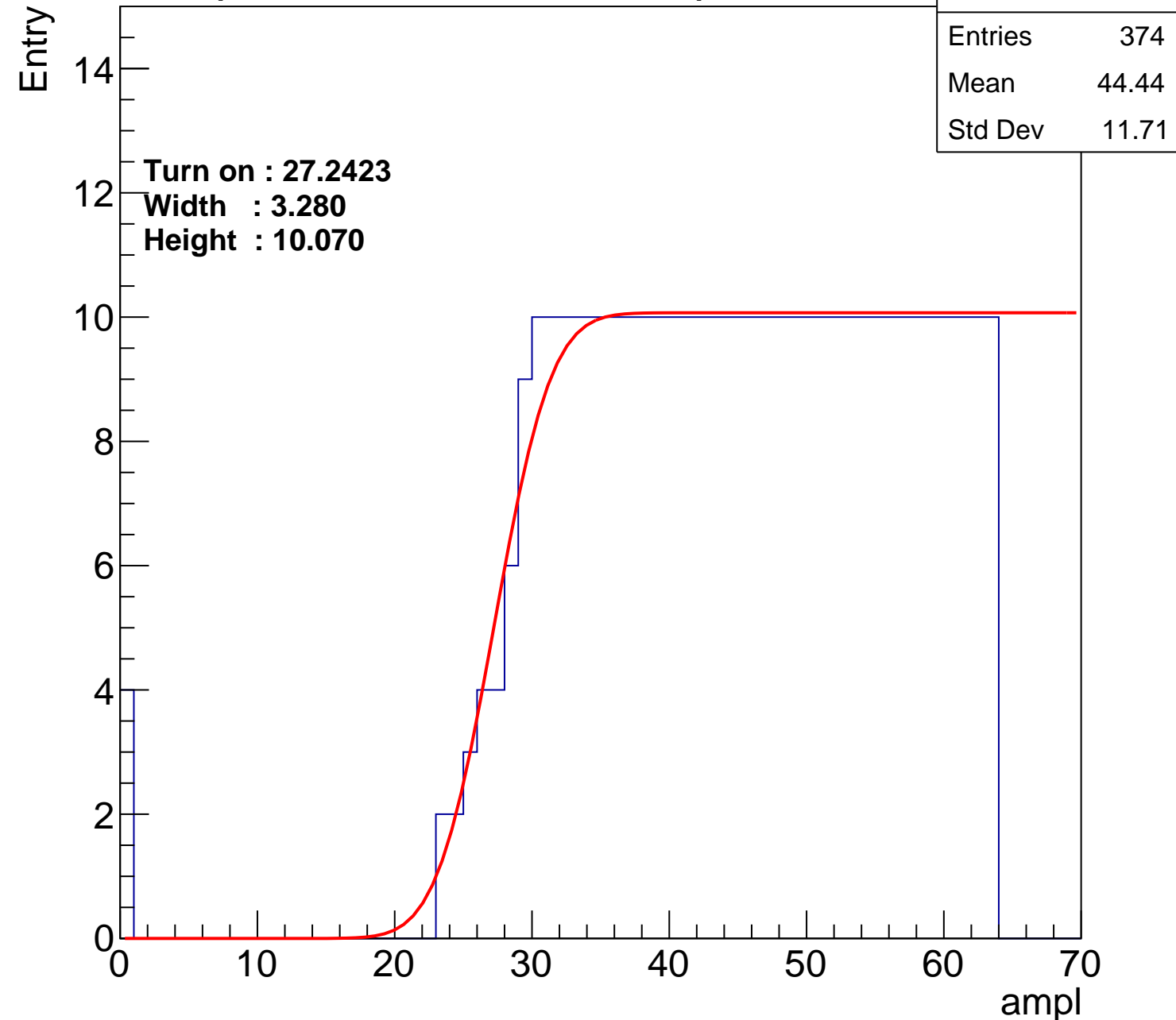
Width : 3.280

Height : 10.070

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch72

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	372
Mean	44.64
Std Dev	11.34

Turn on : 27.1112

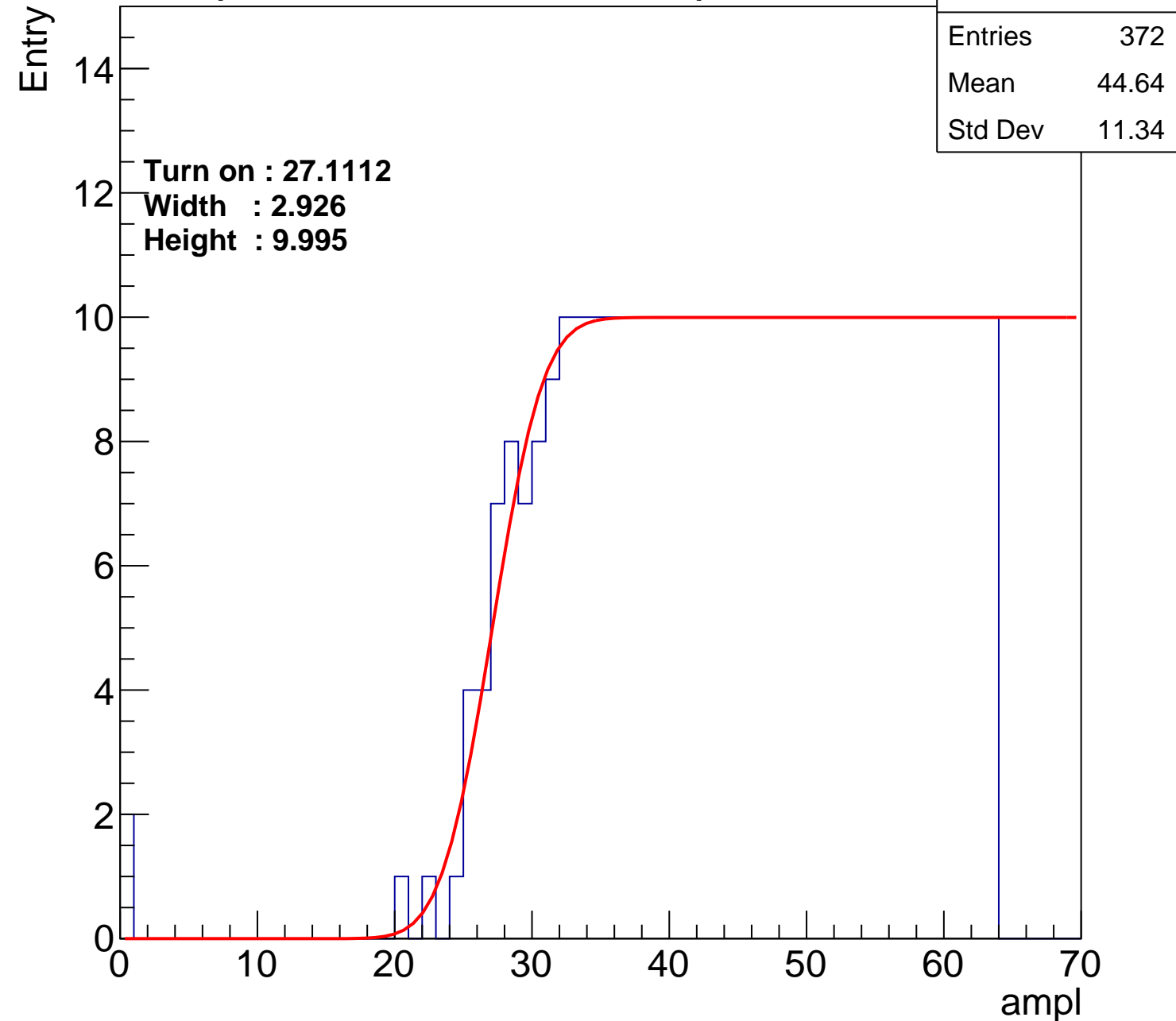
Width : 2.926

Height : 9.995

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch73

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	362
Mean	45.25
Std Dev	10.8

Turn on : 28.1690

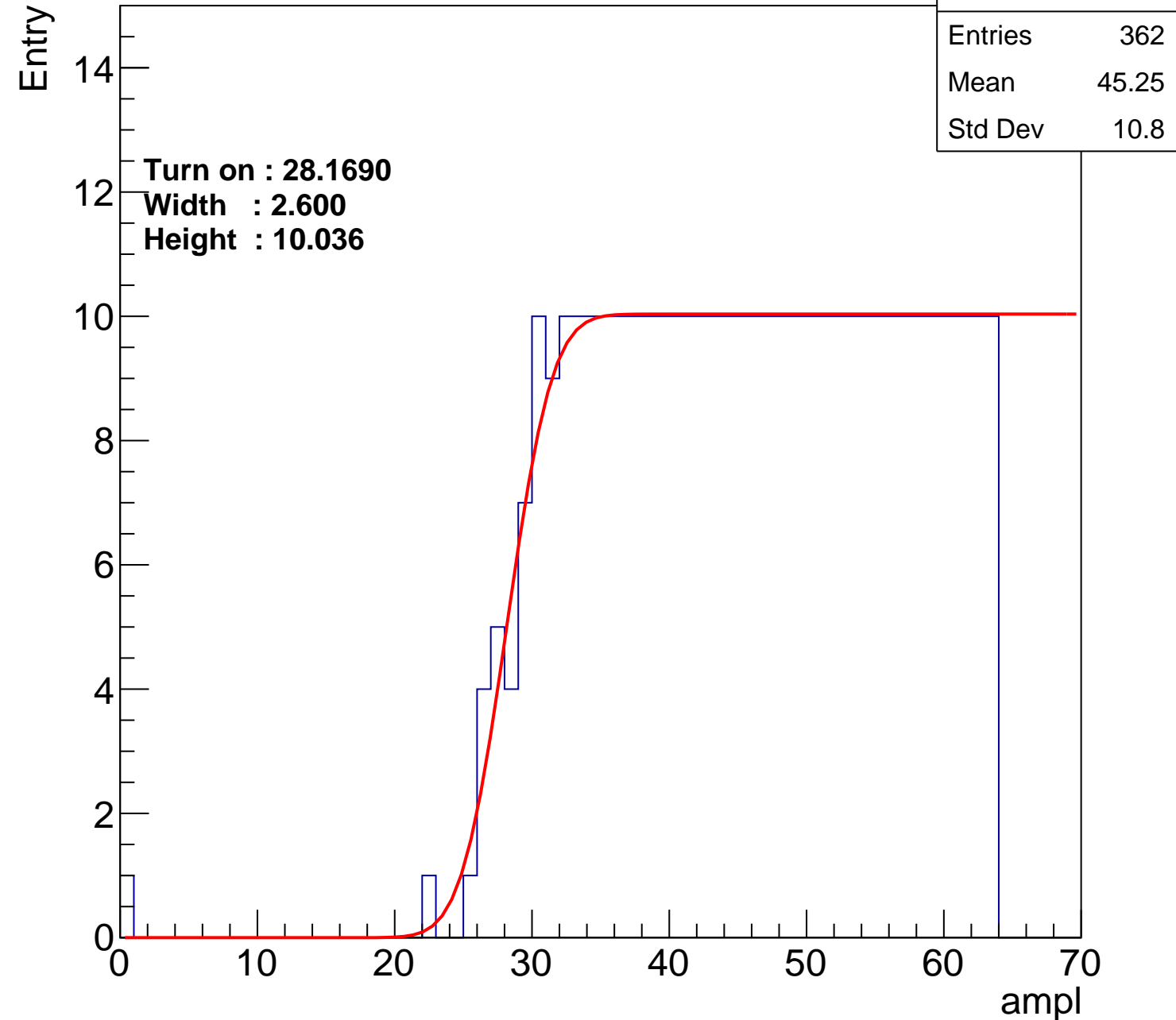
Width : 2.600

Height : 10.036

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch74

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	380
Mean	44.08
Std Dev	12.02

Turn on : 26.8950

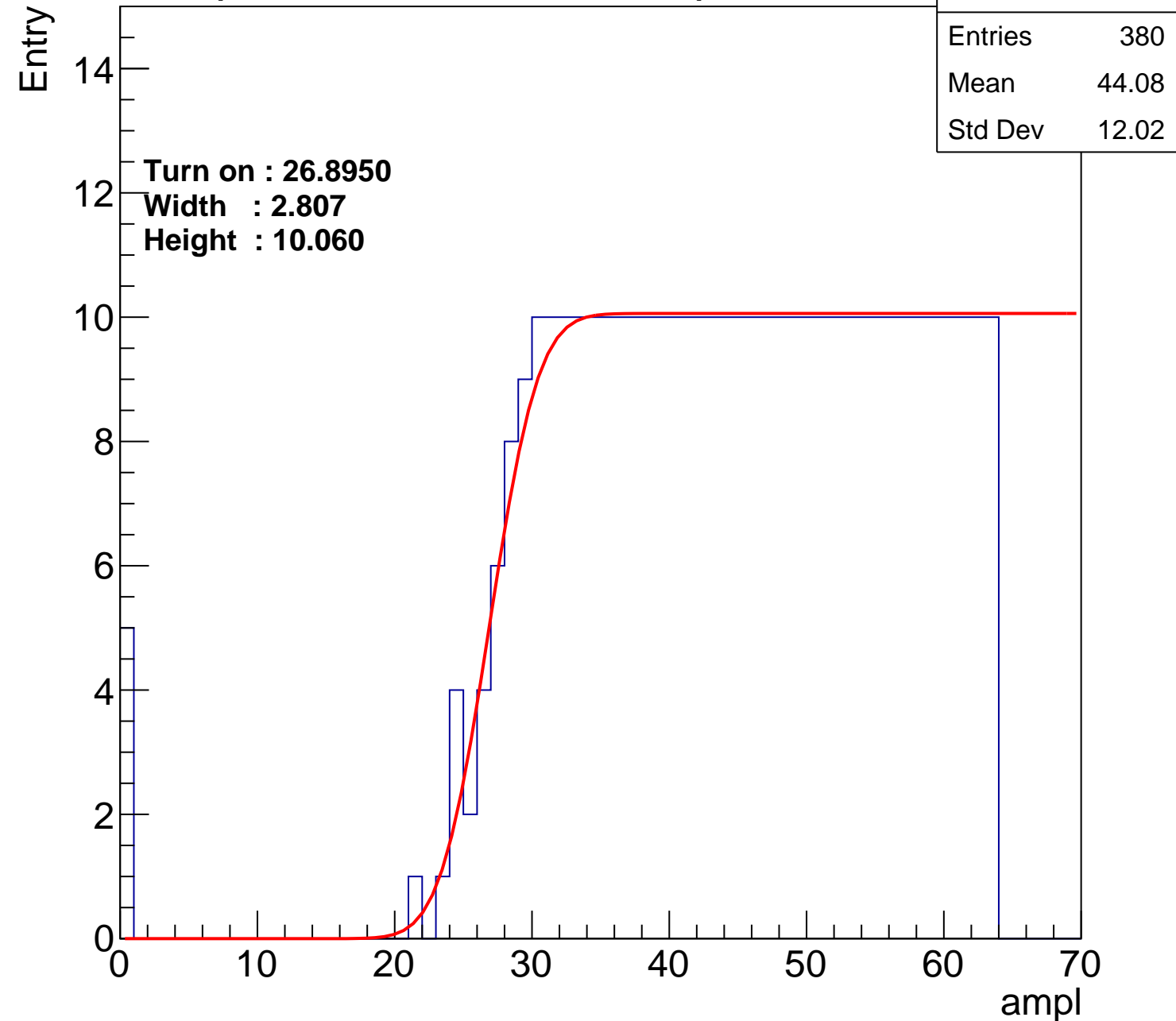
Width : 2.807

Height : 10.060

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch75

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	353
Mean	45.6
Std Dev	11.06

Turn on : 28.9202

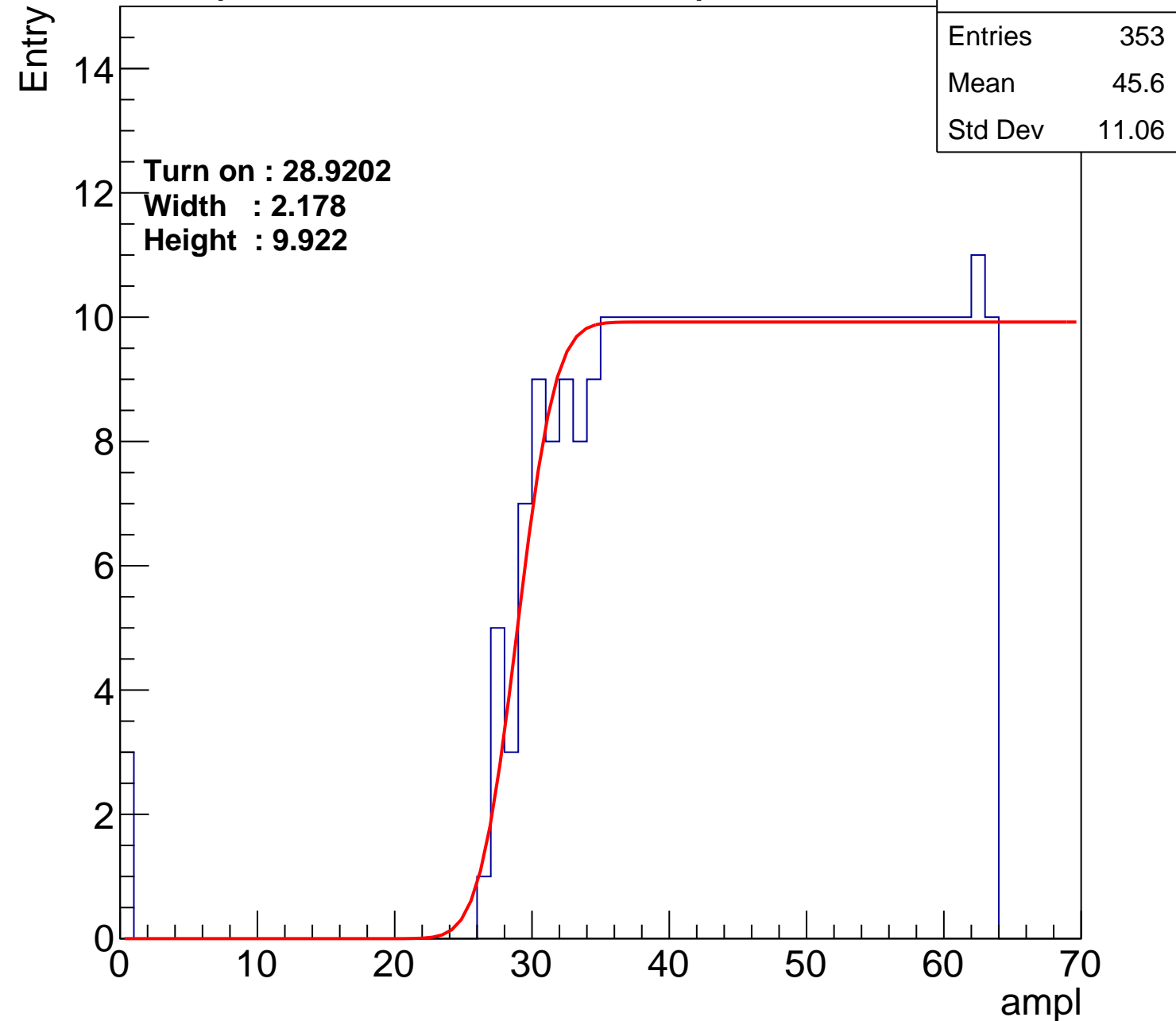
Width : 2.178

Height : 9.922

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch76

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	360
Mean	45.25
Std Dev	10.99

Turn on : 28.1952

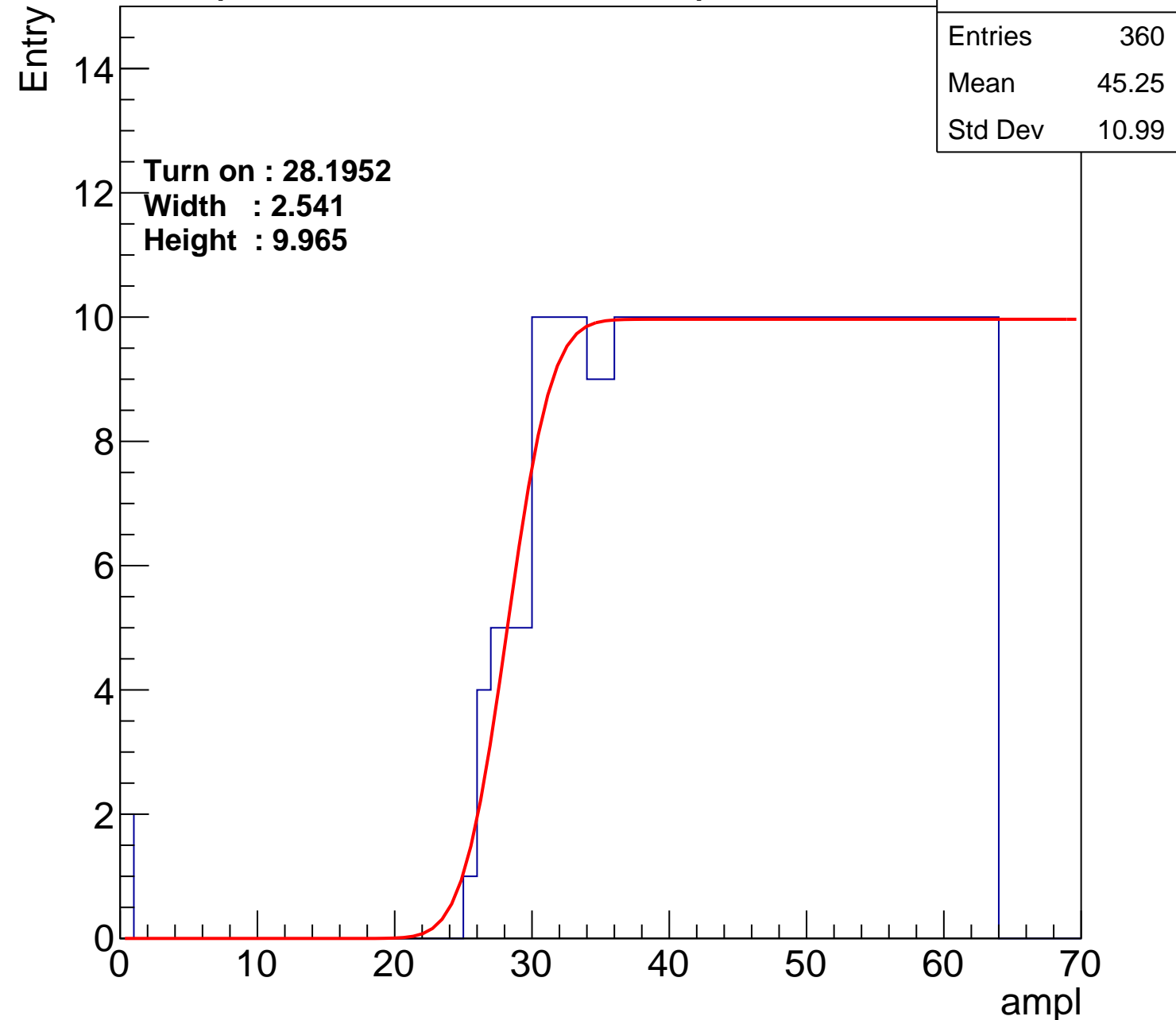
Width : 2.541

Height : 9.965

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch77

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	351
Mean	45.8
Std Dev	10.49

Turn on : 29.0229

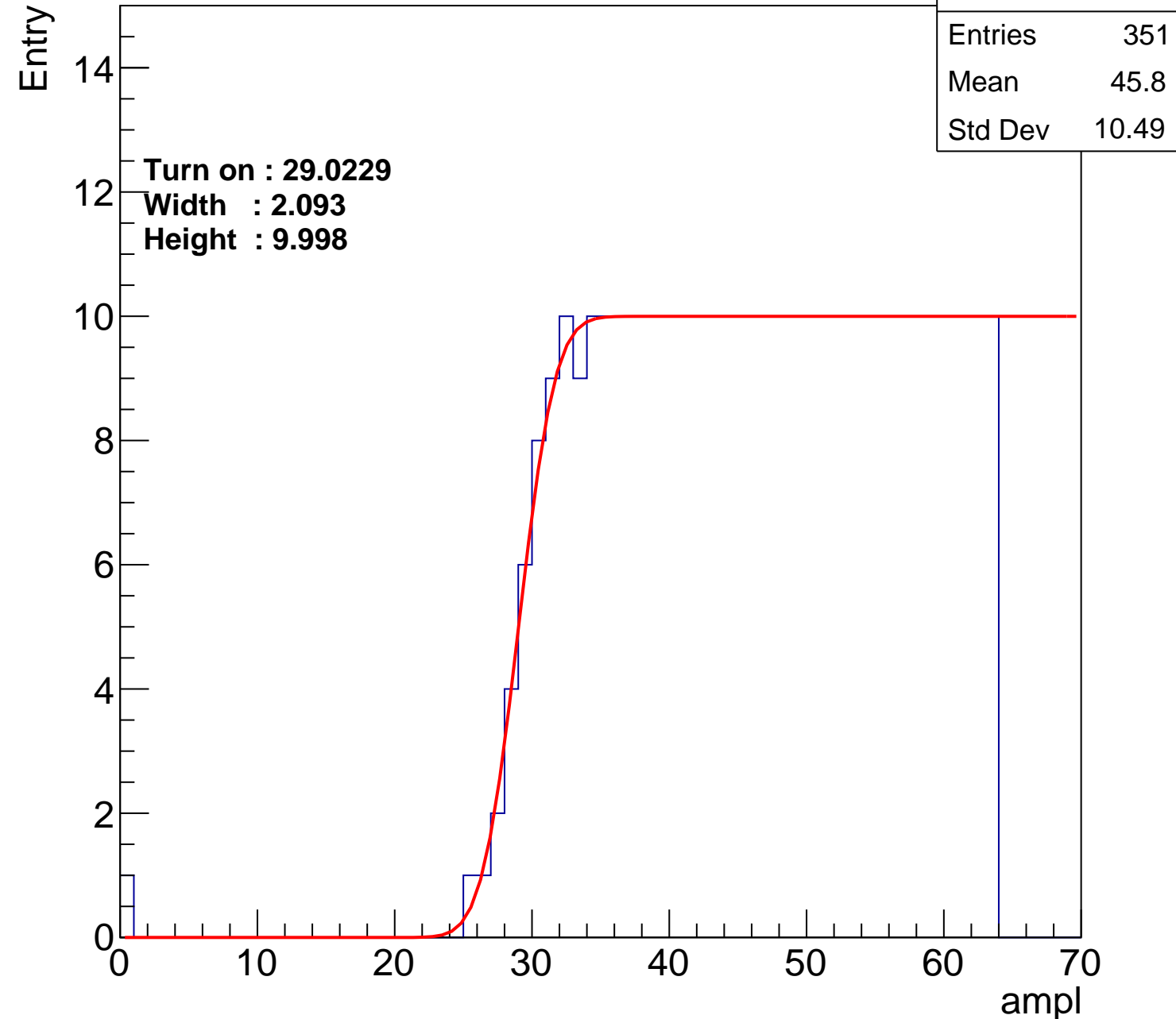
Width : 2.093

Height : 9.998

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch78

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	365
Mean	44.79
Std Dev	11.72

**Turn on : 28.4177**

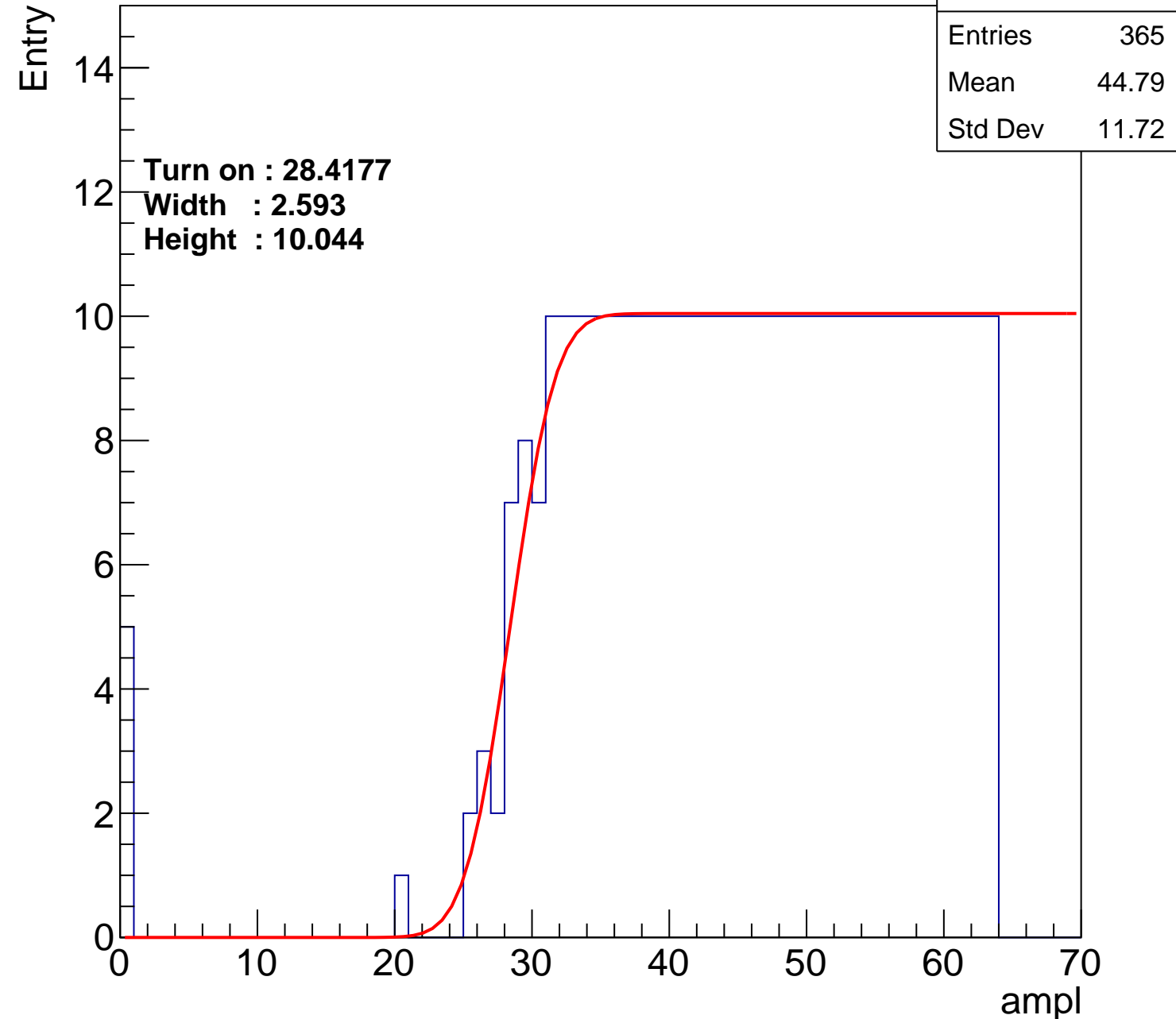
**Width : 2.593**

**Height : 10.044**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U24-ch79

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	374
Mean	44.55
Std Dev	11.37

Turn on : 27.3494

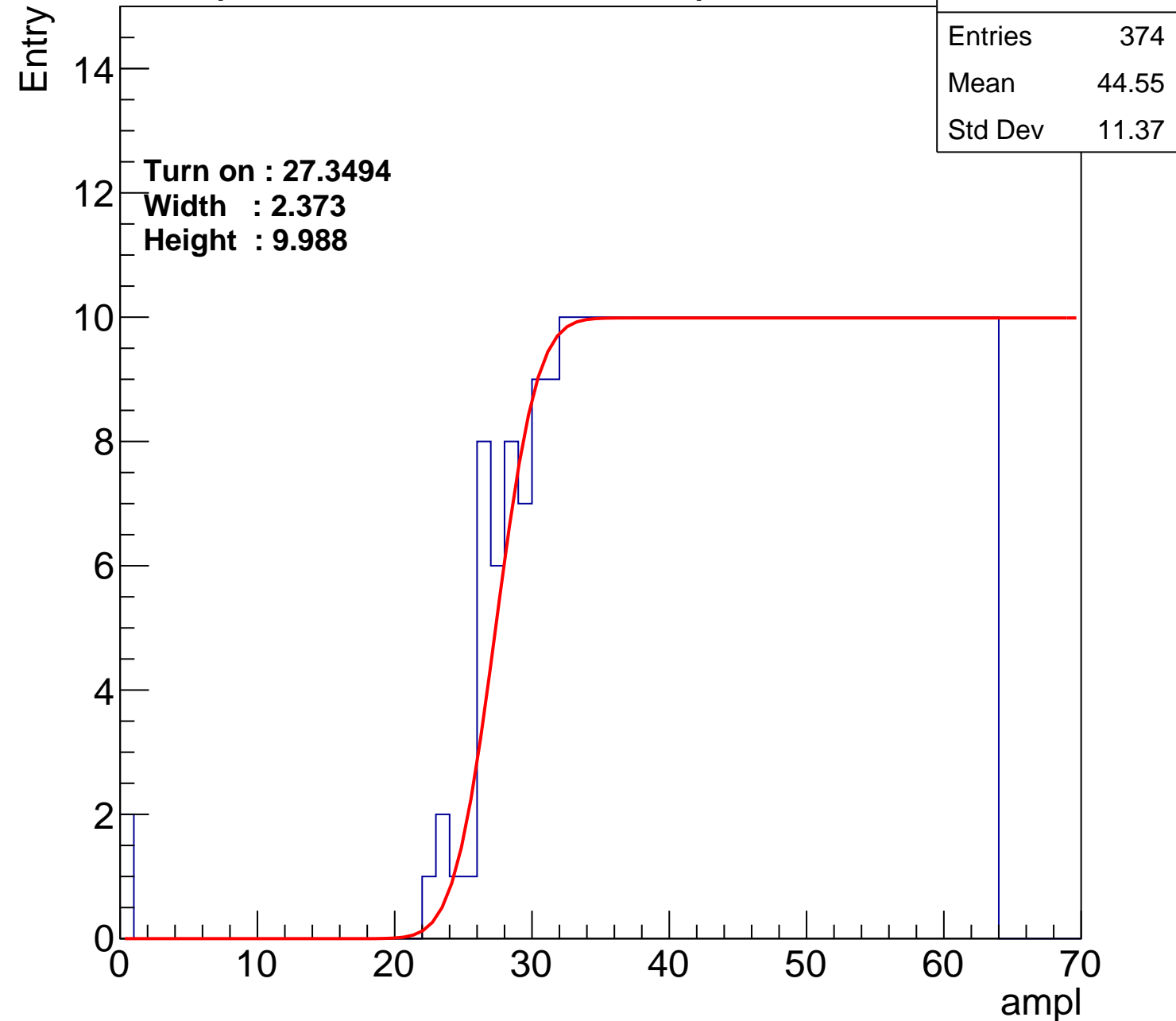
Width : 2.373

Height : 9.988

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch80

calib\_packv5\_042523\_0143.root, FC#9, port A1

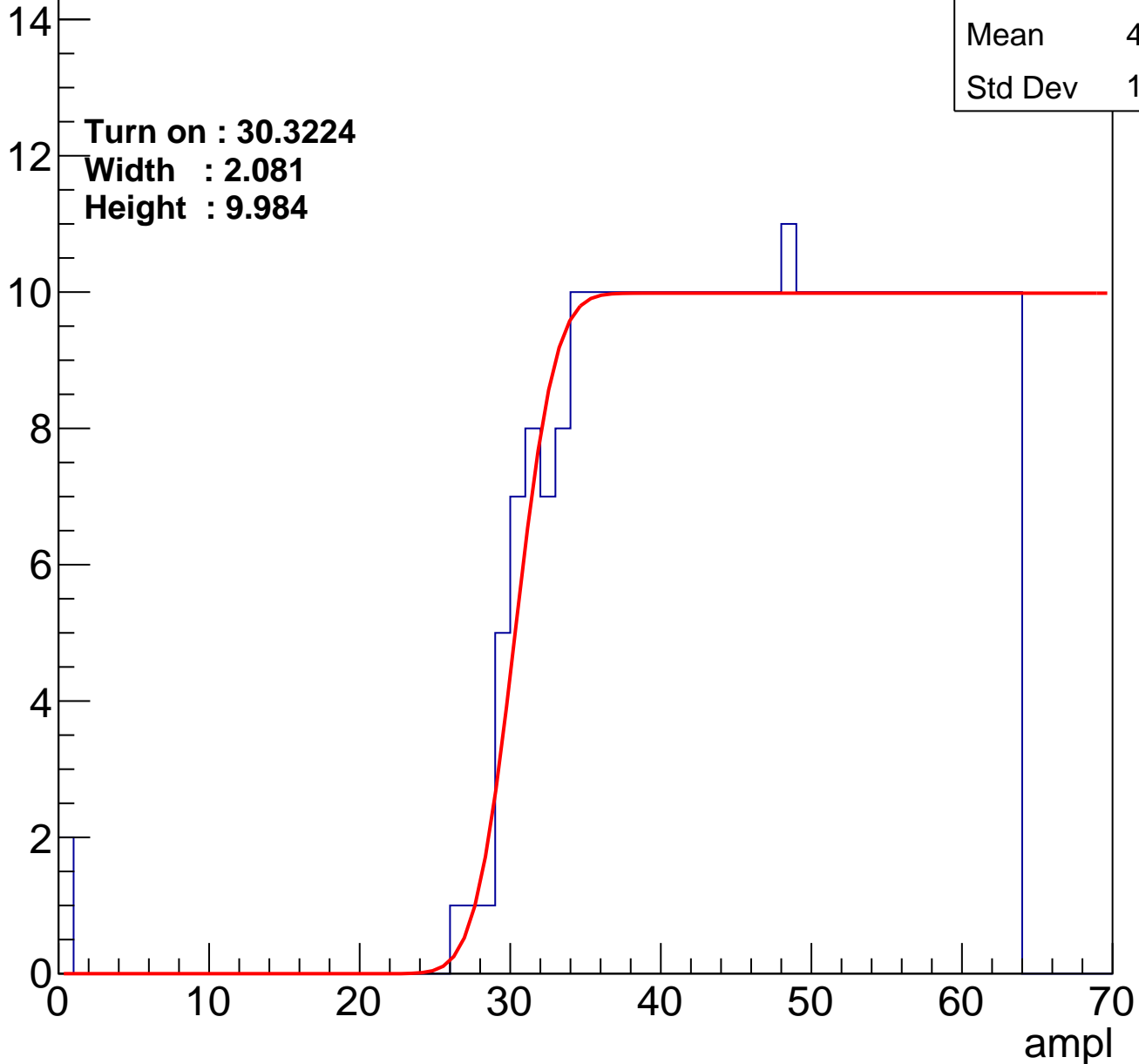
Entries	341
Mean	46.25
Std Dev	10.47

Turn on : 30.3224

Width : 2.081

Height : 9.984

Entry



# B0L001S, U24-ch81

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	376
Mean	44.39
Std Dev	11.6

Turn on : 28.0201

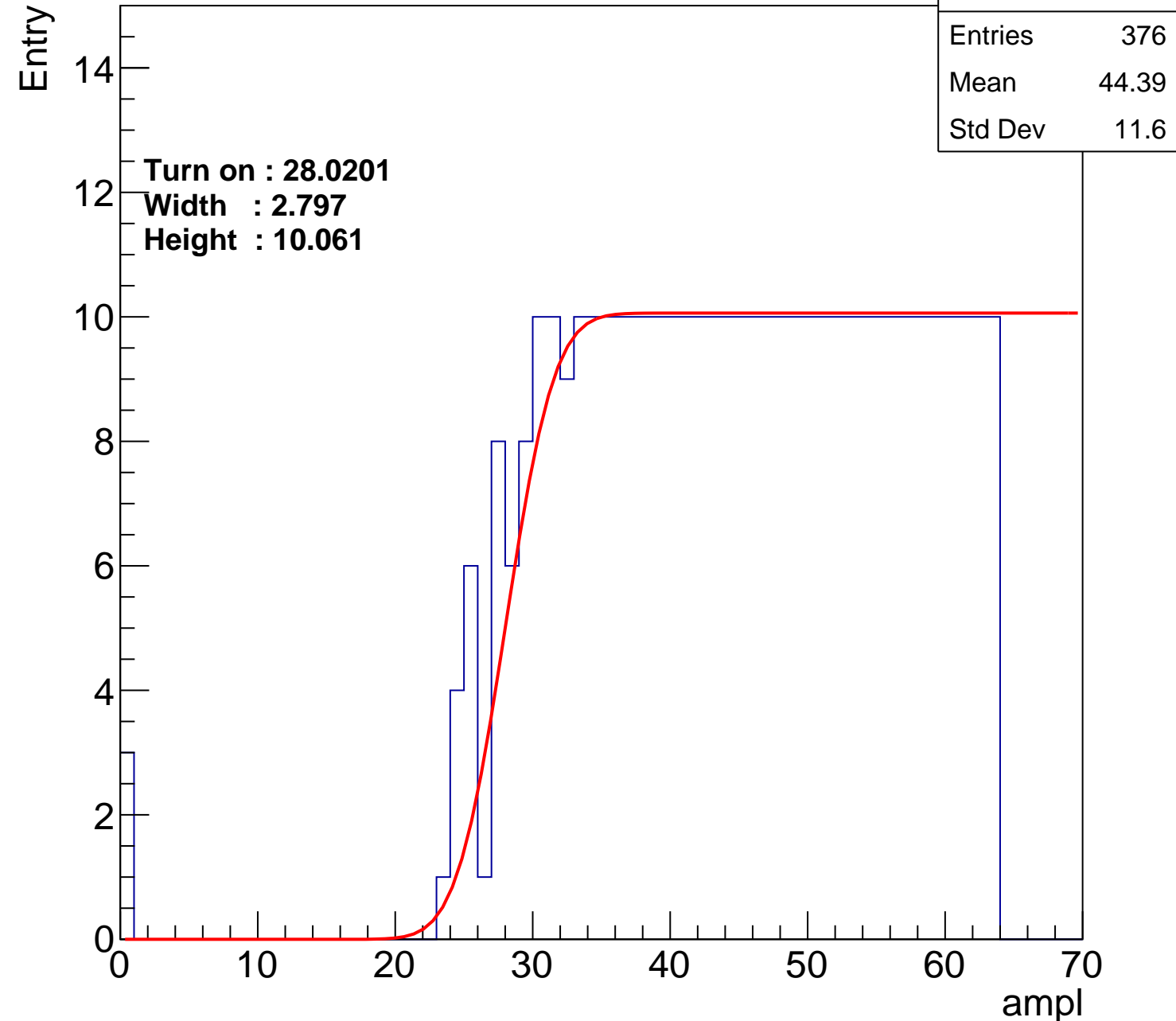
Width : 2.797

Height : 10.061

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch82

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	379
Mean	44.23
Std Dev	11.69

Turn on : 26.7521

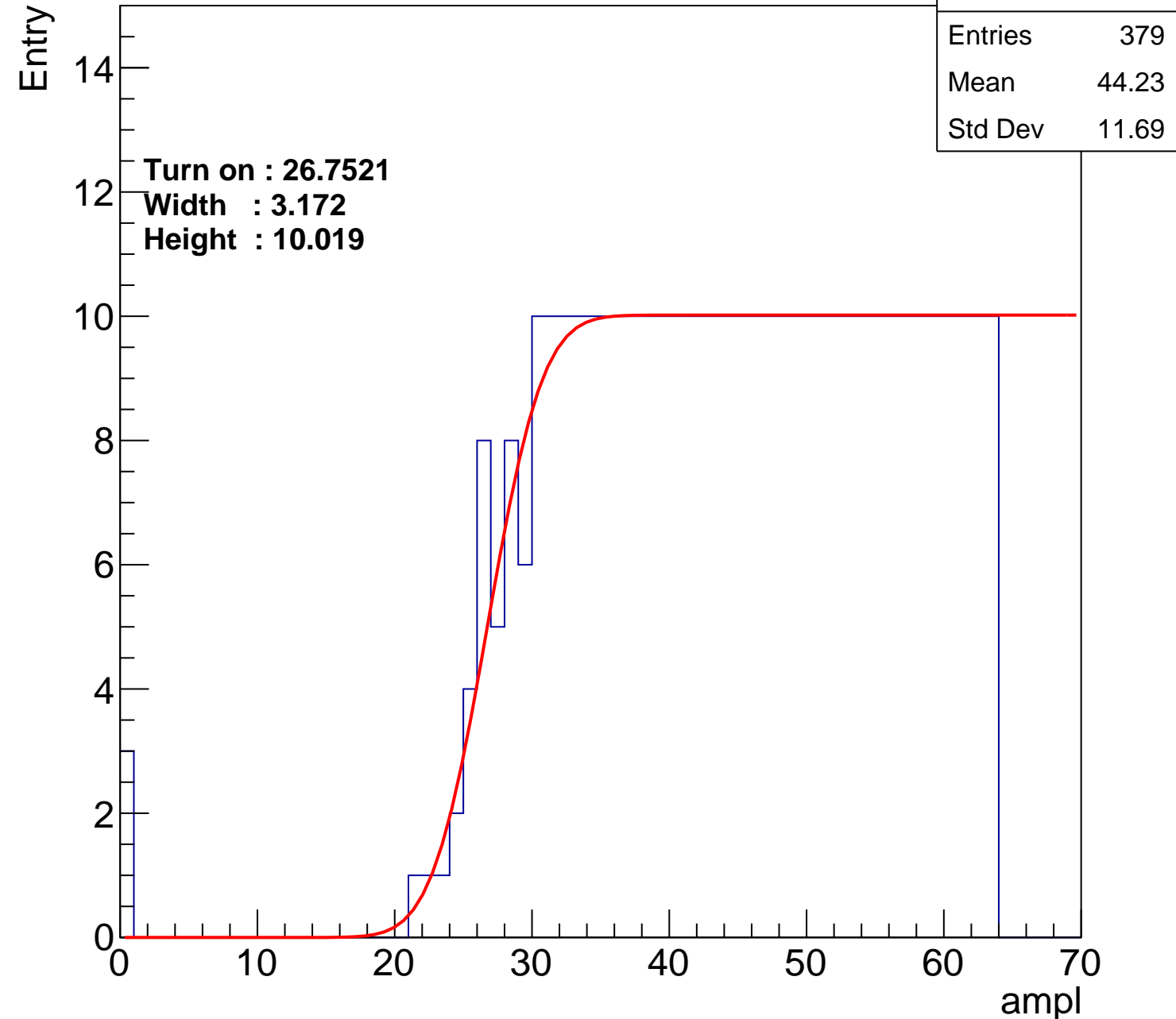
Width : 3.172

Height : 10.019

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch83

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	356
Mean	45.17
Std Dev	11.61

Turn on : 29.2581

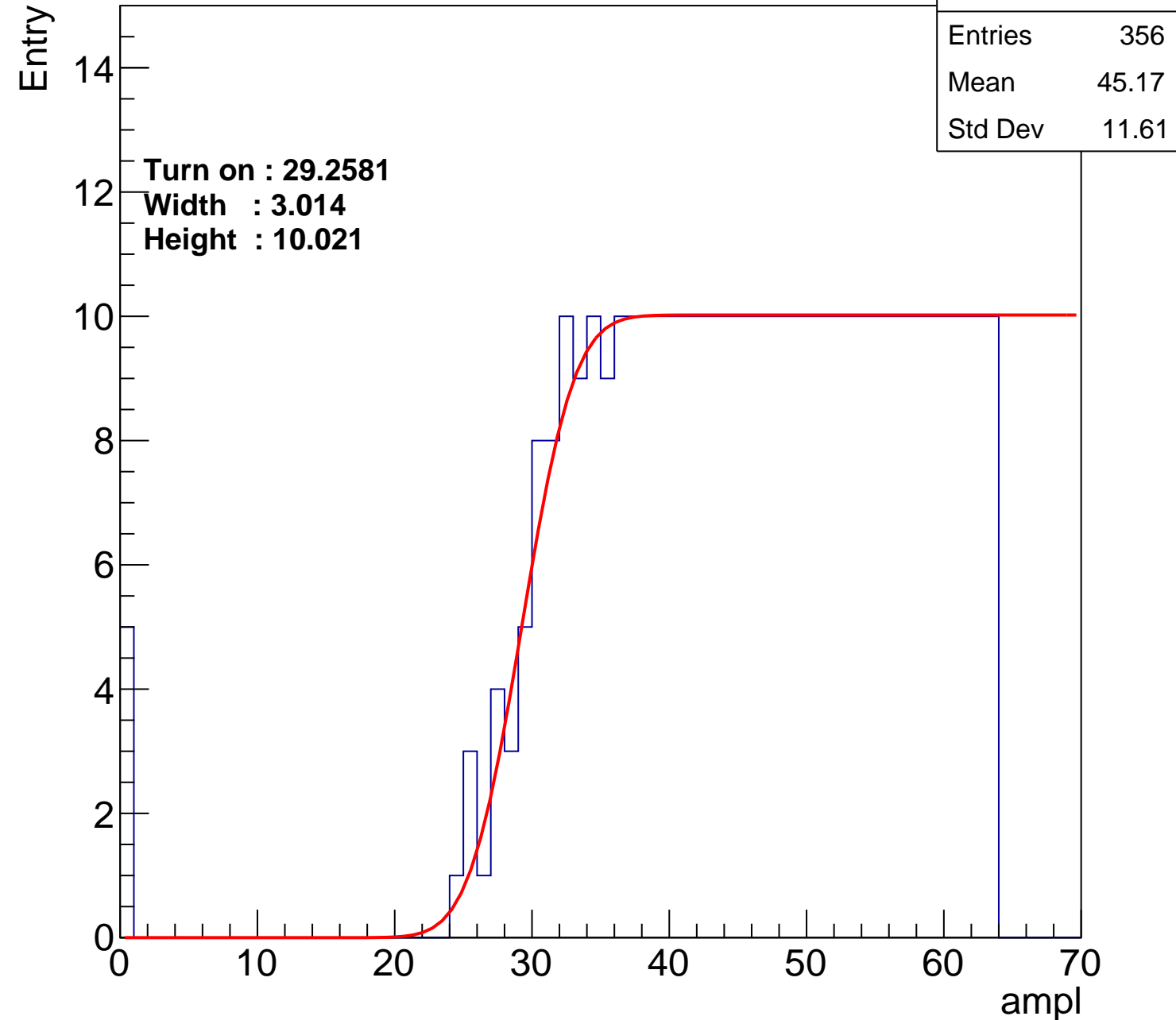
Width : 3.014

Height : 10.021

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch84

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	363
Mean	44.89
Std Dev	11.67

Turn on : 28.5291

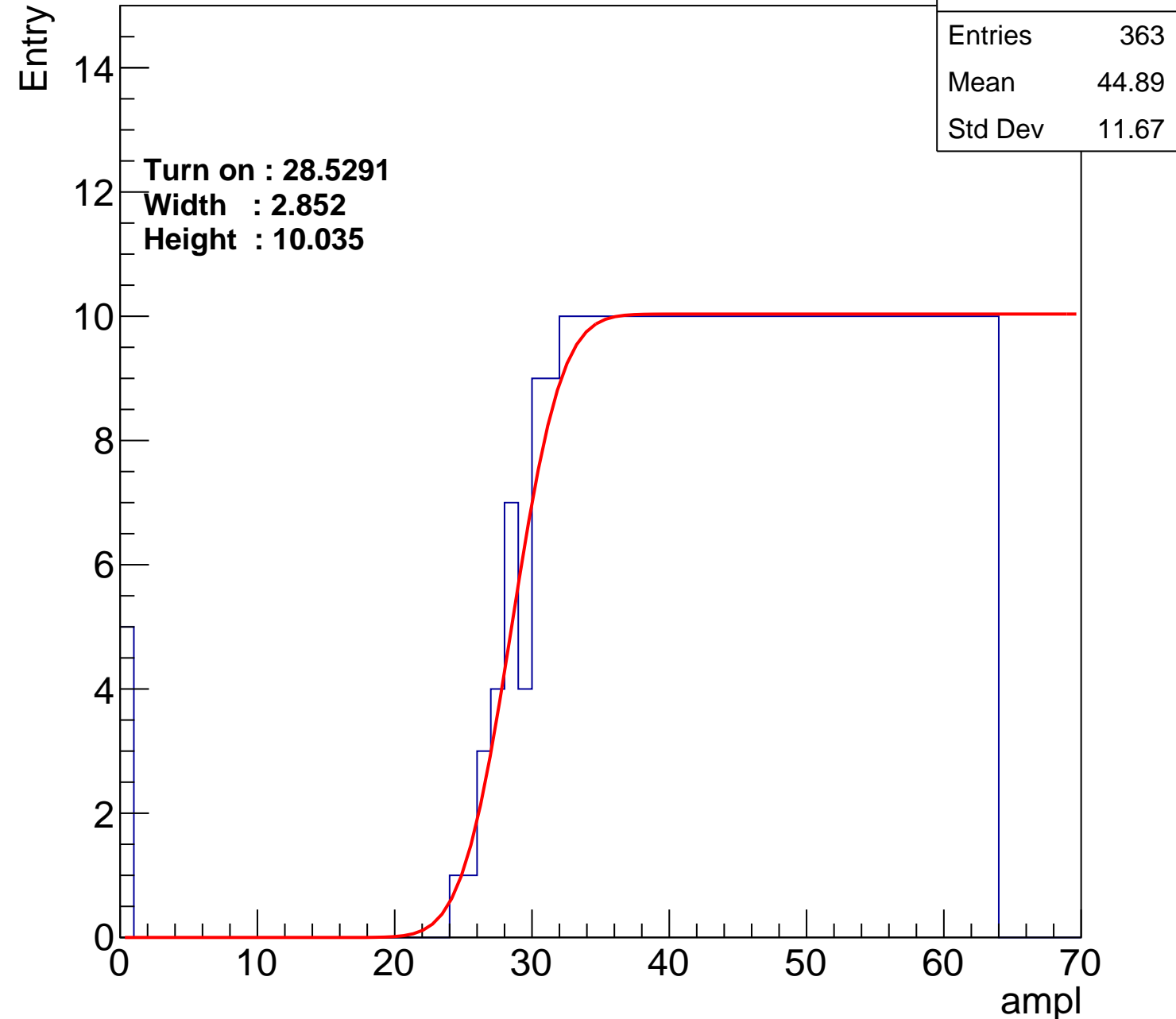
Width : 2.852

Height : 10.035

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch85

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	364
Mean	45.04
Std Dev	11.13

Turn on : 28.5881

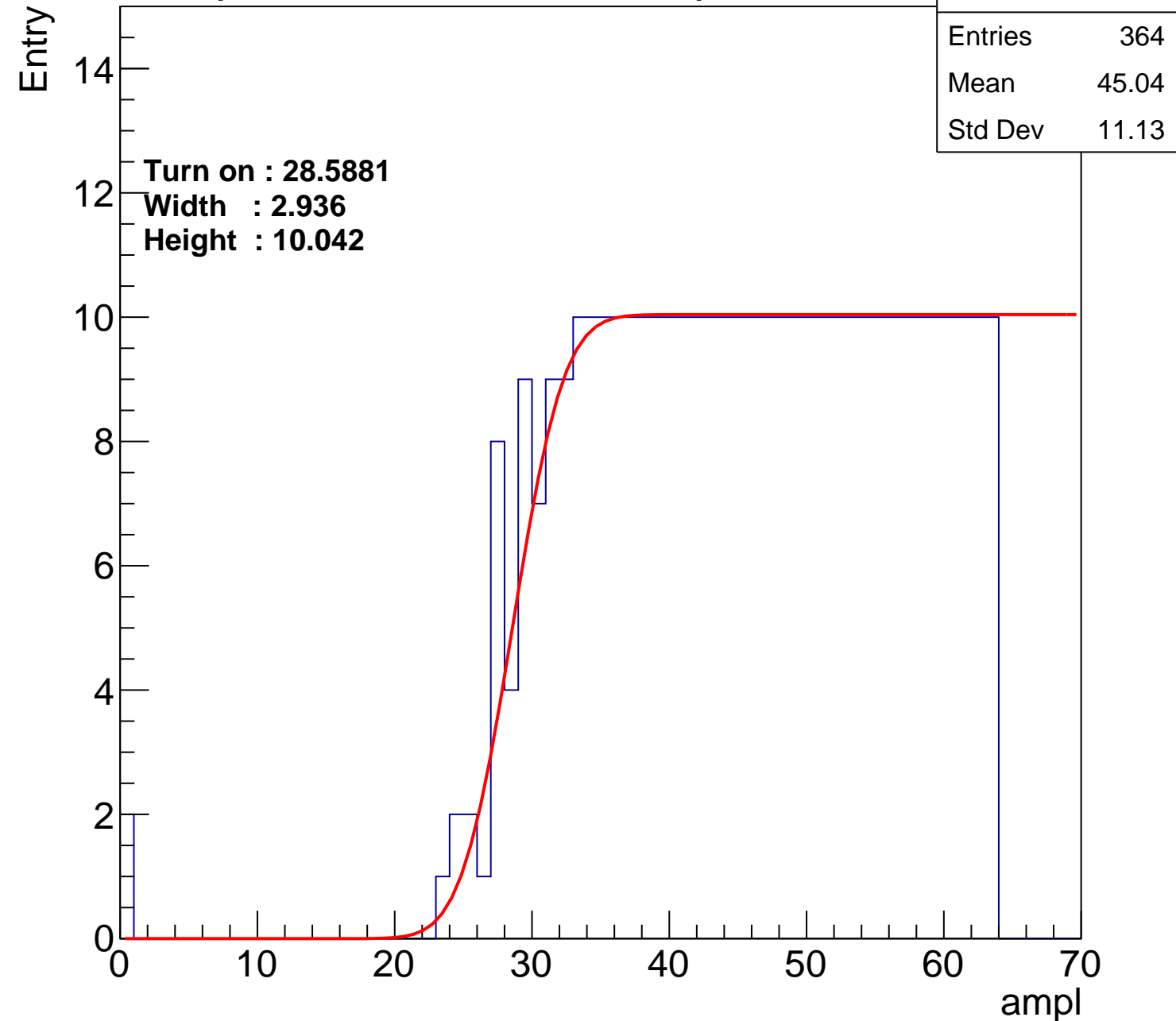
Width : 2.936

Height : 10.042

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch86

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	374
Mean	44.58
Std Dev	11.25

**Turn on : 27.7065**

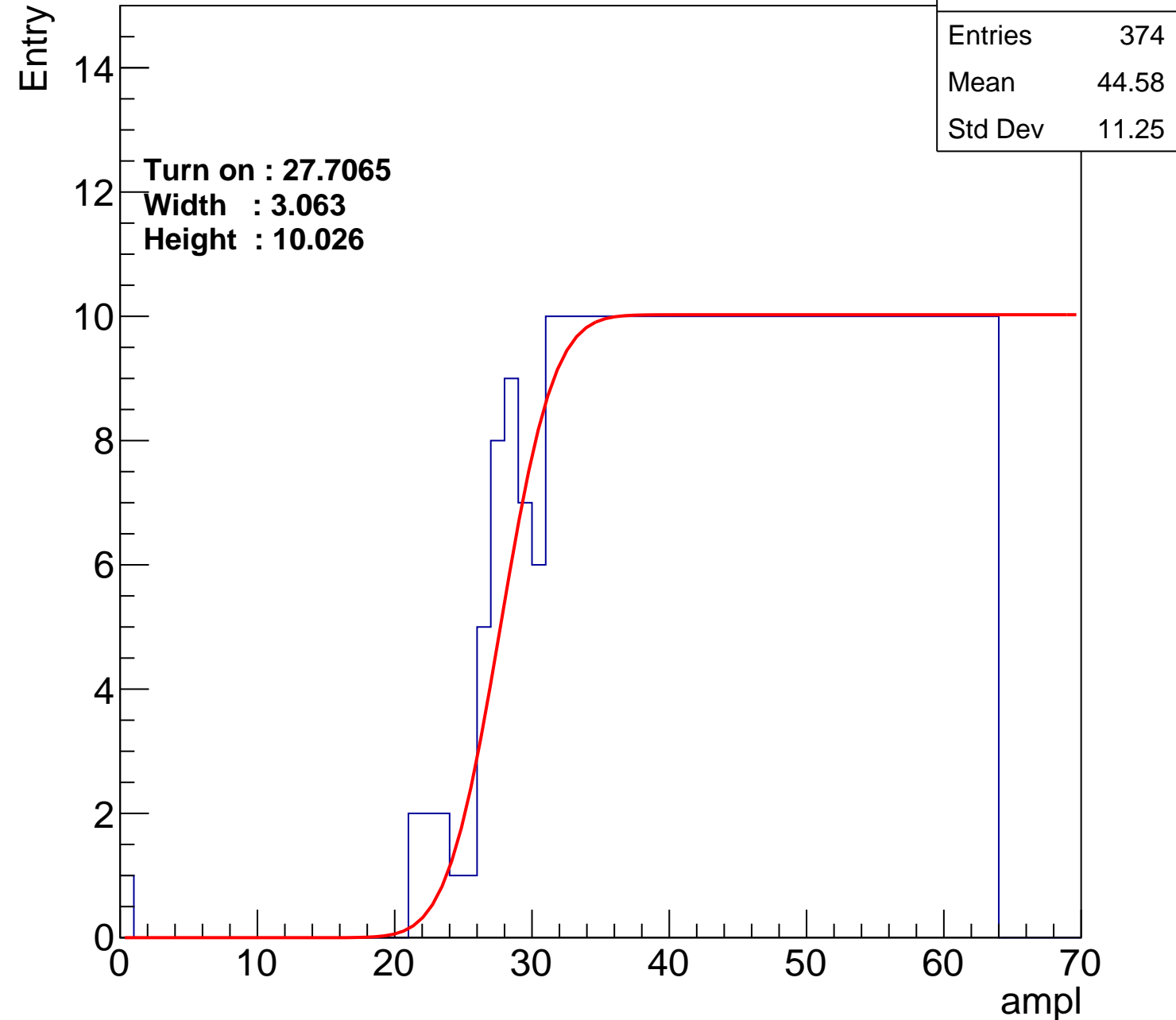
**Width : 3.063**

**Height : 10.026**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





B0L001S, U24-ch87

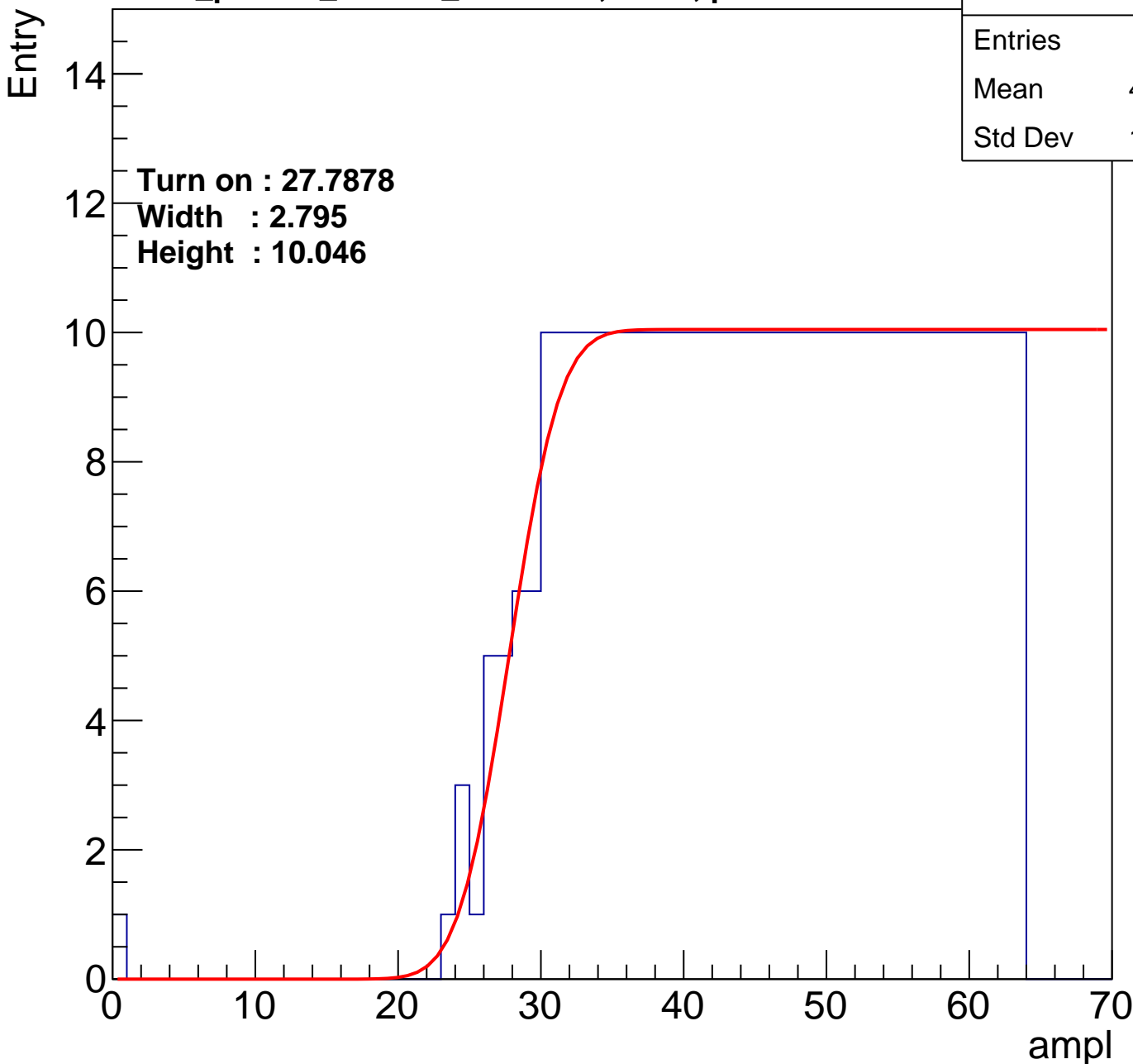
**calib\_packv5\_042523\_0143.root, FC#9, port A1**

Entries	368
Mean	44.94
Std Dev	10.99

**Turn on : 27.7878**

**Width : 2.795**

**Height : 10.046**



# B0L001S, U24-ch88

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	349
Mean	45.63
Std Dev	11.18

Turn on : 29.5041

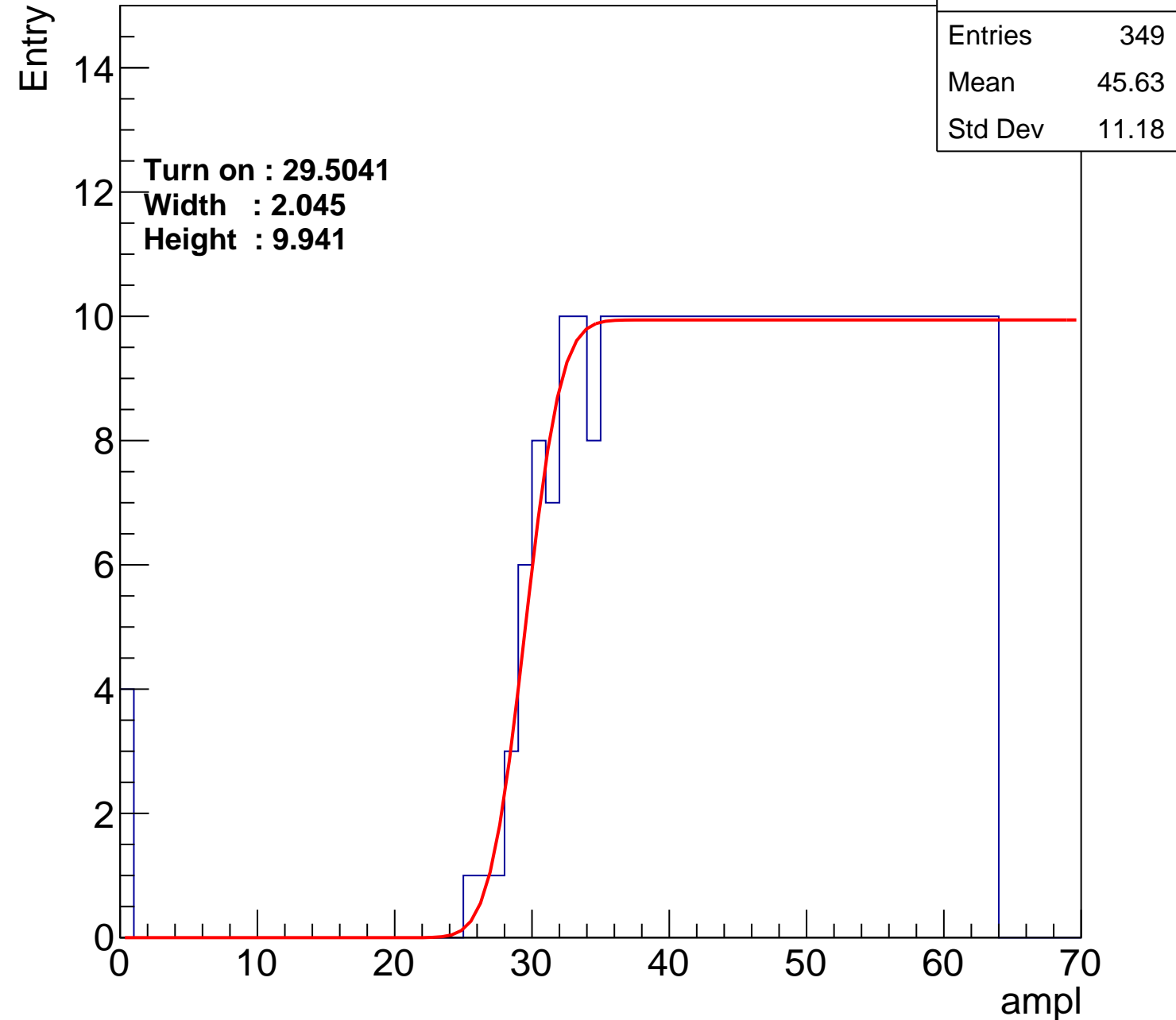
Width : 2.045

Height : 9.941

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch89

calib\_packv5\_042523\_0143.root, FC#9, port A1

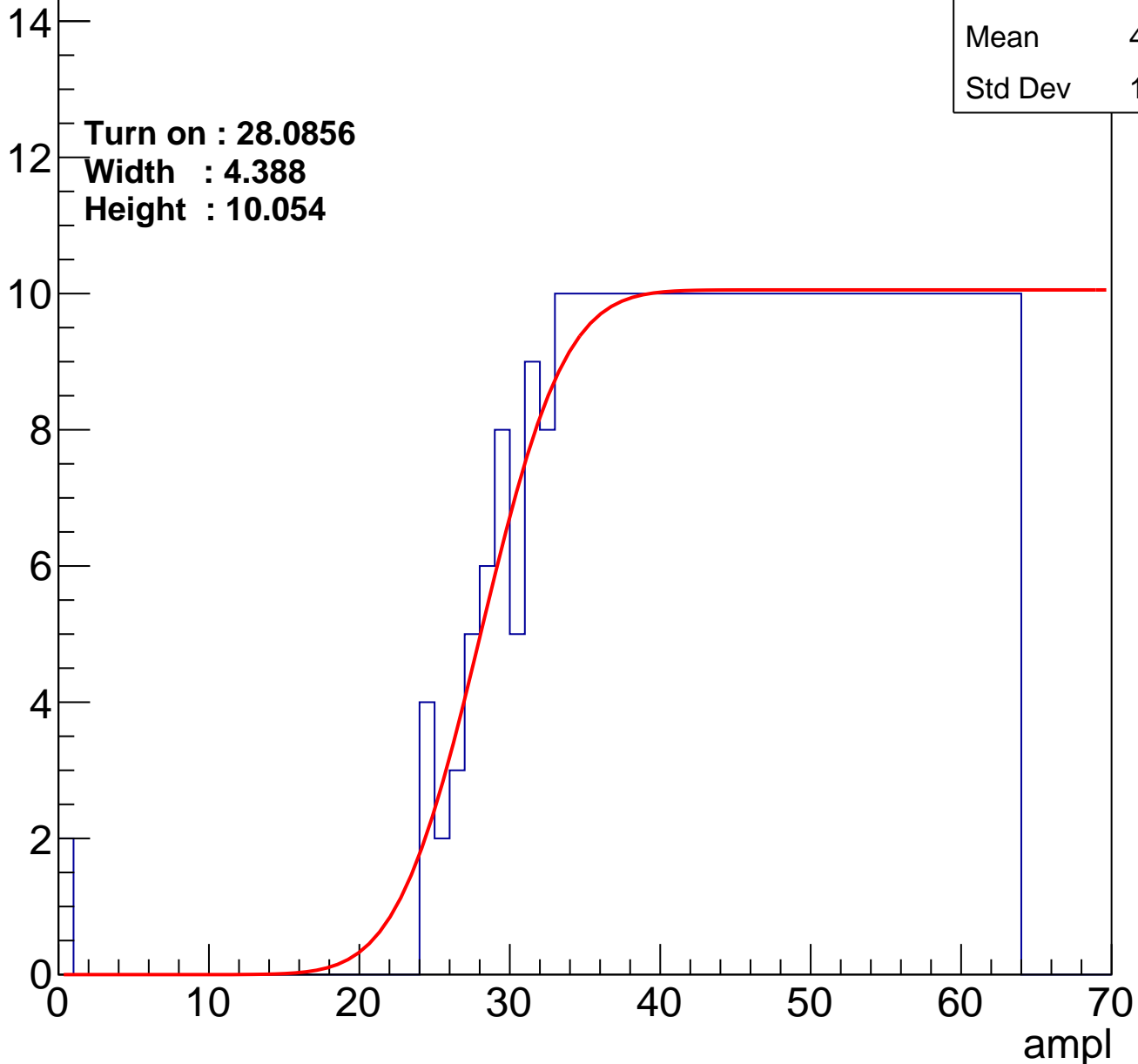
Entries	362
Mean	45.09
Std Dev	11.14

Turn on : 28.0856

Width : 4.388

Height : 10.054

Entry



# B0L001S, U24-ch90

calib\_packv5\_042523\_0143.root, FC#9, port A1

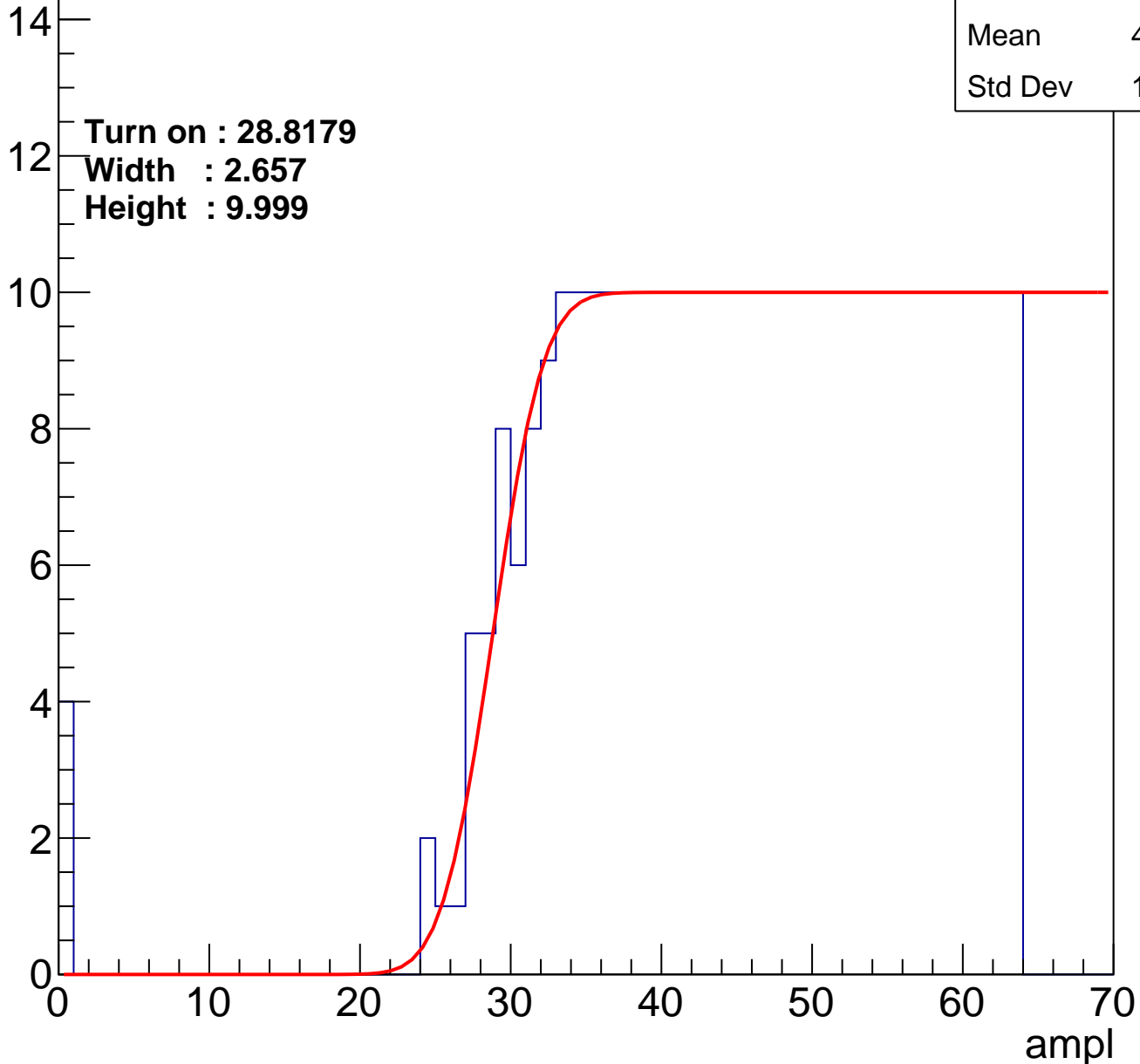
Entries	359
Mean	45.13
Std Dev	11.43

Turn on : 28.8179

Width : 2.657

Height : 9.999

Entry



# B0L001S, U24-ch91

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	358
Mean	45.27
Std Dev	11.17

**Turn on : 28.7973**

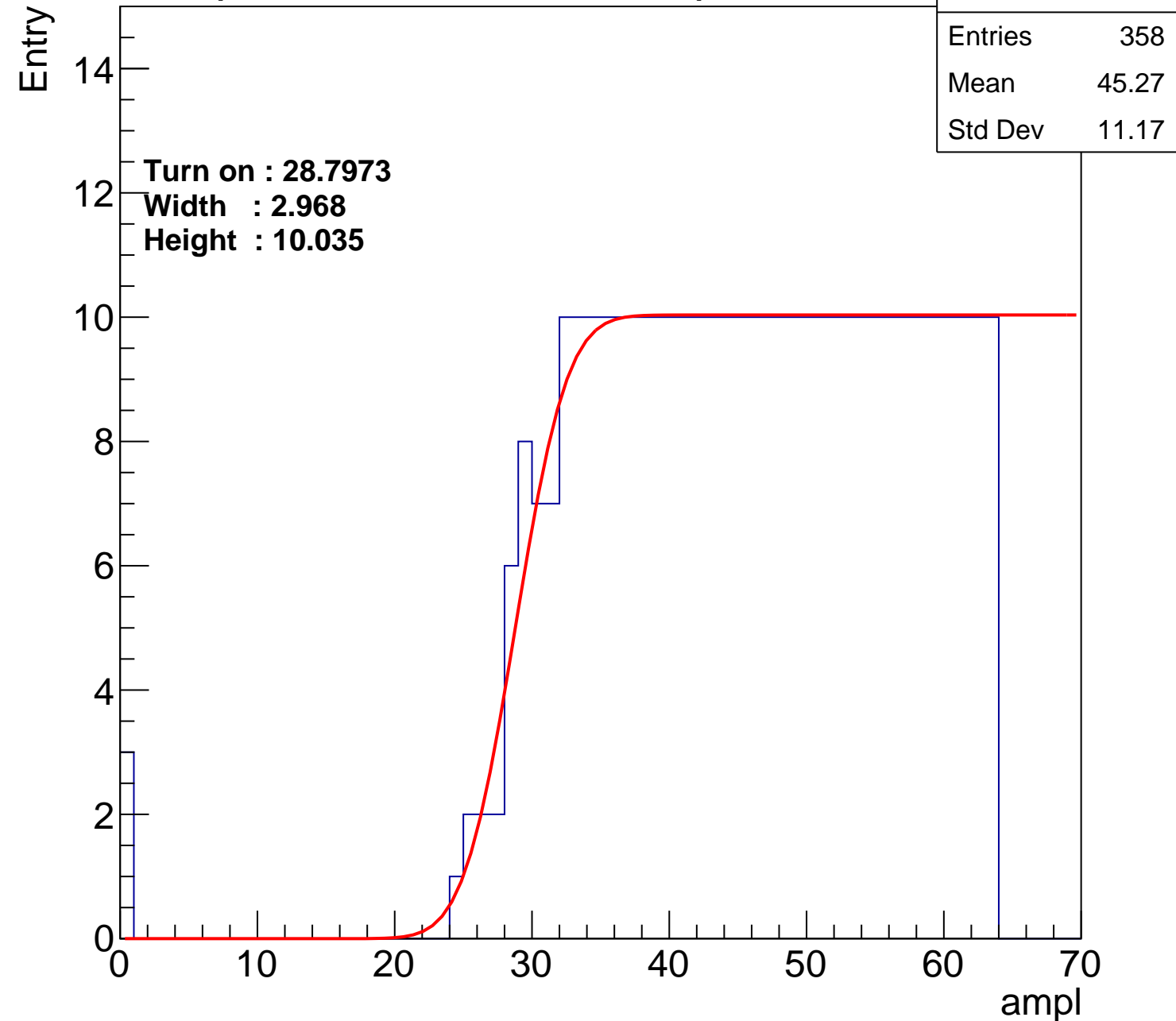
**Width : 2.968**

**Height : 10.035**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch92

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	375
Mean	44.6
Std Dev	11.16

Turn on : 26.5763

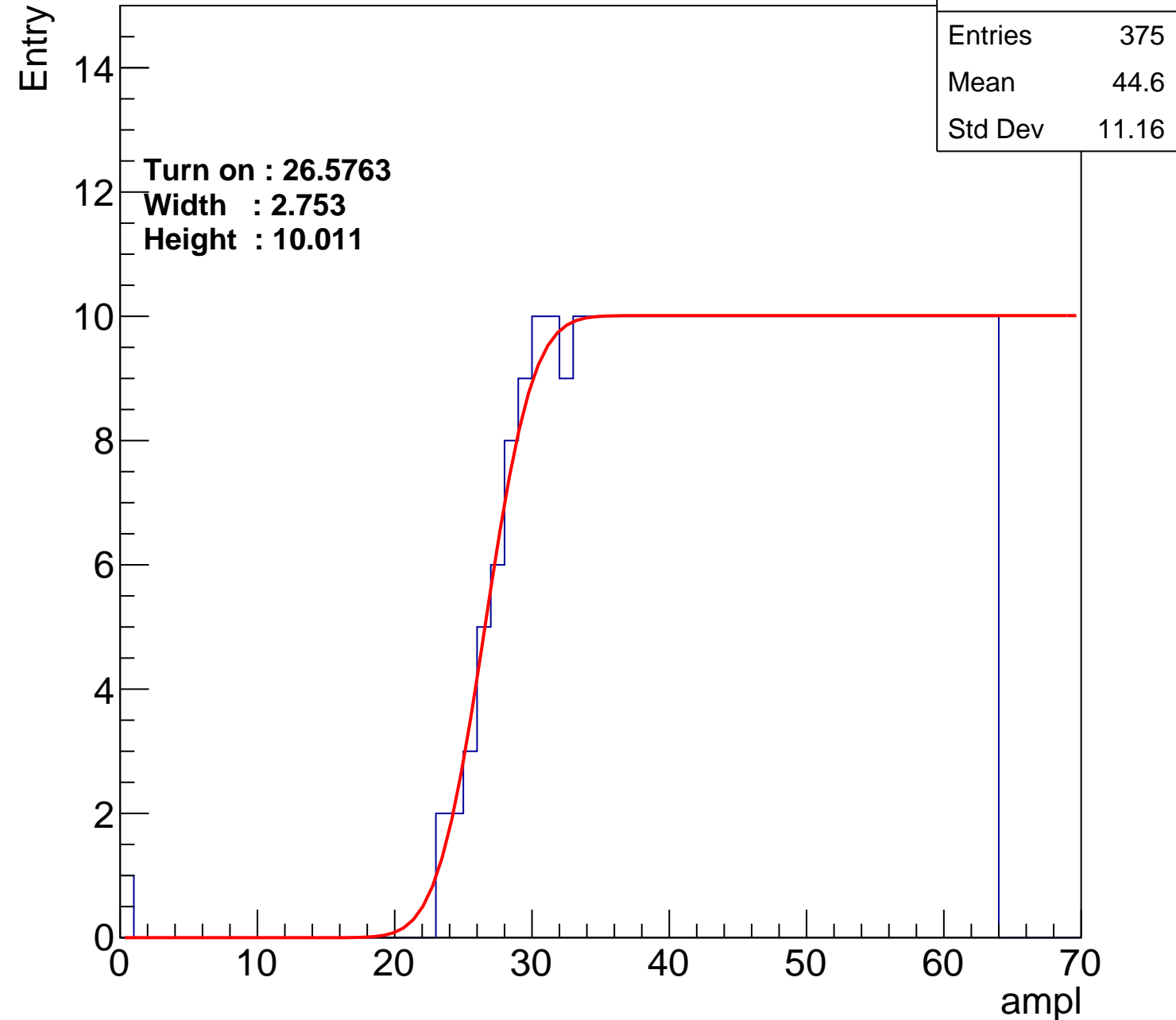
Width : 2.753

Height : 10.011

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch93

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	339
Mean	46.29
Std Dev	10.47

**Turn on : 30.4377**

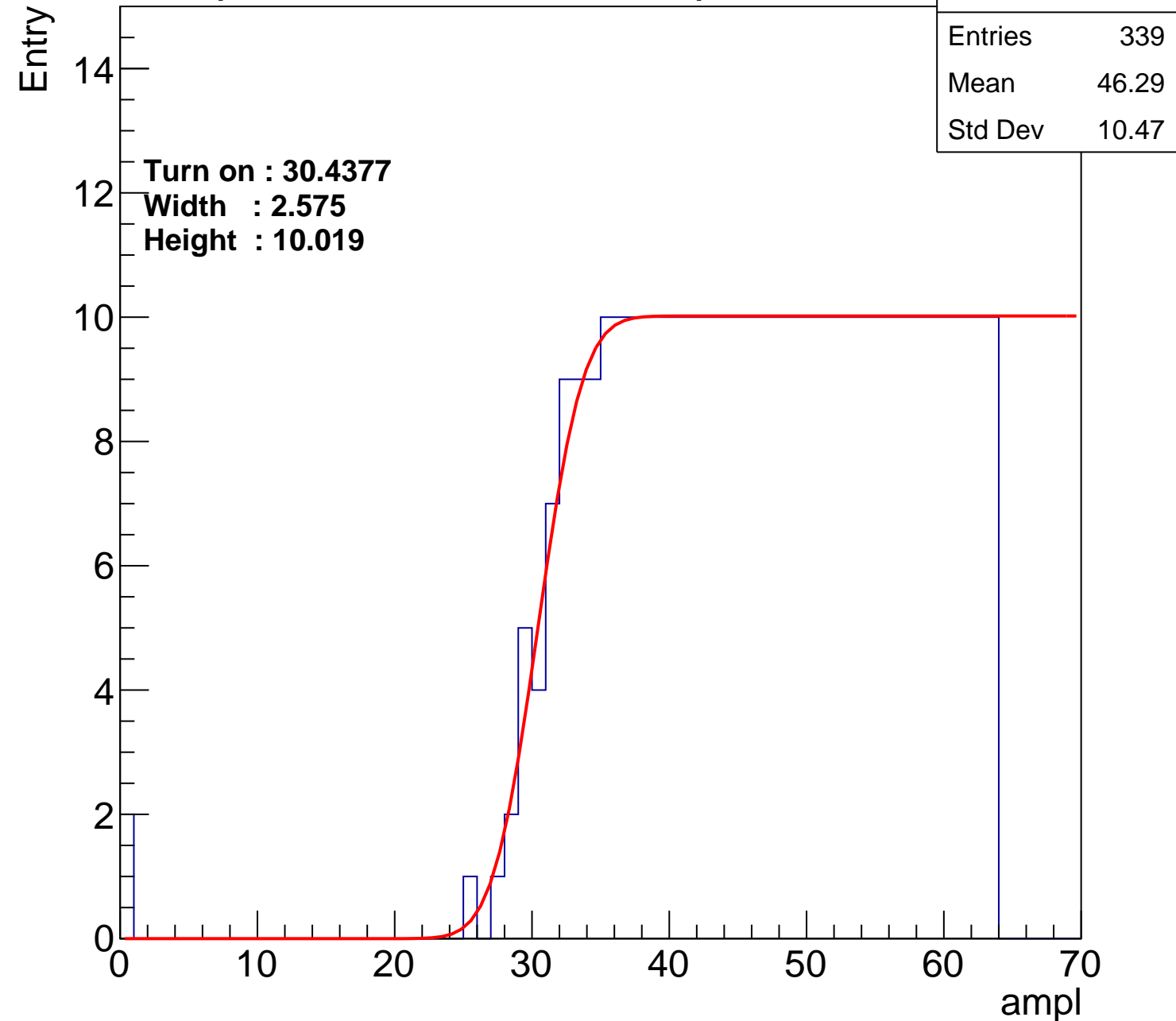
**Width : 2.575**

**Height : 10.019**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch94

calib\_packv5\_042523\_0143.root, FC#9, port A1

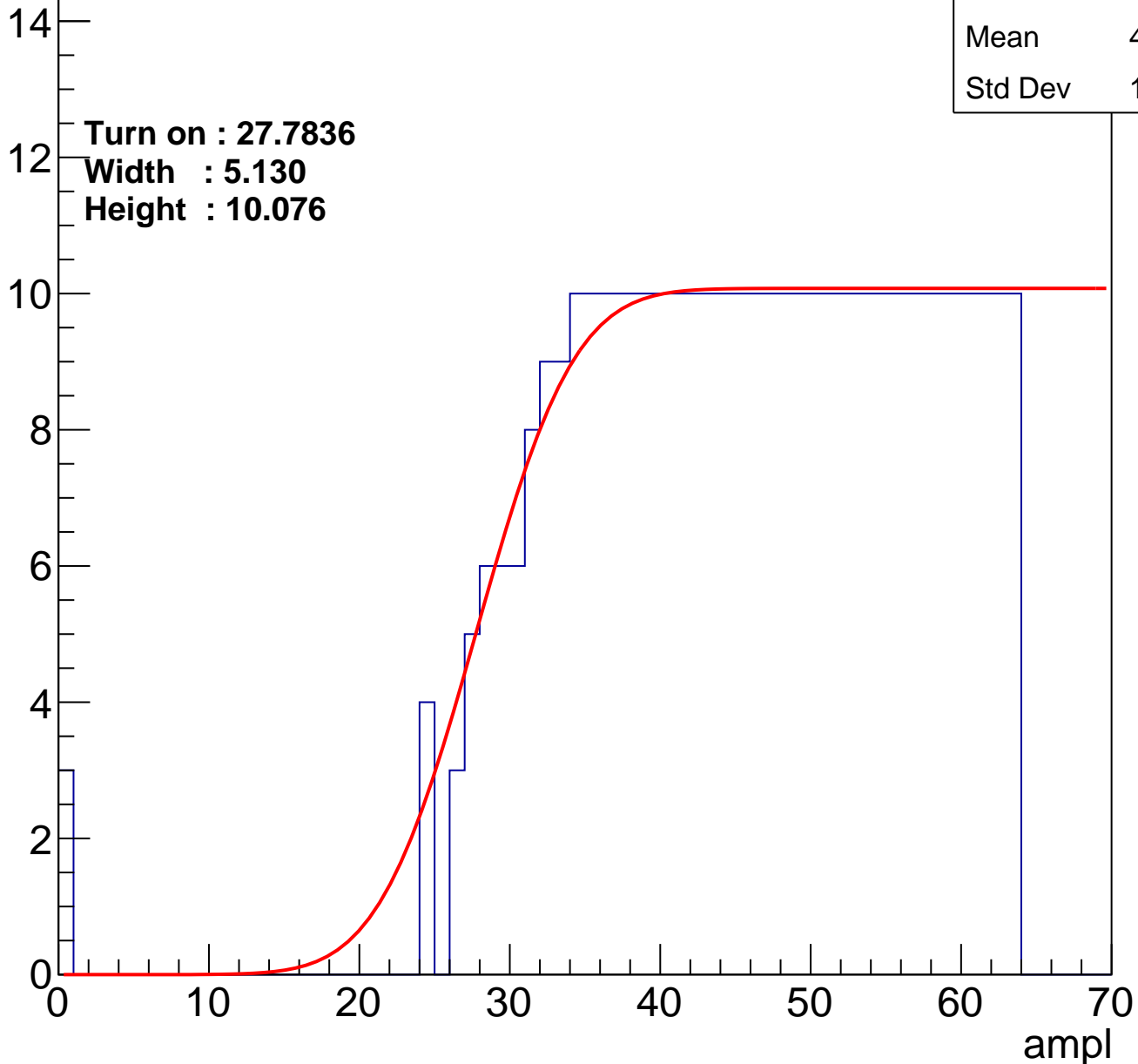
Entries	359
Mean	45.16
Std Dev	11.28

Turn on : 27.7836

Width : 5.130

Height : 10.076

Entry





# B0L001S, U24-ch95

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	365
Mean	44.67
Std Dev	11.99

Turn on : 28.1662

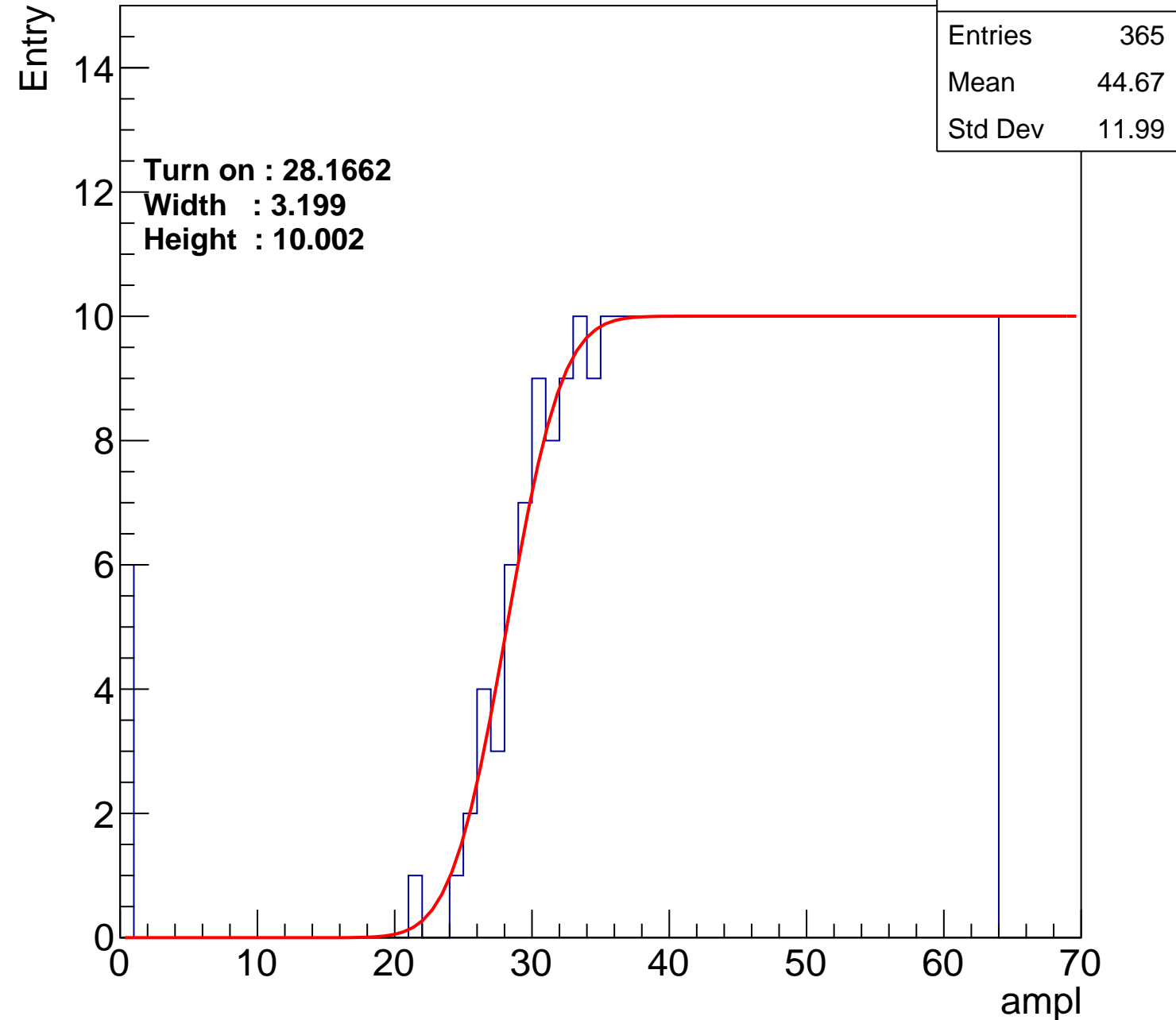
Width : 3.199

Height : 10.002

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch96

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	351
Mean	45.77
Std Dev	10.55

**Turn on : 29.5400**

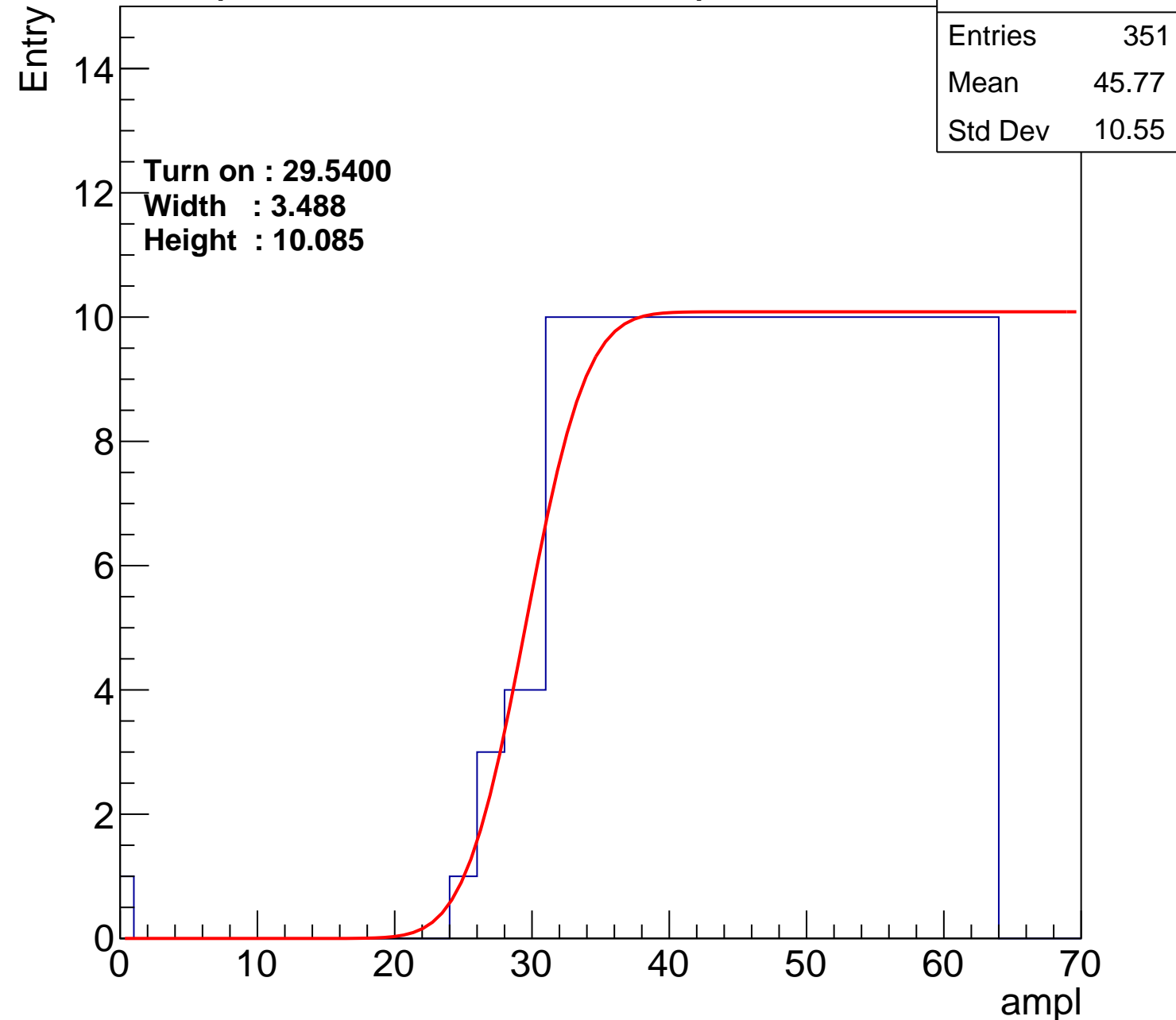
**Width : 3.488**

**Height : 10.085**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch97

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	361
Mean	45.07
Std Dev	11.32

**Turn on : 28.1904**

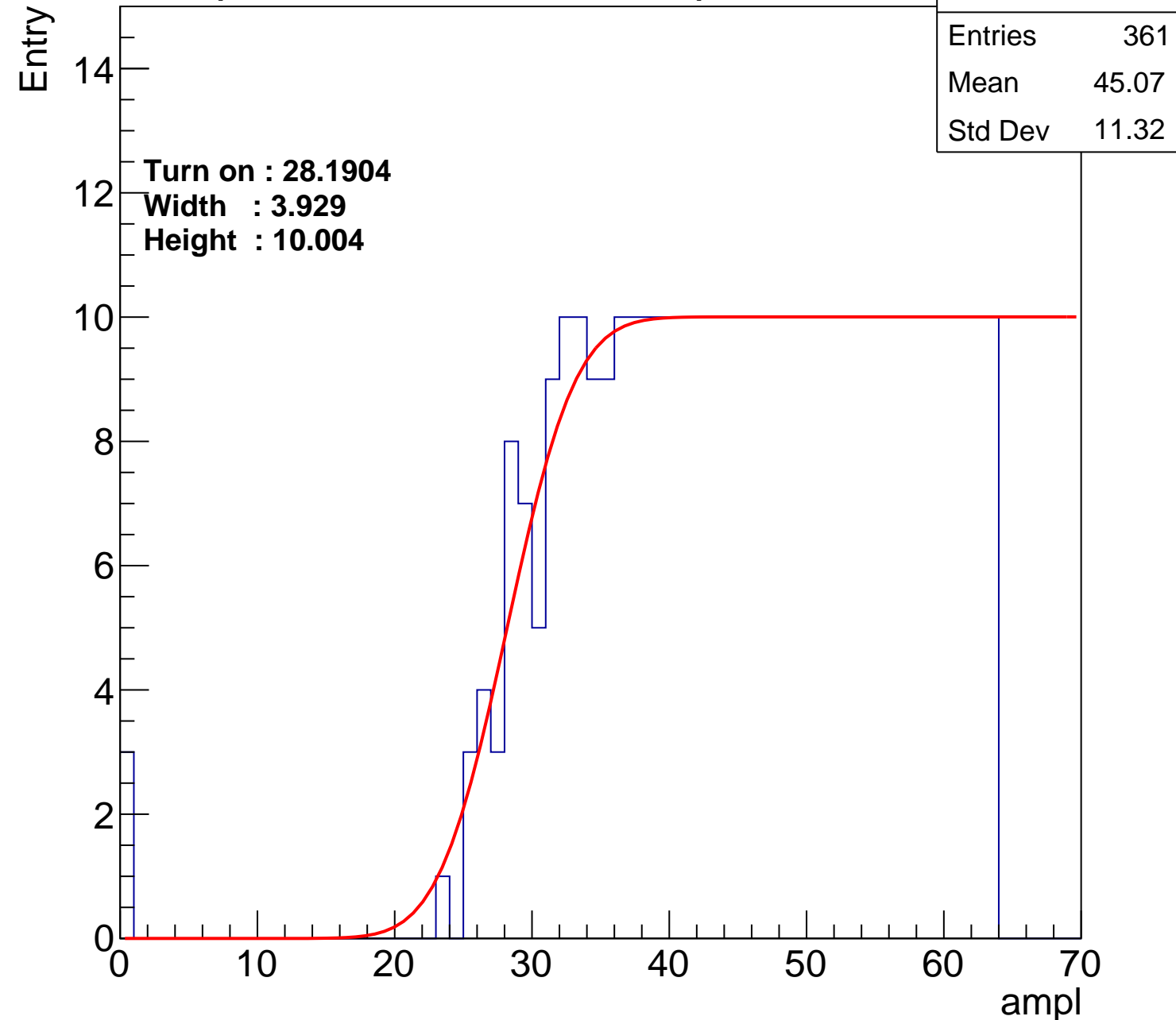
**Width : 3.929**

**Height : 10.004**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch98

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	350
Mean	45.59
Std Dev	11.09

Turn on : 29.4155

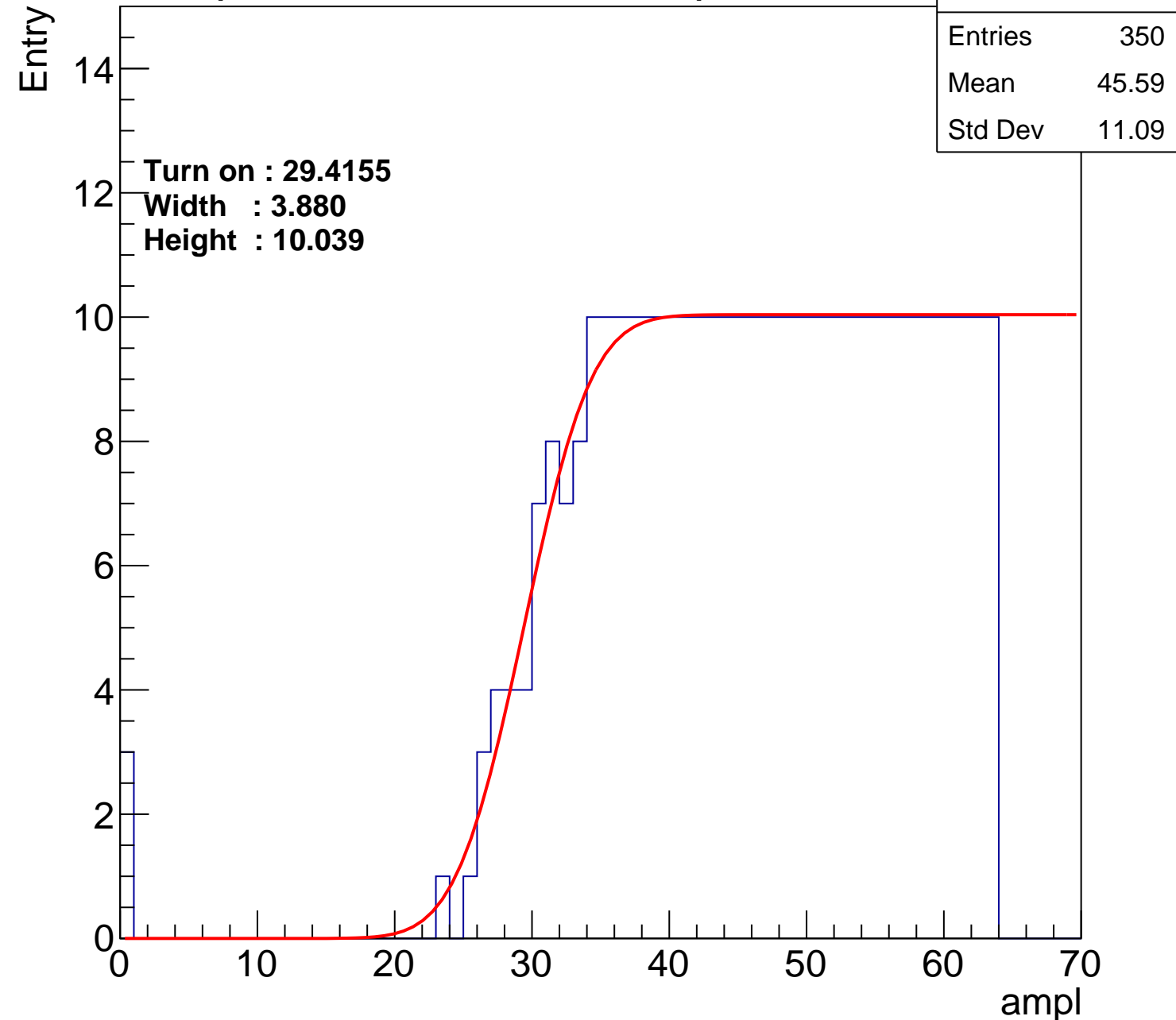
Width : 3.880

Height : 10.039

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch99

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	353
Mean	45.6
Std Dev	10.81

**Turn on : 29.4459**

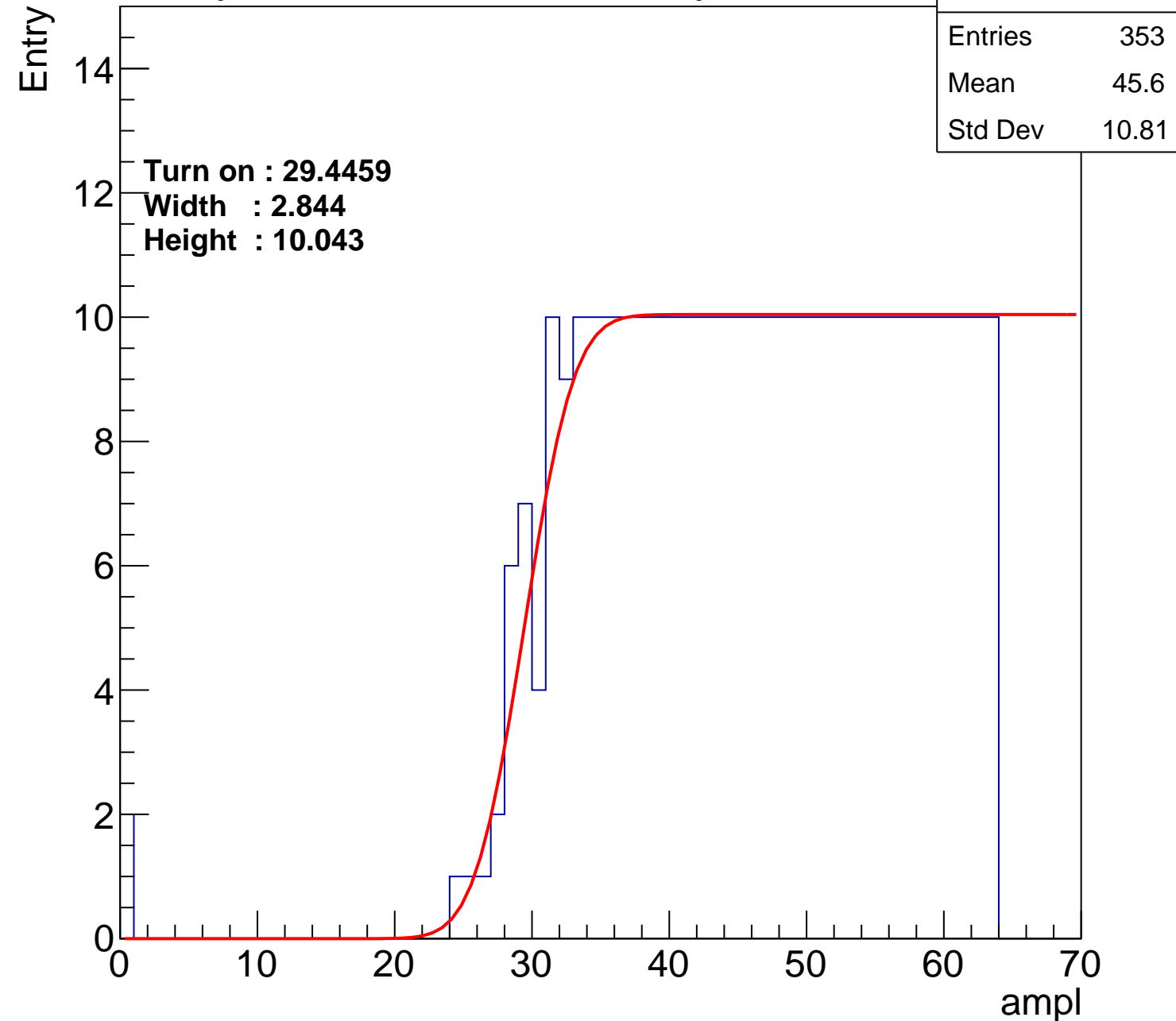
**Width : 2.844**

**Height : 10.043**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch100

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	374
Mean	44.45
Std Dev	11.69

Turn on : 26.7667

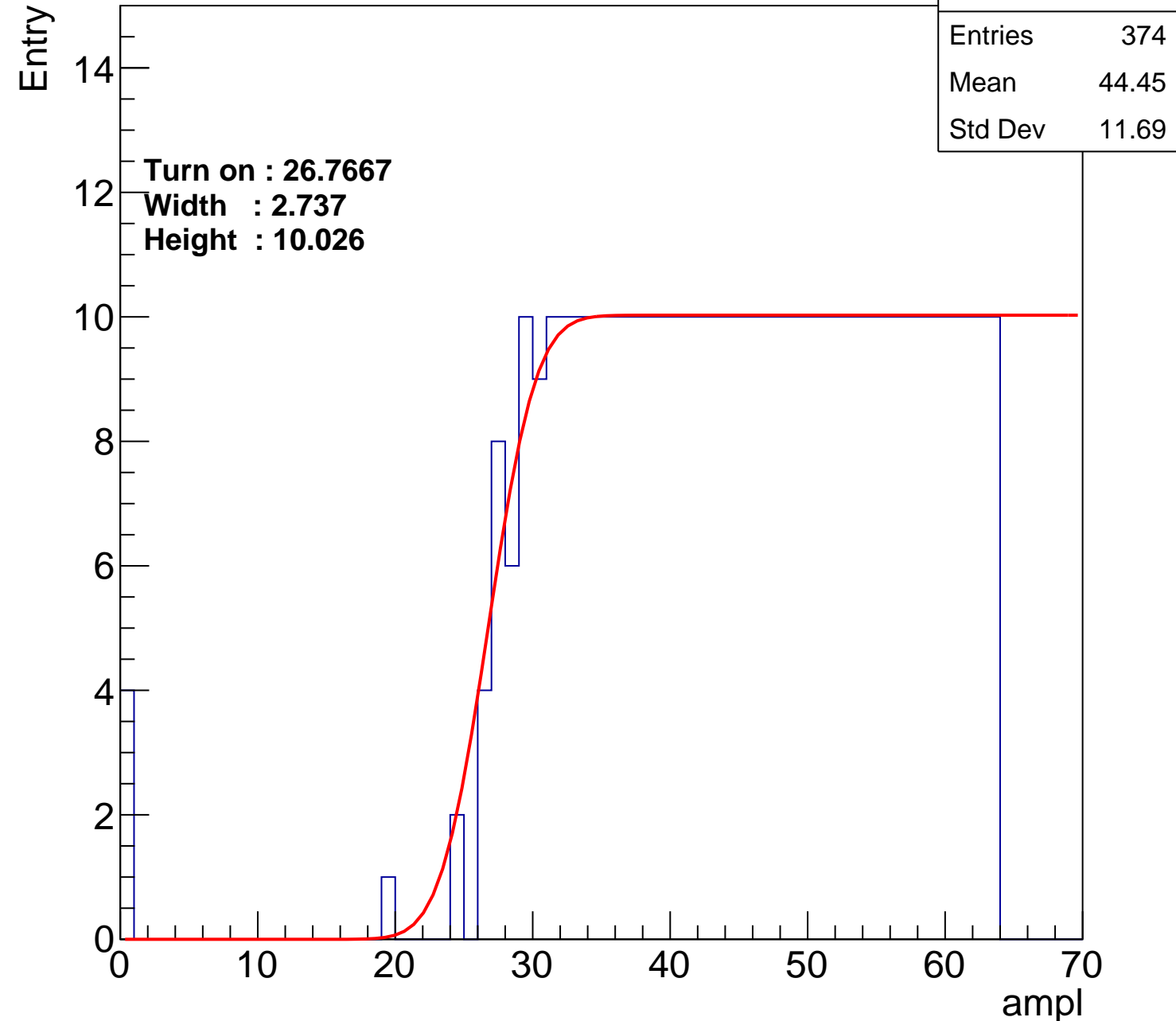
Width : 2.737

Height : 10.026

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch101

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	364
Mean	44.93
Std Dev	11.54

Turn on : 28.4442

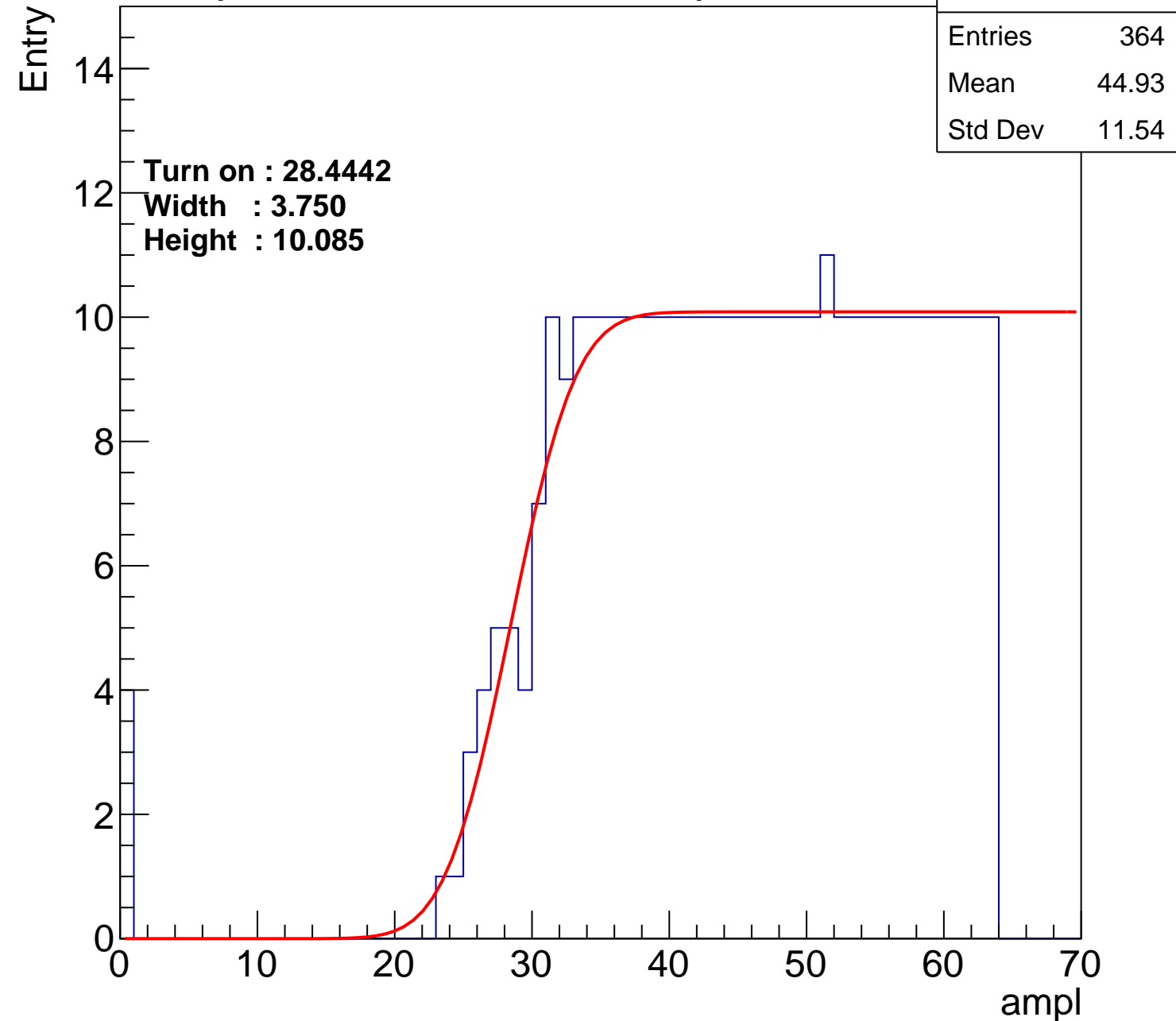
Width : 3.750

Height : 10.085

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch102

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	358
Mean	45.25
Std Dev	11.2

Turn on : 29.7010

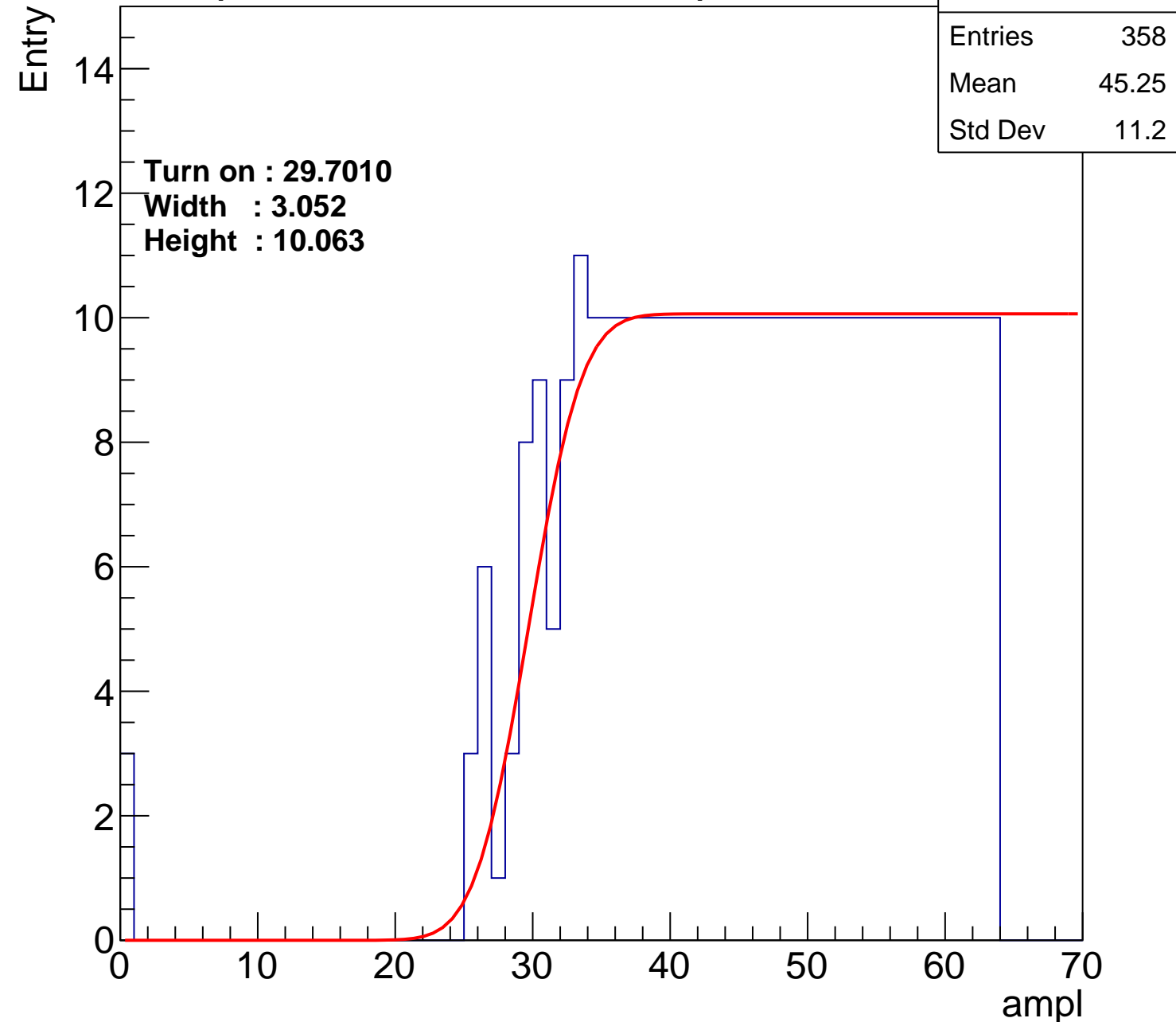
Width : 3.052

Height : 10.063

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U24-ch103

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	354
Mean	45.55
Std Dev	10.75

Turn on : 29.2405

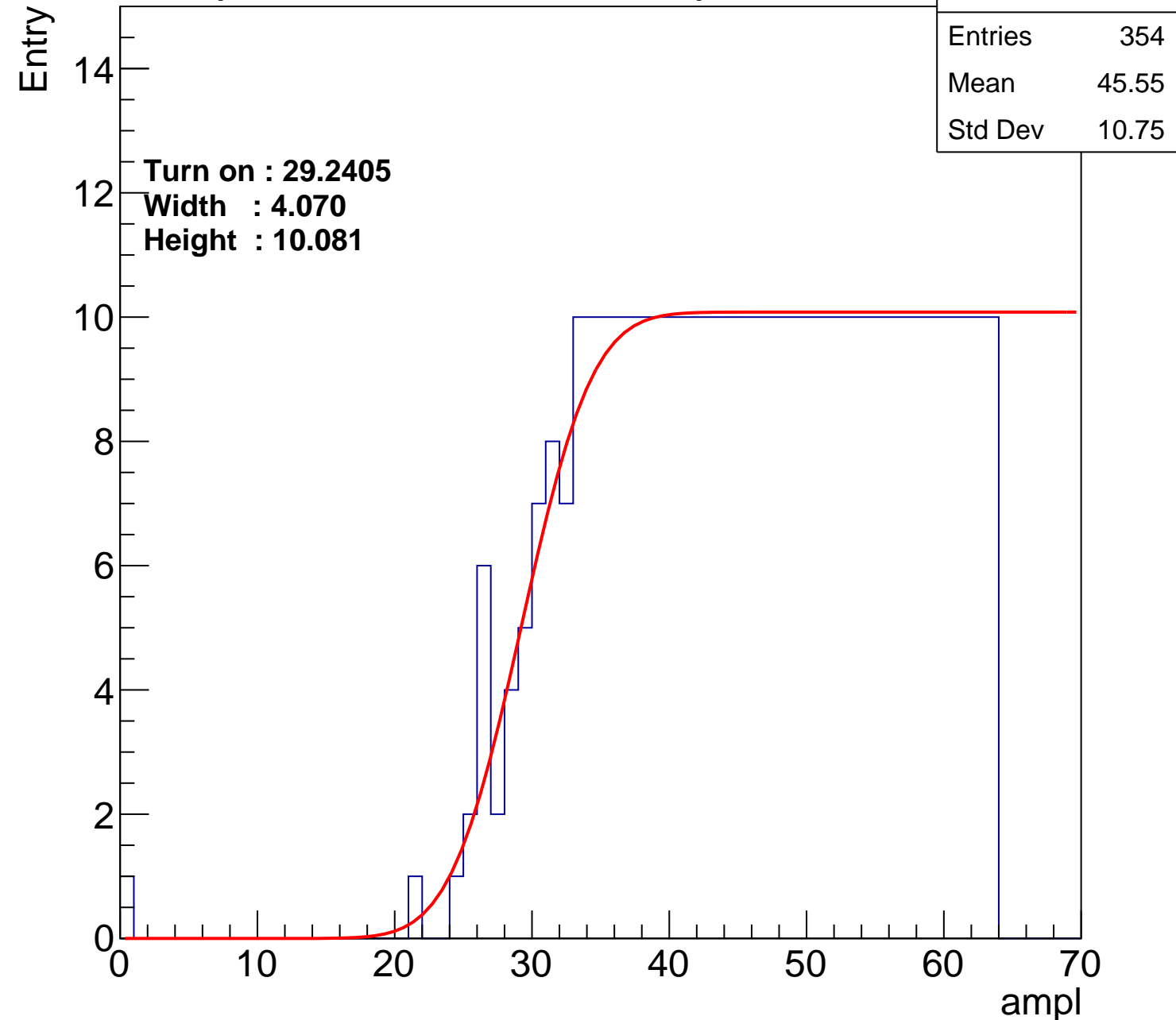
Width : 4.070

Height : 10.081

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch104

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	366
Mean	44.69
Std Dev	11.8

Turn on : 28.1991

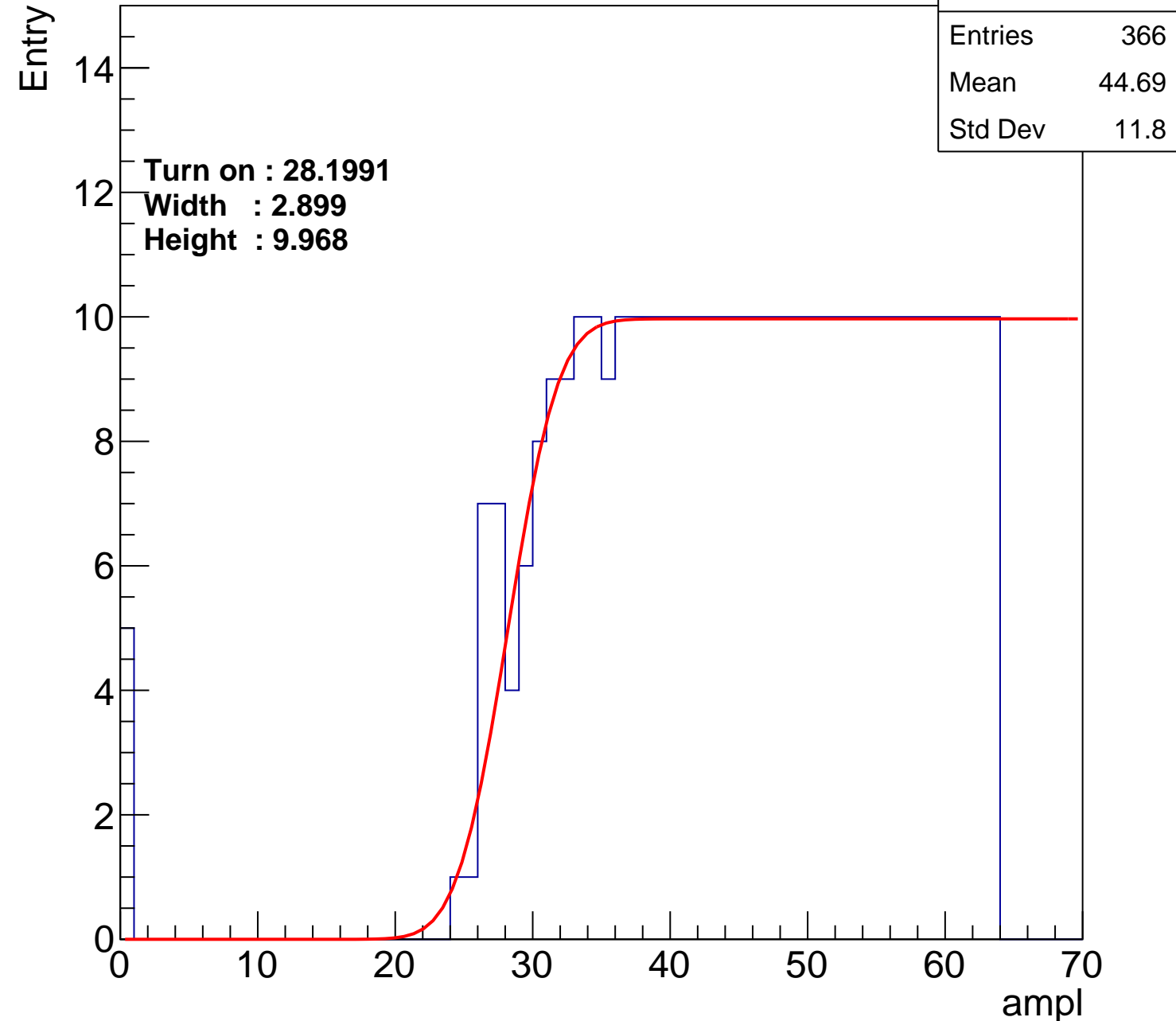
Width : 2.899

Height : 9.968

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch105

calib\_packv5\_042523\_0143.root, FC#9, port A1

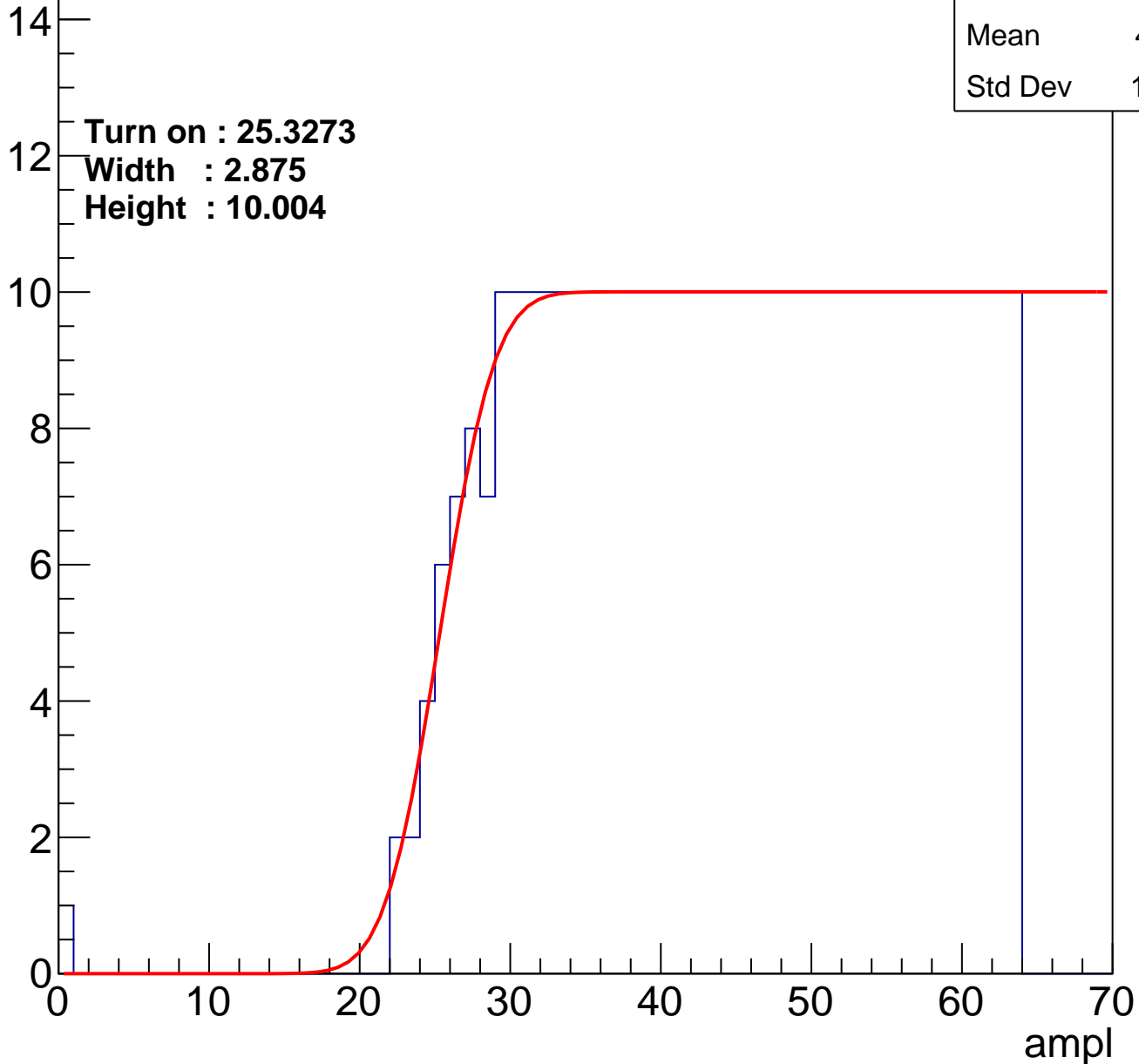
Entries	387
Mean	44.01
Std Dev	11.48

**Turn on : 25.3273**

**Width : 2.875**

**Height : 10.004**

Entry



# B0L001S, U24-ch106

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	349
Mean	45.79
Std Dev	10.73

**Turn on : 29.1839**

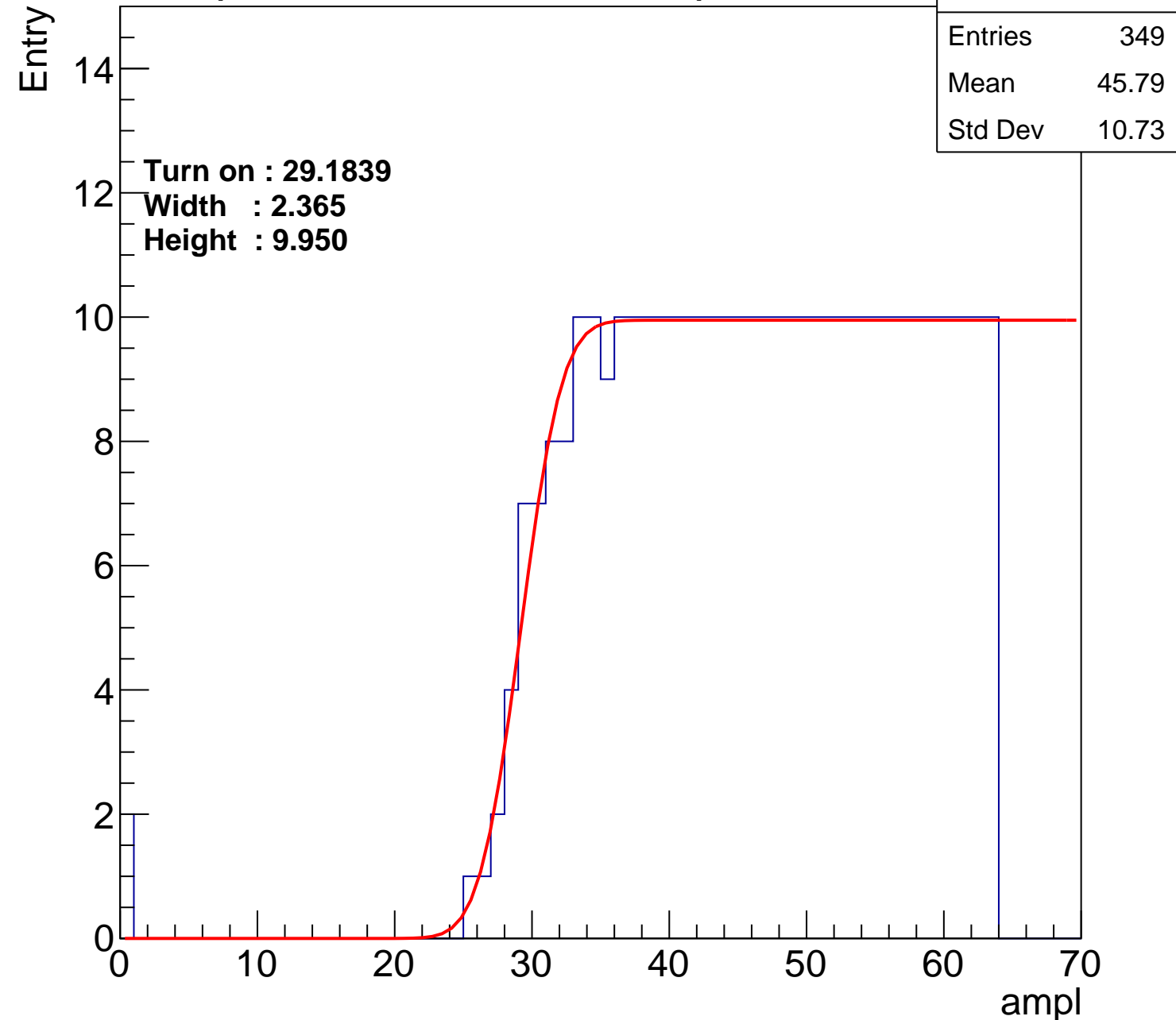
**Width : 2.365**

**Height : 9.950**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch107

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	361
Mean	45.11
Std Dev	11.35

**Turn on : 28.6003**

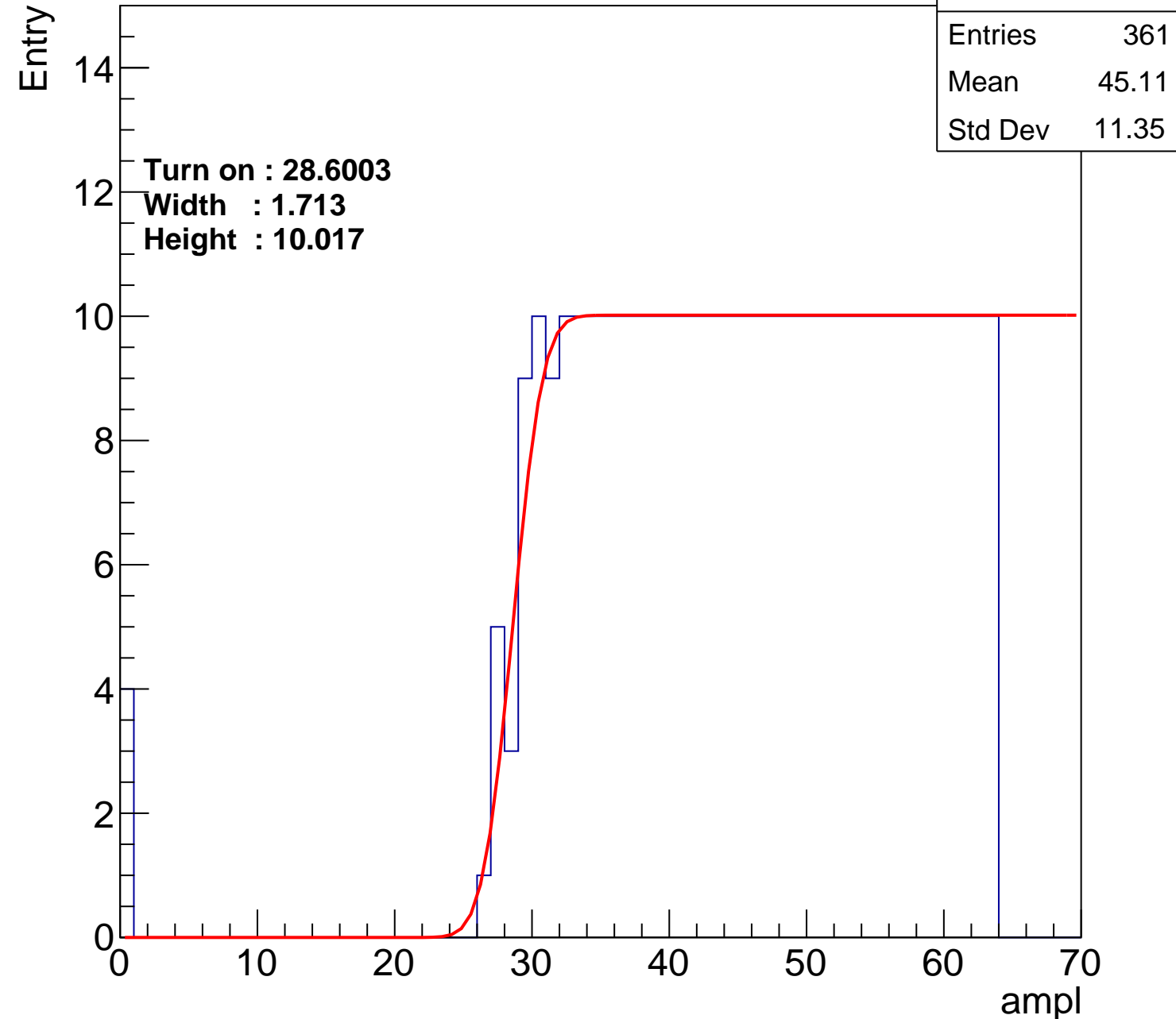
**Width : 1.713**

**Height : 10.017**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch108

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	345
Mean	45.64
Std Dev	11.47

Turn on : 29.8419

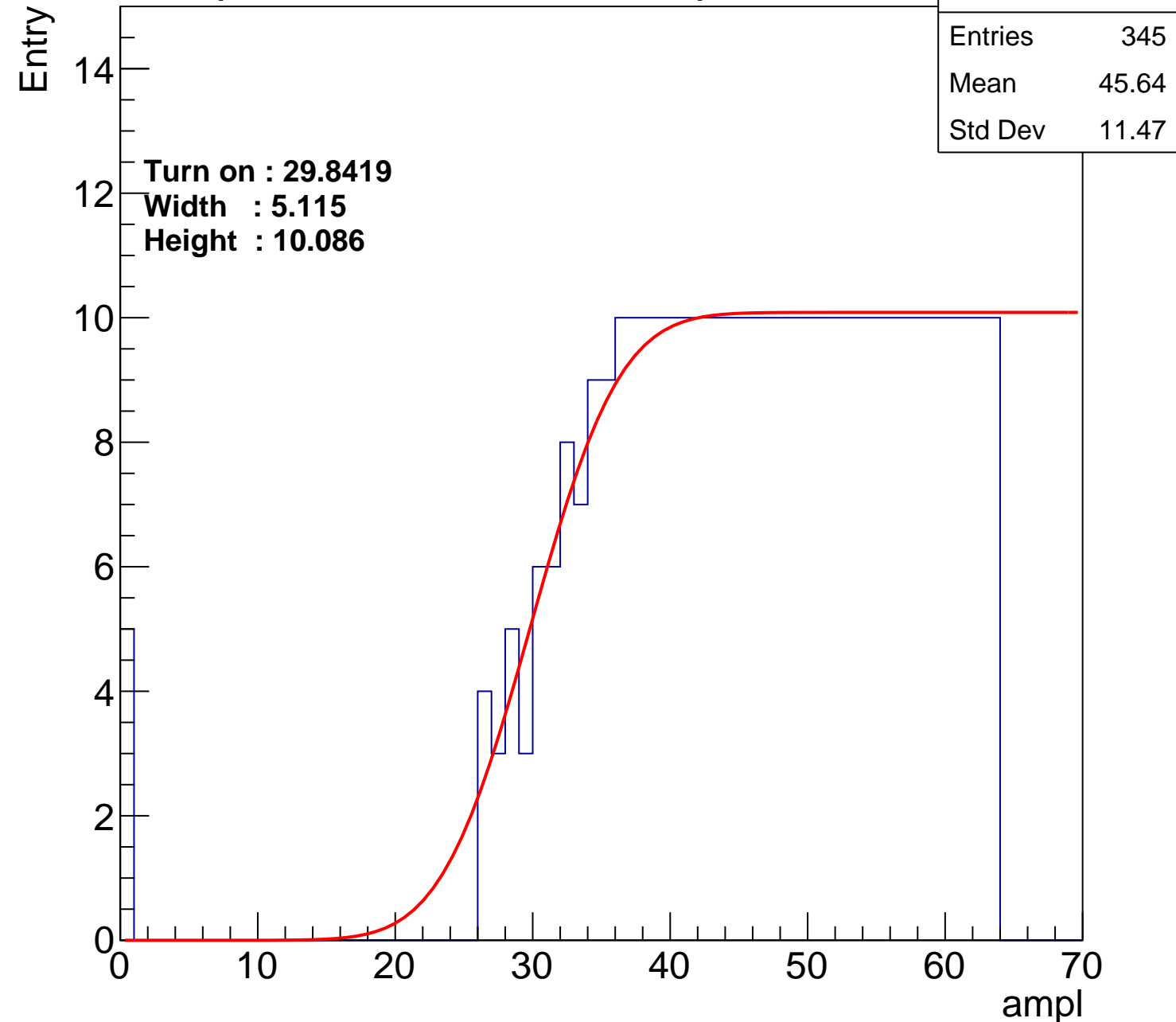
Width : 5.115

Height : 10.086

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch109

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	358
Mean	45.26
Std Dev	11.18

**Turn on : 28.4897**

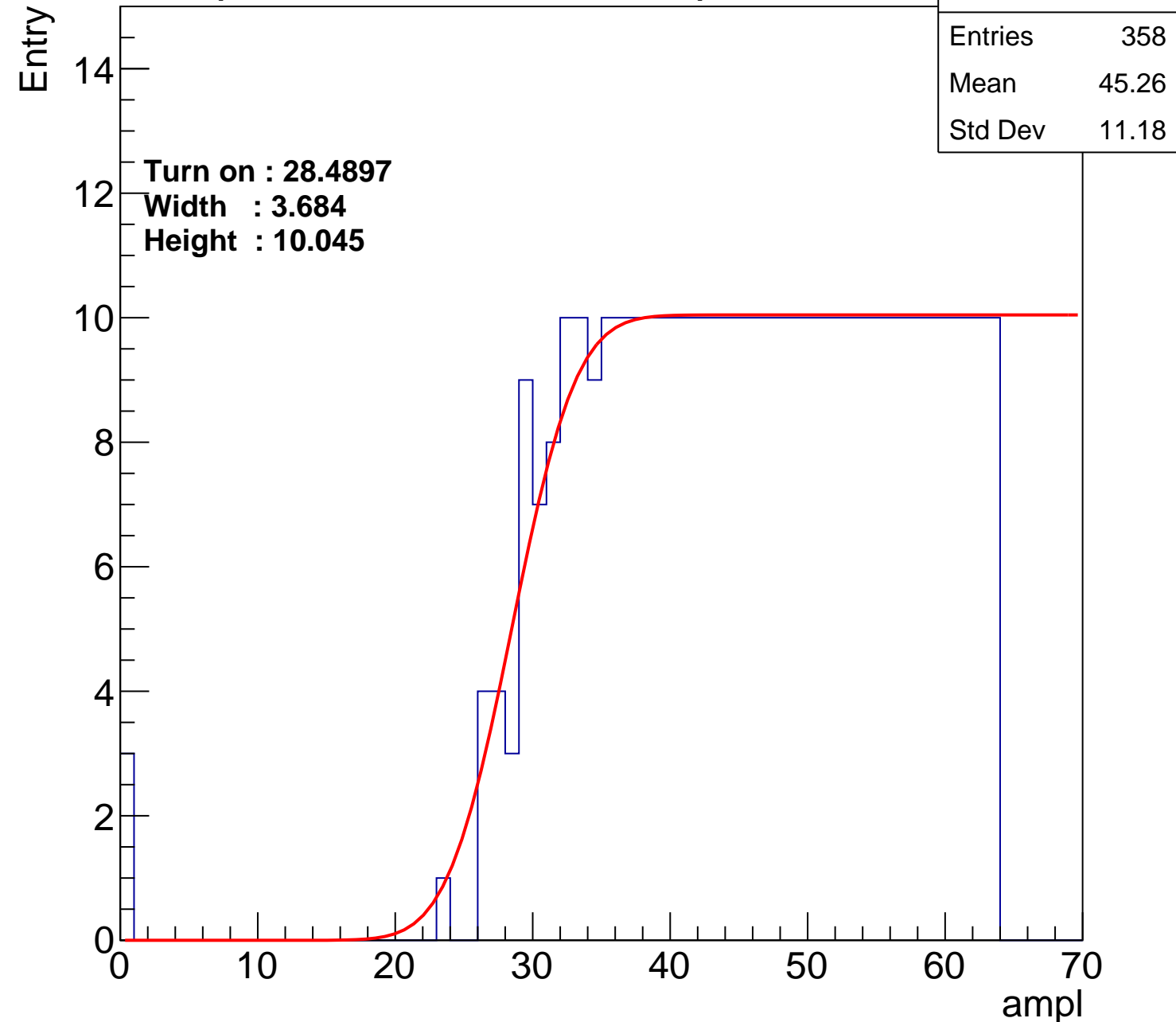
**Width : 3.684**

**Height : 10.045**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch110

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	376
Mean	44.39
Std Dev	11.62

Turn on : 27.1801

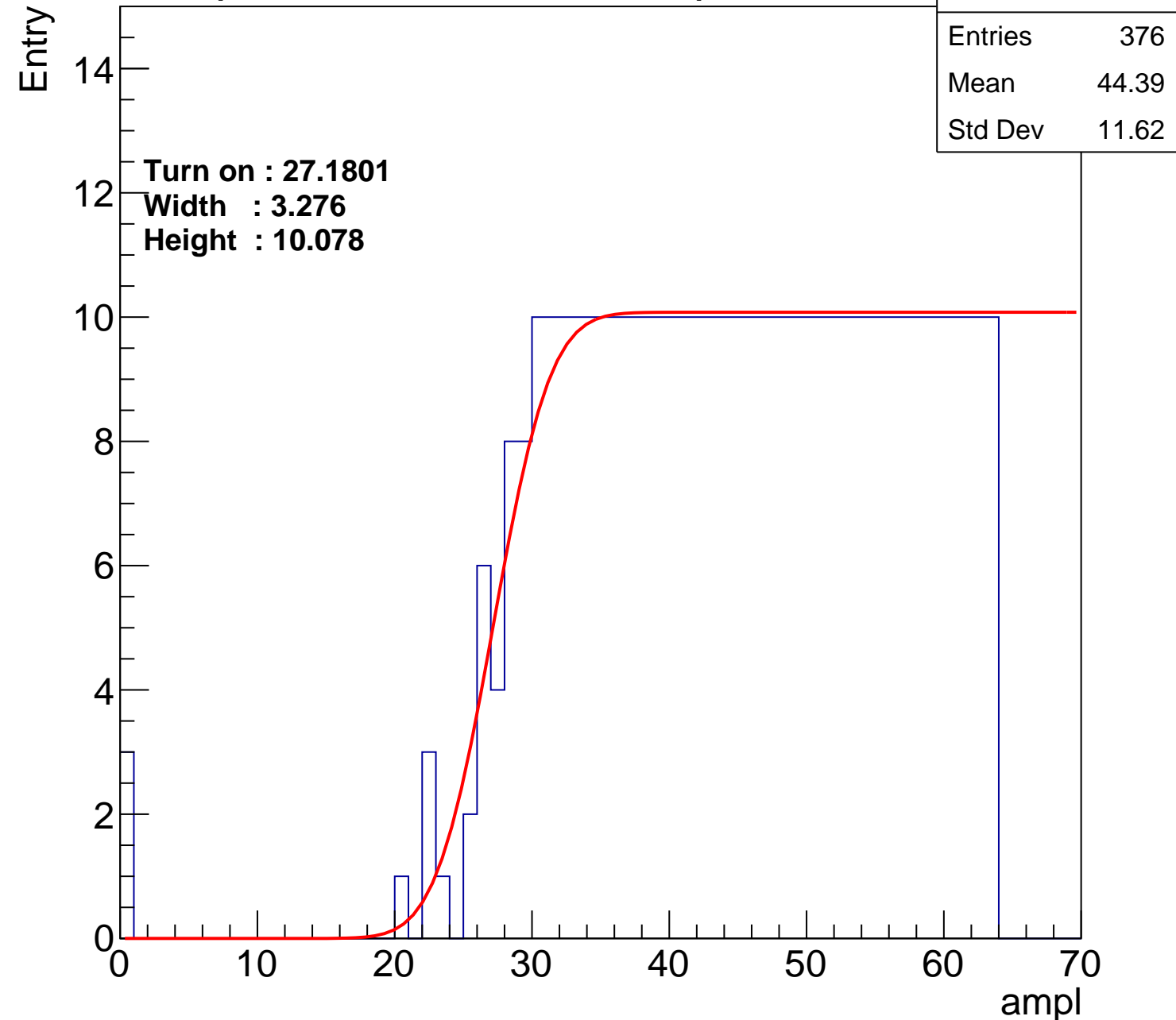
Width : 3.276

Height : 10.078

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U24-ch111

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	350
Mean	45.48
Std Dev	11.46

Turn on : 29.5716

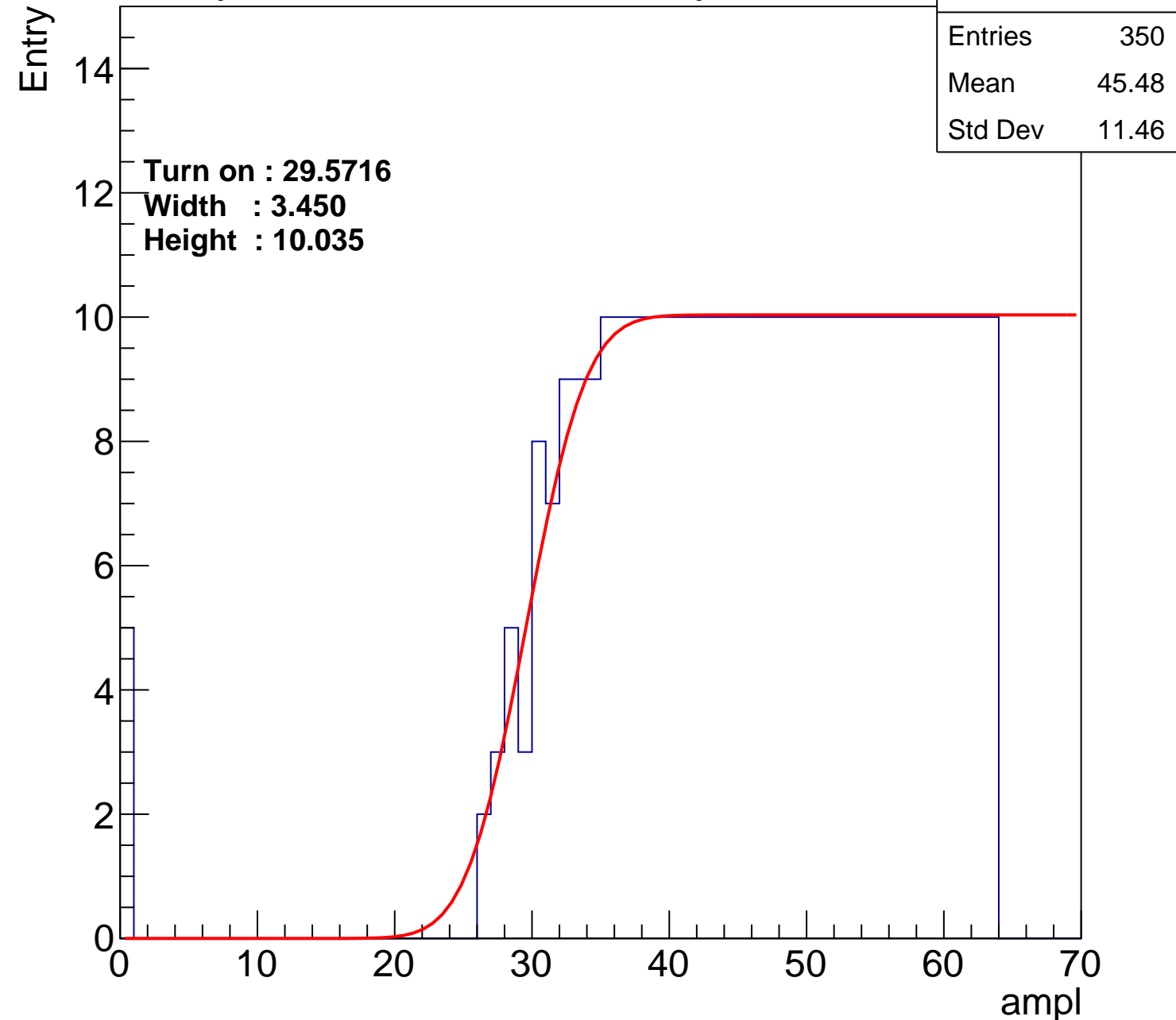
Width : 3.450

Height : 10.035

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch112

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	352
Mean	45.49
Std Dev	11.26

**Turn on : 29.0573**

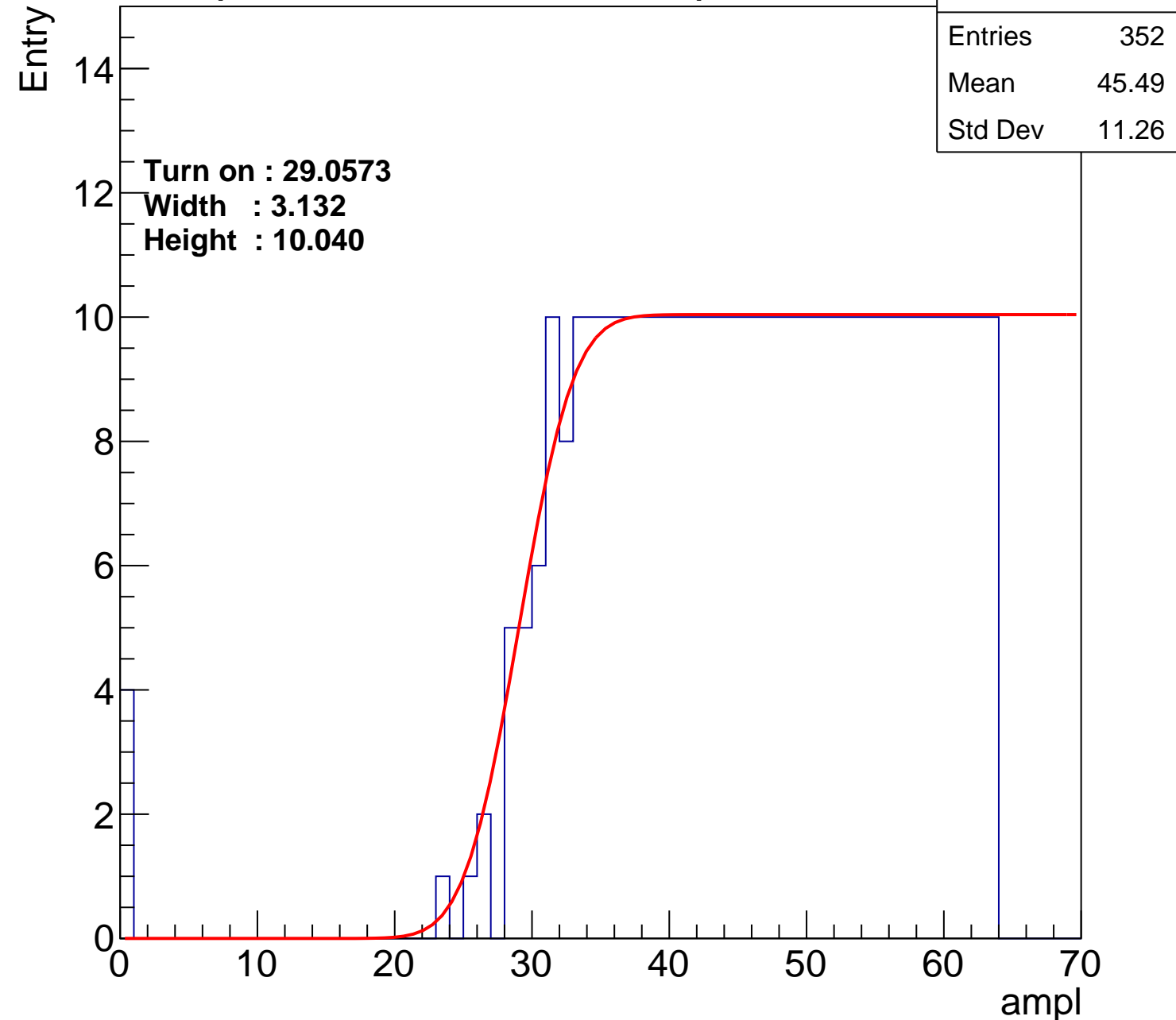
**Width : 3.132**

**Height : 10.040**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch113

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	361
Mean	45.08
Std Dev	11.46

Turn on : 28.8175

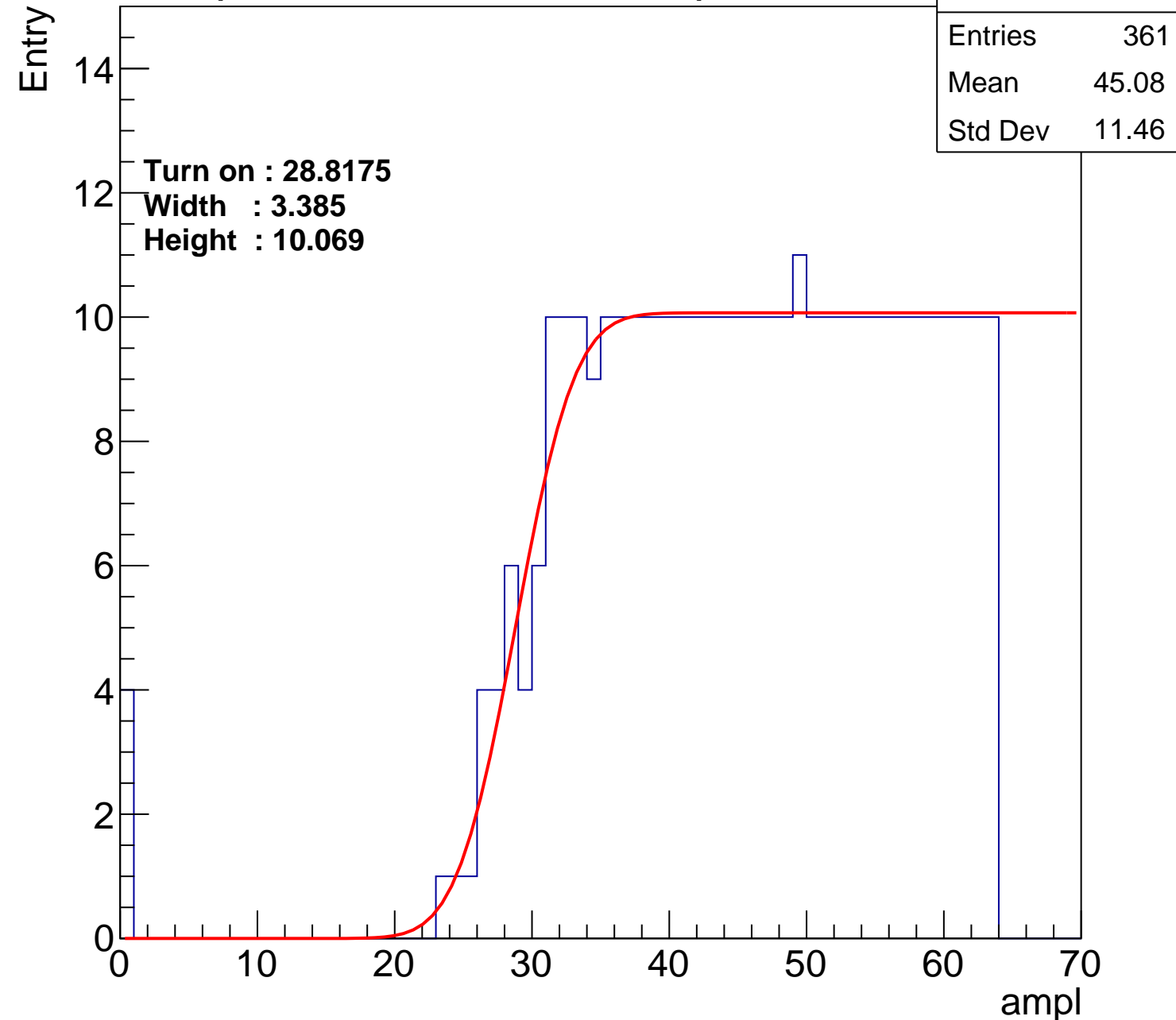
Width : 3.385

Height : 10.069

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch114

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	383
Mean	43.54
Std Dev	13

Turn on : 27.0001

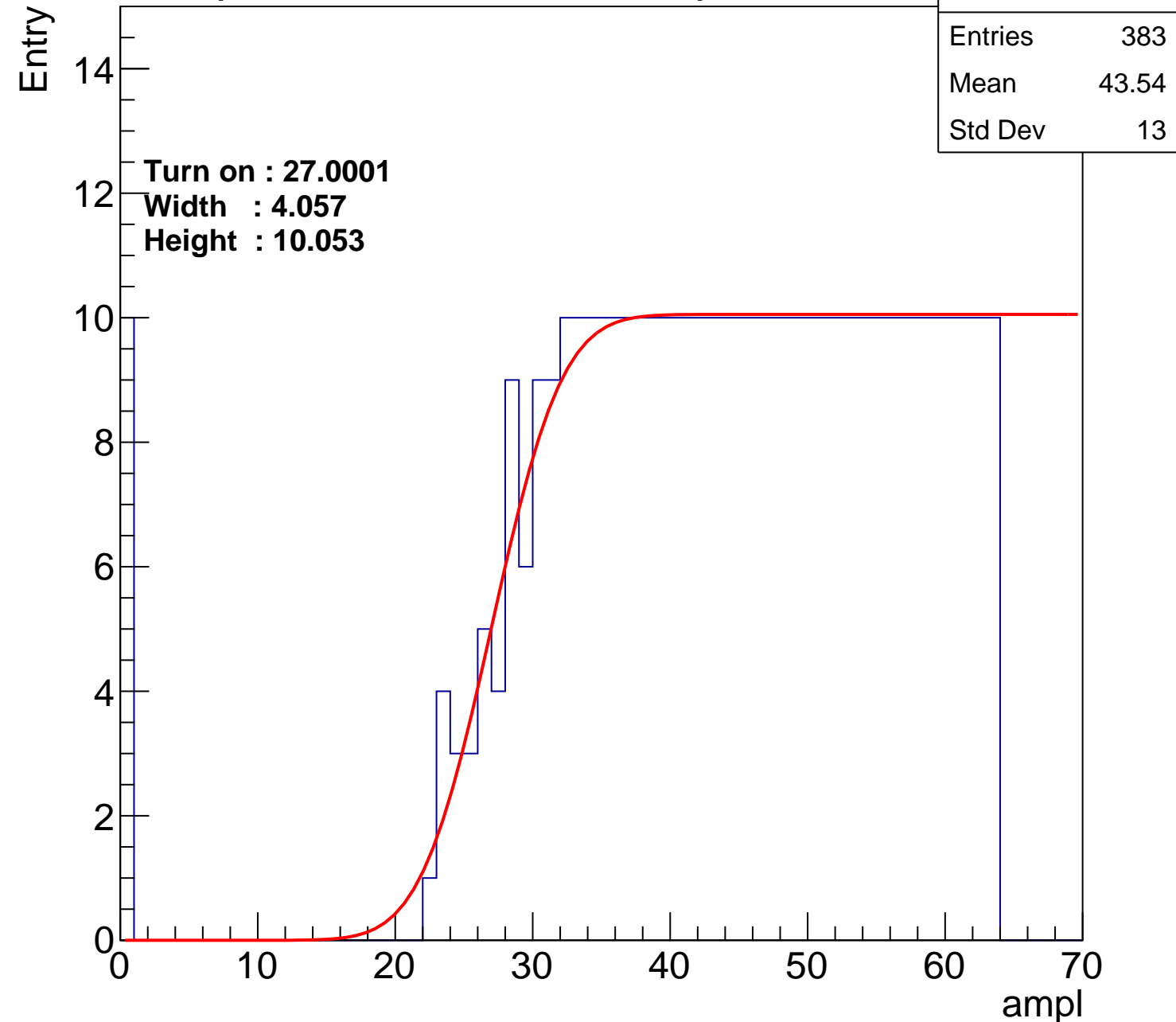
Width : 4.057

Height : 10.053

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch115

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	345
Mean	45.97
Std Dev	10.65

Turn on : 30.9820

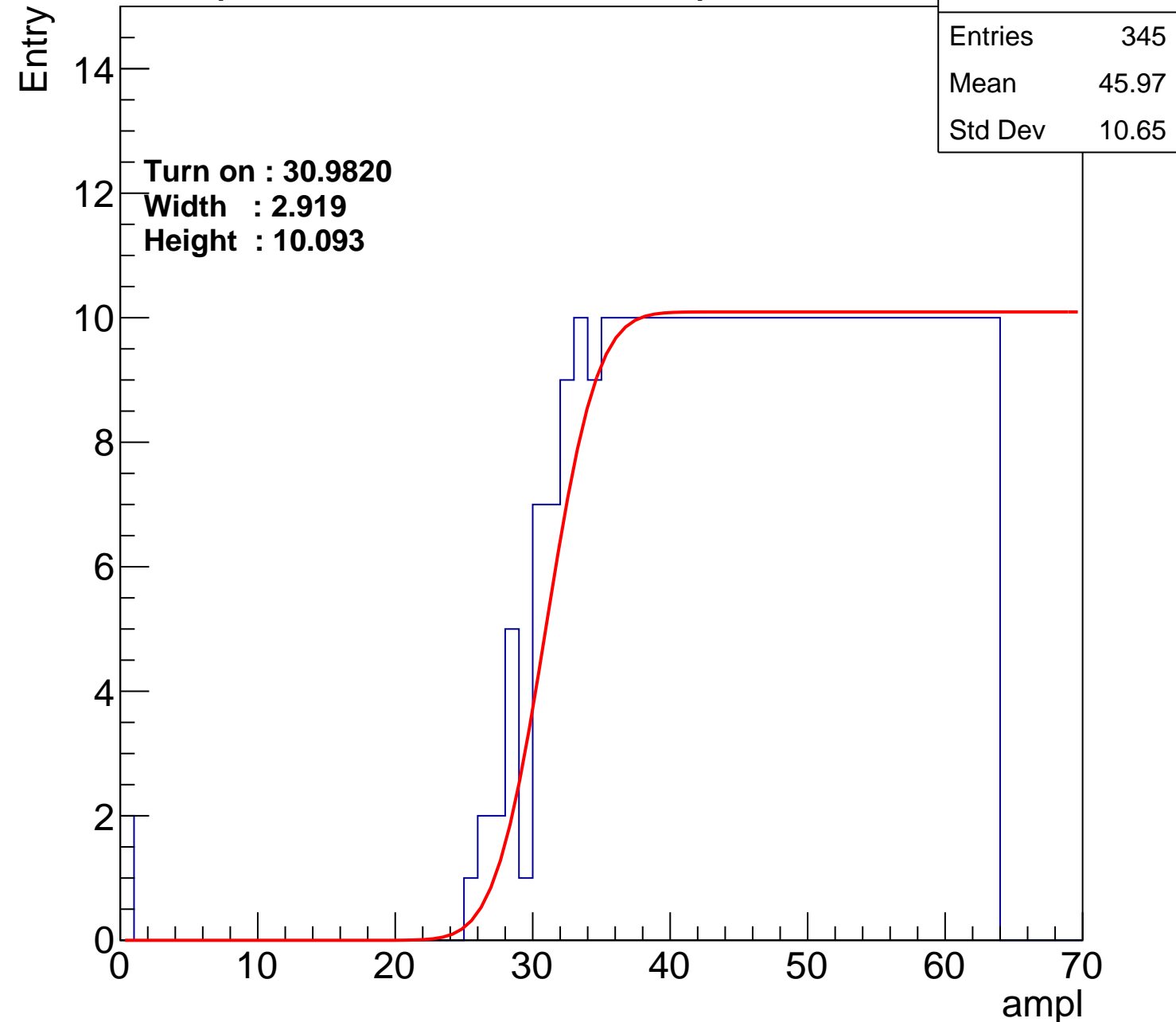
Width : 2.919

Height : 10.093

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch116

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	379
Mean	44.33
Std Dev	11.46

Turn on : 26.6212

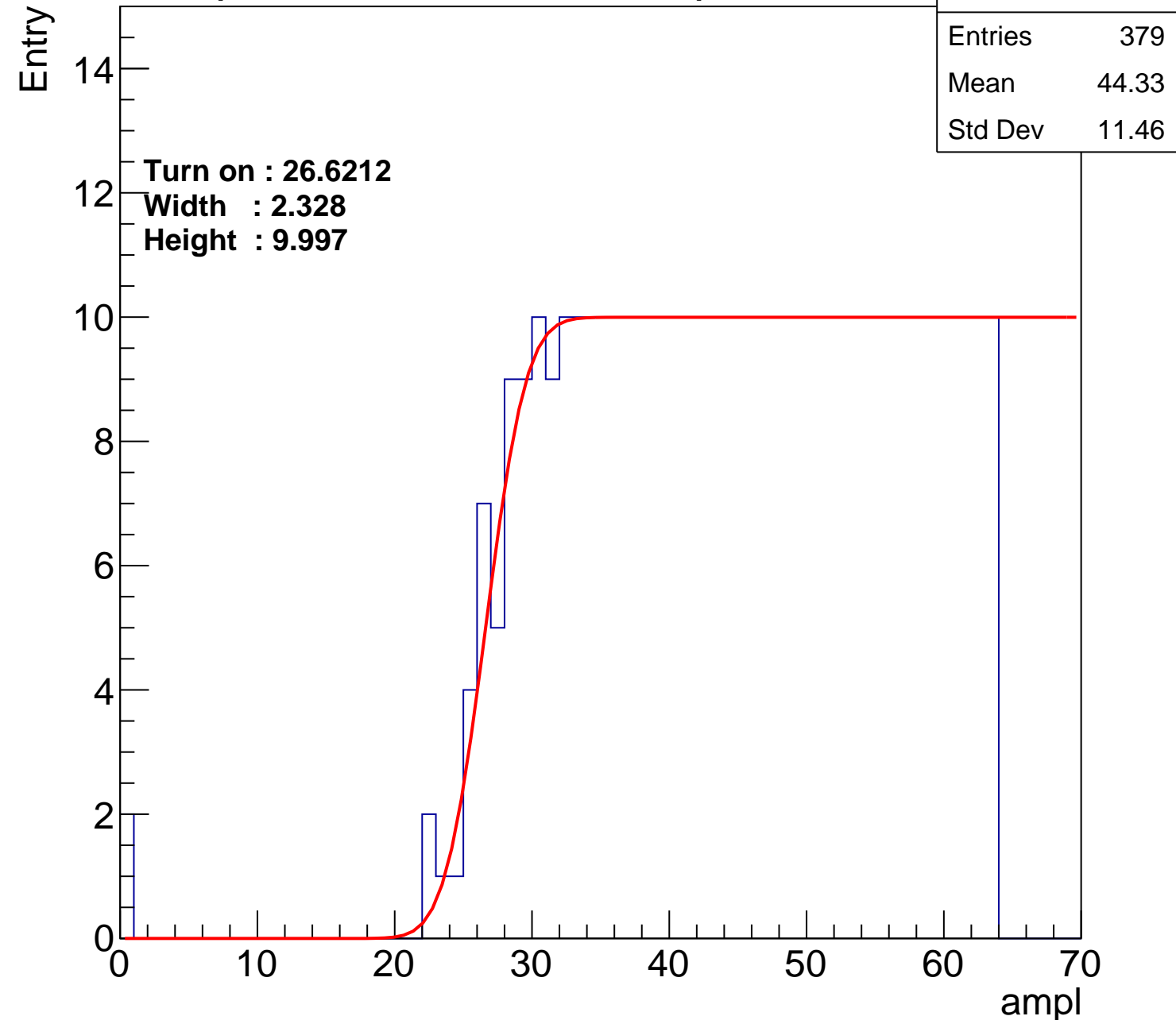
Width : 2.328

Height : 9.997

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch117

calib\_packv5\_042523\_0143.root, FC#9, port A1

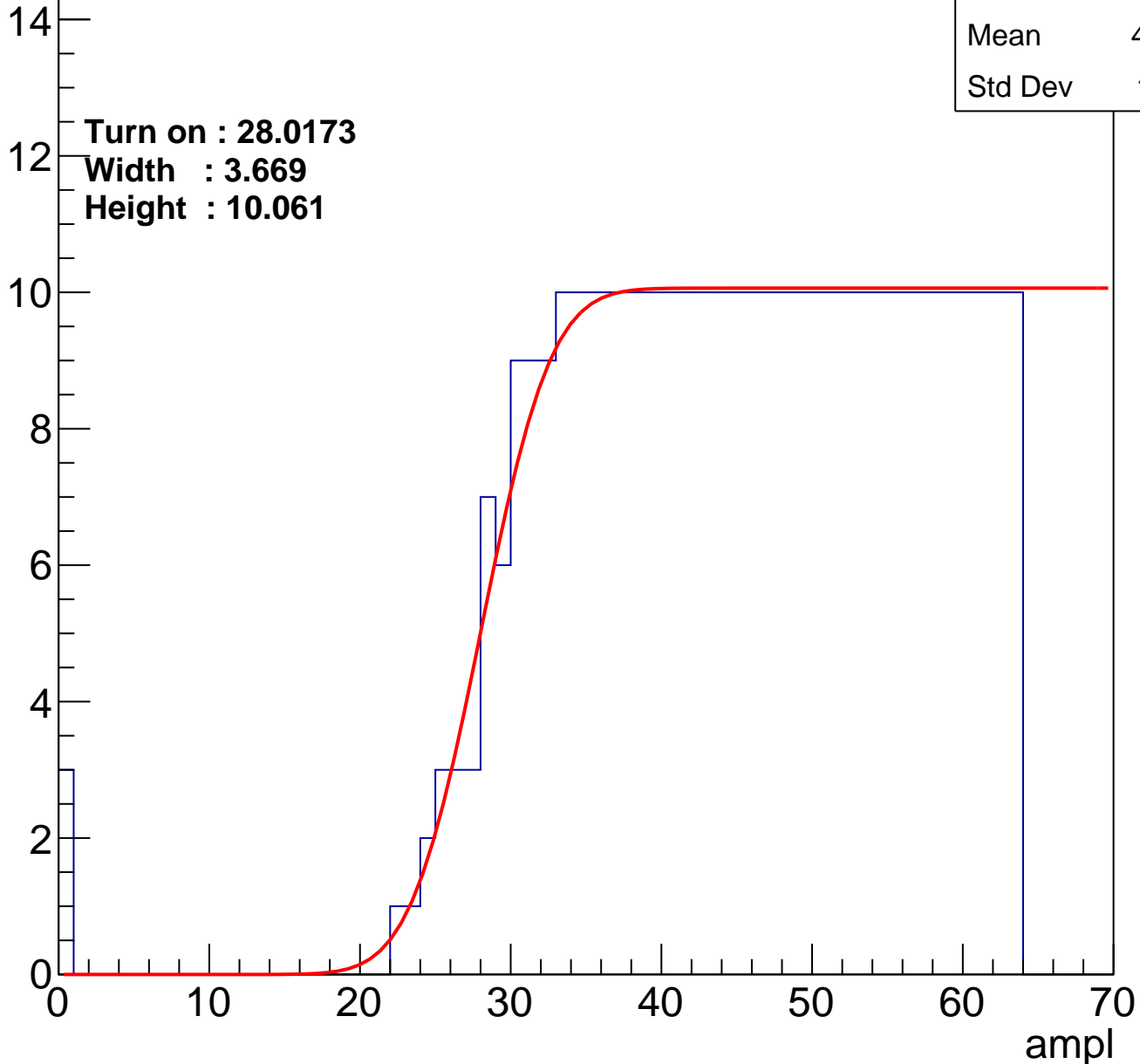
Entries	366
Mean	44.85
Std Dev	11.41

Turn on : 28.0173

Width : 3.669

Height : 10.061

Entry



# B0L001S, U24-ch118

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	372
Mean	44.52
Std Dev	11.69

**Turn on : 27.8999**

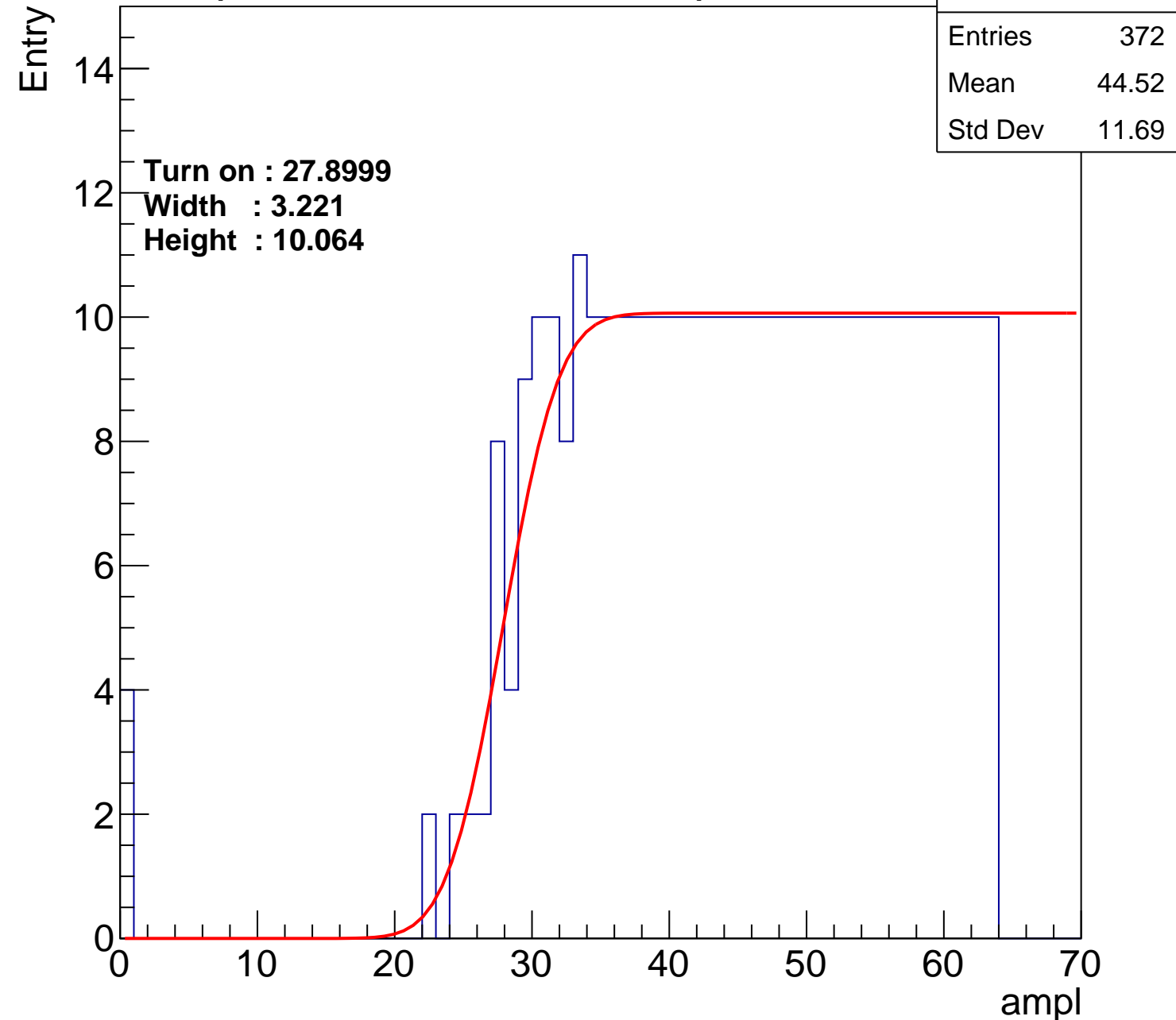
**Width : 3.221**

**Height : 10.064**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L001S, U24-ch119

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	329
Mean	46.24
Std Dev	11.66

Turn on : 32.0690

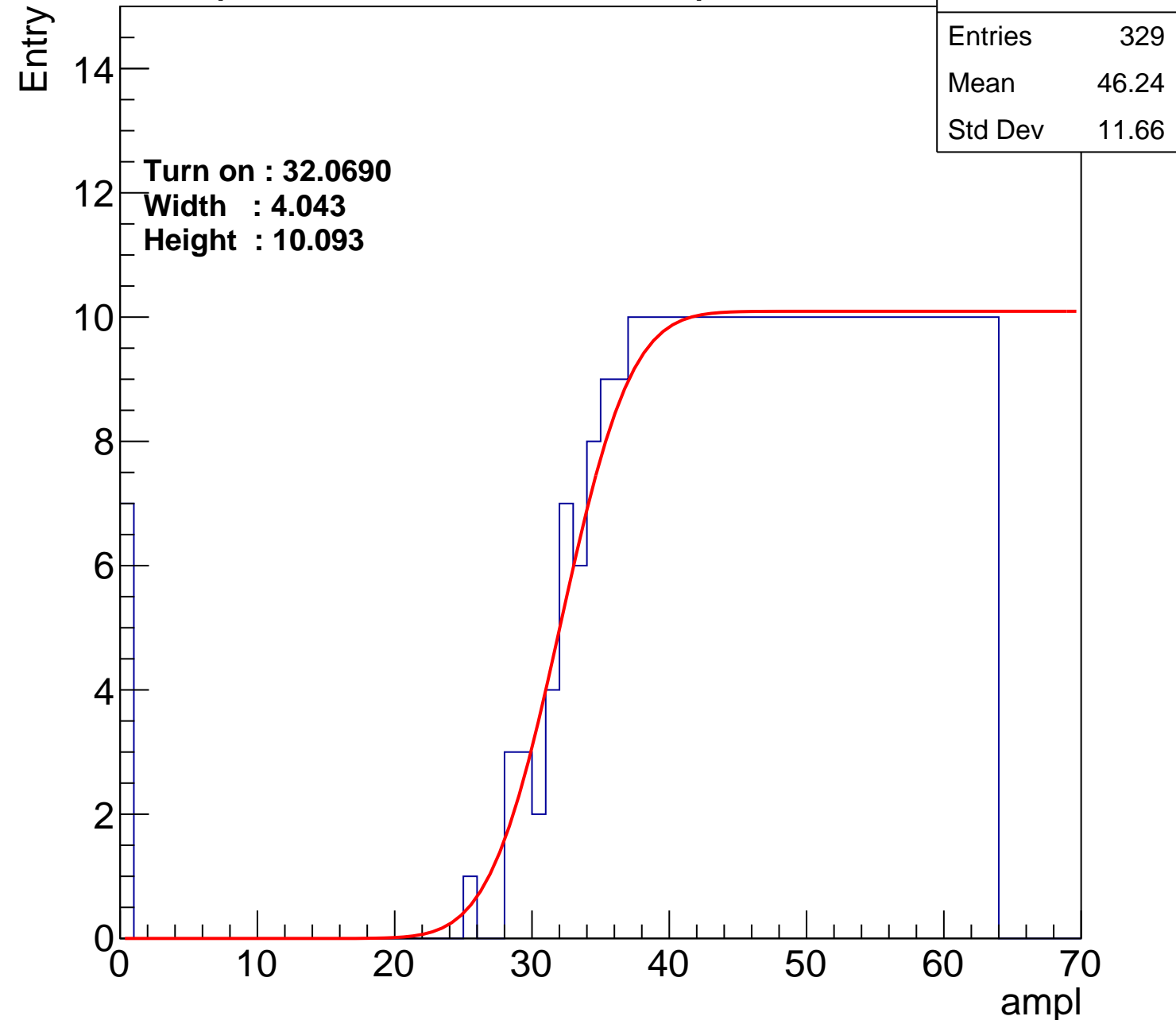
Width : 4.043

Height : 10.093

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch120

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	332
Mean	46.44
Std Dev	10.73

Turn on : 31.3687

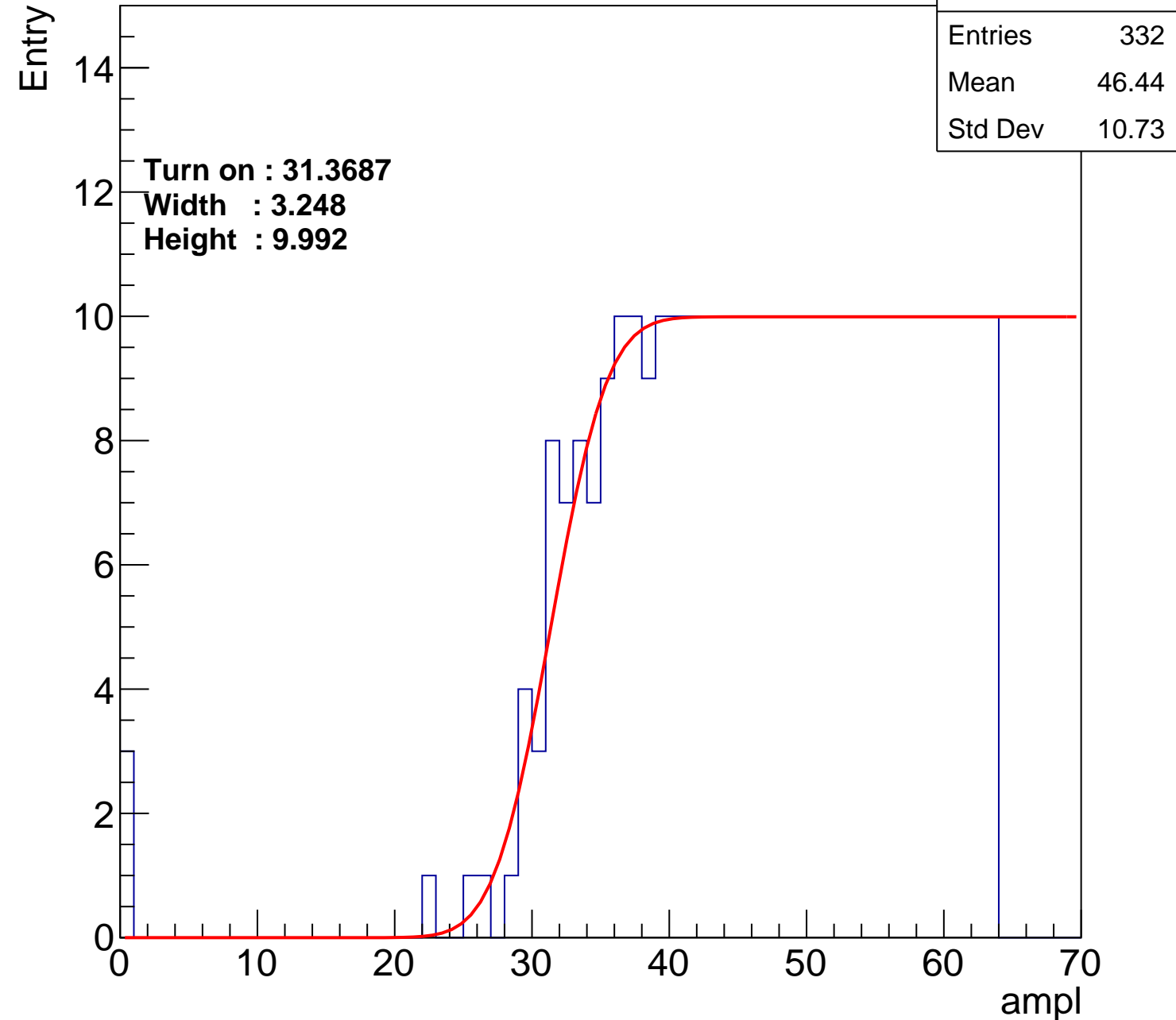
Width : 3.248

Height : 9.992

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch121

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	367
Mean	44.67
Std Dev	11.8

Turn on : 28.1161

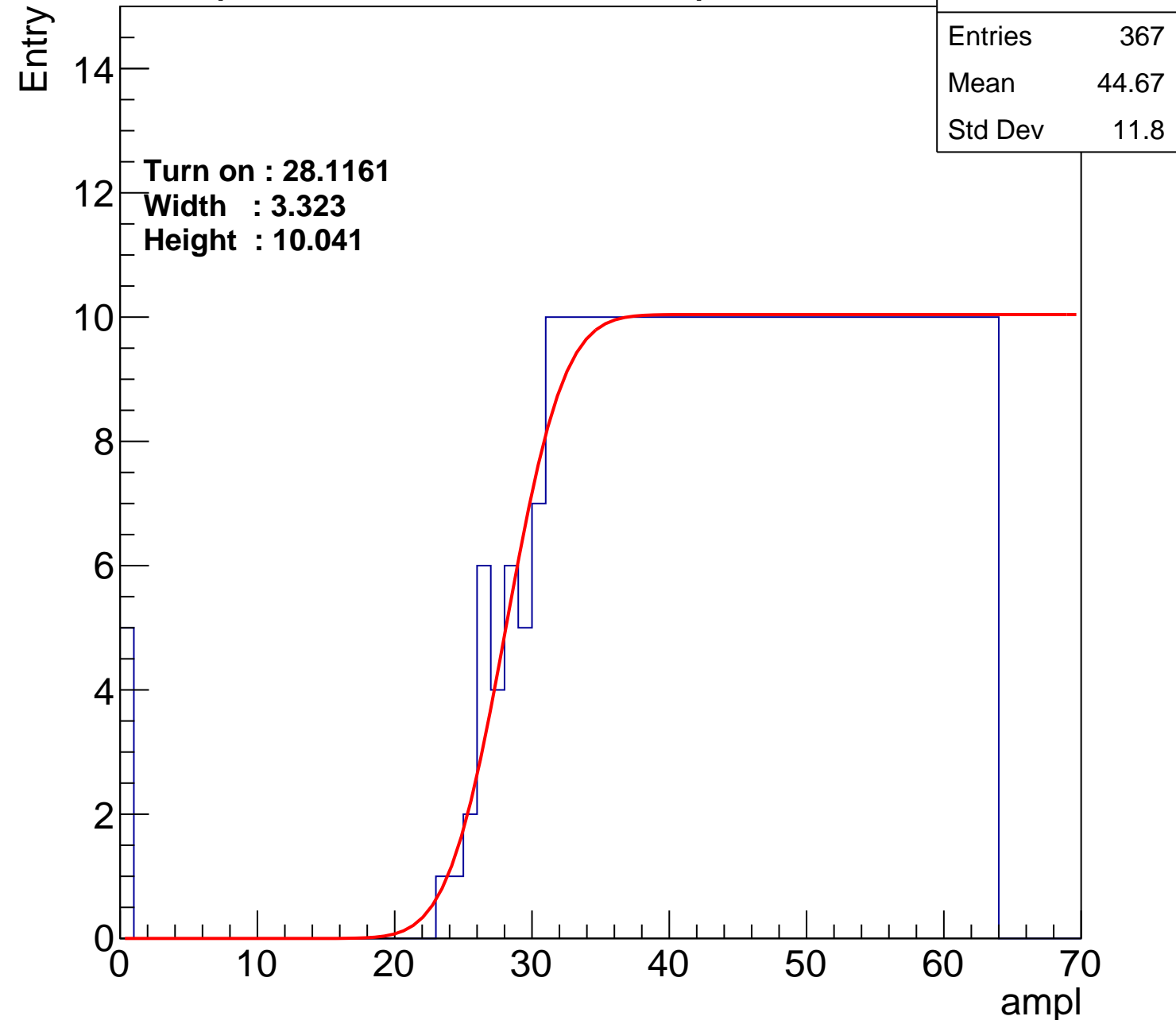
Width : 3.323

Height : 10.041

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch122

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	368
Mean	44.81
Std Dev	11.28

**Turn on : 27.7286**

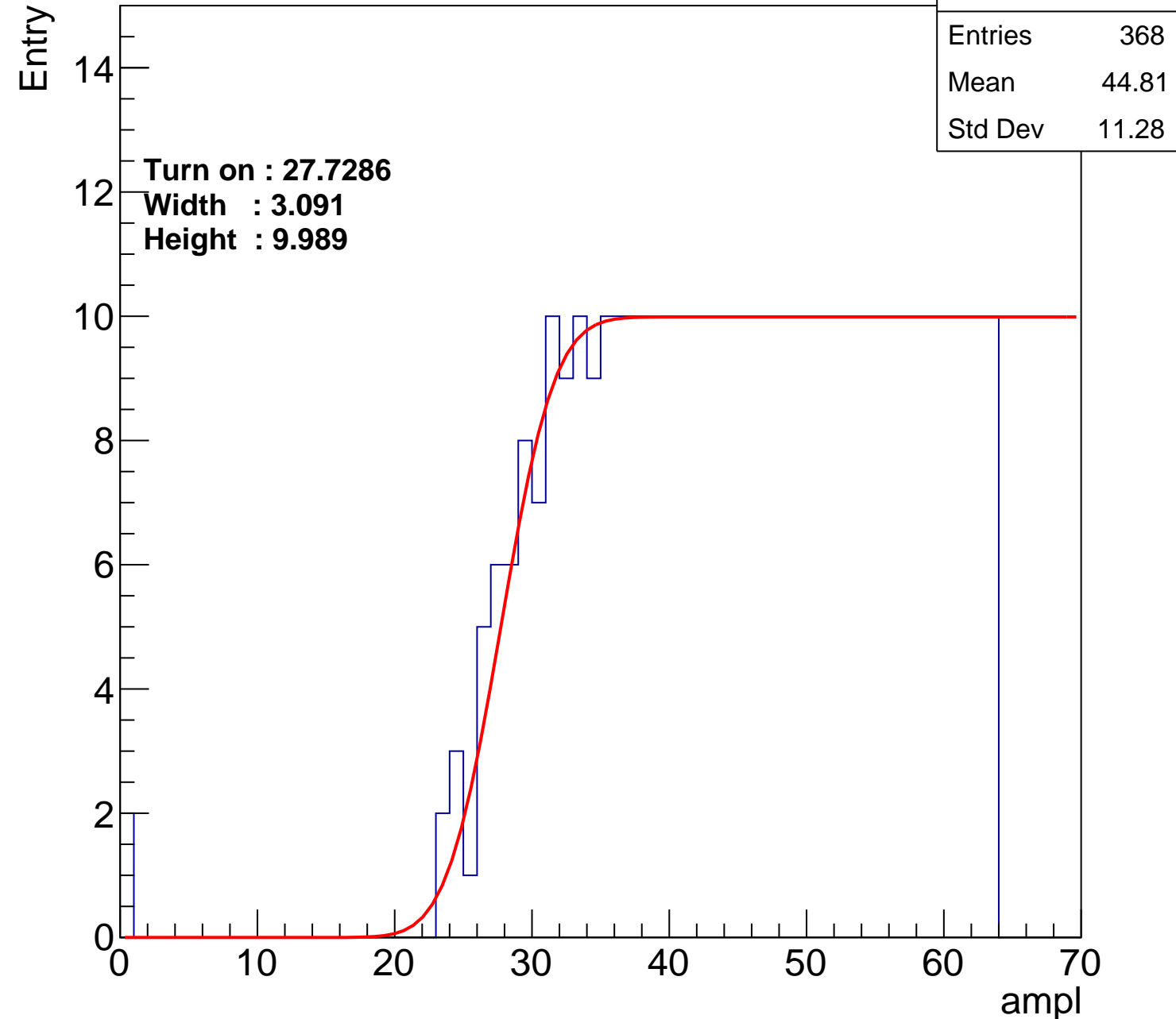
**Width : 3.091**

**Height : 9.989**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch123

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	339
Mean	46.06
Std Dev	11.06

Turn on : 30.5560

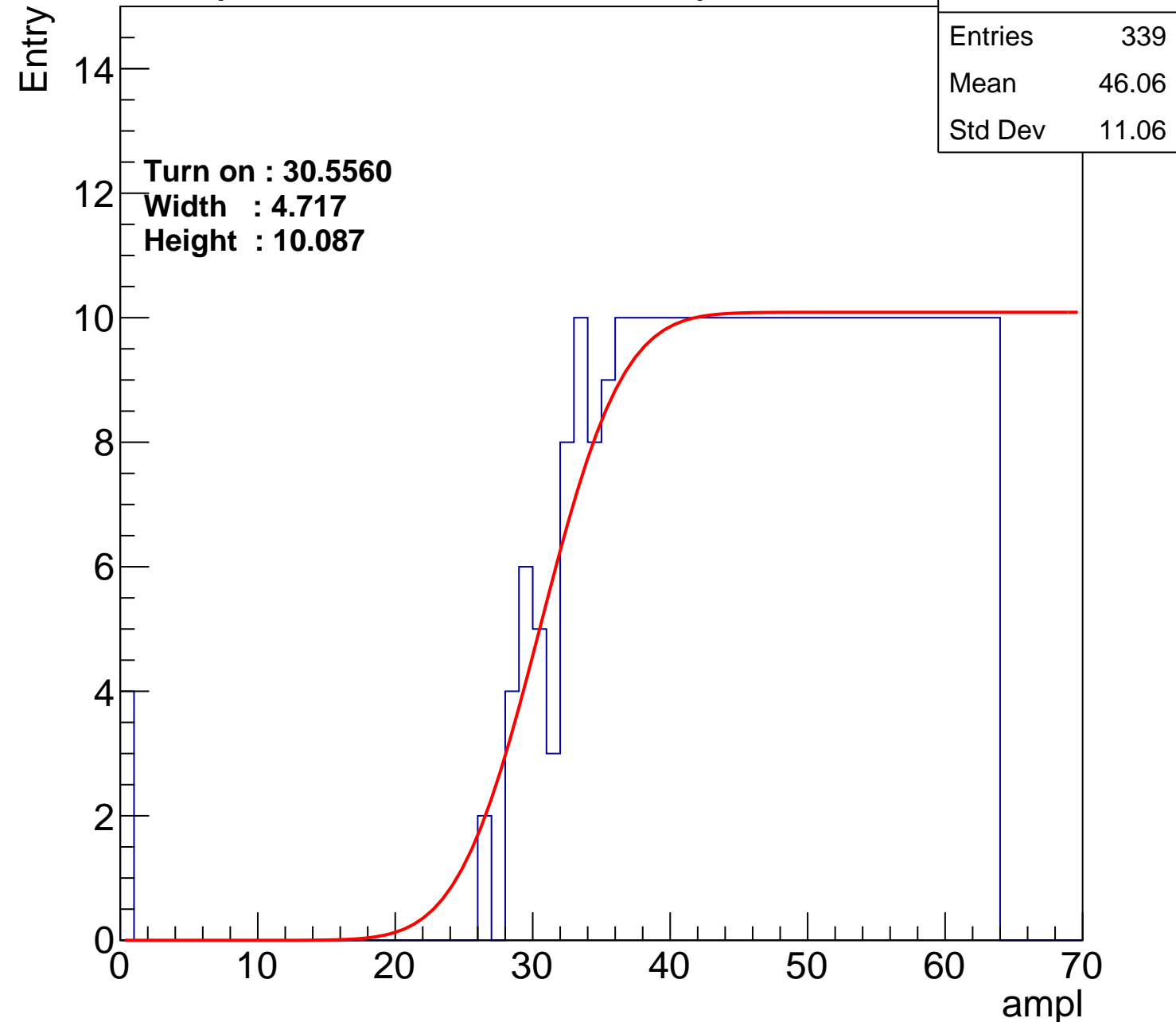
Width : 4.717

Height : 10.087

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch124

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	355
Mean	45.41
Std Dev	11.13

Turn on : 29.7441

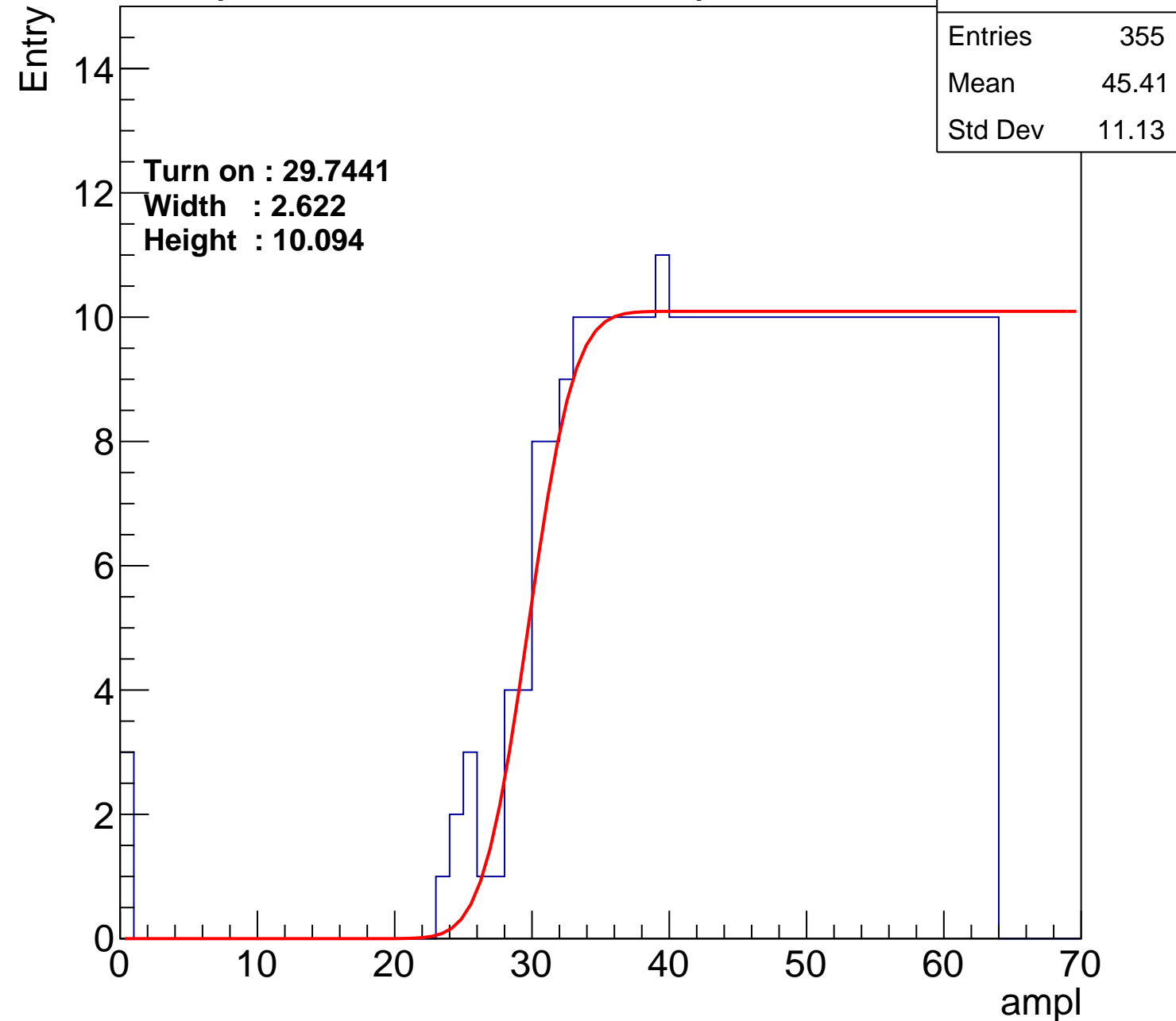
Width : 2.622

Height : 10.094

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch125

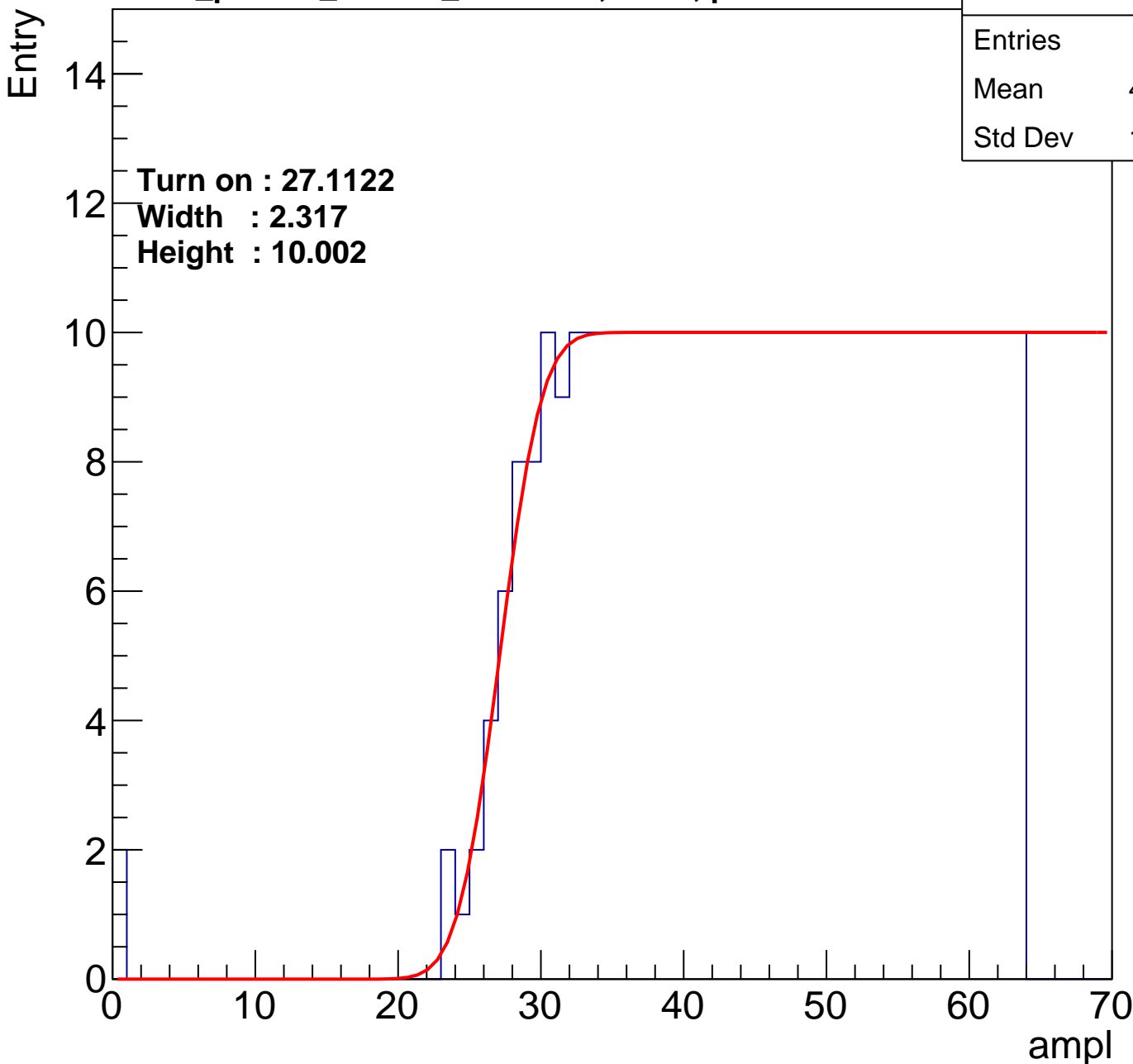
**calib\_packv5\_042523\_0143.root, FC#9, port A1**

**Turn on : 27.1122**

**Width : 2.317**

**Height : 10.002**

Entries	372
Mean	44.68
Std Dev	11.27



# B0L001S, U24-ch126

calib\_packv5\_042523\_0143.root, FC#9, port A1

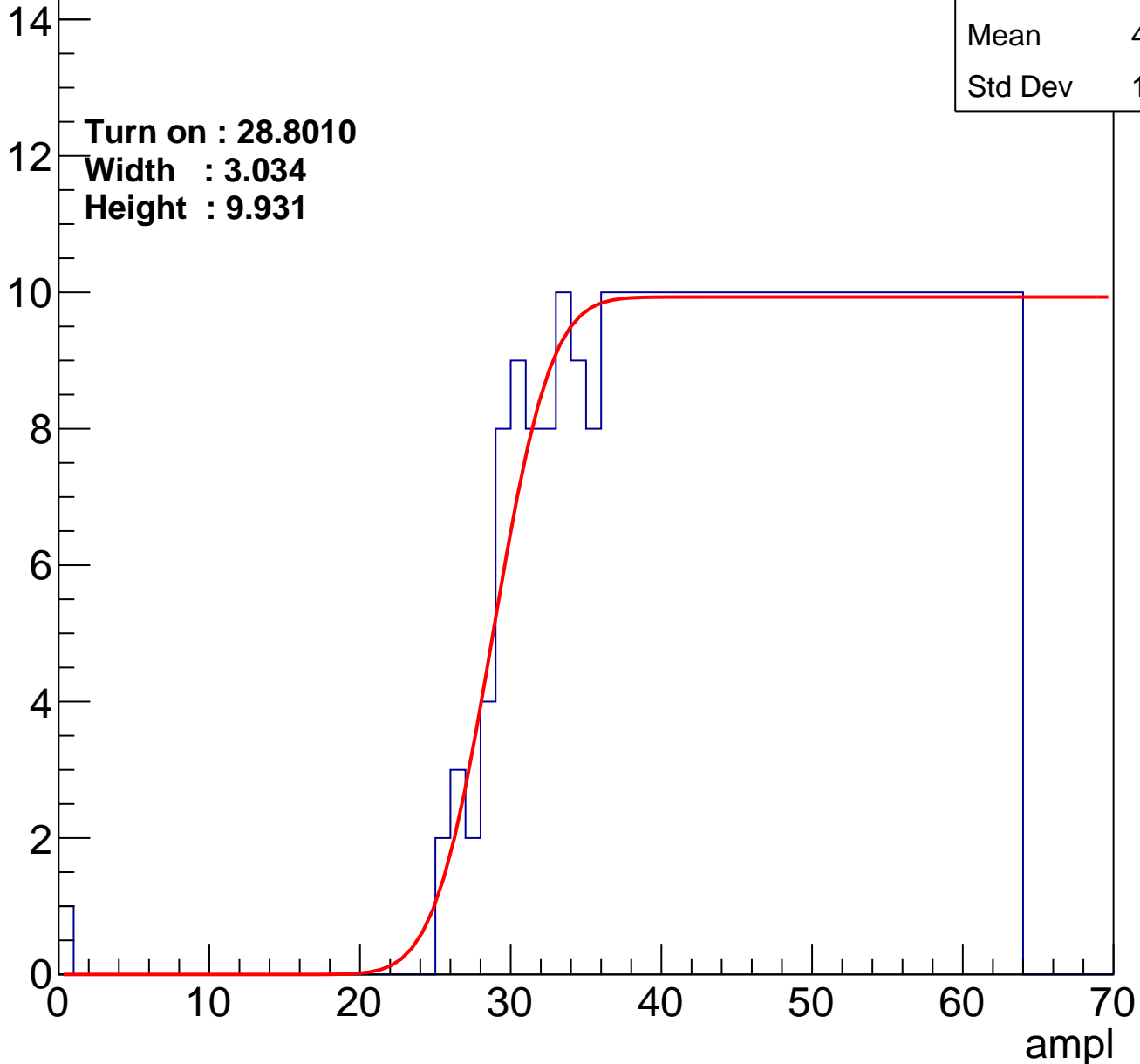
Entries	352
Mean	45.67
Std Dev	10.64

Turn on : 28.8010

Width : 3.034

Height : 9.931

Entry





# B0L001S, U24-ch127

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	366
Mean	44.91
Std Dev	11.21

Turn on : 27.3014

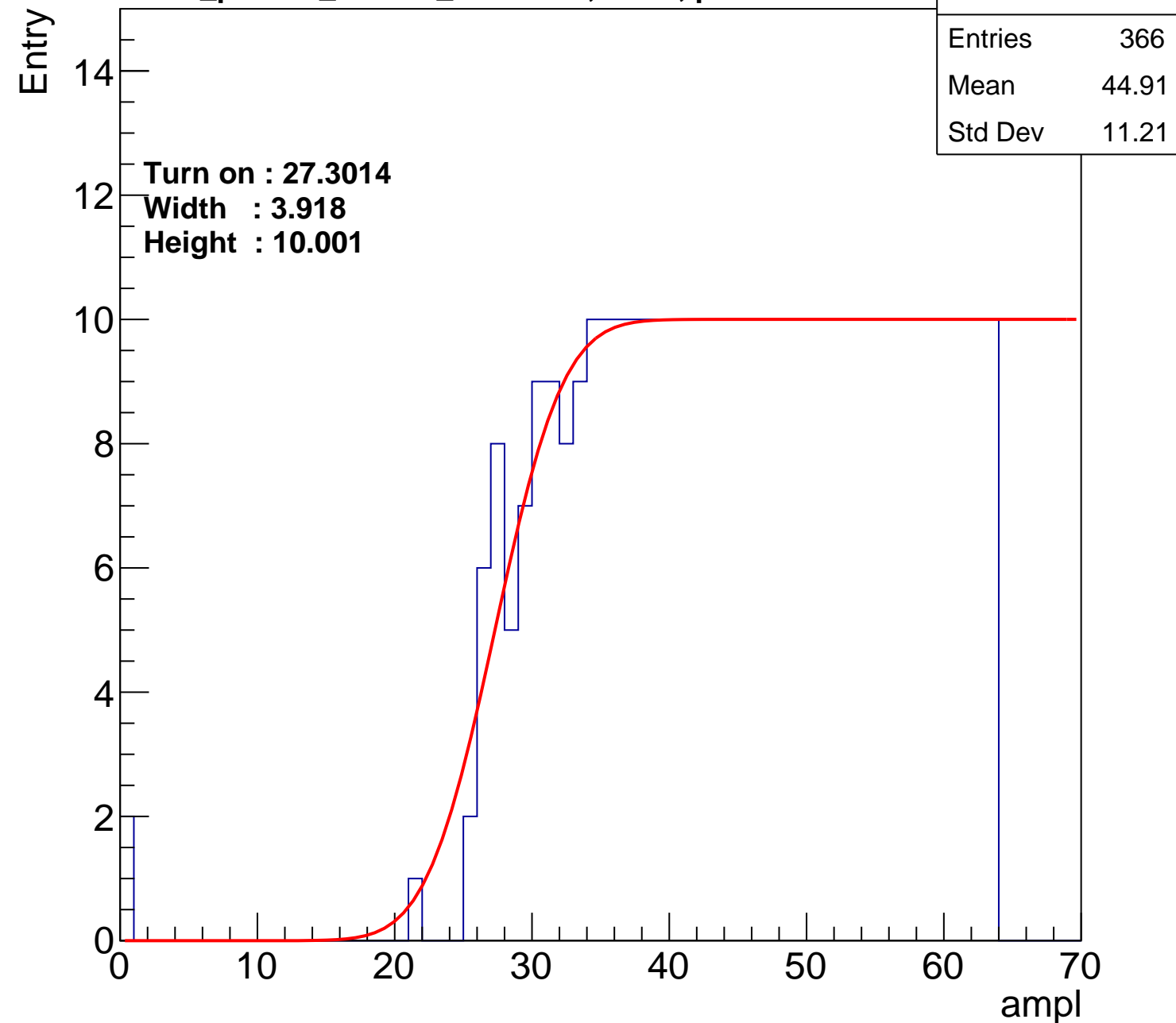
Width : 3.918

Height : 10.001

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L001S, U24-ch127

calib\_packv5\_042523\_0143.root, FC#9, port A1

Entries	366
Mean	44.91
Std Dev	11.21

Turn on : 27.3014

Width : 3.918

Height : 10.001

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

