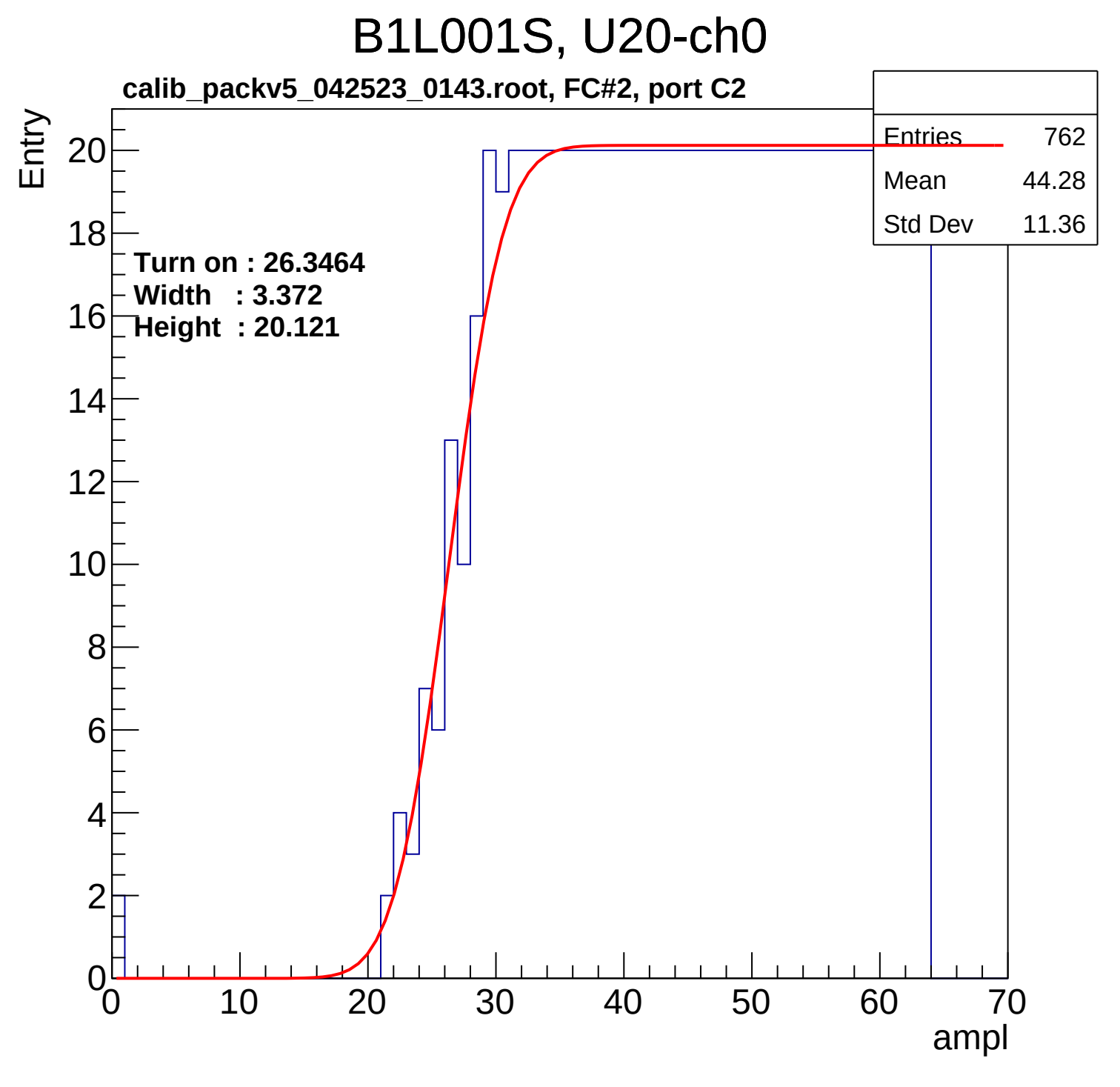
B1L001S, U20-ch0
calib_packv5_042523_0143.root, FC#2, port C2
Entries 762
Mean 44.28
Std Dev 11.36
Turn on : 26.3464
Width : 3.372
Height : 20.121
Entry
ampl
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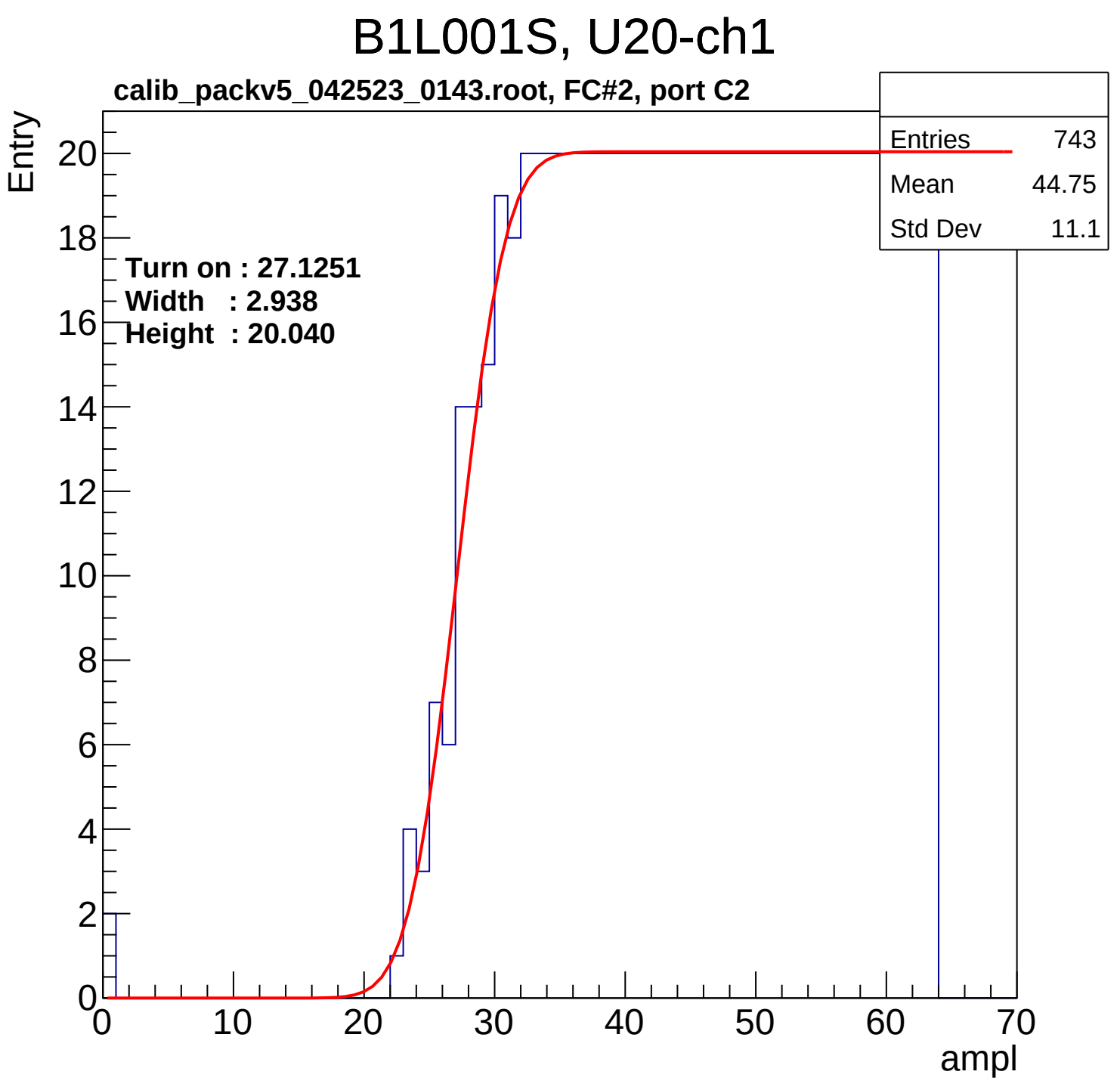
B1L001S, U20-ch1
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.75
Std Dev 11.1
Turn on : 27.1251
Width : 2.938
Height : 20.040
Entry
ampl
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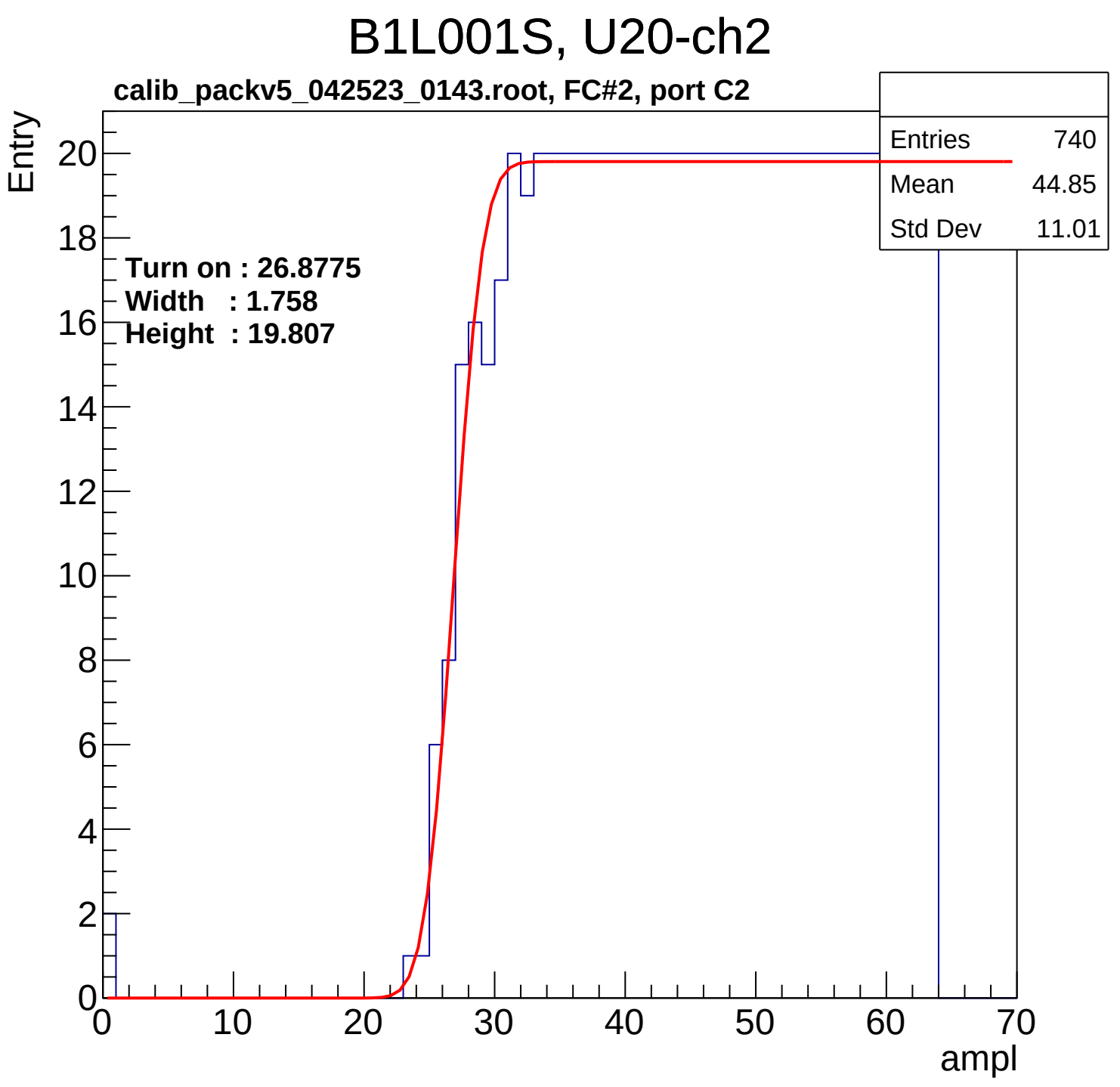
B1L001S, U20-ch2
calib_packv5_042523_0143.root, FC#2, port C2
Entries 740
Mean 44.85
Std Dev 11.01
Turn on : 26.8775
Width : 1.758
Height : 19.807
Entry
ampl
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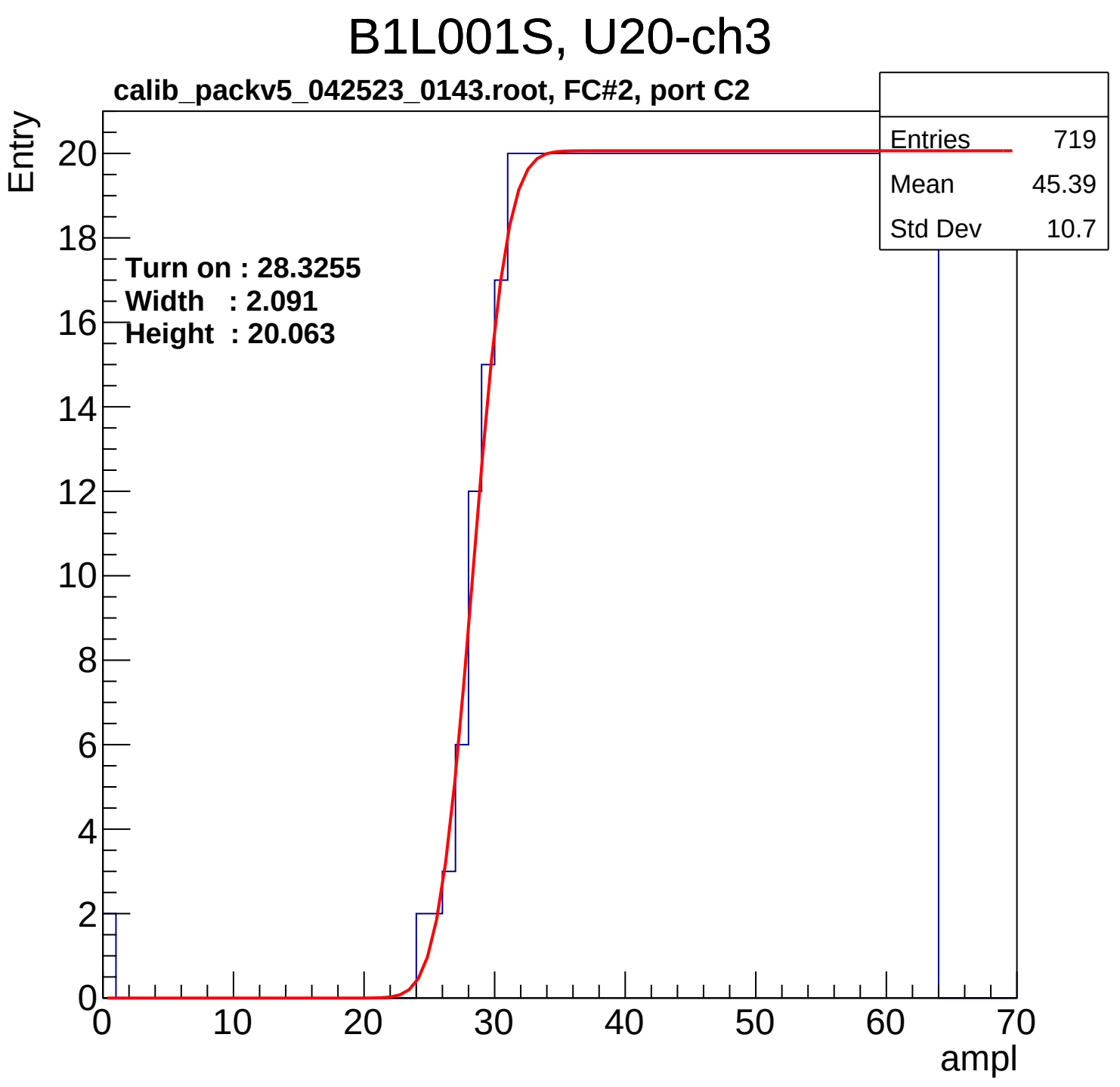
B1L001S, U20-ch3
calib_packv5_042523_0143.root, FC#2, port C2
Entries 719
Mean 45.39
Std Dev 10.7
Turn on : 28.3255
Width : 2.091
Height : 20.063
Entry
ampl
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6
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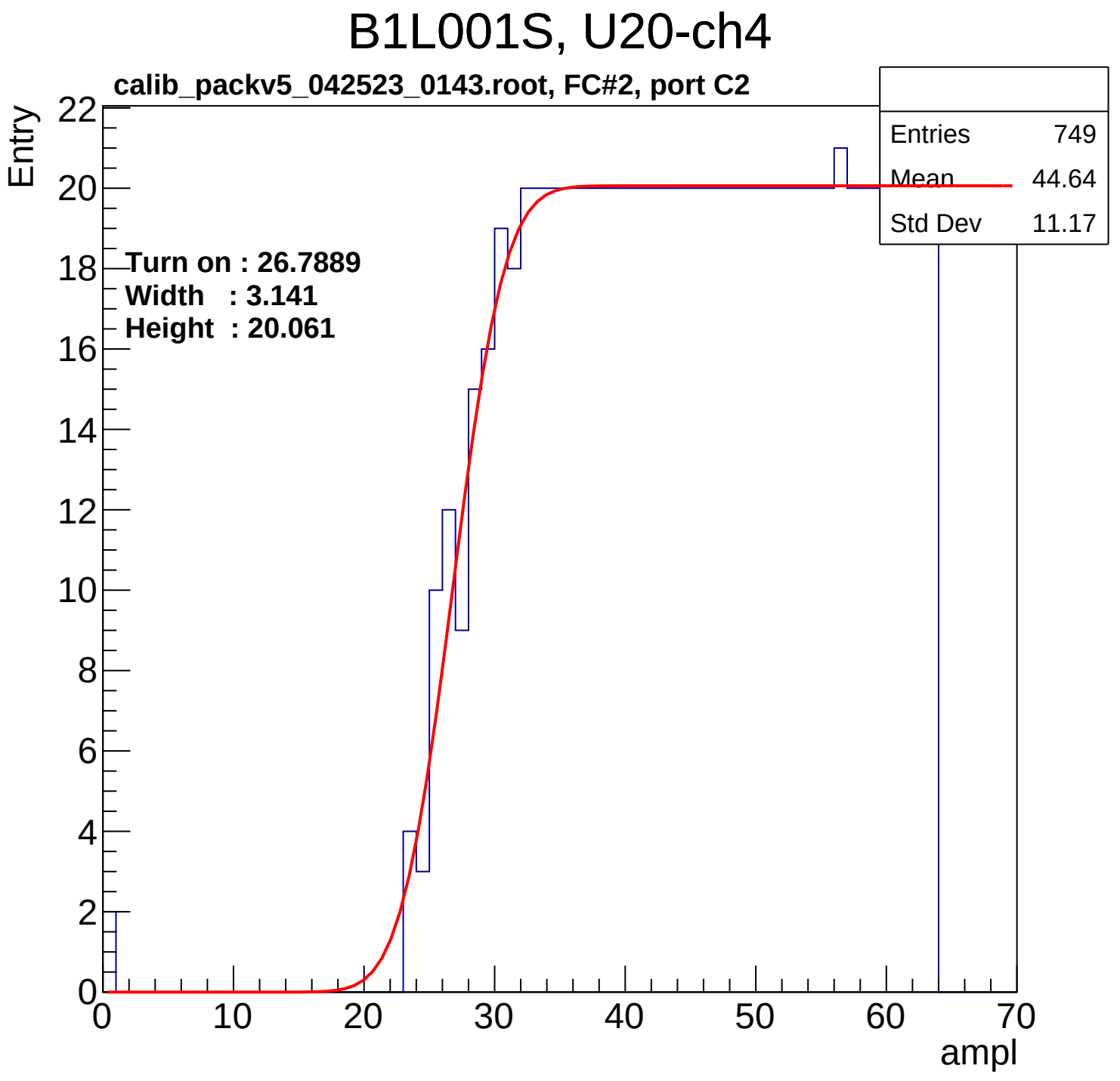
B1L001S, U20-ch4
calib_packv5_042523_0143.root, FC#2, port C2
Entries 749
Mean 44.64
Std Dev 11.17
Turn on : 26.7889
Width : 3.141
Height : 20.061
Entry
ampl
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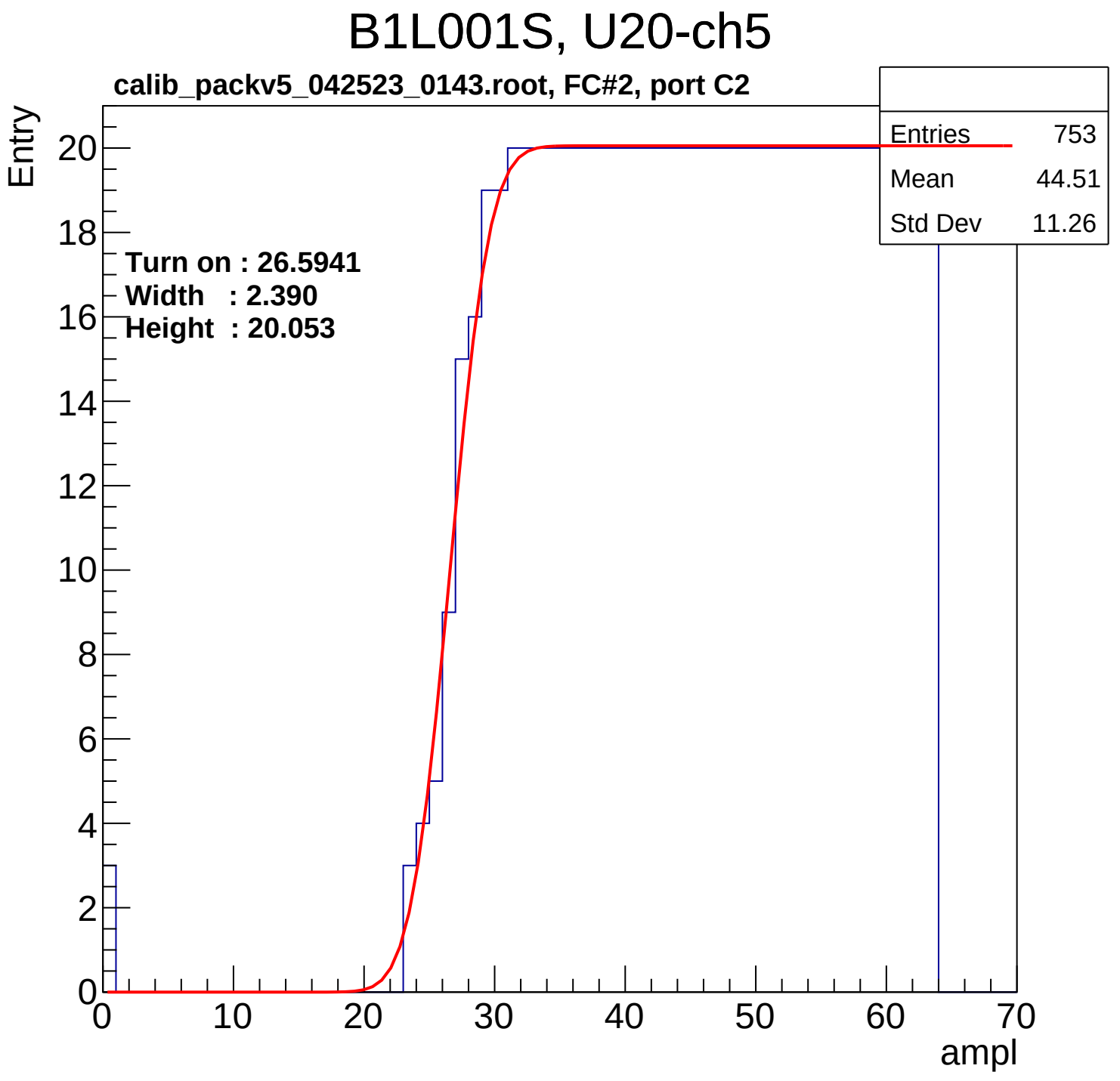
B1L001S, U20-ch5
calib_packv5_042523_0143.root, FC#2, port C2
Entries 753
Mean 44.51
Std Dev 11.26
Turn on : 26.5941
Width : 2.390
Height : 20.053
Entry
ampl
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6
8
10
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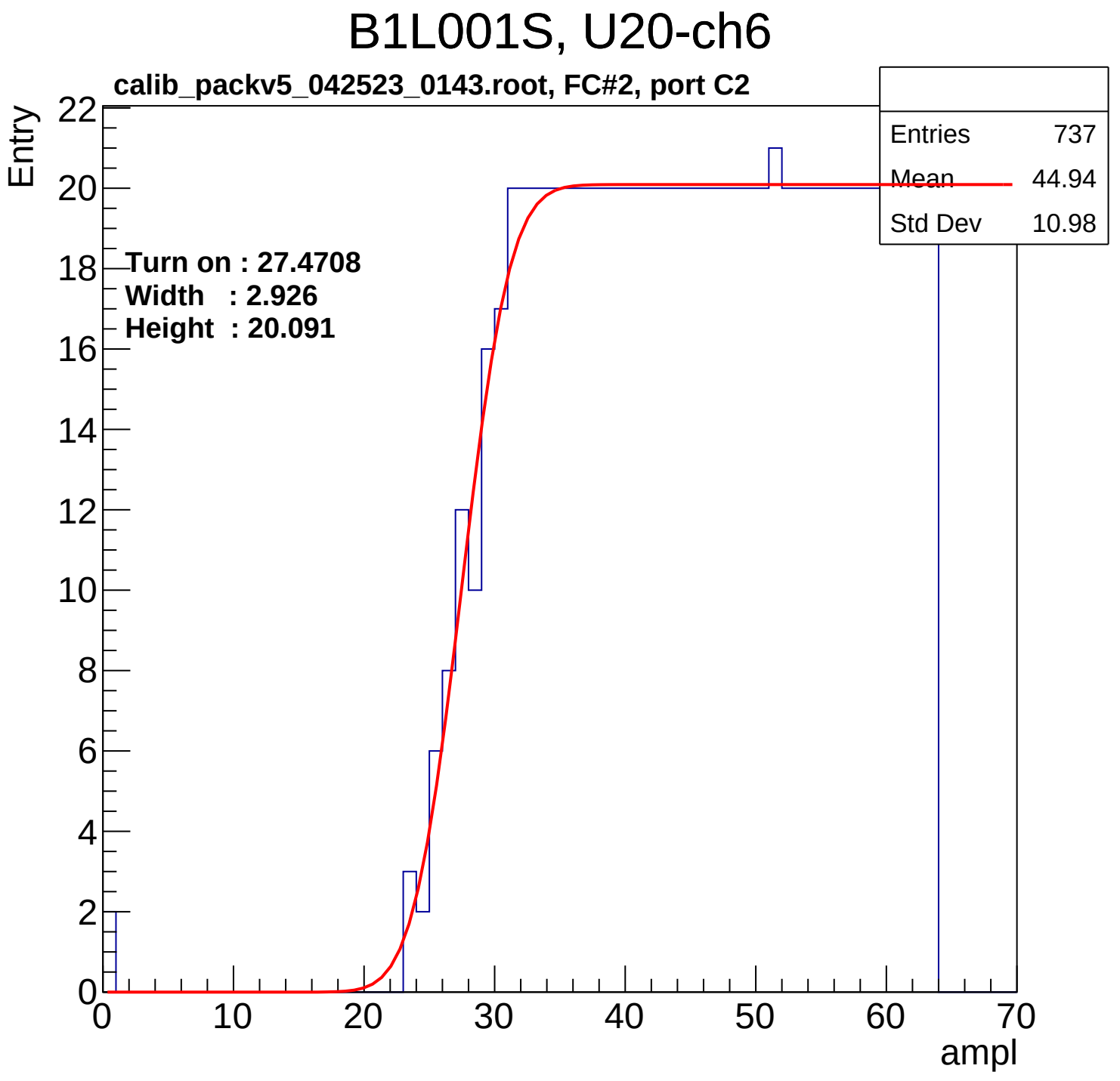
B1L001S, U20-ch6
calib_packv5_042523_0143.root, FC#2, port C2
Entries 737
Mean 44.94
Std Dev 10.98
Turn on : 27.4708
Width : 2.926
Height : 20.091
Entry
ampl
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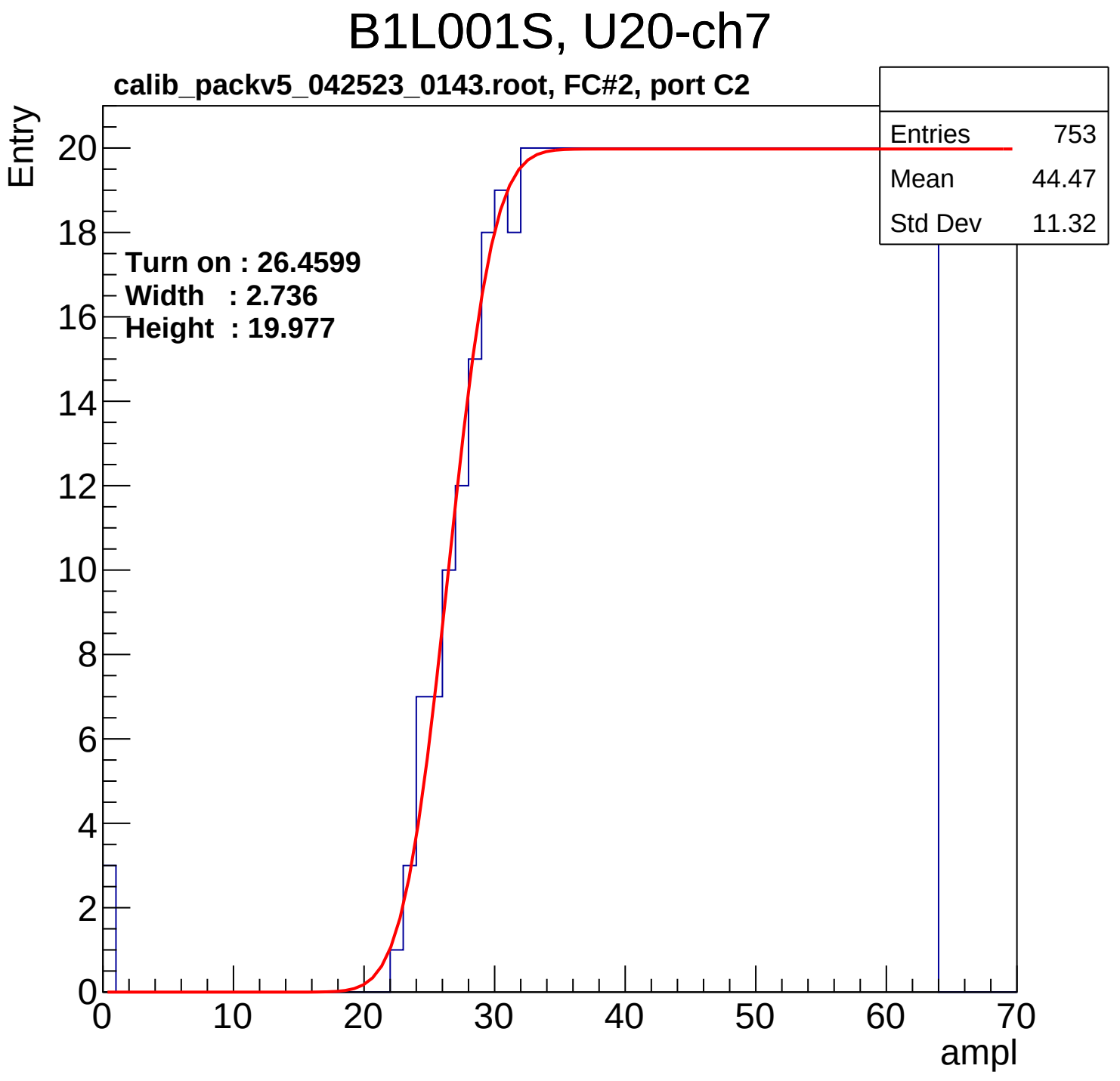
B1L001S, U20-ch7
calib_packv5_042523_0143.root, FC#2, port C2
Entries 753
Mean 44.47
Std Dev 11.32
Turn on : 26.4599
Width : 2.736
Height : 19.977
Entry
ampl
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6
8
10
12
14
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0
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20
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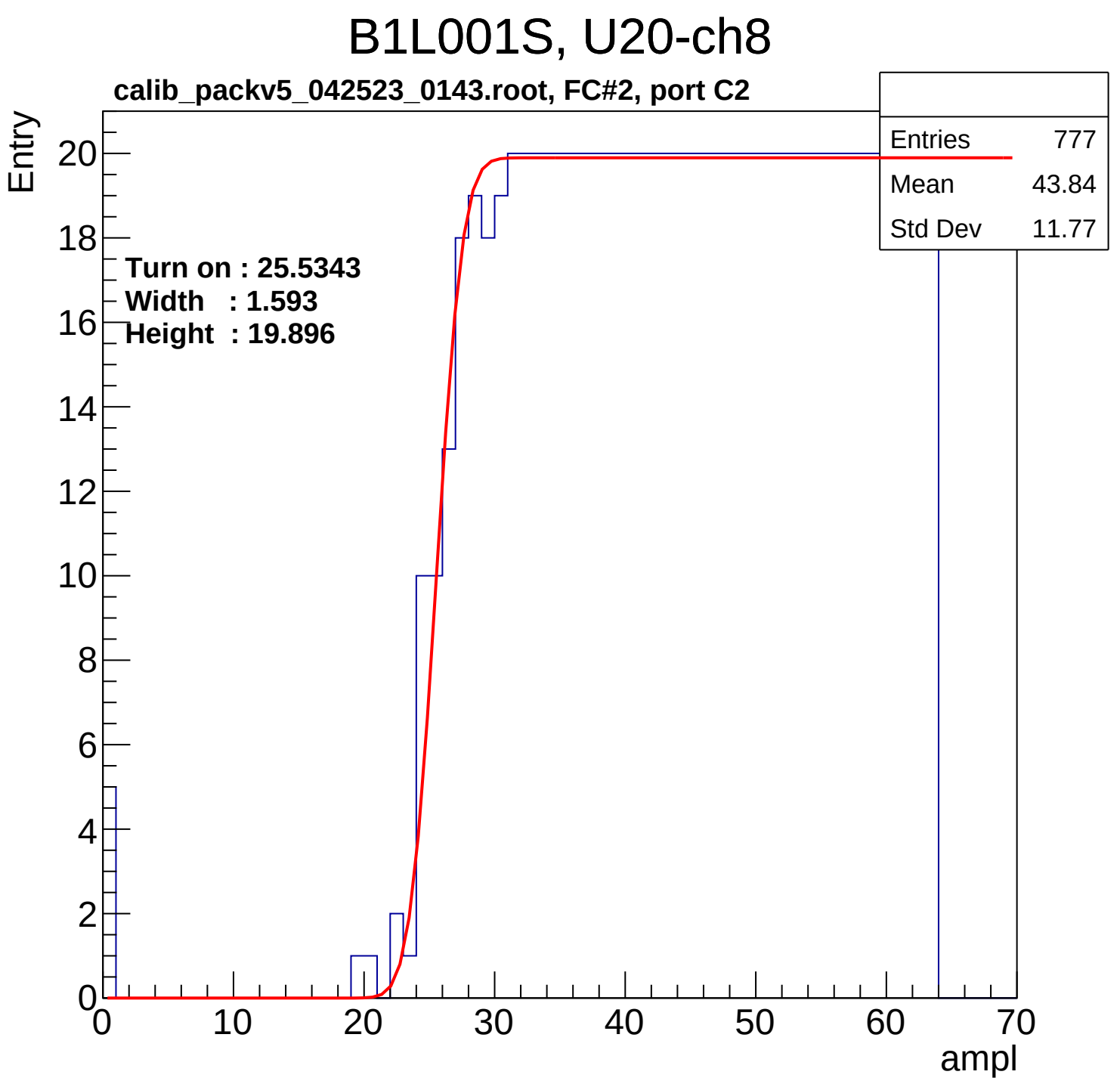
B1L001S, U20-ch8
calib_packv5_042523_0143.root, FC#2, port C2
Entries 777
Mean 43.84
Std Dev 11.77
Turn on : 25.5343
Width : 1.593
Height : 19.896
Entry
ampl
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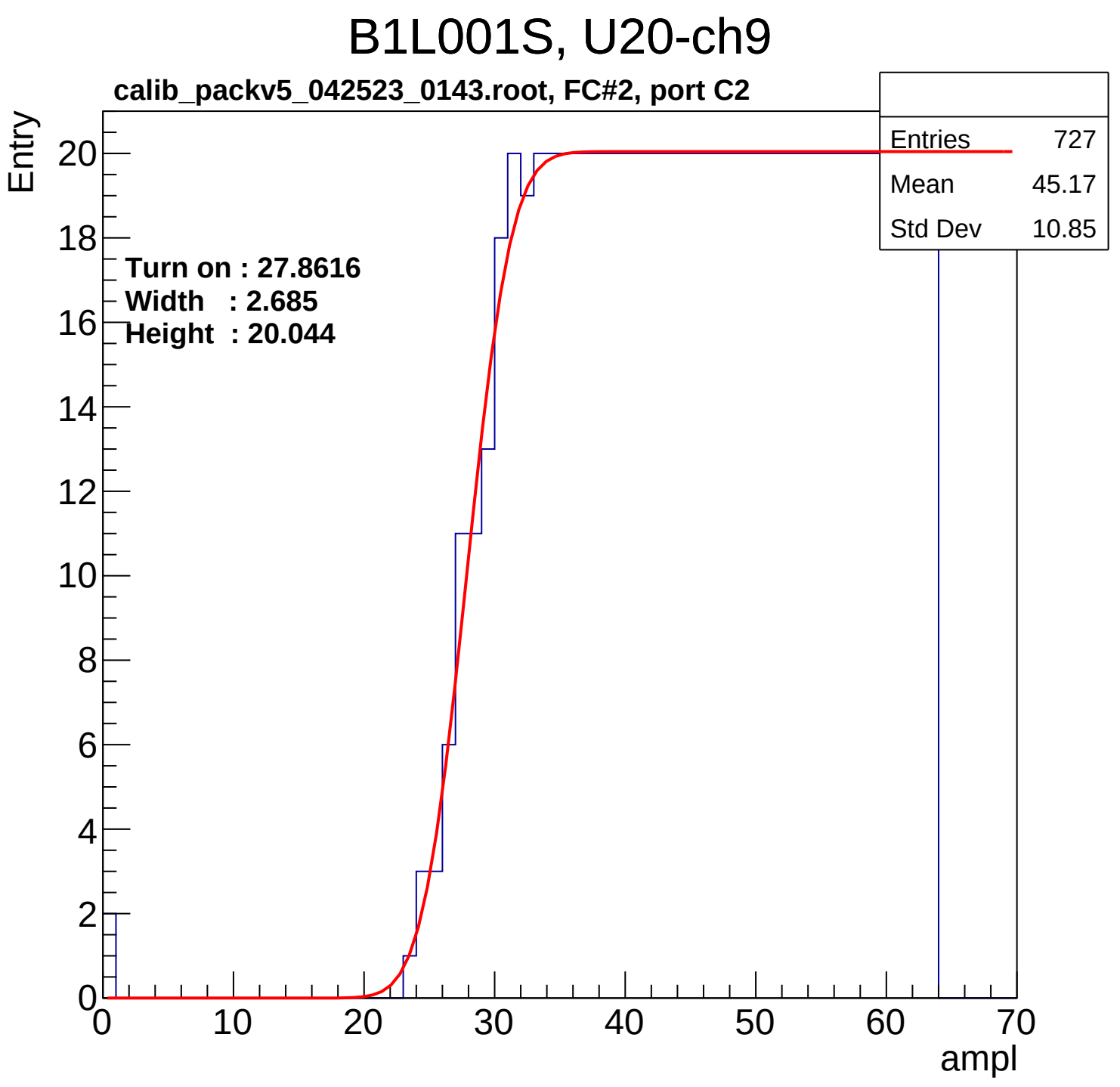
B1L001S, U20-ch9
calib_packv5_042523_0143.root, FC#2, port C2
Entries 727
Mean 45.17
Std Dev 10.85
Turn on : 27.8616
Width : 2.685
Height : 20.044
Entry
ampl
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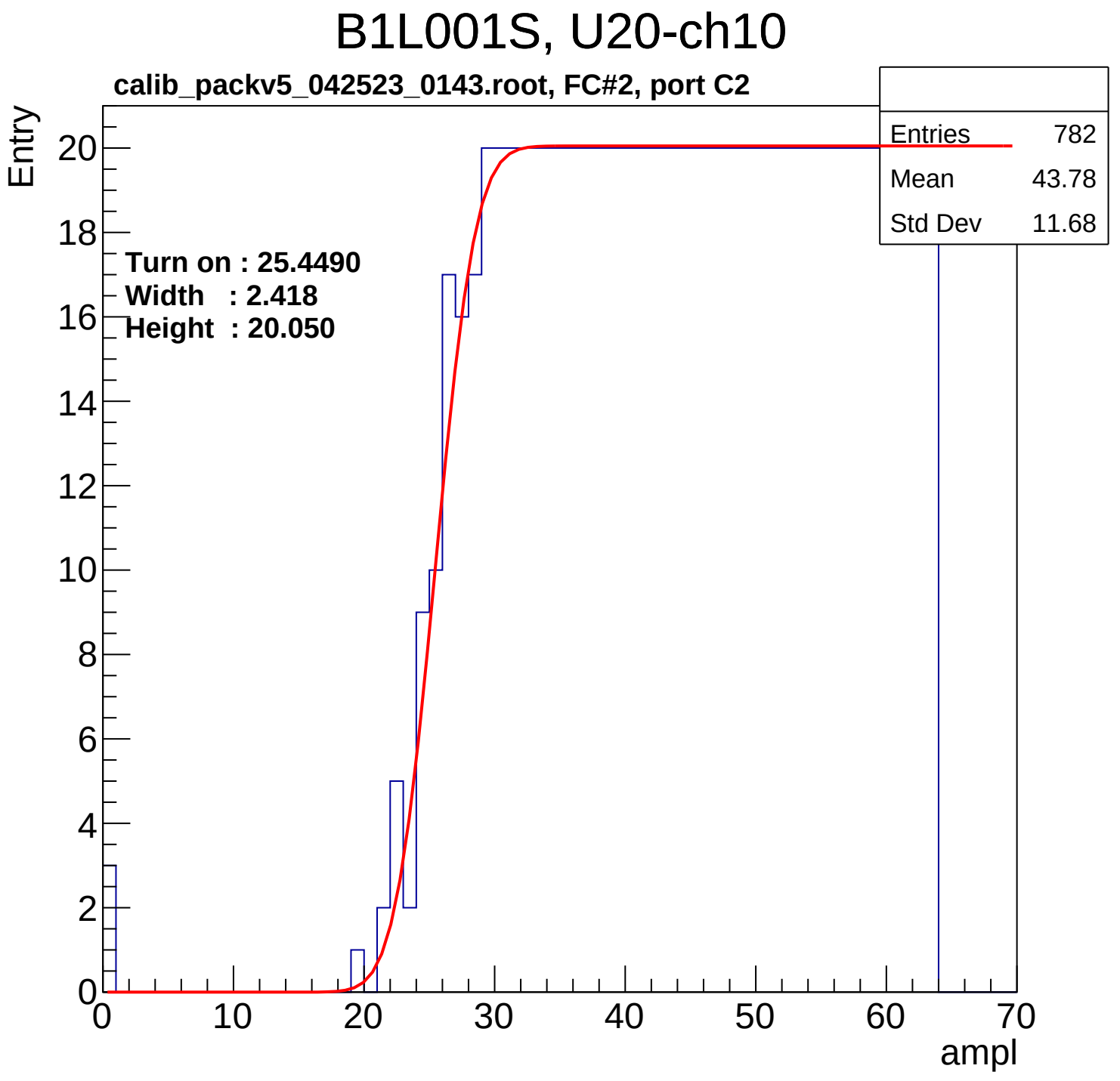
B1L001S, U20-ch10
calib_packv5_042523_0143.root, FC#2, port C2
Entries 782
Mean 43.78
Std Dev 11.68
Turn on : 25.4490
Width : 2.418
Height : 20.050
Entry
ampl
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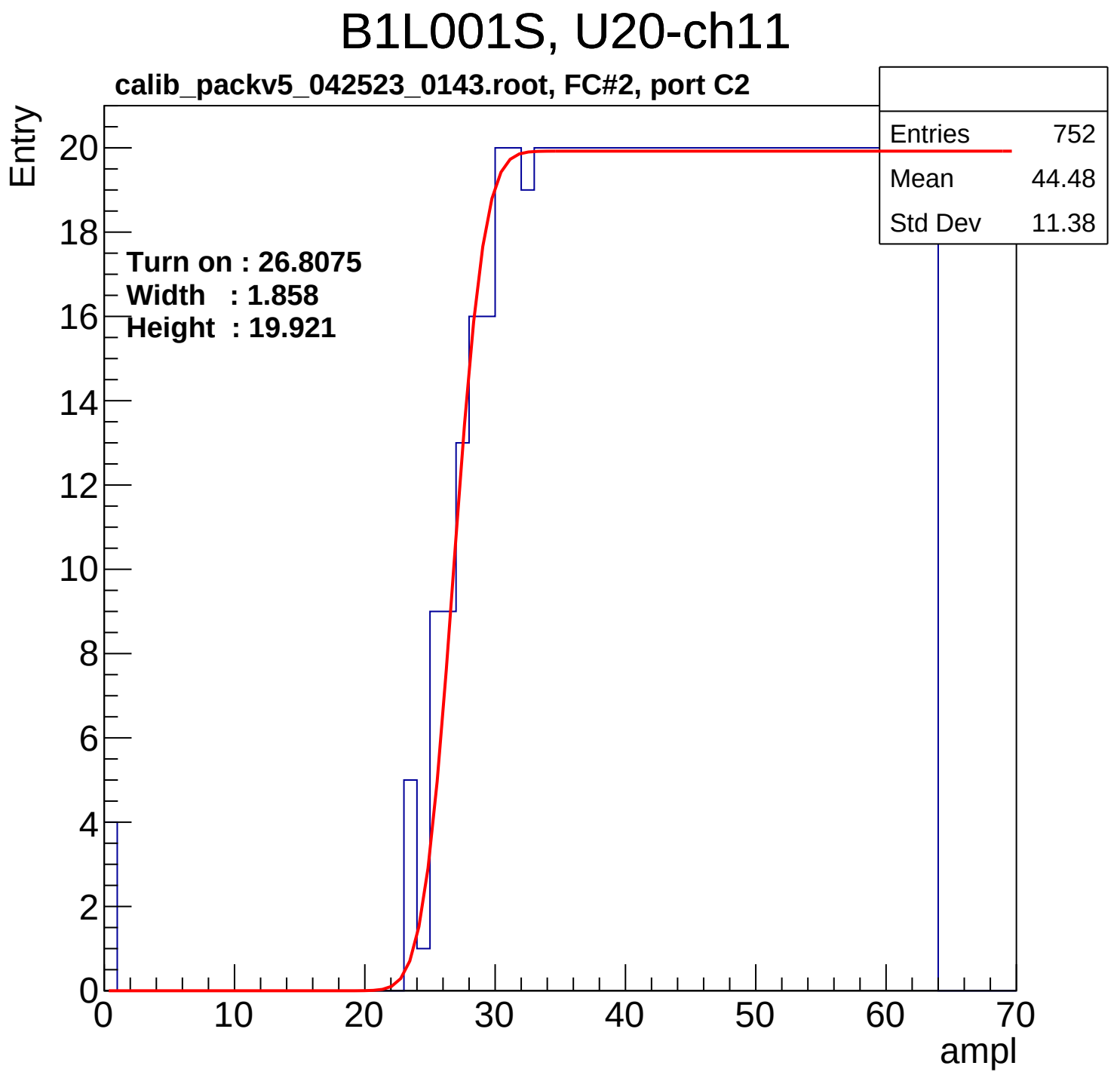
B1L001S, U20-ch11
calib_packv5_042523_0143.root, FC#2, port C2
Entries 752
Mean 44.48
Std Dev 11.38
Turn on : 26.8075
Width : 1.858
Height : 19.921
Entry
ampl
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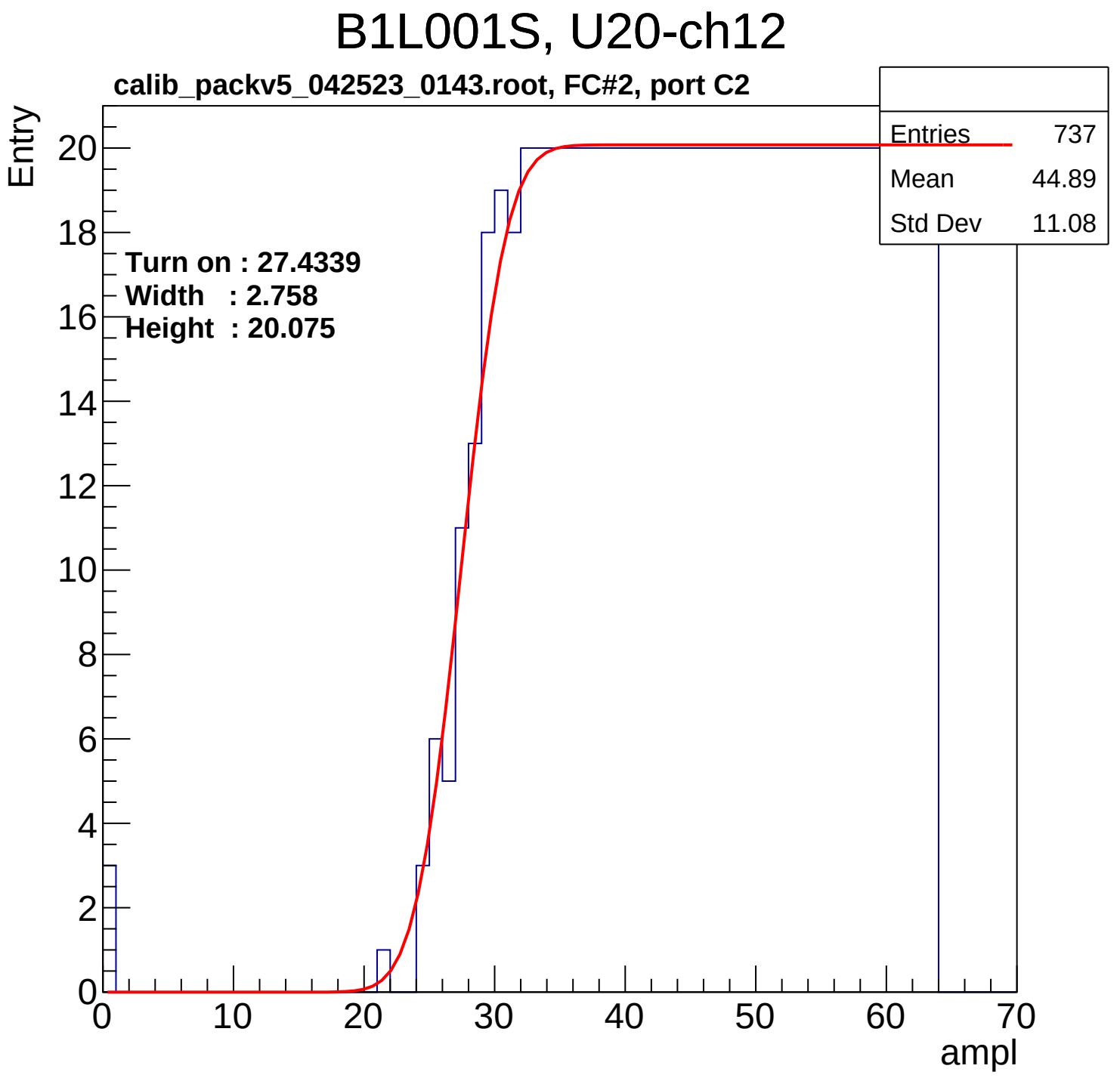
B1L001S, U20-ch12
calib_packv5_042523_0143.root, FC#2, port C2
Entries 737
Mean 44.89
Std Dev 11.08
Turn on : 27.4339
Width : 2.758
Height : 20.075
Entry
ampl
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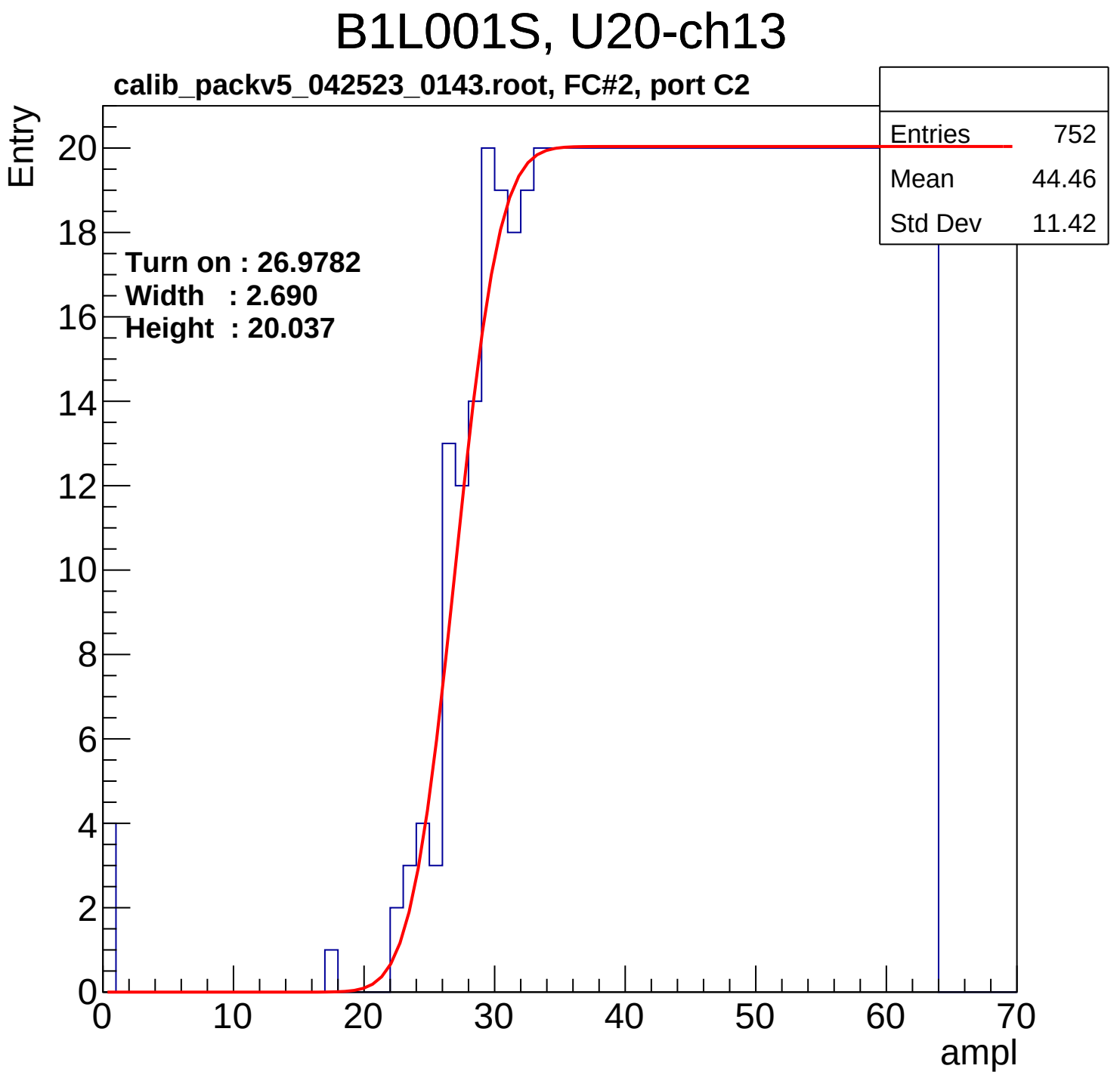
B1L001S, U20-ch13
calib_packv5_042523_0143.root, FC#2, port C2
Entries 752
Mean 44.46
Std Dev 11.42
Turn on : 26.9782
Width : 2.690
Height : 20.037
Entry
ampl
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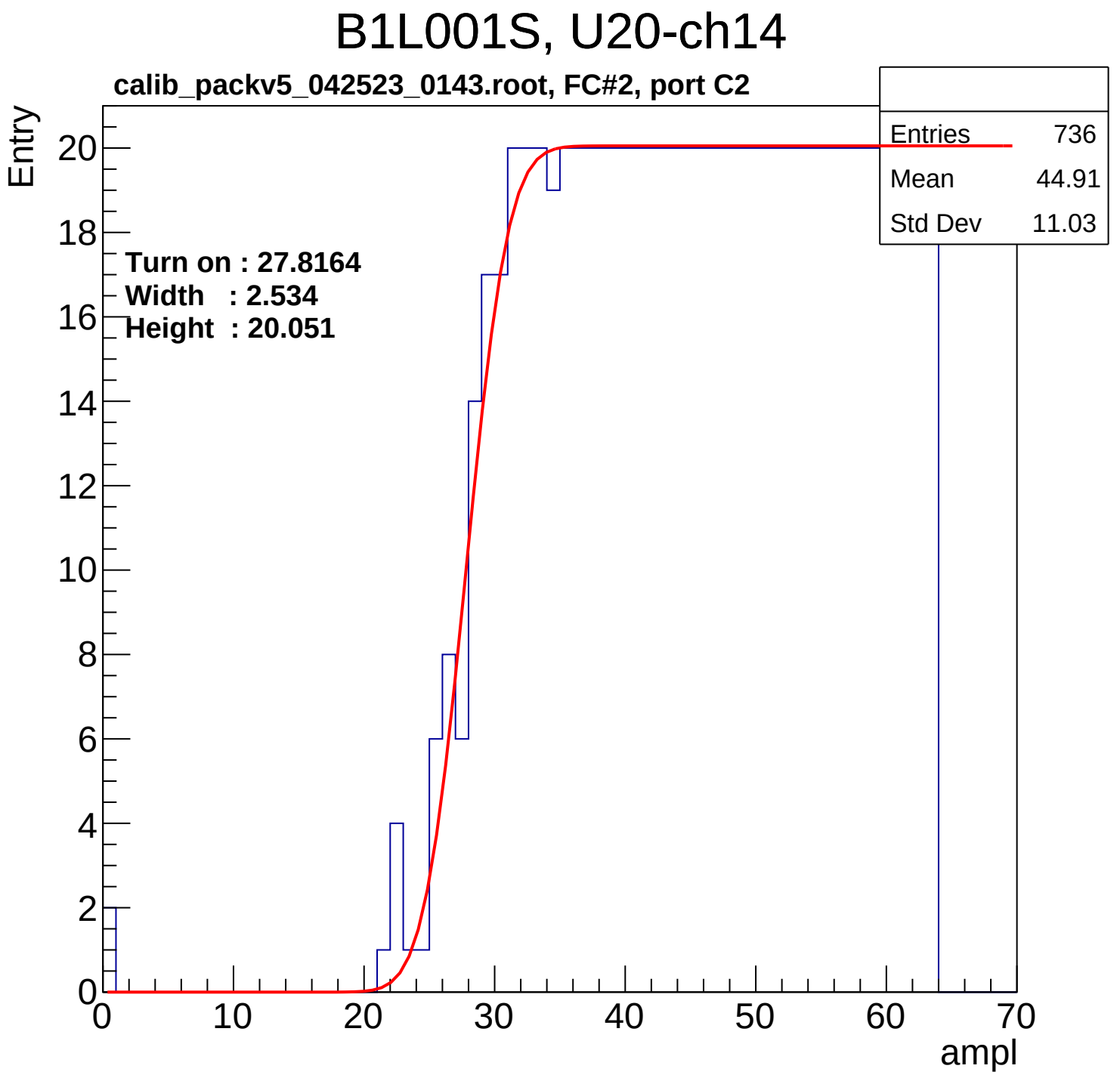
B1L001S, U20-ch14
calib_packv5_042523_0143.root, FC#2, port C2
Entries 736
Mean 44.91
Std Dev 11.03
Turn on : 27.8164
Width : 2.534
Height : 20.051
Entry
ampl
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6
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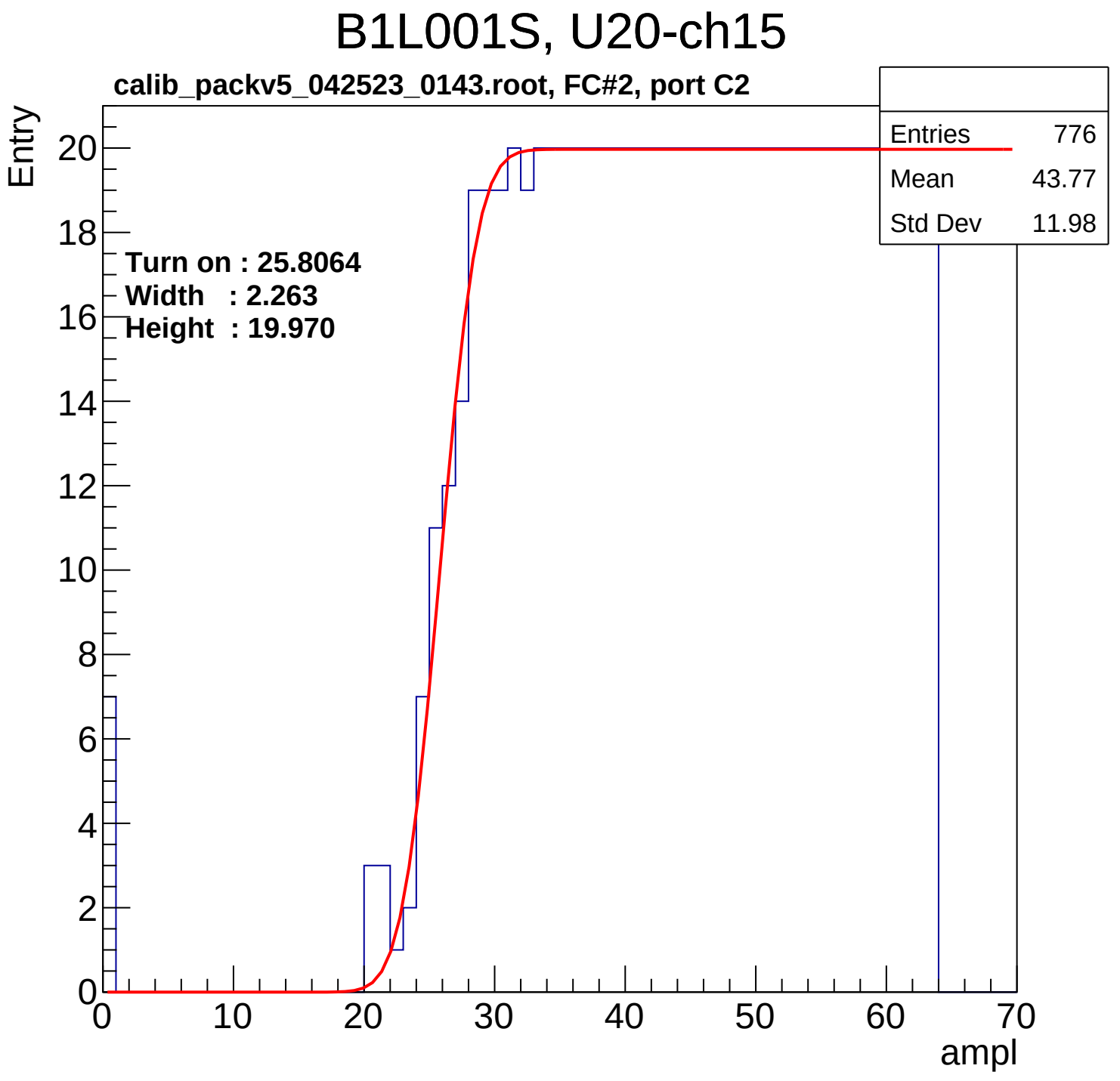
B1L001S, U20-ch15
calib_packv5_042523_0143.root, FC#2, port C2
Entries 776
Mean 43.77
Std Dev 11.98
Turn on : 25.8064
Width : 2.263
Height : 19.970
Entry
ampl
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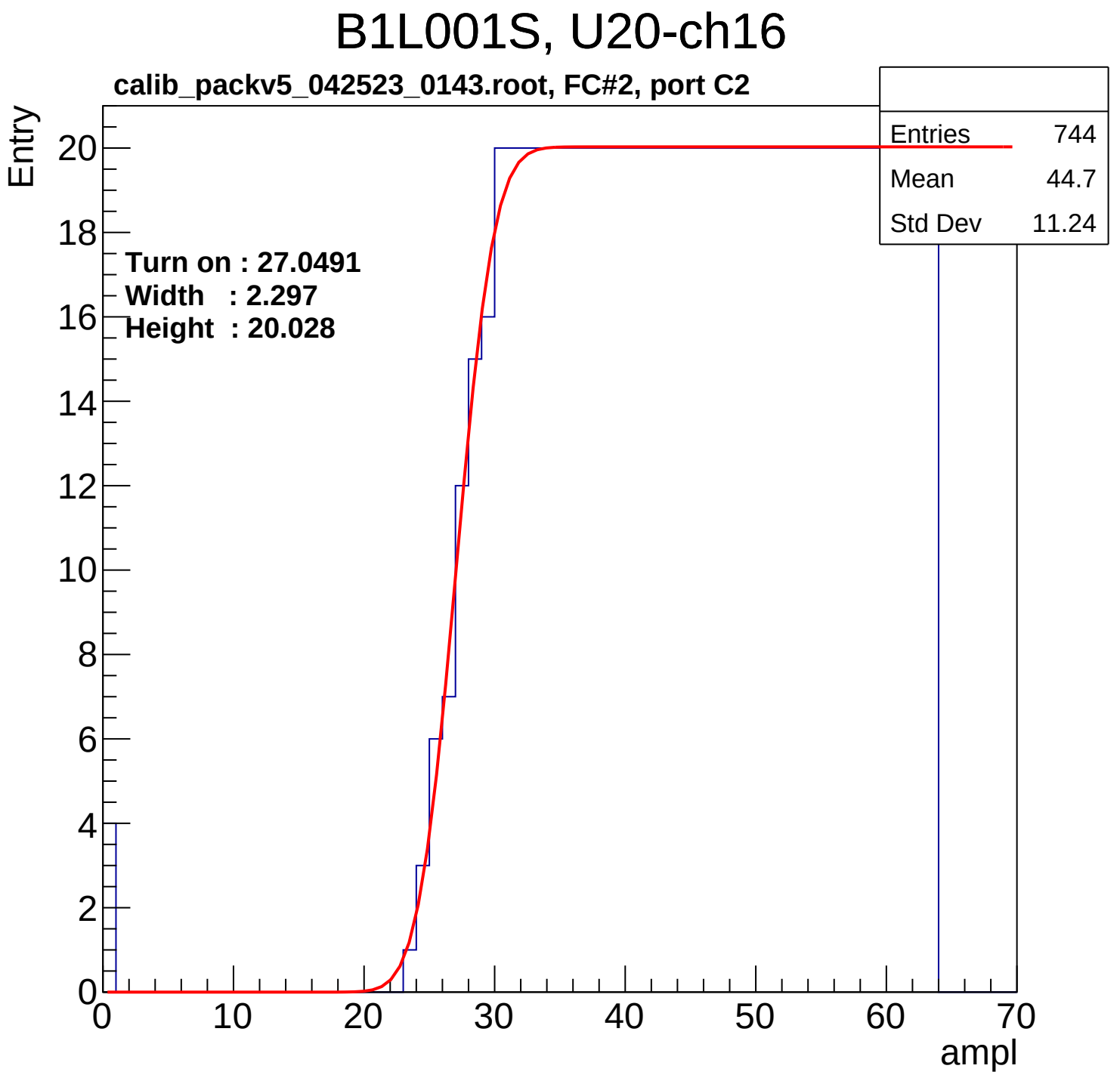
B1L001S, U20-ch16
calib_packv5_042523_0143.root, FC#2, port C2
Entries 744
Mean 44.7
Std Dev 11.24
Turn on : 27.0491
Width : 2.297
Height : 20.028
Entry
ampl
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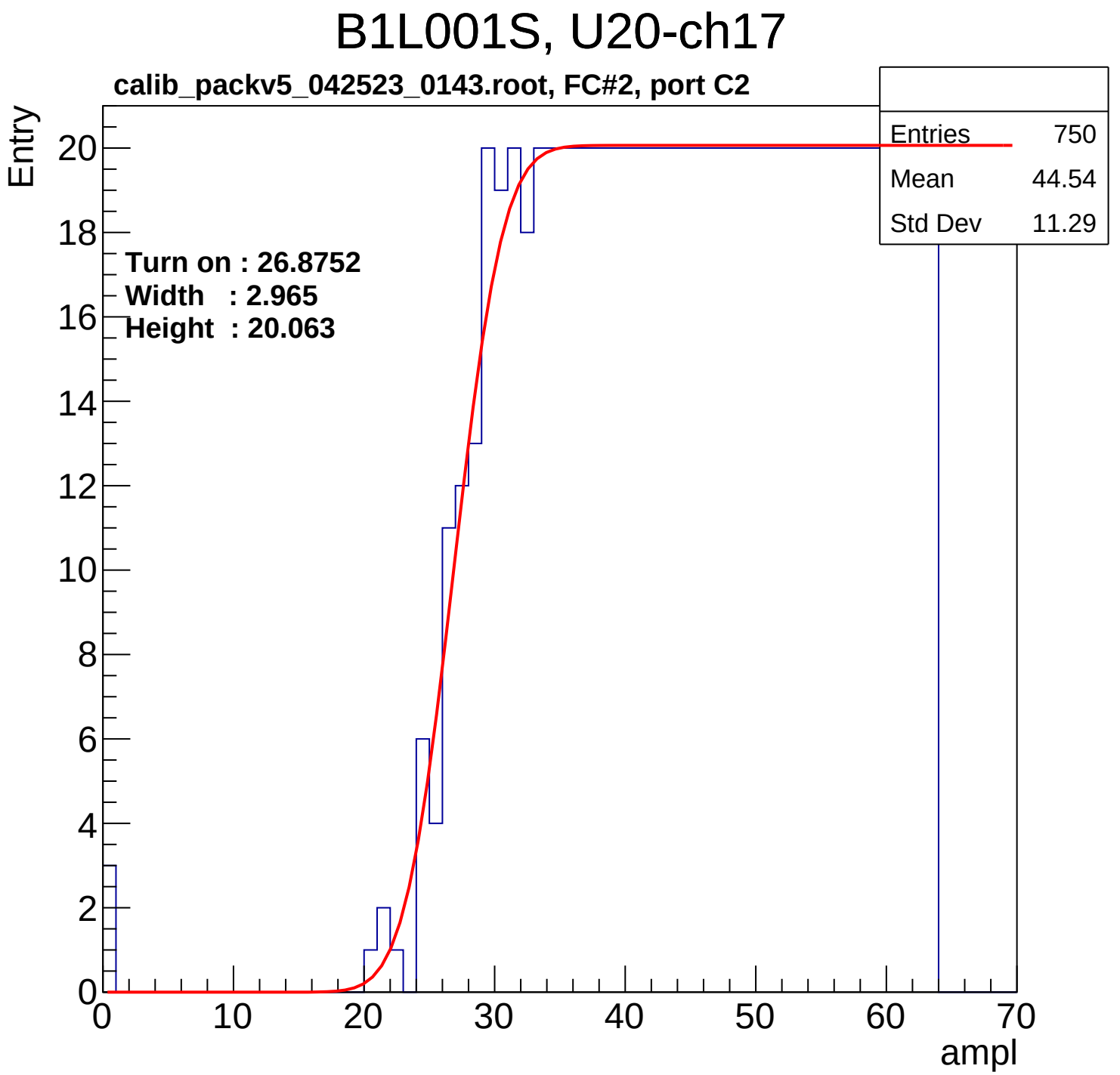
B1L001S, U20-ch17
calib_packv5_042523_0143.root, FC#2, port C2
Entries 750
Mean 44.54
Std Dev 11.29
Turn on : 26.8752
Width : 2.965
Height : 20.063
Entry
ampl
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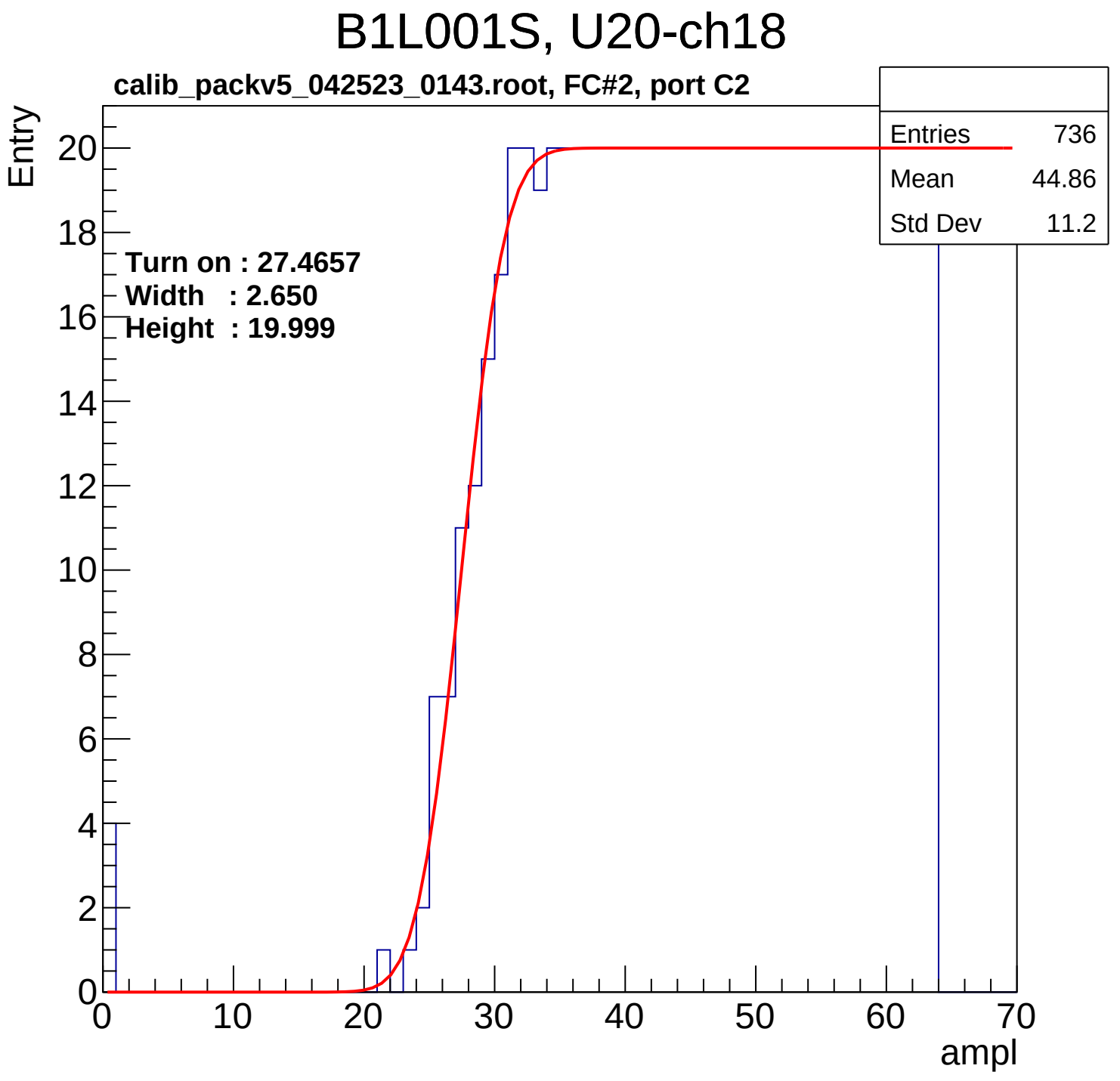
B1L001S, U20-ch18
calib_packv5_042523_0143.root, FC#2, port C2
Entries 736
Mean 44.86
Std Dev 11.2
Turn on : 27.4657
Width : 2.650
Height : 19.999
Entry
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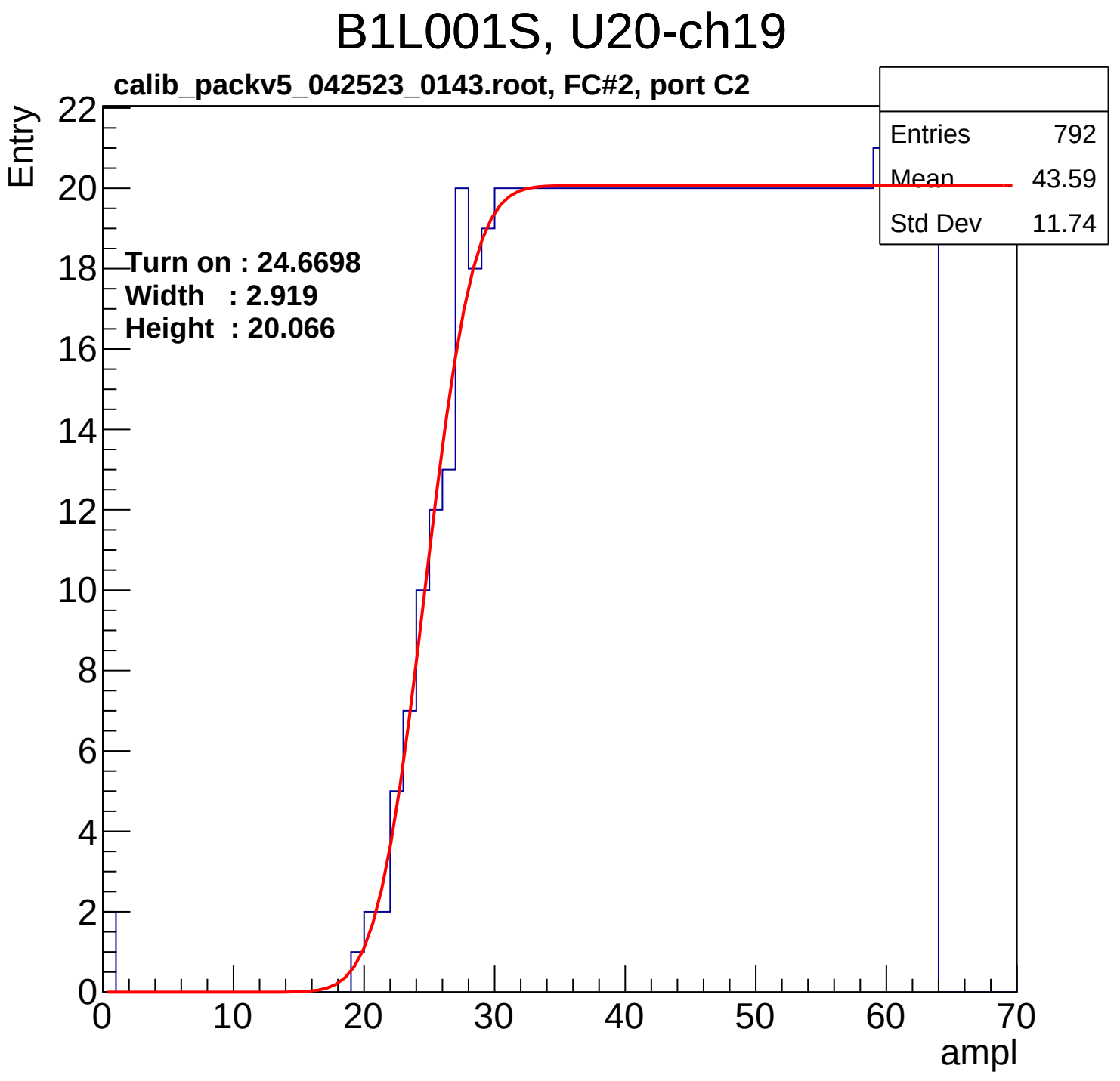
B1L001S, U20-ch19
calib_packv5_042523_0143.root, FC#2, port C2
Entries 792
Mean 43.59
Std Dev 11.74
Turn on : 24.6698
Width : 2.919
Height : 20.066
Entry
ampl
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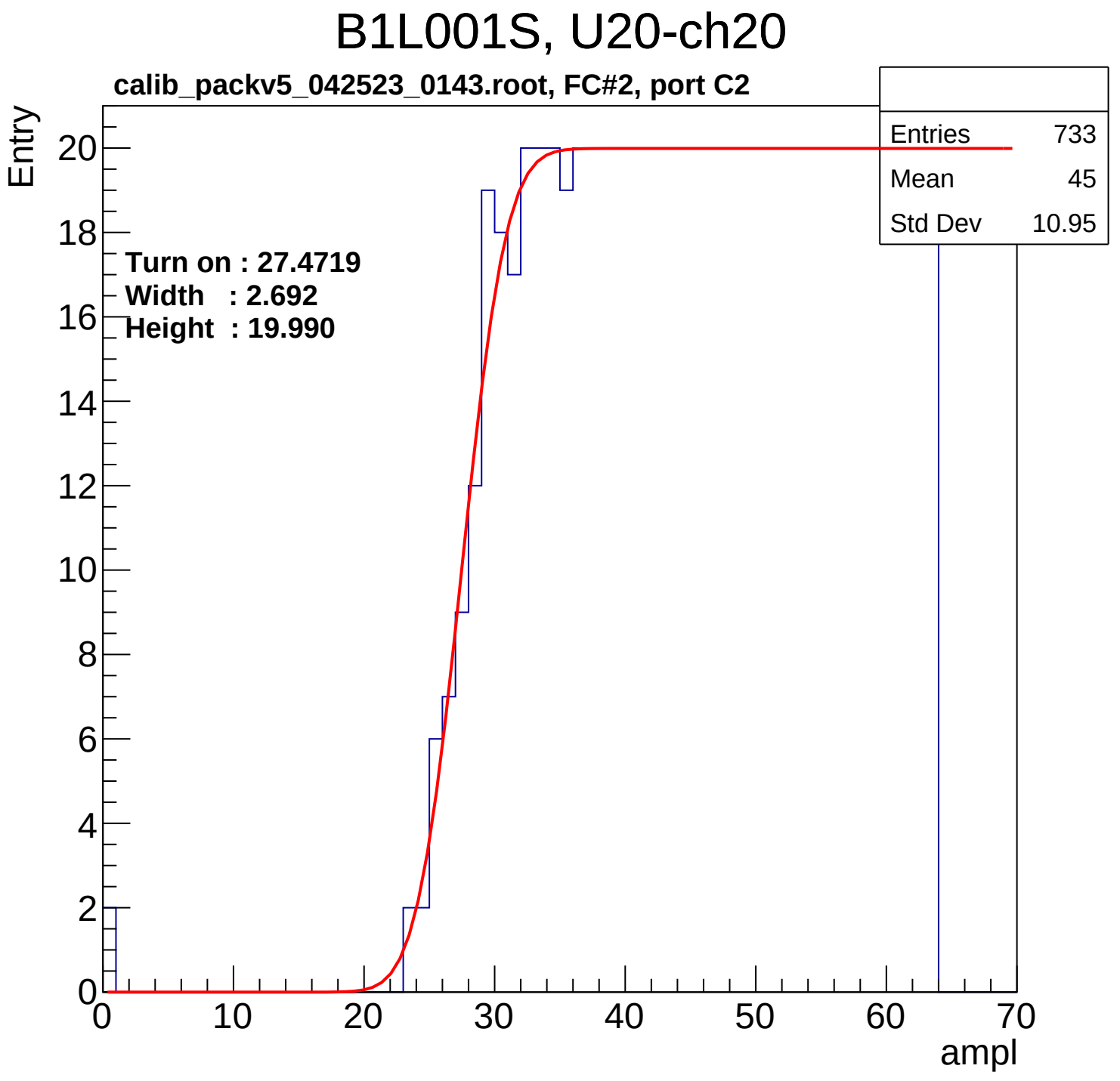
B1L001S, U20-ch20
calib_packv5_042523_0143.root, FC#2, port C2
Entries 733
Mean 45
Std Dev 10.95
Turn on : 27.4719
Width : 2.692
Height : 19.990
Entry
ampl
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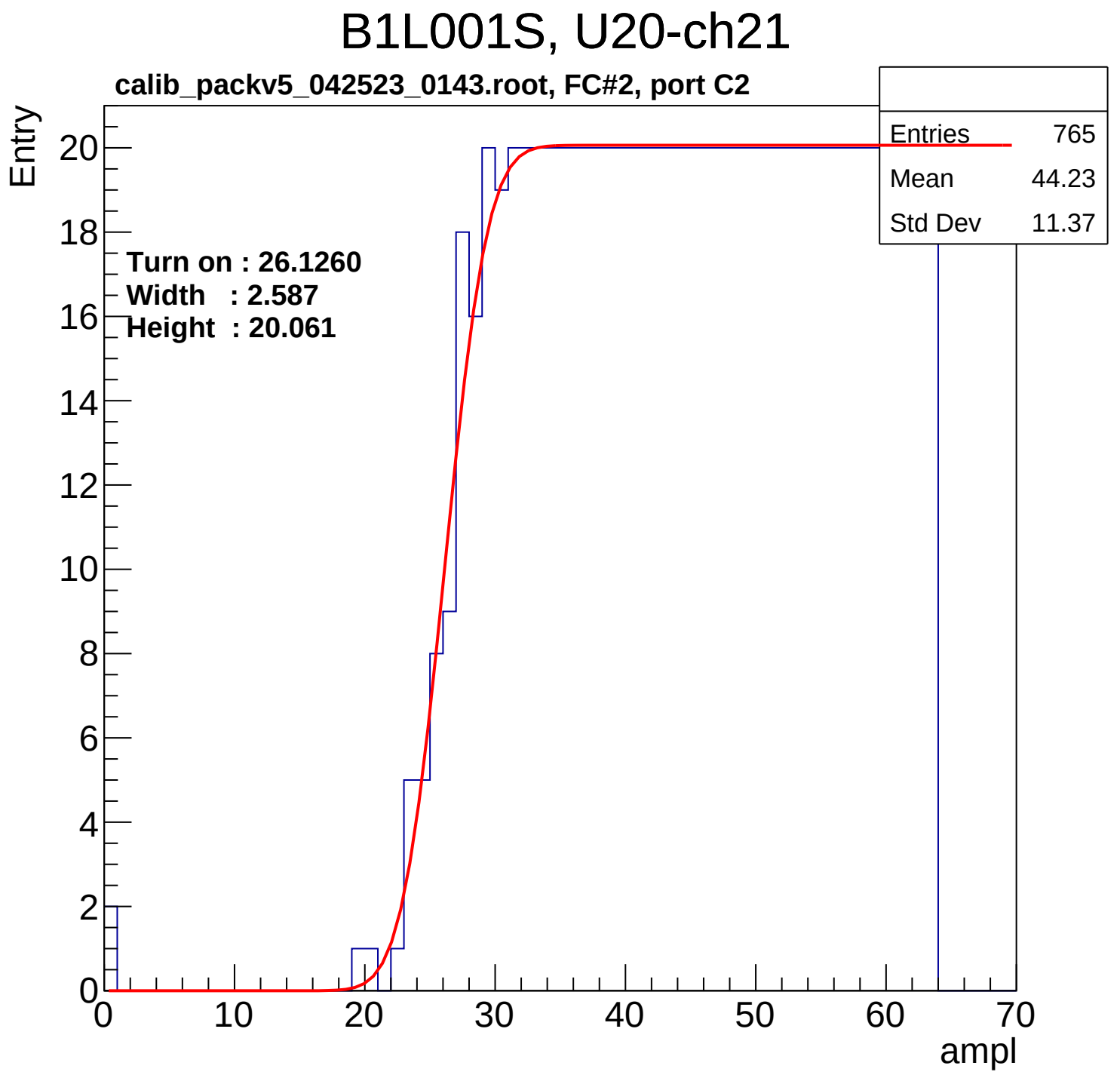
B1L001S, U20-ch21
calib_packv5_042523_0143.root, FC#2, port C2
Entries 765
Mean 44.23
Std Dev 11.37
Turn on : 26.1260
Width : 2.587
Height : 20.061
Entry
ampl
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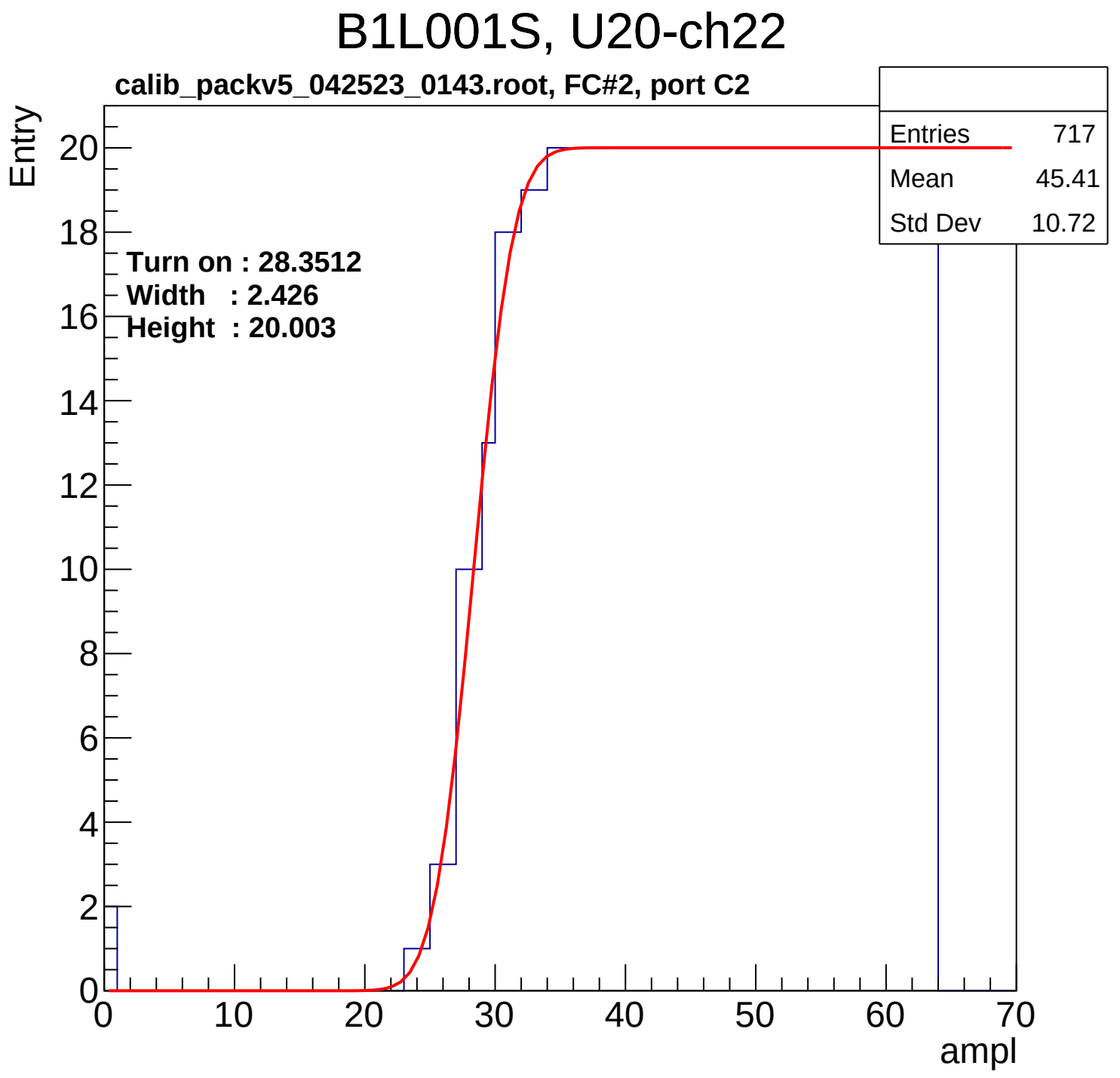
B1L001S, U20-ch22
calib_packv5_042523_0143.root, FC#2, port C2
Entries 717
Mean 45.41
Std Dev 10.72
Turn on : 28.3512
Width : 2.426
Height : 20.003
Entry
ampl
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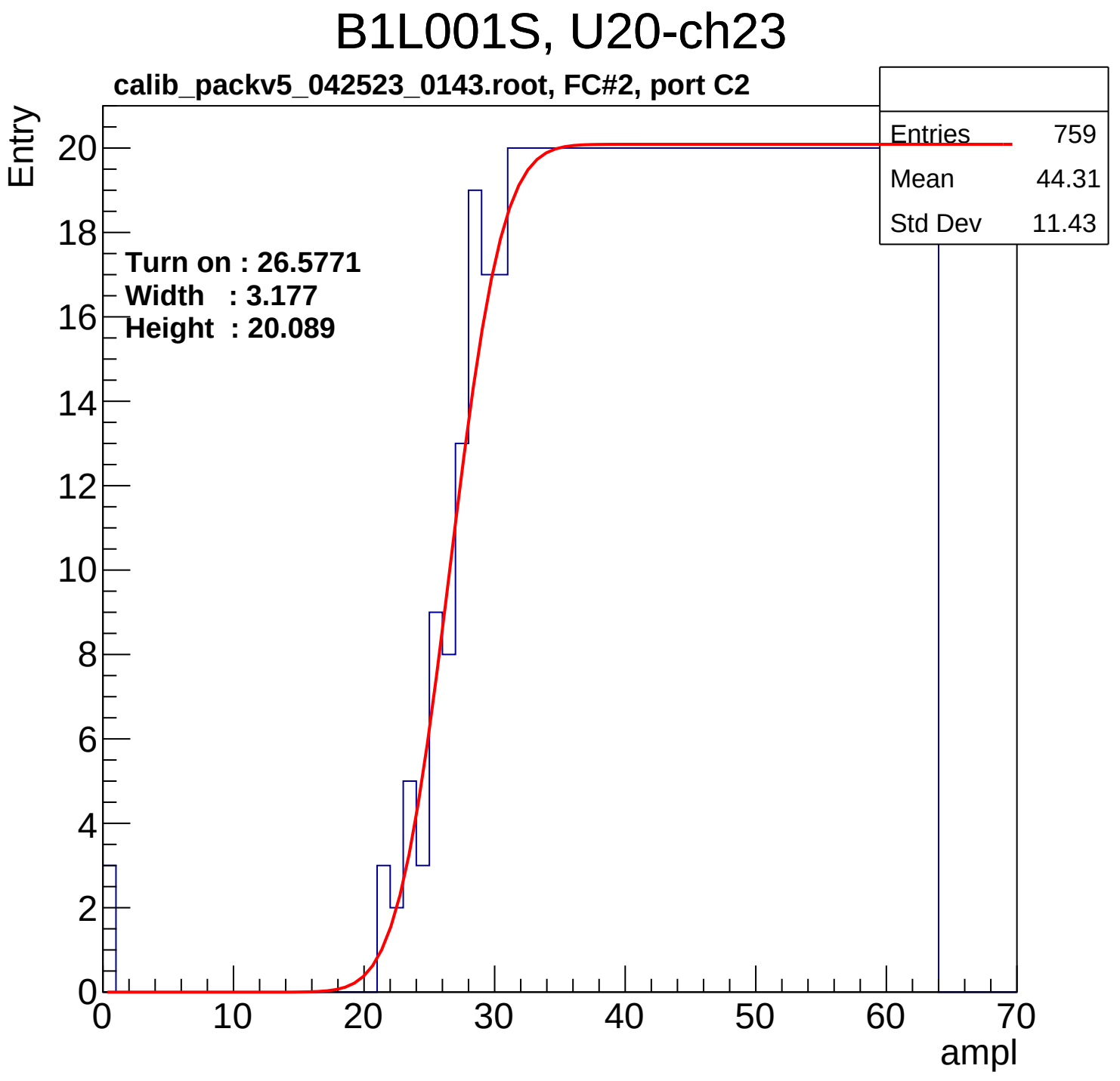
B1L001S, U20-ch23
calib_packv5_042523_0143.root, FC#2, port C2
Entries 759
Mean 44.31
Std Dev 11.43
Turn on : 26.5771
Width : 3.177
Height : 20.089
Entry
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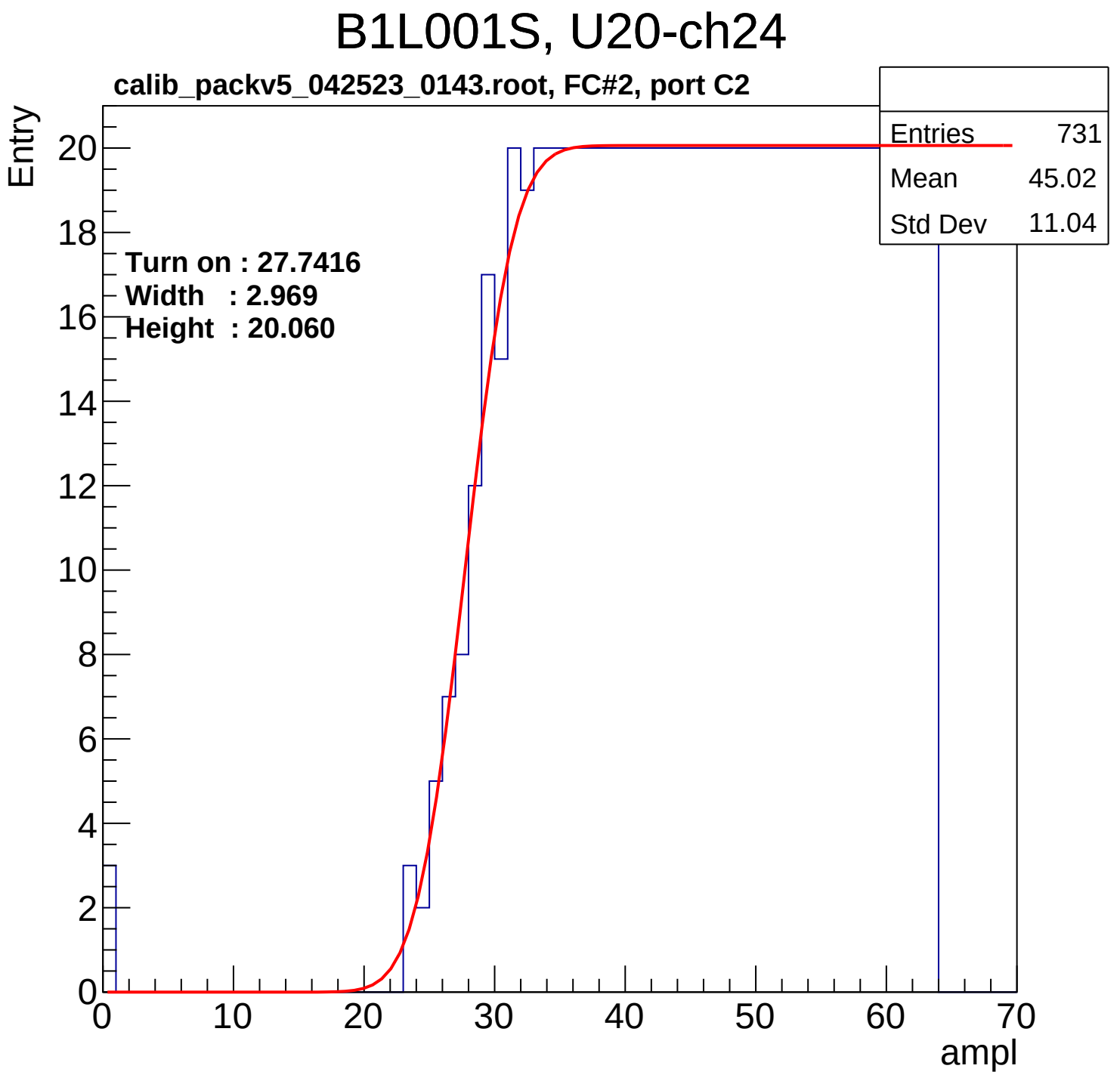
B1L001S, U20-ch24
calib_packv5_042523_0143.root, FC#2, port C2
Entries 731
Mean 45.02
Std Dev 11.04
Turn on : 27.7416
Width : 2.969
Height : 20.060
Entry
ampl
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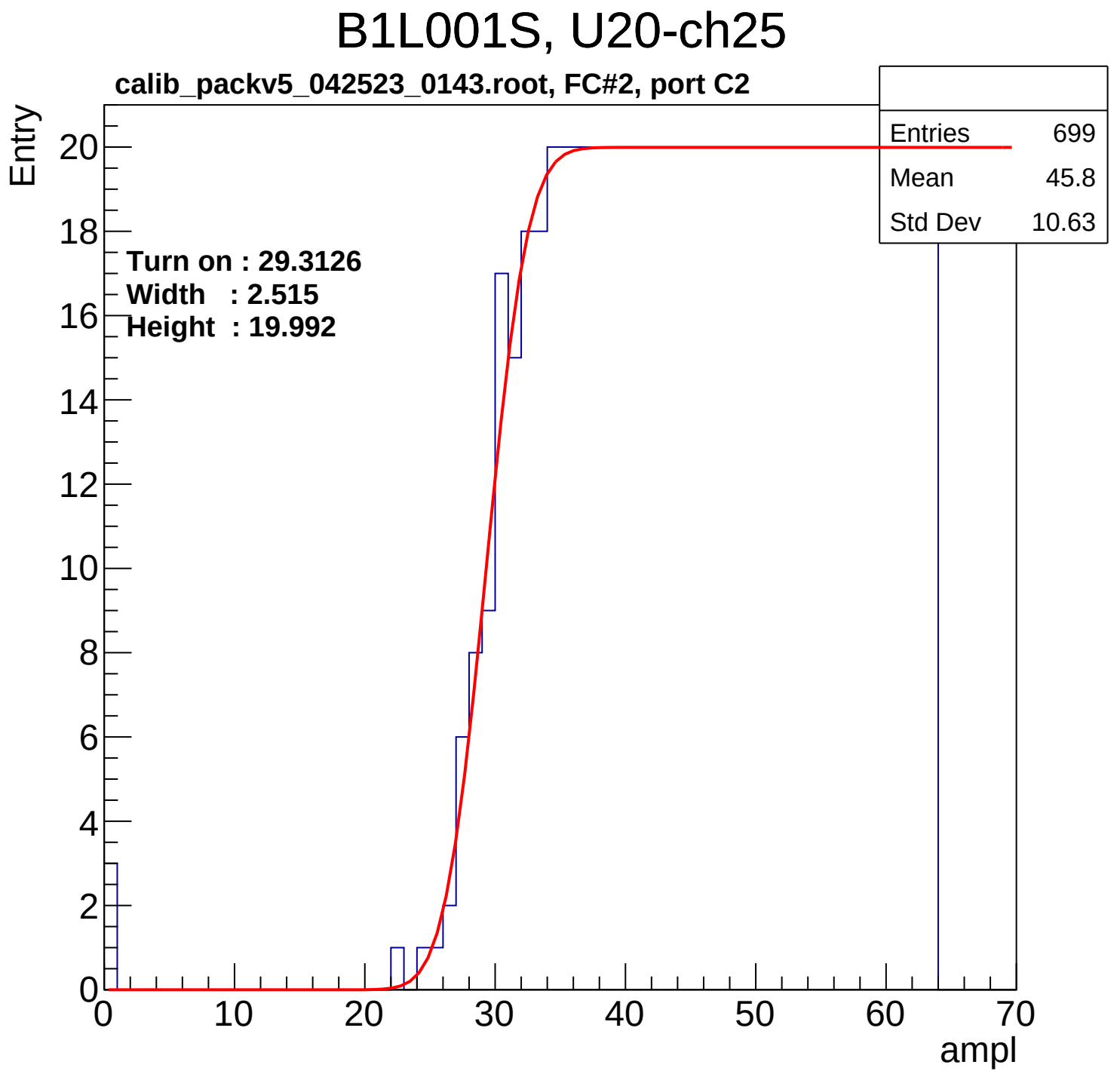
B1L001S, U20-ch25
calib_packv5_042523_0143.root, FC#2, port C2
Entries 699
Mean 45.8
Std Dev 10.63
Turn on : 29.3126
Width : 2.515
Height : 19.992
Entry
ampl
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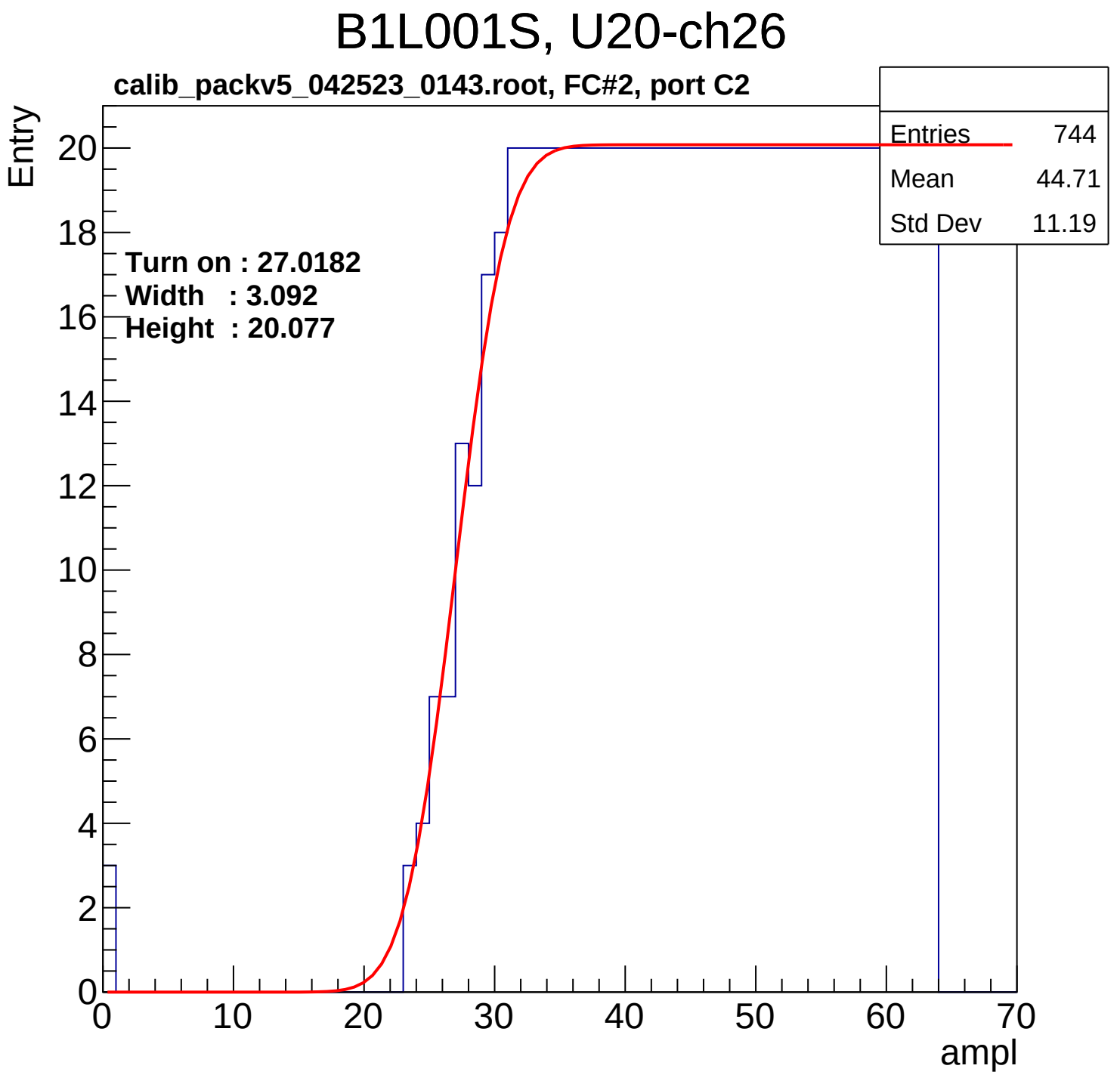
B1L001S, U20-ch26
calib_packv5_042523_0143.root, FC#2, port C2
Entries 744
Mean 44.71
Std Dev 11.19
Turn on : 27.0182
Width : 3.092
Height : 20.077
Entry
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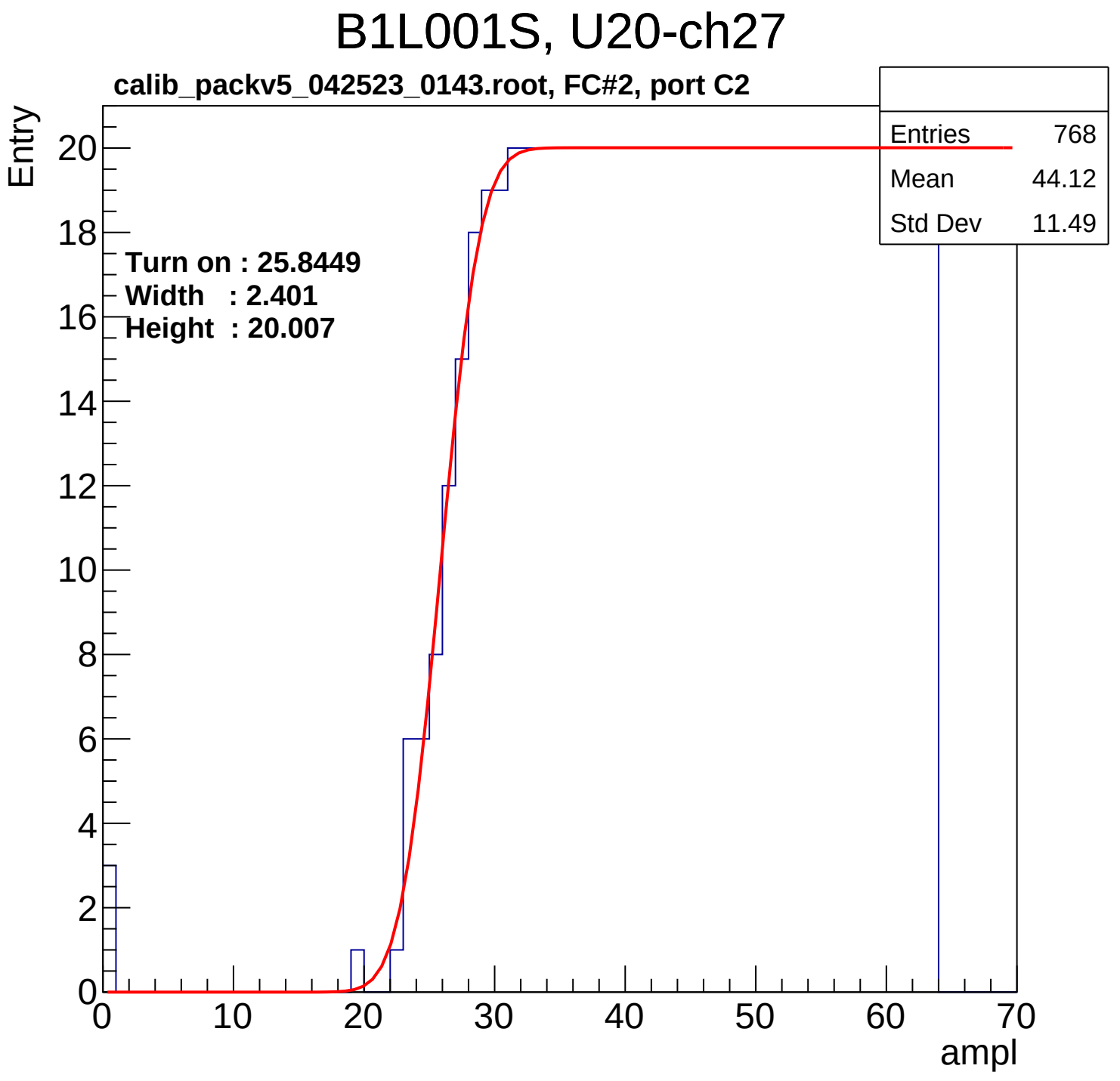
B1L001S, U20-ch27
calib_packv5_042523_0143.root, FC#2, port C2
Entries 768
Mean 44.12
Std Dev 11.49
Turn on : 25.8449
Width : 2.401
Height : 20.007
Entry
ampl
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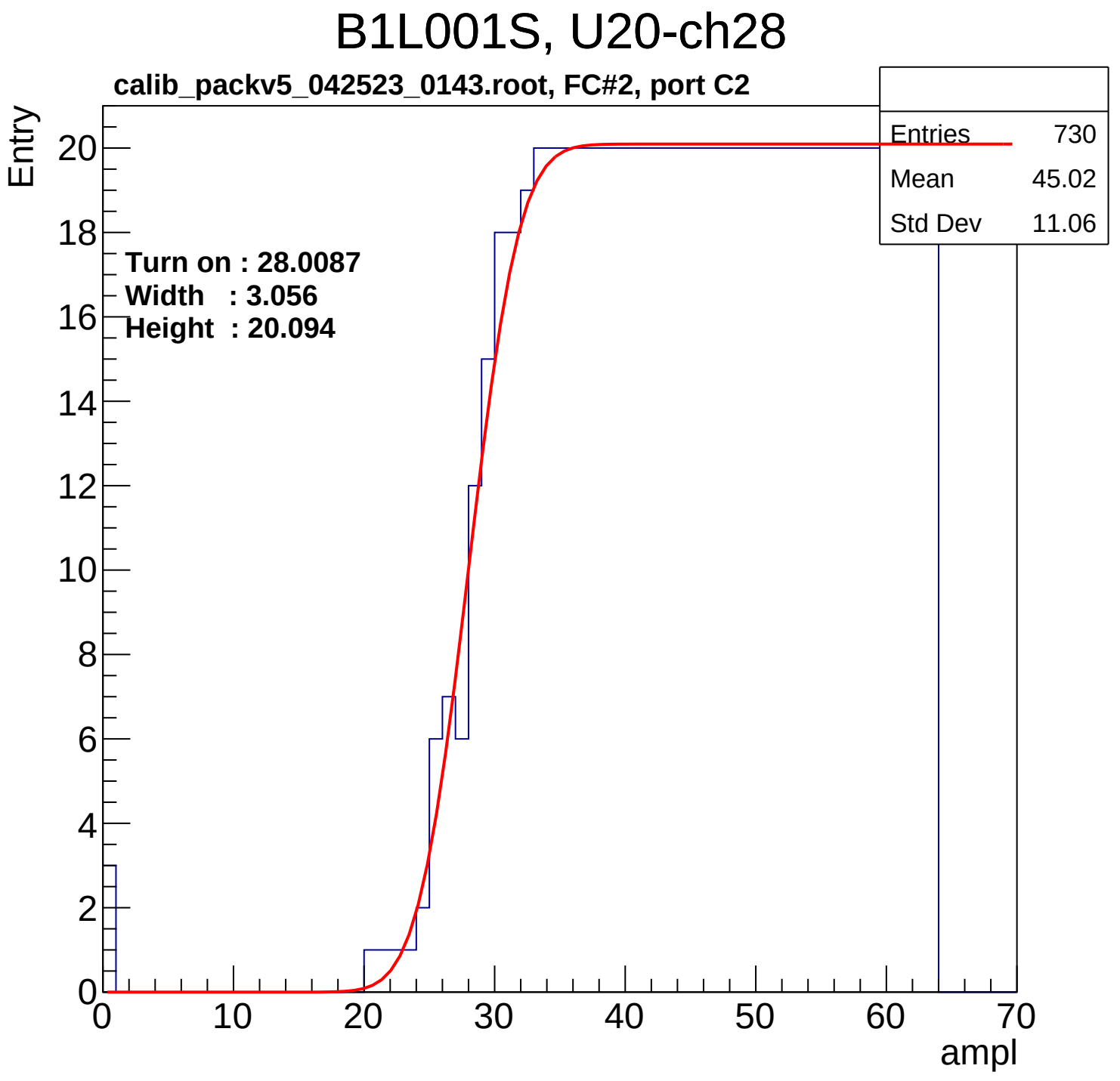
B1L001S, U20-ch28
calib_packv5_042523_0143.root, FC#2, port C2
Entries 730
Mean 45.02
Std Dev 11.06
Turn on : 28.0087
Width : 3.056
Height : 20.094
Entry
ampl
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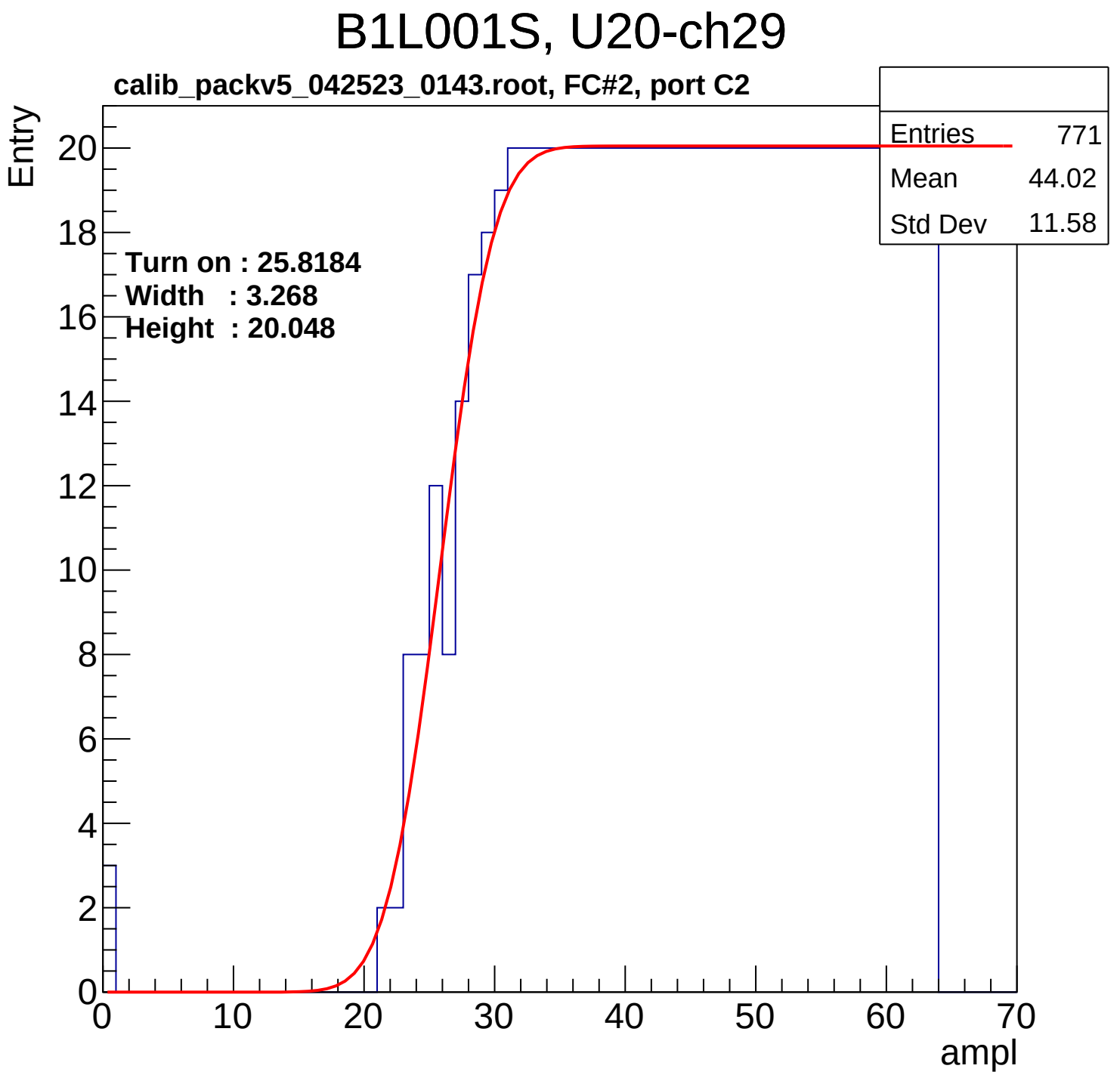
B1L001S, U20-ch29
calib_packv5_042523_0143.root, FC#2, port C2
Entries 771
Mean 44.02
Std Dev 11.58
Turn on : 25.8184
Width : 3.268
Height : 20.048
Entry
ampl
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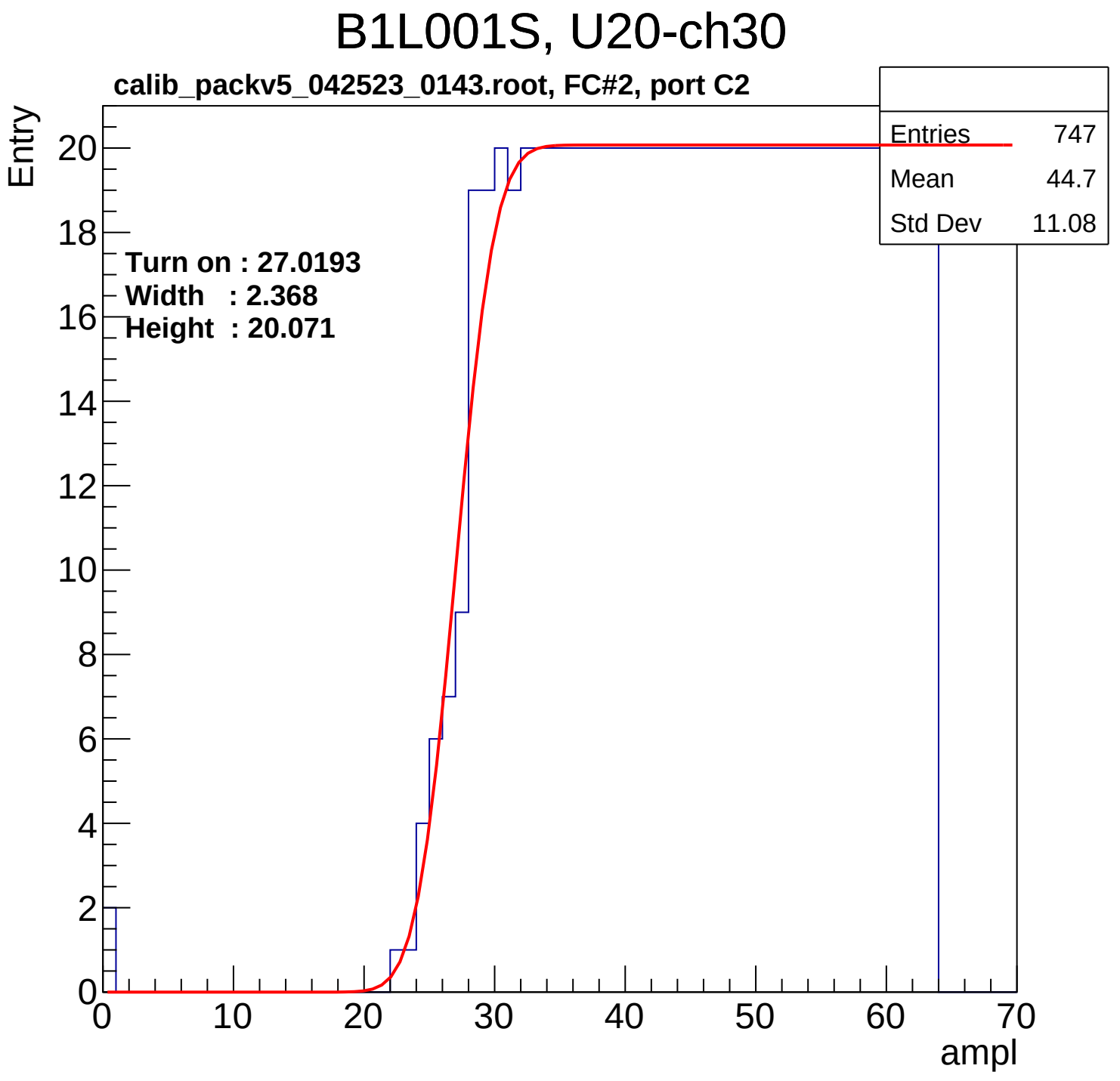
B1L001S, U20-ch30
calib_packv5_042523_0143.root, FC#2, port C2
Entries 747
Mean 44.7
Std Dev 11.08
Turn on : 27.0193
Width : 2.368
Height : 20.071
Entry
ampl
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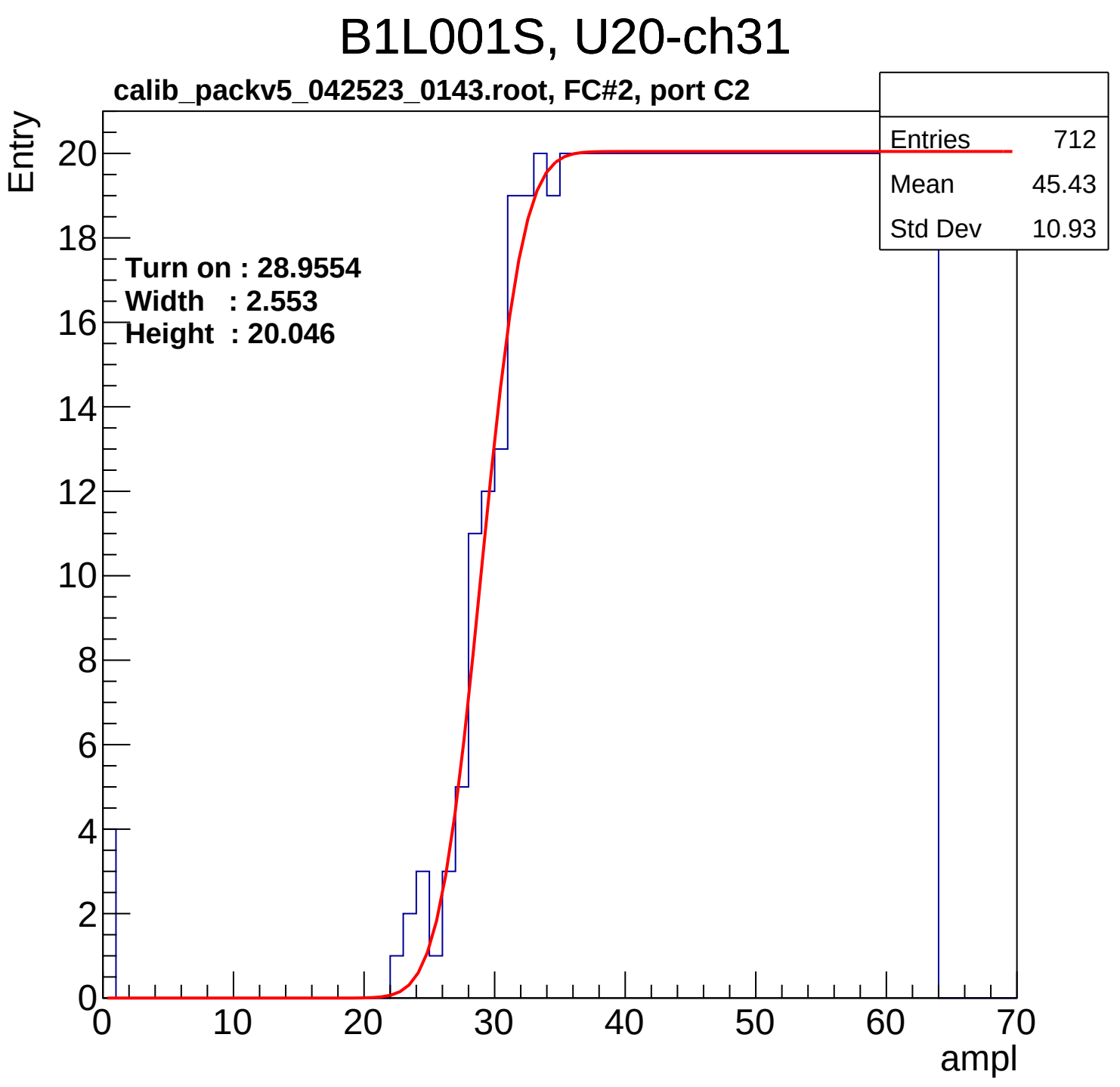
B1L001S, U20-ch31
calib_packv5_042523_0143.root, FC#2, port C2
Entries 712
Mean 45.43
Std Dev 10.93
Turn on : 28.9554
Width : 2.553
Height : 20.046
Entry
ampl
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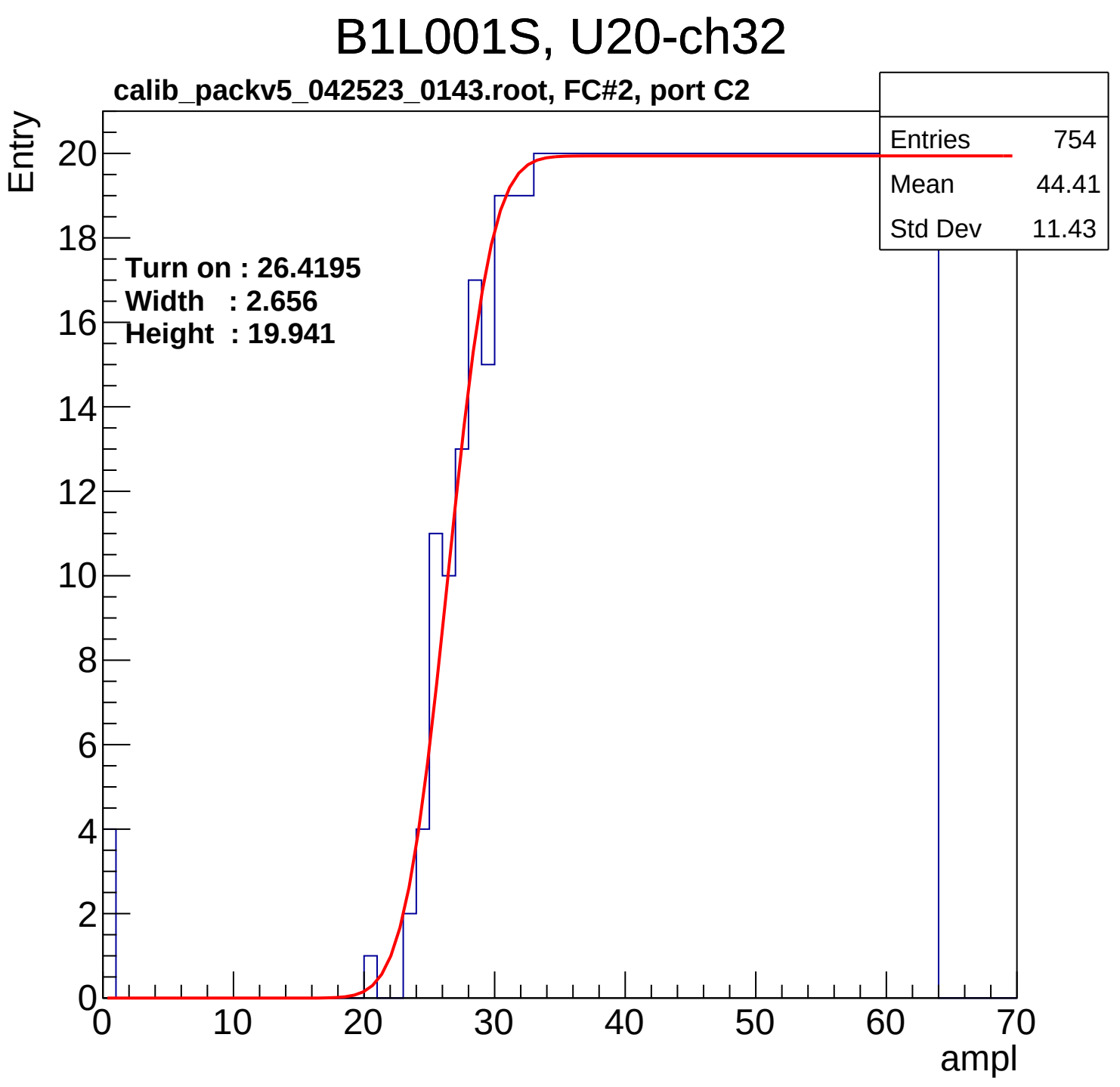
B1L001S, U20-ch32
calib_packv5_042523_0143.root, FC#2, port C2
Entries 754
Mean 44.41
Std Dev 11.43
Turn on : 26.4195
Width : 2.656
Height : 19.941
Entry
ampl
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6
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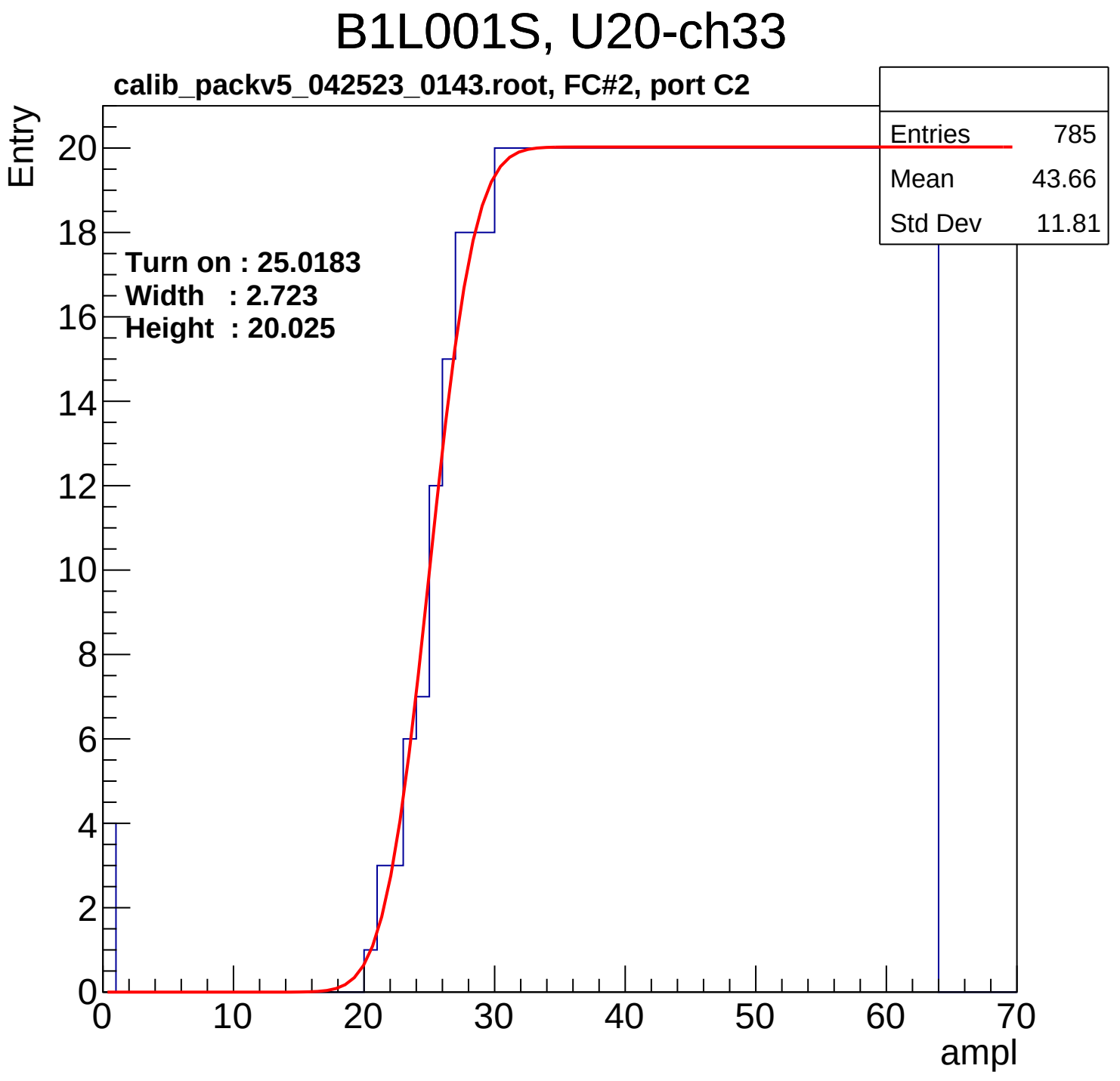
B1L001S, U20-ch33
calib_packv5_042523_0143.root, FC#2, port C2
Entries 785
Mean 43.66
Std Dev 11.81
Turn on : 25.0183
Width : 2.723
Height : 20.025
Entry
ampl
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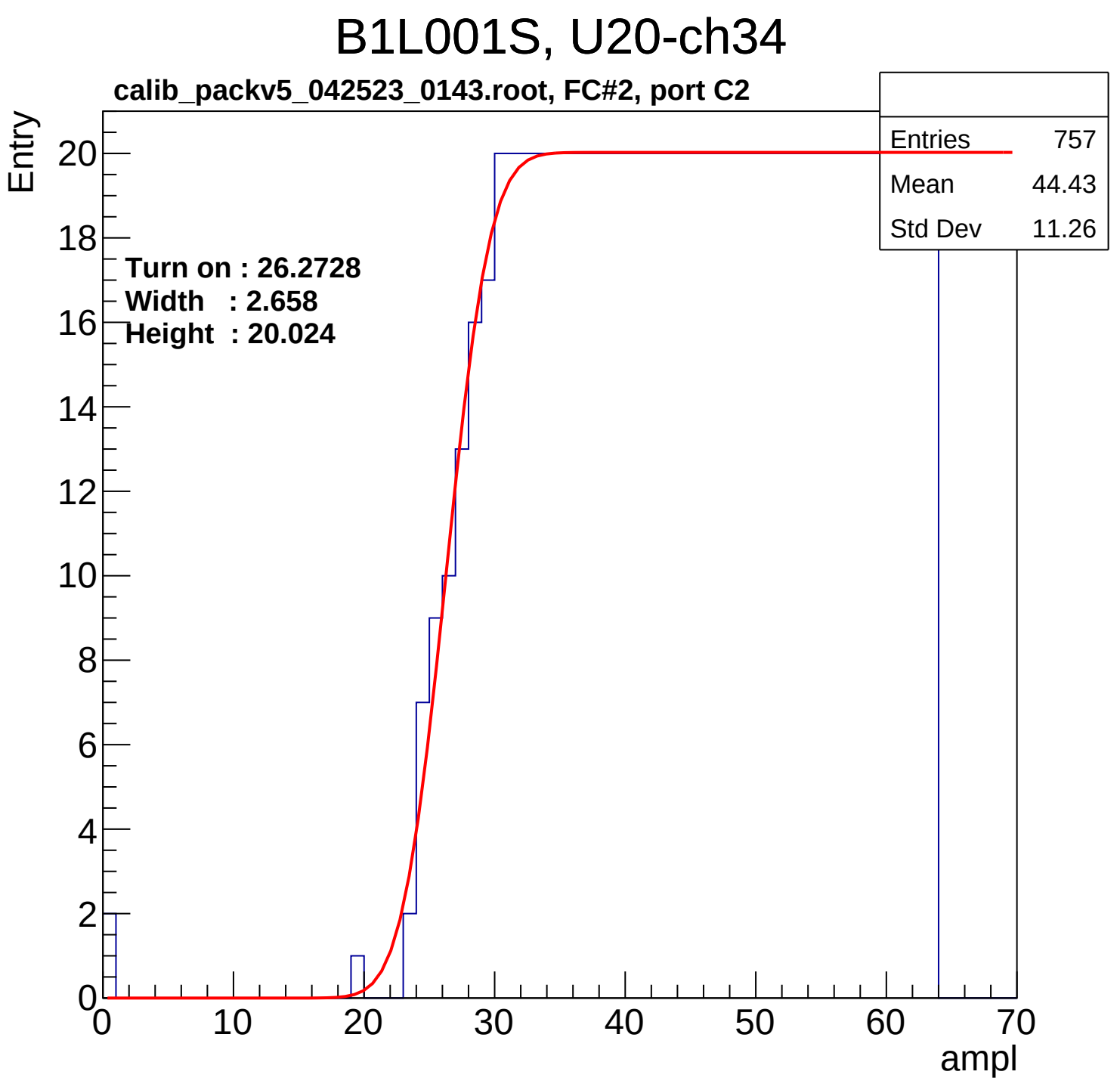
B1L001S, U20-ch34
calib_packv5_042523_0143.root, FC#2, port C2
Entries 757
Mean 44.43
Std Dev 11.26
Turn on : 26.2728
Width : 2.658
Height : 20.024
Entry
ampl
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6
8
10
12
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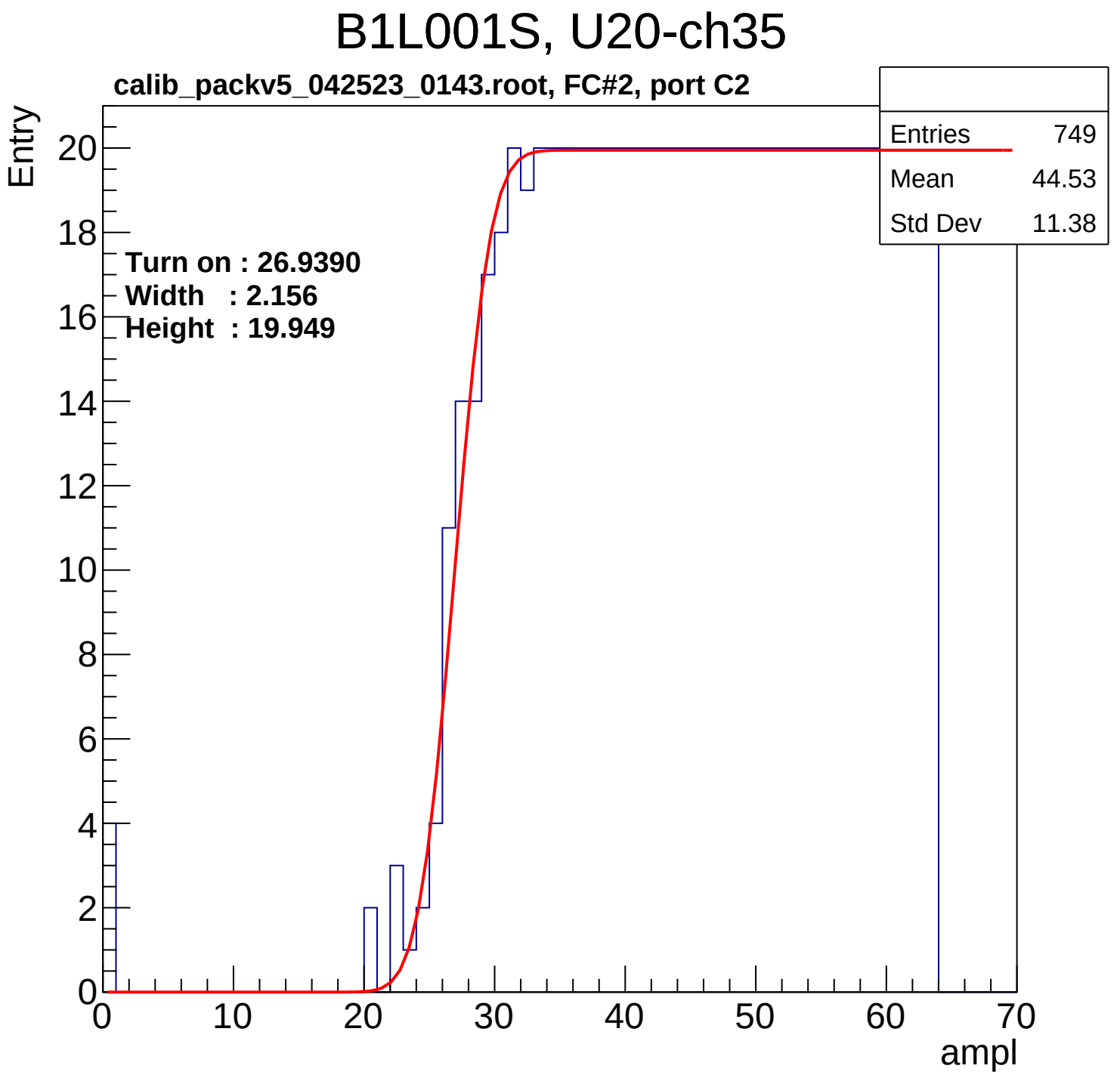
B1L001S, U20-ch35
calib_packv5_042523_0143.root, FC#2, port C2
Entries 749
Mean 44.53
Std Dev 11.38
Turn on : 26.9390
Width : 2.156
Height : 19.949
Entry
ampl
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6
8
10
12
14
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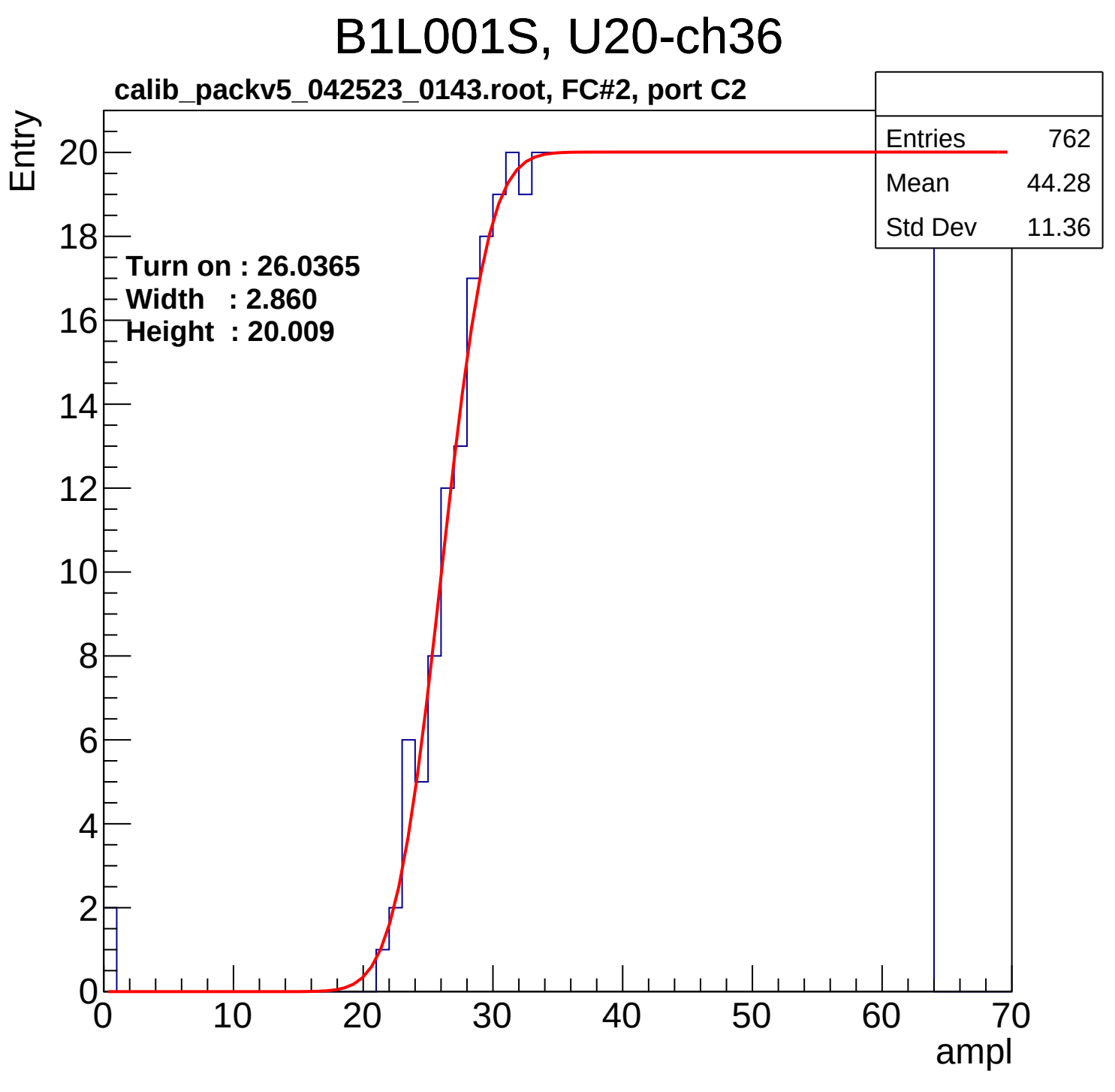
B1L001S, U20-ch36
calib_packv5_042523_0143.root, FC#2, port C2
Entries 762
Mean 44.28
Std Dev 11.36
Turn on : 26.0365
Width : 2.860
Height : 20.009
Entry
ampl
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6
8
10
12
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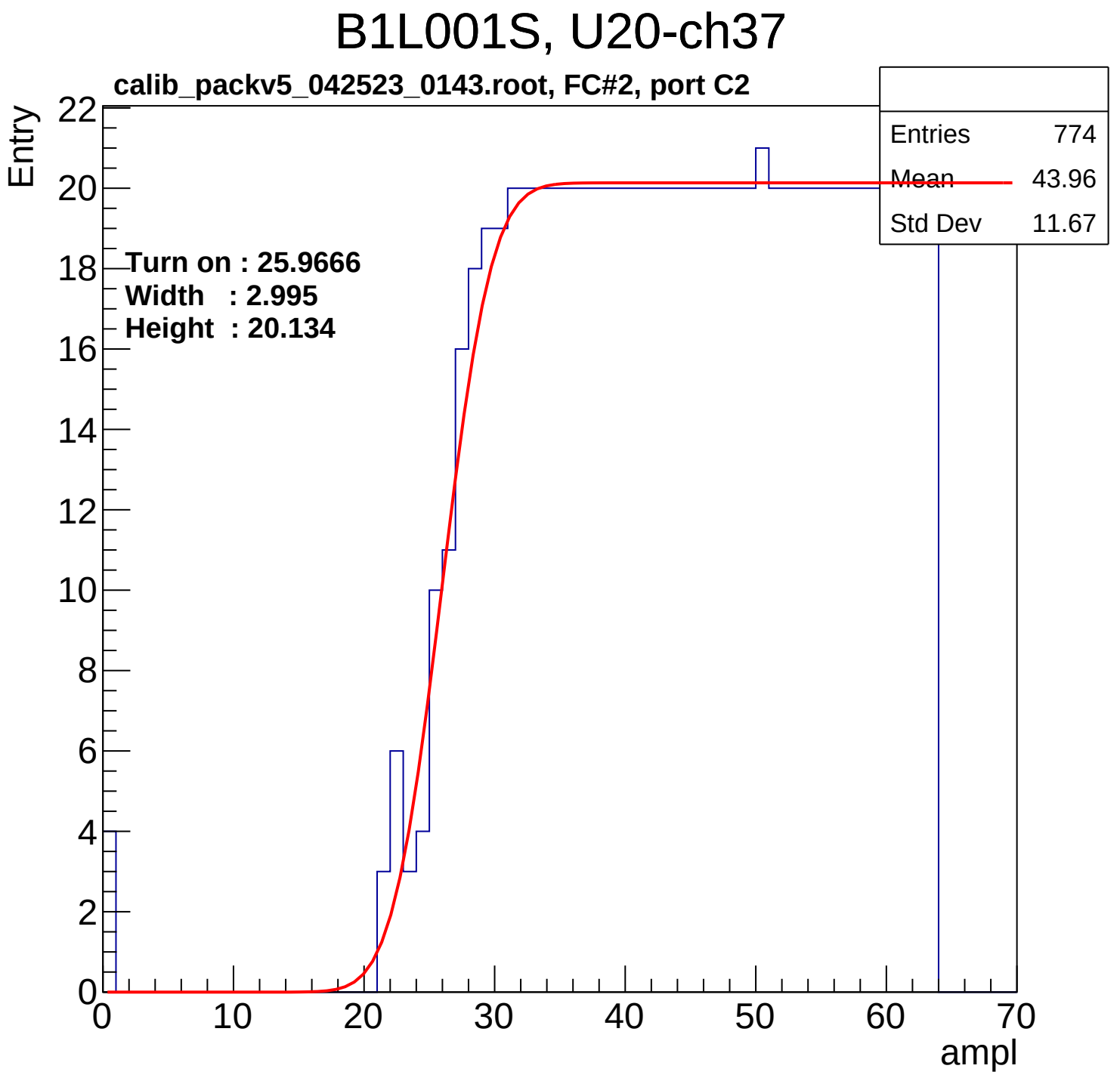
B1L001S, U20-ch37
calib_packv5_042523_0143.root, FC#2, port C2
Entries 774
Mean 43.96
Std Dev 11.67
Turn on : 25.9666
Width : 2.995
Height : 20.134
Entry
ampl
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8
10
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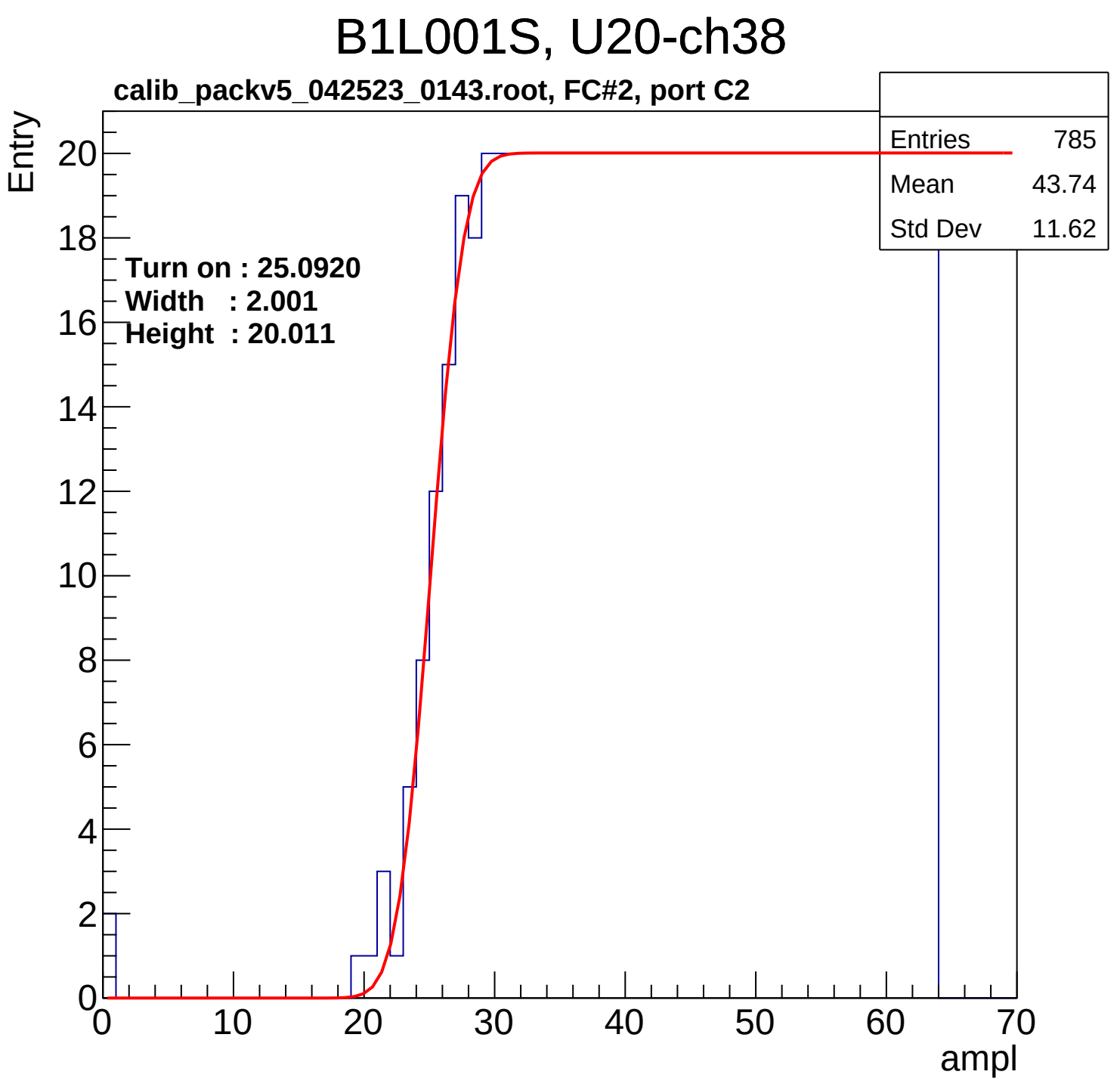
B1L001S, U20-ch38
calib_packv5_042523_0143.root, FC#2, port C2
Entries 785
Mean 43.74
Std Dev 11.62
Turn on : 25.0920
Width : 2.001
Height : 20.011
Entry
ampl
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6
8
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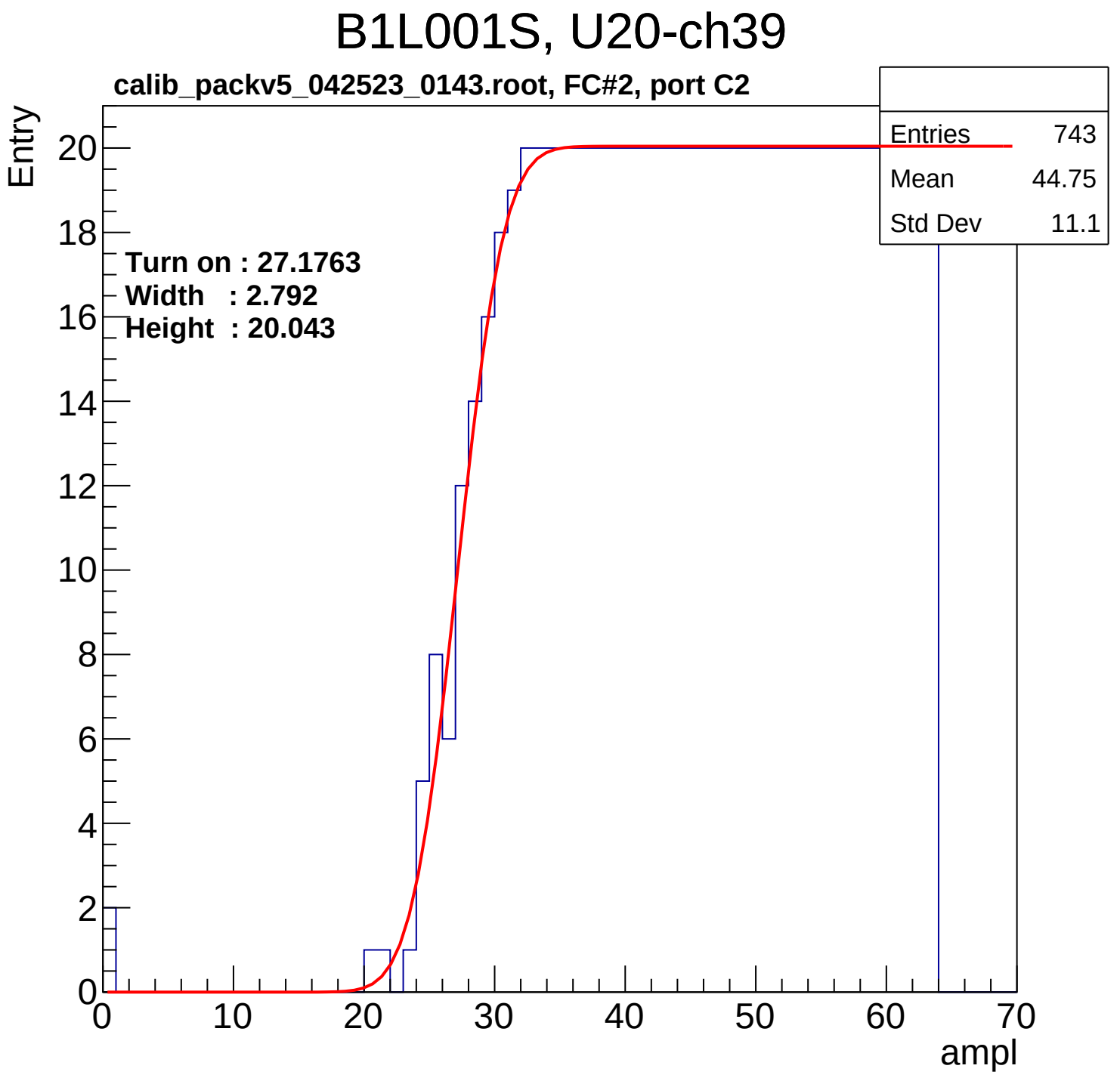
B1L001S, U20-ch39
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.75
Std Dev 11.1
Turn on : 27.1763
Width : 2.792
Height : 20.043
Entry
ampl
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6
8
10
12
14
16
18
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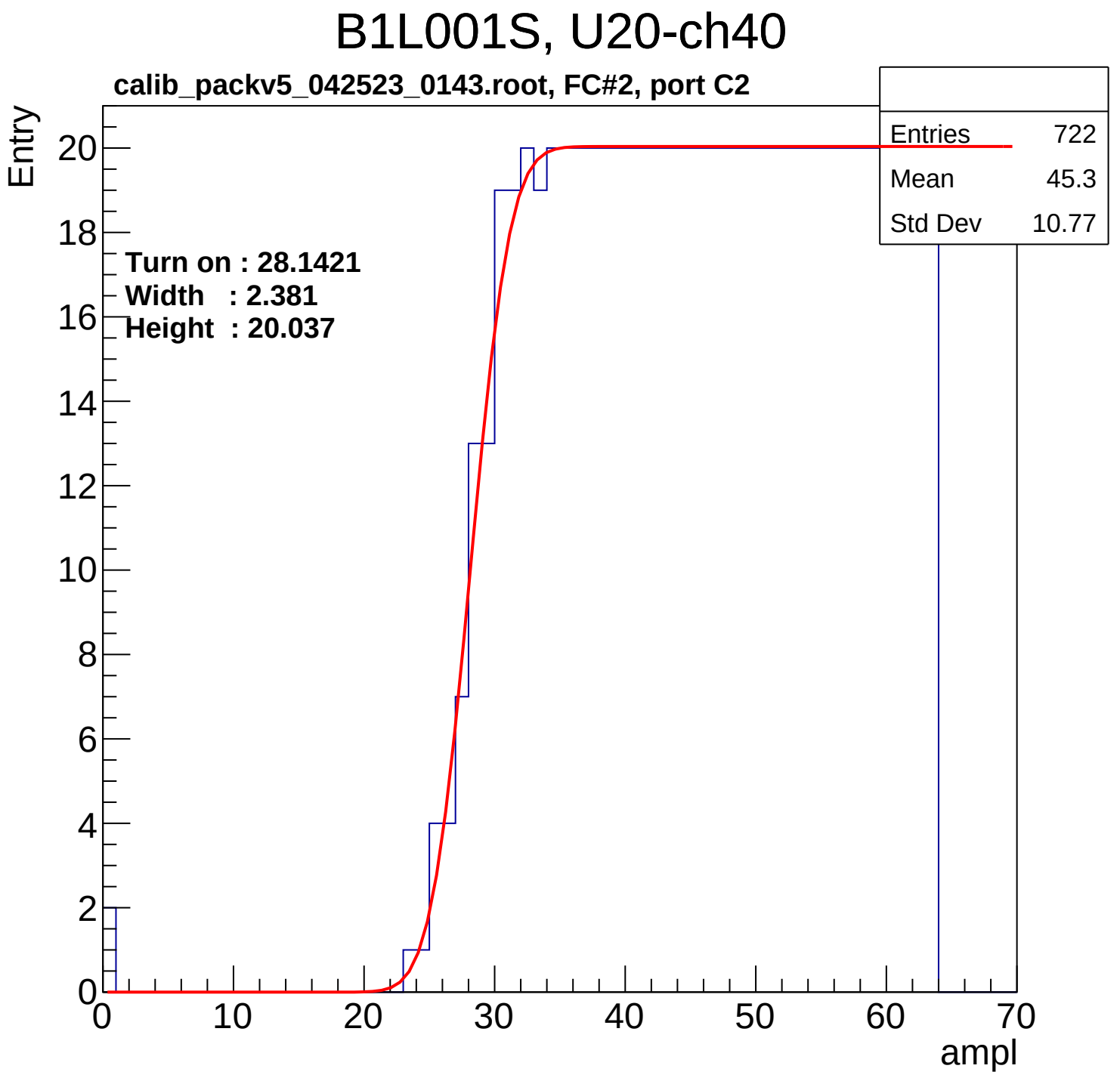
B1L001S, U20-ch40
calib_packv5_042523_0143.root, FC#2, port C2
Entries 722
Mean 45.3
Std Dev 10.77
Turn on : 28.1421
Width : 2.381
Height : 20.037
Entry
ampl
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8
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14
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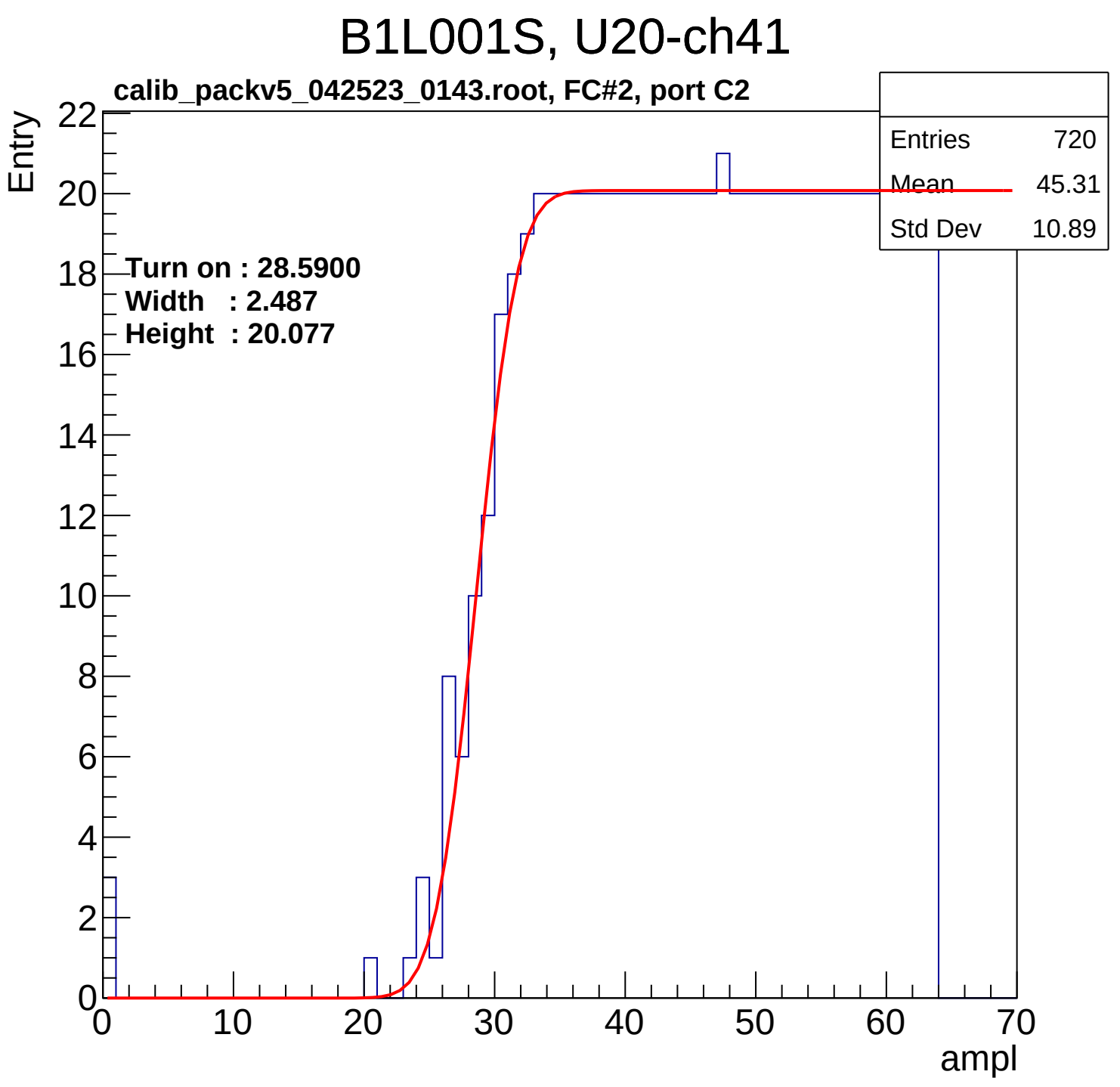
B1L001S, U20-ch41
calib_packv5_042523_0143.root, FC#2, port C2
Entries 720
Mean 45.31
Std Dev 10.89
Turn on : 28.5900
Width : 2.487
Height : 20.077
Entry
ampl
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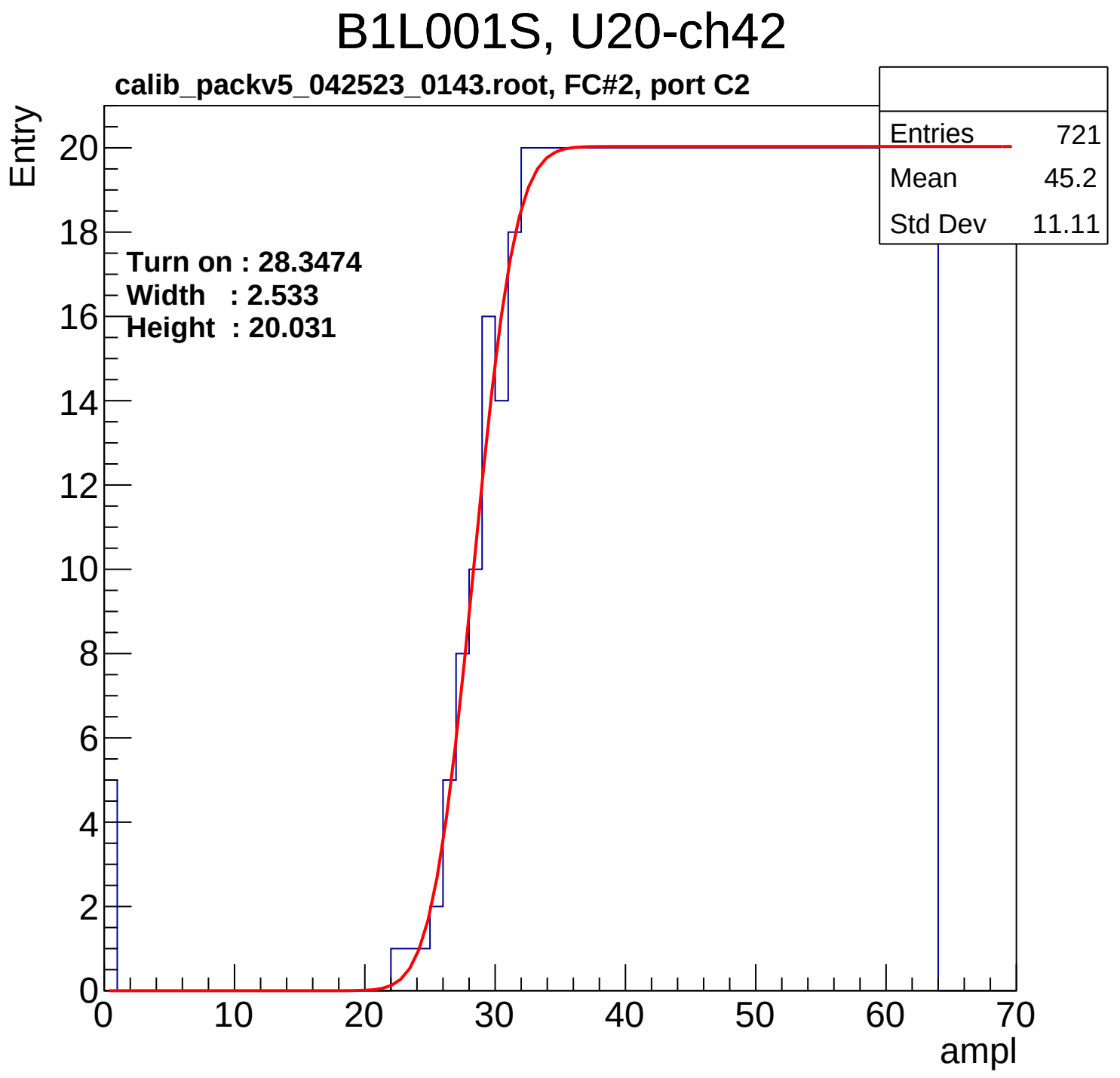
B1L001S, U20-ch42
calib_packv5_042523_0143.root, FC#2, port C2
Entries 721
Mean 45.2
Std Dev 11.11
Turn on : 28.3474
Width : 2.533
Height : 20.031
Entry
ampl
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6
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14
16
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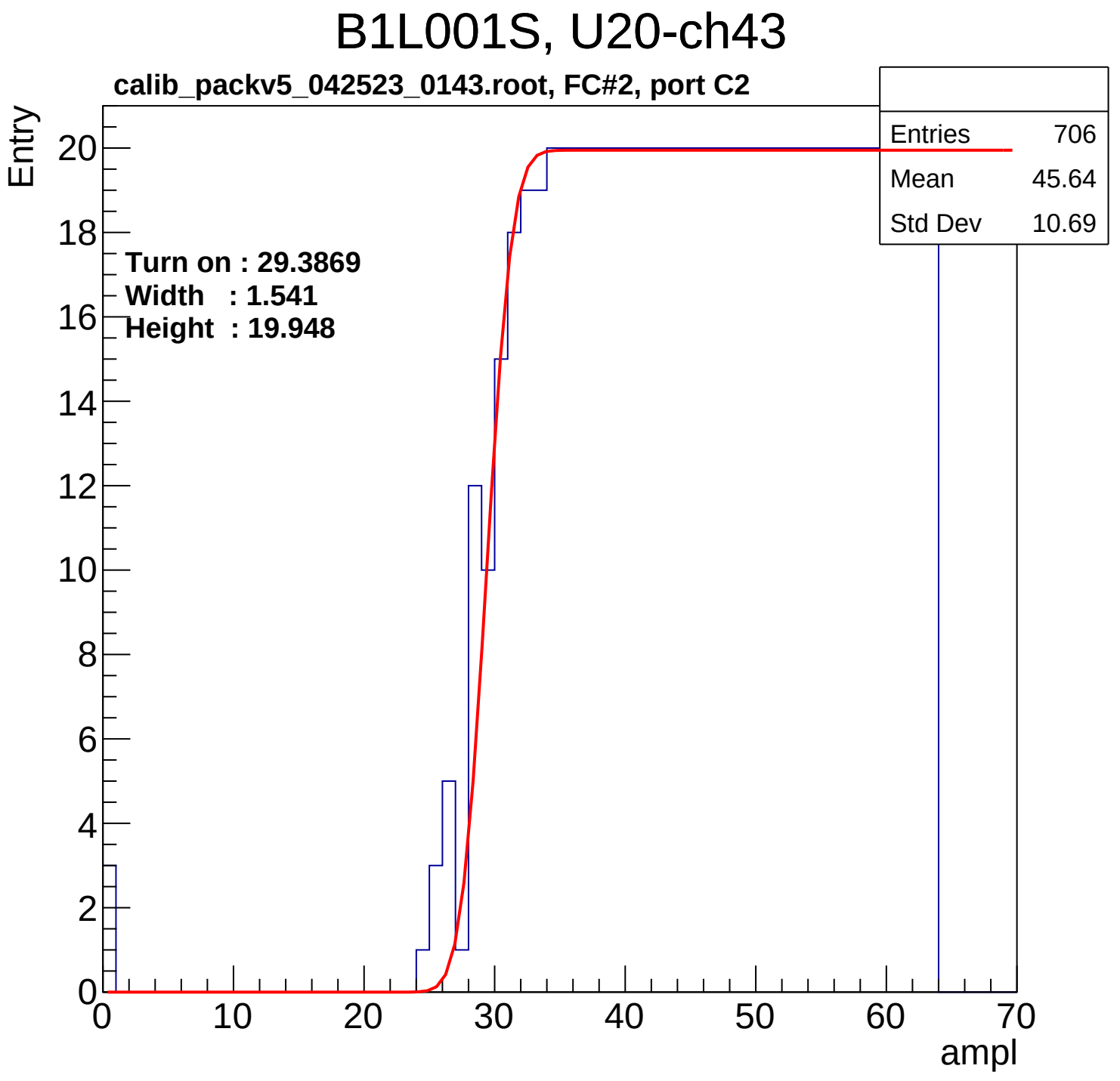
B1L001S, U20-ch43
calib_packv5_042523_0143.root, FC#2, port C2
Entries 706
Mean 45.64
Std Dev 10.69
Turn on : 29.3869
Width : 1.541
Height : 19.948
Entry
ampl
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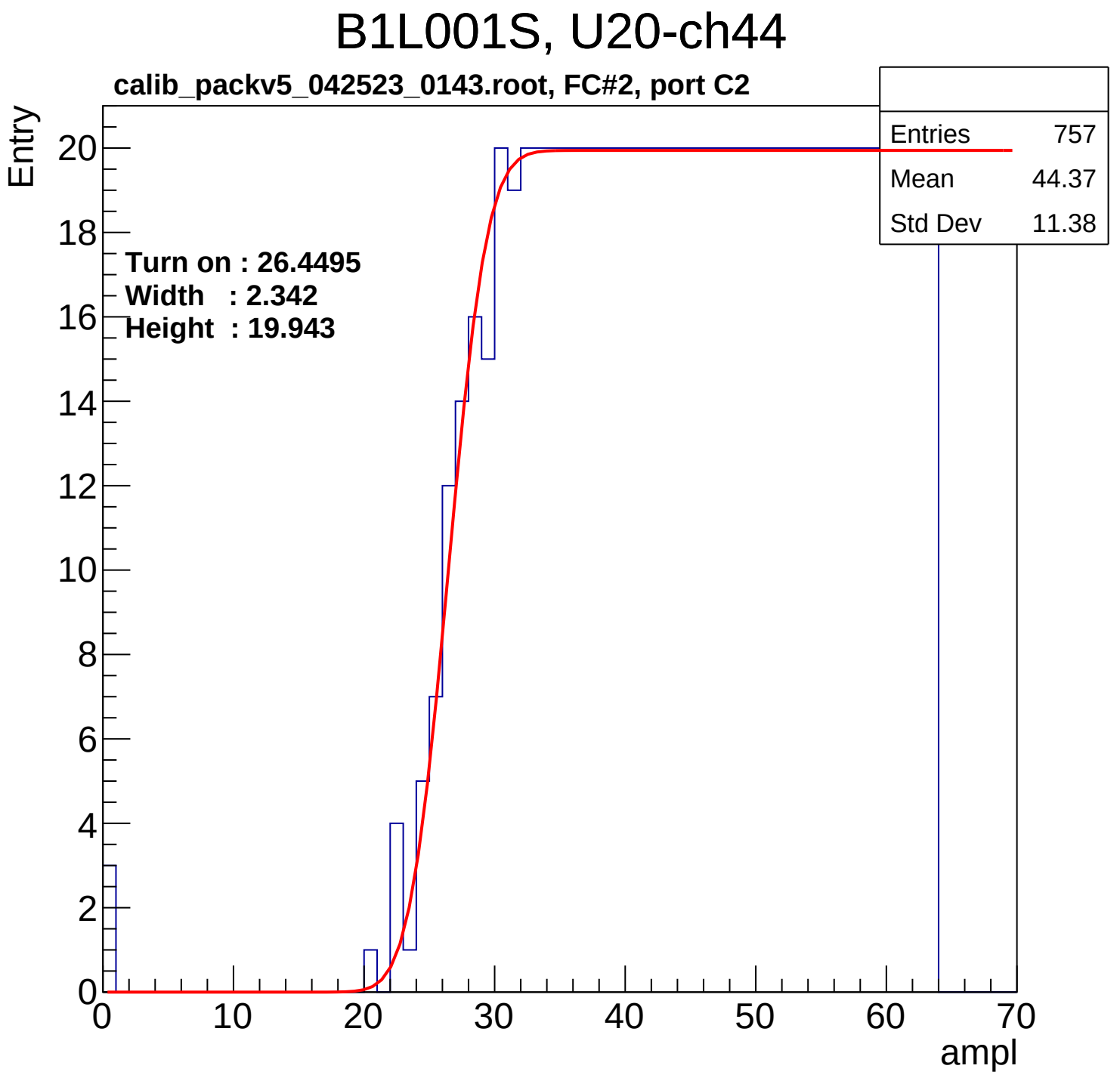
B1L001S, U20-ch44
calib_packv5_042523_0143.root, FC#2, port C2
Entries 757
Mean 44.37
Std Dev 11.38
Turn on : 26.4495
Width : 2.342
Height : 19.943
Entry
ampl
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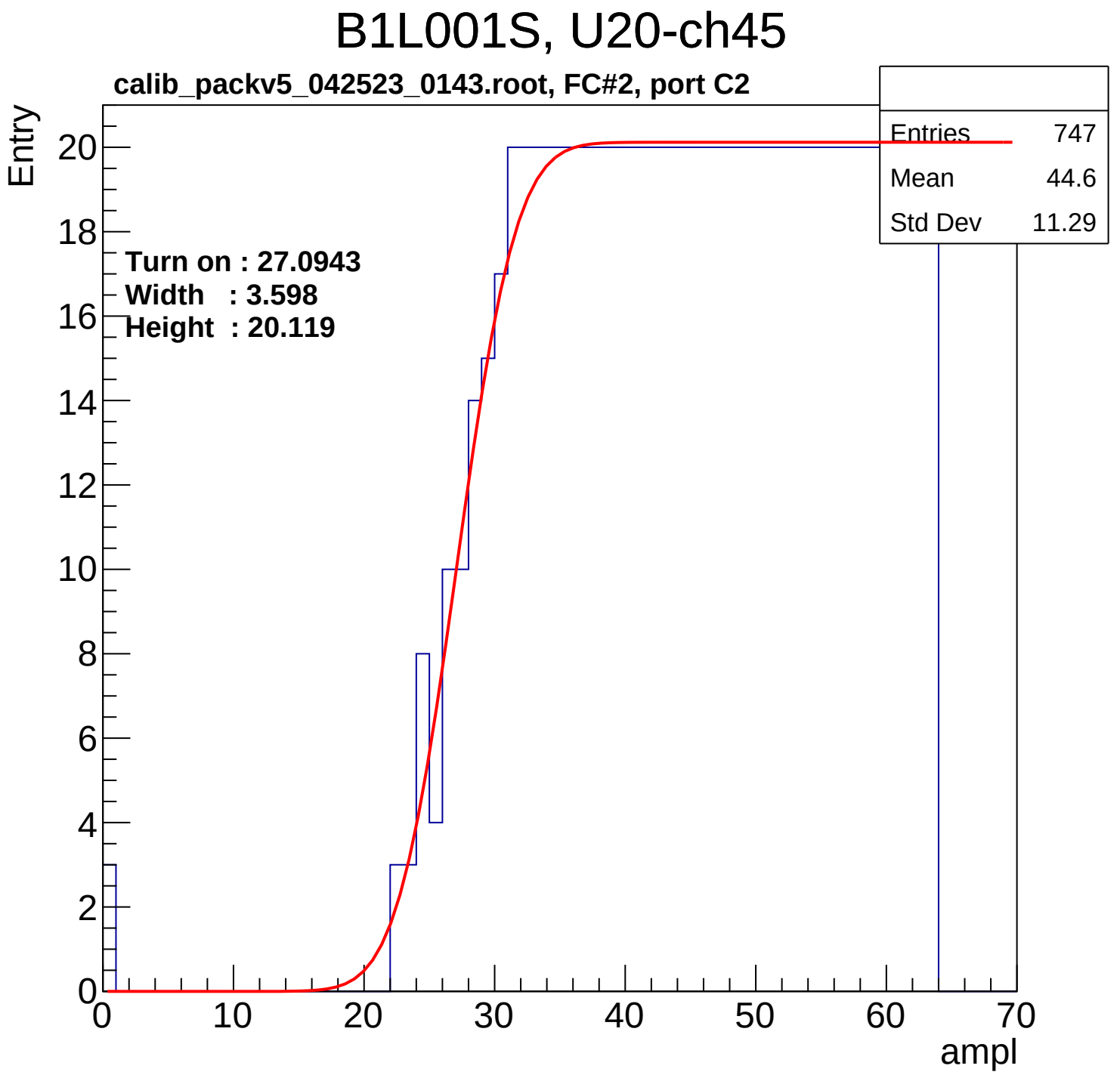
B1L001S, U20-ch45
calib_packv5_042523_0143.root, FC#2, port C2
Entries 747
Mean 44.6
Std Dev 11.29
Turn on : 27.0943
Width : 3.598
Height : 20.119
Entry
ampl
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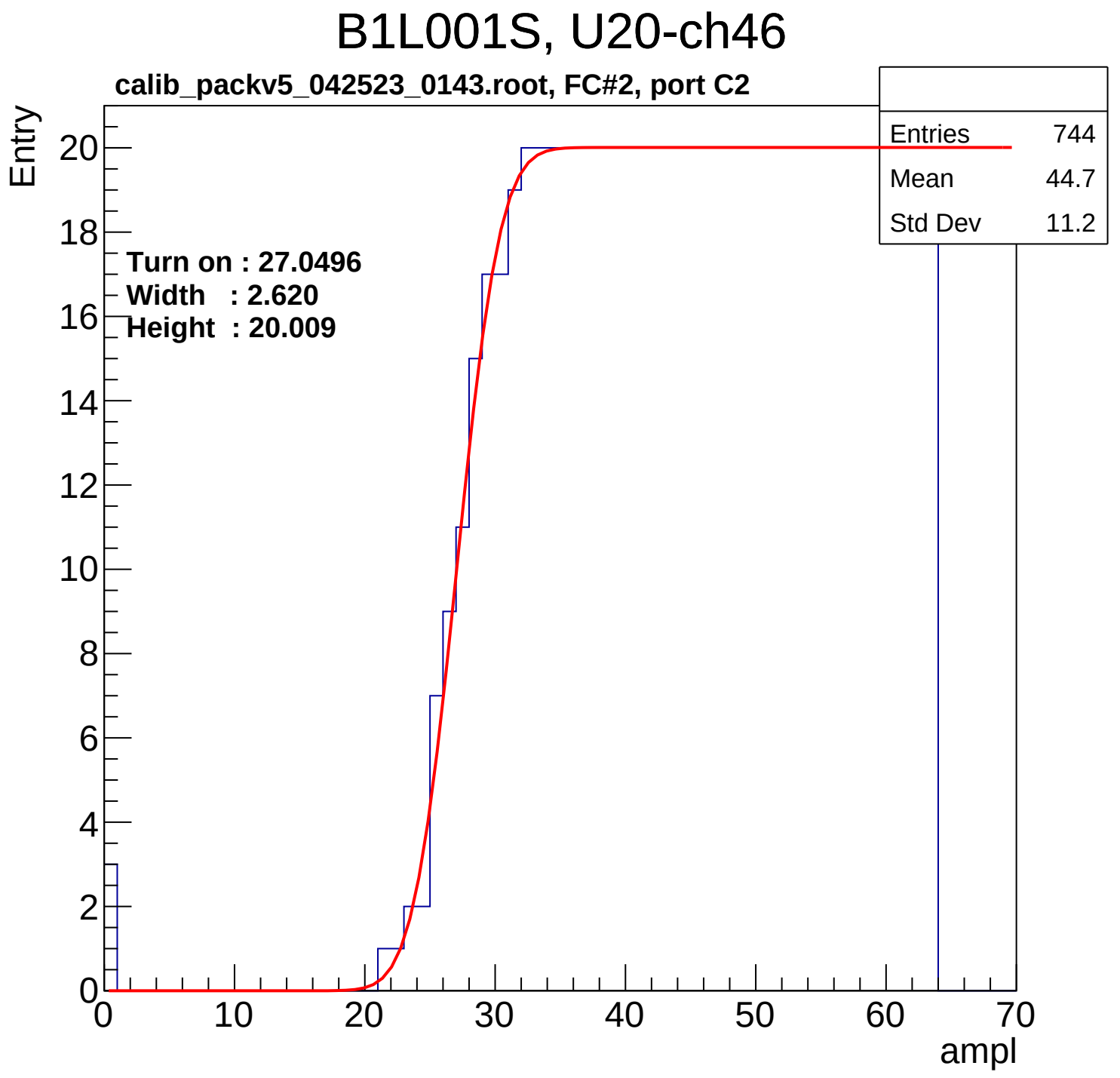
B1L001S, U20-ch46
calib_packv5_042523_0143.root, FC#2, port C2
Entries 744
Mean 44.7
Std Dev 11.2
Turn on : 27.0496
Width : 2.620
Height : 20.009
Entry
ampl
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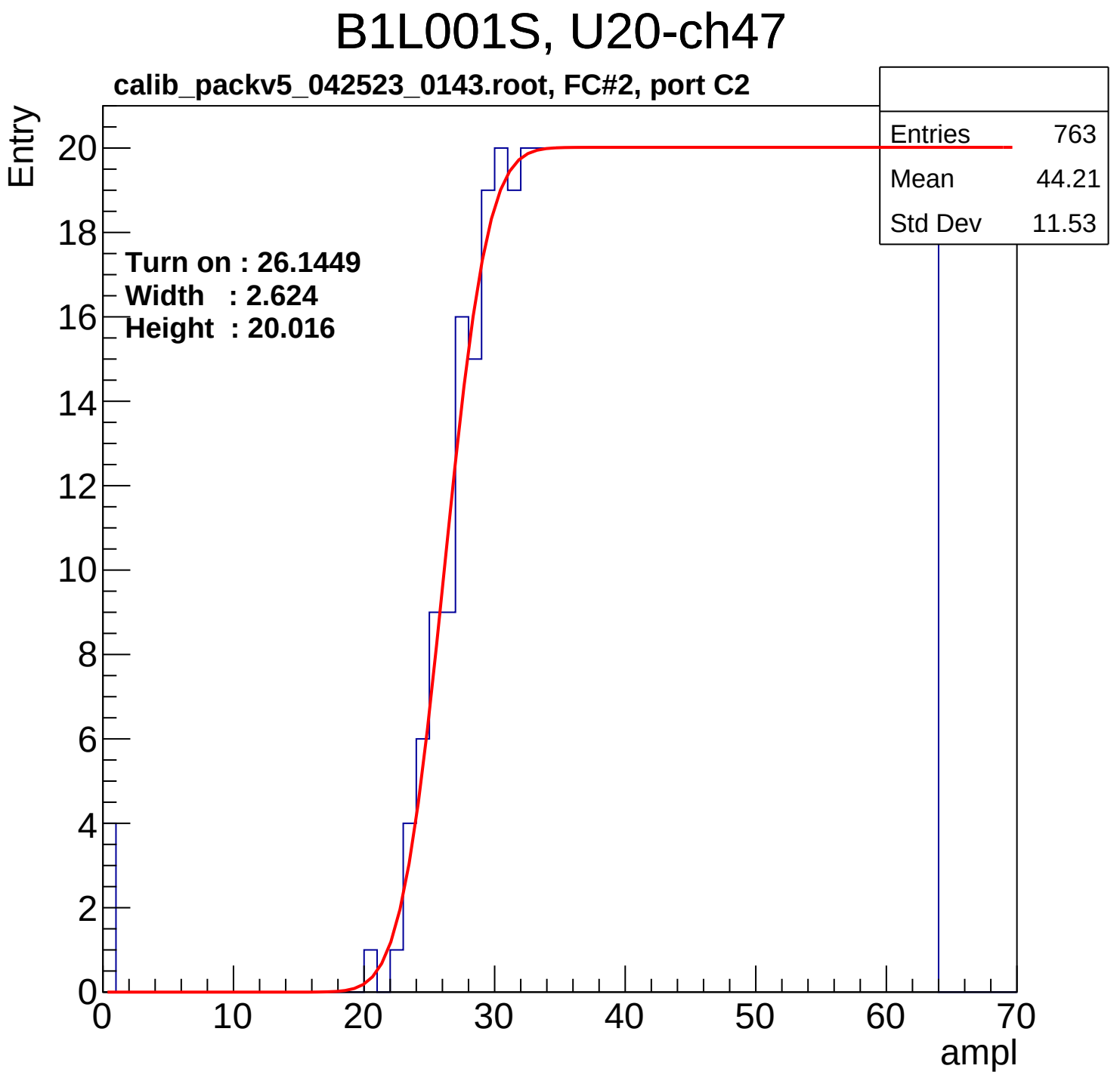
B1L001S, U20-ch47
calib_packv5_042523_0143.root, FC#2, port C2
Entries 763
Mean 44.21
Std Dev 11.53
Turn on : 26.1449
Width : 2.624
Height : 20.016
Entry
ampl
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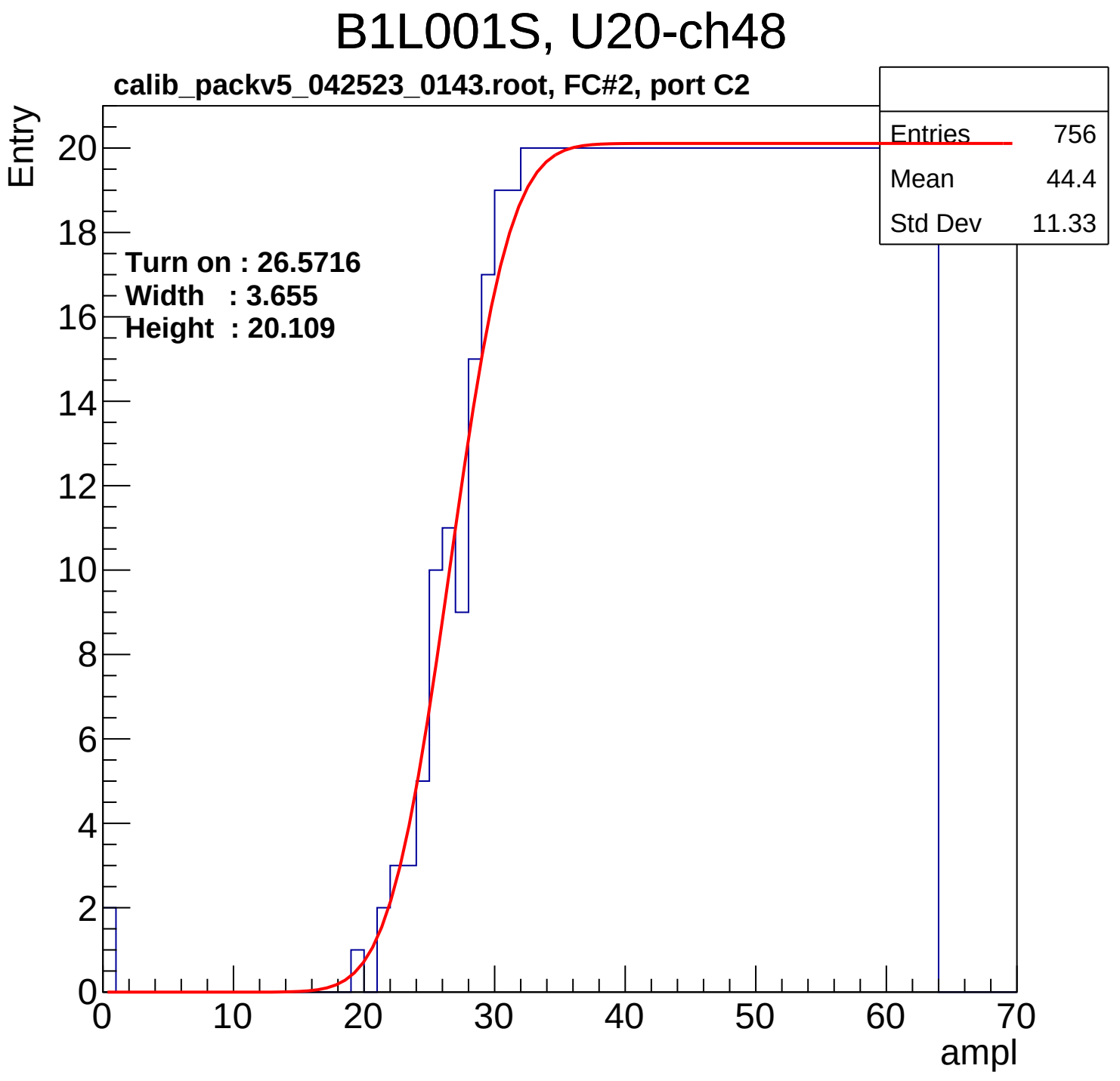
B1L001S, U20-ch48
calib_packv5_042523_0143.root, FC#2, port C2
Entries 756
Mean 44.4
Std Dev 11.33
Turn on : 26.5716
Width : 3.655
Height : 20.109
Entry
ampl
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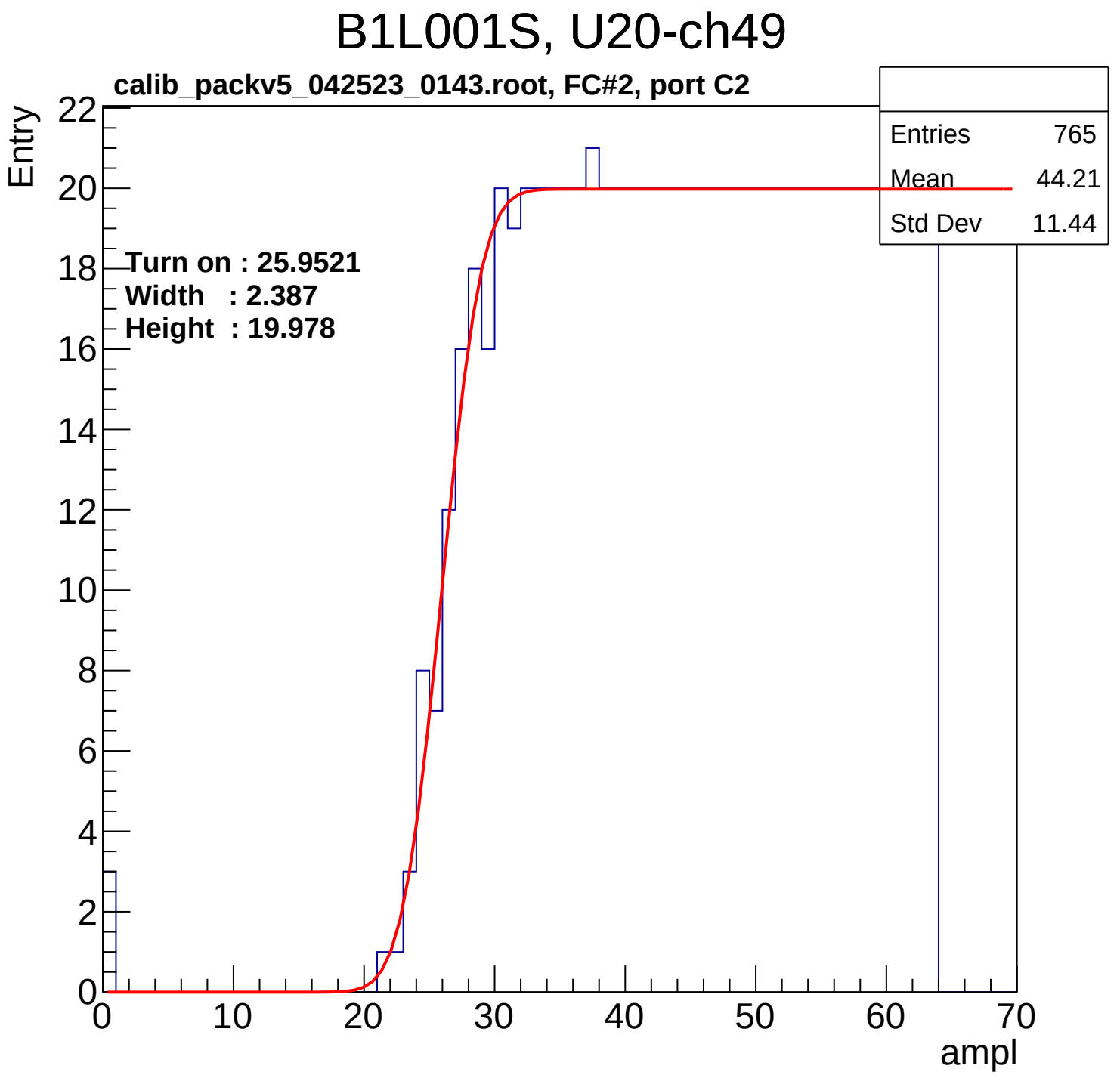
B1L001S, U20-ch49
calib_packv5_042523_0143.root, FC#2, port C2
Entries 765
Mean 44.21
Std Dev 11.44
Turn on : 25.9521
Width : 2.387
Height : 19.978
Entry
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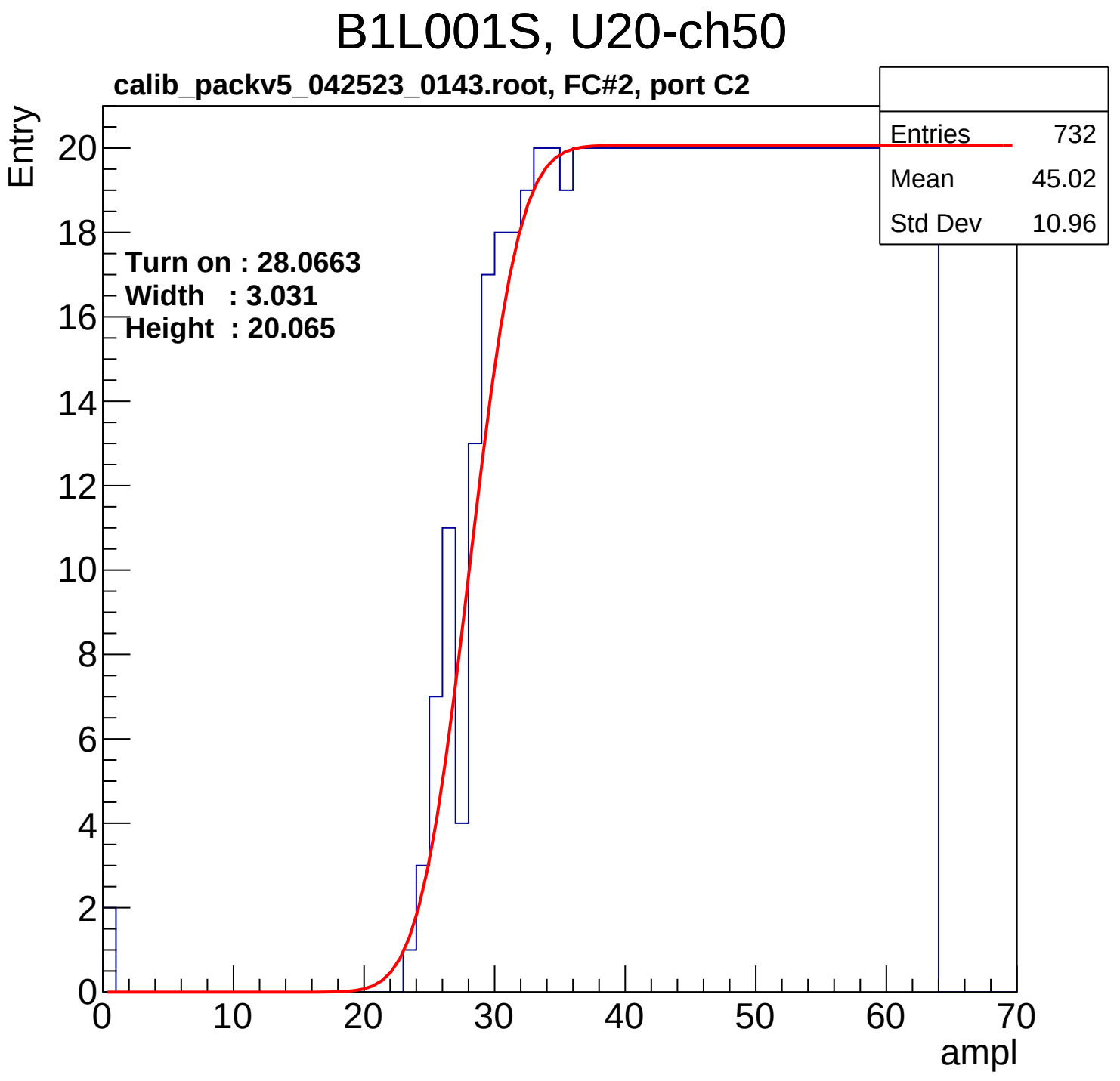
B1L001S, U20-ch50
calib_packv5_042523_0143.root, FC#2, port C2
Entries 732
Mean 45.02
Std Dev 10.96
Turn on : 28.0663
Width : 3.031
Height : 20.065
Entry
ampl
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6
8
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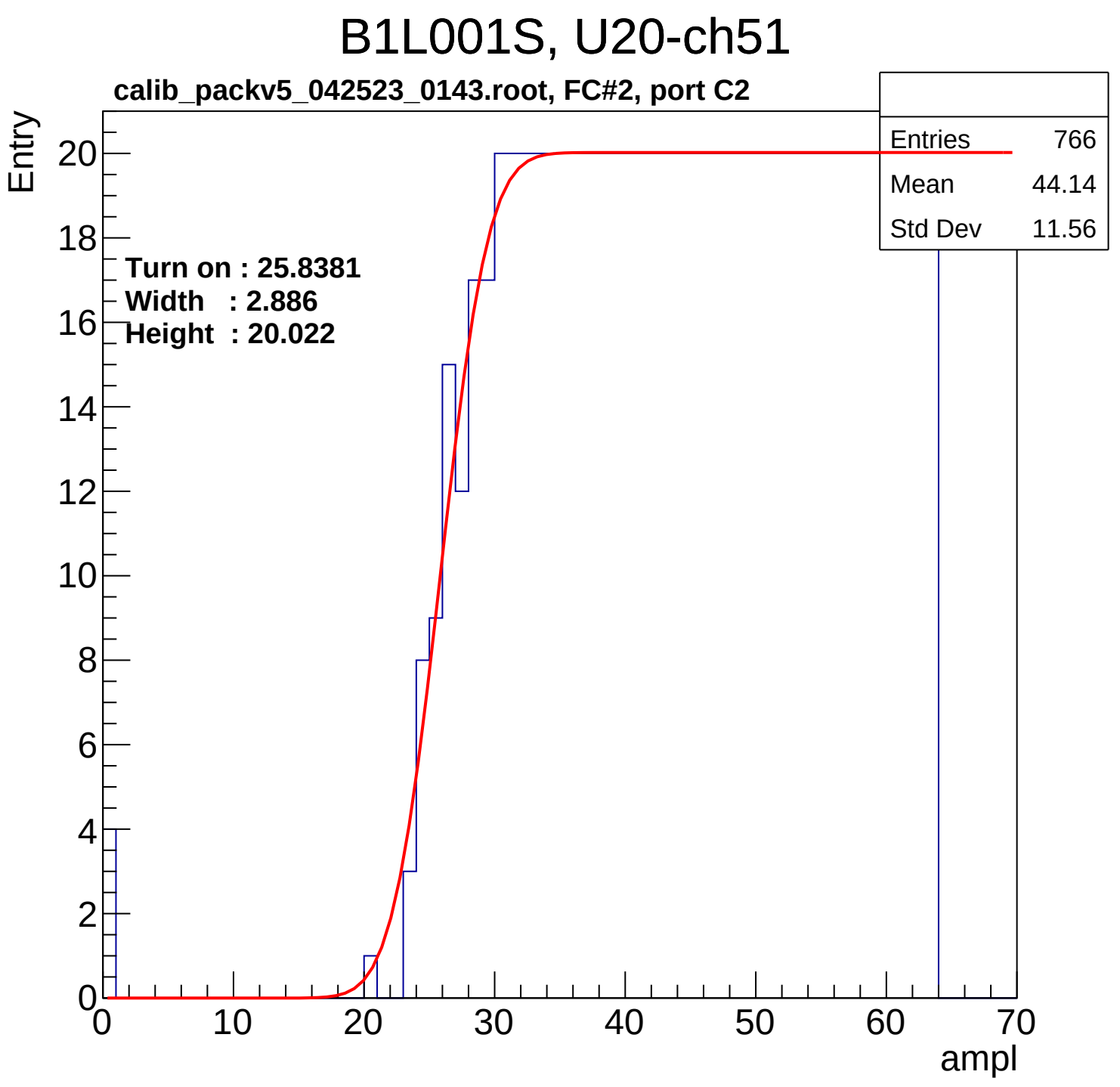
B1L001S, U20-ch51
calib_packv5_042523_0143.root, FC#2, port C2
Entries 766
Mean 44.14
Std Dev 11.56
Turn on : 25.8381
Width : 2.886
Height : 20.022
Entry
ampl
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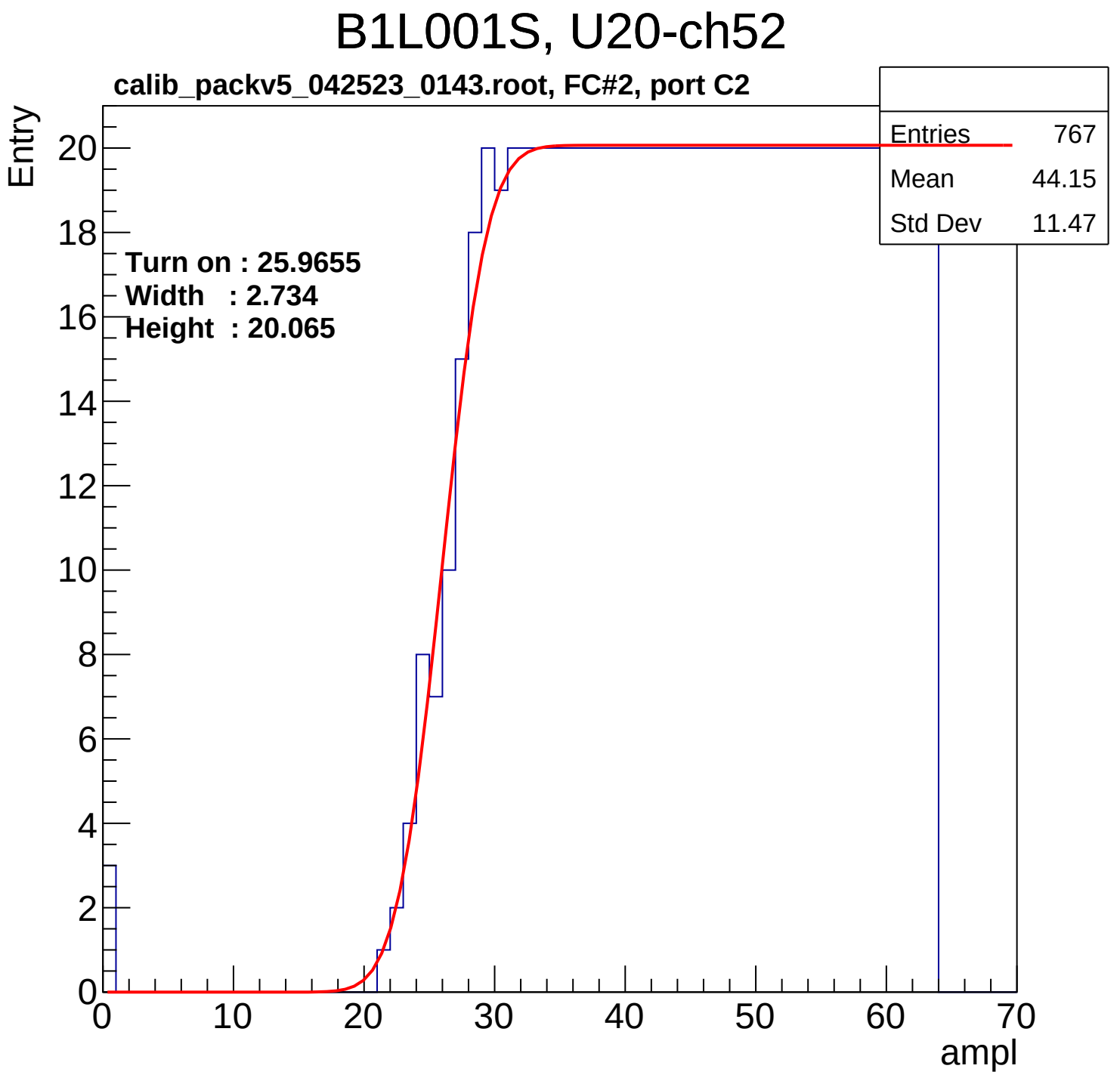
B1L001S, U20-ch52
calib_packv5_042523_0143.root, FC#2, port C2
Entries 767
Mean 44.15
Std Dev 11.47
Turn on : 25.9655
Width : 2.734
Height : 20.065
Entry
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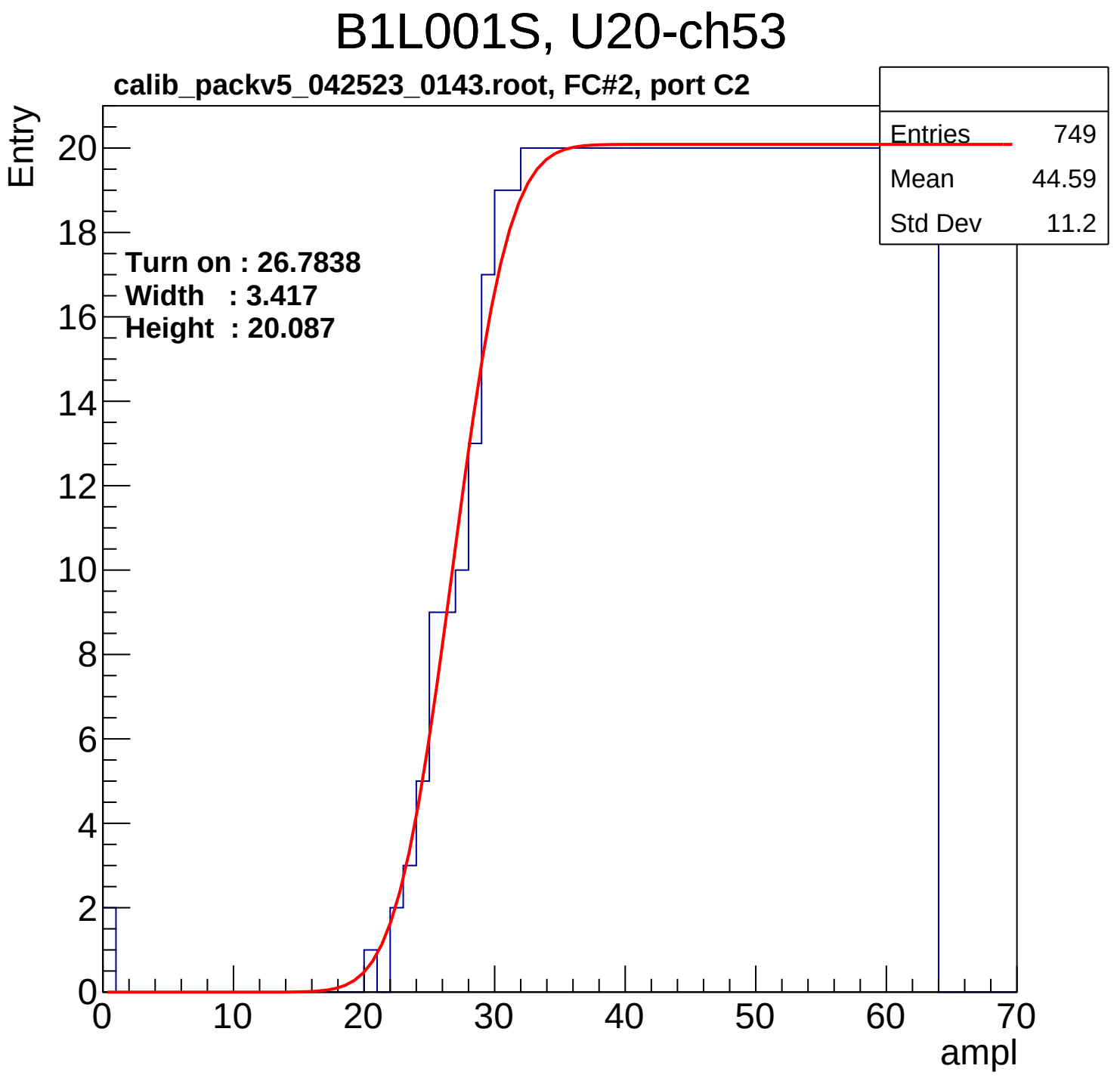
B1L001S, U20-ch53
calib_packv5_042523_0143.root, FC#2, port C2
Entries 749
Mean 44.59
Std Dev 11.2
Turn on : 26.7838
Width : 3.417
Height : 20.087
Entry
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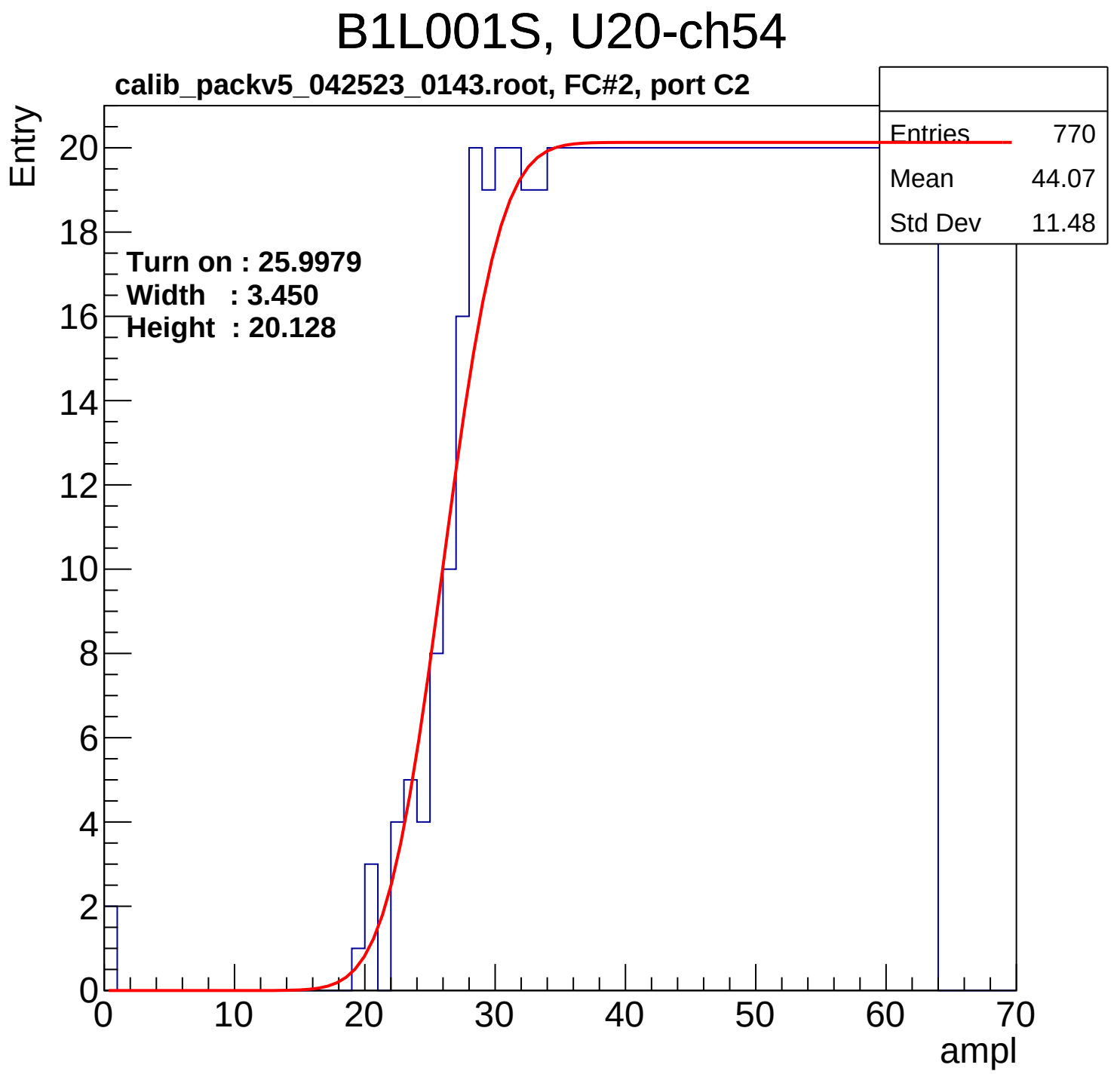
B1L001S, U20-ch54
calib_packv5_042523_0143.root, FC#2, port C2
Entries 770
Mean 44.07
Std Dev 11.48
Turn on : 25.9979
Width : 3.450
Height : 20.128
Entry
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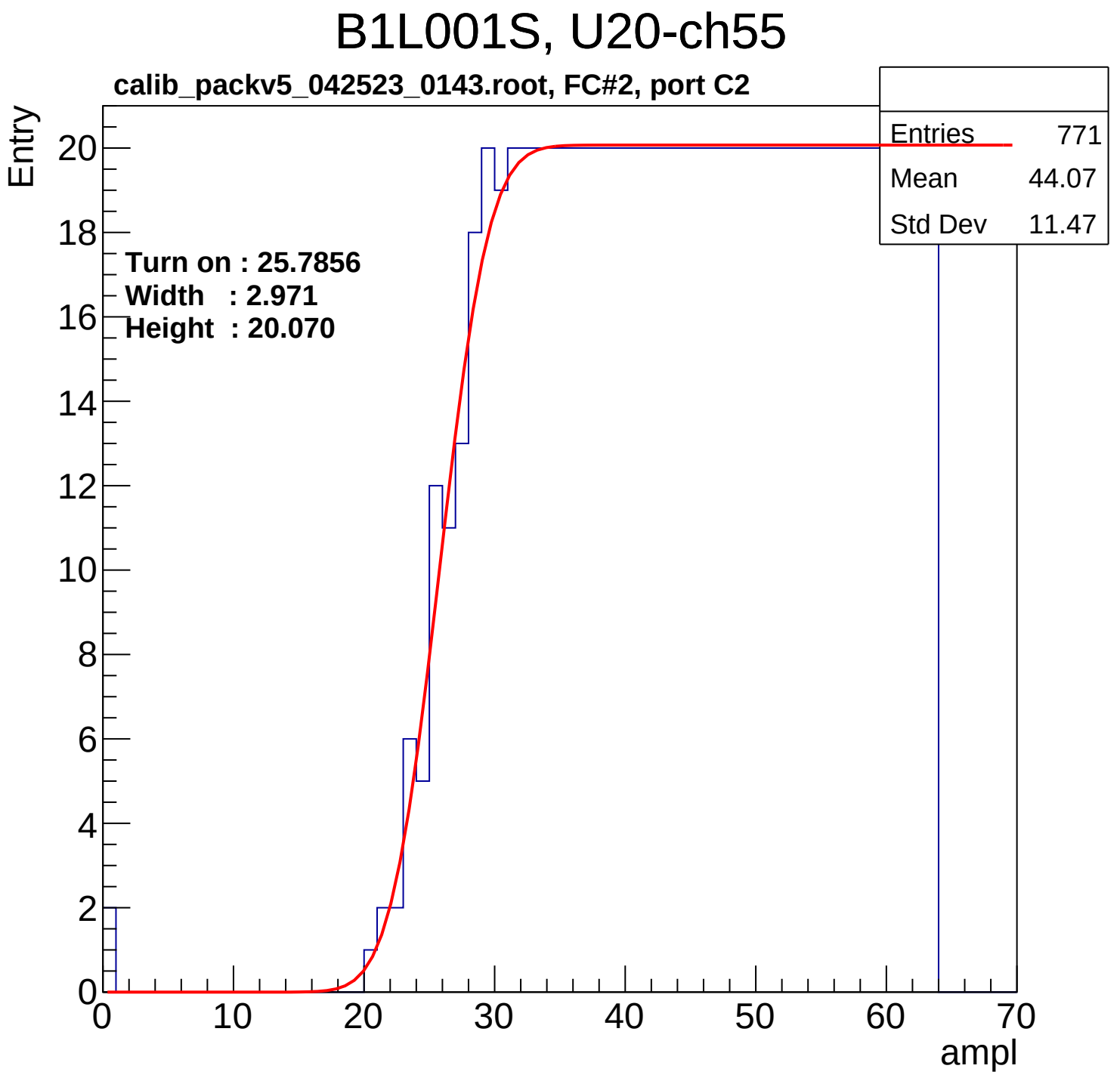
B1L001S, U20-ch55
calib_packv5_042523_0143.root, FC#2, port C2
Entries 771
Mean 44.07
Std Dev 11.47
Turn on : 25.7856
Width : 2.971
Height : 20.070
Entry
ampl
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6
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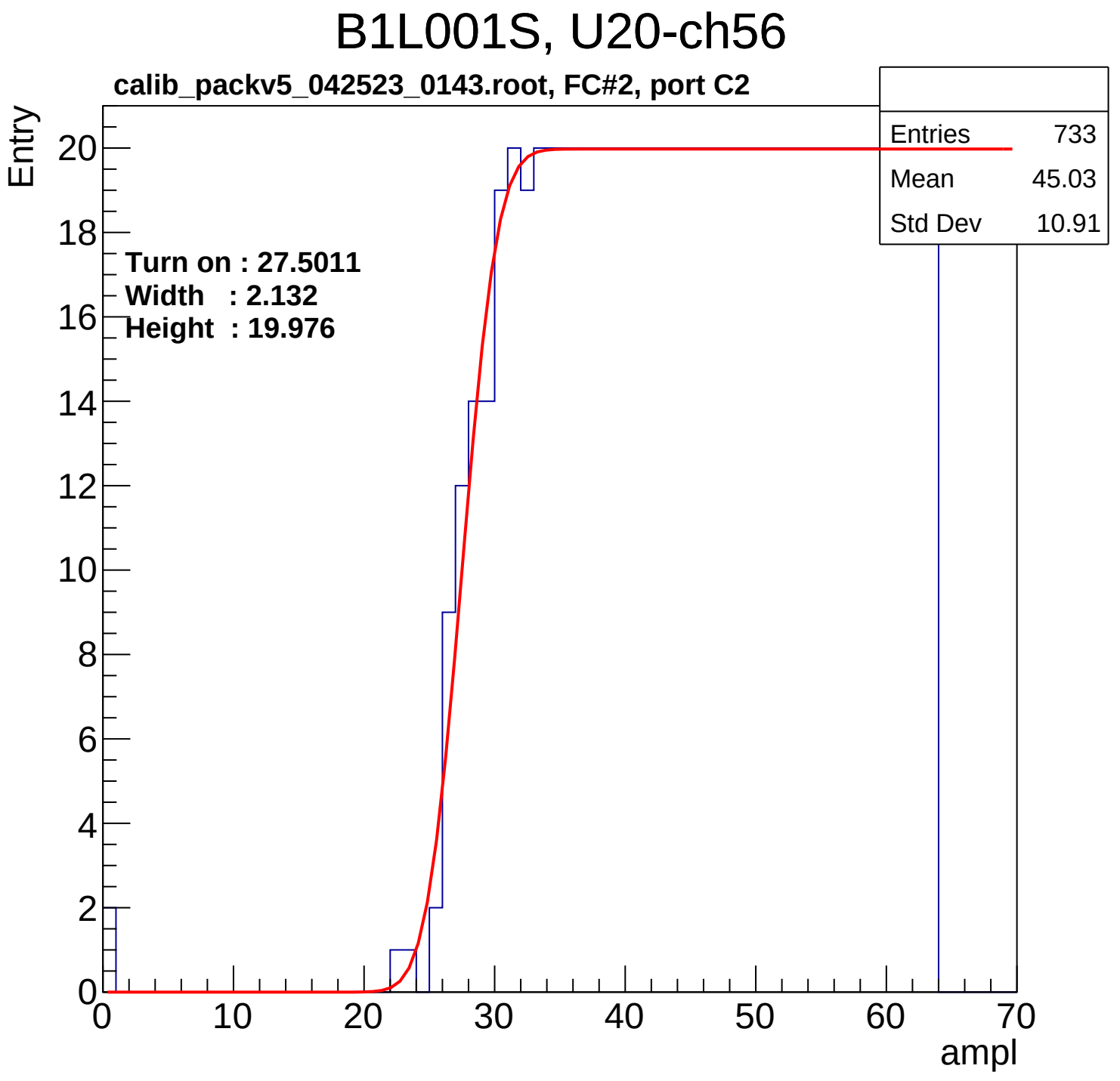
B1L001S, U20-ch56
calib_packv5_042523_0143.root, FC#2, port C2
Entries 733
Mean 45.03
Std Dev 10.91
Turn on : 27.5011
Width : 2.132
Height : 19.976
Entry
ampl
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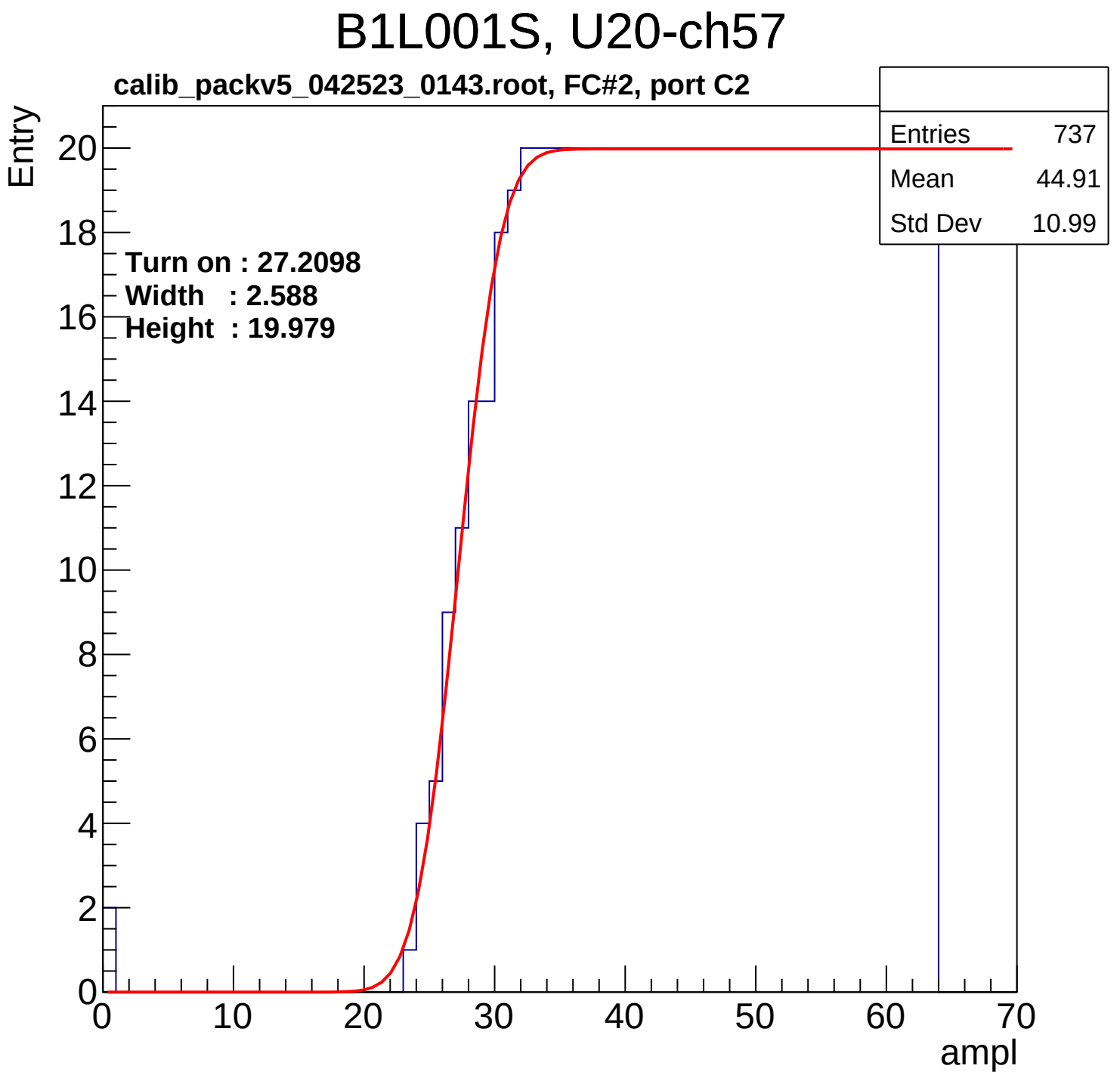
B1L001S, U20-ch57
calib_packv5_042523_0143.root, FC#2, port C2
Entries 737
Mean 44.91
Std Dev 10.99
Turn on : 27.2098
Width : 2.588
Height : 19.979
Entry
ampl
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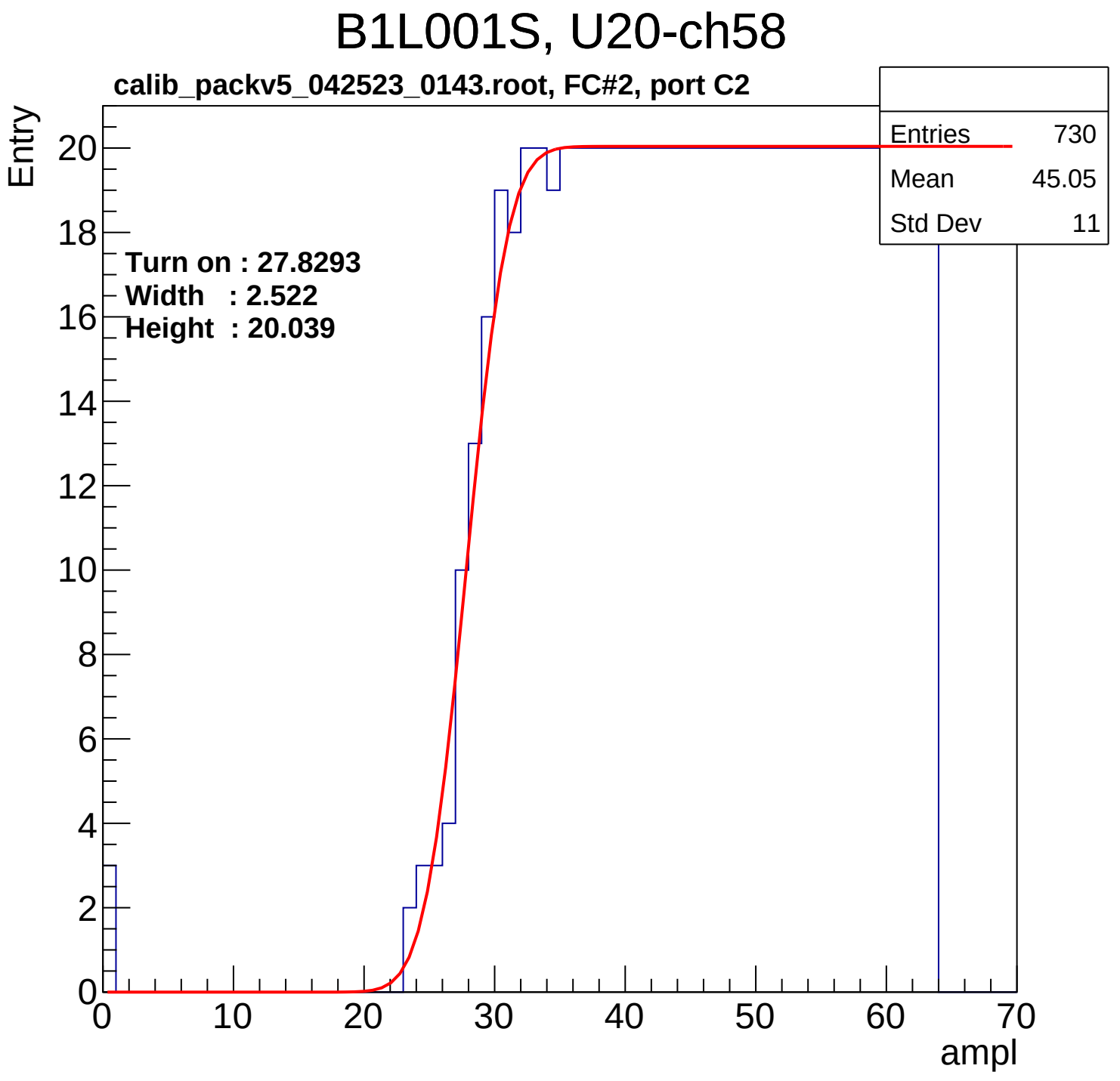
B1L001S, U20-ch58
calib_packv5_042523_0143.root, FC#2, port C2
Entries 730
Mean 45.05
Std Dev 11
Turn on : 27.8293
Width : 2.522
Height : 20.039
Entry
ampl
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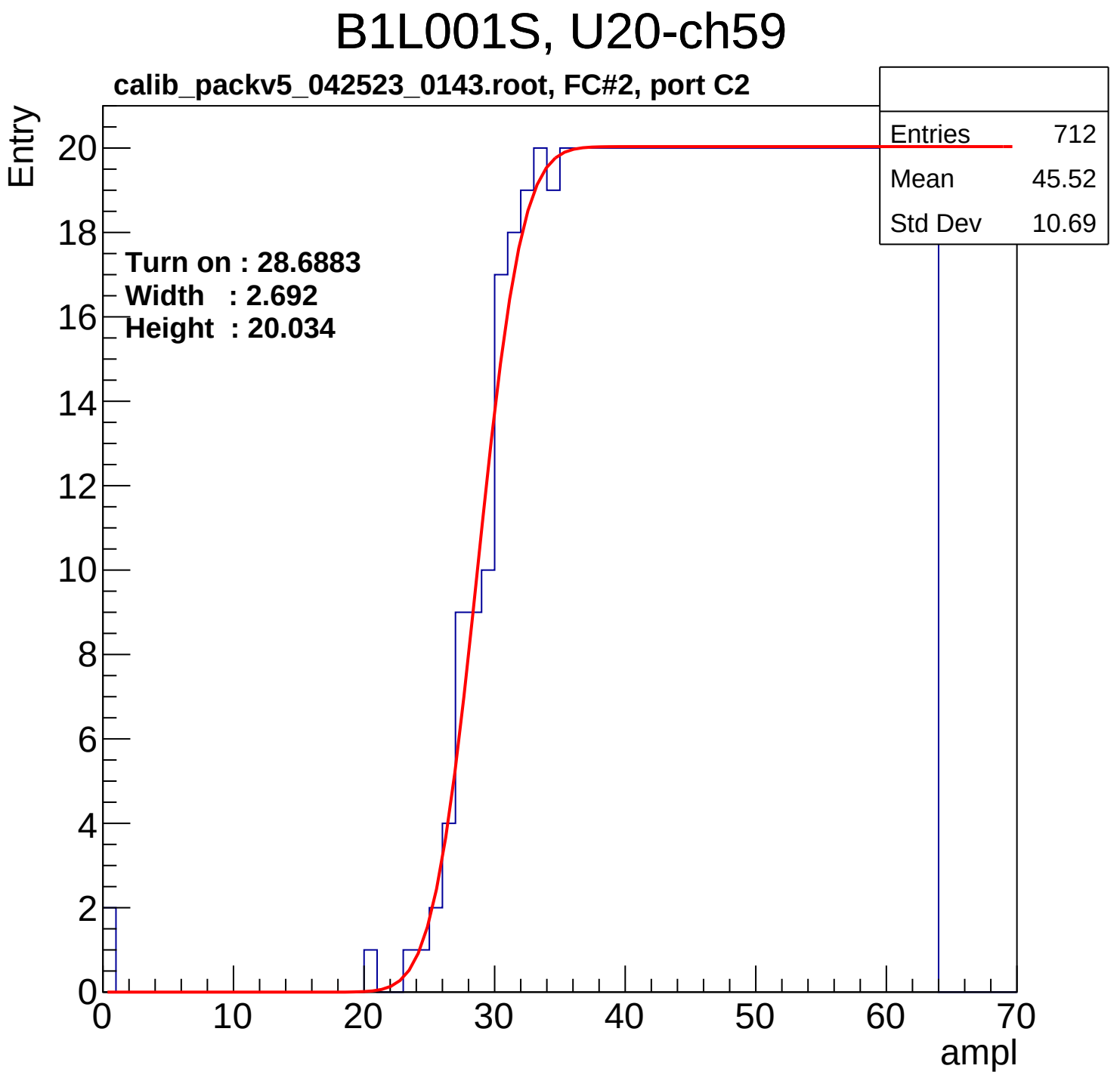
B1L001S, U20-ch59
calib_packv5_042523_0143.root, FC#2, port C2
Entries 712
Mean 45.52
Std Dev 10.69
Turn on : 28.6883
Width : 2.692
Height : 20.034
Entry
ampl
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6
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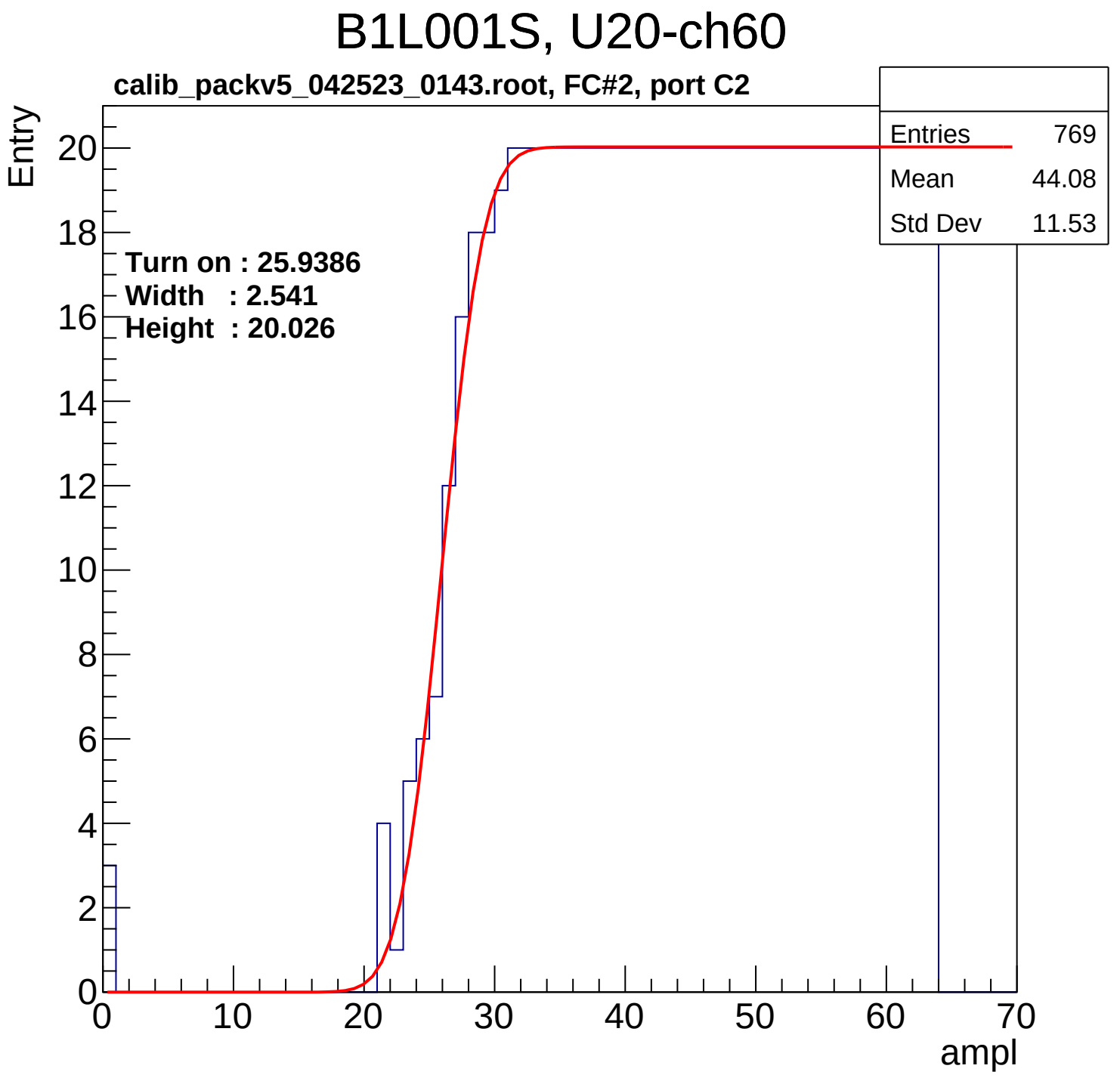
B1L001S, U20-ch60
calib_packv5_042523_0143.root, FC#2, port C2
Entries 769
Mean 44.08
Std Dev 11.53
Turn on : 25.9386
Width : 2.541
Height : 20.026
Entry
ampl
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14
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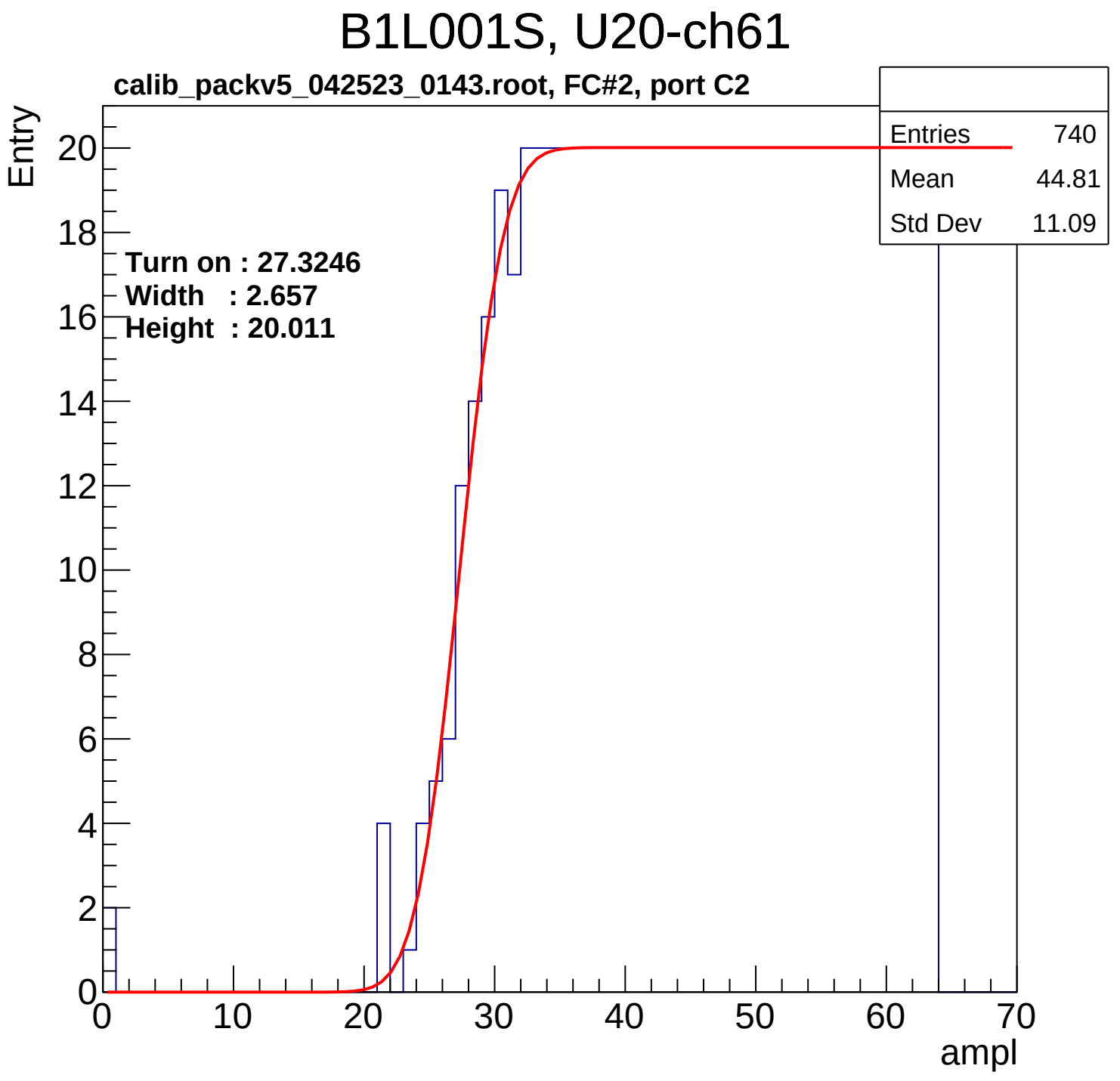
B1L001S, U20-ch61
calib_packv5_042523_0143.root, FC#2, port C2
Entries 740
Mean 44.81
Std Dev 11.09
Turn on : 27.3246
Width : 2.657
Height : 20.011
Entry
ampl
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6
8
10
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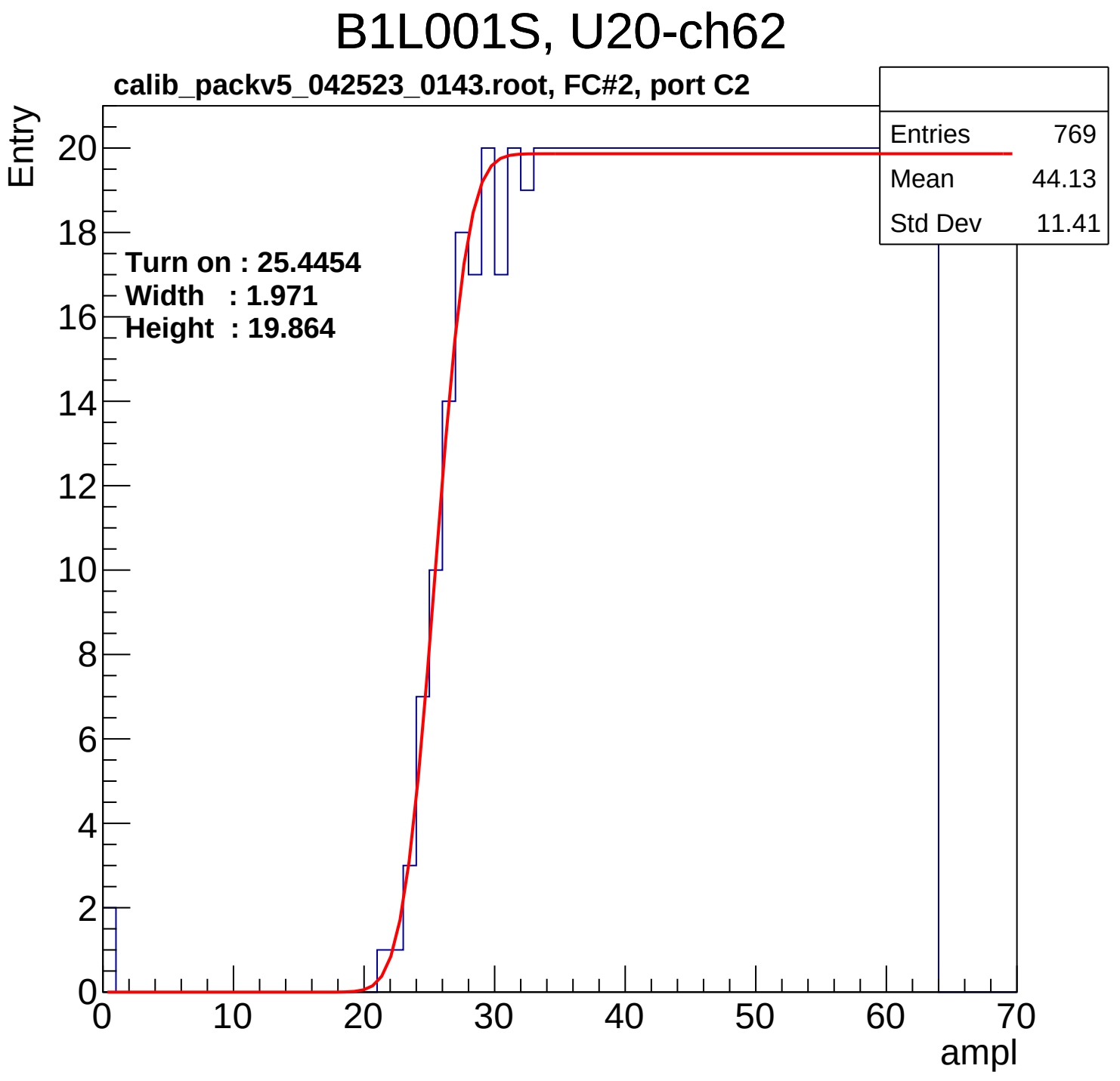
B1L001S, U20-ch62
calib_packv5_042523_0143.root, FC#2, port C2
Entries 769
Mean 44.13
Std Dev 11.41
Turn on : 25.4454
Width : 1.971
Height : 19.864
Entry
ampl
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6
8
10
12
14
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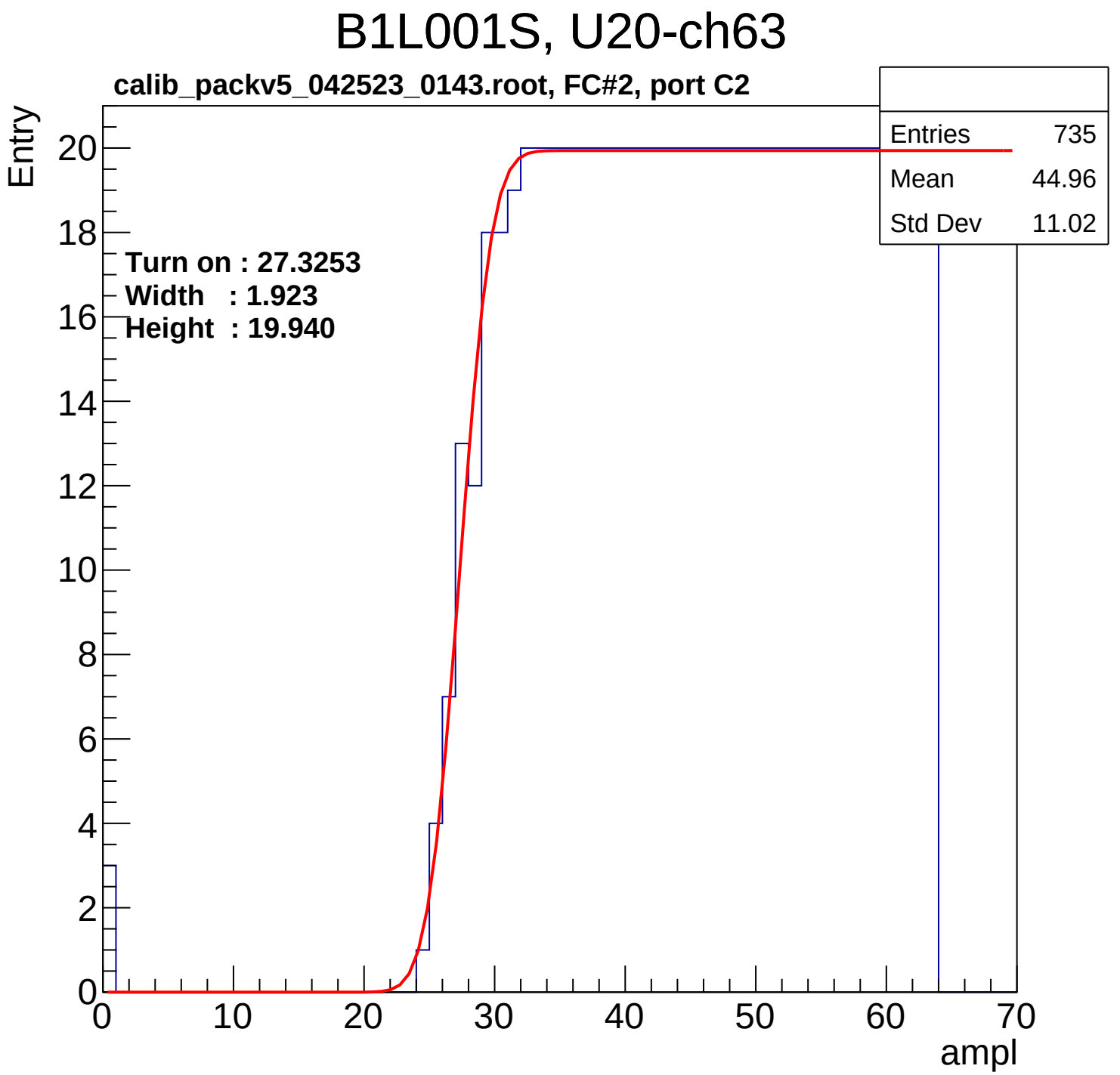
B1L001S, U20-ch63
calib_packv5_042523_0143.root, FC#2, port C2
Entries 735
Mean 44.96
Std Dev 11.02
Turn on : 27.3253
Width : 1.923
Height : 19.940
Entry
ampl
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6
8
10
12
14
16
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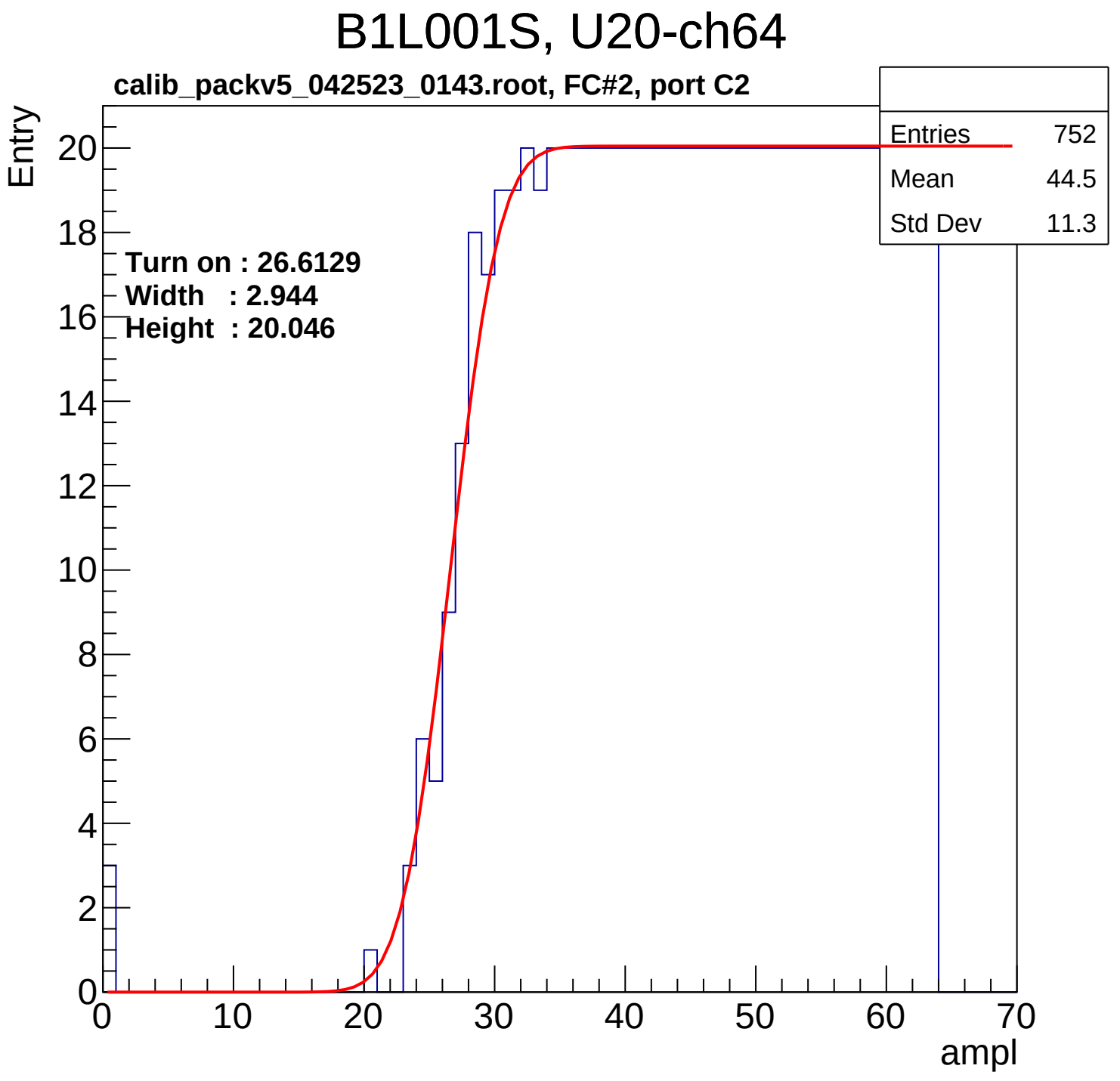
B1L001S, U20-ch64
calib_packv5_042523_0143.root, FC#2, port C2
Entries 752
Mean 44.5
Std Dev 11.3
Turn on : 26.6129
Width : 2.944
Height : 20.046
Entry
ampl
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6
8
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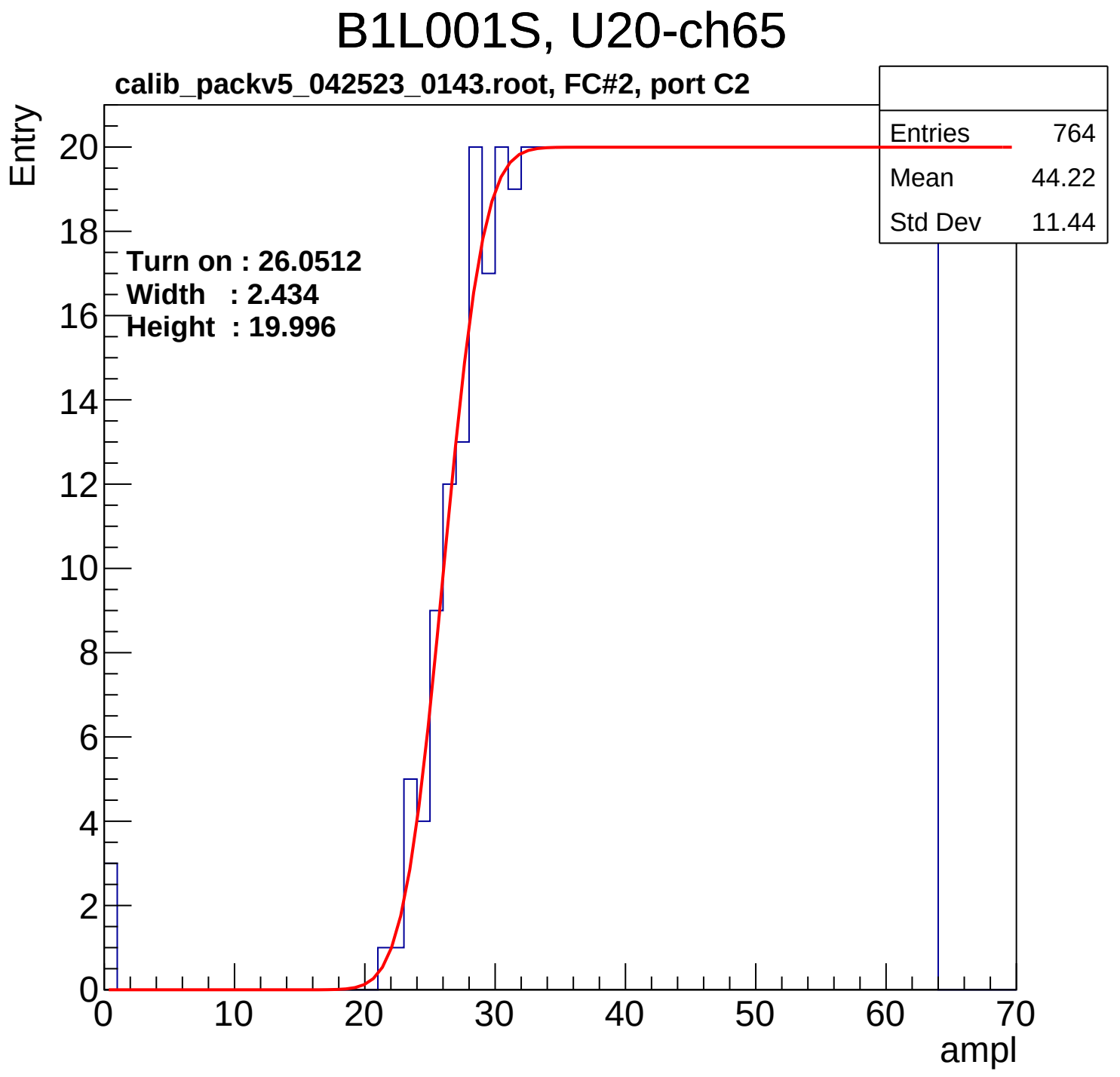
B1L001S, U20-ch65
calib_packv5_042523_0143.root, FC#2, port C2
Entries 764
Mean 44.22
Std Dev 11.44
Turn on : 26.0512
Width : 2.434
Height : 19.996
Entry
ampl
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6
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12
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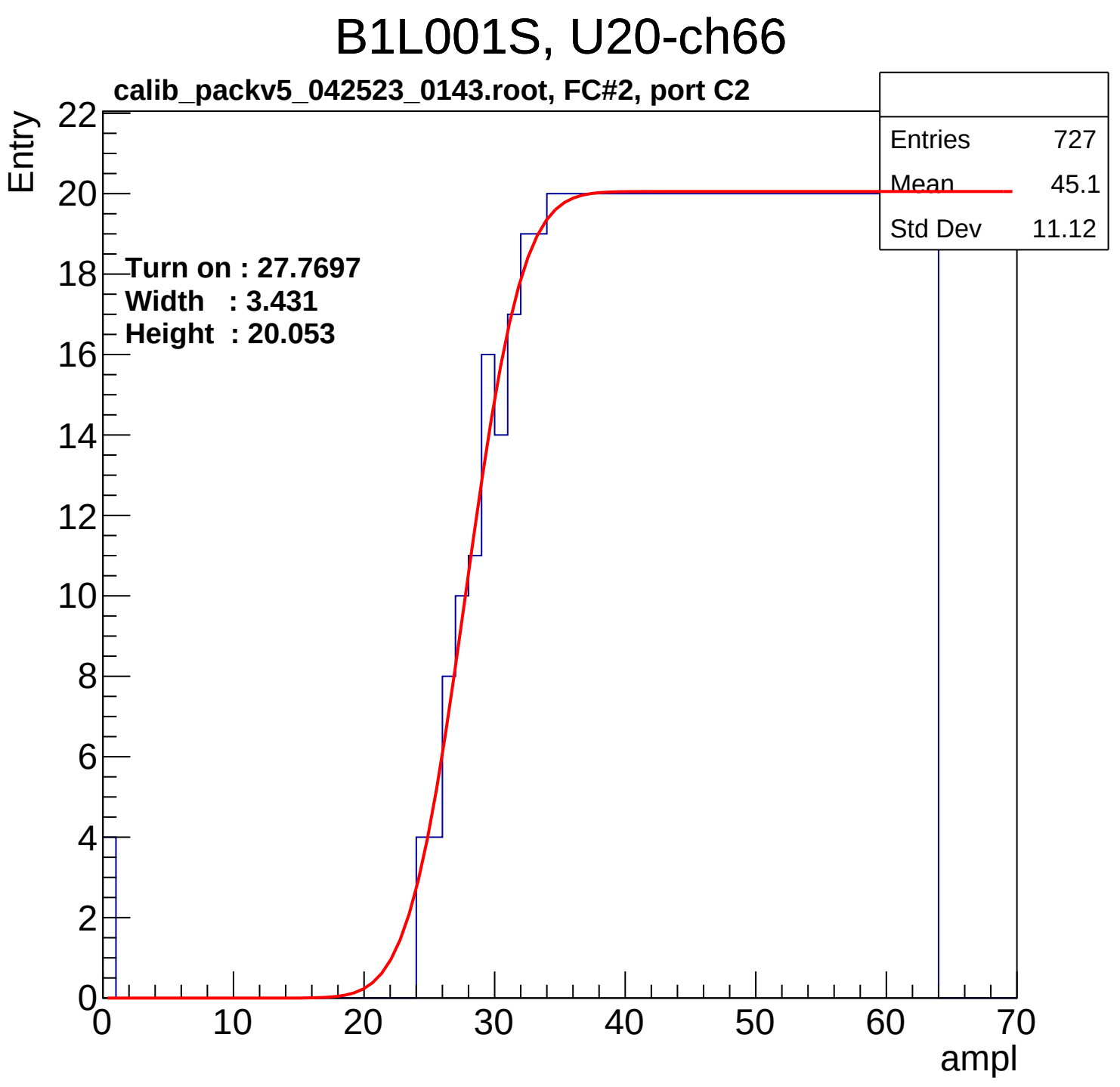
B1L001S, U20-ch66
calib_packv5_042523_0143.root, FC#2, port C2
Entries 727
Mean 45.1
Std Dev 11.12
Turn on : 27.7697
Width : 3.431
Height : 20.053
Entry
ampl
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8
10
12
14
16
18
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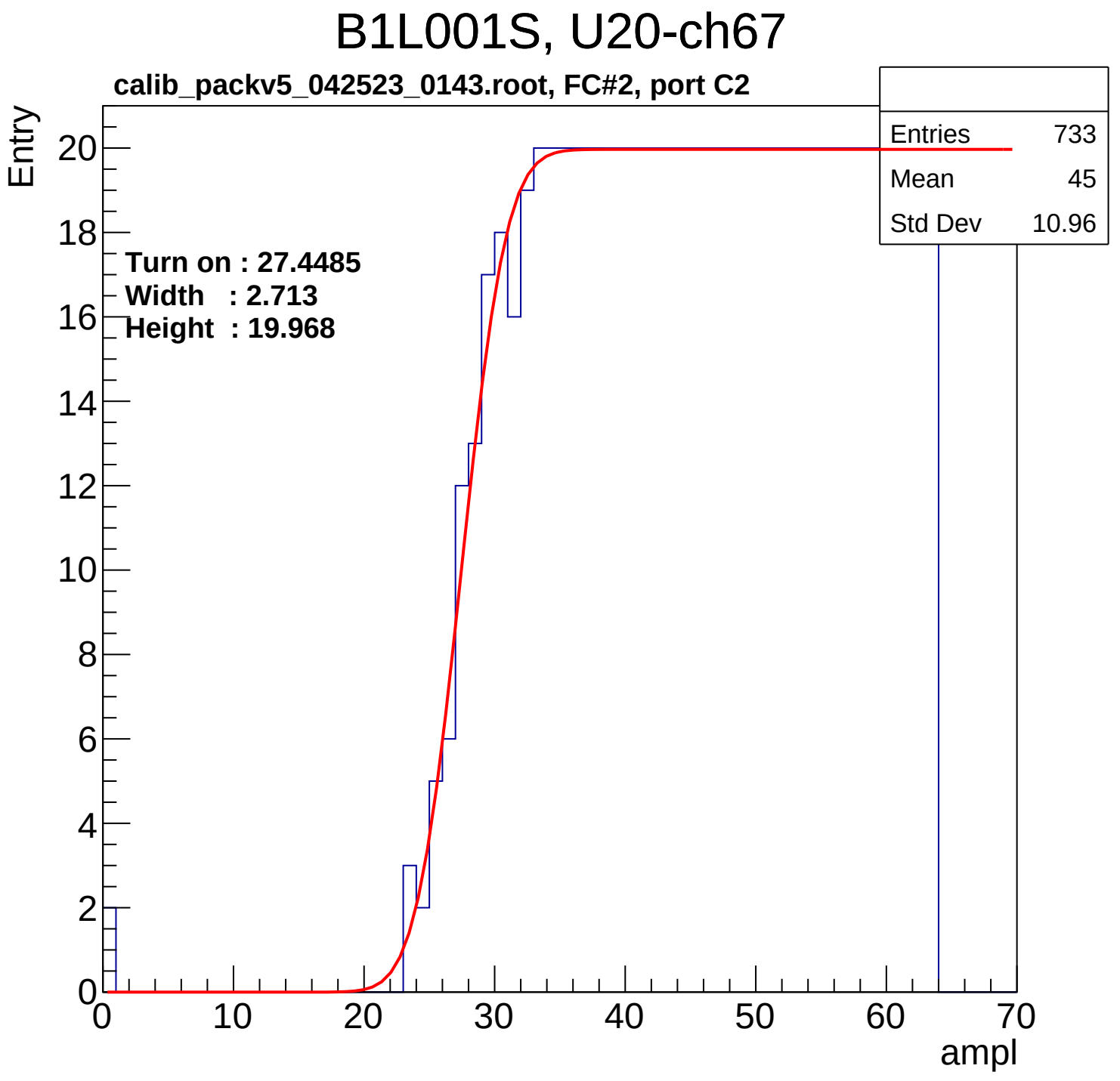
B1L001S, U20-ch67
calib_packv5_042523_0143.root, FC#2, port C2
Entries 733
Mean 45
Std Dev 10.96
Turn on : 27.4485
Width : 2.713
Height : 19.968
Entry
ampl
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6
8
10
12
14
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18
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0
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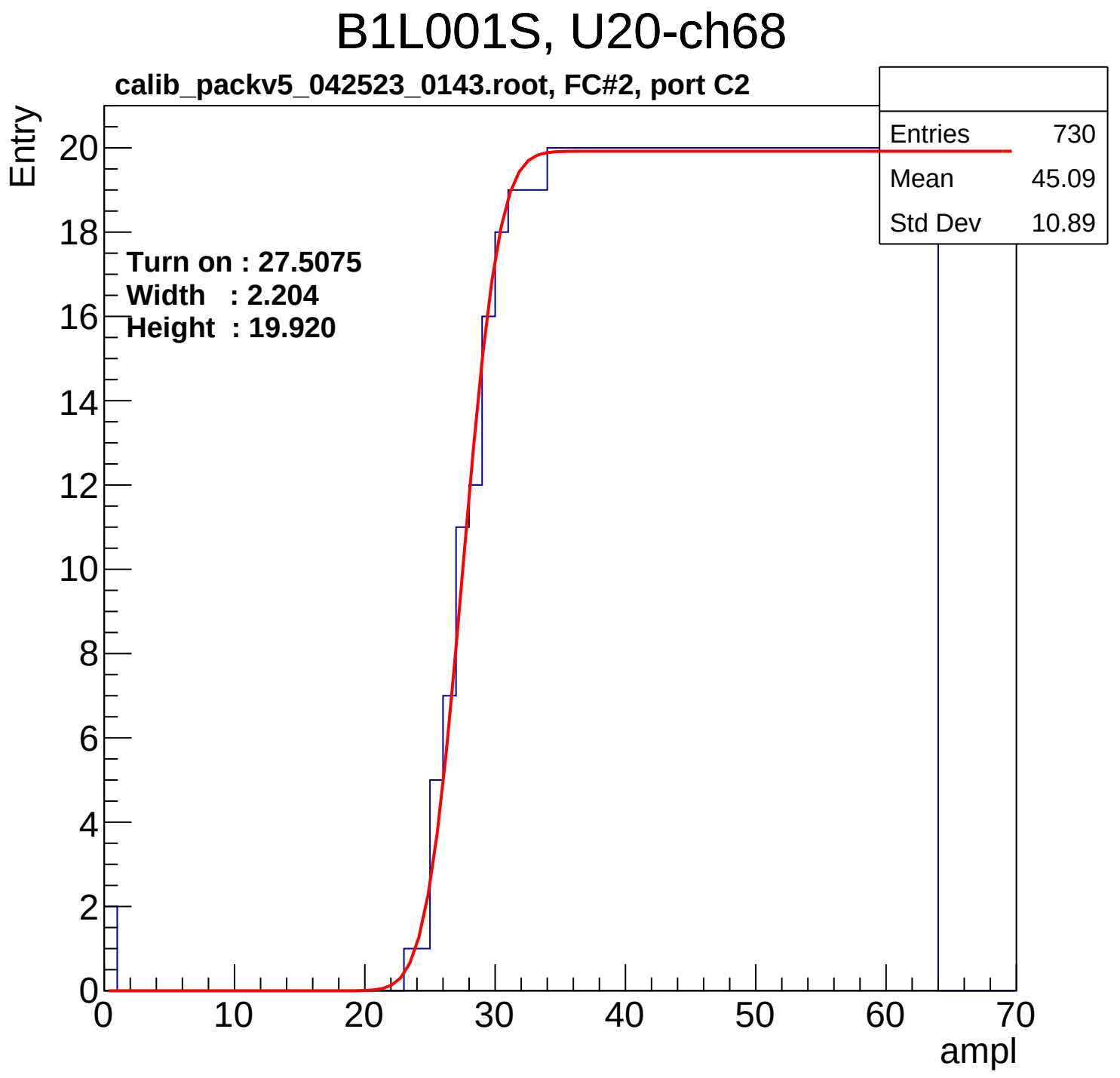
B1L001S, U20-ch68
calib_packv5_042523_0143.root, FC#2, port C2
Entries 730
Mean 45.09
Std Dev 10.89
Turn on : 27.5075
Width : 2.204
Height : 19.920
Entry
ampl
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6
8
10
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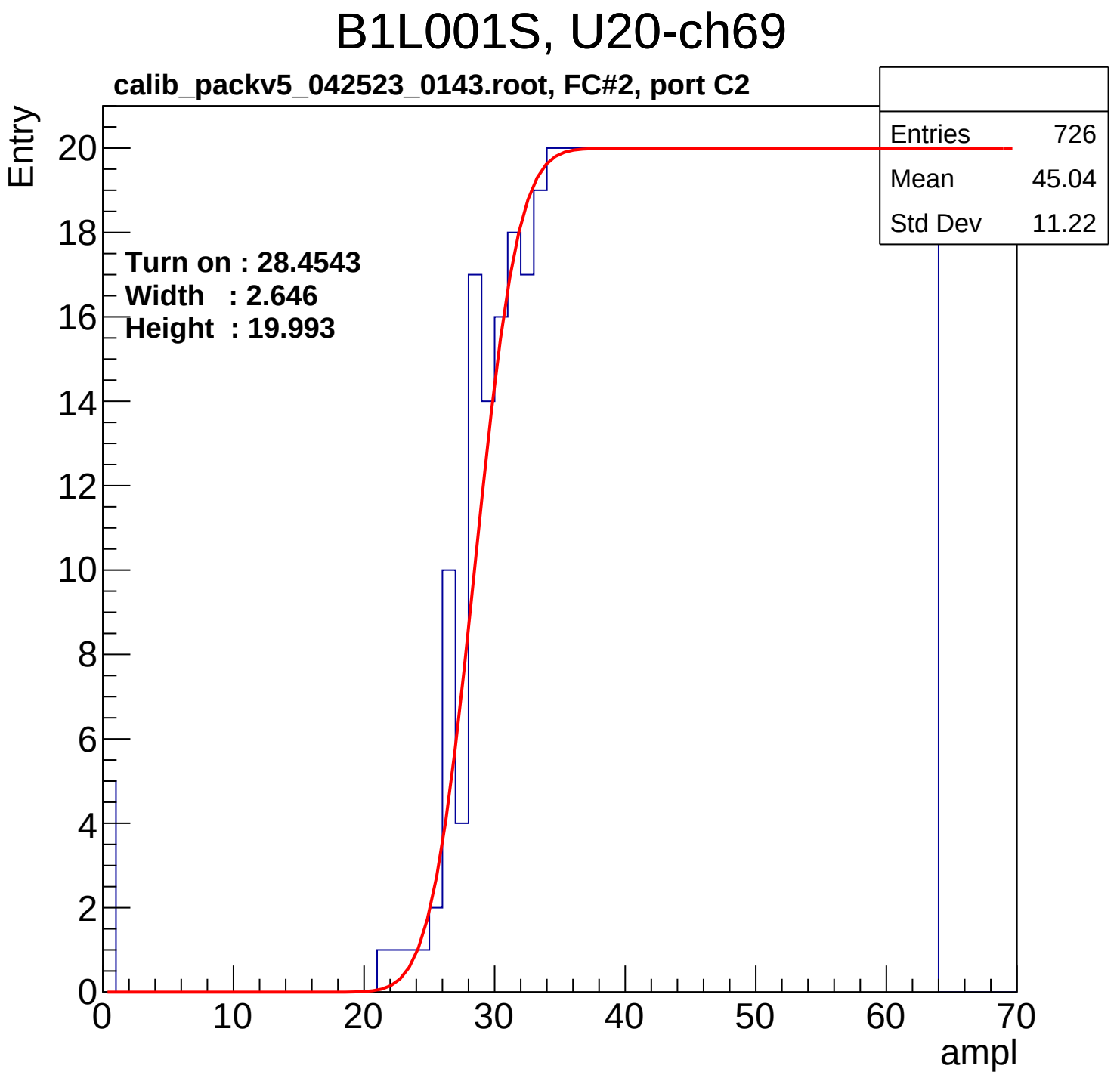
B1L001S, U20-ch69
calib_packv5_042523_0143.root, FC#2, port C2
Entries 726
Mean 45.04
Std Dev 11.22
Turn on : 28.4543
Width : 2.646
Height : 19.993
Entry
ampl
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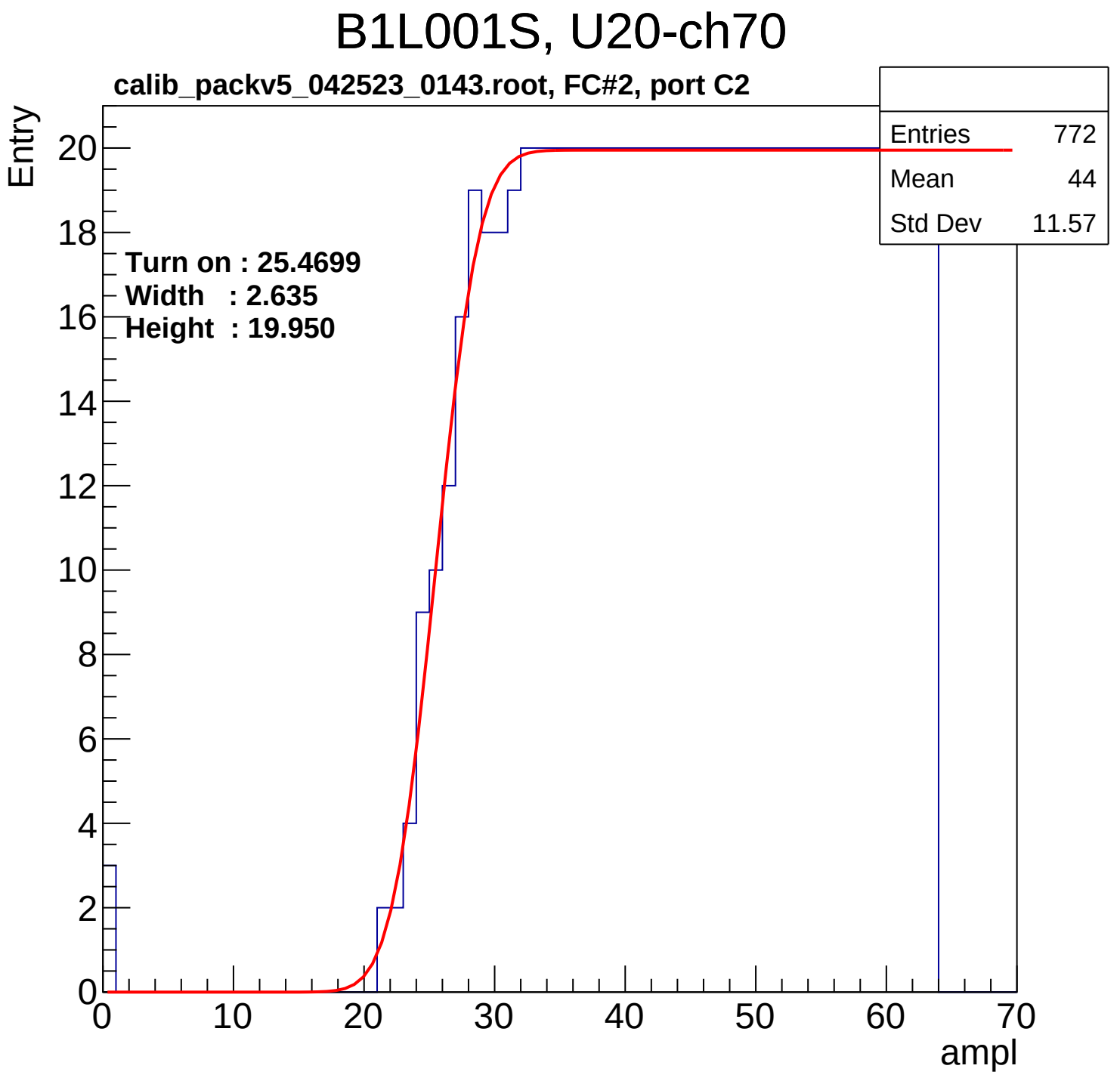
B1L001S, U20-ch70
calib_packv5_042523_0143.root, FC#2, port C2
Entries 772
Mean 44
Std Dev 11.57
Turn on : 25.4699
Width : 2.635
Height : 19.950
Entry
ampl
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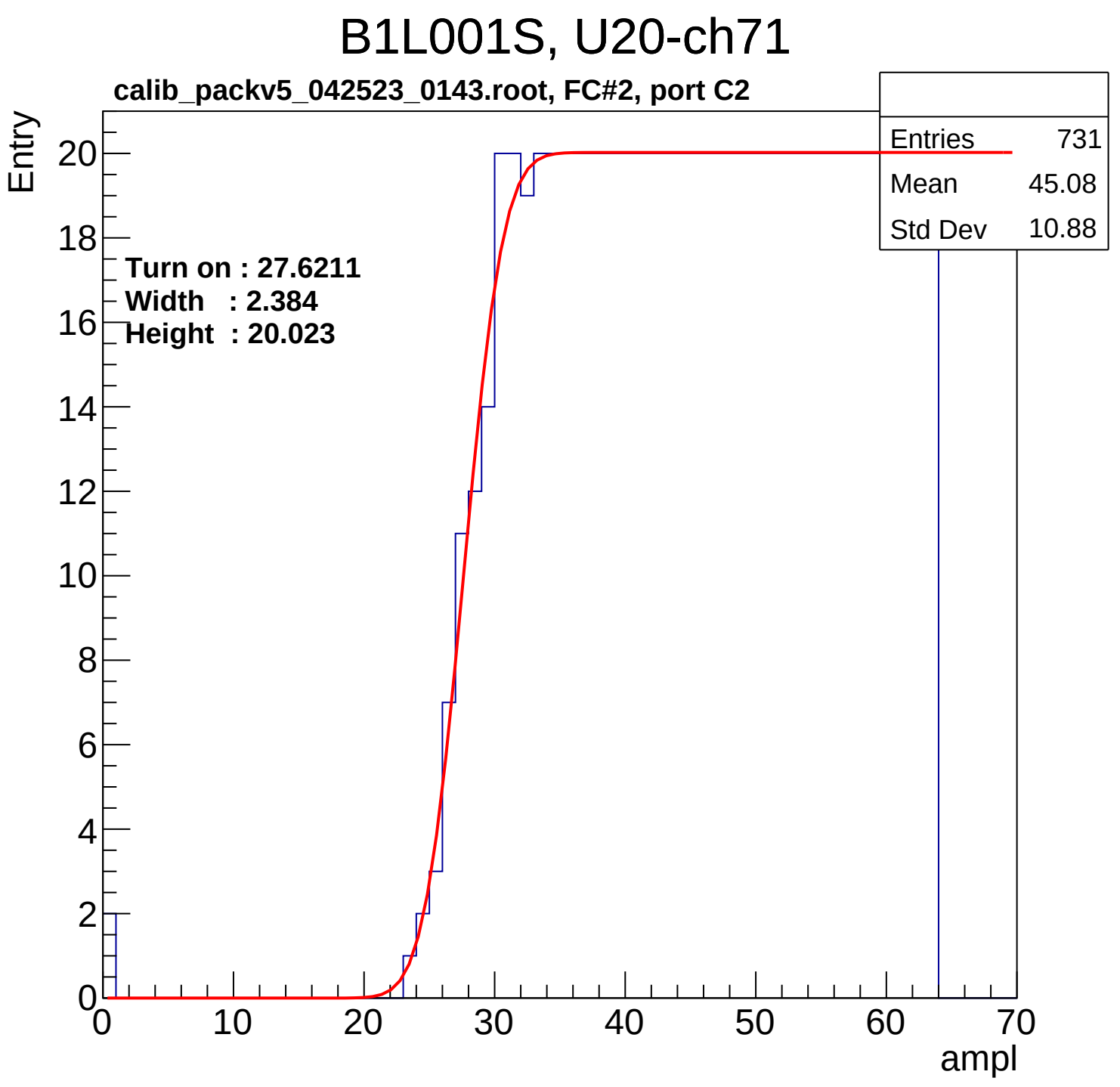
B1L001S, U20-ch71
calib_packv5_042523_0143.root, FC#2, port C2
Entries 731
Mean 45.08
Std Dev 10.88
Turn on : 27.6211
Width : 2.384
Height : 20.023
Entry
ampl
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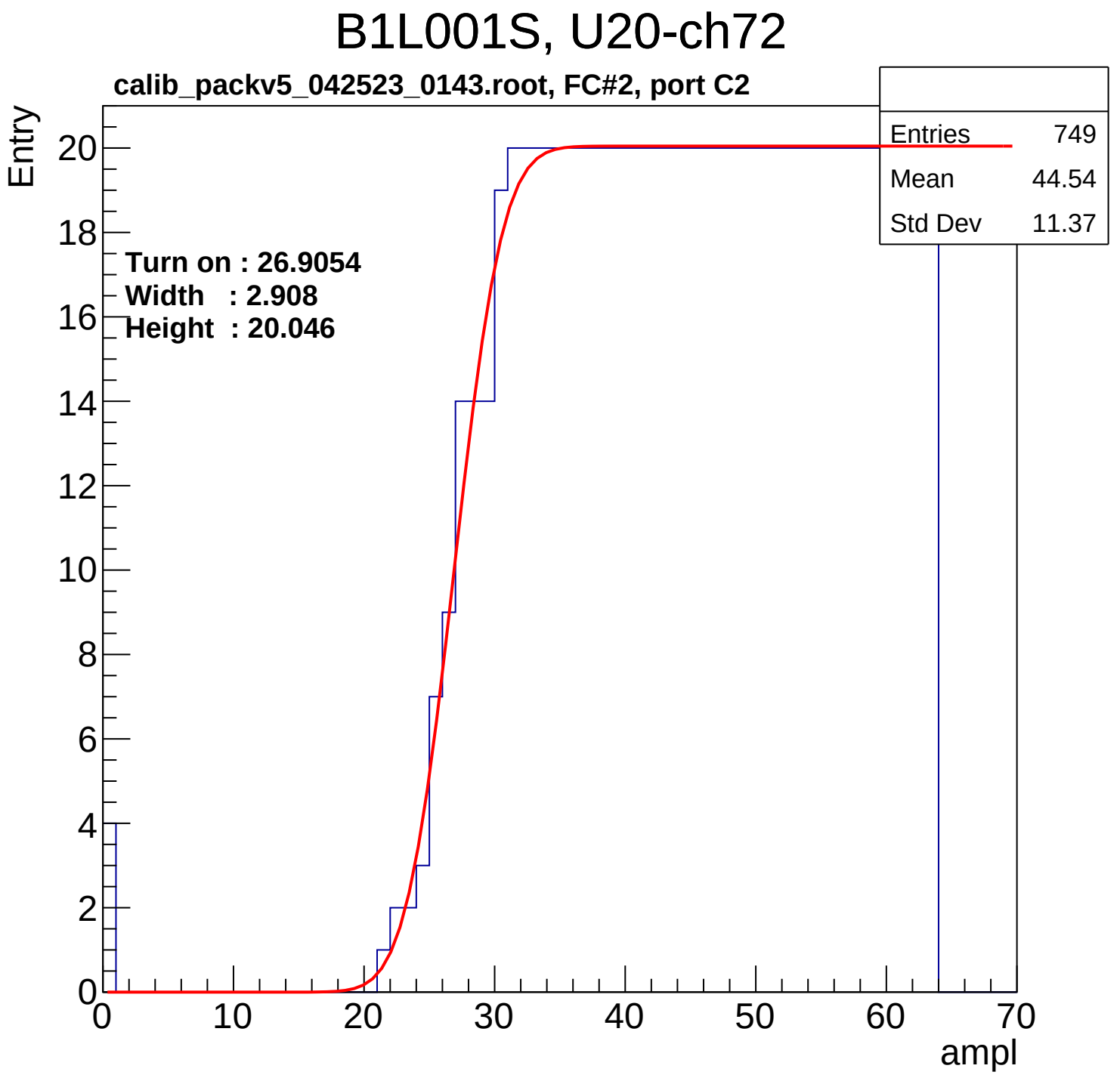
B1L001S, U20-ch72
calib_packv5_042523_0143.root, FC#2, port C2
Entries 749
Mean 44.54
Std Dev 11.37
Turn on : 26.9054
Width : 2.908
Height : 20.046
Entry
ampl
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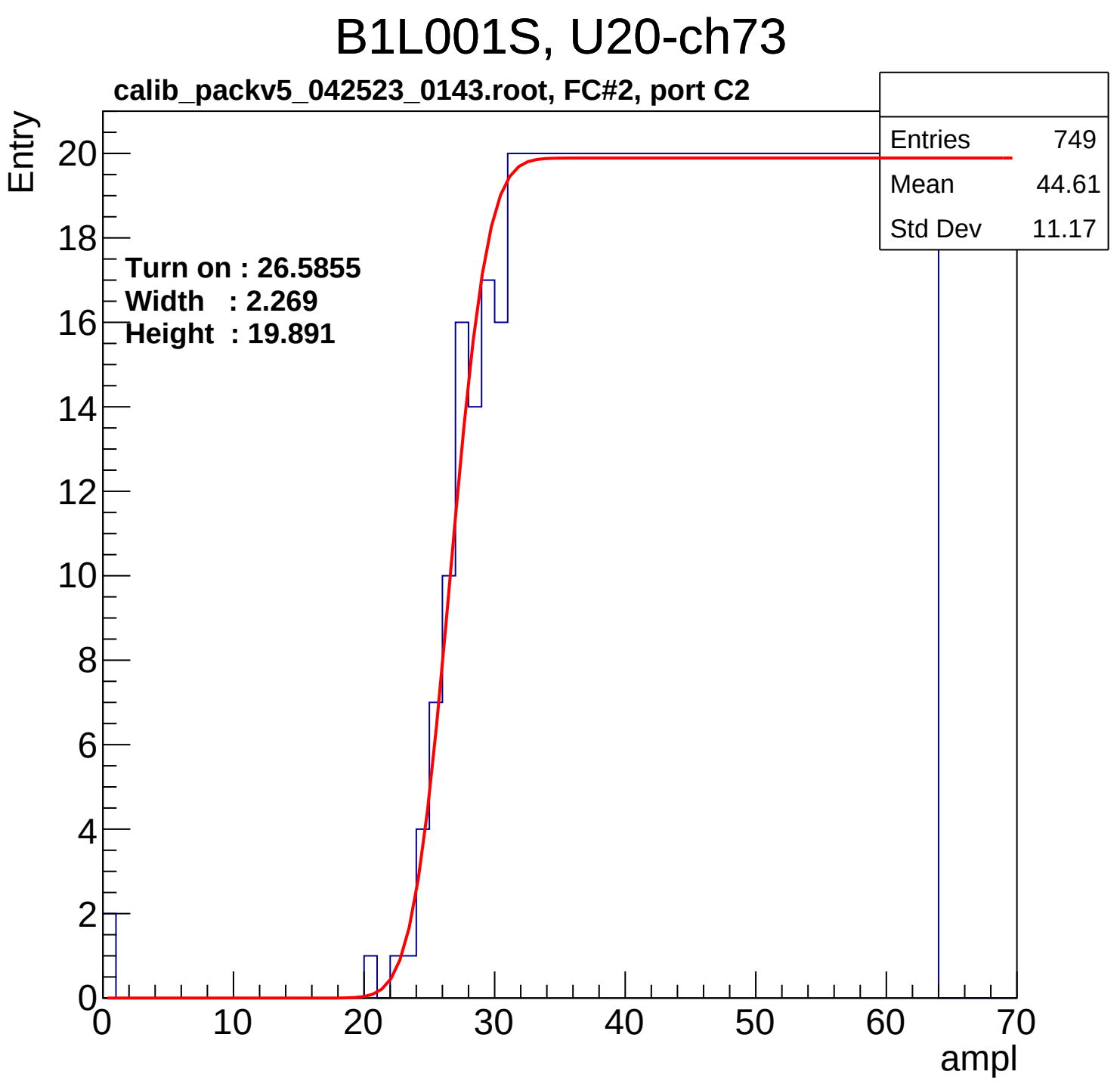
B1L001S, U20-ch73
calib_packv5_042523_0143.root, FC#2, port C2
Entries 749
Mean 44.61
Std Dev 11.17
Turn on : 26.5855
Width : 2.269
Height : 19.891
Entry
ampl
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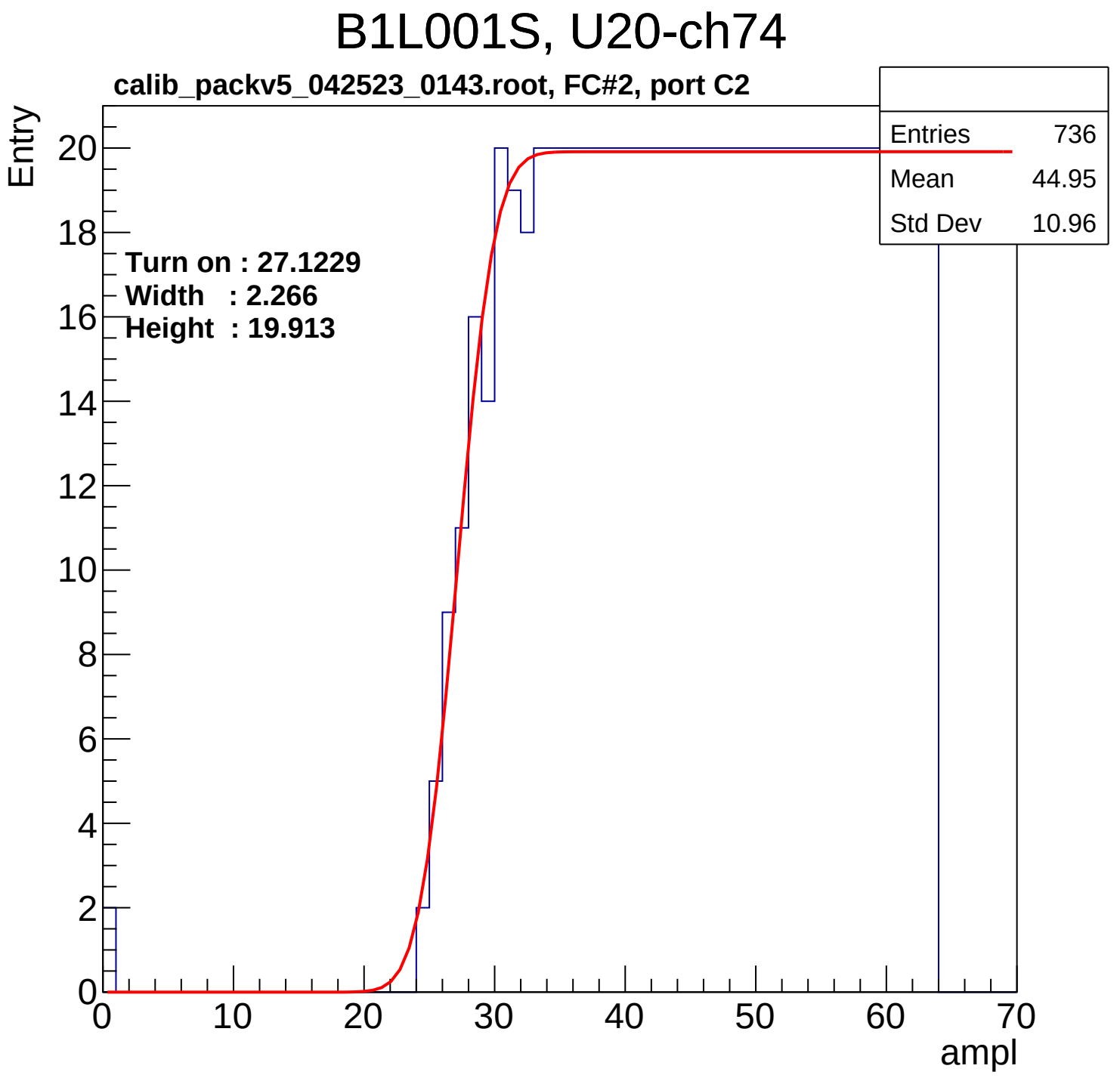
B1L001S, U20-ch74
calib_packv5_042523_0143.root, FC#2, port C2
Entries 736
Mean 44.95
Std Dev 10.96
Turn on : 27.1229
Width : 2.266
Height : 19.913
Entry
ampl
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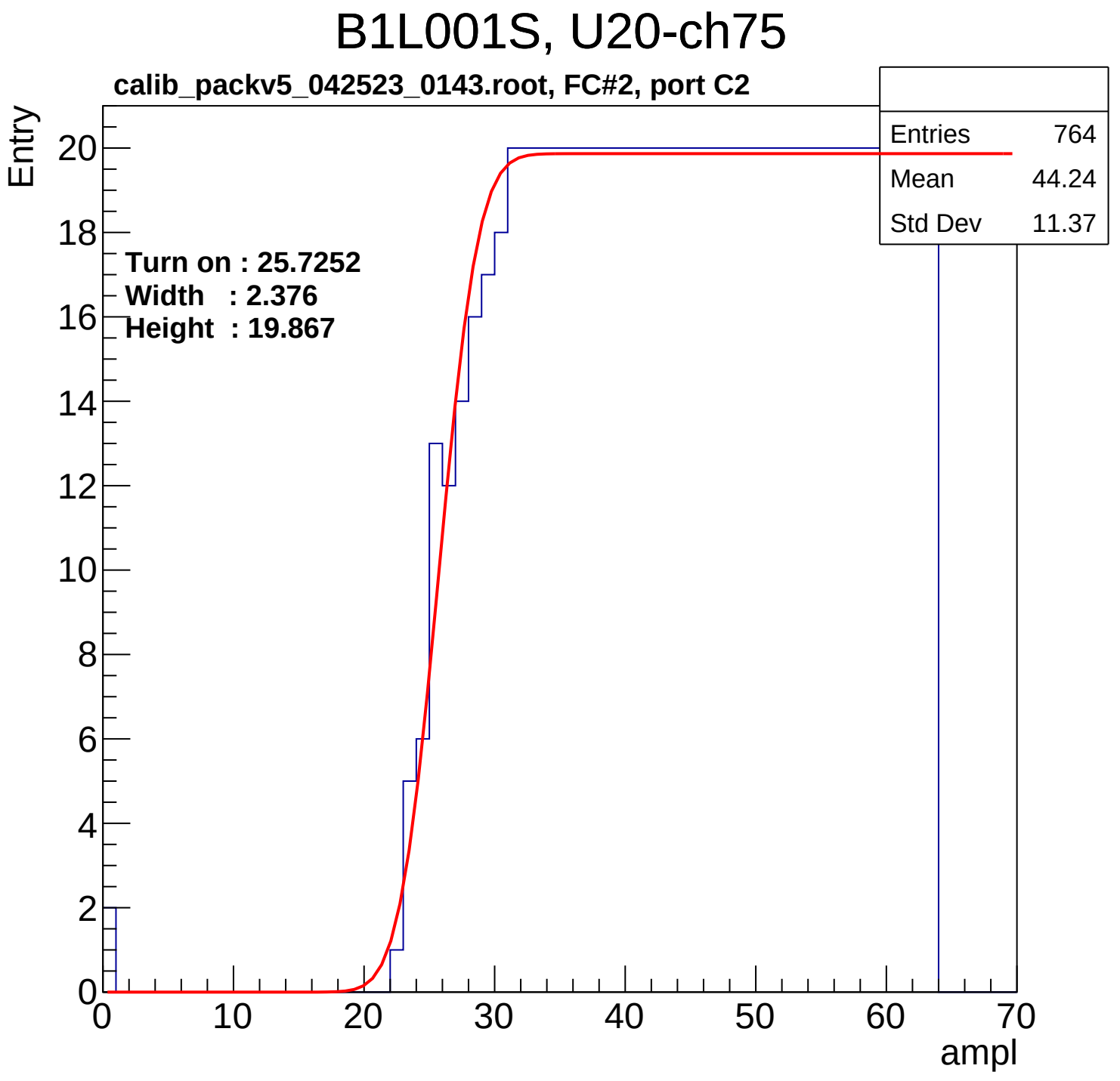
B1L001S, U20-ch75
calib_packv5_042523_0143.root, FC#2, port C2
Entries 764
Mean 44.24
Std Dev 11.37
Turn on : 25.7252
Width : 2.376
Height : 19.867
Entry
ampl
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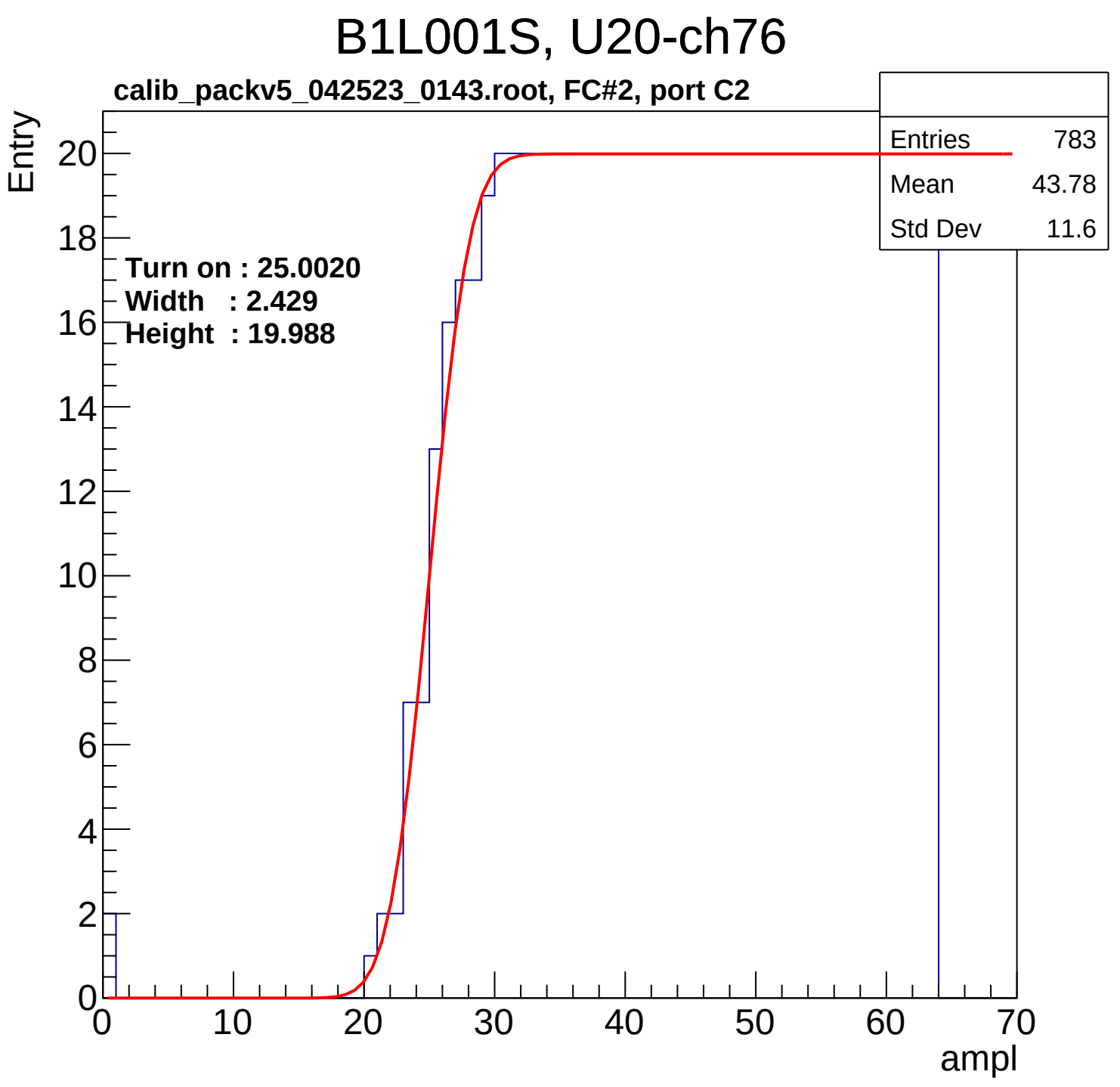
B1L001S, U20-ch76
calib_packv5_042523_0143.root, FC#2, port C2
Entries 783
Mean 43.78
Std Dev 11.6
Turn on : 25.0020
Width : 2.429
Height : 19.988
Entry
ampl
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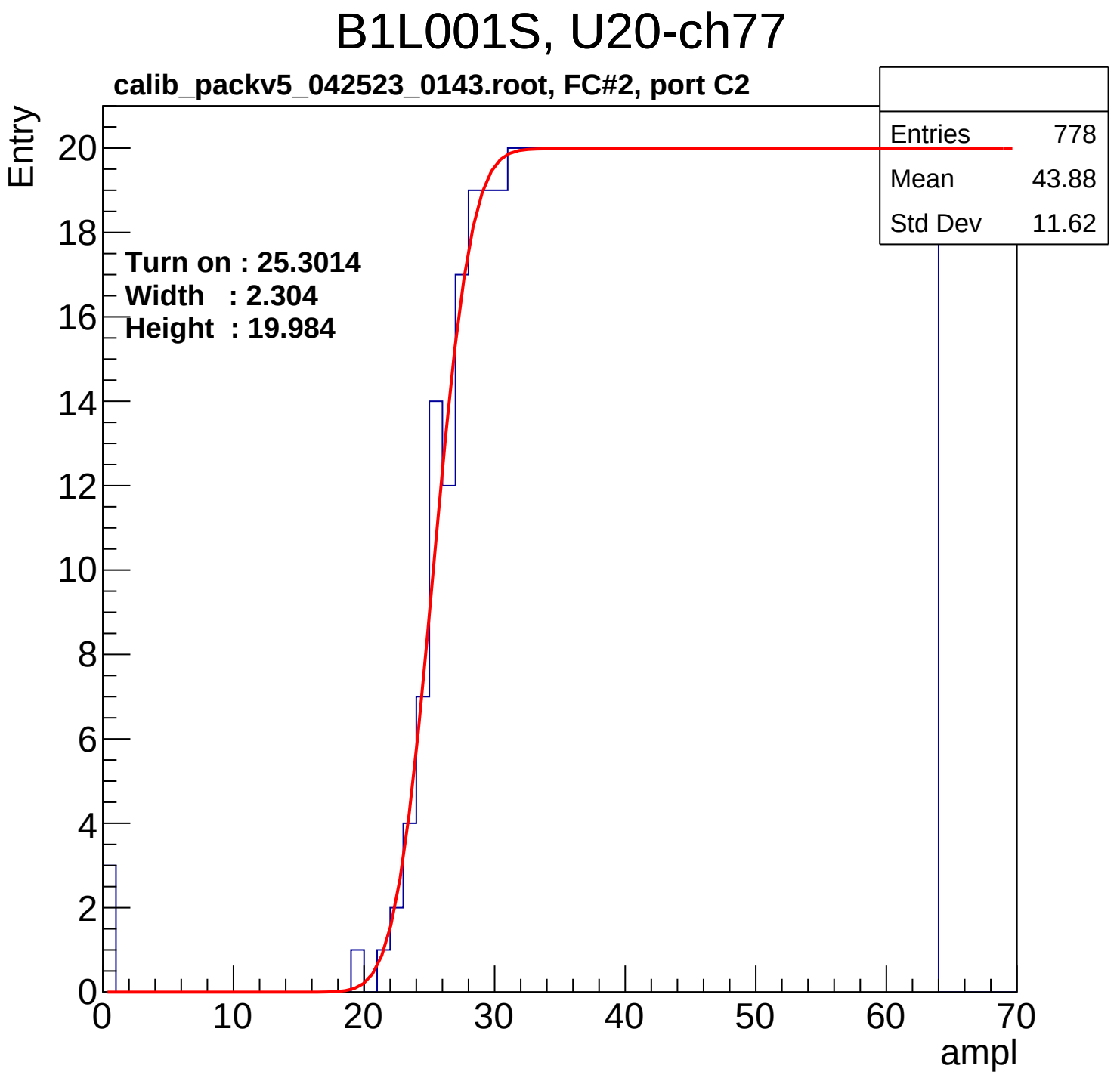
B1L001S, U20-ch77
calib_packv5_042523_0143.root, FC#2, port C2
Entries 778
Mean 43.88
Std Dev 11.62
Turn on : 25.3014
Width : 2.304
Height : 19.984
Entry
ampl
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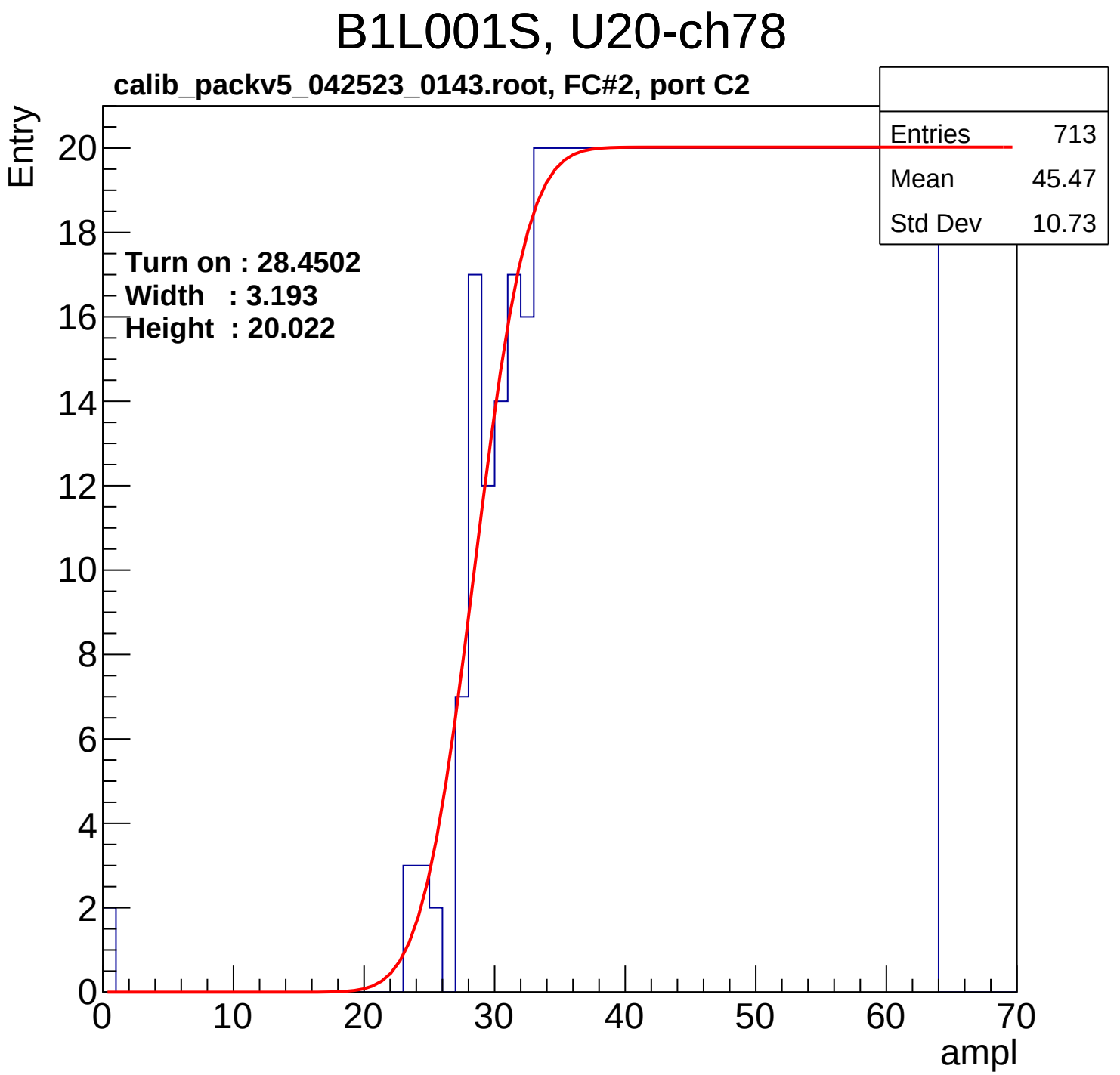
B1L001S, U20-ch78
calib_packv5_042523_0143.root, FC#2, port C2
Entries 713
Mean 45.47
Std Dev 10.73
Turn on : 28.4502
Width : 3.193
Height : 20.022
Entry
ampl
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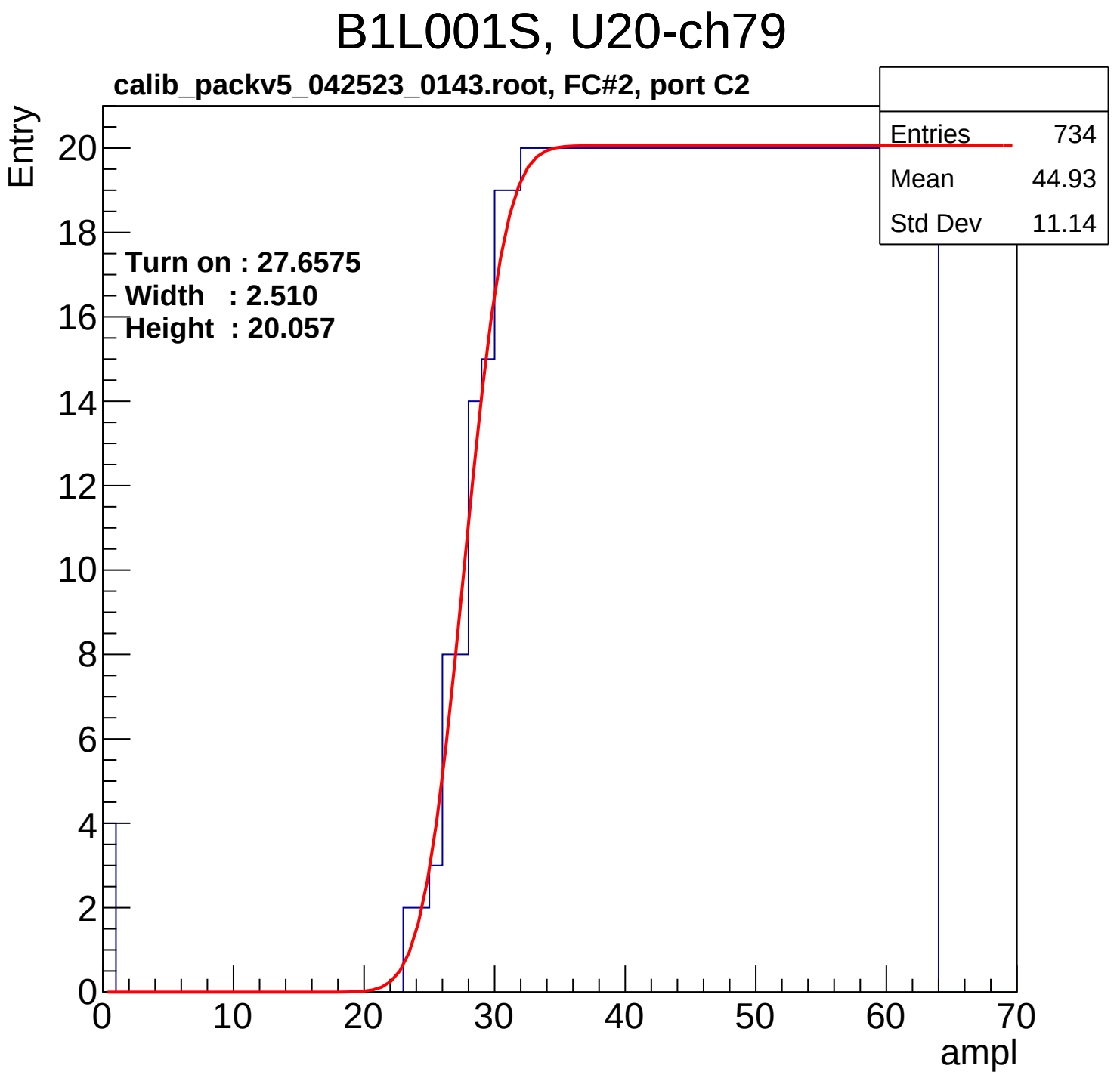
B1L001S, U20-ch79
calib_packv5_042523_0143.root, FC#2, port C2
Entries 734
Mean 44.93
Std Dev 11.14
Turn on : 27.6575
Width : 2.510
Height : 20.057
Entry
ampl
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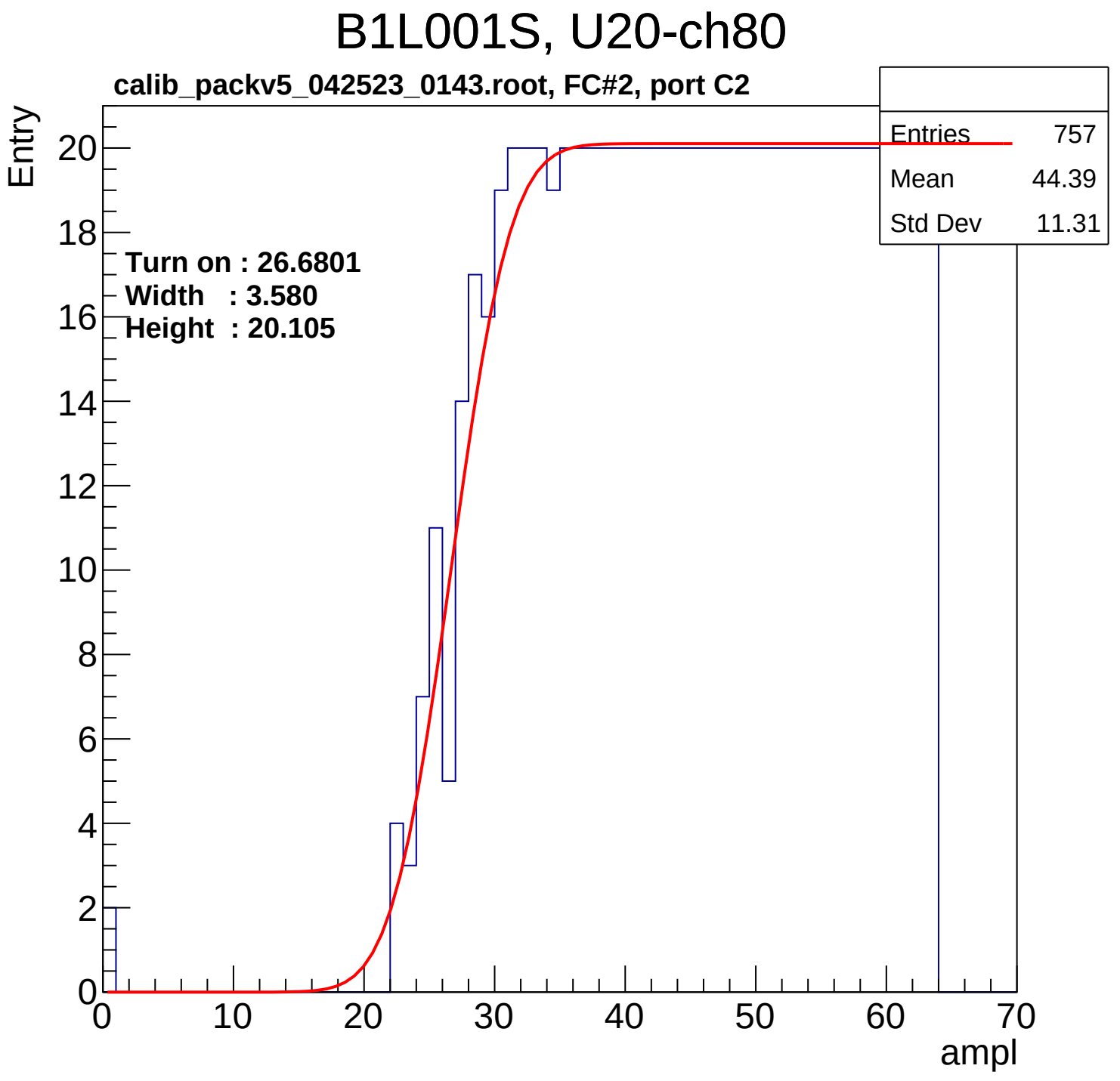
B1L001S, U20-ch80
calib_packv5_042523_0143.root, FC#2, port C2
Entries 757
Mean 44.39
Std Dev 11.31
Turn on : 26.6801
Width : 3.580
Height : 20.105
Entry
ampl
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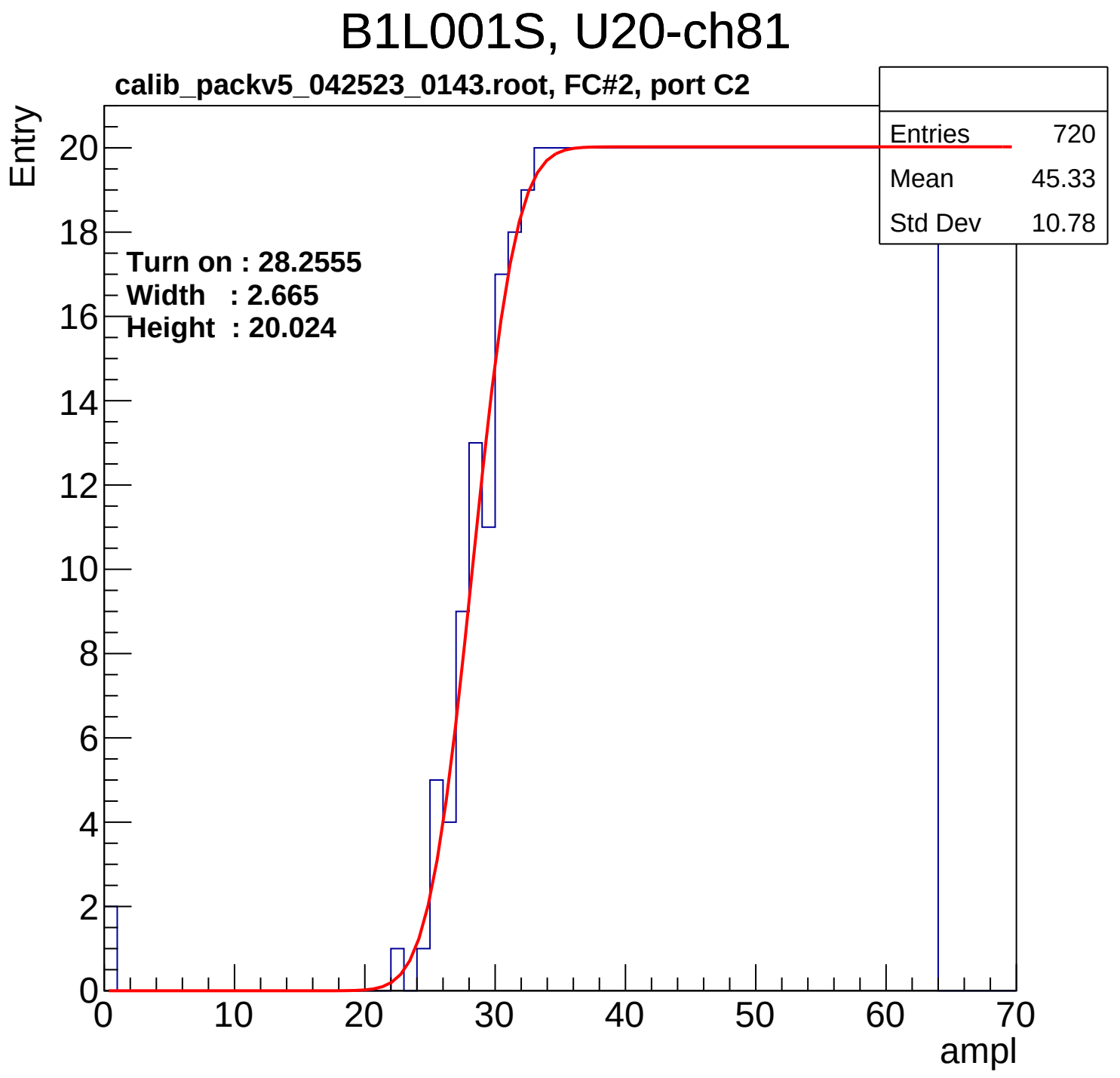
B1L001S, U20-ch81
calib_packv5_042523_0143.root, FC#2, port C2
Entries 720
Mean 45.33
Std Dev 10.78
Turn on : 28.2555
Width : 2.665
Height : 20.024
Entry
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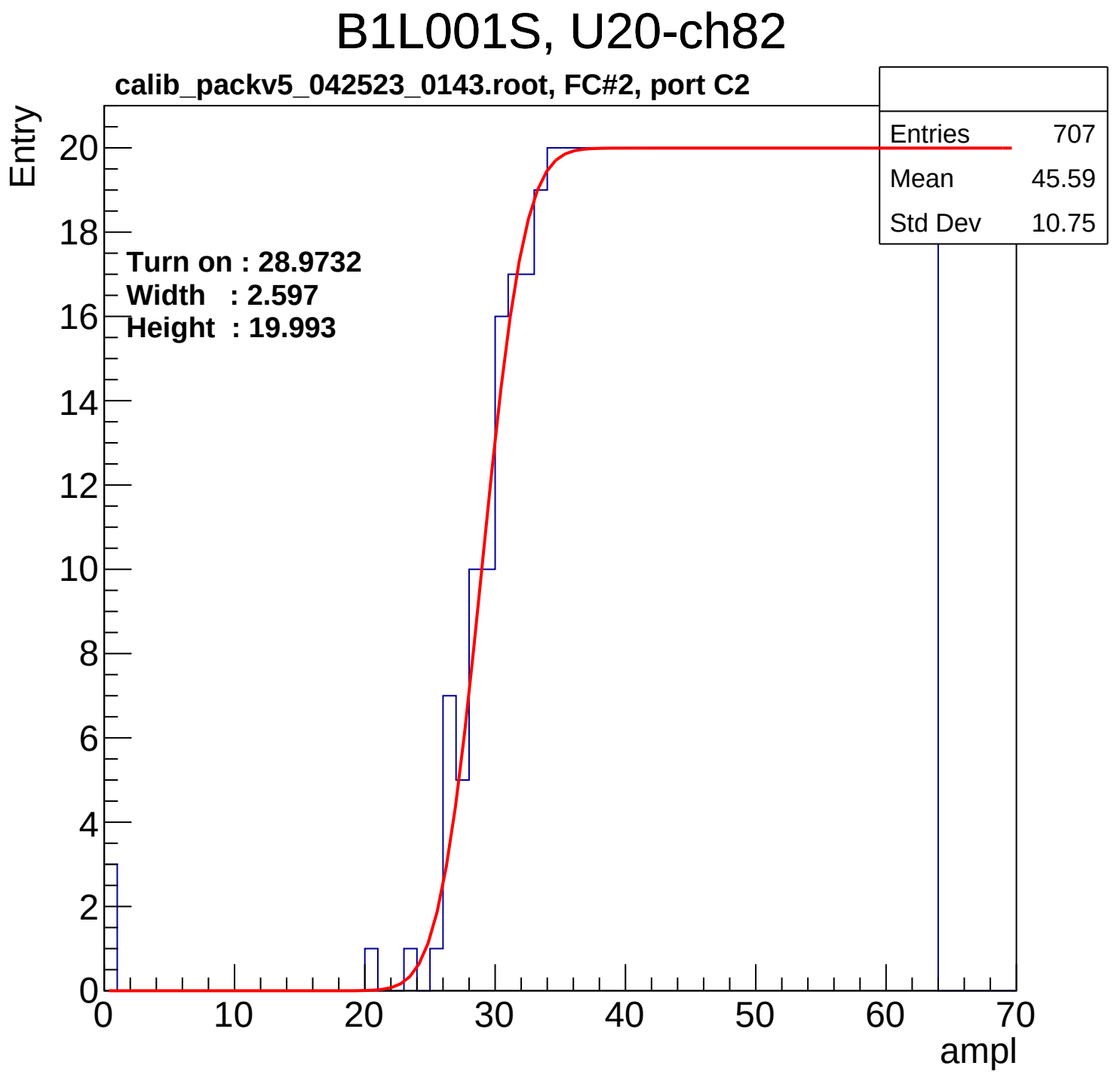
B1L001S, U20-ch82
calib_packv5_042523_0143.root, FC#2, port C2
Entries 707
Mean 45.59
Std Dev 10.75
Turn on : 28.9732
Width : 2.597
Height : 19.993
Entry
ampl
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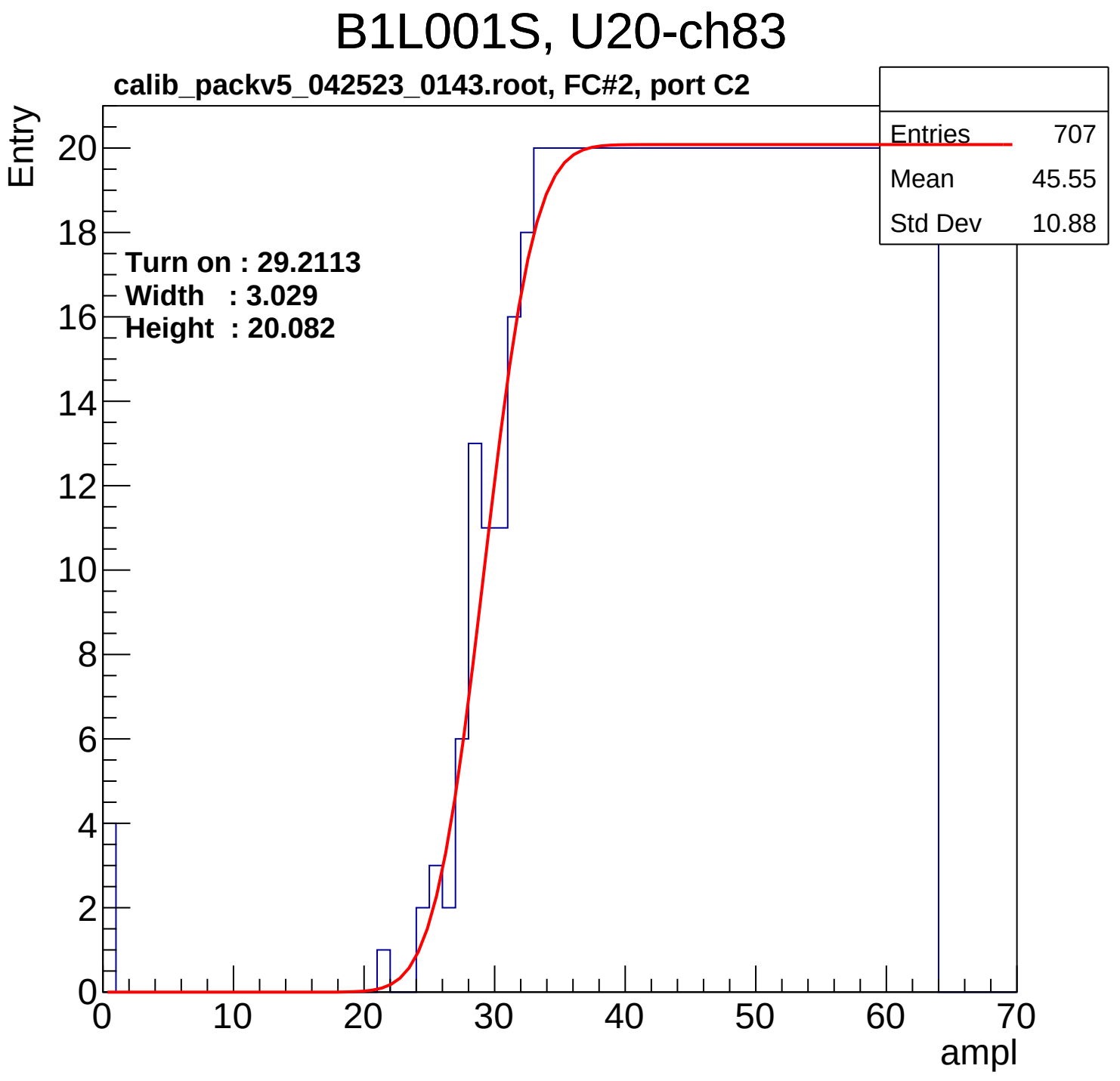
B1L001S, U20-ch83
calib_packv5_042523_0143.root, FC#2, port C2
Entries 707
Mean 45.55
Std Dev 10.88
Turn on : 29.2113
Width : 3.029
Height : 20.082
Entry
ampl
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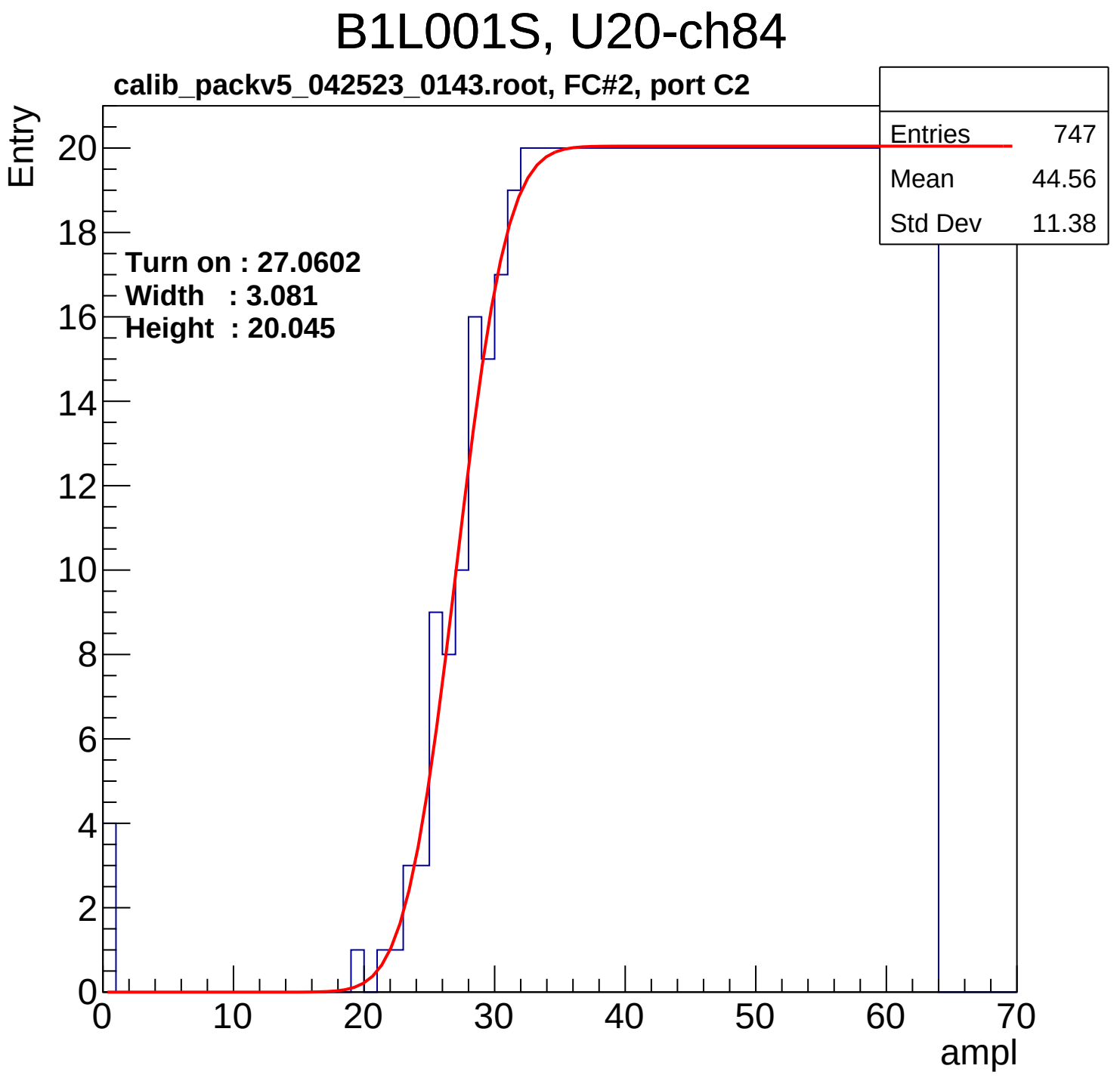
B1L001S, U20-ch84
calib_packv5_042523_0143.root, FC#2, port C2
Entries 747
Mean 44.56
Std Dev 11.38
Turn on : 27.0602
Width : 3.081
Height : 20.045
Entry
ampl
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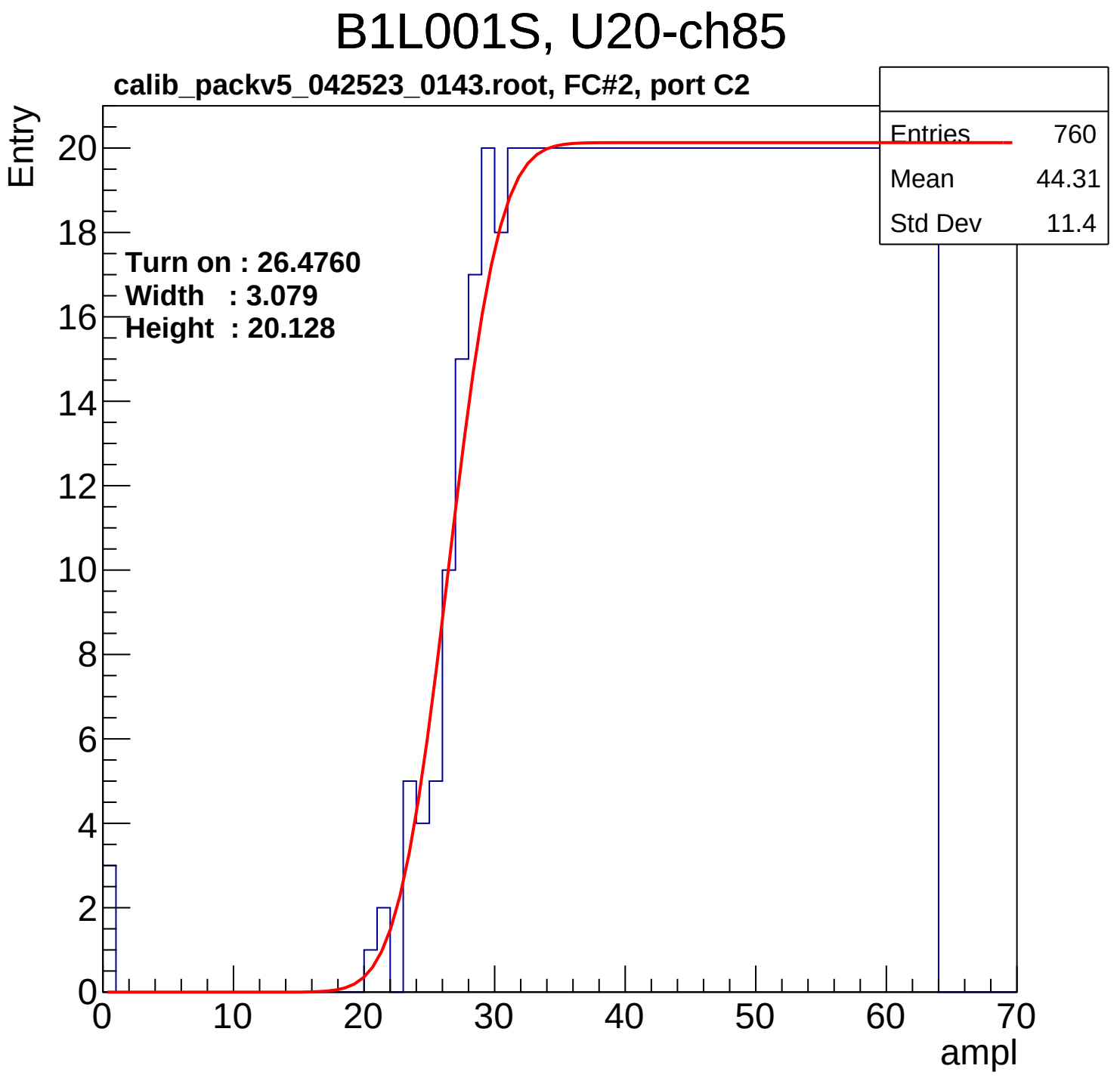
B1L001S, U20-ch85
calib_packv5_042523_0143.root, FC#2, port C2
Entries 760
Mean 44.31
Std Dev 11.4
Turn on : 26.4760
Width : 3.079
Height : 20.128
Entry
ampl
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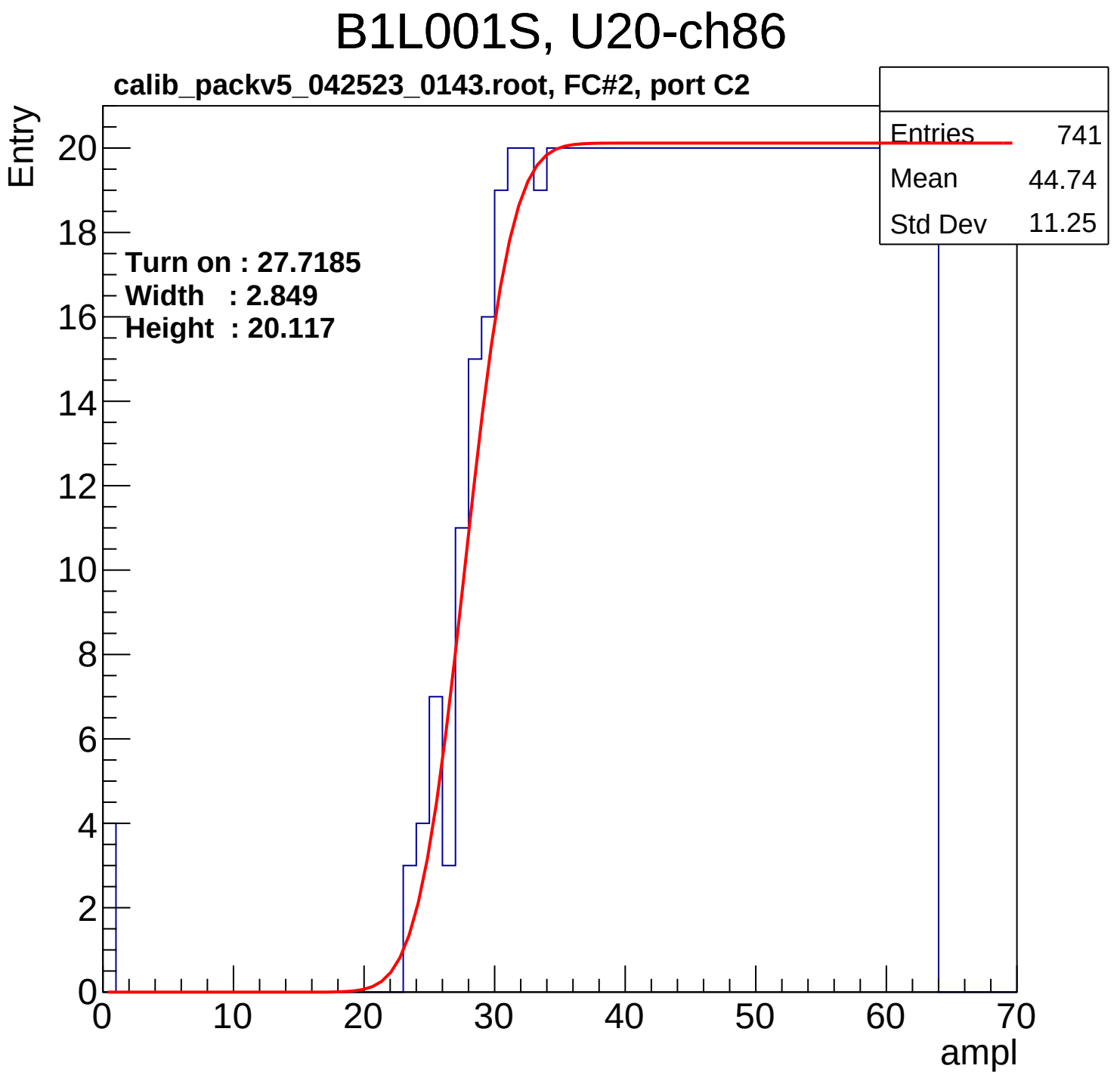
B1L001S, U20-ch86
calib_packv5_042523_0143.root, FC#2, port C2
Entries 741
Mean 44.74
Std Dev 11.25
Turn on : 27.7185
Width : 2.849
Height : 20.117
Entry
ampl
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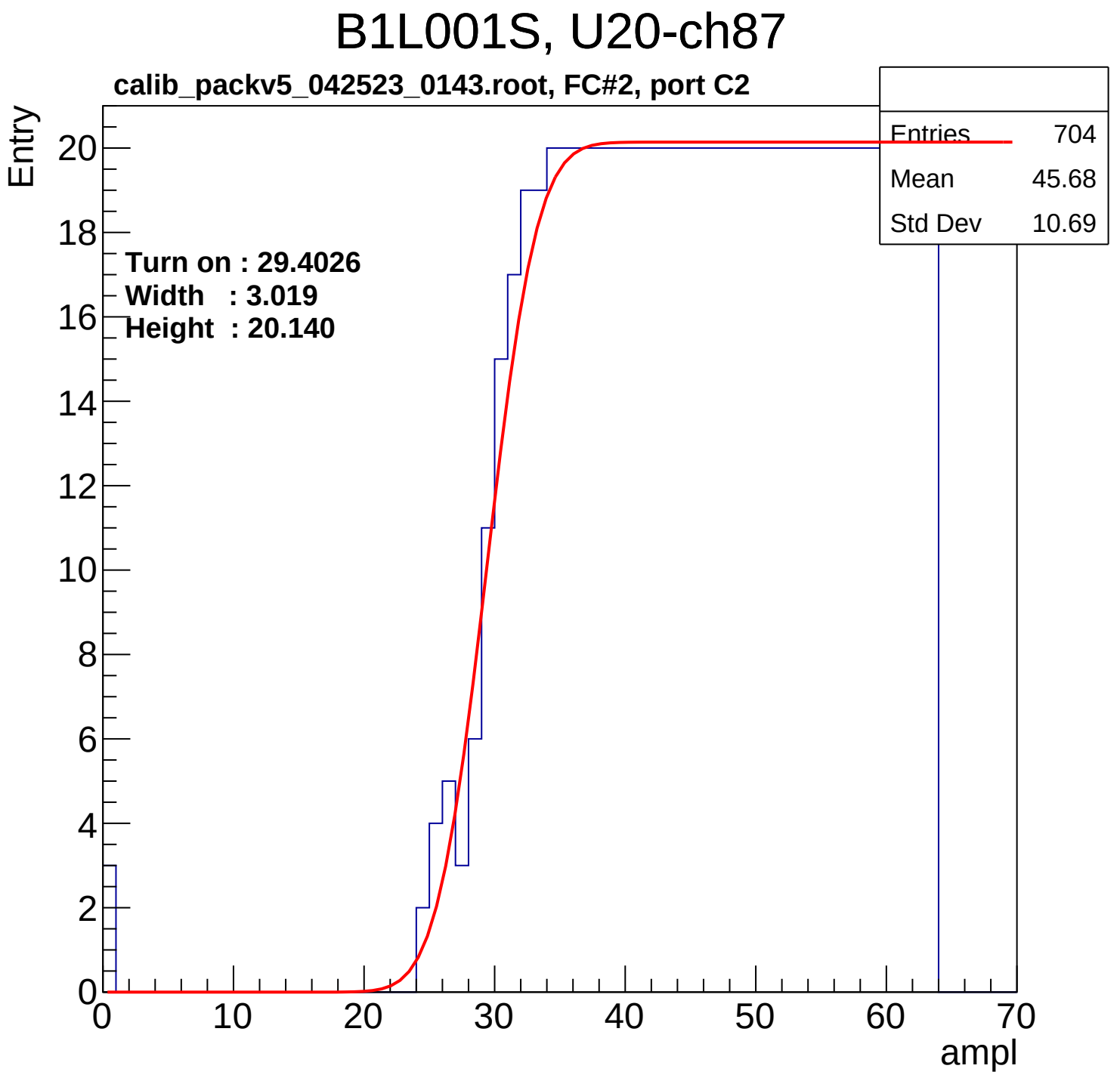
B1L001S, U20-ch87
calib_packv5_042523_0143.root, FC#2, port C2
Entries 704
Mean 45.68
Std Dev 10.69
Turn on : 29.4026
Width : 3.019
Height : 20.140
Entry
ampl
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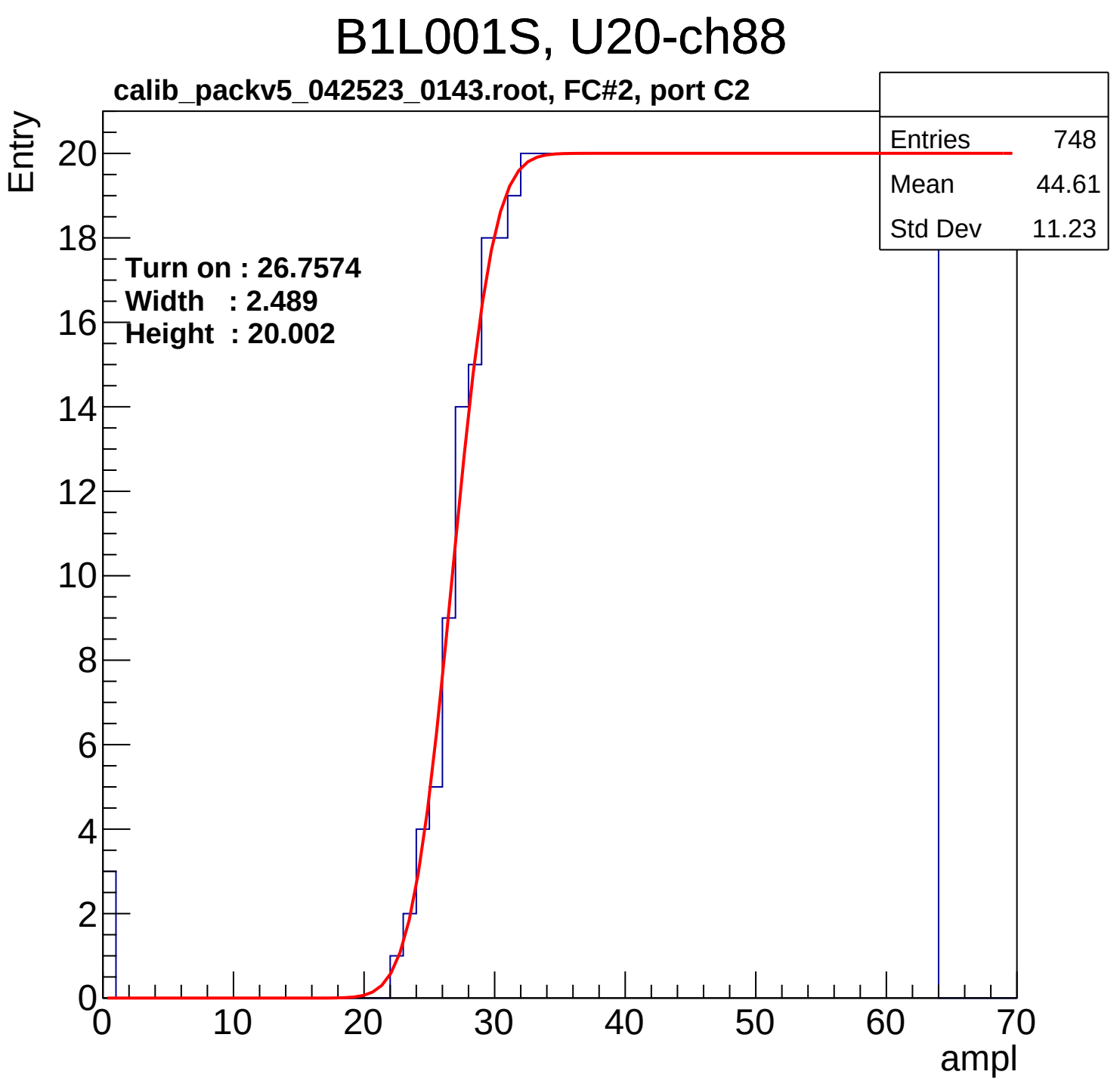
B1L001S, U20-ch88
calib_packv5_042523_0143.root, FC#2, port C2
Entries 748
Mean 44.61
Std Dev 11.23
Turn on : 26.7574
Width : 2.489
Height : 20.002
Entry
ampl
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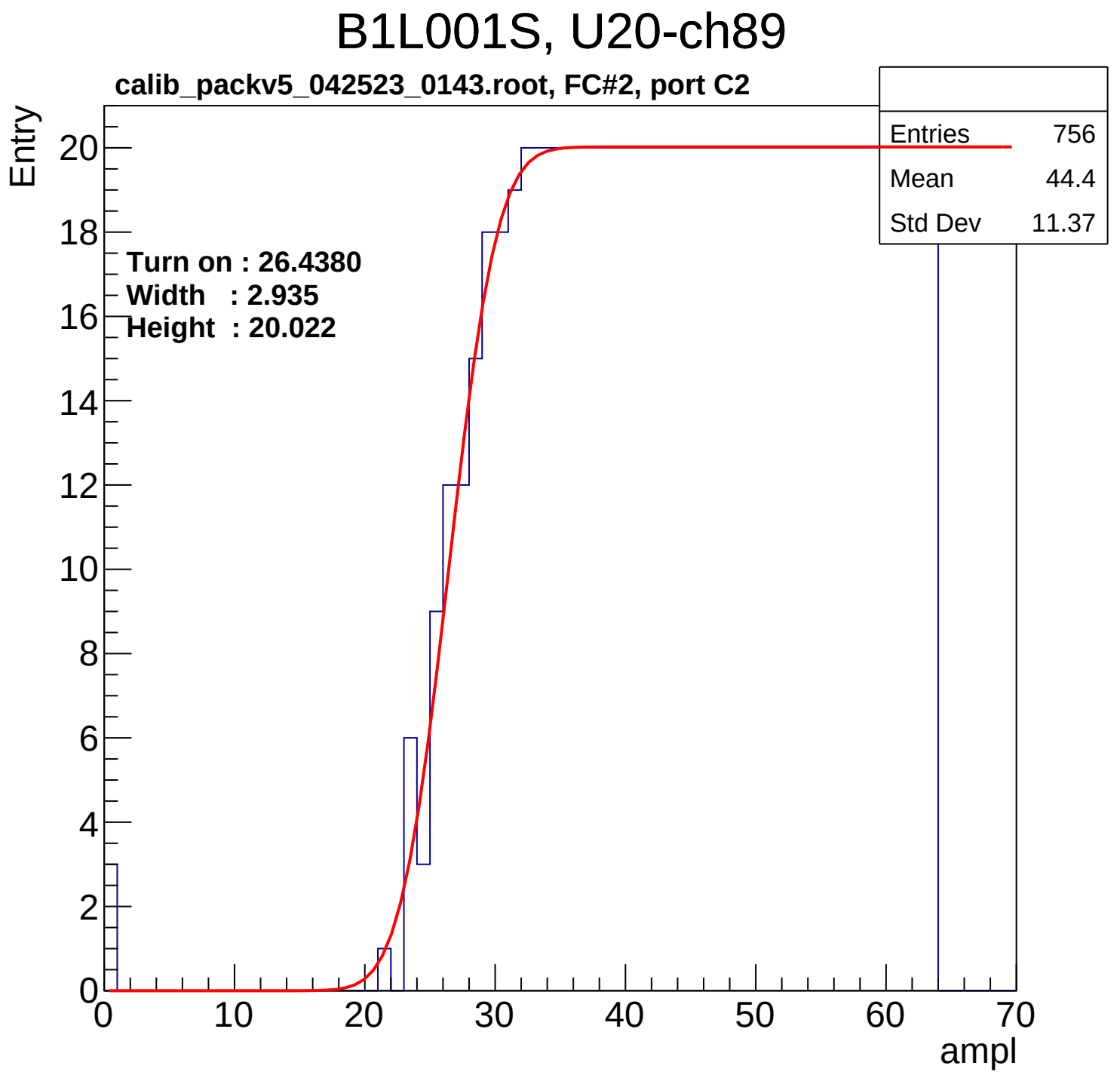
B1L001S, U20-ch89
calib_packv5_042523_0143.root, FC#2, port C2
Entries 756
Mean 44.4
Std Dev 11.37
Turn on : 26.4380
Width : 2.935
Height : 20.022
Entry
ampl
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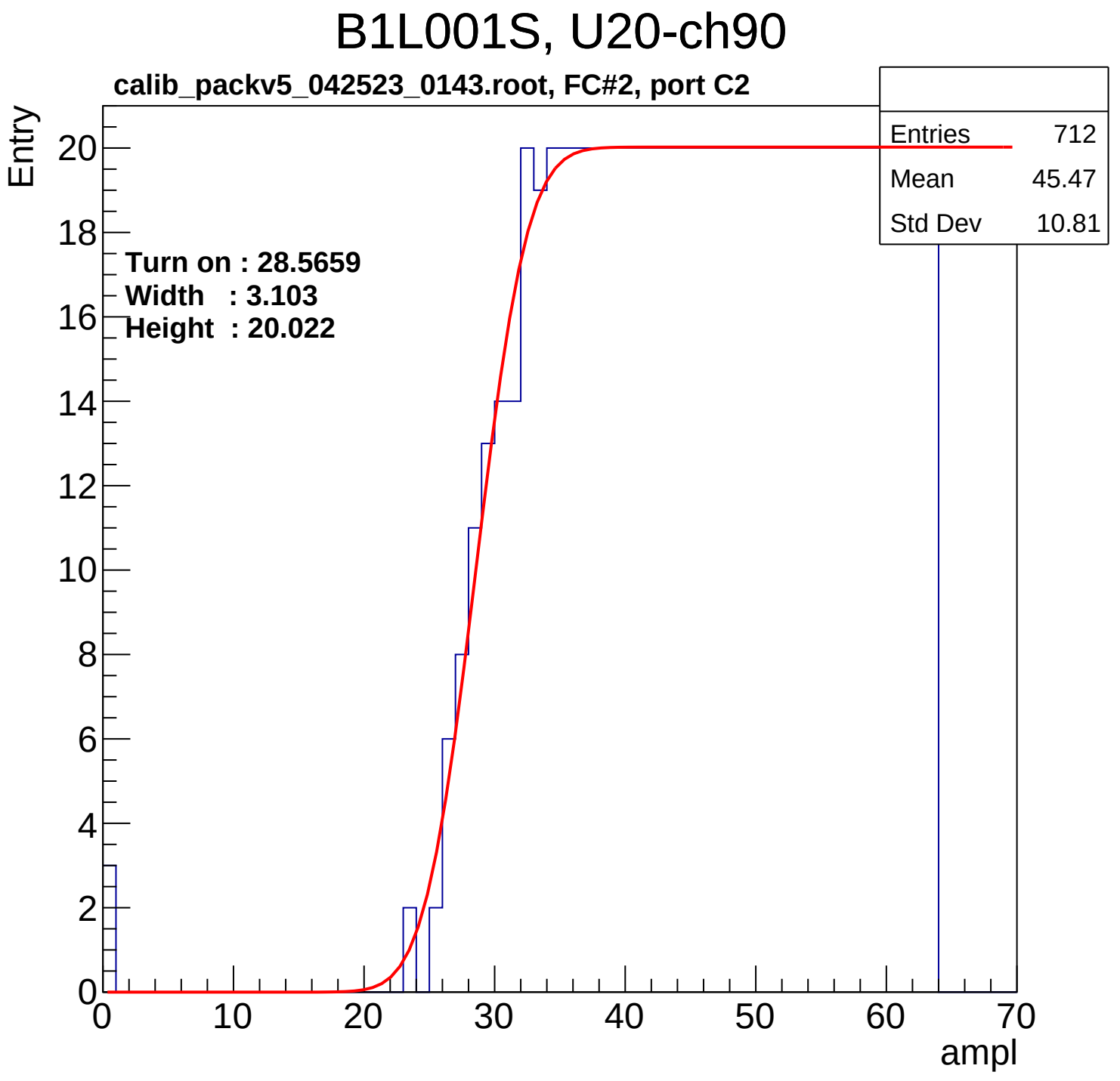
B1L001S, U20-ch90
calib_packv5_042523_0143.root, FC#2, port C2
Entries 712
Mean 45.47
Std Dev 10.81
Turn on : 28.5659
Width : 3.103
Height : 20.022
Entry
ampl
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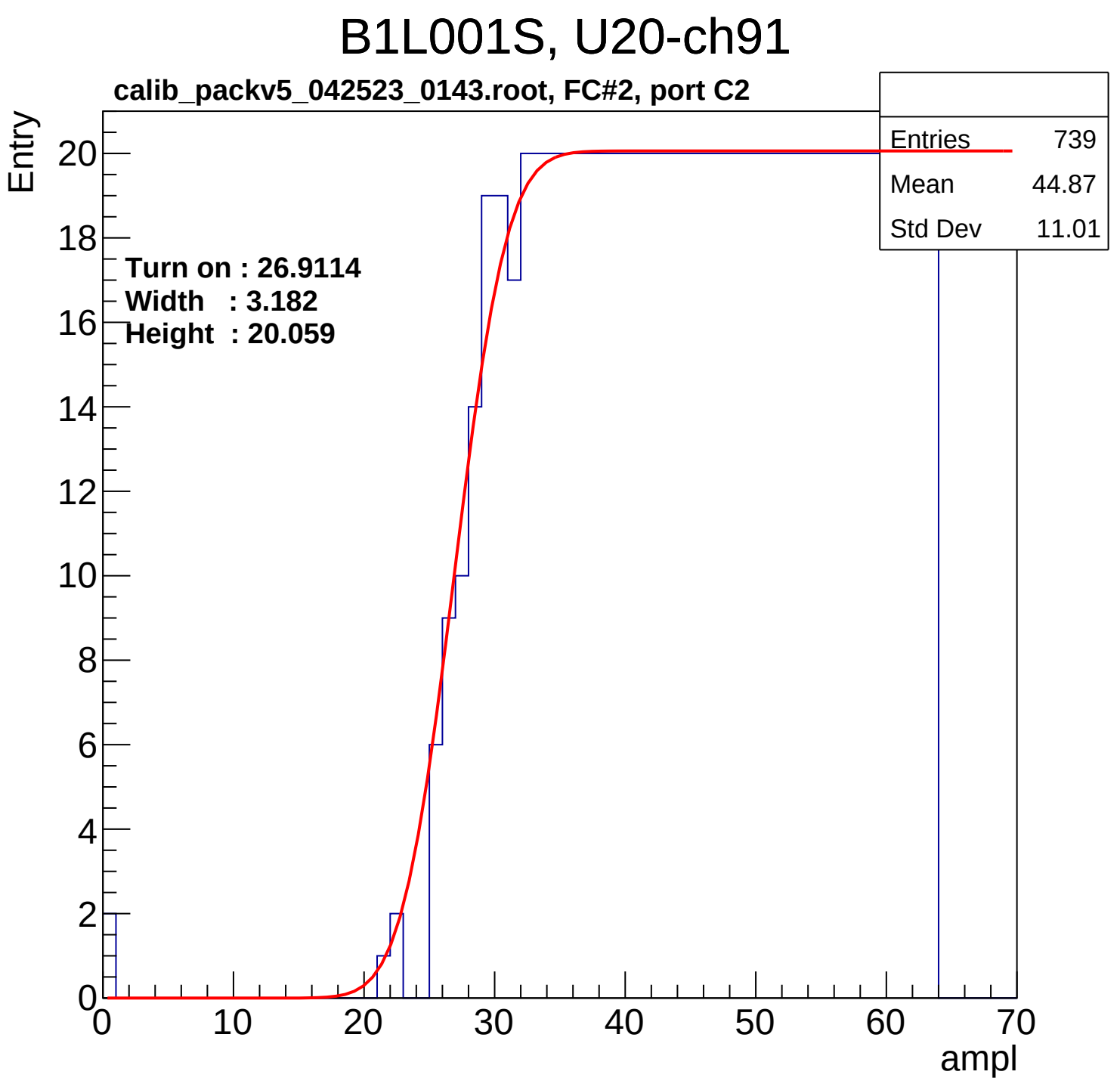
B1L001S, U20-ch91
calib_packv5_042523_0143.root, FC#2, port C2
Entries 739
Mean 44.87
Std Dev 11.01
Turn on : 26.9114
Width : 3.182
Height : 20.059
Entry
ampl
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6
8
10
12
14
16
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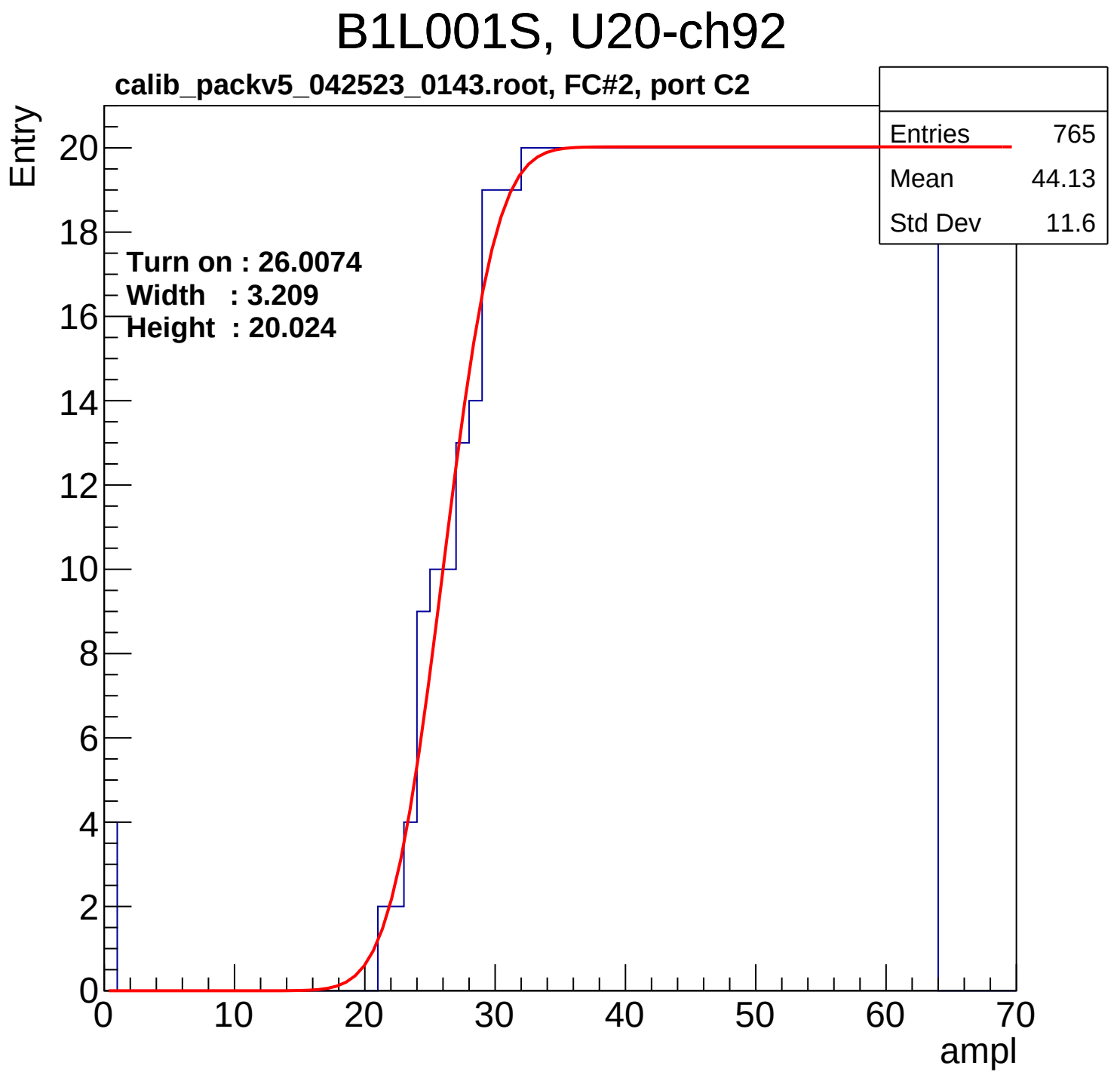
B1L001S, U20-ch92
calib_packv5_042523_0143.root, FC#2, port C2
Entries 765
Mean 44.13
Std Dev 11.6
Turn on : 26.0074
Width : 3.209
Height : 20.024
Entry
ampl
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6
8
10
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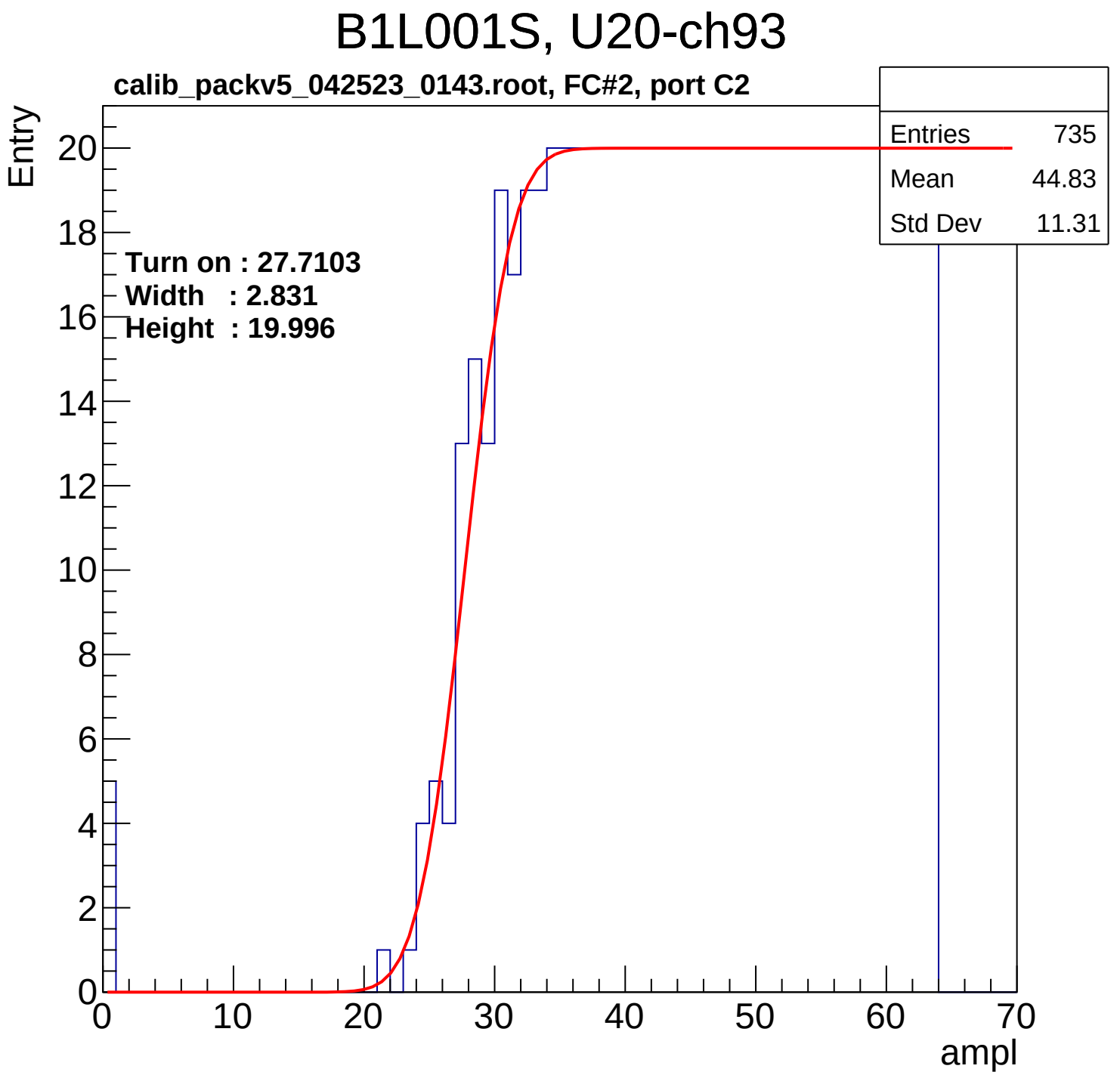
B1L001S, U20-ch93
calib_packv5_042523_0143.root, FC#2, port C2
Entries 735
Mean 44.83
Std Dev 11.31
Turn on : 27.7103
Width : 2.831
Height : 19.996
Entry
ampl
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6
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14
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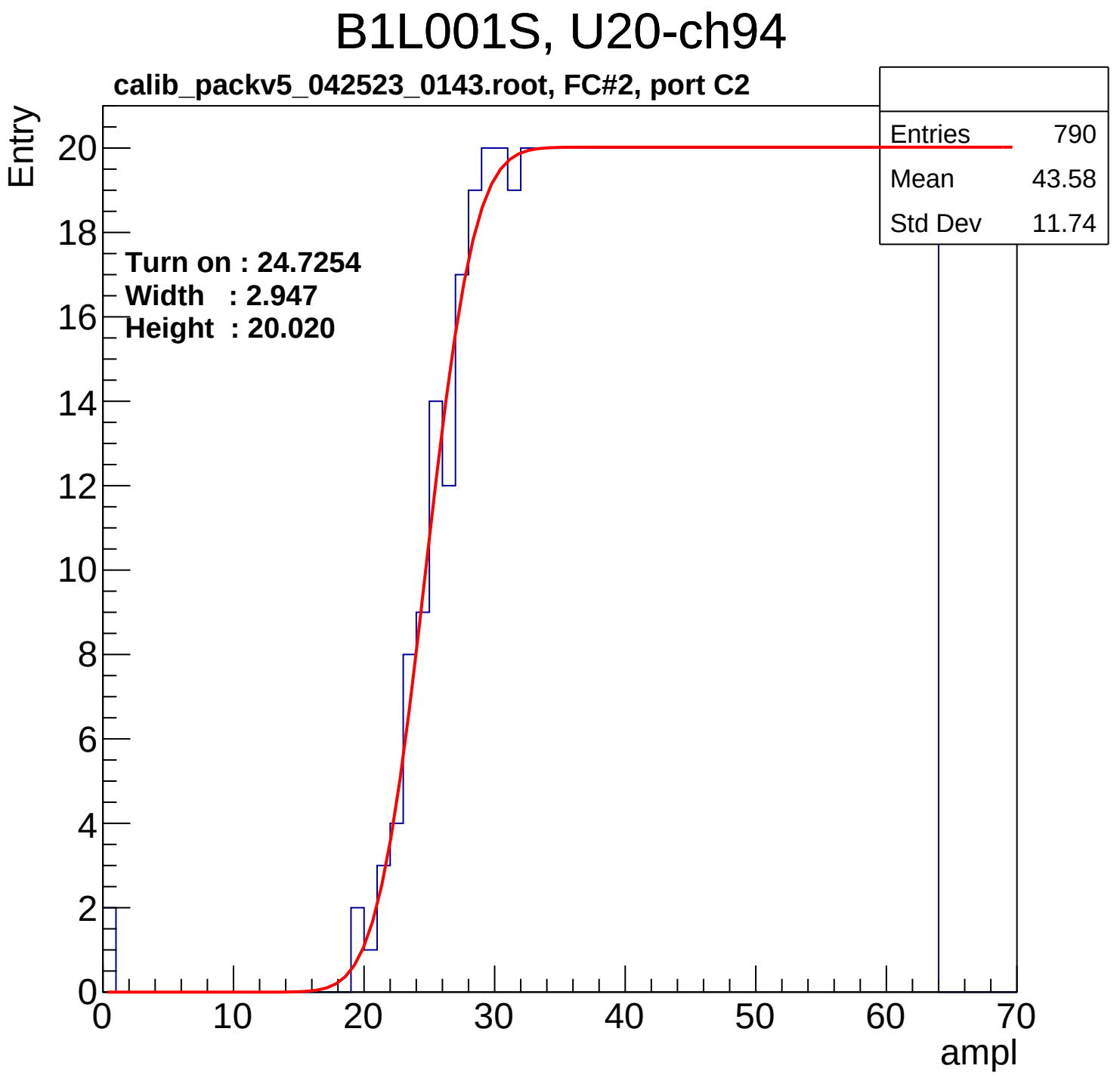
B1L001S, U20-ch94
calib_packv5_042523_0143.root, FC#2, port C2
Entries 790
Mean 43.58
Std Dev 11.74
Turn on : 24.7254
Width : 2.947
Height : 20.020
Entry
ampl
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6
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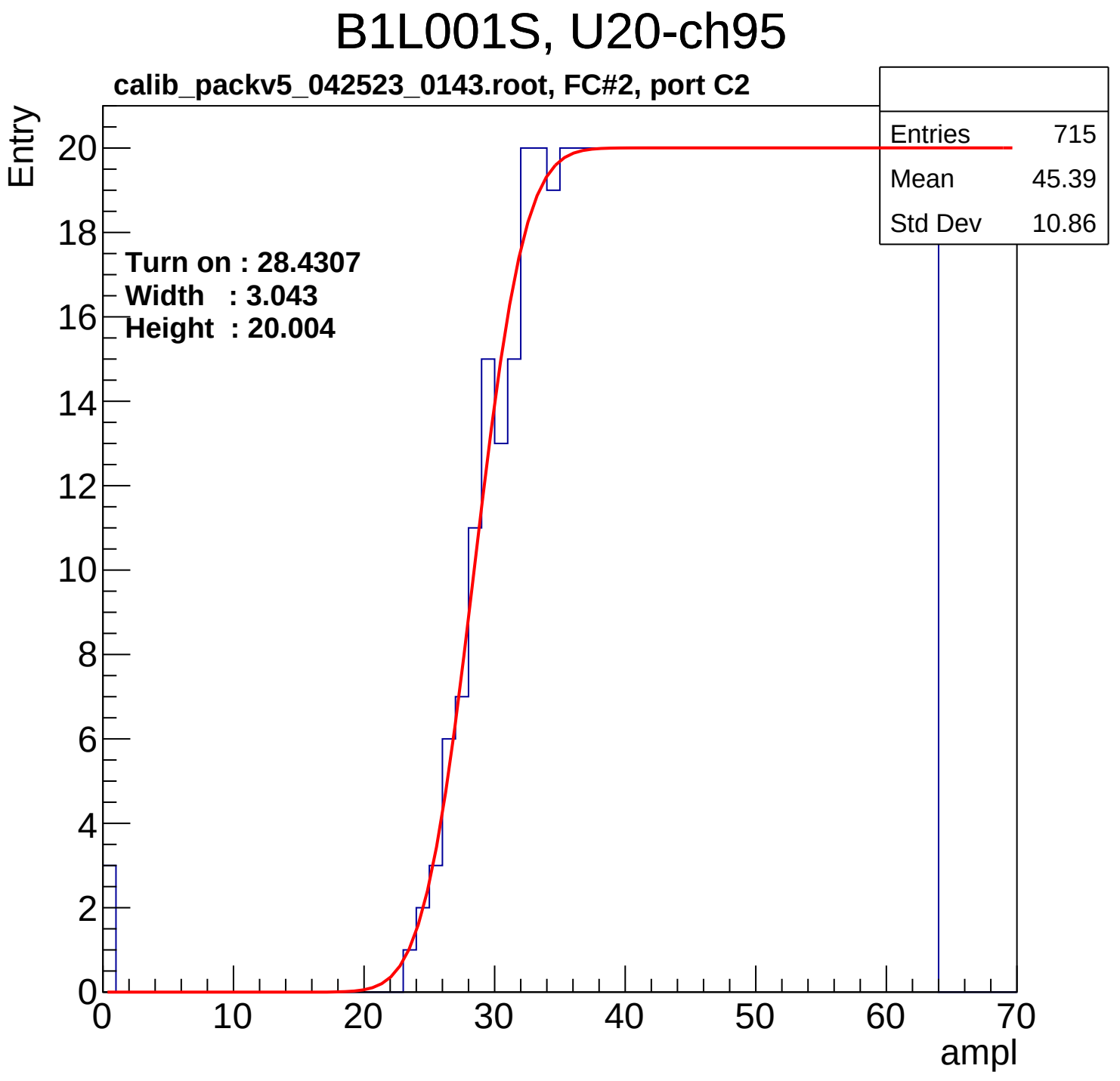
B1L001S, U20-ch95
calib_packv5_042523_0143.root, FC#2, port C2
Entries 715
Mean 45.39
Std Dev 10.86
Turn on : 28.4307
Width : 3.043
Height : 20.004
Entry
ampl
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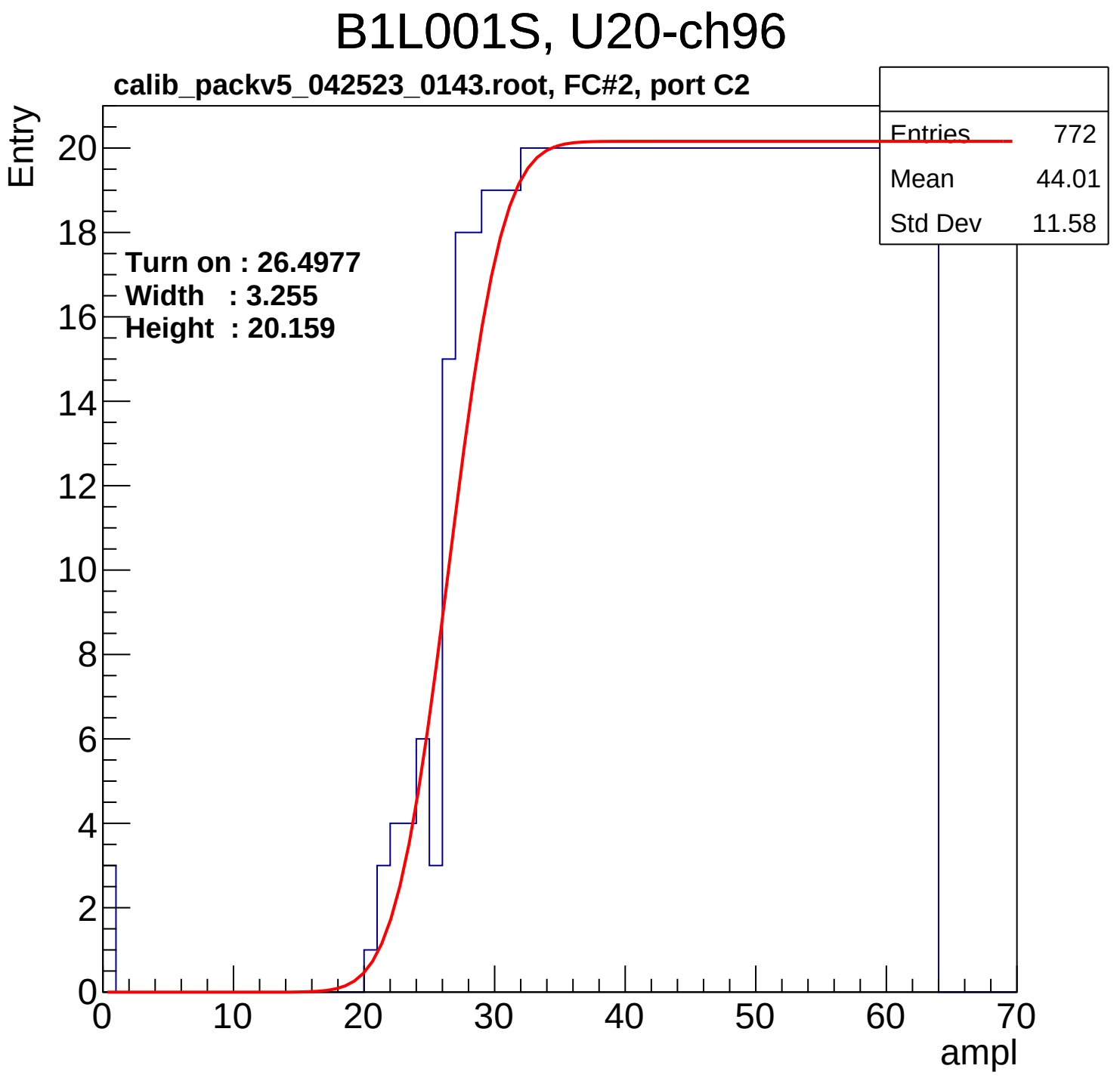
B1L001S, U20-ch96
calib_packv5_042523_0143.root, FC#2, port C2
Entries 772
Mean 44.01
Std Dev 11.58
Turn on : 26.4977
Width : 3.255
Height : 20.159
Entry
ampl
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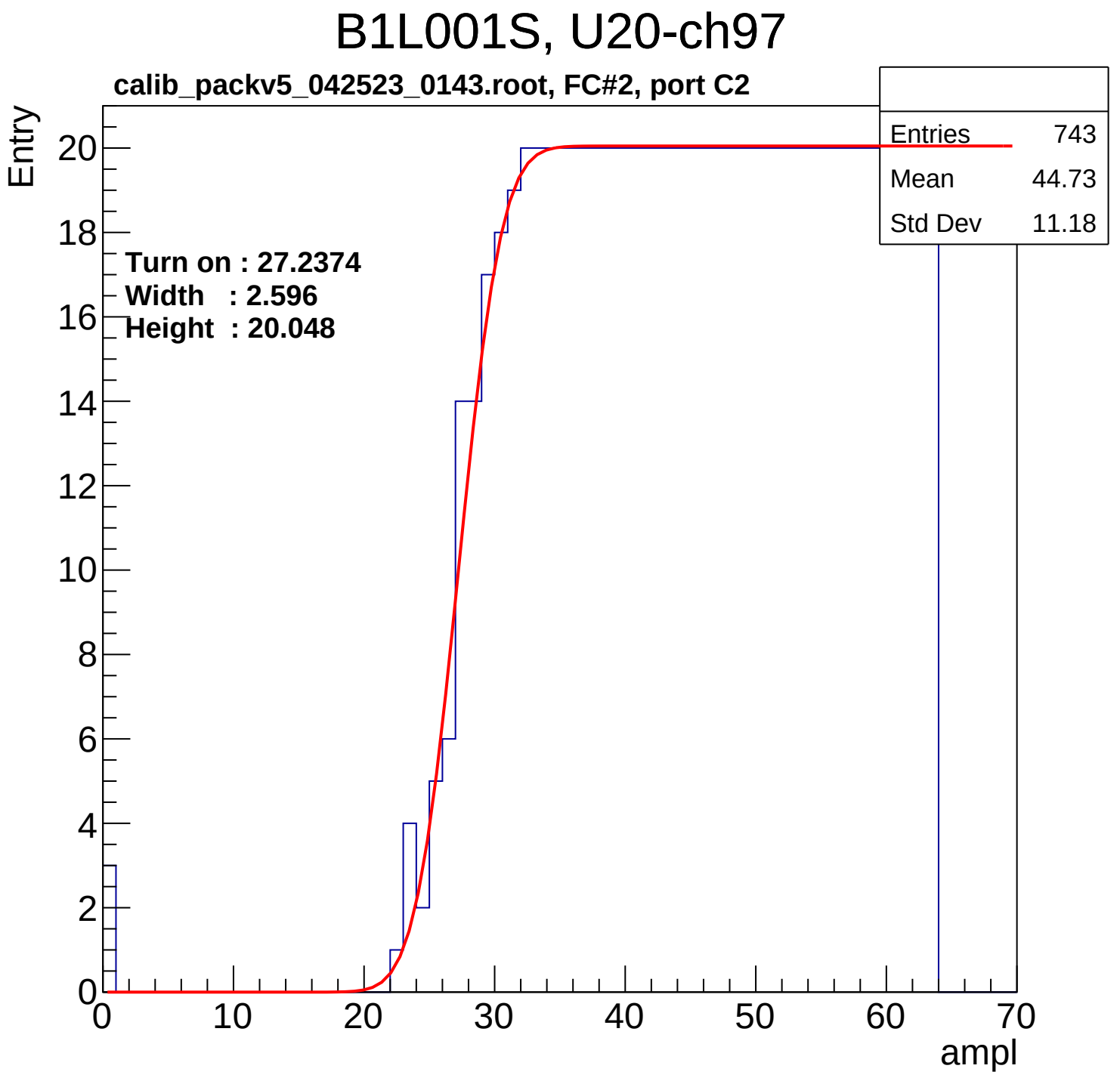
B1L001S, U20-ch97
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.73
Std Dev 11.18
Turn on : 27.2374
Width : 2.596
Height : 20.048
Entry
ampl
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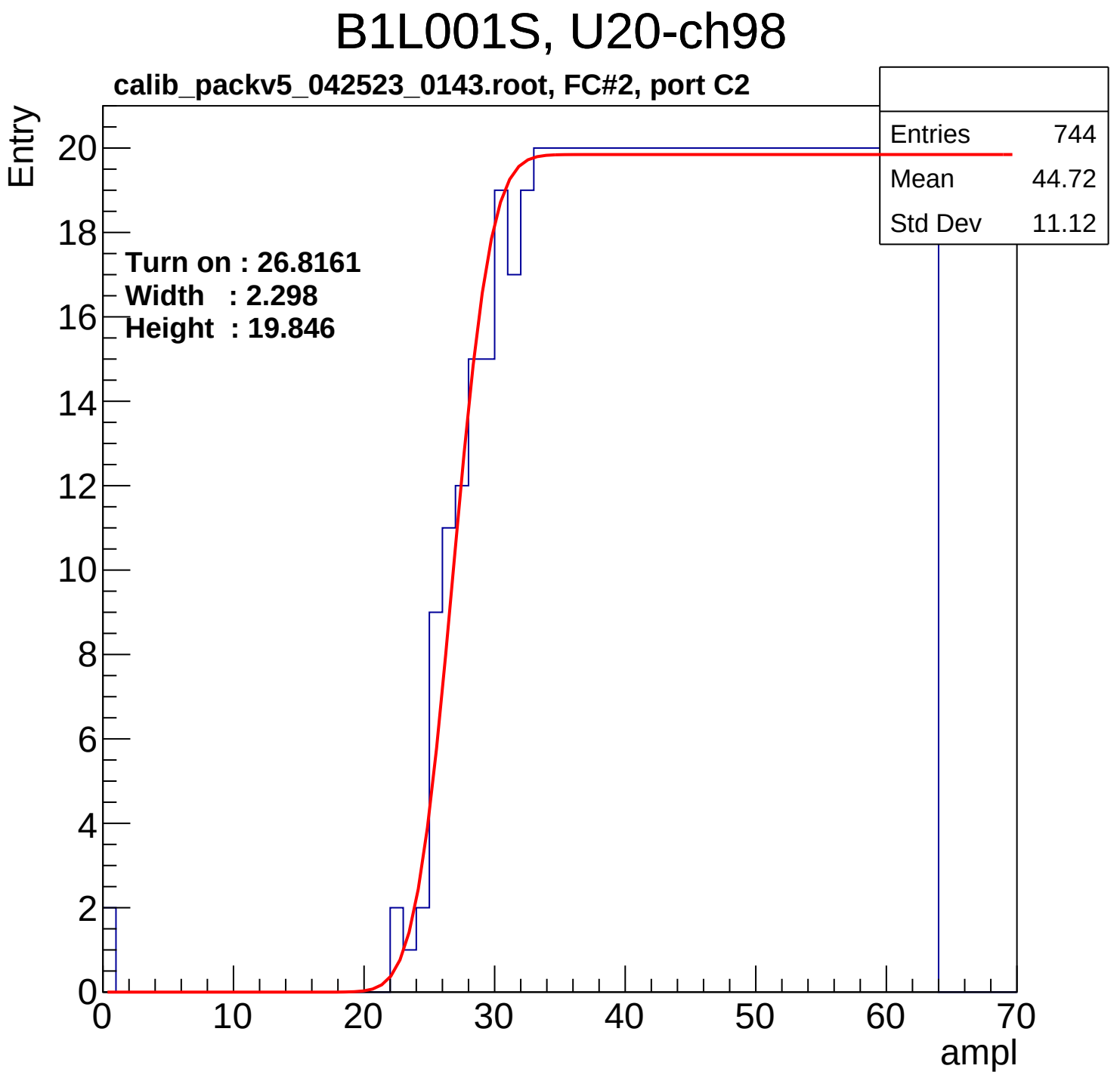
B1L001S, U20-ch98
calib_packv5_042523_0143.root, FC#2, port C2
Entries 744
Mean 44.72
Std Dev 11.12
Turn on : 26.8161
Width : 2.298
Height : 19.846
Entry
ampl
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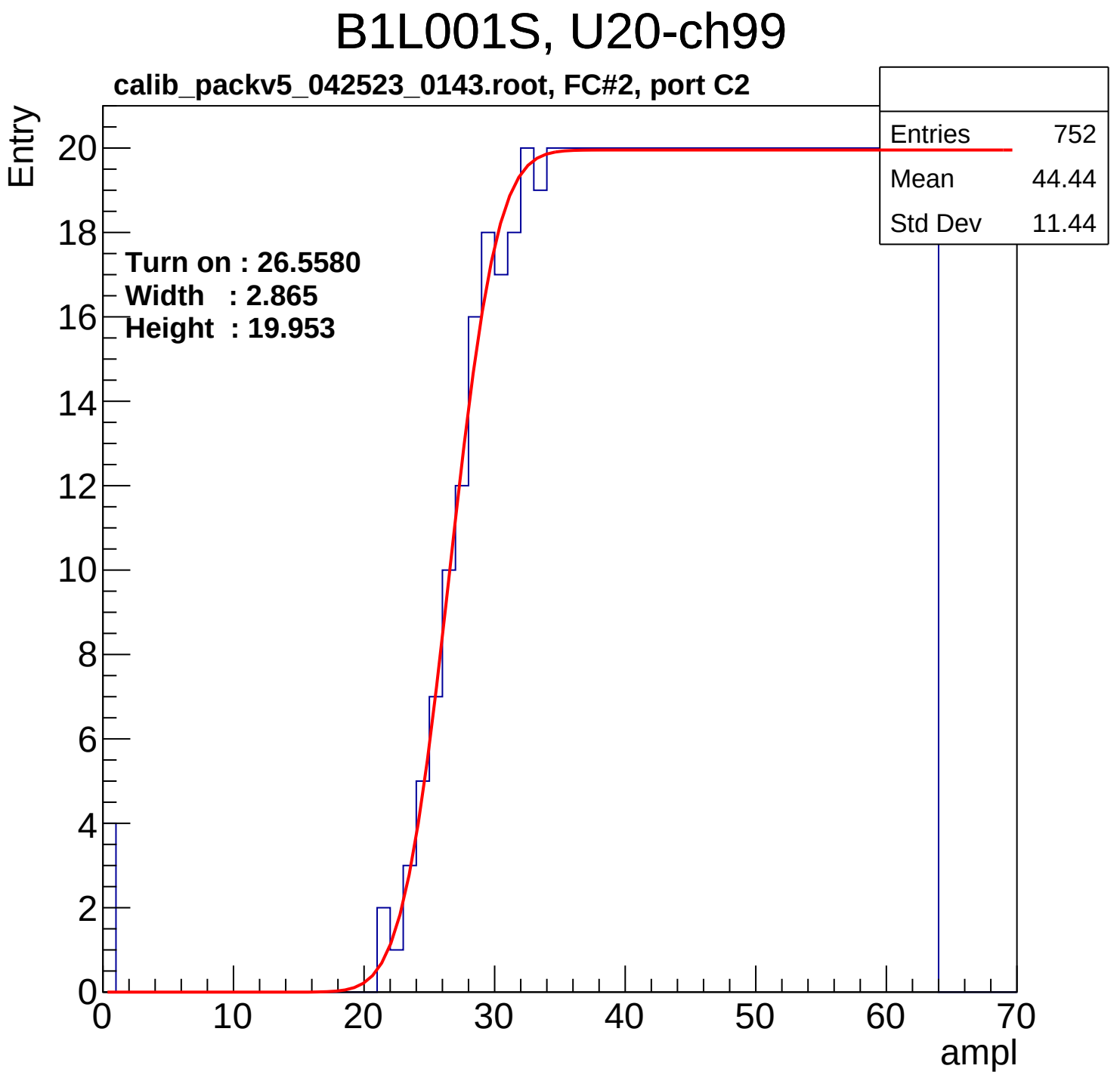
B1L001S, U20-ch99
calib_packv5_042523_0143.root, FC#2, port C2
Entries 752
Mean 44.44
Std Dev 11.44
Turn on : 26.5580
Width : 2.865
Height : 19.953
Entry
ampl
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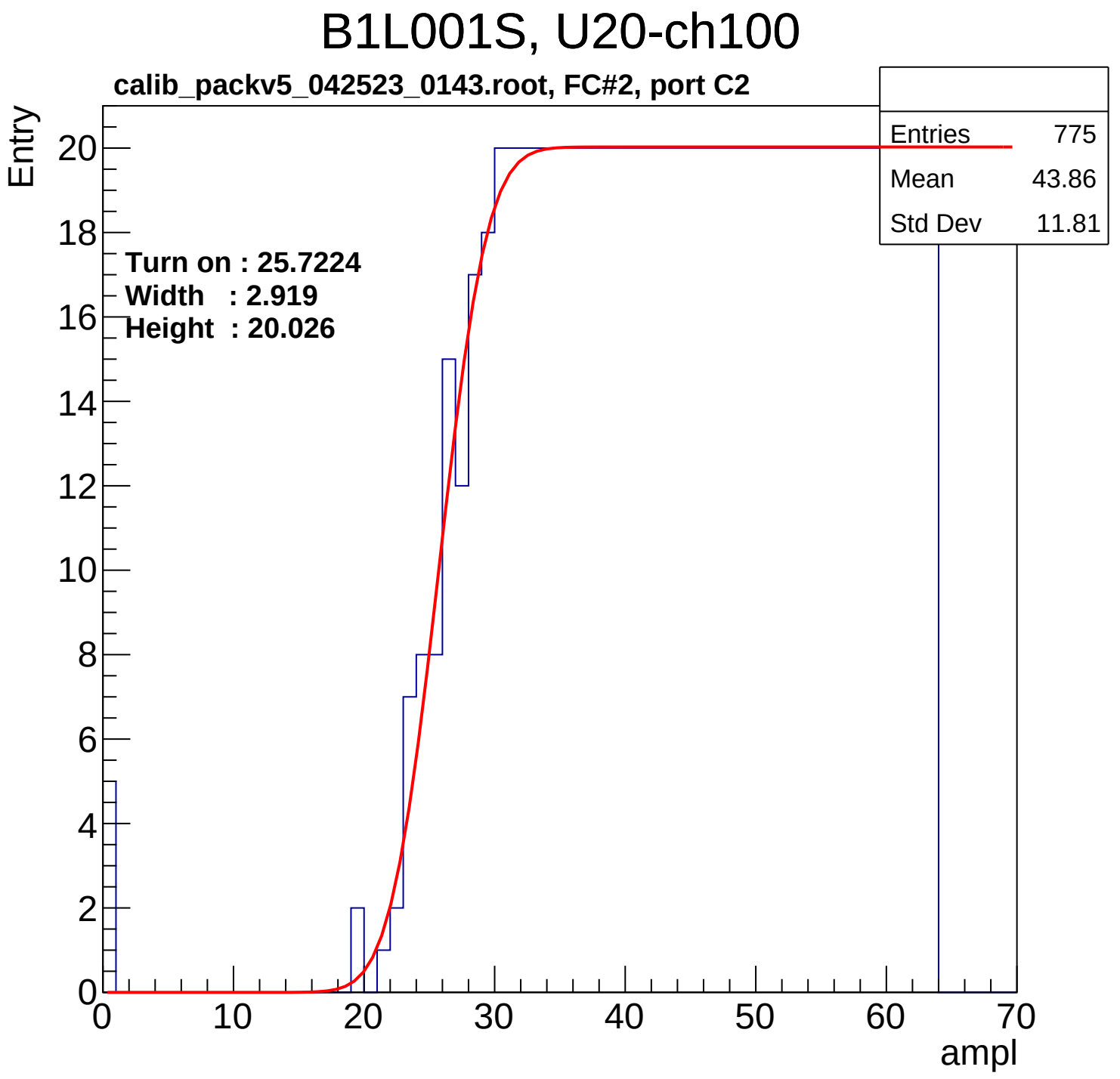
B1L001S, U20-ch100
calib_packv5_042523_0143.root, FC#2, port C2
Entries 775
Mean 43.86
Std Dev 11.81
Turn on : 25.7224
Width : 2.919
Height : 20.026
Entry
ampl
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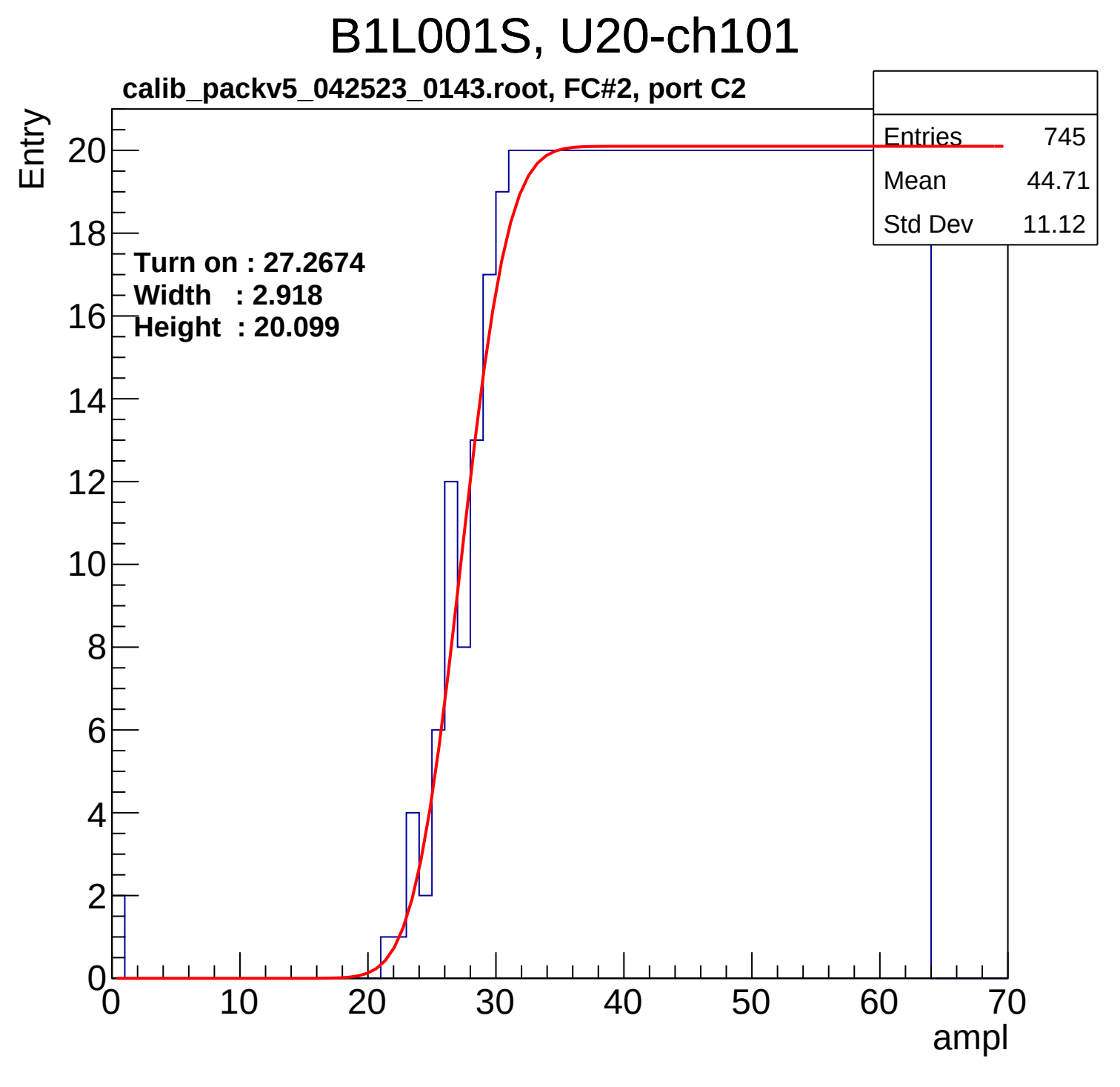
B1L001S, U20-ch101
calib_packv5_042523_0143.root, FC#2, port C2
Entries 745
Mean 44.71
Std Dev 11.12
Turn on : 27.2674
Width : 2.918
Height : 20.099
Entry
ampl
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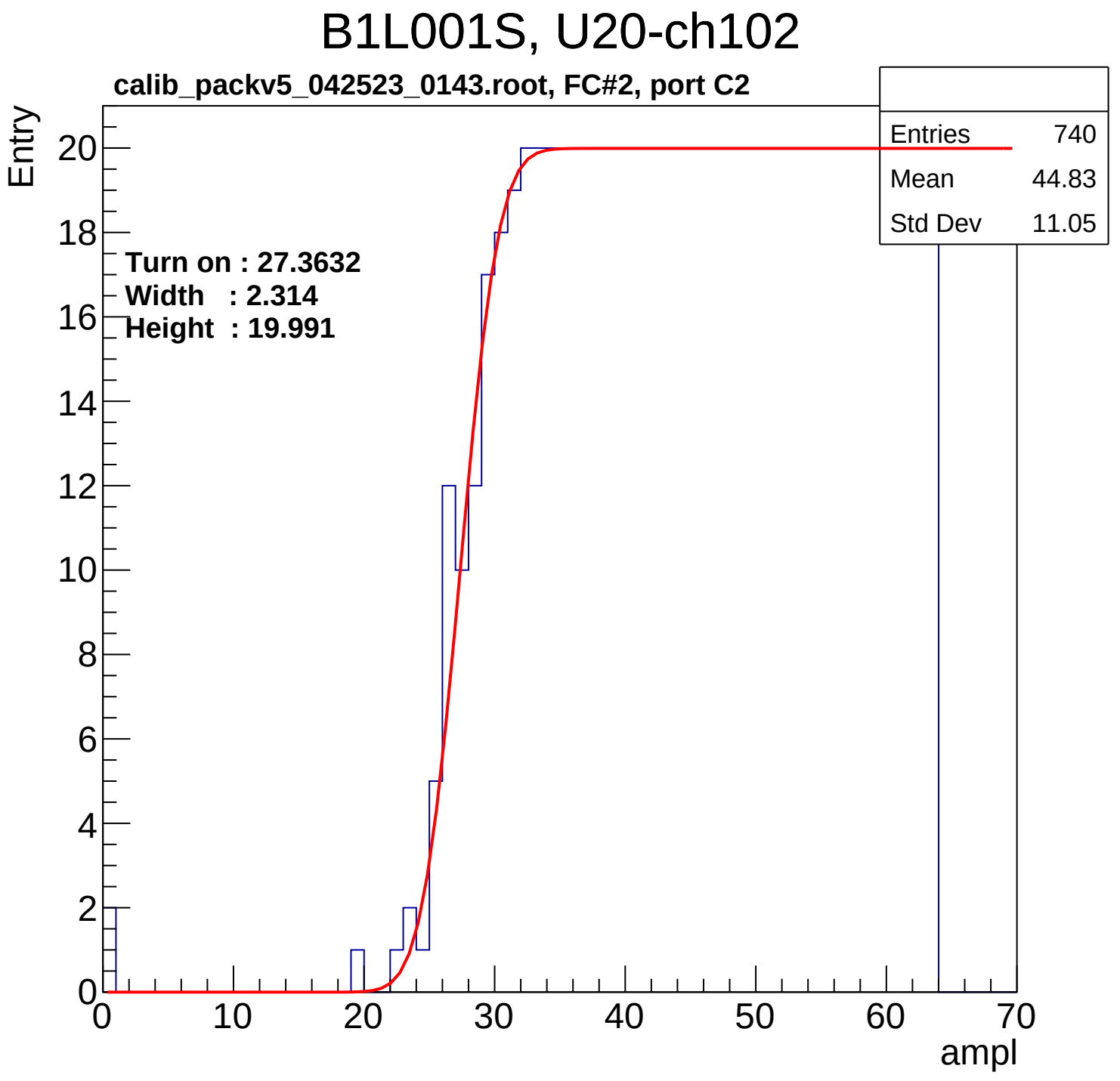
B1L001S, U20-ch102
calib_packv5_042523_0143.root, FC#2, port C2
Entries 740
Mean 44.83
Std Dev 11.05
Turn on : 27.3632
Width : 2.314
Height : 19.991
Entry
ampl
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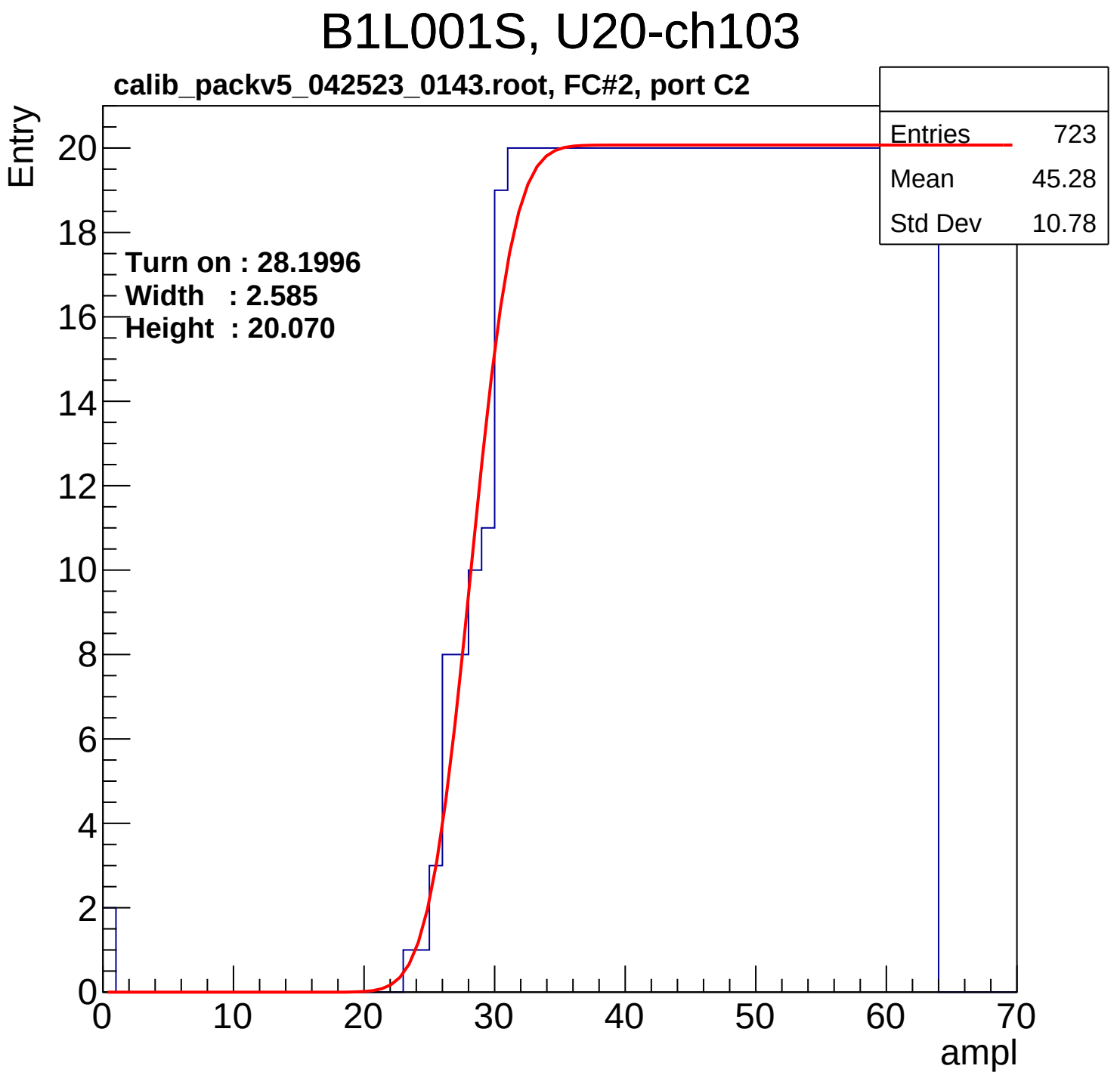
B1L001S, U20-ch103
calib_packv5_042523_0143.root, FC#2, port C2
Entries 723
Mean 45.28
Std Dev 10.78
Turn on : 28.1996
Width : 2.585
Height : 20.070
Entry
ampl
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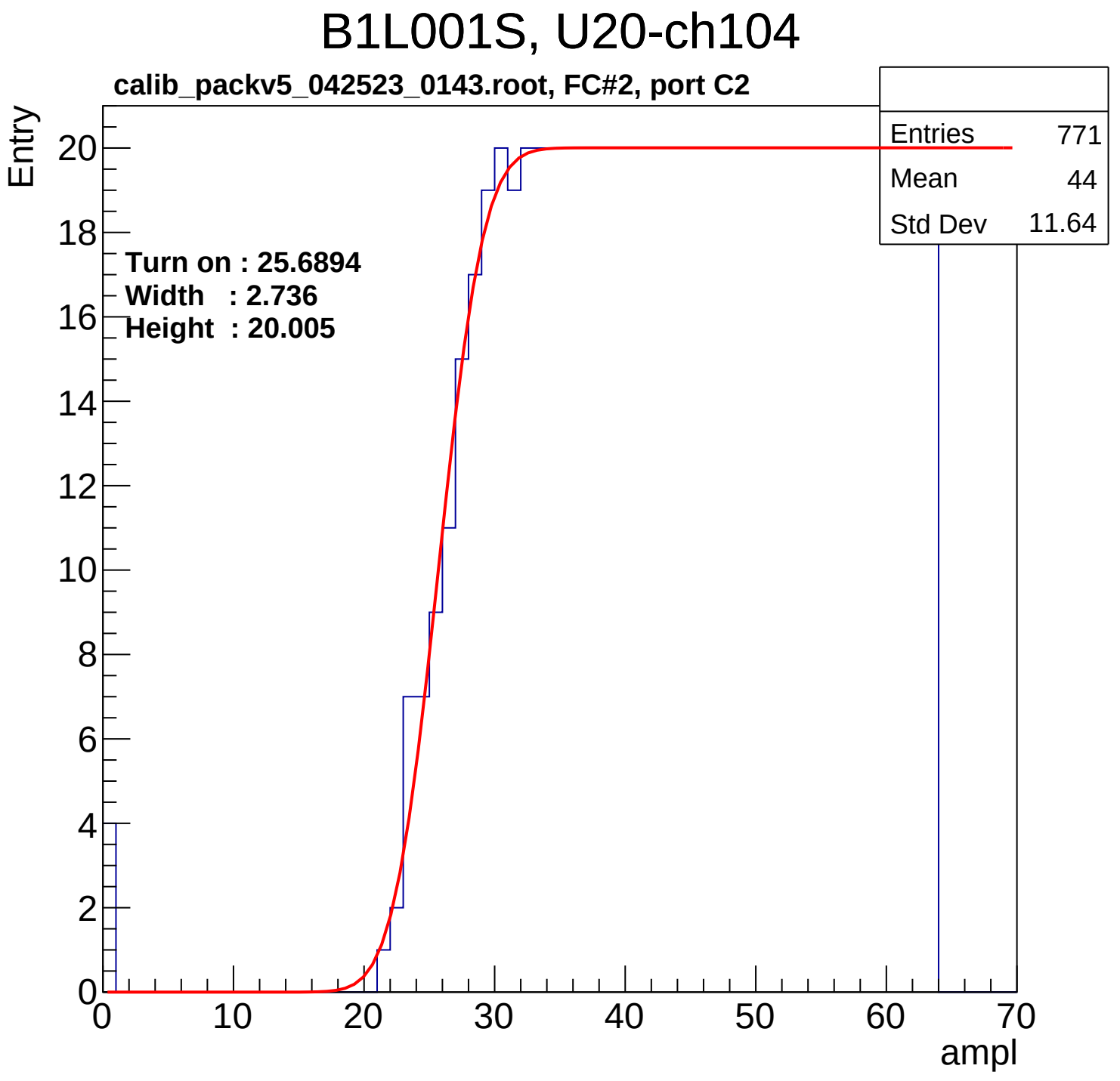
B1L001S, U20-ch104
calib_packv5_042523_0143.root, FC#2, port C2
Entries 771
Mean 44
Std Dev 11.64
Turn on : 25.6894
Width : 2.736
Height : 20.005
Entry
ampl
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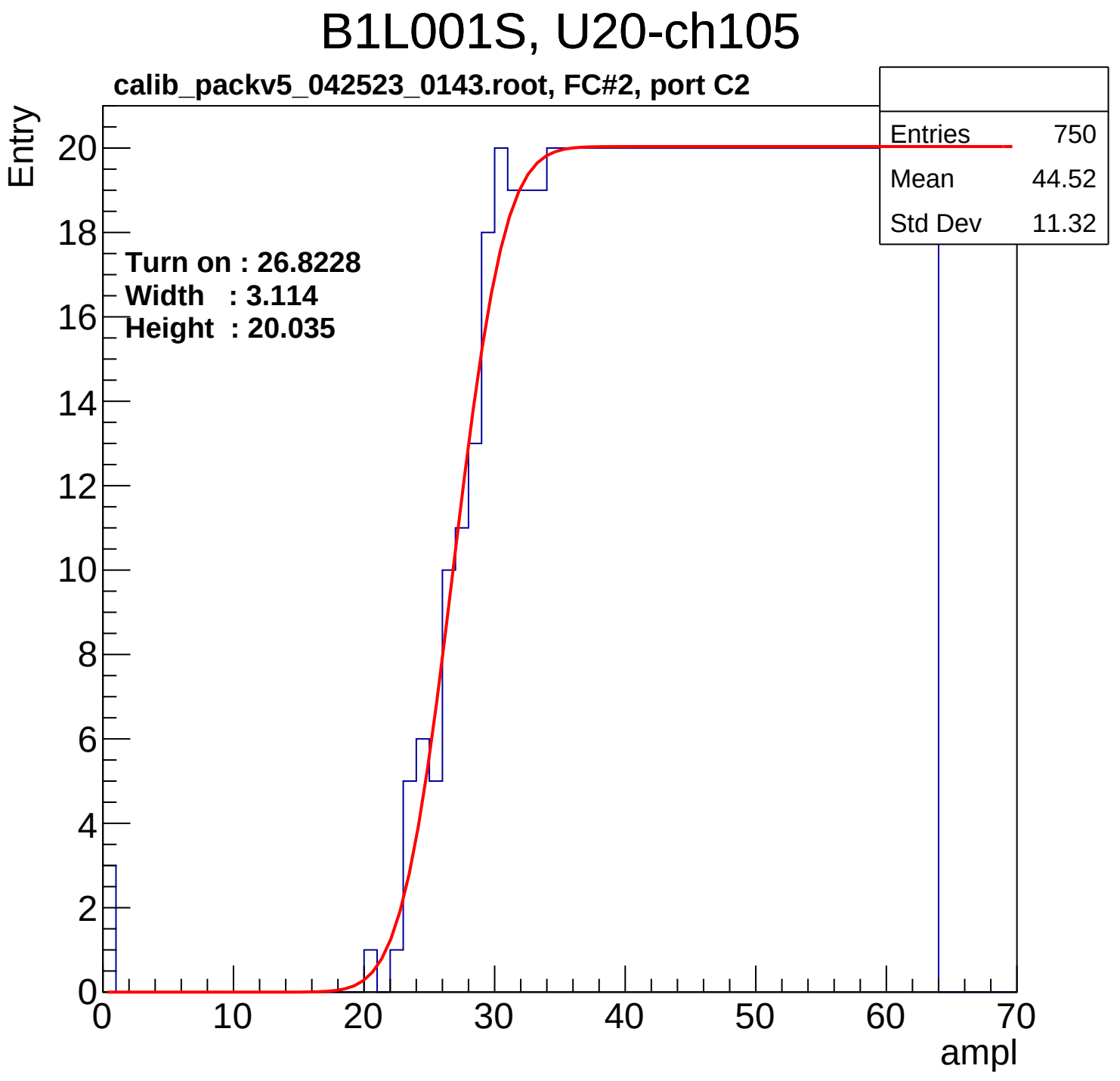
B1L001S, U20-ch105
calib_packv5_042523_0143.root, FC#2, port C2
Entries 750
Mean 44.52
Std Dev 11.32
Turn on : 26.8228
Width : 3.114
Height : 20.035
Entry
ampl
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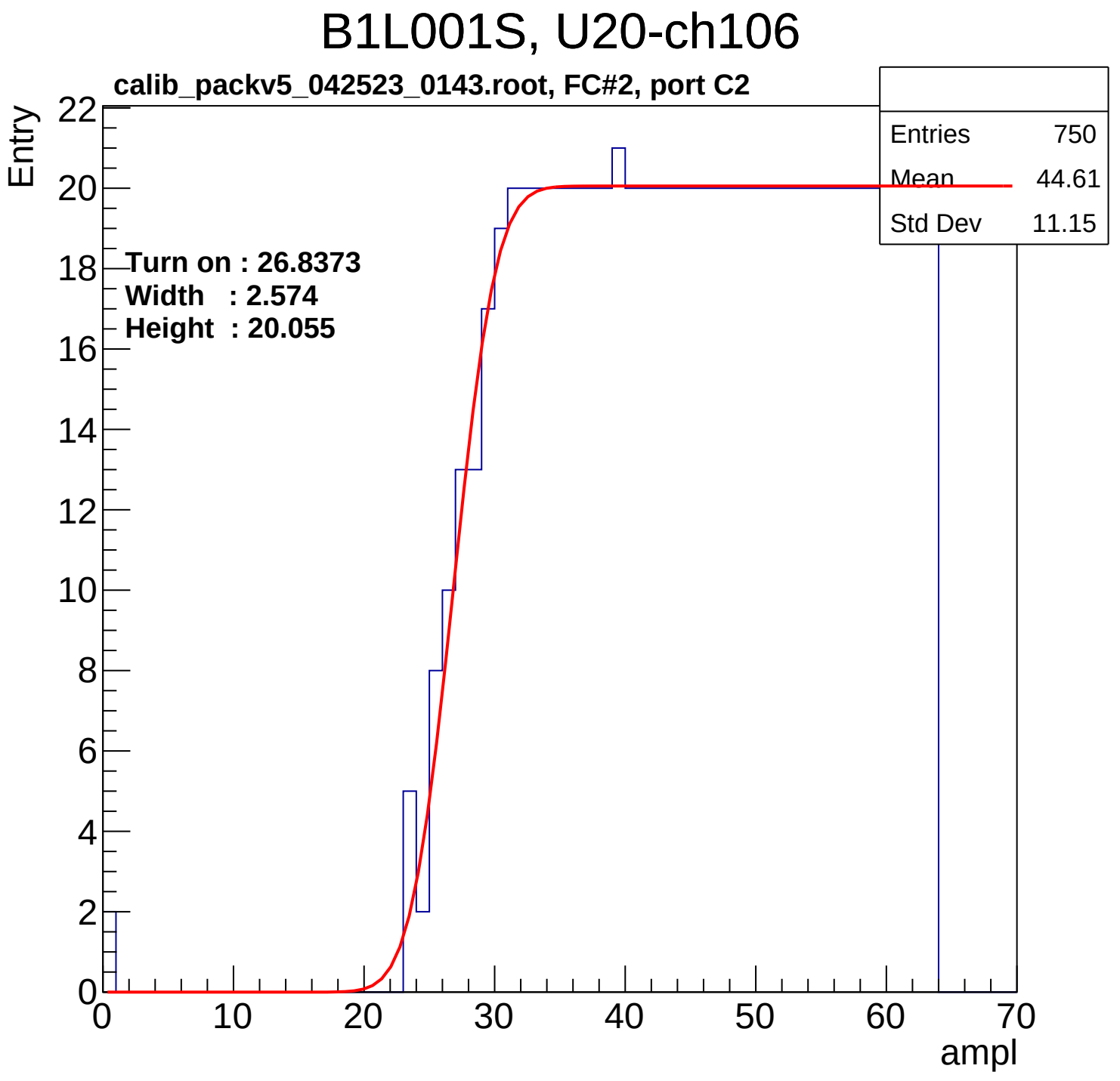
B1L001S, U20-ch106
calib_packv5_042523_0143.root, FC#2, port C2
Entries 750
Mean 44.61
Std Dev 11.15
Turn on : 26.8373
Width : 2.574
Height : 20.055
Entry
ampl
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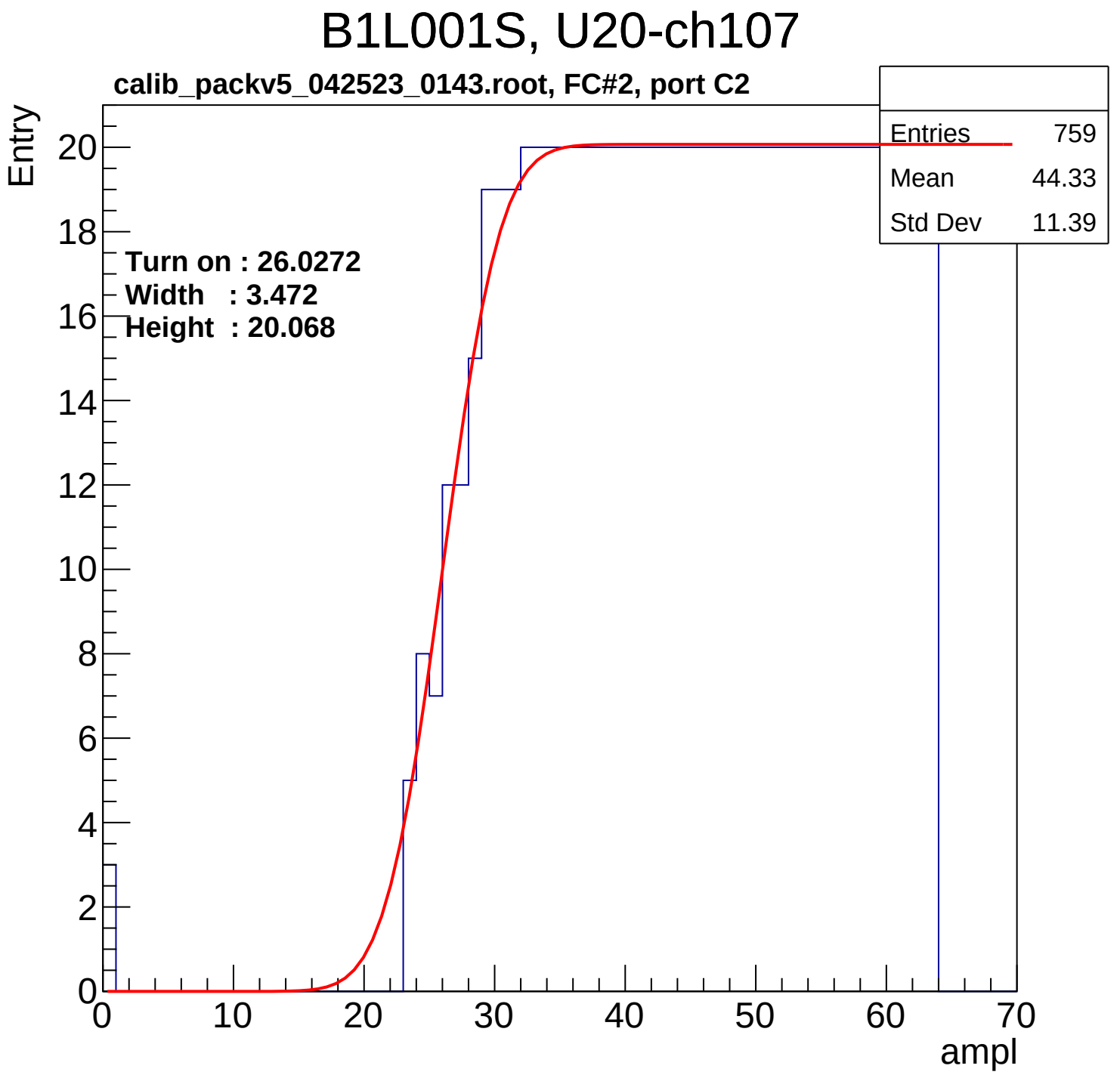
B1L001S, U20-ch107
calib_packv5_042523_0143.root, FC#2, port C2
Entries 759
Mean 44.33
Std Dev 11.39
Turn on : 26.0272
Width : 3.472
Height : 20.068
Entry
ampl
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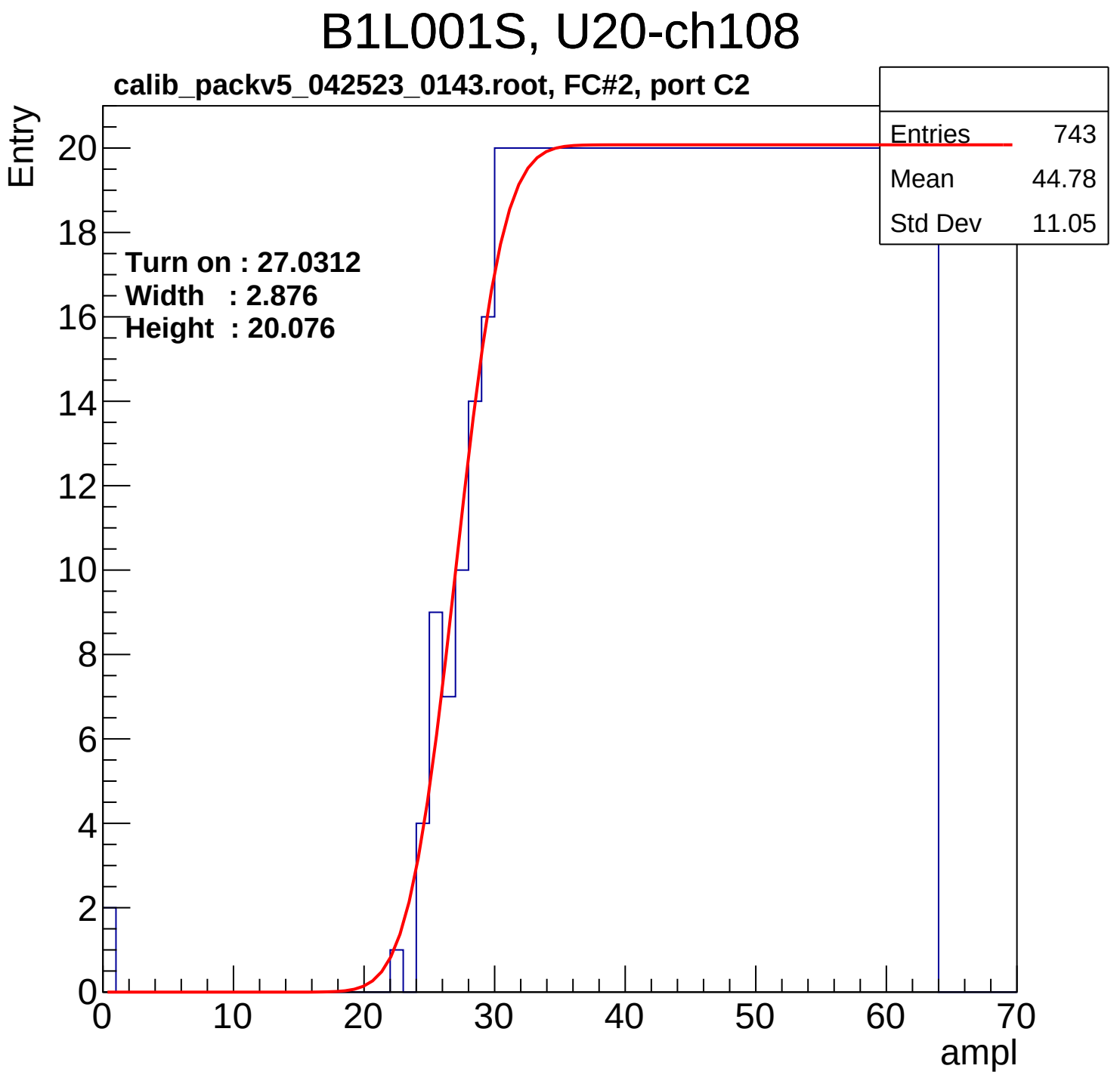
B1L001S, U20-ch108
calib_packv5_042523_0143.root, FC#2, port C2
Entries 743
Mean 44.78
Std Dev 11.05
Turn on : 27.0312
Width : 2.876
Height : 20.076
Entry
ampl
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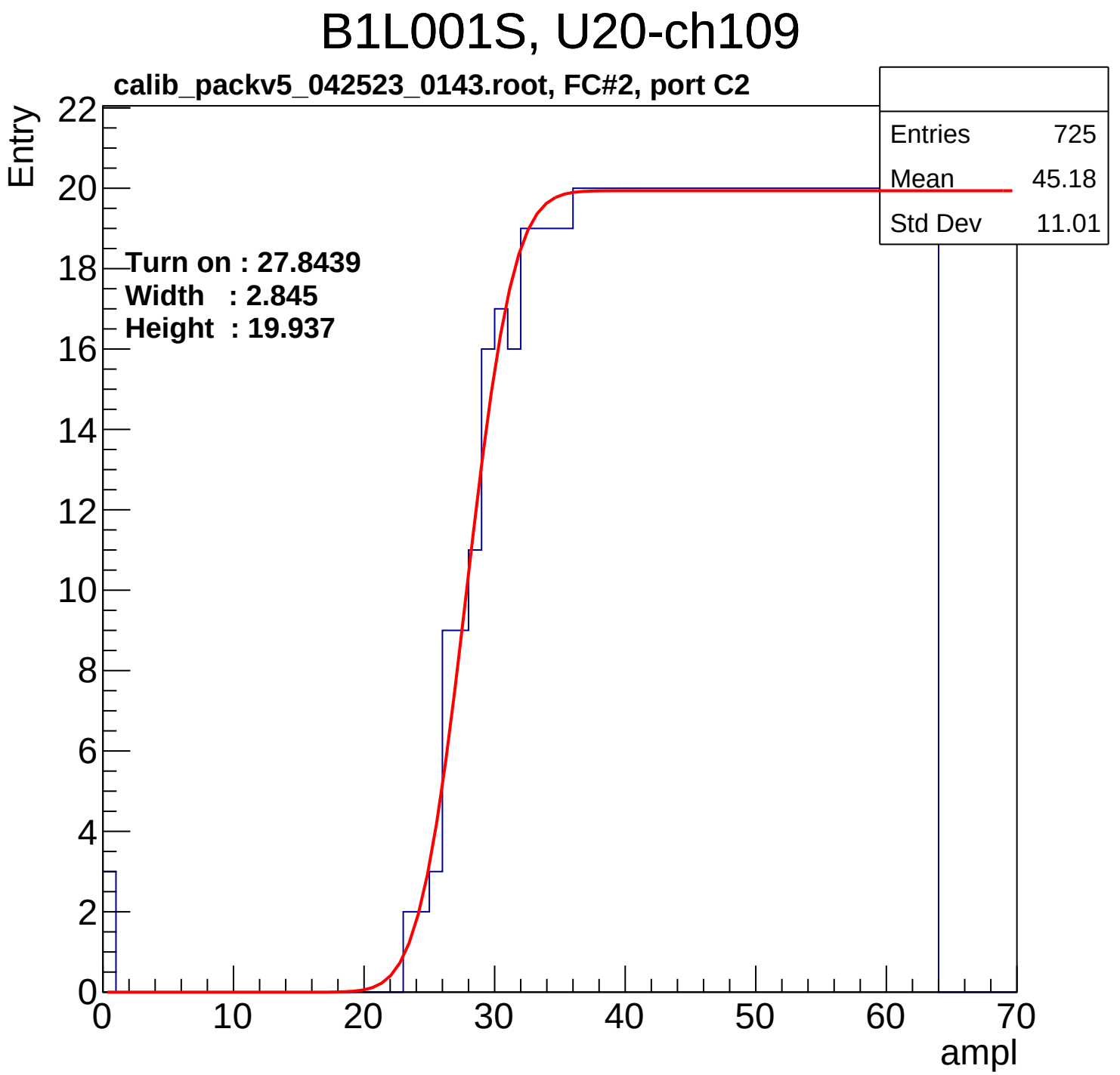
B1L001S, U20-ch109
calib_packv5_042523_0143.root, FC#2, port C2
Entries 725
Mean 45.18
Std Dev 11.01
Turn on : 27.8439
Width : 2.845
Height : 19.937
Entry
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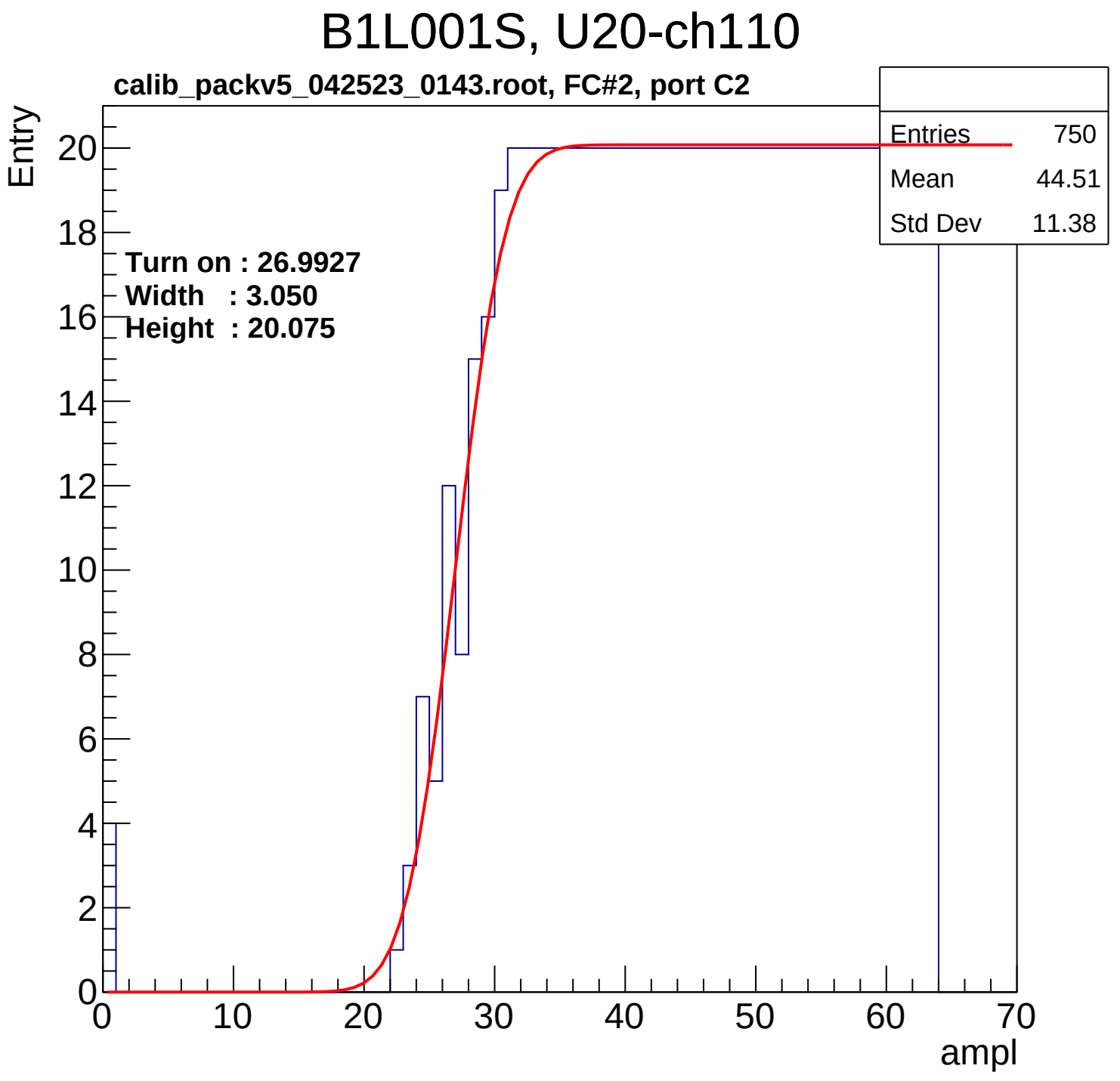
B1L001S, U20-ch110
calib_packv5_042523_0143.root, FC#2, port C2
Entries 750
Mean 44.51
Std Dev 11.38
Turn on : 26.9927
Width : 3.050
Height : 20.075
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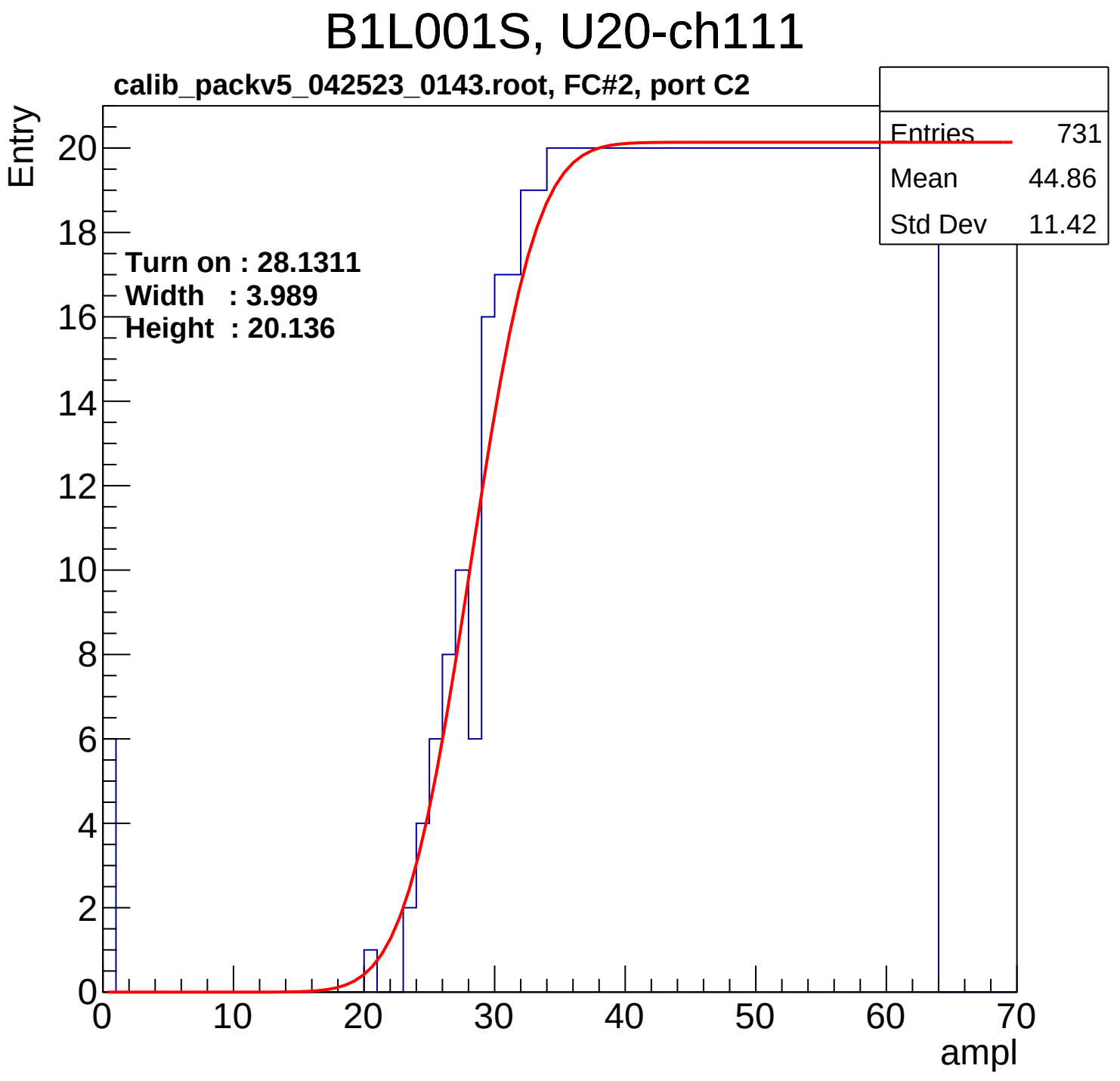
B1L001S, U20-ch111
calib_packv5_042523_0143.root, FC#2, port C2
Entries 731
Mean 44.86
Std Dev 11.42
Turn on : 28.1311
Width : 3.989
Height : 20.136
Entry
ampl
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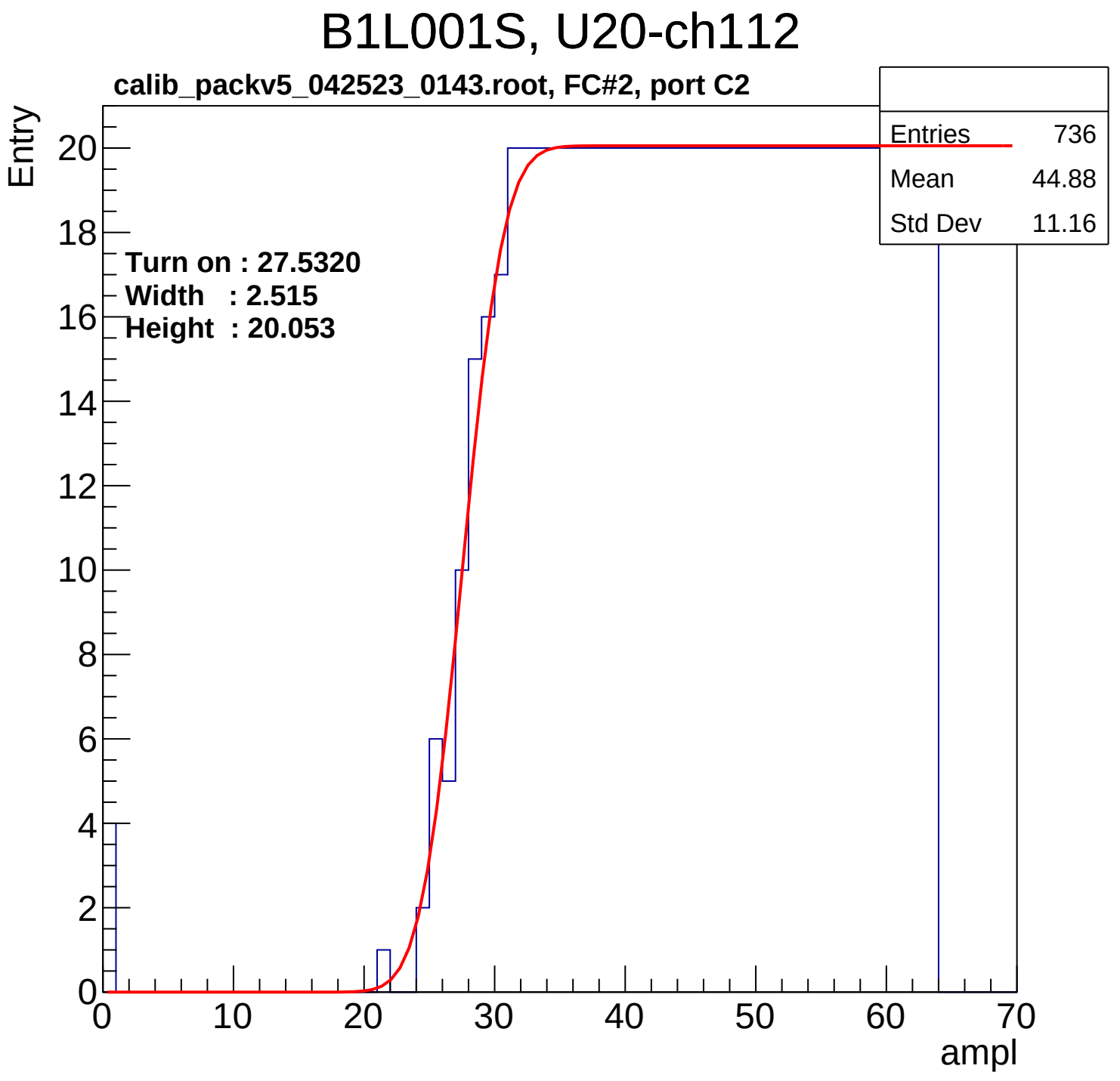
B1L001S, U20-ch112
calib_packv5_042523_0143.root, FC#2, port C2
Entries 736
Mean 44.88
Std Dev 11.16
Turn on : 27.5320
Width : 2.515
Height : 20.053
Entry
ampl
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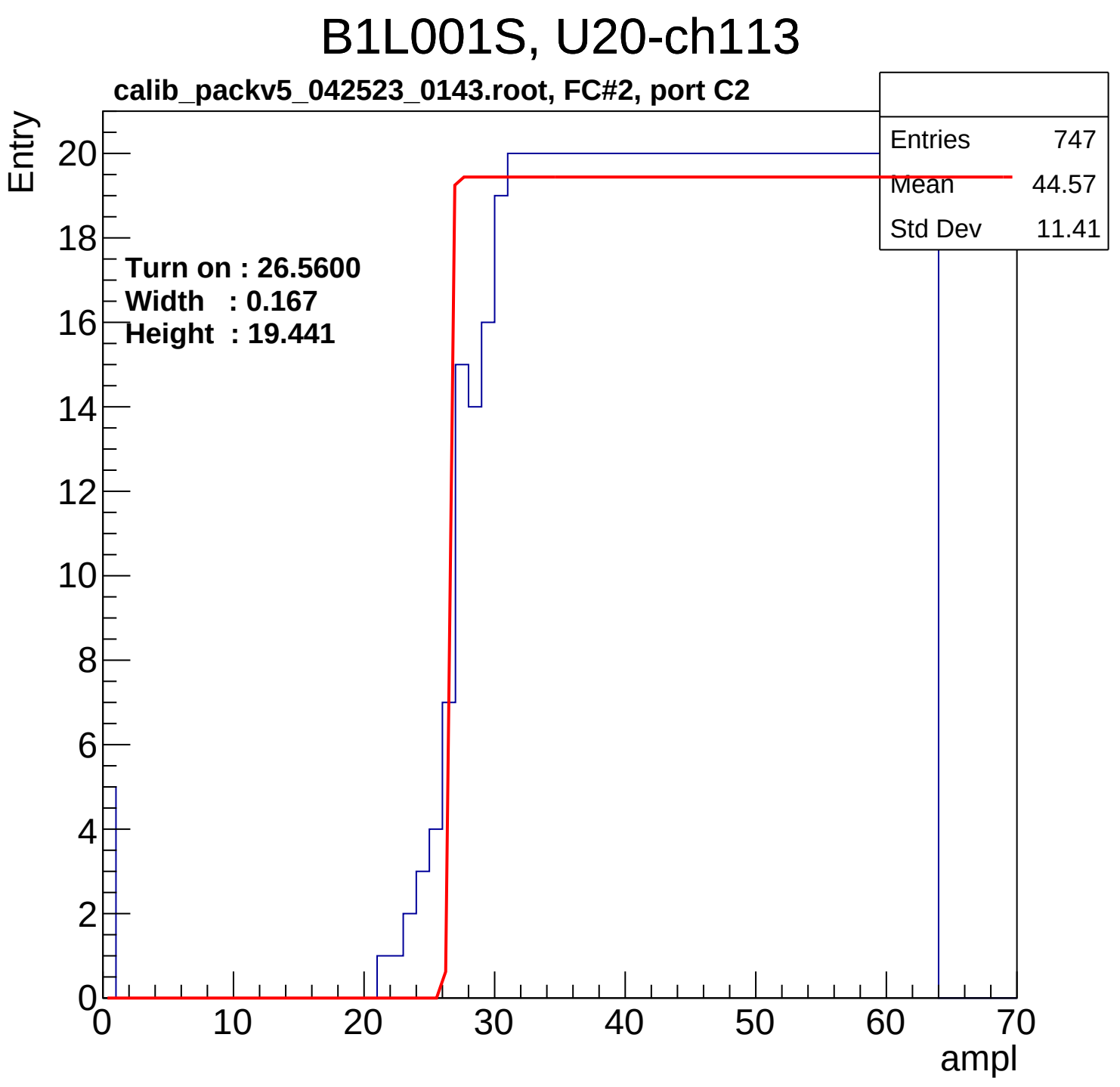
B1L001S, U20-ch113
calib_packv5_042523_0143.root, FC#2, port C2
Entries 747
Mean 44.57
Std Dev 11.41
Turn on : 26.5600
Width : 0.167
Height : 19.441
Entry
ampl
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6
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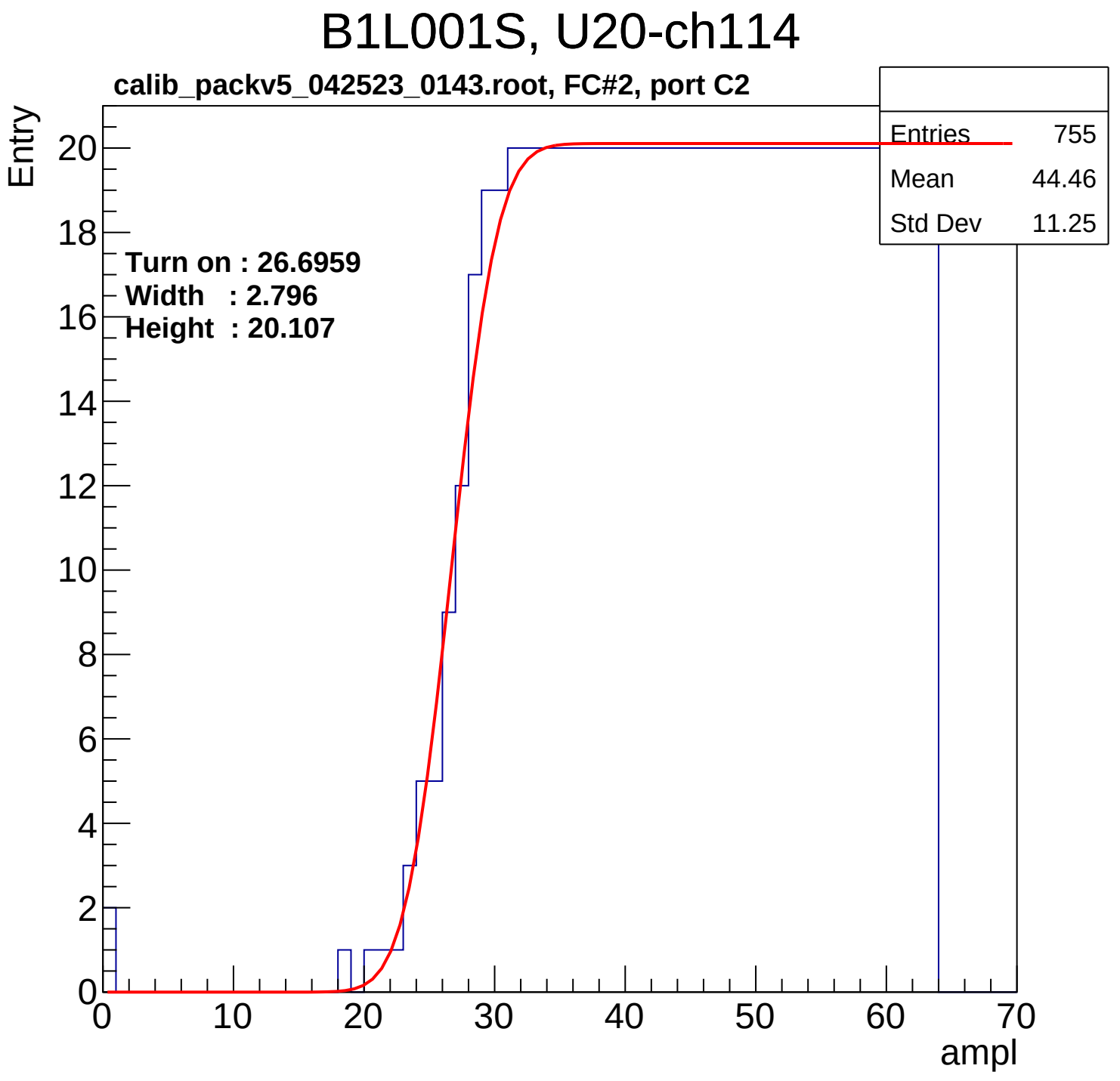
B1L001S, U20-ch114
calib_packv5_042523_0143.root, FC#2, port C2
Entries 755
Mean 44.46
Std Dev 11.25
Turn on : 26.6959
Width : 2.796
Height : 20.107
Entry
ampl
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6
8
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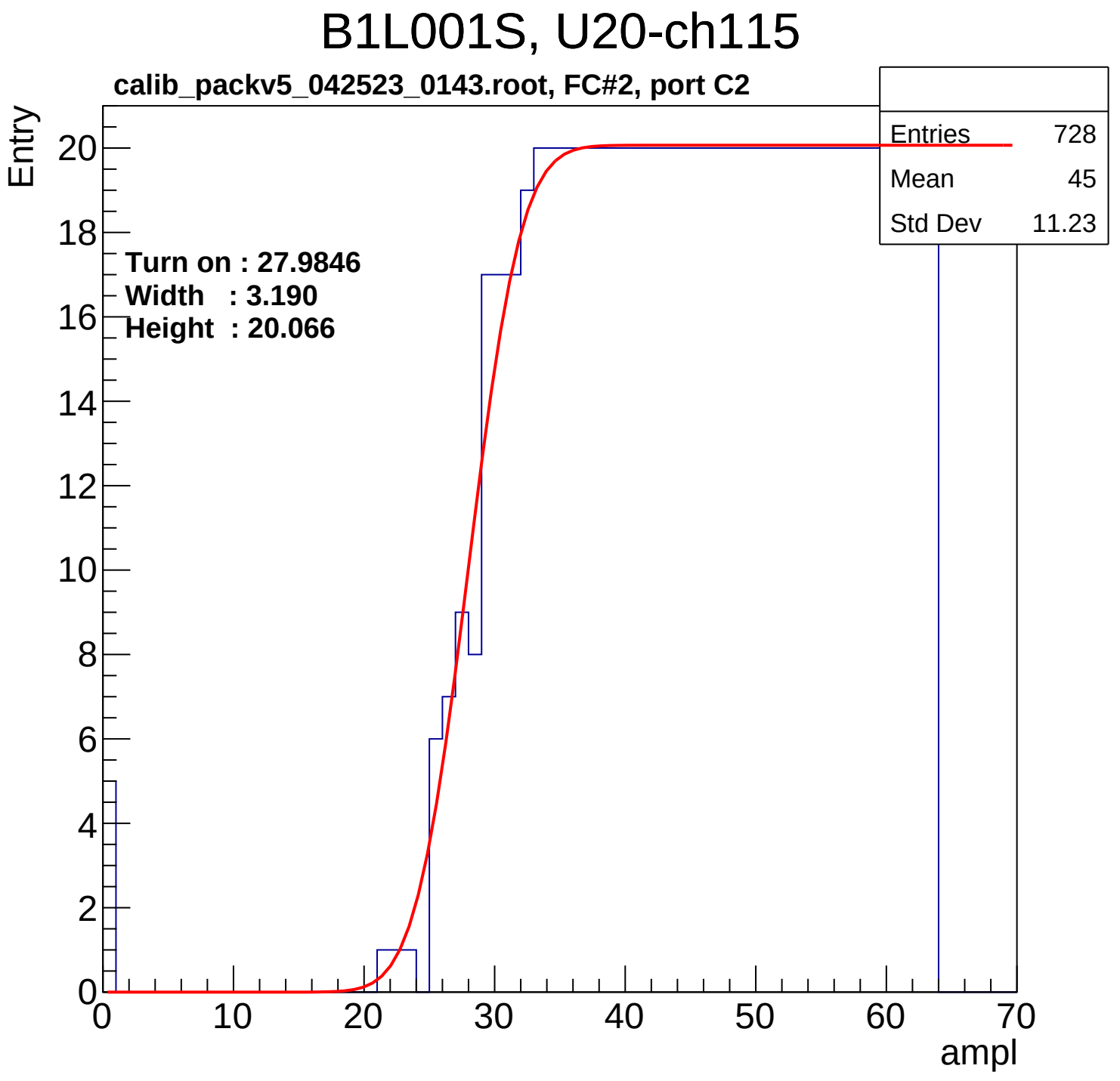
B1L001S, U20-ch115
calib_packv5_042523_0143.root, FC#2, port C2
Entries 728
Mean 45
Std Dev 11.23
Turn on : 27.9846
Width : 3.190
Height : 20.066
Entry
ampl
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6
8
10
12
14
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18
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0
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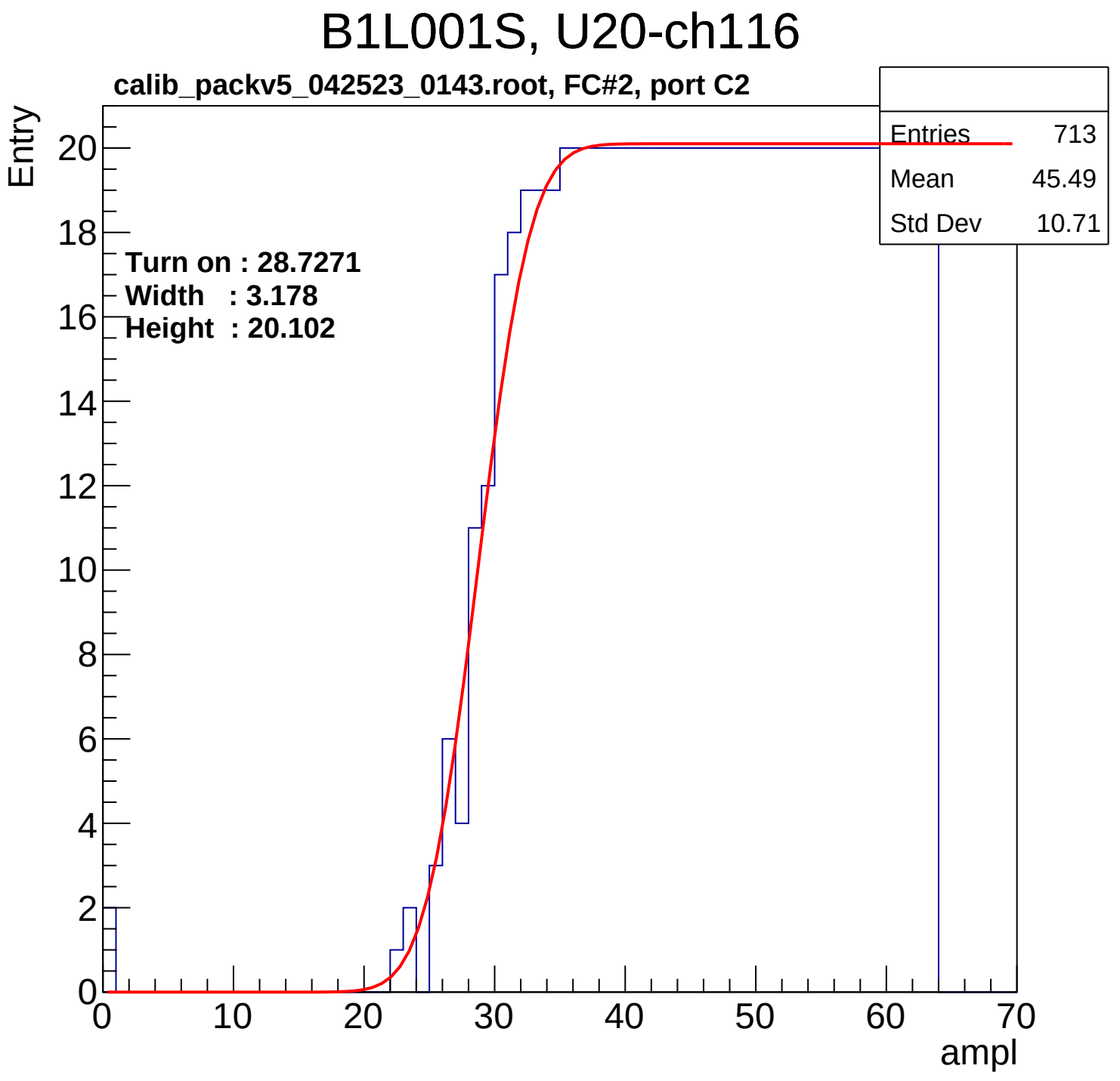
B1L001S, U20-ch116
calib_packv5_042523_0143.root, FC#2, port C2
Entries 713
Mean 45.49
Std Dev 10.71
Turn on : 28.7271
Width : 3.178
Height : 20.102
Entry
ampl
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6
8
10
12
14
16
18
20
0
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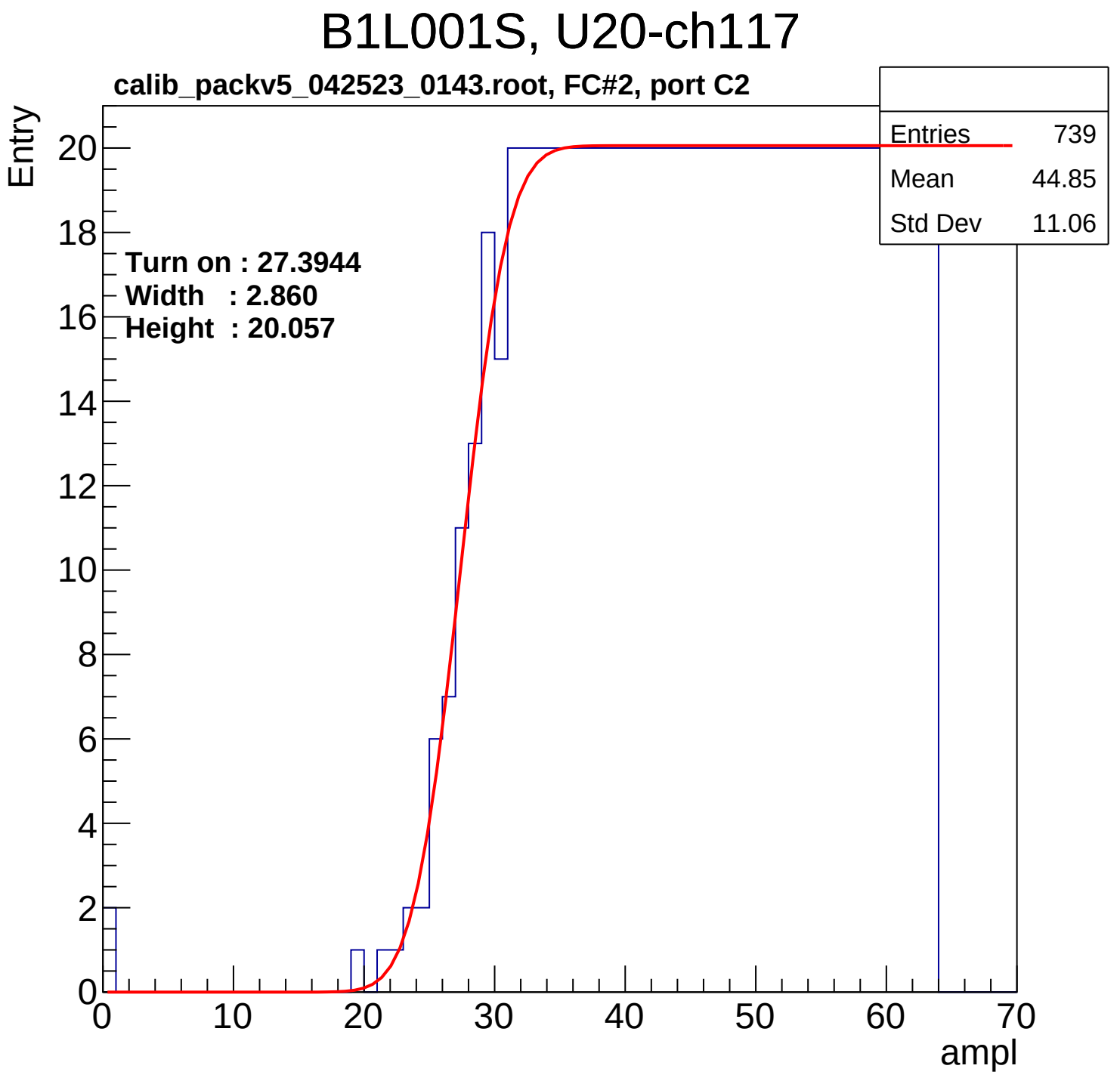
B1L001S, U20-ch117
calib_packv5_042523_0143.root, FC#2, port C2
Entries 739
Mean 44.85
Std Dev 11.06
Turn on : 27.3944
Width : 2.860
Height : 20.057
Entry
ampl
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6
8
10
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14
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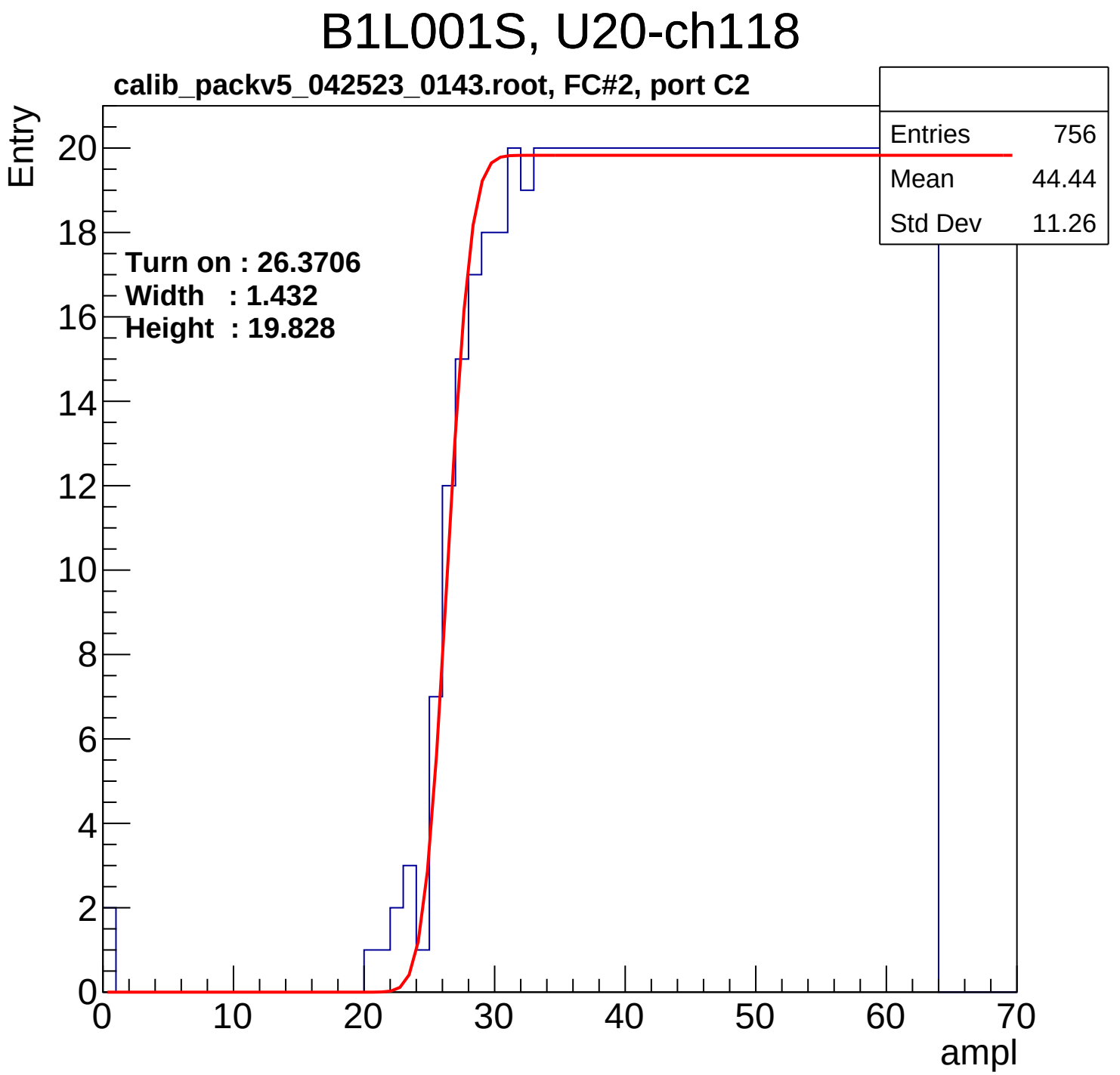
B1L001S, U20-ch118
calib_packv5_042523_0143.root, FC#2, port C2
Entries 756
Mean 44.44
Std Dev 11.26
Turn on : 26.3706
Width : 1.432
Height : 19.828
Entry
ampl
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8
10
12
14
16
18
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0
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20
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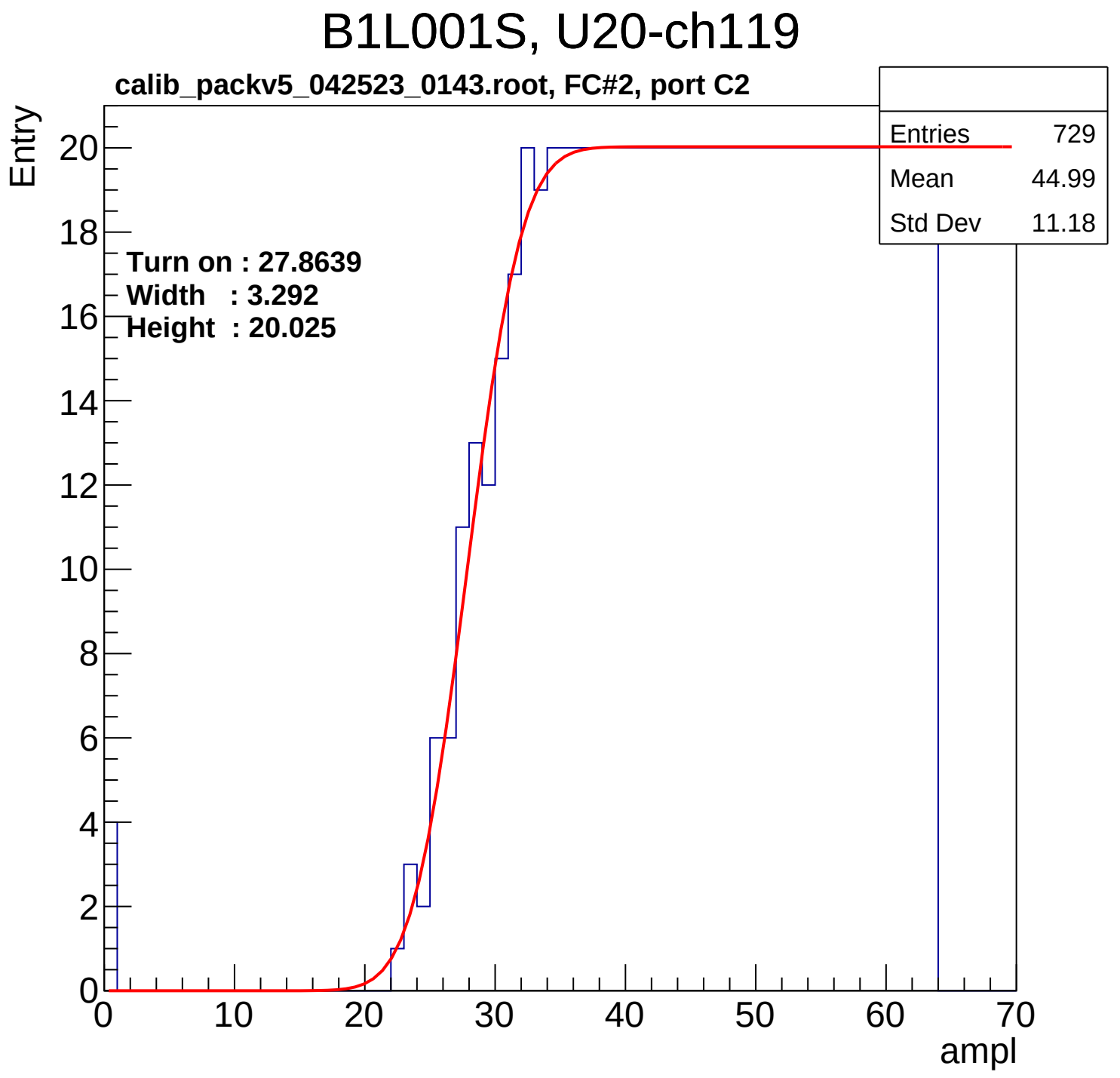
B1L001S, U20-ch119
calib_packv5_042523_0143.root, FC#2, port C2
Entries 729
Mean 44.99
Std Dev 11.18
Turn on : 27.8639
Width : 3.292
Height : 20.025
Entry
ampl
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6
8
10
12
14
16
18
20
0
10
20
30
40
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60
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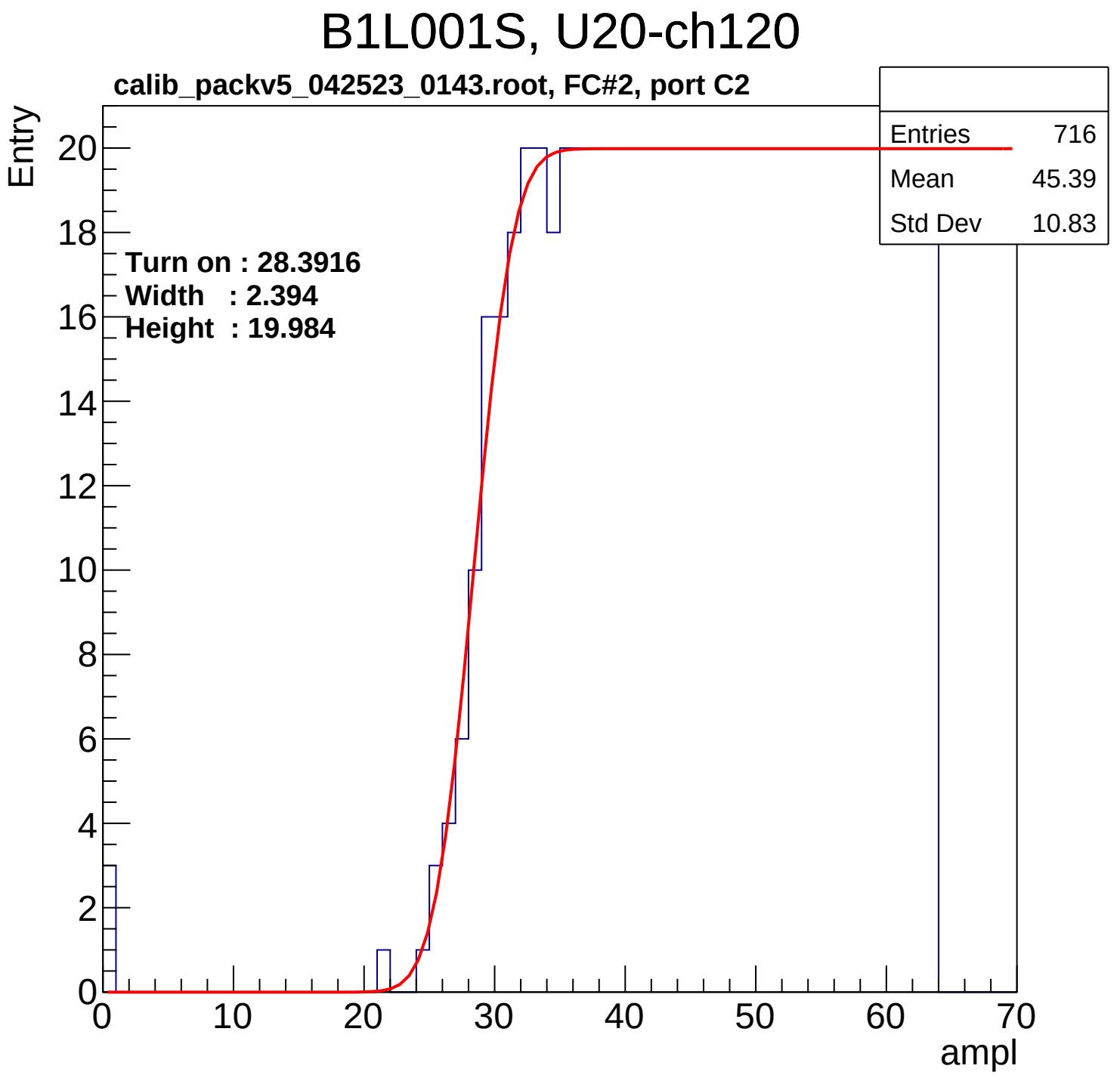
B1L001S, U20-ch120
calib_packv5_042523_0143.root, FC#2, port C2
Entries 716
Mean 45.39
Std Dev 10.83
Turn on : 28.3916
Width : 2.394
Height : 19.984
Entry
ampl
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6
8
10
12
14
16
18
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0
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20
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40
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60
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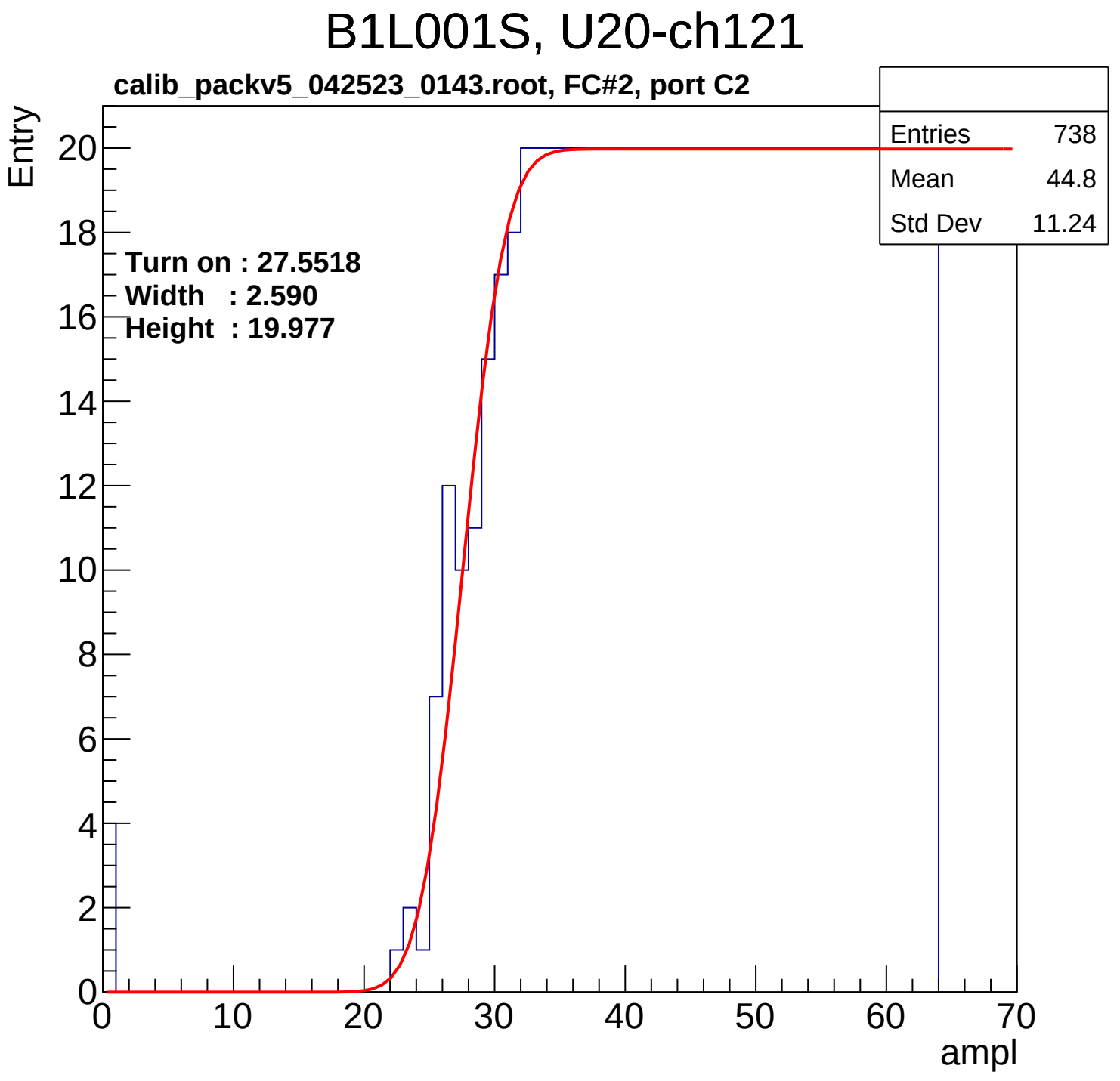
B1L001S, U20-ch121
calib_packv5_042523_0143.root, FC#2, port C2
Entries 738
Mean 44.8
Std Dev 11.24
Turn on : 27.5518
Width : 2.590
Height : 19.977
Entry
ampl
0
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6
8
10
12
14
16
18
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0
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20
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40
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60
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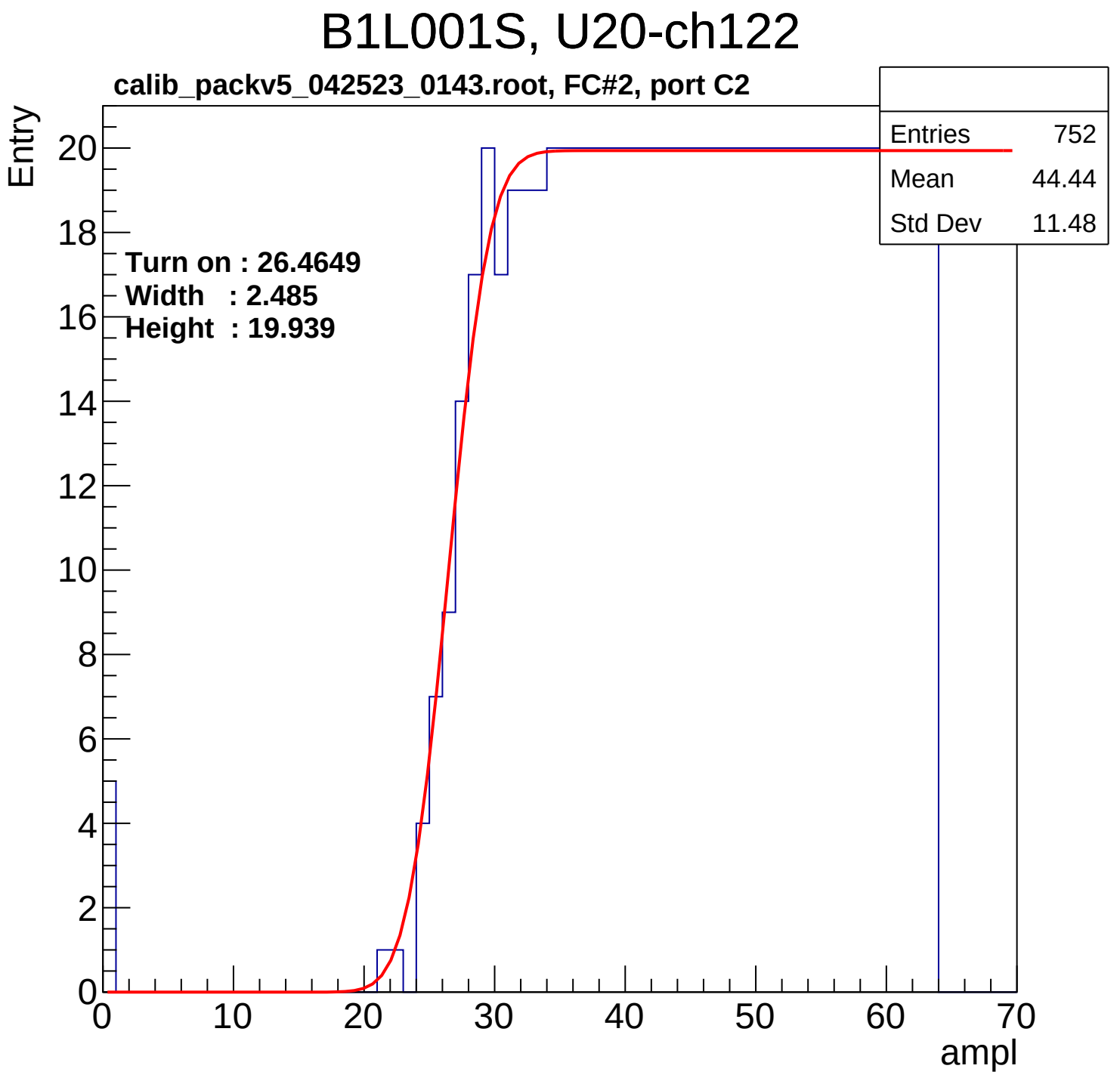
B1L001S, U20-ch122
calib_packv5_042523_0143.root, FC#2, port C2
Entries 752
Mean 44.44
Std Dev 11.48
Turn on : 26.4649
Width : 2.485
Height : 19.939
Entry
ampl
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6
8
10
12
14
16
18
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0
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40
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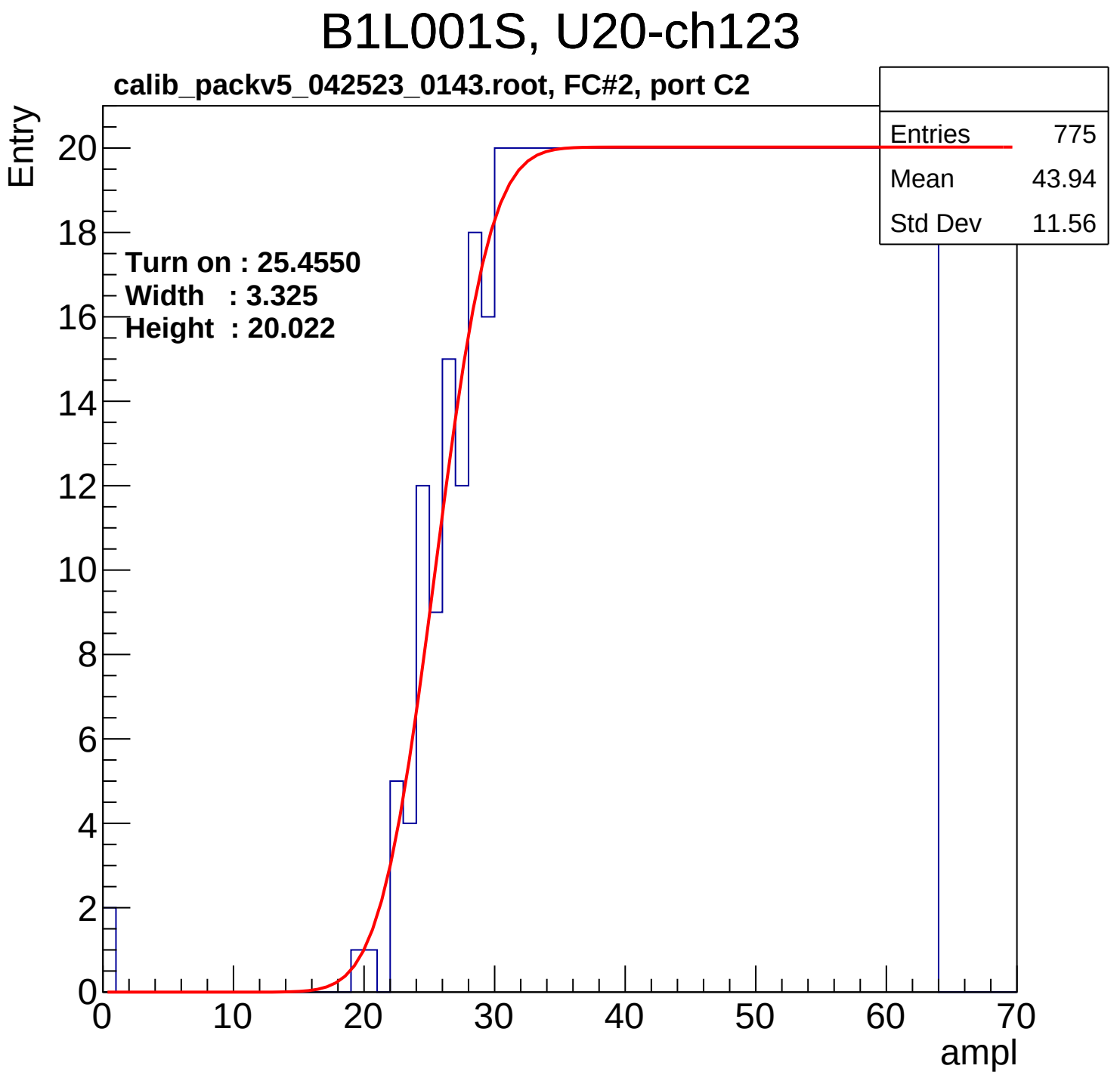
B1L001S, U20-ch123
calib_packv5_042523_0143.root, FC#2, port C2
Entries 775
Mean 43.94
Std Dev 11.56
Turn on : 25.4550
Width : 3.325
Height : 20.022
Entry
ampl
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6
8
10
12
14
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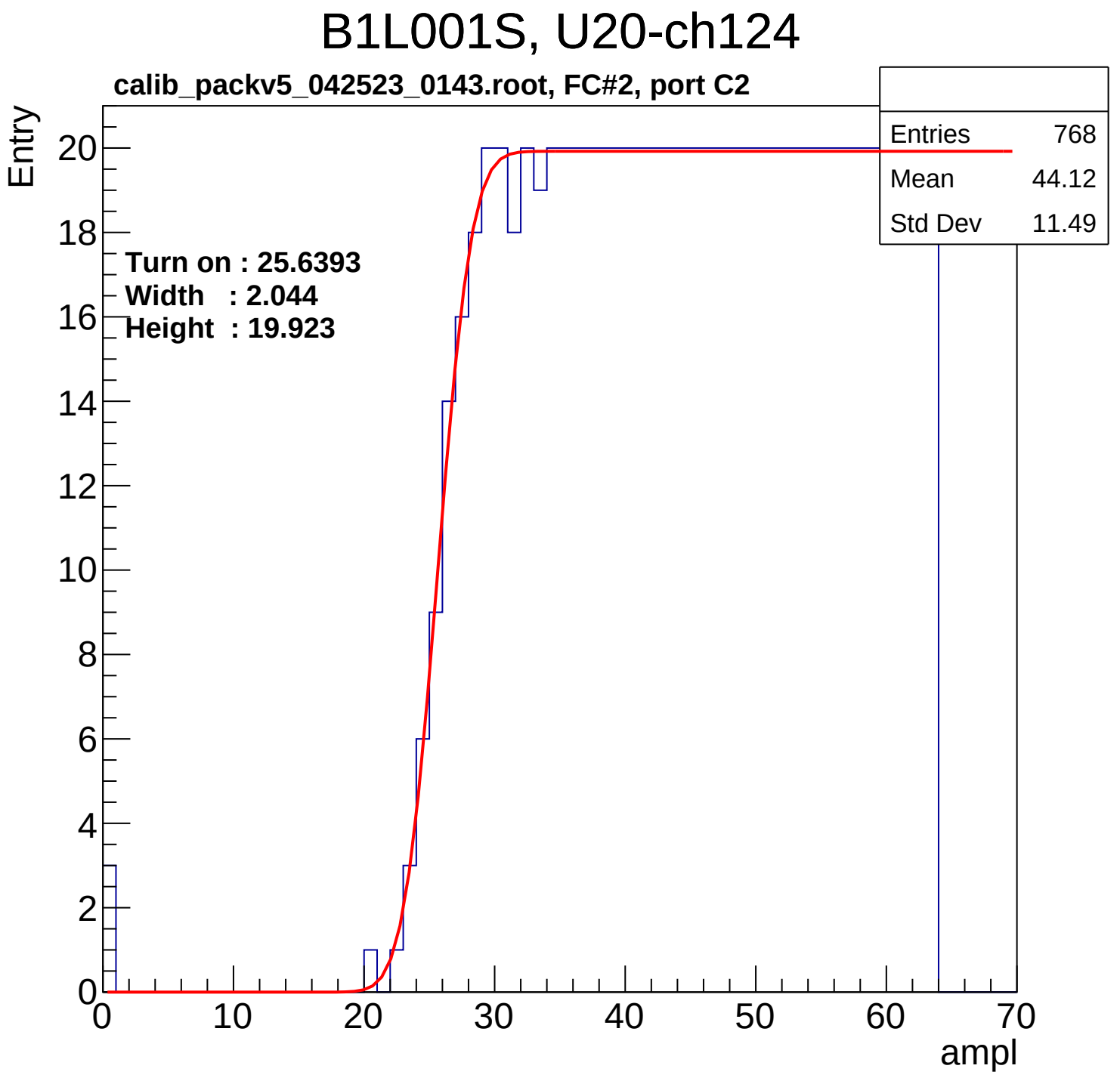
B1L001S, U20-ch124
calib_packv5_042523_0143.root, FC#2, port C2
Entries 768
Mean 44.12
Std Dev 11.49
Turn on : 25.6393
Width : 2.044
Height : 19.923
Entry
ampl
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8
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12
14
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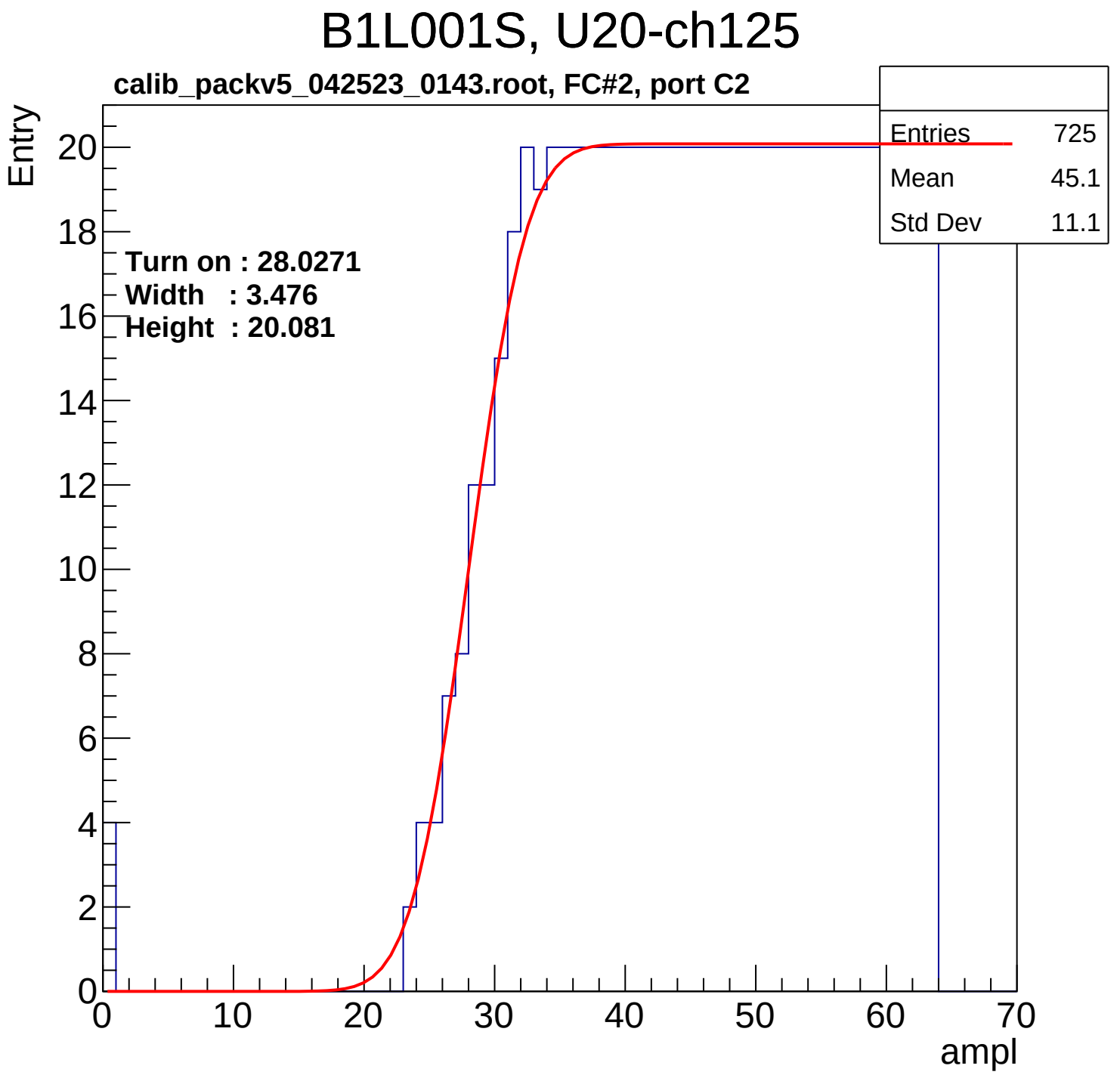
B1L001S, U20-ch125
calib_packv5_042523_0143.root, FC#2, port C2
Entries 725
Mean 45.1
Std Dev 11.1
Turn on : 28.0271
Width : 3.476
Height : 20.081
Entry
ampl
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14
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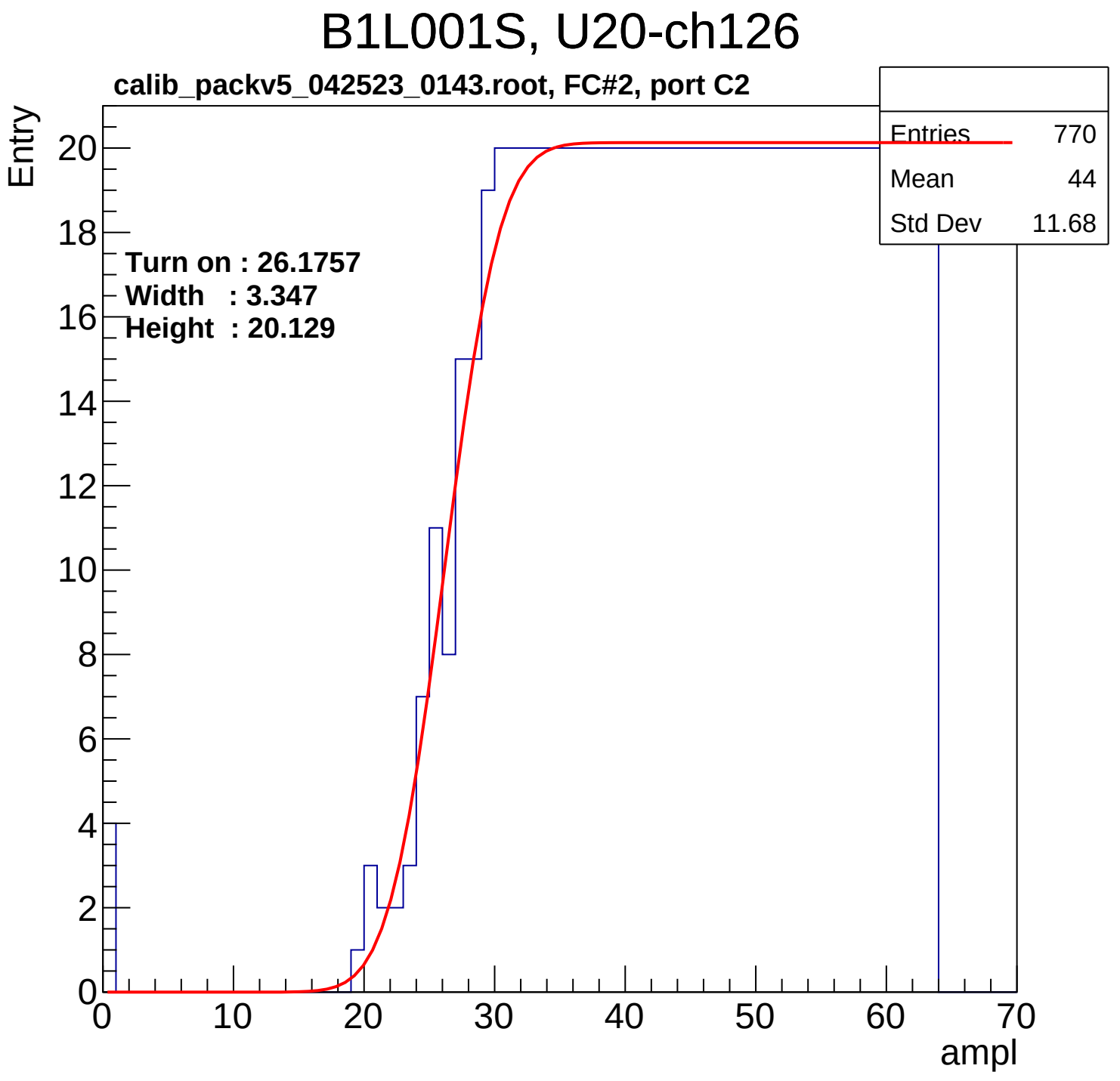
B1L001S, U20-ch126
calib_packv5_042523_0143.root, FC#2, port C2
Entries 770
Mean 44
Std Dev 11.68
Turn on : 26.1757
Width : 3.347
Height : 20.129
Entry
ampl
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12
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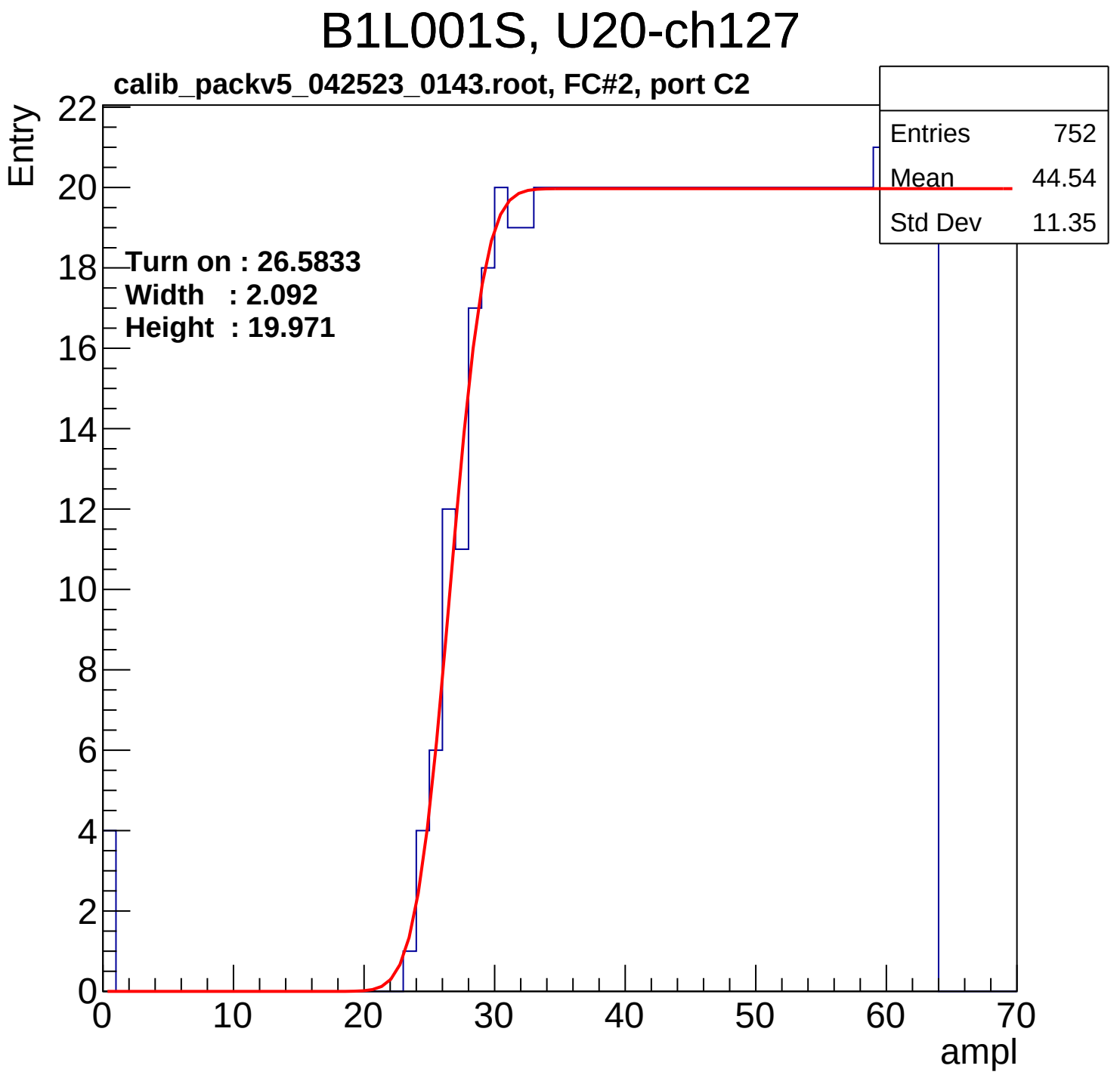
B1L001S, U20-ch127
calib_packv5_042523_0143.root, FC#2, port C2
Entries 752
Mean 44.54
Std Dev 11.35
Turn on : 26.5833
Width : 2.092
Height : 19.971
Entry
ampl
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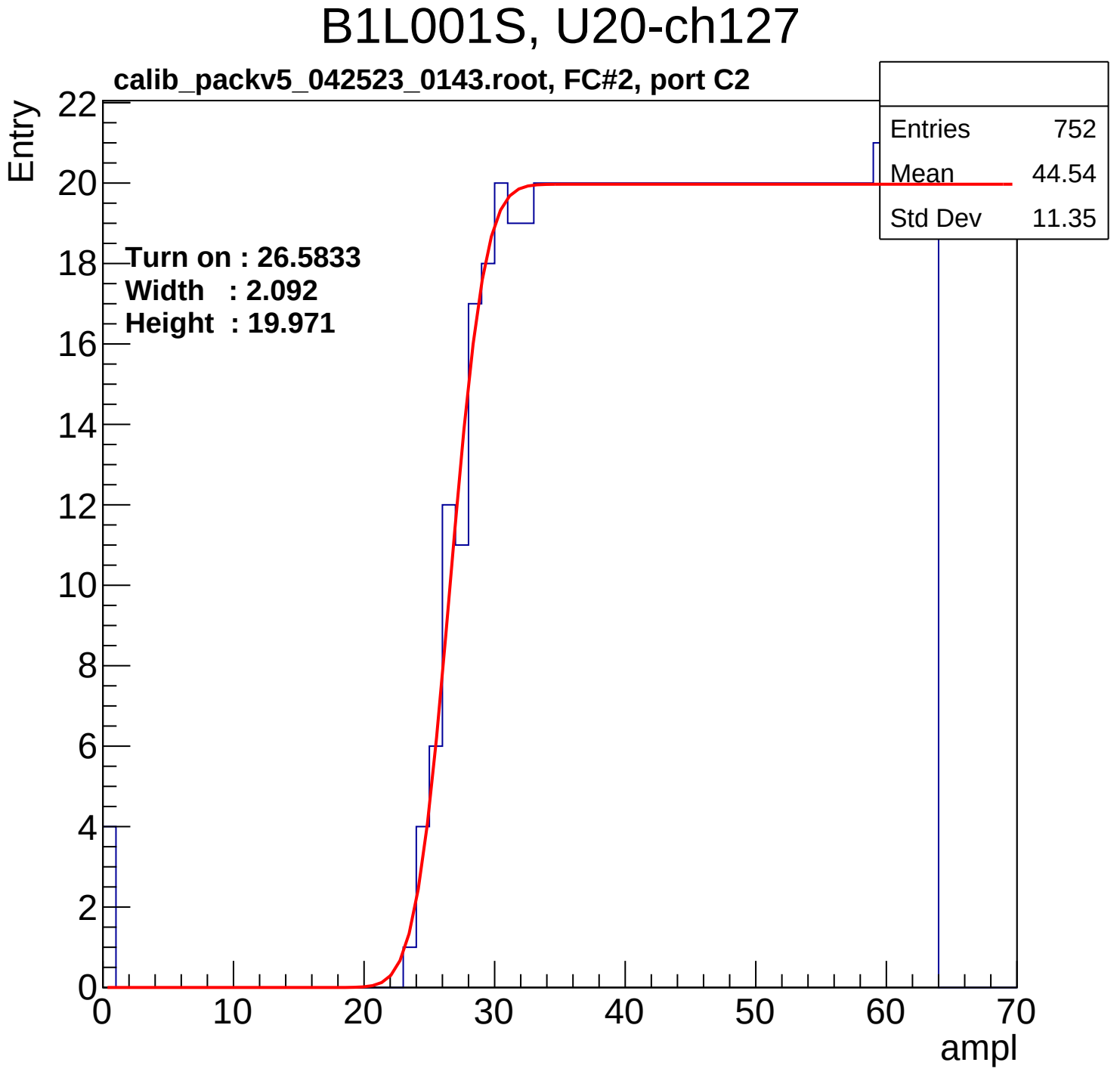
B1L001S, U20-ch127
calib_packv5_042523_0143.root, FC#2, port C2
Entries 752
Mean 44.54
Std Dev 11.35
Turn on : 26.5833
Width : 2.092
Height : 19.971
Entry
ampl
0
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4
6
8
10
12
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16
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