

B1L101S, U24-ch0

calib_packv5_042523_0143.root, FC#0, port D2

Entries	370
Mean	44.58
Std Dev	11.69

Turn on : 27.5418

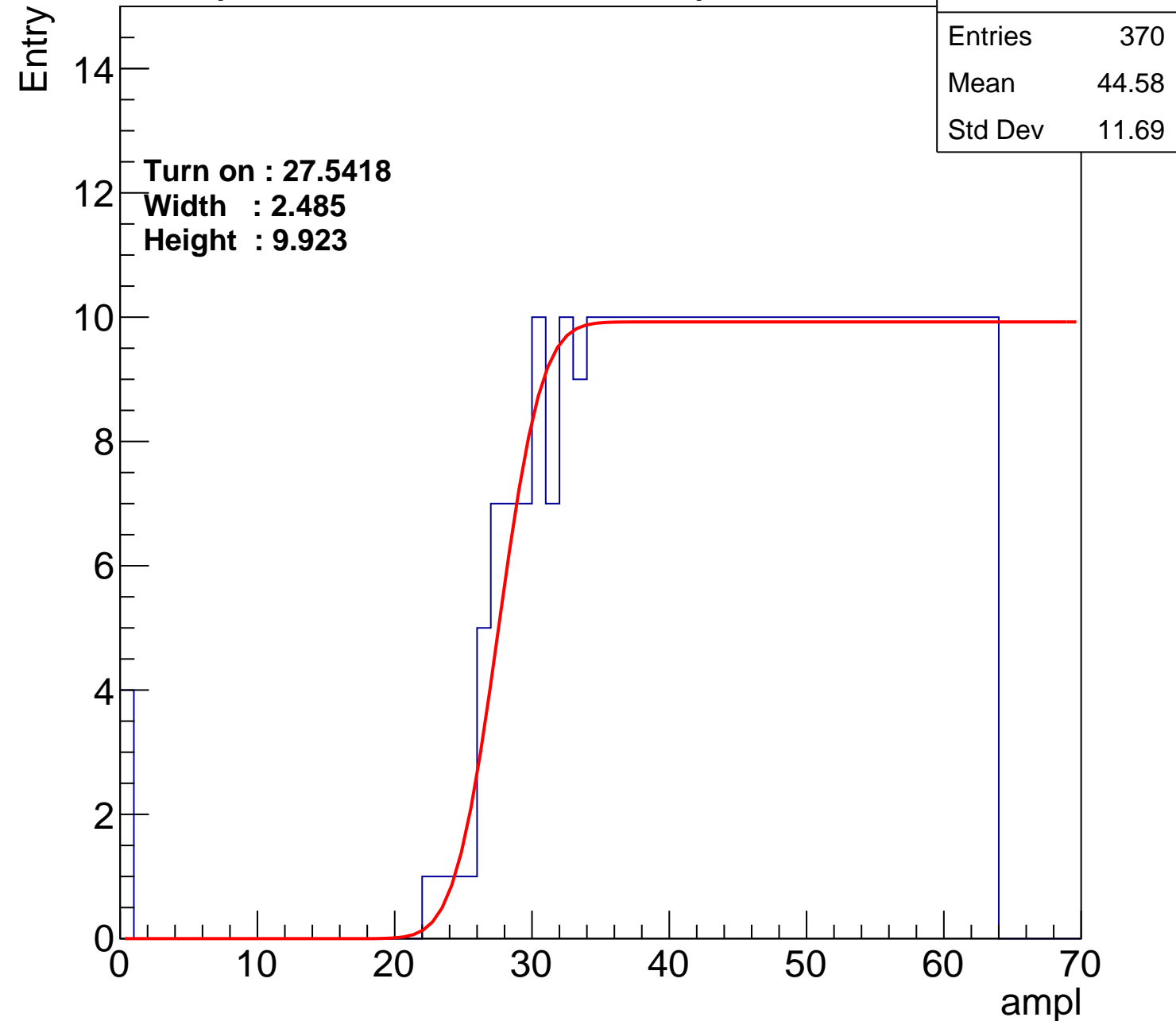
Width : 2.485

Height : 9.923

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch1

calib_packv5_042523_0143.root, FC#0, port D2

Entries	372
Mean	44.62
Std Dev	11.46

Turn on : 26.9537

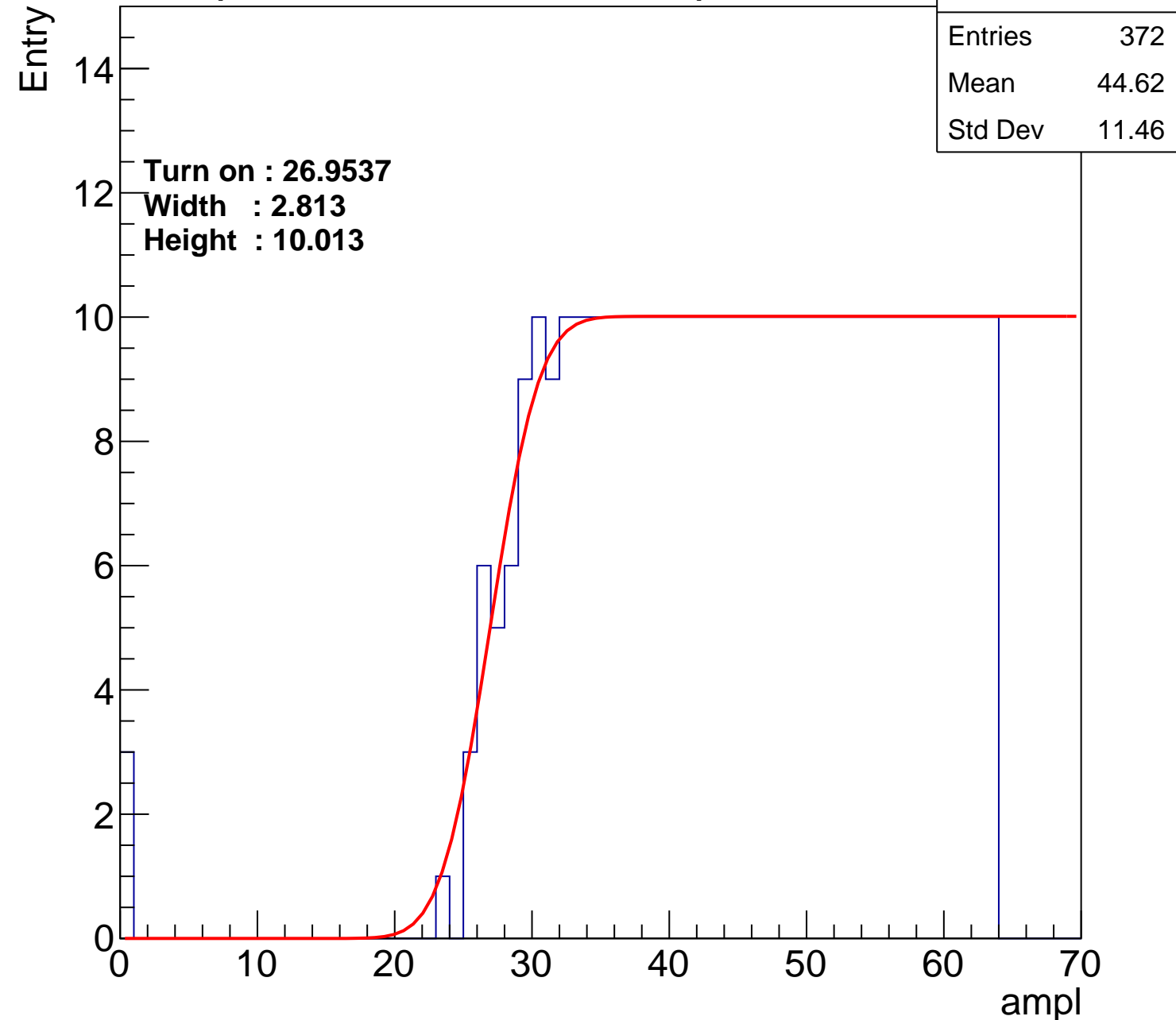
Width : 2.813

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch2

calib_packv5_042523_0143.root, FC#0, port D2

Entries	364
Mean	45.02
Std Dev	11.15

Turn on : 27.6372

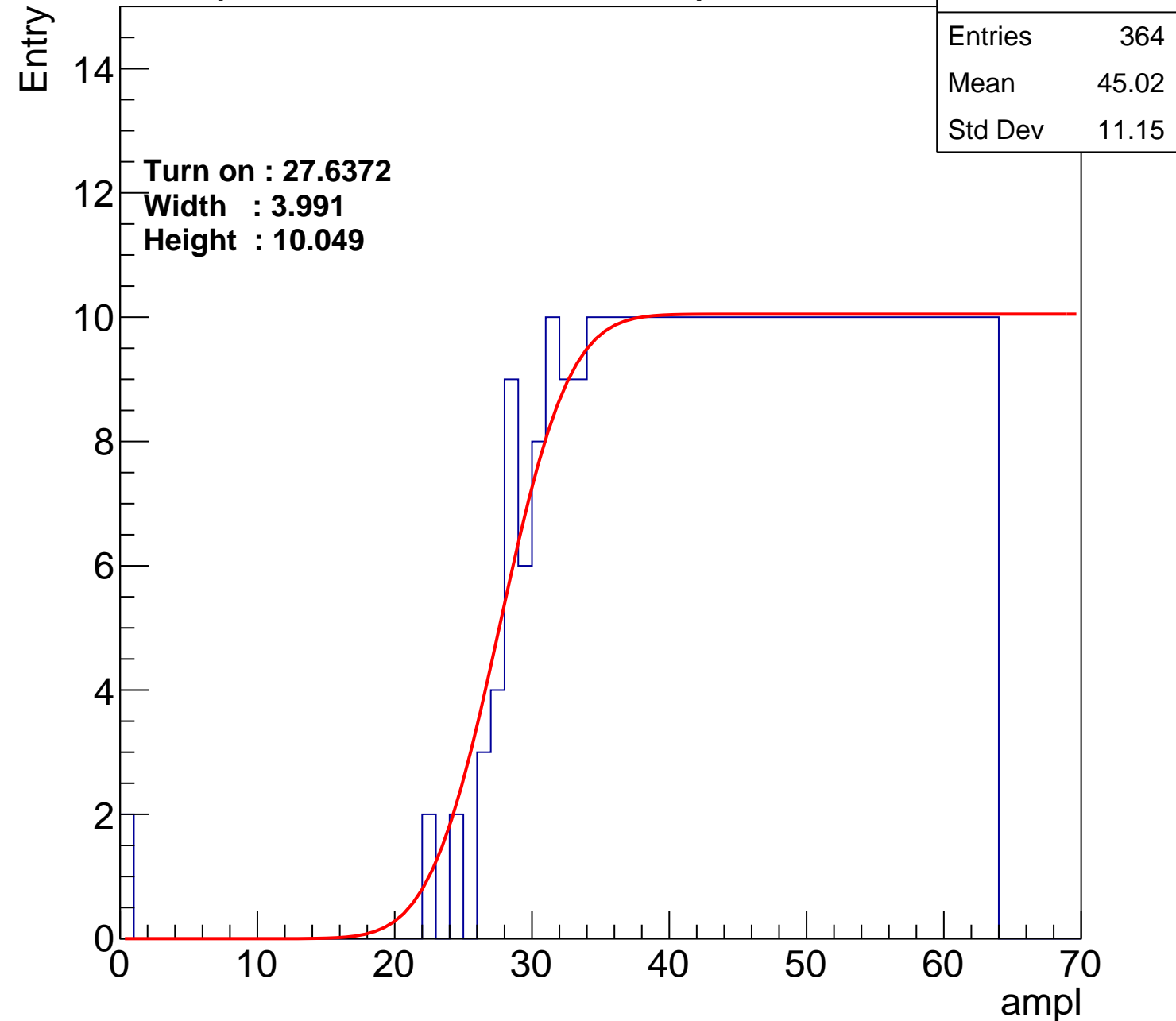
Width : 3.991

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch3

calib_packv5_042523_0143.root, FC#0, port D2

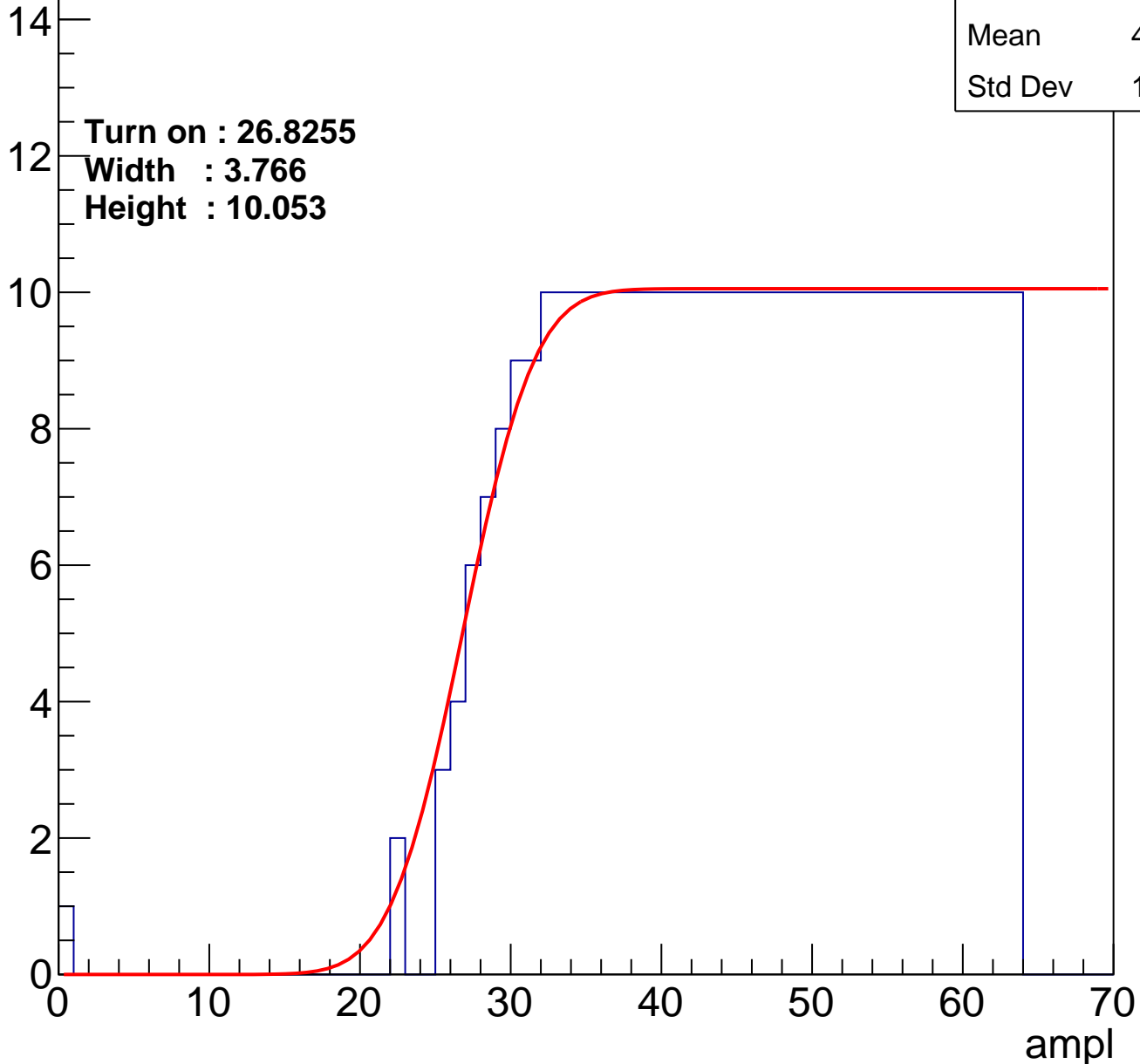
Entries	369
Mean	44.88
Std Dev	11.02

Turn on : 26.8255

Width : 3.766

Height : 10.053

Entry



B1L101S, U24-ch4

calib_packv5_042523_0143.root, FC#0, port D2

Entries	370
Mean	44.71
Std Dev	11.42

Turn on : 27.3874

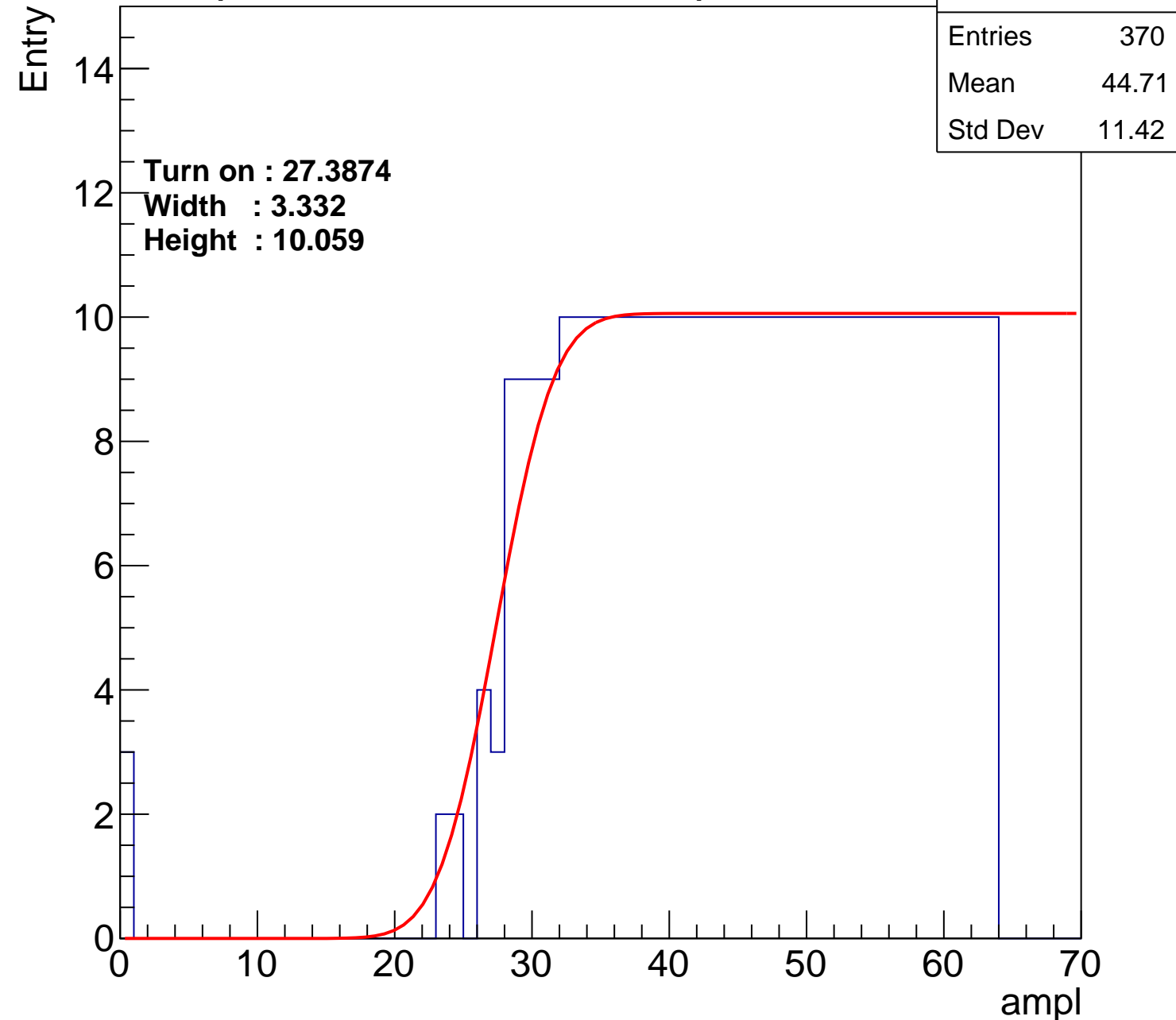
Width : 3.332

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch5

calib_packv5_042523_0143.root, FC#0, port D2

Entries	343
Mean	46.04
Std Dev	10.65

Turn on : 29.8639

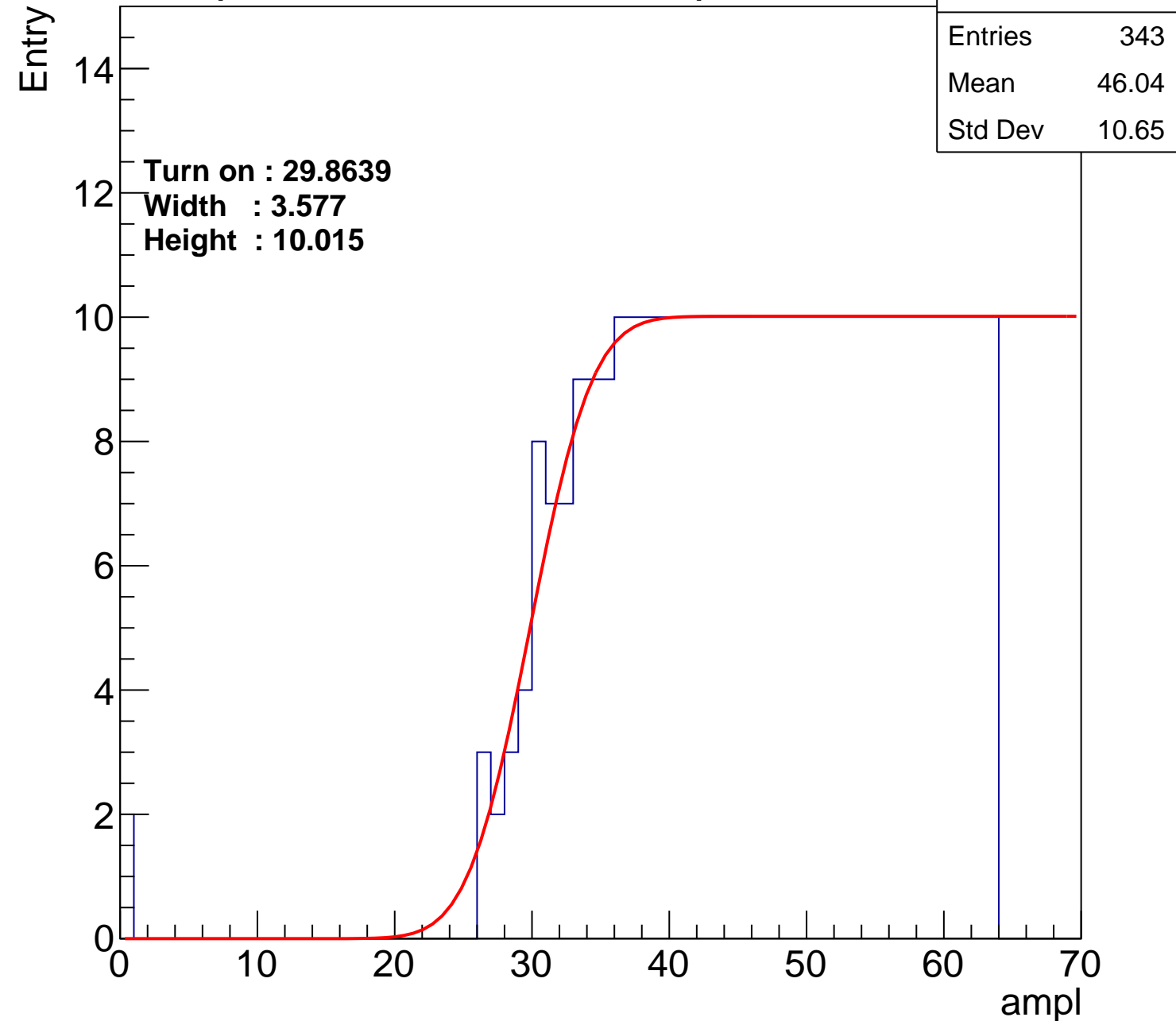
Width : 3.577

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch6

calib_packv5_042523_0143.root, FC#0, port D2

Entries	367
Mean	44.94
Std Dev	11.03

Turn on : 27.4556

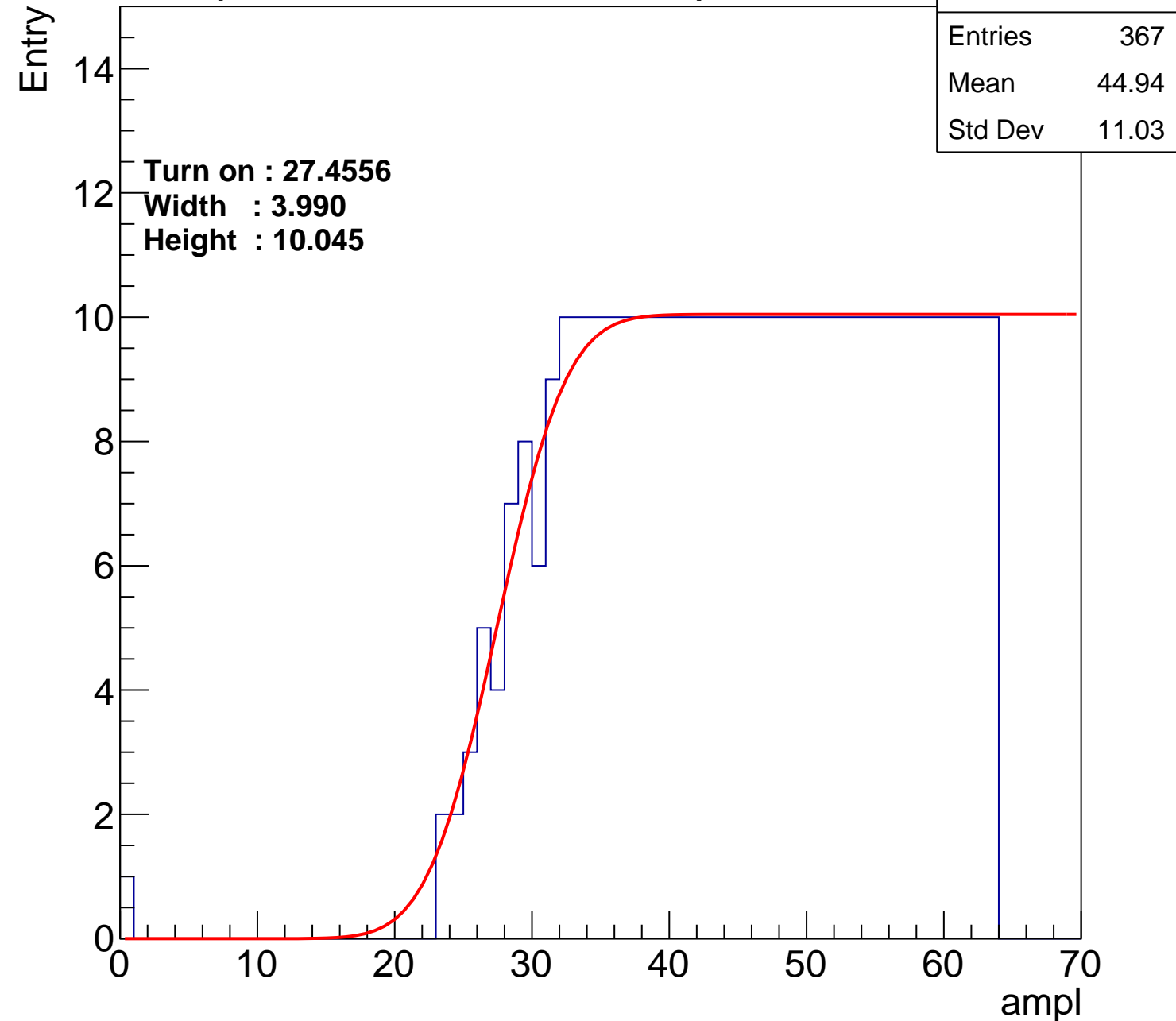
Width : 3.990

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch7

calib_packv5_042523_0143.root, FC#0, port D2

Entries	370
Mean	44.63
Std Dev	11.54

Turn on : 27.7543

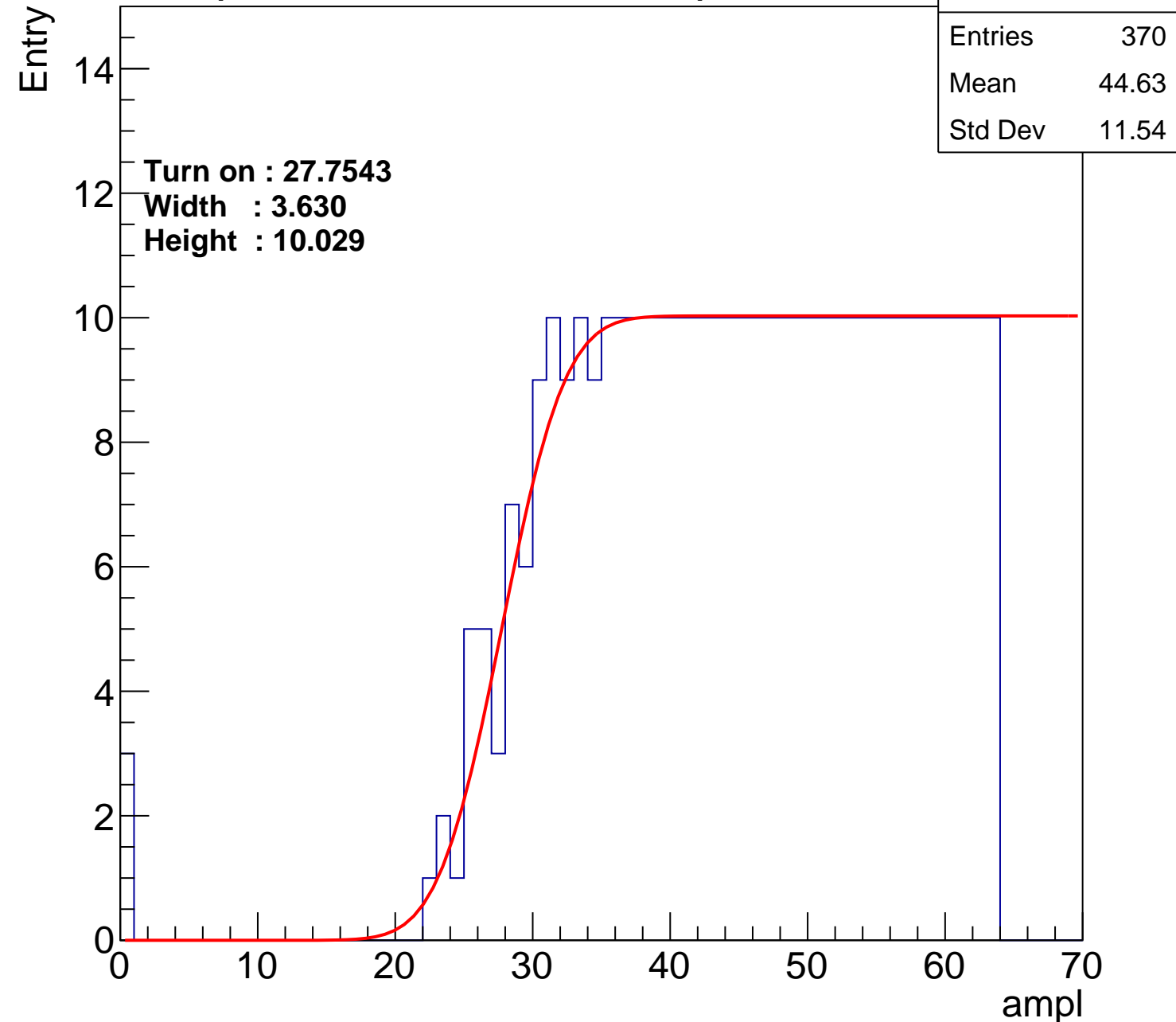
Width : 3.630

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch8

calib_packv5_042523_0143.root, FC#0, port D2

Entries	367
Mean	44.77
Std Dev	11.56

Turn on : 27.6444

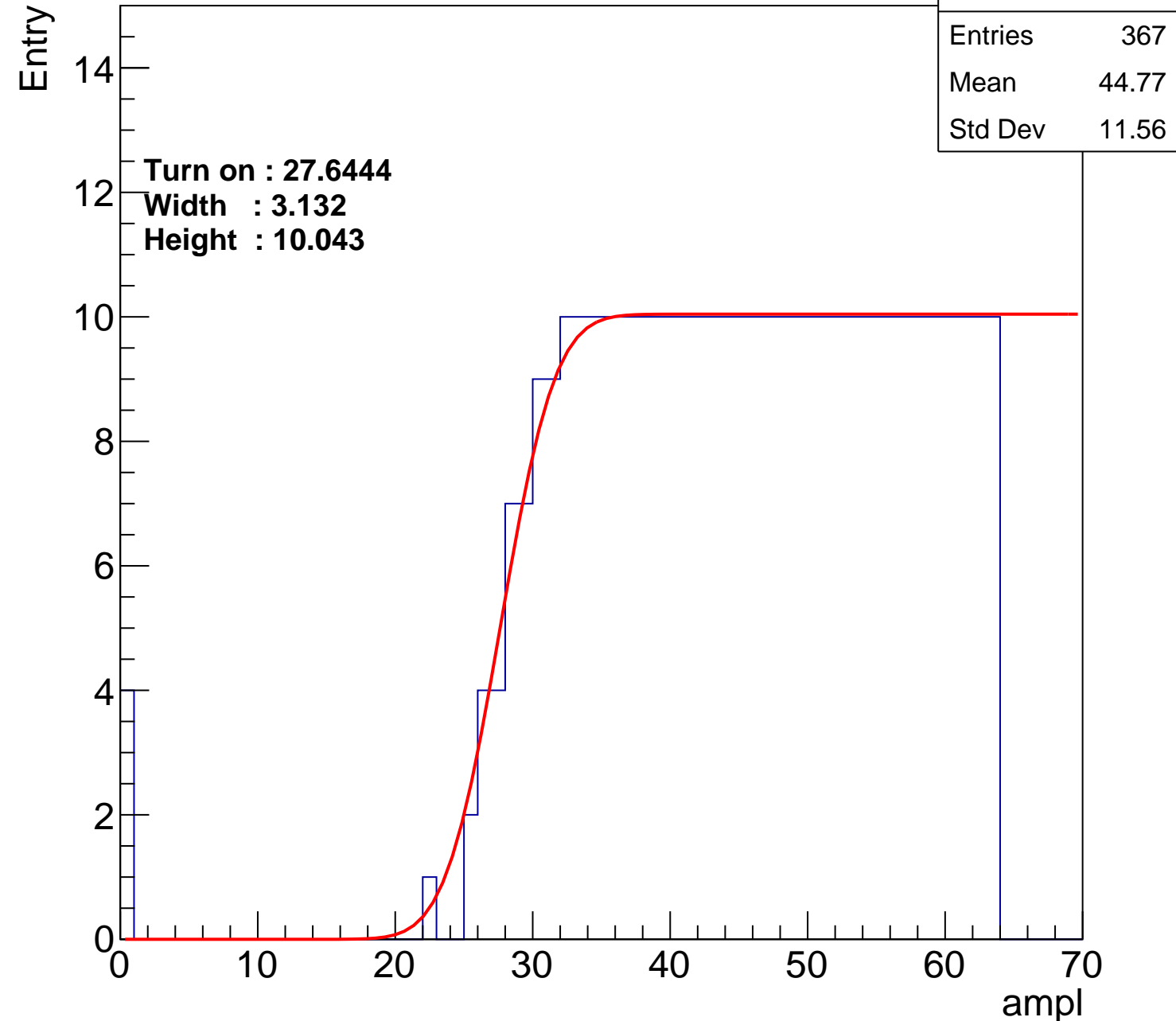
Width : 3.132

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch9

calib_packv5_042523_0143.root, FC#0, port D2

Entries	381
Mean	44.14
Std Dev	11.73

Turn on : 26.2643

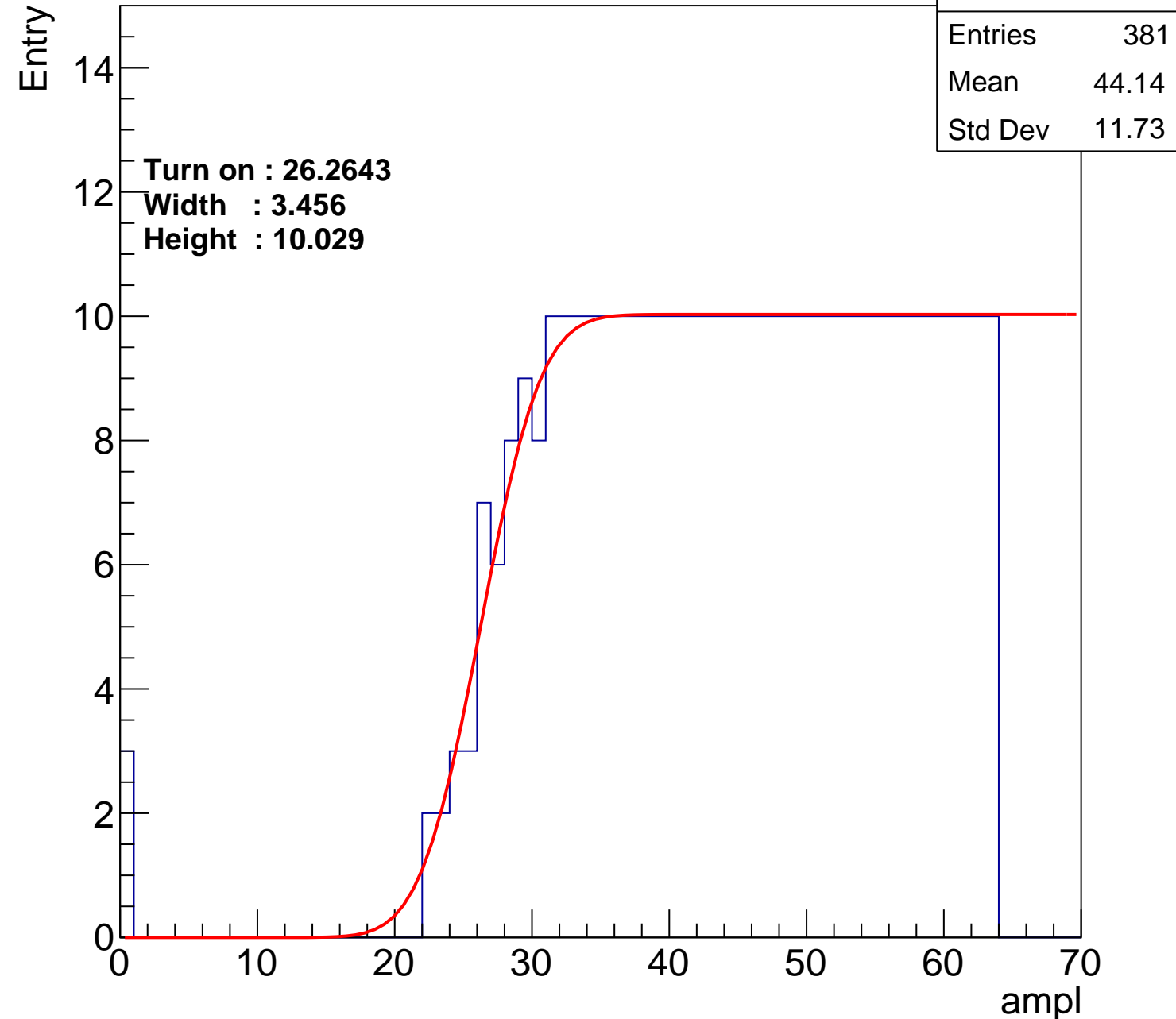
Width : 3.456

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch10

calib_packv5_042523_0143.root, FC#0, port D2

Entries	361
Mean	45.05
Std Dev	11.45

Turn on : 28.2600

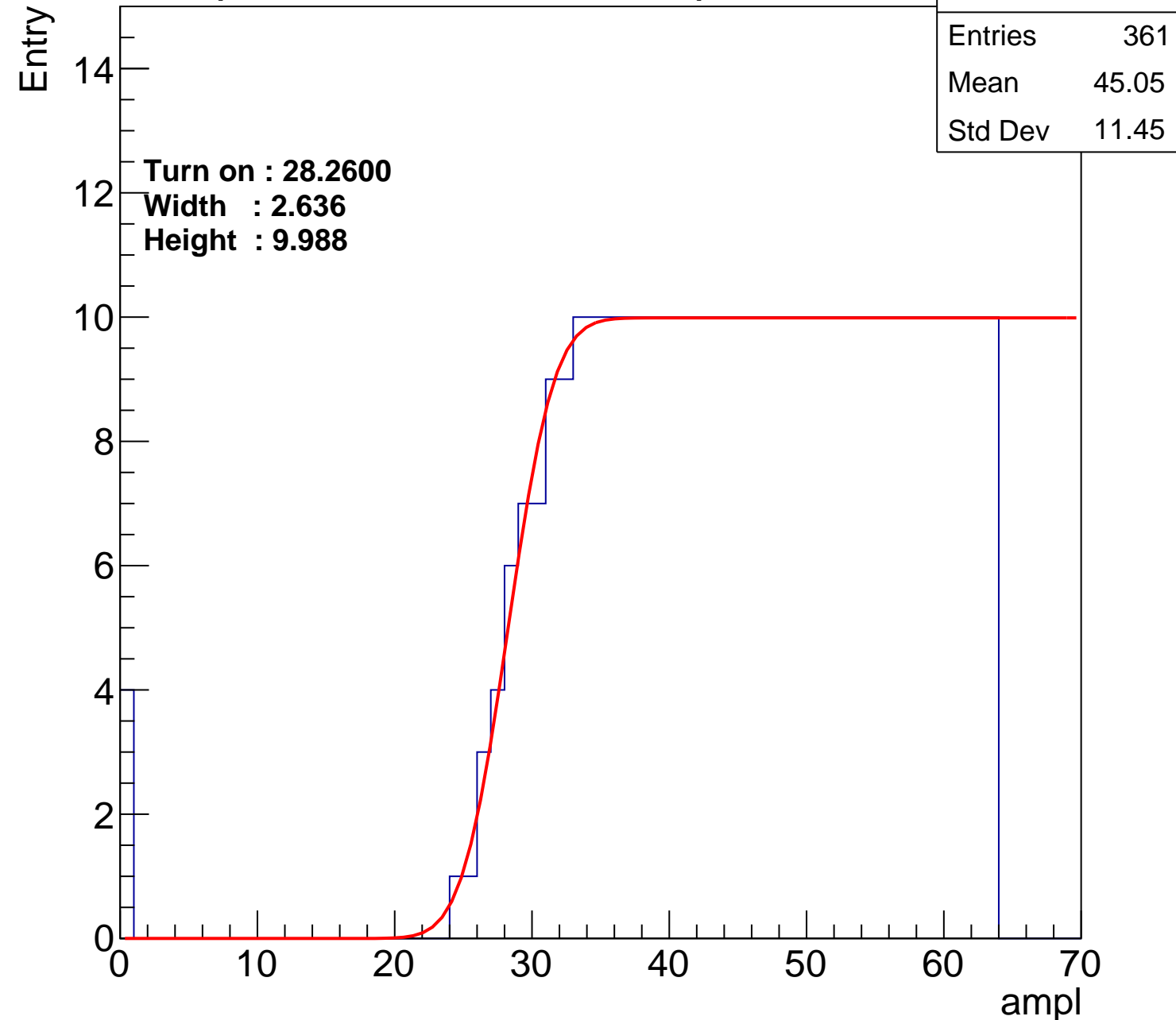
Width : 2.636

Height : 9.988

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch11

calib_packv5_042523_0143.root, FC#0, port D2

Entries	361
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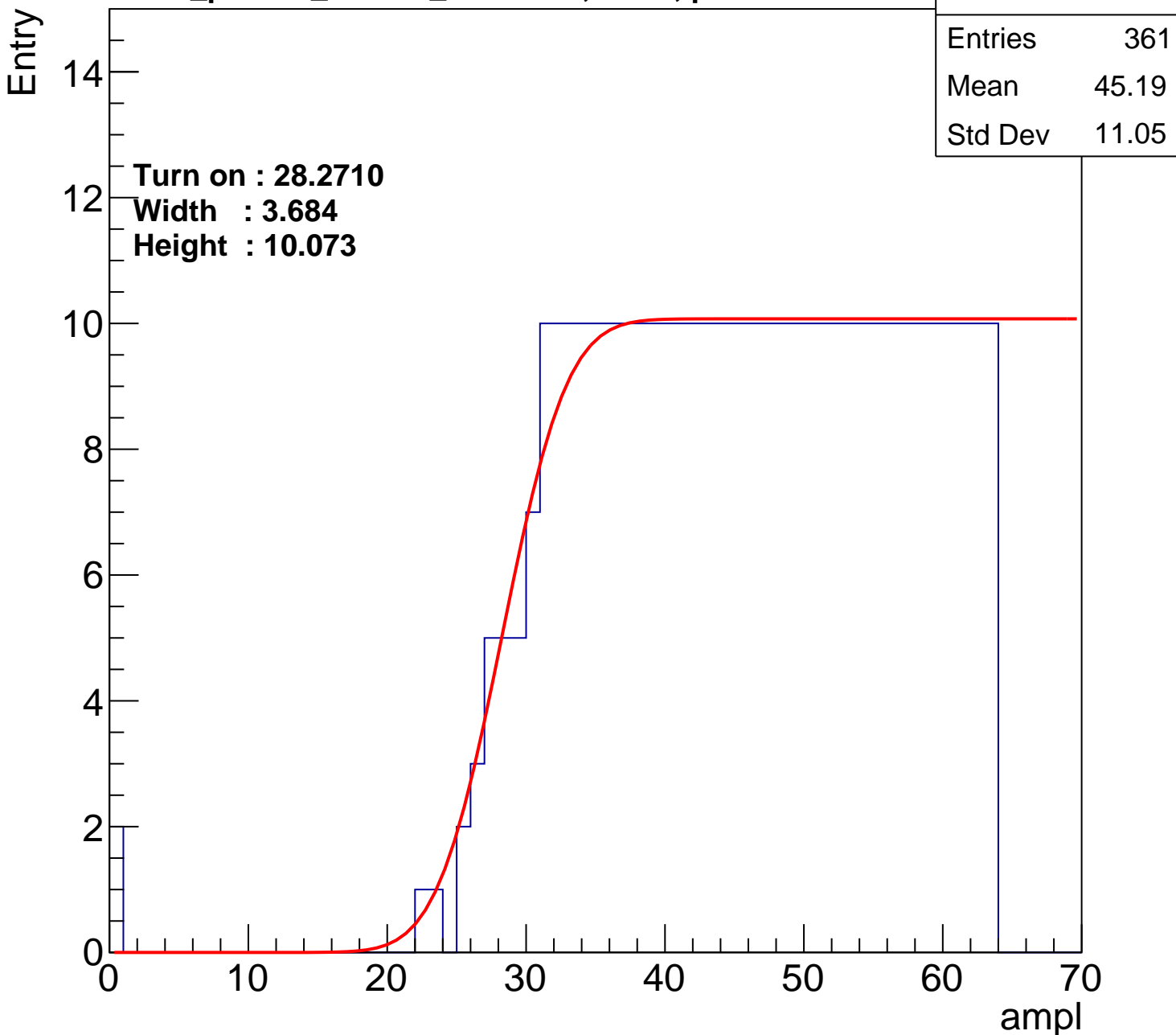
Mean	45.19
------	-------

Std Dev	11.05
---------	-------

Turn on : 28.2710

Width : 3.684

Height : 10.073



B1L101S, U24-ch12

calib_packv5_042523_0143.root, FC#0, port D2

Entries	370
Mean	44.82
Std Dev	11.07

Turn on : 27.1878

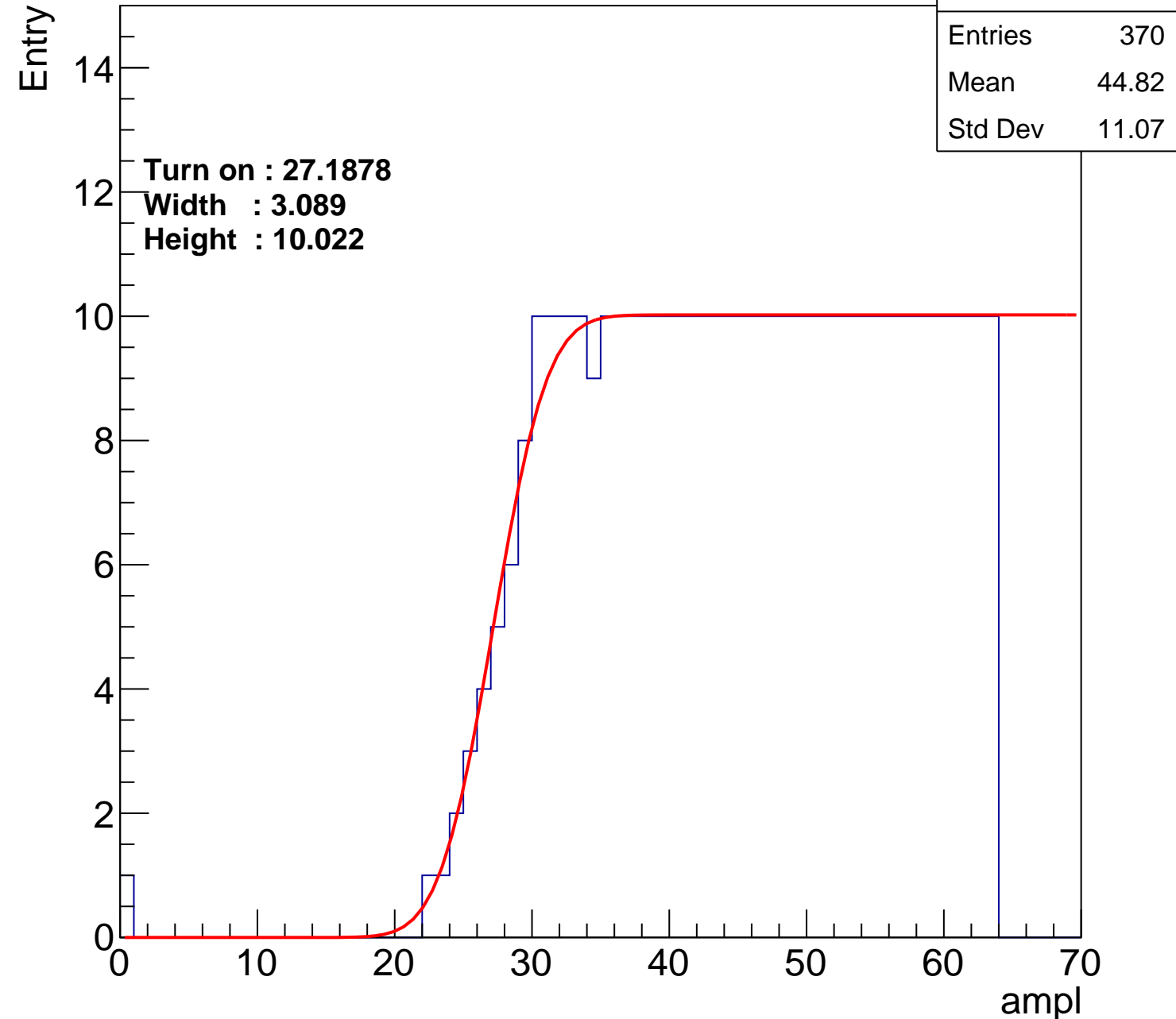
Width : 3.089

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch13

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.49
Std Dev	11.23

Turn on : 26.7908

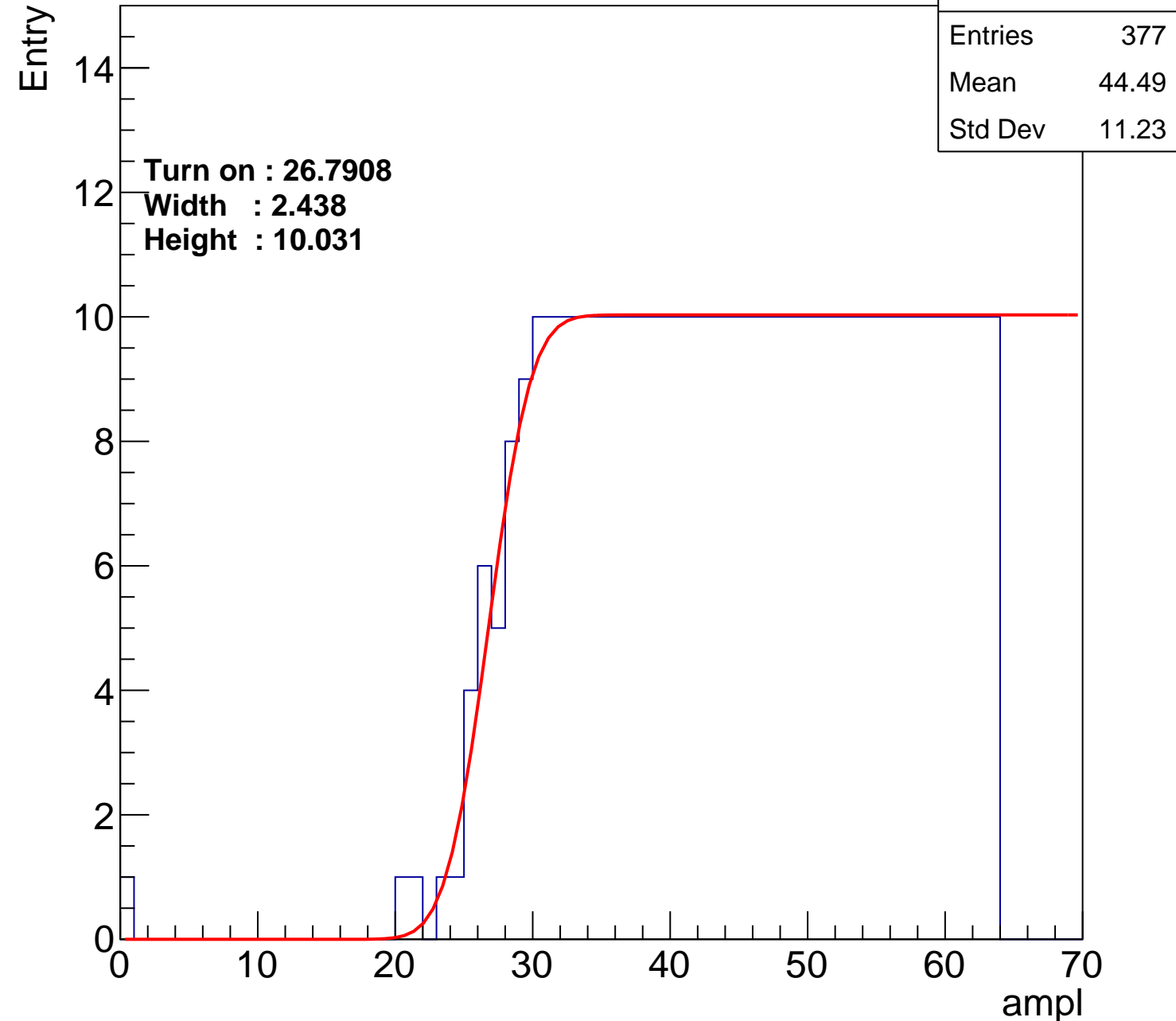
Width : 2.438

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch14

calib_packv5_042523_0143.root, FC#0, port D2

Entries	366
Mean	44.89
Std Dev	11.34

Turn on : 27.8706

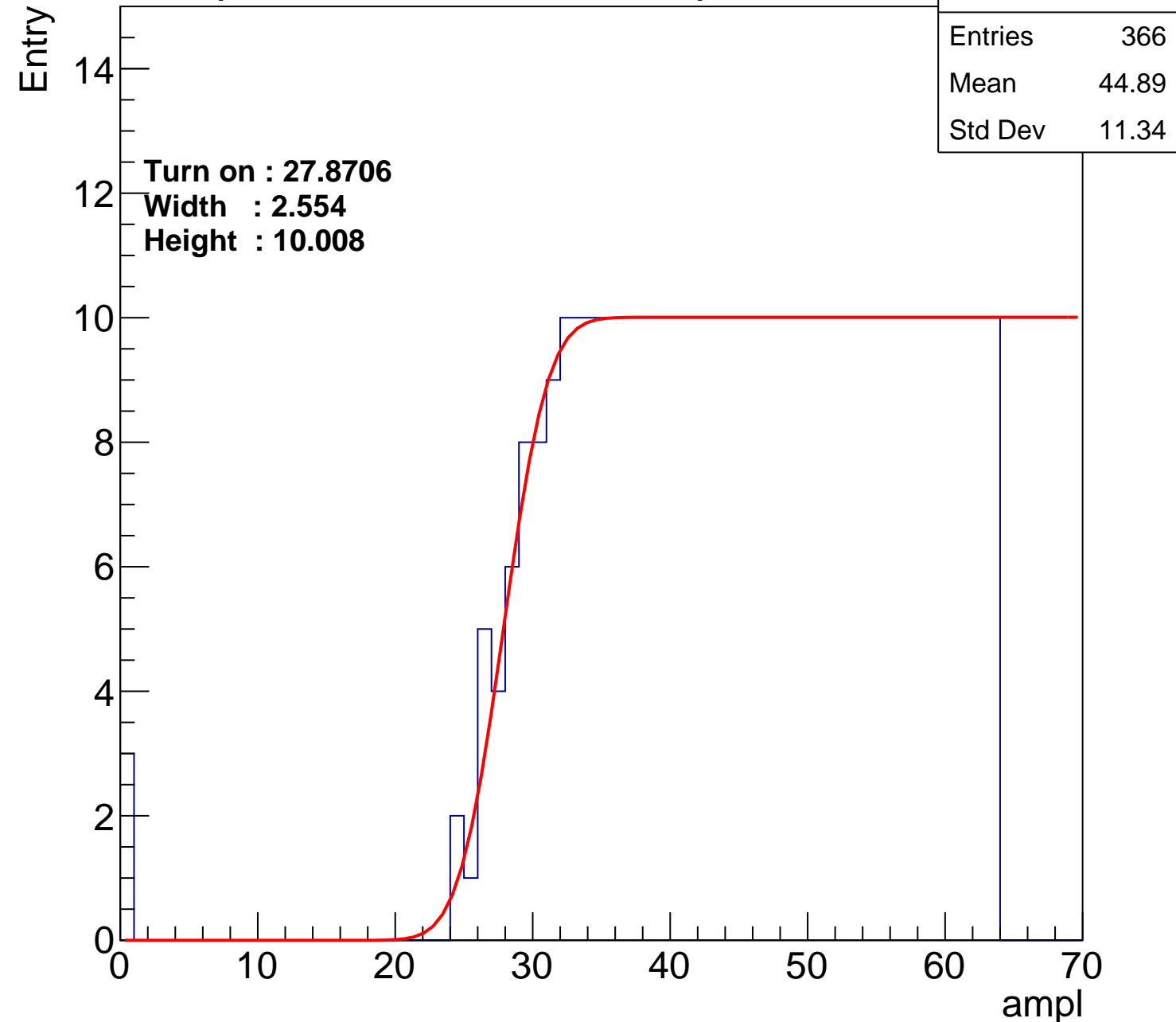
Width : 2.554

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch15

calib_packv5_042523_0143.root, FC#0, port D2

Entries	361
Mean	45.29
Std Dev	10.78

Turn on : 28.2607

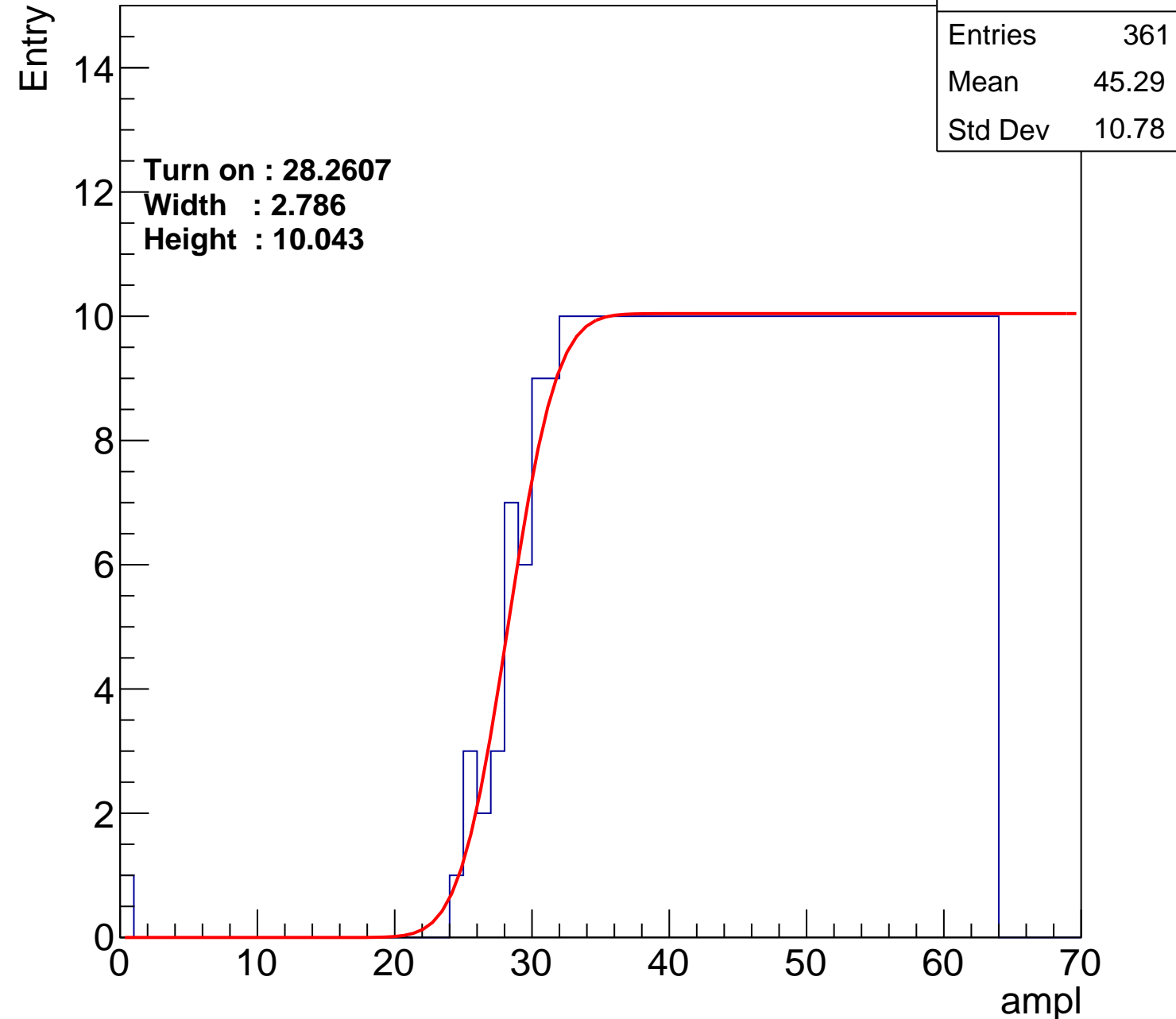
Width : 2.786

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch16

calib_packv5_042523_0143.root, FC#0, port D2

Entries	365
Mean	44.93
Std Dev	11.33

Turn on : 27.8550

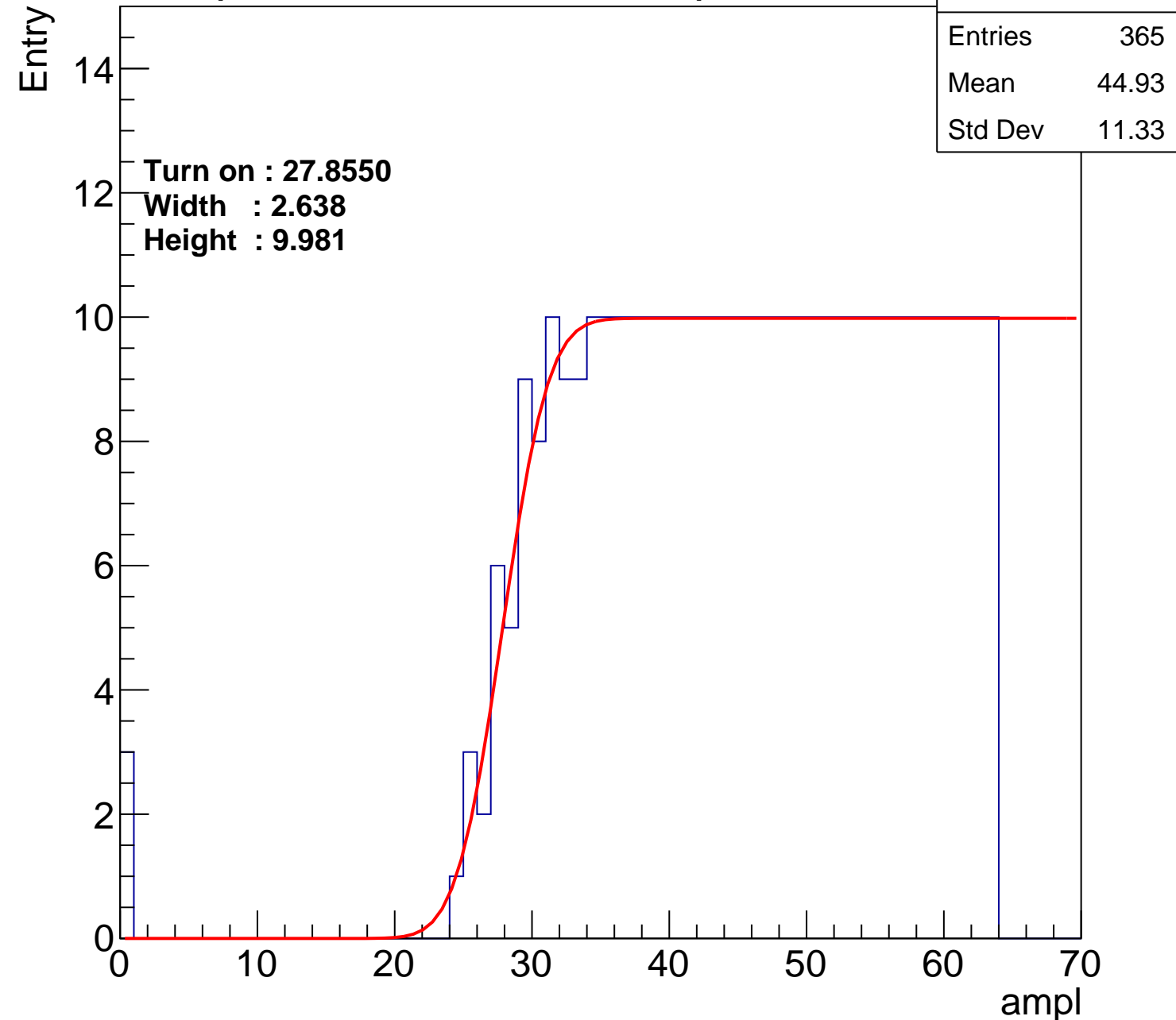
Width : 2.638

Height : 9.981

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch17

calib_packv5_042523_0143.root, FC#0, port D2

Entries	367
Mean	44.57
Std Dev	12.04

Turn on : 28.2605

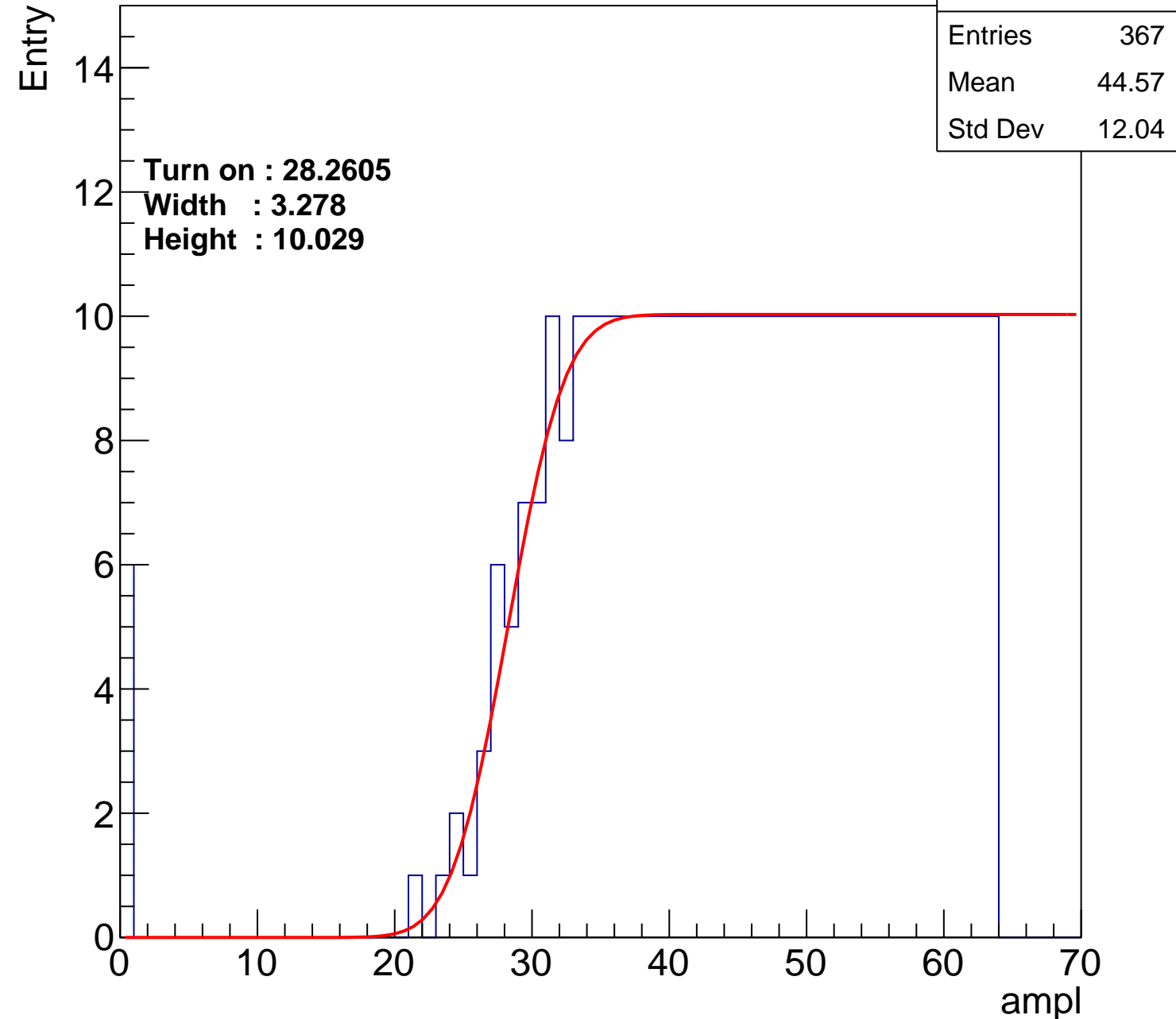
Width : 3.278

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch18

calib_packv5_042523_0143.root, FC#0, port D2

Entries	368
Mean	44.76
Std Dev	11.45

Turn on : 27.9987

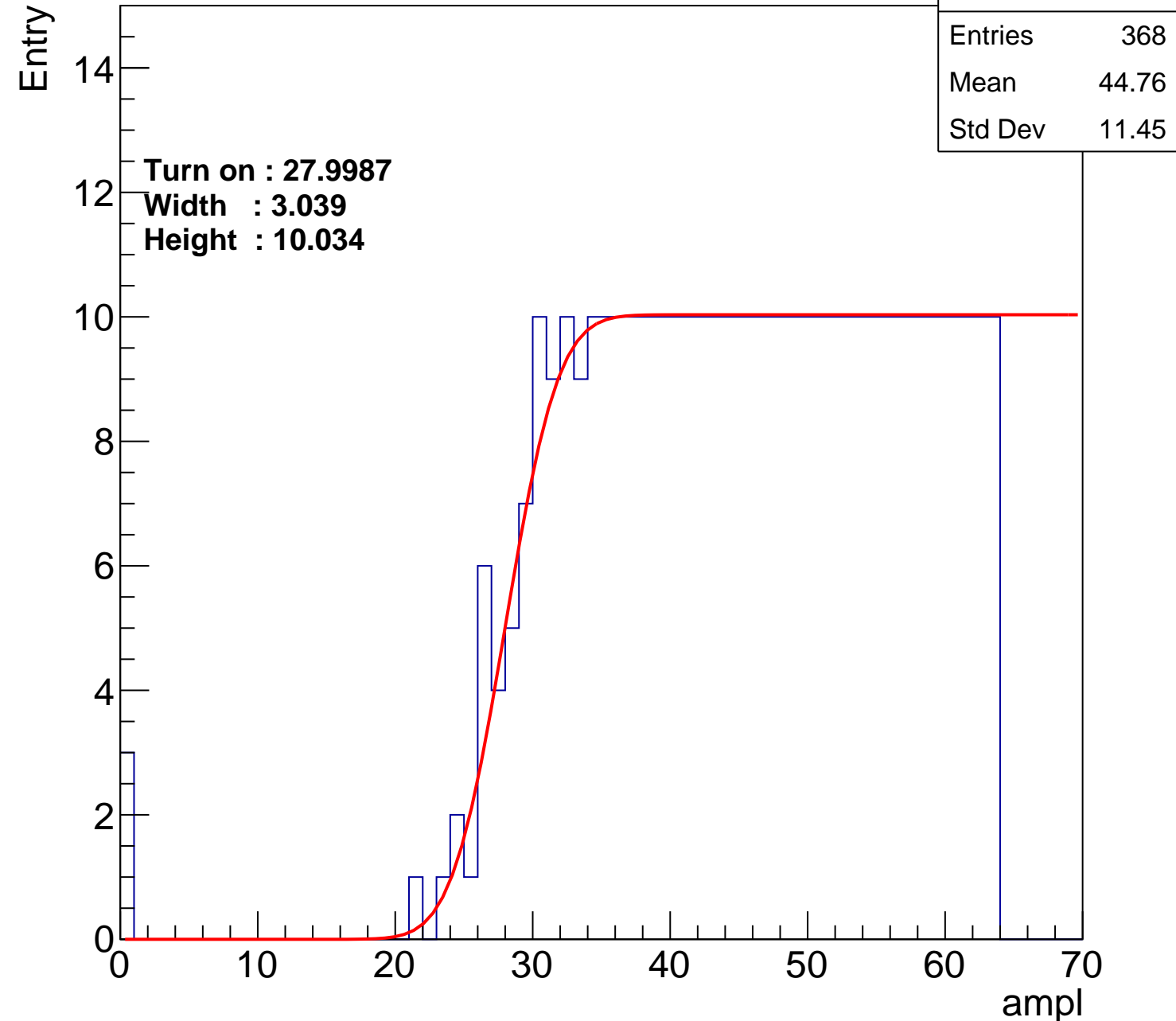
Width : 3.039

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch19

calib_packv5_042523_0143.root, FC#0, port D2

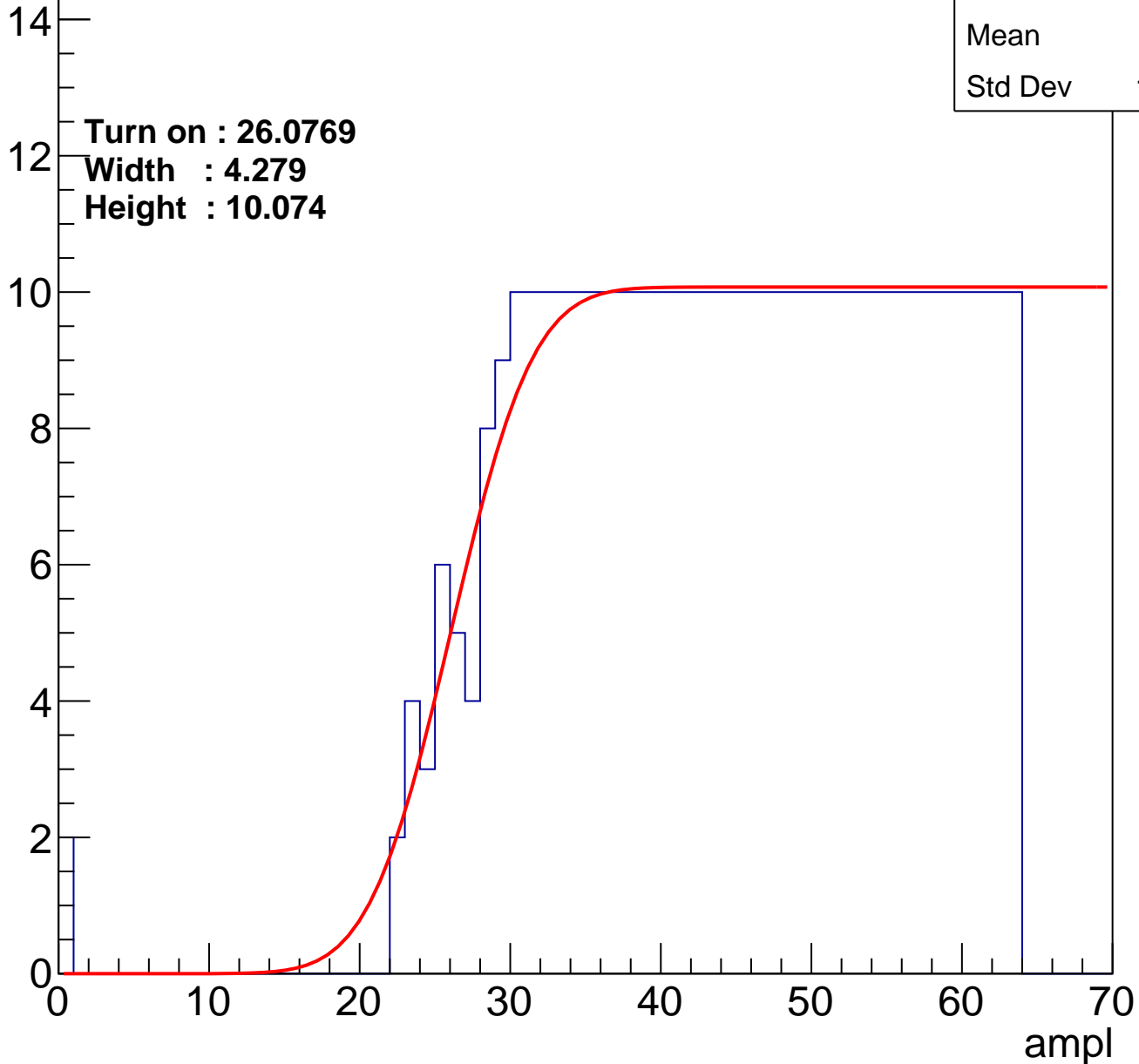
Entries	383
Mean	44.1
Std Dev	11.61

Turn on : 26.0769

Width : 4.279

Height : 10.074

Entry



B1L101S, U24-ch20

calib_packv5_042523_0143.root, FC#0, port D2

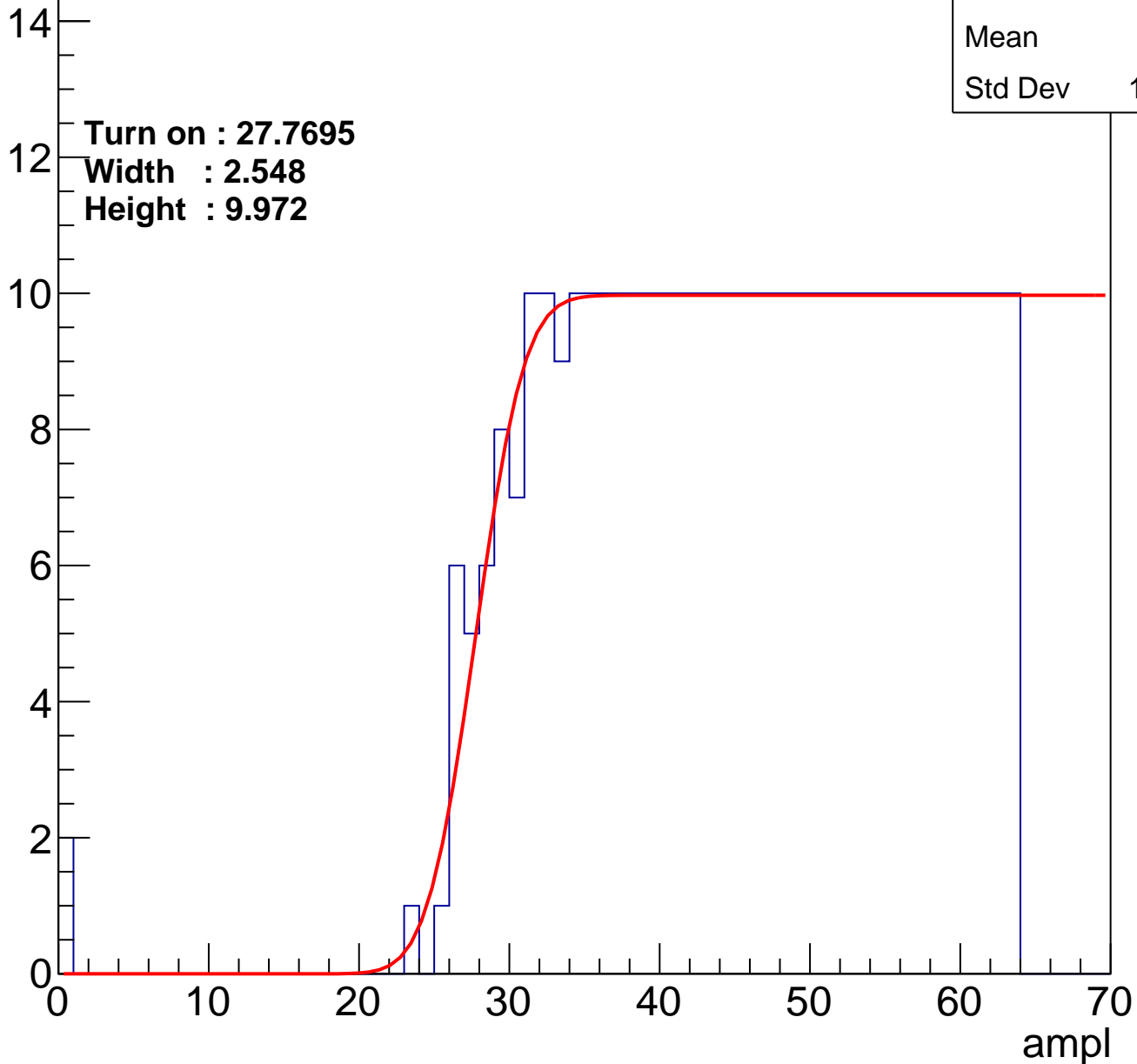
Entries	365
Mean	45
Std Dev	11.12

Turn on : 27.7695

Width : 2.548

Height : 9.972

Entry



B1L101S, U24-ch21

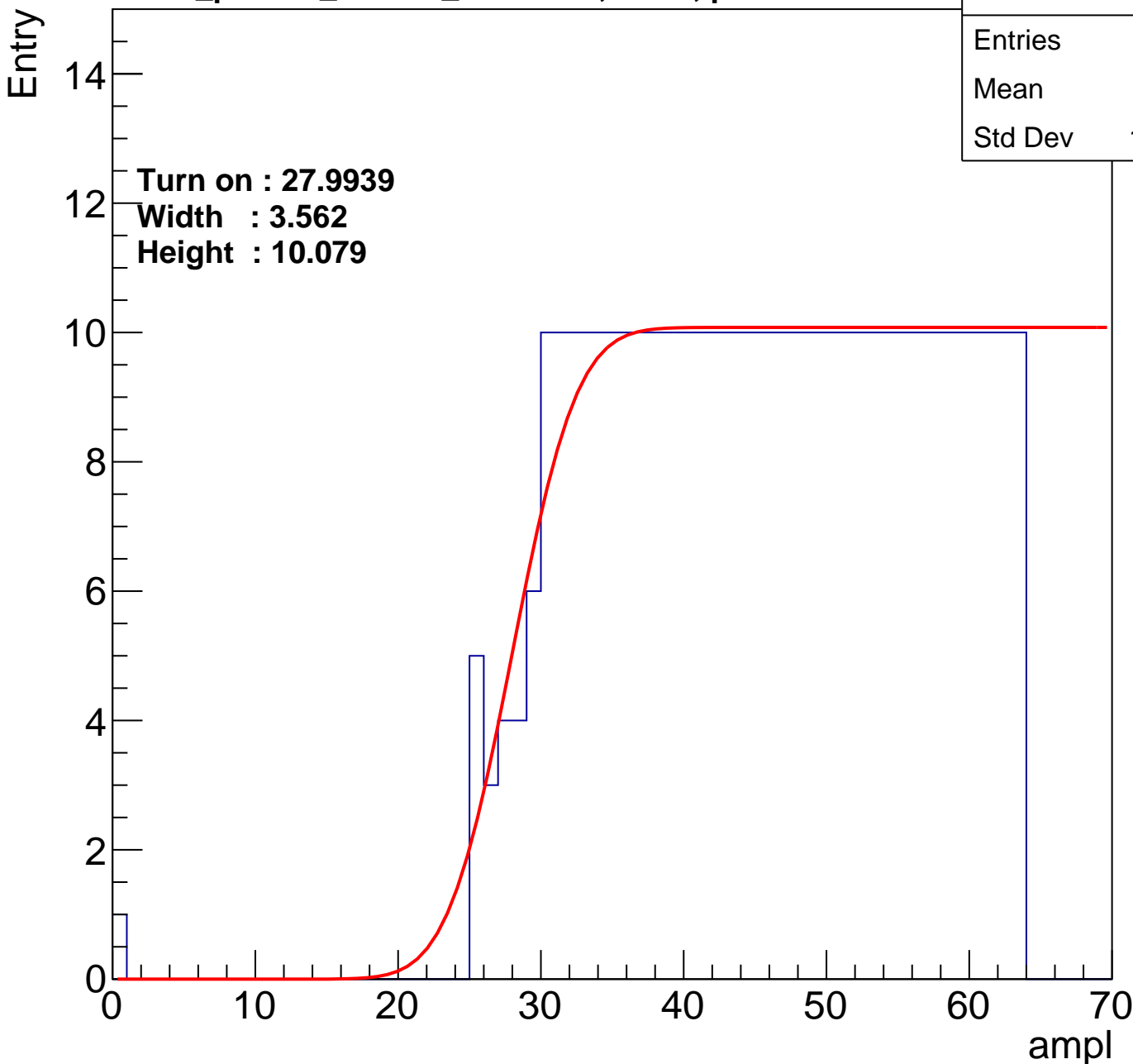
calib_packv5_042523_0143.root, FC#0, port D2

Turn on : 27.9939

Width : 3.562

Height : 10.079

Entries	363
Mean	45.2
Std Dev	10.83



B1L101S, U24-ch22

calib_packv5_042523_0143.root, FC#0, port D2

Entries	365
Mean	44.92
Std Dev	11.34

Turn on : 27.9689

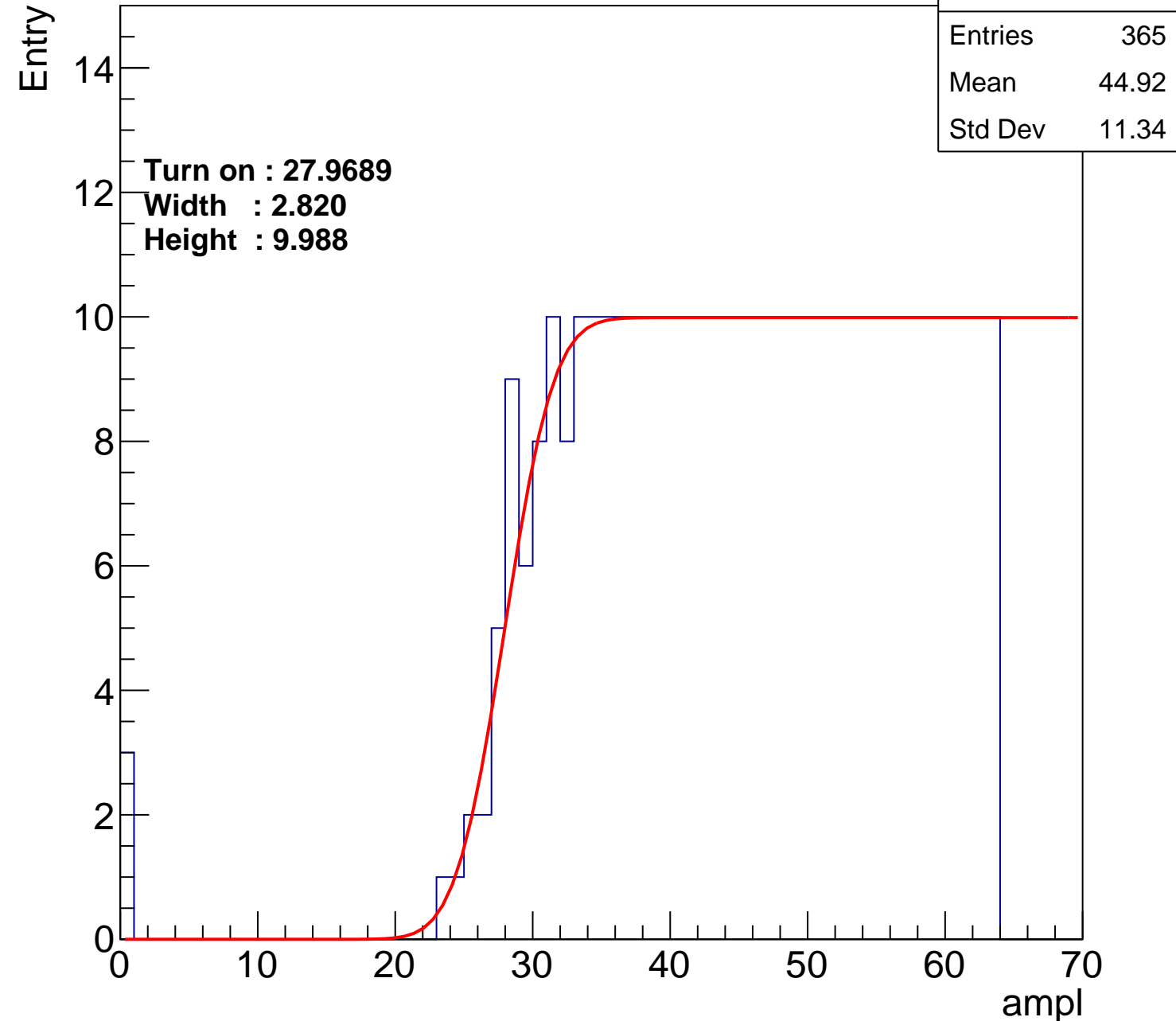
Width : 2.820

Height : 9.988

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch23

calib_packv5_042523_0143.root, FC#0, port D2

Entries	361
Mean	45.29
Std Dev	10.78

Turn on : 27.6326

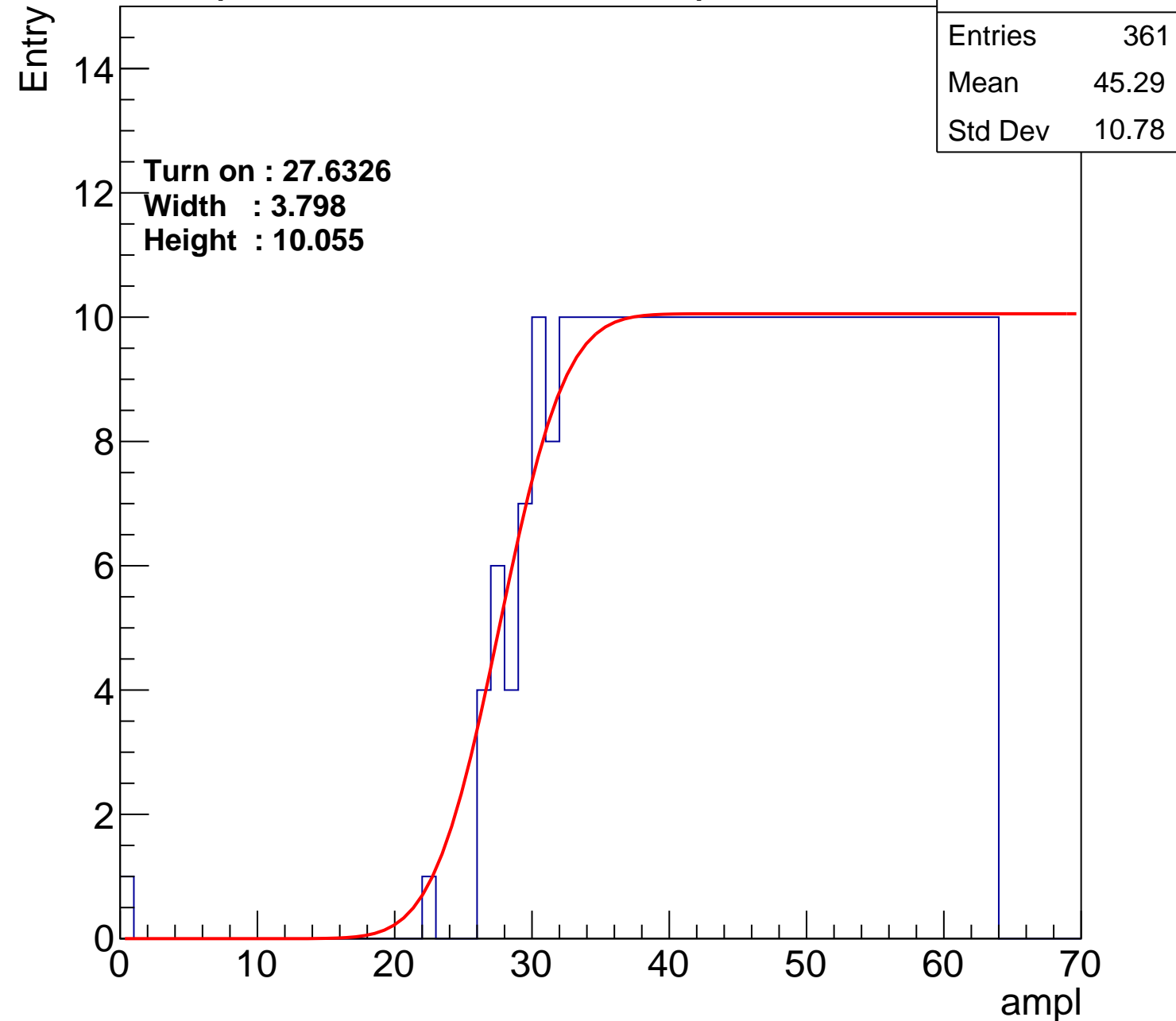
Width : 3.798

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch24

calib_packv5_042523_0143.root, FC#0, port D2

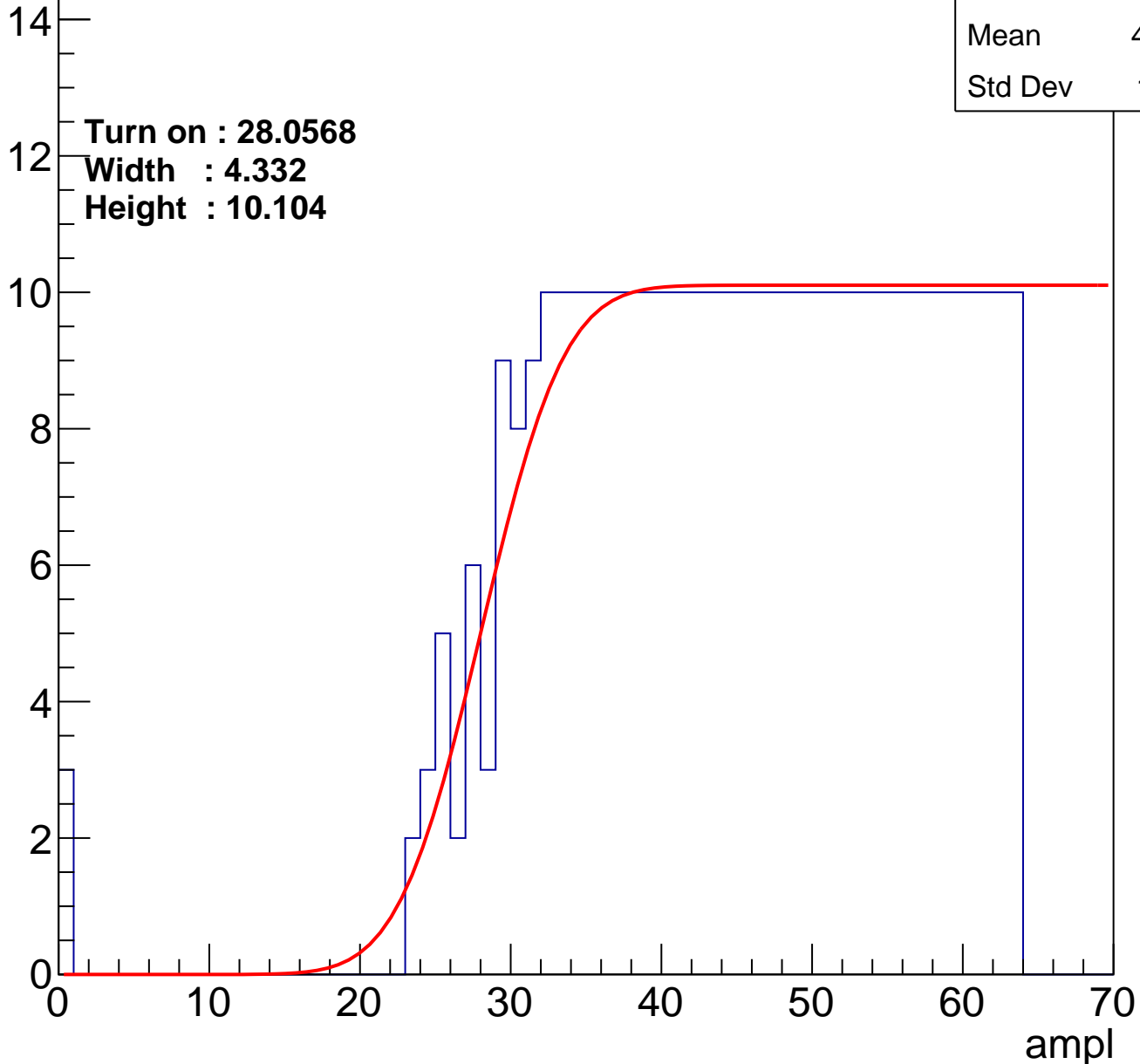
Entries	370
Mean	44.65
Std Dev	11.51

Turn on : 28.0568

Width : 4.332

Height : 10.104

Entry



B1L101S, U24-ch25

calib_packv5_042523_0143.root, FC#0, port D2

Entries	361
Mean	45.24
Std Dev	10.86

Turn on : 27.8569

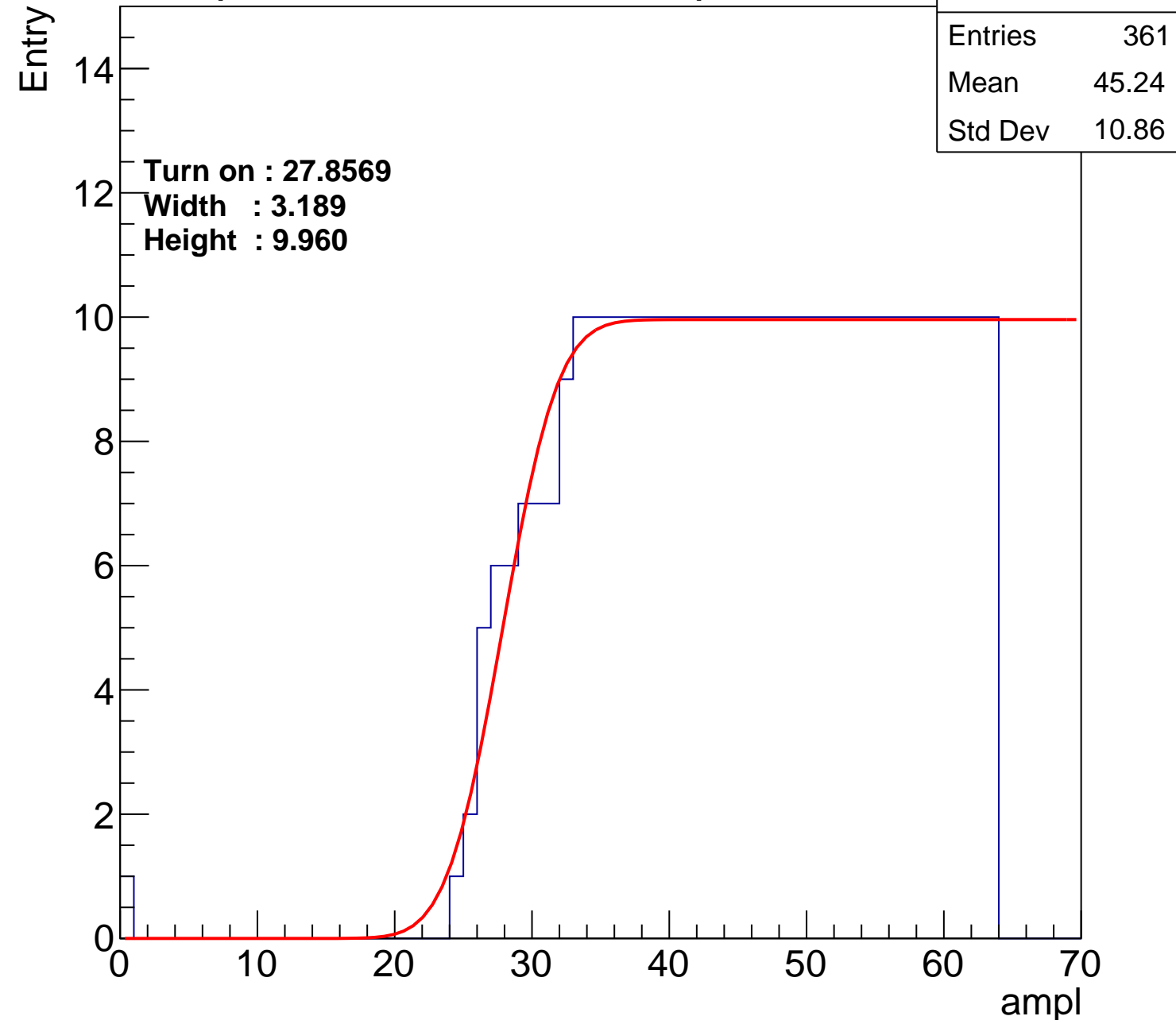
Width : 3.189

Height : 9.960

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch26

calib_packv5_042523_0143.root, FC#0, port D2

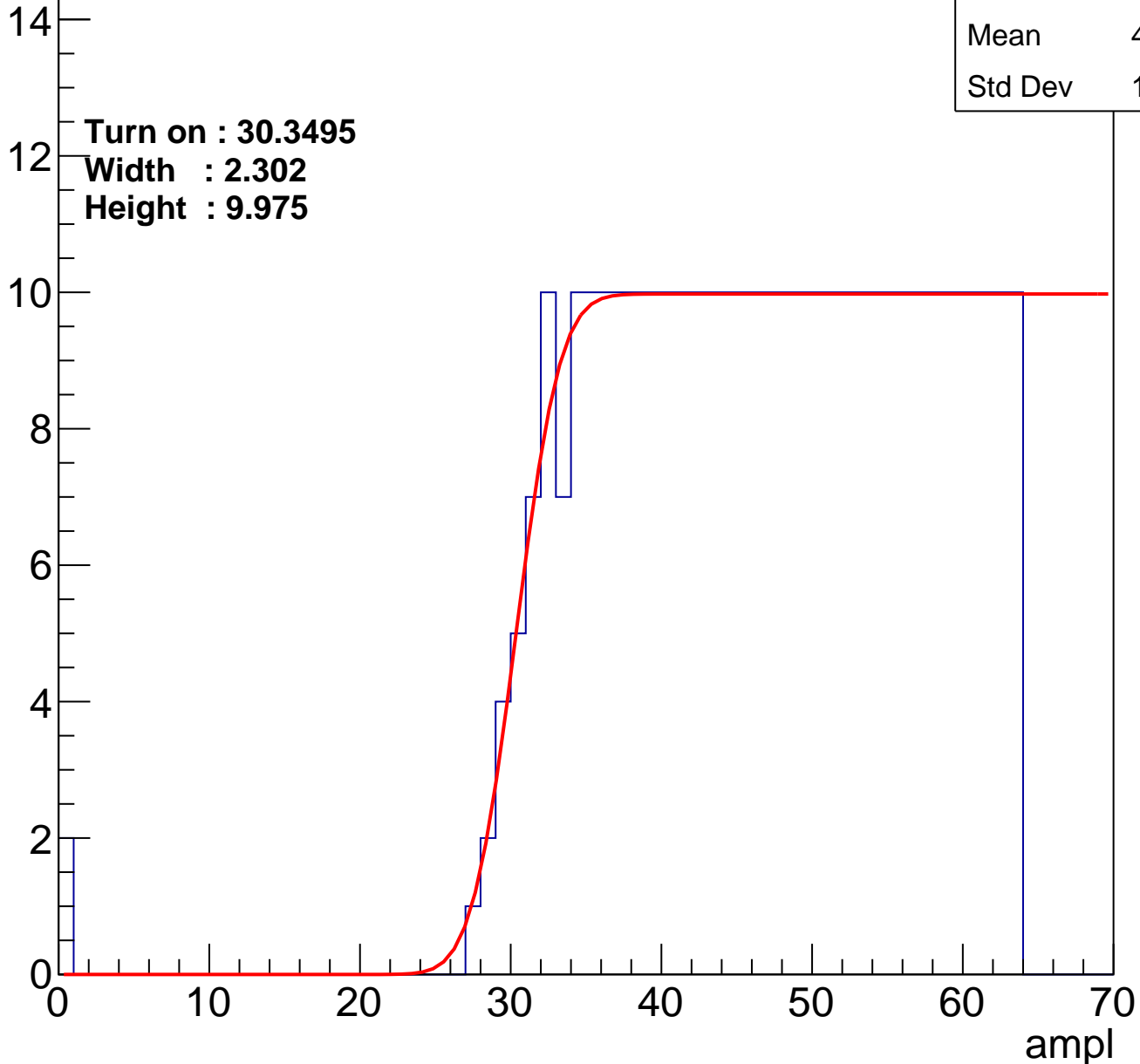
Entries	338
Mean	46.35
Std Dev	10.42

Turn on : 30.3495

Width : 2.302

Height : 9.975

Entry



B1L101S, U24-ch27

calib_packv5_042523_0143.root, FC#0, port D2

Entries	383
Mean	43.99
Std Dev	11.86

Turn on : 26.4342

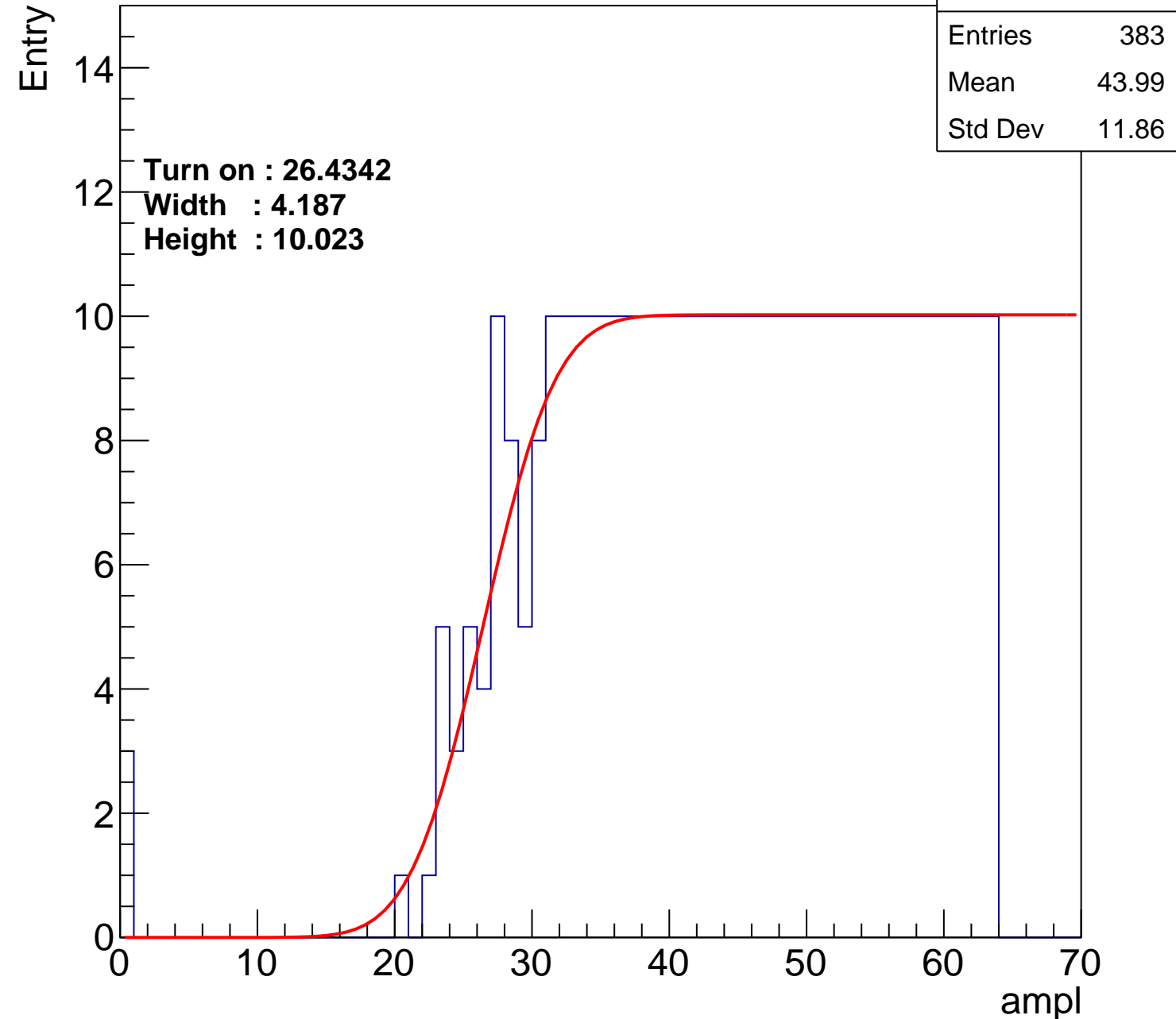
Width : 4.187

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch28

calib_packv5_042523_0143.root, FC#0, port D2

Entries	383
Mean	44.02
Std Dev	11.82

Turn on : 26.3815

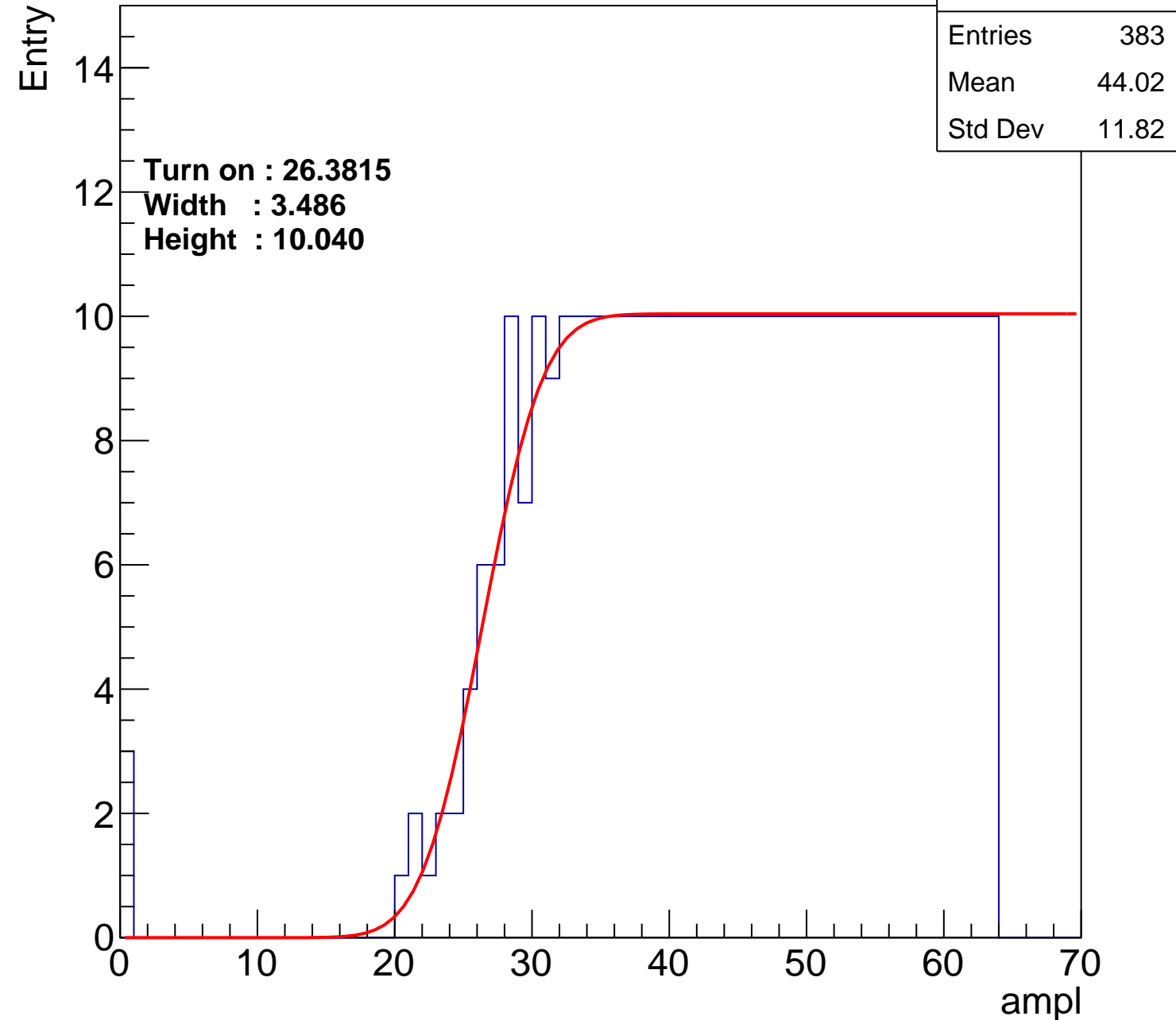
Width : 3.486

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch29

calib_packv5_042523_0143.root, FC#0, port D2

Entries	372
Mean	44.56
Std Dev	11.54

Turn on : 26.9171

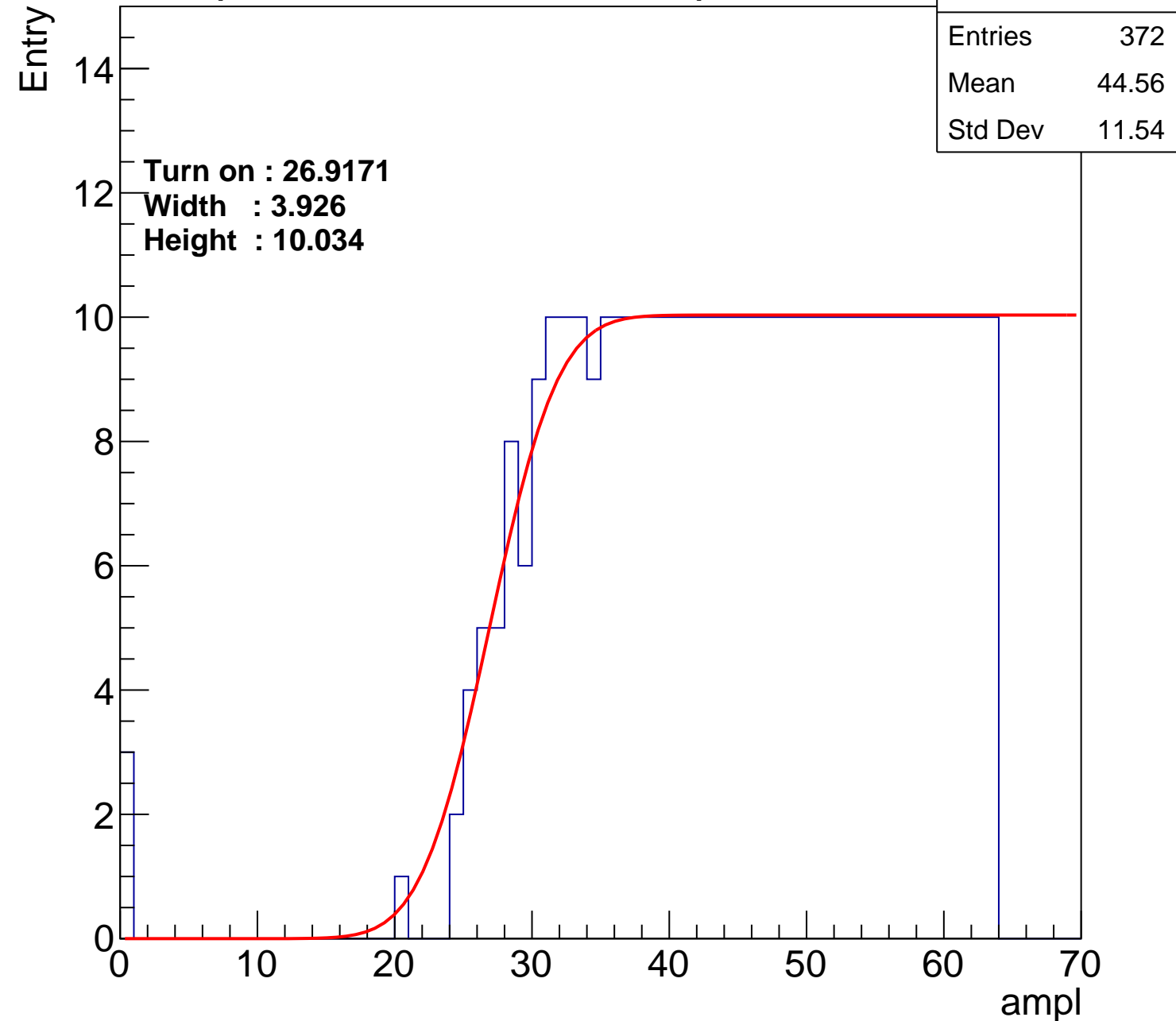
Width : 3.926

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch30

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.45
Std Dev	11.55

Turn on : 26.7940

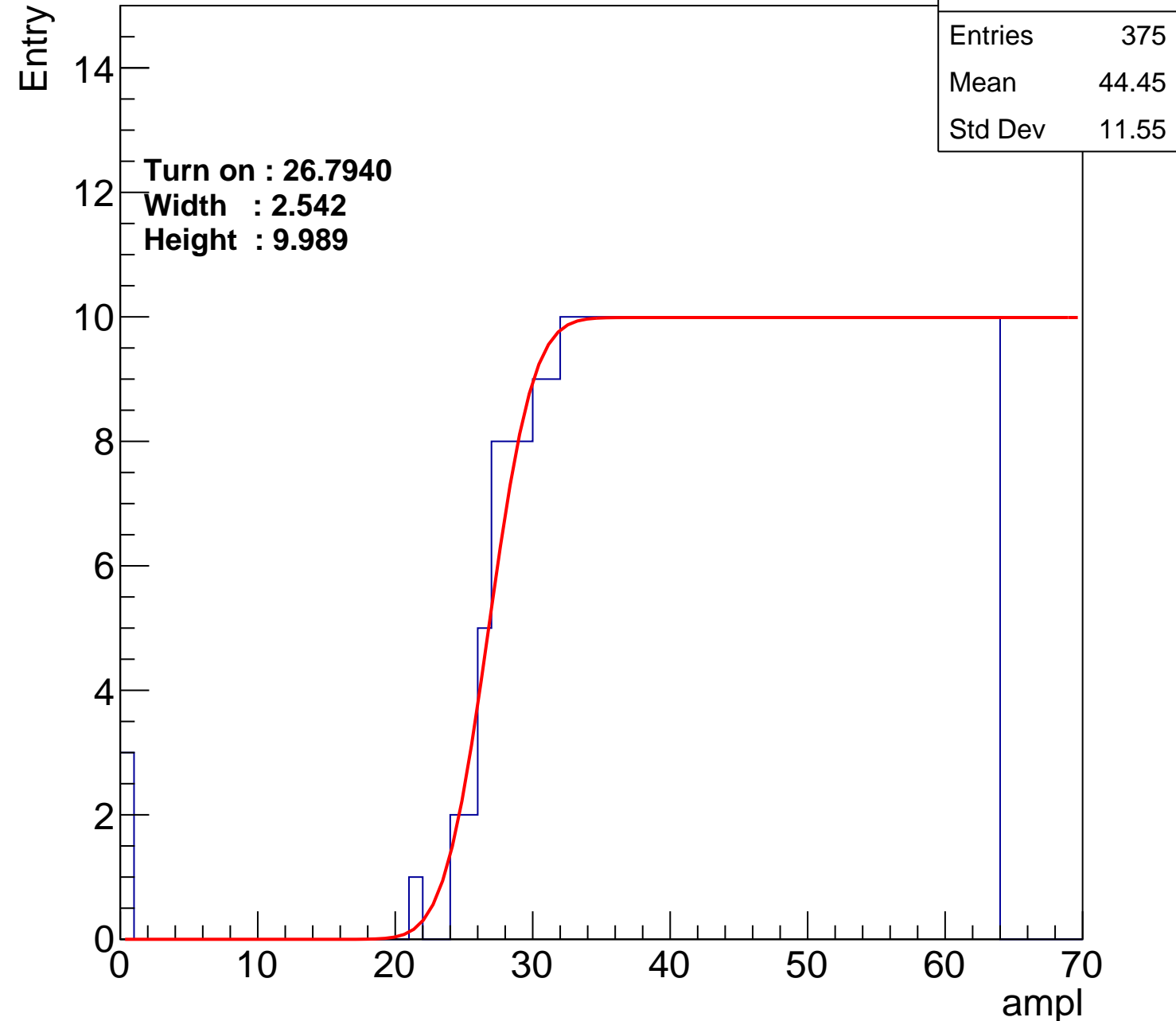
Width : 2.542

Height : 9.989

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch31

calib_packv5_042523_0143.root, FC#0, port D2

Entries	363
Mean	45.13
Std Dev	10.95

Turn on : 27.8205

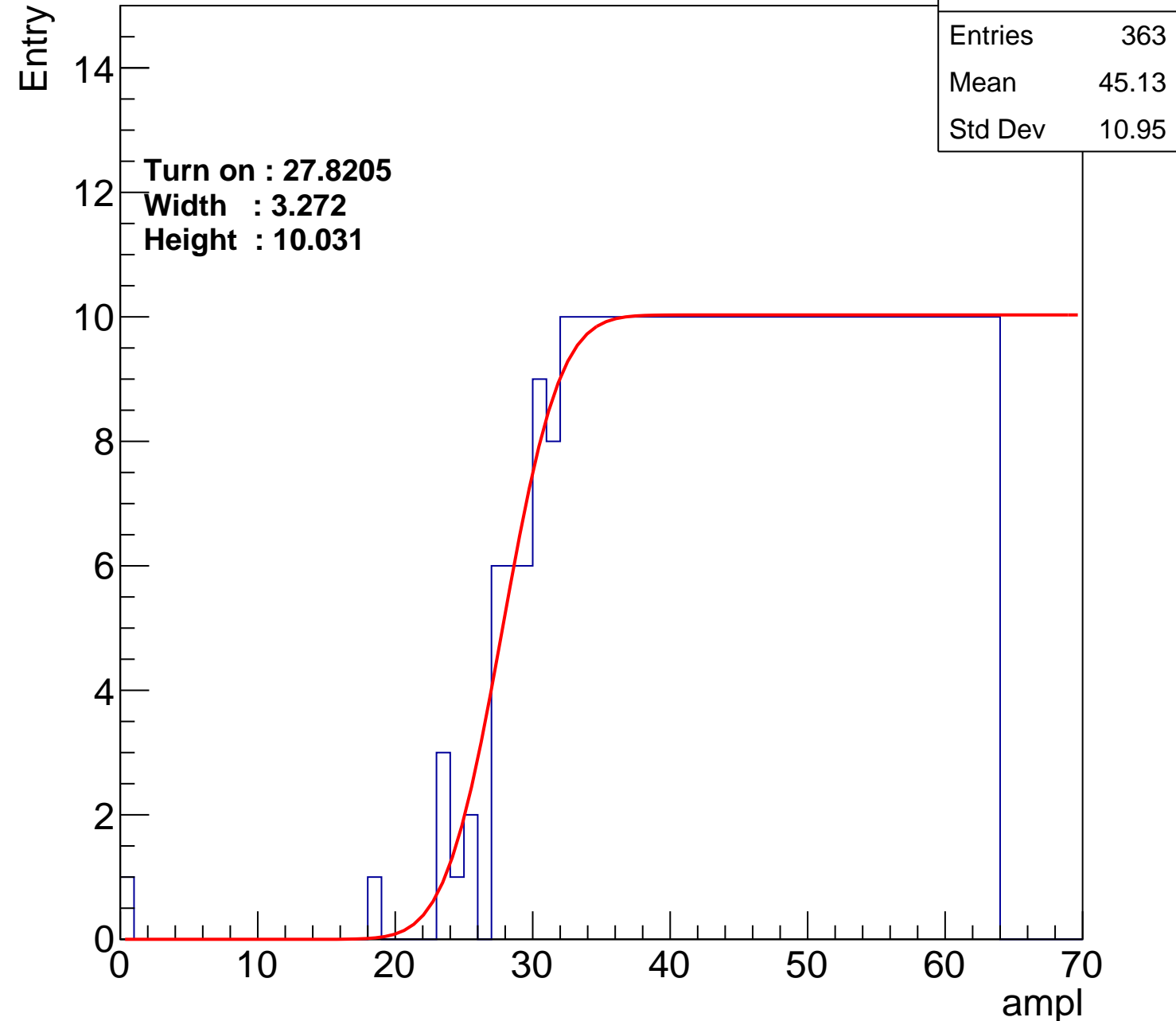
Width : 3.272

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch32

calib_packv5_042523_0143.root, FC#0, port D2

Entries	384
Mean	43.98
Std Dev	11.82

Turn on : 26.3842

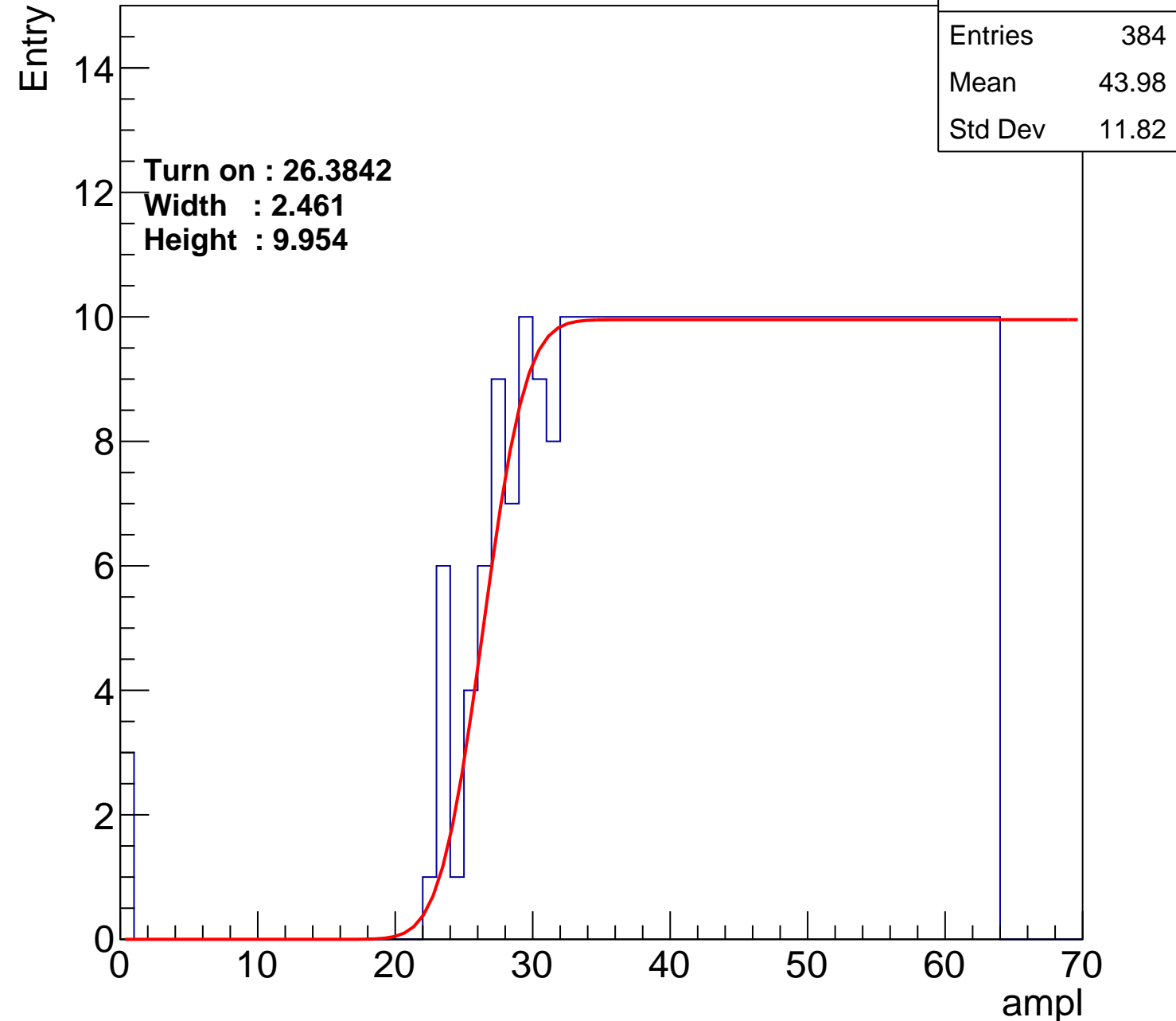
Width : 2.461

Height : 9.954

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch33

calib_packv5_042523_0143.root, FC#0, port D2

Entries	348
Mean	45.94
Std Dev	10.43

Turn on : 28.7540

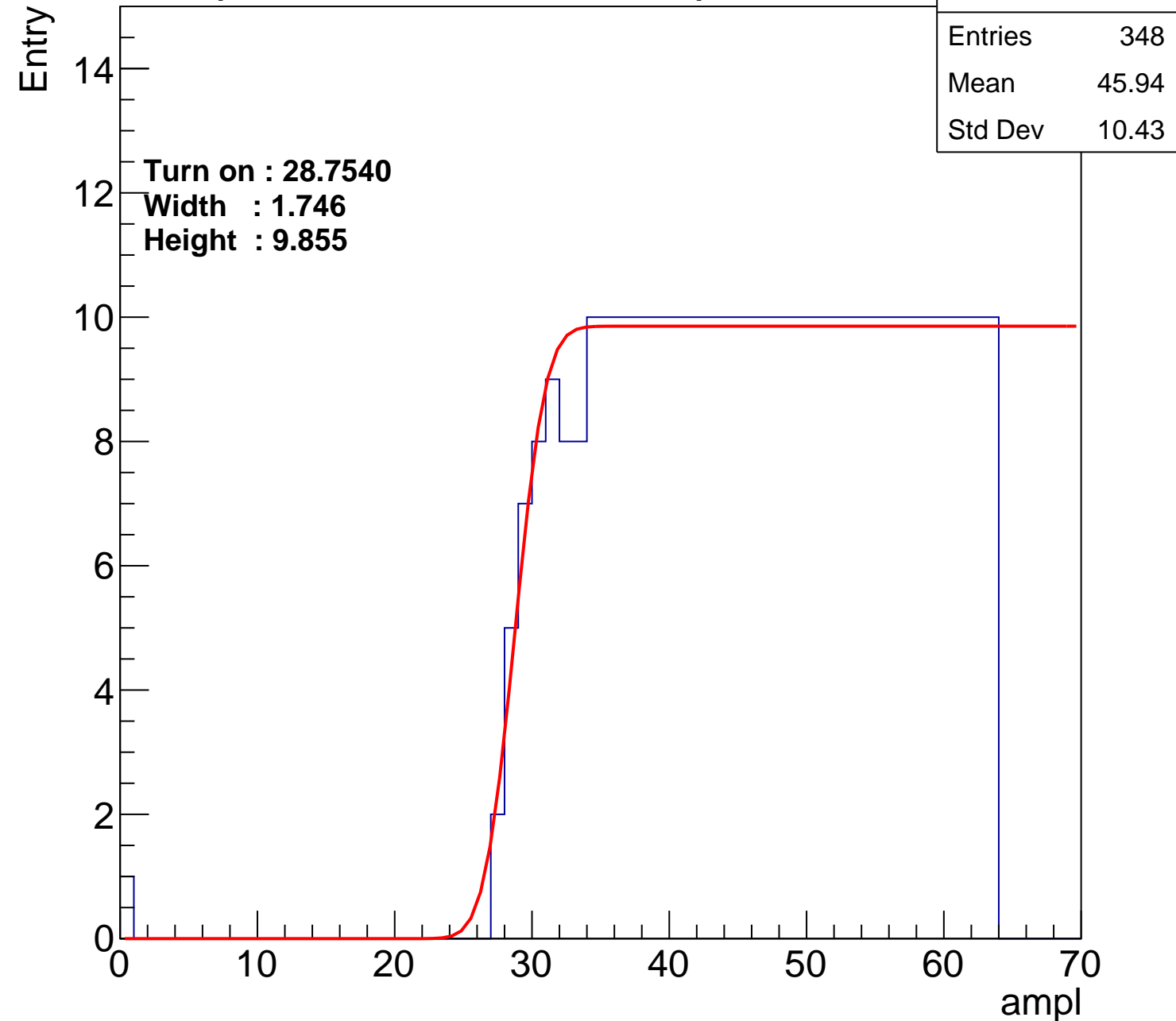
Width : 1.746

Height : 9.855

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch34

calib_packv5_042523_0143.root, FC#0, port D2

Entries	361
Mean	45.09
Std Dev	11.3

Turn on : 28.6993

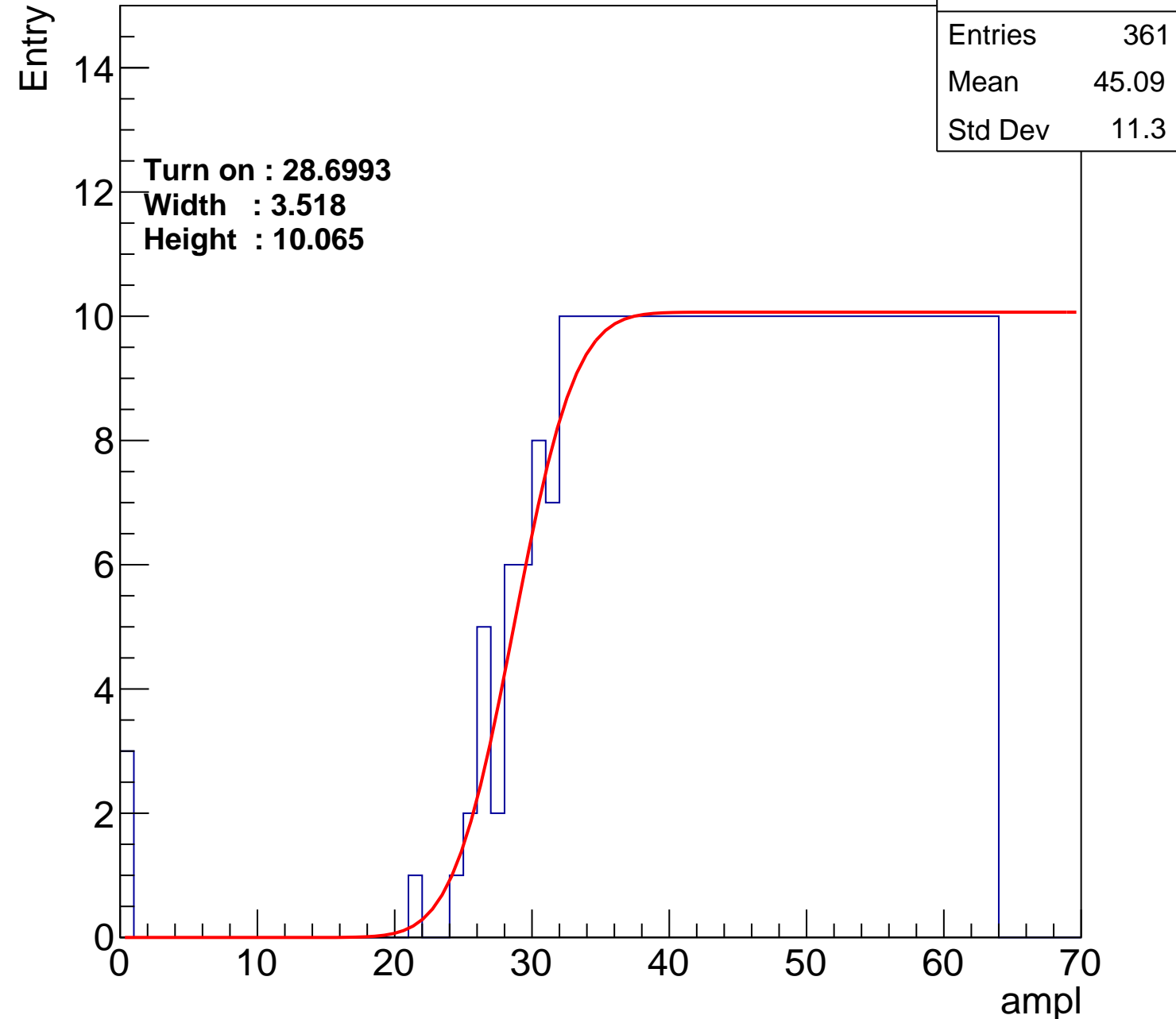
Width : 3.518

Height : 10.065

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch35

calib_packv5_042523_0143.root, FC#0, port D2

Entries	371
Mean	44.57
Std Dev	11.66

Turn on : 27.6131

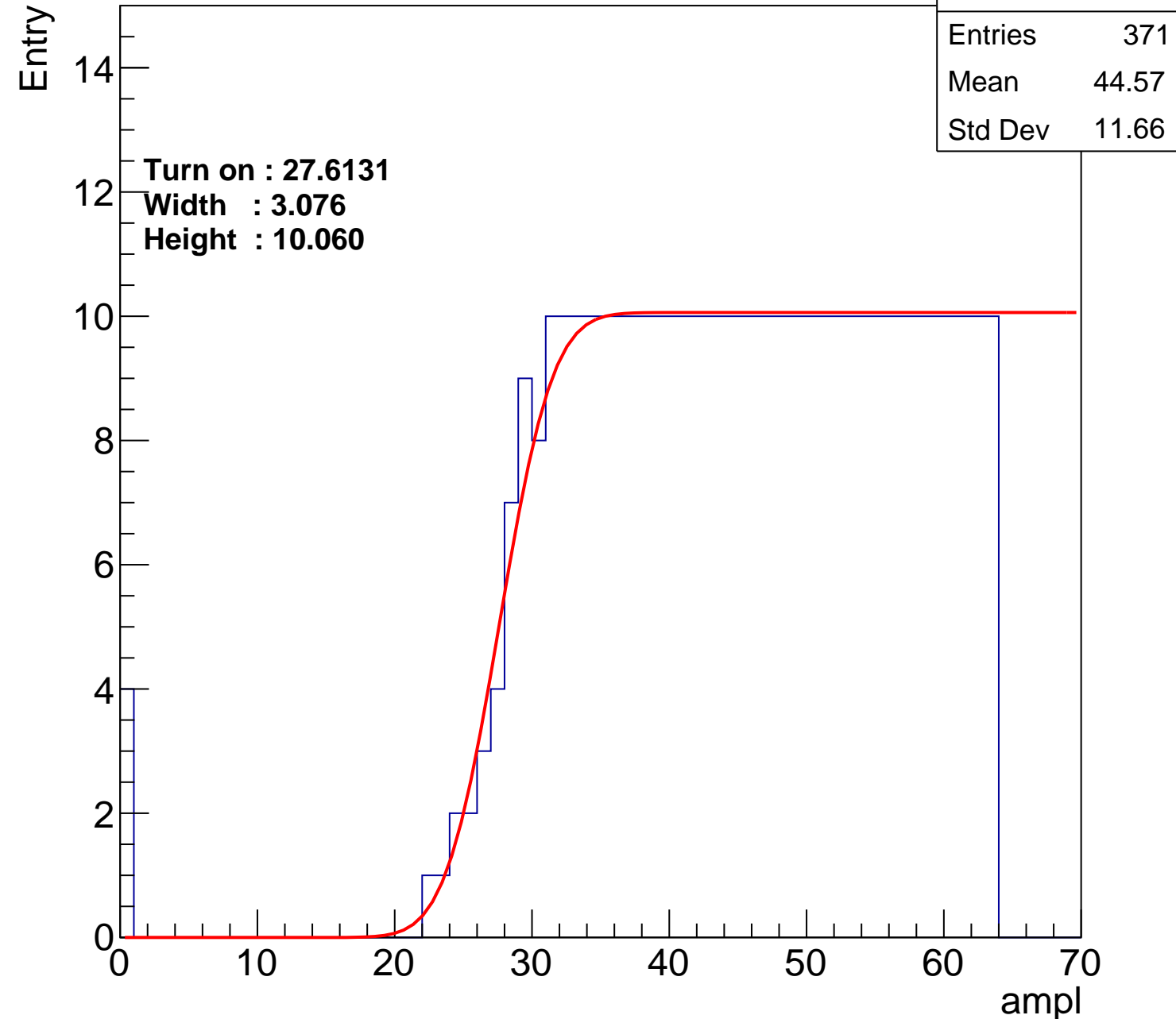
Width : 3.076

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch36

calib_packv5_042523_0143.root, FC#0, port D2

Entries	362
Mean	45.13
Std Dev	11.1

Turn on : 28.5351

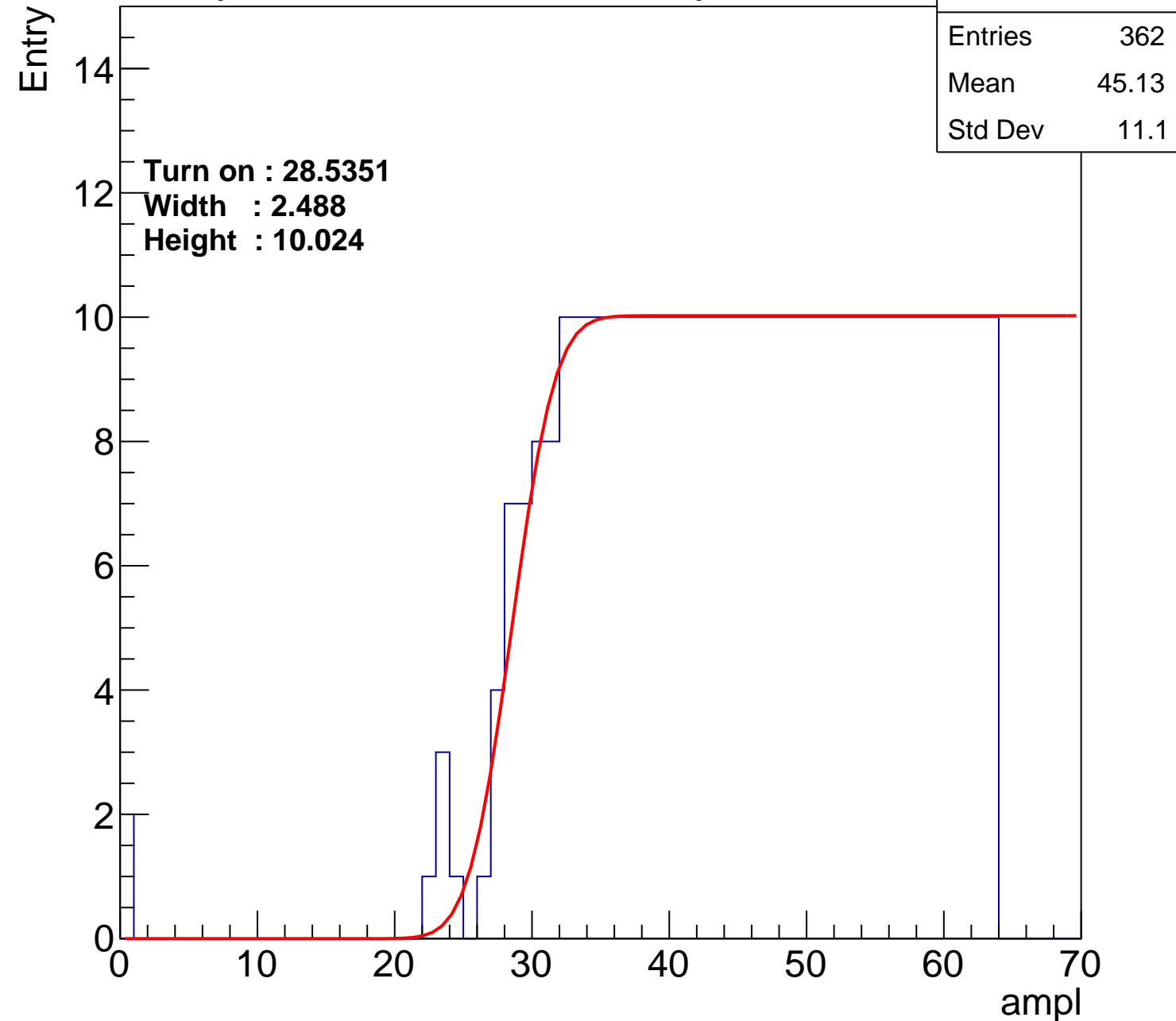
Width : 2.488

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch37

calib_packv5_042523_0143.root, FC#0, port D2

Entries	381
Mean	44.23
Std Dev	11.52

Turn on : 26.4351

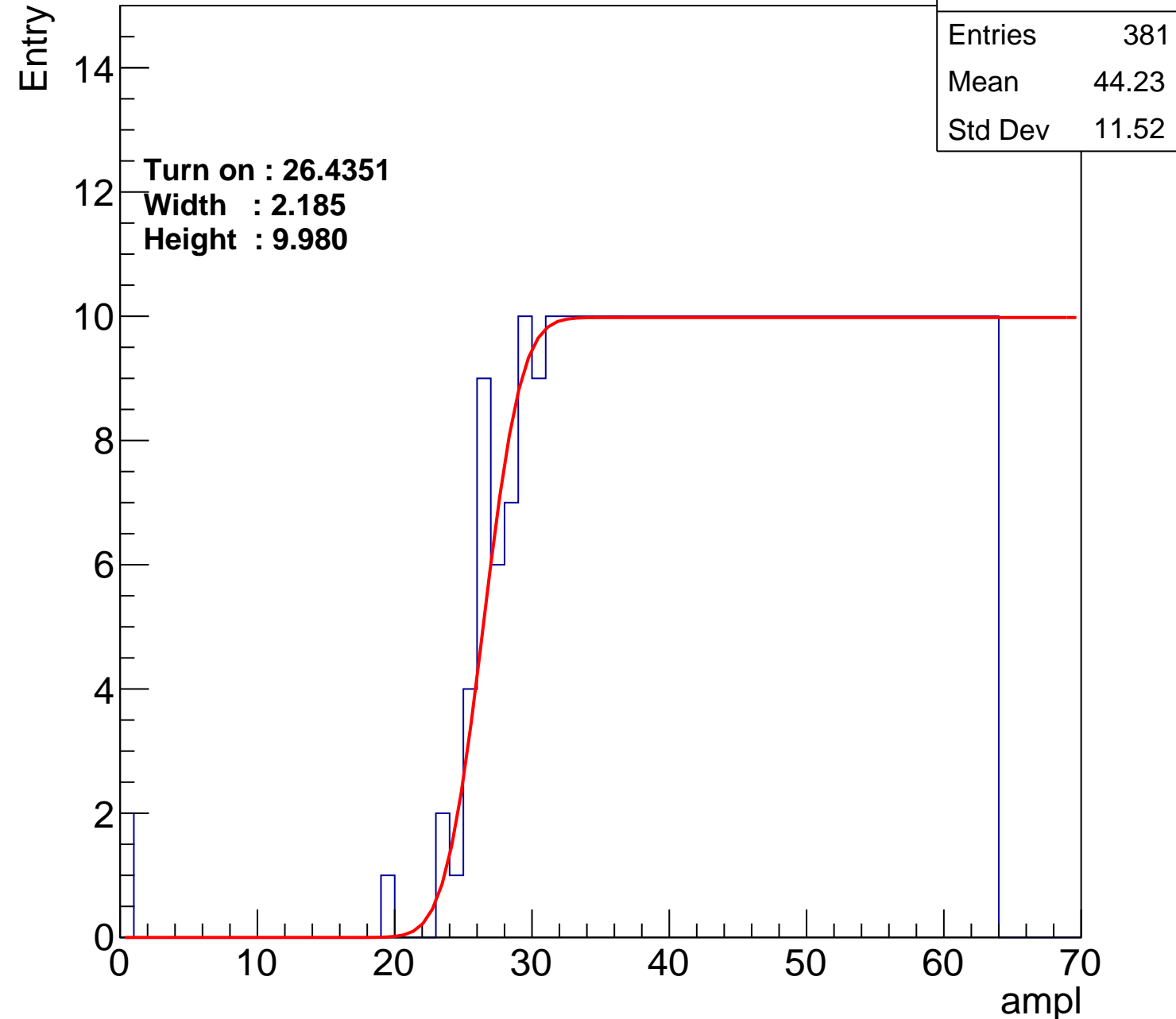
Width : 2.185

Height : 9.980

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch38

calib_packv5_042523_0143.root, FC#0, port D2

Entries	366
Mean	44.75
Std Dev	11.73

Turn on : 28.0573

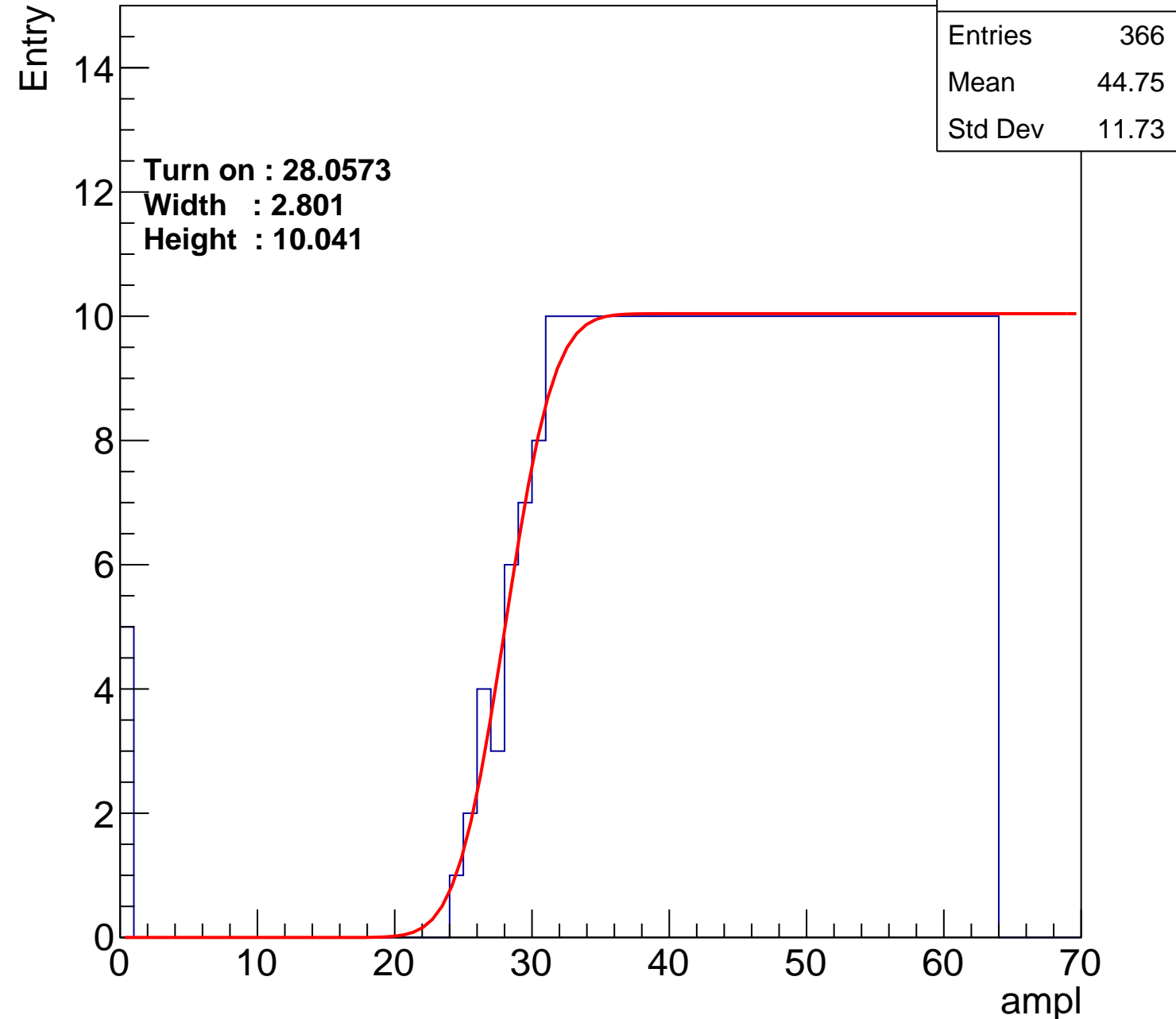
Width : 2.801

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch39

calib_packv5_042523_0143.root, FC#0, port D2

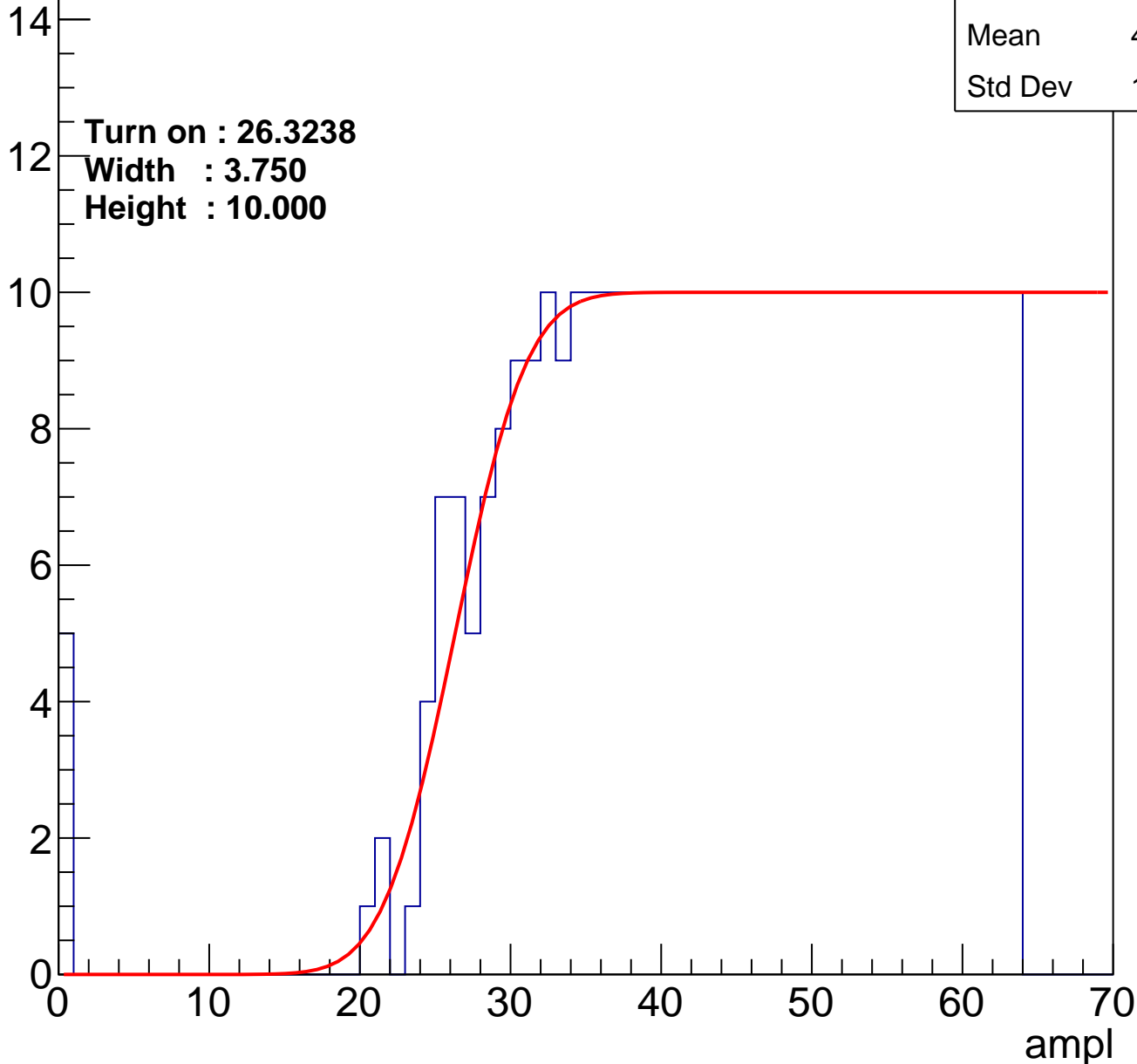
Entries	384
Mean	43.79
Std Dev	12.24

Turn on : 26.3238

Width : 3.750

Height : 10.000

Entry



B1L101S, U24-ch40

calib_packv5_042523_0143.root, FC#0, port D2

Entries	361
Mean	45.05
Std Dev	11.44

Turn on : 28.2007

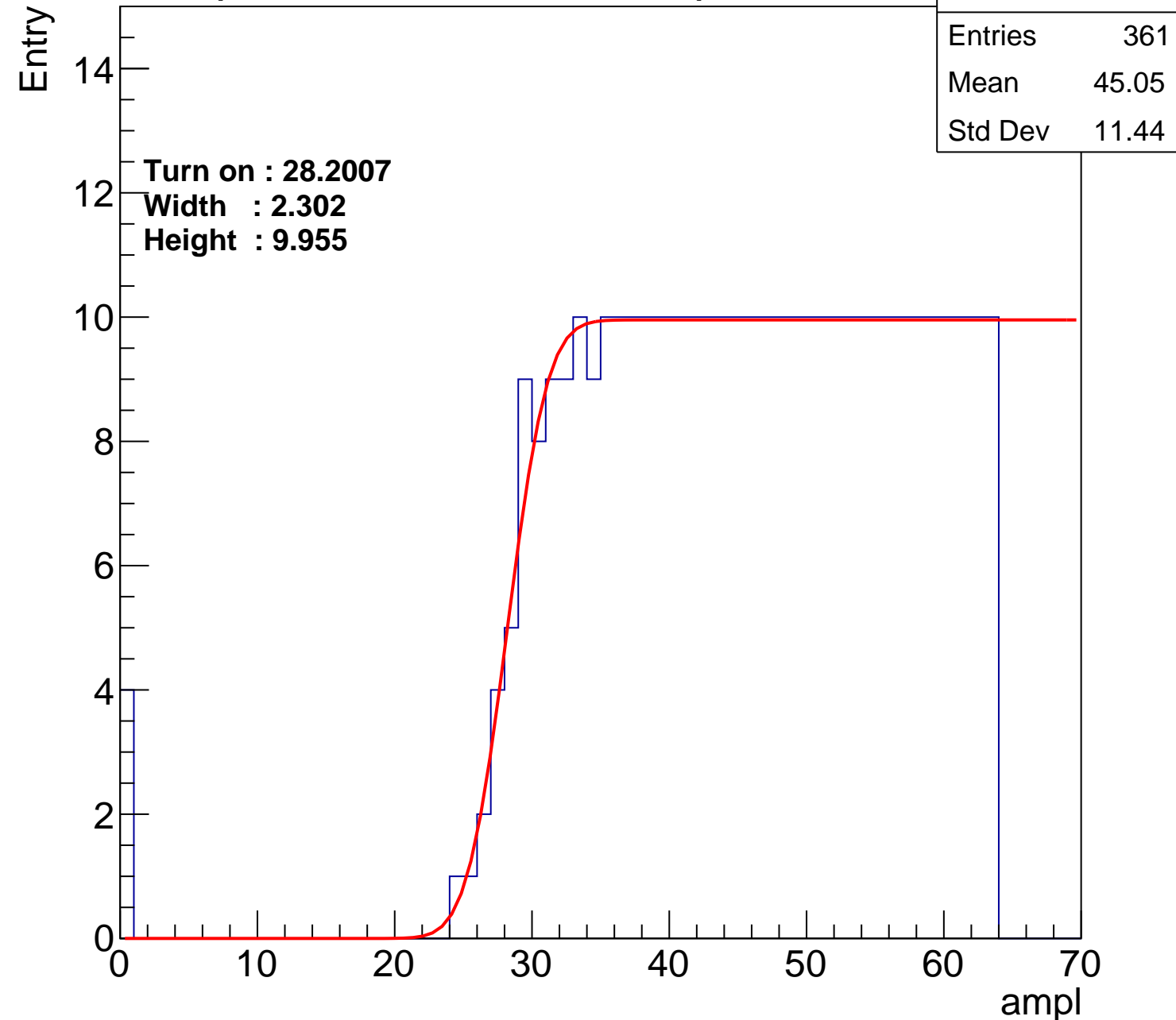
Width : 2.302

Height : 9.955

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch41

calib_packv5_042523_0143.root, FC#0, port D2

Entries	380
Mean	44.29
Std Dev	11.48

Turn on : 26.5961

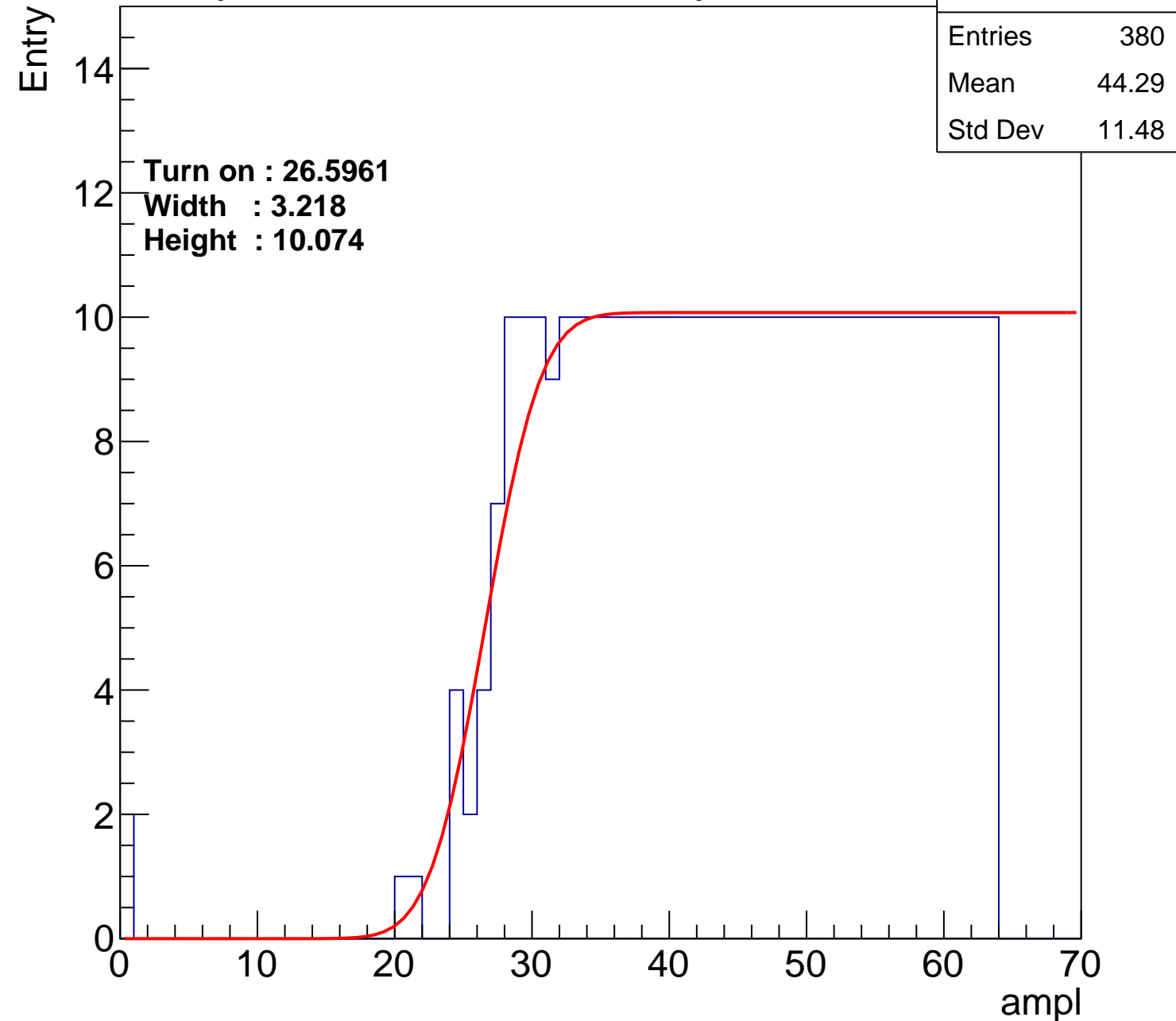
Width : 3.218

Height : 10.074

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch42

calib_packv5_042523_0143.root, FC#0, port D2

Entries	382
Mean	44.2
Std Dev	11.51

Turn on : 25.8761

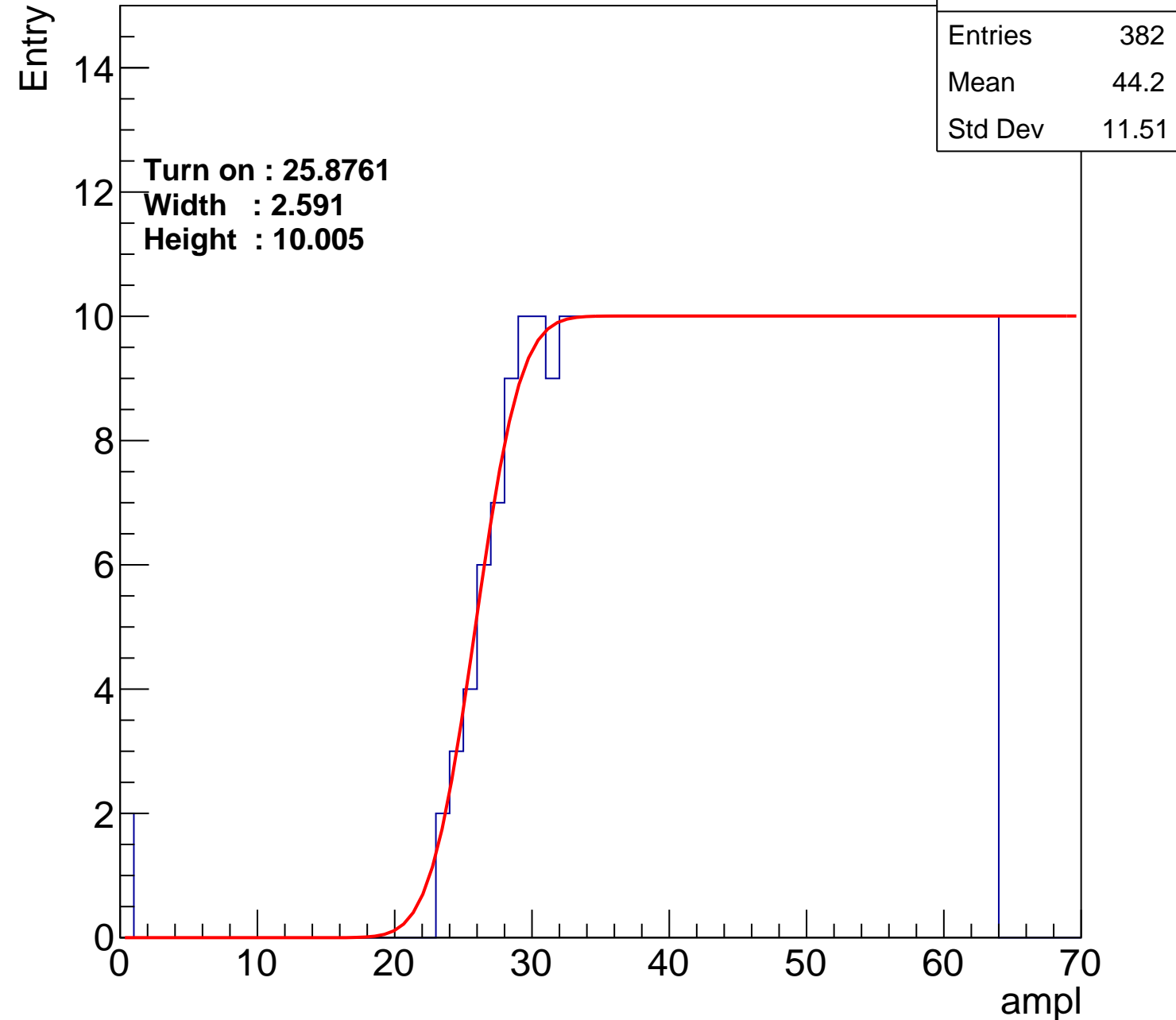
Width : 2.591

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch43

calib_packv5_042523_0143.root, FC#0, port D2

Entries	354
Mean	45.51
Std Dev	10.91

Turn on : 29.5091

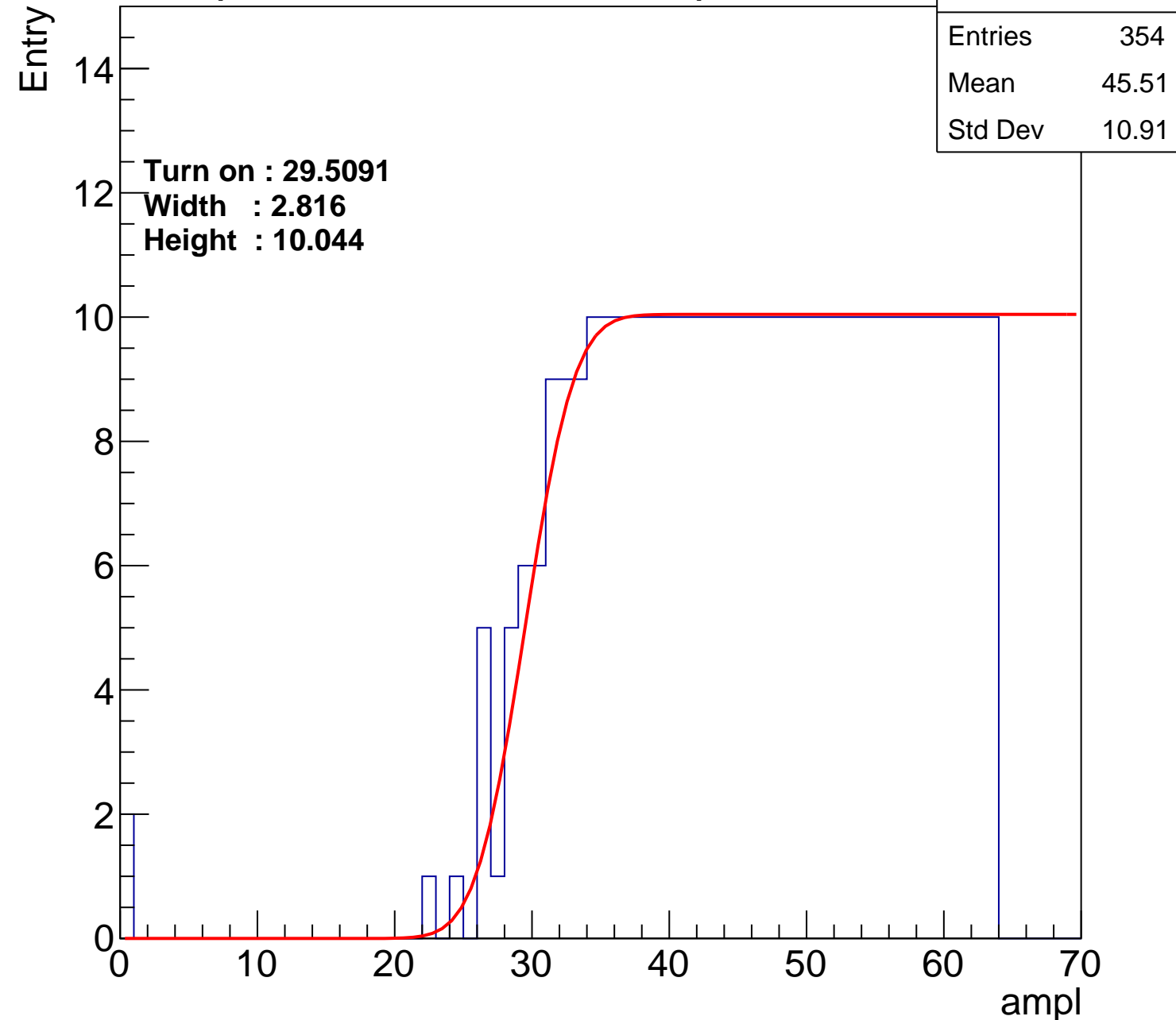
Width : 2.816

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch44

calib_packv5_042523_0143.root, FC#0, port D2

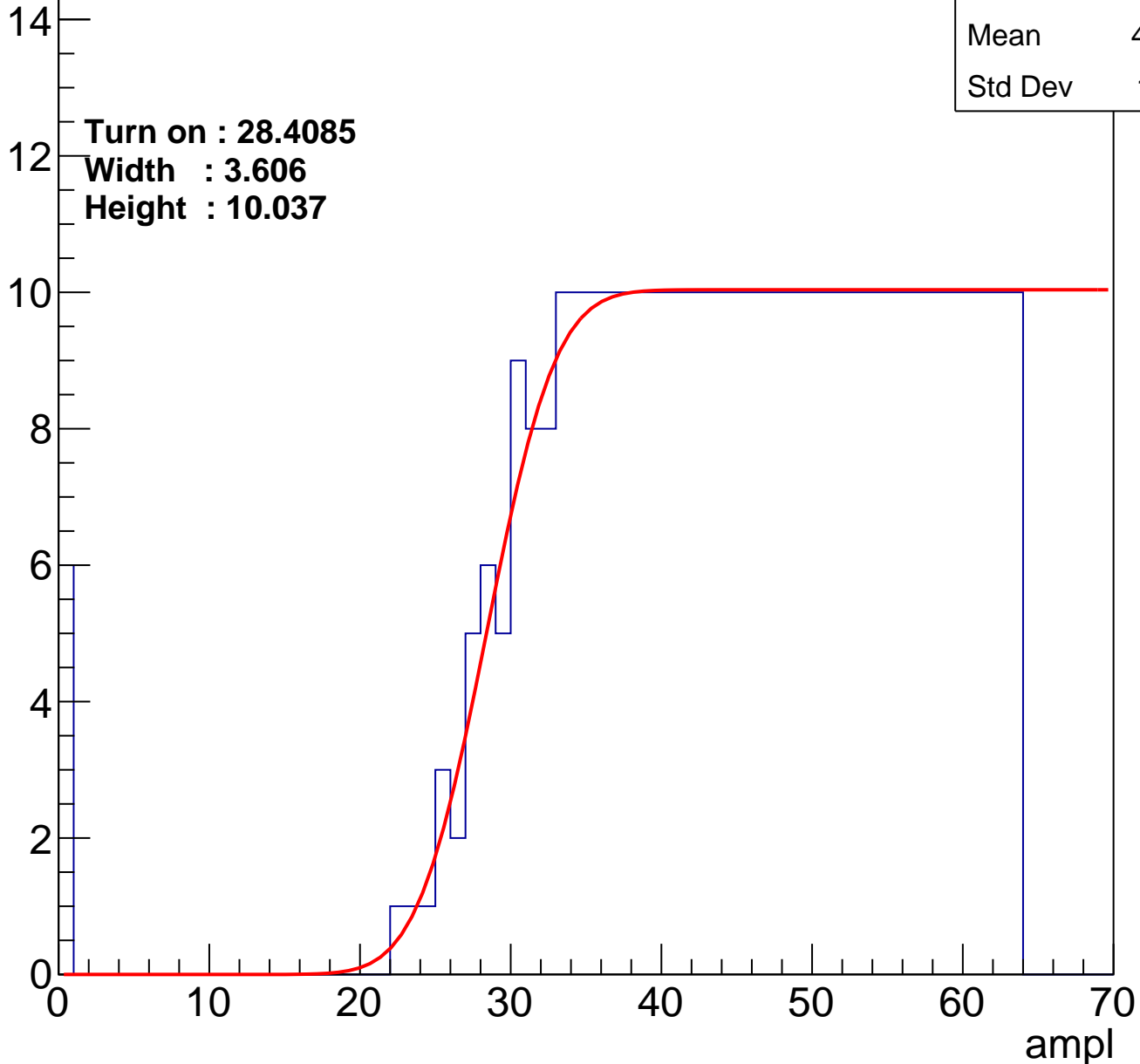
Entries	365
Mean	44.65
Std Dev	12.01

Turn on : 28.4085

Width : 3.606

Height : 10.037

Entry



B1L101S, U24-ch45

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.35
Std Dev	11.62

Turn on : 27.8831

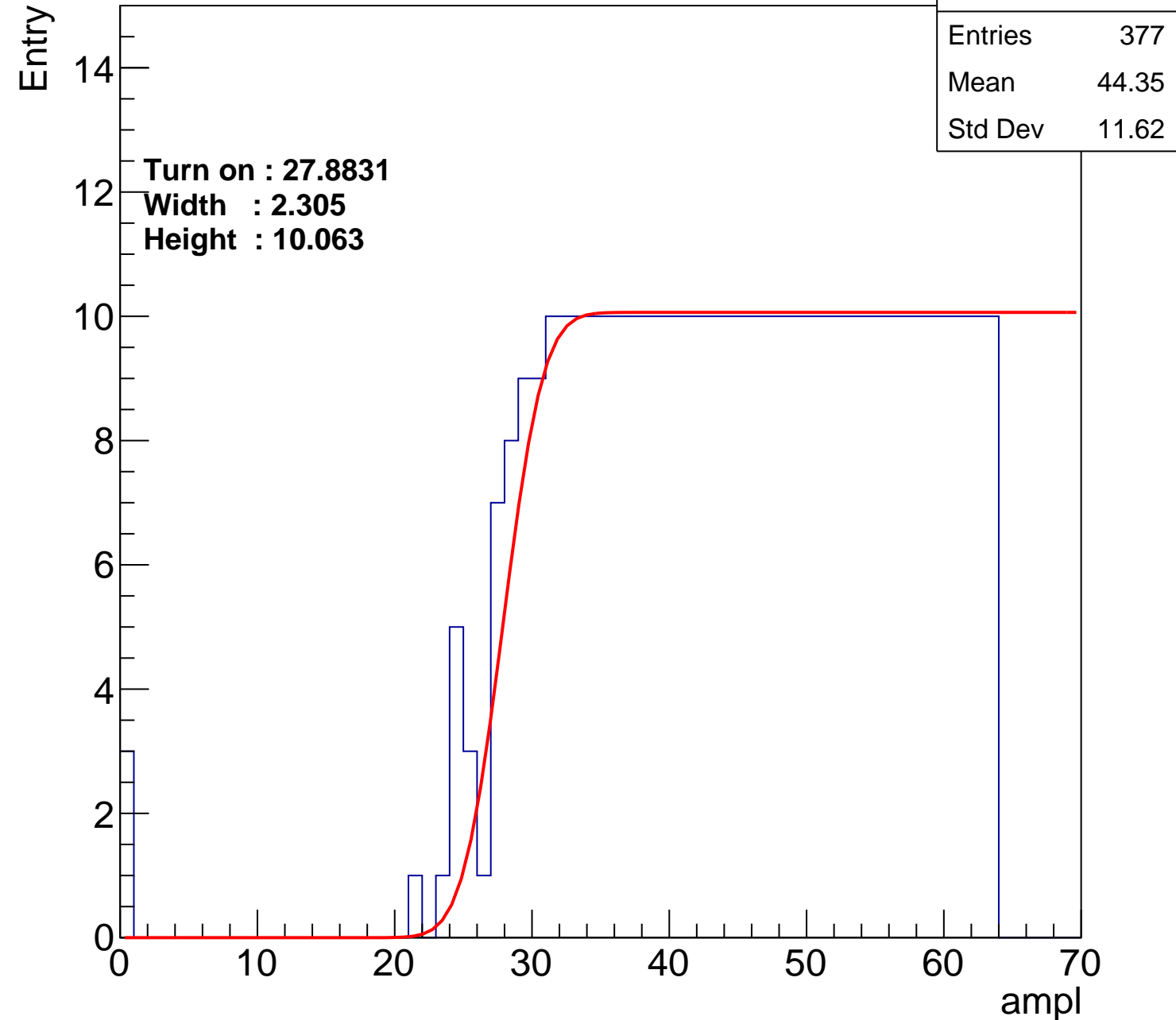
Width : 2.305

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch46

calib_packv5_042523_0143.root, FC#0, port D2

Entries	372
Mean	44.59
Std Dev	11.5

Turn on : 27.5878

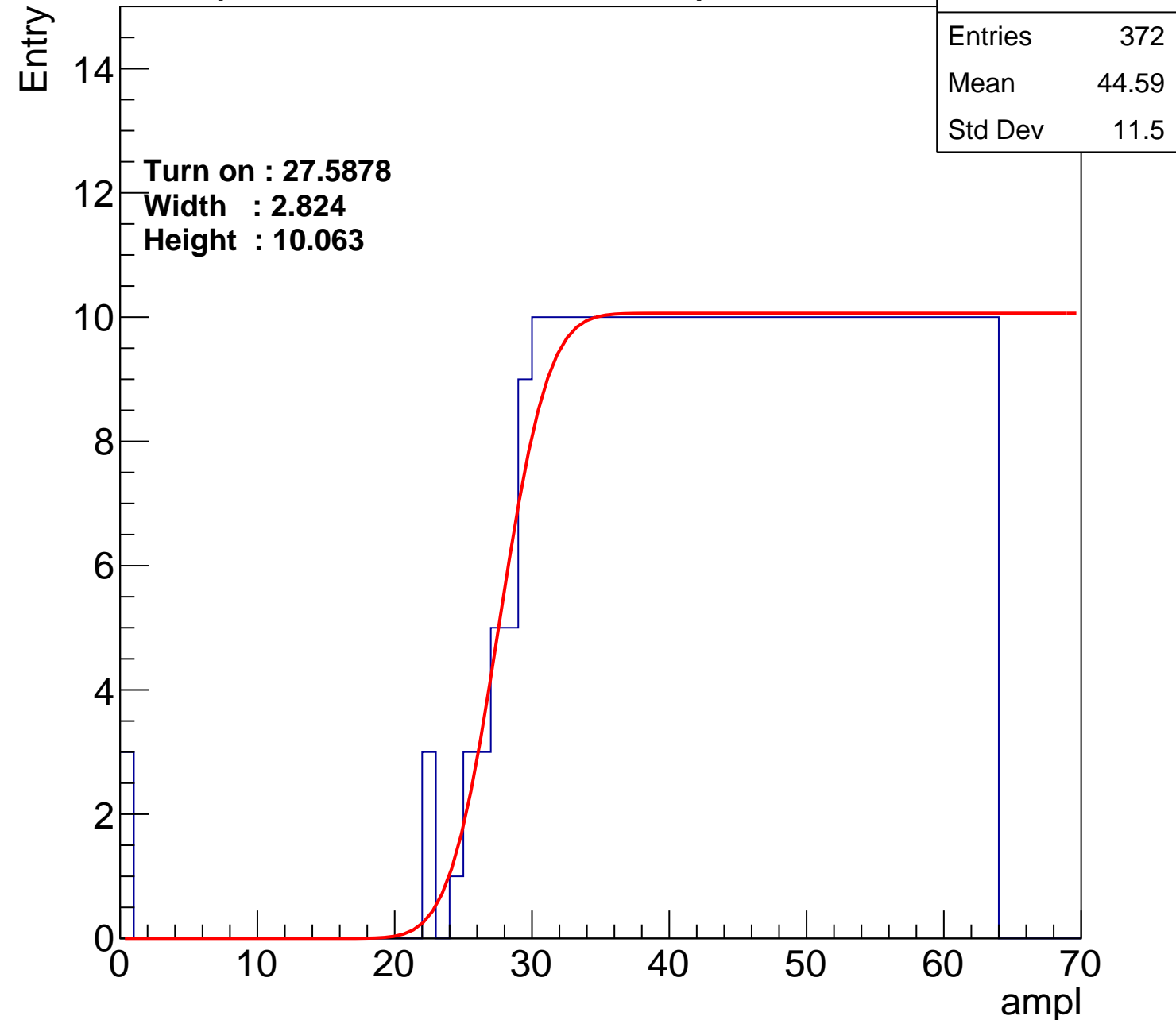
Width : 2.824

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch47

calib_packv5_042523_0143.root, FC#0, port D2

Entries	371
Mean	44.79
Std Dev	11.06

Turn on : 27.3347

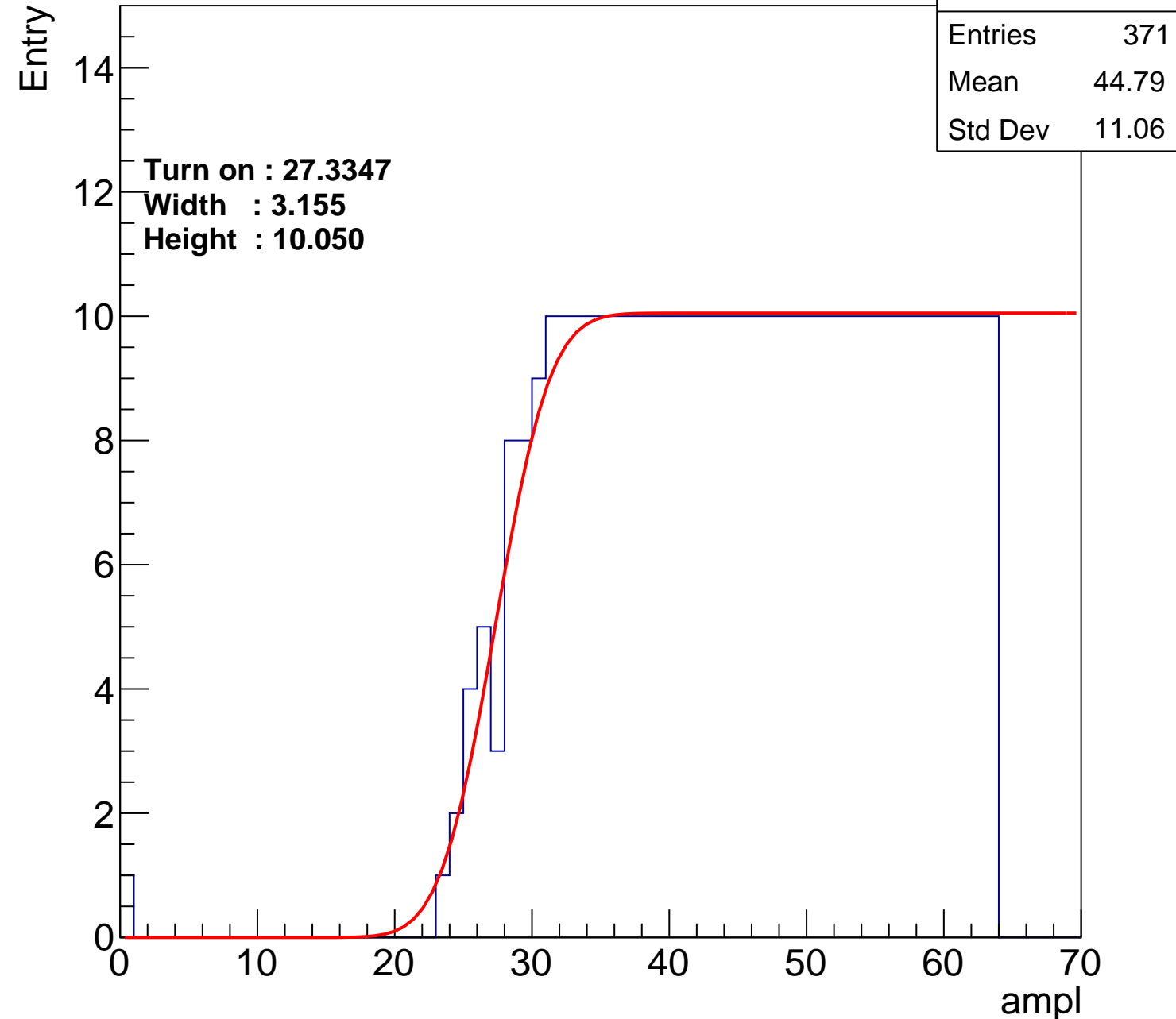
Width : 3.155

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch48

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.32
Std Dev	11.97

Turn on : 27.3884

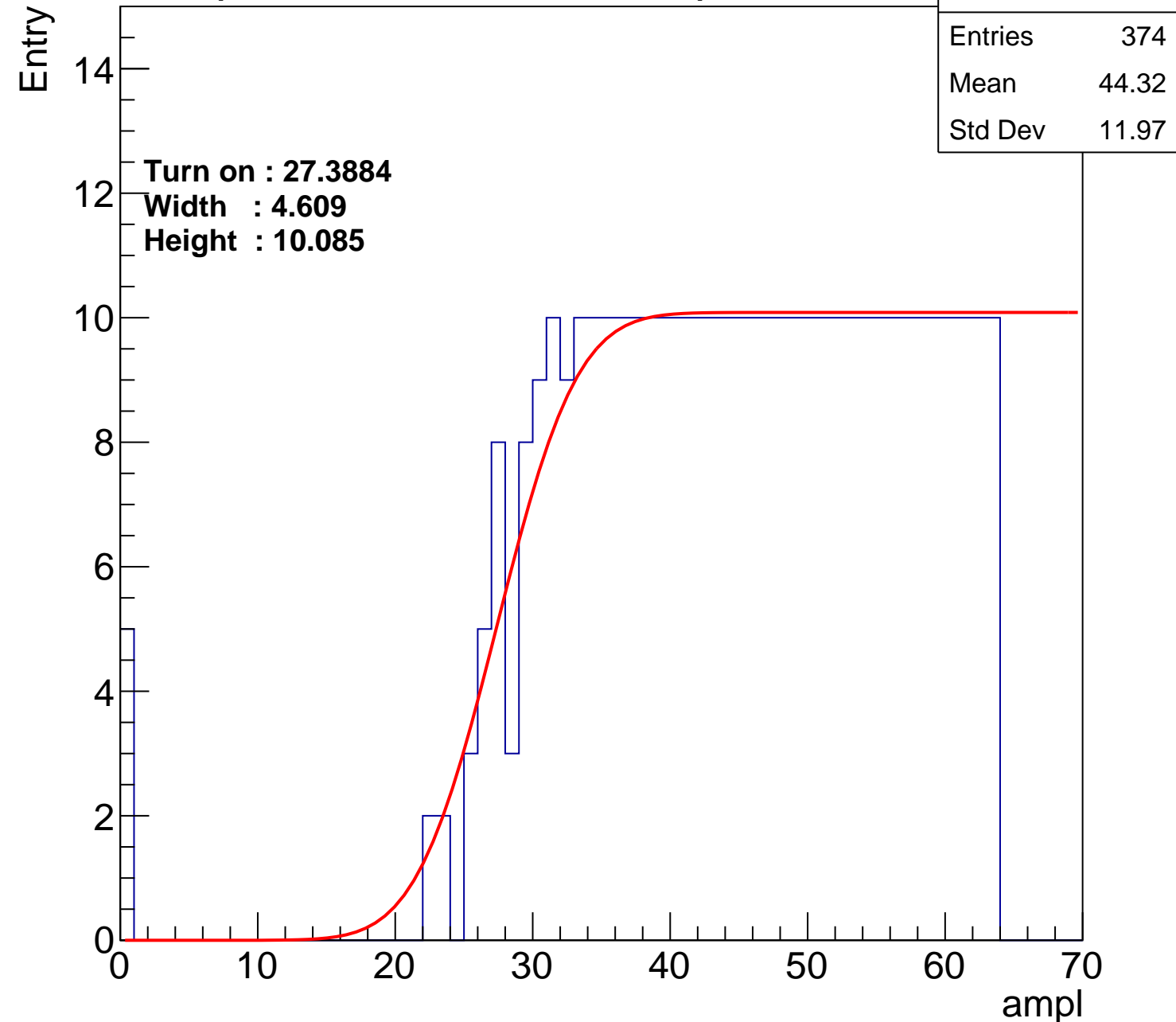
Width : 4.609

Height : 10.085

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch49

calib_packv5_042523_0143.root, FC#0, port D2

Entries	370
Mean	44.85
Std Dev	11.02

Turn on : 27.3271

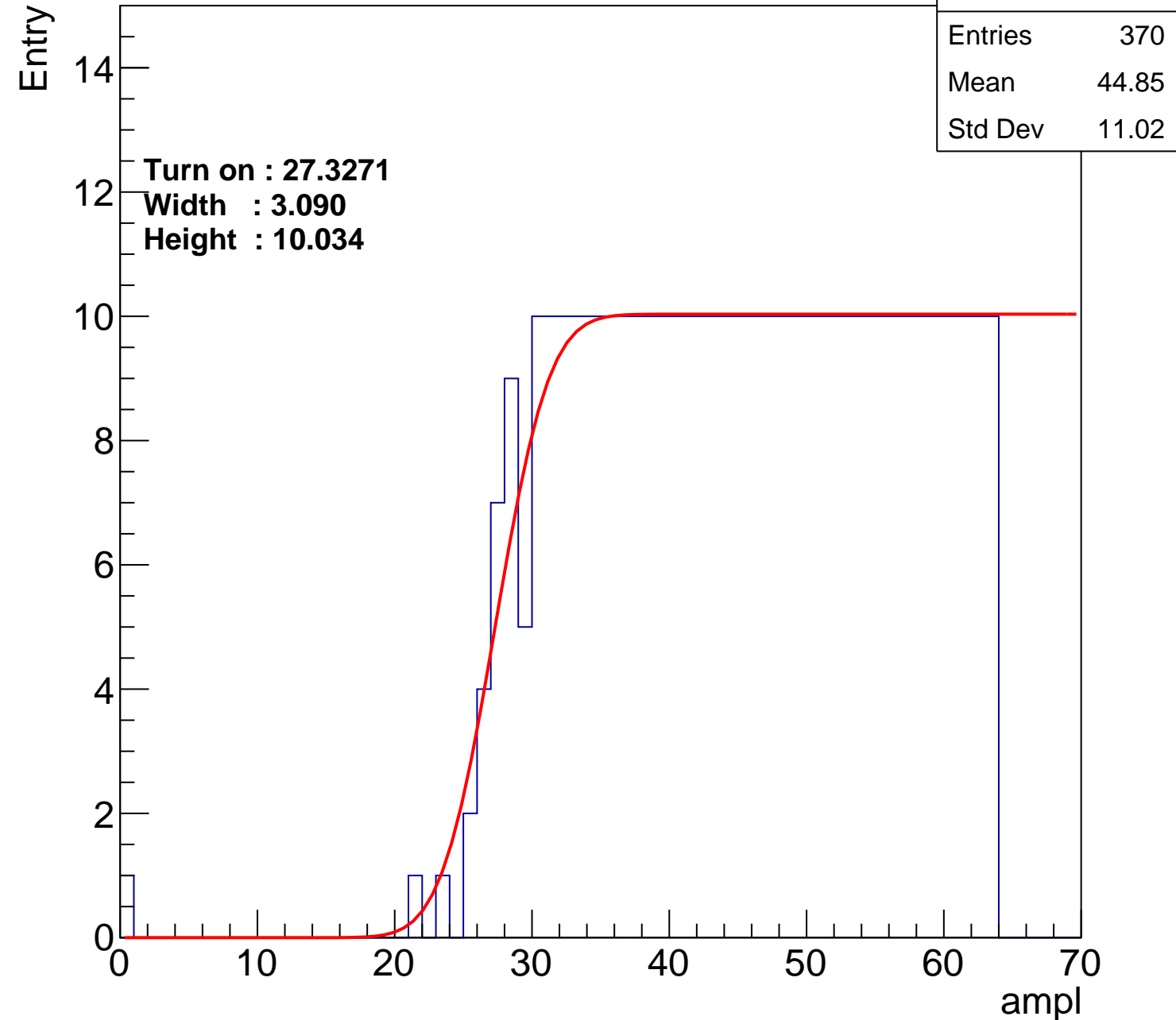
Width : 3.090

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch50

calib_packv5_042523_0143.root, FC#0, port D2

Entries	394
Mean	43.5
Std Dev	11.99

Turn on : 25.2517

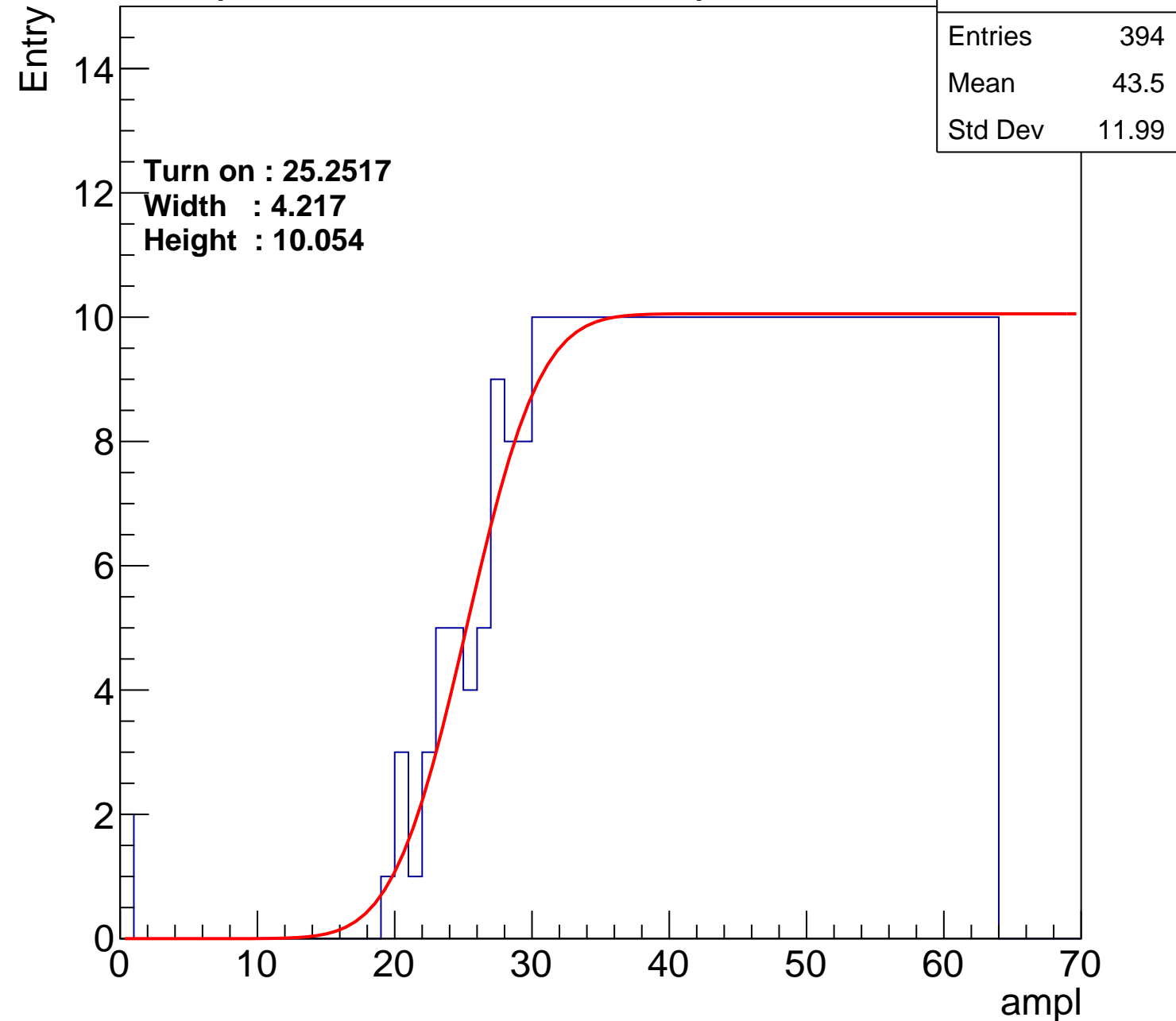
Width : 4.217

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch51

calib_packv5_042523_0143.root, FC#0, port D2

Entries	388
Mean	43.78
Std Dev	11.93

Turn on : 25.2021

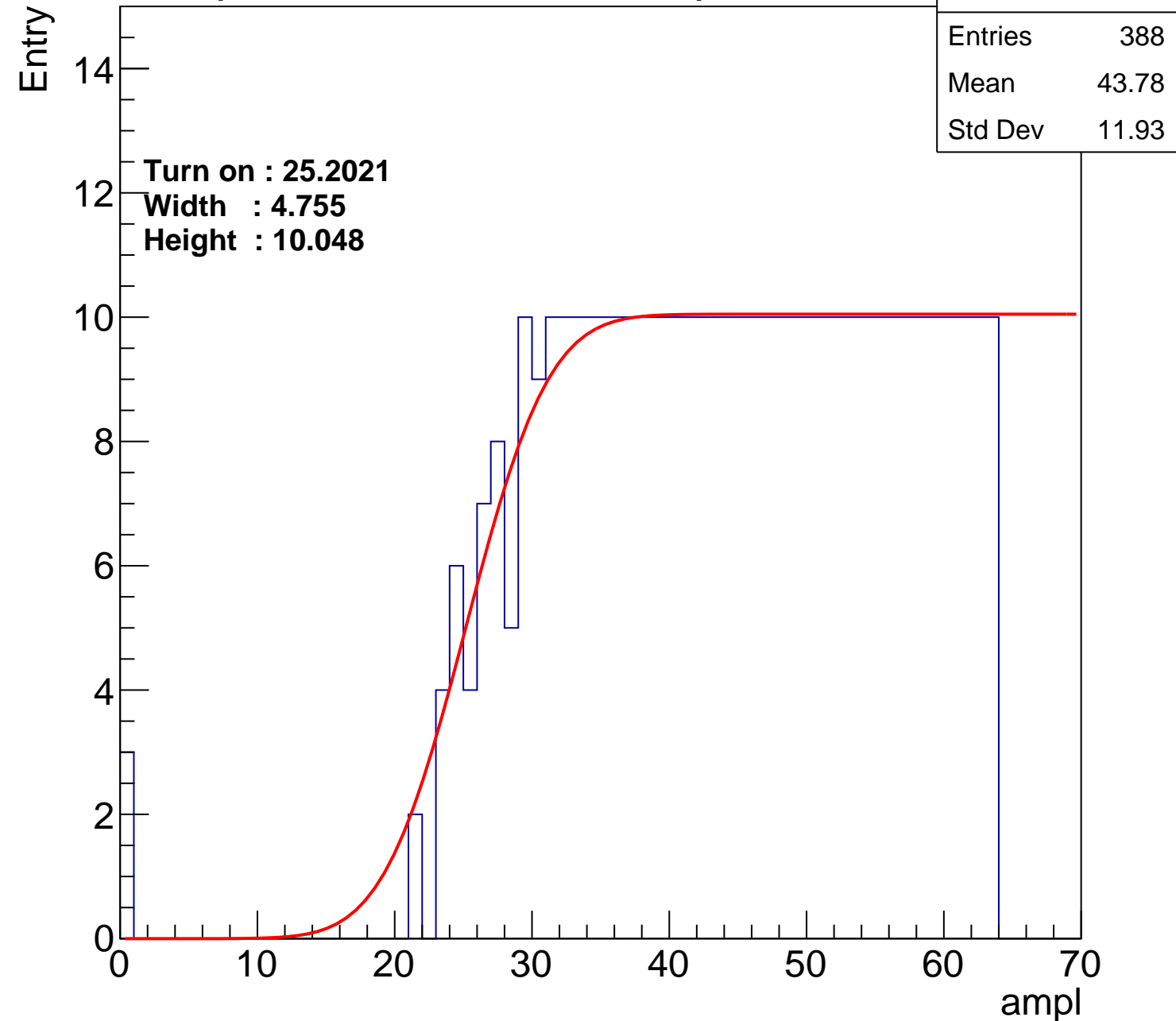
Width : 4.755

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch52

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.16
Std Dev	12.04

Turn on : 26.6639

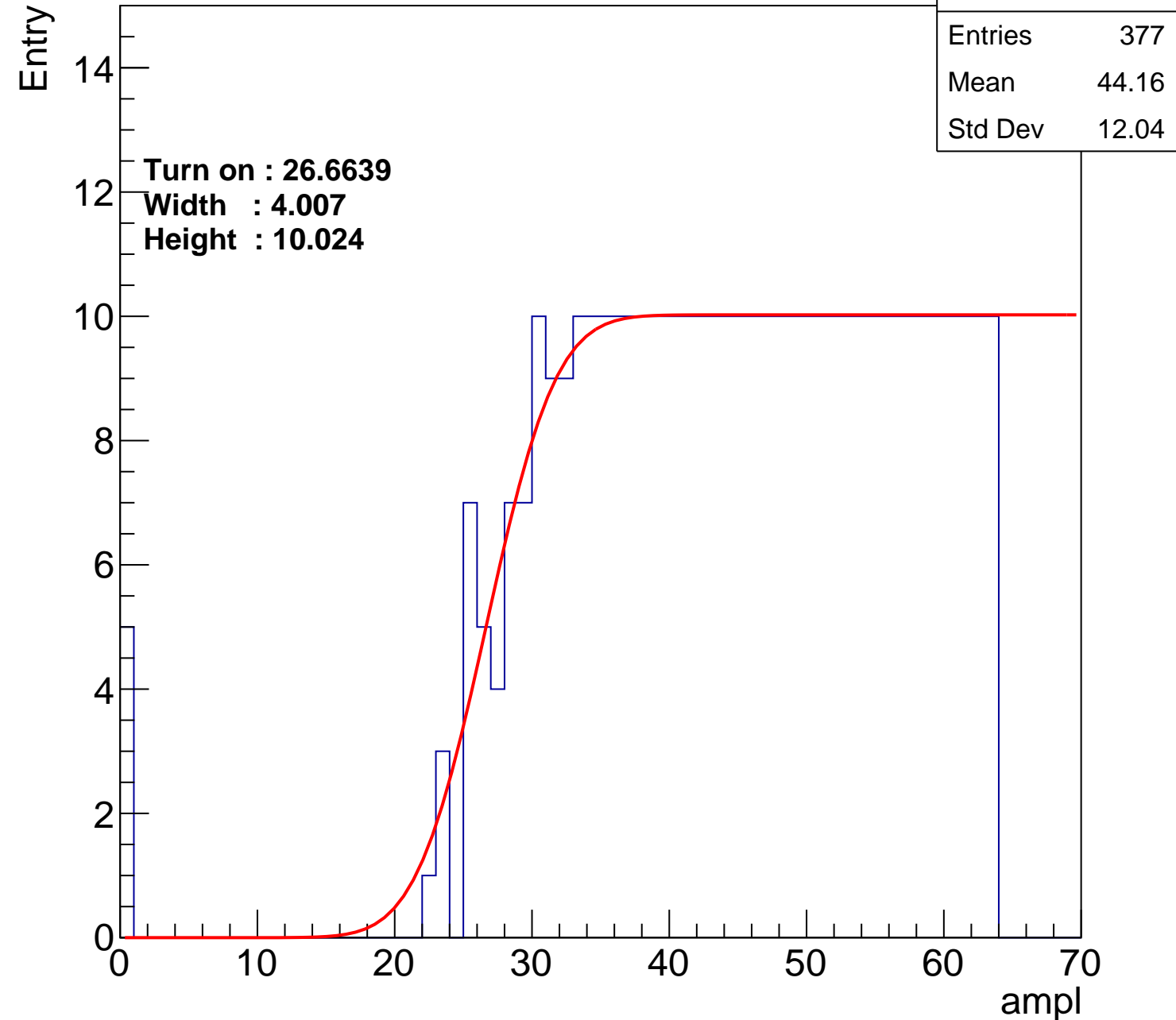
Width : 4.007

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch53

calib_packv5_042523_0143.root, FC#0, port D2

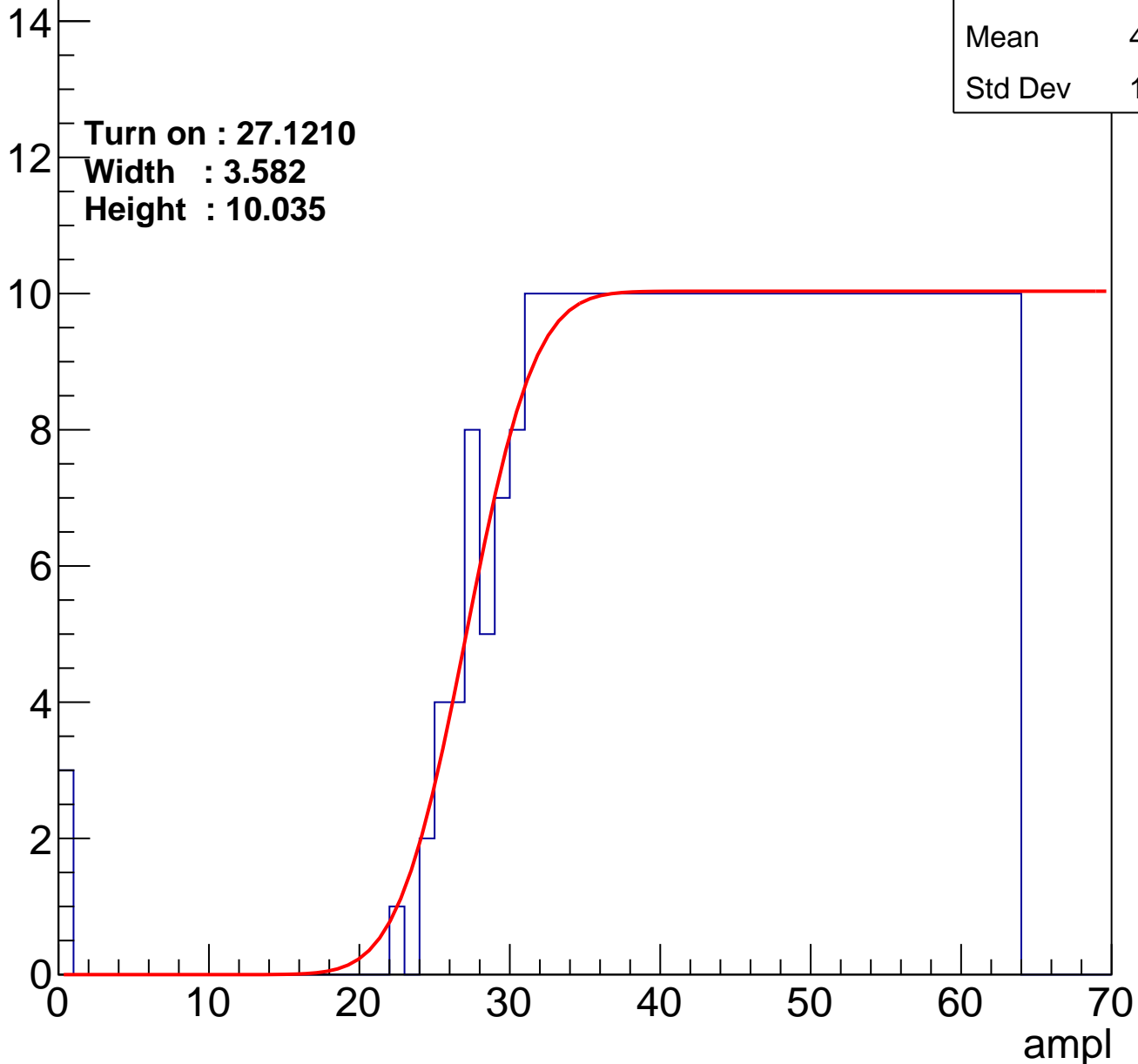
Entries	372
Mean	44.58
Std Dev	11.52

Turn on : 27.1210

Width : 3.582

Height : 10.035

Entry



B1L101S, U24-ch54

calib_packv5_042523_0143.root, FC#0, port D2

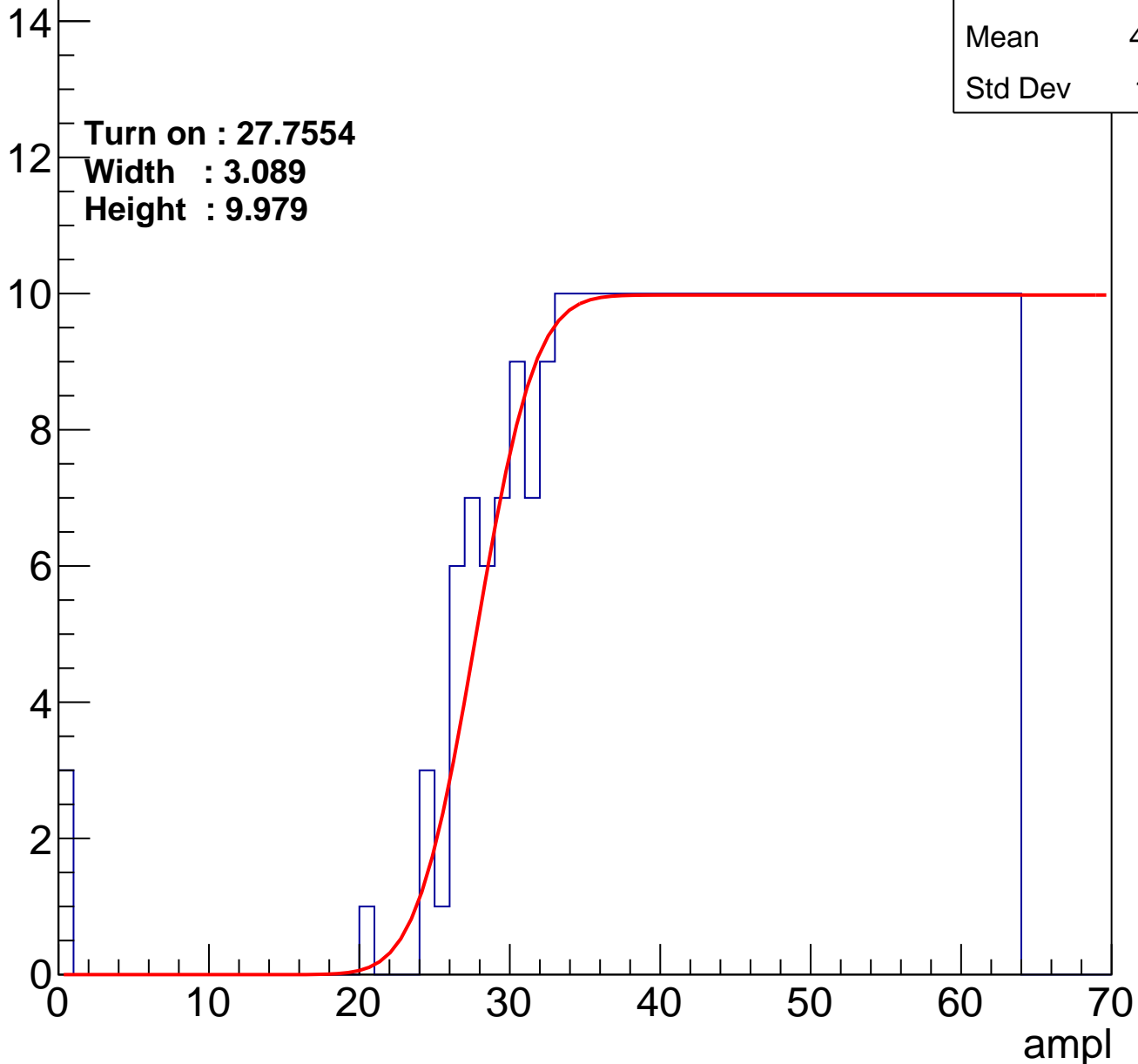
Entries	369
Mean	44.68
Std Dev	11.51

Turn on : 27.7554

Width : 3.089

Height : 9.979

Entry



B1L101S, U24-ch55

calib_packv5_042523_0143.root, FC#0, port D2

Entries	351
Mean	45.75
Std Dev	10.57

Turn on : 28.7160

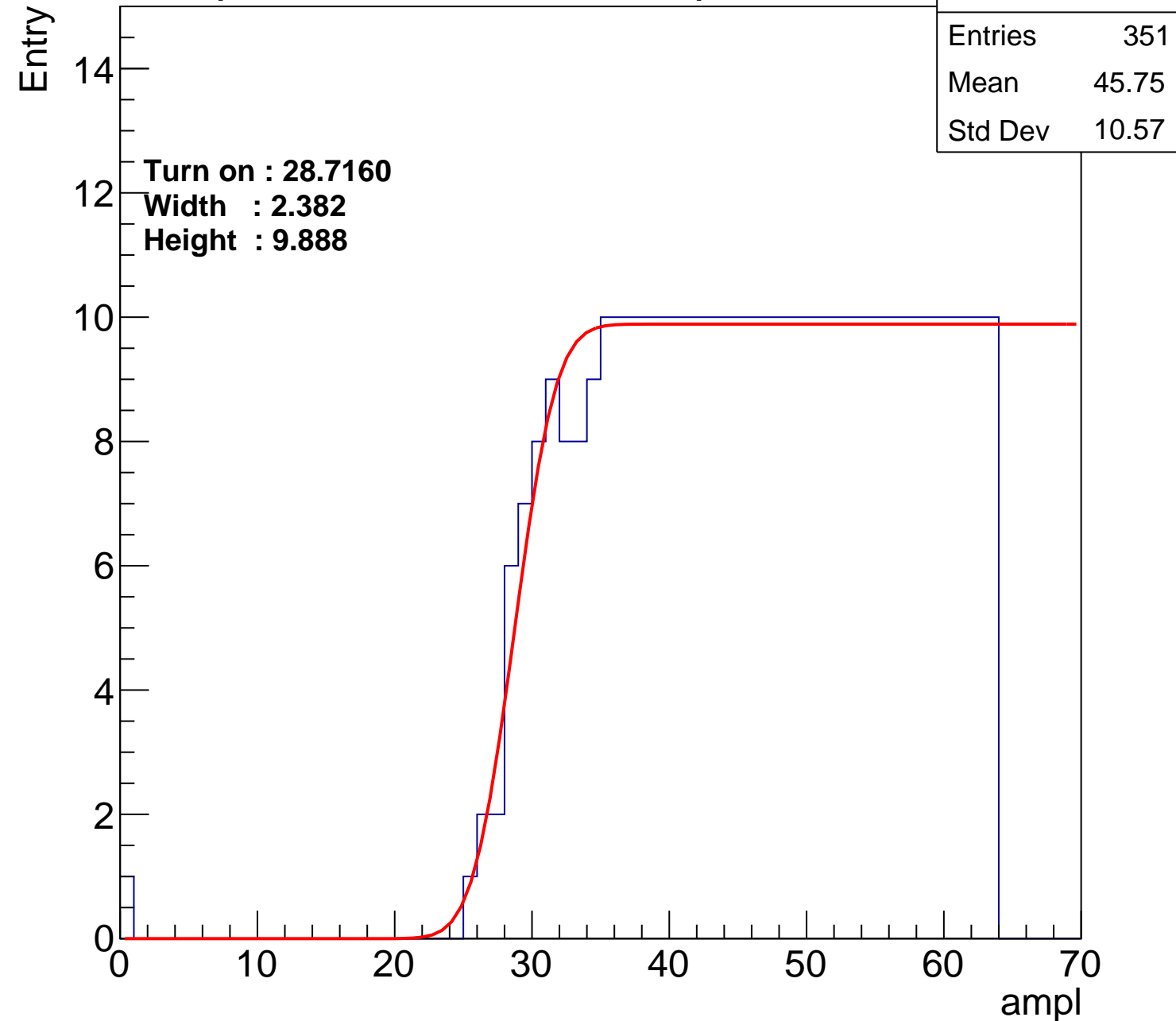
Width : 2.382

Height : 9.888

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch56

calib_packv5_042523_0143.root, FC#0, port D2

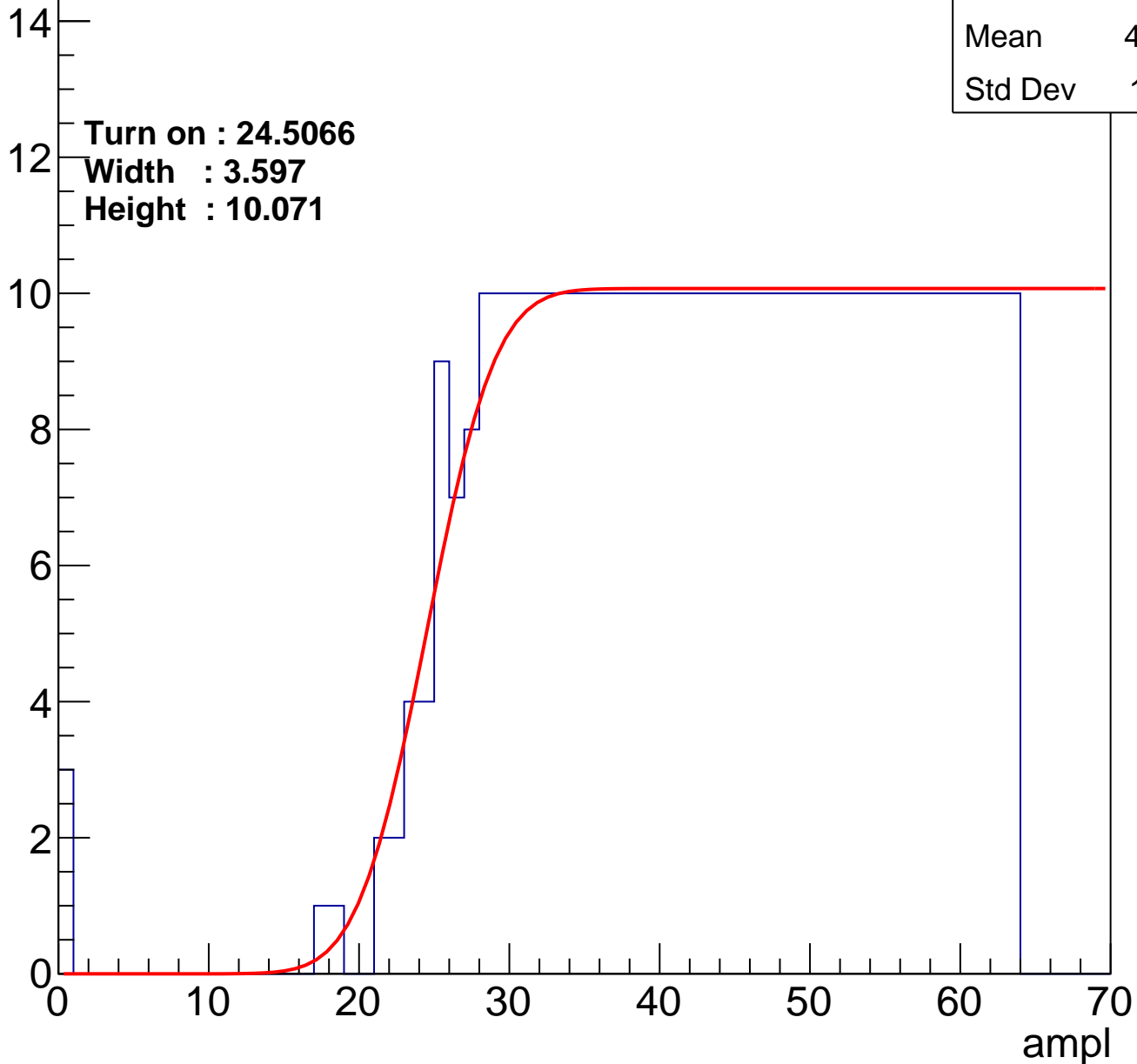
Entries	401
Mean	43.17
Std Dev	12.21

Turn on : 24.5066

Width : 3.597

Height : 10.071

Entry



B1L101S, U24-ch57

calib_packv5_042523_0143.root, FC#0, port D2

Entries	380
Mean	44.26
Std Dev	11.44

Turn on : 26.0119

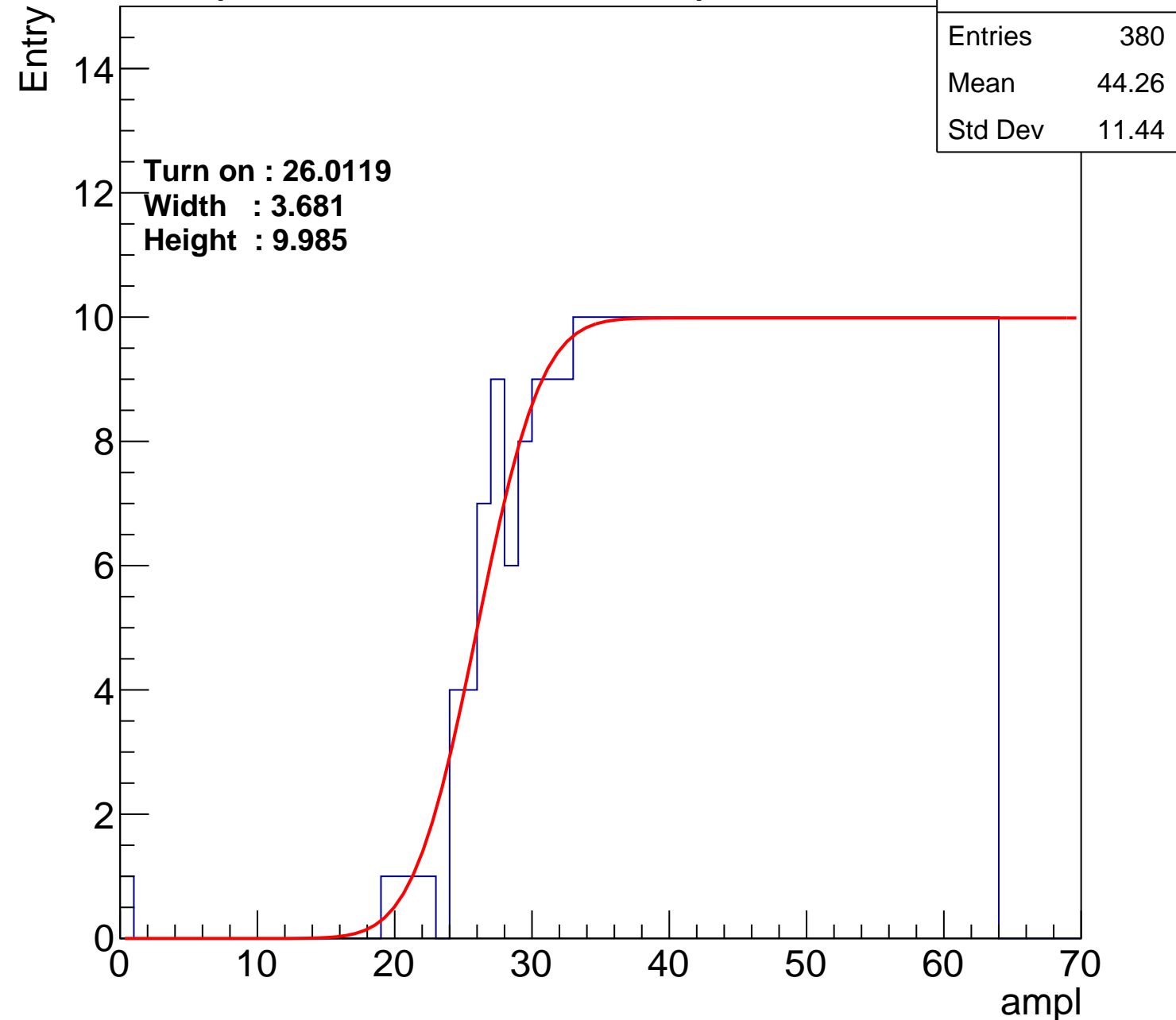
Width : 3.681

Height : 9.985

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch58

calib_packv5_042523_0143.root, FC#0, port D2

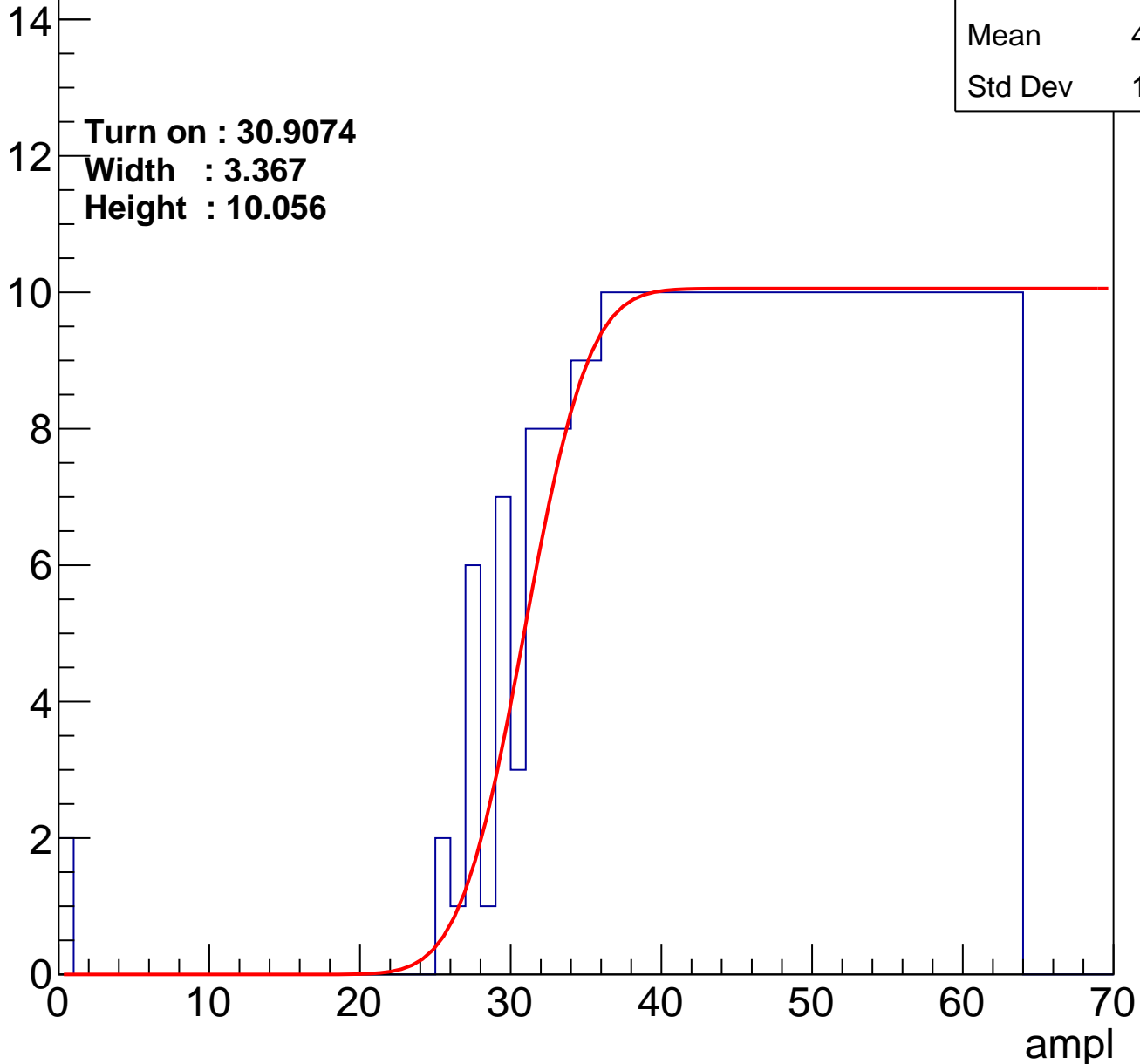
Entries	344
Mean	45.95
Std Dev	10.73

Turn on : 30.9074

Width : 3.367

Height : 10.056

Entry



B1L101S, U24-ch59

calib_packv5_042523_0143.root, FC#0, port D2

Entries	355
Mean	45.39
Std Dev	11.14

Turn on : 29.5607

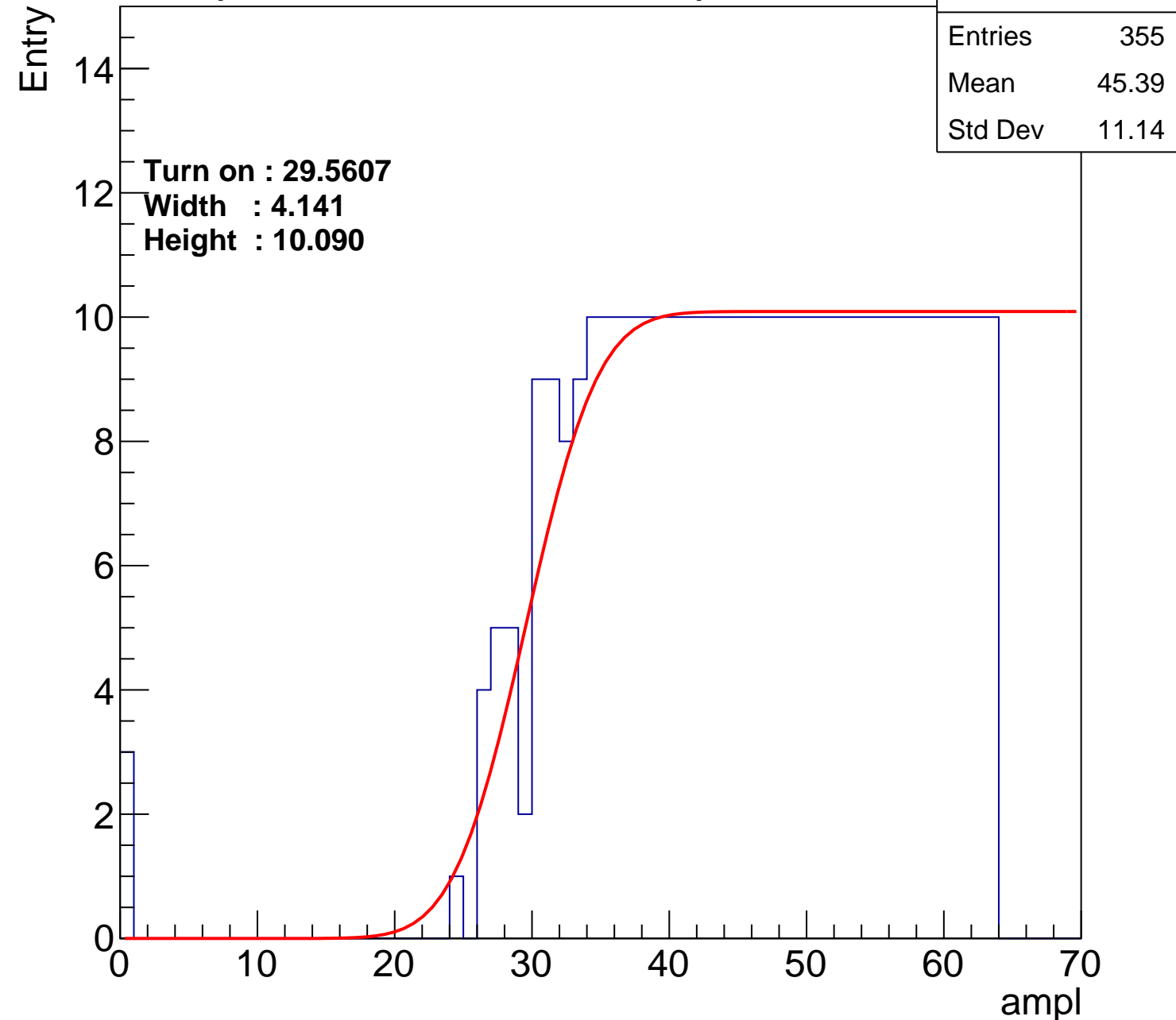
Width : 4.141

Height : 10.090

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch60

calib_packv5_042523_0143.root, FC#0, port D2

Entries	358
Mean	45.24
Std Dev	11.21

Turn on : 28.5876

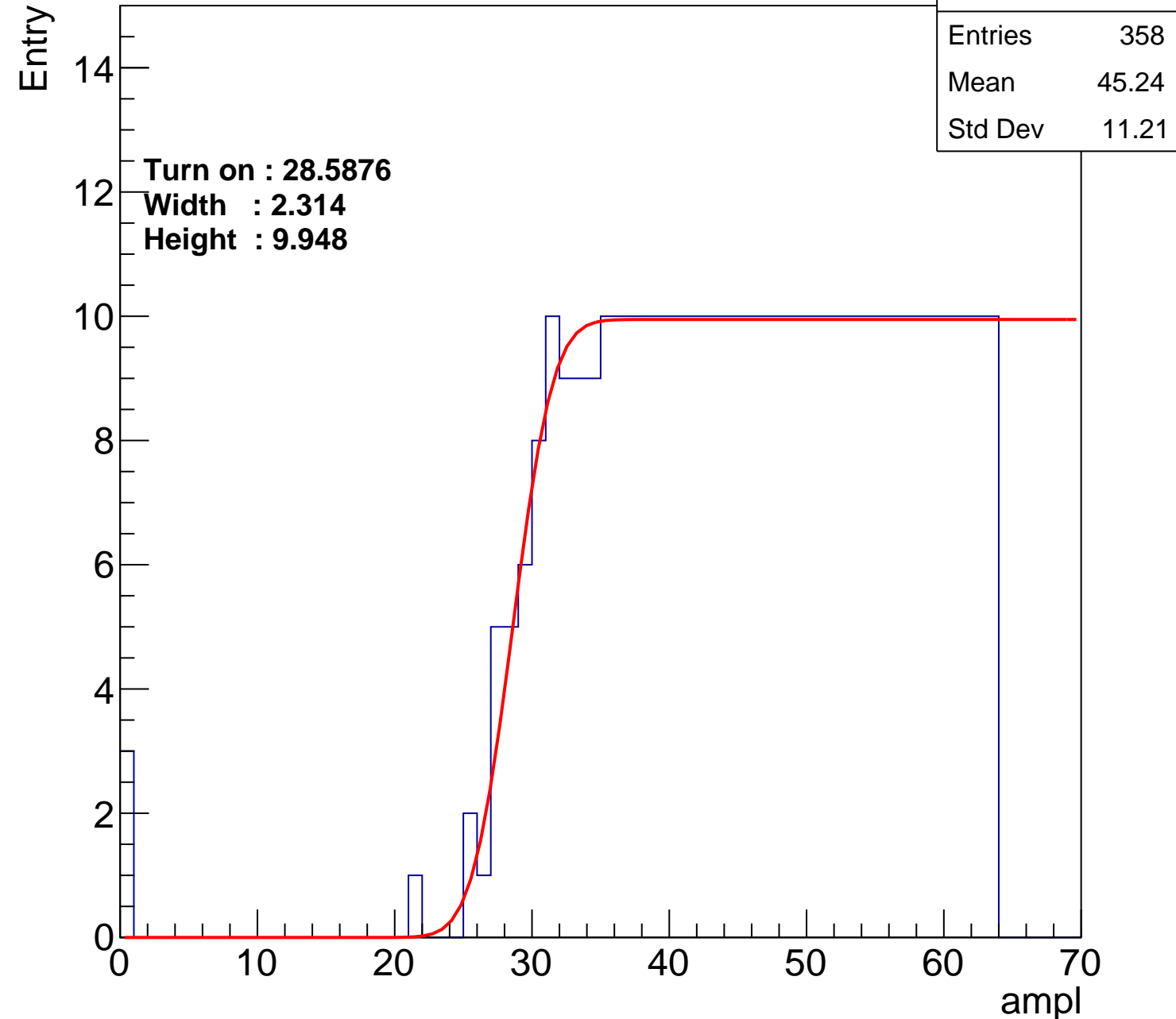
Width : 2.314

Height : 9.948

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch61

calib_packv5_042523_0143.root, FC#0, port D2

Entries	369
Mean	44.66
Std Dev	11.62

Turn on : 27.4327

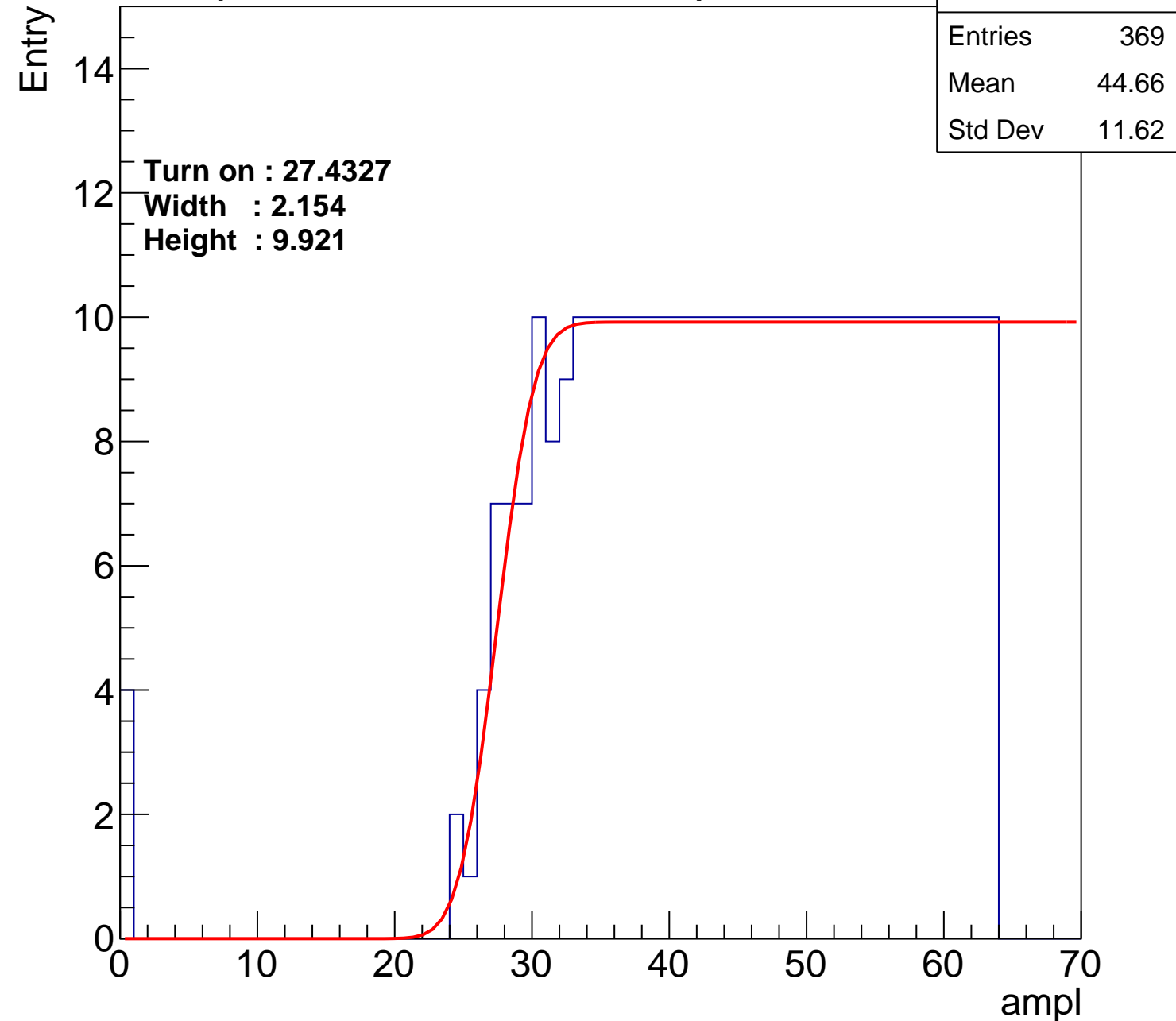
Width : 2.154

Height : 9.921

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch62

calib_packv5_042523_0143.root, FC#0, port D2

Entries	370
Mean	44.72
Std Dev	11.32

Turn on : 27.4994

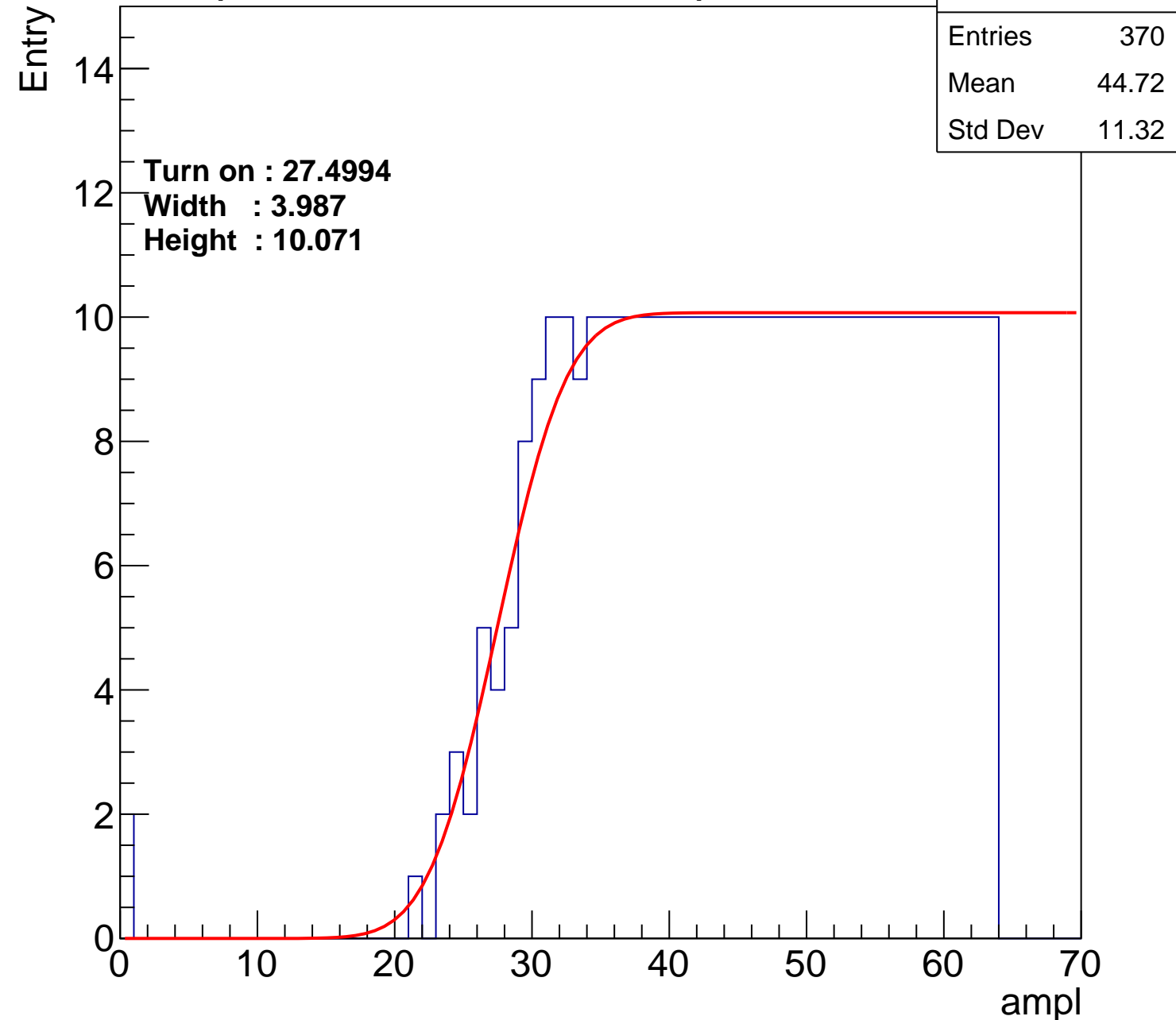
Width : 3.987

Height : 10.071

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch63

calib_packv5_042523_0143.root, FC#0, port D2

Entries	370
Mean	44.72
Std Dev	11.32

Turn on : 27.6648

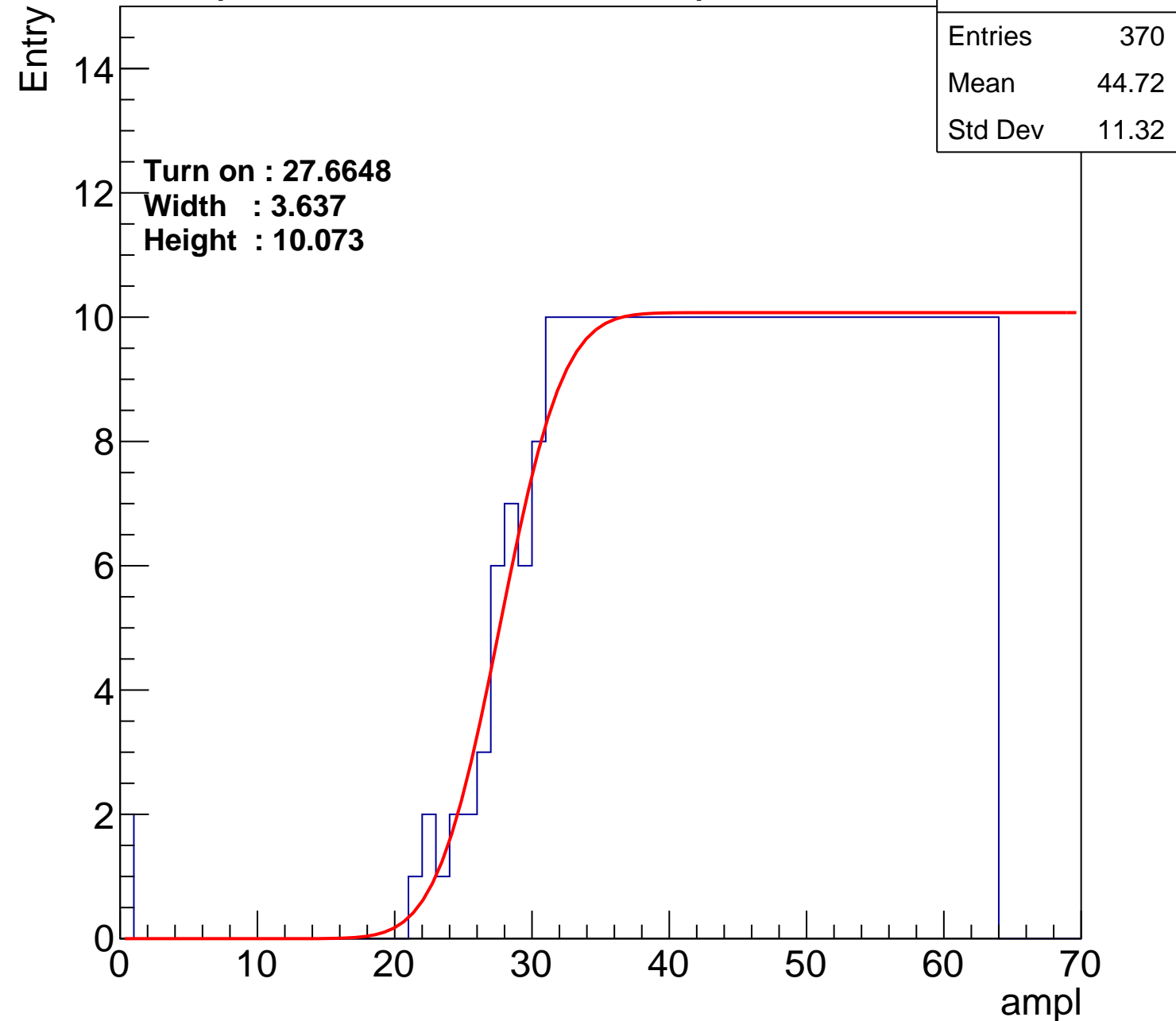
Width : 3.637

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch64

calib_packv5_042523_0143.root, FC#0, port D2

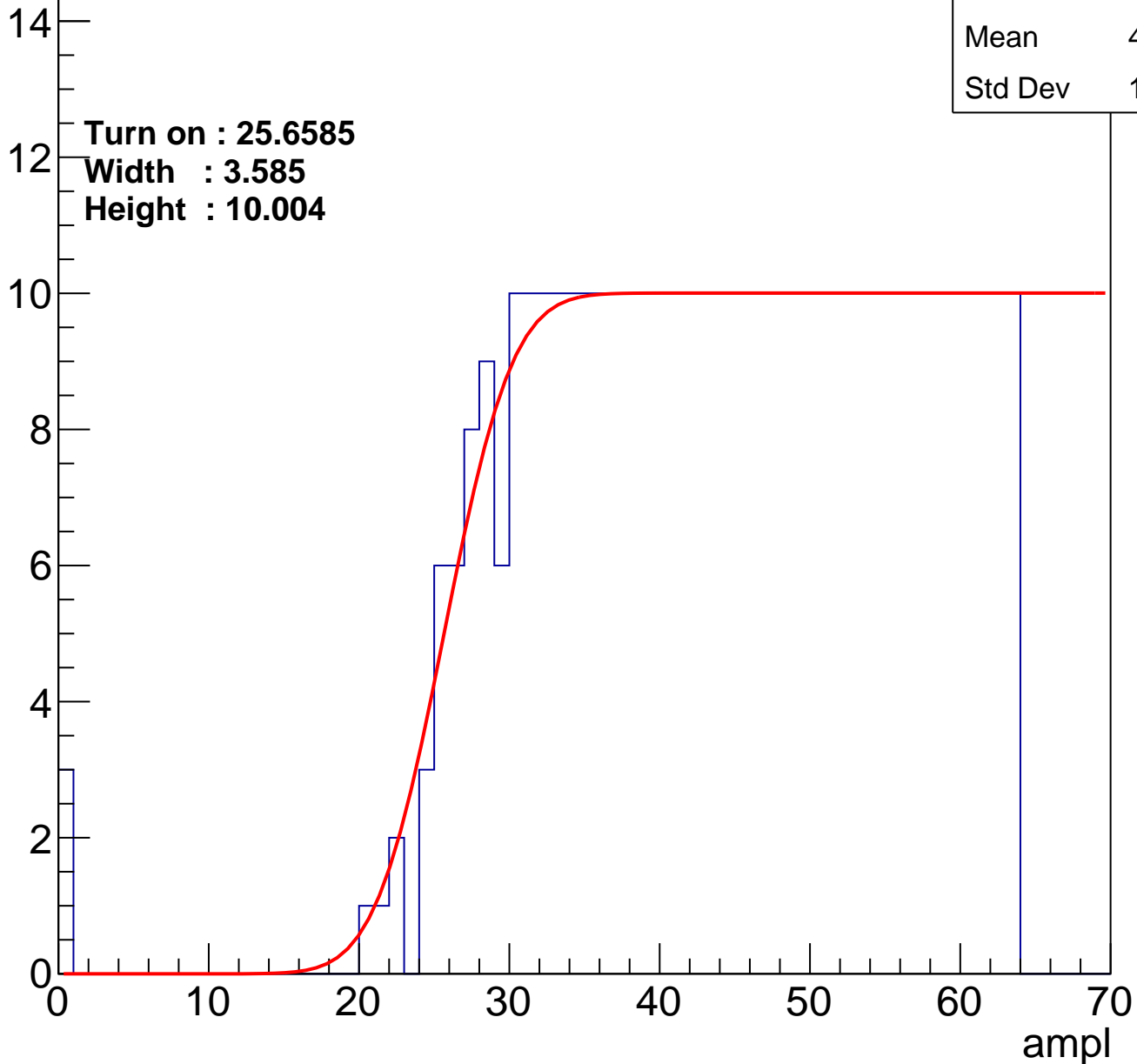
Entries	385
Mean	43.94
Std Dev	11.84

Turn on : 25.6585

Width : 3.585

Height : 10.004

Entry



B1L101S, U24-ch65

calib_packv5_042523_0143.root, FC#0, port D2

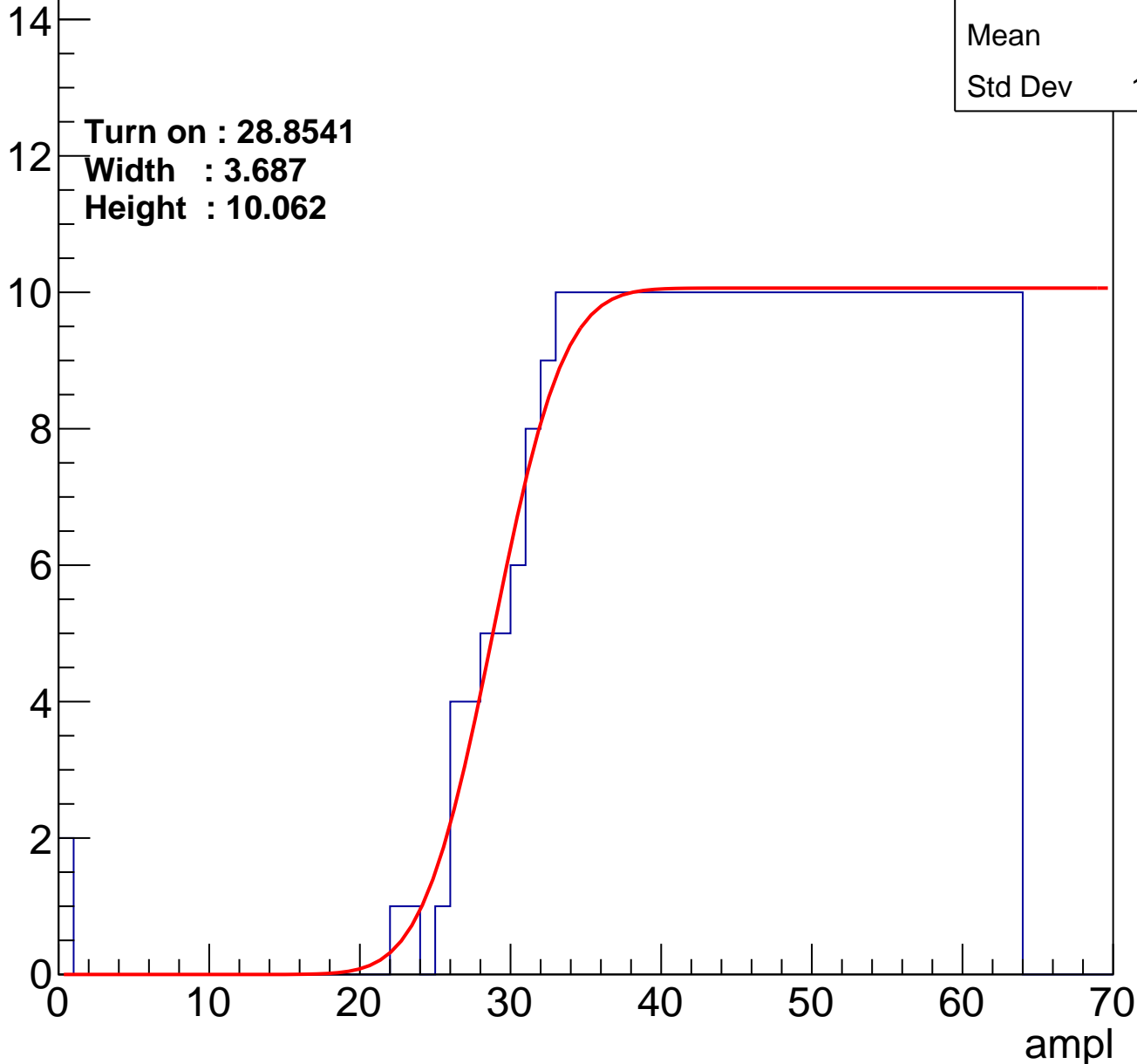
Entries	356
Mean	45.4
Std Dev	10.98

Turn on : 28.8541

Width : 3.687

Height : 10.062

Entry



B1L101S, U24-ch66

calib_packv5_042523_0143.root, FC#0, port D2

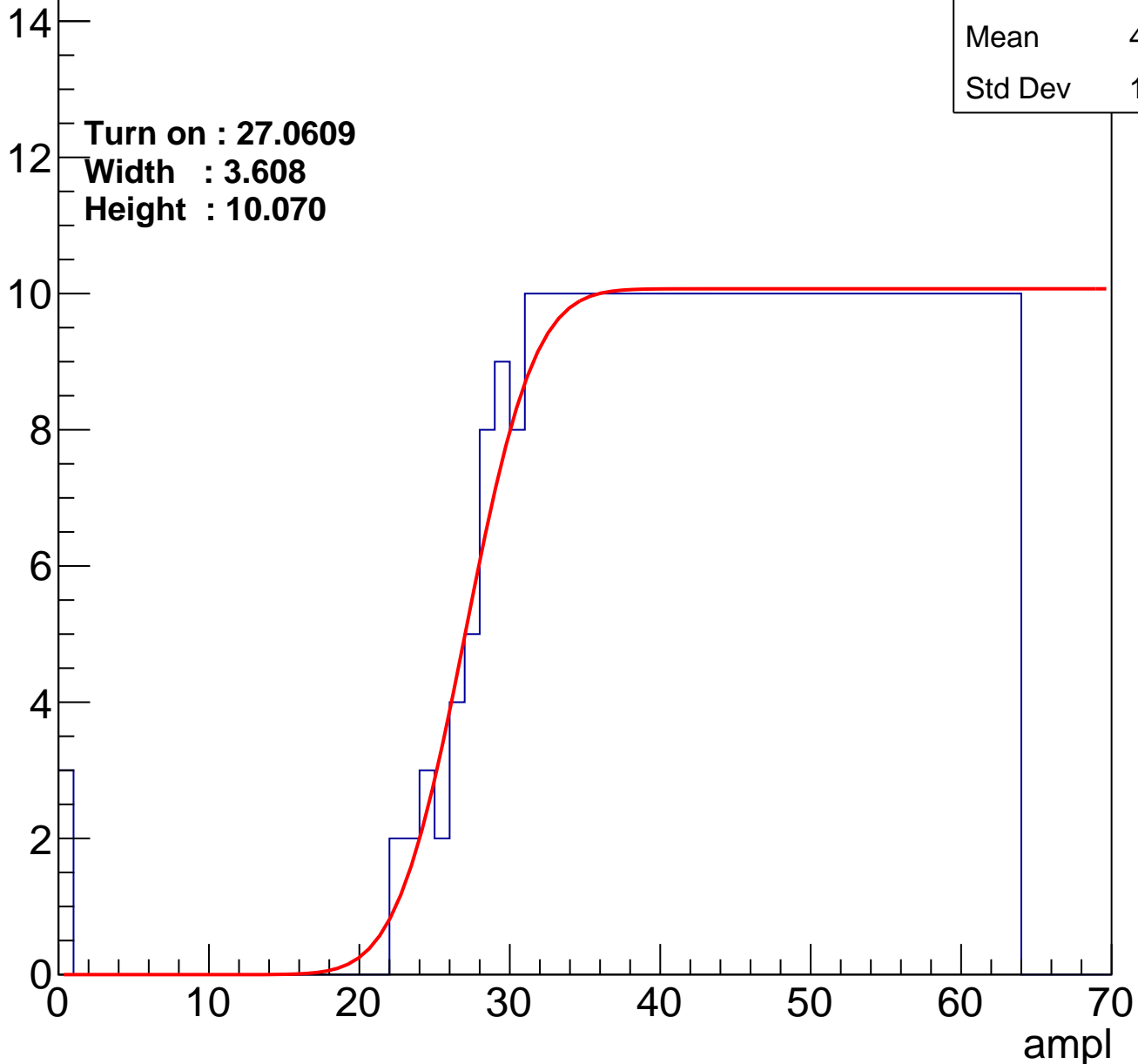
Entries	376
Mean	44.38
Std Dev	11.62

Turn on : 27.0609

Width : 3.608

Height : 10.070

Entry



B1L101S, U24-ch67

calib_packv5_042523_0143.root, FC#0, port D2

Entries	351
Mean	45.64
Std Dev	10.86

Turn on : 29.3933

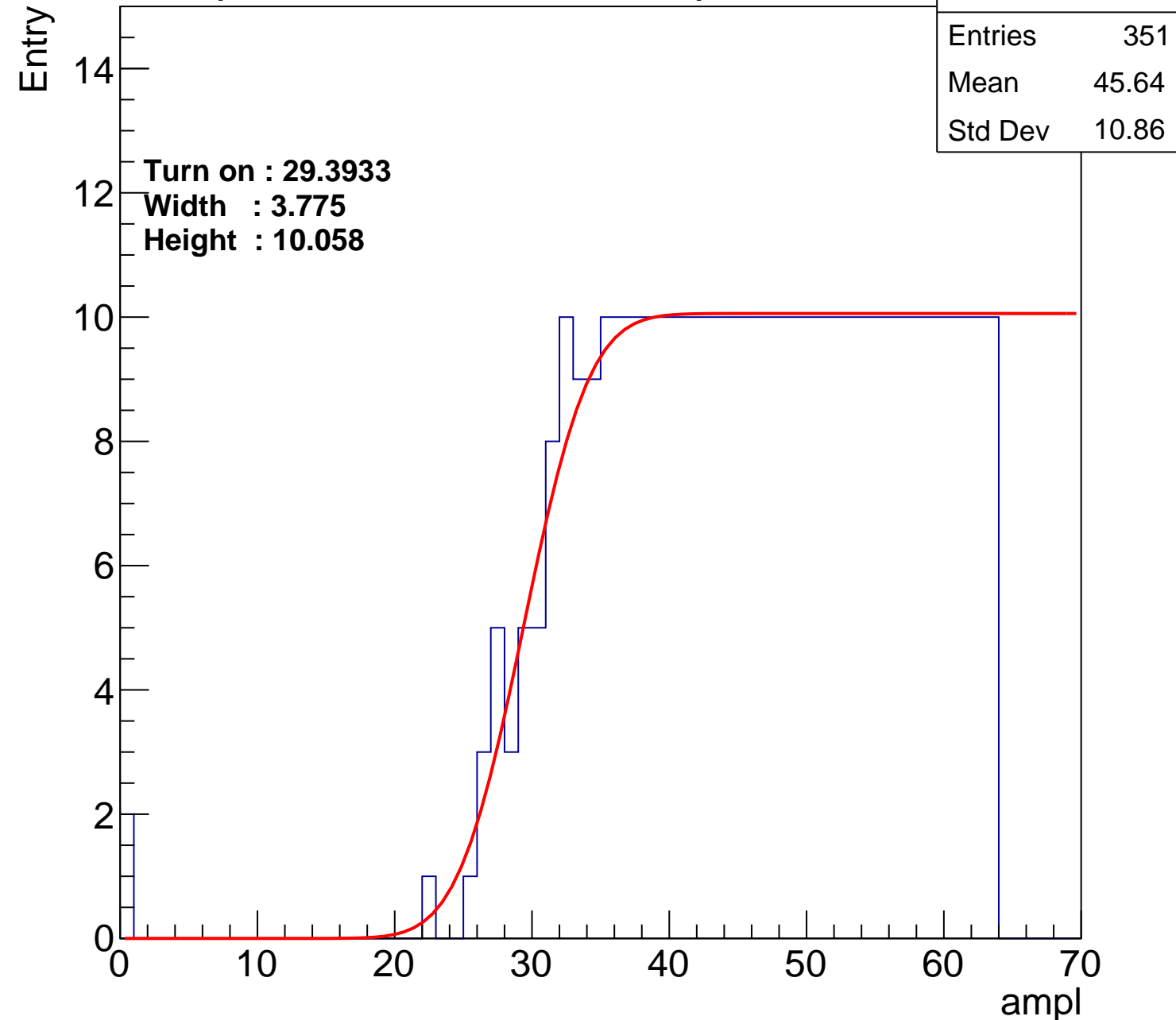
Width : 3.775

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch68

calib_packv5_042523_0143.root, FC#0, port D2

Entries	360
Mean	45.16
Std Dev	11.24

Turn on : 29.0067

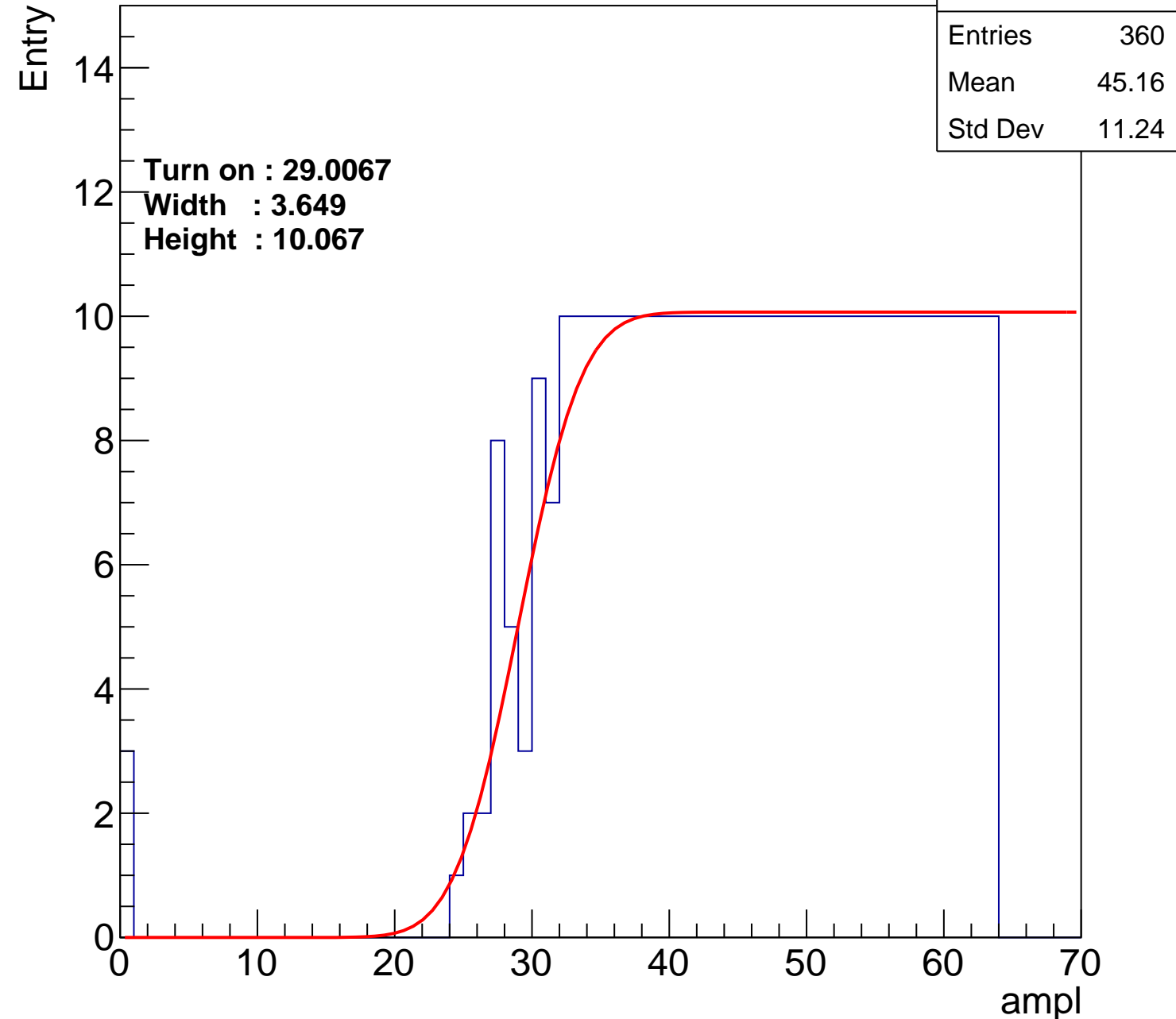
Width : 3.649

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch69

calib_packv5_042523_0143.root, FC#0, port D2

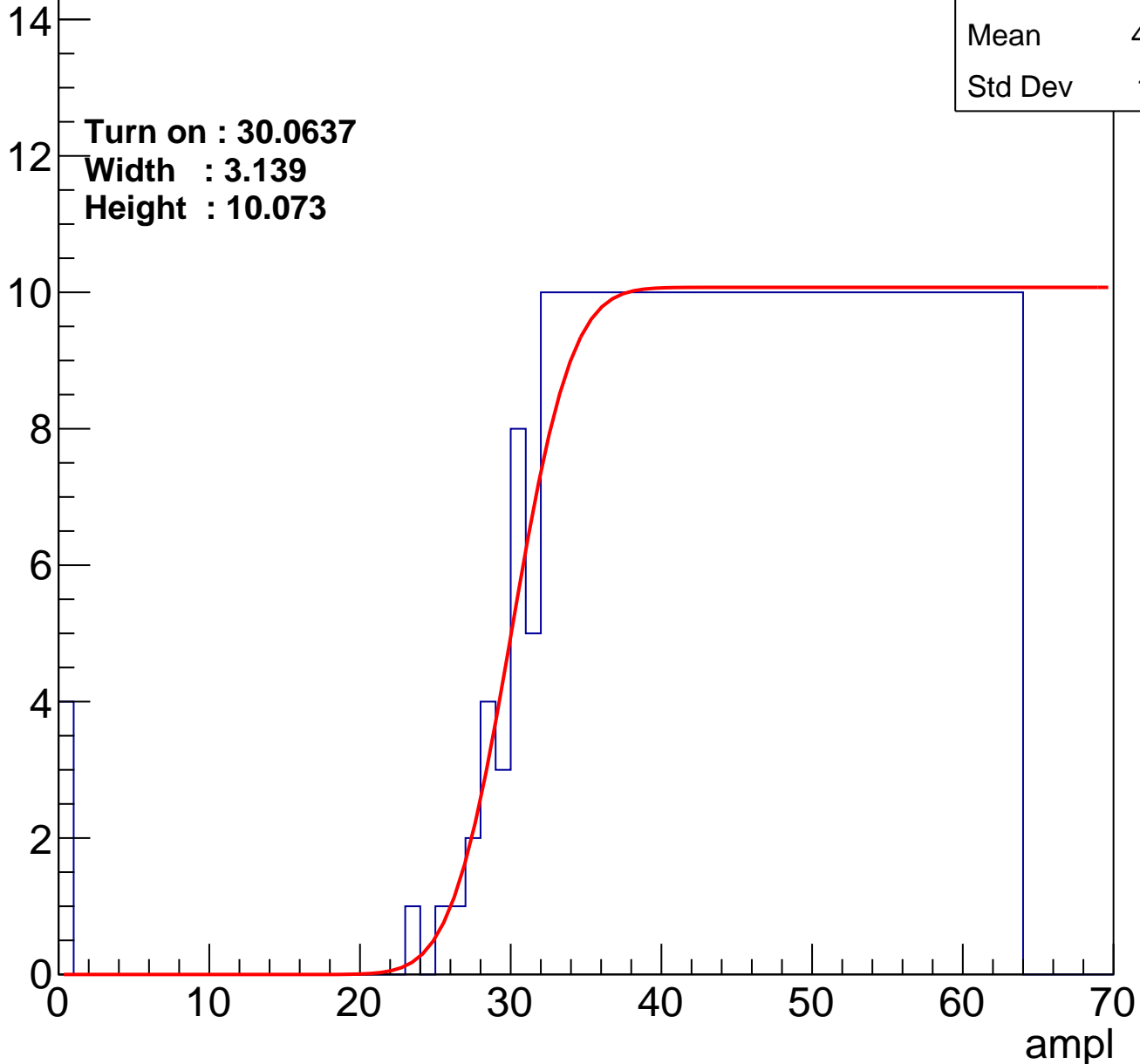
Entries	349
Mean	45.62
Std Dev	11.21

Turn on : 30.0637

Width : 3.139

Height : 10.073

Entry



B1L101S, U24-ch70

calib_packv5_042523_0143.root, FC#0, port D2

Entries	382
Mean	43.87
Std Dev	12.32

Turn on : 27.0714

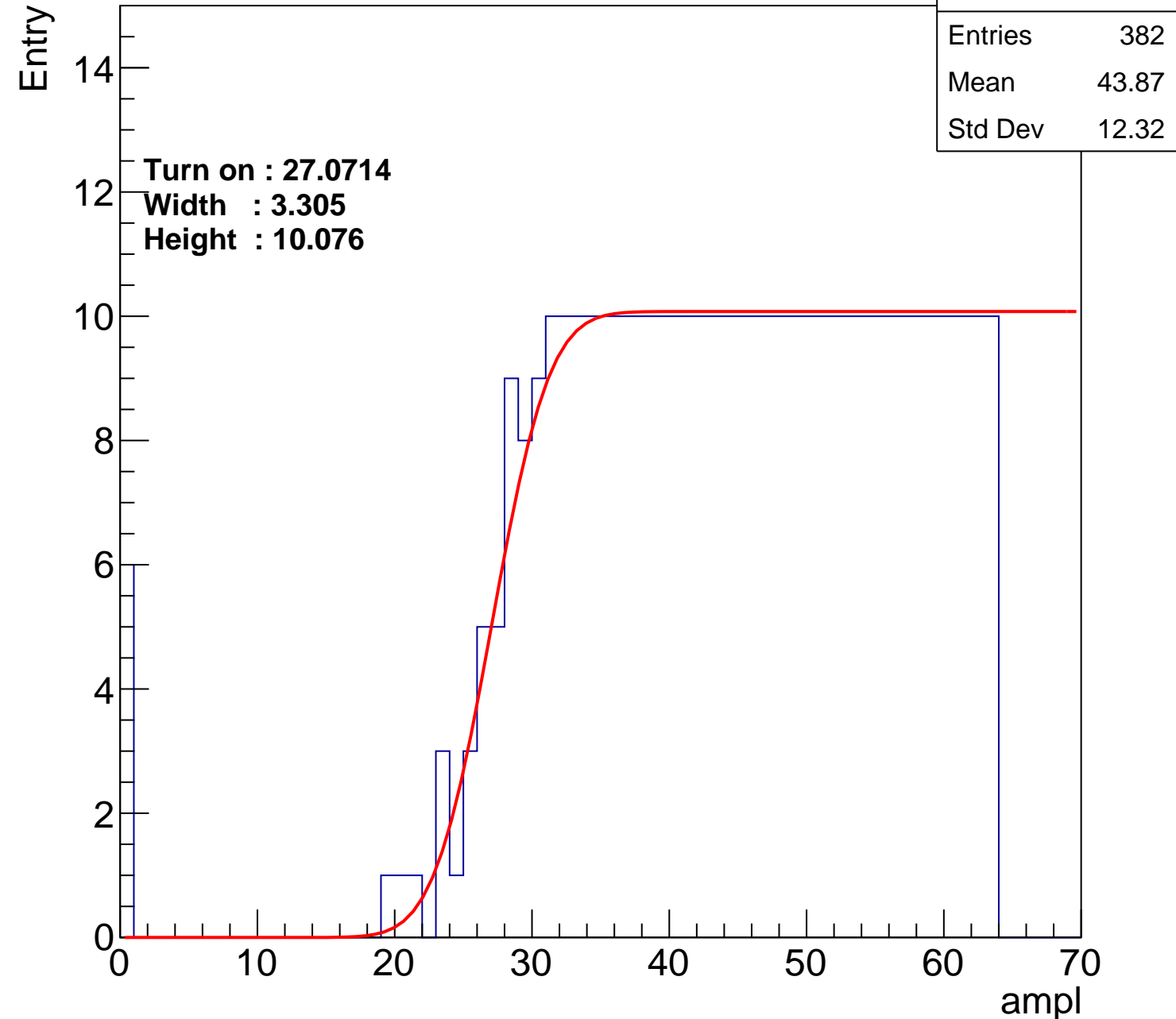
Width : 3.305

Height : 10.076

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch71

calib_packv5_042523_0143.root, FC#0, port D2

Entries	361
Mean	45.06
Std Dev	11.36

Turn on : 28.9582

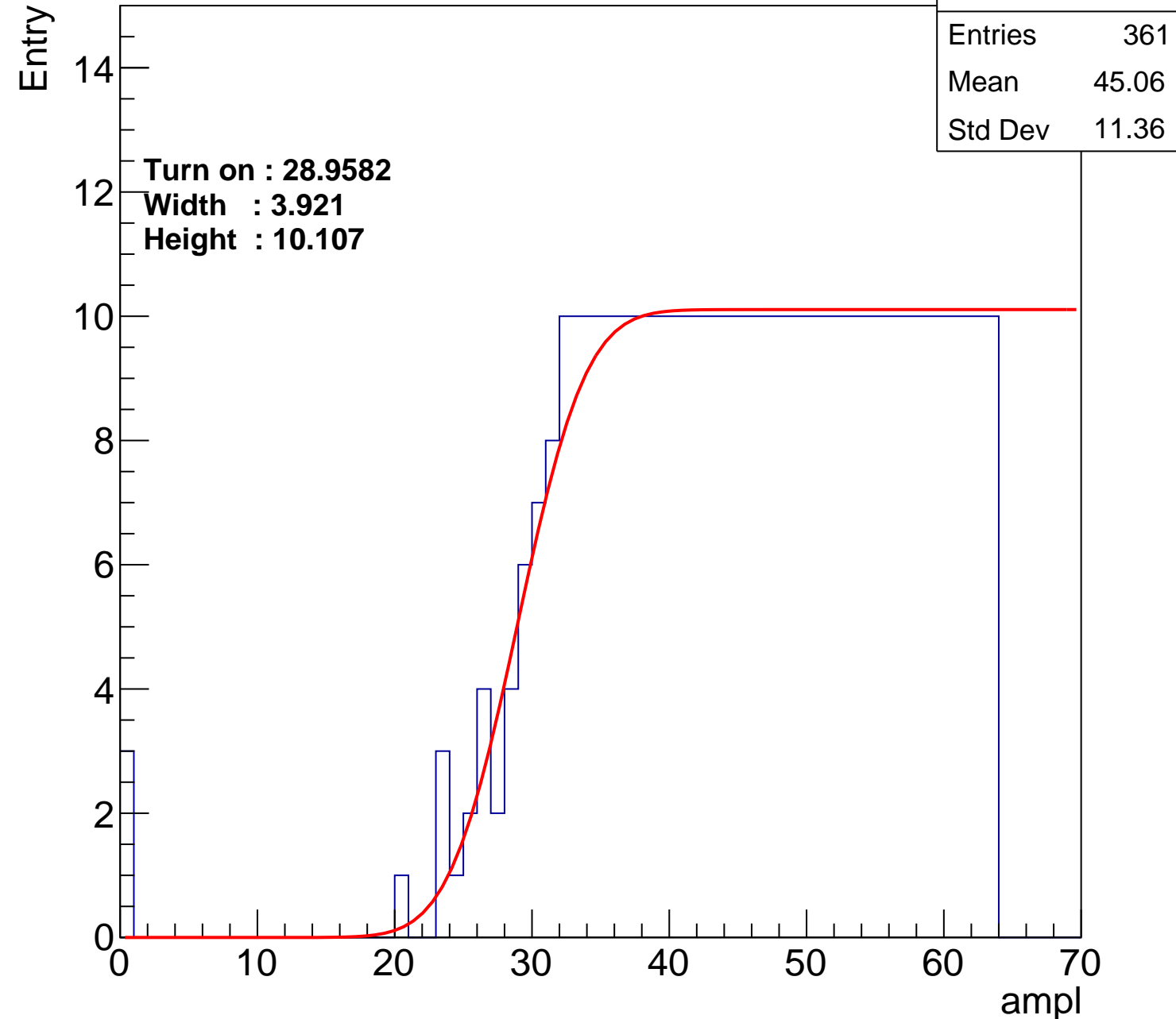
Width : 3.921

Height : 10.107

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch72

calib_packv5_042523_0143.root, FC#0, port D2

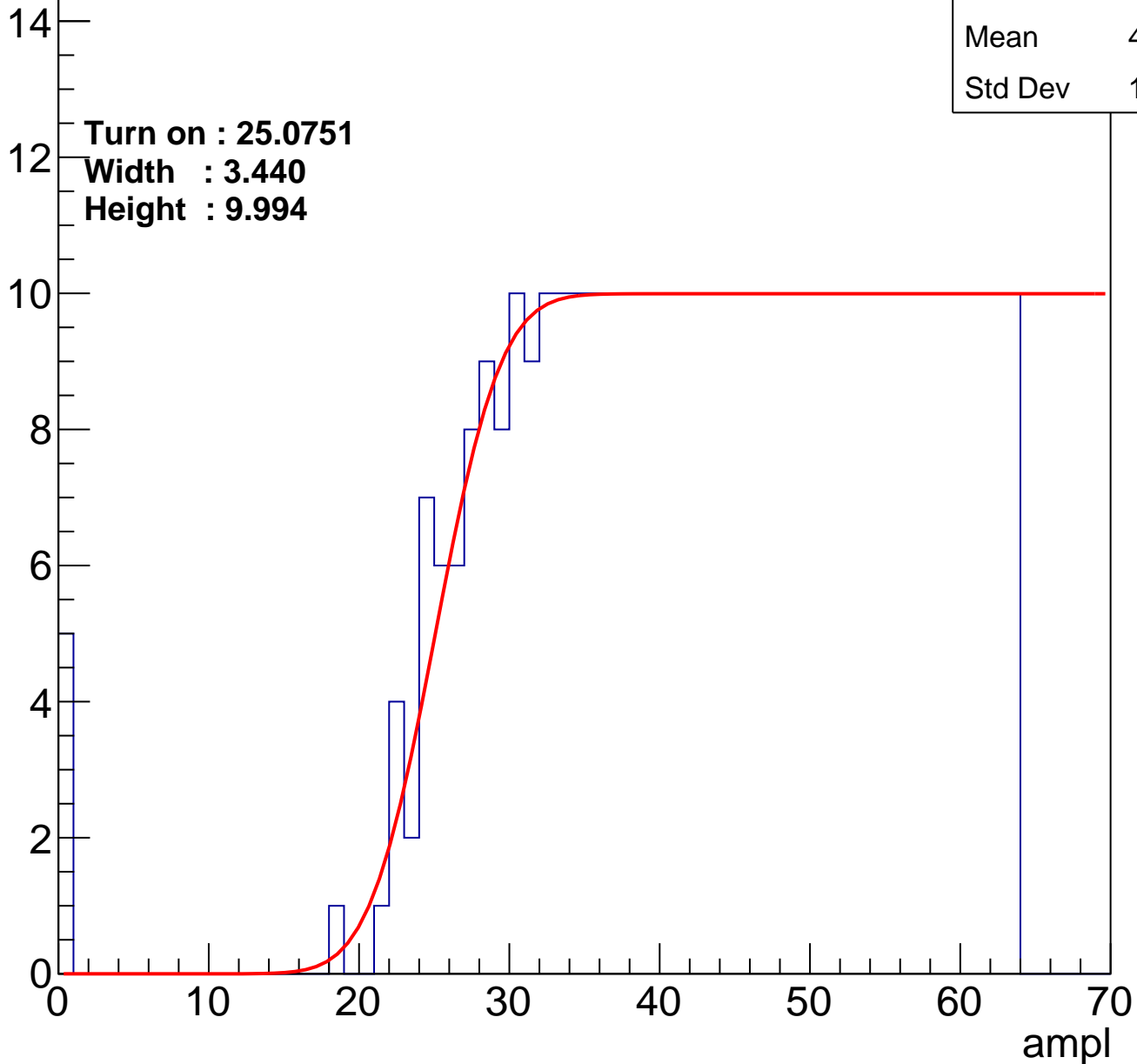
Entries	396
Mean	43.25
Std Dev	12.46

Turn on : 25.0751

Width : 3.440

Height : 9.994

Entry



B1L101S, U24-ch73

calib_packv5_042523_0143.root, FC#0, port D2

Entries	351
Mean	45.65
Std Dev	10.84

Turn on : 29.4426

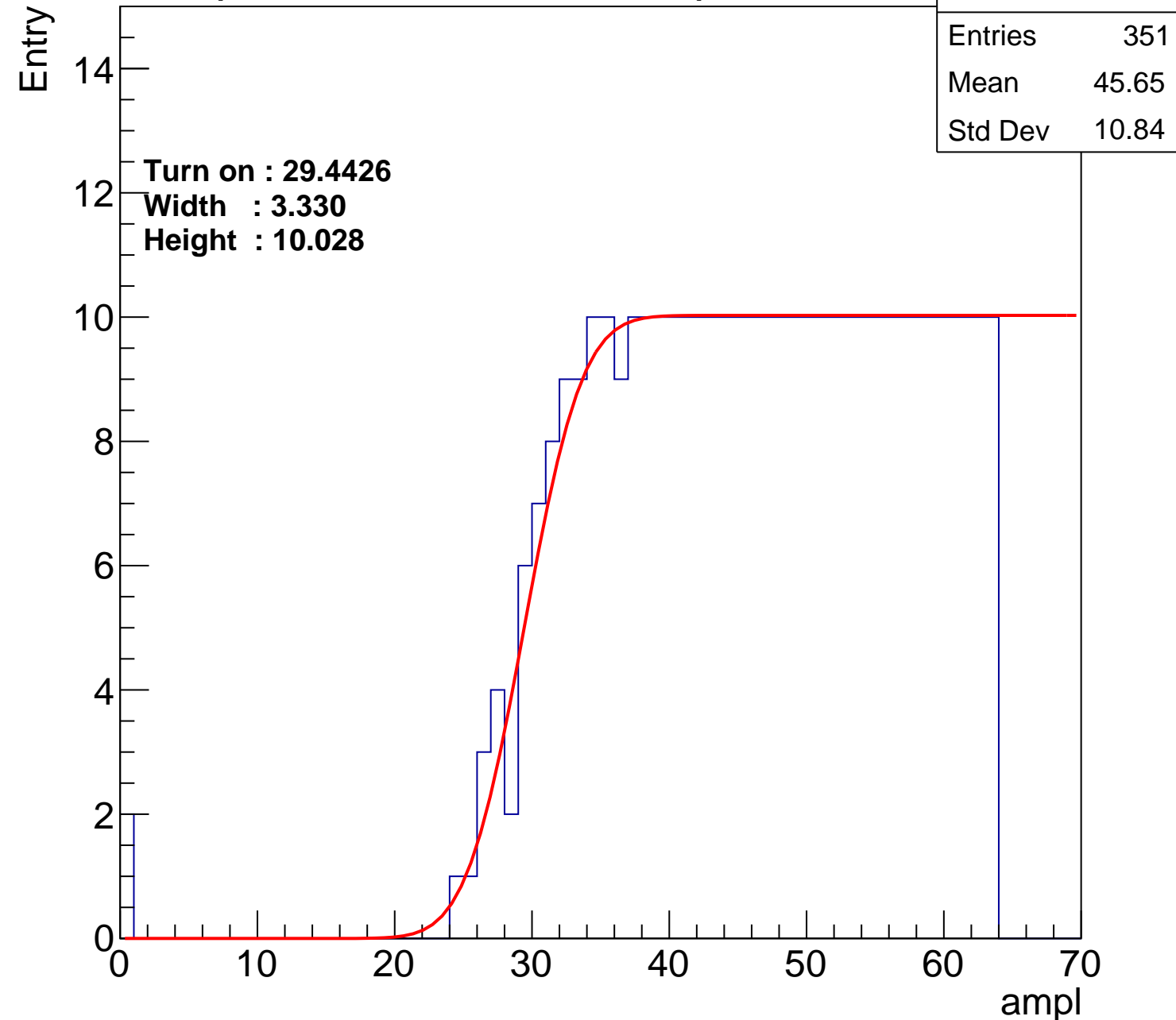
Width : 3.330

Height : 10.028

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch74

calib_packv5_042523_0143.root, FC#0, port D2

Entries	363
Mean	44.92
Std Dev	11.54

Turn on : 28.1900

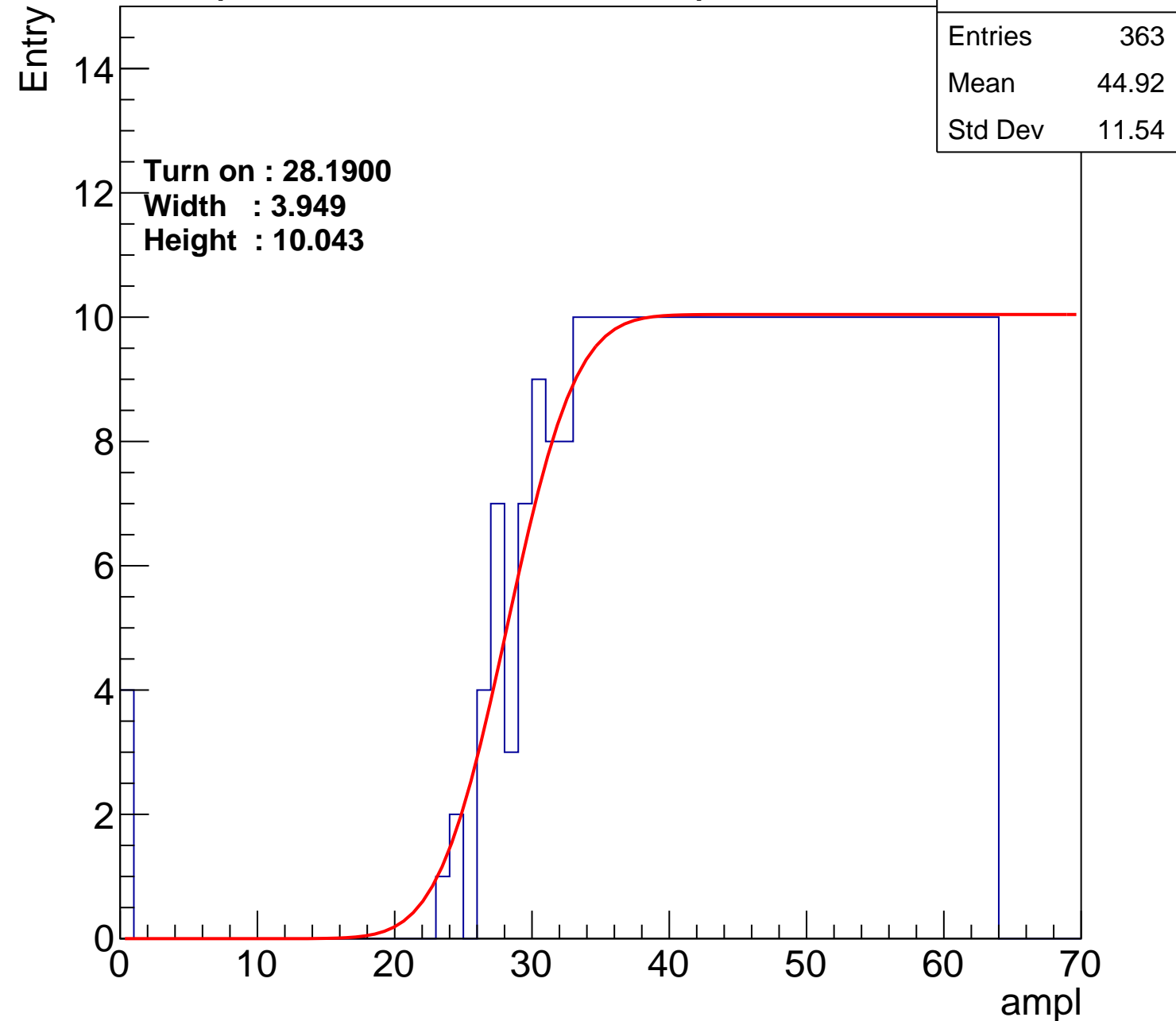
Width : 3.949

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch75

calib_packv5_042523_0143.root, FC#0, port D2

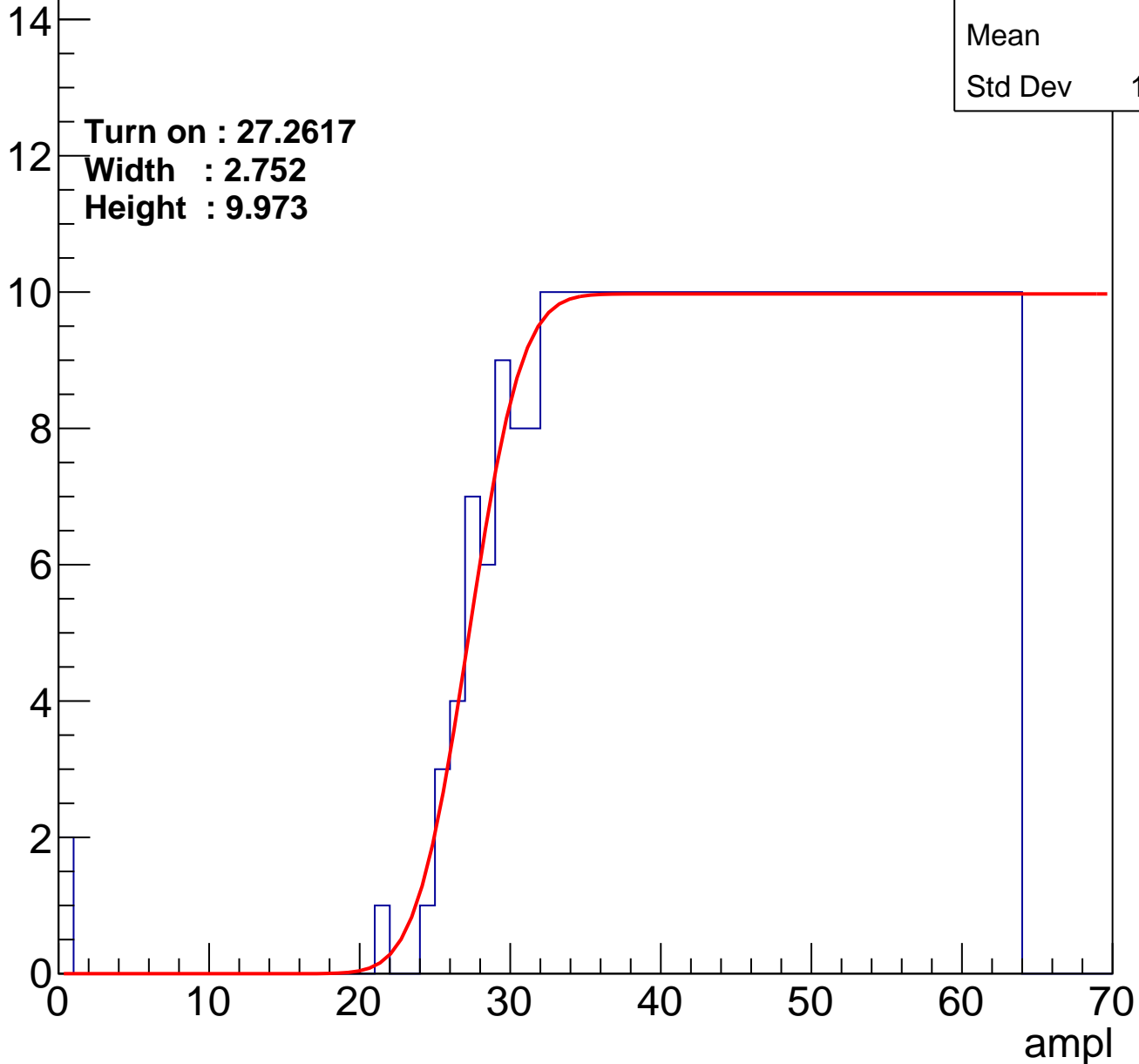
Entries	369
Mean	44.8
Std Dev	11.24

Turn on : 27.2617

Width : 2.752

Height : 9.973

Entry



B1L101S, U24-ch76

calib_packv5_042523_0143.root, FC#0, port D2

Entries	351
Mean	45.53
Std Dev	11.24

Turn on : 28.9846

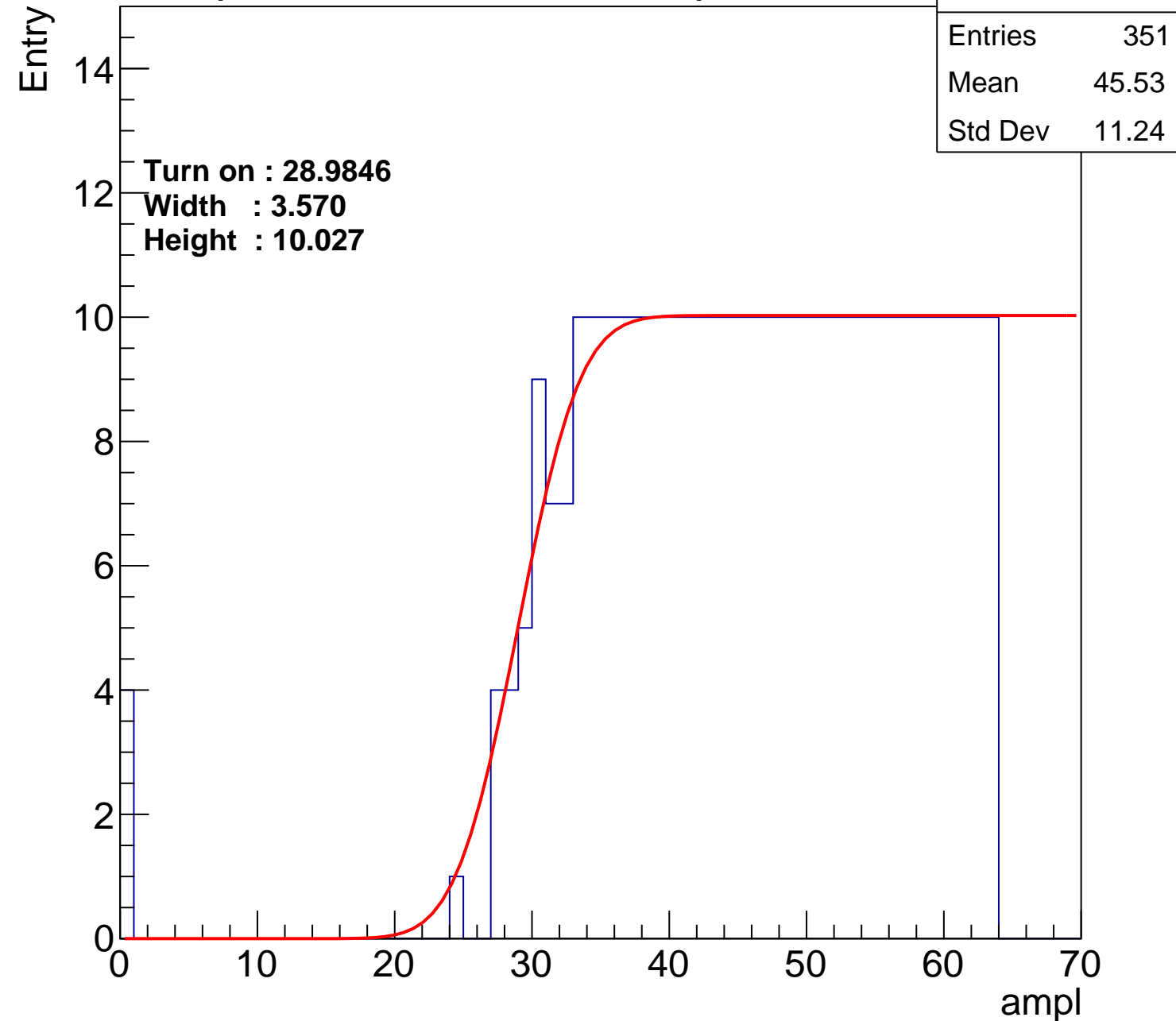
Width : 3.570

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch77

calib_packv5_042523_0143.root, FC#0, port D2

Entries	352
Mean	45.59
Std Dev	10.89

Turn on : 29.5731

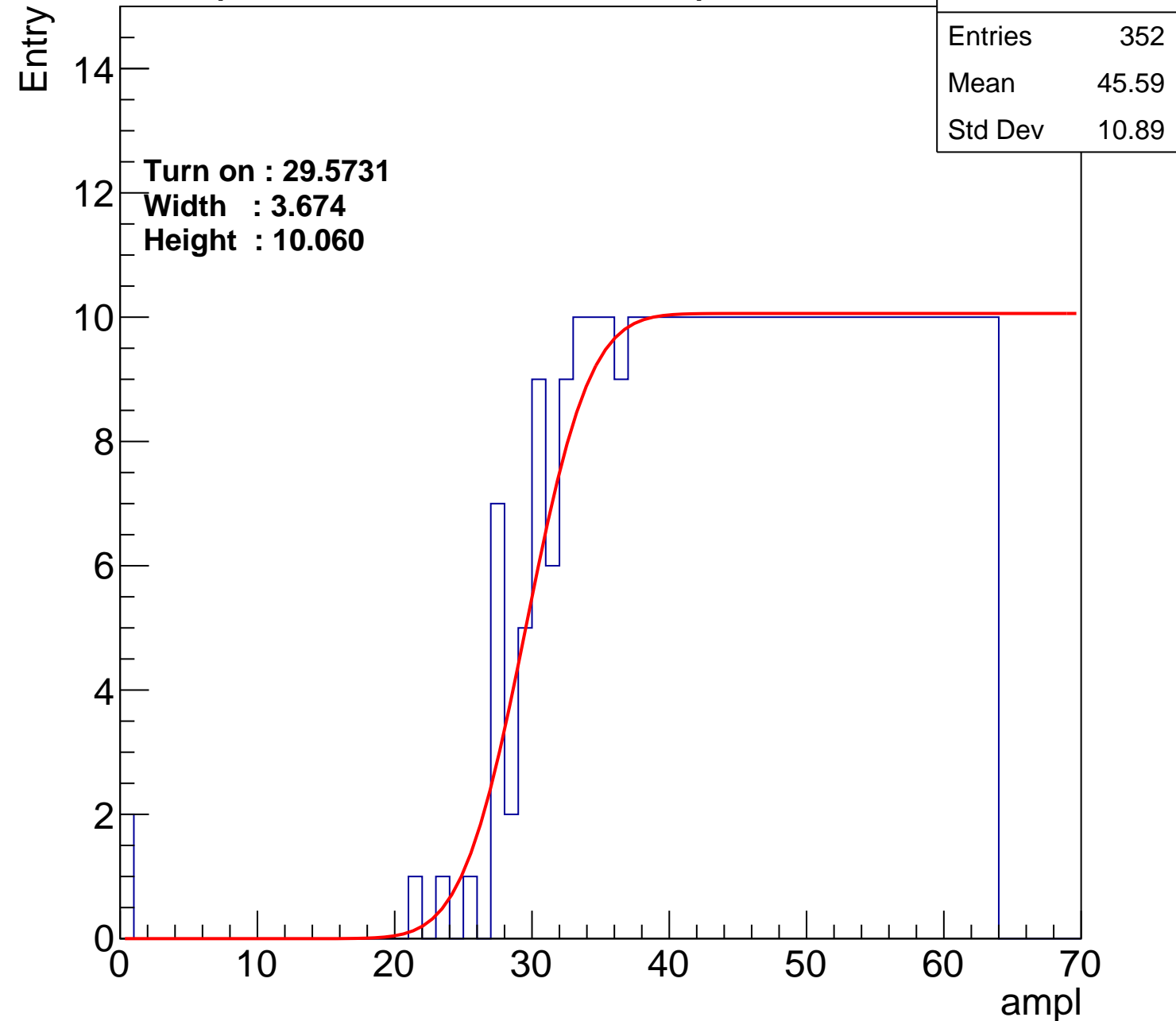
Width : 3.674

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch78

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.27
Std Dev	12.11

Turn on : 27.1437

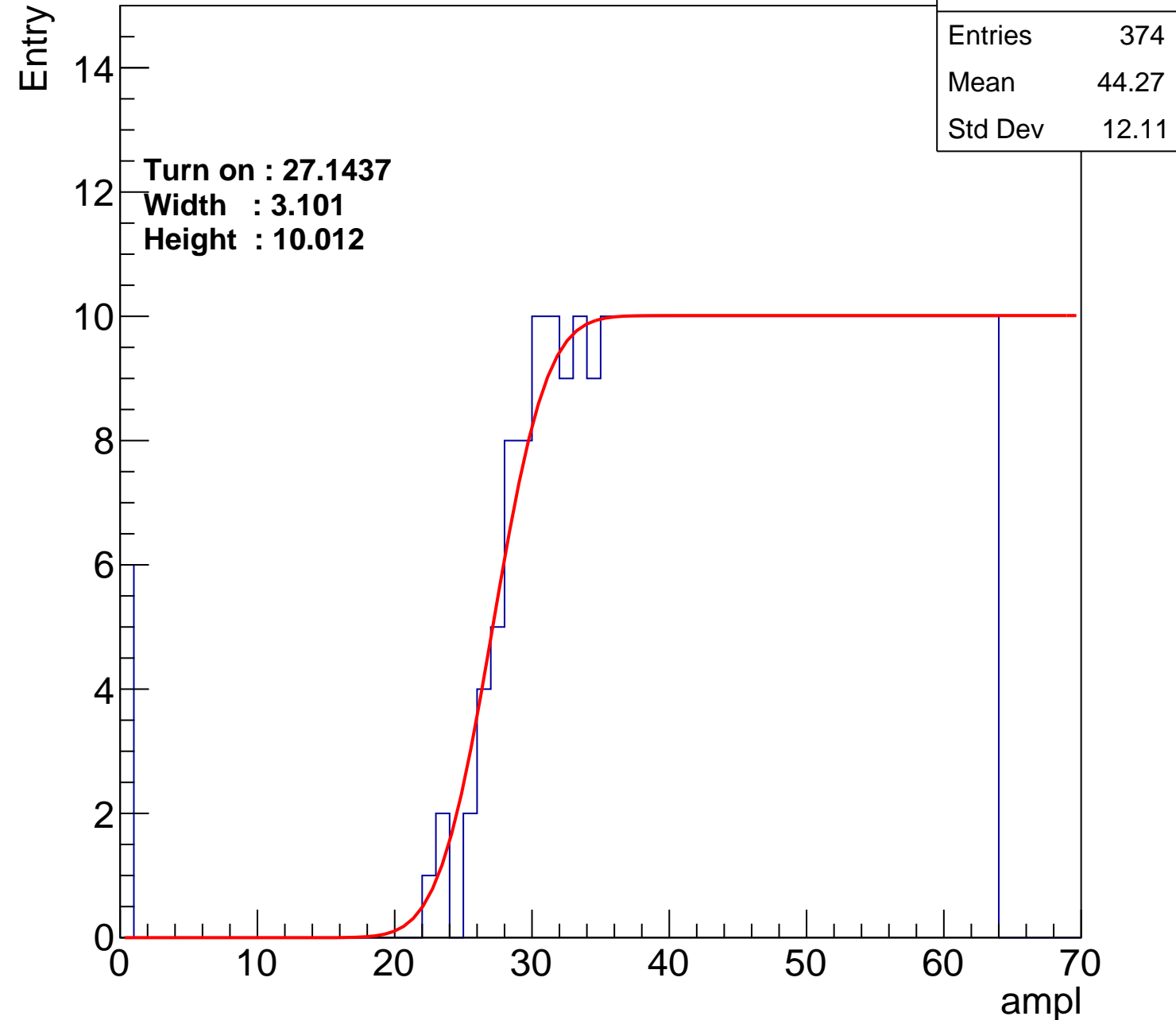
Width : 3.101

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch79

calib_packv5_042523_0143.root, FC#0, port D2

Entries	351
Mean	45.66
Std Dev	10.83

Turn on : 29.4125

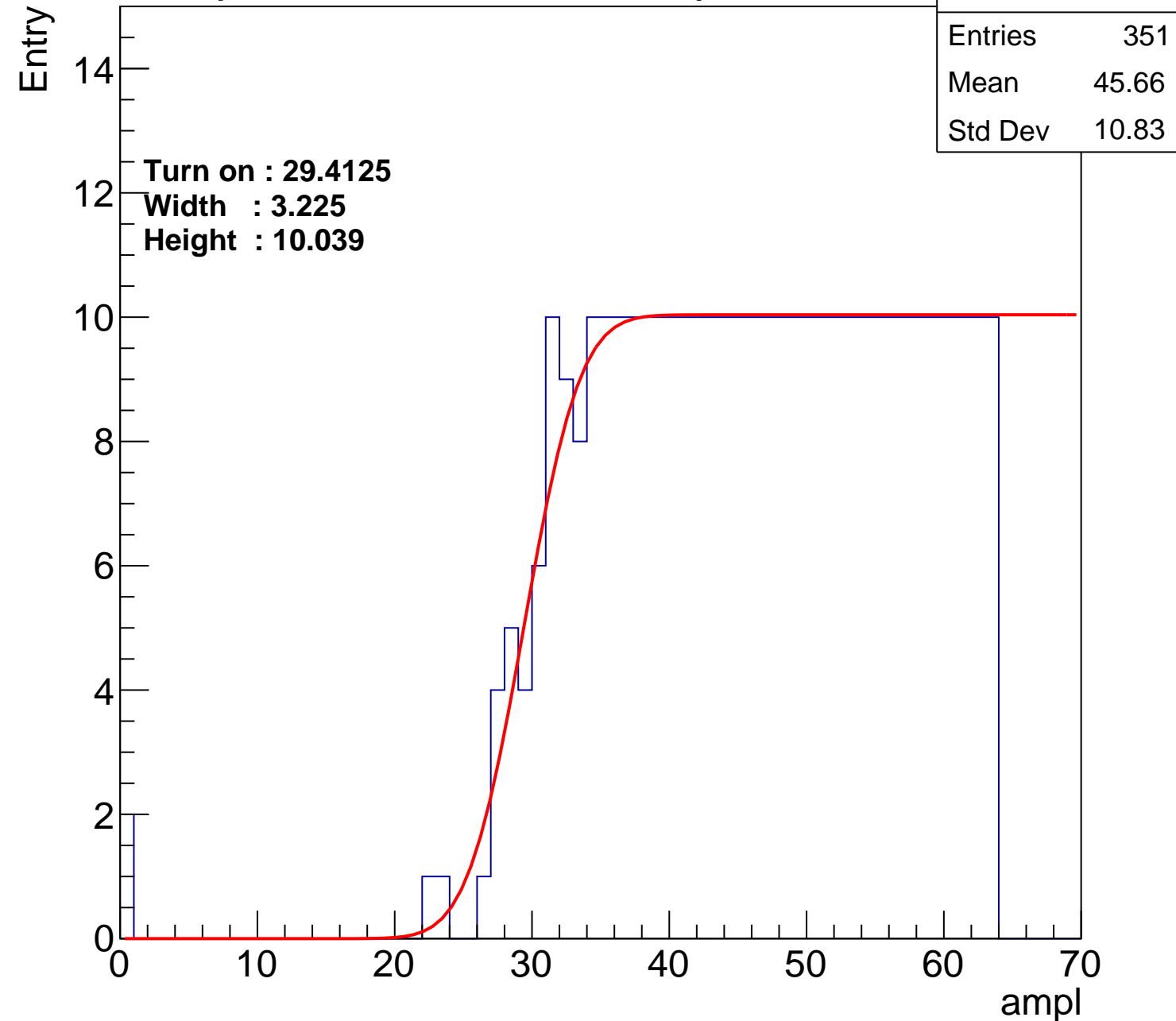
Width : 3.225

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch80

calib_packv5_042523_0143.root, FC#0, port D2

Entries	354
Mean	45.51
Std Dev	10.91

Turn on : 29.0001

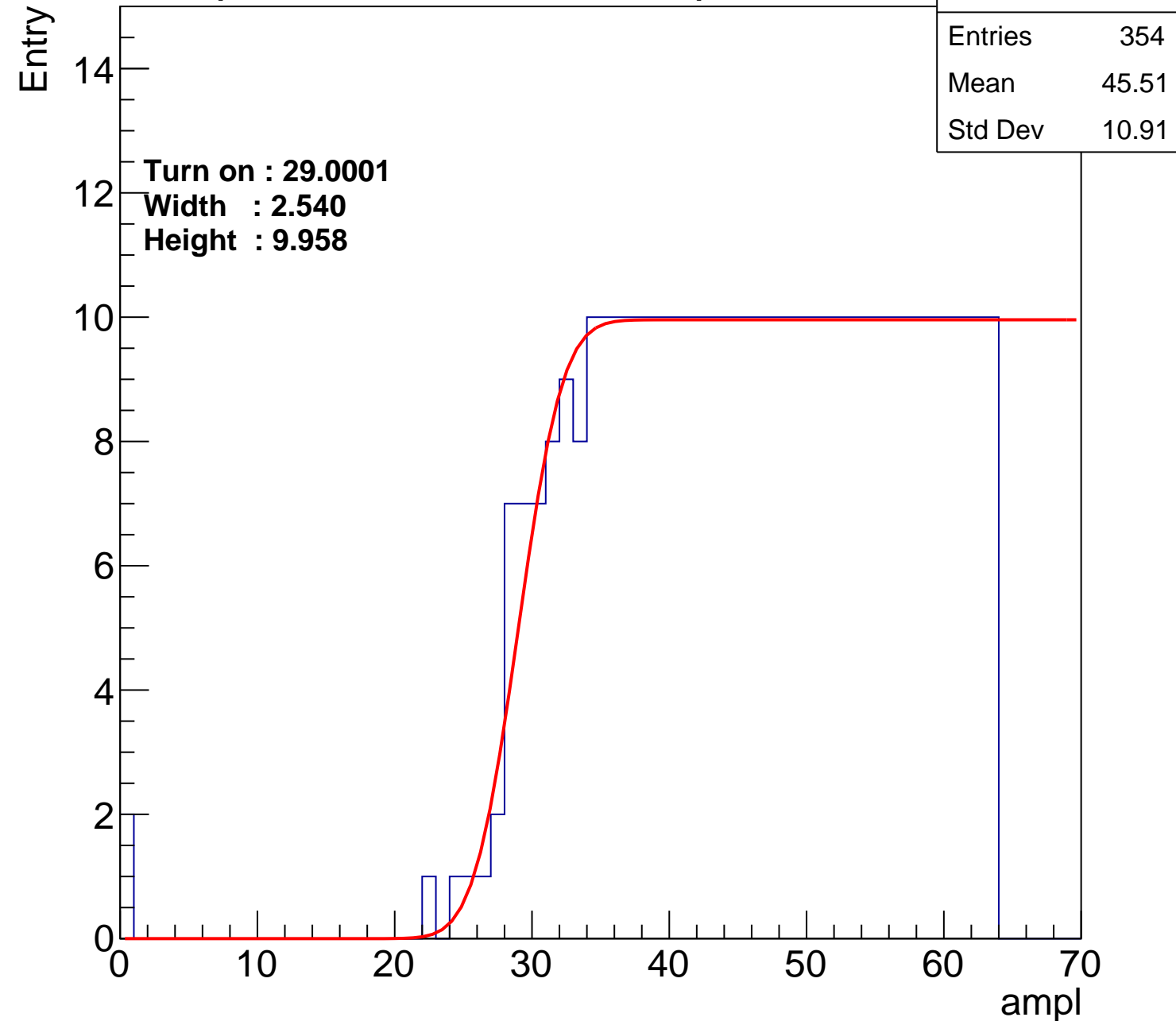
Width : 2.540

Height : 9.958

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch81

calib_packv5_042523_0143.root, FC#0, port D2

Entries	345
Mean	45.88
Std Dev	10.91

Turn on : 29.9705

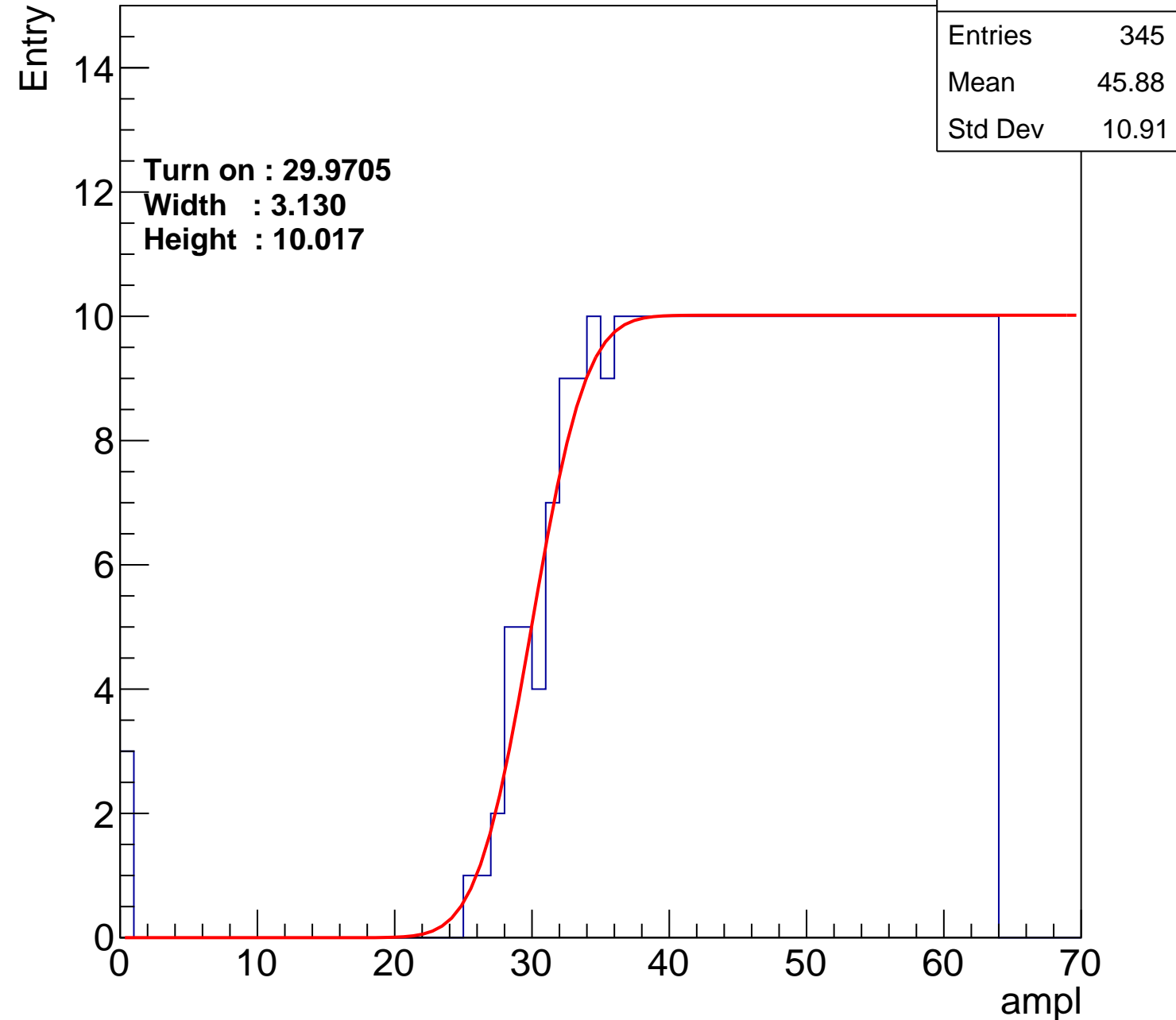
Width : 3.130

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch82

calib_packv5_042523_0143.root, FC#0, port D2

Entries	358
Mean	45.35
Std Dev	10.85

Turn on : 28.7566

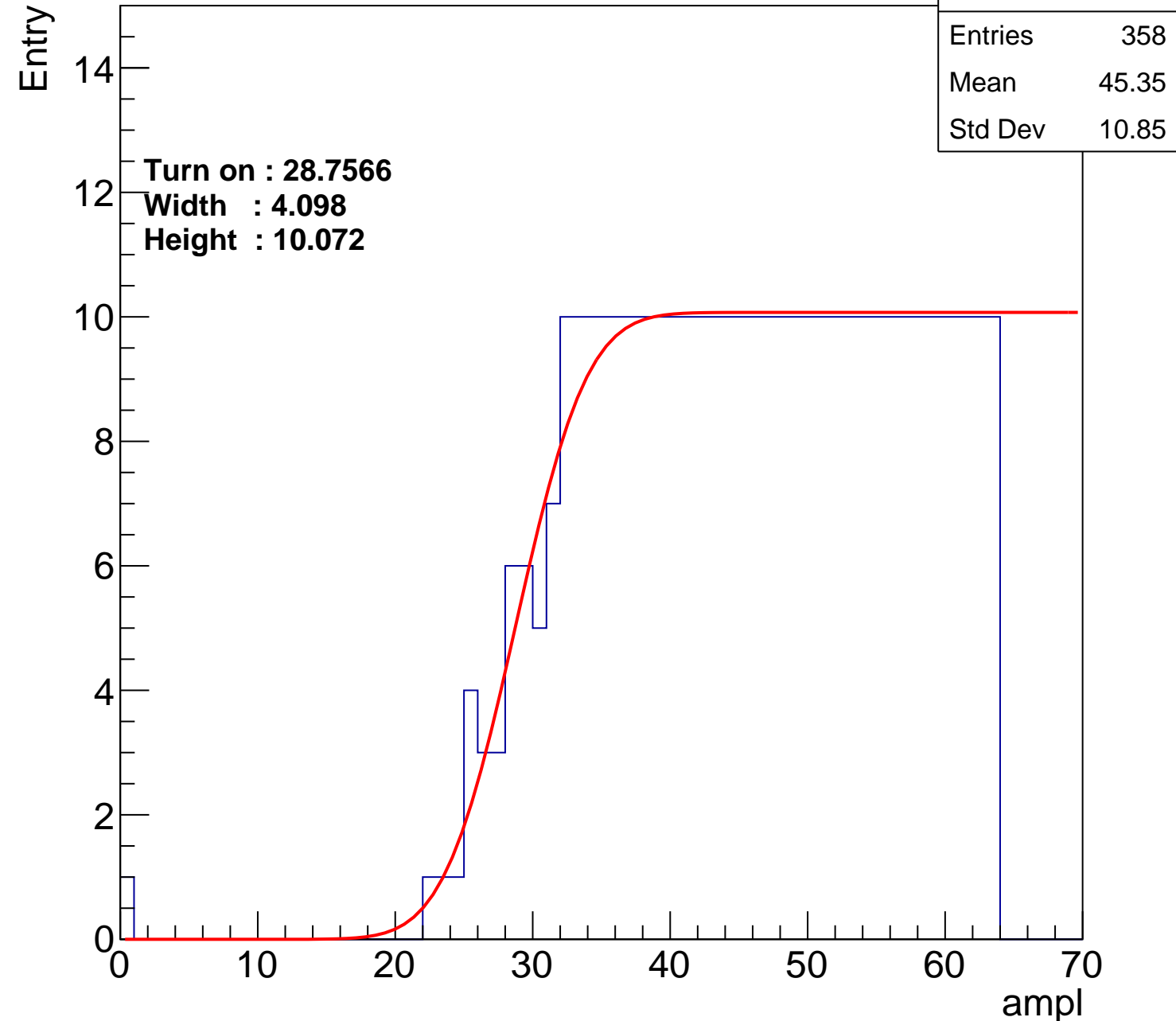
Width : 4.098

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch83

calib_packv5_042523_0143.root, FC#0, port D2

Entries	350
Mean	45.64
Std Dev	11.03

Turn on : 29.8198

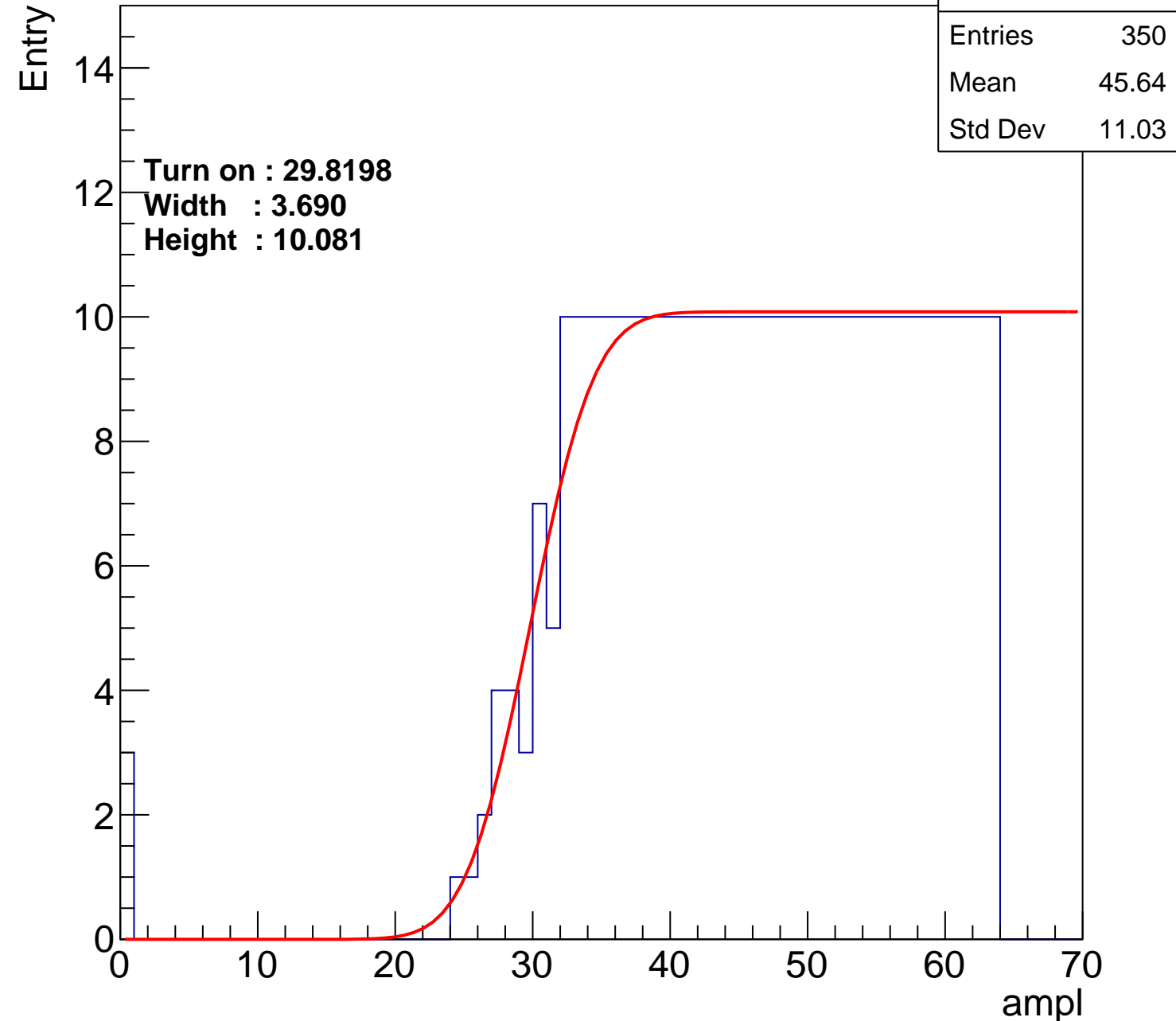
Width : 3.690

Height : 10.081

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch84

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.3
Std Dev	11.82

Turn on : 27.0194

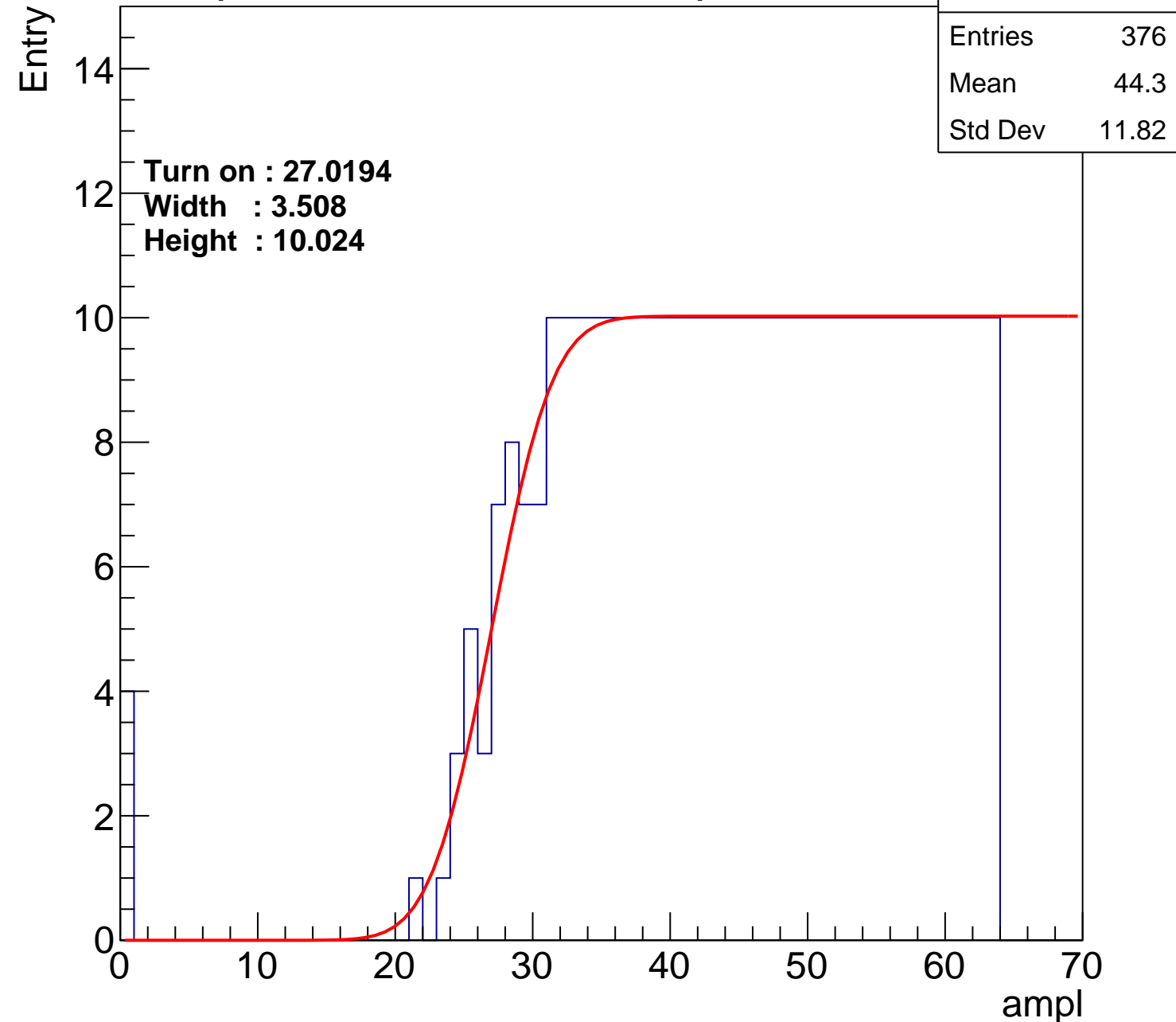
Width : 3.508

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch85

calib_packv5_042523_0143.root, FC#0, port D2

Entries	359
Mean	45.23
Std Dev	11.18

Turn on : 28.3050

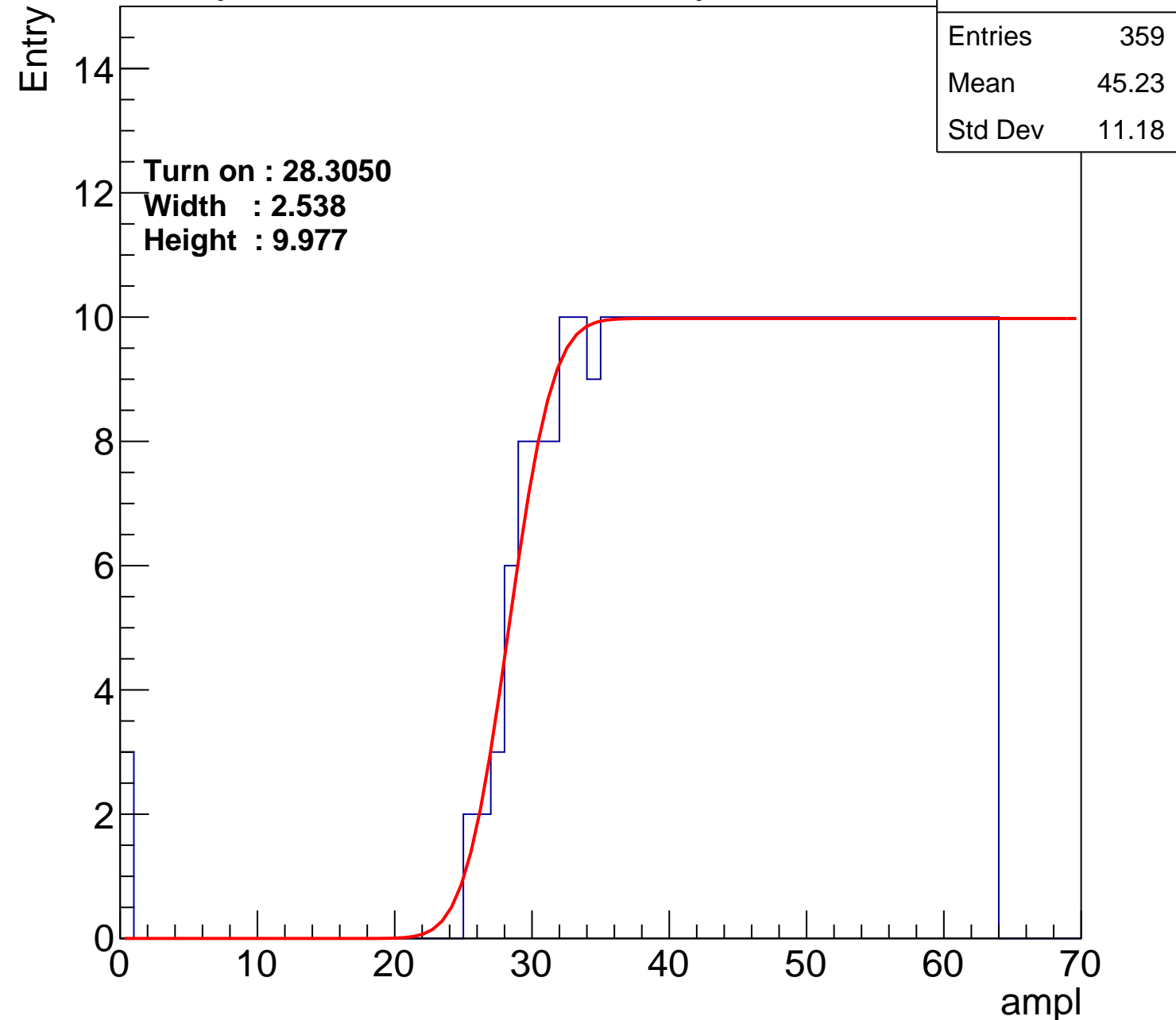
Width : 2.538

Height : 9.977

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch86

calib_packv5_042523_0143.root, FC#0, port D2

Entries	370
Mean	44.36
Std Dev	12.26

Turn on : 27.7013

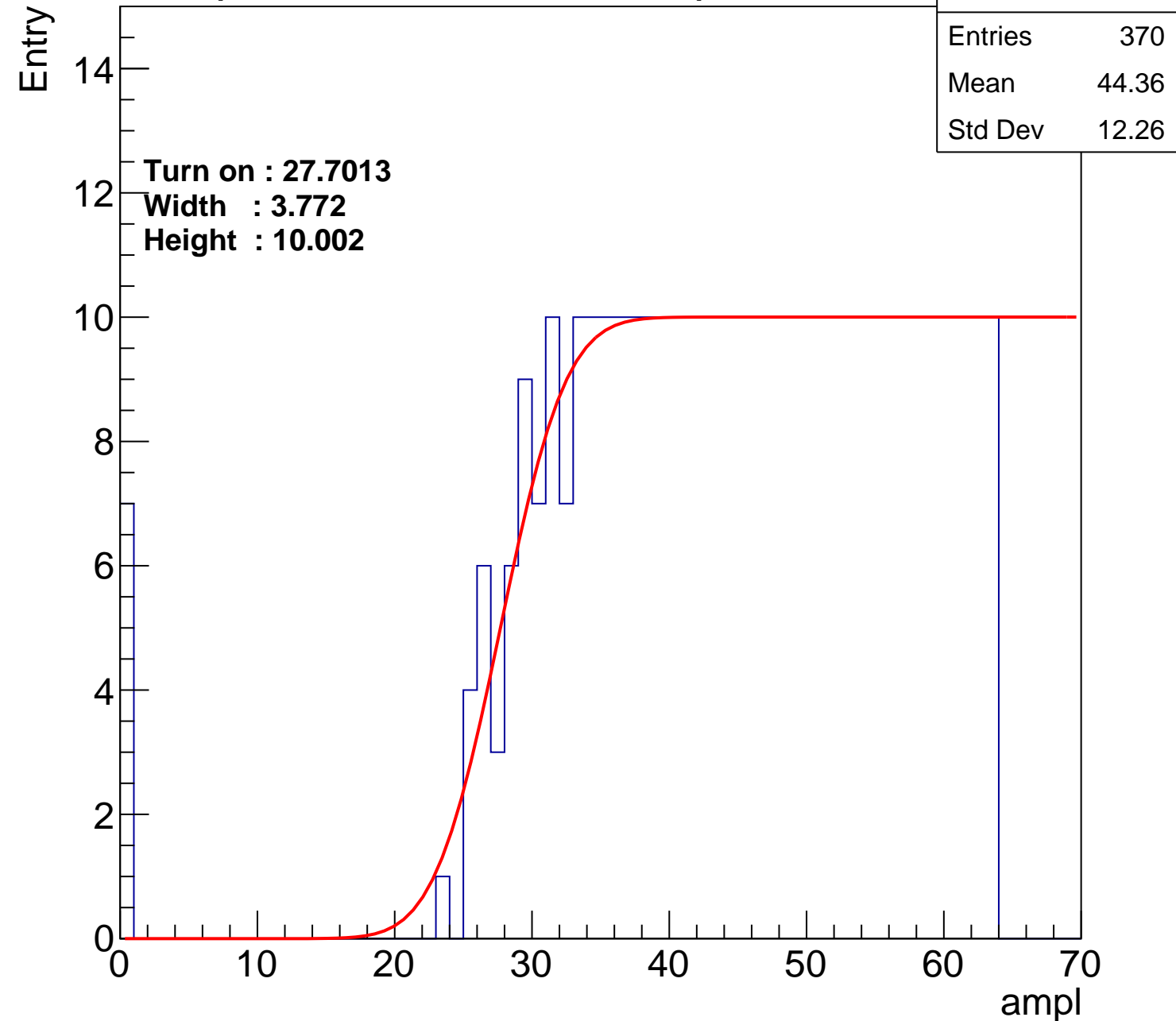
Width : 3.772

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch87

calib_packv5_042523_0143.root, FC#0, port D2

Entries	366
Mean	44.8
Std Dev	11.57

Turn on : 28.3056

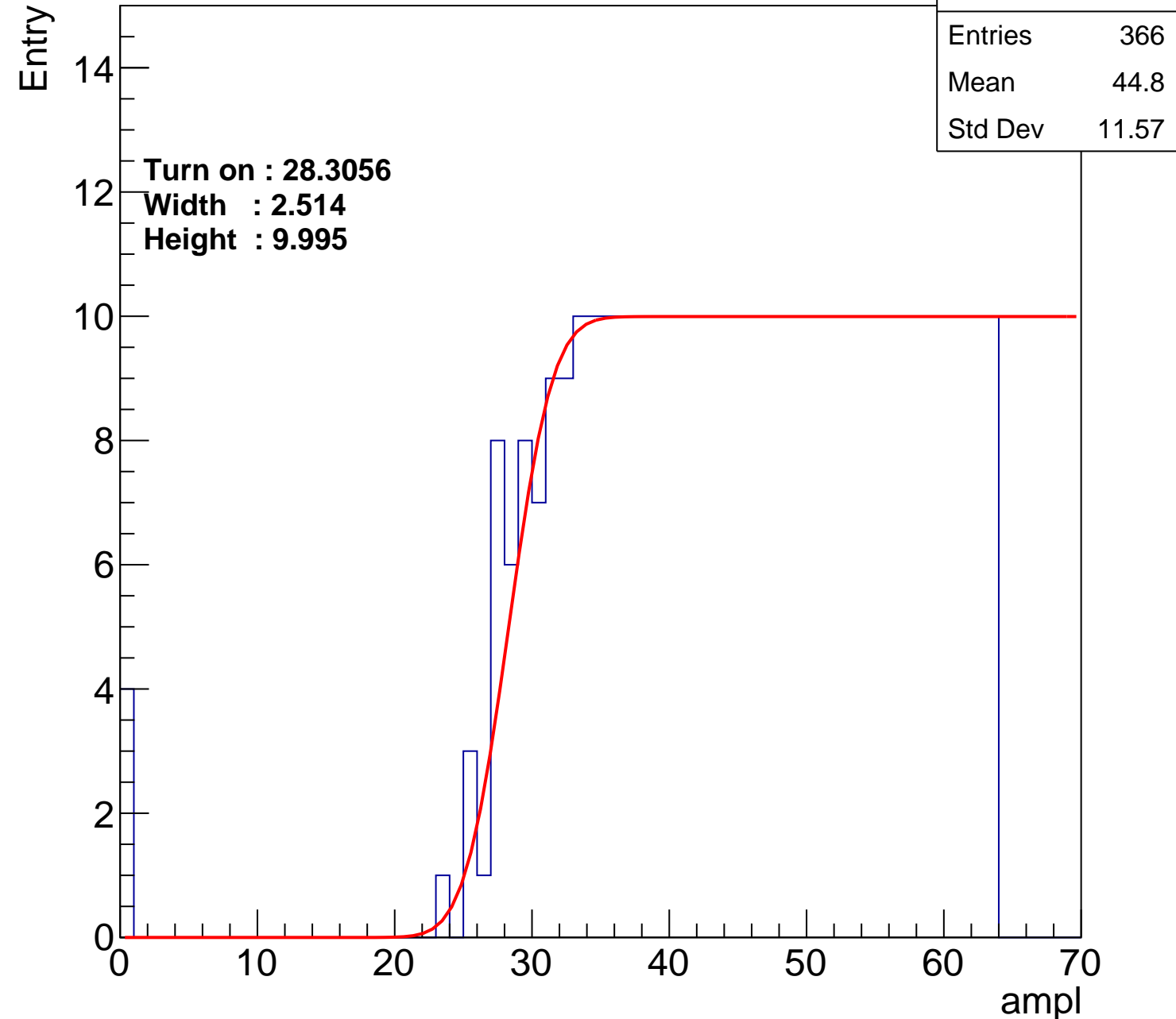
Width : 2.514

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch88

calib_packv5_042523_0143.root, FC#0, port D2

Entries	356
Mean	45.28
Std Dev	11.25

Turn on : 29.1758

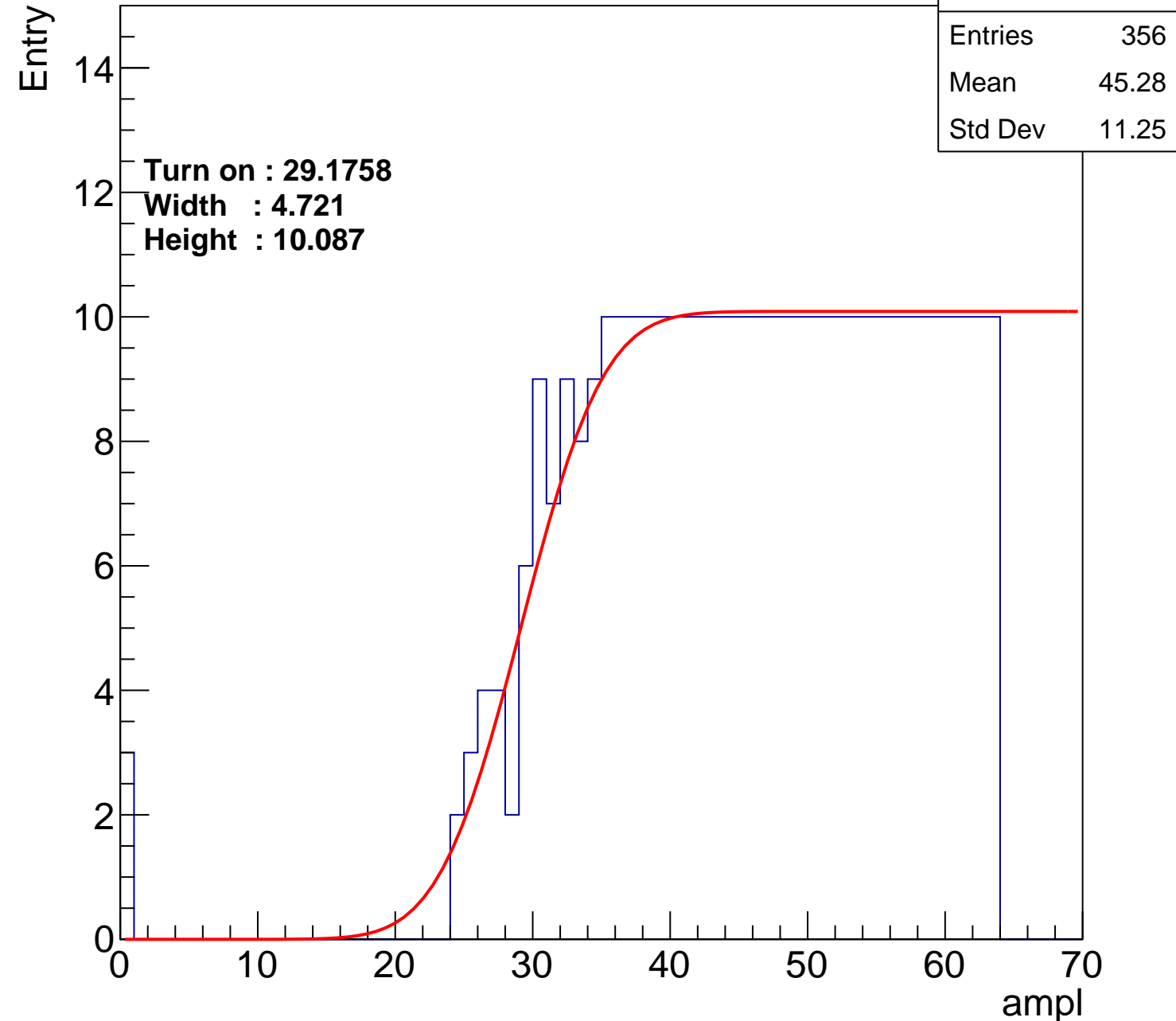
Width : 4.721

Height : 10.087

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch89

calib_packv5_042523_0143.root, FC#0, port D2

Entries	356
Mean	45.16
Std Dev	11.73

Turn on : 29.3400

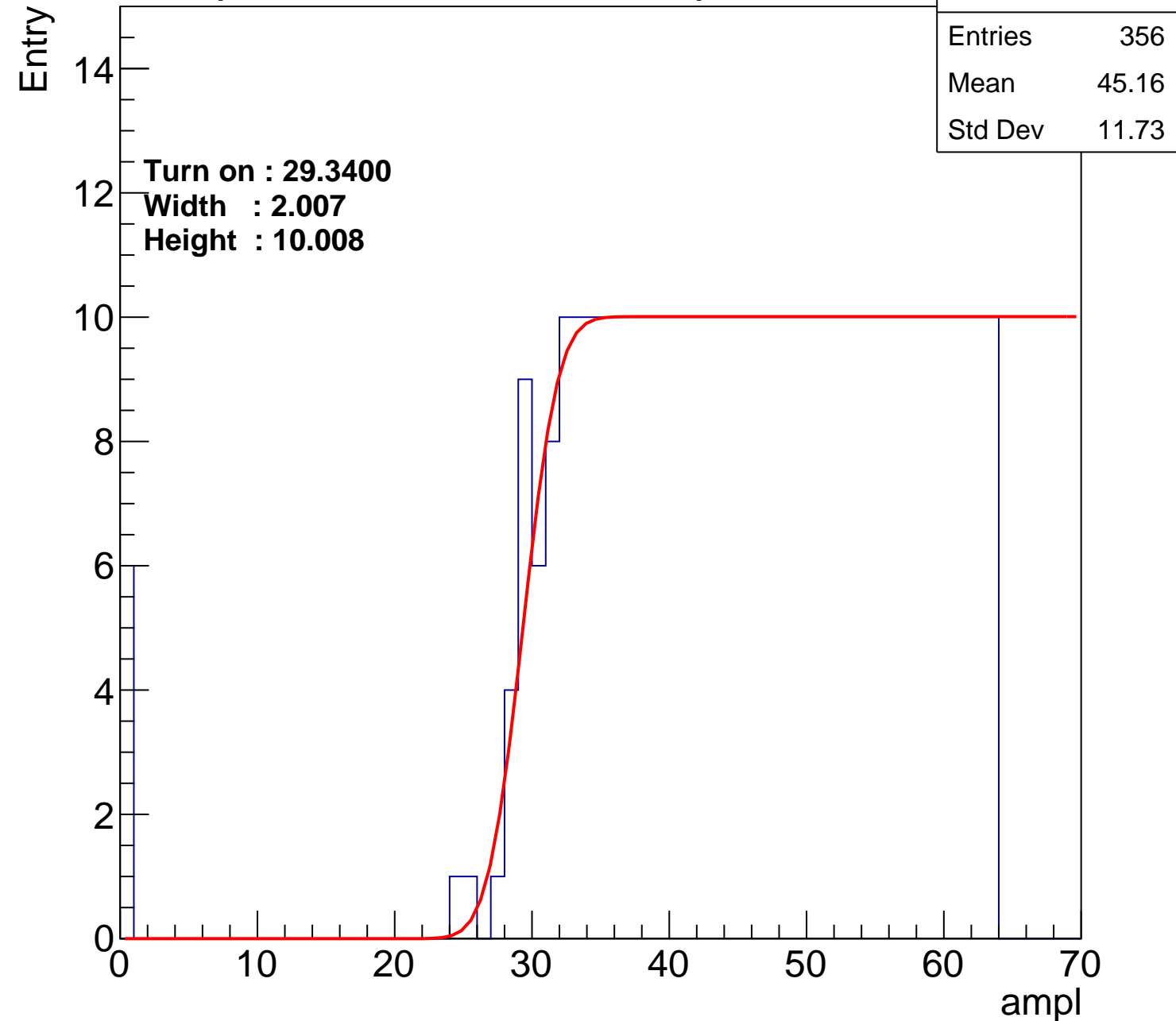
Width : 2.007

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch90

calib_packv5_042523_0143.root, FC#0, port D2

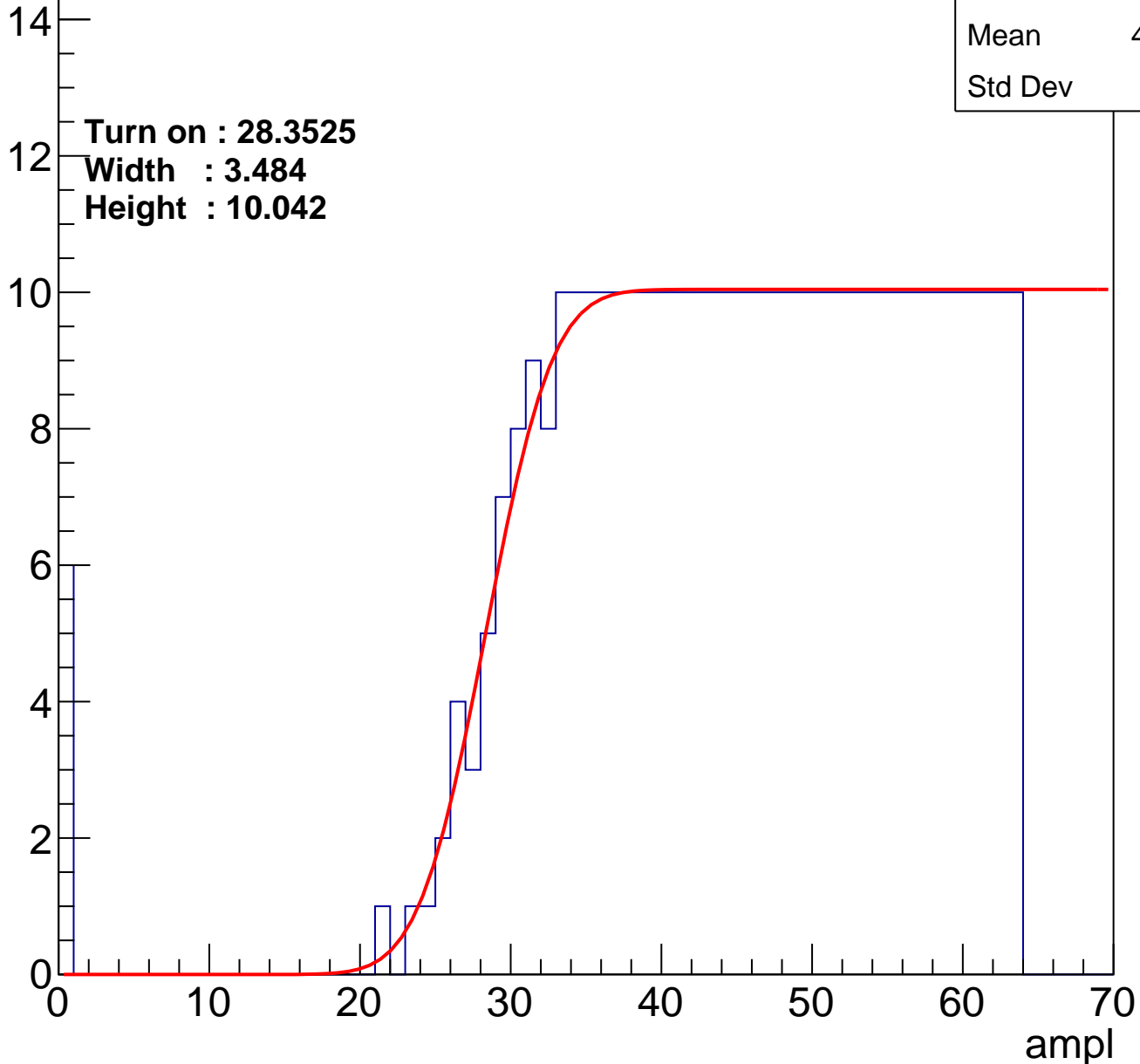
Entries	365
Mean	44.66
Std Dev	12

Turn on : 28.3525

Width : 3.484

Height : 10.042

Entry



B1L101S, U24-ch91

calib_packv5_042523_0143.root, FC#0, port D2

Entries	352
Mean	45.57
Std Dev	11.02

Turn on : 29.1131

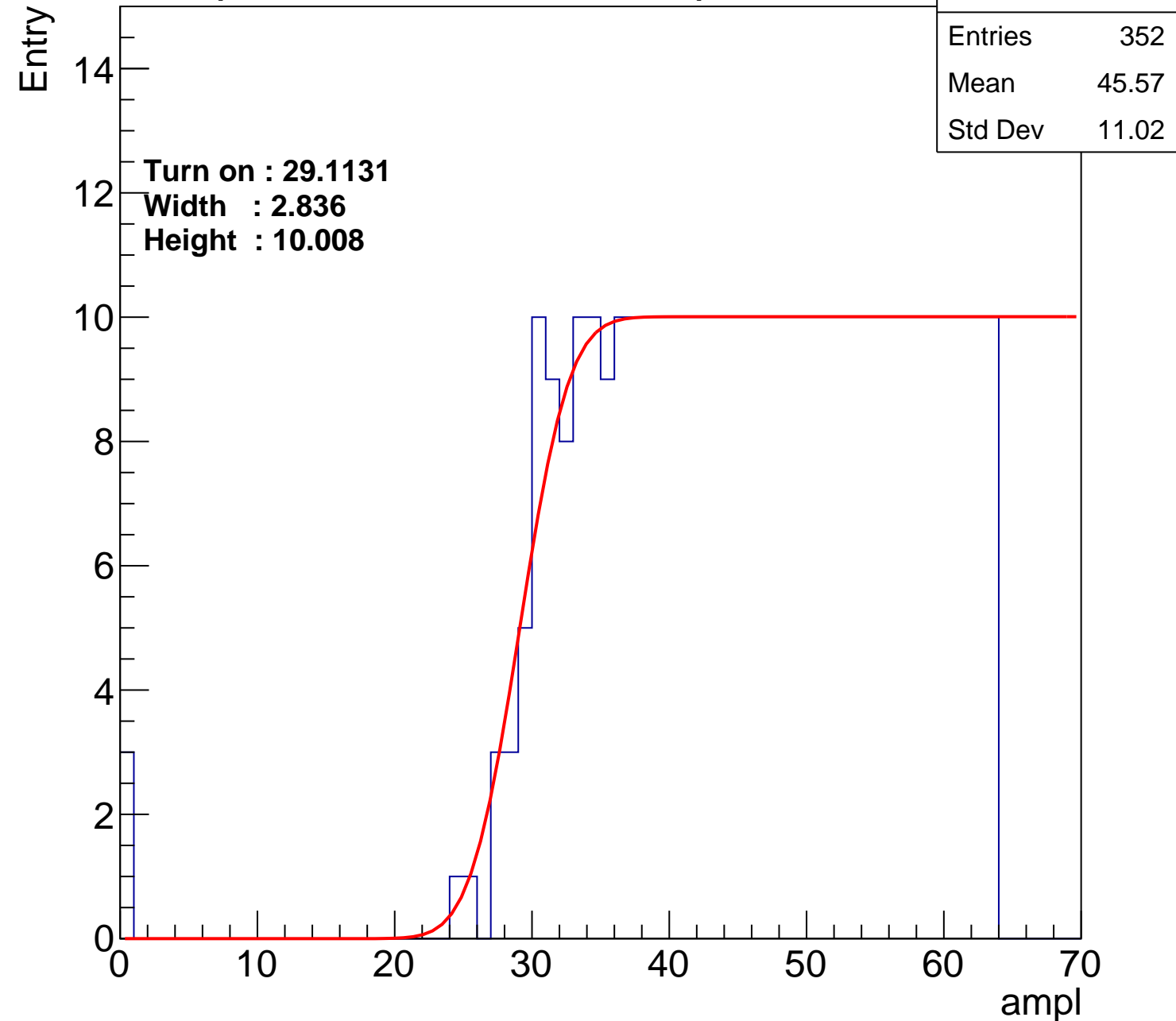
Width : 2.836

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch92

calib_packv5_042523_0143.root, FC#0, port D2

Entries	363
Mean	44.99
Std Dev	11.51

Turn on : 28.7748

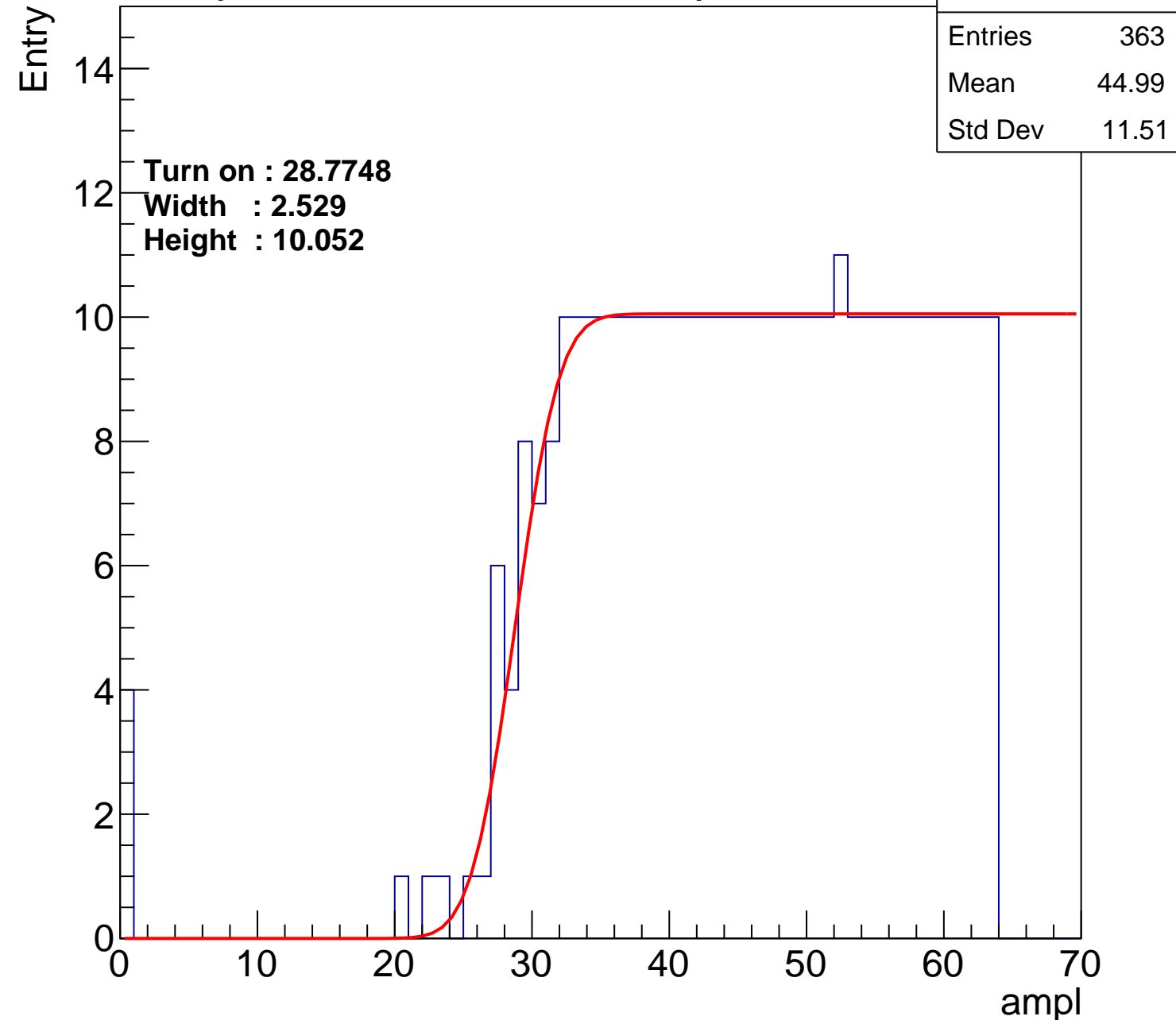
Width : 2.529

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch93

calib_packv5_042523_0143.root, FC#0, port D2

Entries	363
Mean	45.05
Std Dev	11.25

Turn on : 27.9021

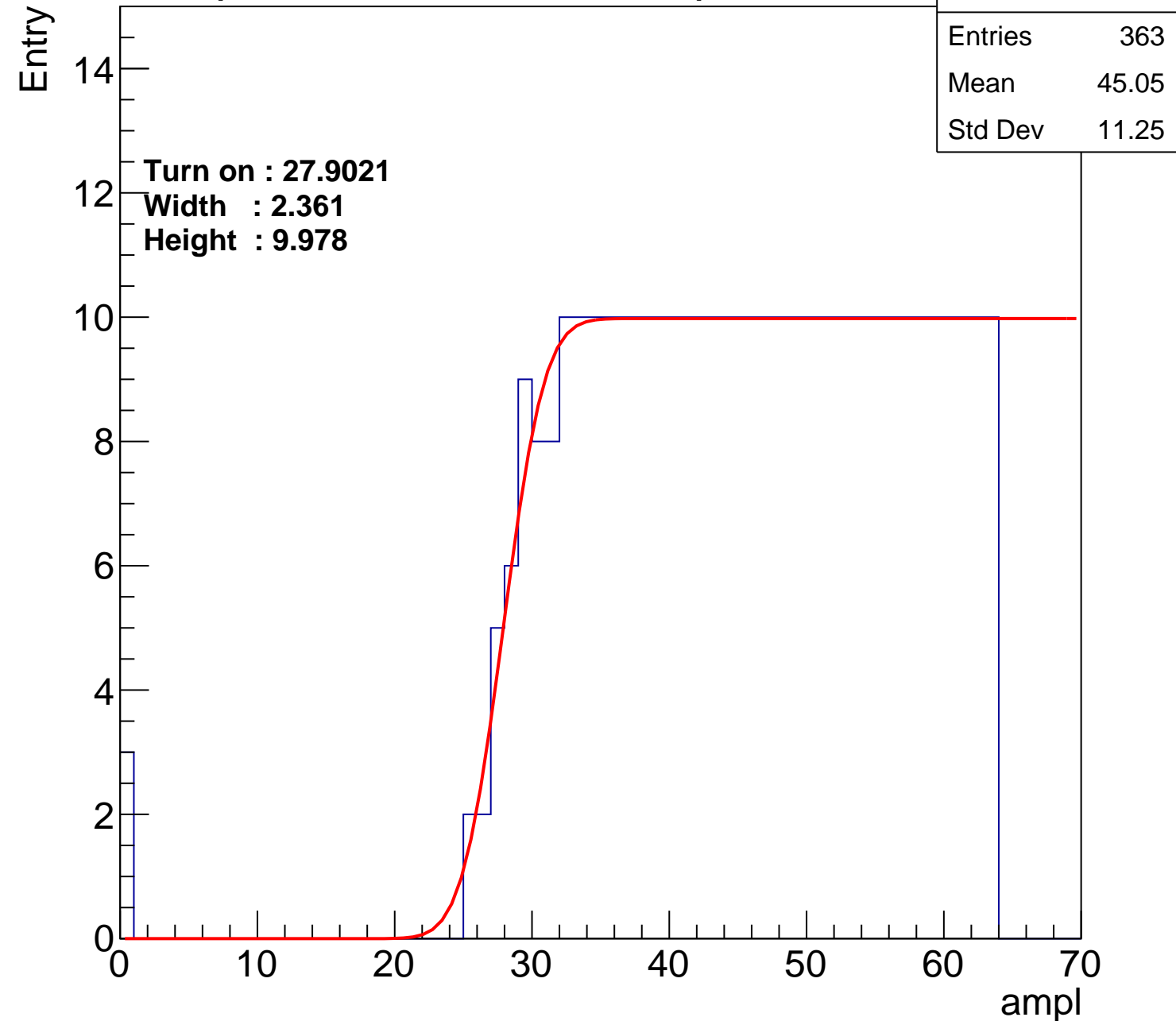
Width : 2.361

Height : 9.978

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch94

calib_packv5_042523_0143.root, FC#0, port D2

Entries	363
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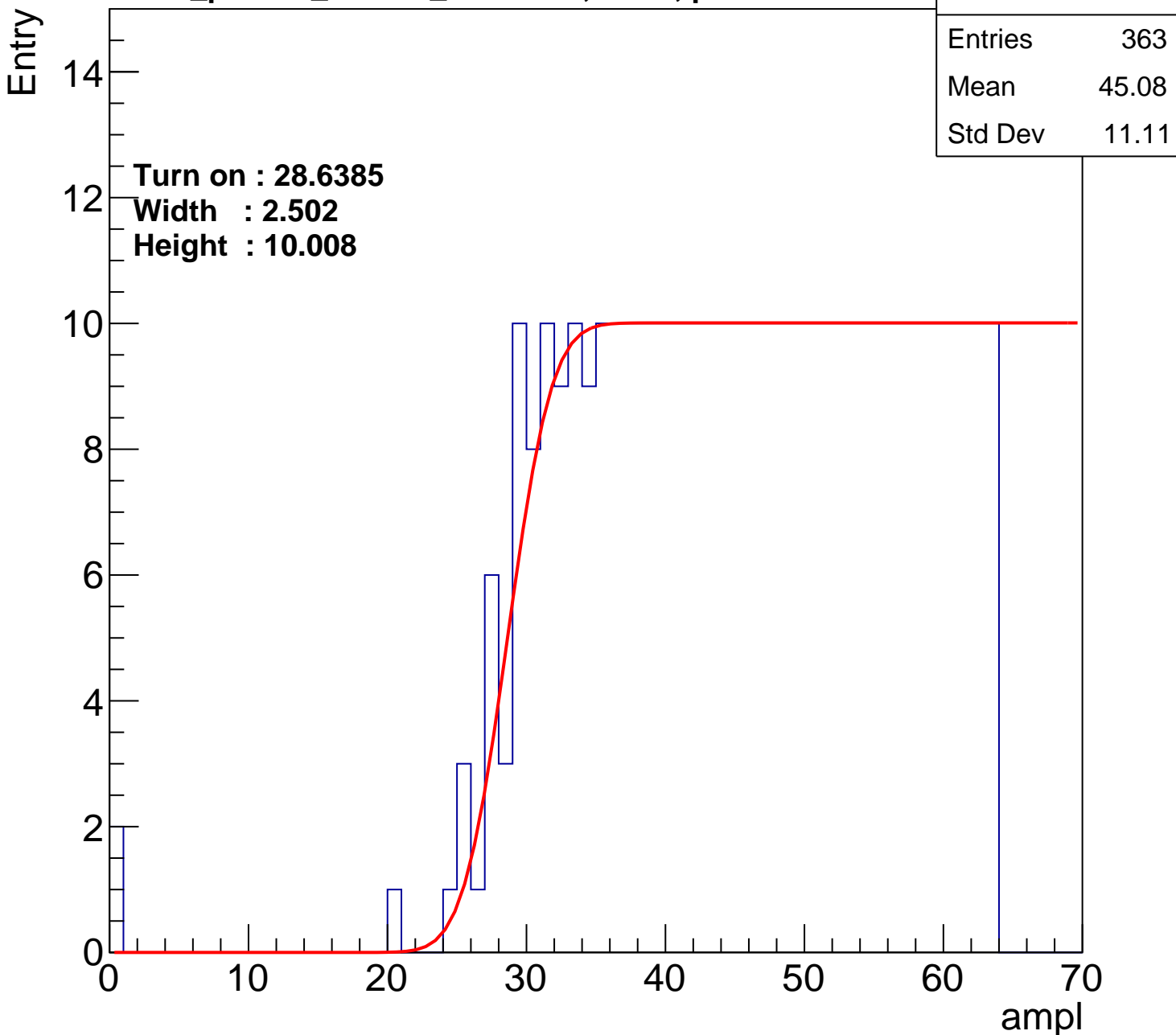
Mean	45.08
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Std Dev	11.11
---------	-------

Turn on : 28.6385

Width : 2.502

Height : 10.008



B1L101S, U24-ch95

calib_packv5_042523_0143.root, FC#0, port D2

Entries	369
Mean	44.66
Std Dev	11.63

Turn on : 27.9270

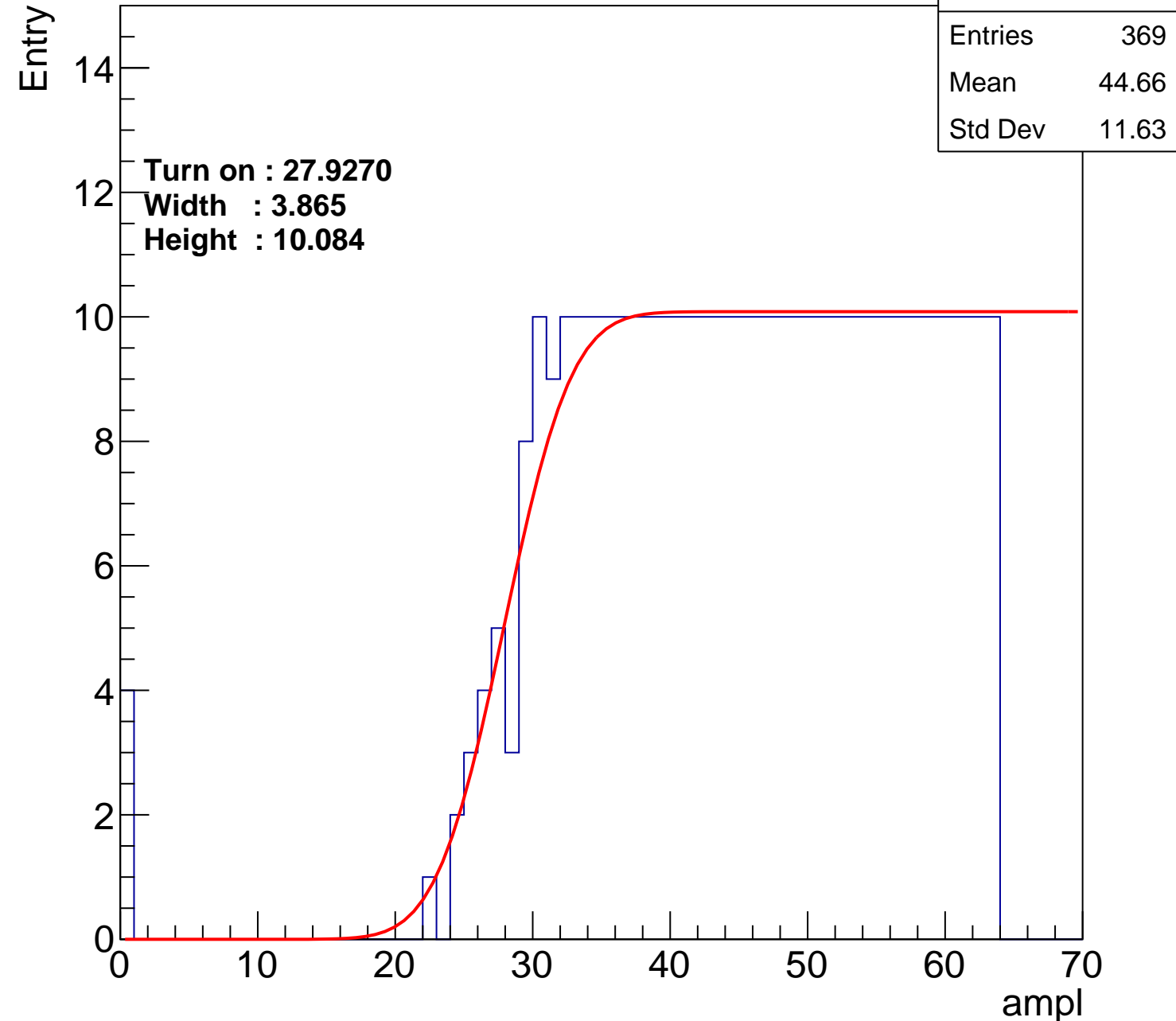
Width : 3.865

Height : 10.084

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch96

calib_packv5_042523_0143.root, FC#0, port D2

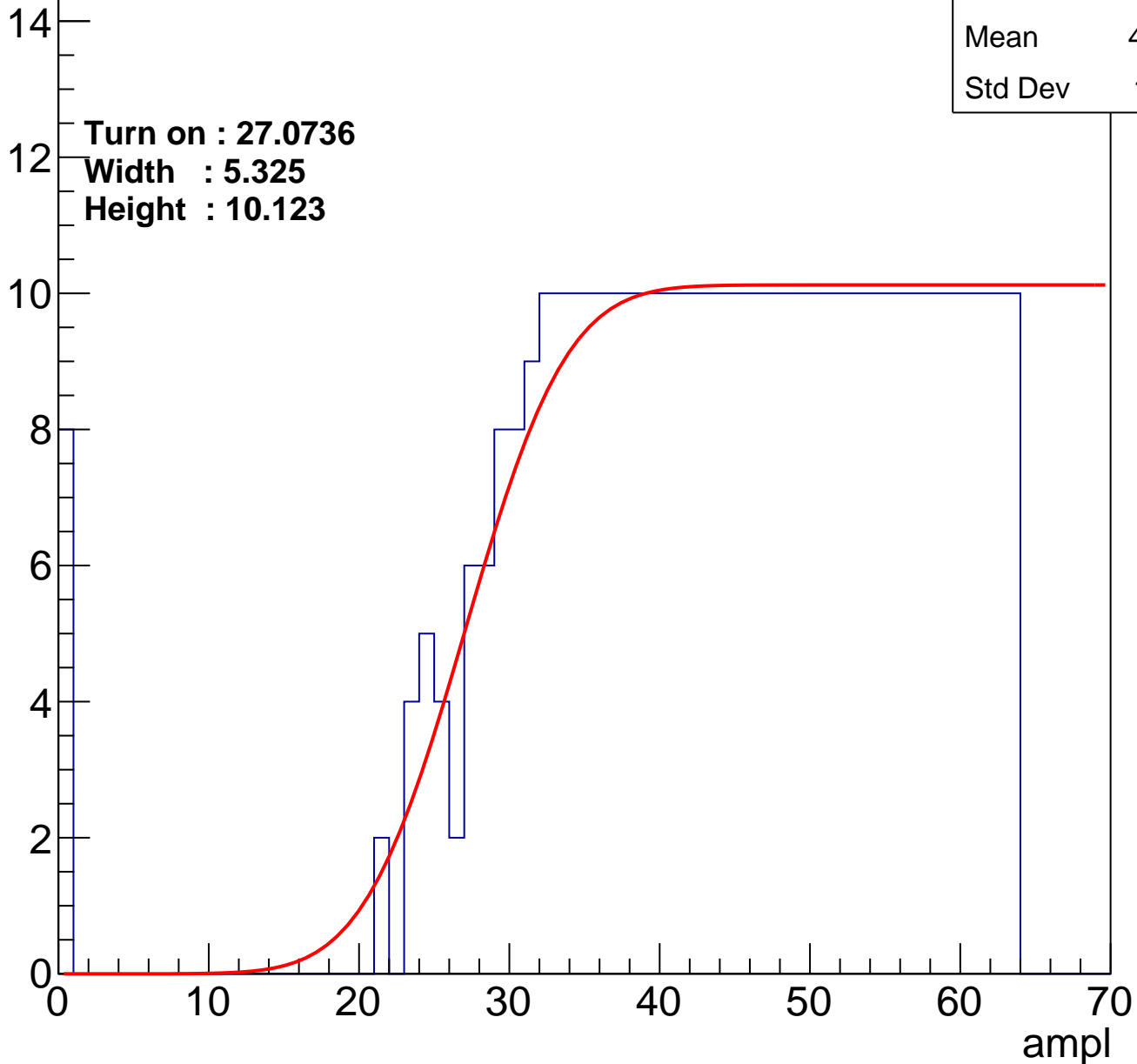
Entries	382
Mean	43.68
Std Dev	12.71

Turn on : 27.0736

Width : 5.325

Height : 10.123

Entry



B1L101S, U24-ch97

calib_packv5_042523_0143.root, FC#0, port D2

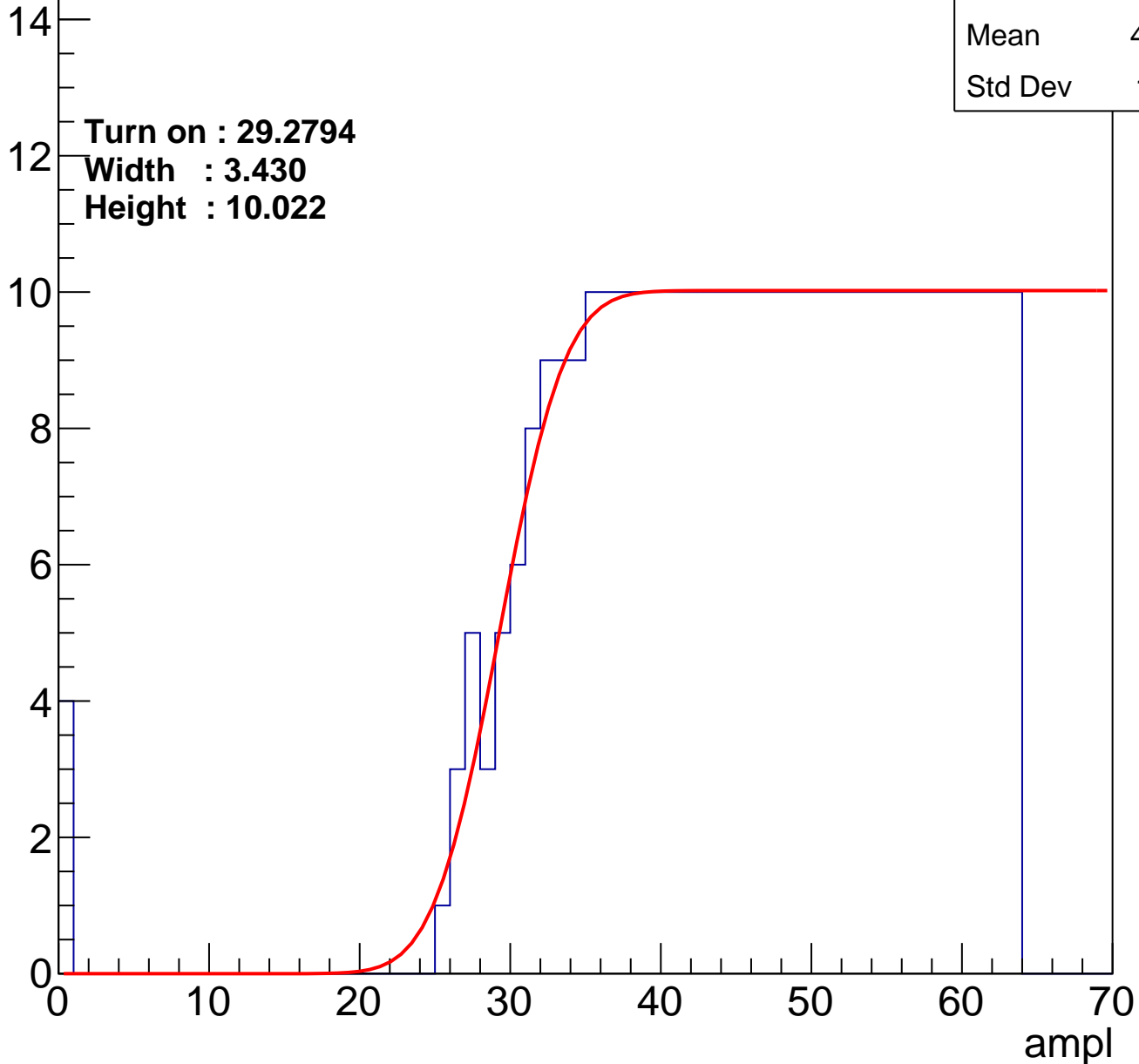
Entries	352
Mean	45.44
Std Dev	11.31

Turn on : 29.2794

Width : 3.430

Height : 10.022

Entry



B1L101S, U24-ch98

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	43.99
Std Dev	12.57

Turn on : 27.5708

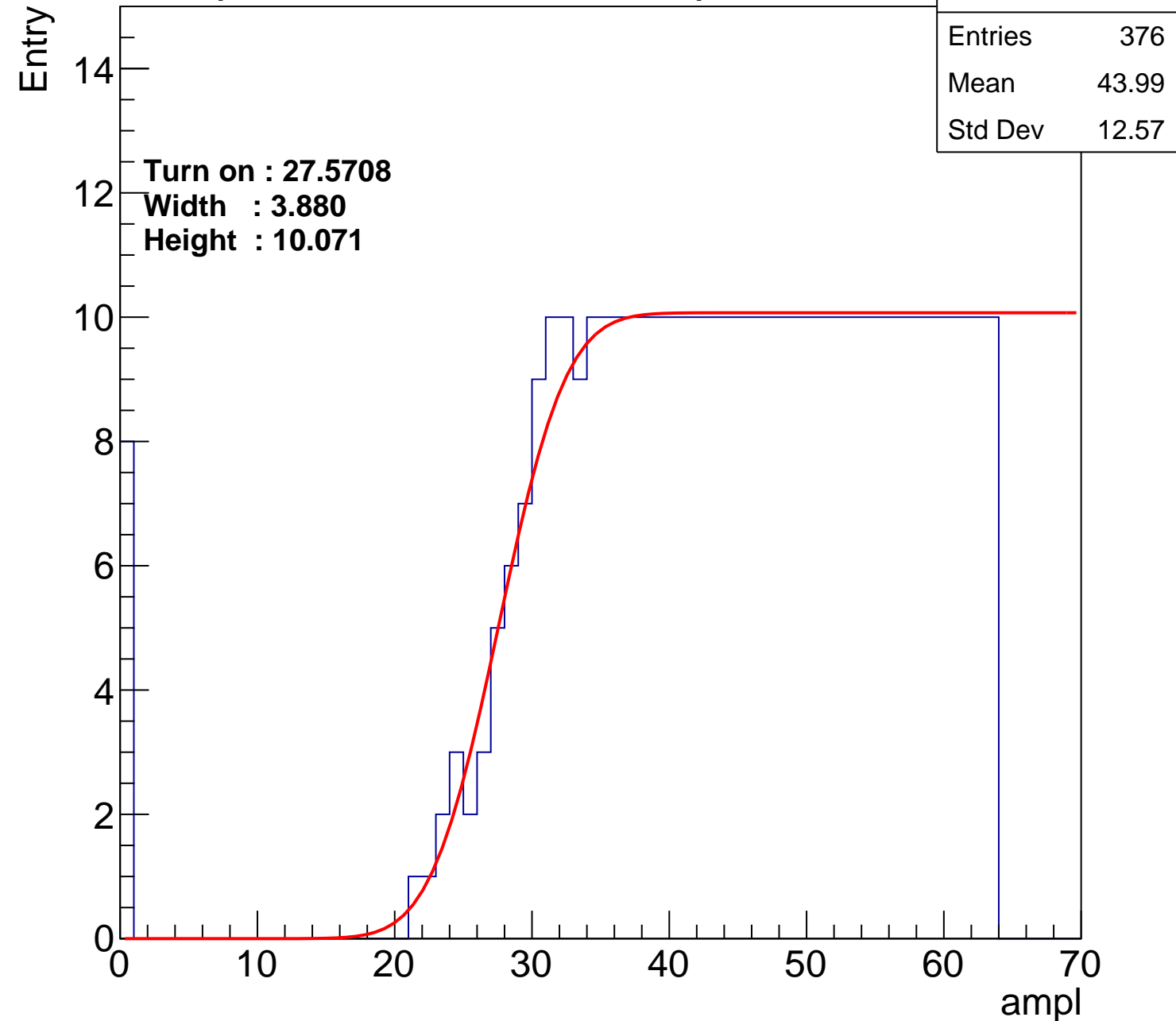
Width : 3.880

Height : 10.071

Entry

14
12
10
8
6
4
2
0

ampl



calib_packv5_042523_0143.root, FC#0, port D2

calib_packv5_042523_0143.root, FC#0, port D2

Turn on : 28.3951
Width : 2.746
Height : 10.009



B1L101S, U24-ch100

calib_packv5_042523_0143.root, FC#0, port D2

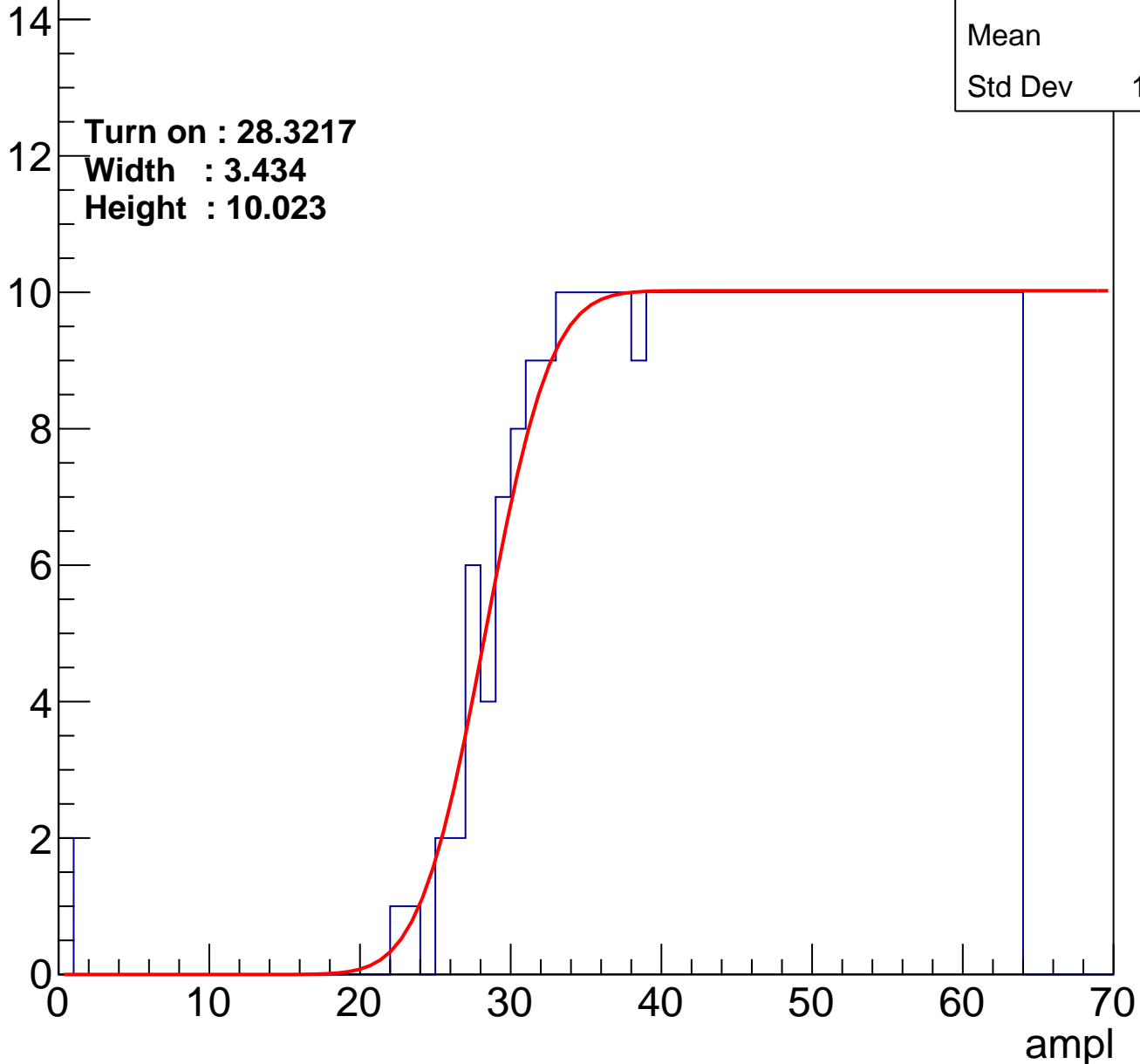
Entries	360
Mean	45.2
Std Dev	11.07

Turn on : 28.3217

Width : 3.434

Height : 10.023

Entry



B1L101S, U24-ch101

calib_packv5_042523_0143.root, FC#0, port D2

Entries	371
Mean	44.51
Std Dev	11.84

Turn on : 27.7357

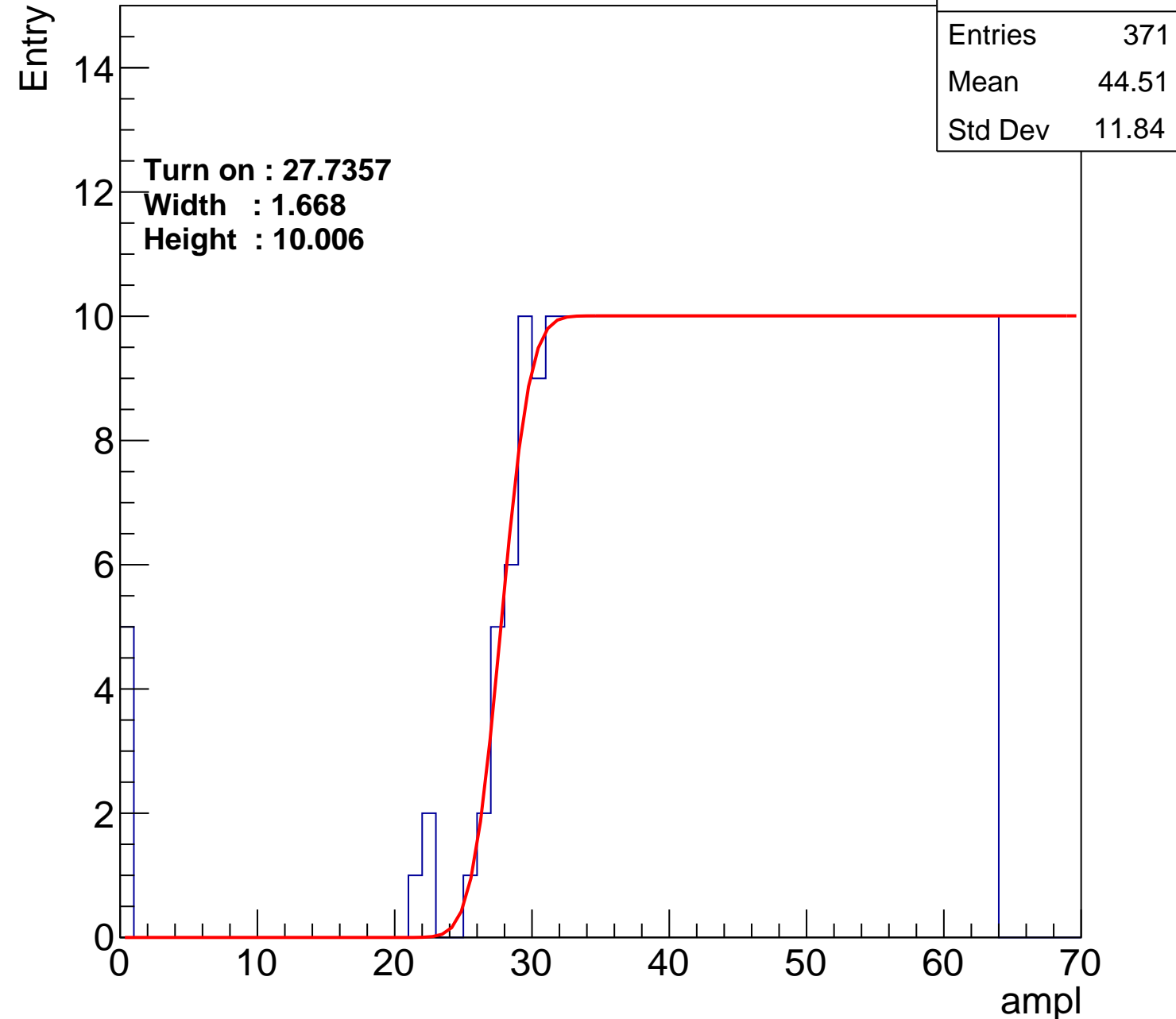
Width : 1.668

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch102

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.28
Std Dev	11.85

Turn on : 26.3883

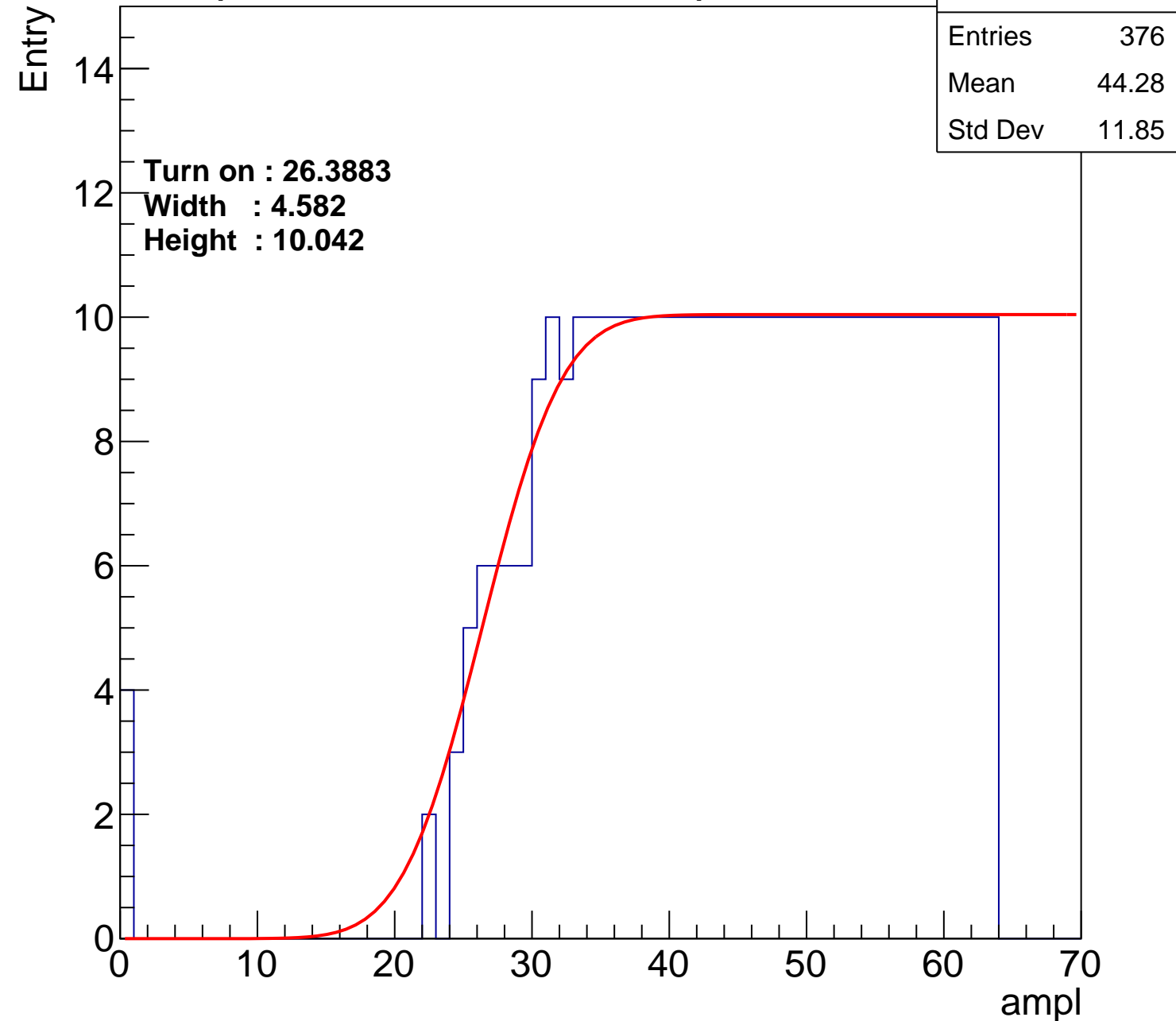
Width : 4.582

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch103

calib_packv5_042523_0143.root, FC#0, port D2

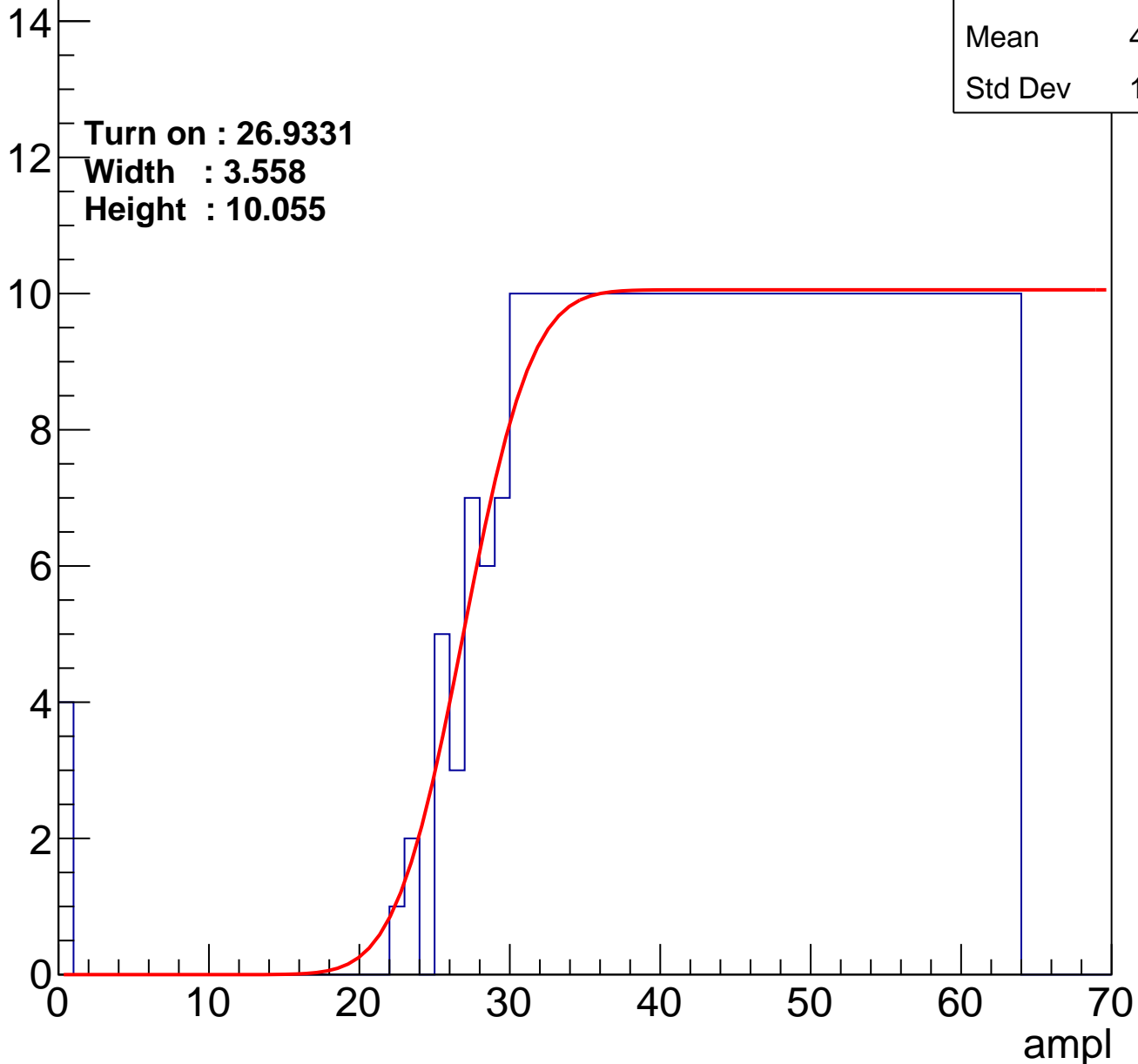
Entries	375
Mean	44.38
Std Dev	11.76

Turn on : 26.9331

Width : 3.558

Height : 10.055

Entry



B1L101S, U24-ch104

calib_packv5_042523_0143.root, FC#0, port D2

Entries	359
Mean	45.08
Std Dev	11.52

Turn on : 28.7936

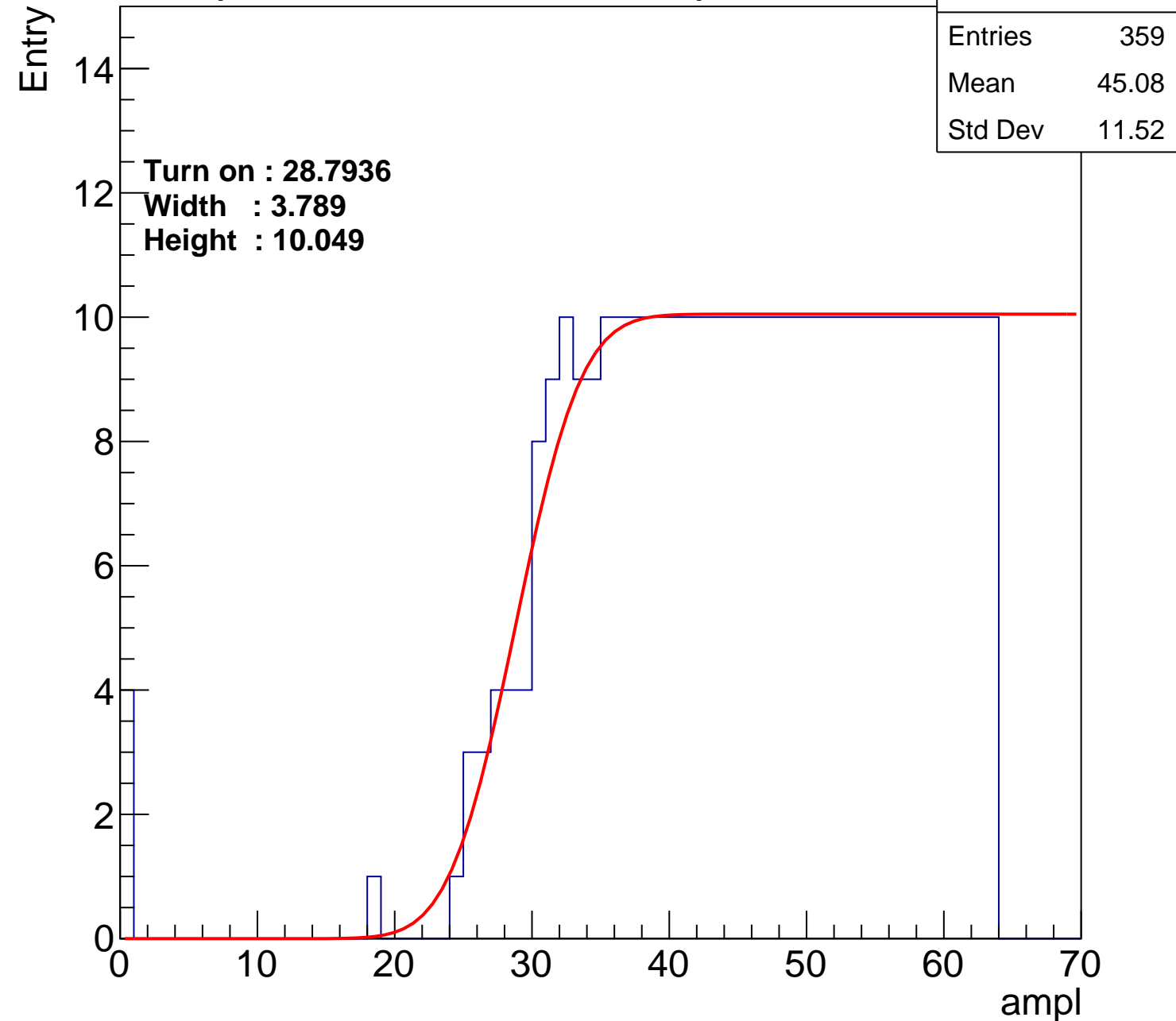
Width : 3.789

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch105

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.54
Std Dev	11.39

Turn on : 26.7531

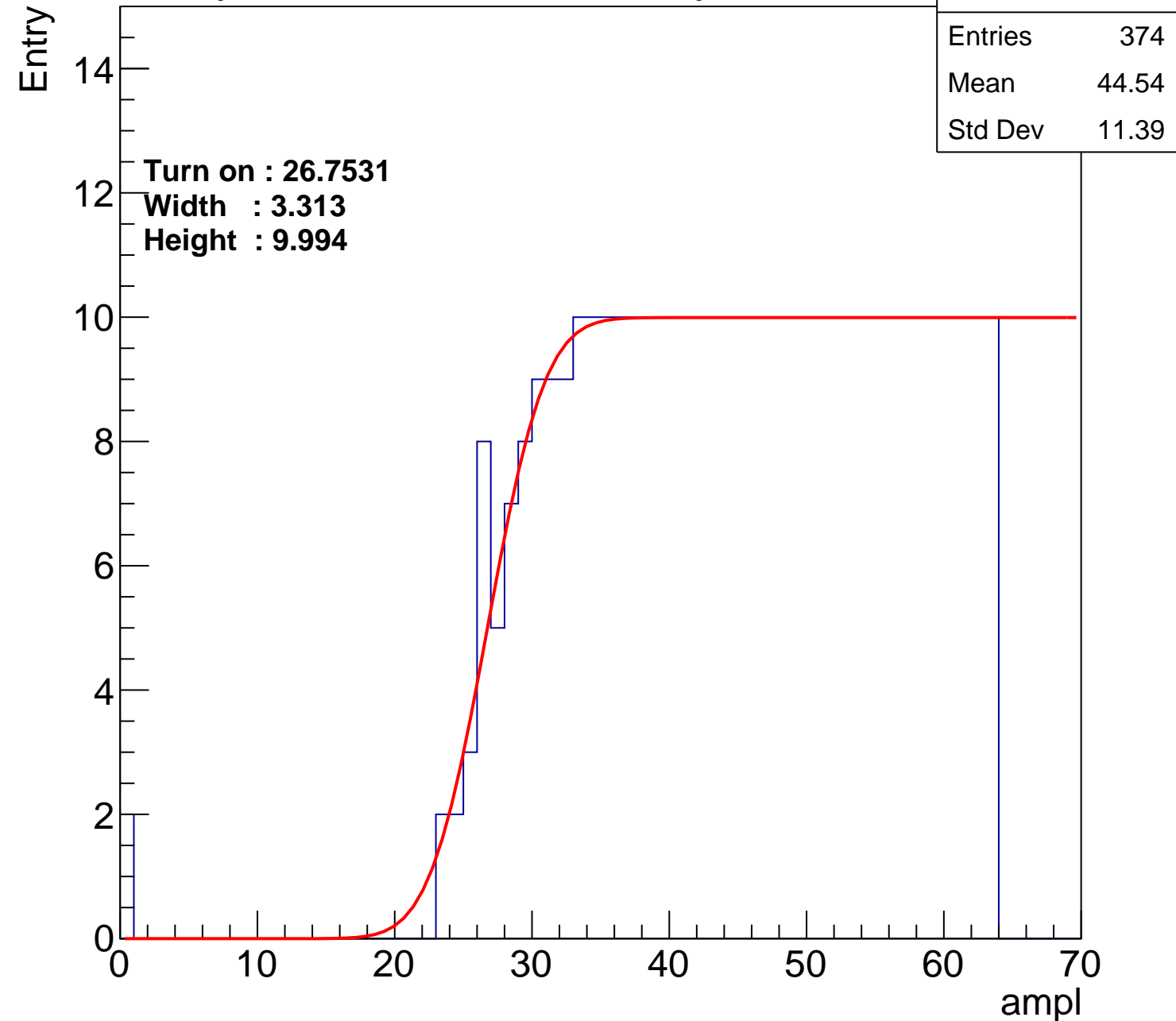
Width : 3.313

Height : 9.994

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch106

calib_packv5_042523_0143.root, FC#0, port D2

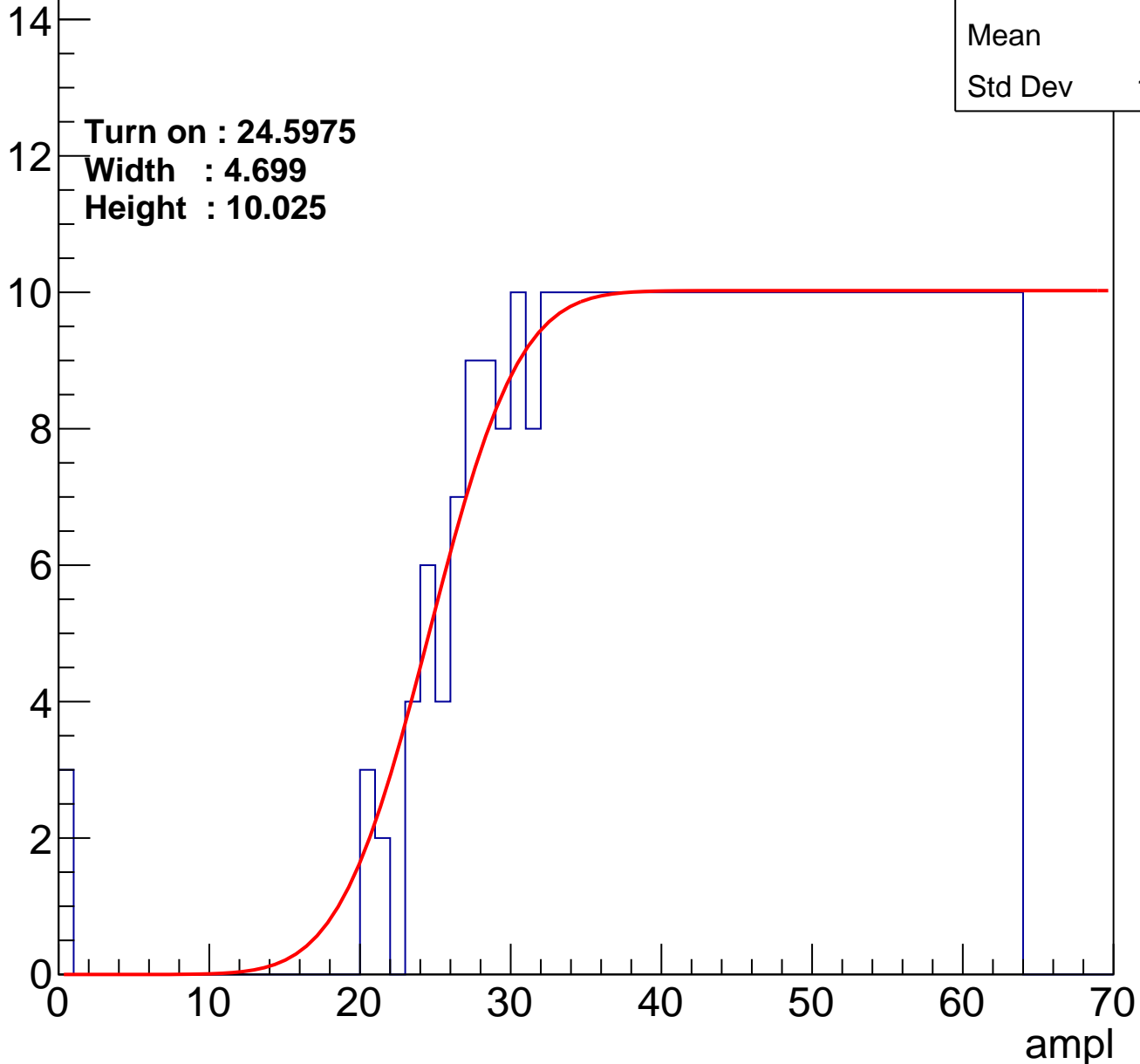
Entries	393
Mean	43.5
Std Dev	12.11

Turn on : 24.5975

Width : 4.699

Height : 10.025

Entry



B1L101S, U24-ch107

calib_packv5_042523_0143.root, FC#0, port D2

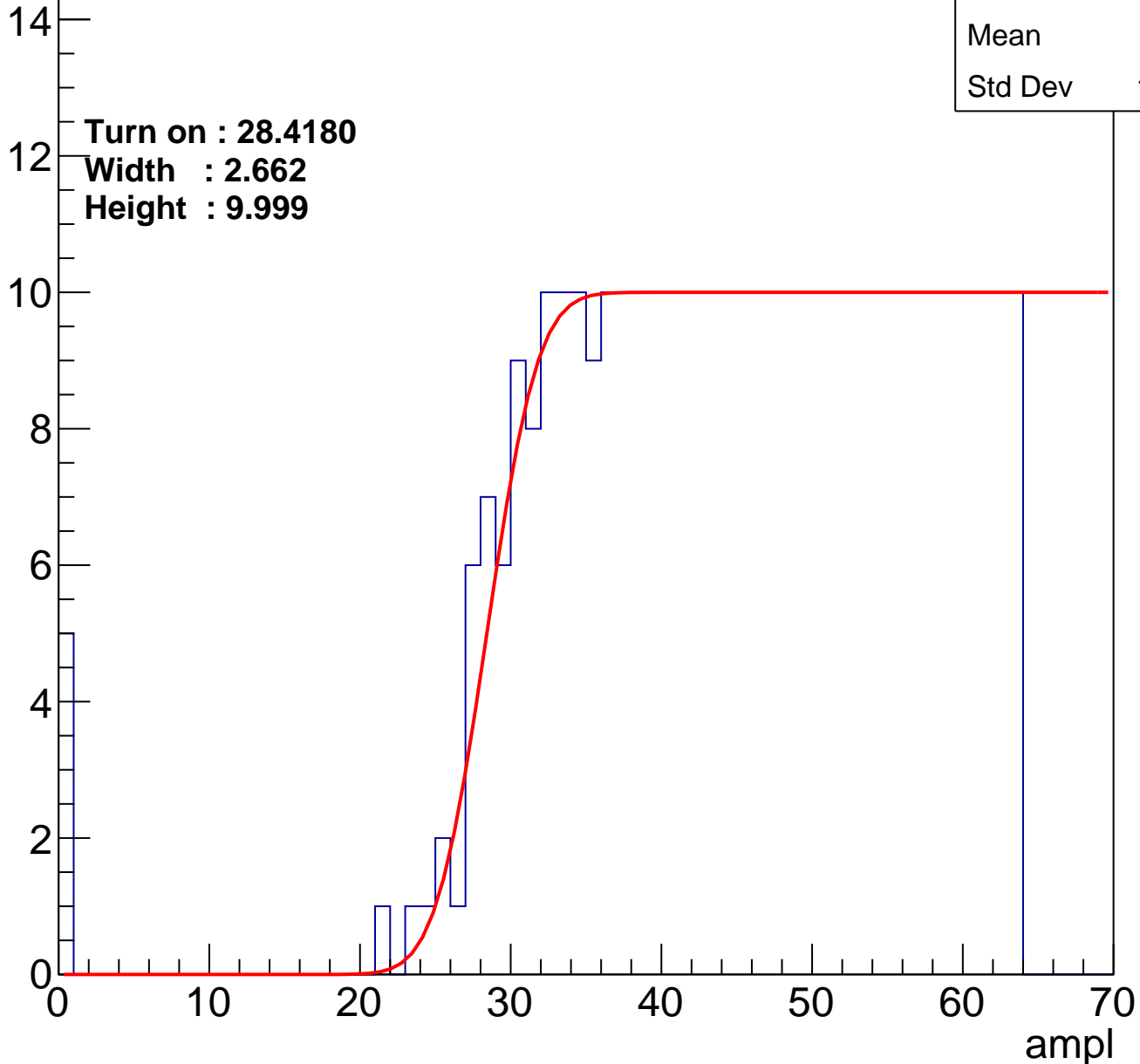
Entries	366
Mean	44.7
Std Dev	11.81

Turn on : 28.4180

Width : 2.662

Height : 9.999

Entry



B1L101S, U24-ch108

calib_packv5_042523_0143.root, FC#0, port D2

Entries	371
Mean	44.68
Std Dev	11.34

Turn on : 27.6425

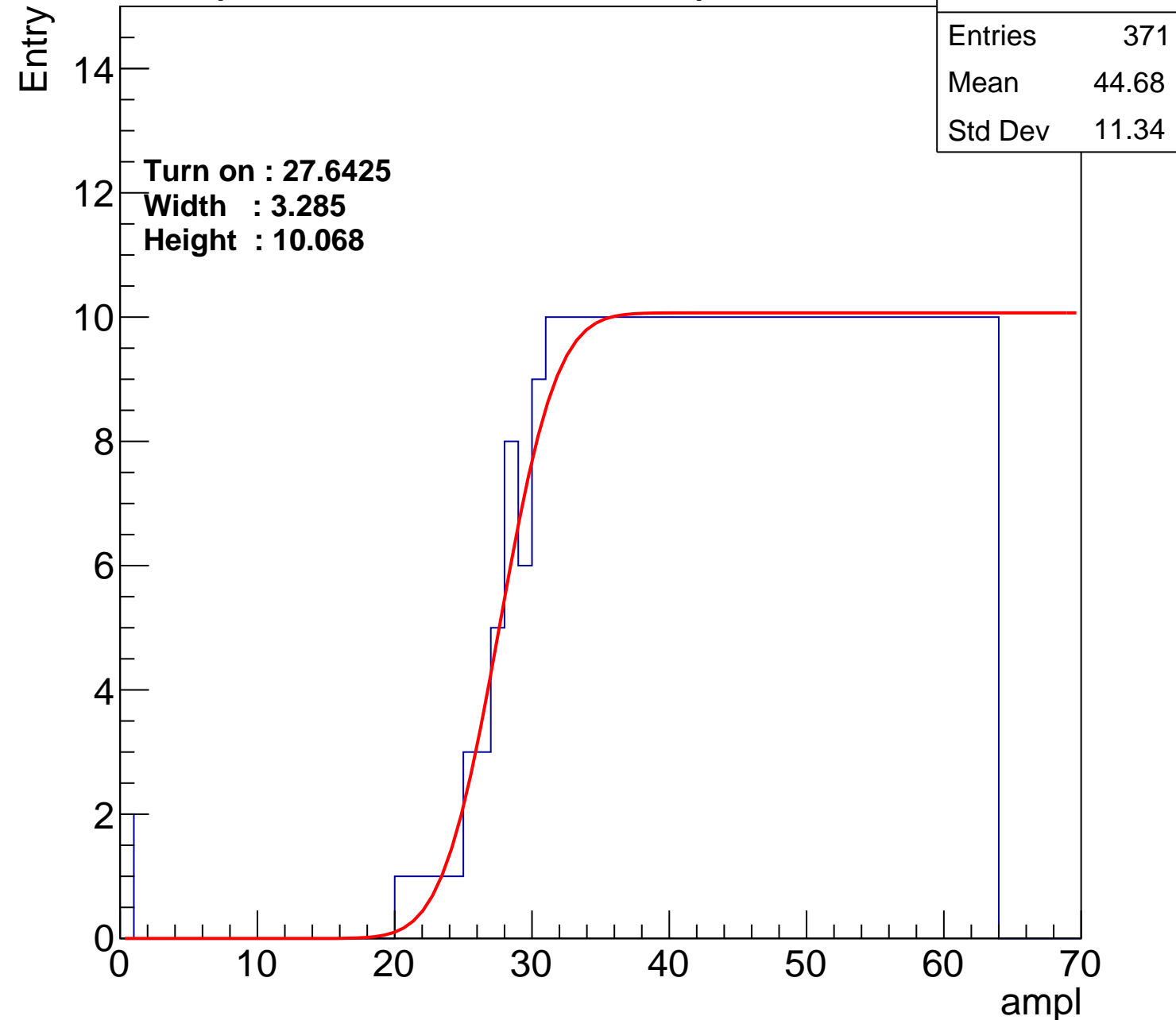
Width : 3.285

Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch109

calib_packv5_042523_0143.root, FC#0, port D2

Entries	364
Mean	44.95
Std Dev	11.35

Turn on : 27.7888

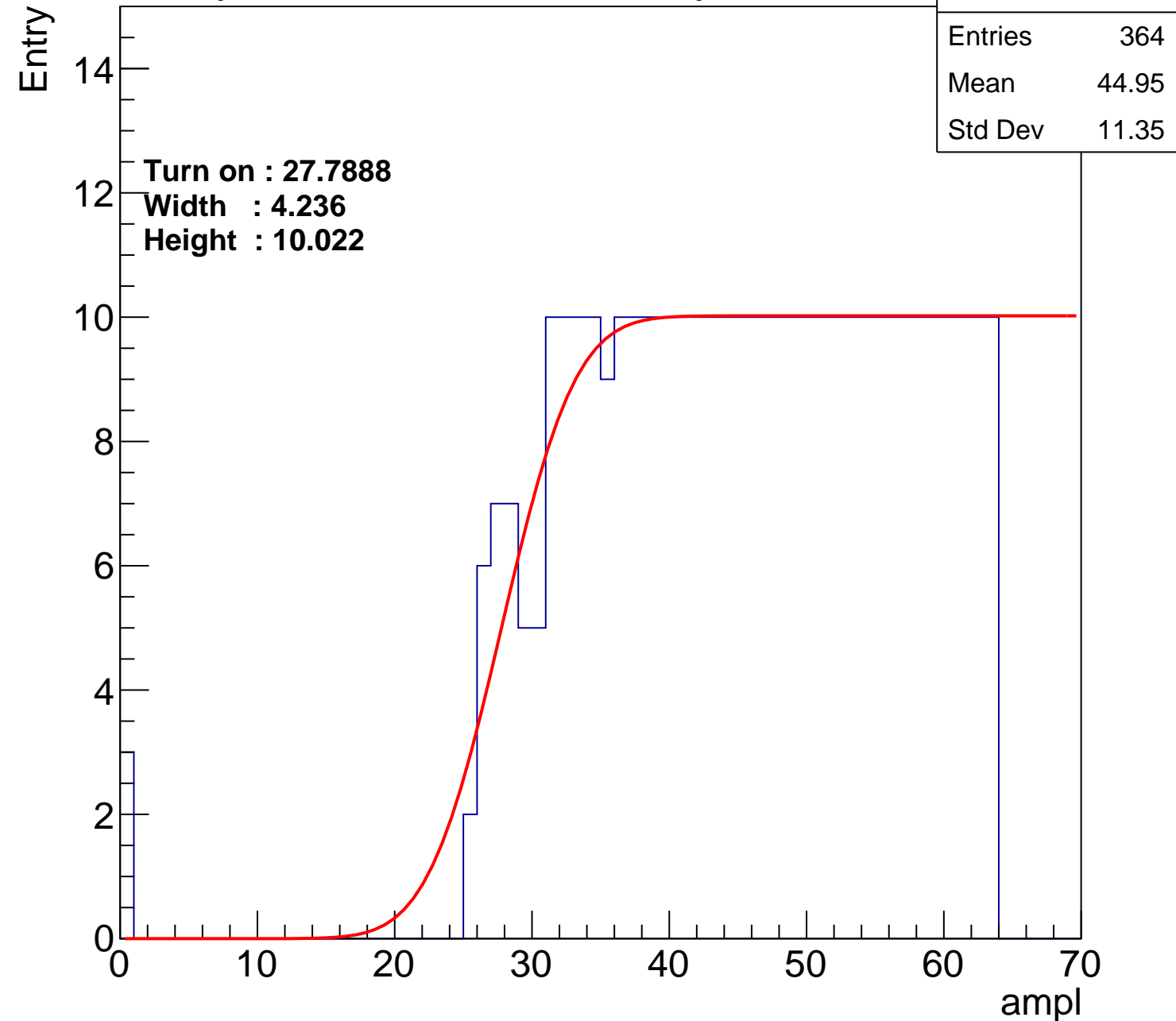
Width : 4.236

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch110

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.4
Std Dev	11.57

Turn on : 26.6576

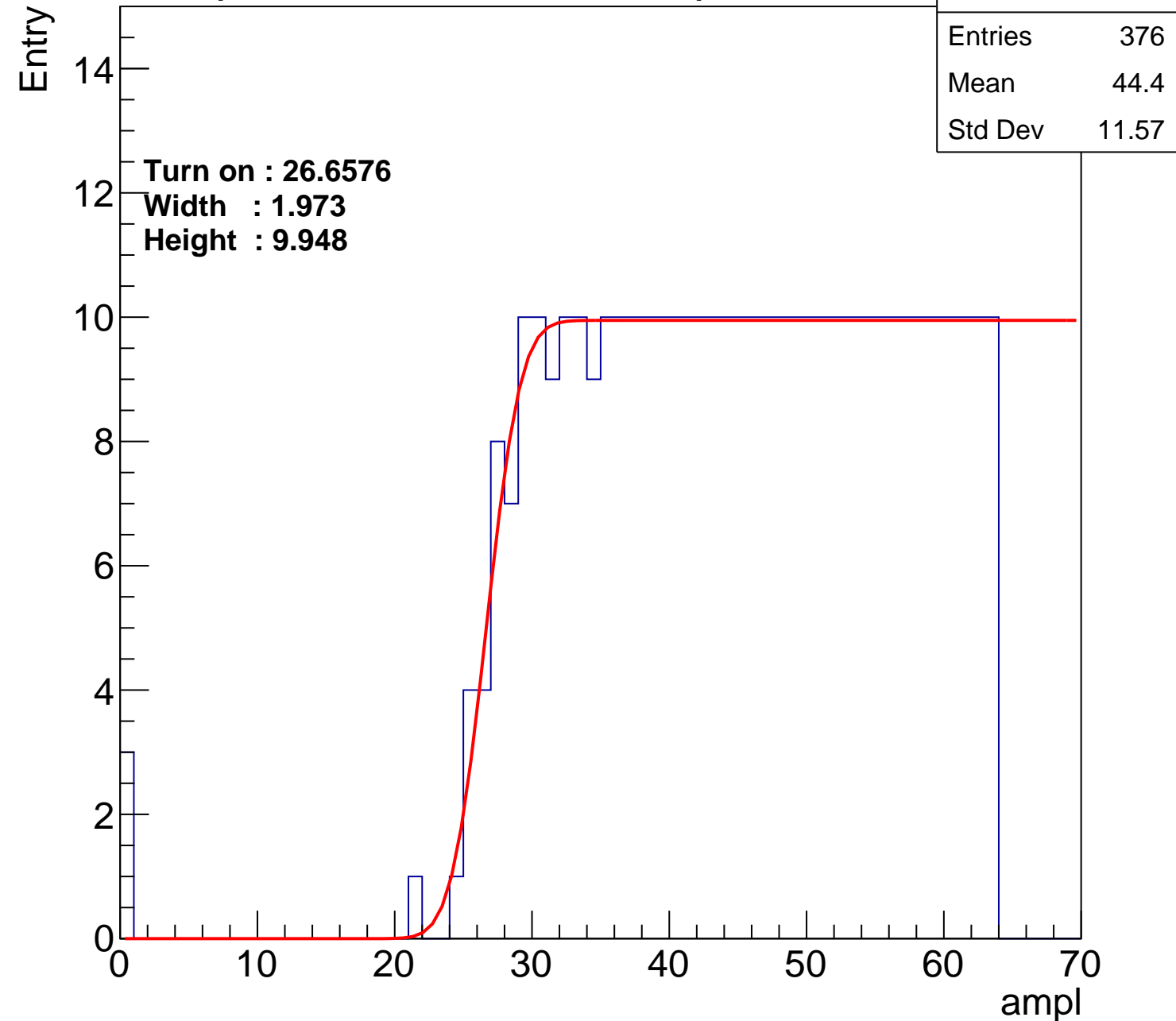
Width : 1.973

Height : 9.948

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch111

calib_packv5_042523_0143.root, FC#0, port D2

Entries	353
Mean	45.53
Std Dev	10.92

Turn on : 28.8663

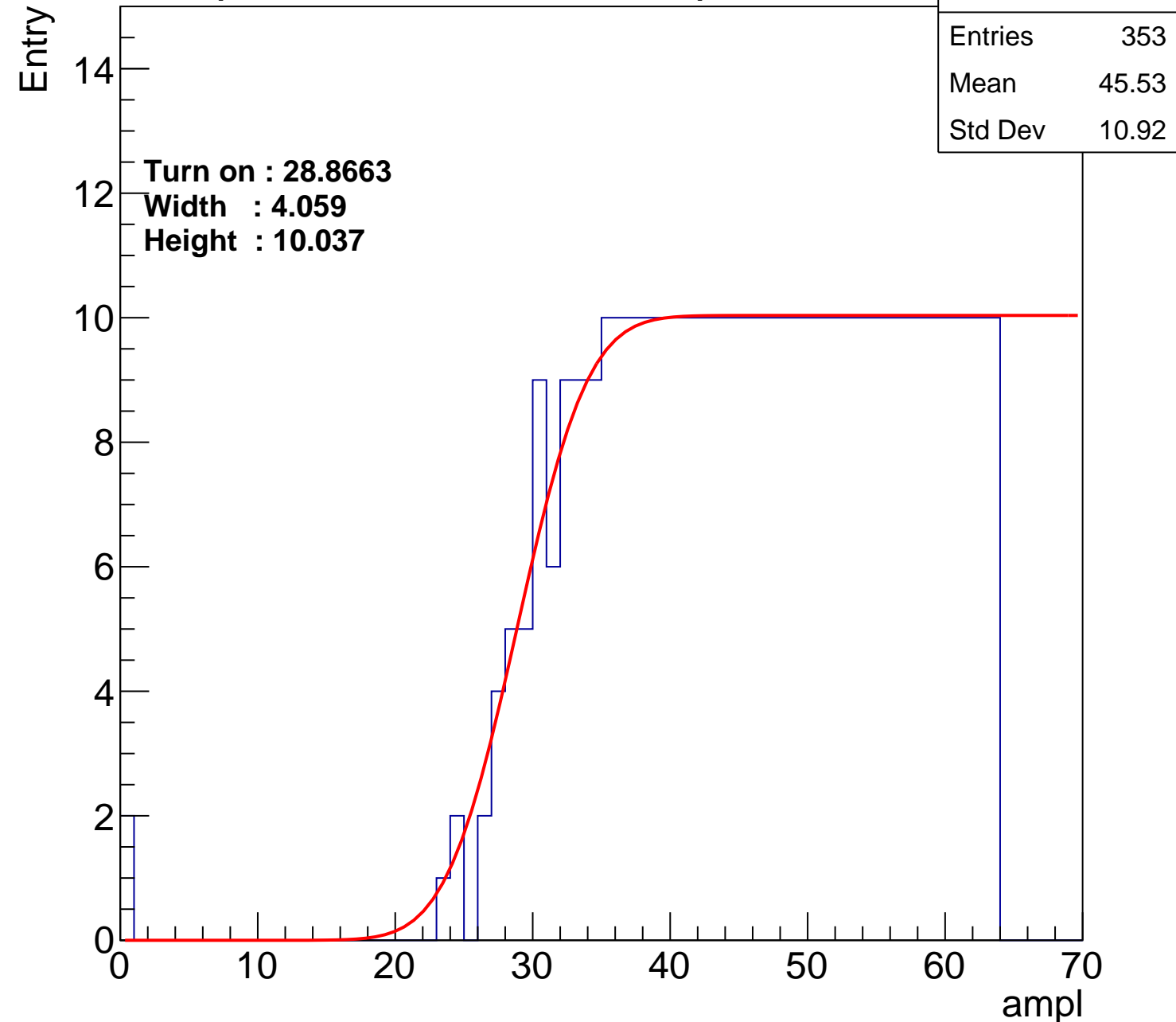
Width : 4.059

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch112

calib_packv5_042523_0143.root, FC#0, port D2

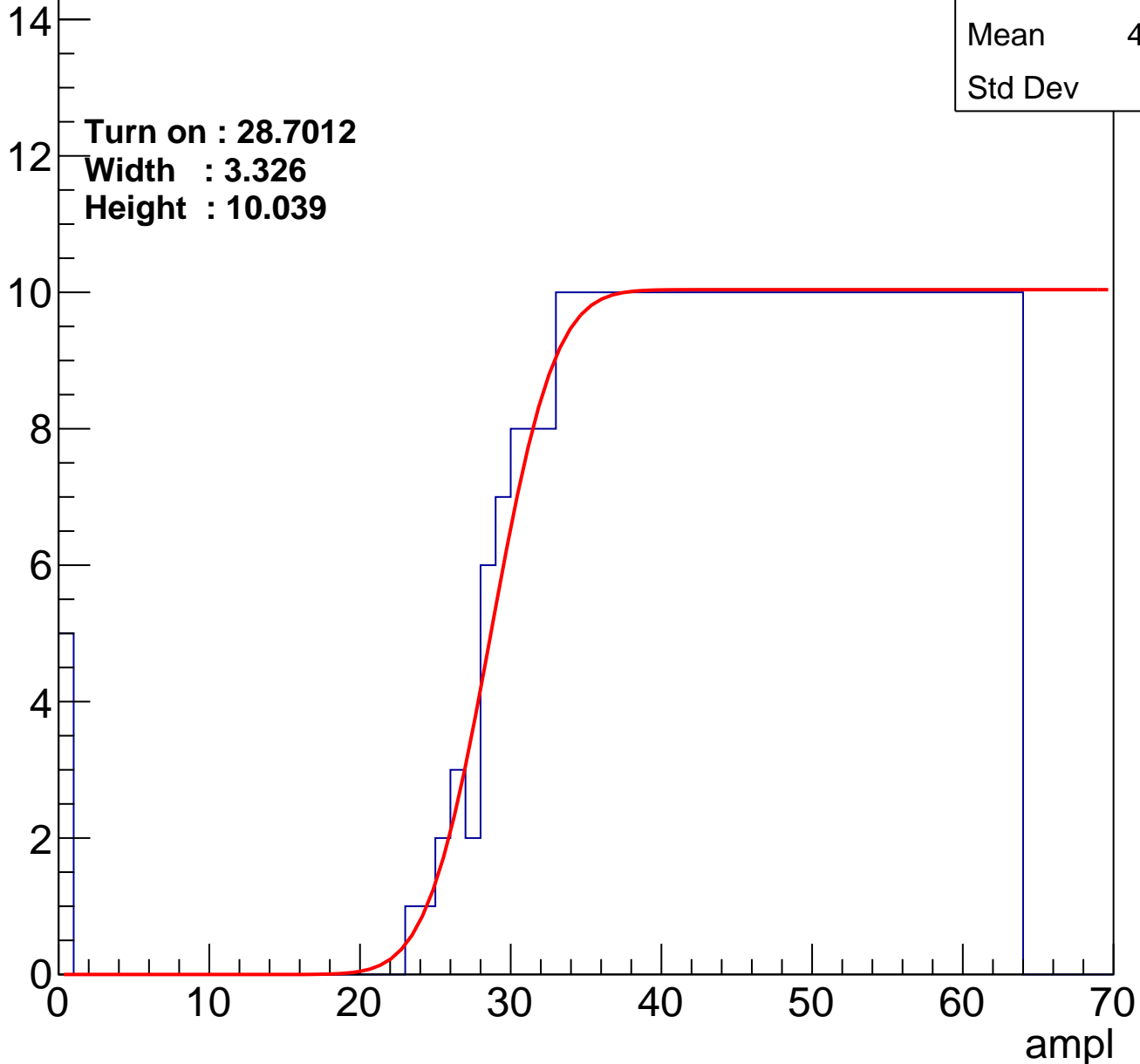
Entries	361
Mean	44.94
Std Dev	11.7

Turn on : 28.7012

Width : 3.326

Height : 10.039

Entry



B1L101S, U24-ch113

calib_packv5_042523_0143.root, FC#0, port D2

Entries	362
Mean	45.09
Std Dev	11.25

Turn on : 28.2511

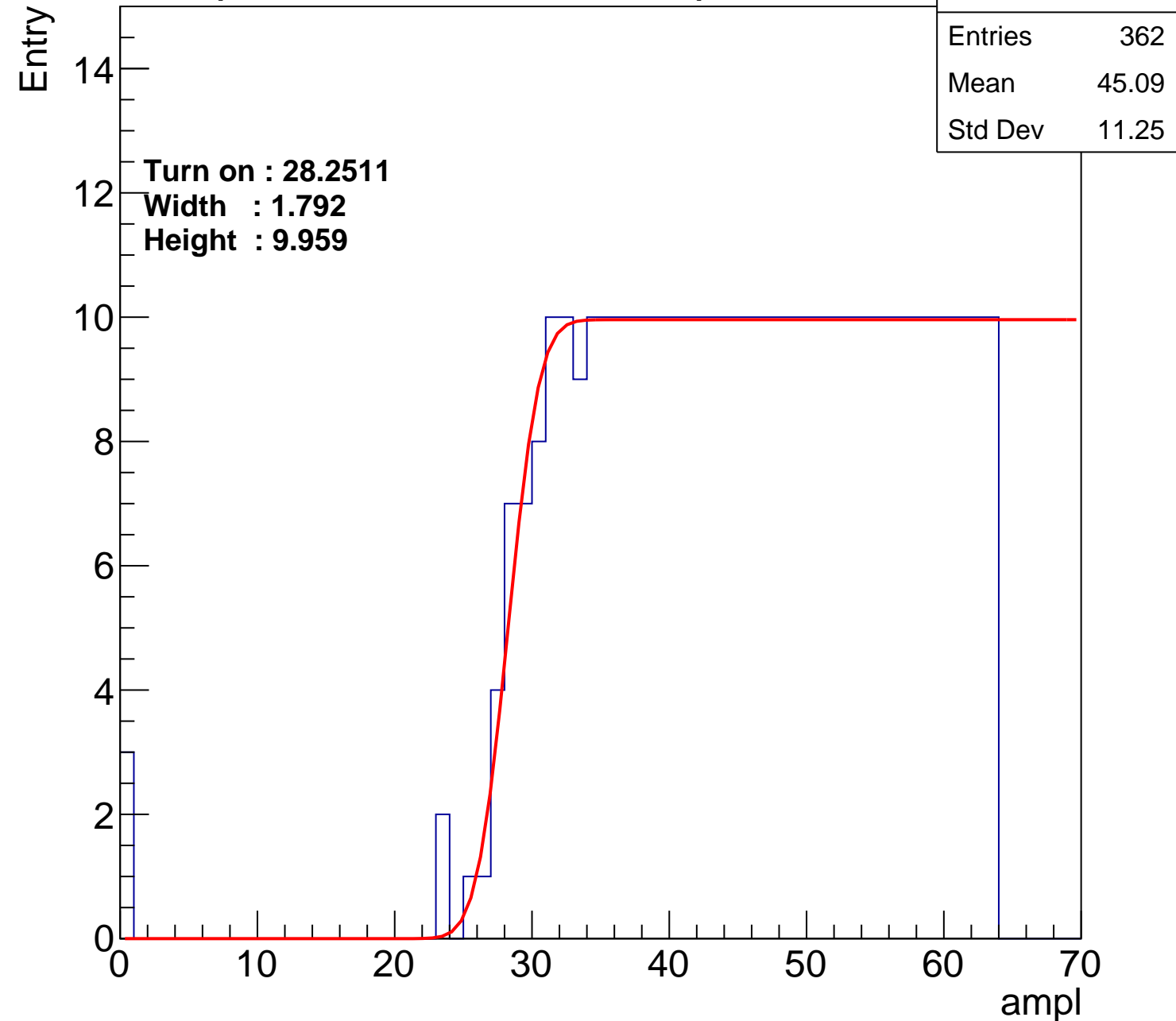
Width : 1.792

Height : 9.959

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch114

calib_packv5_042523_0143.root, FC#0, port D2

Entries	390
Mean	43.49
Std Dev	12.47

Turn on : 25.6677

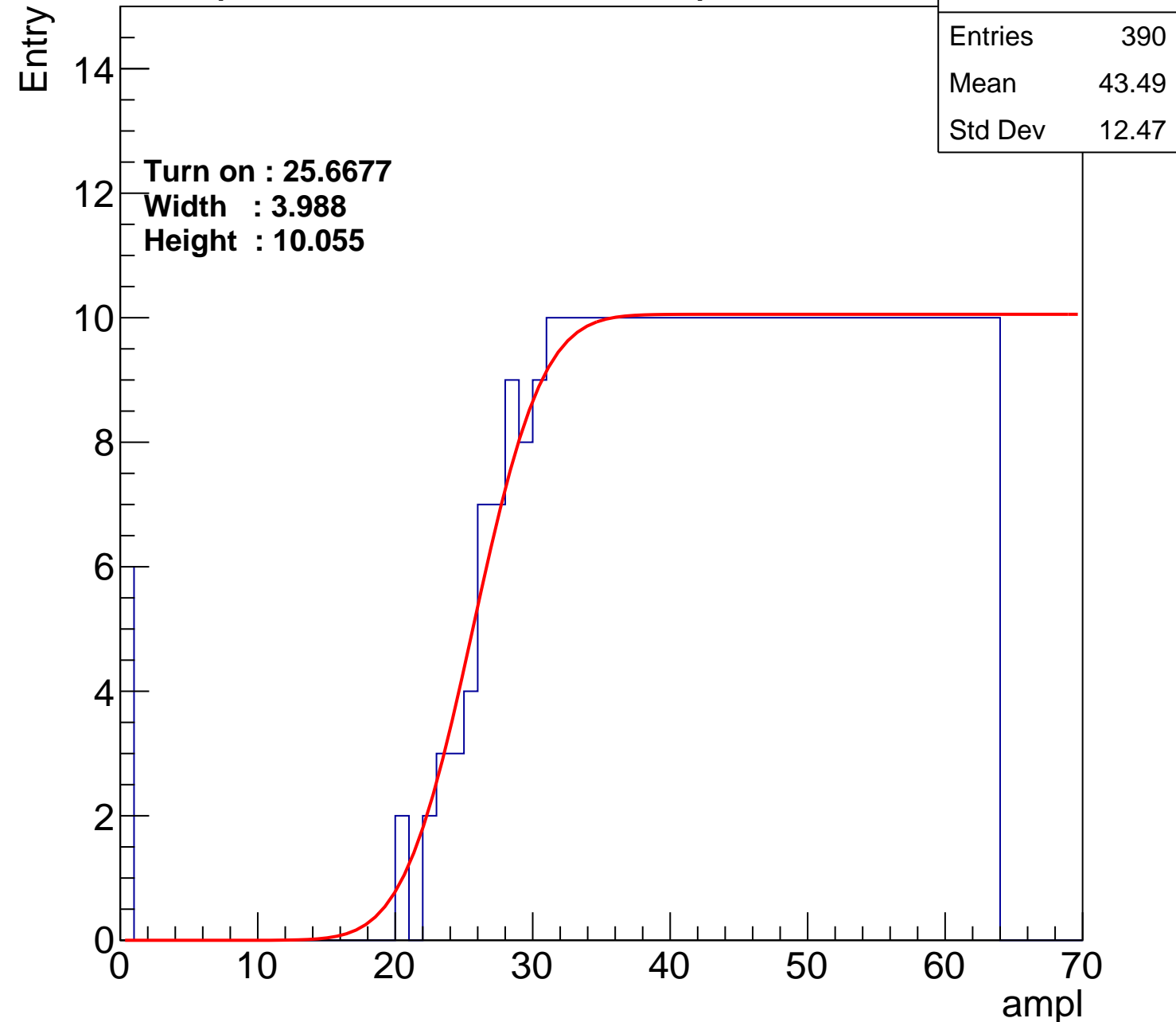
Width : 3.988

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch115

calib_packv5_042523_0143.root, FC#0, port D2

Entries	355
Mean	45.41
Std Dev	11.11

Turn on : 29.2170

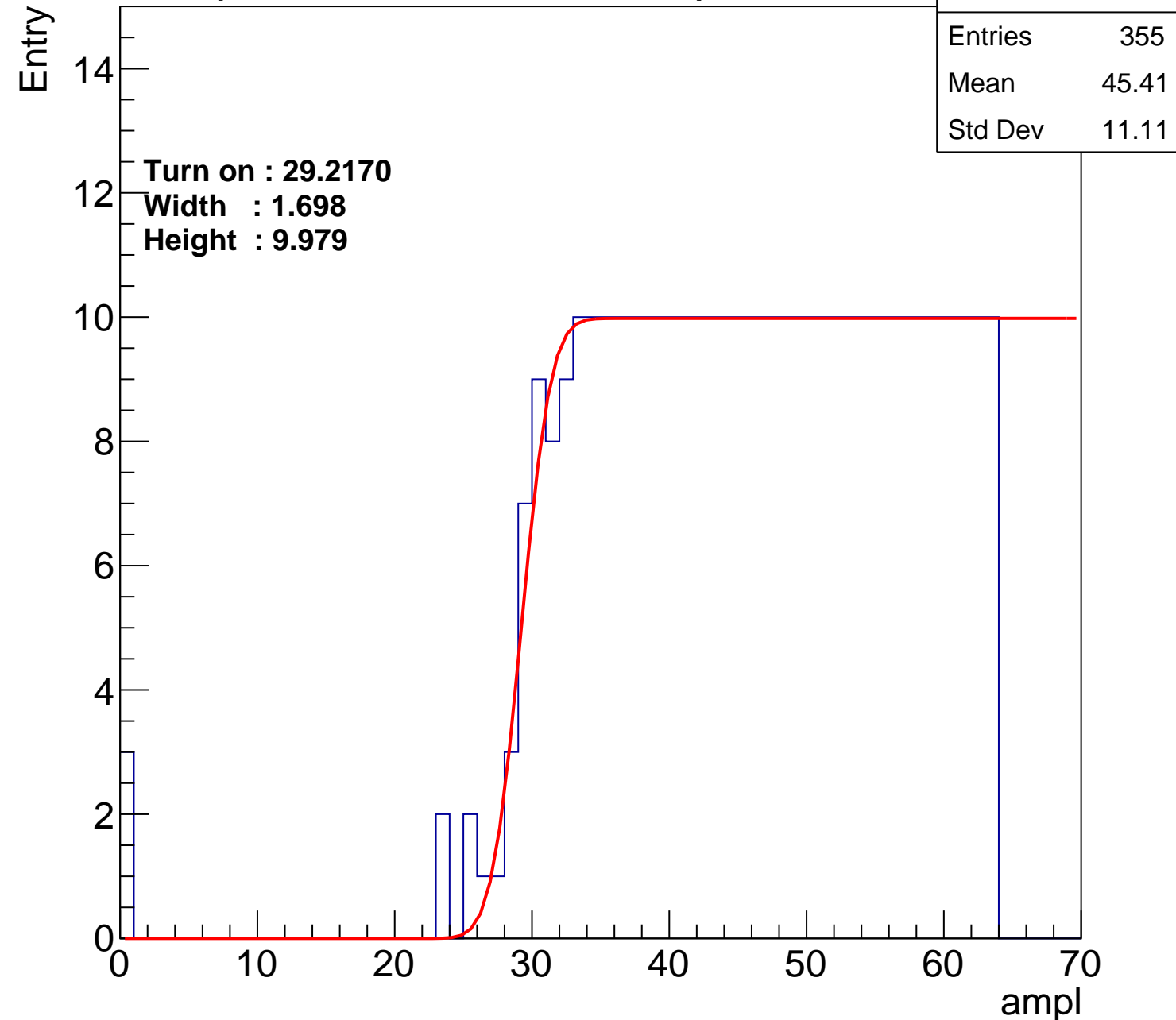
Width : 1.698

Height : 9.979

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch116

calib_packv5_042523_0143.root, FC#0, port D2

Entries	381
Mean	44.2
Std Dev	11.57

Turn on : 26.7991

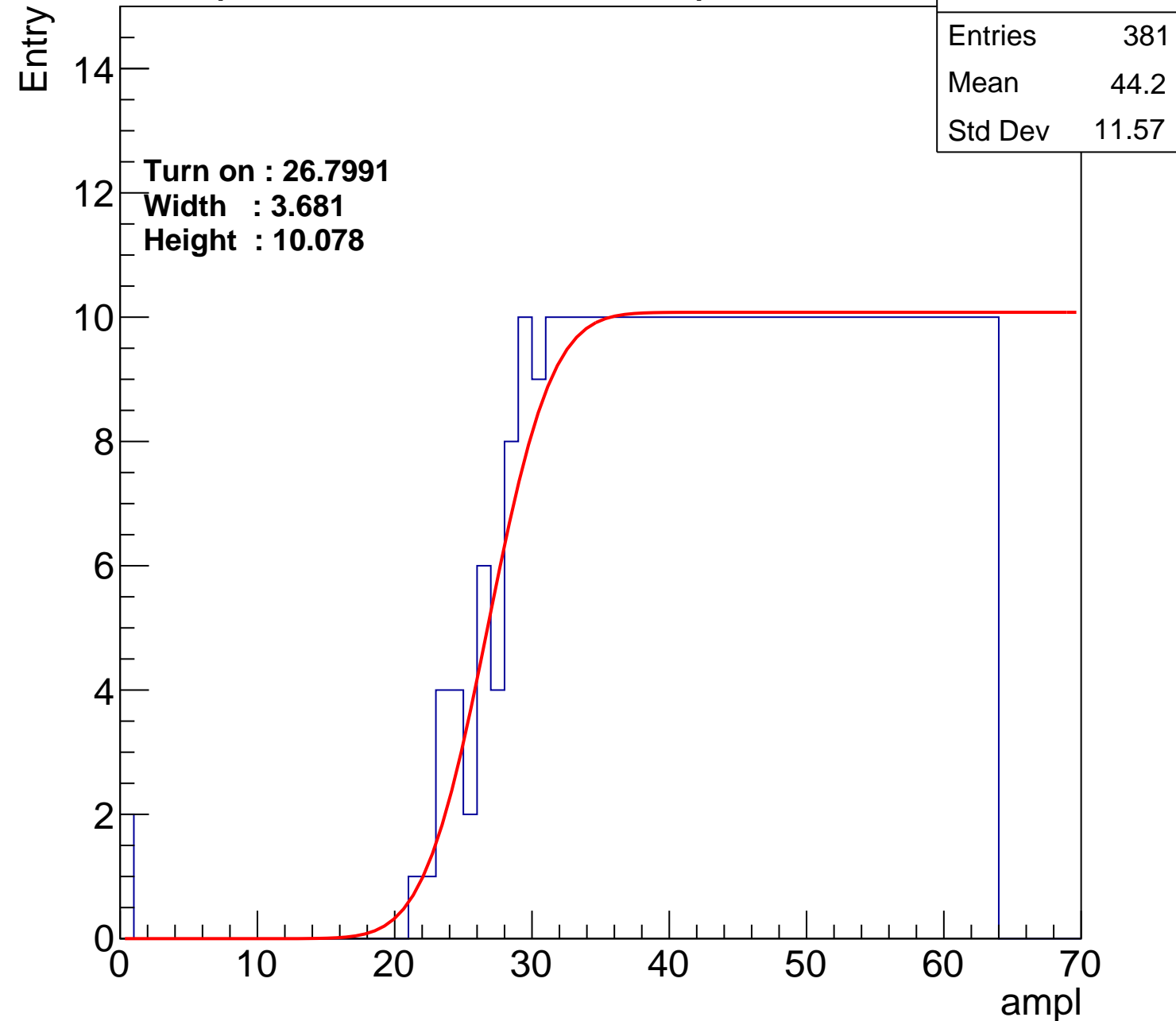
Width : 3.681

Height : 10.078

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch117

calib_packv5_042523_0143.root, FC#0, port D2

Entries	361
Mean	45.1
Std Dev	11.29

Turn on : 29.1945

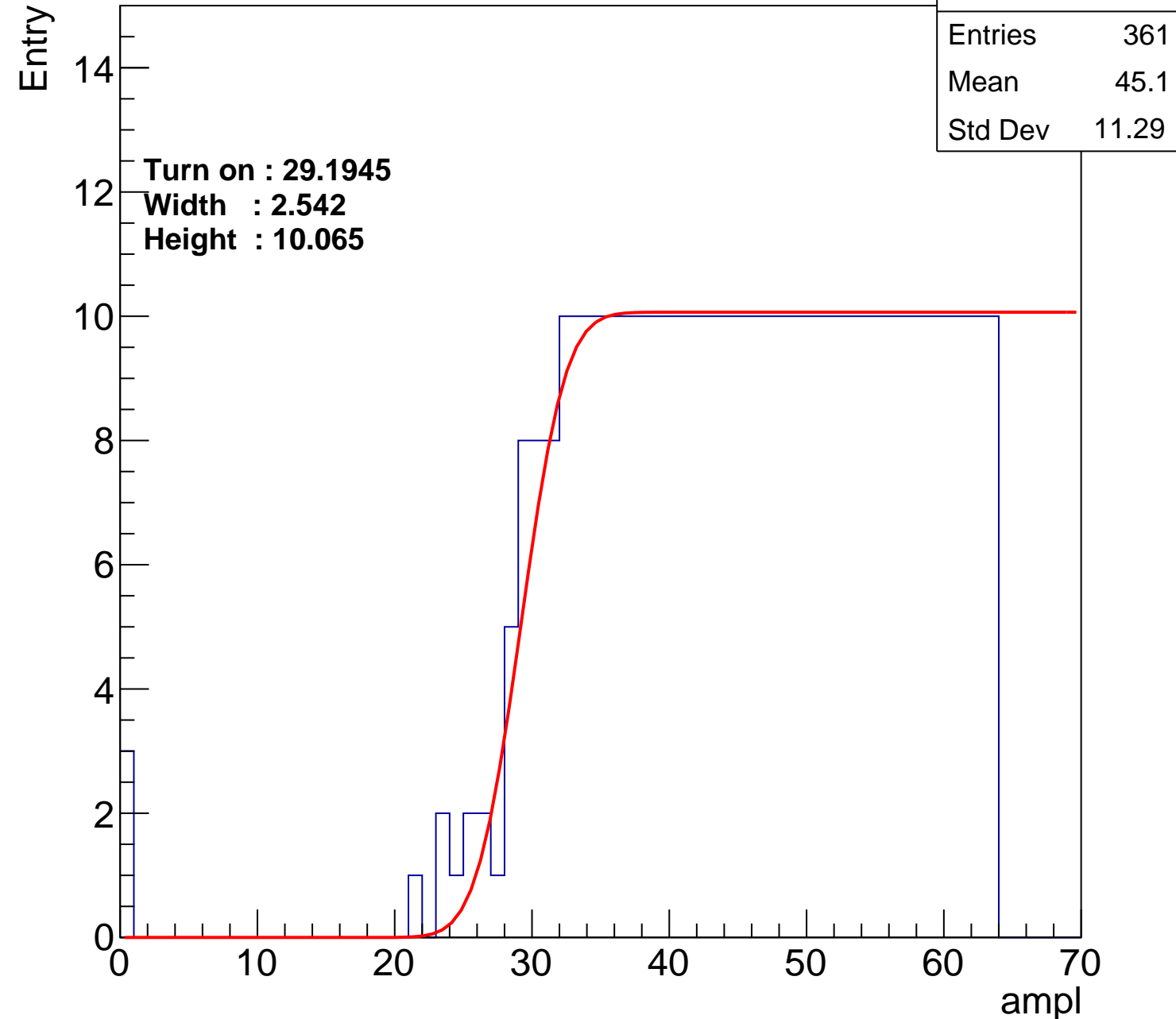
Width : 2.542

Height : 10.065

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch118

calib_packv5_042523_0143.root, FC#0, port D2

Entries	382
Mean	43.95
Std Dev	12.11

Turn on : 26.0558

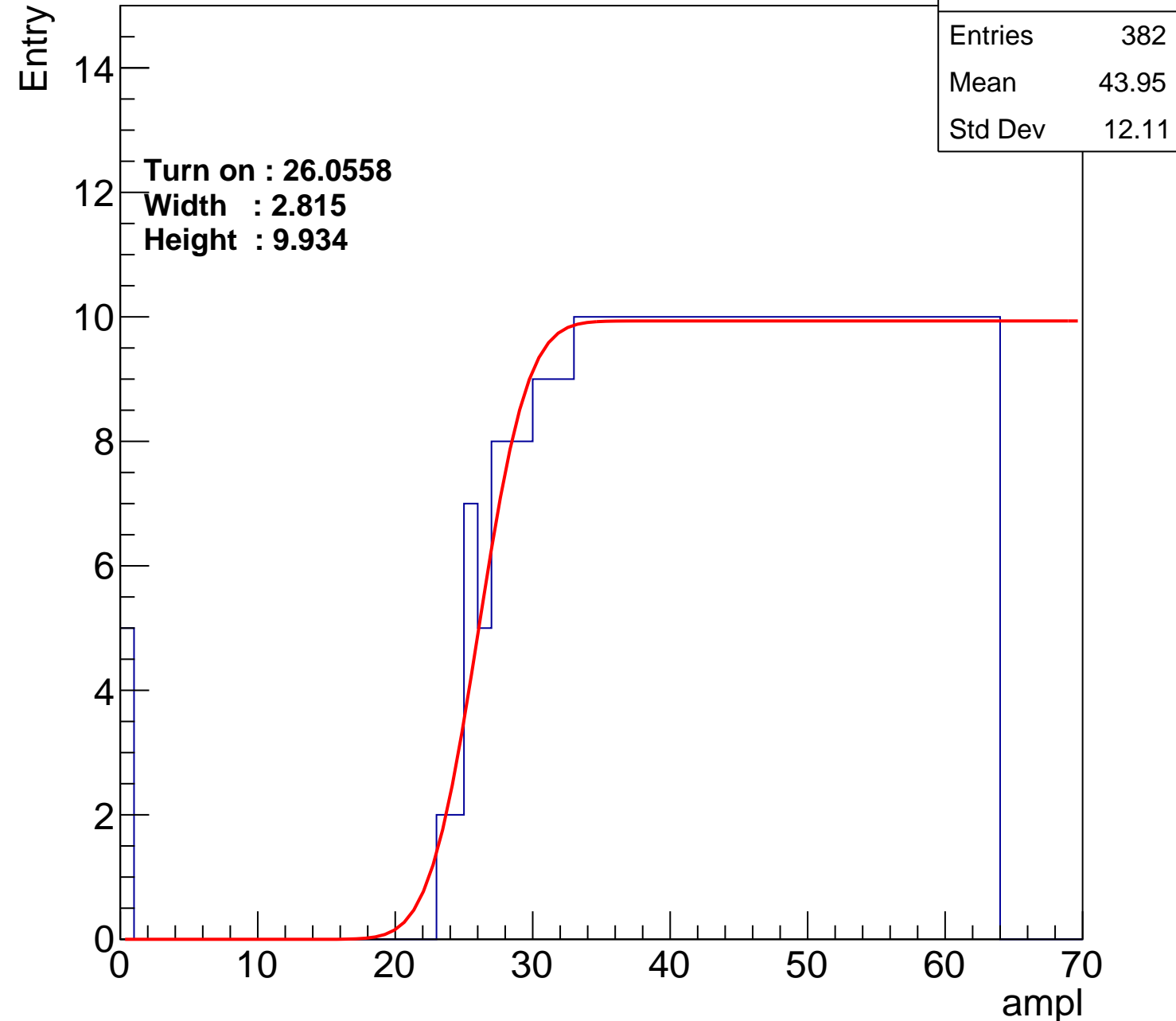
Width : 2.815

Height : 9.934

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch119

calib_packv5_042523_0143.root, FC#0, port D2

Entries	360
Mean	45.16
Std Dev	11.24

Turn on : 29.2485

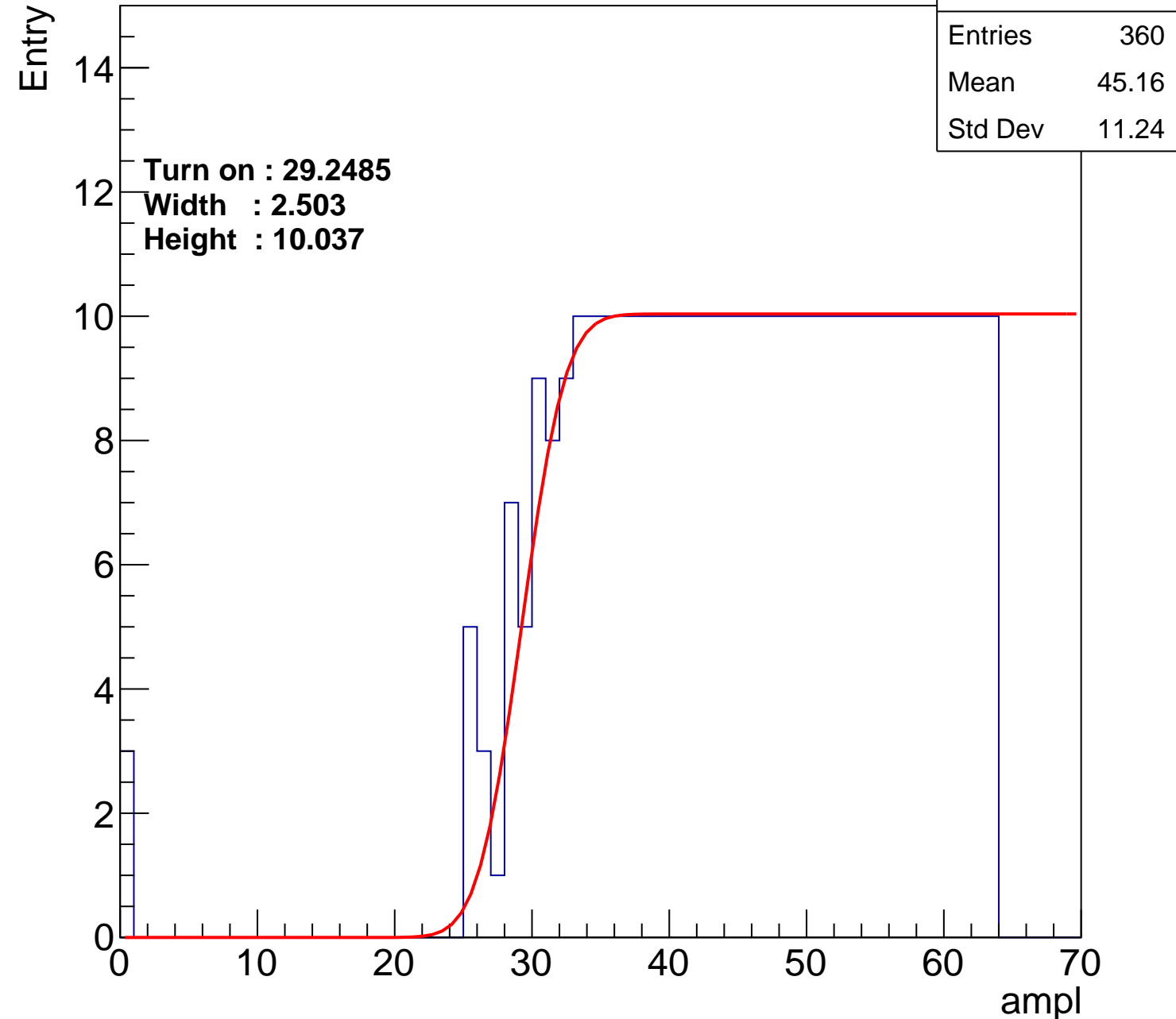
Width : 2.503

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch120

calib_packv5_042523_0143.root, FC#0, port D2

Entries	356
Mean	45.17
Std Dev	11.62

Turn on : 29.6503

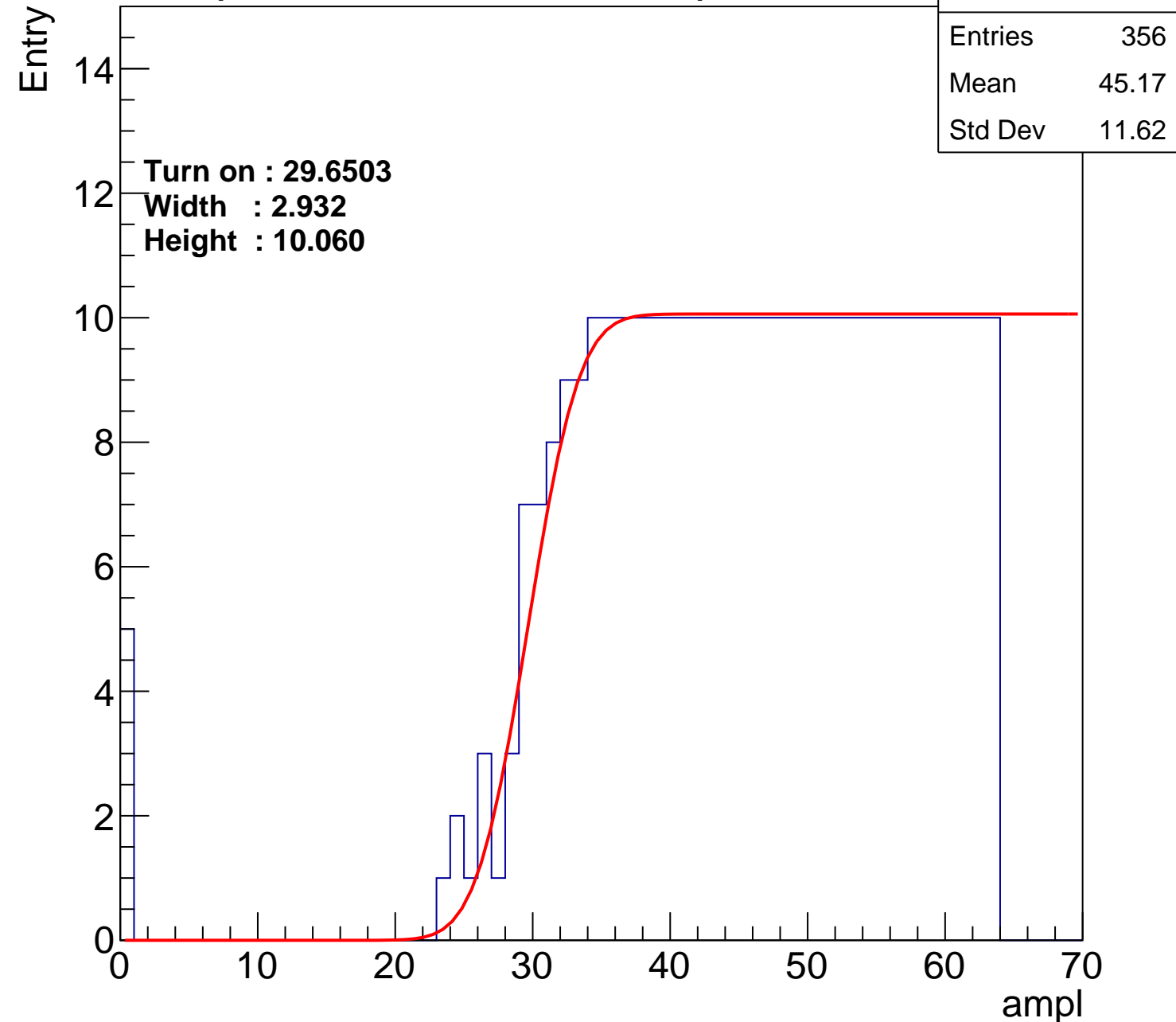
Width : 2.932

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch121

calib_packv5_042523_0143.root, FC#0, port D2

Entries	352
Mean	45.56
Std Dev	11.04

Turn on : 29.5137

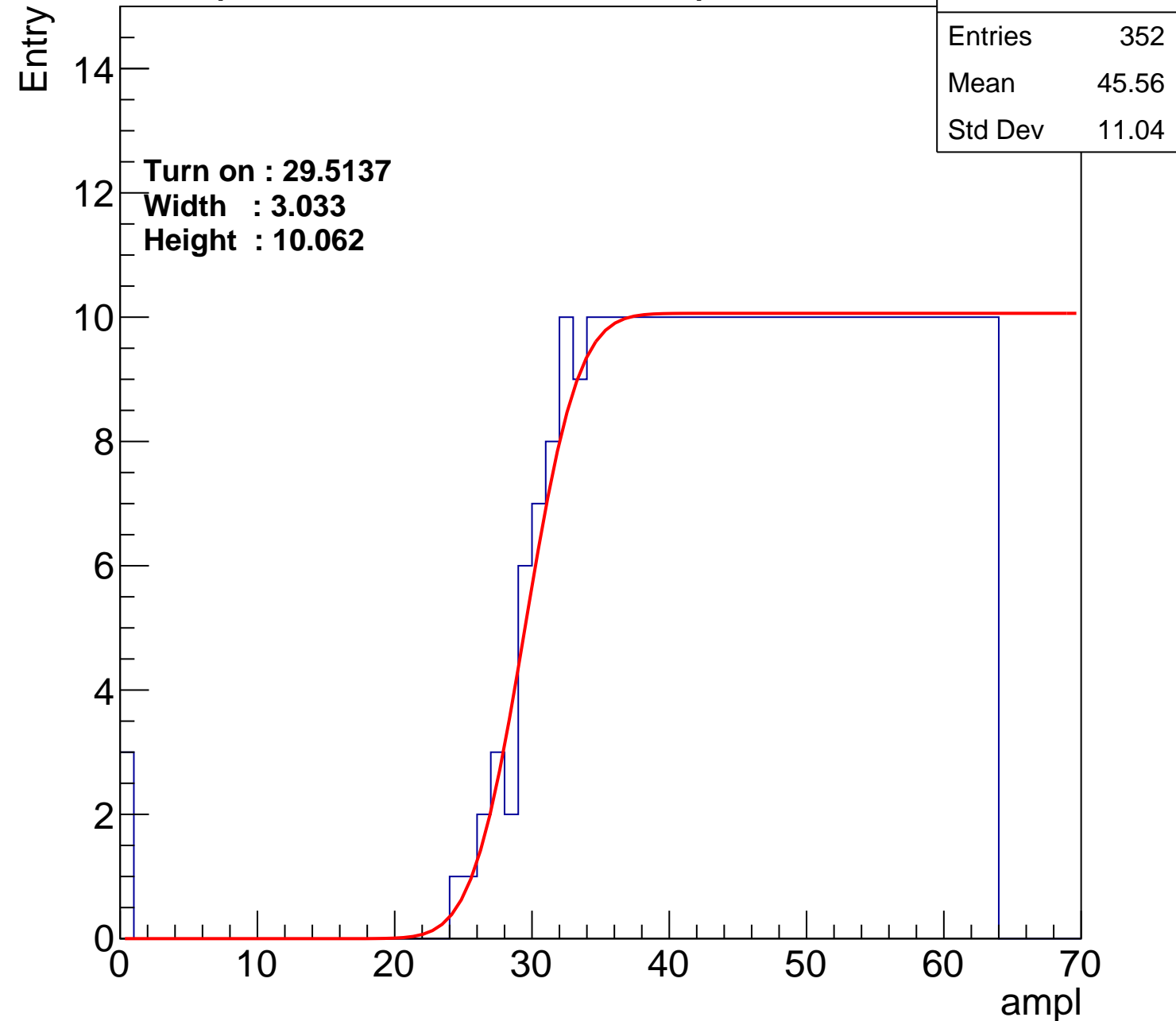
Width : 3.033

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch122

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.45
Std Dev	11.57

Turn on : 27.3210

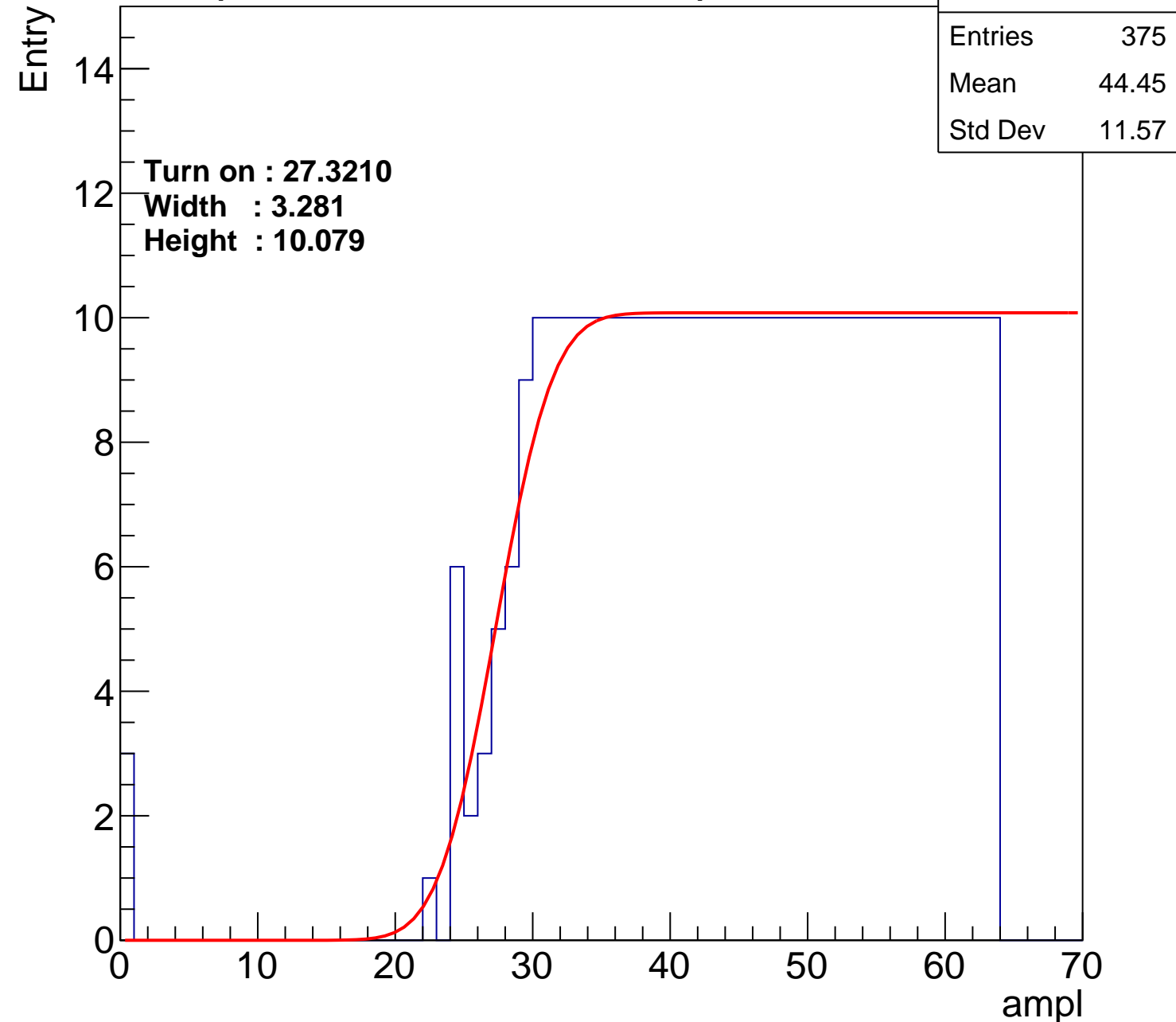
Width : 3.281

Height : 10.079

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch123

calib_packv5_042523_0143.root, FC#0, port D2

Entries	359
Mean	45.15
Std Dev	11.41

Turn on : 28.6211

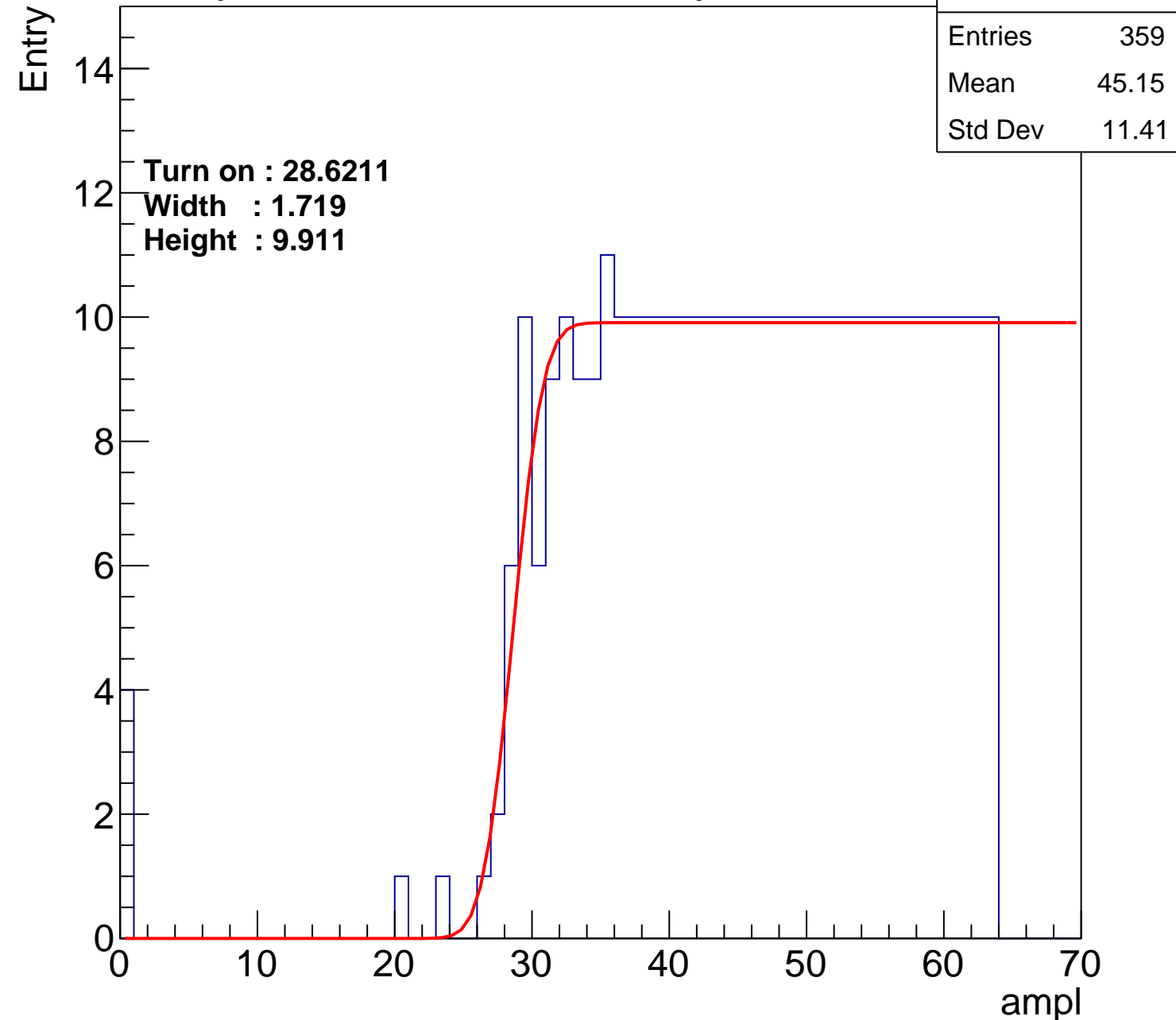
Width : 1.719

Height : 9.911

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch124

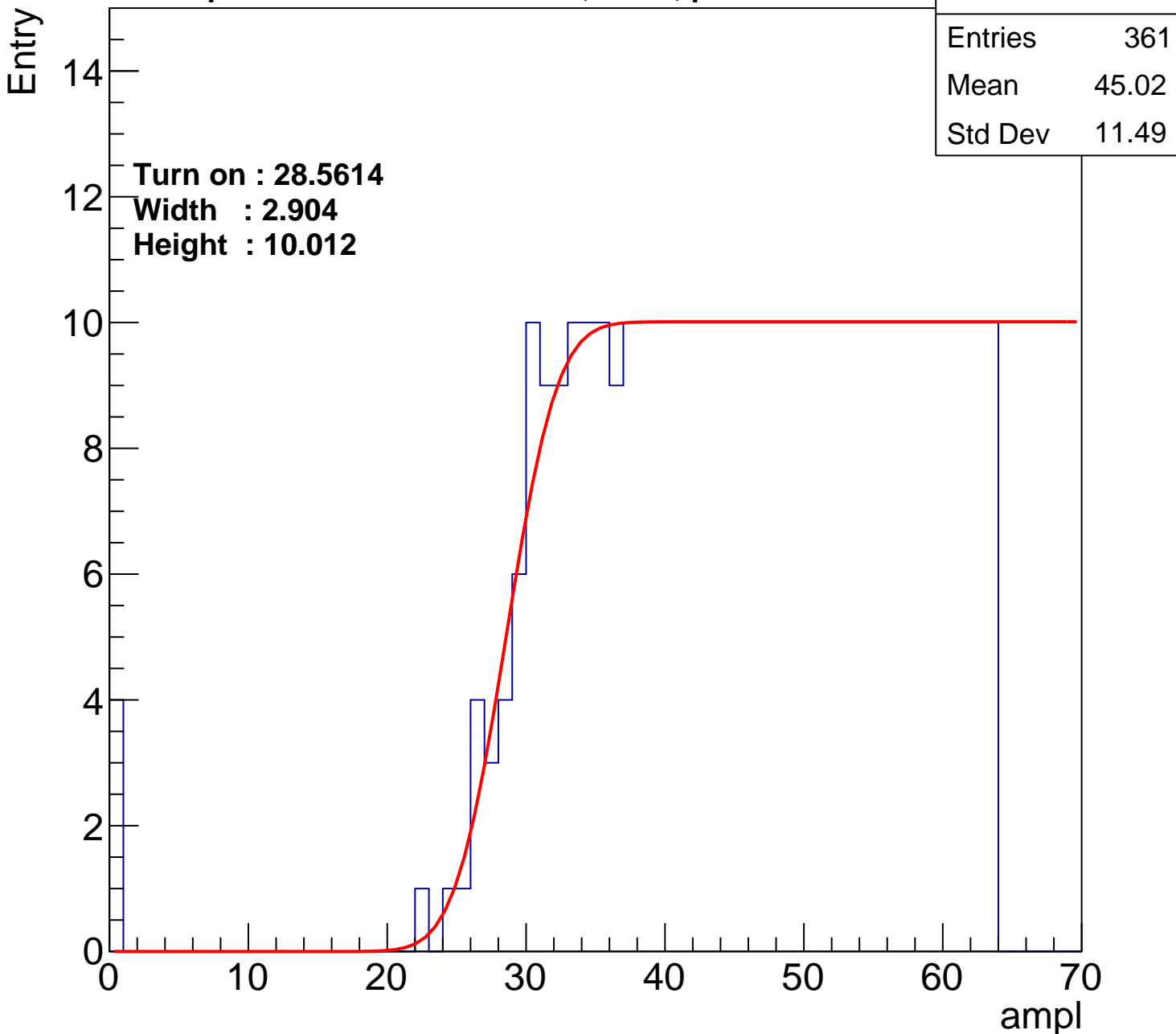
calib_packv5_042523_0143.root, FC#0, port D2

Turn on : 28.5614

Width : 2.904

Height : 10.012

Entries	361
Mean	45.02
Std Dev	11.49



B1L101S, U24-ch125

calib_packv5_042523_0143.root, FC#0, port D2

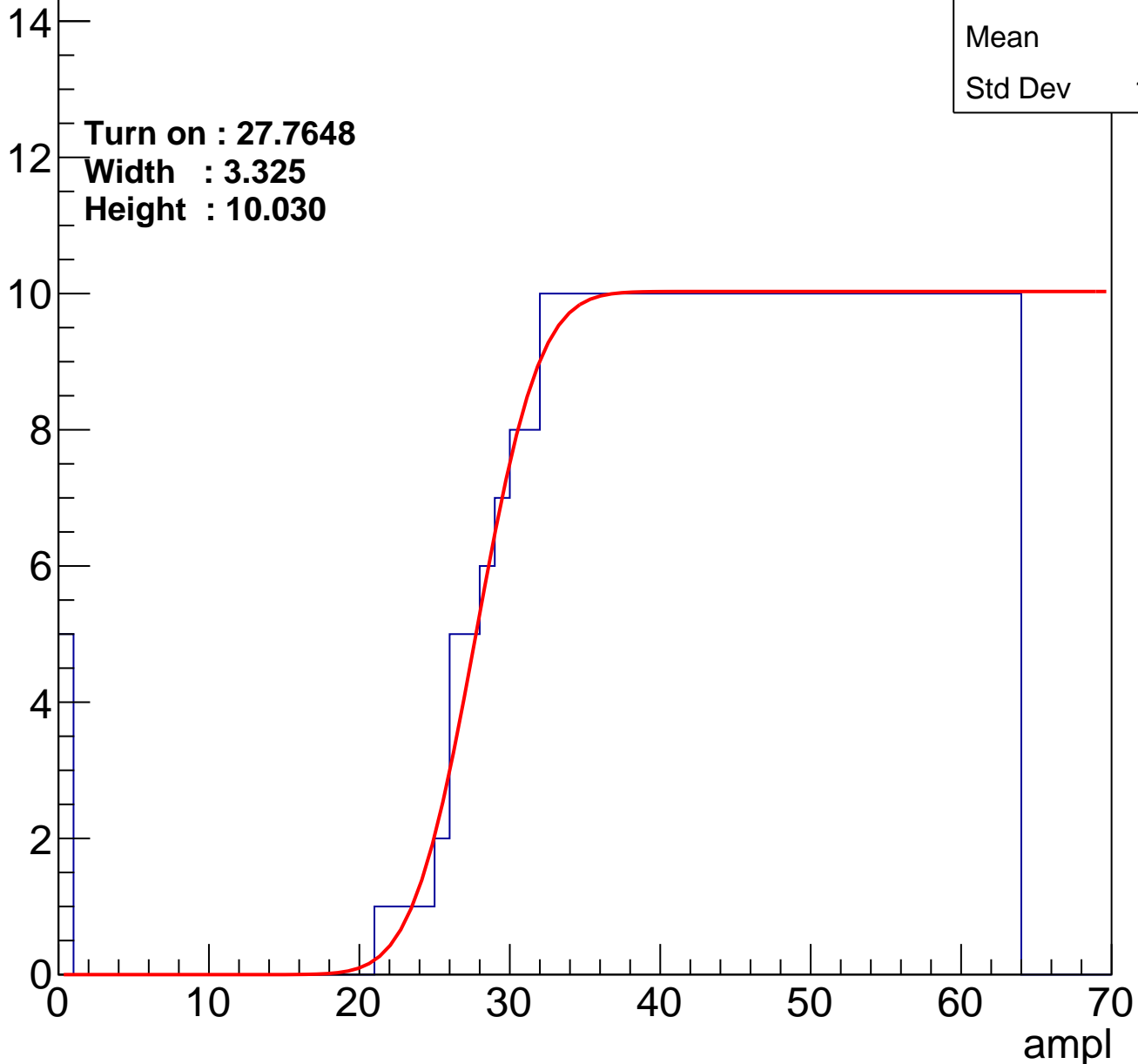
Entries	370
Mean	44.5
Std Dev	11.91

Turn on : 27.7648

Width : 3.325

Height : 10.030

Entry



B1L101S, U24-ch126

calib_packv5_042523_0143.root, FC#0, port D2

Entries	381
Mean	43.96
Std Dev	12.15

Turn on : 26.7642

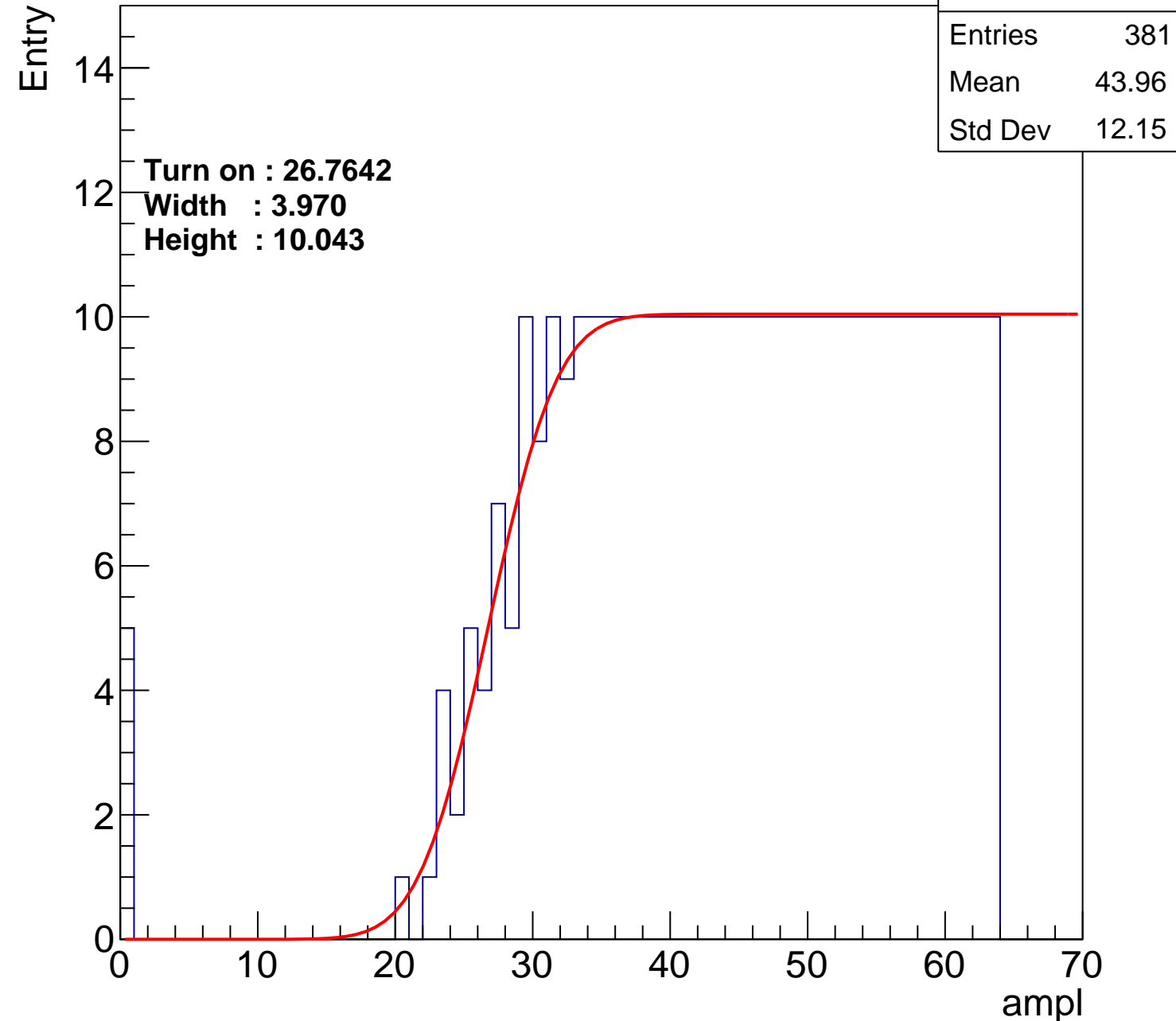
Width : 3.970

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch127

calib_packv5_042523_0143.root, FC#0, port D2

Entries	367
Mean	44.82
Std Dev	11.4

Turn on : 27.6896

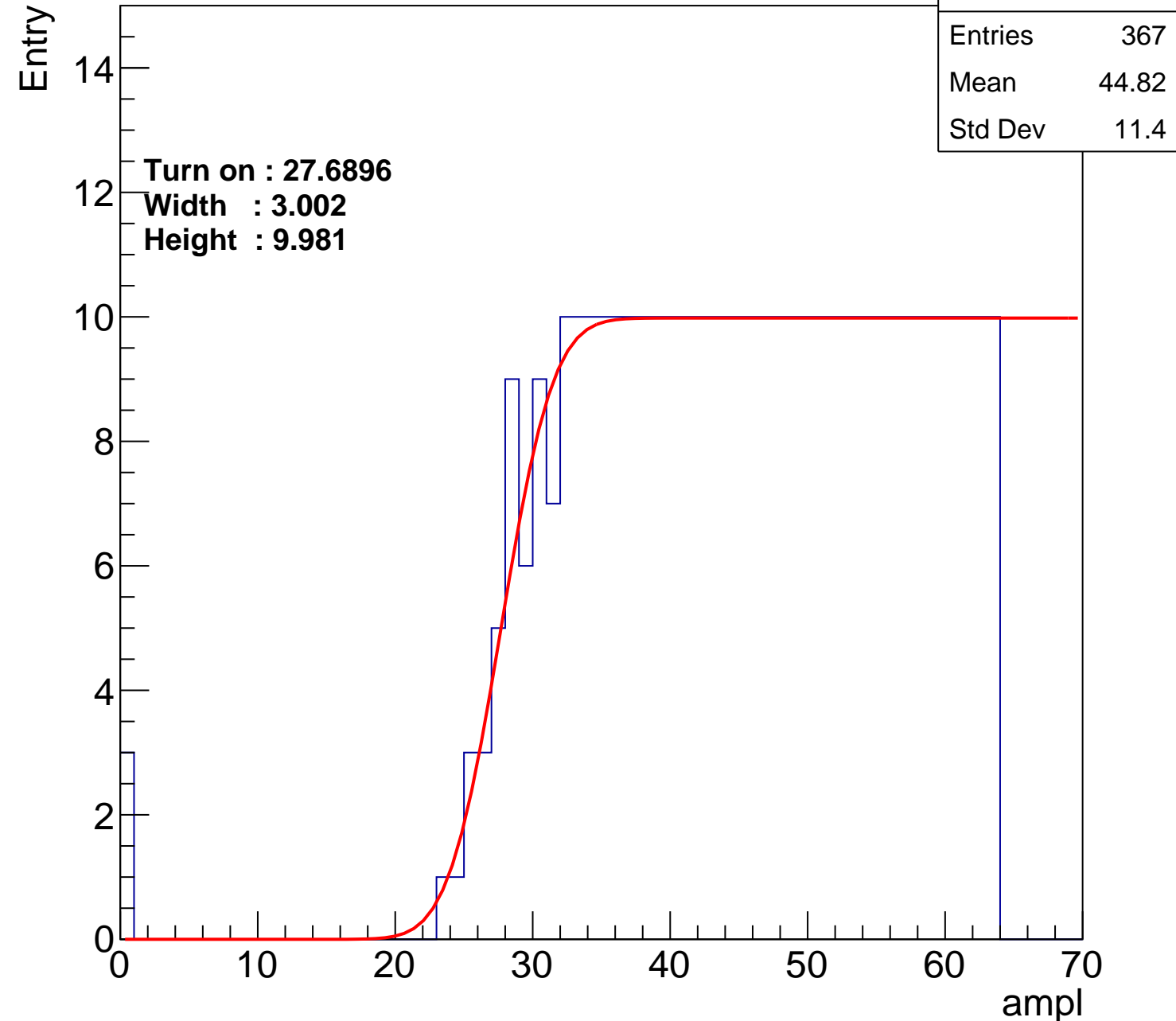
Width : 3.002

Height : 9.981

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U24-ch127

calib_packv5_042523_0143.root, FC#0, port D2

Entries	367
Mean	44.82
Std Dev	11.4

Turn on : 27.6896

Width : 3.002

Height : 9.981

Entry

14
12
10
8
6
4
2
0

ampl

