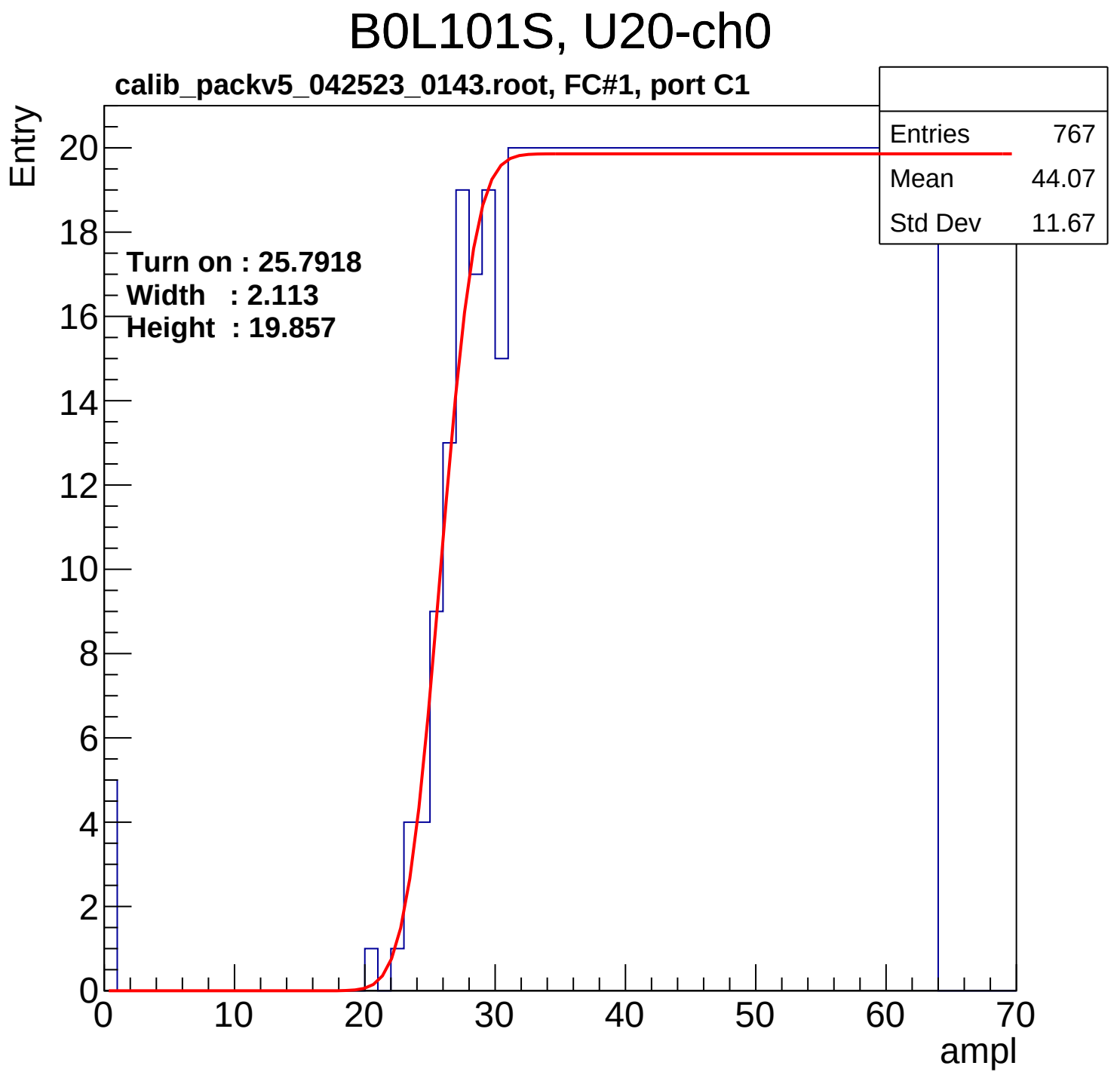
B0L101S, U20-ch0
calib_packv5_042523_0143.root, FC#1, port C1
Entries 767
Mean 44.07
Std Dev 11.67
Turn on : 25.7918
Width : 2.113
Height : 19.857
Entry
ampl
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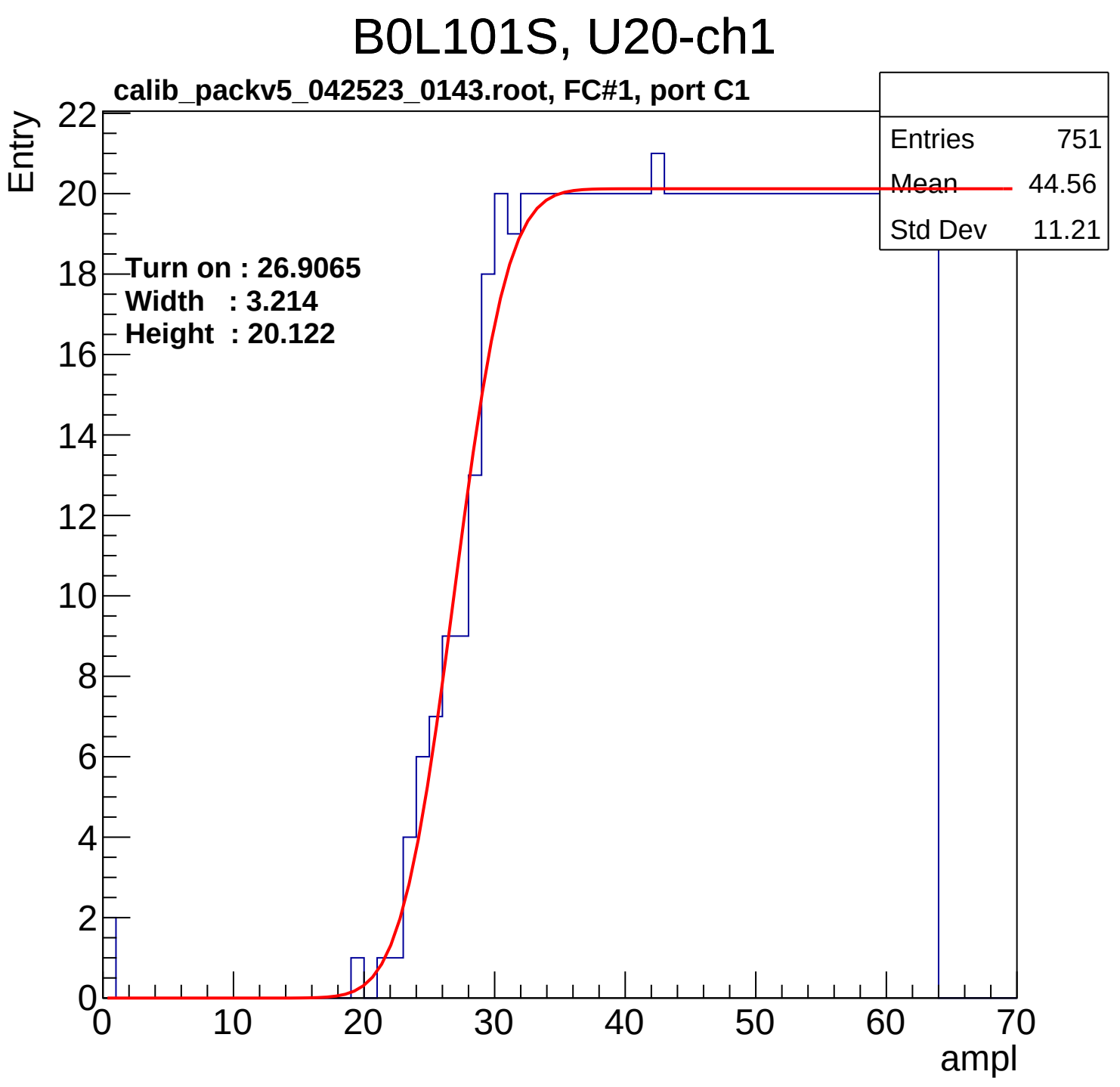
B0L101S, U20-ch1
calib_packv5_042523_0143.root, FC#1, port C1
Entries 751
Mean 44.56
Std Dev 11.21
Turn on : 26.9065
Width : 3.214
Height : 20.122
Entry
ampl
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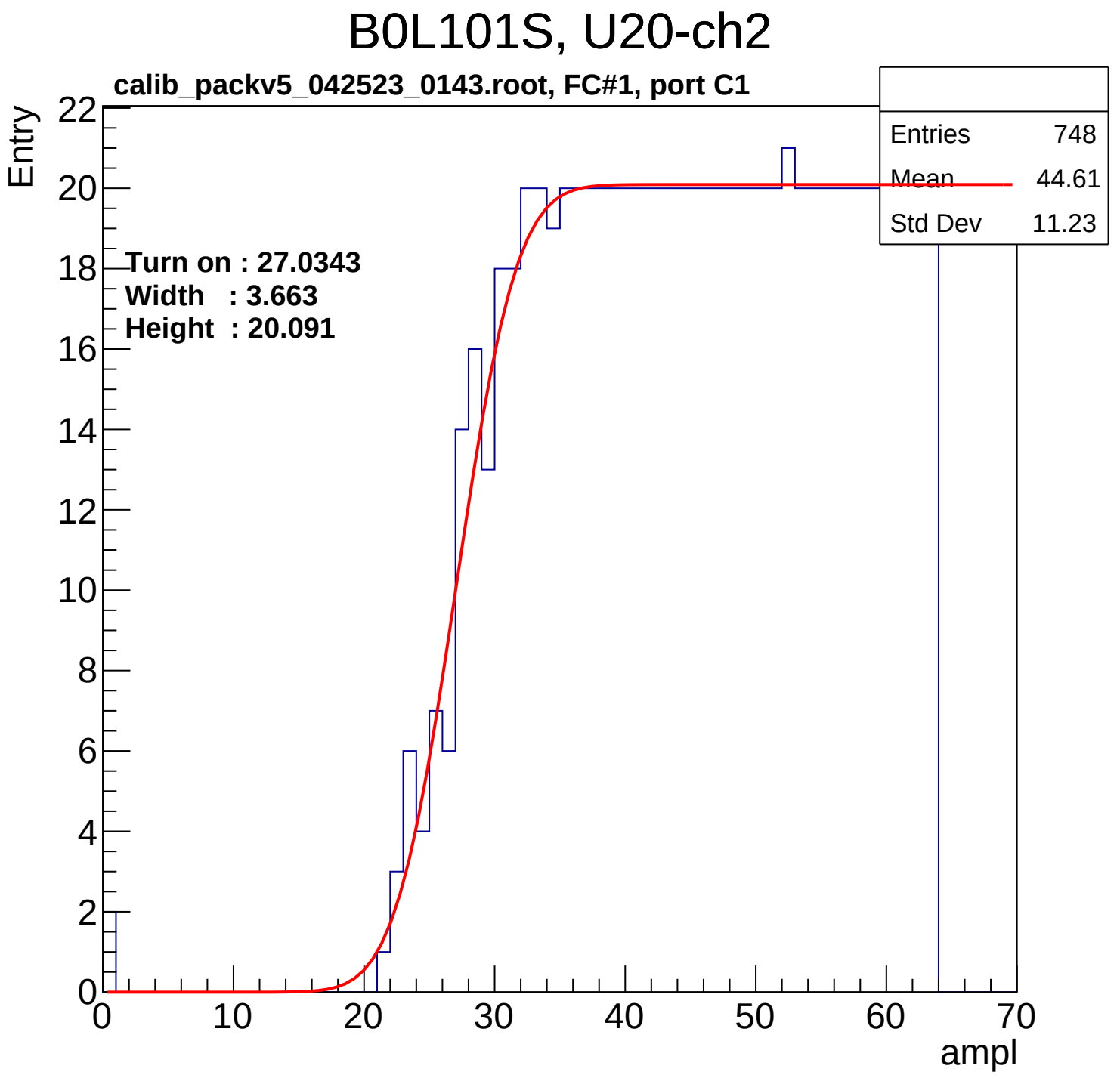
B0L101S, U20-ch2
calib_packv5_042523_0143.root, FC#1, port C1
Entries 748
Mean 44.61
Std Dev 11.23
Turn on : 27.0343
Width : 3.663
Height : 20.091
Entry
ampl
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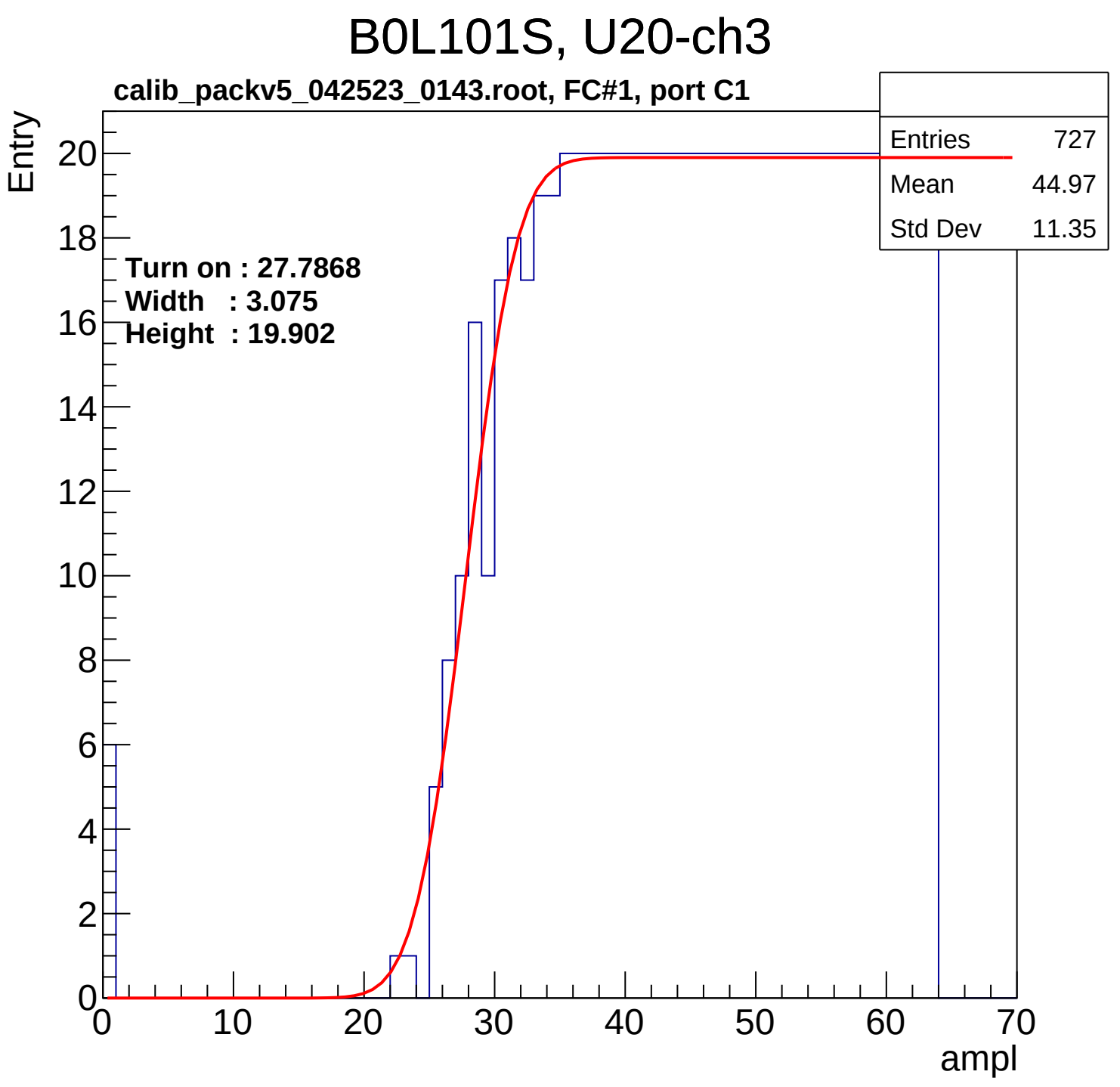
B0L101S, U20-ch3
calib_packv5_042523_0143.root, FC#1, port C1
Entries 727
Mean 44.97
Std Dev 11.35
Turn on : 27.7868
Width : 3.075
Height : 19.902
Entry
ampl
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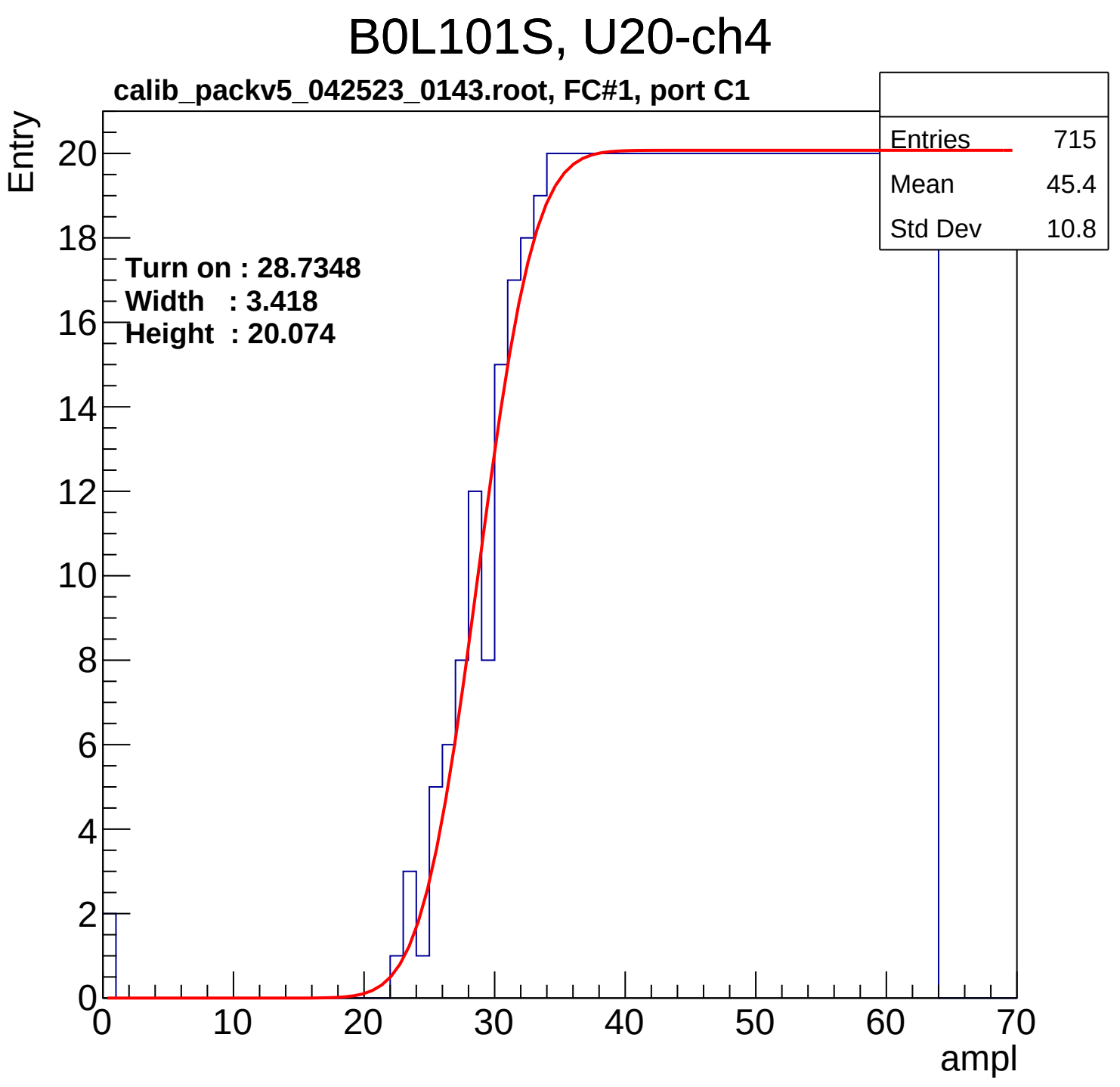
B0L101S, U20-ch4
calib_packv5_042523_0143.root, FC#1, port C1
Entries 715
Mean 45.4
Std Dev 10.8
Turn on : 28.7348
Width : 3.418
Height : 20.074
Entry
ampl
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6
8
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12
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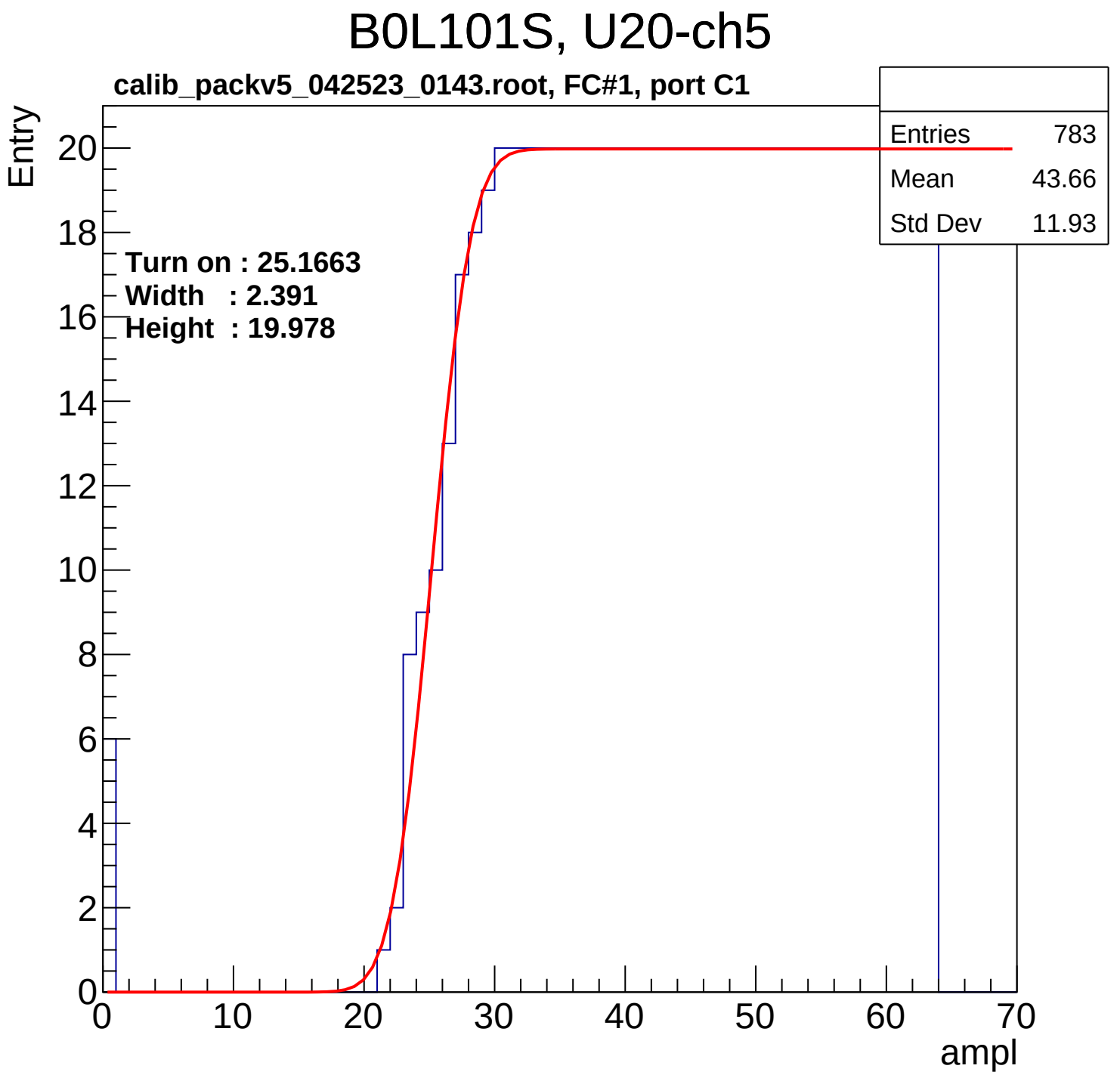
B0L101S, U20-ch5
calib_packv5_042523_0143.root, FC#1, port C1
Entries 783
Mean 43.66
Std Dev 11.93
Turn on : 25.1663
Width : 2.391
Height : 19.978
Entry
ampl
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6
8
10
12
14
16
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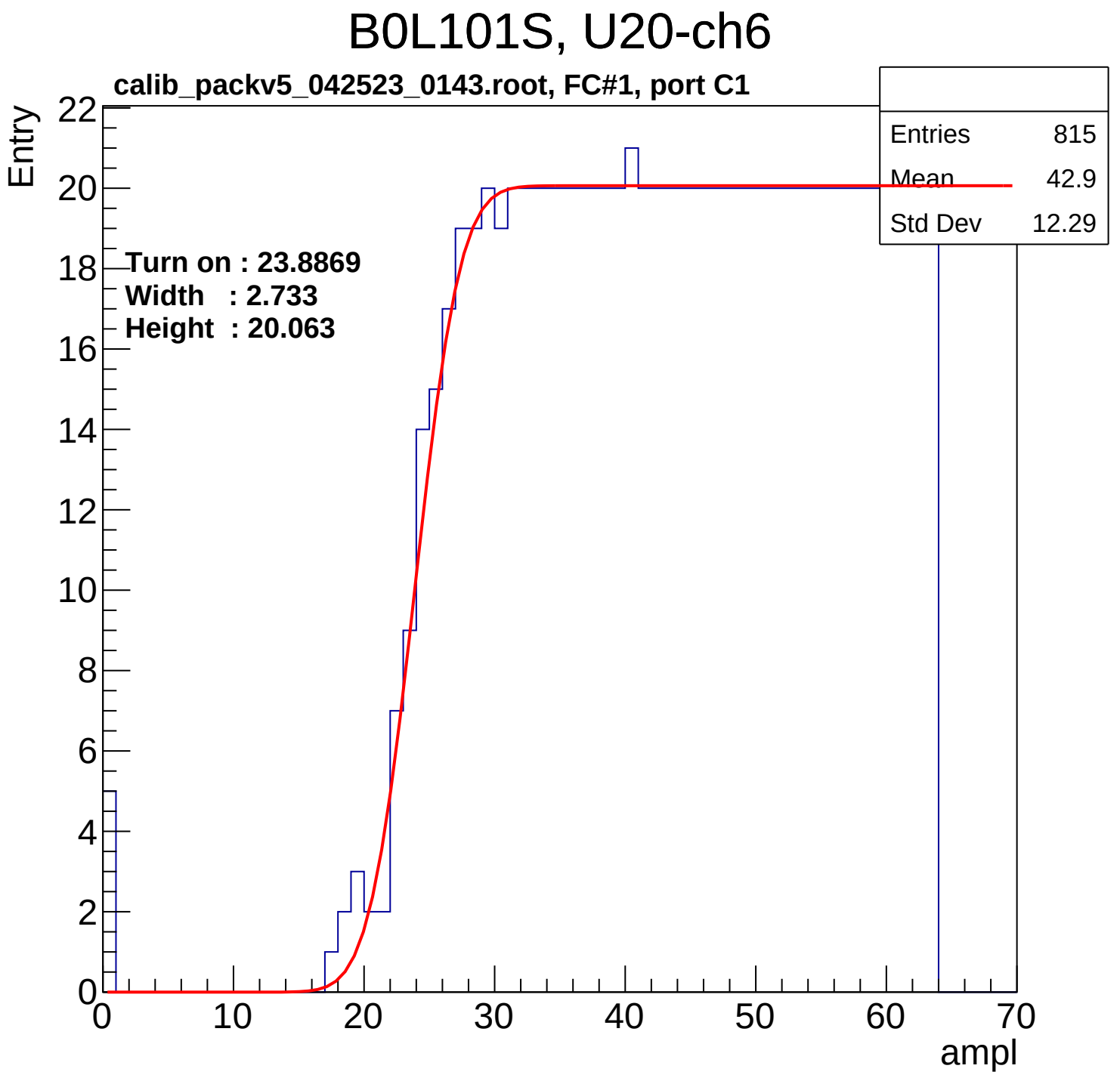
B0L101S, U20-ch6
calib_packv5_042523_0143.root, FC#1, port C1
Entries 815
Mean 42.9
Std Dev 12.29
Turn on : 23.8869
Width : 2.733
Height : 20.063
Entry
ampl
0
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8
10
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16
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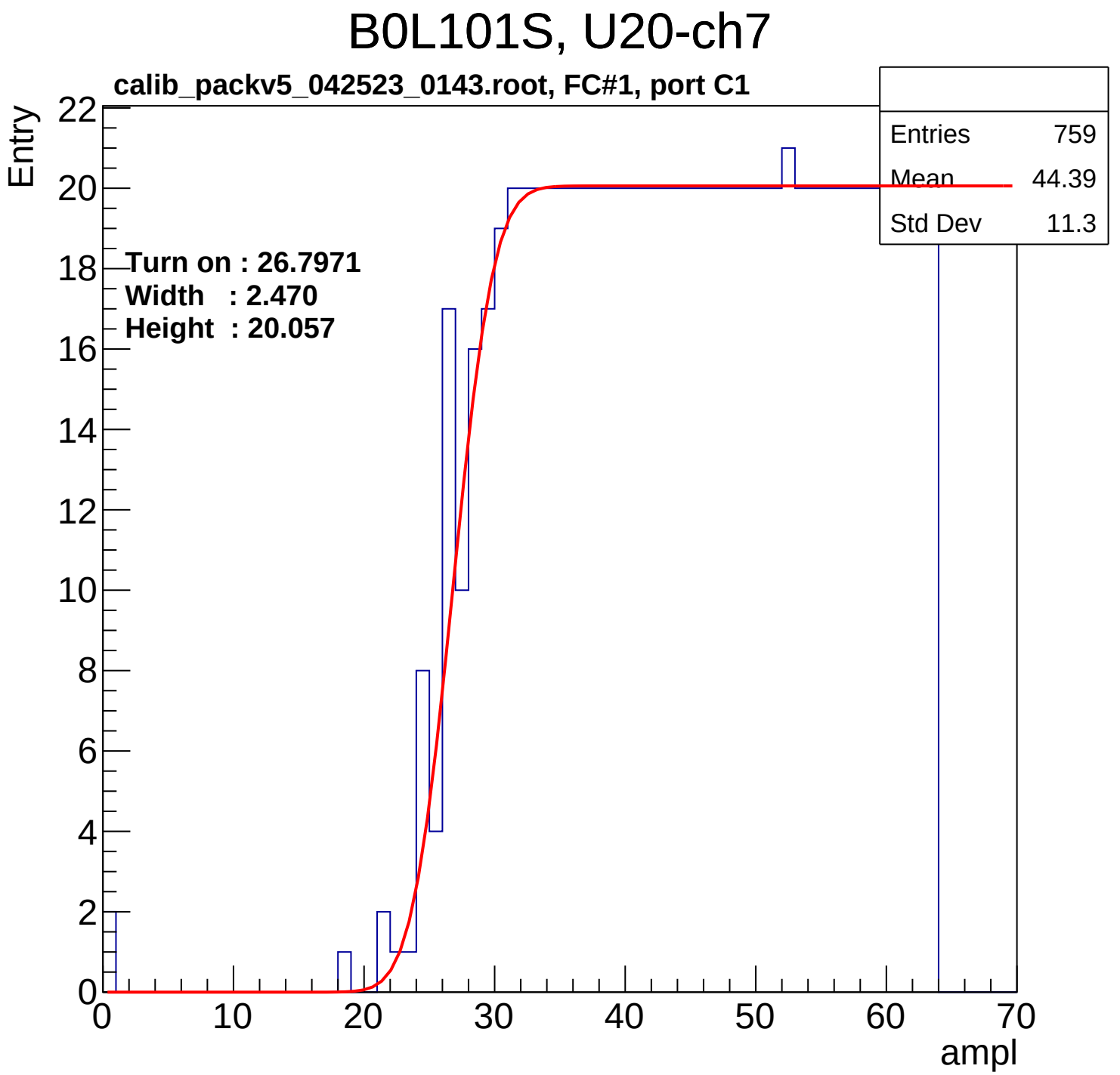
B0L101S, U20-ch7
calib_packv5_042523_0143.root, FC#1, port C1
Entries 759
Mean 44.39
Std Dev 11.3
Turn on : 26.7971
Width : 2.470
Height : 20.057
Entry
ampl
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6
8
10
12
14
16
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0
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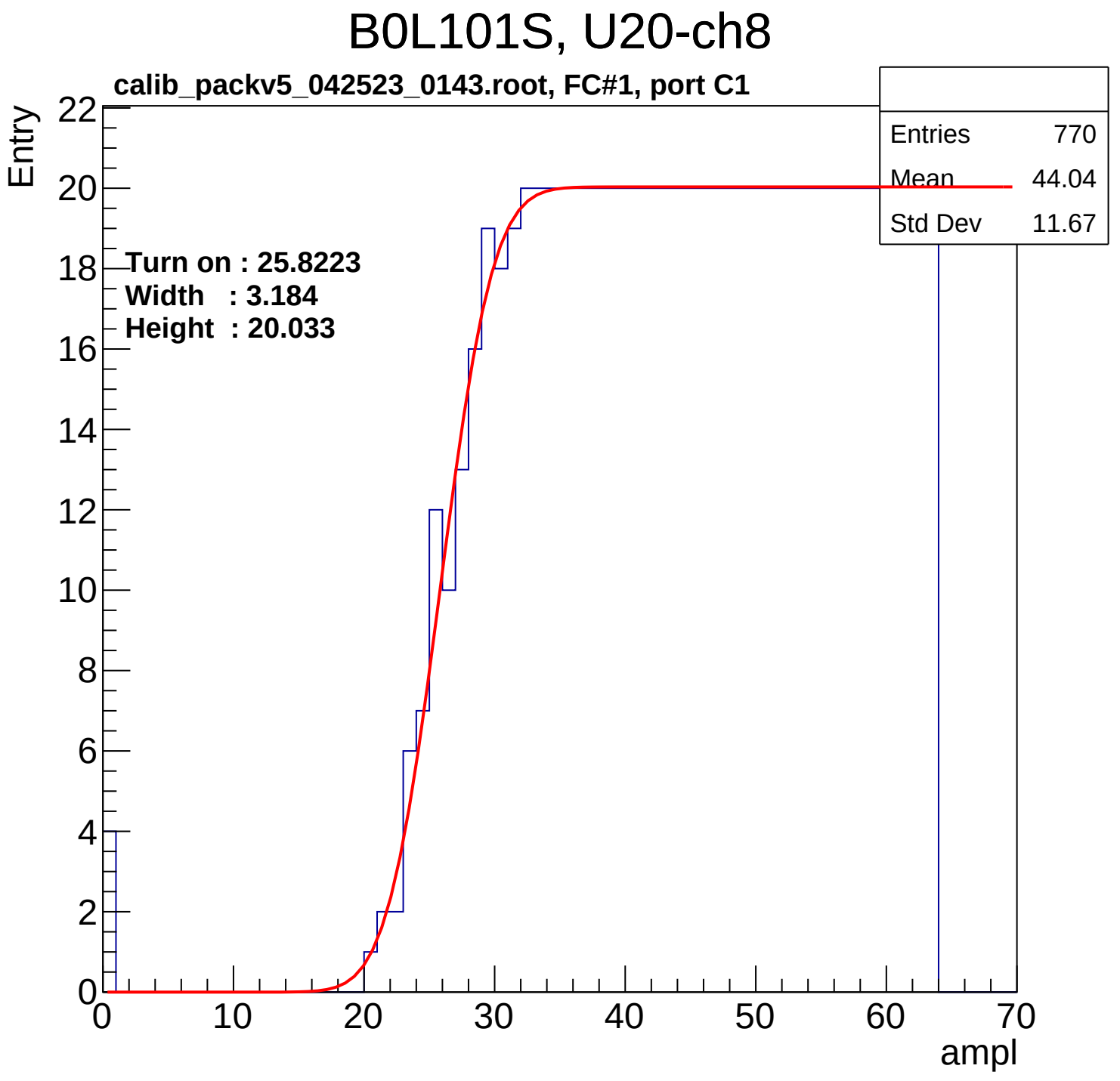
B0L101S, U20-ch8
calib_packv5_042523_0143.root, FC#1, port C1
Entries 770
Mean 44.04
Std Dev 11.67
Turn on : 25.8223
Width : 3.184
Height : 20.033
Entry
ampl
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10
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16
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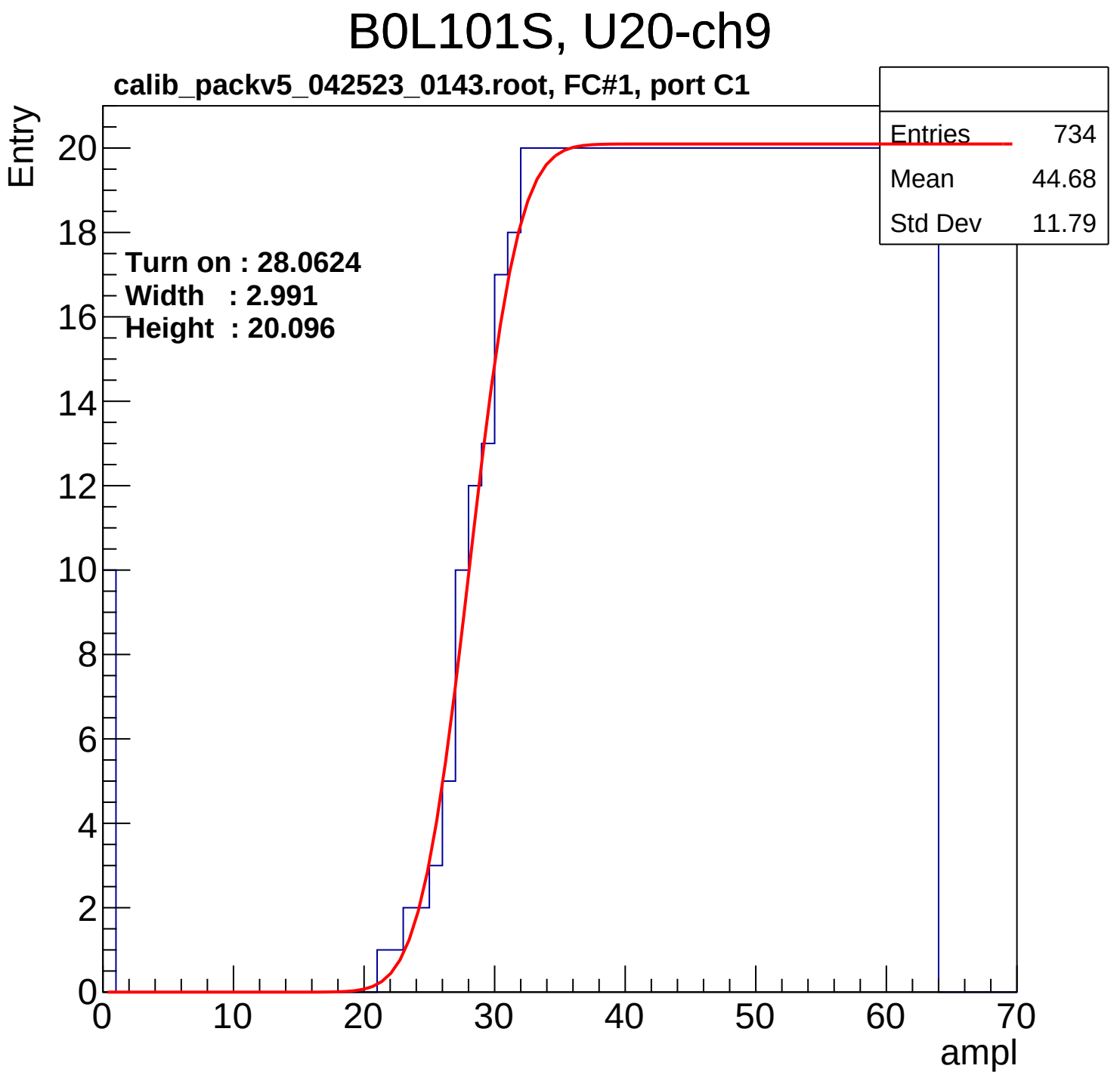
B0L101S, U20-ch9
calib_packv5_042523_0143.root, FC#1, port C1
Entries 734
Mean 44.68
Std Dev 11.79
Turn on : 28.0624
Width : 2.991
Height : 20.096
Entry
ampl
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6
8
10
12
14
16
18
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0
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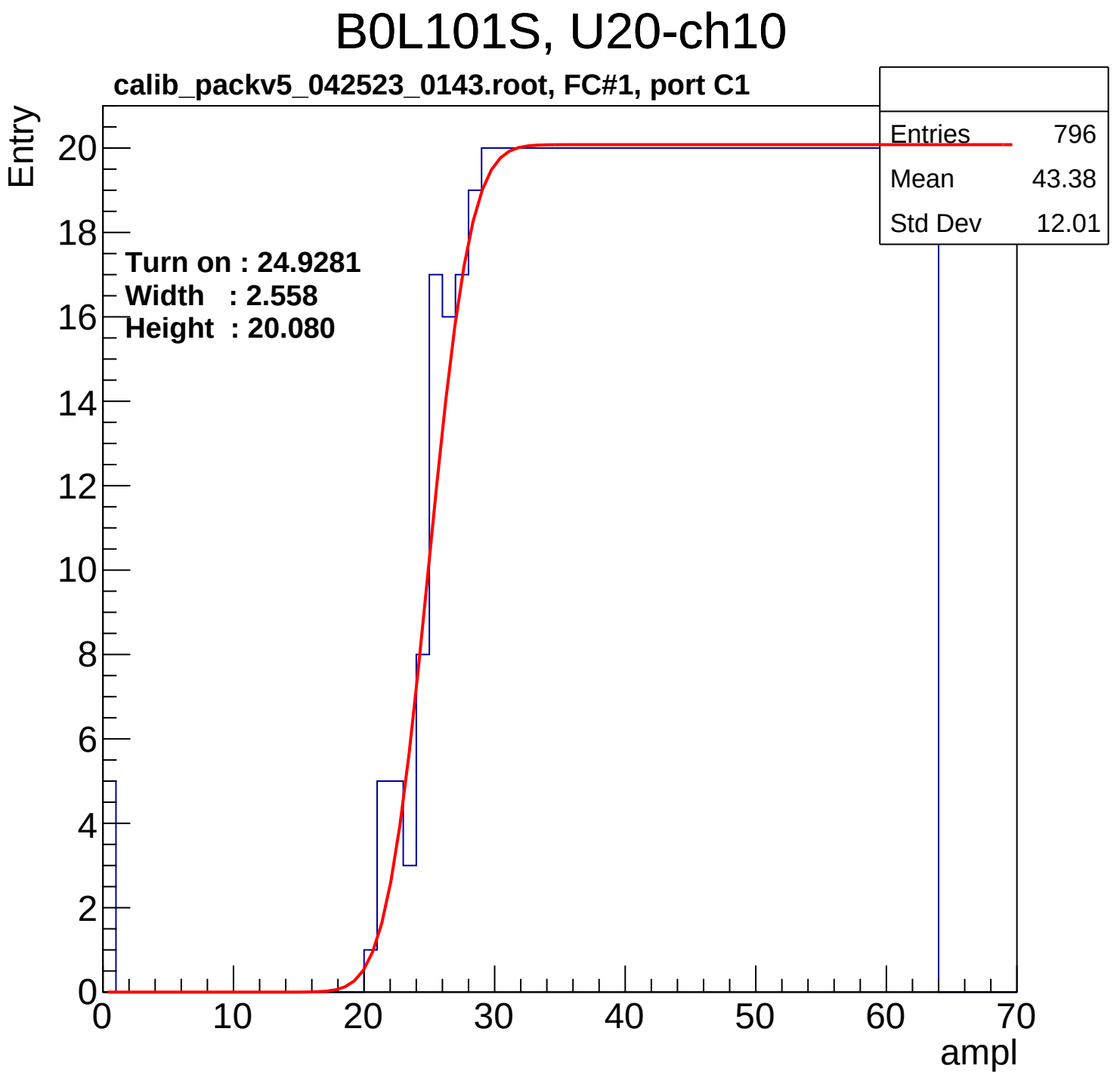
B0L101S, U20-ch10
calib_packv5_042523_0143.root, FC#1, port C1
Entries 796
Mean 43.38
Std Dev 12.01
Turn on : 24.9281
Width : 2.558
Height : 20.080
Entry
ampl
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6
8
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12
14
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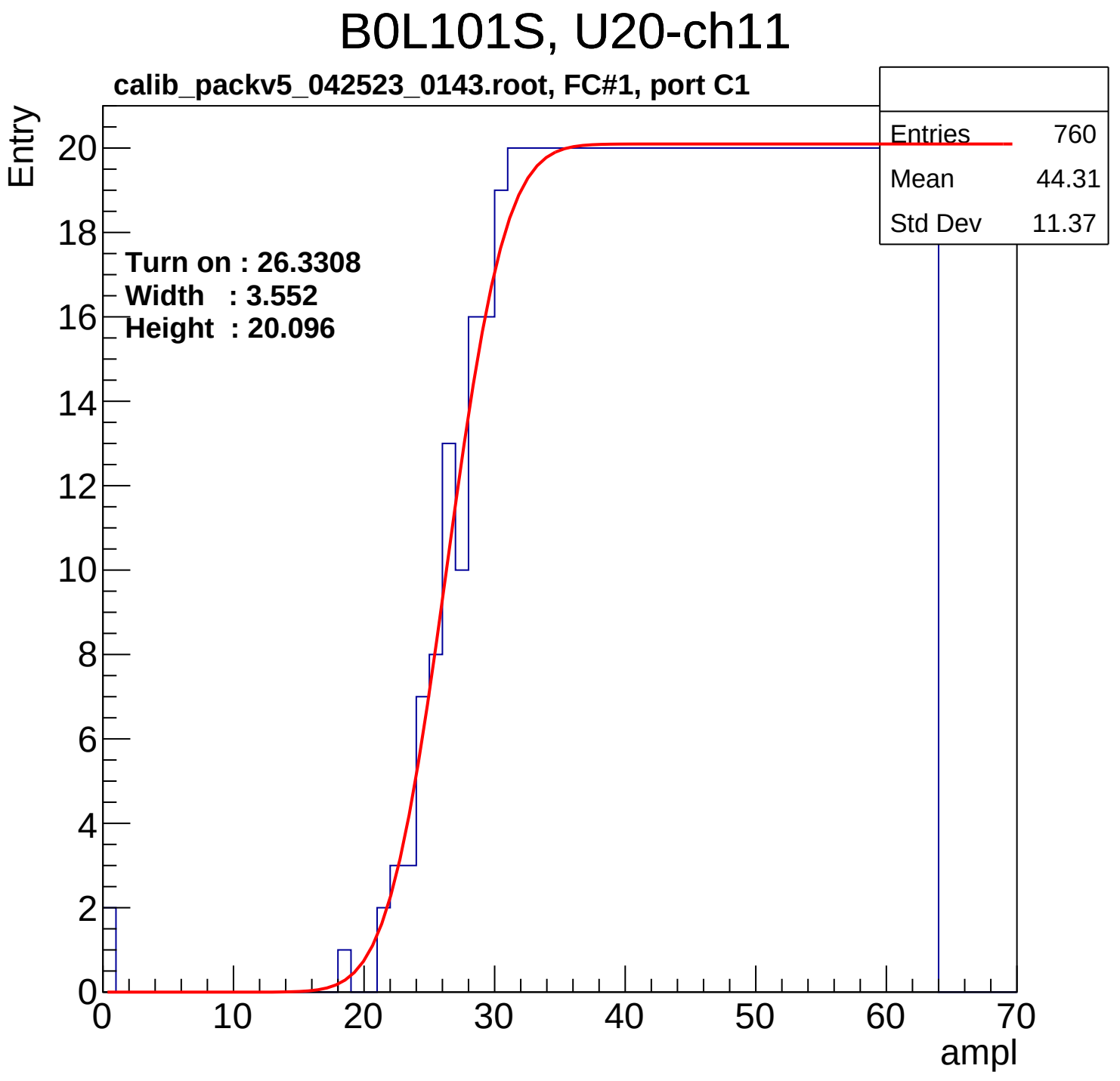
B0L101S, U20-ch11
calib_packv5_042523_0143.root, FC#1, port C1
Entries 760
Mean 44.31
Std Dev 11.37
Turn on : 26.3308
Width : 3.552
Height : 20.096
Entry
ampl
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6
8
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12
14
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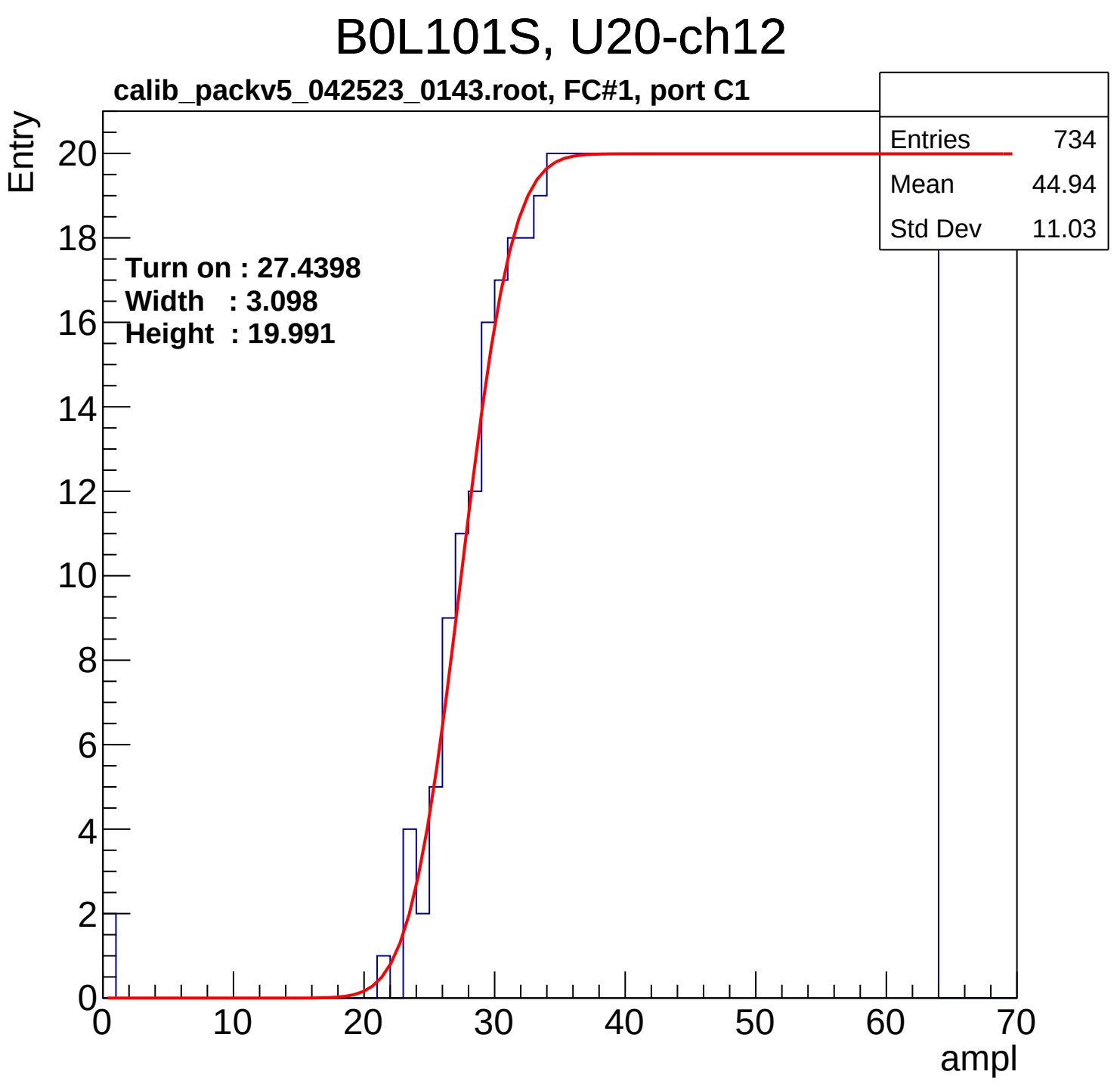
B0L101S, U20-ch12
calib_packv5_042523_0143.root, FC#1, port C1
Entries 734
Mean 44.94
Std Dev 11.03
Turn on : 27.4398
Width : 3.098
Height : 19.991
Entry
ampl
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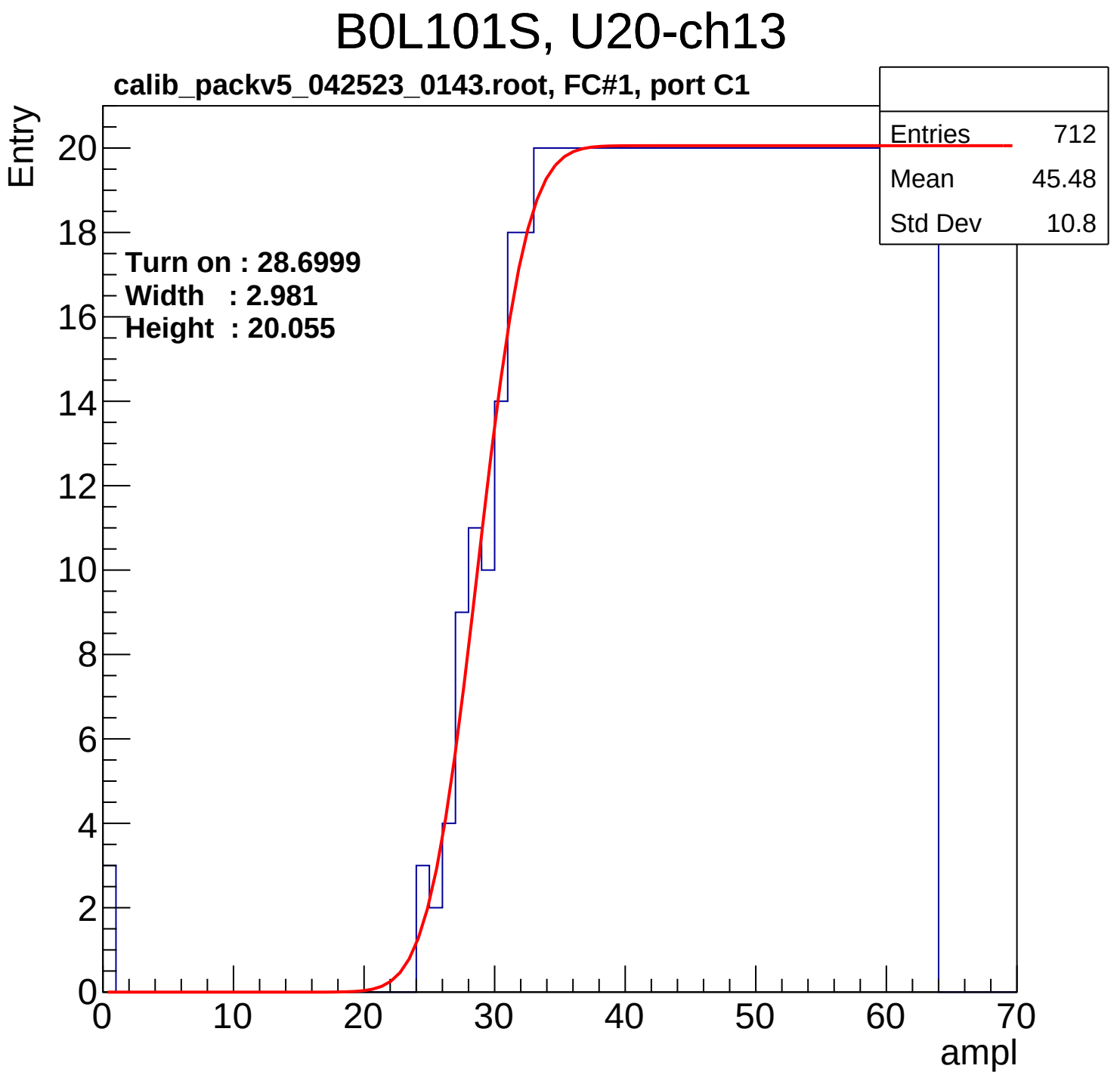
B0L101S, U20-ch13
calib_packv5_042523_0143.root, FC#1, port C1
Entries 712
Mean 45.48
Std Dev 10.8
Turn on : 28.6999
Width : 2.981
Height : 20.055
Entry
ampl
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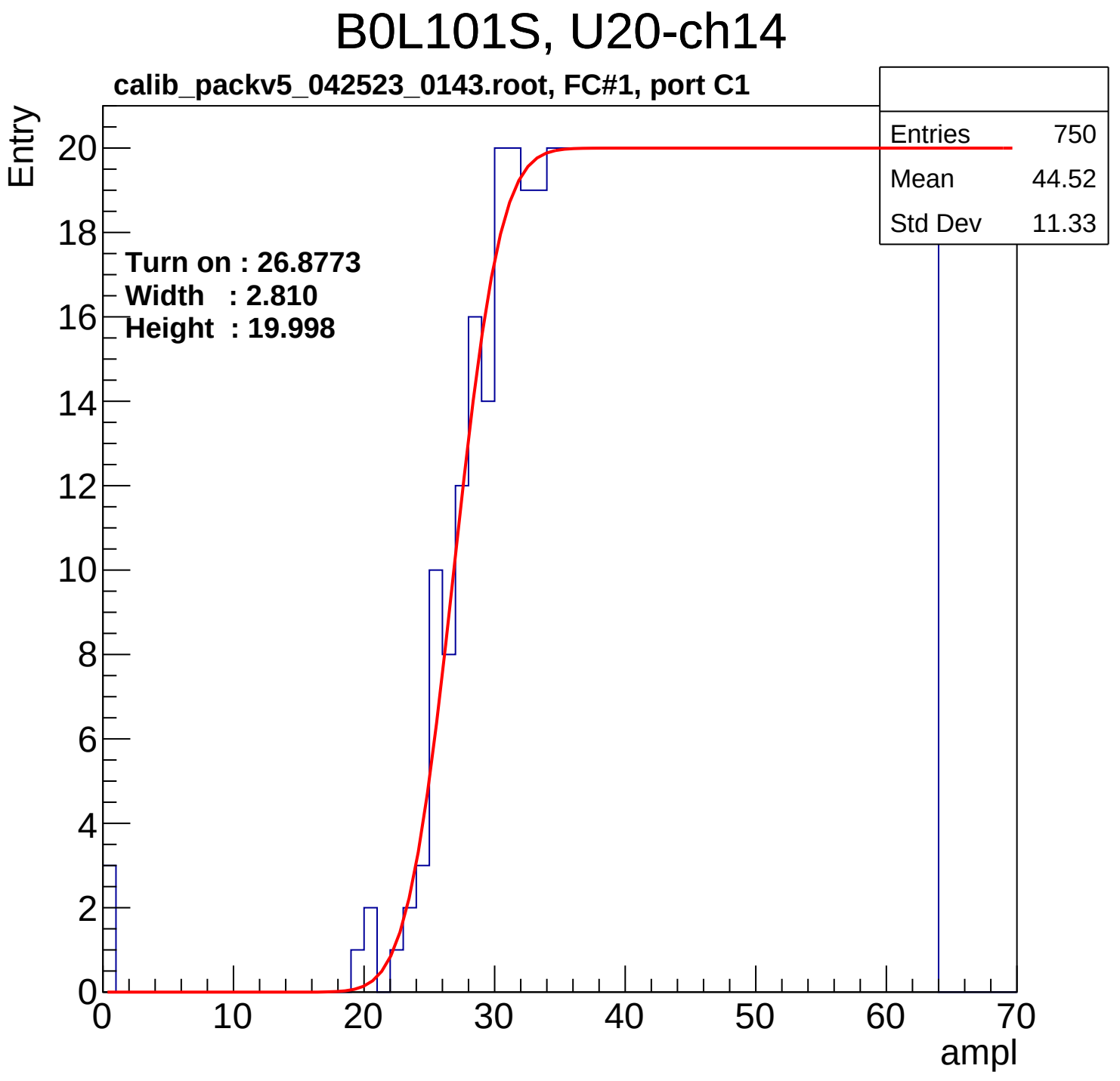
B0L101S, U20-ch14
calib_packv5_042523_0143.root, FC#1, port C1
Entries 750
Mean 44.52
Std Dev 11.33
Turn on : 26.8773
Width : 2.810
Height : 19.998
Entry
ampl
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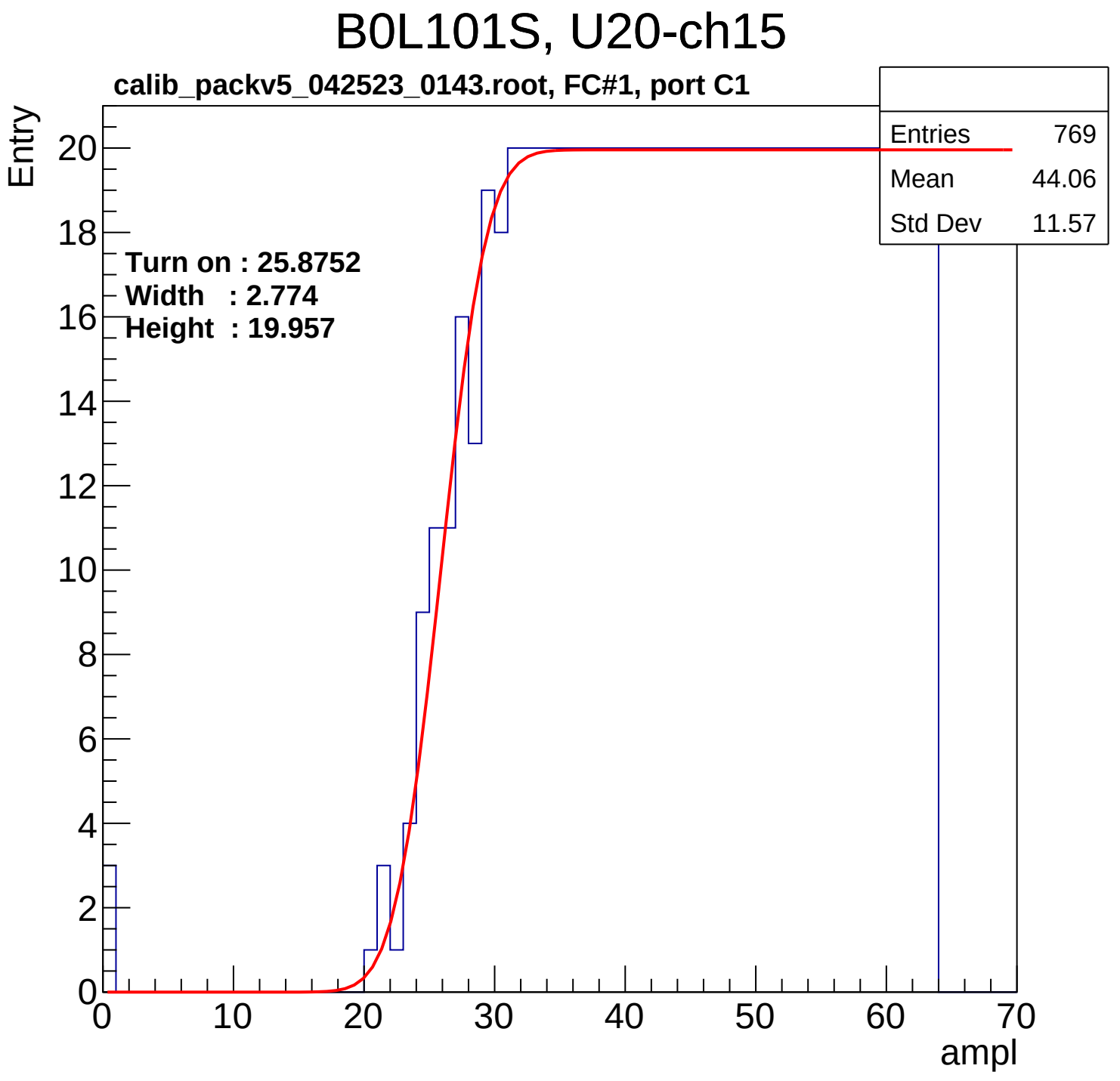
B0L101S, U20-ch15
calib_packv5_042523_0143.root, FC#1, port C1
Entries 769
Mean 44.06
Std Dev 11.57
Turn on : 25.8752
Width : 2.774
Height : 19.957
Entry
ampl
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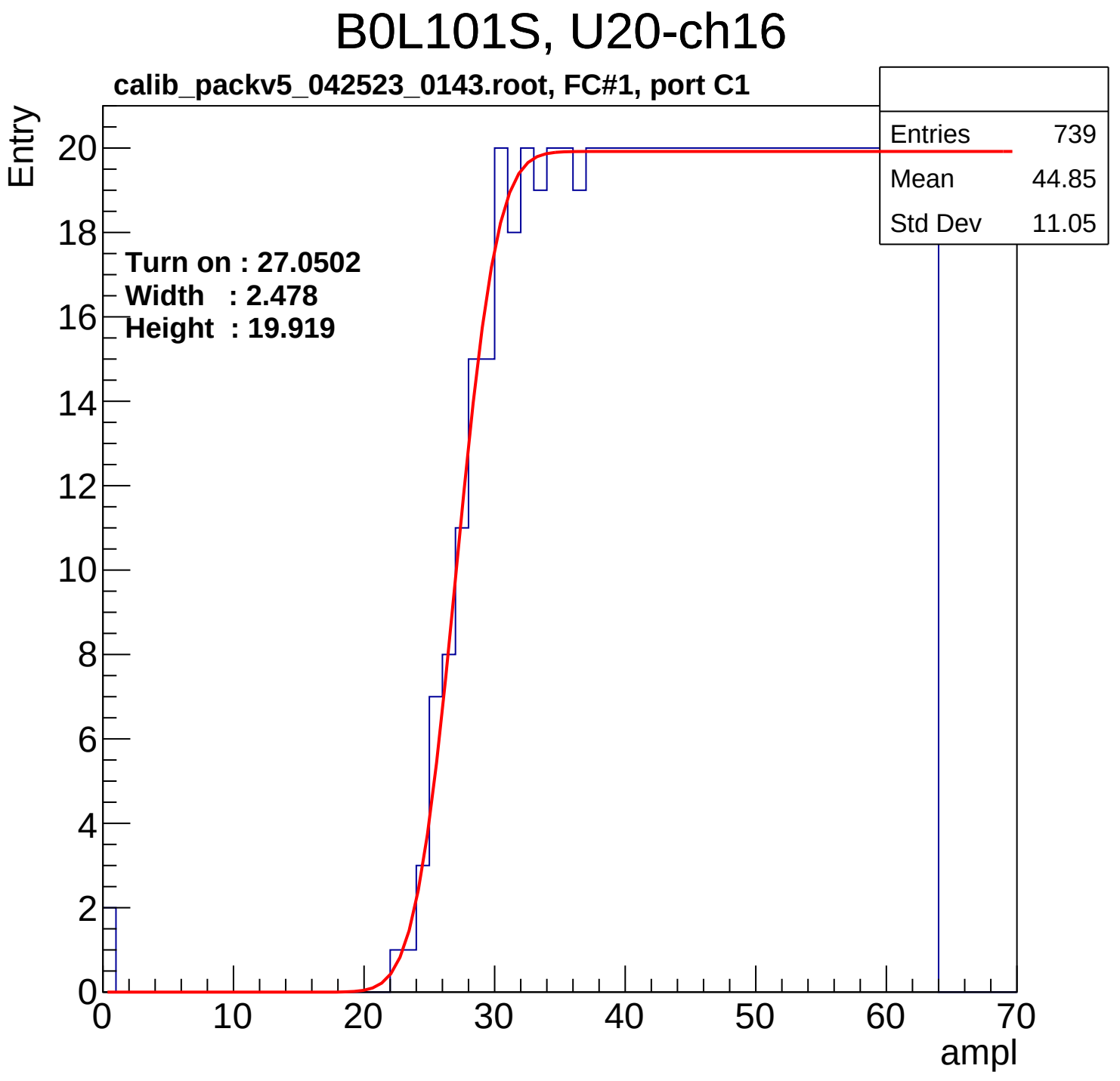
B0L101S, U20-ch16
calib_packv5_042523_0143.root, FC#1, port C1
Entries 739
Mean 44.85
Std Dev 11.05
Turn on : 27.0502
Width : 2.478
Height : 19.919
Entry
ampl
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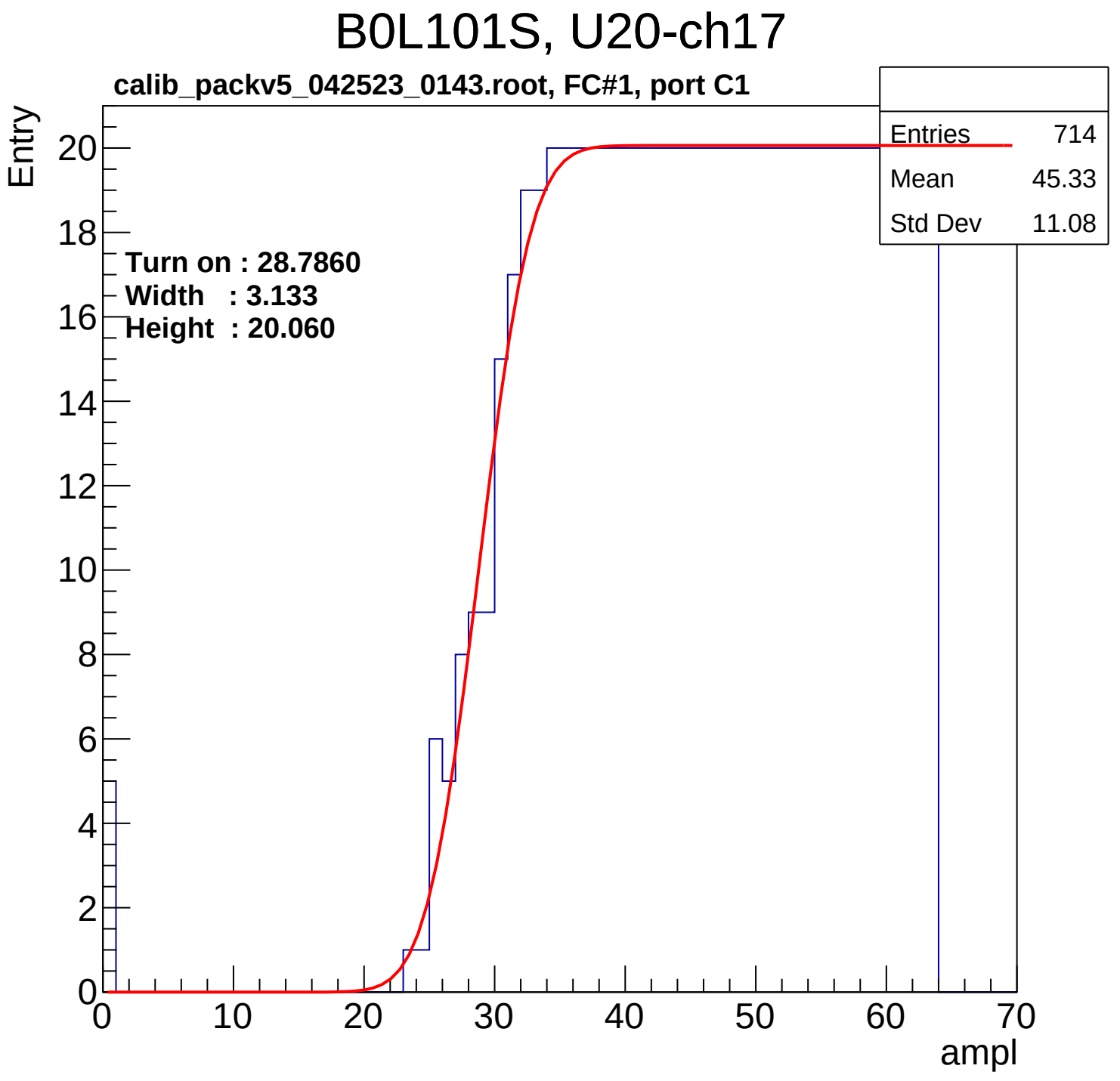
B0L101S, U20-ch17
calib_packv5_042523_0143.root, FC#1, port C1
Entries 714
Mean 45.33
Std Dev 11.08
Turn on : 28.7860
Width : 3.133
Height : 20.060
Entry
ampl
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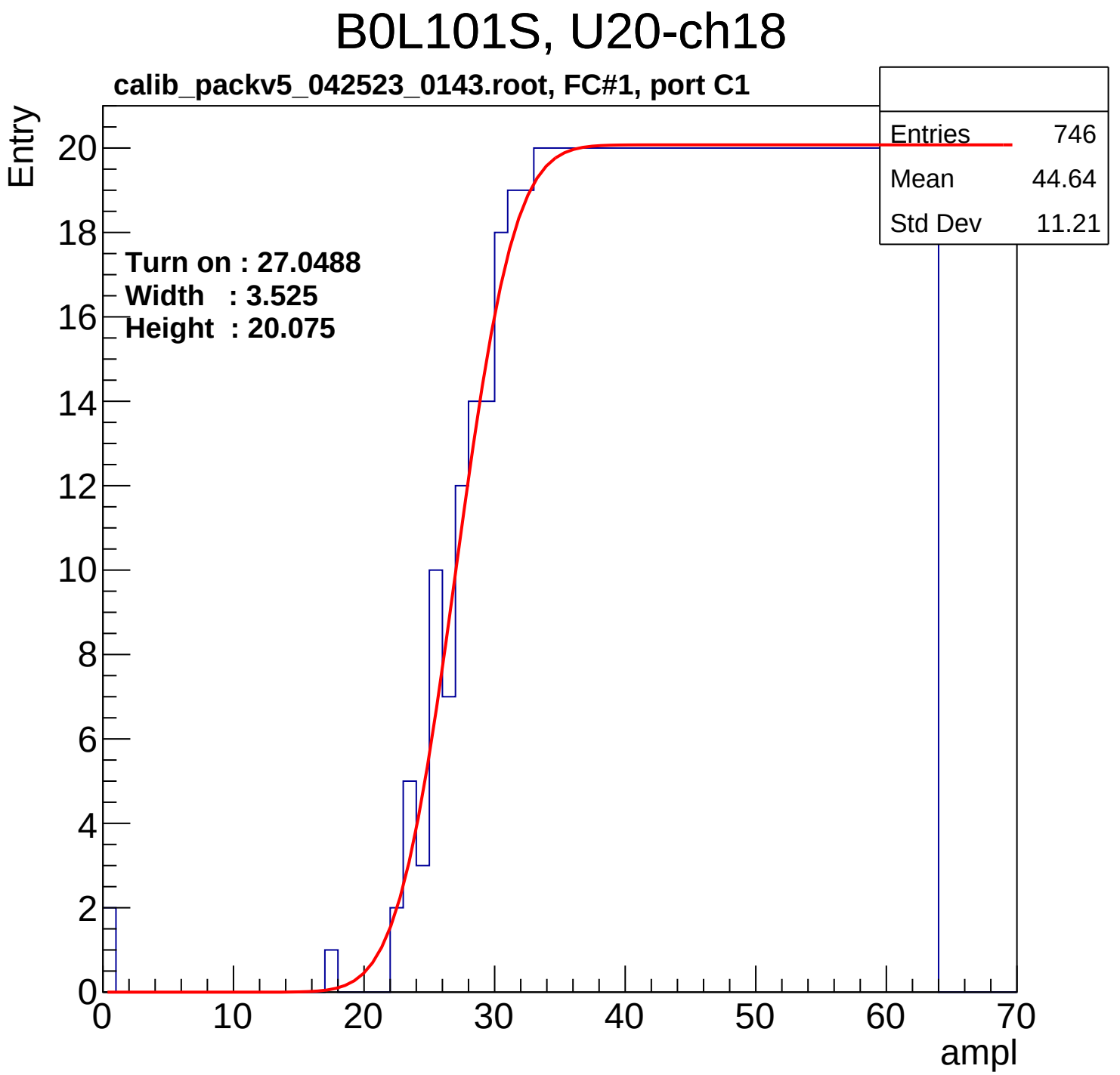
B0L101S, U20-ch18
calib_packv5_042523_0143.root, FC#1, port C1
Entries 746
Mean 44.64
Std Dev 11.21
Turn on : 27.0488
Width : 3.525
Height : 20.075
Entry
ampl
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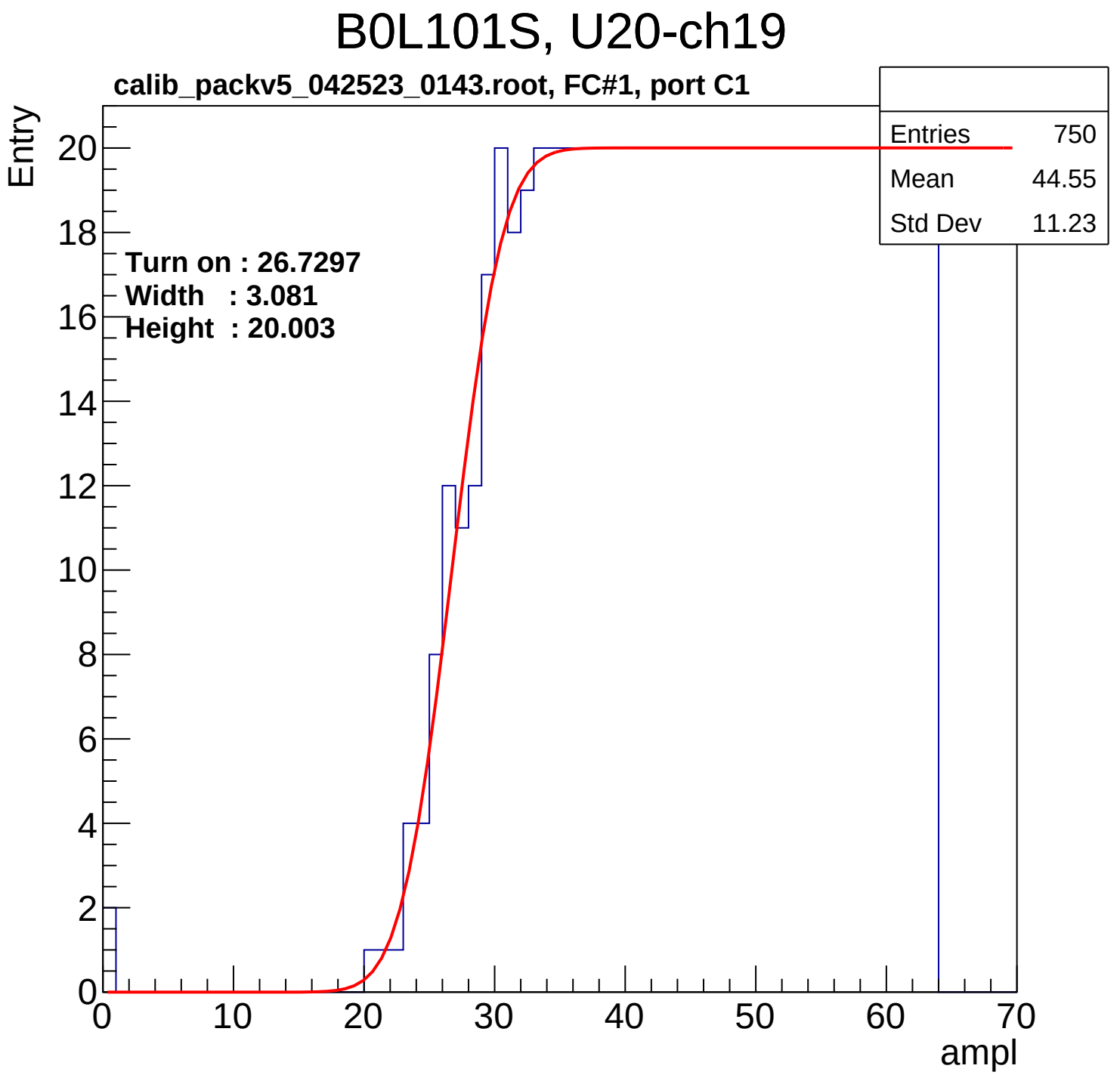
B0L101S, U20-ch19
calib_packv5_042523_0143.root, FC#1, port C1
Entries 750
Mean 44.55
Std Dev 11.23
Turn on : 26.7297
Width : 3.081
Height : 20.003
Entry
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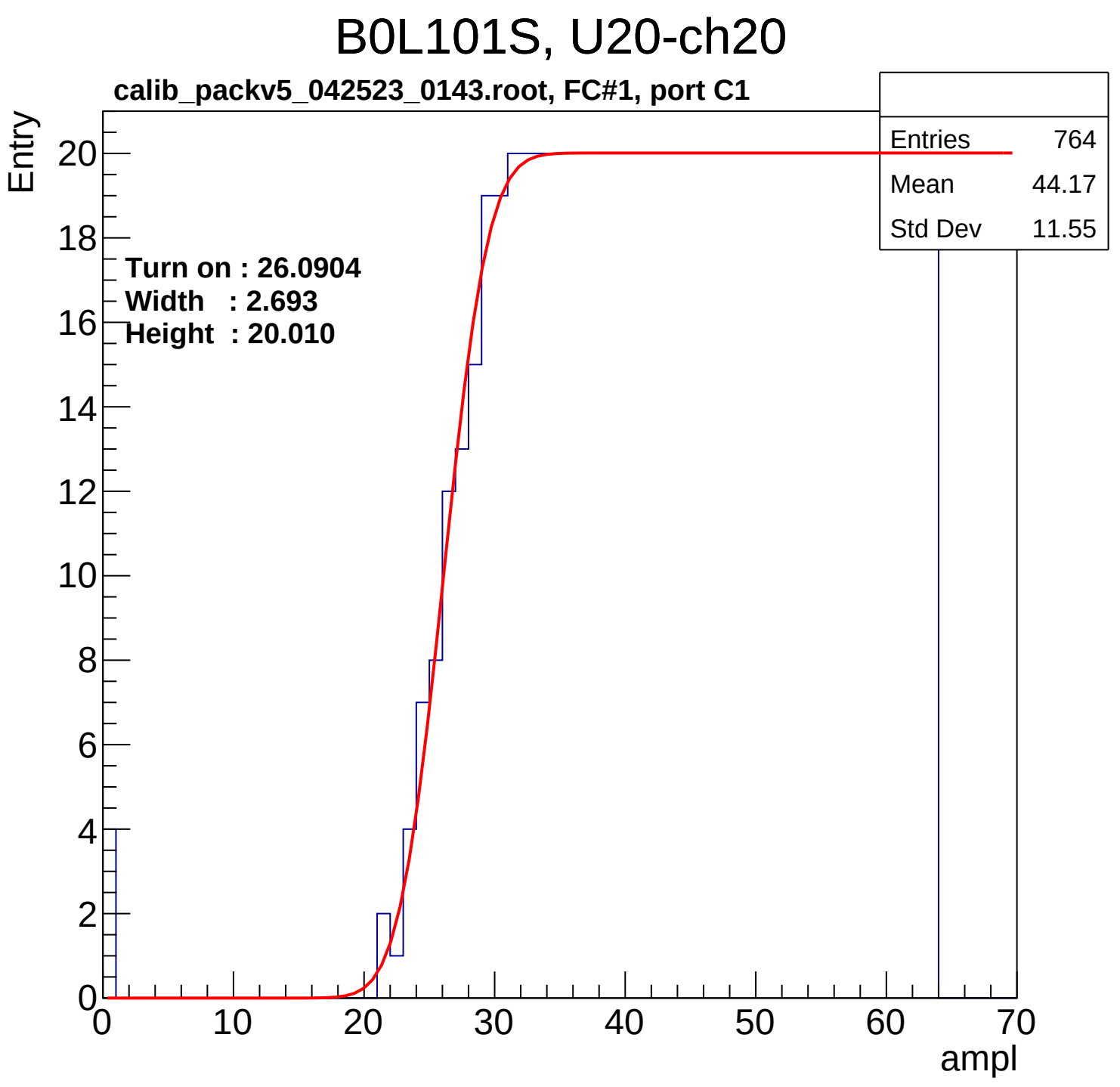
B0L101S, U20-ch20
calib_packv5_042523_0143.root, FC#1, port C1
Entries 764
Mean 44.17
Std Dev 11.55
Turn on : 26.0904
Width : 2.693
Height : 20.010
Entry
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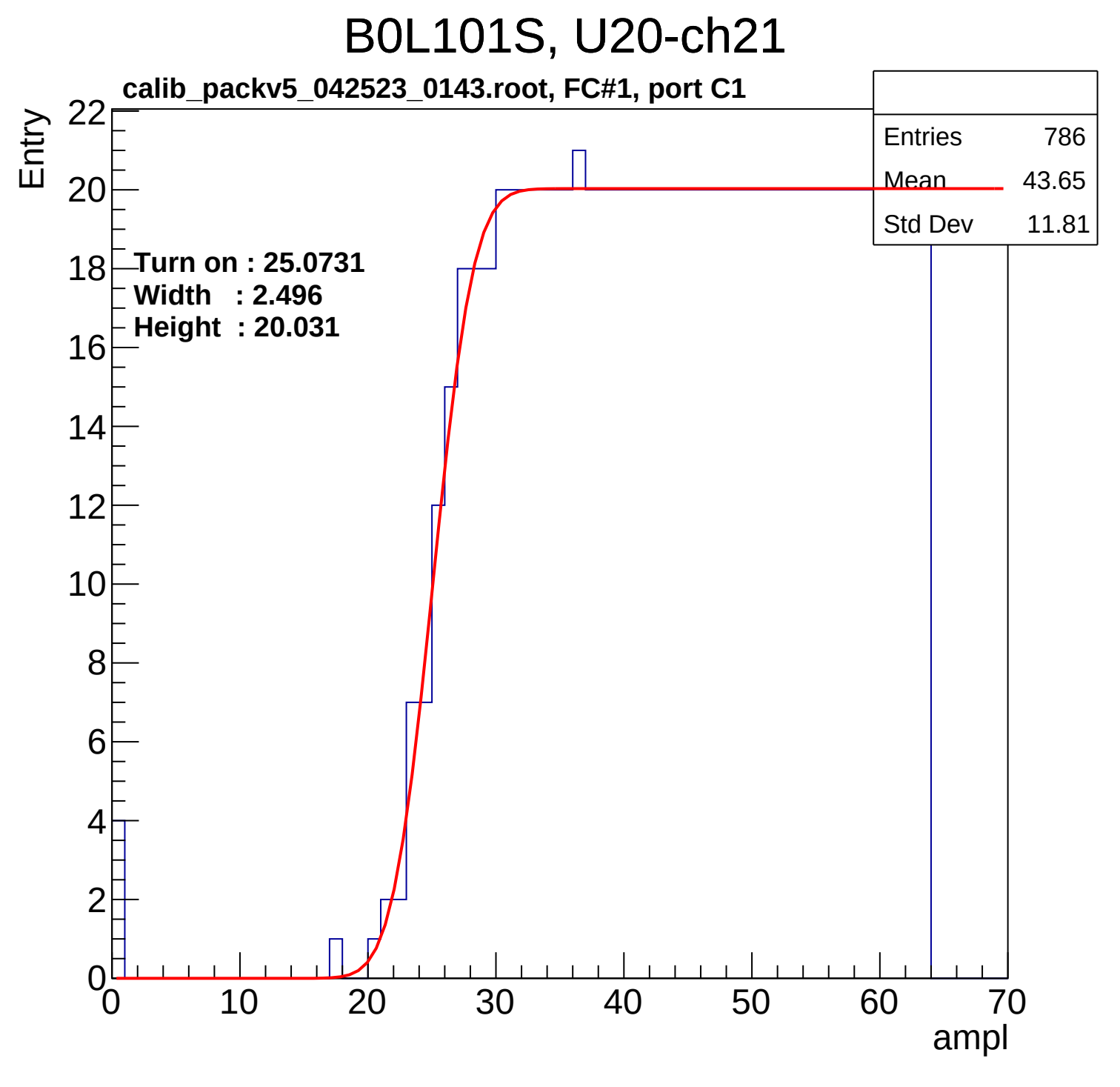
B0L101S, U20-ch21
calib_packv5_042523_0143.root, FC#1, port C1
Entries 786
Mean 43.65
Std Dev 11.81
Turn on : 25.0731
Width : 2.496
Height : 20.031
Entry
ampl
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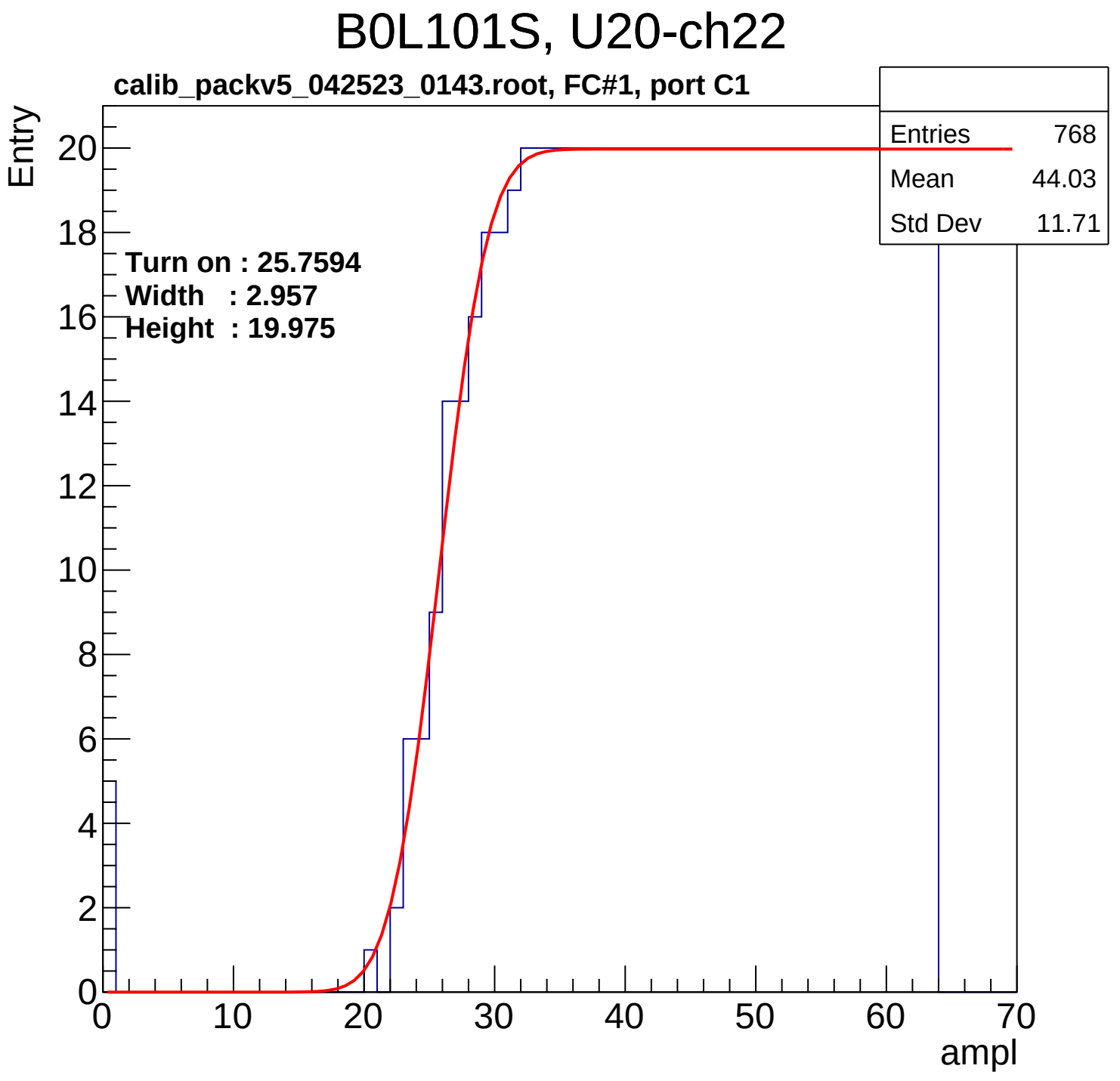
B0L101S, U20-ch22
calib_packv5_042523_0143.root, FC#1, port C1
Entries 768
Mean 44.03
Std Dev 11.71
Turn on : 25.7594
Width : 2.957
Height : 19.975
Entry
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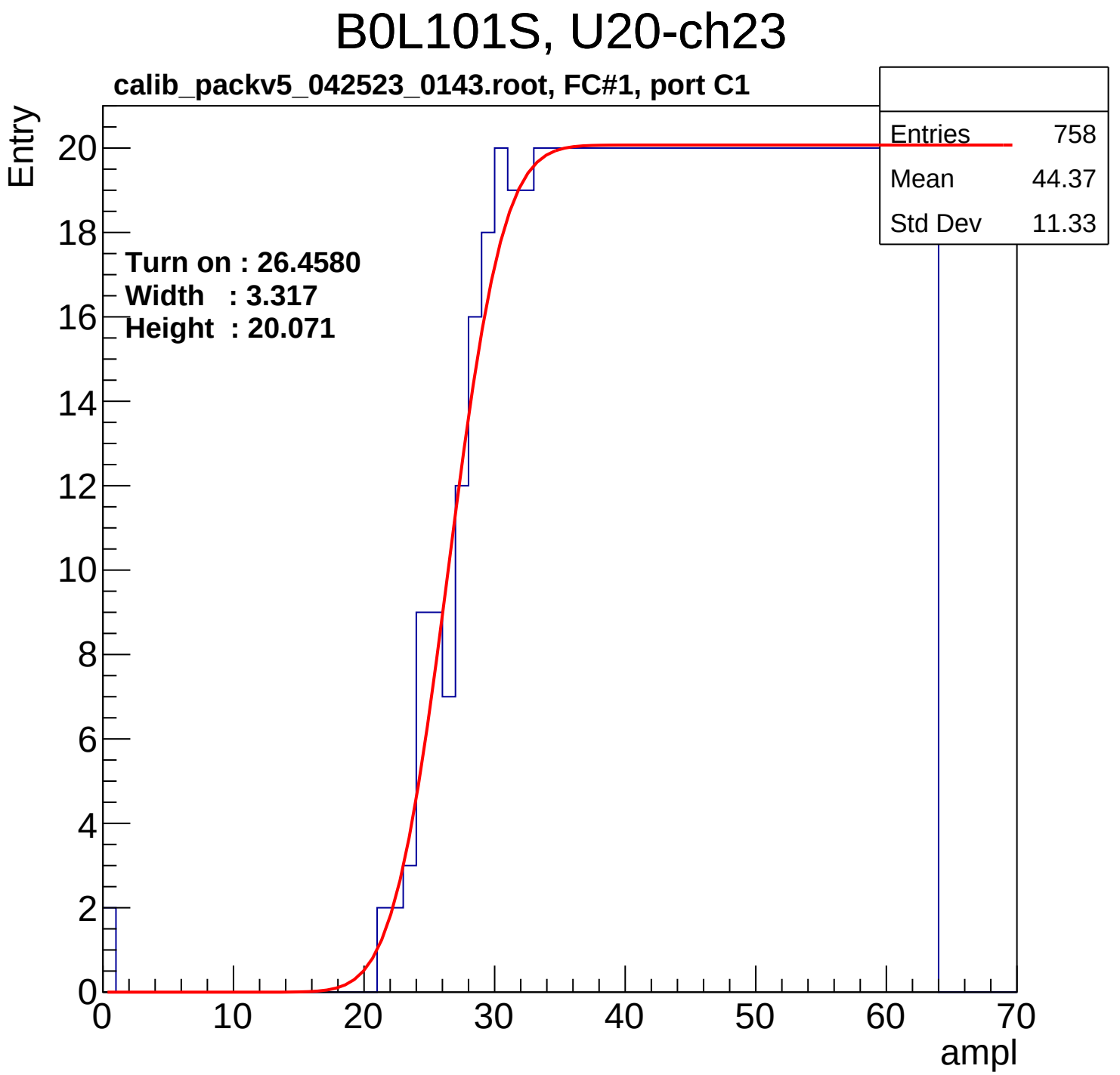
B0L101S, U20-ch23
calib_packv5_042523_0143.root, FC#1, port C1
Entries 758
Mean 44.37
Std Dev 11.33
Turn on : 26.4580
Width : 3.317
Height : 20.071
Entry
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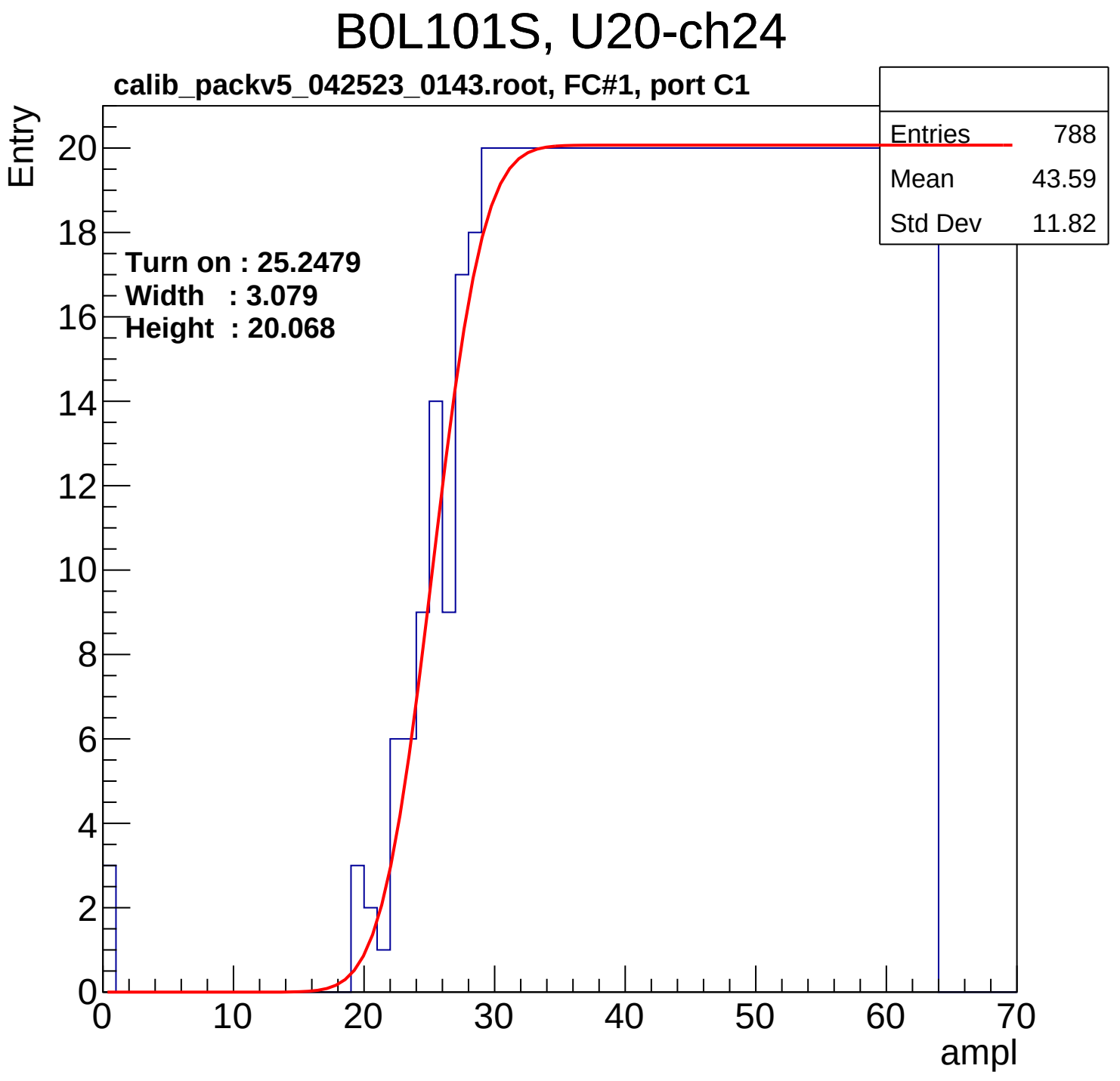
B0L101S, U20-ch24
calib_packv5_042523_0143.root, FC#1, port C1
Entries 788
Mean 43.59
Std Dev 11.82
Turn on : 25.2479
Width : 3.079
Height : 20.068
Entry
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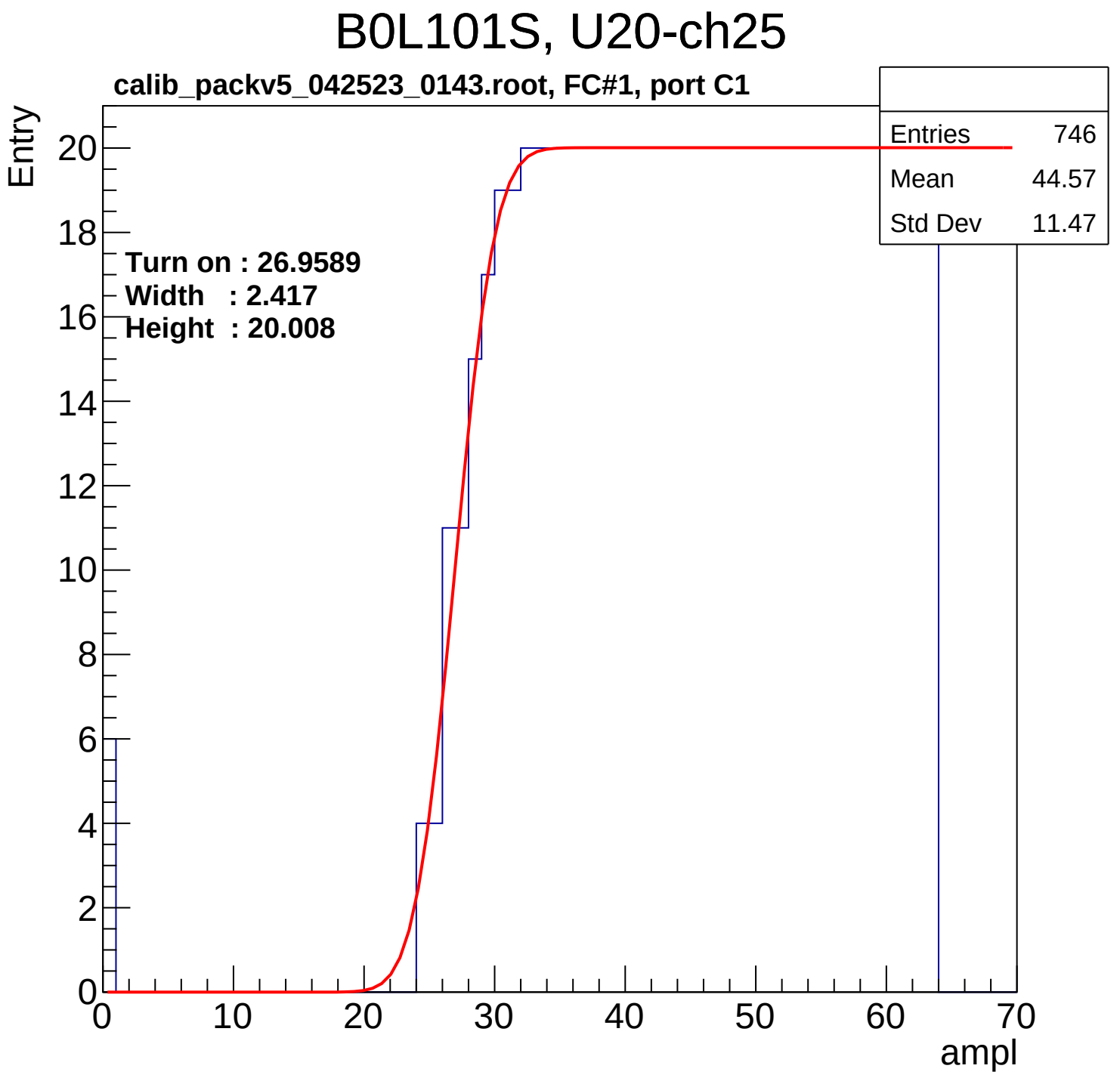
B0L101S, U20-ch25
calib_packv5_042523_0143.root, FC#1, port C1
Entries 746
Mean 44.57
Std Dev 11.47
Turn on : 26.9589
Width : 2.417
Height : 20.008
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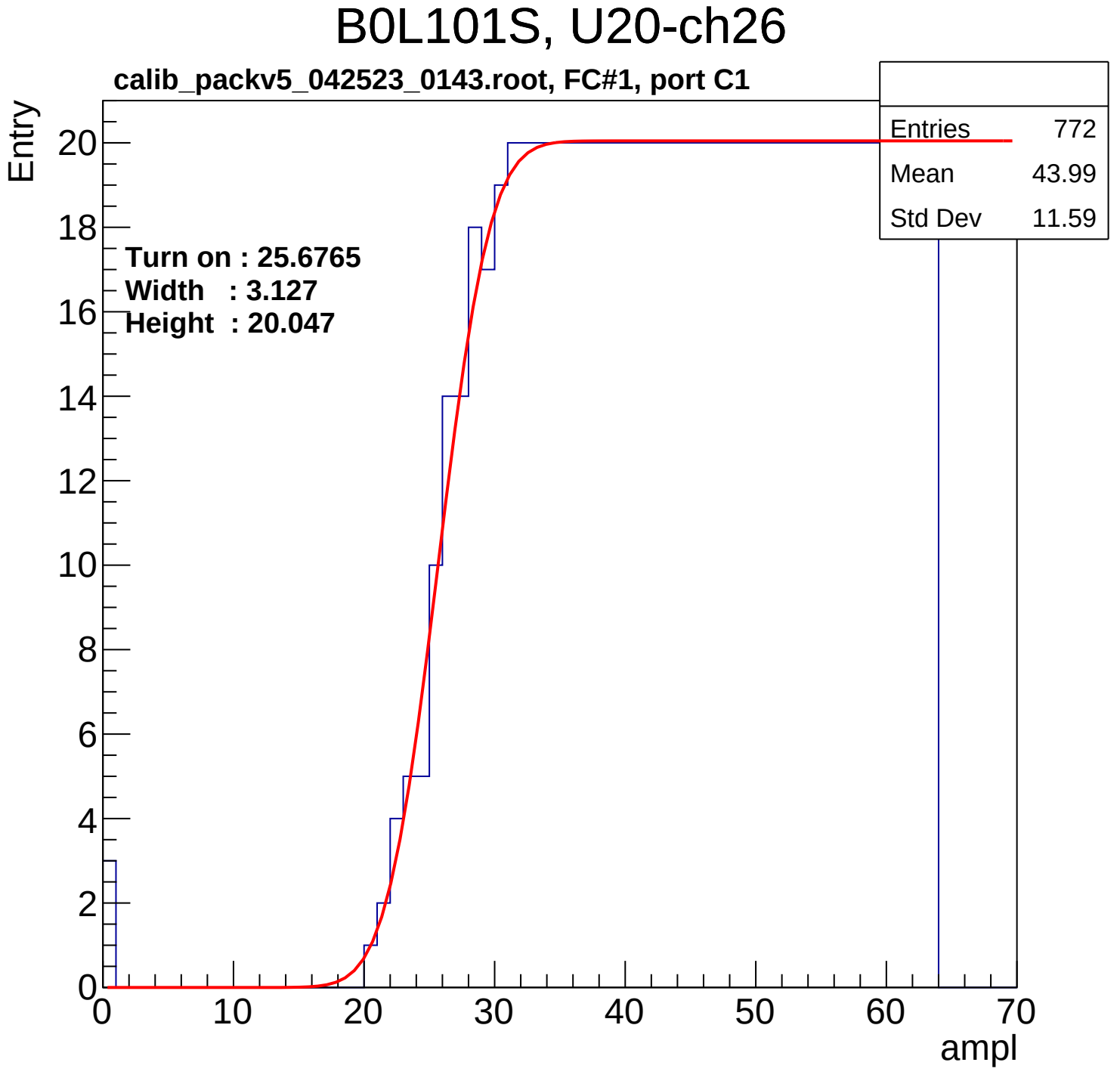
B0L101S, U20-ch26
calib_packv5_042523_0143.root, FC#1, port C1
Entries 772
Mean 43.99
Std Dev 11.59
Turn on : 25.6765
Width : 3.127
Height : 20.047
Entry
ampl
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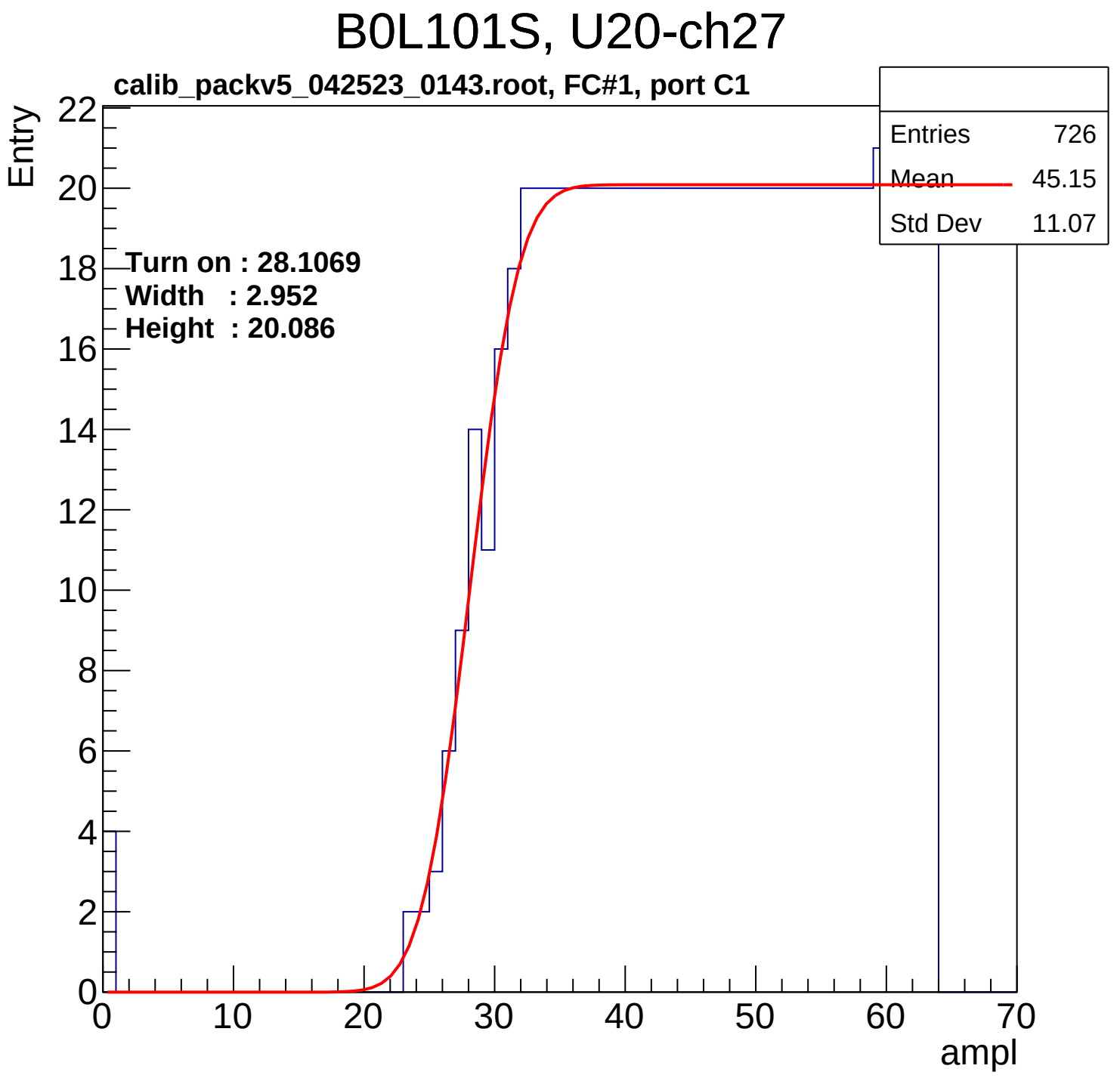
B0L101S, U20-ch27
calib_packv5_042523_0143.root, FC#1, port C1
Entries 726
Mean 45.15
Std Dev 11.07
Turn on : 28.1069
Width : 2.952
Height : 20.086
Entry
ampl
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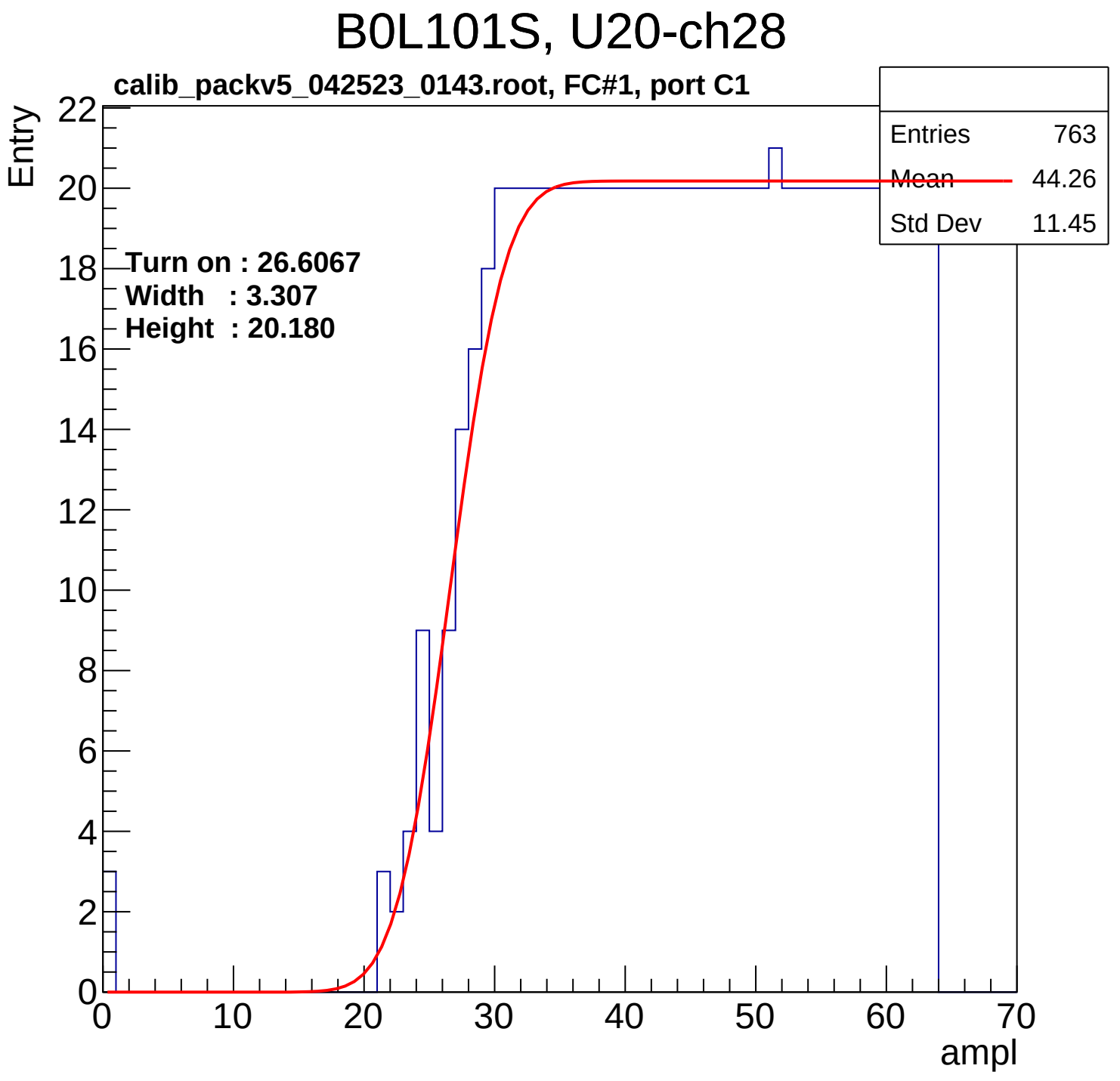
B0L101S, U20-ch28
calib_packv5_042523_0143.root, FC#1, port C1
Entries 763
Mean 44.26
Std Dev 11.45
Turn on : 26.6067
Width : 3.307
Height : 20.180
Entry
ampl
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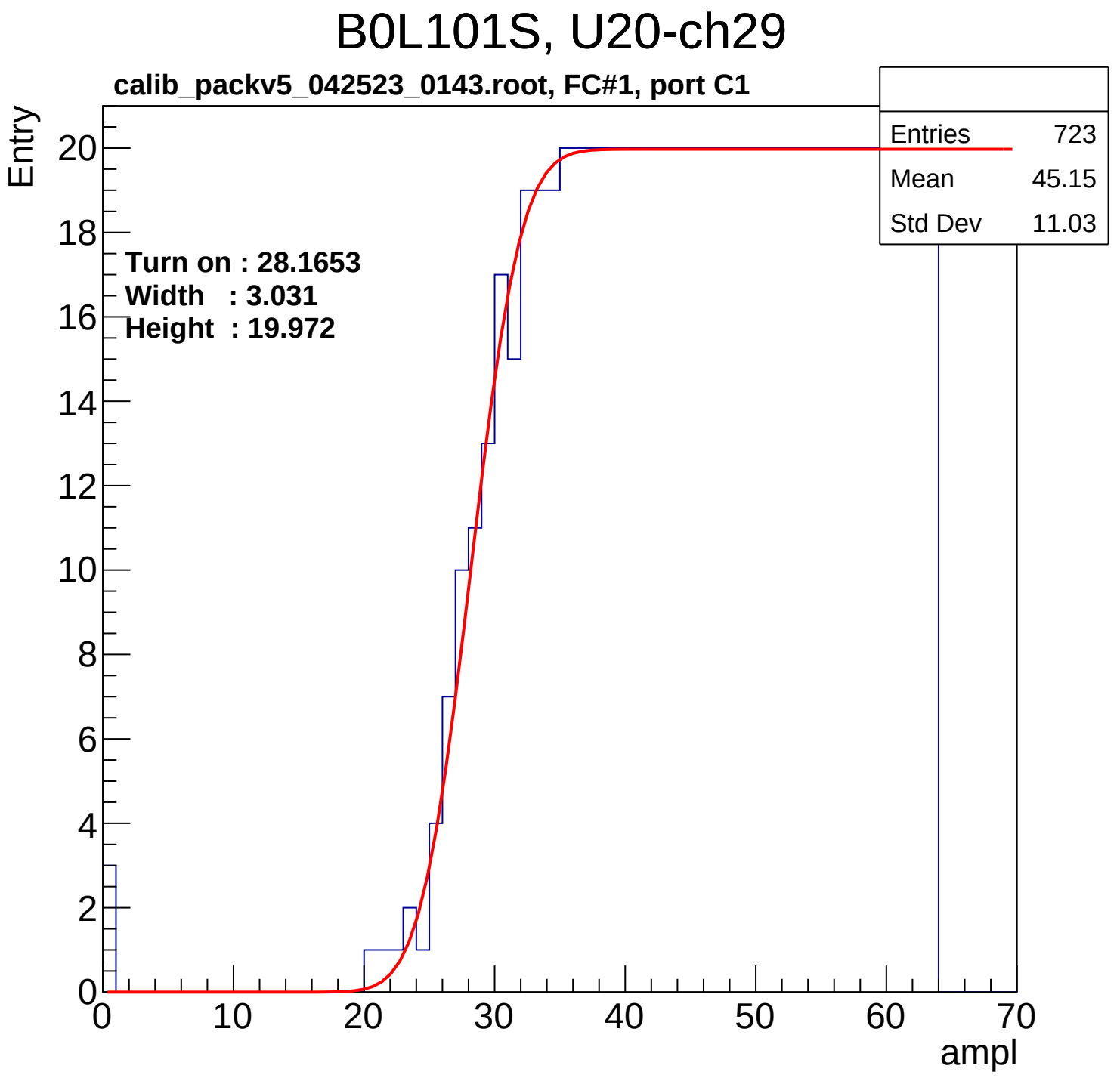
B0L101S, U20-ch29
calib_packv5_042523_0143.root, FC#1, port C1
Entries 723
Mean 45.15
Std Dev 11.03
Turn on : 28.1653
Width : 3.031
Height : 19.972
Entry
ampl
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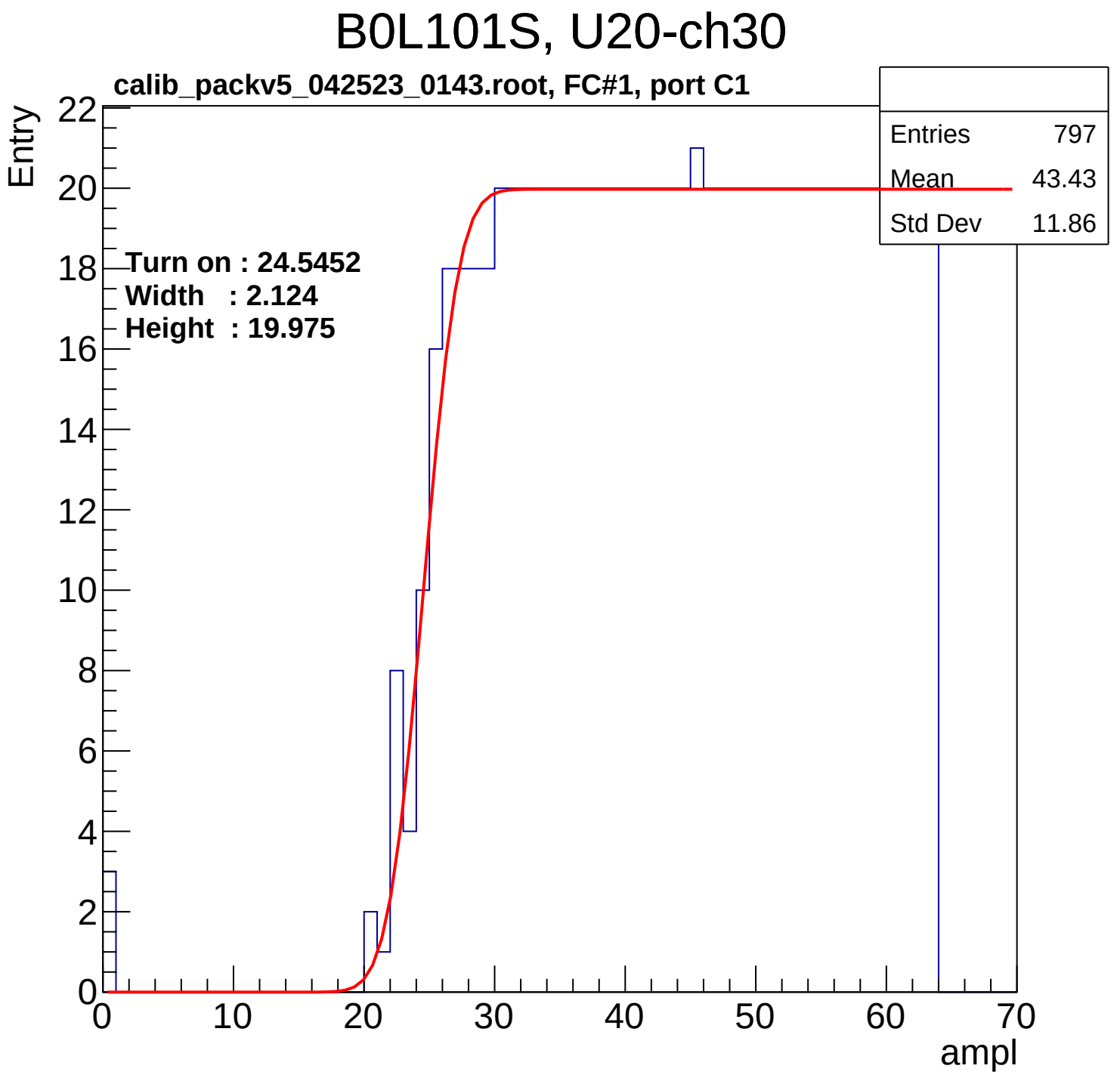
B0L101S, U20-ch30
calib_packv5_042523_0143.root, FC#1, port C1
Entries 797
Mean 43.43
Std Dev 11.86
Turn on : 24.5452
Width : 2.124
Height : 19.975
Entry
ampl
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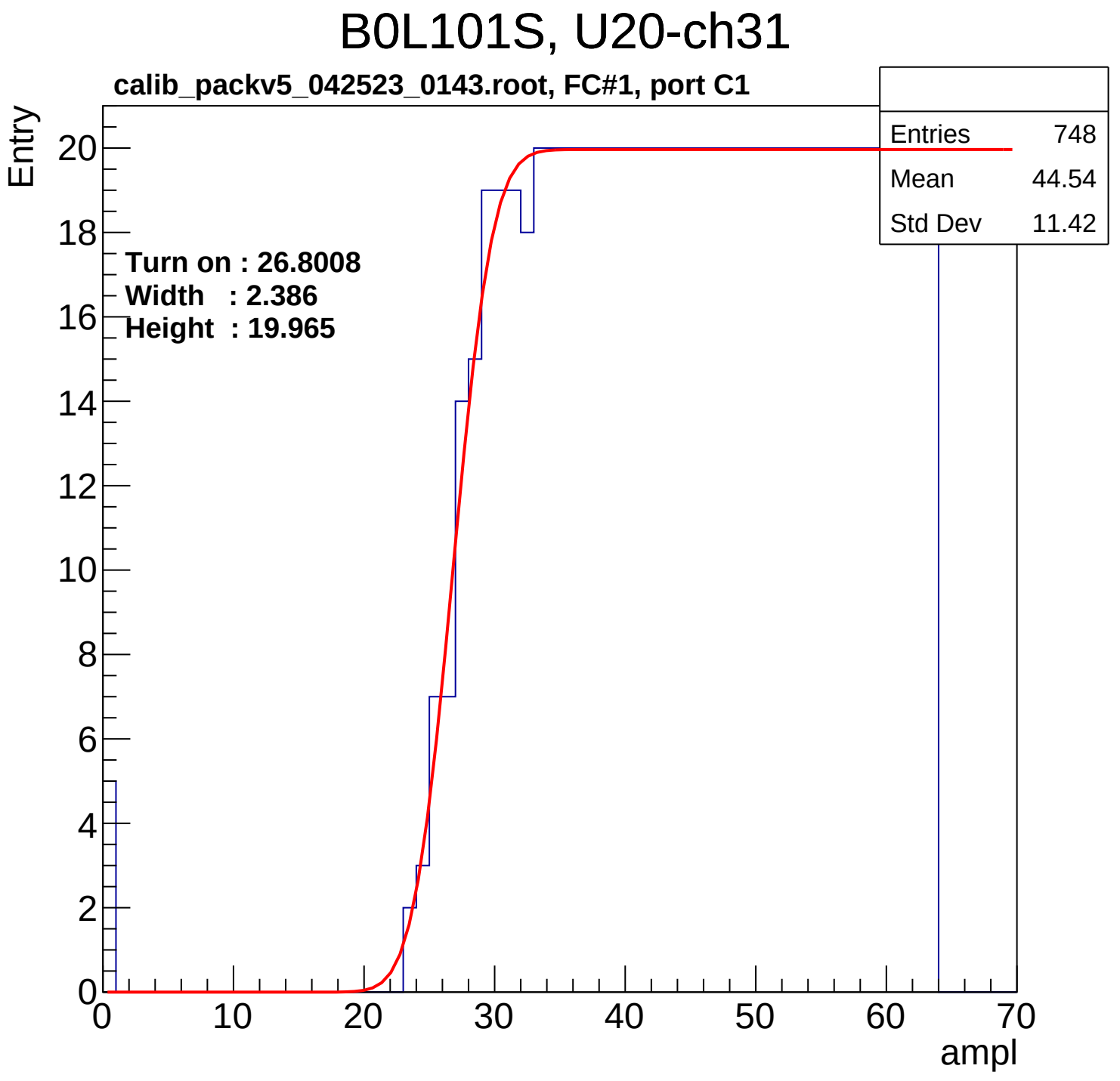
B0L101S, U20-ch31
calib_packv5_042523_0143.root, FC#1, port C1
Entries 748
Mean 44.54
Std Dev 11.42
Turn on : 26.8008
Width : 2.386
Height : 19.965
Entry
ampl
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8
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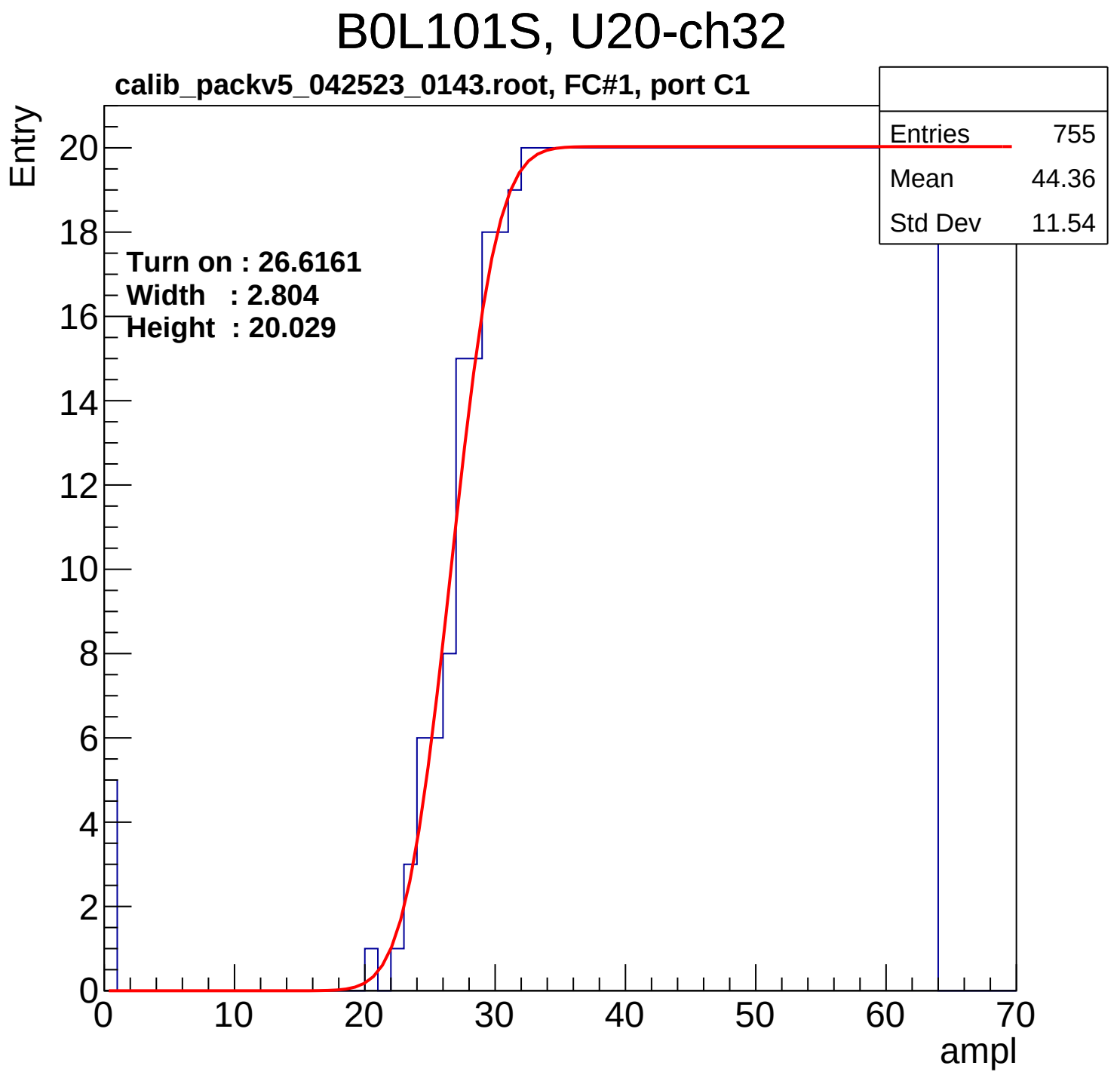
B0L101S, U20-ch32
calib_packv5_042523_0143.root, FC#1, port C1
Entries 755
Mean 44.36
Std Dev 11.54
Turn on : 26.6161
Width : 2.804
Height : 20.029
Entry
ampl
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8
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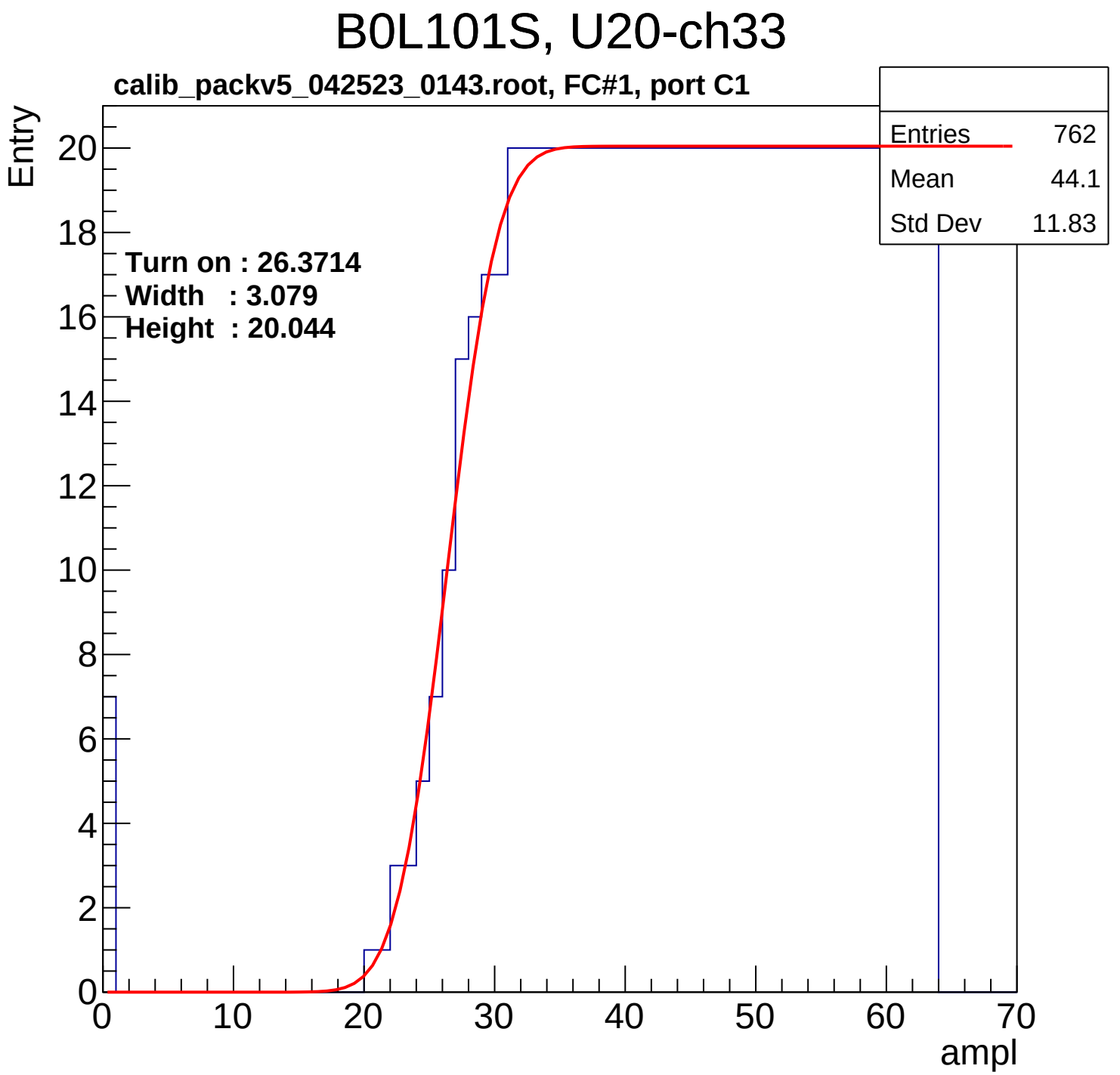
B0L101S, U20-ch33
calib_packv5_042523_0143.root, FC#1, port C1
Entries 762
Mean 44.1
Std Dev 11.83
Turn on : 26.3714
Width : 3.079
Height : 20.044
Entry
ampl
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8
10
12
14
16
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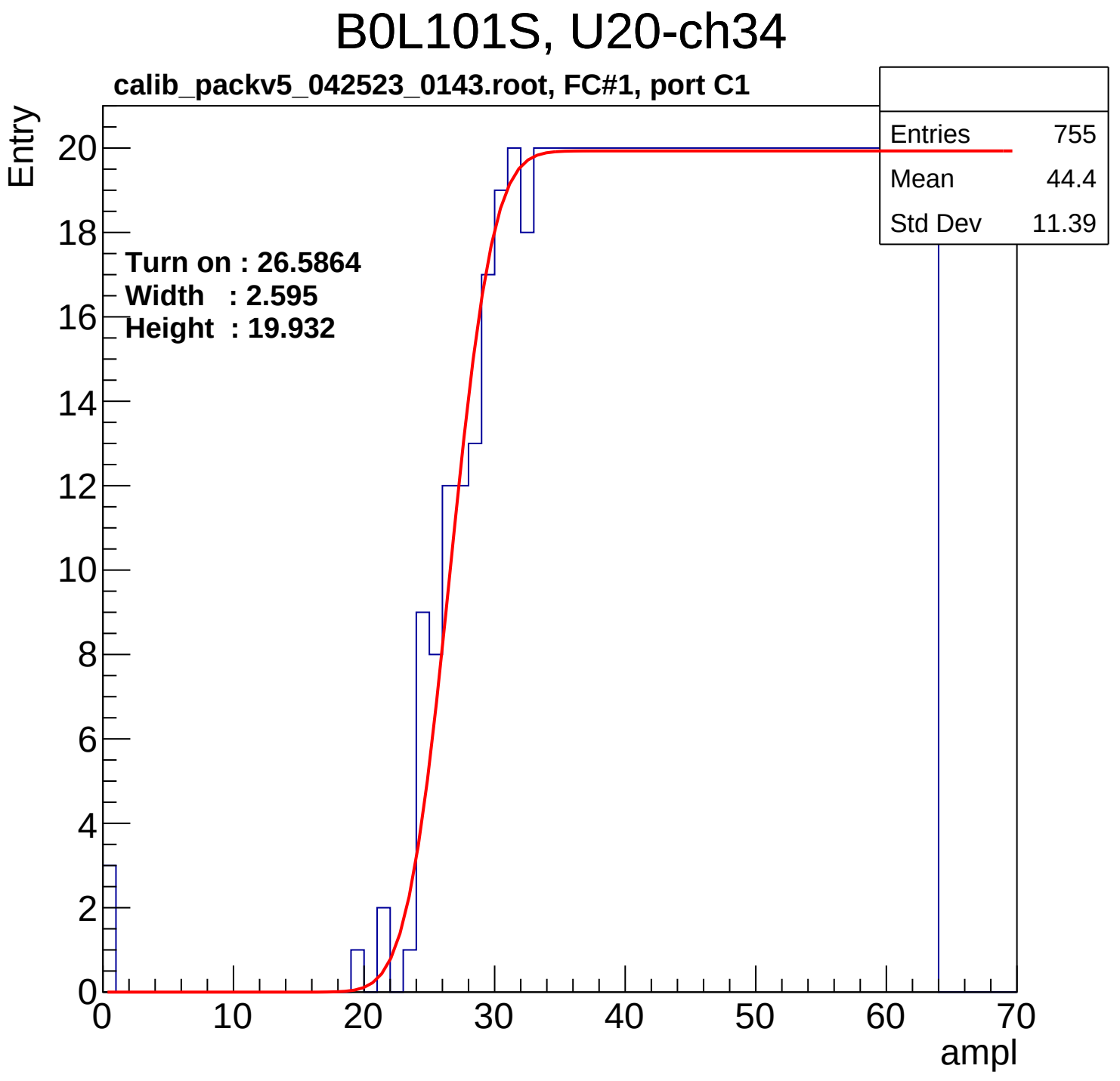
B0L101S, U20-ch34
calib_packv5_042523_0143.root, FC#1, port C1
Entries 755
Mean 44.4
Std Dev 11.39
Turn on : 26.5864
Width : 2.595
Height : 19.932
Entry
ampl
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6
8
10
12
14
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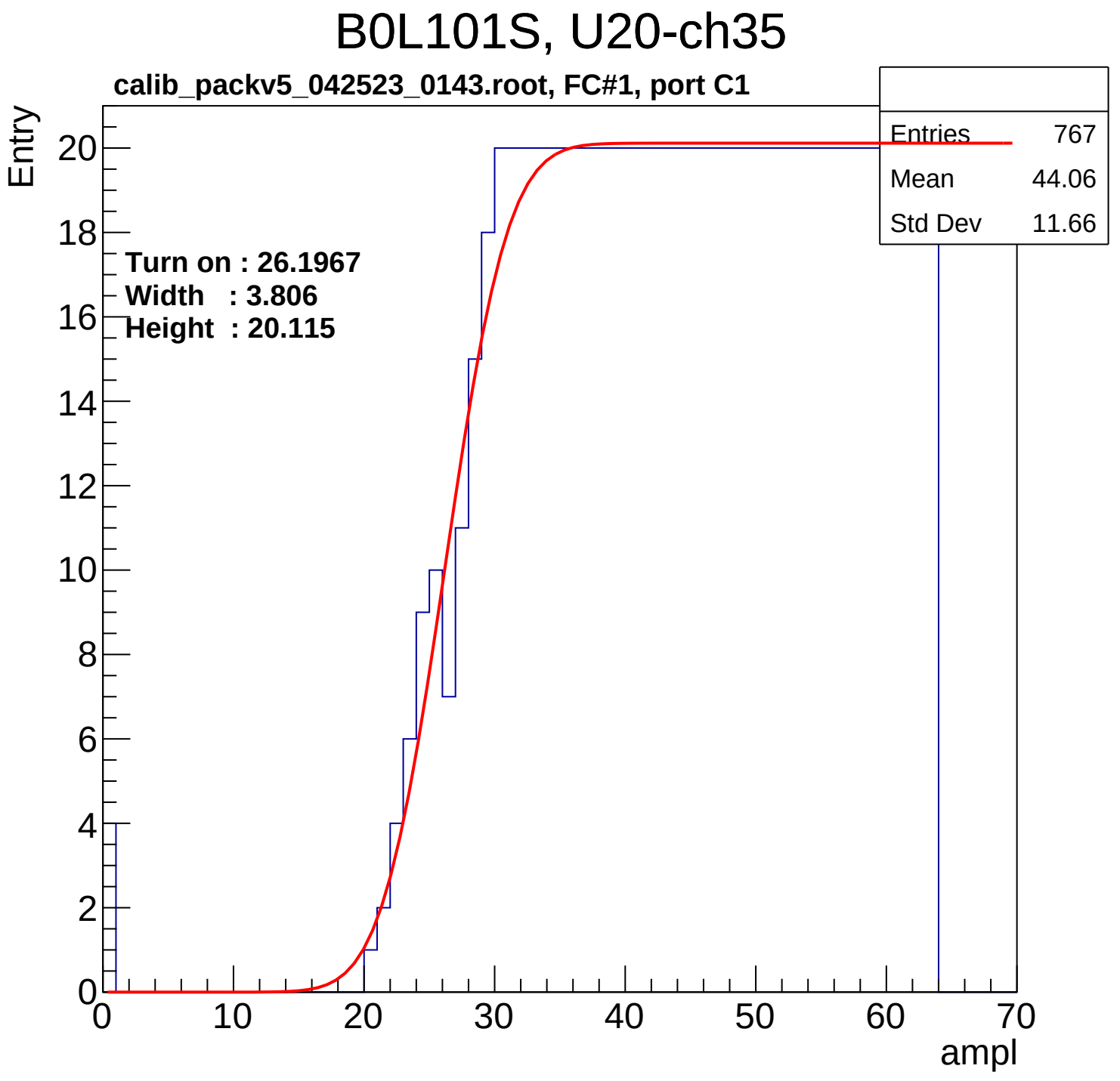
B0L101S, U20-ch35
calib_packv5_042523_0143.root, FC#1, port C1
Entries 767
Mean 44.06
Std Dev 11.66
Turn on : 26.1967
Width : 3.806
Height : 20.115
Entry
ampl
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6
8
10
12
14
16
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0
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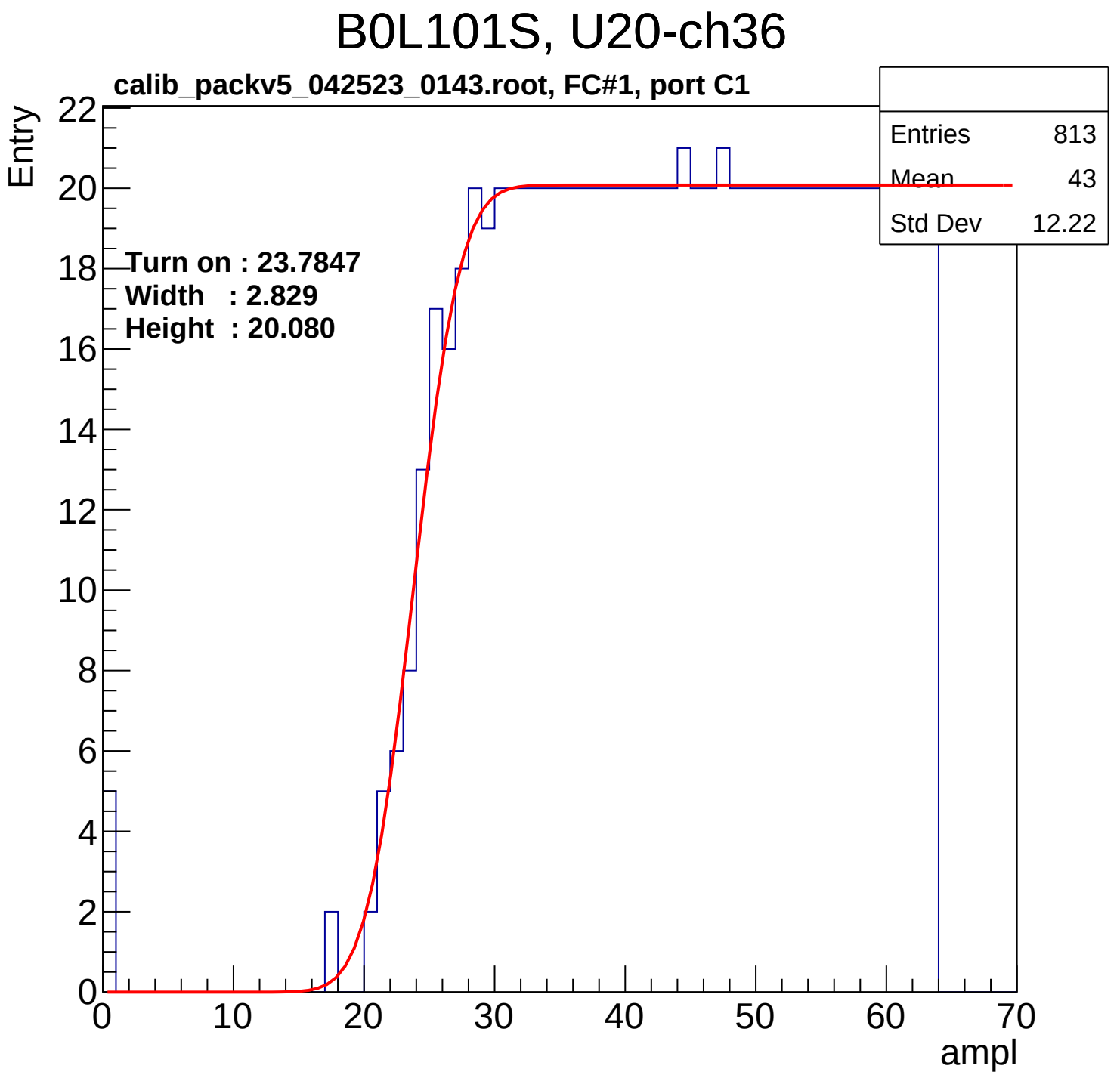
B0L101S, U20-ch36
calib_packv5_042523_0143.root, FC#1, port C1
Entries 813
Mean 43
Std Dev 12.22
Turn on : 23.7847
Width : 2.829
Height : 20.080
Entry
ampl
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8
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16
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0
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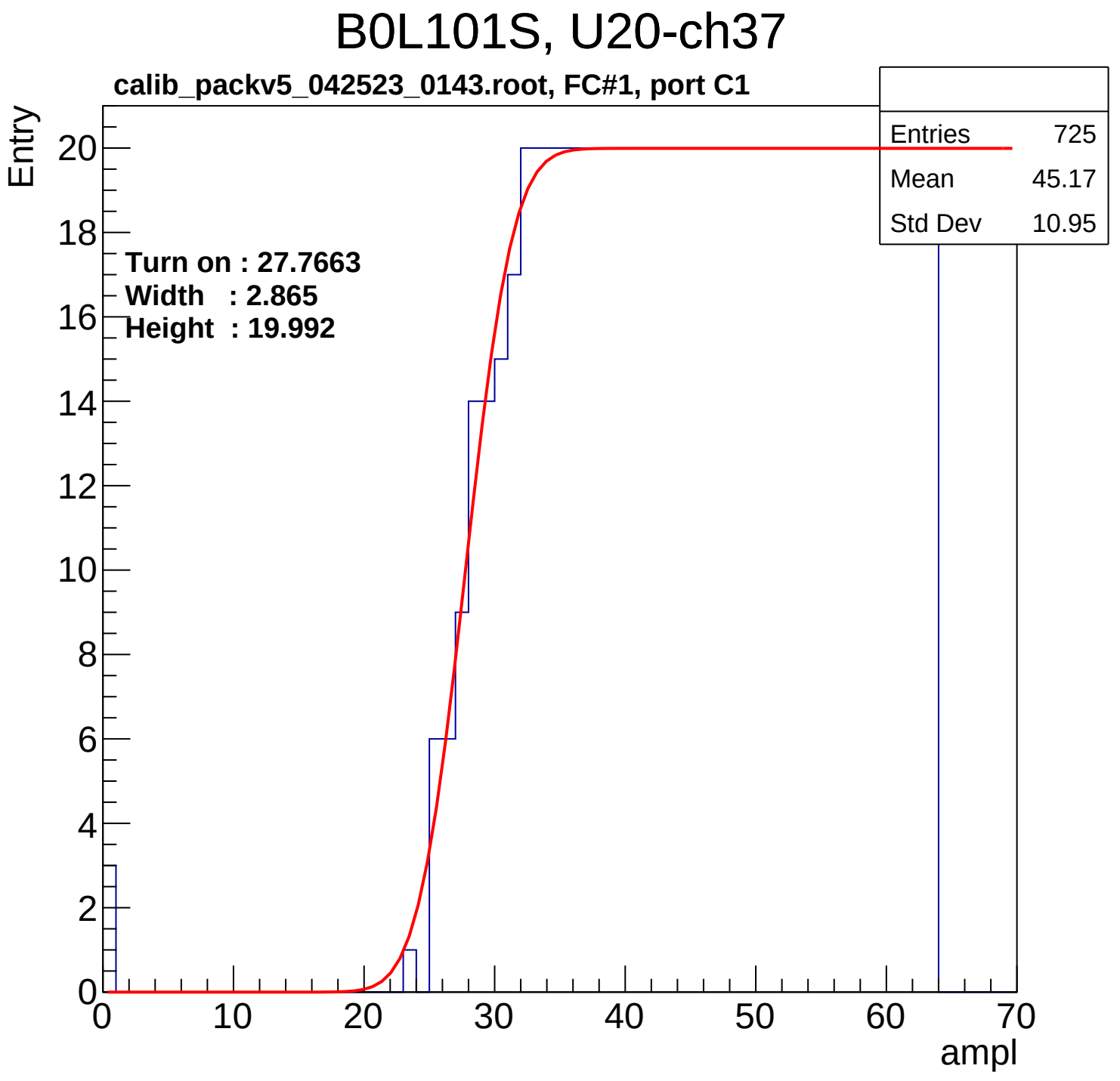
B0L101S, U20-ch37
calib_packv5_042523_0143.root, FC#1, port C1
Entries 725
Mean 45.17
Std Dev 10.95
Turn on : 27.7663
Width : 2.865
Height : 19.992
Entry
ampl
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6
8
10
12
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0
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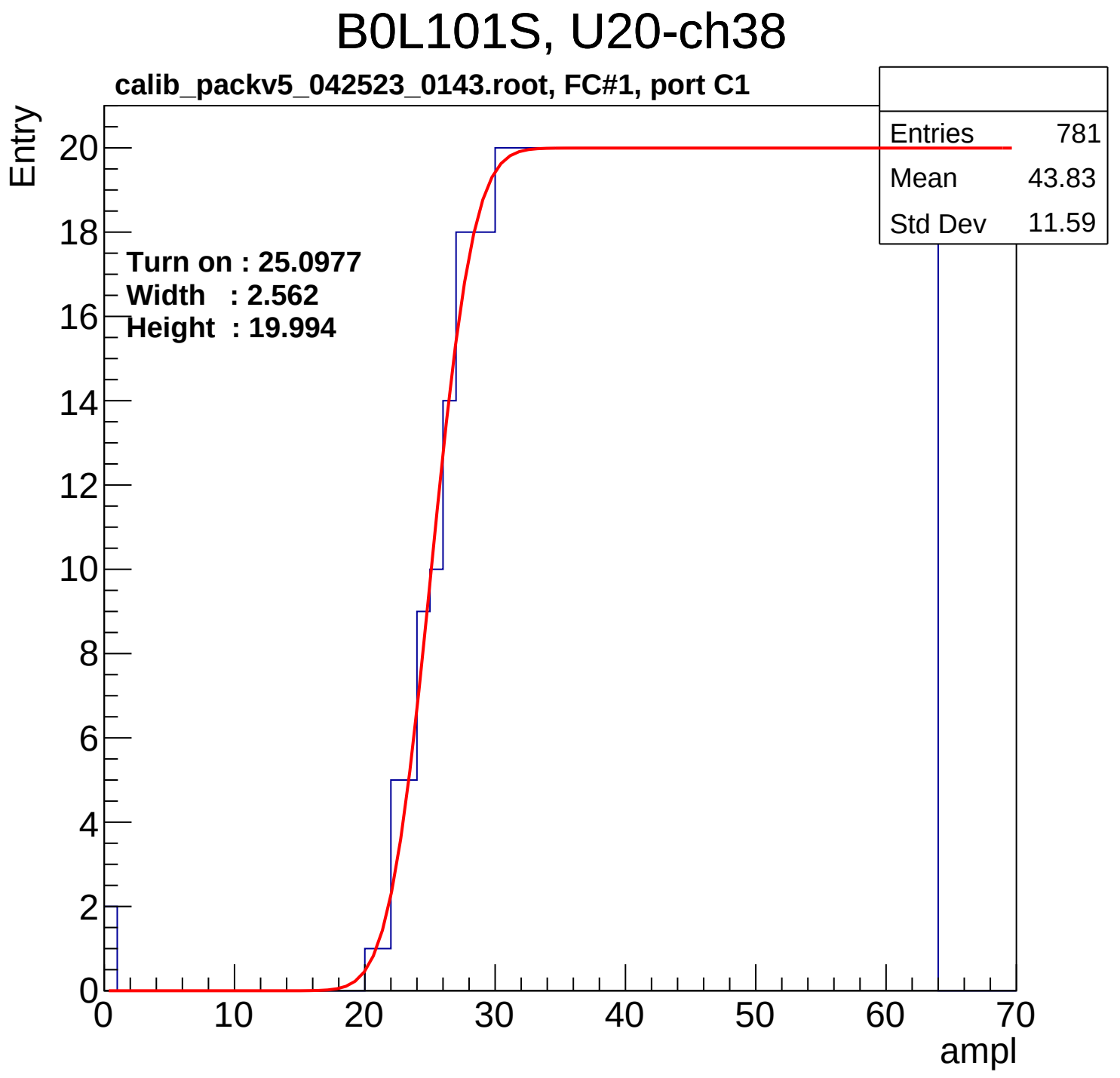
B0L101S, U20-ch38
calib_packv5_042523_0143.root, FC#1, port C1
Entries 781
Mean 43.83
Std Dev 11.59
Turn on : 25.0977
Width : 2.562
Height : 19.994
Entry
ampl
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6
8
10
12
14
16
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0
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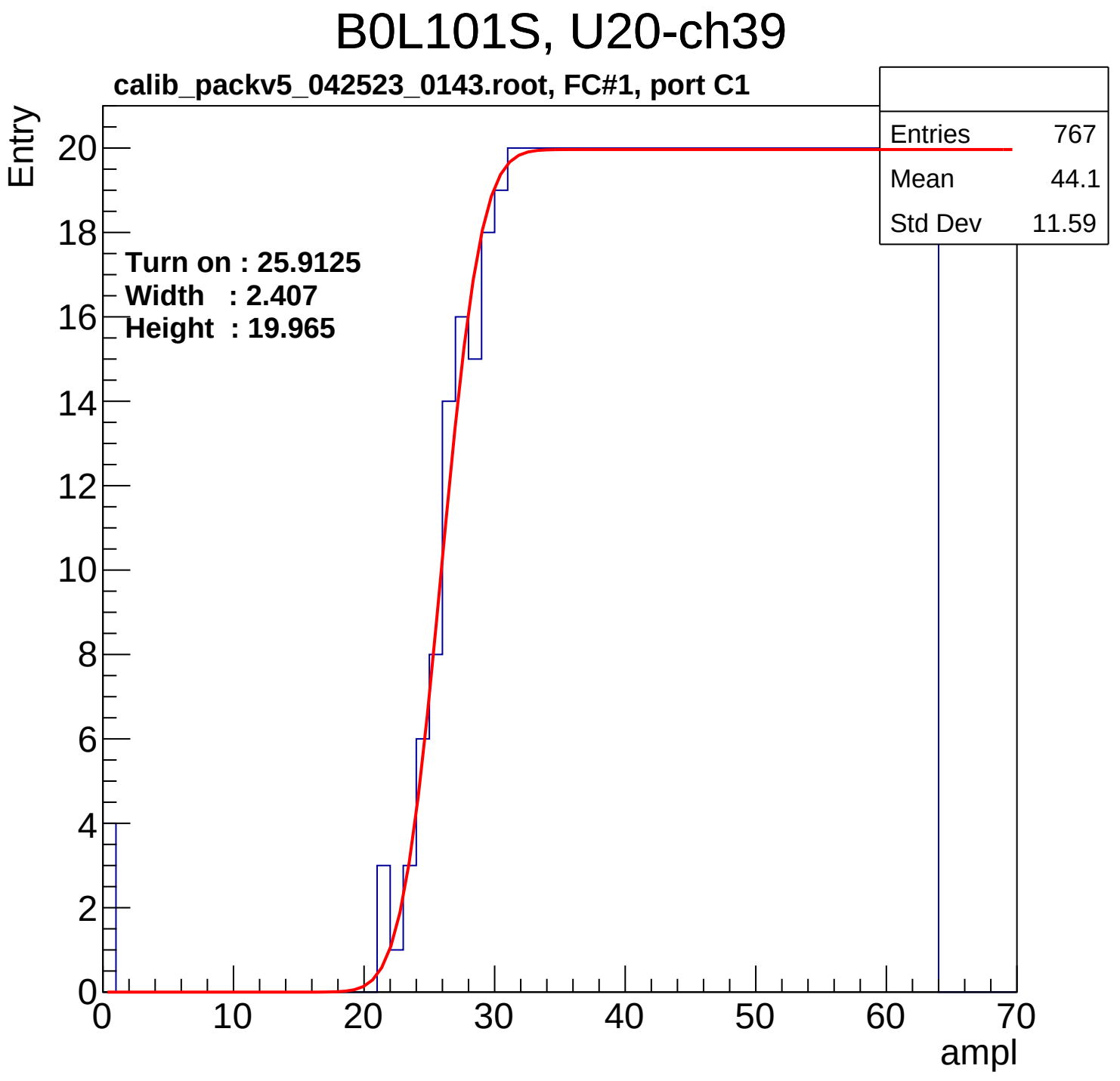
B0L101S, U20-ch39
calib_packv5_042523_0143.root, FC#1, port C1
Entries 767
Mean 44.1
Std Dev 11.59
Turn on : 25.9125
Width : 2.407
Height : 19.965
Entry
ampl
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6
8
10
12
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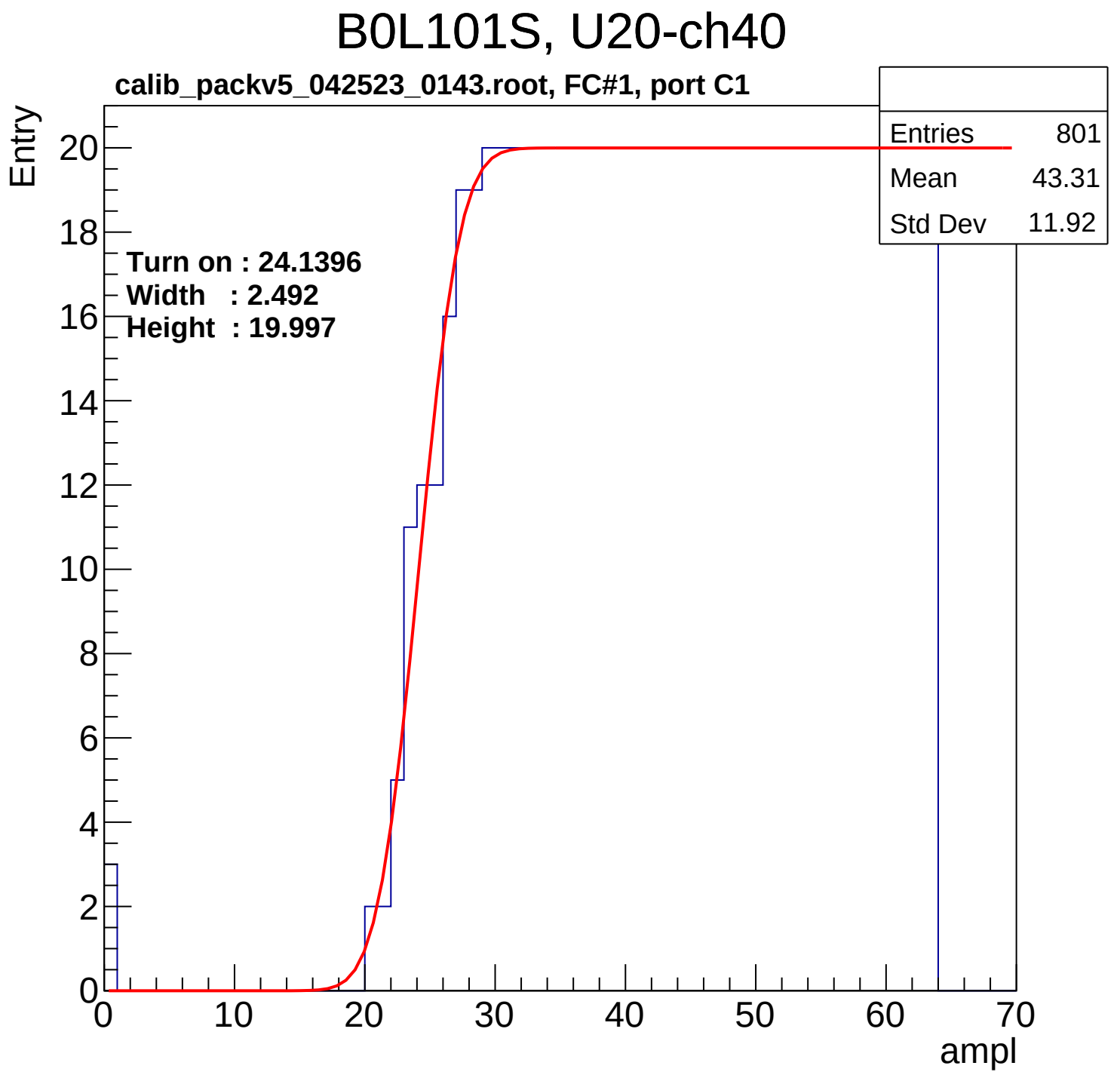
B0L101S, U20-ch40
calib_packv5_042523_0143.root, FC#1, port C1
Entries 801
Mean 43.31
Std Dev 11.92
Turn on : 24.1396
Width : 2.492
Height : 19.997
Entry
ampl
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6
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10
12
14
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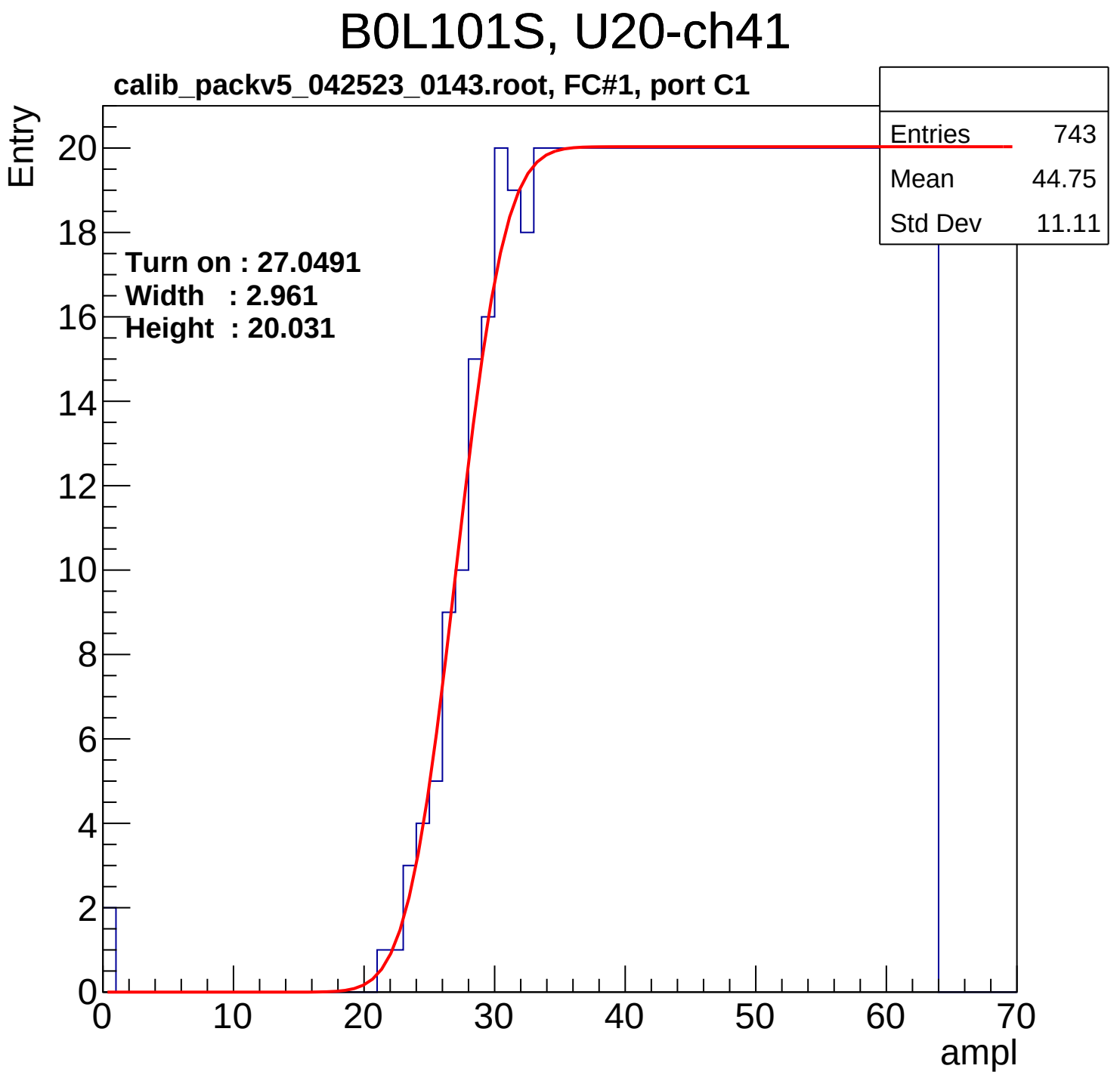
B0L101S, U20-ch41
calib_packv5_042523_0143.root, FC#1, port C1
Entries 743
Mean 44.75
Std Dev 11.11
Turn on : 27.0491
Width : 2.961
Height : 20.031
Entry
ampl
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6
8
10
12
14
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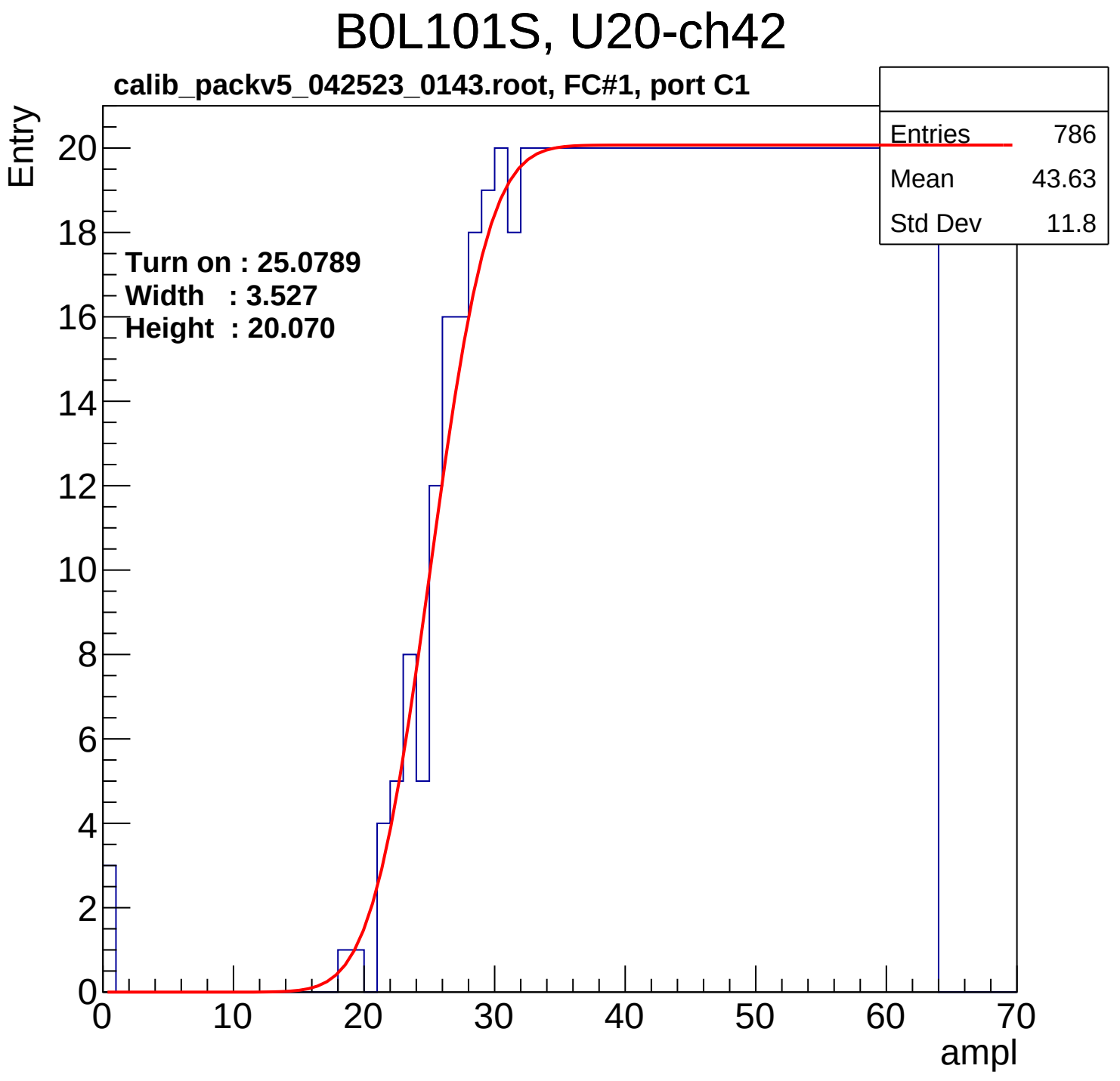
B0L101S, U20-ch42
calib_packv5_042523_0143.root, FC#1, port C1
Entries 786
Mean 43.63
Std Dev 11.8
Turn on : 25.0789
Width : 3.527
Height : 20.070
Entry
ampl
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12
14
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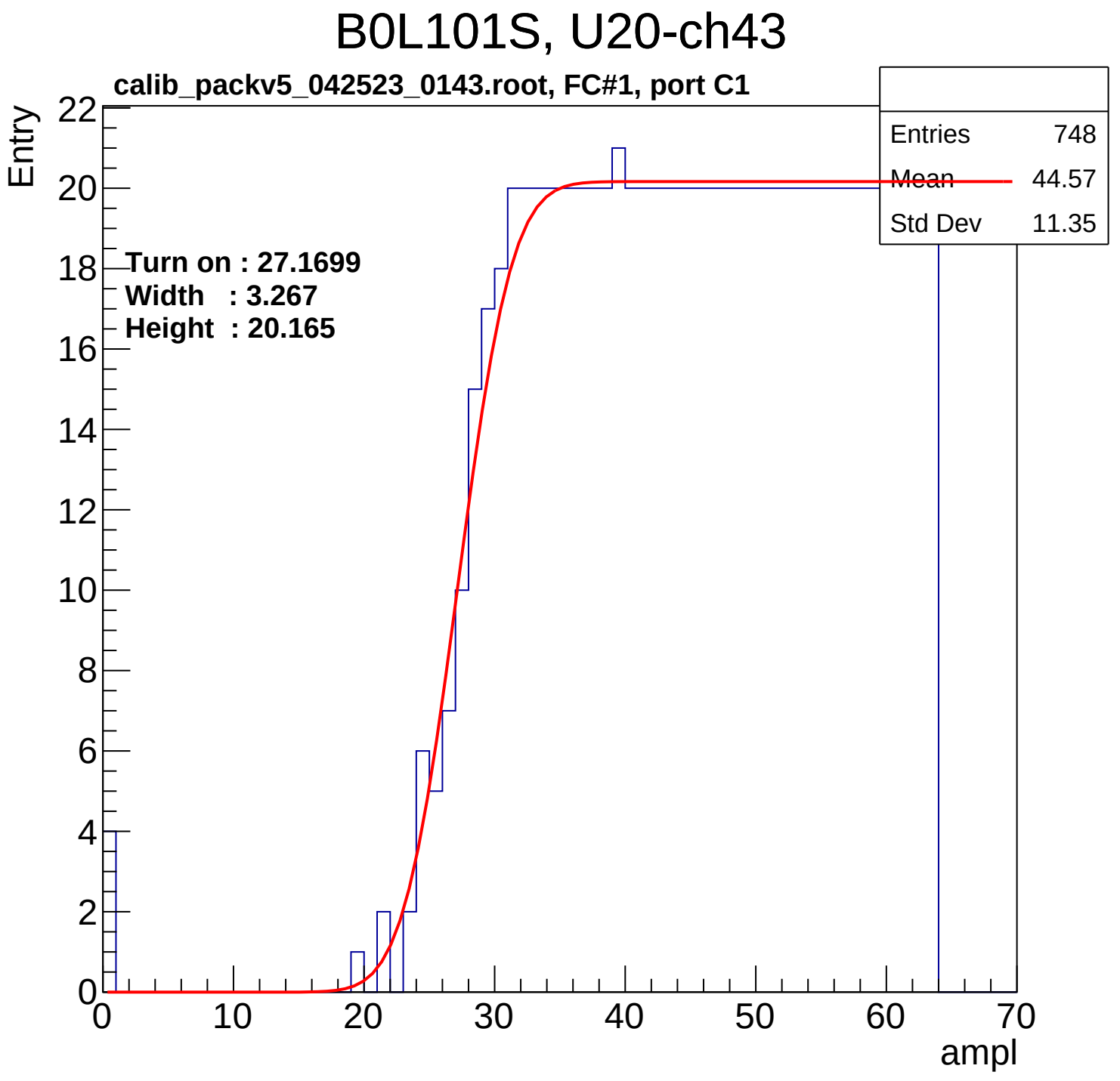
B0L101S, U20-ch43
calib_packv5_042523_0143.root, FC#1, port C1
Entries 748
Mean 44.57
Std Dev 11.35
Turn on : 27.1699
Width : 3.267
Height : 20.165
Entry
ampl
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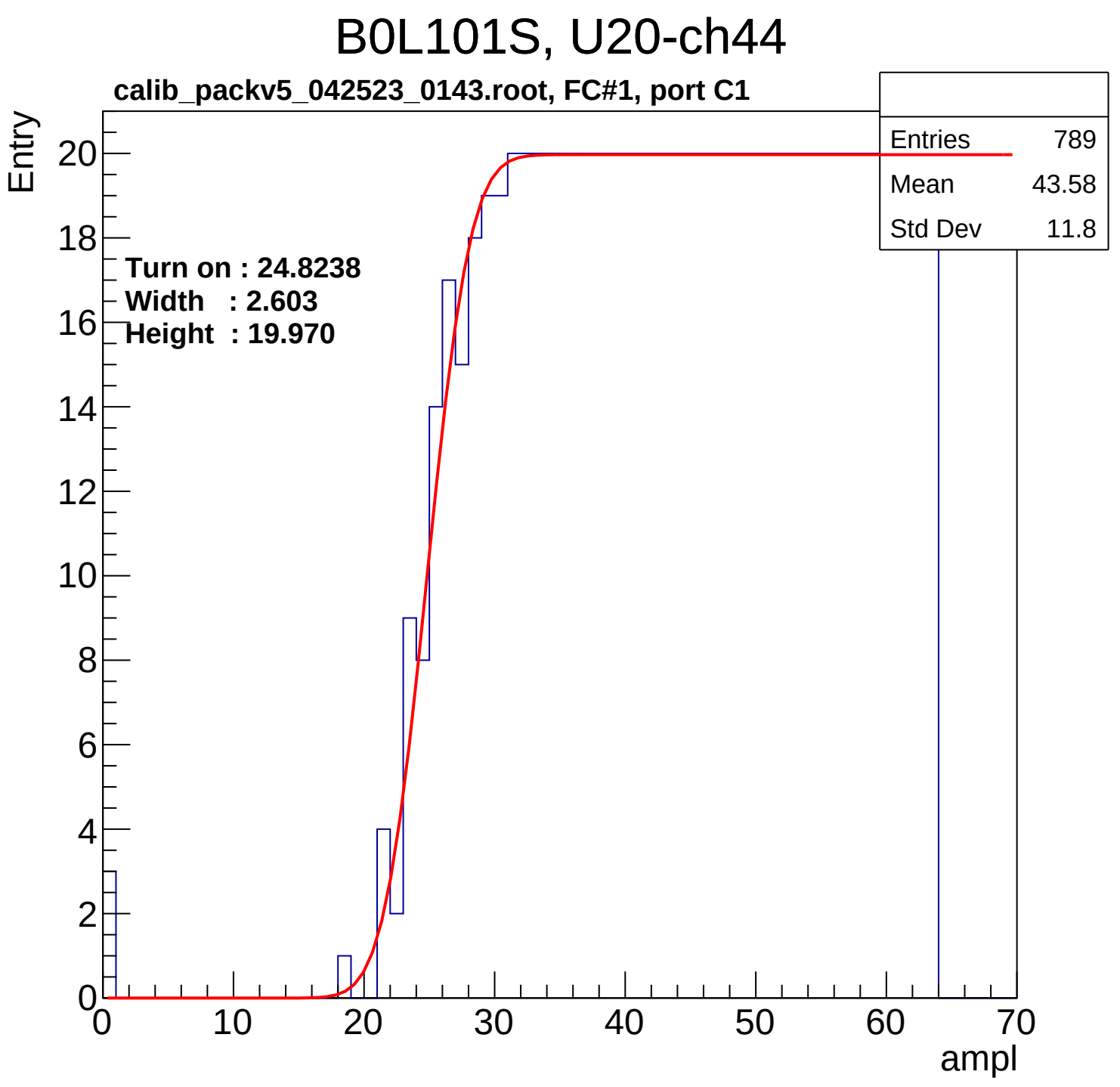
B0L101S, U20-ch44
calib_packv5_042523_0143.root, FC#1, port C1
Entries 789
Mean 43.58
Std Dev 11.8
Turn on : 24.8238
Width : 2.603
Height : 19.970
Entry
ampl
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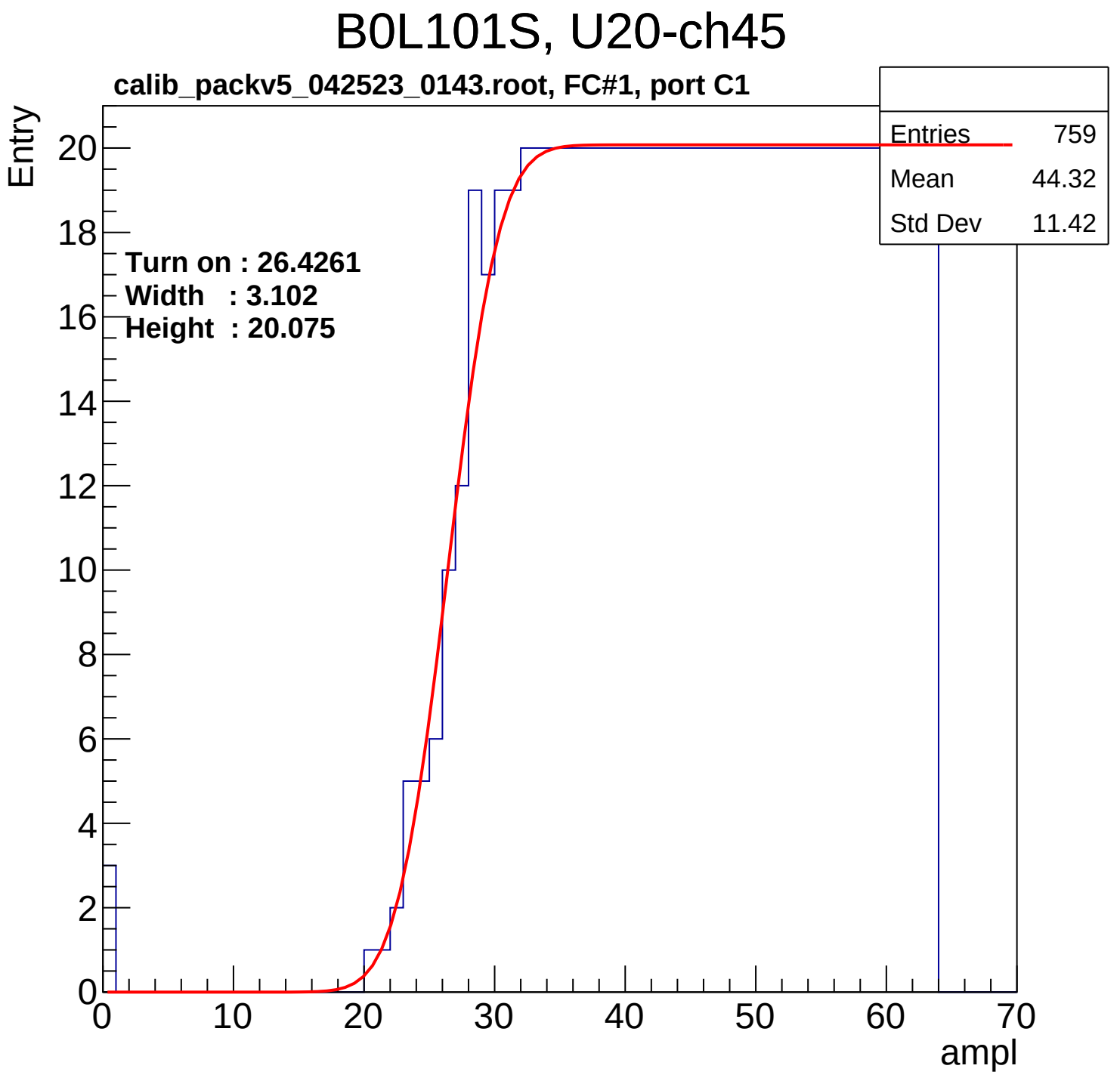
B0L101S, U20-ch45
calib_packv5_042523_0143.root, FC#1, port C1
Entries 759
Mean 44.32
Std Dev 11.42
Turn on : 26.4261
Width : 3.102
Height : 20.075
Entry
ampl
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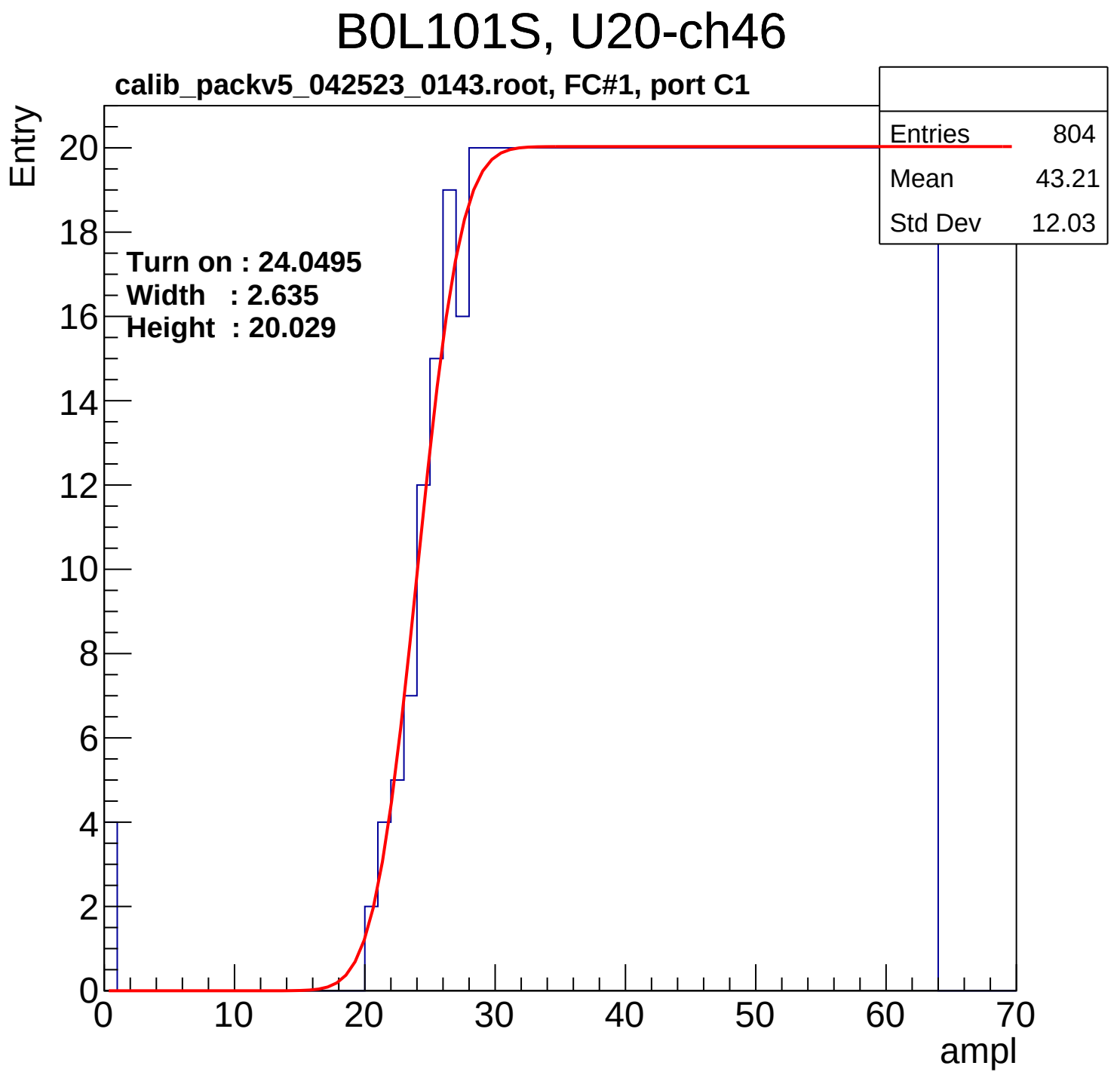
B0L101S, U20-ch46
calib_packv5_042523_0143.root, FC#1, port C1
Entries 804
Mean 43.21
Std Dev 12.03
Turn on : 24.0495
Width : 2.635
Height : 20.029
Entry
ampl
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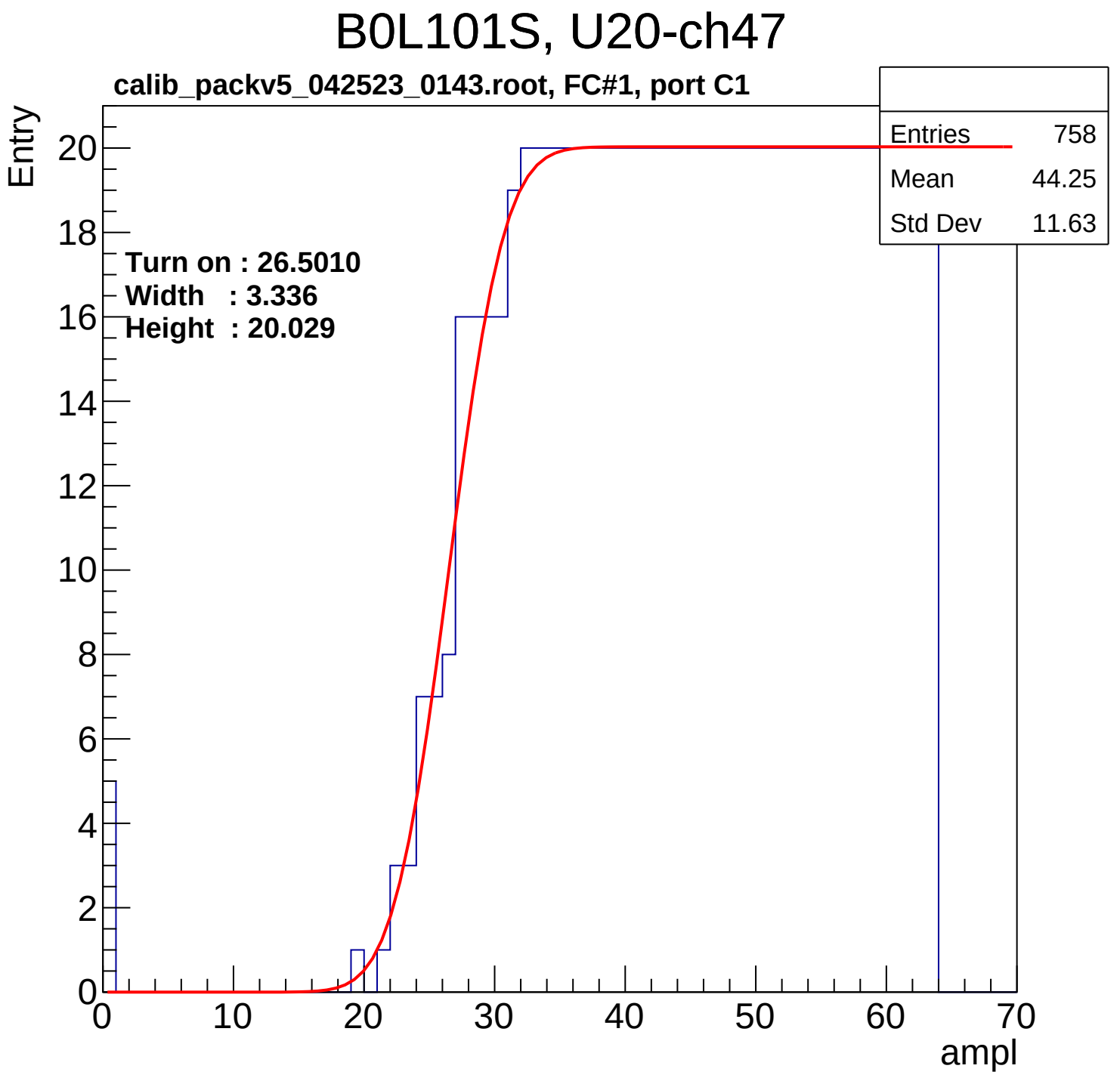
B0L101S, U20-ch47
calib_packv5_042523_0143.root, FC#1, port C1
Entries 758
Mean 44.25
Std Dev 11.63
Turn on : 26.5010
Width : 3.336
Height : 20.029
Entry
ampl
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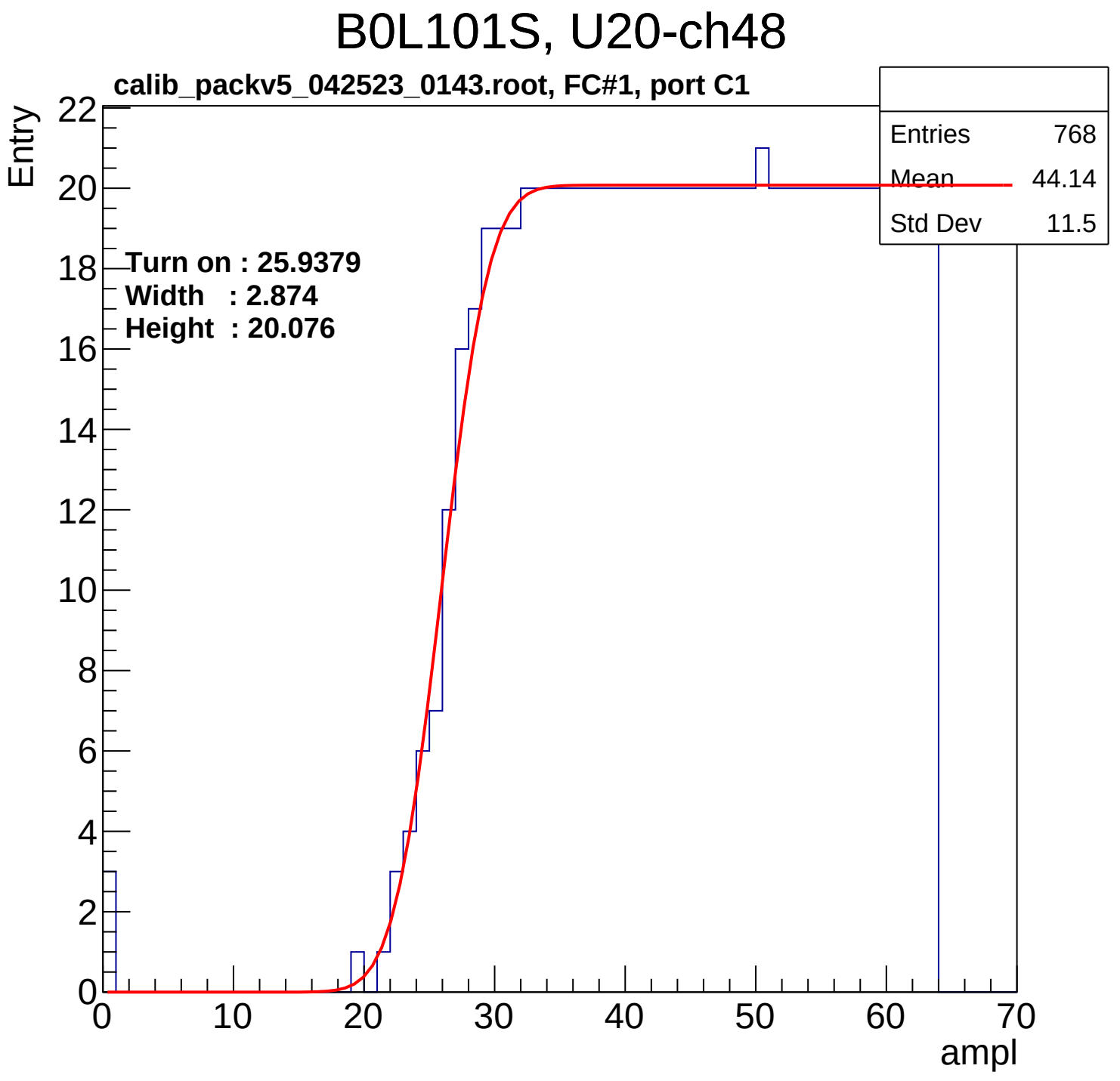
B0L101S, U20-ch48
calib_packv5_042523_0143.root, FC#1, port C1
Entries 768
Mean 44.14
Std Dev 11.5
Turn on : 25.9379
Width : 2.874
Height : 20.076
Entry
ampl
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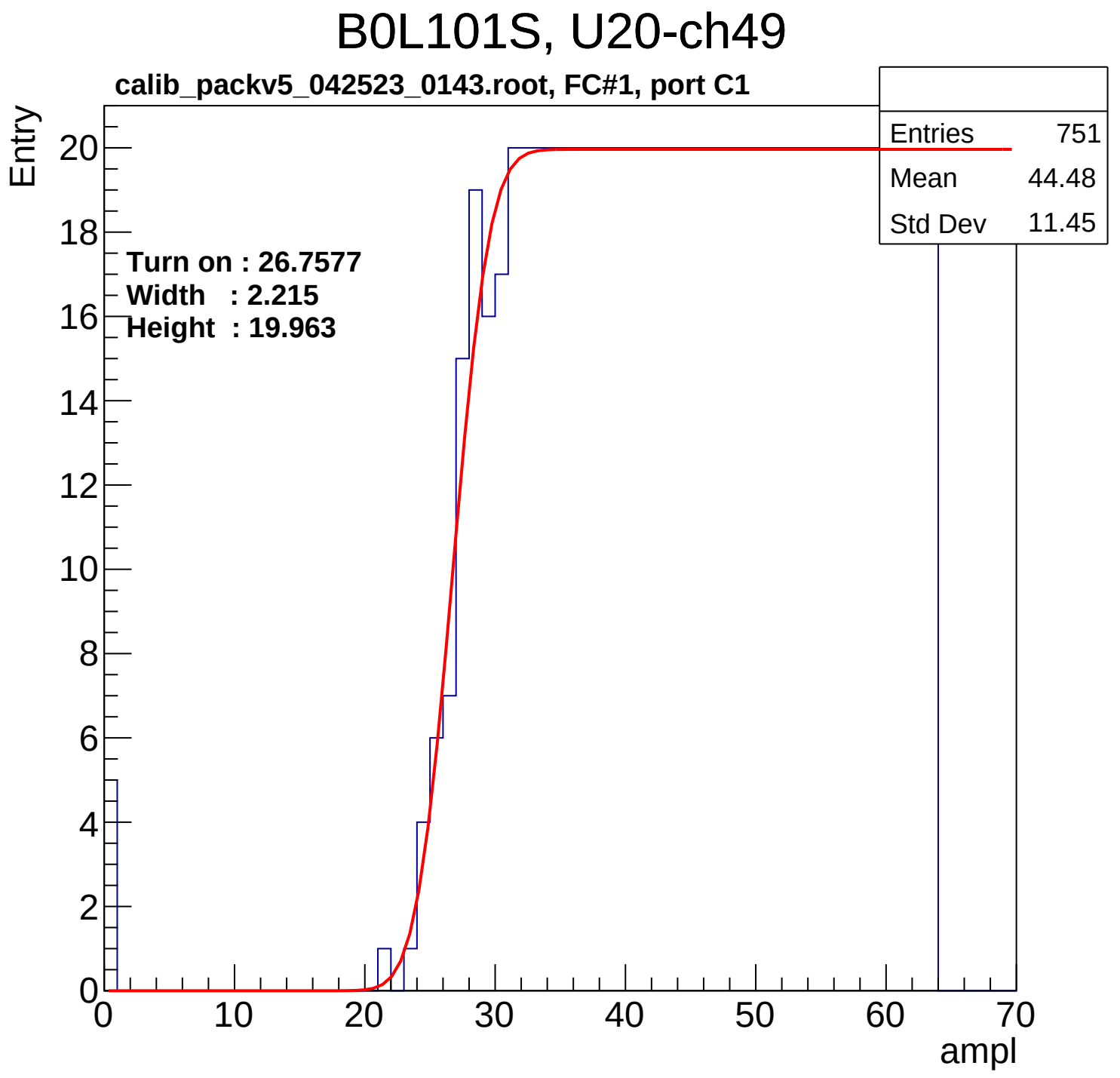
B0L101S, U20-ch49
calib_packv5_042523_0143.root, FC#1, port C1
Entries 751
Mean 44.48
Std Dev 11.45
Turn on : 26.7577
Width : 2.215
Height : 19.963
Entry
ampl
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8
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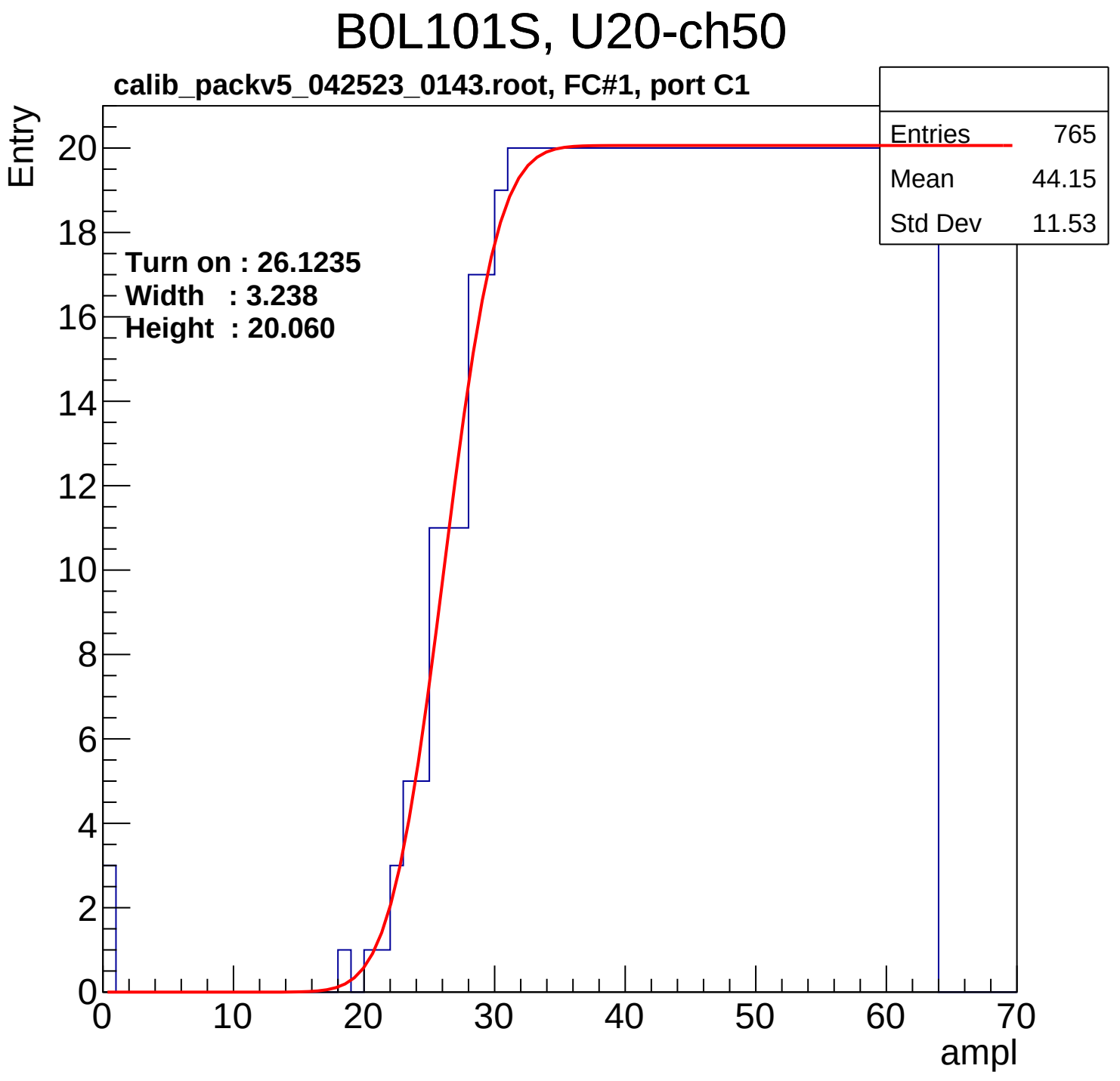
B0L101S, U20-ch50
calib_packv5_042523_0143.root, FC#1, port C1
Entries 765
Mean 44.15
Std Dev 11.53
Turn on : 26.1235
Width : 3.238
Height : 20.060
Entry
ampl
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8
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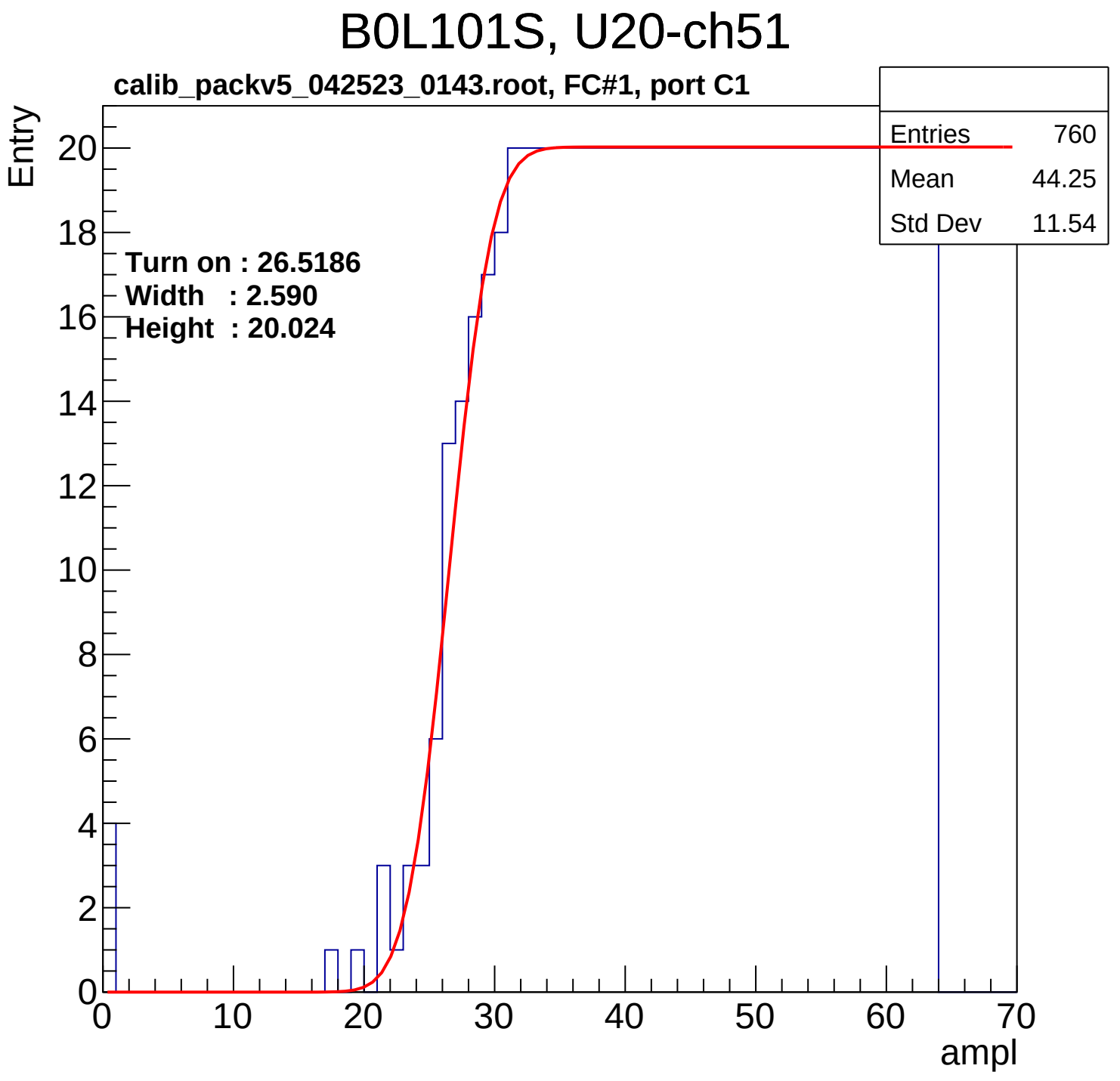
B0L101S, U20-ch51
calib_packv5_042523_0143.root, FC#1, port C1
Entries 760
Mean 44.25
Std Dev 11.54
Turn on : 26.5186
Width : 2.590
Height : 20.024
Entry
ampl
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8
10
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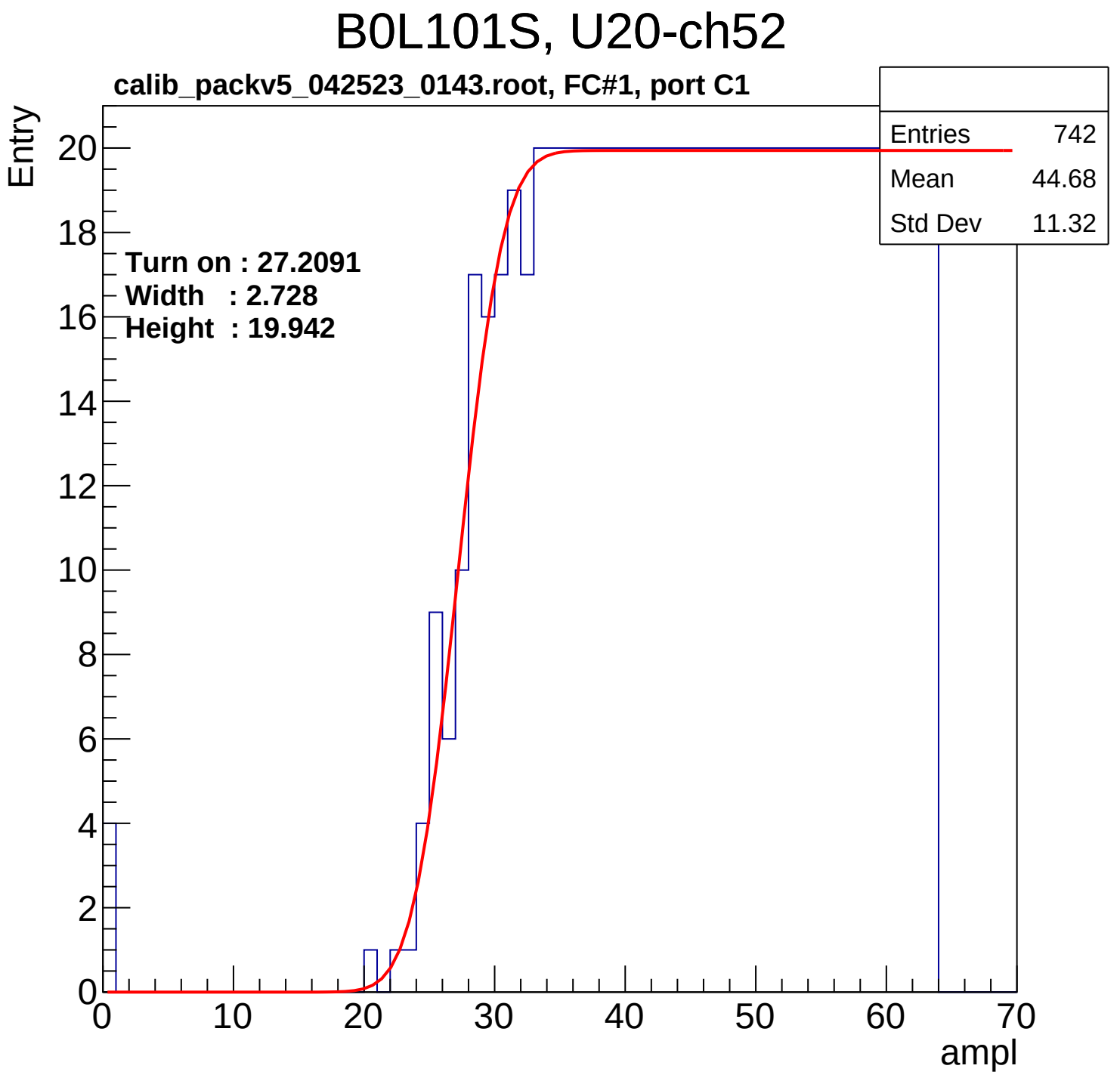
B0L101S, U20-ch52
calib_packv5_042523_0143.root, FC#1, port C1
Entries 742
Mean 44.68
Std Dev 11.32
Turn on : 27.2091
Width : 2.728
Height : 19.942
Entry
ampl
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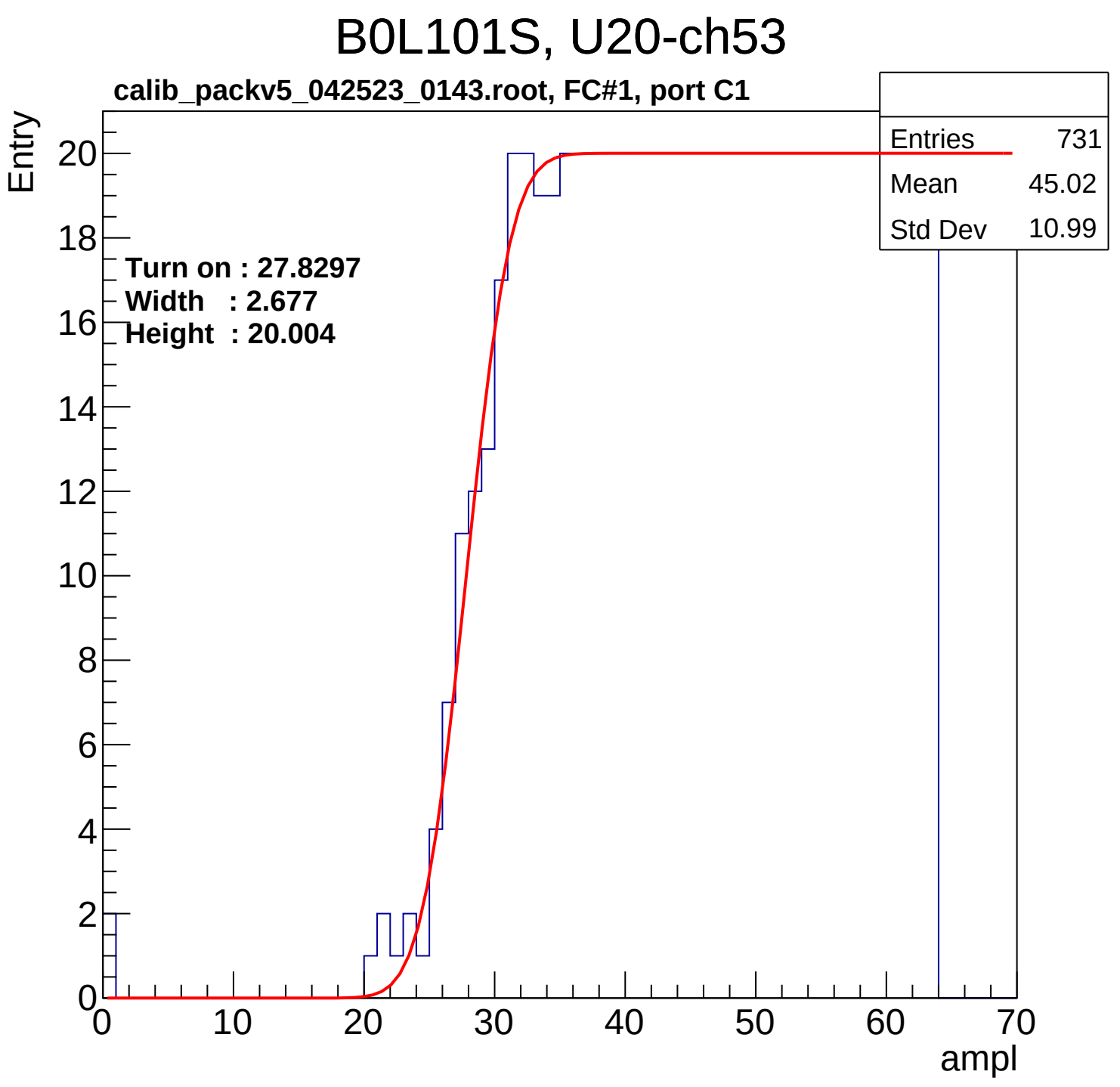
B0L101S, U20-ch53
calib_packv5_042523_0143.root, FC#1, port C1
Entries 731
Mean 45.02
Std Dev 10.99
Turn on : 27.8297
Width : 2.677
Height : 20.004
Entry
ampl
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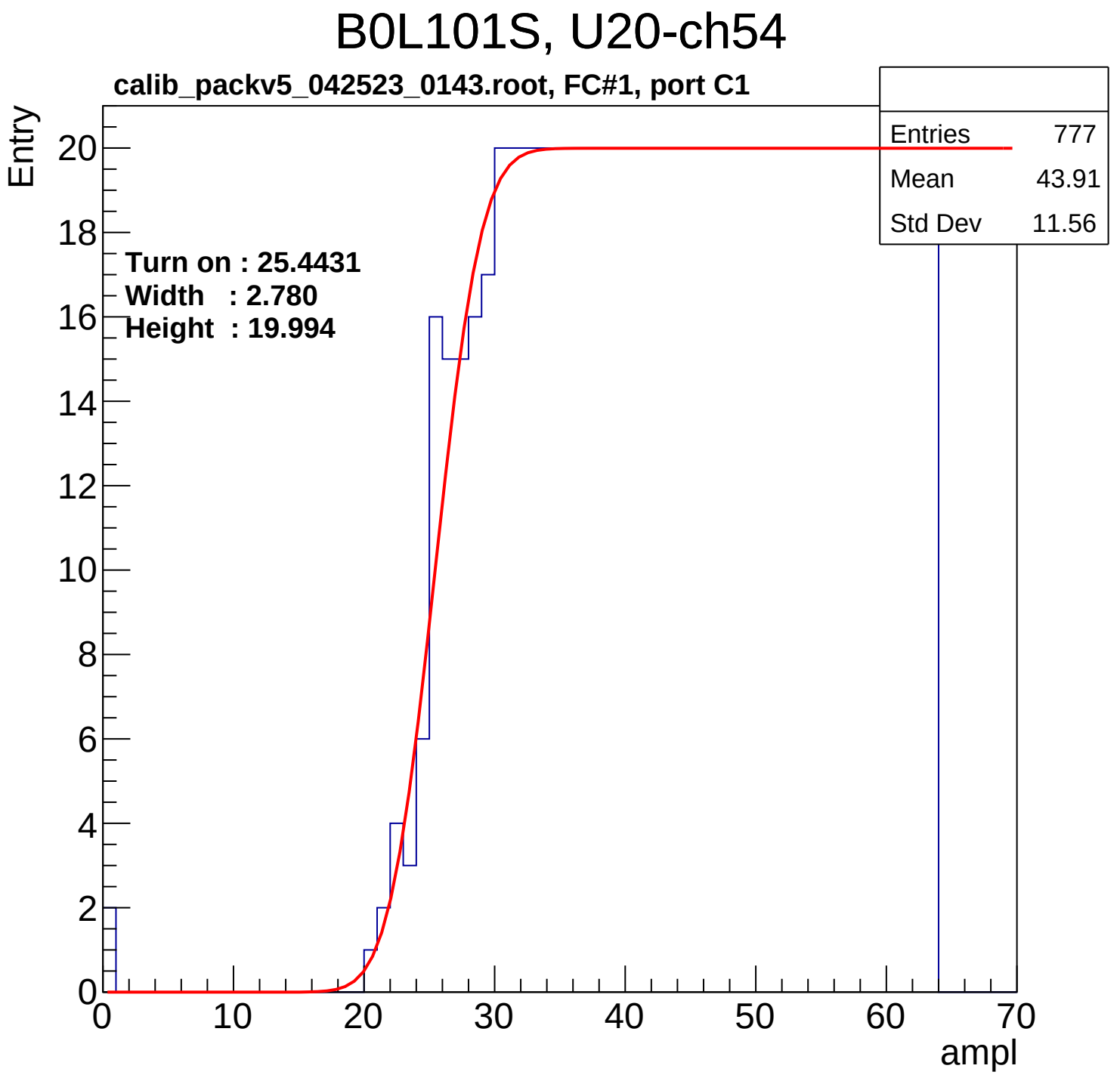
B0L101S, U20-ch54
calib_packv5_042523_0143.root, FC#1, port C1
Entries 777
Mean 43.91
Std Dev 11.56
Turn on : 25.4431
Width : 2.780
Height : 19.994
Entry
ampl
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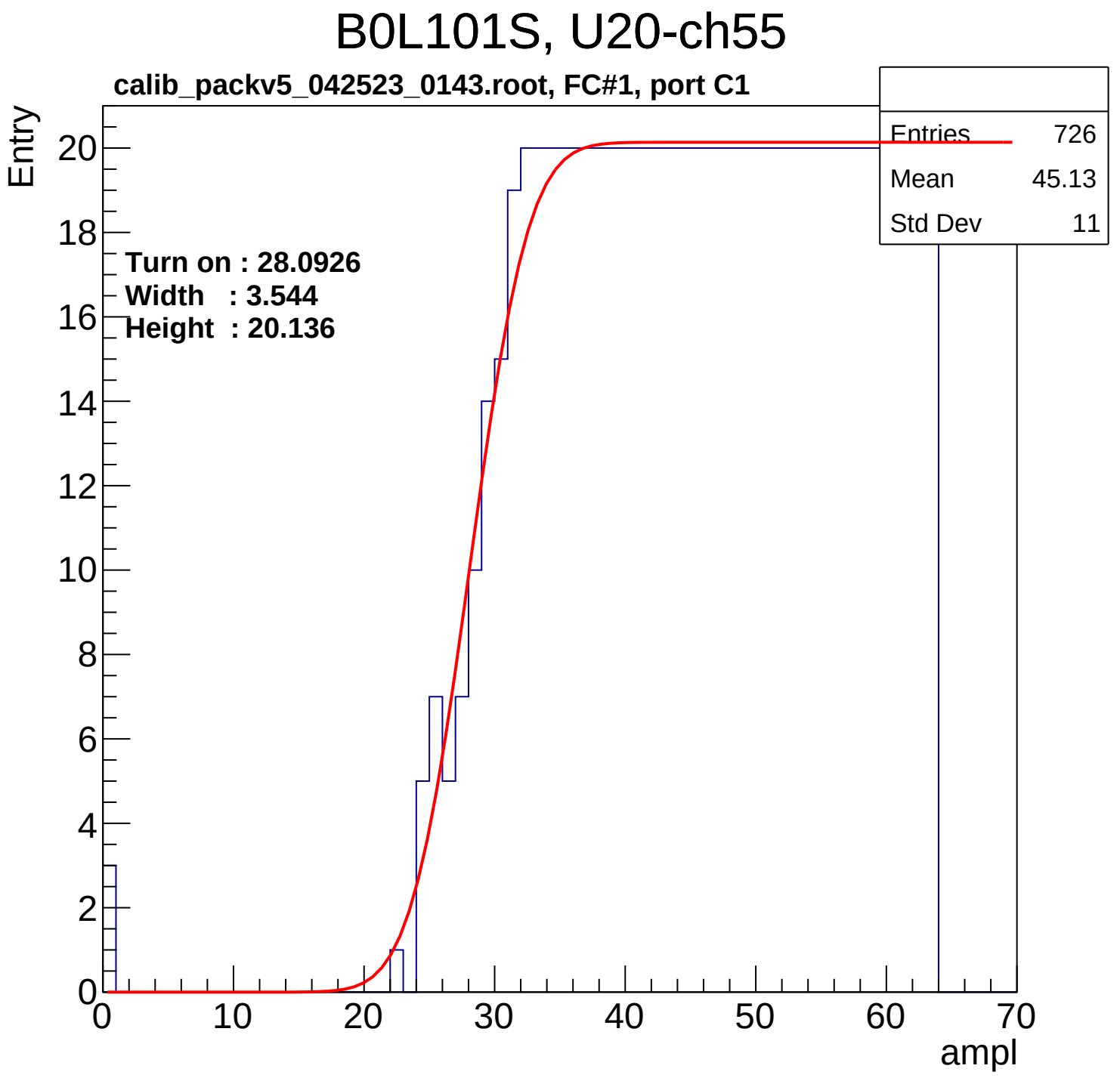
B0L101S, U20-ch55
calib_packv5_042523_0143.root, FC#1, port C1
Entries 726
Mean 45.13
Std Dev 11
Turn on : 28.0926
Width : 3.544
Height : 20.136
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
0
10
20
30
40
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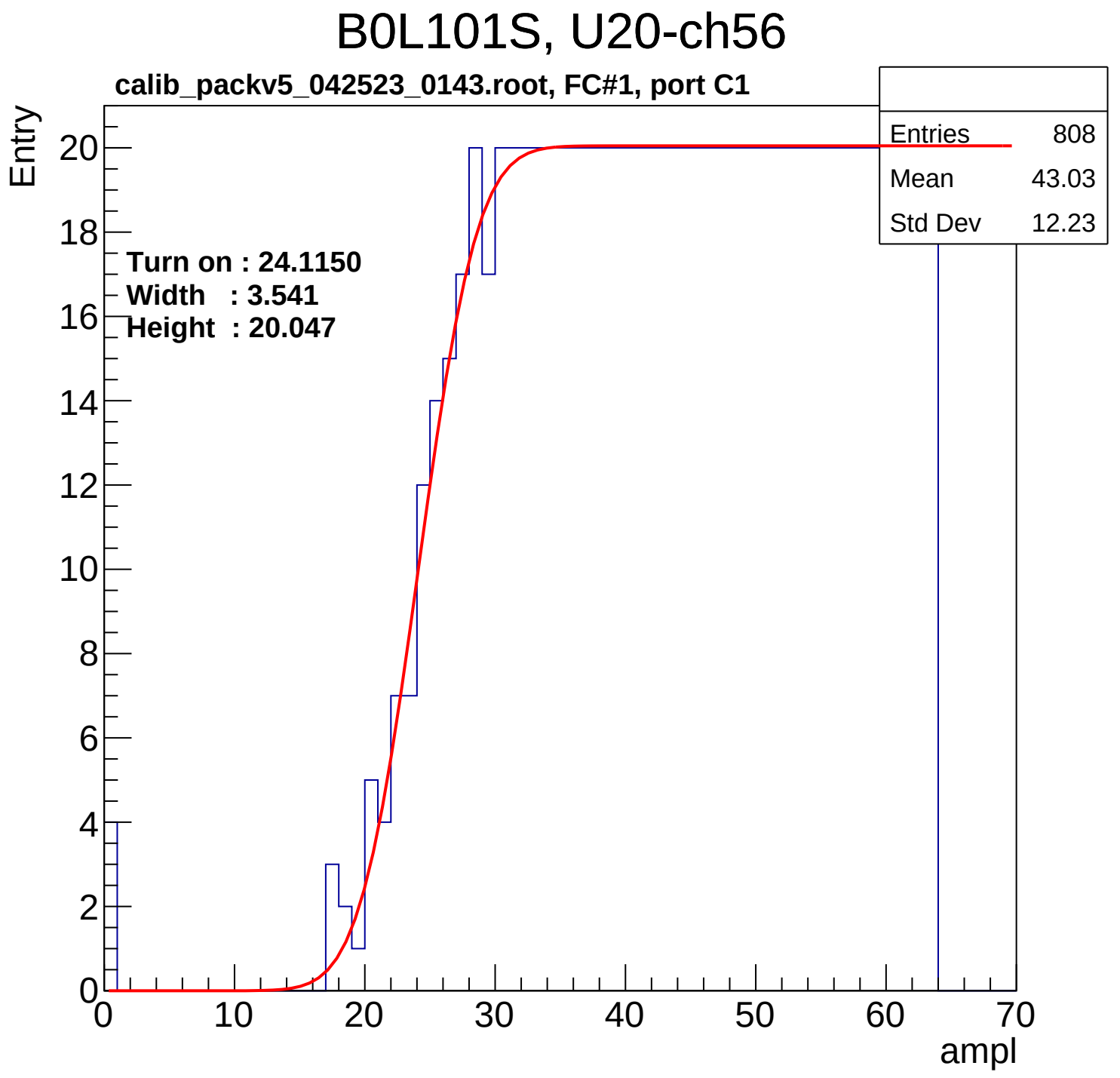
B0L101S, U20-ch56
calib_packv5_042523_0143.root, FC#1, port C1
Entries 808
Mean 43.03
Std Dev 12.23
Turn on : 24.1150
Width : 3.541
Height : 20.047
Entry
ampl
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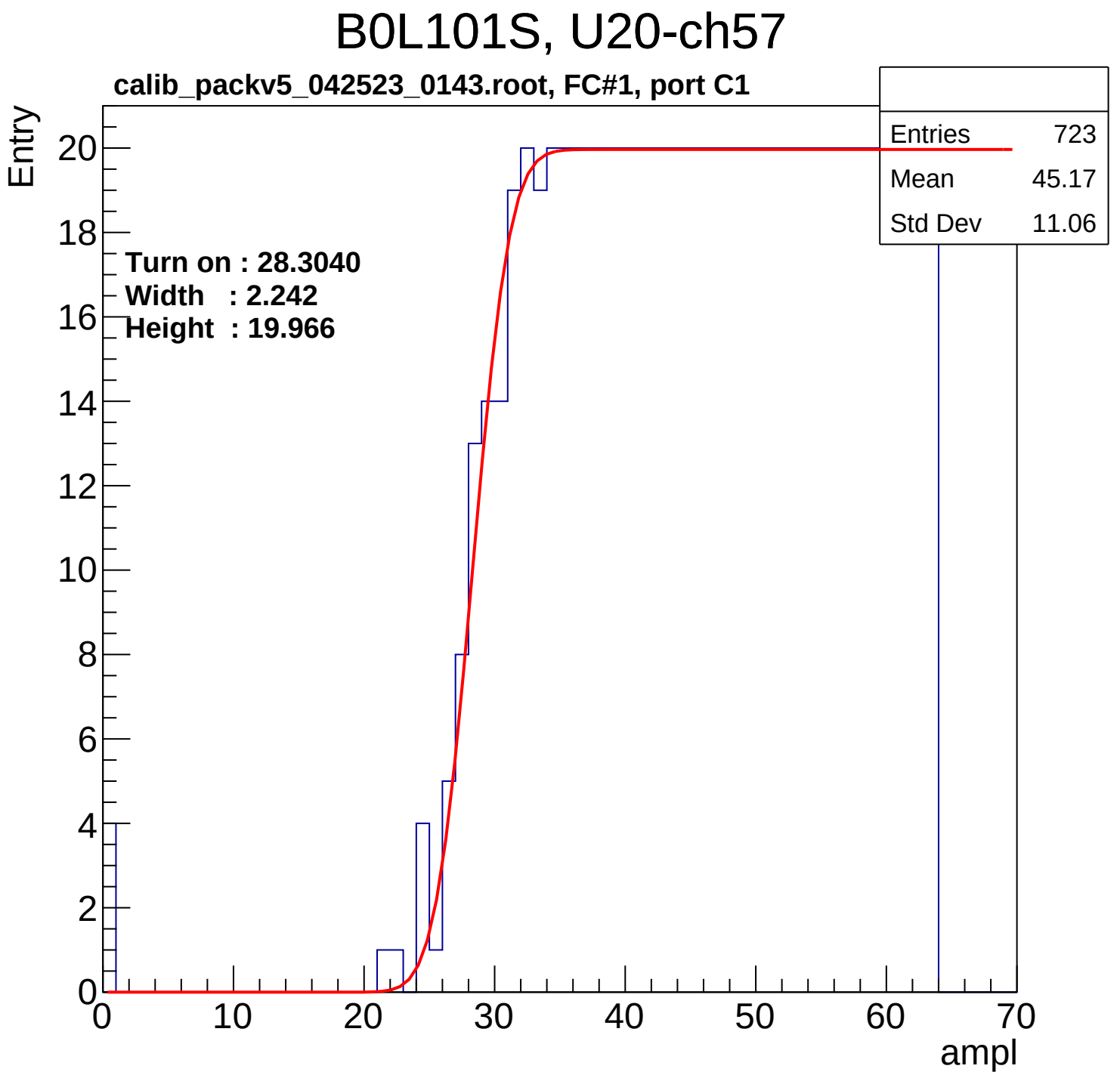
B0L101S, U20-ch57
calib_packv5_042523_0143.root, FC#1, port C1
Entries 723
Mean 45.17
Std Dev 11.06
Turn on : 28.3040
Width : 2.242
Height : 19.966
Entry
ampl
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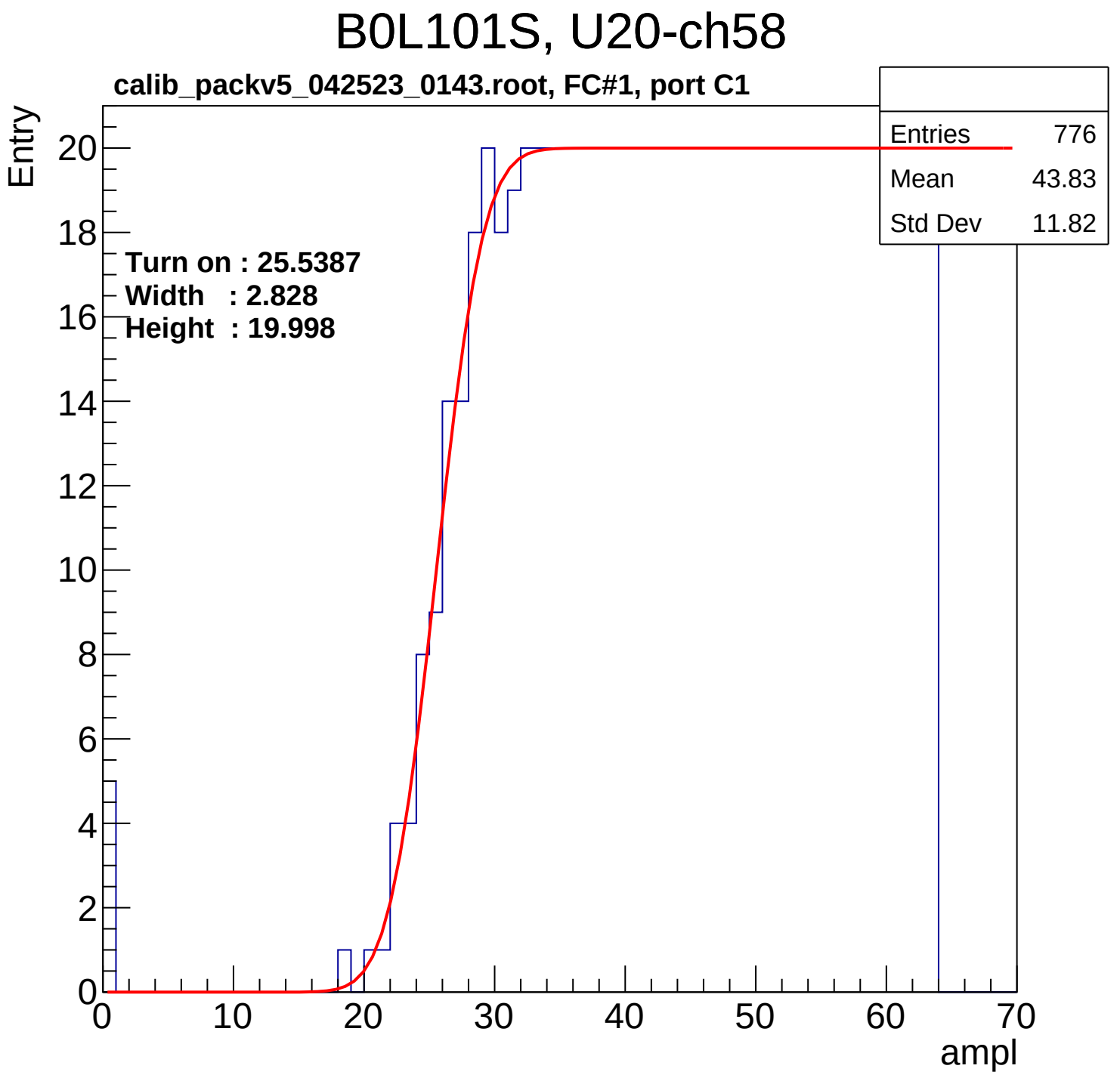
B0L101S, U20-ch58
calib_packv5_042523_0143.root, FC#1, port C1
Entries 776
Mean 43.83
Std Dev 11.82
Turn on : 25.5387
Width : 2.828
Height : 19.998
Entry
ampl
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6
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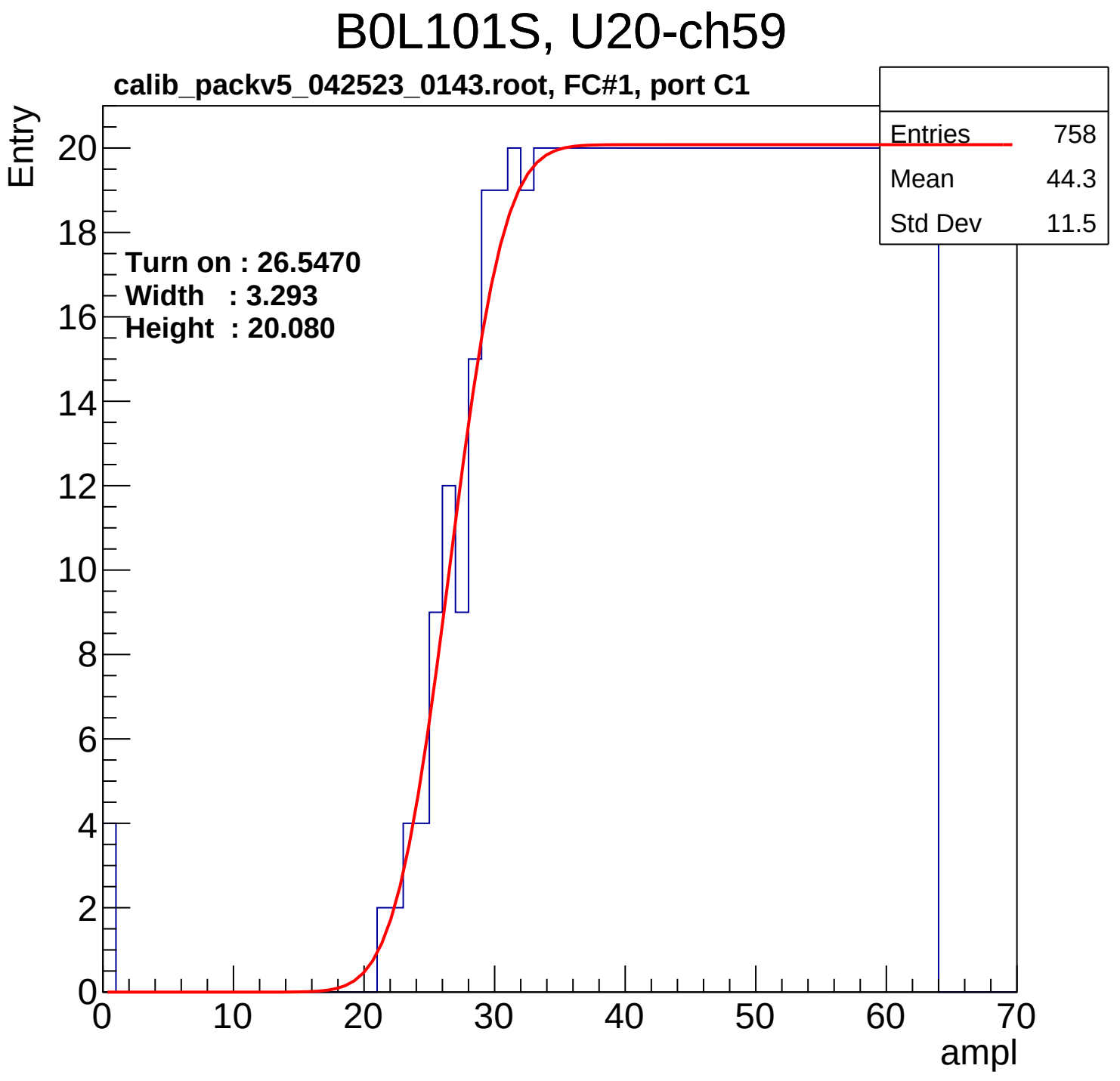
B0L101S, U20-ch59
calib_packv5_042523_0143.root, FC#1, port C1
Entries 758
Mean 44.3
Std Dev 11.5
Turn on : 26.5470
Width : 3.293
Height : 20.080
Entry
ampl
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2
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6
8
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12
14
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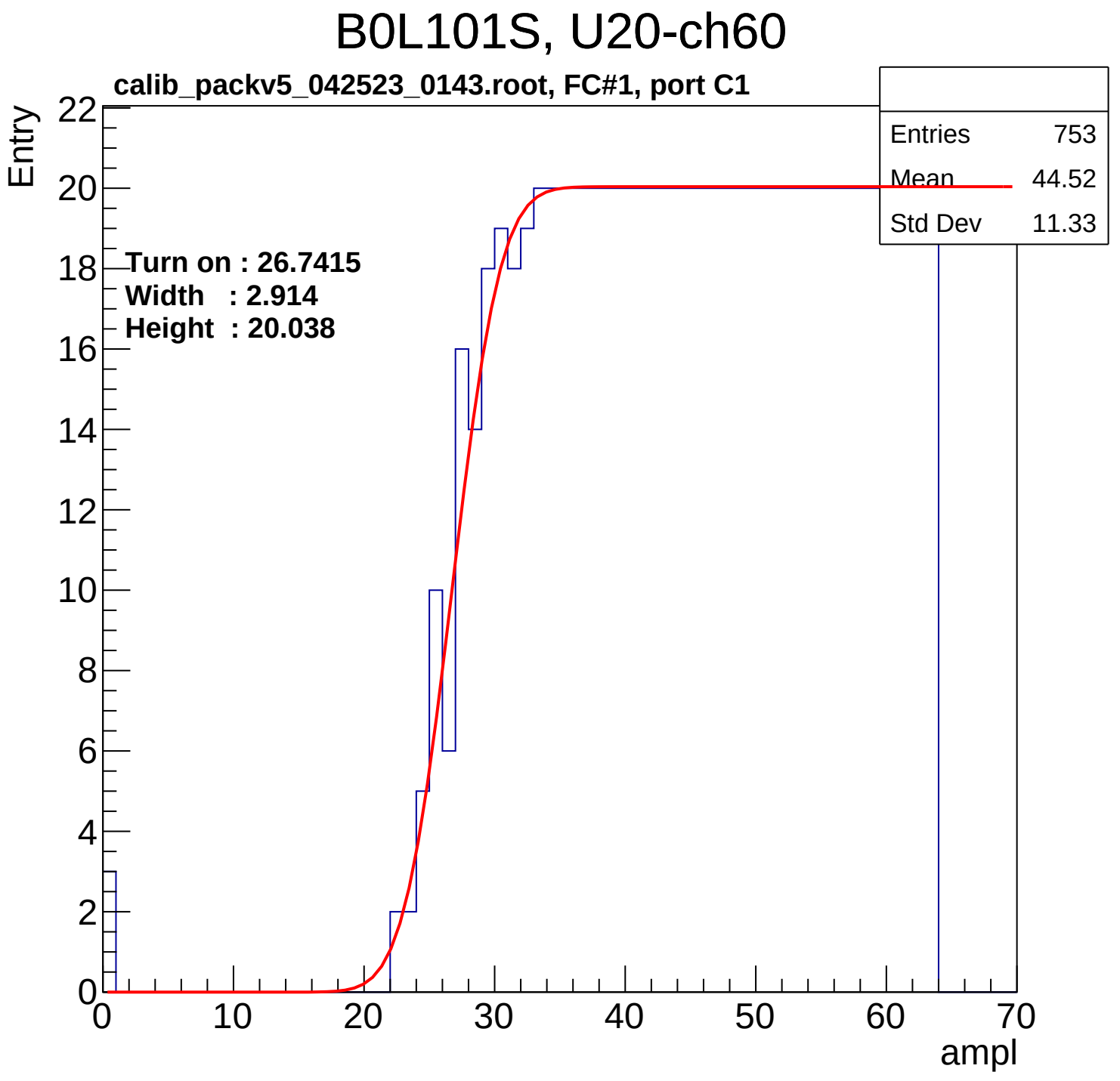
B0L101S, U20-ch60
calib_packv5_042523_0143.root, FC#1, port C1
Entries 753
Mean 44.52
Std Dev 11.33
Turn on : 26.7415
Width : 2.914
Height : 20.038
Entry
ampl
0
2
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6
8
10
12
14
16
18
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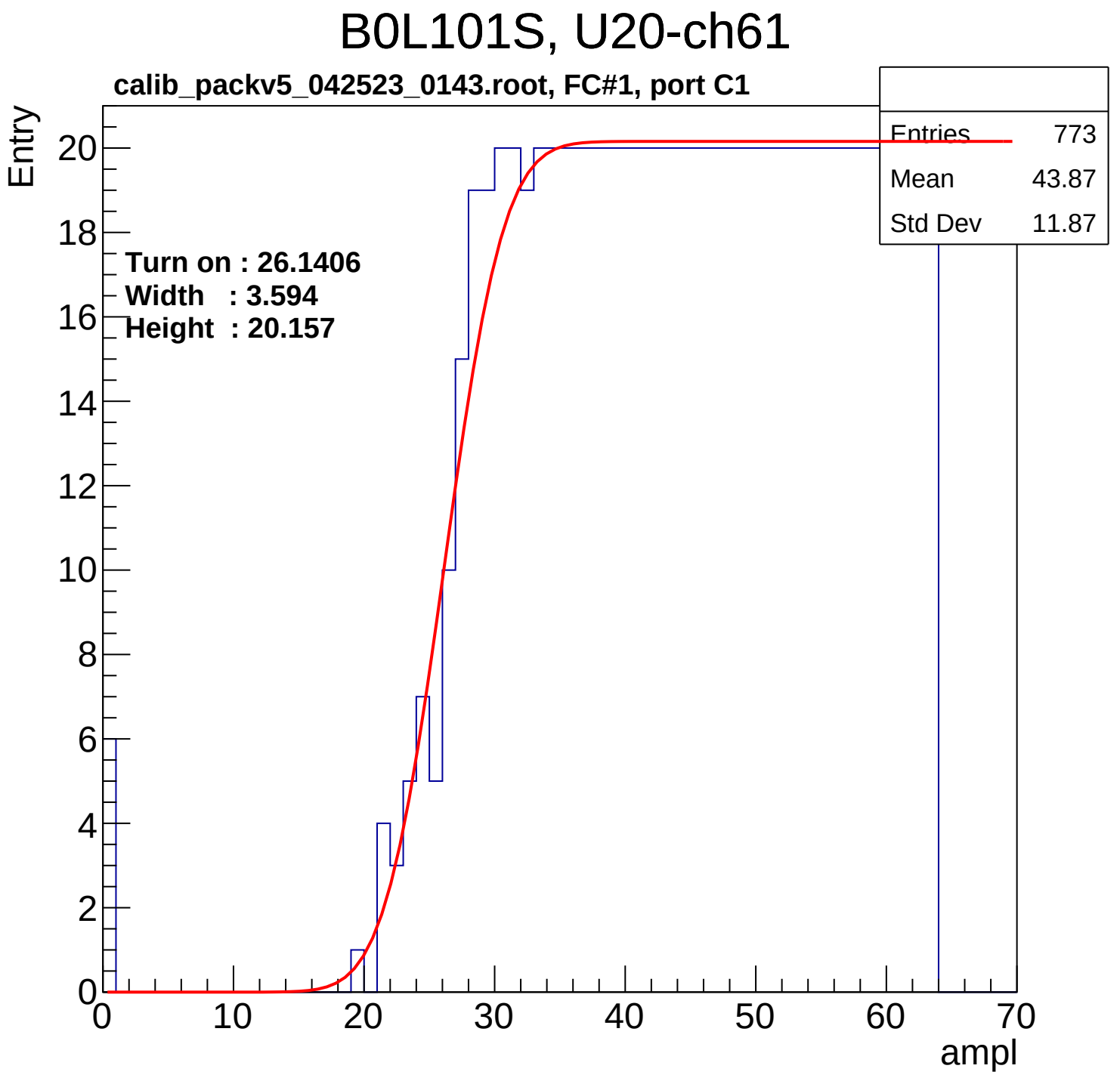
B0L101S, U20-ch61
calib_packv5_042523_0143.root, FC#1, port C1
Entries 773
Mean 43.87
Std Dev 11.87
Turn on : 26.1406
Width : 3.594
Height : 20.157
Entry
ampl
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6
8
10
12
14
16
18
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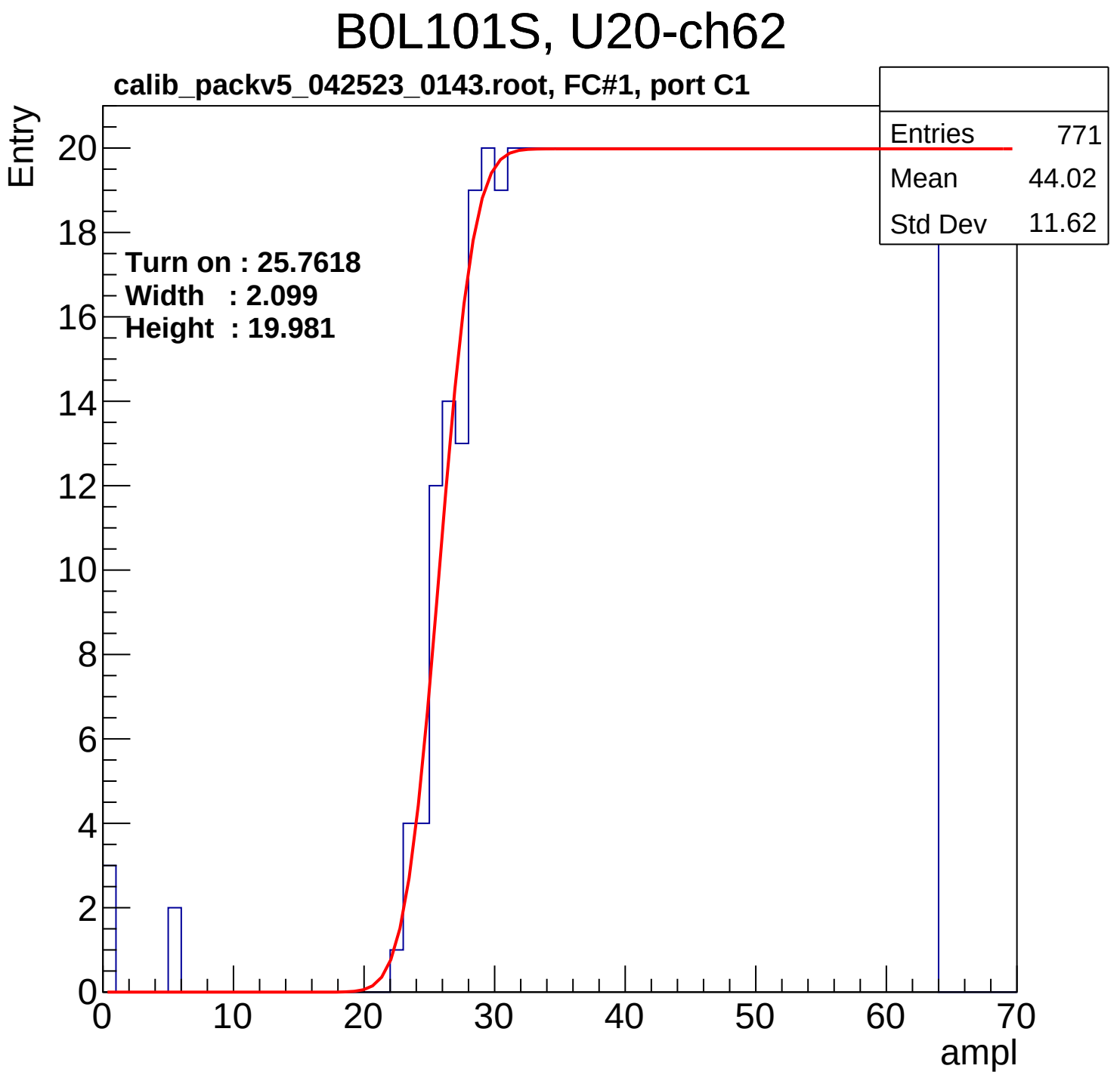
B0L101S, U20-ch62
calib_packv5_042523_0143.root, FC#1, port C1
Entries 771
Mean 44.02
Std Dev 11.62
Turn on : 25.7618
Width : 2.099
Height : 19.981
Entry
ampl
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6
8
10
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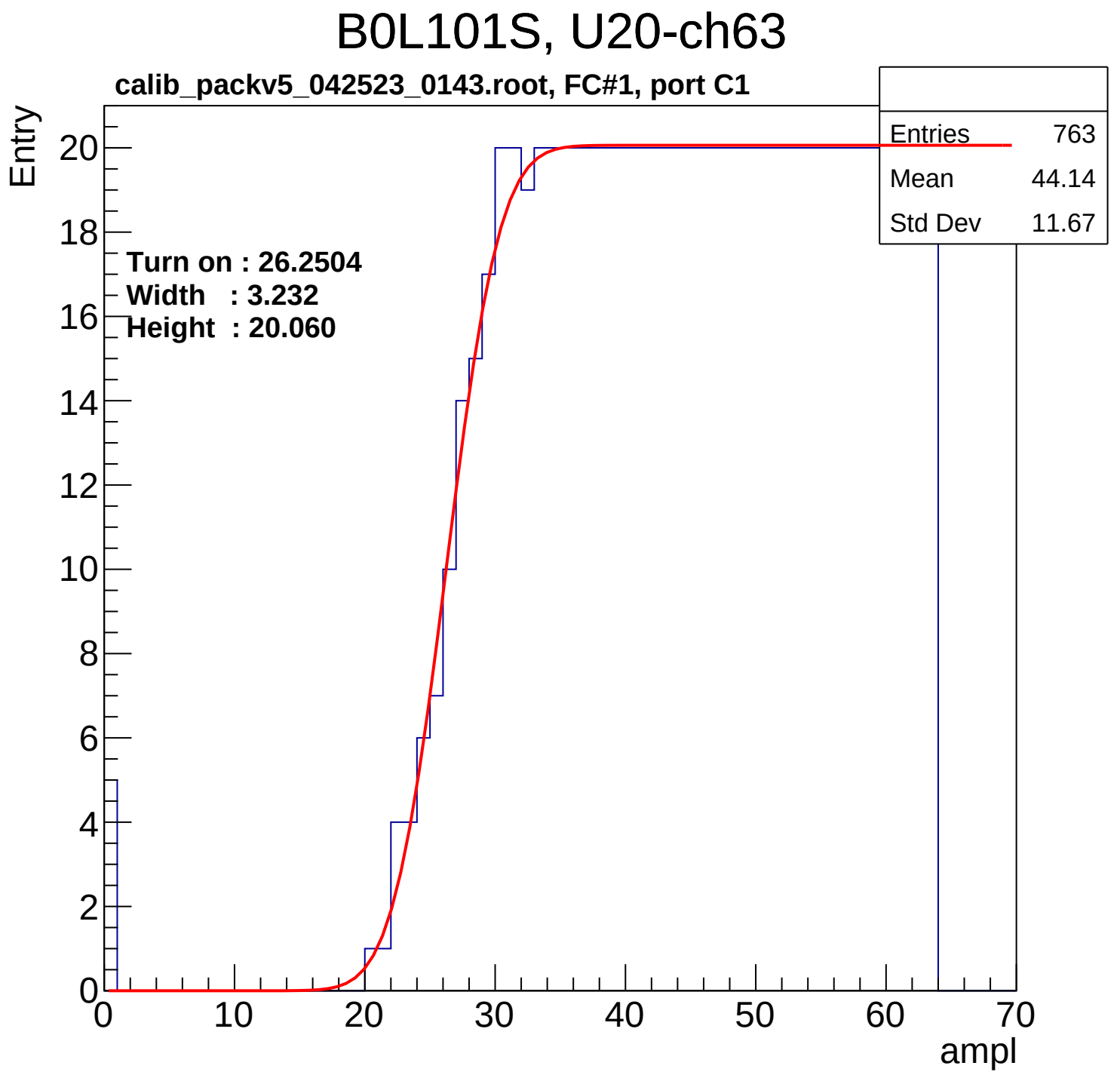
B0L101S, U20-ch63
calib_packv5_042523_0143.root, FC#1, port C1
Entries 763
Mean 44.14
Std Dev 11.67
Turn on : 26.2504
Width : 3.232
Height : 20.060
Entry
ampl
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6
8
10
12
14
16
18
20
0
10
20
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40
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60
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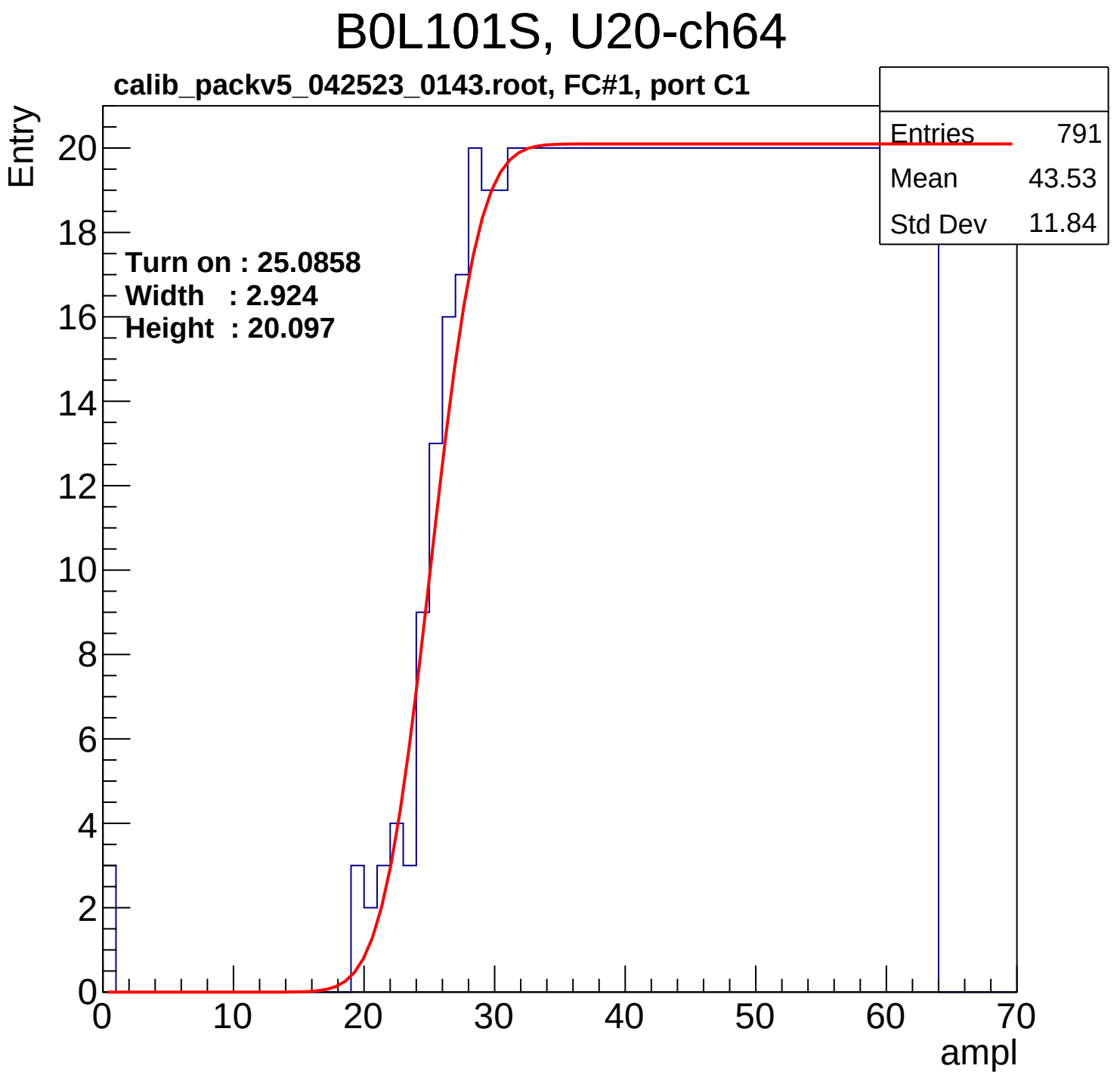
B0L101S, U20-ch64
calib_packv5_042523_0143.root, FC#1, port C1
Entries 791
Mean 43.53
Std Dev 11.84
Turn on : 25.0858
Width : 2.924
Height : 20.097
Entry
ampl
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6
8
10
12
14
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0
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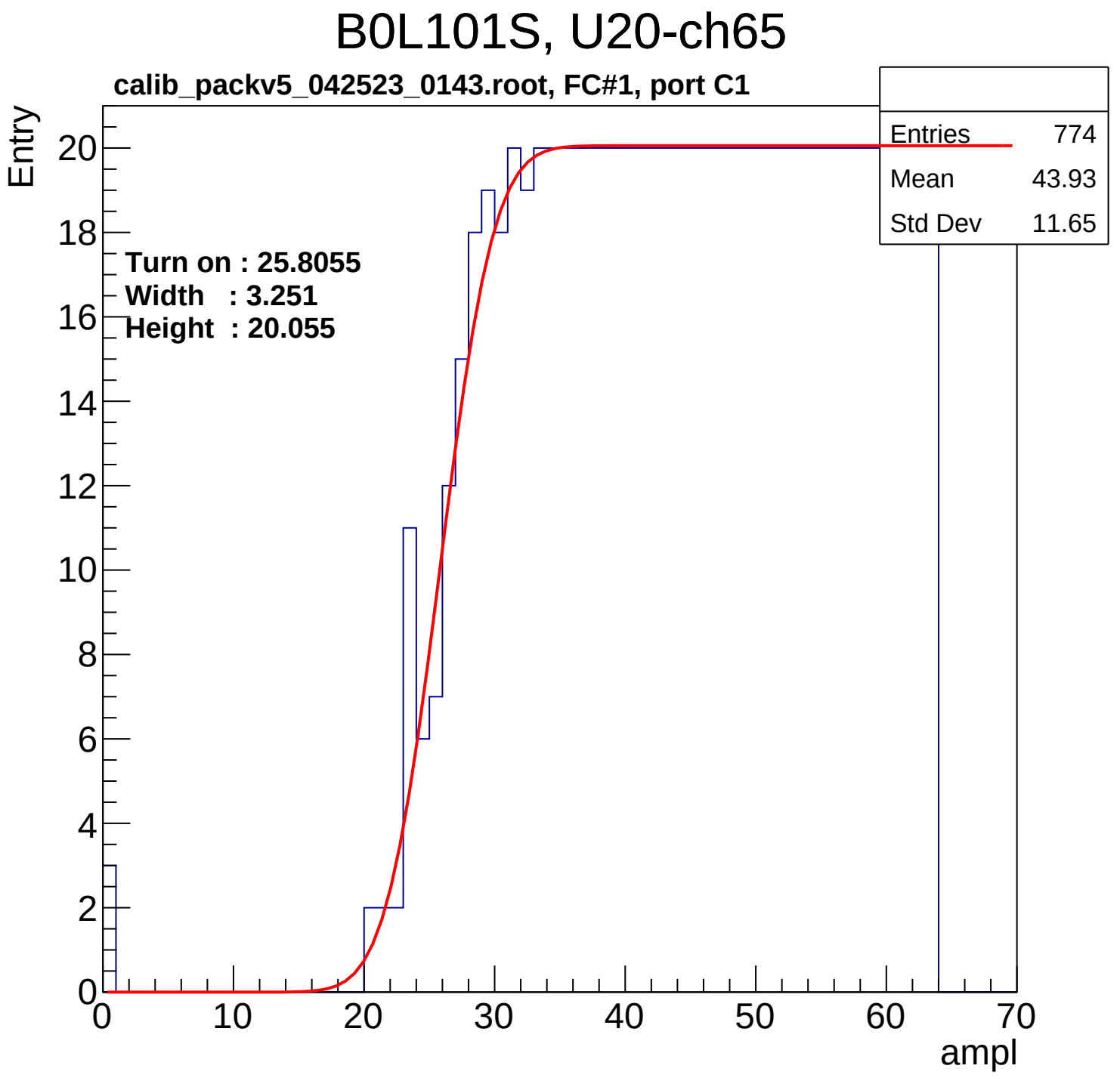
B0L101S, U20-ch65
calib_packv5_042523_0143.root, FC#1, port C1
Entries 774
Mean 43.93
Std Dev 11.65
Turn on : 25.8055
Width : 3.251
Height : 20.055
Entry
ampl
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6
8
10
12
14
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0
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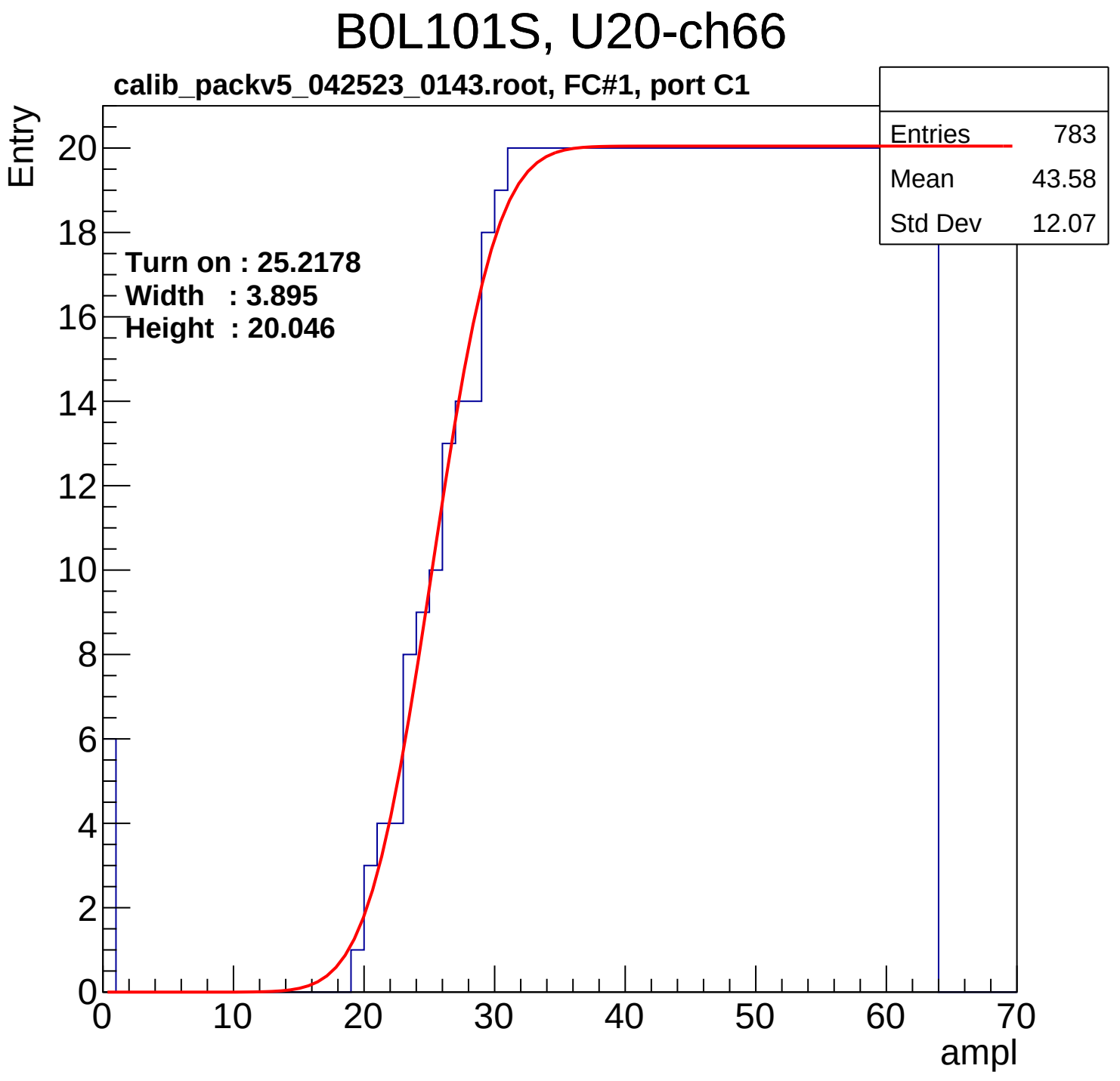
B0L101S, U20-ch66
calib_packv5_042523_0143.root, FC#1, port C1
Entries 783
Mean 43.58
Std Dev 12.07
Turn on : 25.2178
Width : 3.895
Height : 20.046
Entry
ampl
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6
8
10
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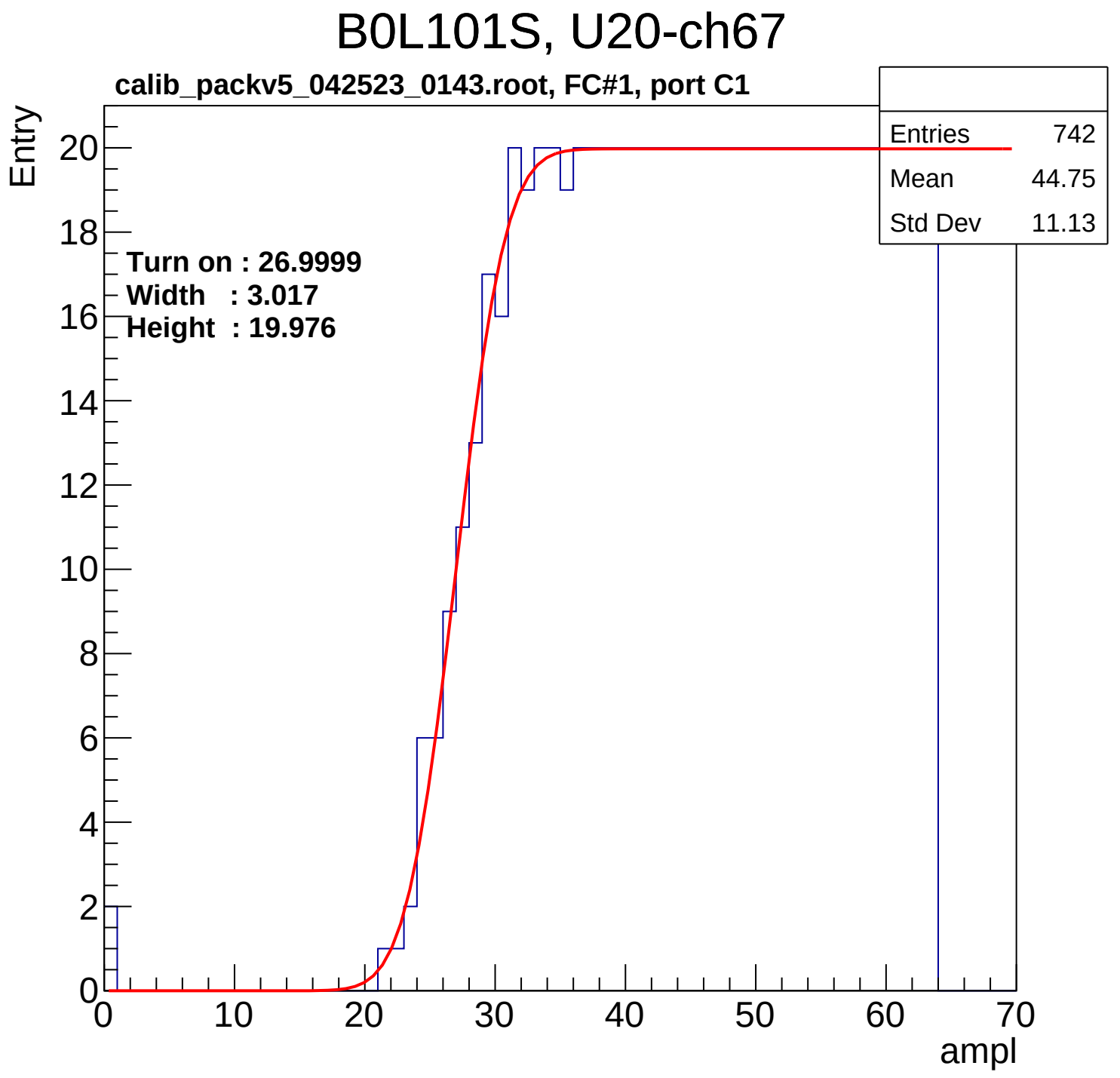
B0L101S, U20-ch67
calib_packv5_042523_0143.root, FC#1, port C1
Entries 742
Mean 44.75
Std Dev 11.13
Turn on : 26.9999
Width : 3.017
Height : 19.976
Entry
ampl
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6
8
10
12
14
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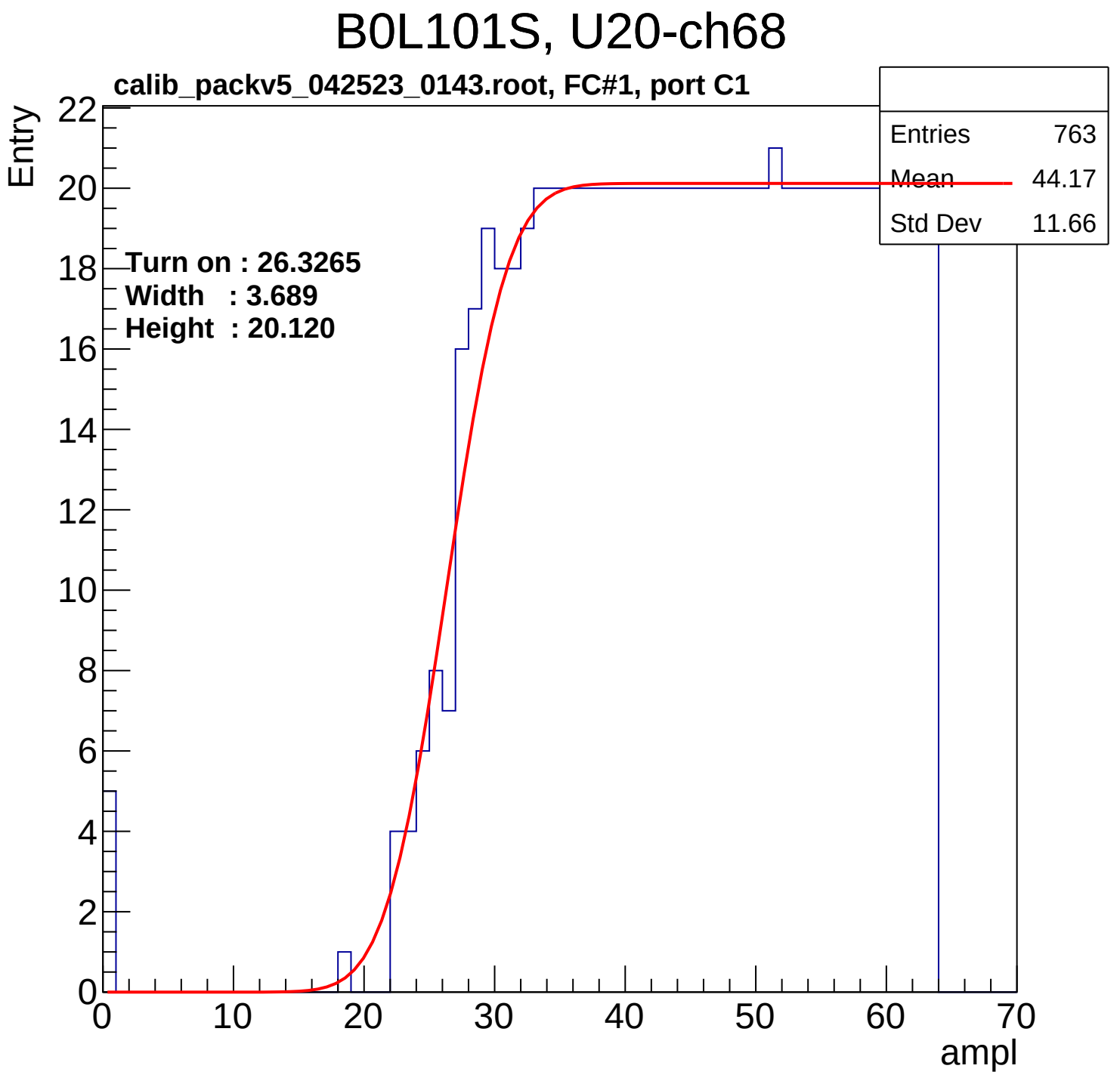
B0L101S, U20-ch68
calib_packv5_042523_0143.root, FC#1, port C1
Entries 763
Mean 44.17
Std Dev 11.66
Turn on : 26.3265
Width : 3.689
Height : 20.120
Entry
ampl
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8
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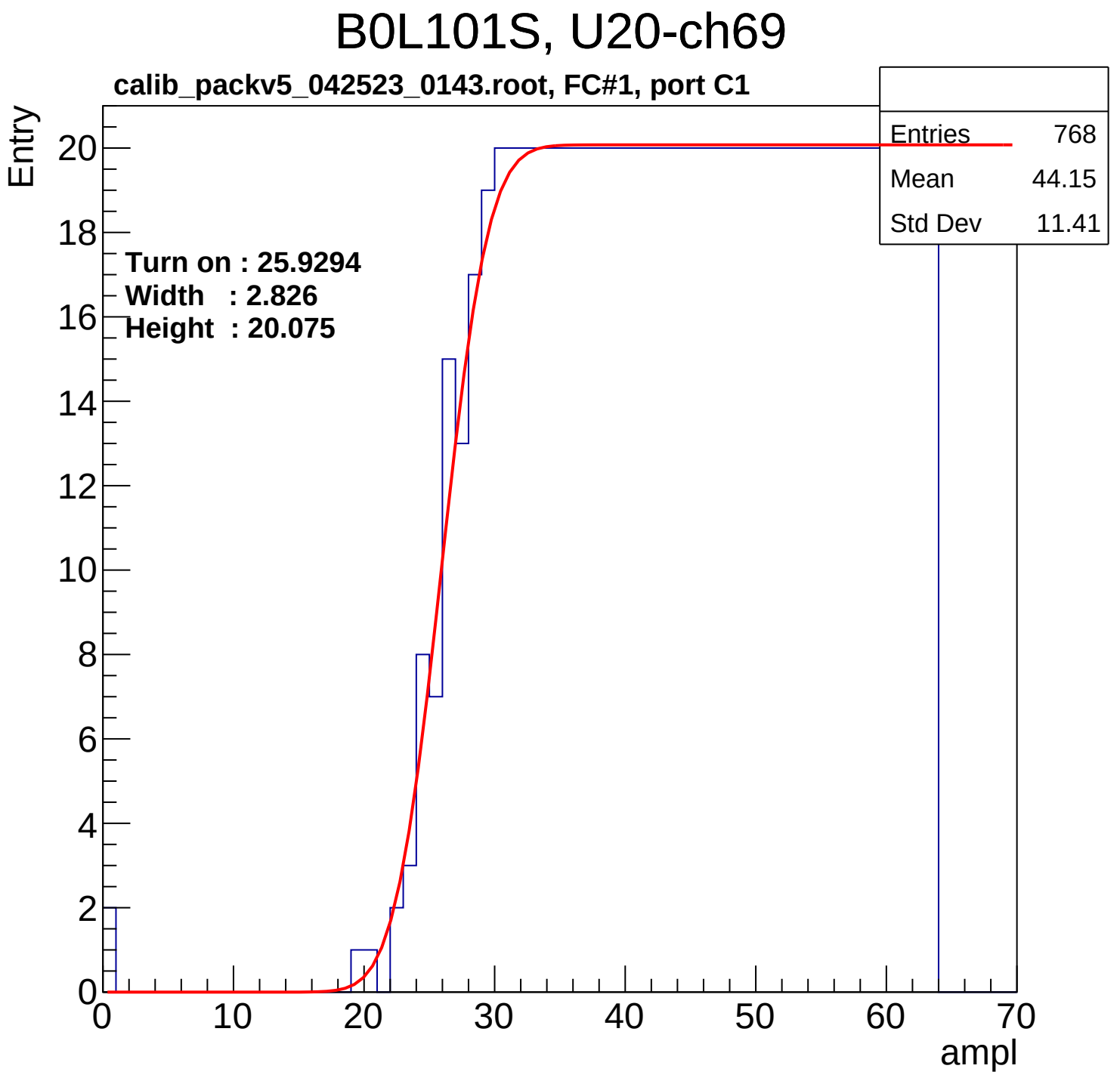
B0L101S, U20-ch69
calib_packv5_042523_0143.root, FC#1, port C1
Entries 768
Mean 44.15
Std Dev 11.41
Turn on : 25.9294
Width : 2.826
Height : 20.075
Entry
ampl
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6
8
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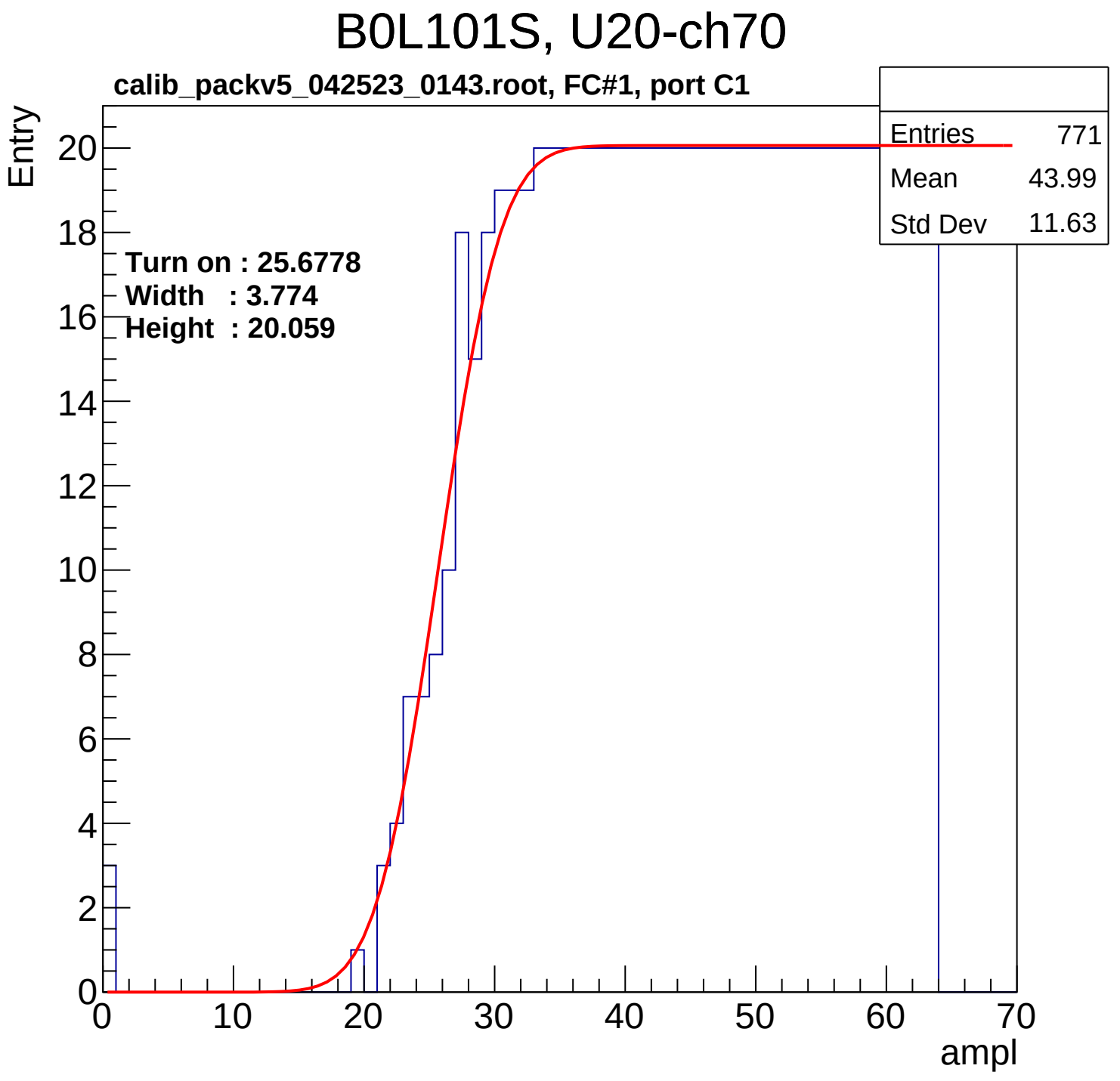
B0L101S, U20-ch70
calib_packv5_042523_0143.root, FC#1, port C1
Entries 771
Mean 43.99
Std Dev 11.63
Turn on : 25.6778
Width : 3.774
Height : 20.059
Entry
ampl
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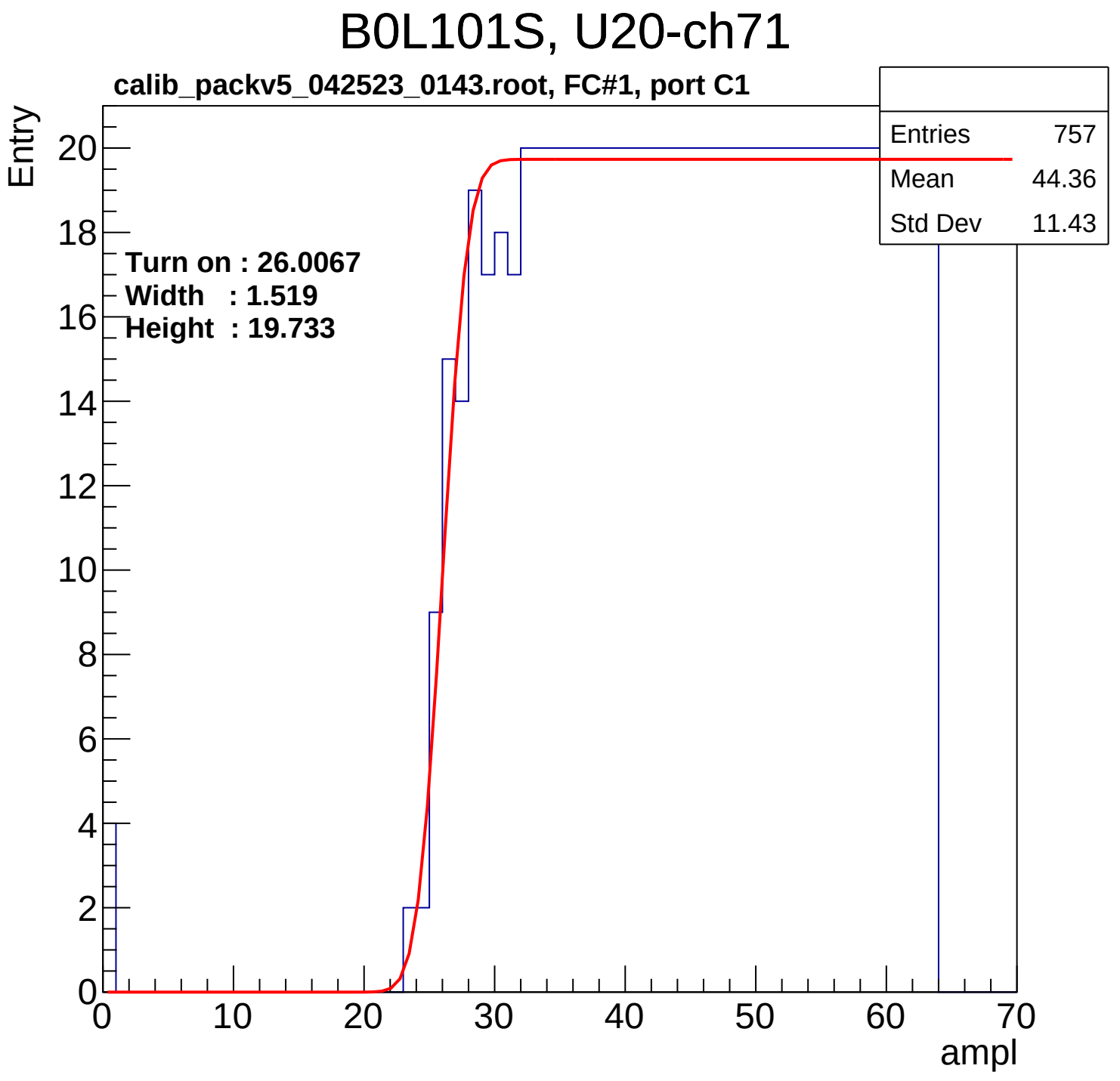
B0L101S, U20-ch71
calib_packv5_042523_0143.root, FC#1, port C1
Entries 757
Mean 44.36
Std Dev 11.43
Turn on : 26.0067
Width : 1.519
Height : 19.733
Entry
ampl
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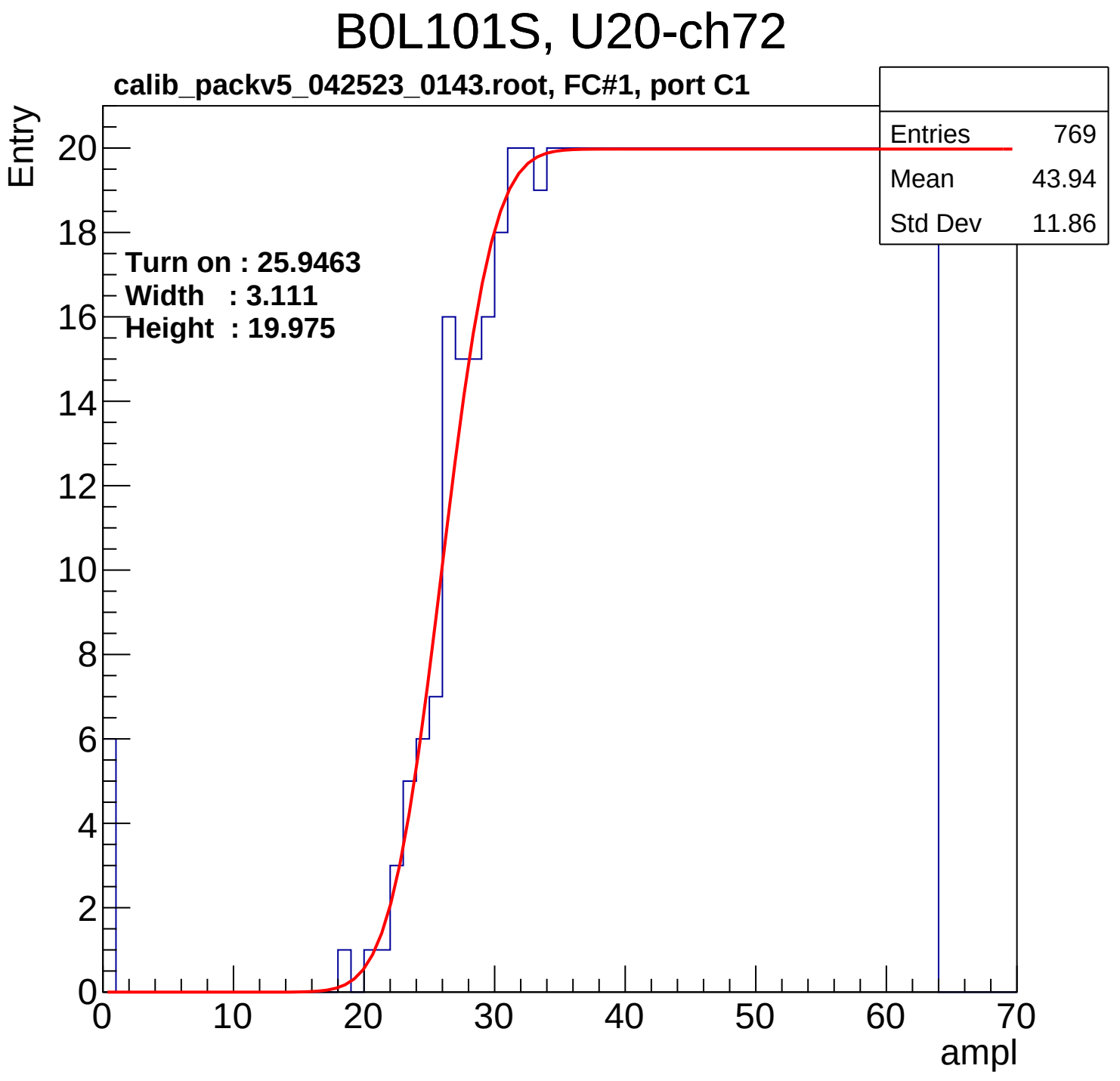
B0L101S, U20-ch72
calib_packv5_042523_0143.root, FC#1, port C1
Entries 769
Mean 43.94
Std Dev 11.86
Turn on : 25.9463
Width : 3.111
Height : 19.975
Entry
ampl
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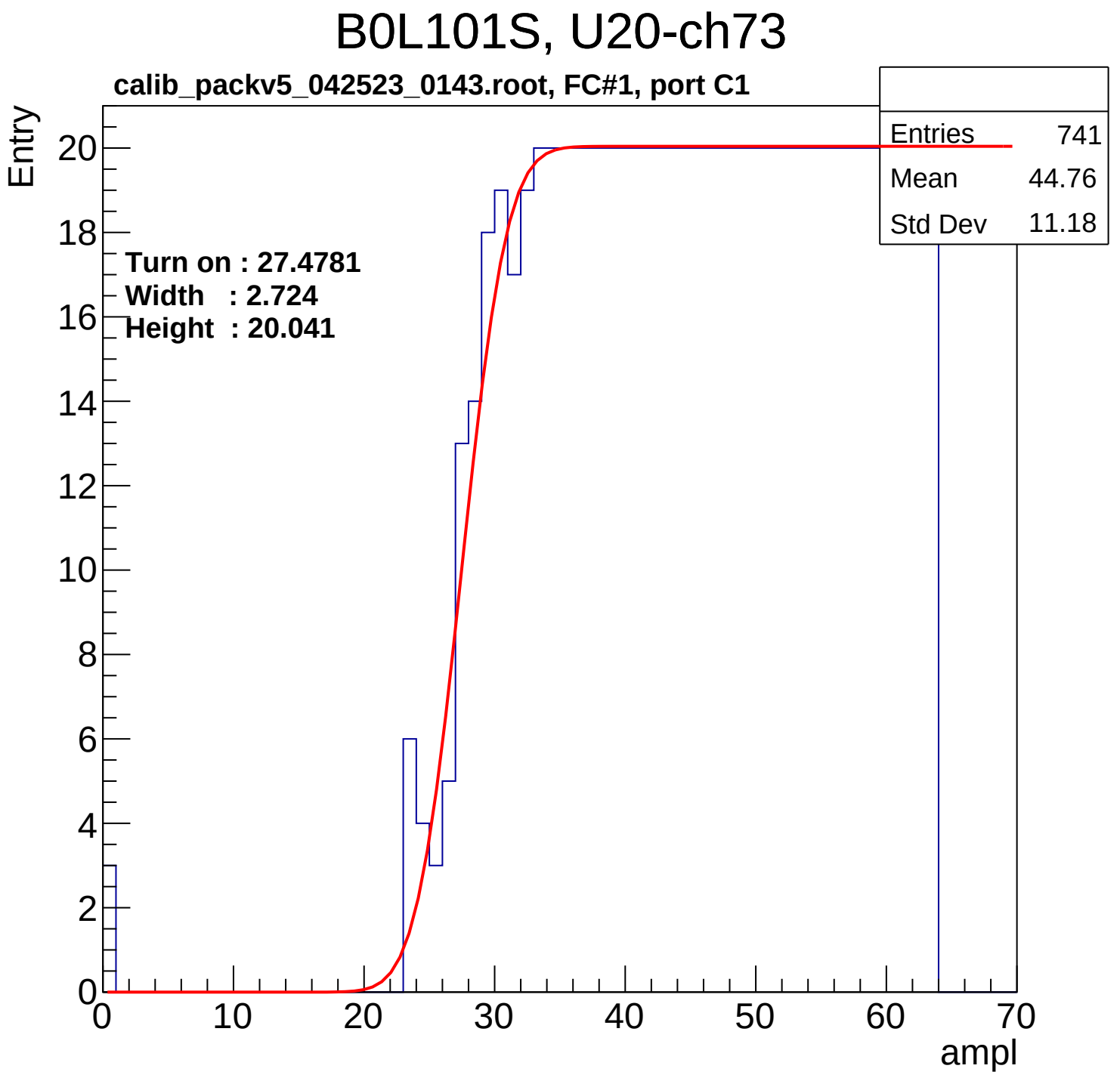
B0L101S, U20-ch73
calib_packv5_042523_0143.root, FC#1, port C1
Entries 741
Mean 44.76
Std Dev 11.18
Turn on : 27.4781
Width : 2.724
Height : 20.041
Entry
ampl
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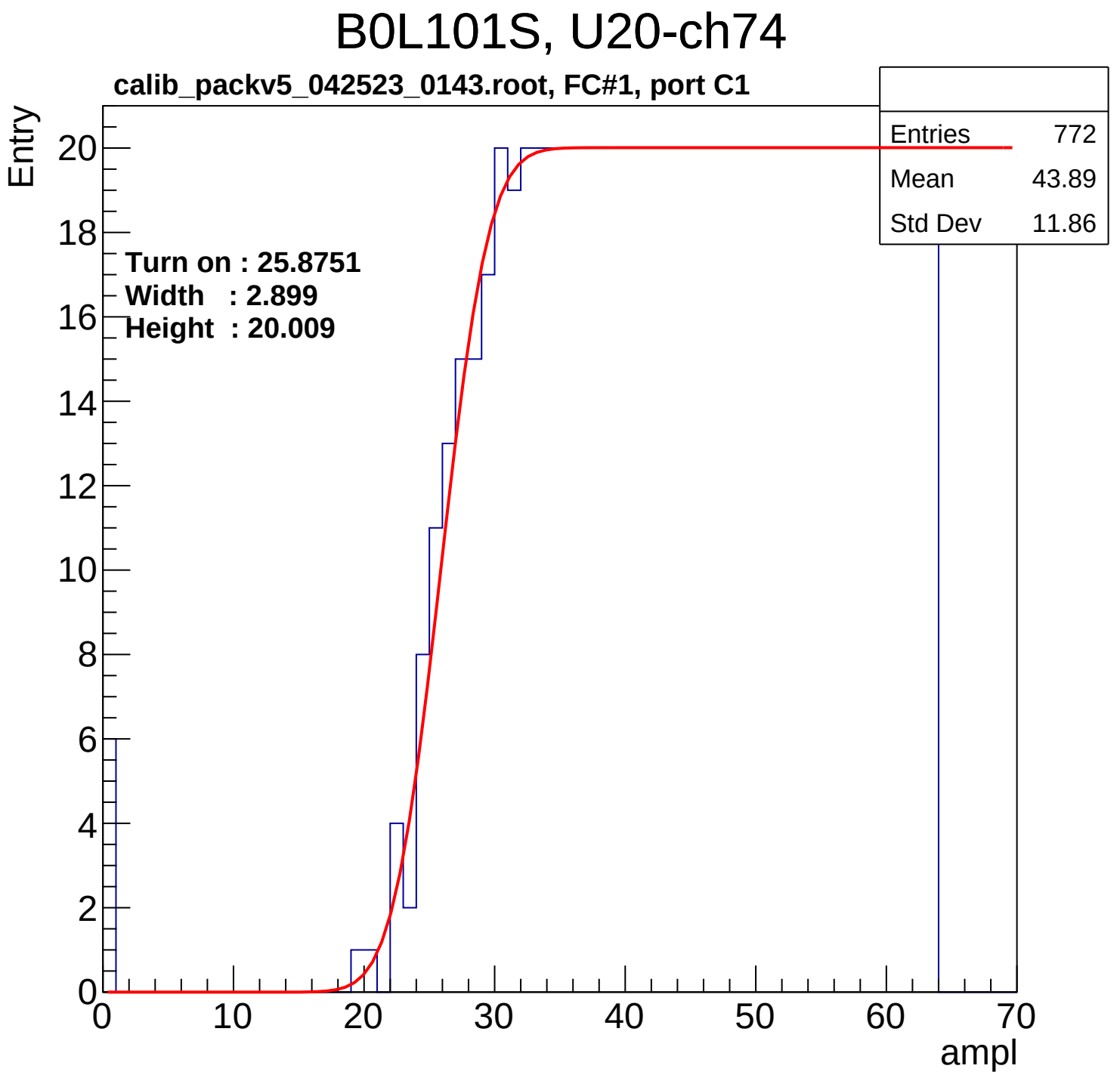
B0L101S, U20-ch74
calib_packv5_042523_0143.root, FC#1, port C1
Entries 772
Mean 43.89
Std Dev 11.86
Turn on : 25.8751
Width : 2.899
Height : 20.009
Entry
ampl
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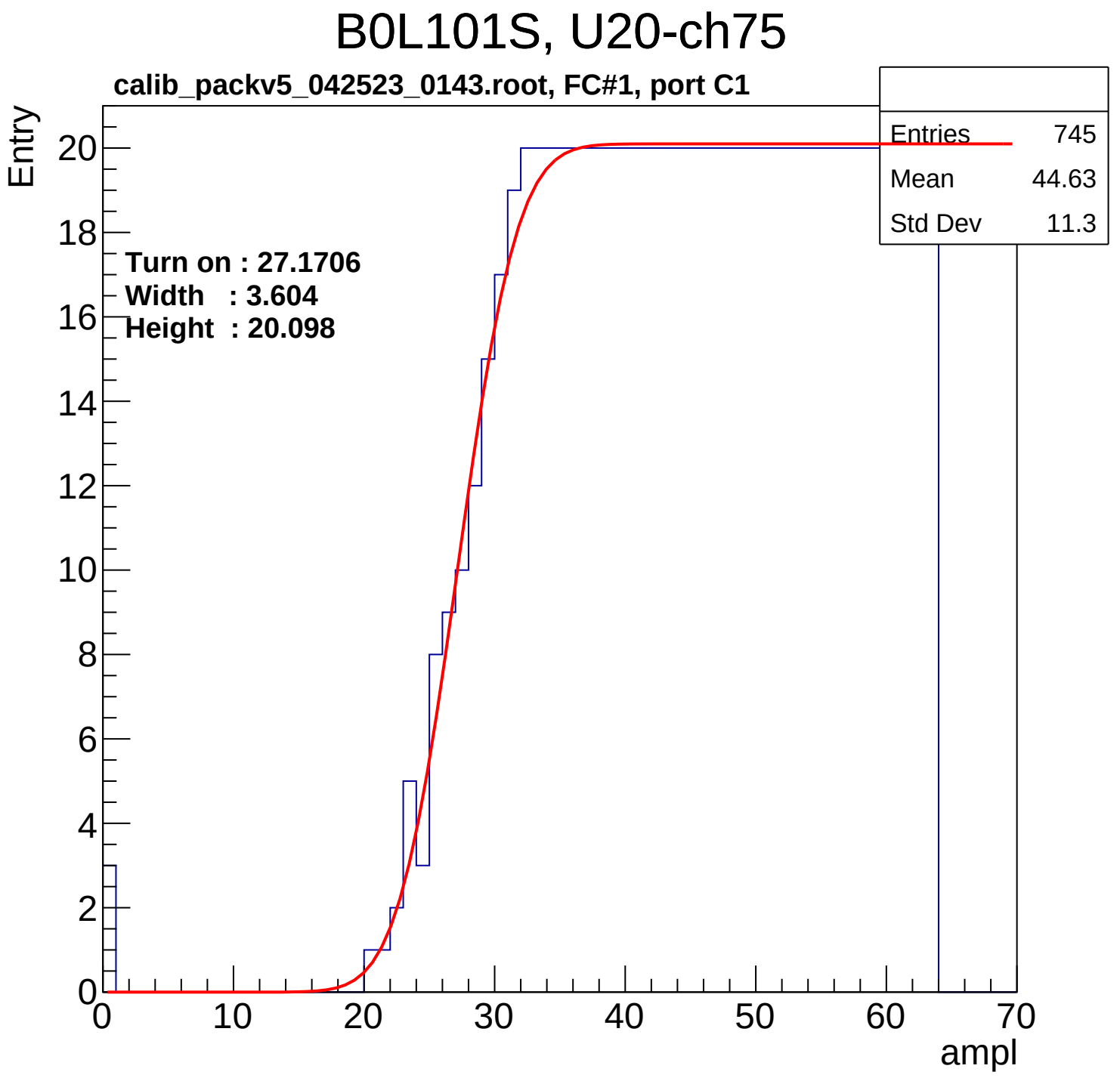
B0L101S, U20-ch75
calib_packv5_042523_0143.root, FC#1, port C1
Entries 745
Mean 44.63
Std Dev 11.3
Turn on : 27.1706
Width : 3.604
Height : 20.098
Entry
ampl
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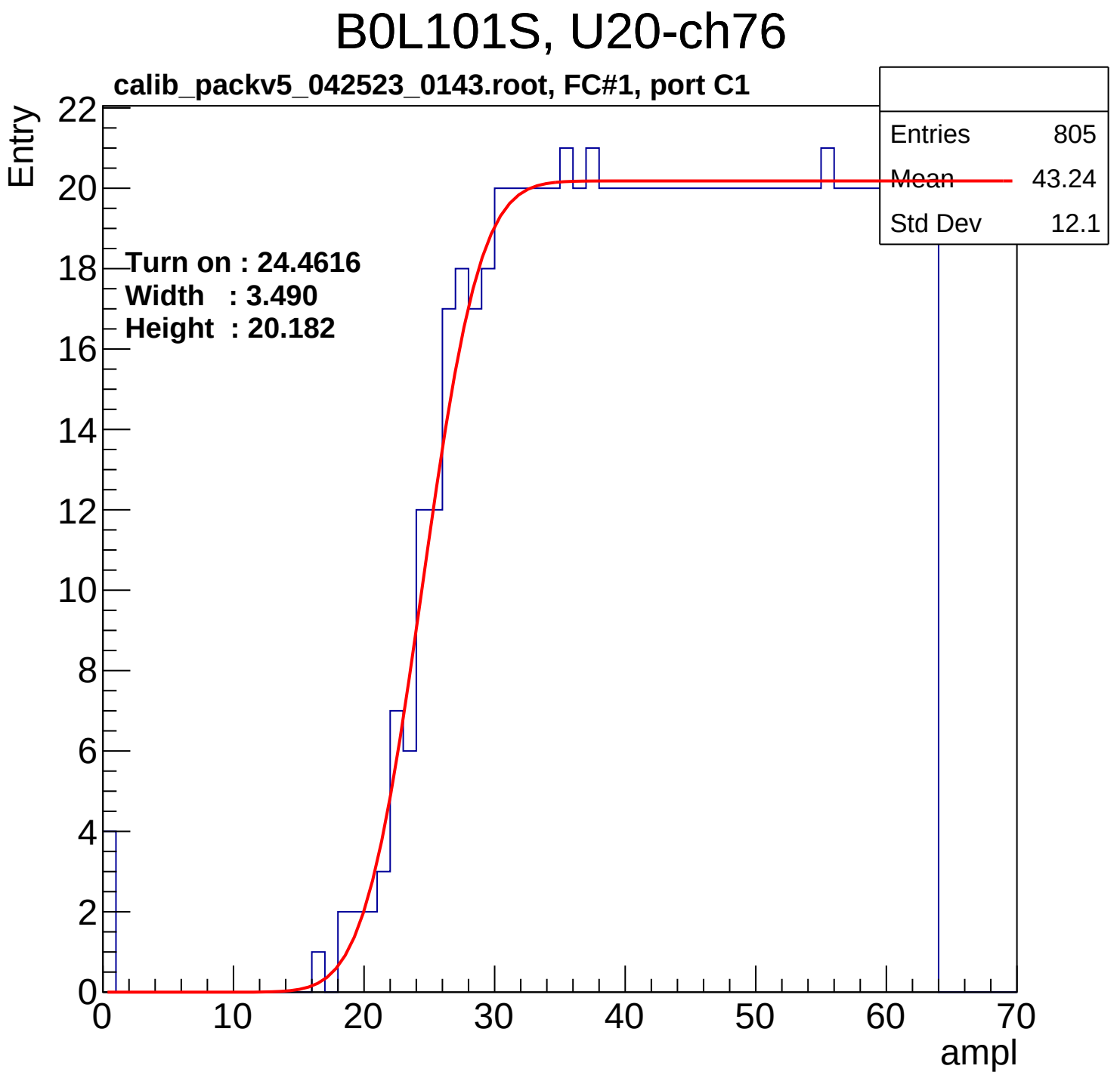
B0L101S, U20-ch76
calib_packv5_042523_0143.root, FC#1, port C1
Entries 805
Mean 43.24
Std Dev 12.1
Turn on : 24.4616
Width : 3.490
Height : 20.182
Entry
ampl
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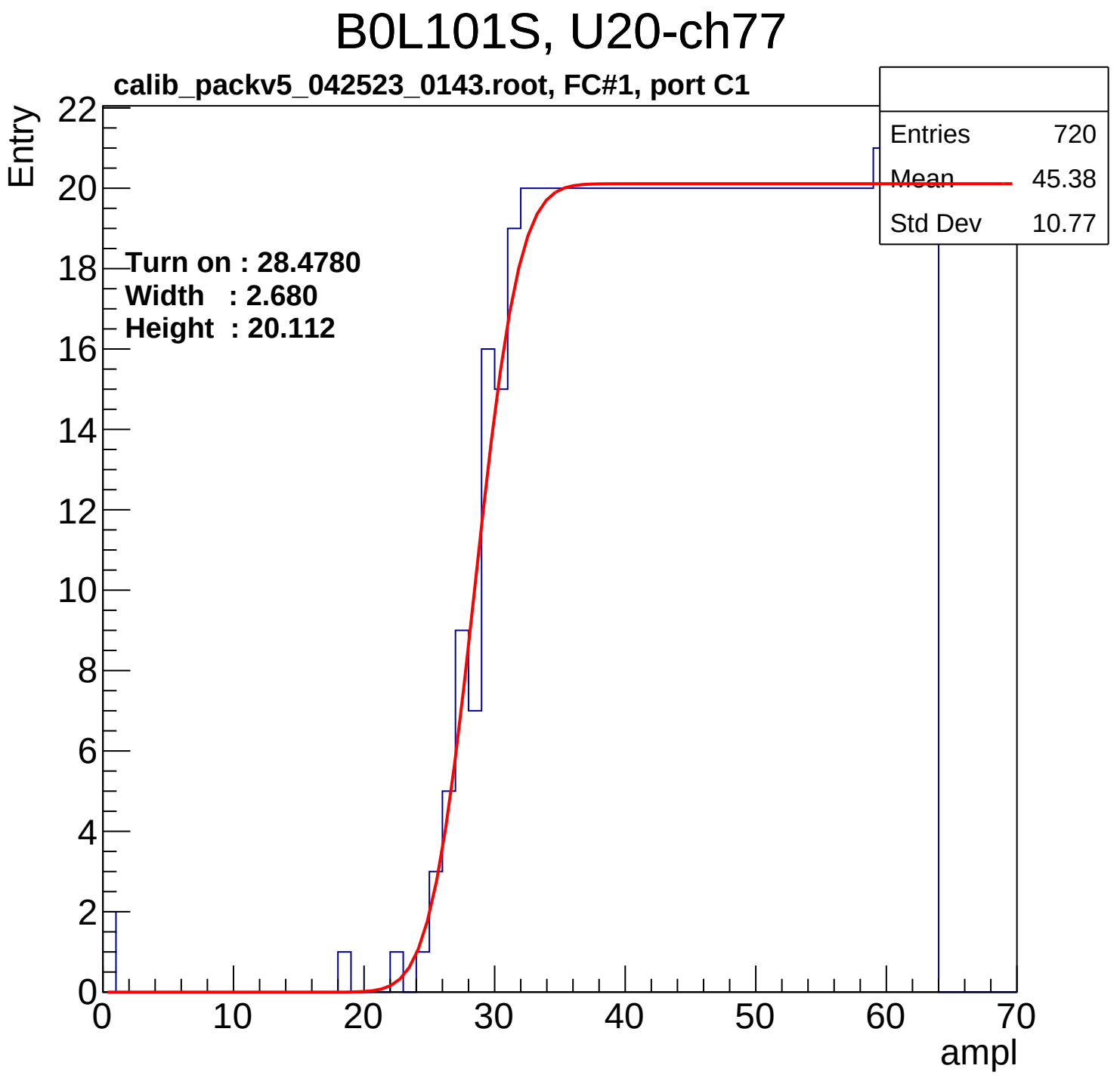
B0L101S, U20-ch77
calib_packv5_042523_0143.root, FC#1, port C1
Entries 720
Mean 45.38
Std Dev 10.77
Turn on : 28.4780
Width : 2.680
Height : 20.112
Entry
ampl
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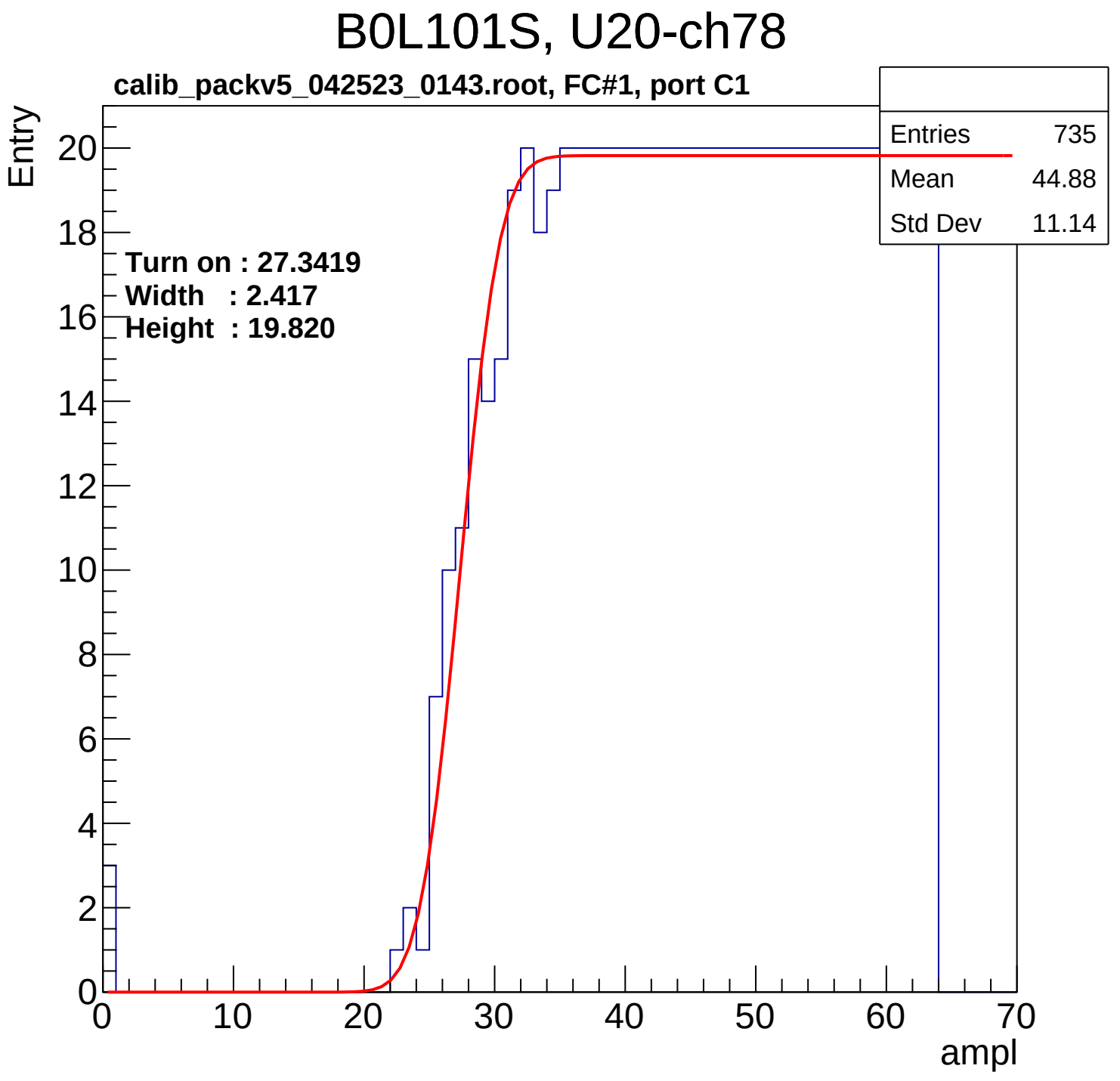
B0L101S, U20-ch78
calib_packv5_042523_0143.root, FC#1, port C1
Entries 735
Mean 44.88
Std Dev 11.14
Turn on : 27.3419
Width : 2.417
Height : 19.820
Entry
ampl
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6
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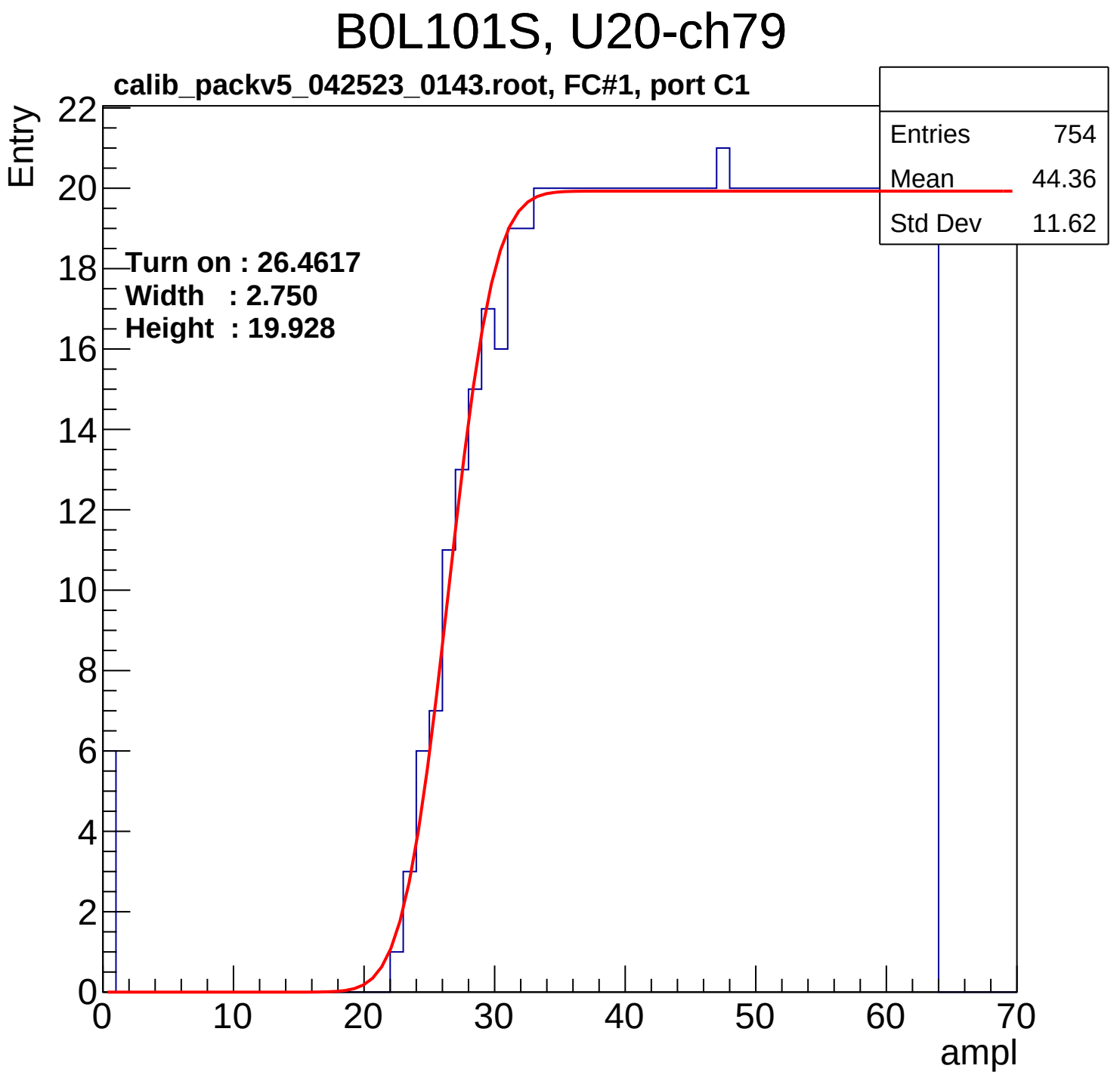
B0L101S, U20-ch79
calib_packv5_042523_0143.root, FC#1, port C1
Entries 754
Mean 44.36
Std Dev 11.62
Turn on : 26.4617
Width : 2.750
Height : 19.928
Entry
ampl
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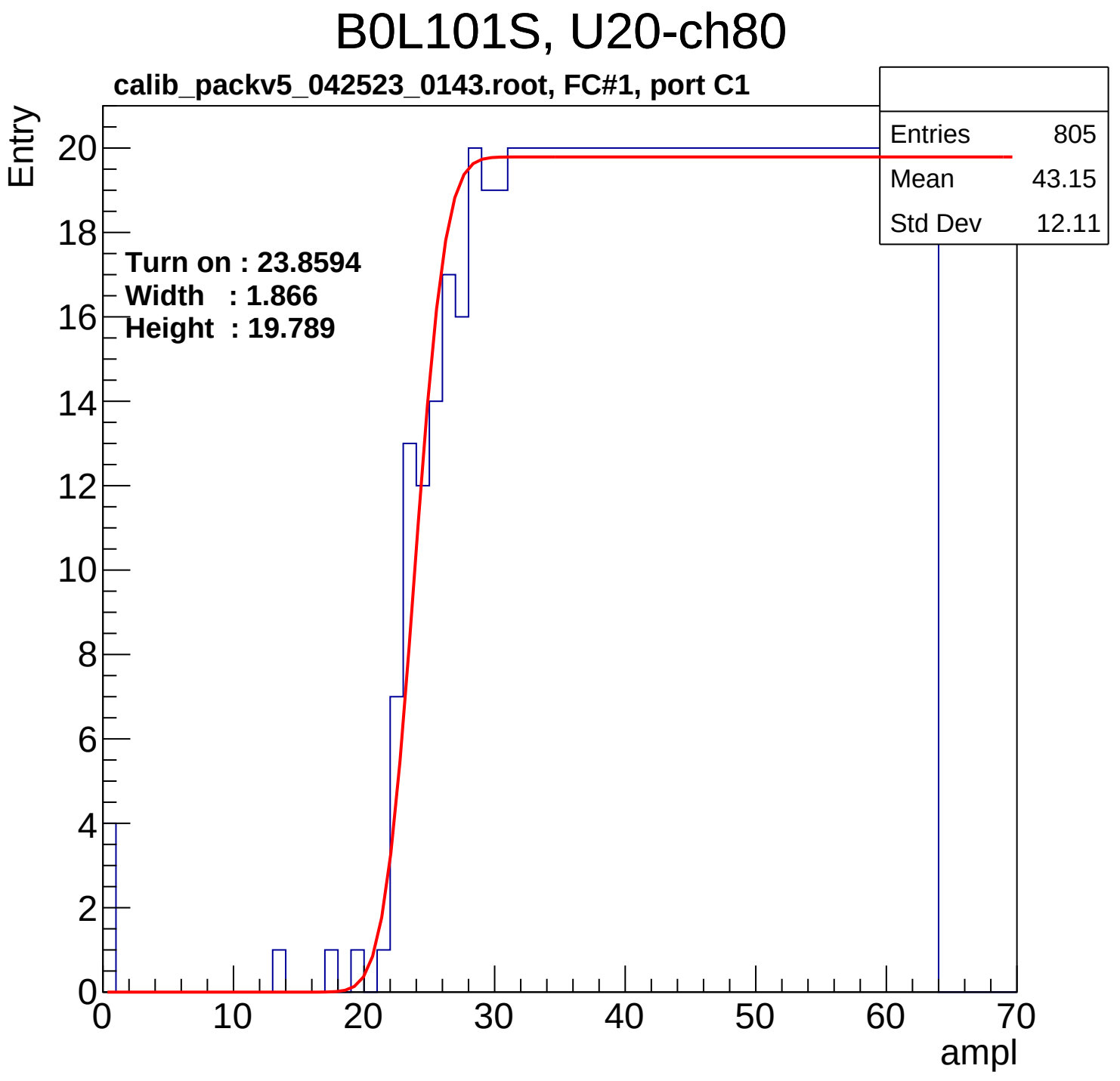
B0L101S, U20-ch80
calib_packv5_042523_0143.root, FC#1, port C1
Entries 805
Mean 43.15
Std Dev 12.11
Turn on : 23.8594
Width : 1.866
Height : 19.789
Entry
ampl
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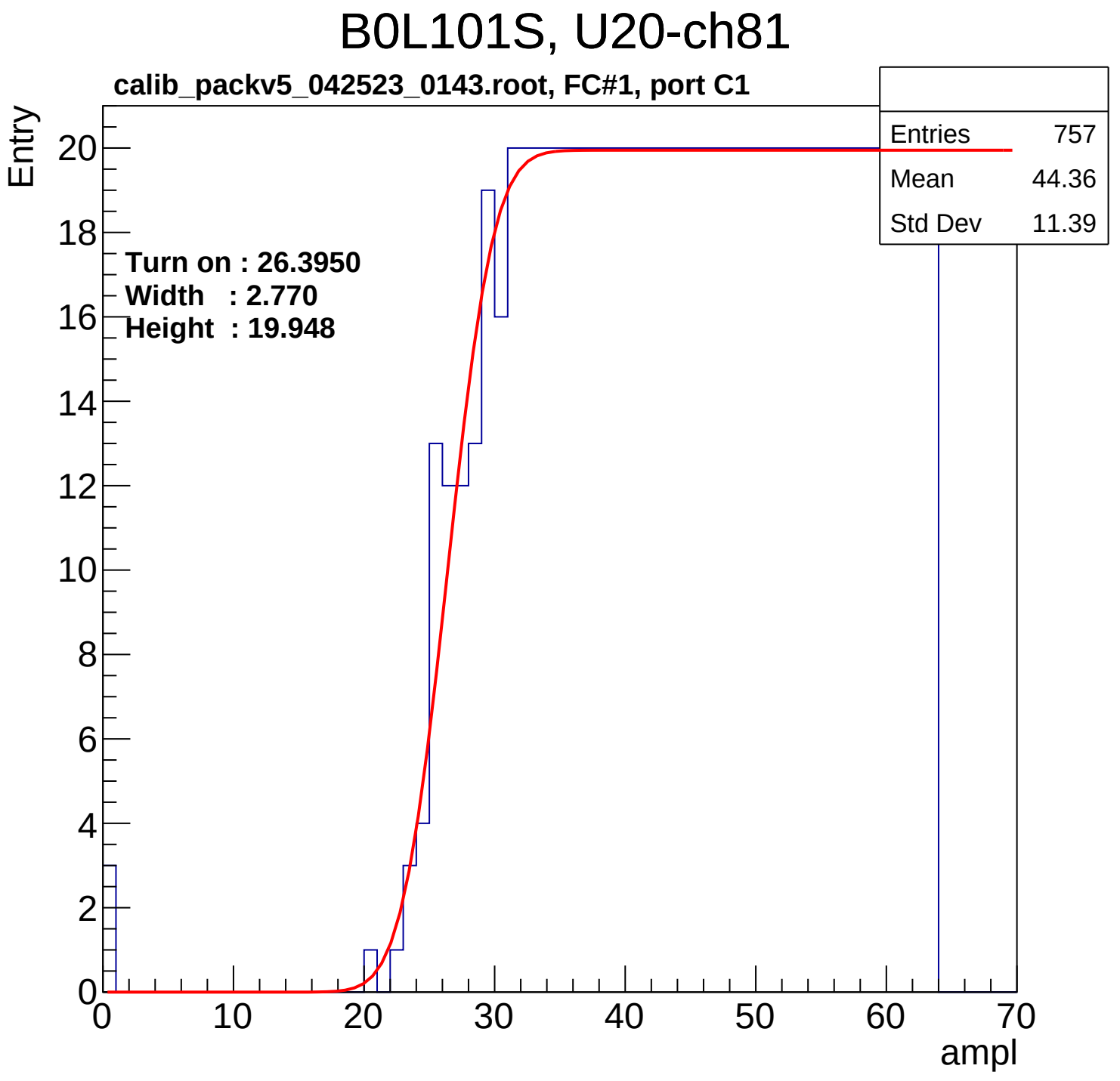
B0L101S, U20-ch81
calib_packv5_042523_0143.root, FC#1, port C1
Entries 757
Mean 44.36
Std Dev 11.39
Turn on : 26.3950
Width : 2.770
Height : 19.948
Entry
ampl
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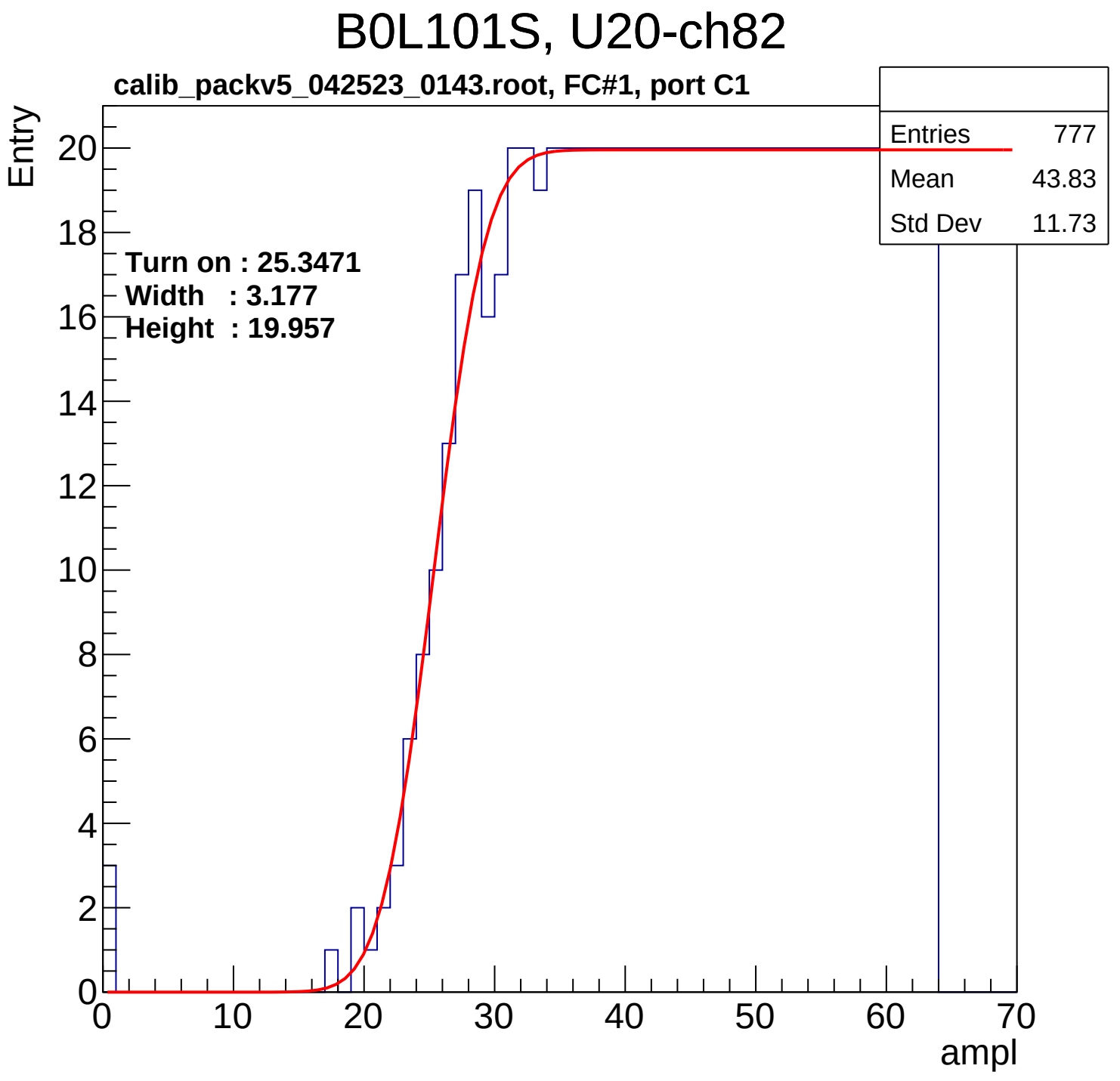
B0L101S, U20-ch82
calib_packv5_042523_0143.root, FC#1, port C1
Entries 777
Mean 43.83
Std Dev 11.73
Turn on : 25.3471
Width : 3.177
Height : 19.957
Entry
ampl
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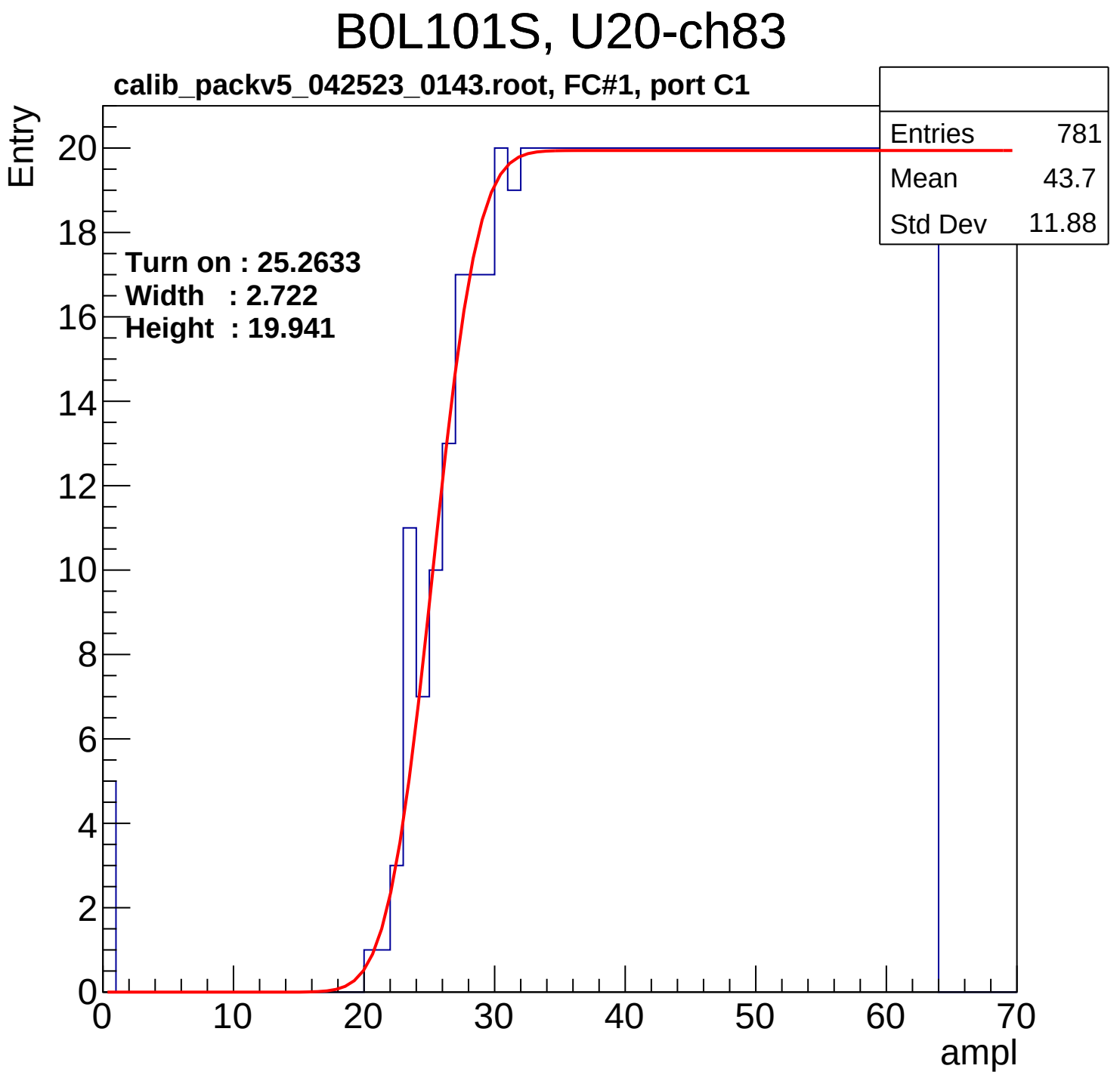
B0L101S, U20-ch83
calib_packv5_042523_0143.root, FC#1, port C1
Entries 781
Mean 43.7
Std Dev 11.88
Turn on : 25.2633
Width : 2.722
Height : 19.941
Entry
ampl
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6
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10
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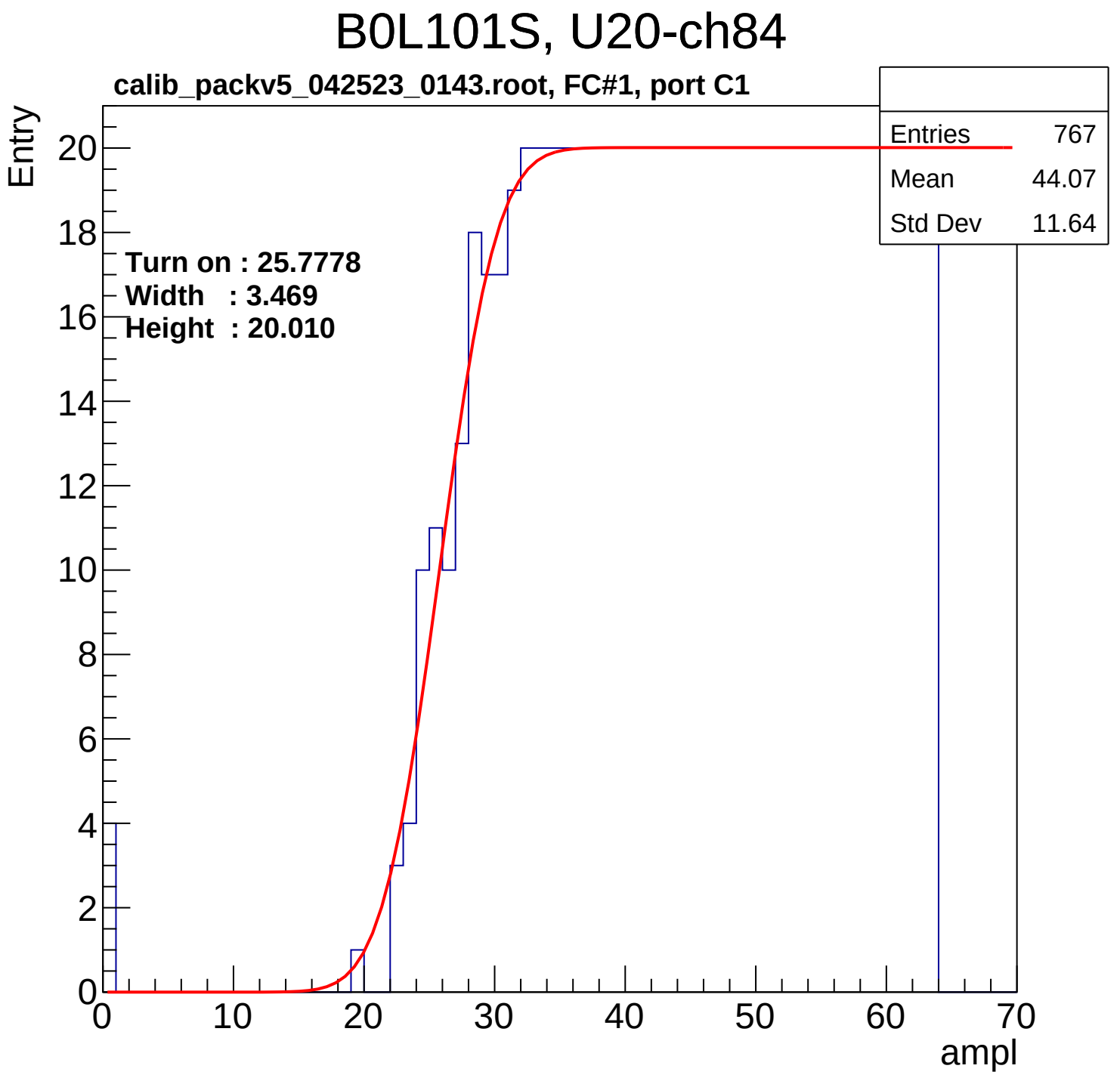
B0L101S, U20-ch84
calib_packv5_042523_0143.root, FC#1, port C1
Entries 767
Mean 44.07
Std Dev 11.64
Turn on : 25.7778
Width : 3.469
Height : 20.010
Entry
ampl
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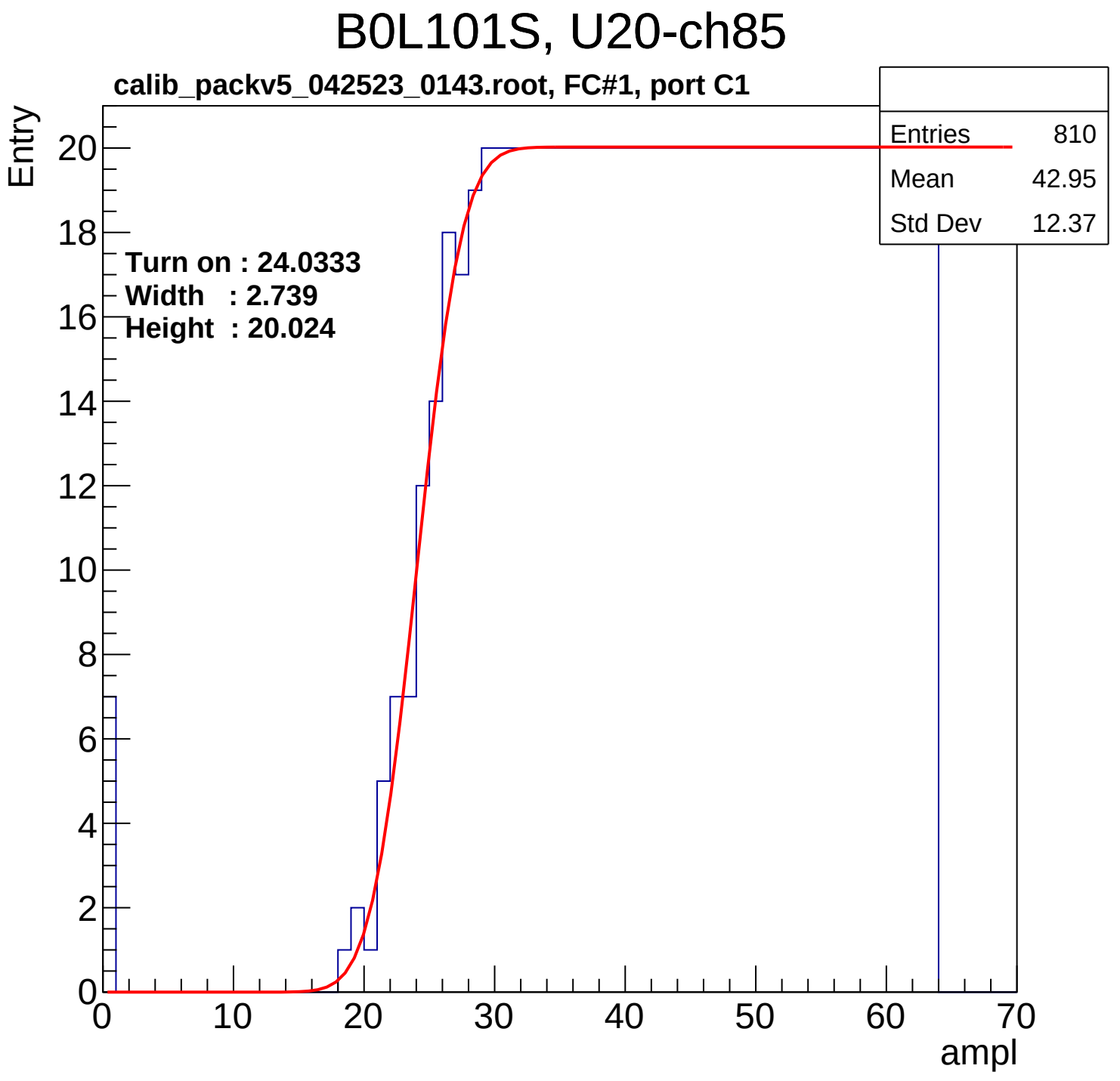
B0L101S, U20-ch85
calib_packv5_042523_0143.root, FC#1, port C1
Entries 810
Mean 42.95
Std Dev 12.37
Turn on : 24.0333
Width : 2.739
Height : 20.024
Entry
ampl
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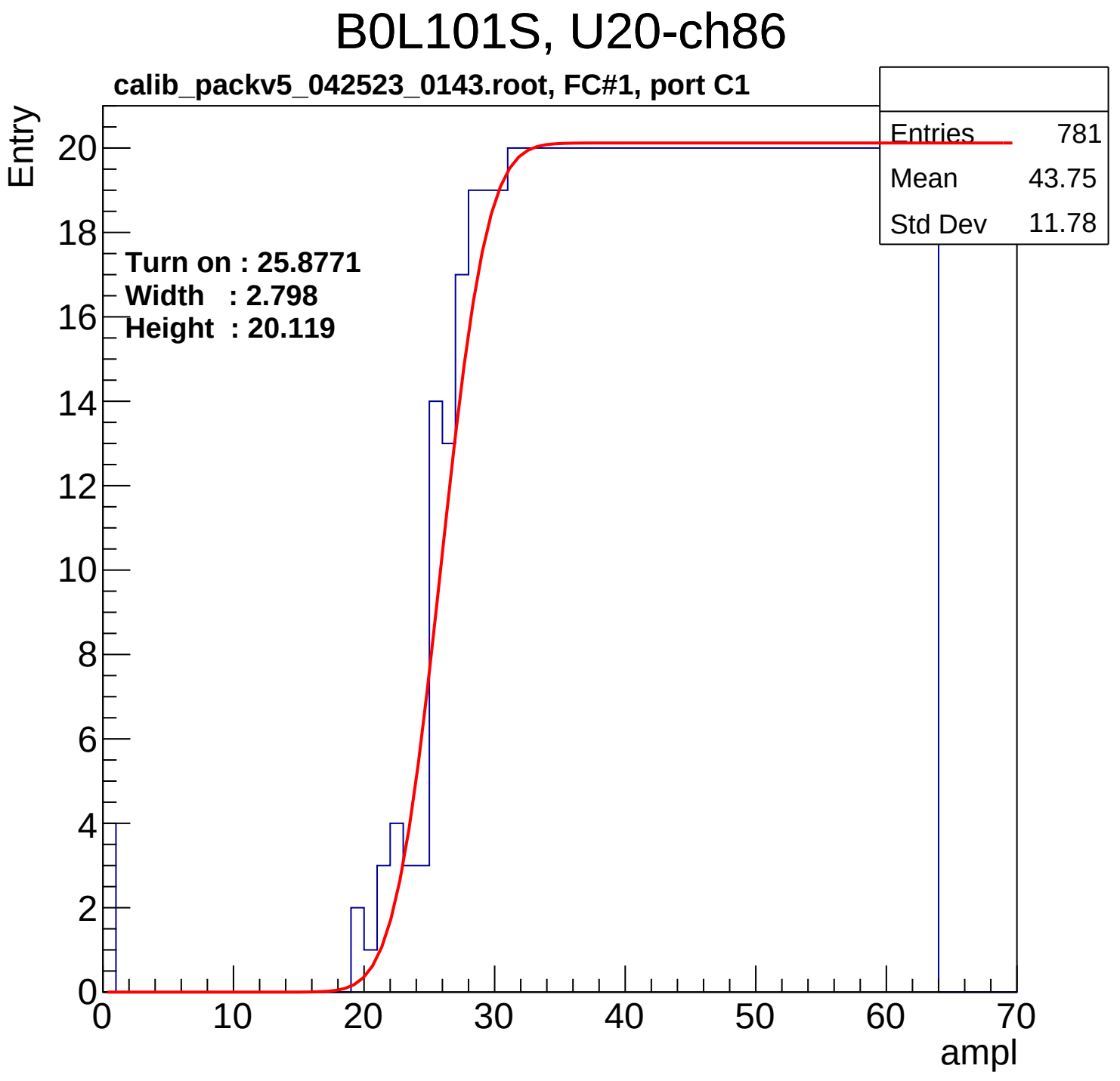
B0L101S, U20-ch86
calib_packv5_042523_0143.root, FC#1, port C1
Entries 781
Mean 43.75
Std Dev 11.78
Turn on : 25.8771
Width : 2.798
Height : 20.119
Entry
ampl
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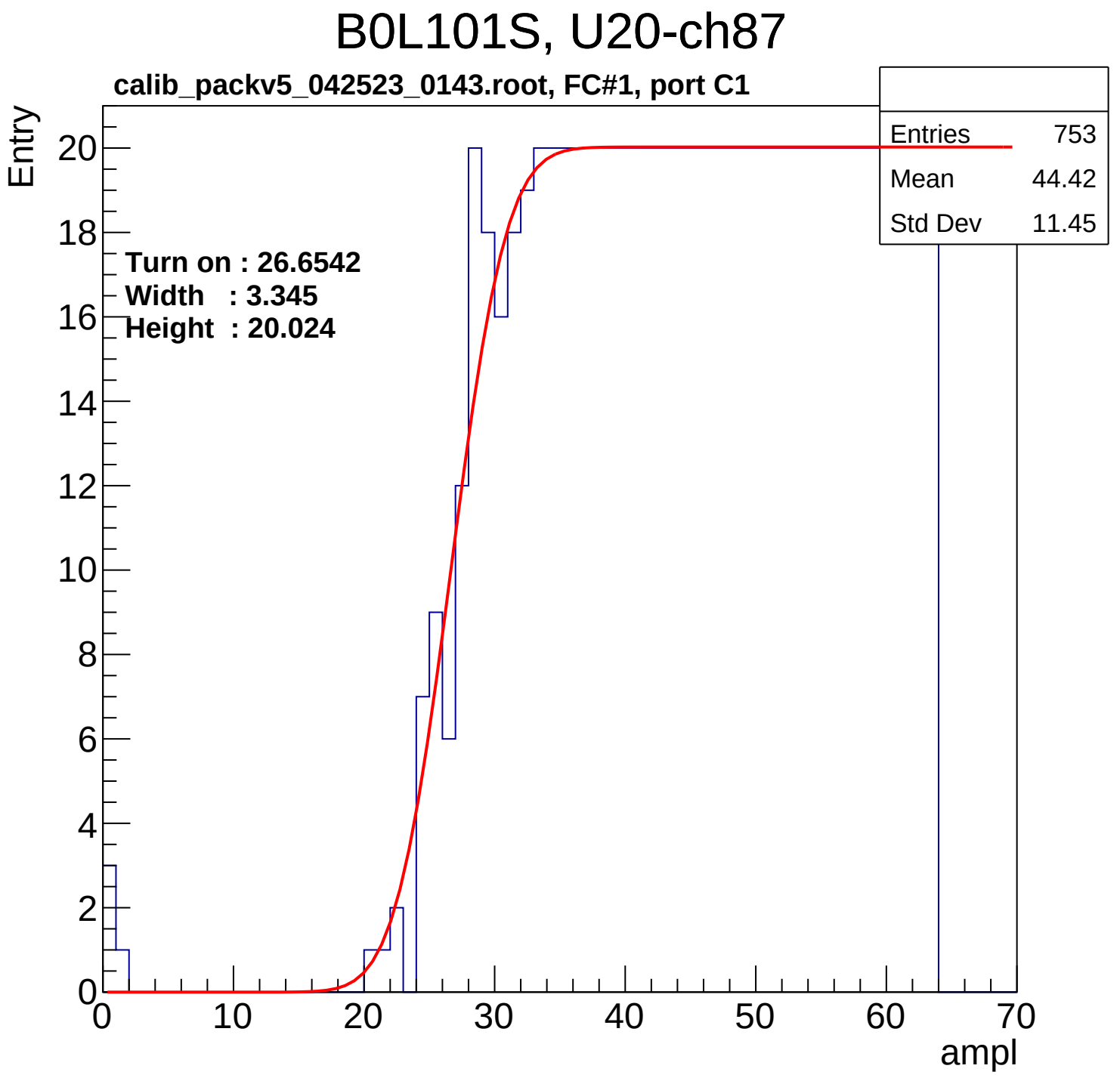
B0L101S, U20-ch87
calib_packv5_042523_0143.root, FC#1, port C1
Entries 753
Mean 44.42
Std Dev 11.45
Turn on : 26.6542
Width : 3.345
Height : 20.024
Entry
ampl
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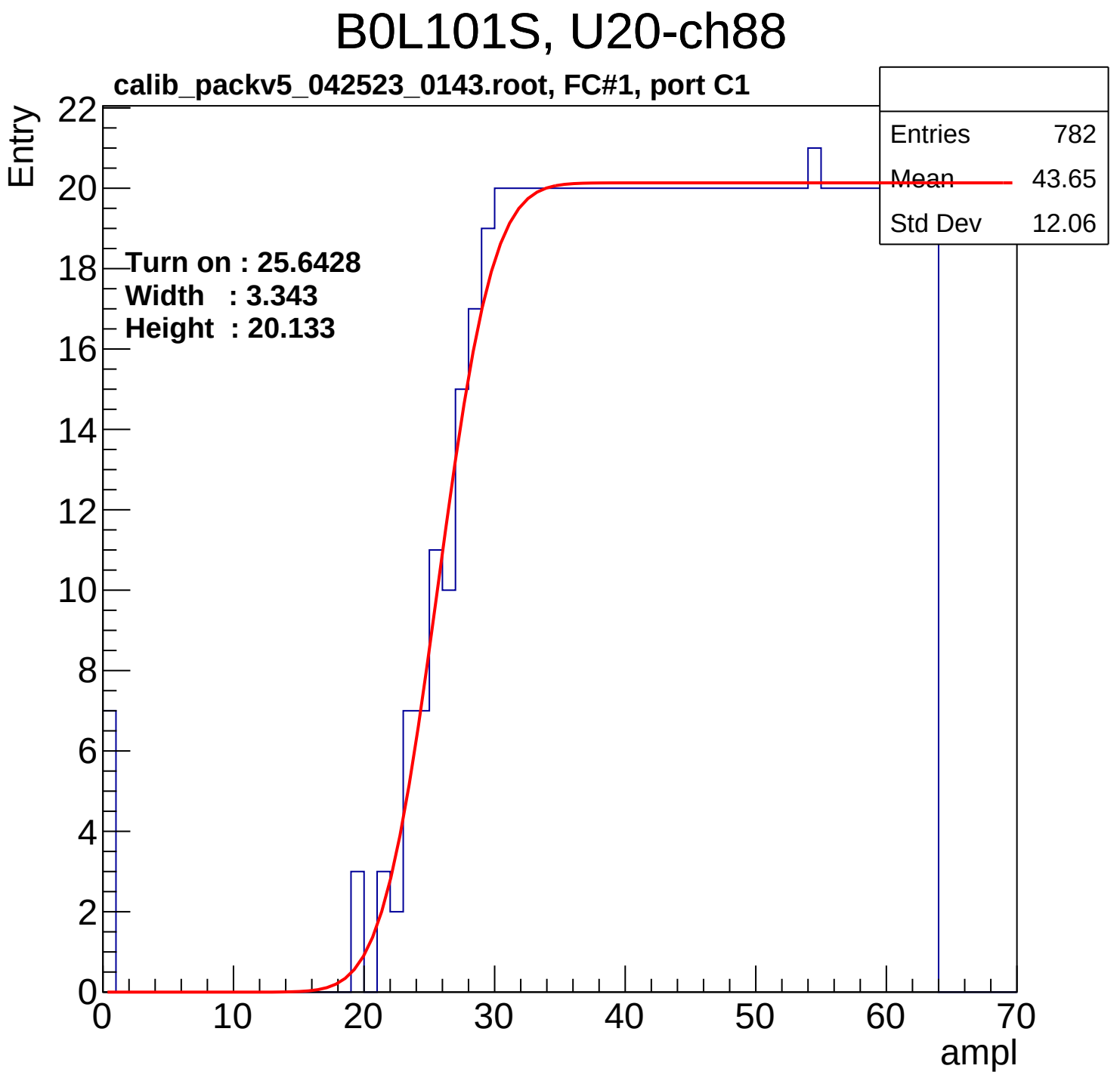
B0L101S, U20-ch88
calib_packv5_042523_0143.root, FC#1, port C1
Entries 782
Mean 43.65
Std Dev 12.06
Turn on : 25.6428
Width : 3.343
Height : 20.133
Entry
ampl
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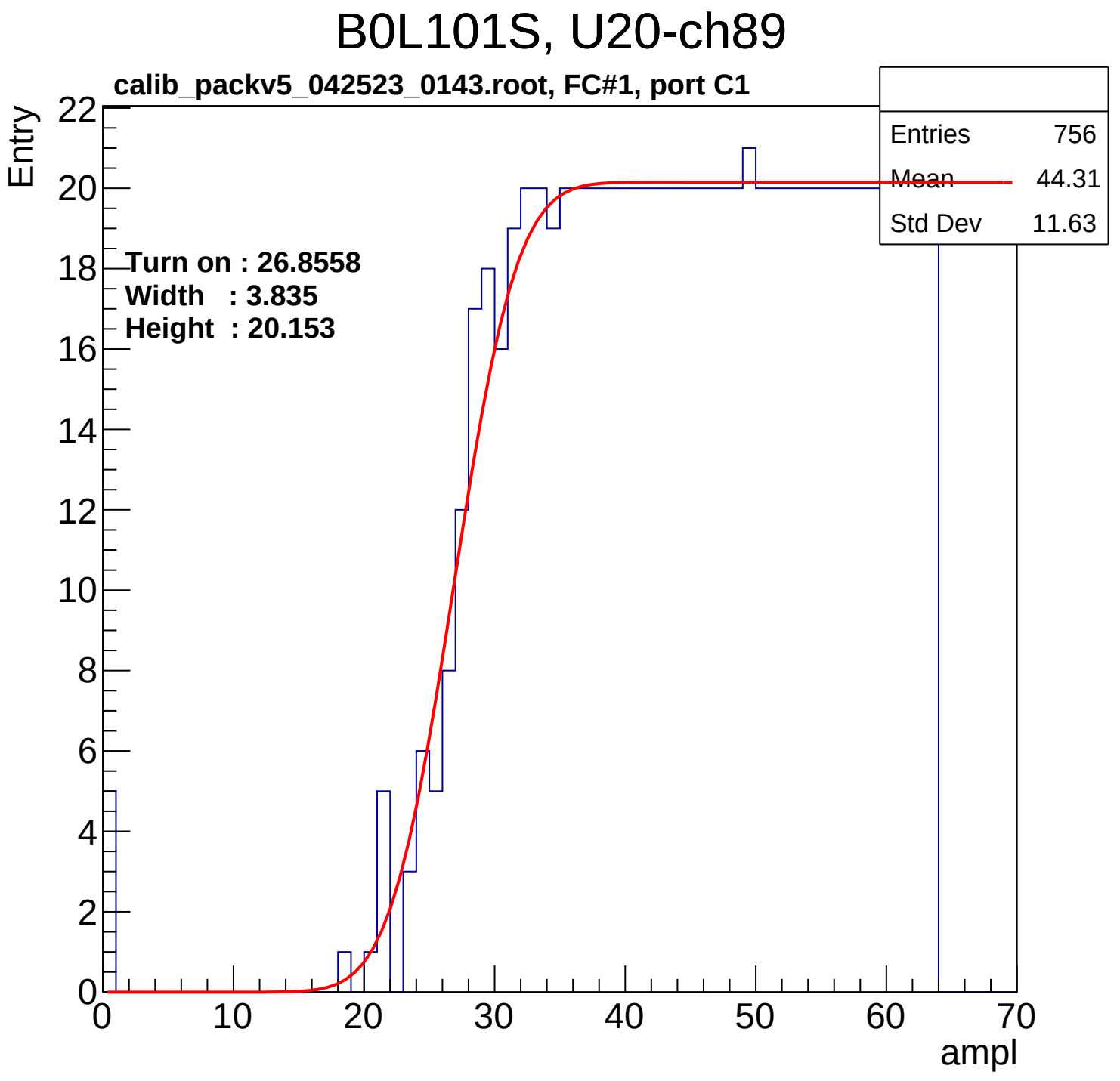
B0L101S, U20-ch89
calib_packv5_042523_0143.root, FC#1, port C1
Entries 756
Mean 44.31
Std Dev 11.63
Turn on : 26.8558
Width : 3.835
Height : 20.153
Entry
ampl
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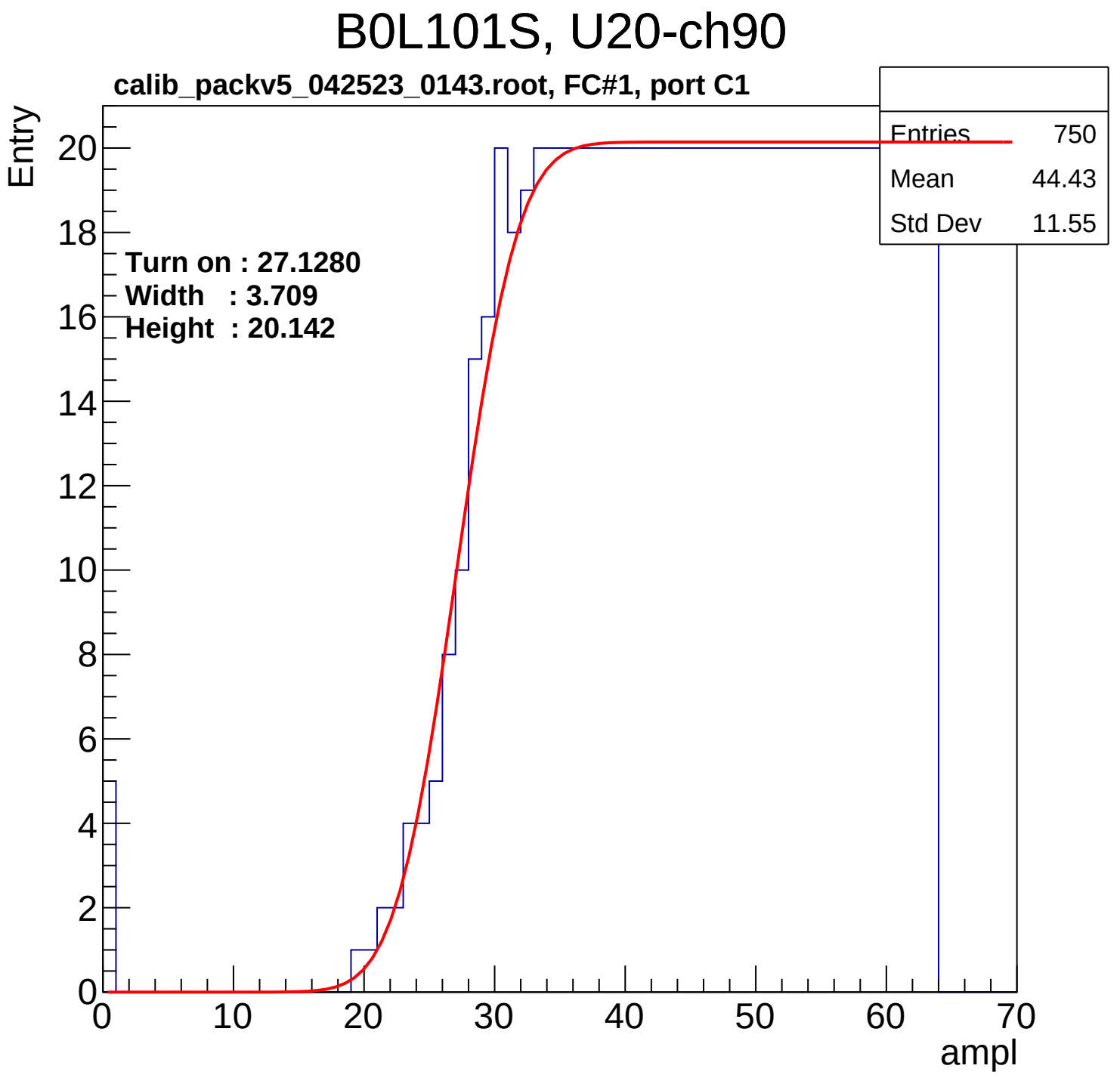
B0L101S, U20-ch90
calib_packv5_042523_0143.root, FC#1, port C1
Entries 750
Mean 44.43
Std Dev 11.55
Turn on : 27.1280
Width : 3.709
Height : 20.142
Entry
ampl
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6
8
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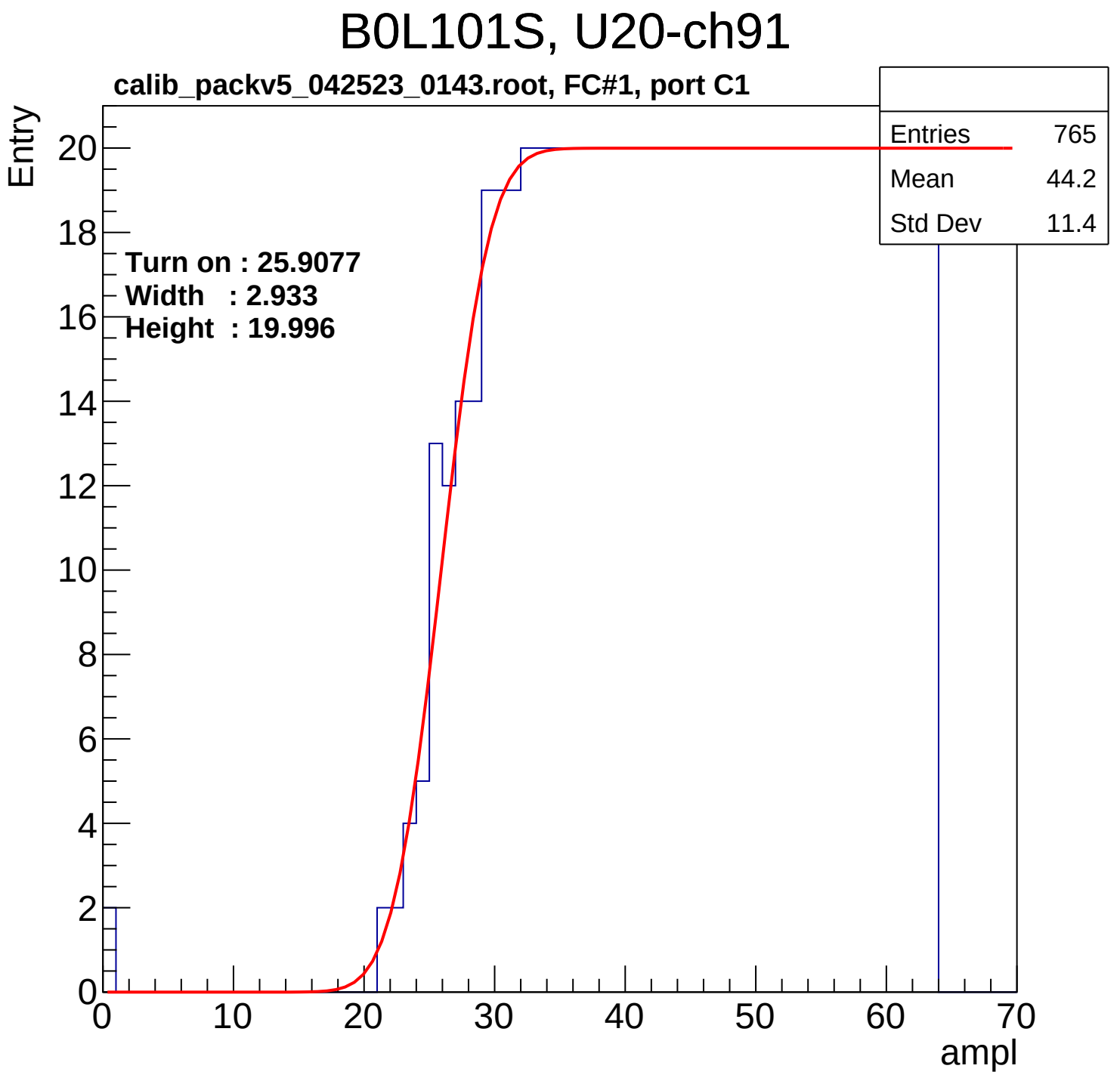
B0L101S, U20-ch91
calib_packv5_042523_0143.root, FC#1, port C1
Entries 765
Mean 44.2
Std Dev 11.4
Turn on : 25.9077
Width : 2.933
Height : 19.996
Entry
ampl
0
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6
8
10
12
14
16
18
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0
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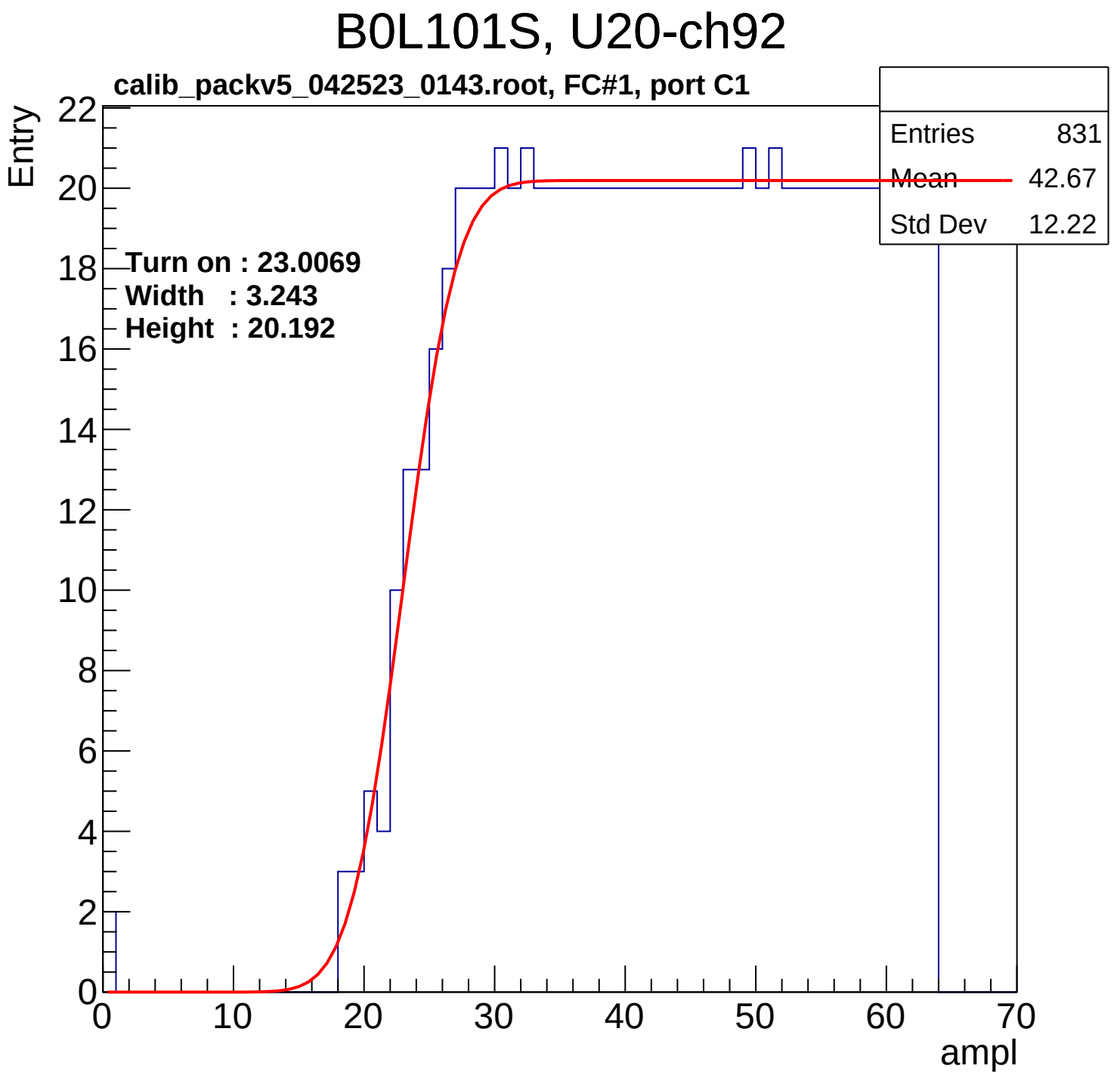
B0L101S, U20-ch92
calib_packv5_042523_0143.root, FC#1, port C1
Entries 831
Mean 42.67
Std Dev 12.22
Turn on : 23.0069
Width : 3.243
Height : 20.192
Entry
ampl
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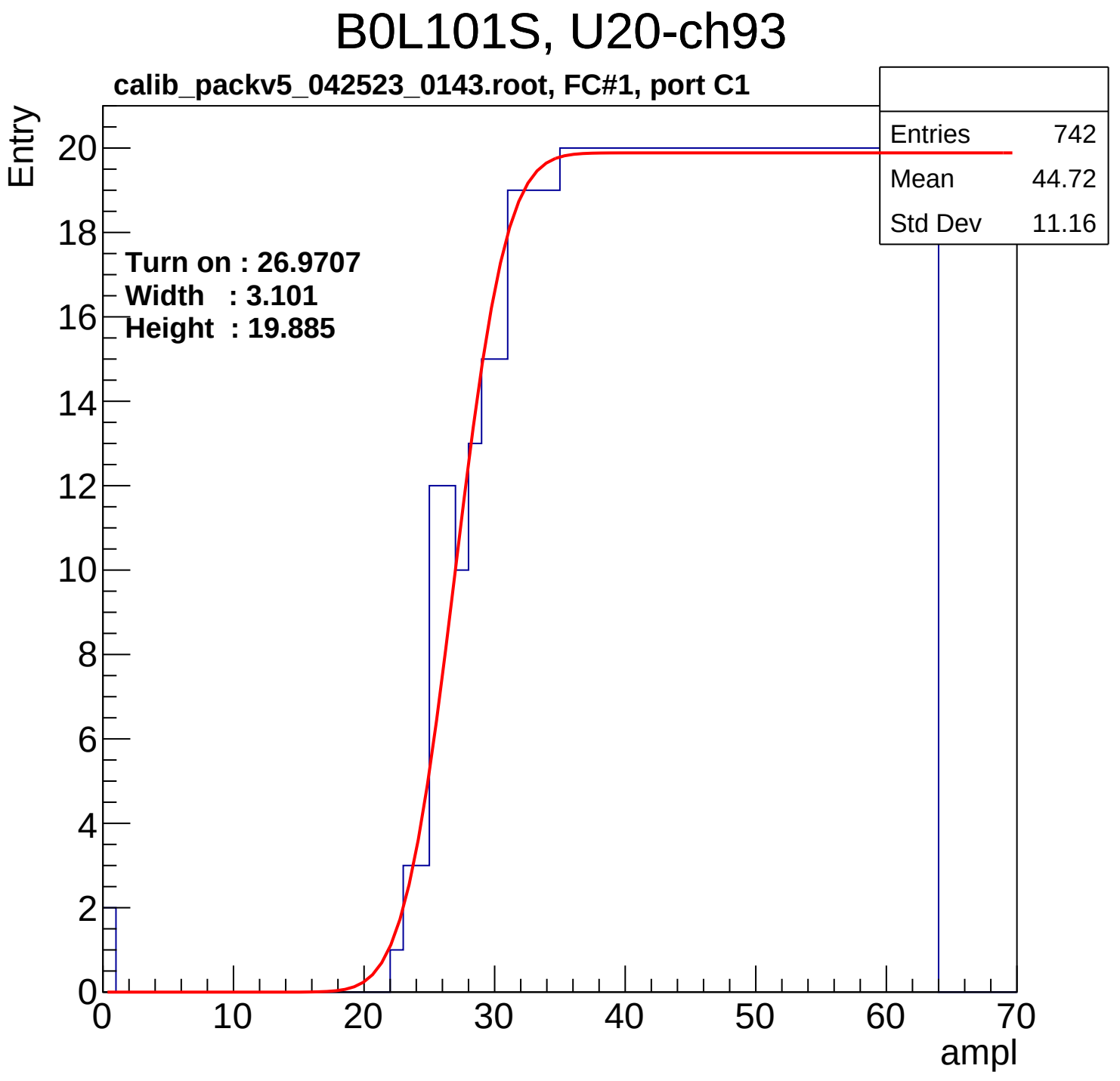
B0L101S, U20-ch93
calib_packv5_042523_0143.root, FC#1, port C1
Entries 742
Mean 44.72
Std Dev 11.16
Turn on : 26.9707
Width : 3.101
Height : 19.885
Entry
ampl
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8
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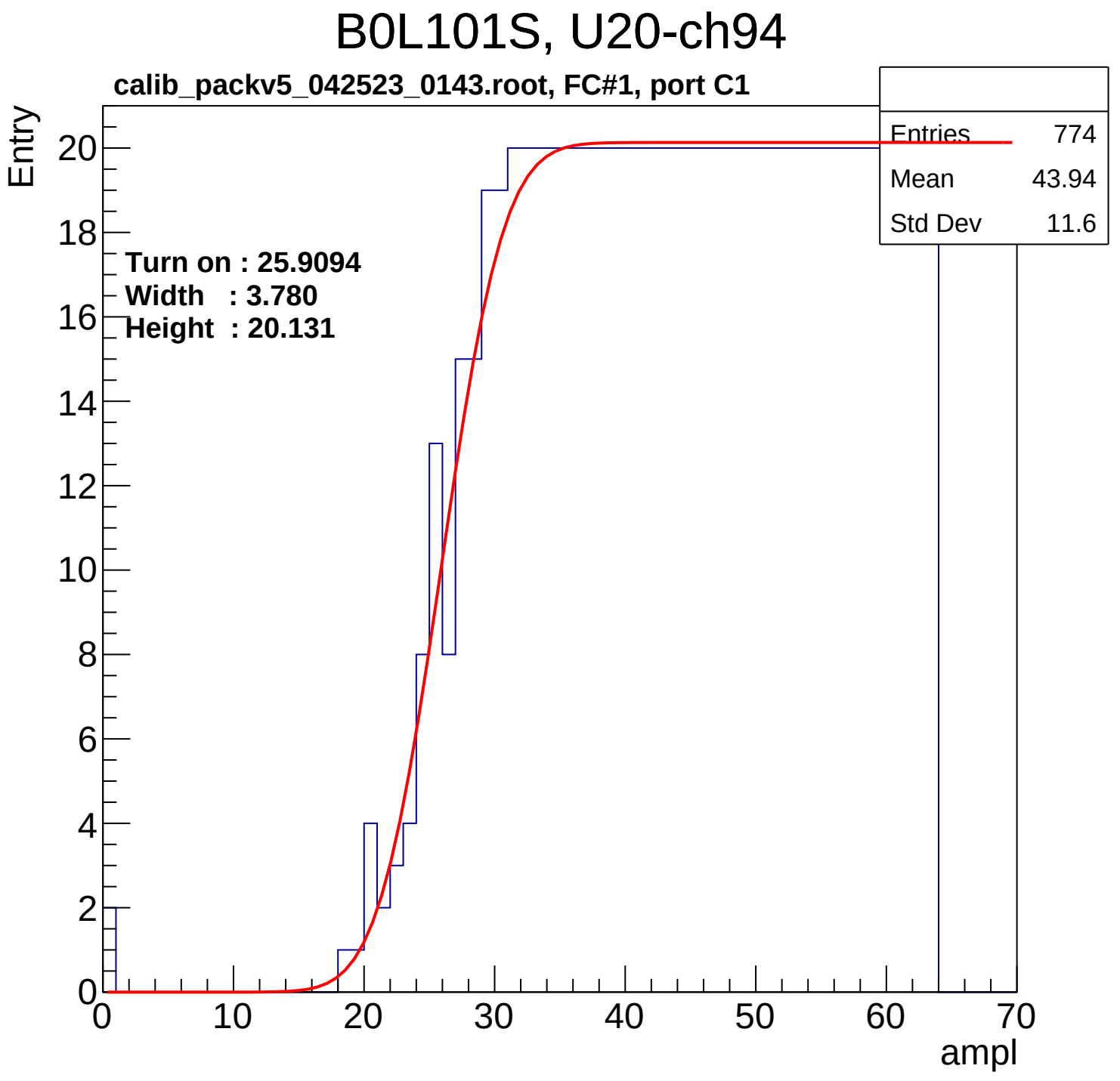
B0L101S, U20-ch94
calib_packv5_042523_0143.root, FC#1, port C1
Entries 774
Mean 43.94
Std Dev 11.6
Turn on : 25.9094
Width : 3.780
Height : 20.131
Entry
ampl
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6
8
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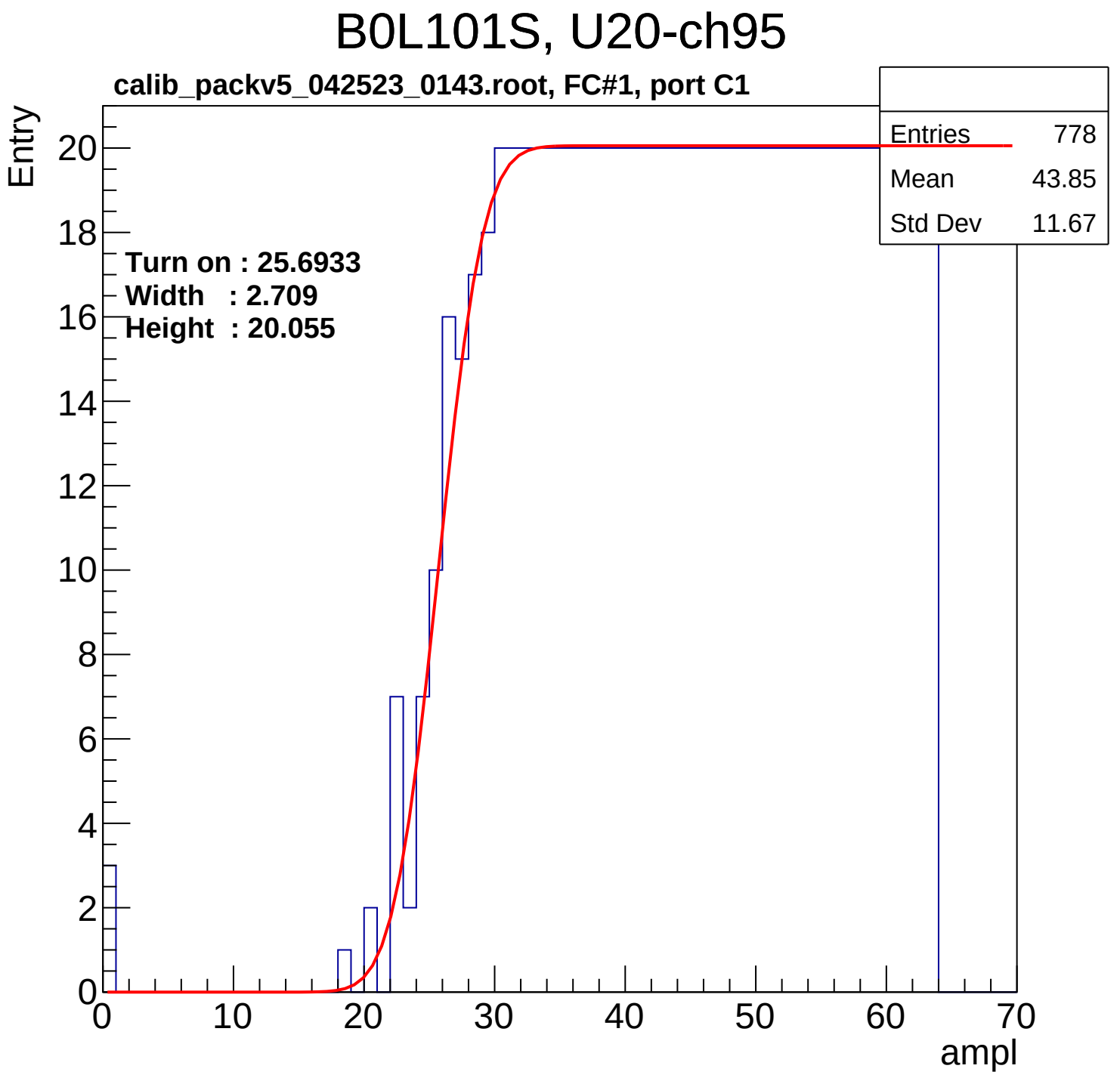
B0L101S, U20-ch95
calib_packv5_042523_0143.root, FC#1, port C1
Entries 778
Mean 43.85
Std Dev 11.67
Turn on : 25.6933
Width : 2.709
Height : 20.055
Entry
ampl
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6
8
10
12
14
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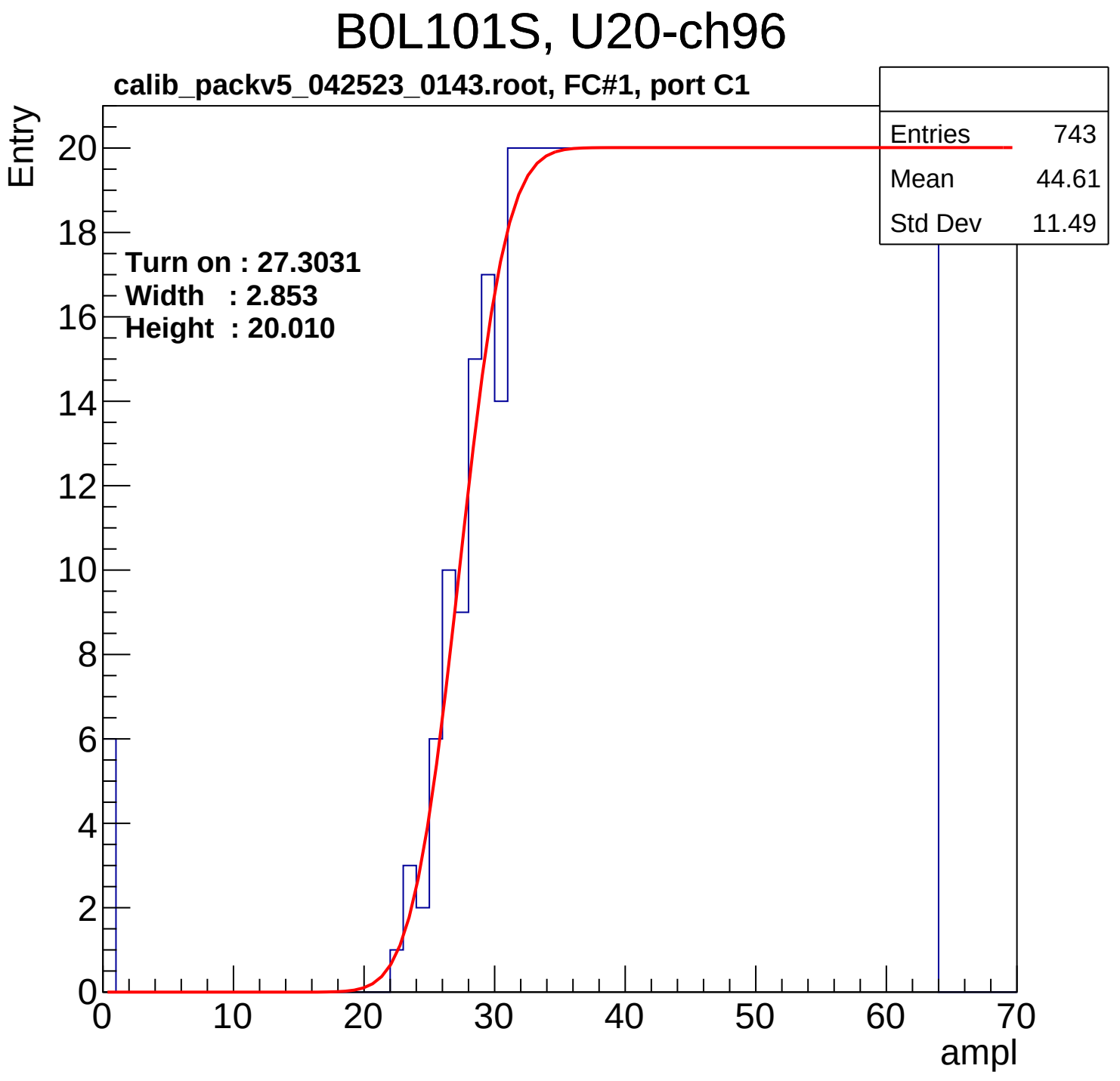
B0L101S, U20-ch96
calib_packv5_042523_0143.root, FC#1, port C1
Entries 743
Mean 44.61
Std Dev 11.49
Turn on : 27.3031
Width : 2.853
Height : 20.010
Entry
ampl
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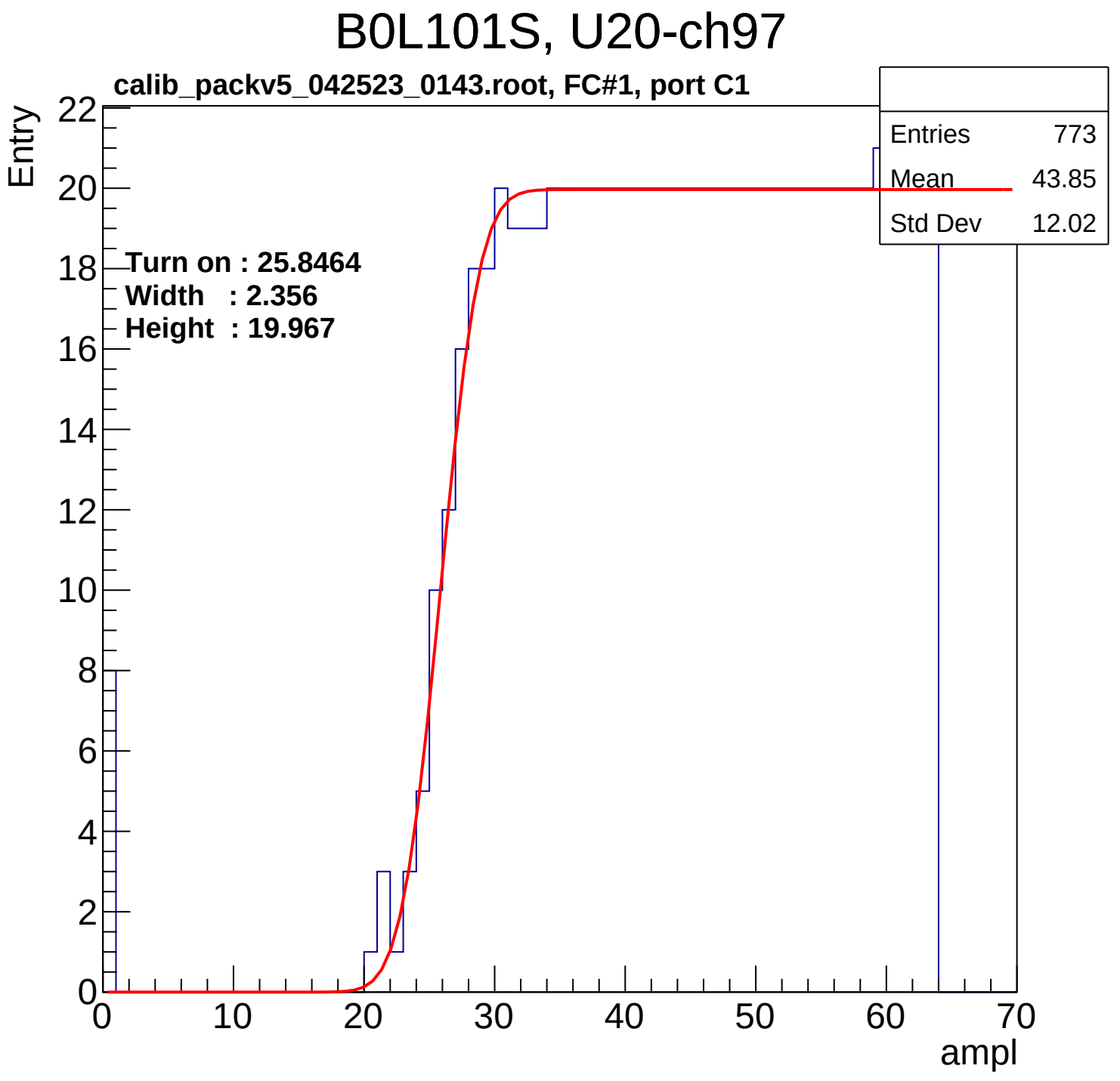
B0L101S, U20-ch97
calib_packv5_042523_0143.root, FC#1, port C1
Entries 773
Mean 43.85
Std Dev 12.02
Turn on : 25.8464
Width : 2.356
Height : 19.967
Entry
ampl
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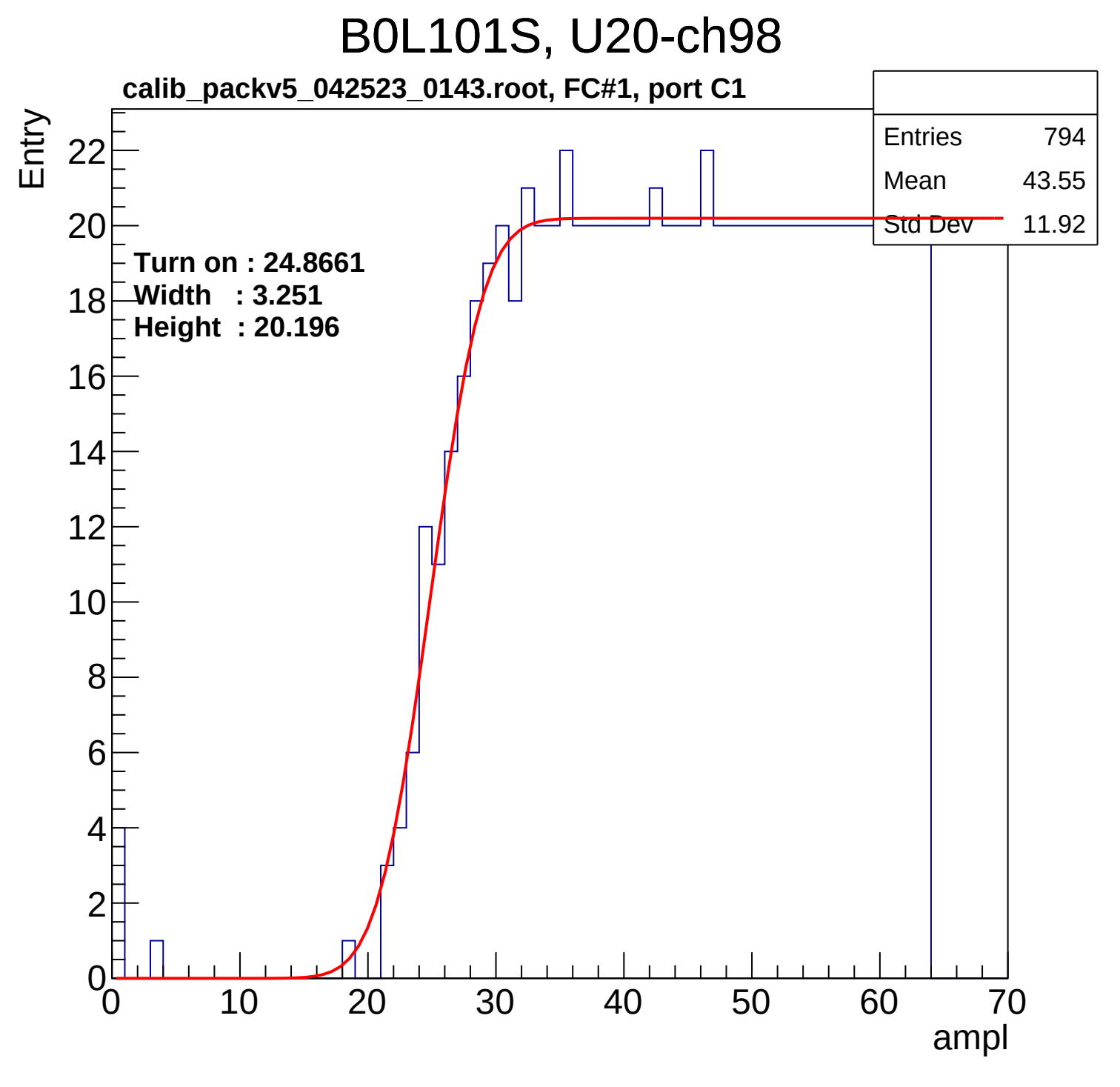
B0L101S, U20-ch98
calib_packv5_042523_0143.root, FC#1, port C1
Entries 794
Mean 43.55
Std Dev 11.92
Turn on : 24.8661
Width : 3.251
Height : 20.196
Entry
ampl
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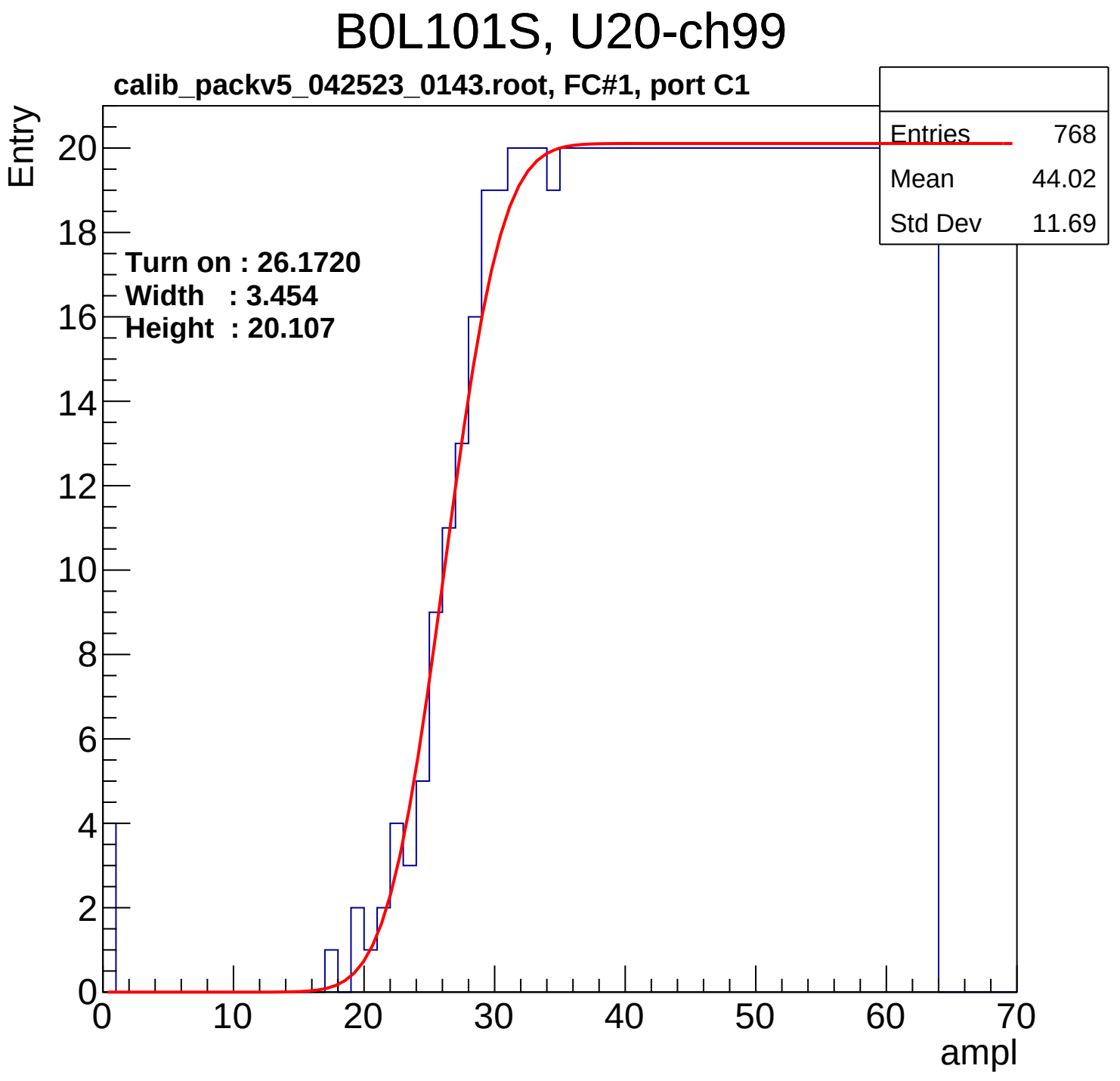
B0L101S, U20-ch99
calib_packv5_042523_0143.root, FC#1, port C1
Entries 768
Mean 44.02
Std Dev 11.69
Turn on : 26.1720
Width : 3.454
Height : 20.107
Entry
ampl
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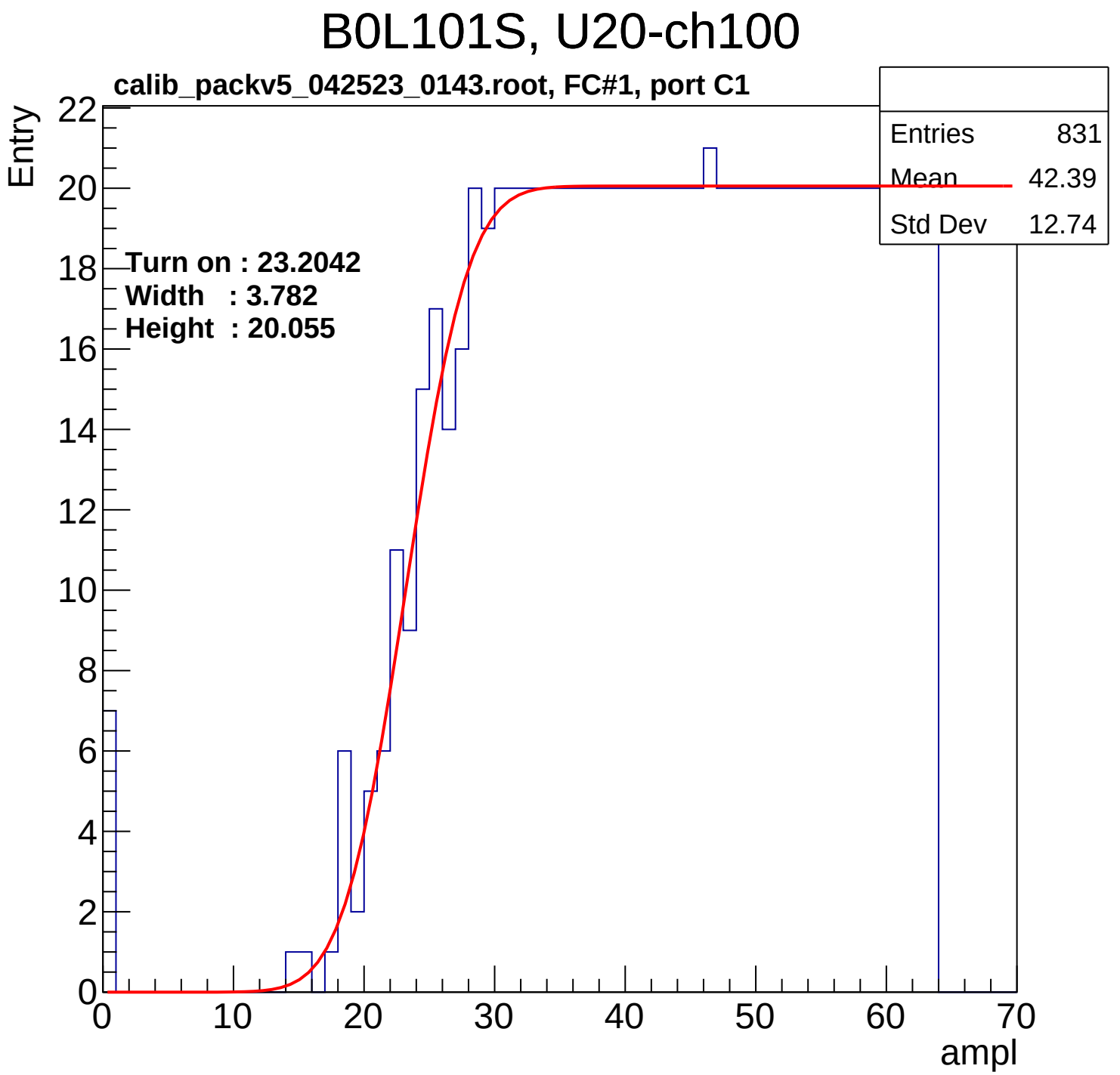
B0L101S, U20-ch100
calib_packv5_042523_0143.root, FC#1, port C1
Entries 831
Mean 42.39
Std Dev 12.74
Turn on : 23.2042
Width : 3.782
Height : 20.055
Entry
ampl
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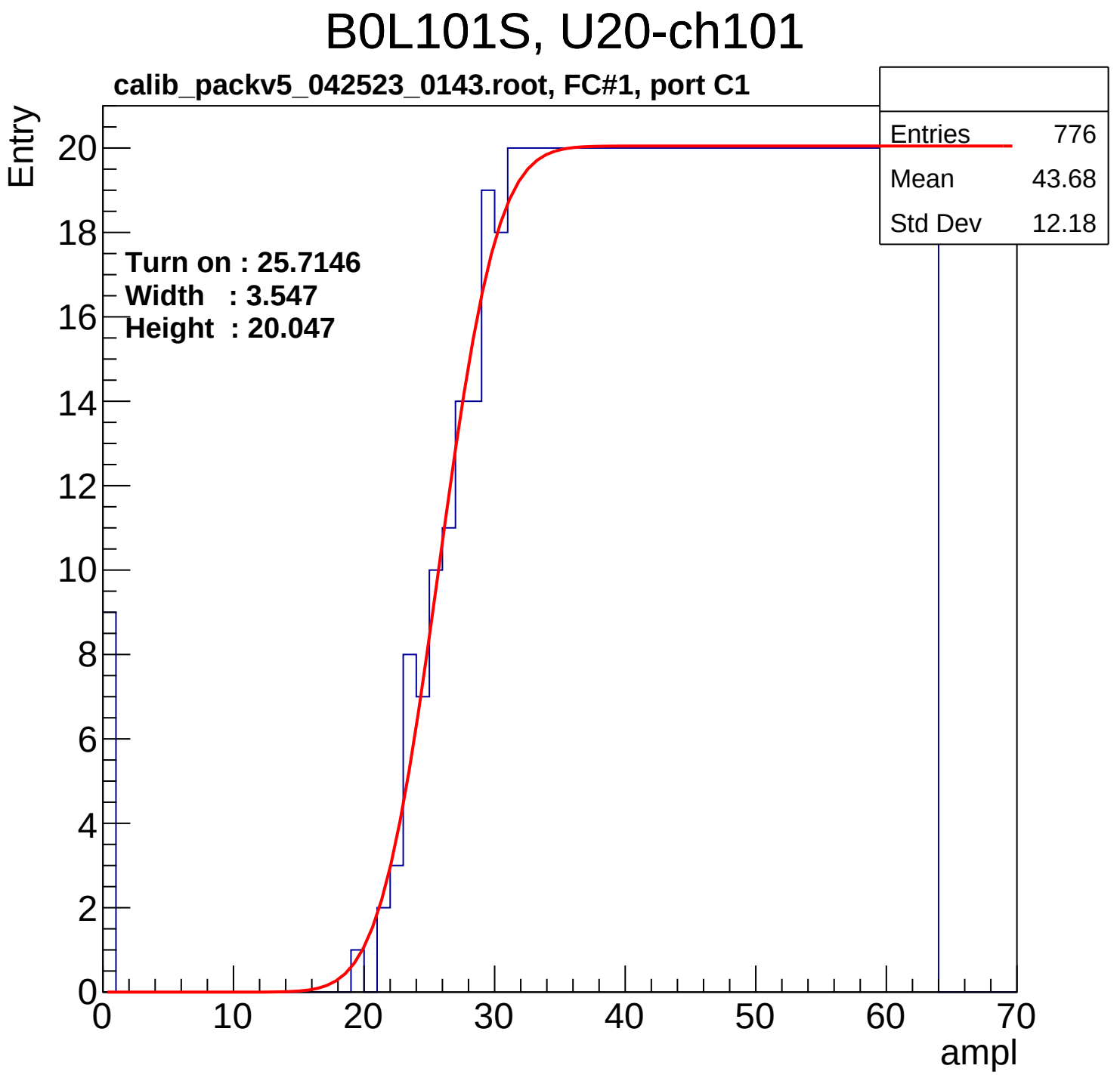
B0L101S, U20-ch101
calib_packv5_042523_0143.root, FC#1, port C1
Entries 776
Mean 43.68
Std Dev 12.18
Turn on : 25.7146
Width : 3.547
Height : 20.047
Entry
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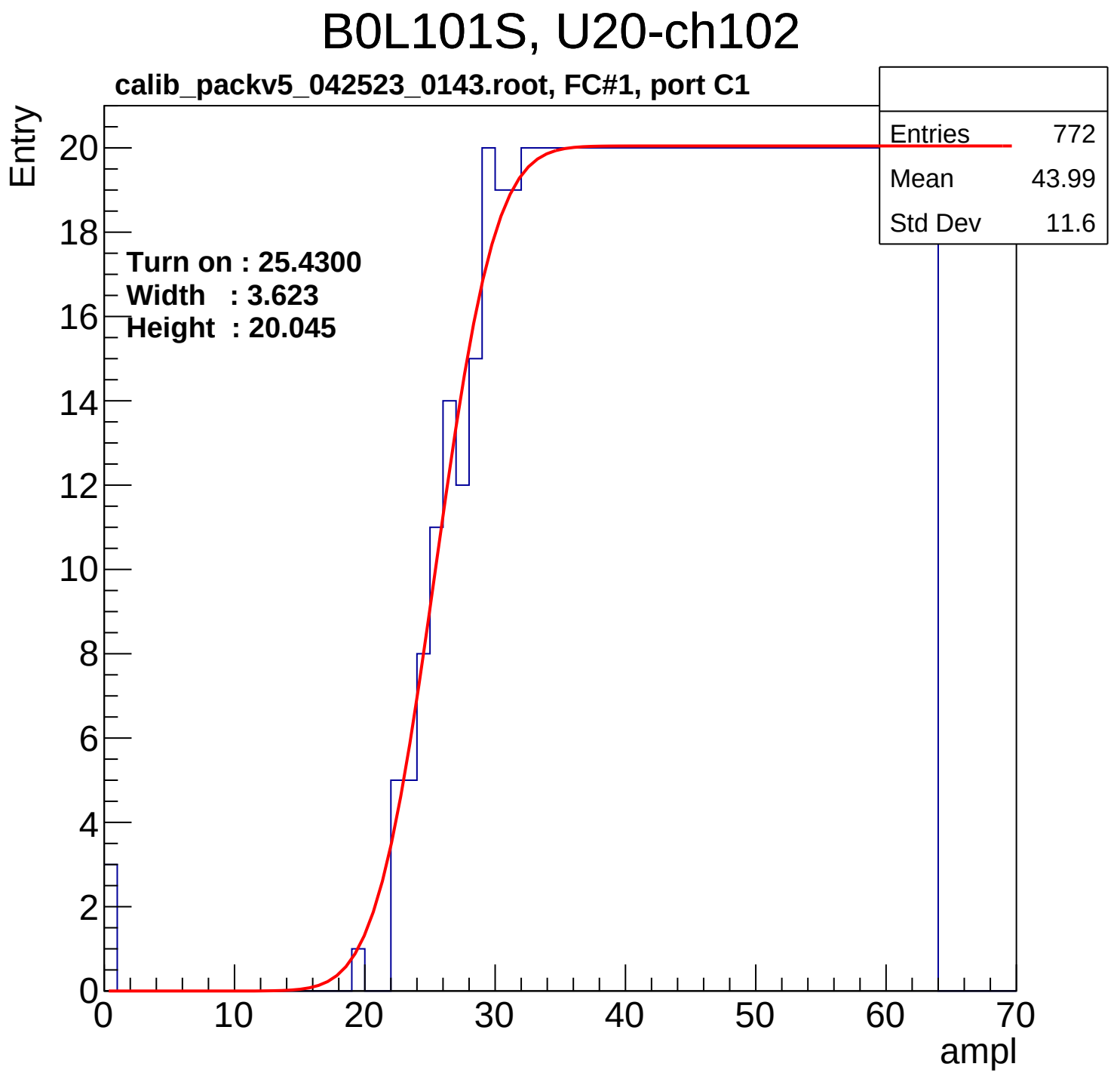
B0L101S, U20-ch102
calib_packv5_042523_0143.root, FC#1, port C1
Entries 772
Mean 43.99
Std Dev 11.6
Turn on : 25.4300
Width : 3.623
Height : 20.045
Entry
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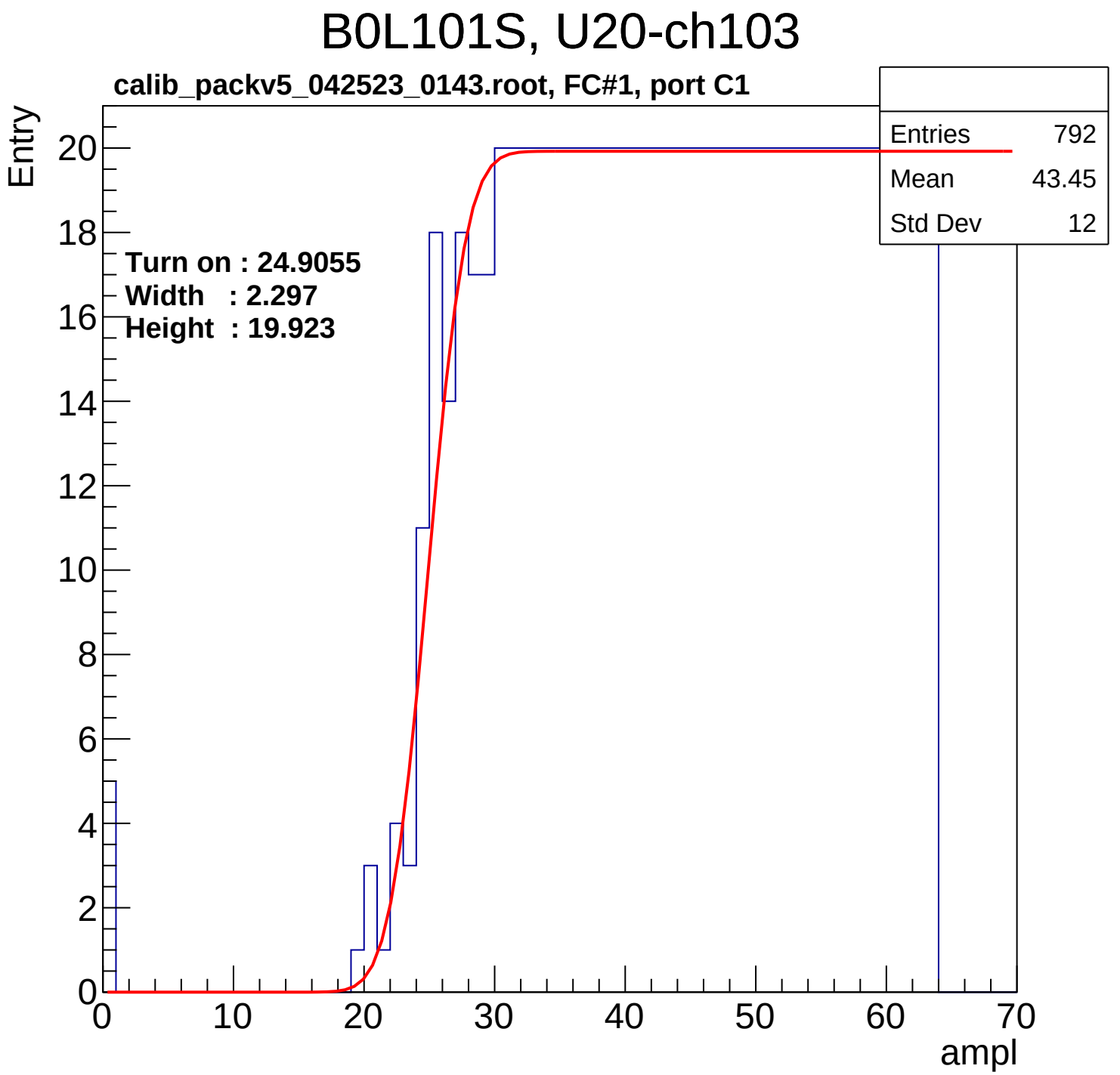
B0L101S, U20-ch103
calib_packv5_042523_0143.root, FC#1, port C1
Entries 792
Mean 43.45
Std Dev 12
Turn on : 24.9055
Width : 2.297
Height : 19.923
Entry
ampl
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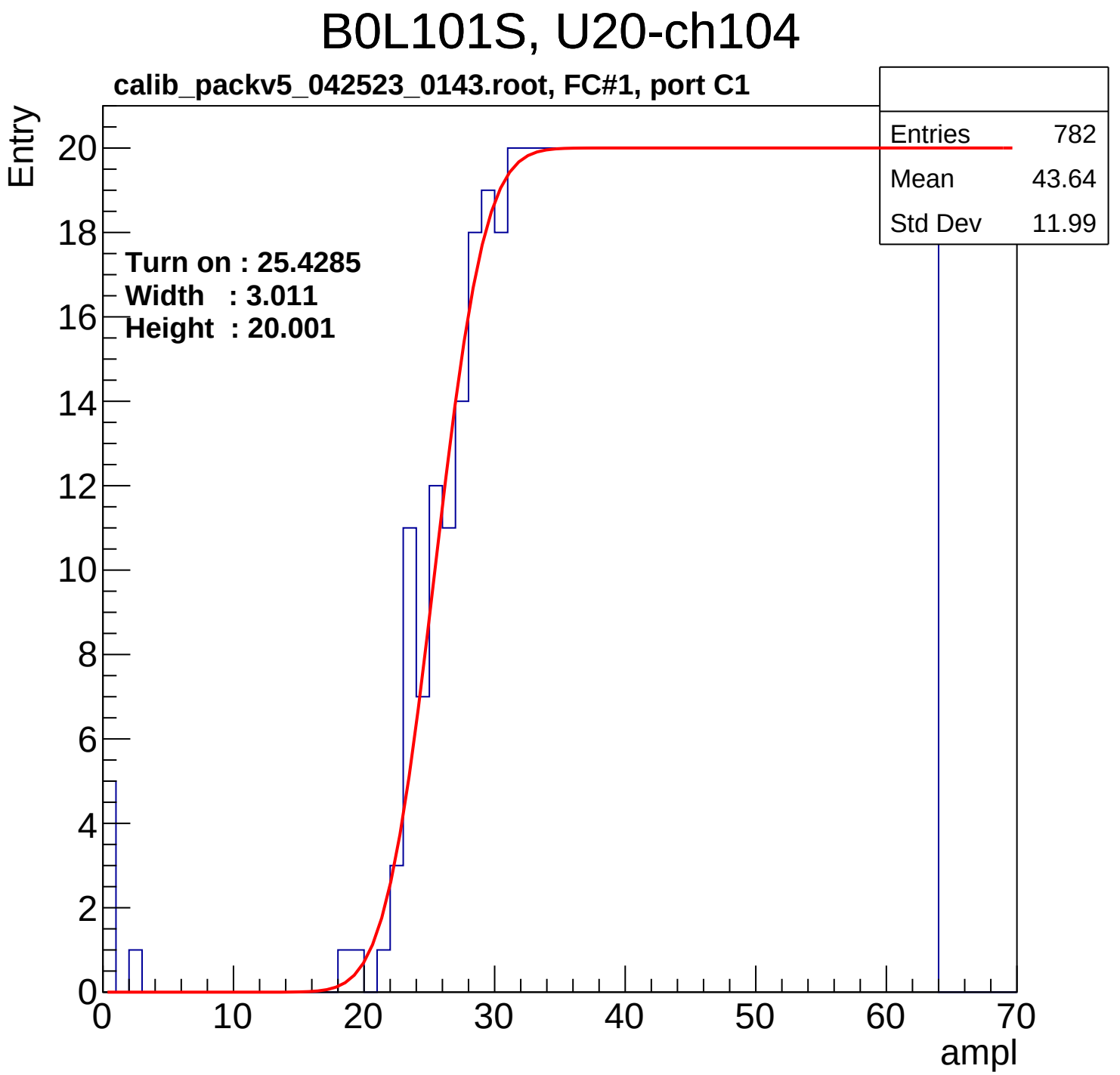
B0L101S, U20-ch104
calib_packv5_042523_0143.root, FC#1, port C1
Entries 782
Mean 43.64
Std Dev 11.99
Turn on : 25.4285
Width : 3.011
Height : 20.001
Entry
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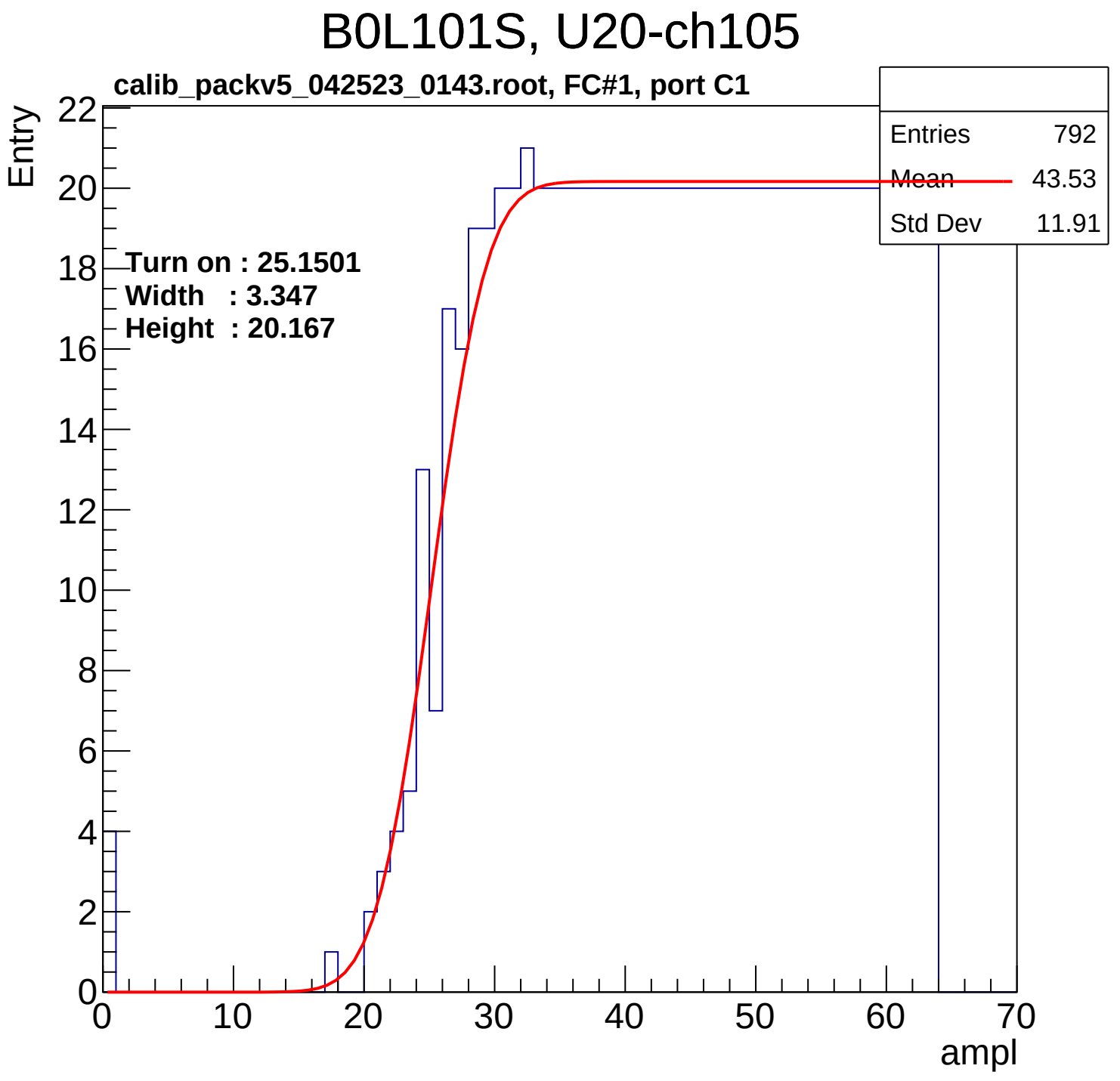
B0L101S, U20-ch105
calib_packv5_042523_0143.root, FC#1, port C1
Entries 792
Mean 43.53
Std Dev 11.91
Turn on : 25.1501
Width : 3.347
Height : 20.167
Entry
ampl
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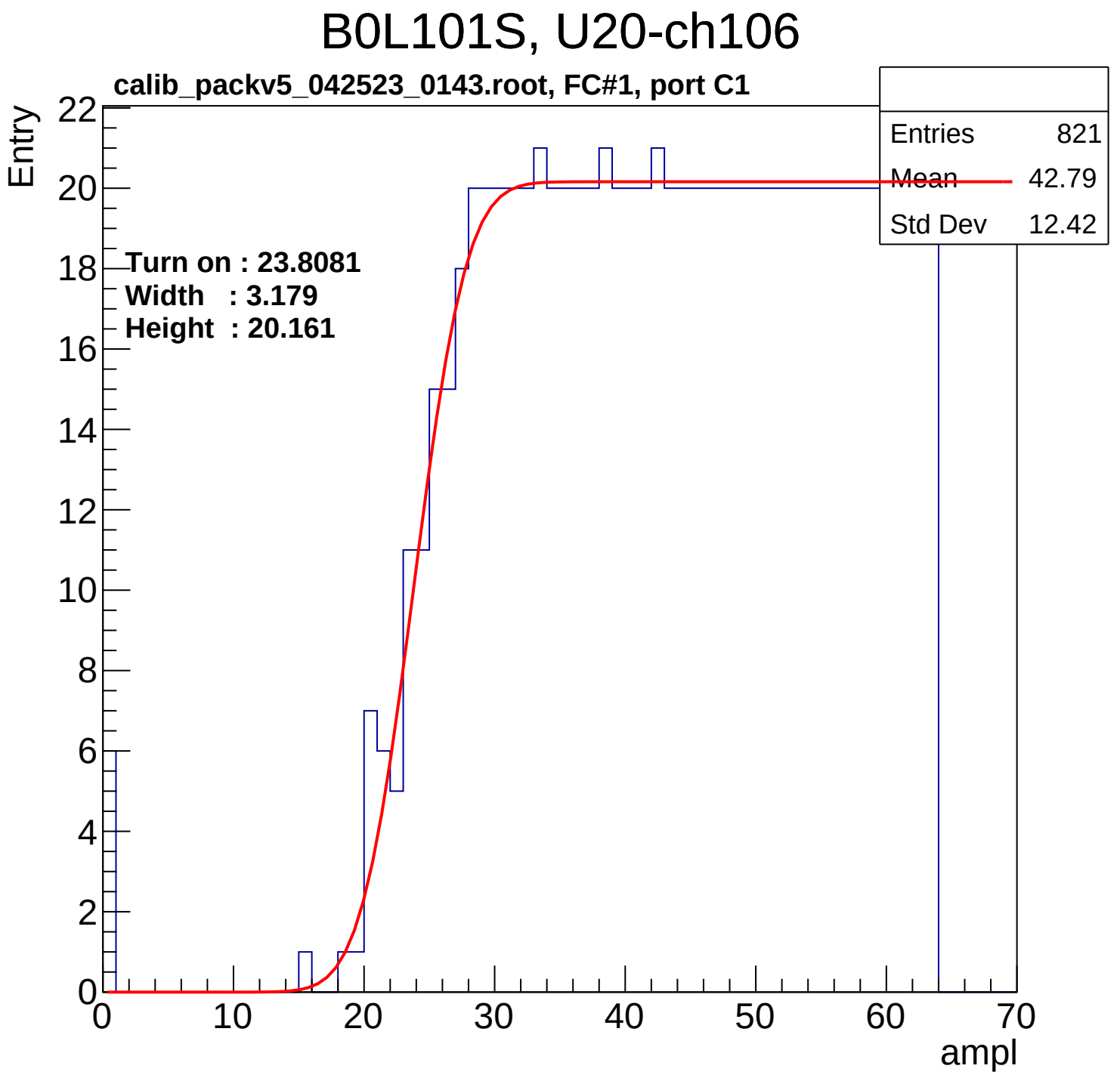
B0L101S, U20-ch106
calib_packv5_042523_0143.root, FC#1, port C1
Entries 821
Mean 42.79
Std Dev 12.42
Turn on : 23.8081
Width : 3.179
Height : 20.161
Entry
ampl
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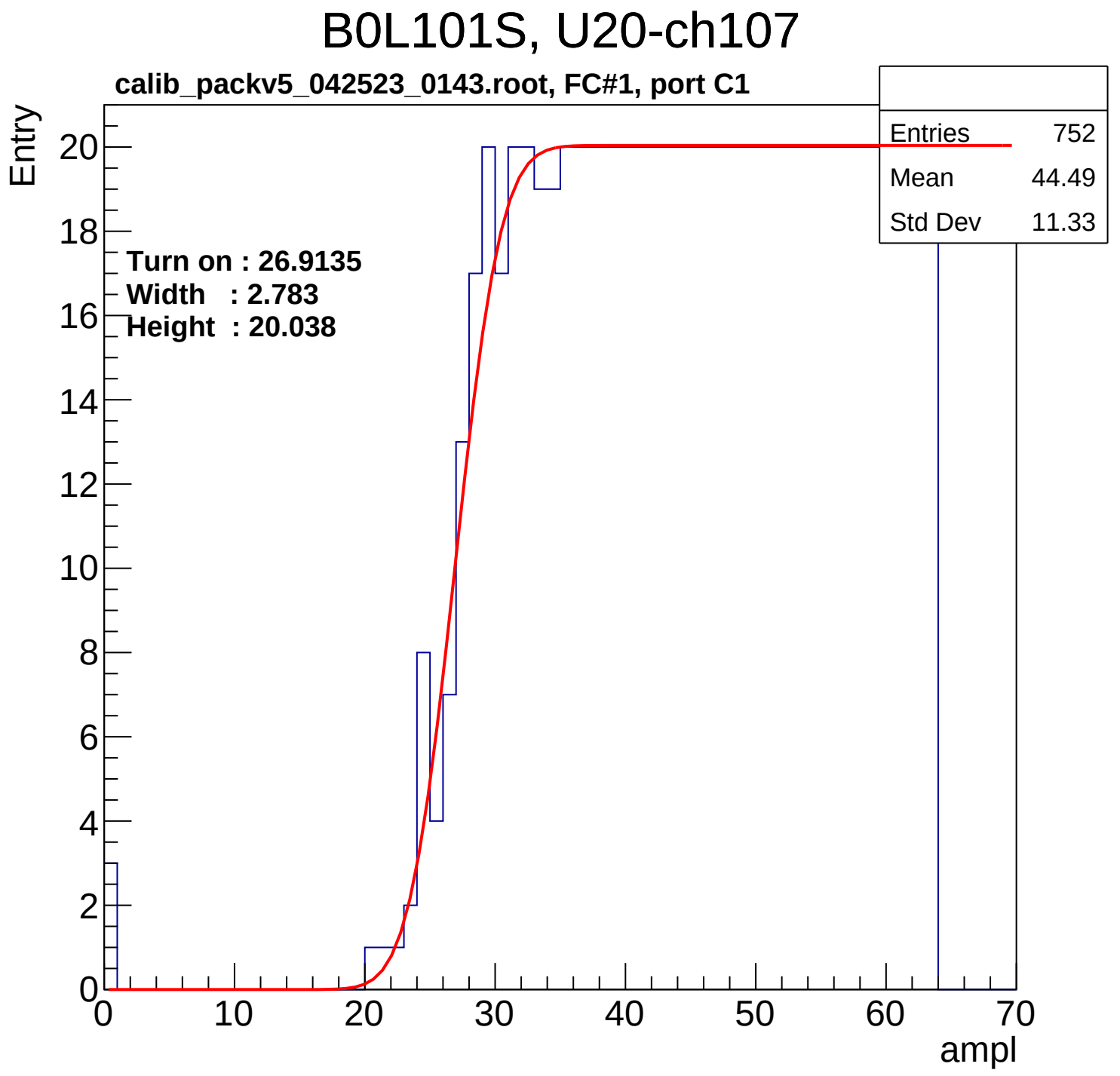
B0L101S, U20-ch107
calib_packv5_042523_0143.root, FC#1, port C1
Entries 752
Mean 44.49
Std Dev 11.33
Turn on : 26.9135
Width : 2.783
Height : 20.038
Entry
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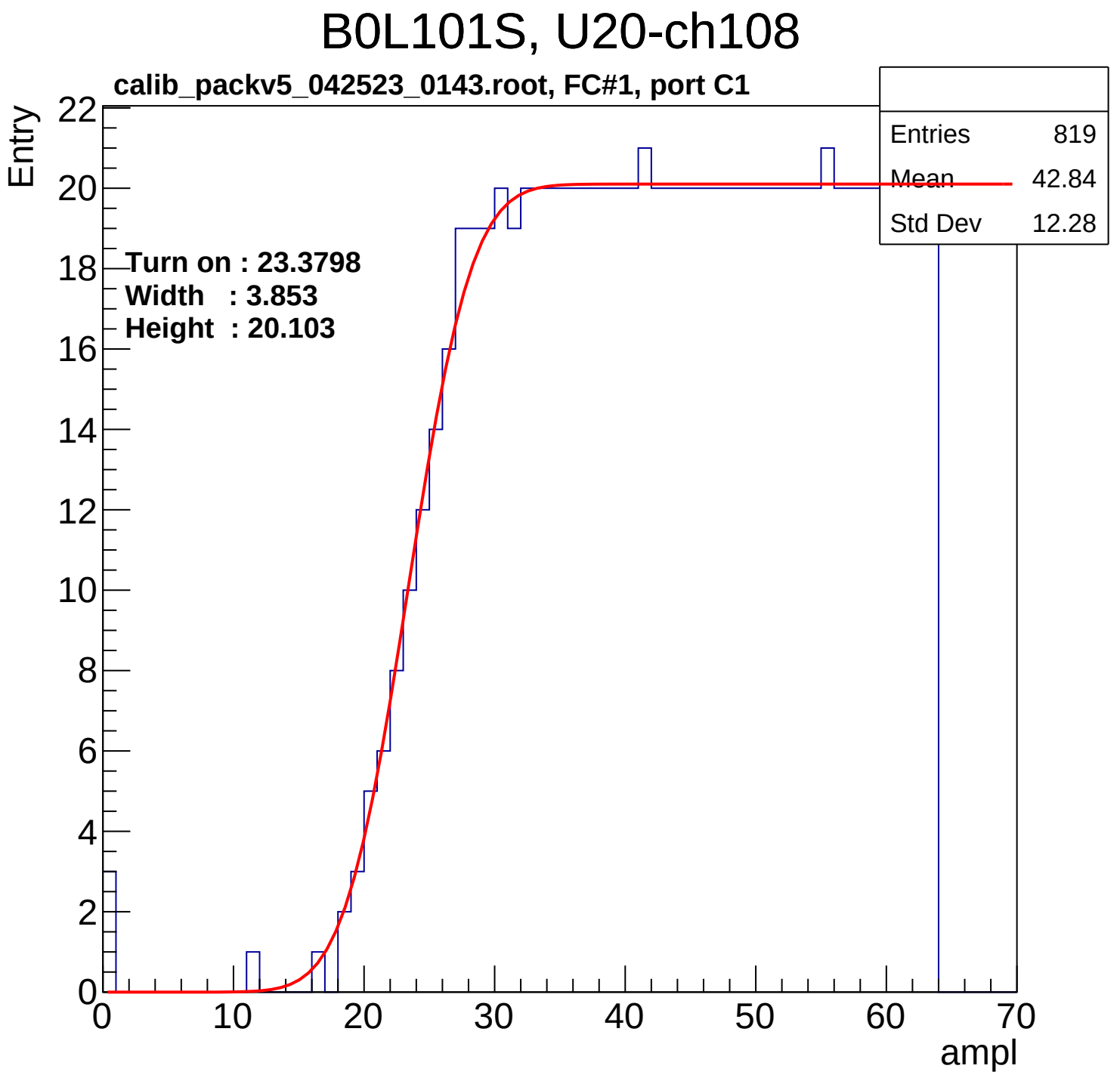
B0L101S, U20-ch108
calib_packv5_042523_0143.root, FC#1, port C1
Entries 819
Mean 42.84
Std Dev 12.28
Turn on : 23.3798
Width : 3.853
Height : 20.103
Entry
ampl
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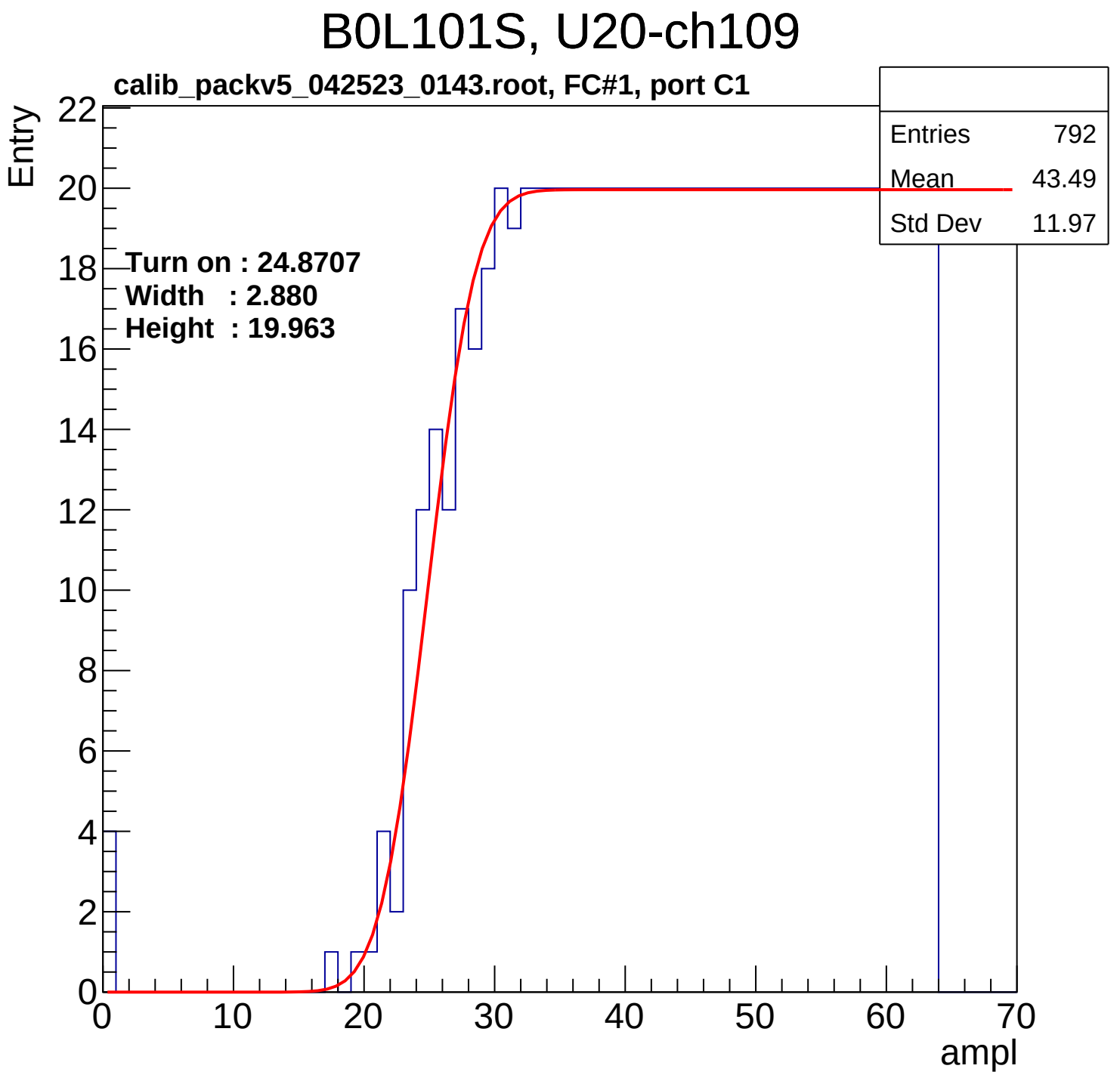
B0L101S, U20-ch109
calib_packv5_042523_0143.root, FC#1, port C1
Entries 792
Mean 43.49
Std Dev 11.97
Turn on : 24.8707
Width : 2.880
Height : 19.963
Entry
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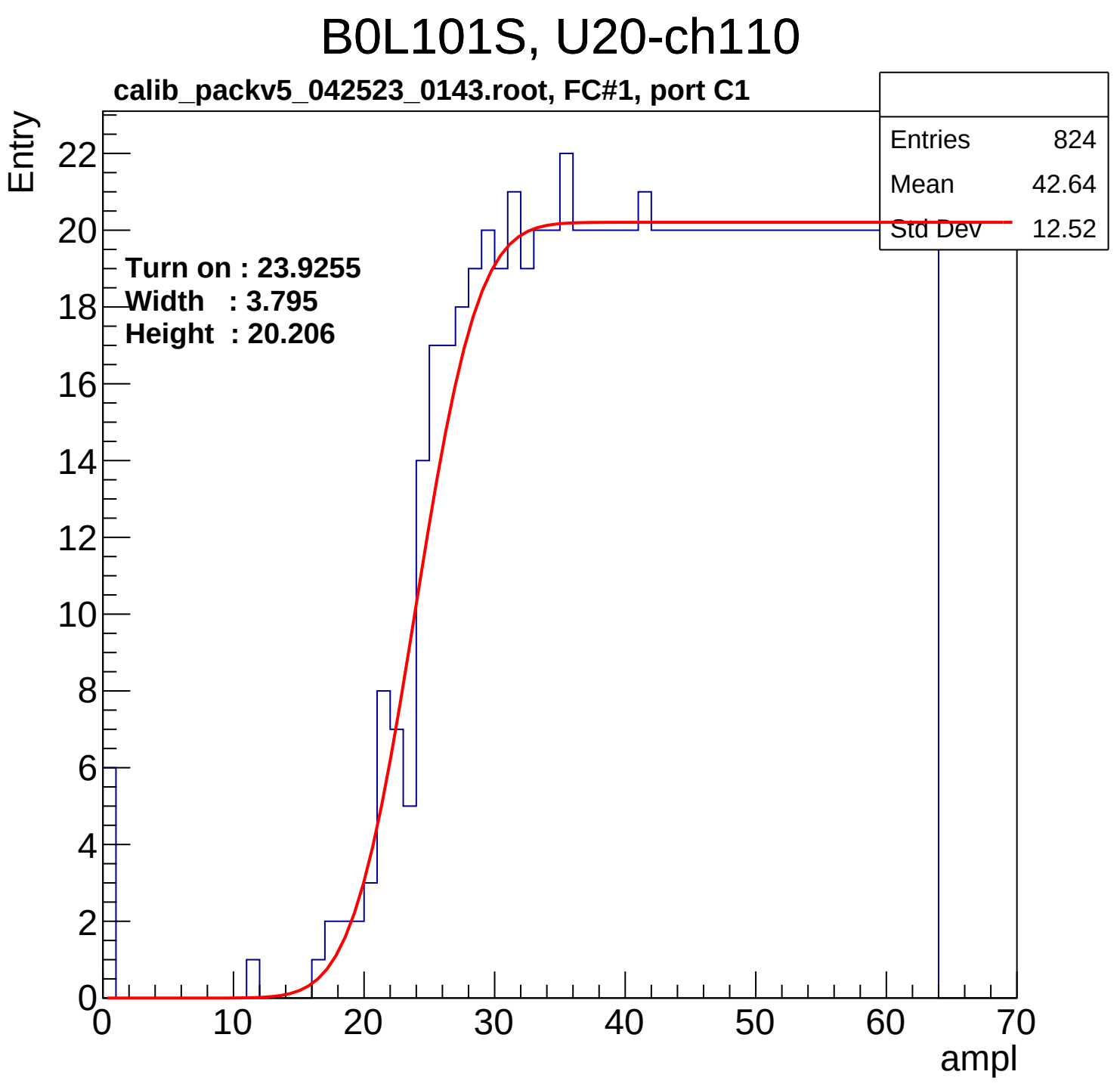
B0L101S, U20-ch110
calib_packv5_042523_0143.root, FC#1, port C1
Entries 824
Mean 42.64
Std Dev 12.52
Turn on : 23.9255
Width : 3.795
Height : 20.206
Entry
ampl
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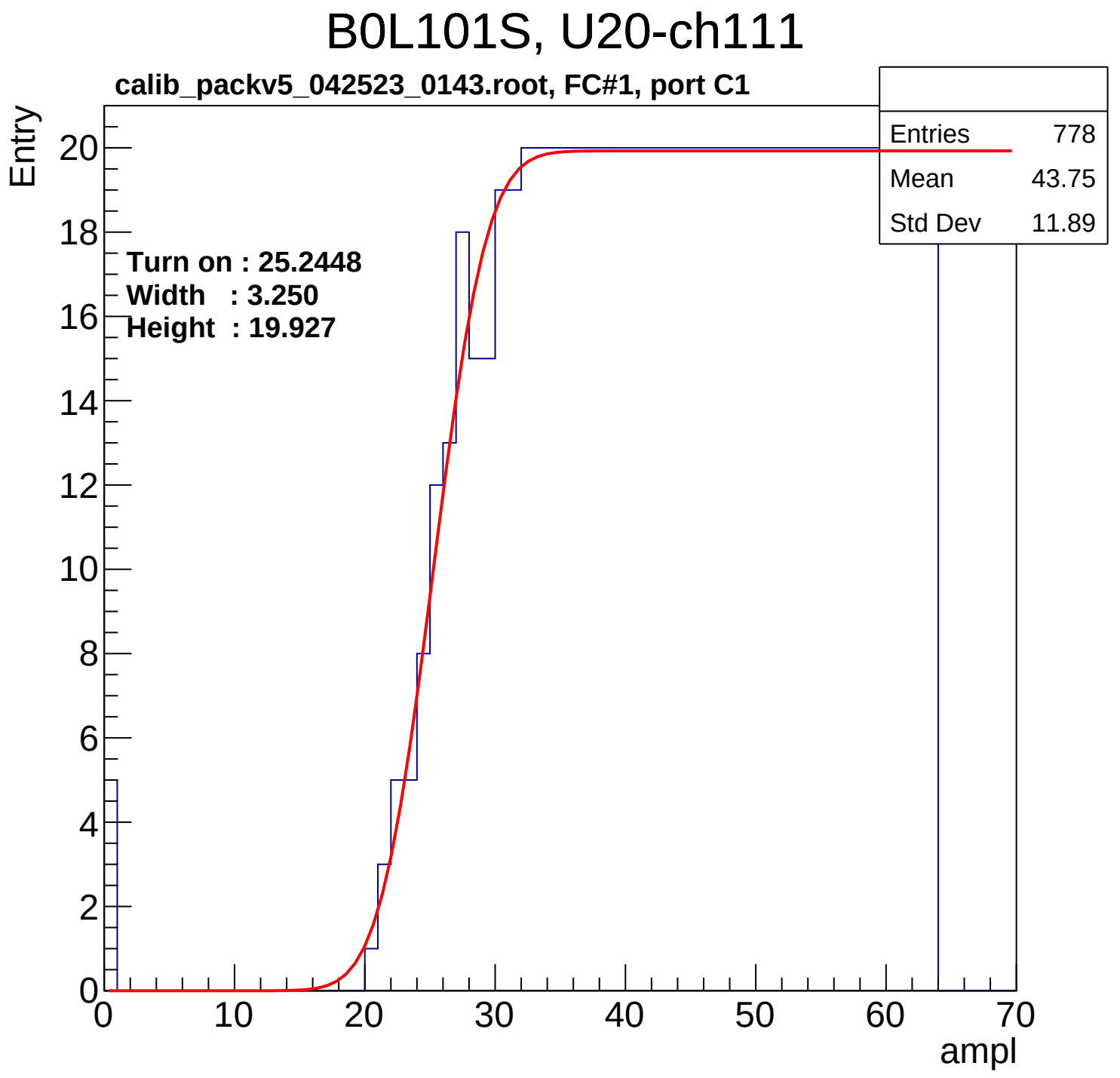
B0L101S, U20-ch111
calib_packv5_042523_0143.root, FC#1, port C1
Entries 778
Mean 43.75
Std Dev 11.89
Turn on : 25.2448
Width : 3.250
Height : 19.927
Entry
ampl
0
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4
6
8
10
12
14
16
18
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10
20
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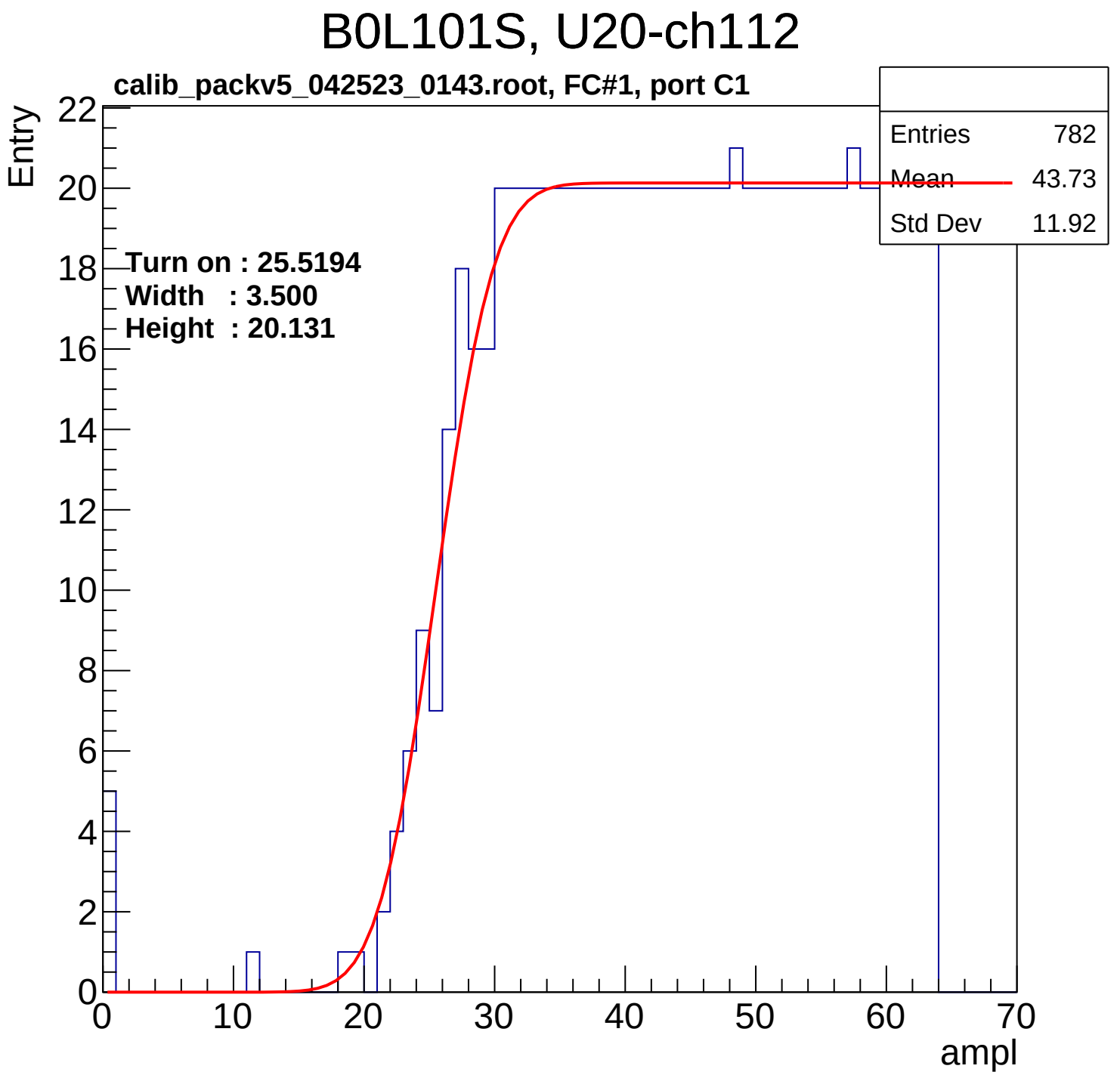
B0L101S, U20-ch112
calib_packv5_042523_0143.root, FC#1, port C1
Entries 782
Mean 43.73
Std Dev 11.92
Turn on : 25.5194
Width : 3.500
Height : 20.131
Entry
ampl
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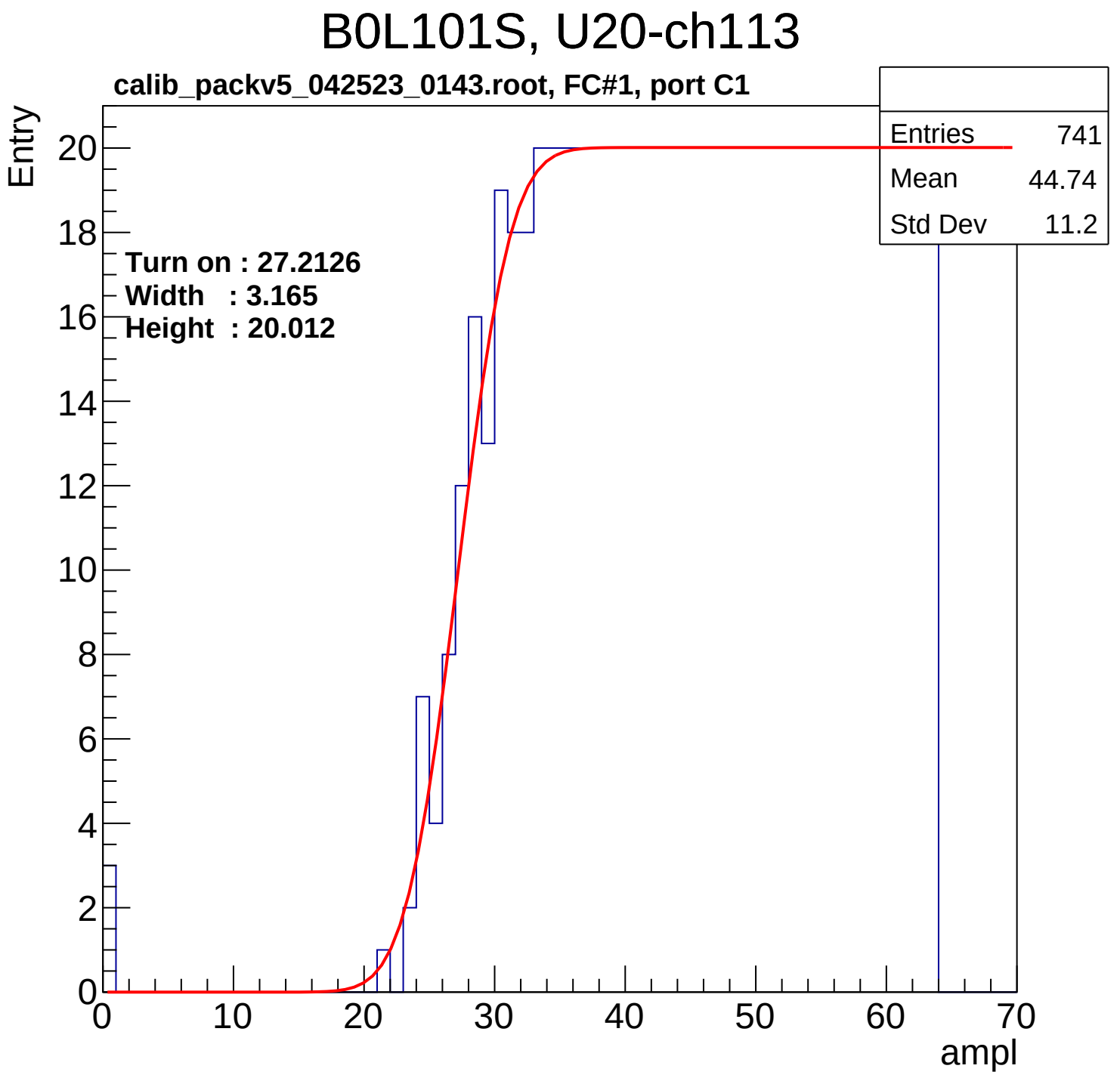
B0L101S, U20-ch113
calib_packv5_042523_0143.root, FC#1, port C1
Entries 741
Mean 44.74
Std Dev 11.2
Turn on : 27.2126
Width : 3.165
Height : 20.012
Entry
ampl
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6
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14
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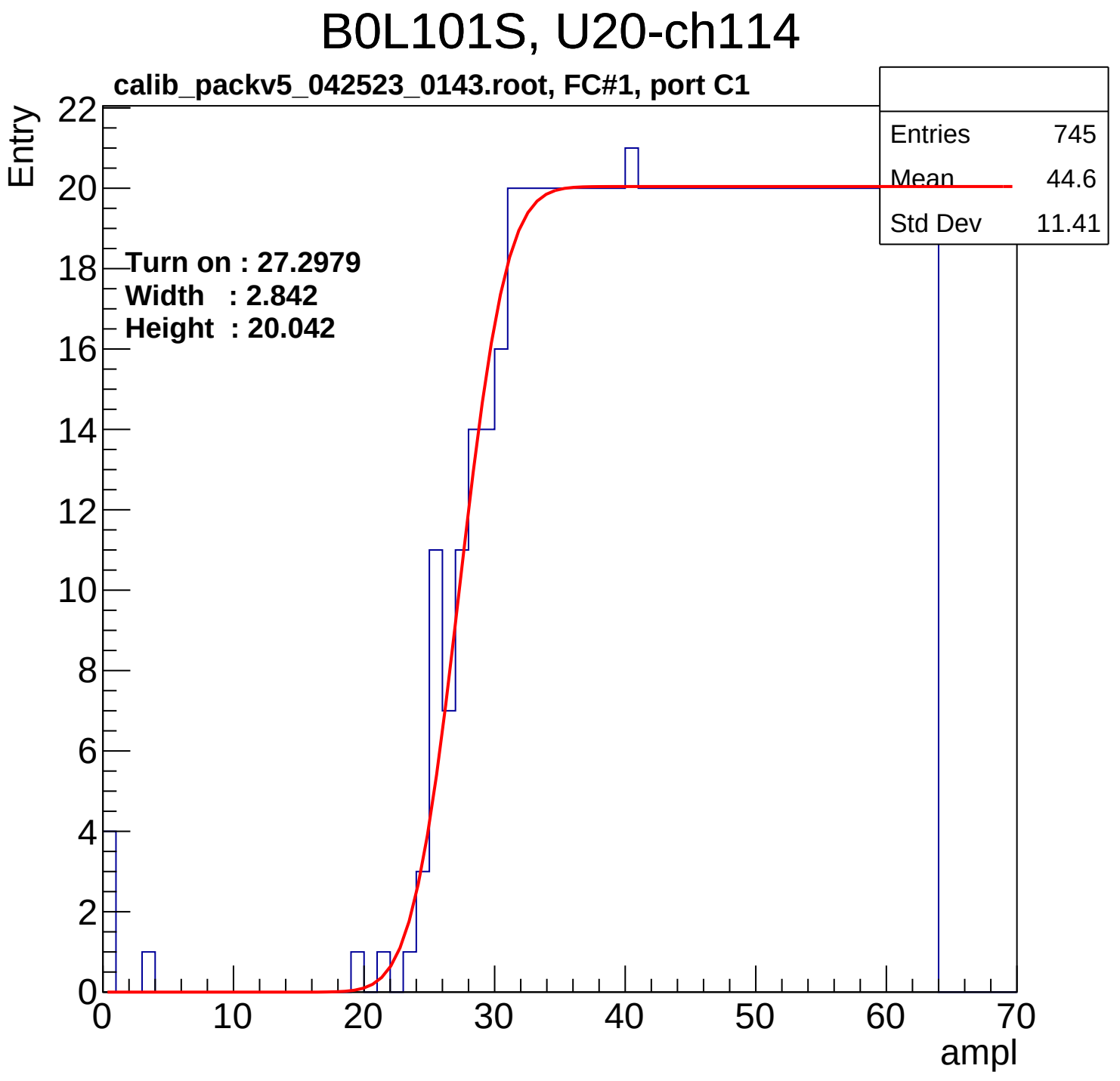
B0L101S, U20-ch114
calib_packv5_042523_0143.root, FC#1, port C1
Entries 745
Mean 44.6
Std Dev 11.41
Turn on : 27.2979
Width : 2.842
Height : 20.042
Entry
ampl
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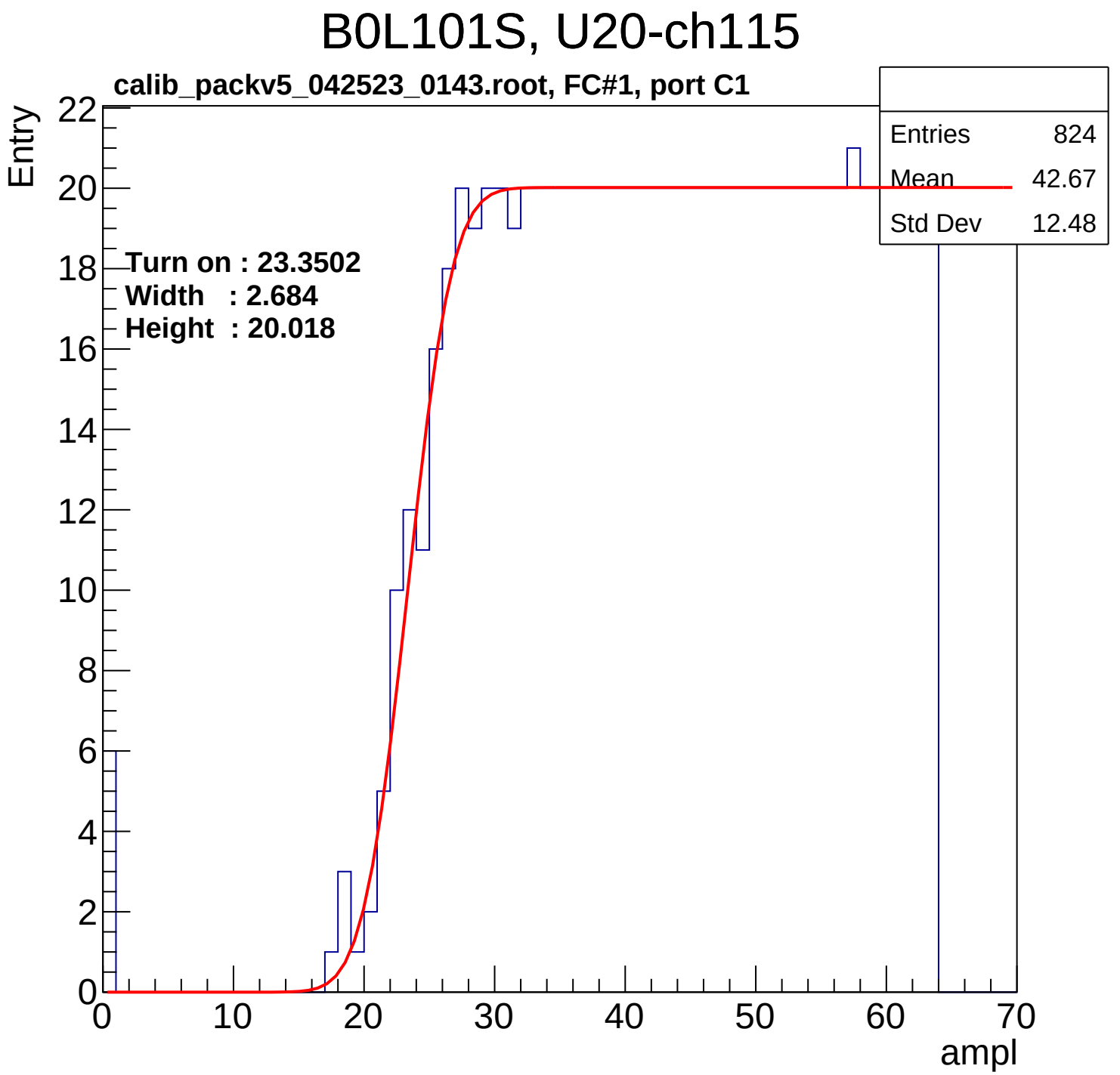
B0L101S, U20-ch115
calib_packv5_042523_0143.root, FC#1, port C1
Entries 824
Mean 42.67
Std Dev 12.48
Turn on : 23.3502
Width : 2.684
Height : 20.018
Entry
ampl
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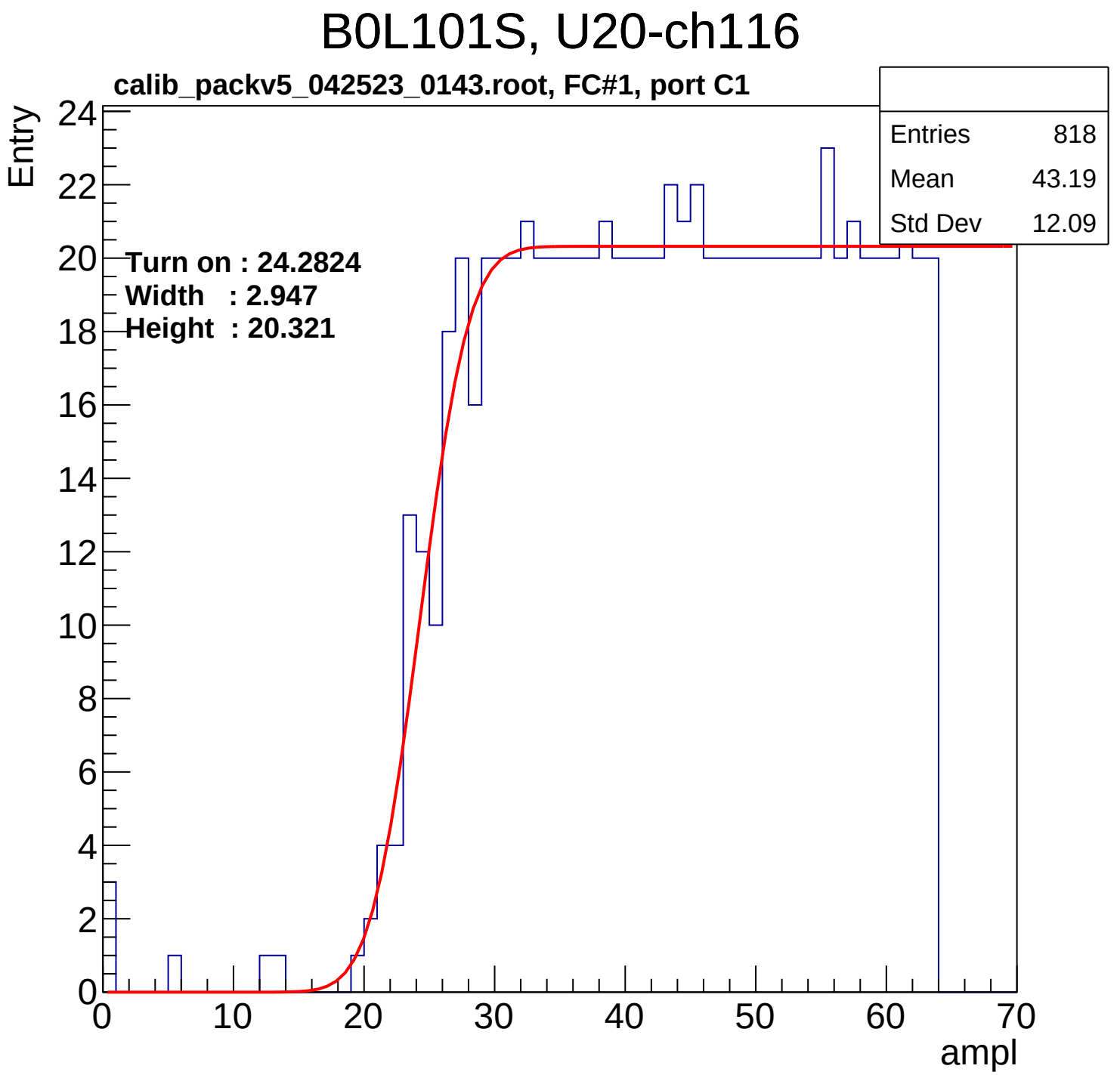
B0L101S, U20-ch116
calib_packv5_042523_0143.root, FC#1, port C1
Entries 818
Mean 43.19
Std Dev 12.09
Turn on : 24.2824
Width : 2.947
Height : 20.321
Entry
ampl
0
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10
12
14
16
18
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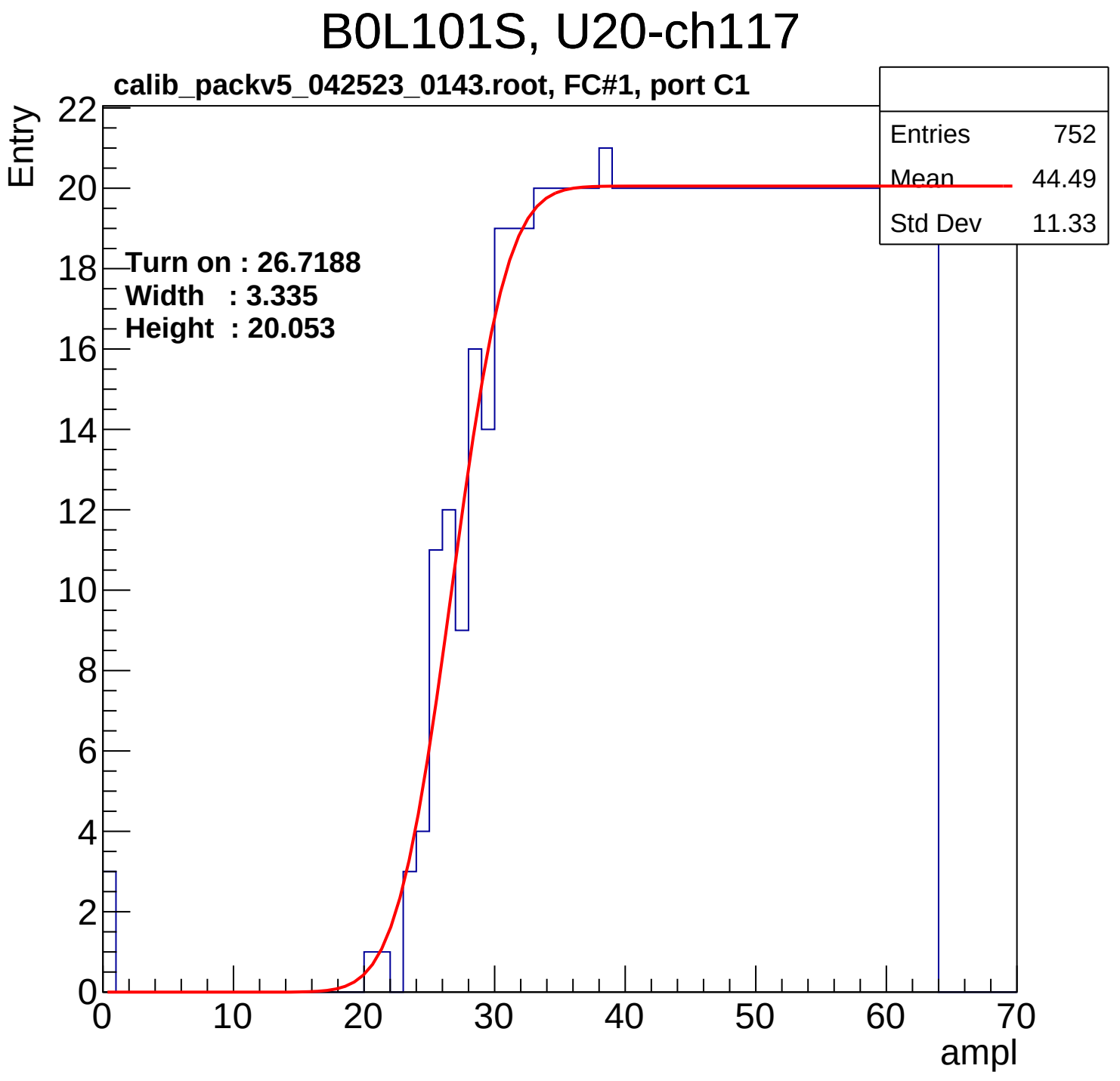
B0L101S, U20-ch117
calib_packv5_042523_0143.root, FC#1, port C1
Entries 752
Mean 44.49
Std Dev 11.33
Turn on : 26.7188
Width : 3.335
Height : 20.053
Entry
ampl
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8
10
12
14
16
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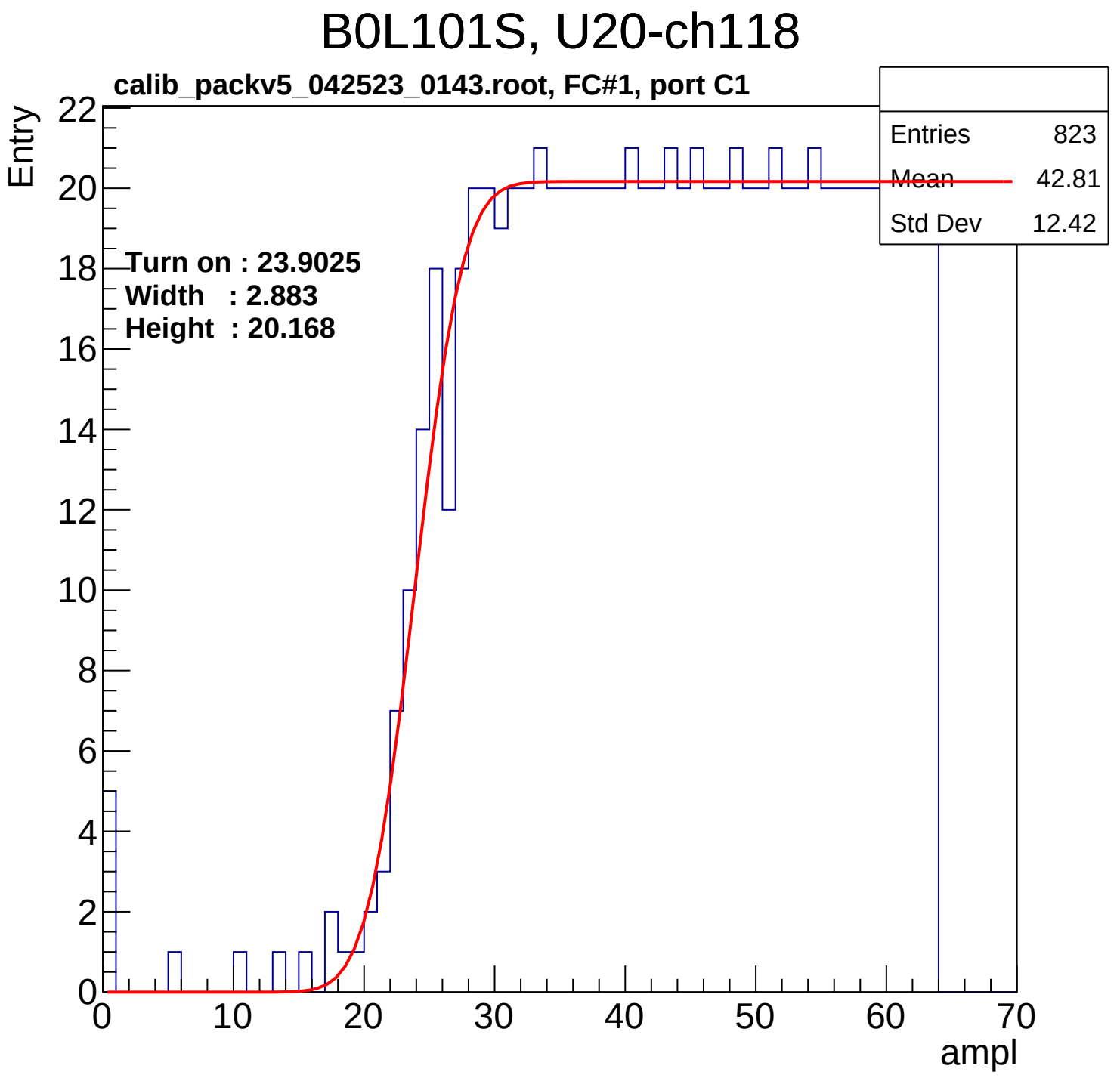
B0L101S, U20-ch118
calib_packv5_042523_0143.root, FC#1, port C1
Entries 823
Mean 42.81
Std Dev 12.42
Turn on : 23.9025
Width : 2.883
Height : 20.168
Entry
ampl
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8
10
12
14
16
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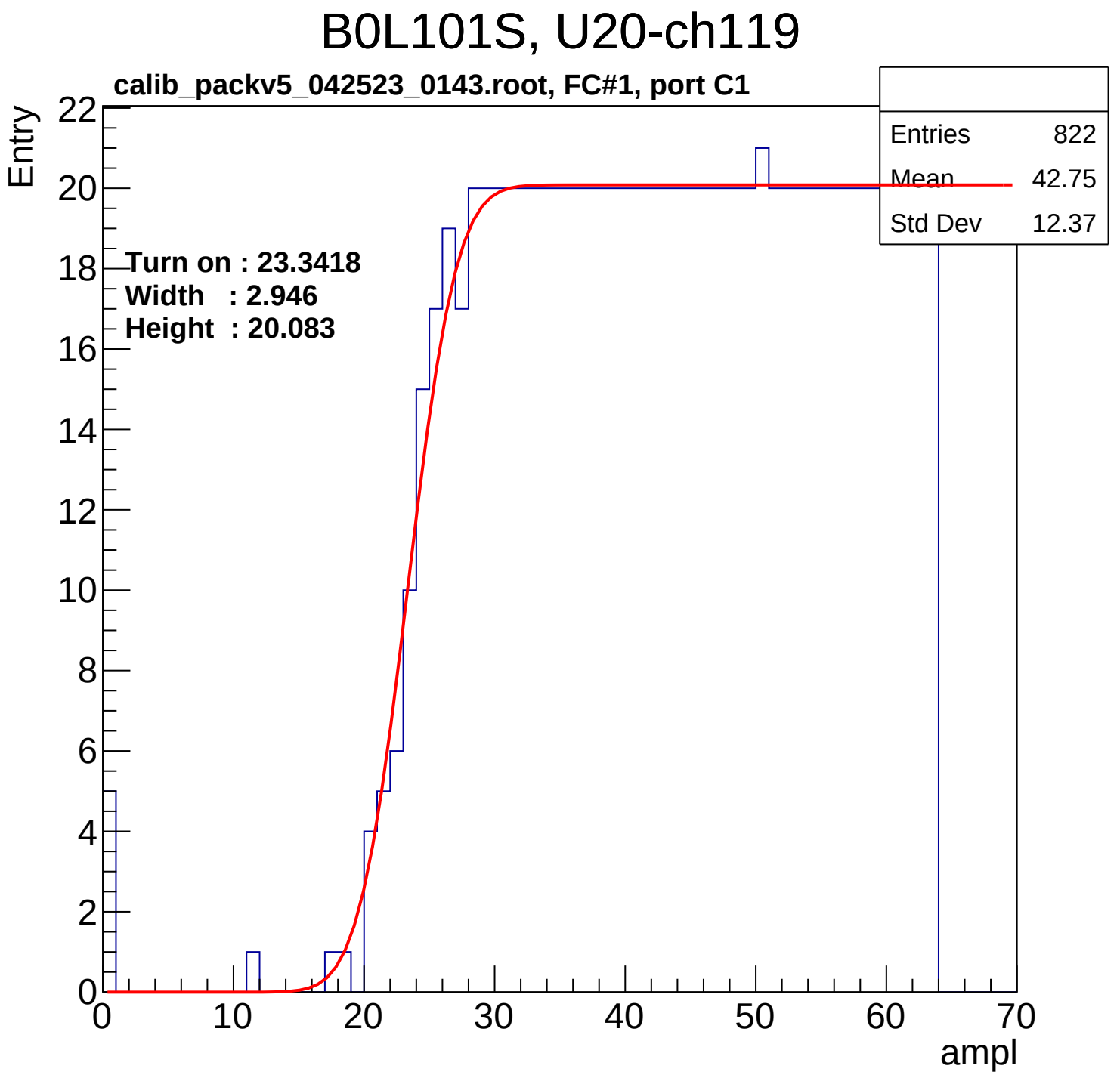
B0L101S, U20-ch119
calib_packv5_042523_0143.root, FC#1, port C1
Entries 822
Mean 42.75
Std Dev 12.37
Turn on : 23.3418
Width : 2.946
Height : 20.083
Entry
ampl
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8
10
12
14
16
18
20
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0
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20
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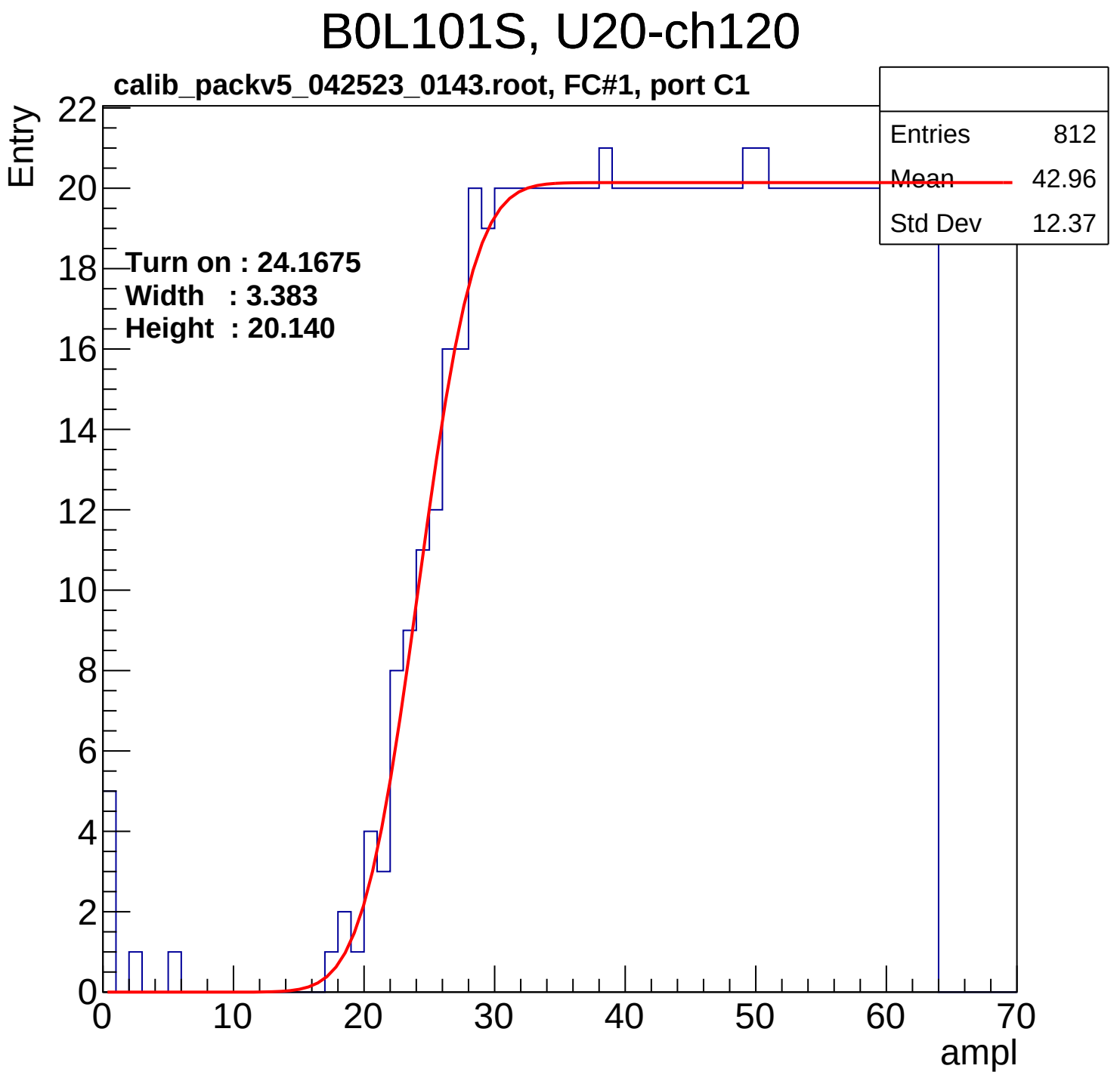
B0L101S, U20-ch120
calib_packv5_042523_0143.root, FC#1, port C1
Entries 812
Mean 42.96
Std Dev 12.37
Turn on : 24.1675
Width : 3.383
Height : 20.140
Entry
ampl
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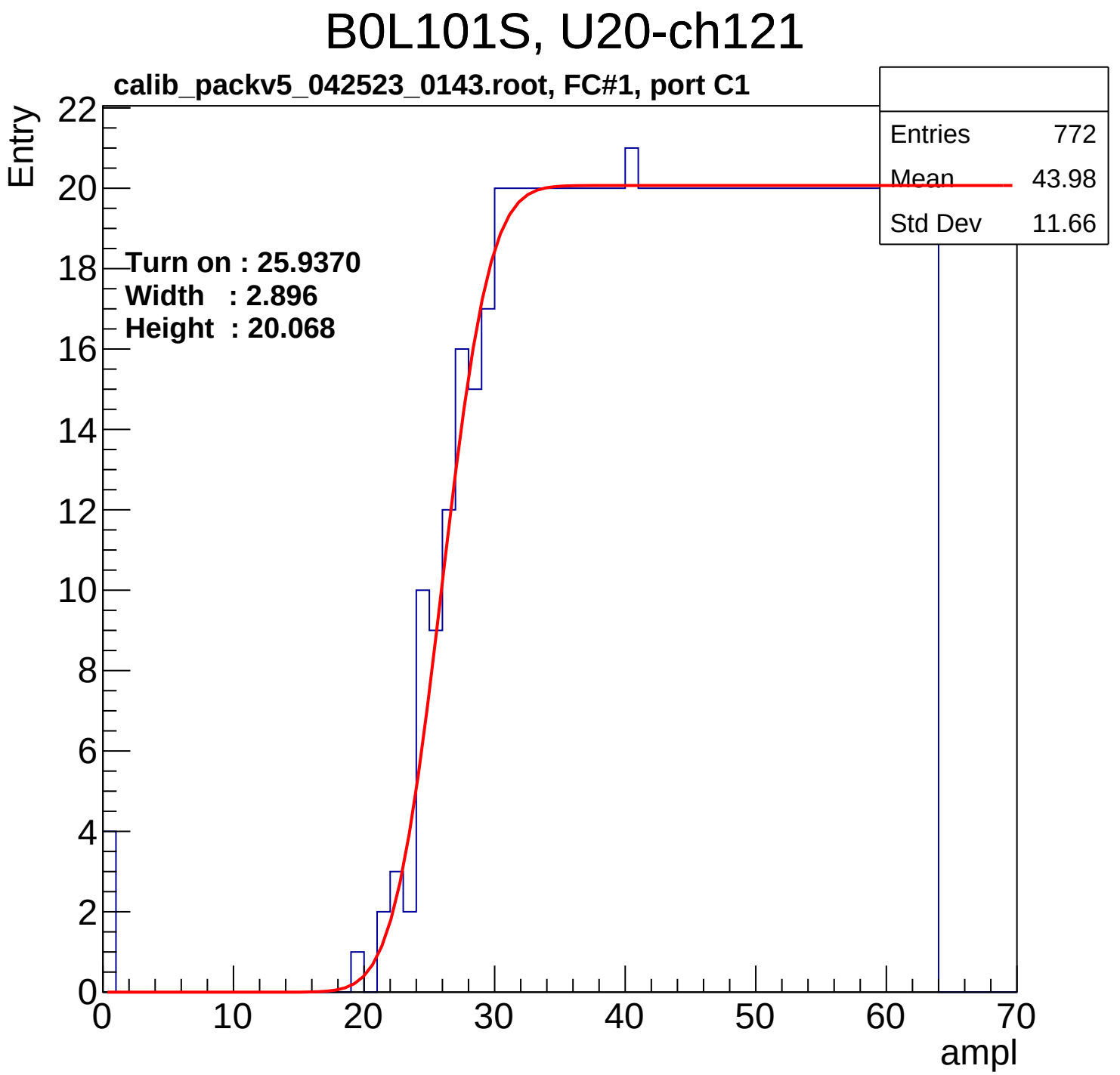
B0L101S, U20-ch121
calib_packv5_042523_0143.root, FC#1, port C1
Entries 772
Mean 43.98
Std Dev 11.66
Turn on : 25.9370
Width : 2.896
Height : 20.068
Entry
ampl
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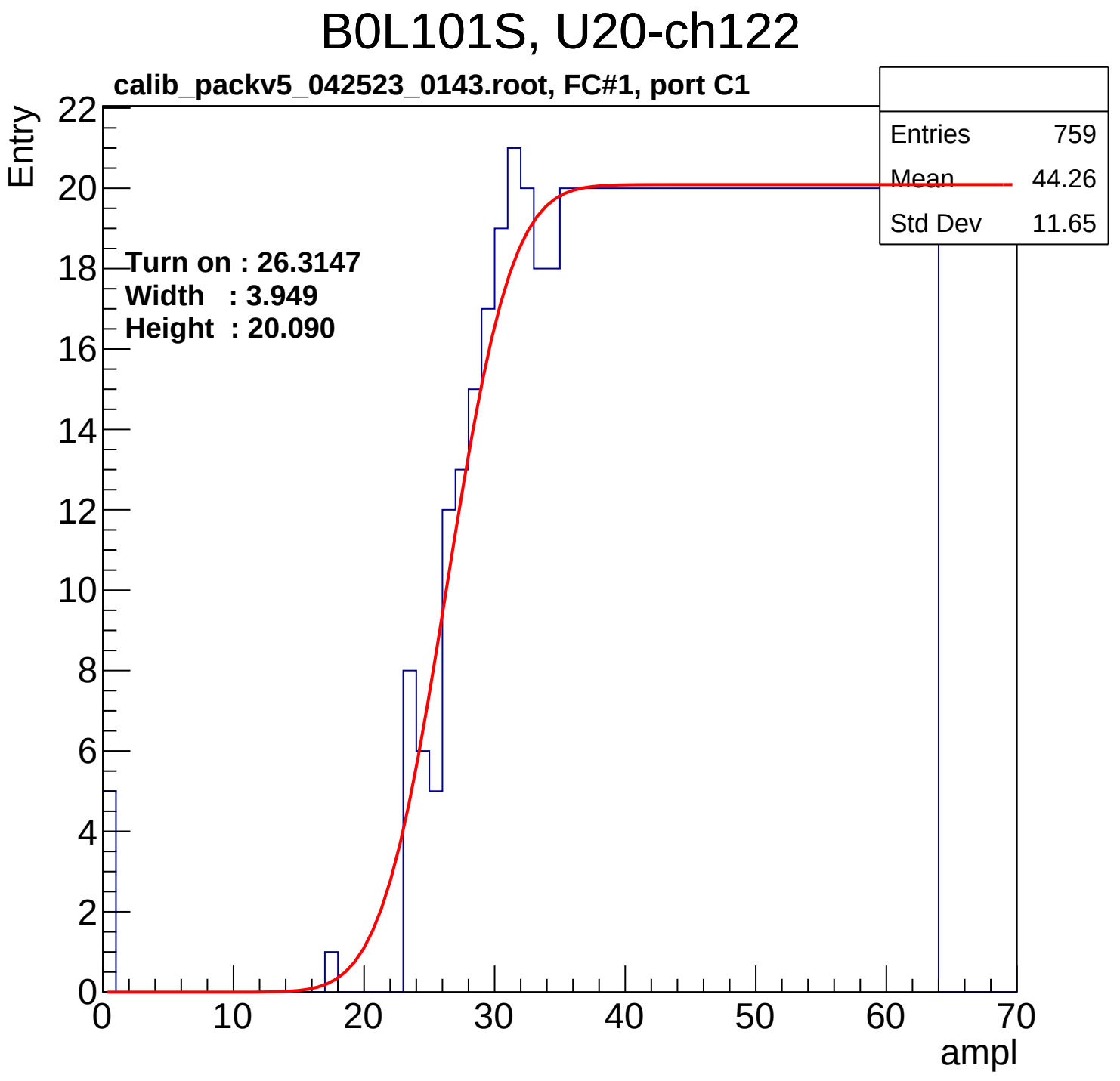
B0L101S, U20-ch122
calib_packv5_042523_0143.root, FC#1, port C1
Entries 759
Mean 44.26
Std Dev 11.65
Turn on : 26.3147
Width : 3.949
Height : 20.090
Entry
ampl
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8
10
12
14
16
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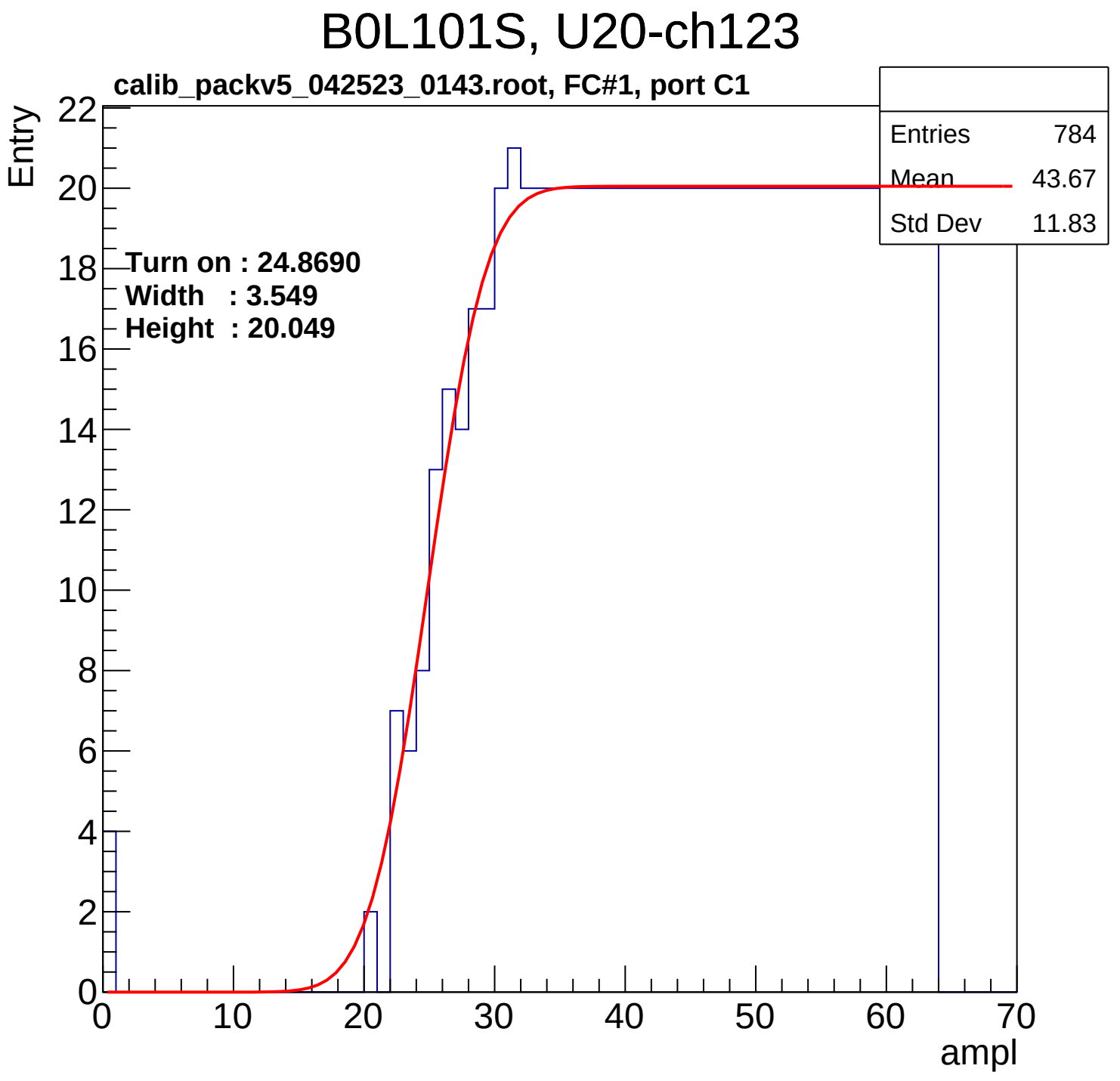
B0L101S, U20-ch123
calib_packv5_042523_0143.root, FC#1, port C1
Entries 784
Mean 43.67
Std Dev 11.83
Turn on : 24.8690
Width : 3.549
Height : 20.049
Entry
ampl
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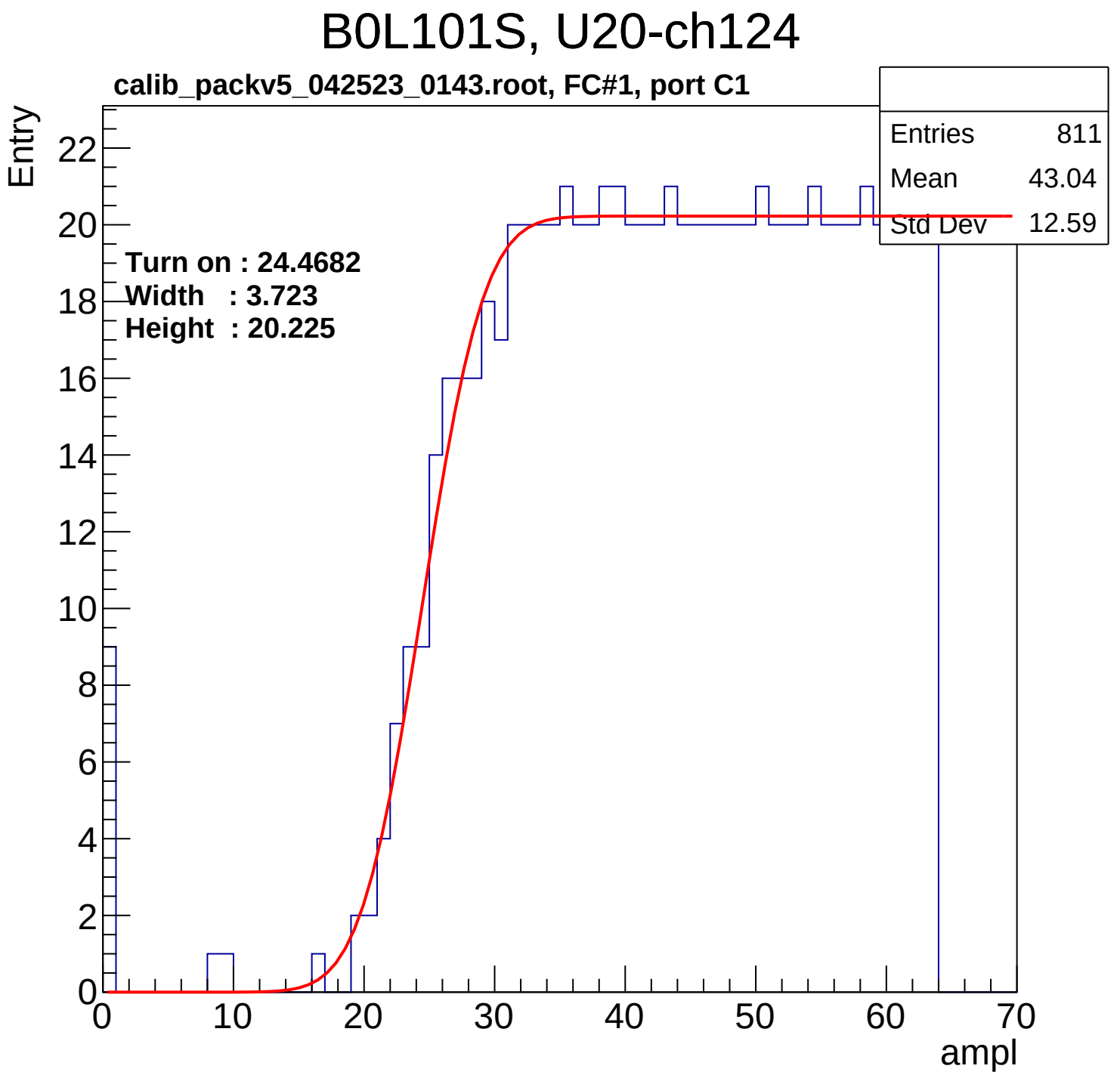
B0L101S, U20-ch124
calib_packv5_042523_0143.root, FC#1, port C1
Entries 811
Mean 43.04
Std Dev 12.59
Turn on : 24.4682
Width : 3.723
Height : 20.225
Entry
ampl
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10
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14
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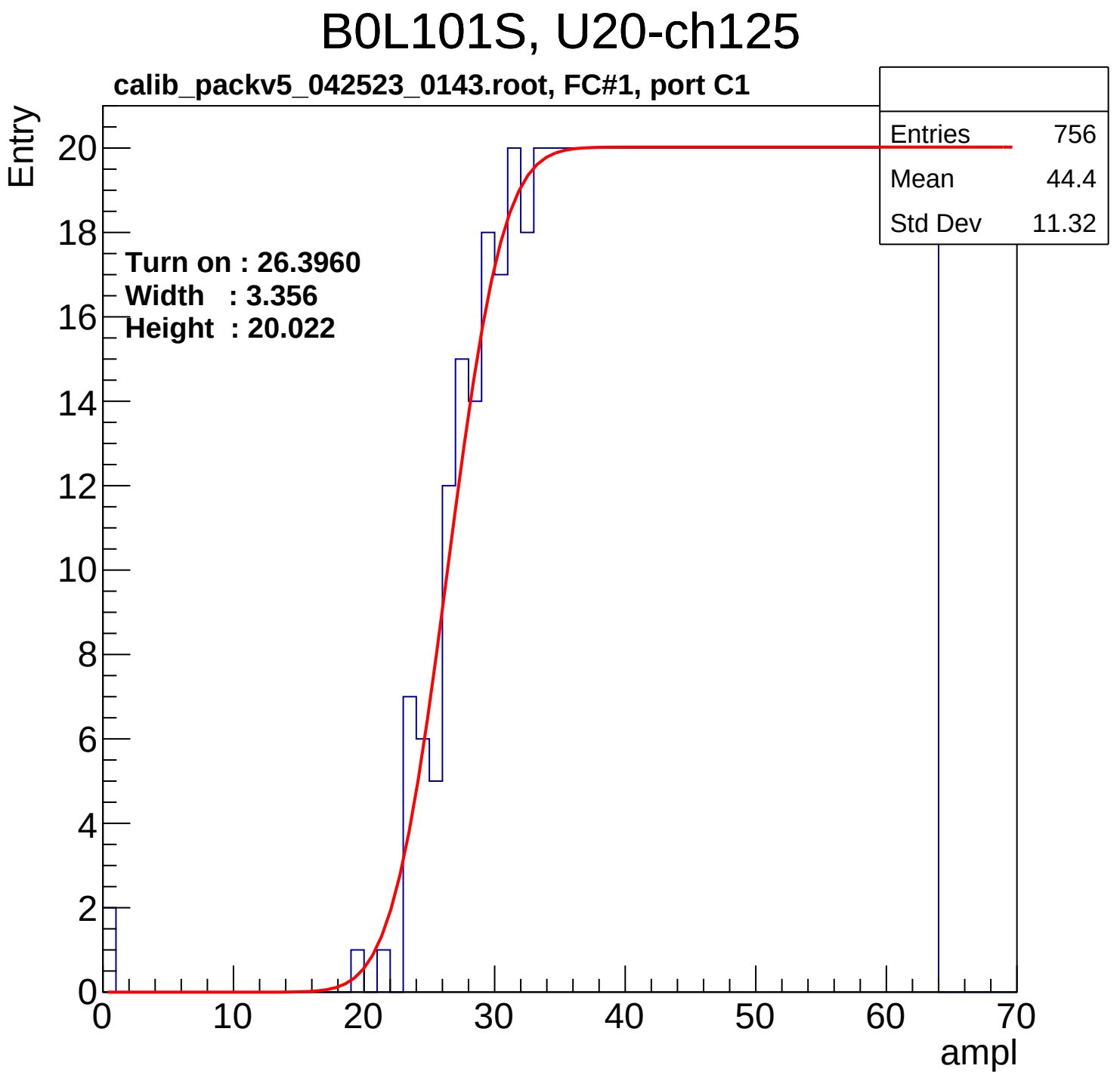
B0L101S, U20-ch125
calib_packv5_042523_0143.root, FC#1, port C1
Entries 756
Mean 44.4
Std Dev 11.32
Turn on : 26.3960
Width : 3.356
Height : 20.022
Entry
ampl
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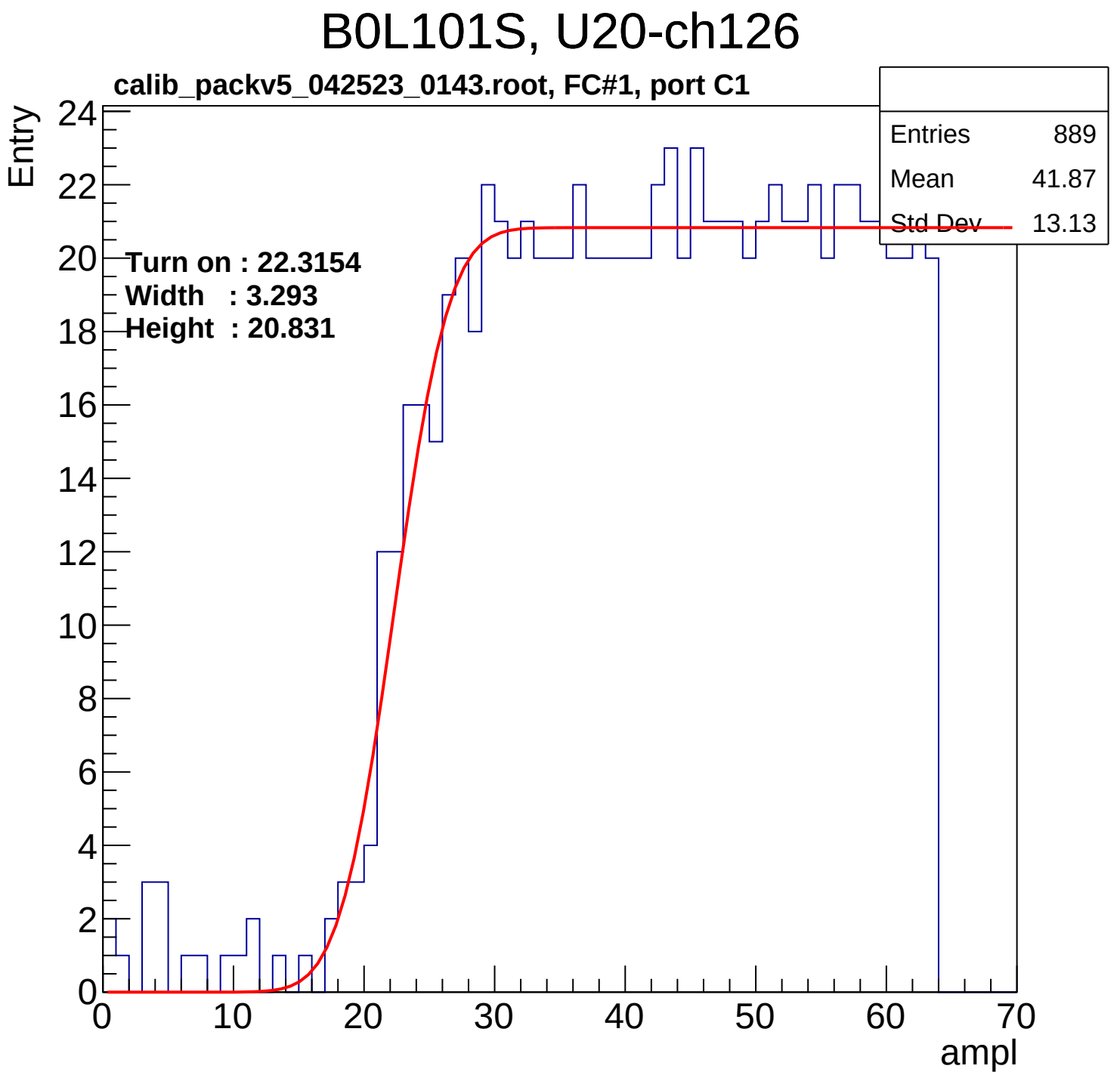
B0L101S, U20-ch126
calib_packv5_042523_0143.root, FC#1, port C1
Entries 889
Mean 41.87
Std Dev 13.13
Turn on : 22.3154
Width : 3.293
Height : 20.831
Entry
ampl
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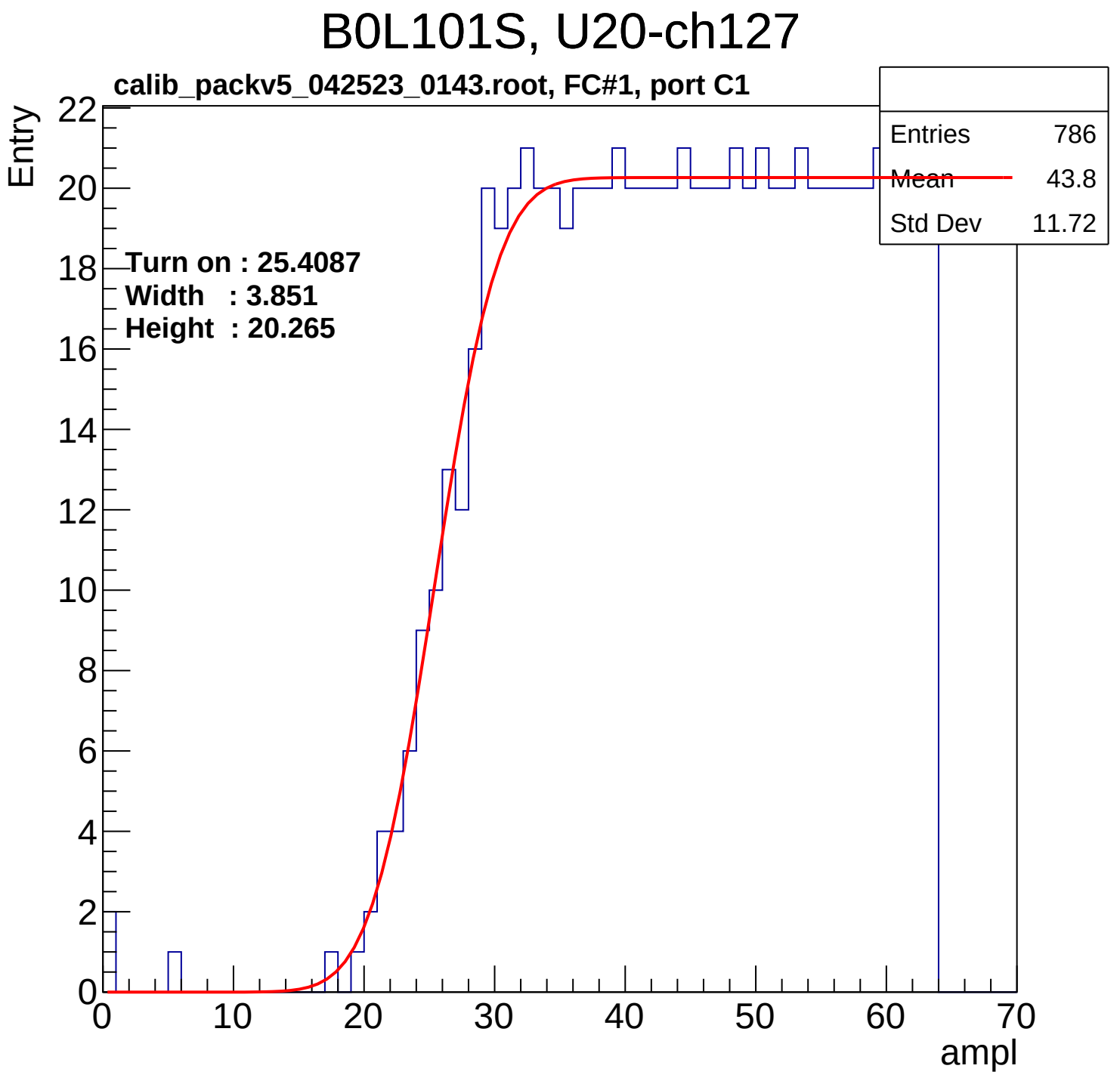
B0L101S, U20-ch127
calib_packv5_042523_0143.root, FC#1, port C1
Entries 786
Mean 43.8
Std Dev 11.72
Turn on : 25.4087
Width : 3.851
Height : 20.265
Entry
ampl
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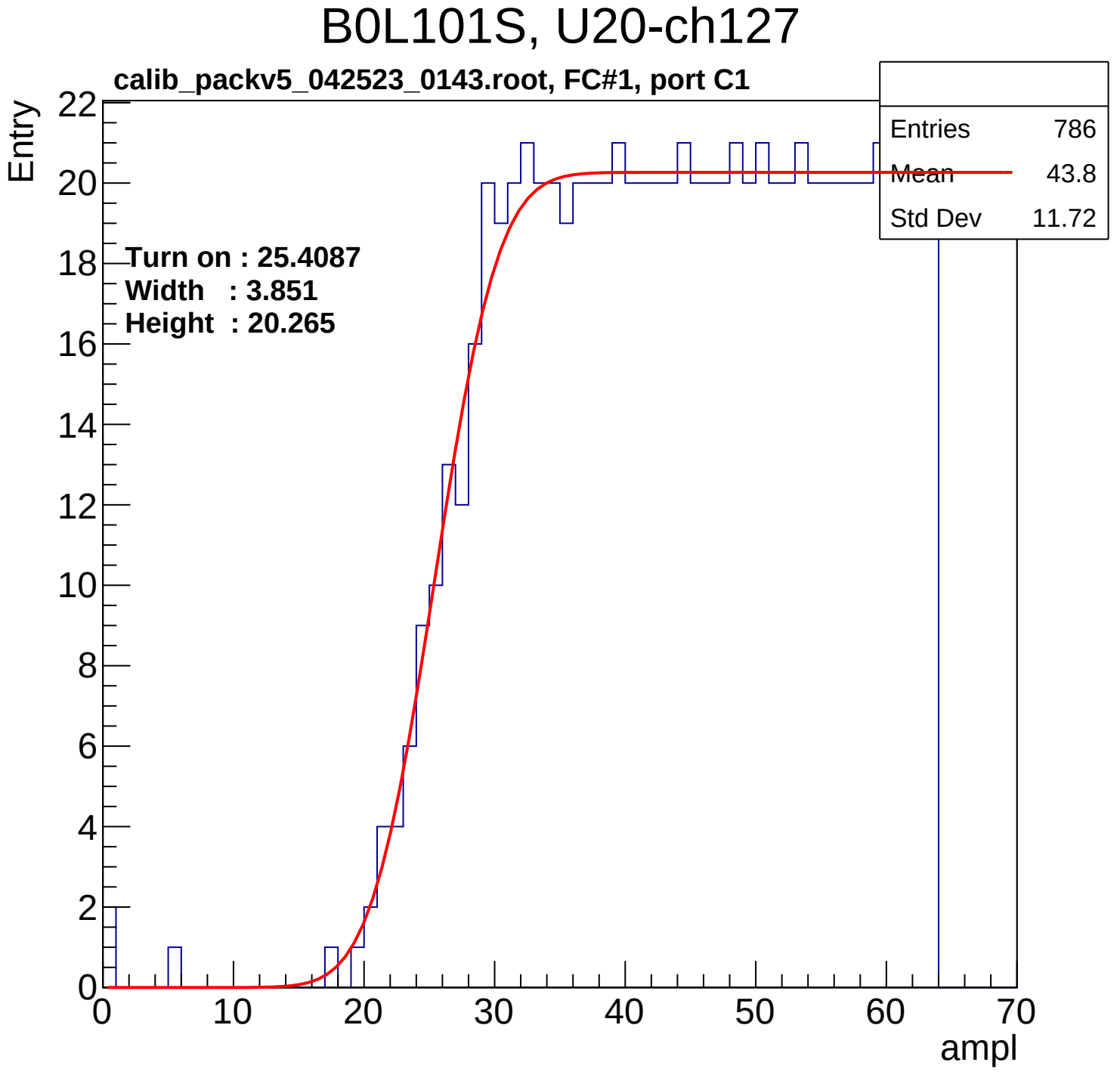
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Entries 786
Mean 43.8
Std Dev 11.72
Turn on : 25.4087
Width : 3.851
Height : 20.265
Entry
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