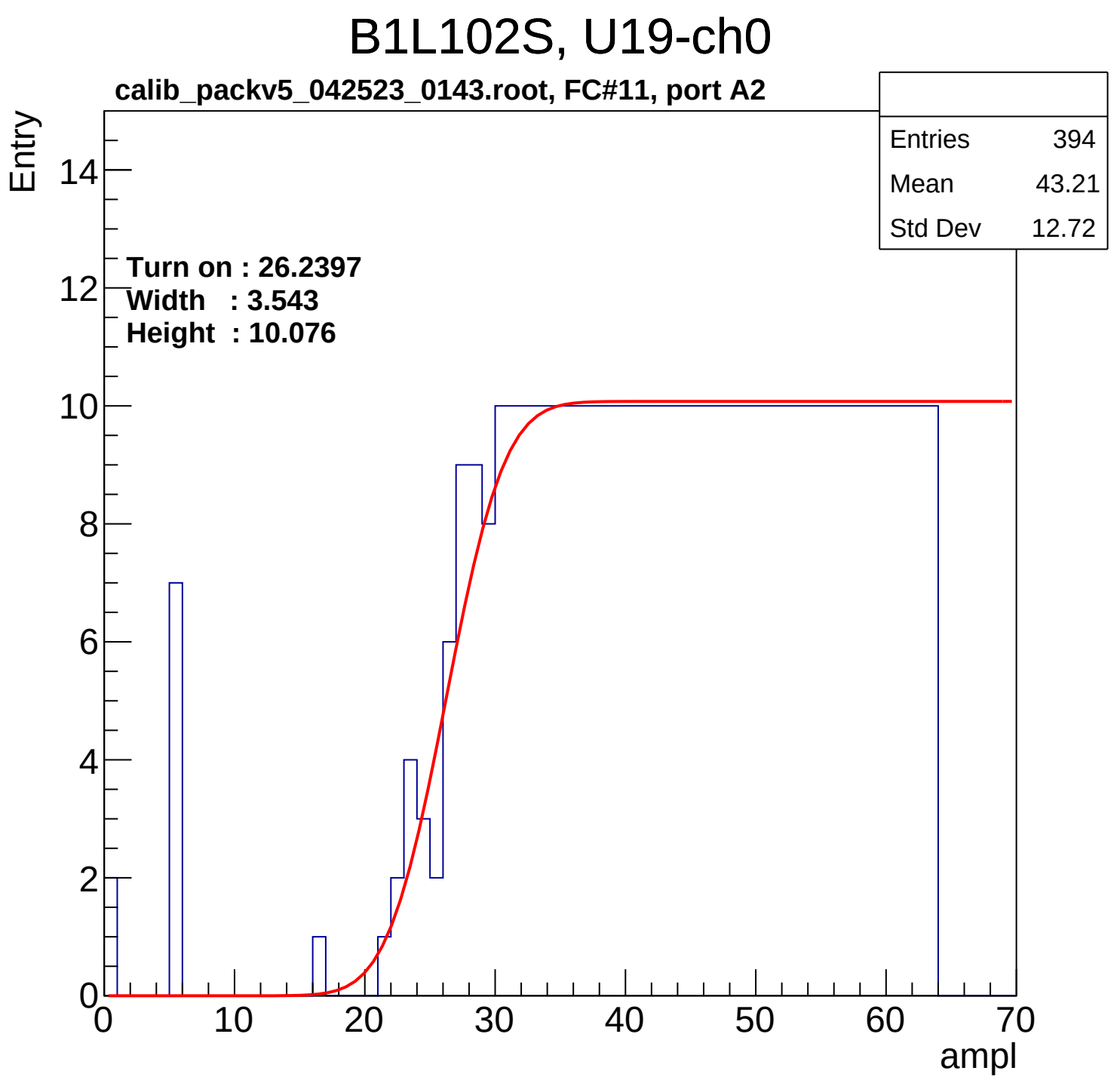
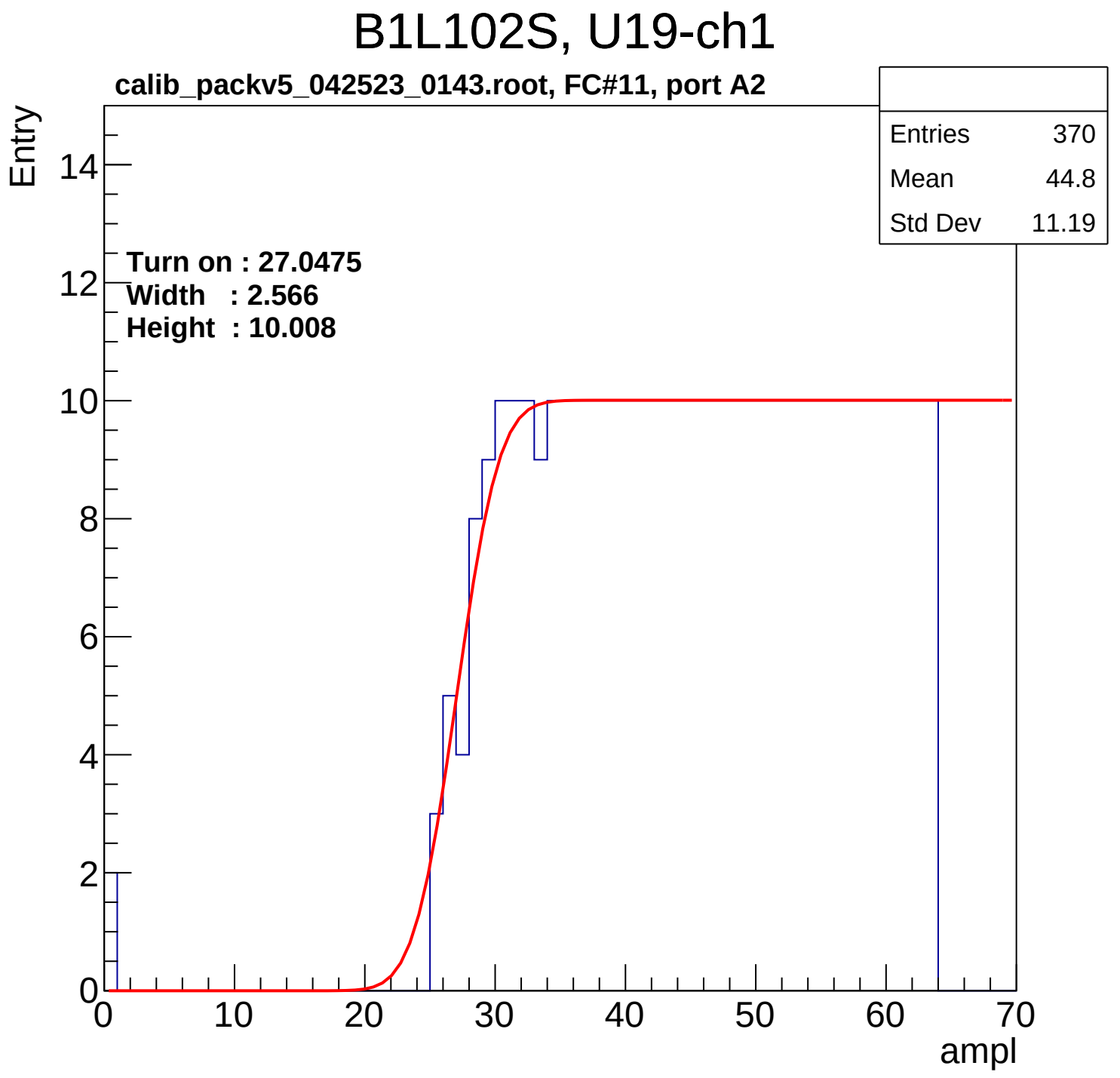
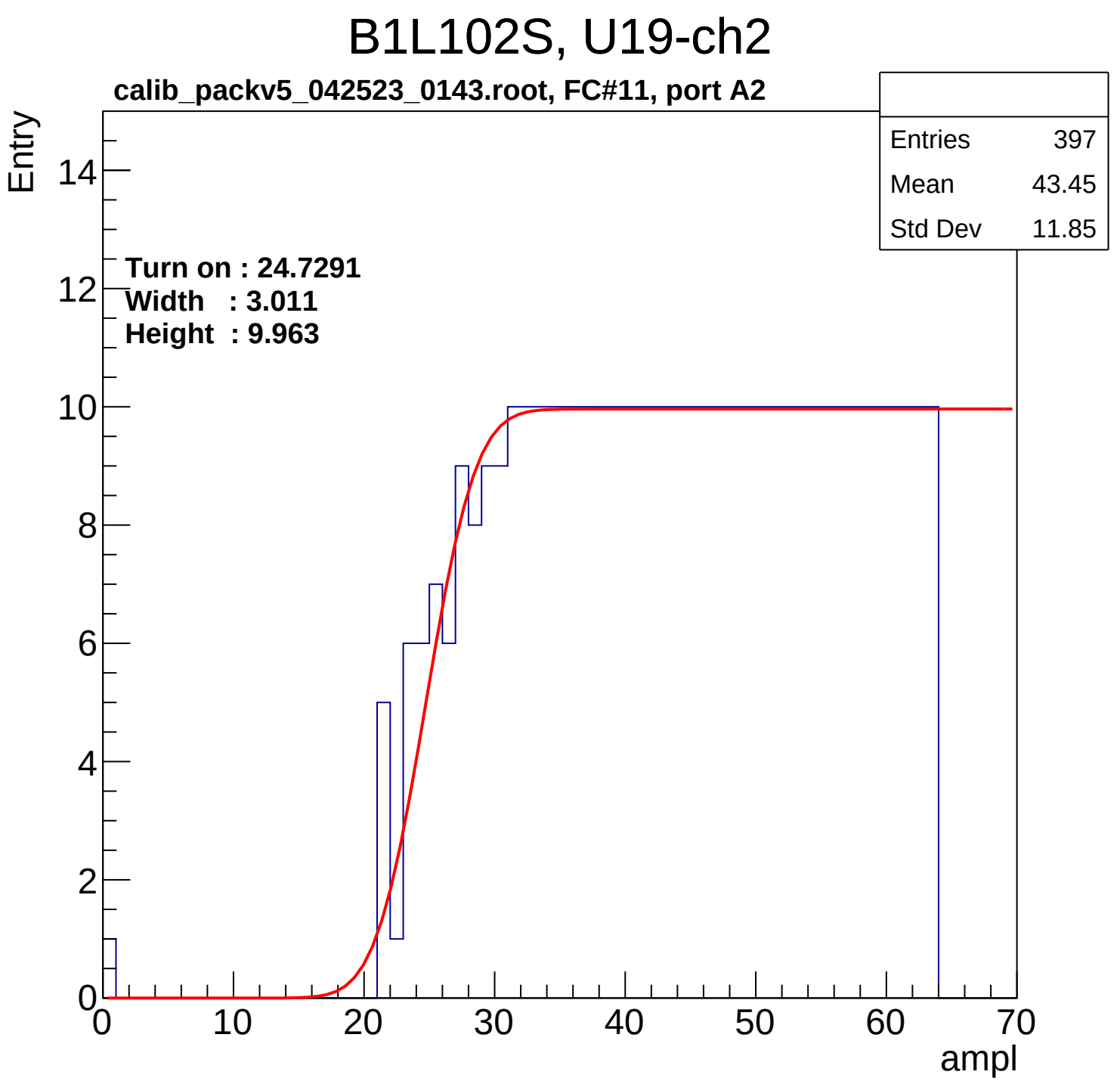
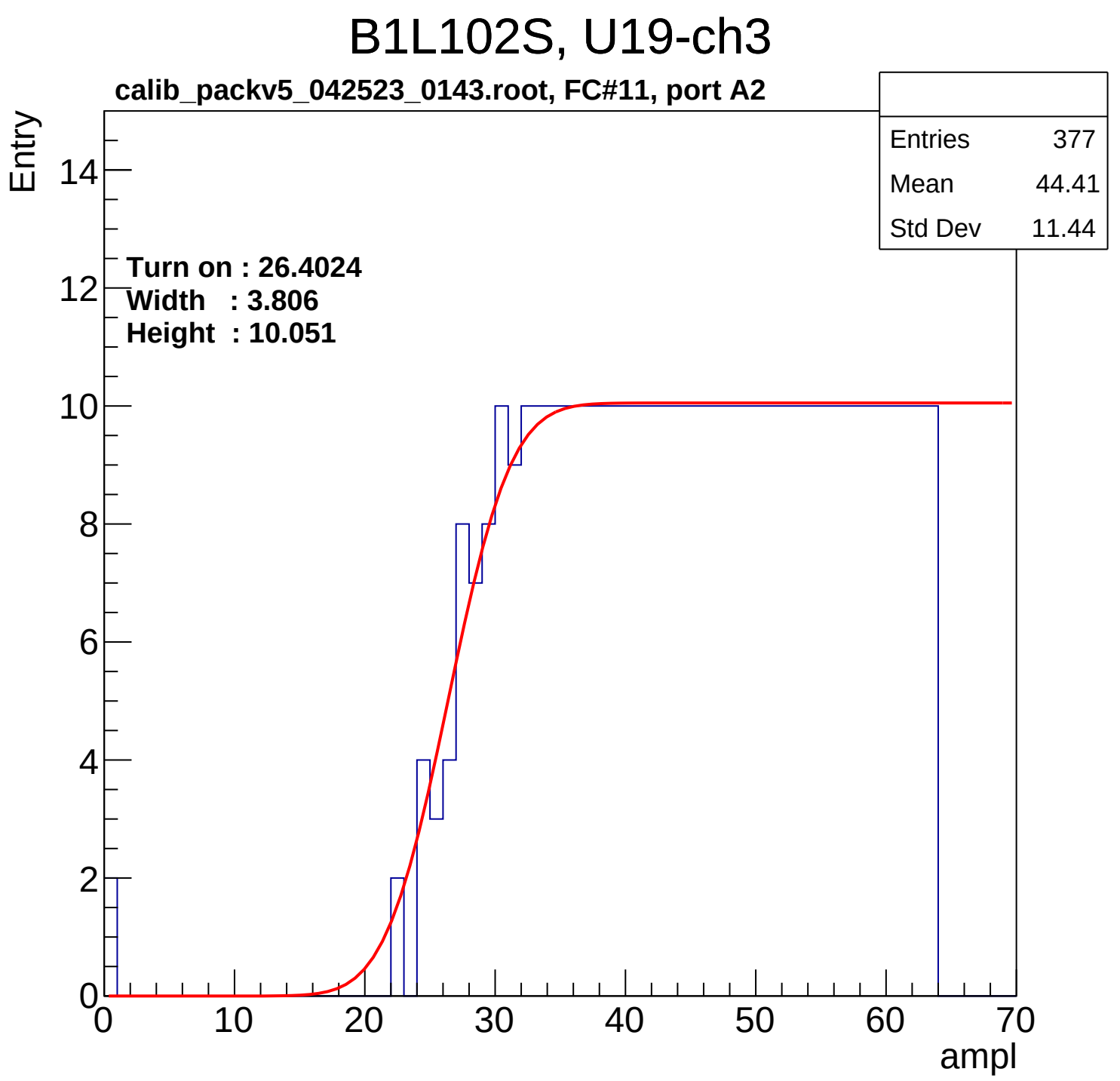
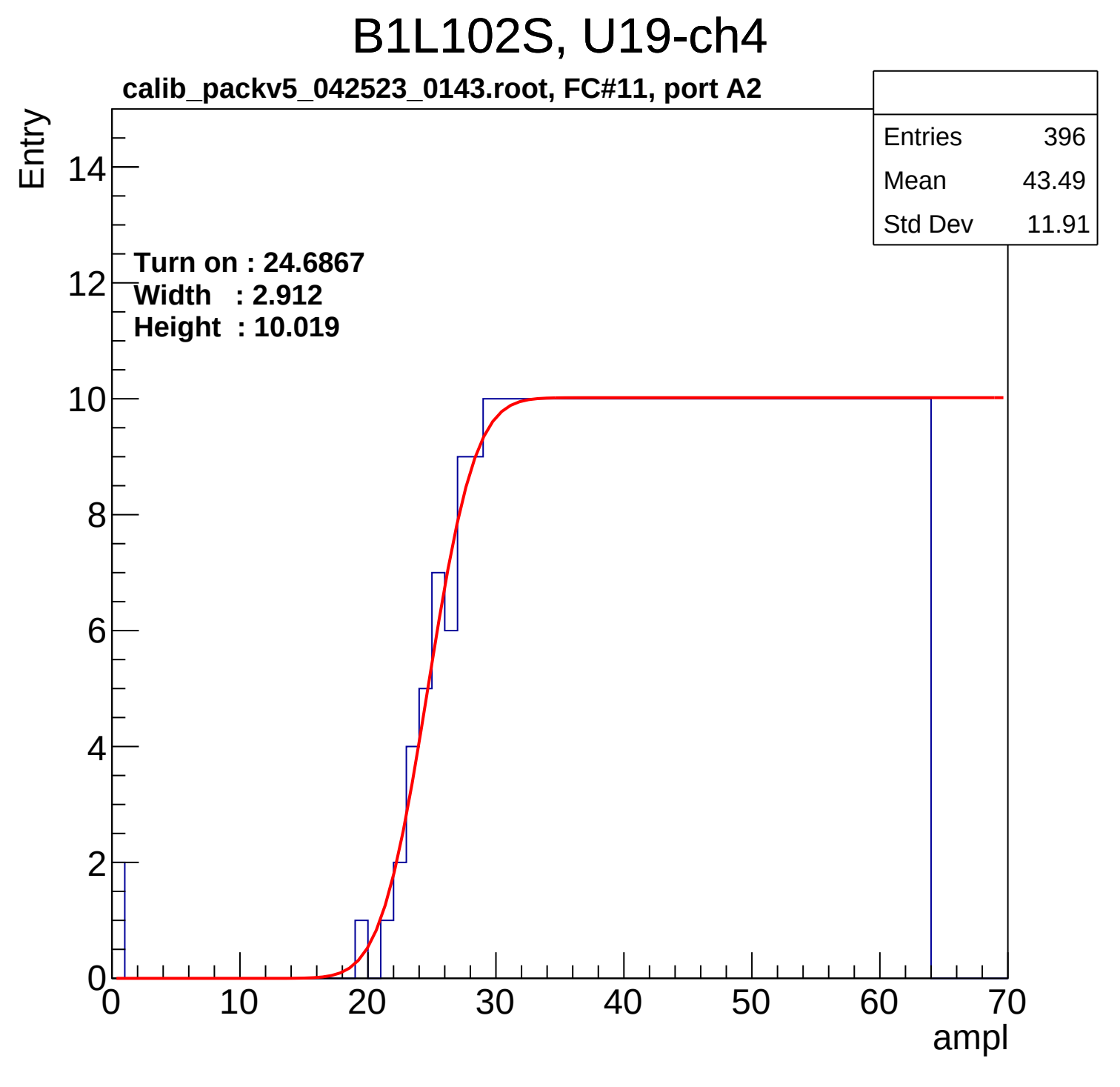
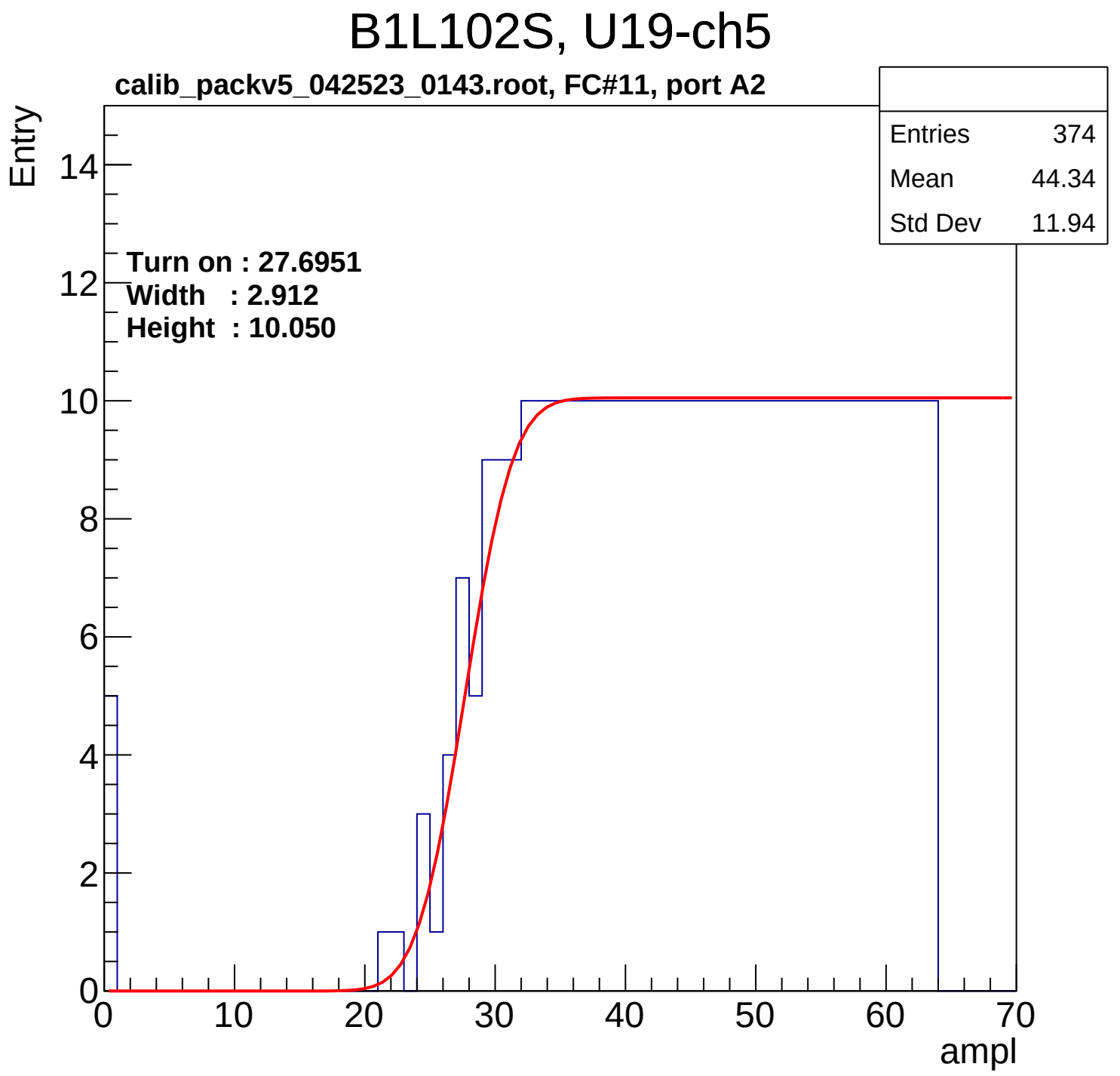

B1L102S, U19-ch0
calib_packv5_042523_0143.root, FC#11, port A2
Entries 394
Mean 43.21
Std Dev 12.72
Turn on : 26.2397
Width : 3.543
Height : 10.076
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

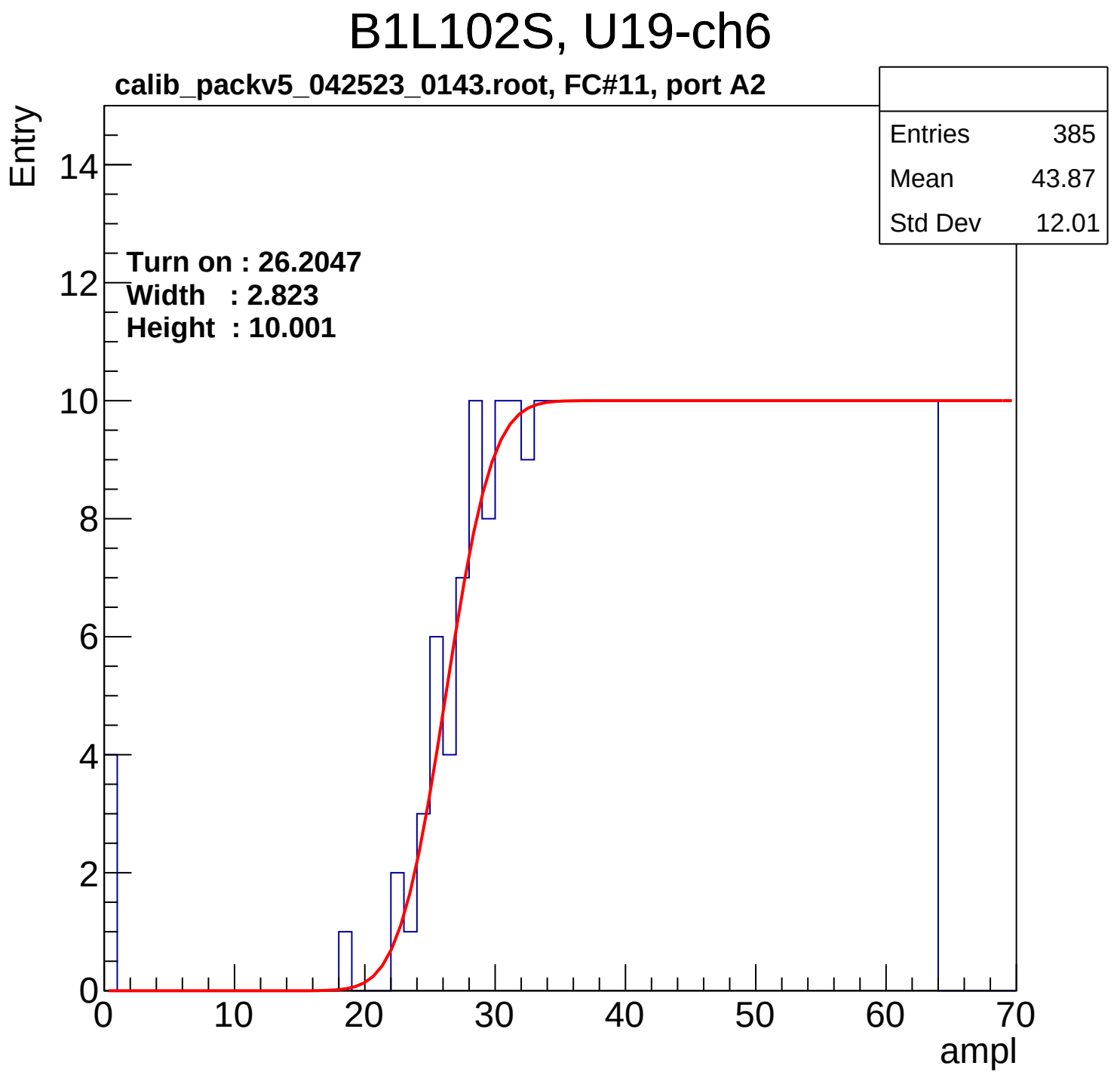

B1L102S, U19-ch1
calib_packv5_042523_0143.root, FC#11, port A2
Entries 370
Mean 44.8
Std Dev 11.19
Turn on : 27.0475
Width : 2.566
Height : 10.008
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

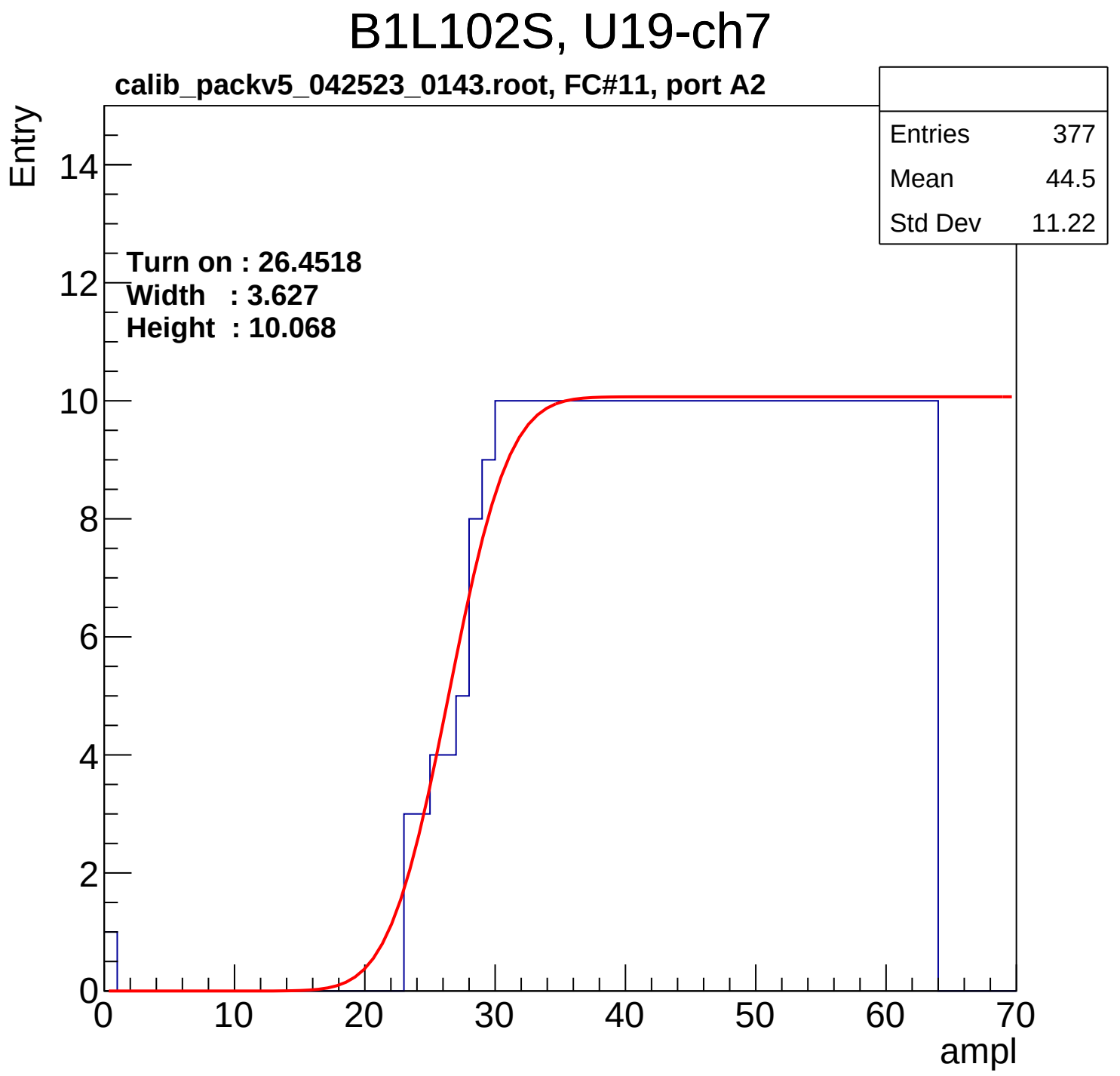

B1L102S, U19-ch2
calib_packv5_042523_0143.root, FC#11, port A2
Entries 397
Mean 43.45
Std Dev 11.85
Turn on : 24.7291
Width : 3.011
Height : 9.963
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

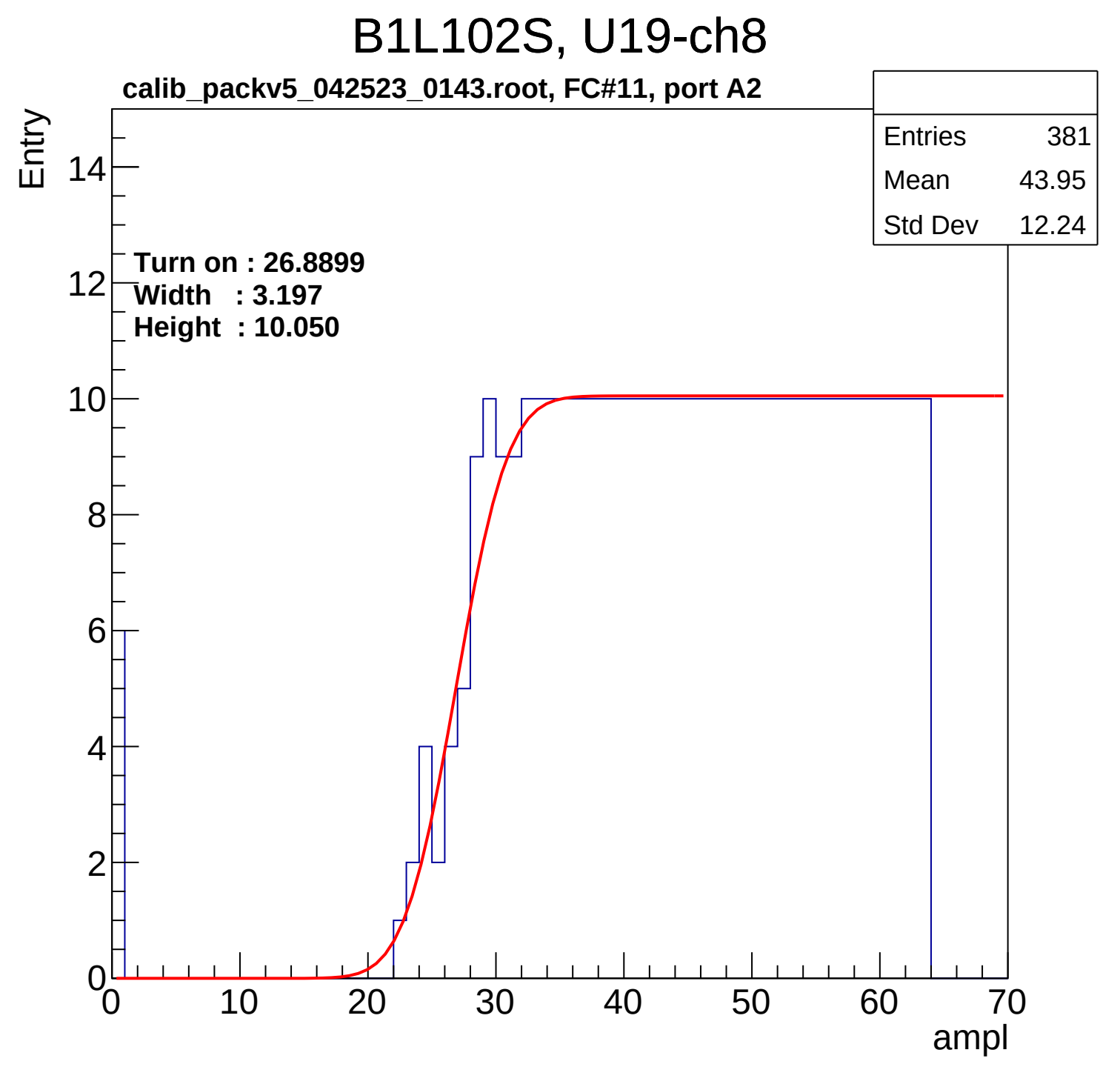

B1L102S, U19-ch3
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.41
Std Dev 11.44
Turn on : 26.4024
Width : 3.806
Height : 10.051
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

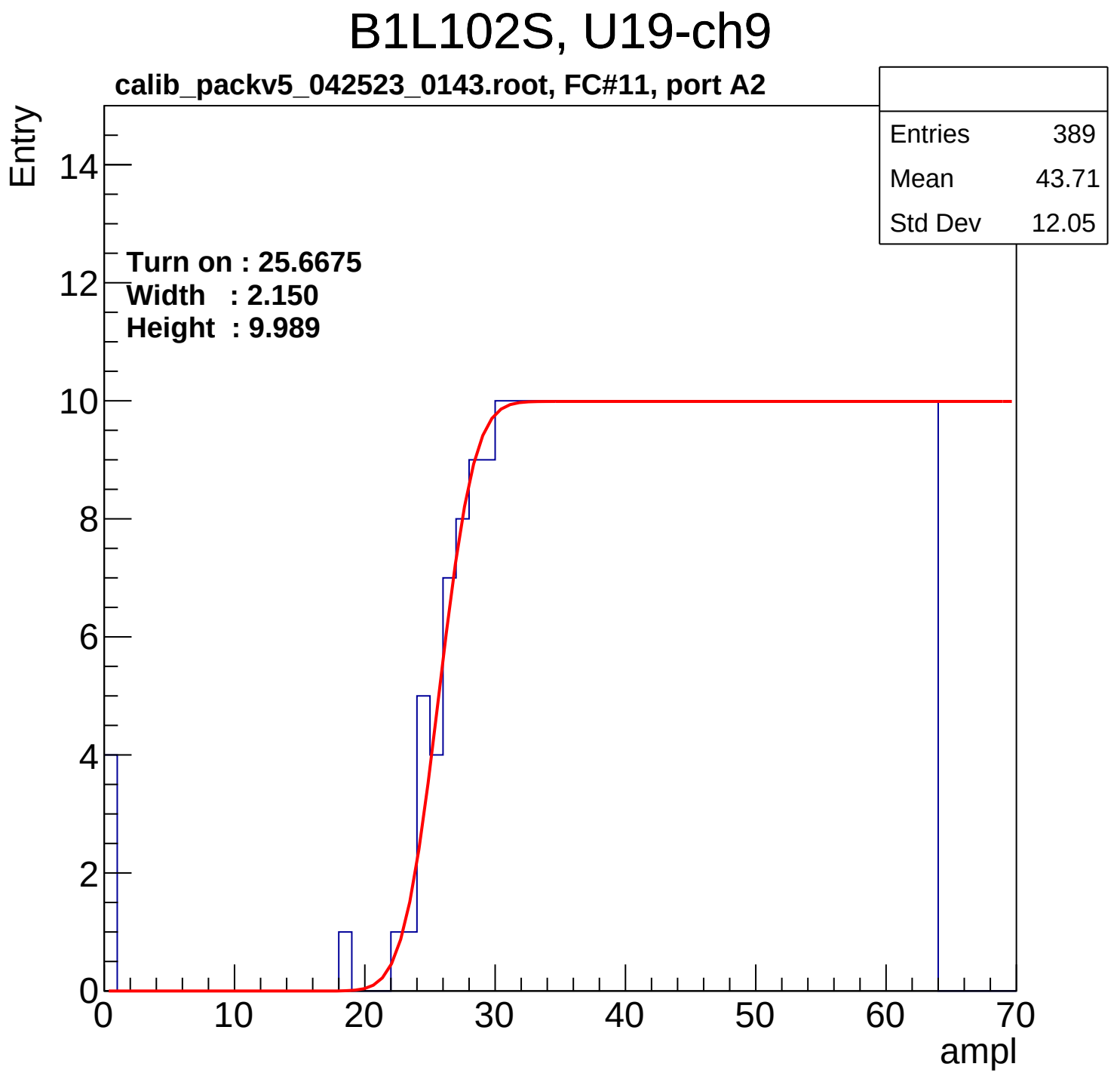

B1L102S, U19-ch4
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.49
Std Dev 11.91
Turn on : 24.6867
Width : 2.912
Height : 10.019
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

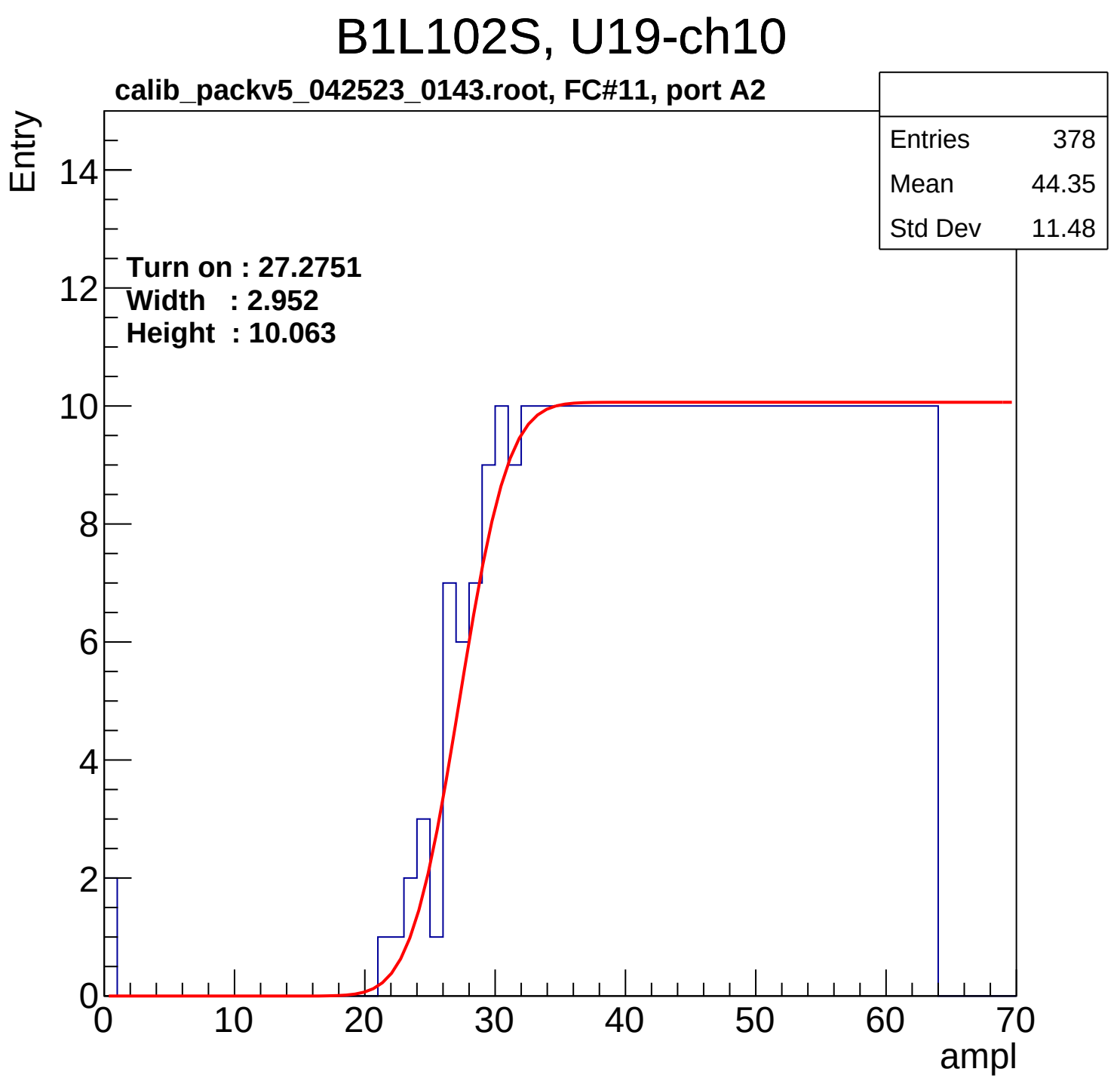

B1L102S, U19-ch5
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.34
Std Dev 11.94
Turn on : 27.6951
Width : 2.912
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

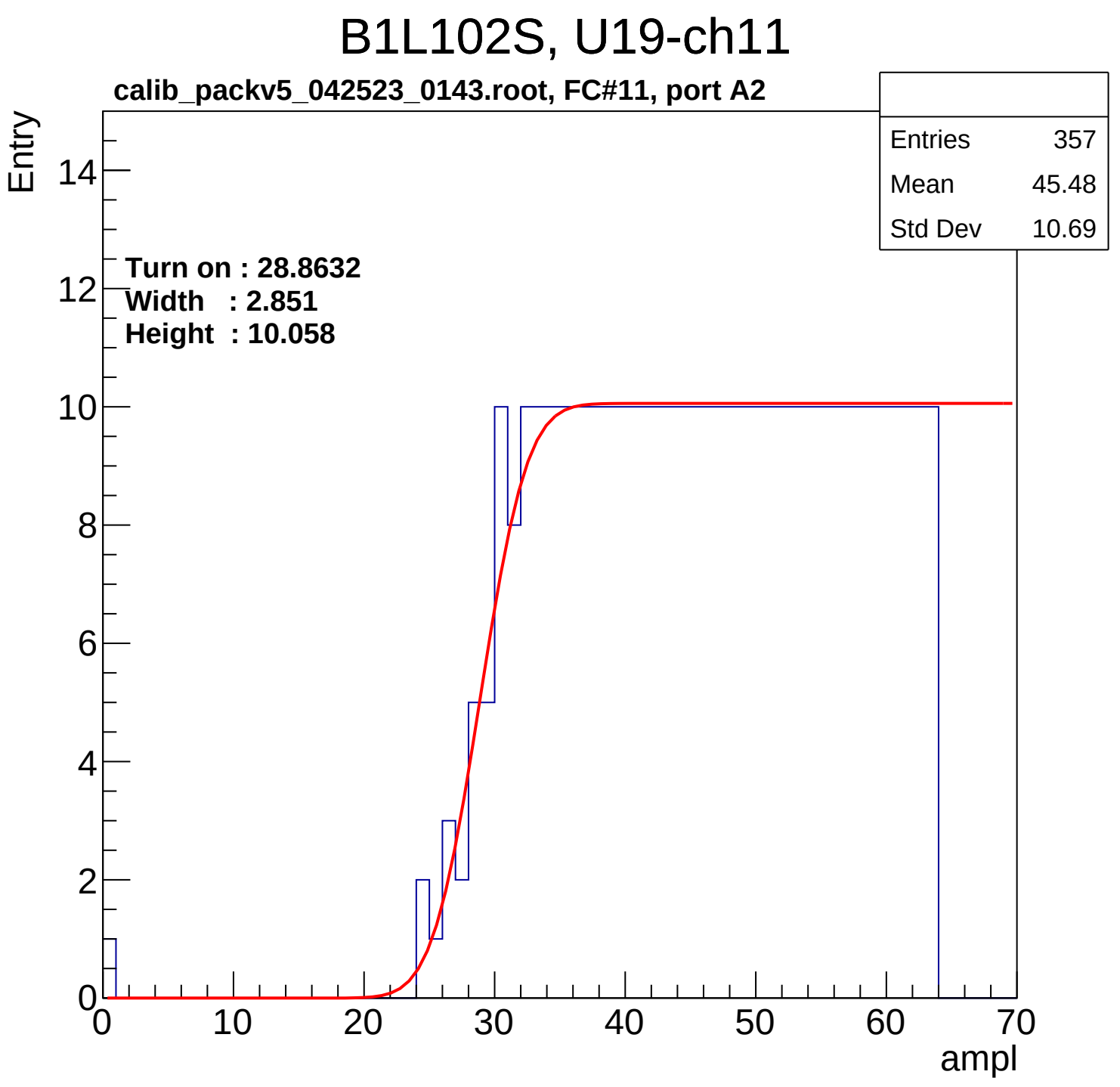

B1L102S, U19-ch6
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.87
Std Dev 12.01
Turn on : 26.2047
Width : 2.823
Height : 10.001
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

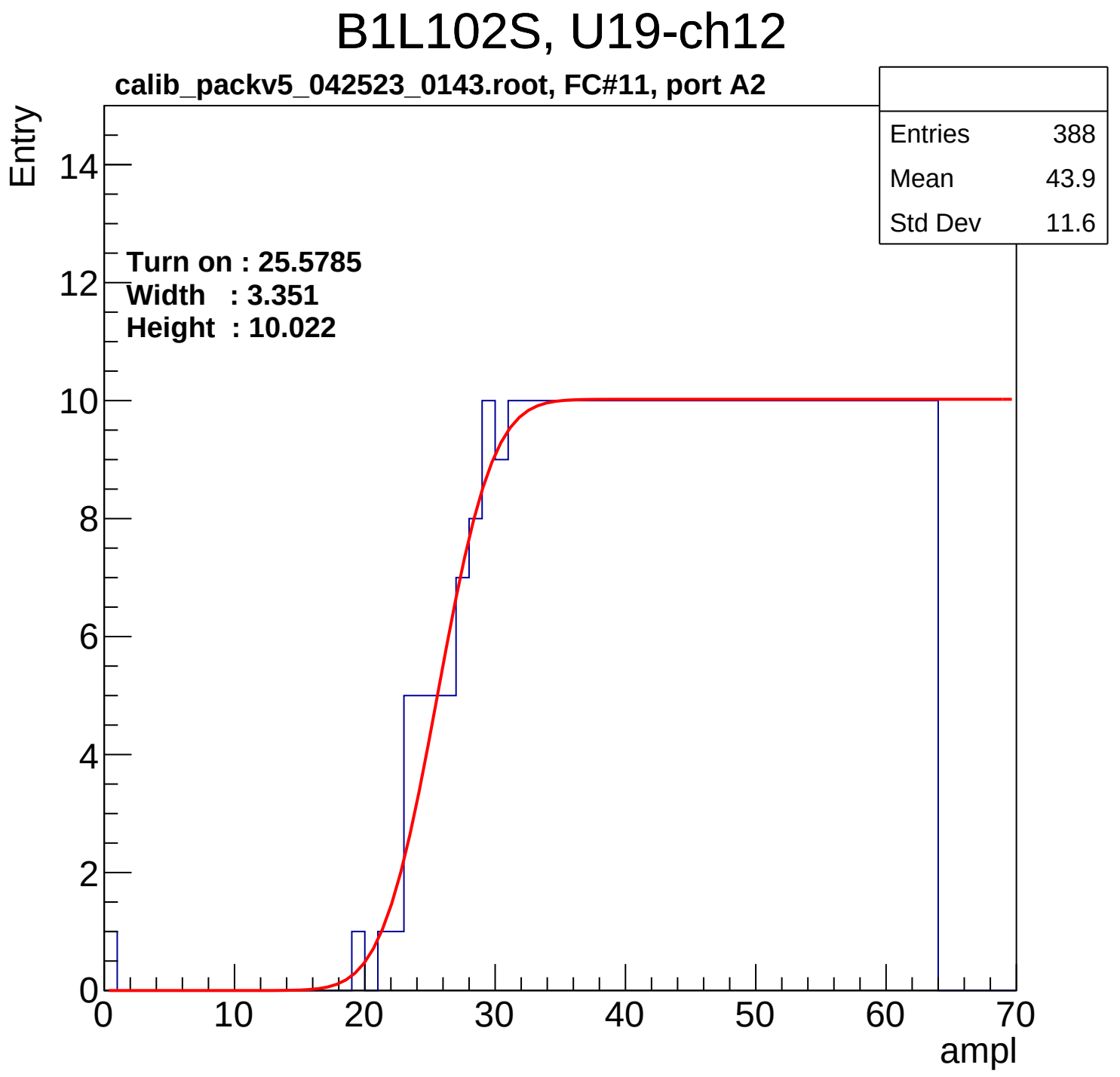

B1L102S, U19-ch7
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.5
Std Dev 11.22
Turn on : 26.4518
Width : 3.627
Height : 10.068
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

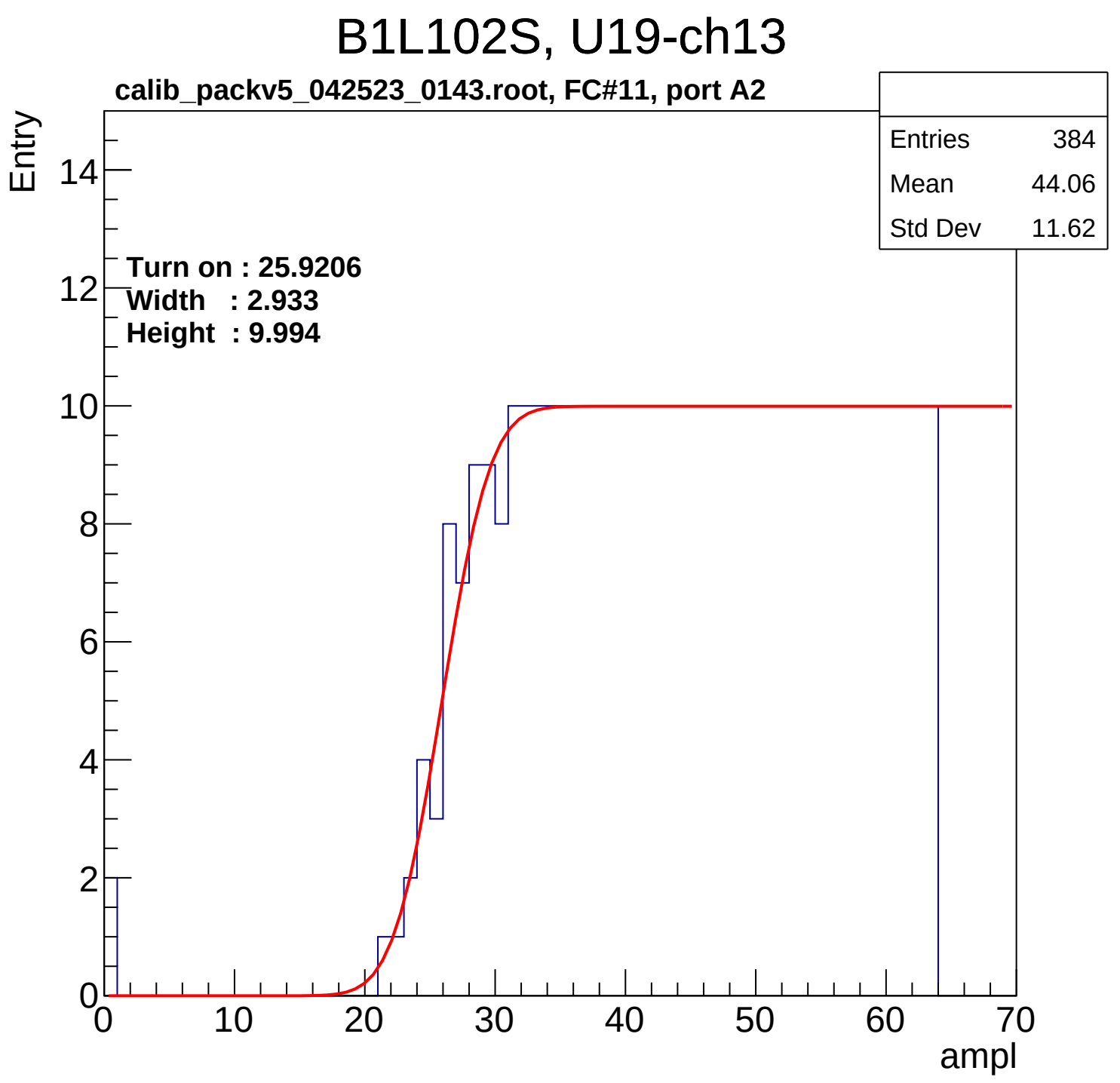

B1L102S, U19-ch8
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 43.95
Std Dev 12.24
Turn on : 26.8899
Width : 3.197
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

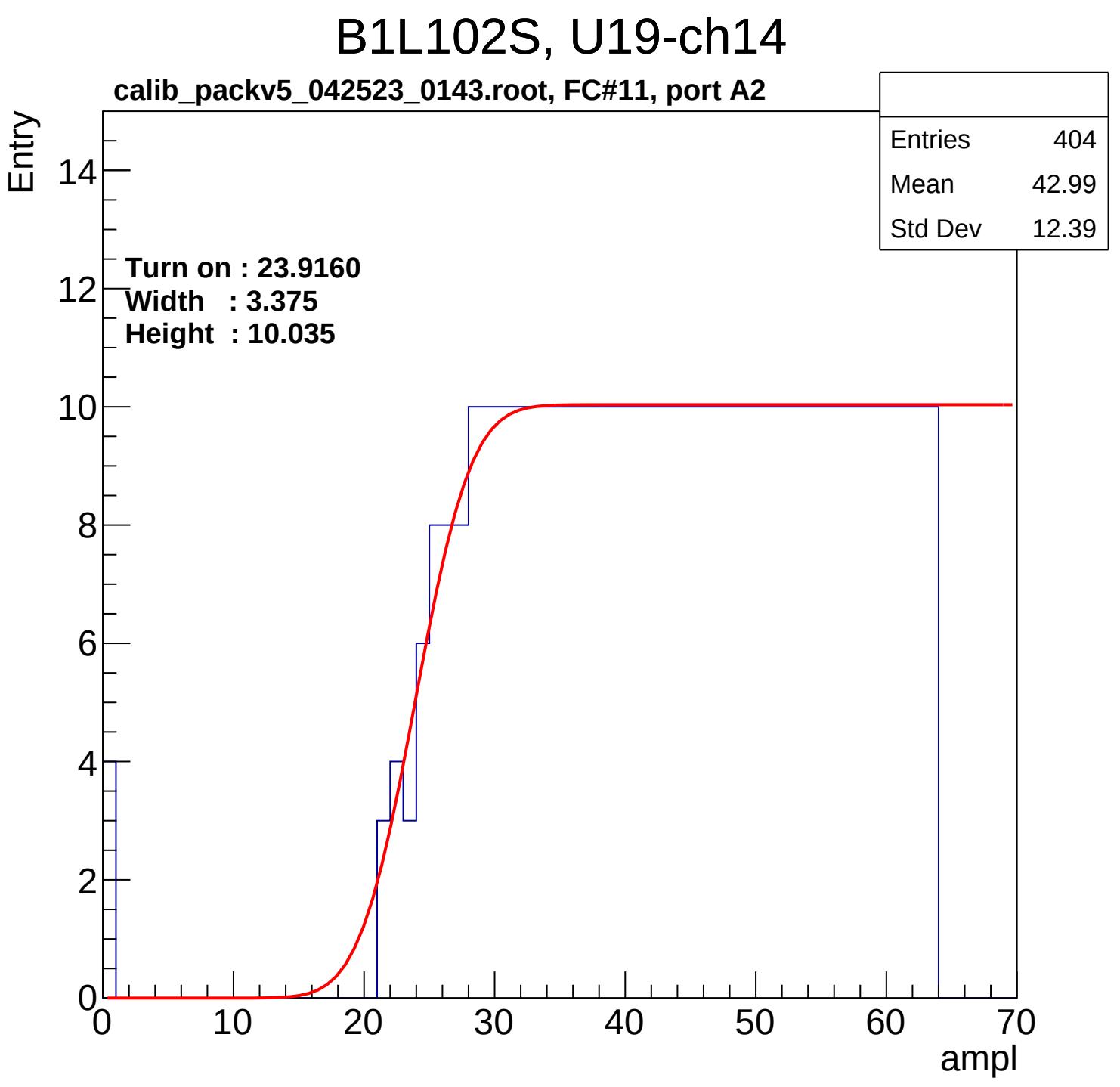

B1L102S, U19-ch9
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.71
Std Dev 12.05
Turn on : 25.6675
Width : 2.150
Height : 9.989
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

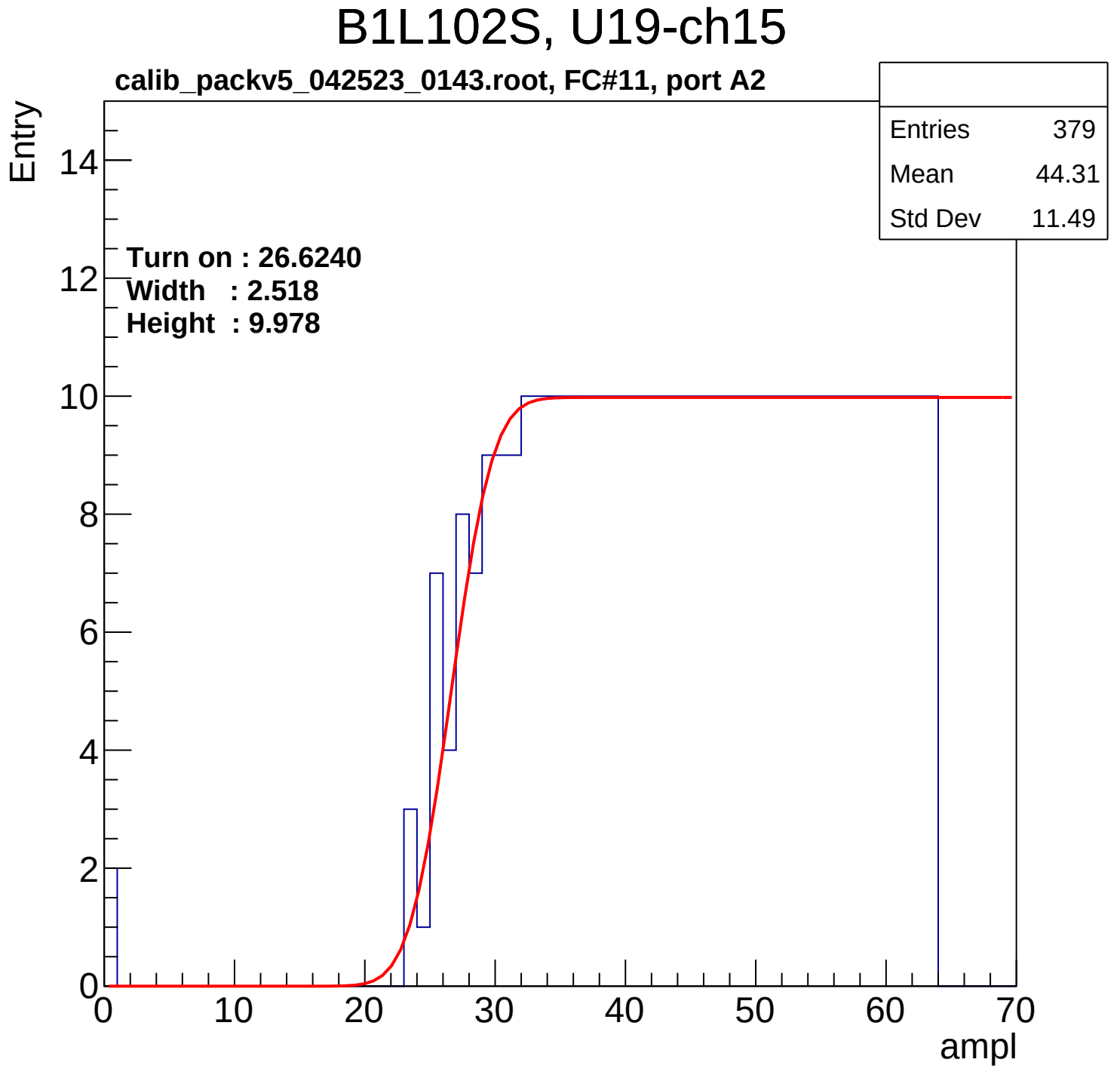

B1L102S, U19-ch10
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.35
Std Dev 11.48
Turn on : 27.2751
Width : 2.952
Height : 10.063
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

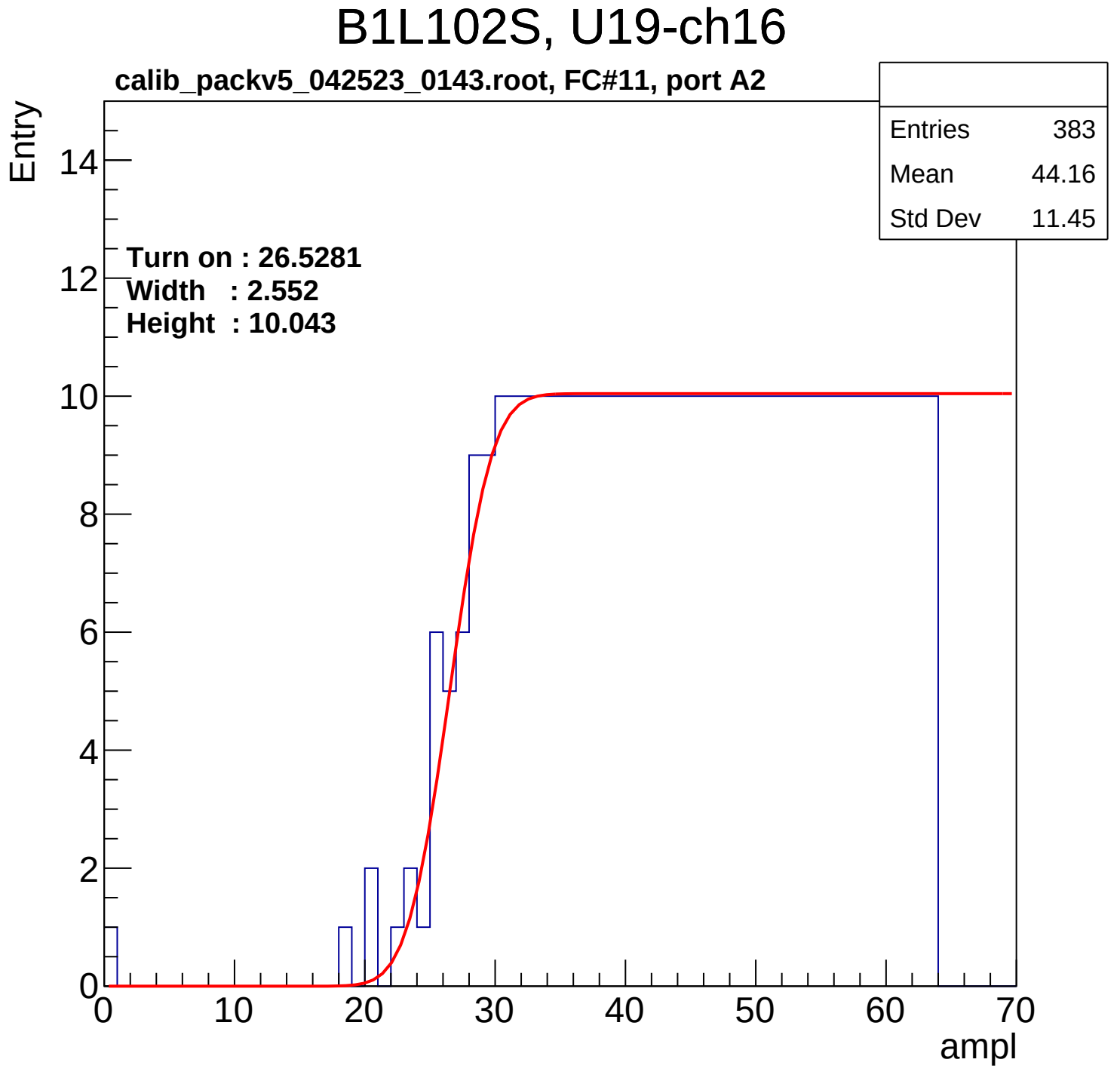

B1L102S, U19-ch11
calib_packv5_042523_0143.root, FC#11, port A2
Entries 357
Mean 45.48
Std Dev 10.69
Turn on : 28.8632
Width : 2.851
Height : 10.058
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

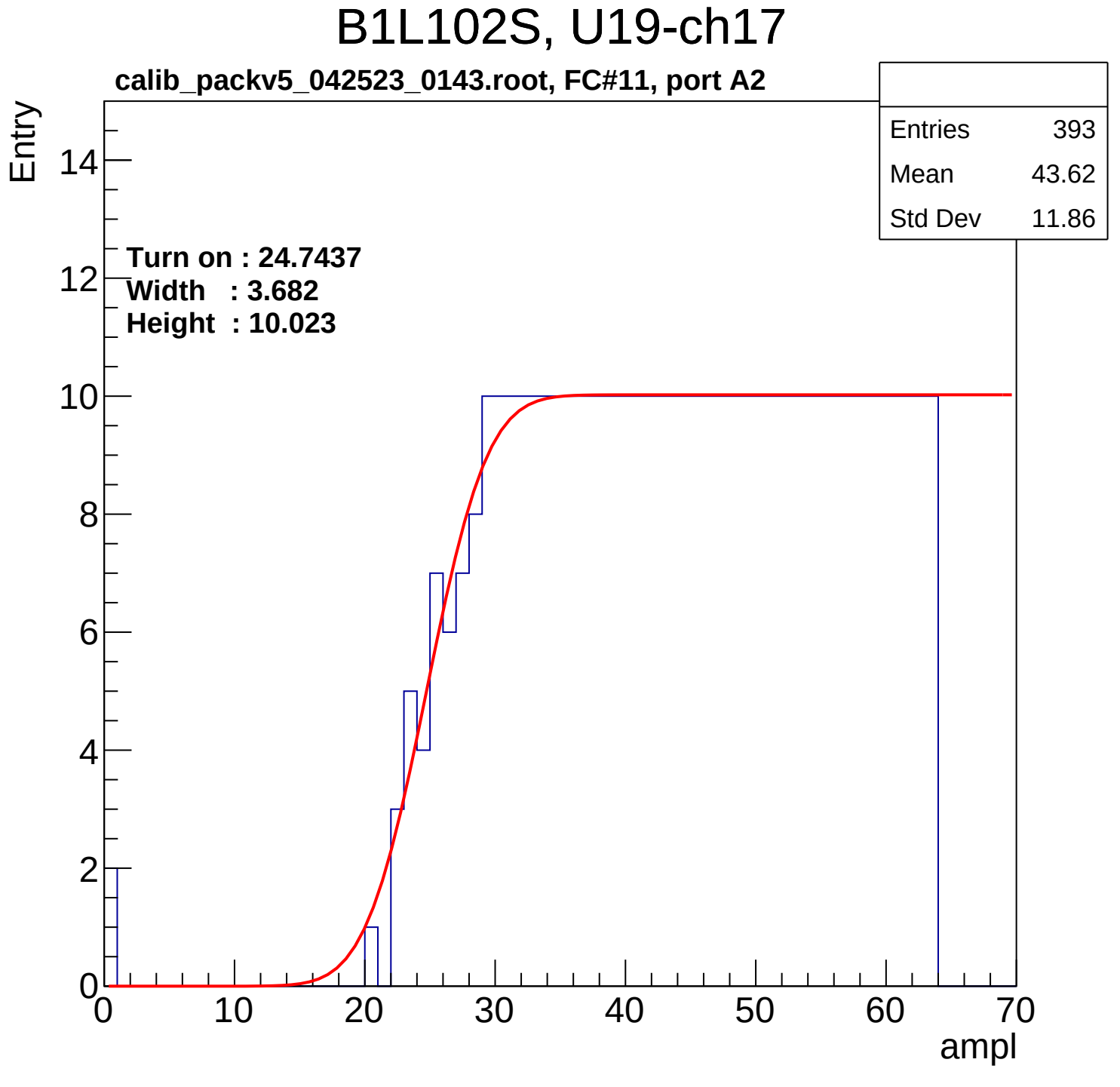

B1L102S, U19-ch12
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.9
Std Dev 11.6
Turn on : 25.5785
Width : 3.351
Height : 10.022
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

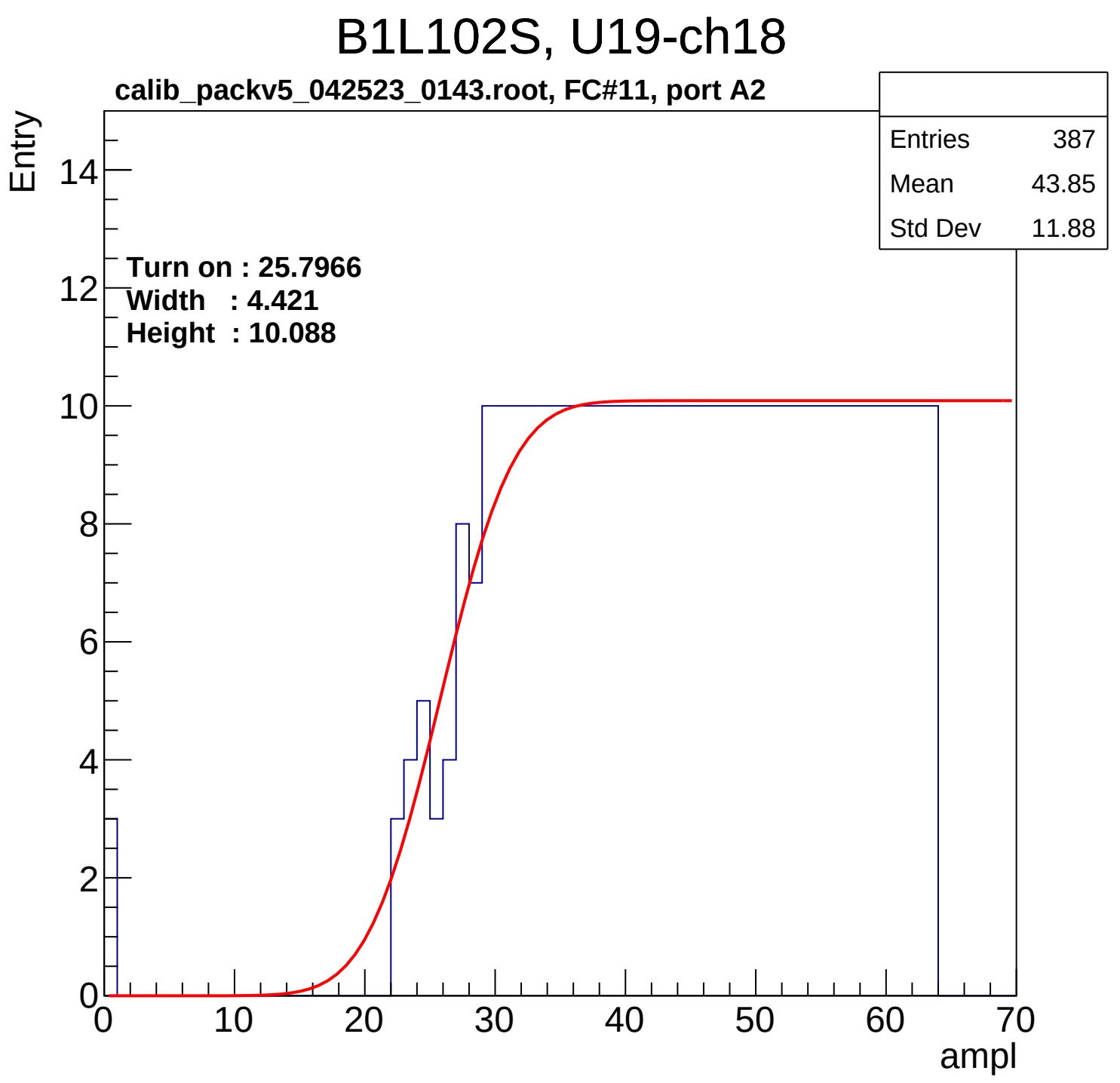

B1L102S, U19-ch13
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.06
Std Dev 11.62
Turn on : 25.9206
Width : 2.933
Height : 9.994
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

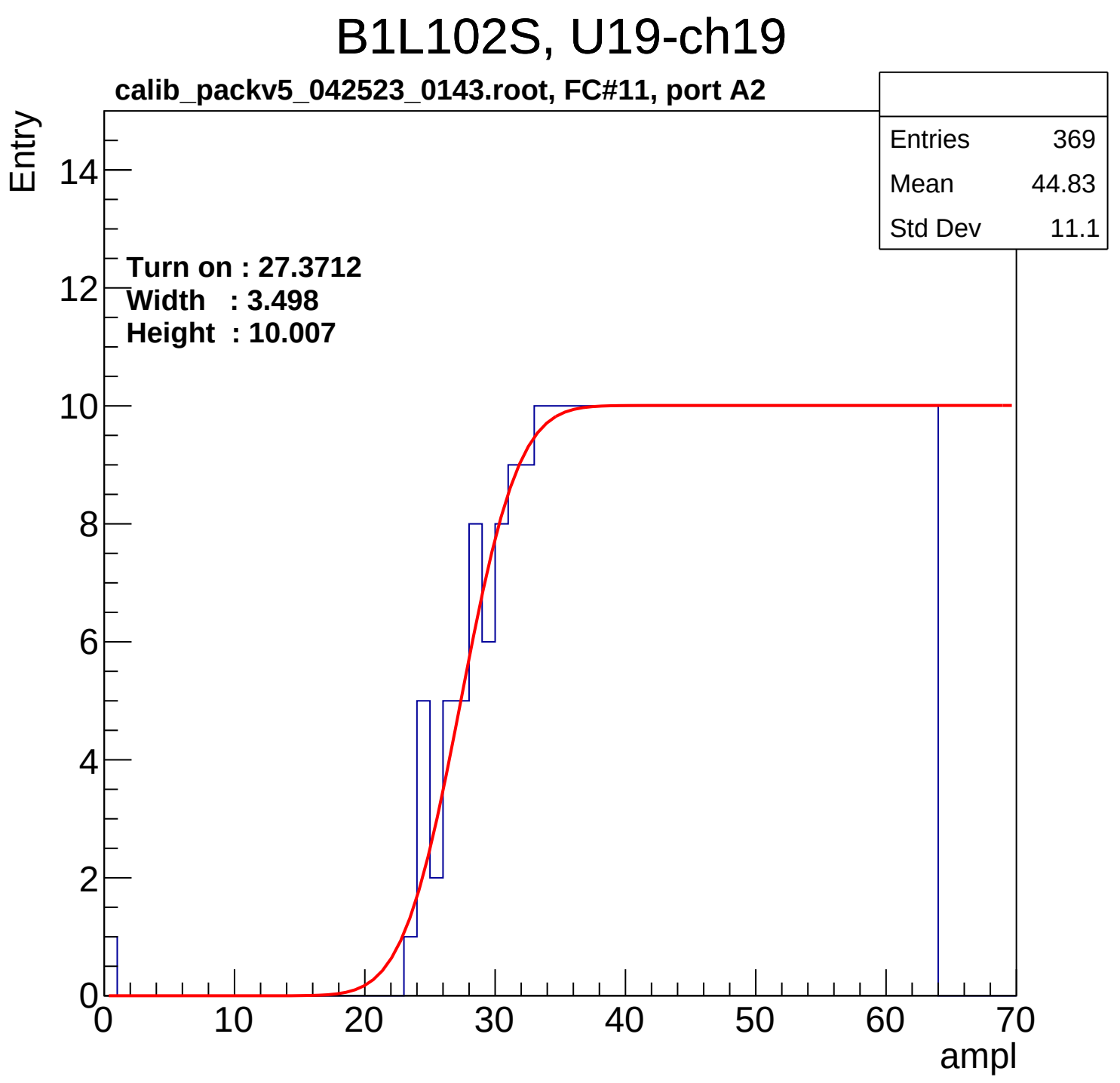

B1L102S, U19-ch14
calib_packv5_042523_0143.root, FC#11, port A2
Entries 404
Mean 42.99
Std Dev 12.39
Turn on : 23.9160
Width : 3.375
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

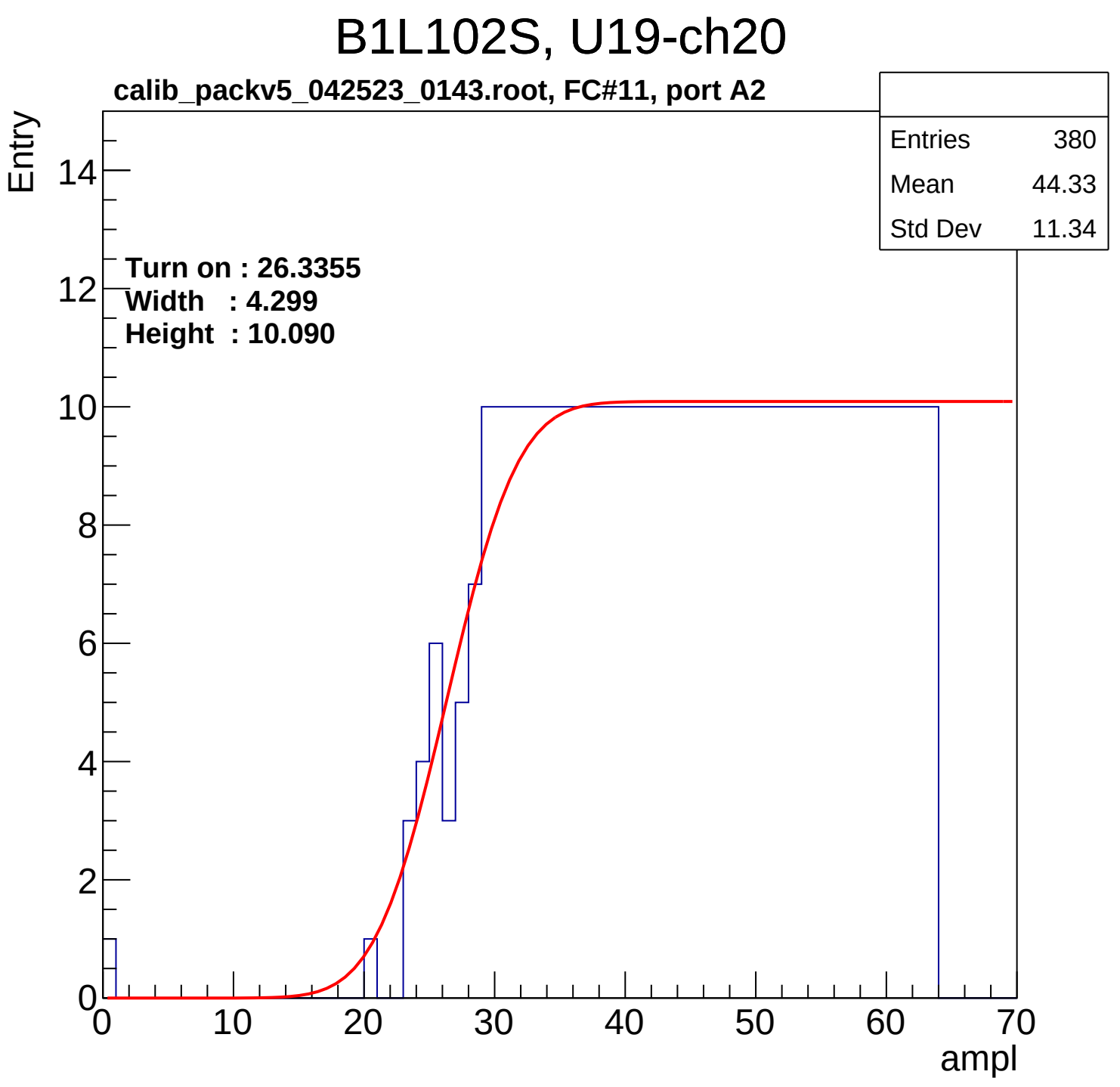

B1L102S, U19-ch15
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.31
Std Dev 11.49
Turn on : 26.6240
Width : 2.518
Height : 9.978
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

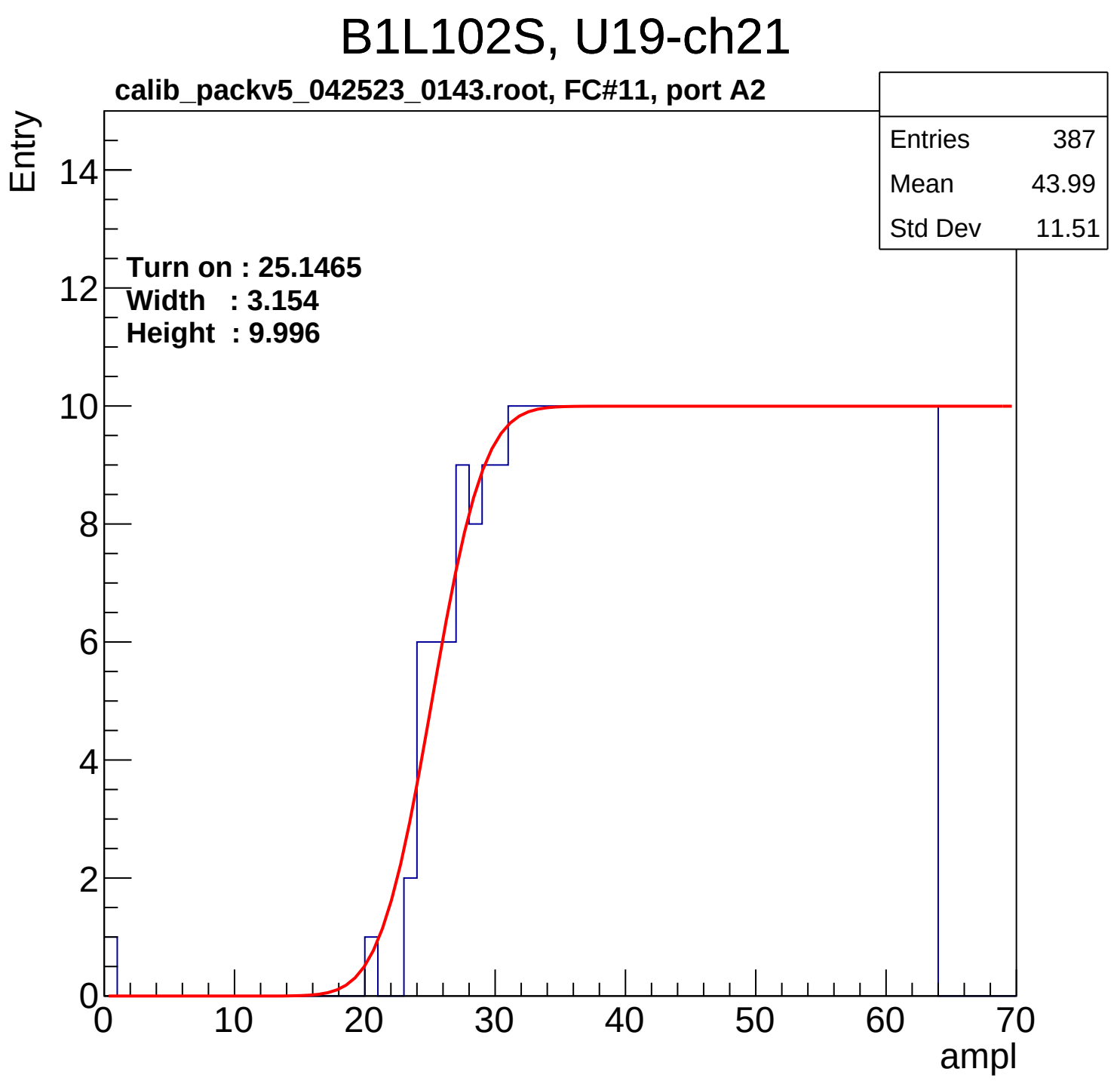

B1L102S, U19-ch16
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.16
Std Dev 11.45
Turn on : 26.5281
Width : 2.552
Height : 10.043
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

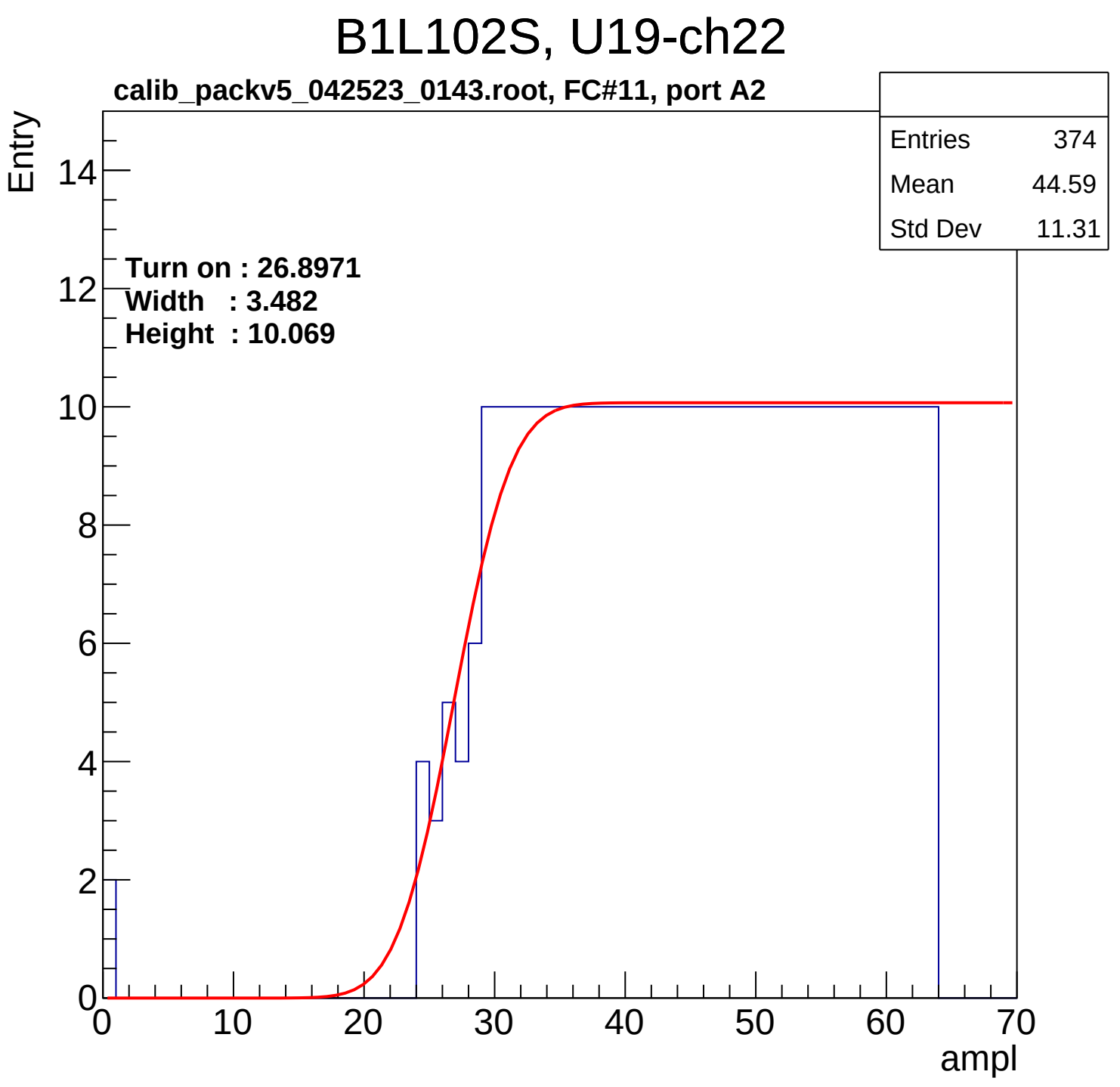

B1L102S, U19-ch17
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.62
Std Dev 11.86
Turn on : 24.7437
Width : 3.682
Height : 10.023
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

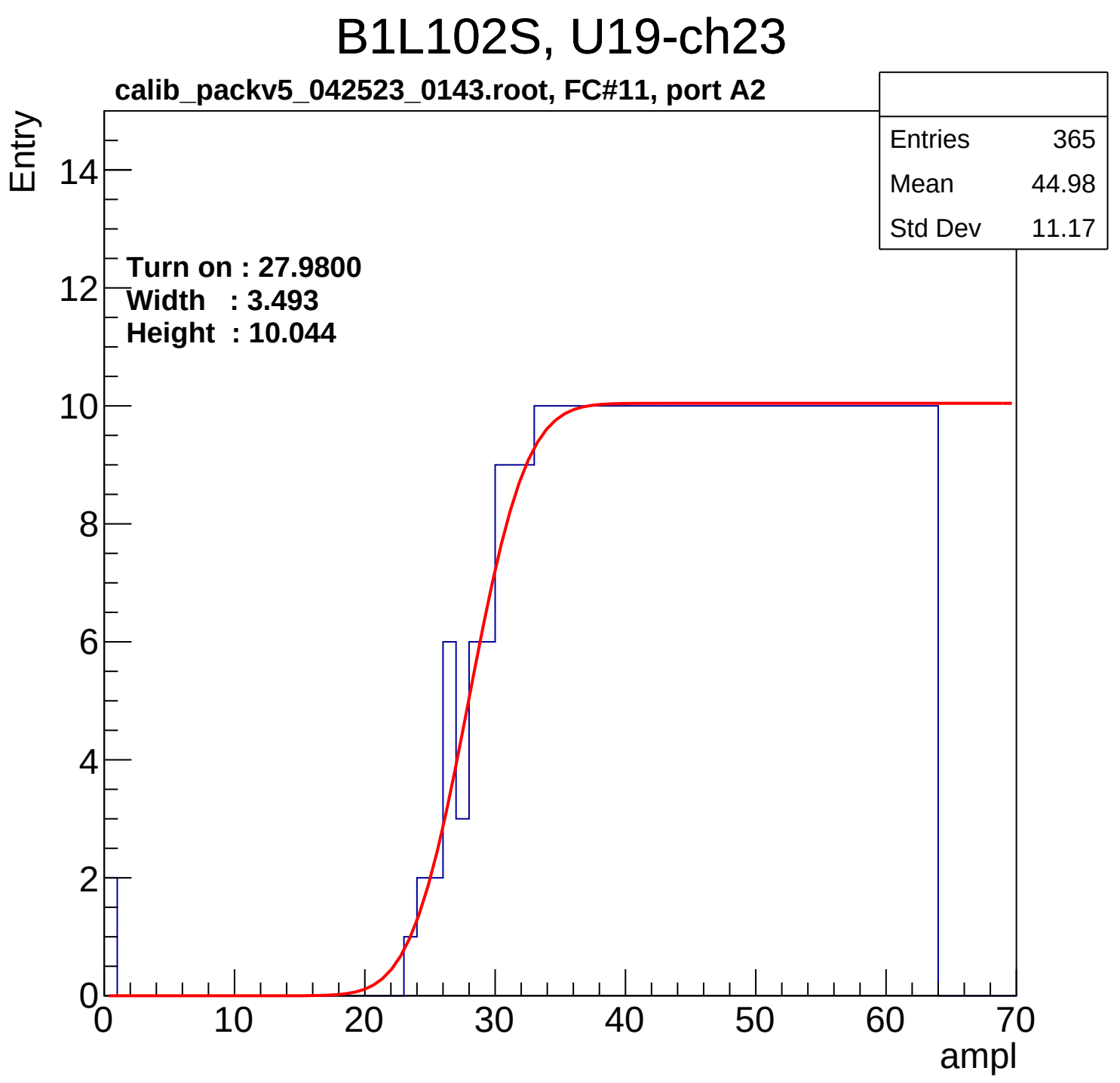

B1L102S, U19-ch18
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.85
Std Dev 11.88
Turn on : 25.7966
Width : 4.421
Height : 10.088
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

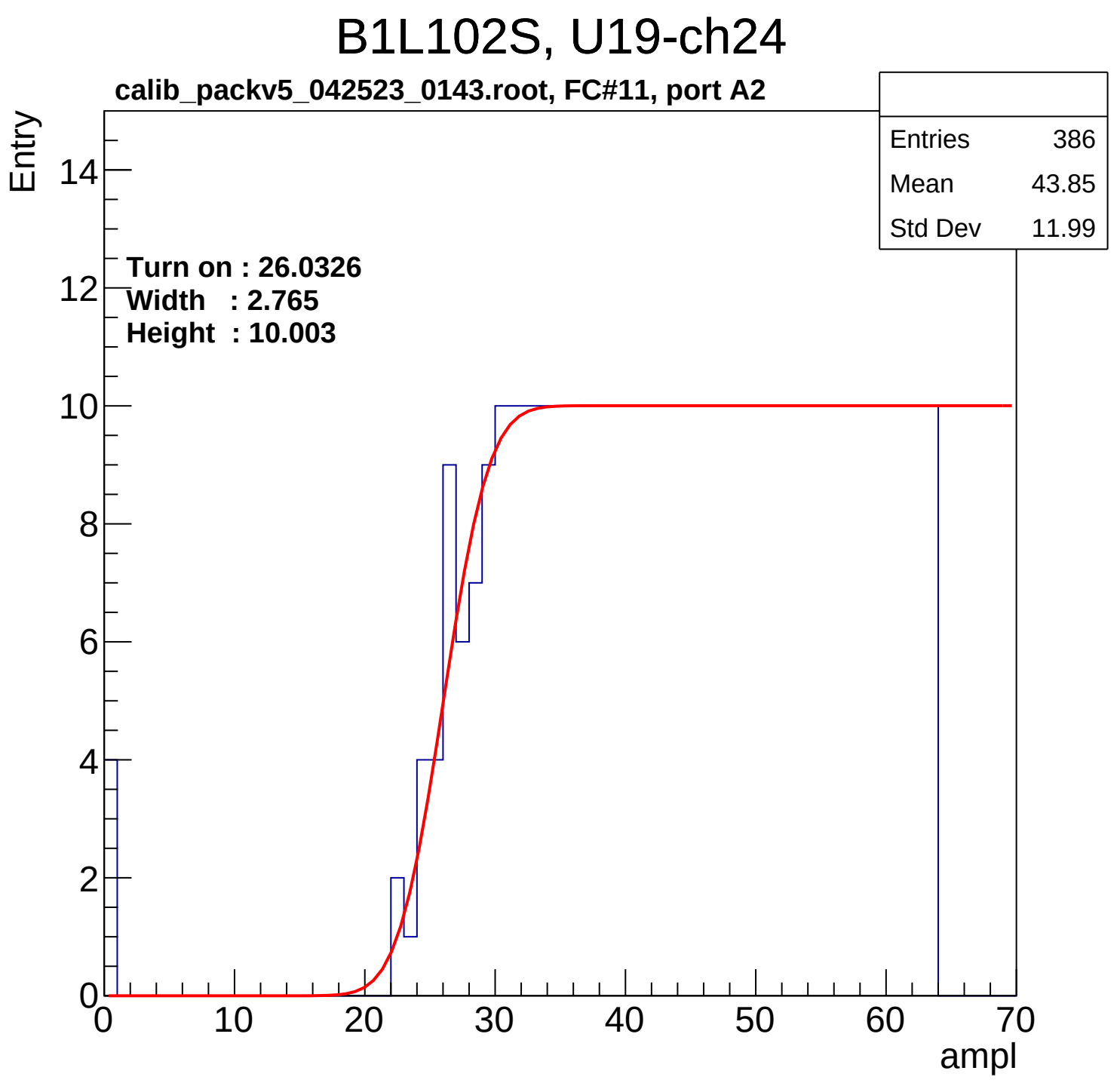

B1L102S, U19-ch19
calib_packv5_042523_0143.root, FC#11, port A2
Entries 369
Mean 44.83
Std Dev 11.1
Turn on : 27.3712
Width : 3.498
Height : 10.007
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

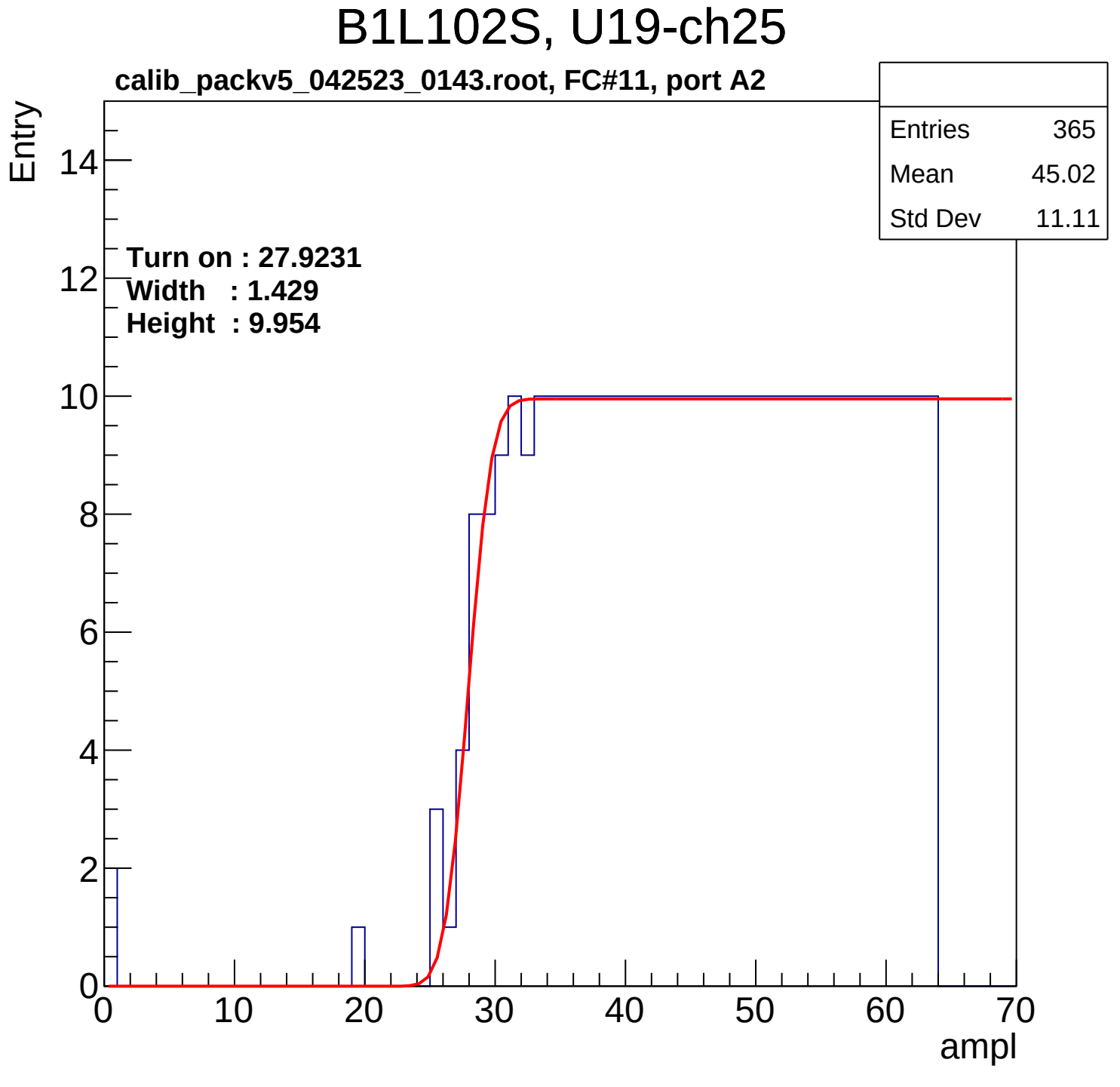

B1L102S, U19-ch20
calib_packv5_042523_0143.root, FC#11, port A2
Entries 380
Mean 44.33
Std Dev 11.34
Turn on : 26.3355
Width : 4.299
Height : 10.090
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

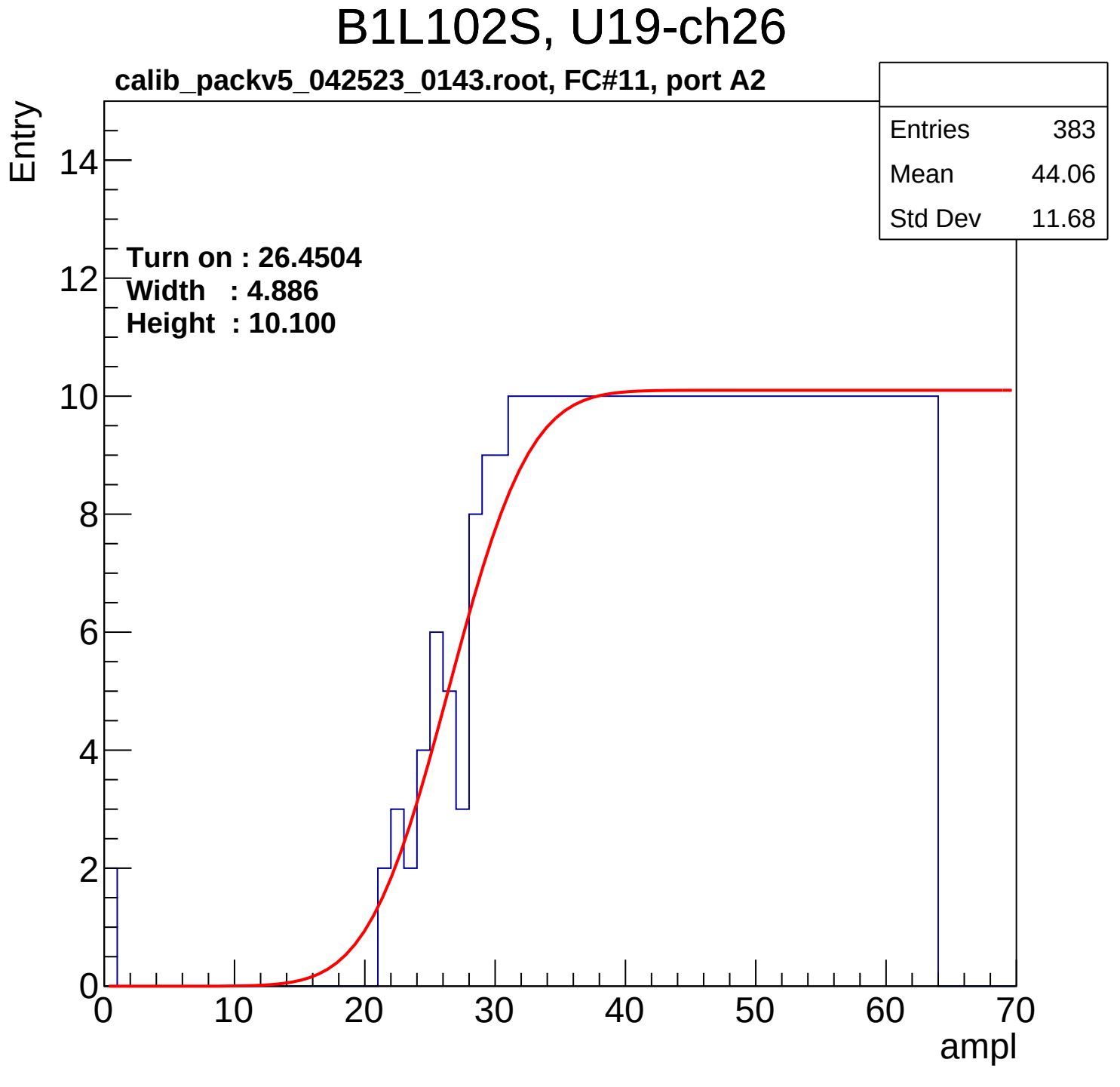

B1L102S, U19-ch21
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.99
Std Dev 11.51
Turn on : 25.1465
Width : 3.154
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

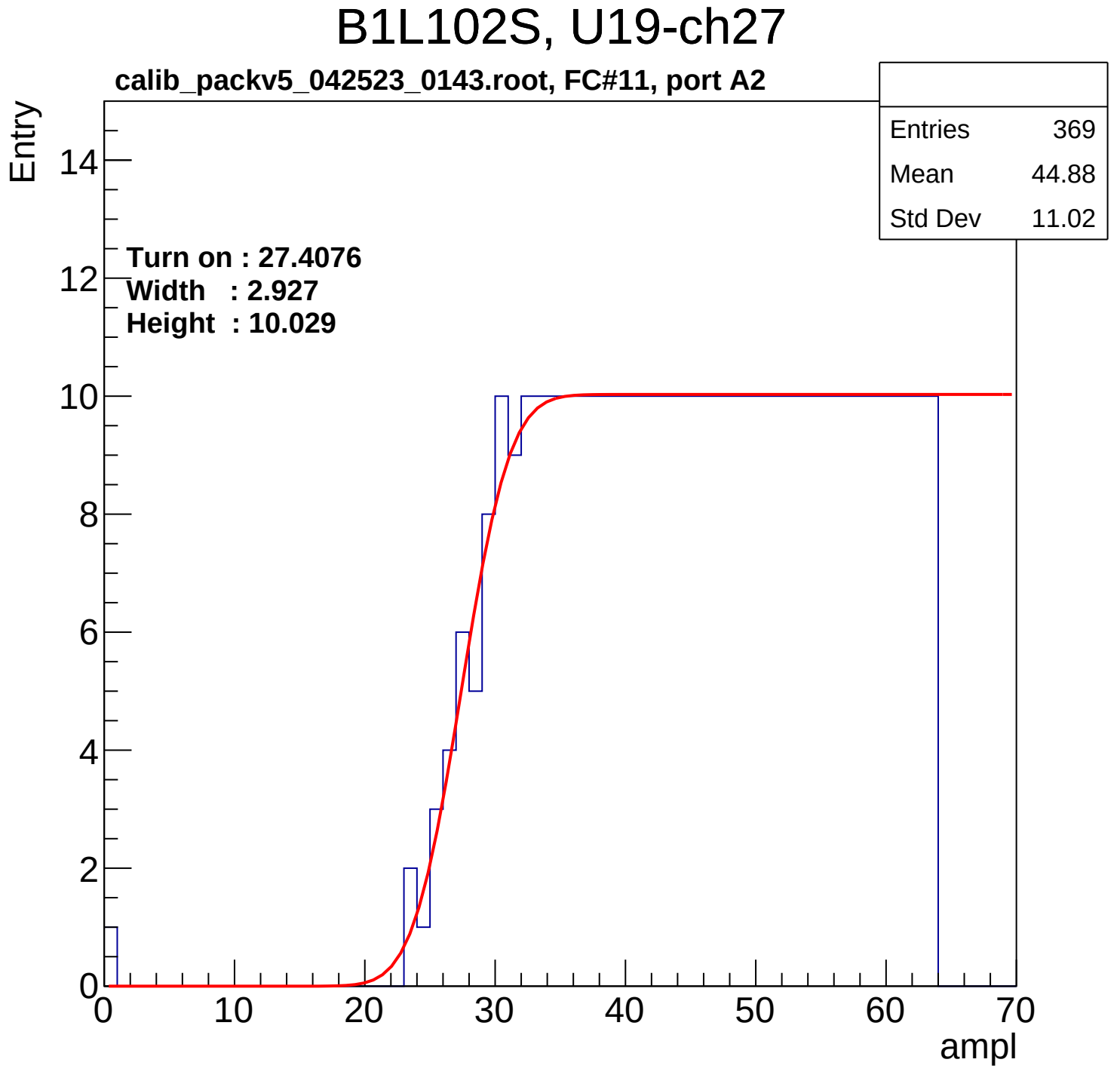

B1L102S, U19-ch22
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.59
Std Dev 11.31
Turn on : 26.8971
Width : 3.482
Height : 10.069
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

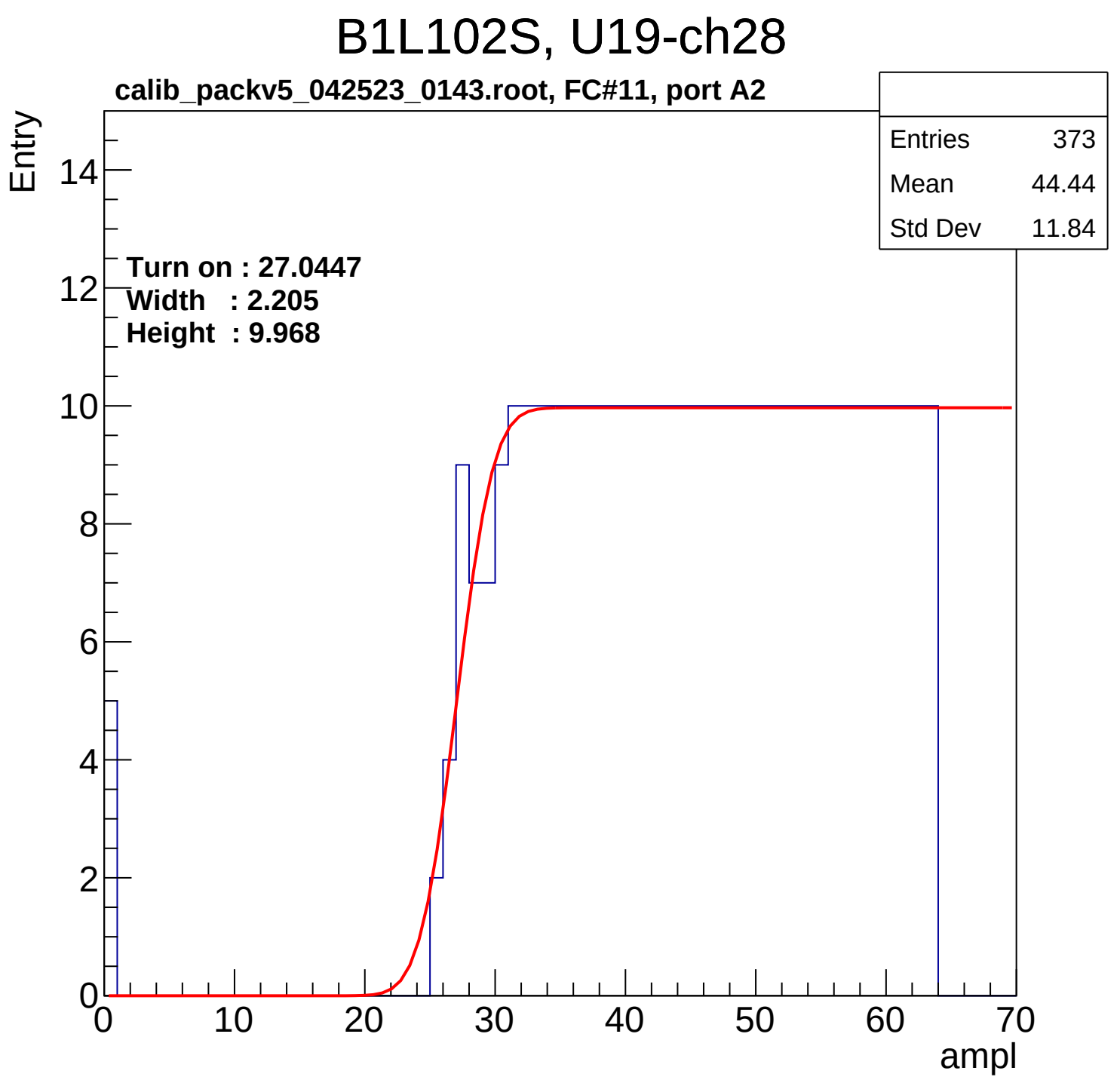

B1L102S, U19-ch23
calib_packv5_042523_0143.root, FC#11, port A2
Entries 365
Mean 44.98
Std Dev 11.17
Turn on : 27.9800
Width : 3.493
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

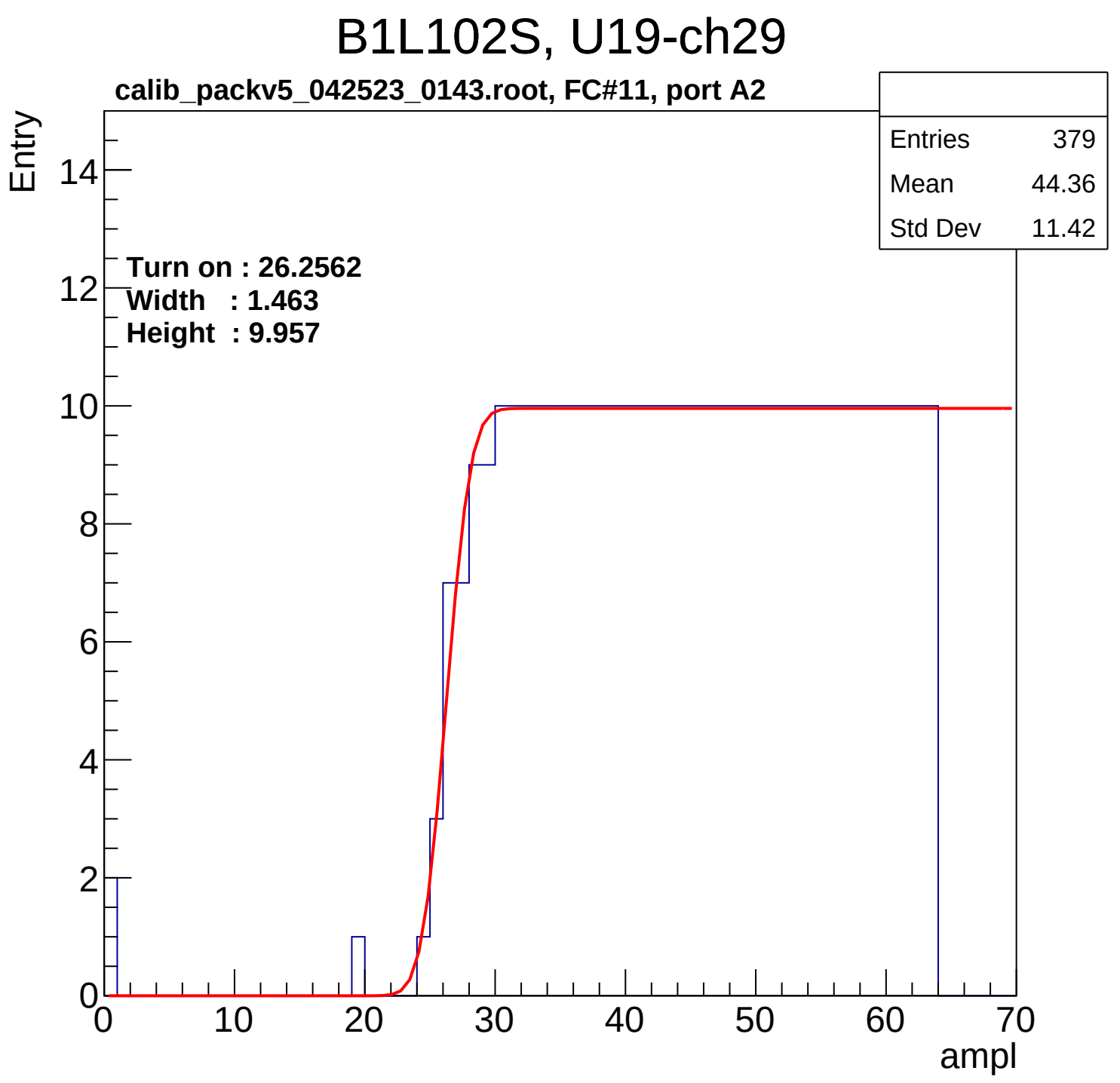

B1L102S, U19-ch24
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.85
Std Dev 11.99
Turn on : 26.0326
Width : 2.765
Height : 10.003
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

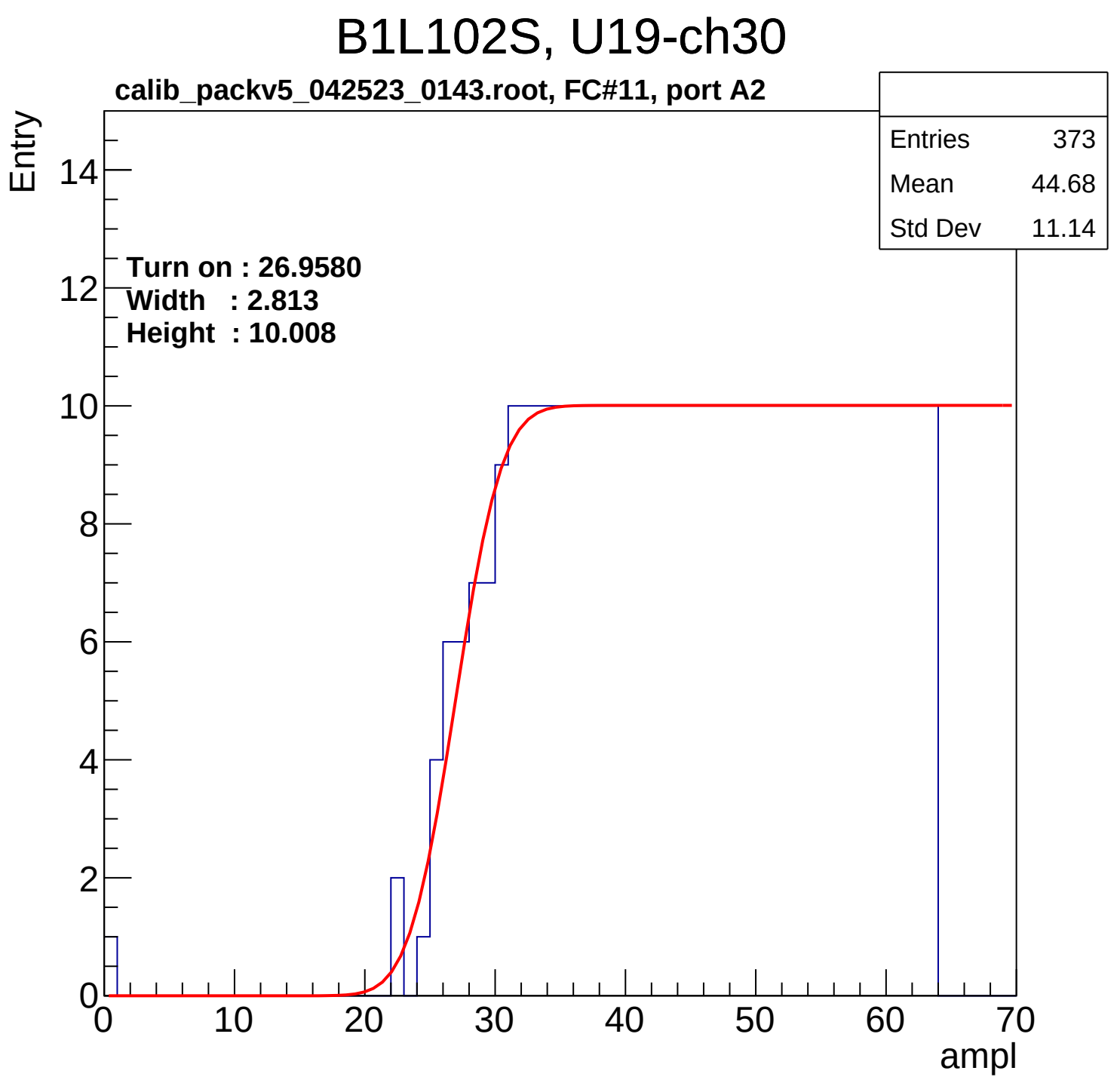

B1L102S, U19-ch25
calib_packv5_042523_0143.root, FC#11, port A2
Entries 365
Mean 45.02
Std Dev 11.11
Turn on : 27.9231
Width : 1.429
Height : 9.954
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

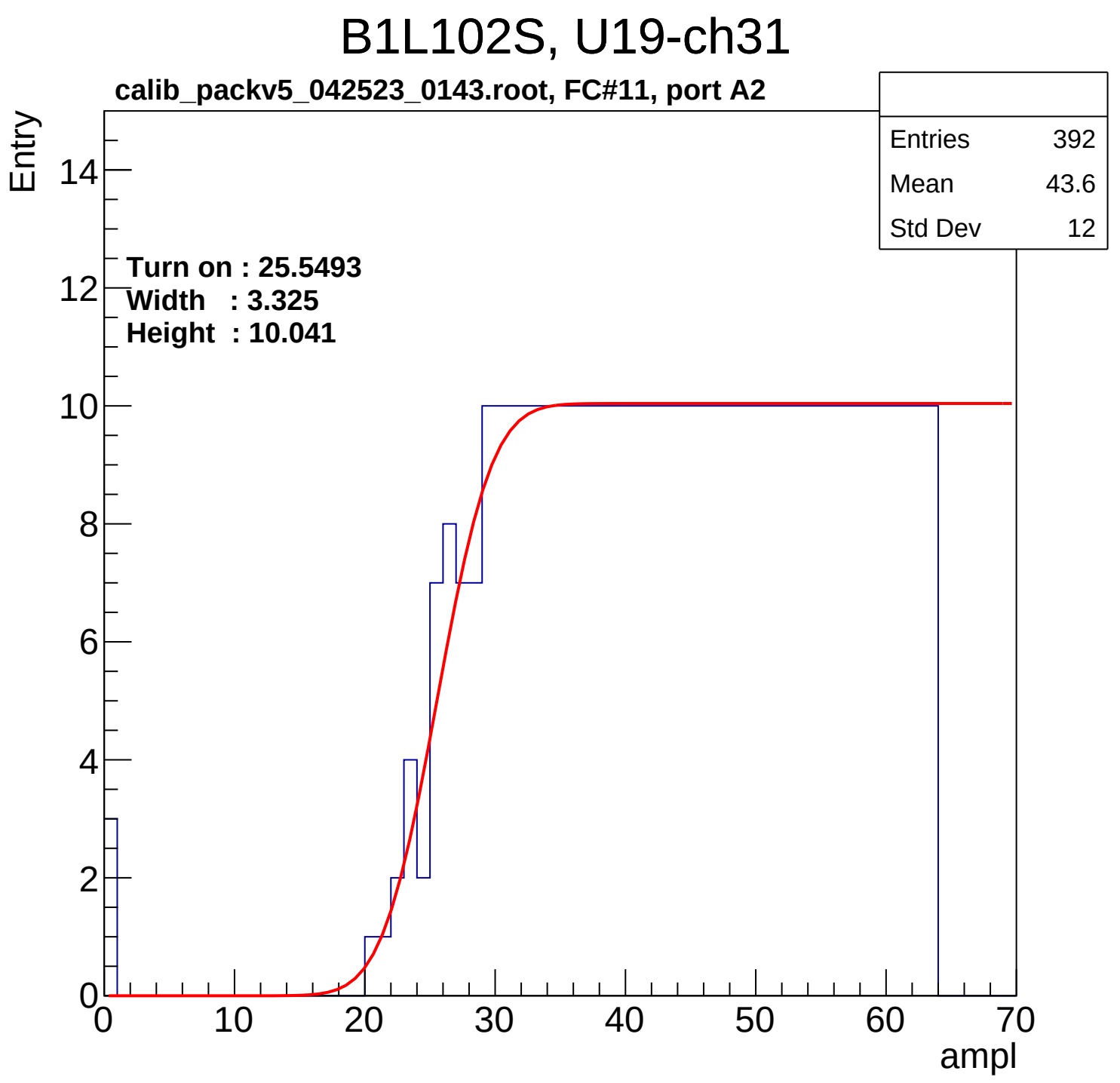

B1L102S, U19-ch26
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.06
Std Dev 11.68
Turn on : 26.4504
Width : 4.886
Height : 10.100
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

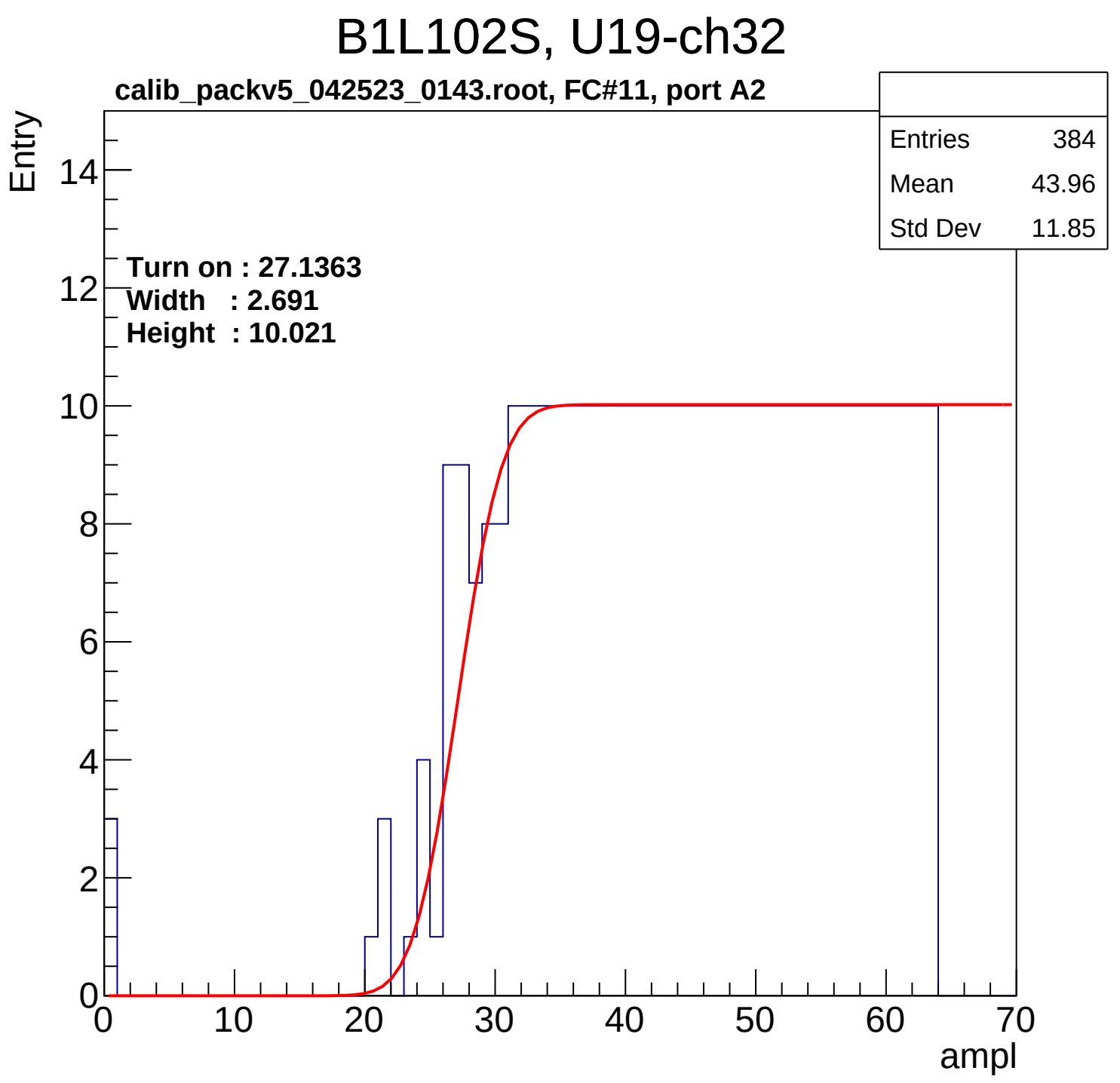

B1L102S, U19-ch27
calib_packv5_042523_0143.root, FC#11, port A2
Entries 369
Mean 44.88
Std Dev 11.02
Turn on : 27.4076
Width : 2.927
Height : 10.029
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

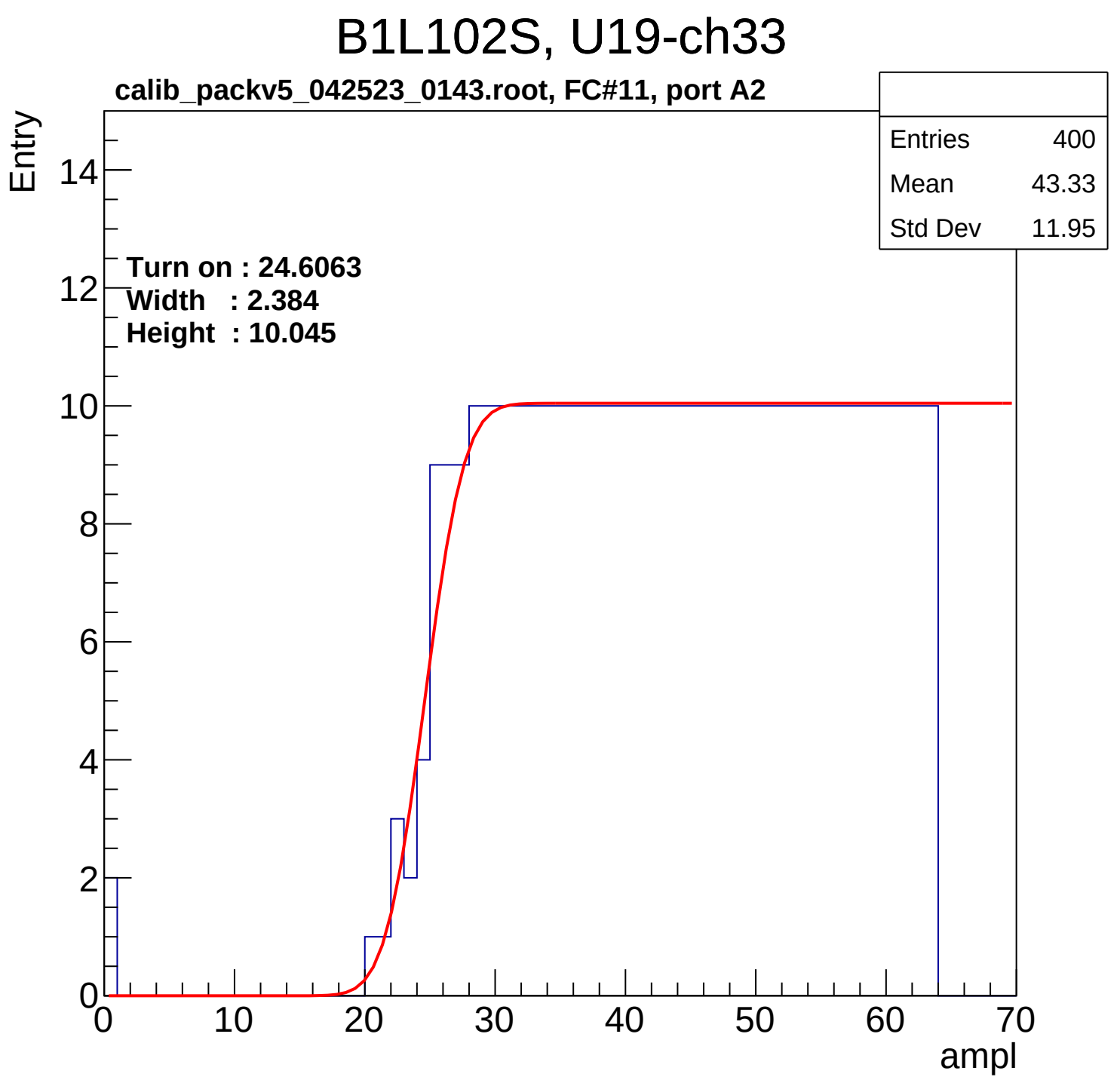

B1L102S, U19-ch28
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.44
Std Dev 11.84
Turn on : 27.0447
Width : 2.205
Height : 9.968
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

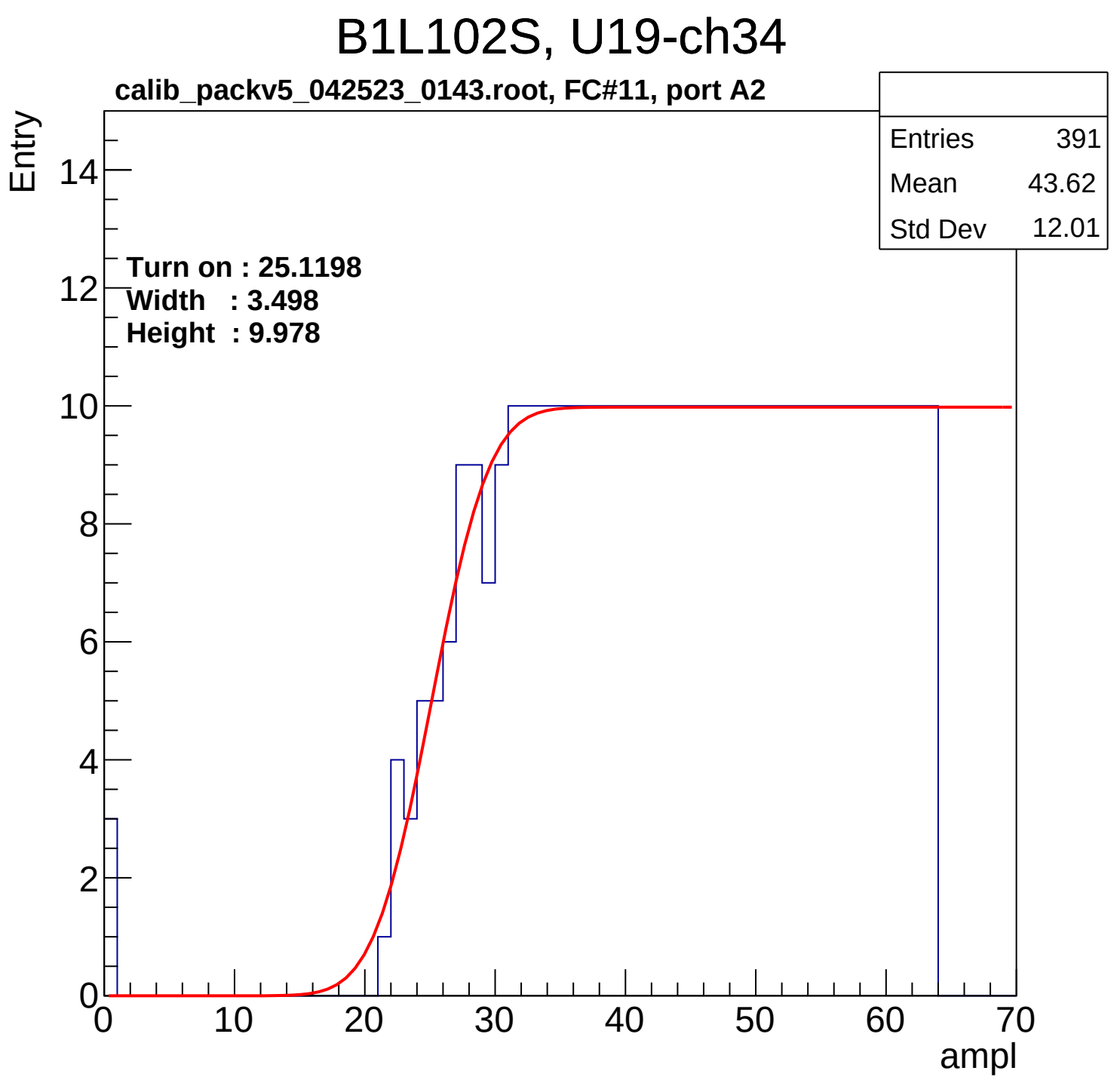

B1L102S, U19-ch29
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.36
Std Dev 11.42
Turn on : 26.2562
Width : 1.463
Height : 9.957
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

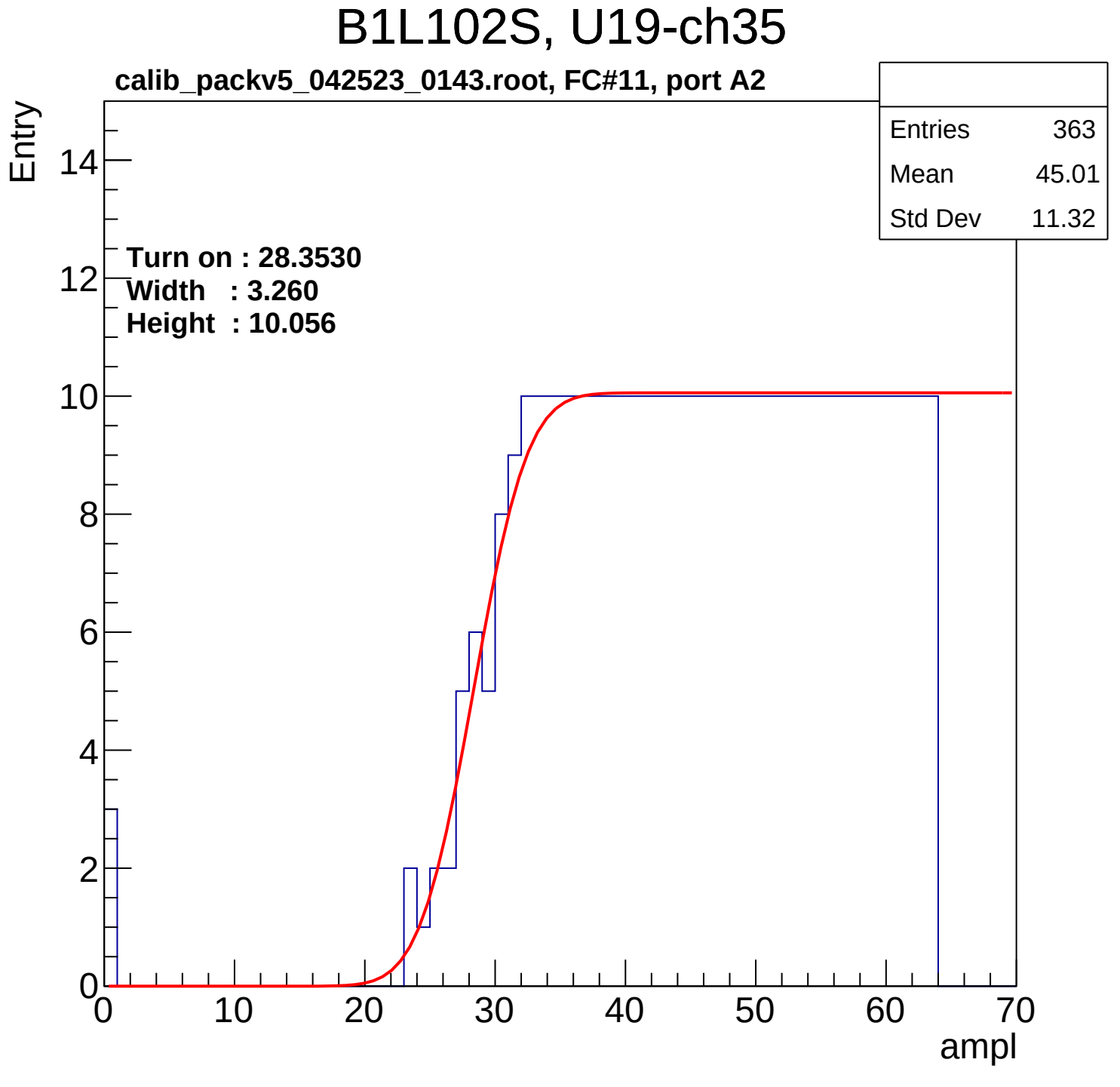

B1L102S, U19-ch30
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.68
Std Dev 11.14
Turn on : 26.9580
Width : 2.813
Height : 10.008
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

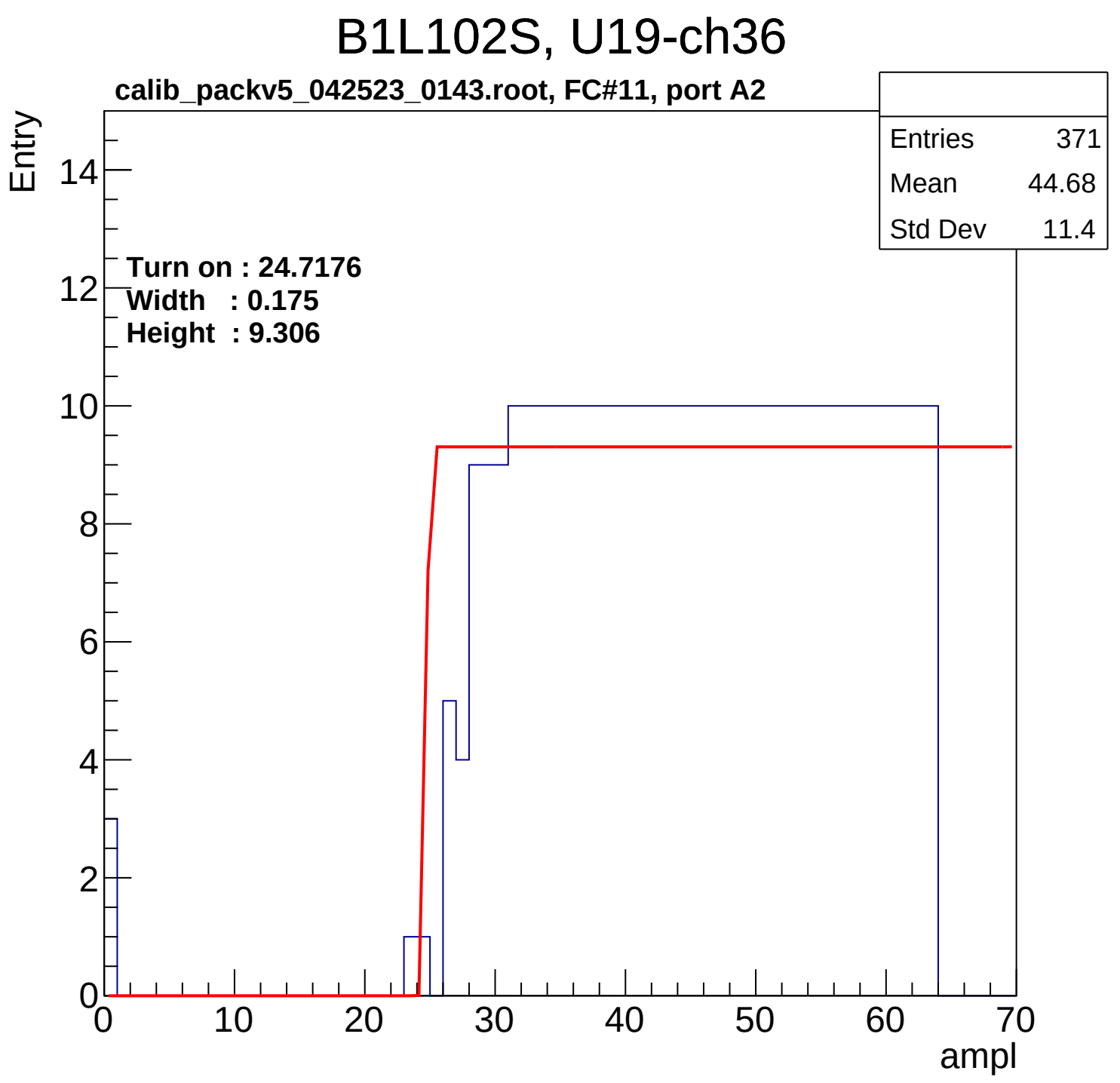

B1L102S, U19-ch31
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.6
Std Dev 12
Turn on : 25.5493
Width : 3.325
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

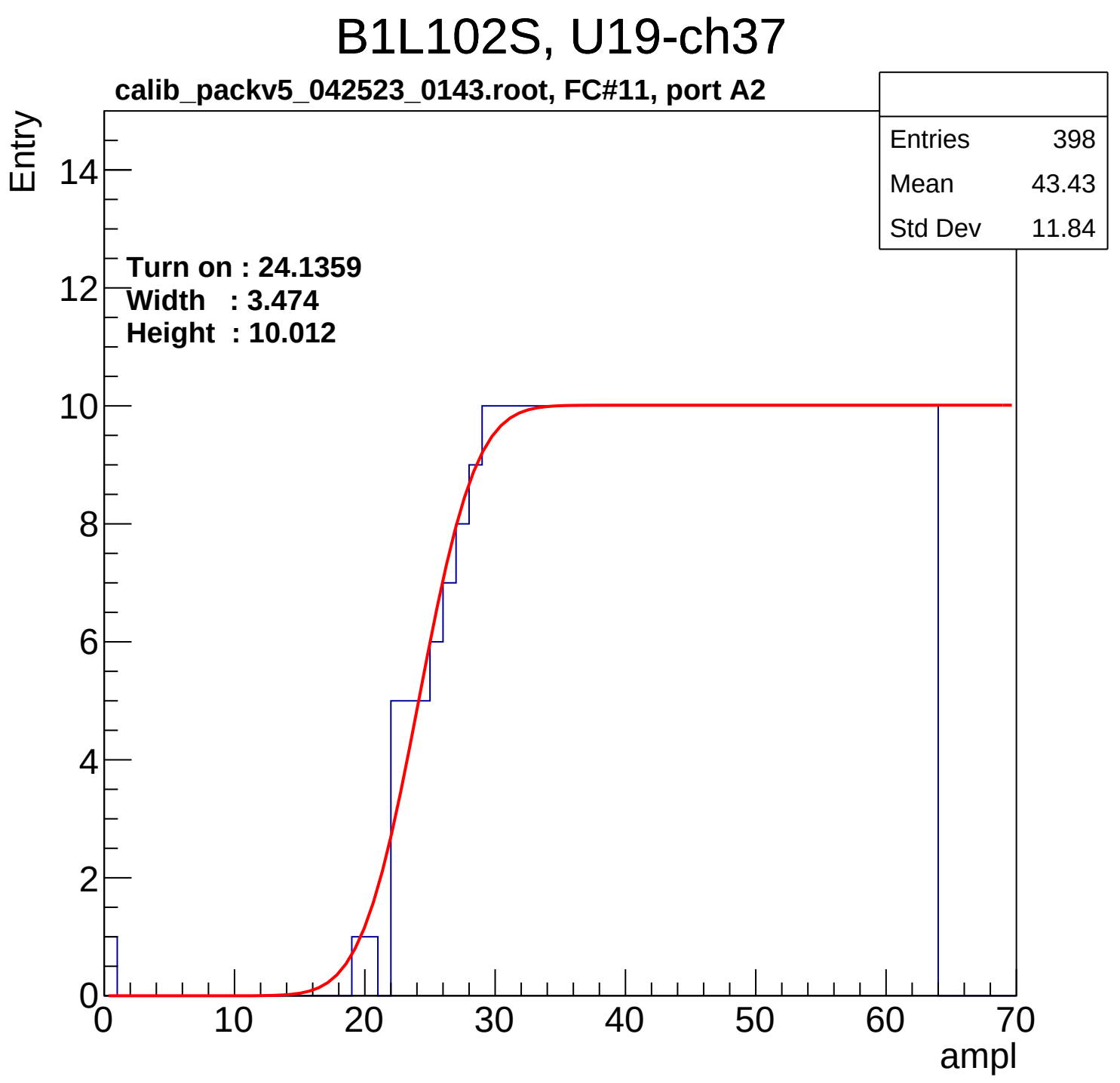

B1L102S, U19-ch32
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 43.96
Std Dev 11.85
Turn on : 27.1363
Width : 2.691
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

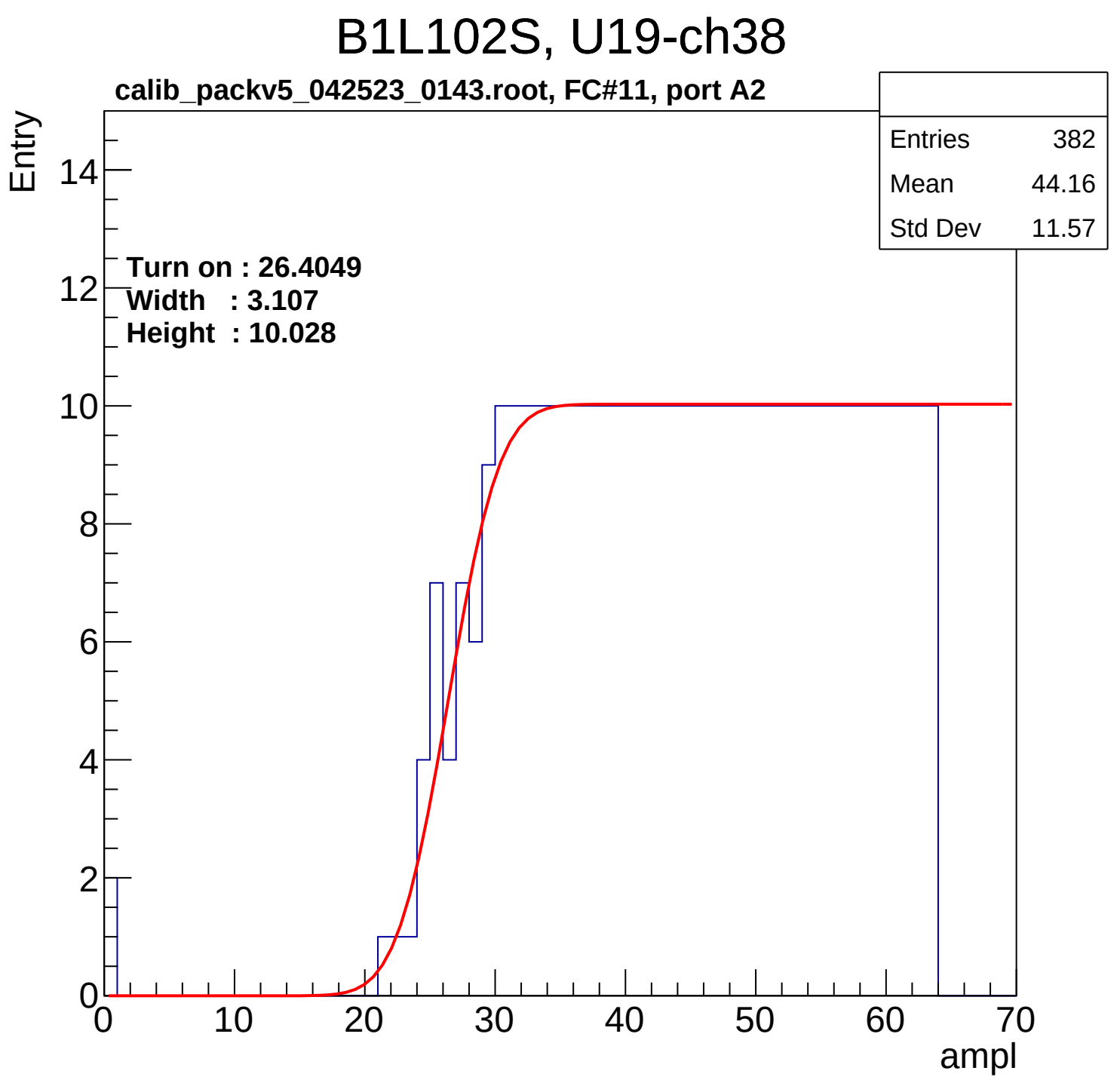

B1L102S, U19-ch33
calib_packv5_042523_0143.root, FC#11, port A2
Entries 400
Mean 43.33
Std Dev 11.95
Turn on : 24.6063
Width : 2.384
Height : 10.045
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

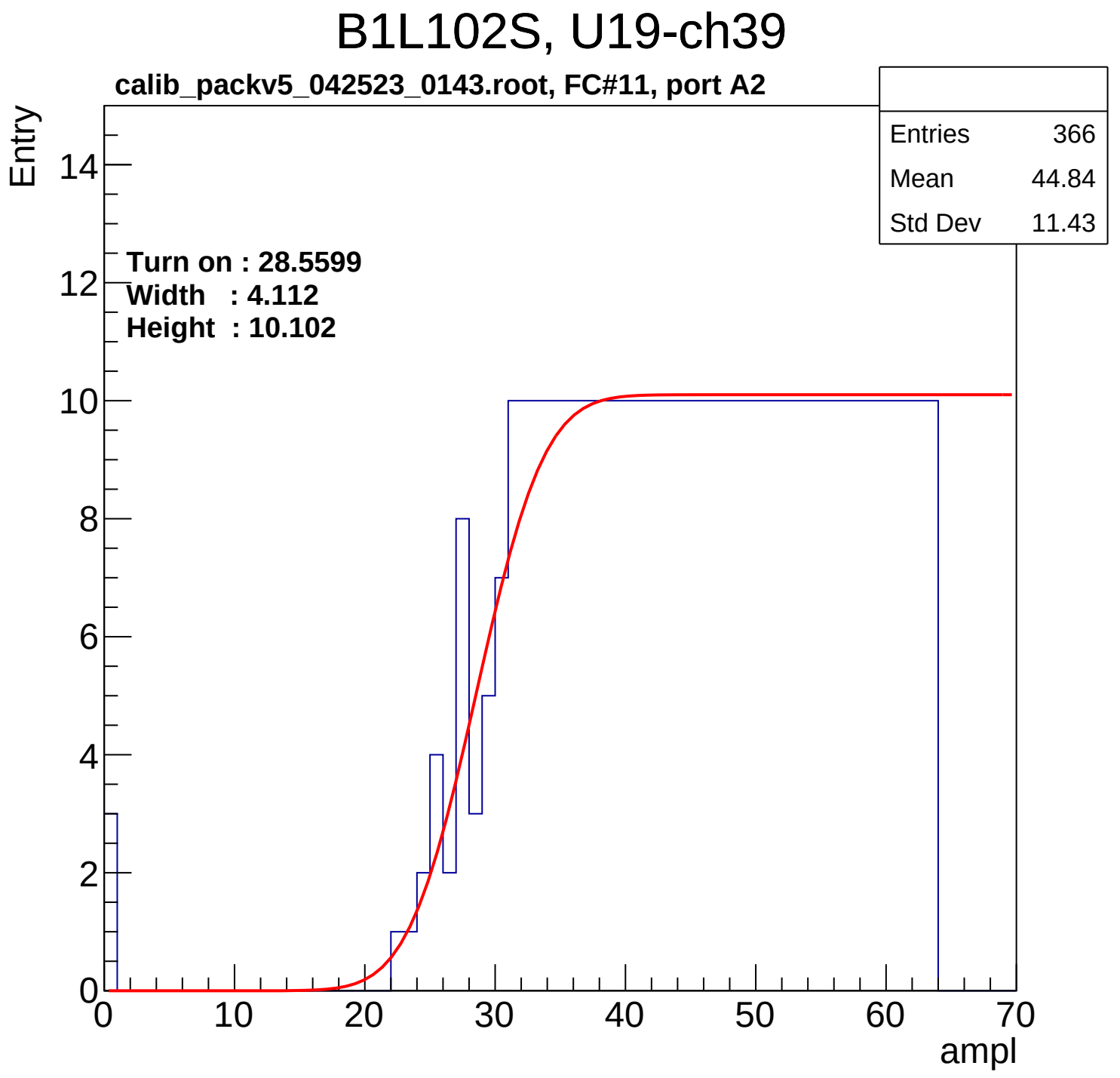

B1L102S, U19-ch34
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.62
Std Dev 12.01
Turn on : 25.1198
Width : 3.498
Height : 9.978
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

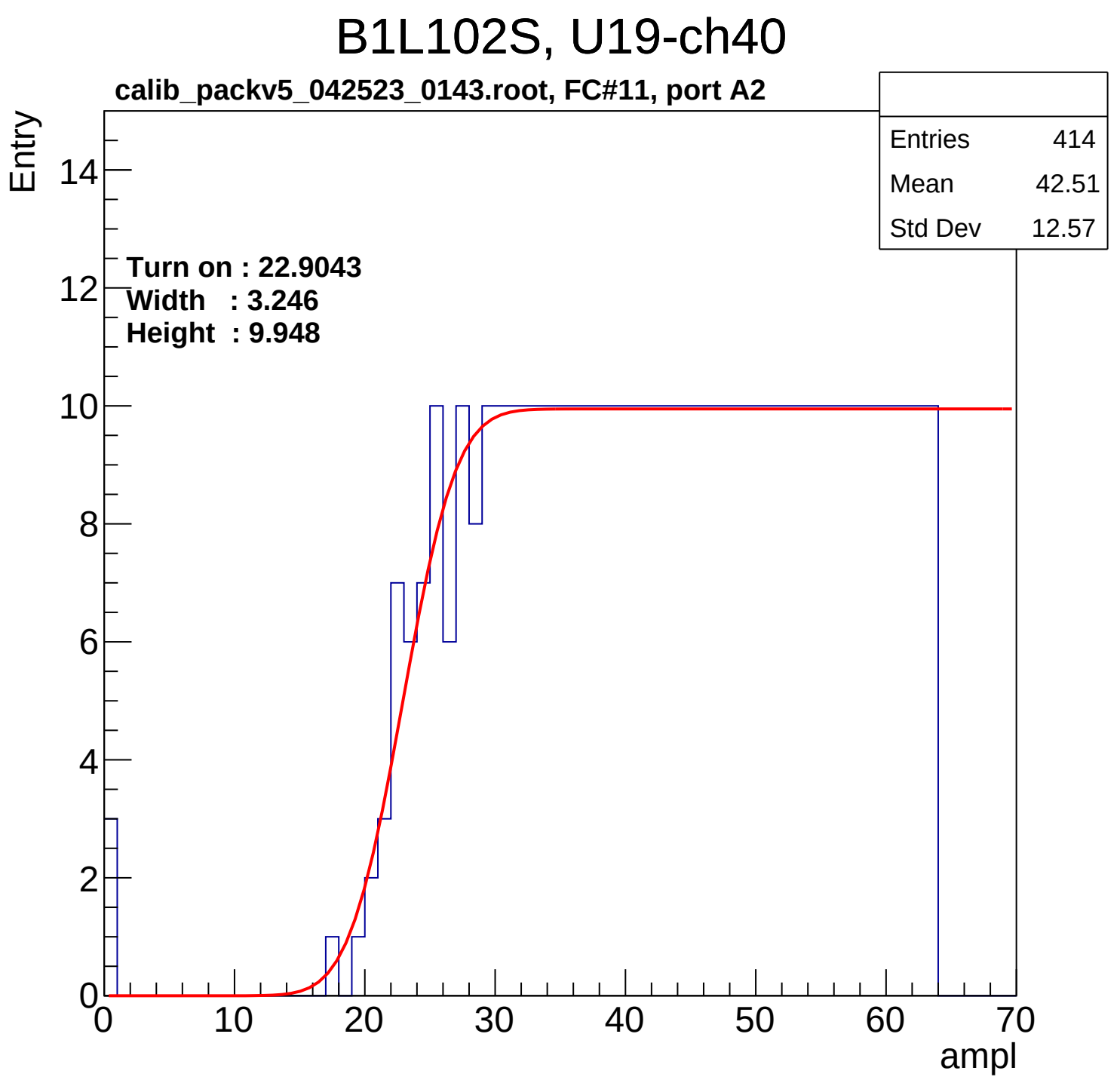

B1L102S, U19-ch35
calib_packv5_042523_0143.root, FC#11, port A2
Entries 363
Mean 45.01
Std Dev 11.32
Turn on : 28.3530
Width : 3.260
Height : 10.056
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

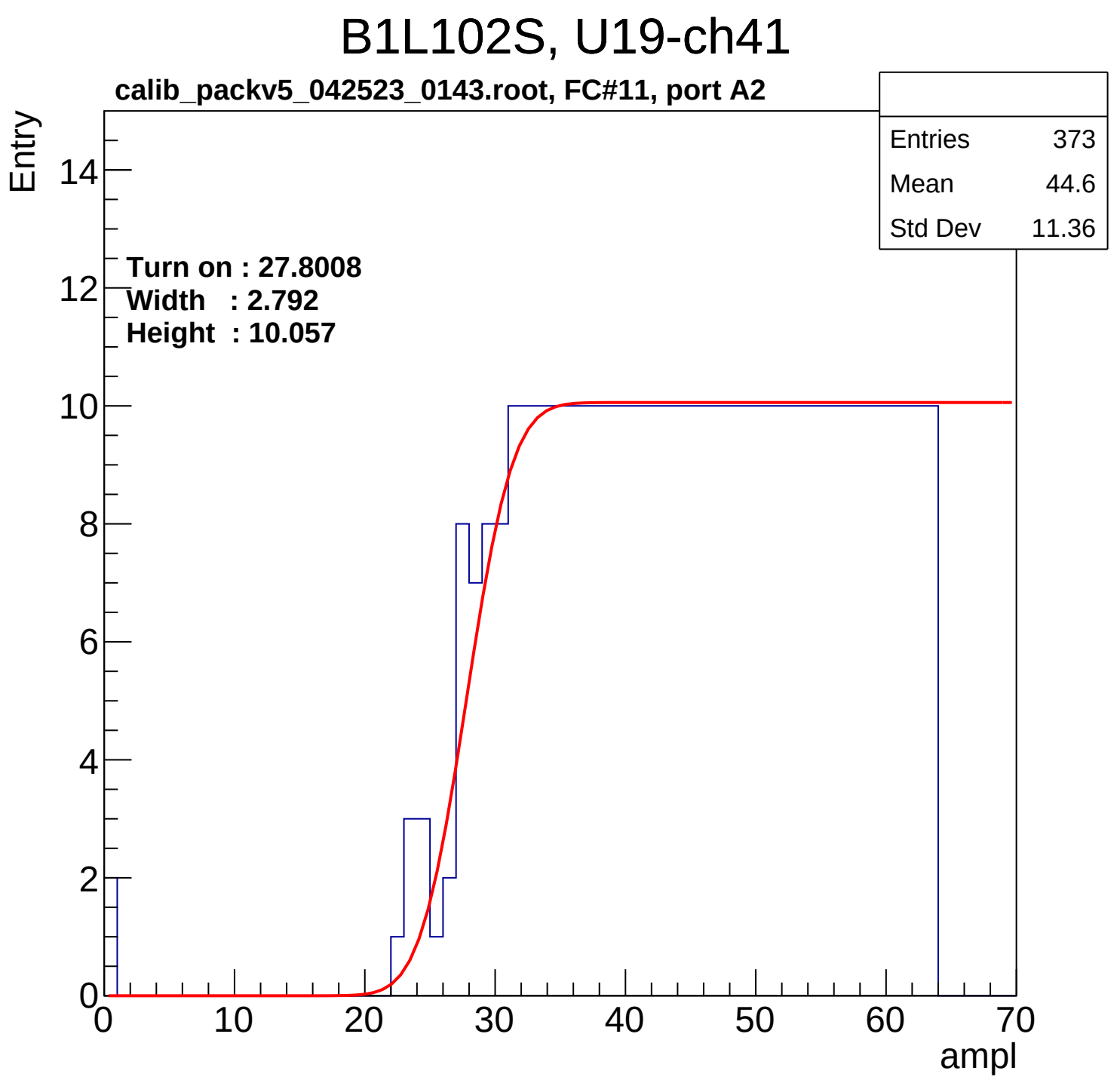

B1L102S, U19-ch36
calib_packv5_042523_0143.root, FC#11, port A2
Entries 371
Mean 44.68
Std Dev 11.4
Turn on : 24.7176
Width : 0.175
Height : 9.306
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

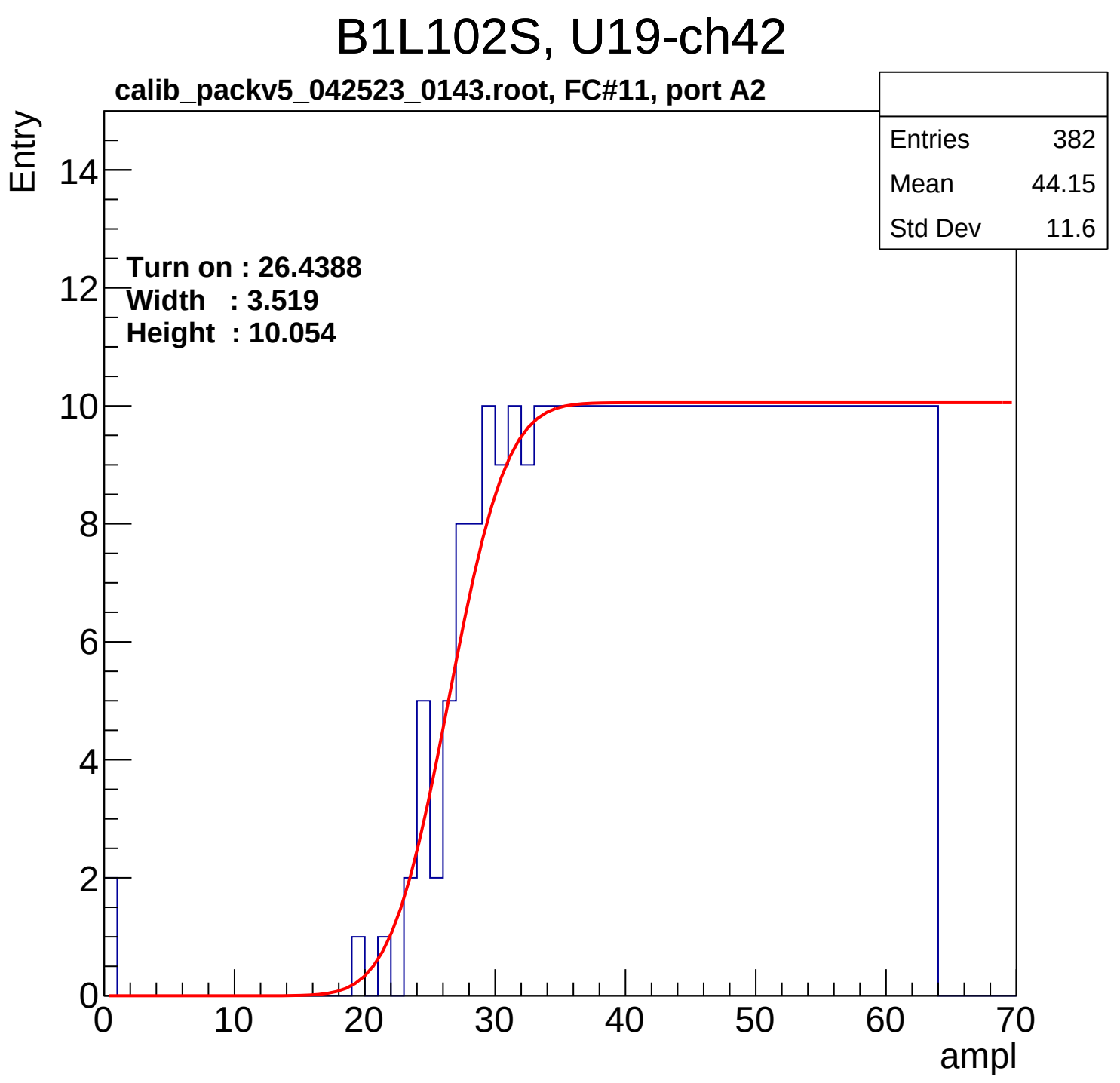

B1L102S, U19-ch37
calib_packv5_042523_0143.root, FC#11, port A2
Entries 398
Mean 43.43
Std Dev 11.84
Turn on : 24.1359
Width : 3.474
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

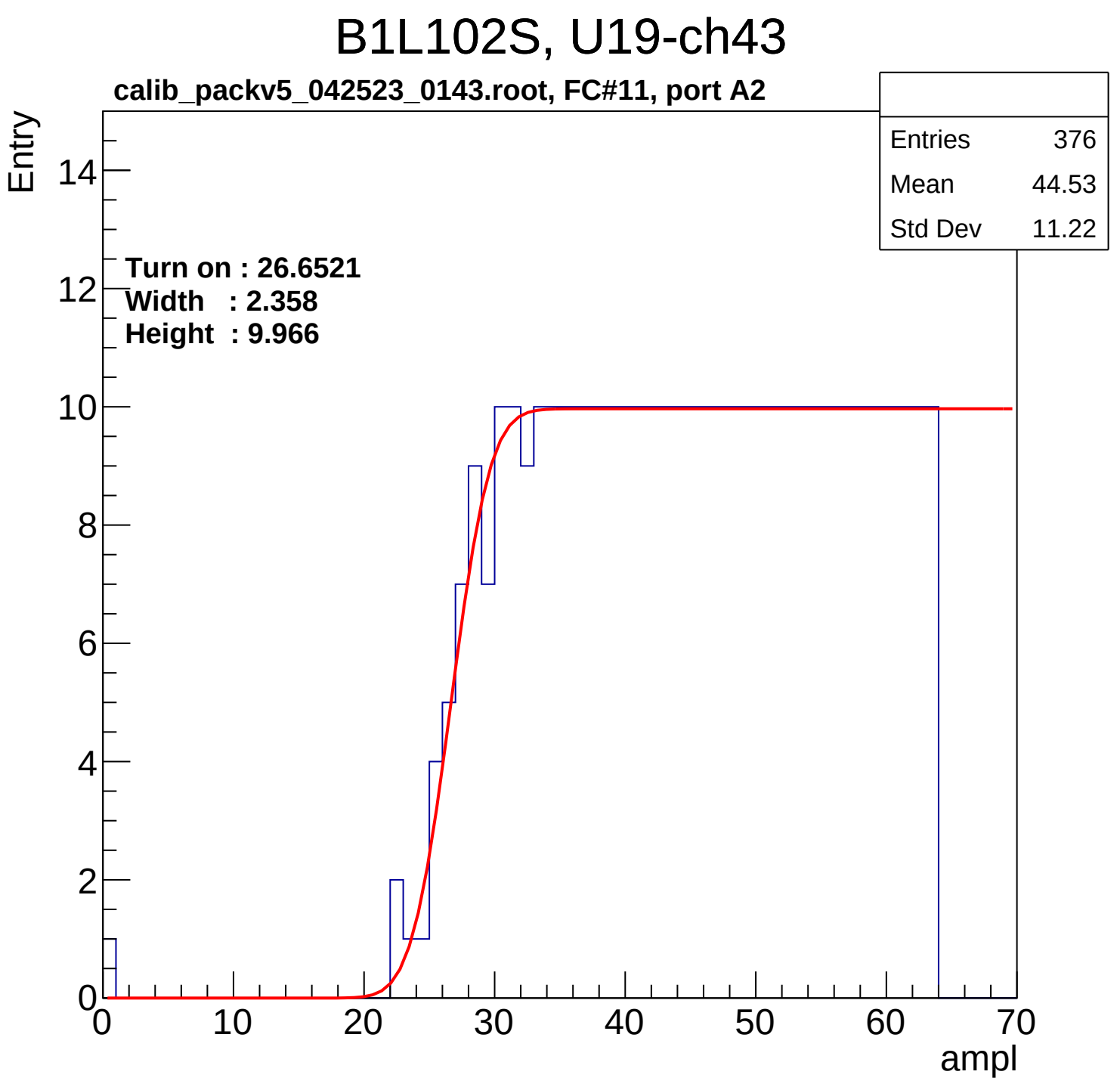

B1L102S, U19-ch38
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.16
Std Dev 11.57
Turn on : 26.4049
Width : 3.107
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

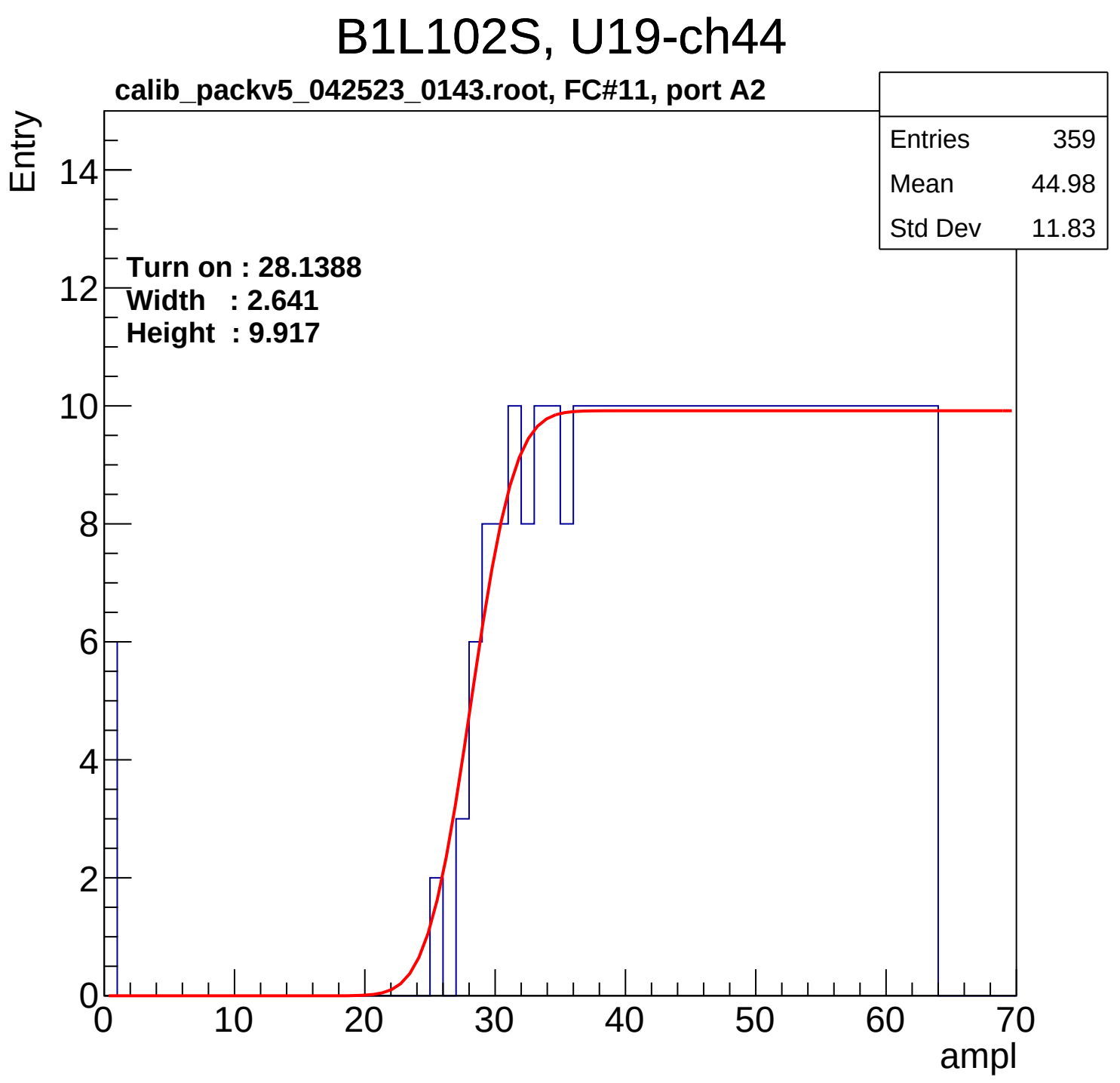

B1L102S, U19-ch39
calib_packv5_042523_0143.root, FC#11, port A2
Entries 366
Mean 44.84
Std Dev 11.43
Turn on : 28.5599
Width : 4.112
Height : 10.102
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

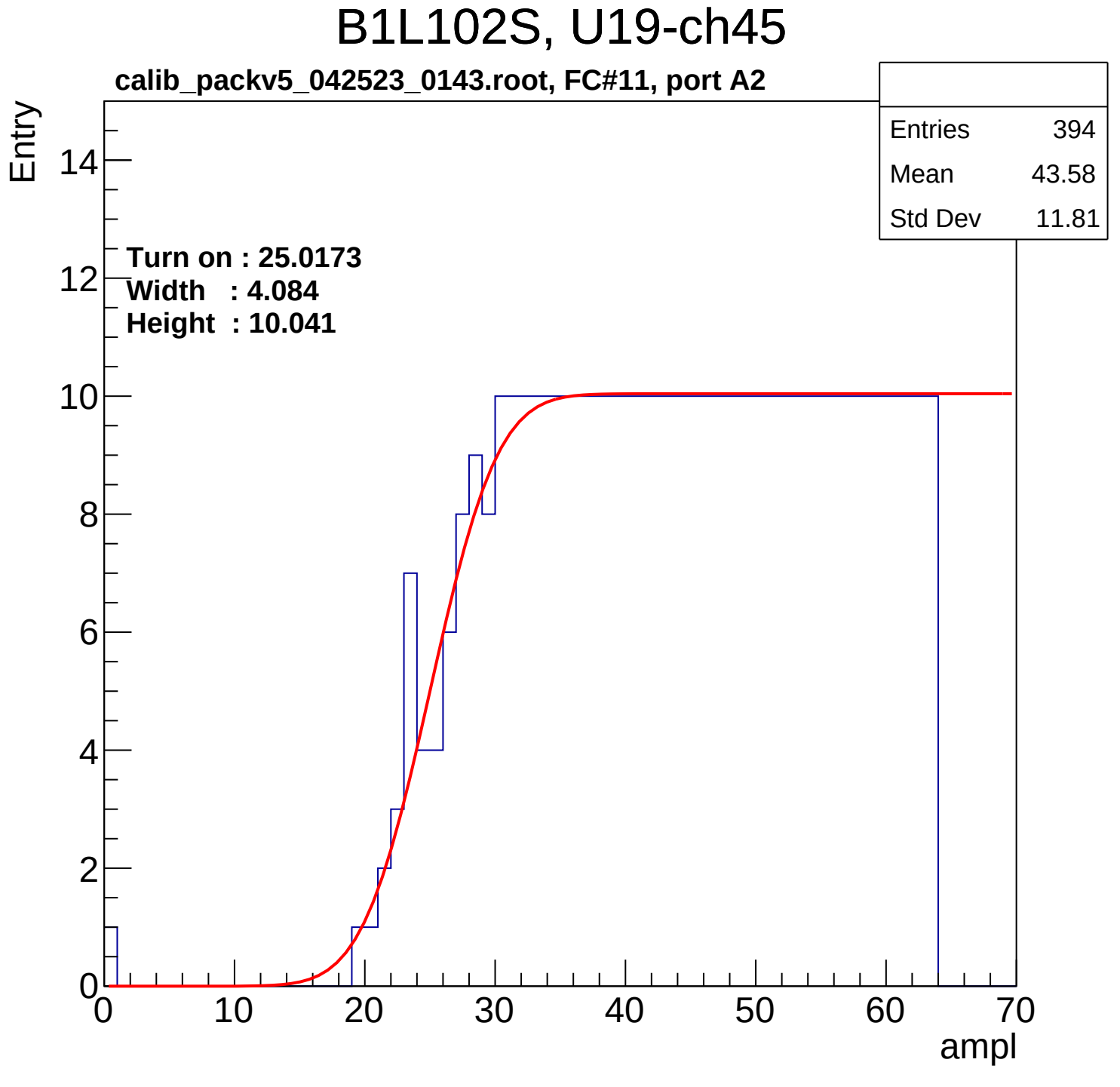

B1L102S, U19-ch40
calib_packv5_042523_0143.root, FC#11, port A2
Entries 414
Mean 42.51
Std Dev 12.57
Turn on : 22.9043
Width : 3.246
Height : 9.948
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

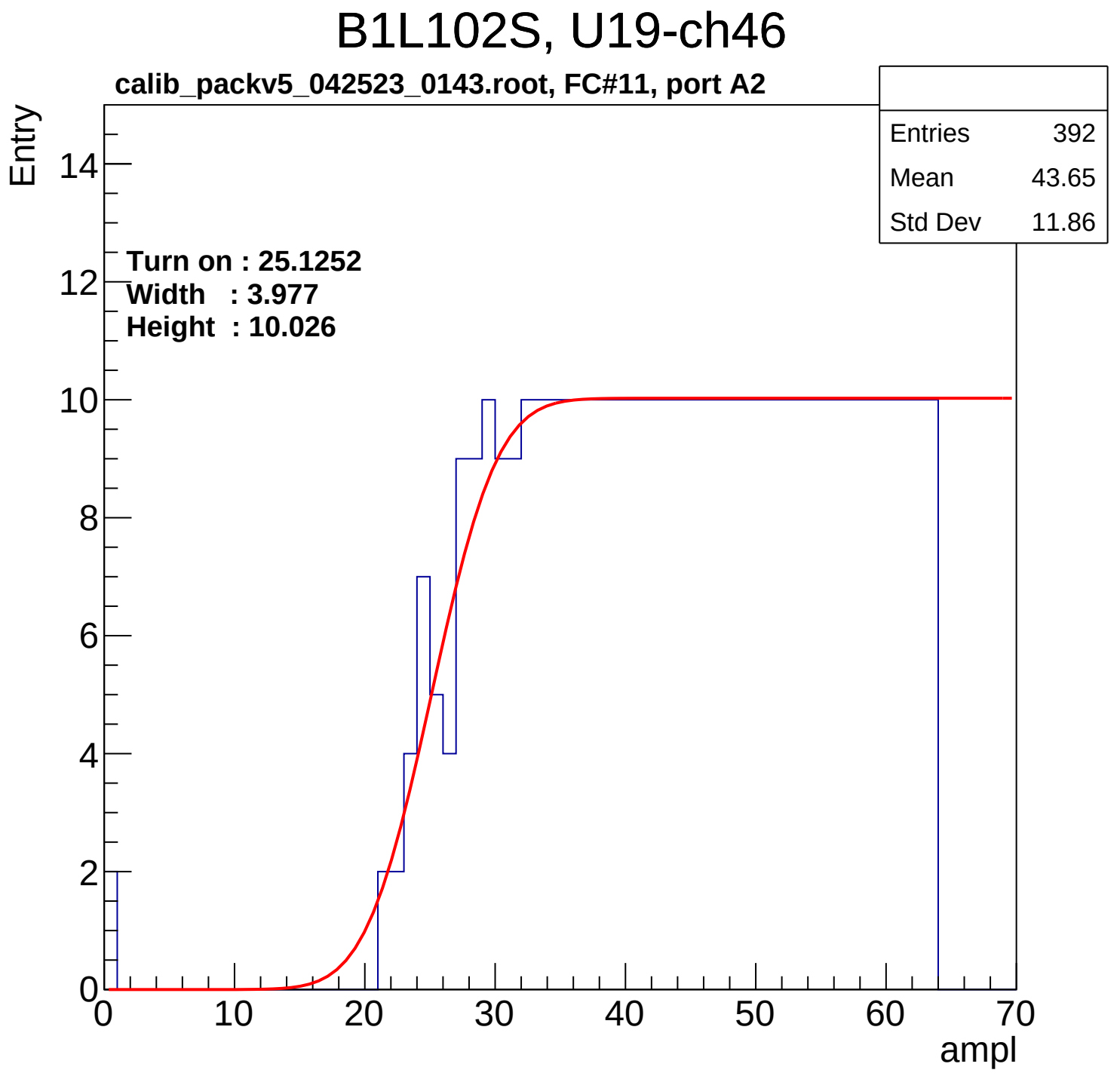

B1L102S, U19-ch41
calib_packv5_042523_0143.root, FC#11, port A2
Entries 373
Mean 44.6
Std Dev 11.36
Turn on : 27.8008
Width : 2.792
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

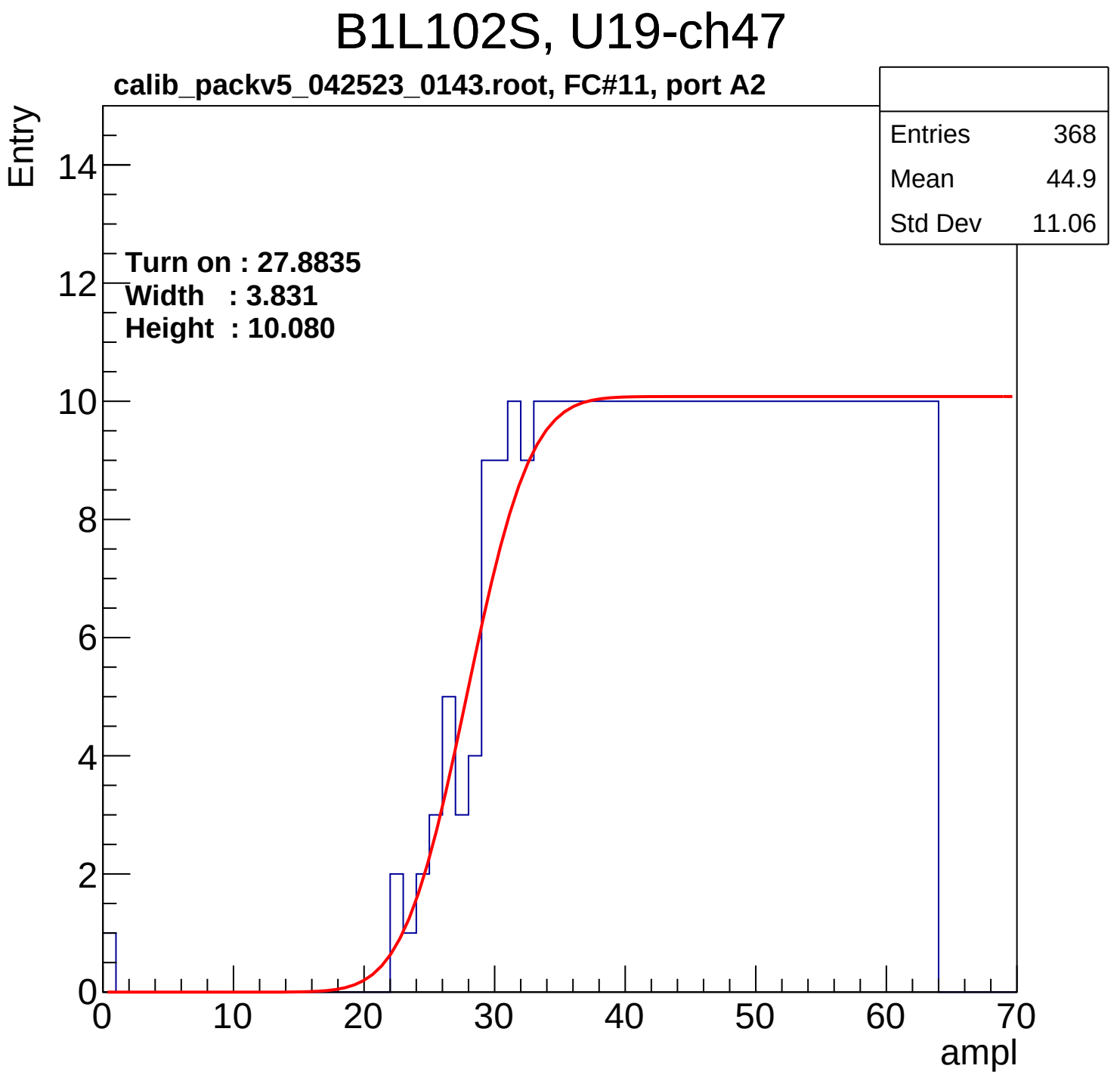

B1L102S, U19-ch42
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.15
Std Dev 11.6
Turn on : 26.4388
Width : 3.519
Height : 10.054
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

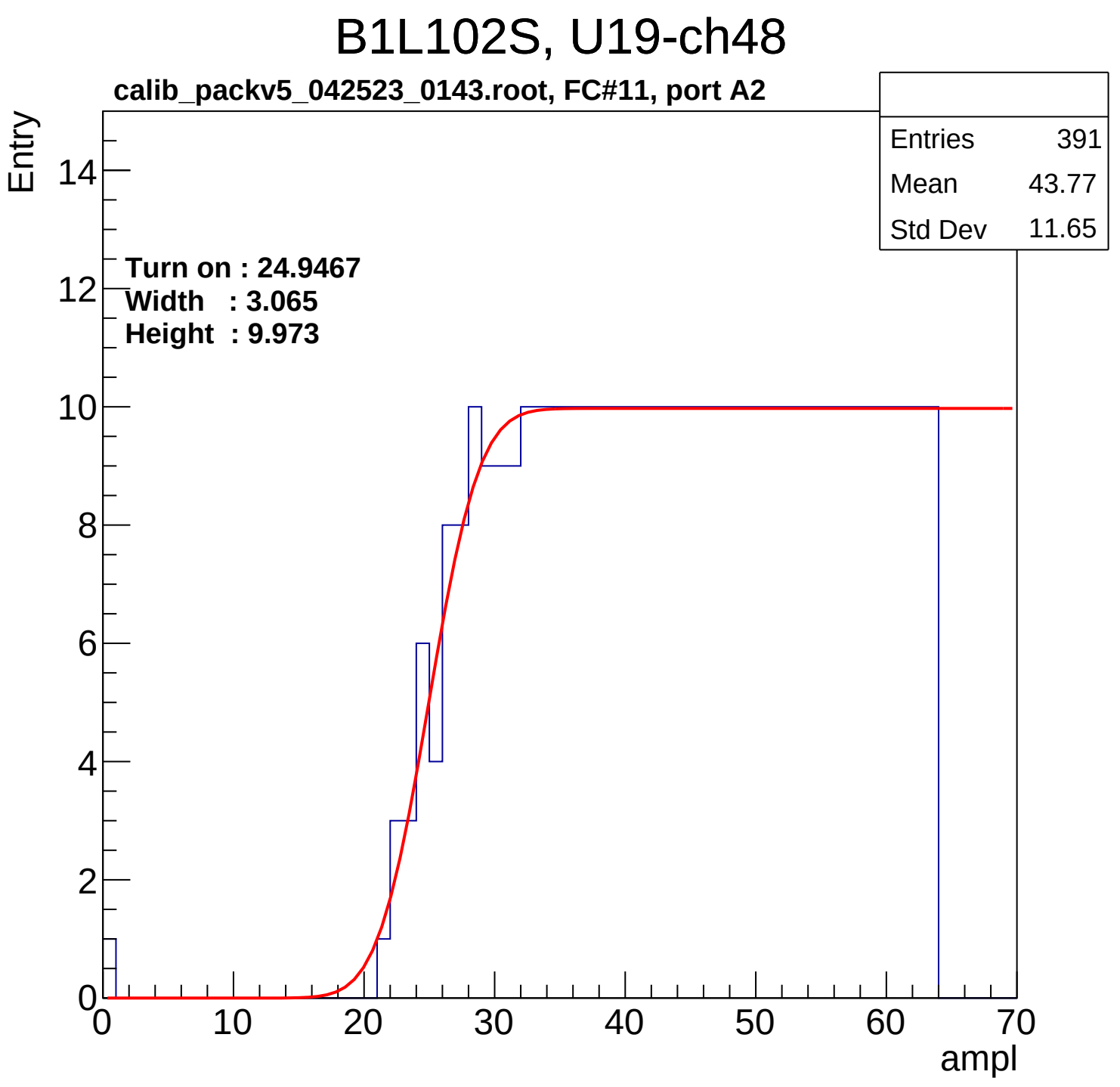

B1L102S, U19-ch43
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.53
Std Dev 11.22
Turn on : 26.6521
Width : 2.358
Height : 9.966
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

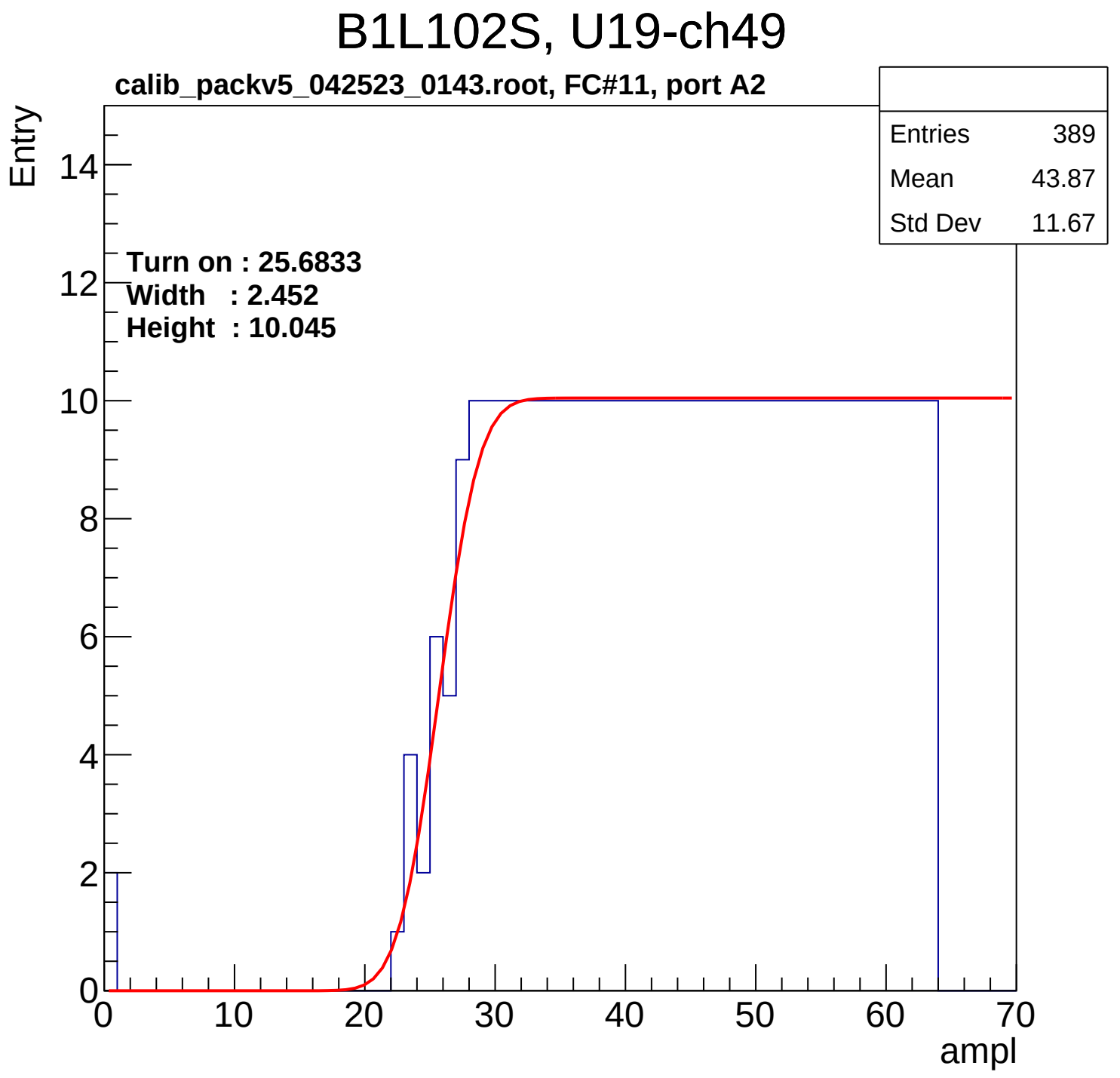

B1L102S, U19-ch44
calib_packv5_042523_0143.root, FC#11, port A2
Entries 359
Mean 44.98
Std Dev 11.83
Turn on : 28.1388
Width : 2.641
Height : 9.917
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

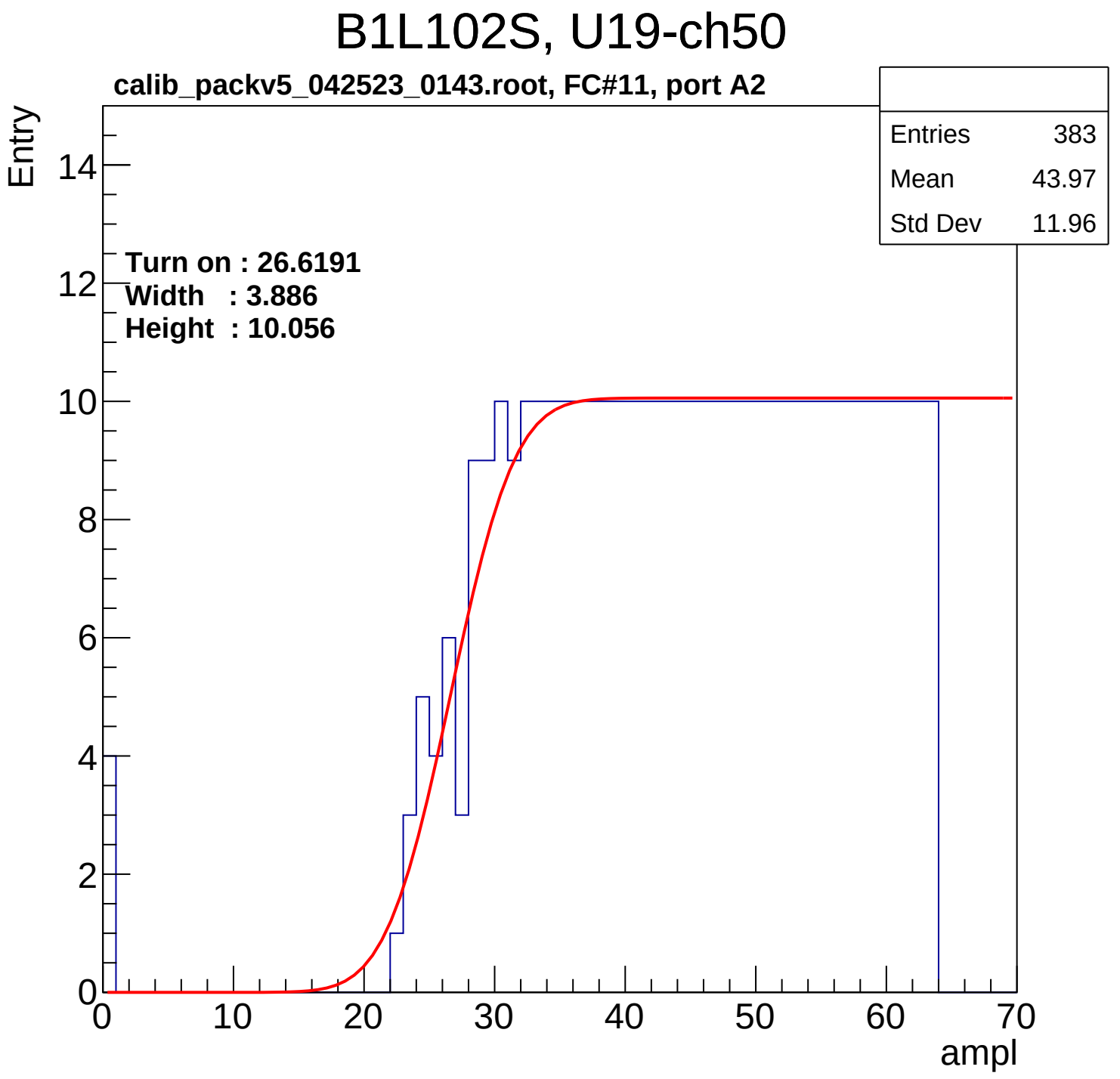

B1L102S, U19-ch45
calib_packv5_042523_0143.root, FC#11, port A2
Entries 394
Mean 43.58
Std Dev 11.81
Turn on : 25.0173
Width : 4.084
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

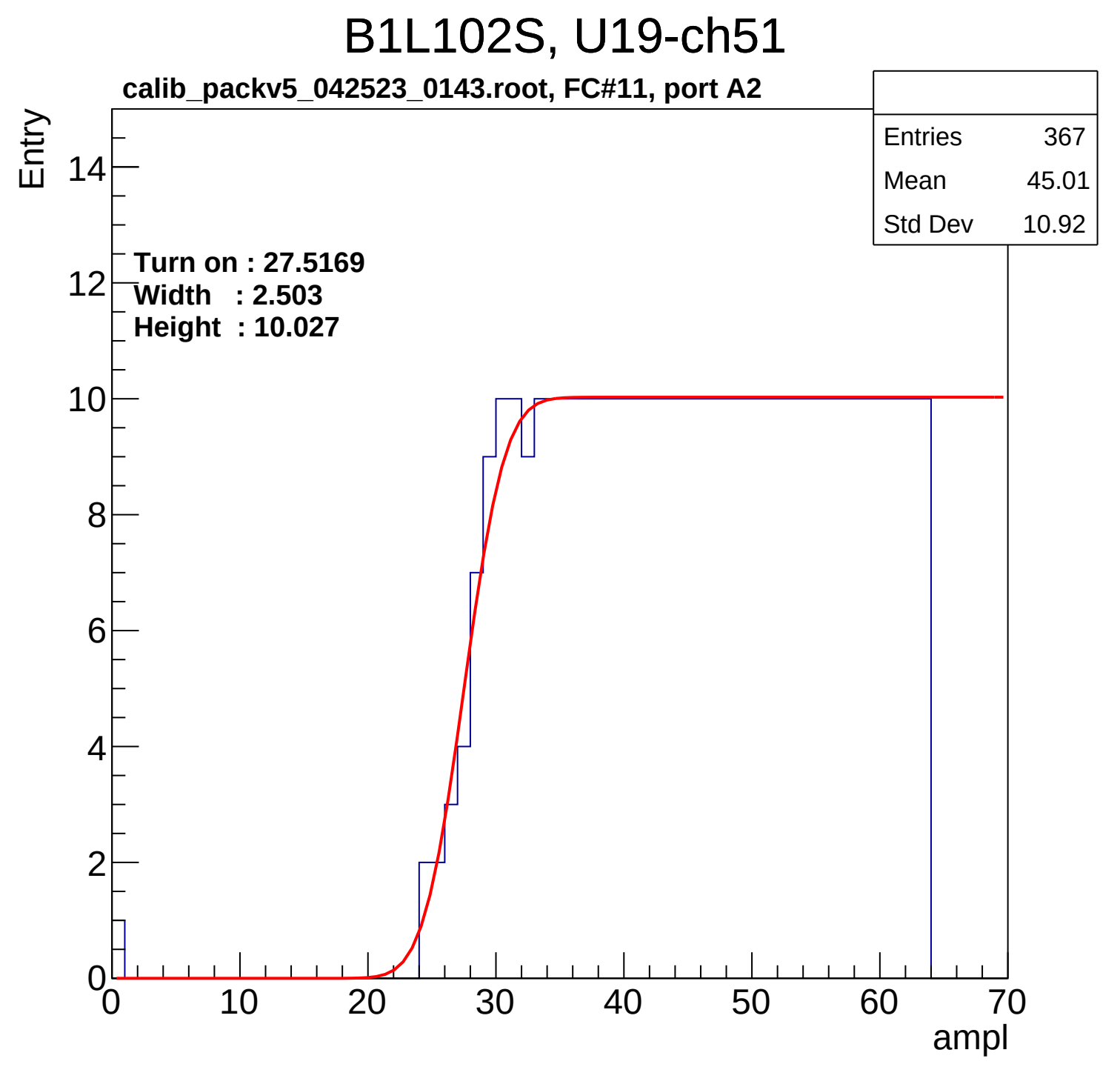

B1L102S, U19-ch46
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.65
Std Dev 11.86
Turn on : 25.1252
Width : 3.977
Height : 10.026
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

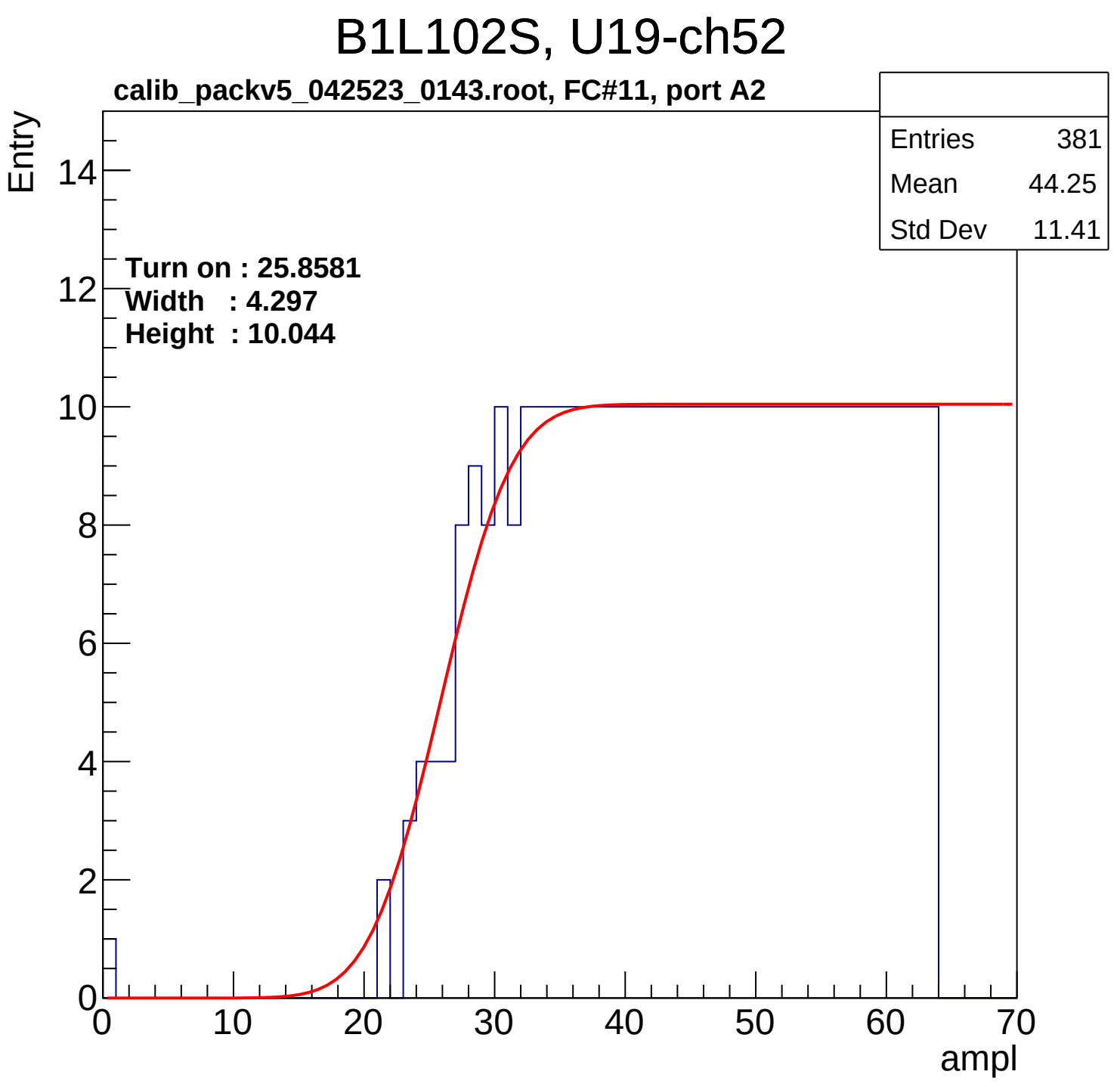

B1L102S, U19-ch47
calib_packv5_042523_0143.root, FC#11, port A2
Entries 368
Mean 44.9
Std Dev 11.06
Turn on : 27.8835
Width : 3.831
Height : 10.080
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

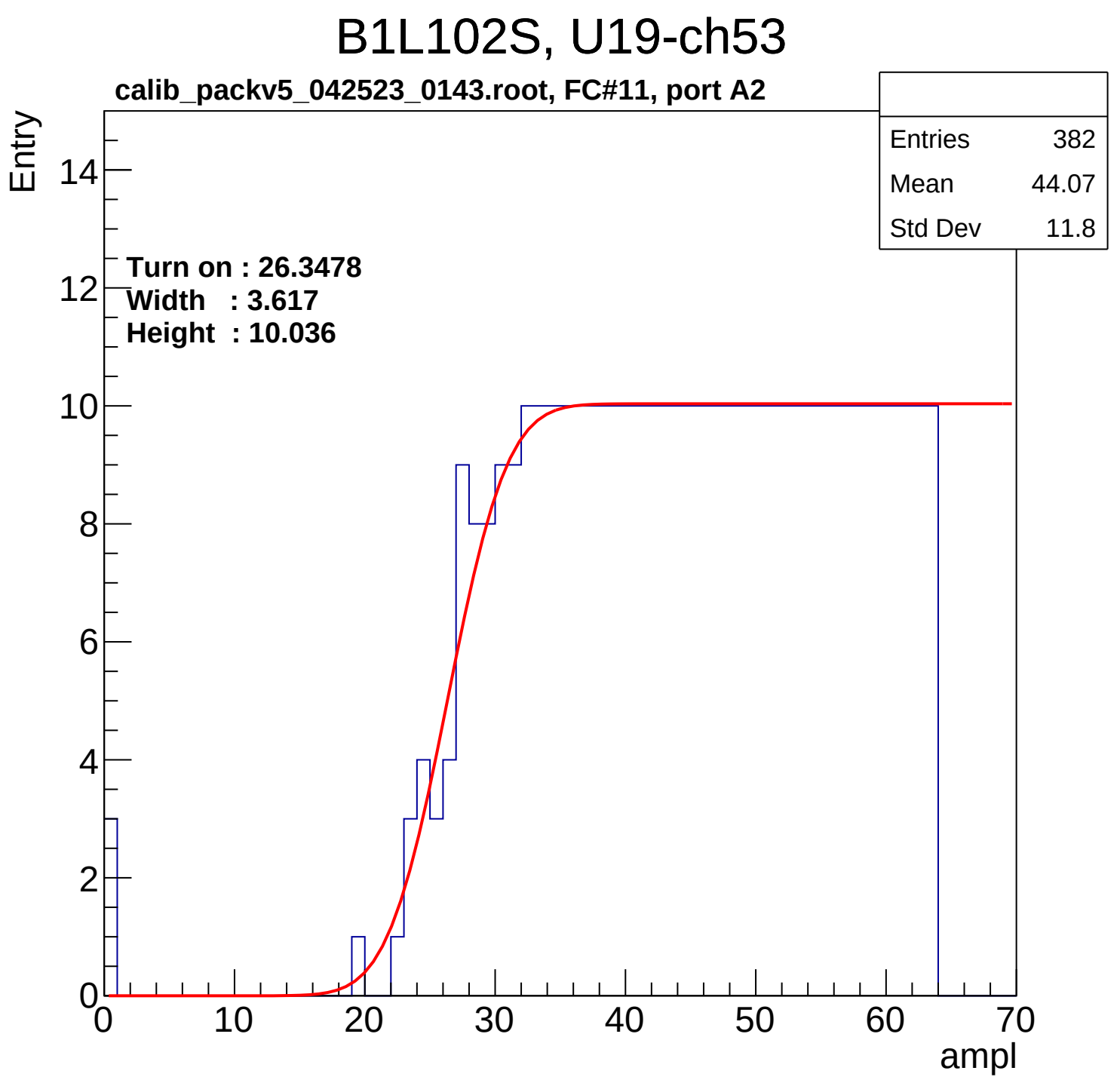

B1L102S, U19-ch48
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.77
Std Dev 11.65
Turn on : 24.9467
Width : 3.065
Height : 9.973
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

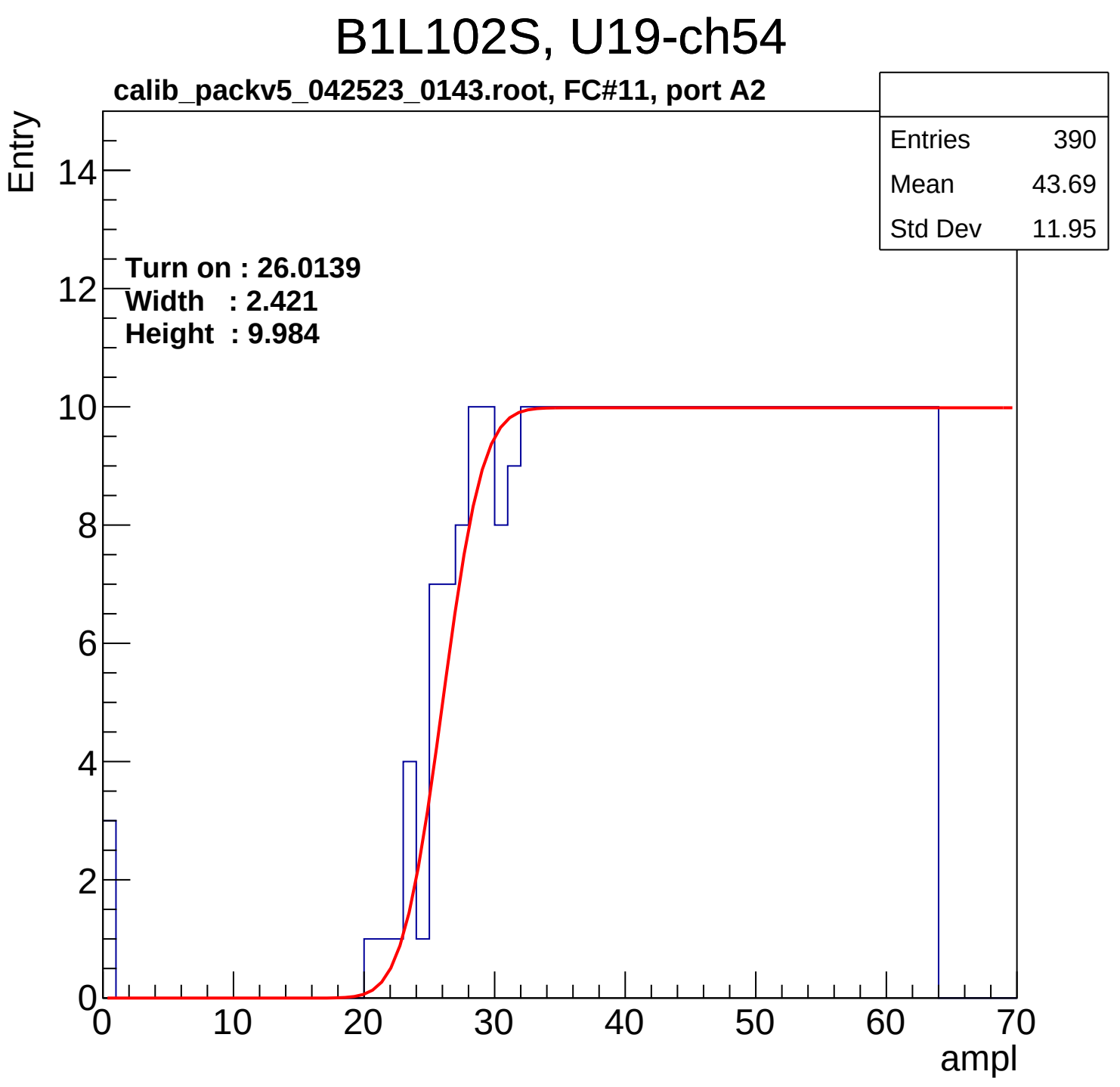

B1L102S, U19-ch49
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.87
Std Dev 11.67
Turn on : 25.6833
Width : 2.452
Height : 10.045
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

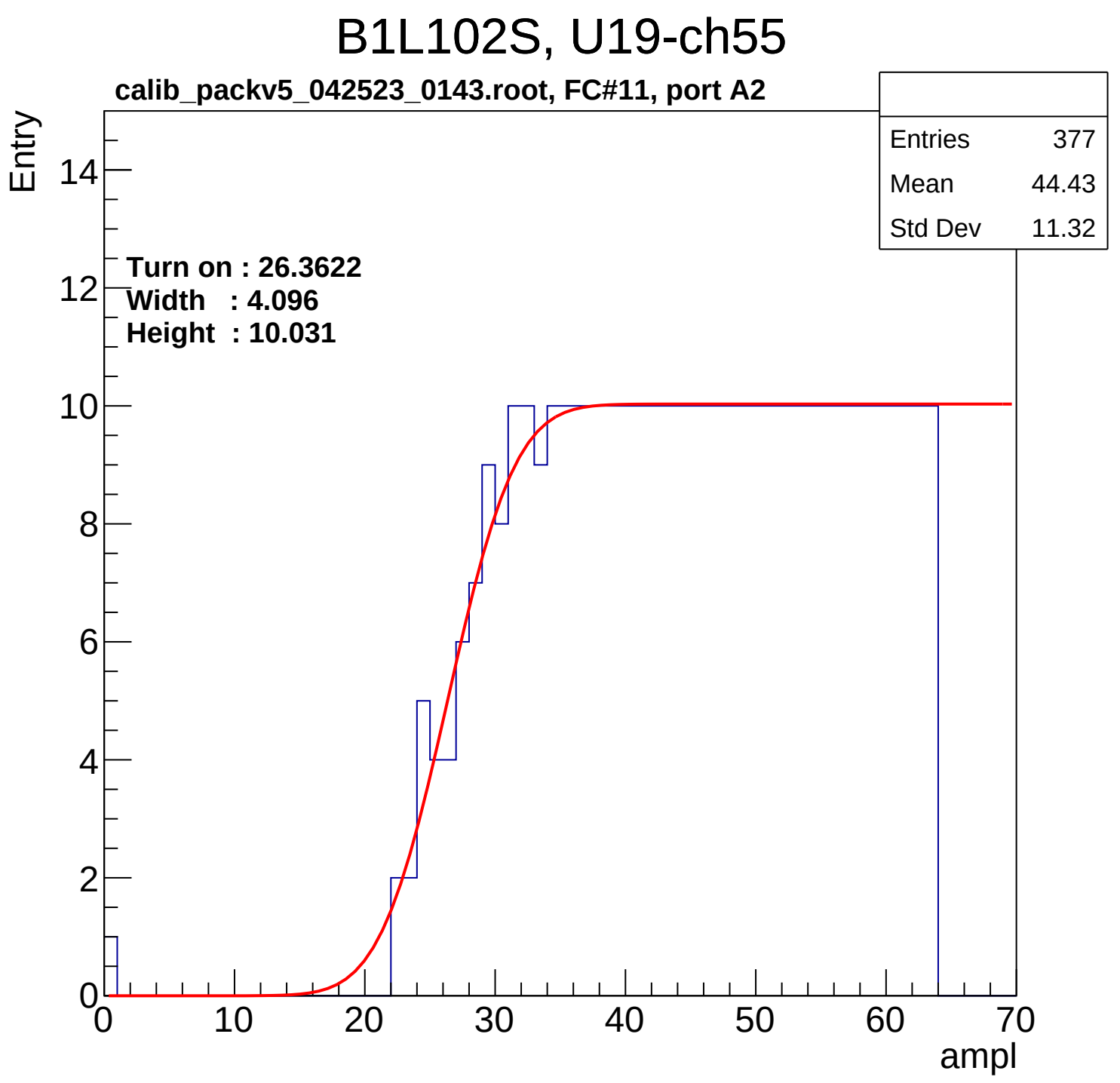

B1L102S, U19-ch50
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 43.97
Std Dev 11.96
Turn on : 26.6191
Width : 3.886
Height : 10.056
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

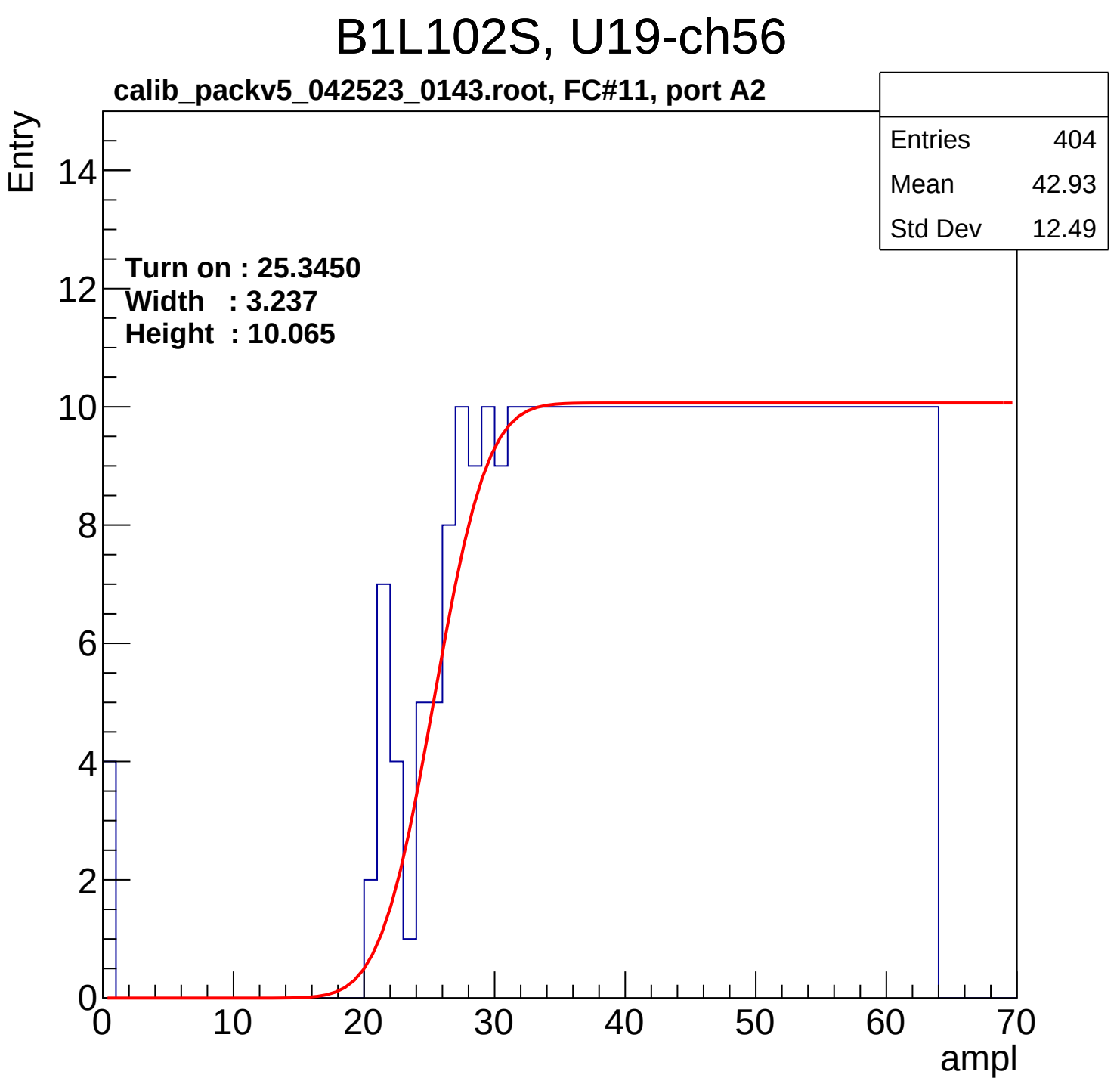

B1L102S, U19-ch51
calib_packv5_042523_0143.root, FC#11, port A2
Entries 367
Mean 45.01
Std Dev 10.92
Turn on : 27.5169
Width : 2.503
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

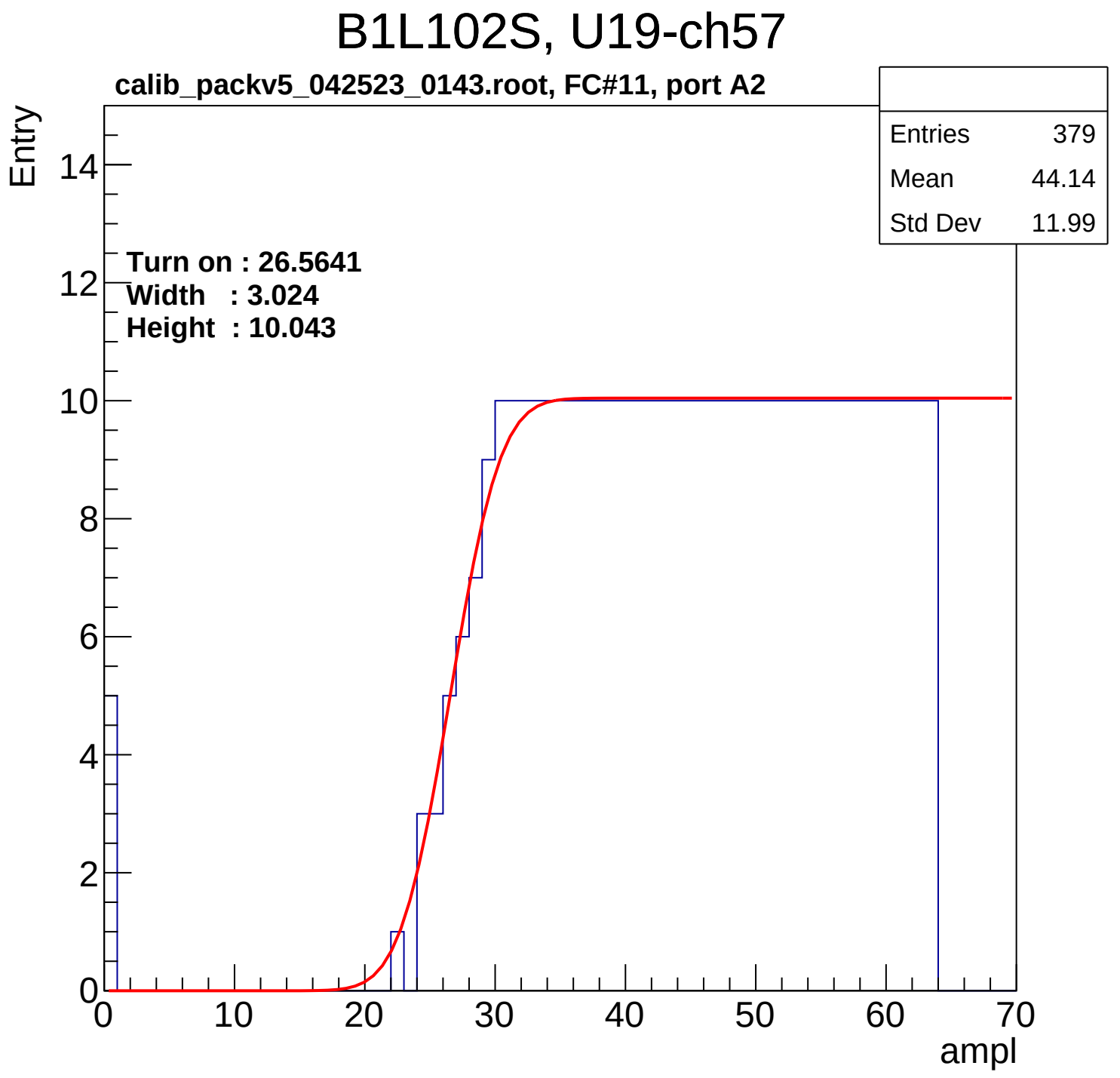

B1L102S, U19-ch52
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.25
Std Dev 11.41
Turn on : 25.8581
Width : 4.297
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

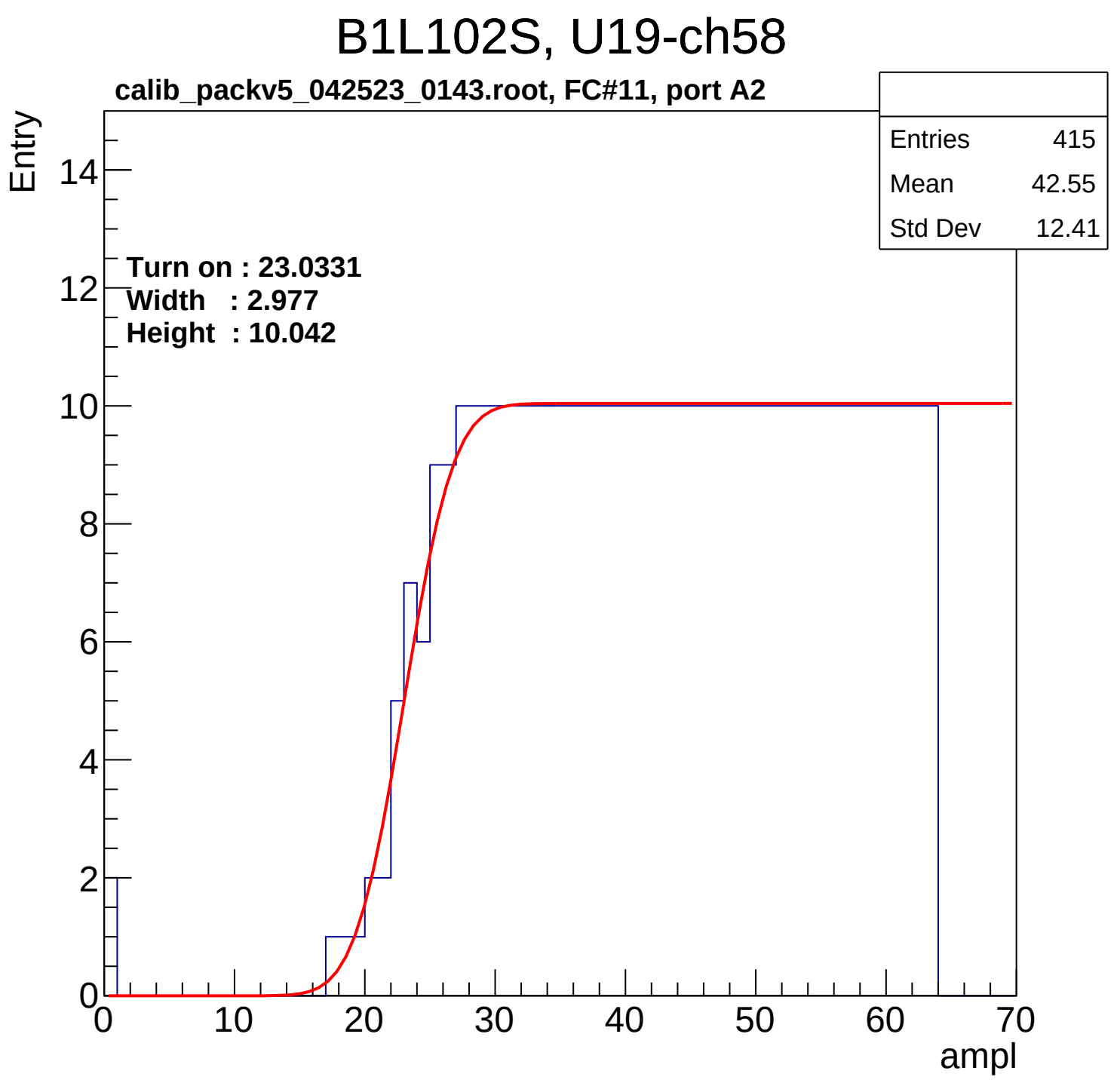

B1L102S, U19-ch53
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.07
Std Dev 11.8
Turn on : 26.3478
Width : 3.617
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

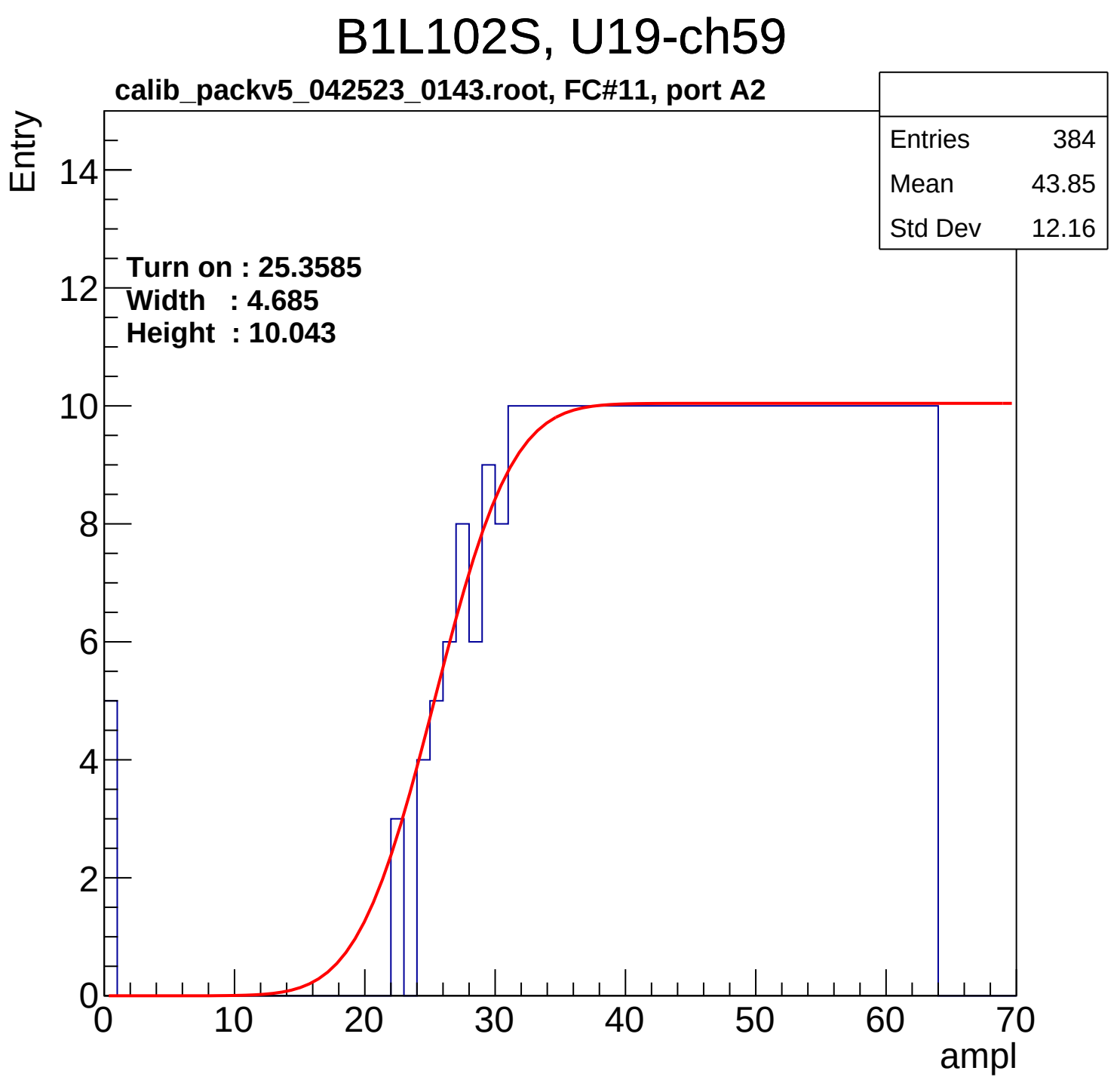

B1L102S, U19-ch54
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.69
Std Dev 11.95
Turn on : 26.0139
Width : 2.421
Height : 9.984
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

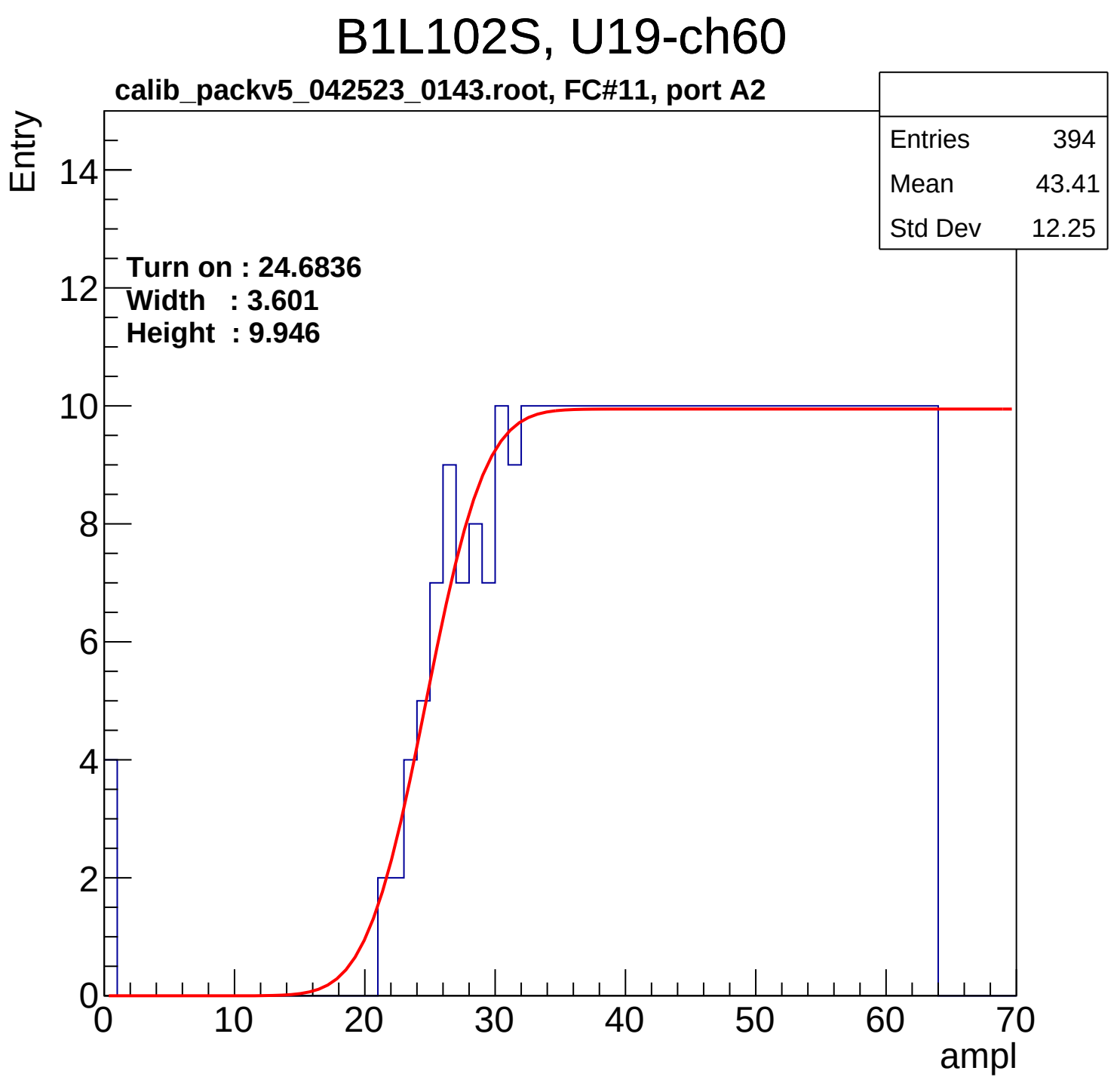

B1L102S, U19-ch55
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.43
Std Dev 11.32
Turn on : 26.3622
Width : 4.096
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

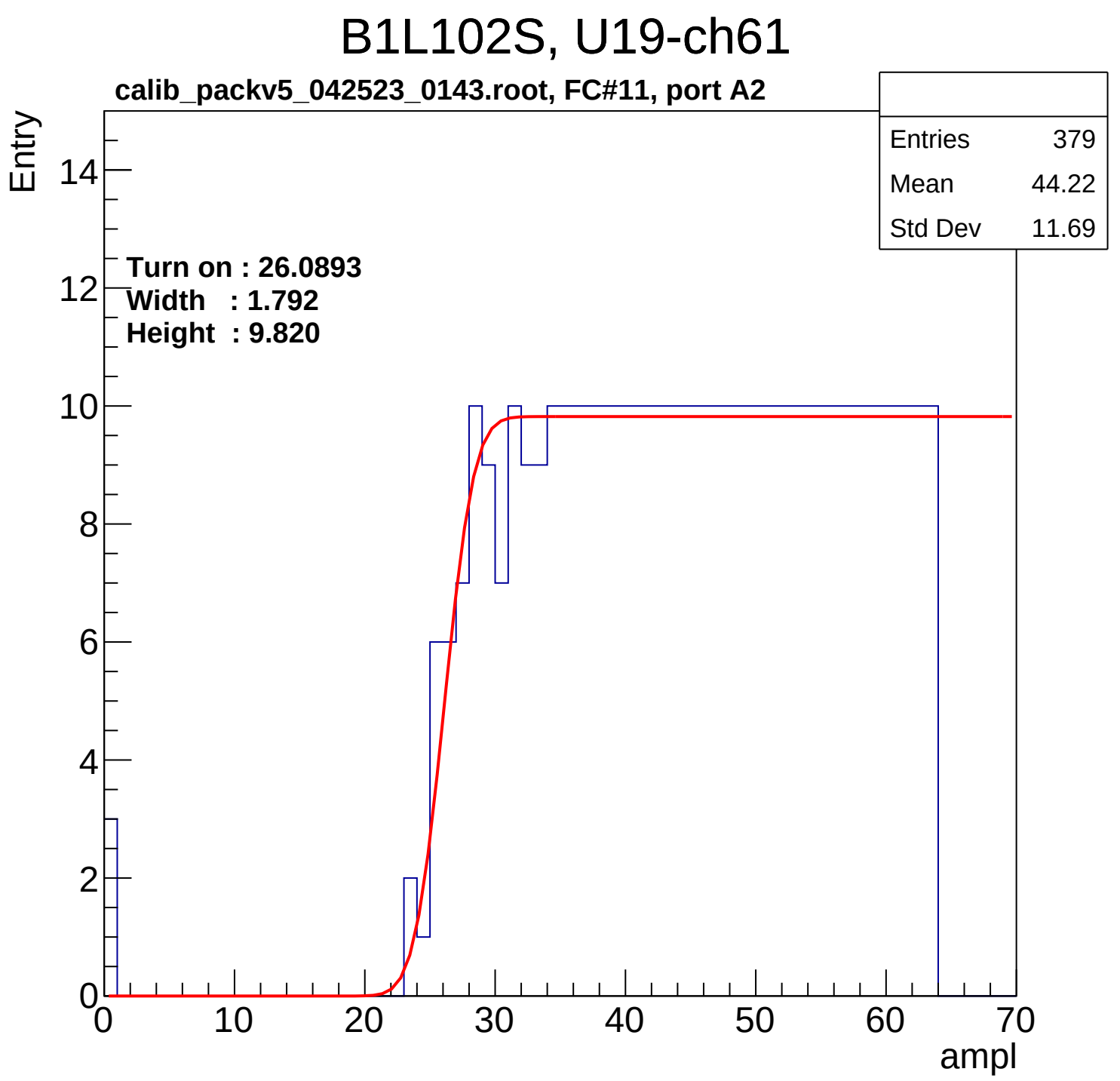

B1L102S, U19-ch56
calib_packv5_042523_0143.root, FC#11, port A2
Entries 404
Mean 42.93
Std Dev 12.49
Turn on : 25.3450
Width : 3.237
Height : 10.065
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

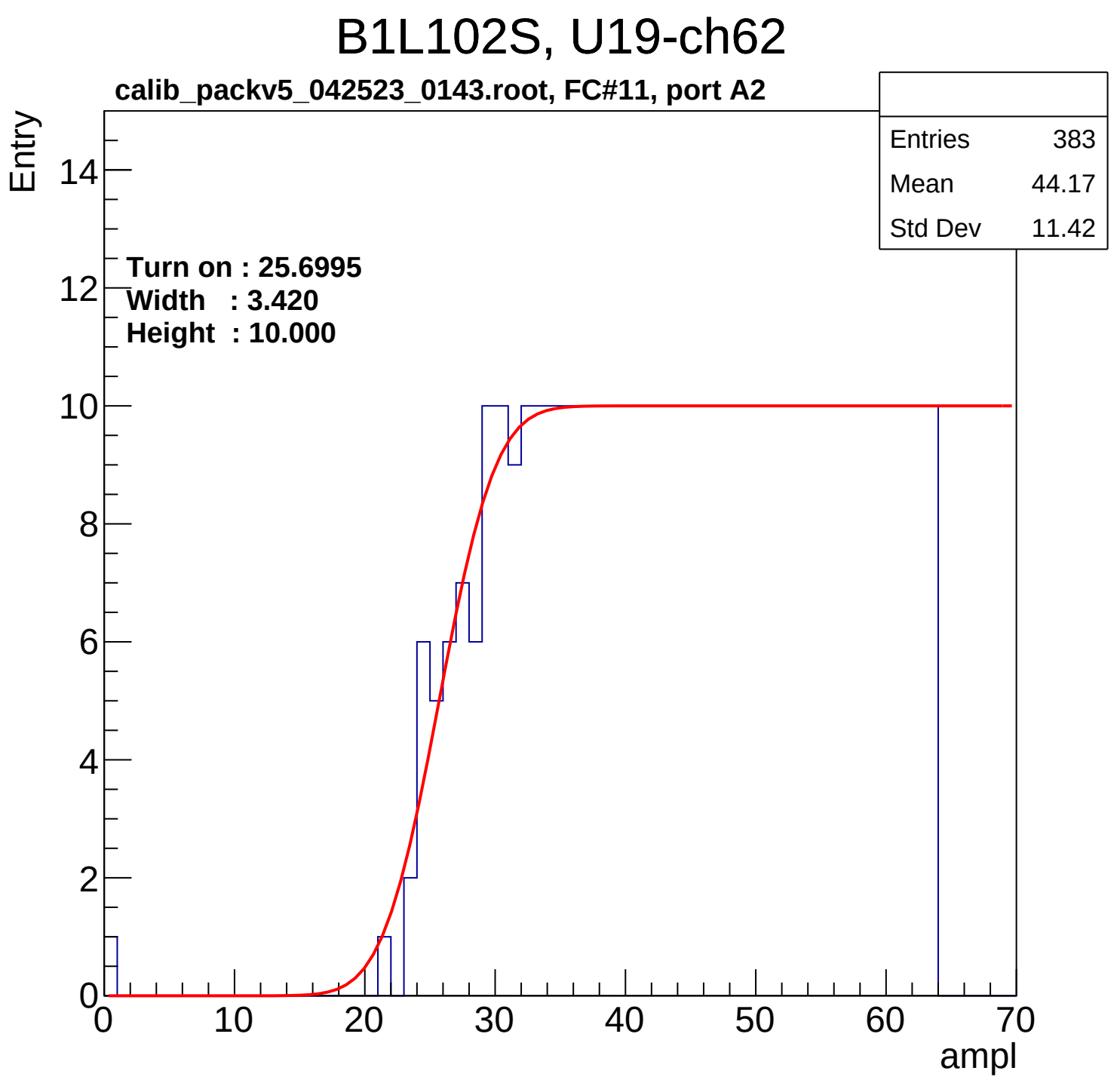

B1L102S, U19-ch57
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.14
Std Dev 11.99
Turn on : 26.5641
Width : 3.024
Height : 10.043
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

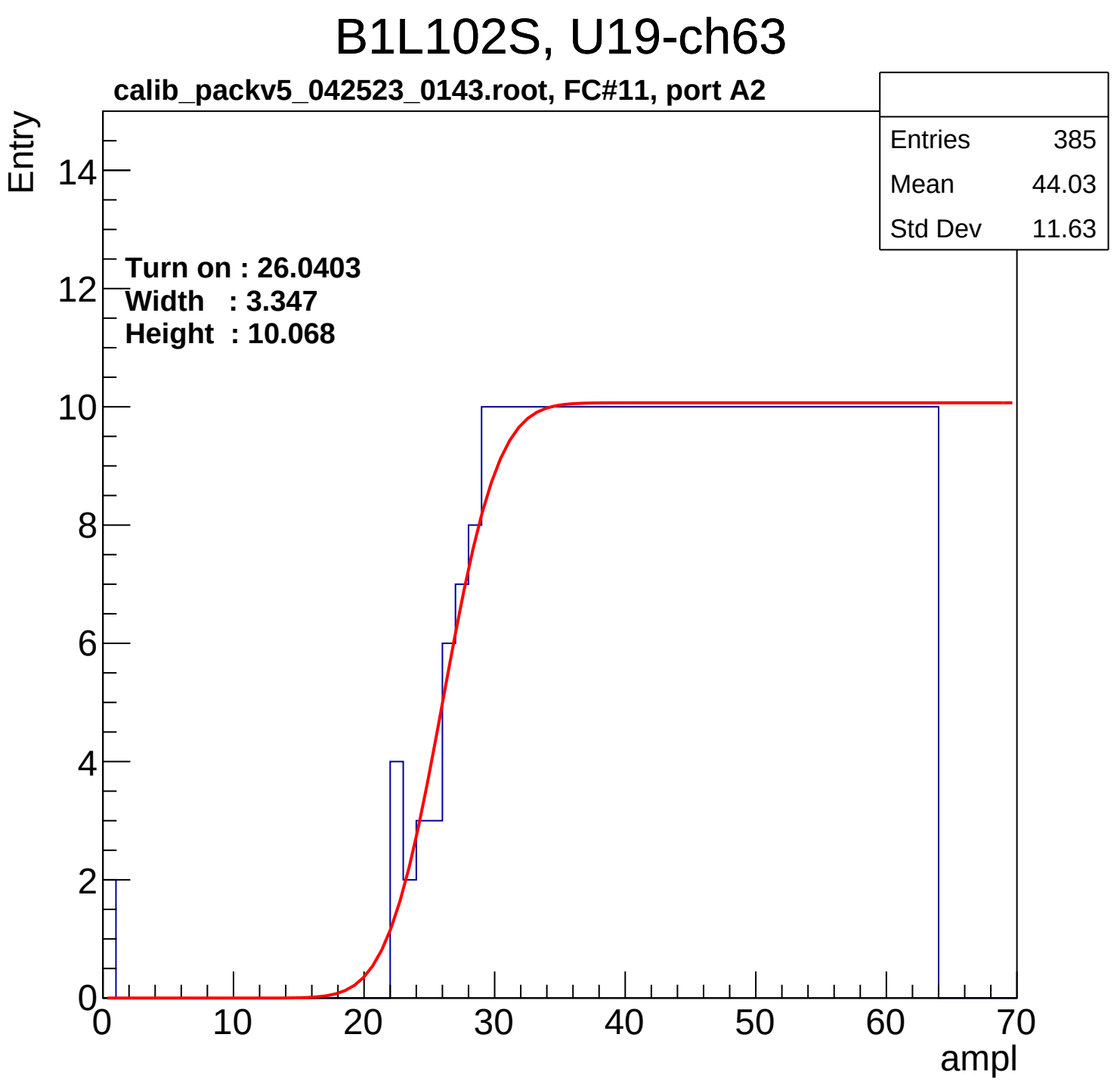

B1L102S, U19-ch58
calib_packv5_042523_0143.root, FC#11, port A2
Entries 415
Mean 42.55
Std Dev 12.41
Turn on : 23.0331
Width : 2.977
Height : 10.042
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

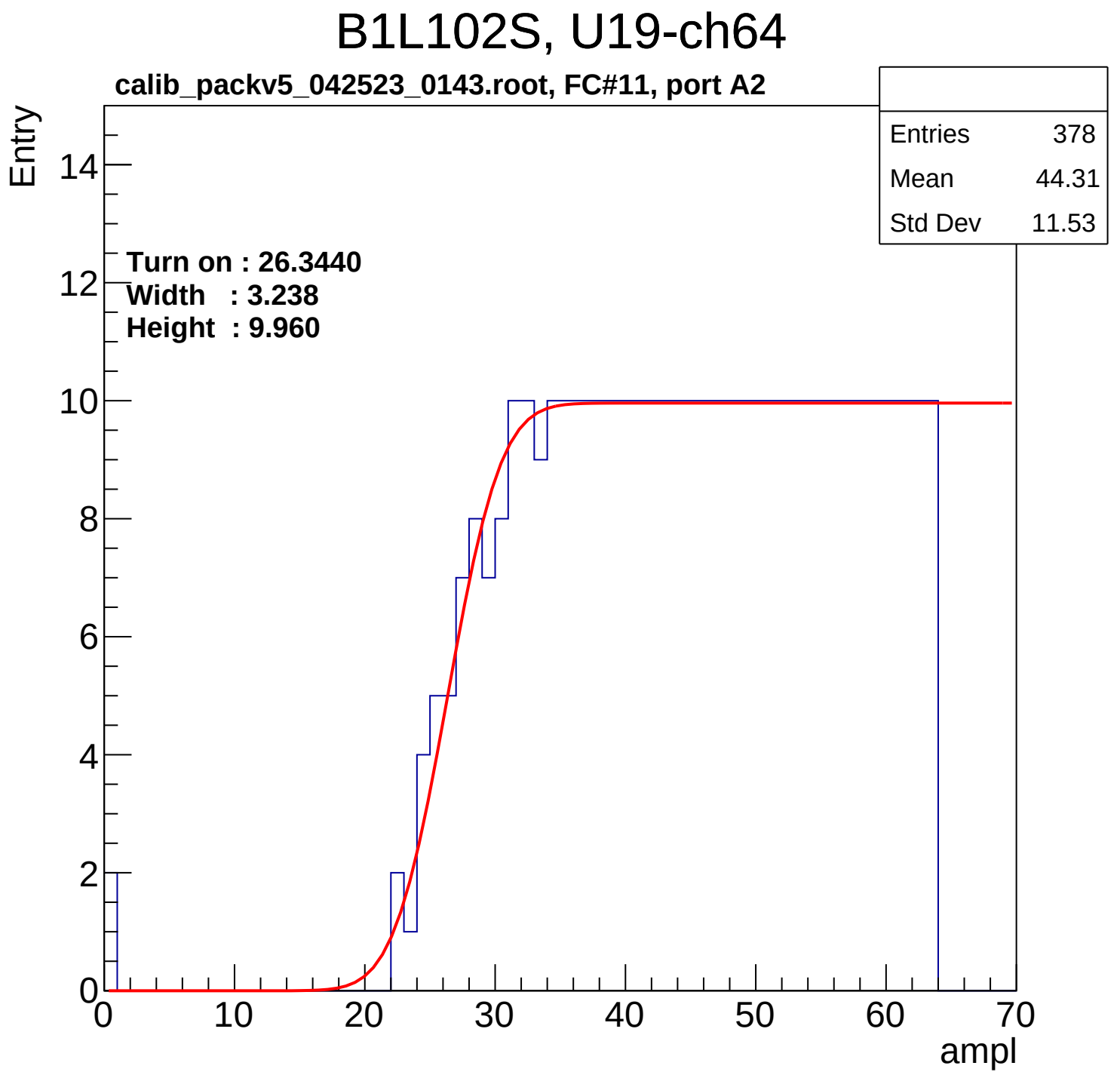

B1L102S, U19-ch59
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 43.85
Std Dev 12.16
Turn on : 25.3585
Width : 4.685
Height : 10.043
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

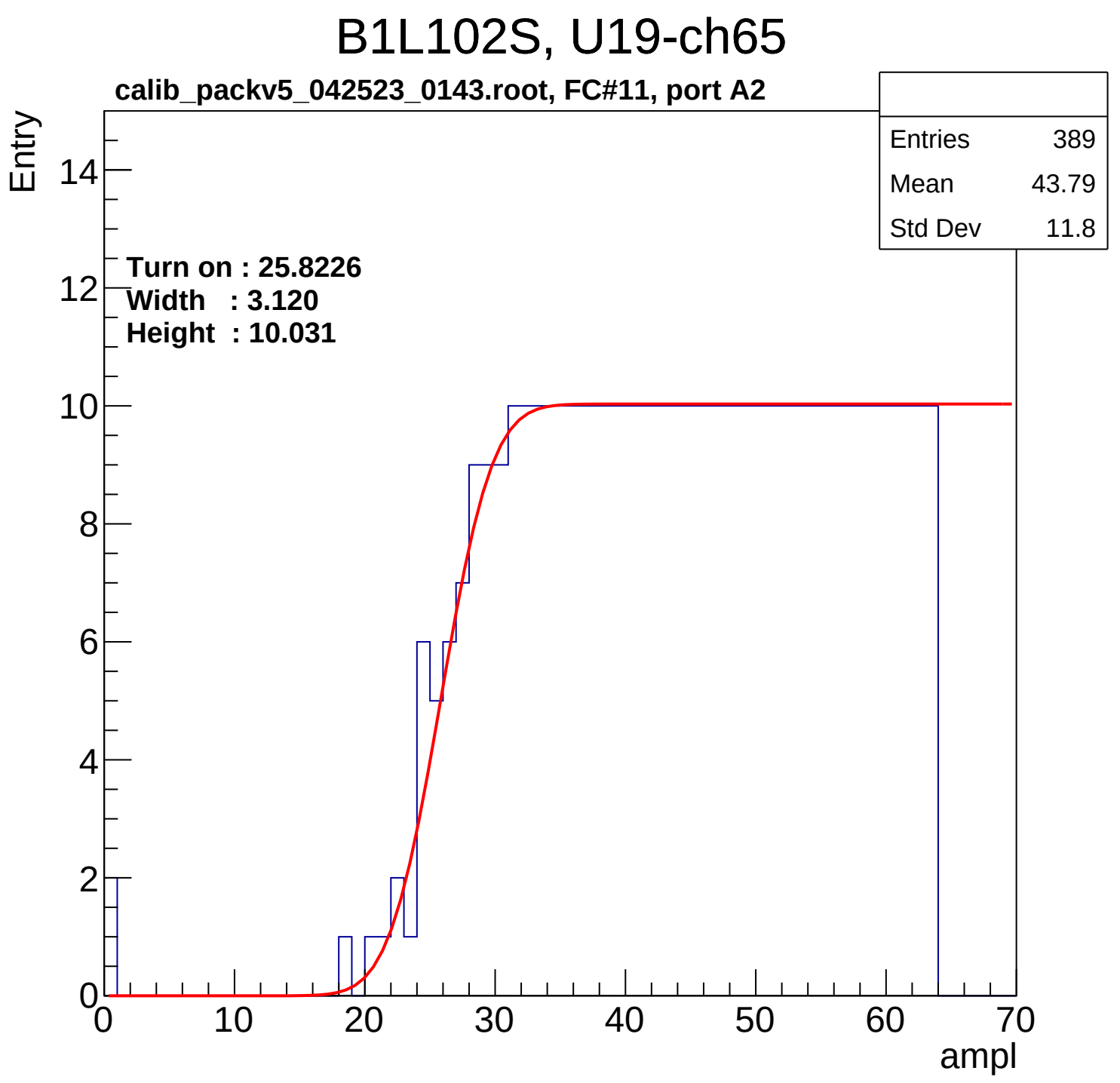

B1L102S, U19-ch60
calib_packv5_042523_0143.root, FC#11, port A2
Entries 394
Mean 43.41
Std Dev 12.25
Turn on : 24.6836
Width : 3.601
Height : 9.946
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

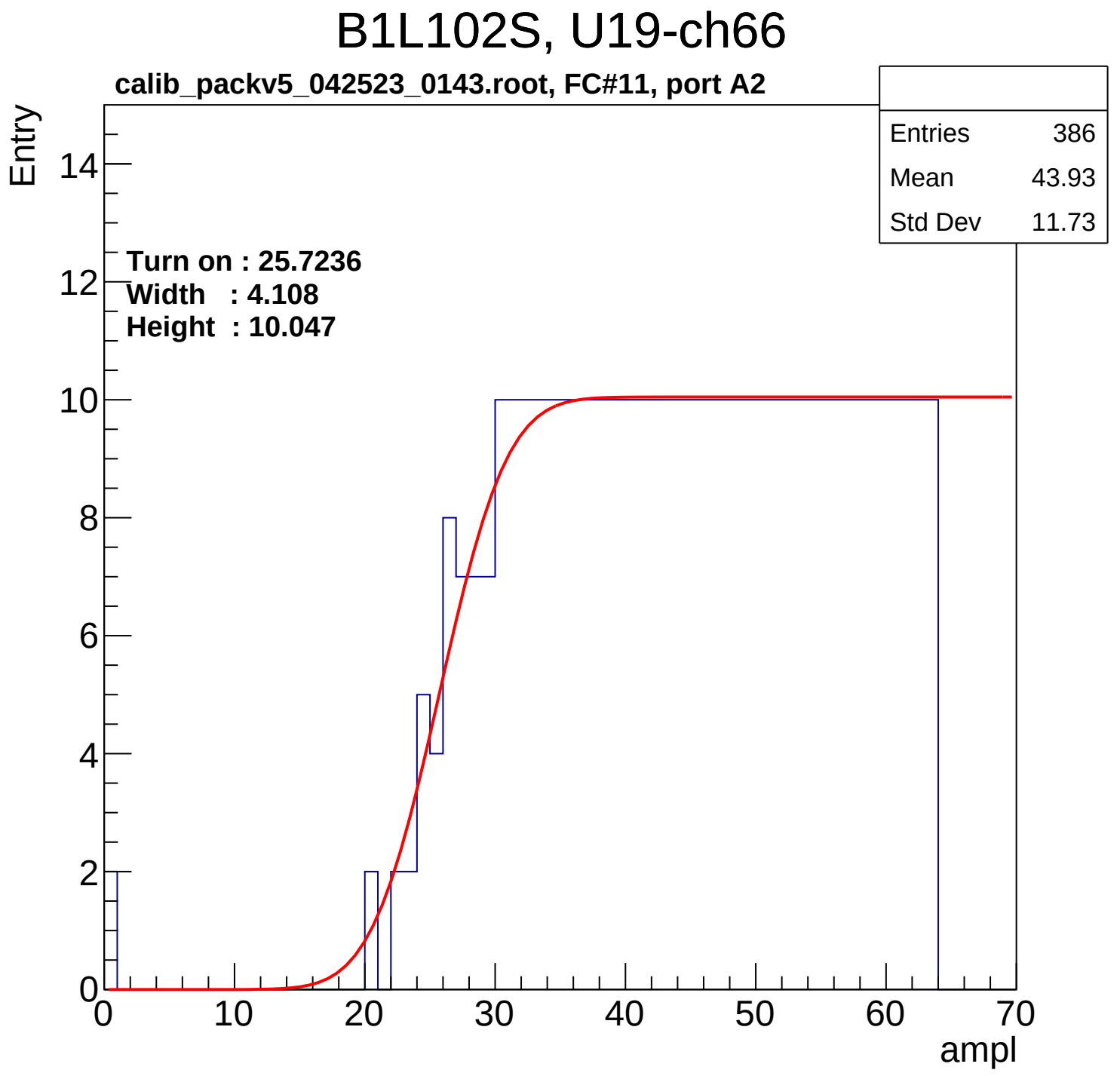

B1L102S, U19-ch61
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.22
Std Dev 11.69
Turn on : 26.0893
Width : 1.792
Height : 9.820
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

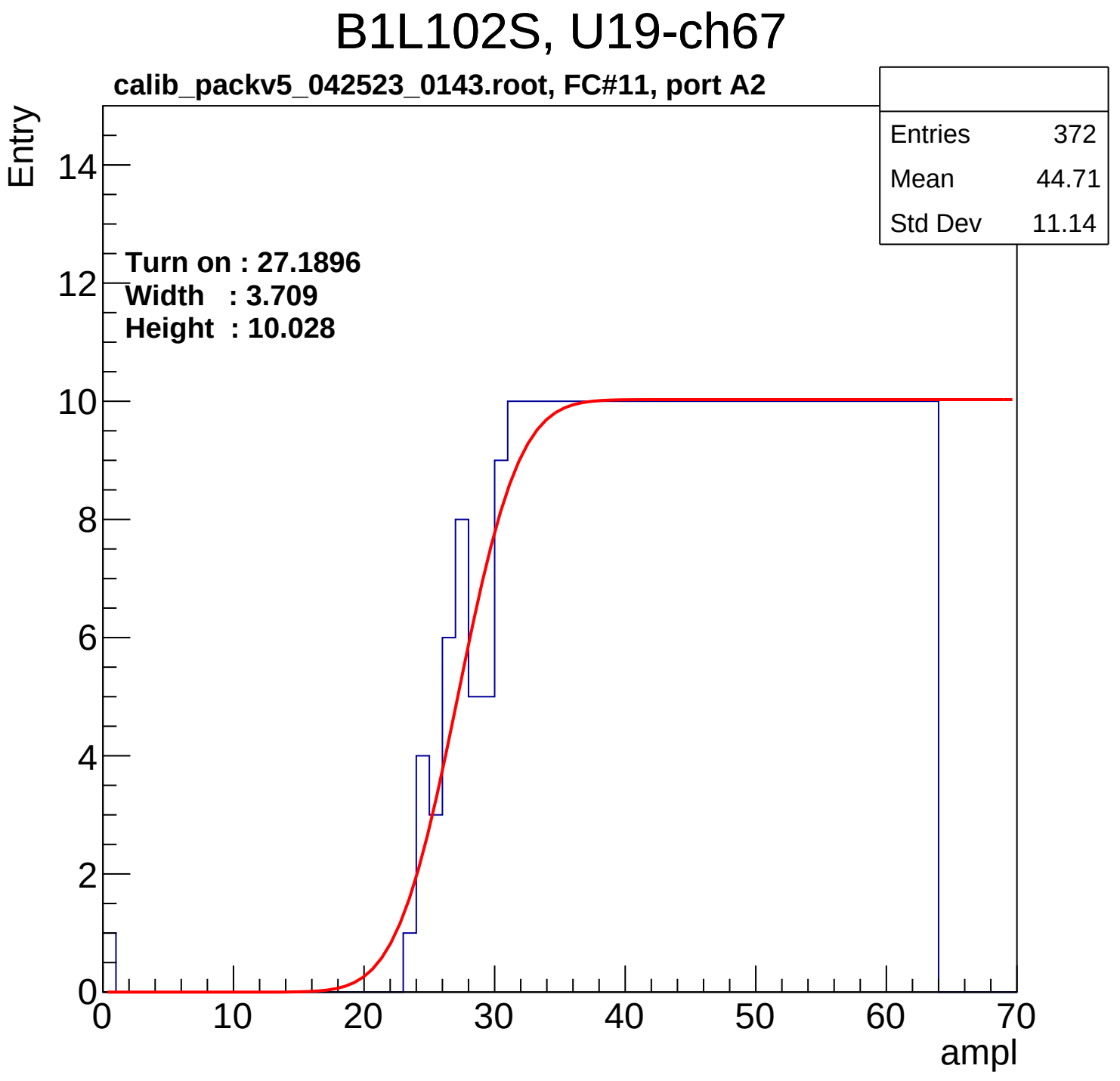

B1L102S, U19-ch62
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.17
Std Dev 11.42
Turn on : 25.6995
Width : 3.420
Height : 10.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

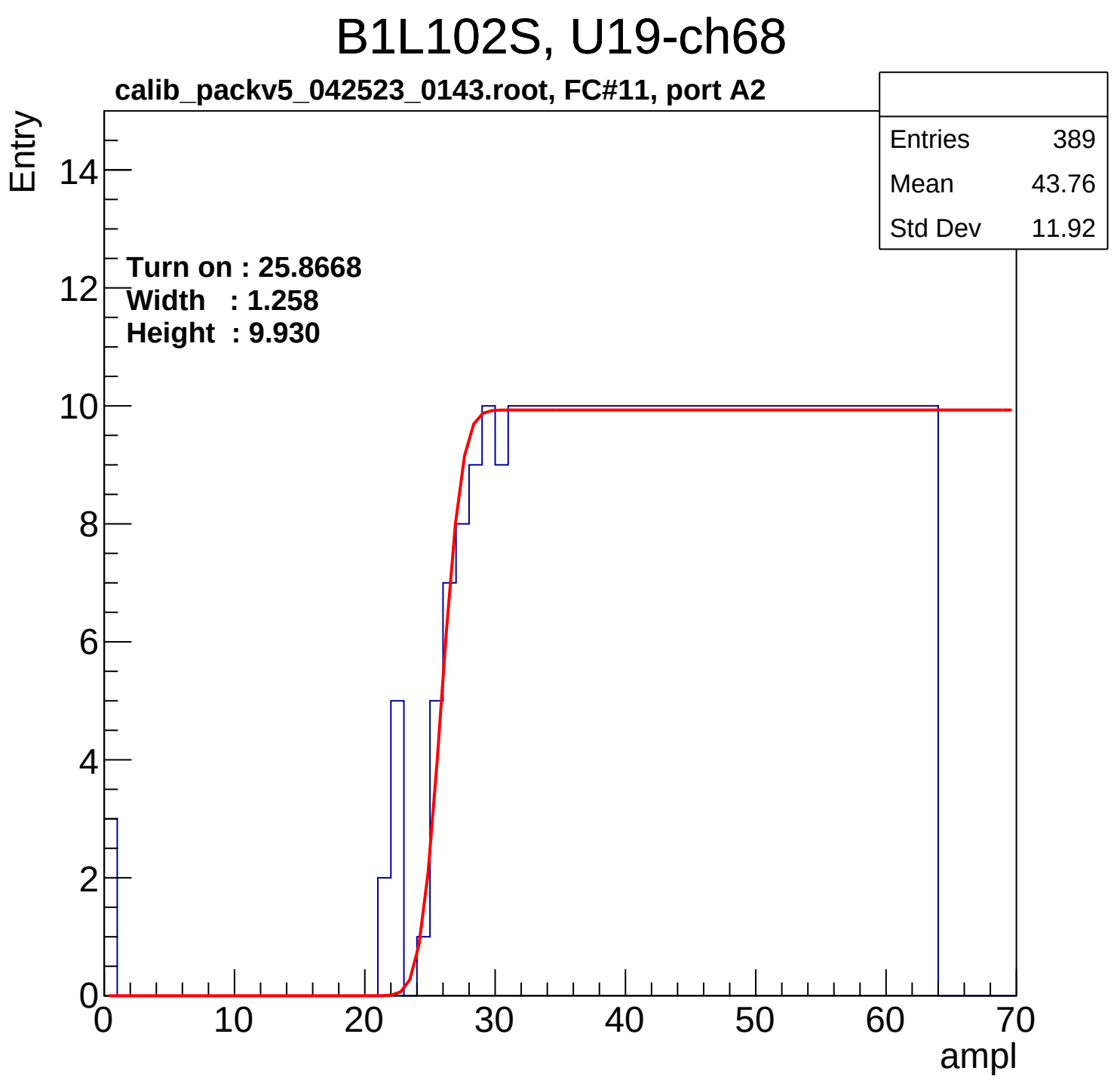

B1L102S, U19-ch63
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 44.03
Std Dev 11.63
Turn on : 26.0403
Width : 3.347
Height : 10.068
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

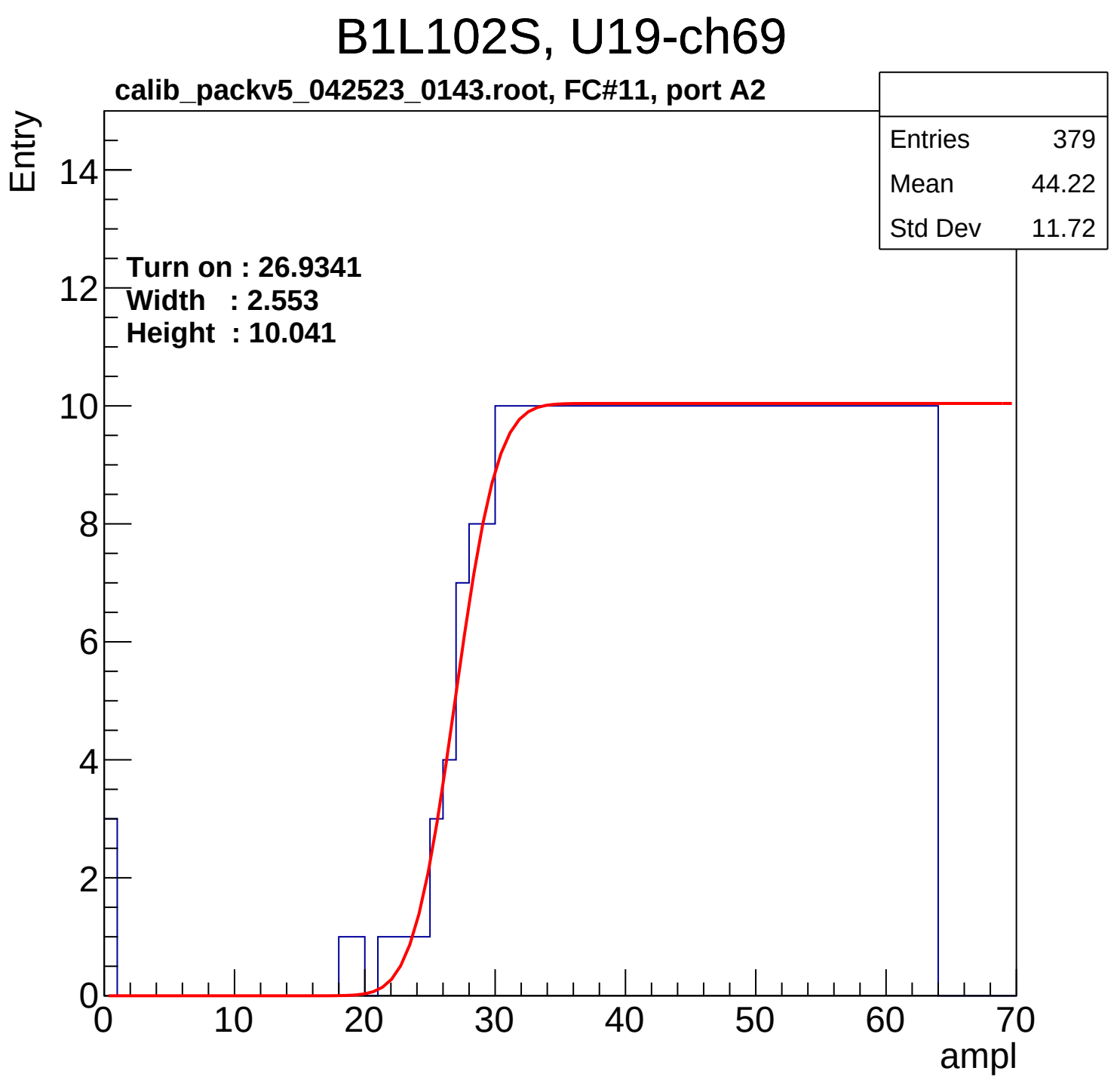

B1L102S, U19-ch64
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.31
Std Dev 11.53
Turn on : 26.3440
Width : 3.238
Height : 9.960
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

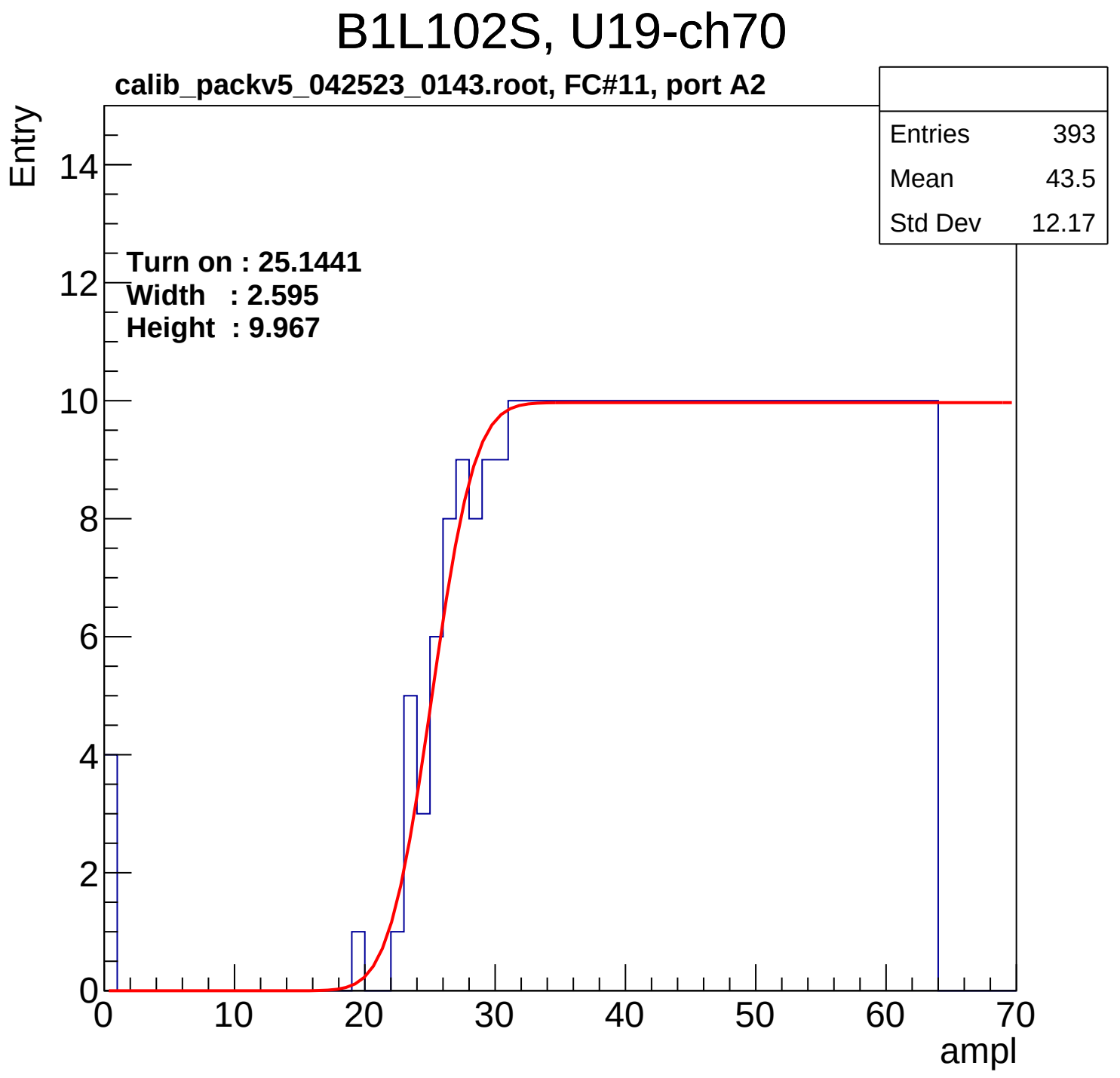

B1L102S, U19-ch65
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.79
Std Dev 11.8
Turn on : 25.8226
Width : 3.120
Height : 10.031
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

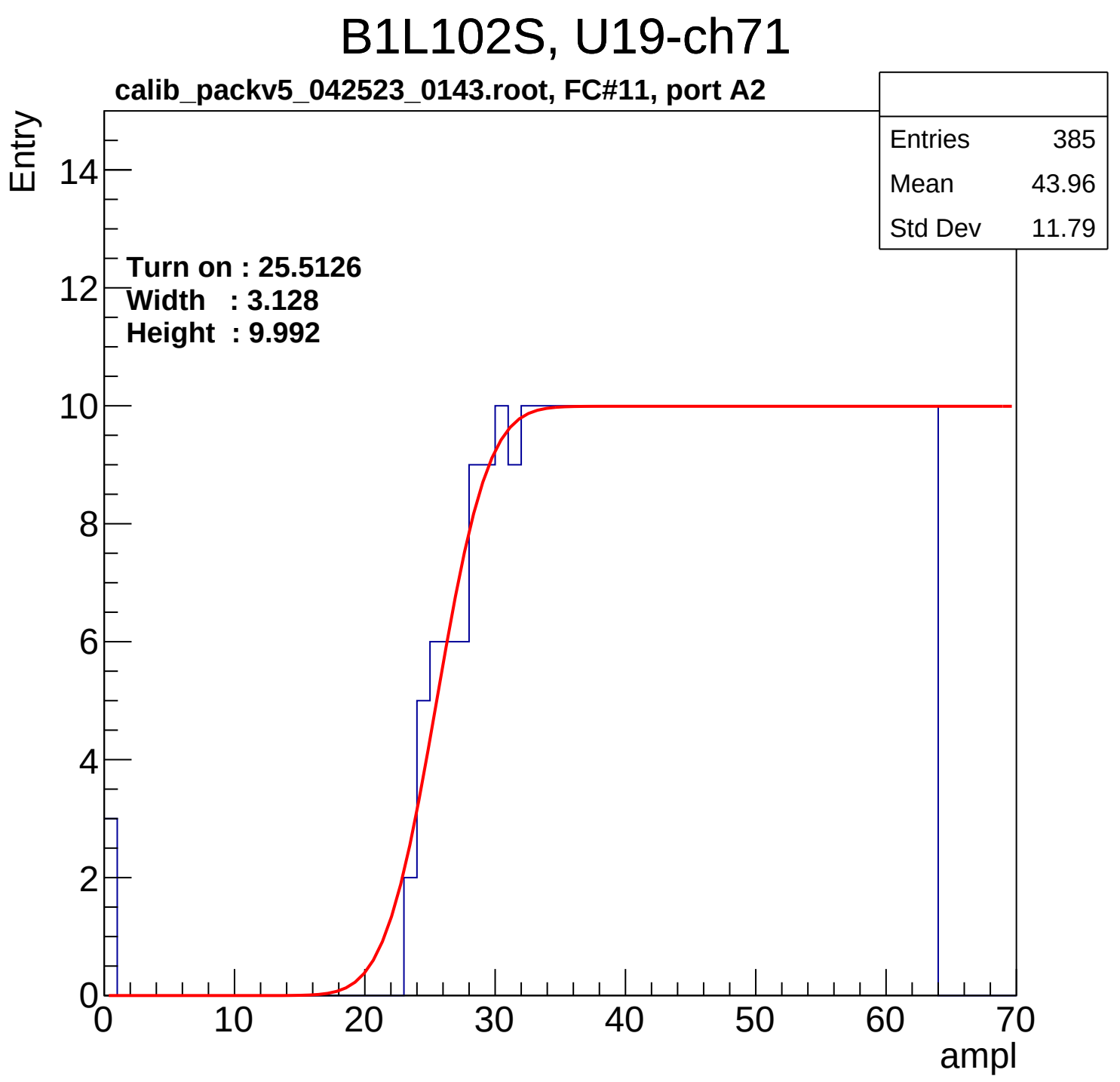

B1L102S, U19-ch66
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.93
Std Dev 11.73
Turn on : 25.7236
Width : 4.108
Height : 10.047
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

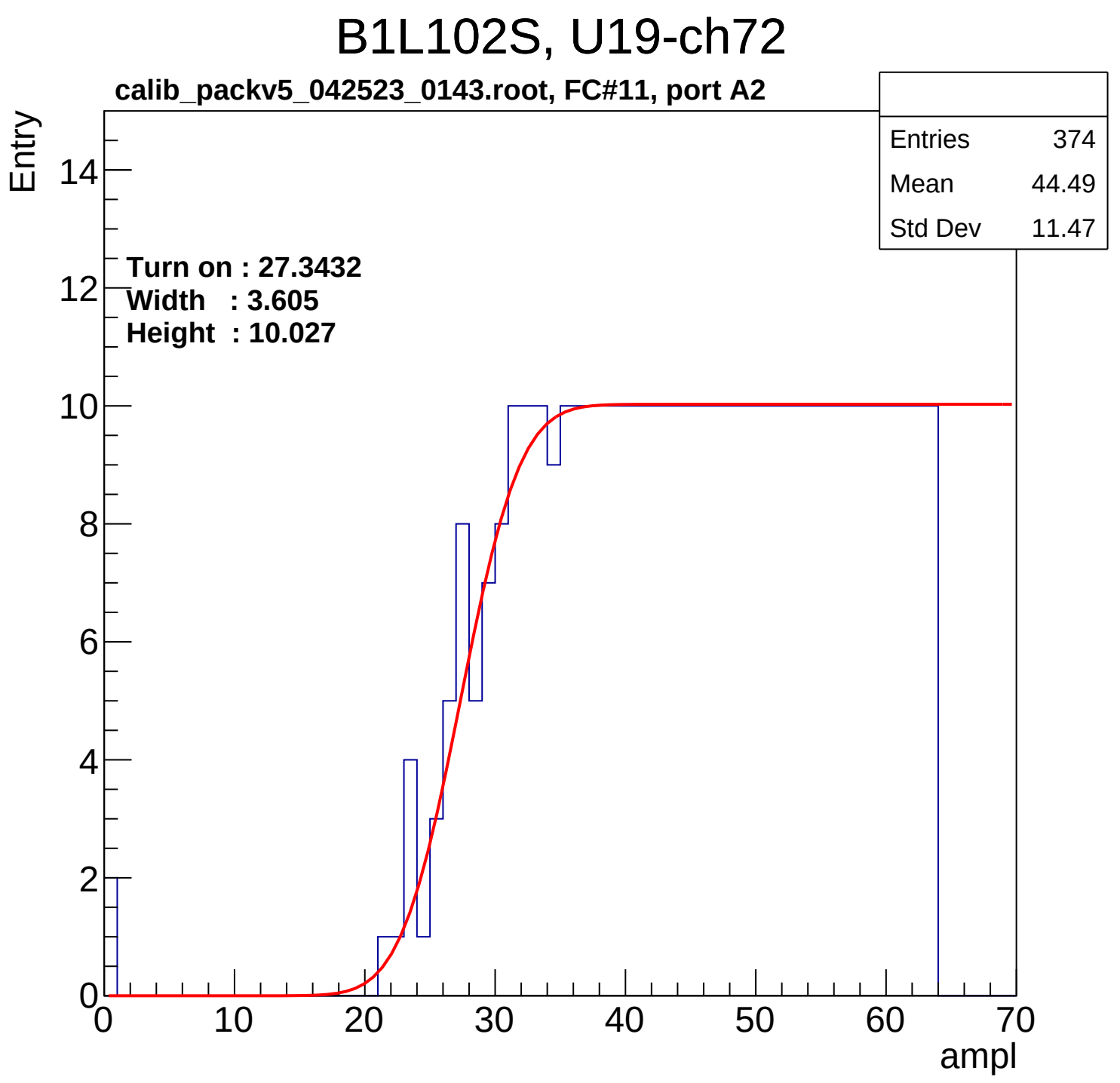

B1L102S, U19-ch67
calib_packv5_042523_0143.root, FC#11, port A2
Entries 372
Mean 44.71
Std Dev 11.14
Turn on : 27.1896
Width : 3.709
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

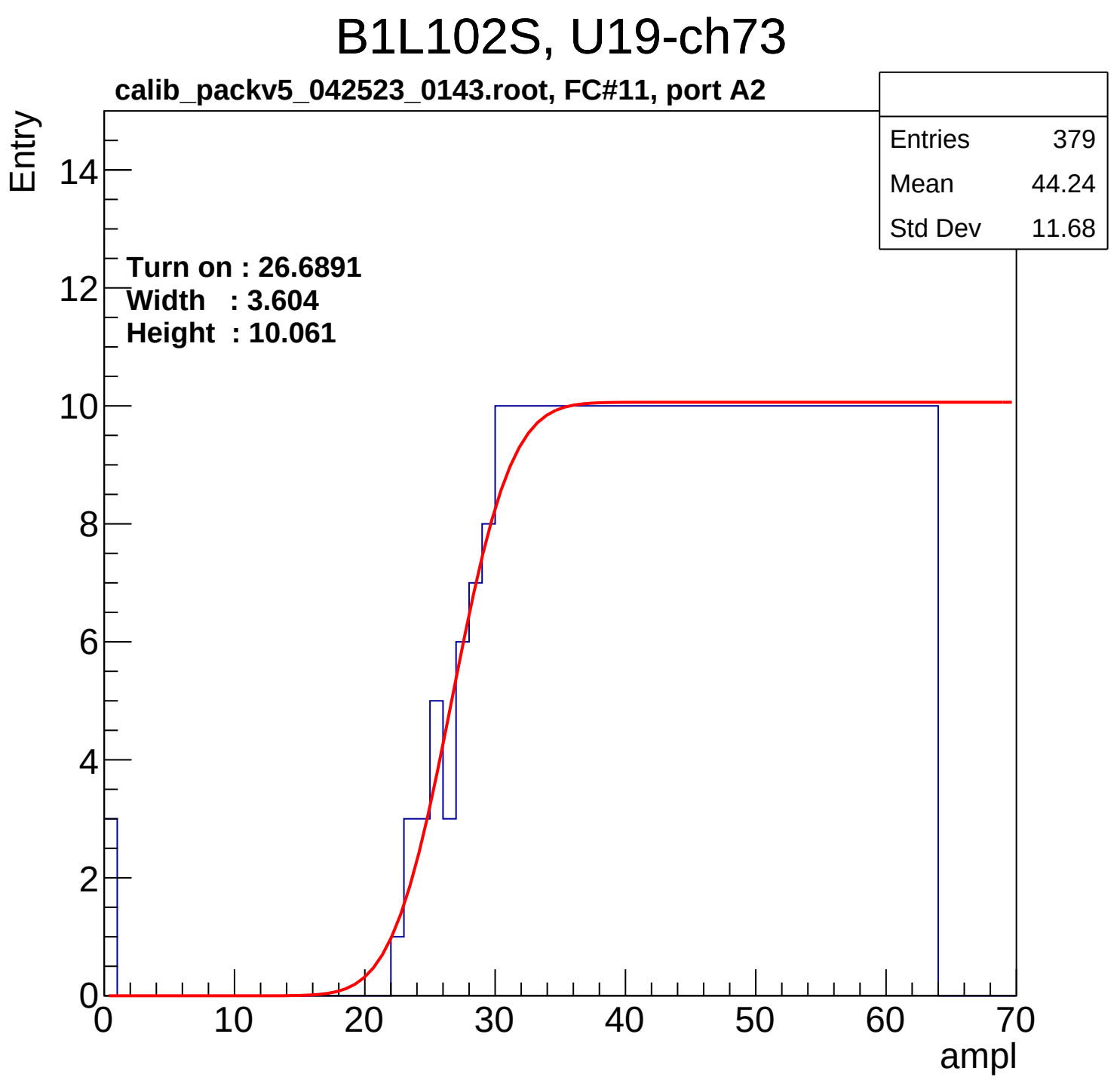

B1L102S, U19-ch68
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.76
Std Dev 11.92
Turn on : 25.8668
Width : 1.258
Height : 9.930
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

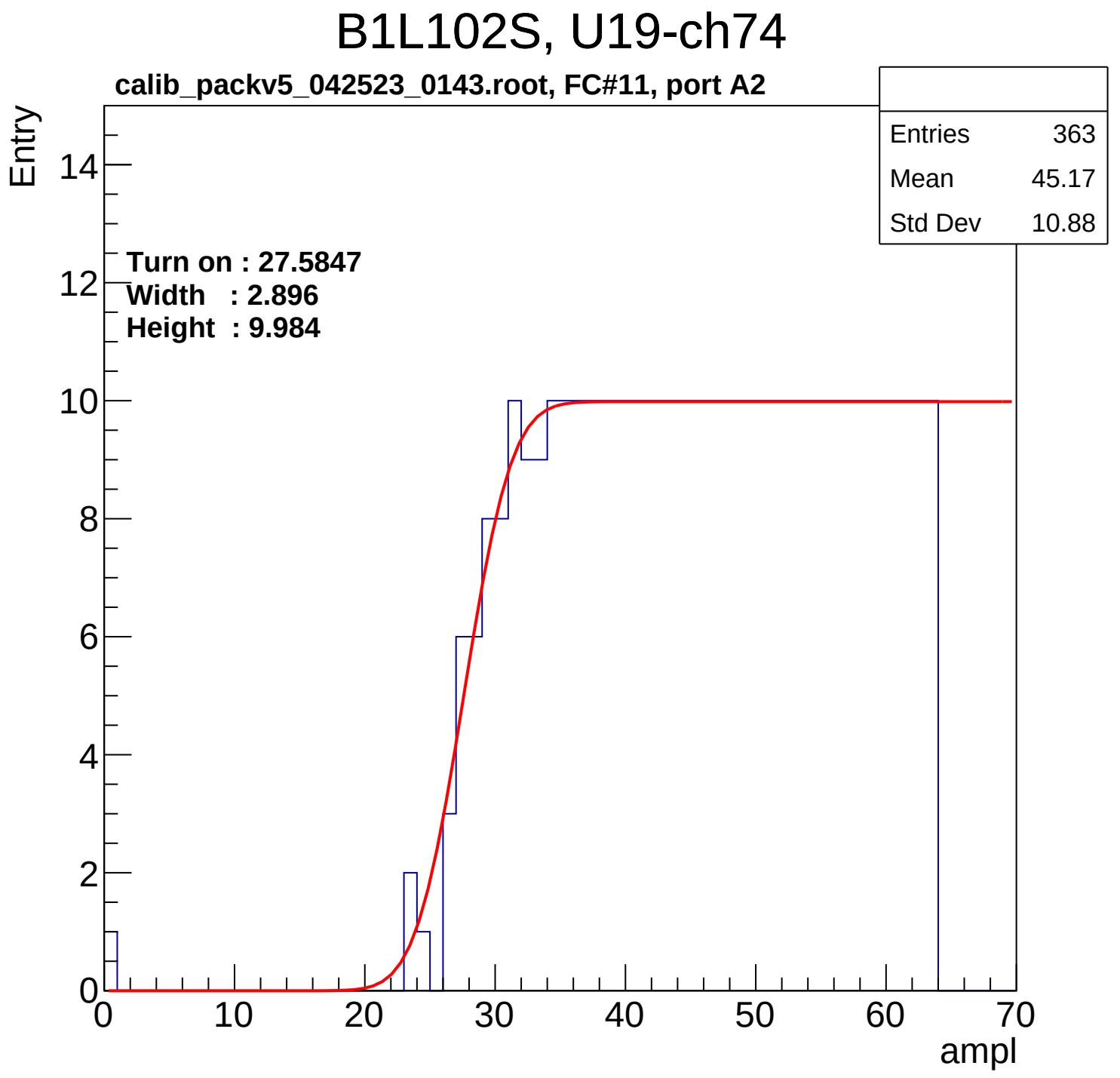

B1L102S, U19-ch69
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.22
Std Dev 11.72
Turn on : 26.9341
Width : 2.553
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

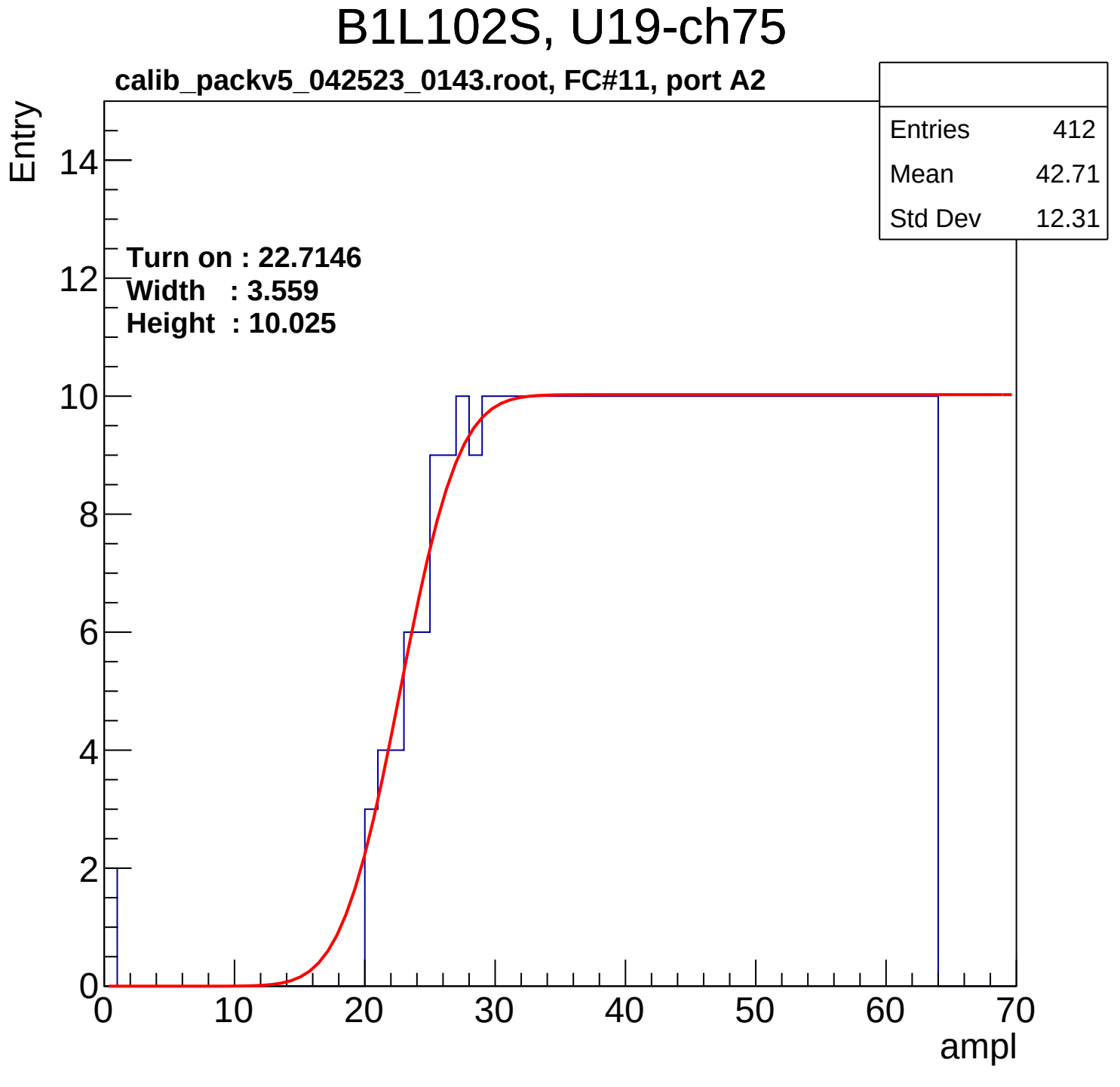

B1L102S, U19-ch70
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.5
Std Dev 12.17
Turn on : 25.1441
Width : 2.595
Height : 9.967
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

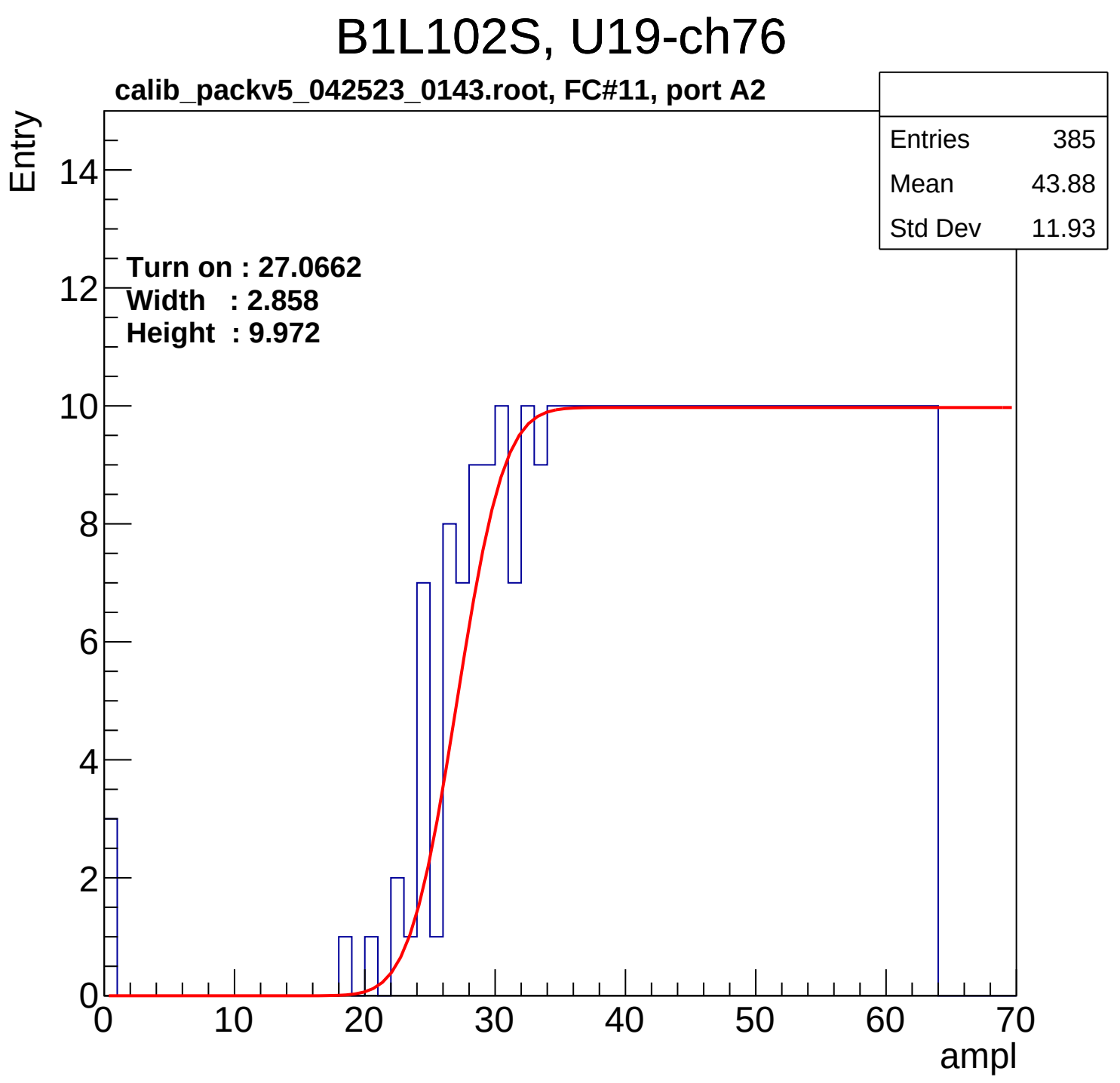

B1L102S, U19-ch71
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.96
Std Dev 11.79
Turn on : 25.5126
Width : 3.128
Height : 9.992
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

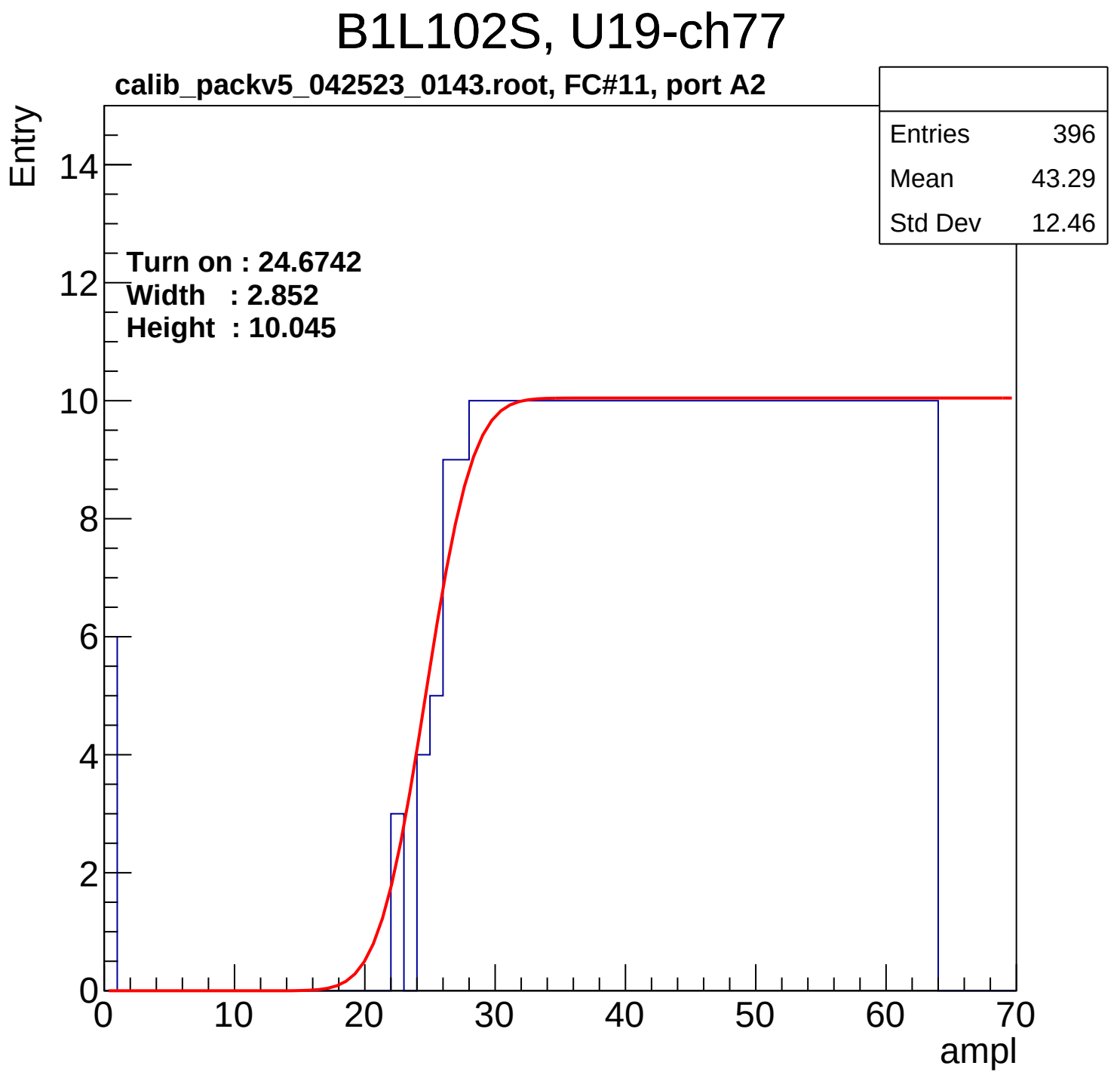

B1L102S, U19-ch72
calib_packv5_042523_0143.root, FC#11, port A2
Entries 374
Mean 44.49
Std Dev 11.47
Turn on : 27.3432
Width : 3.605
Height : 10.027
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

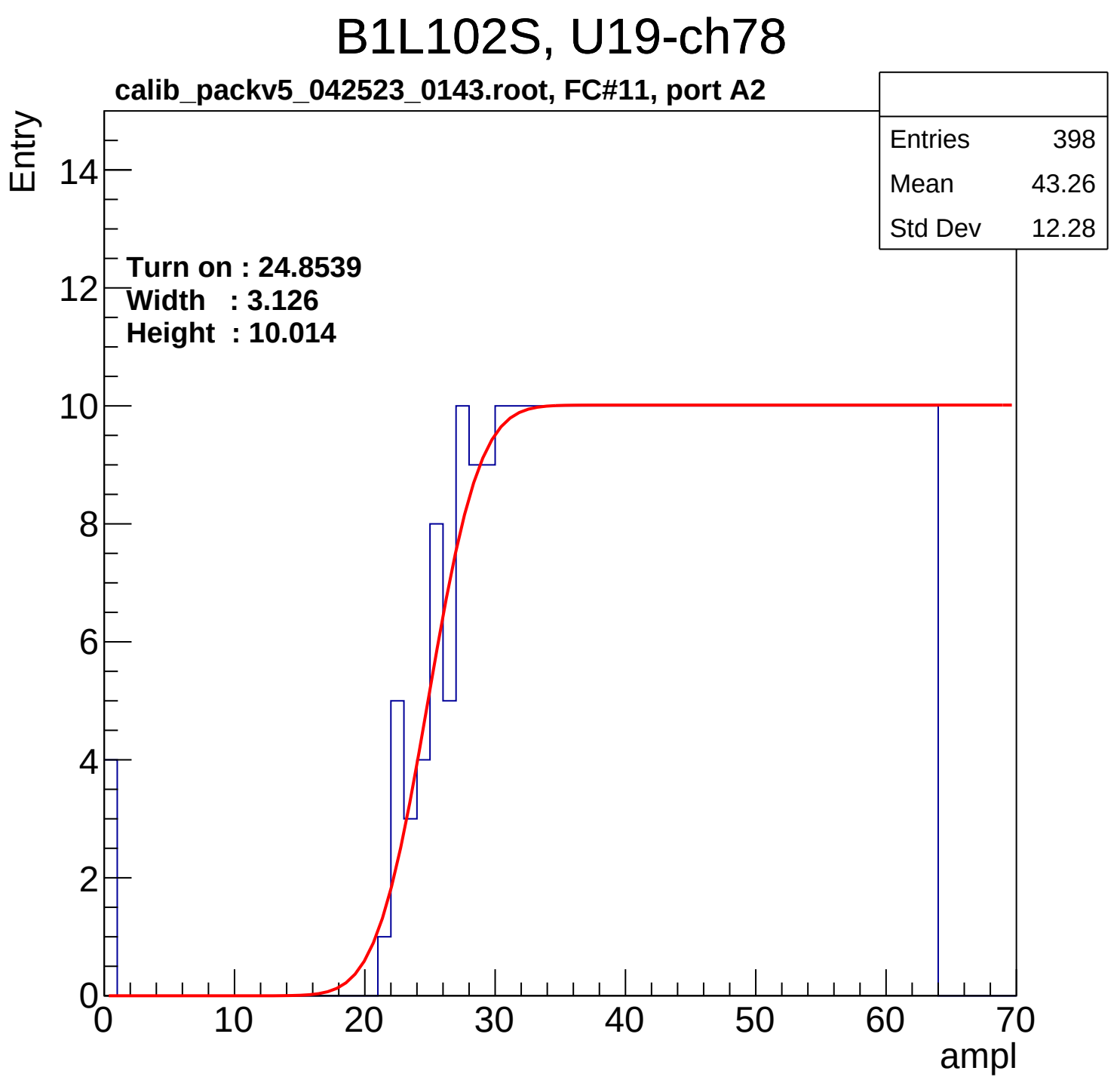

B1L102S, U19-ch73
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.24
Std Dev 11.68
Turn on : 26.6891
Width : 3.604
Height : 10.061
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

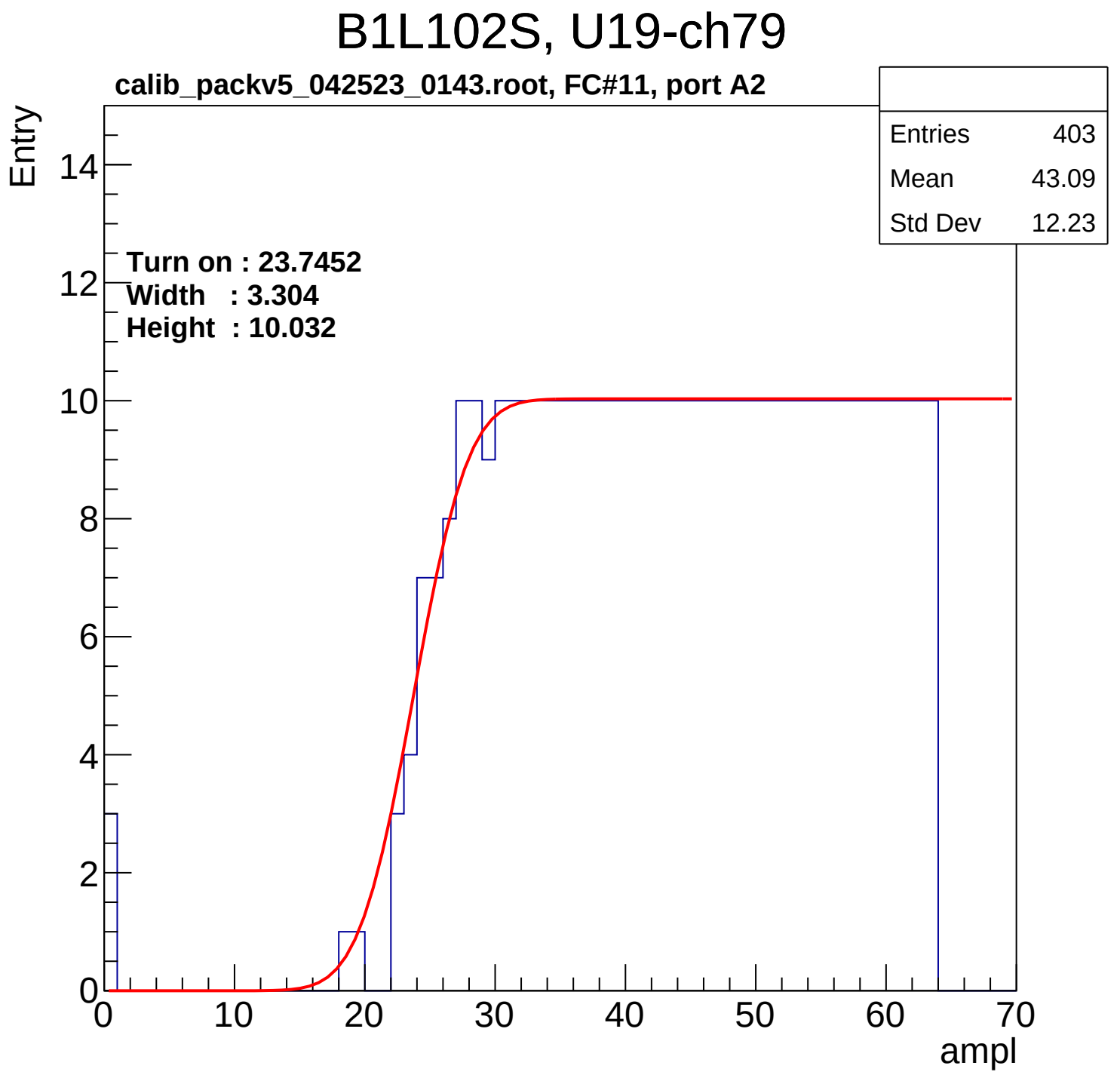

B1L102S, U19-ch74
calib_packv5_042523_0143.root, FC#11, port A2
Entries 363
Mean 45.17
Std Dev 10.88
Turn on : 27.5847
Width : 2.896
Height : 9.984
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

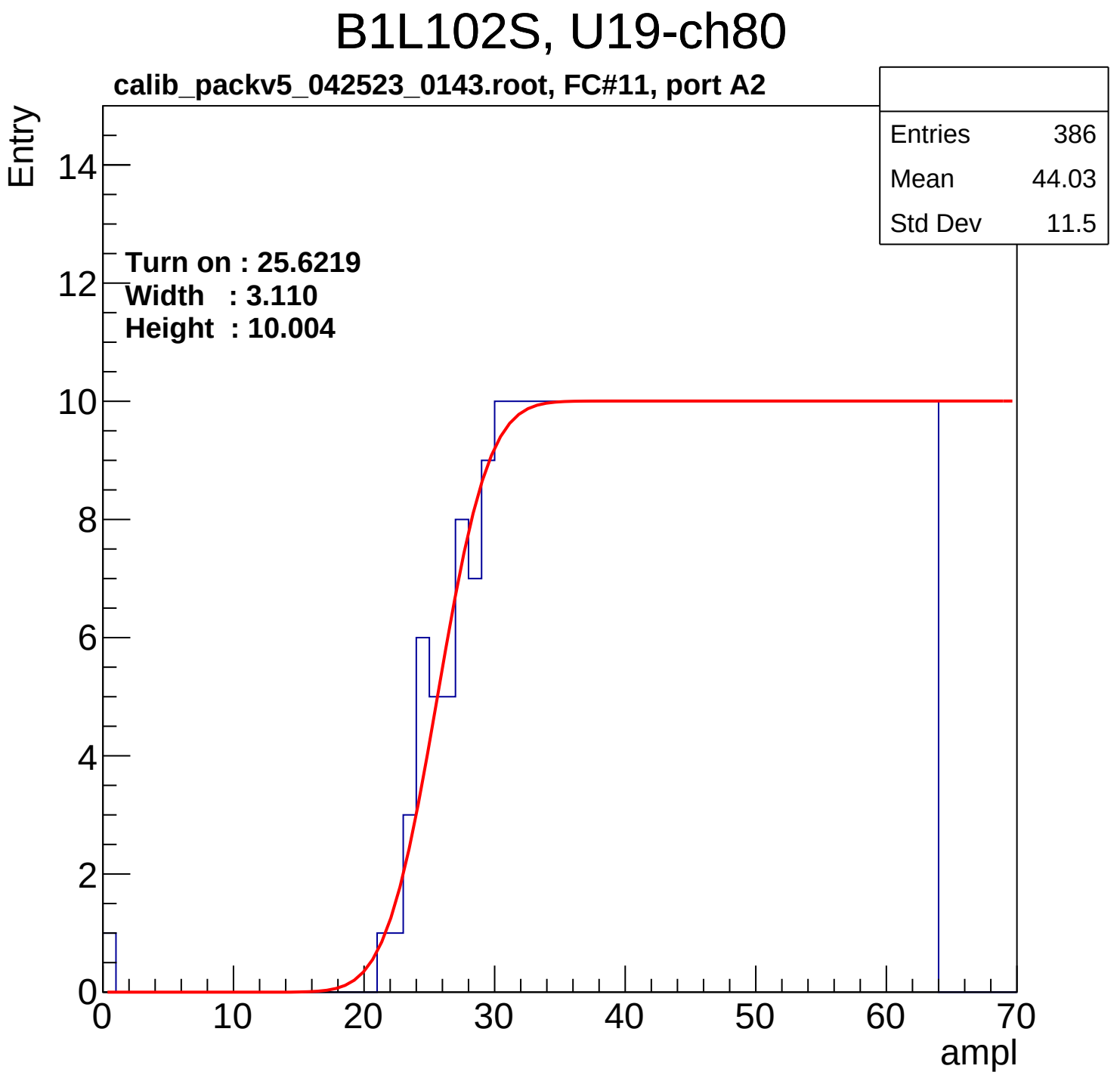

B1L102S, U19-ch75
calib_packv5_042523_0143.root, FC#11, port A2
Entries 412
Mean 42.71
Std Dev 12.31
Turn on : 22.7146
Width : 3.559
Height : 10.025
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

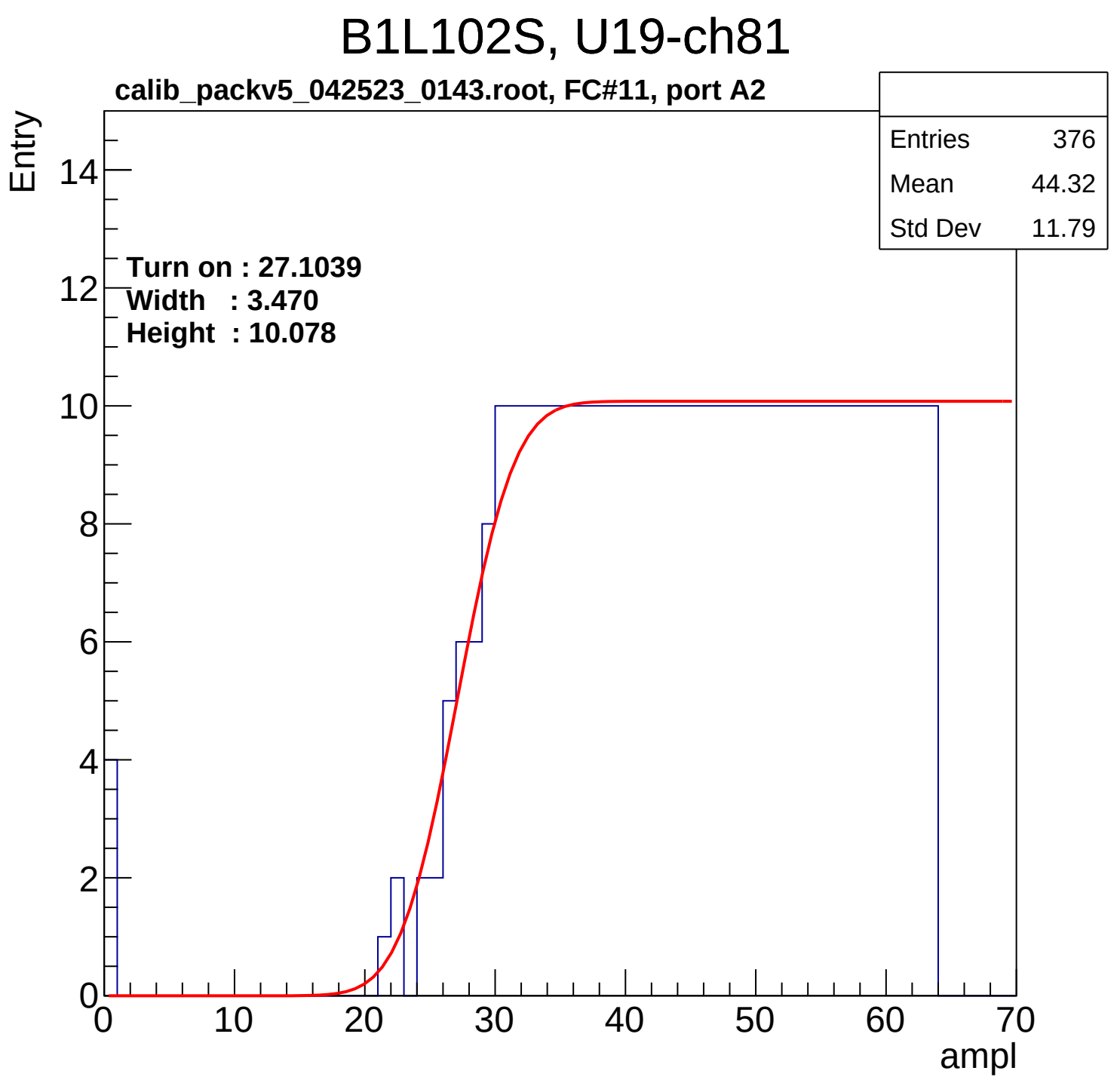

B1L102S, U19-ch76
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.88
Std Dev 11.93
Turn on : 27.0662
Width : 2.858
Height : 9.972
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

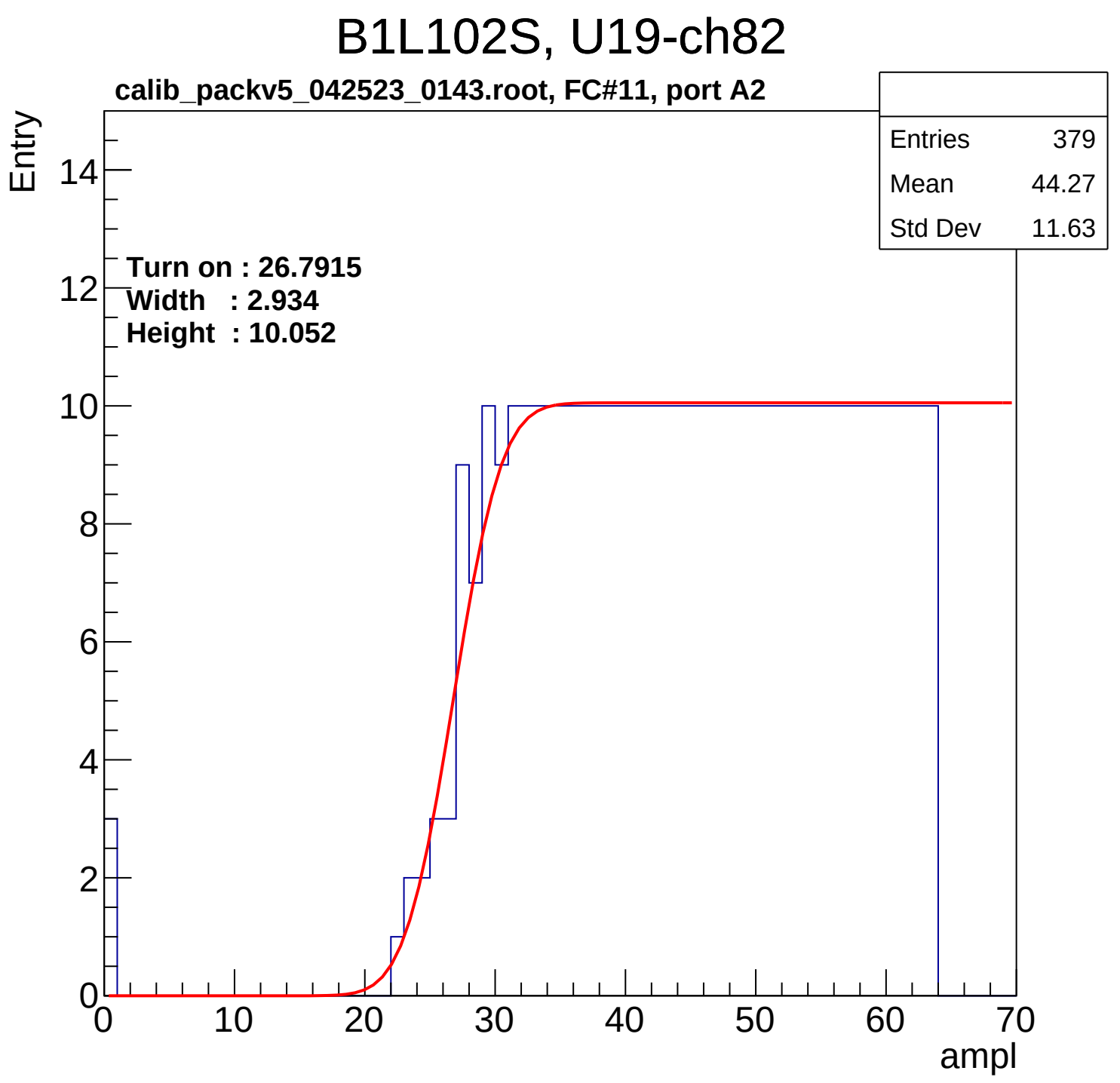

B1L102S, U19-ch77
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.29
Std Dev 12.46
Turn on : 24.6742
Width : 2.852
Height : 10.045
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

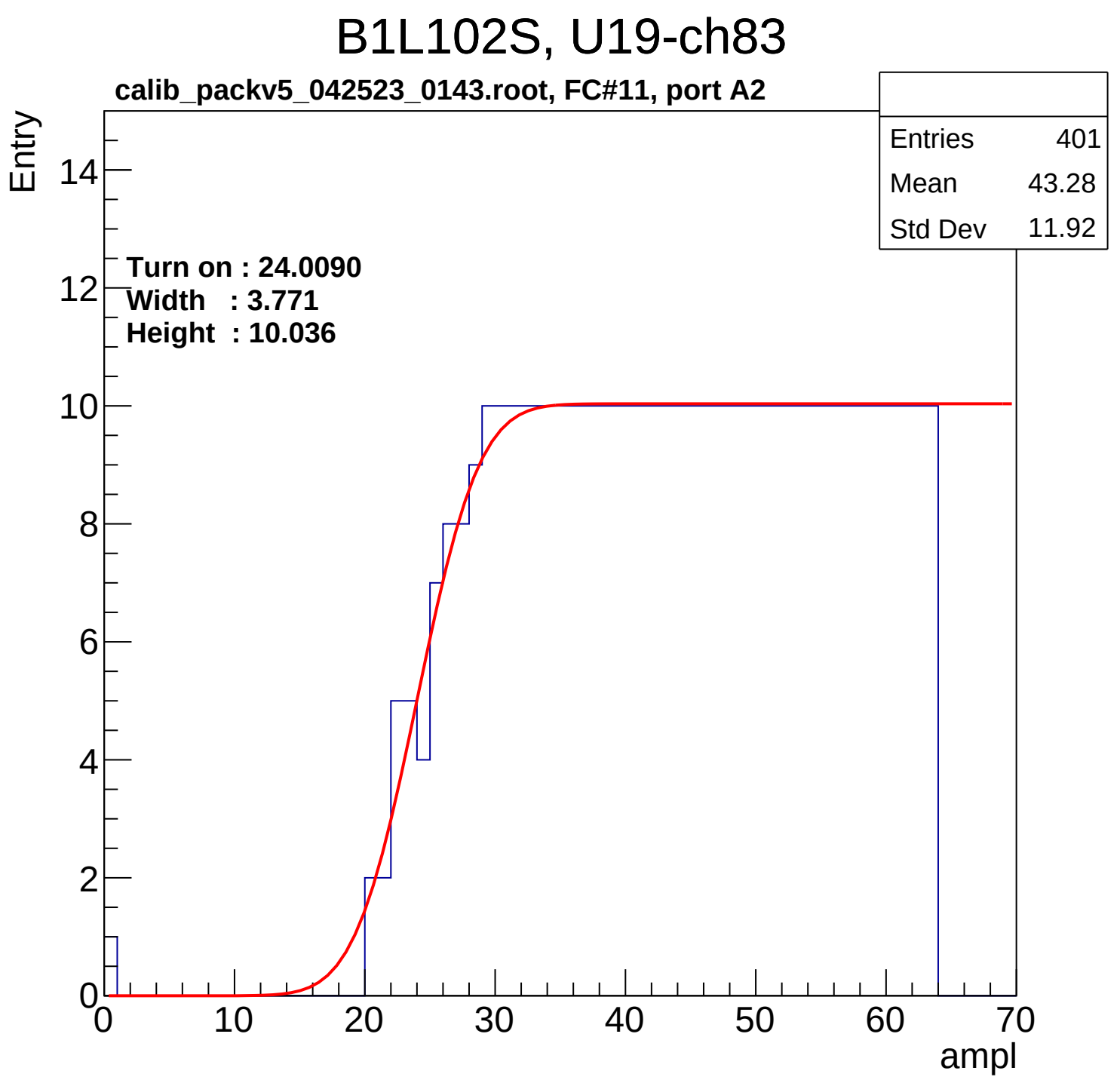

B1L102S, U19-ch78
calib_packv5_042523_0143.root, FC#11, port A2
Entries 398
Mean 43.26
Std Dev 12.28
Turn on : 24.8539
Width : 3.126
Height : 10.014
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

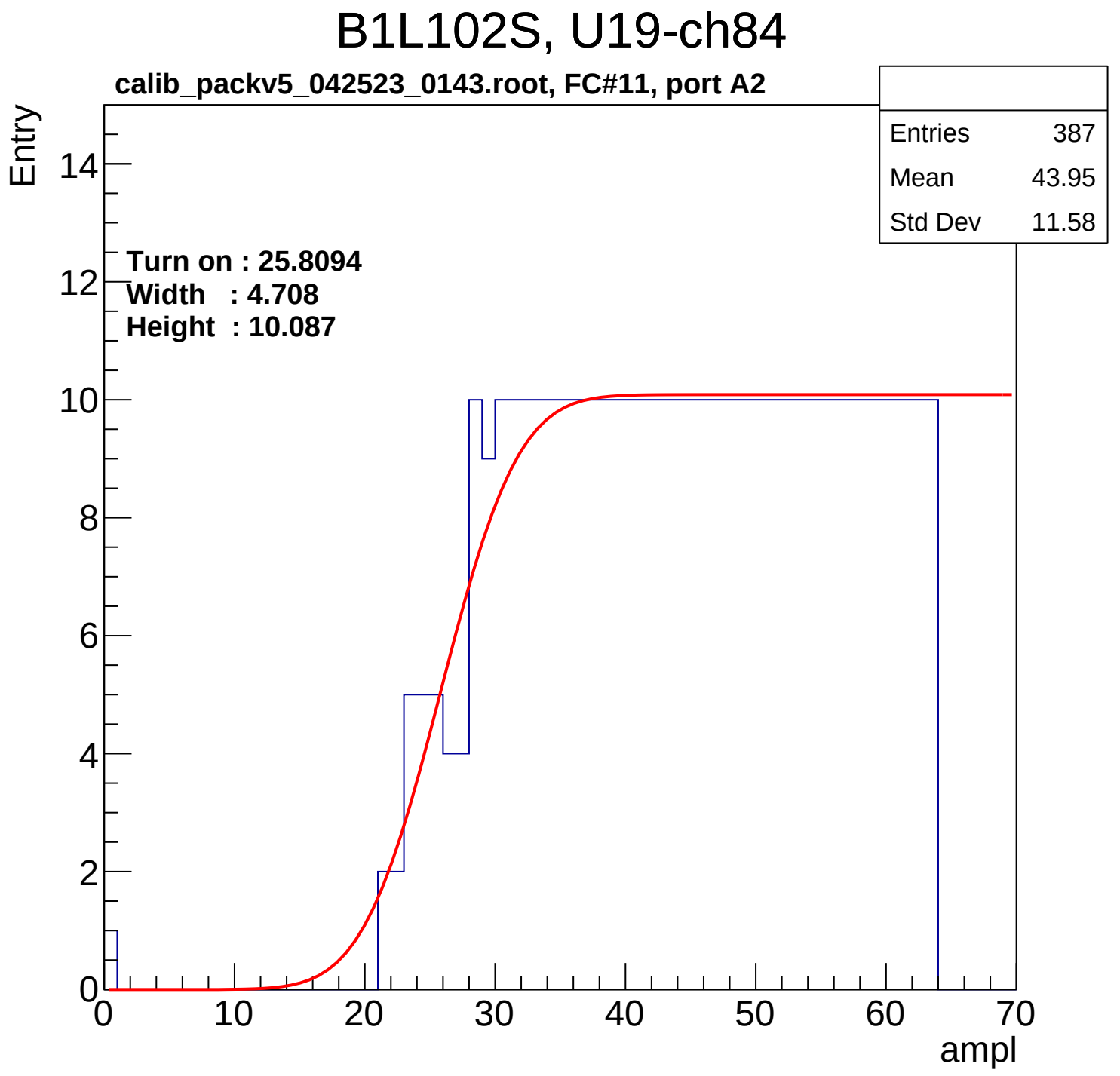

B1L102S, U19-ch79
calib_packv5_042523_0143.root, FC#11, port A2
Entries 403
Mean 43.09
Std Dev 12.23
Turn on : 23.7452
Width : 3.304
Height : 10.032
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

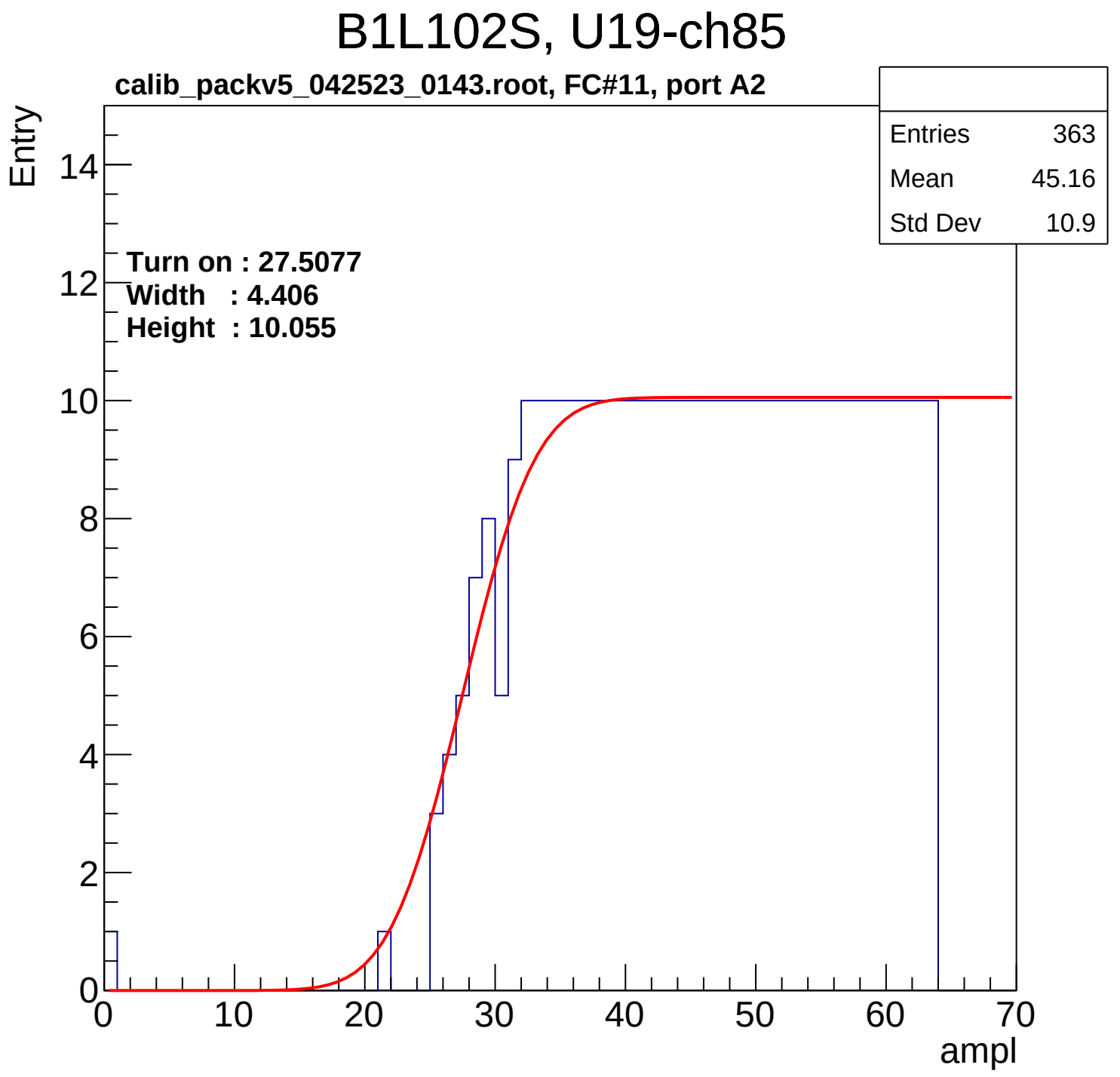

B1L102S, U19-ch80
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 44.03
Std Dev 11.5
Turn on : 25.6219
Width : 3.110
Height : 10.004
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

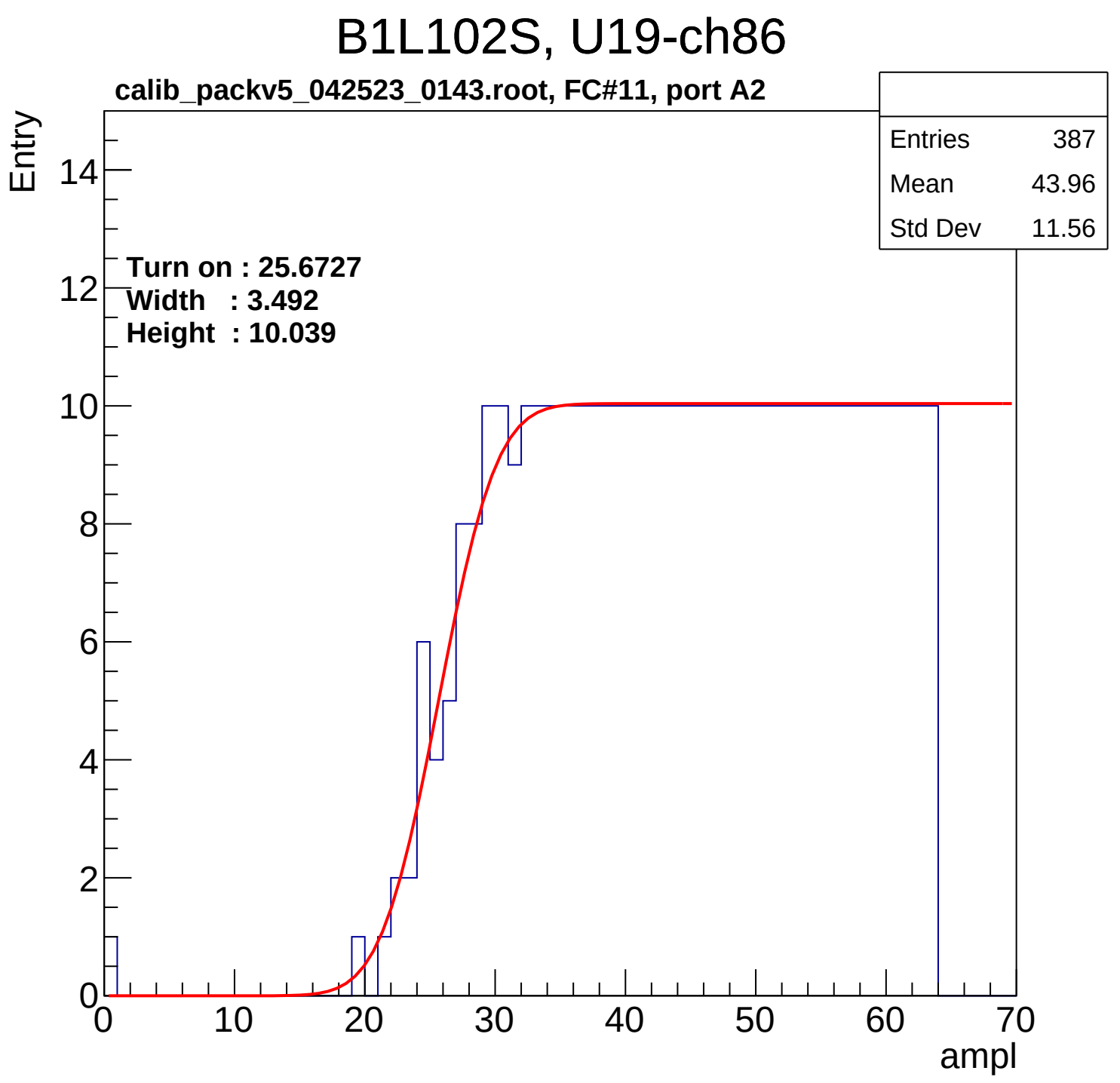

B1L102S, U19-ch81
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.32
Std Dev 11.79
Turn on : 27.1039
Width : 3.470
Height : 10.078
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

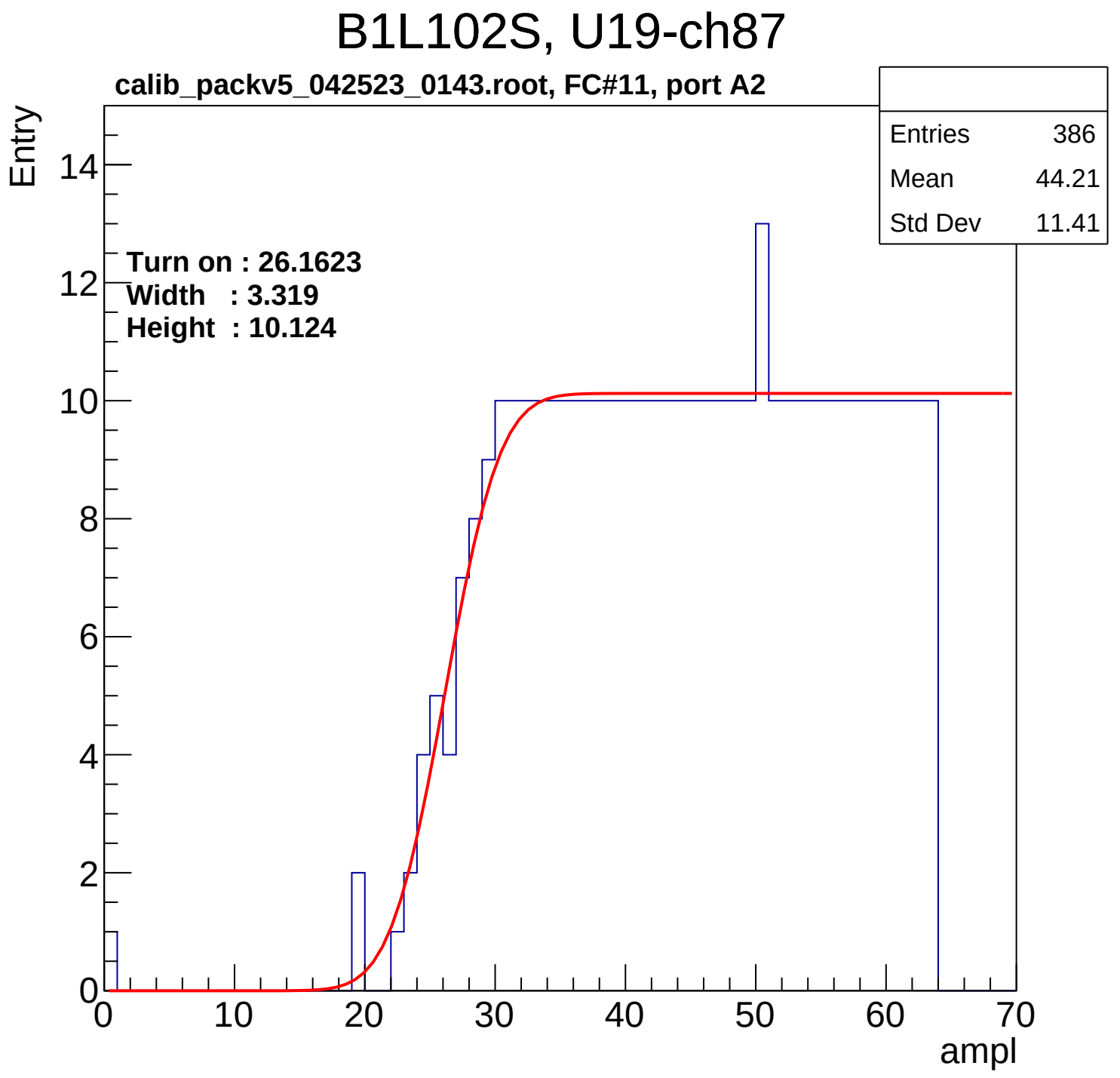

B1L102S, U19-ch82
calib_packv5_042523_0143.root, FC#11, port A2
Entries 379
Mean 44.27
Std Dev 11.63
Turn on : 26.7915
Width : 2.934
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

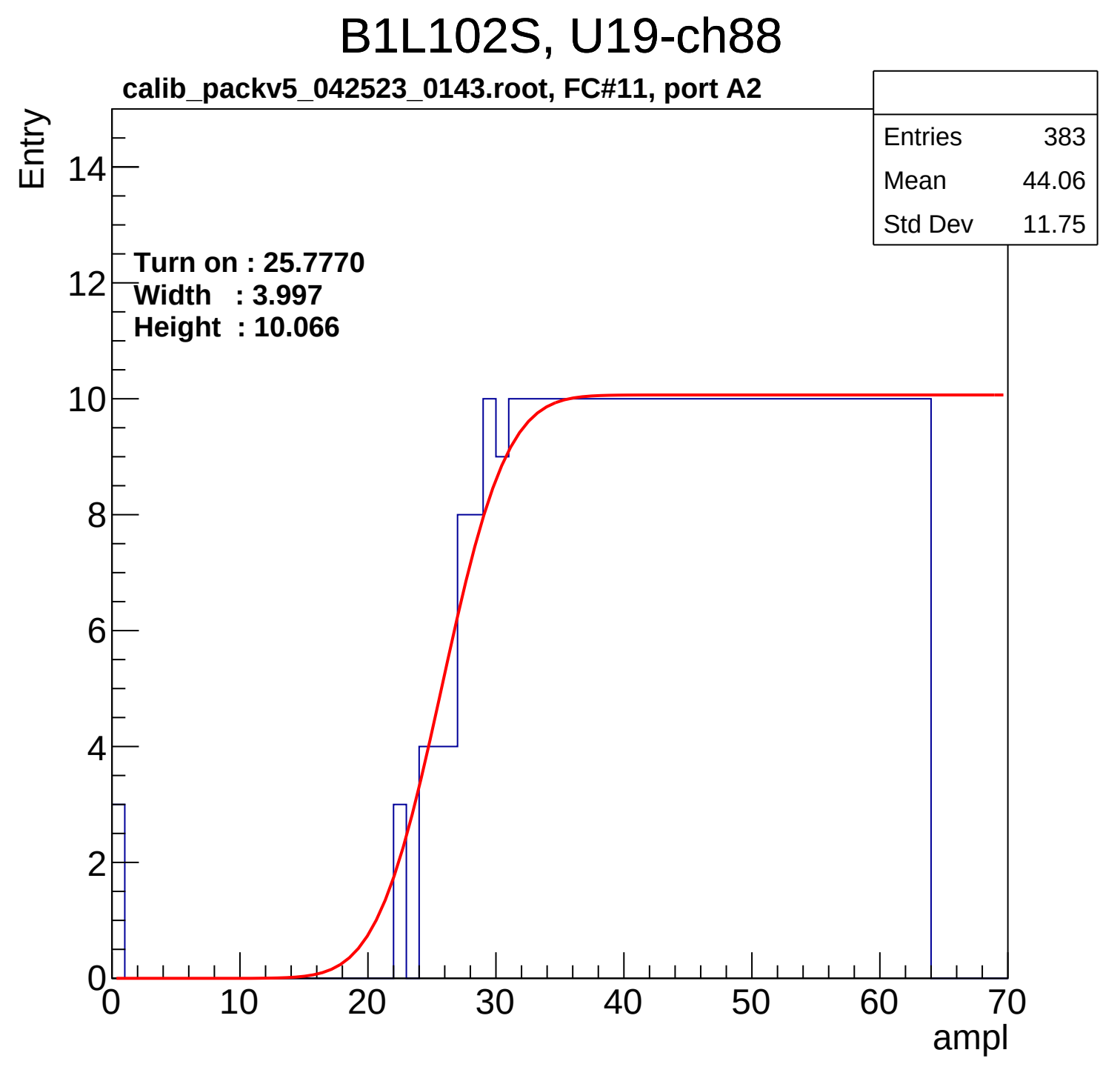

B1L102S, U19-ch83
calib_packv5_042523_0143.root, FC#11, port A2
Entries 401
Mean 43.28
Std Dev 11.92
Turn on : 24.0090
Width : 3.771
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

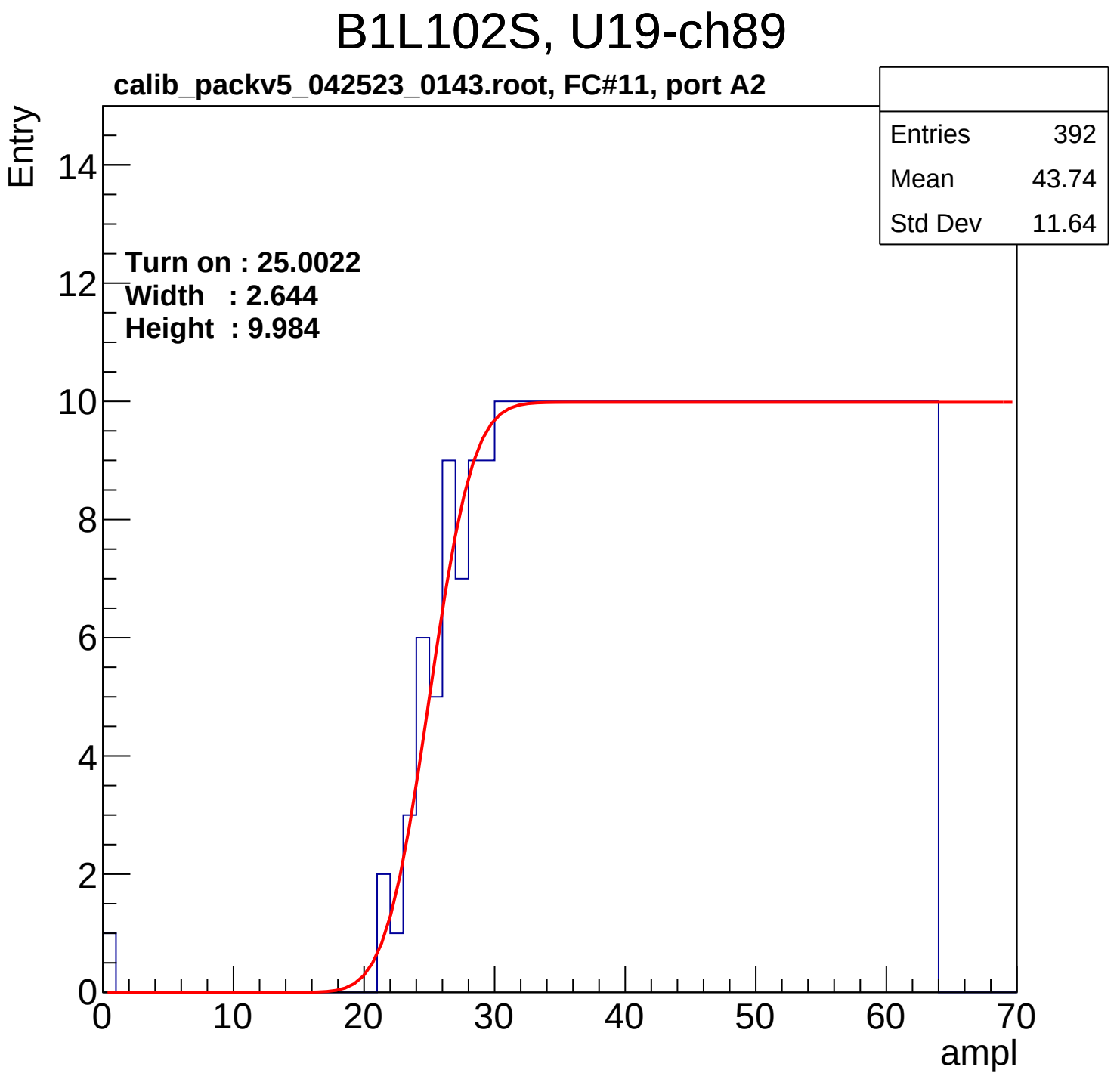

B1L102S, U19-ch84
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.95
Std Dev 11.58
Turn on : 25.8094
Width : 4.708
Height : 10.087
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

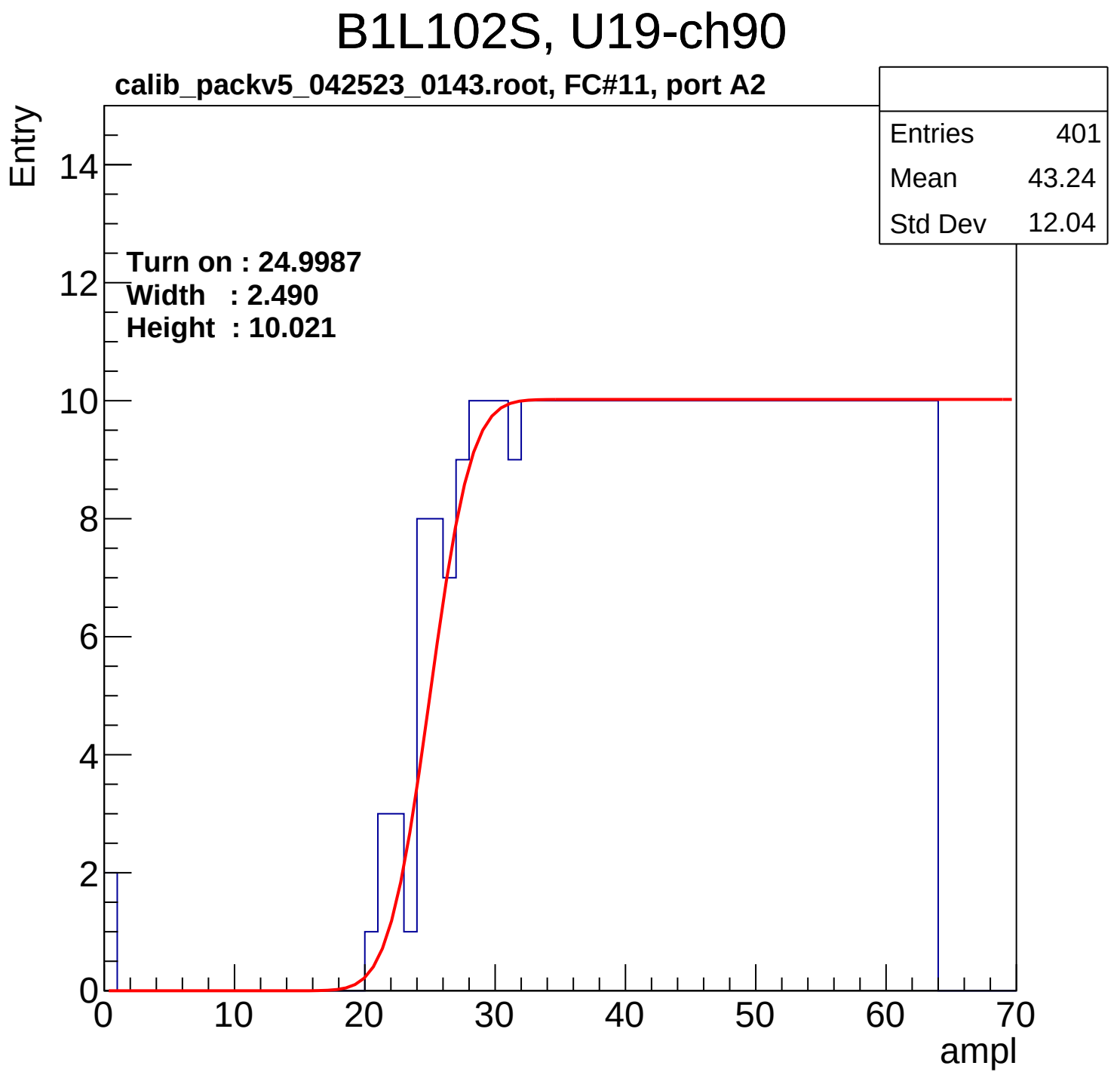

B1L102S, U19-ch85
calib_packv5_042523_0143.root, FC#11, port A2
Entries 363
Mean 45.16
Std Dev 10.9
Turn on : 27.5077
Width : 4.406
Height : 10.055
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

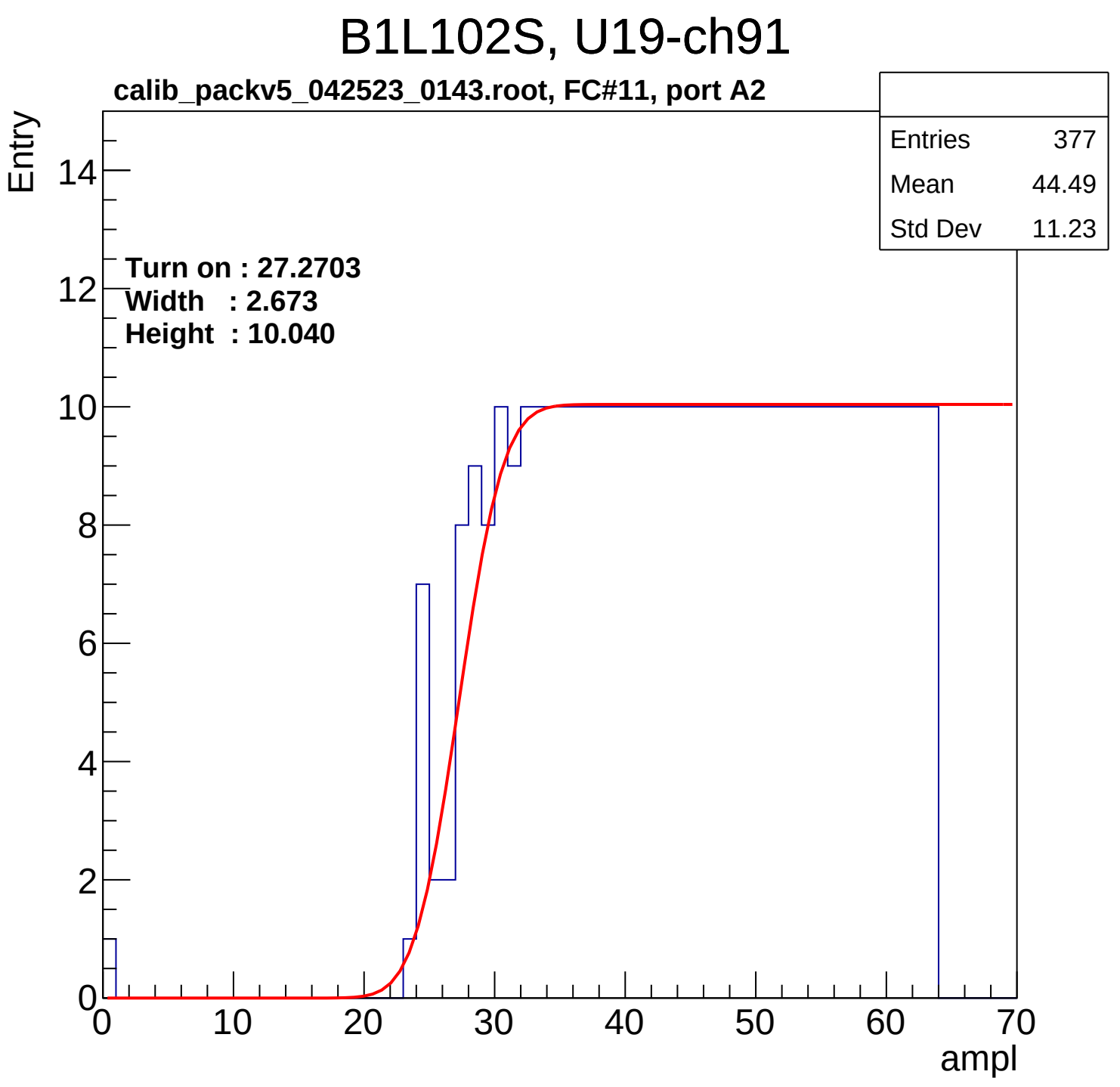

B1L102S, U19-ch86
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.96
Std Dev 11.56
Turn on : 25.6727
Width : 3.492
Height : 10.039
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

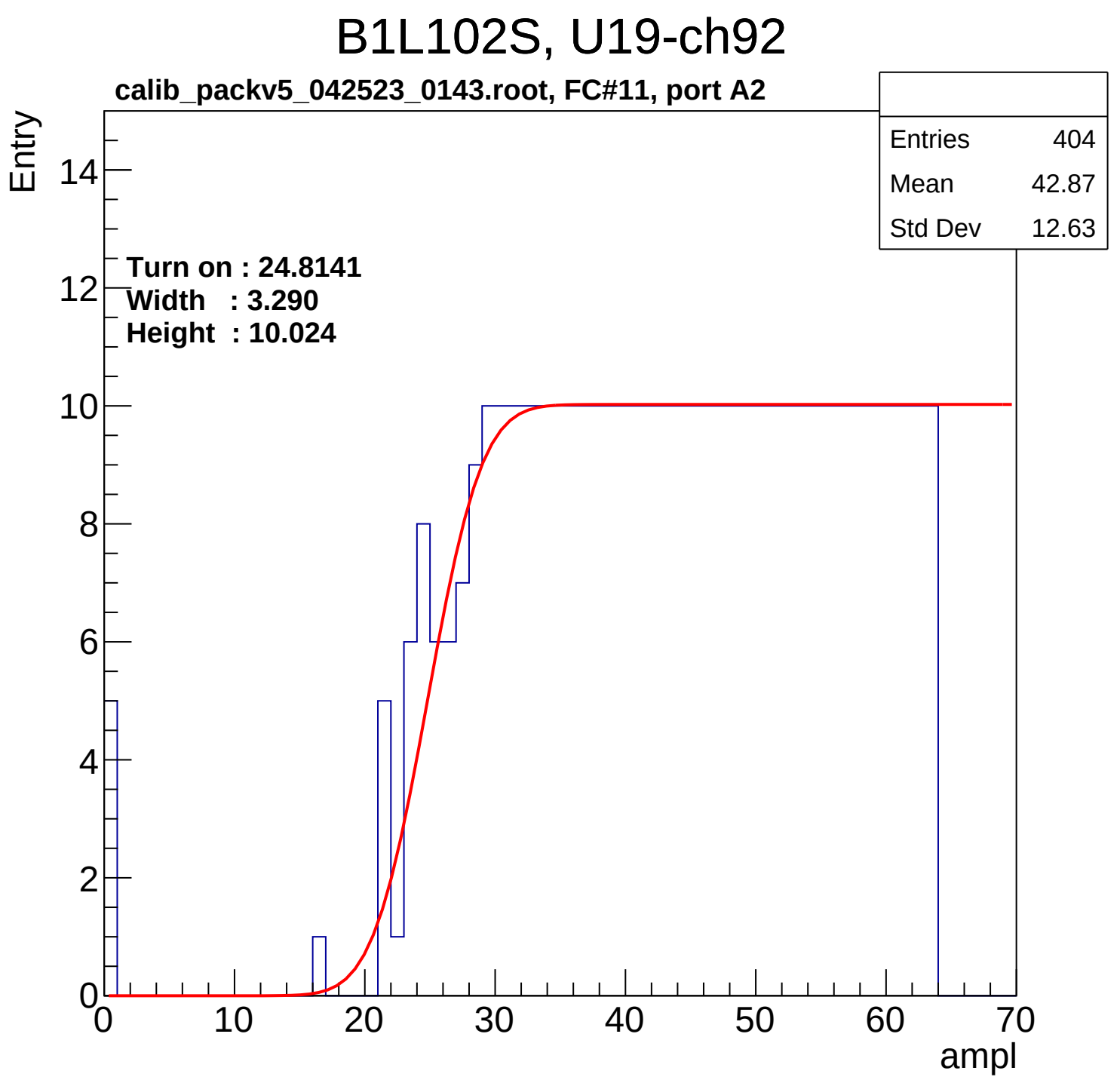

B1L102S, U19-ch87
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 44.21
Std Dev 11.41
Turn on : 26.1623
Width : 3.319
Height : 10.124
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

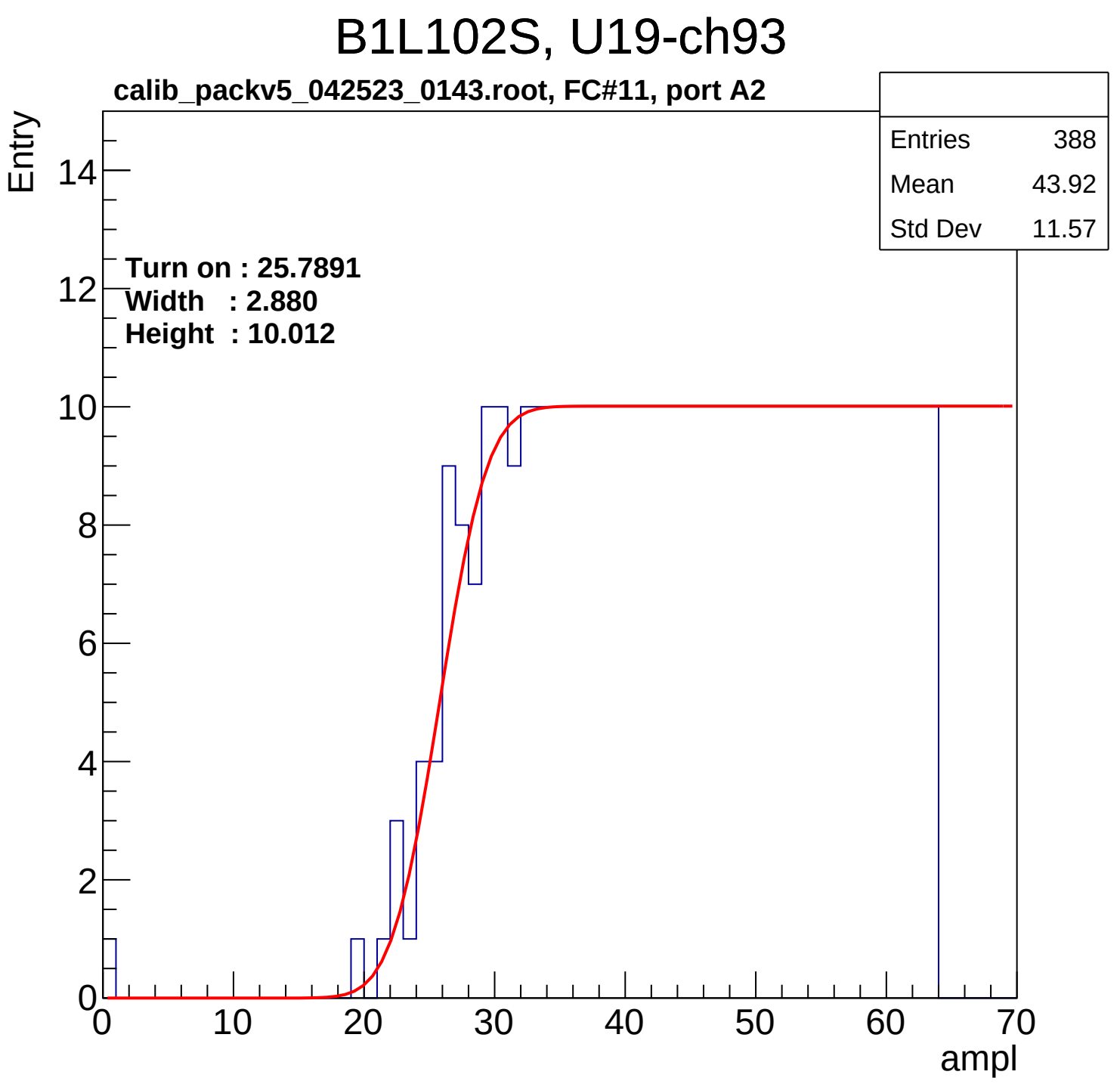

B1L102S, U19-ch88
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.06
Std Dev 11.75
Turn on : 25.7770
Width : 3.997
Height : 10.066
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

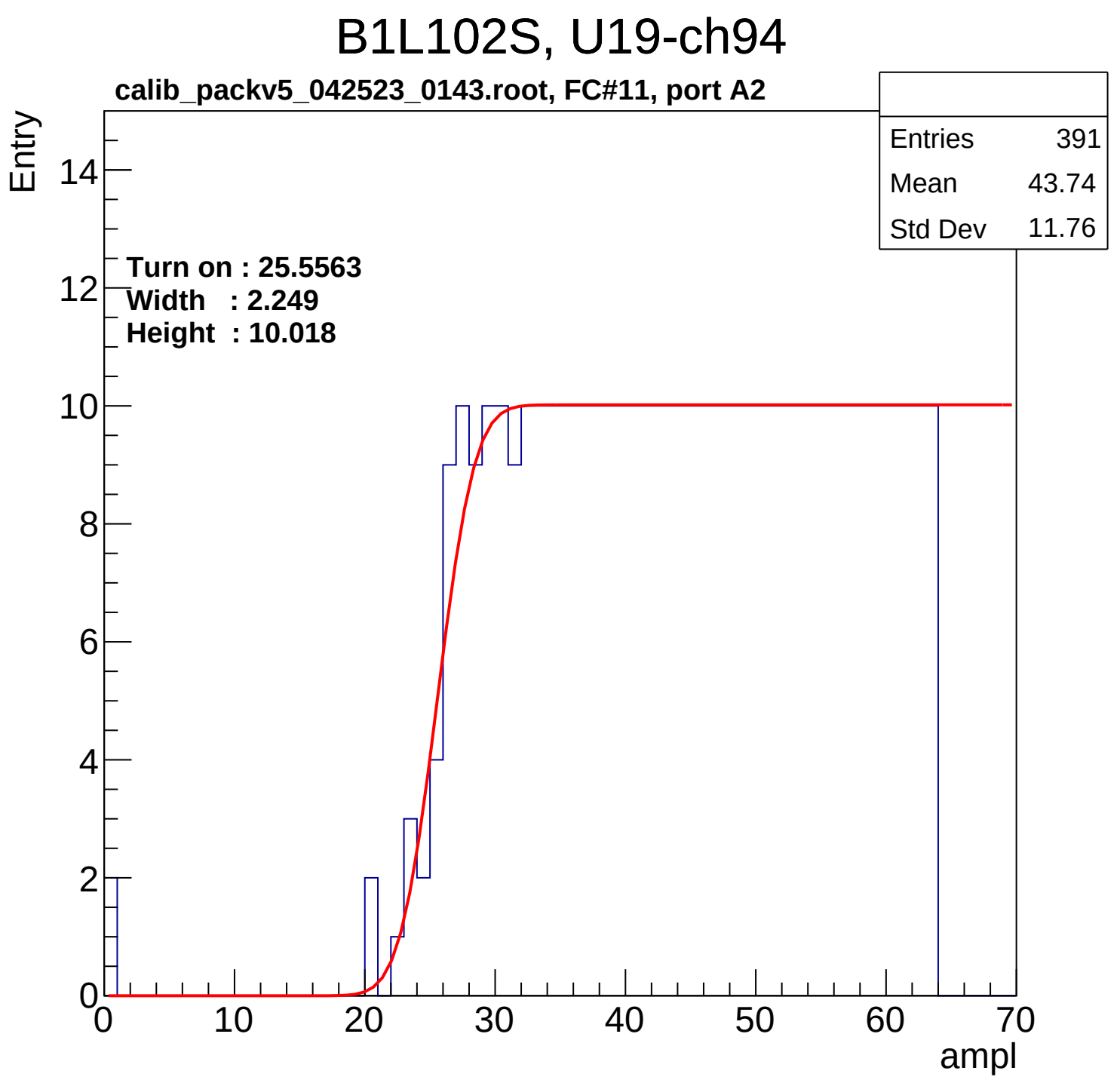

B1L102S, U19-ch89
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.74
Std Dev 11.64
Turn on : 25.0022
Width : 2.644
Height : 9.984
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

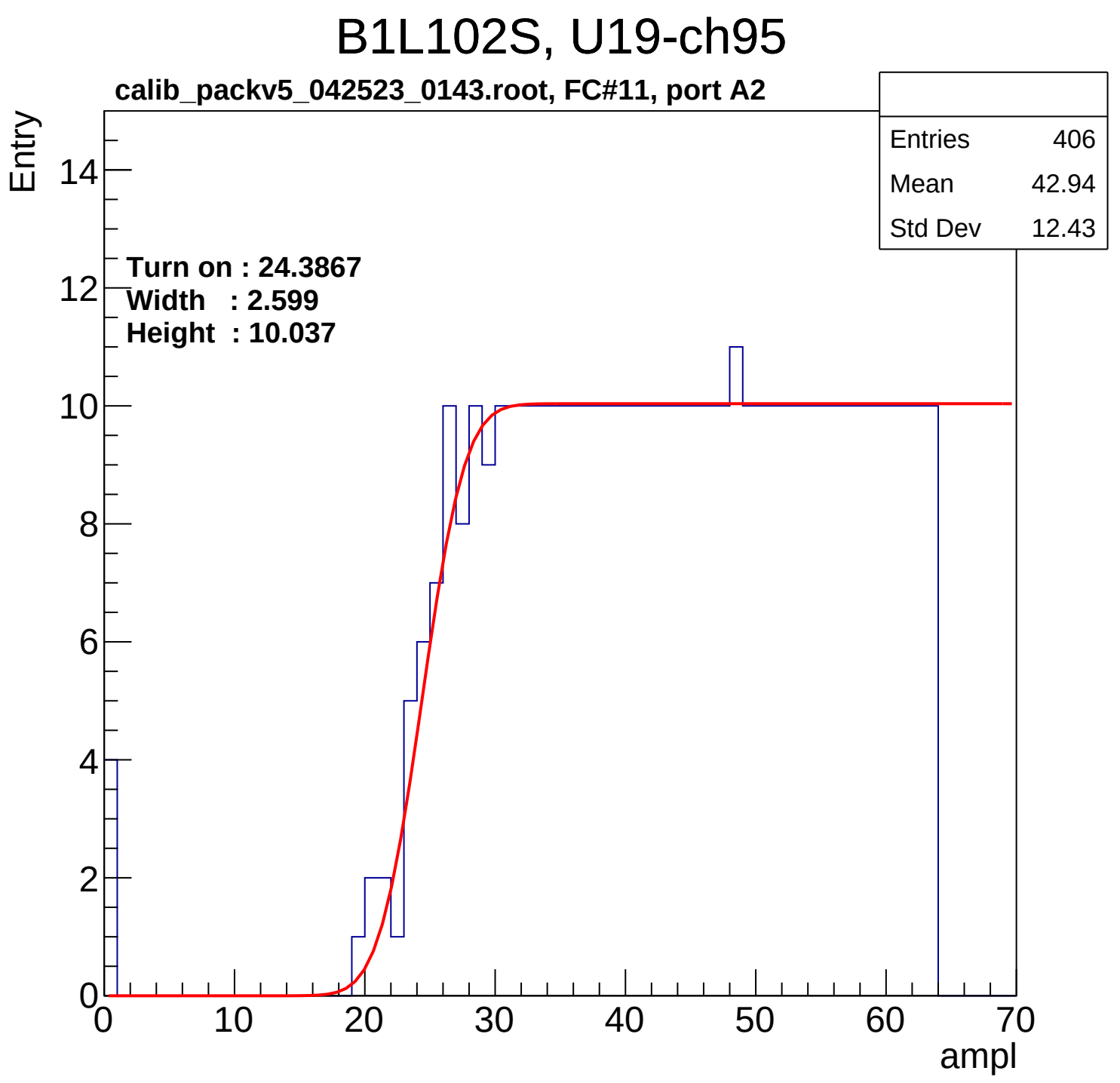

B1L102S, U19-ch90
calib_packv5_042523_0143.root, FC#11, port A2
Entries 401
Mean 43.24
Std Dev 12.04
Turn on : 24.9987
Width : 2.490
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

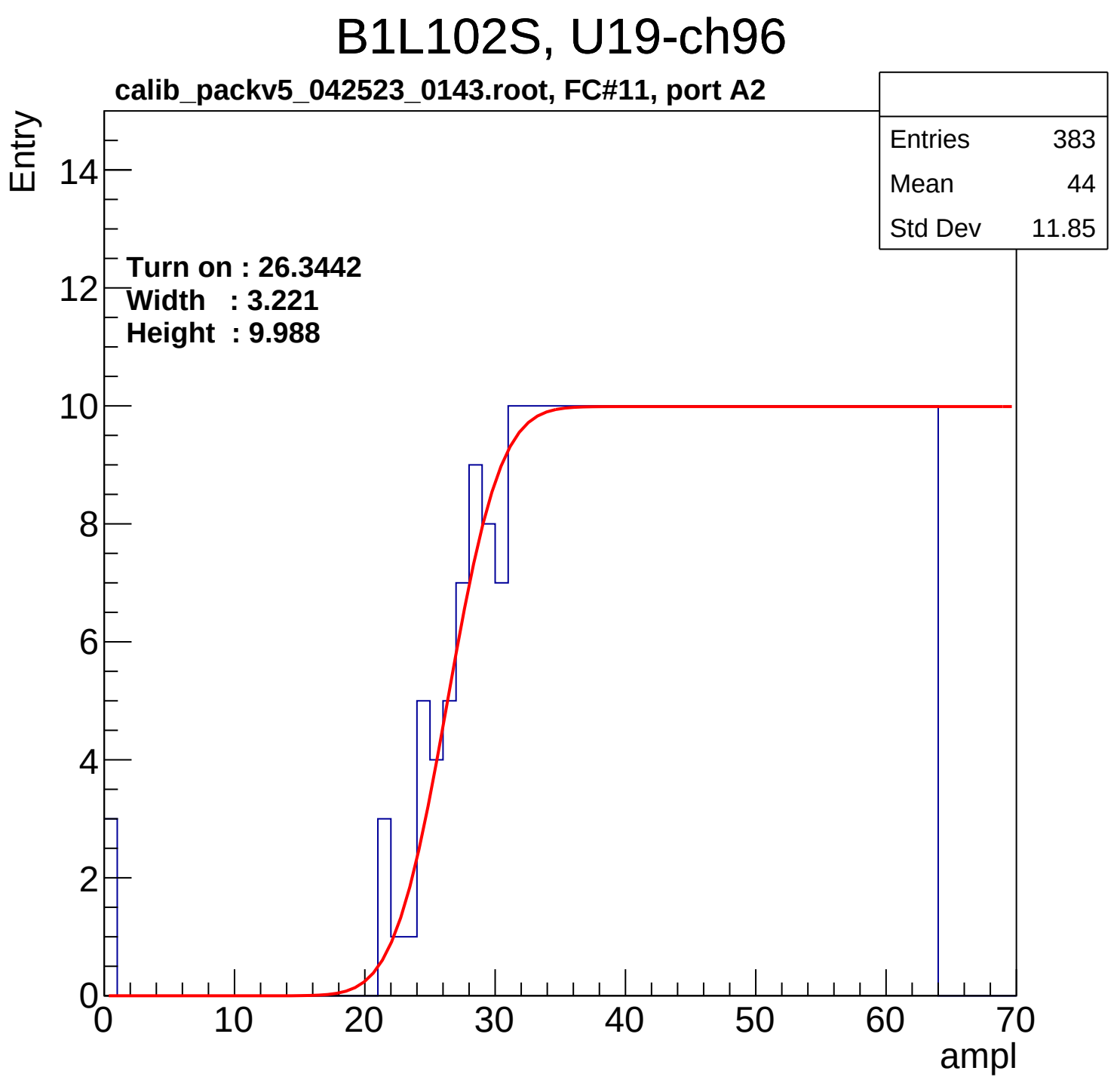

B1L102S, U19-ch91
calib_packv5_042523_0143.root, FC#11, port A2
Entries 377
Mean 44.49
Std Dev 11.23
Turn on : 27.2703
Width : 2.673
Height : 10.040
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

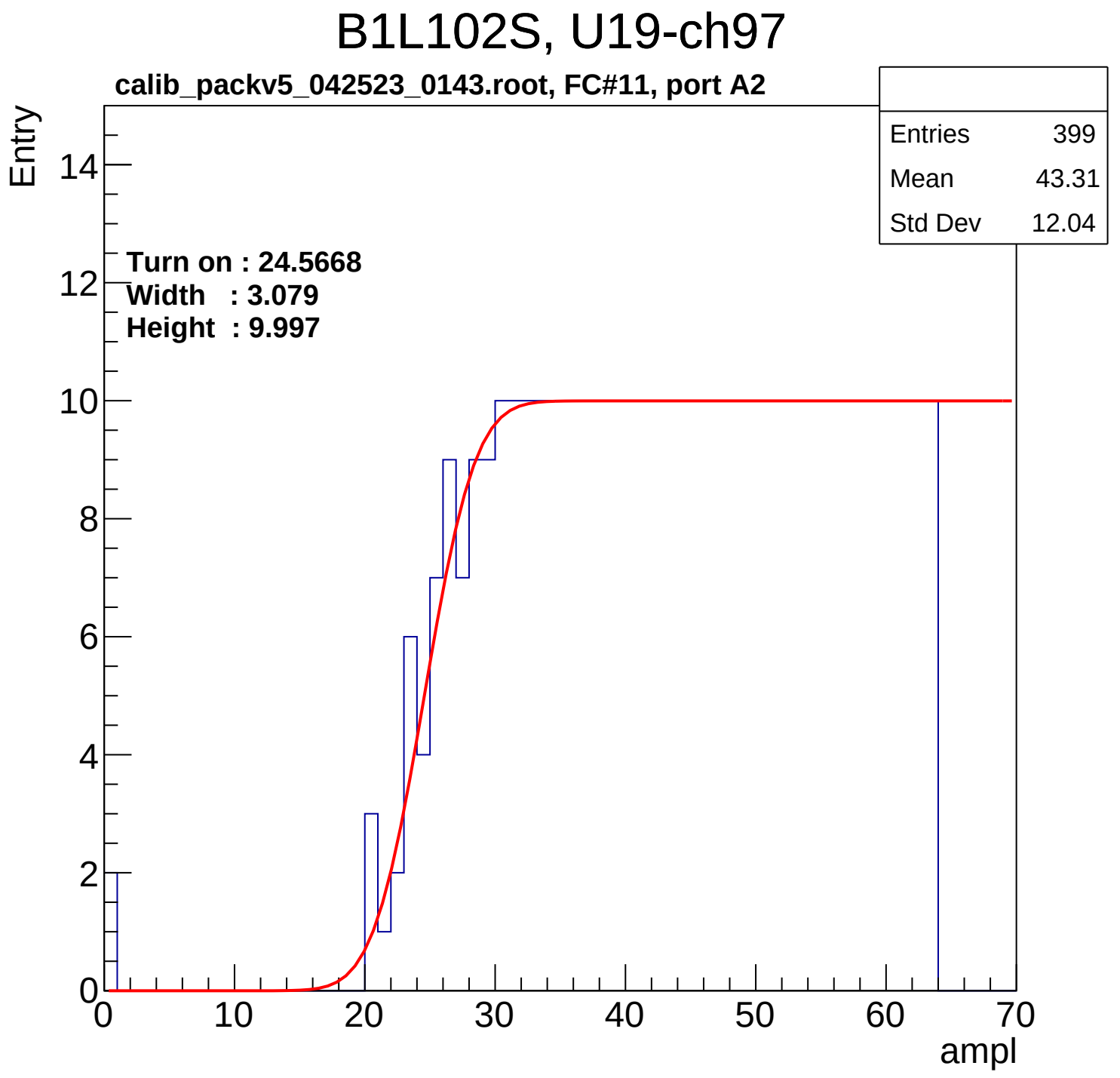

B1L102S, U19-ch92
calib_packv5_042523_0143.root, FC#11, port A2
Entries 404
Mean 42.87
Std Dev 12.63
Turn on : 24.8141
Width : 3.290
Height : 10.024
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

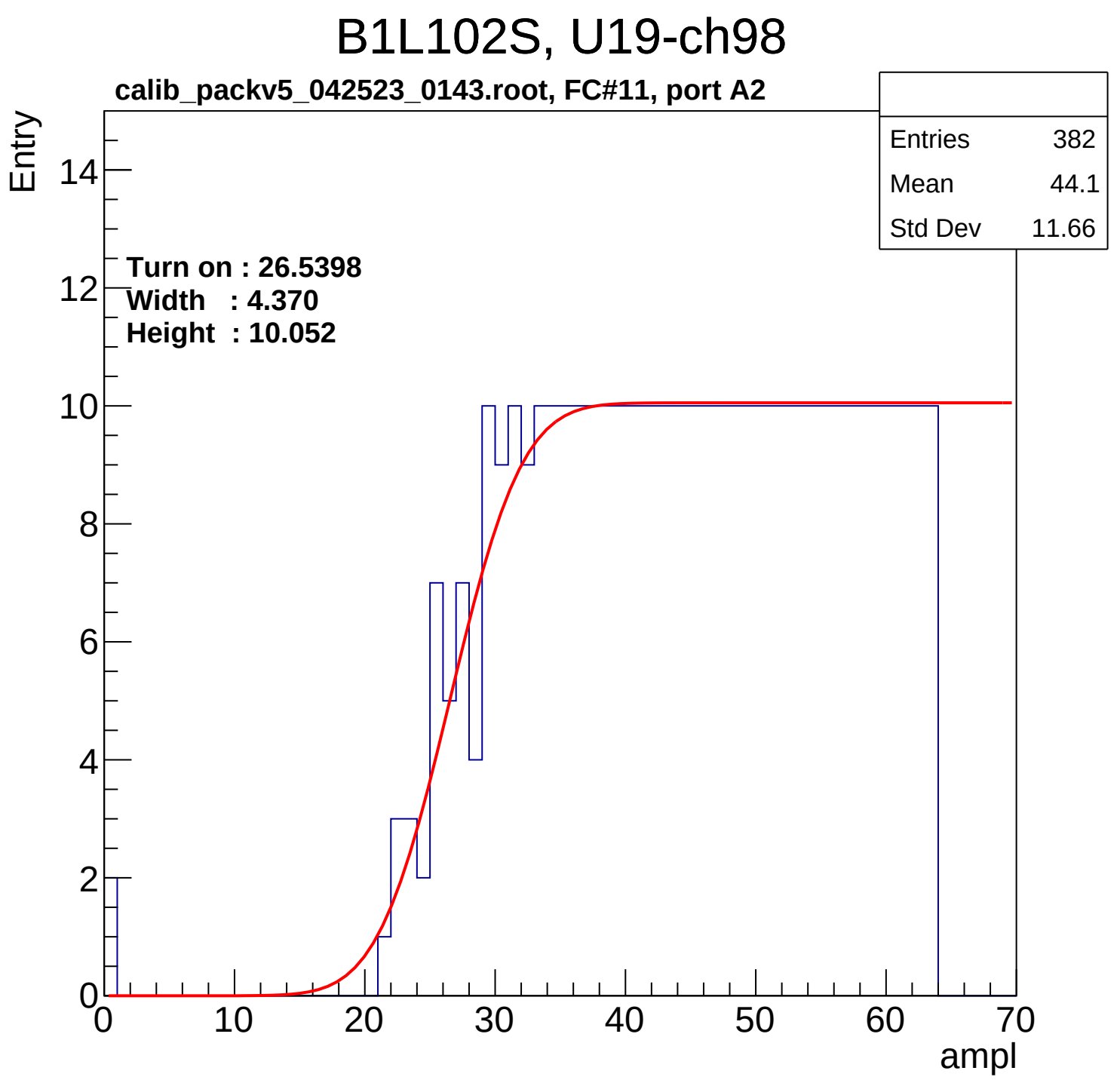

B1L102S, U19-ch93
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.92
Std Dev 11.57
Turn on : 25.7891
Width : 2.880
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

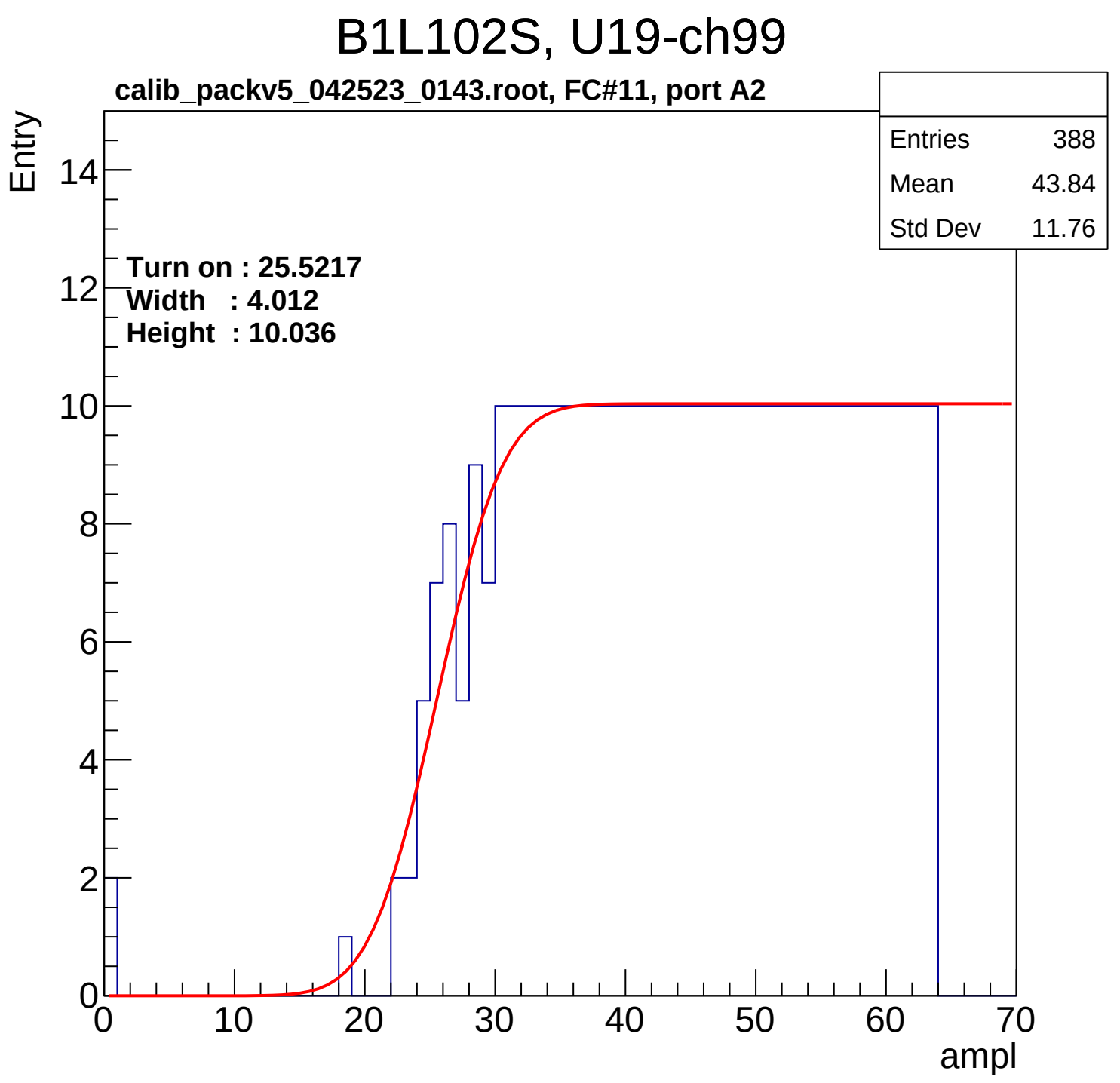

B1L102S, U19-ch94
calib_packv5_042523_0143.root, FC#11, port A2
Entries 391
Mean 43.74
Std Dev 11.76
Turn on : 25.5563
Width : 2.249
Height : 10.018
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

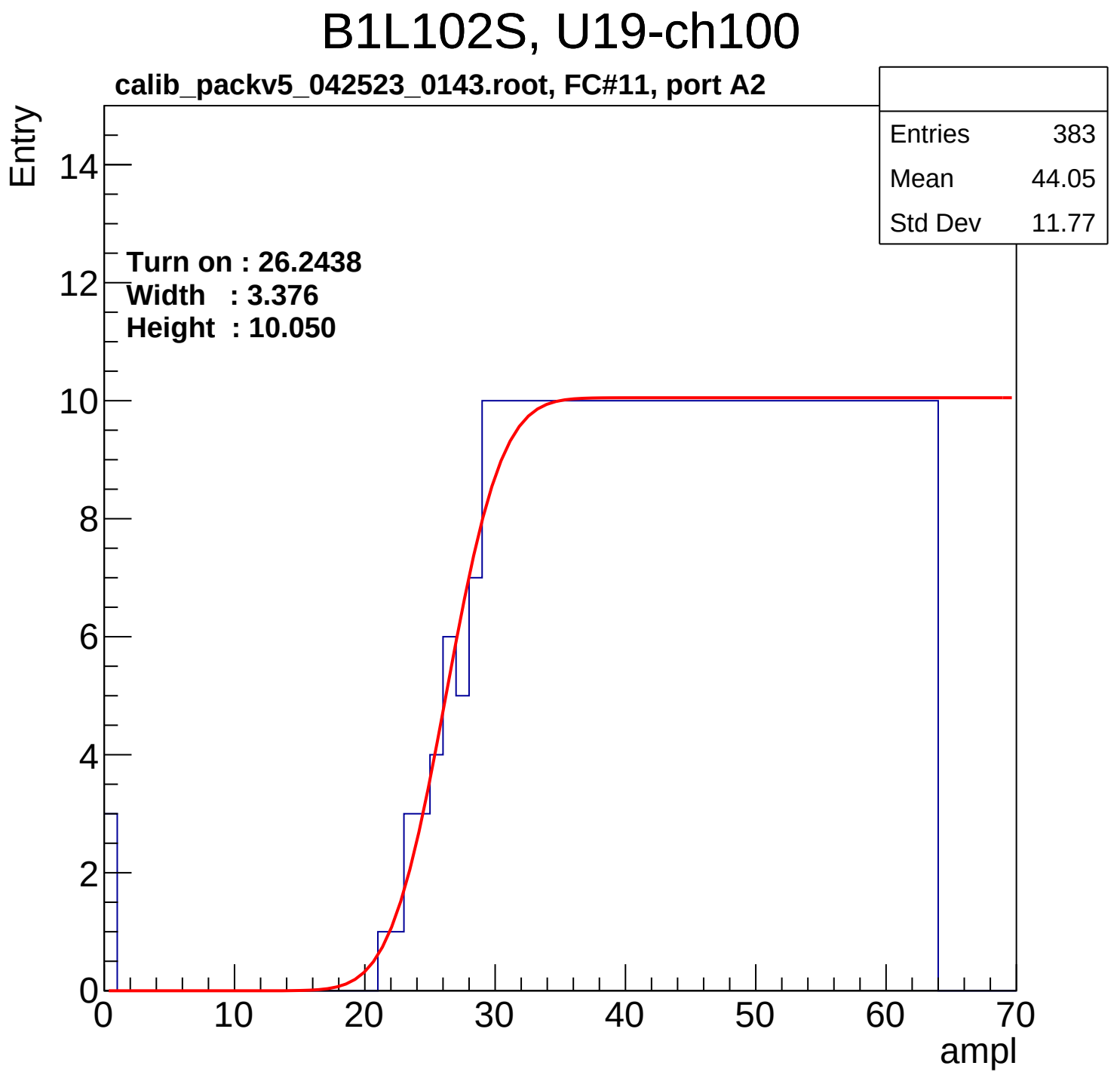

B1L102S, U19-ch95
calib_packv5_042523_0143.root, FC#11, port A2
Entries 406
Mean 42.94
Std Dev 12.43
Turn on : 24.3867
Width : 2.599
Height : 10.037
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

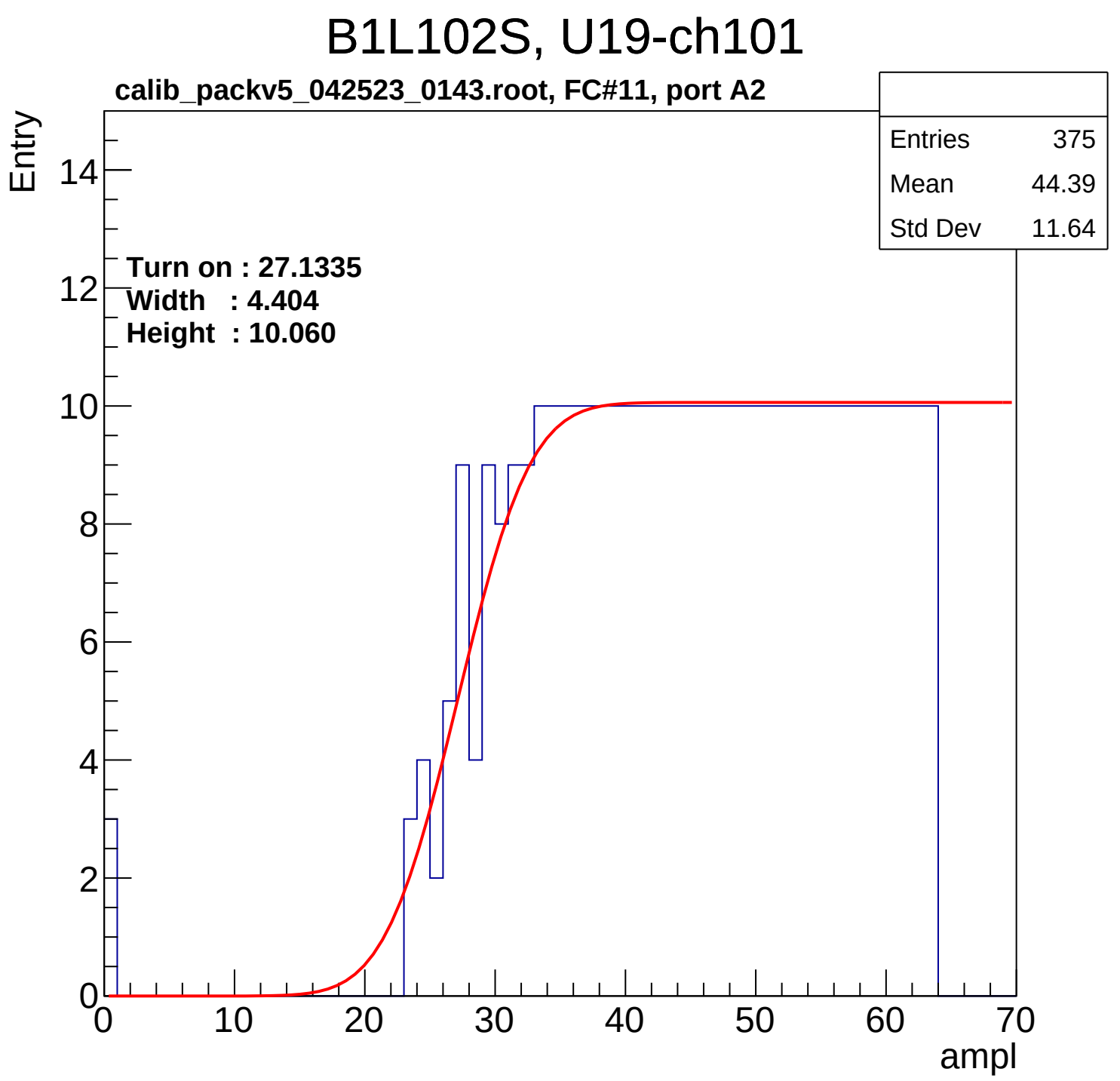

B1L102S, U19-ch96
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44
Std Dev 11.85
Turn on : 26.3442
Width : 3.221
Height : 9.988
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

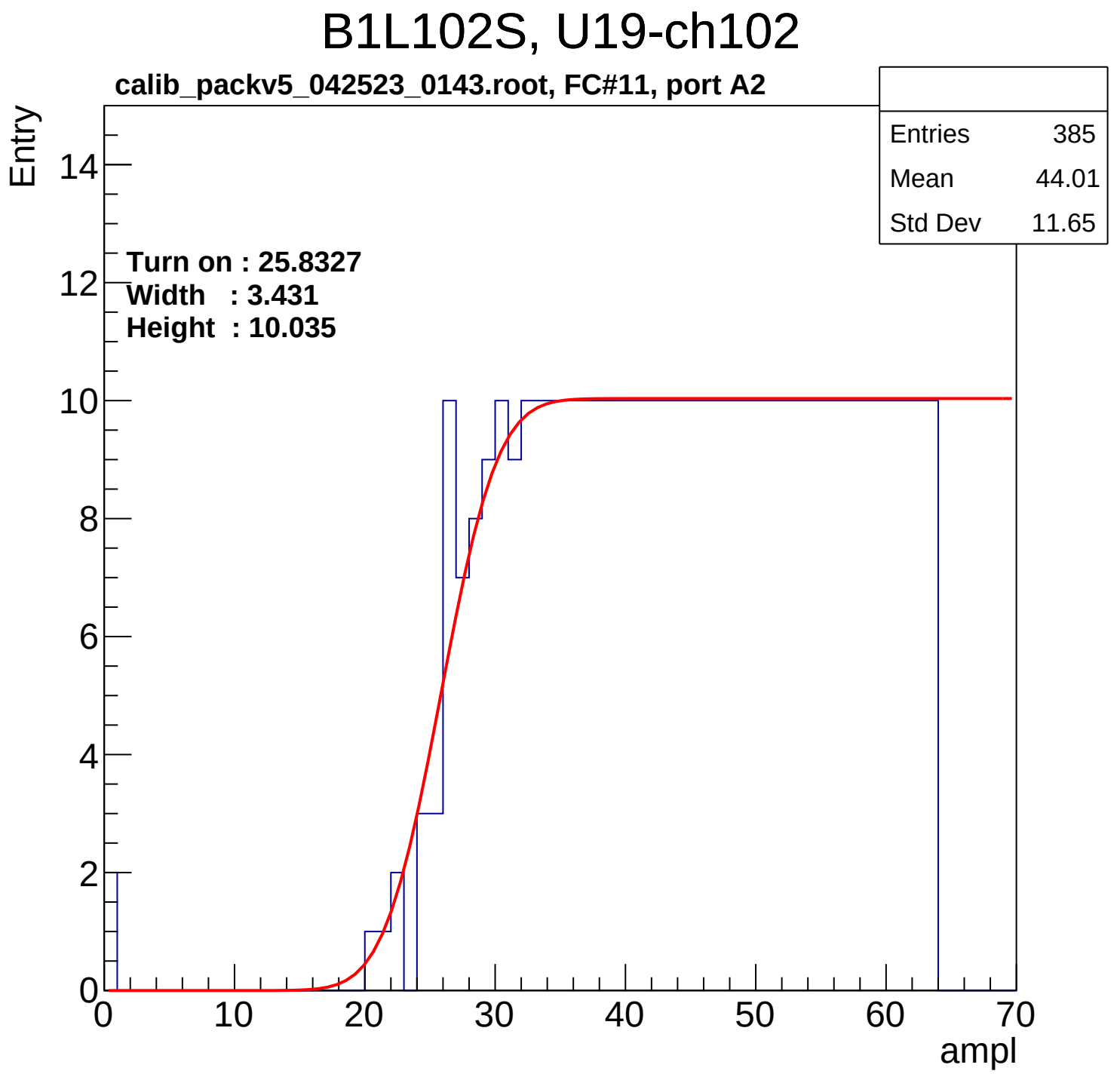

B1L102S, U19-ch97
calib_packv5_042523_0143.root, FC#11, port A2
Entries 399
Mean 43.31
Std Dev 12.04
Turn on : 24.5668
Width : 3.079
Height : 9.997
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

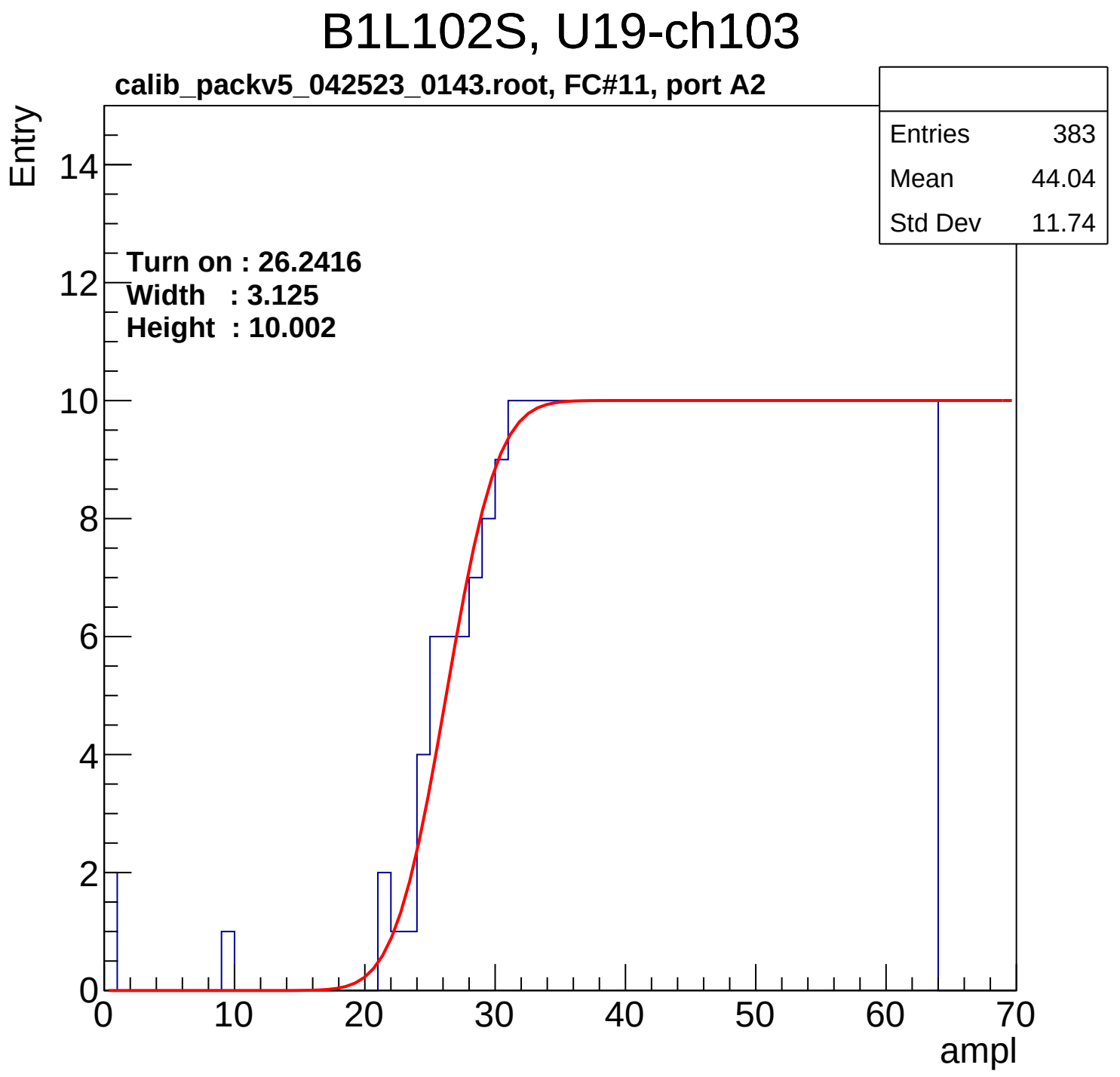

B1L102S, U19-ch98
calib_packv5_042523_0143.root, FC#11, port A2
Entries 382
Mean 44.1
Std Dev 11.66
Turn on : 26.5398
Width : 4.370
Height : 10.052
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

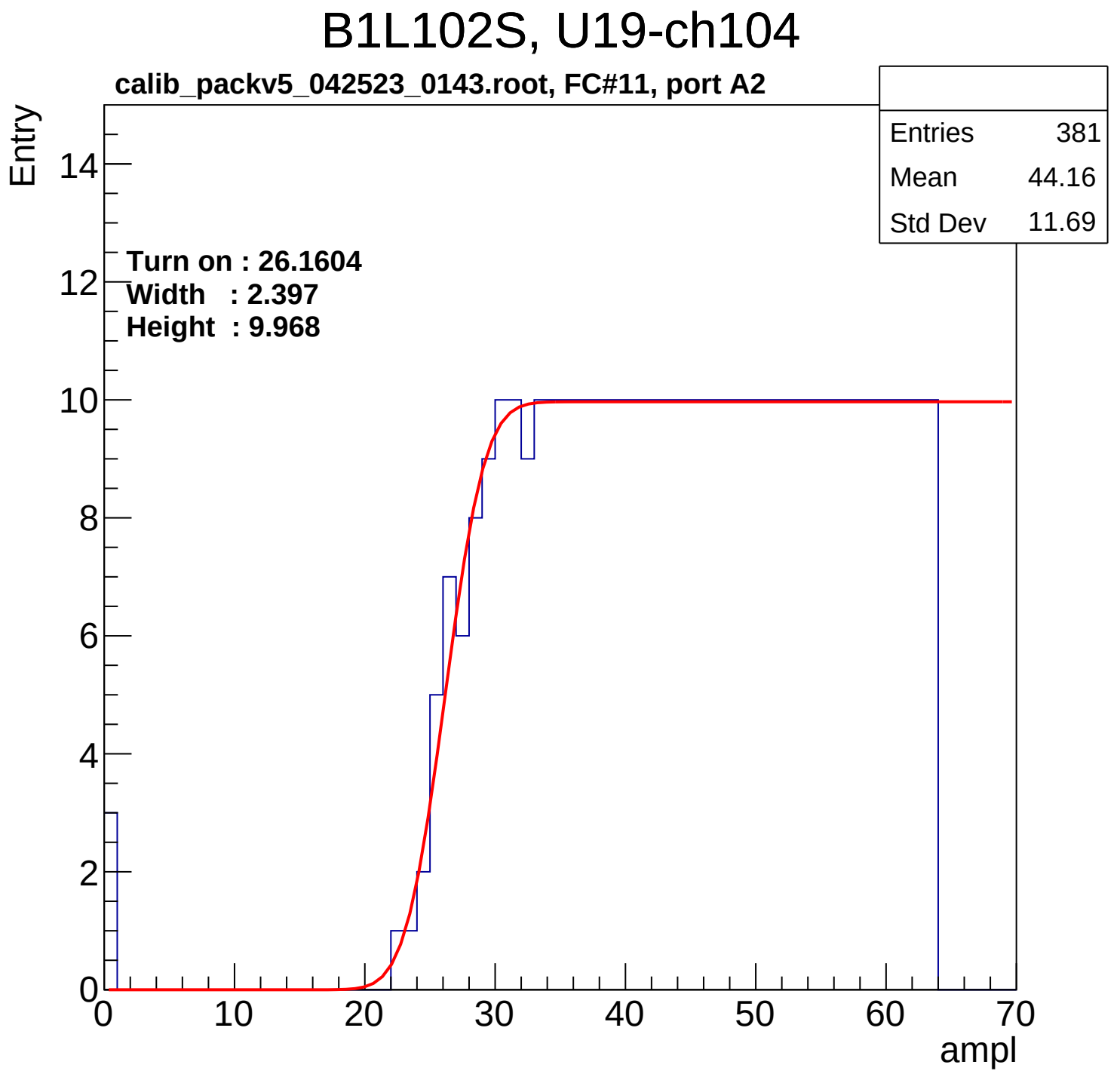

B1L102S, U19-ch99
calib_packv5_042523_0143.root, FC#11, port A2
Entries 388
Mean 43.84
Std Dev 11.76
Turn on : 25.5217
Width : 4.012
Height : 10.036
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

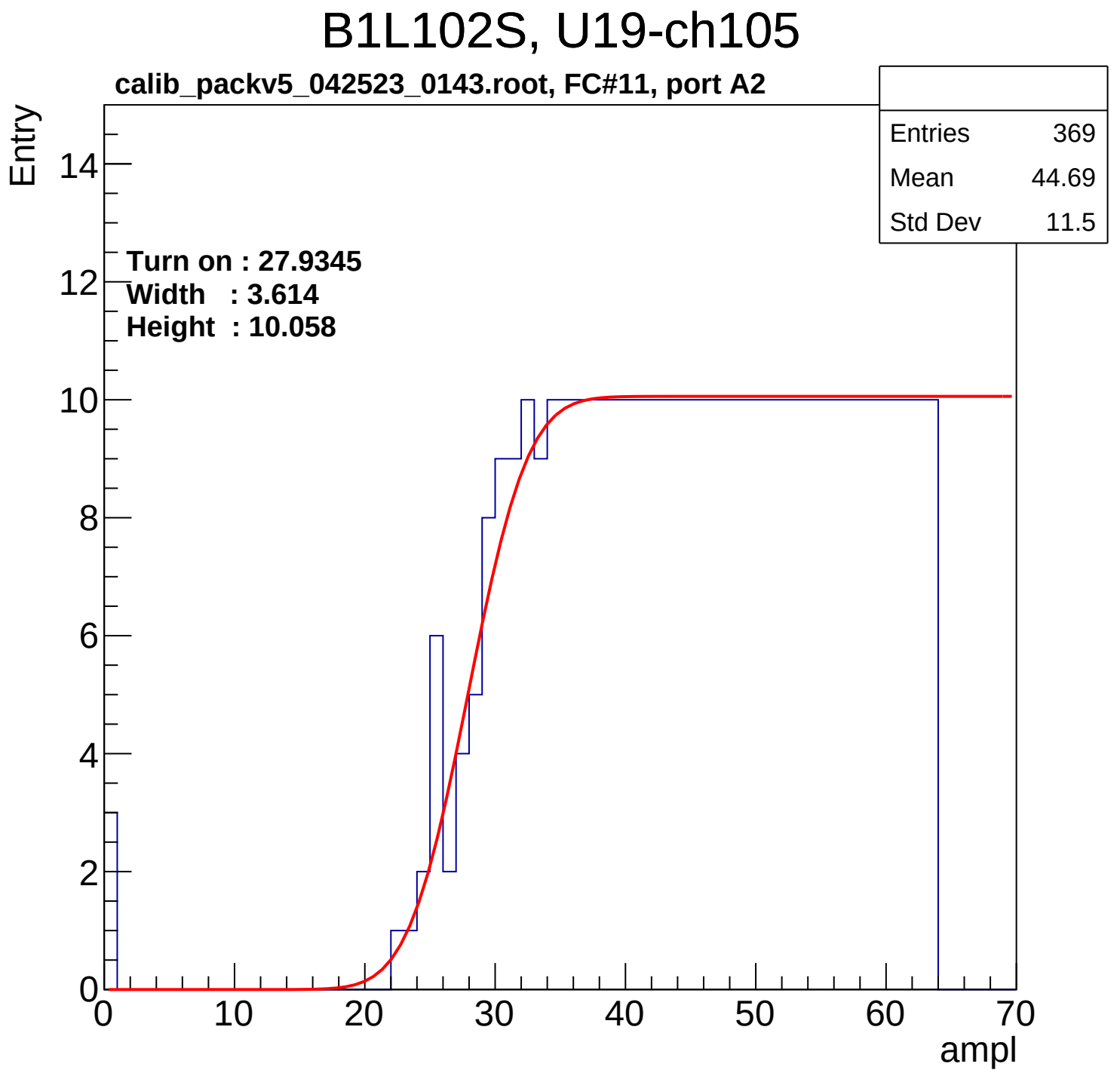

B1L102S, U19-ch100
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.05
Std Dev 11.77
Turn on : 26.2438
Width : 3.376
Height : 10.050
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

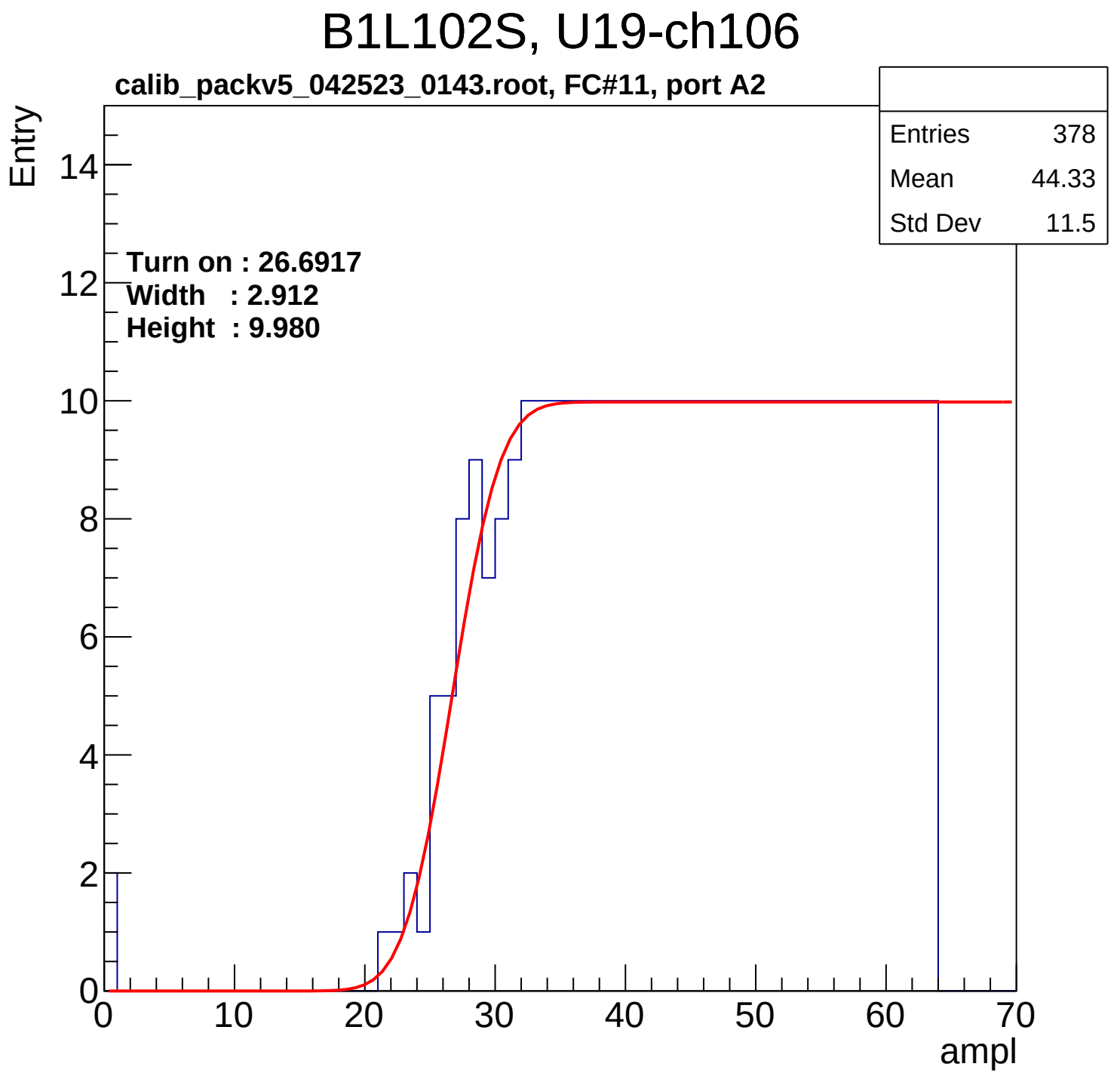

B1L102S, U19-ch101
calib_packv5_042523_0143.root, FC#11, port A2
Entries 375
Mean 44.39
Std Dev 11.64
Turn on : 27.1335
Width : 4.404
Height : 10.060
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

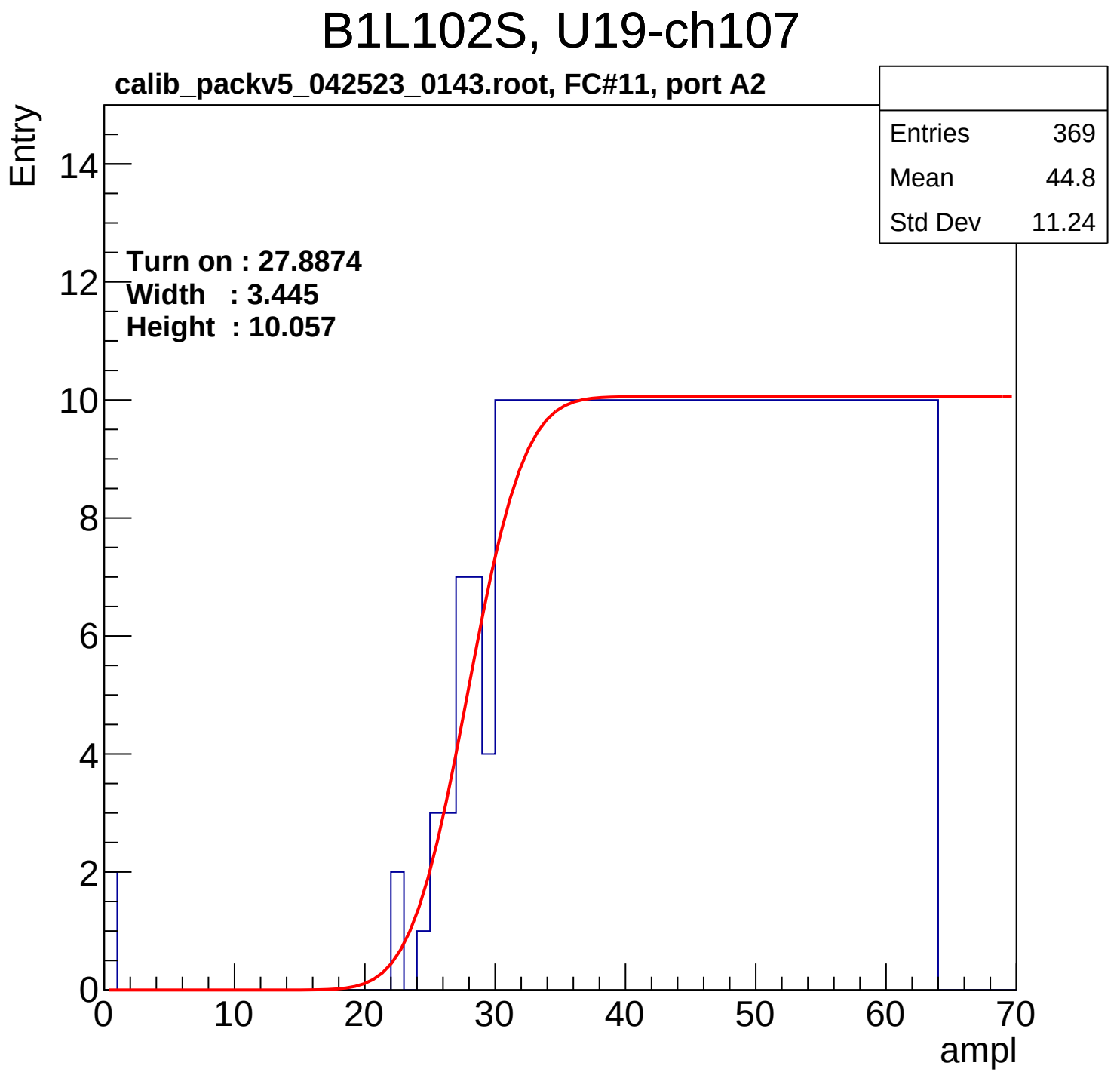

B1L102S, U19-ch102
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 44.01
Std Dev 11.65
Turn on : 25.8327
Width : 3.431
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

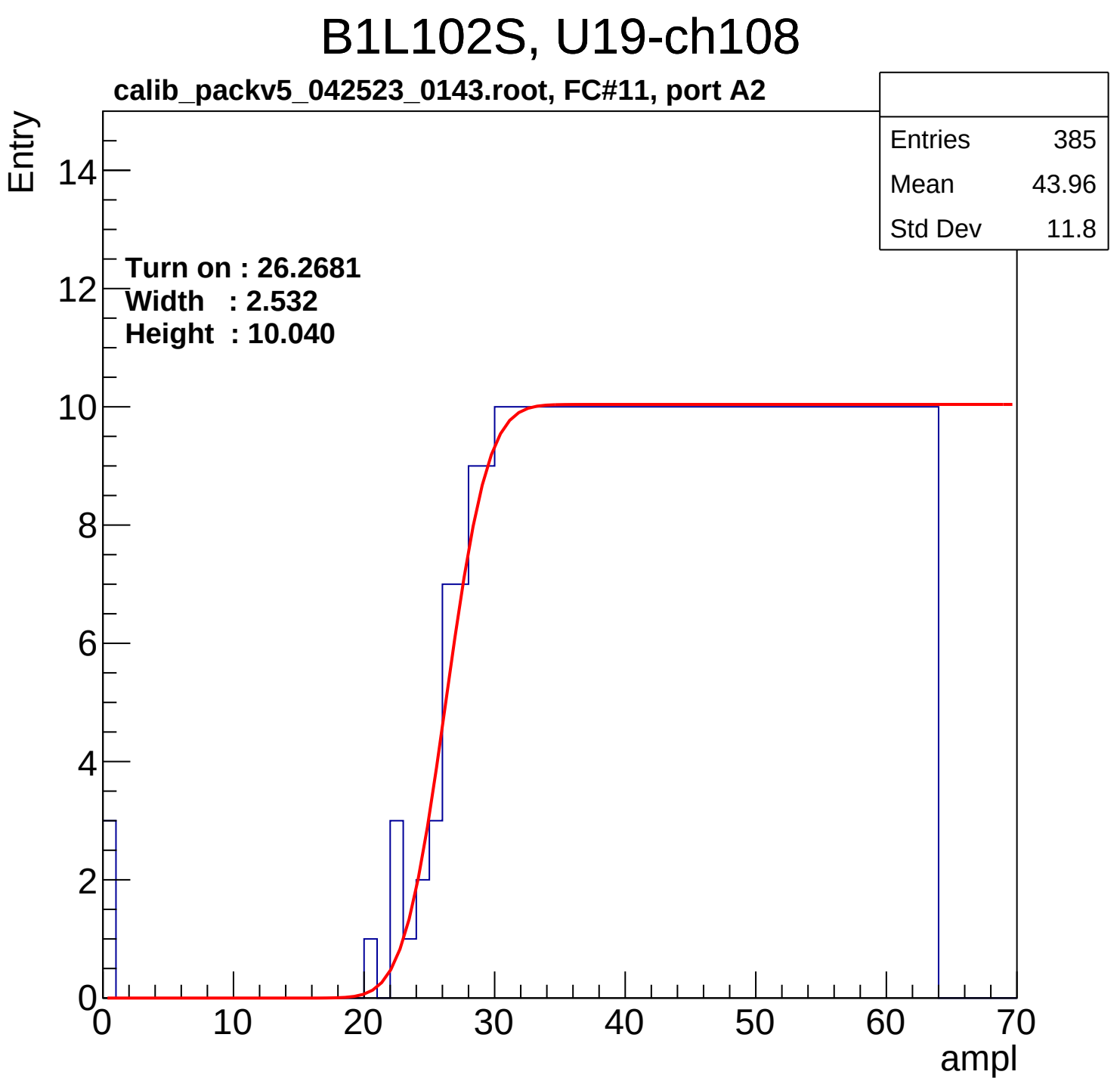

B1L102S, U19-ch103
calib_packv5_042523_0143.root, FC#11, port A2
Entries 383
Mean 44.04
Std Dev 11.74
Turn on : 26.2416
Width : 3.125
Height : 10.002
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

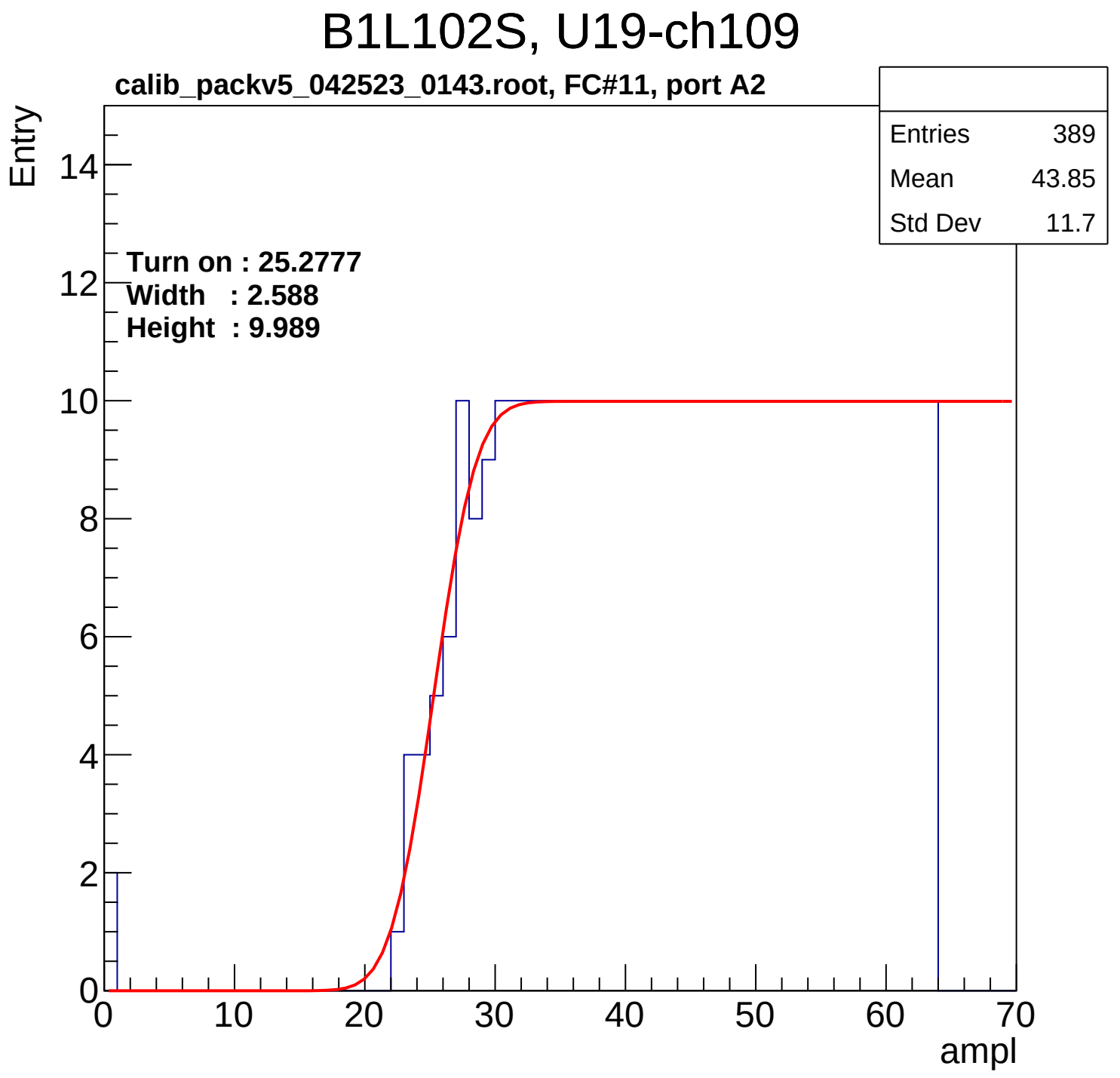

B1L102S, U19-ch104
calib_packv5_042523_0143.root, FC#11, port A2
Entries 381
Mean 44.16
Std Dev 11.69
Turn on : 26.1604
Width : 2.397
Height : 9.968
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

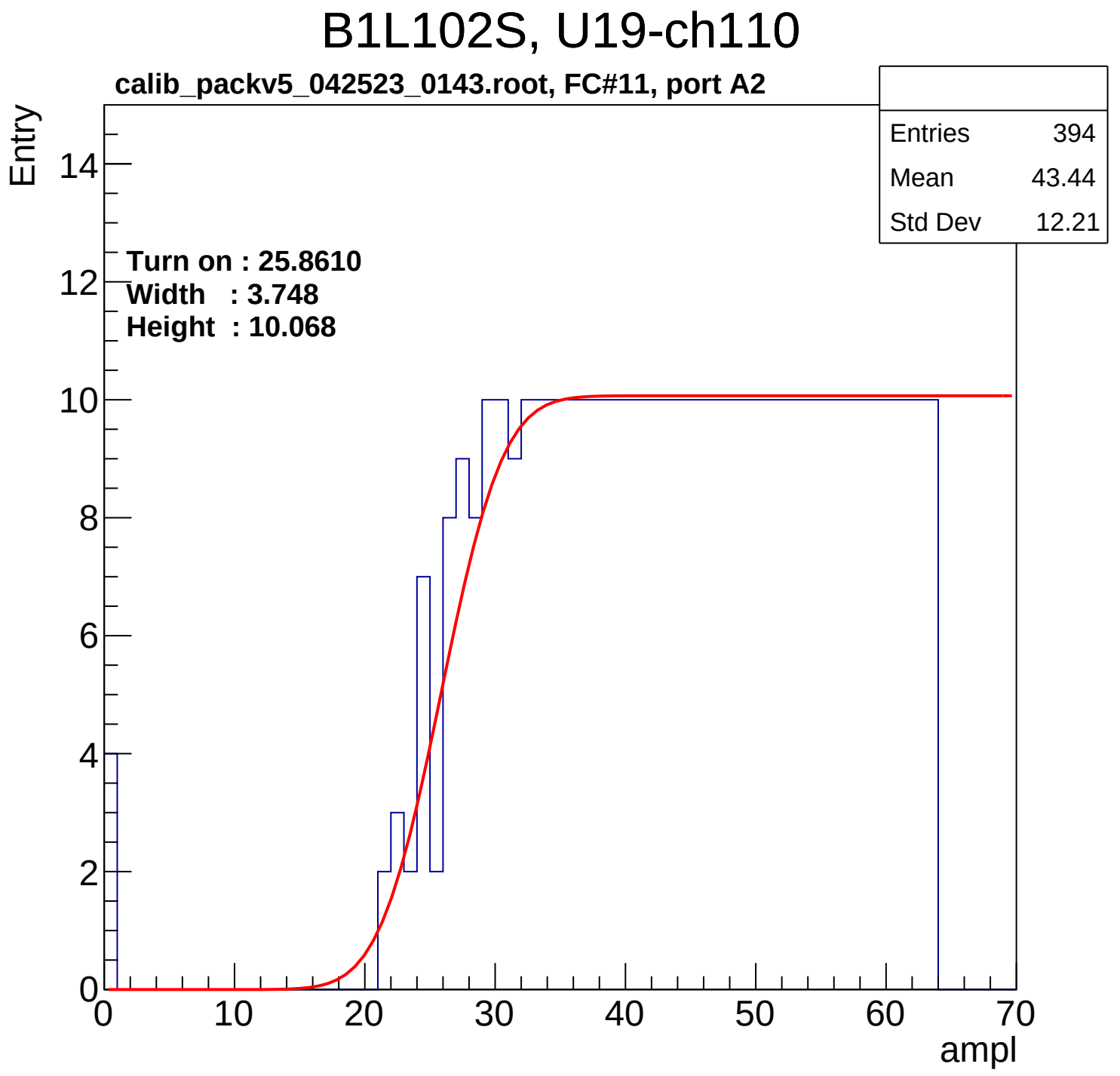

B1L102S, U19-ch105
calib_packv5_042523_0143.root, FC#11, port A2
Entries 369
Mean 44.69
Std Dev 11.5
Turn on : 27.9345
Width : 3.614
Height : 10.058
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

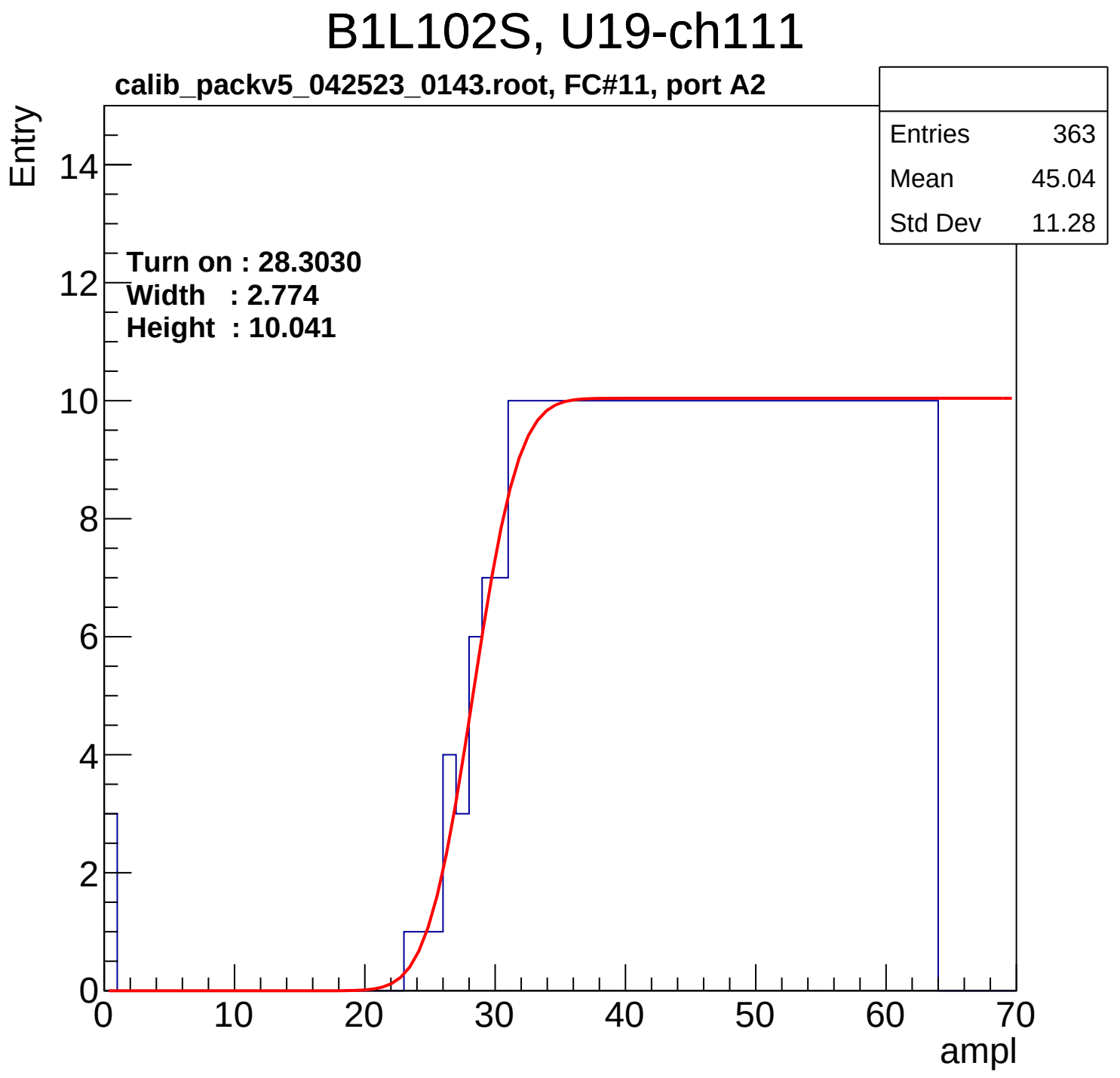

B1L102S, U19-ch106
calib_packv5_042523_0143.root, FC#11, port A2
Entries 378
Mean 44.33
Std Dev 11.5
Turn on : 26.6917
Width : 2.912
Height : 9.980
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

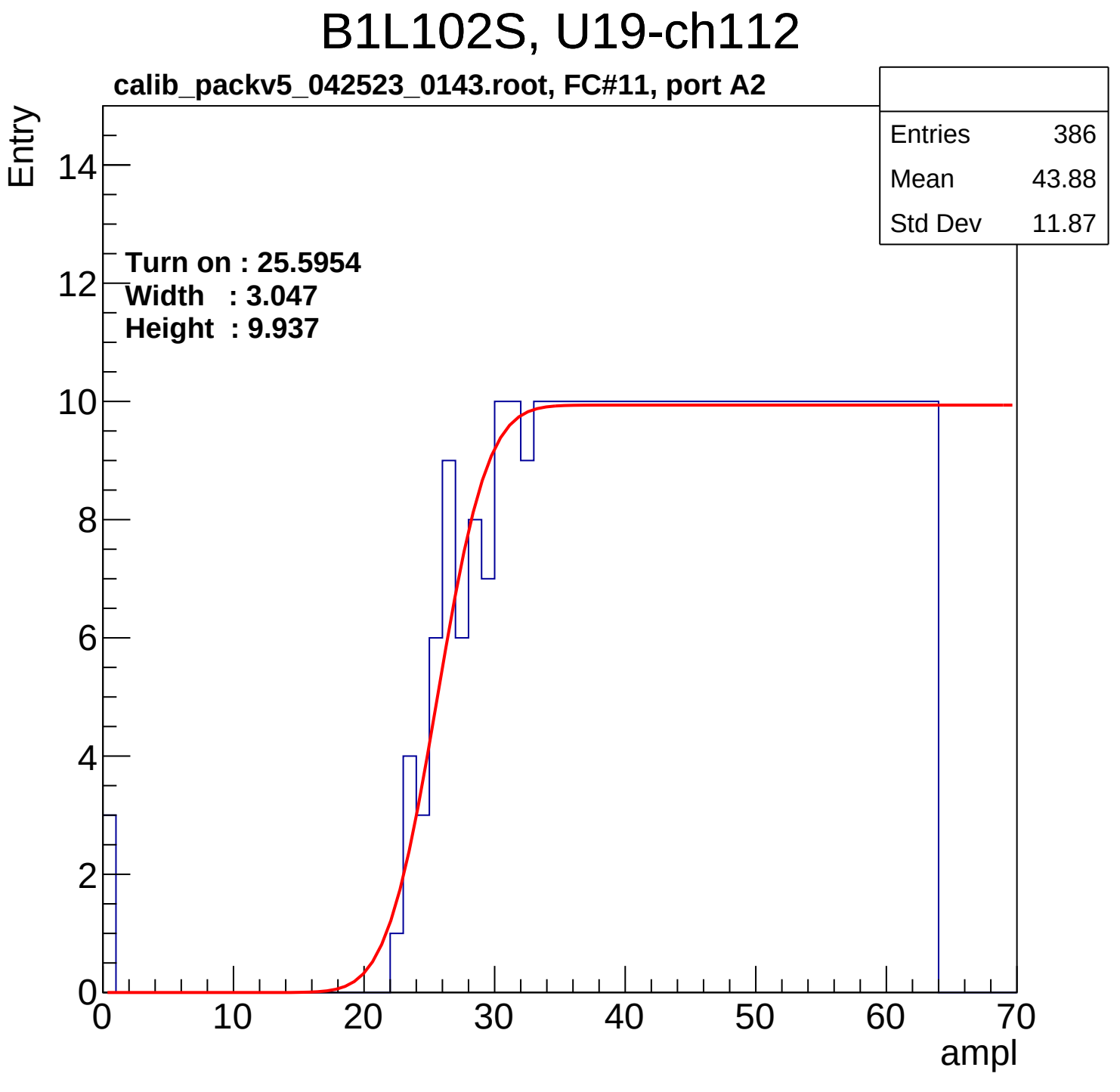

B1L102S, U19-ch107
calib_packv5_042523_0143.root, FC#11, port A2
Entries 369
Mean 44.8
Std Dev 11.24
Turn on : 27.8874
Width : 3.445
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

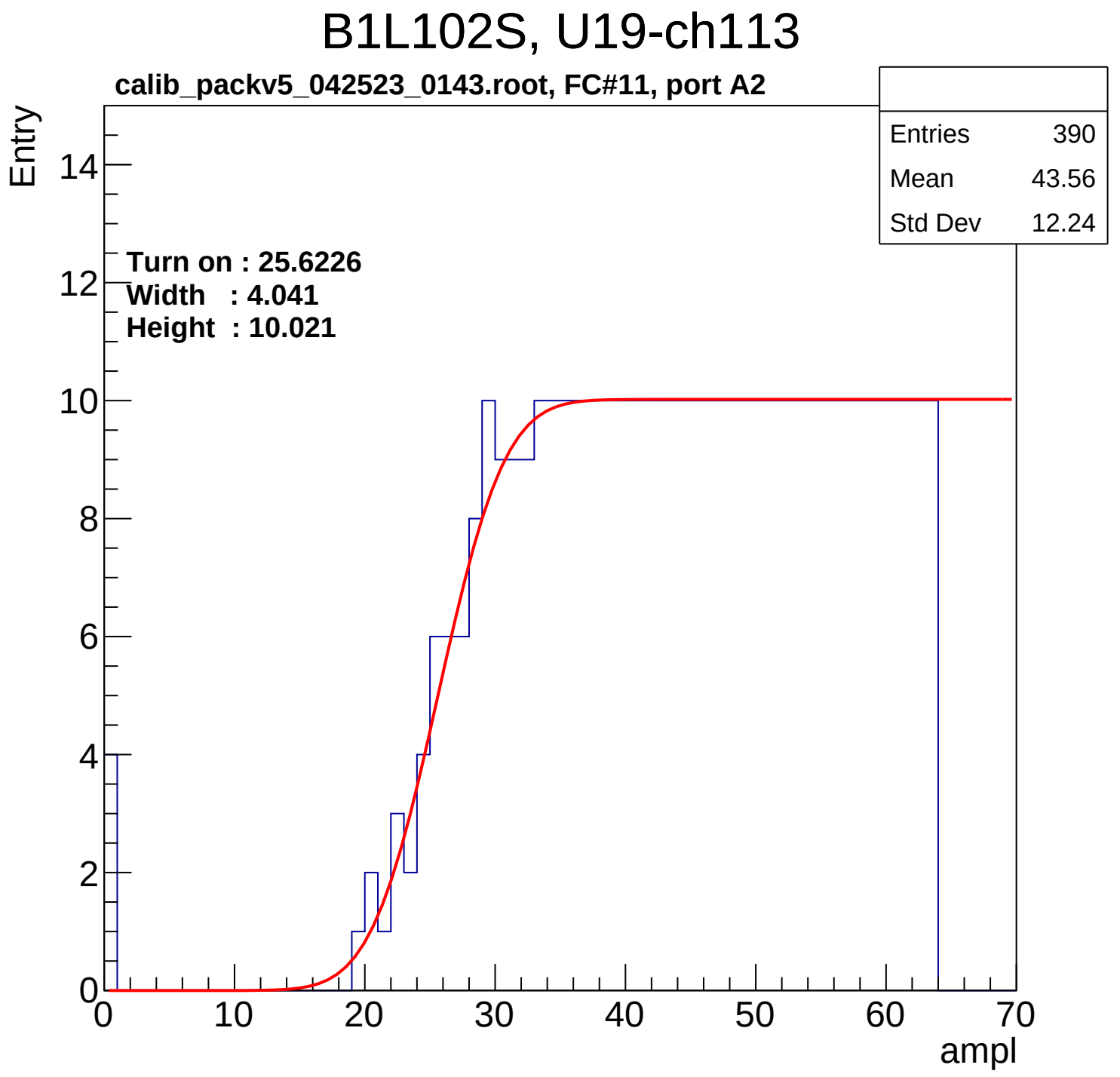

B1L102S, U19-ch108
calib_packv5_042523_0143.root, FC#11, port A2
Entries 385
Mean 43.96
Std Dev 11.8
Turn on : 26.2681
Width : 2.532
Height : 10.040
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

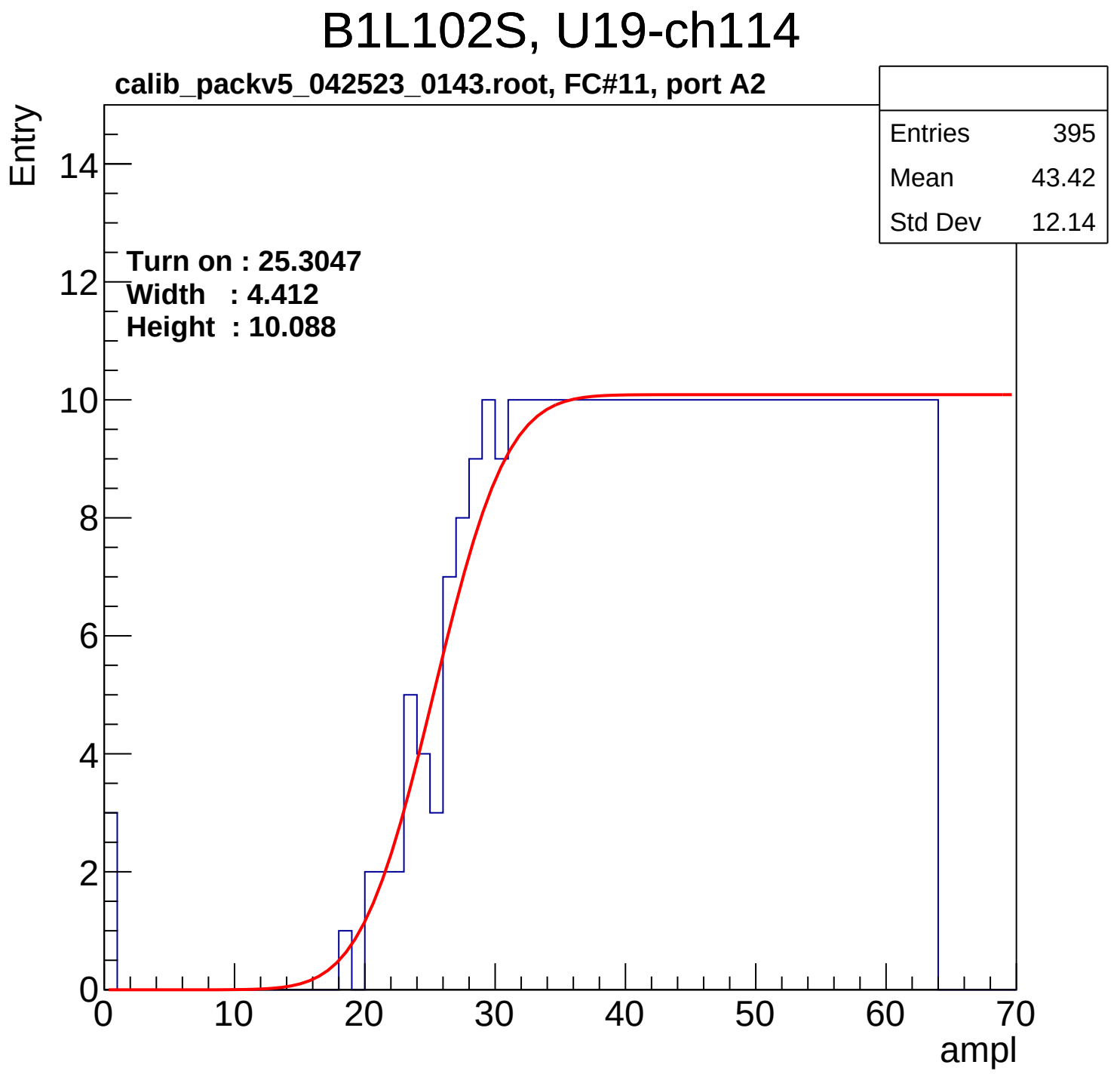

B1L102S, U19-ch109
calib_packv5_042523_0143.root, FC#11, port A2
Entries 389
Mean 43.85
Std Dev 11.7
Turn on : 25.2777
Width : 2.588
Height : 9.989
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

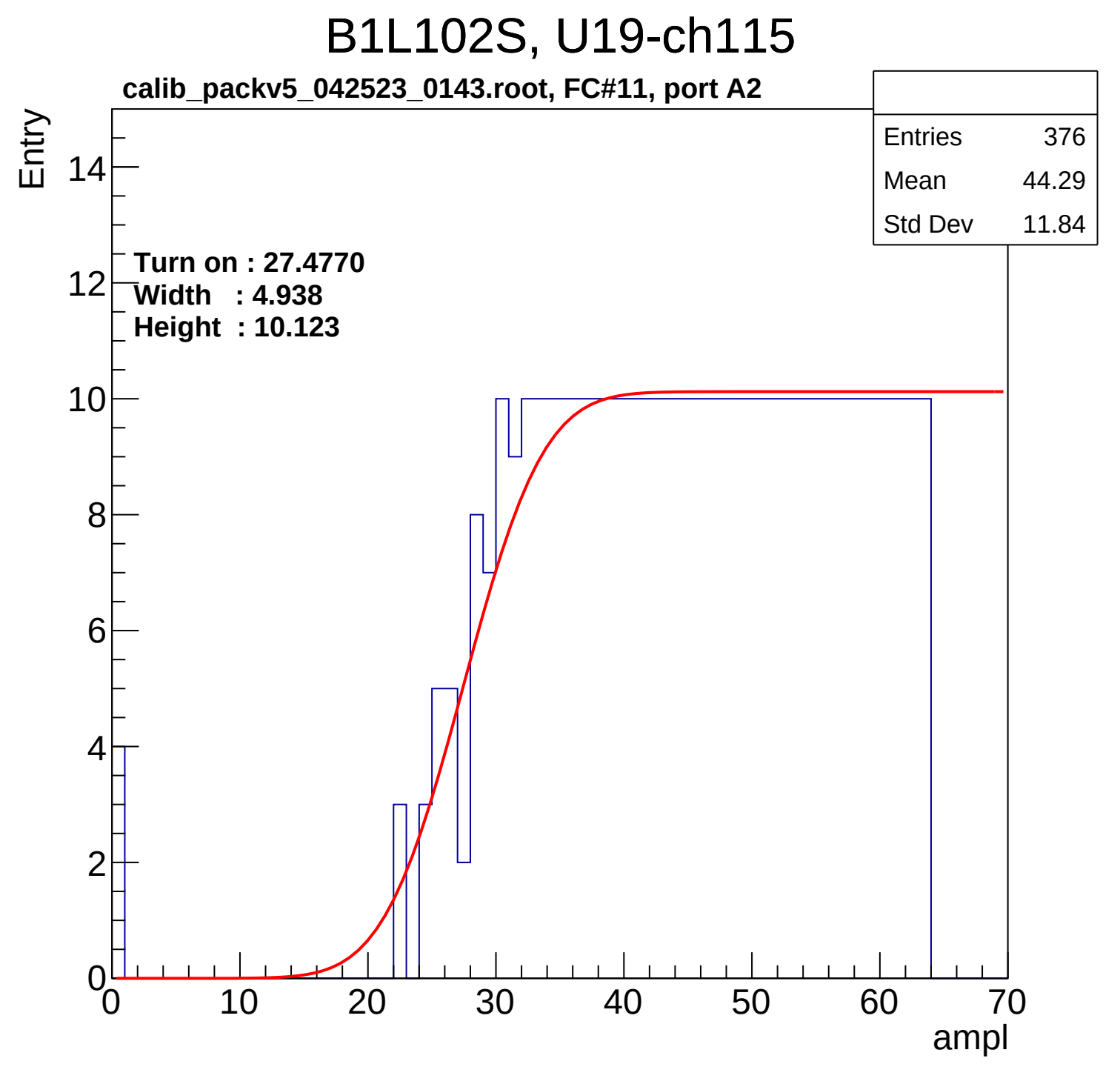

B1L102S, U19-ch110
calib_packv5_042523_0143.root, FC#11, port A2
Entries 394
Mean 43.44
Std Dev 12.21
Turn on : 25.8610
Width : 3.748
Height : 10.068
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

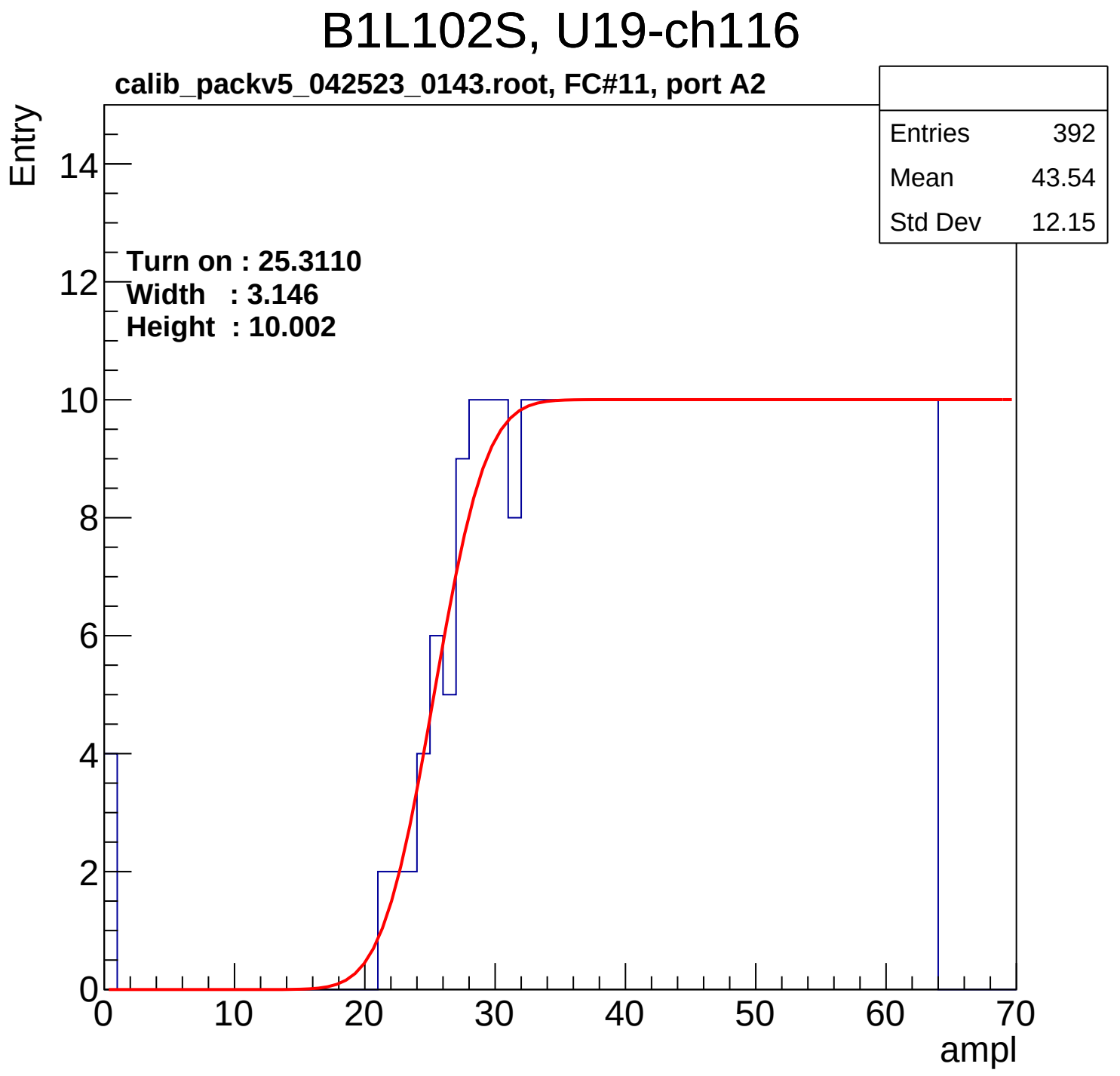

B1L102S, U19-ch111
calib_packv5_042523_0143.root, FC#11, port A2
Entries 363
Mean 45.04
Std Dev 11.28
Turn on : 28.3030
Width : 2.774
Height : 10.041
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

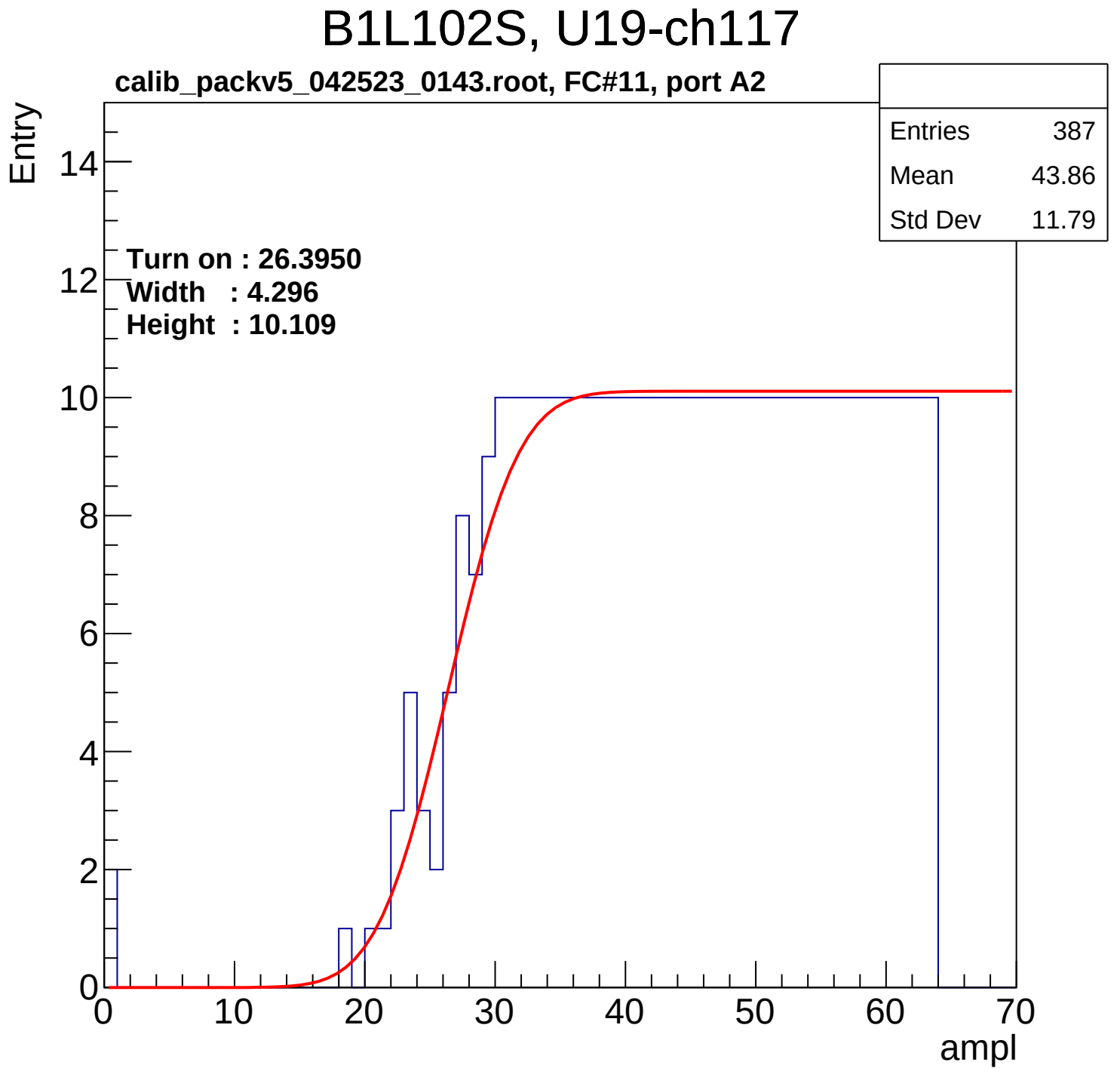

B1L102S, U19-ch112
calib_packv5_042523_0143.root, FC#11, port A2
Entries 386
Mean 43.88
Std Dev 11.87
Turn on : 25.5954
Width : 3.047
Height : 9.937
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

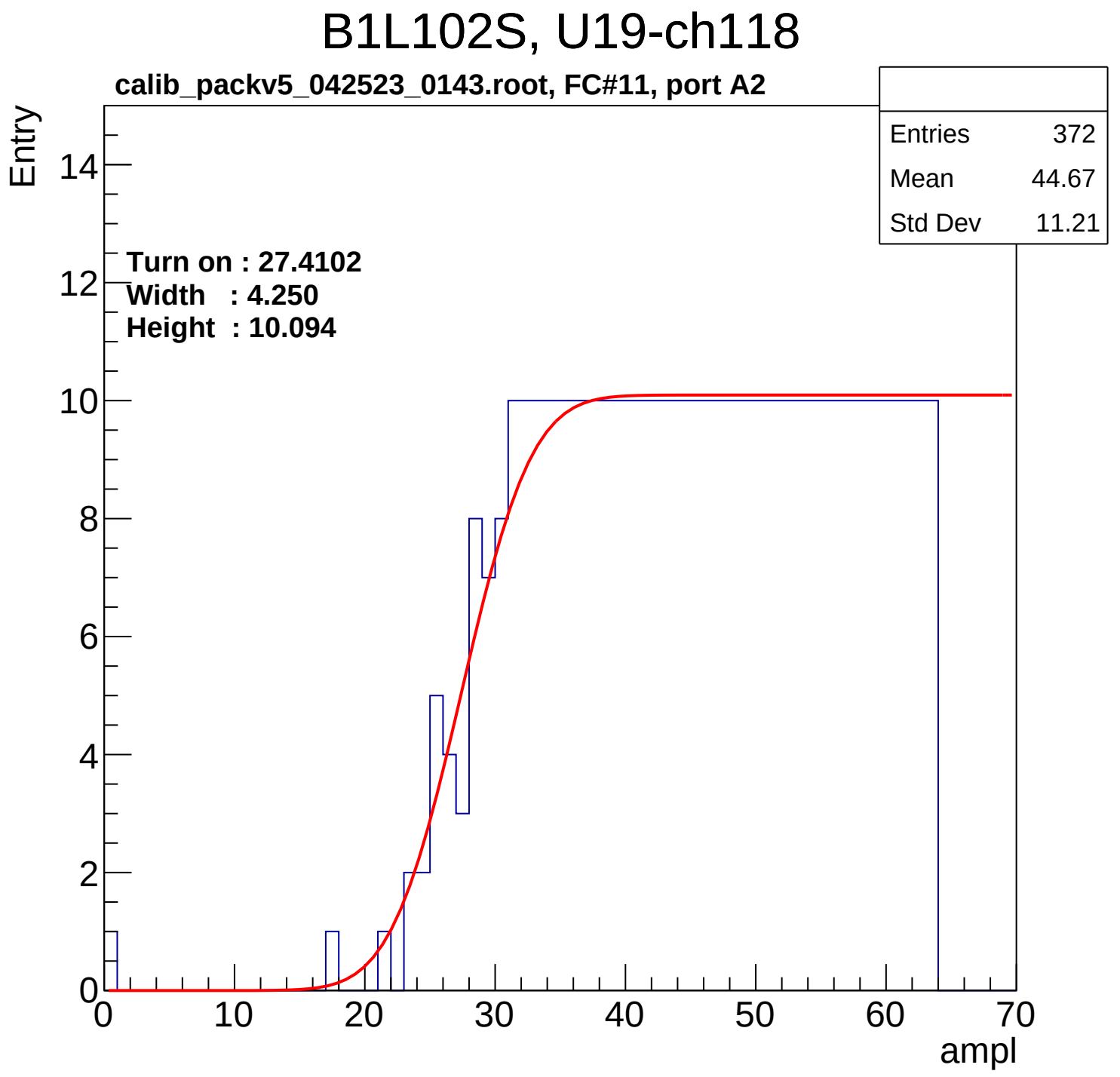

B1L102S, U19-ch113
calib_packv5_042523_0143.root, FC#11, port A2
Entries 390
Mean 43.56
Std Dev 12.24
Turn on : 25.6226
Width : 4.041
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

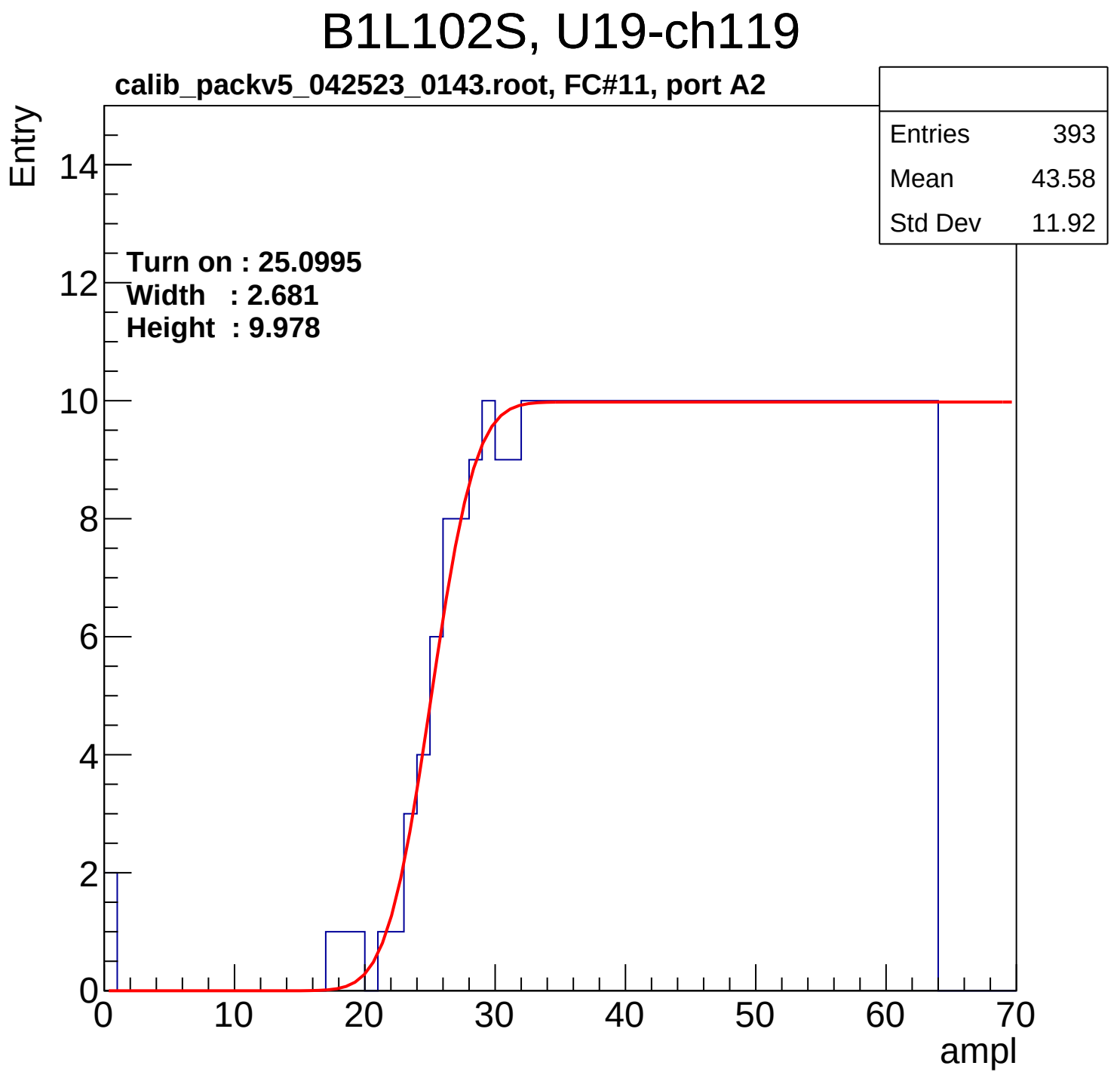

B1L102S, U19-ch114
calib_packv5_042523_0143.root, FC#11, port A2
Entries 395
Mean 43.42
Std Dev 12.14
Turn on : 25.3047
Width : 4.412
Height : 10.088
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

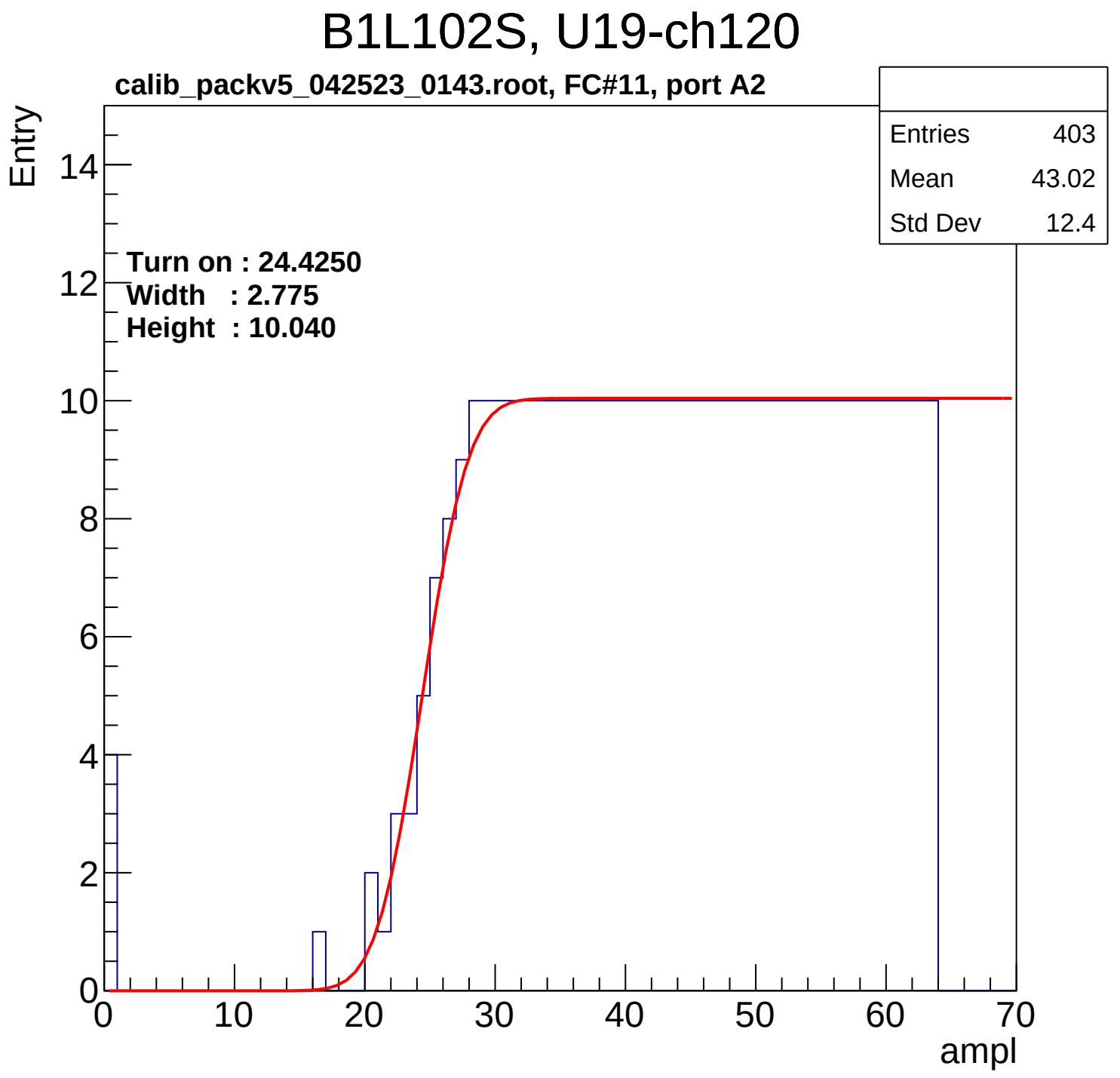

B1L102S, U19-ch115
calib_packv5_042523_0143.root, FC#11, port A2
Entries 376
Mean 44.29
Std Dev 11.84
Turn on : 27.4770
Width : 4.938
Height : 10.123
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

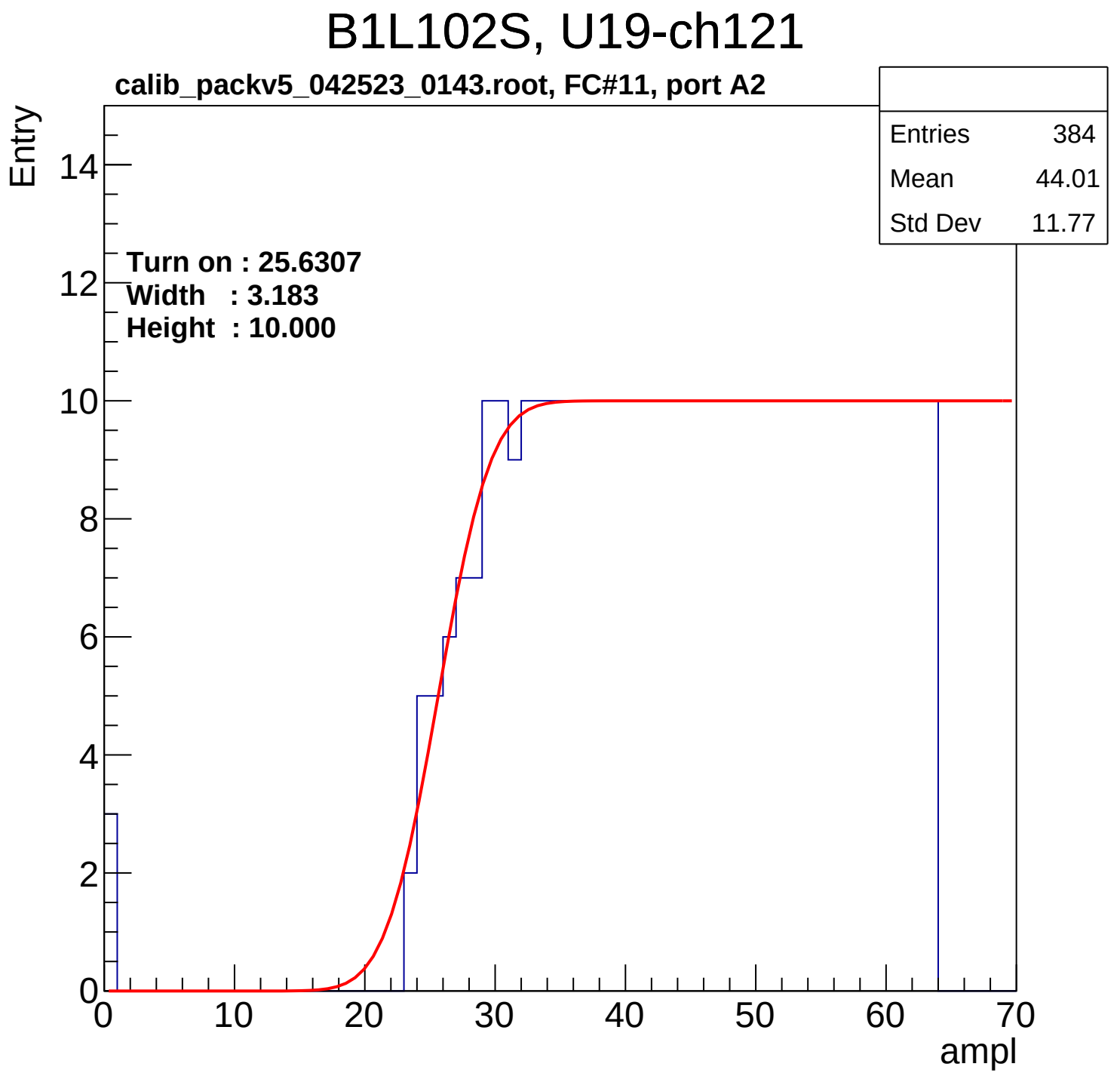

B1L102S, U19-ch116
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.54
Std Dev 12.15
Turn on : 25.3110
Width : 3.146
Height : 10.002
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

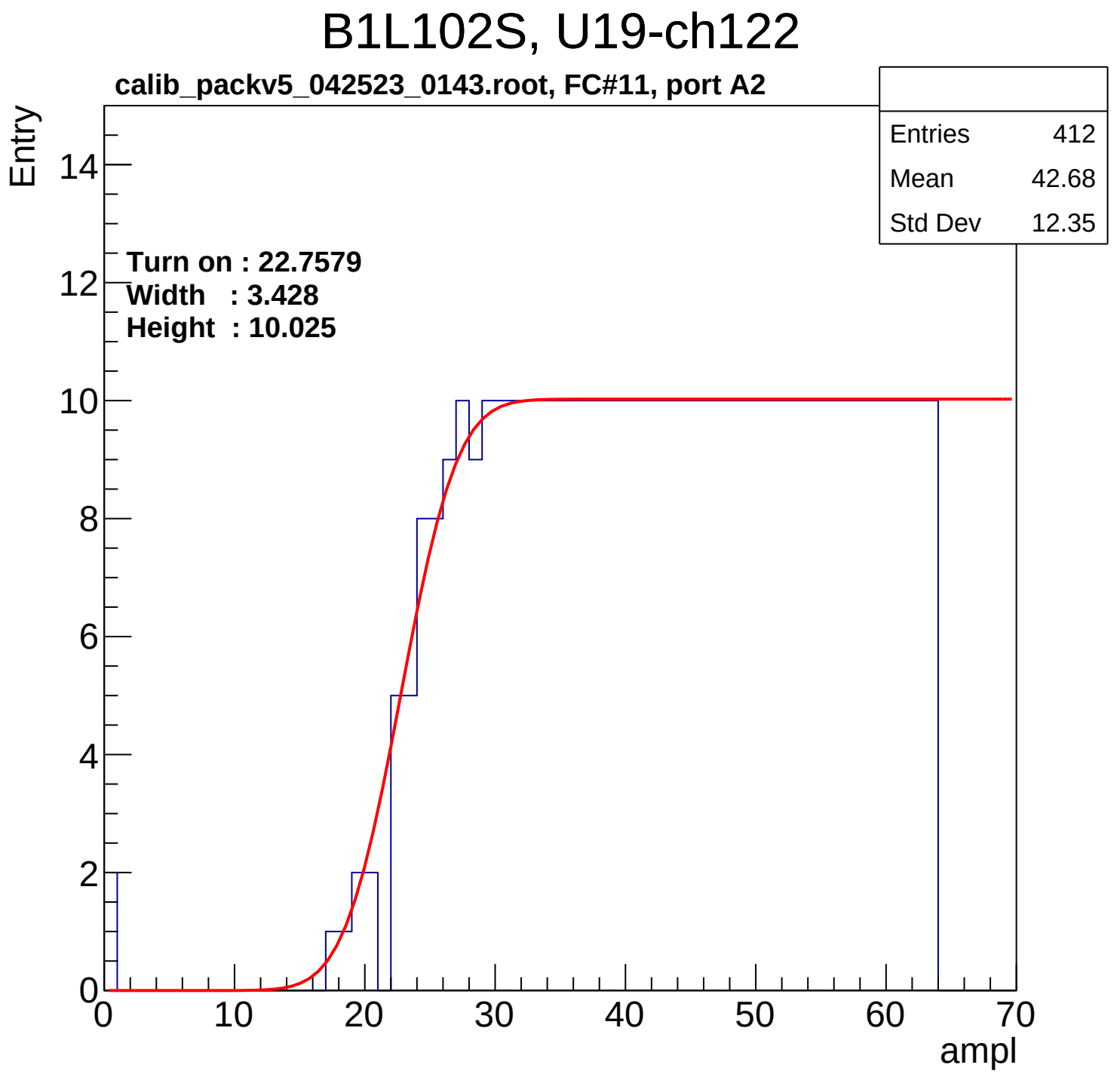

B1L102S, U19-ch117
calib_packv5_042523_0143.root, FC#11, port A2
Entries 387
Mean 43.86
Std Dev 11.79
Turn on : 26.3950
Width : 4.296
Height : 10.109
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

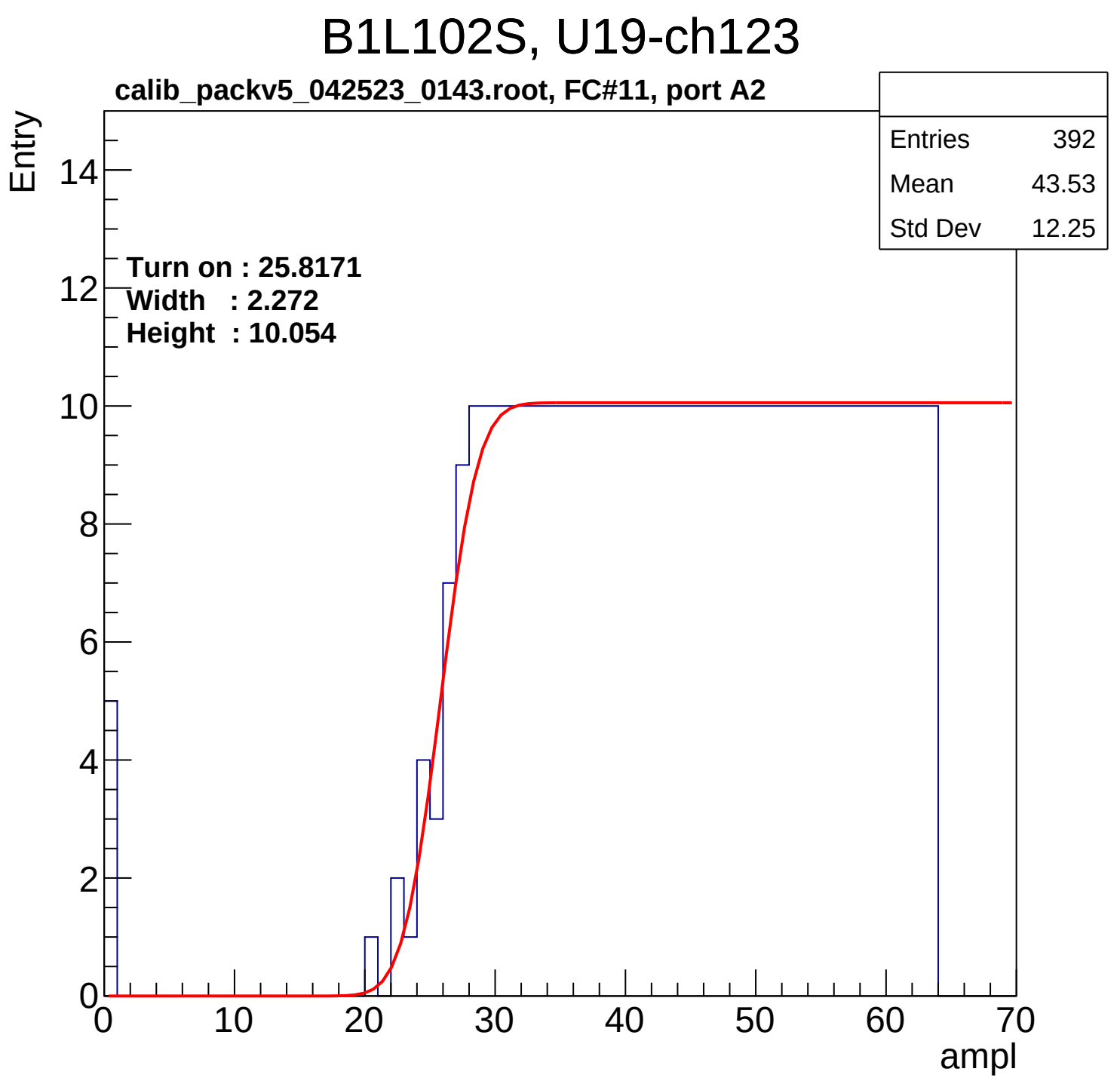

B1L102S, U19-ch118
calib_packv5_042523_0143.root, FC#11, port A2
Entries 372
Mean 44.67
Std Dev 11.21
Turn on : 27.4102
Width : 4.250
Height : 10.094
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

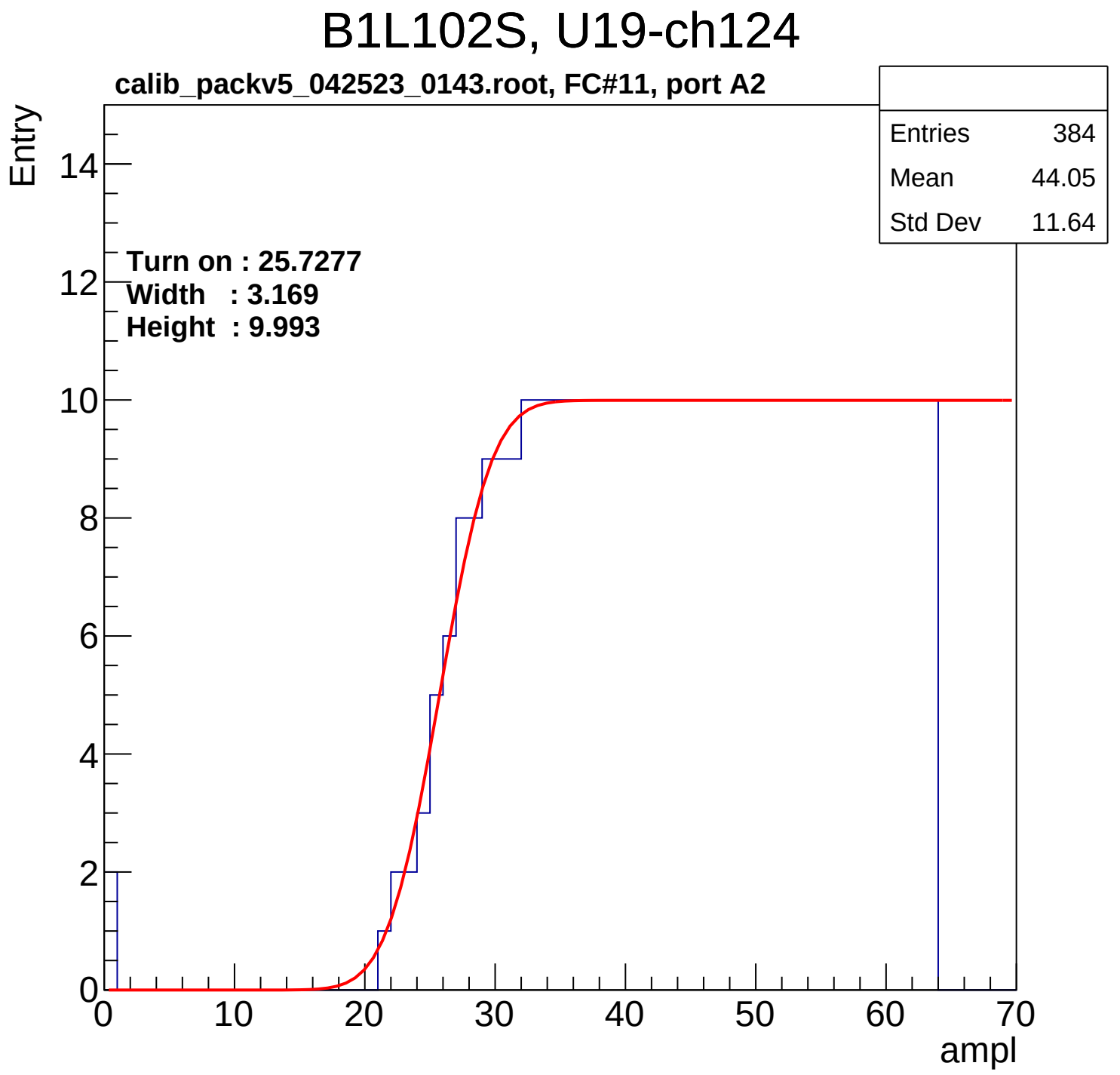

B1L102S, U19-ch119
calib_packv5_042523_0143.root, FC#11, port A2
Entries 393
Mean 43.58
Std Dev 11.92
Turn on : 25.0995
Width : 2.681
Height : 9.978
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

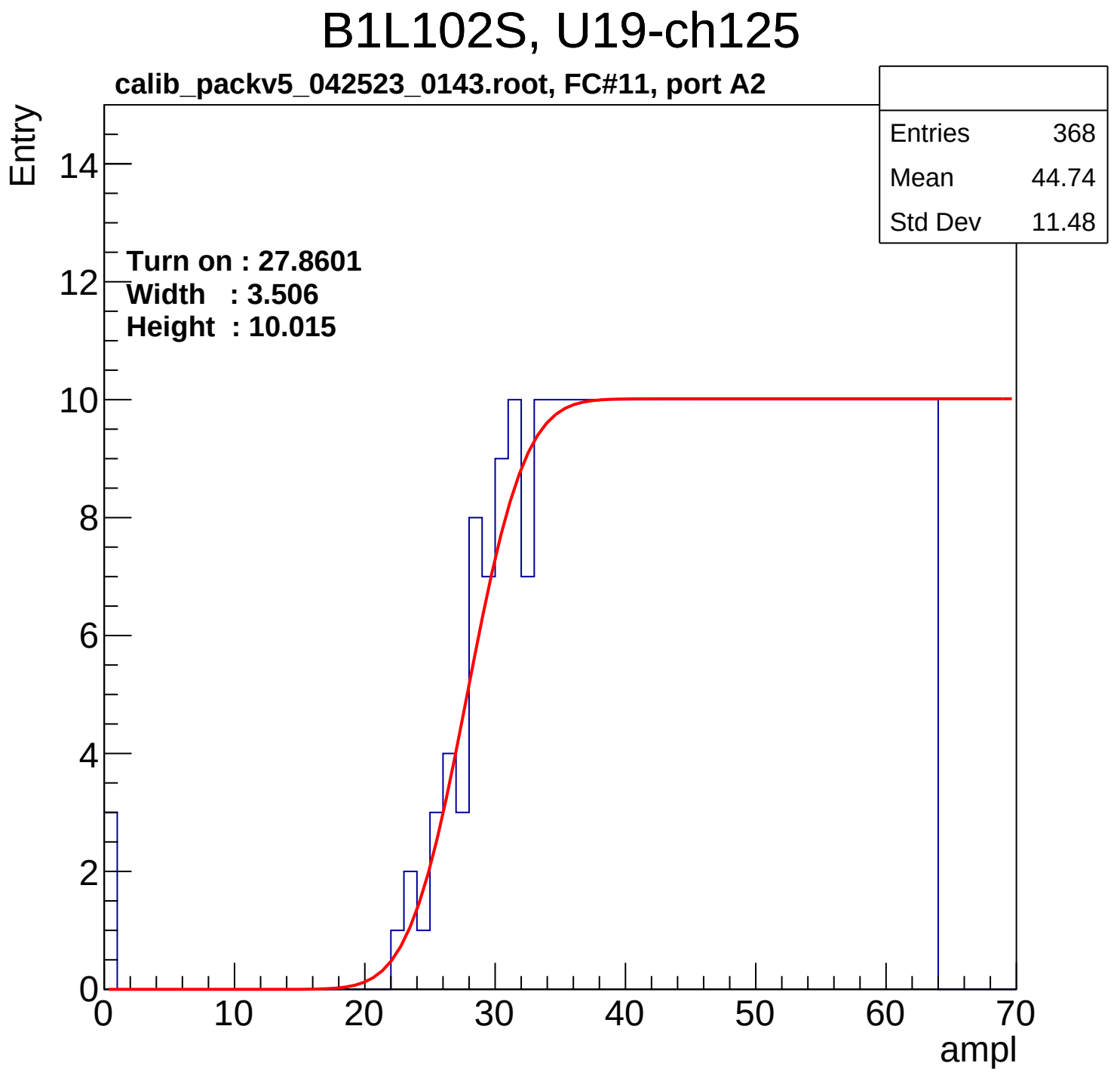

B1L102S, U19-ch120
calib_packv5_042523_0143.root, FC#11, port A2
Entries 403
Mean 43.02
Std Dev 12.4
Turn on : 24.4250
Width : 2.775
Height : 10.040
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

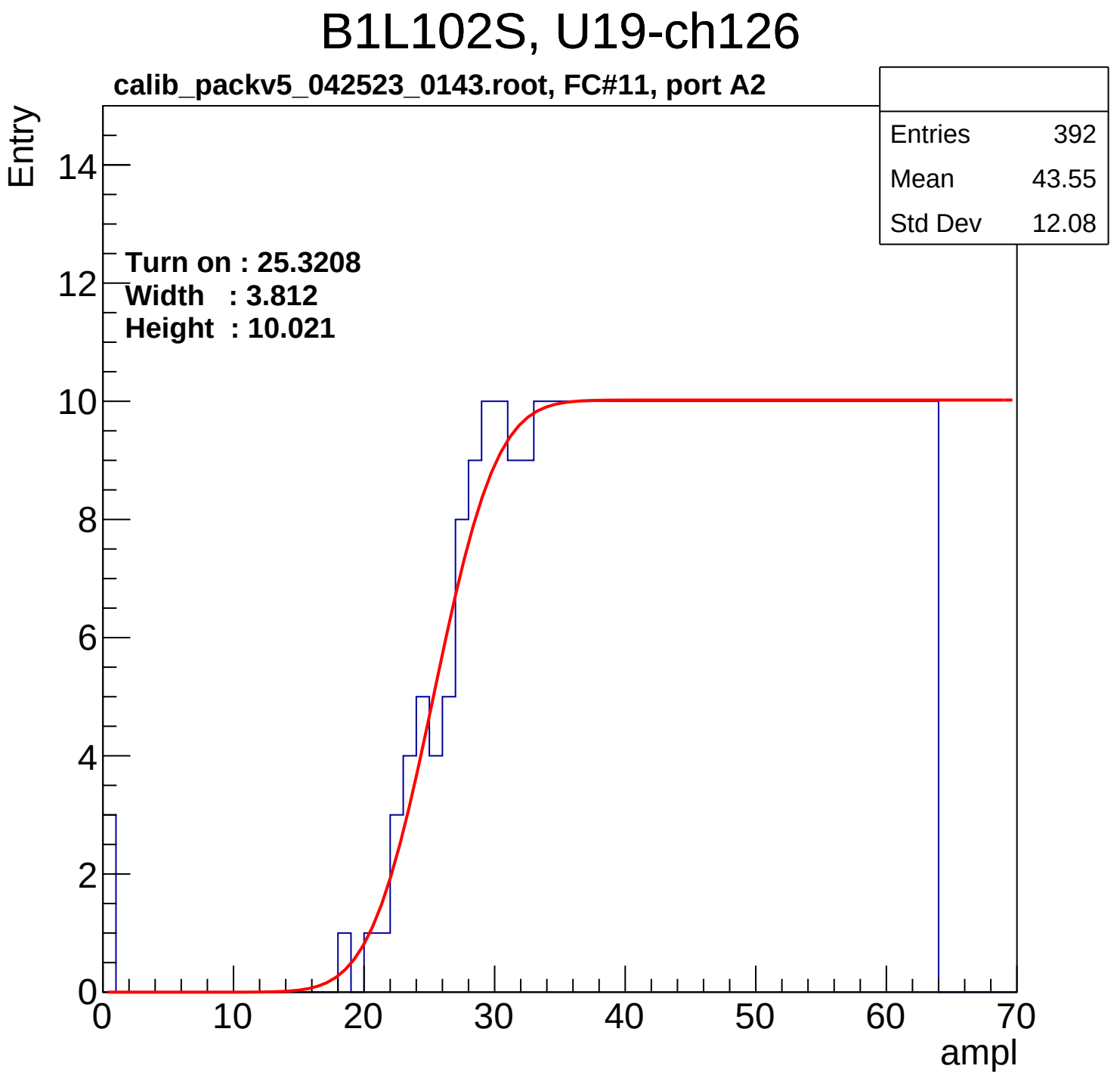

B1L102S, U19-ch121
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.01
Std Dev 11.77
Turn on : 25.6307
Width : 3.183
Height : 10.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

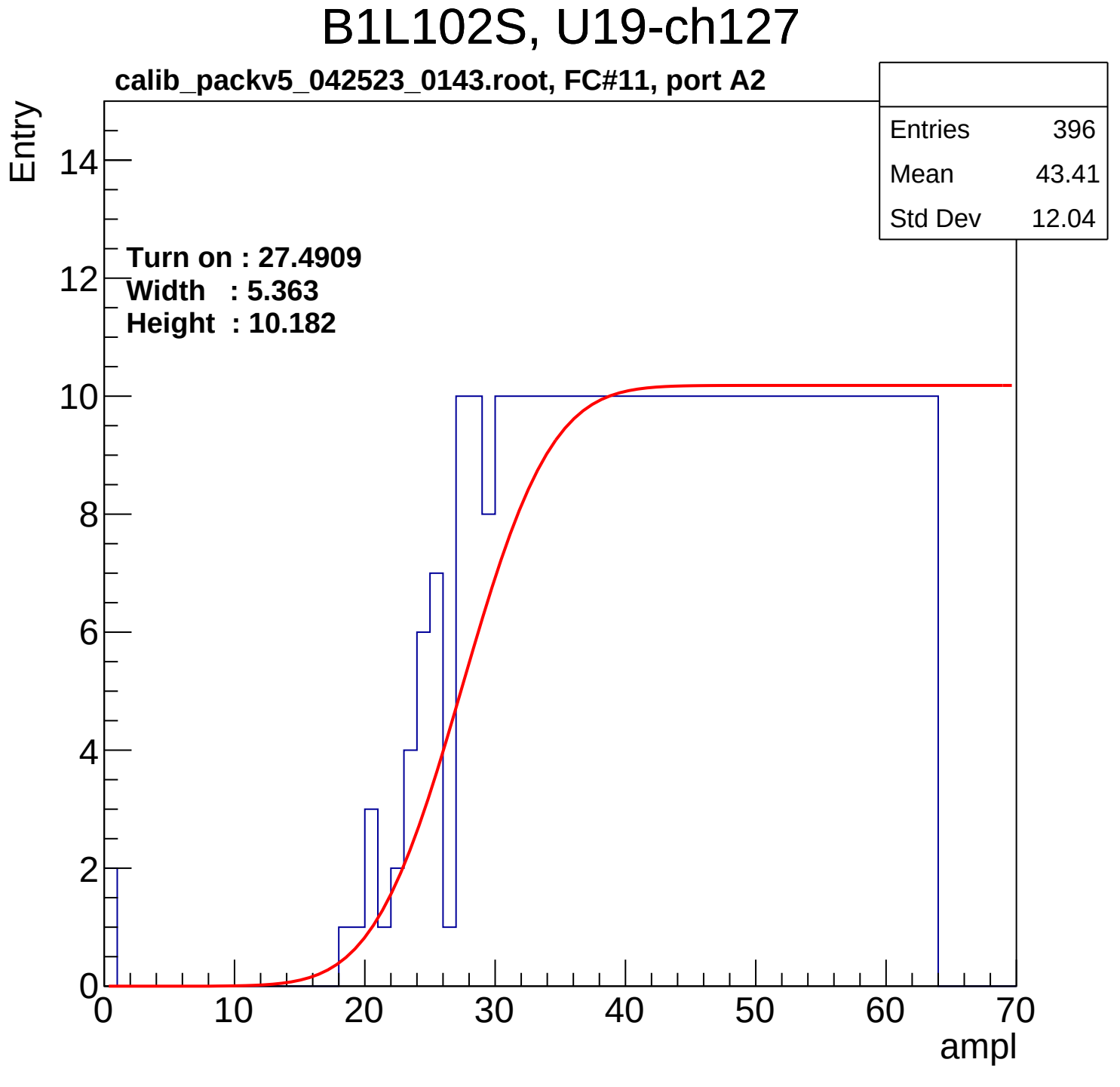

B1L102S, U19-ch122
calib_packv5_042523_0143.root, FC#11, port A2
Entries 412
Mean 42.68
Std Dev 12.35
Turn on : 22.7579
Width : 3.428
Height : 10.025
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

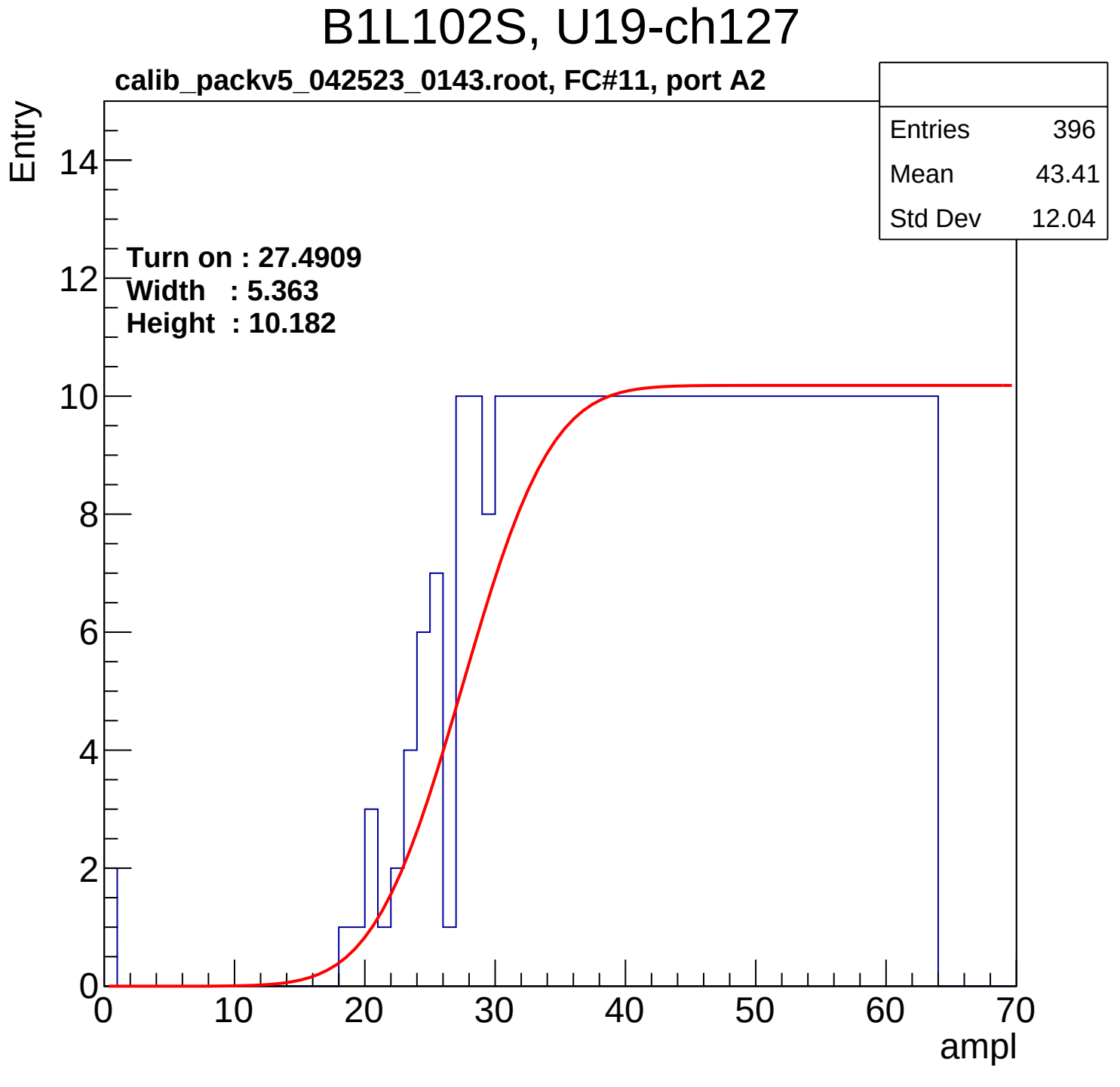

B1L102S, U19-ch123
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.53
Std Dev 12.25
Turn on : 25.8171
Width : 2.272
Height : 10.054
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U19-ch124
calib_packv5_042523_0143.root, FC#11, port A2
Entries 384
Mean 44.05
Std Dev 11.64
Turn on : 25.7277
Width : 3.169
Height : 9.993
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U19-ch125
calib_packv5_042523_0143.root, FC#11, port A2
Entries 368
Mean 44.74
Std Dev 11.48
Turn on : 27.8601
Width : 3.506
Height : 10.015
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U19-ch126
calib_packv5_042523_0143.root, FC#11, port A2
Entries 392
Mean 43.55
Std Dev 12.08
Turn on : 25.3208
Width : 3.812
Height : 10.021
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U19-ch127
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.41
Std Dev 12.04
Turn on : 27.4909
Width : 5.363
Height : 10.182
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L102S, U19-ch127
calib_packv5_042523_0143.root, FC#11, port A2
Entries 396
Mean 43.41
Std Dev 12.04
Turn on : 27.4909
Width : 5.363
Height : 10.182
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
70