



# B1L103S, U1-ch0, adc0

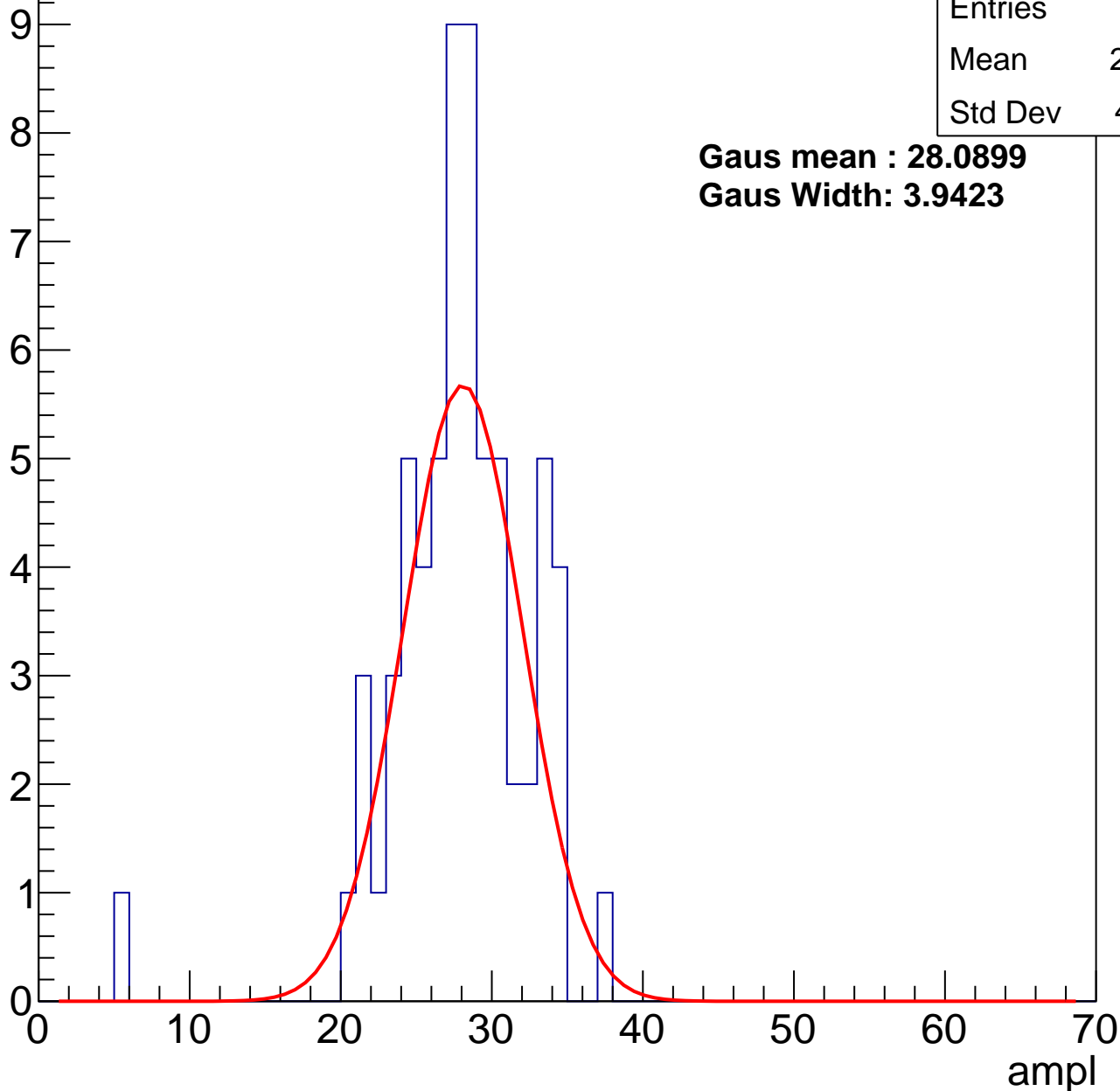
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	27.43
Std Dev	4.641

**Gaus mean : 28.0899**

**Gaus Width: 3.9423**



# B1L103S, U1-ch0, adc1

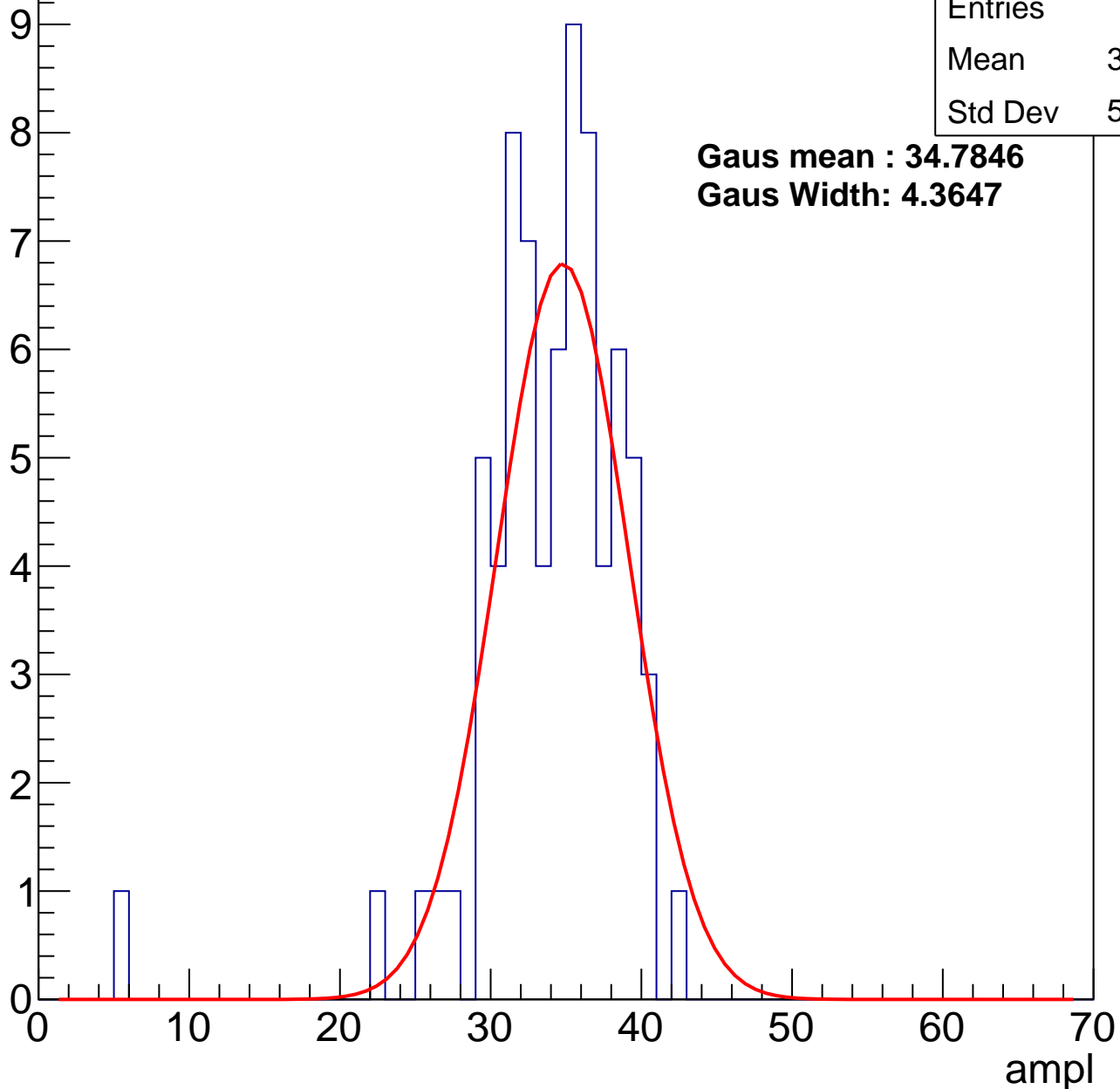
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	33.52
Std Dev	5.066

**Gaus mean : 34.7846**

**Gaus Width: 4.3647**



# B1L103S, U1-ch0, adc2

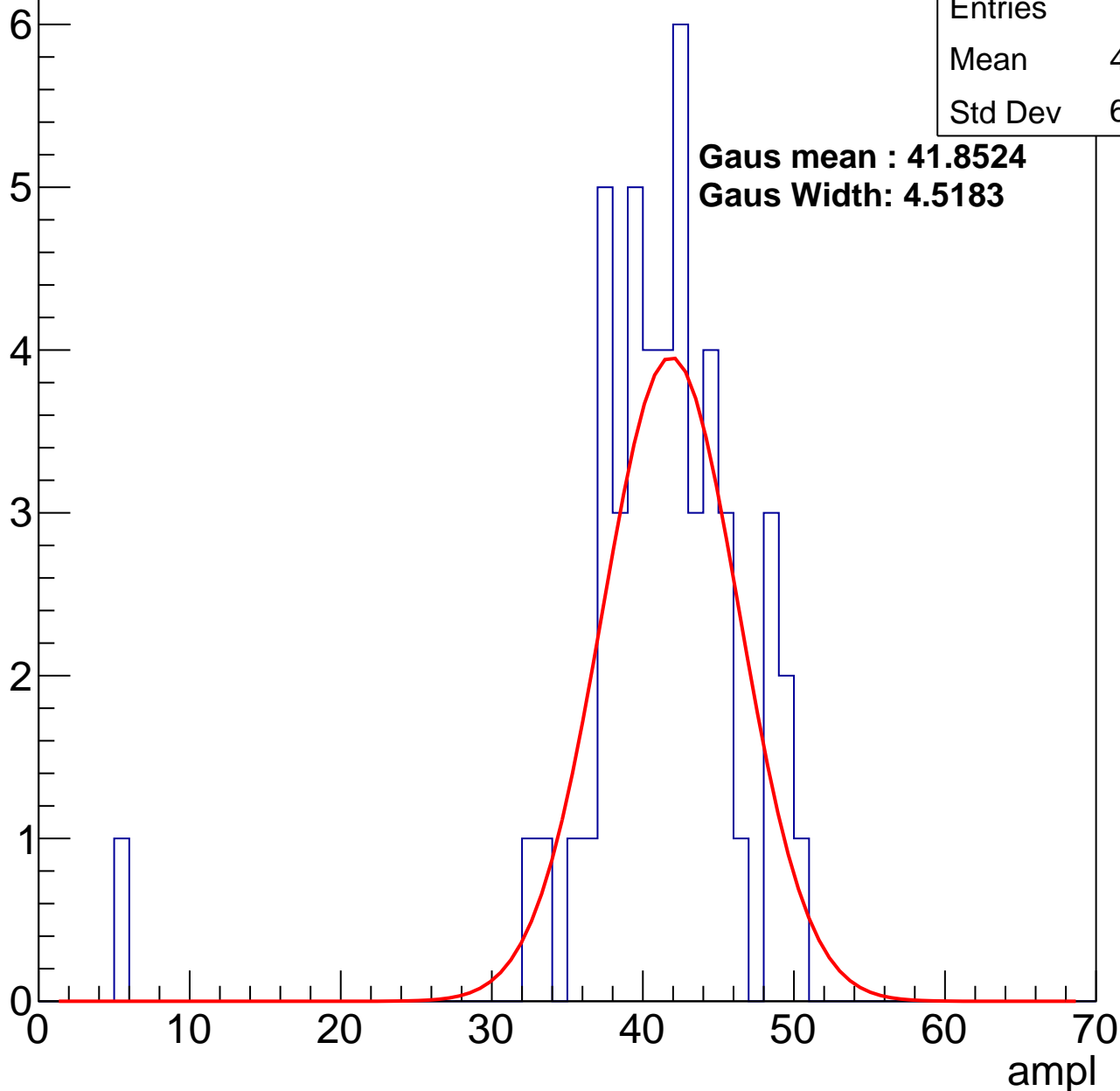
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	40.59
Std Dev	6.559

**Gaus mean : 41.8524**

**Gaus Width: 4.5183**

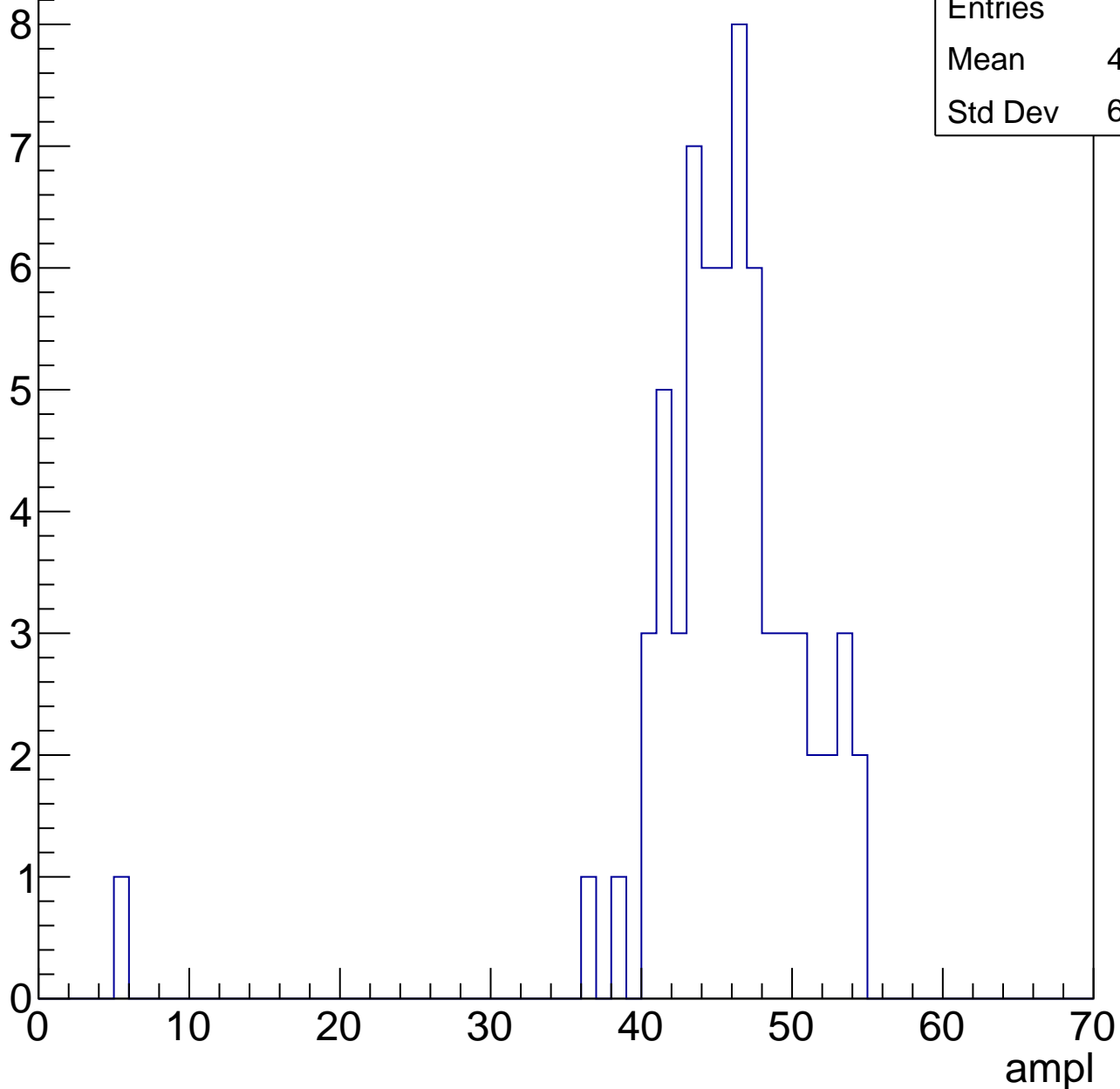


# B1L103S, U1-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	45.06
Std Dev	6.387

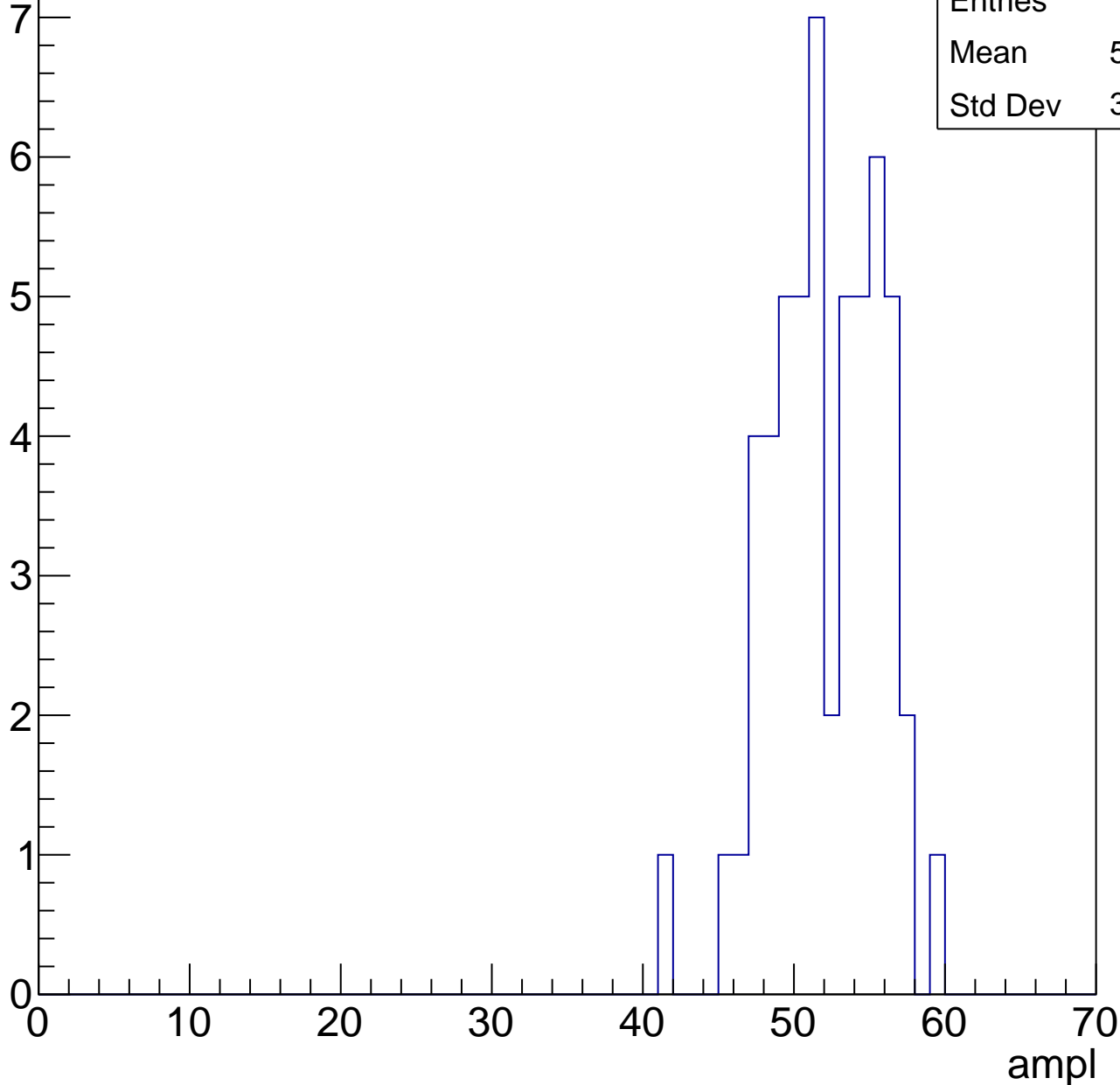


# B1L103S, U1-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	51.59
Std Dev	3.577

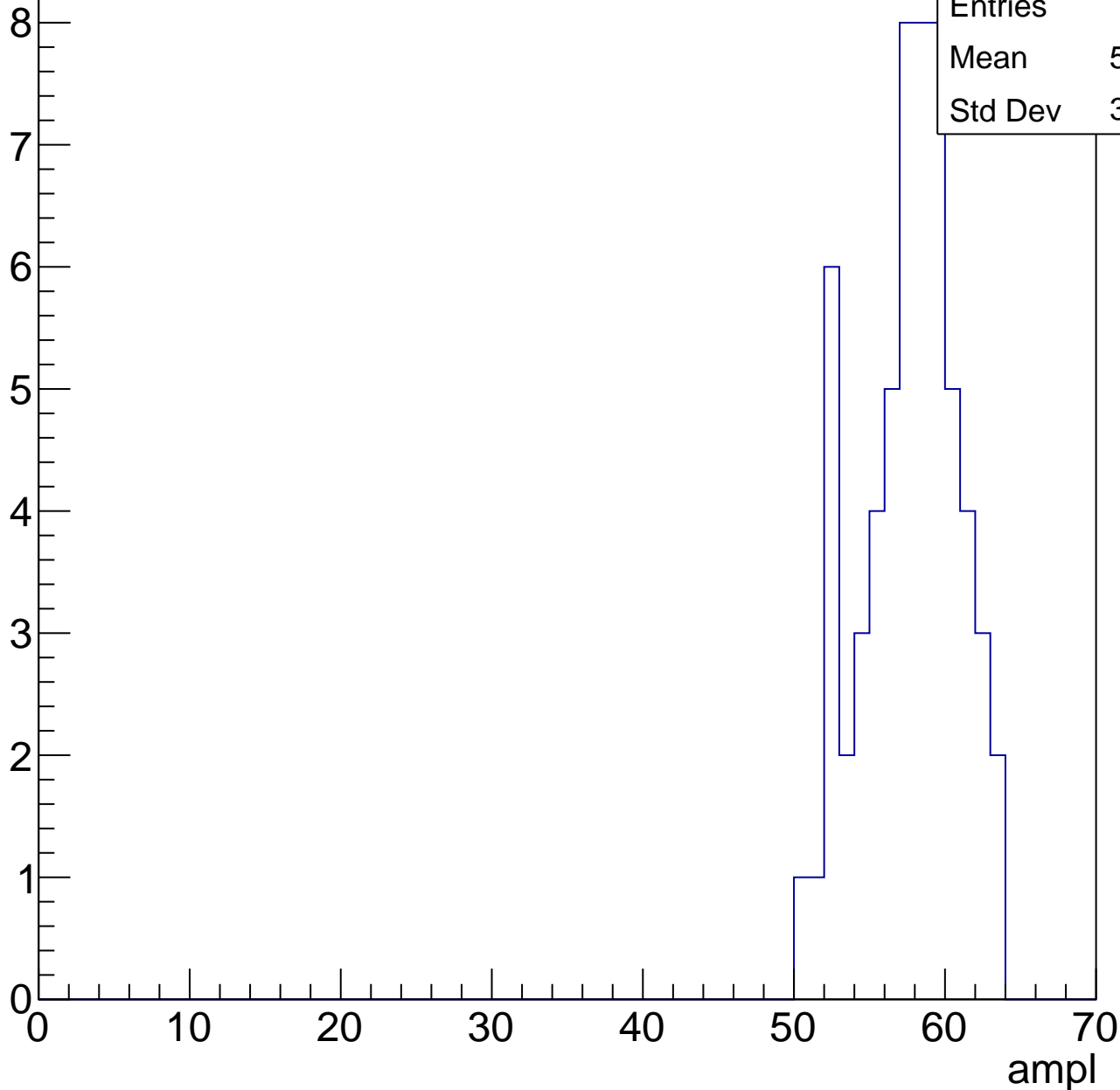


# B1L103S, U1-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

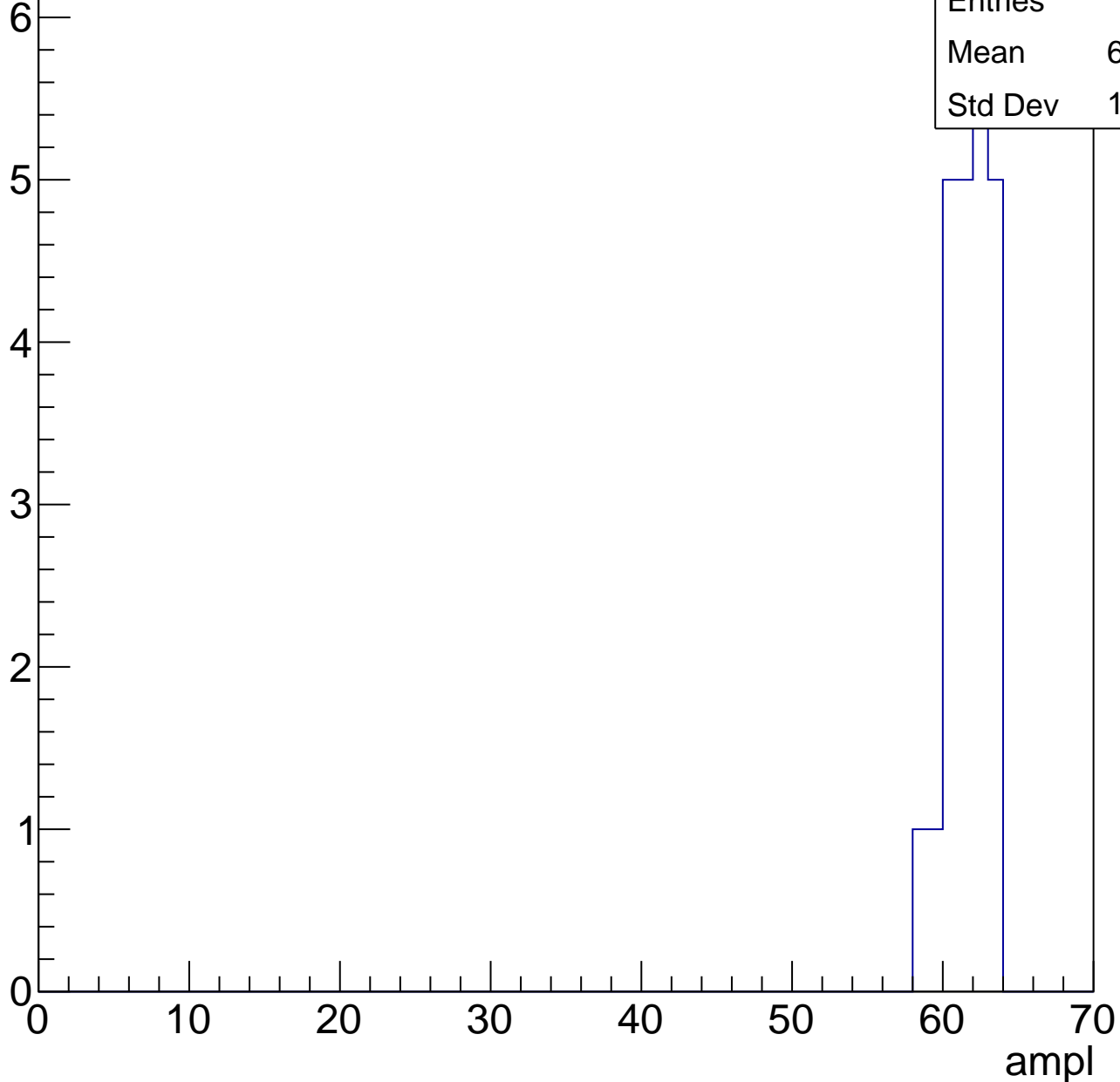
Entries	60
Mean	57.15
Std Dev	3.188



# B1L103S, U1-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

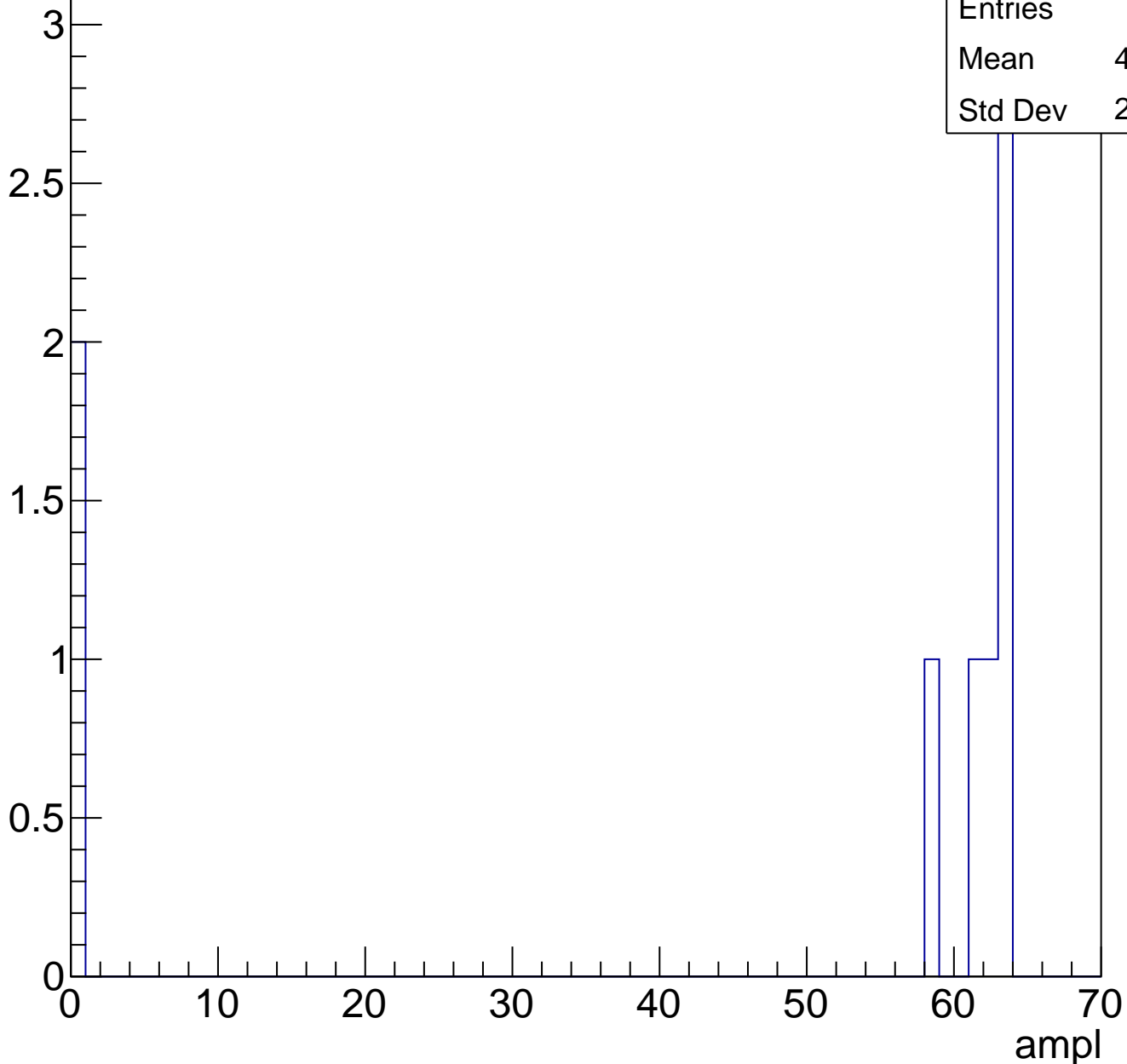




# B1L103S, U1-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch1, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	70
Mean	26.97
Std Dev	6.522

**Gaus mean : 28.3248**

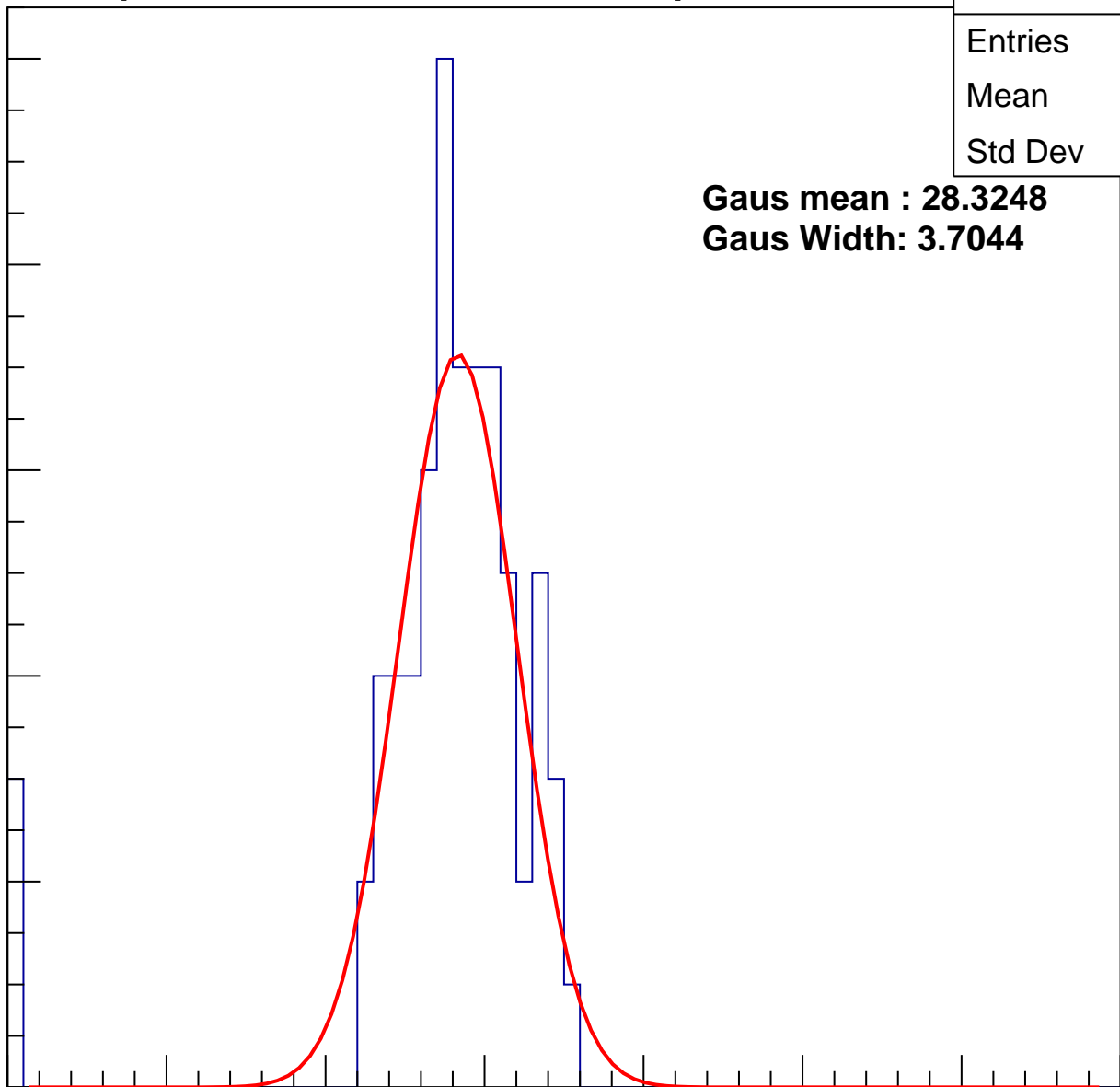
**Gaus Width: 3.7044**

Entry

10  
8  
6  
4  
2  
0

ampl

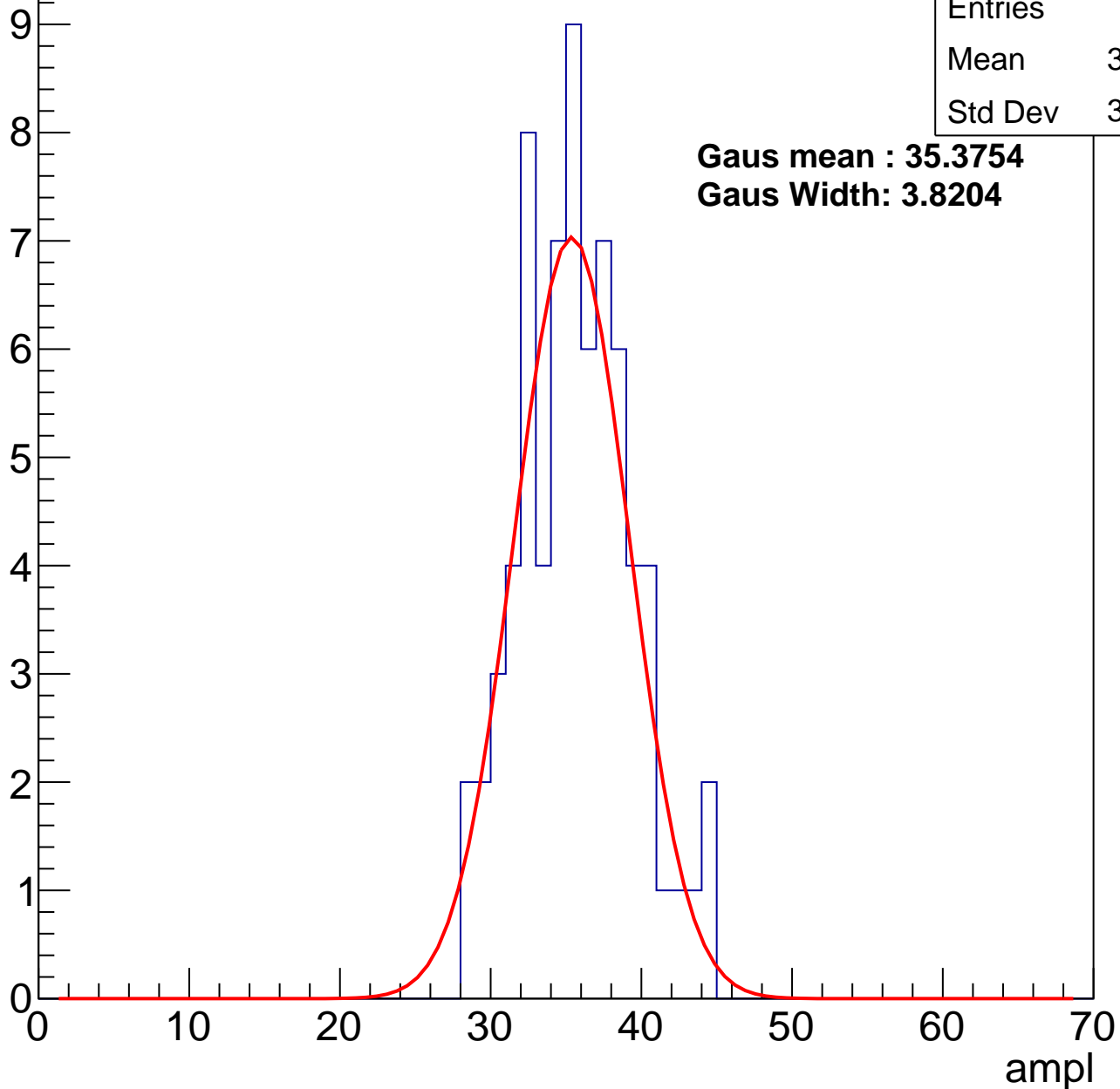
0 10 20 30 40 50 60 70



# B1L103S, U1-ch1, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch1, adc2

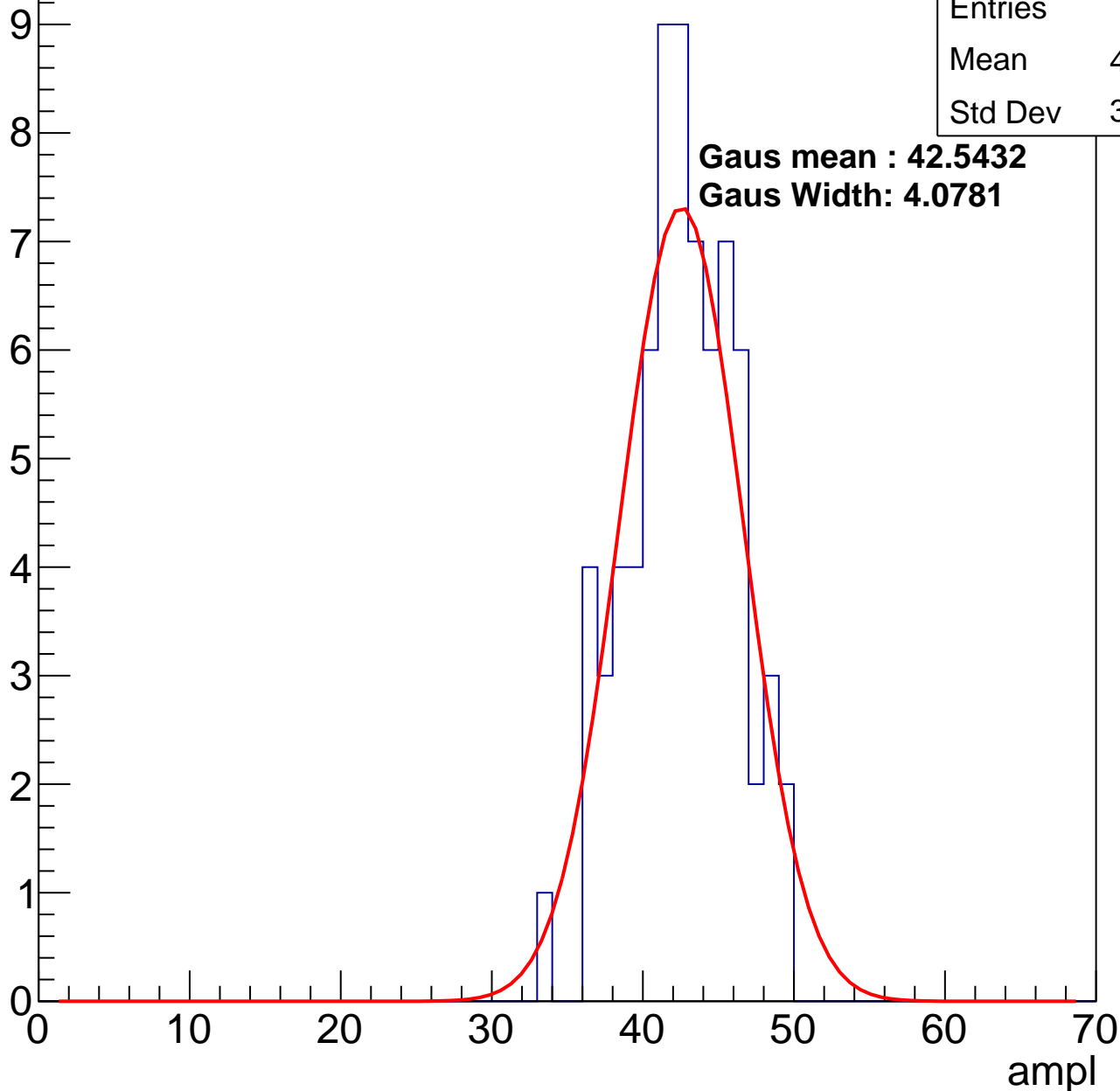
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	42.12
Std Dev	3.468

**Gaus mean : 42.5432**

**Gaus Width: 4.0781**

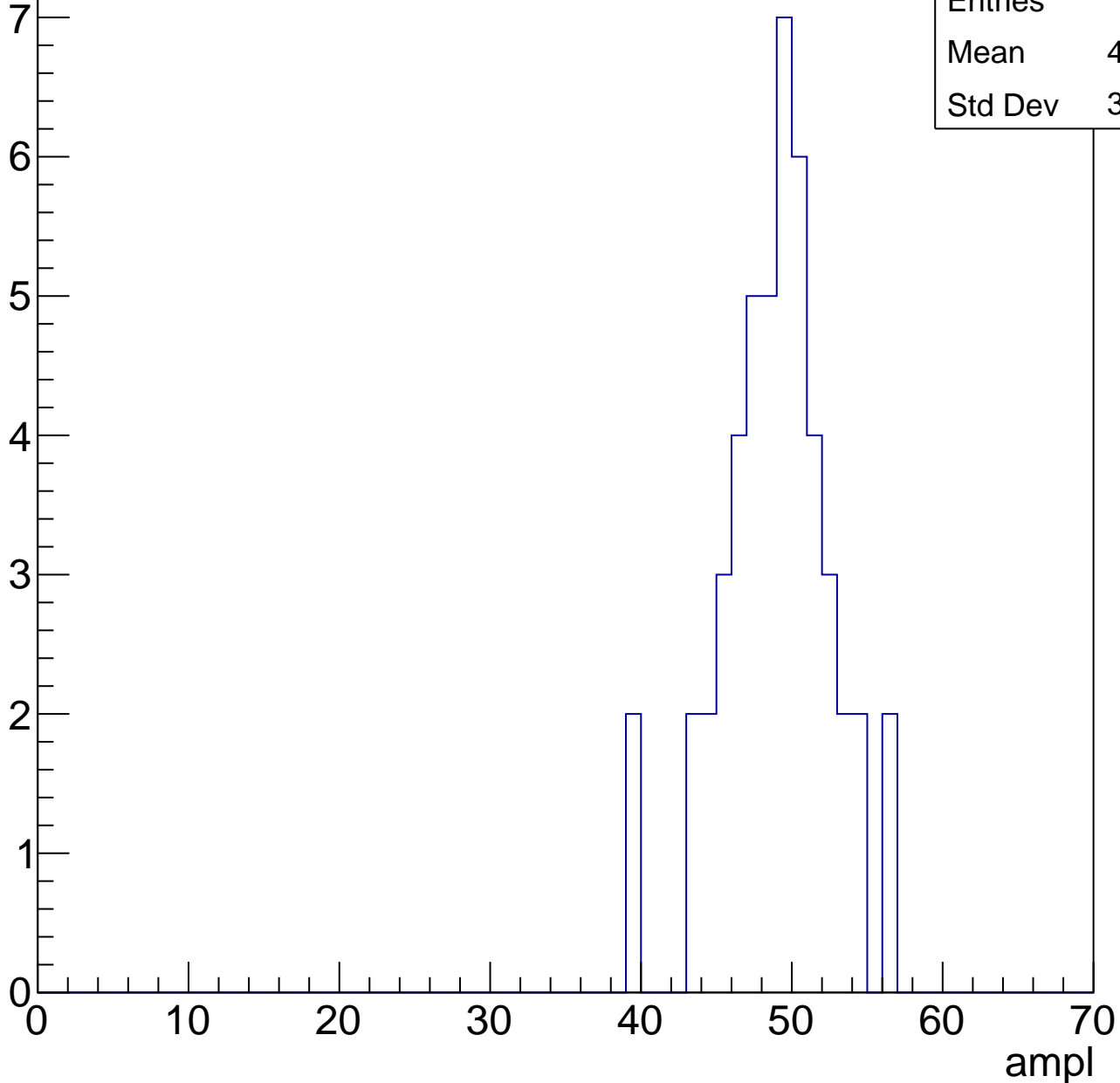


# B1L103S, U1-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

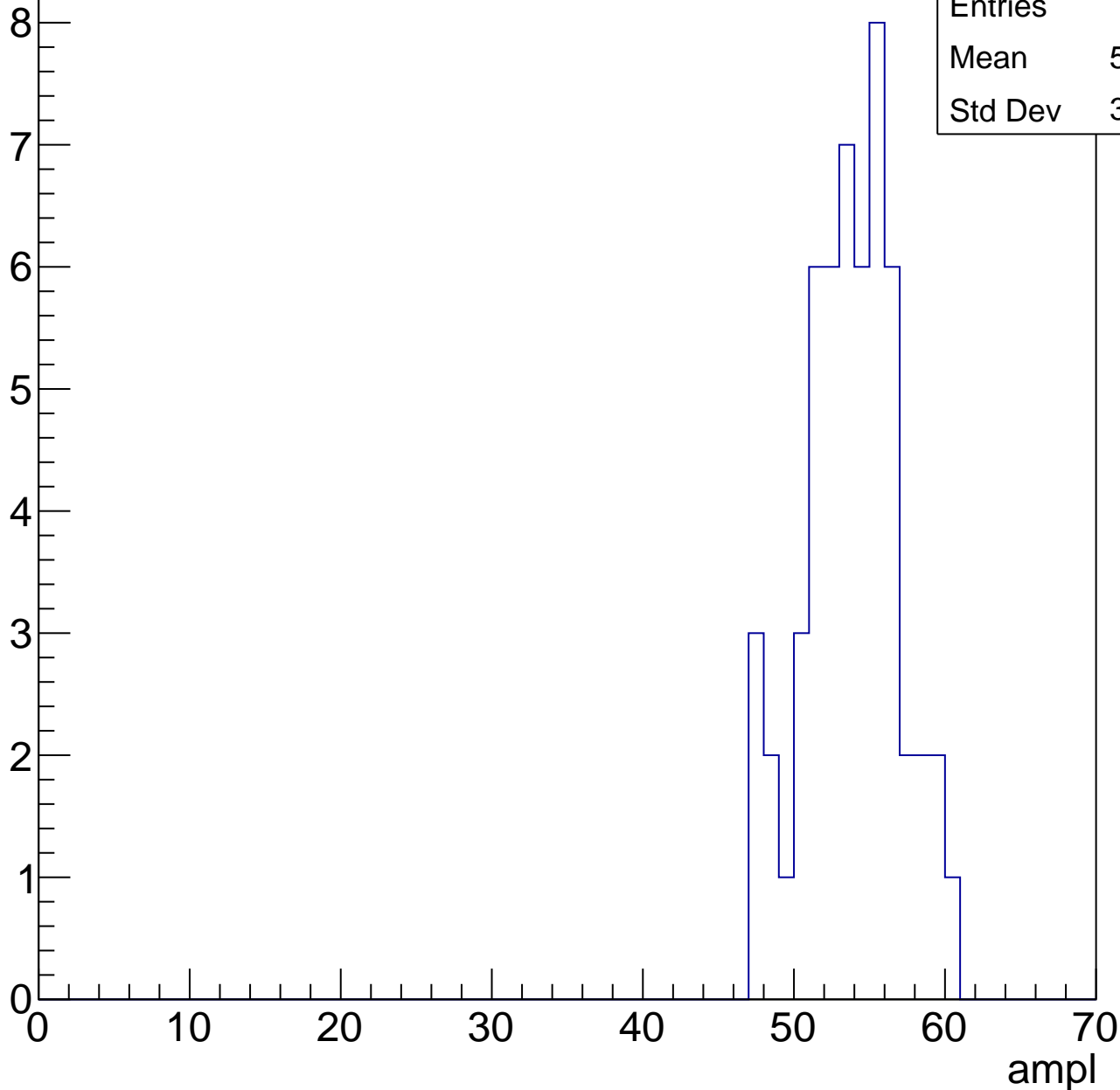
Entries	49
Mean	48.47
Std Dev	3.632



# B1L103S, U1-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

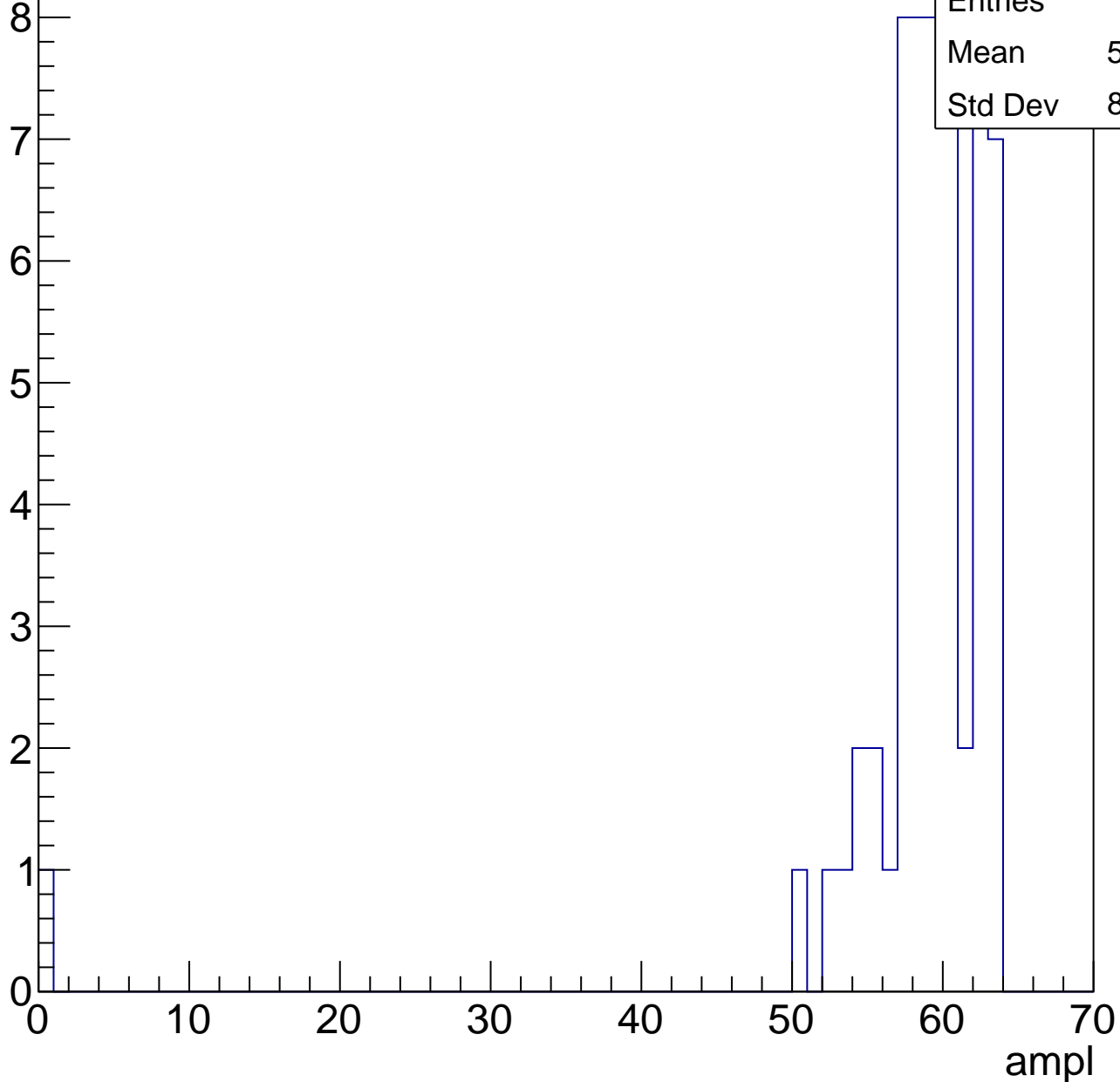


Entries	55
Mean	53.33
Std Dev	3.075

# B1L103S, U1-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

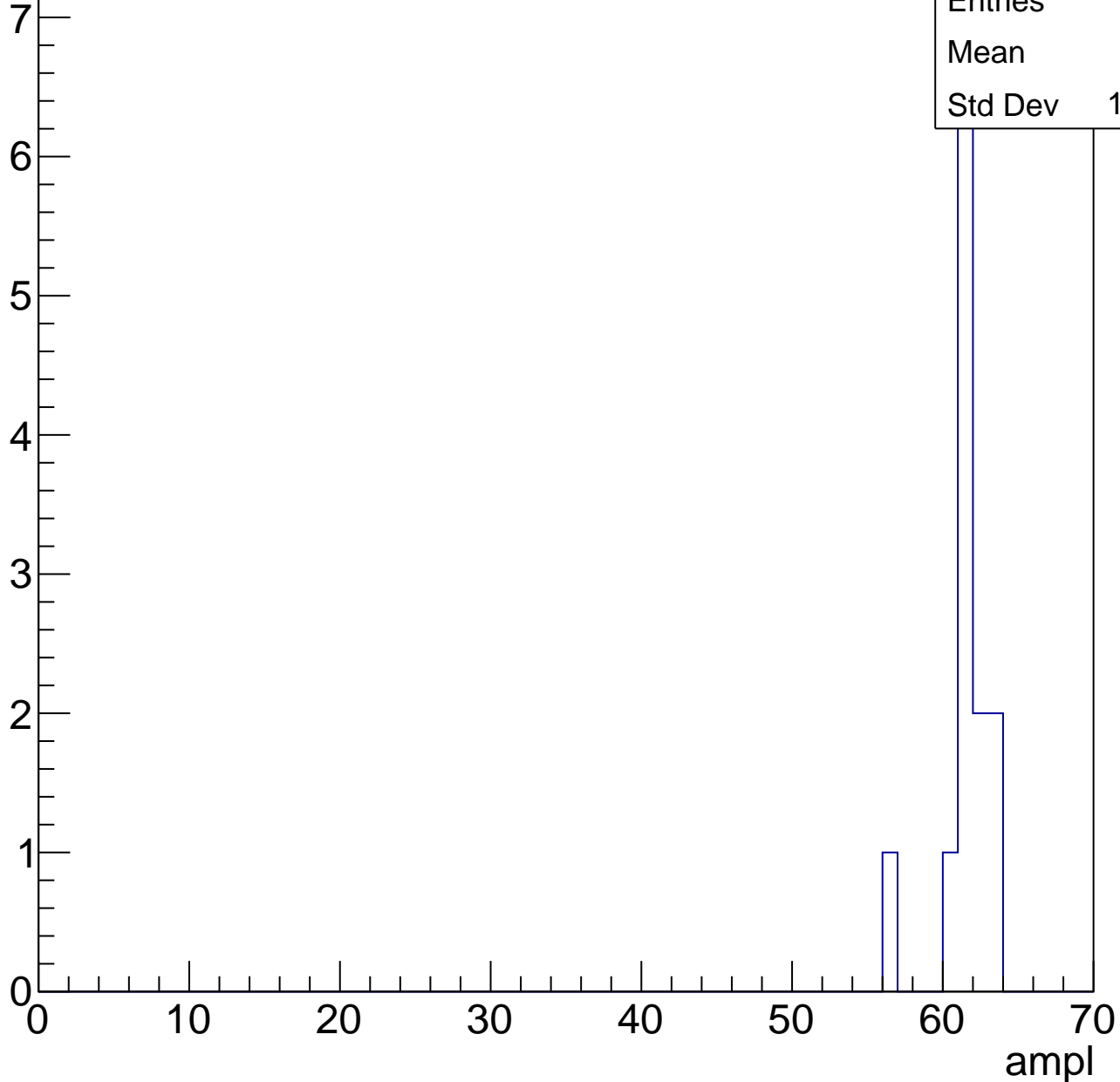


# B1L103S, U1-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	13
Mean	61
Std Dev	1.664





# B1L103S, U1-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch2, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	76
Mean	28.96
Std Dev	6.049

**Gaus mean : 30.6008**

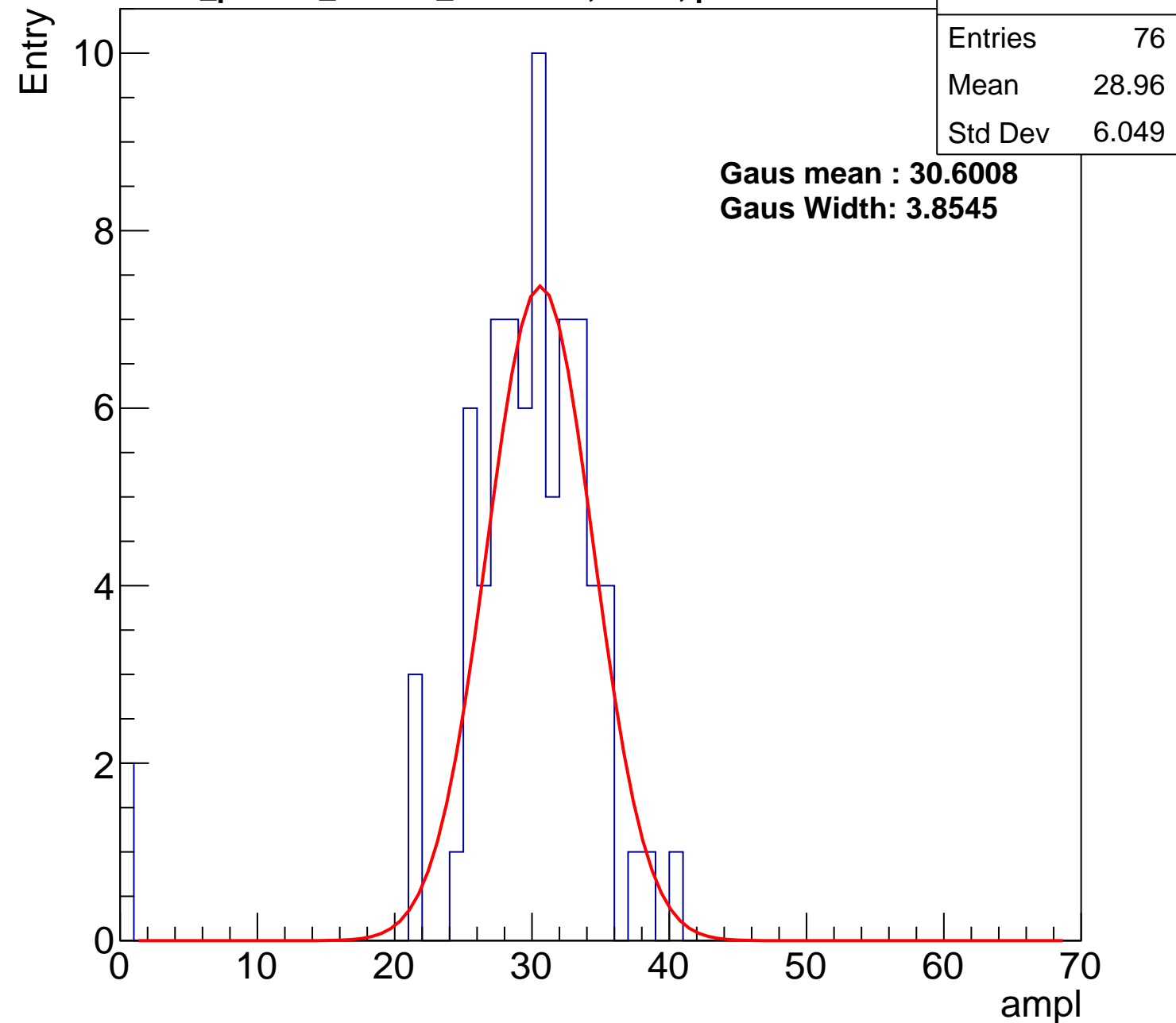
**Gaus Width: 3.8545**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U1-ch2, adc1

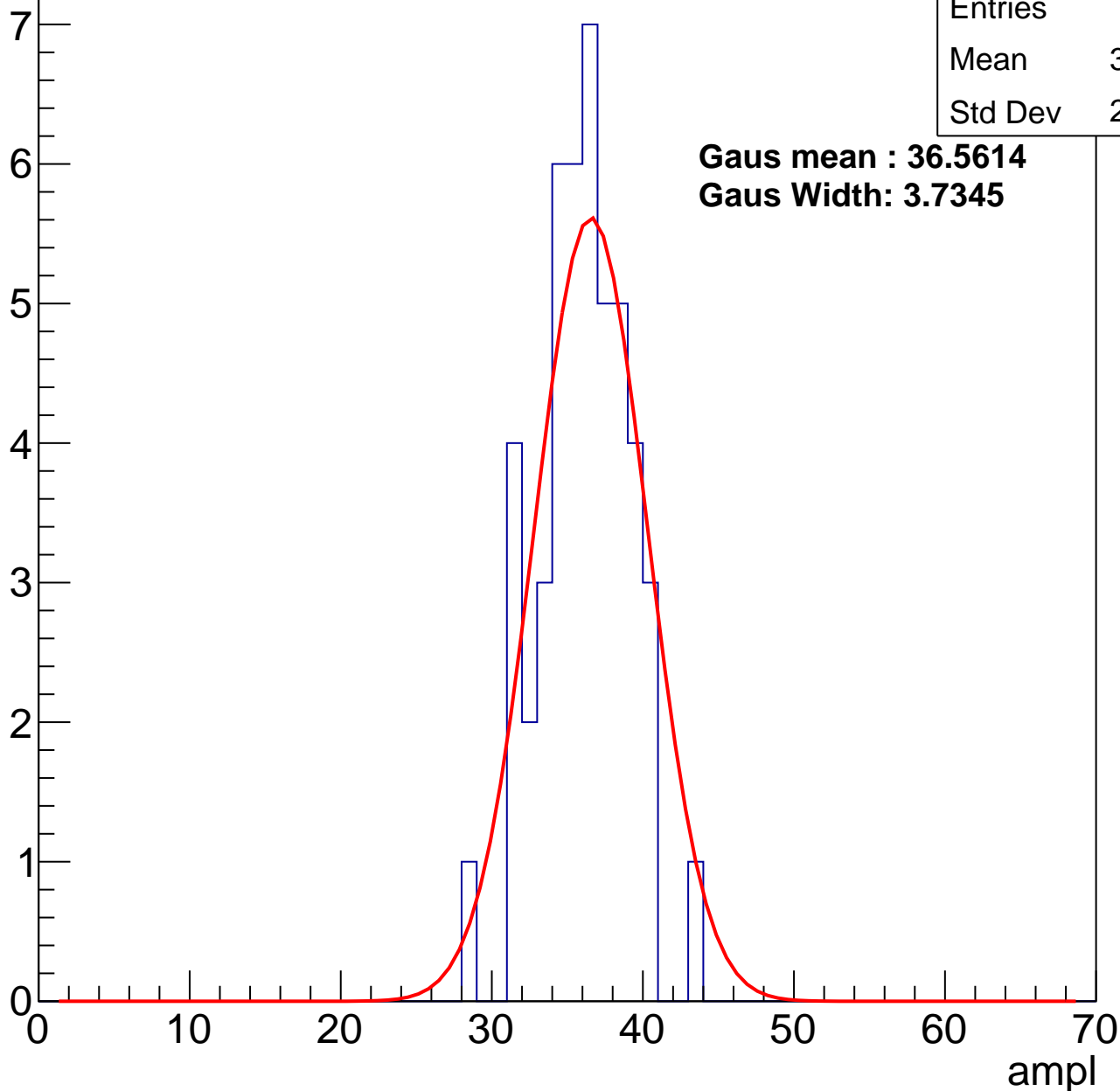
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	35.64
Std Dev	2.935

**Gaus mean : 36.5614**

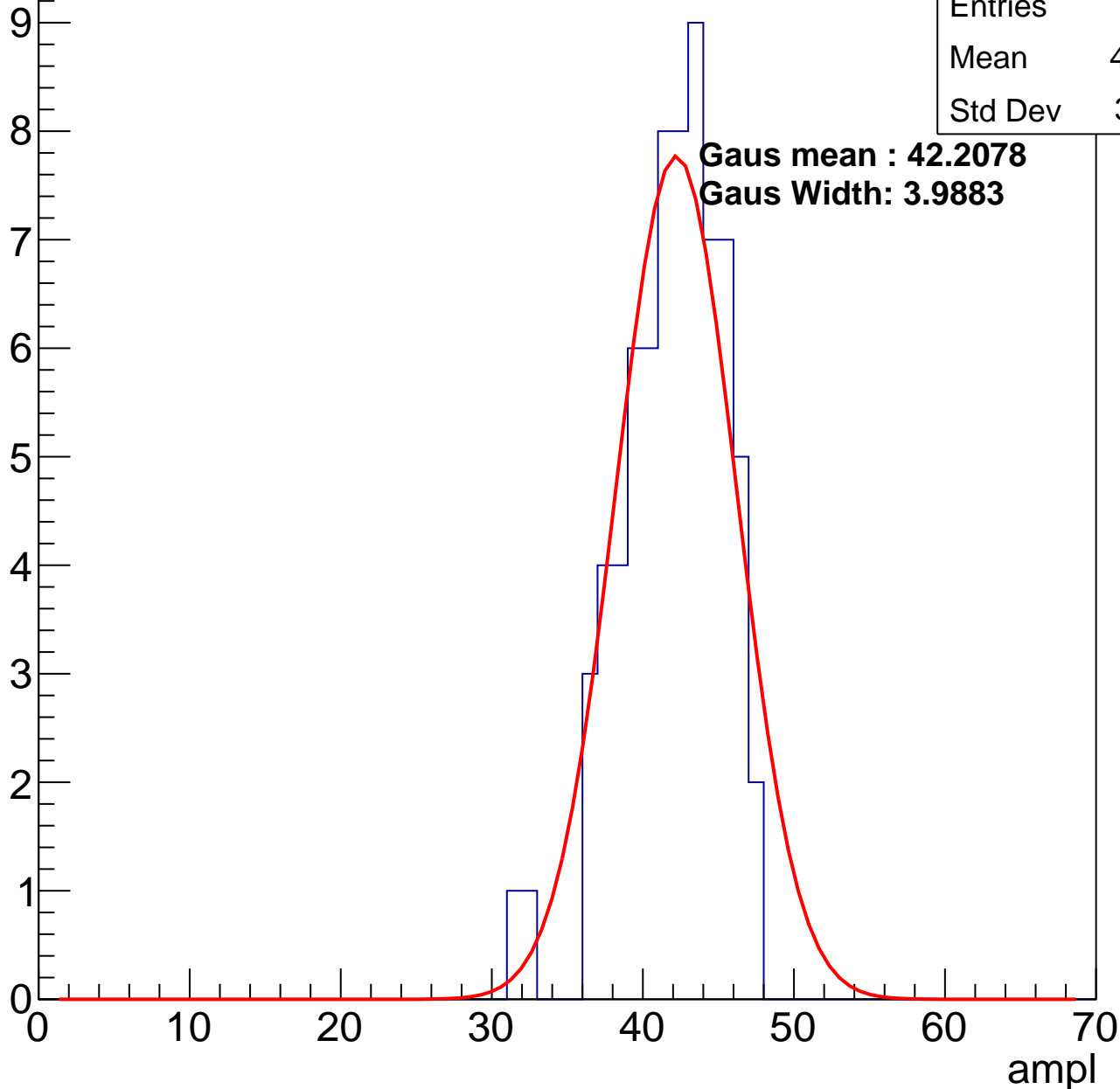
**Gaus Width: 3.7345**



# B1L103S, U1-ch2, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	77
Mean	49.6
Std Dev	3.988

Entry

10

8

6

4

2

0

0

10

20

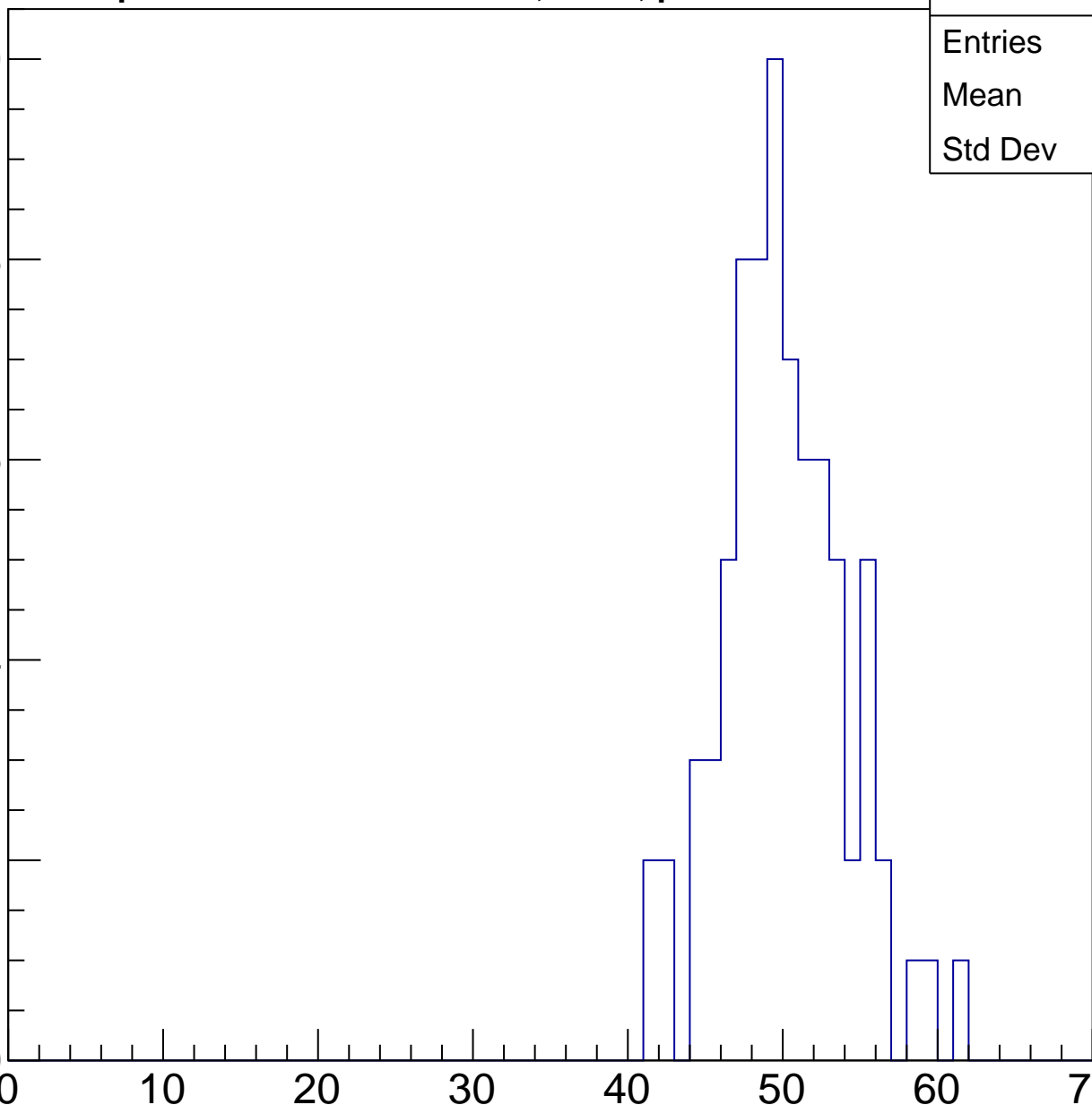
30

40

50

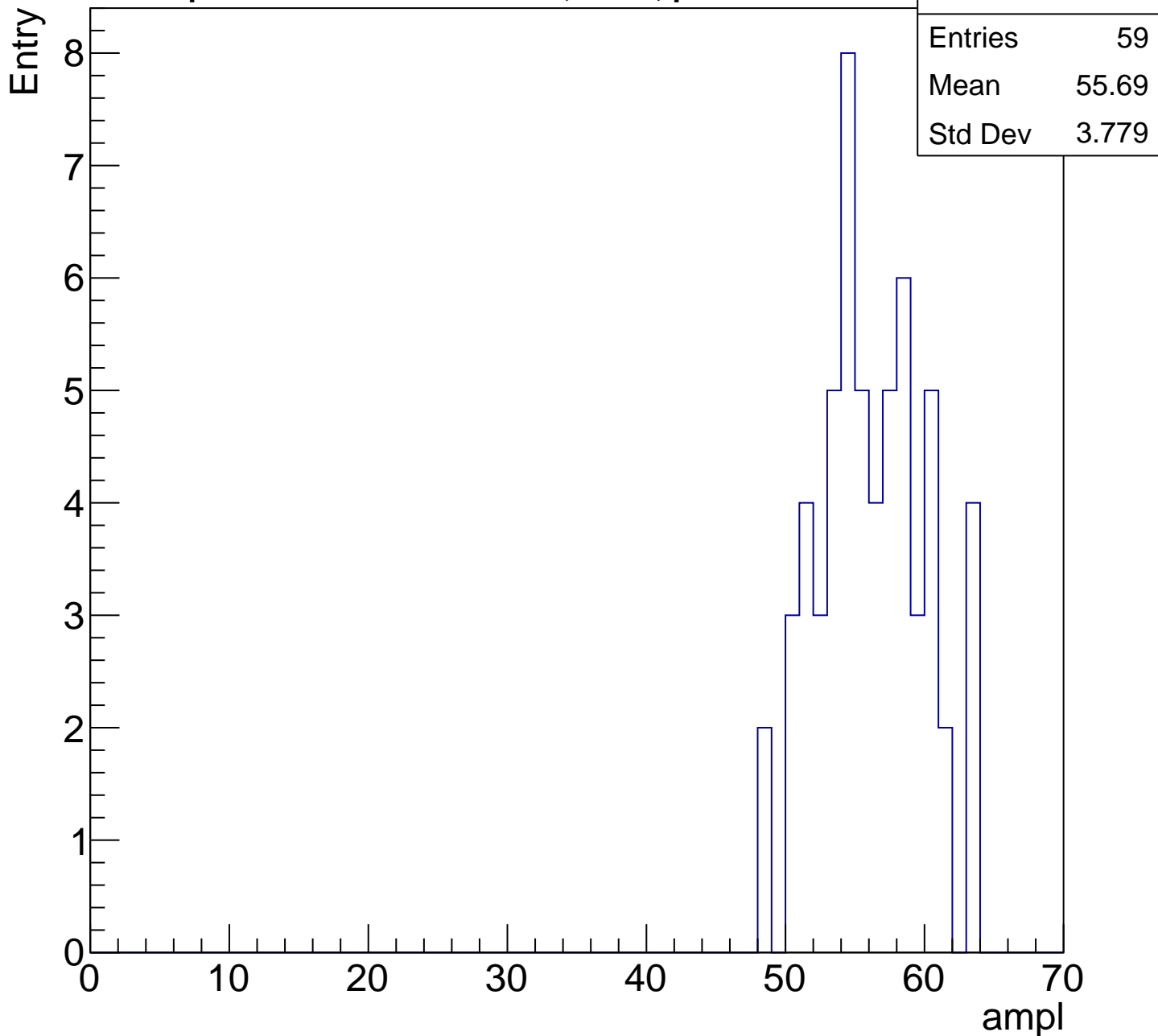
60

ampl



# B1L103S, U1-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

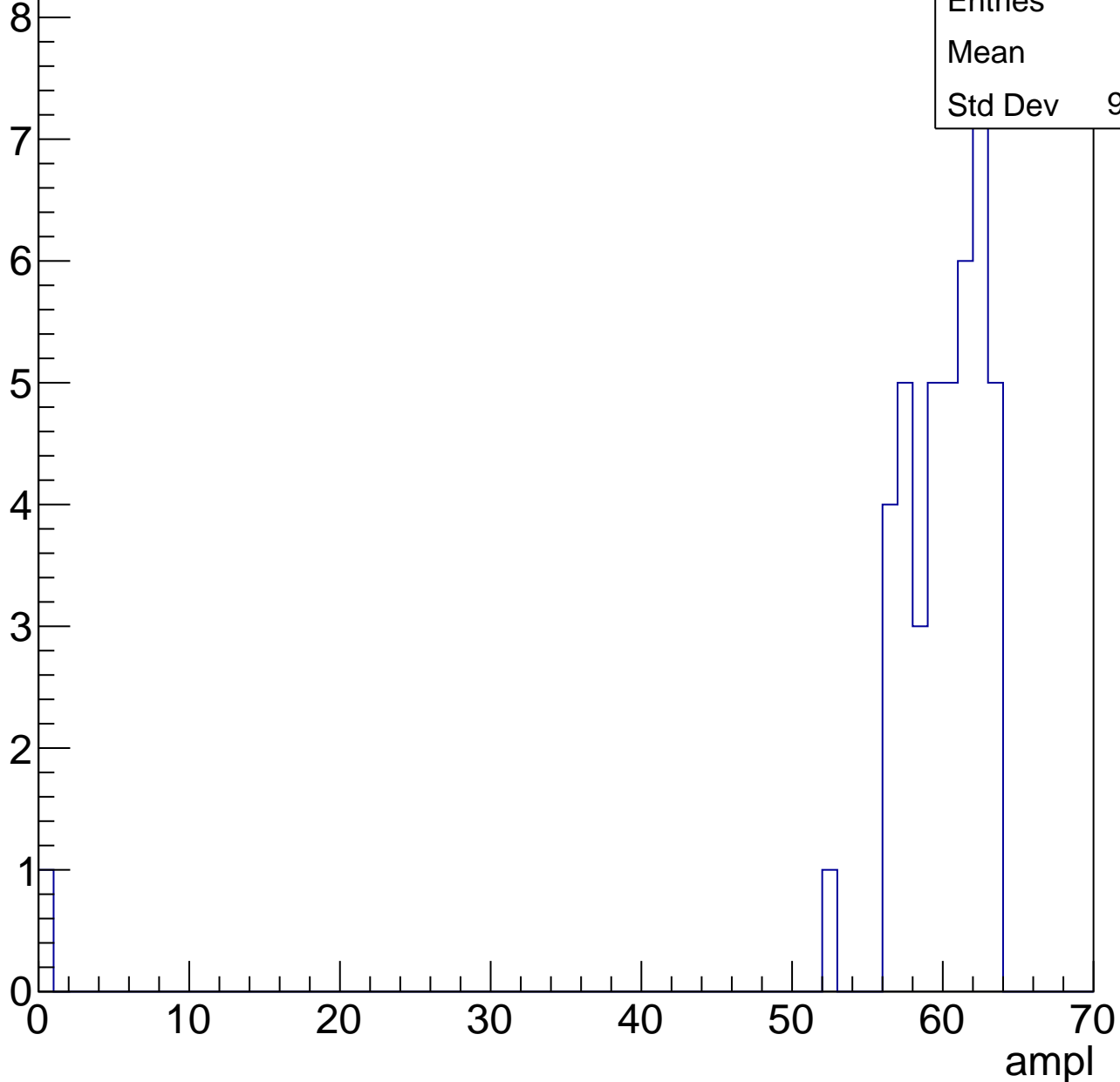


# B1L103S, U1-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	43
Mean	58.3
Std Dev	9.337



# B1L103S, U1-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.4
Std Dev	1.356

ampl

0 10 20 30 40 50 60 70



# B1L103S, U1-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch3, adc0

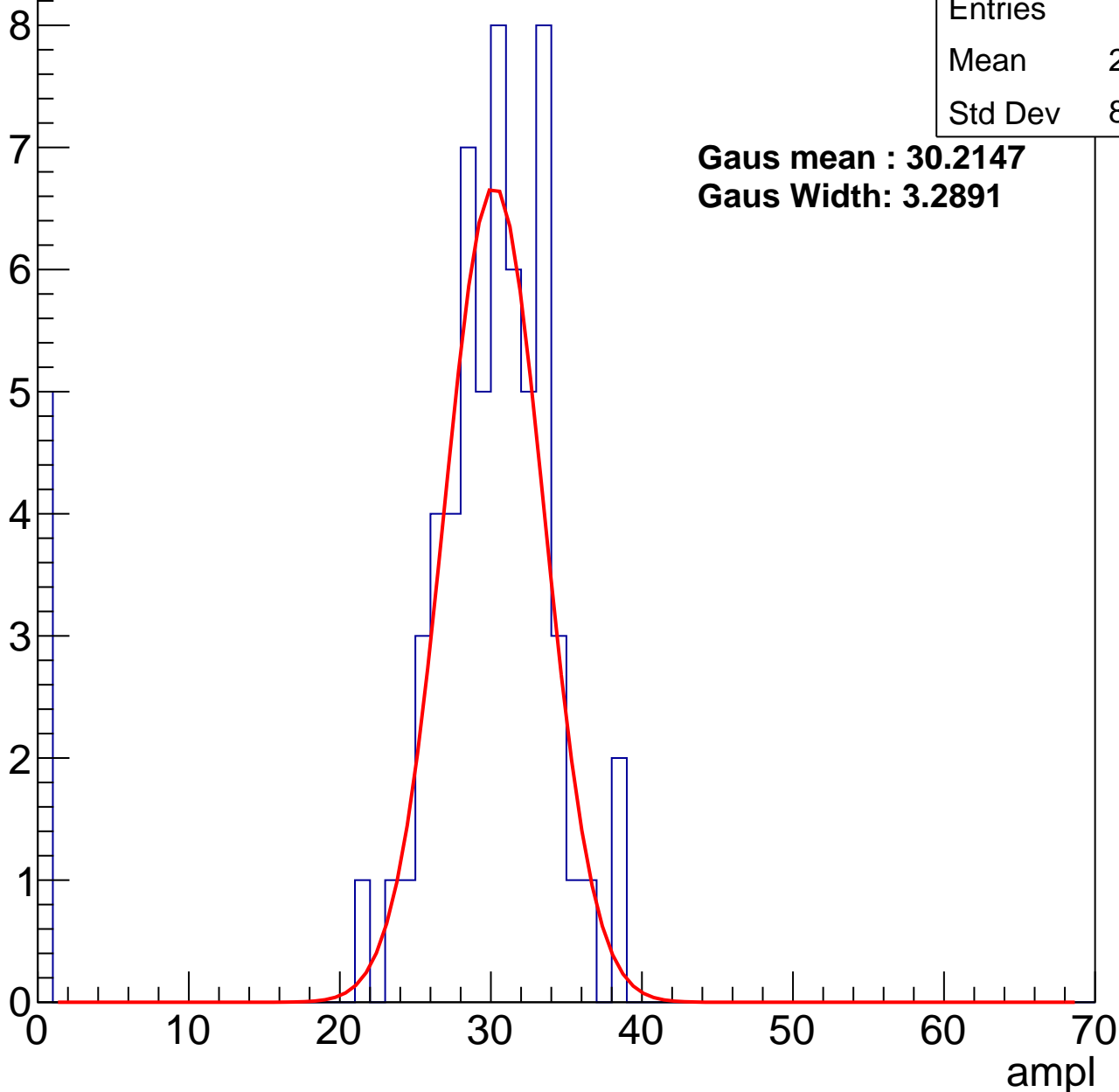
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	27.62
Std Dev	8.629

**Gaus mean : 30.2147**

**Gaus Width: 3.2891**



# B1L103S, U1-ch3, adc1

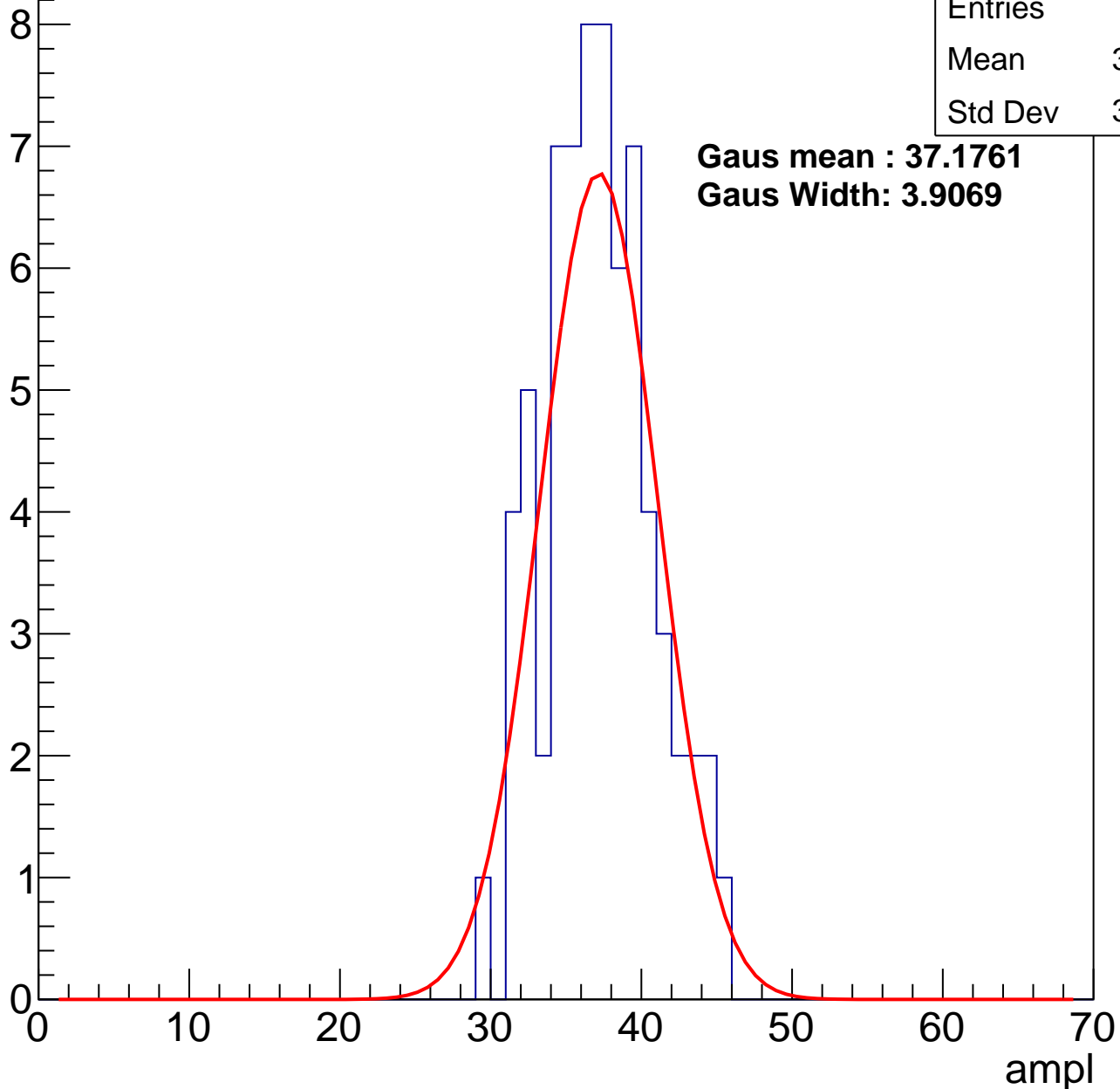
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	36.71
Std Dev	3.531

**Gaus mean : 37.1761**

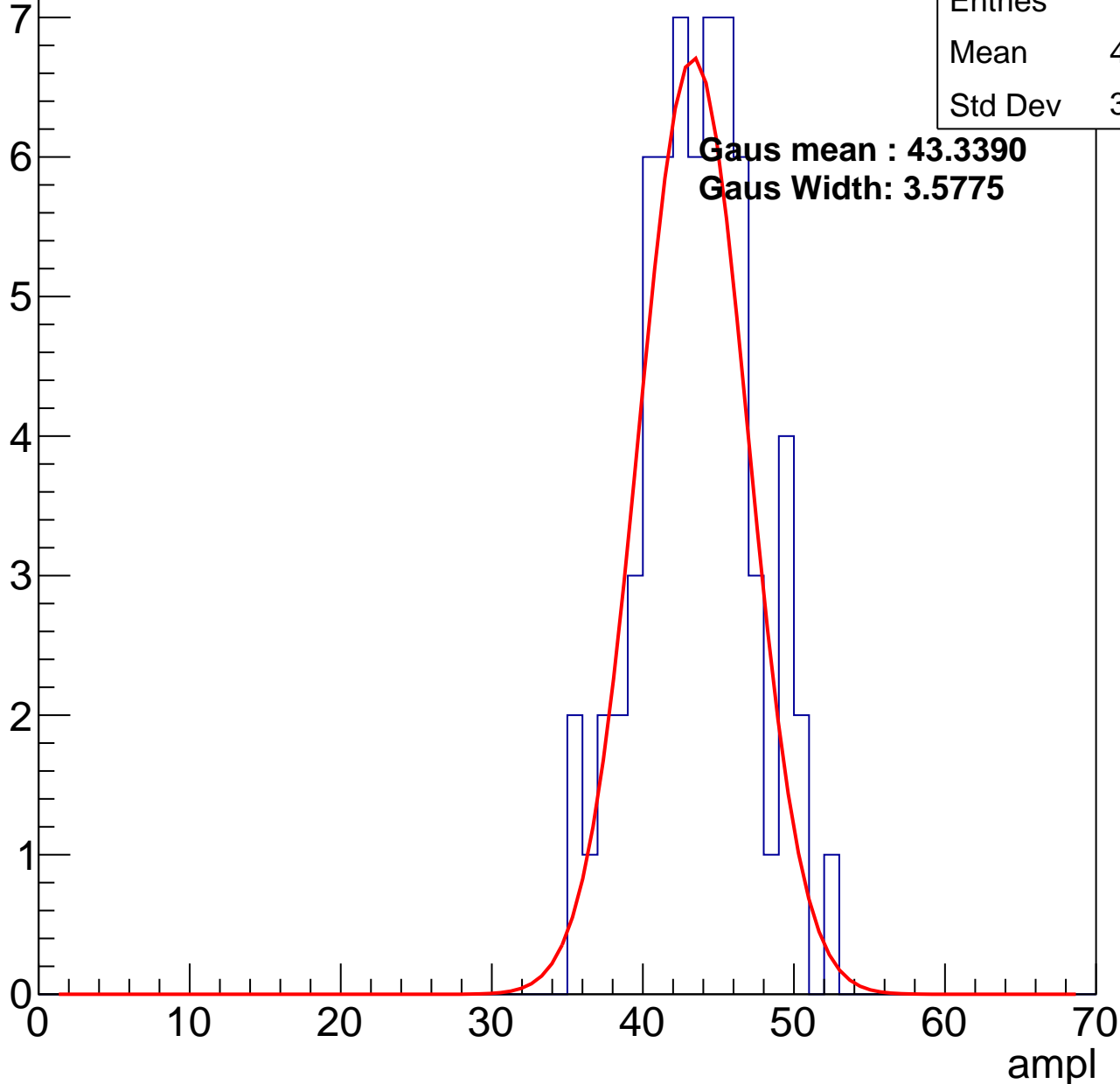
**Gaus Width: 3.9069**



# B1L103S, U1-ch3, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

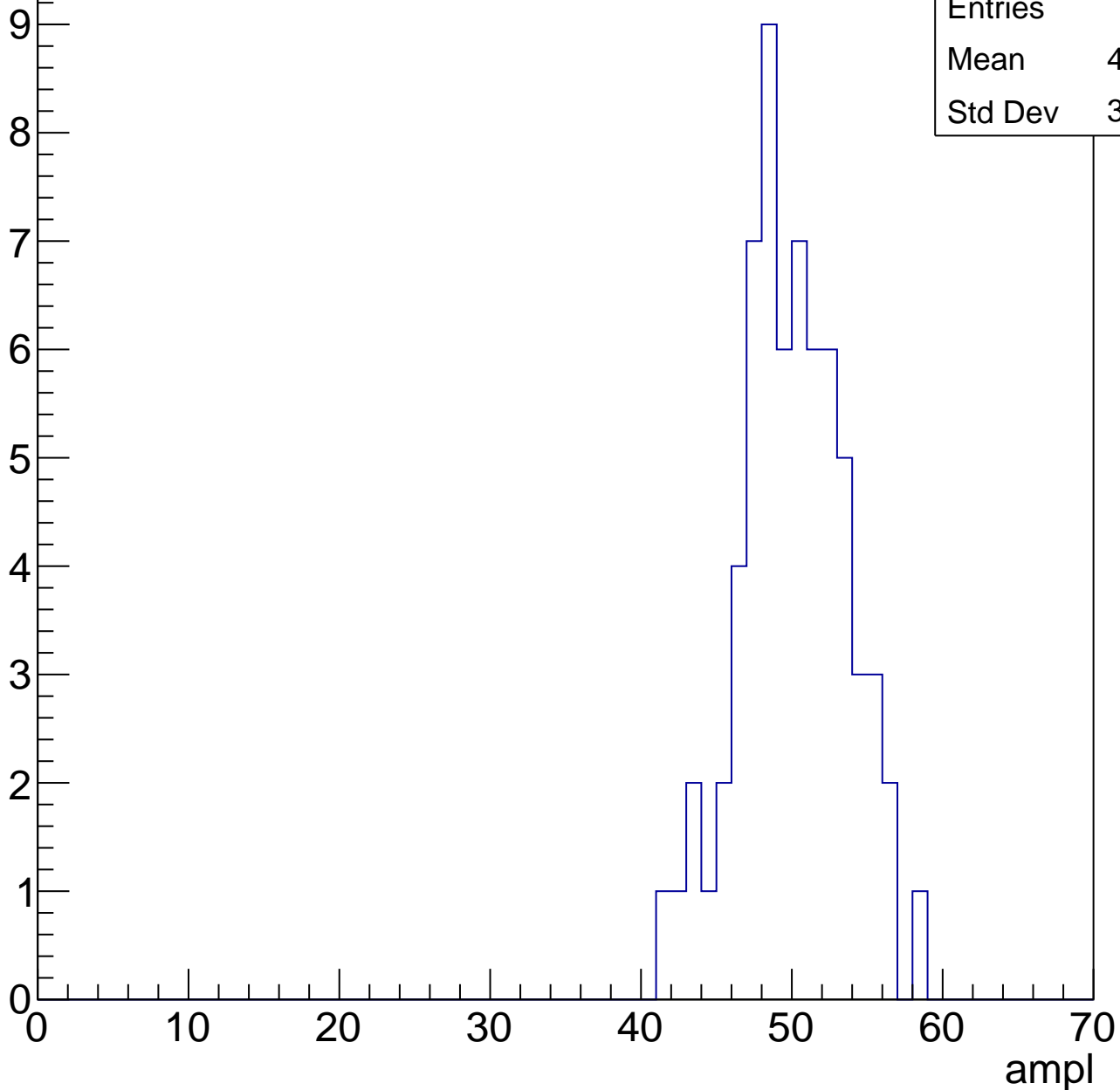


# B1L103S, U1-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	49.58
Std Dev	3.525

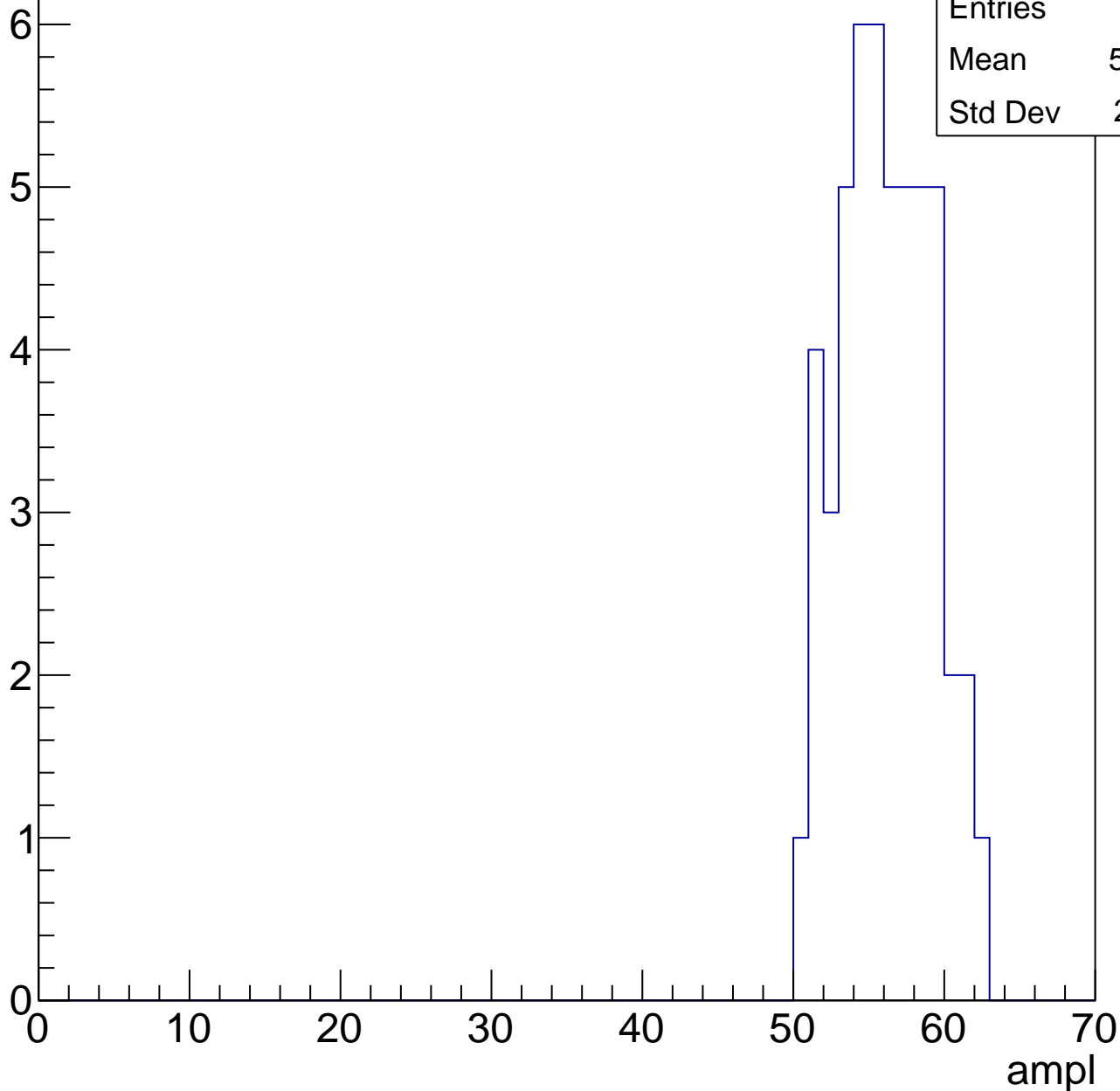


# B1L103S, U1-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	55.66
Std Dev	2.971



# B1L103S, U1-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	47
Mean	58.64
Std Dev	8.969

ampl

0

10

20

30

40

50

60

70

# B1L103S, U1-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

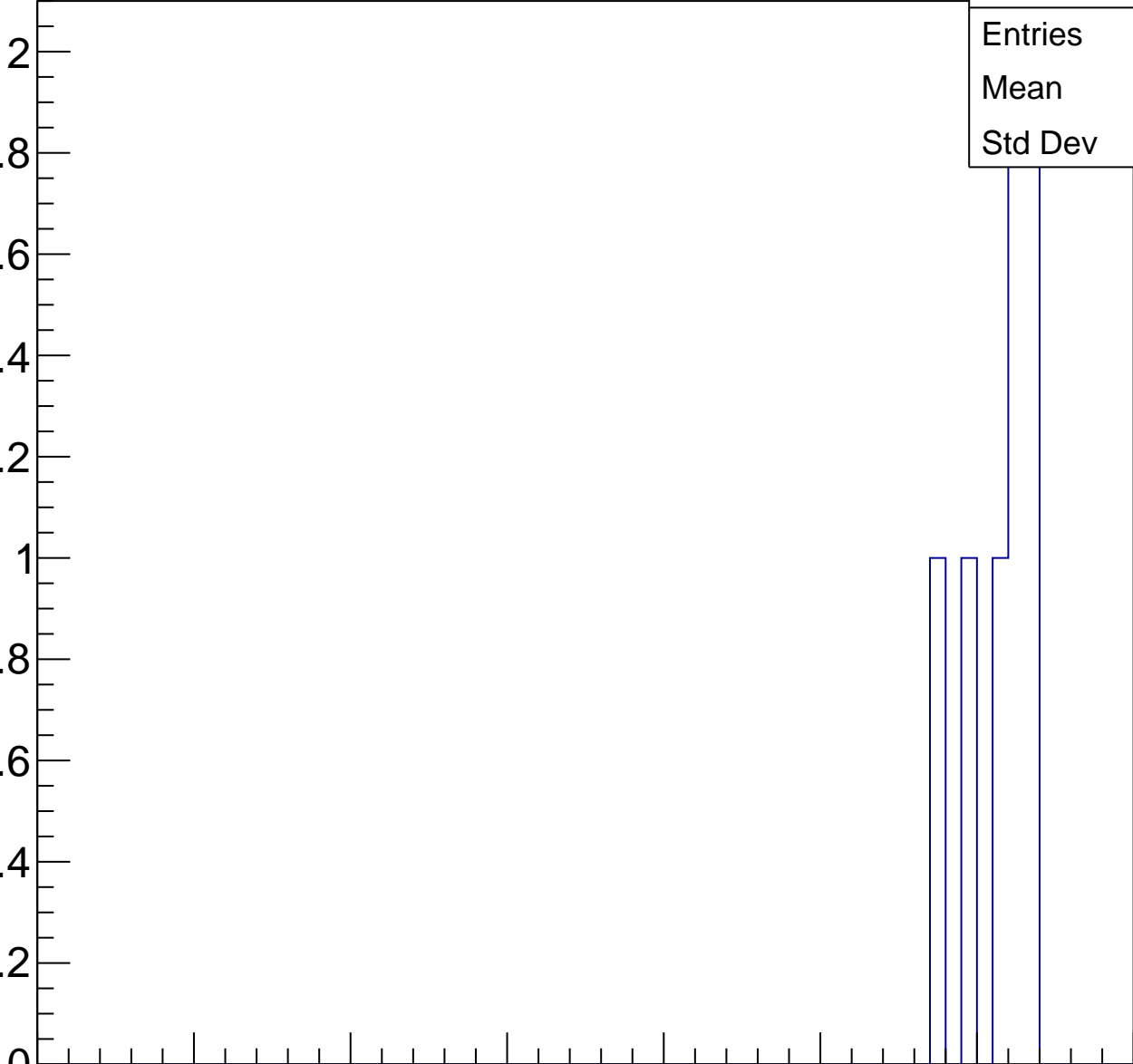
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	61
Std Dev	2.07

ampl

0 10 20 30 40 50 60 70





# B1L103S, U1-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch4, adc0

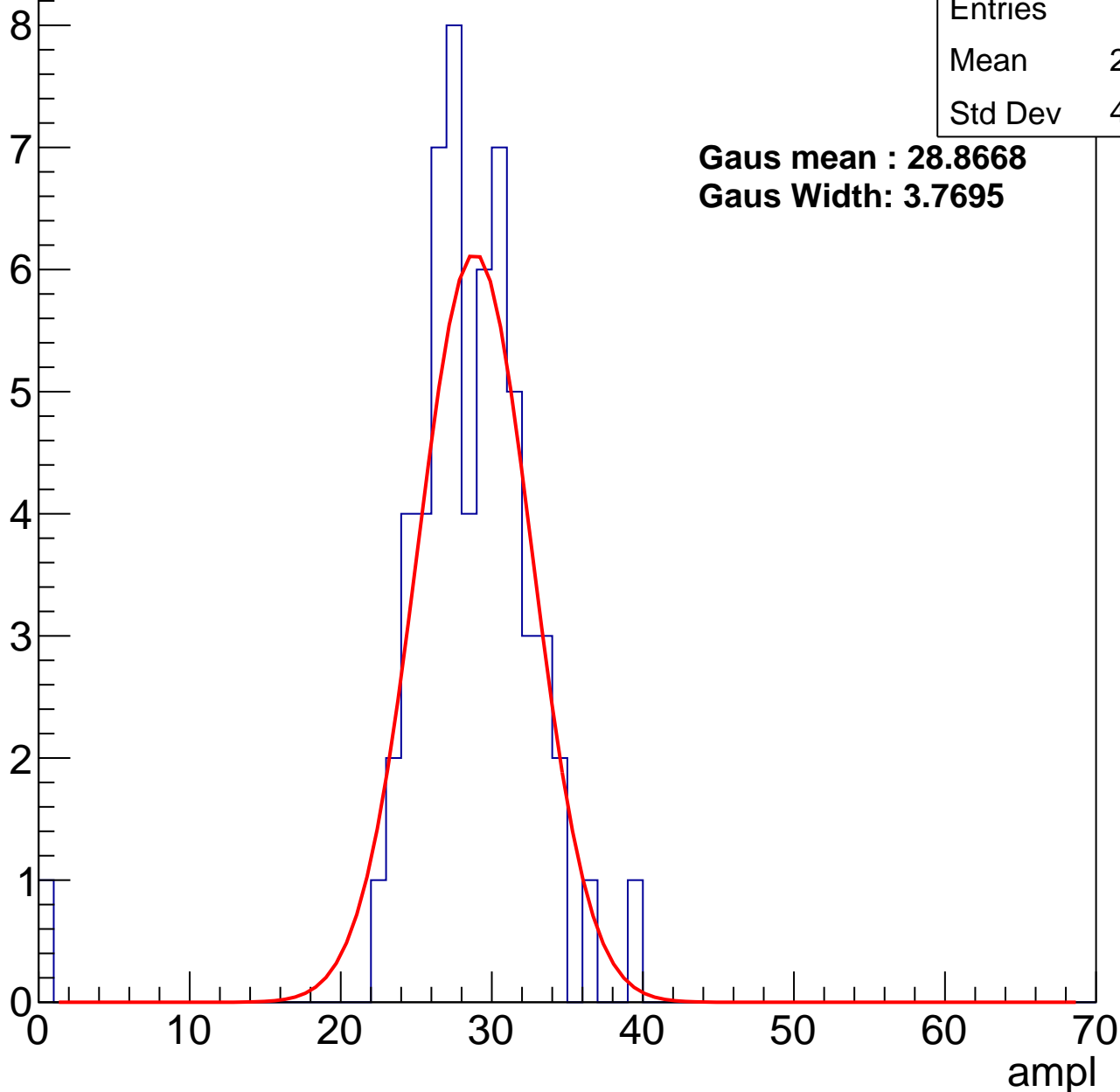
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	27.98
Std Dev	4.983

**Gaus mean : 28.8668**

**Gaus Width: 3.7695**



# B1L103S, U1-ch4, adc1

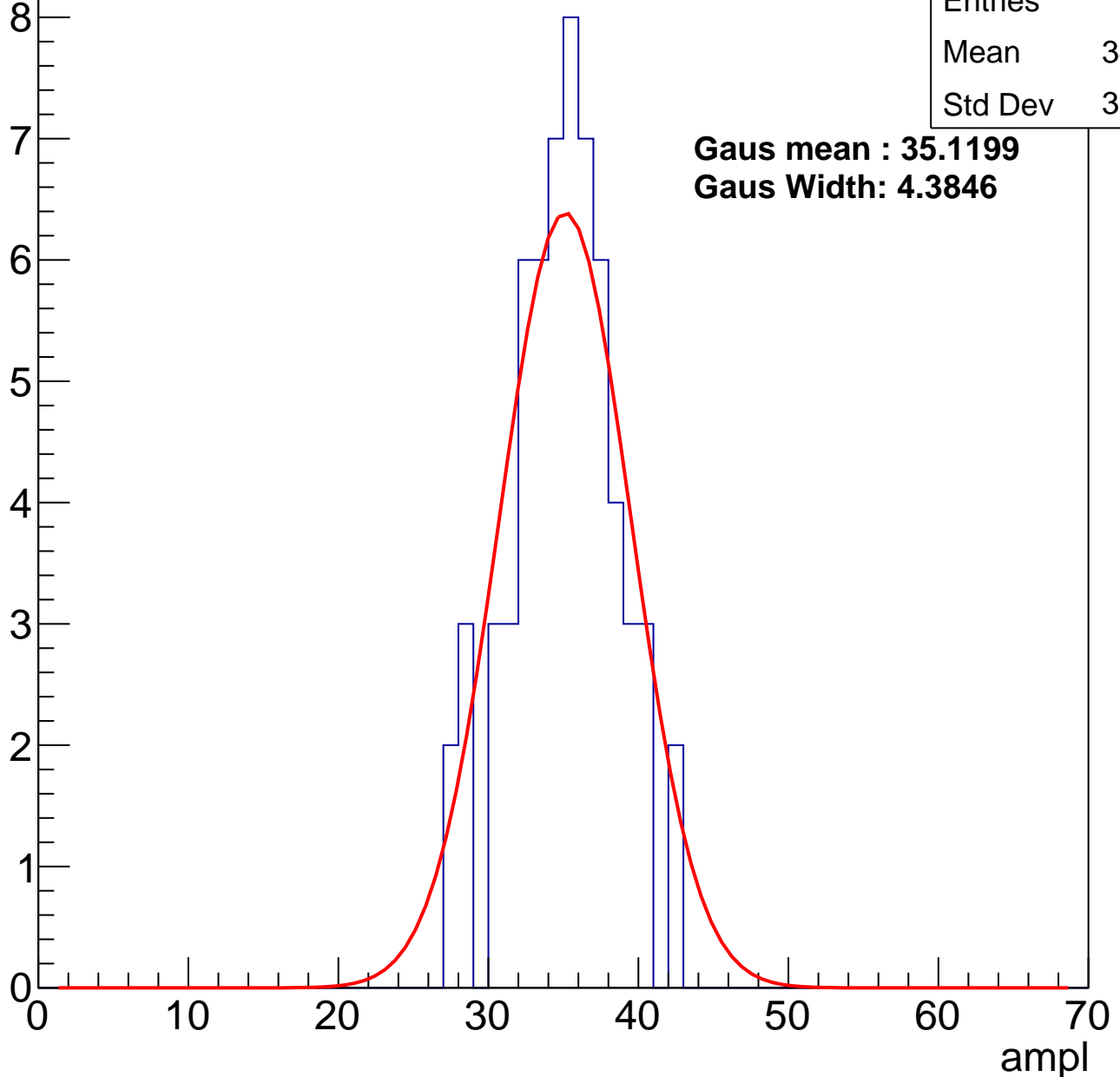
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	34.54
Std Dev	3.468

**Gaus mean : 35.1199**

**Gaus Width: 4.3846**



# B1L103S, U1-ch4, adc2

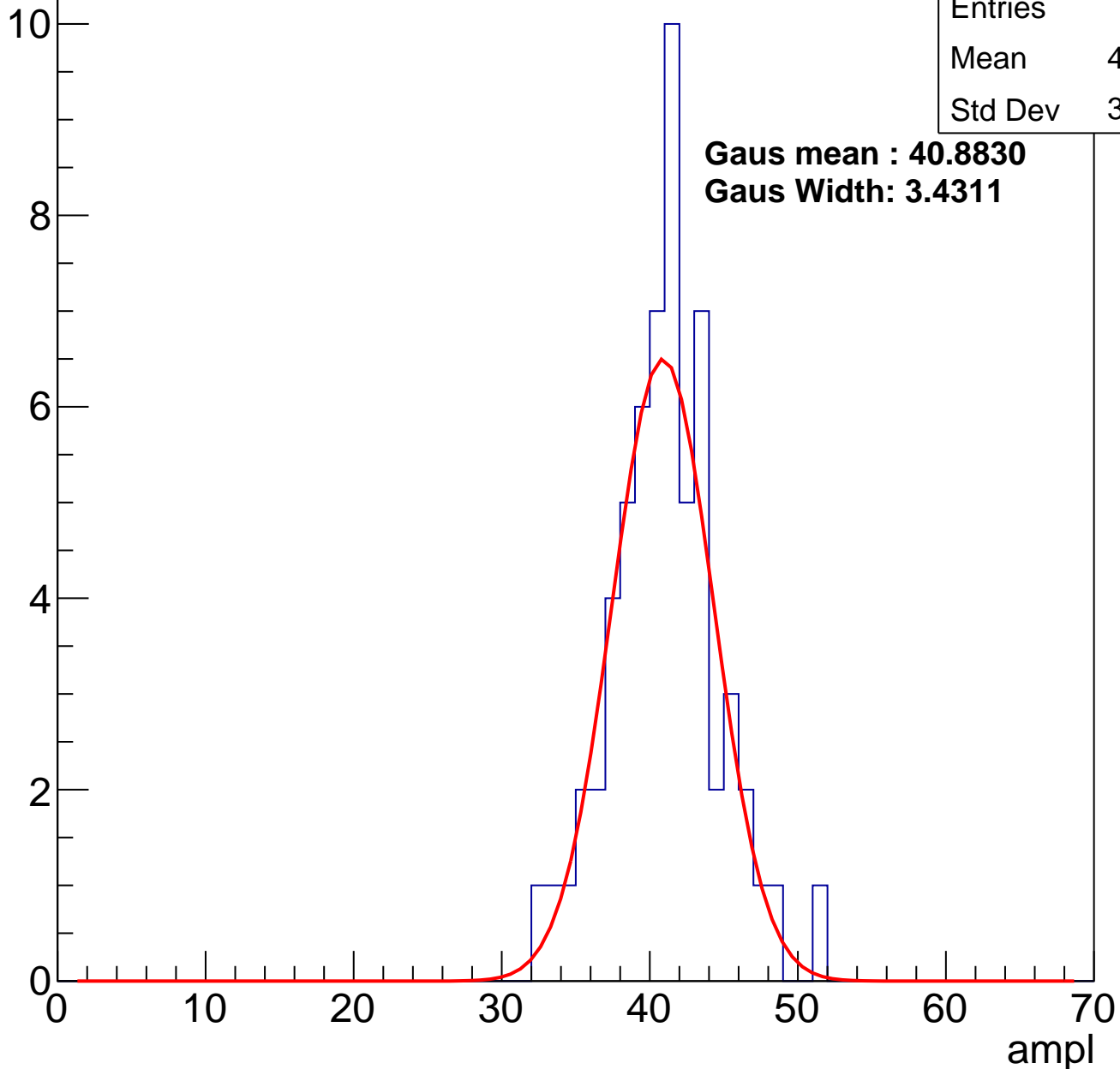
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	61
Mean	40.57
Std Dev	3.573

**Gaus mean : 40.8830**

**Gaus Width: 3.4311**

Entry

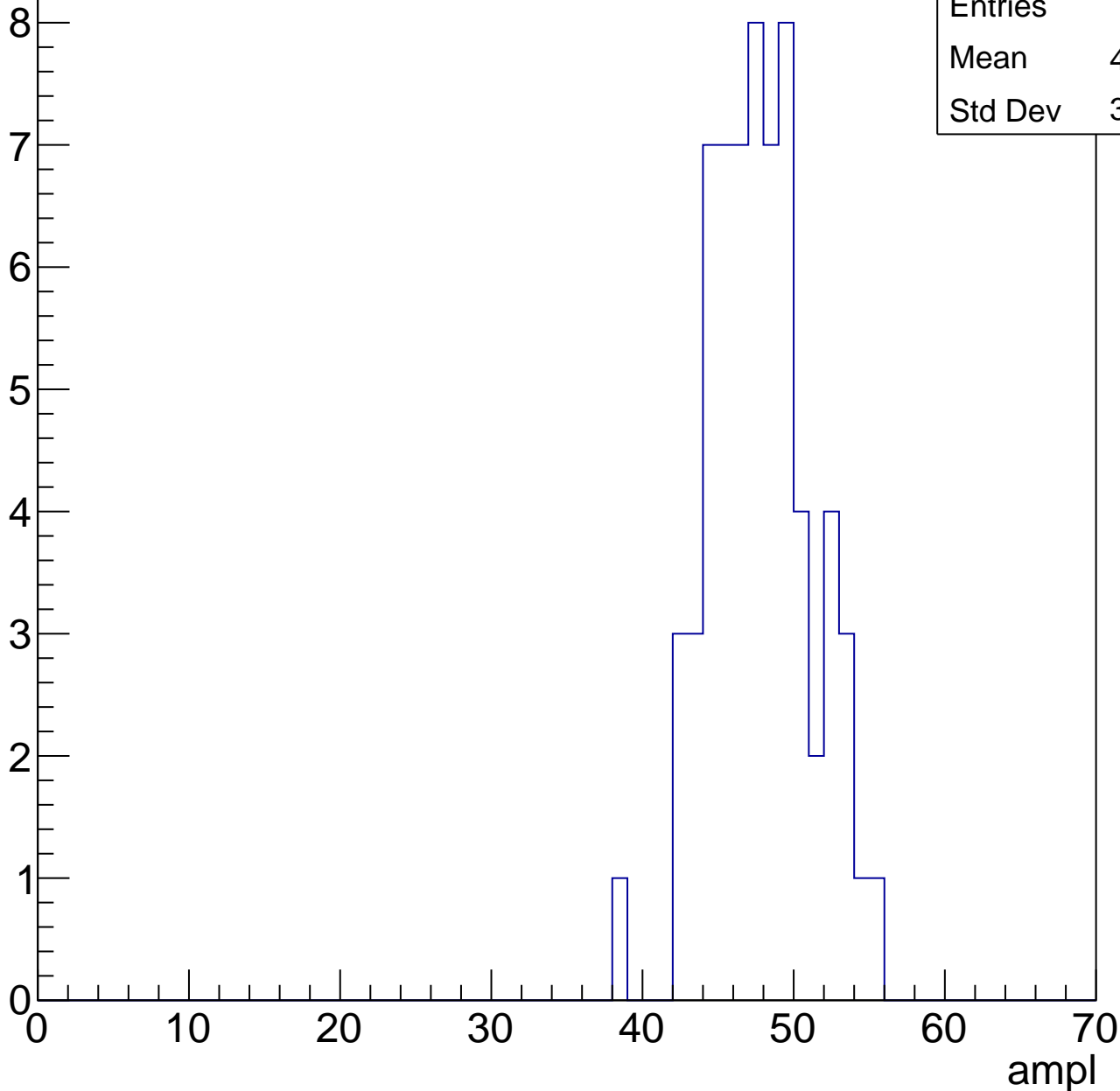


# B1L103S, U1-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	47.27
Std Dev	3.315

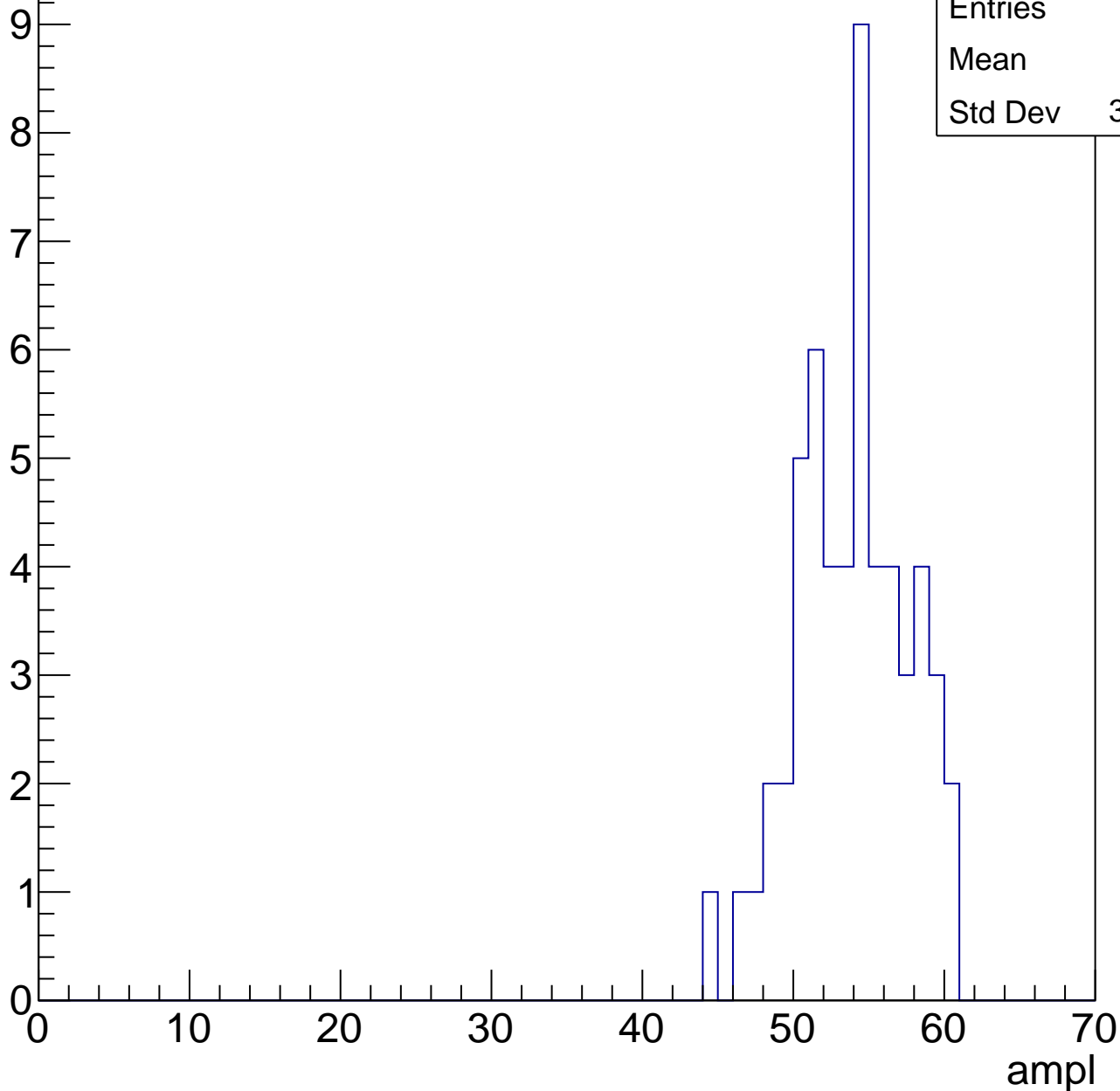


# B1L103S, U1-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	53.4
Std Dev	3.636



# B1L103S, U1-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	62
Mean	57.24
Std Dev	7.928

Entry

10

8

6

4

2

0

0

10

20

30

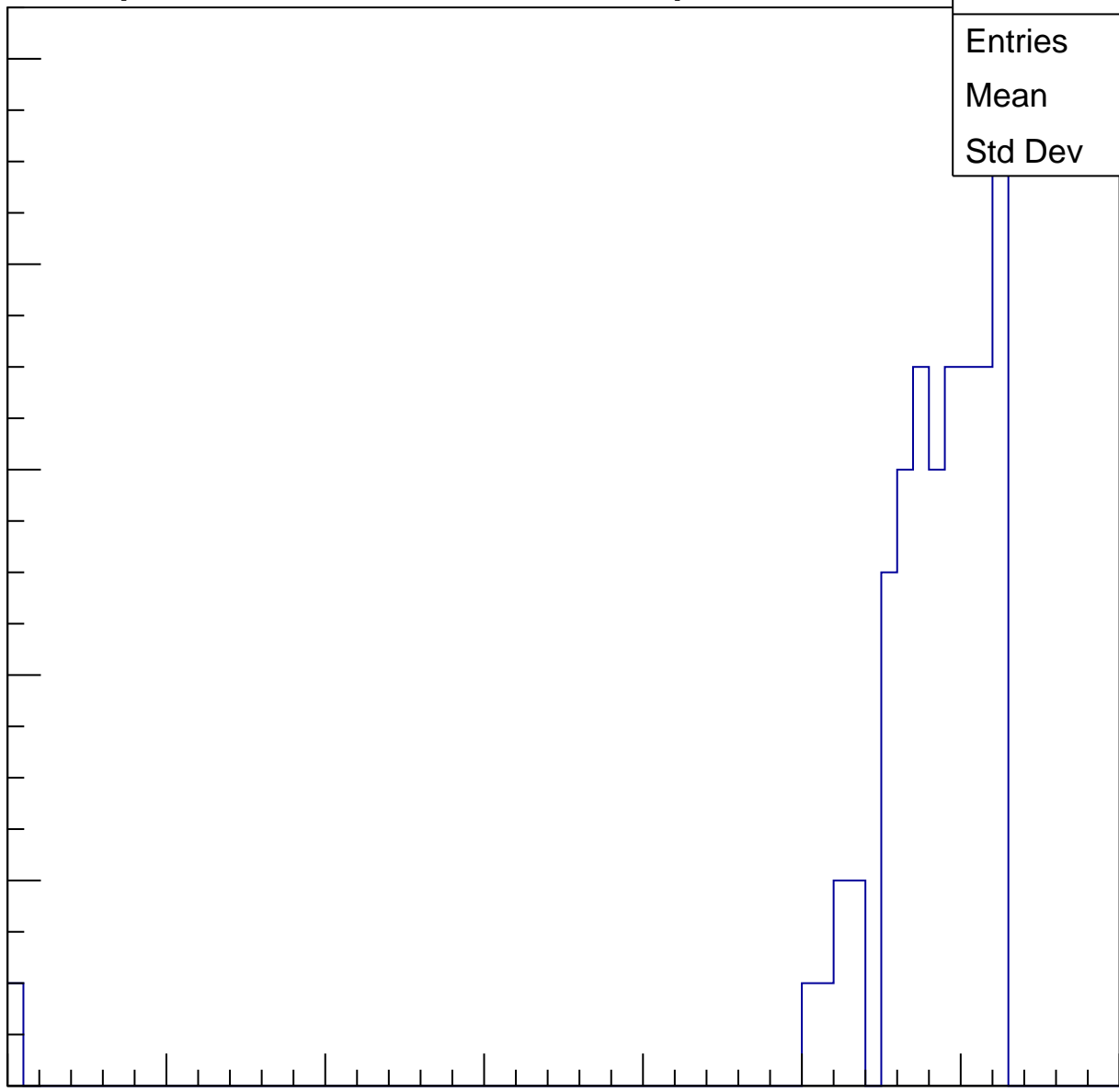
40

50

60

70

ampl

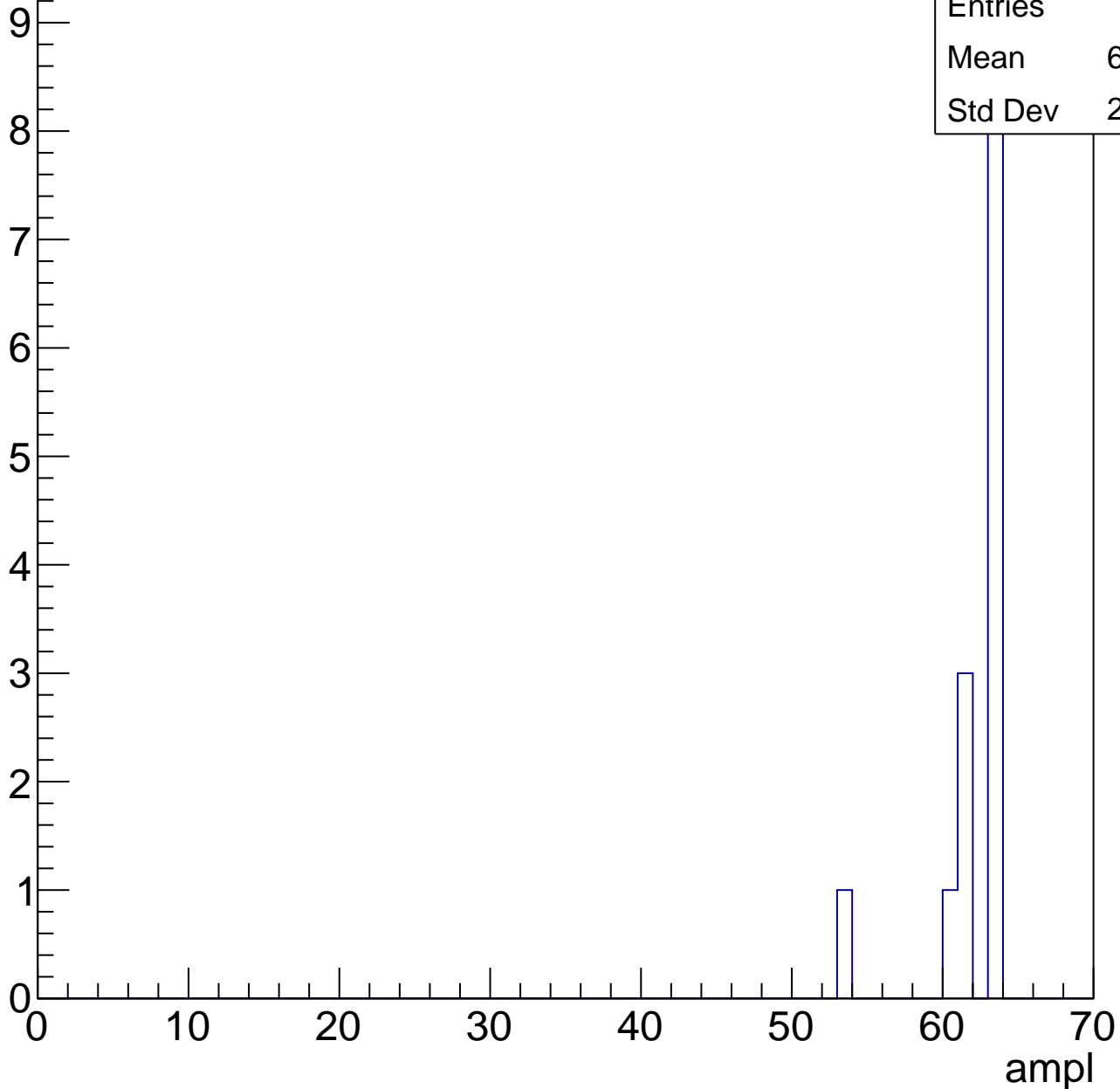


# B1L103S, U1-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	14
Mean	61.64
Std Dev	2.608

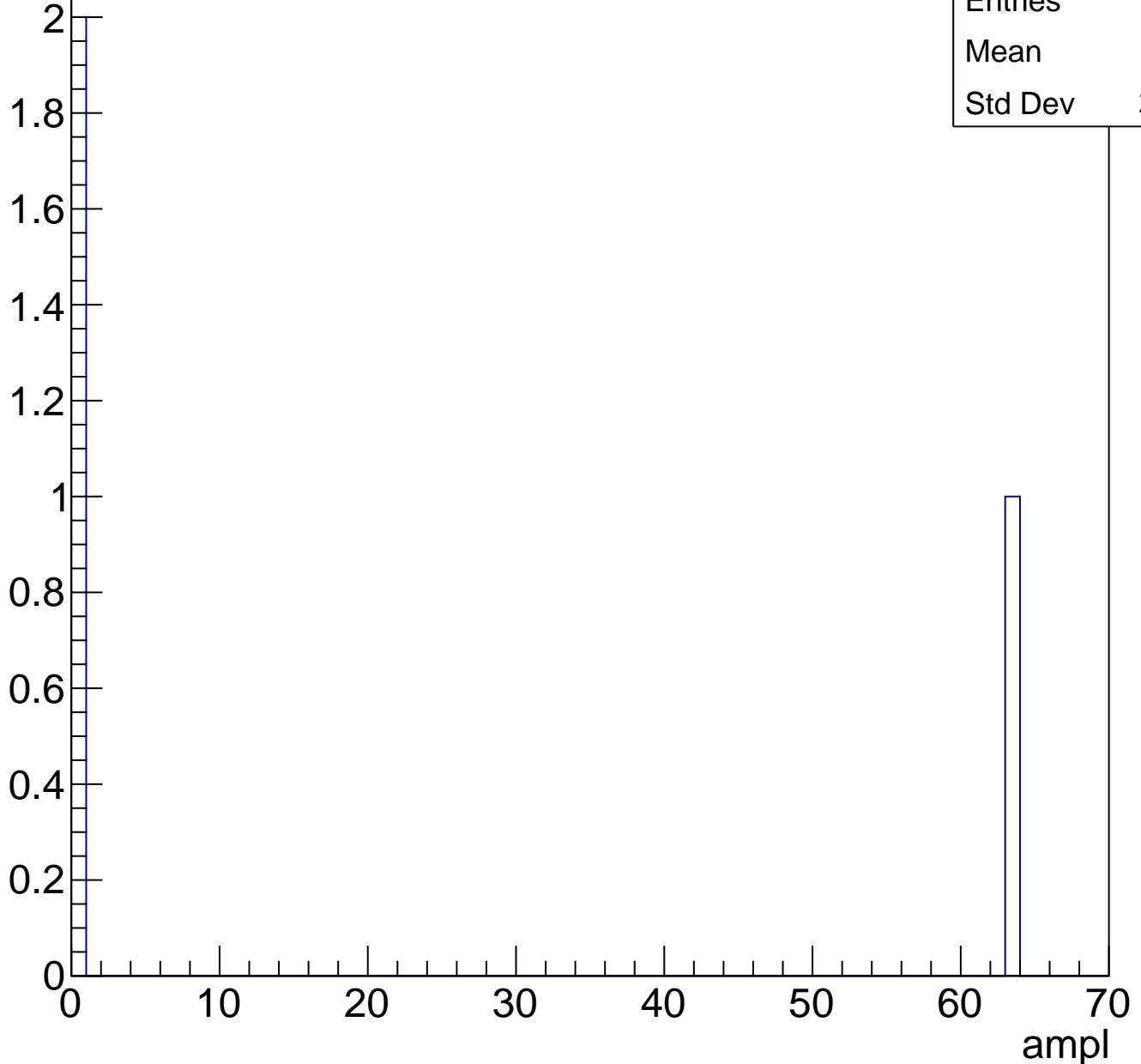




# B1L103S, U1-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L103S, U1-ch5, adc0

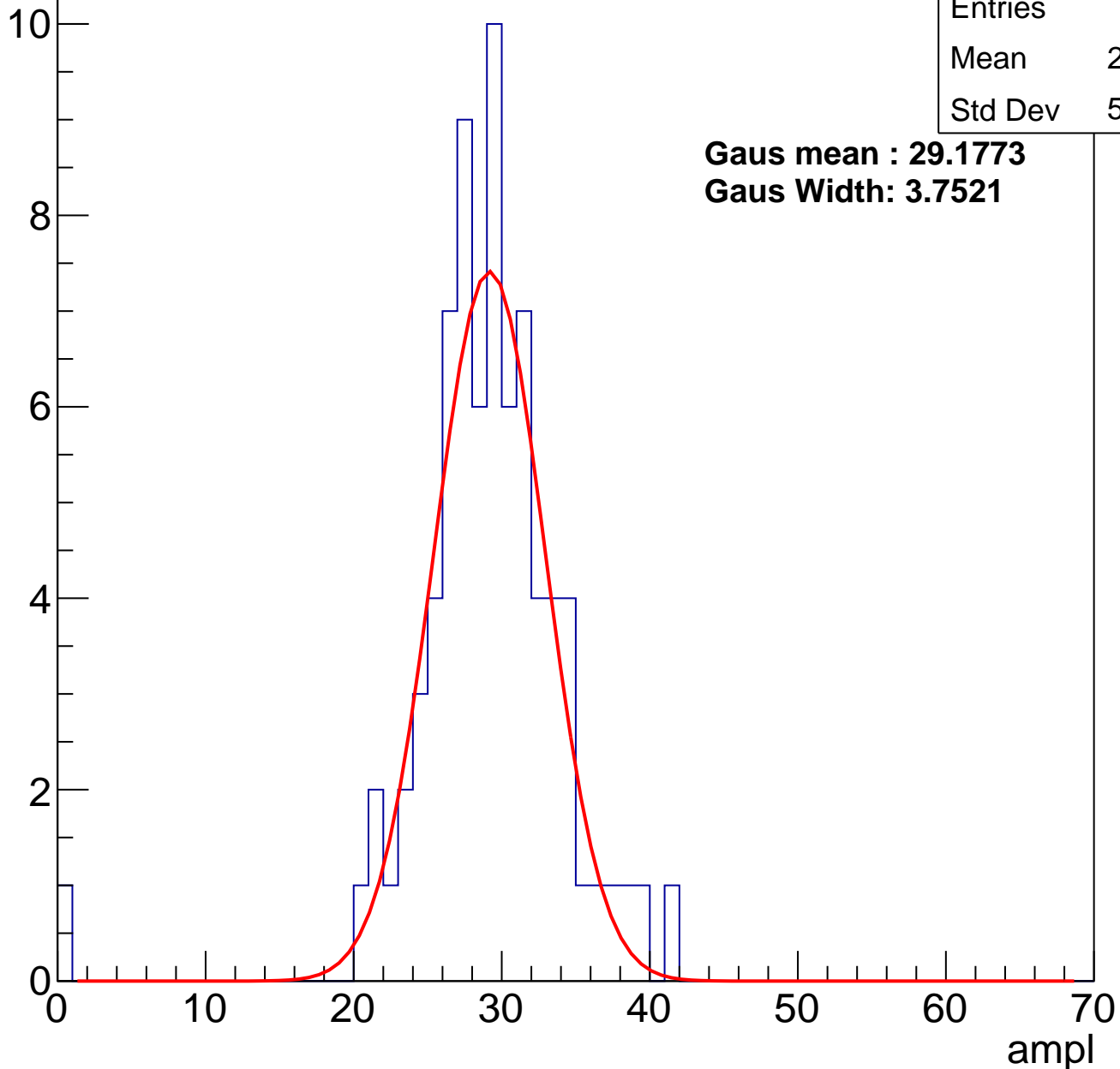
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	77
Mean	28.62
Std Dev	5.237

**Gaus mean : 29.1773**

**Gaus Width: 3.7521**

Entry



# B1L103S, U1-ch5, adc1

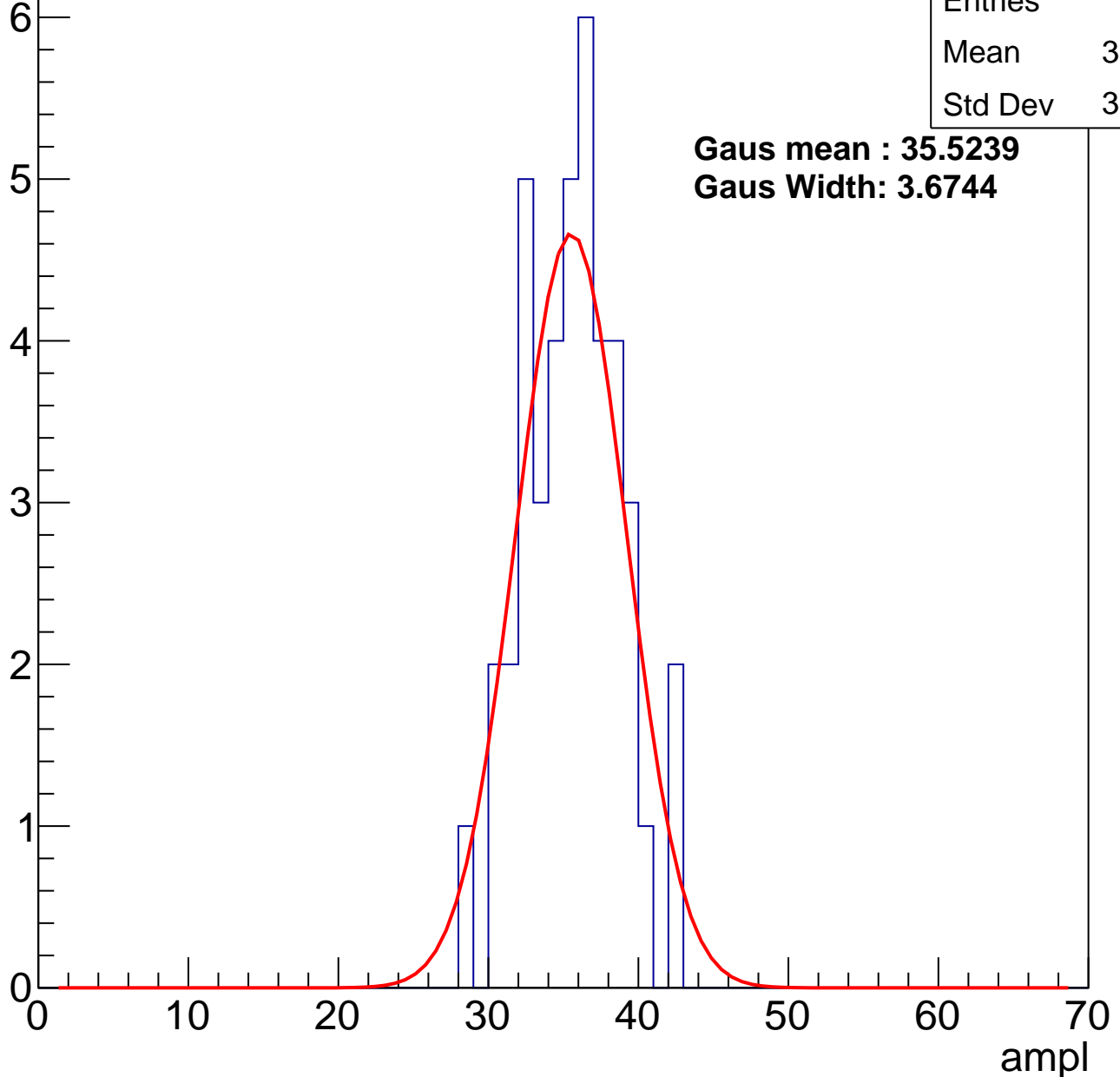
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	42
Mean	35.17
Std Dev	3.162

**Gaus mean : 35.5239**

**Gaus Width: 3.6744**



# B1L103S, U1-ch5, adc2

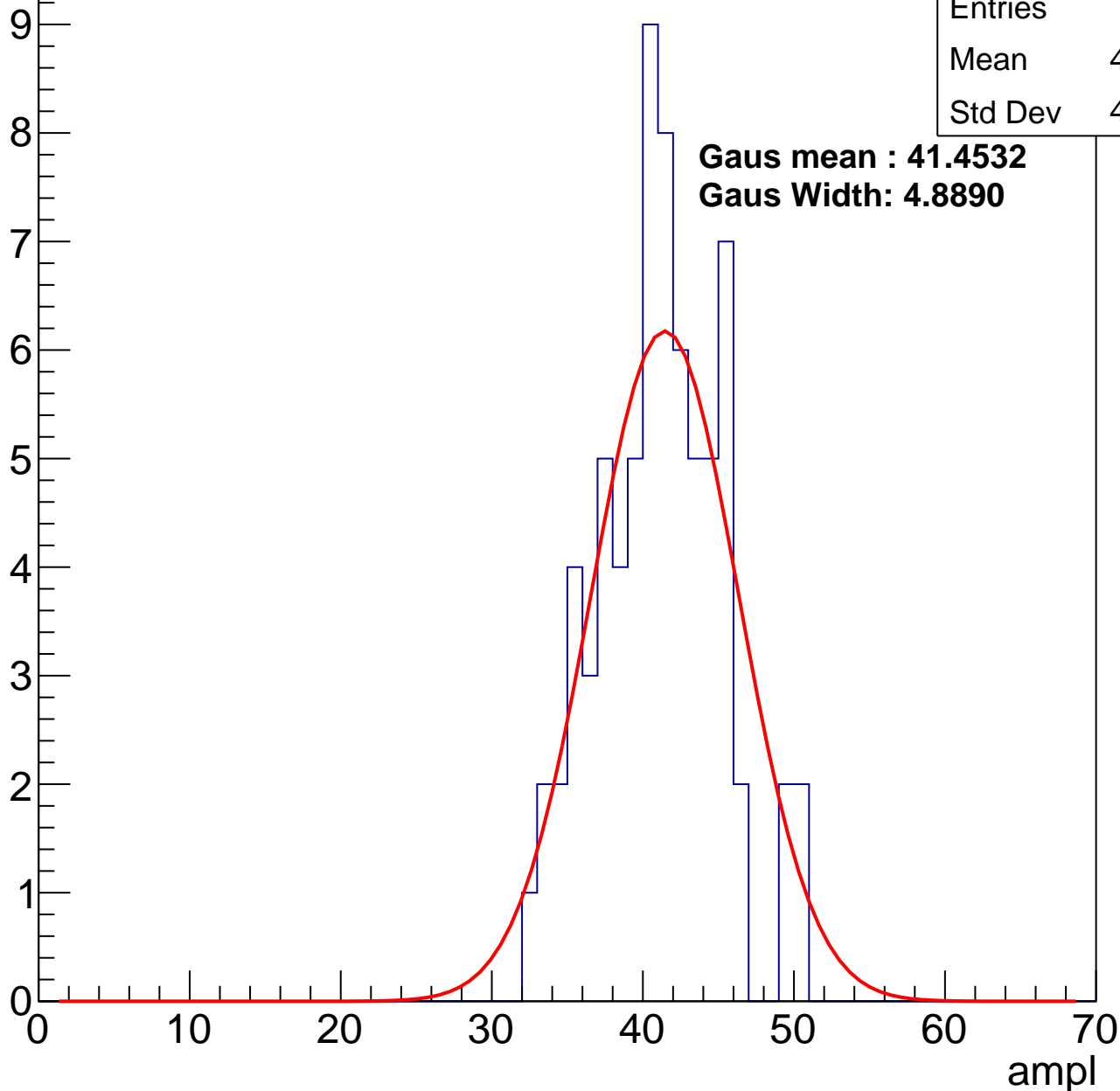
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	40.64
Std Dev	4.056

**Gaus mean : 41.4532**

**Gaus Width: 4.8890**

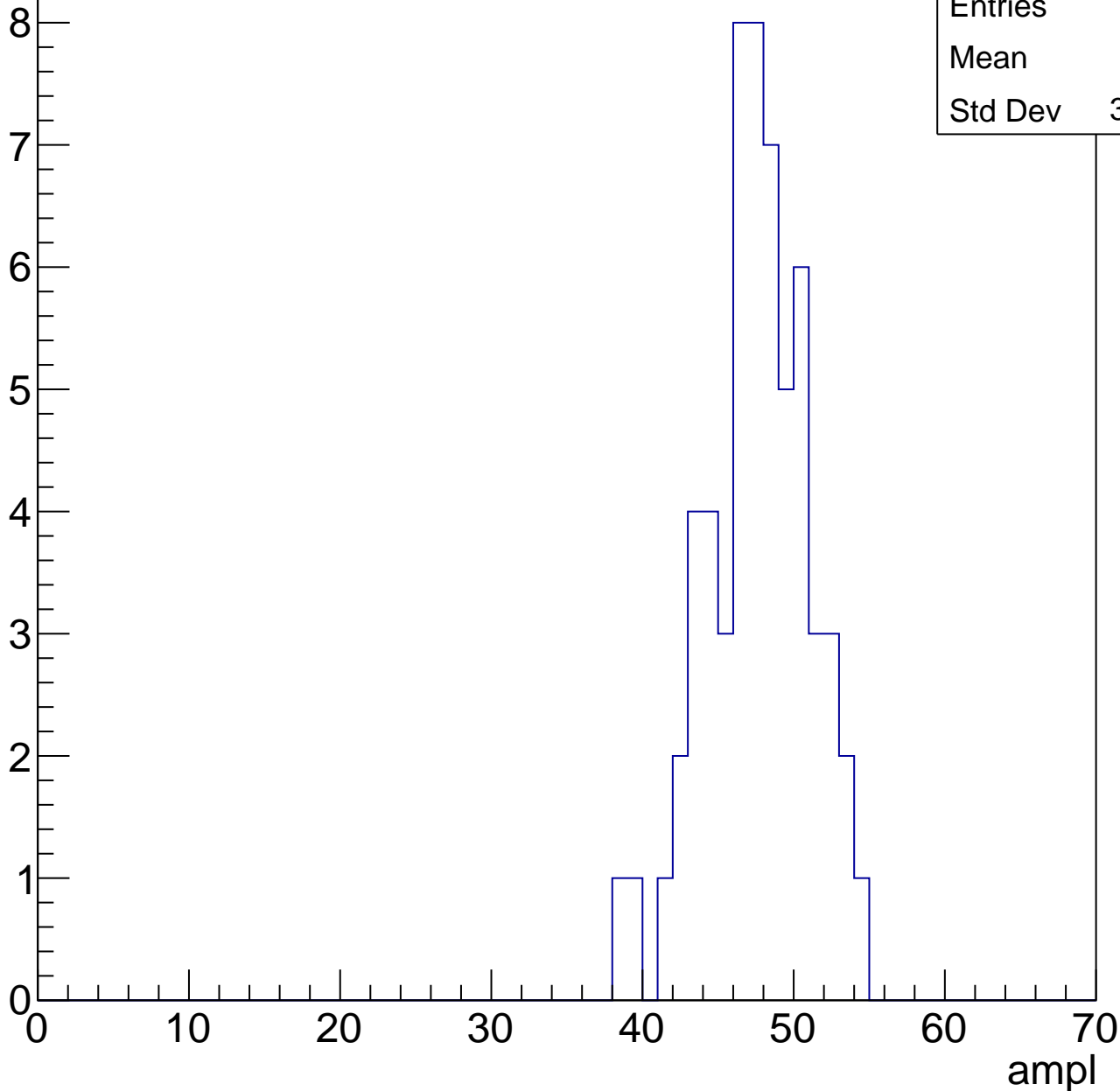


# B1L103S, U1-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	47.1
Std Dev	3.383

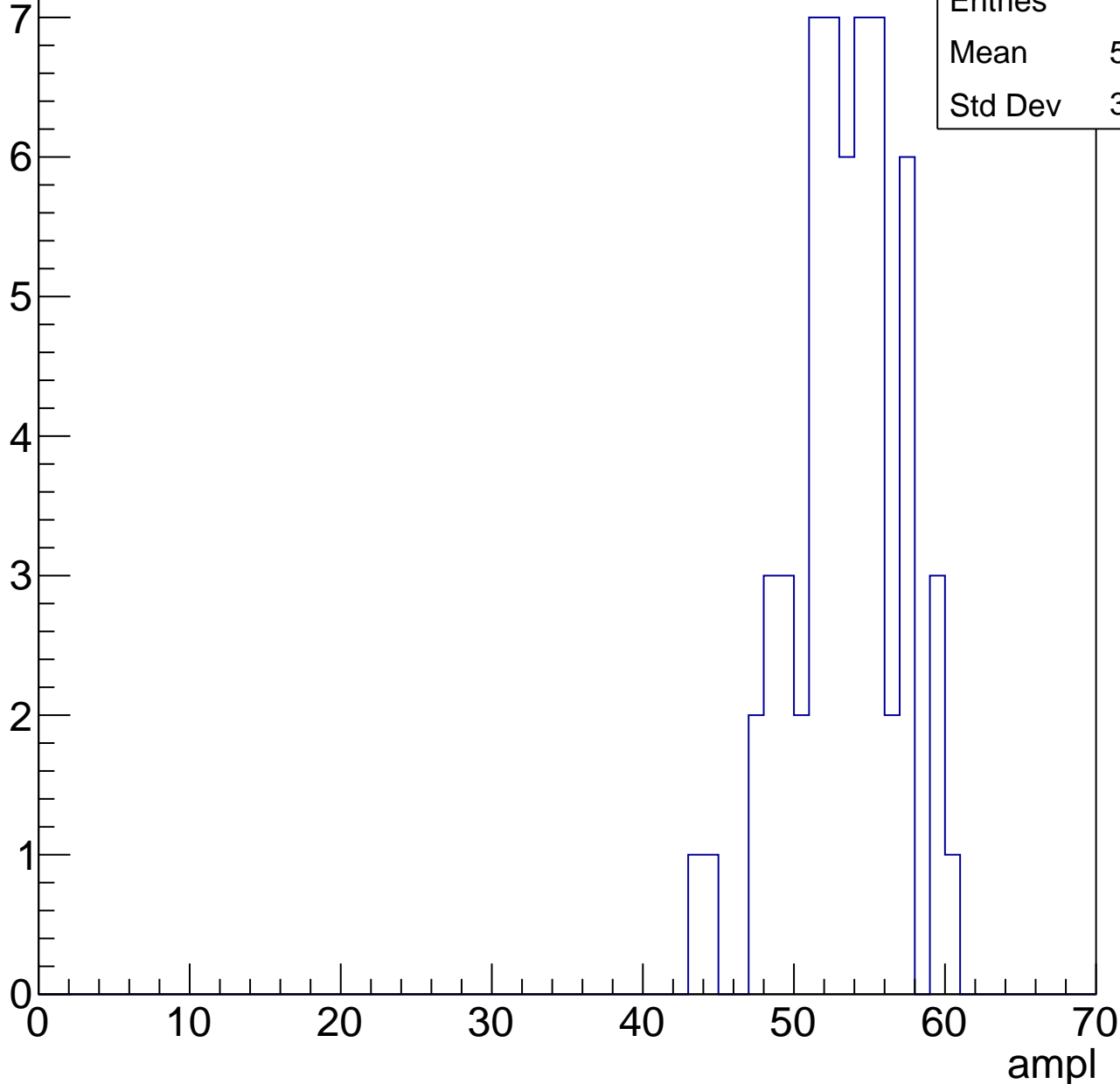


# B1L103S, U1-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

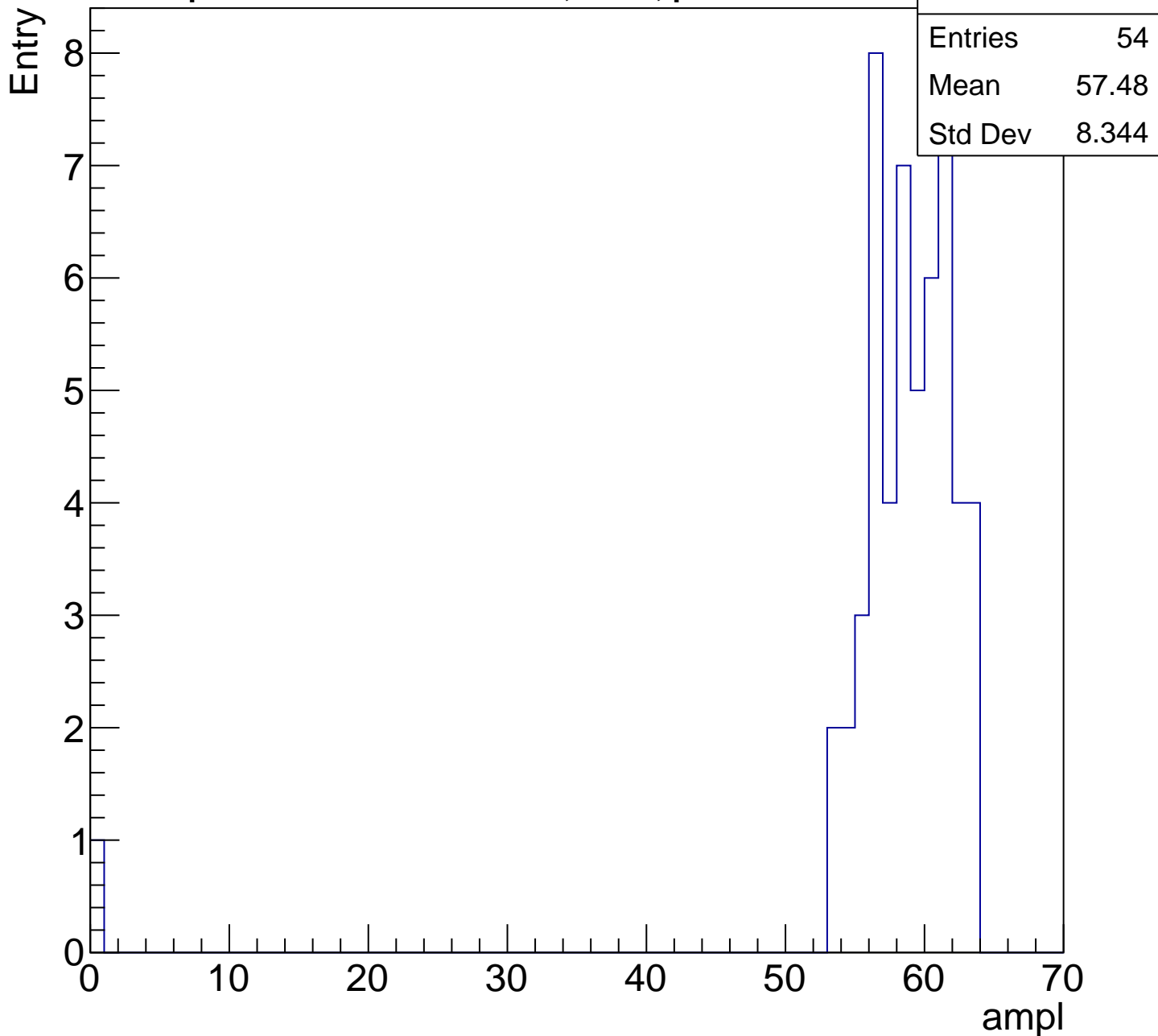
Entry

Entries	58
Mean	52.84
Std Dev	3.556



# B1L103S, U1-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

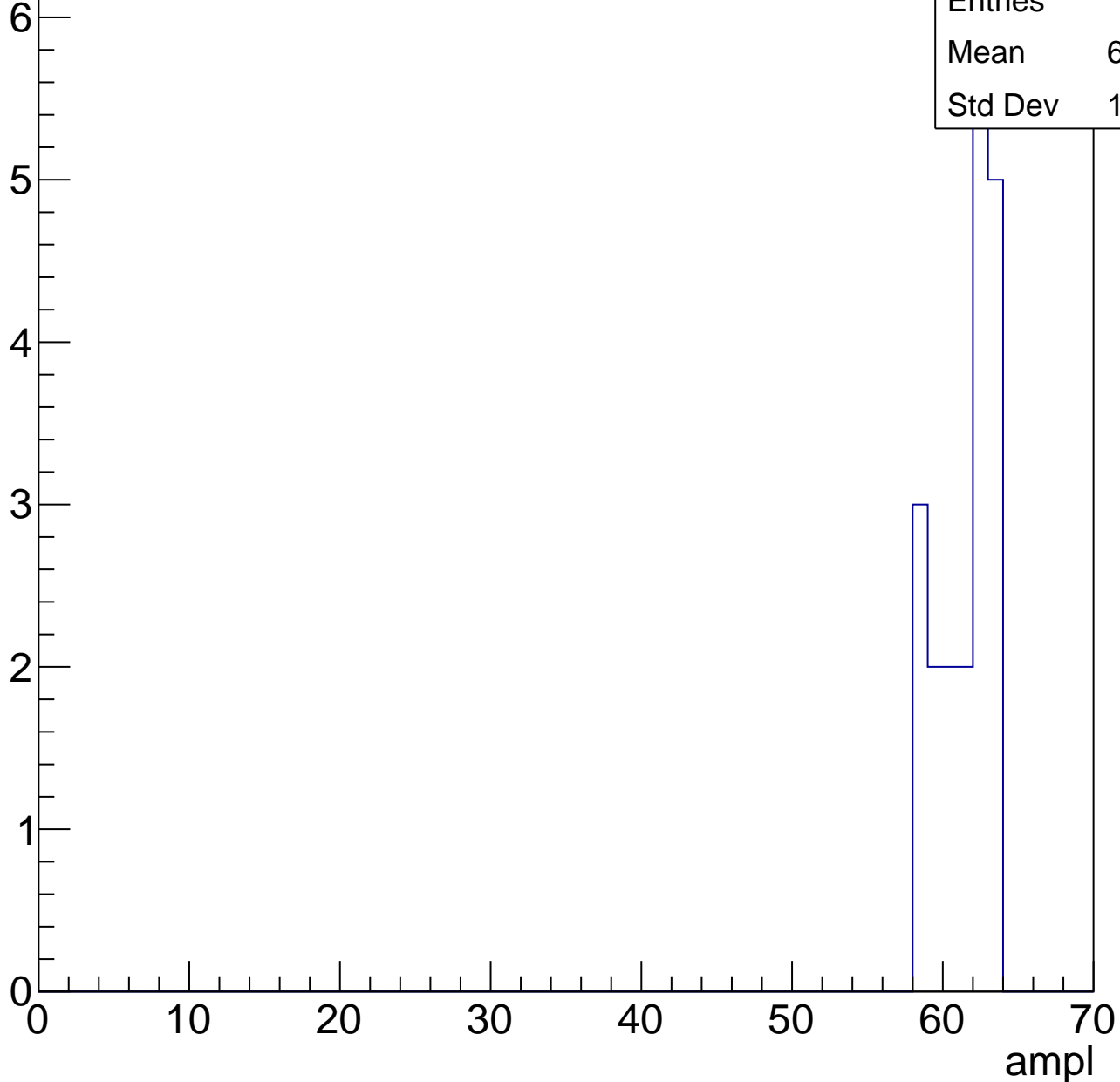


# B1L103S, U1-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	20
Mean	61.05
Std Dev	1.774

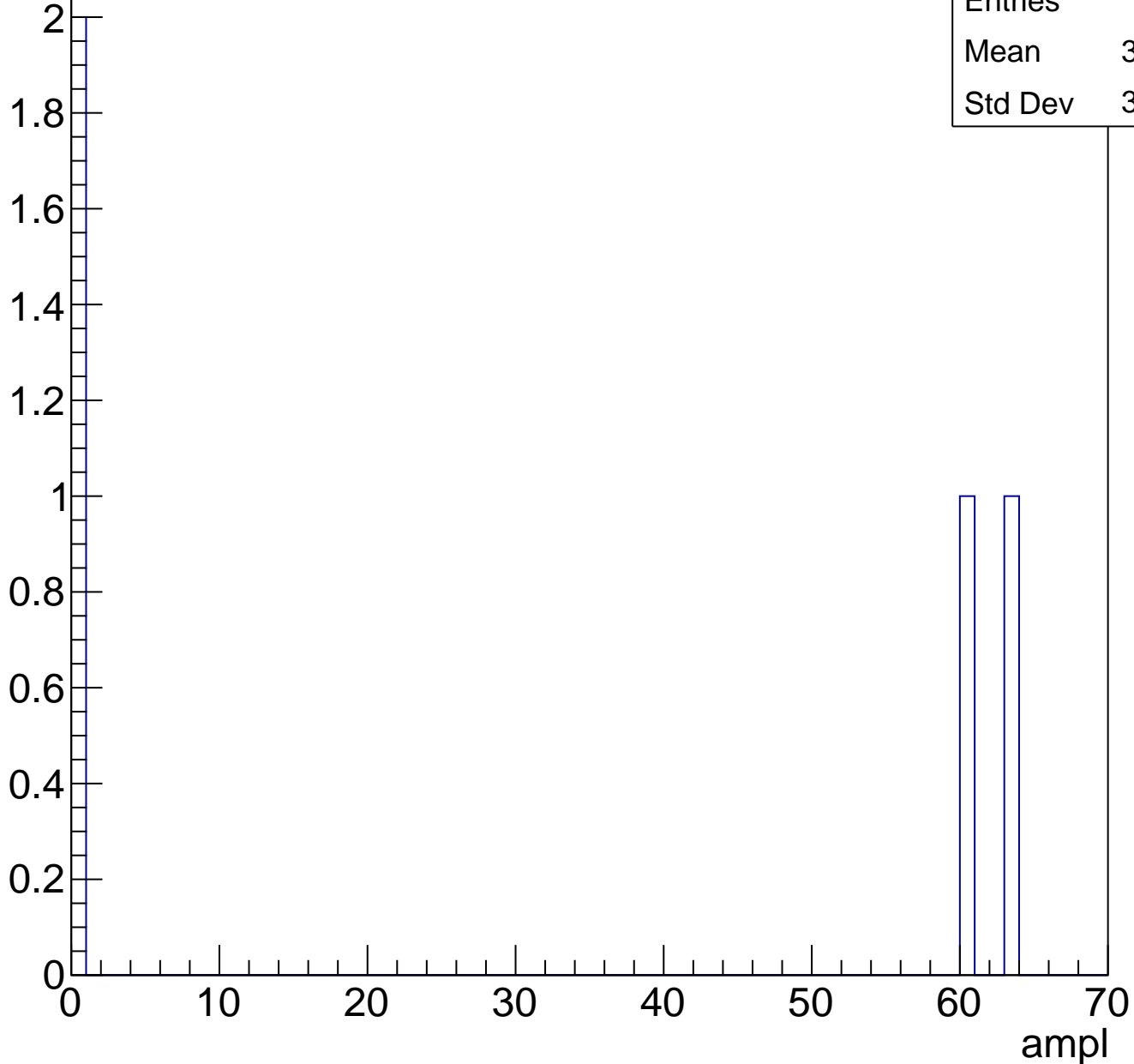




# B1L103S, U1-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	4
Mean	30.75
Std Dev	30.77

# B1L103S, U1-ch6, adc0

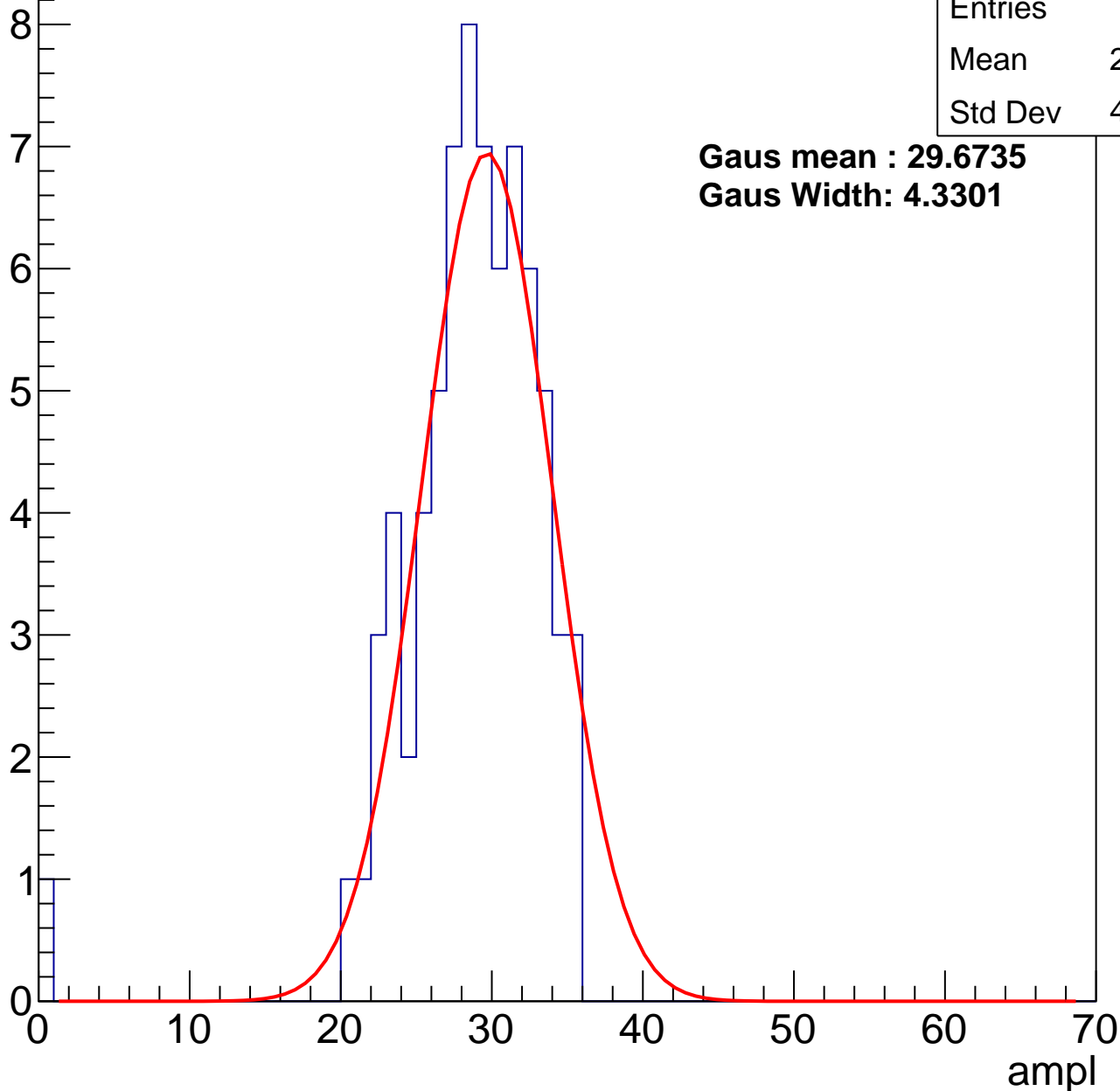
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	28.14
Std Dev	4.922

**Gaus mean : 29.6735**

**Gaus Width: 4.3301**



# B1L103S, U1-ch6, adc1

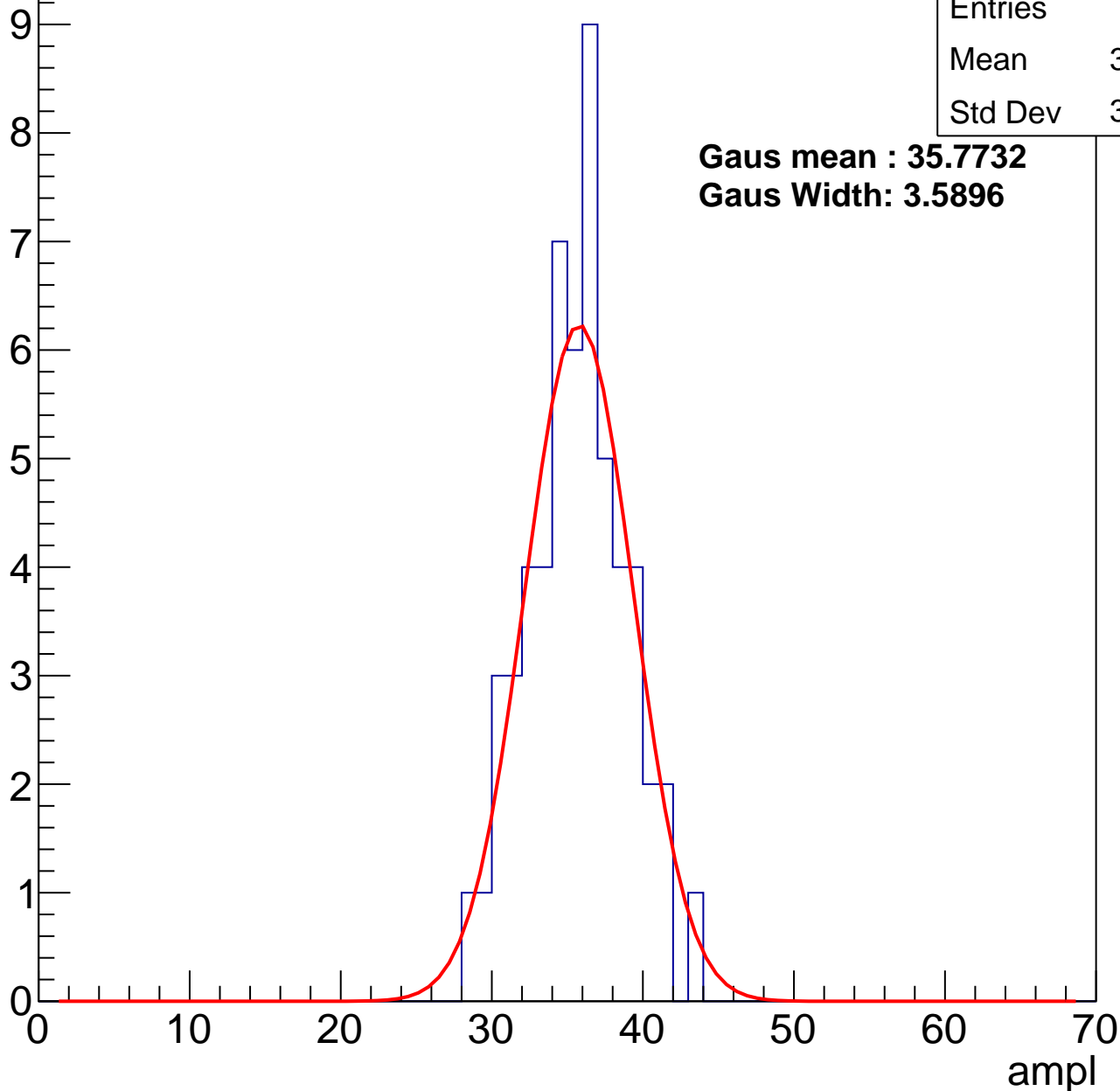
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	35.18
Std Dev	3.219

**Gaus mean : 35.7732**

**Gaus Width: 3.5896**



# B1L103S, U1-ch6, adc2

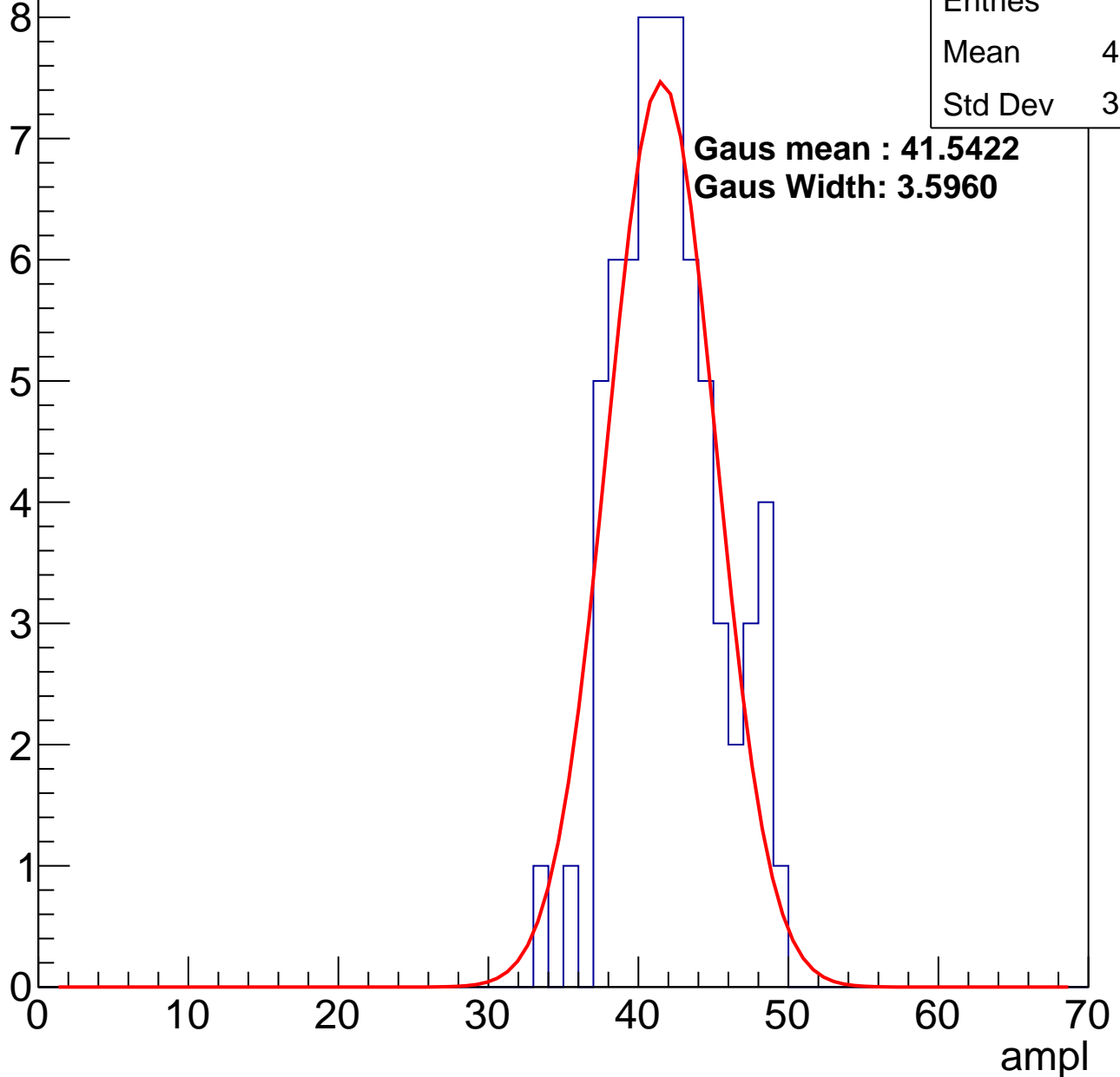
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	41.58
Std Dev	3.426

**Gaus mean : 41.5422**

**Gaus Width: 3.5960**

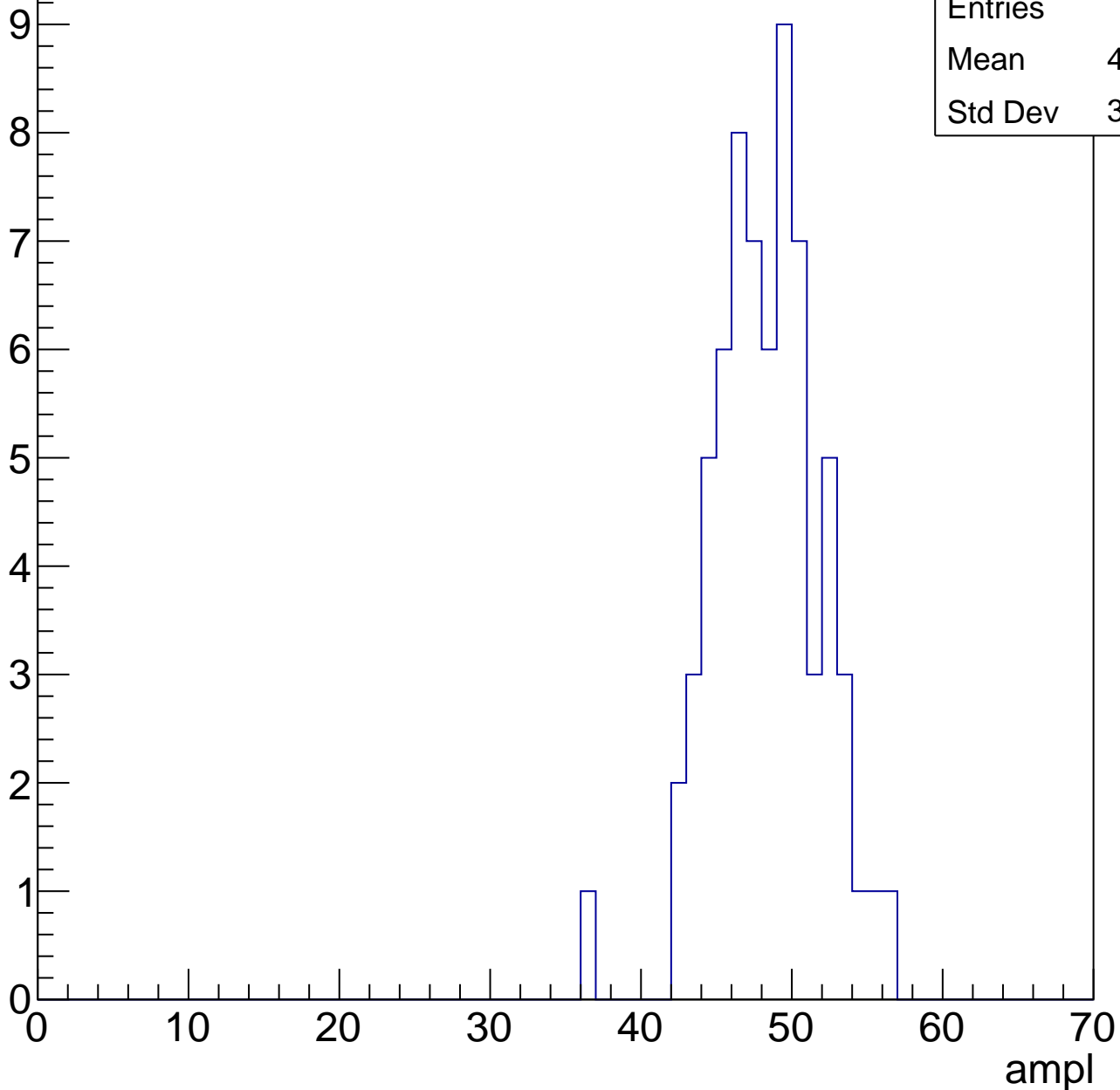


# B1L103S, U1-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

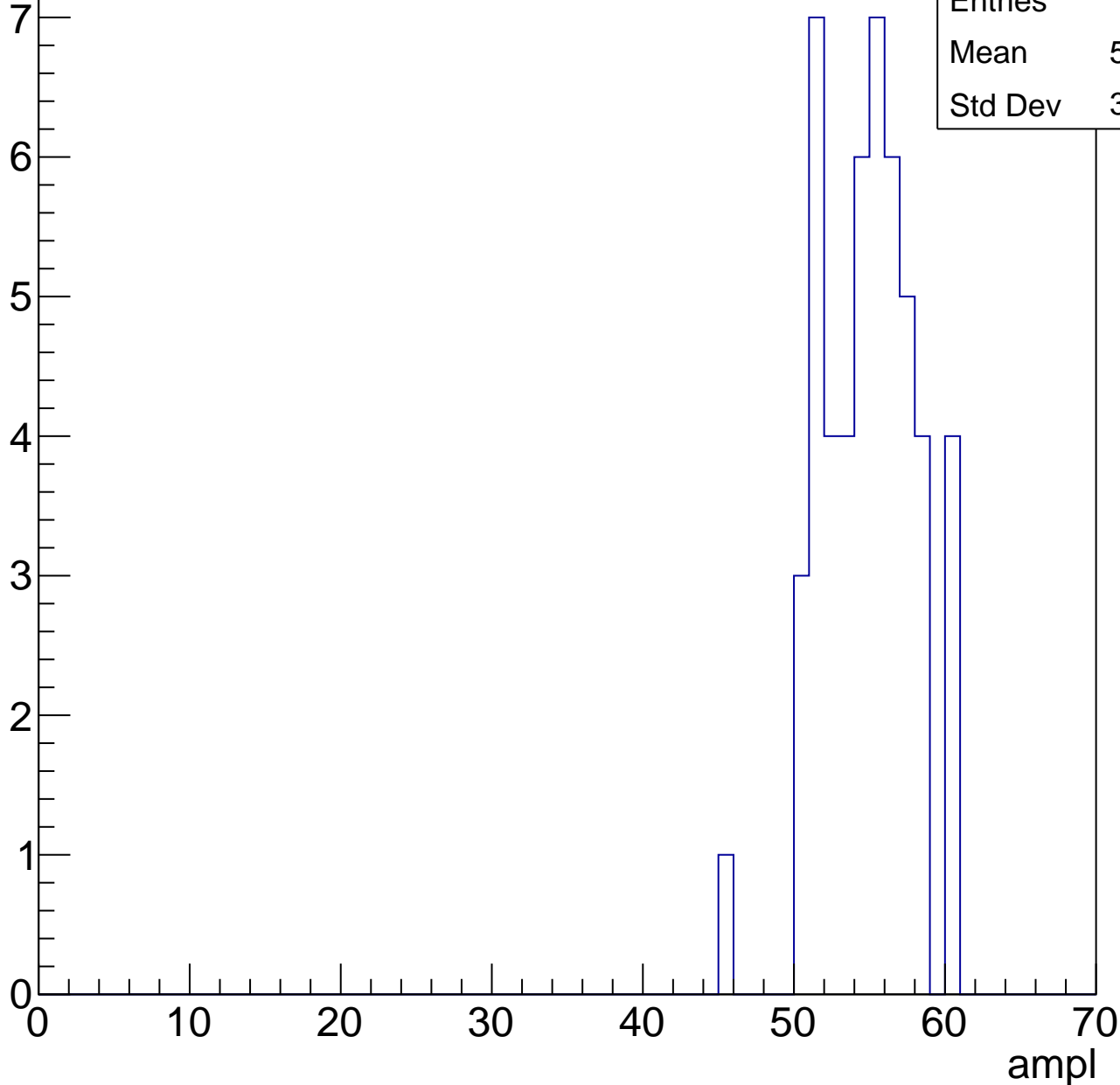
Entries	68
Mean	47.82
Std Dev	3.493



# B1L103S, U1-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

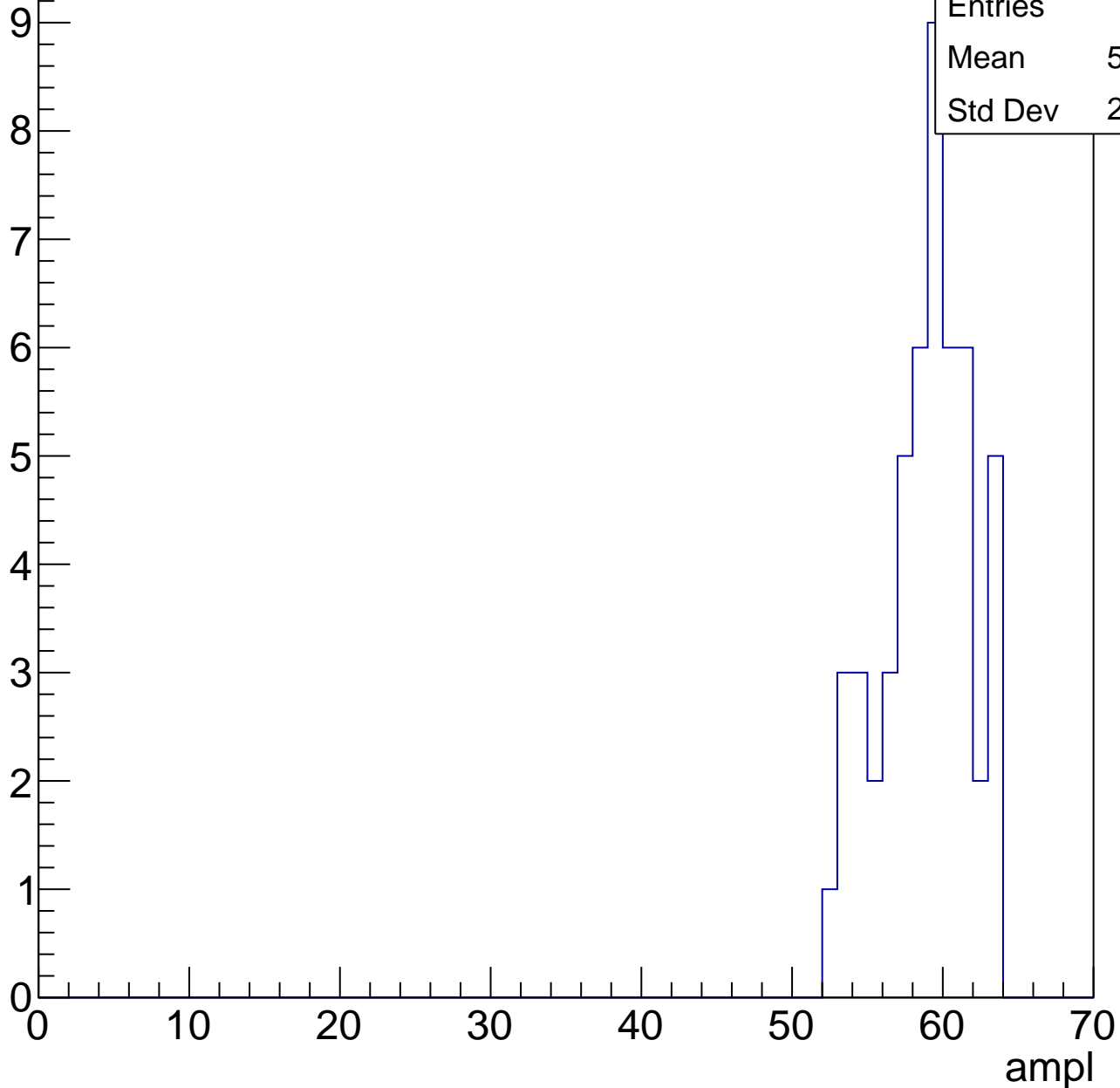


Entries	51
Mean	54.39
Std Dev	3.094

# B1L103S, U1-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



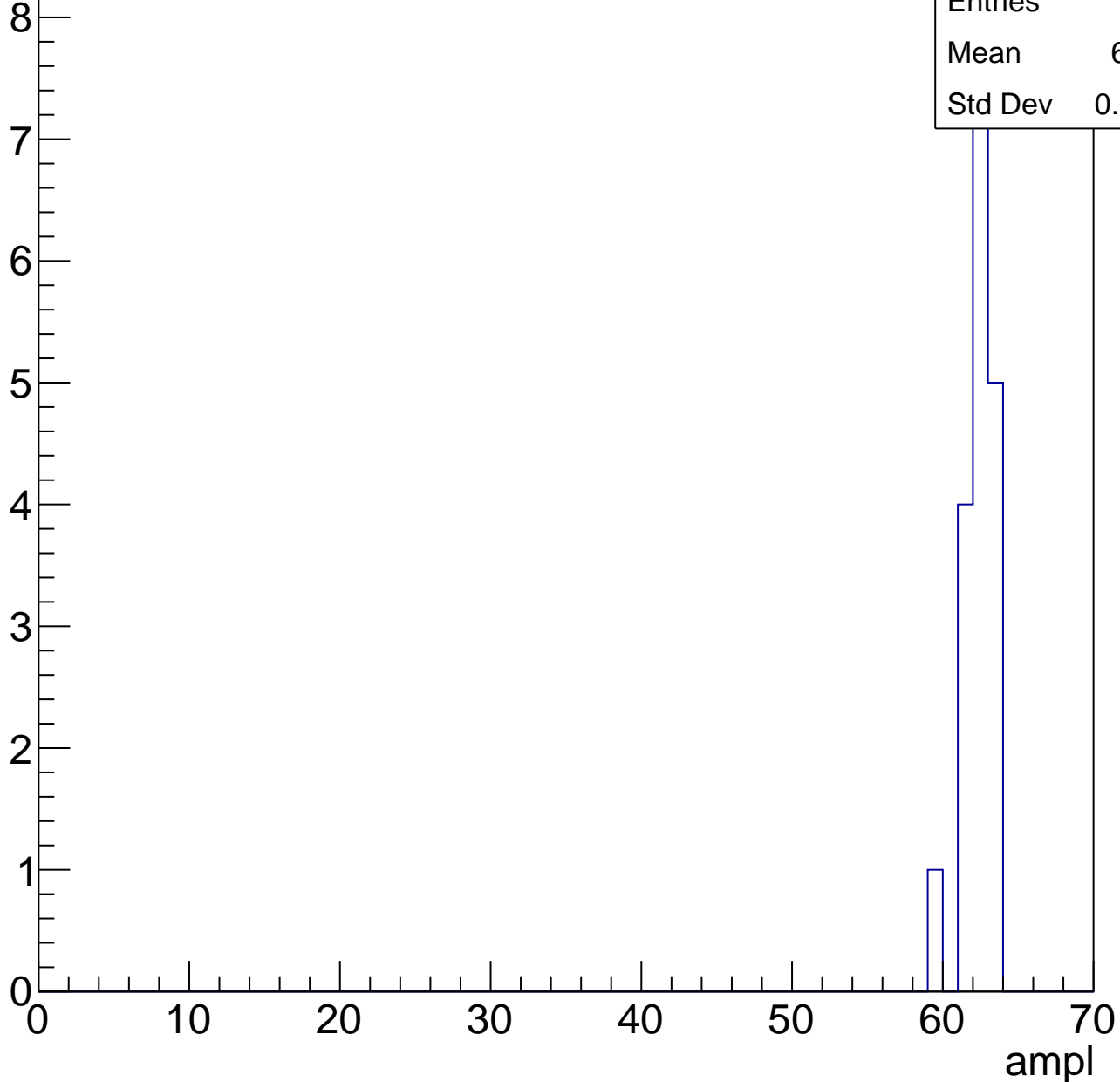
Entries	51
Mean	58.43
Std Dev	2.899

# B1L103S, U1-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	18
Mean	61.89
Std Dev	0.9938





# B1L103S, U1-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch7, adc0

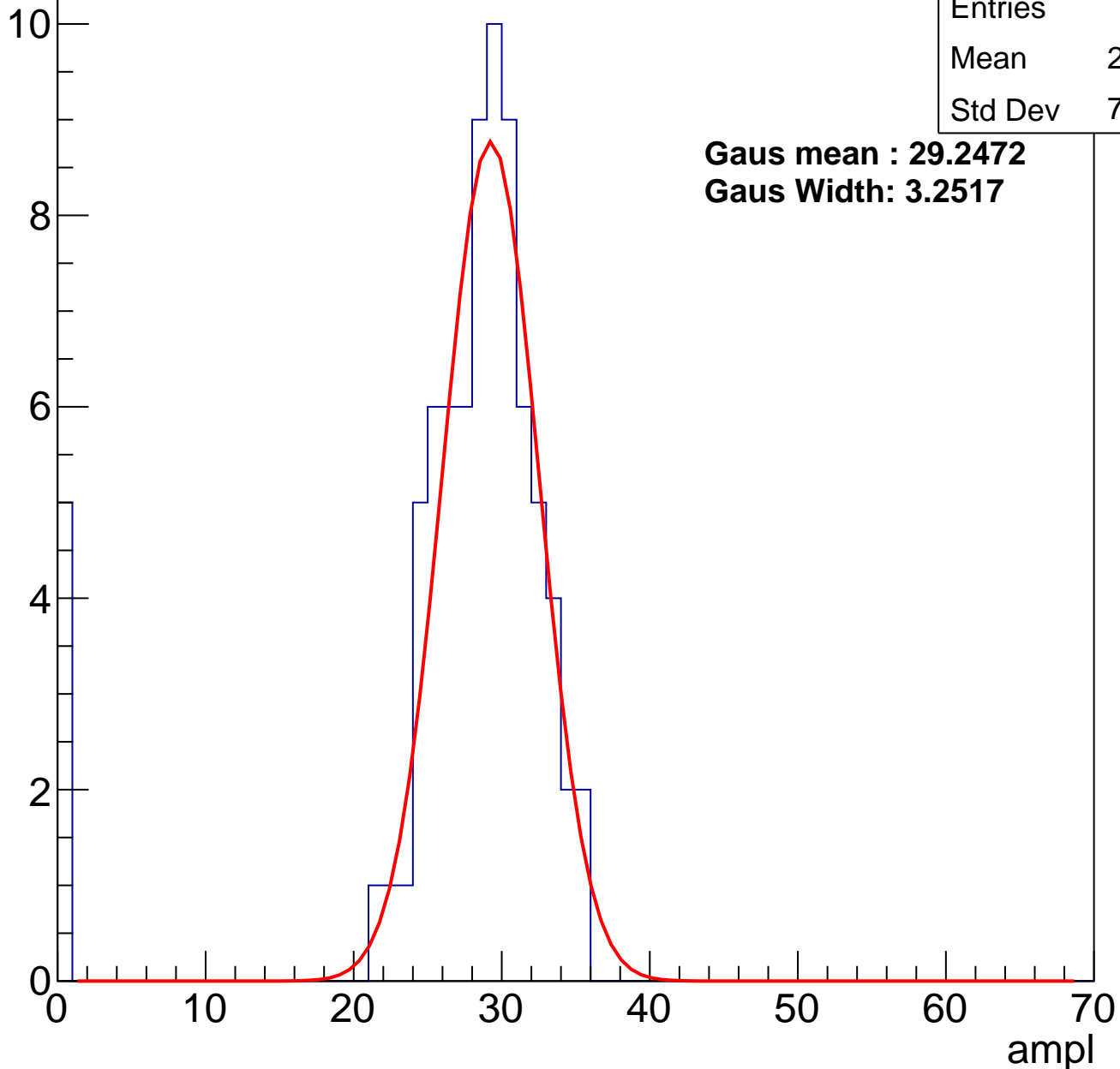
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	78
Mean	26.69
Std Dev	7.604

**Gaus mean : 29.2472**

**Gaus Width: 3.2517**

Entry



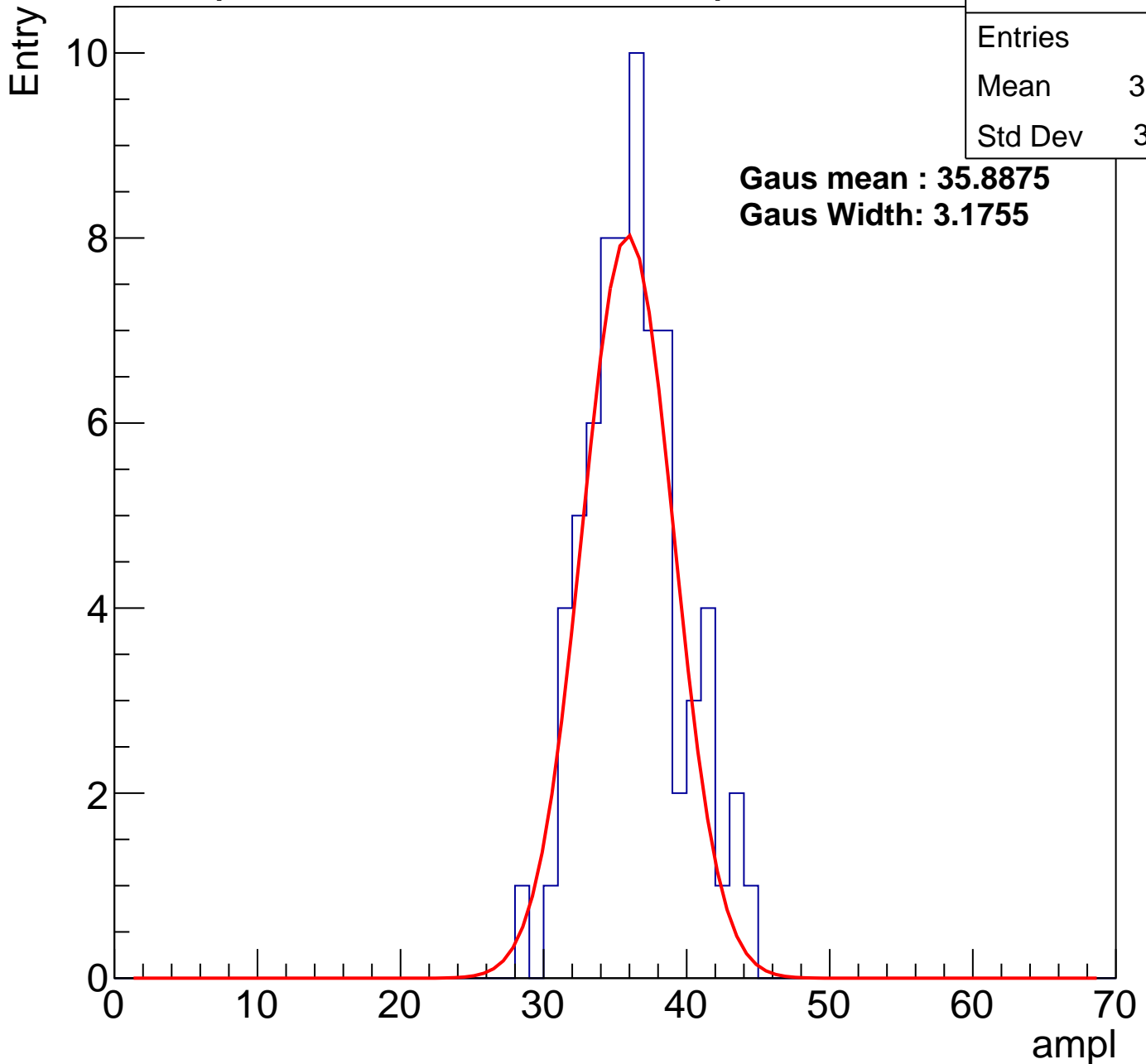
# B1L103S, U1-ch7, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	70
Mean	35.87
Std Dev	3.321

**Gaus mean : 35.8875**

**Gaus Width: 3.1755**



# B1L103S, U1-ch7, adc2

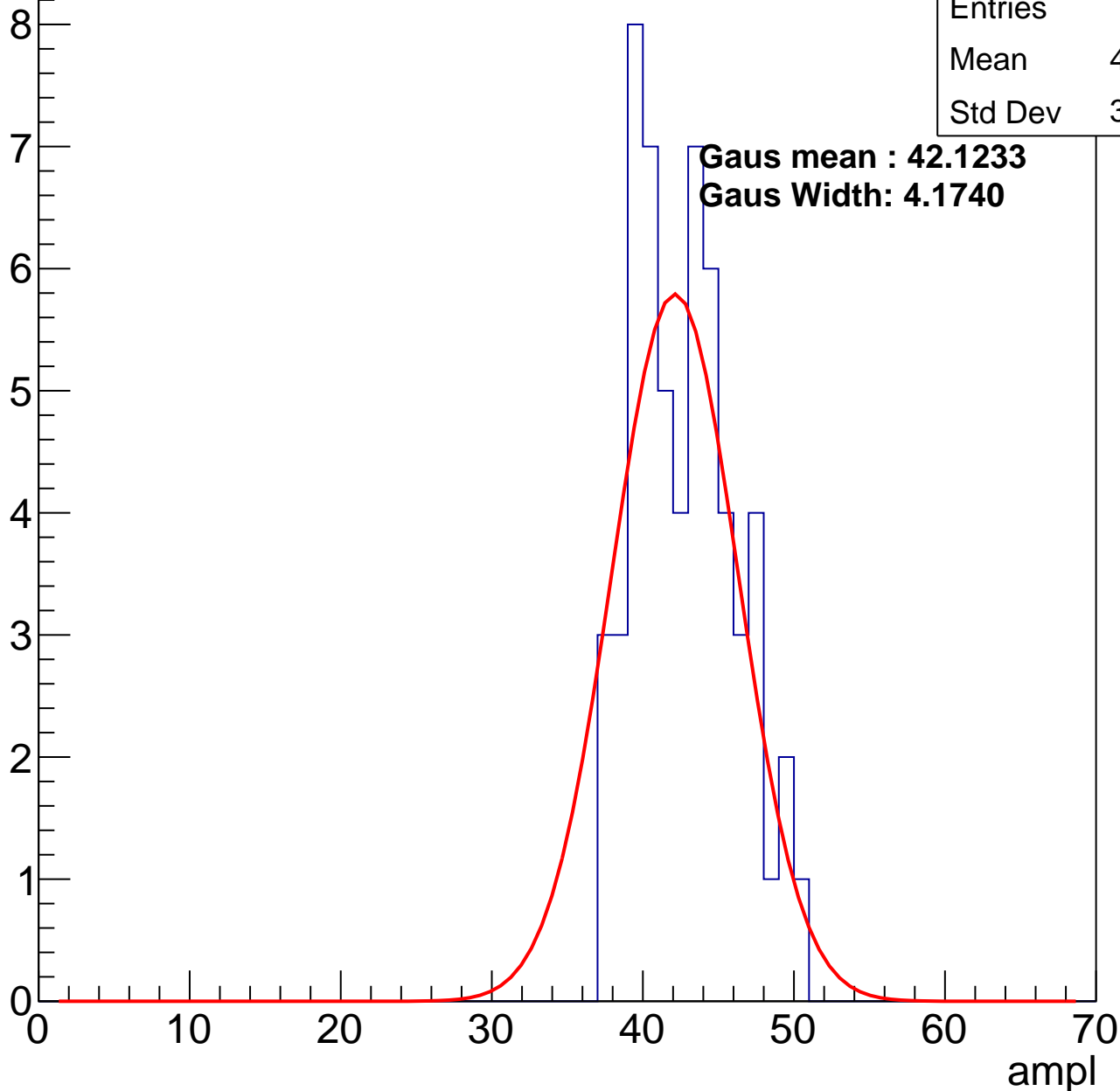
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	42.36
Std Dev	3.305

**Gaus mean : 42.1233**

**Gaus Width: 4.1740**

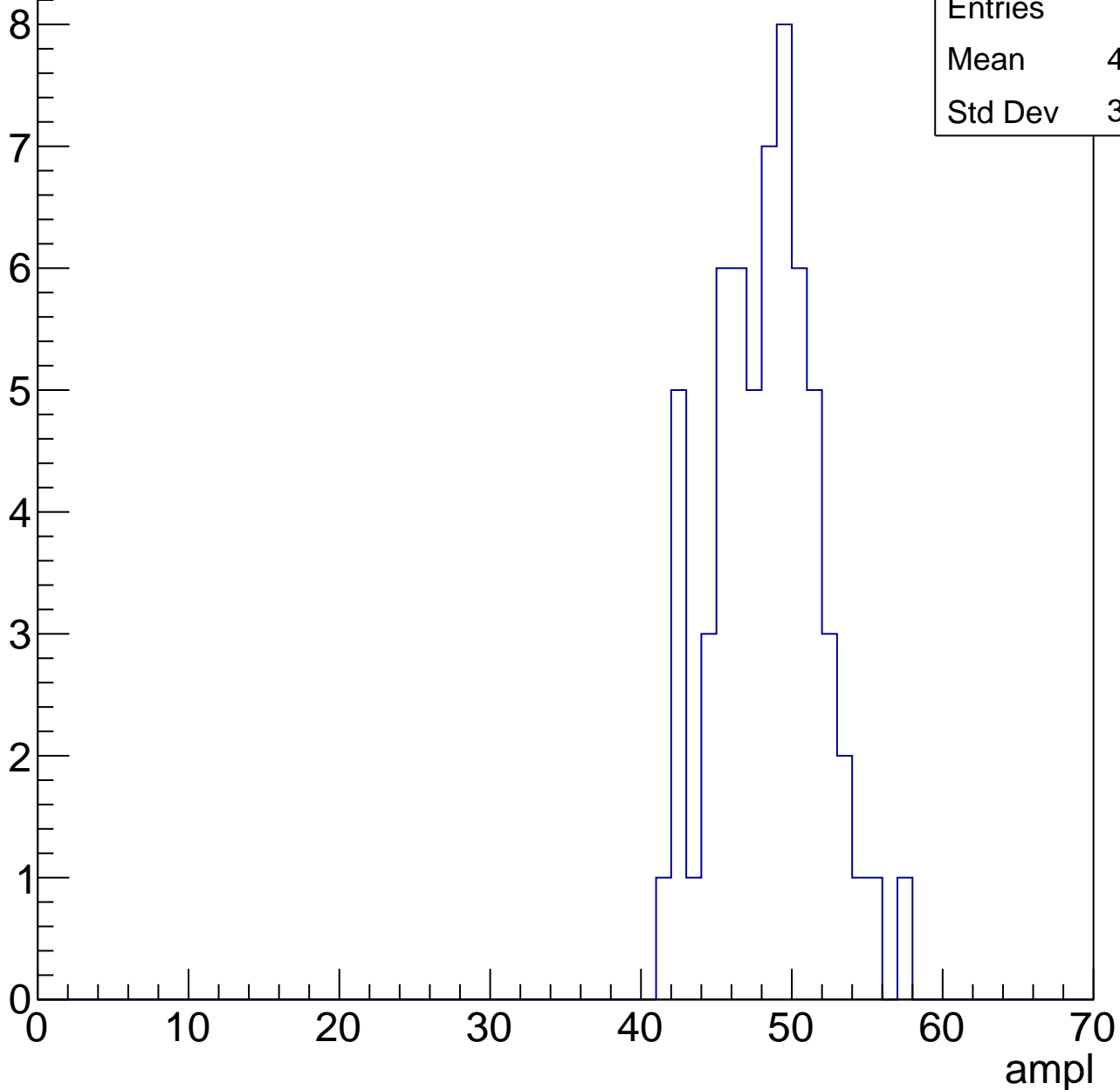


# B1L103S, U1-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

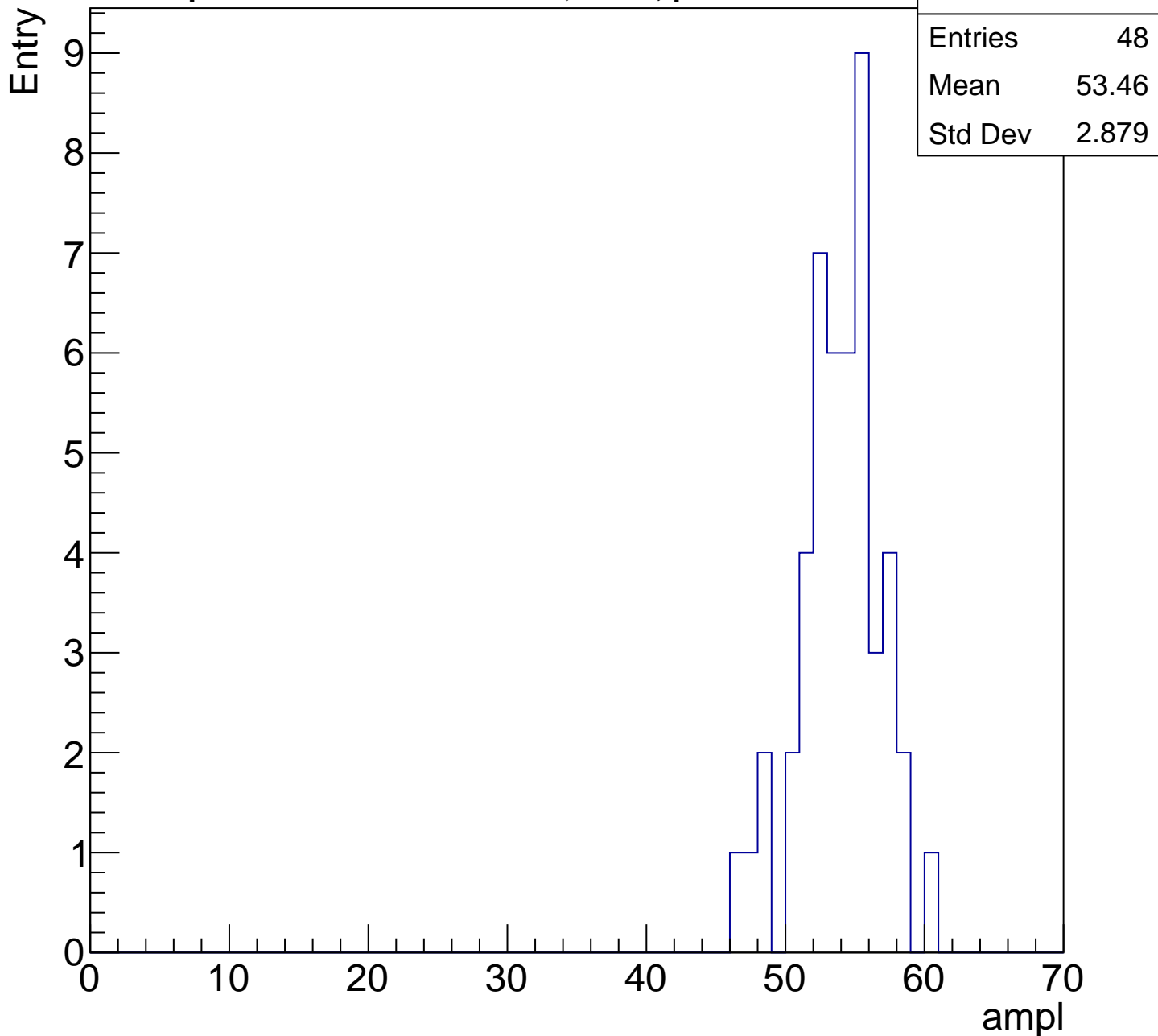
Entry

Entries	61
Mean	47.84
Std Dev	3.446



# B1L103S, U1-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U1-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	60
Mean	57.53
Std Dev	8.049

Entry

10

8

6

4

2

0

0

10

20

30

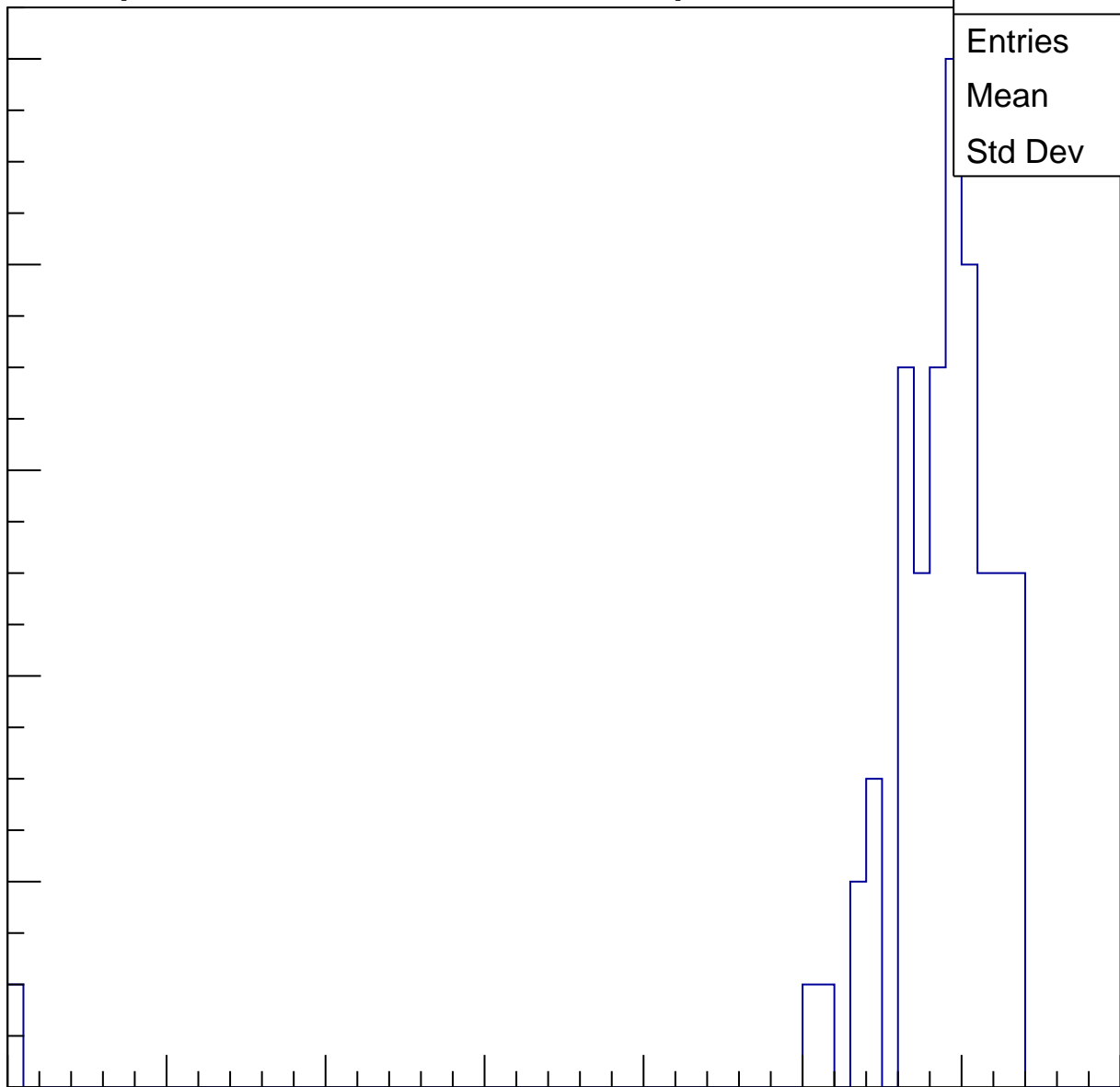
40

50

60

70

ampl

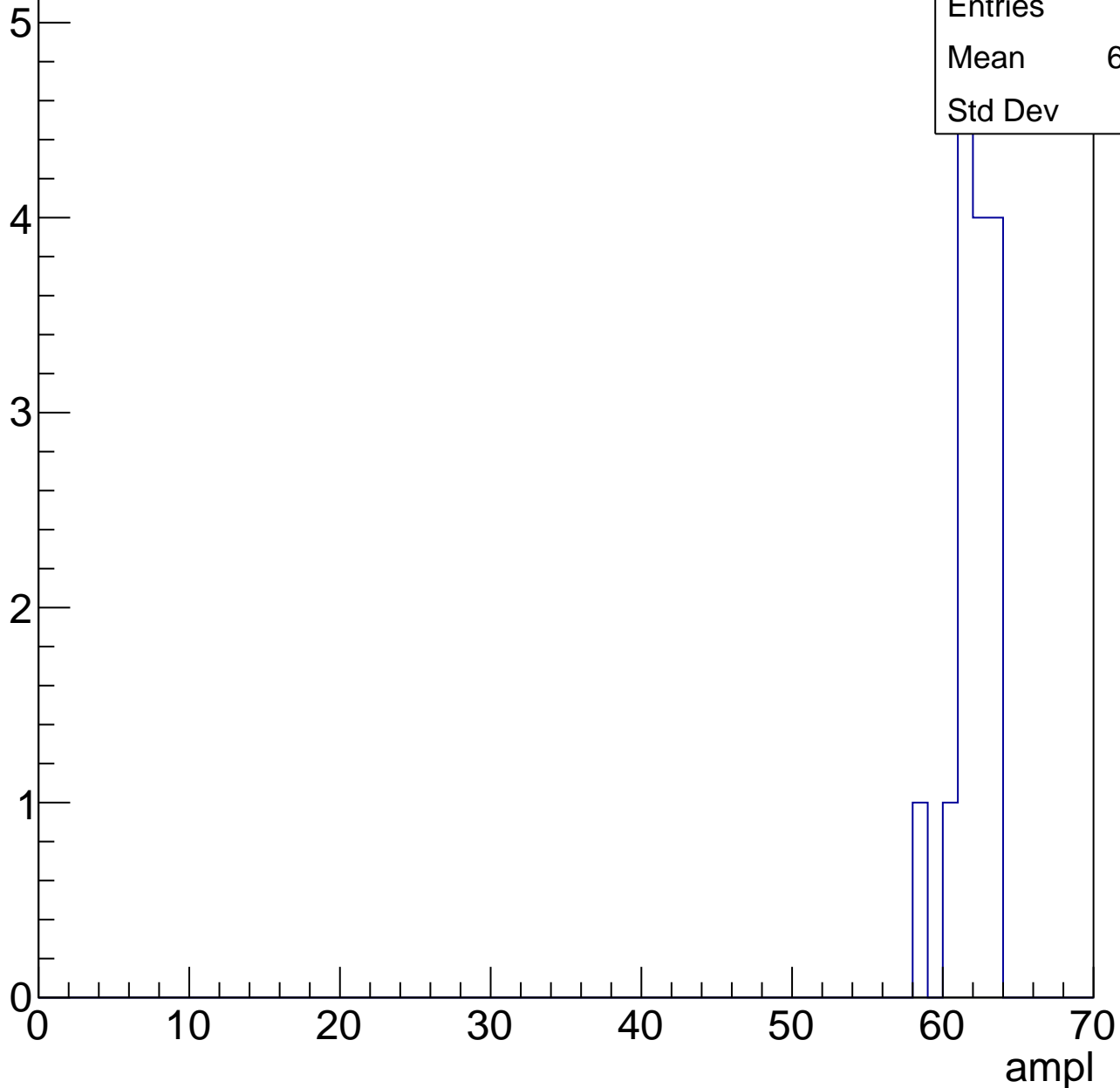


# B1L103S, U1-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	15
Mean	61.53
Std Dev	1.31

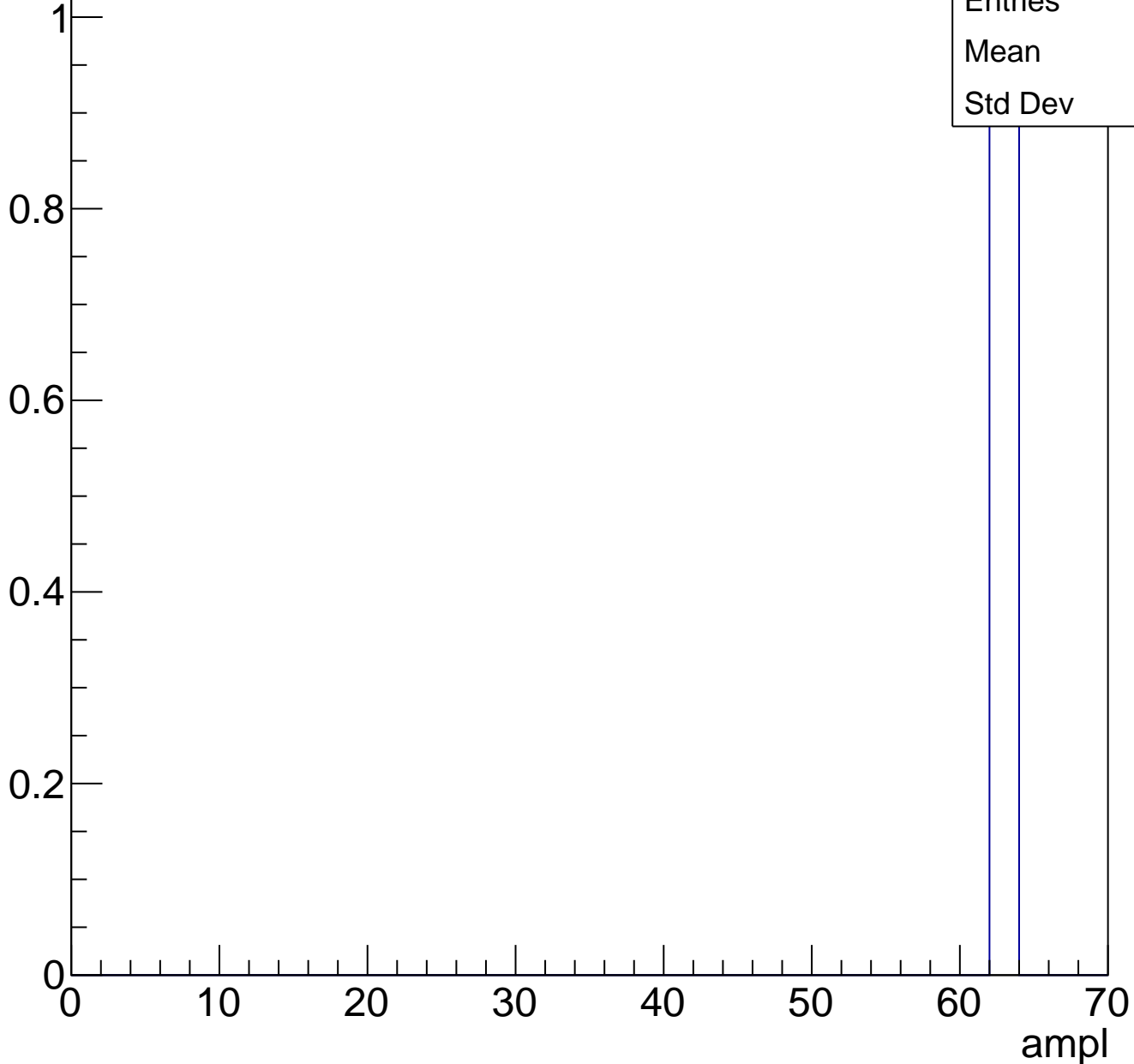




# B1L103S, U1-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch8, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	85
Mean	27.94
Std Dev	4.82

**Gaus mean : 28.3311**

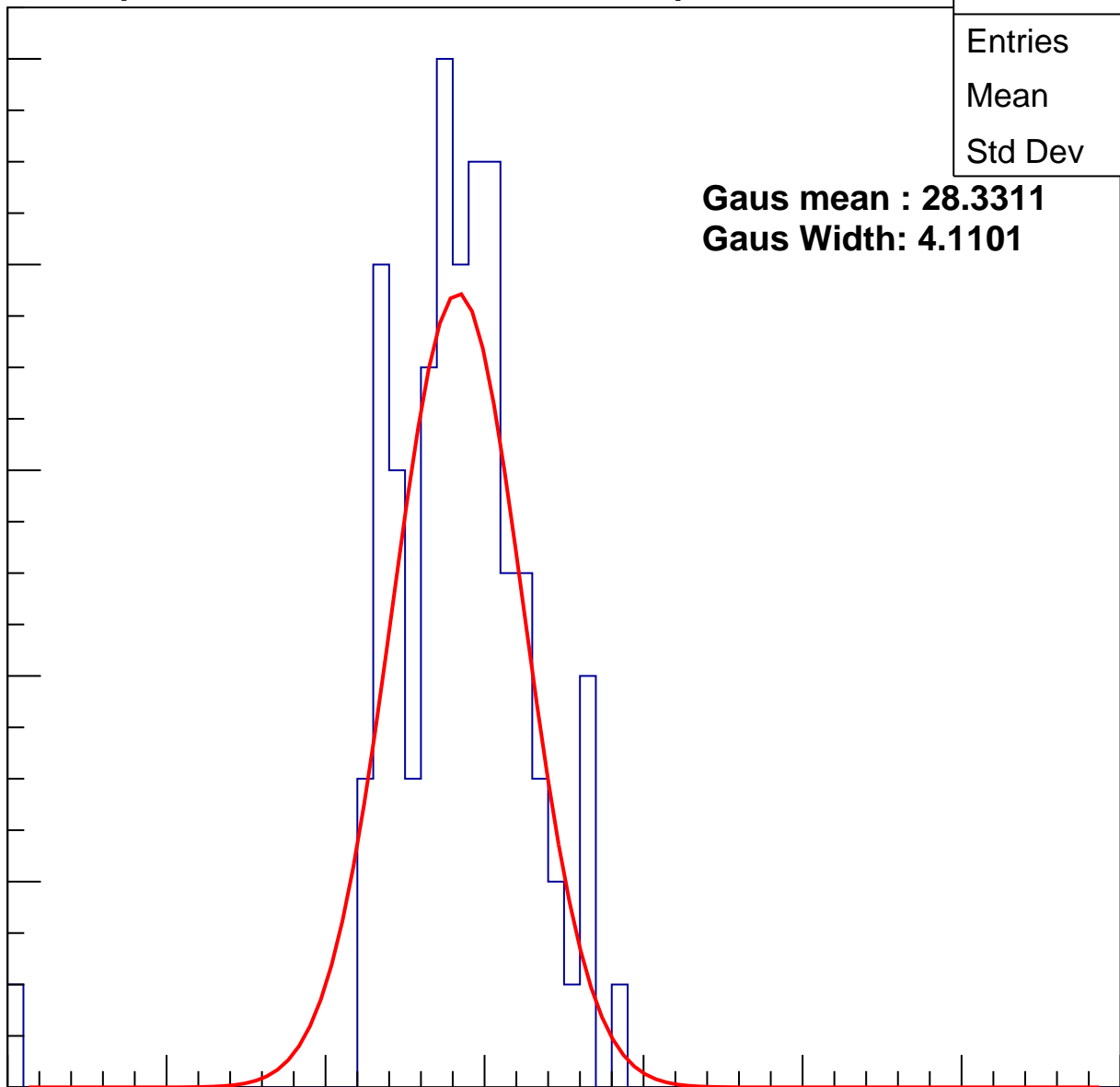
**Gaus Width: 4.1101**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U1-ch8, adc1

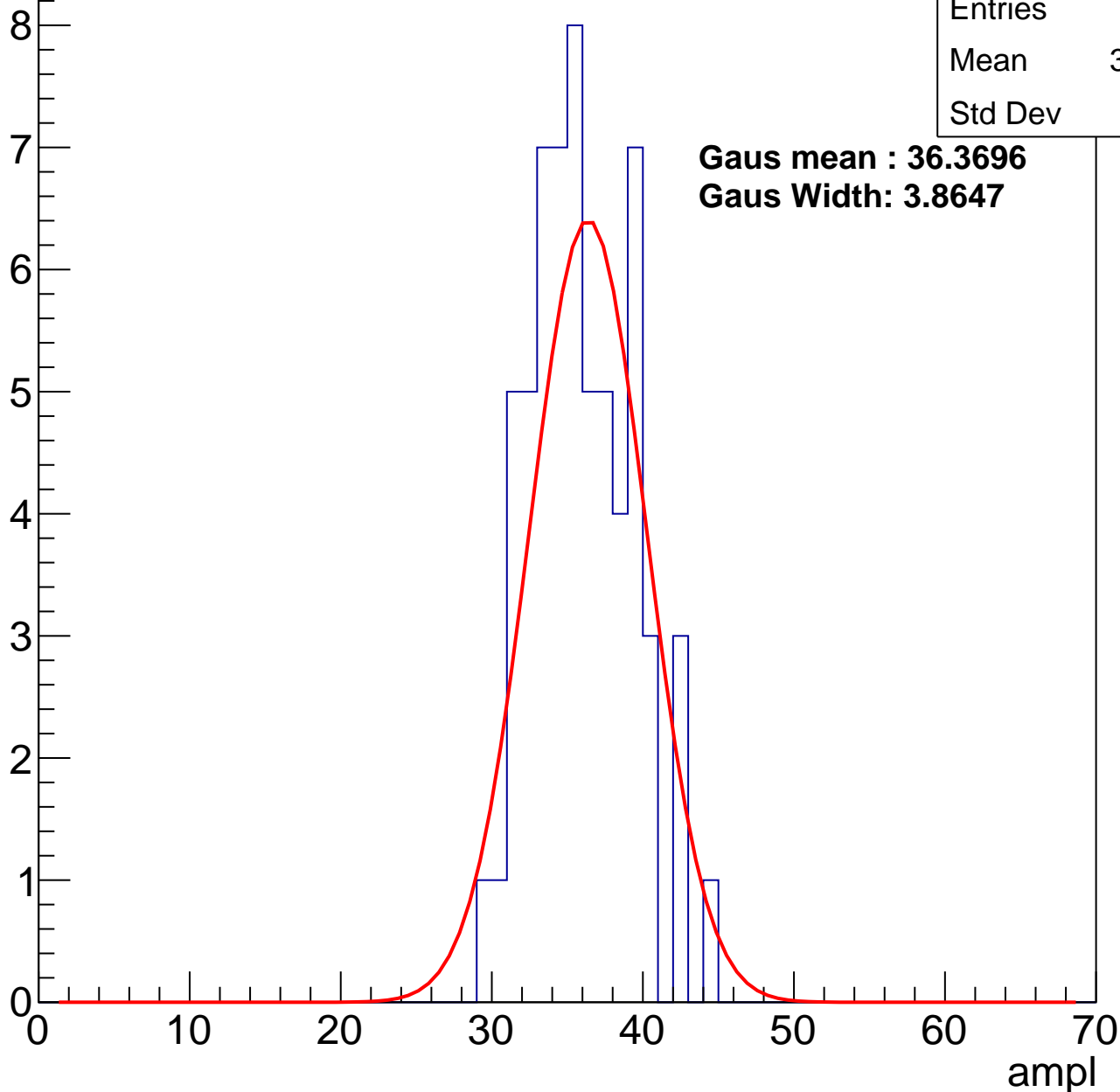
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	35.53
Std Dev	3.31

**Gaus mean : 36.3696**

**Gaus Width: 3.8647**



# B1L103S, U1-ch8, adc2

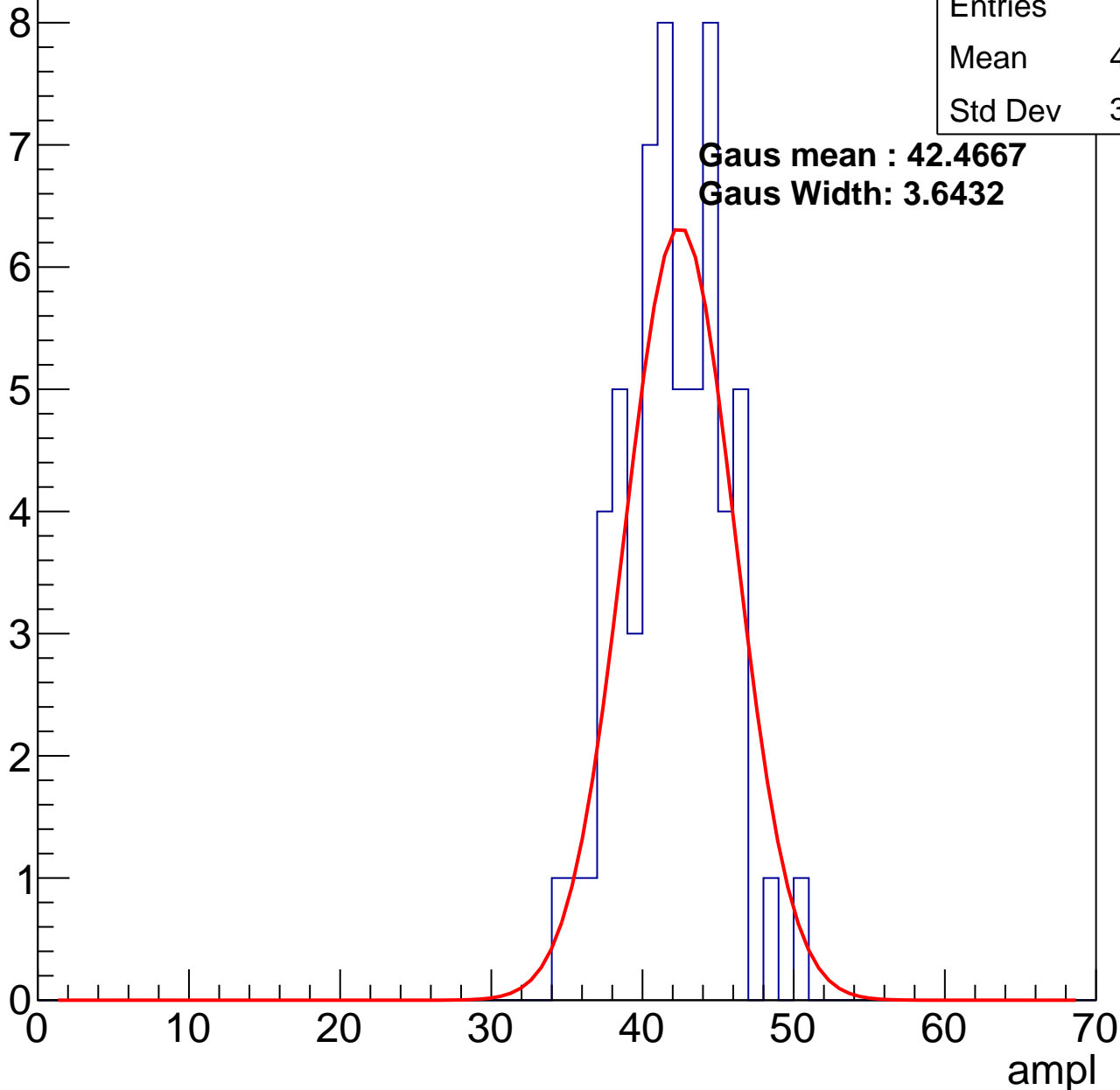
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	41.58
Std Dev	3.279

**Gaus mean : 42.4667**

**Gaus Width: 3.6432**



# B1L103S, U1-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

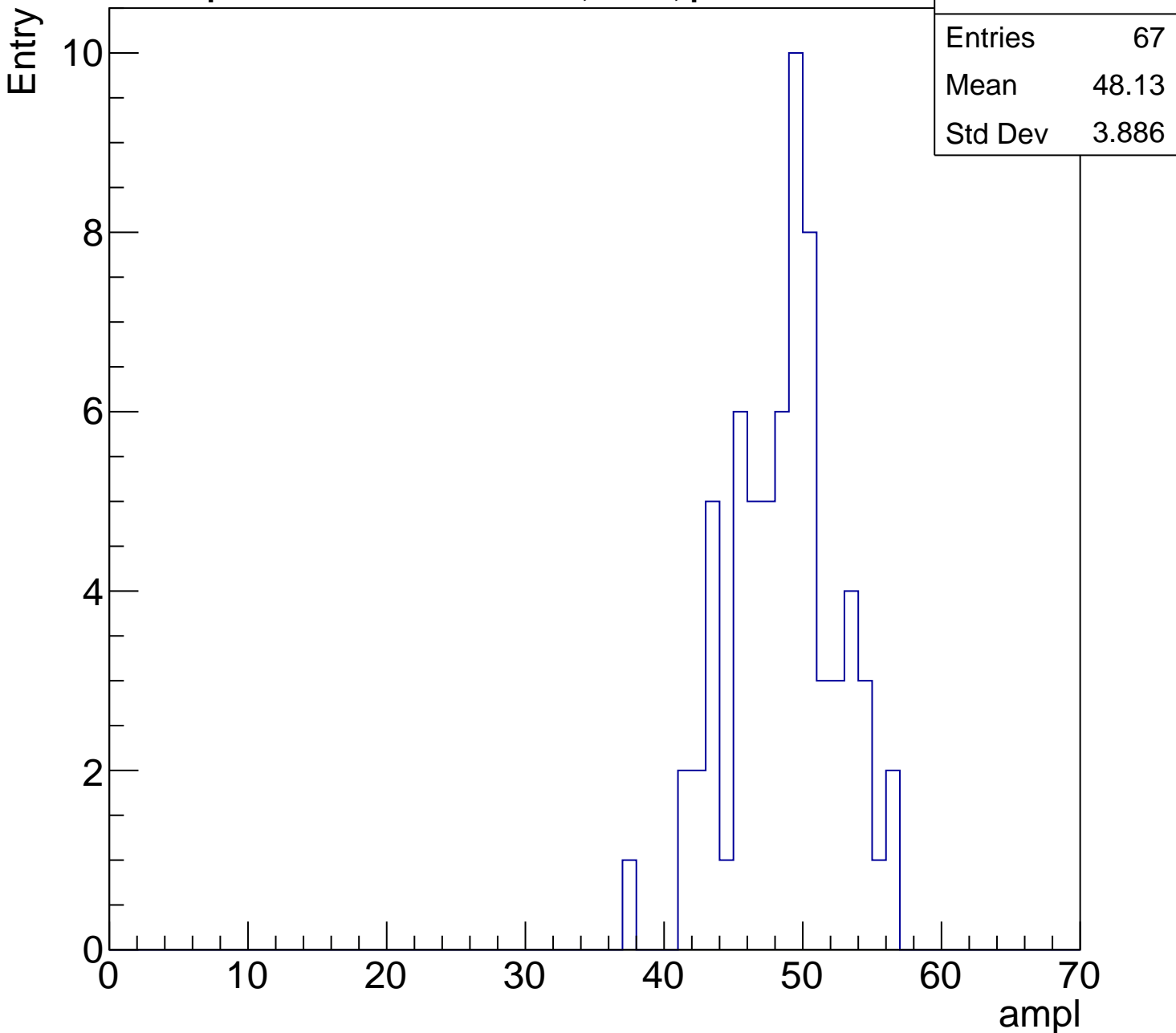
Entries	67
Mean	48.13
Std Dev	3.886

Entry

10  
8  
6  
4  
2  
0

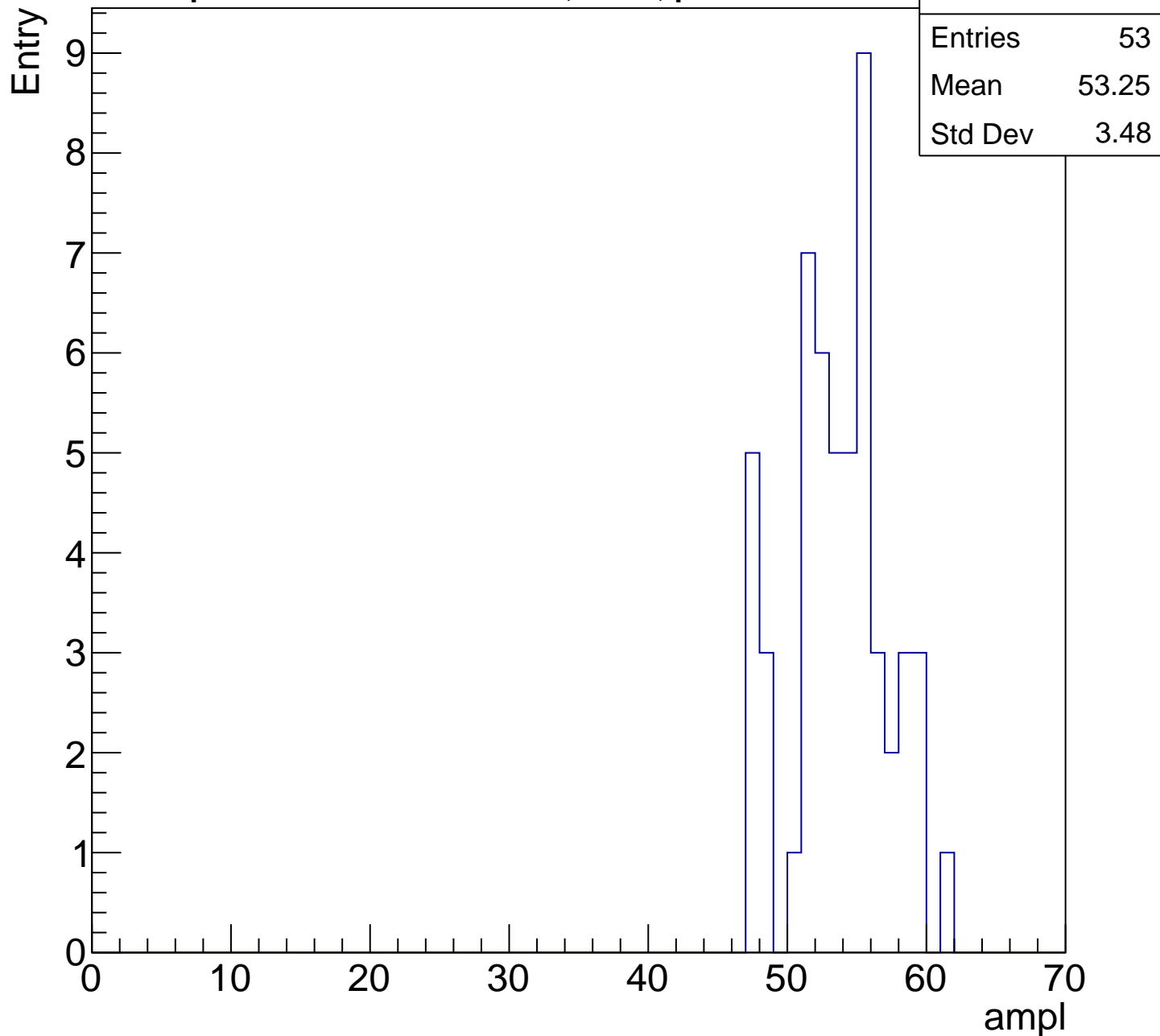
0 10 20 30 40 50 60 70

ampl



# B1L103S, U1-ch8, adc4

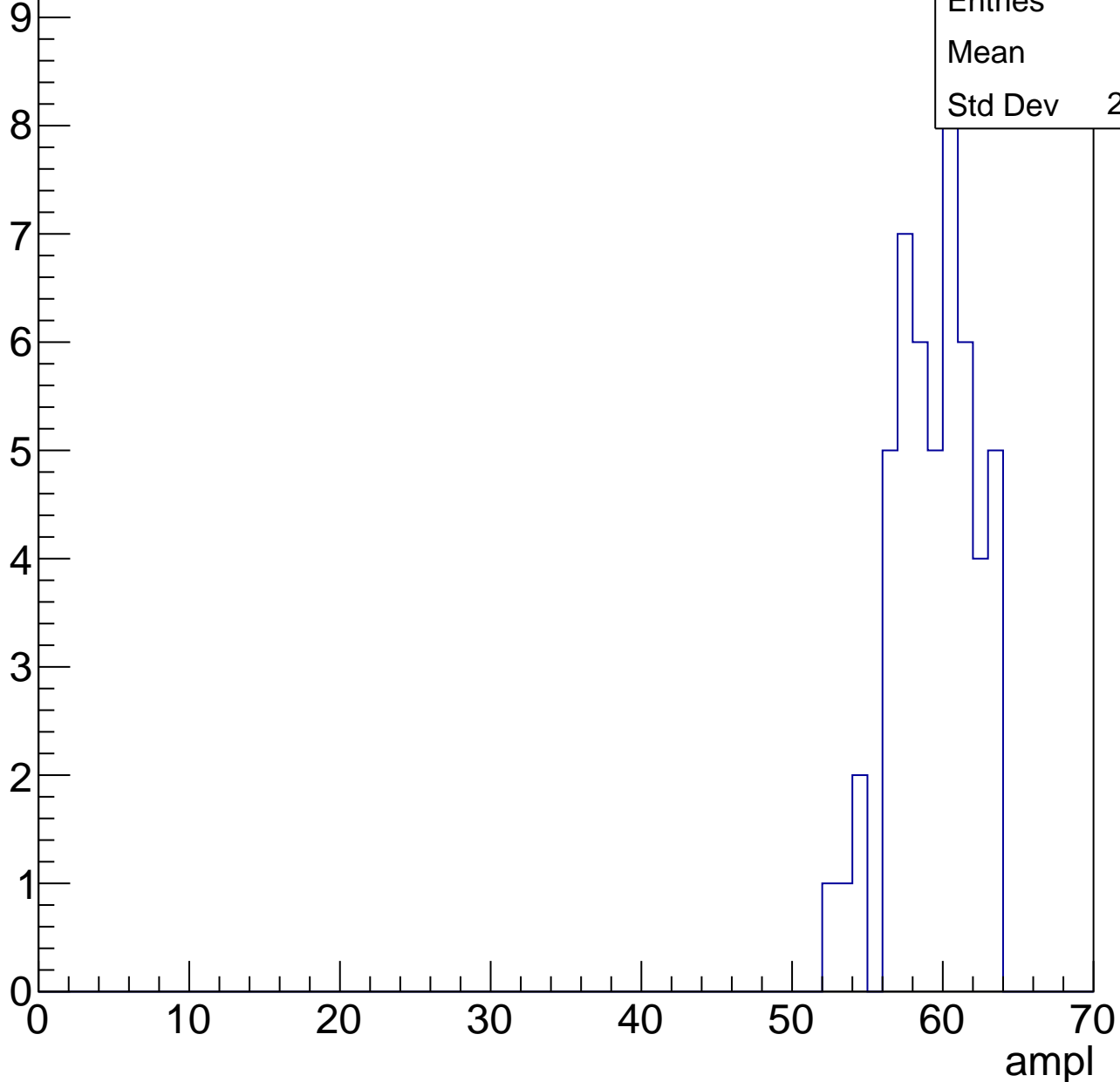
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U1-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

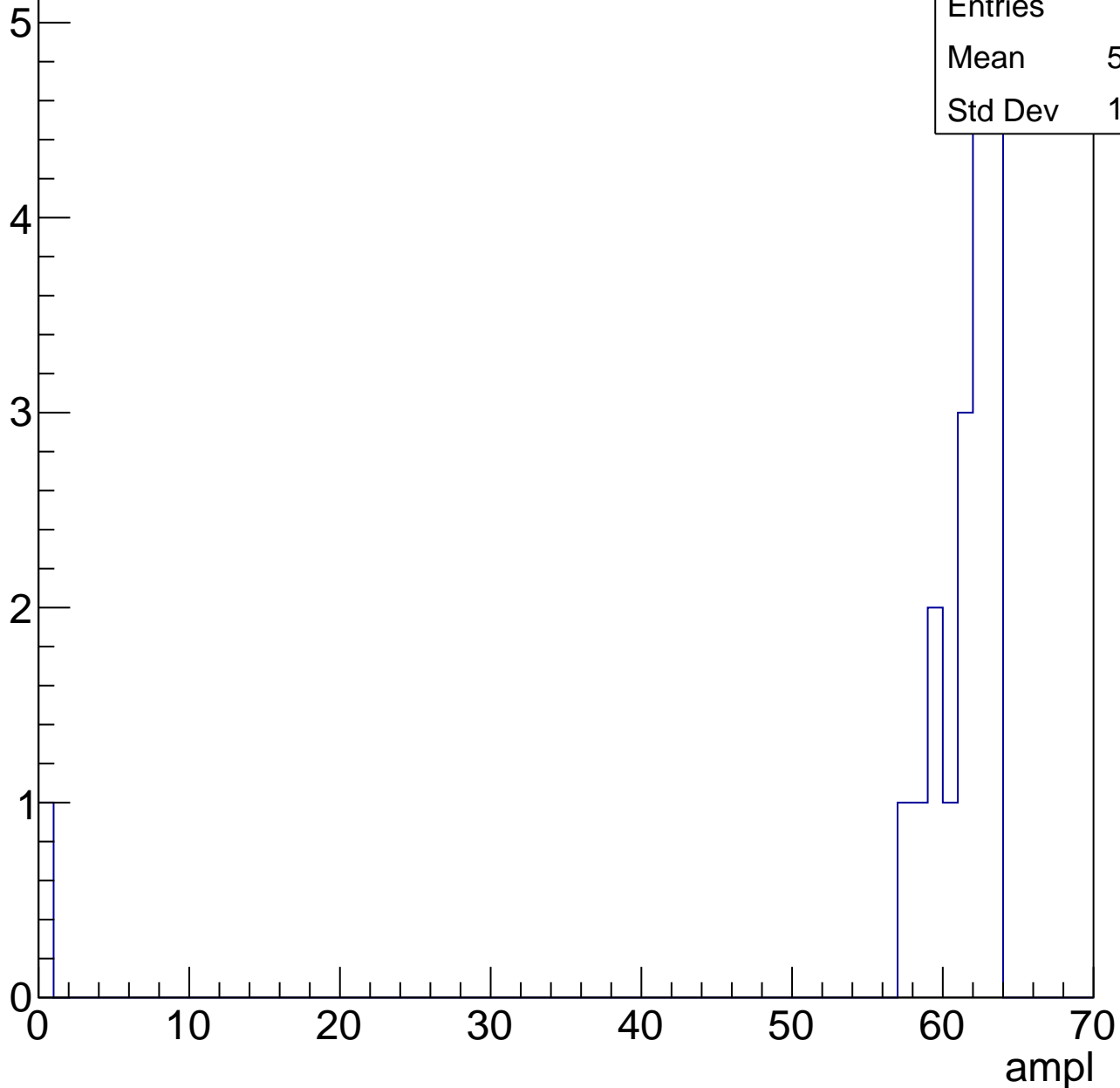


# B1L103S, U1-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	19
Mean	57.95
Std Dev	13.77

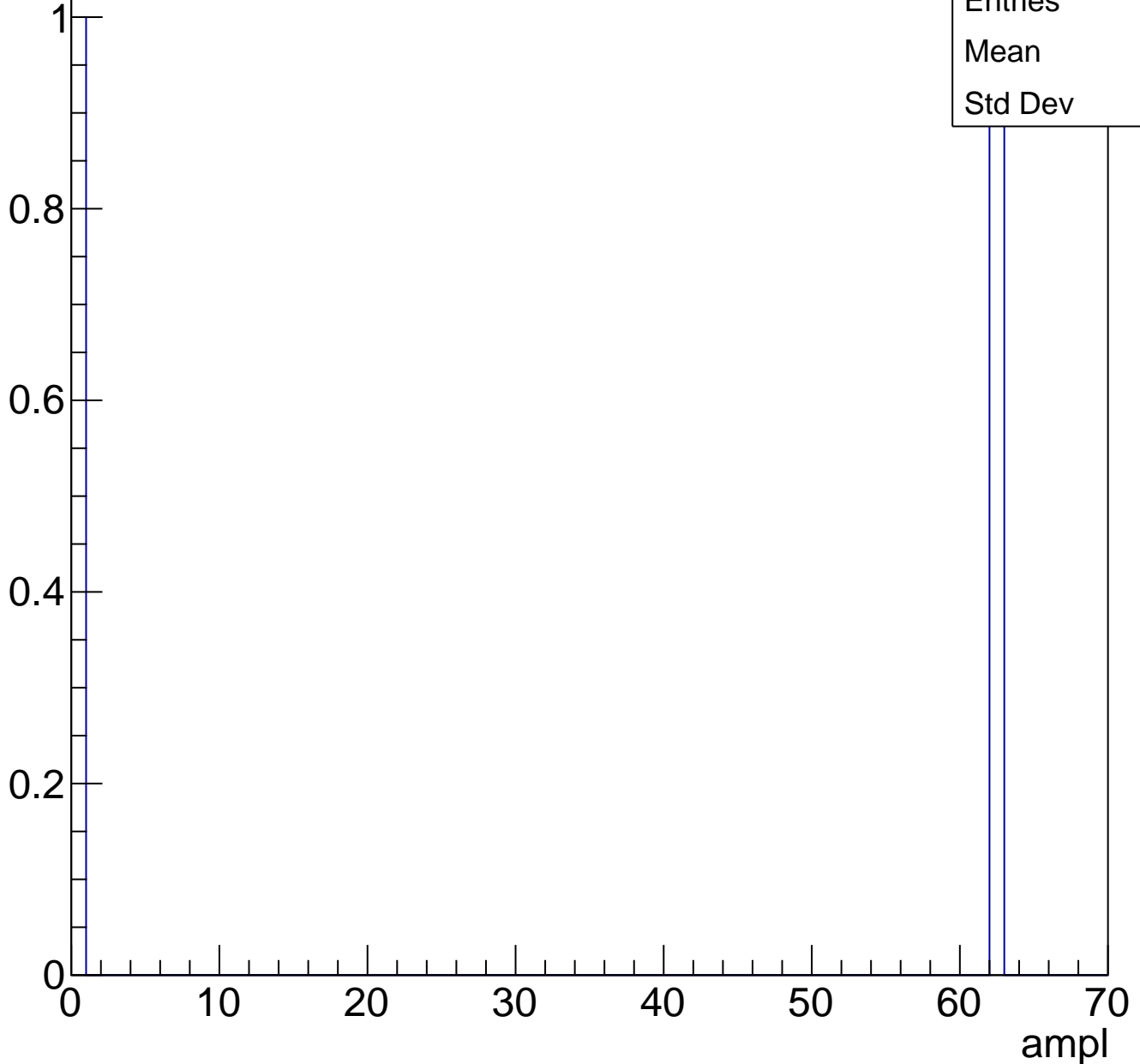




# B1L103S, U1-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch9, adc0

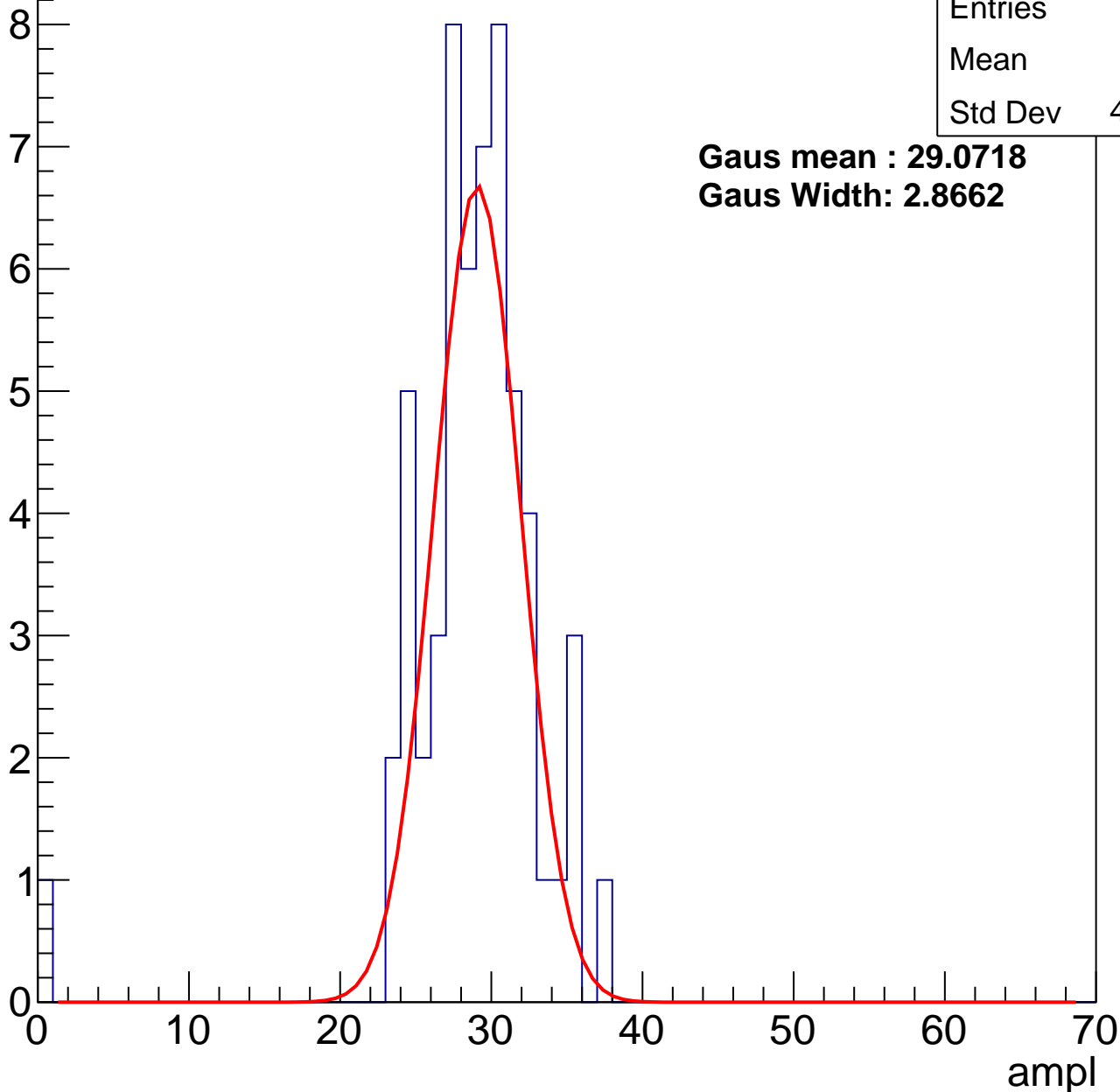
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	28.3
Std Dev	4.927

**Gaus mean : 29.0718**

**Gaus Width: 2.8662**



# B1L103S, U1-ch9, adc1

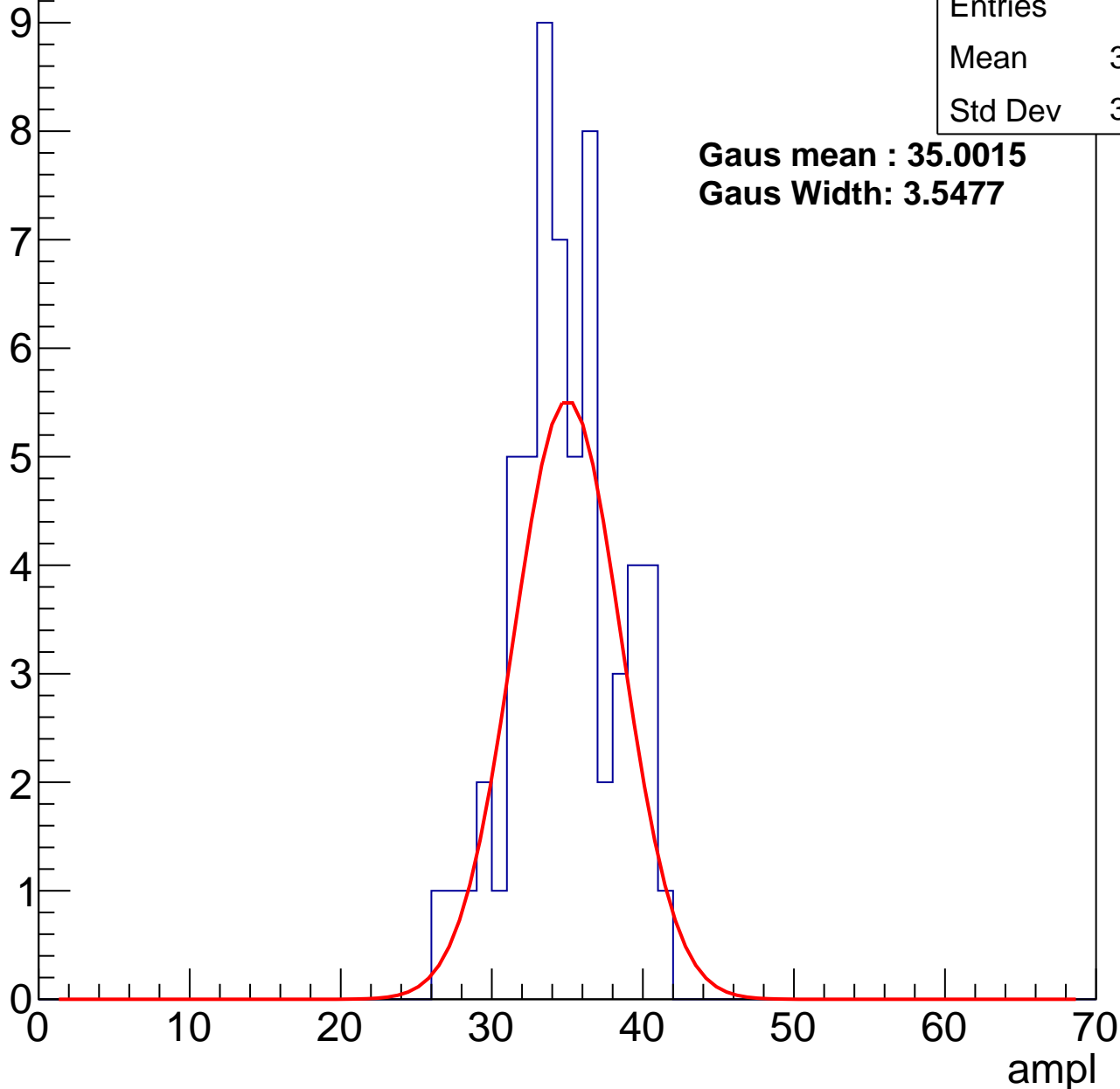
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	34.36
Std Dev	3.389

**Gaus mean : 35.0015**

**Gaus Width: 3.5477**



# B1L103S, U1-ch9, adc2

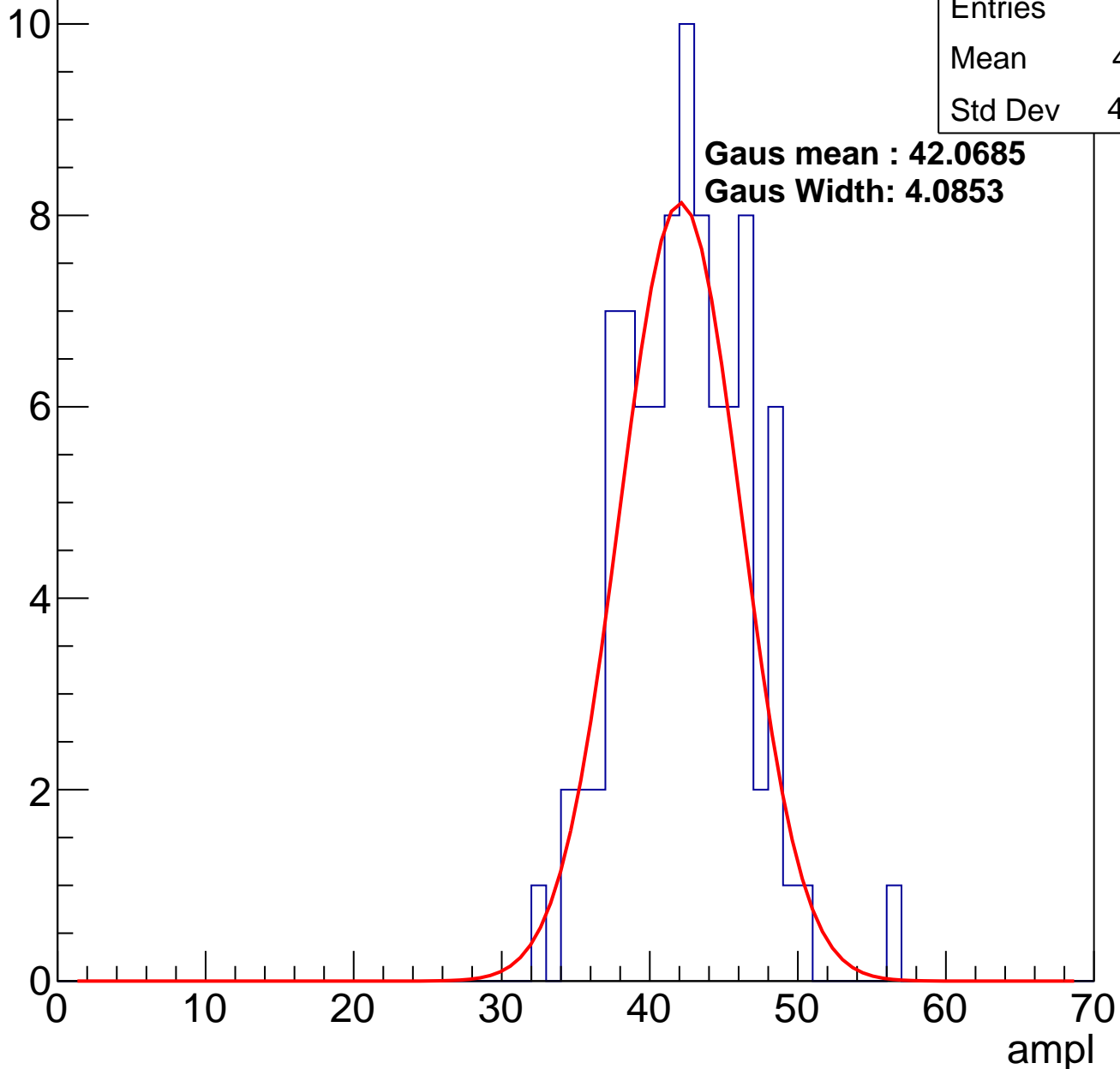
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	90
Mean	41.91
Std Dev	4.162

**Gaus mean : 42.0685**

**Gaus Width: 4.0853**

Entry

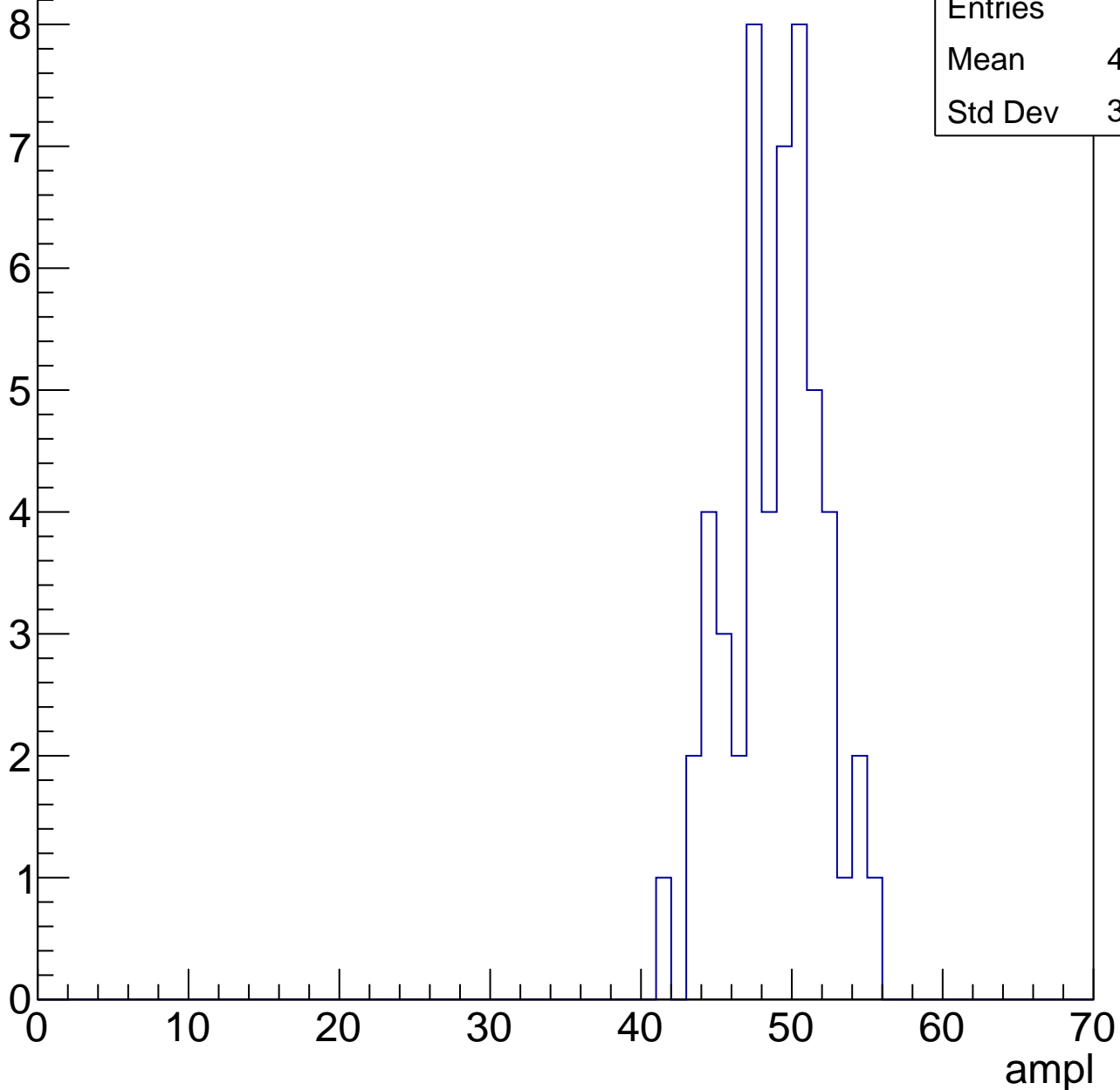


# B1L103S, U1-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

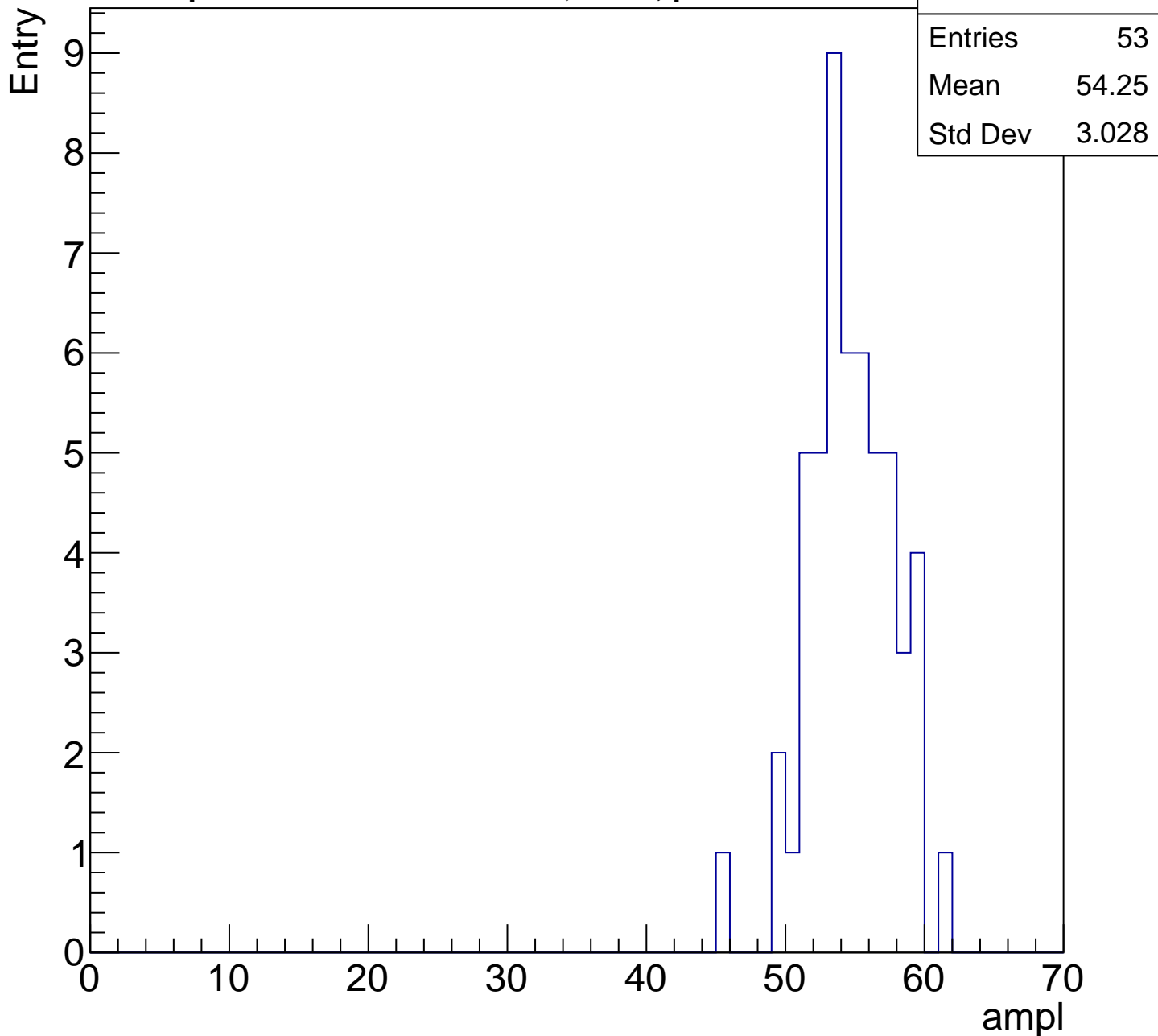
Entry

Entries	52
Mean	48.46
Std Dev	3.066



# B1L103S, U1-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

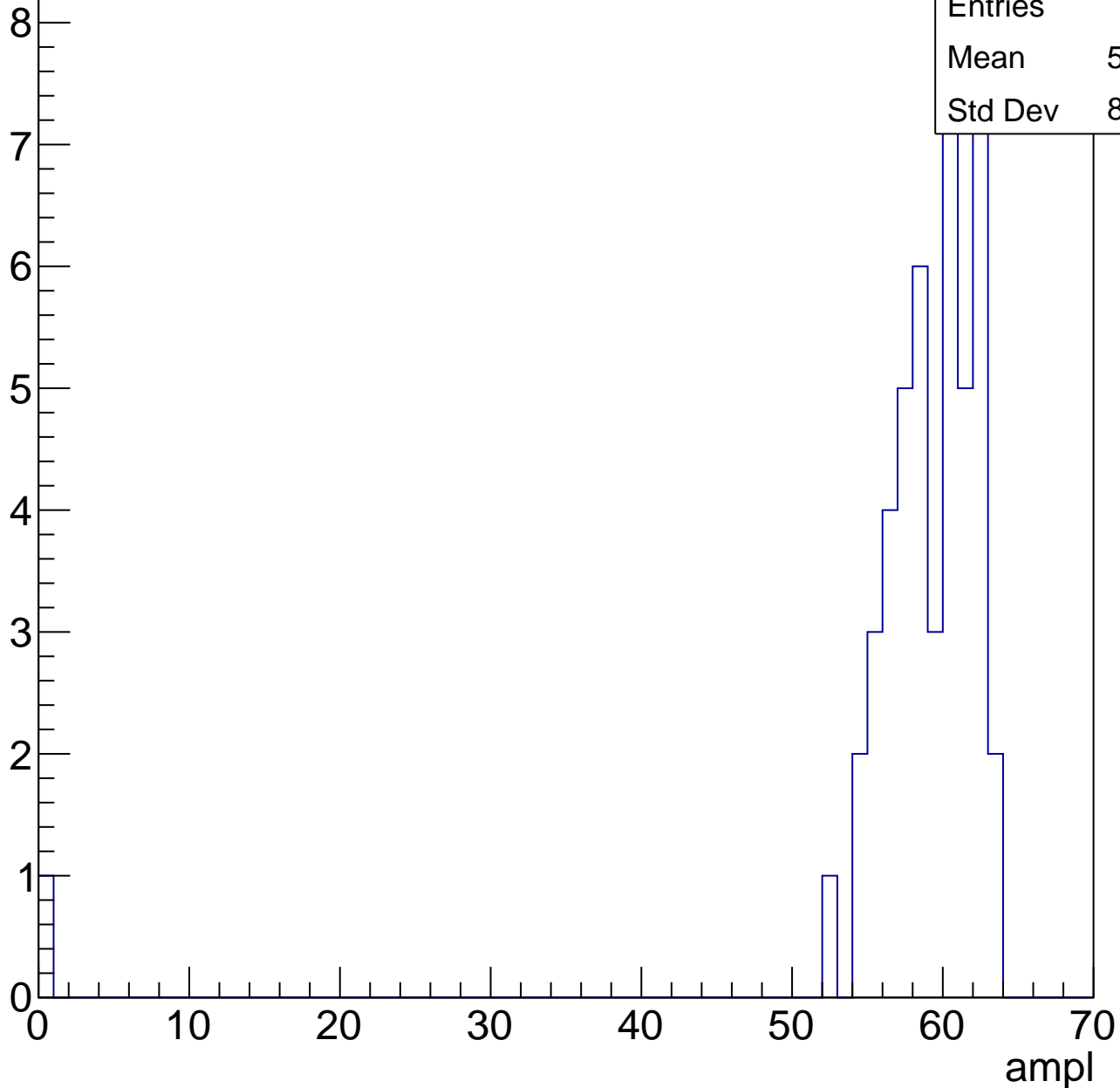


# B1L103S, U1-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

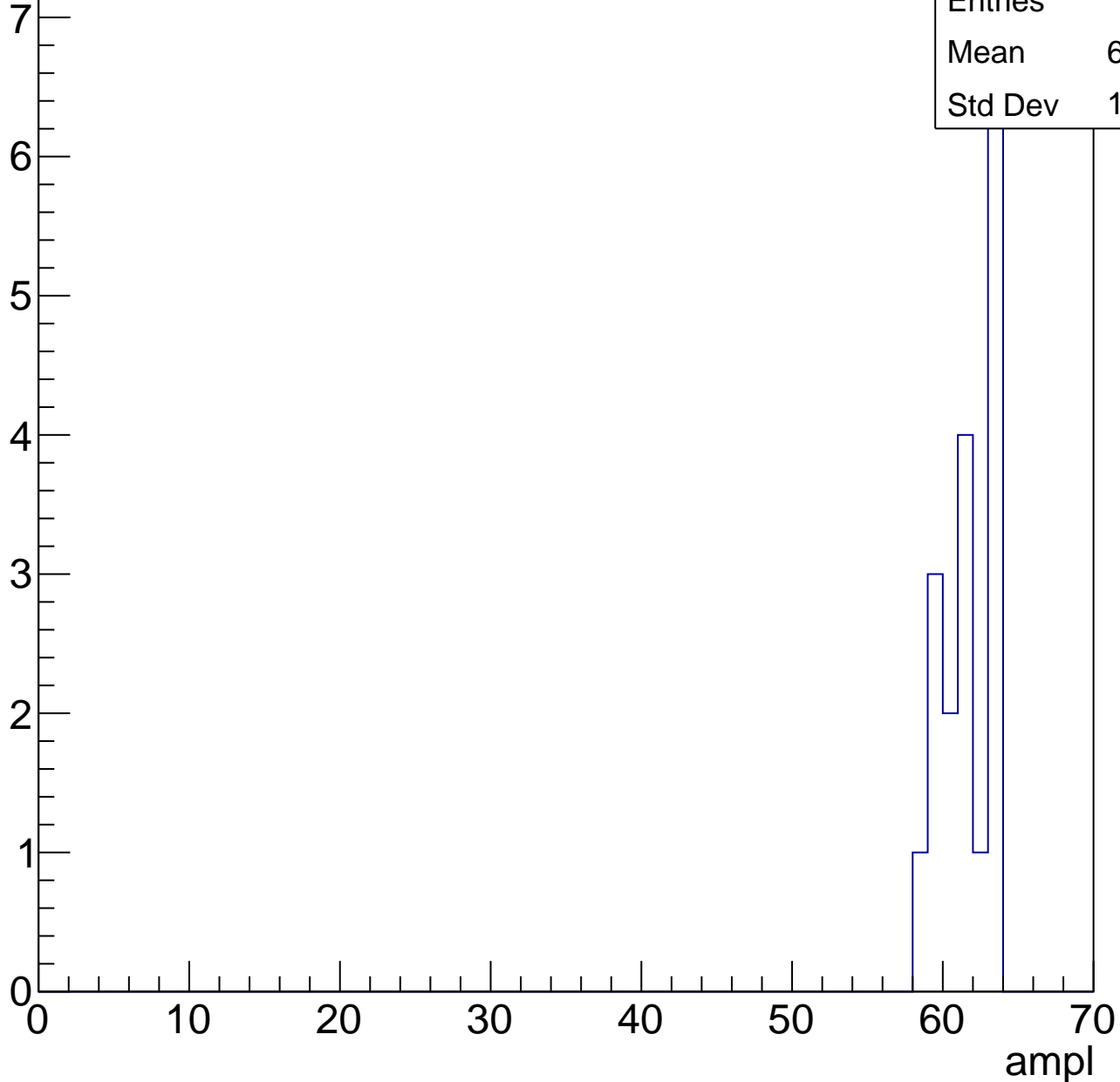
Entries	48
Mean	57.62
Std Dev	8.817



# B1L103S, U1-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

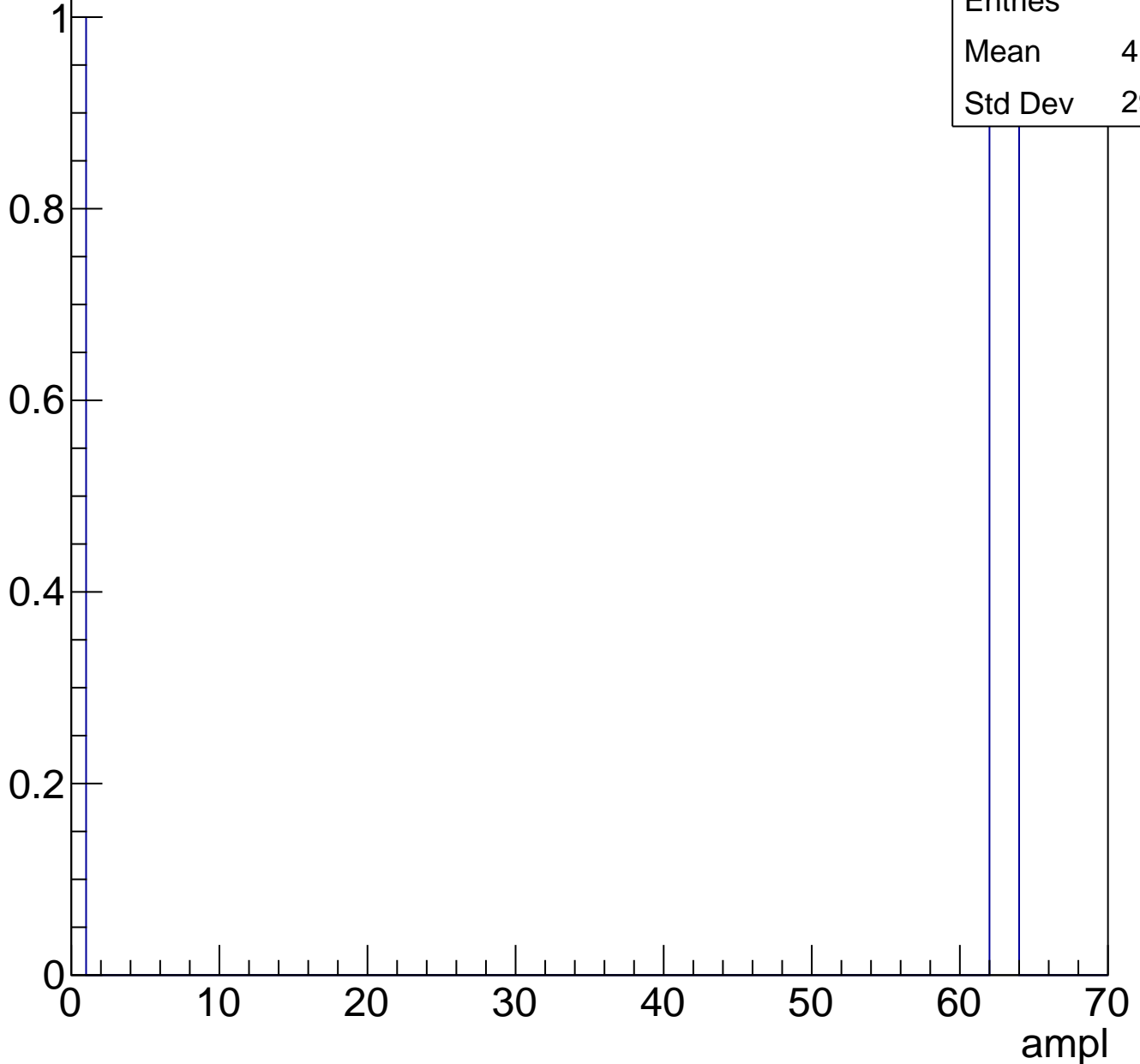




# B1L103S, U1-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch10, adc0

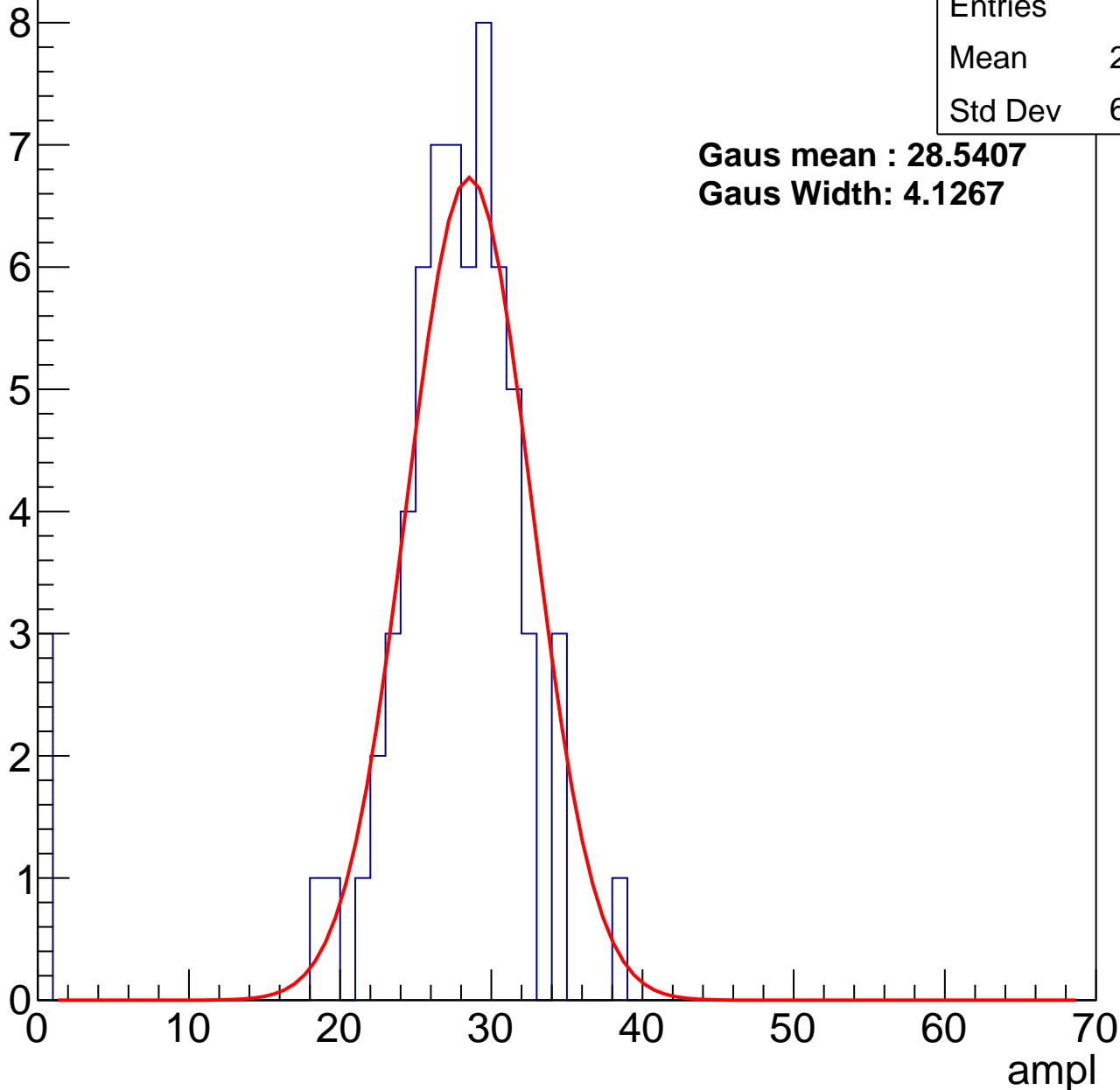
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	26.25
Std Dev	6.703

**Gaus mean : 28.5407**

**Gaus Width: 4.1267**



# B1L103S, U1-ch10, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	67
Mean	33.75
Std Dev	3.525

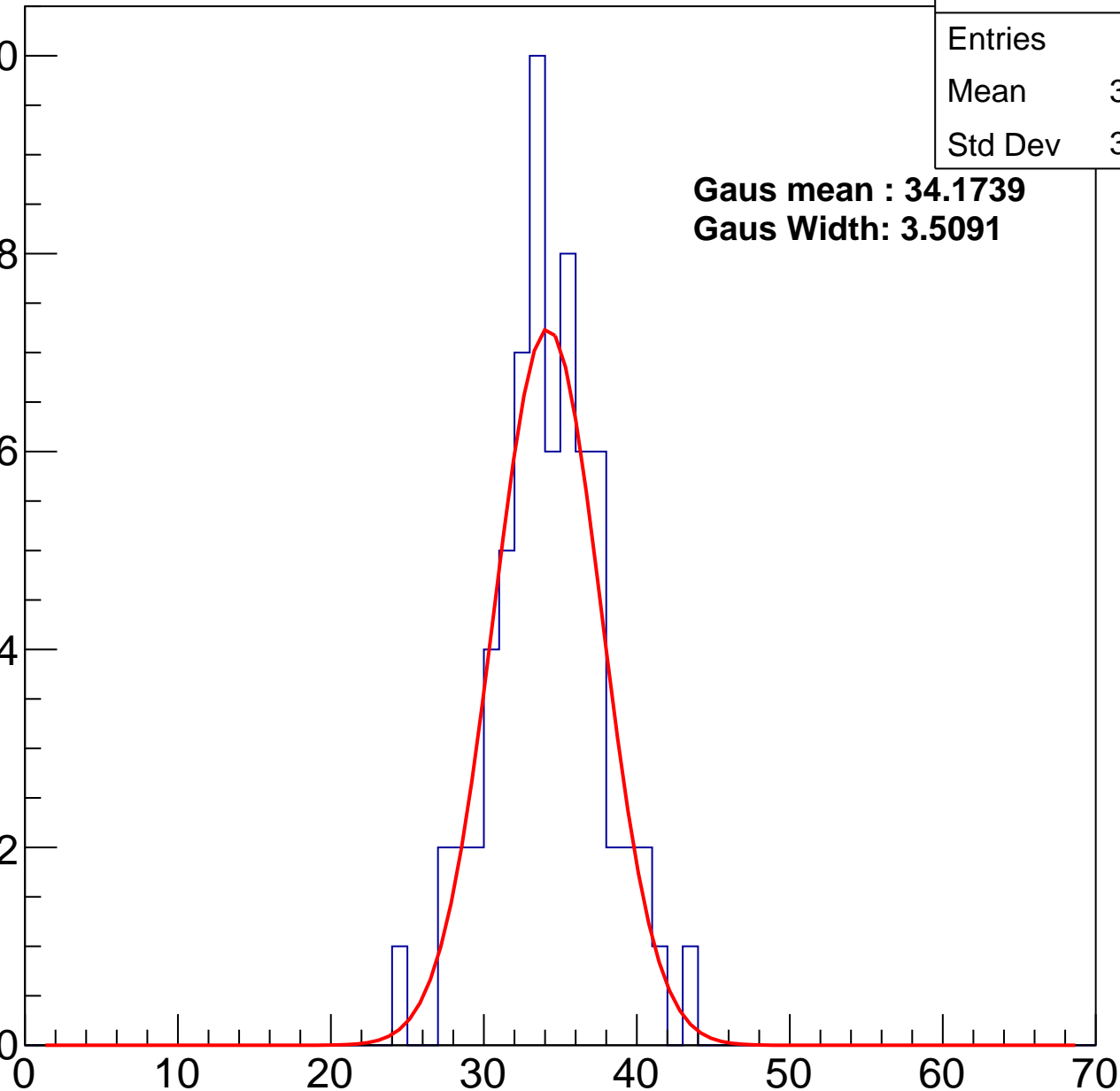
**Gaus mean : 34.1739**

**Gaus Width: 3.5091**

Entry

10  
8  
6  
4  
2  
0

ampl



# B1L103S, U1-ch10, adc2

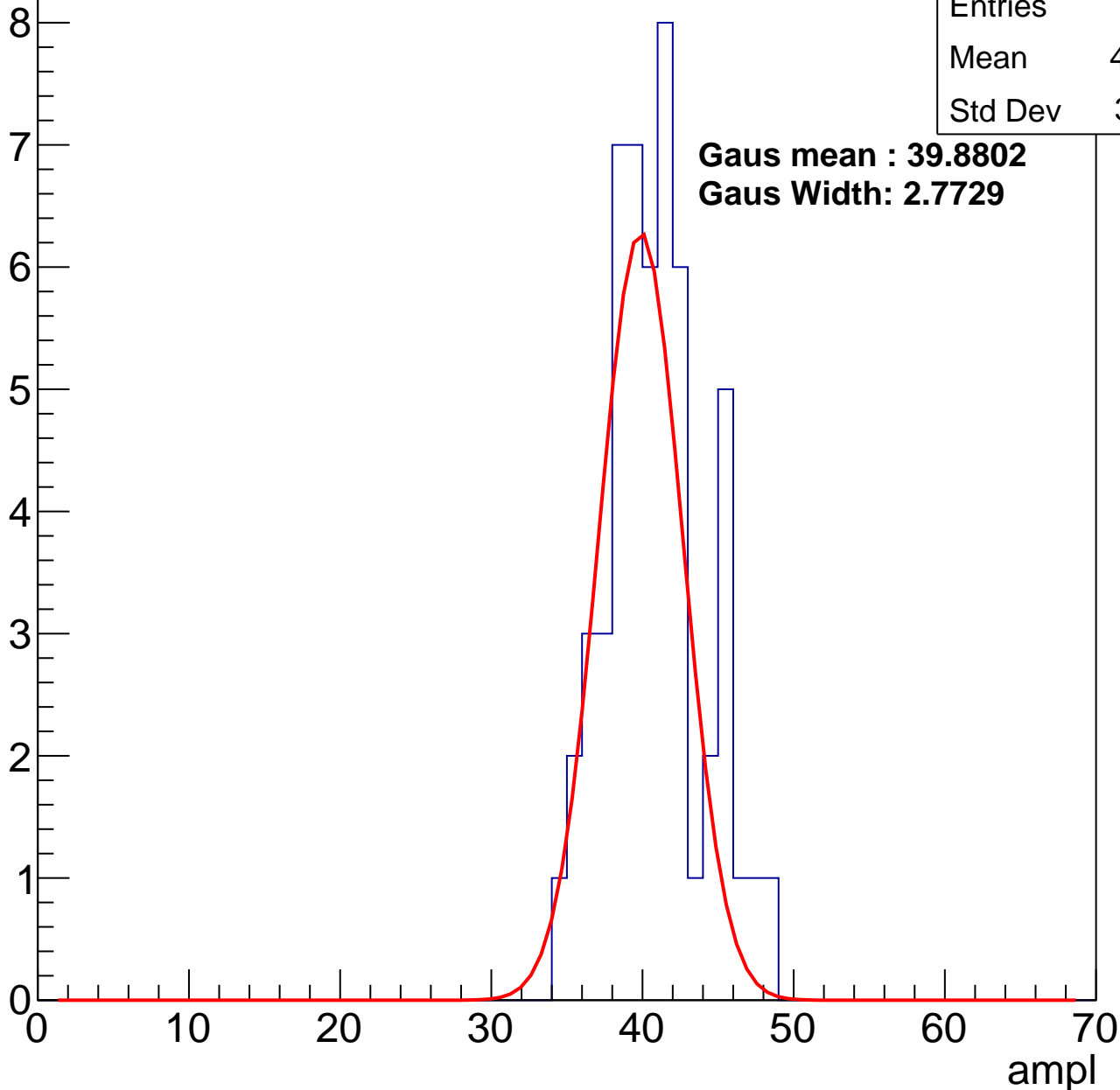
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	40.35
Std Dev	3.151

**Gaus mean : 39.8802**

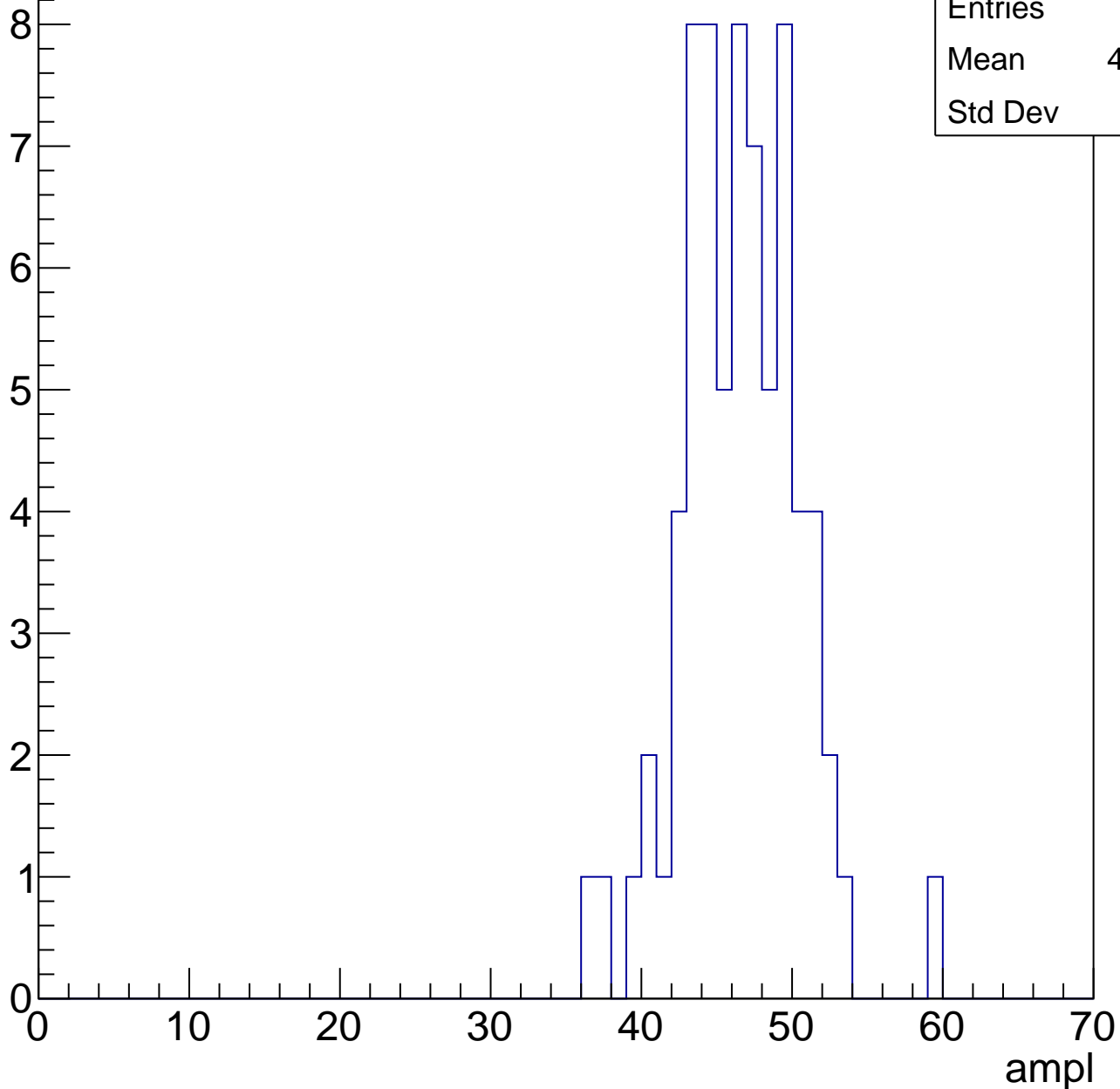
**Gaus Width: 2.7729**



# B1L103S, U1-ch10, adc3

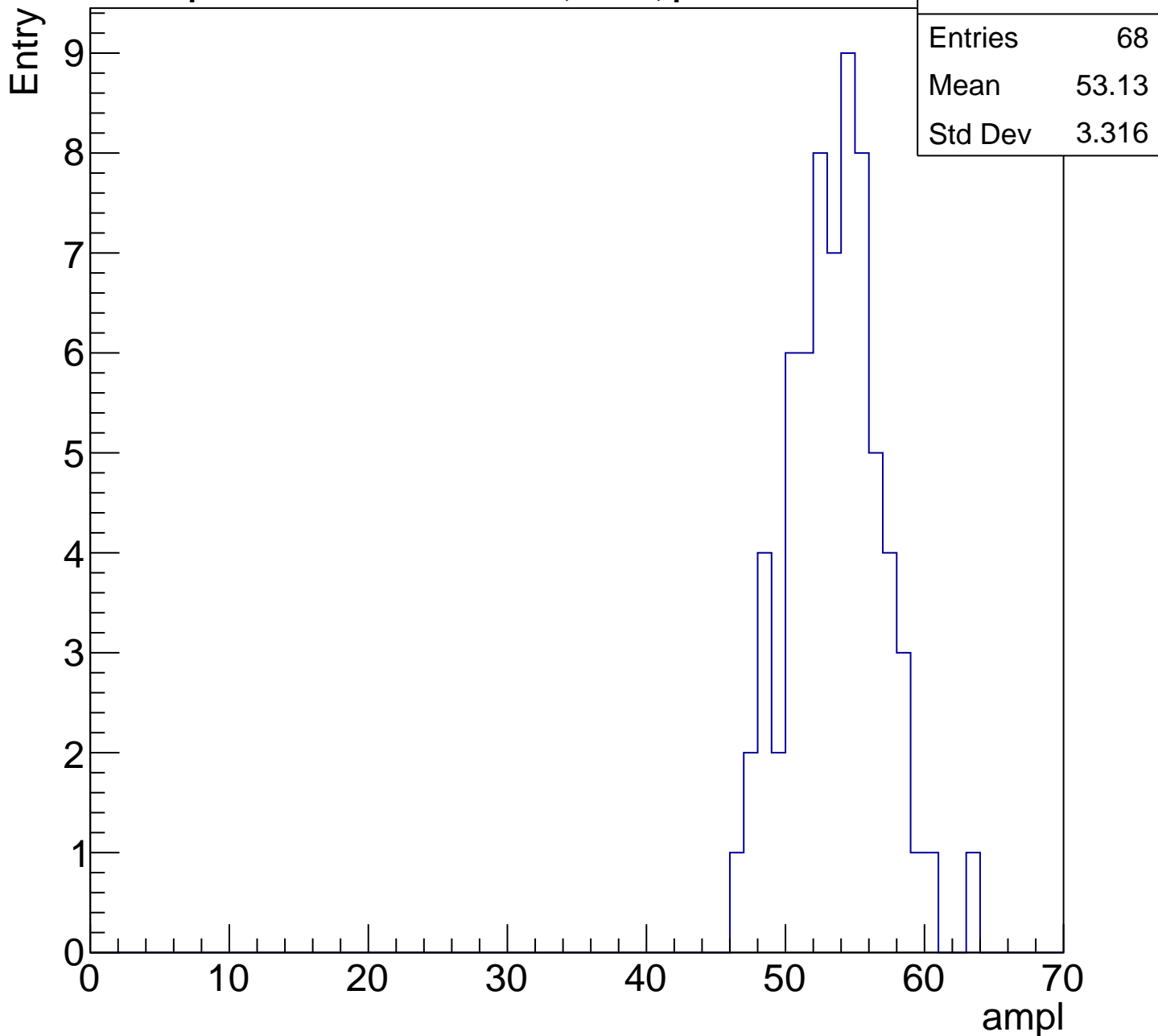
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



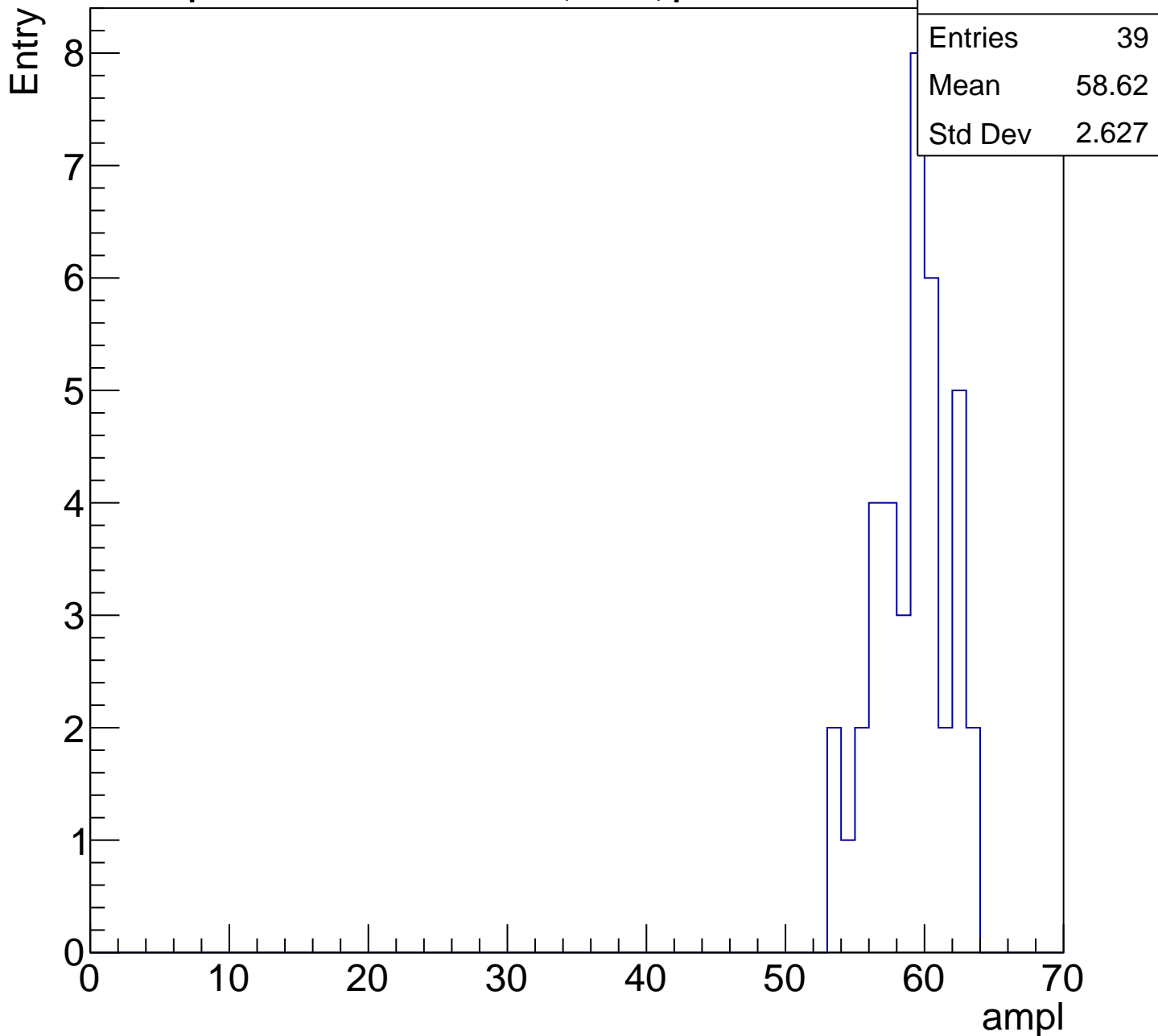
# B1L103S, U1-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U1-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

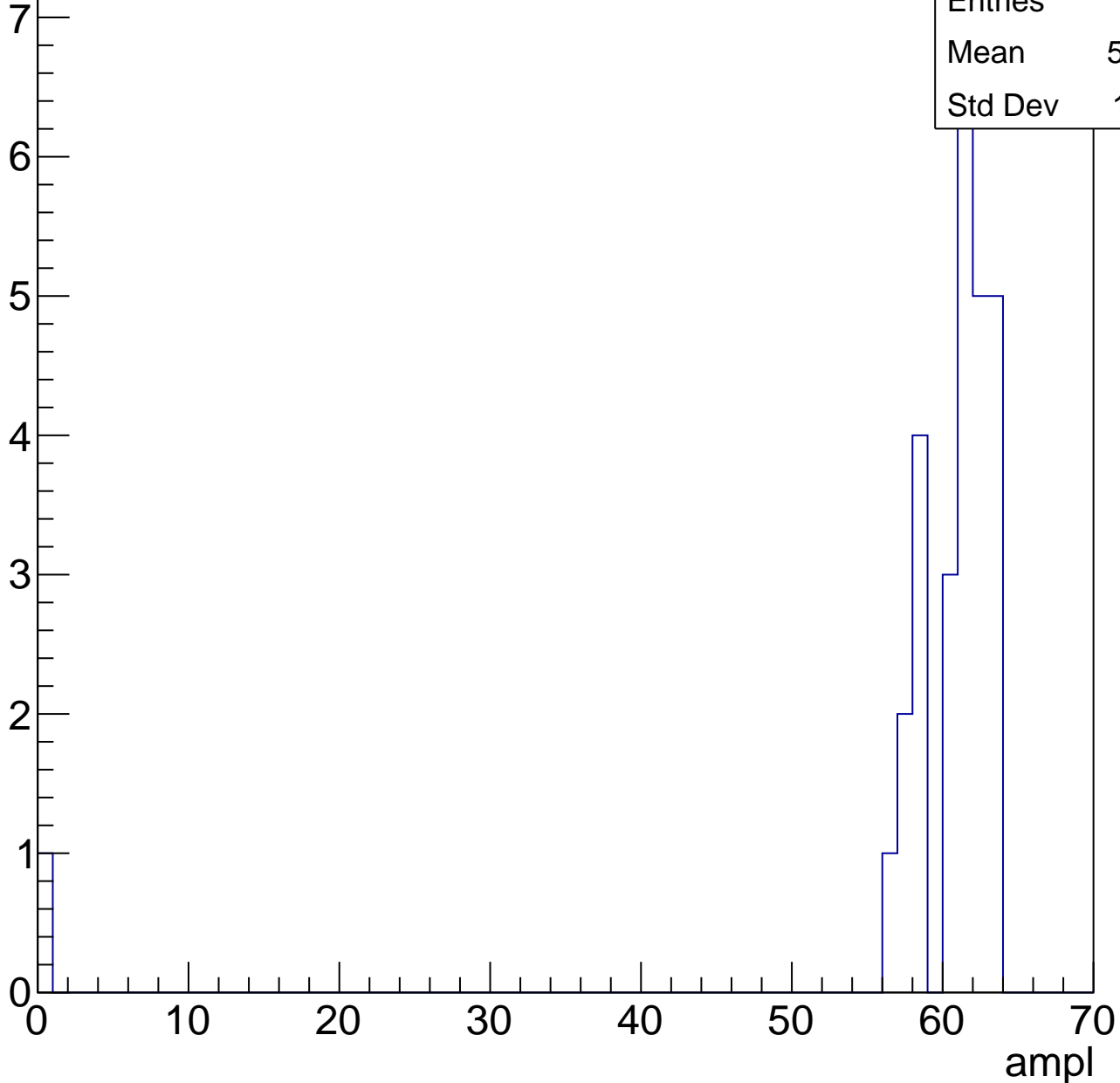


# B1L103S, U1-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	28
Mean	58.36
Std Dev	11.41





# B1L103S, U1-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

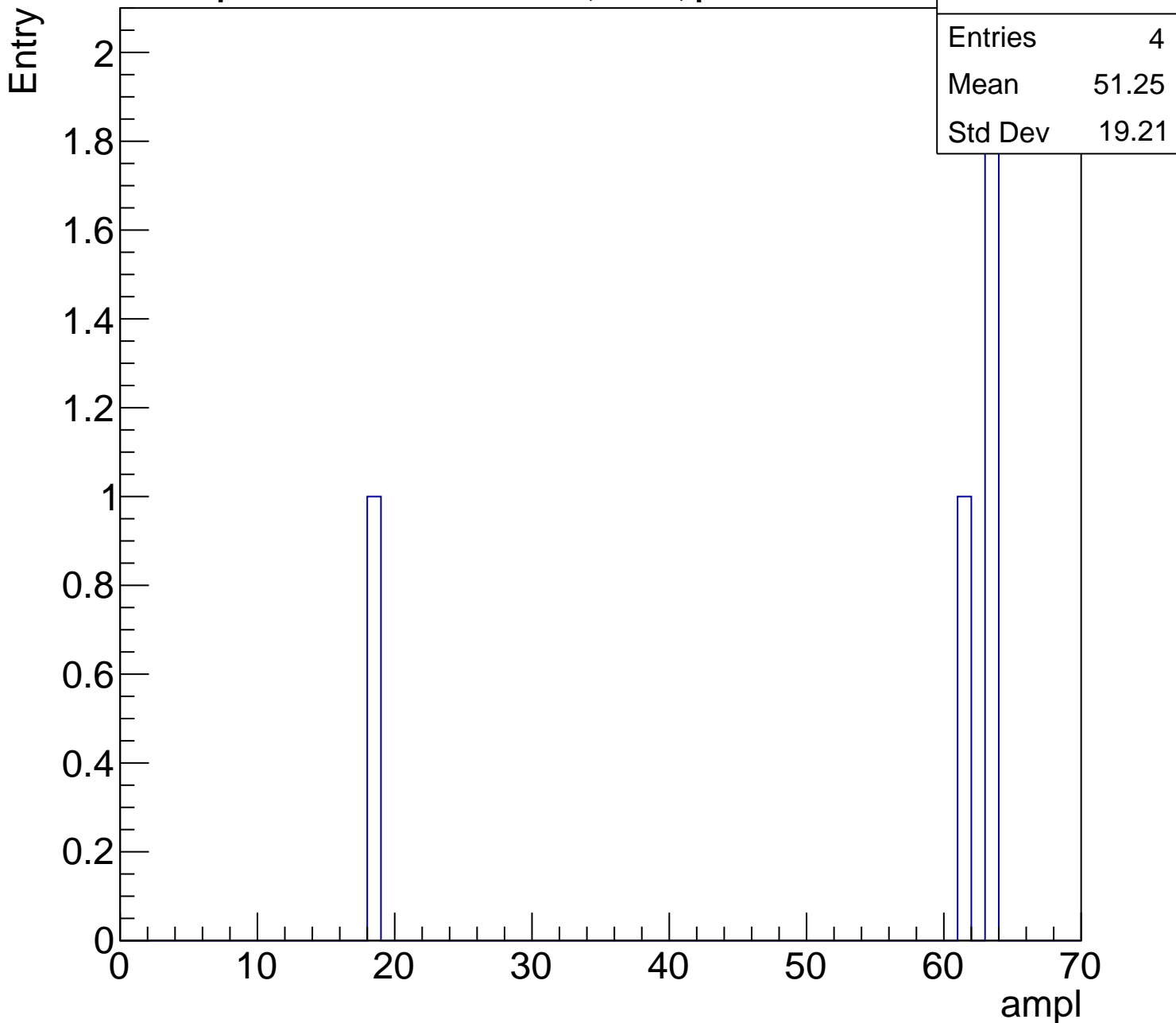
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	51.25
Std Dev	19.21

0 10 20 30 40 50 60 70

ampl



# B1L103S, U1-ch11, adc0

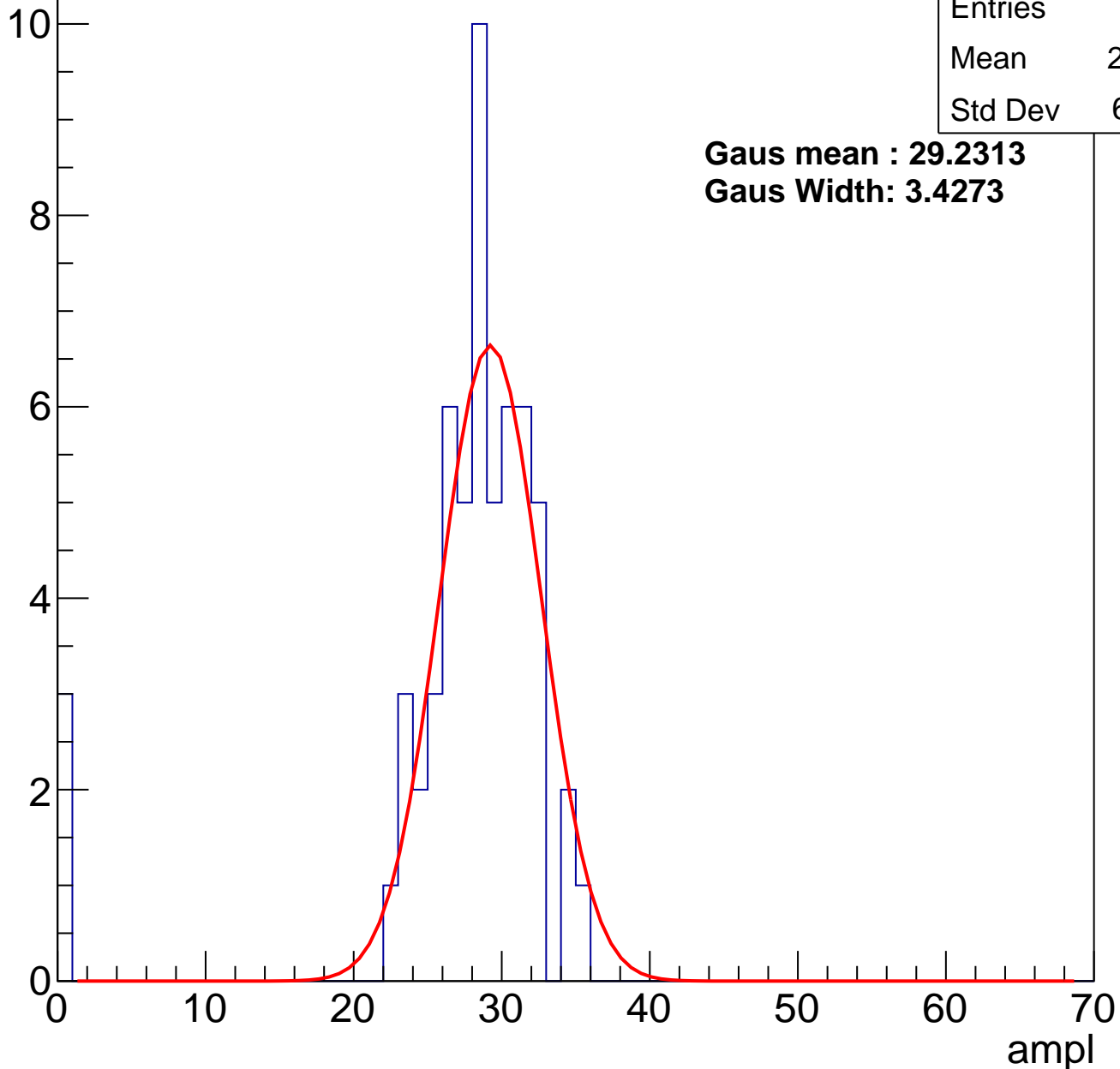
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	58
Mean	26.88
Std Dev	6.901

**Gaus mean : 29.2313**

**Gaus Width: 3.4273**

Entry



# B1L103S, U1-ch11, adc1

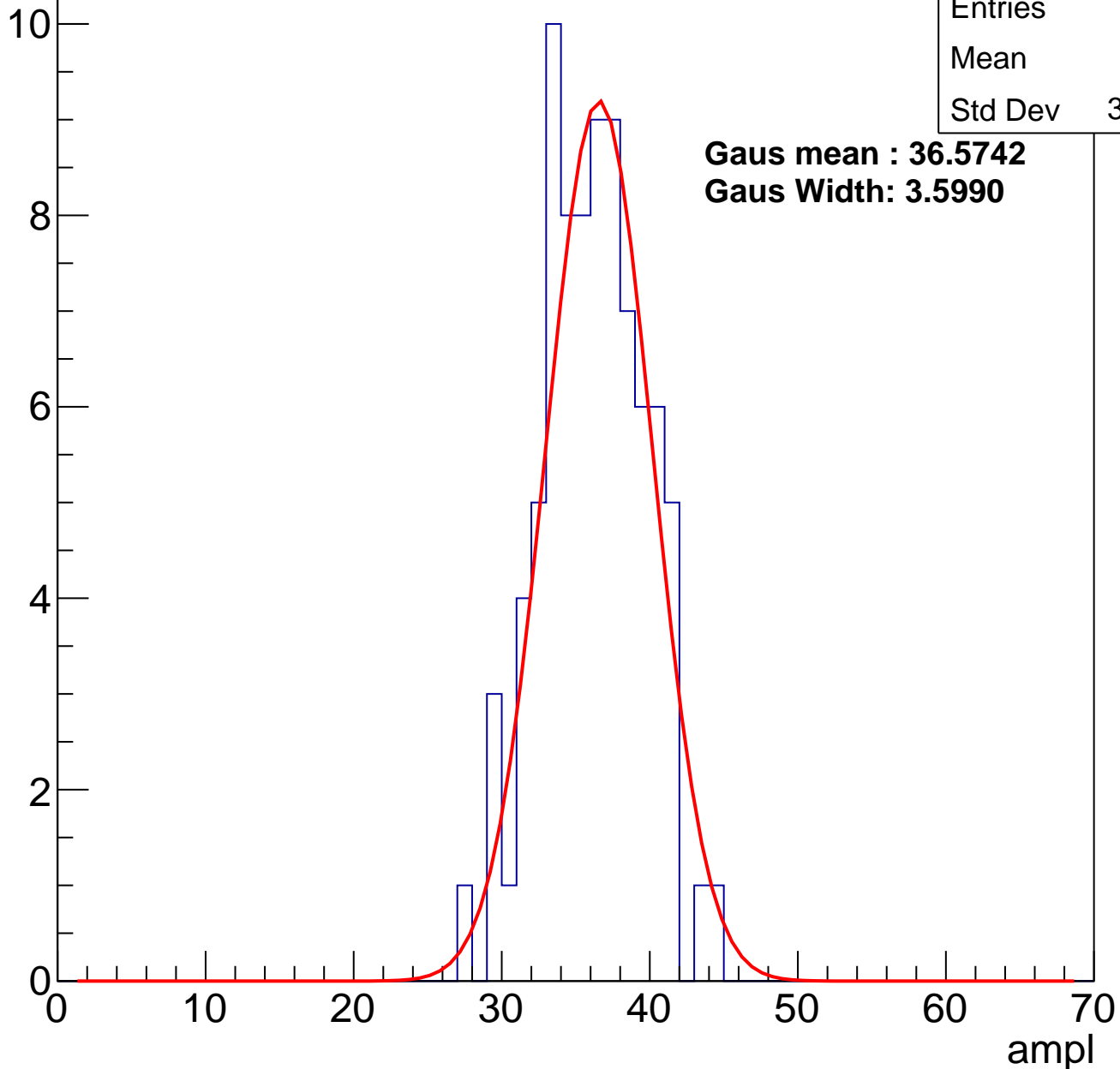
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	84
Mean	35.7
Std Dev	3.436

**Gaus mean : 36.5742**

**Gaus Width: 3.5990**

Entry



# B1L103S, U1-ch11, adc2

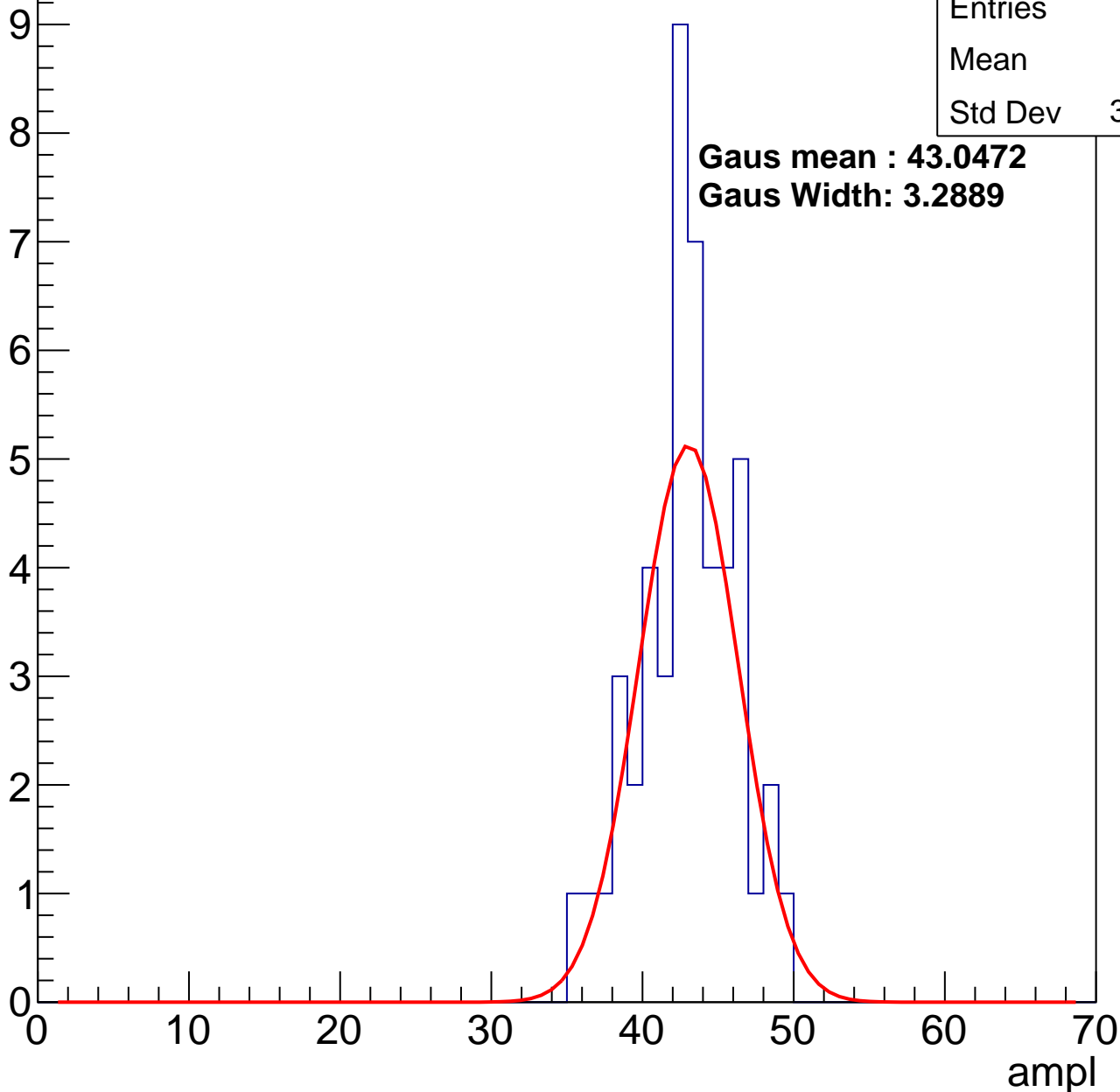
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	42.5
Std Dev	3.122

**Gaus mean : 43.0472**

**Gaus Width: 3.2889**

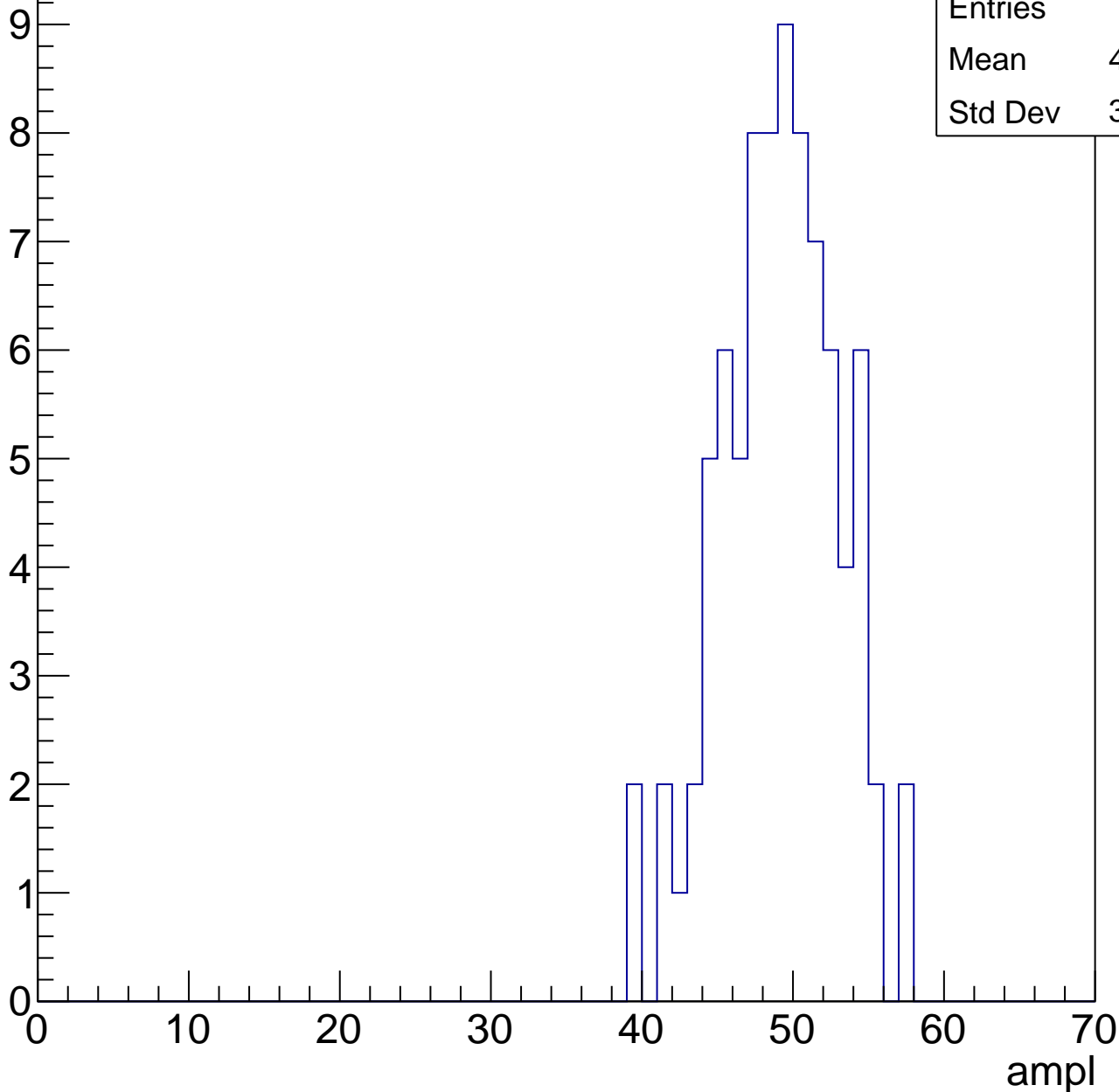


# B1L103S, U1-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	48.65
Std Dev	3.879

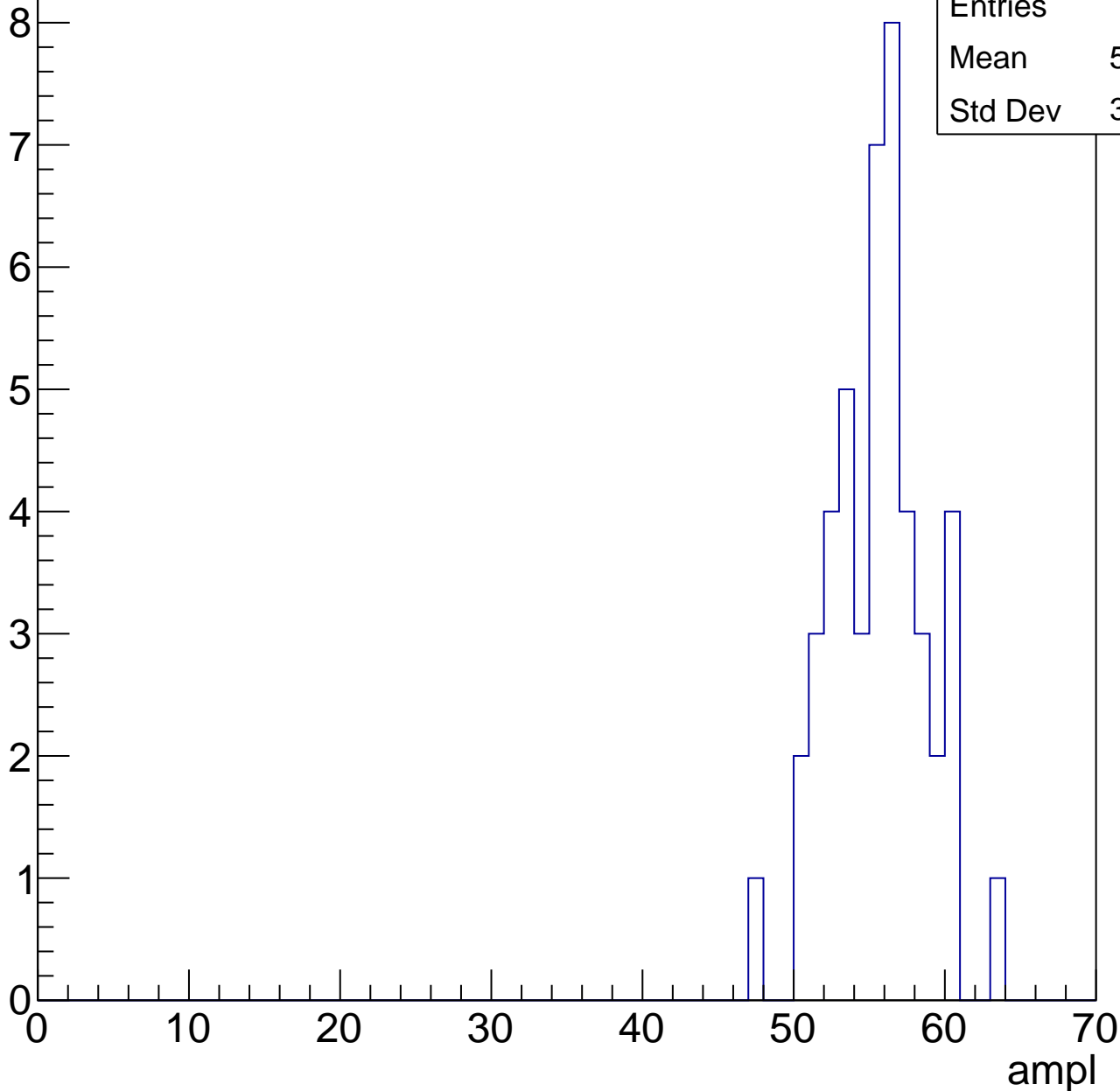


# B1L103S, U1-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

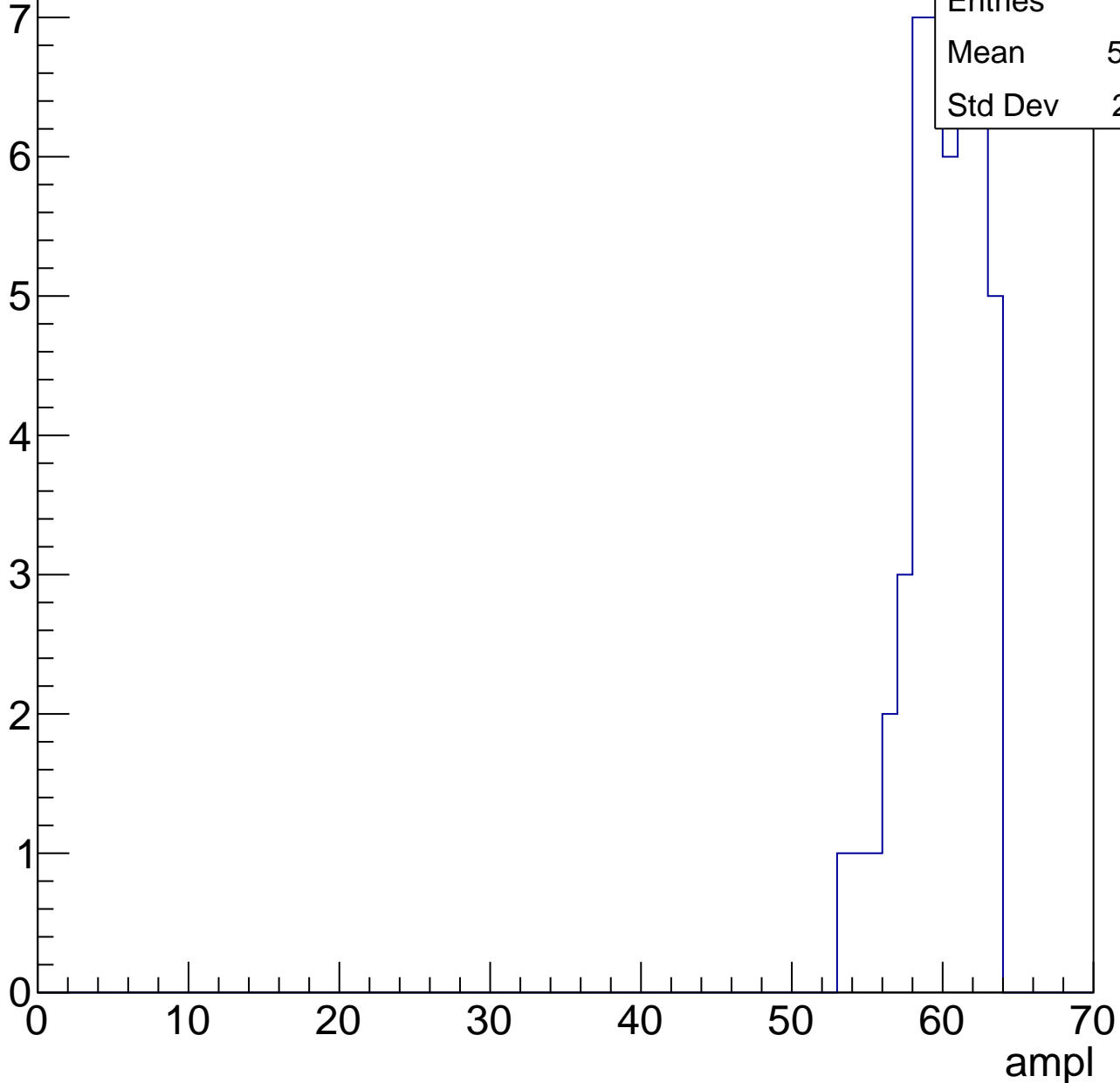
Entries	47
Mean	55.13
Std Dev	3.153



# B1L103S, U1-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

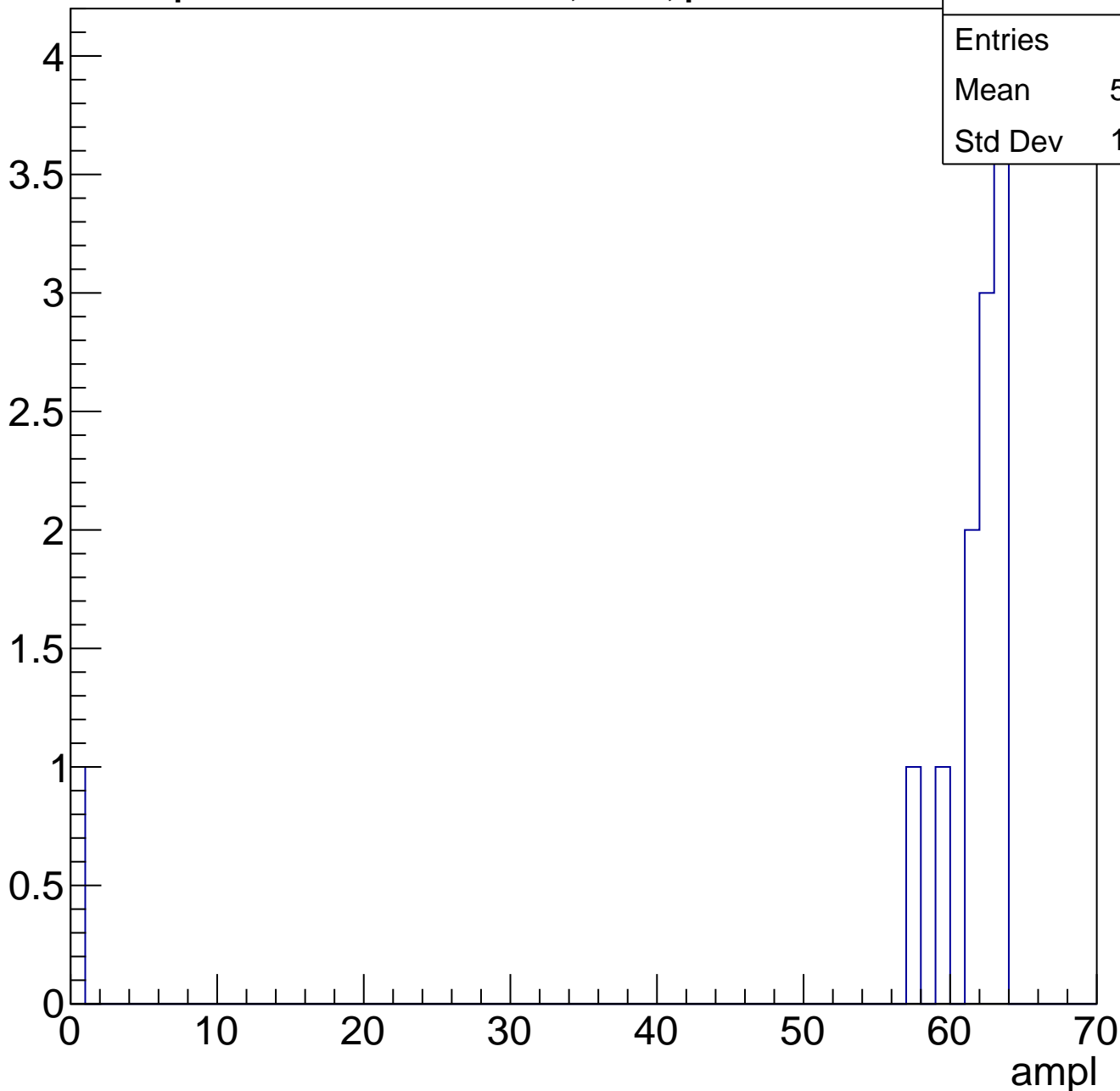


Entries	47
Mean	59.57
Std Dev	2.421

# B1L103S, U1-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	12
Mean	56.33
Std Dev	17.07



# B1L103S, U1-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch12, adc0

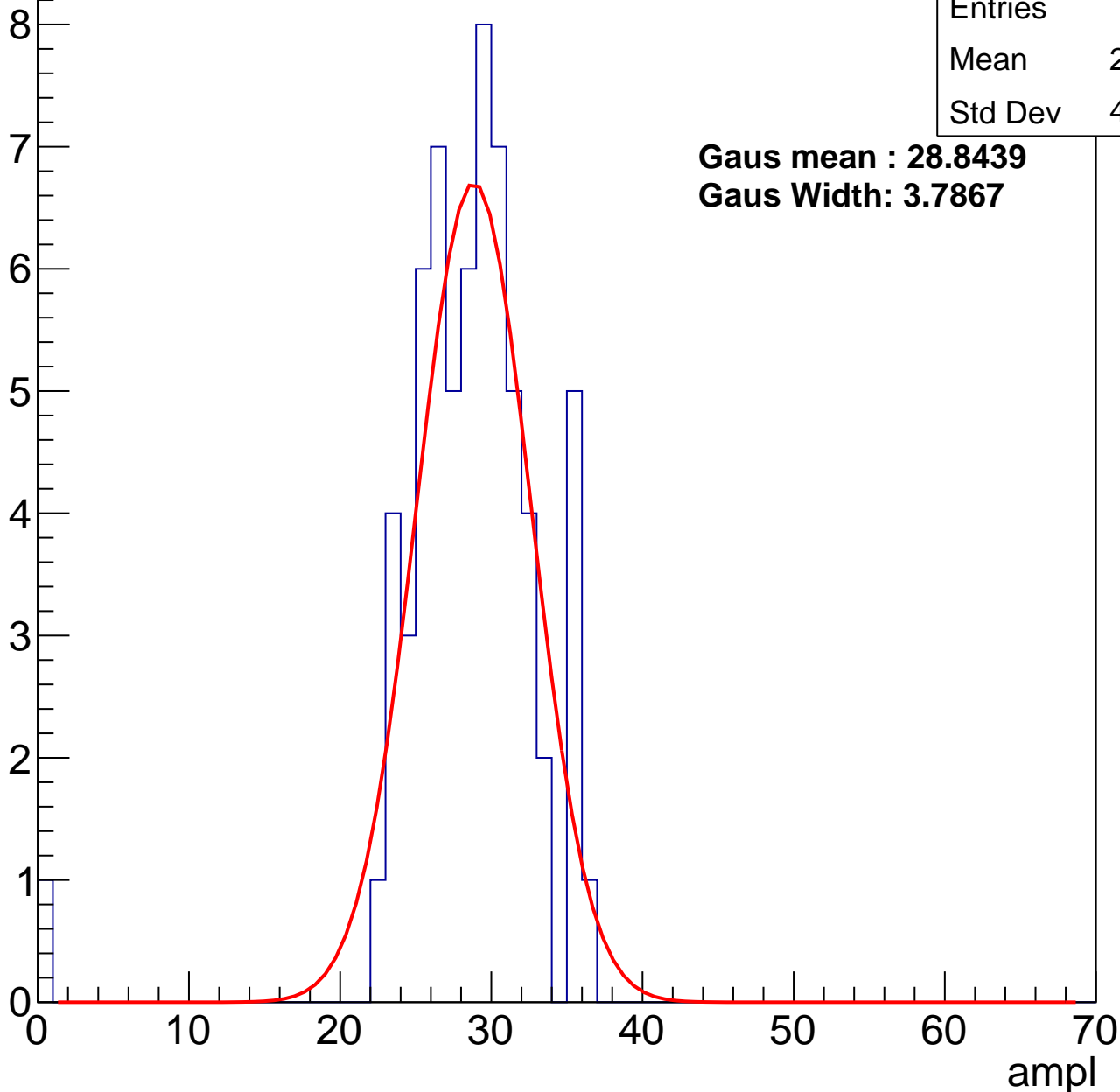
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	28.05
Std Dev	4.897

**Gaus mean : 28.8439**

**Gaus Width: 3.7867**



# B1L103S, U1-ch12, adc1

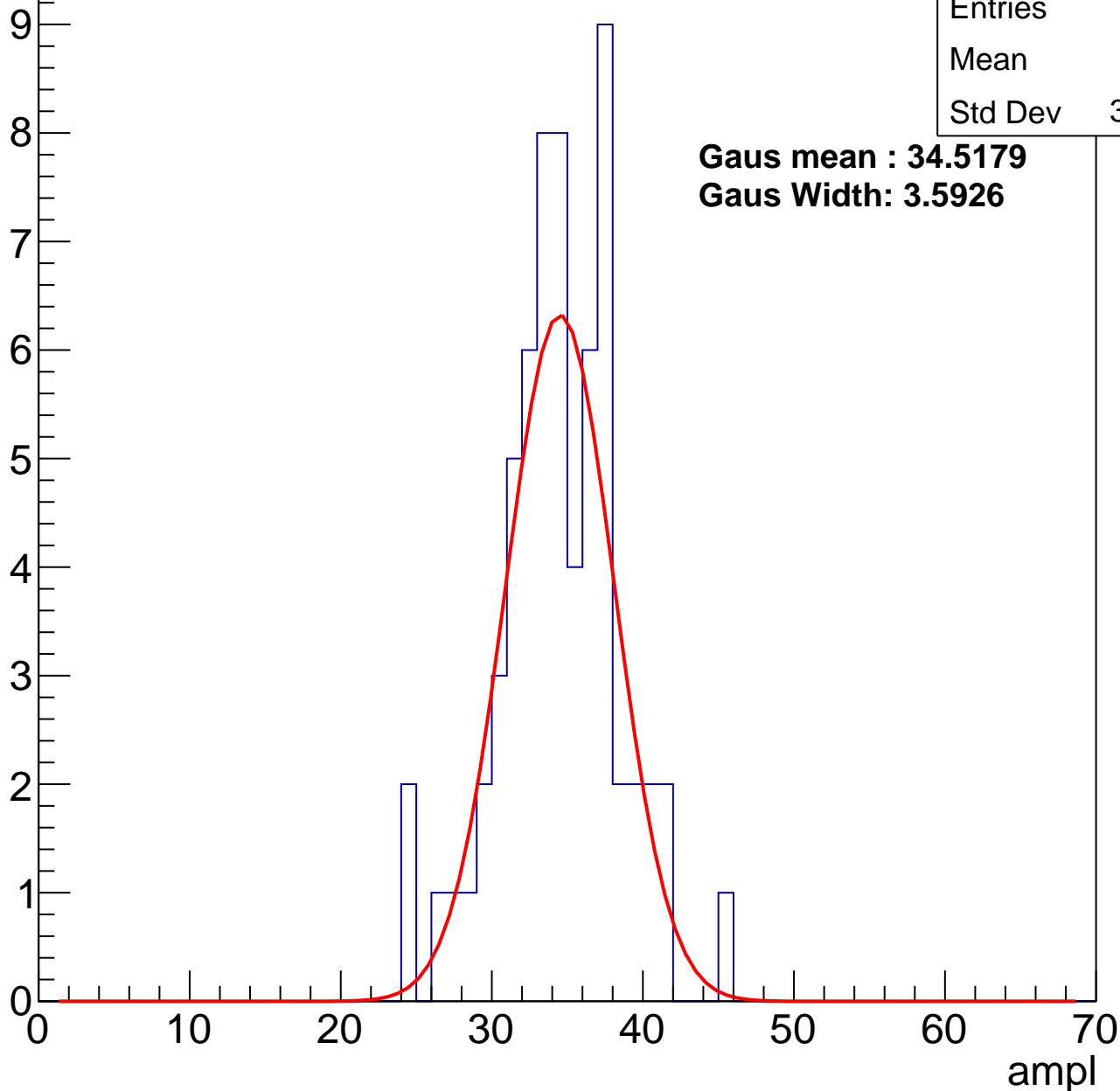
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	34
Std Dev	3.934

**Gaus mean : 34.5179**

**Gaus Width: 3.5926**



# B1L103S, U1-ch12, adc2

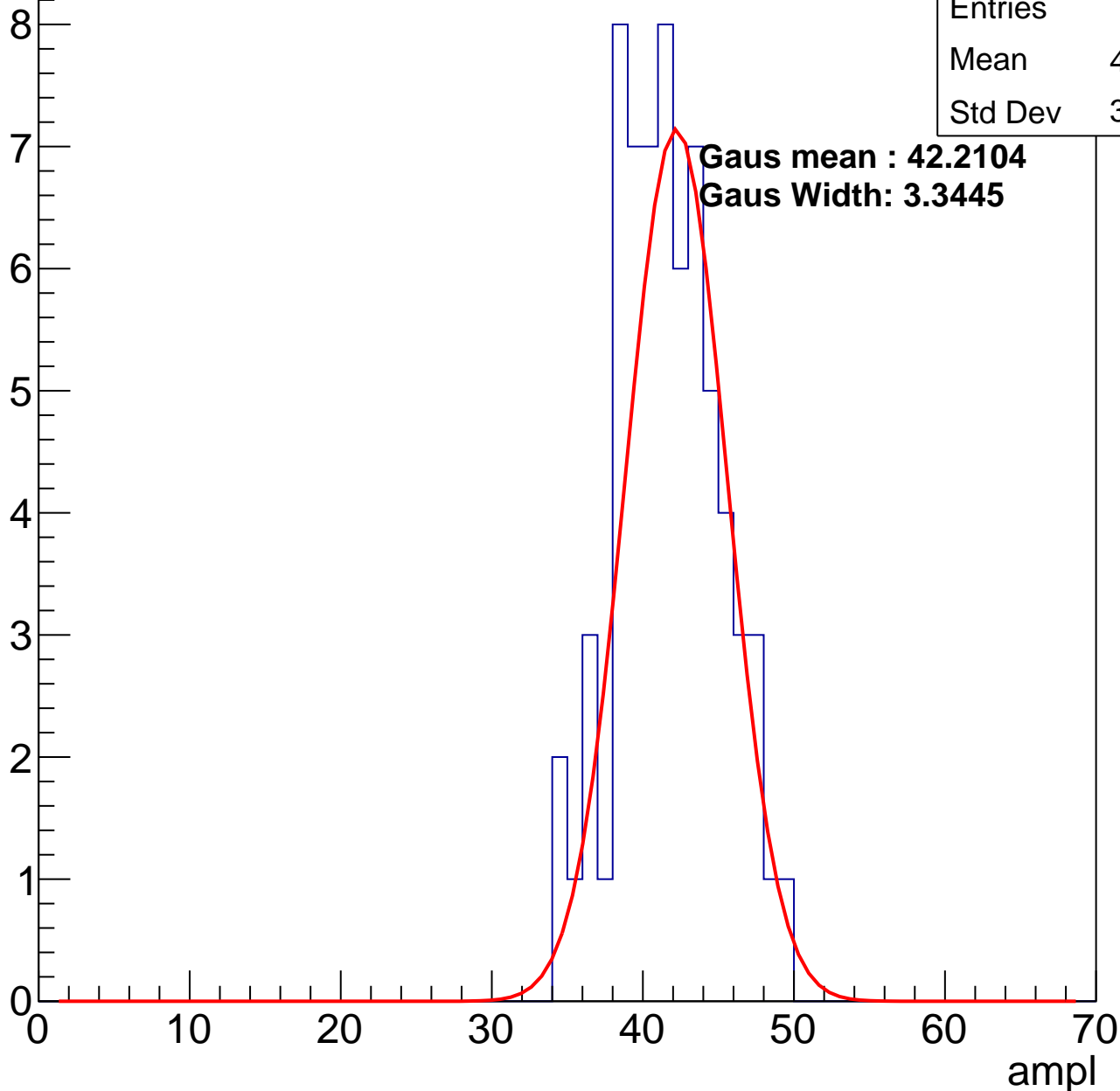
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	41.22
Std Dev	3.385

**Gaus mean : 42.2104**

**Gaus Width: 3.3445**

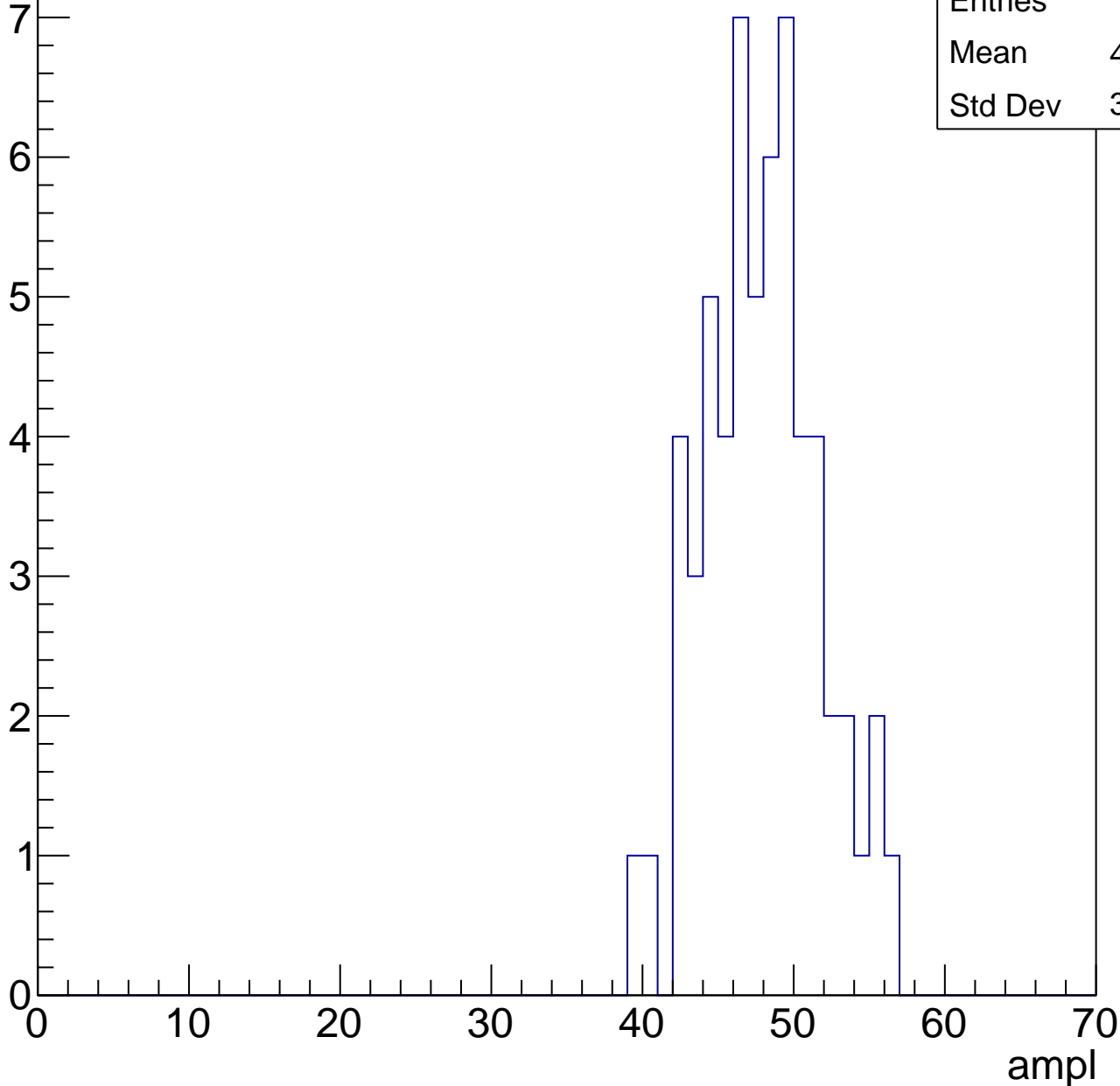


# B1L103S, U1-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	47.42
Std Dev	3.756

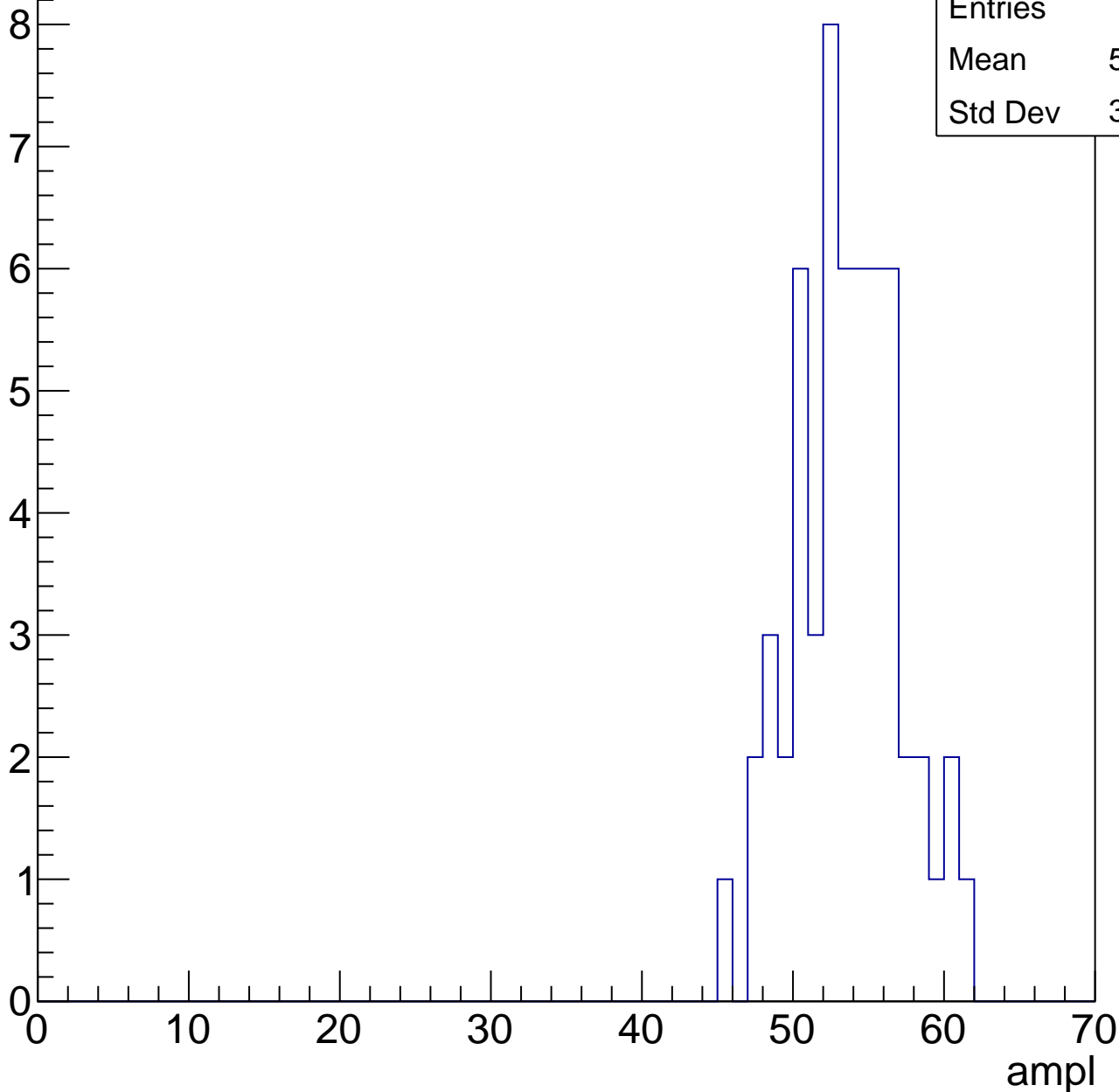


# B1L103S, U1-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

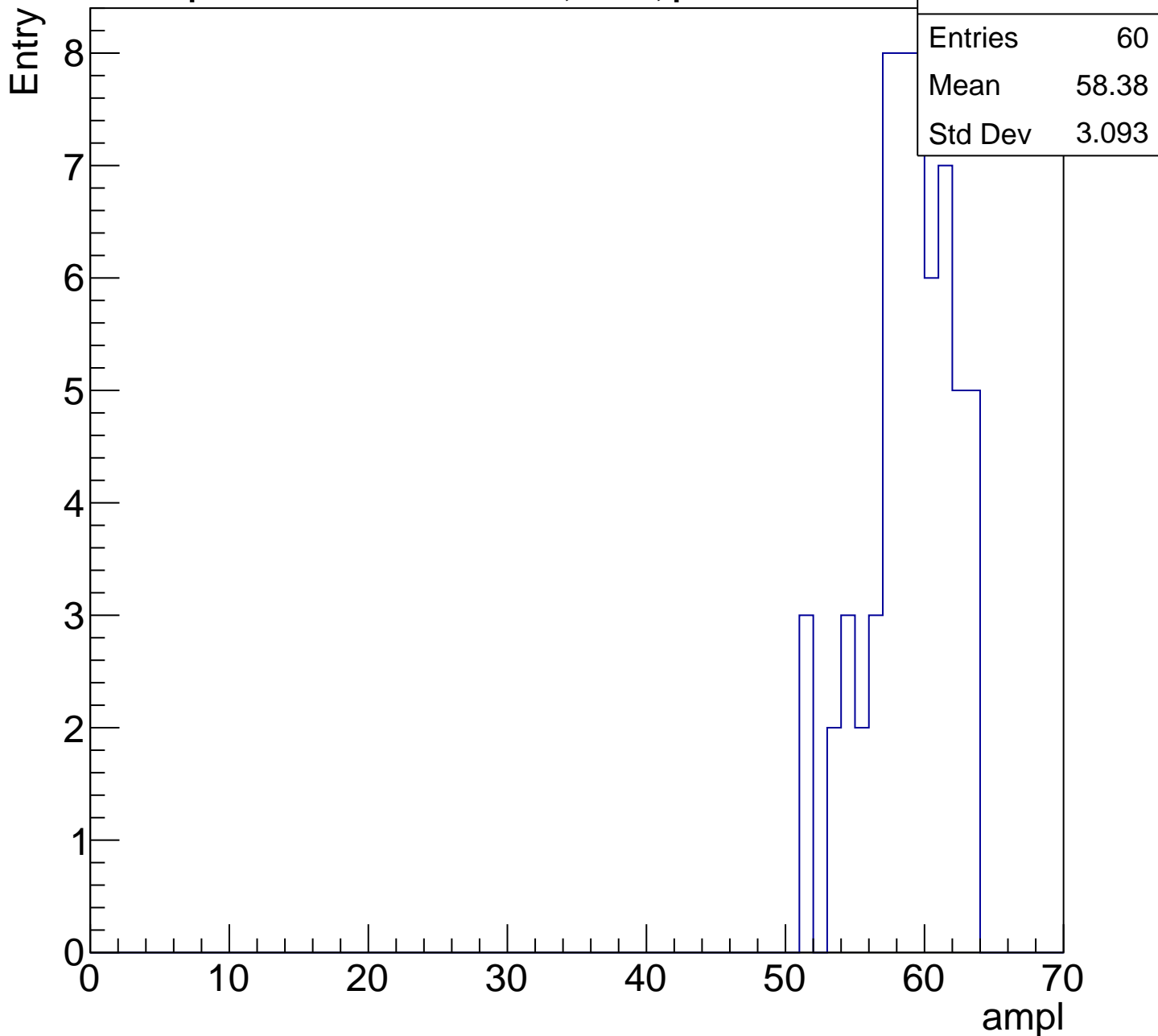
Entry

Entries	57
Mean	53.12
Std Dev	3.454



# B1L103S, U1-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

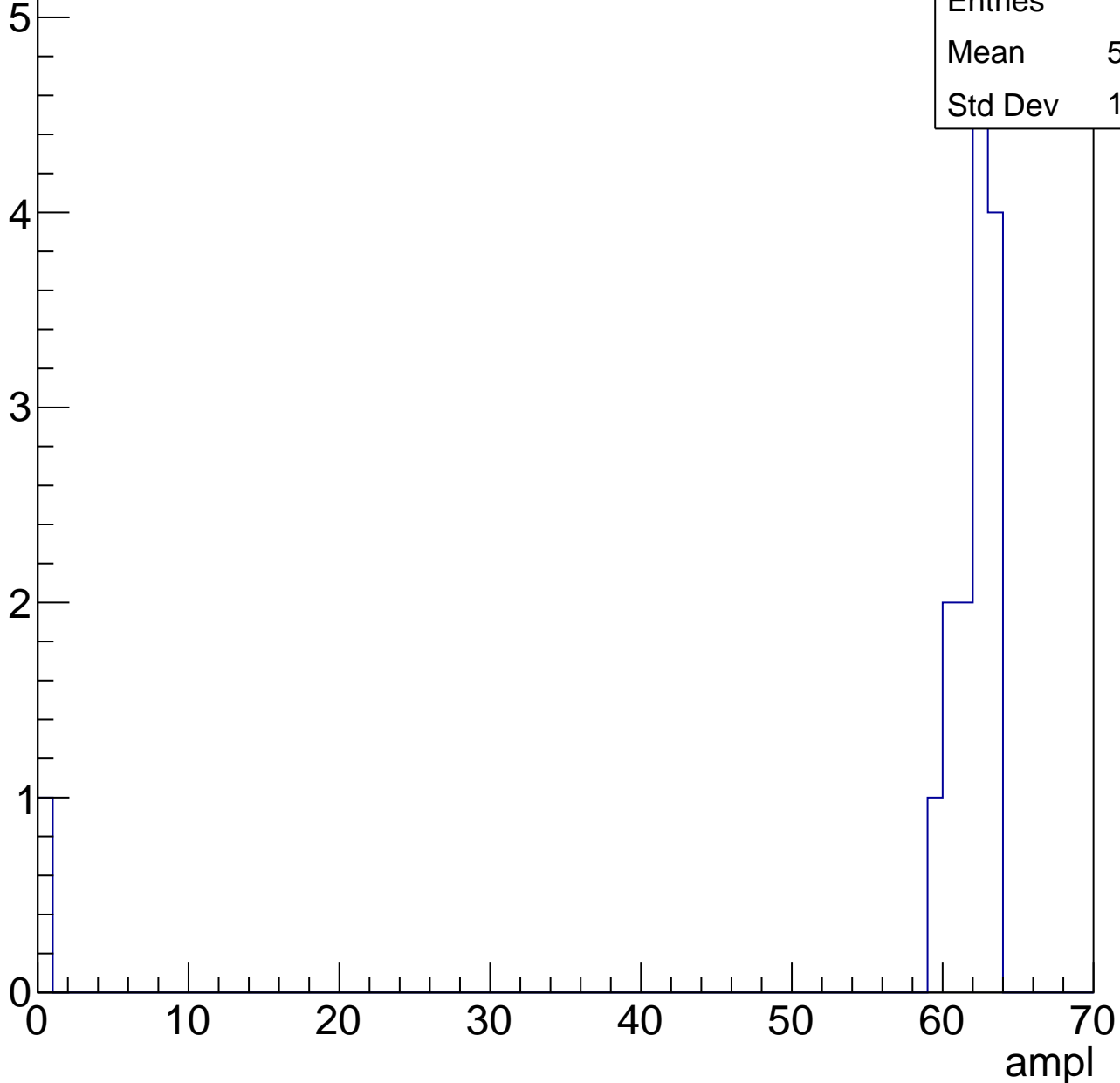


# B1L103S, U1-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	15
Mean	57.53
Std Dev	15.42

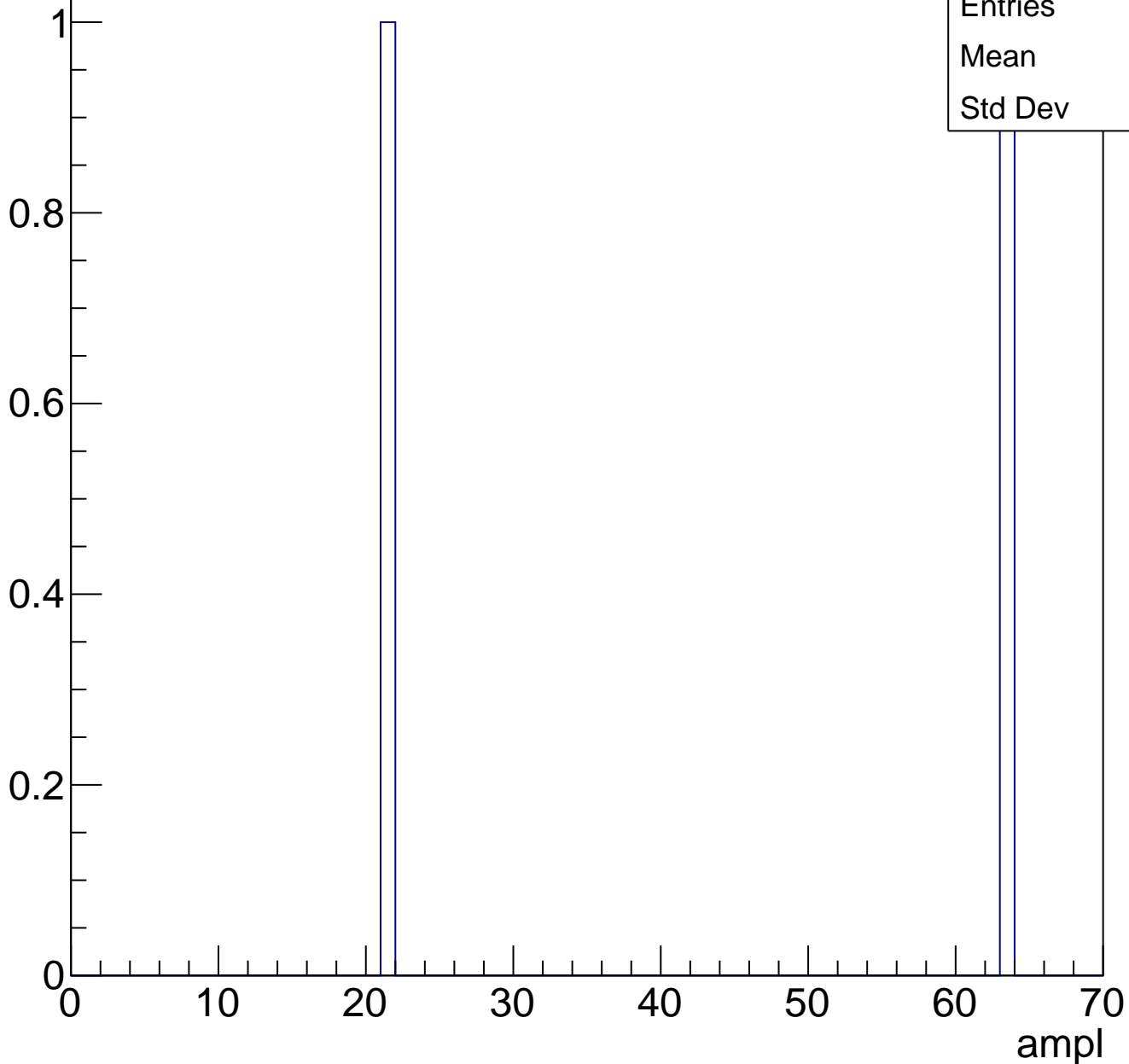




# B1L103S, U1-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch13, adc0

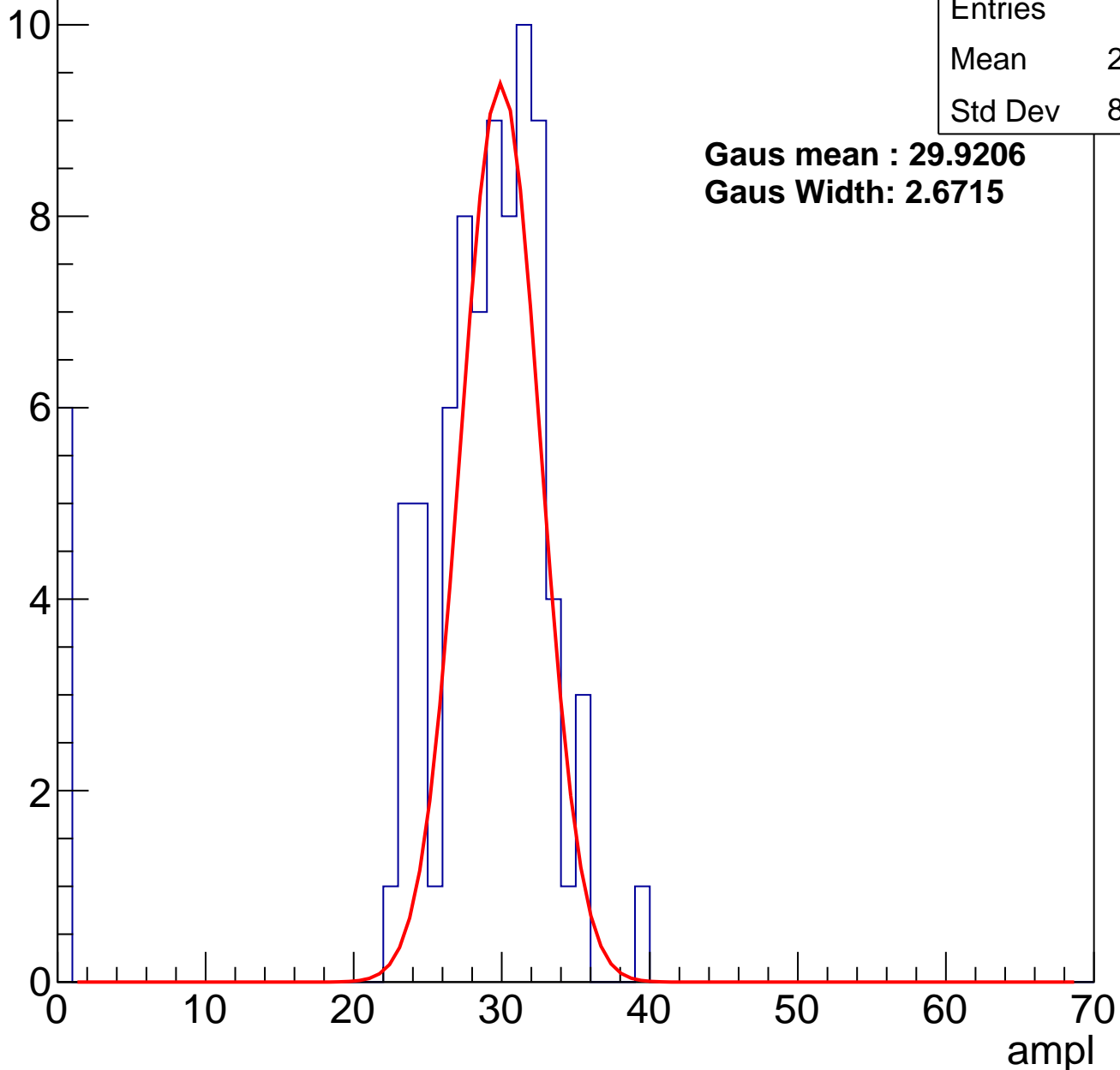
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	84
Mean	26.89
Std Dev	8.137

**Gaus mean : 29.9206**

**Gaus Width: 2.6715**

Entry



# B1L103S, U1-ch13, adc1

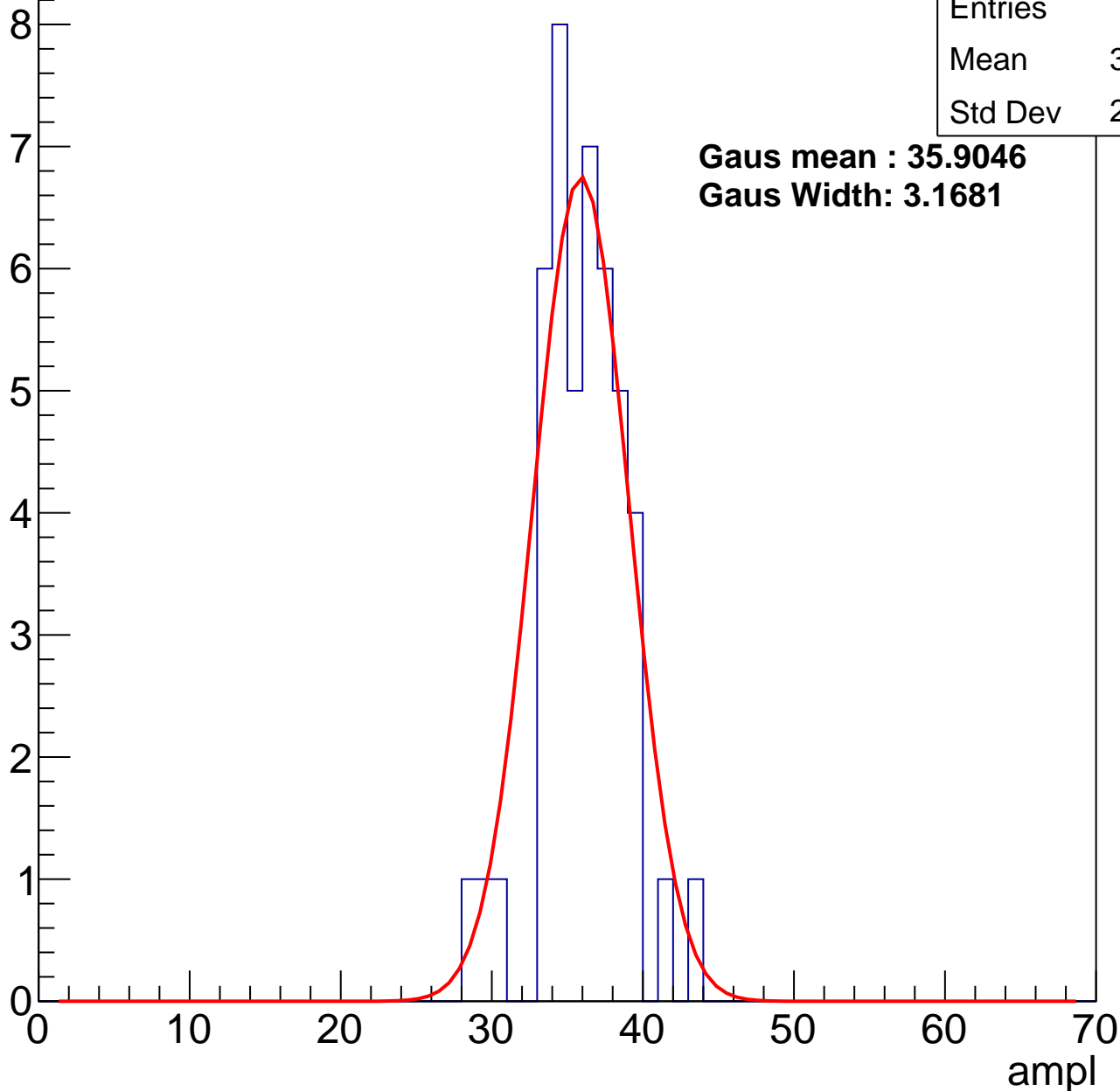
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	35.57
Std Dev	2.826

**Gaus mean : 35.9046**

**Gaus Width: 3.1681**



# B1L103S, U1-ch13, adc2

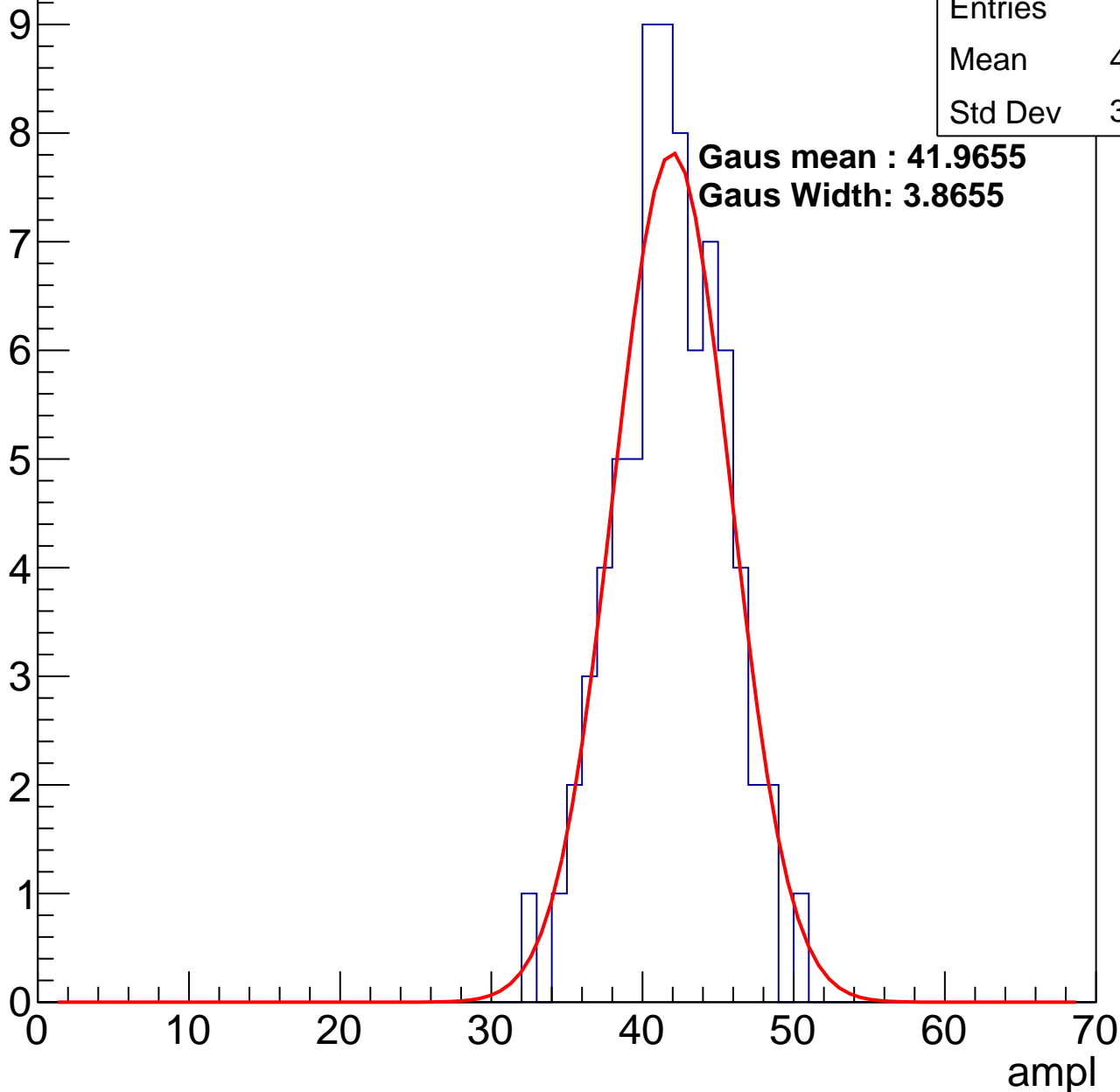
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	41.36
Std Dev	3.554

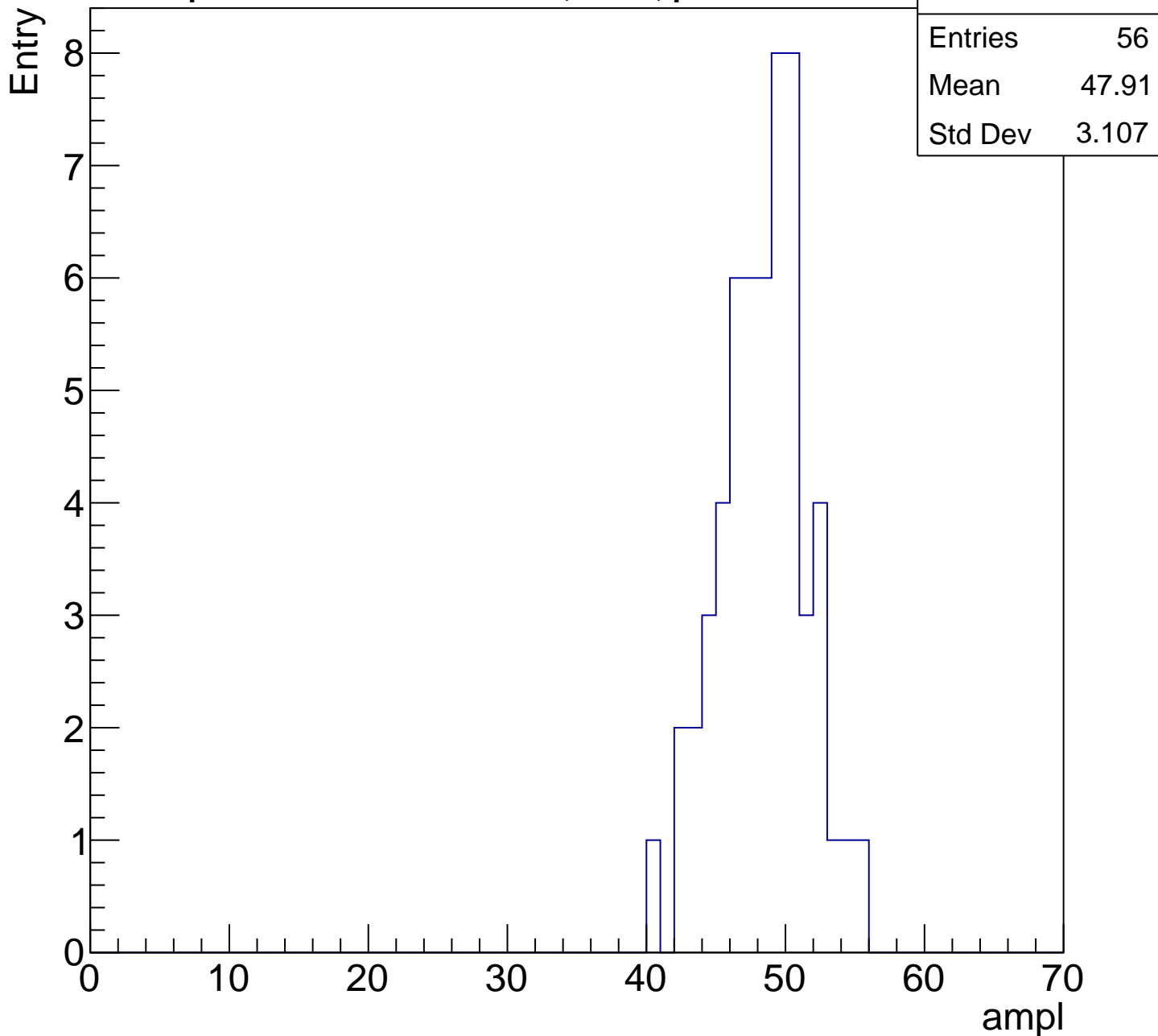
**Gaus mean : 41.9655**

**Gaus Width: 3.8655**



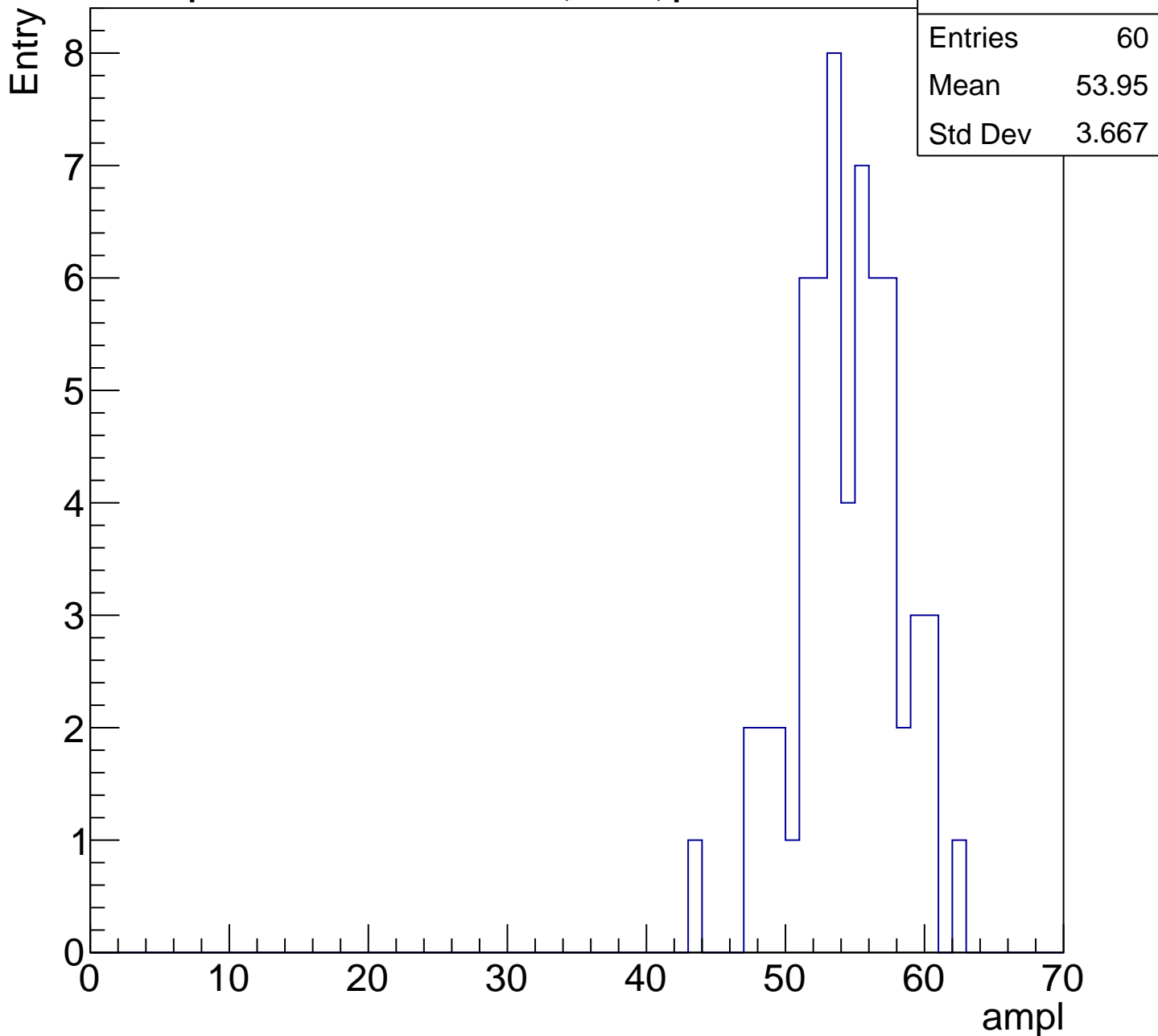
# B1L103S, U1-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U1-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

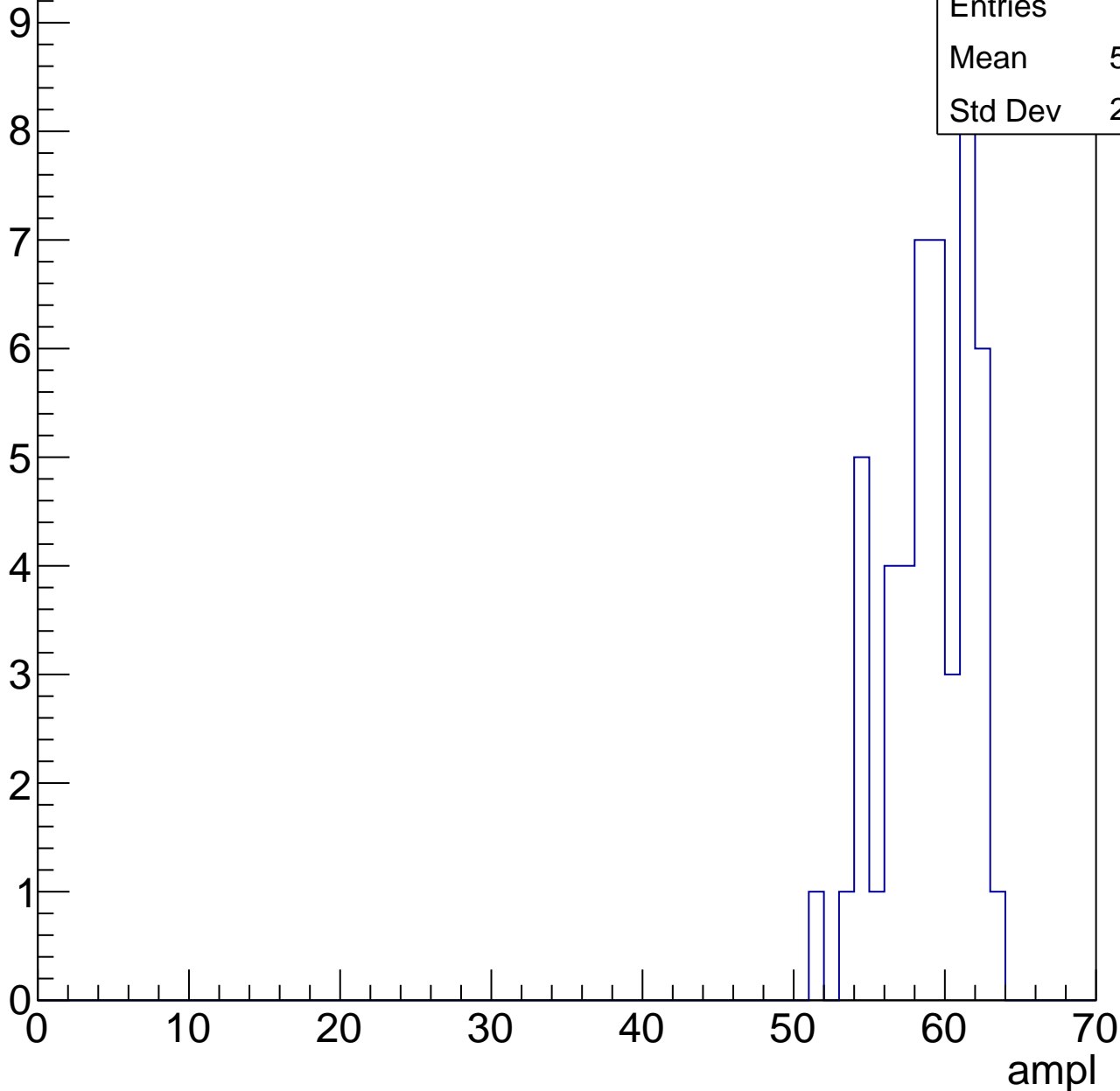


# B1L103S, U1-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	58.45
Std Dev	2.836

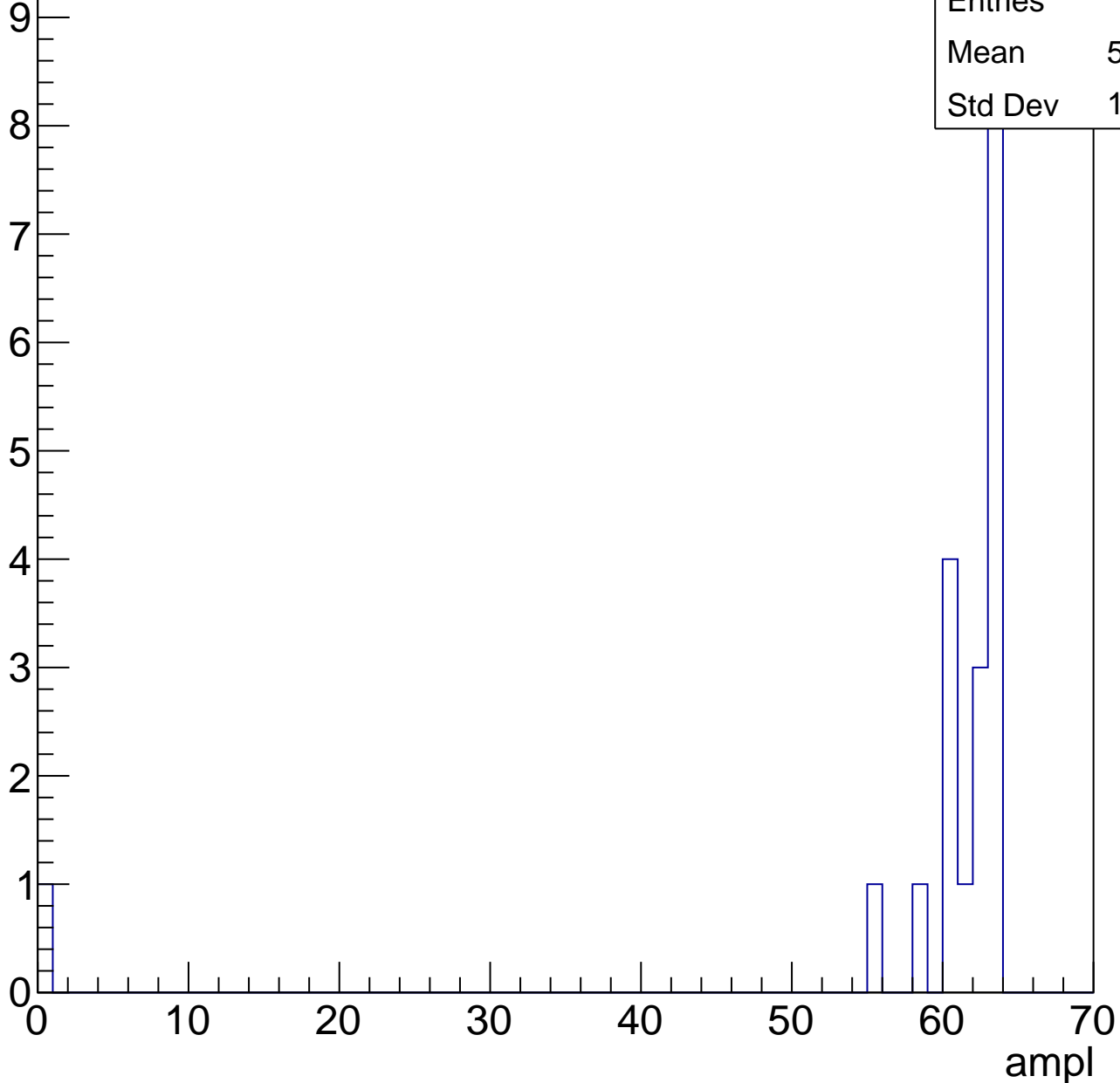


# B1L103S, U1-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	20
Mean	58.35
Std Dev	13.54





# B1L103S, U1-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch14, adc0

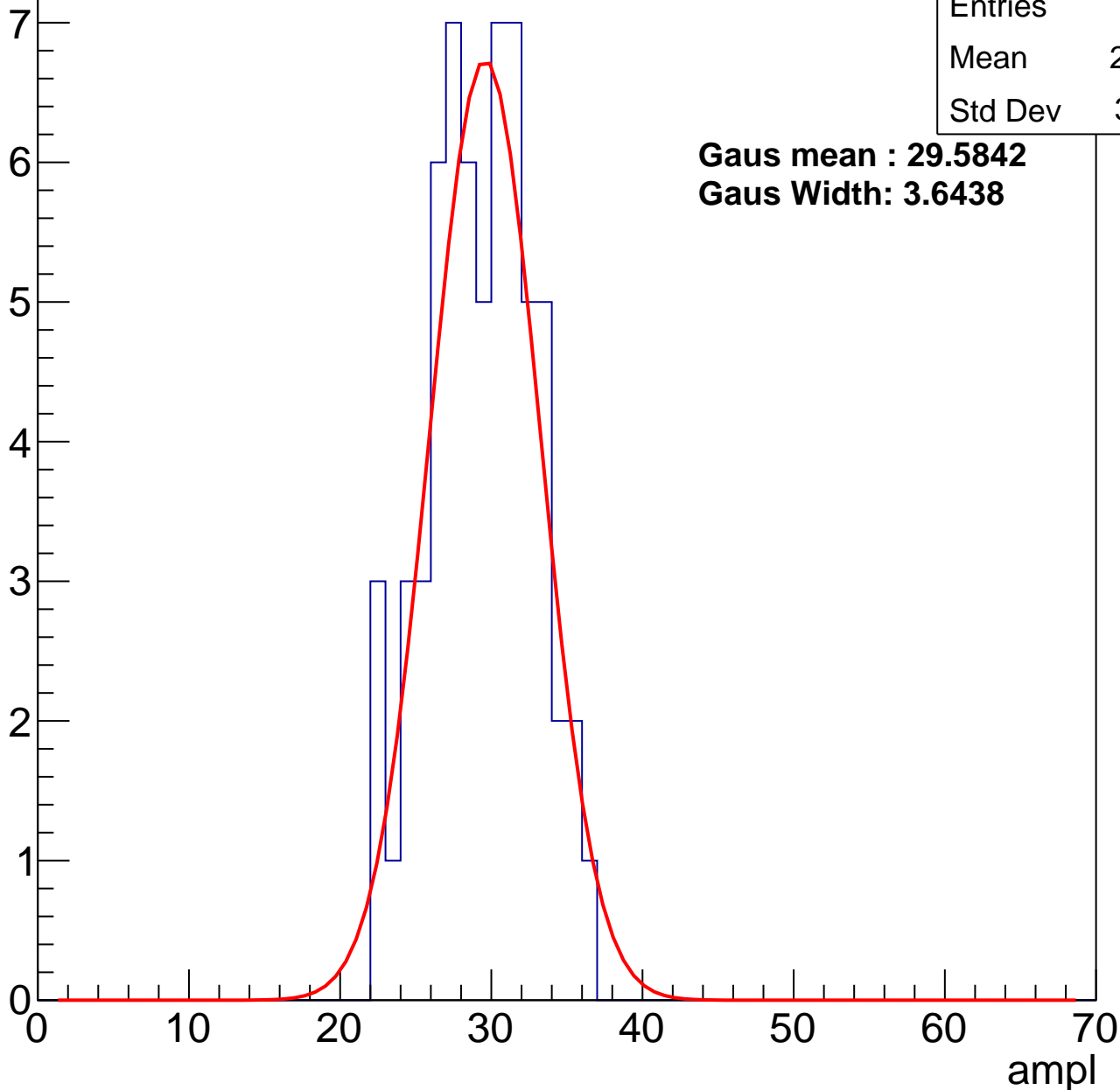
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	28.89
Std Dev	3.391

**Gaus mean : 29.5842**

**Gaus Width: 3.6438**



# B1L103S, U1-ch14, adc1

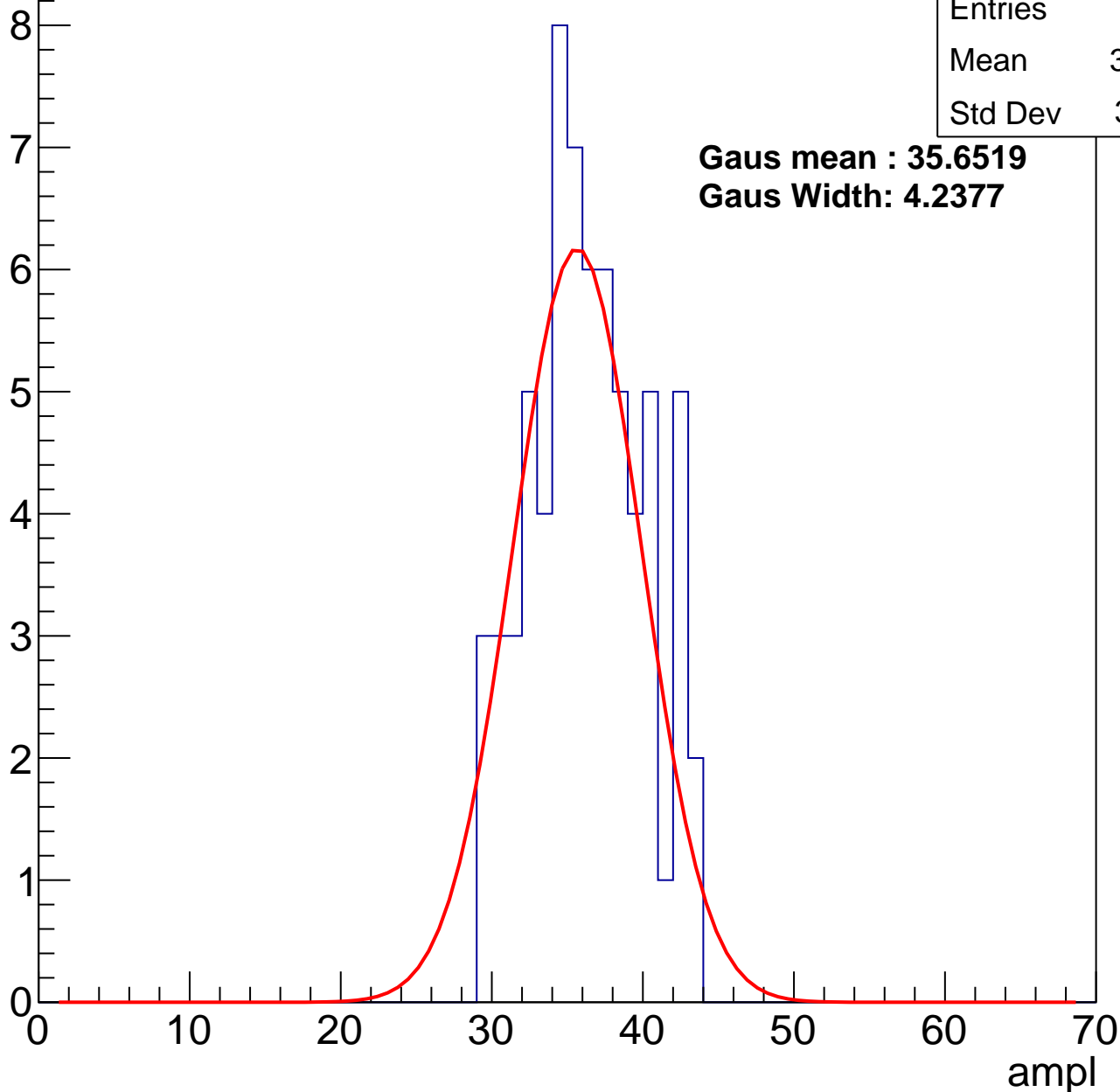
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	35.82
Std Dev	3.721

**Gaus mean : 35.6519**

**Gaus Width: 4.2377**



# B1L103S, U1-ch14, adc2

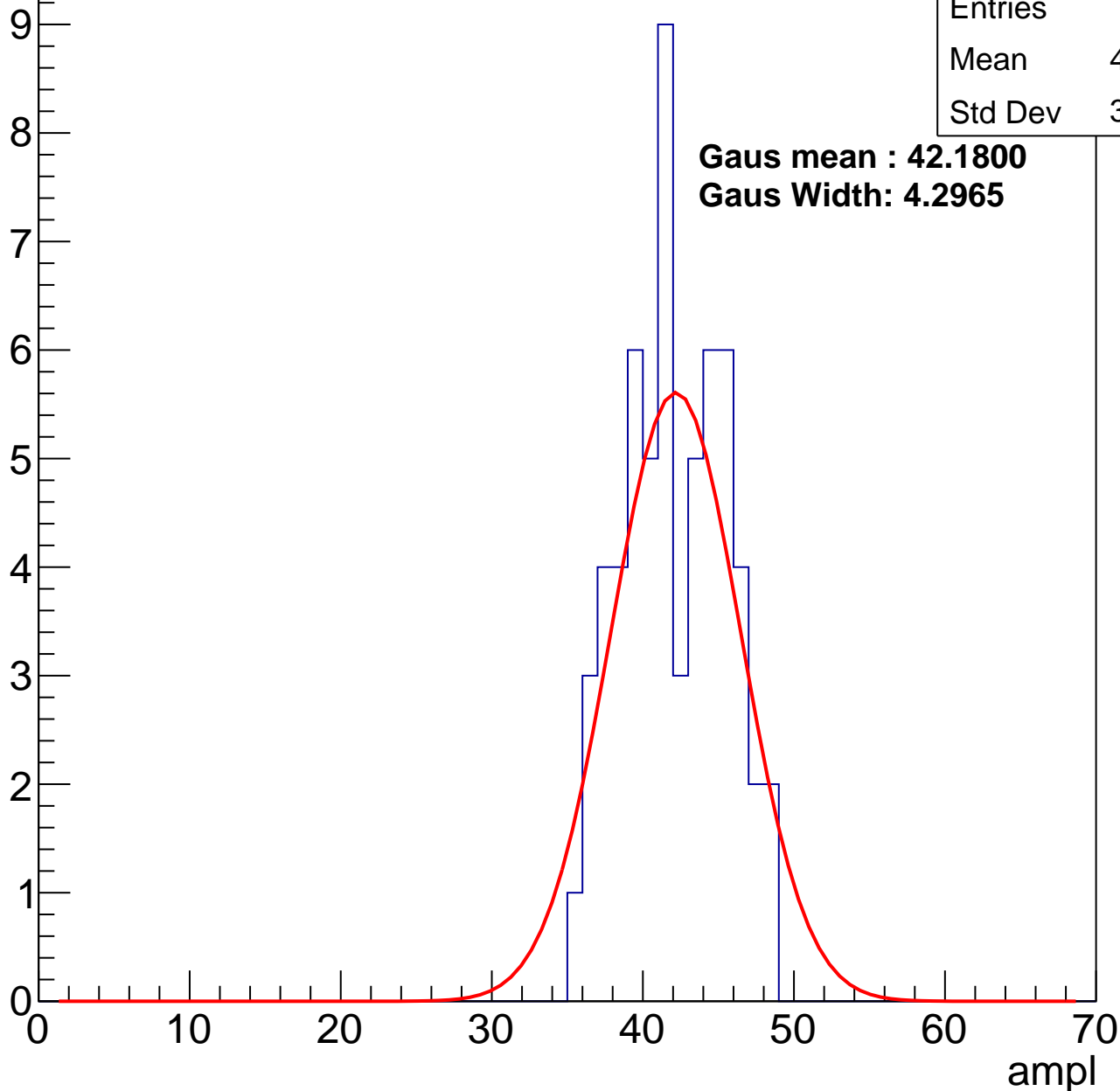
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	41.58
Std Dev	3.323

**Gaus mean : 42.1800**

**Gaus Width: 4.2965**

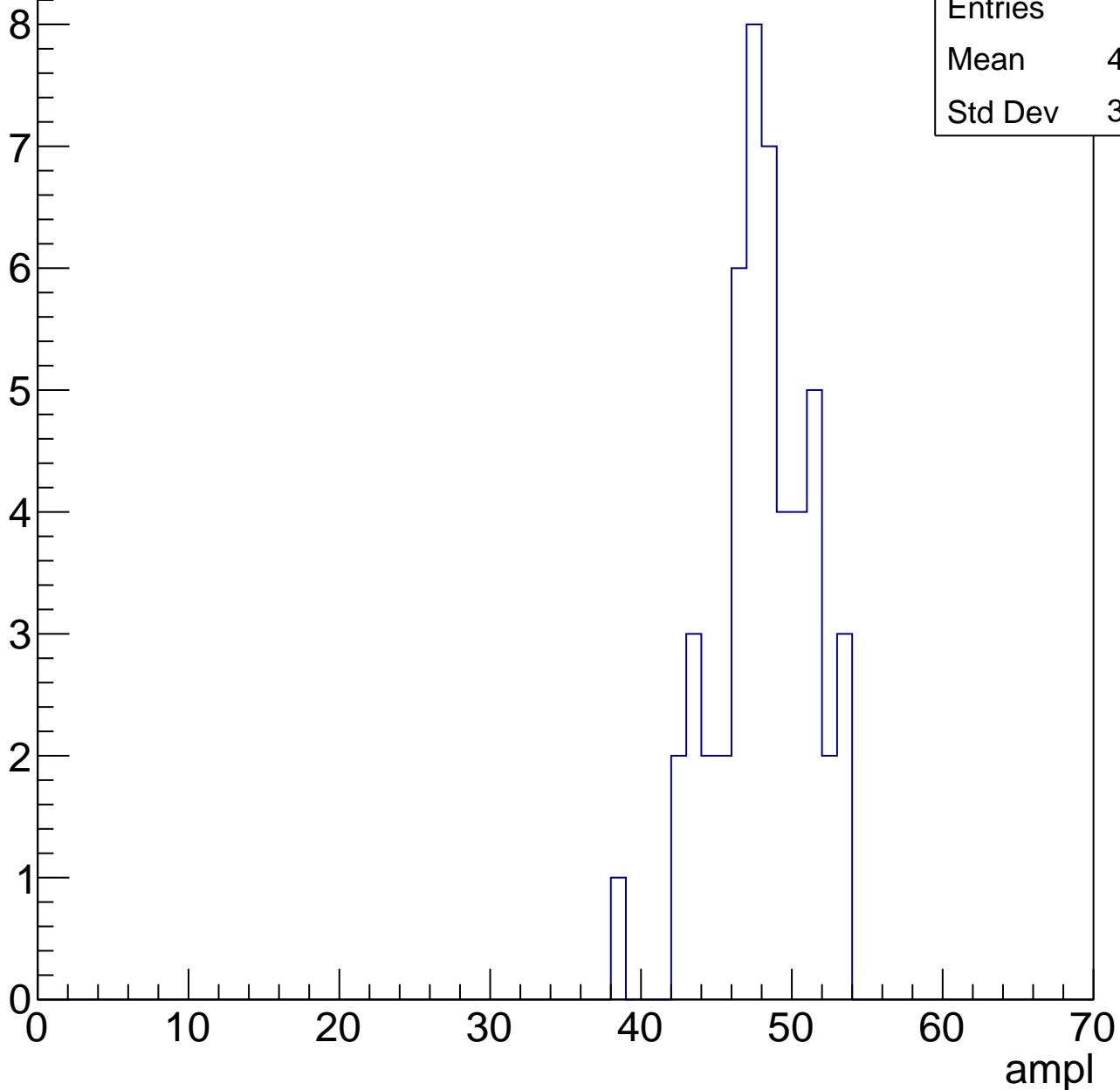


# B1L103S, U1-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	47.57
Std Dev	3.169

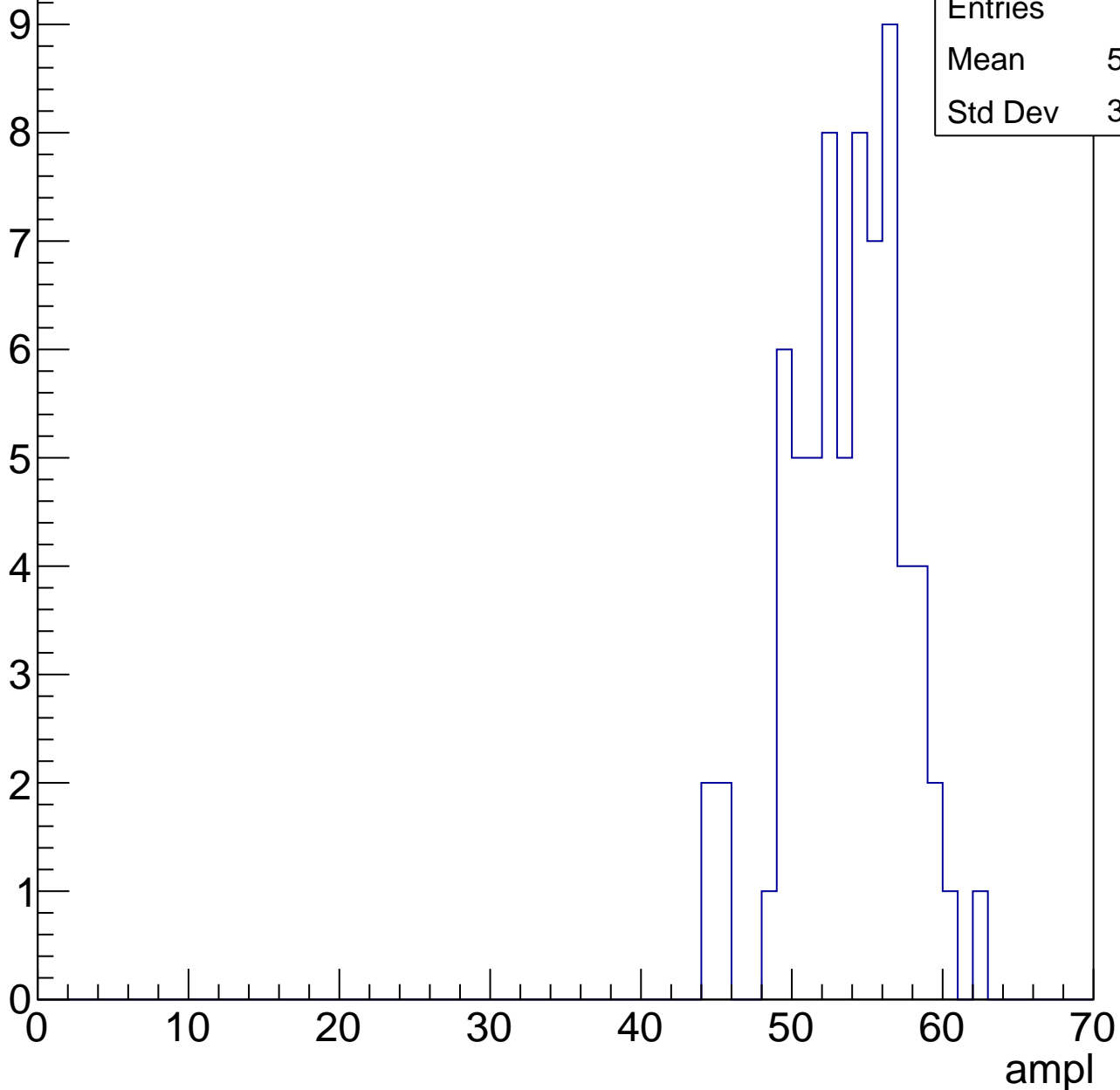


# B1L103S, U1-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	53.24
Std Dev	3.709

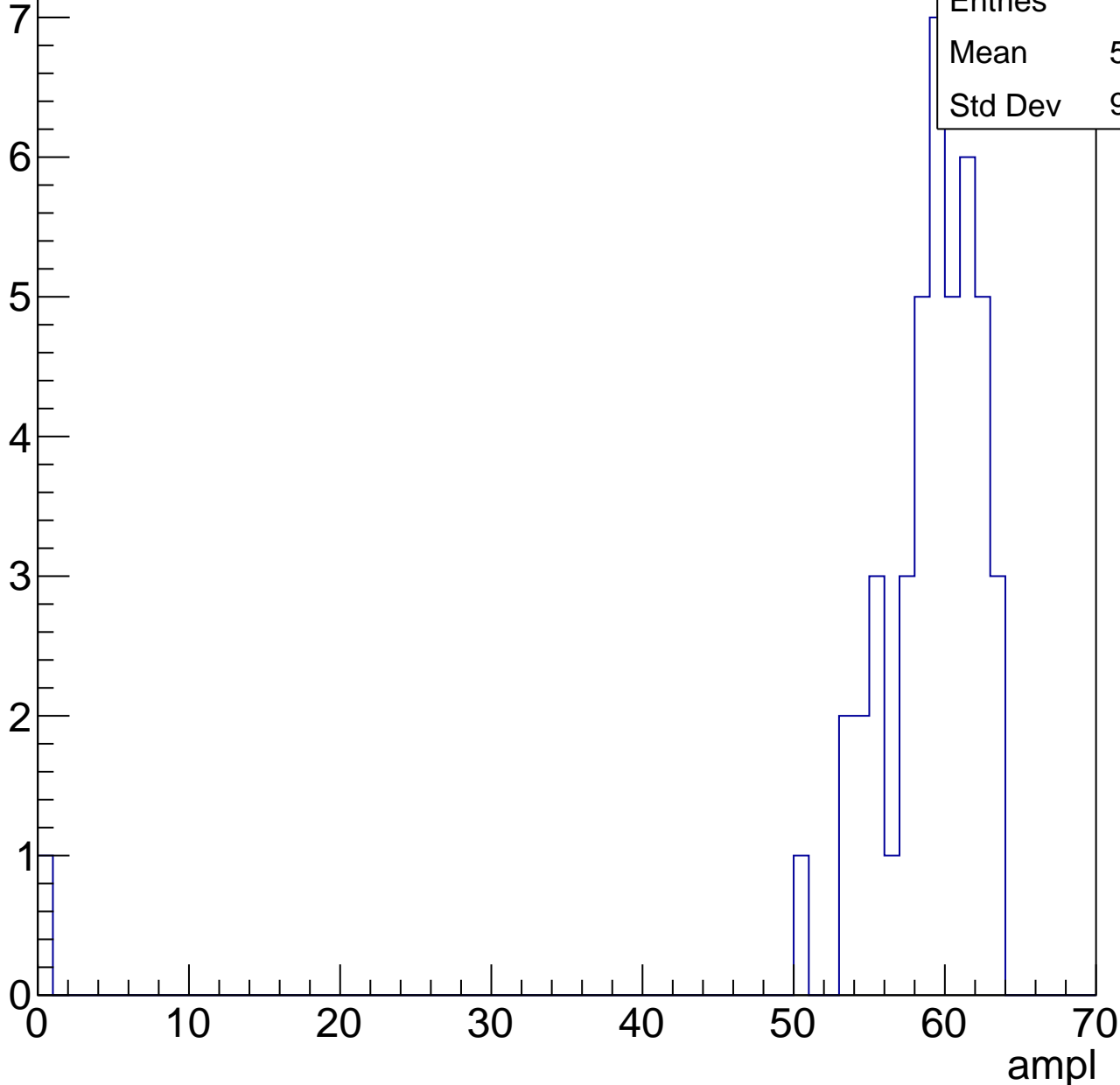


# B1L103S, U1-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	57.36
Std Dev	9.247

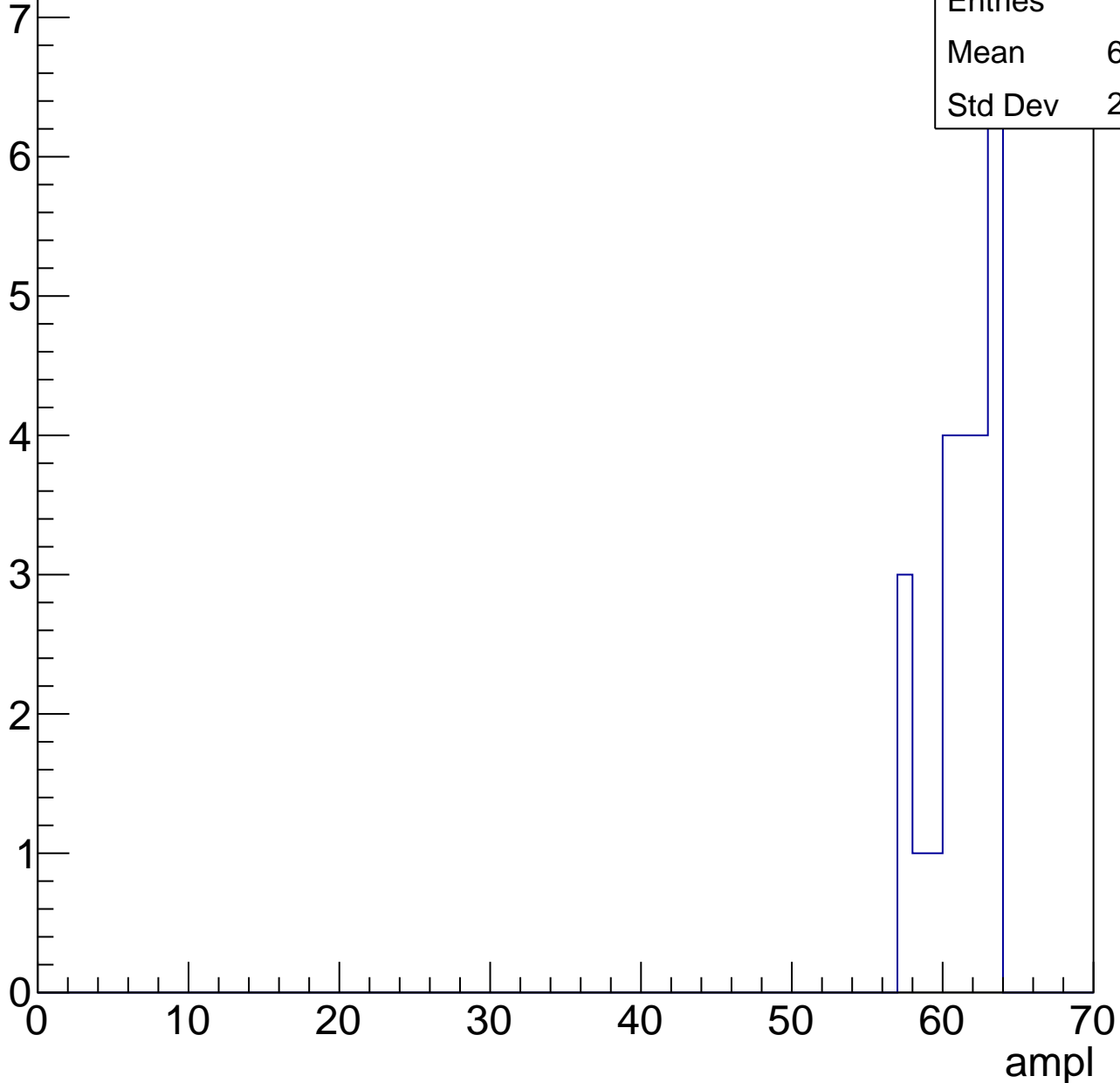


# B1L103S, U1-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	24
Mean	60.88
Std Dev	2.006





# B1L103S, U1-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch15, adc0

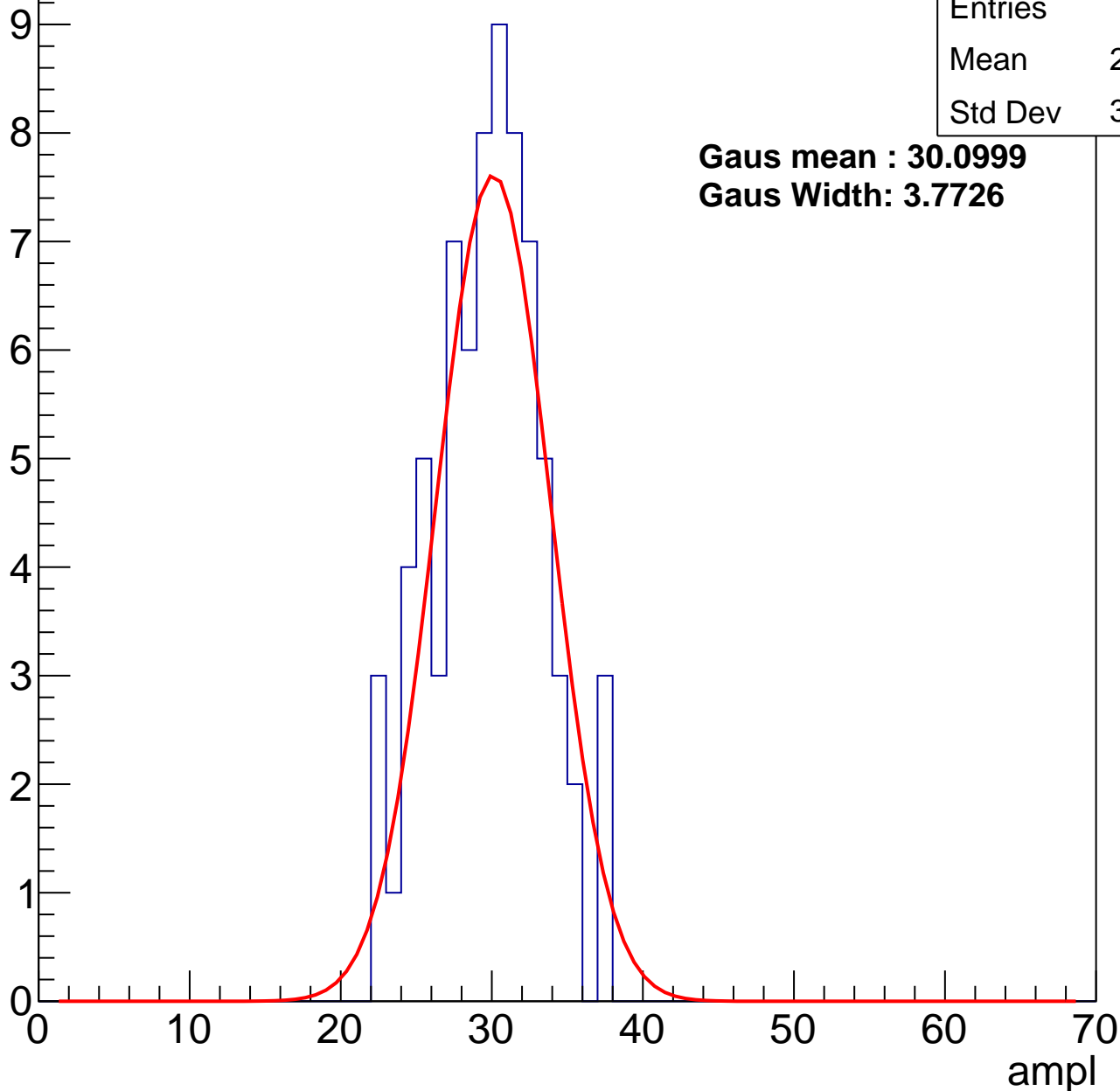
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	29.28
Std Dev	3.566

**Gaus mean : 30.0999**

**Gaus Width: 3.7726**



# B1L103S, U1-ch15, adc1

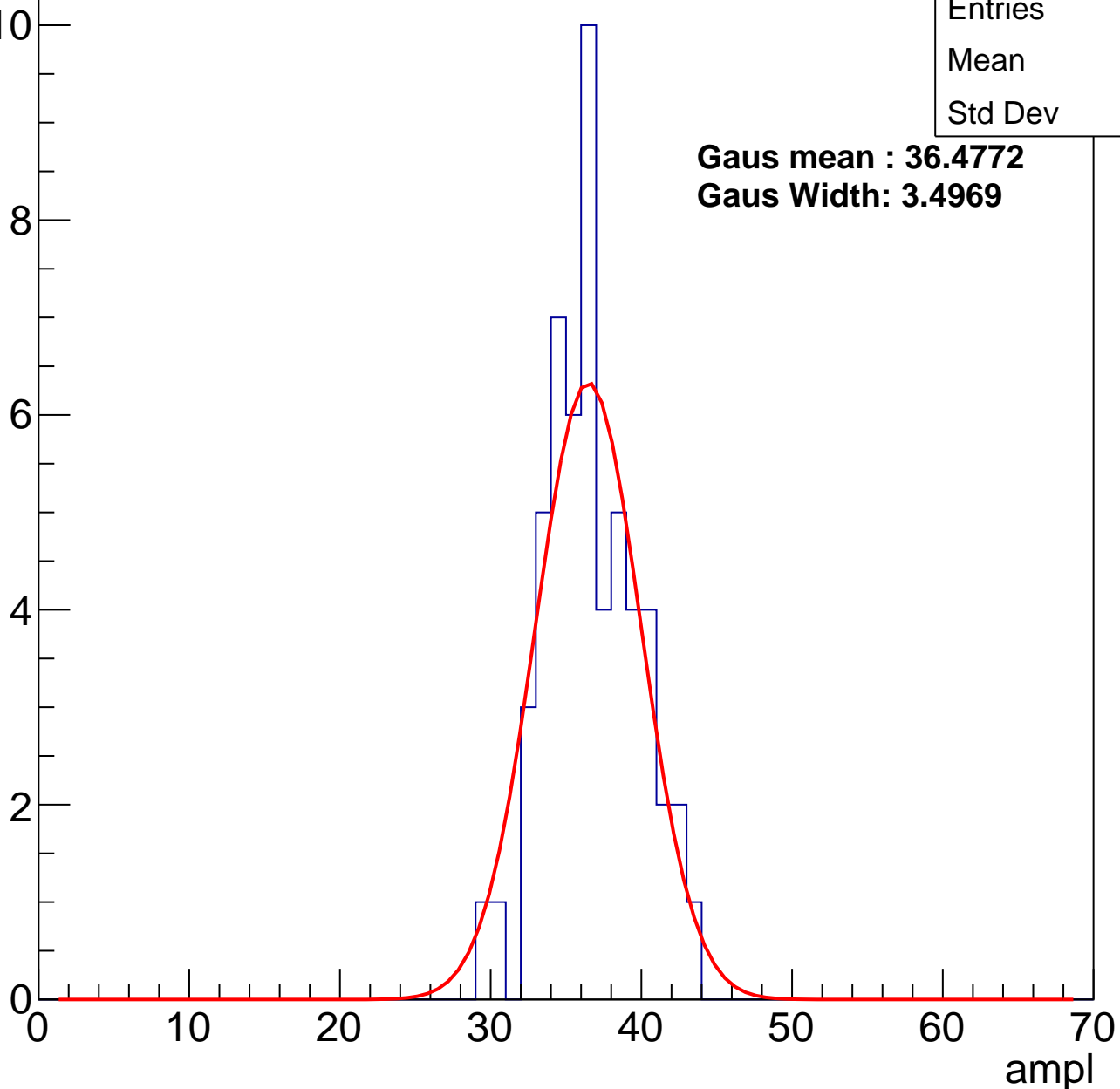
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	36.2
Std Dev	3.03

**Gaus mean : 36.4772**

**Gaus Width: 3.4969**



# B1L103S, U1-ch15, adc2

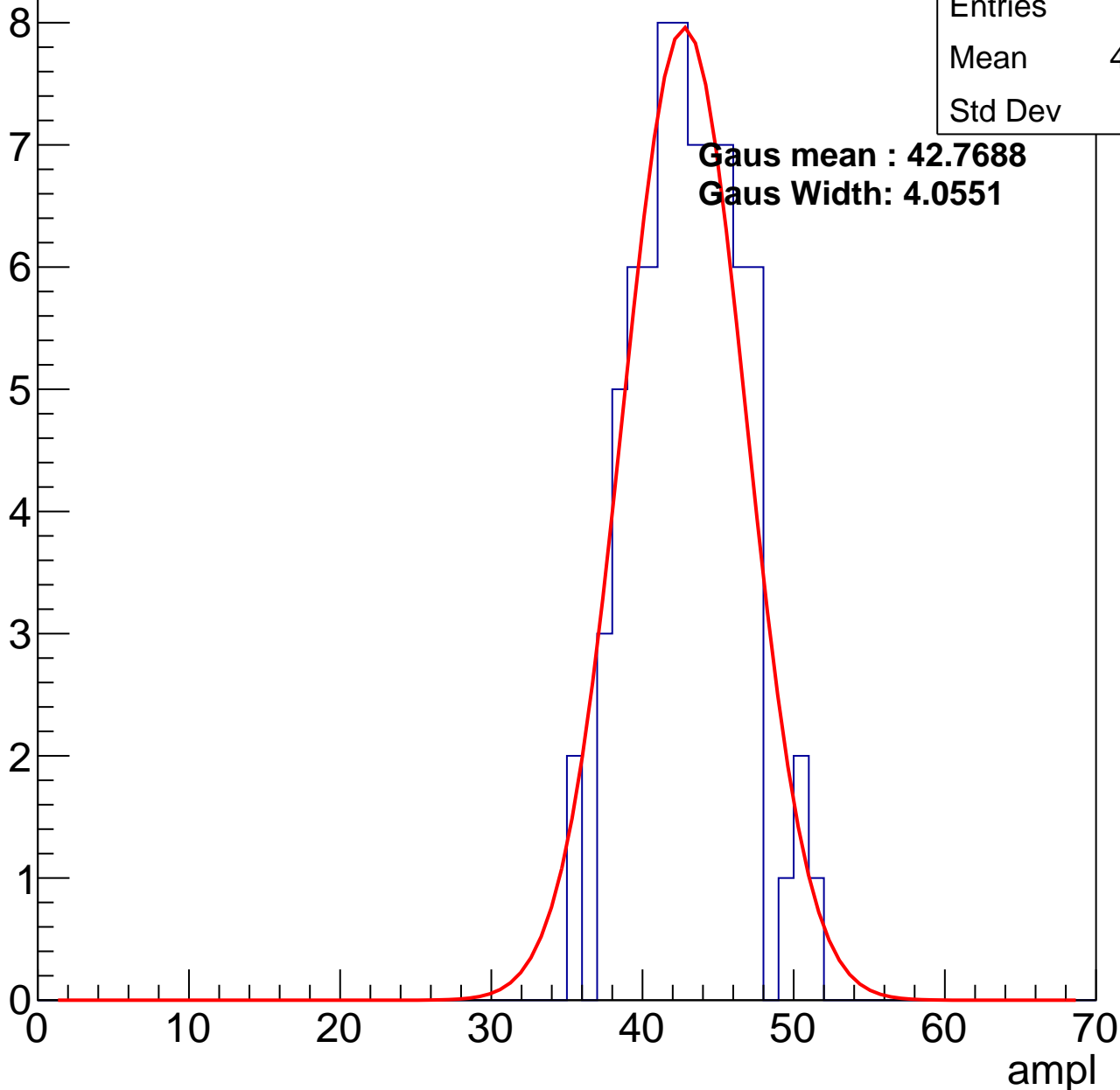
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	42.55
Std Dev	3.5

**Gaus mean : 42.7688**

**Gaus Width: 4.0551**

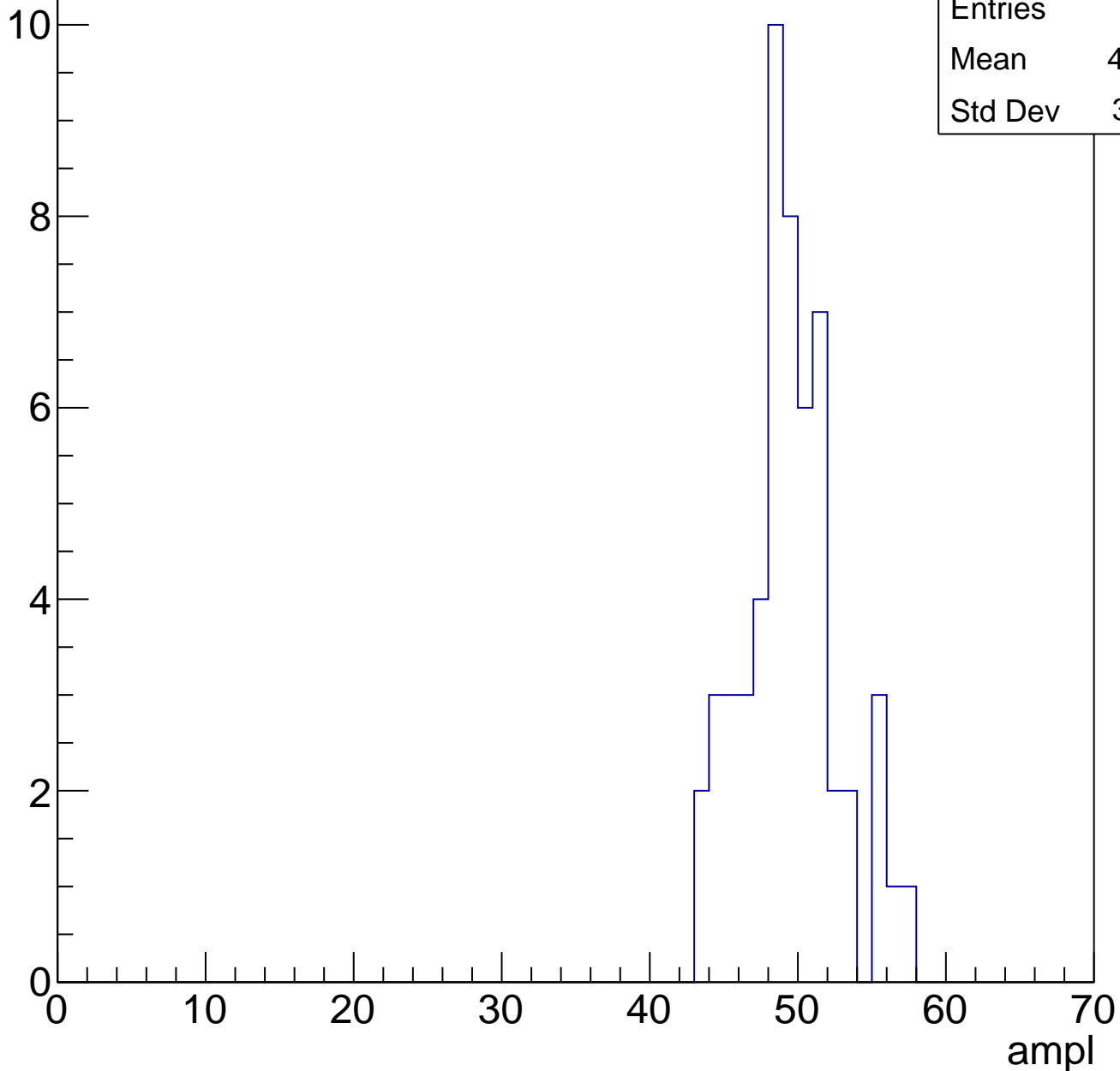


# B1L103S, U1-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	55
Mean	49.02
Std Dev	3.171

Entry

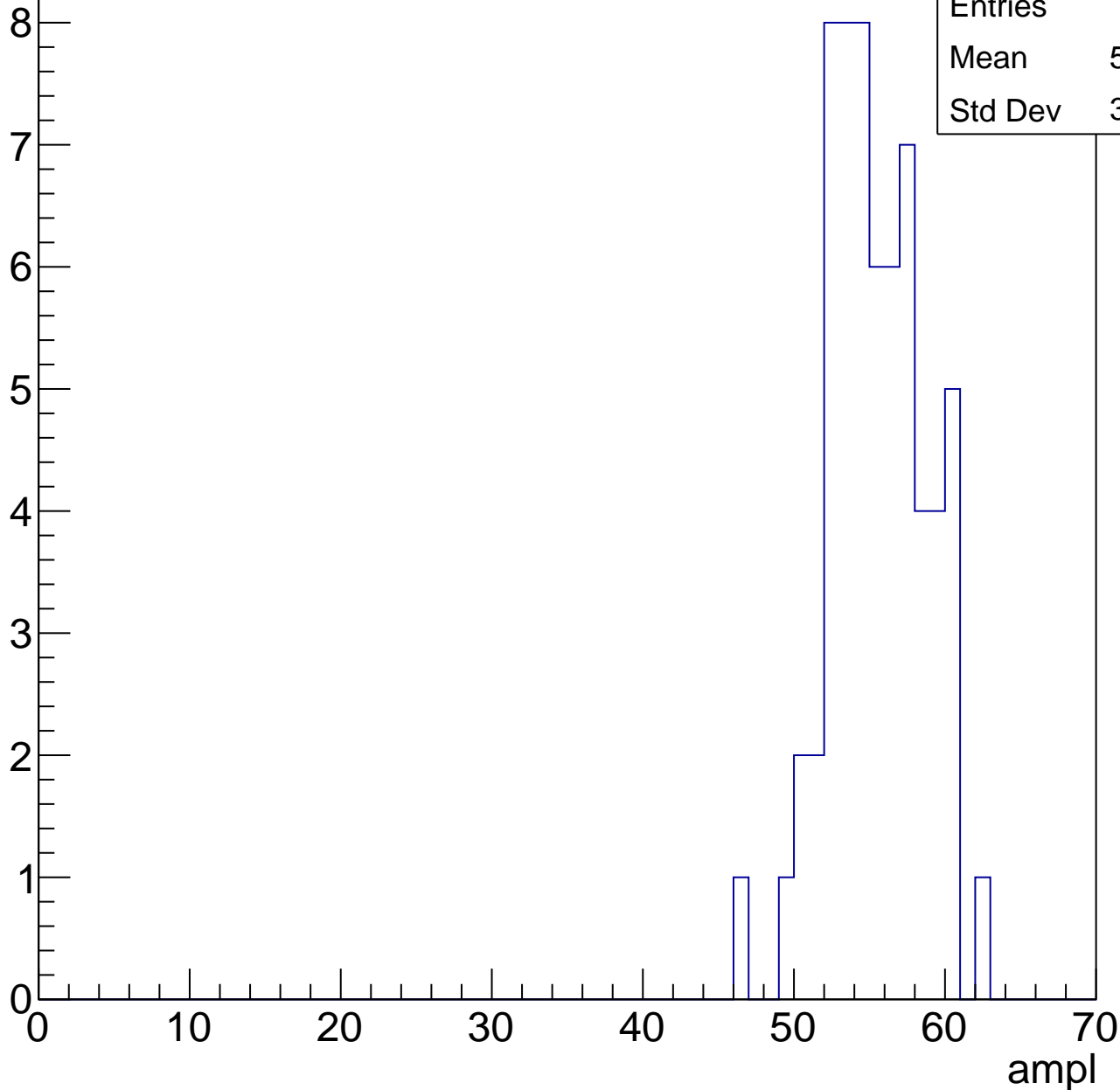


# B1L103S, U1-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	54.98
Std Dev	3.135

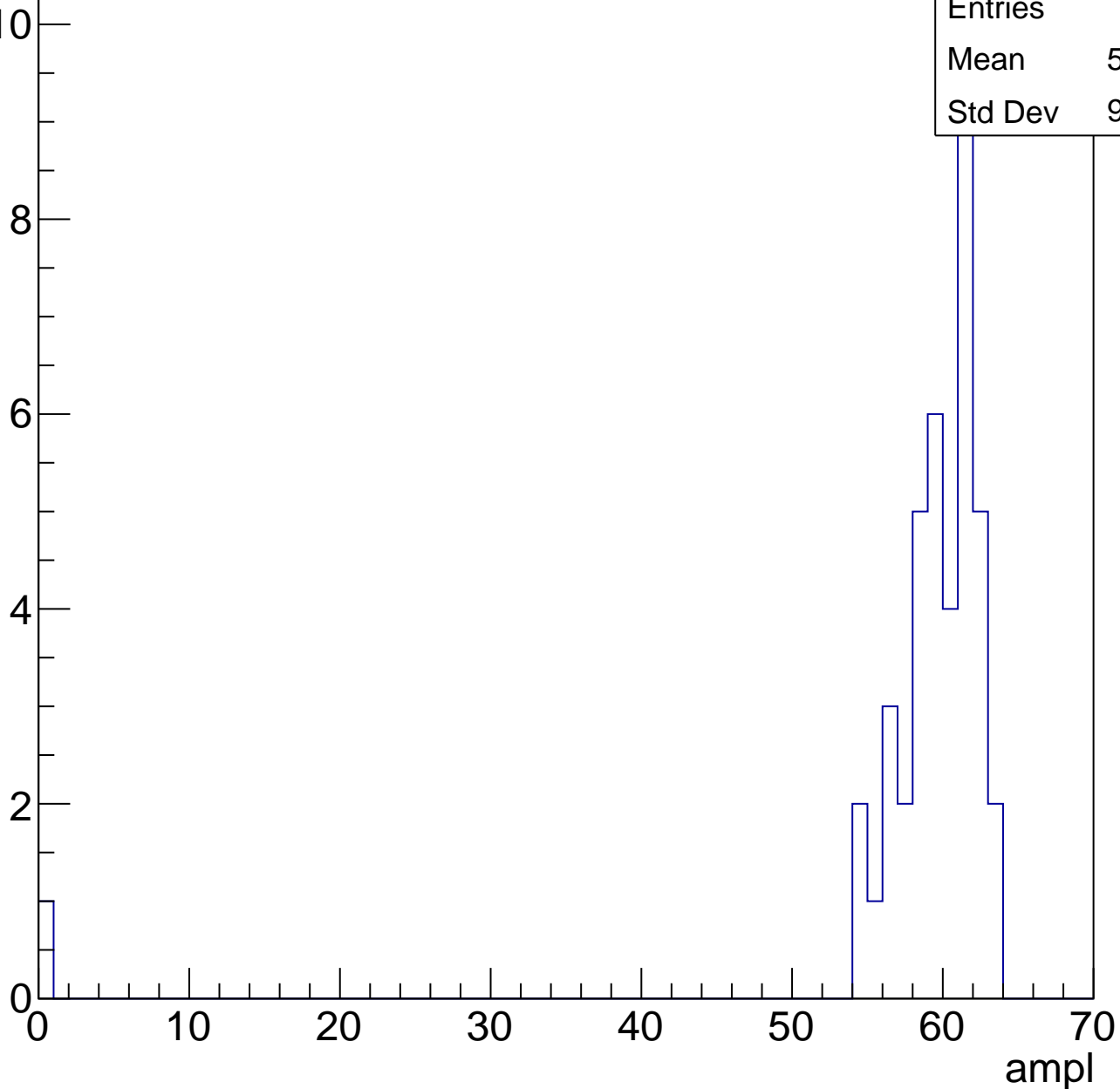


# B1L103S, U1-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	41
Mean	57.93
Std Dev	9.449

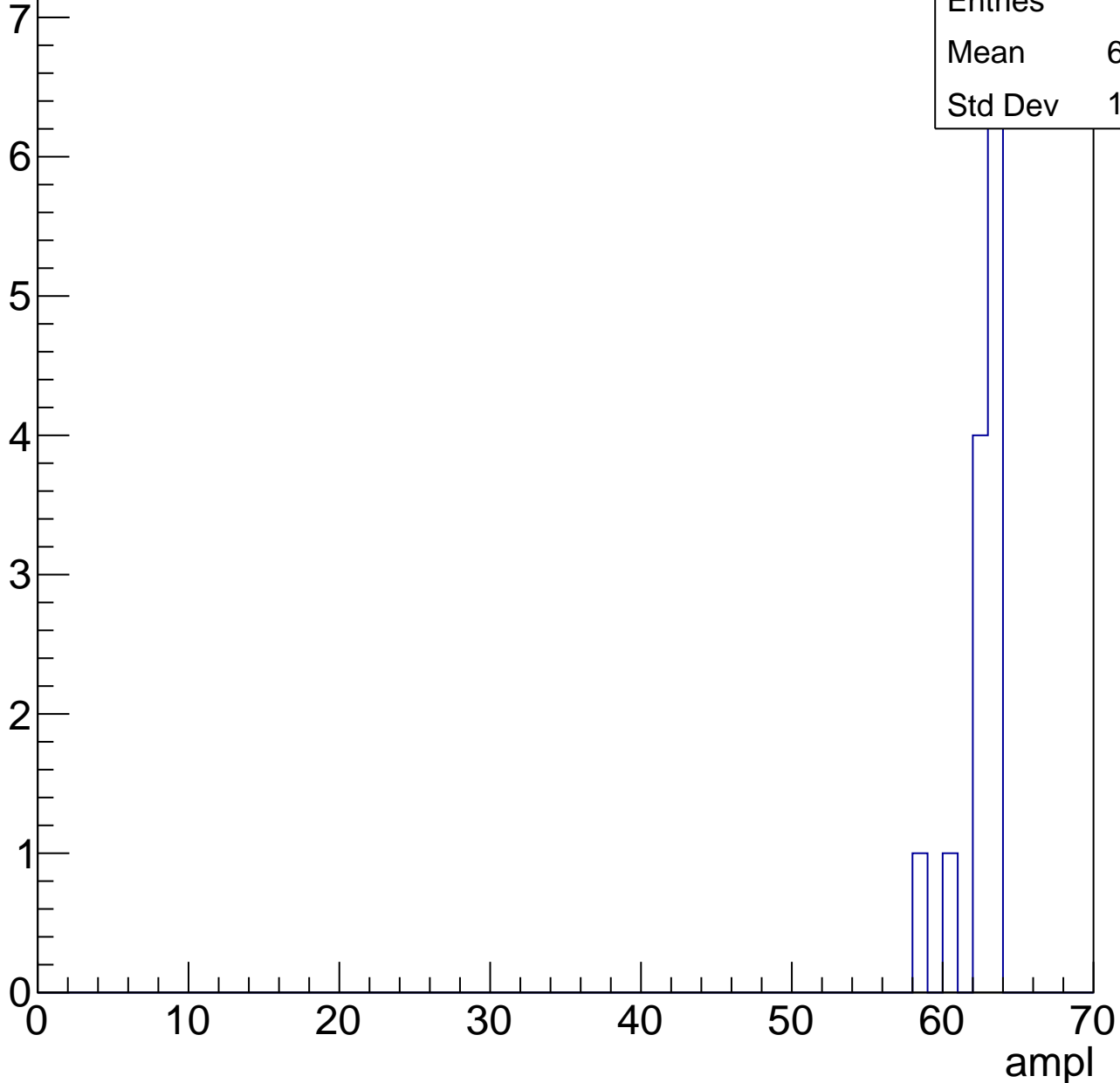


# B1L103S, U1-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	13
Mean	62.08
Std Dev	1.439





# B1L103S, U1-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch16, adc0

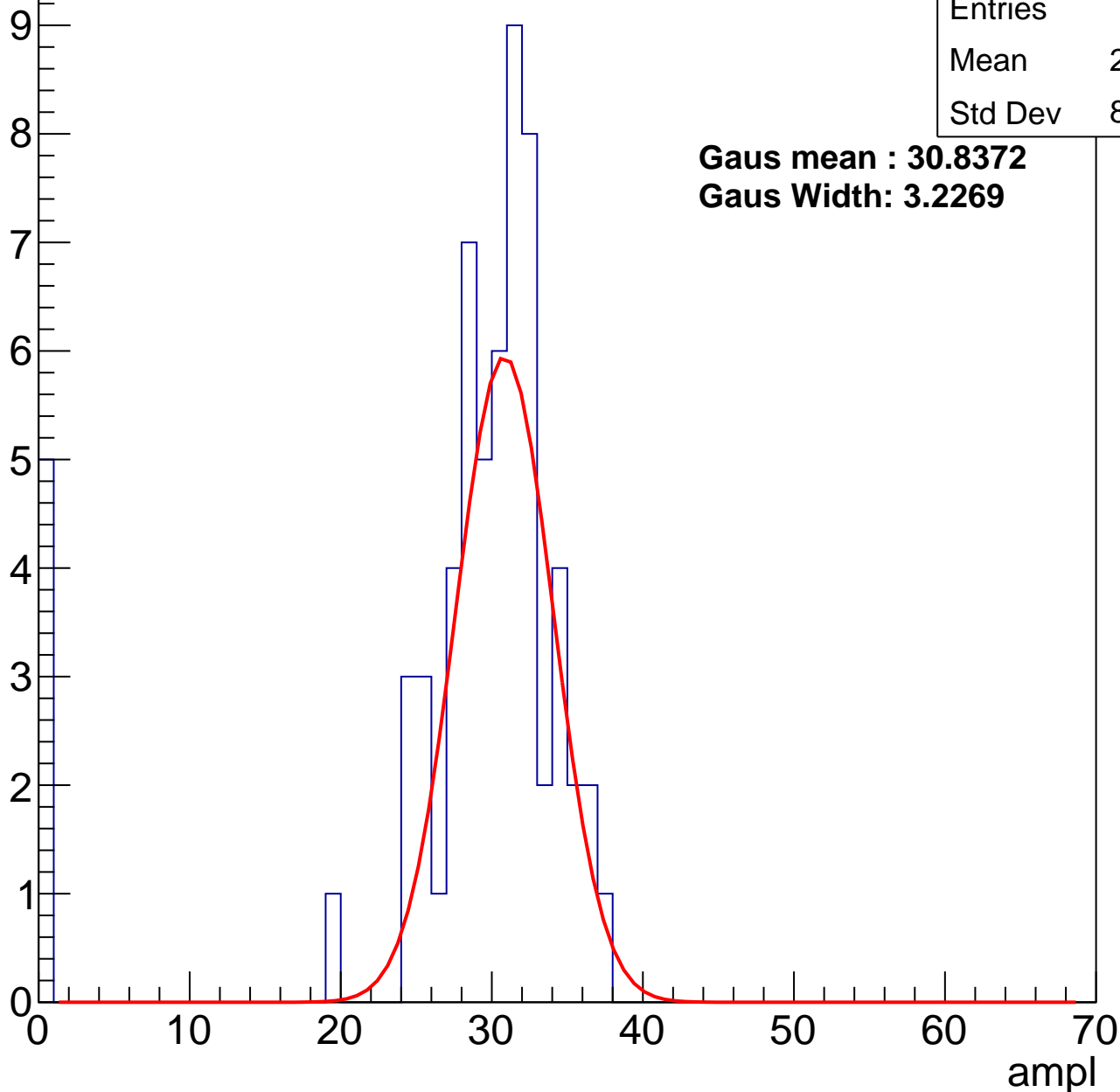
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	27.57
Std Dev	8.739

**Gaus mean : 30.8372**

**Gaus Width: 3.2269**



# B1L103S, U1-ch16, adc1

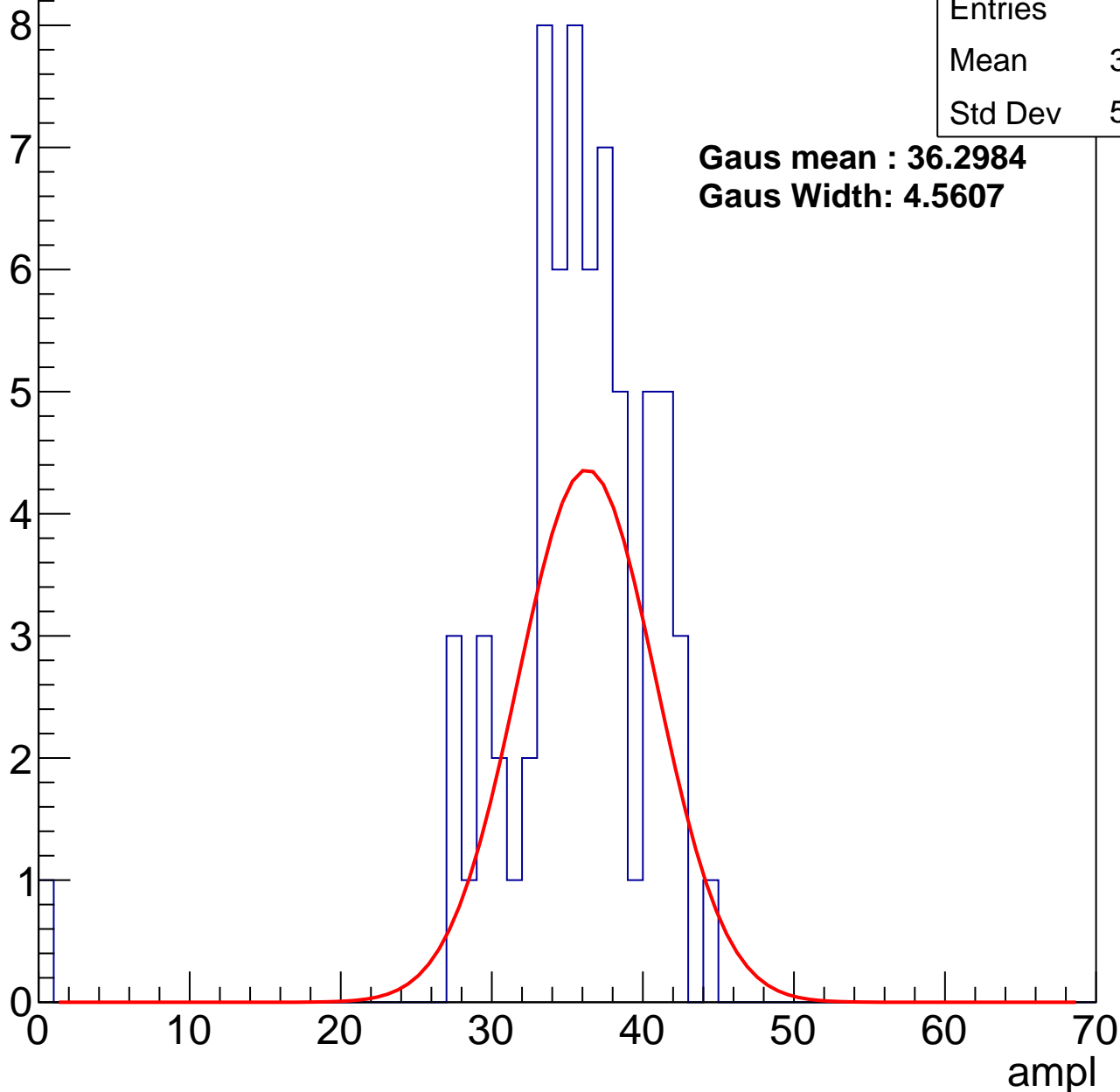
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	34.97
Std Dev	5.846

**Gaus mean : 36.2984**

**Gaus Width: 4.5607**



# B1L103S, U1-ch16, adc2

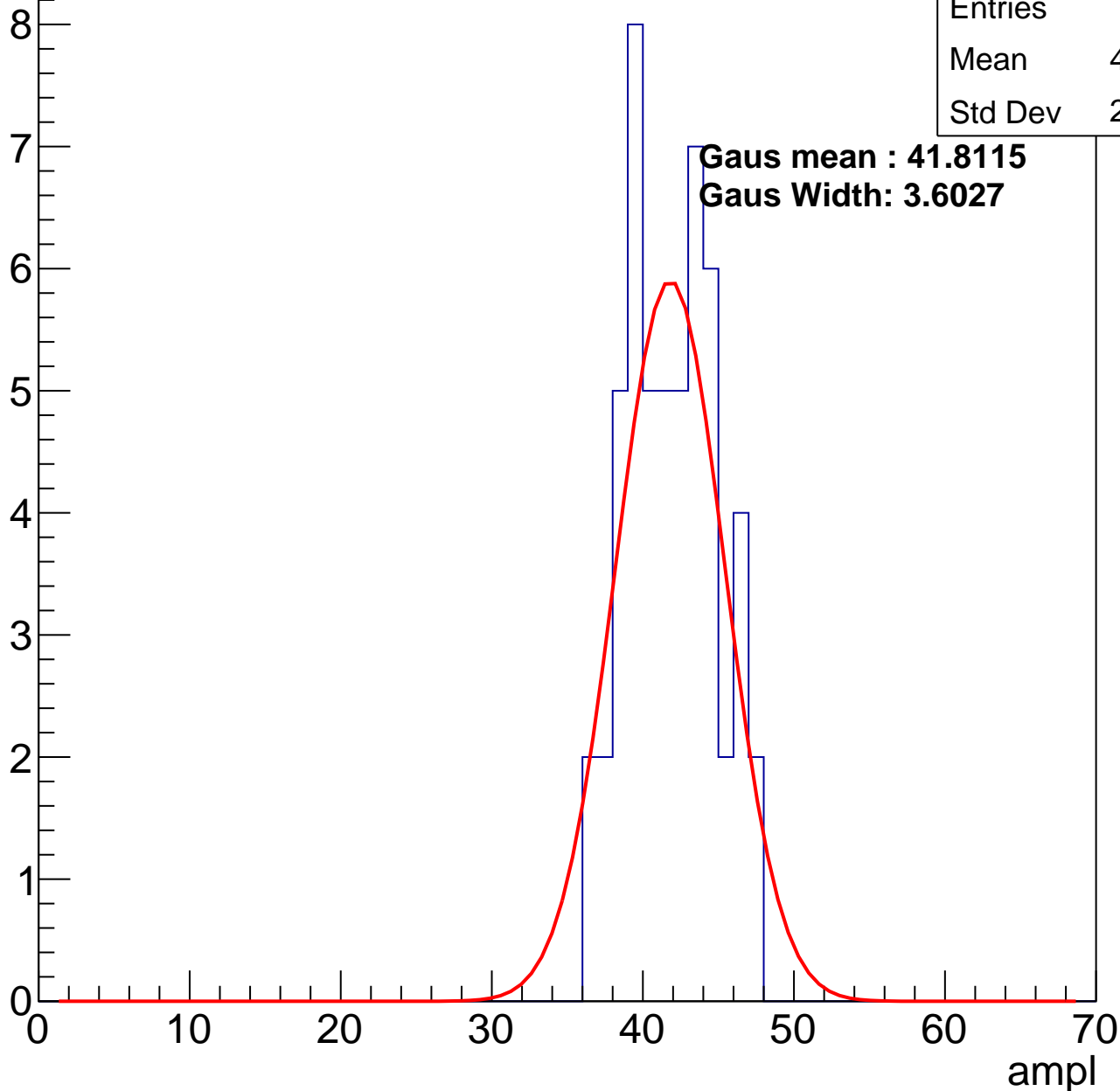
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	41.43
Std Dev	2.898

**Gaus mean : 41.8115**

**Gaus Width: 3.6027**

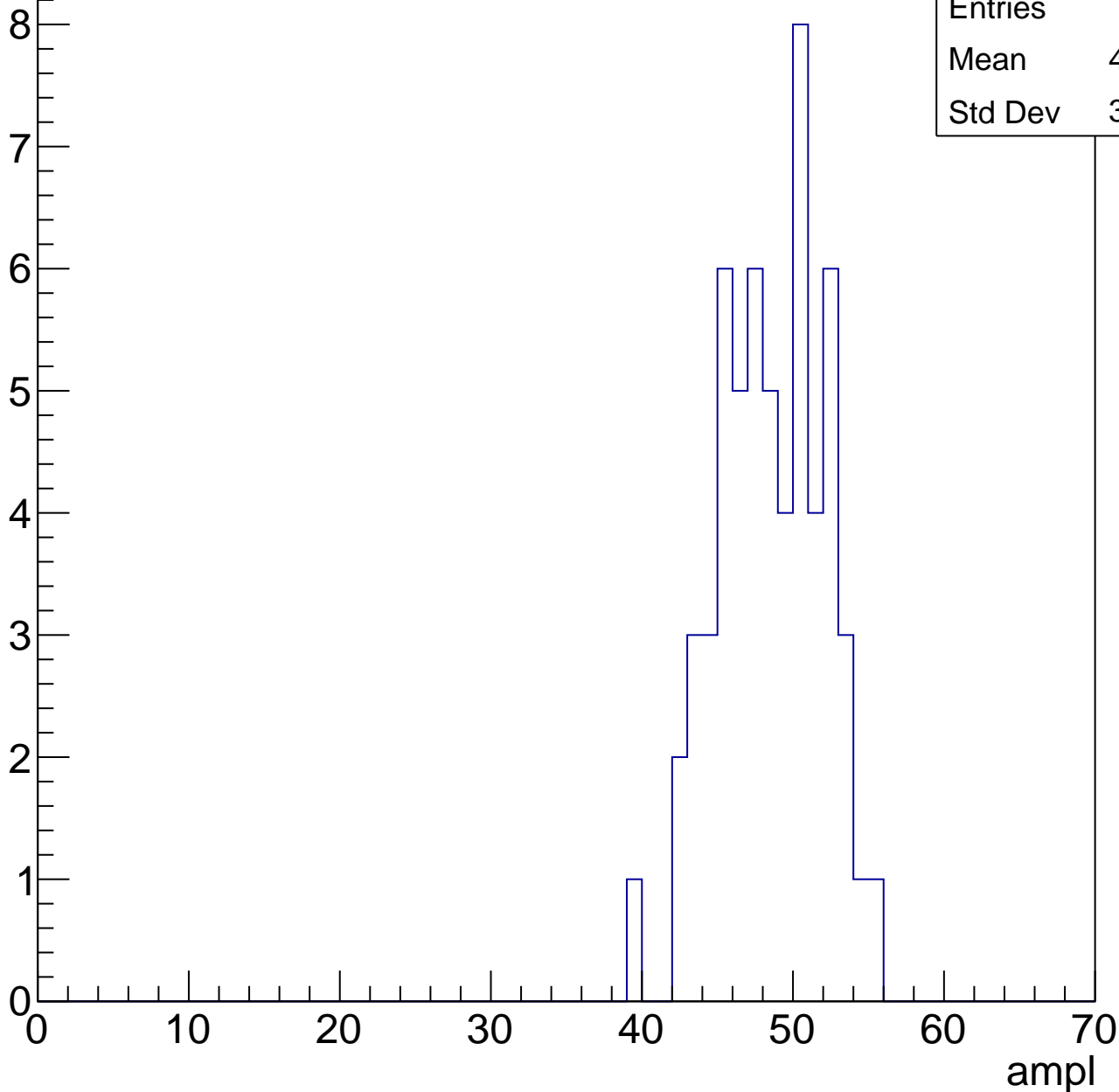


# B1L103S, U1-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	48.03
Std Dev	3.434

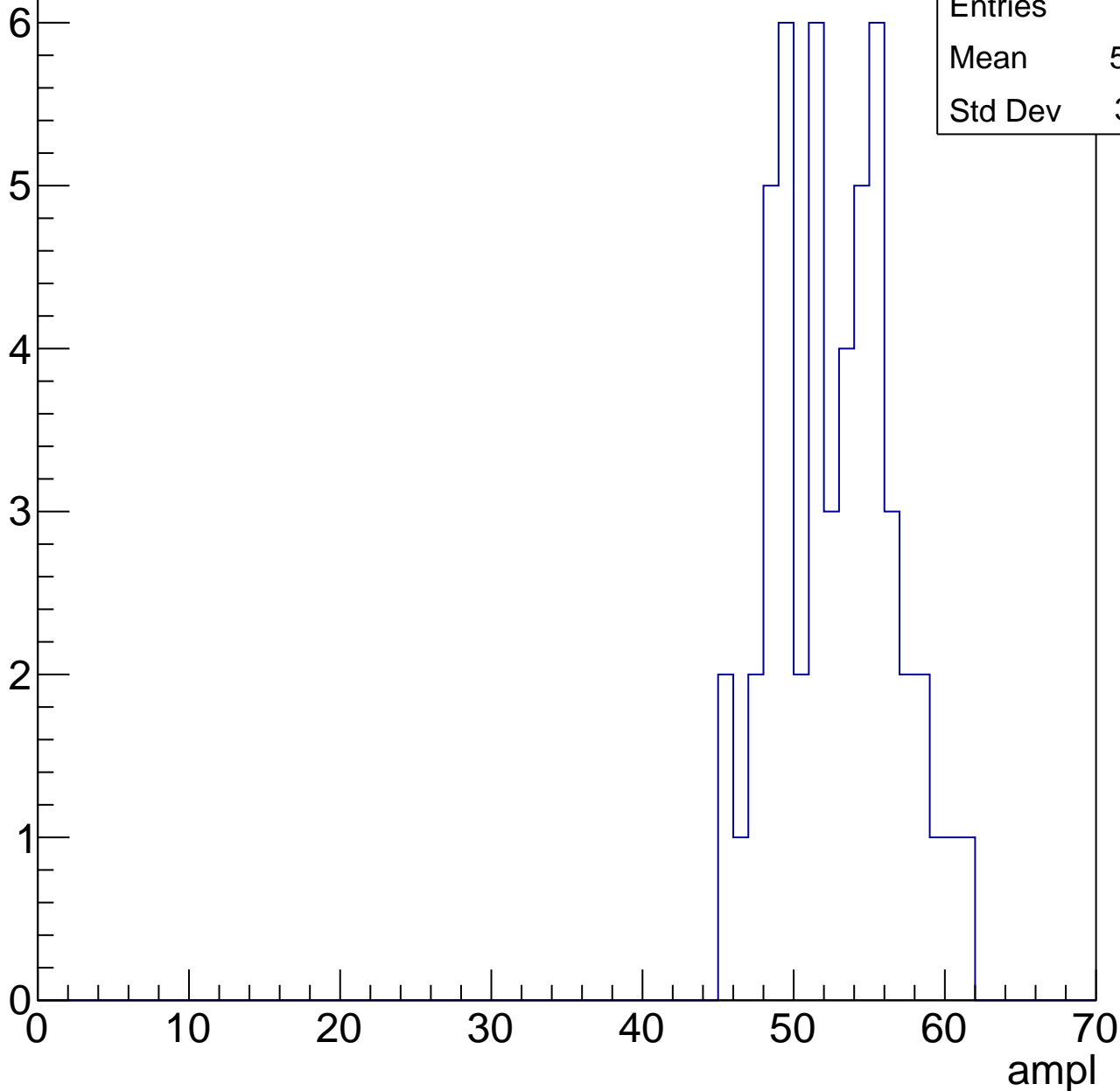


# B1L103S, U1-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

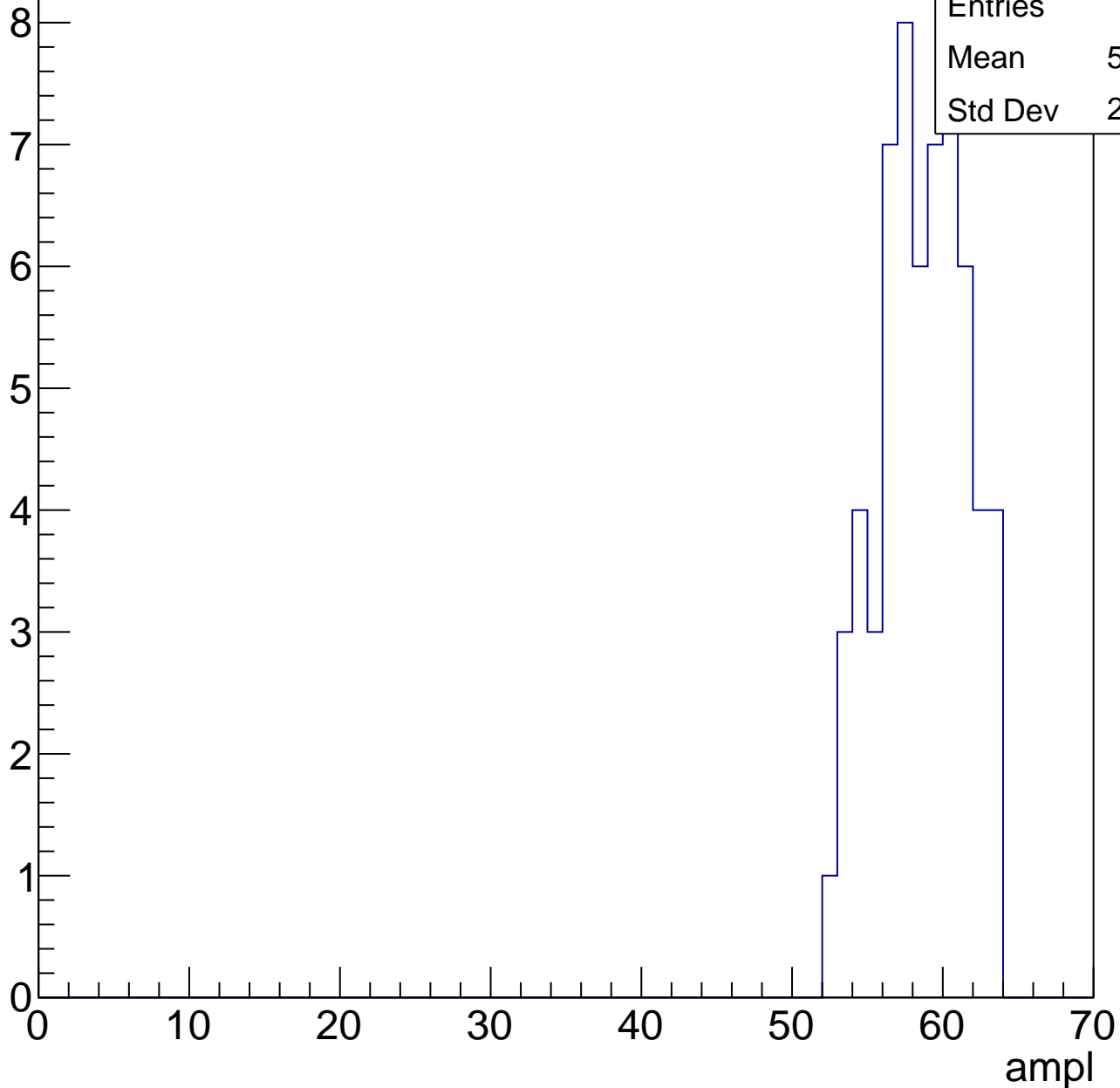
Entries	52
Mean	52.23
Std Dev	3.851



# B1L103S, U1-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

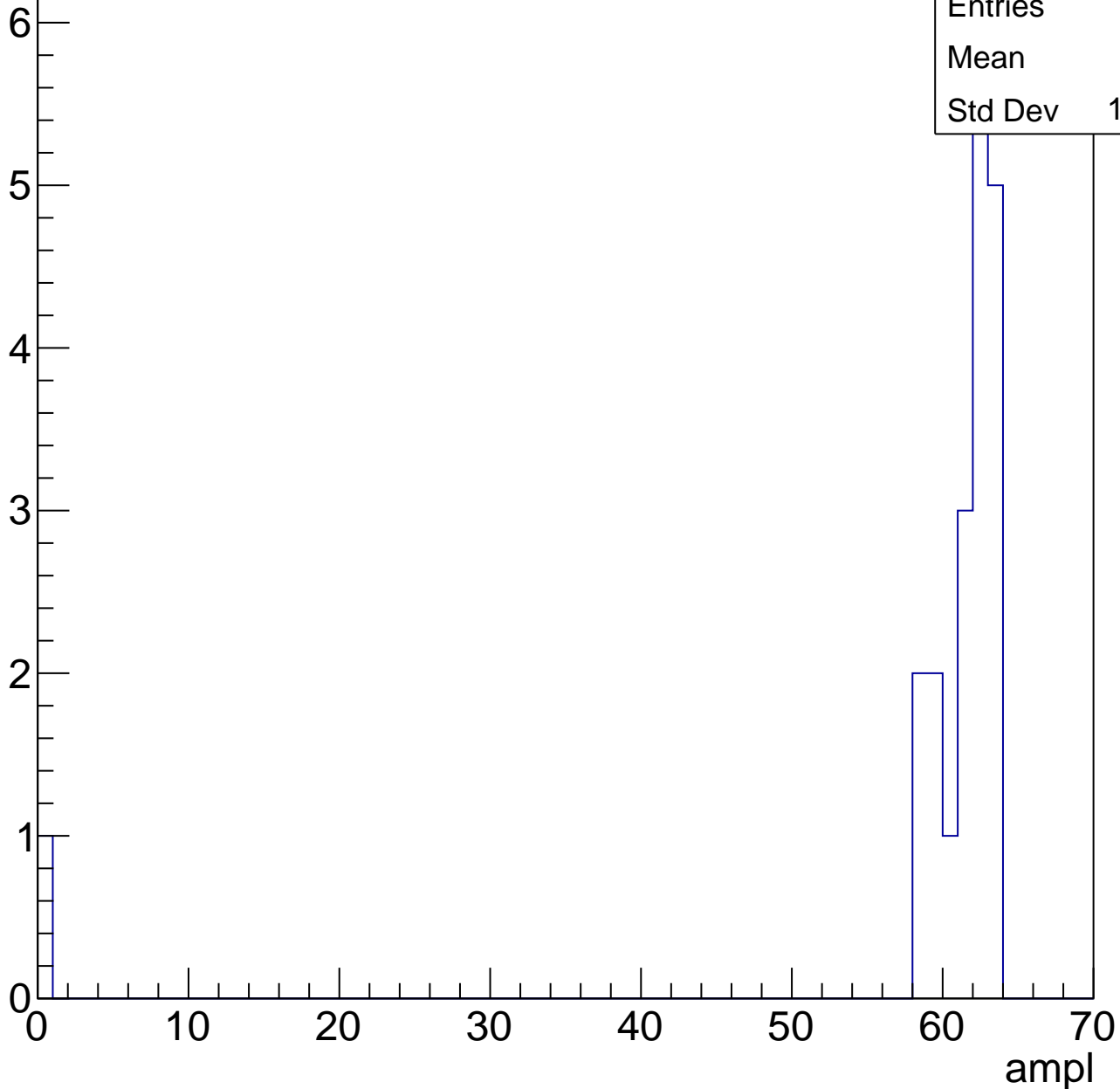


# B1L103S, U1-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	20
Mean	58.2
Std Dev	13.45





# B1L103S, U1-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch17, adc0

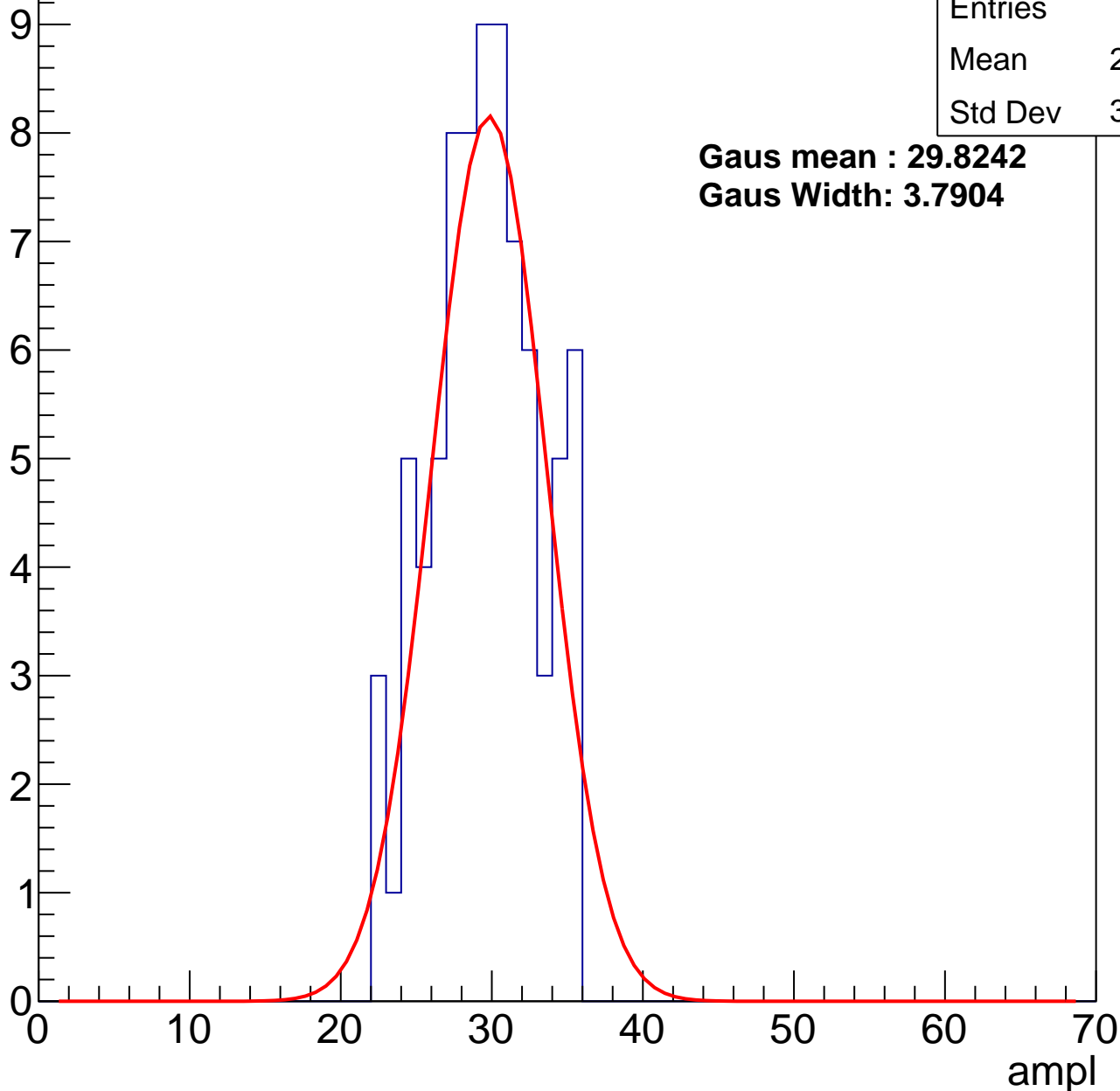
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	29.09
Std Dev	3.443

**Gaus mean : 29.8242**

**Gaus Width: 3.7904**



# B1L103S, U1-ch17, adc1

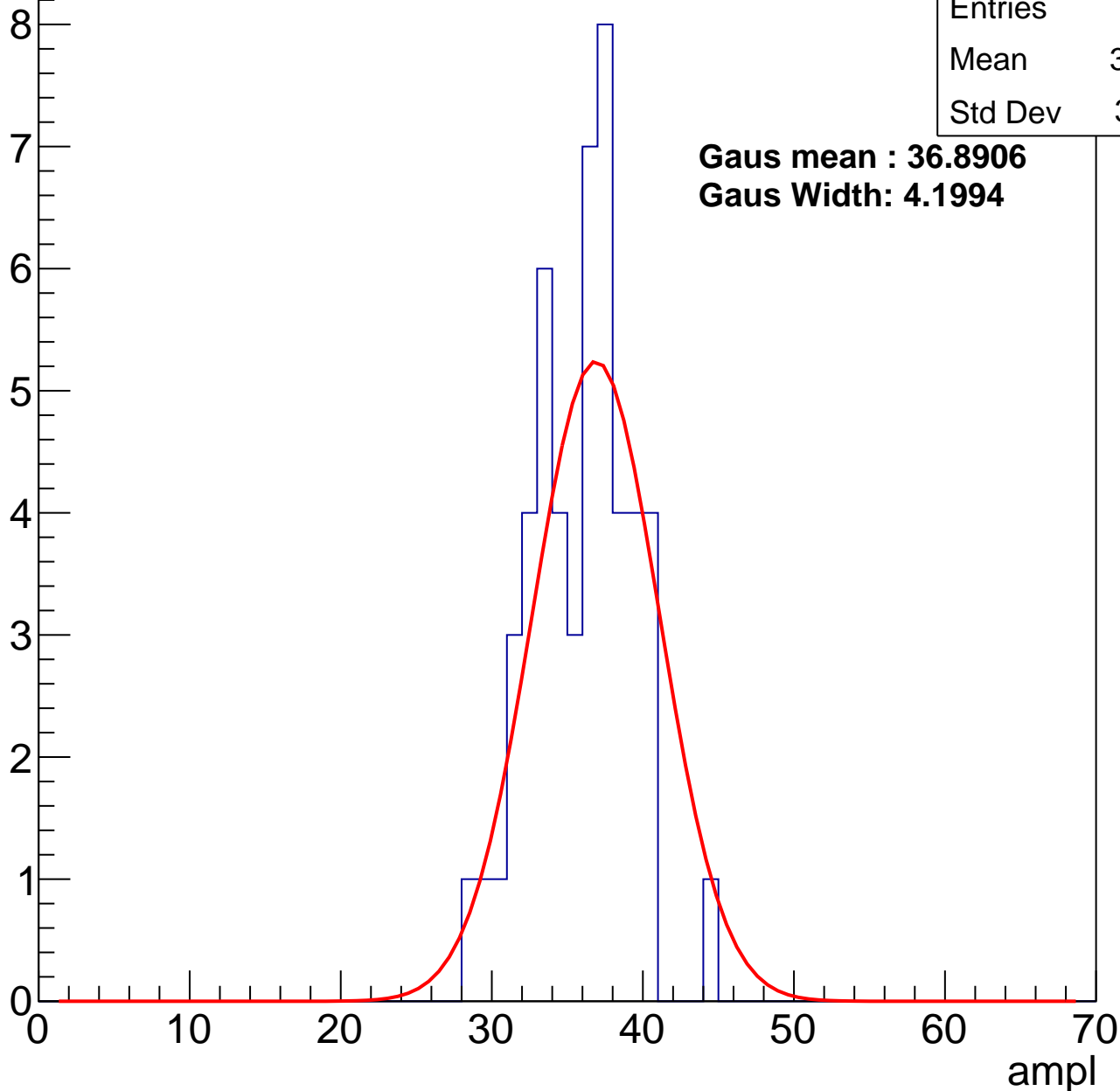
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	35.43
Std Dev	3.231

**Gaus mean : 36.8906**

**Gaus Width: 4.1994**



# B1L103S, U1-ch17, adc2

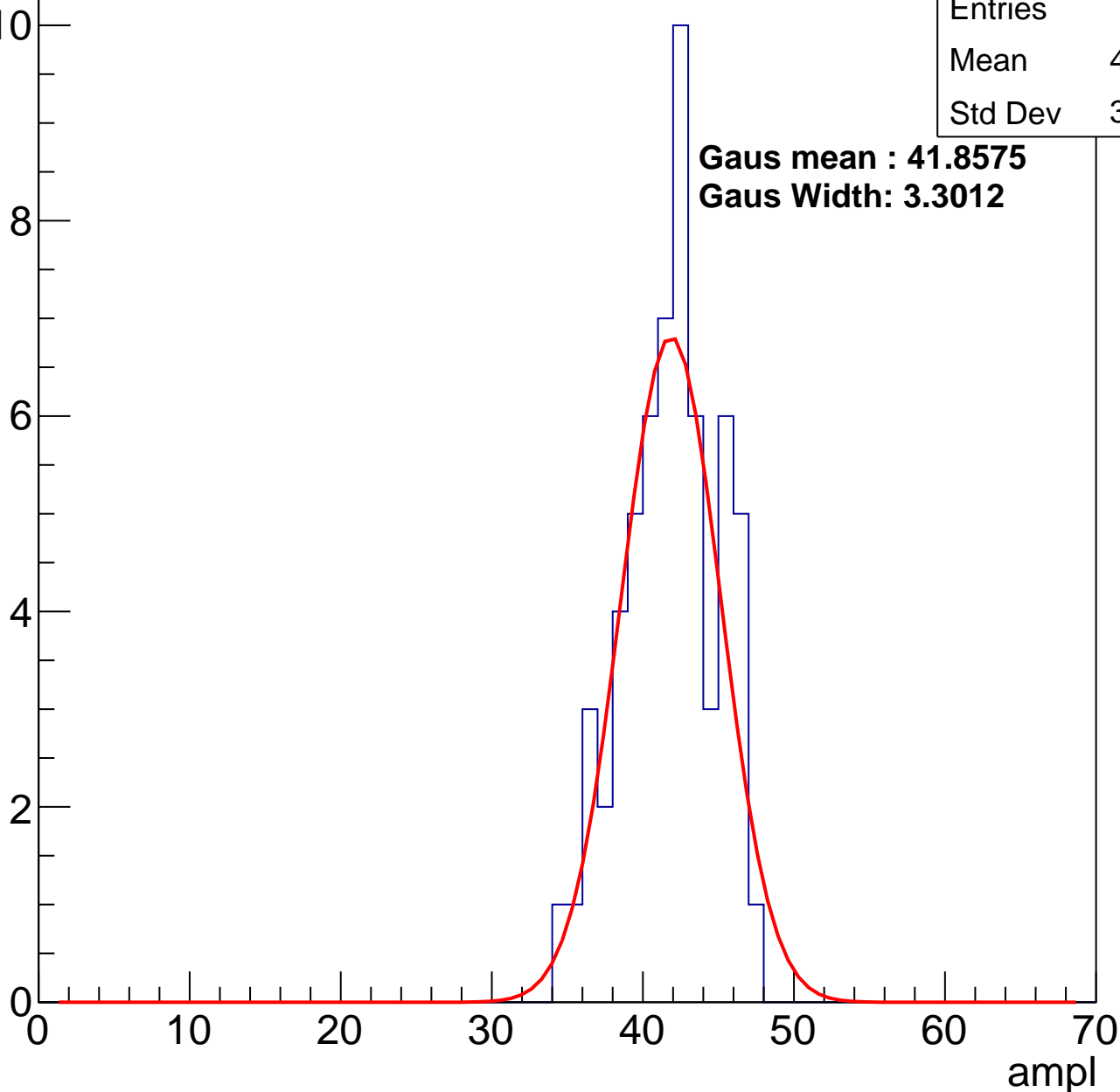
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	41.37
Std Dev	3.066

**Gaus mean : 41.8575**

**Gaus Width: 3.3012**

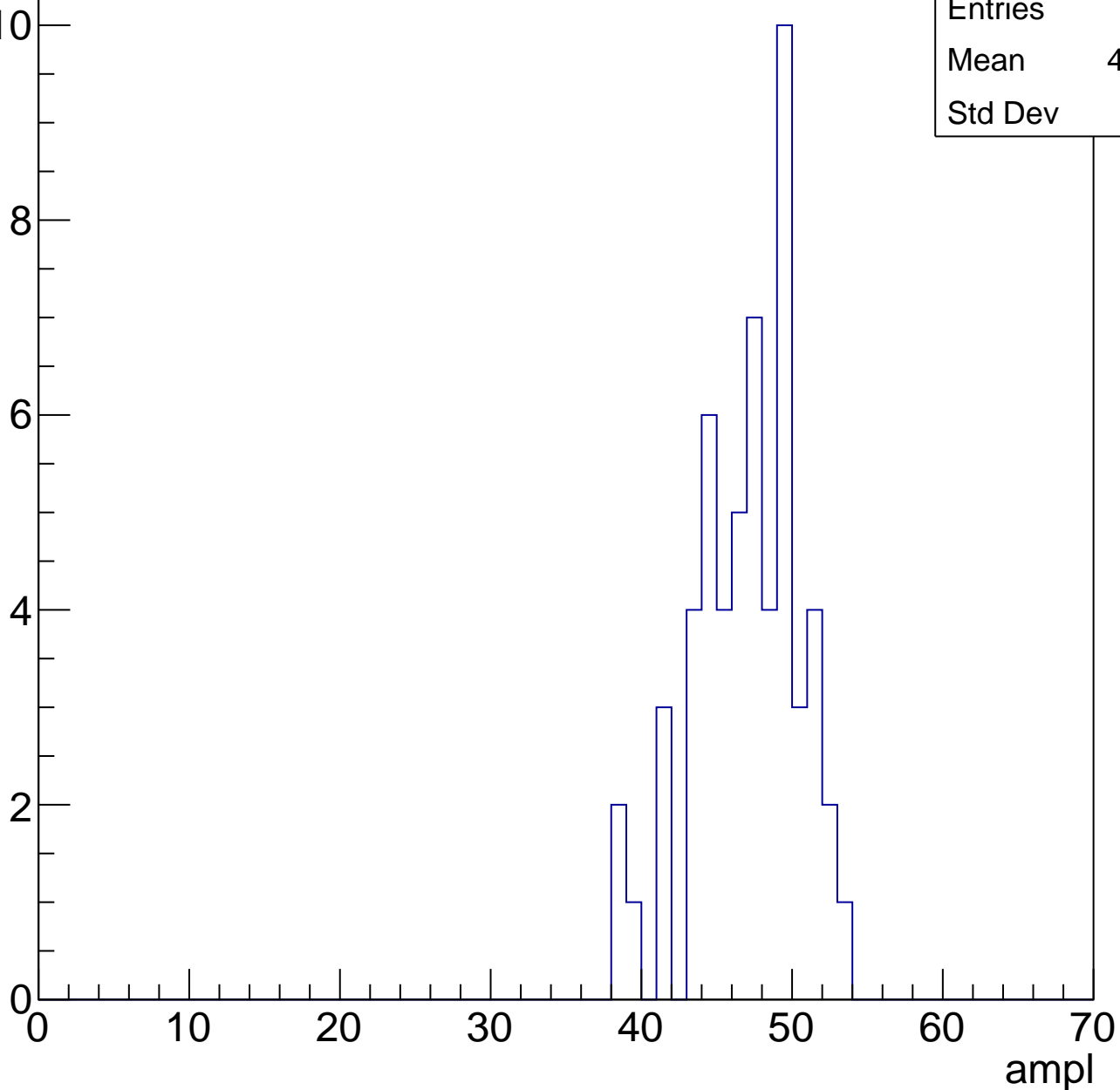


# B1L103S, U1-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	46.54
Std Dev	3.49

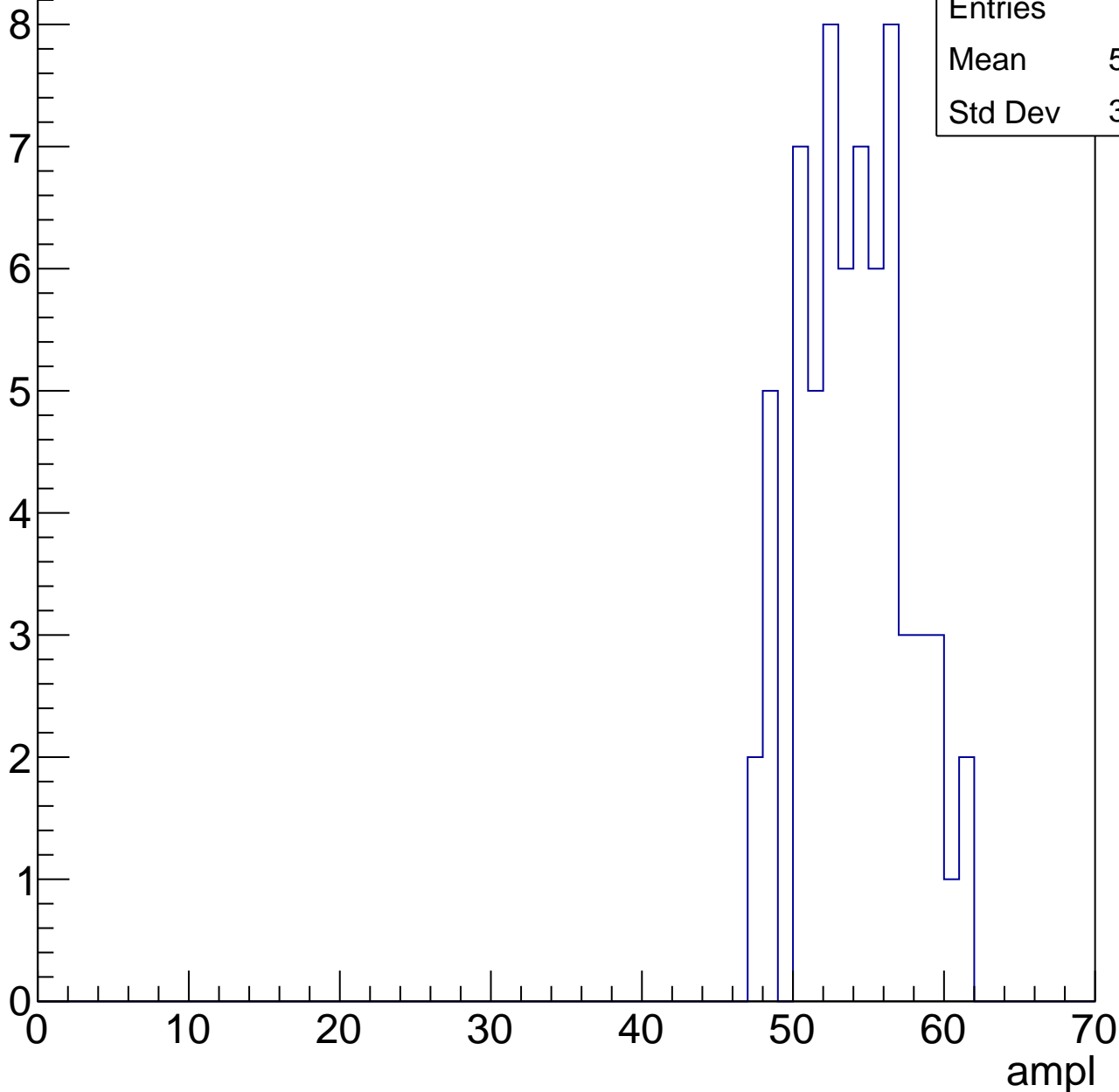


# B1L103S, U1-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	53.53
Std Dev	3.439



# B1L103S, U1-ch17, adc5

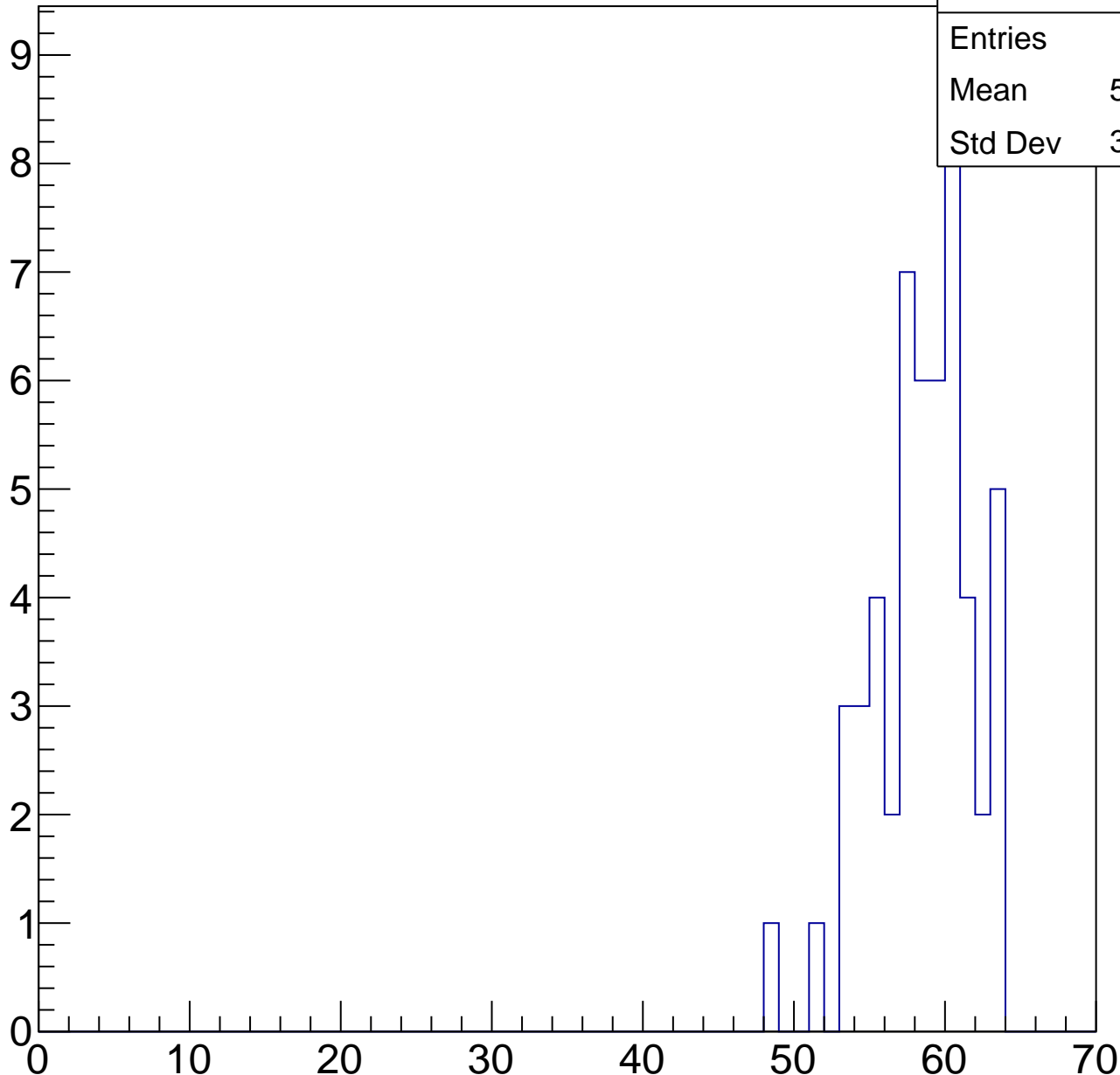
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	53
Mean	58.04
Std Dev	3.245

ampl

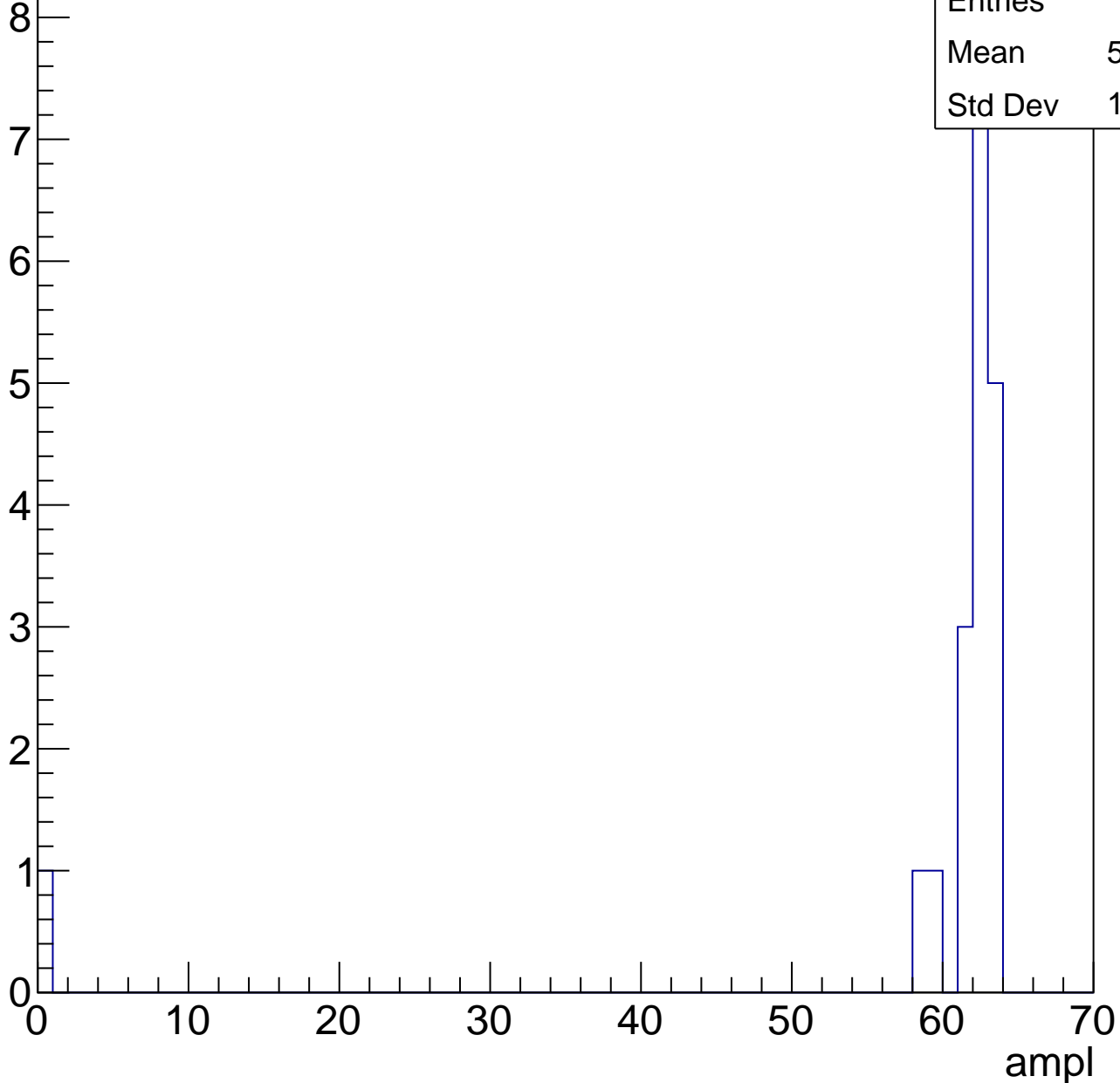


# B1L103S, U1-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	19
Mean	58.47
Std Dev	13.84





# B1L103S, U1-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	20.33
Std Dev	28.76

# B1L103S, U1-ch18, adc0

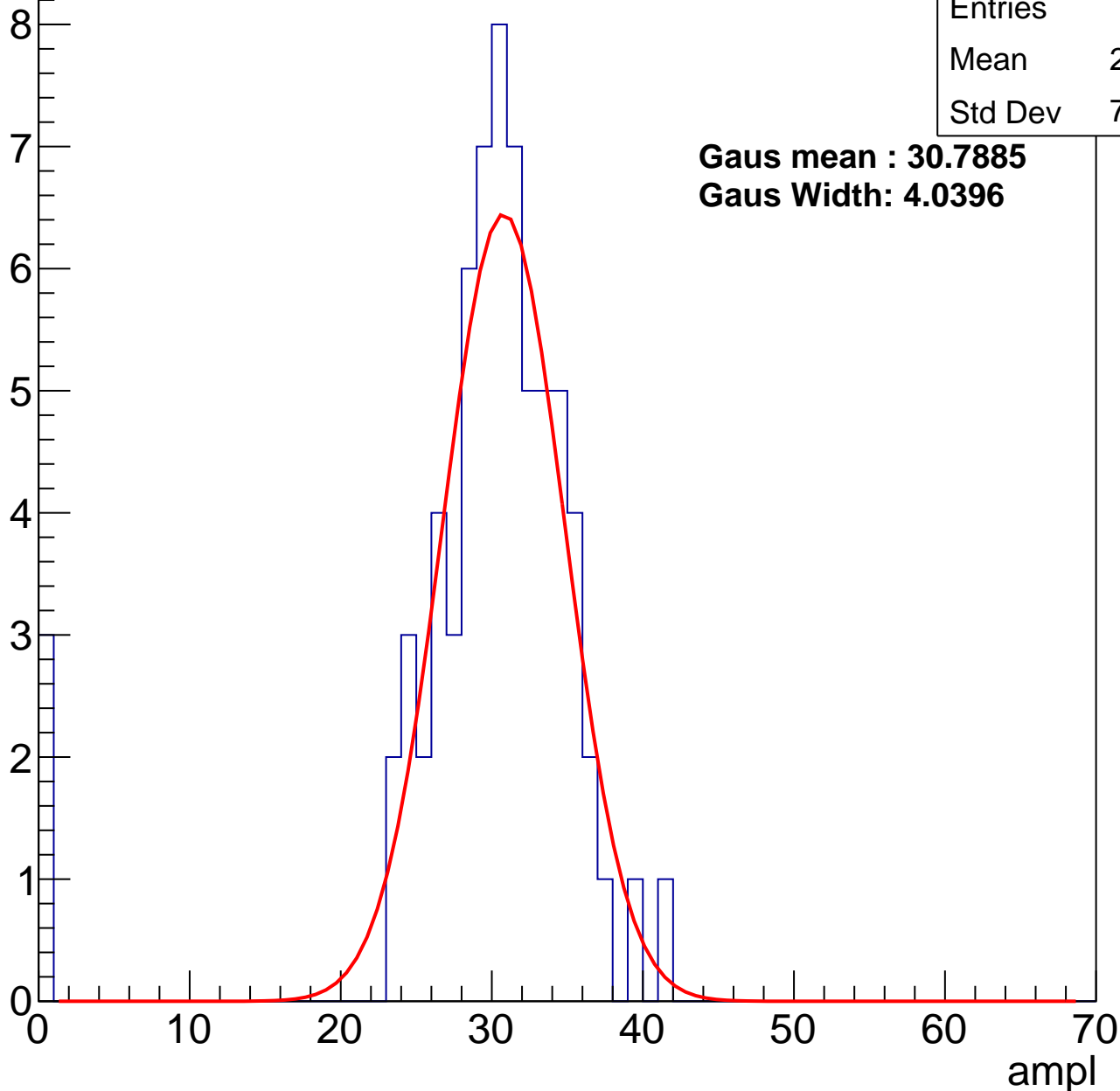
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	29.06
Std Dev	7.215

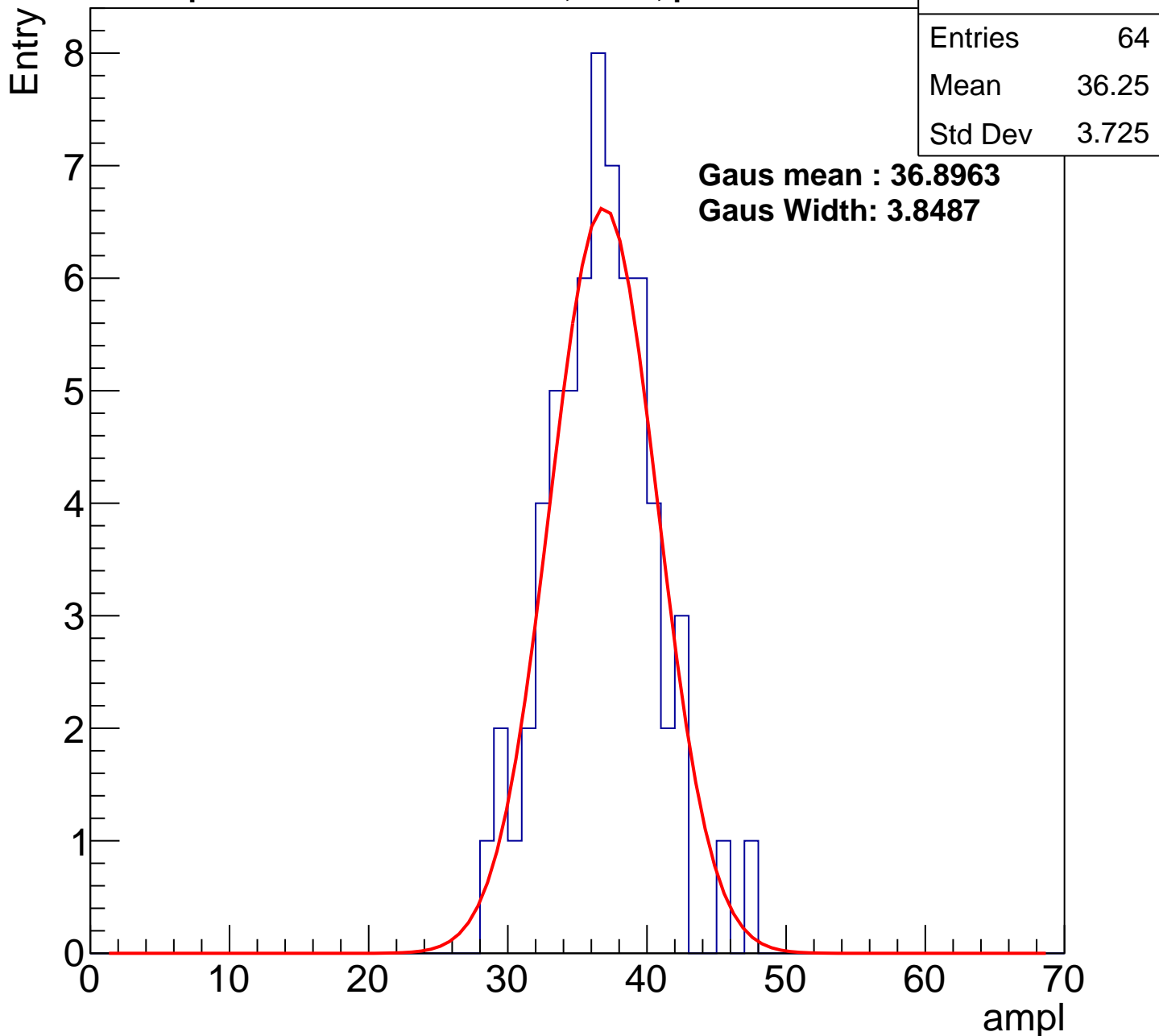
**Gaus mean : 30.7885**

**Gaus Width: 4.0396**



# B1L103S, U1-ch18, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

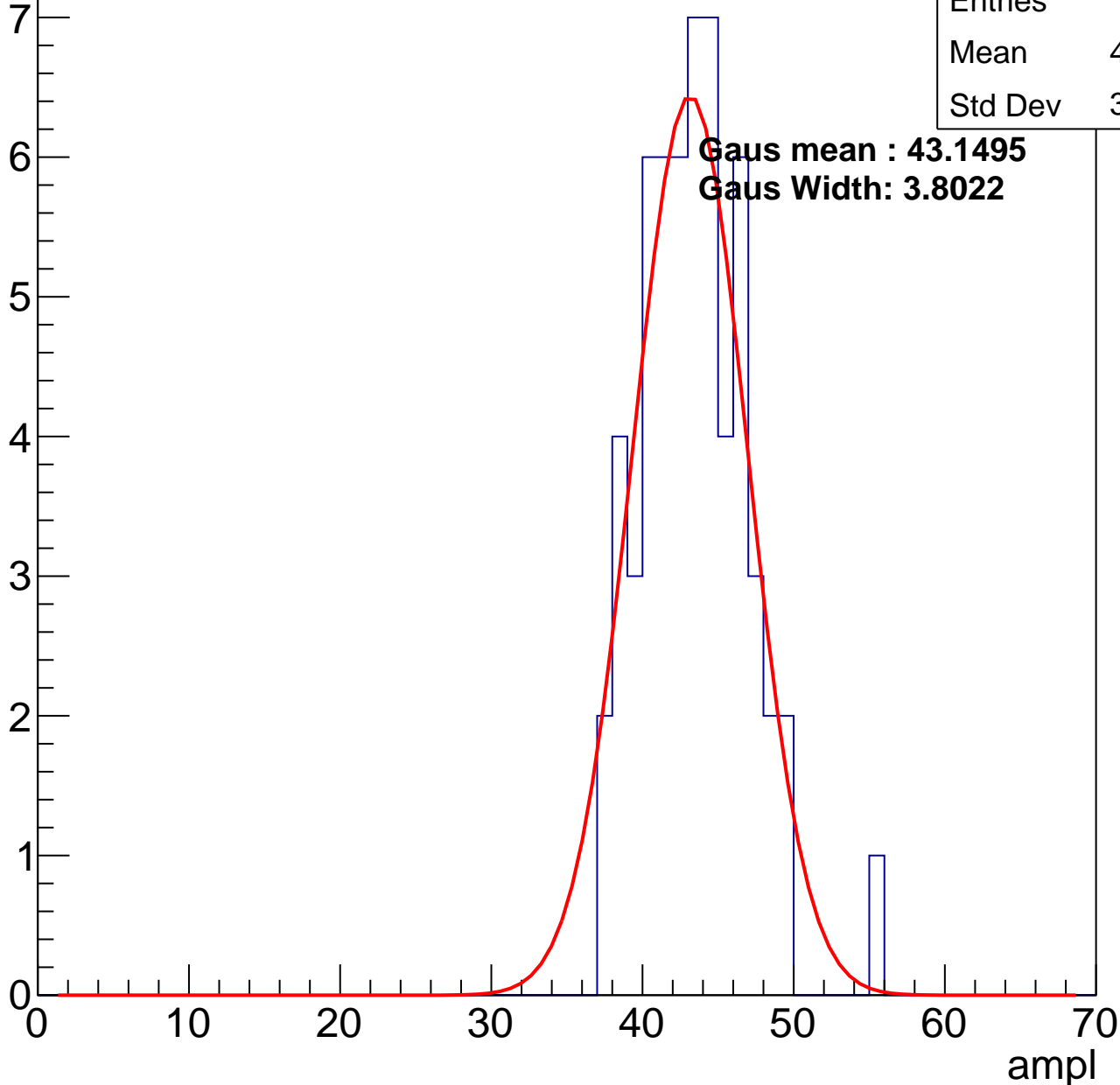


# B1L103S, U1-ch18, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	42.98
Std Dev	3.432

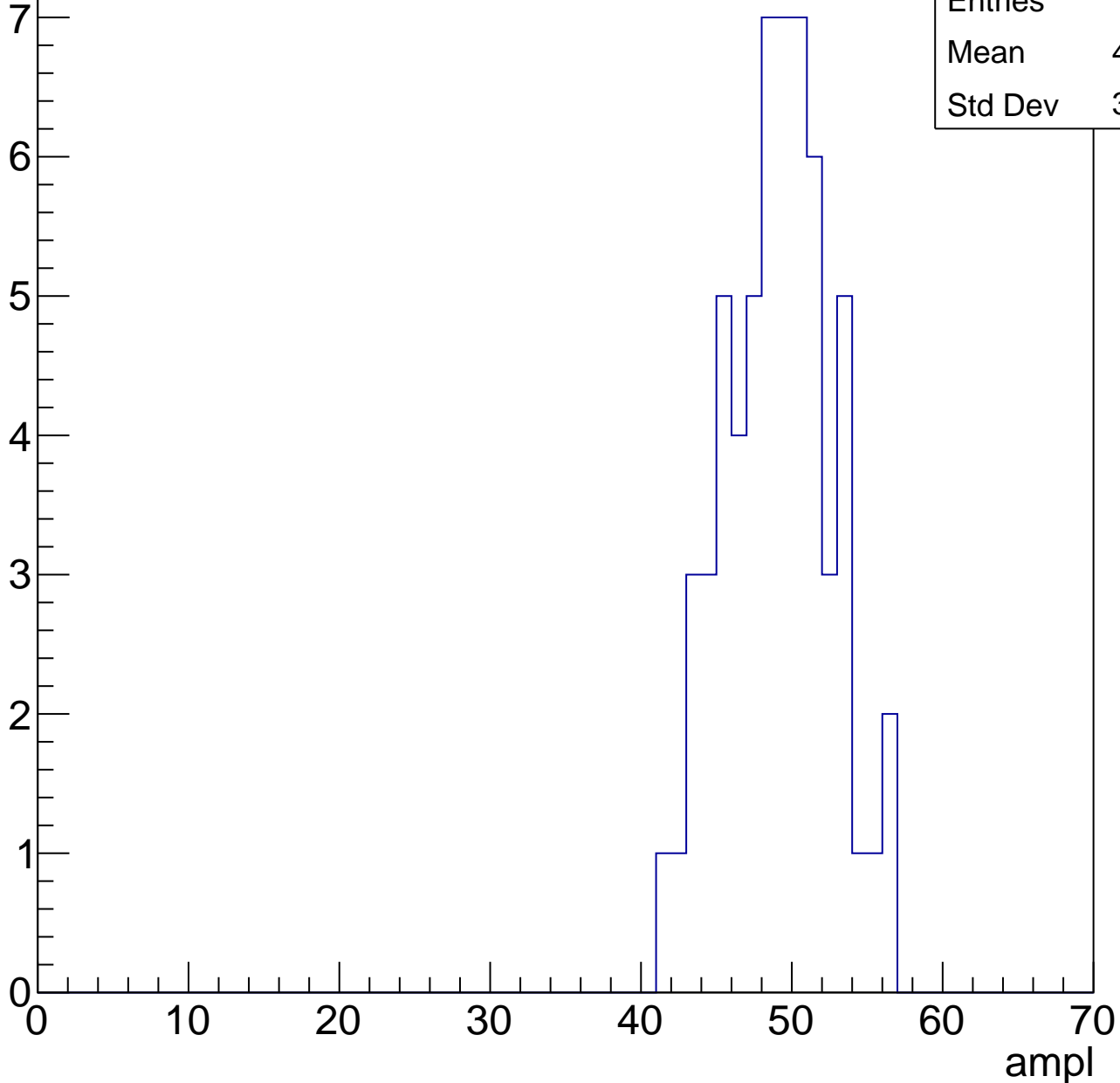


# B1L103S, U1-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

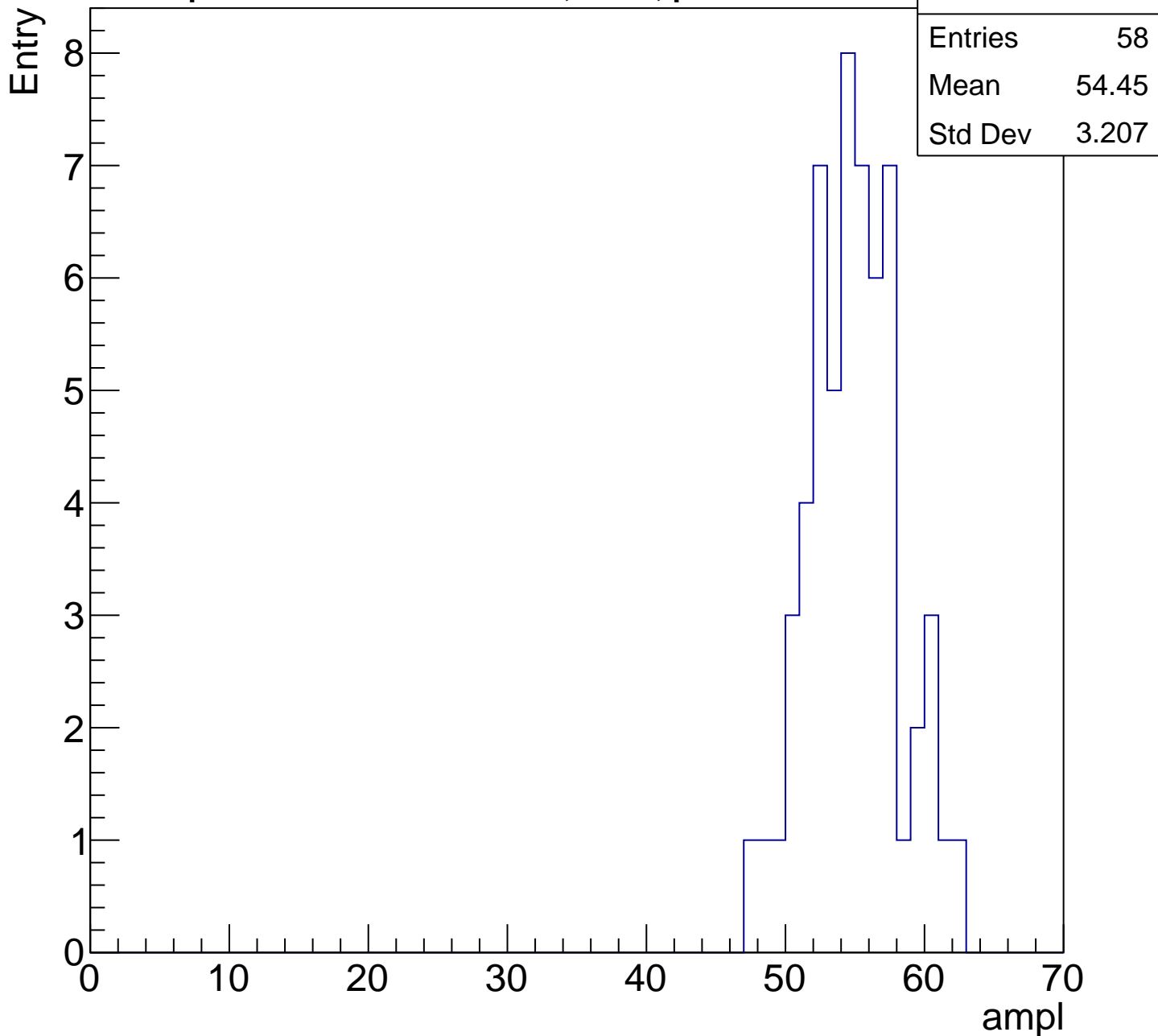
Entry

Entries	61
Mean	48.61
Std Dev	3.451



# B1L103S, U1-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

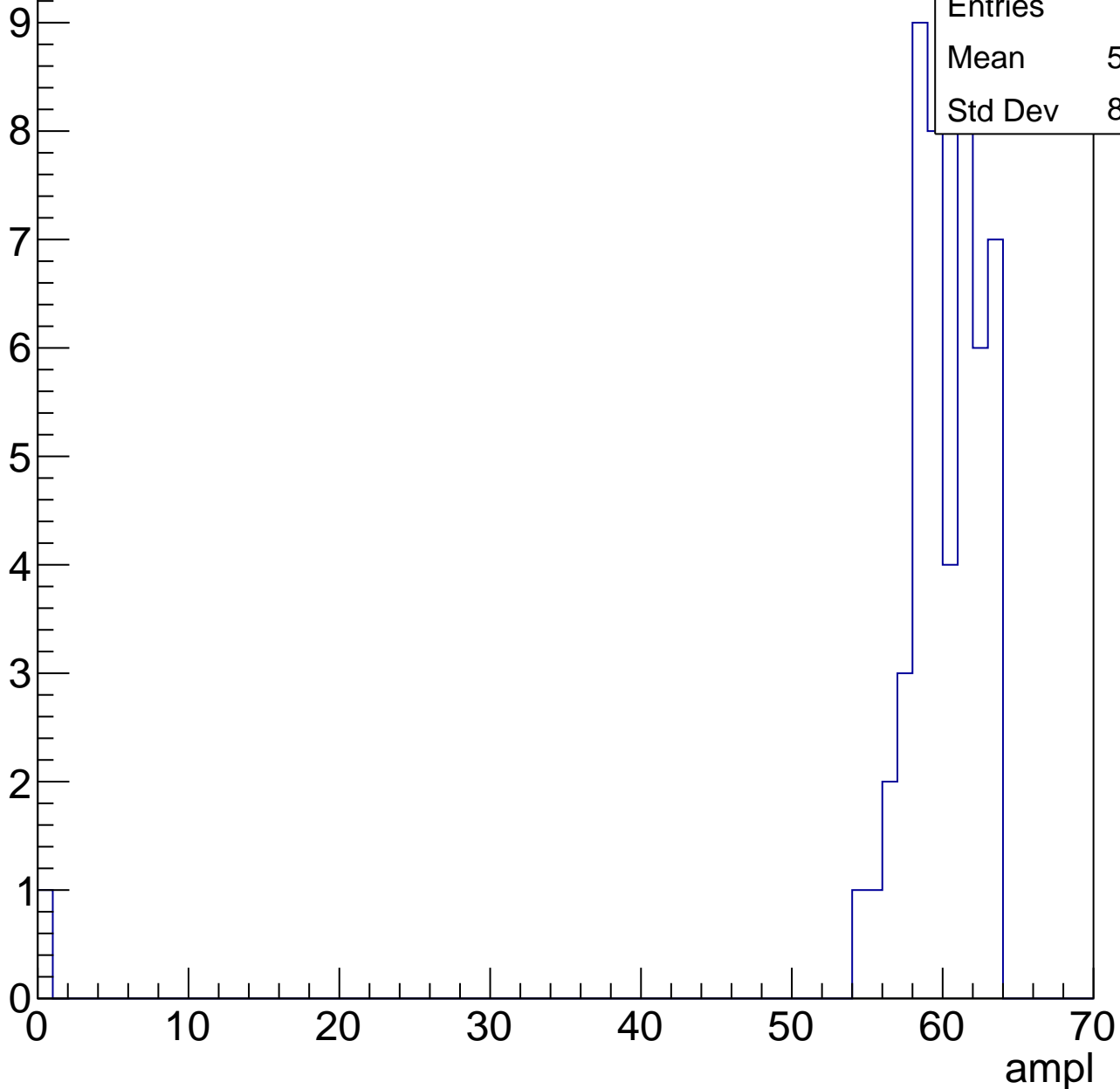


# B1L103S, U1-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	58.59
Std Dev	8.584



# B1L103S, U1-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries	9
Mean	61.67
Std Dev	1.247



# B1L103S, U1-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U1-ch19, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	84
Mean	28.25
Std Dev	5.223

**Gaus mean : 28.7531**

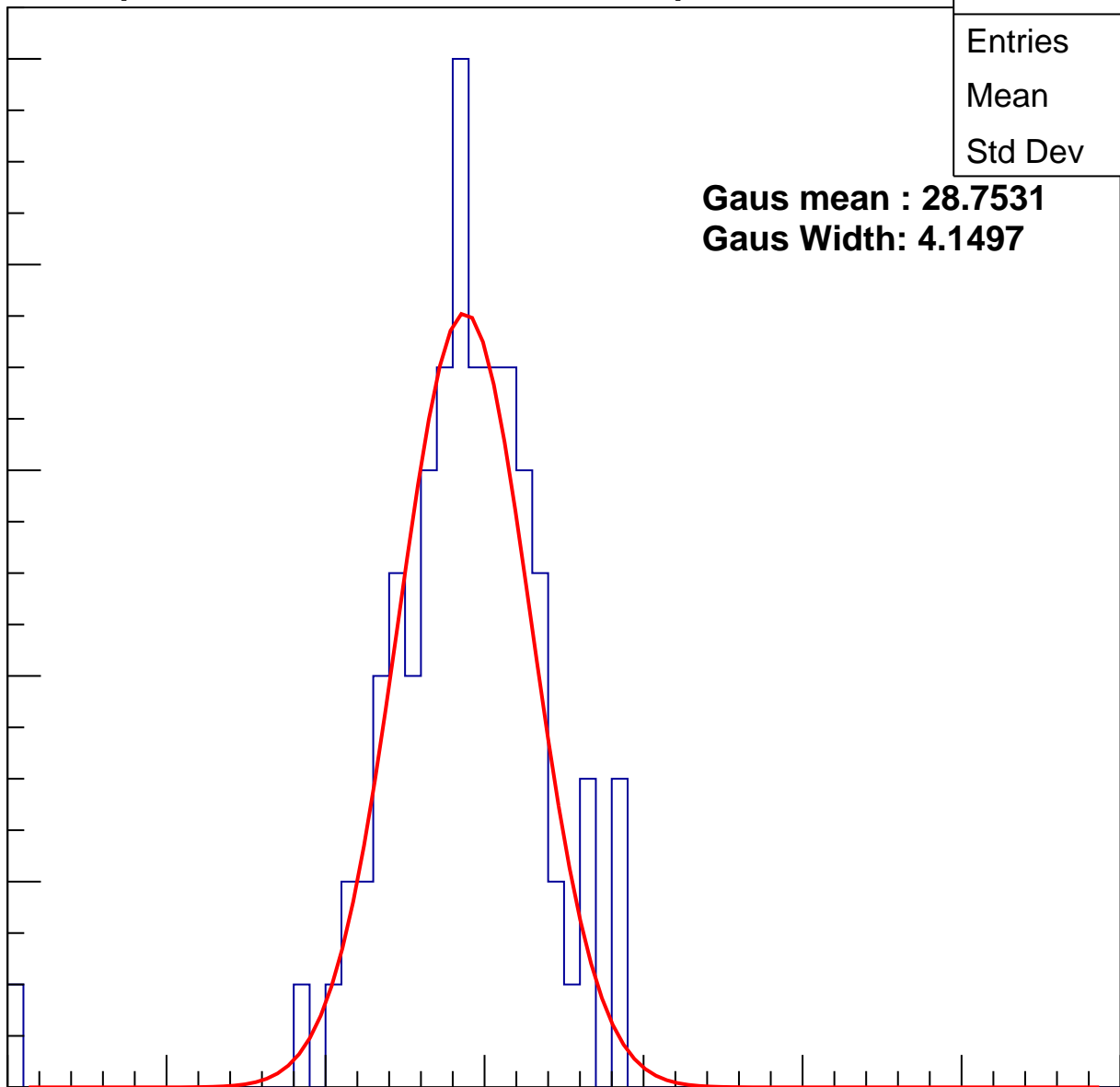
**Gaus Width: 4.1497**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U1-ch19, adc1

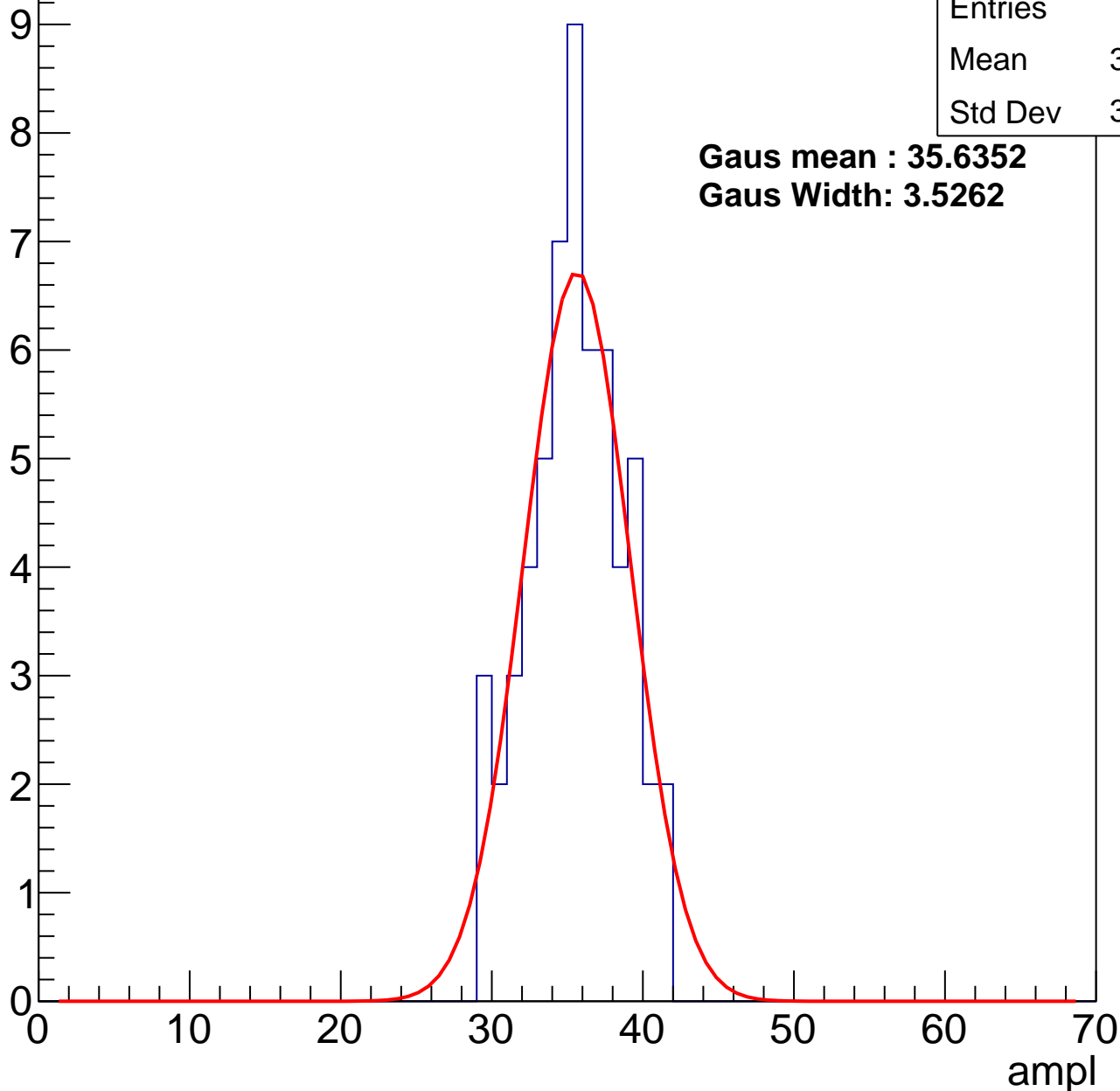
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	35.05
Std Dev	3.042

**Gaus mean : 35.6352**

**Gaus Width: 3.5262**



# B1L103S, U1-ch19, adc2

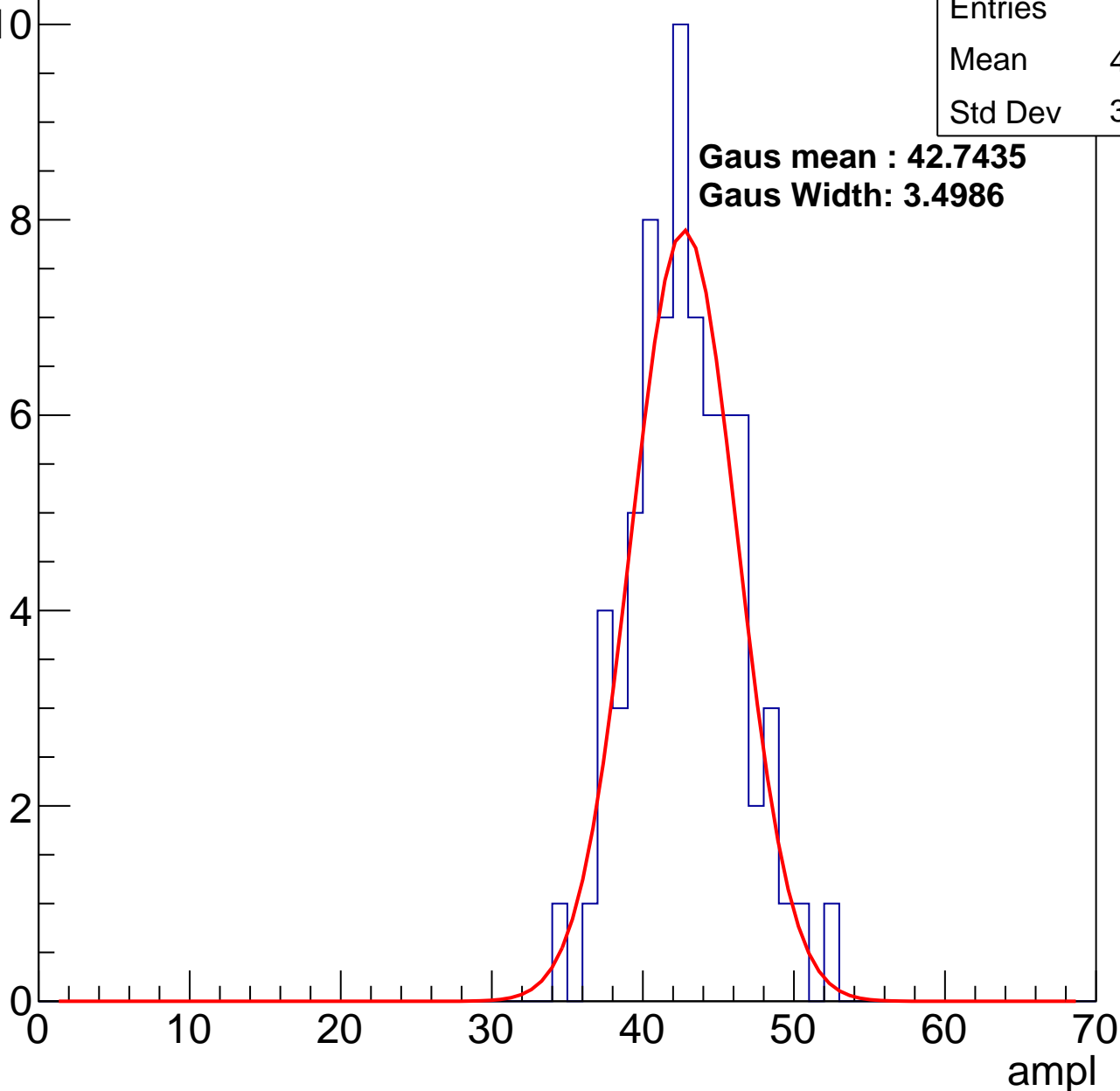
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	42.42
Std Dev	3.479

**Gaus mean : 42.7435**

**Gaus Width: 3.4986**

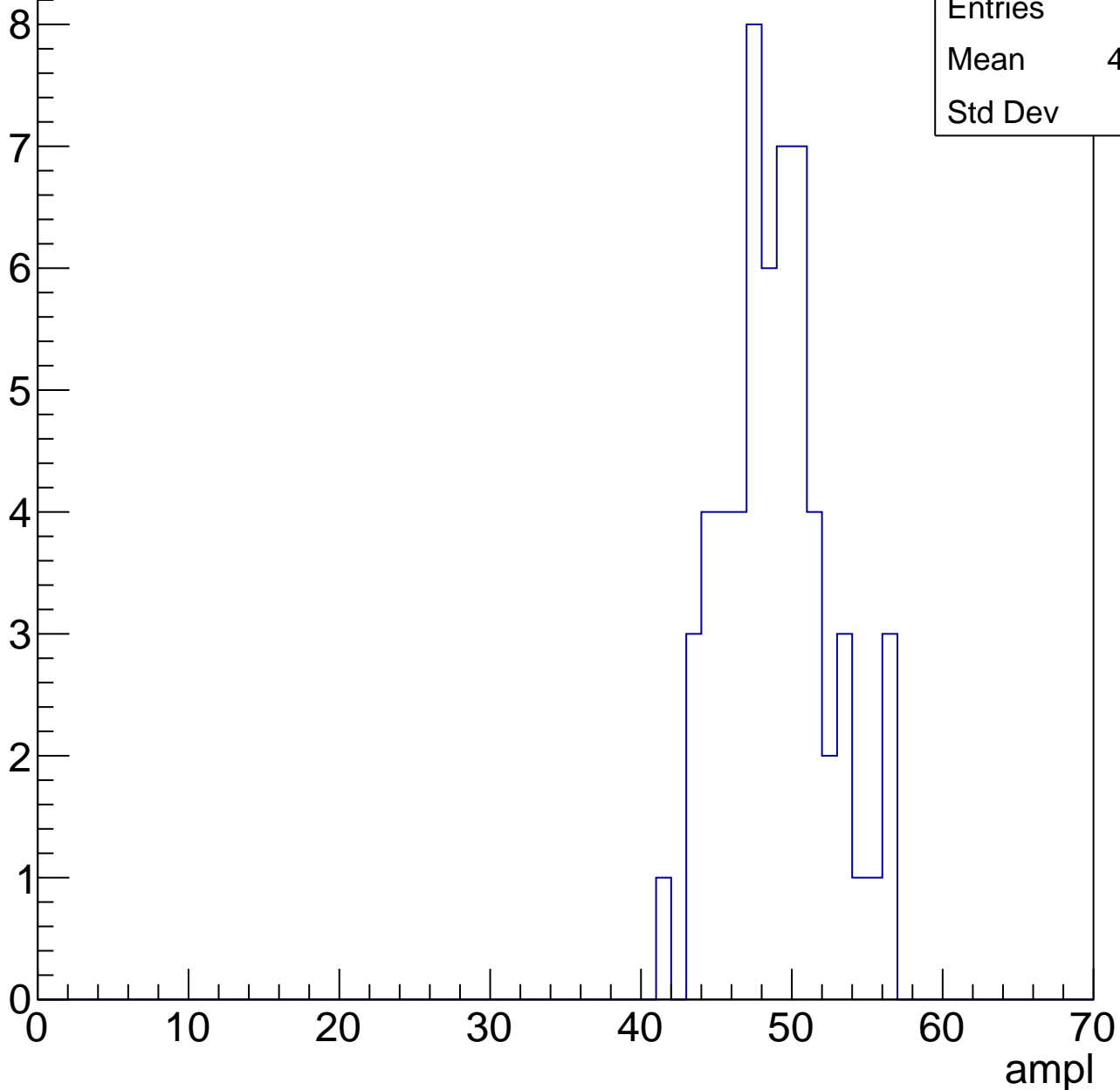


# B1L103S, U1-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

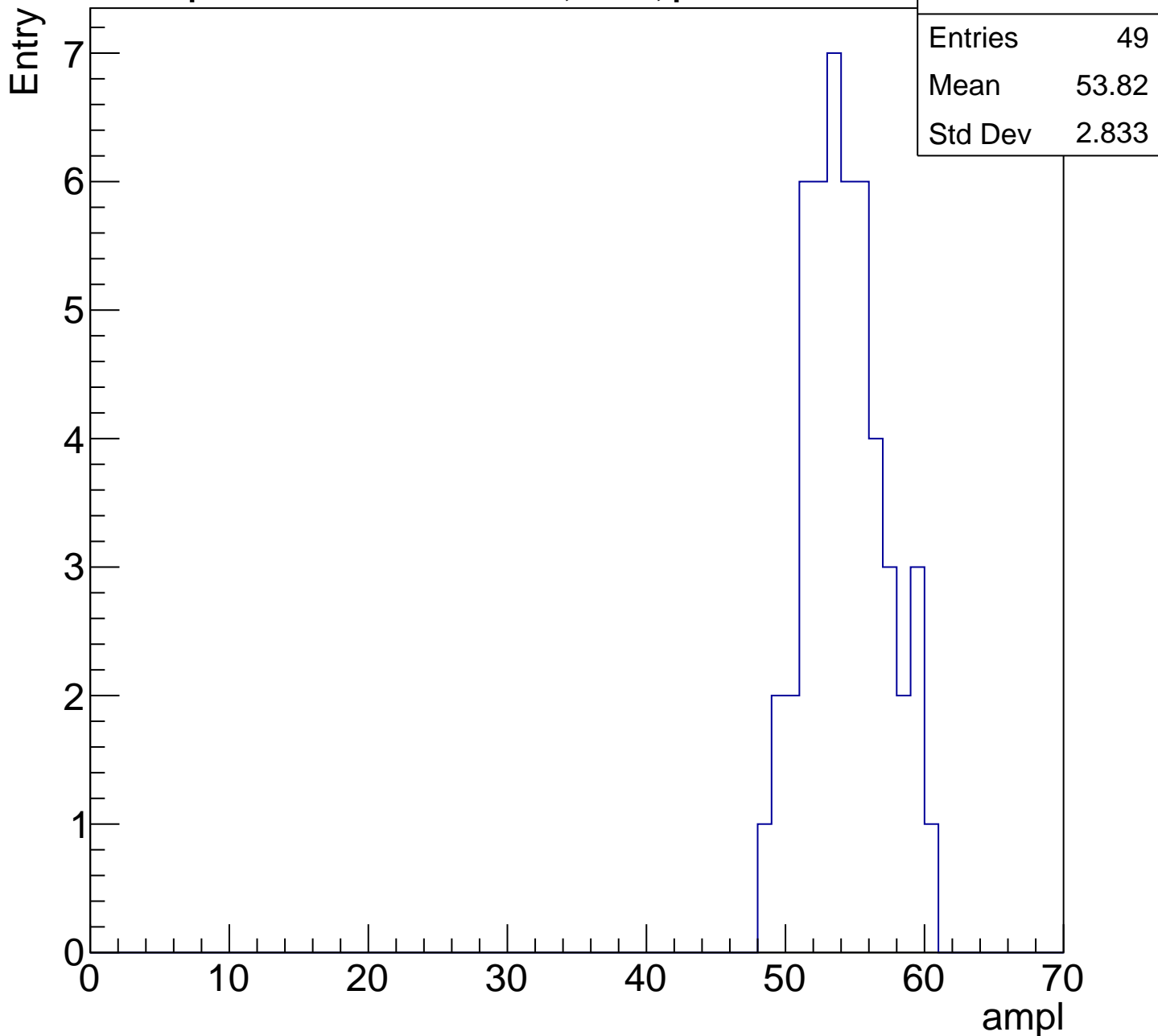
Entry

Entries	58
Mean	48.47
Std Dev	3.45



# B1L103S, U1-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

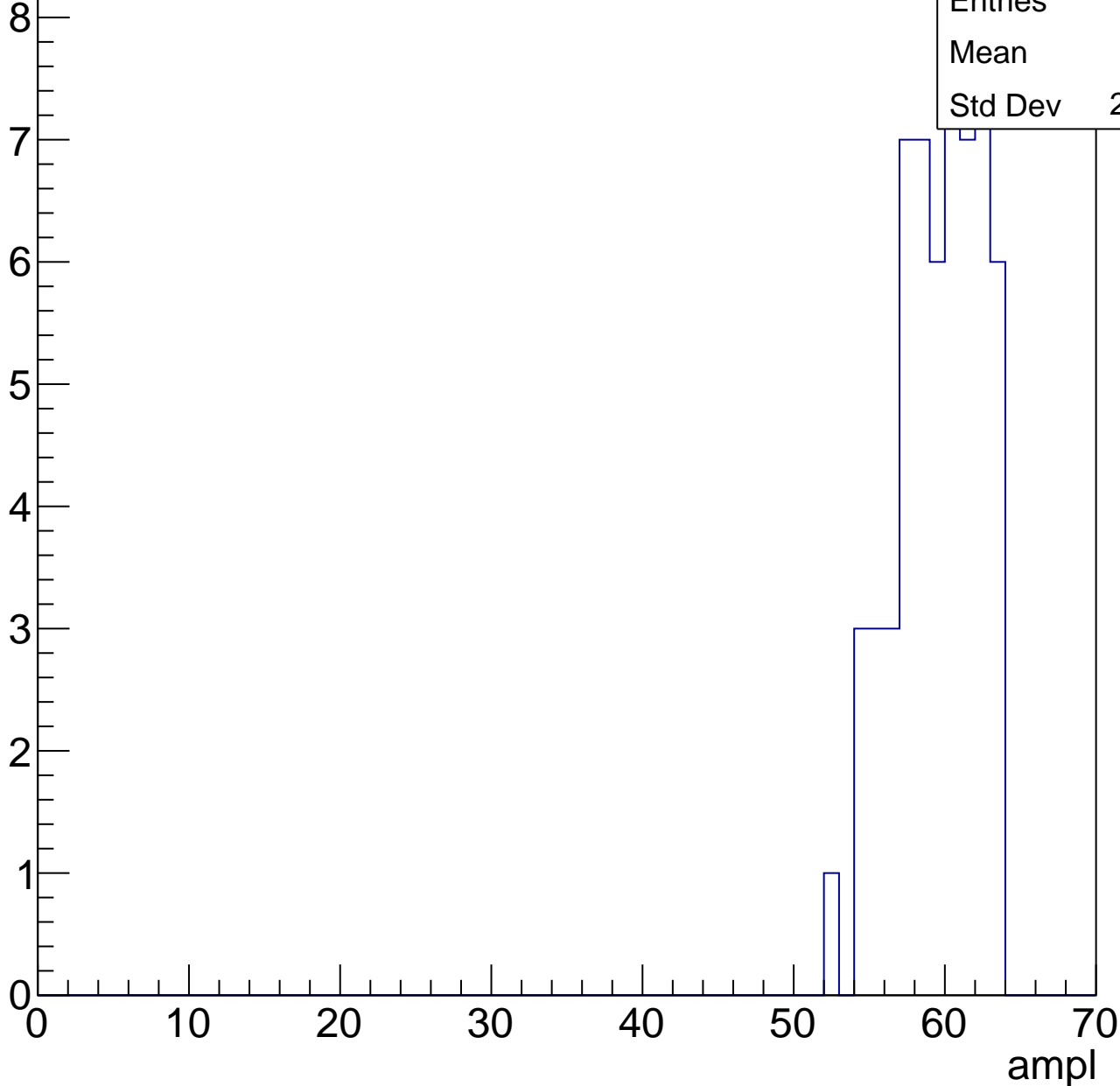


# B1L103S, U1-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

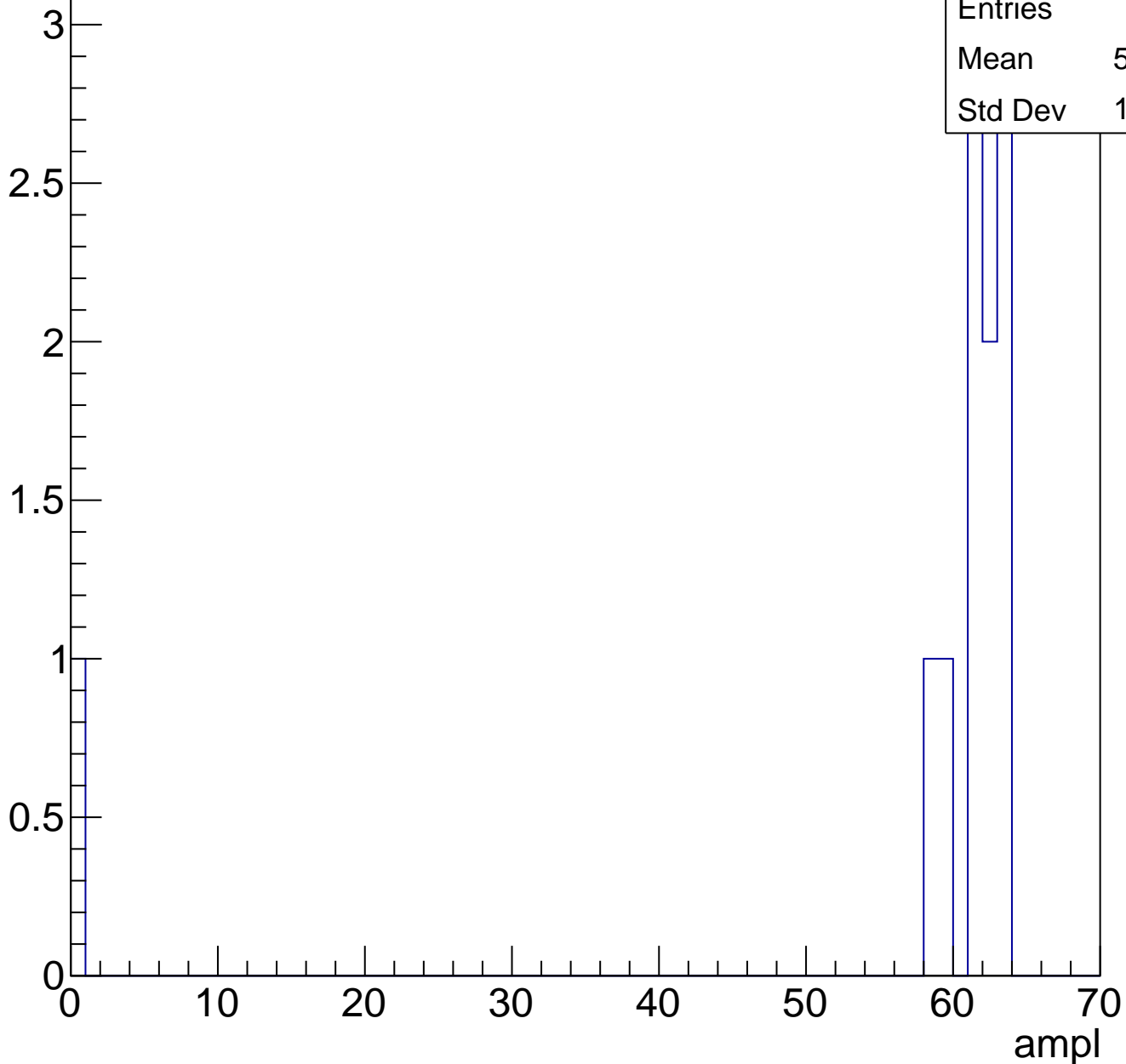
Entries	59
Mean	59.1
Std Dev	2.723



# B1L103S, U1-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

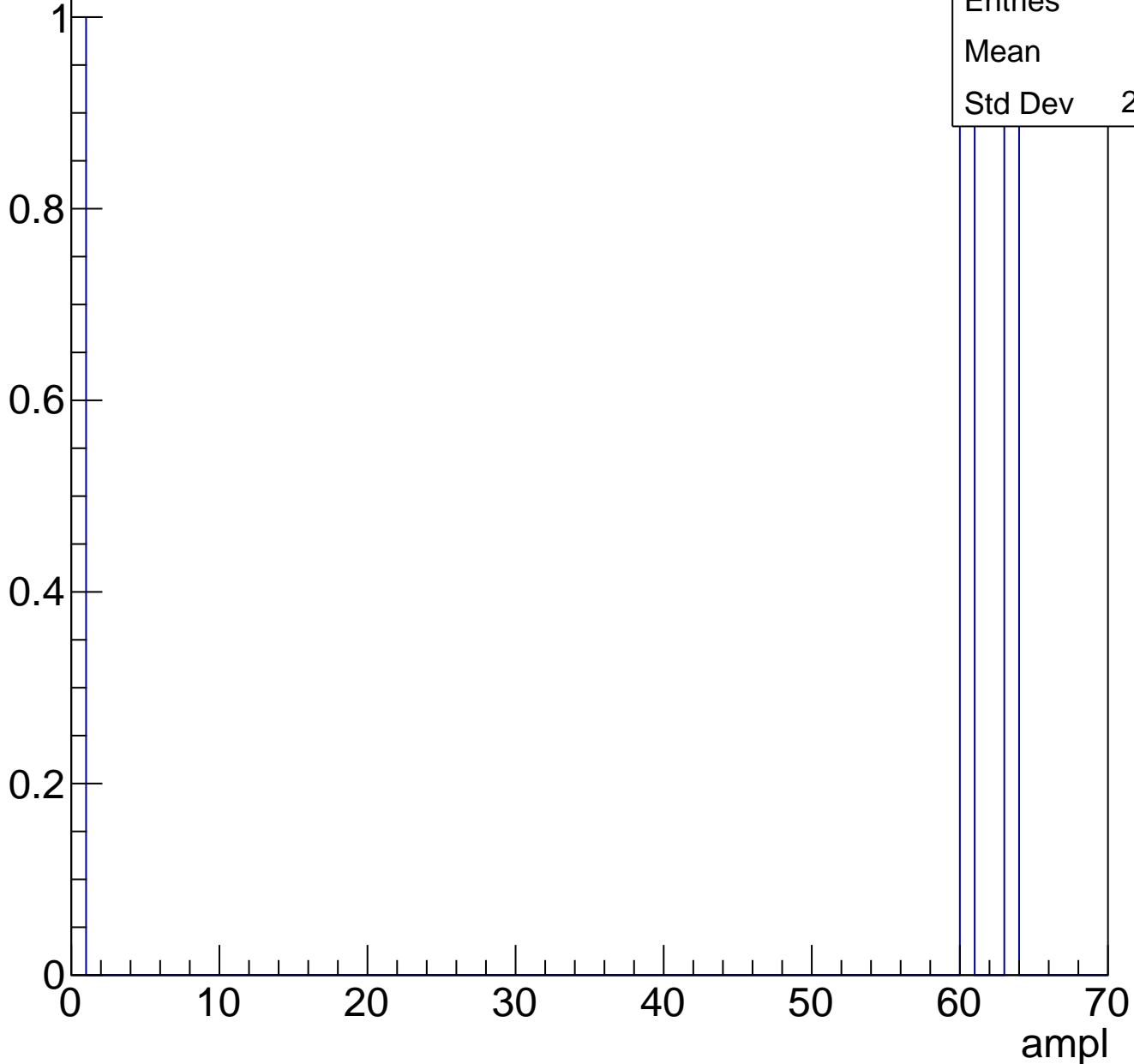




# B1L103S, U1-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch20, adc0

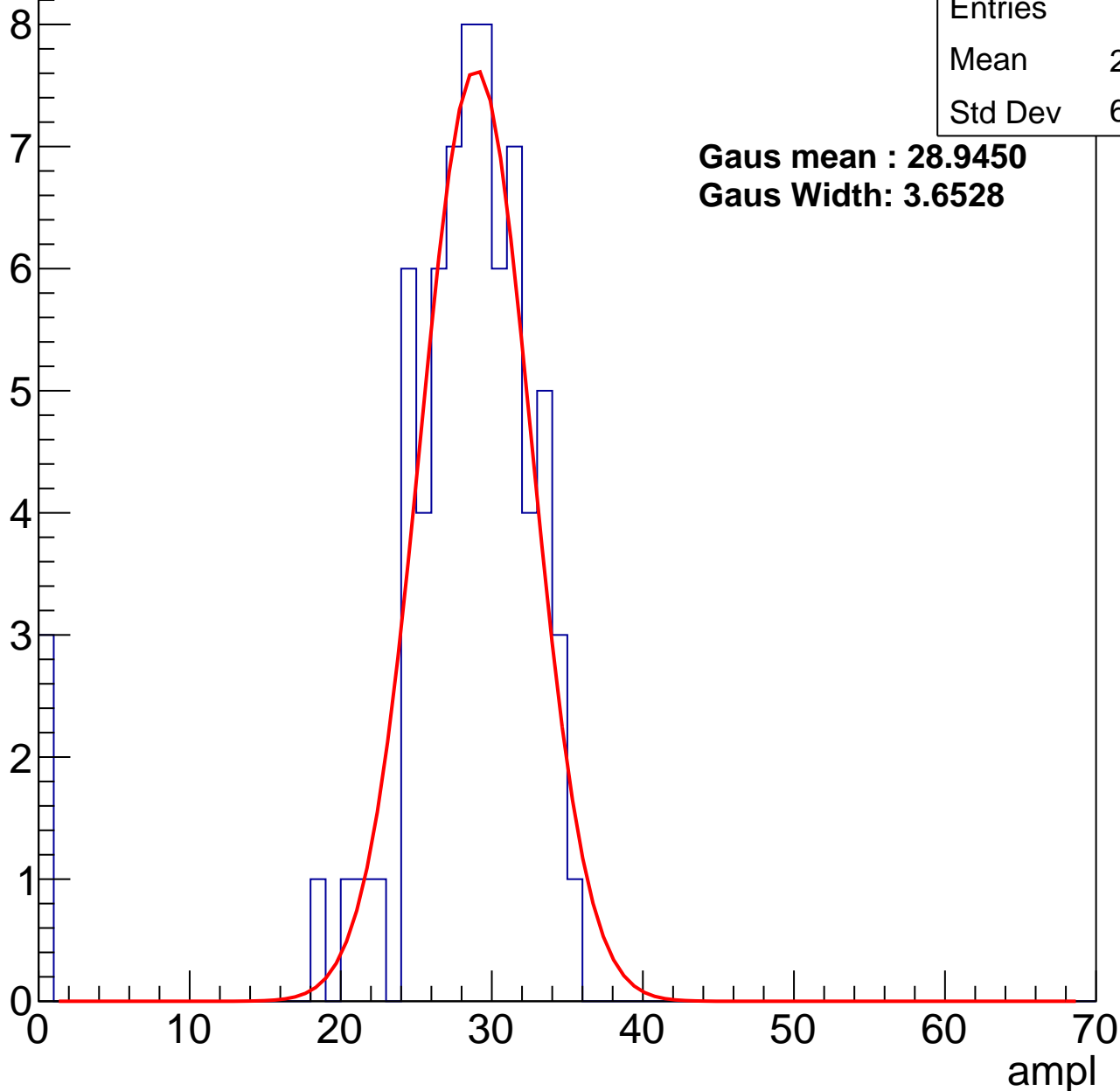
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	27.12
Std Dev	6.614

**Gaus mean : 28.9450**

**Gaus Width: 3.6528**



# B1L103S, U1-ch20, adc1

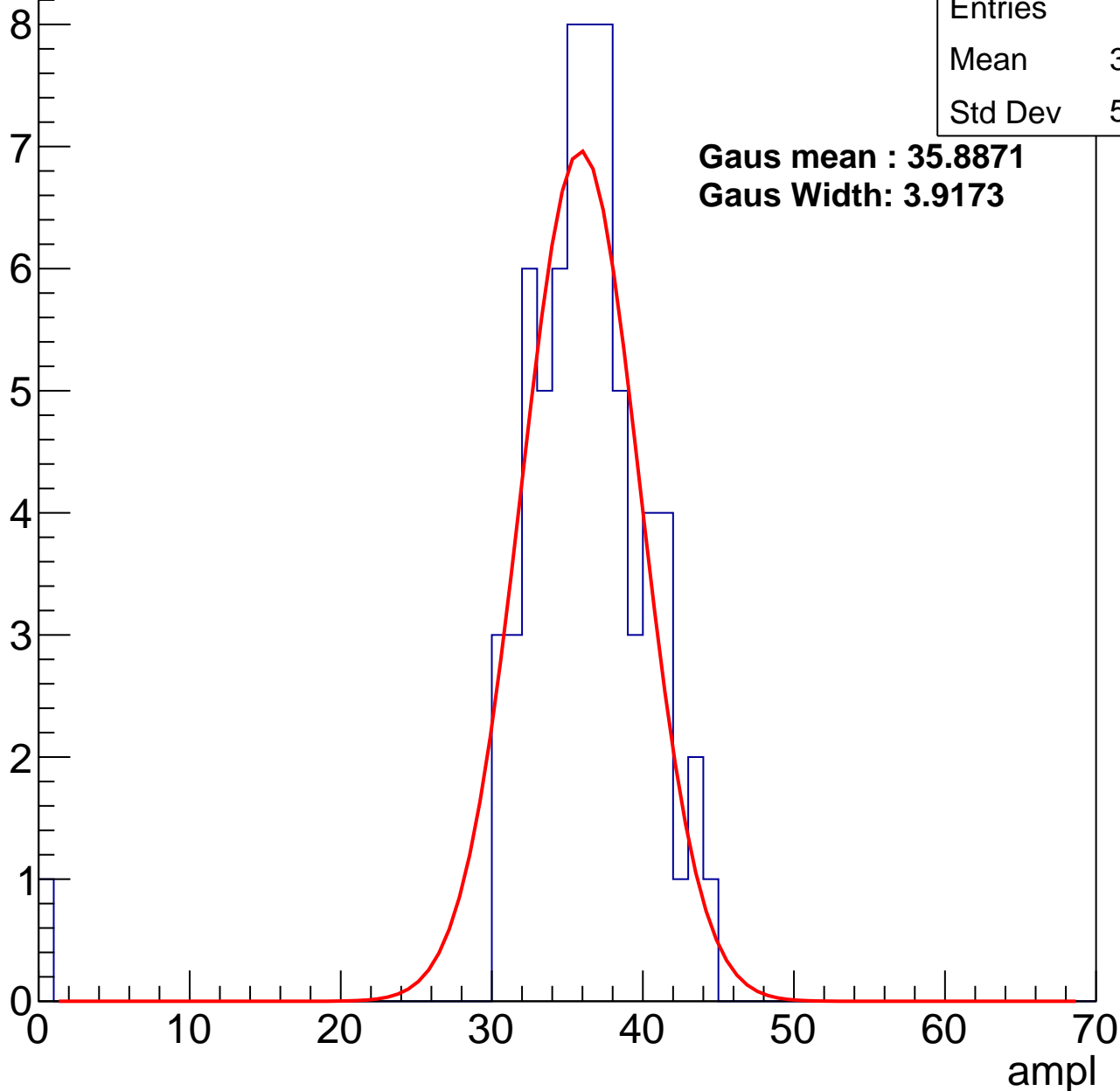
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	35.46
Std Dev	5.489

**Gaus mean : 35.8871**

**Gaus Width: 3.9173**



# B1L103S, U1-ch20, adc2

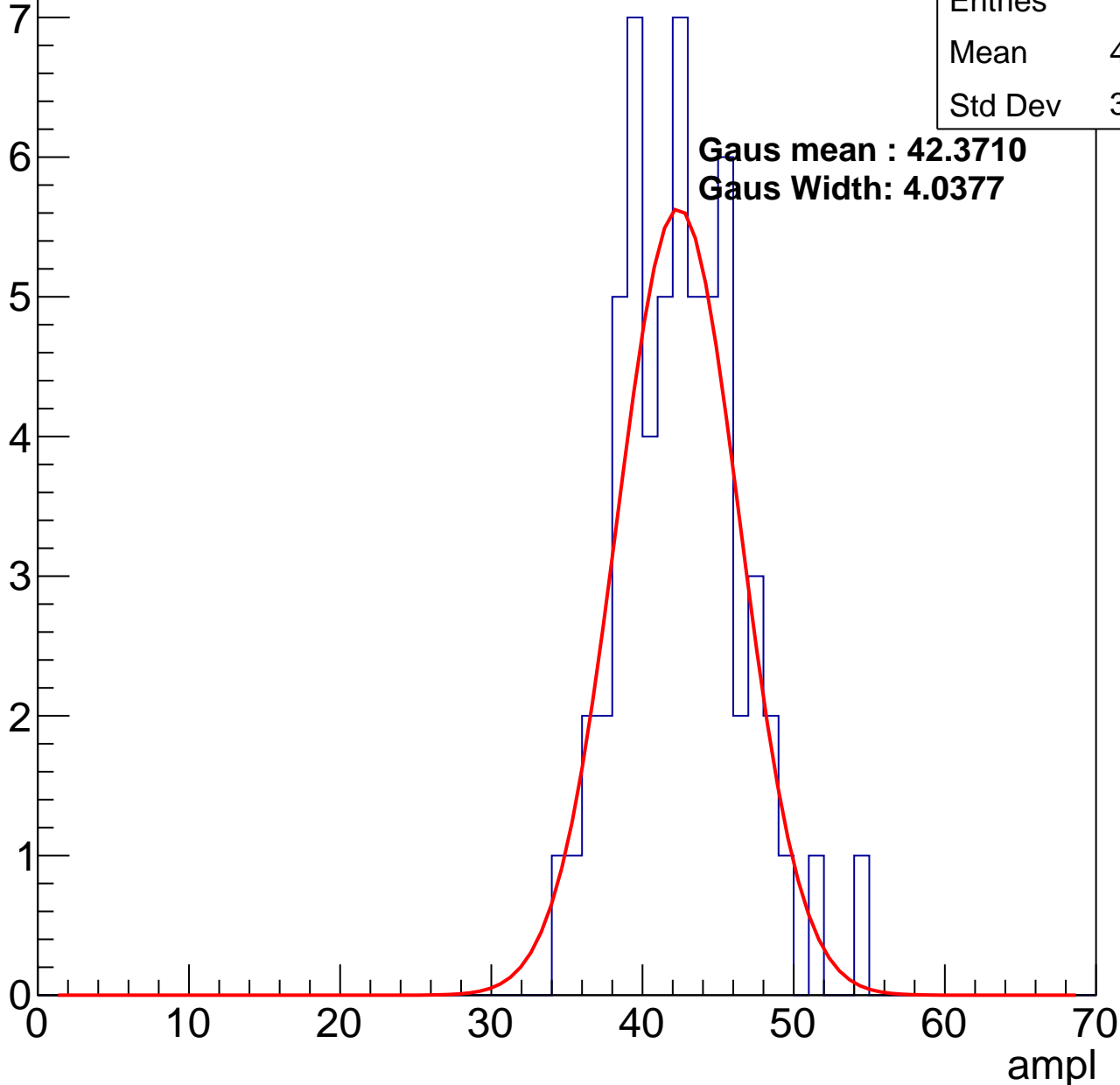
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	42.08
Std Dev	3.938

**Gaus mean : 42.3710**

**Gaus Width: 4.0377**

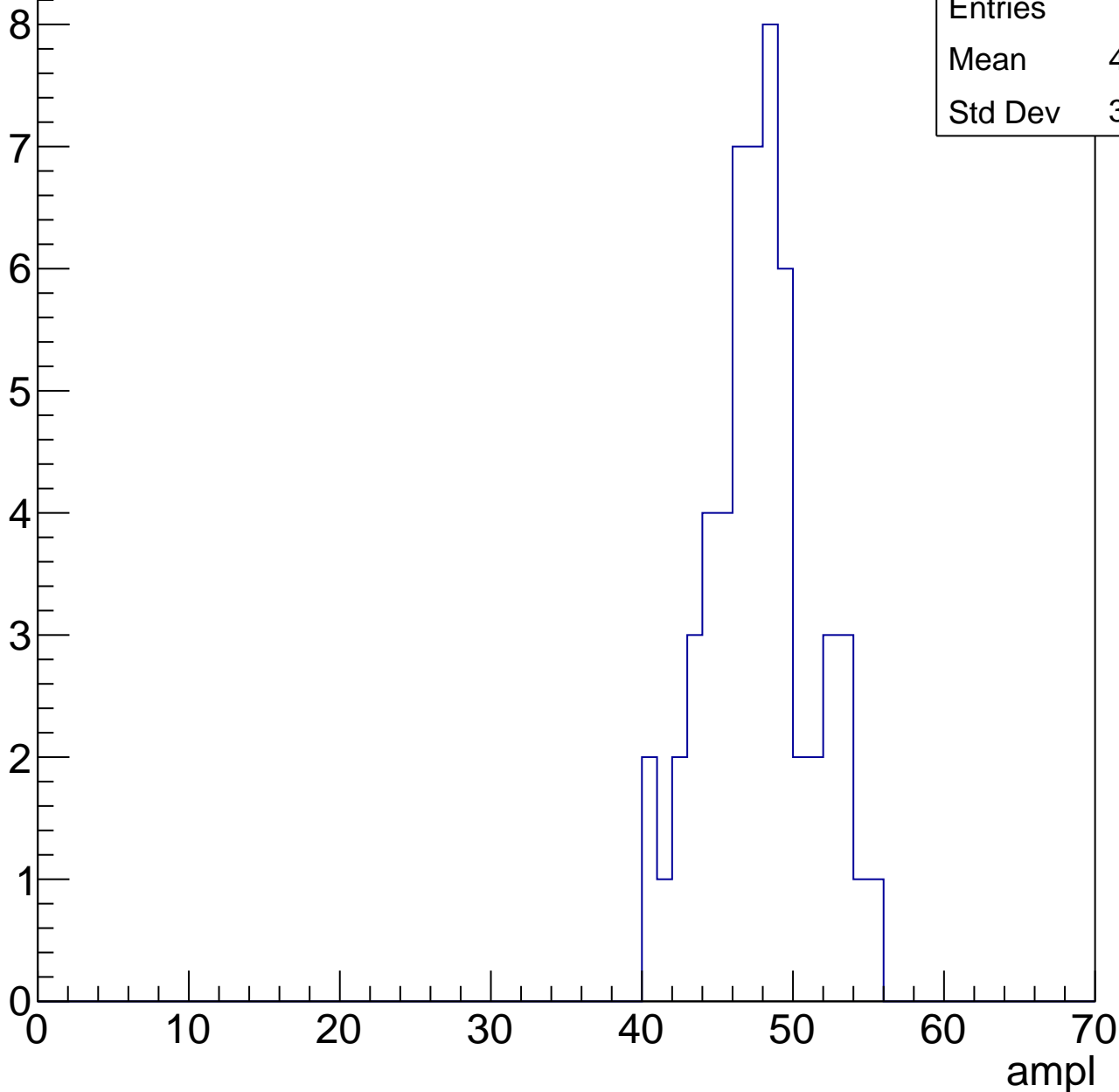


# B1L103S, U1-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	47.23
Std Dev	3.449

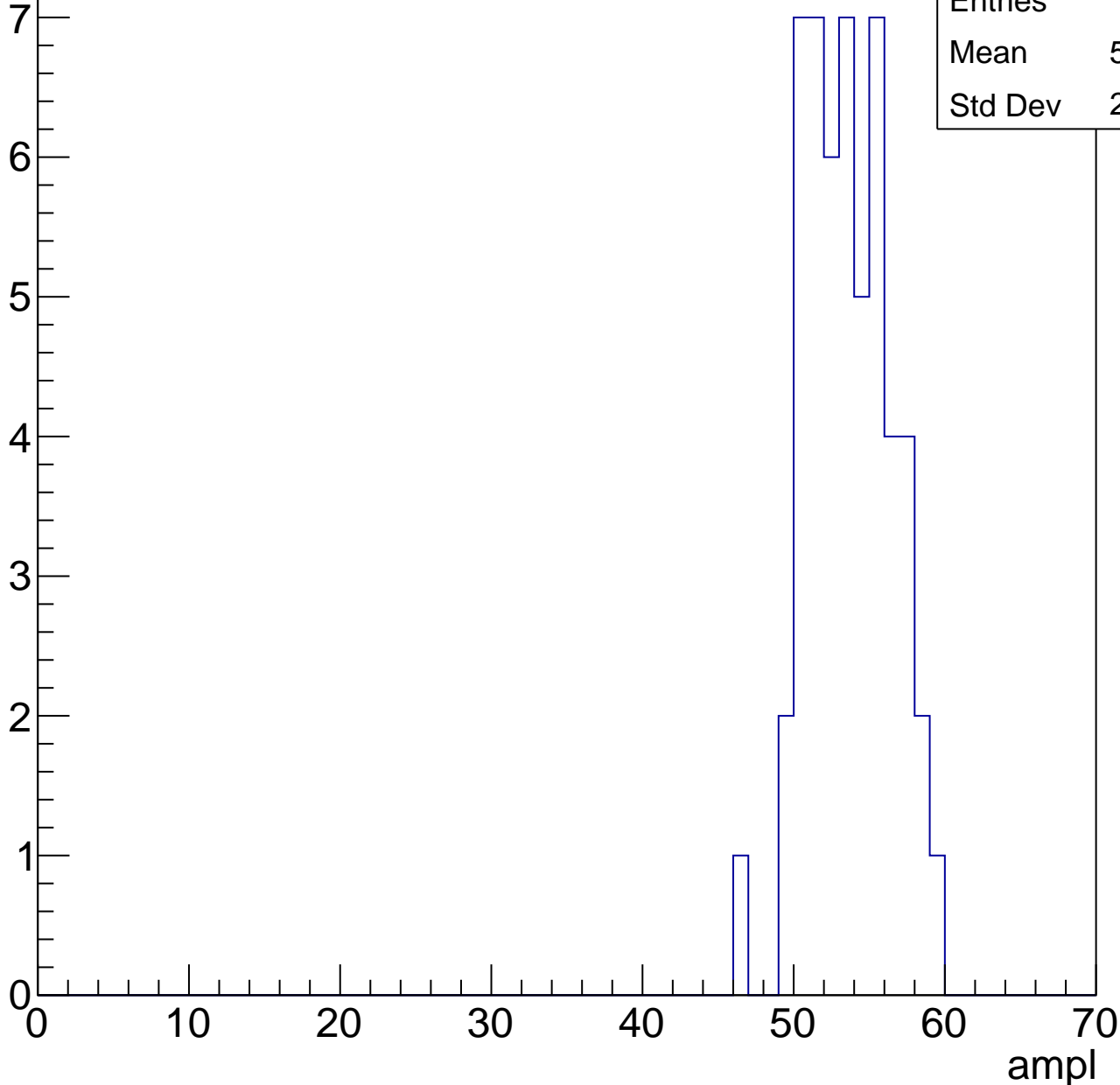


# B1L103S, U1-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	53.13
Std Dev	2.734

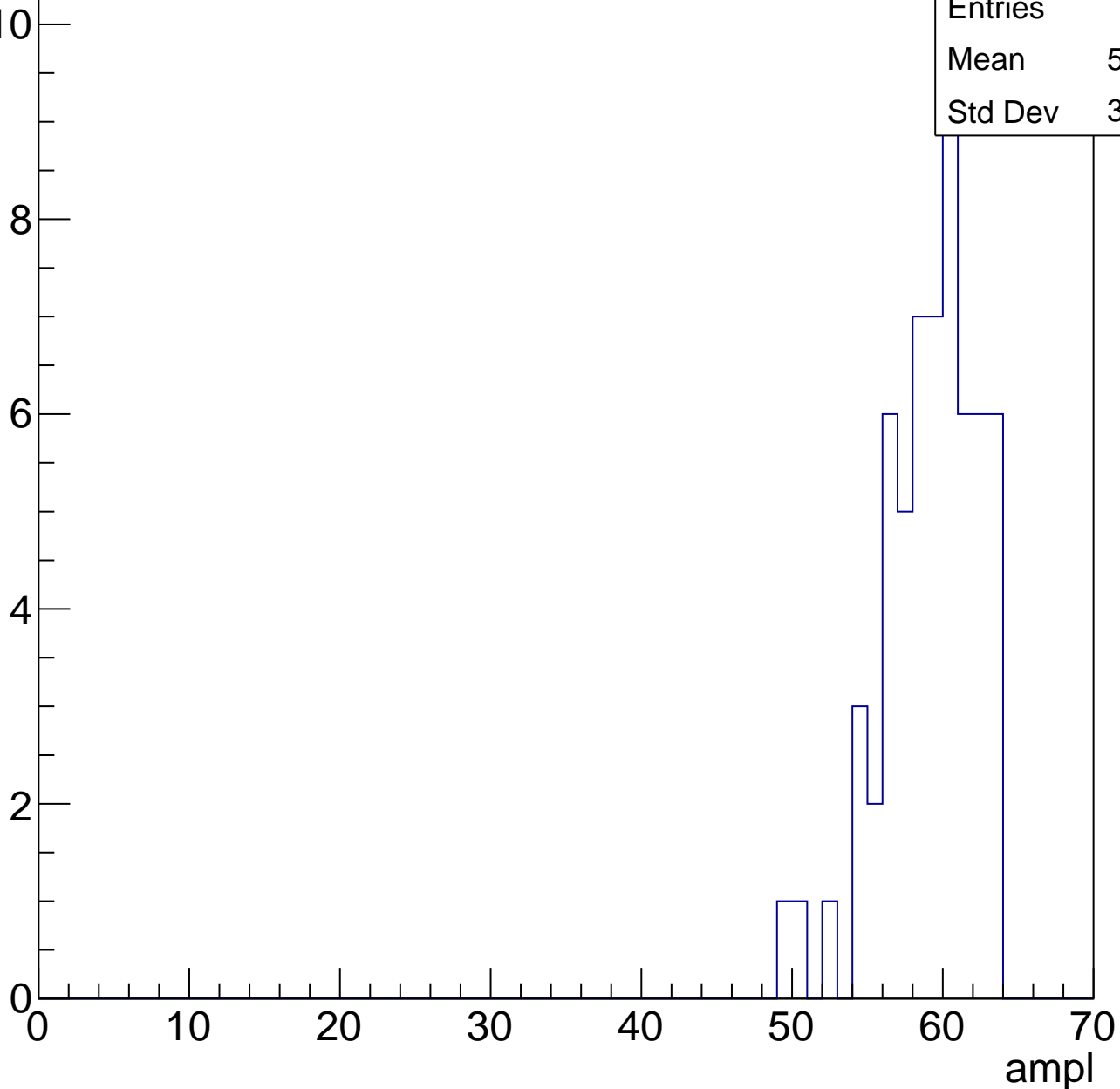


# B1L103S, U1-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

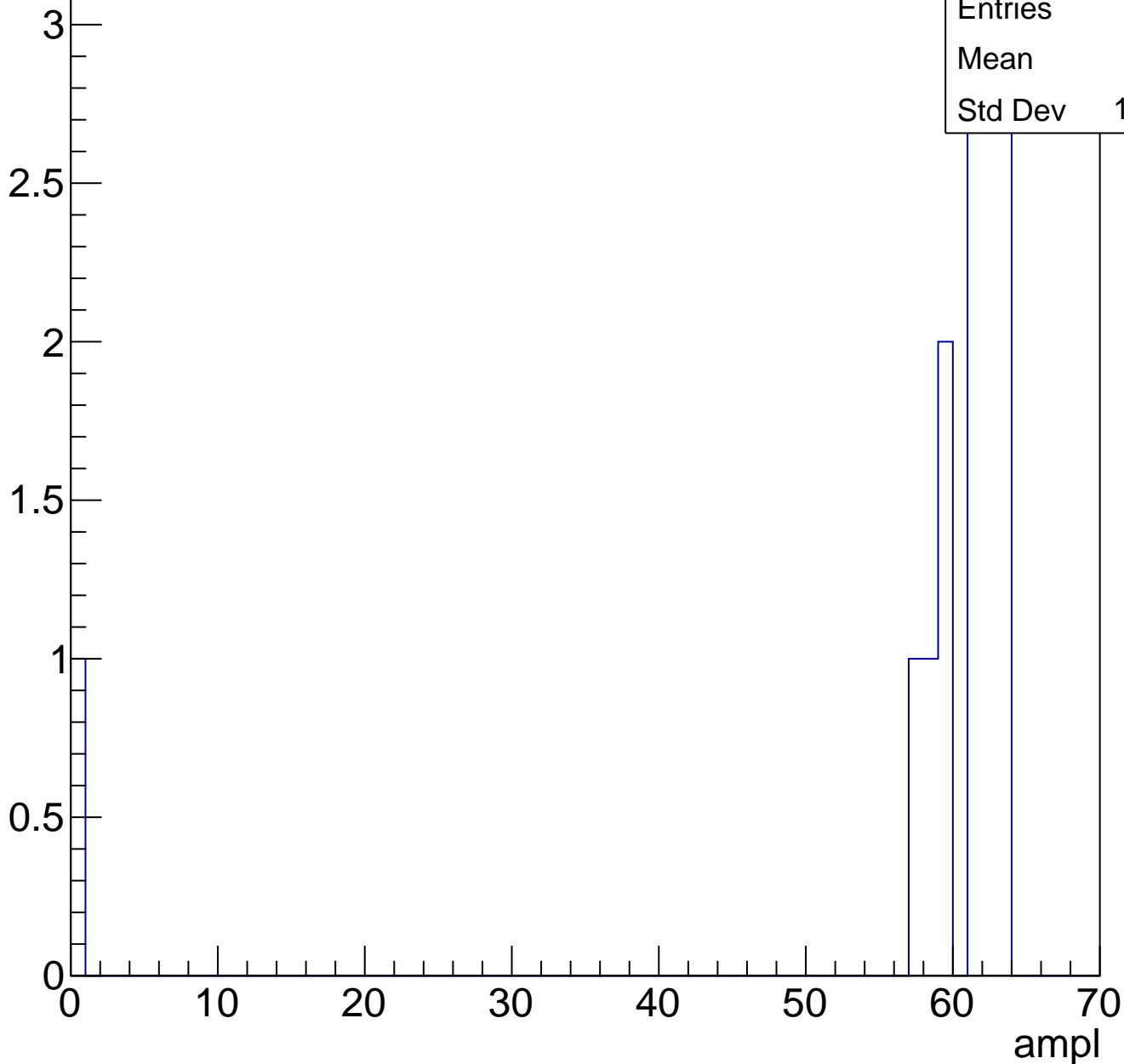
Entries	61
Mean	58.67
Std Dev	3.124



# B1L103S, U1-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

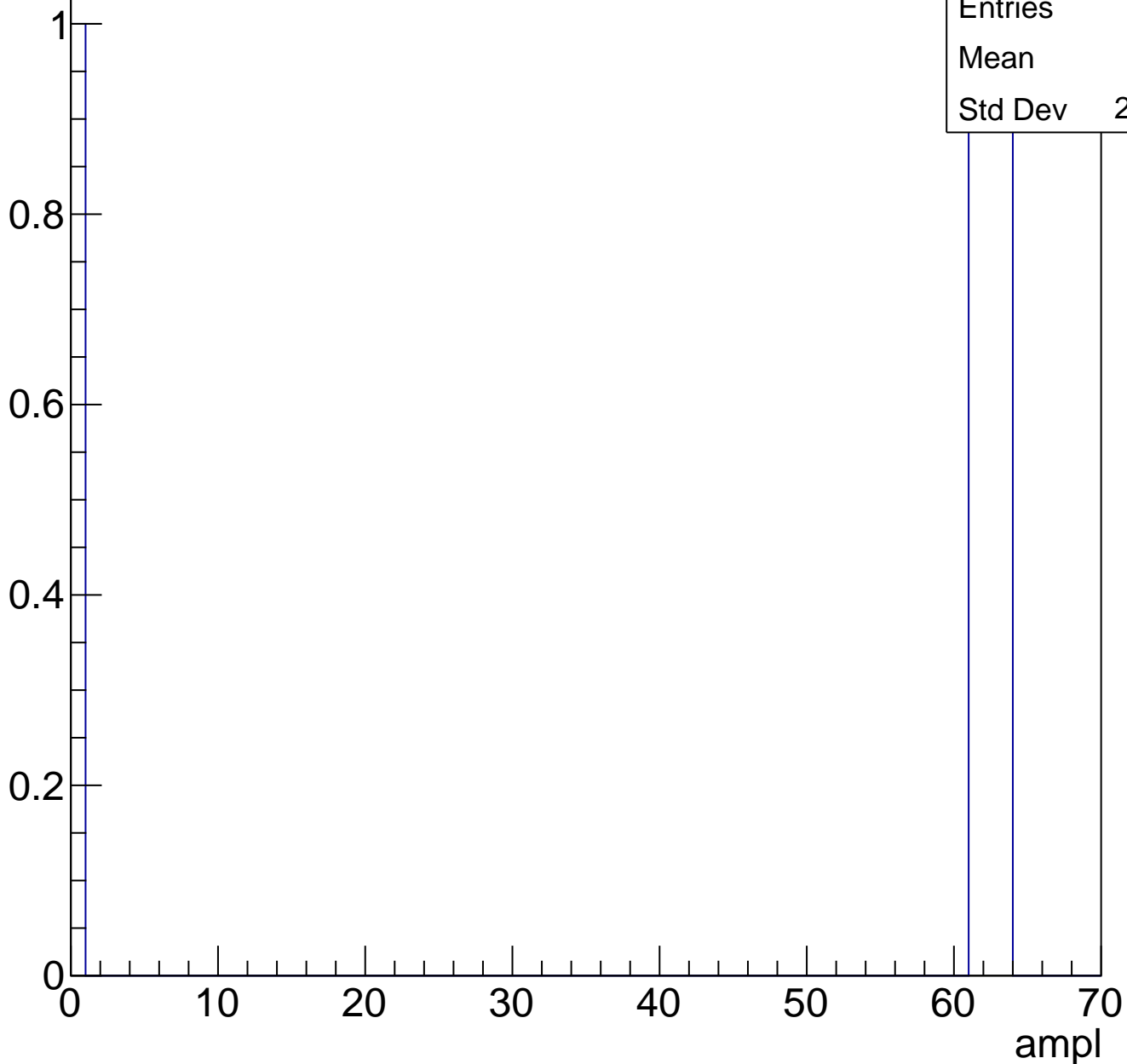




# B1L103S, U1-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch21, adc0

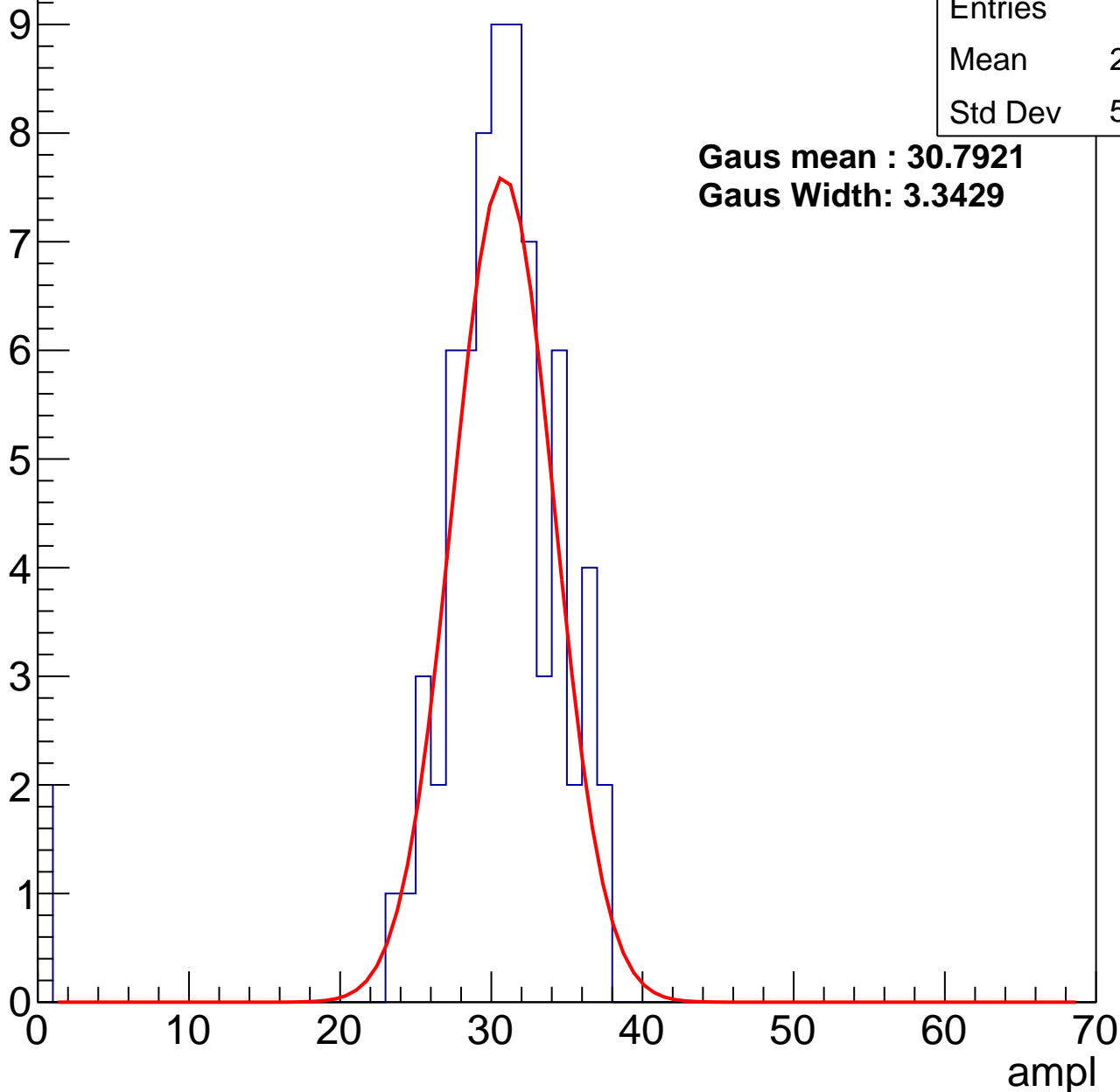
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	29.58
Std Dev	5.954

**Gaus mean : 30.7921**

**Gaus Width: 3.3429**



# B1L103S, U1-ch21, adc1

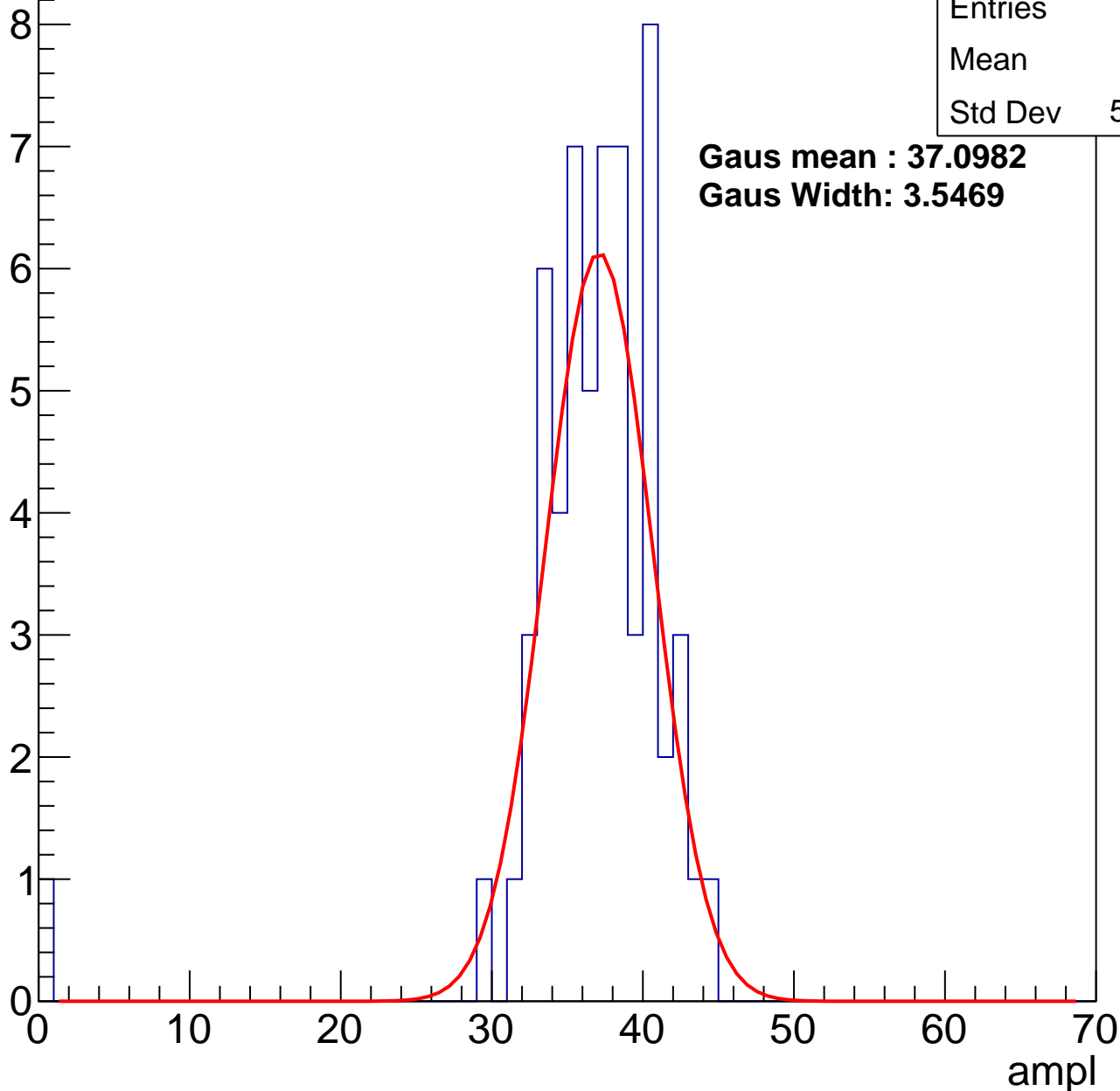
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	36.2
Std Dev	5.706

**Gaus mean : 37.0982**

**Gaus Width: 3.5469**



# B1L103S, U1-ch21, adc2

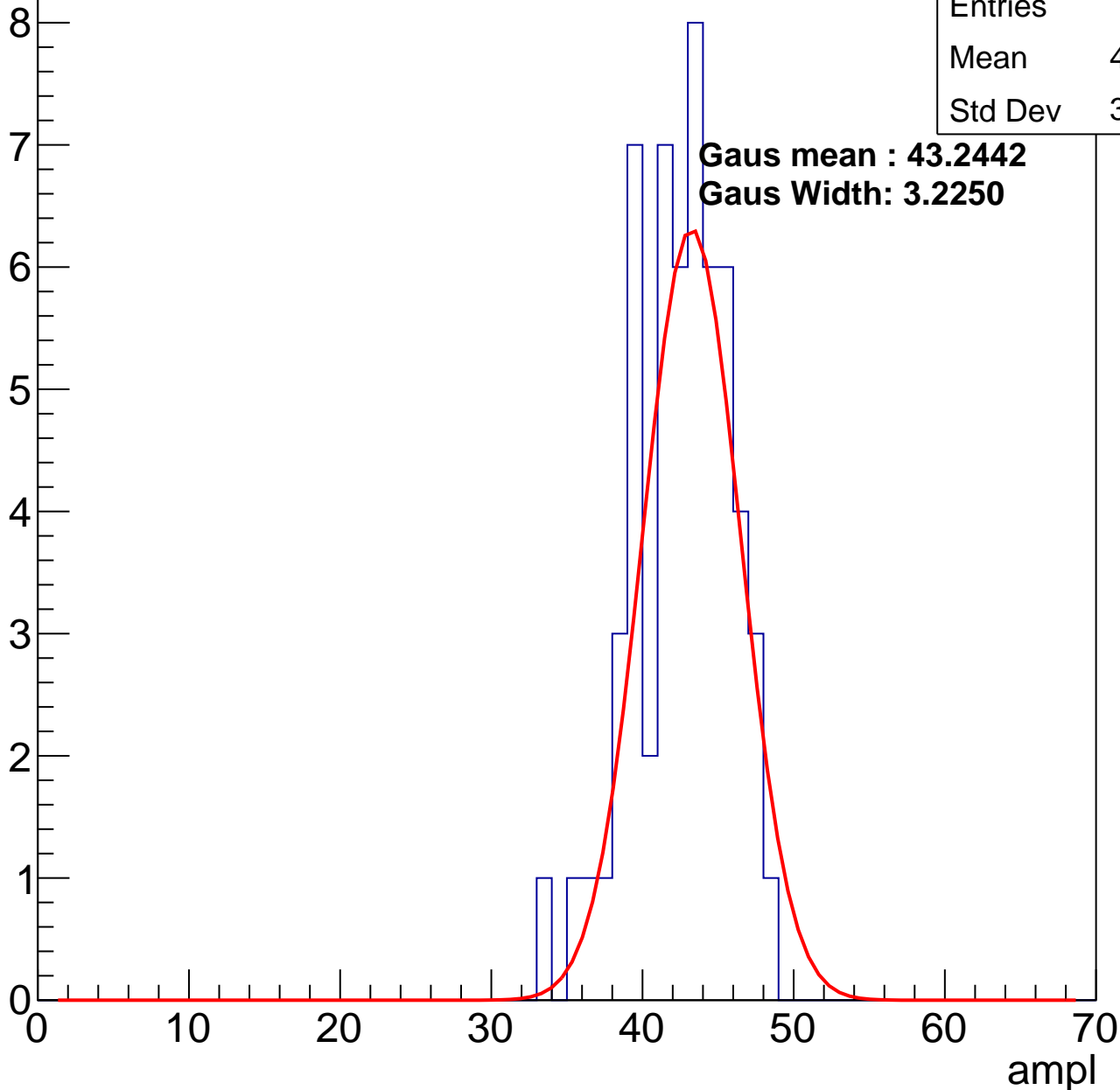
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	42.07
Std Dev	3.184

**Gaus mean : 43.2442**

**Gaus Width: 3.2250**

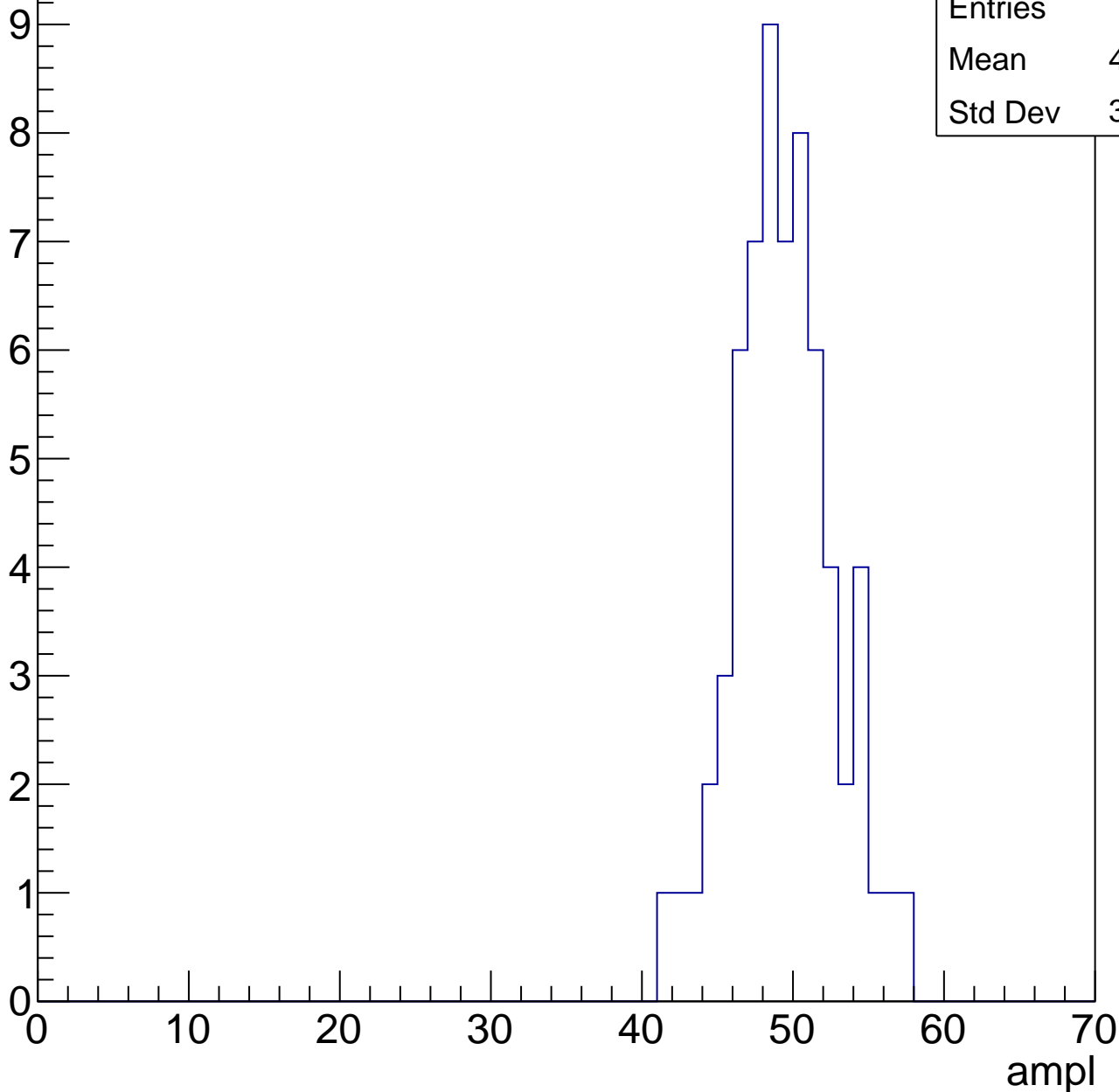


# B1L103S, U1-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

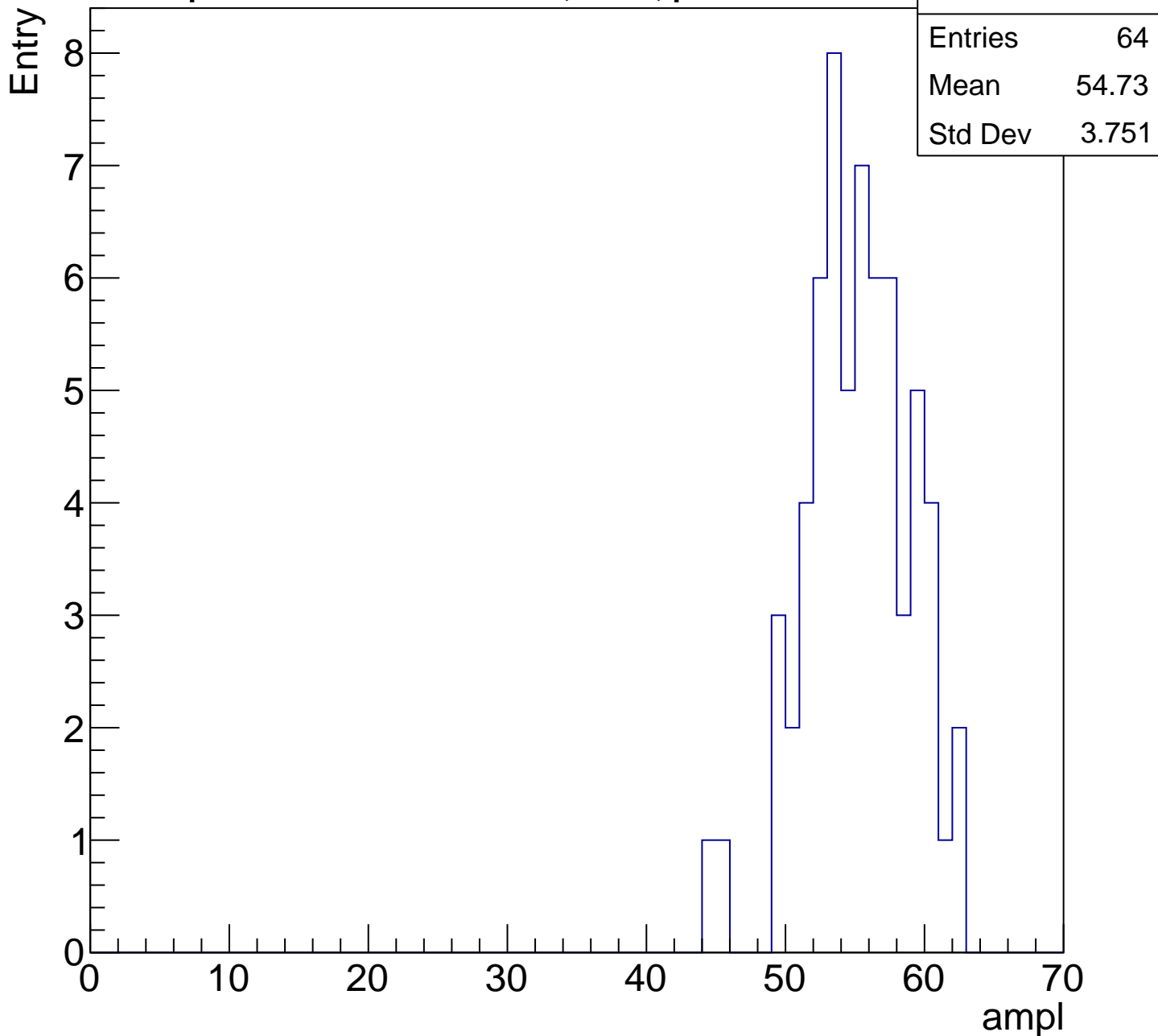
Entry

Entries	64
Mean	48.95
Std Dev	3.276



# B1L103S, U1-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

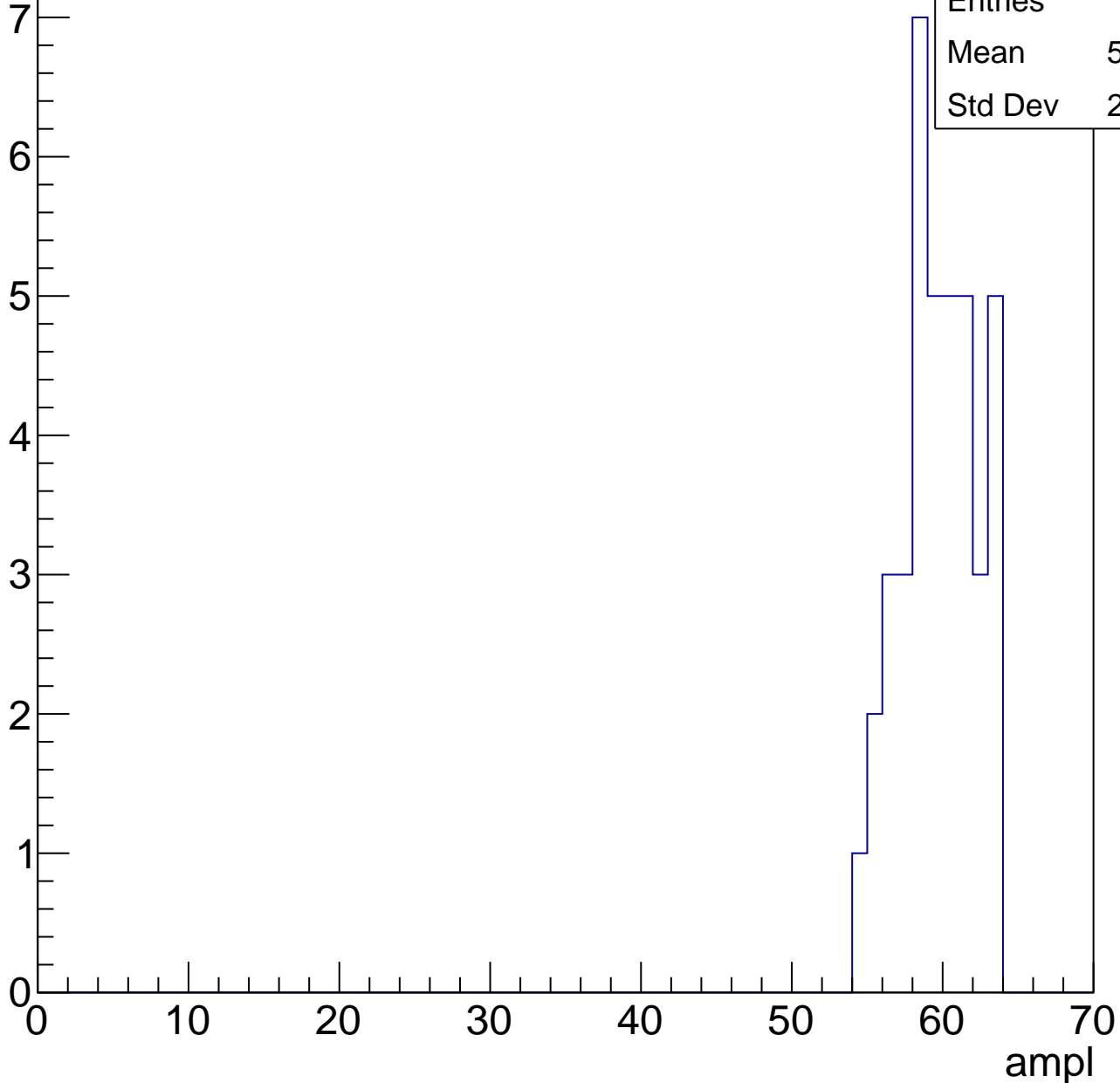


# B1L103S, U1-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	39
Mean	59.23
Std Dev	2.444

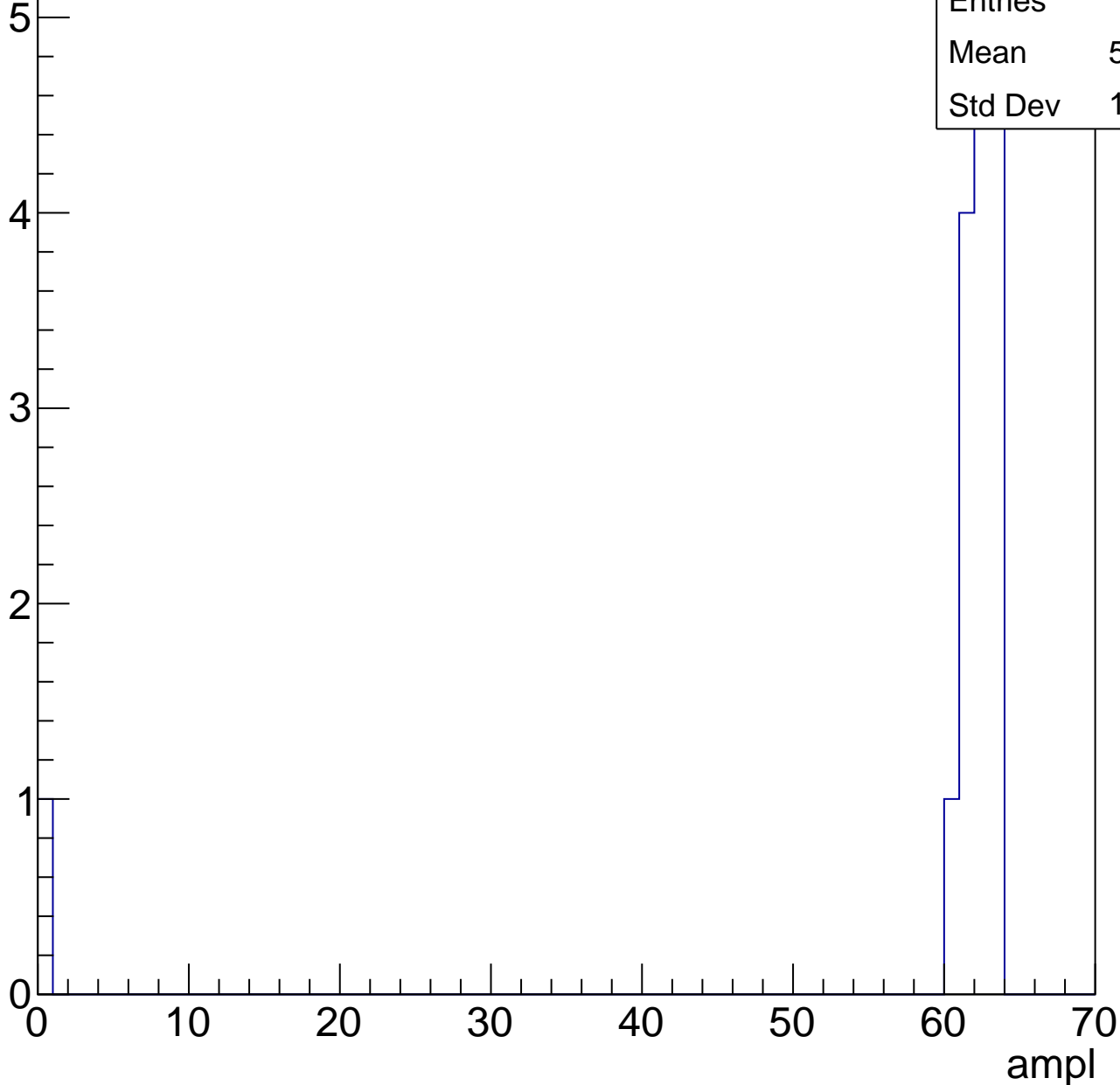


# B1L103S, U1-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	16
Mean	58.06
Std Dev	15.02





# B1L103S, U1-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch22, adc0

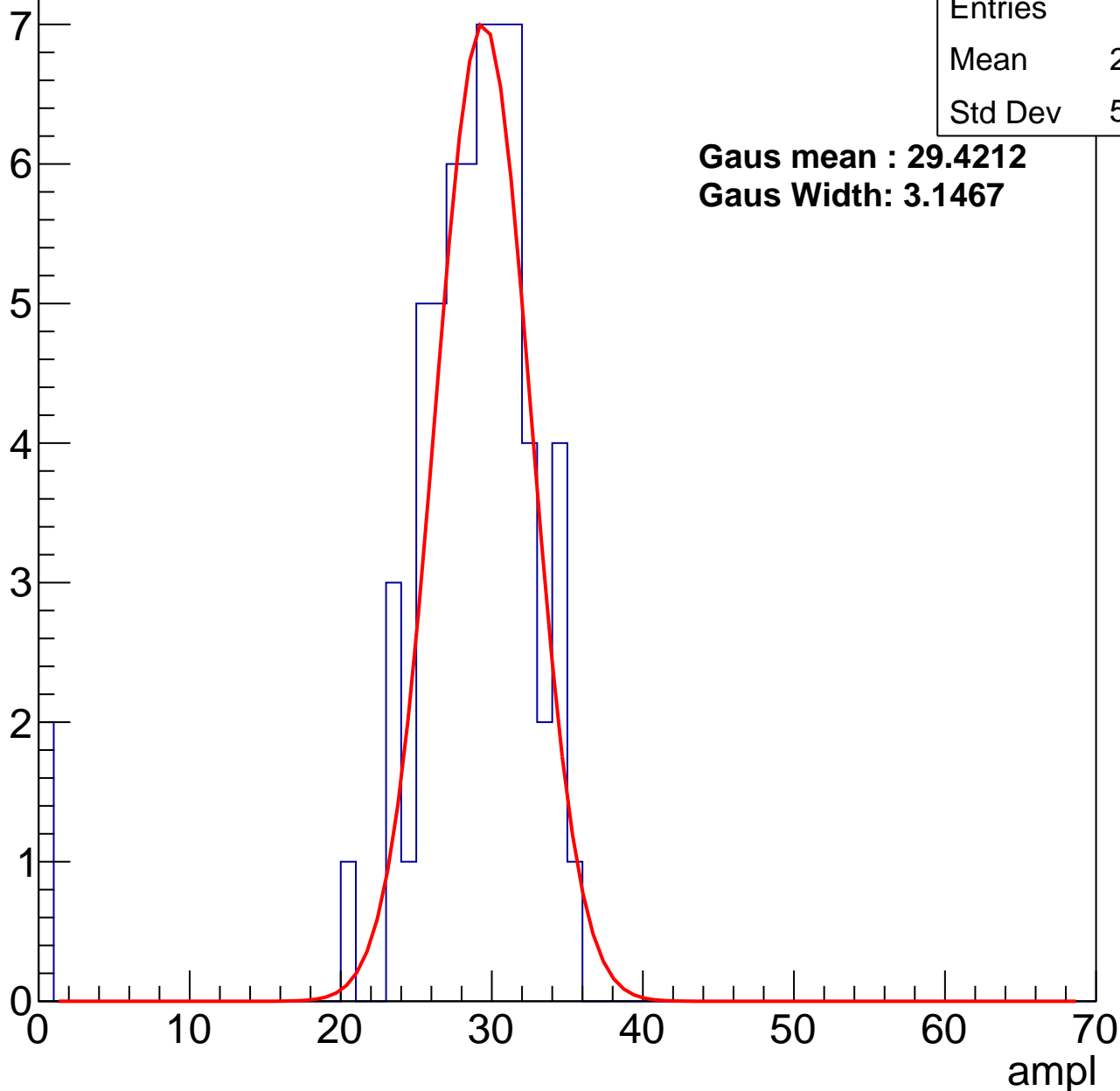
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	27.75
Std Dev	5.999

**Gaus mean : 29.4212**

**Gaus Width: 3.1467**



# B1L103S, U1-ch22, adc1

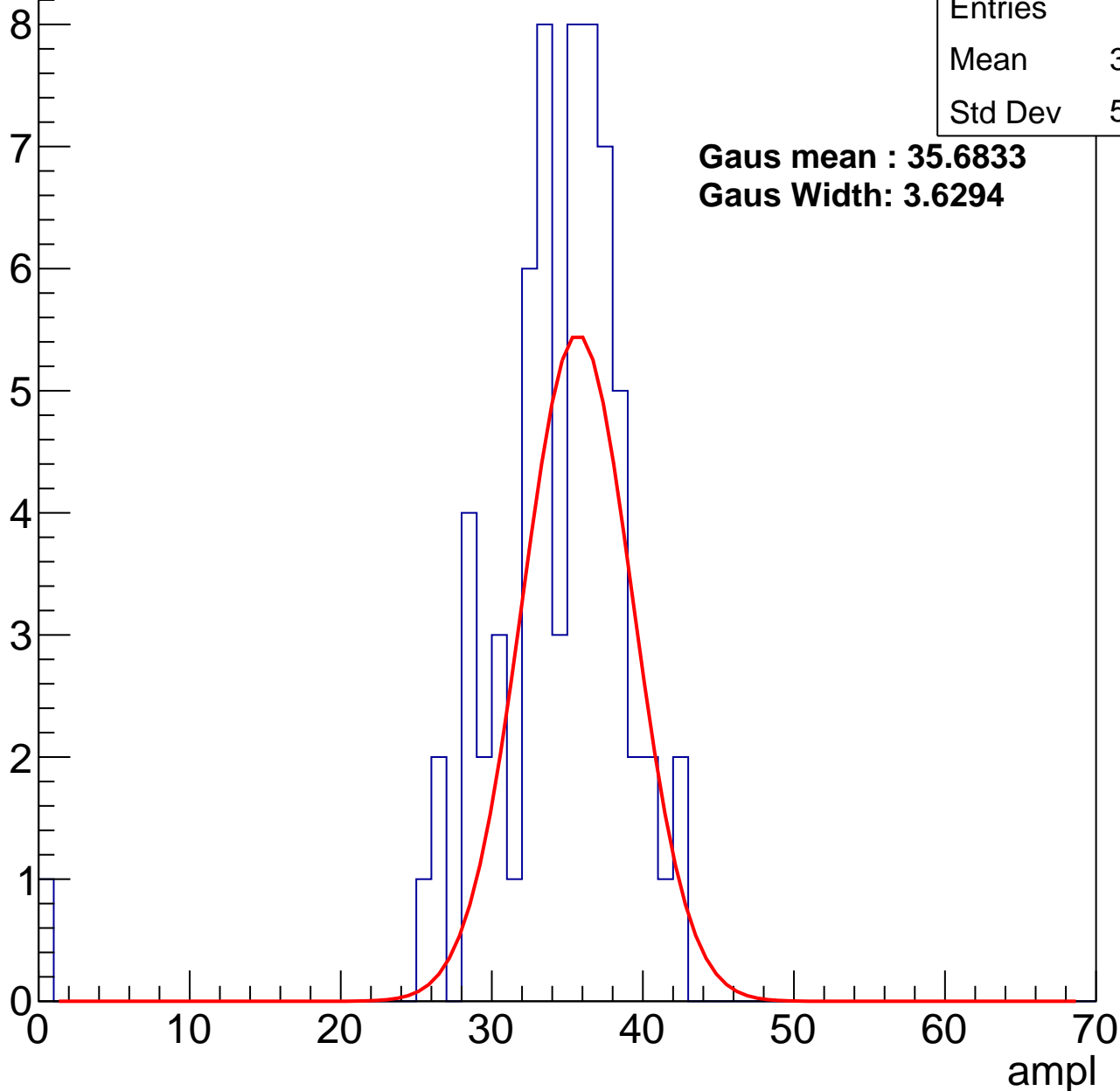
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	33.73
Std Dev	5.674

**Gaus mean : 35.6833**

**Gaus Width: 3.6294**



# B1L103S, U1-ch22, adc2

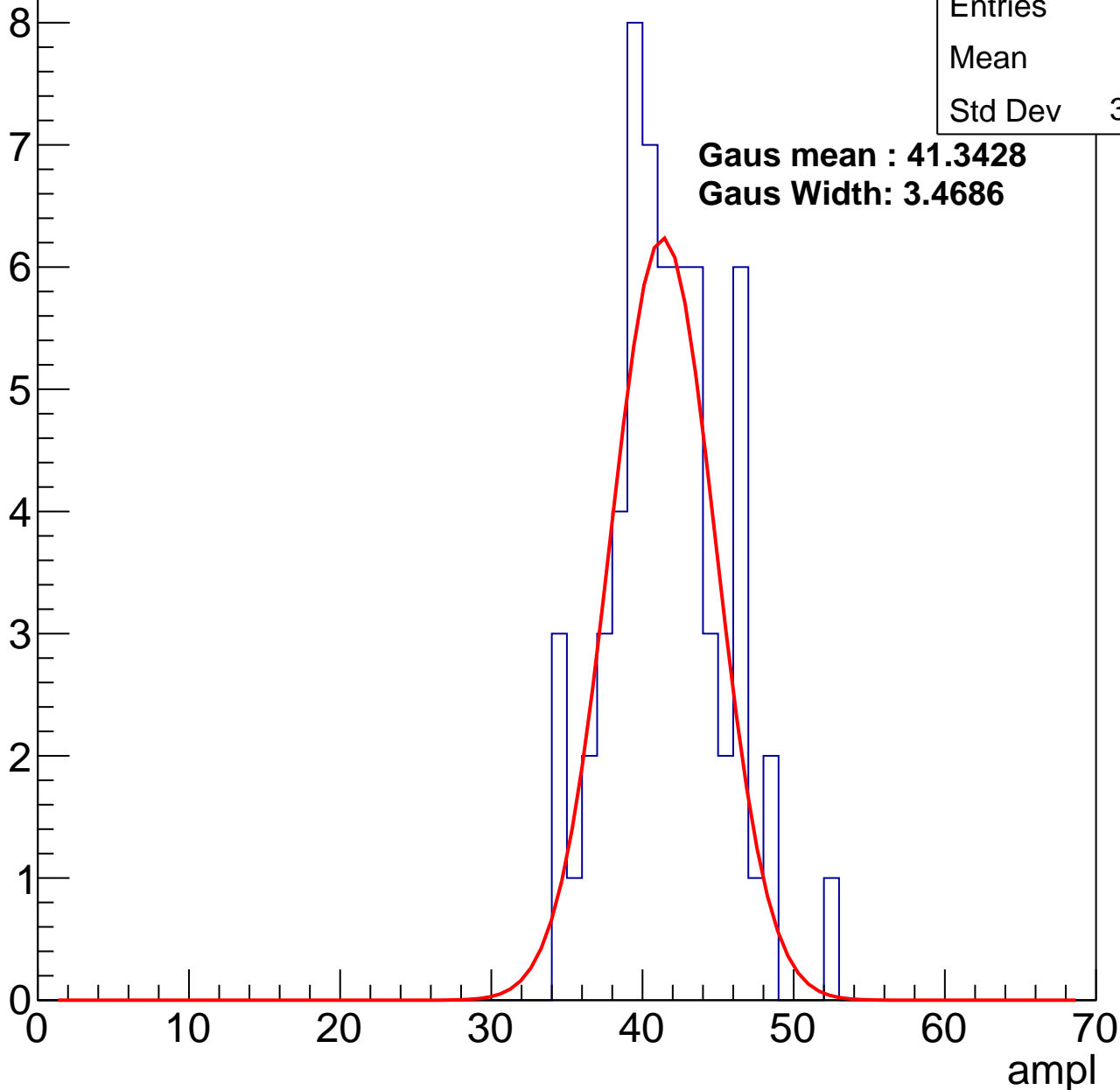
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	41.2
Std Dev	3.728

**Gaus mean : 41.3428**

**Gaus Width: 3.4686**

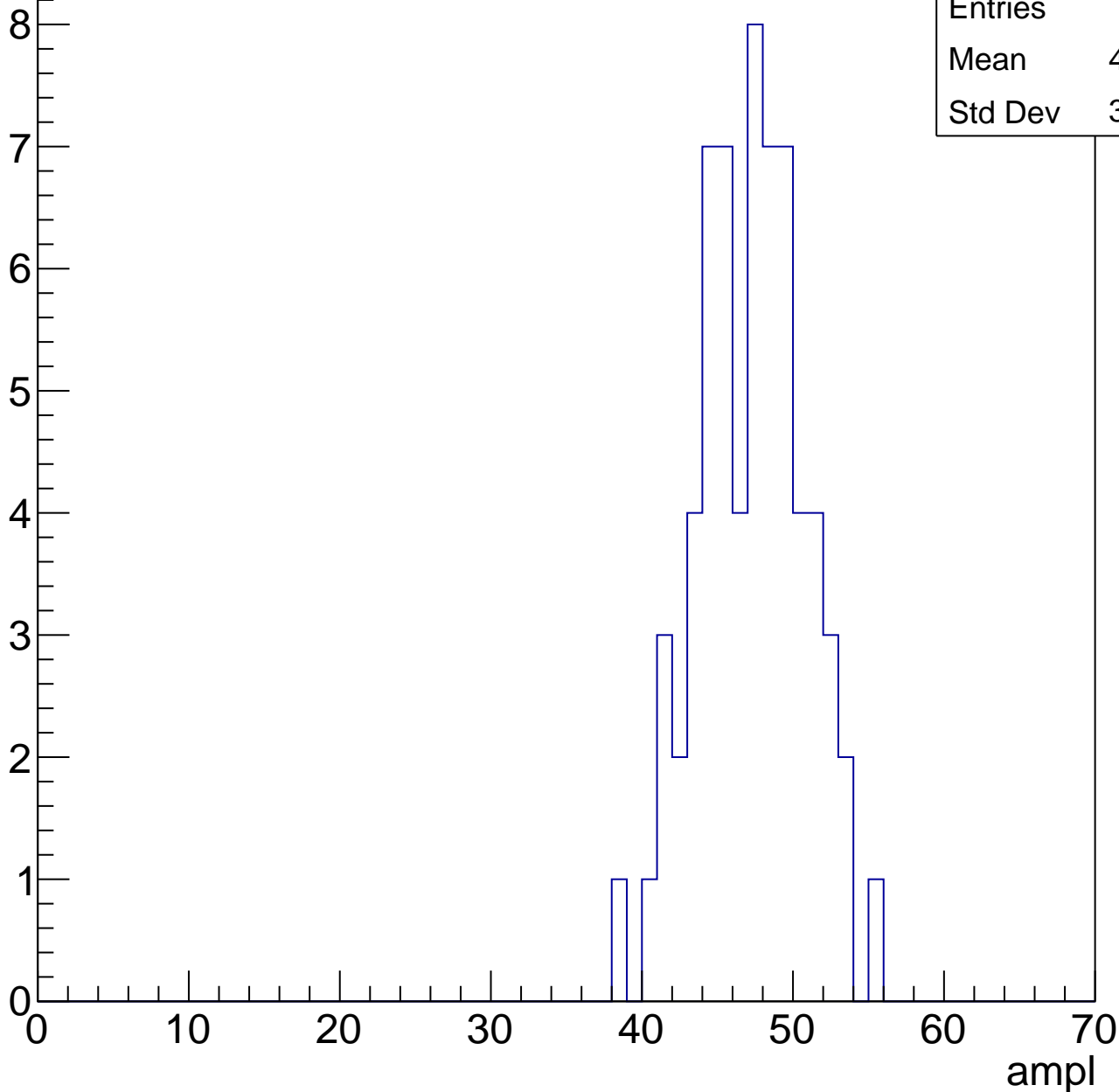


# B1L103S, U1-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	46.77
Std Dev	3.485

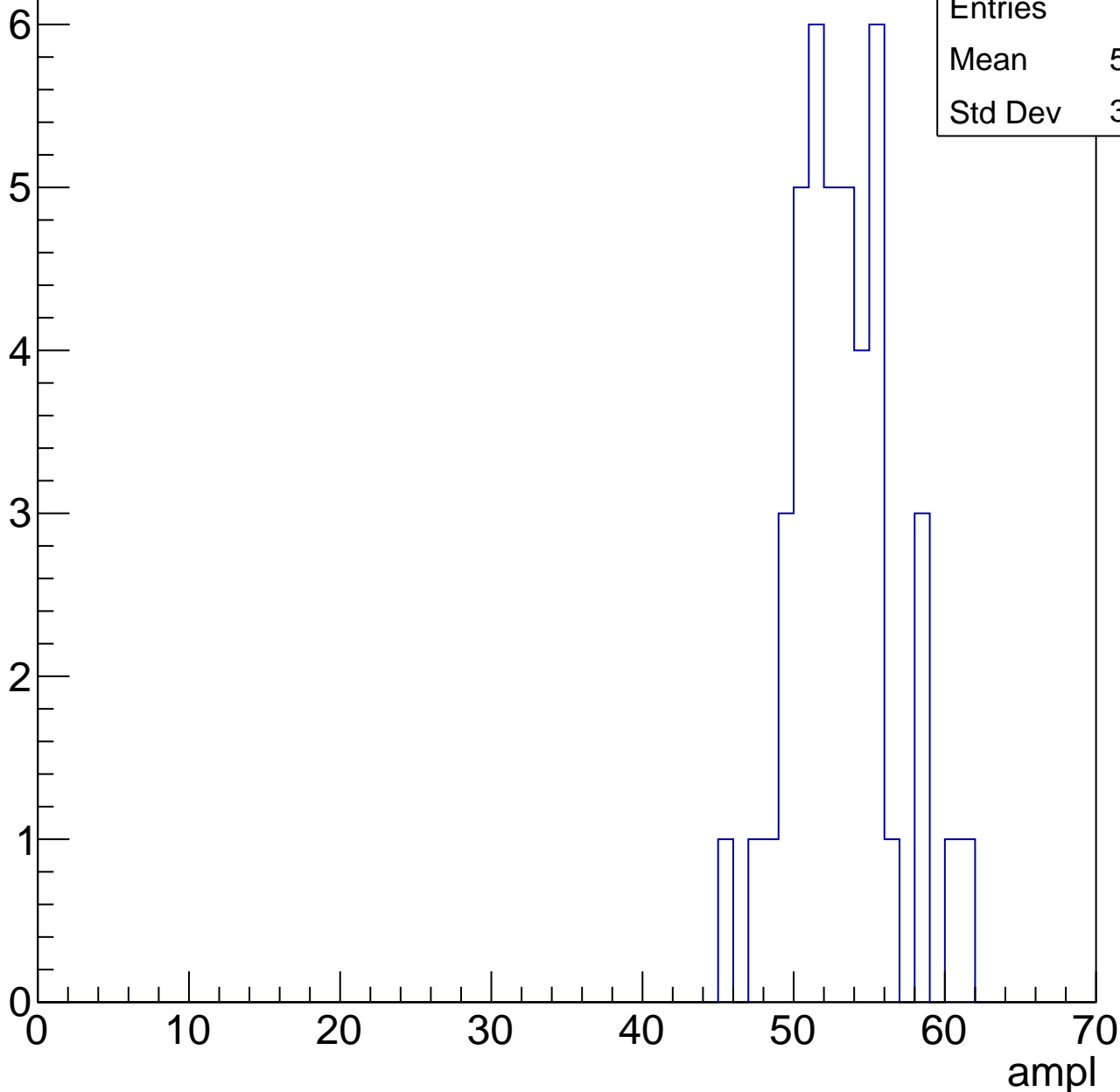


# B1L103S, U1-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

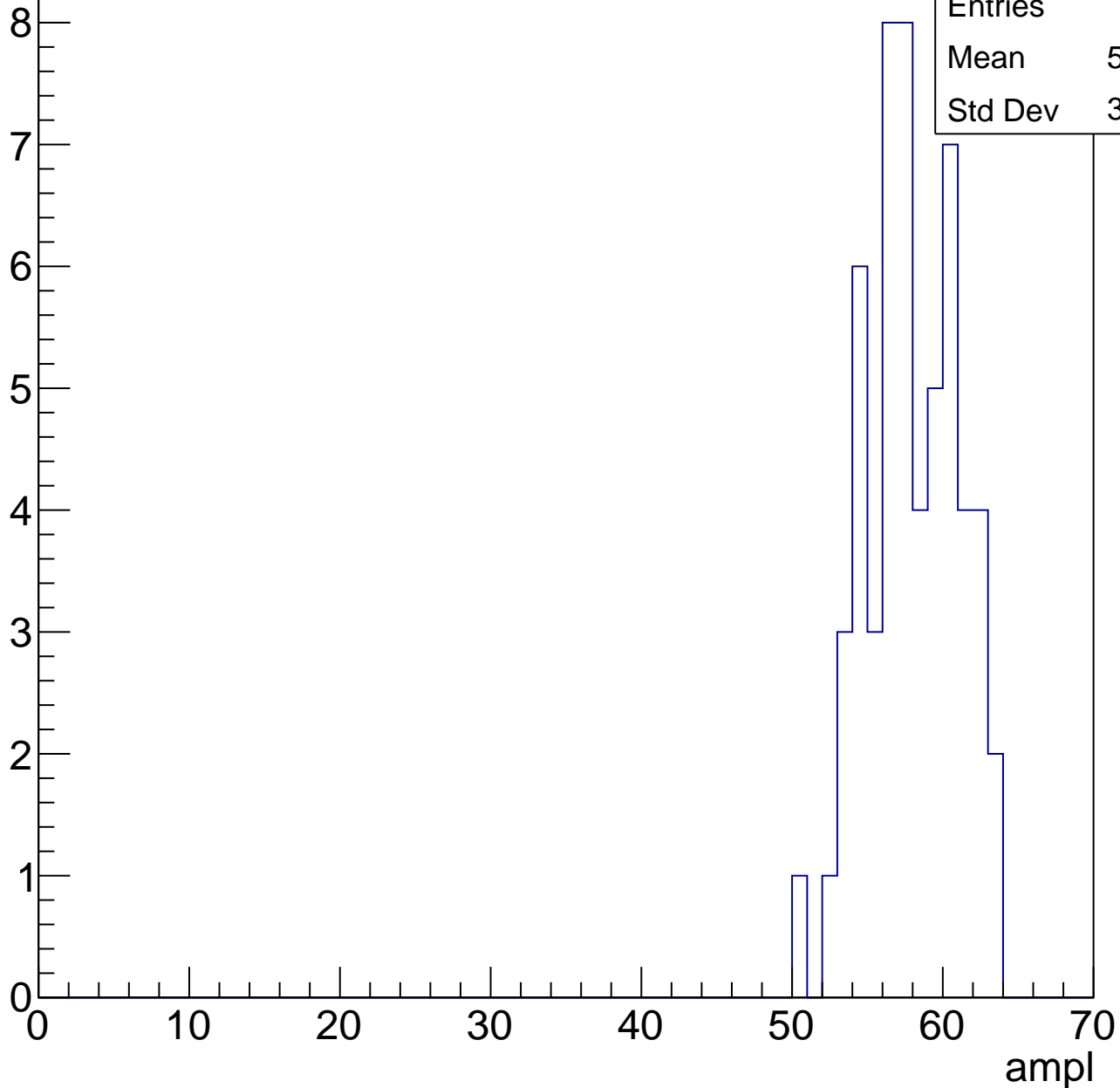
Entries	43
Mean	52.67
Std Dev	3.297



# B1L103S, U1-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

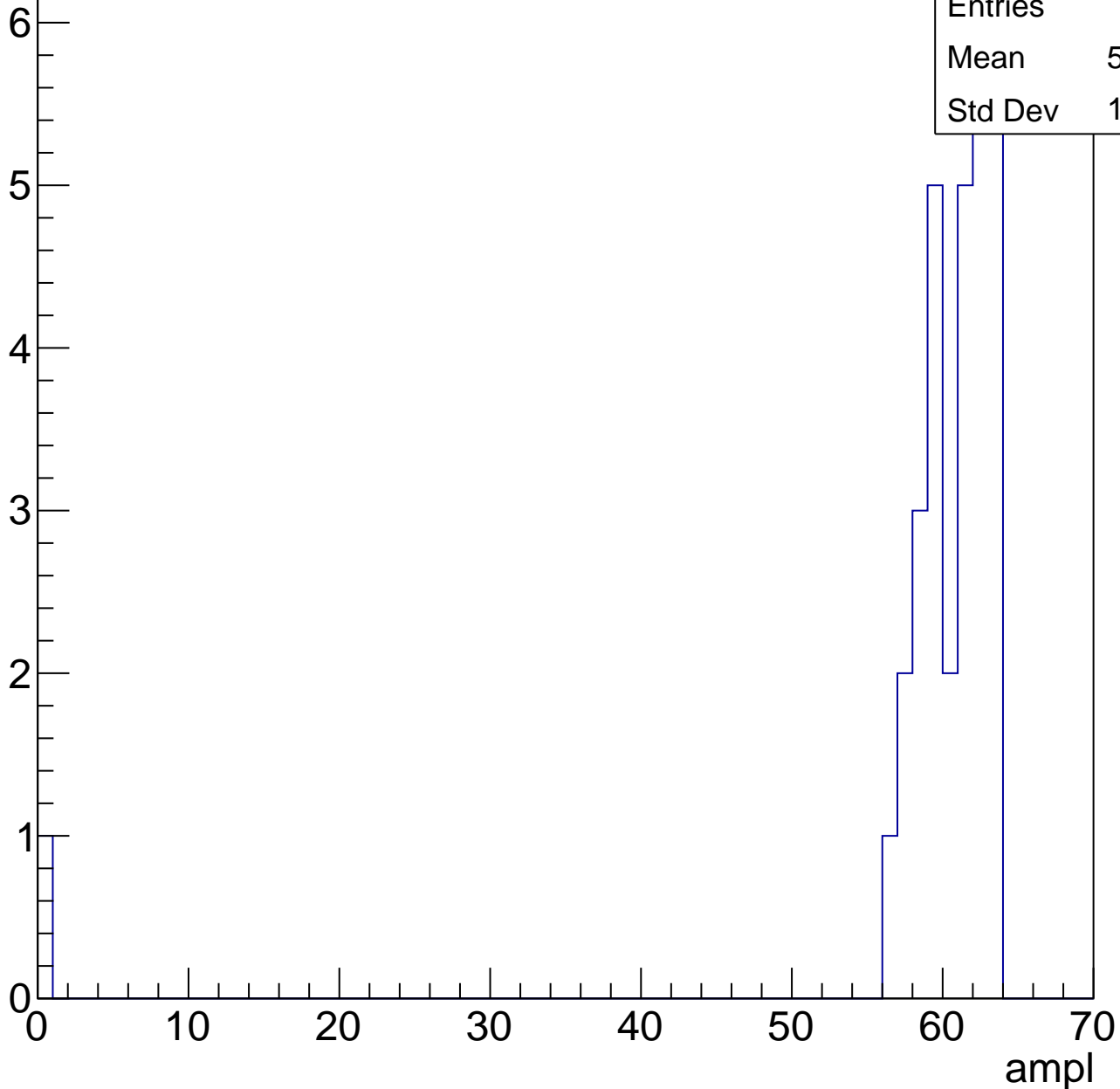


# B1L103S, U1-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	31
Mean	58.52
Std Dev	10.87





# B1L103S, U1-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch23, adc0

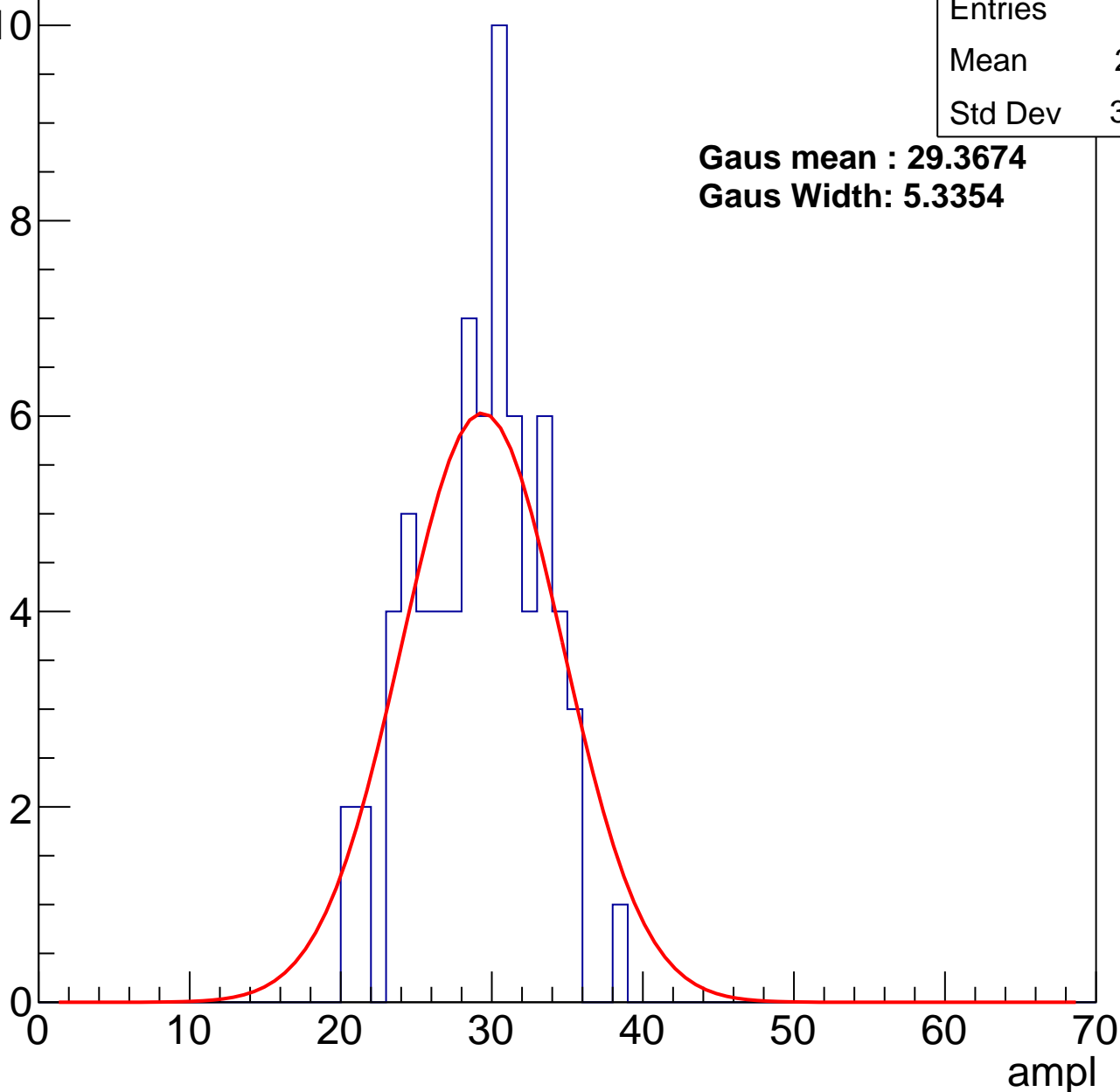
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	28.71
Std Dev	3.963

**Gaus mean : 29.3674**

**Gaus Width: 5.3354**



# B1L103S, U1-ch23, adc1

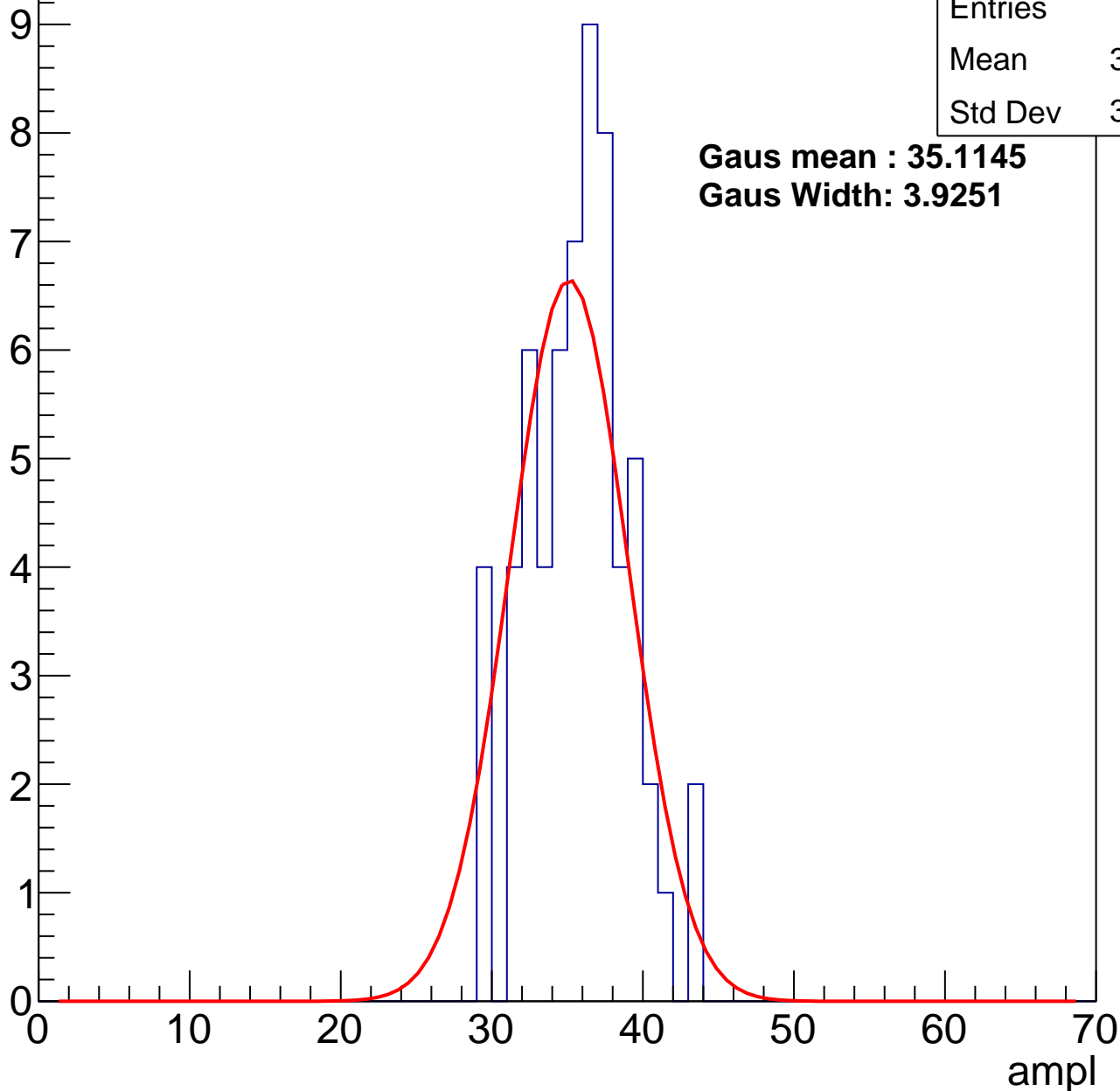
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	35.27
Std Dev	3.239

**Gaus mean : 35.1145**

**Gaus Width: 3.9251**



# B1L103S, U1-ch23, adc2

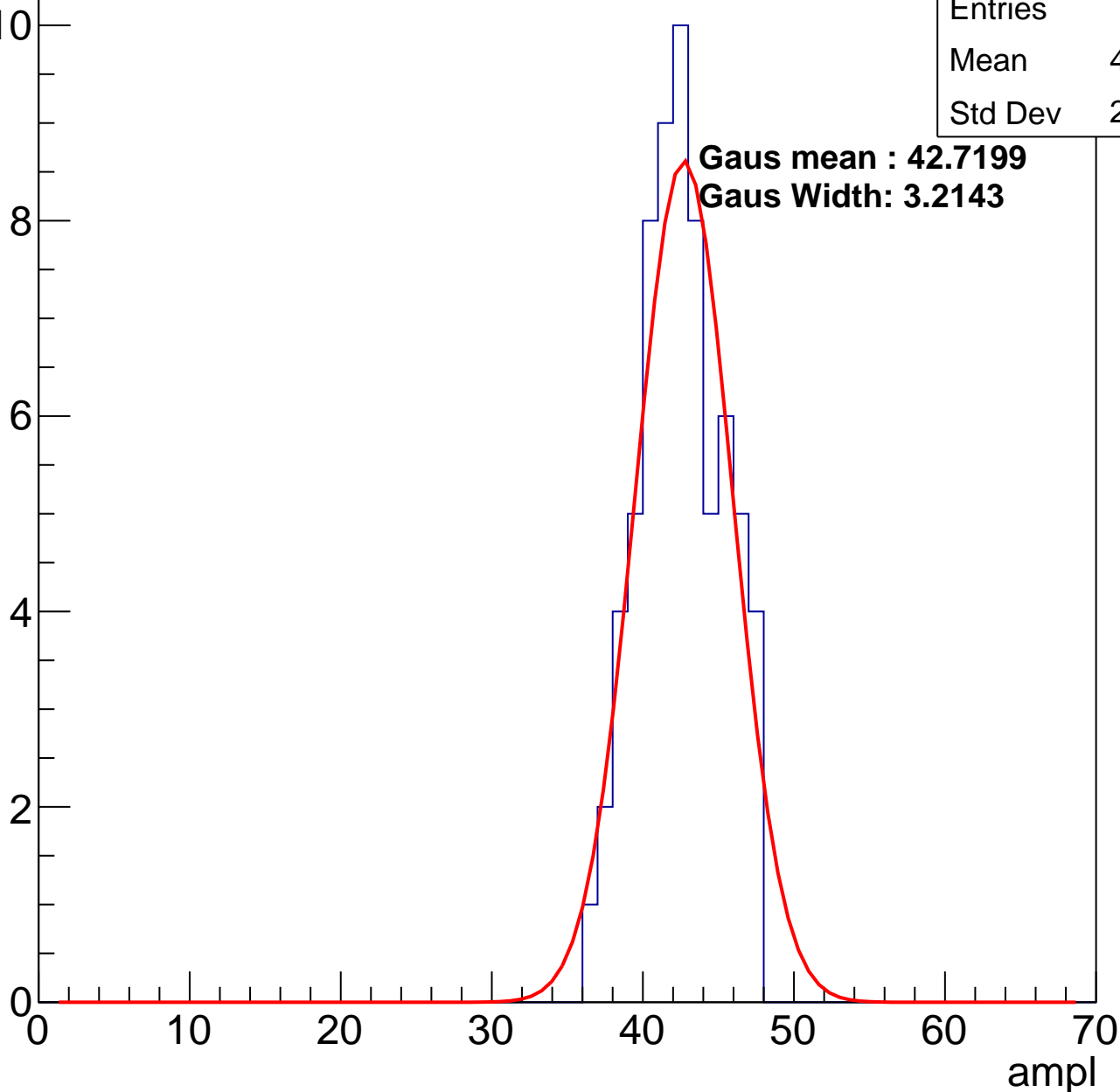
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	42.06
Std Dev	2.726

**Gaus mean : 42.7199**

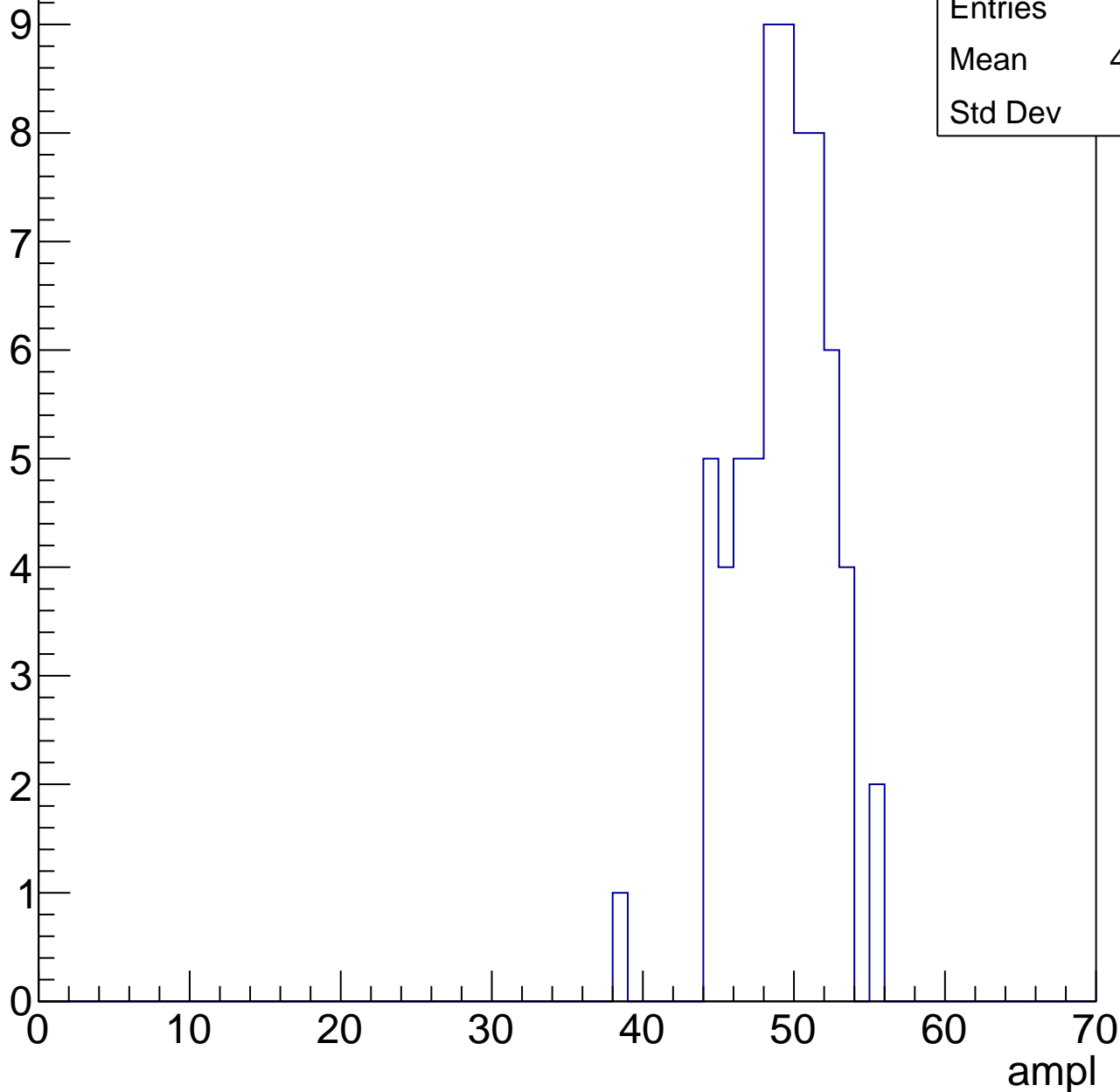
**Gaus Width: 3.2143**



# B1L103S, U1-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

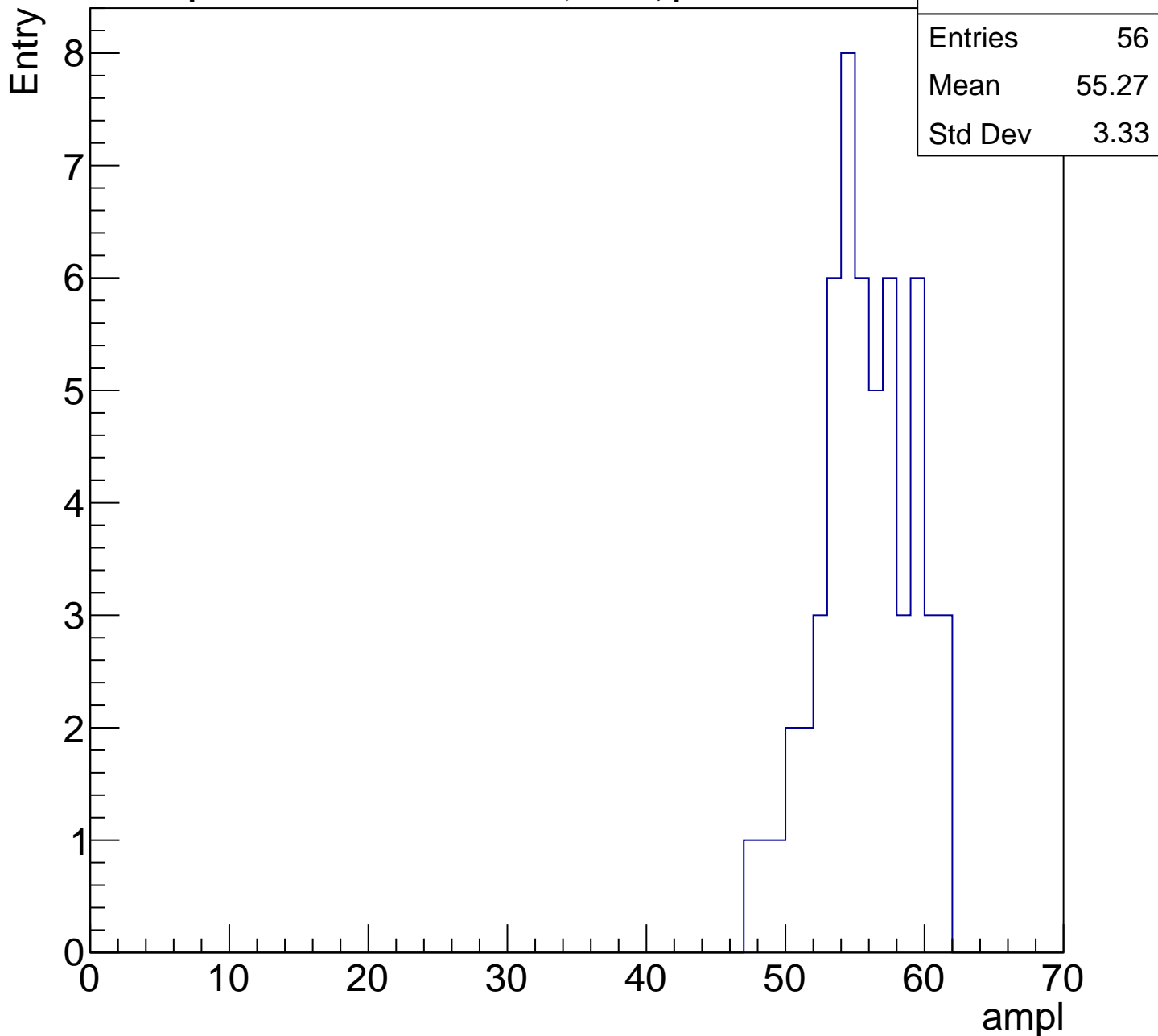
Entry



Entries	66
Mean	48.76
Std Dev	3.04

# B1L103S, U1-ch23, adc4

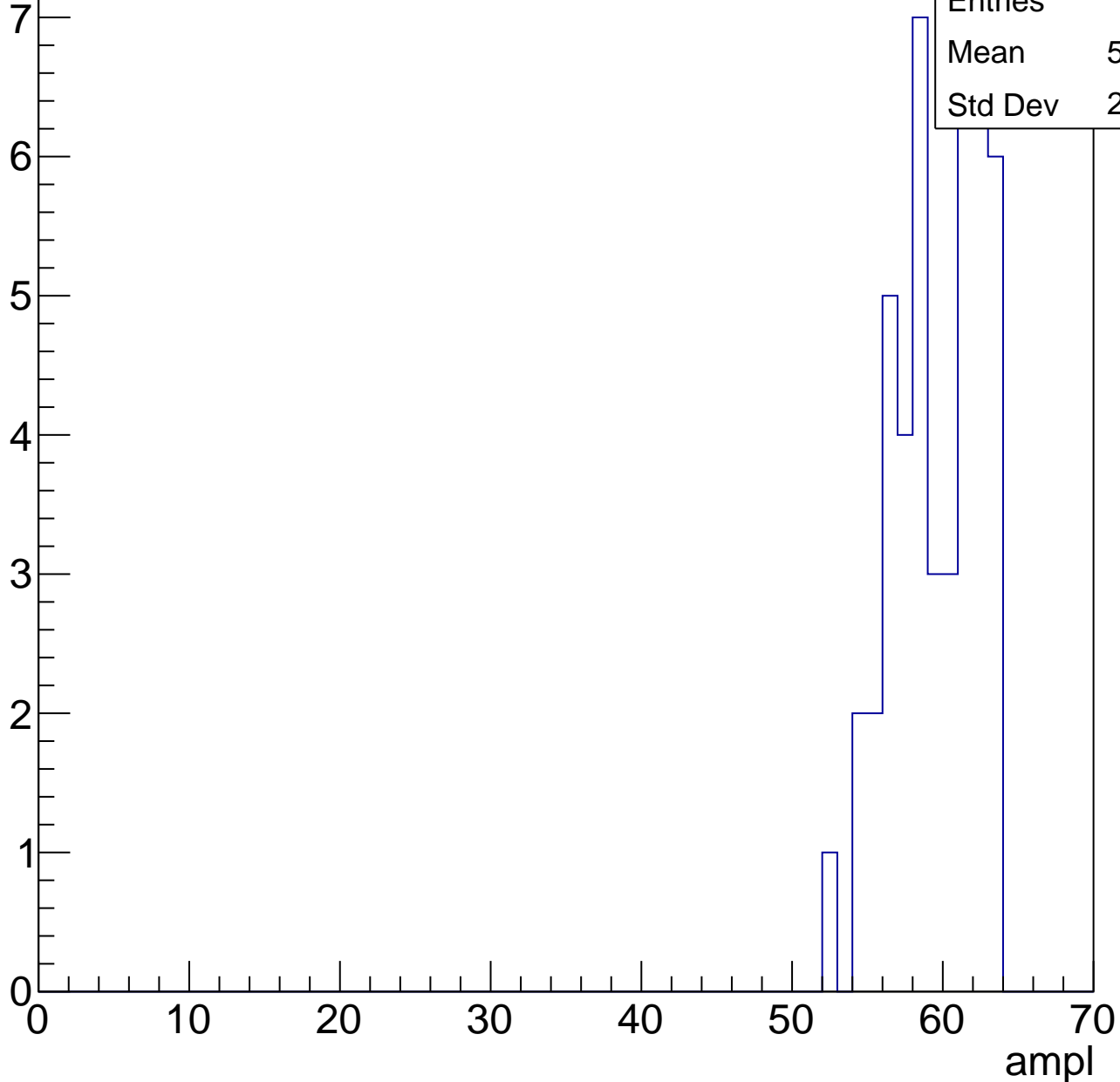
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U1-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

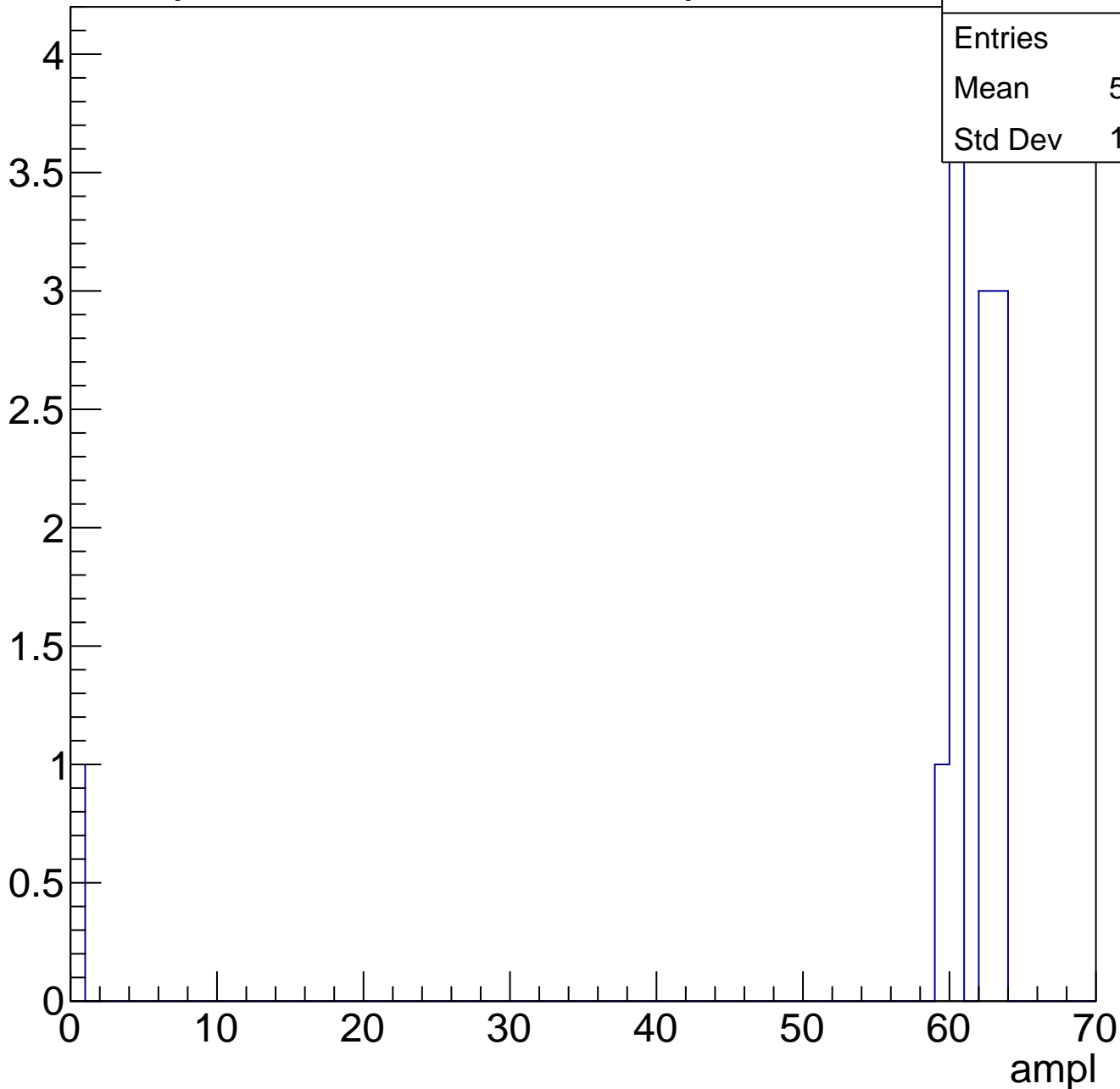


Entries	47
Mean	59.15
Std Dev	2.873

# B1L103S, U1-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U1-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch24, adc0

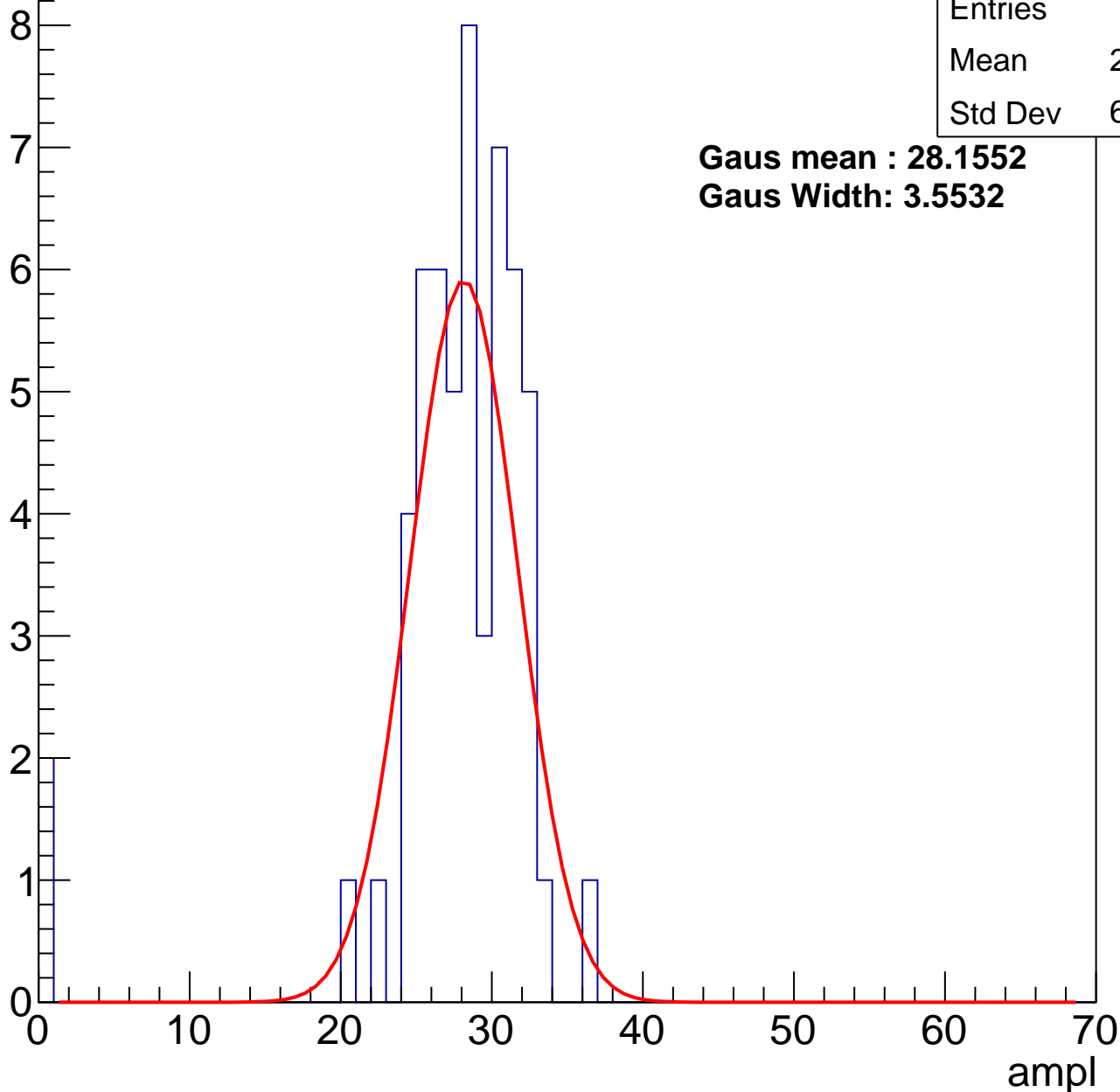
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	27.05
Std Dev	6.004

**Gaus mean : 28.1552**

**Gaus Width: 3.5532**



# B1L103S, U1-ch24, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	65
Mean	34.57
Std Dev	3.258

**Gaus mean : 35.2100**

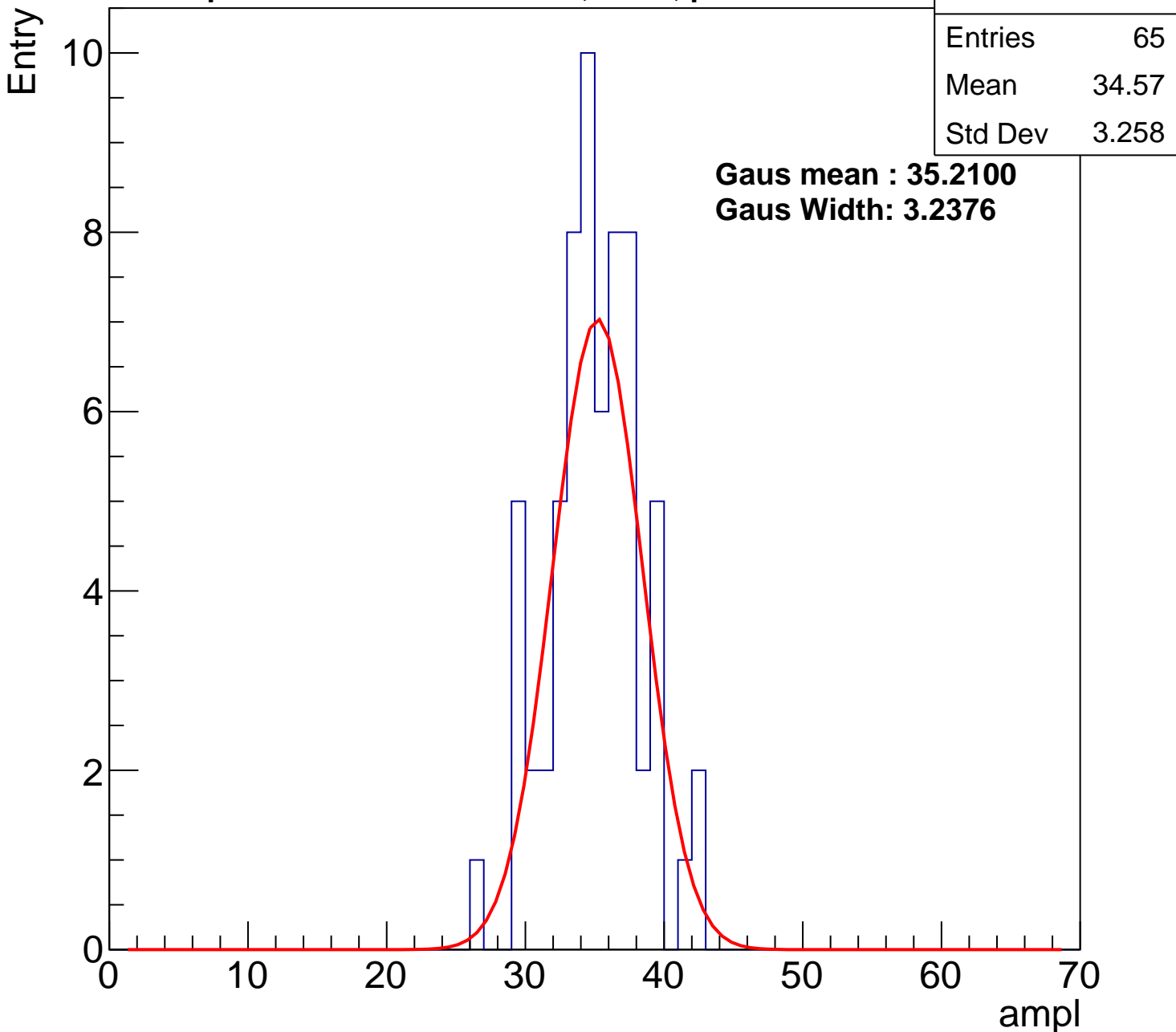
**Gaus Width: 3.2376**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U1-ch24, adc2

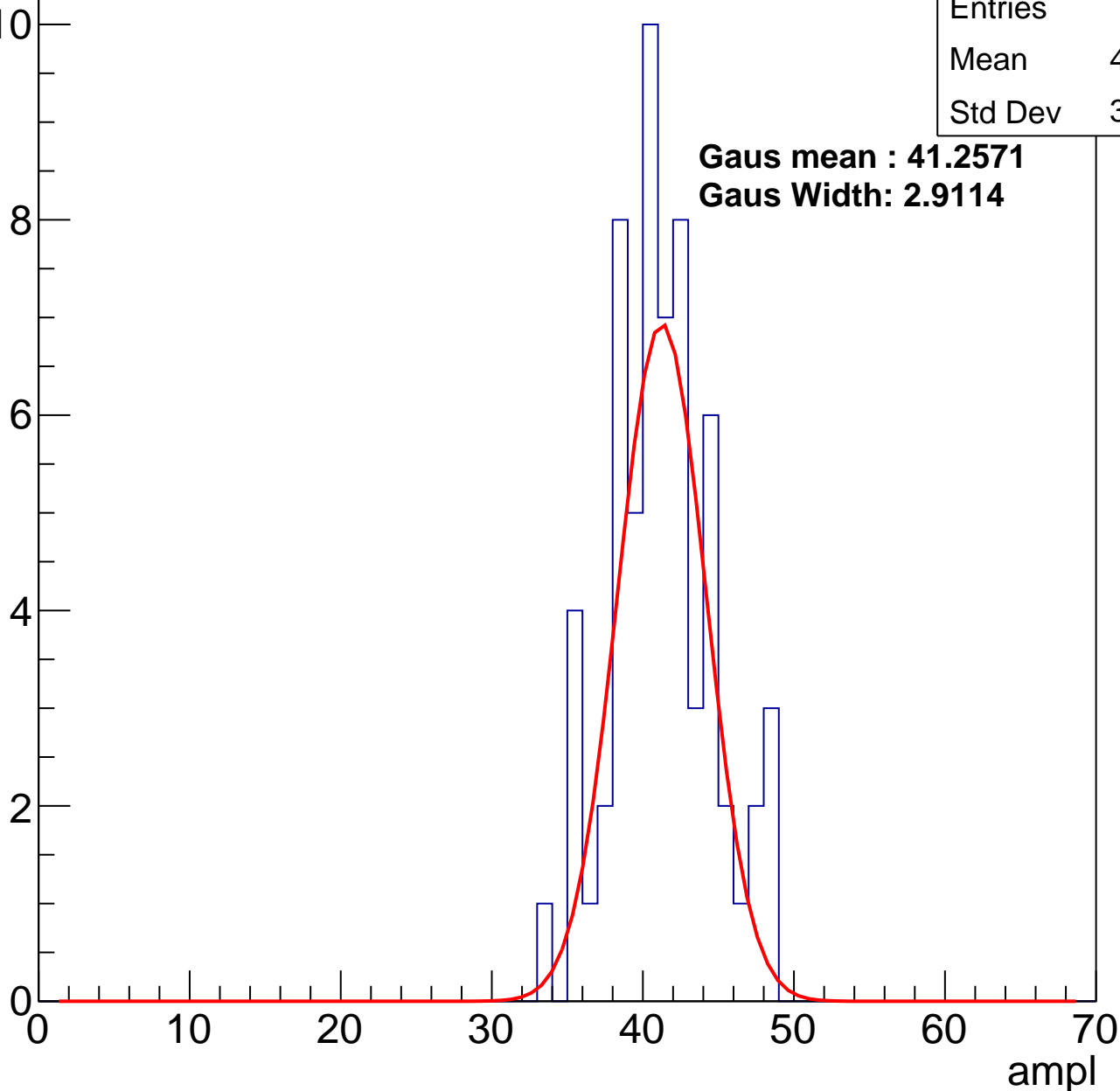
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	40.83
Std Dev	3.369

**Gaus mean : 41.2571**

**Gaus Width: 2.9114**

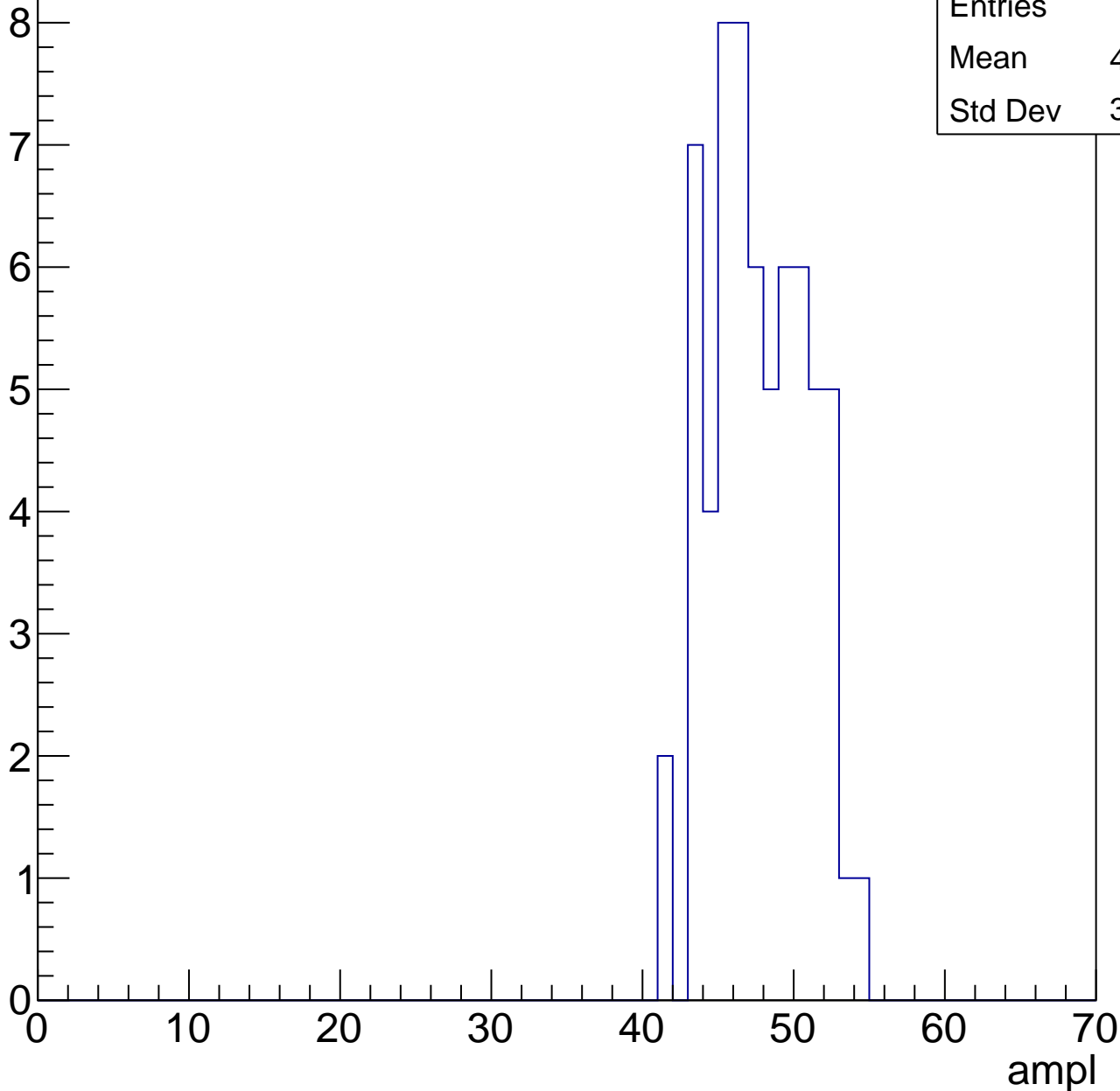


# B1L103S, U1-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	47.27
Std Dev	3.134

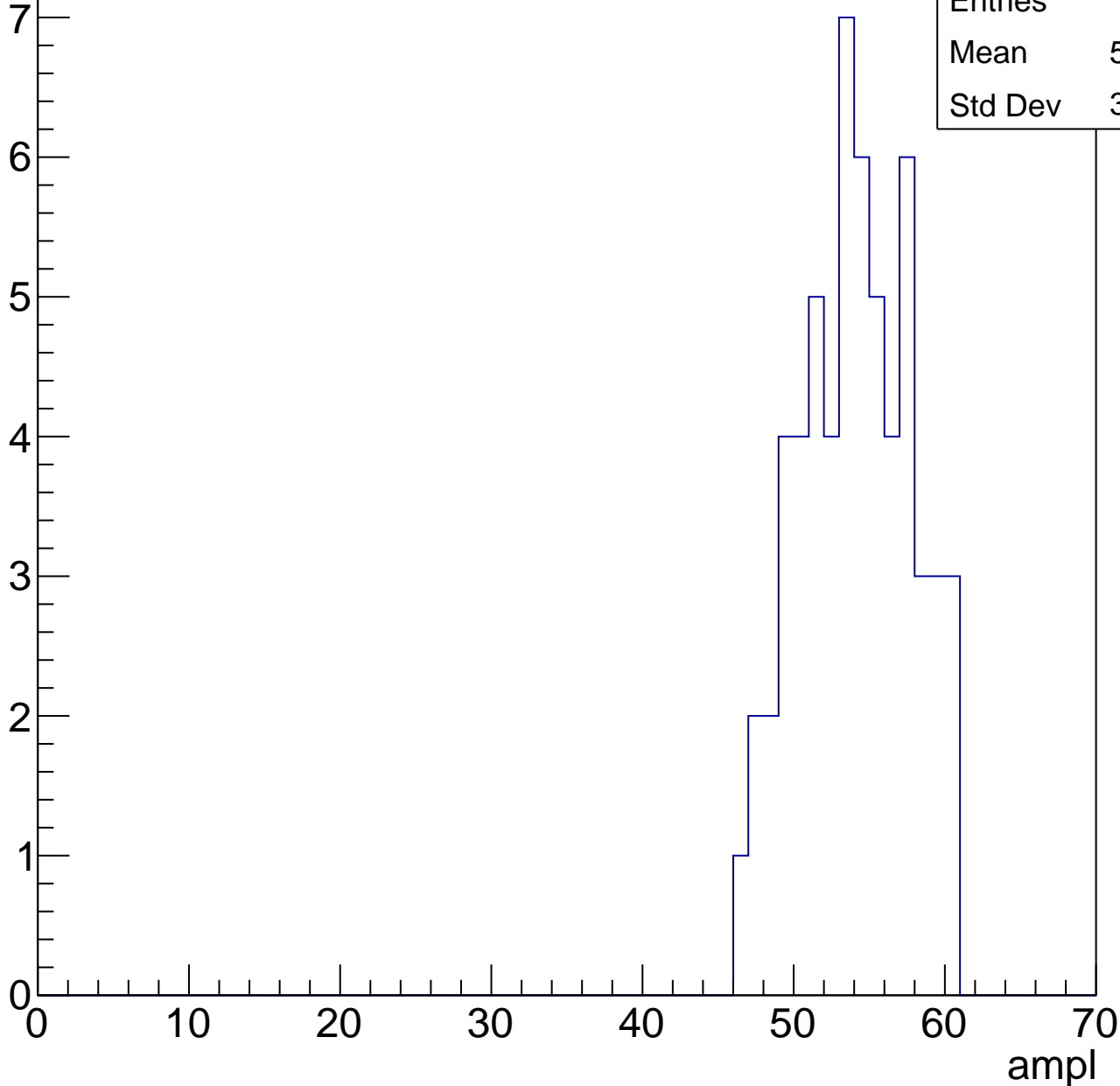


# B1L103S, U1-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

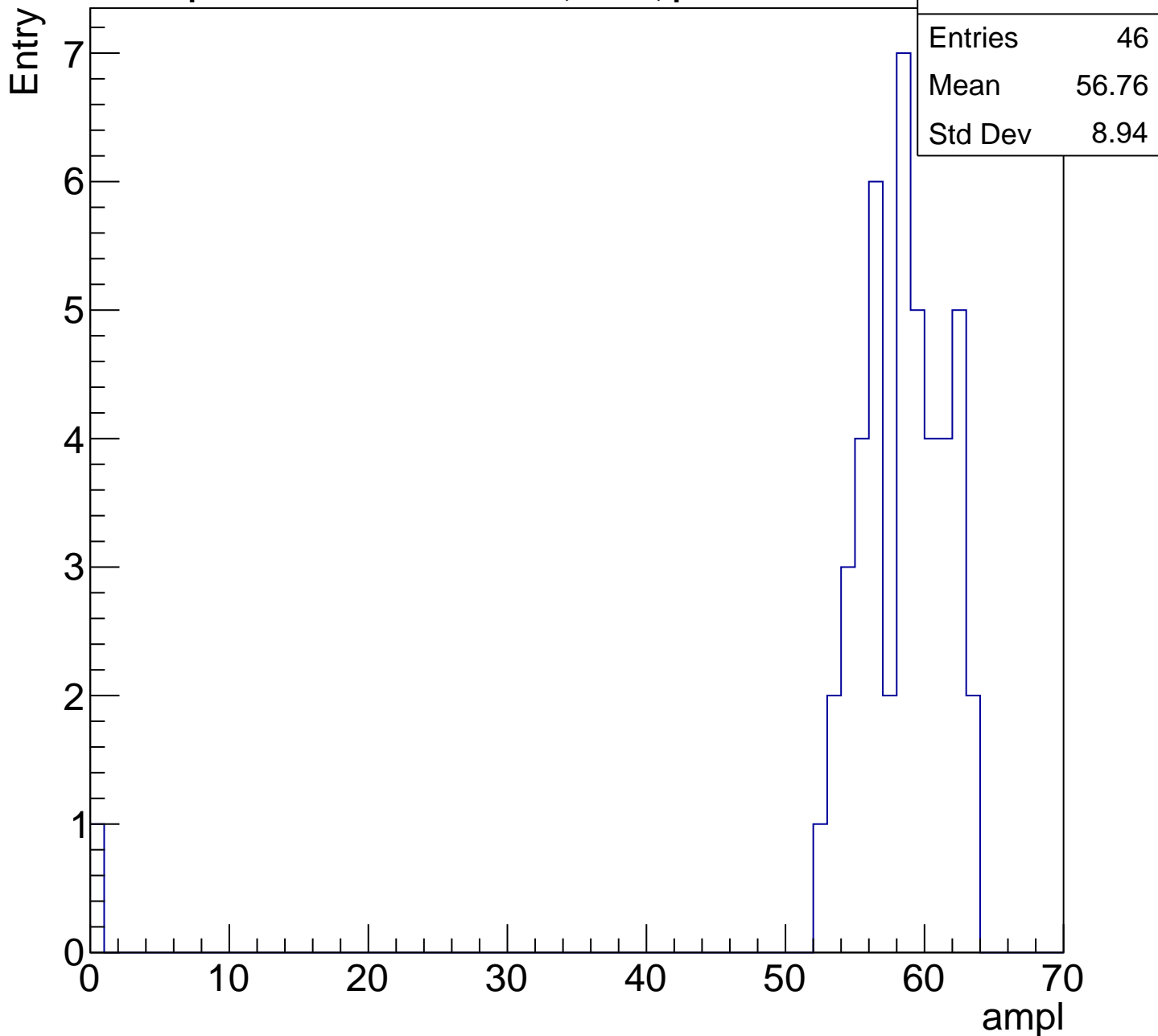
Entry

Entries	59
Mean	53.59
Std Dev	3.594



# B1L103S, U1-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

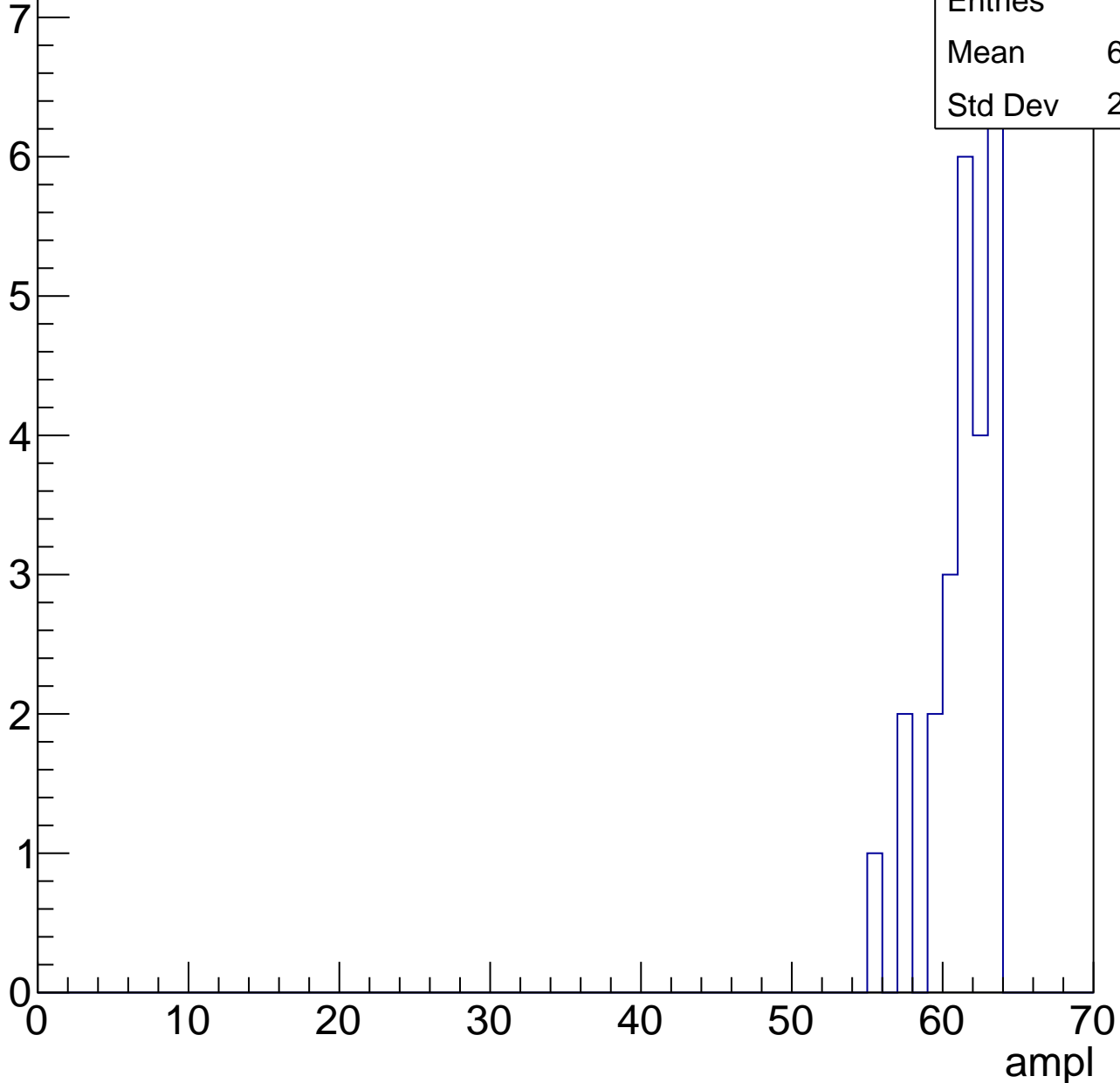


# B1L103S, U1-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	25
Mean	60.88
Std Dev	2.104





# B1L103S, U1-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch25, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	90
Mean	28.27
Std Dev	6.234

**Gaus mean : 29.1128**

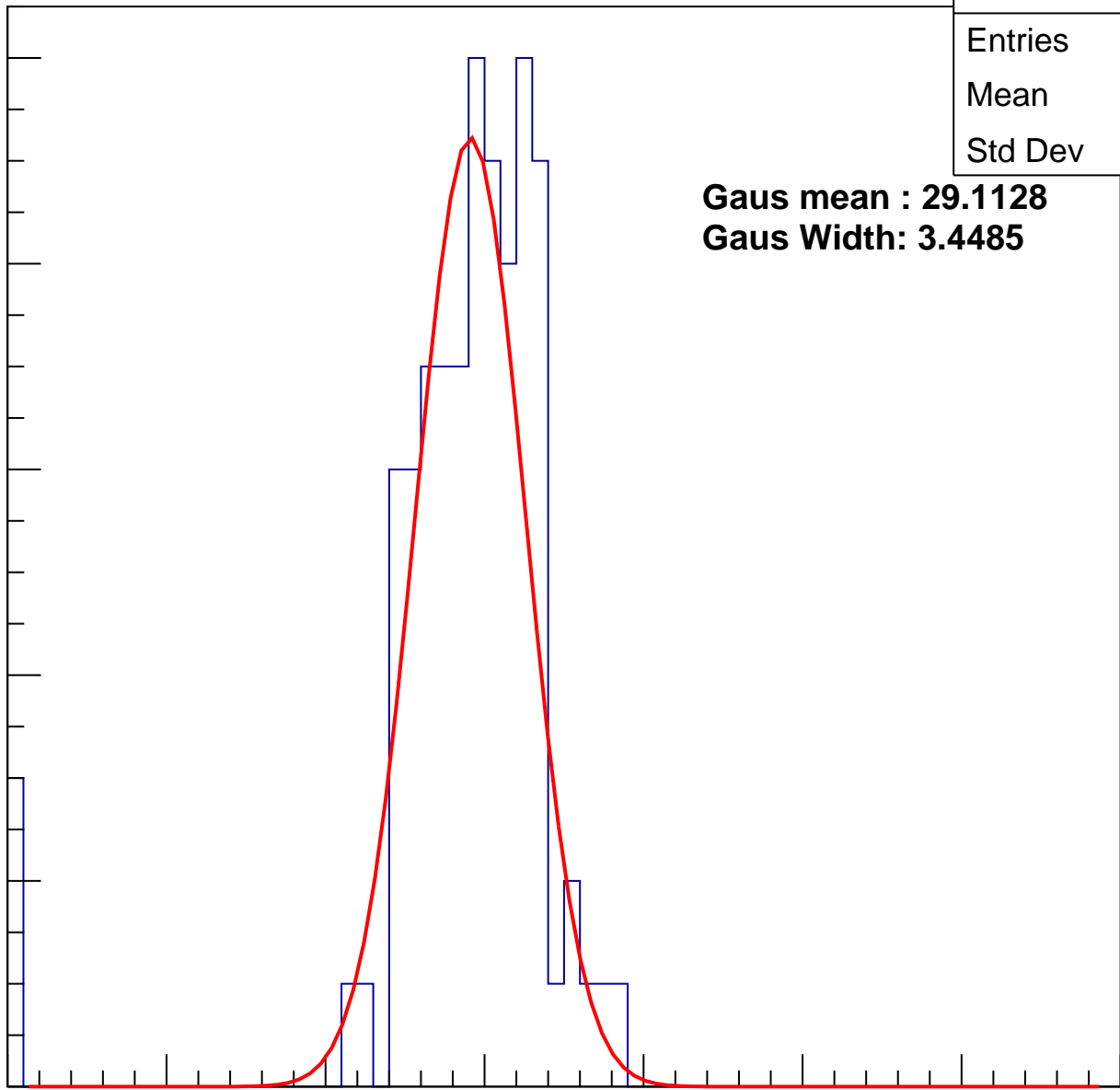
**Gaus Width: 3.4485**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U1-ch25, adc1

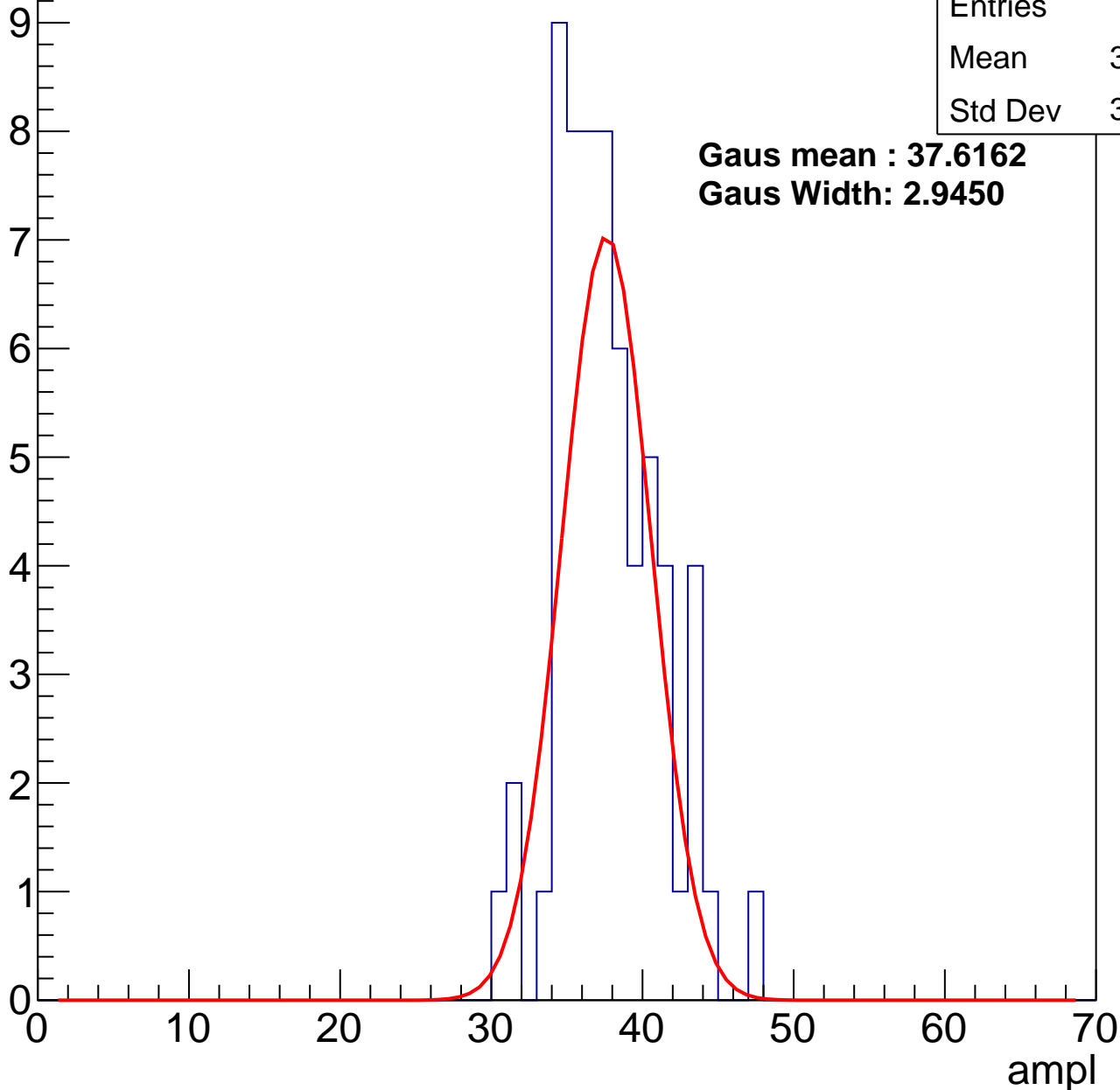
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	37.27
Std Dev	3.339

**Gaus mean : 37.6162**

**Gaus Width: 2.9450**



# B1L103S, U1-ch25, adc2

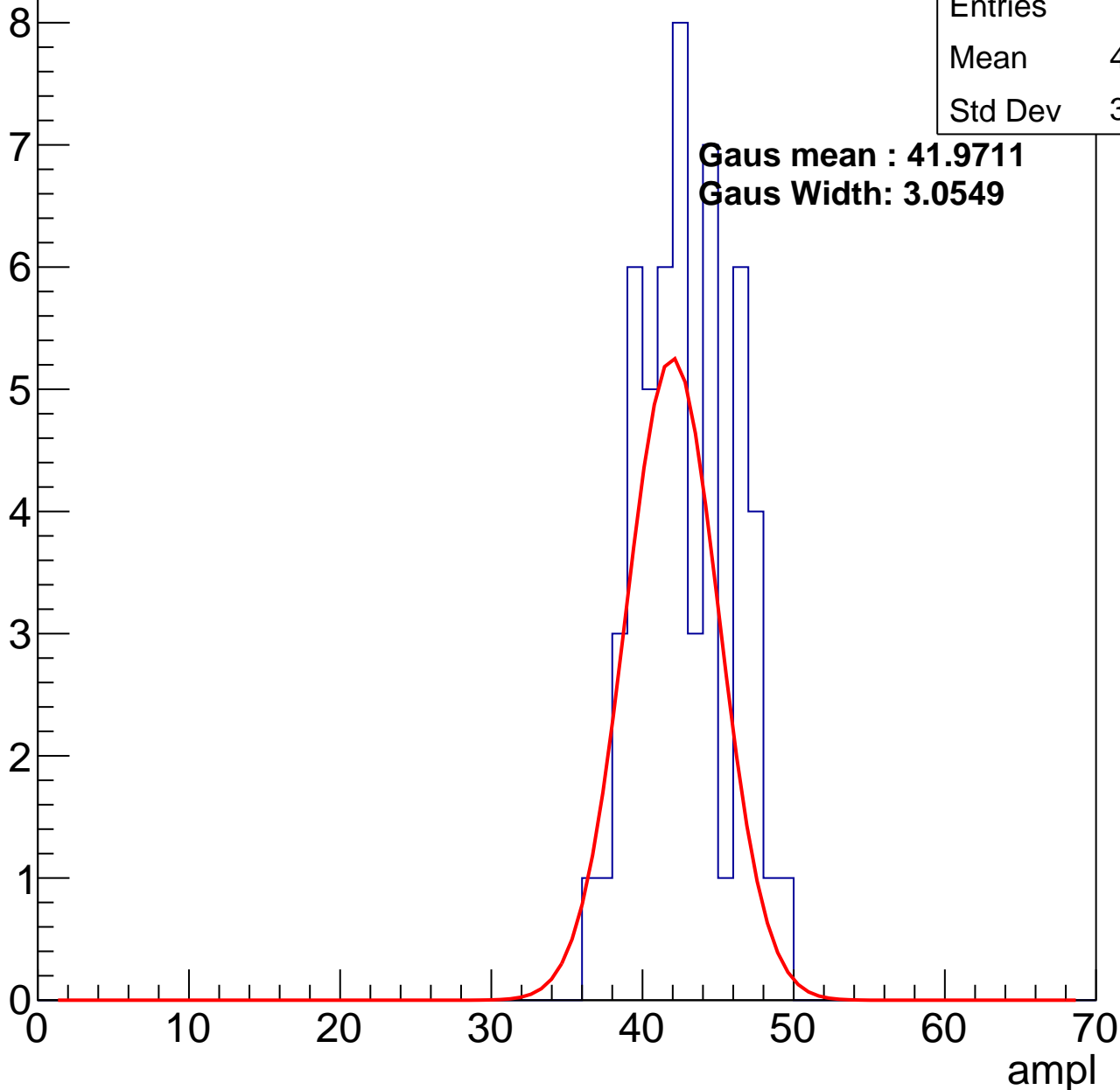
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	42.38
Std Dev	3.079

**Gaus mean : 41.9711**

**Gaus Width: 3.0549**

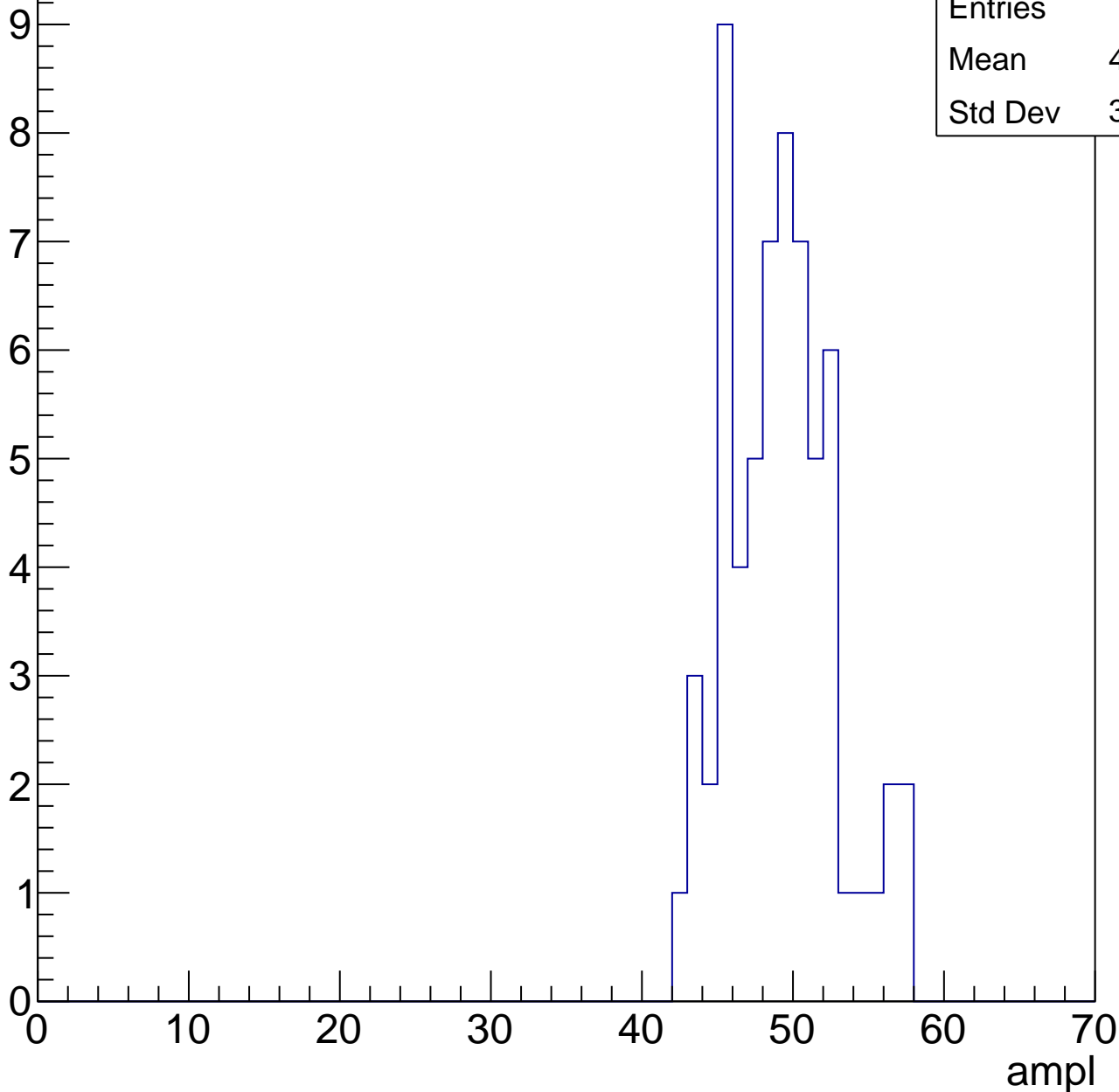


# B1L103S, U1-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

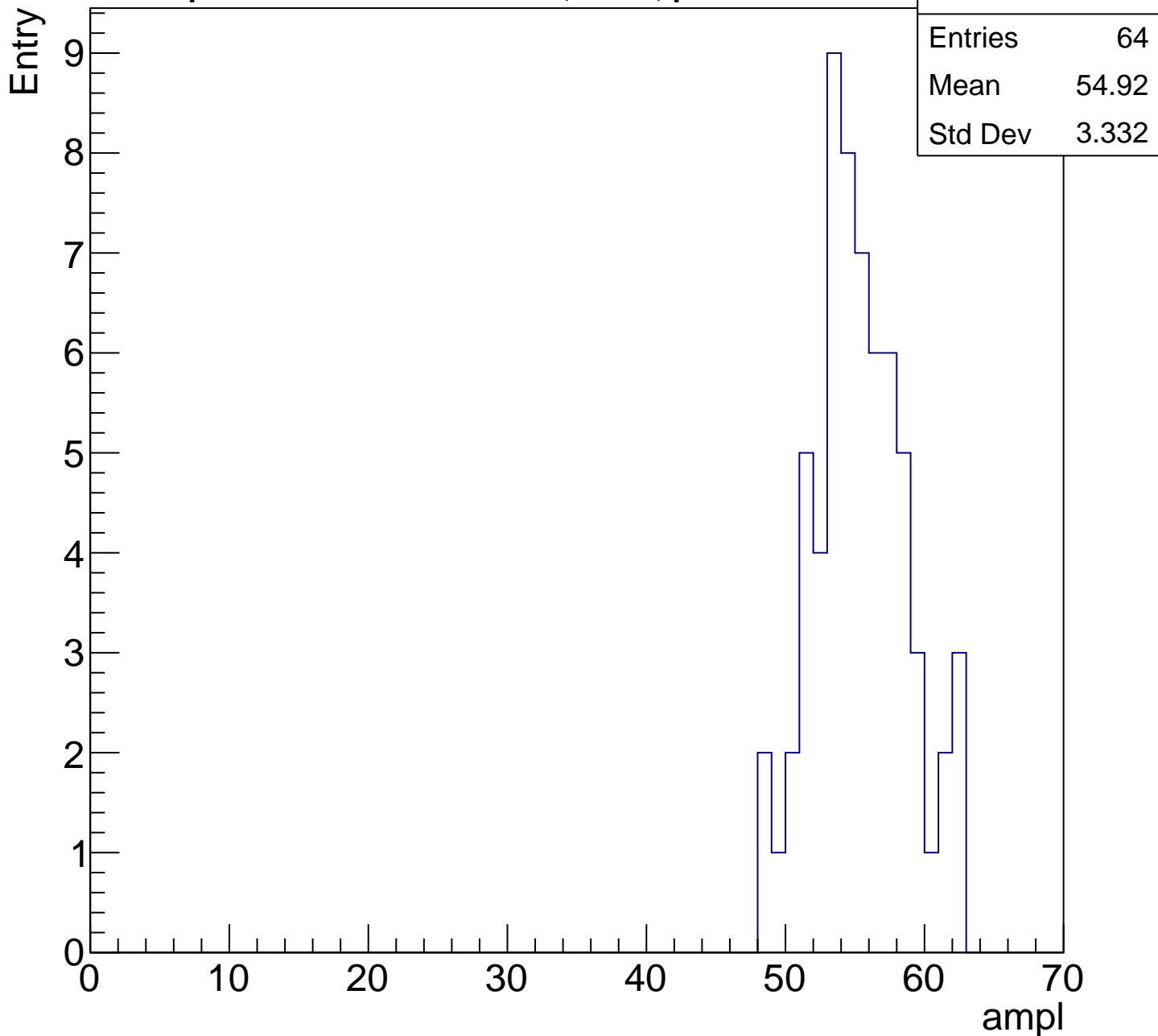
Entry

Entries	64
Mean	48.69
Std Dev	3.517



# B1L103S, U1-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U1-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

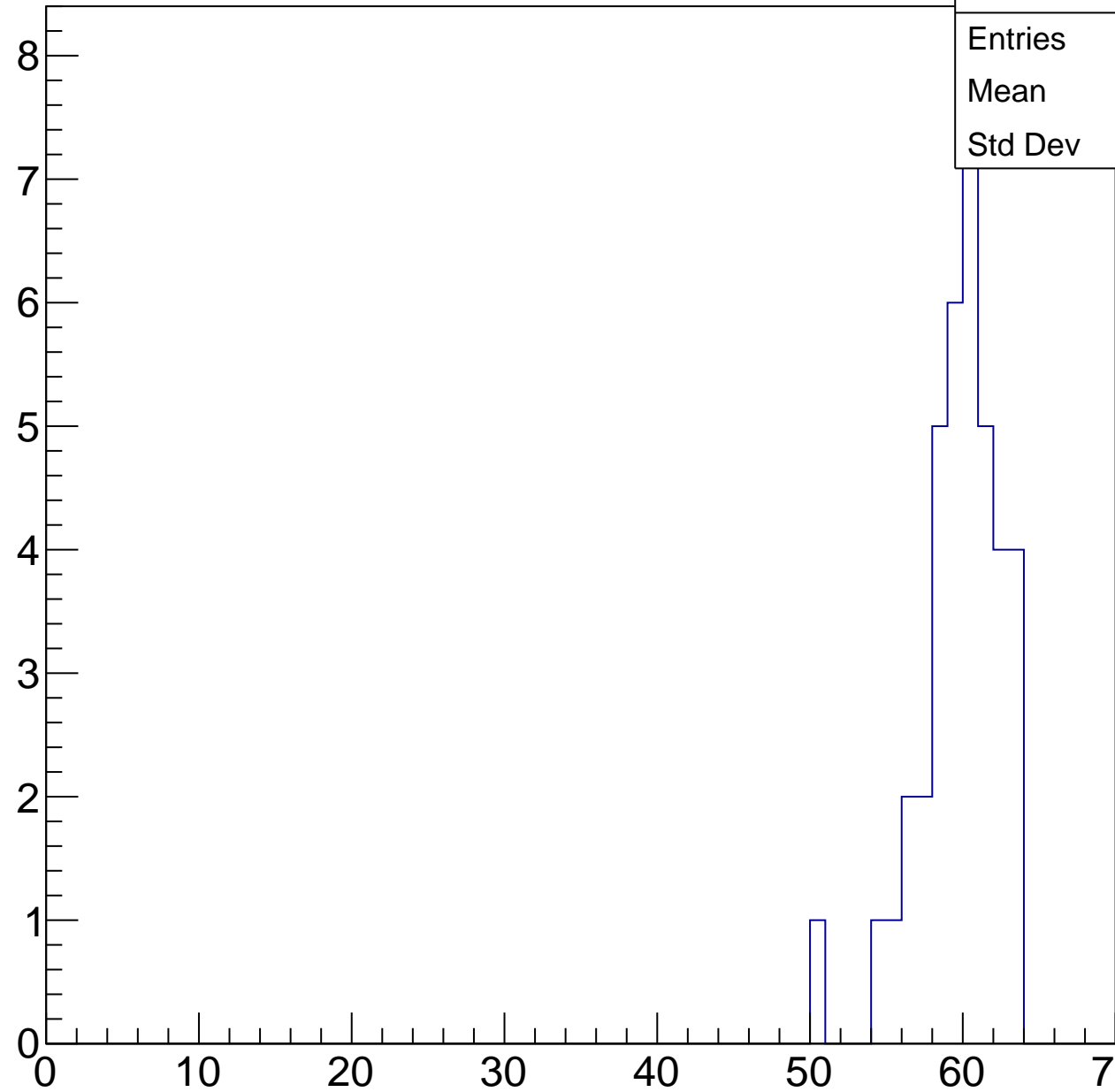
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	39
Mean	59.33
Std Dev	2.663

ampl

0 10 20 30 40 50 60 70

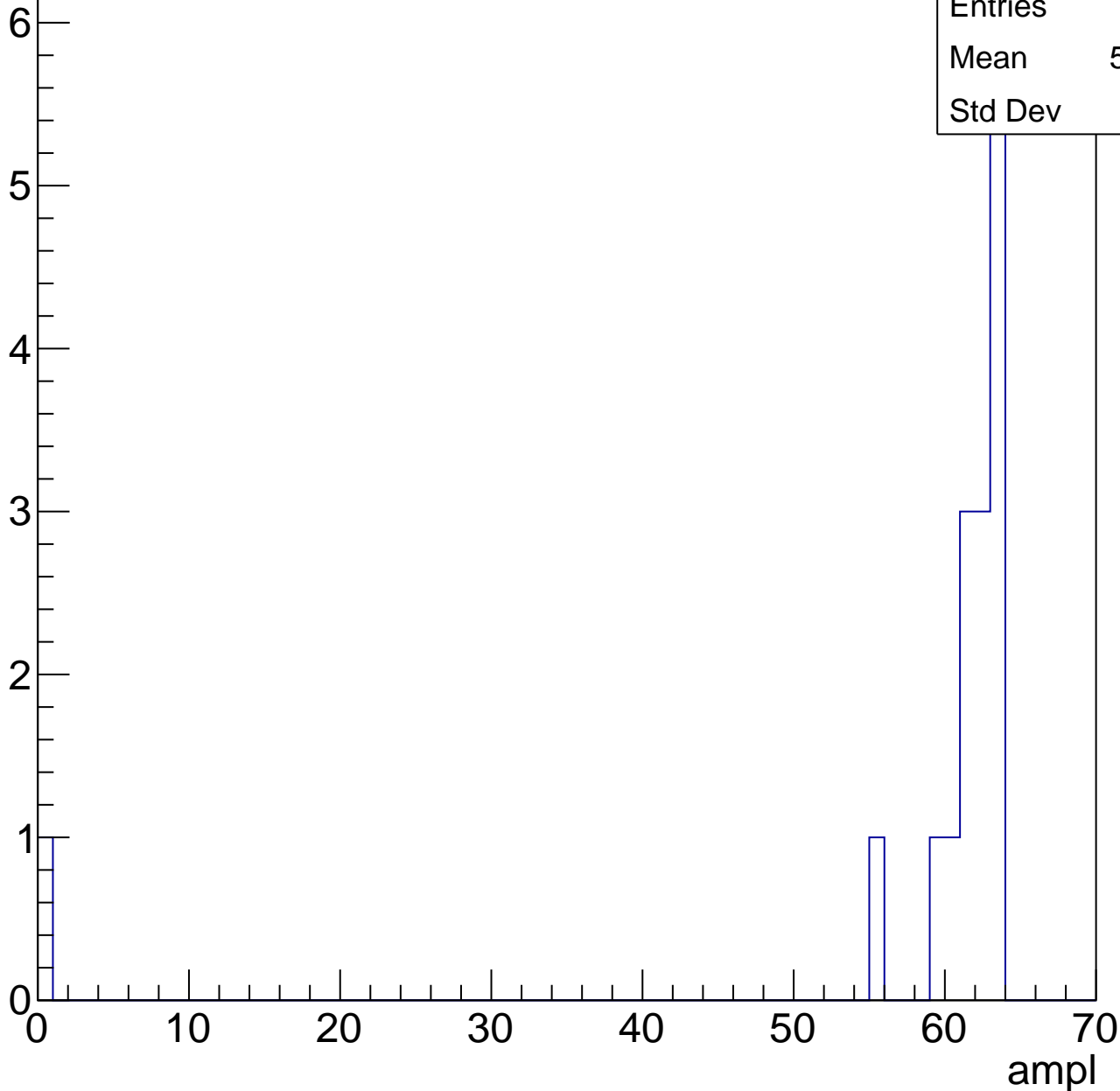


# B1L103S, U1-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	16
Mean	57.56
Std Dev	15





# B1L103S, U1-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U1-ch26, adc0

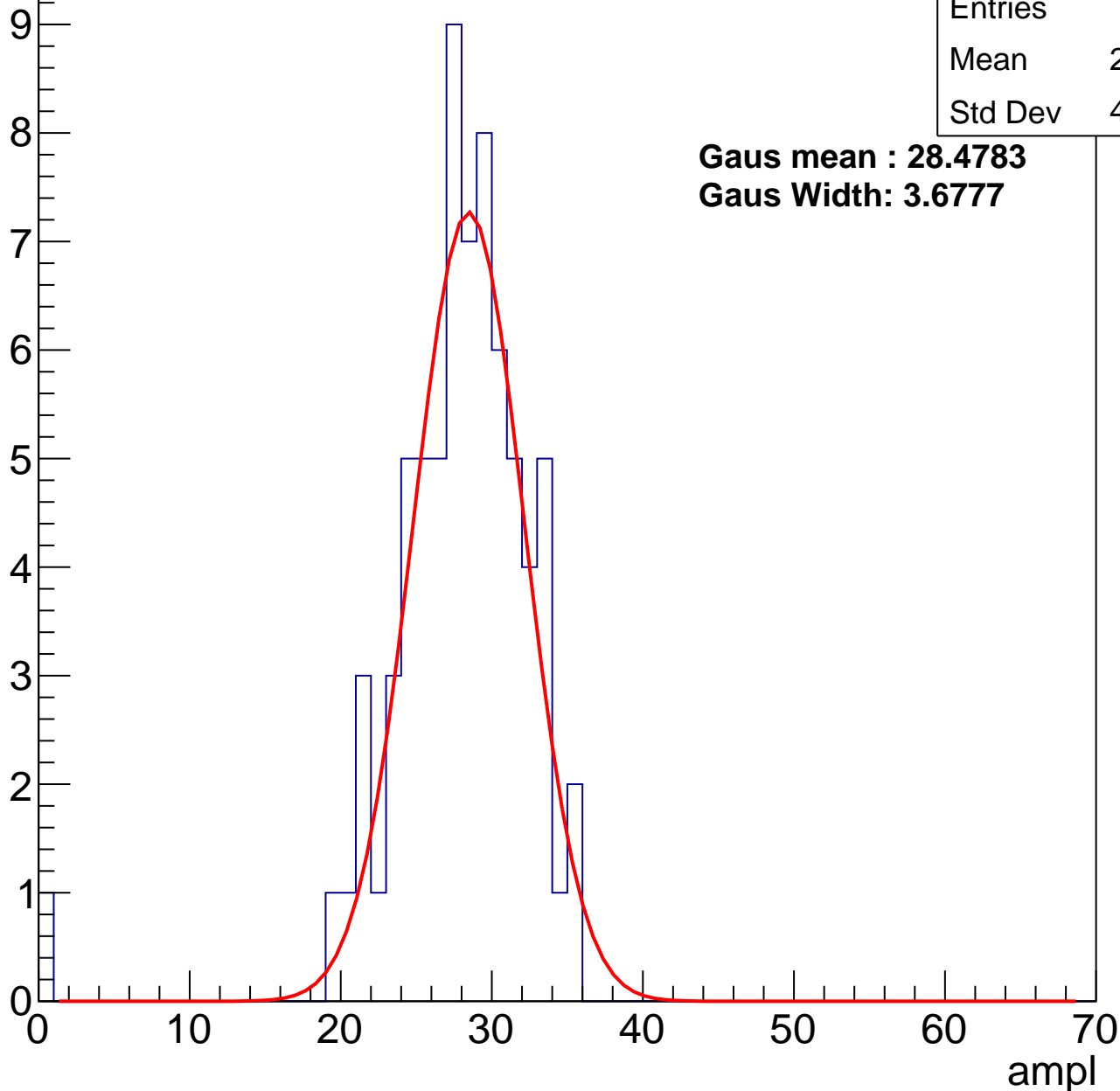
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	27.38
Std Dev	4.877

**Gaus mean : 28.4783**

**Gaus Width: 3.6777**



# B1L103S, U1-ch26, adc1

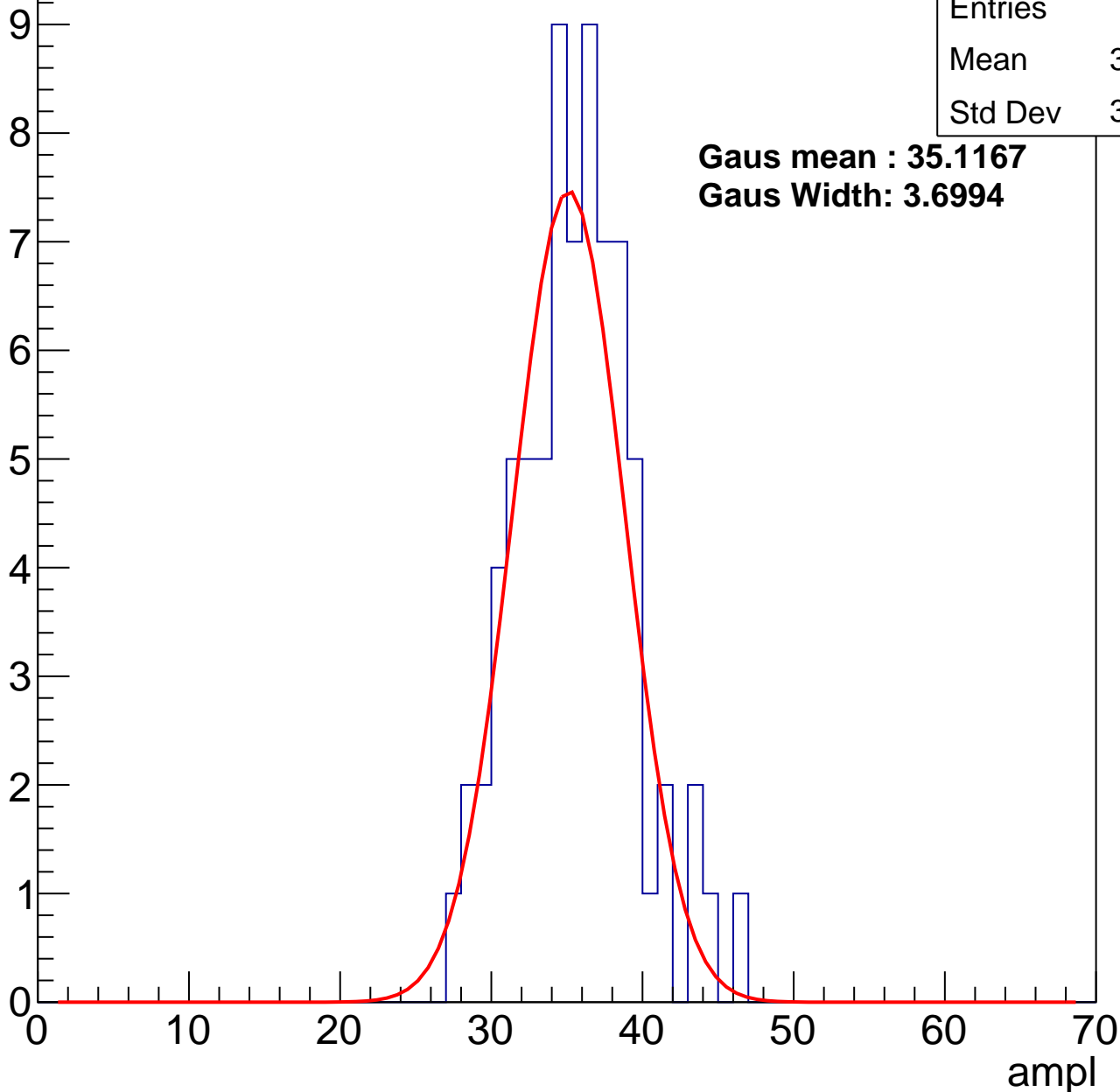
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	35.12
Std Dev	3.819

**Gaus mean : 35.1167**

**Gaus Width: 3.6994**



# B1L103S, U1-ch26, adc2

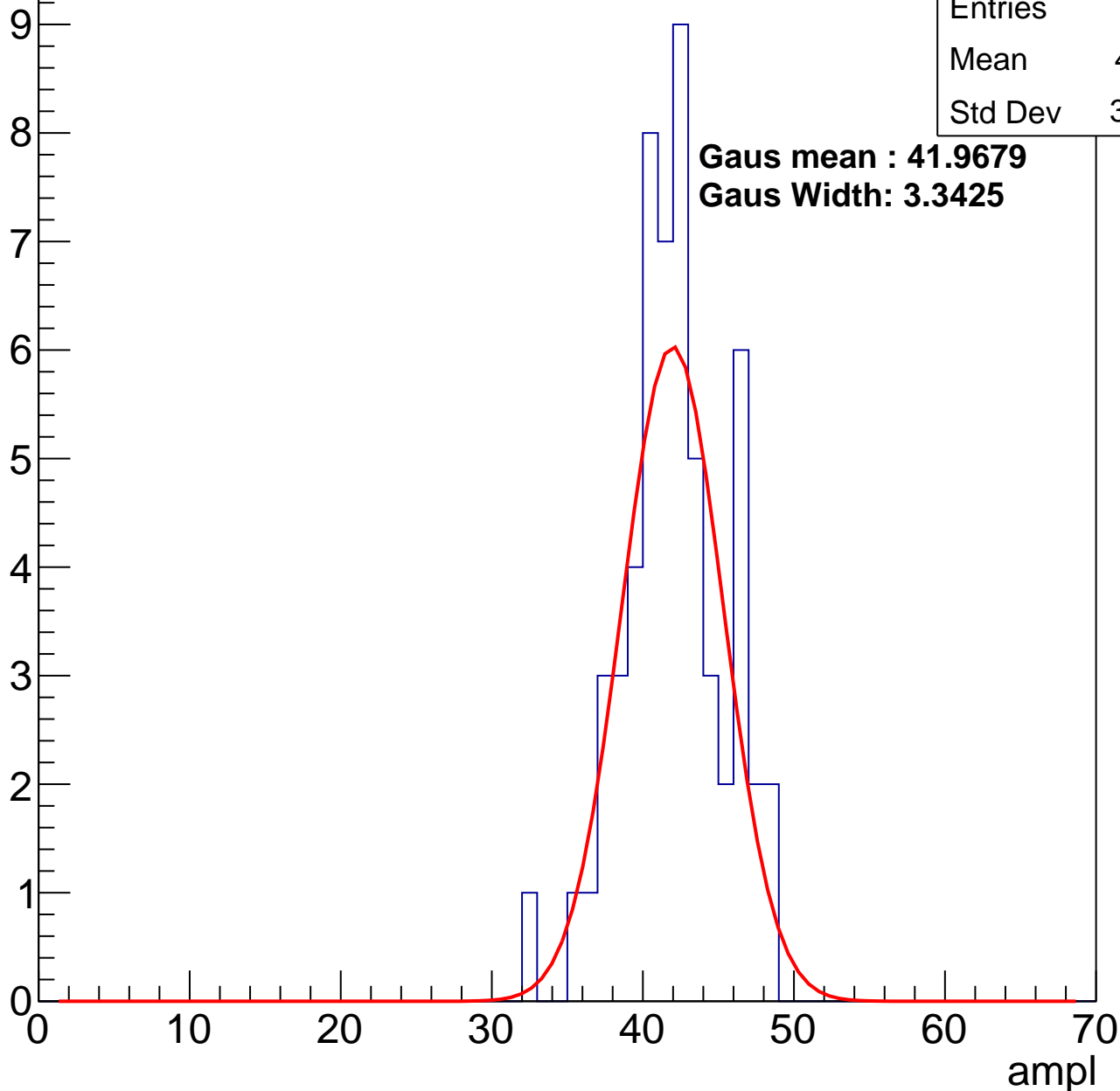
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	41.61
Std Dev	3.318

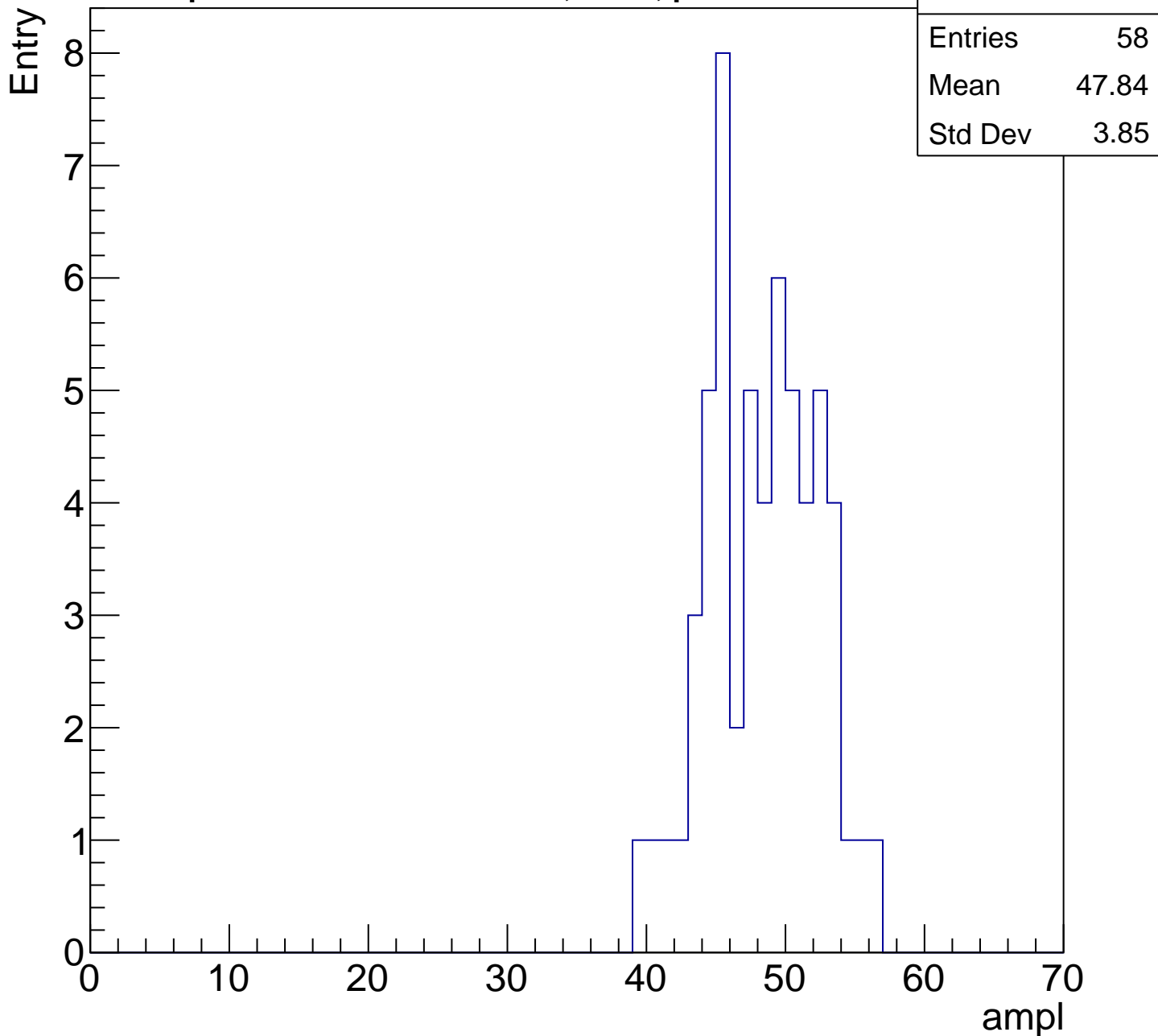
**Gaus mean : 41.9679**

**Gaus Width: 3.3425**



# B1L103S, U1-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

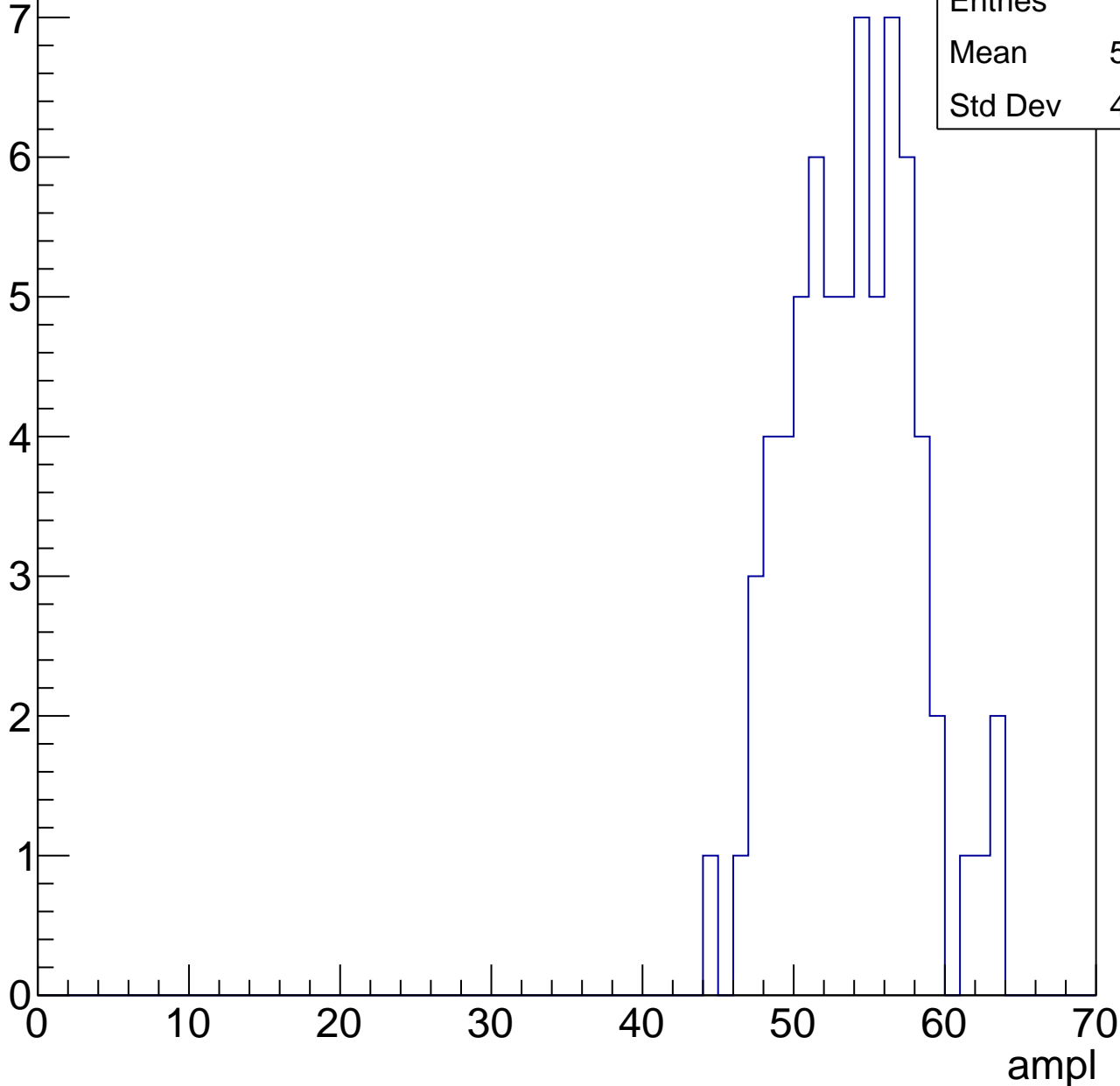


# B1L103S, U1-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	53.42
Std Dev	4.112

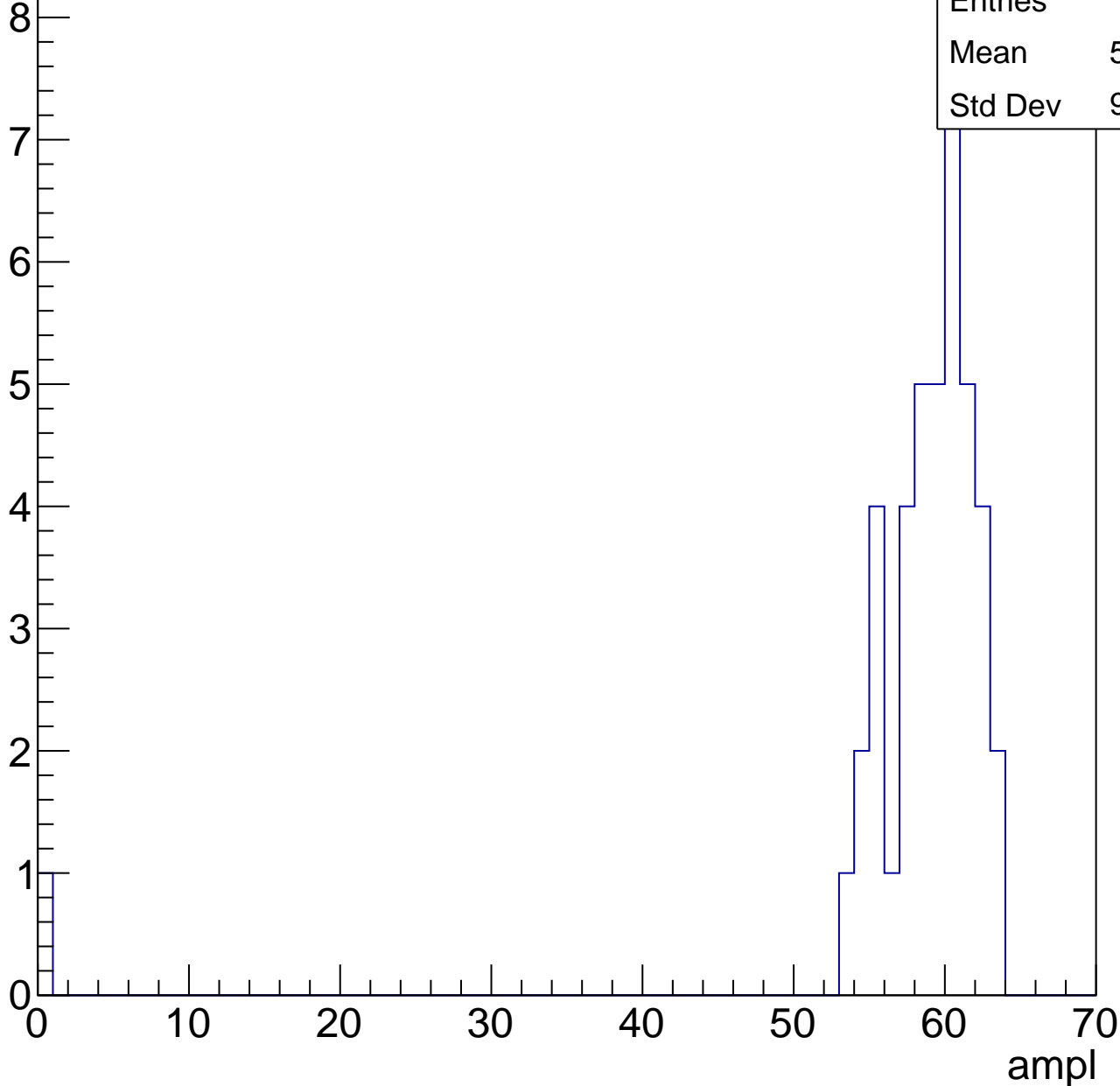


# B1L103S, U1-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	42
Mean	57.36
Std Dev	9.314

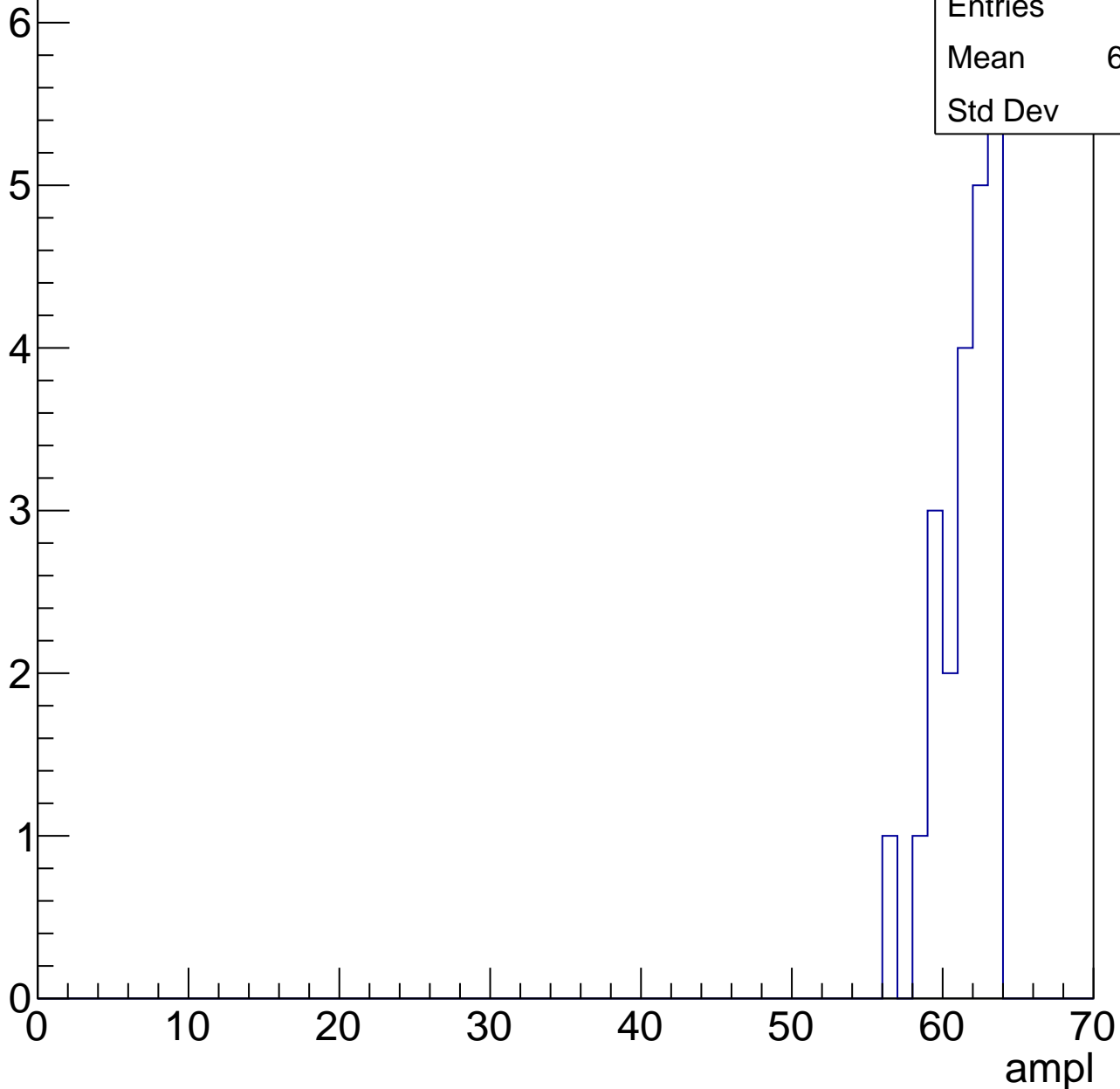


# B1L103S, U1-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	22
Mean	61.05
Std Dev	1.87





# B1L103S, U1-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U1-ch27, adc0

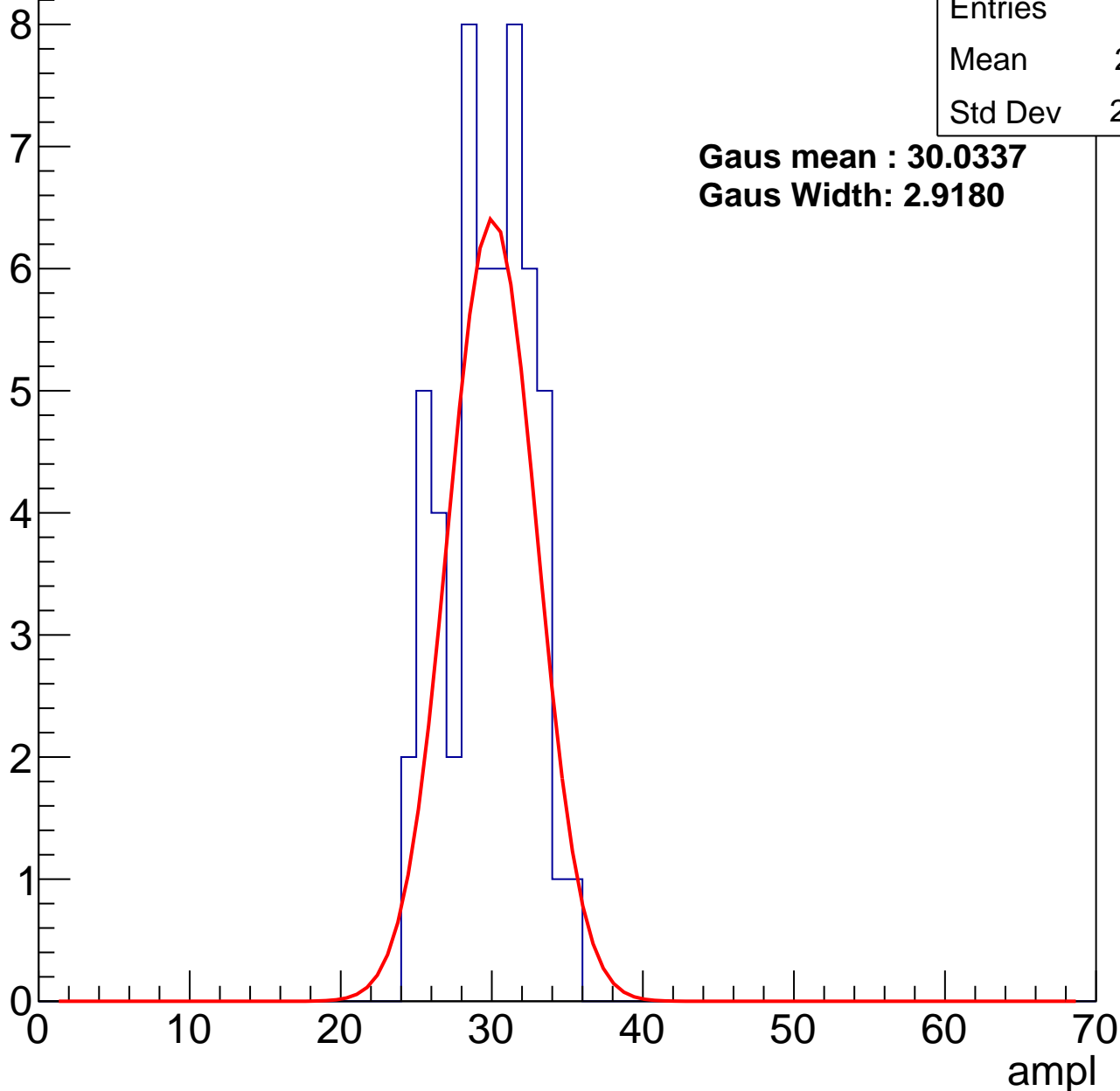
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	29.31
Std Dev	2.754

**Gaus mean : 30.0337**

**Gaus Width: 2.9180**



# B1L103S, U1-ch27, adc1

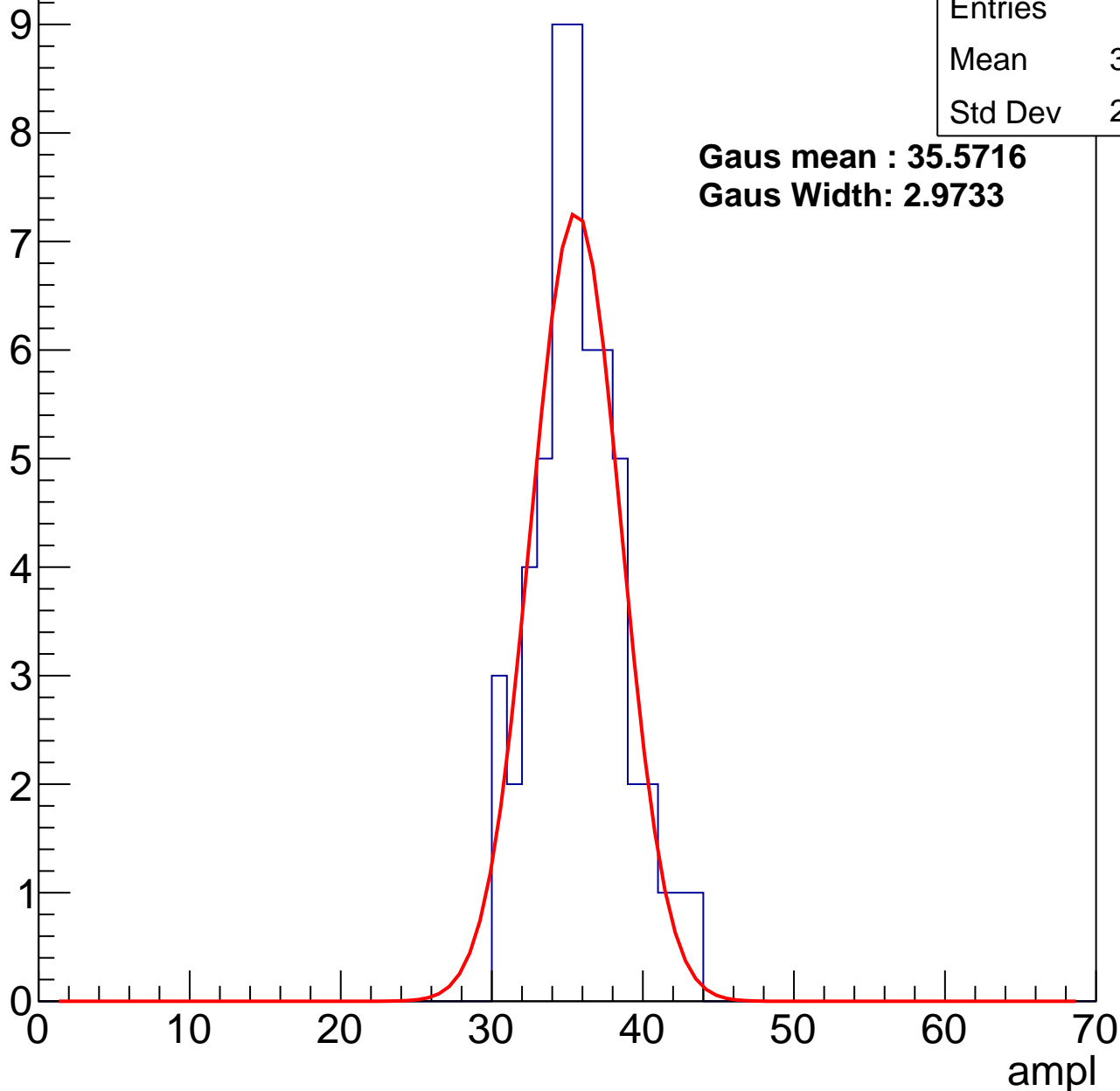
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	35.32
Std Dev	2.904

**Gaus mean : 35.5716**

**Gaus Width: 2.9733**



# B1L103S, U1-ch27, adc2

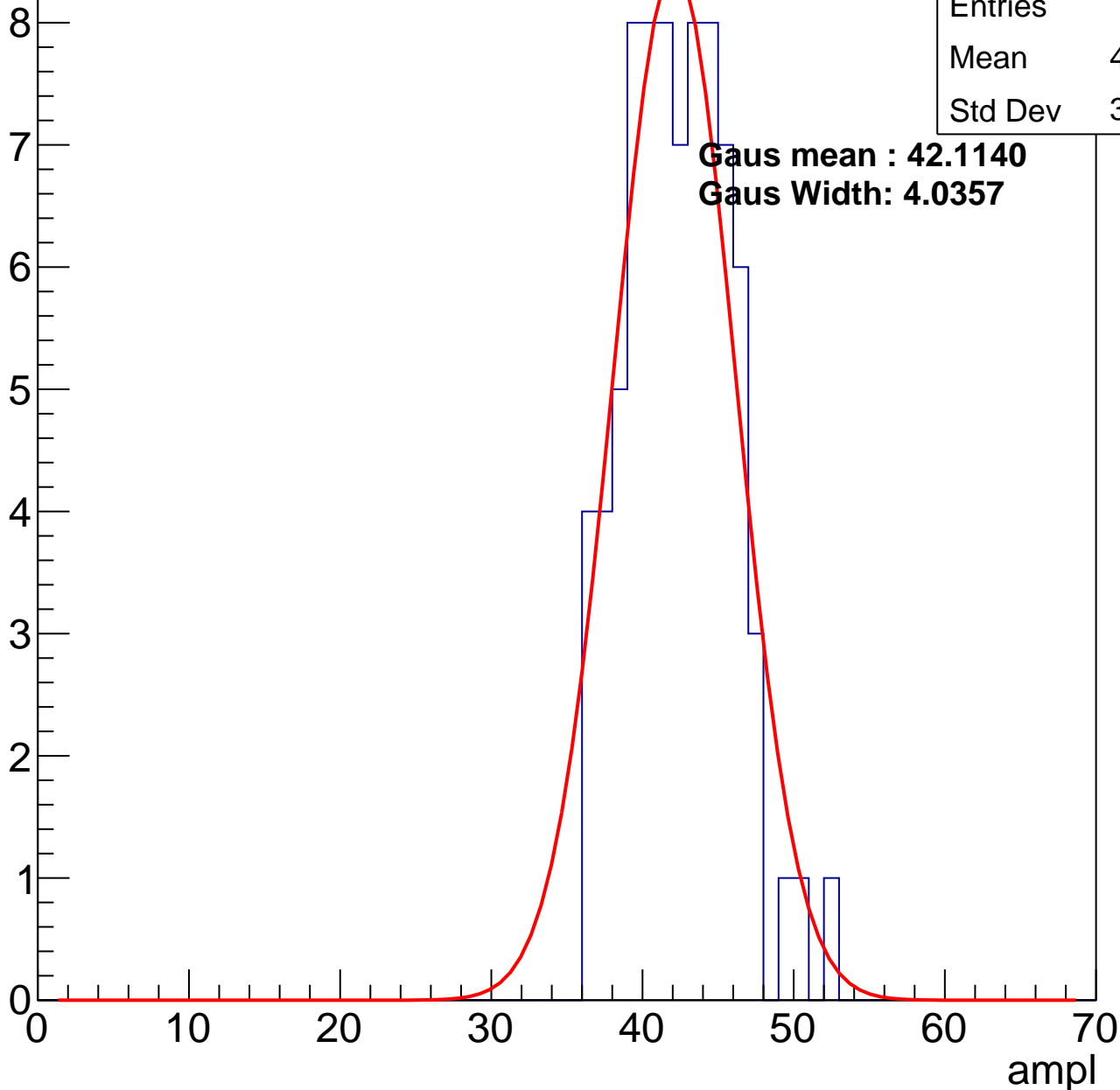
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	41.96
Std Dev	3.418

**Gaus mean : 42.1140**

**Gaus Width: 4.0357**

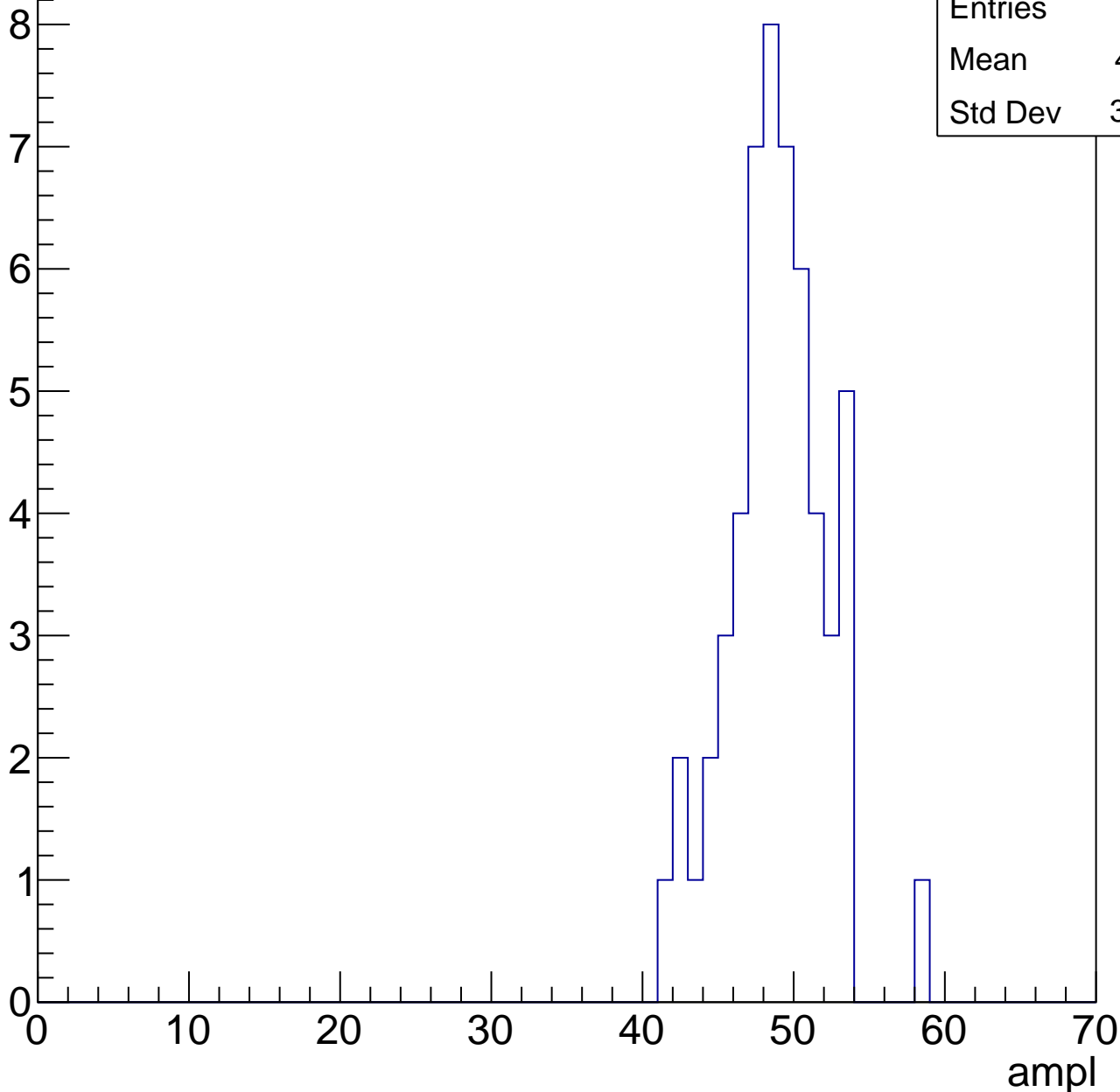


# B1L103S, U1-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

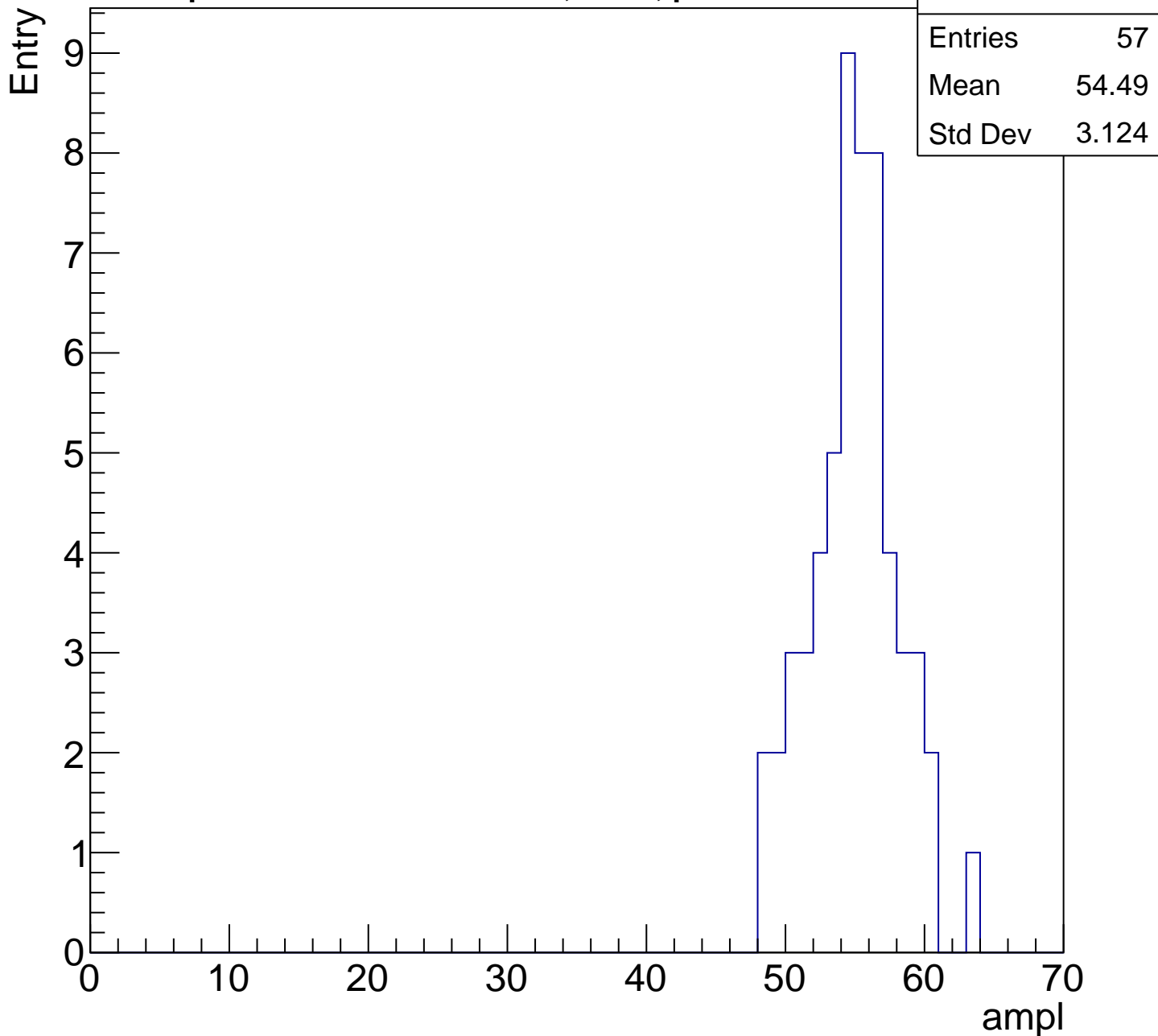
Entry

Entries	54
Mean	48.41
Std Dev	3.218



# B1L103S, U1-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

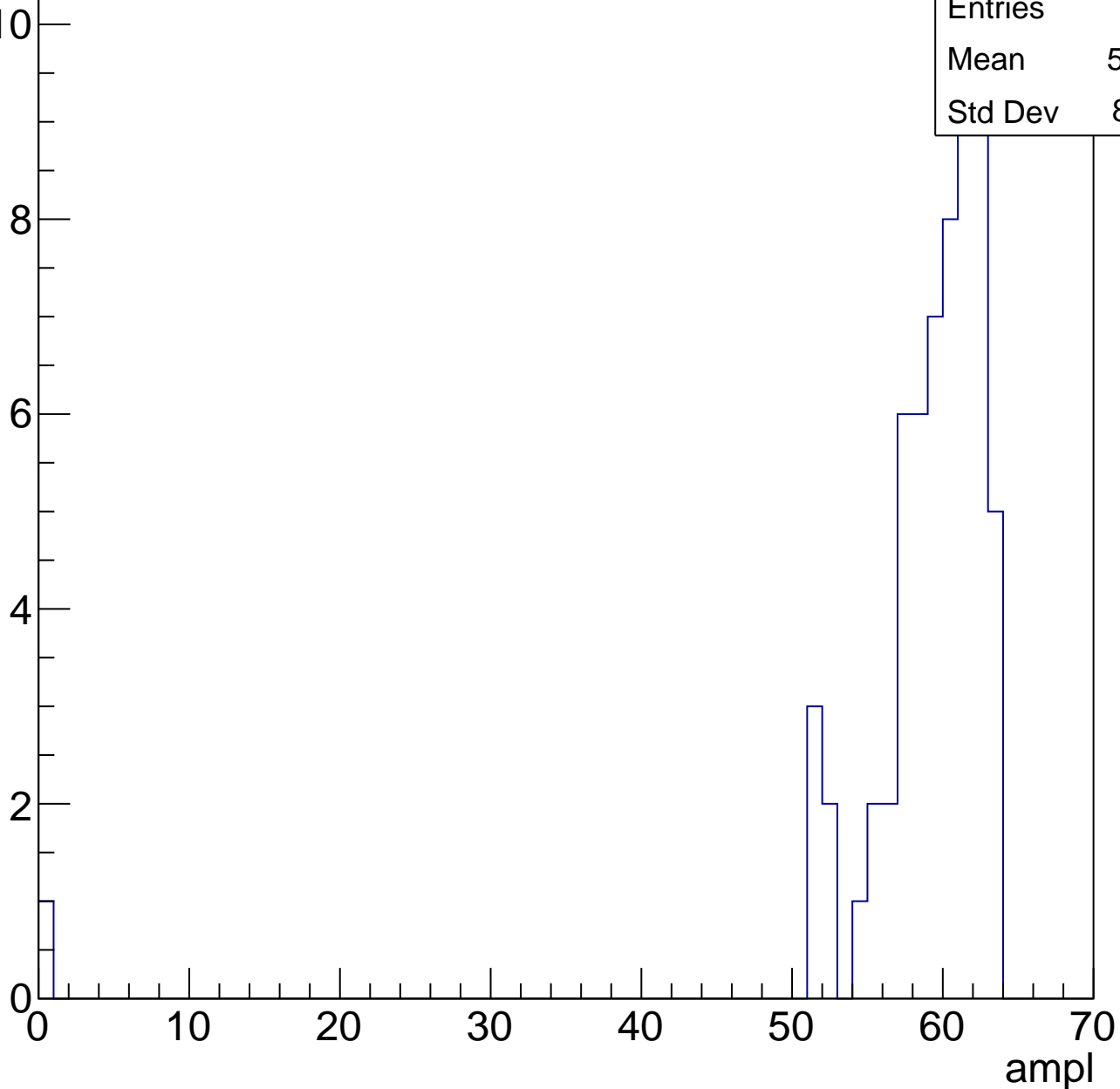


# B1L103S, U1-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

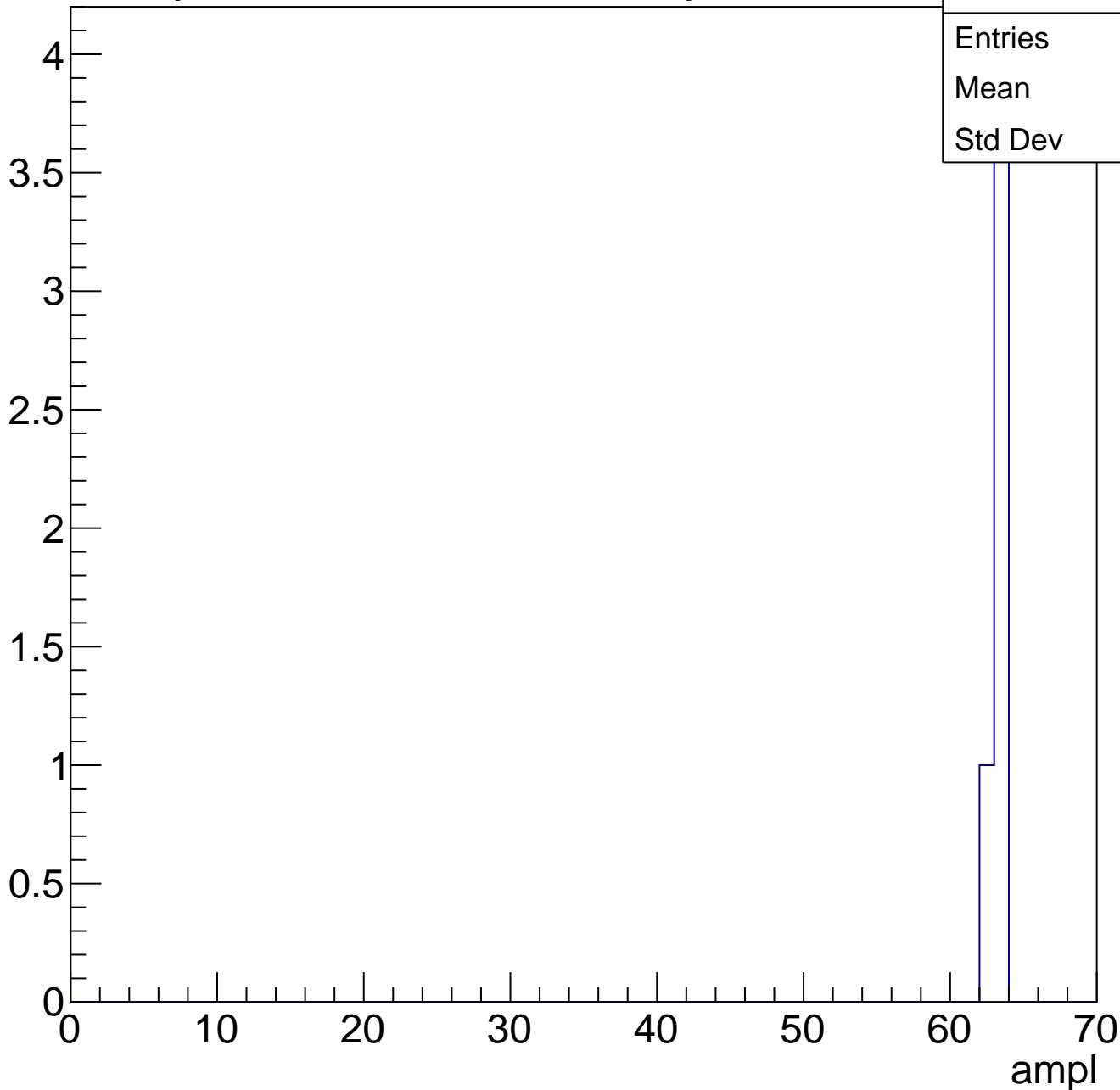
Entries	62
Mean	58.05
Std Dev	8.061



# B1L103S, U1-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U1-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U1-ch28, adc0

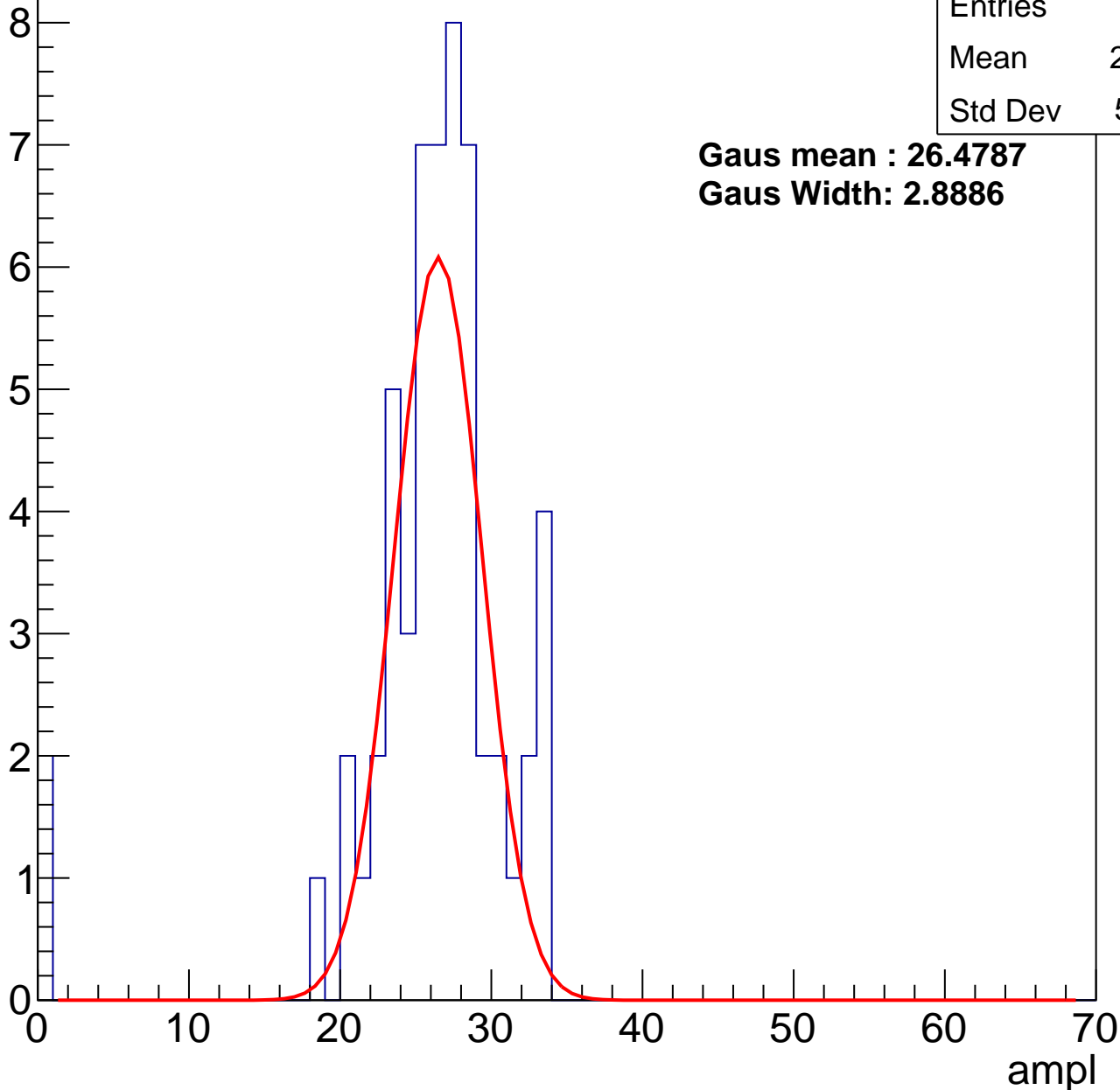
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	25.43
Std Dev	5.931

**Gaus mean : 26.4787**

**Gaus Width: 2.8886**



# B1L103S, U1-ch28, adc1

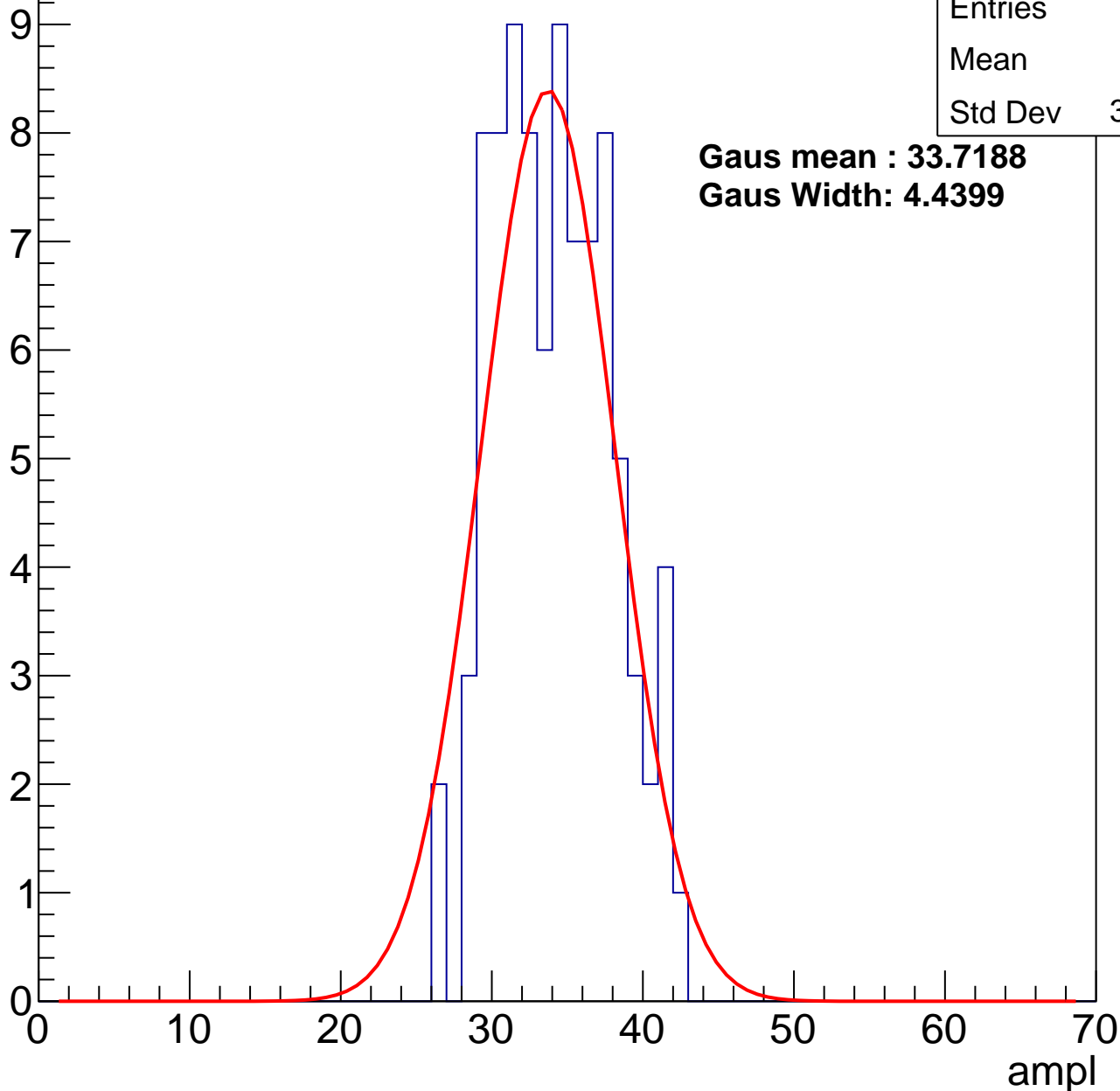
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	90
Mean	33.7
Std Dev	3.755

**Gaus mean : 33.7188**

**Gaus Width: 4.4399**

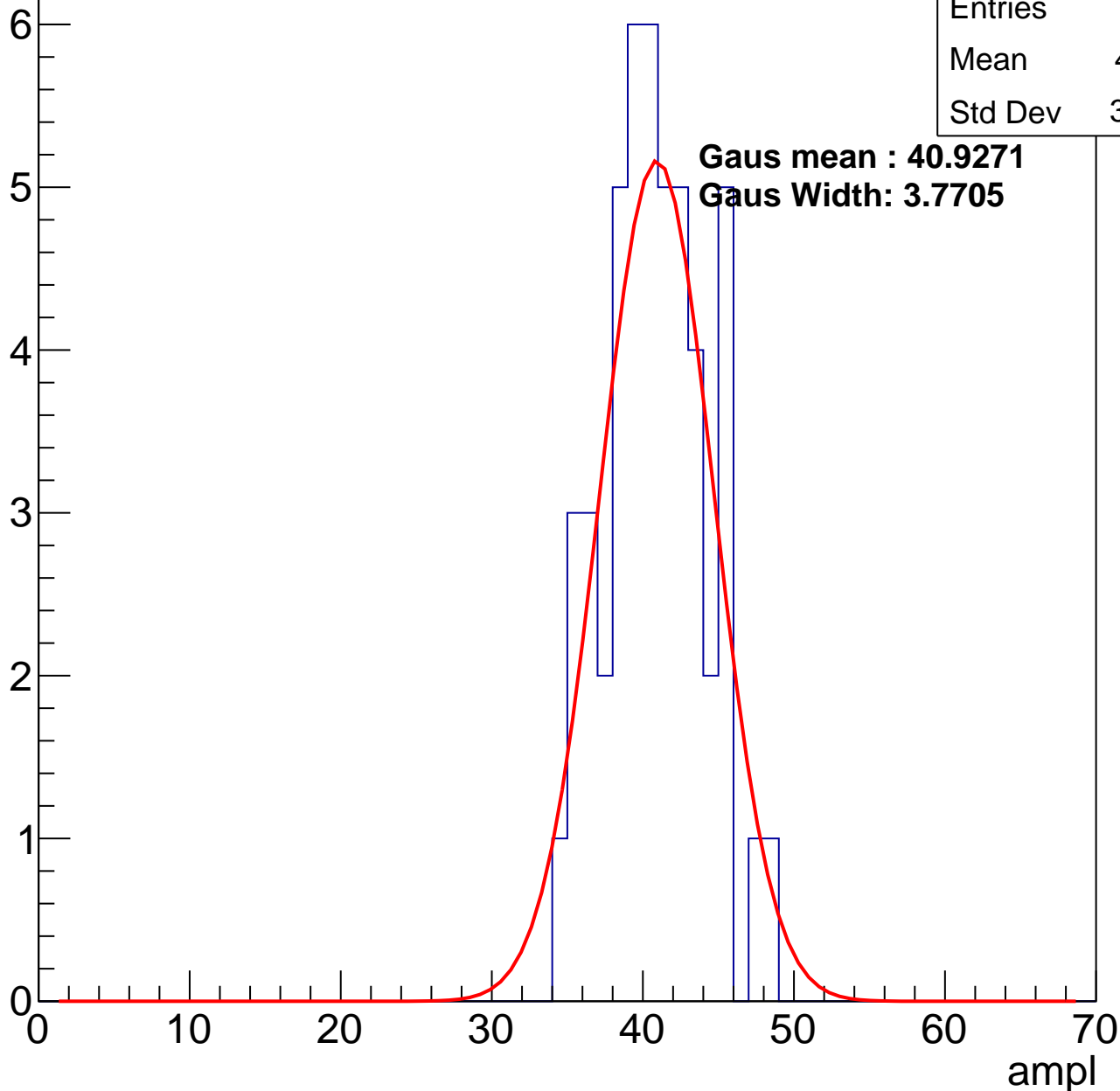


# B1L103S, U1-ch28, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	40.41
Std Dev	3.276

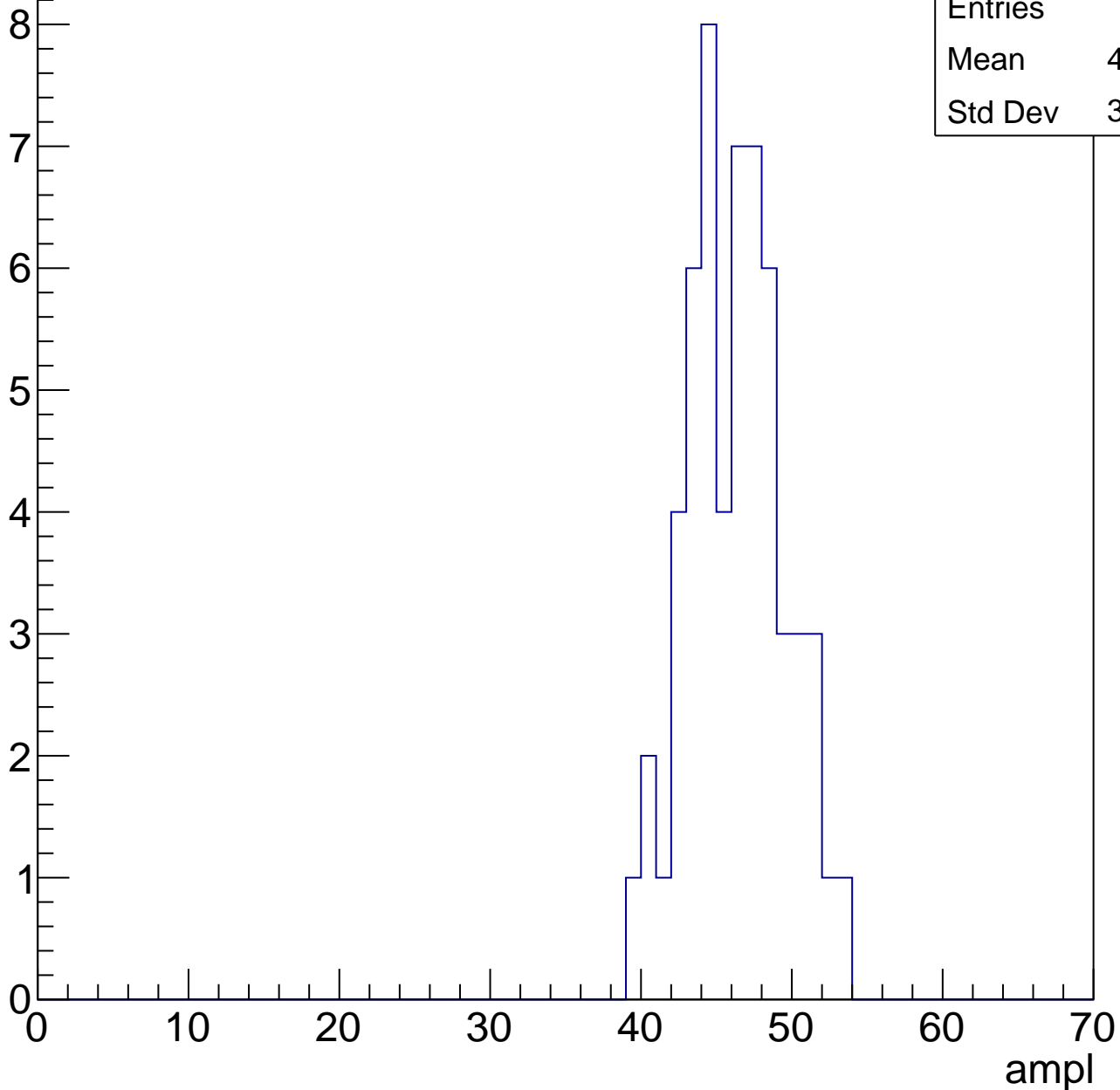


# B1L103S, U1-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

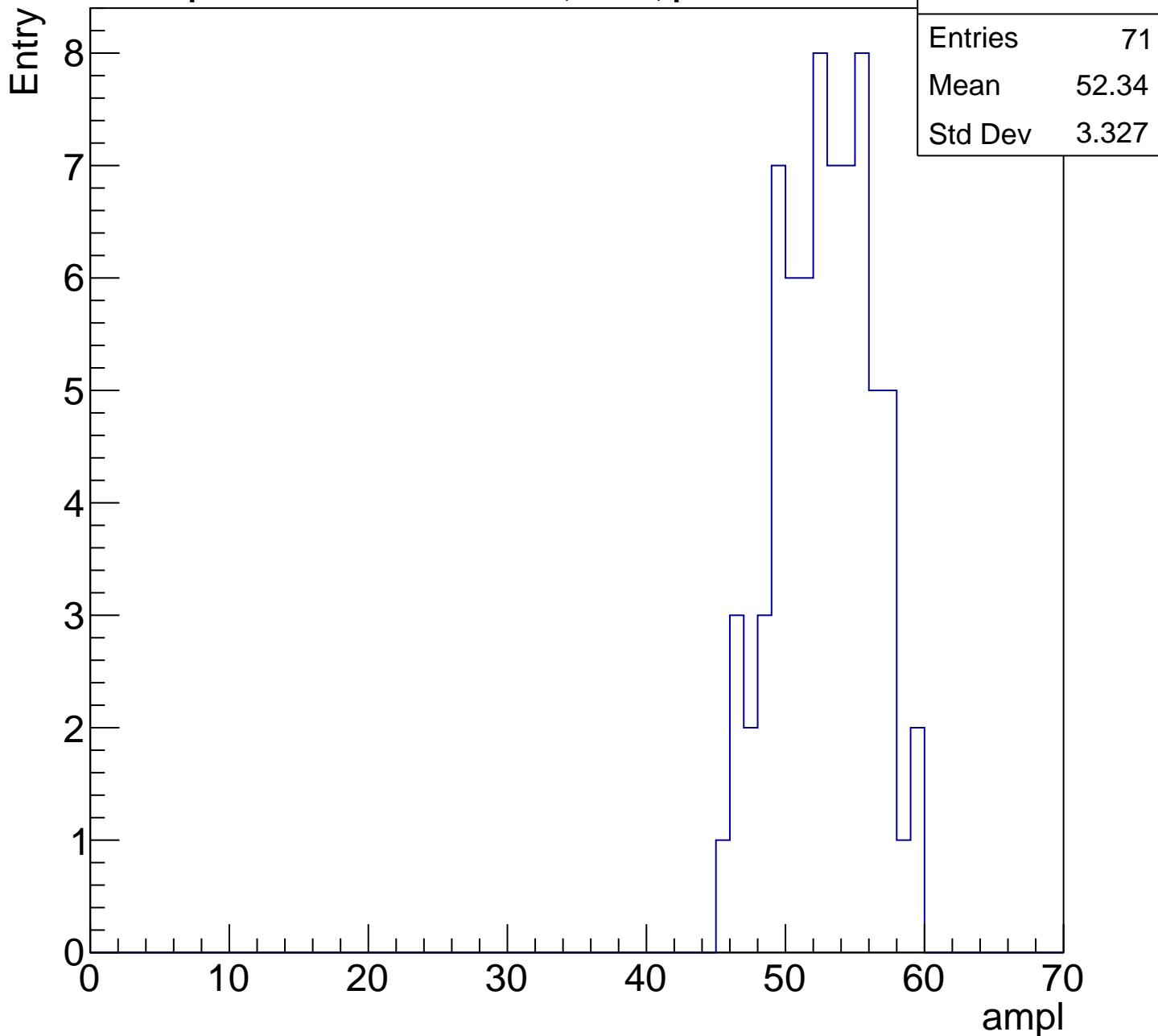
Entry

Entries	57
Mean	45.82
Std Dev	3.146



# B1L103S, U1-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

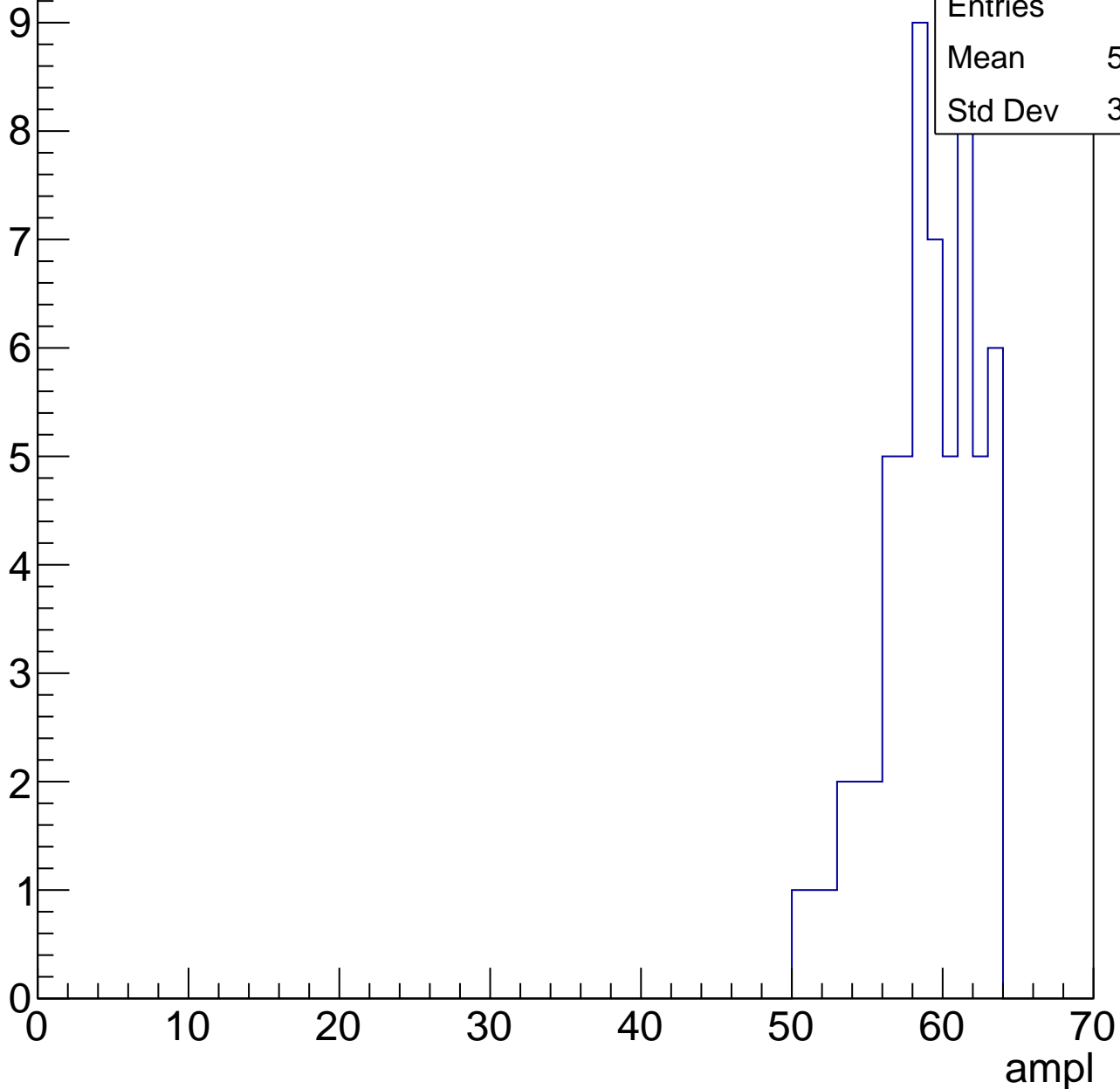


# B1L103S, U1-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	58.57
Std Dev	3.143

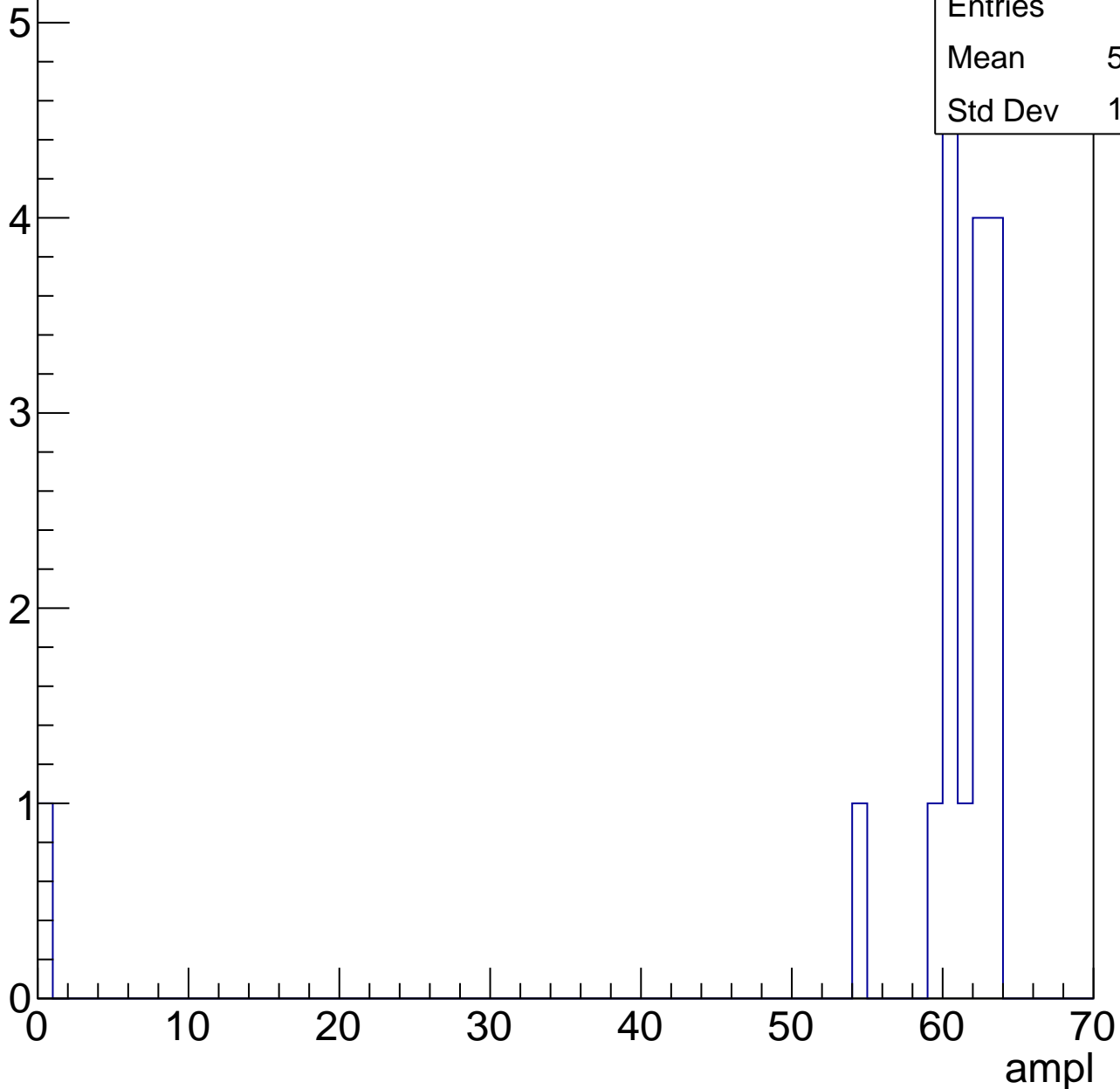


# B1L103S, U1-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	17
Mean	57.29
Std Dev	14.48





# B1L103S, U1-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	62
Std Dev	0

# B1L103S, U1-ch29, adc0

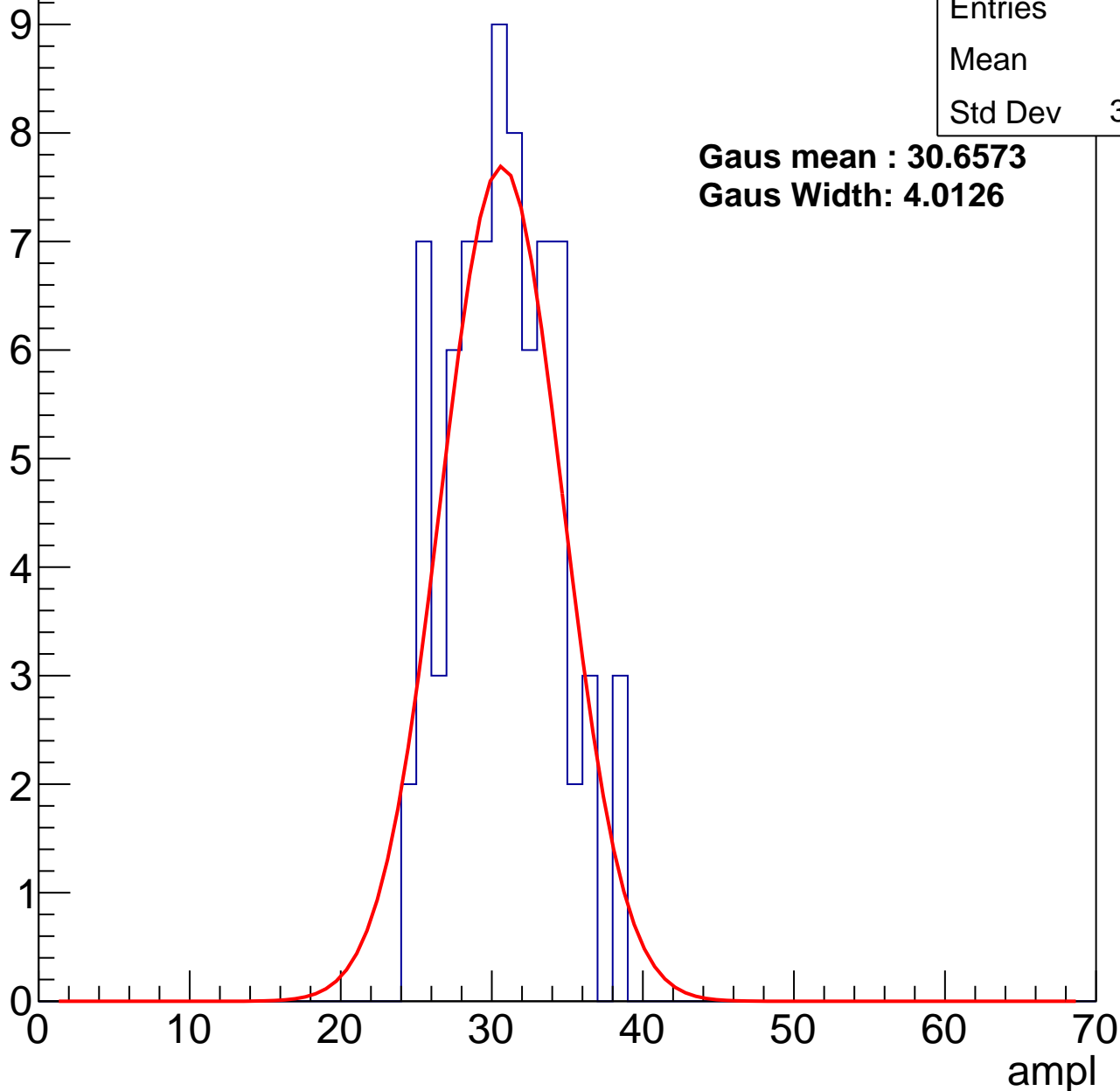
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	30.3
Std Dev	3.483

**Gaus mean : 30.6573**

**Gaus Width: 4.0126**



# B1L103S, U1-ch29, adc1

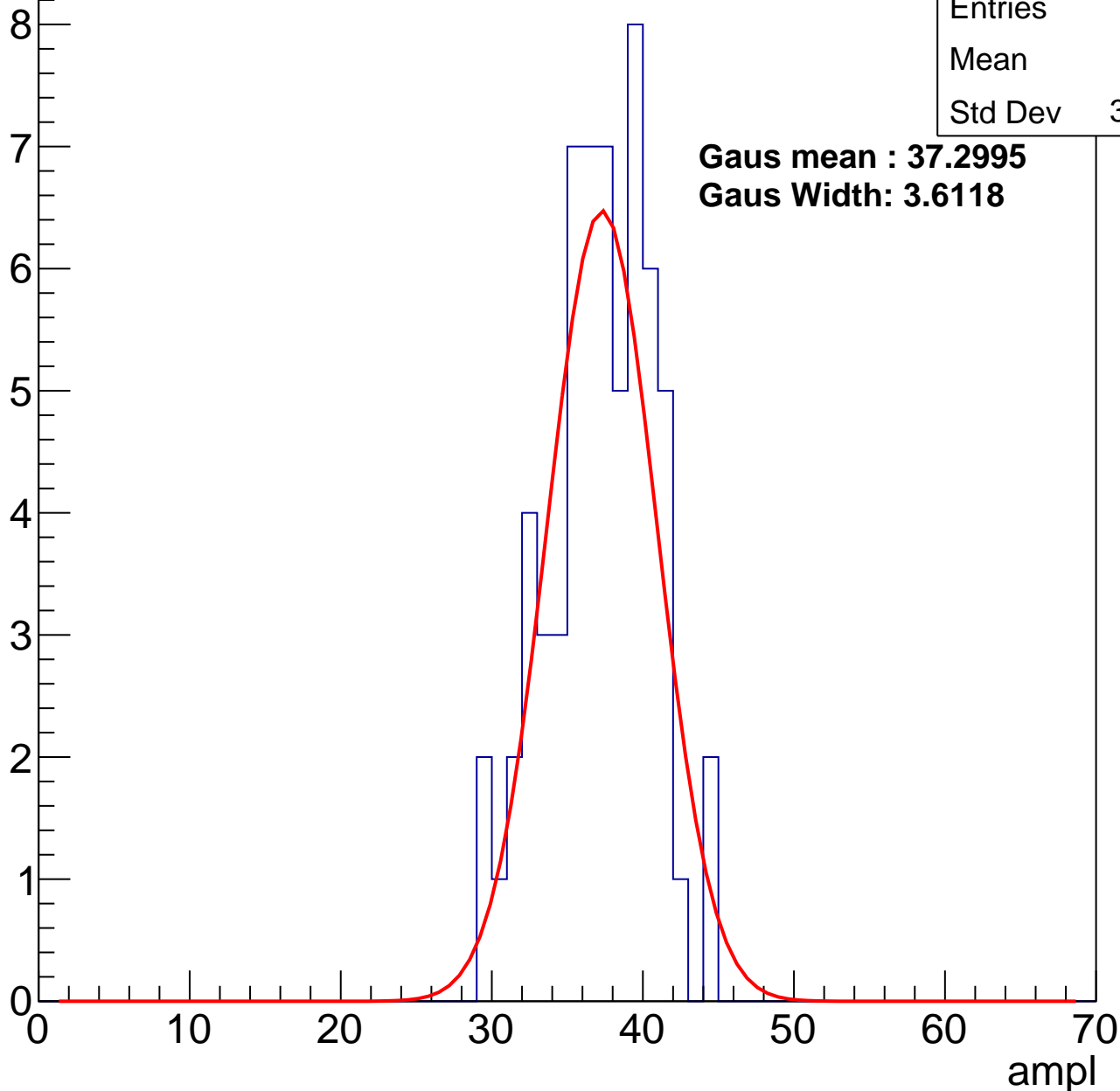
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	36.7
Std Dev	3.444

**Gaus mean : 37.2995**

**Gaus Width: 3.6118**



# B1L103S, U1-ch29, adc2

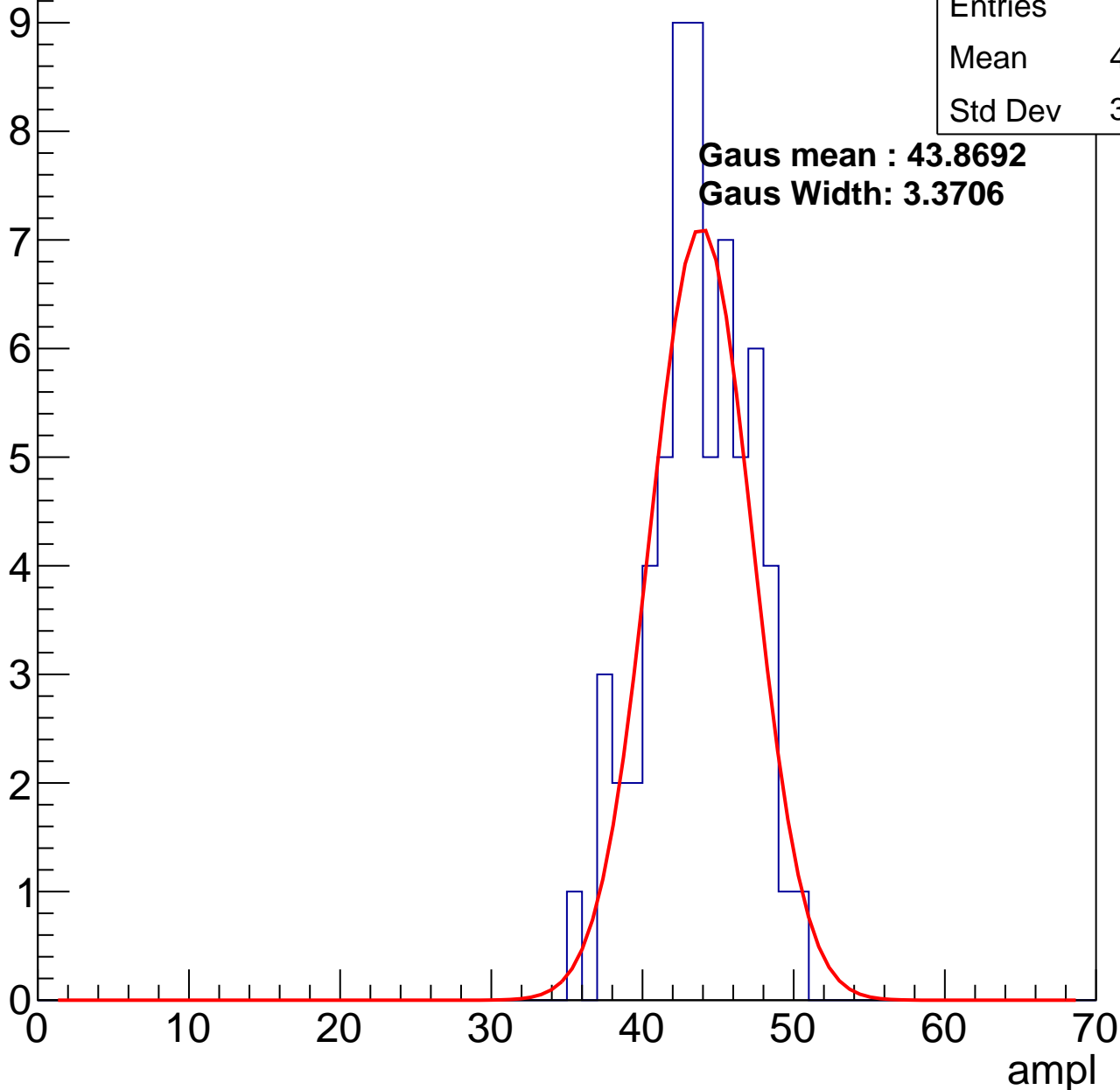
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	43.25
Std Dev	3.245

**Gaus mean : 43.8692**

**Gaus Width: 3.3706**

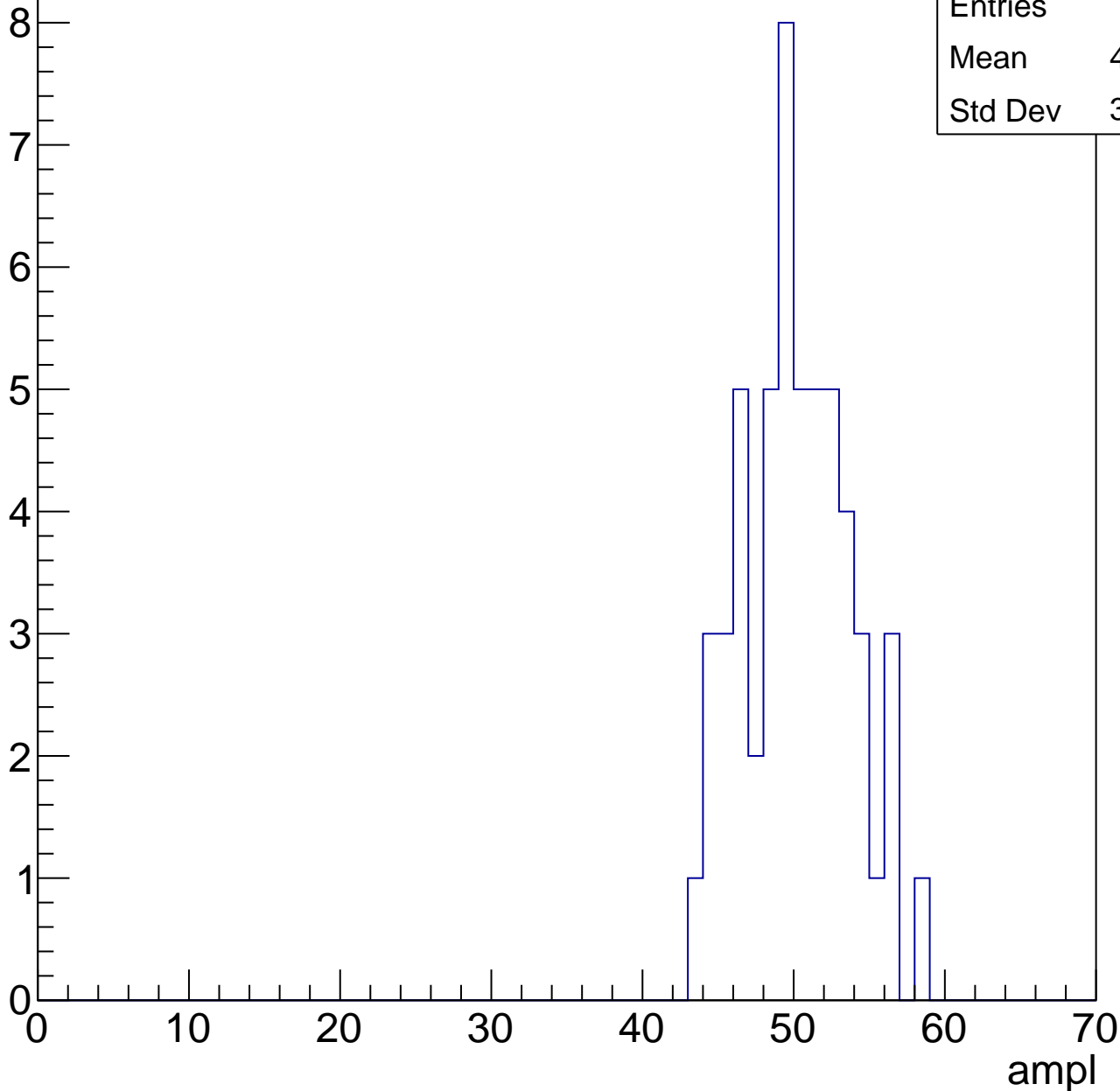


# B1L103S, U1-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

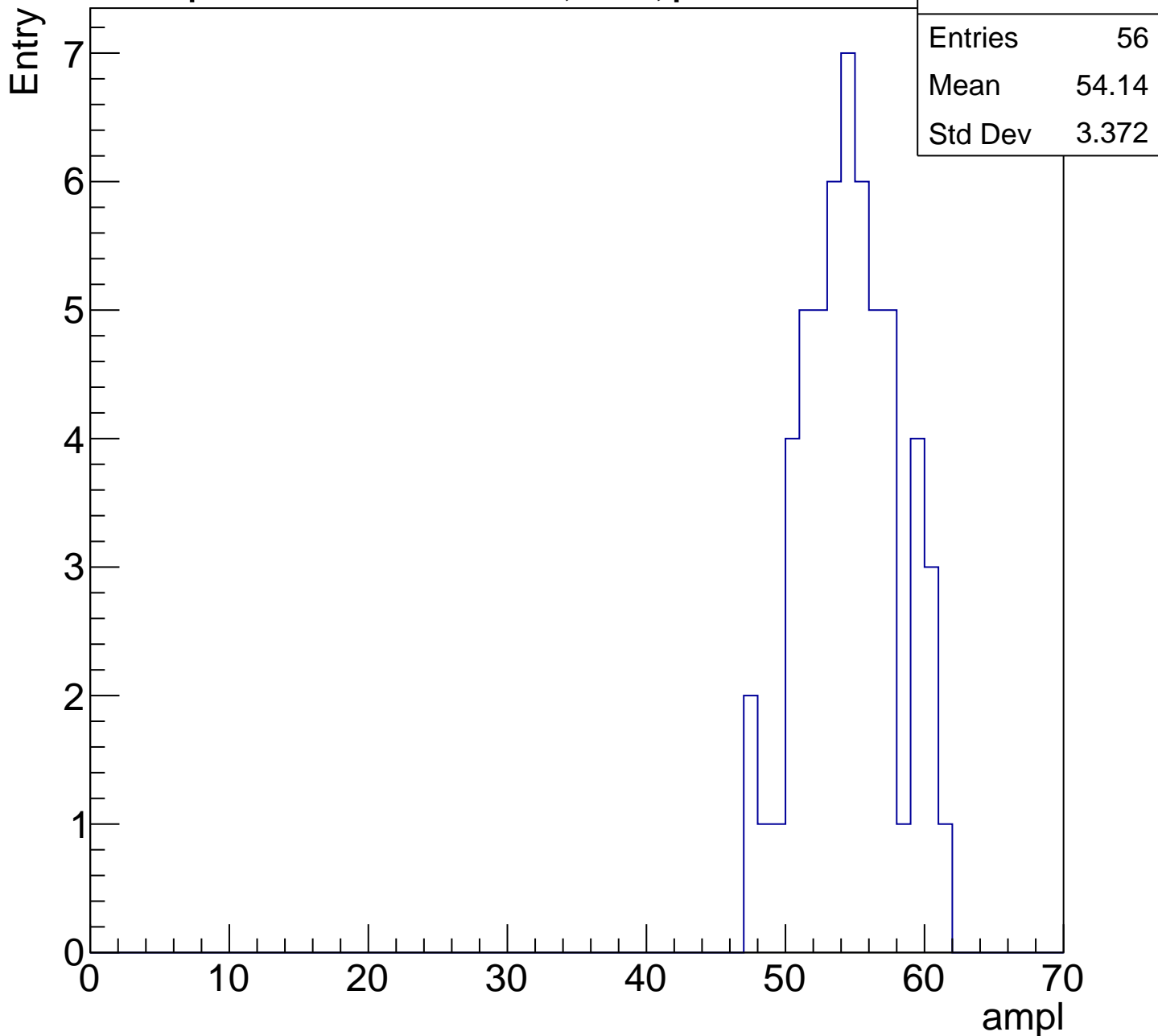
Entry

Entries	54
Mean	49.74
Std Dev	3.497



# B1L103S, U1-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U1-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	52
Mean	58.79
Std Dev	8.547

ampl

0

10

20

30

40

50

60

70

# B1L103S, U1-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries	9
Mean	60.22
Std Dev	2.439



# B1L103S, U1-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U1-ch30, adc0

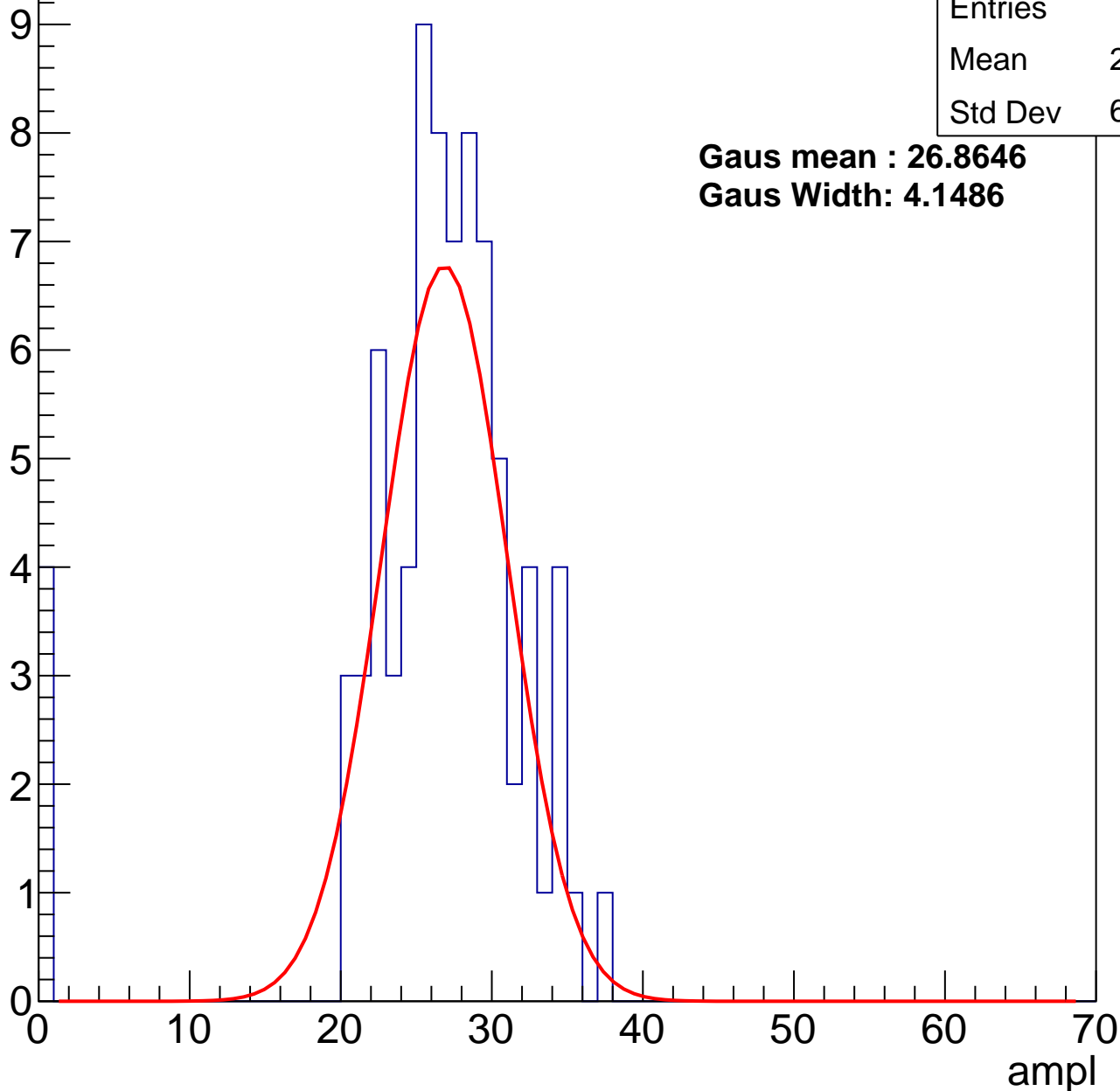
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	25.62
Std Dev	6.988

**Gaus mean : 26.8646**

**Gaus Width: 4.1486**



# B1L103S, U1-ch30, adc1

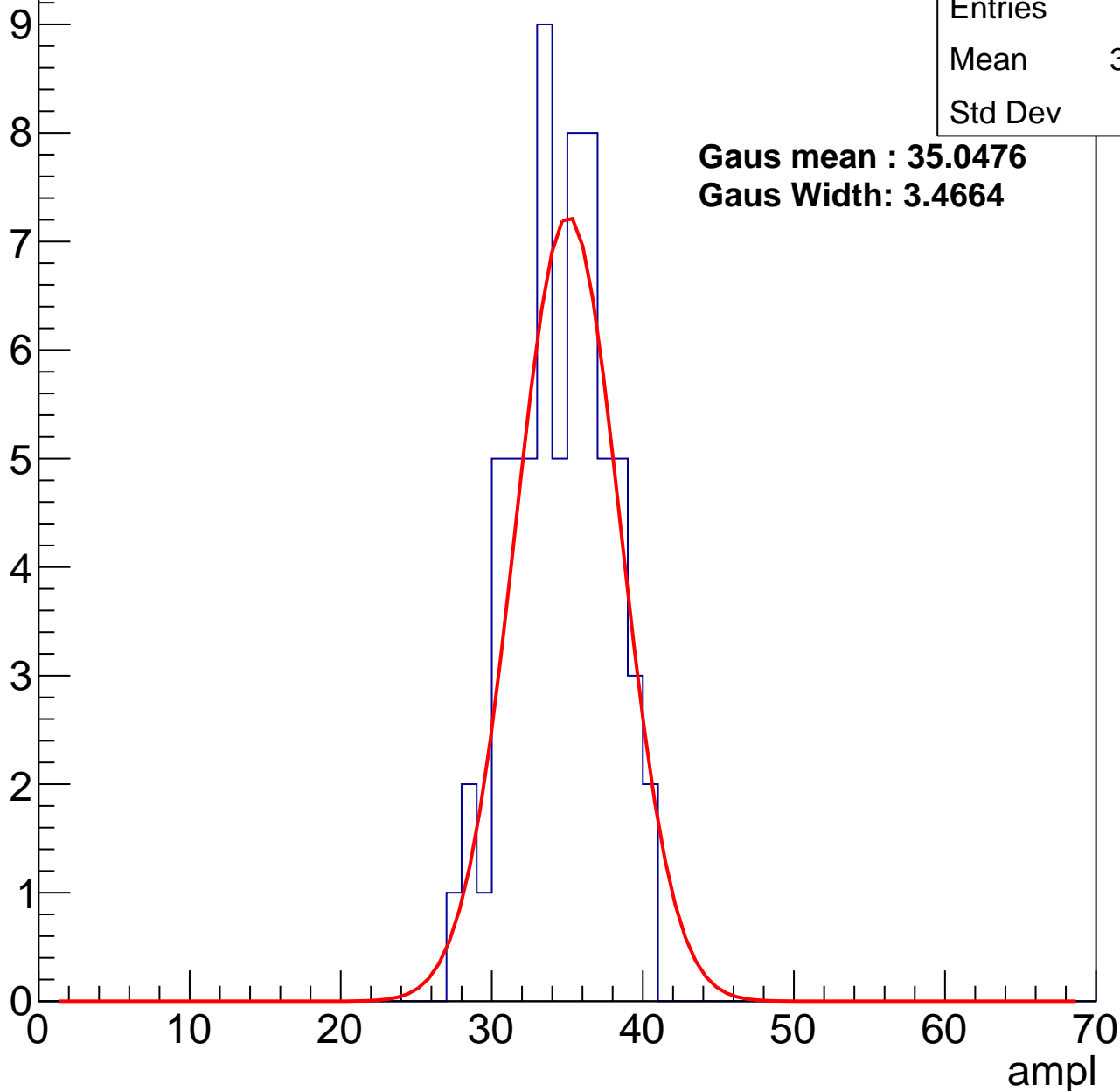
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	34.12
Std Dev	3.09

**Gaus mean : 35.0476**

**Gaus Width: 3.4664**



# B1L103S, U1-ch30, adc2

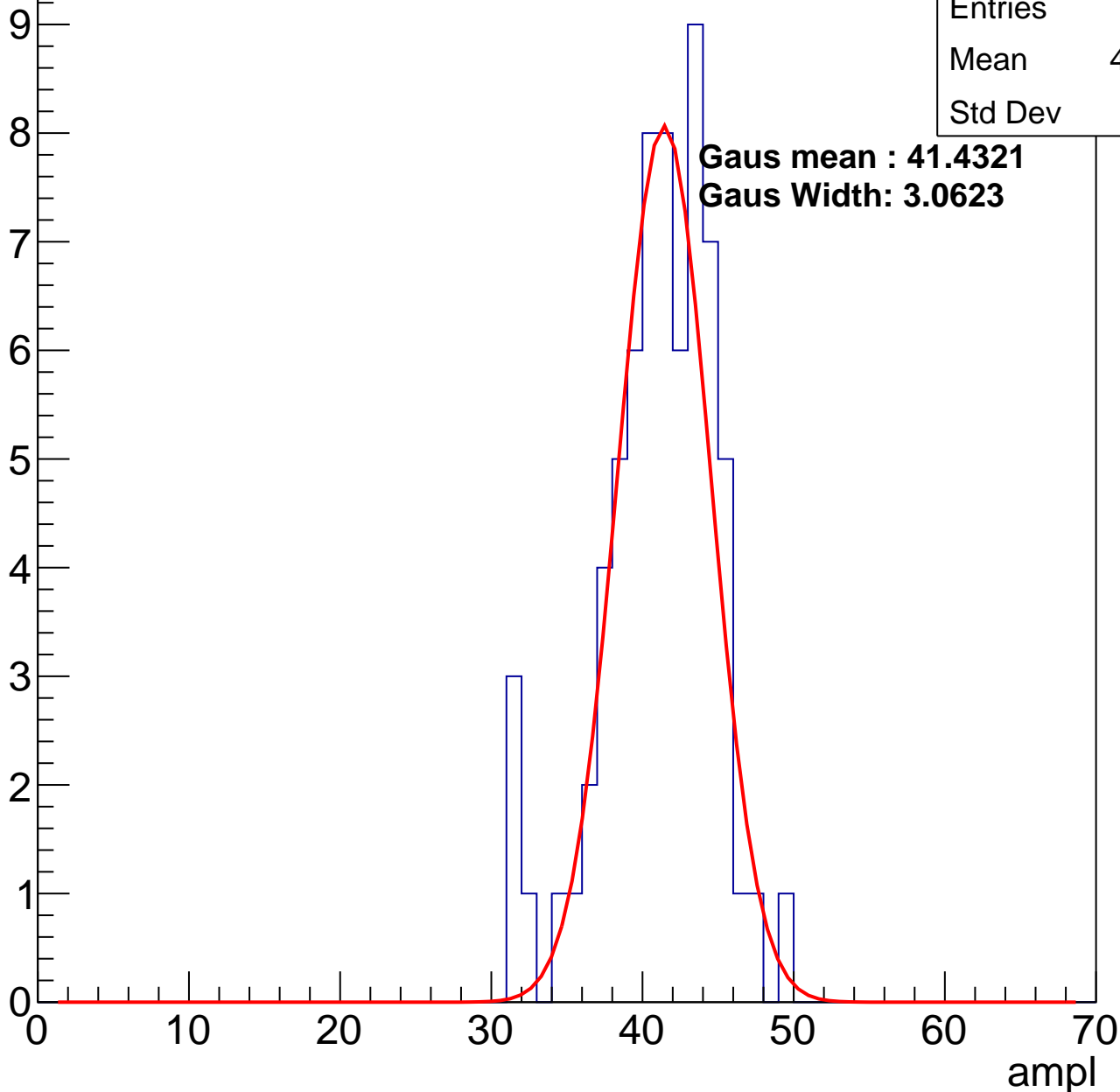
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	40.58
Std Dev	3.72

**Gaus mean : 41.4321**

**Gaus Width: 3.0623**

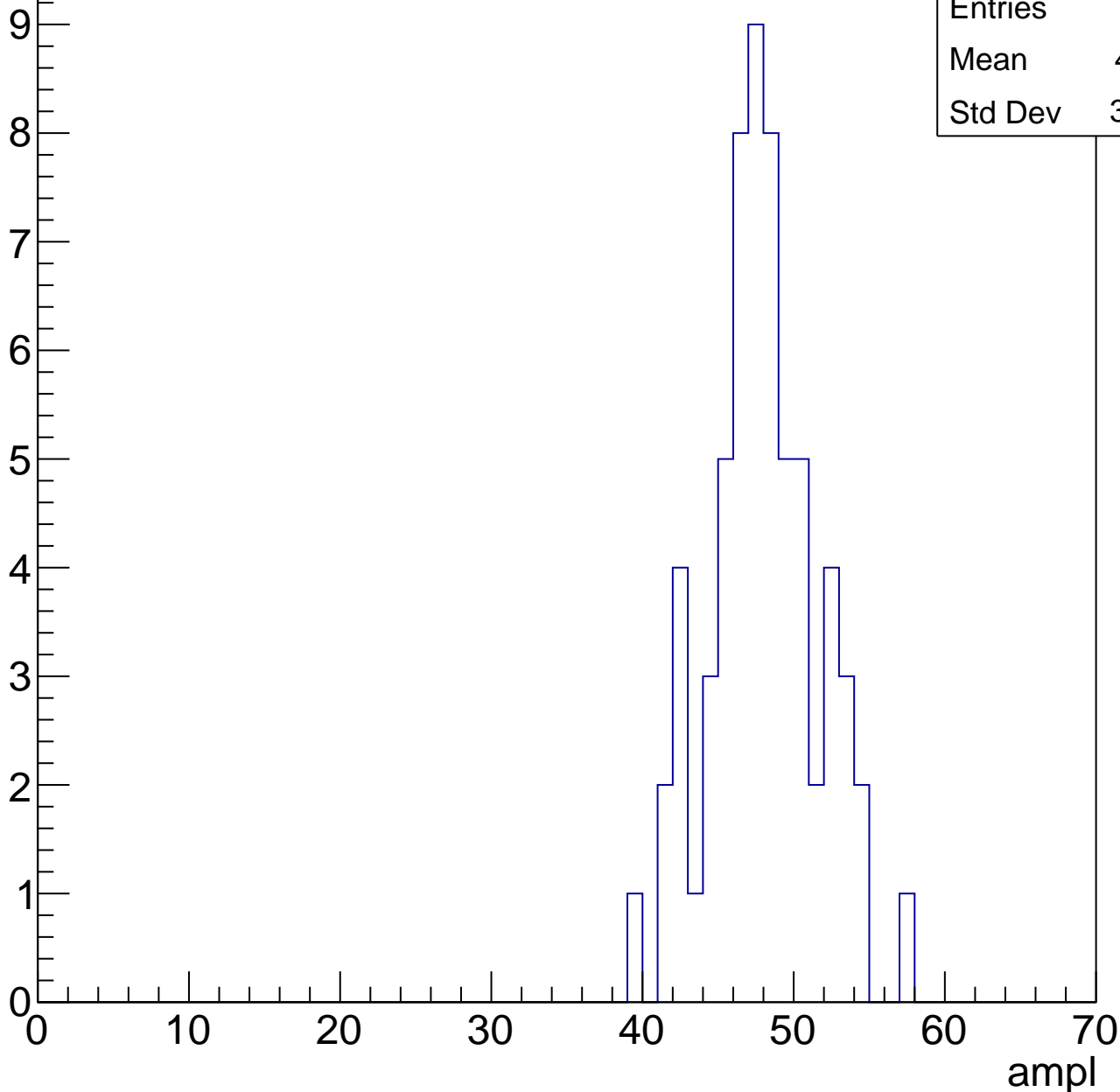


# B1L103S, U1-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	47.51
Std Dev	3.567

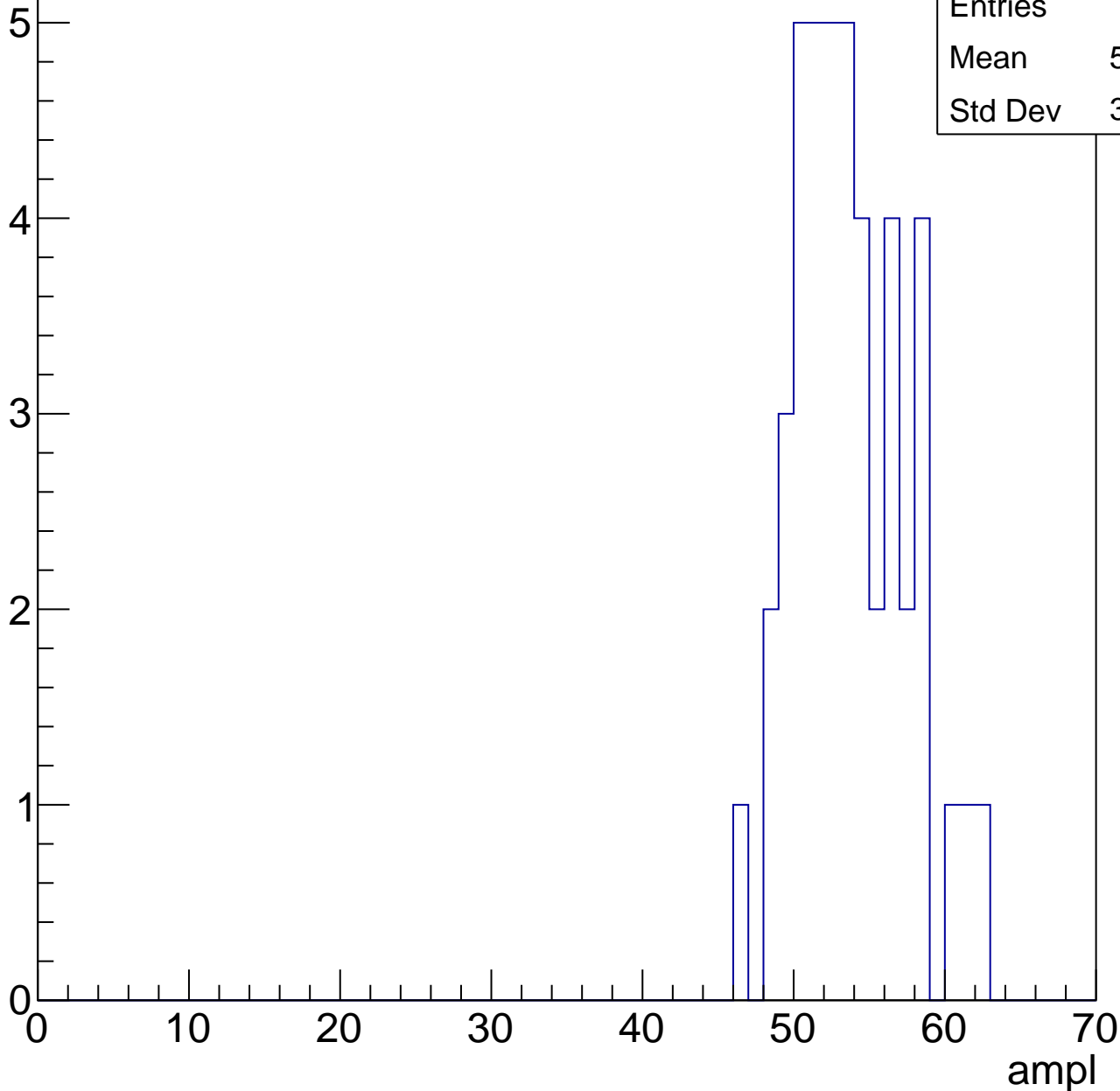


# B1L103S, U1-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

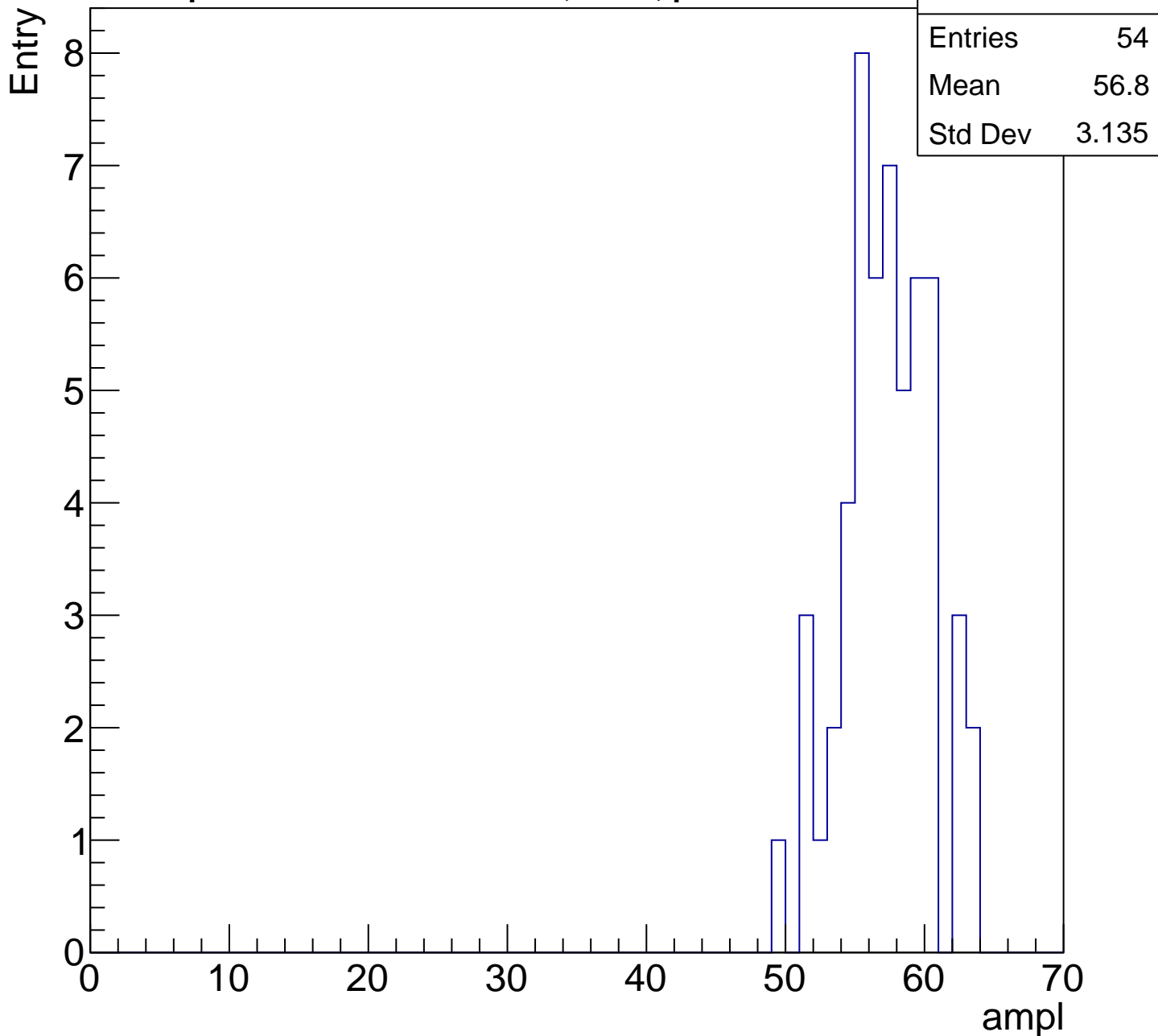
Entry

Entries	45
Mean	53.29
Std Dev	3.612



# B1L103S, U1-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

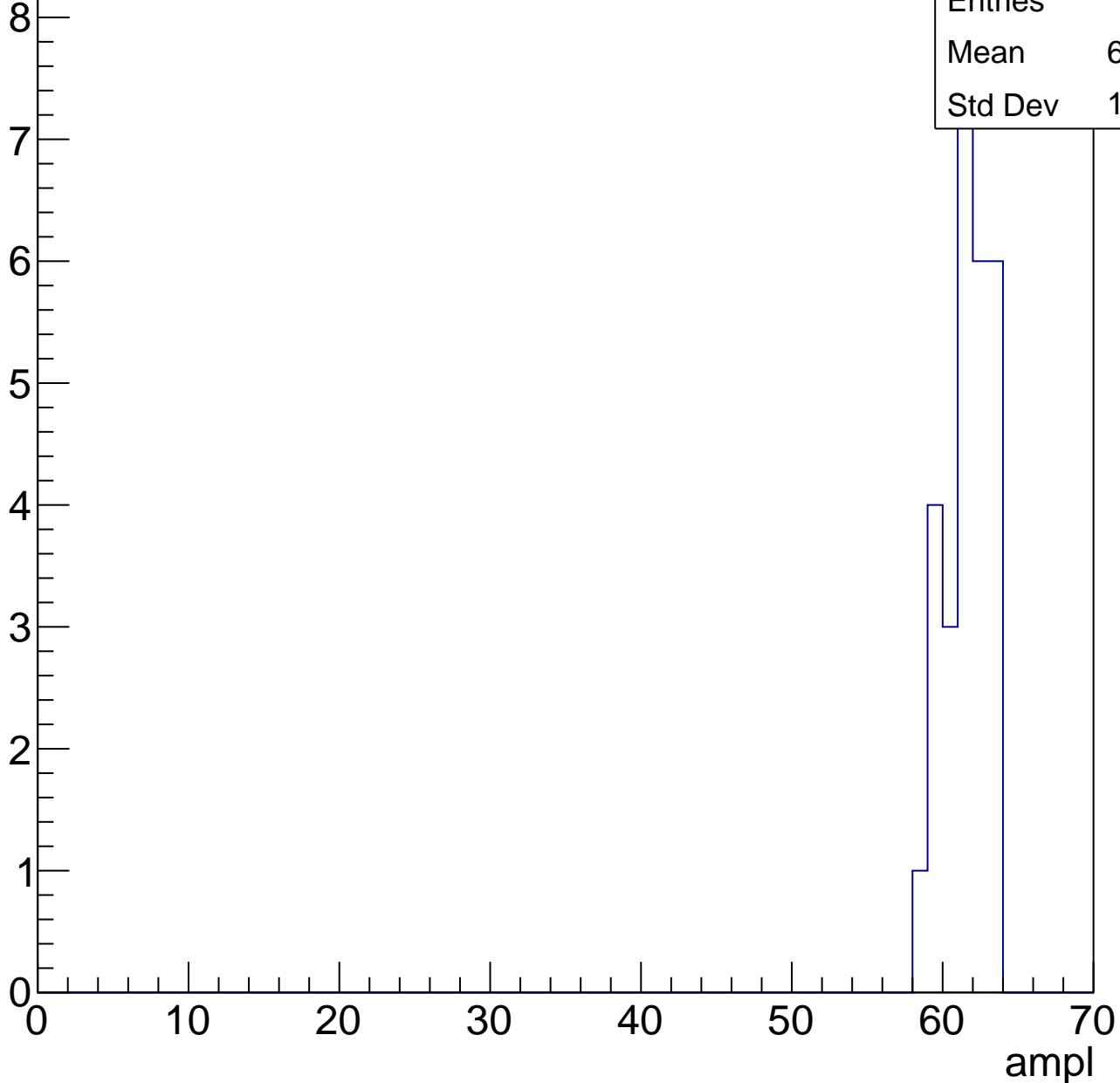


# B1L103S, U1-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	28
Mean	61.14
Std Dev	1.432

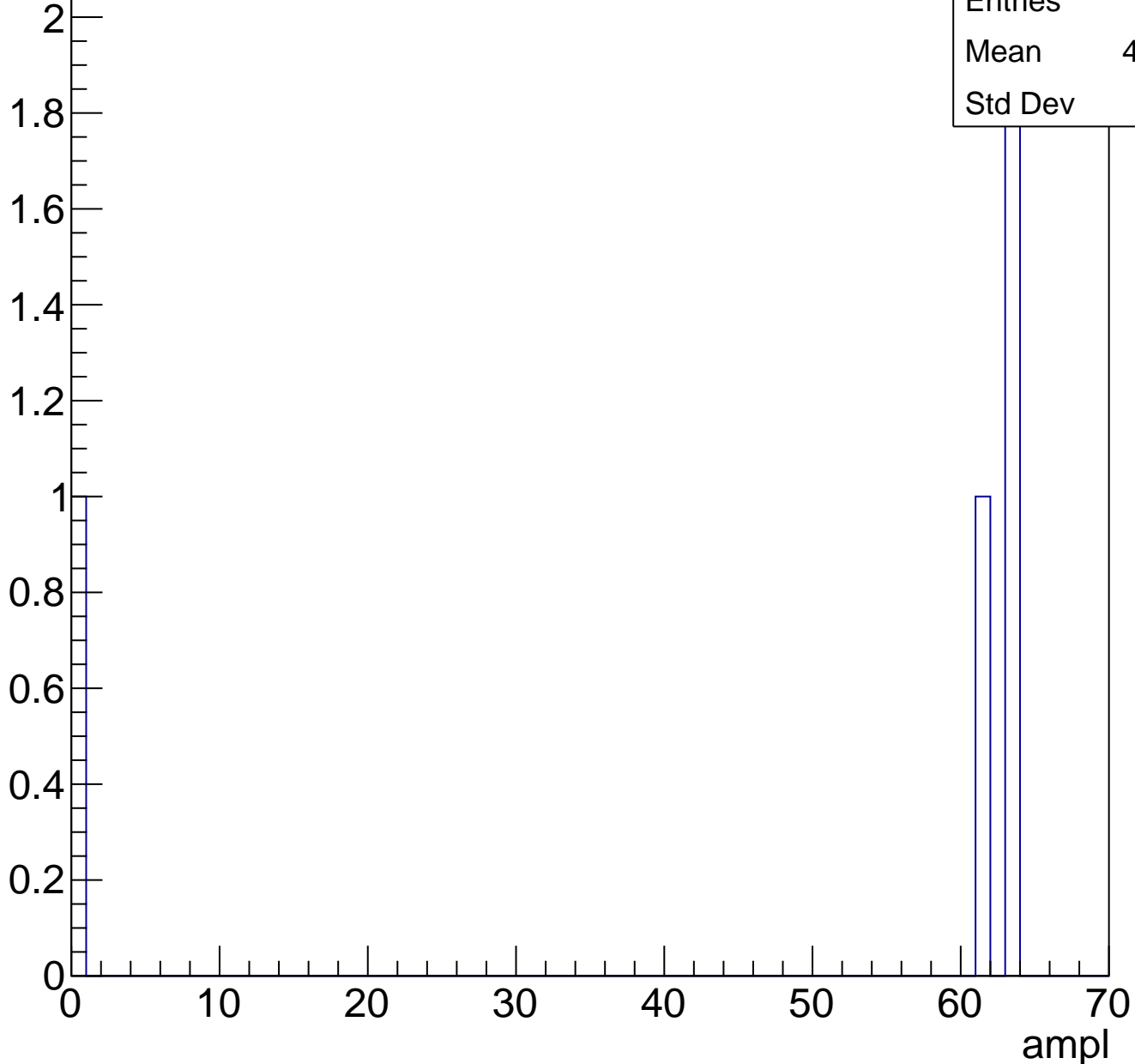




# B1L103S, U1-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	4
Mean	46.75
Std Dev	27

# B1L103S, U1-ch31, adc0

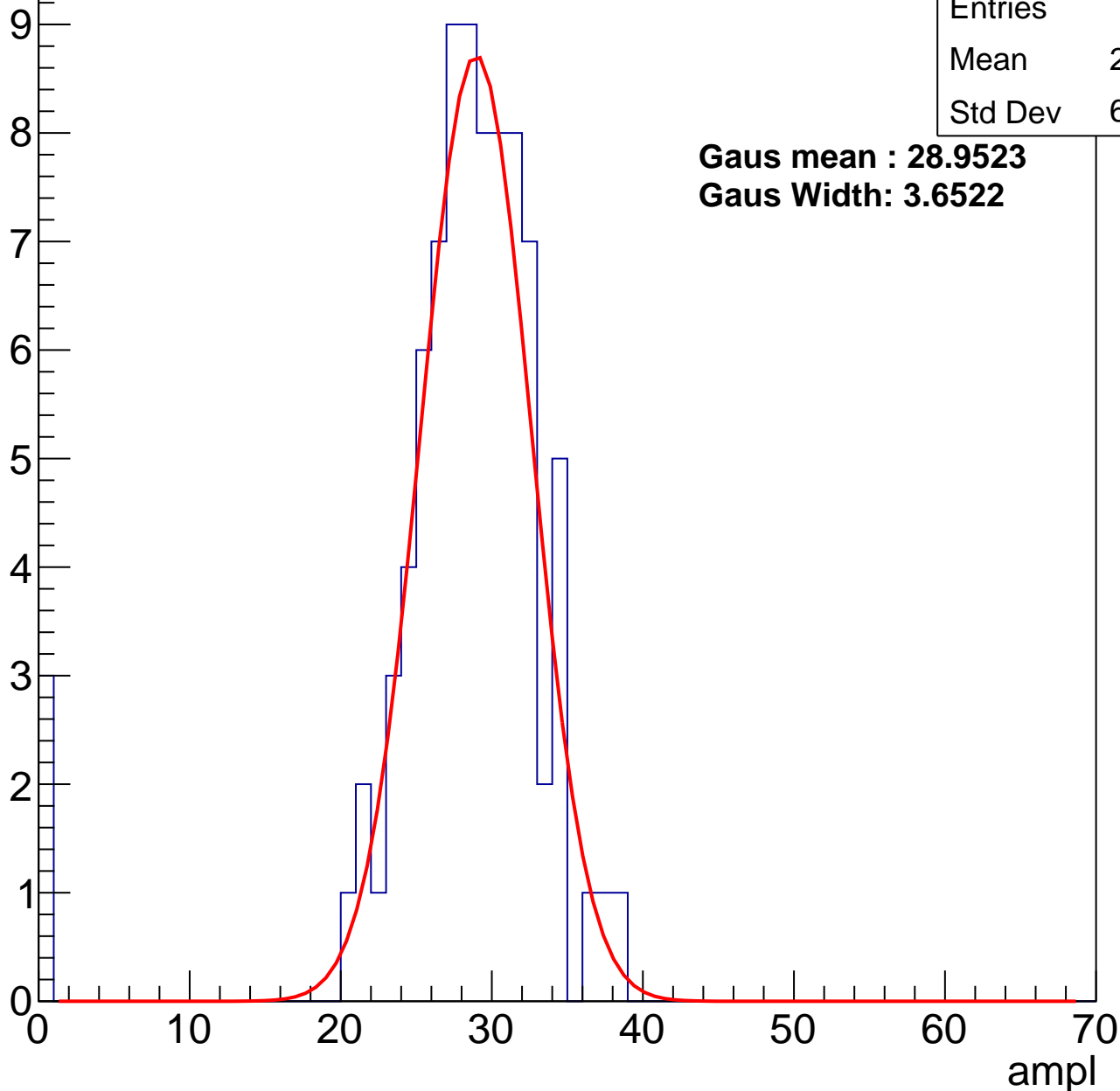
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	86
Mean	27.52
Std Dev	6.342

**Gaus mean : 28.9523**

**Gaus Width: 3.6522**



# B1L103S, U1-ch31, adc1

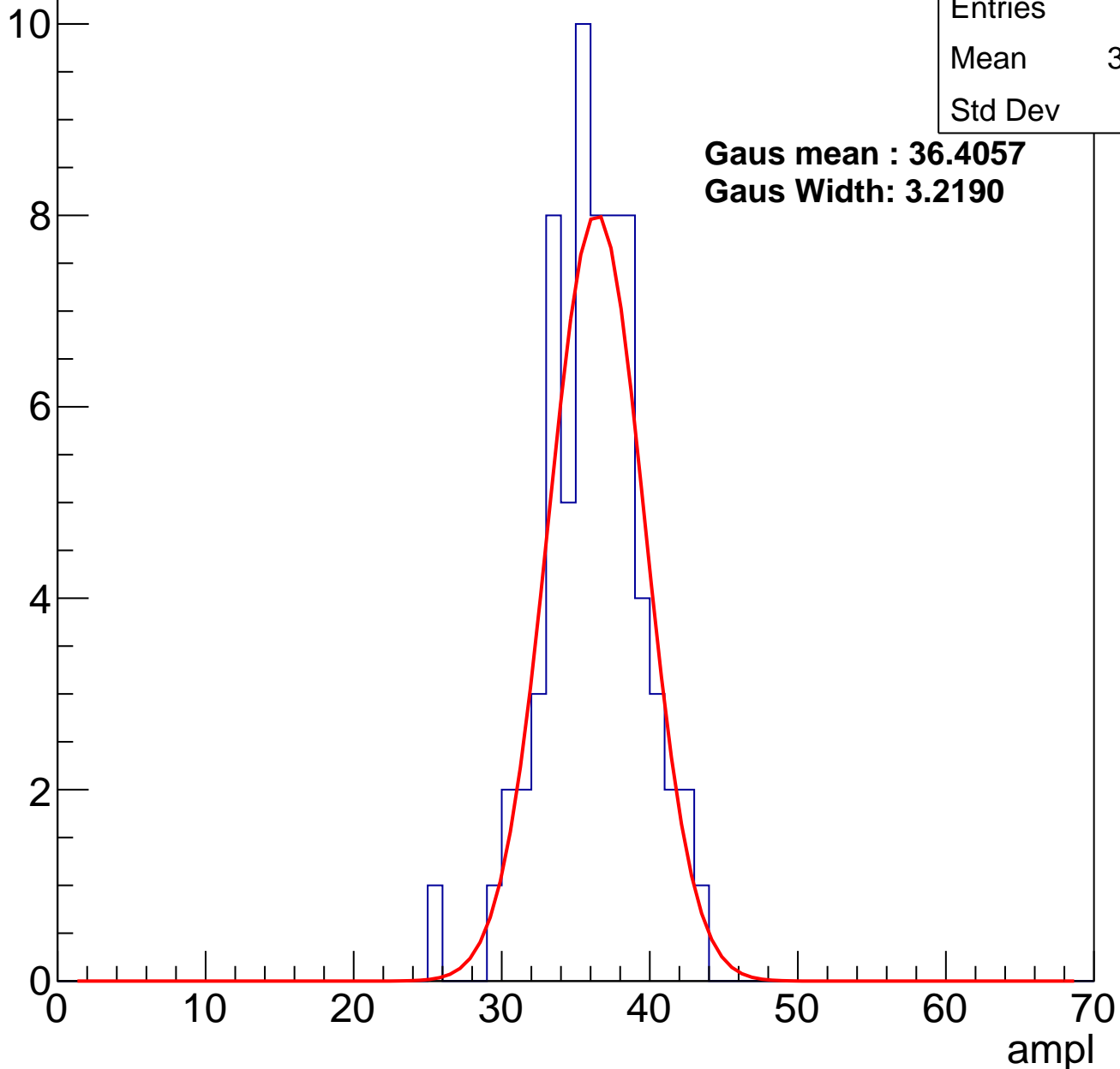
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	68
Mean	35.72
Std Dev	3.28

**Gaus mean : 36.4057**

**Gaus Width: 3.2190**

Entry



# B1L103S, U1-ch31, adc2

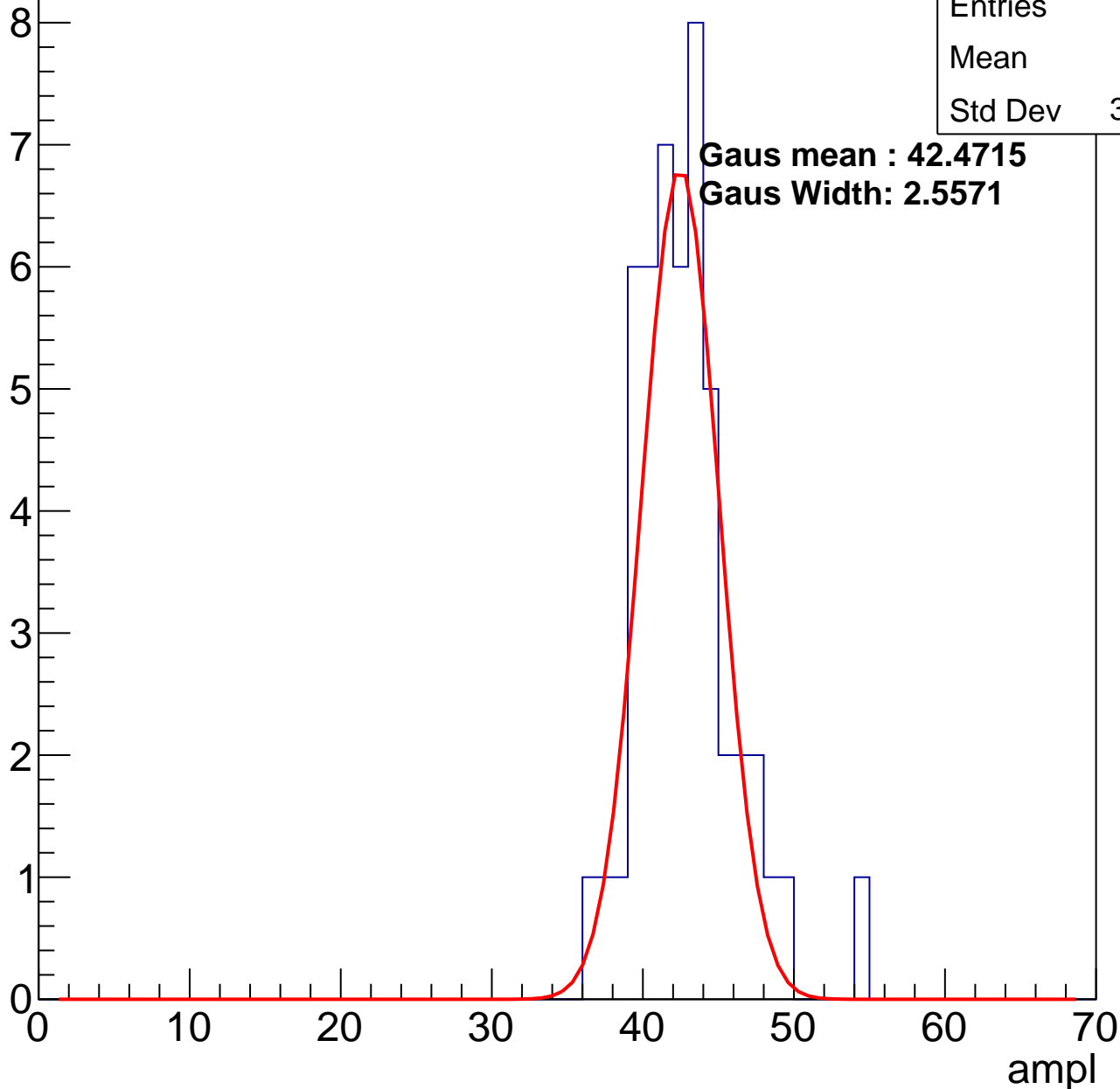
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	42.3
Std Dev	3.208

**Gaus mean : 42.4715**

**Gaus Width: 2.5571**

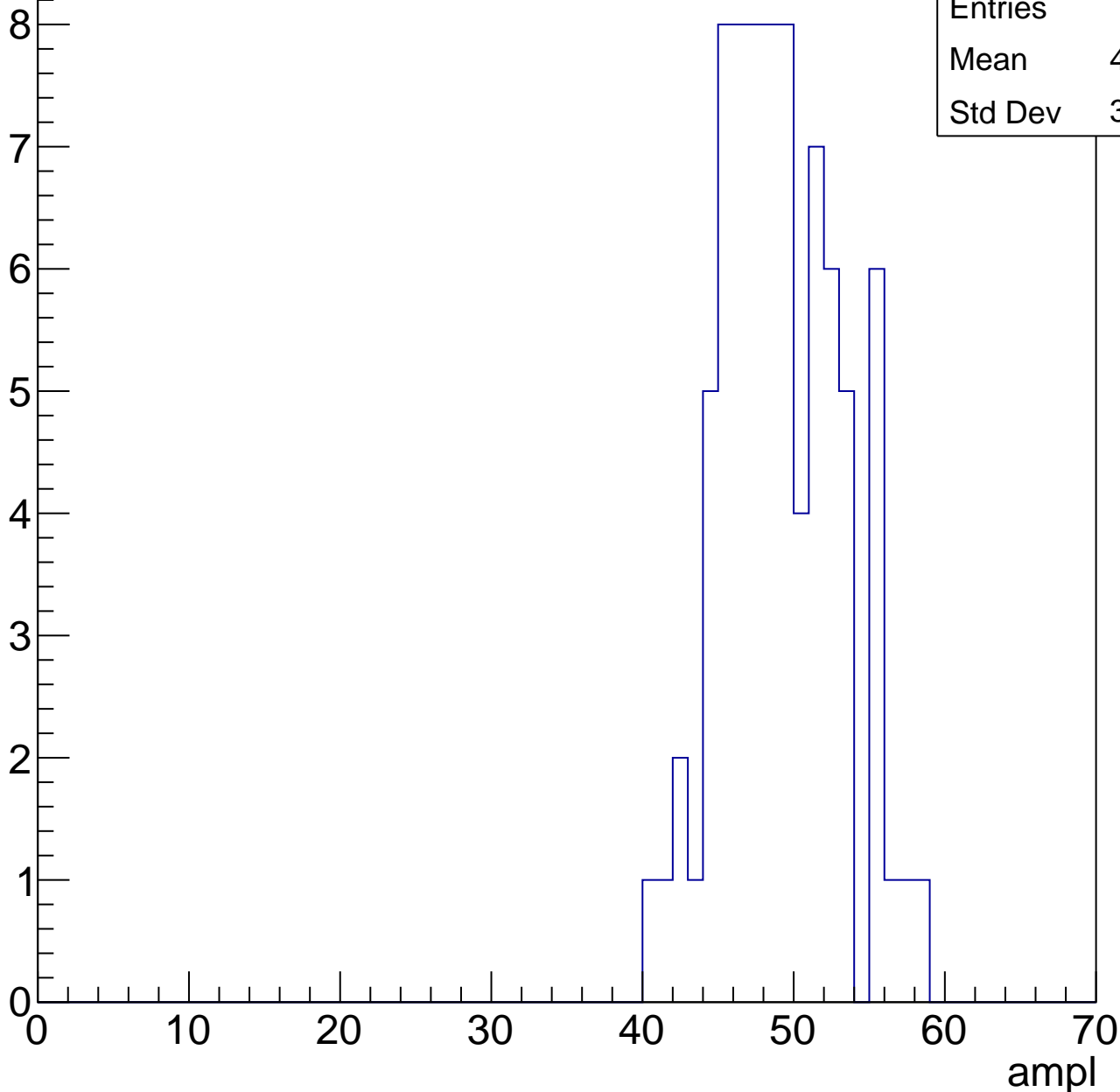


# B1L103S, U1-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

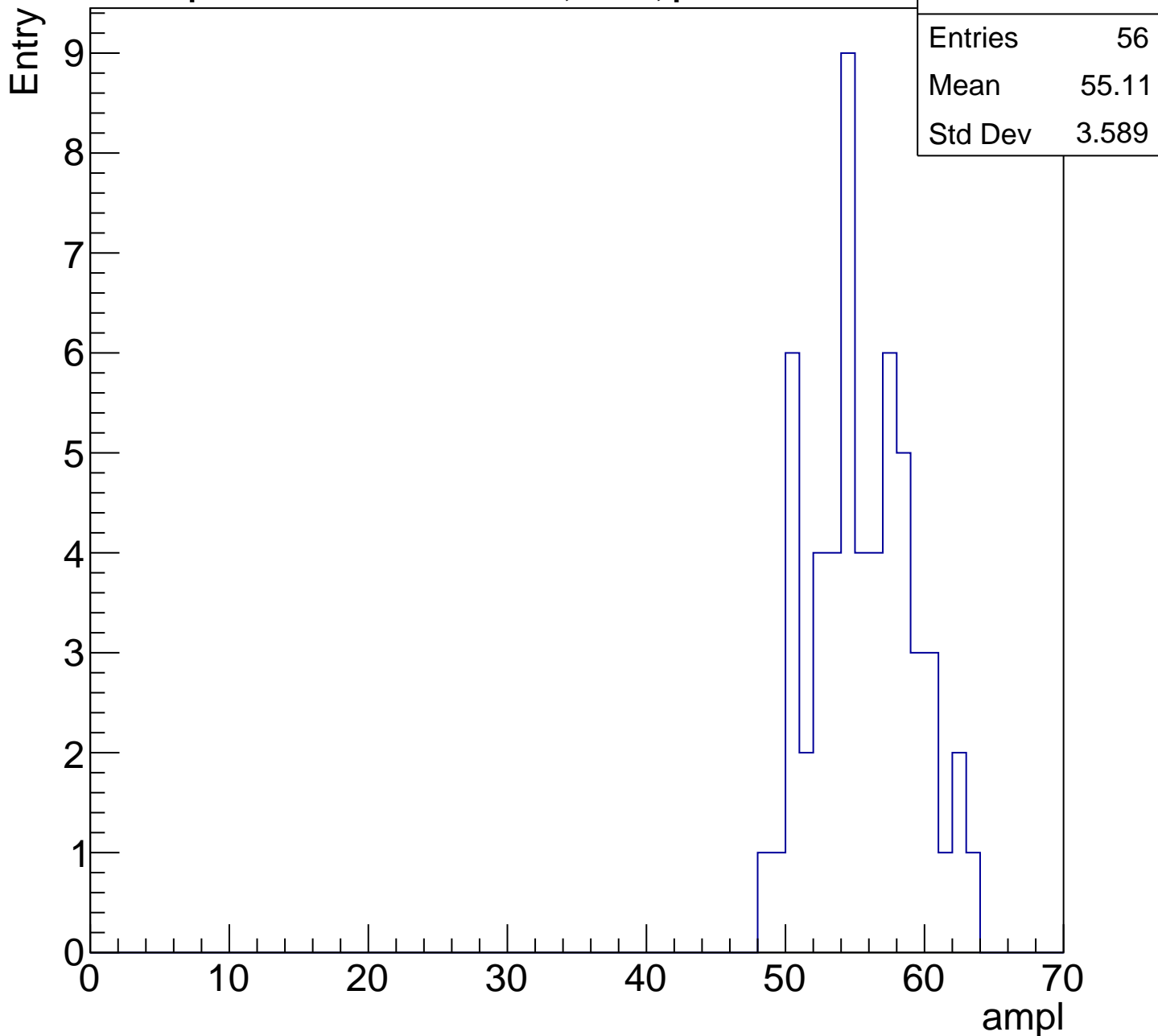
Entry

Entries	81
Mean	48.68
Std Dev	3.868



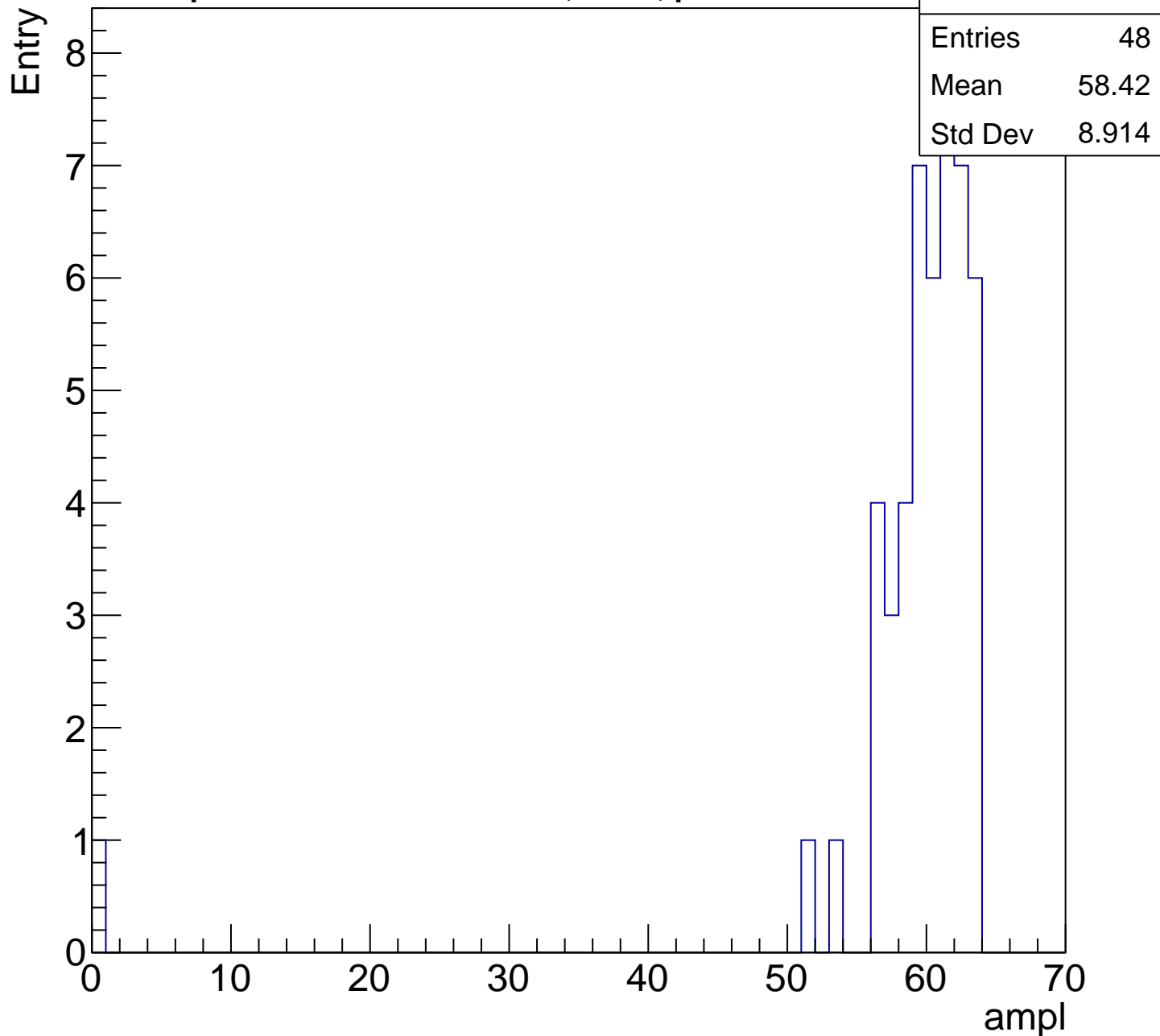
# B1L103S, U1-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U1-ch31, adc5

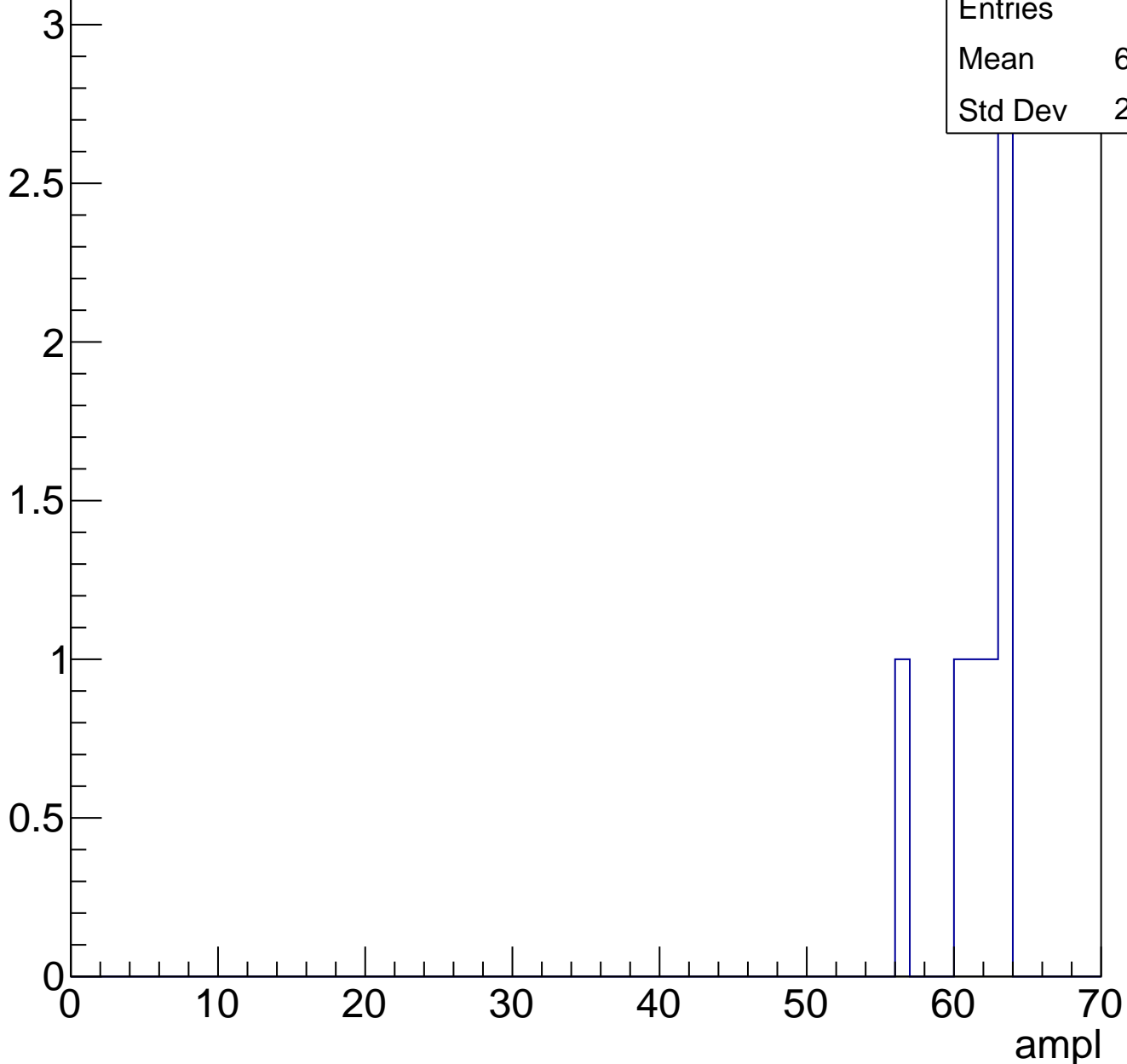
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U1-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U1-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U1-ch32, adc0

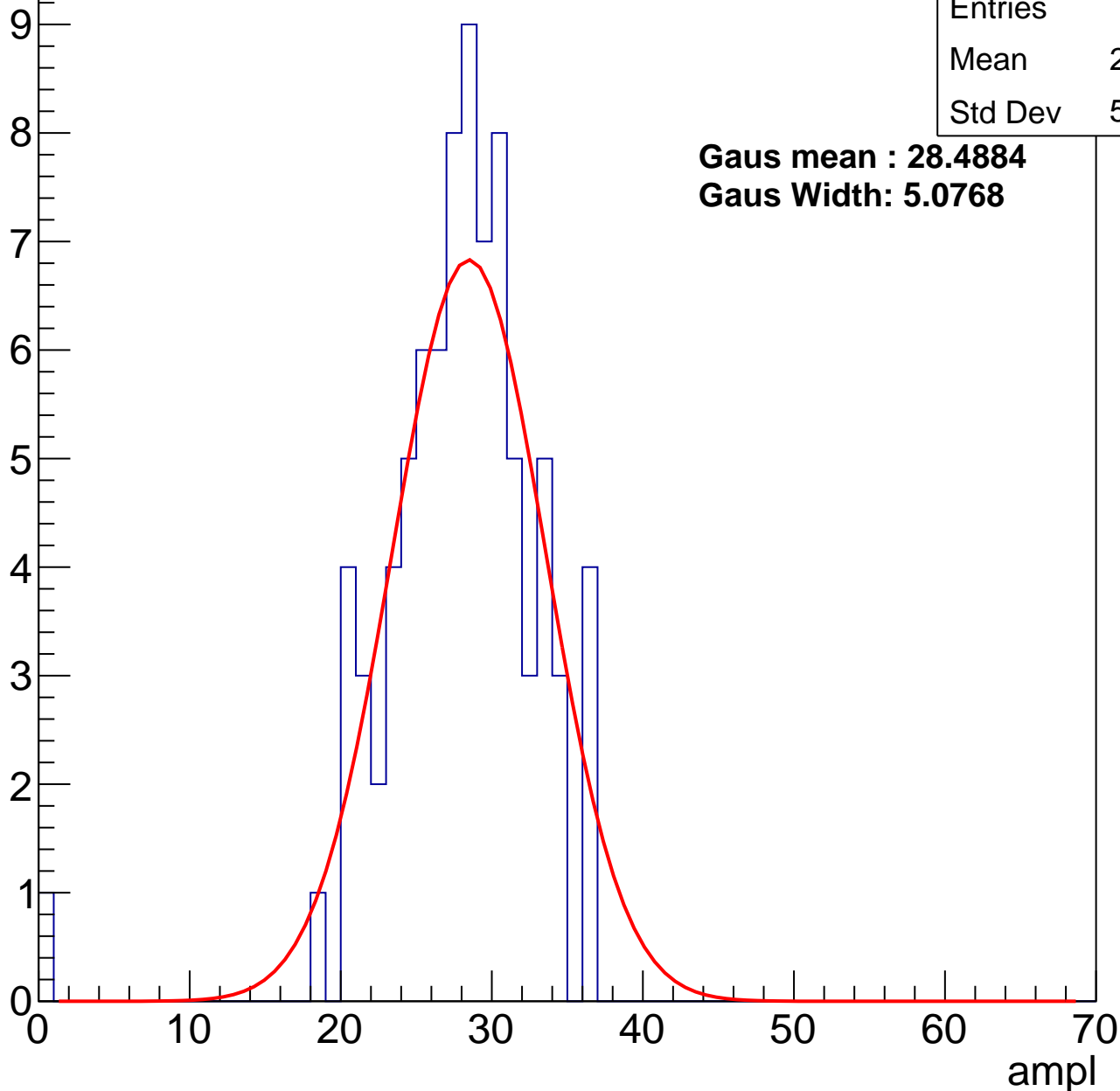
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	84
Mean	27.33
Std Dev	5.128

**Gaus mean : 28.4884**

**Gaus Width: 5.0768**



# B1L103S, U1-ch32, adc1

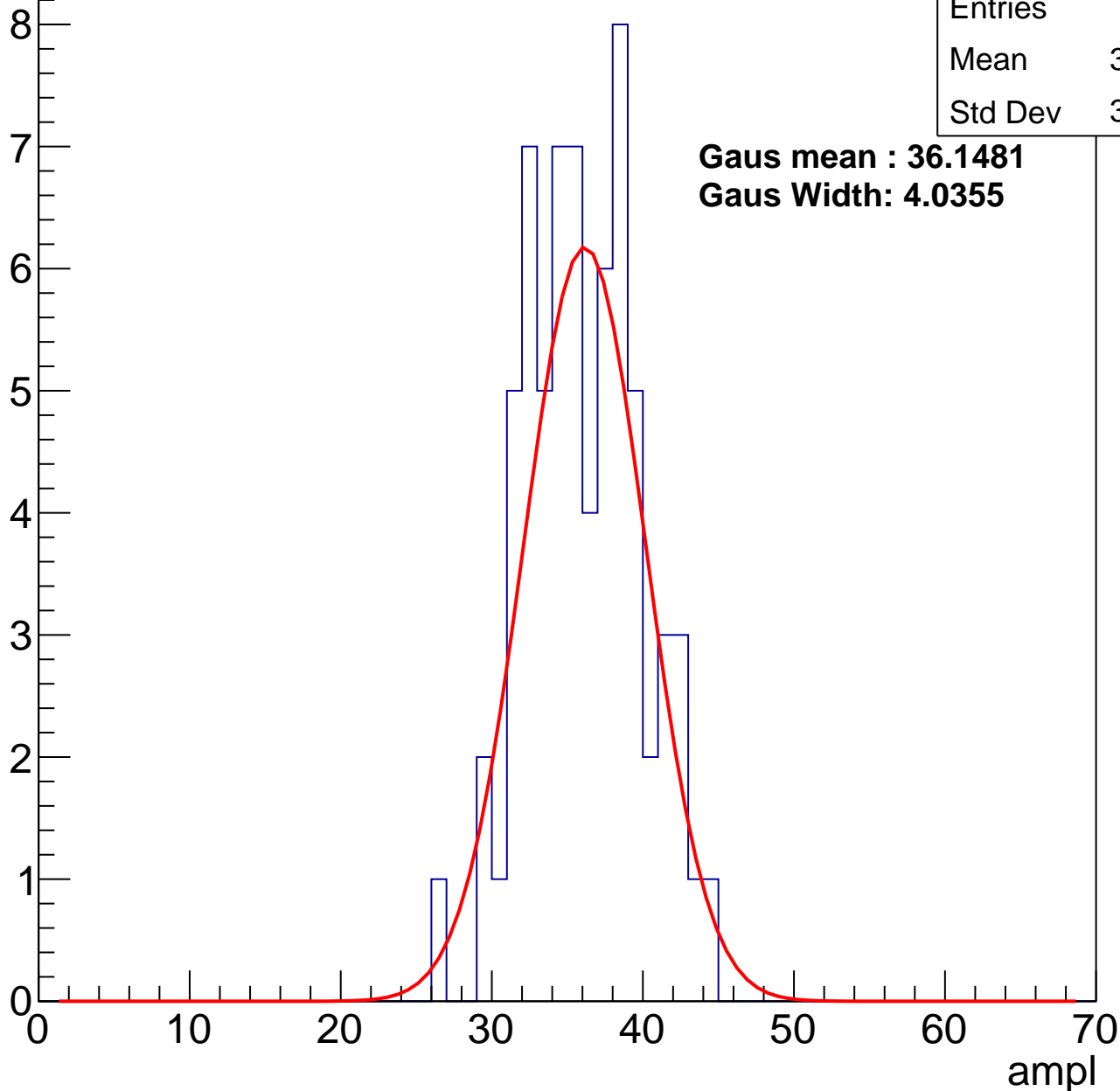
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	35.62
Std Dev	3.742

**Gaus mean : 36.1481**

**Gaus Width: 4.0355**



# B1L103S, U1-ch32, adc2

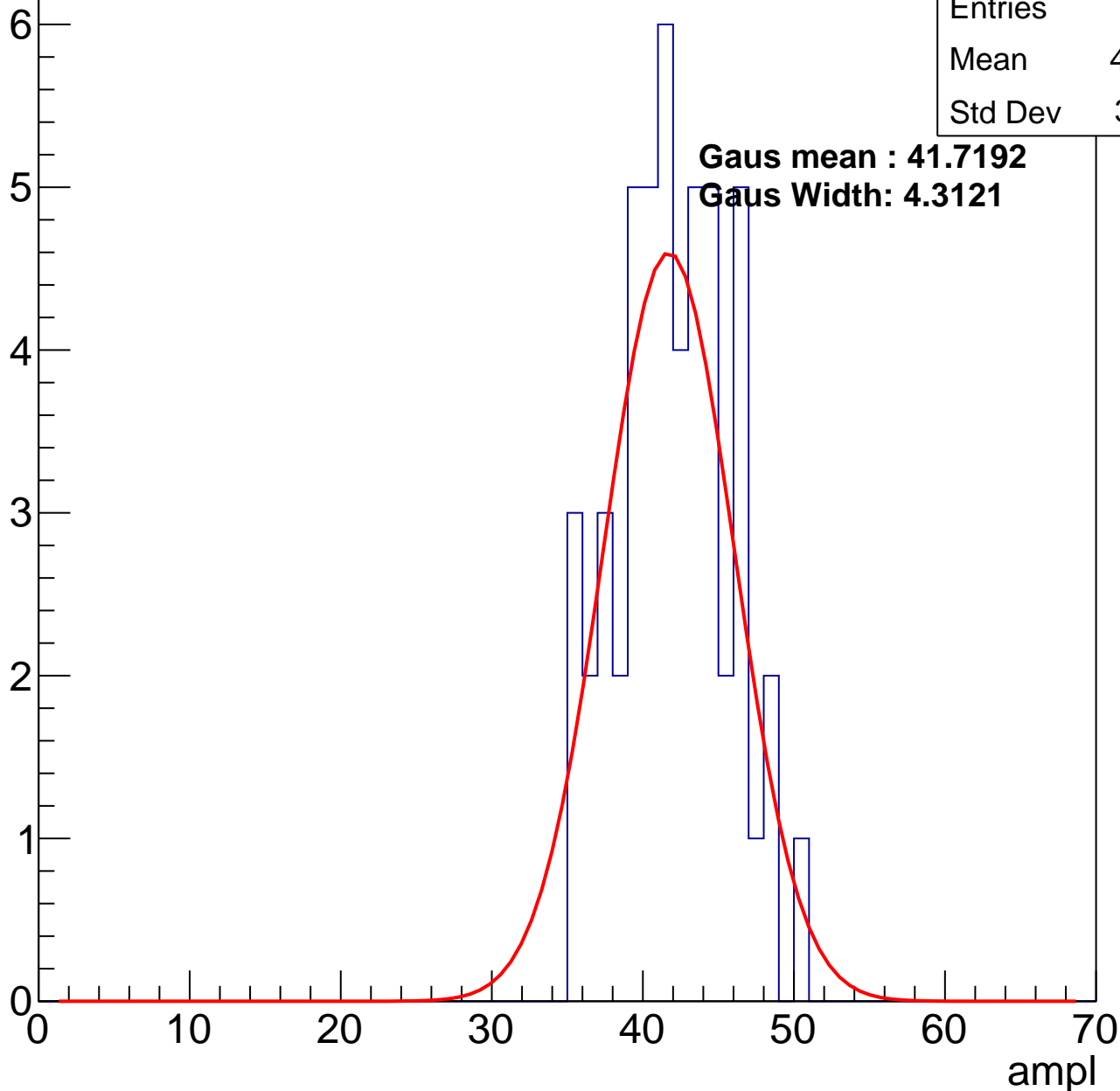
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	41.59
Std Dev	3.631

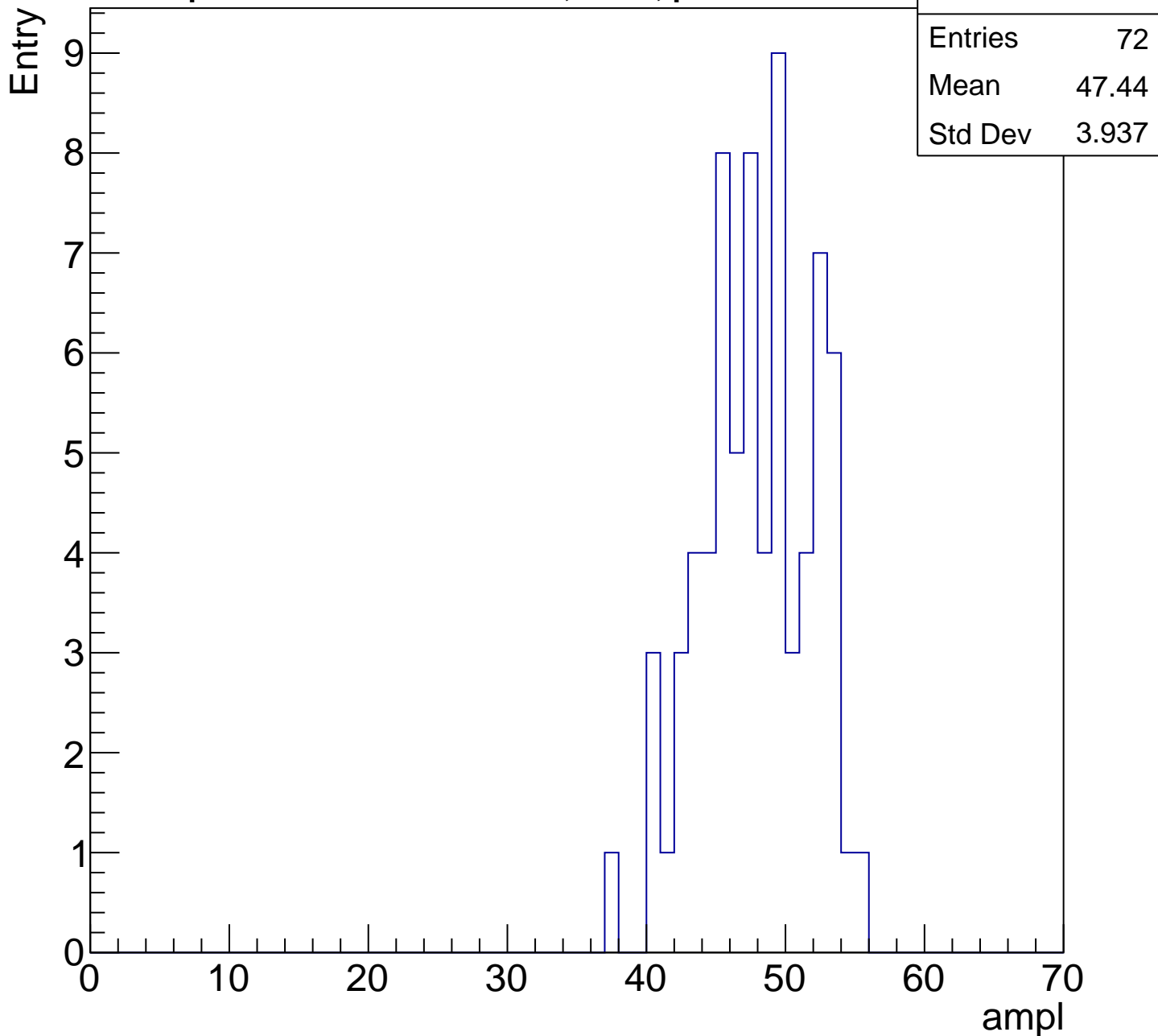
**Gaus mean : 41.7192**

**Gaus Width: 4.3121**



# B1L103S, U1-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

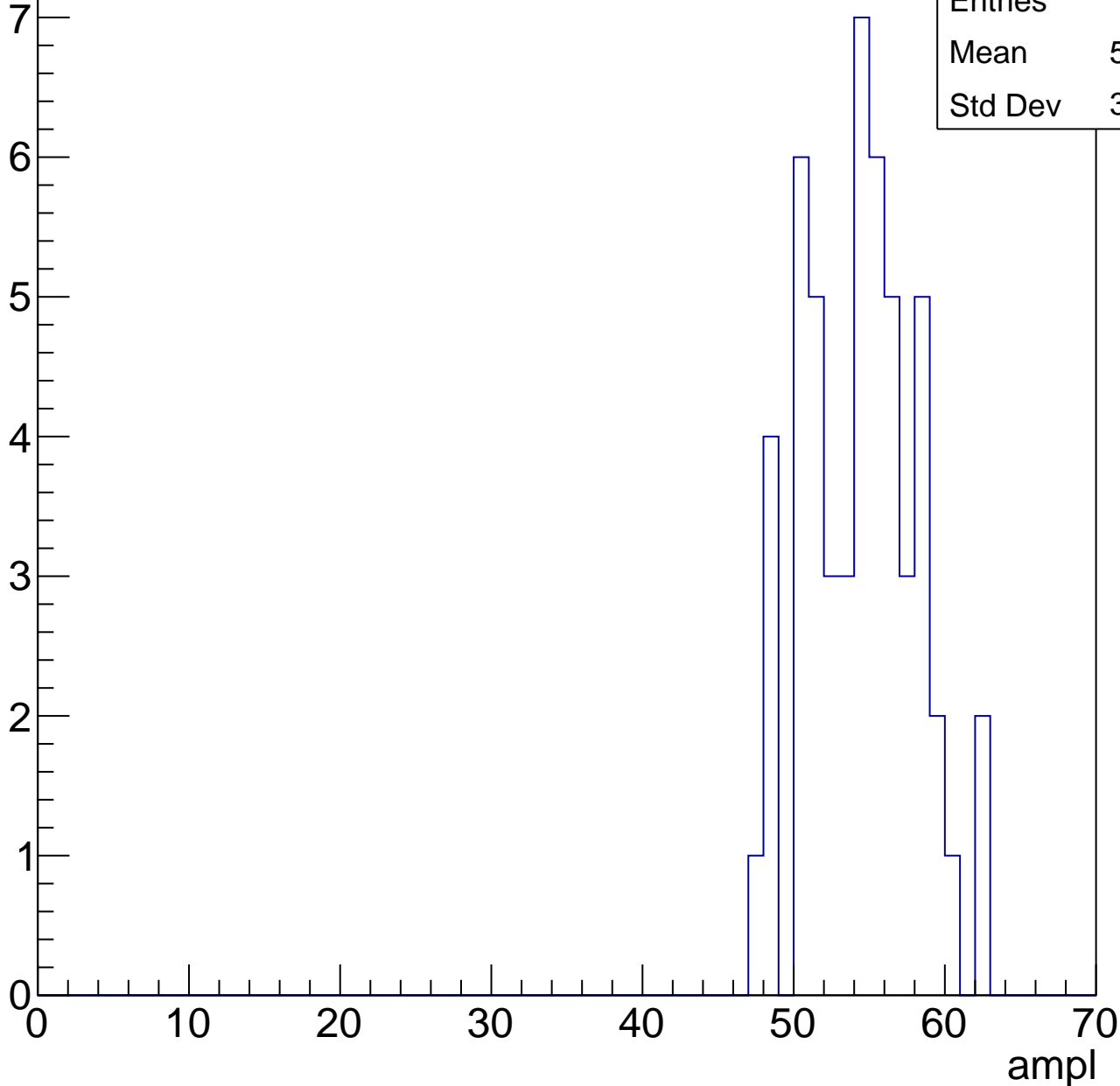


# B1L103S, U1-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

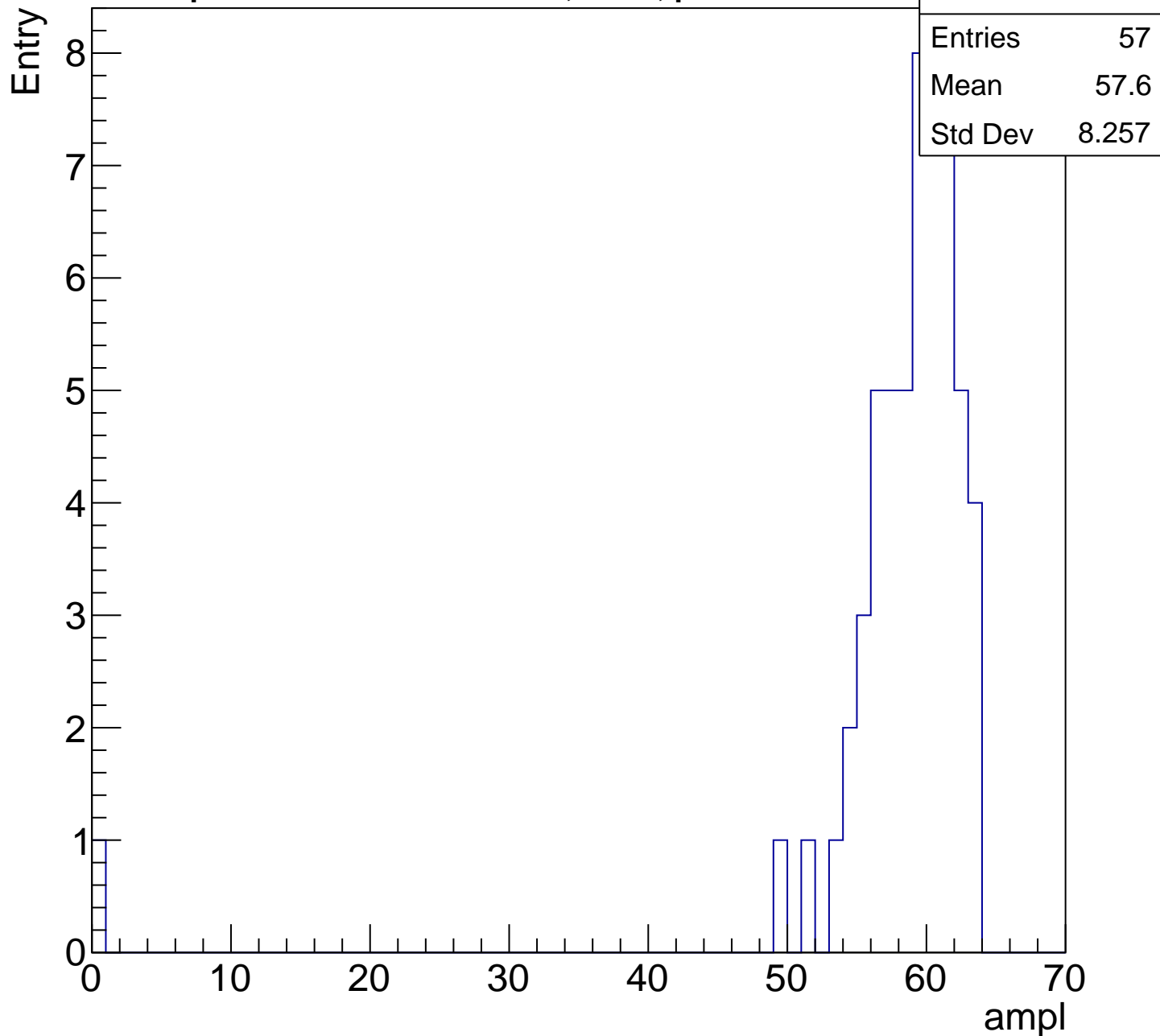
Entry

Entries	53
Mean	53.96
Std Dev	3.624



# B1L103S, U1-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

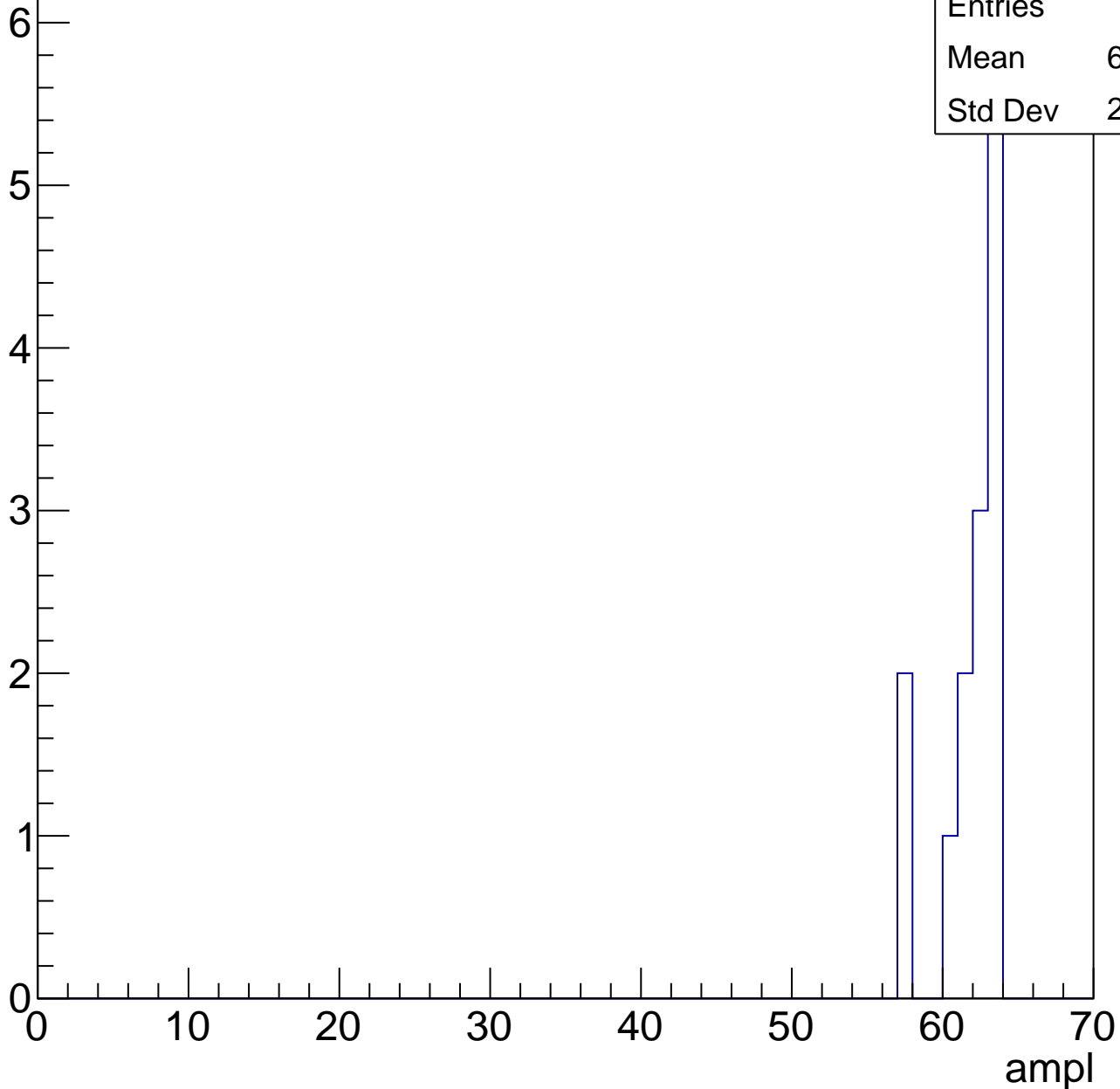


# B1L103S, U1-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	14
Mean	61.43
Std Dev	2.025





# B1L103S, U1-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U1-ch33, adc0

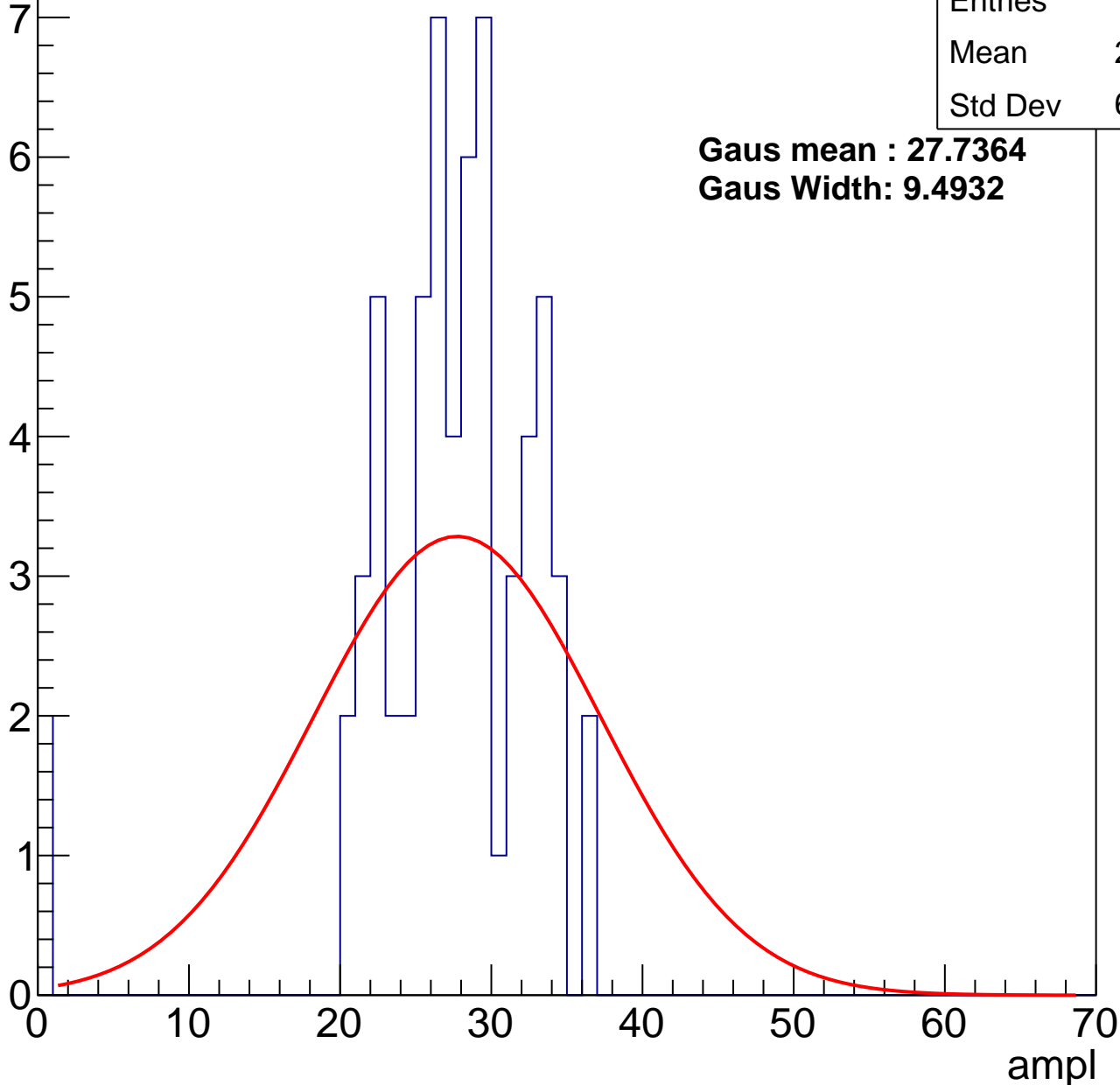
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	26.71
Std Dev	6.351

**Gaus mean : 27.7364**

**Gaus Width: 9.4932**



# B1L103S, U1-ch33, adc1

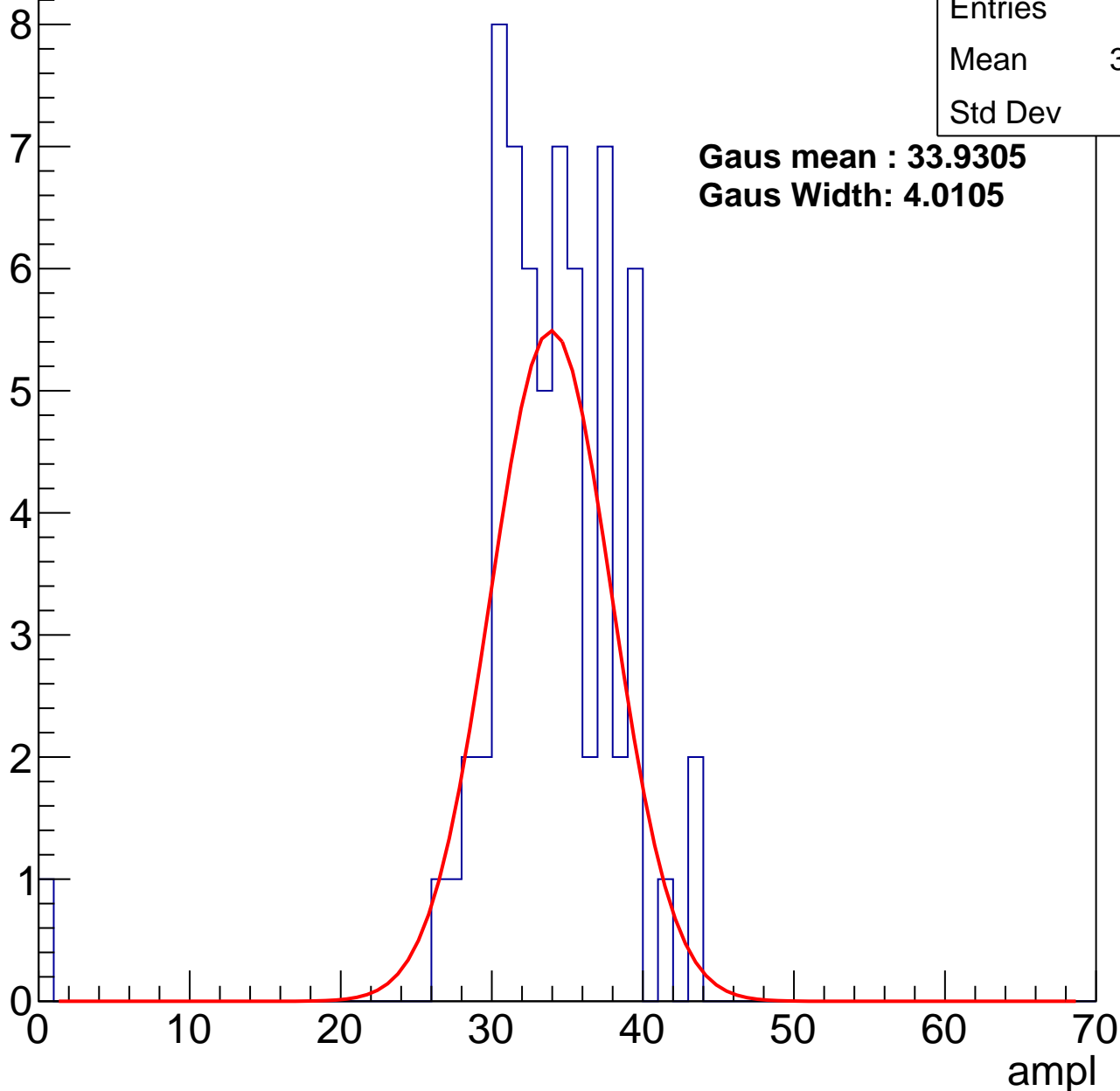
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	33.29
Std Dev	5.57

**Gaus mean : 33.9305**

**Gaus Width: 4.0105**



# B1L103S, U1-ch33, adc2

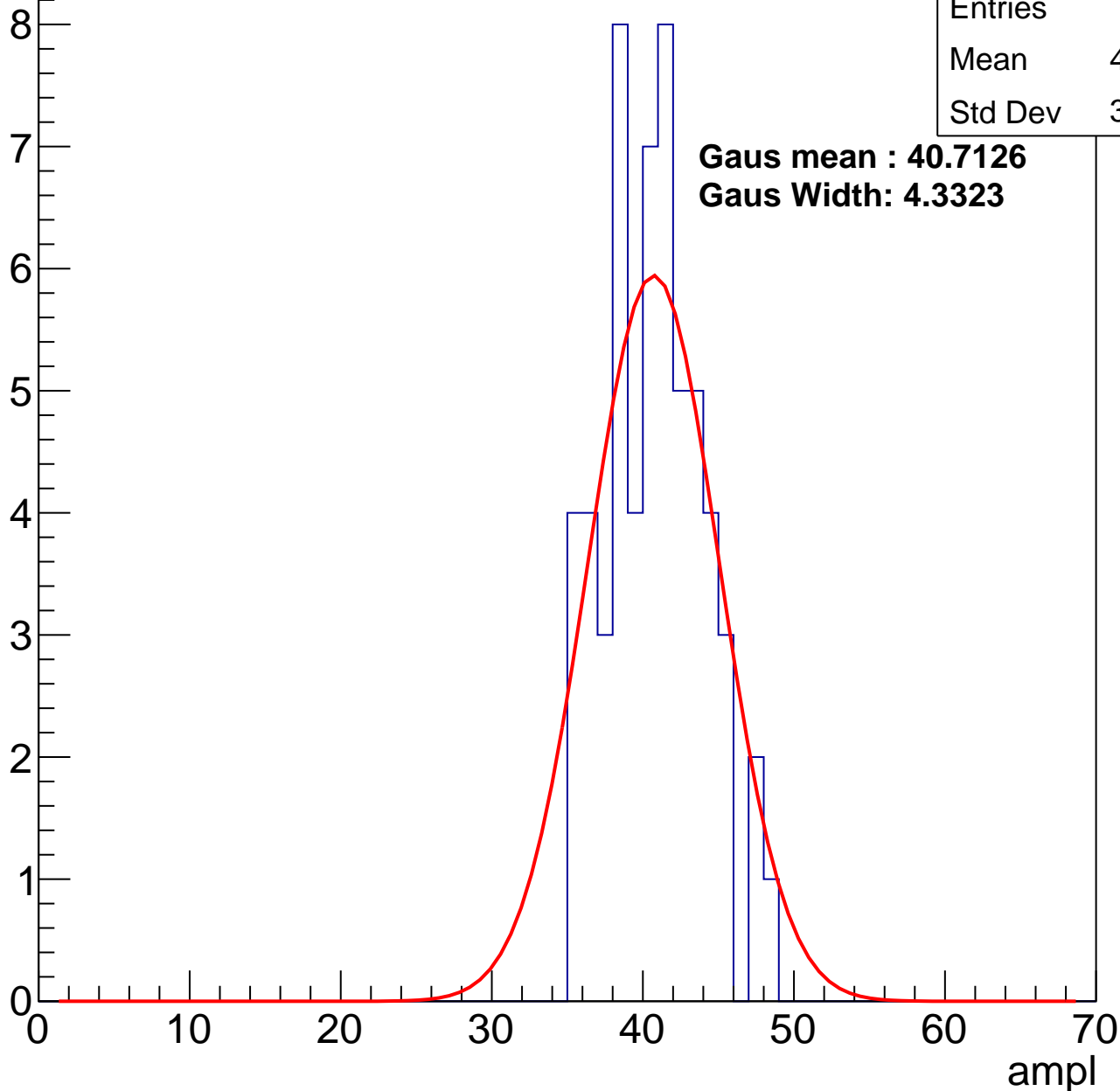
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	40.36
Std Dev	3.199

**Gaus mean : 40.7126**

**Gaus Width: 4.3323**

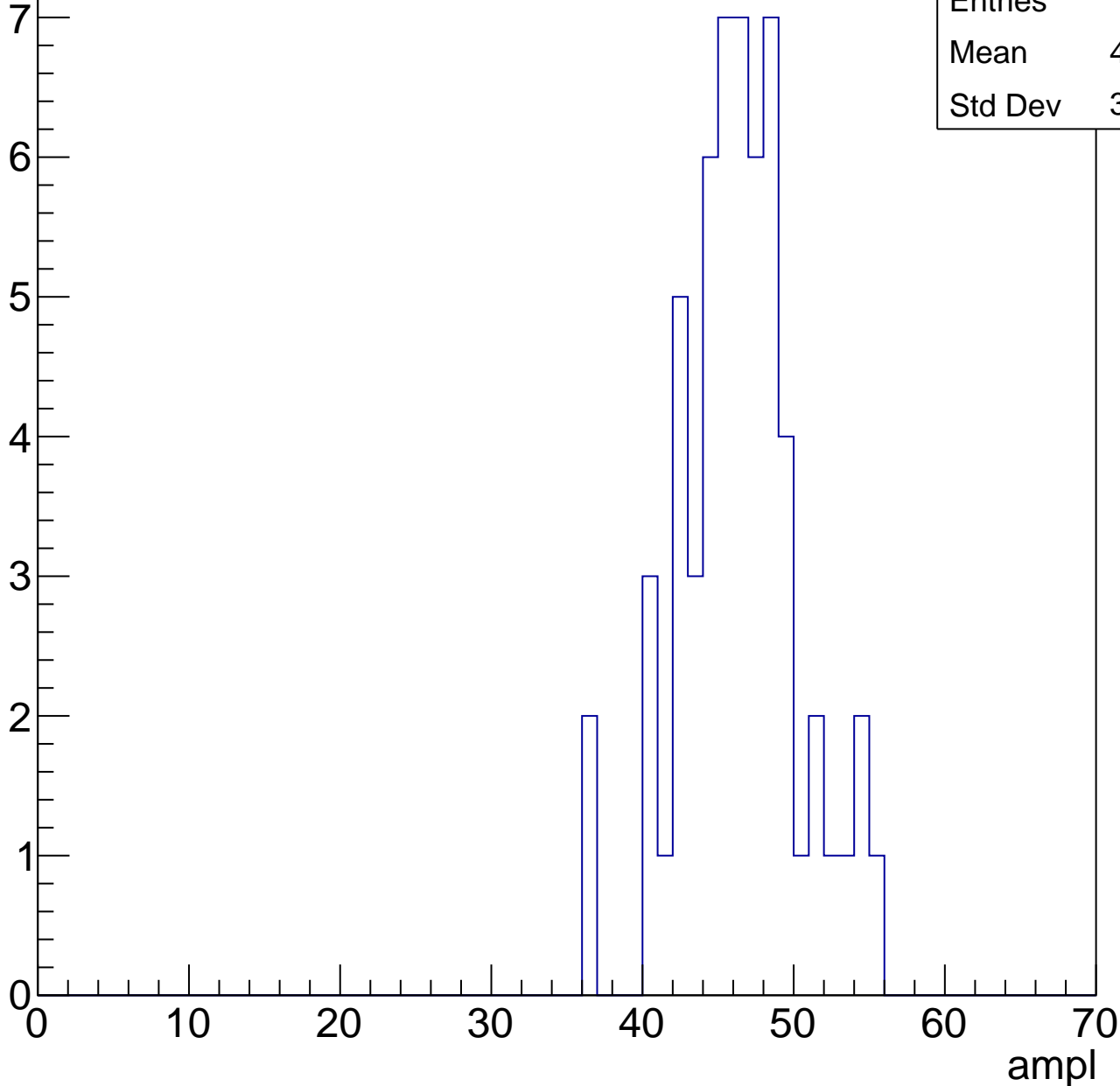


# B1L103S, U1-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	45.88
Std Dev	3.906

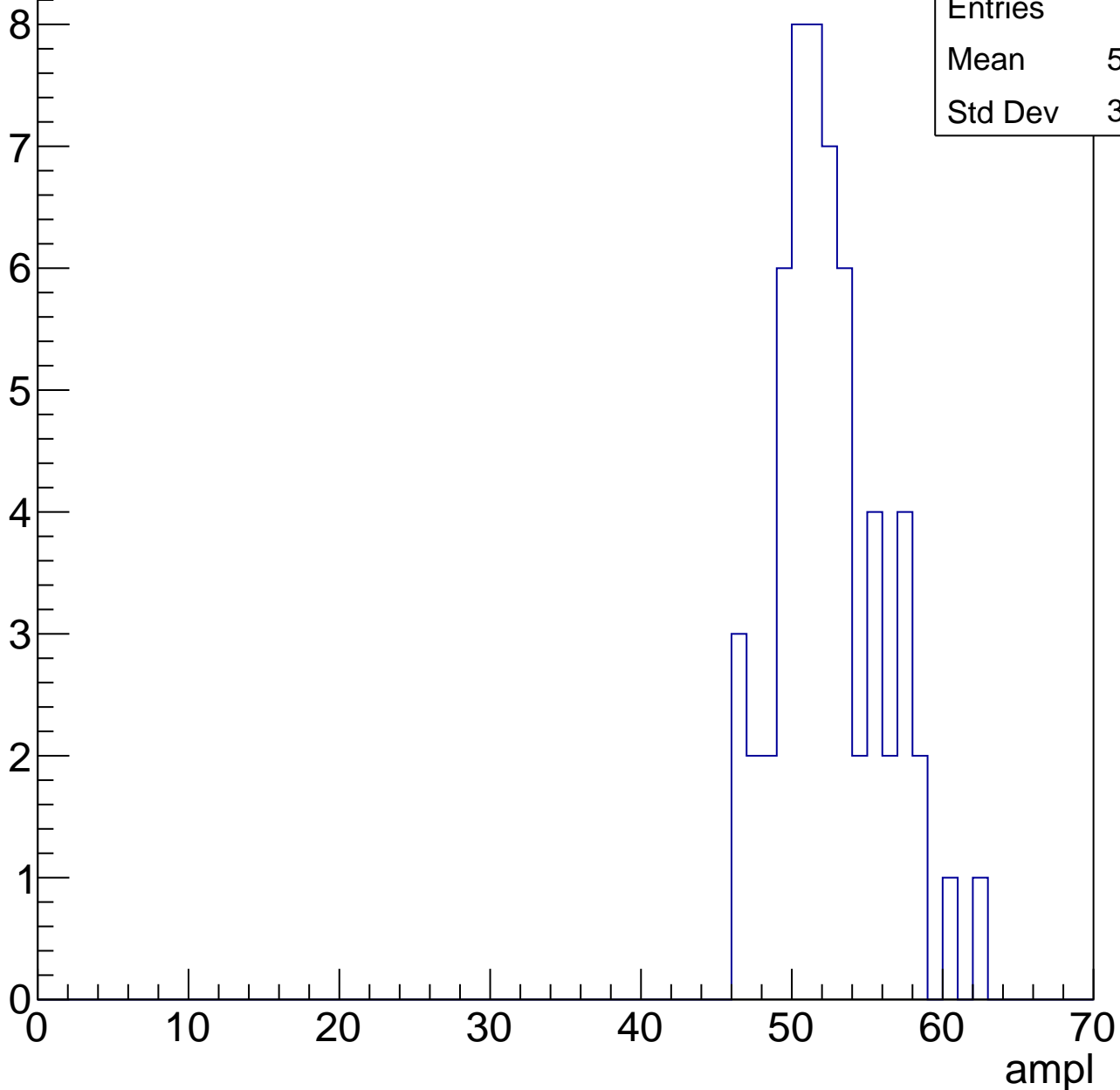


# B1L103S, U1-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	52.03
Std Dev	3.479

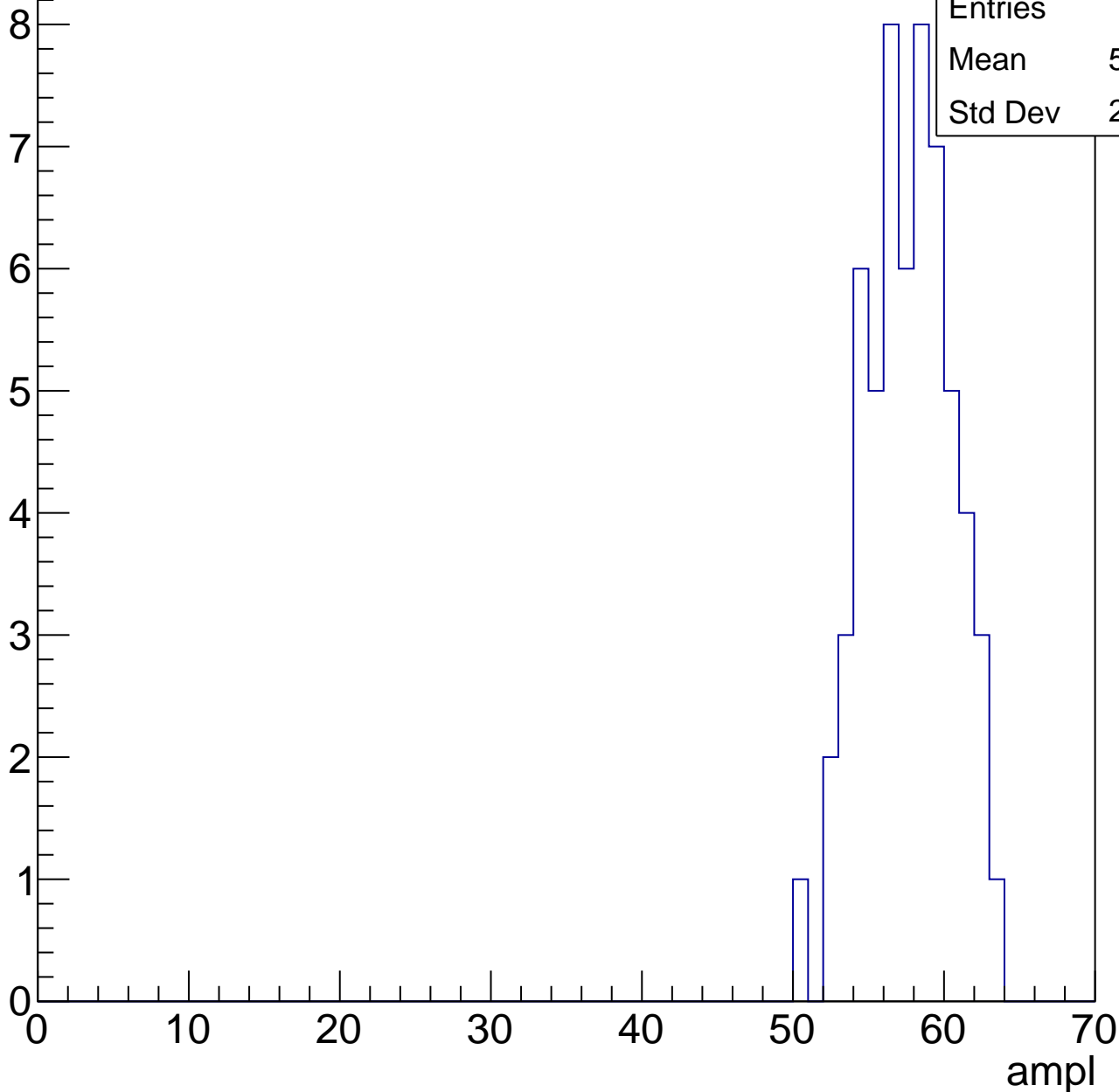


# B1L103S, U1-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	57.15
Std Dev	2.863

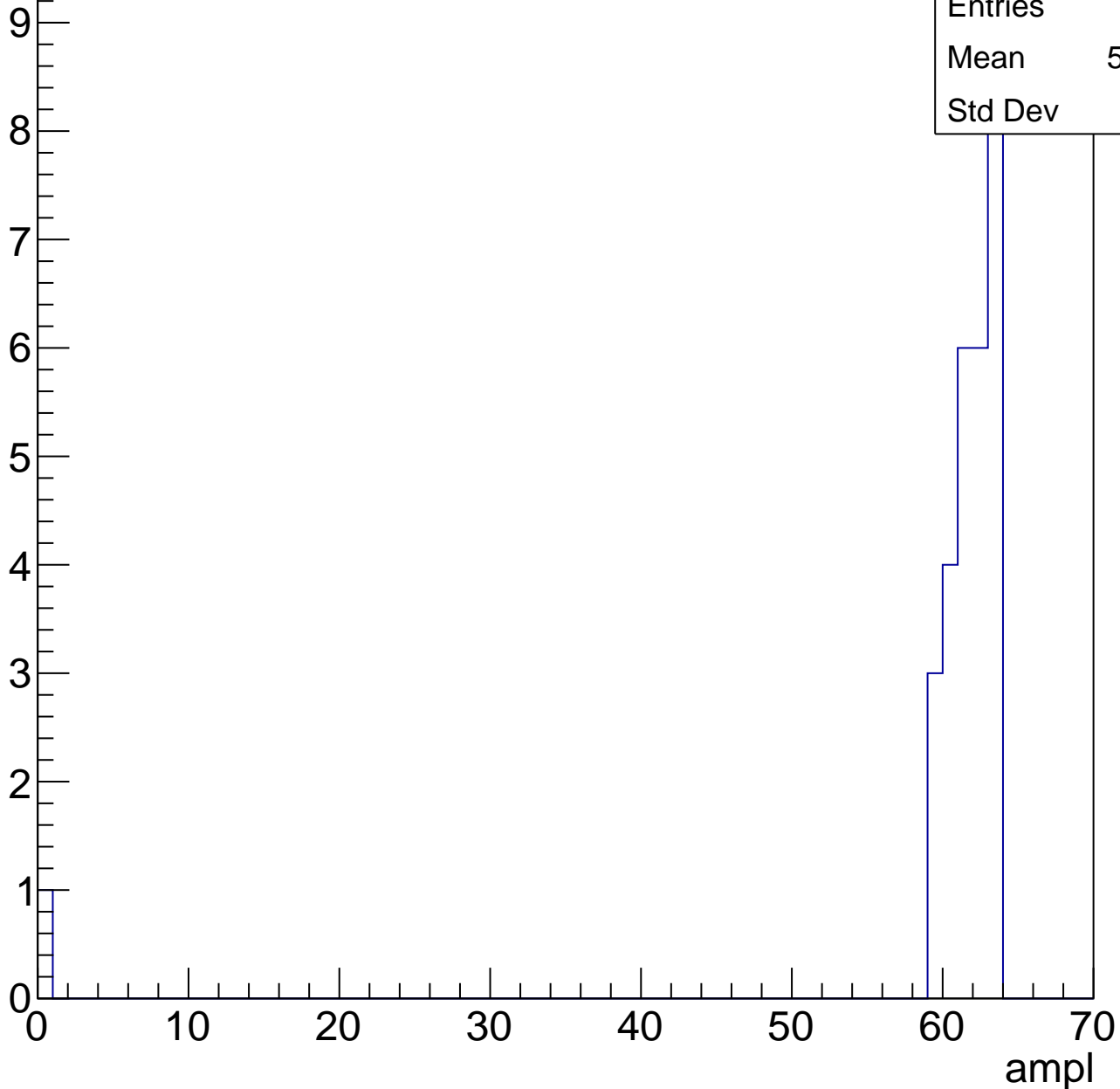


# B1L103S, U1-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	29
Mean	59.38
Std Dev	11.3

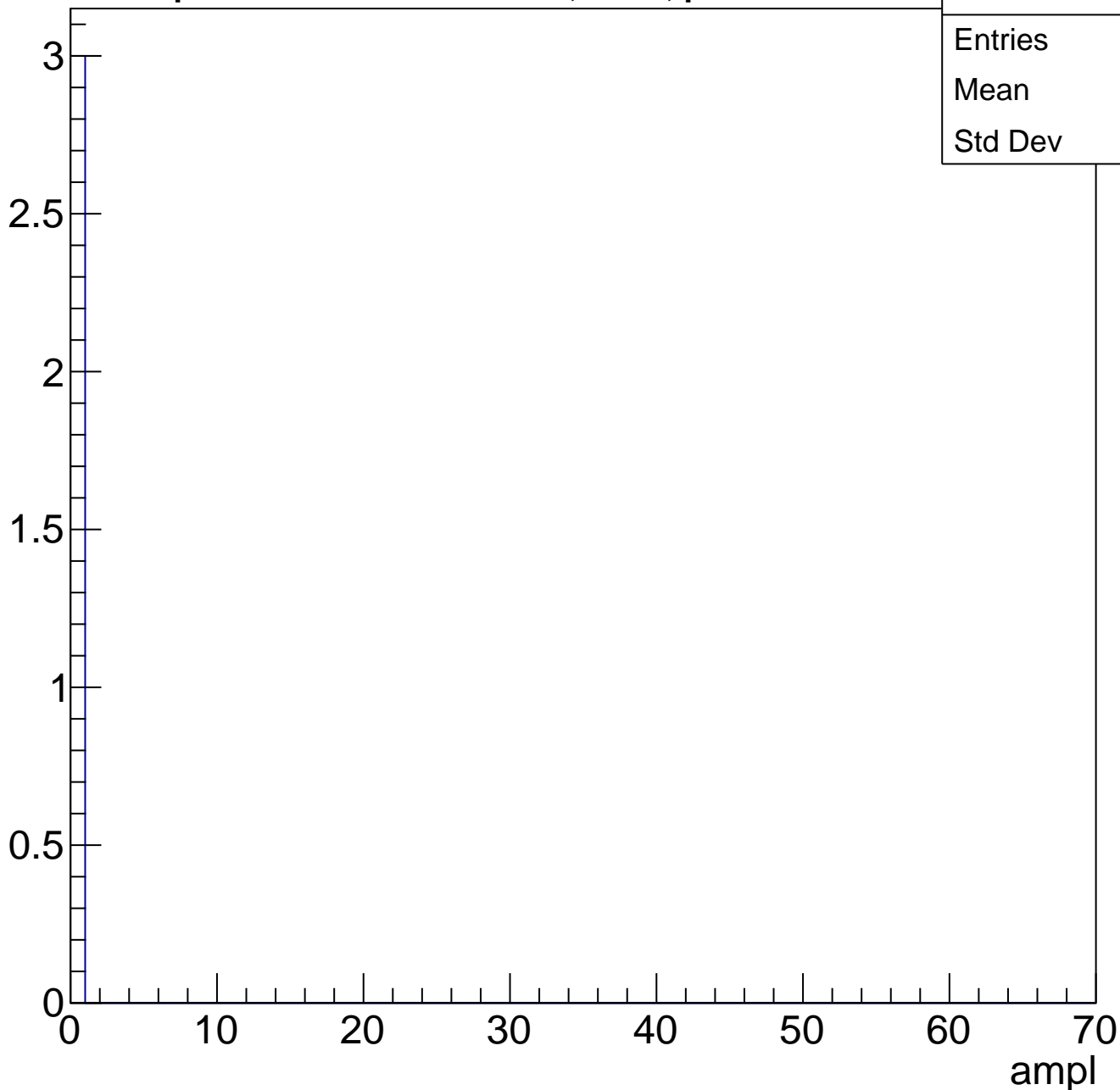




# B1L103S, U1-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L103S, U1-ch34, adc0

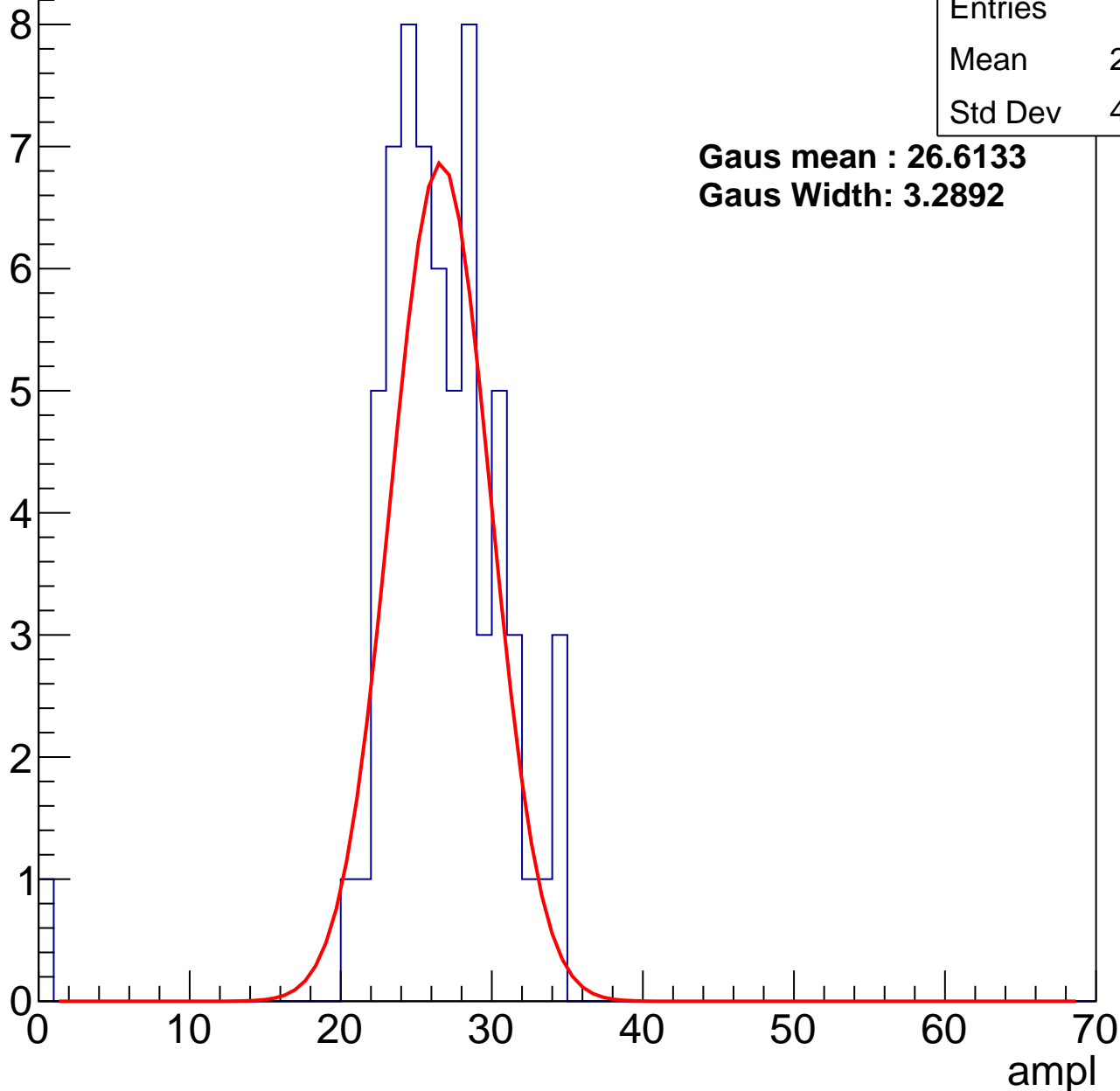
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	26.02
Std Dev	4.666

**Gaus mean : 26.6133**

**Gaus Width: 3.2892**



# B1L103S, U1-ch34, adc1

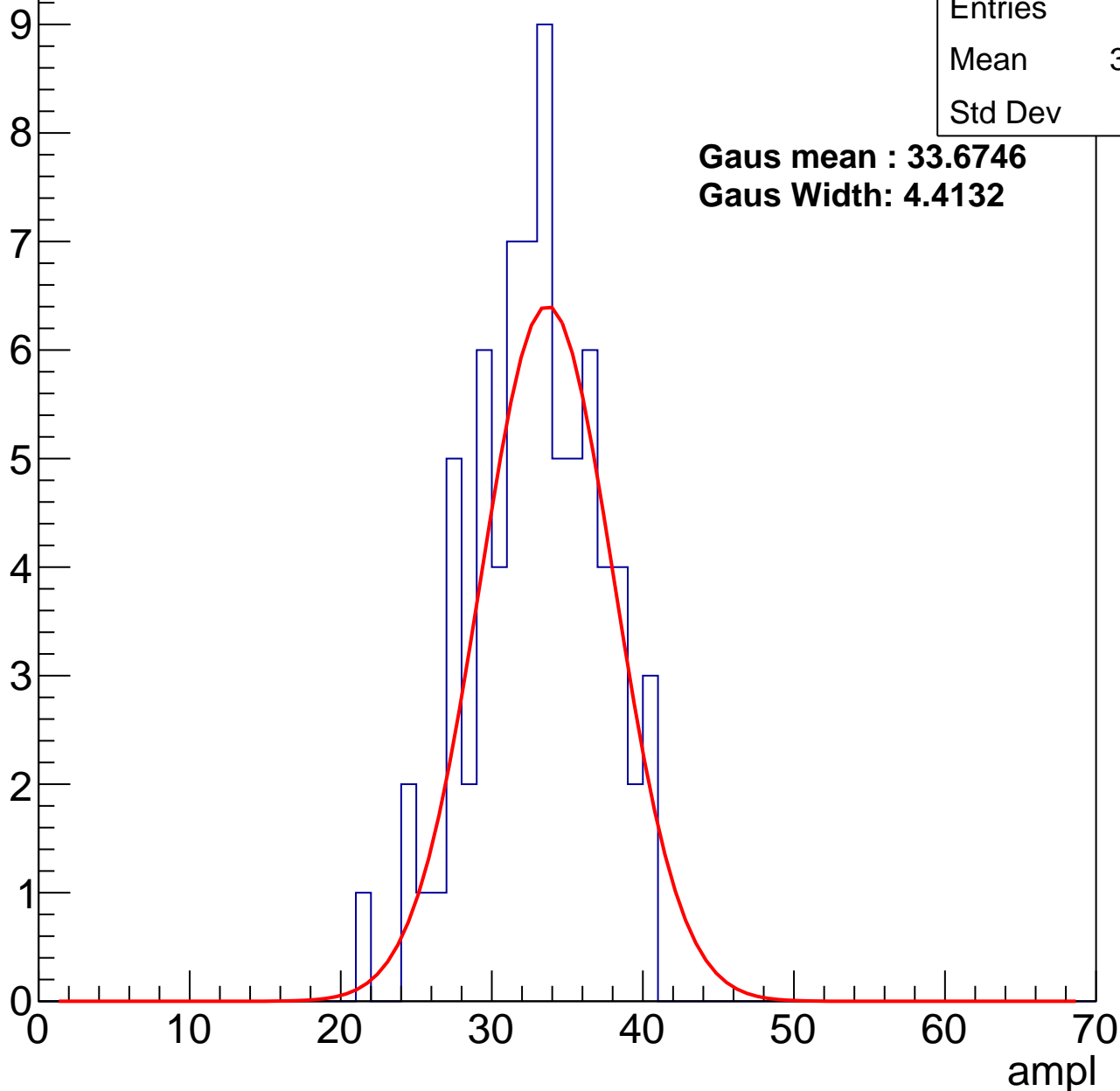
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	32.46
Std Dev	4.12

**Gaus mean : 33.6746**

**Gaus Width: 4.4132**



# B1L103S, U1-ch34, adc2

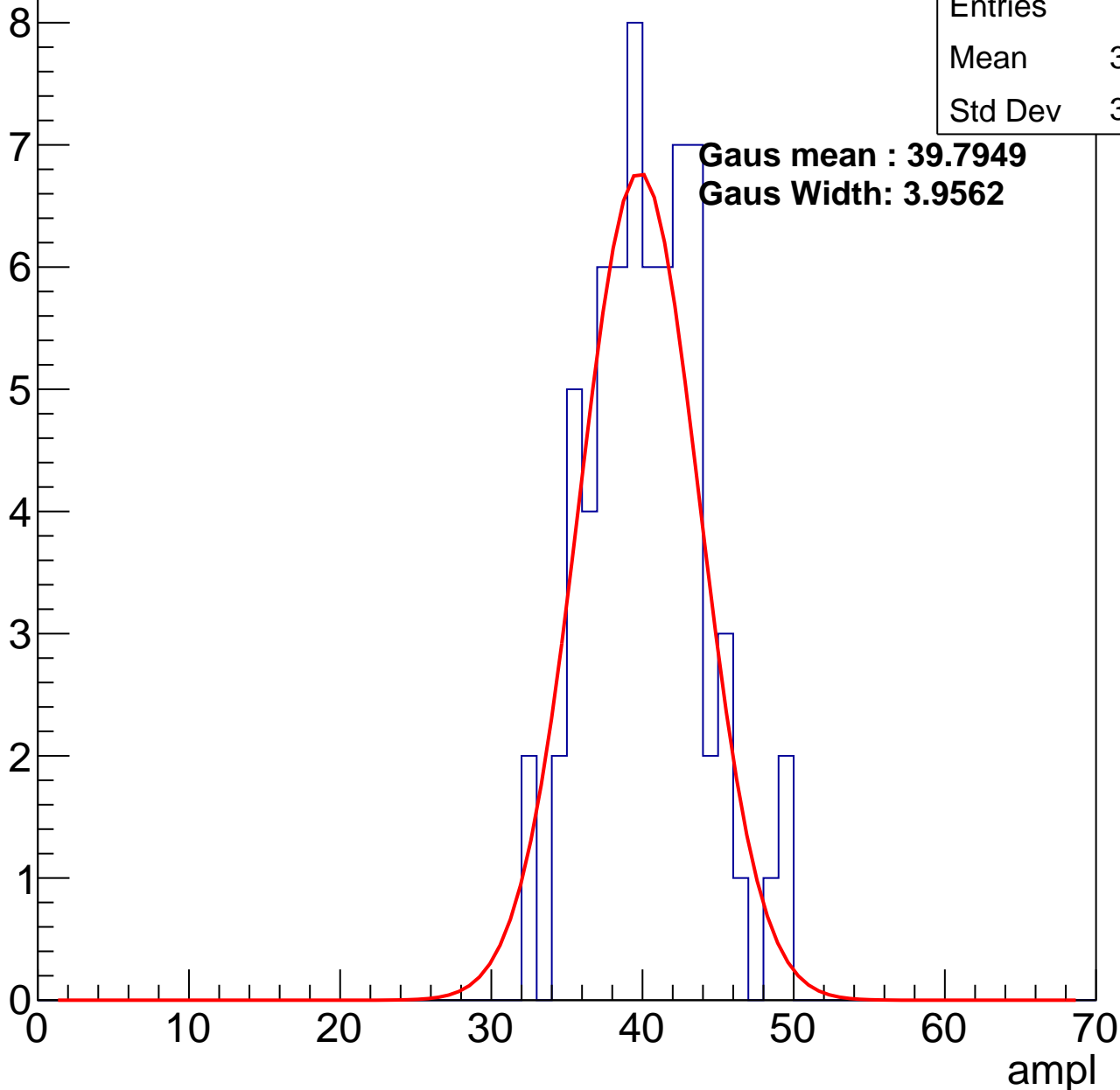
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	39.84
Std Dev	3.716

**Gaus mean : 39.7949**

**Gaus Width: 3.9562**

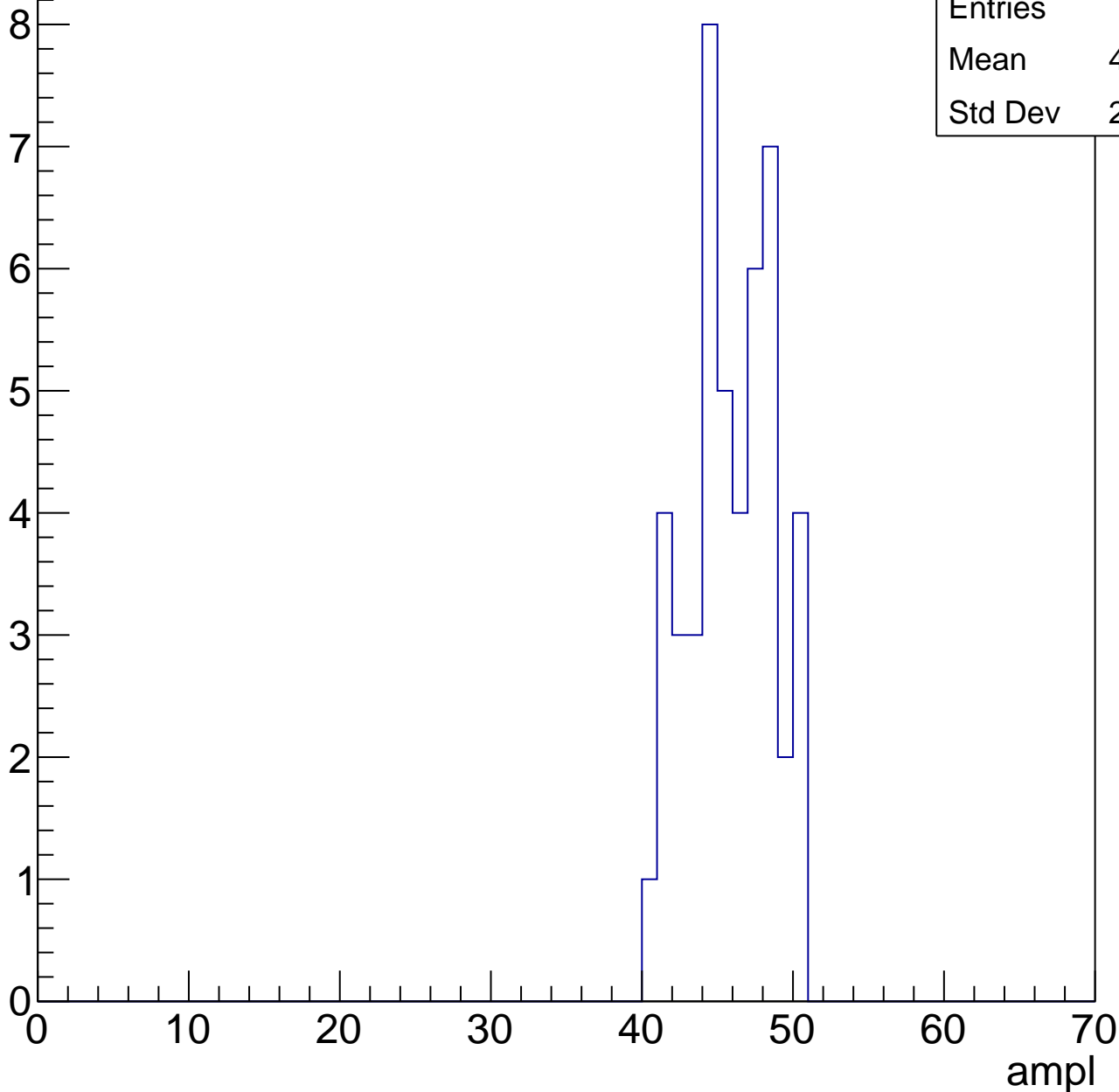


# B1L103S, U1-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

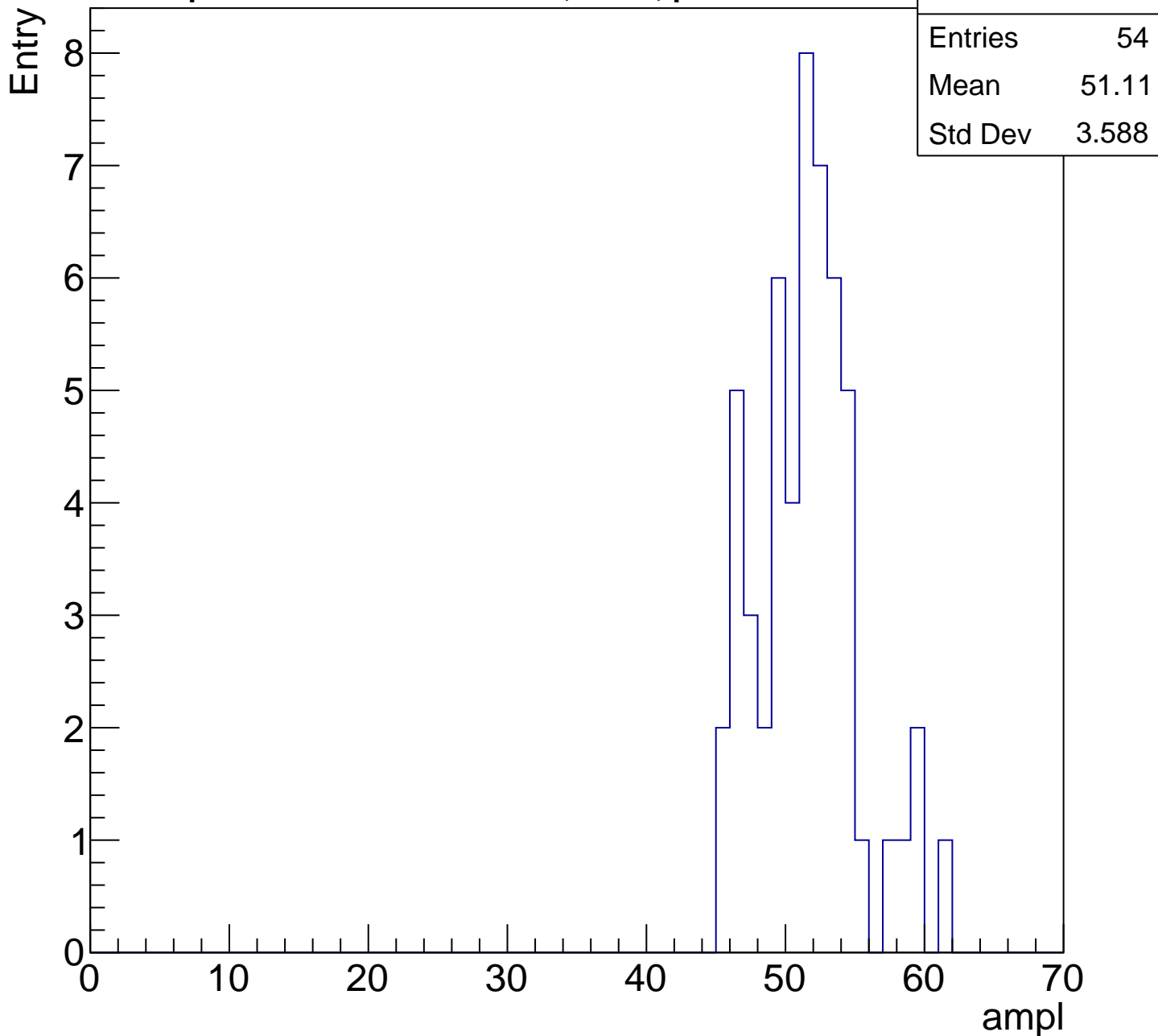
Entry

Entries	47
Mean	45.45
Std Dev	2.727



# B1L103S, U1-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

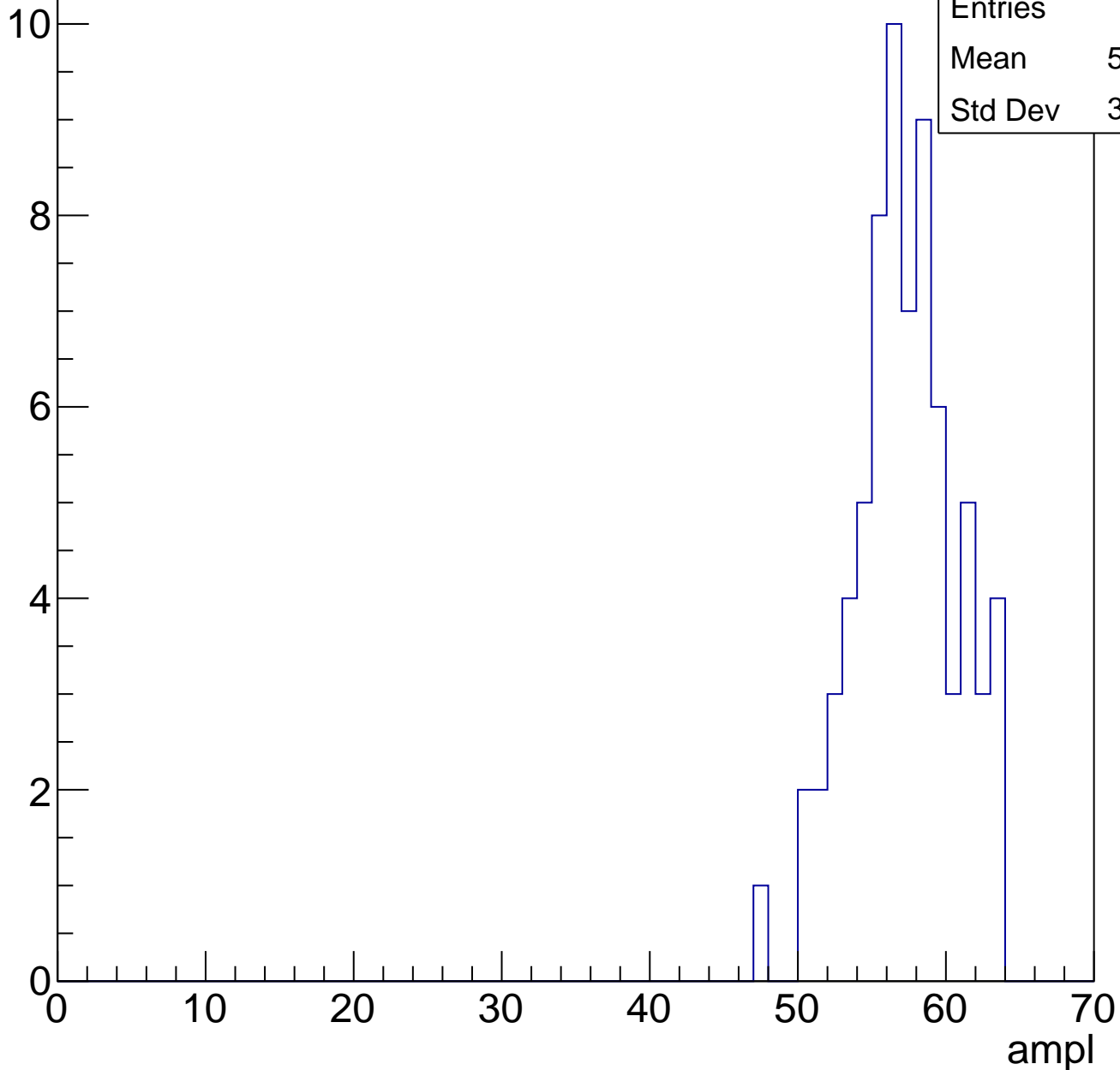


# B1L103S, U1-ch34, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	72
Mean	56.74
Std Dev	3.436

Entry

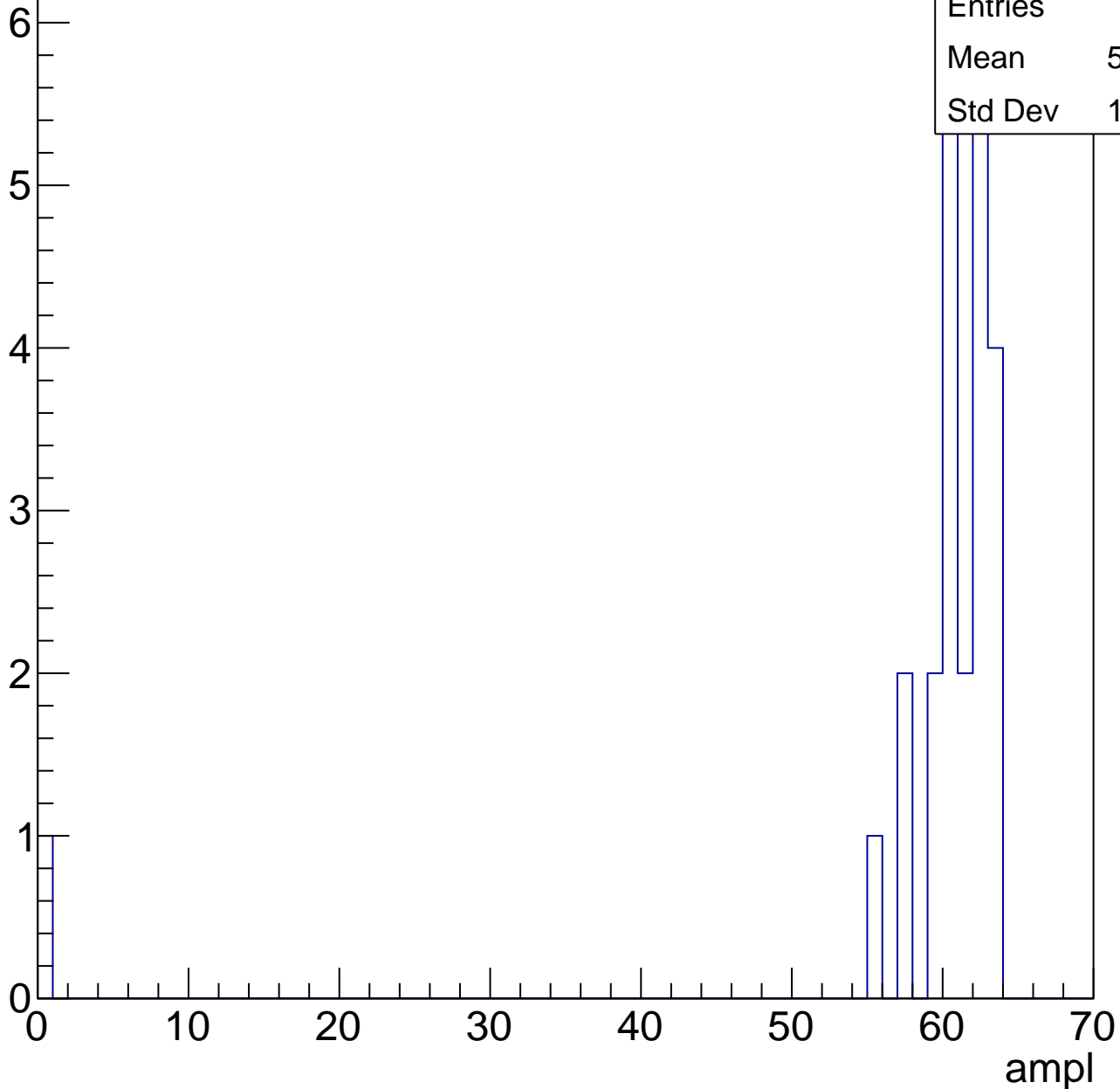


# B1L103S, U1-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	24
Mean	58.04
Std Dev	12.27





# B1L103S, U1-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

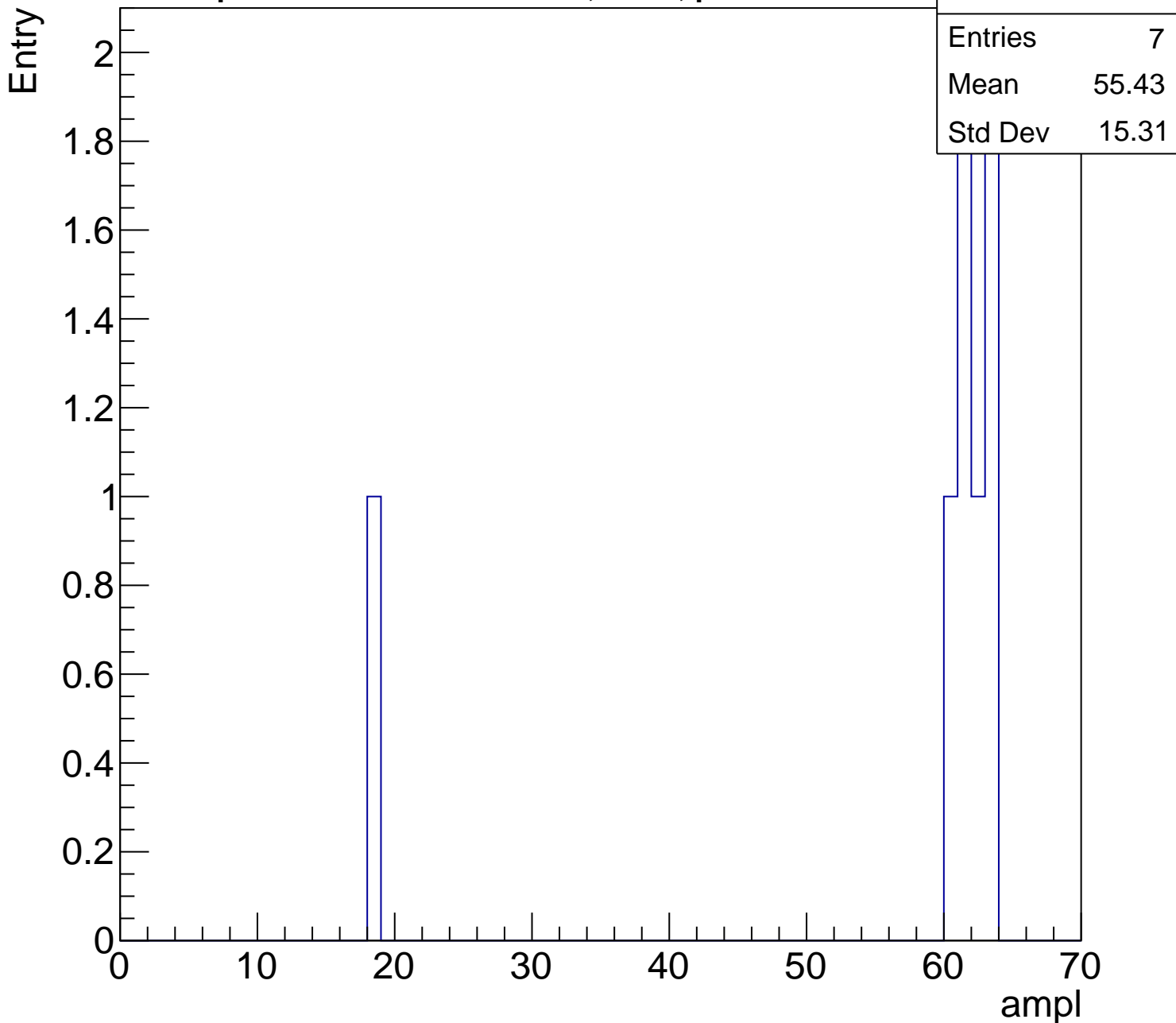
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	55.43
Std Dev	15.31

ampl

0 10 20 30 40 50 60 70



# B1L103S, U1-ch35, adc0

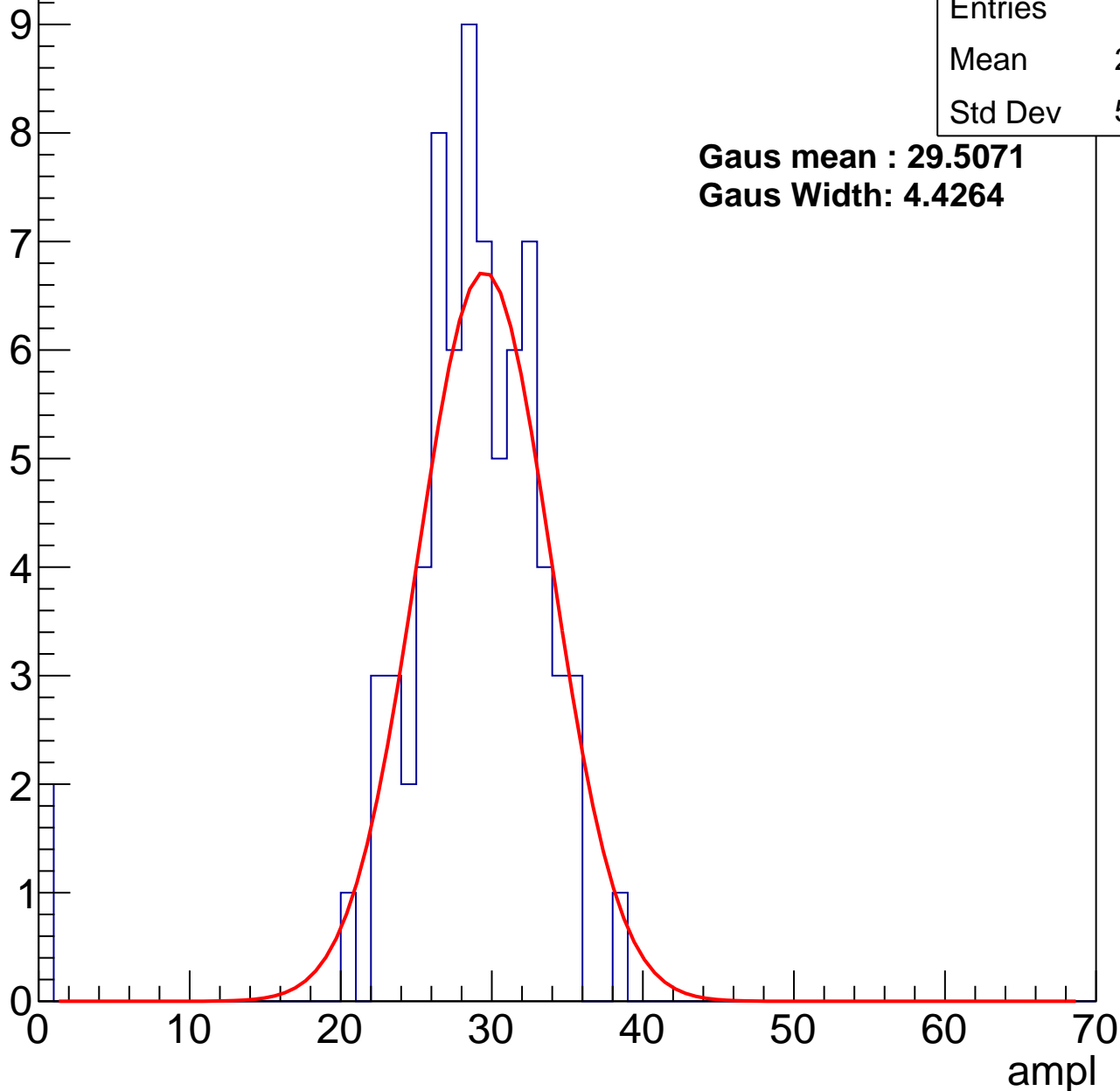
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	27.91
Std Dev	5.891

**Gaus mean : 29.5071**

**Gaus Width: 4.4264**



# B1L103S, U1-ch35, adc1

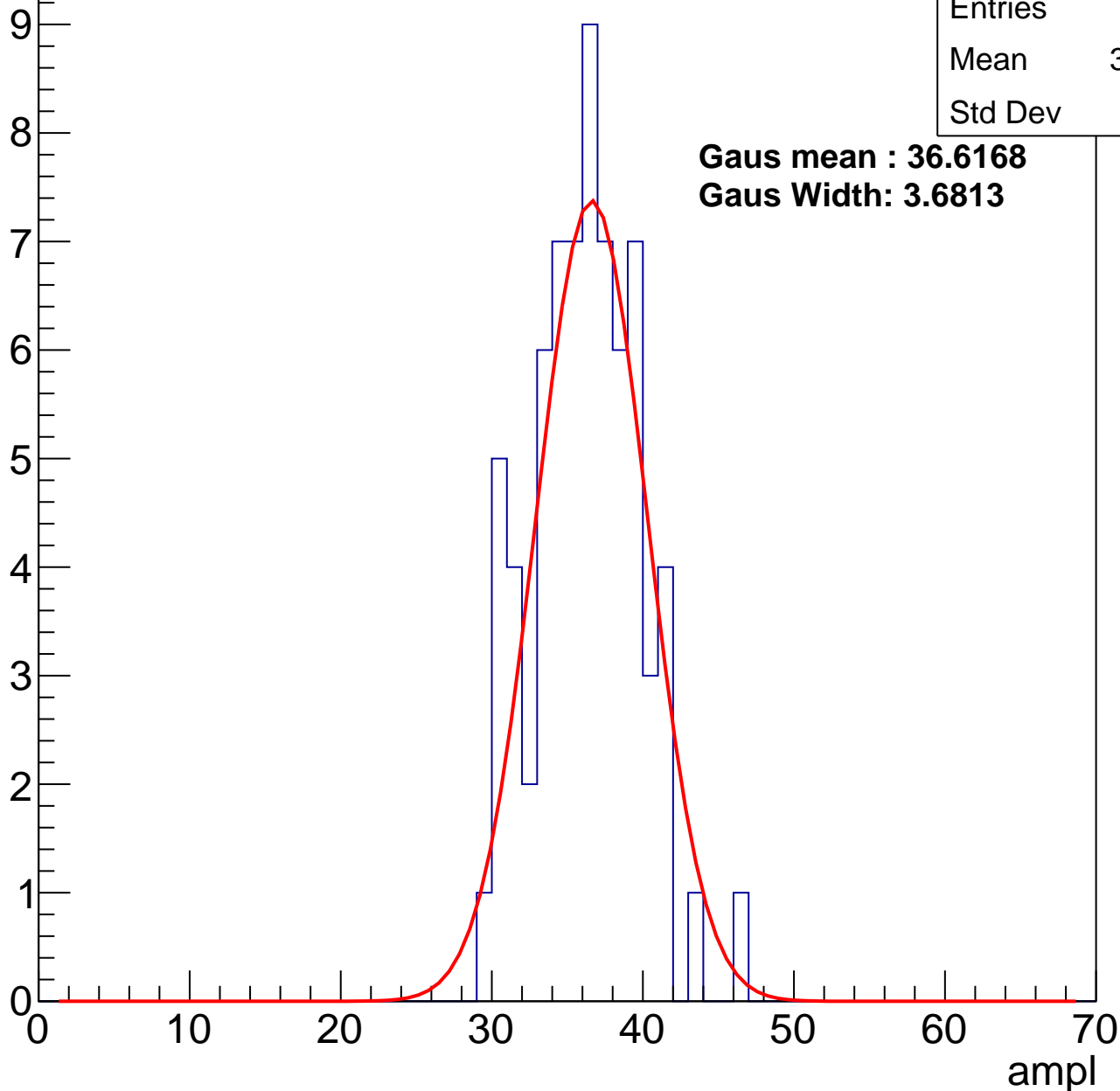
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	35.79
Std Dev	3.46

**Gaus mean : 36.6168**

**Gaus Width: 3.6813**



# B1L103S, U1-ch35, adc2

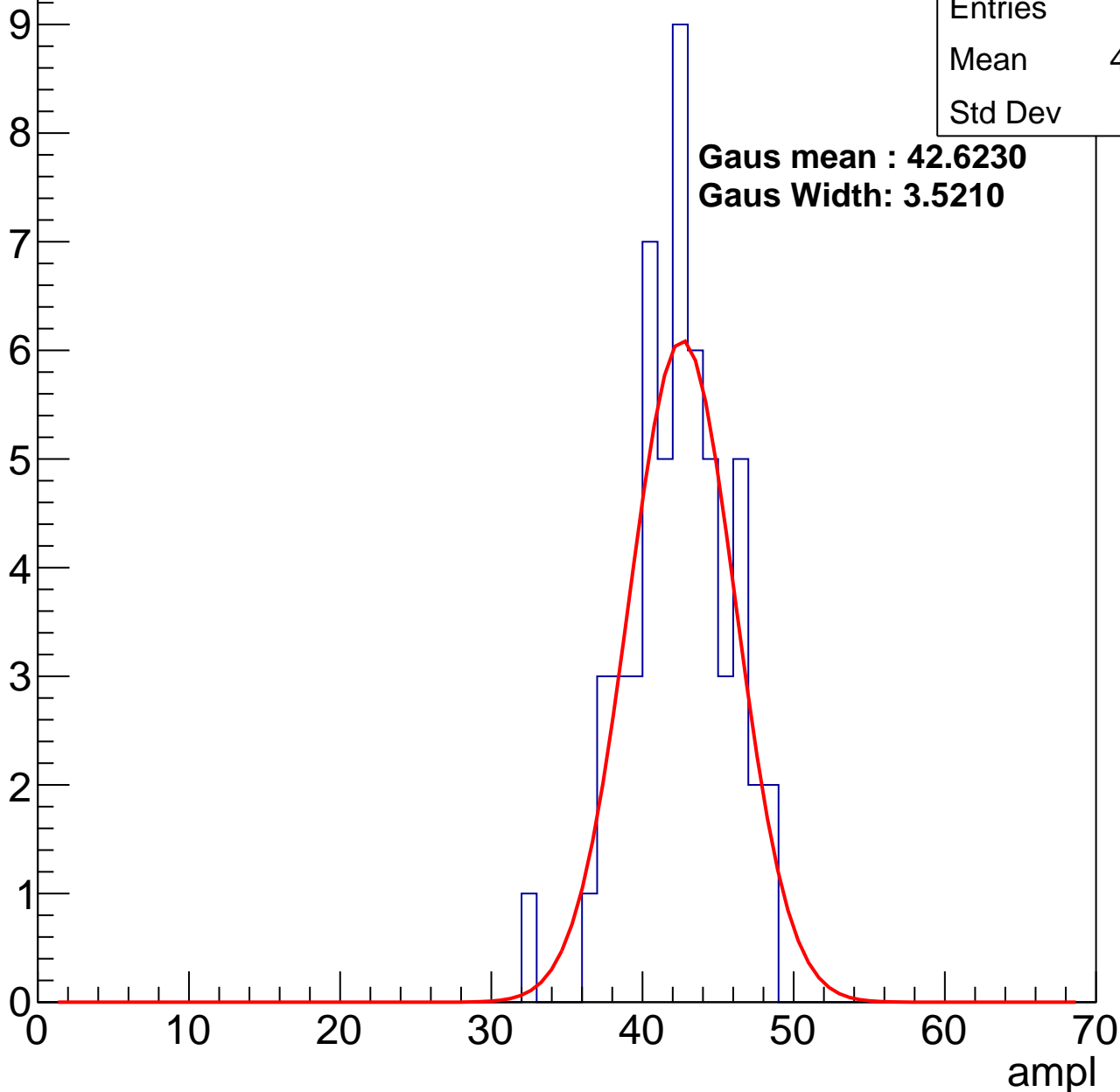
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	41.93
Std Dev	3.23

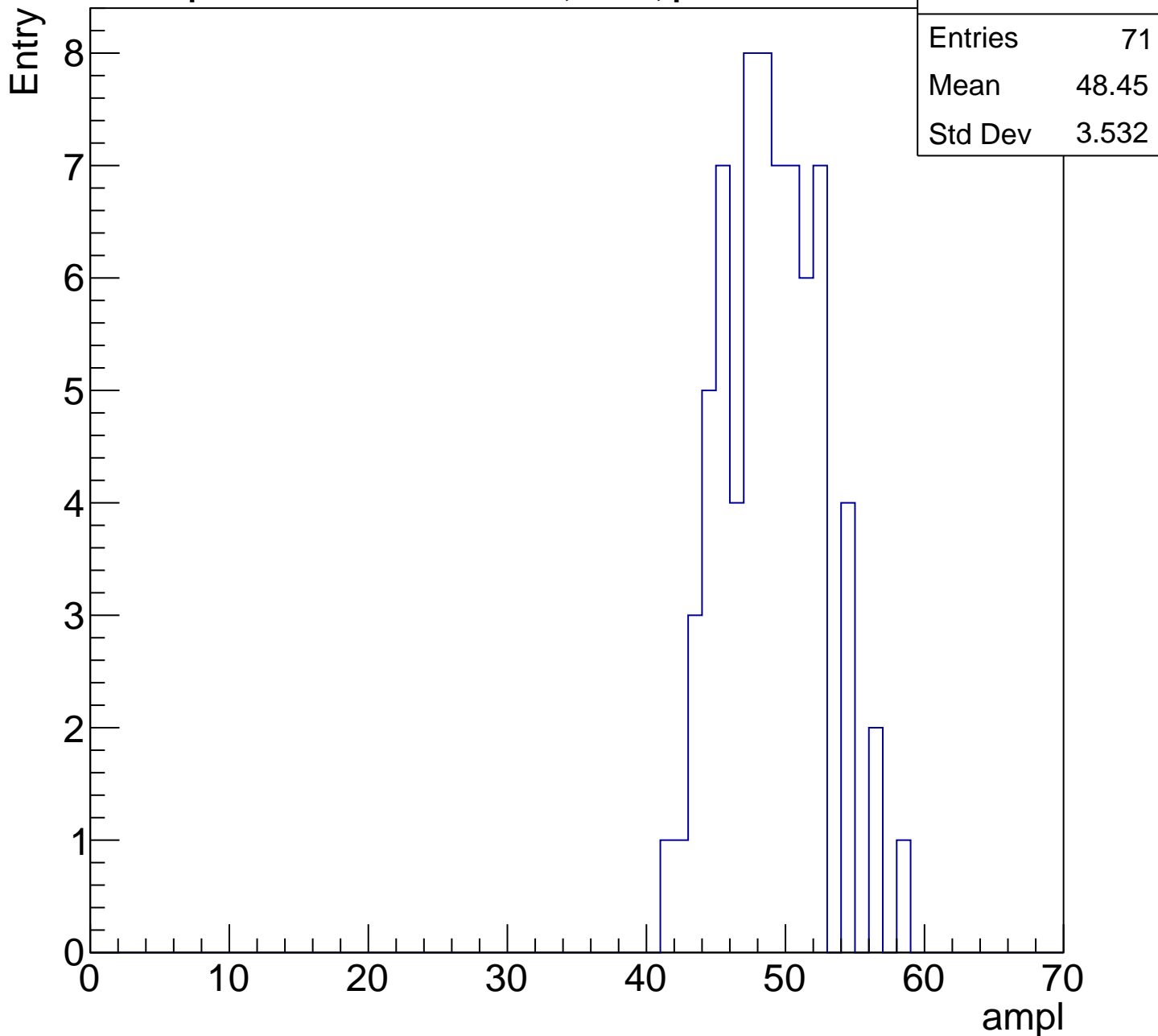
**Gaus mean : 42.6230**

**Gaus Width: 3.5210**



# B1L103S, U1-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

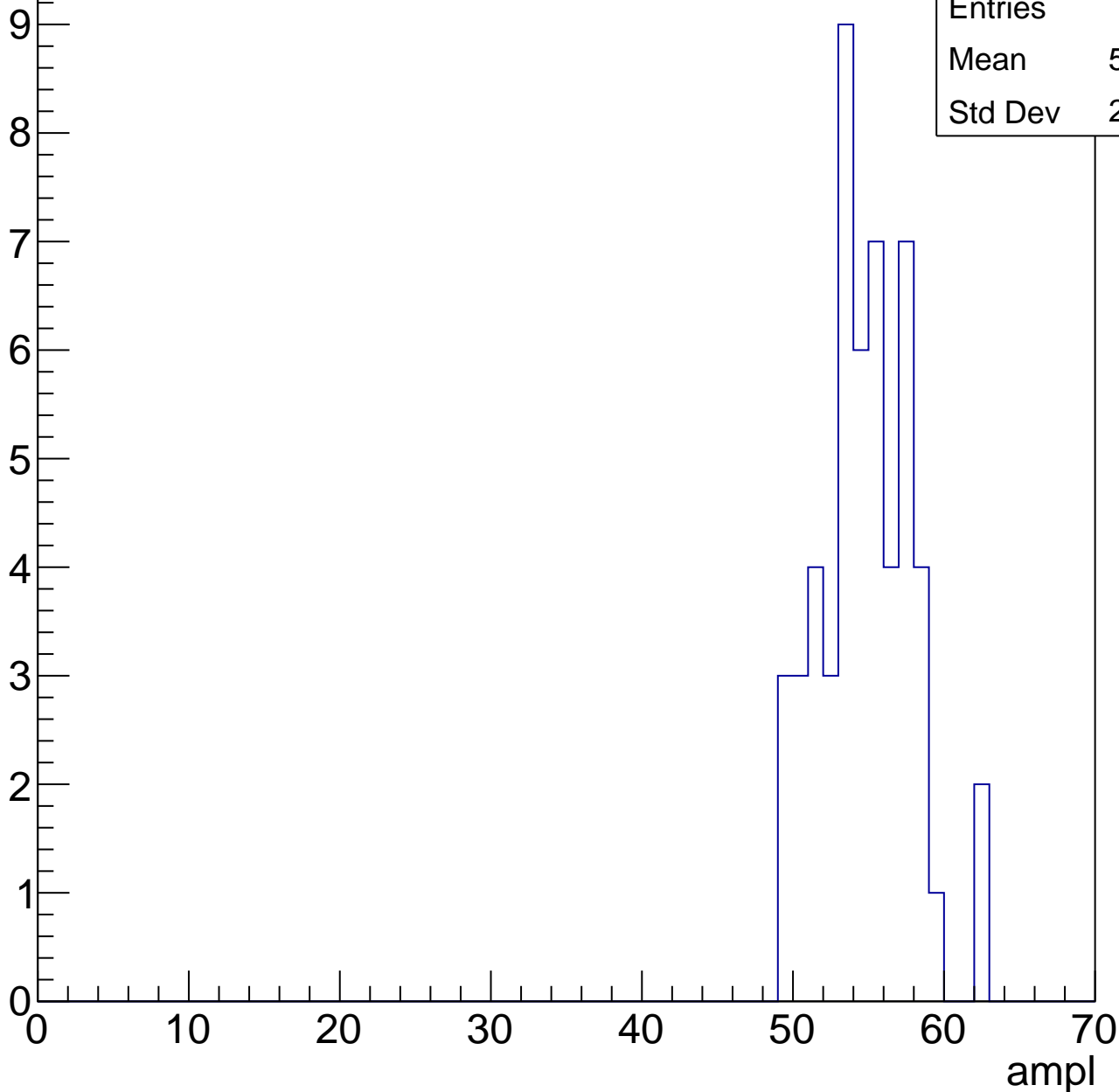


# B1L103S, U1-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

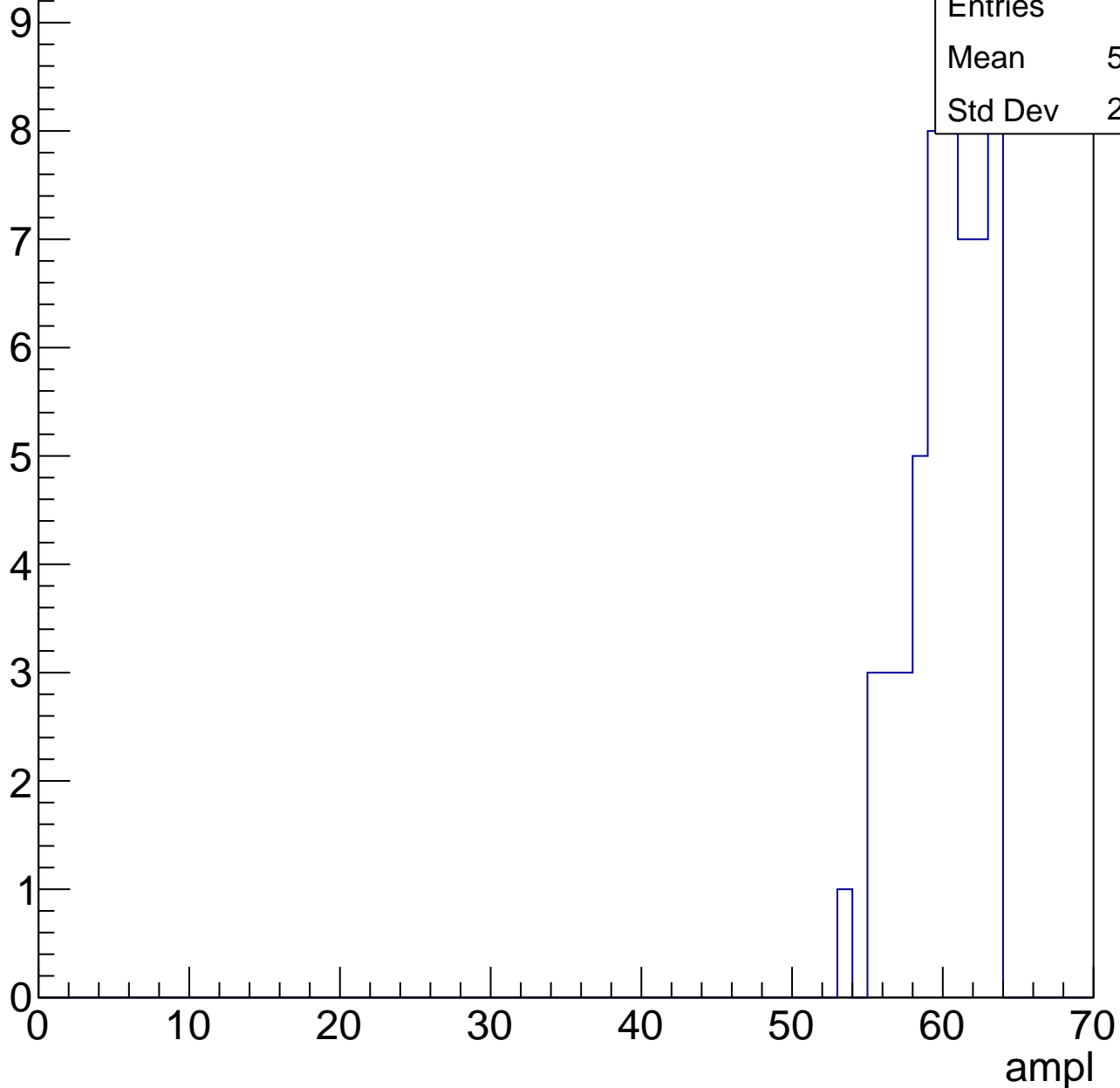
Entries	53
Mean	54.36
Std Dev	2.997



# B1L103S, U1-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

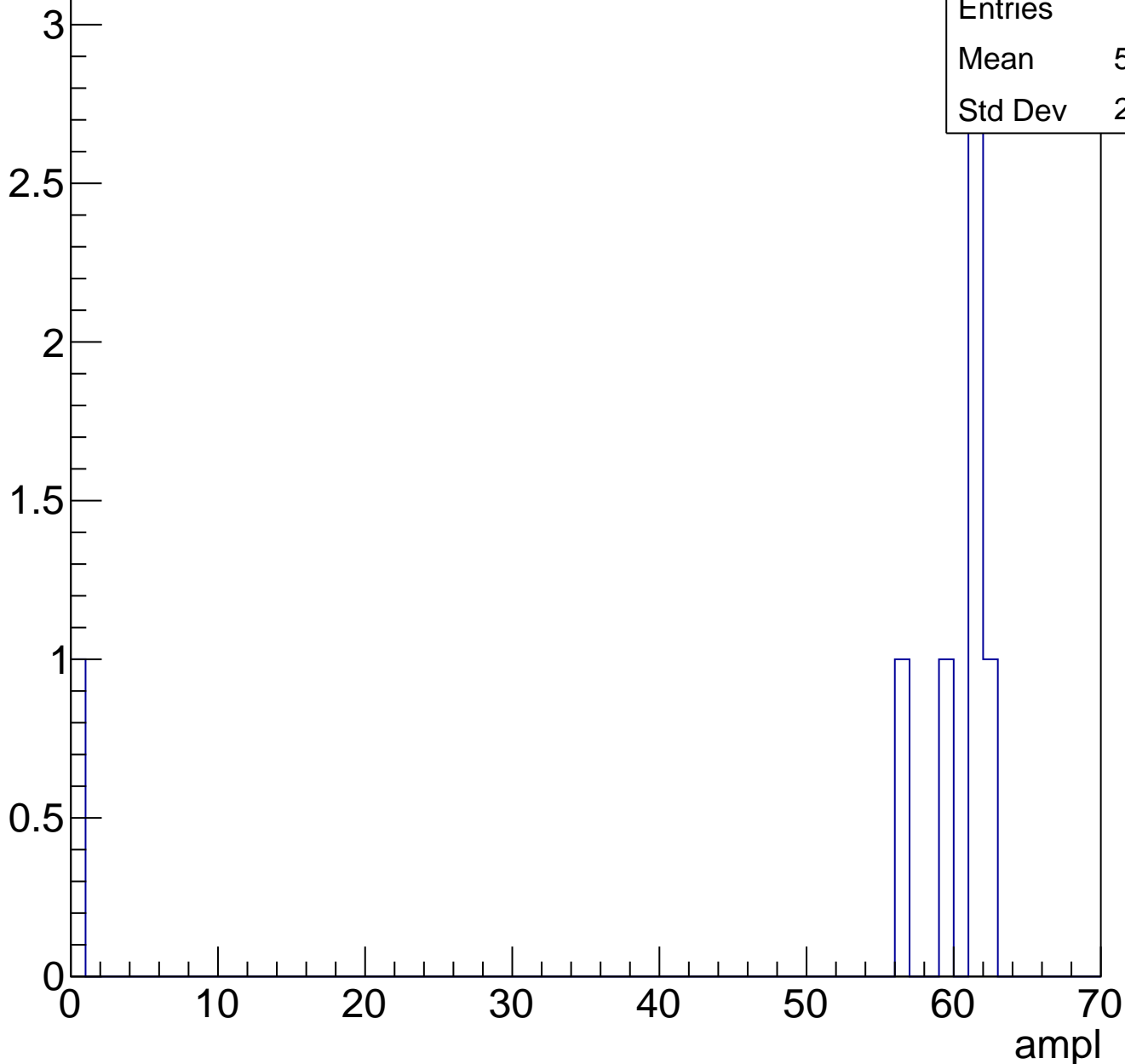
Entry



# B1L103S, U1-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

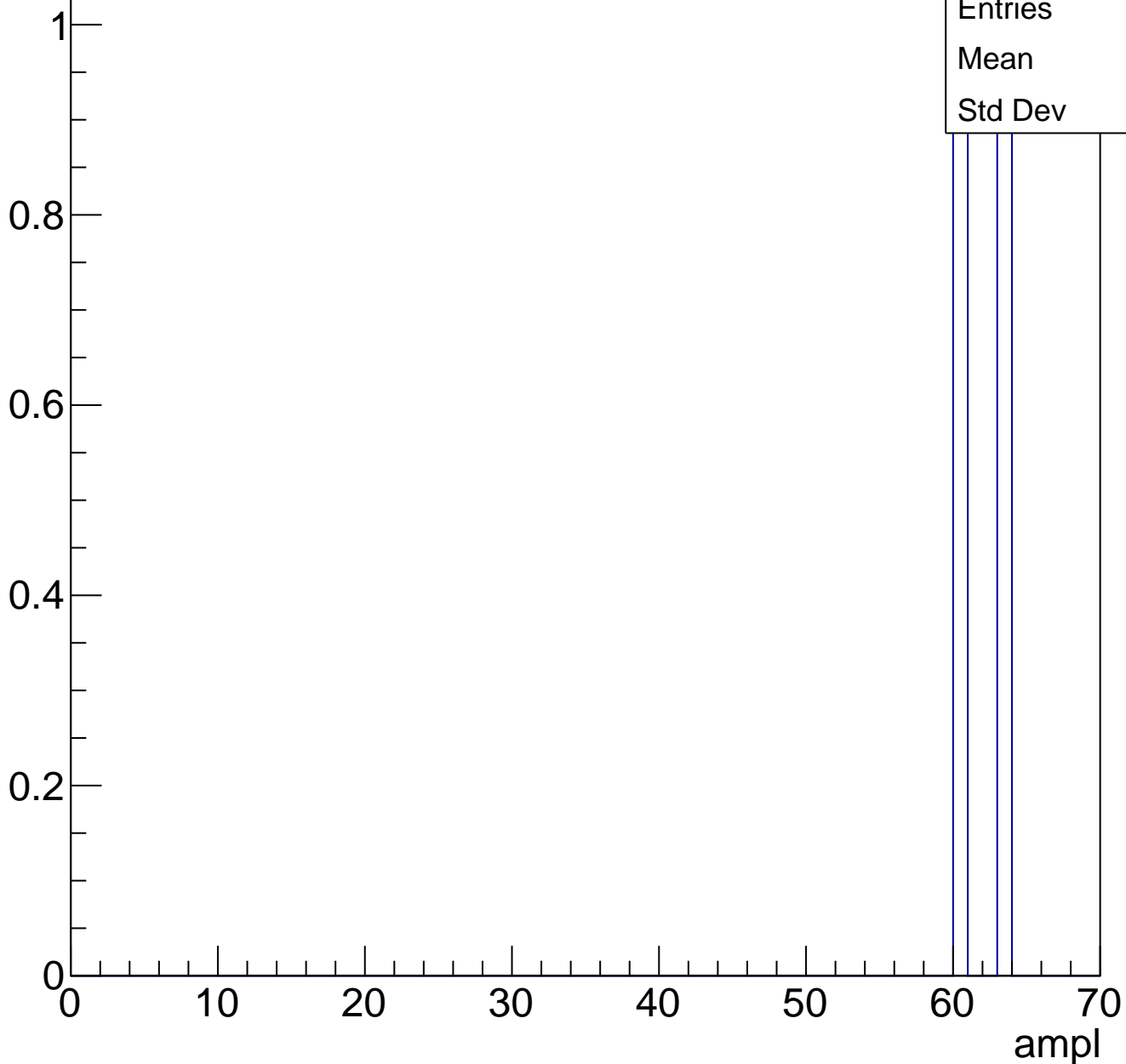




# B1L103S, U1-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch36, adc0

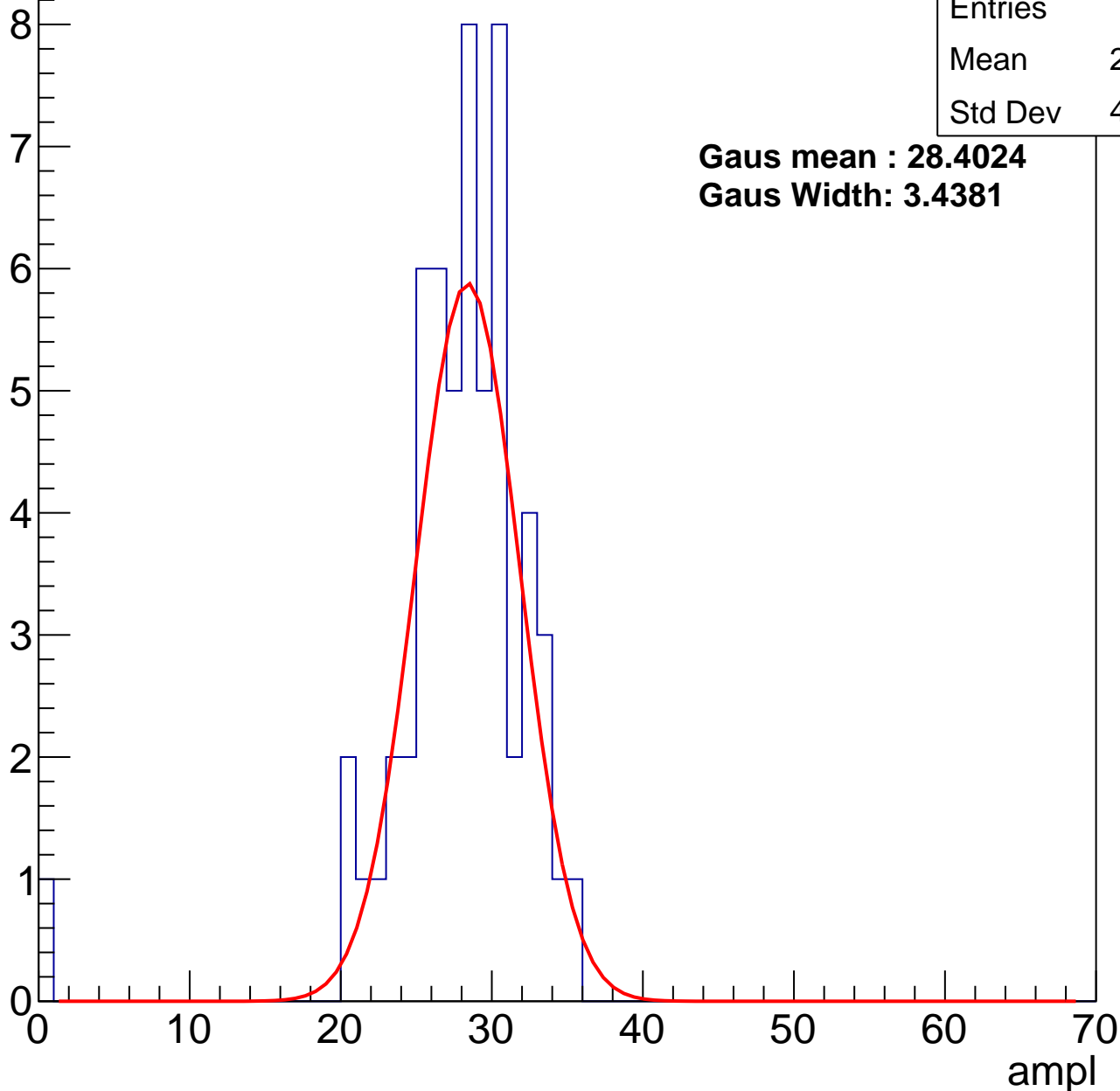
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	27.33
Std Dev	4.939

**Gaus mean : 28.4024**

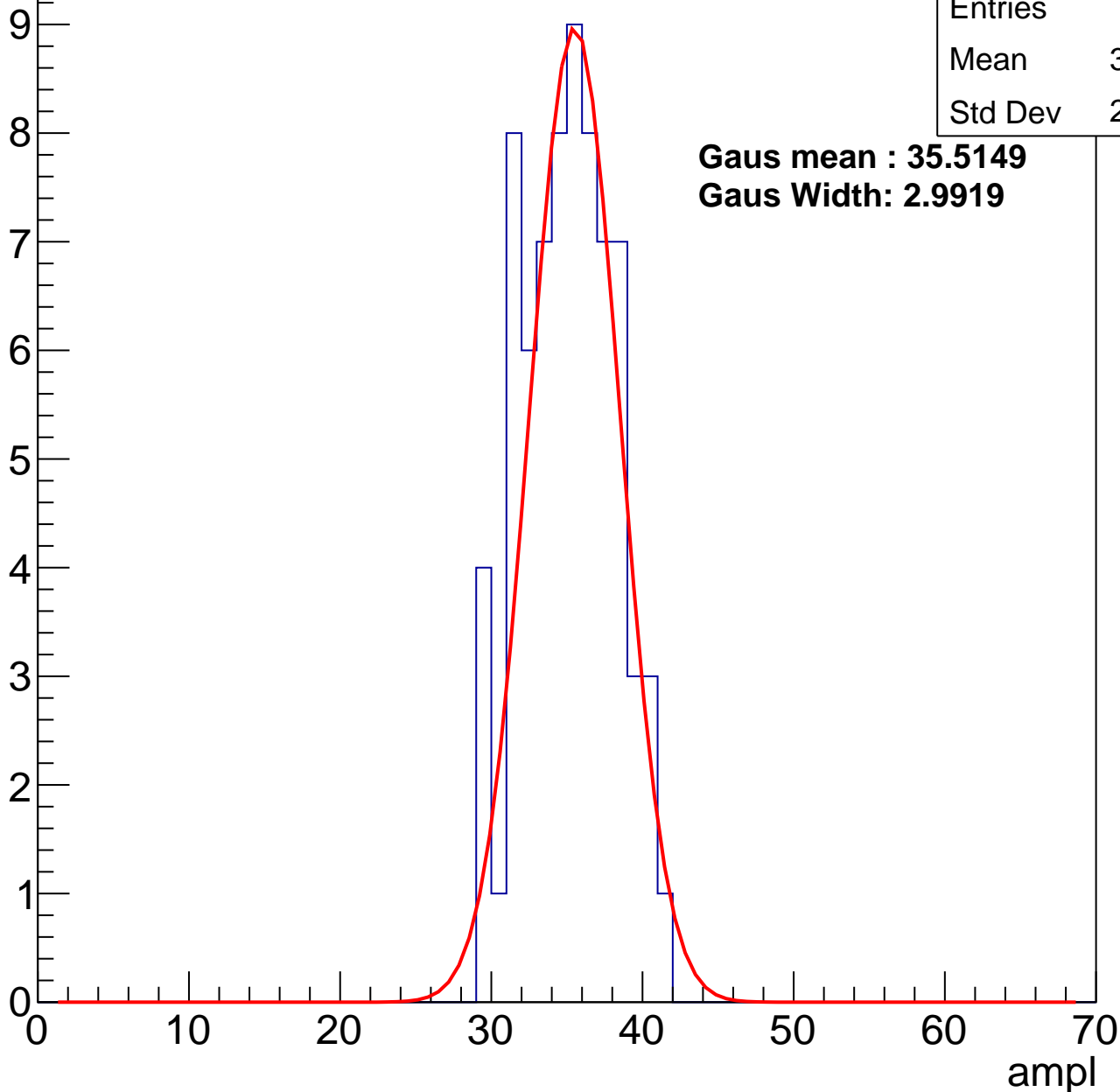
**Gaus Width: 3.4381**



# B1L103S, U1-ch36, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch36, adc2

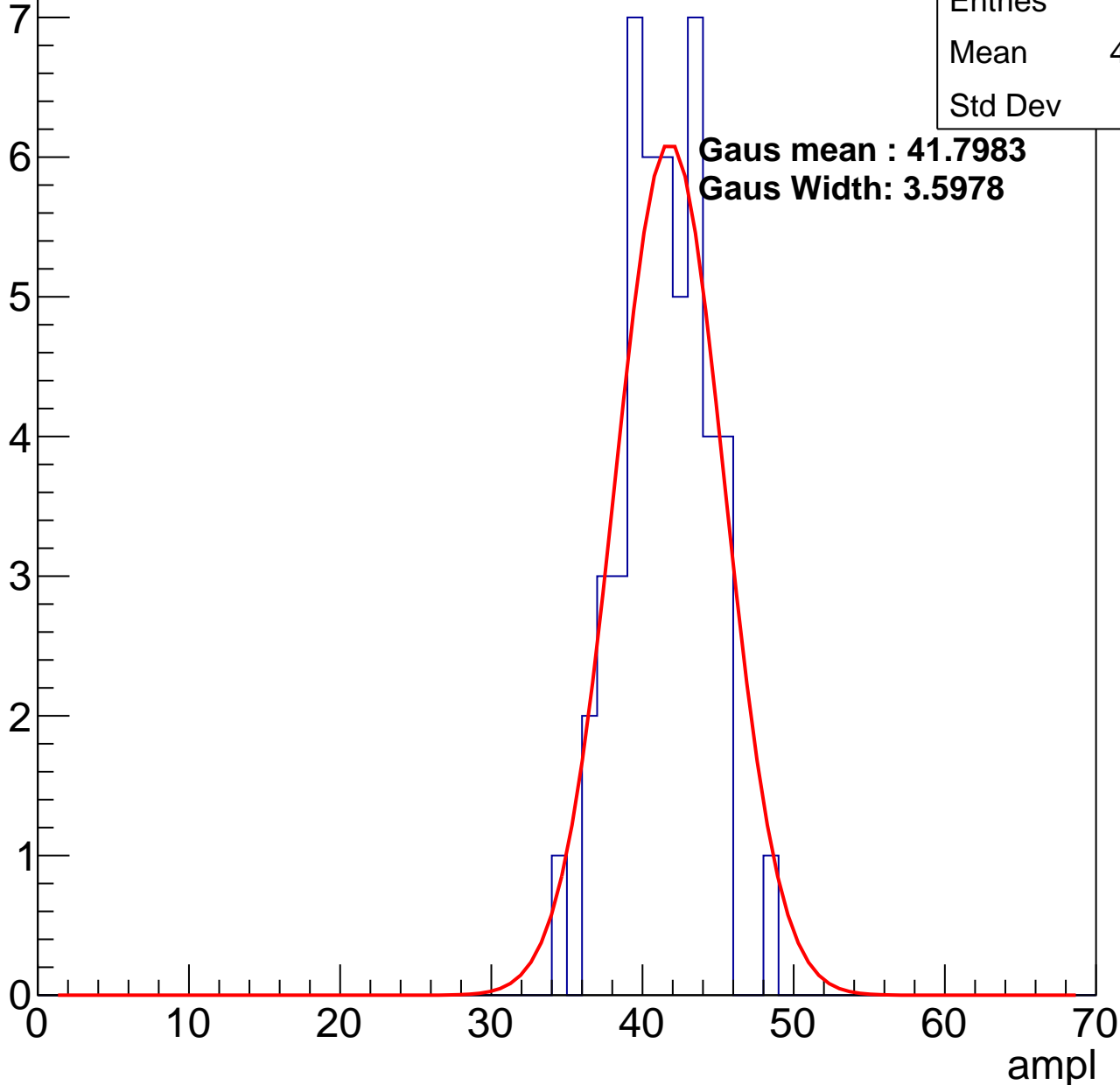
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	40.92
Std Dev	2.82

**Gaus mean : 41.7983**

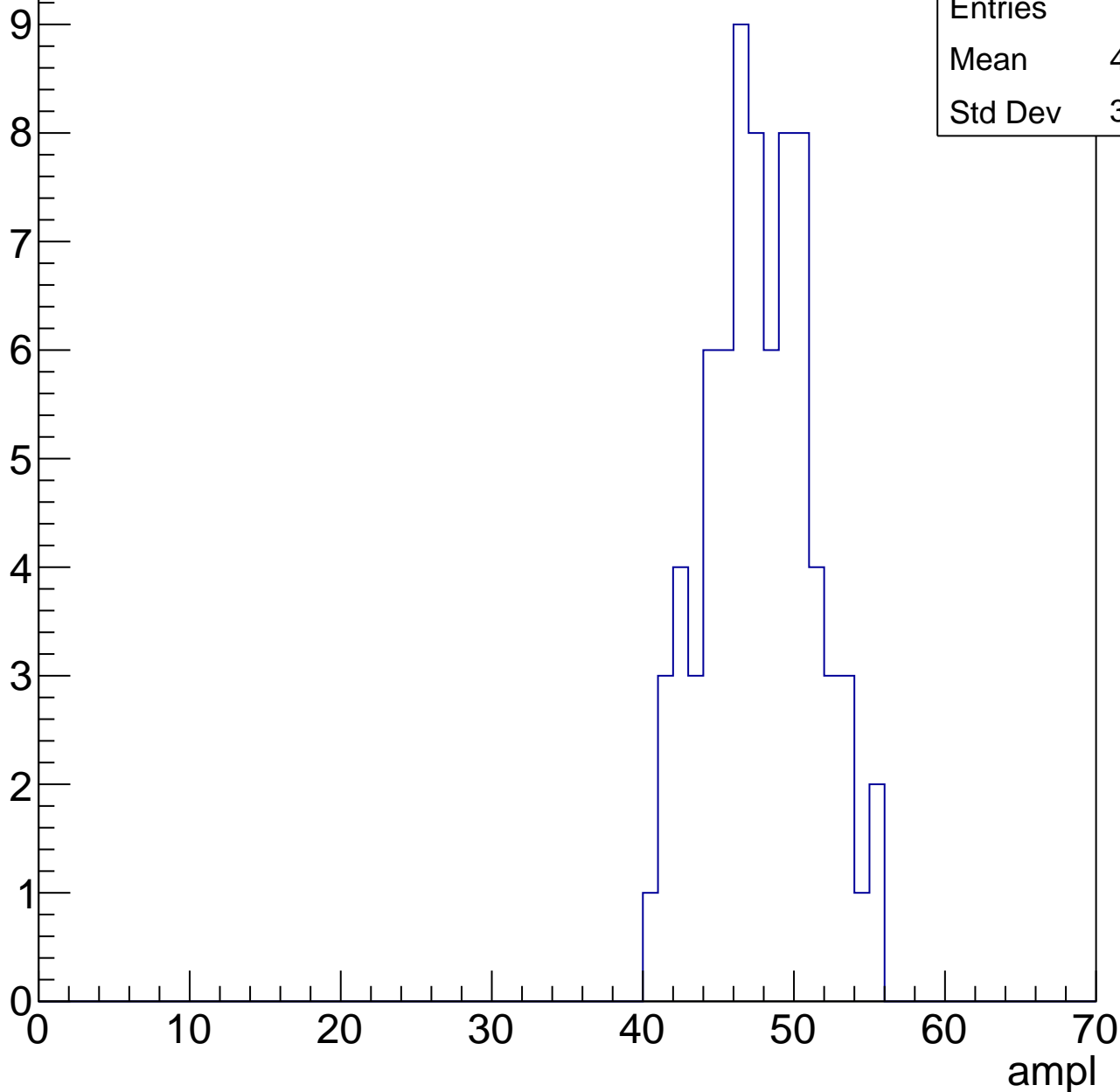
**Gaus Width: 3.5978**



# B1L103S, U1-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



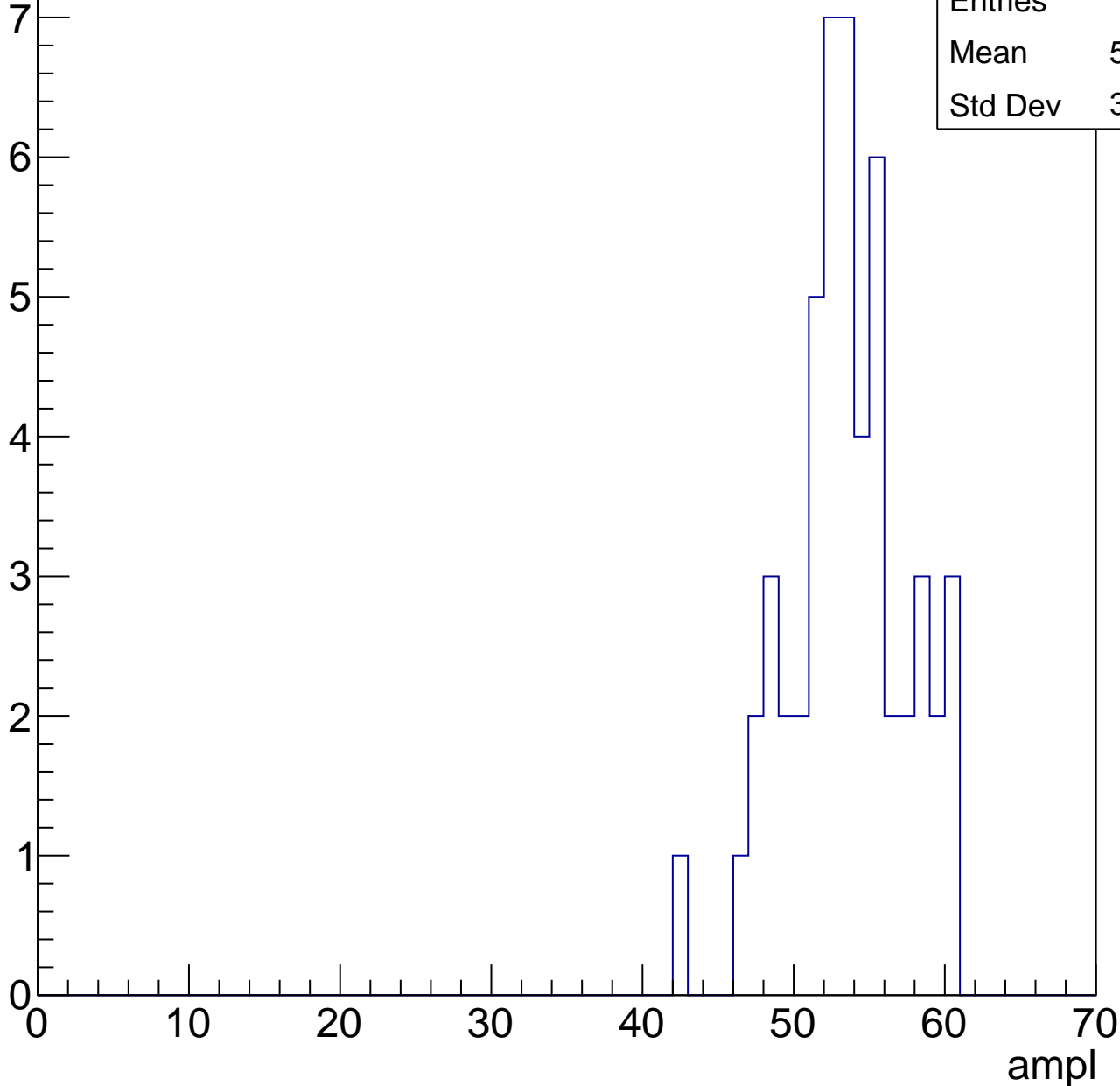
Entries	75
Mean	47.29
Std Dev	3.502

# B1L103S, U1-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

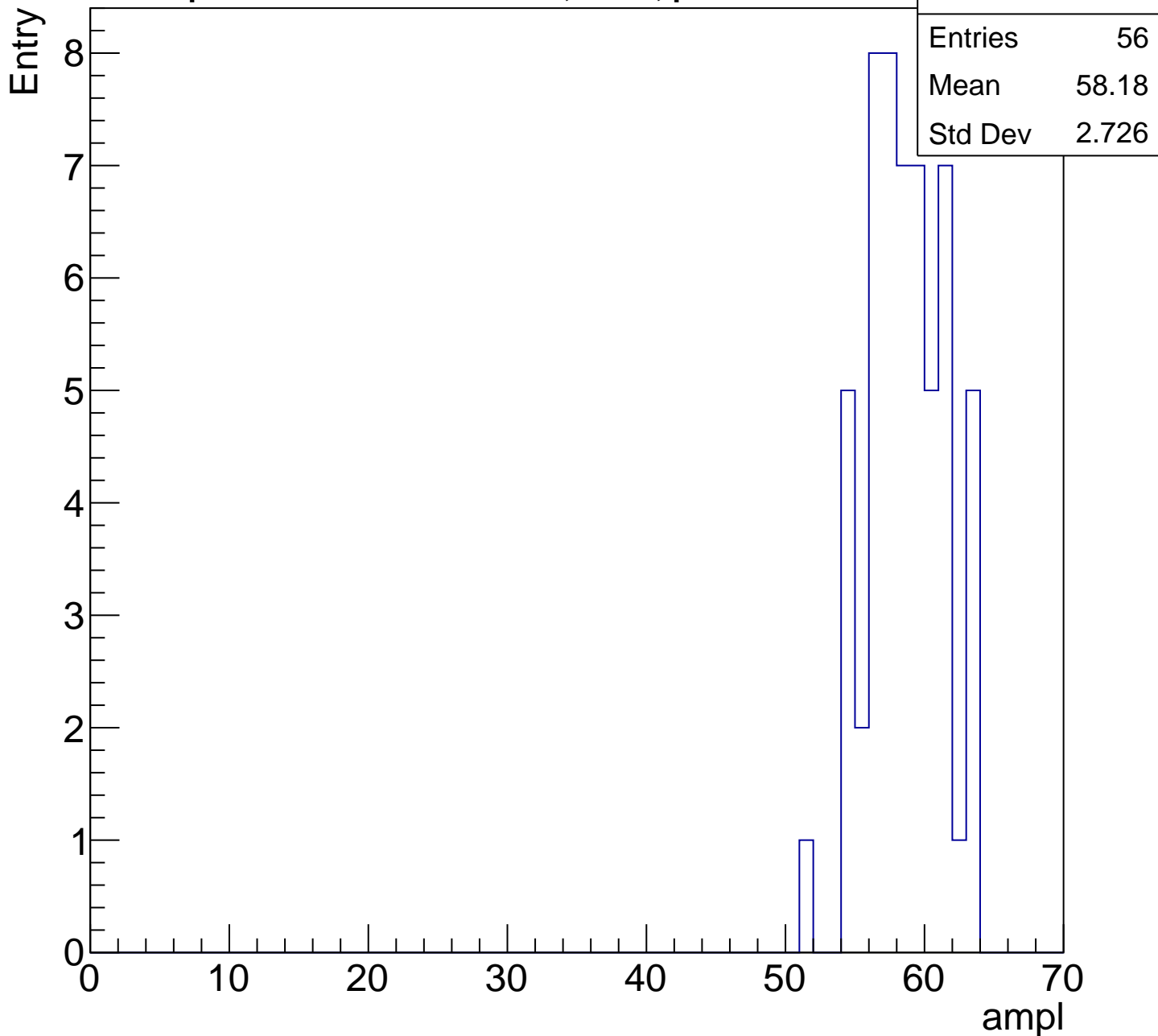
Entry

Entries	52
Mean	53.04
Std Dev	3.838



# B1L103S, U1-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

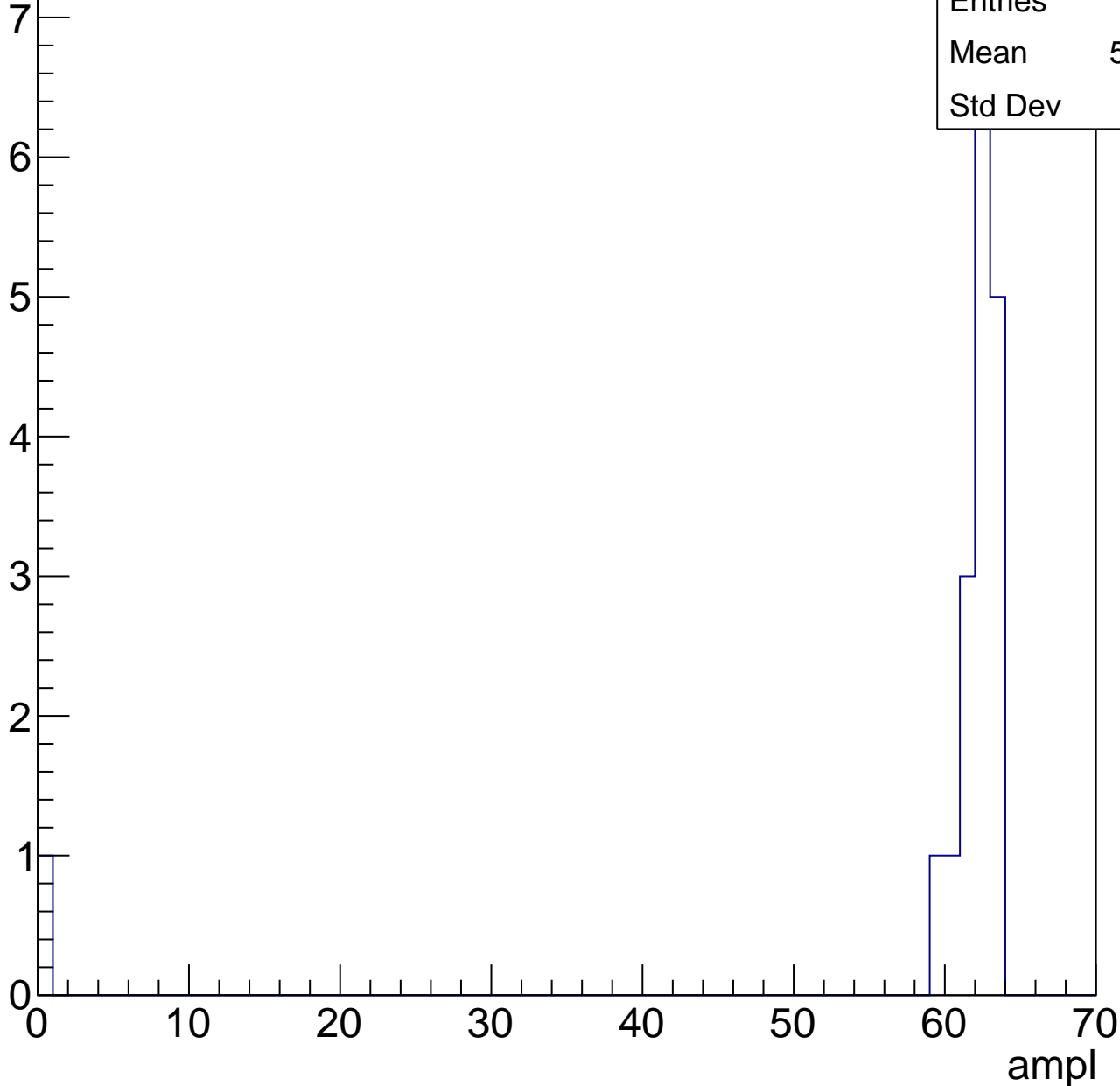


# B1L103S, U1-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	18
Mean	58.39
Std Dev	14.2

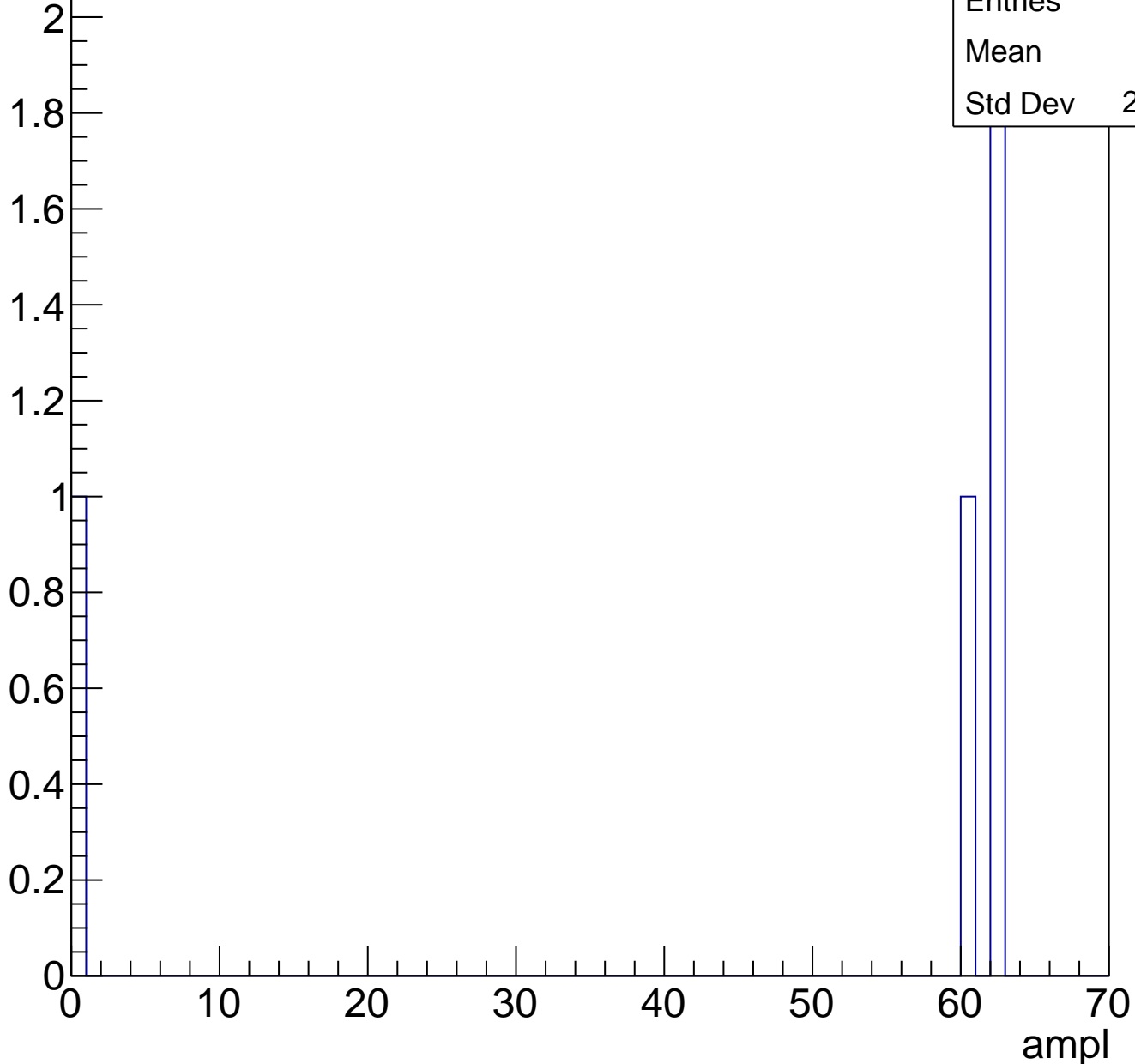




# B1L103S, U1-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	4
Mean	46
Std Dev	26.57

# B1L103S, U1-ch37, adc0

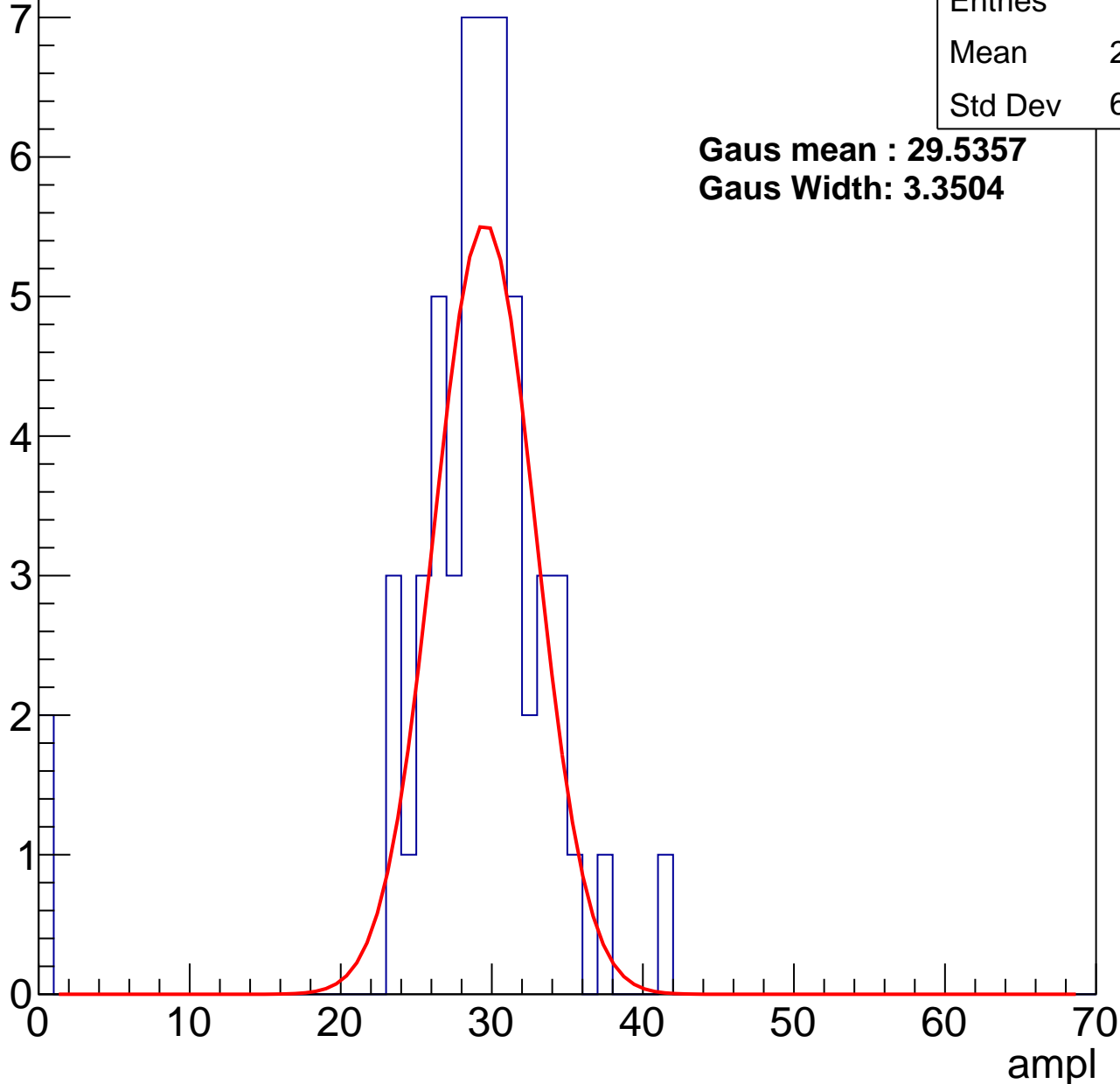
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	28.17
Std Dev	6.528

**Gaus mean : 29.5357**

**Gaus Width: 3.3504**



# B1L103S, U1-ch37, adc1

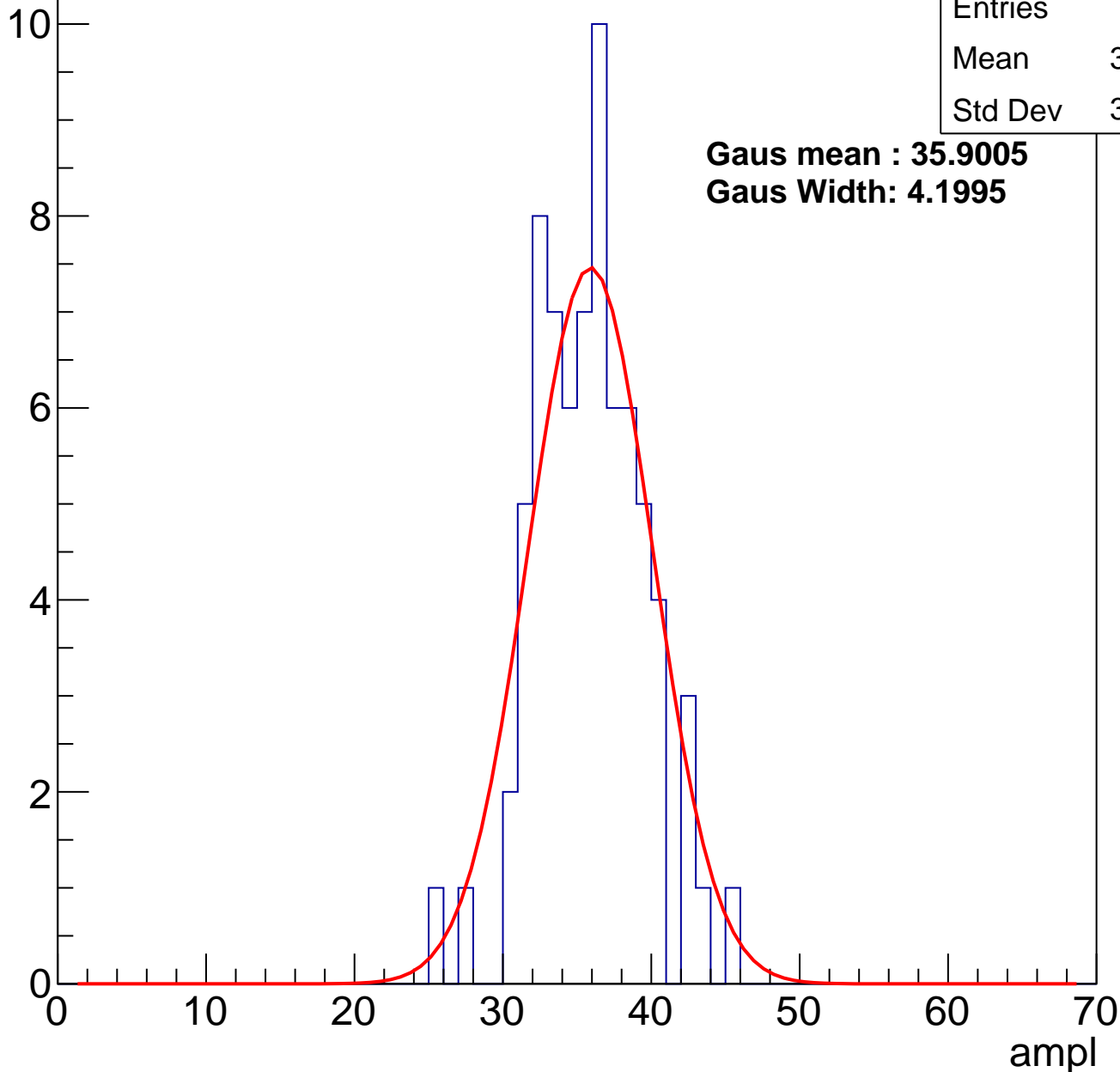
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	73
Mean	35.37
Std Dev	3.643

**Gaus mean : 35.9005**

**Gaus Width: 4.1995**

Entry



# B1L103S, U1-ch37, adc2

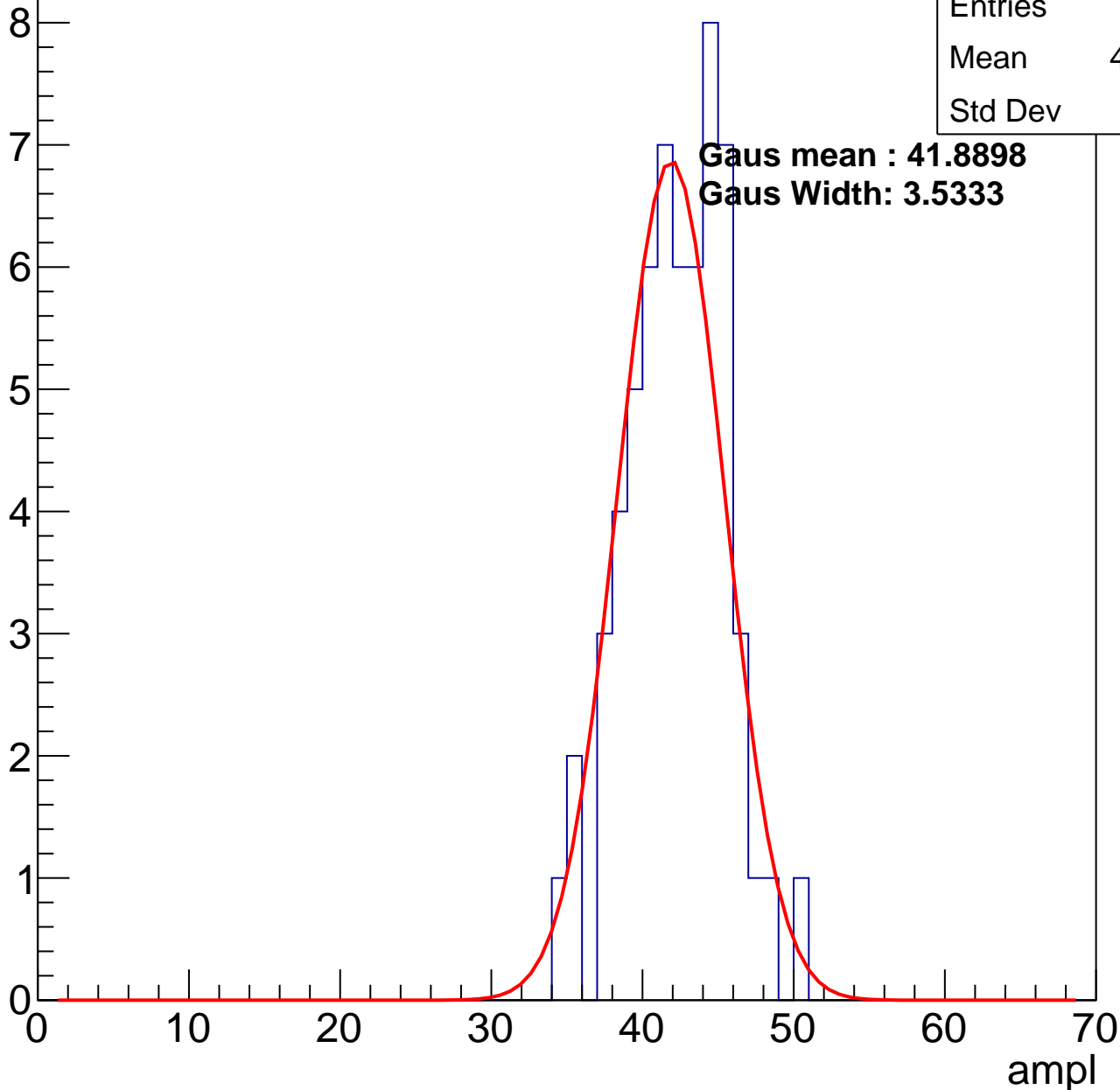
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	41.79
Std Dev	3.26

**Gaus mean : 41.8898**

**Gaus Width: 3.5333**

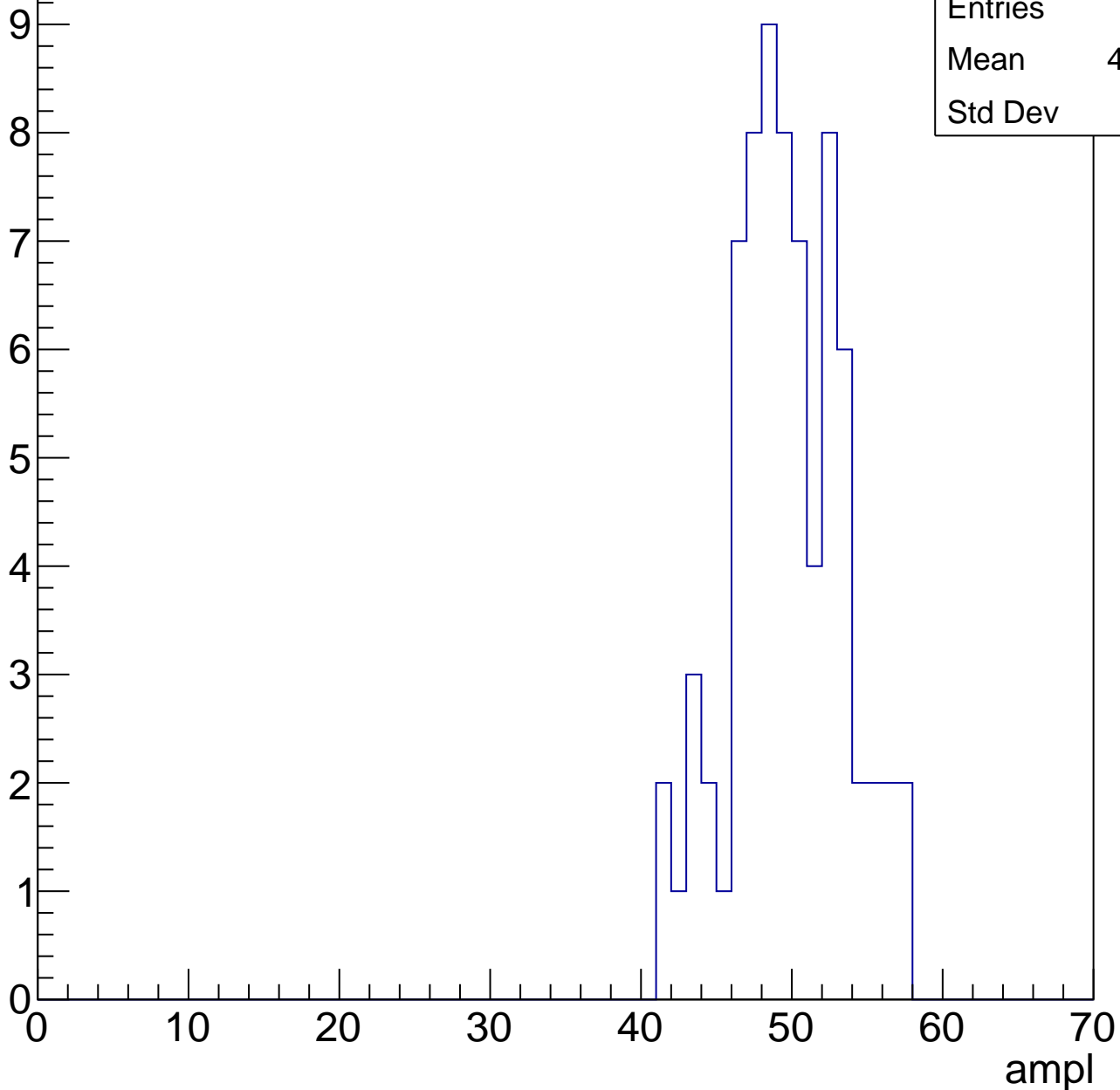


# B1L103S, U1-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	49.19
Std Dev	3.66

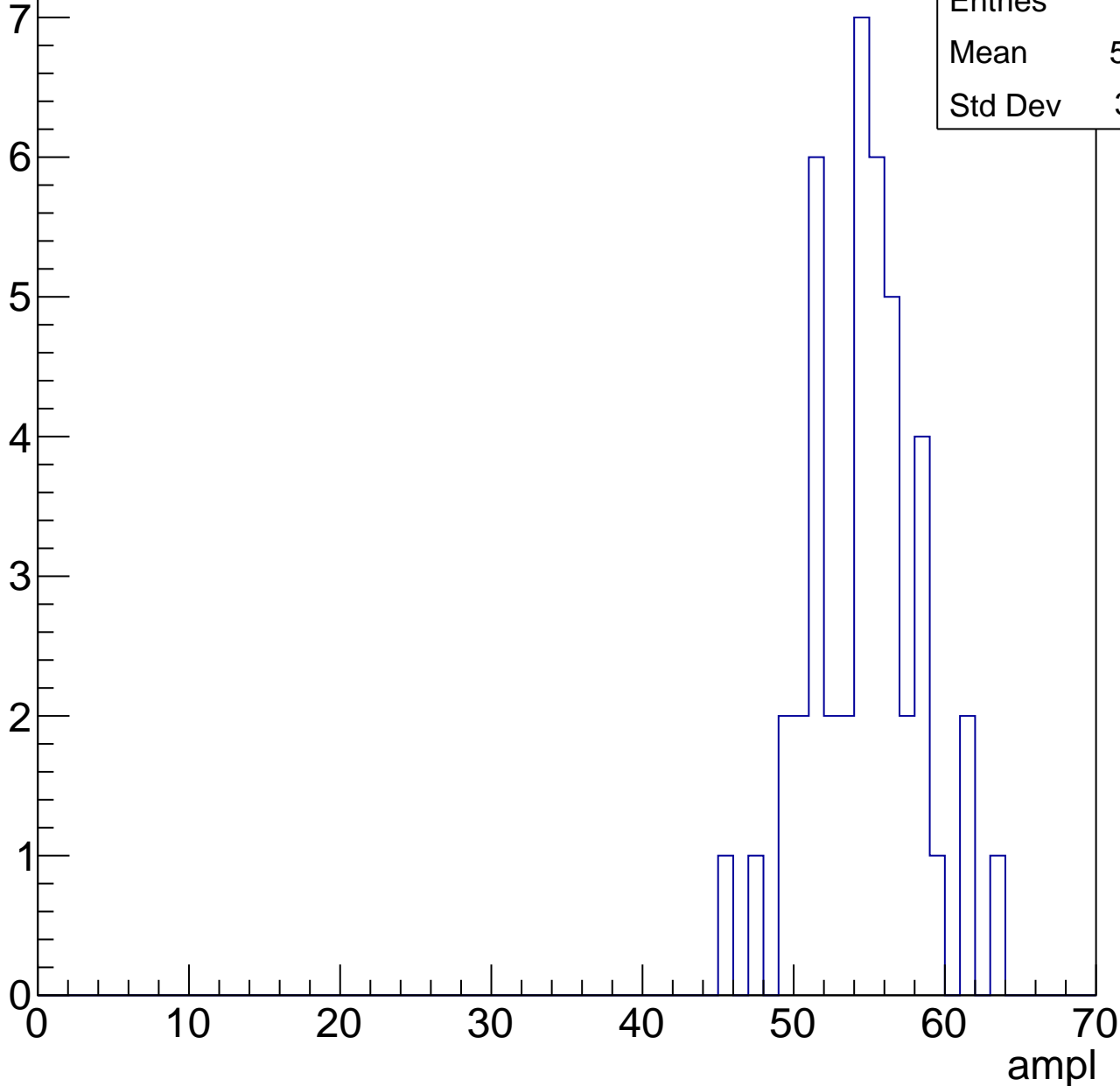


# B1L103S, U1-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	54.18
Std Dev	3.651



# B1L103S, U1-ch37, adc5

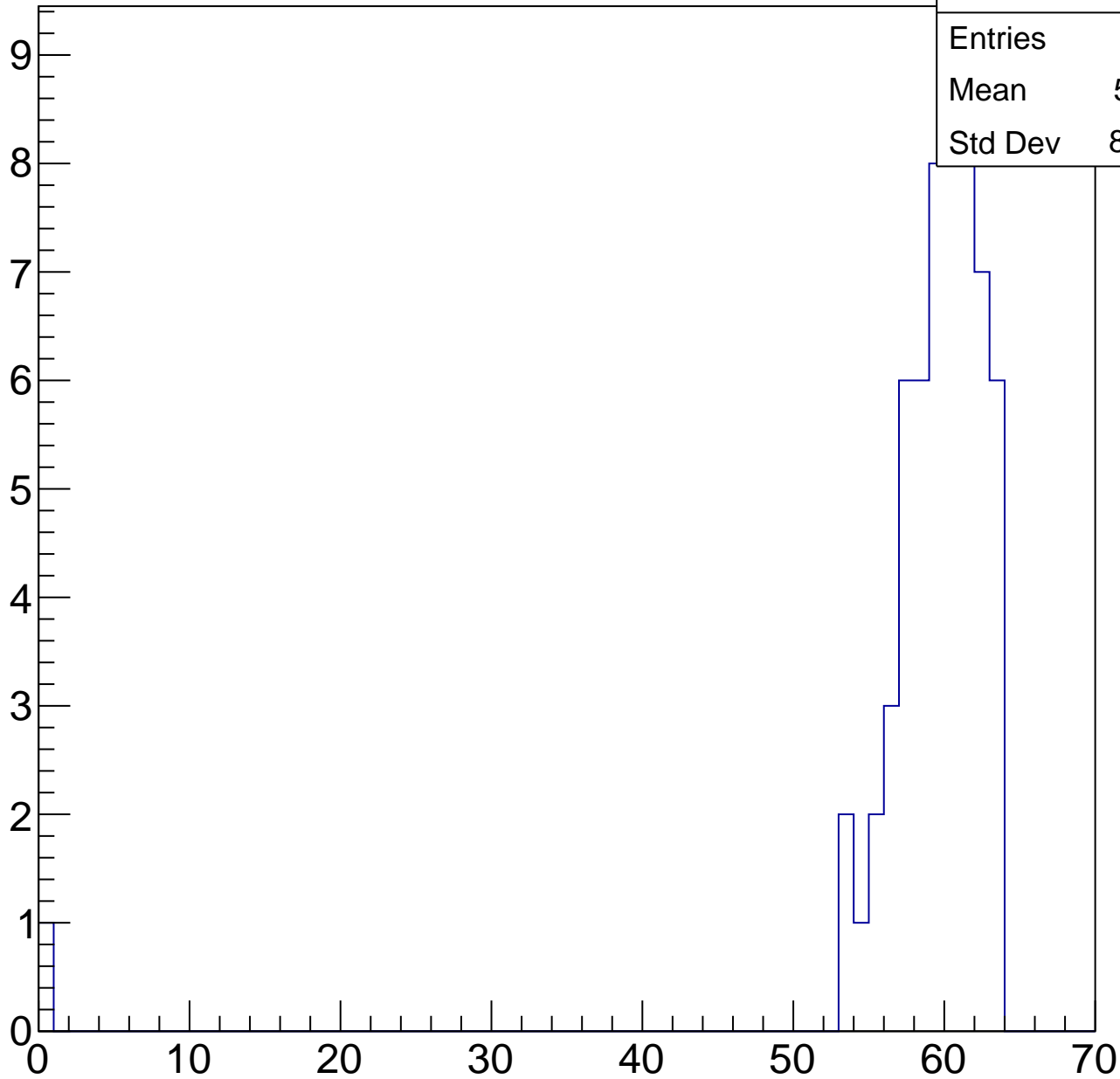
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	59
Mean	58.31
Std Dev	8.066

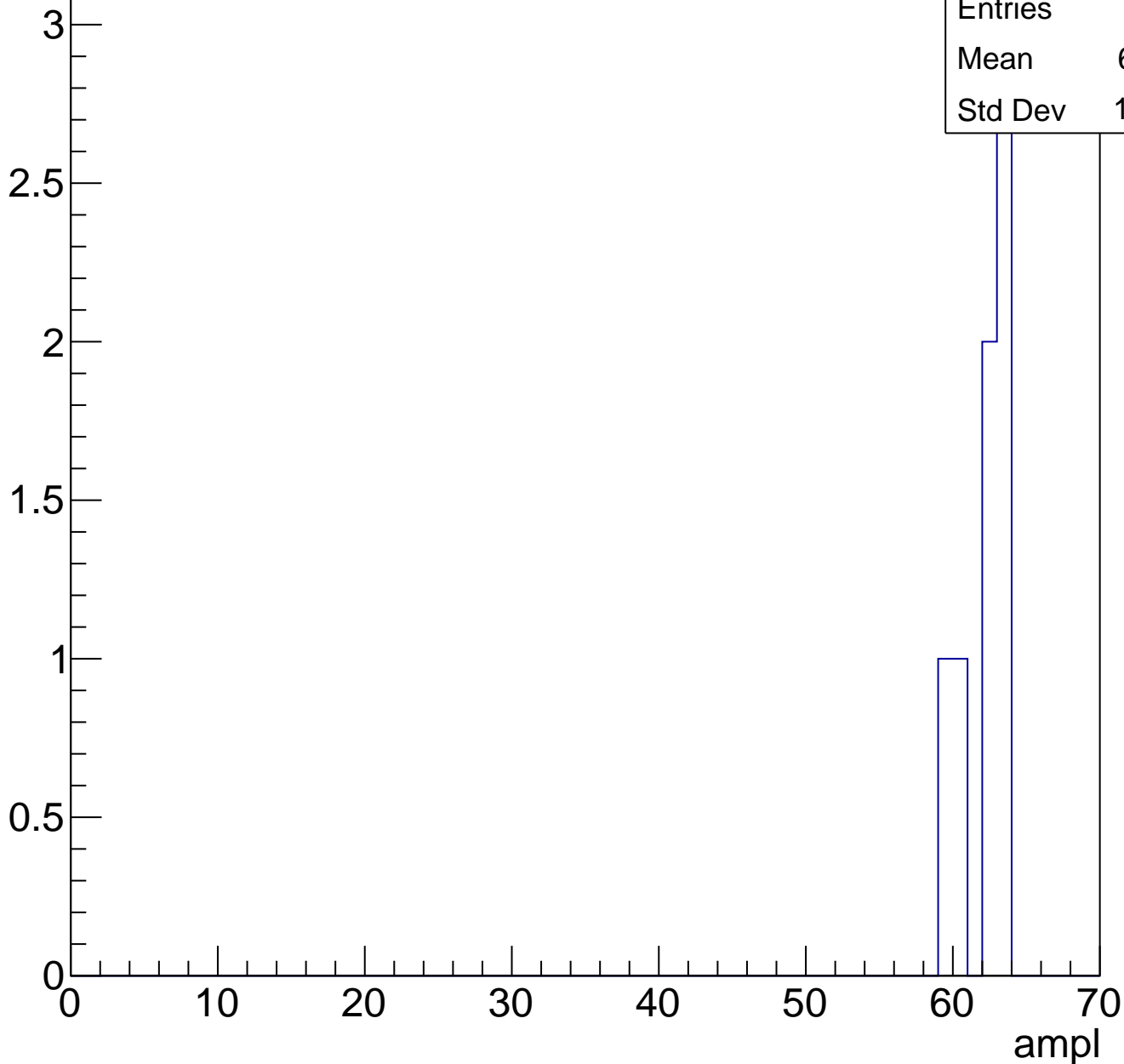
ampl



# B1L103S, U1-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

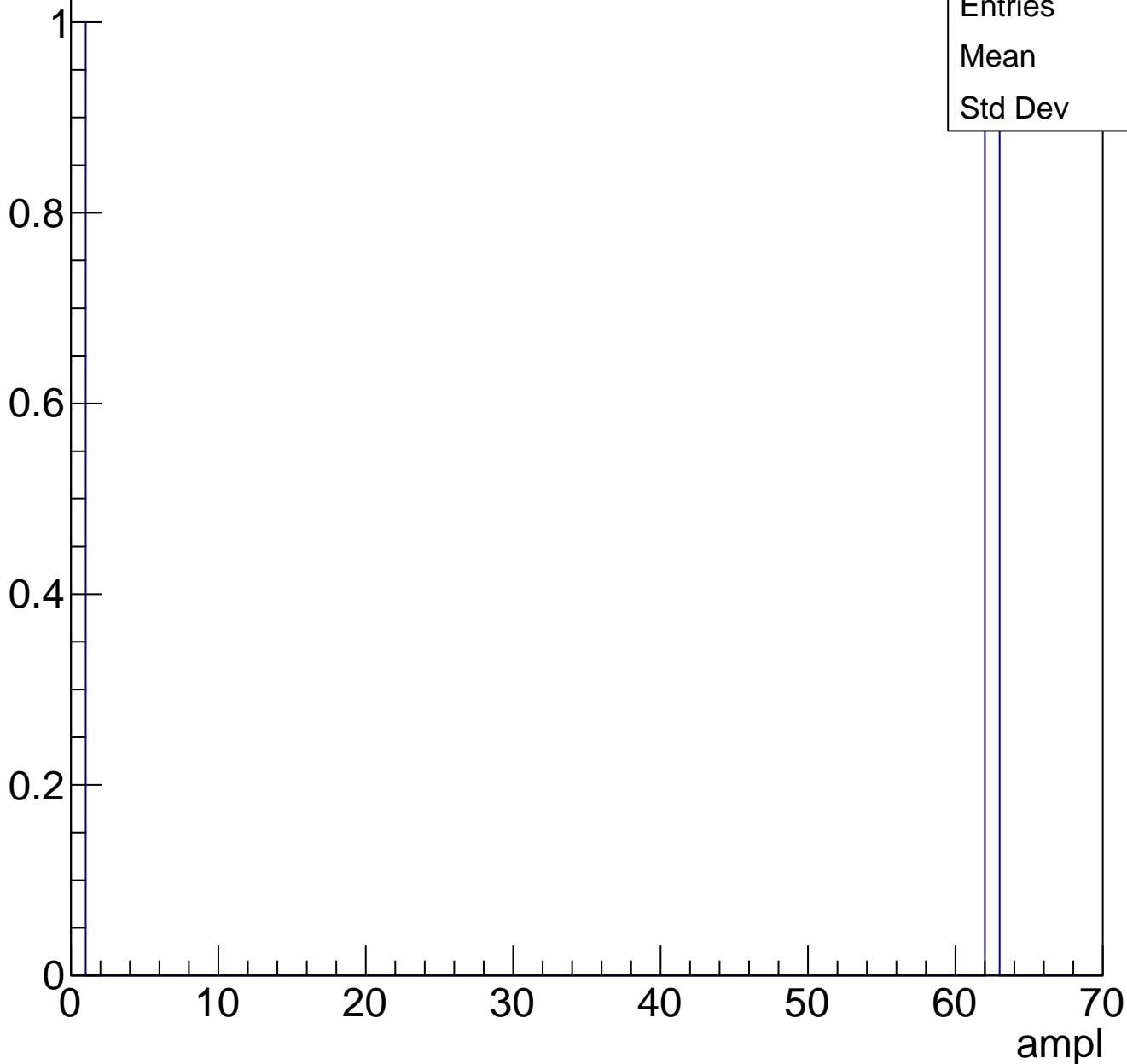




# B1L103S, U1-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch38, adc0

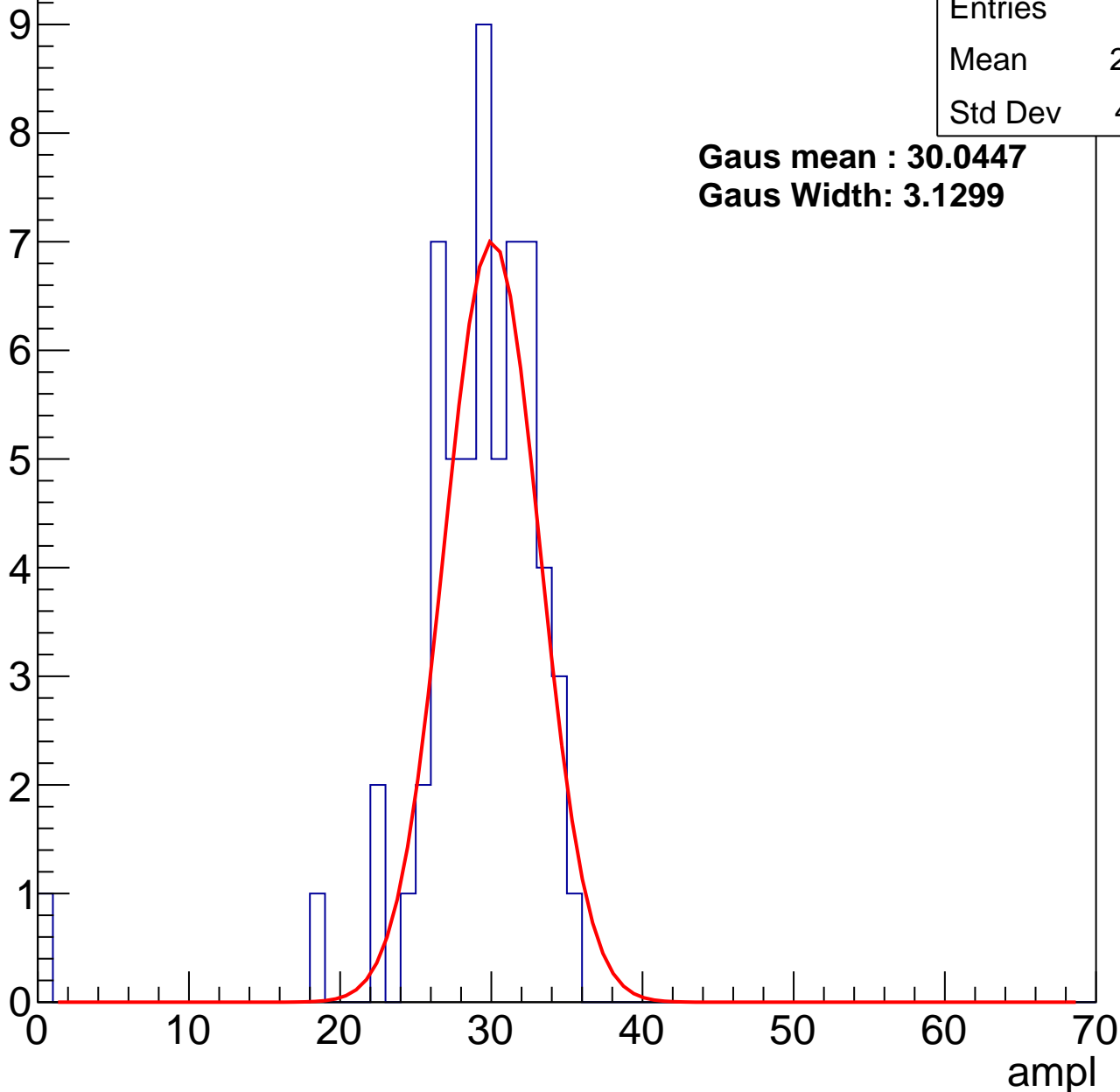
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	28.57
Std Dev	4.941

**Gaus mean : 30.0447**

**Gaus Width: 3.1299**



# B1L103S, U1-ch38, adc1

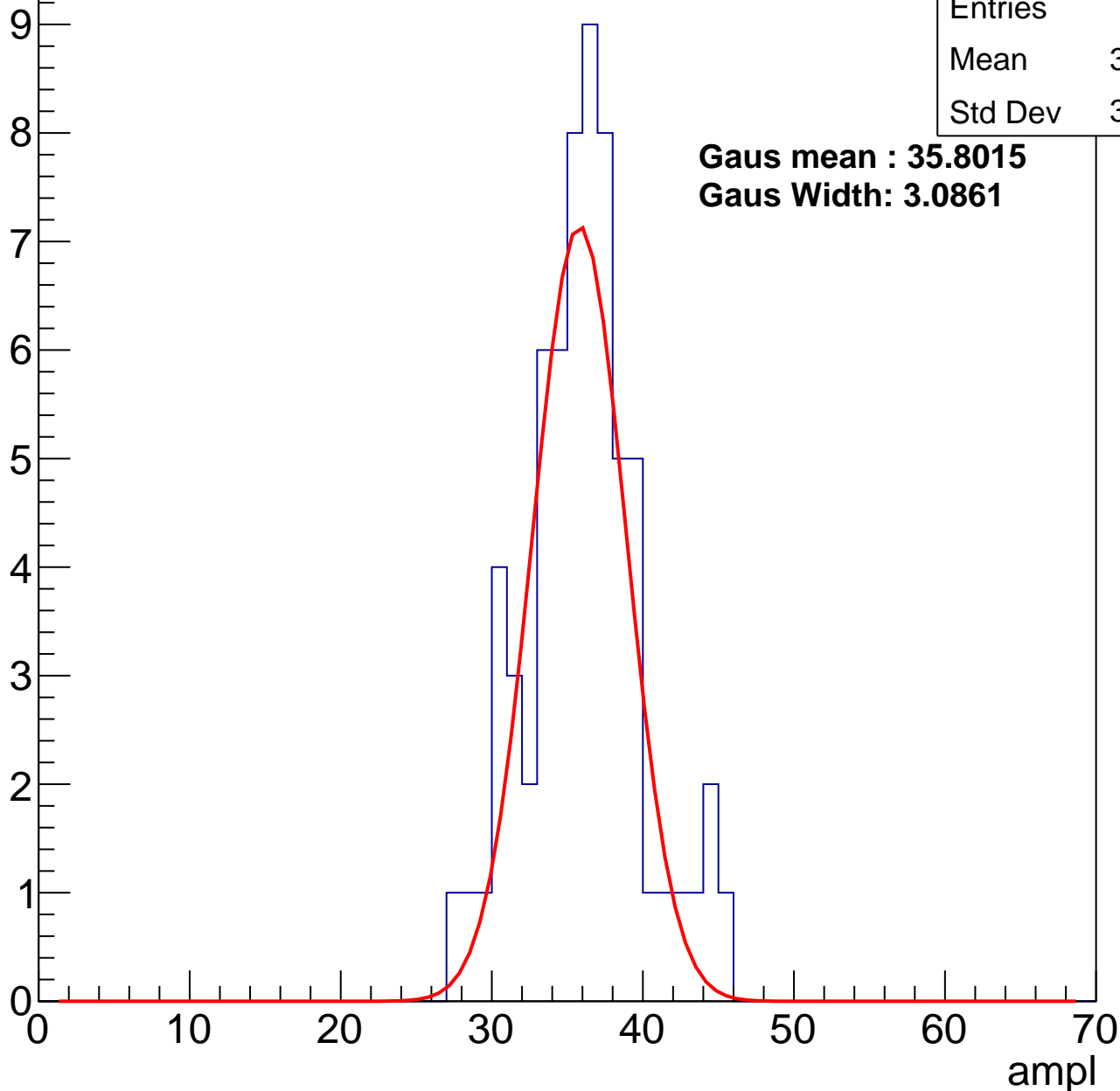
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	35.56
Std Dev	3.746

**Gaus mean : 35.8015**

**Gaus Width: 3.0861**



# B1L103S, U1-ch38, adc2

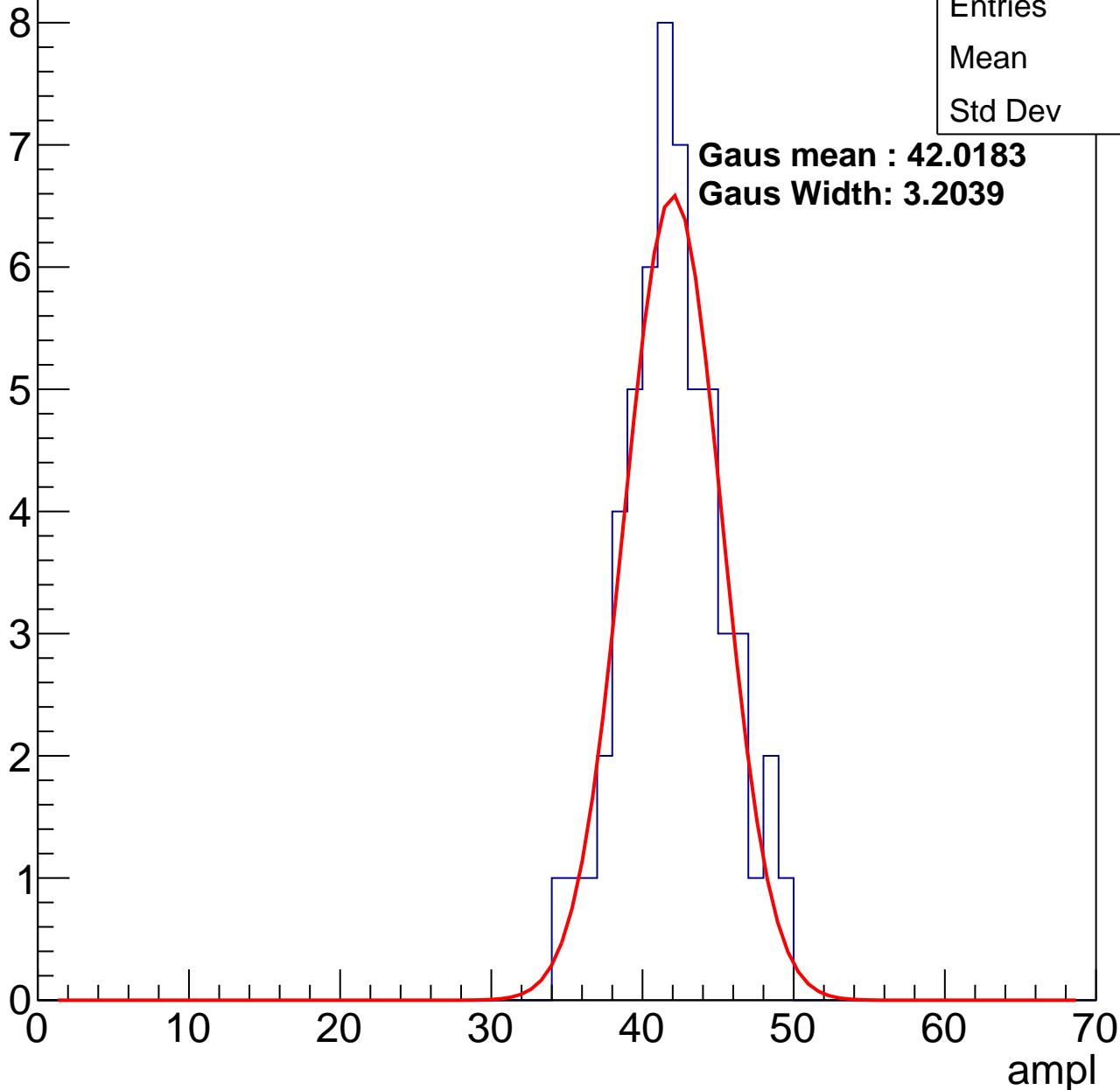
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	41.6
Std Dev	3.24

**Gaus mean : 42.0183**

**Gaus Width: 3.2039**

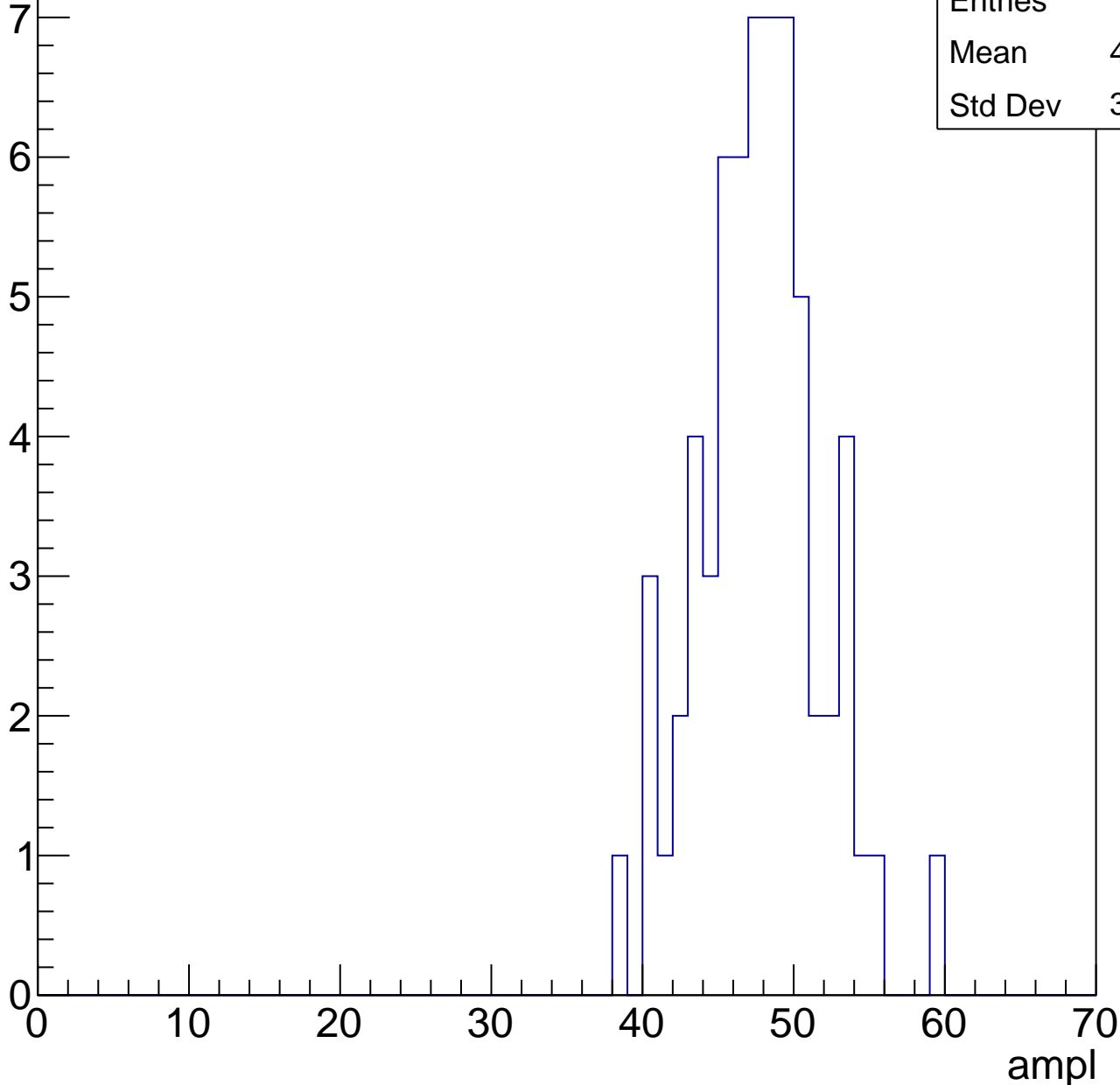


# B1L103S, U1-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

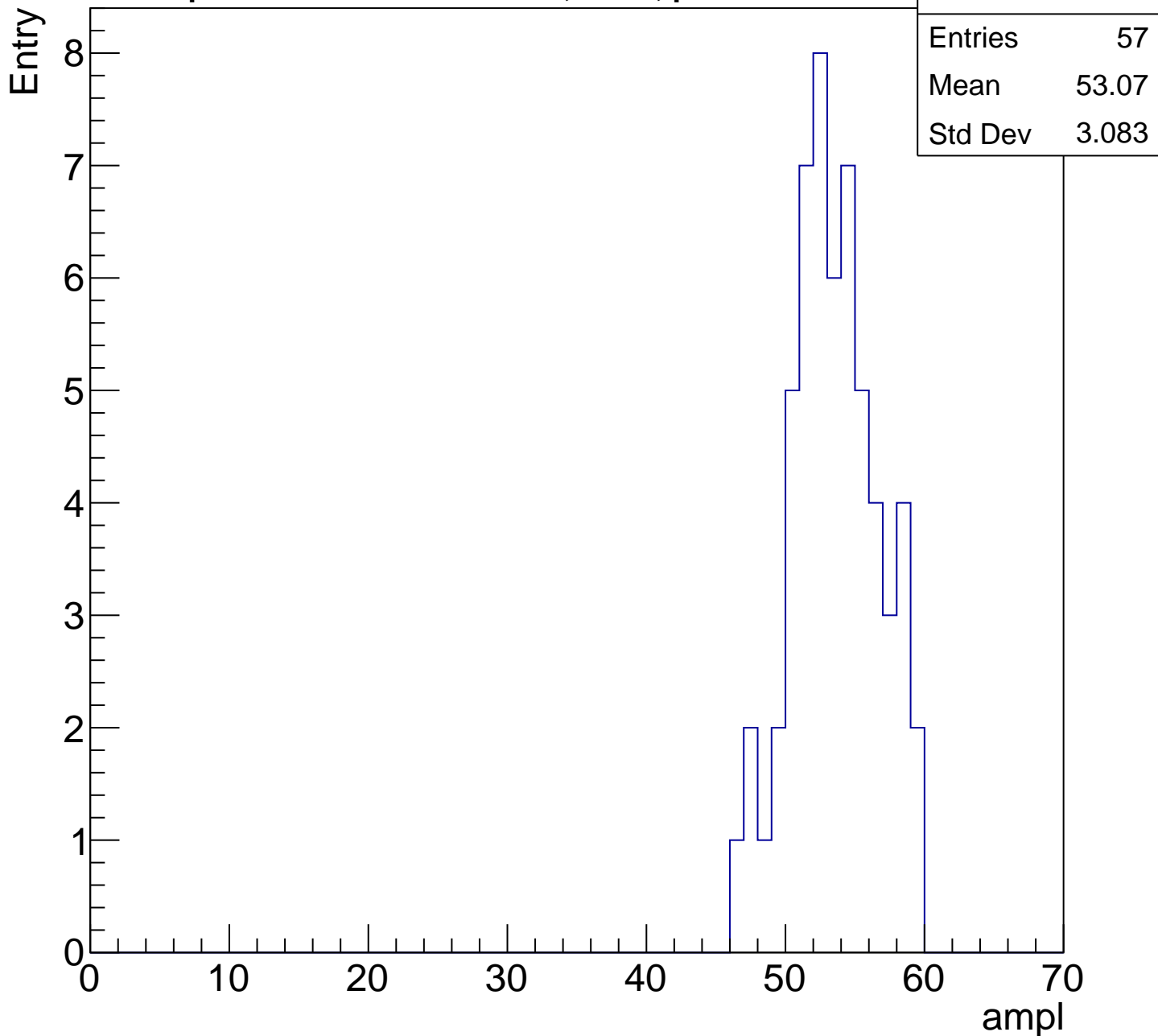
Entry

Entries	63
Mean	47.25
Std Dev	3.972



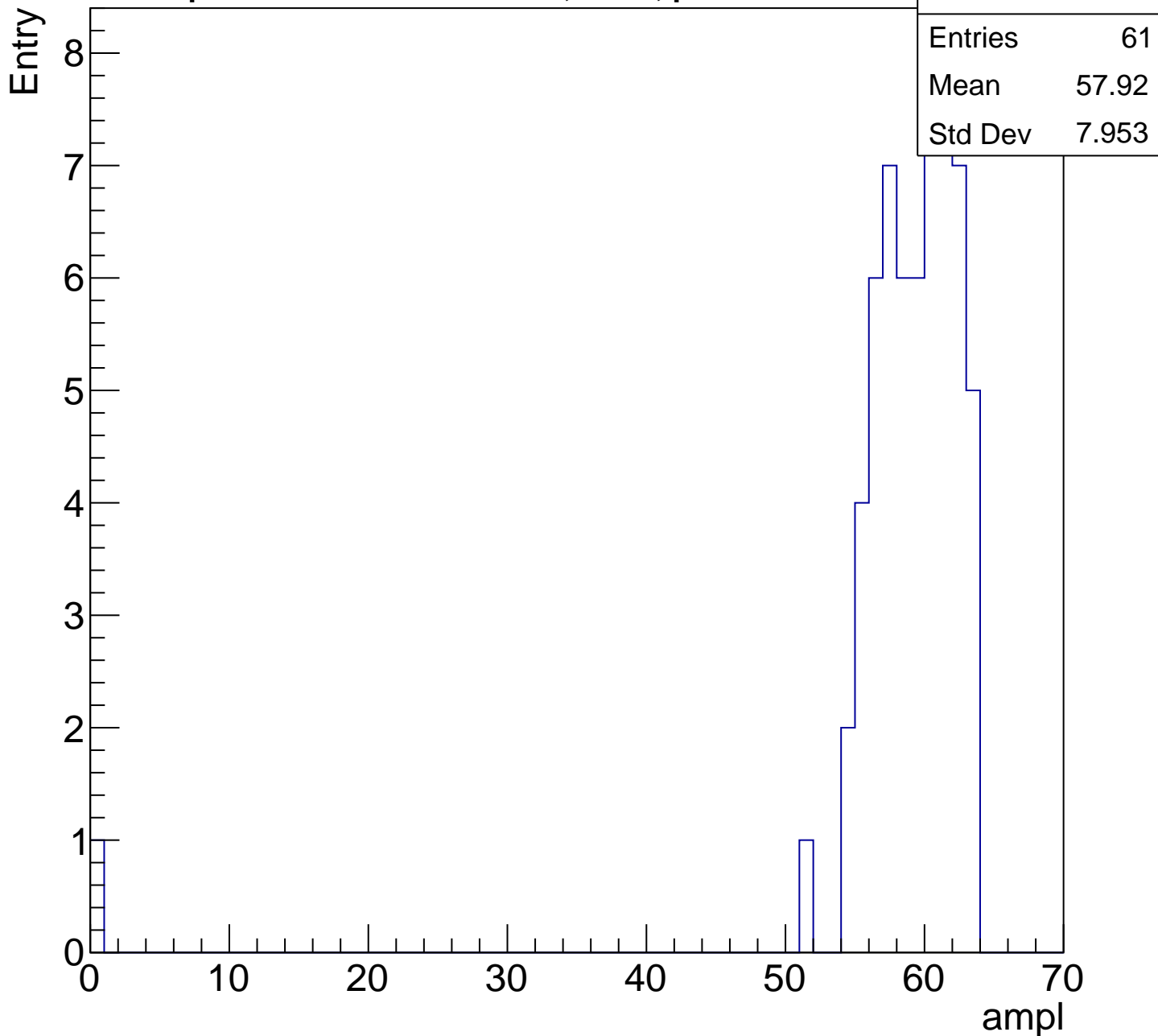
# B1L103S, U1-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U1-ch38, adc5

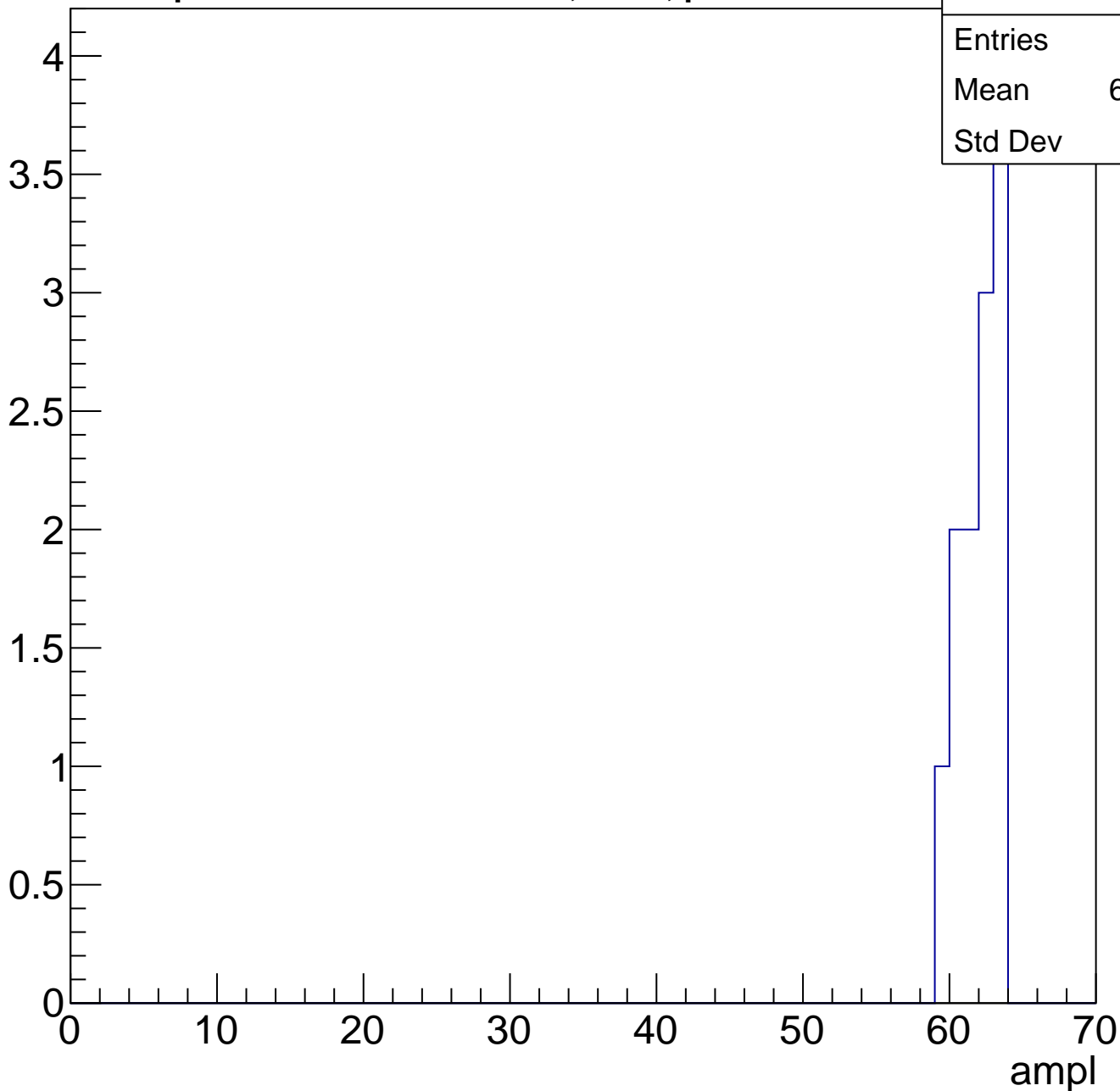
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U1-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U1-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

1

Mean

63

Std Dev

0

# B1L103S, U1-ch39, adc0

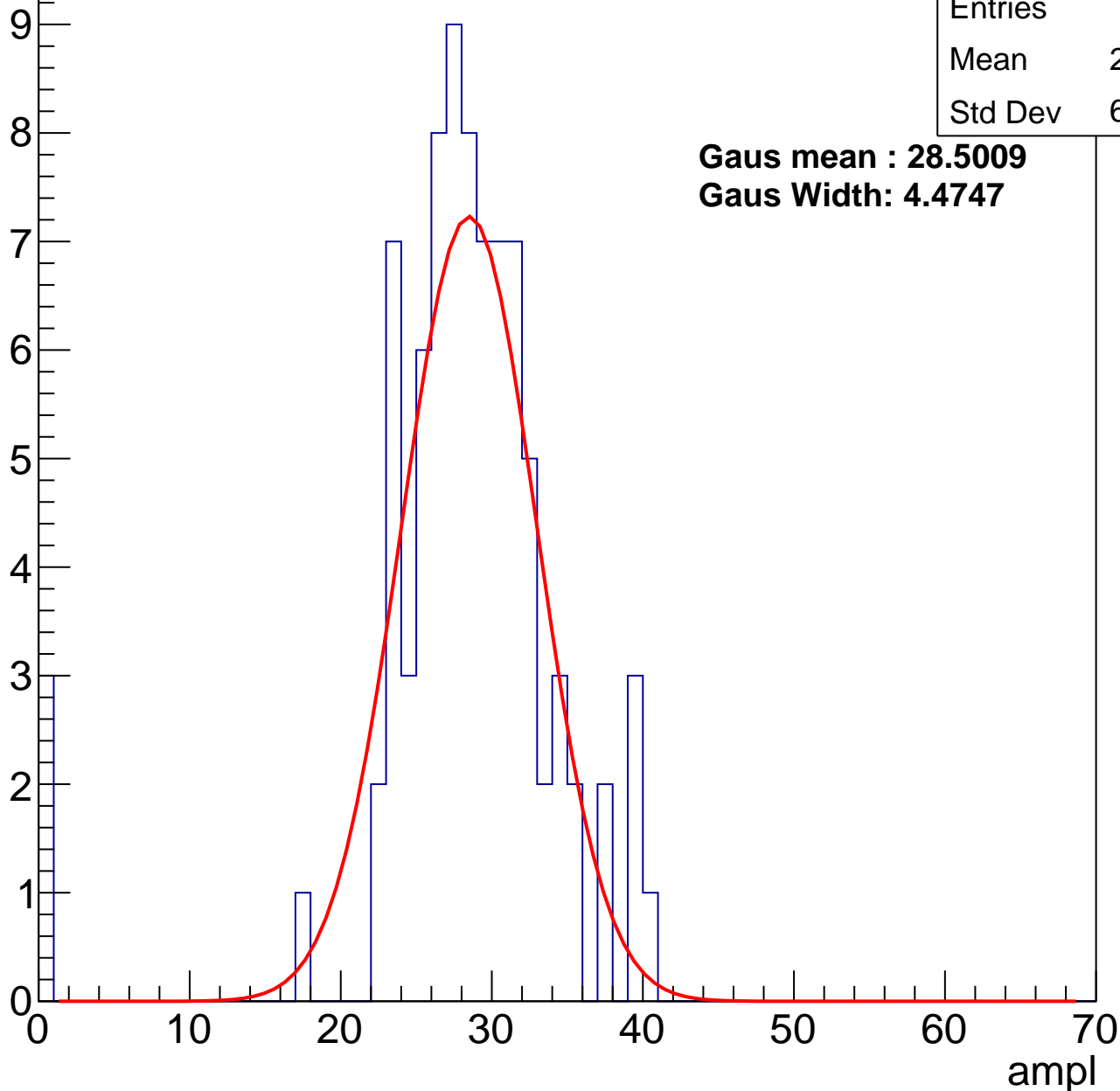
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	86
Mean	27.65
Std Dev	6.782

**Gaus mean : 28.5009**

**Gaus Width: 4.4747**



# B1L103S, U1-ch39, adc1

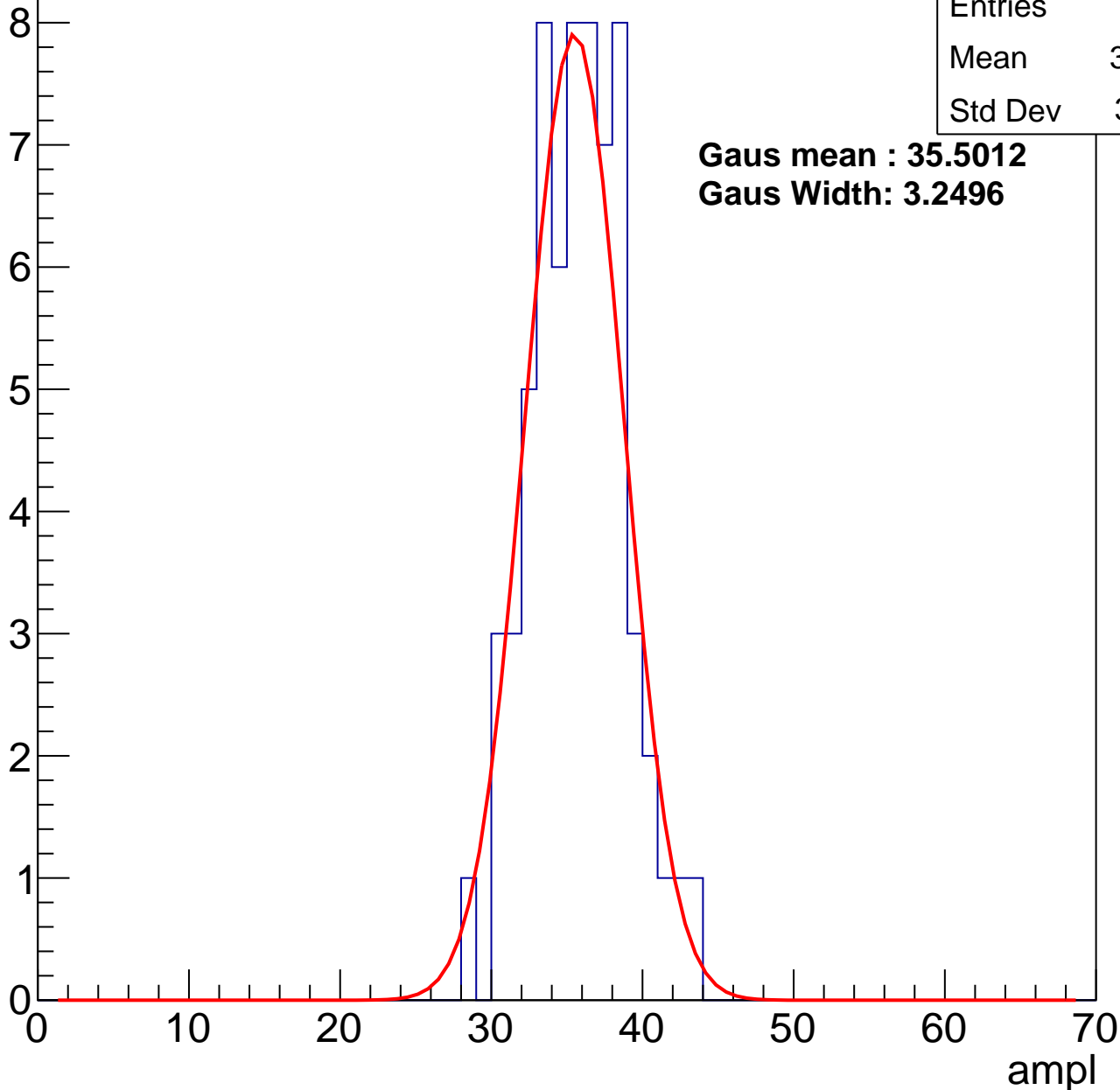
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	35.28
Std Dev	3.051

**Gaus mean : 35.5012**

**Gaus Width: 3.2496**



# B1L103S, U1-ch39, adc2

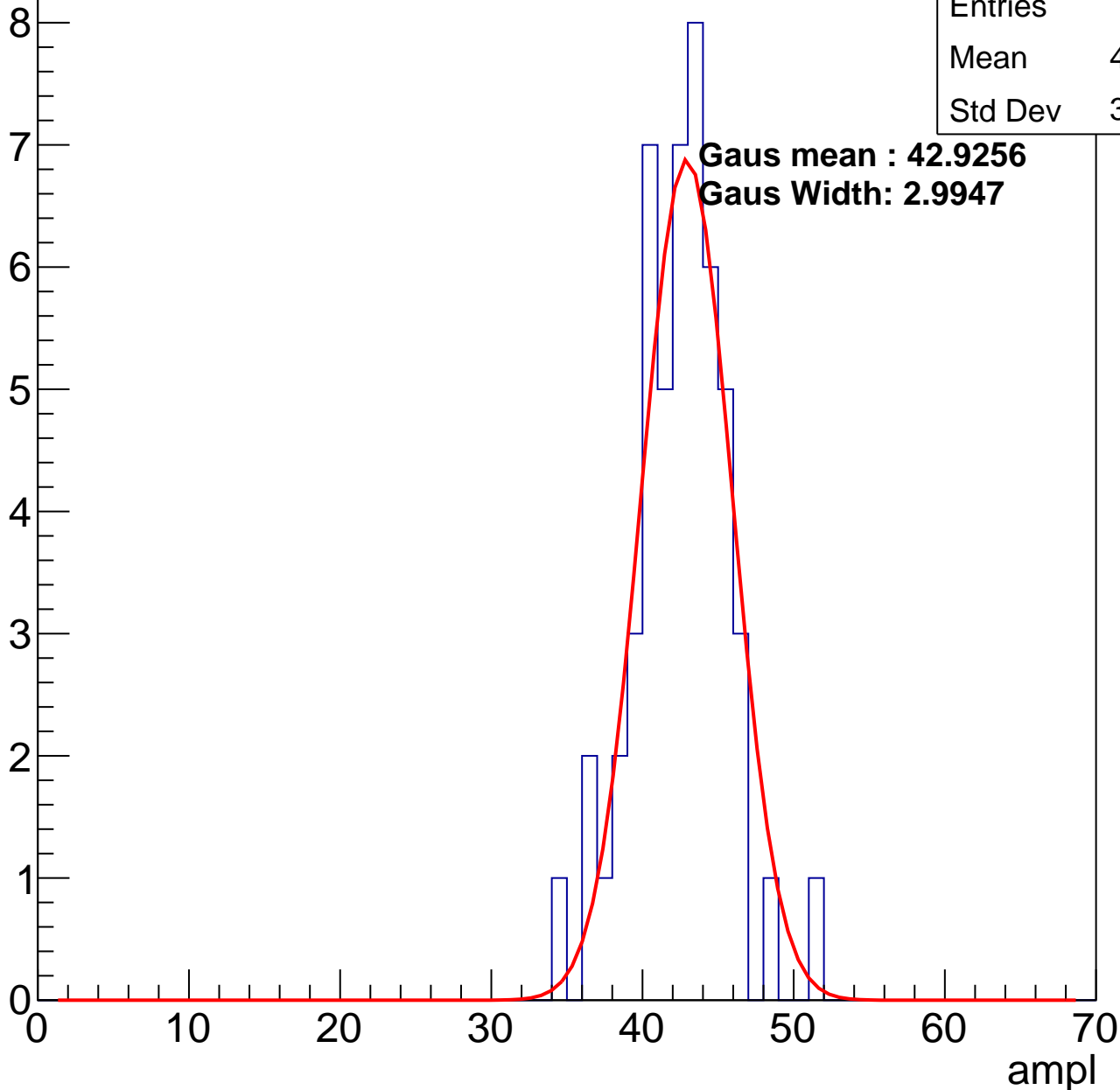
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	42.02
Std Dev	3.085

**Gaus mean : 42.9256**

**Gaus Width: 2.9947**

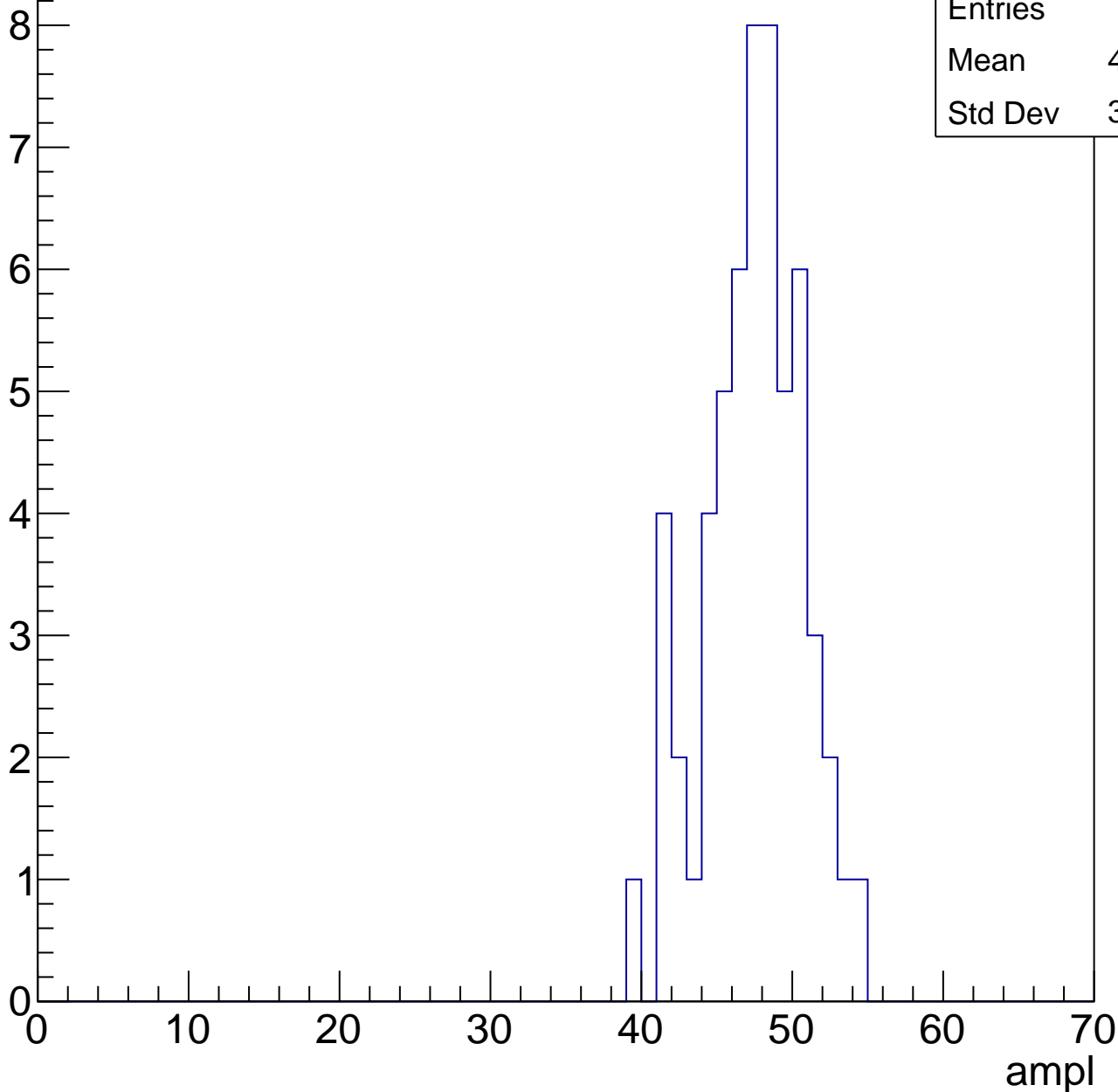


# B1L103S, U1-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	46.95
Std Dev	3.247

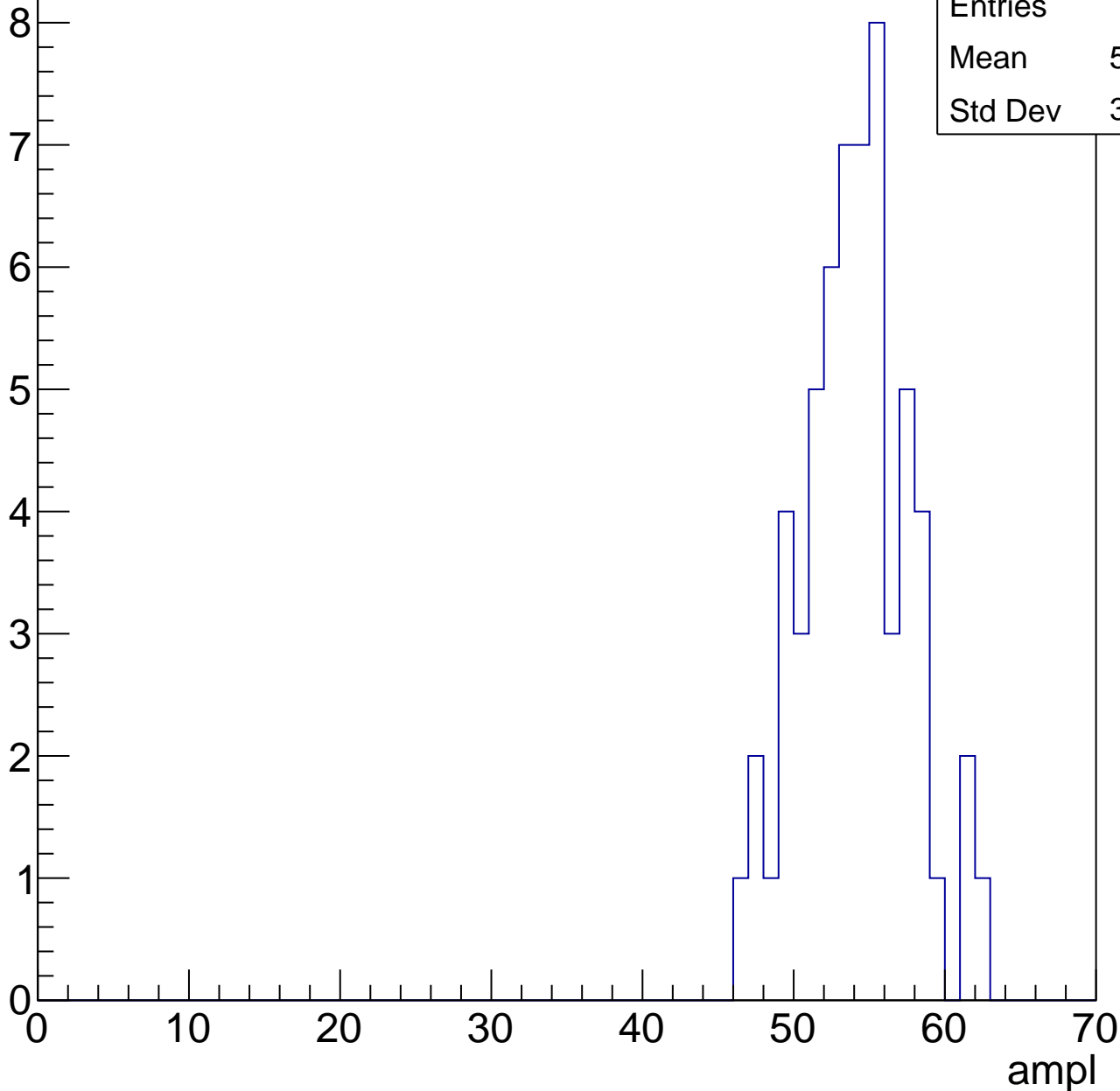


# B1L103S, U1-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

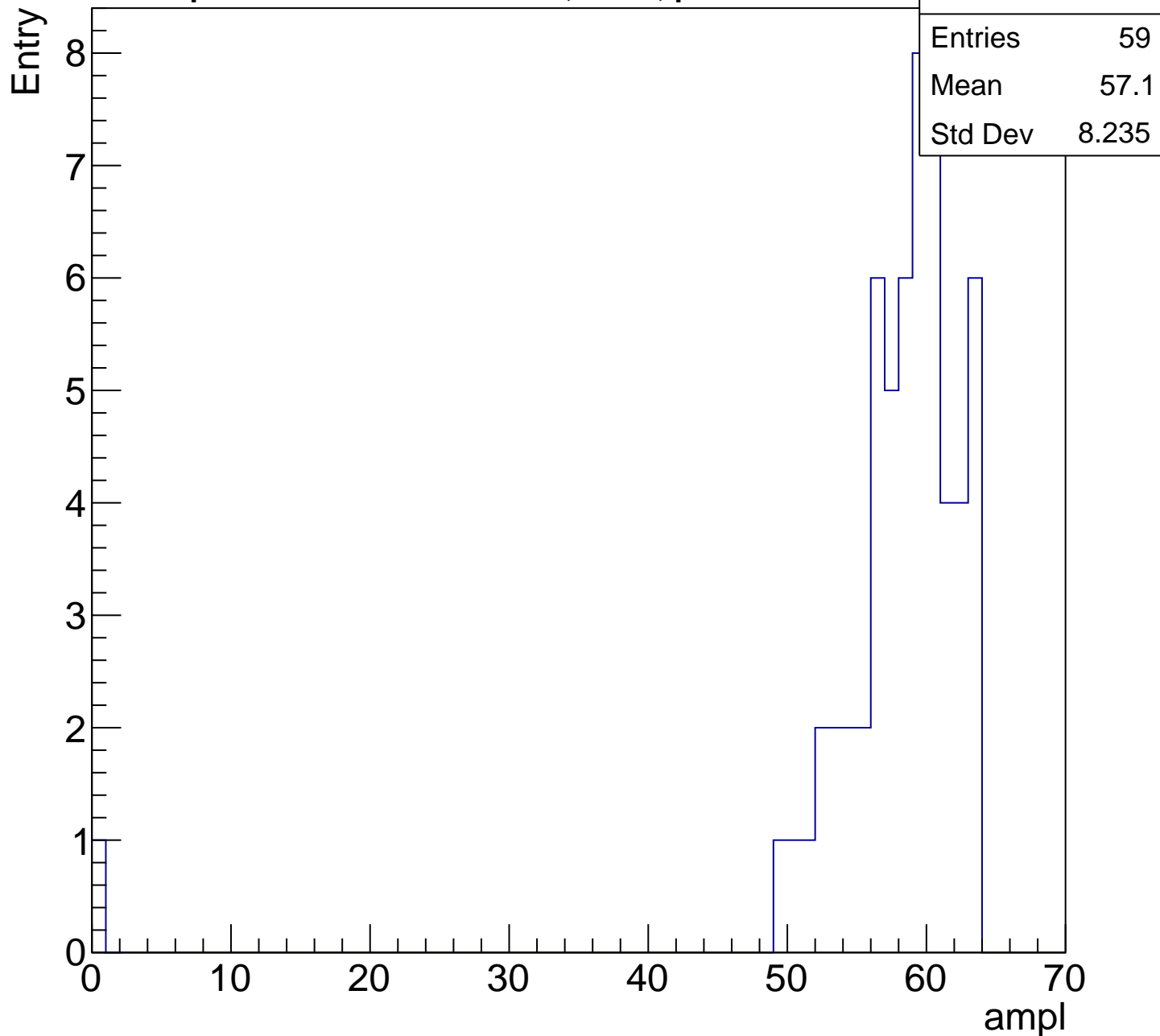
Entry

Entries	60
Mean	53.63
Std Dev	3.488



# B1L103S, U1-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

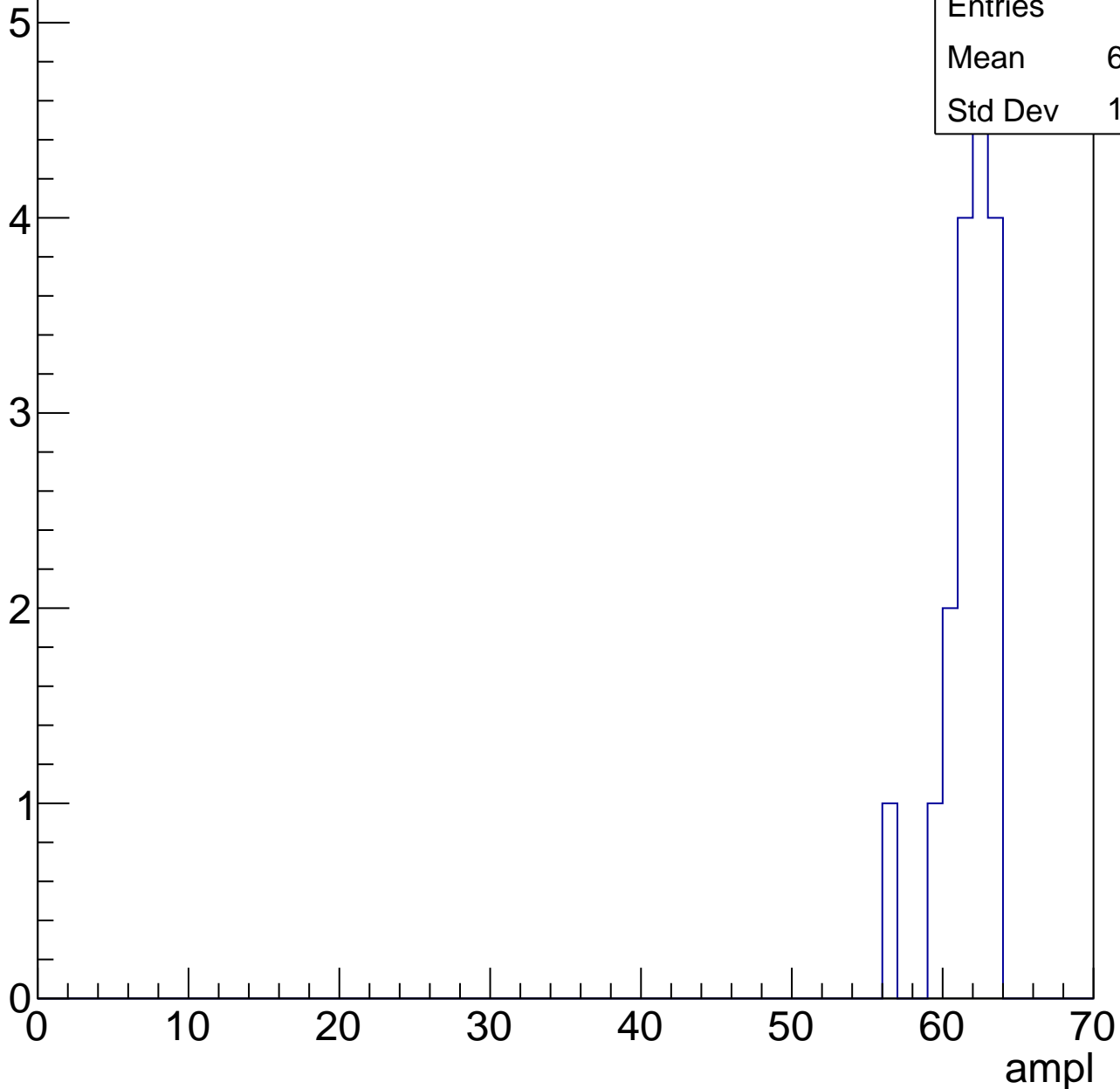


# B1L103S, U1-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	17
Mean	61.24
Std Dev	1.733





# B1L103S, U1-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U1-ch40, adc0

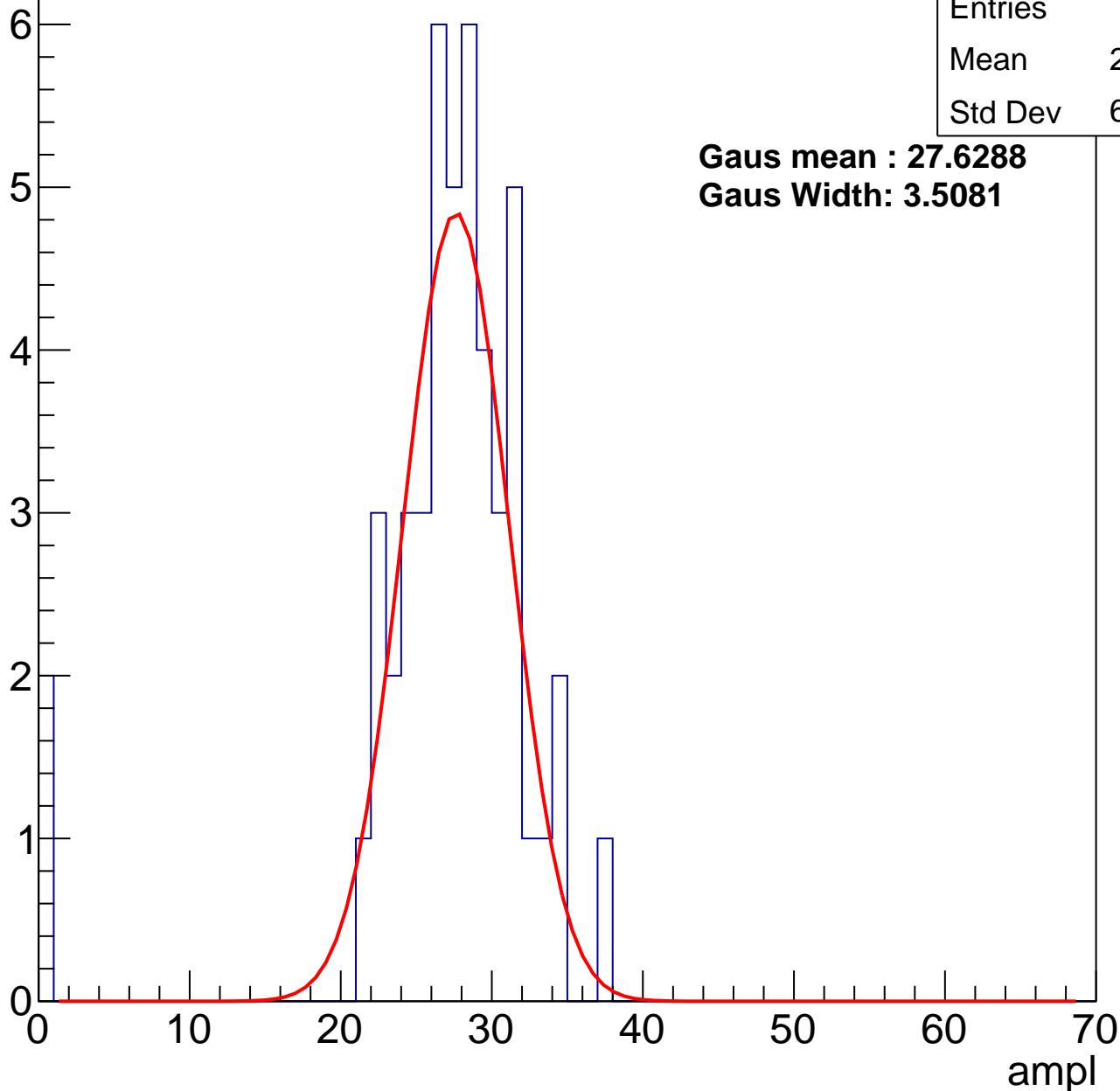
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	26.46
Std Dev	6.487

**Gaus mean : 27.6288**

**Gaus Width: 3.5081**



# B1L103S, U1-ch40, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	85
Mean	33.4
Std Dev	5.27

**Gaus mean : 33.8808**

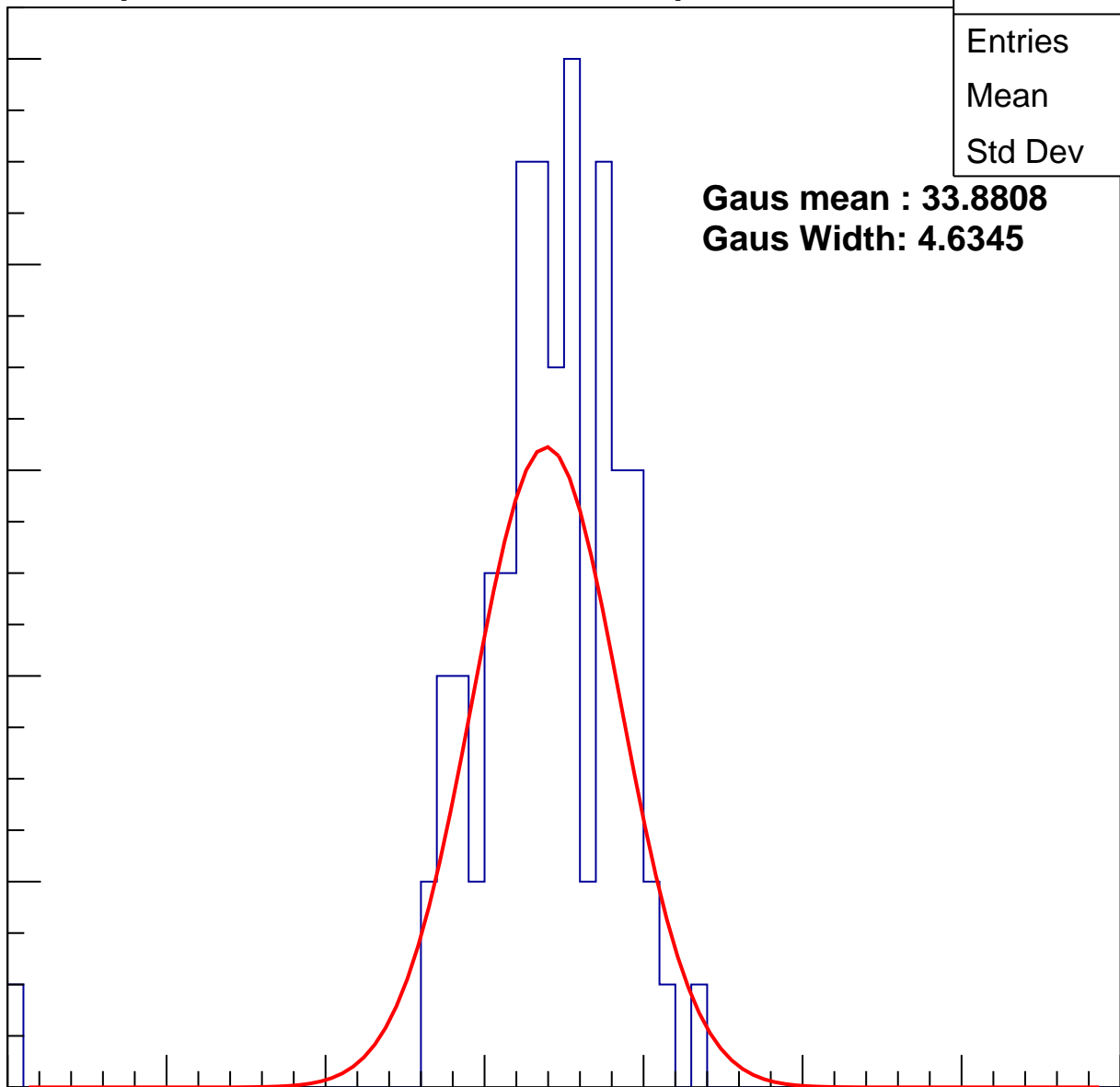
**Gaus Width: 4.6345**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U1-ch40, adc2

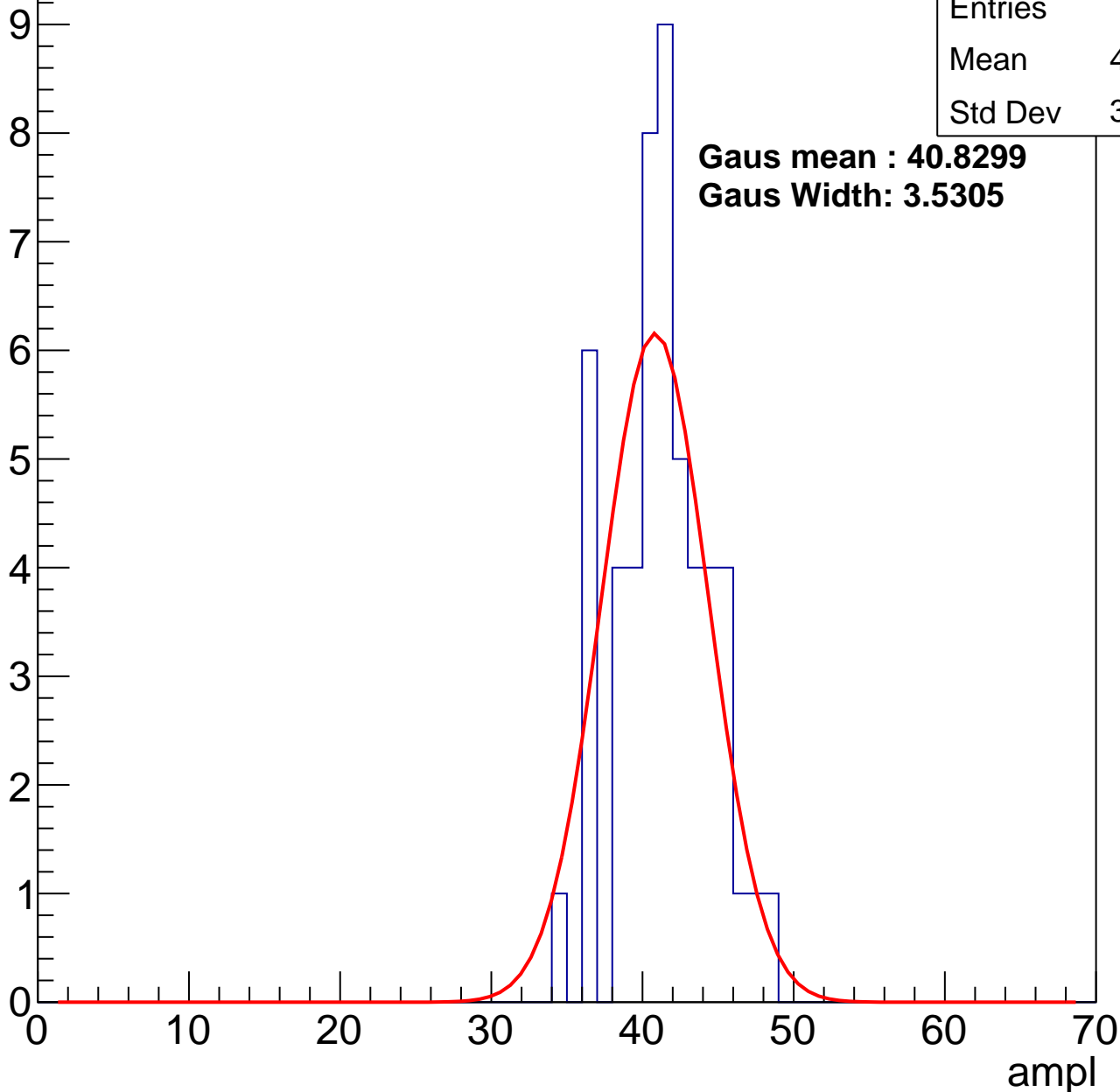
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	40.88
Std Dev	3.068

**Gaus mean : 40.8299**

**Gaus Width: 3.5305**

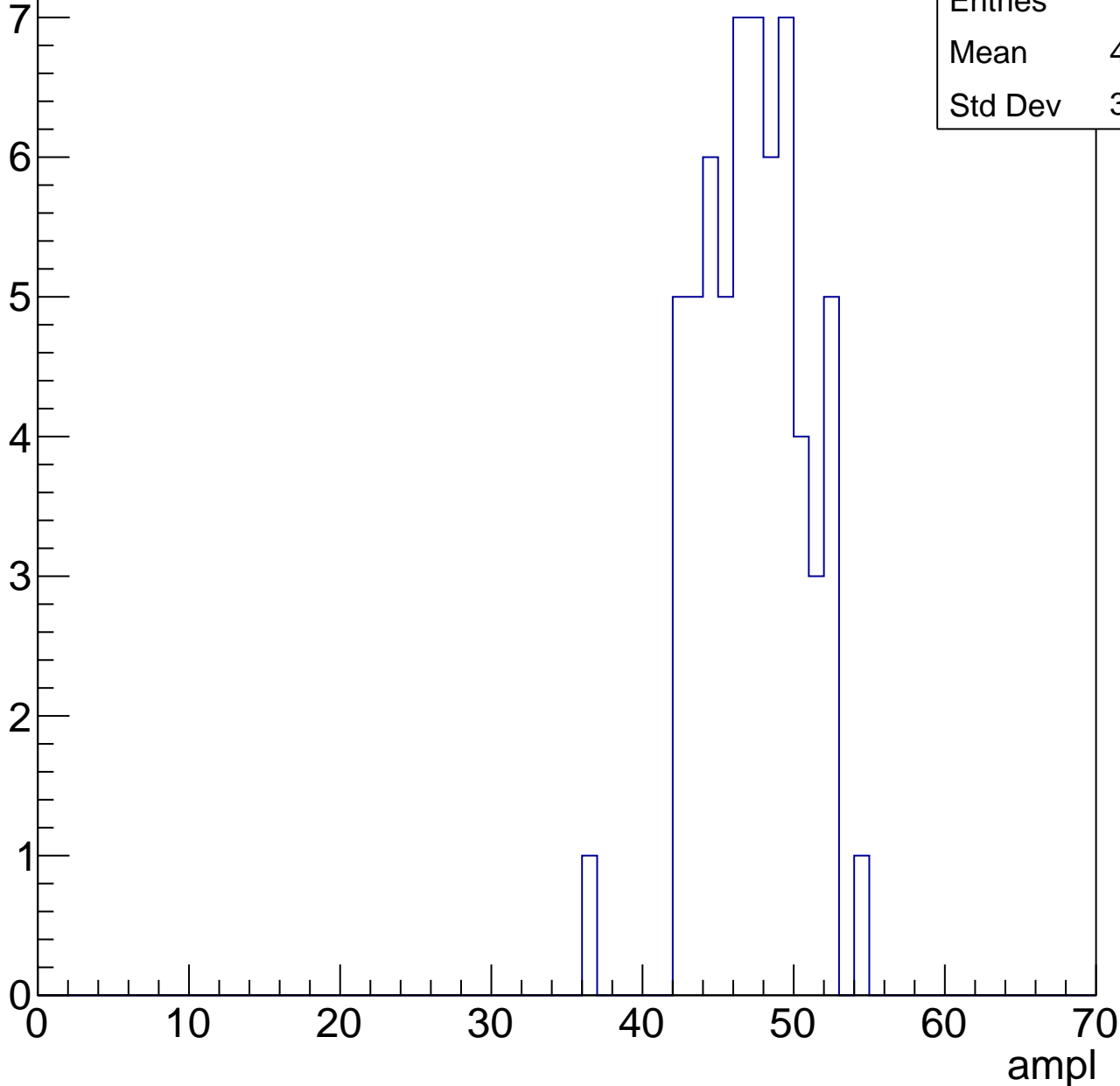


# B1L103S, U1-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	46.76
Std Dev	3.349

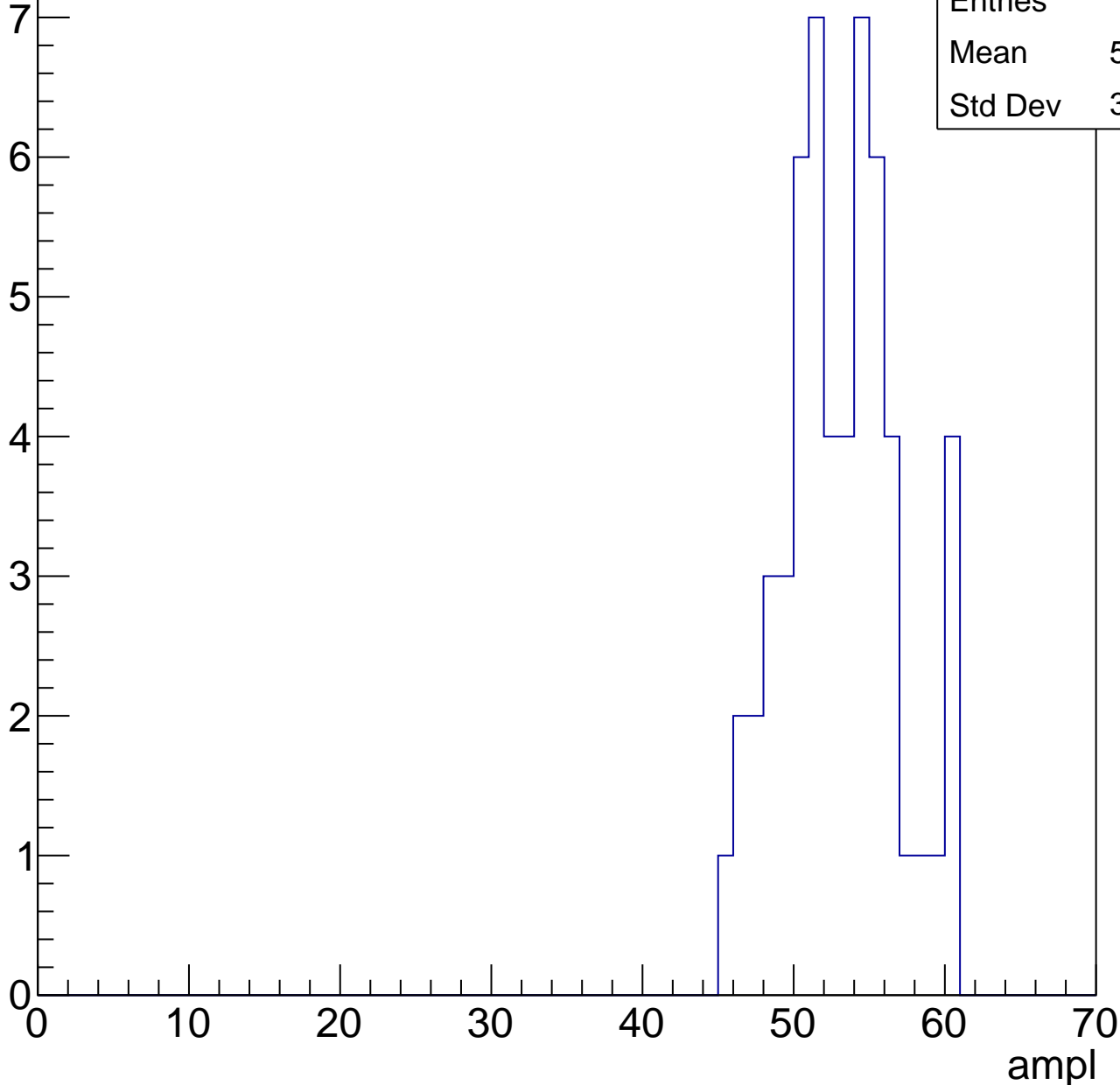


# B1L103S, U1-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	52.59
Std Dev	3.717

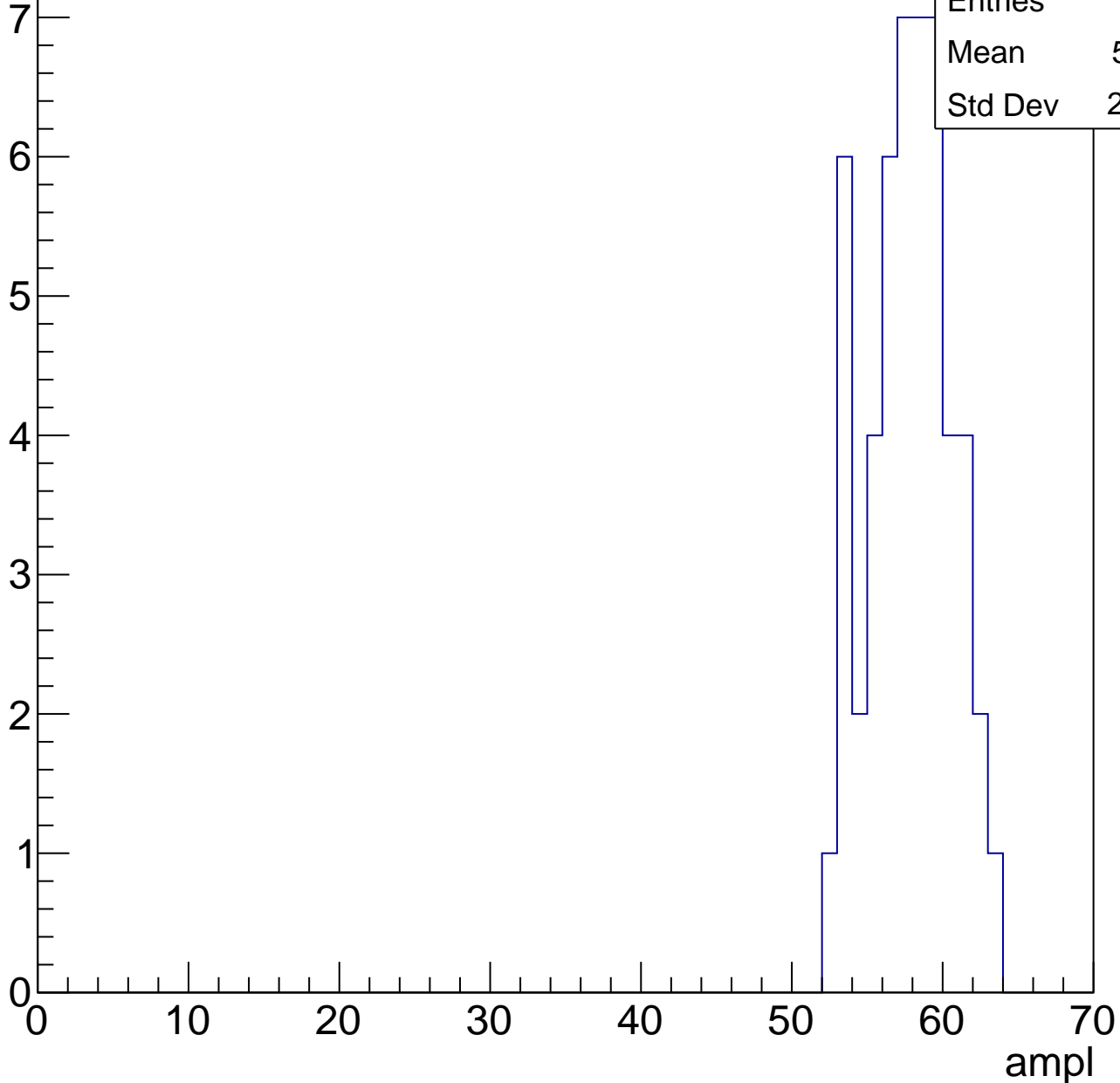


# B1L103S, U1-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	57.31
Std Dev	2.719

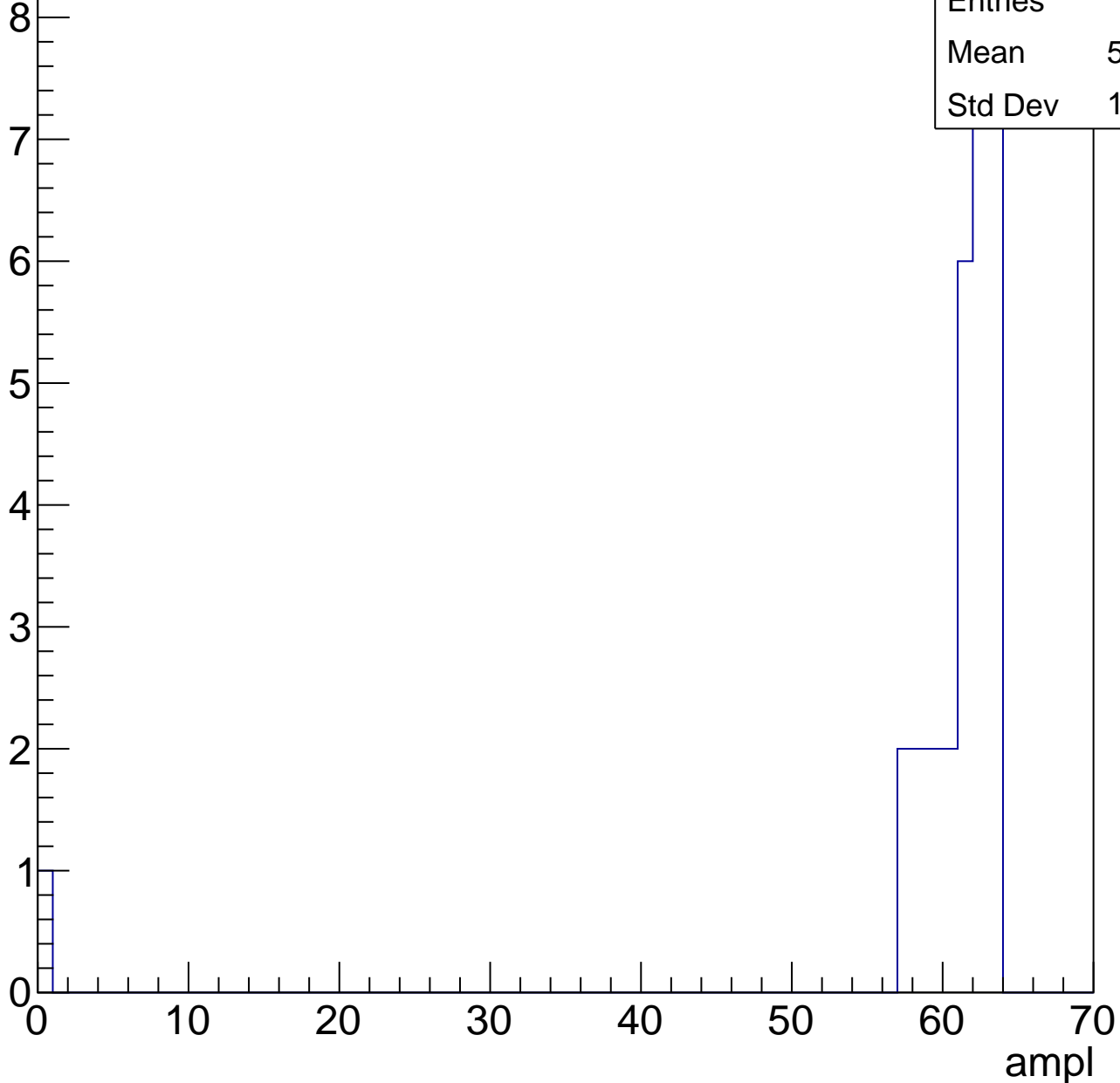


# B1L103S, U1-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	31
Mean	59.16
Std Dev	10.95





# B1L103S, U1-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch41, adc0

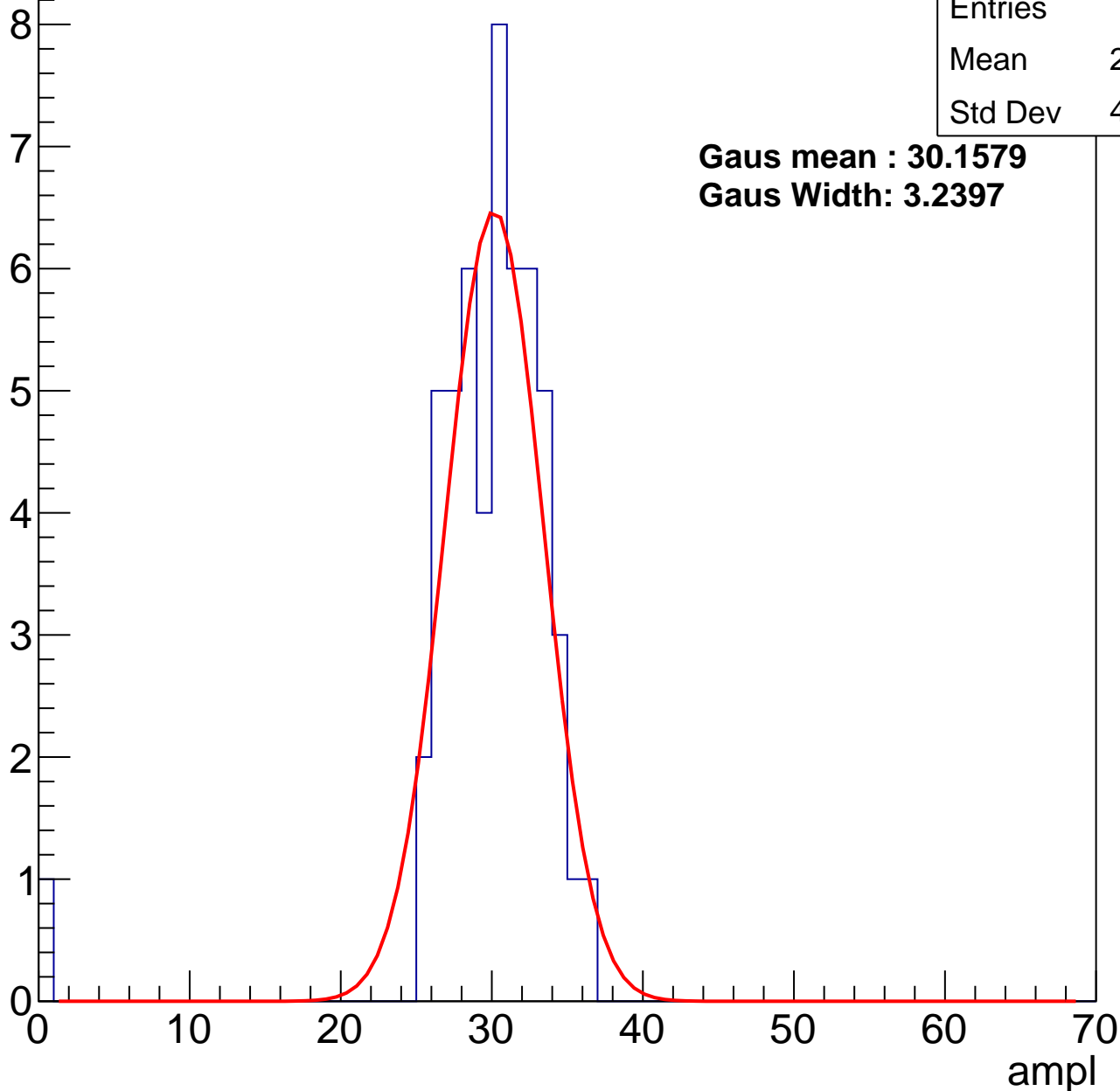
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	29.34
Std Dev	4.883

**Gaus mean : 30.1579**

**Gaus Width: 3.2397**



# B1L103S, U1-ch41, adc1

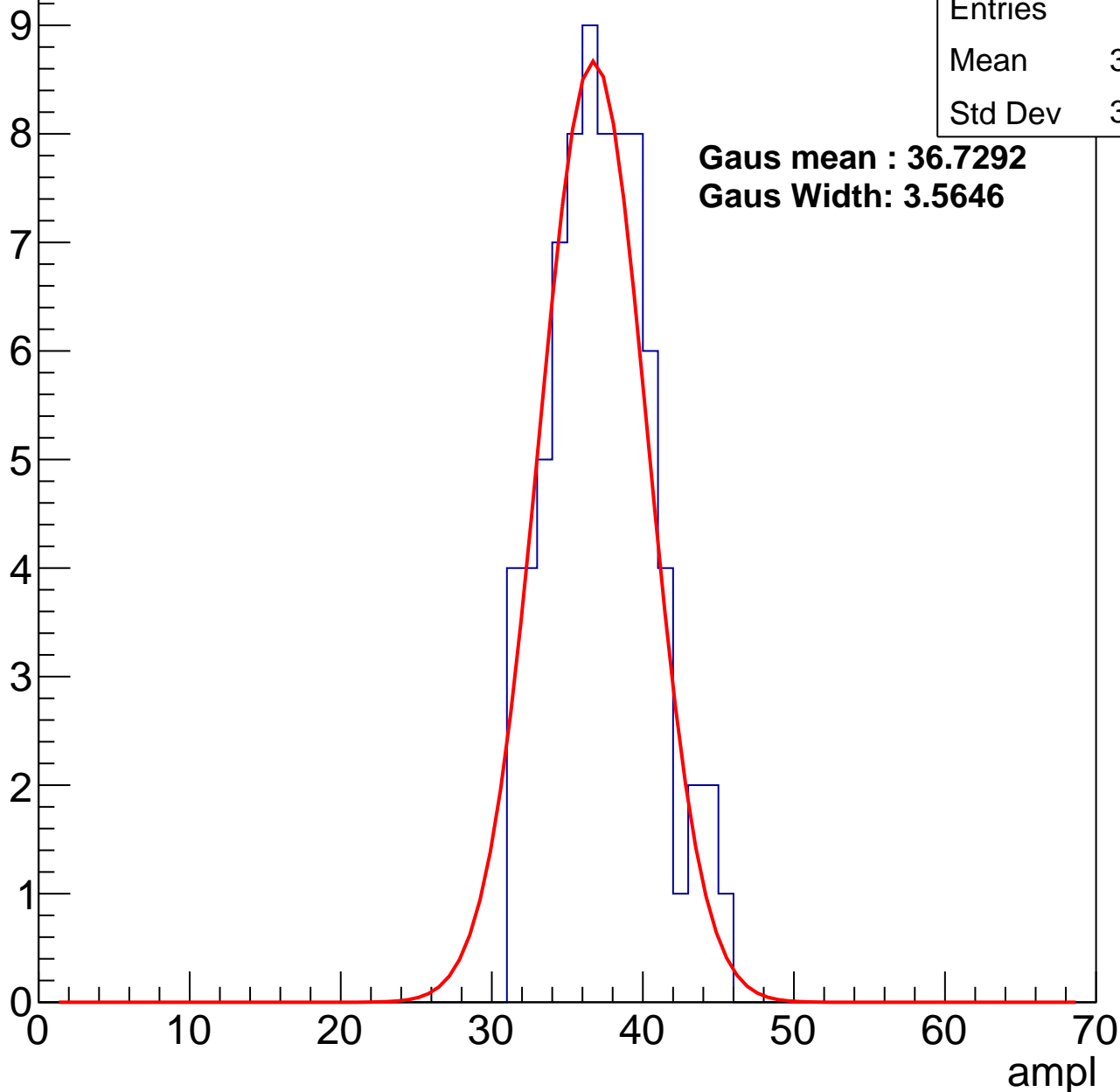
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	36.83
Std Dev	3.308

**Gaus mean : 36.7292**

**Gaus Width: 3.5646**



# B1L103S, U1-ch41, adc2

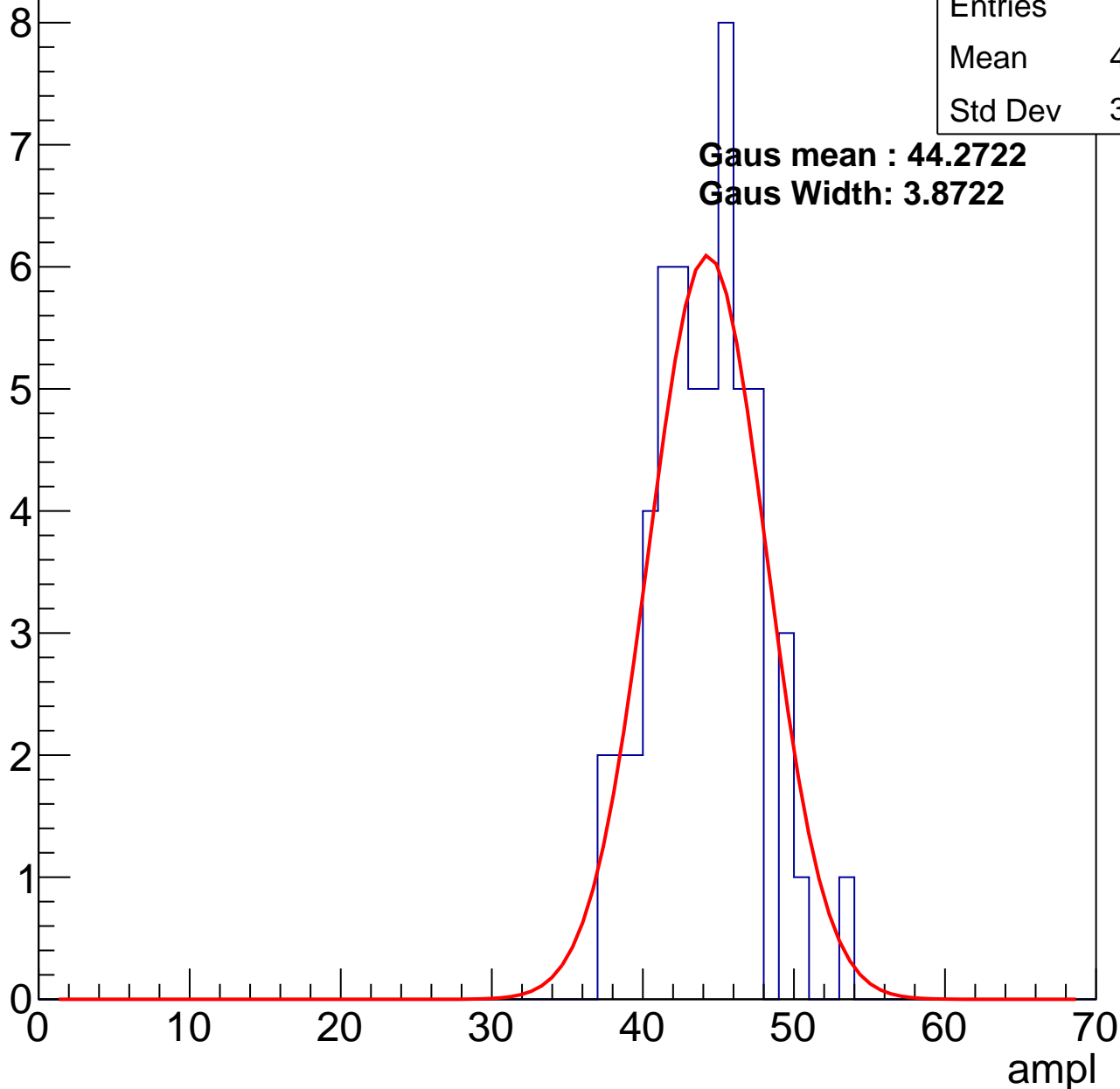
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	43.56
Std Dev	3.362

**Gaus mean : 44.2722**

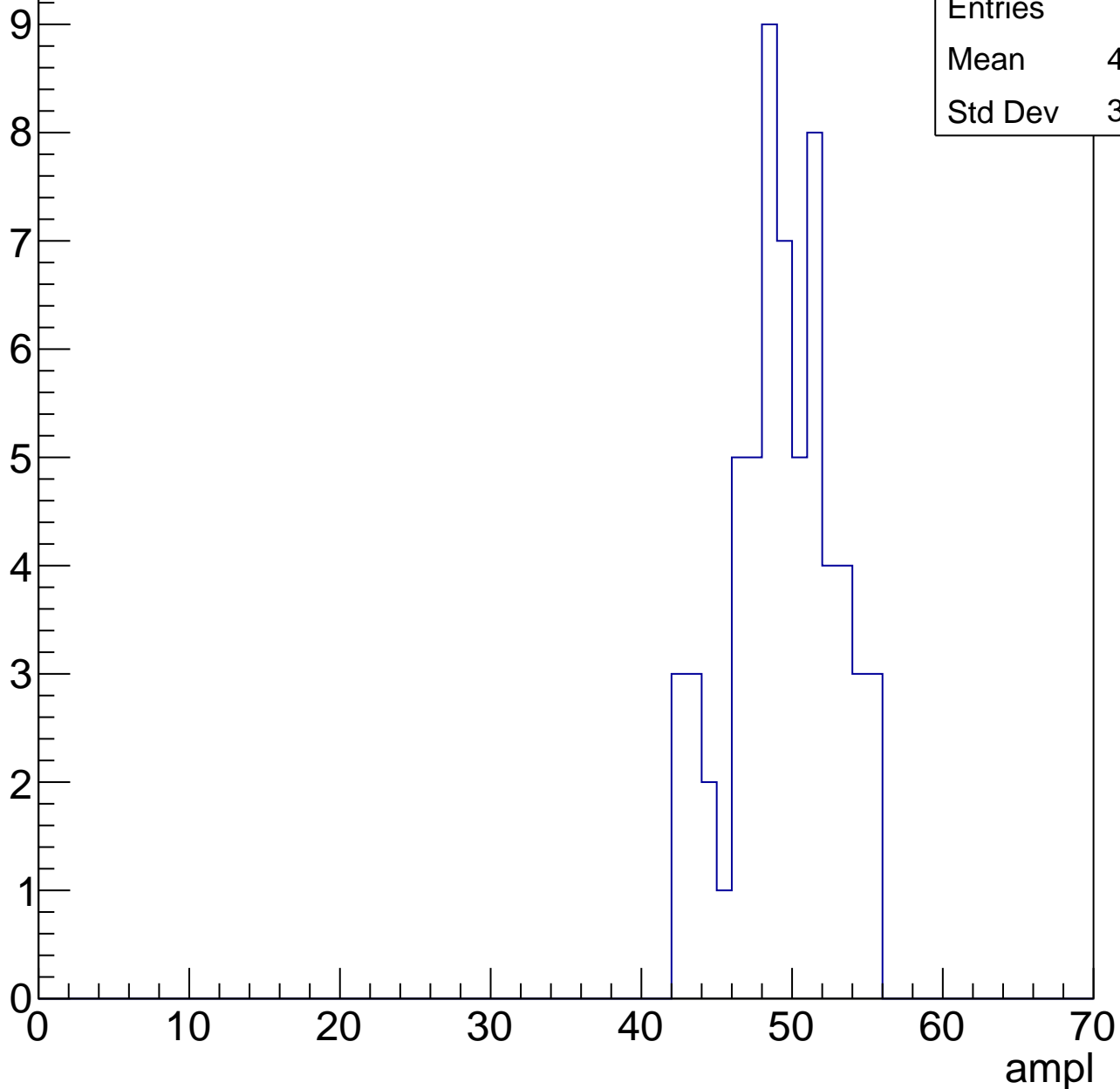
**Gaus Width: 3.8722**



# B1L103S, U1-ch41, adc3

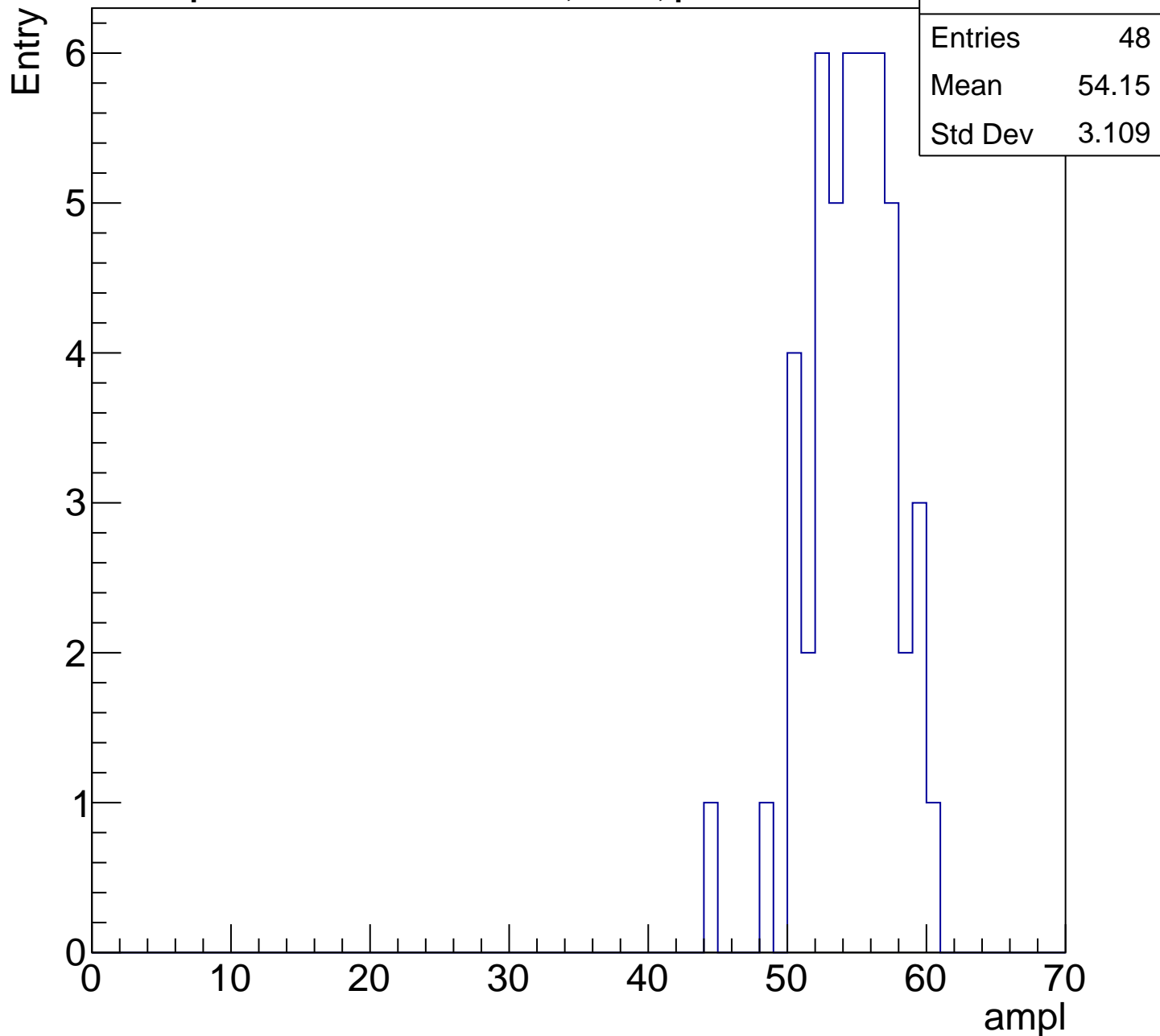
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

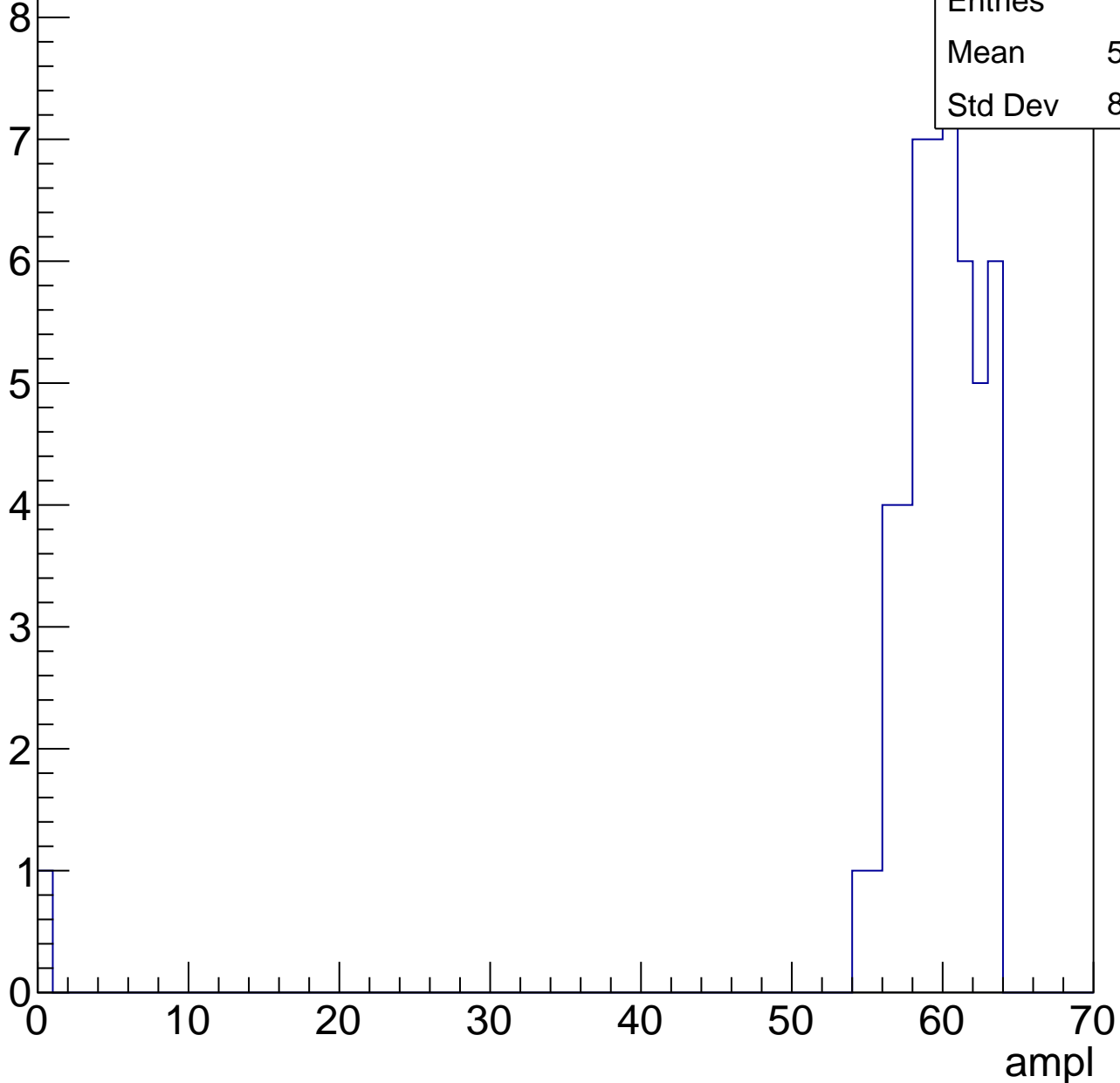


# B1L103S, U1-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	58.28
Std Dev	8.635

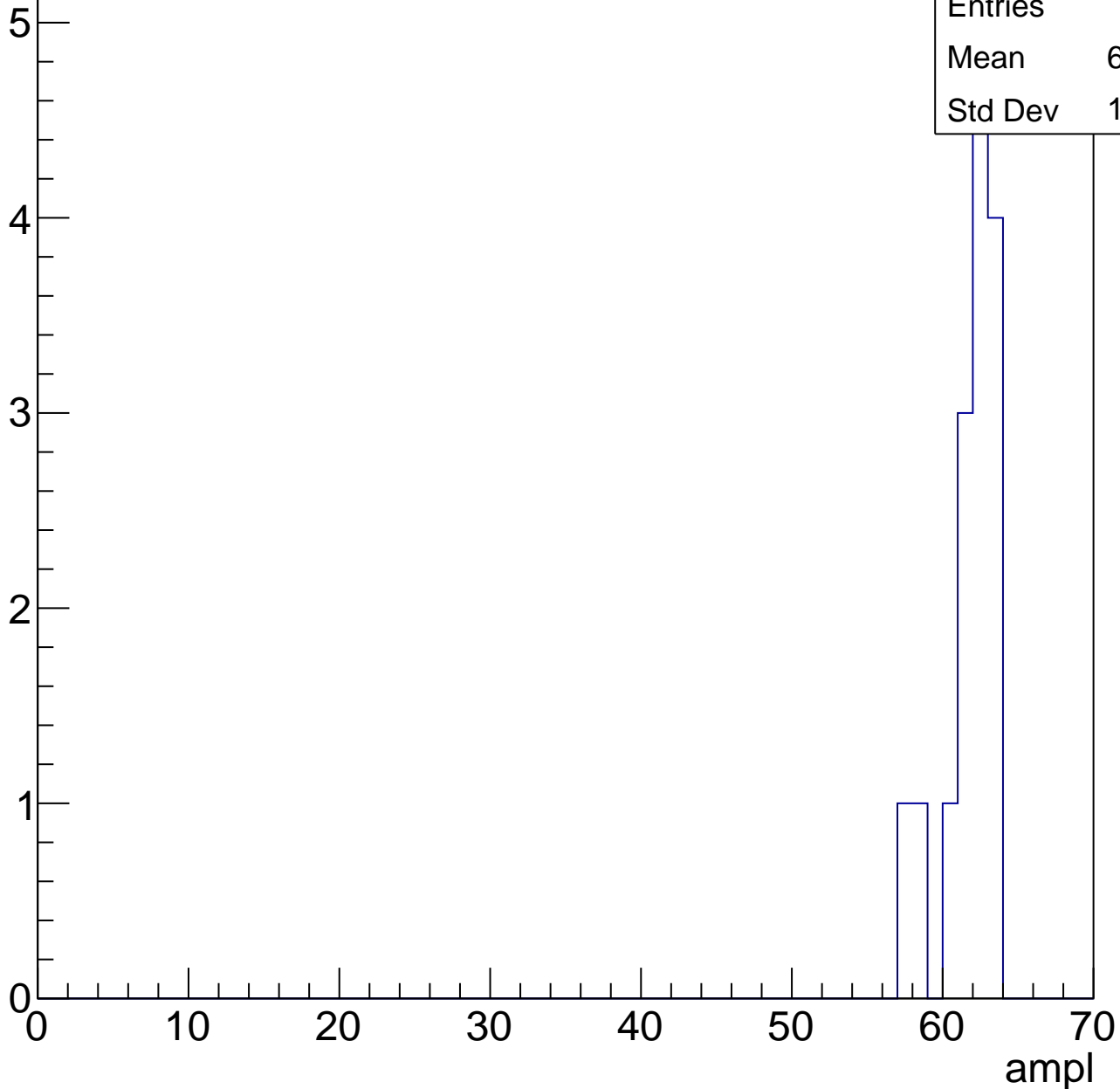


# B1L103S, U1-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	15
Mean	61.33
Std Dev	1.738

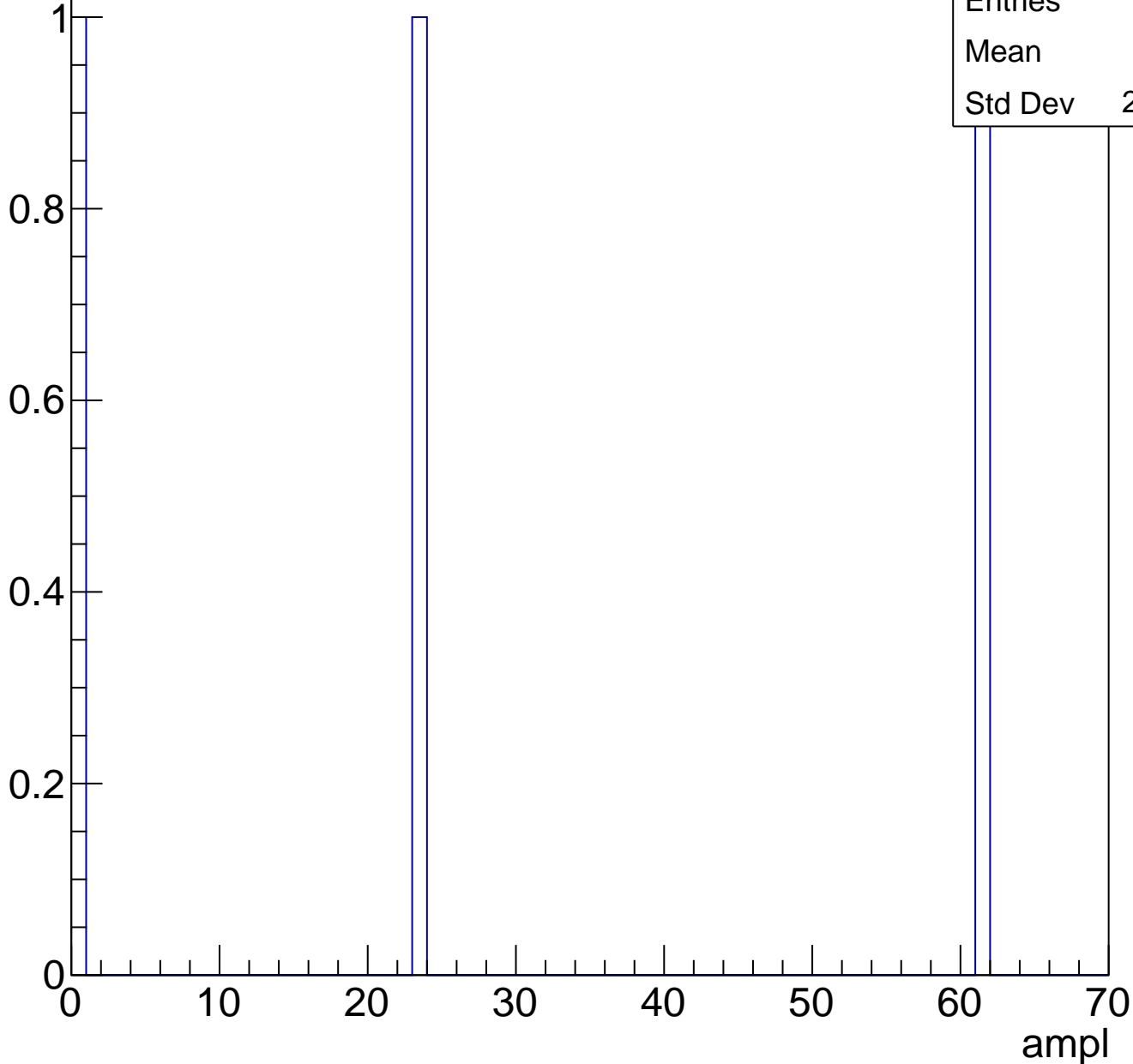




# B1L103S, U1-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch42, adc0

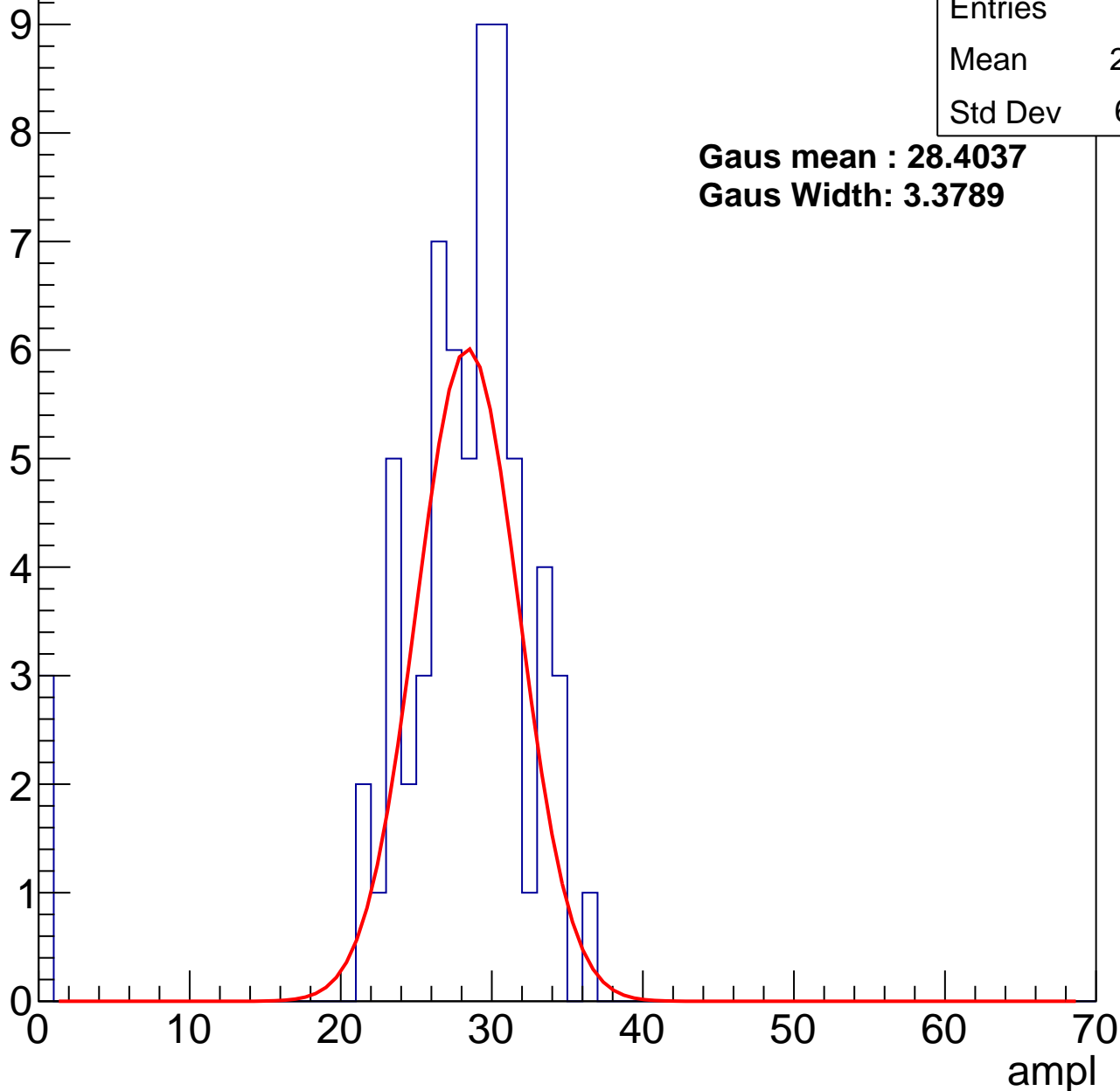
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	26.88
Std Dev	6.741

**Gaus mean : 28.4037**

**Gaus Width: 3.3789**



# B1L103S, U1-ch42, adc1

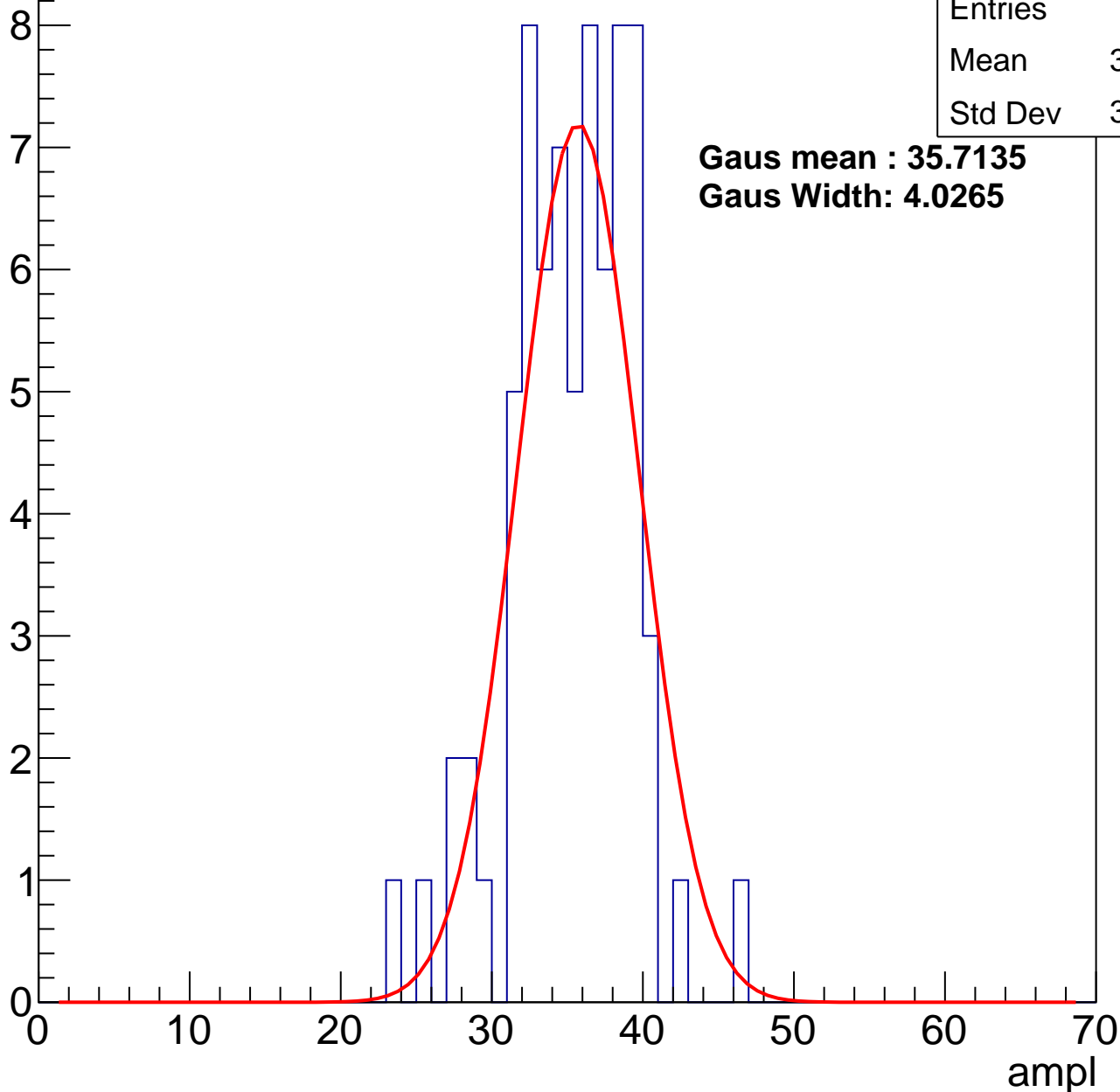
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	34.84
Std Dev	3.993

**Gaus mean : 35.7135**

**Gaus Width: 4.0265**



# B1L103S, U1-ch42, adc2

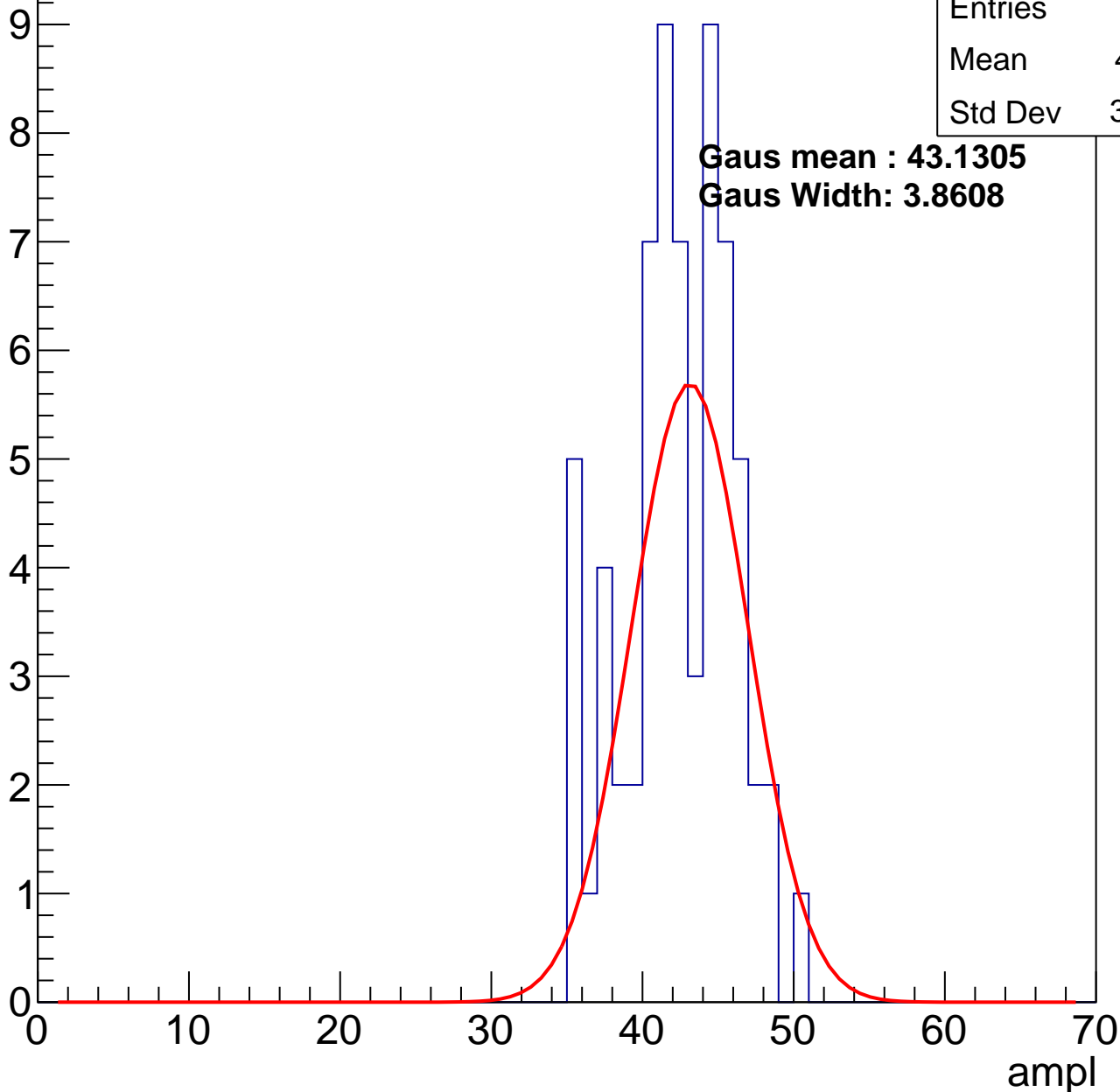
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	41.91
Std Dev	3.558

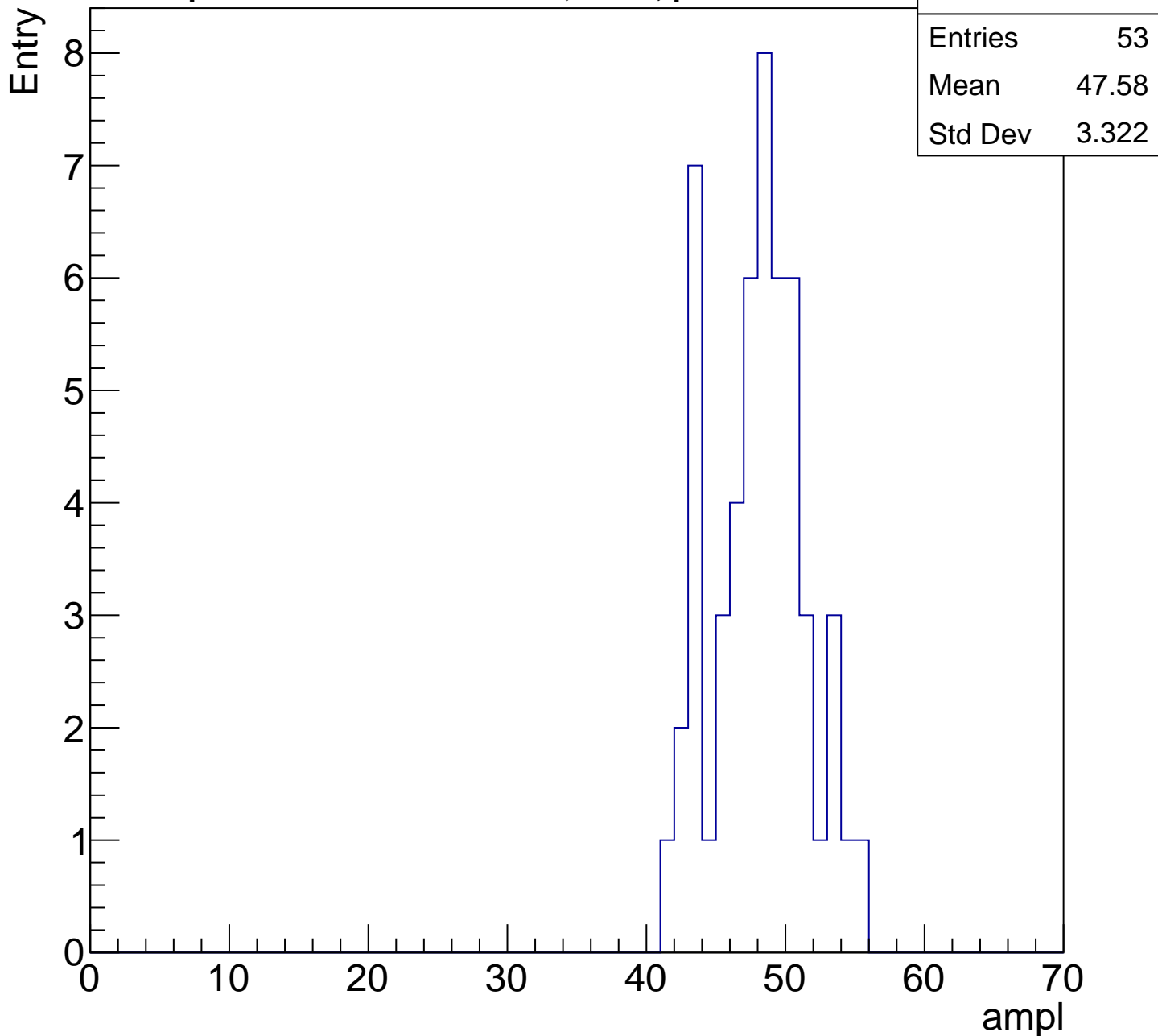
**Gaus mean : 43.1305**

**Gaus Width: 3.8608**



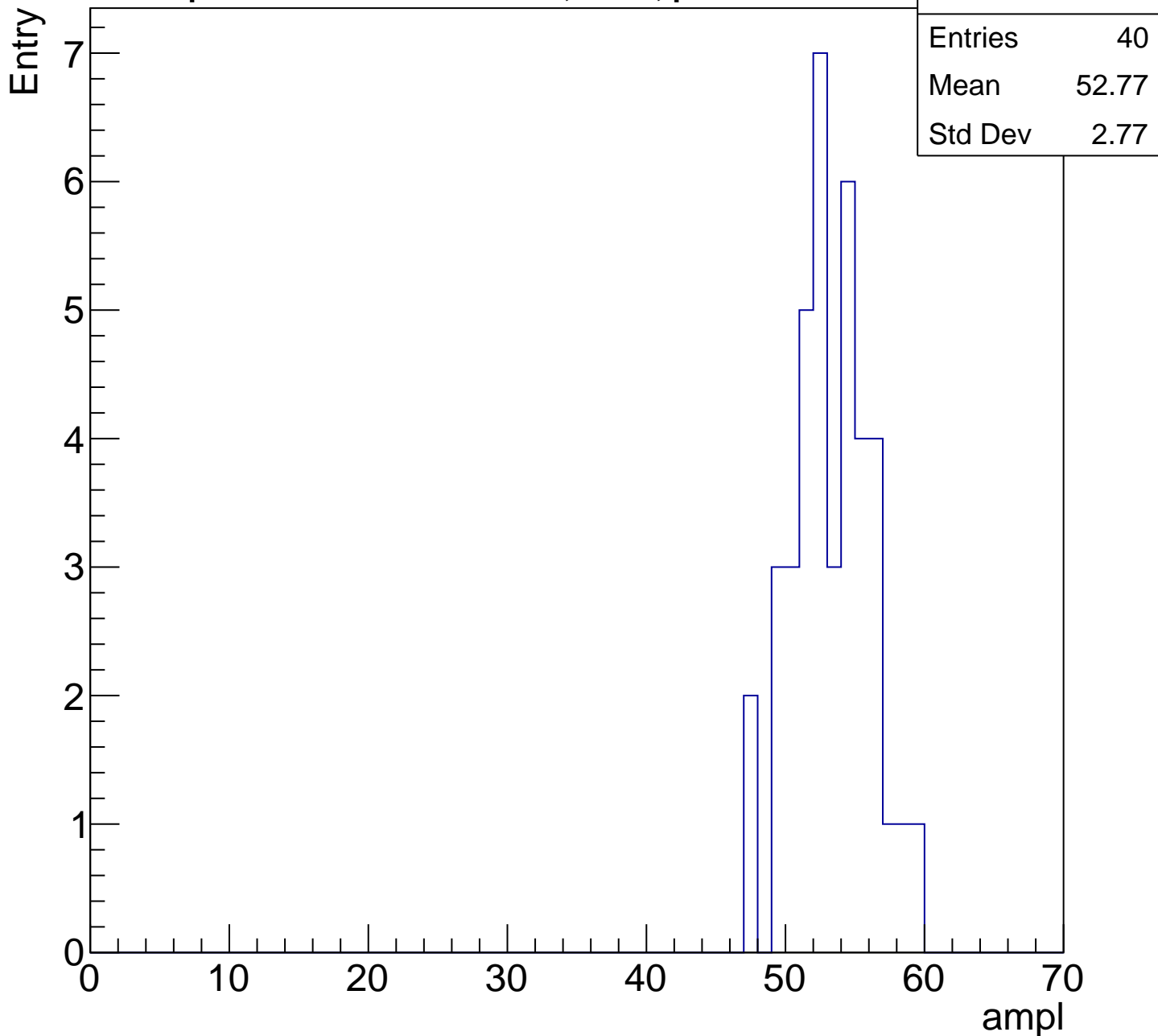
# B1L103S, U1-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U1-ch42, adc4

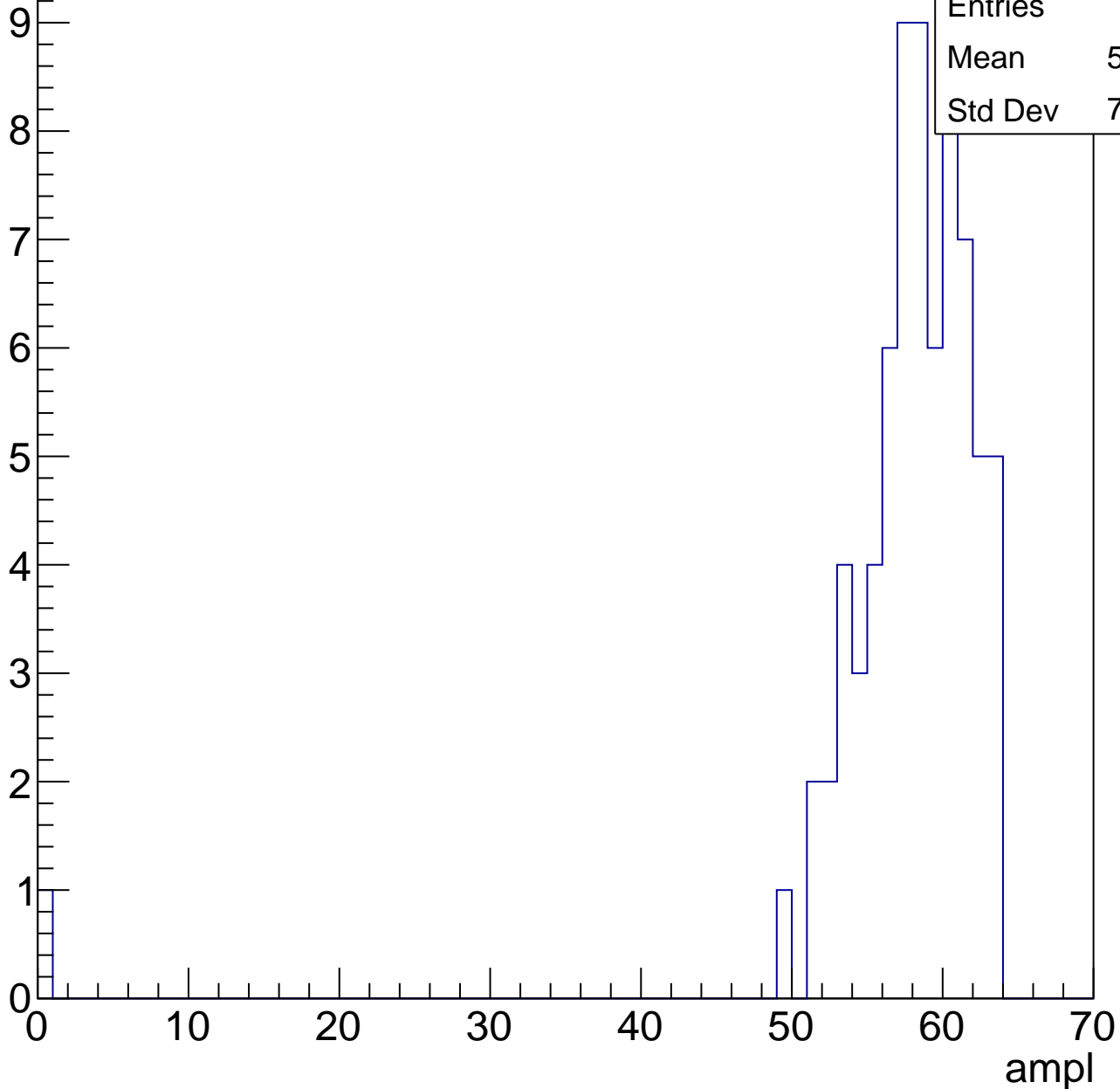
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U1-ch42, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

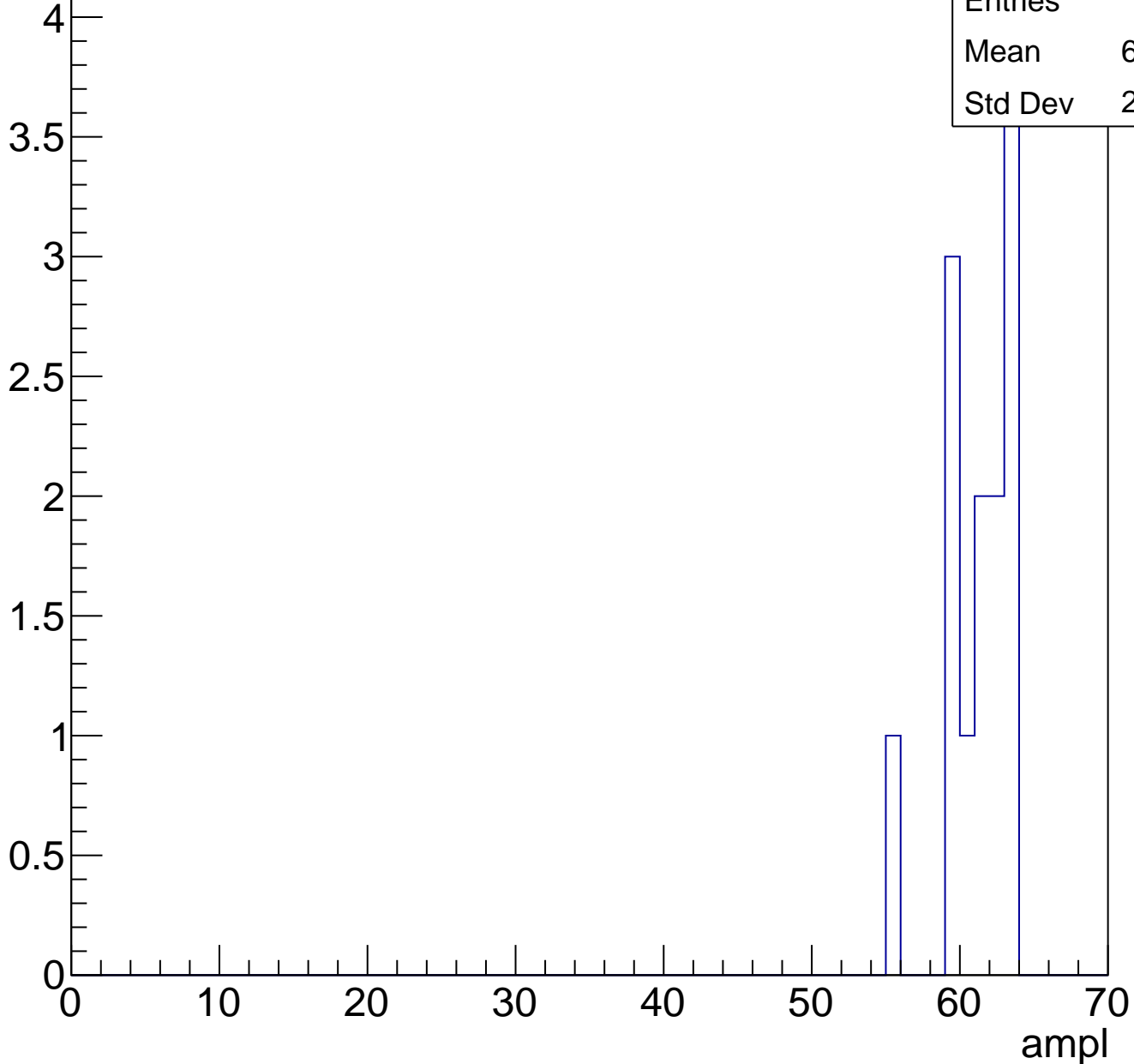
Entry



# B1L103S, U1-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

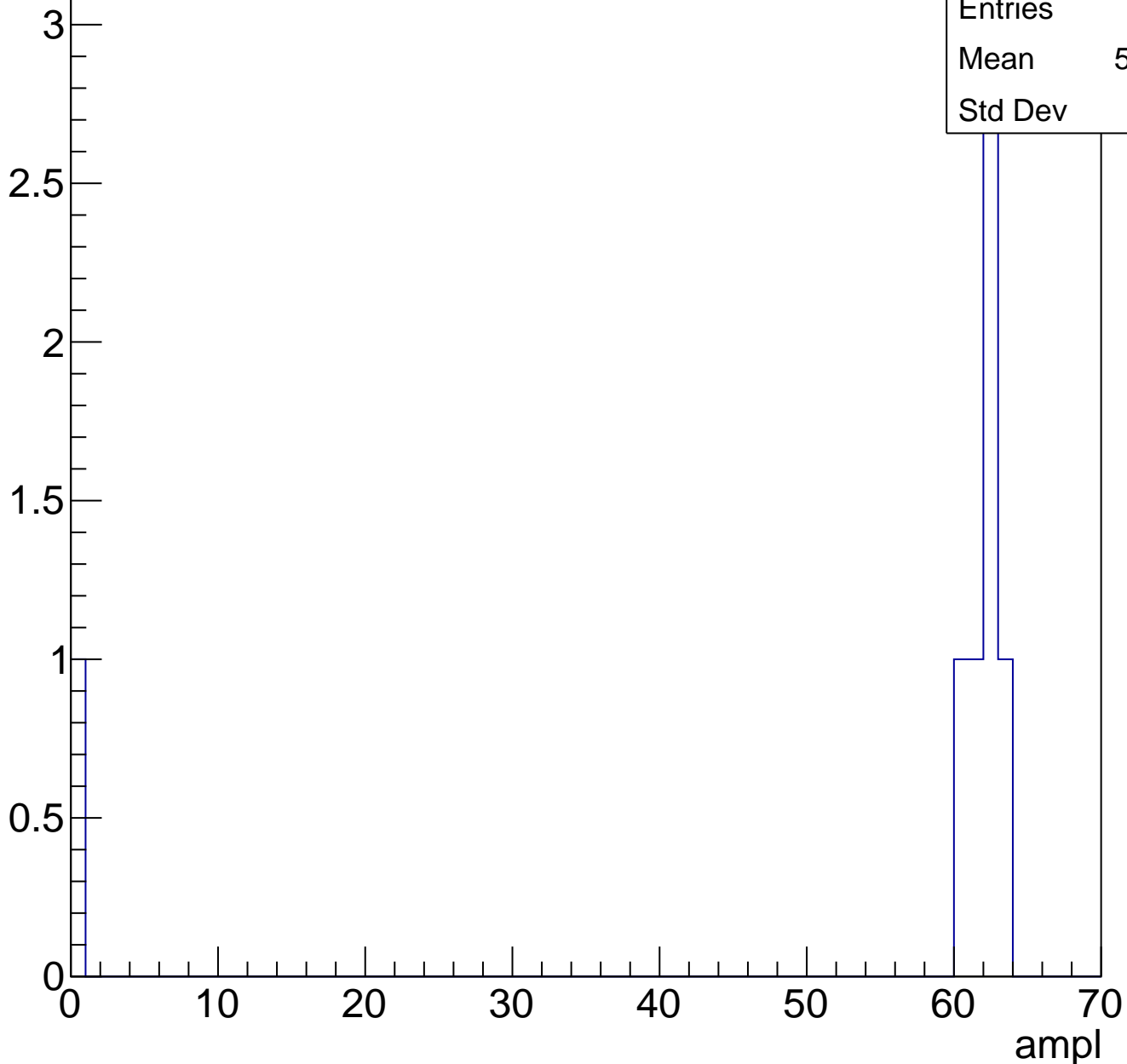




# B1L103S, U1-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch43, adc0

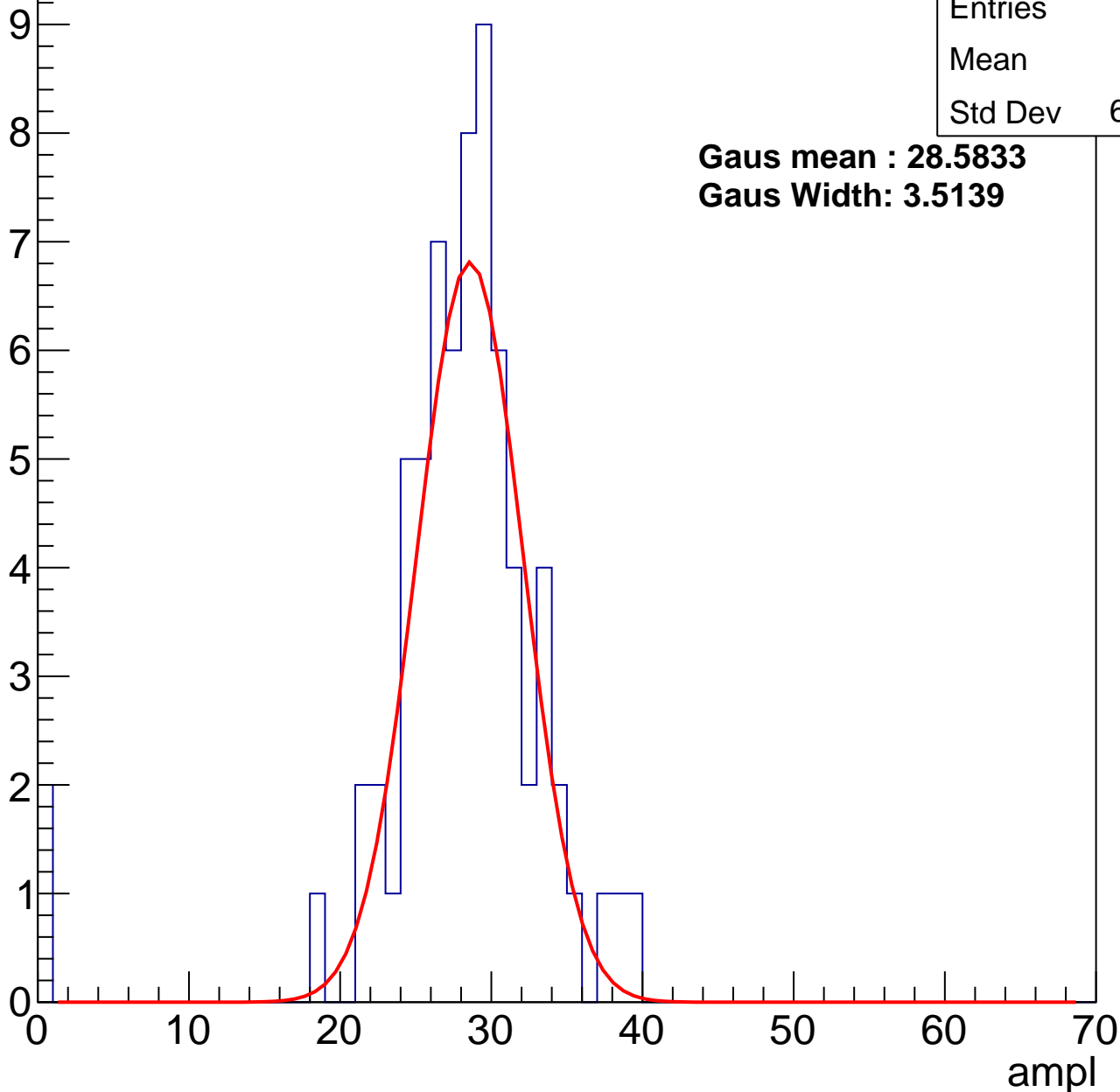
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	27.4
Std Dev	6.119

**Gaus mean : 28.5833**

**Gaus Width: 3.5139**



# B1L103S, U1-ch43, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	73
Mean	35.14
Std Dev	3.724

**Gaus mean : 35.5553**

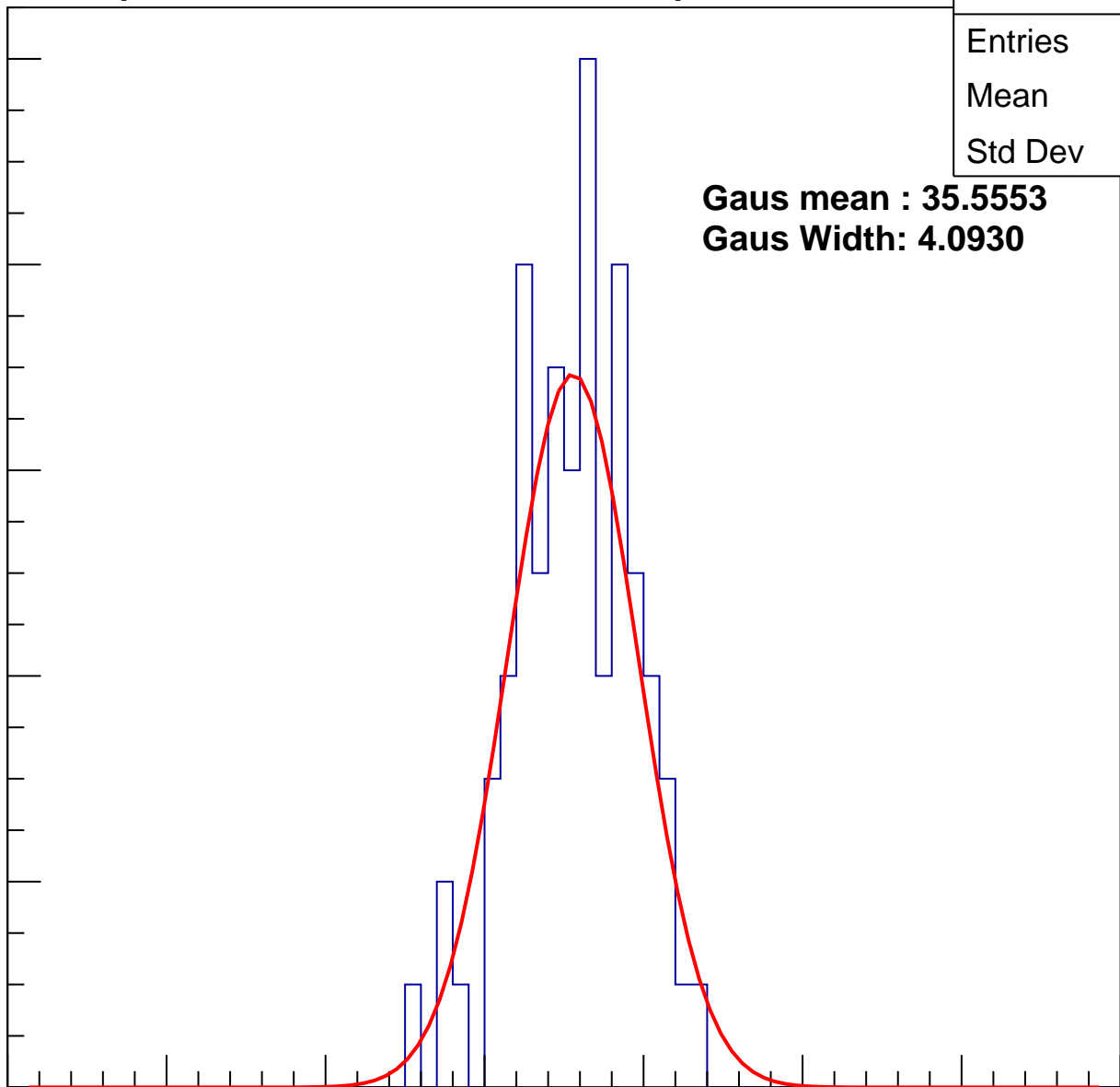
**Gaus Width: 4.0930**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U1-ch43, adc2

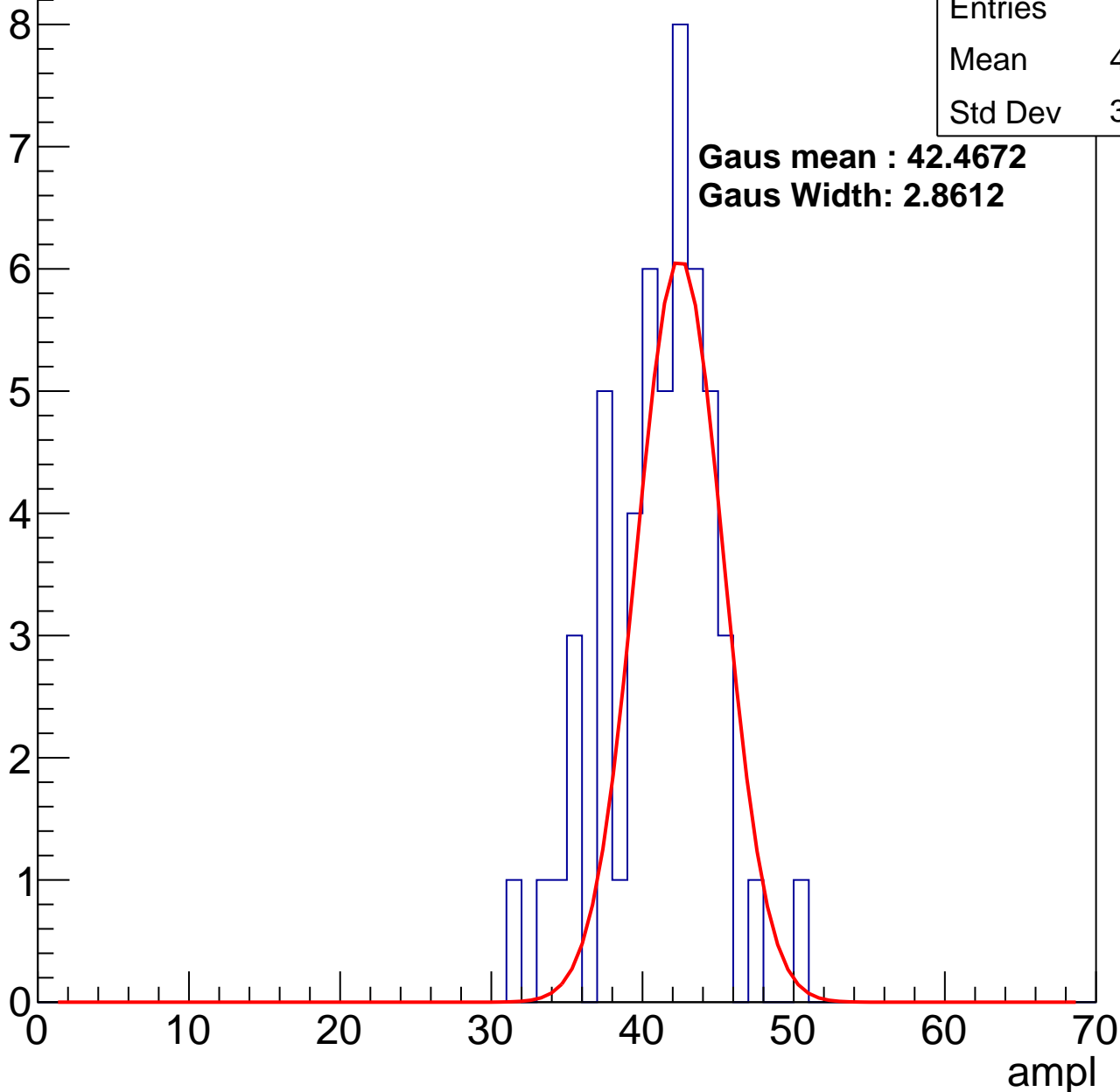
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	40.65
Std Dev	3.618

**Gaus mean : 42.4672**

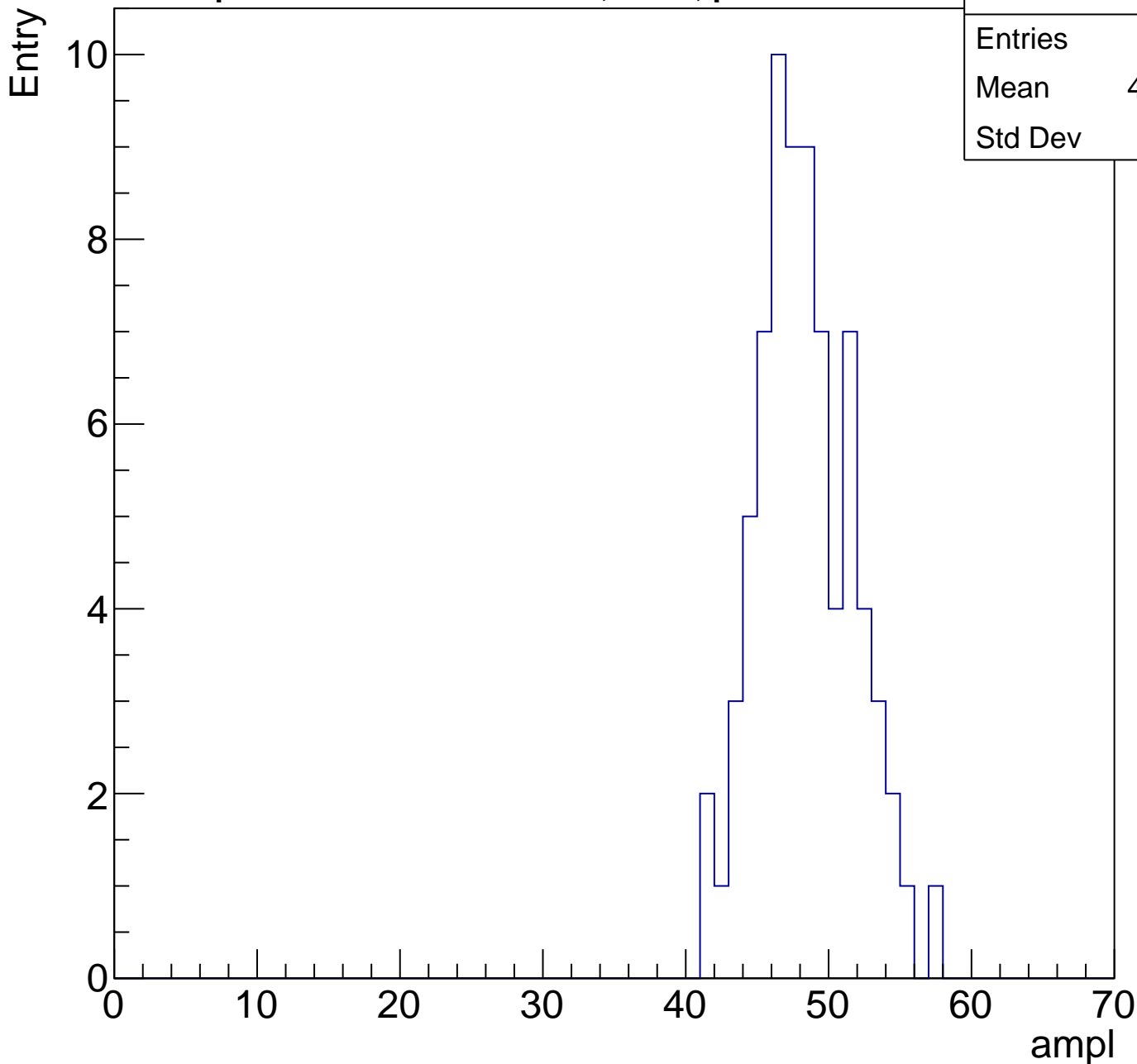
**Gaus Width: 2.8612**



# B1L103S, U1-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	75
Mean	47.87
Std Dev	3.32

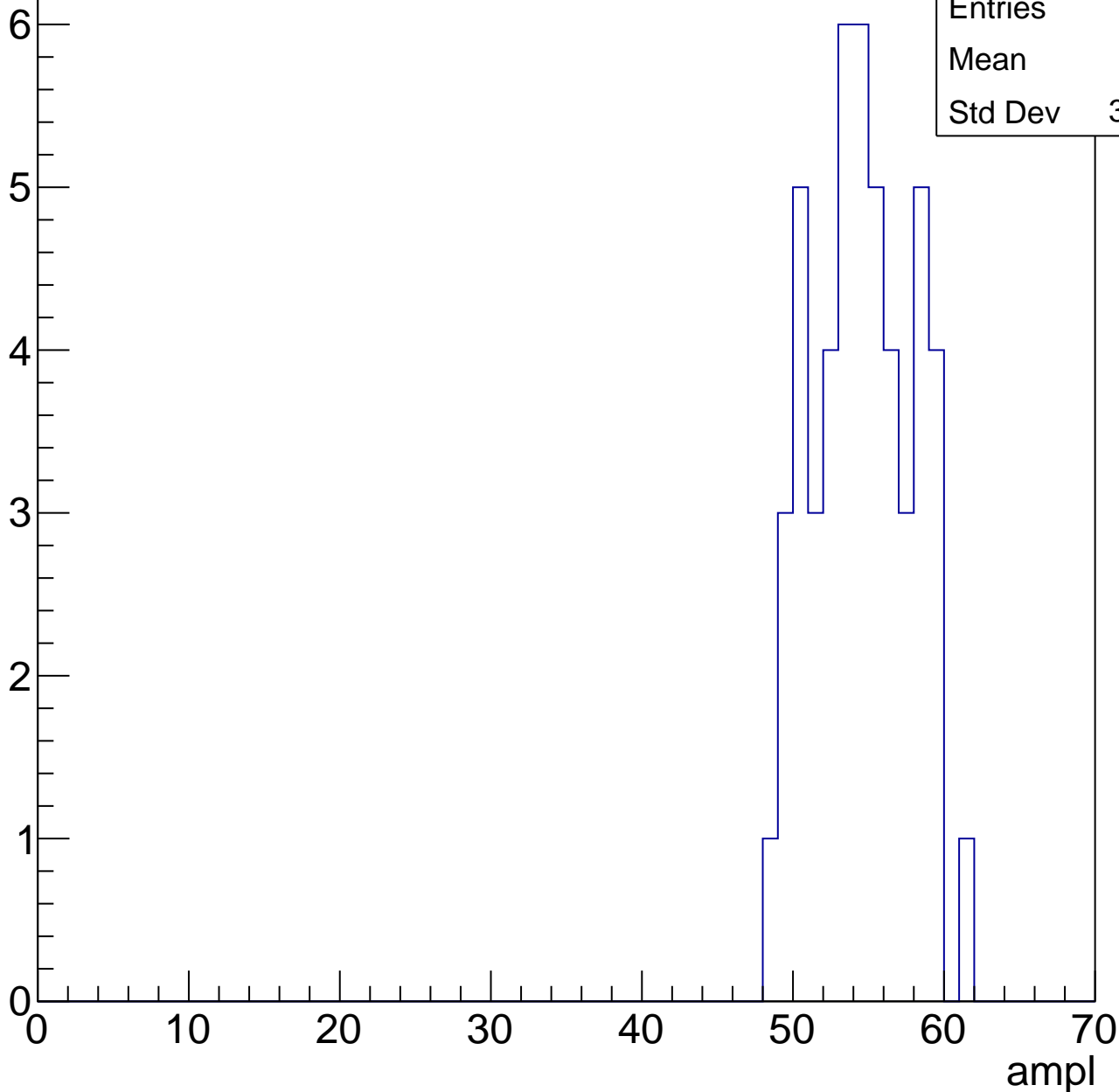


# B1L103S, U1-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	54.1
Std Dev	3.214

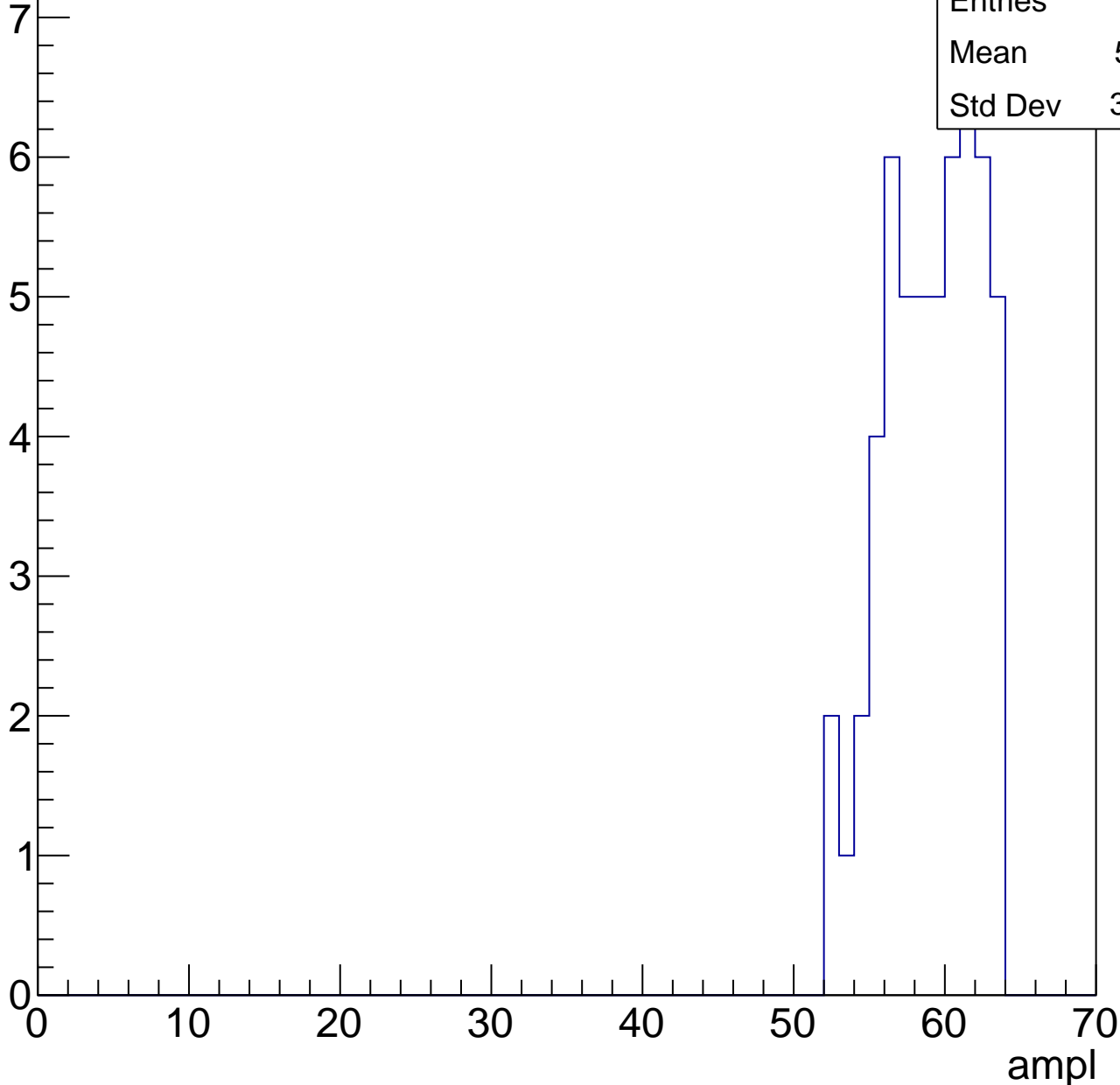


# B1L103S, U1-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

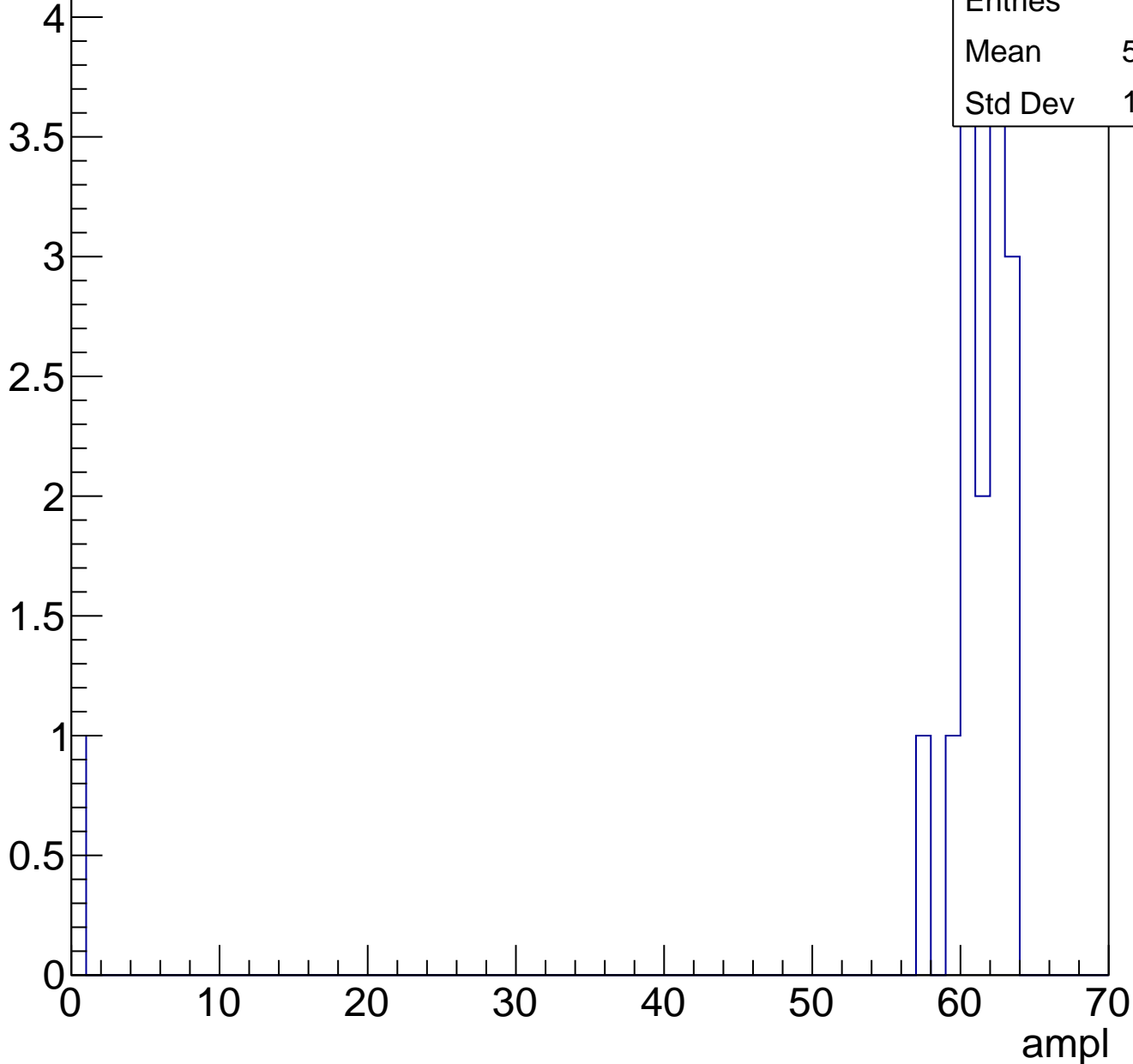
Entries	54
Mean	58.61
Std Dev	3.003



# B1L103S, U1-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U1-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch44, adc0

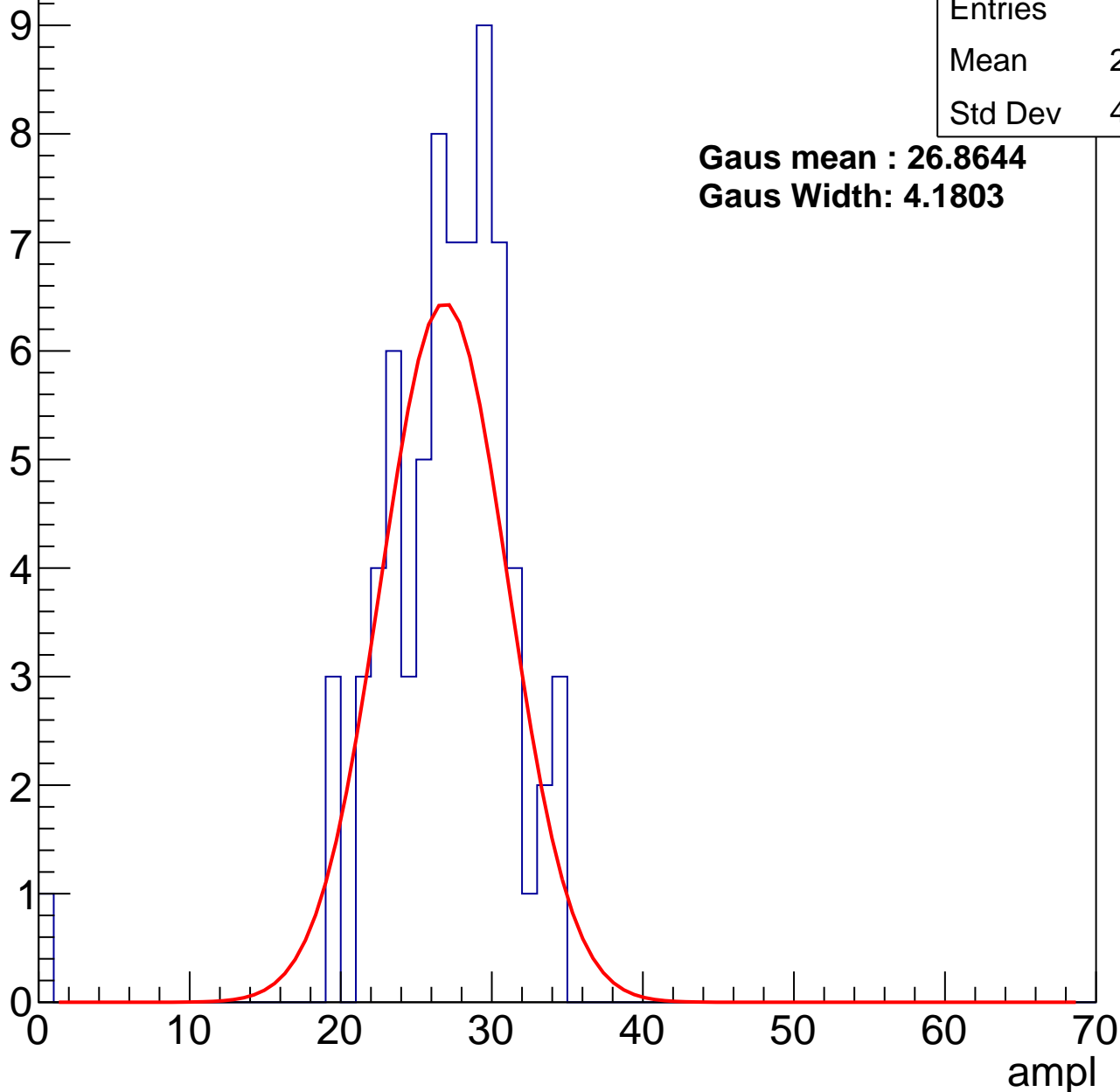
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	26.45
Std Dev	4.786

**Gaus mean : 26.8644**

**Gaus Width: 4.1803**



# B1L103S, U1-ch44, adc1

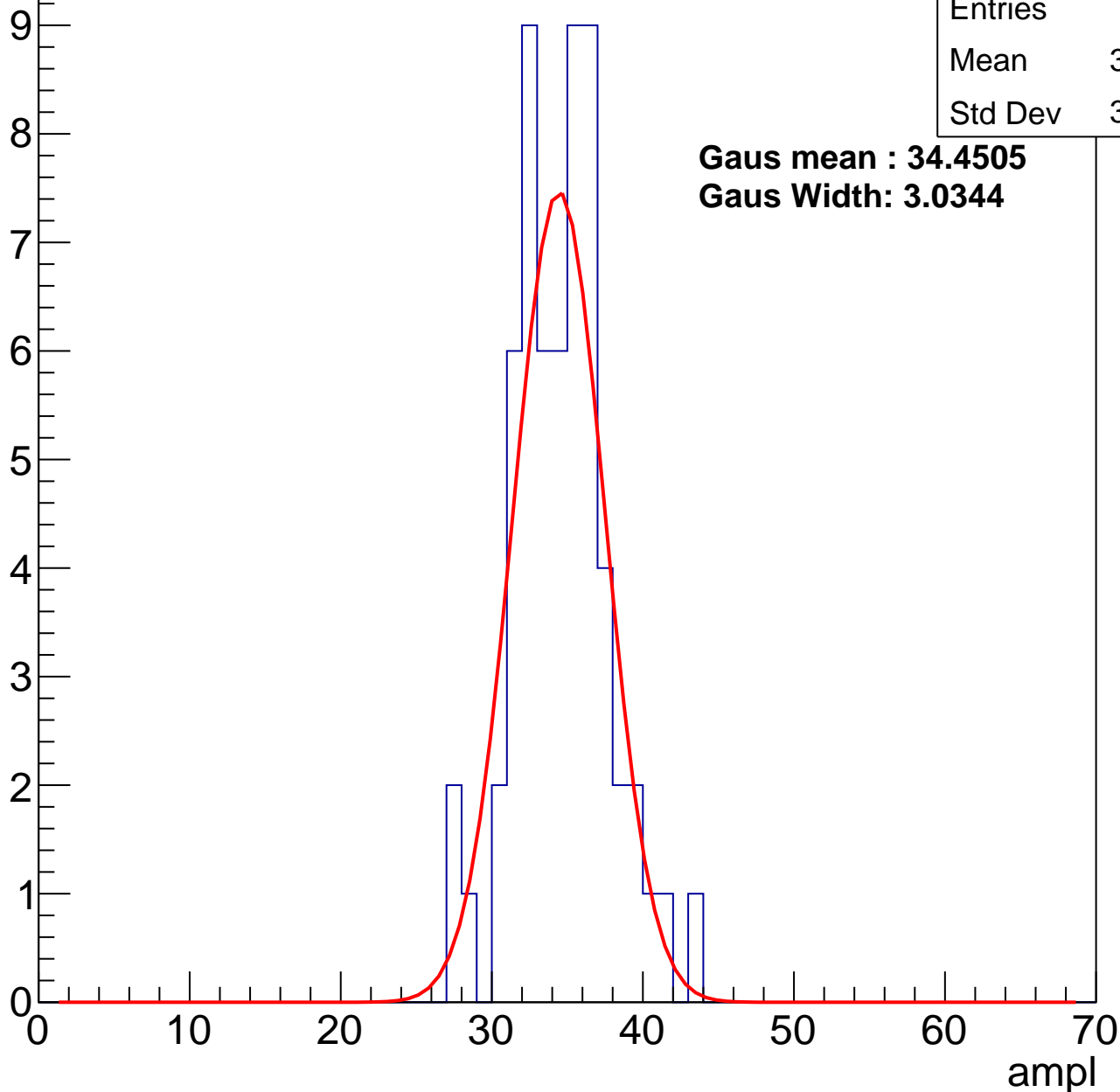
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	34.15
Std Dev	3.109

**Gaus mean : 34.4505**

**Gaus Width: 3.0344**



# B1L103S, U1-ch44, adc2

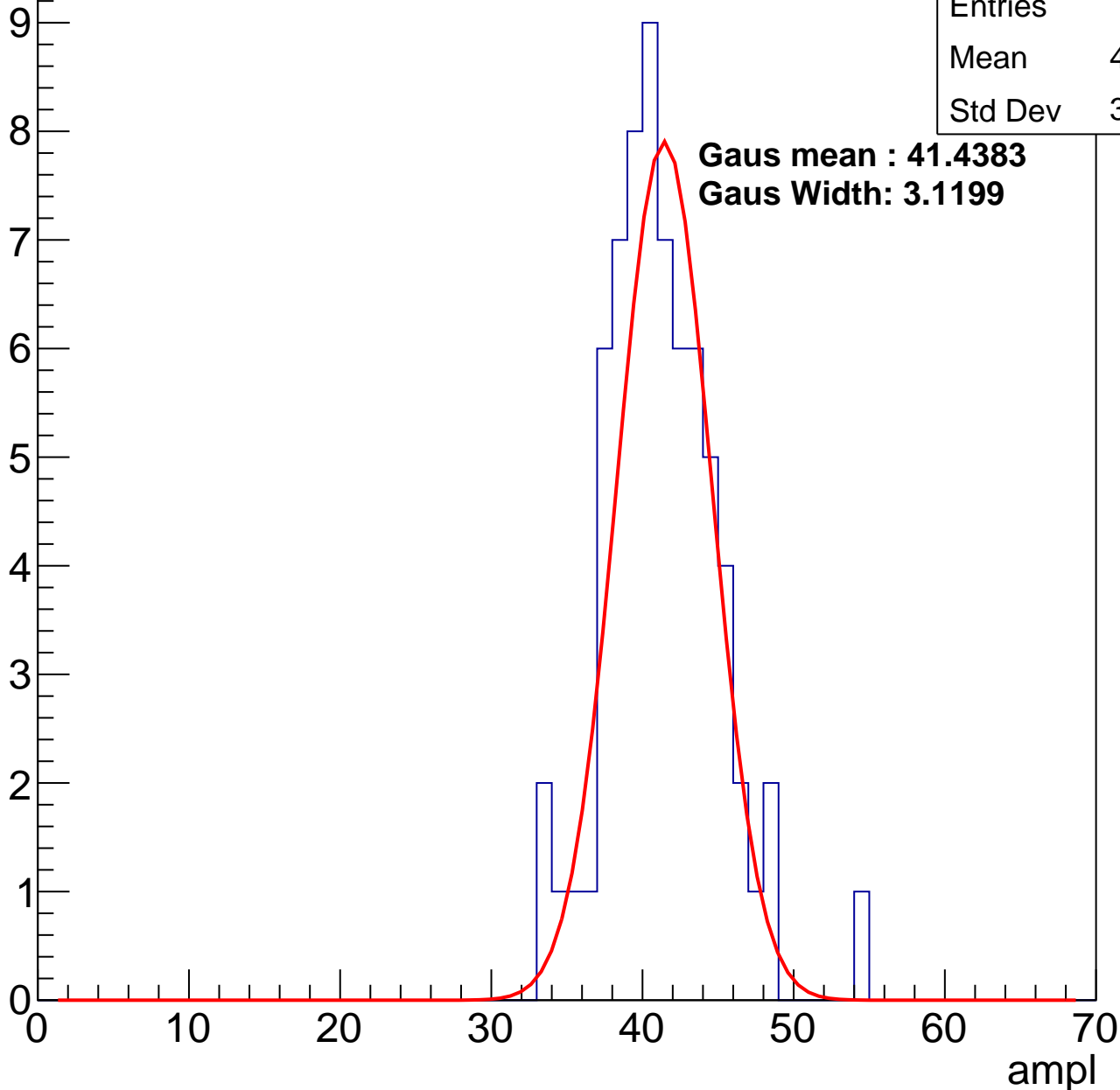
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	40.83
Std Dev	3.667

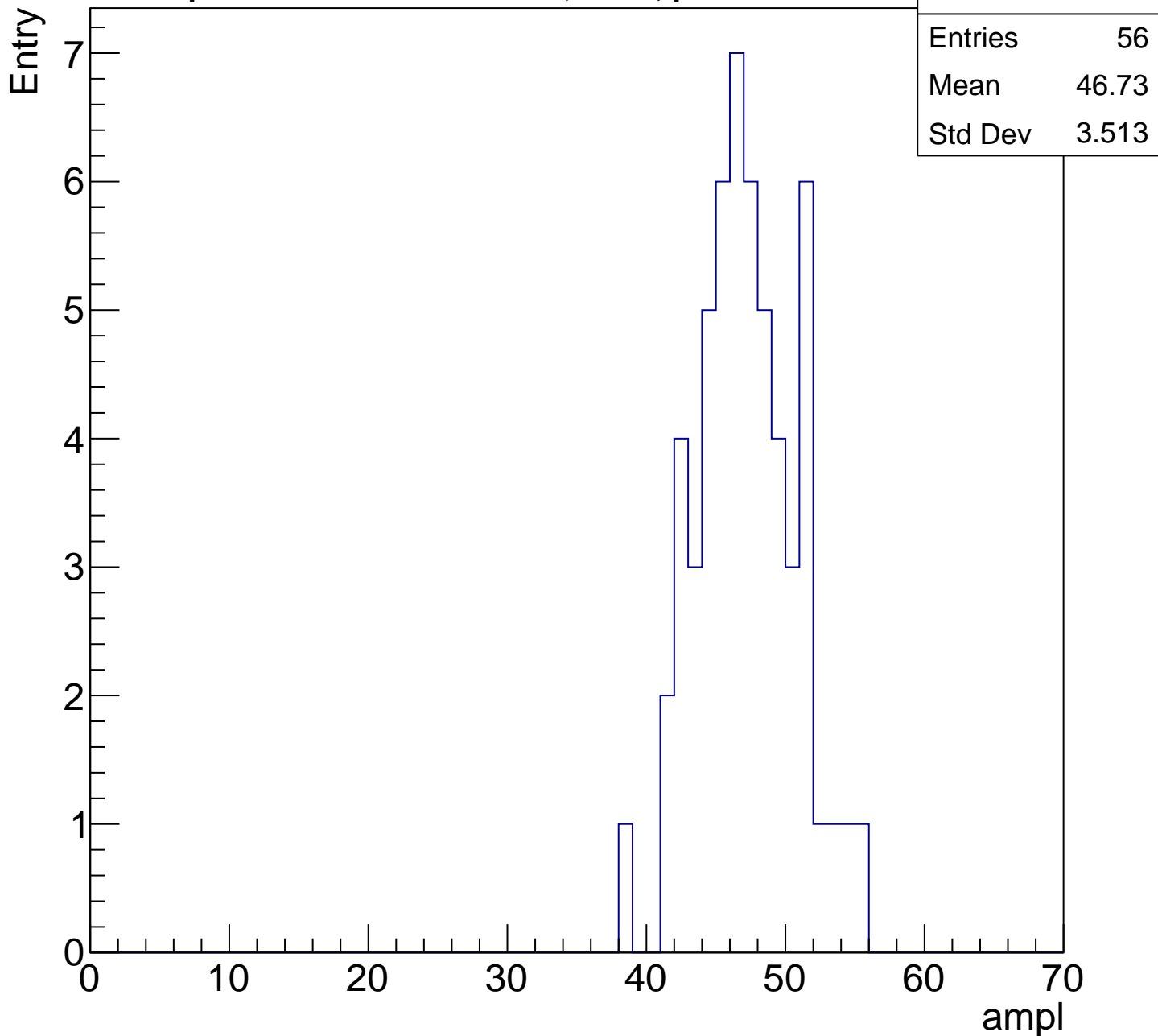
**Gaus mean : 41.4383**

**Gaus Width: 3.1199**



# B1L103S, U1-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

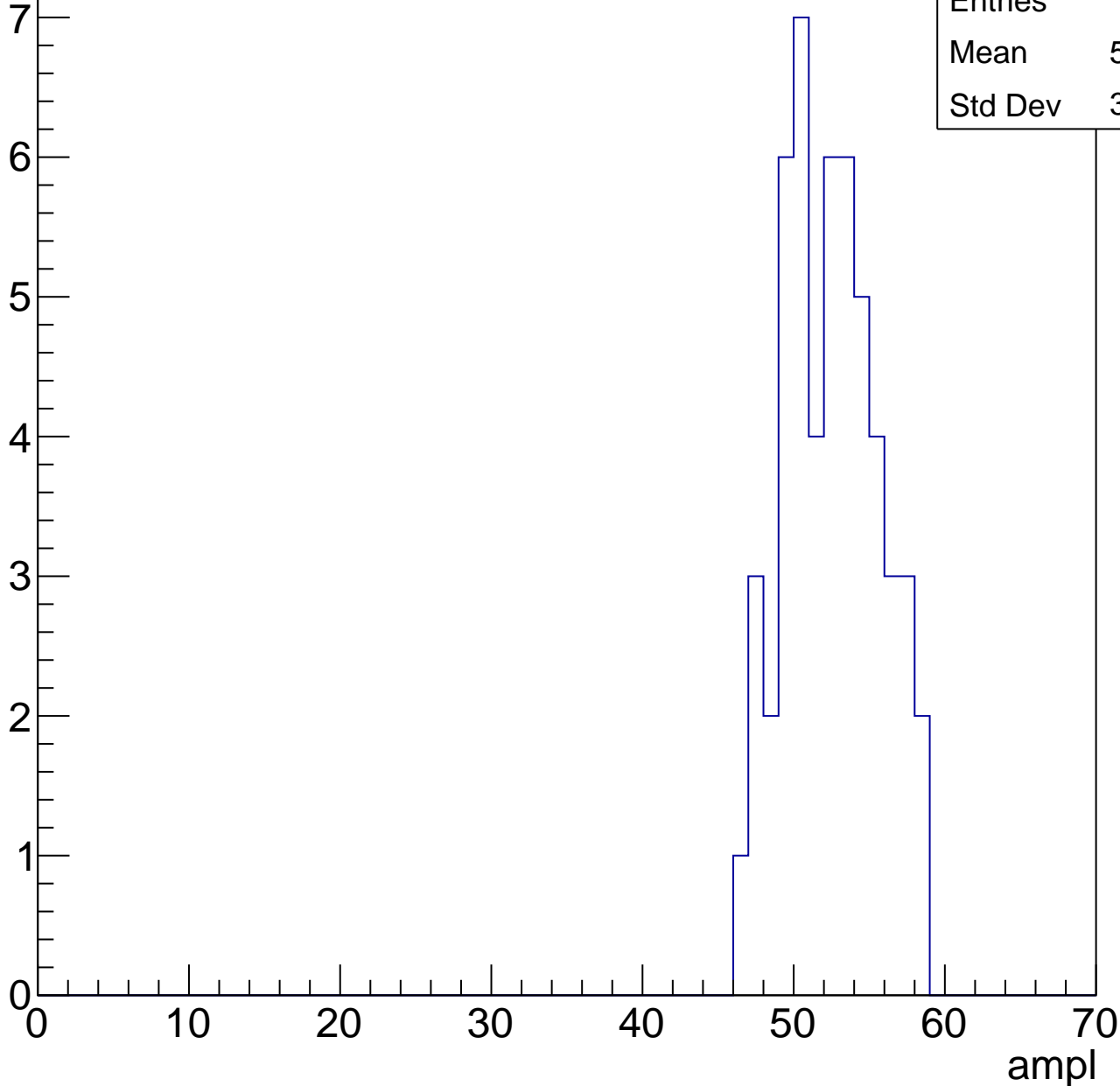


# B1L103S, U1-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	52.04
Std Dev	3.057

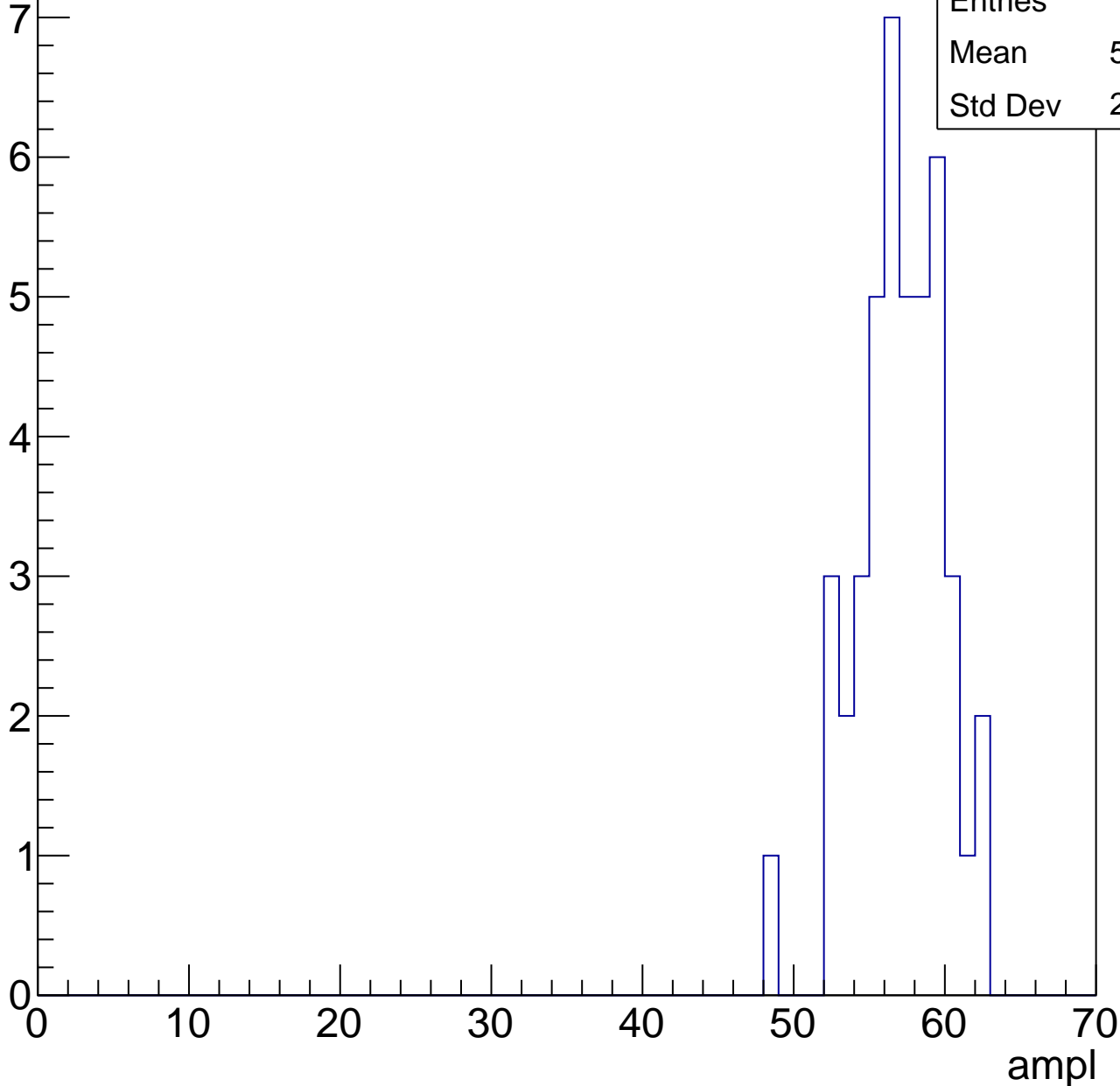


# B1L103S, U1-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	43
Mean	56.58
Std Dev	2.879

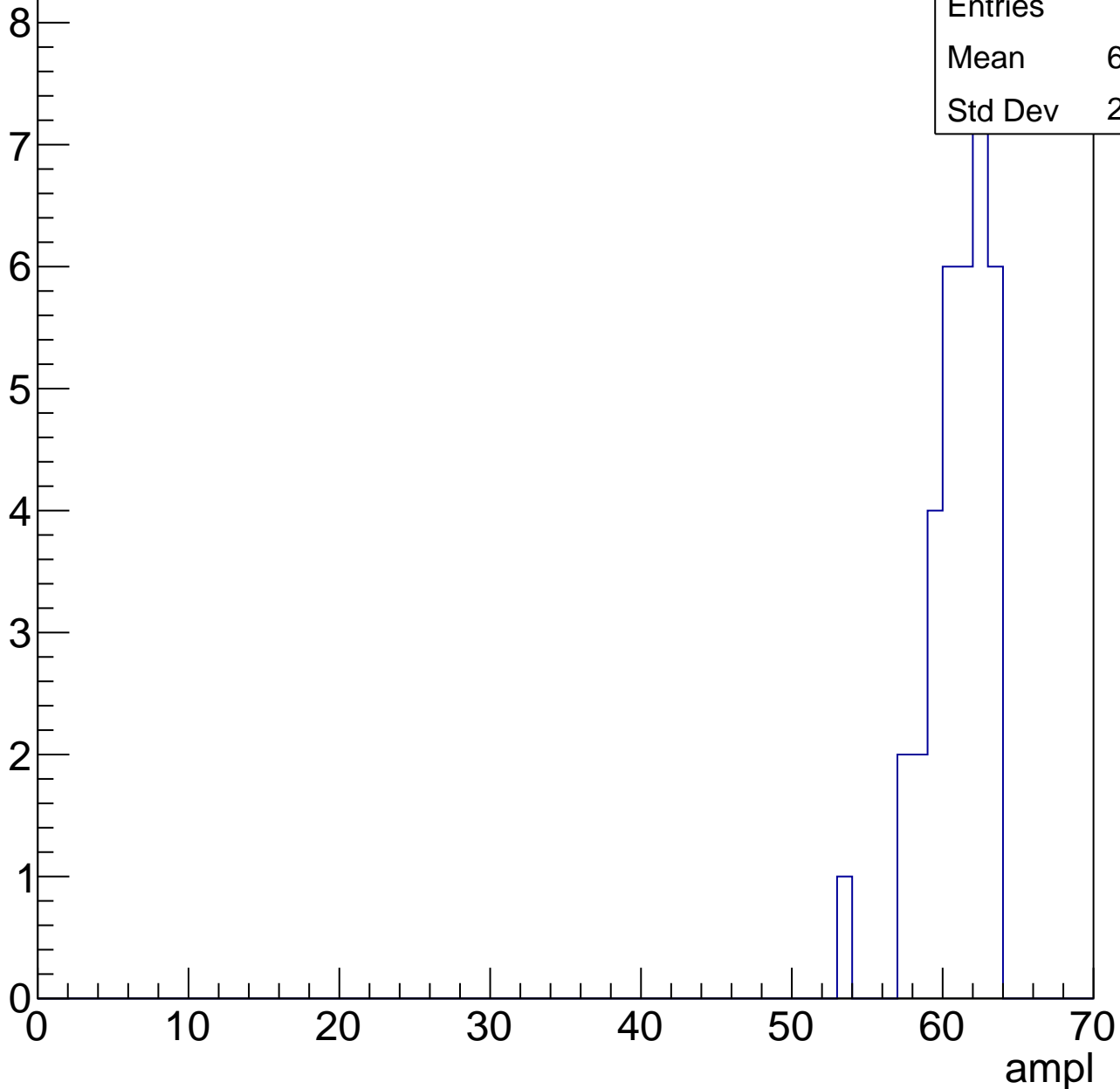


# B1L103S, U1-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	35
Mean	60.54
Std Dev	2.143



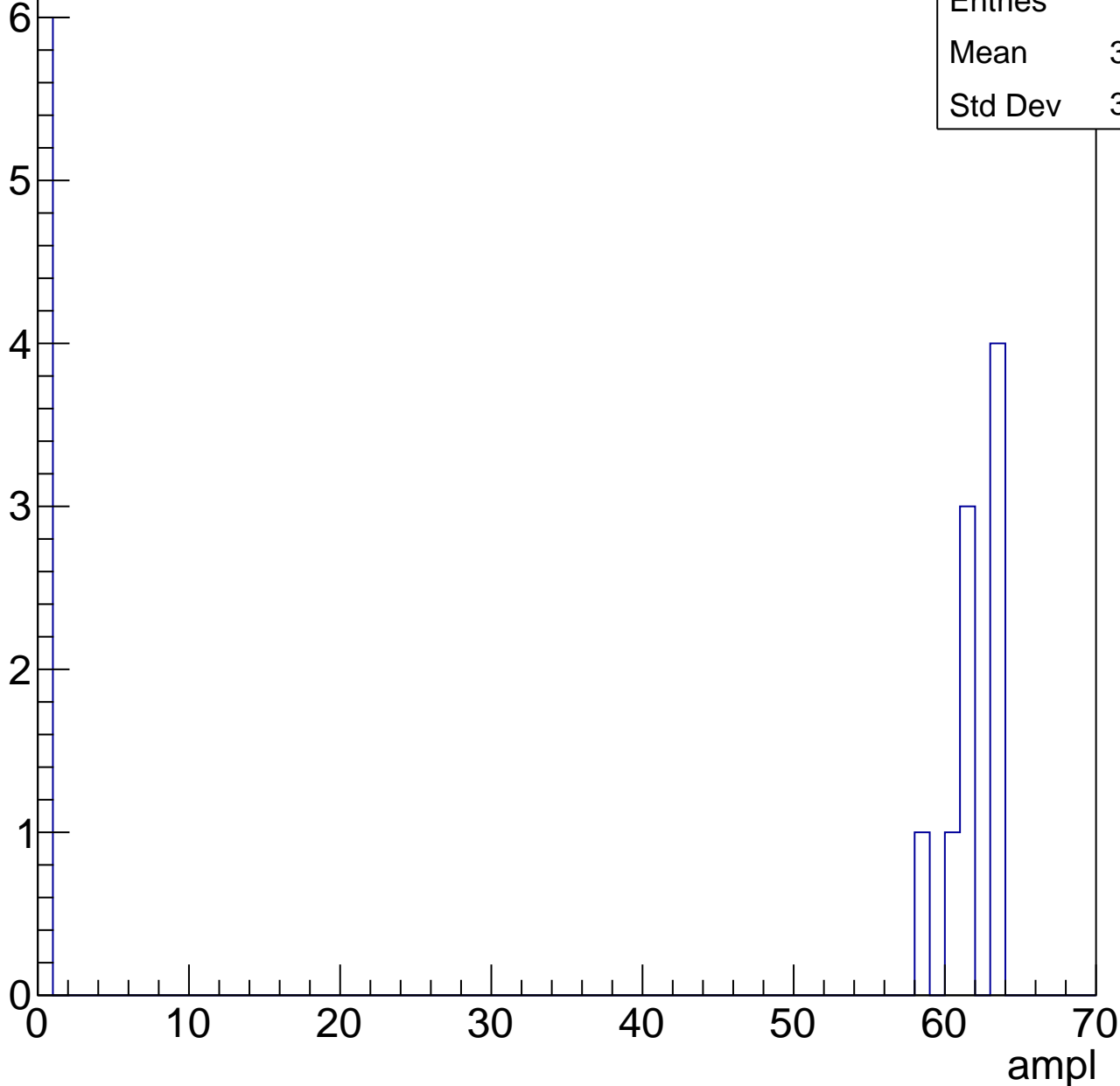


# B1L103S, U1-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	15
Mean	36.87
Std Dev	30.13



# B1L103S, U1-ch45, adc0

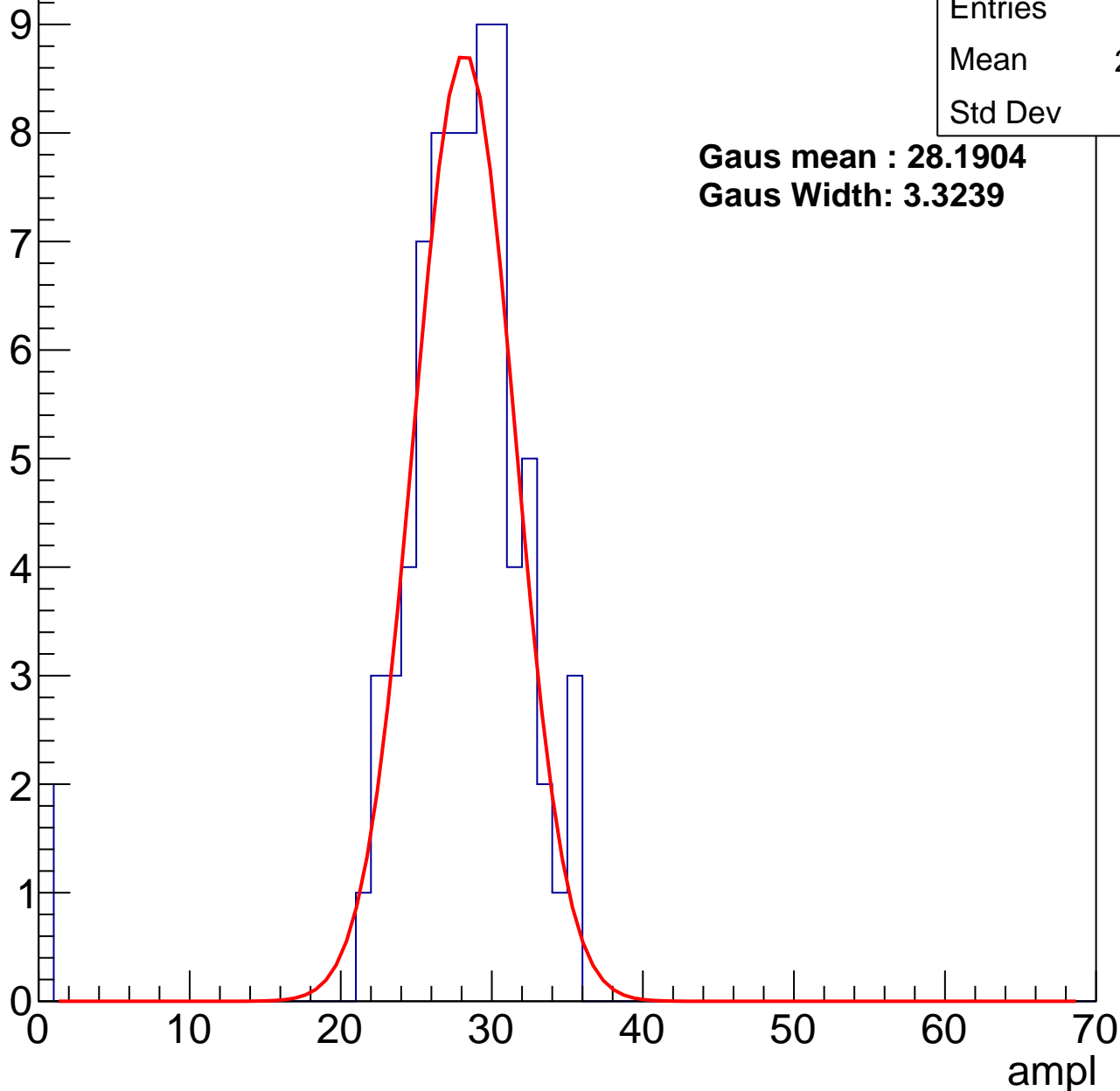
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	27.21
Std Dev	5.48

**Gaus mean : 28.1904**

**Gaus Width: 3.3239**



# B1L103S, U1-ch45, adc1

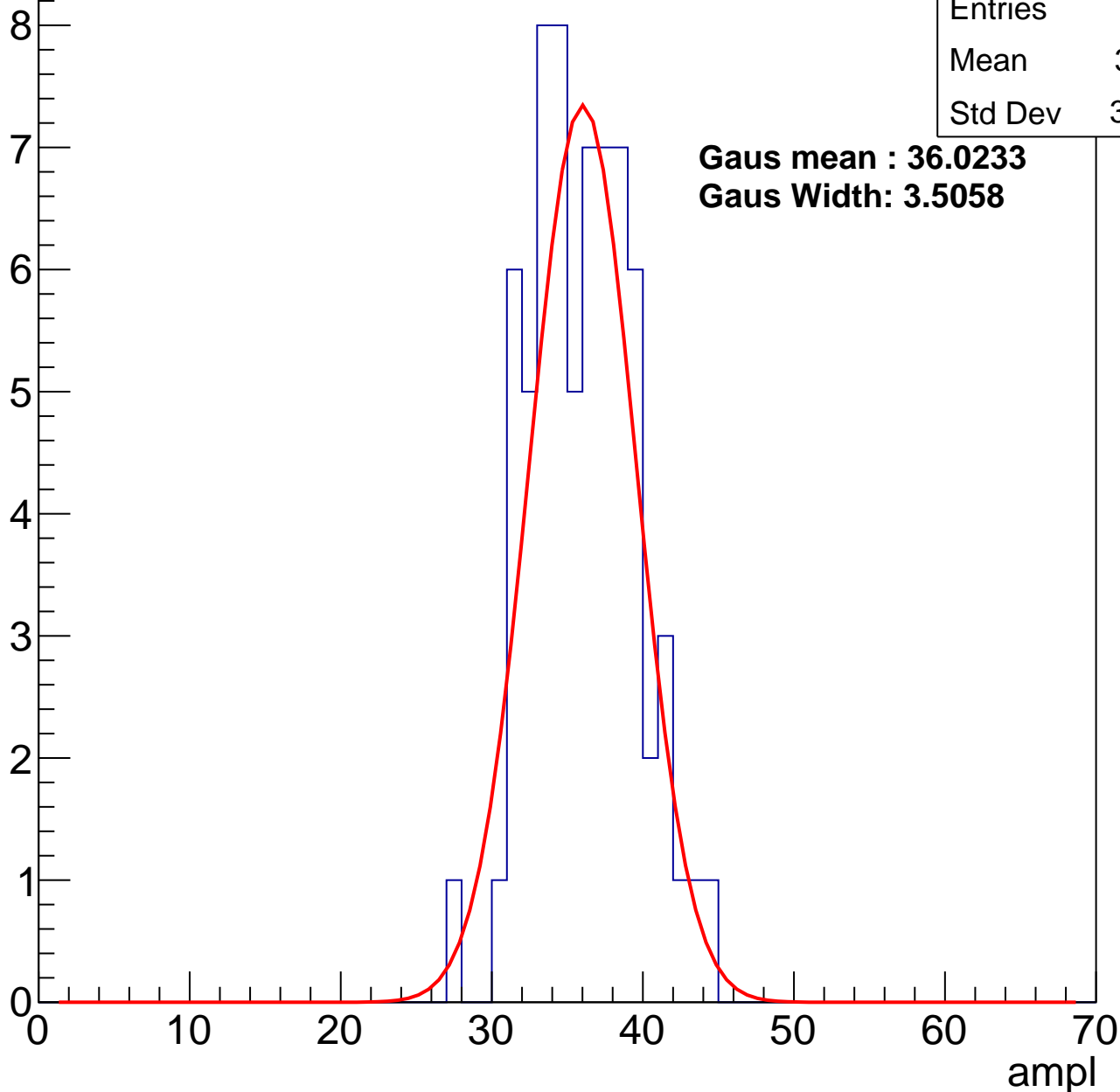
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	35.61
Std Dev	3.385

**Gaus mean : 36.0233**

**Gaus Width: 3.5058**



# B1L103S, U1-ch45, adc2

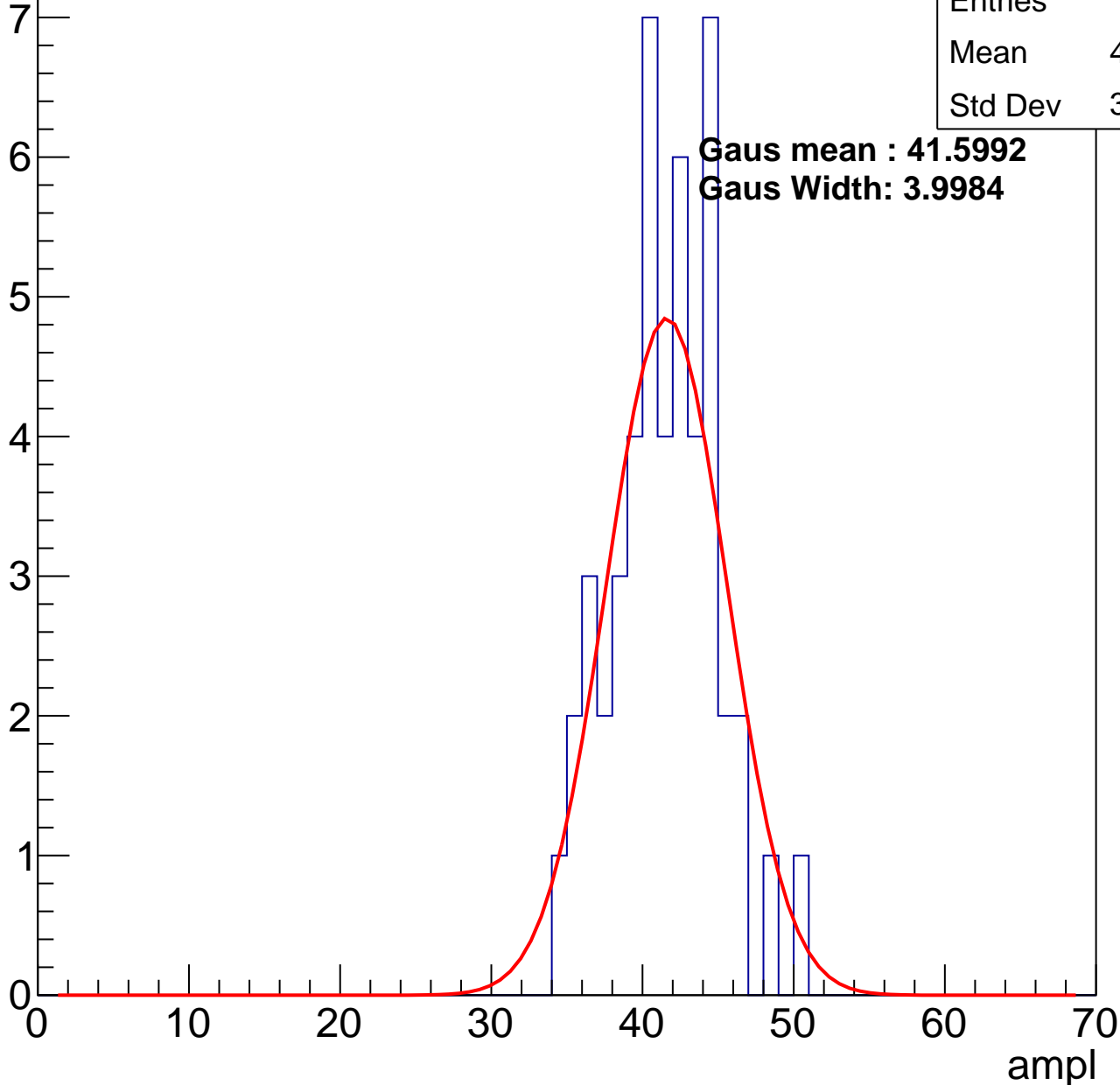
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	41.06
Std Dev	3.425

**Gaus mean : 41.5992**

**Gaus Width: 3.9984**

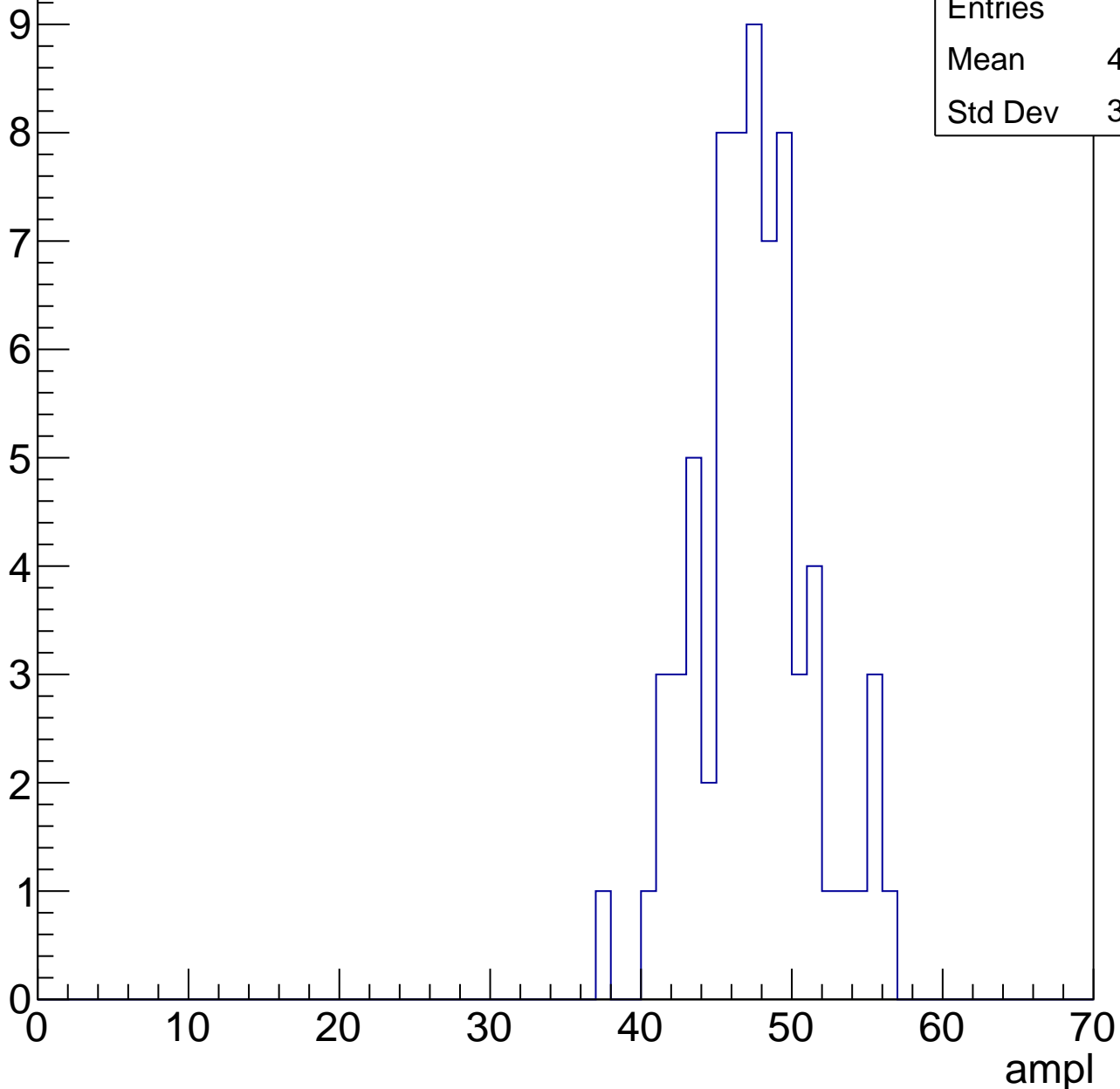


# B1L103S, U1-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	46.99
Std Dev	3.774

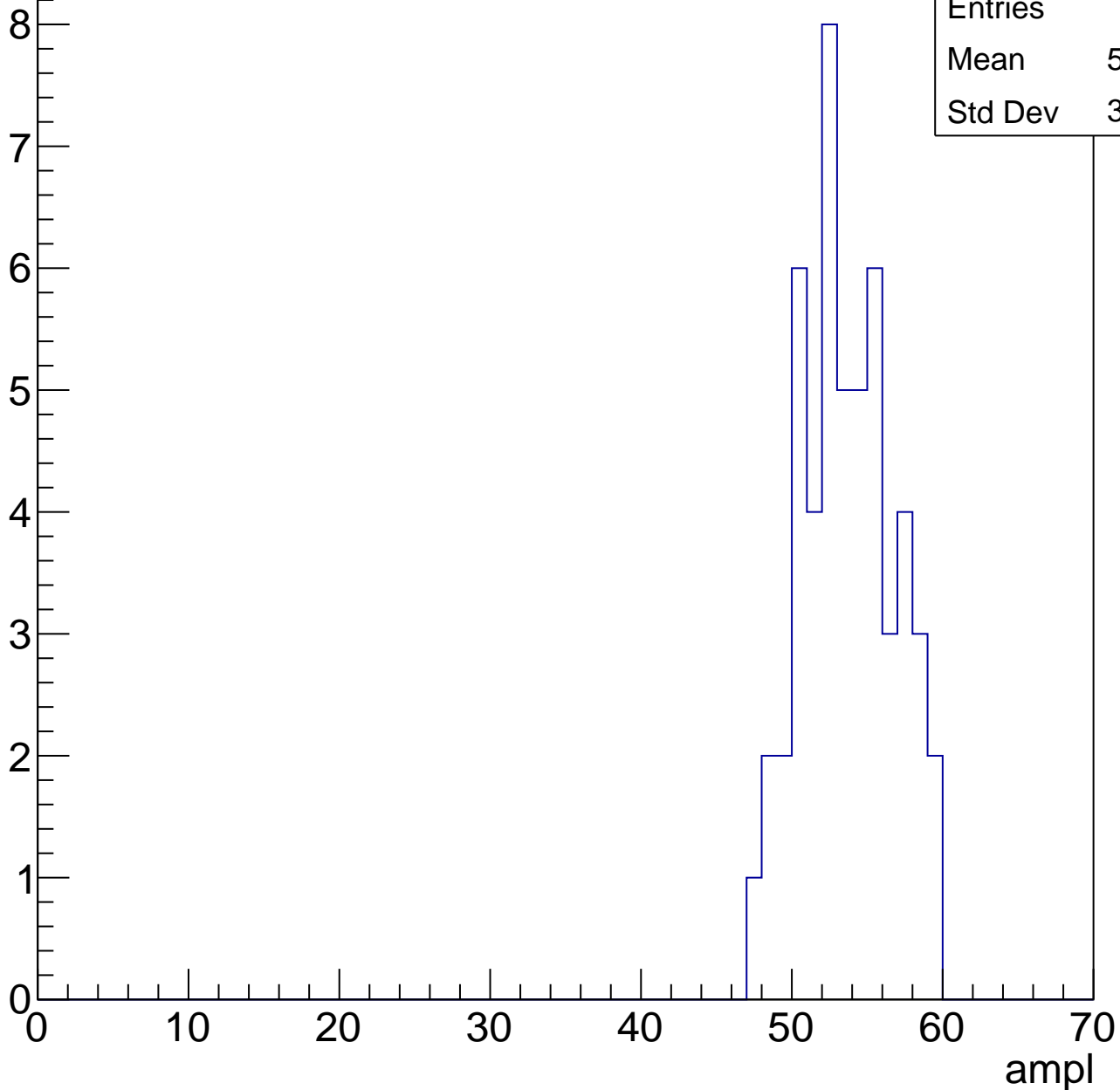


# B1L103S, U1-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	53.22
Std Dev	3.005



# B1L103S, U1-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

7

6

5

4

3

2

1

0

Entries 52

Mean 57.79

Std Dev 3.248

ampl

0

10

20

30

40

50

60

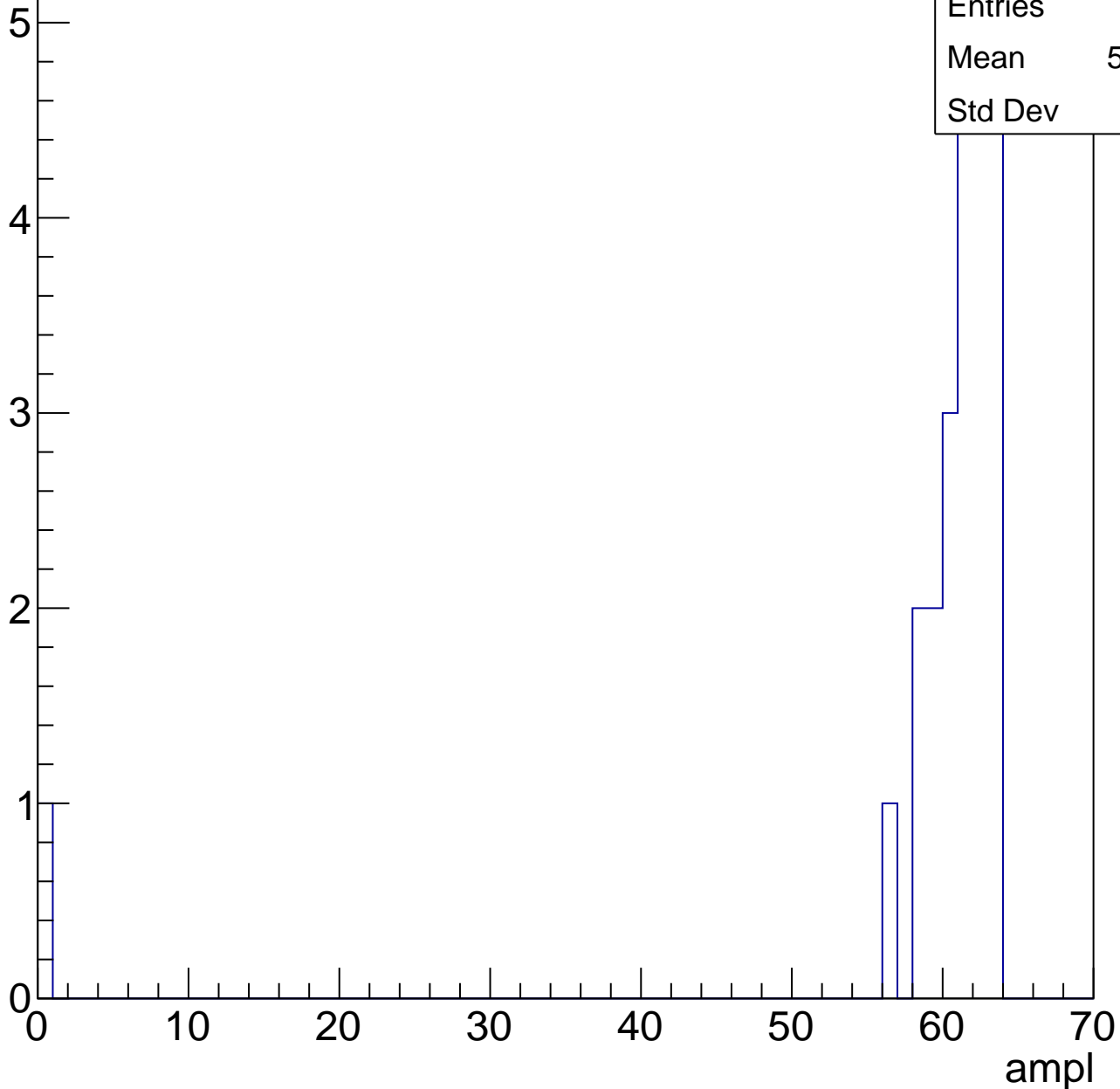
70

# B1L103S, U1-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	24
Mean	58.33
Std Dev	12.3

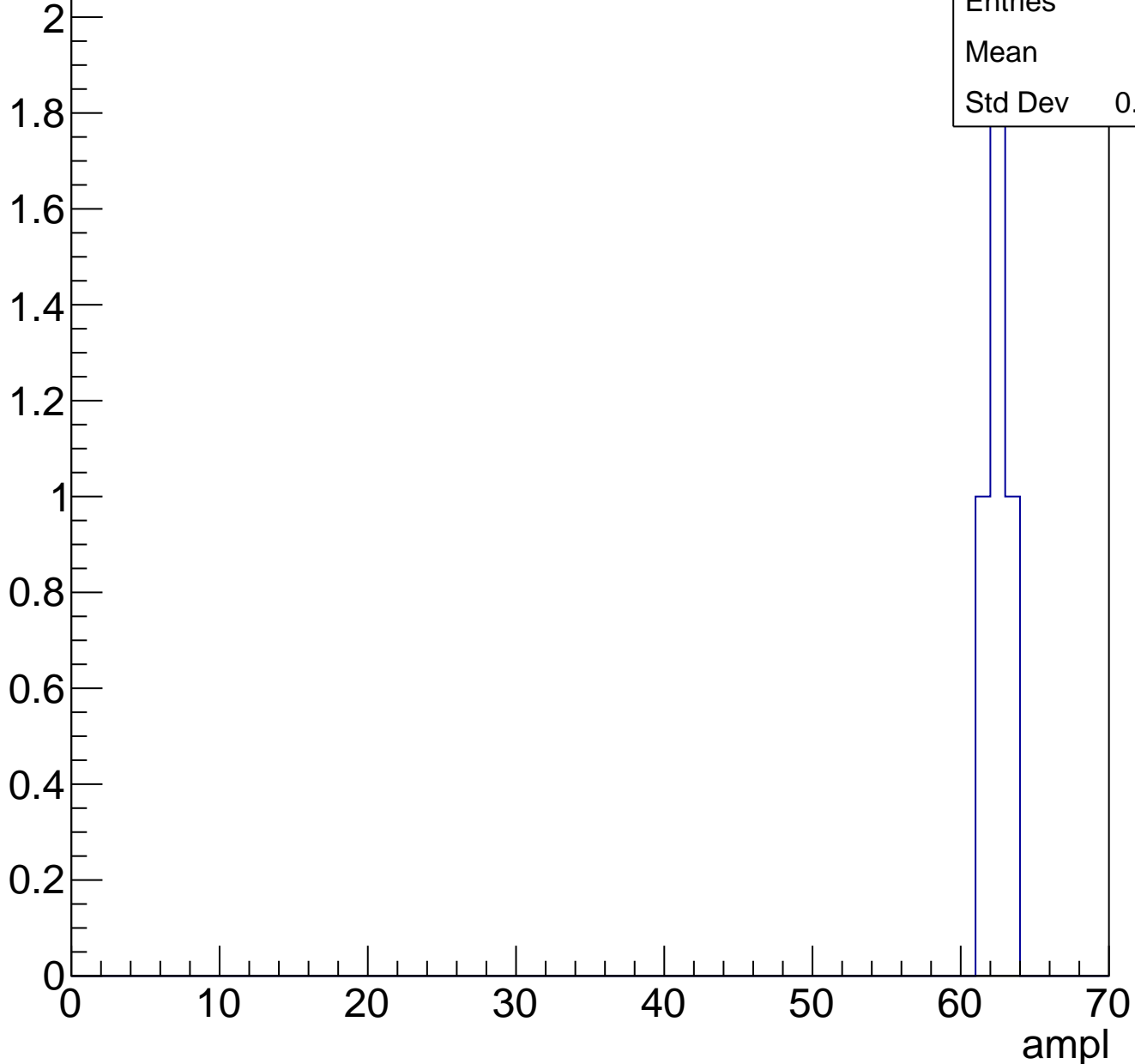




# B1L103S, U1-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch46, adc0

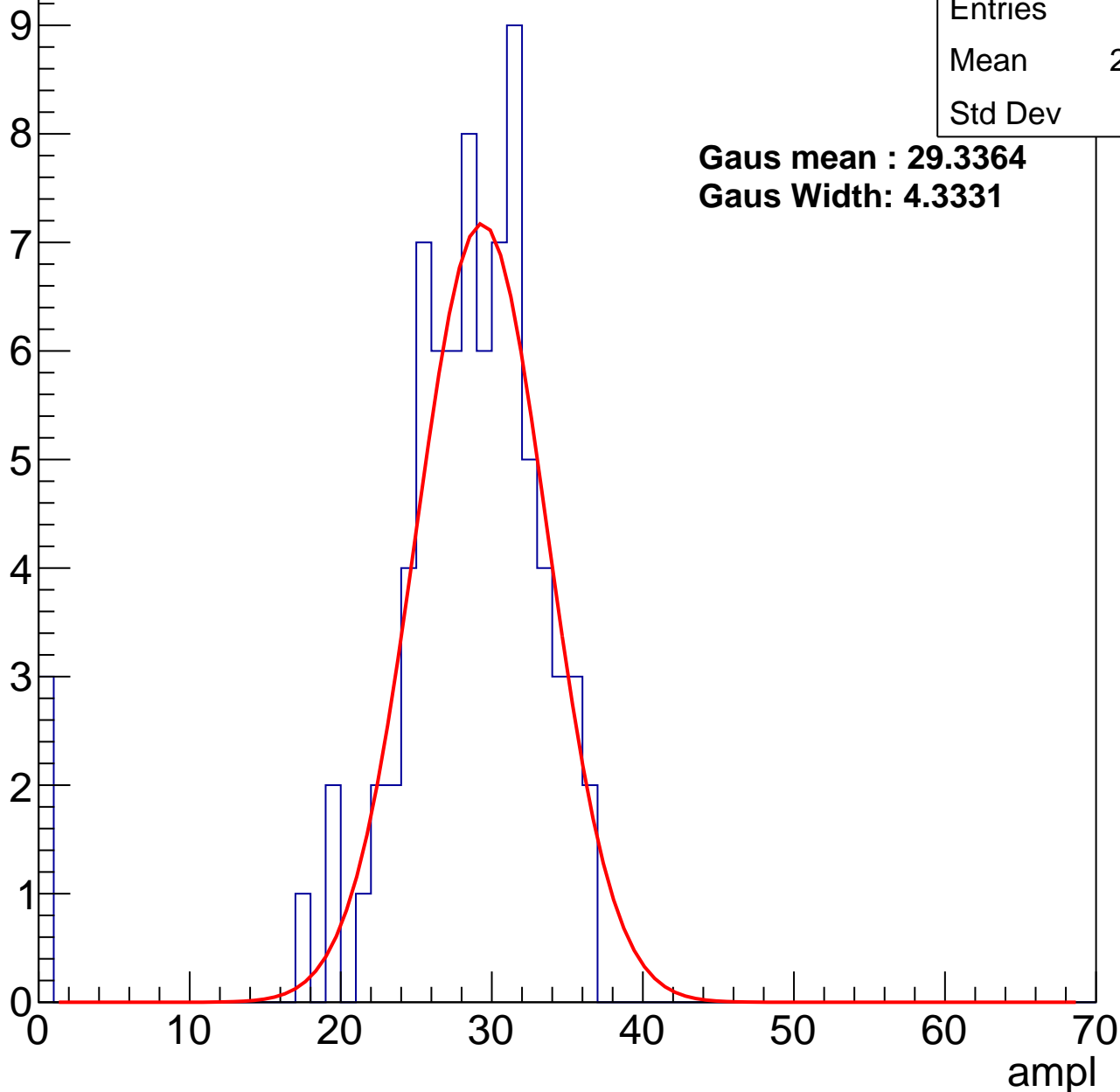
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	81
Mean	27.32
Std Dev	6.67

**Gaus mean : 29.3364**

**Gaus Width: 4.3331**



# B1L103S, U1-ch46, adc1

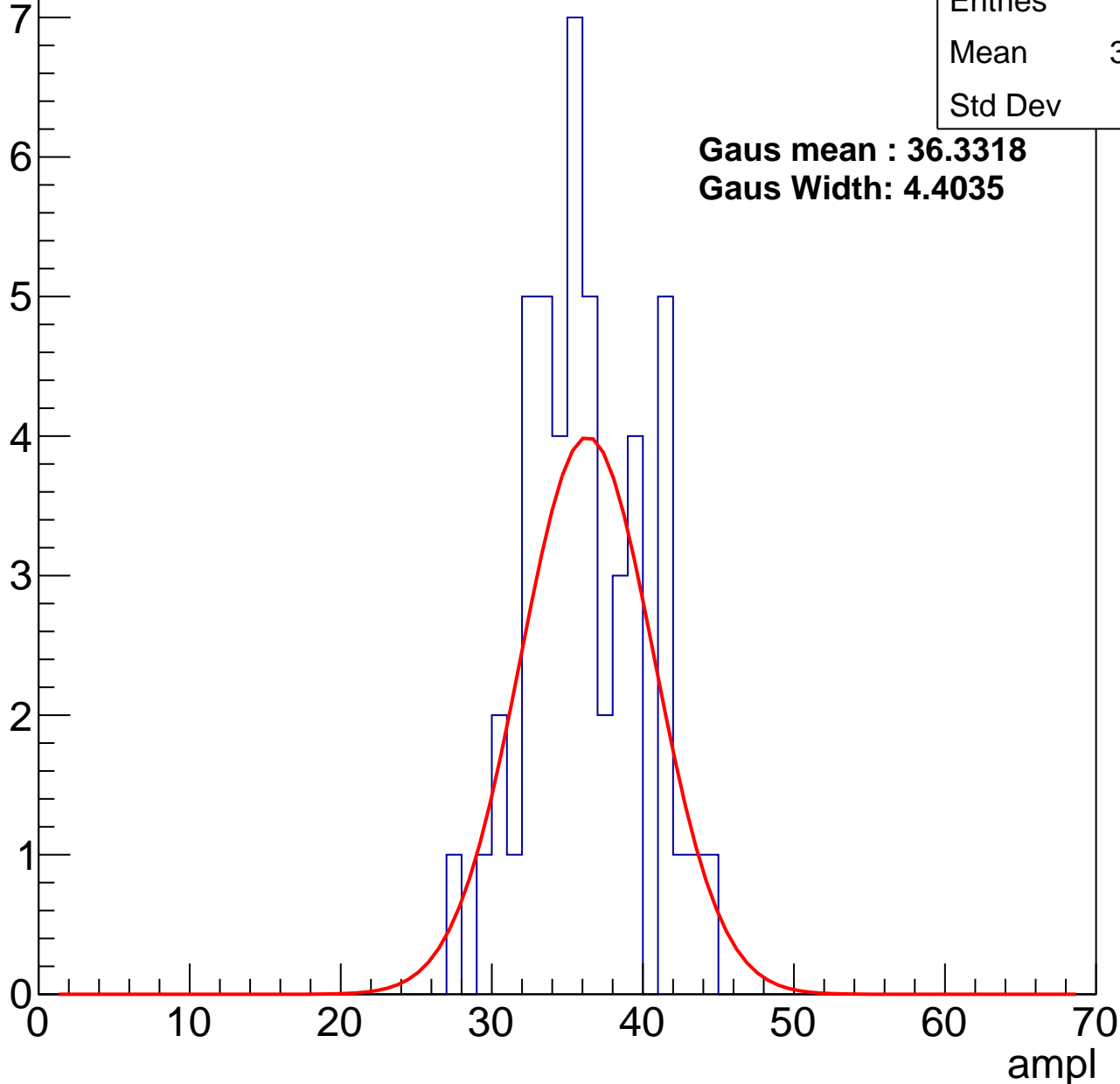
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	35.65
Std Dev	3.8

**Gaus mean : 36.3318**

**Gaus Width: 4.4035**



# B1L103S, U1-ch46, adc2

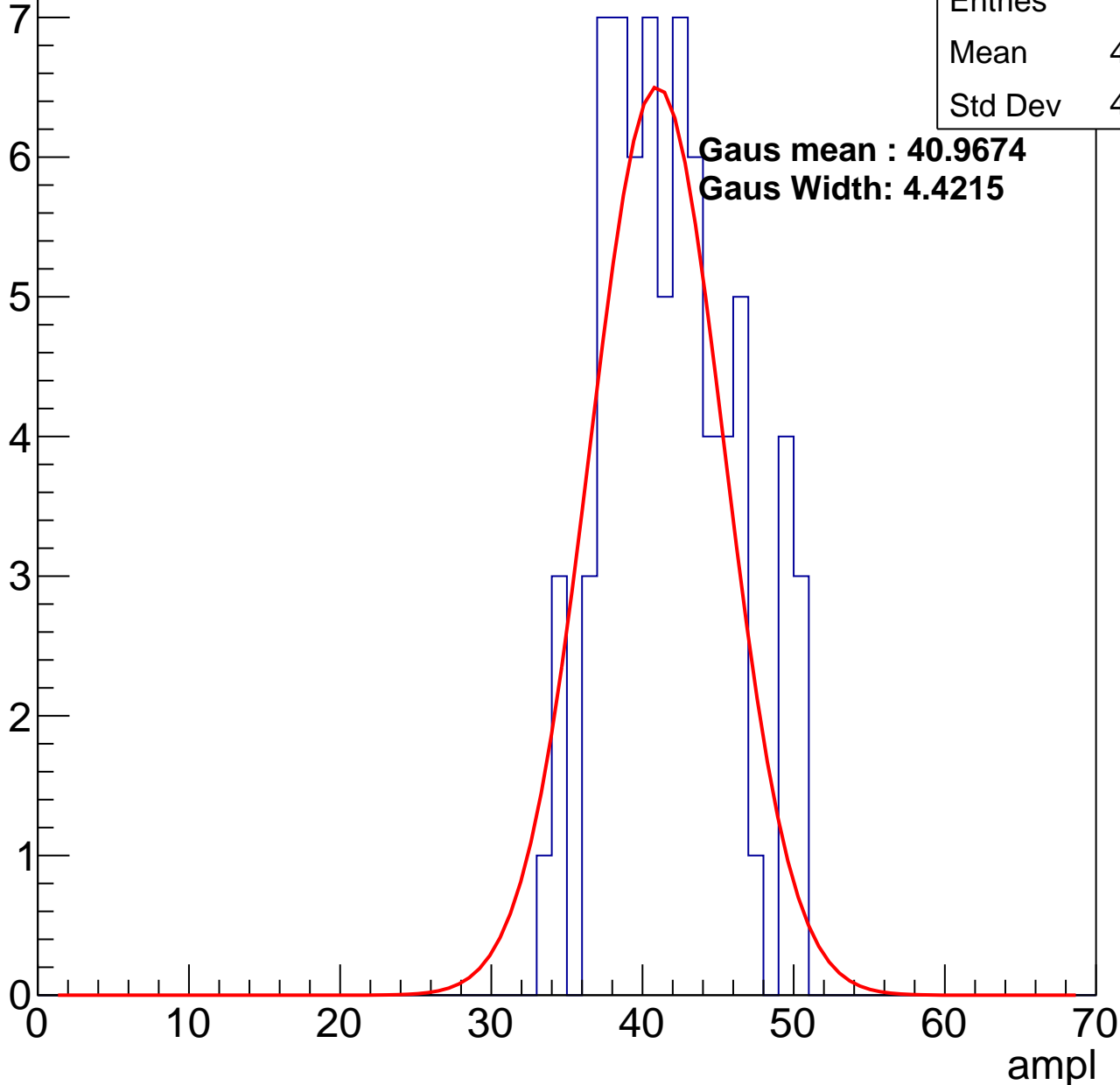
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	41.34
Std Dev	4.178

**Gaus mean : 40.9674**

**Gaus Width: 4.4215**

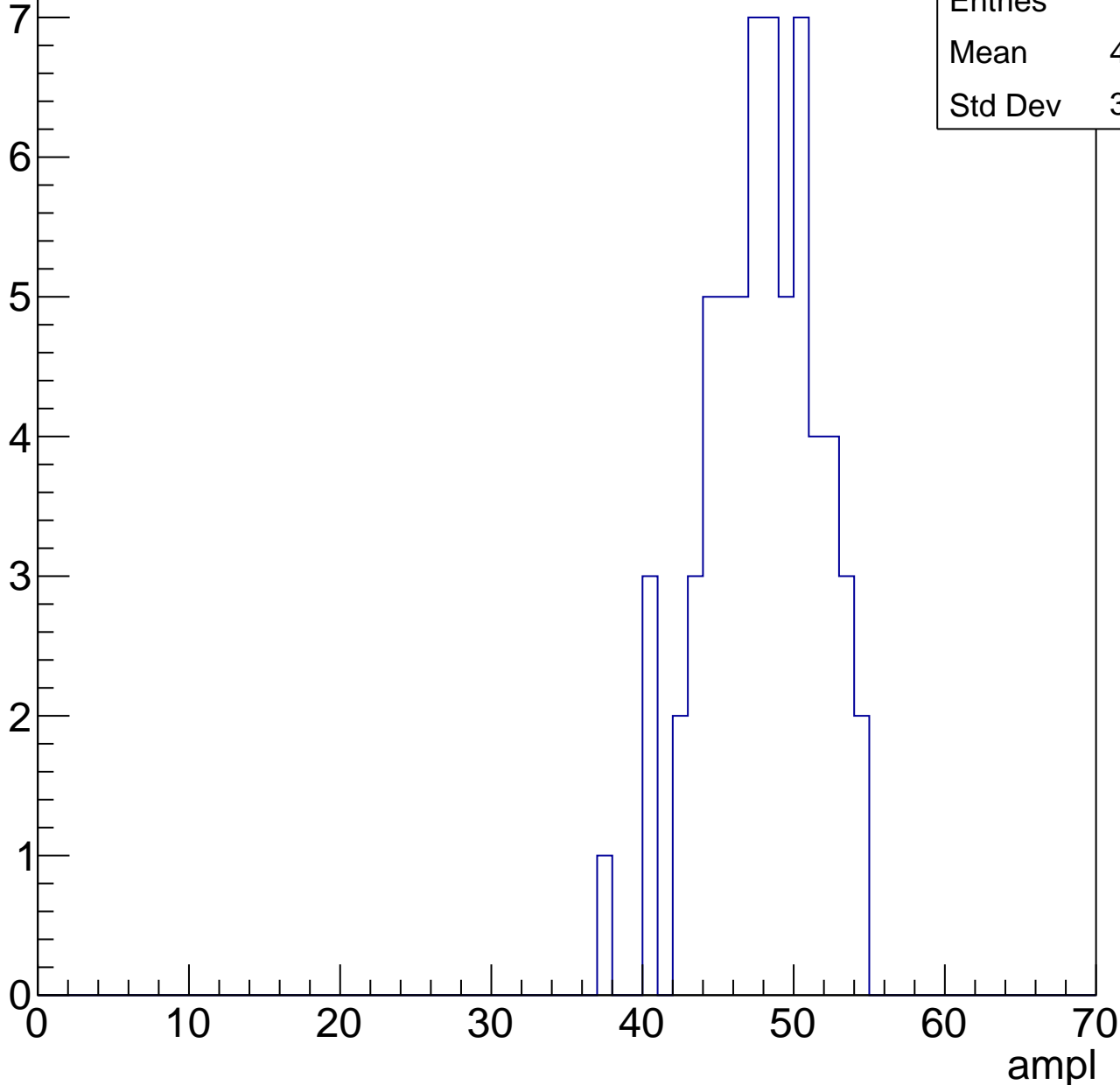


# B1L103S, U1-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	47.37
Std Dev	3.709

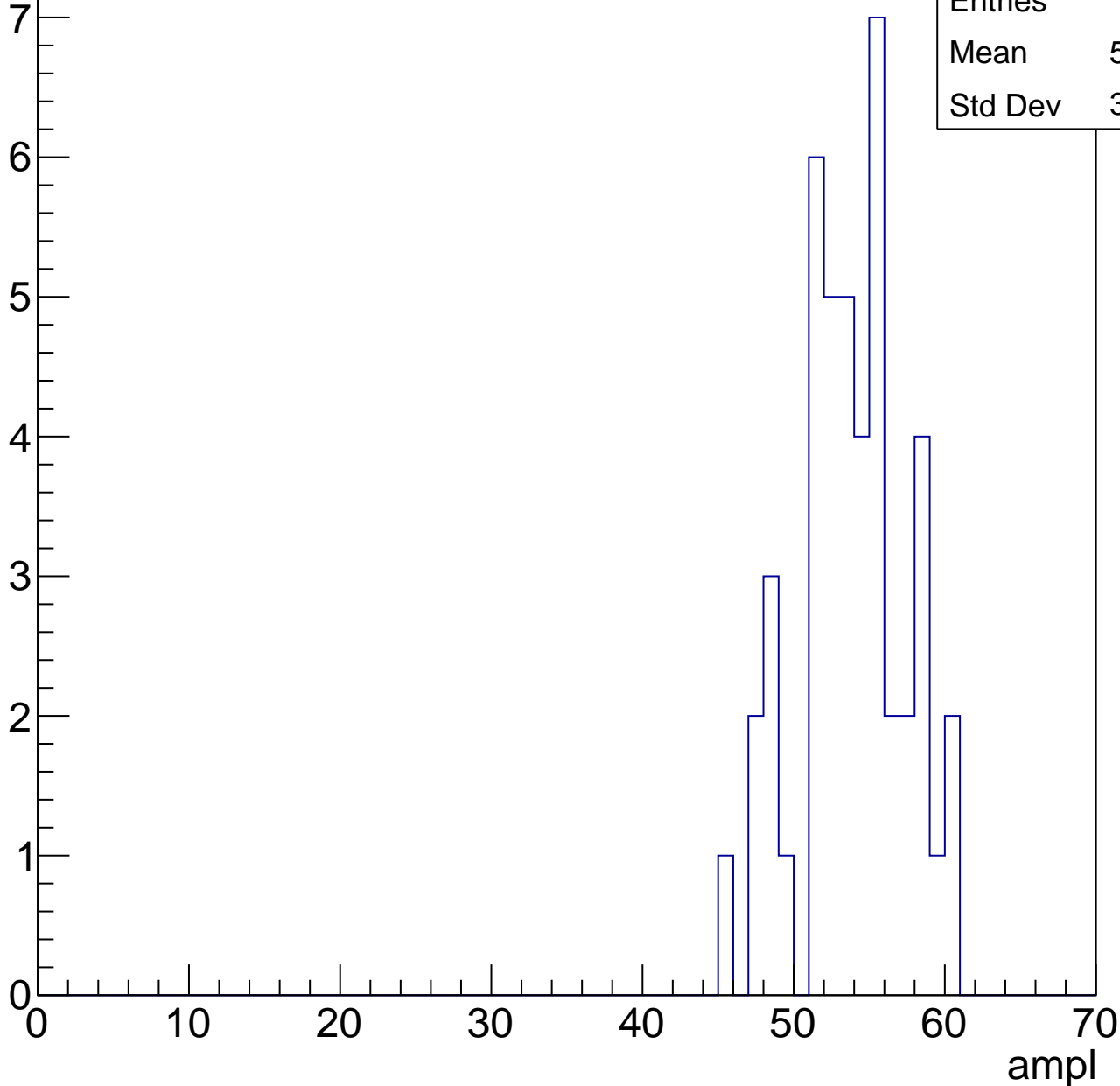


# B1L103S, U1-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

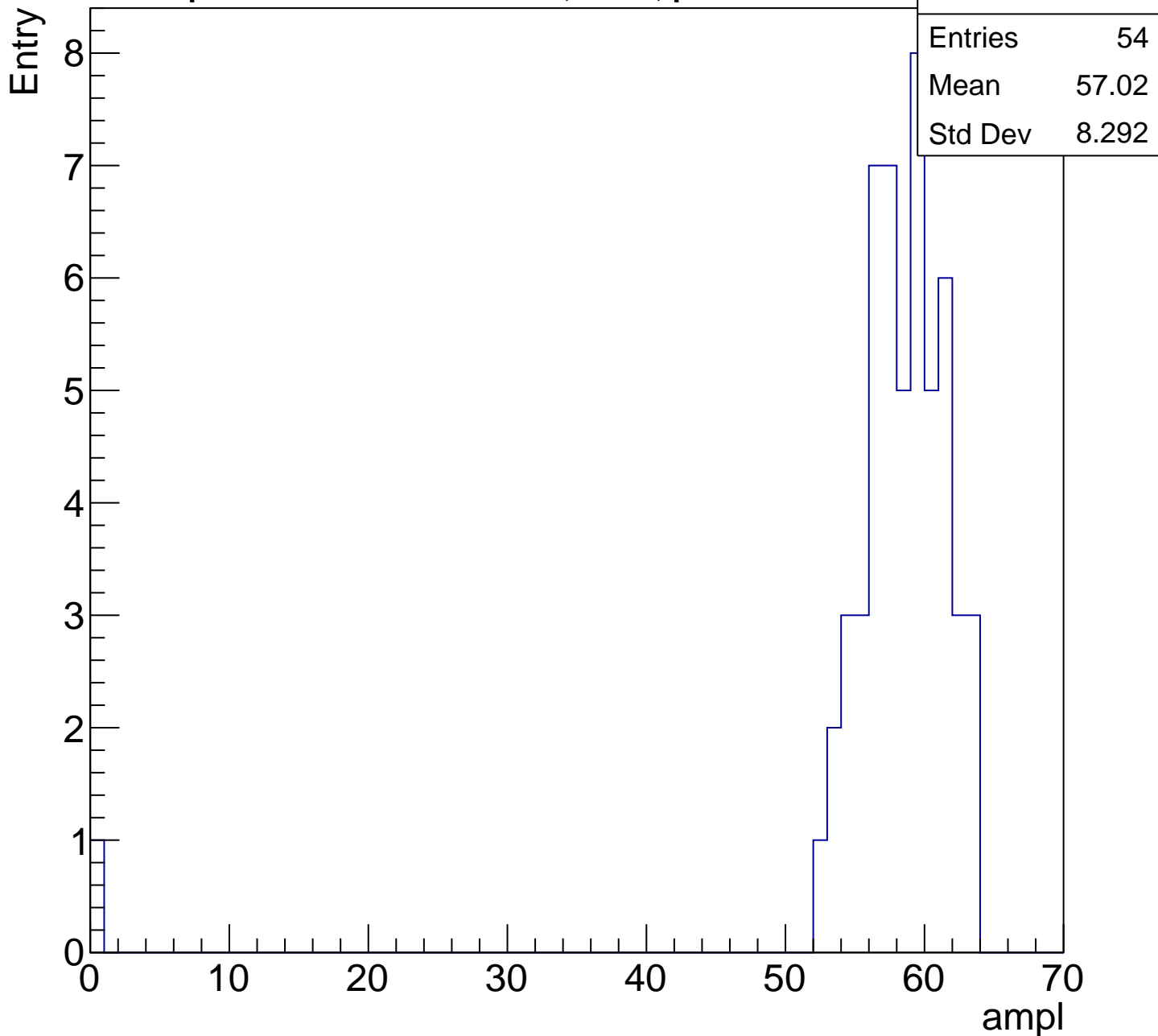
Entry

Entries	45
Mean	53.36
Std Dev	3.547



# B1L103S, U1-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

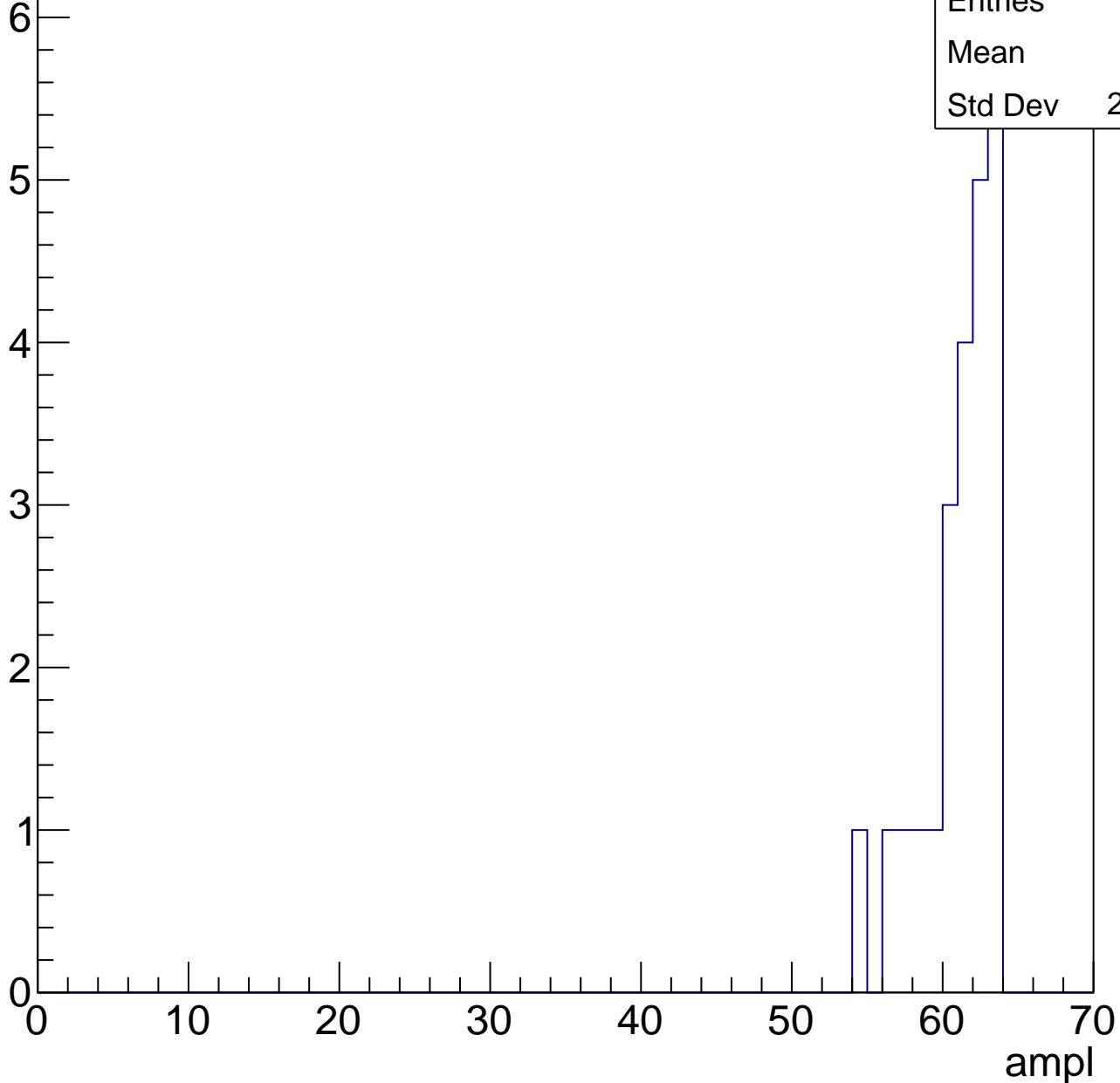


# B1L103S, U1-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	23
Mean	60.7
Std Dev	2.404

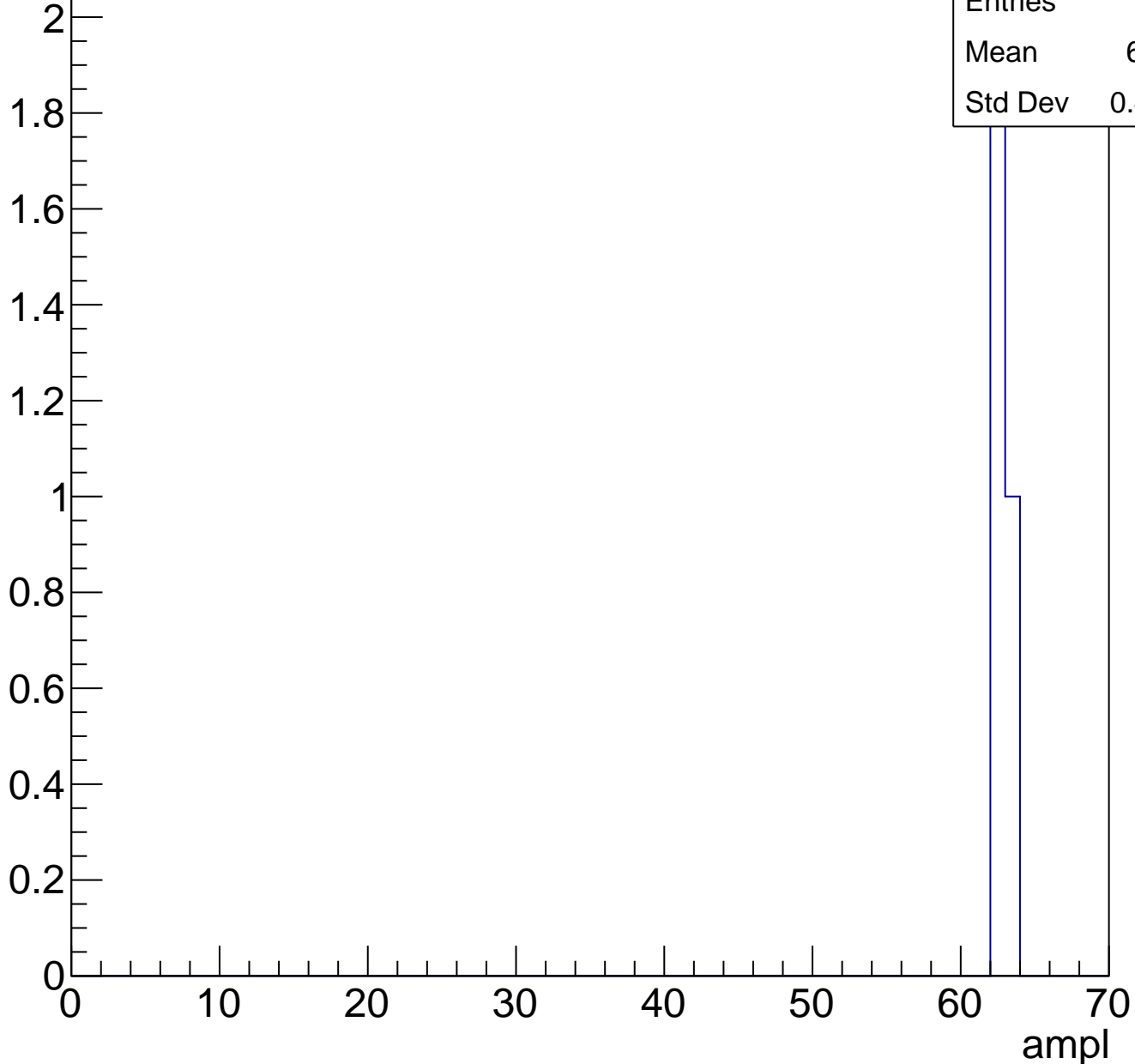




# B1L103S, U1-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch47, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	73
Mean	27.1
Std Dev	5.569

**Gaus mean : 28.4256**

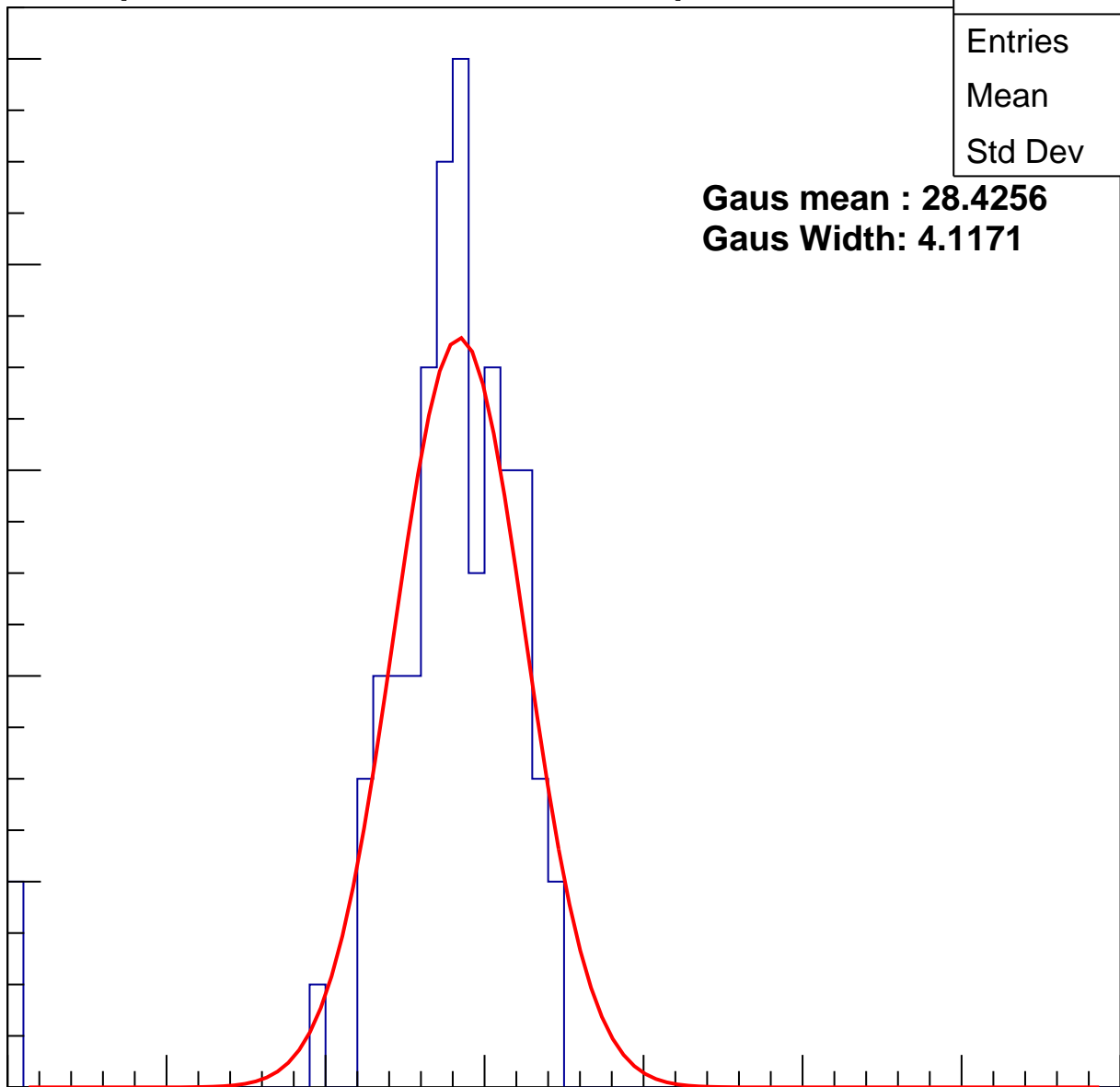
**Gaus Width: 4.1171**

Entry

10  
8  
6  
4  
2  
0

ampl

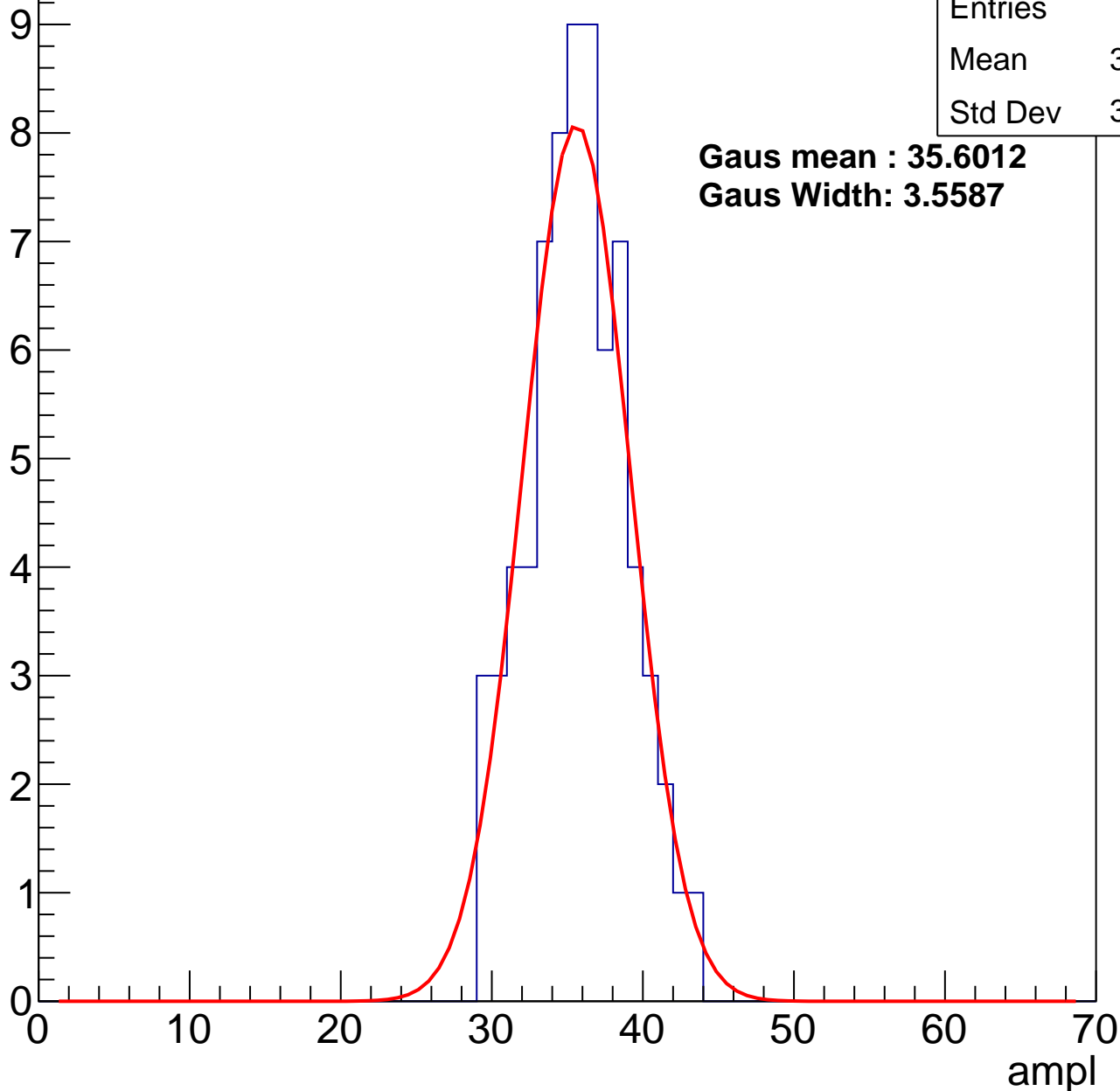
0 10 20 30 40 50 60 70



# B1L103S, U1-ch47, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch47, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	57
Mean	41.75
Std Dev	3.153

**Gaus mean : 42.0275**

**Gaus Width: 3.1082**

Entry

10  
8  
6  
4  
2  
0

ampl

0

10

20

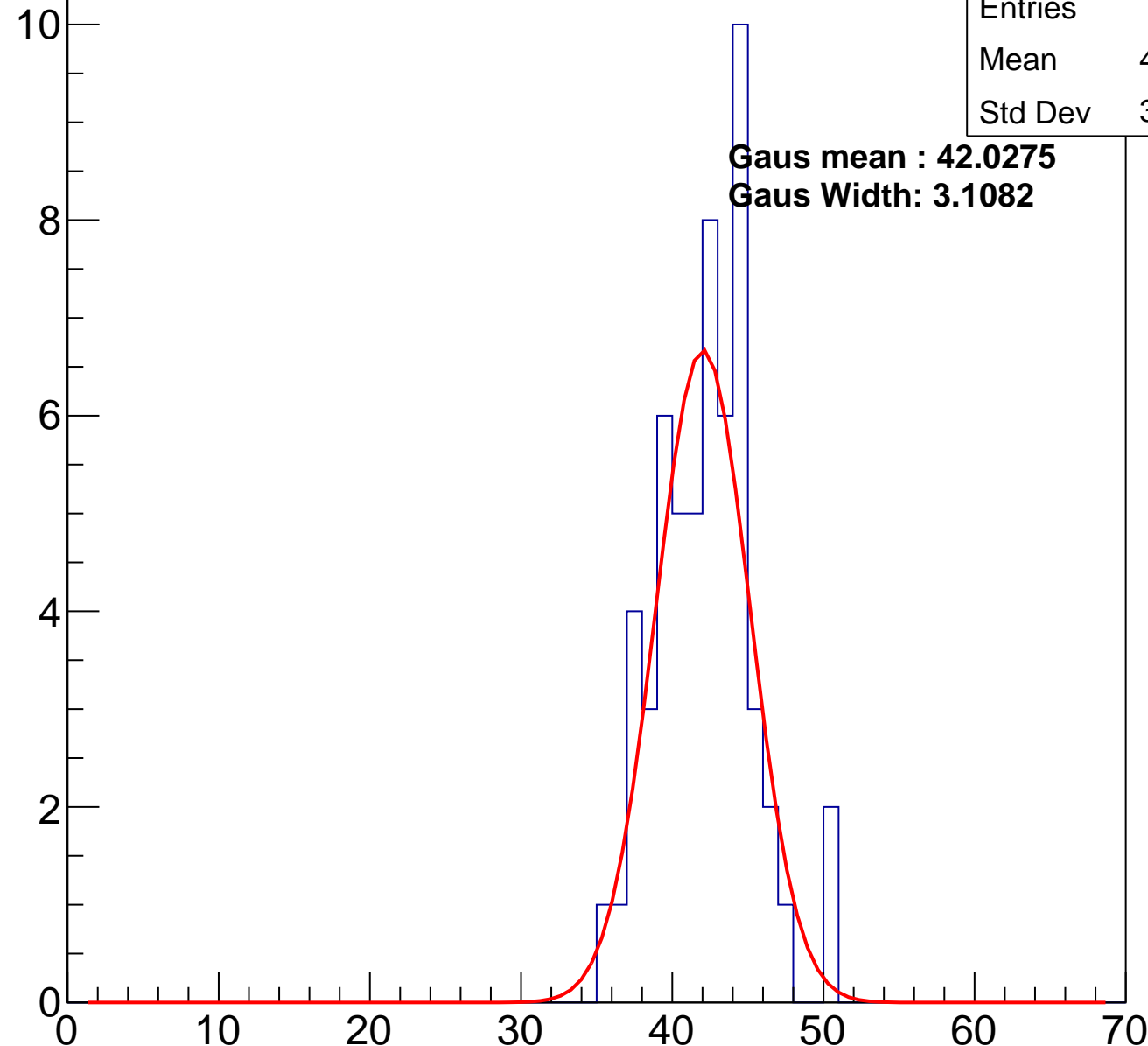
30

40

50

60

70

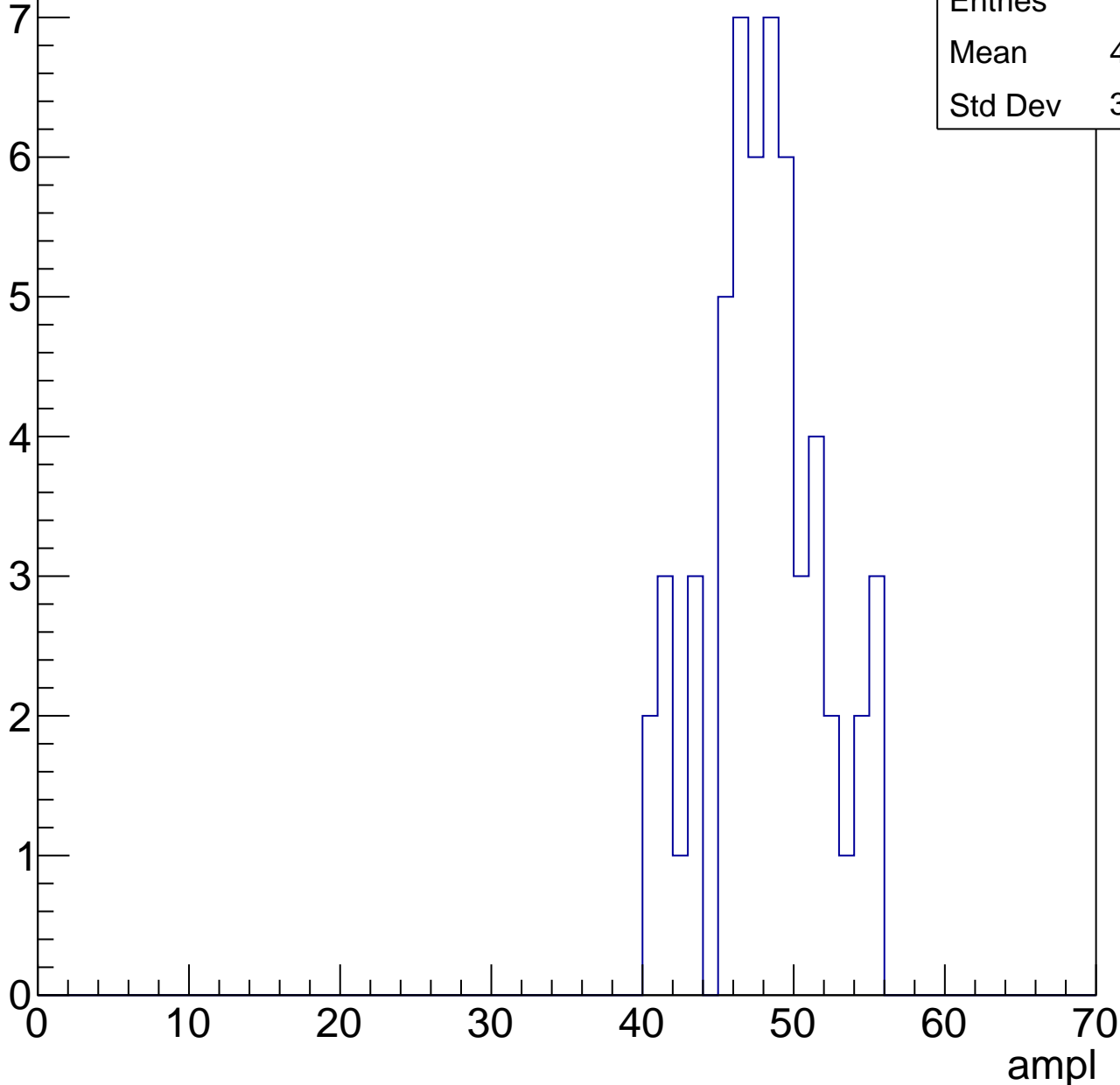


# B1L103S, U1-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

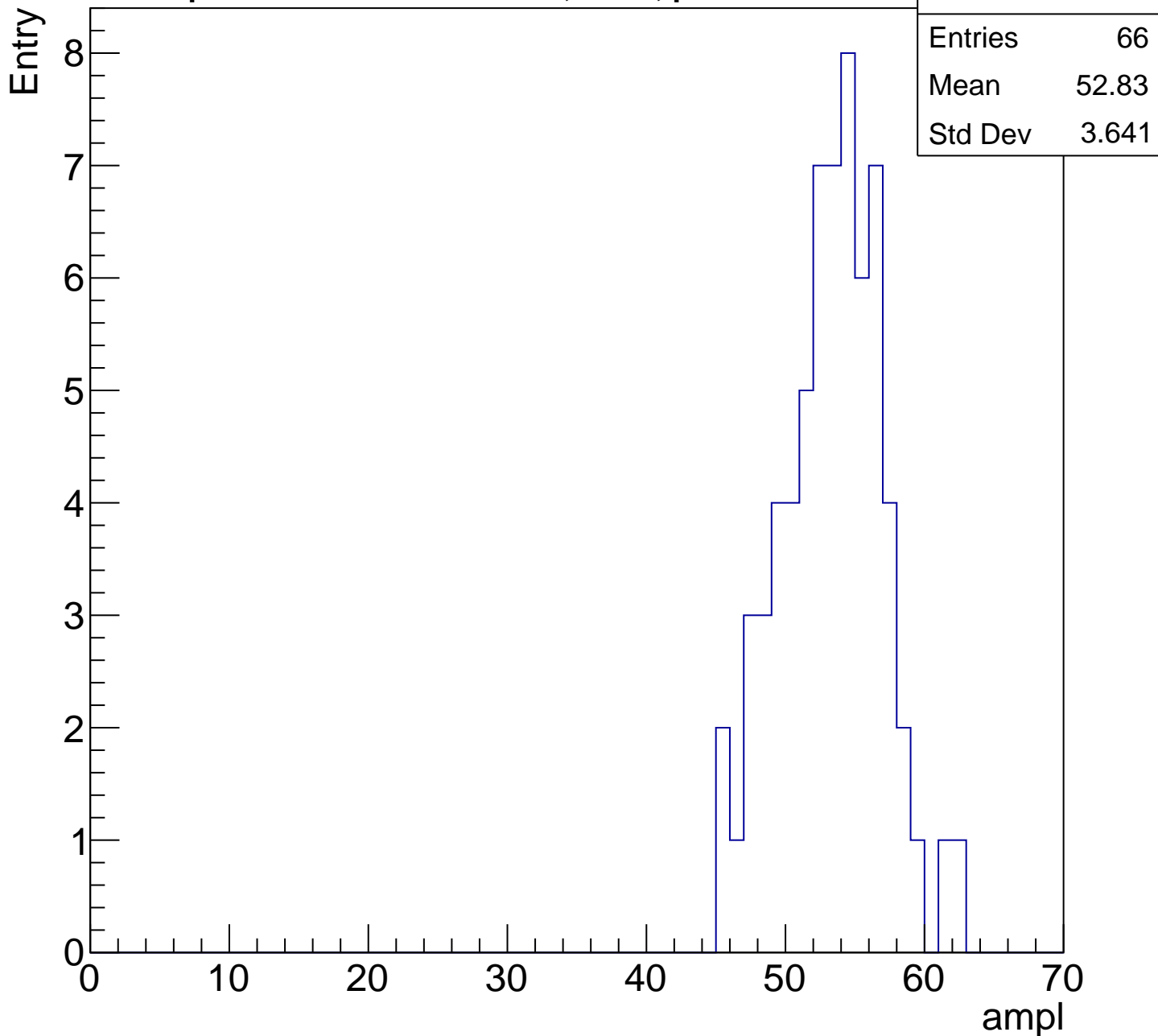
Entry

Entries	55
Mean	47.58
Std Dev	3.779



# B1L103S, U1-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U1-ch47, adc5

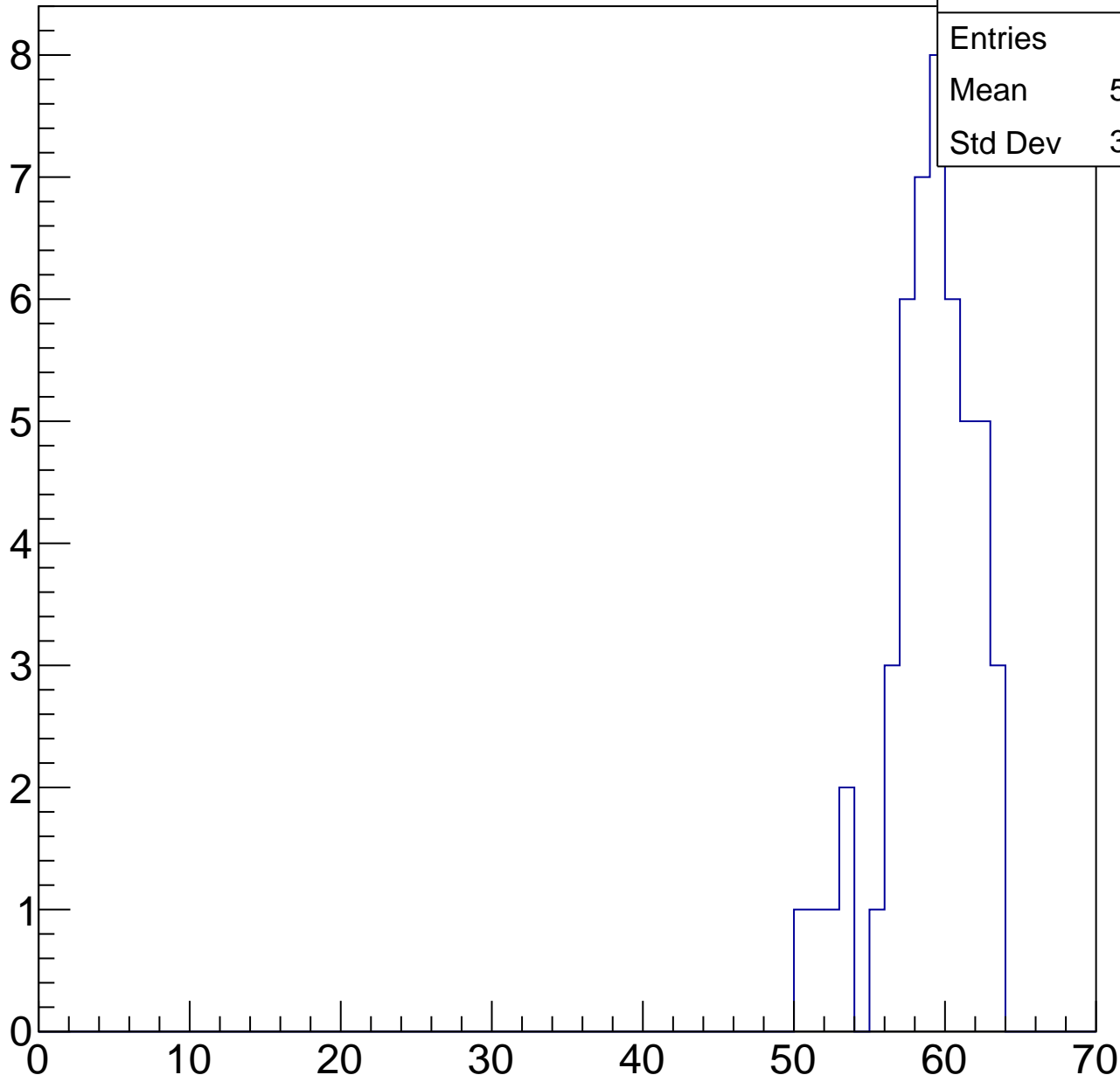
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	58.49
Std Dev	3.018

ampl

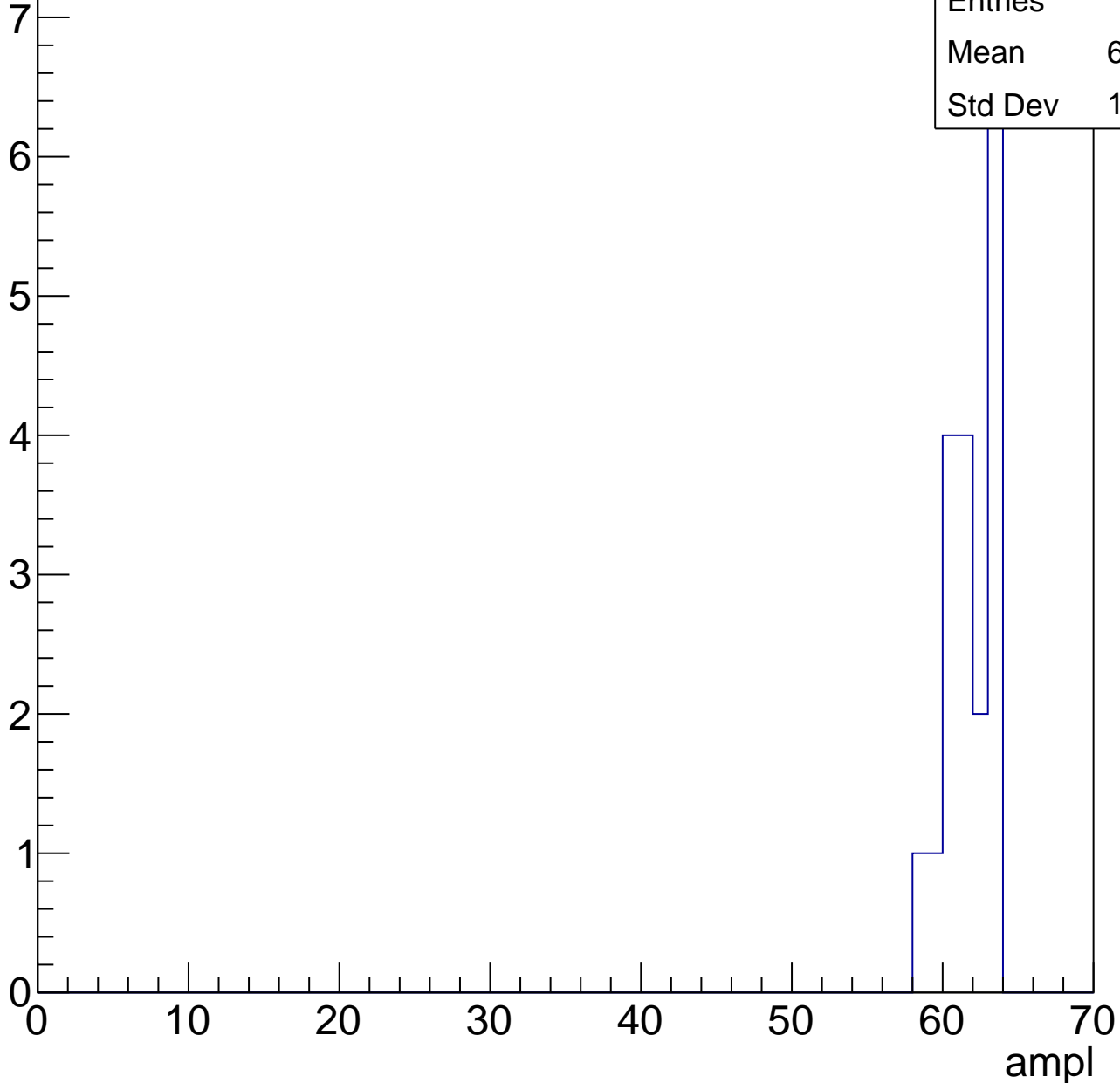


# B1L103S, U1-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	19
Mean	61.37
Std Dev	1.529

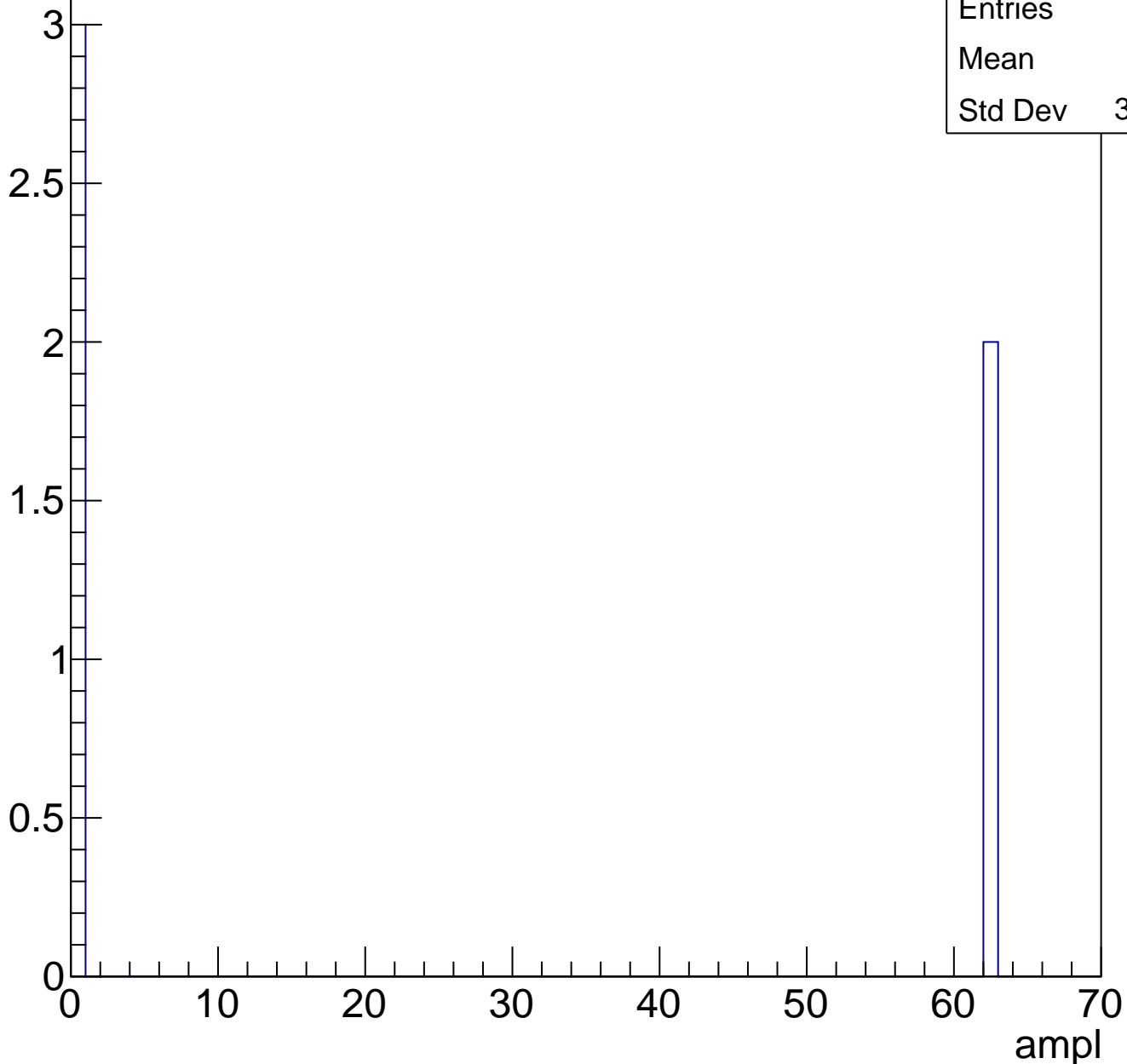




# B1L103S, U1-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch48, adc0

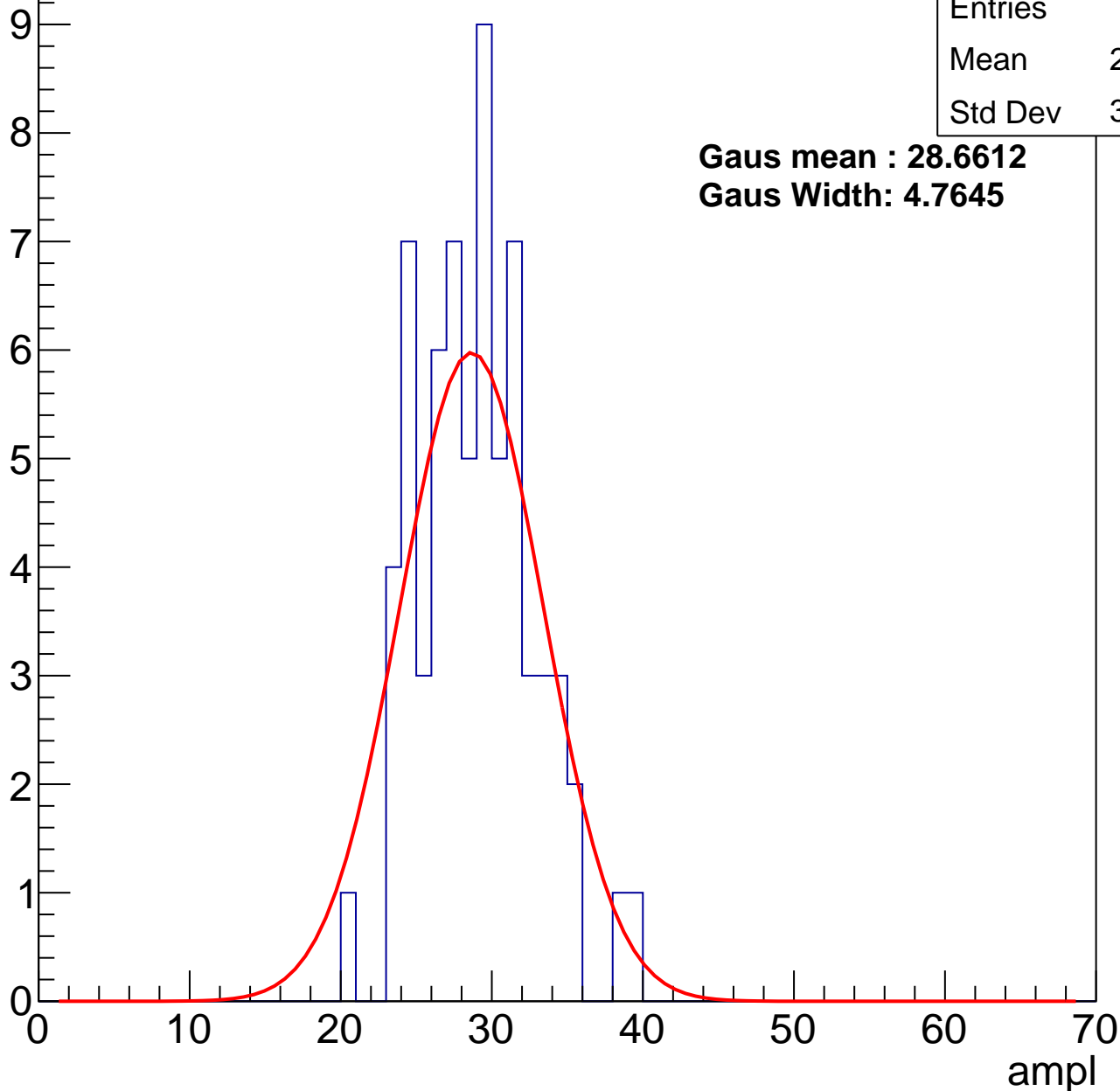
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	28.54
Std Dev	3.779

**Gaus mean : 28.6612**

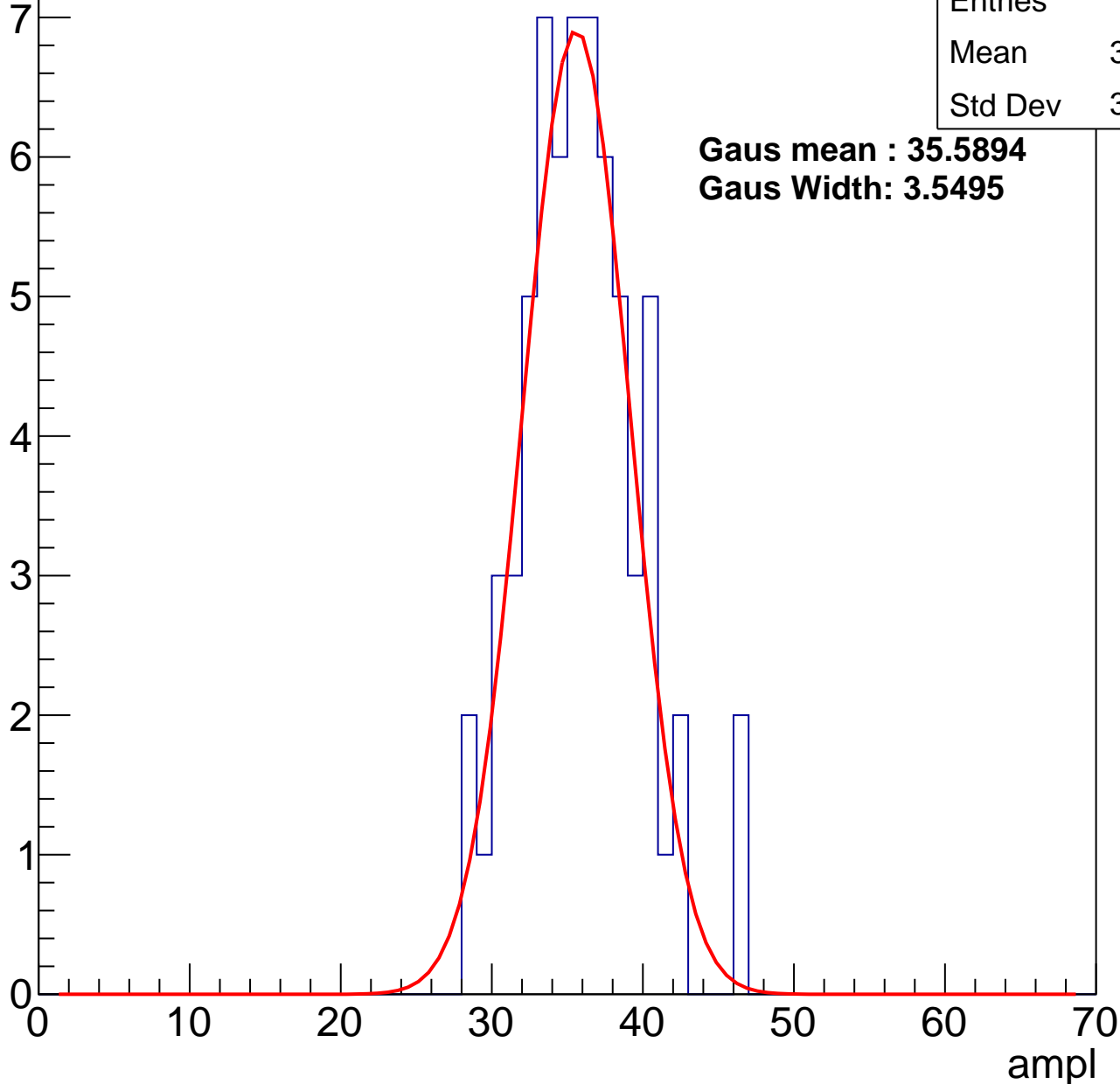
**Gaus Width: 4.7645**



# B1L103S, U1-ch48, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch48, adc2

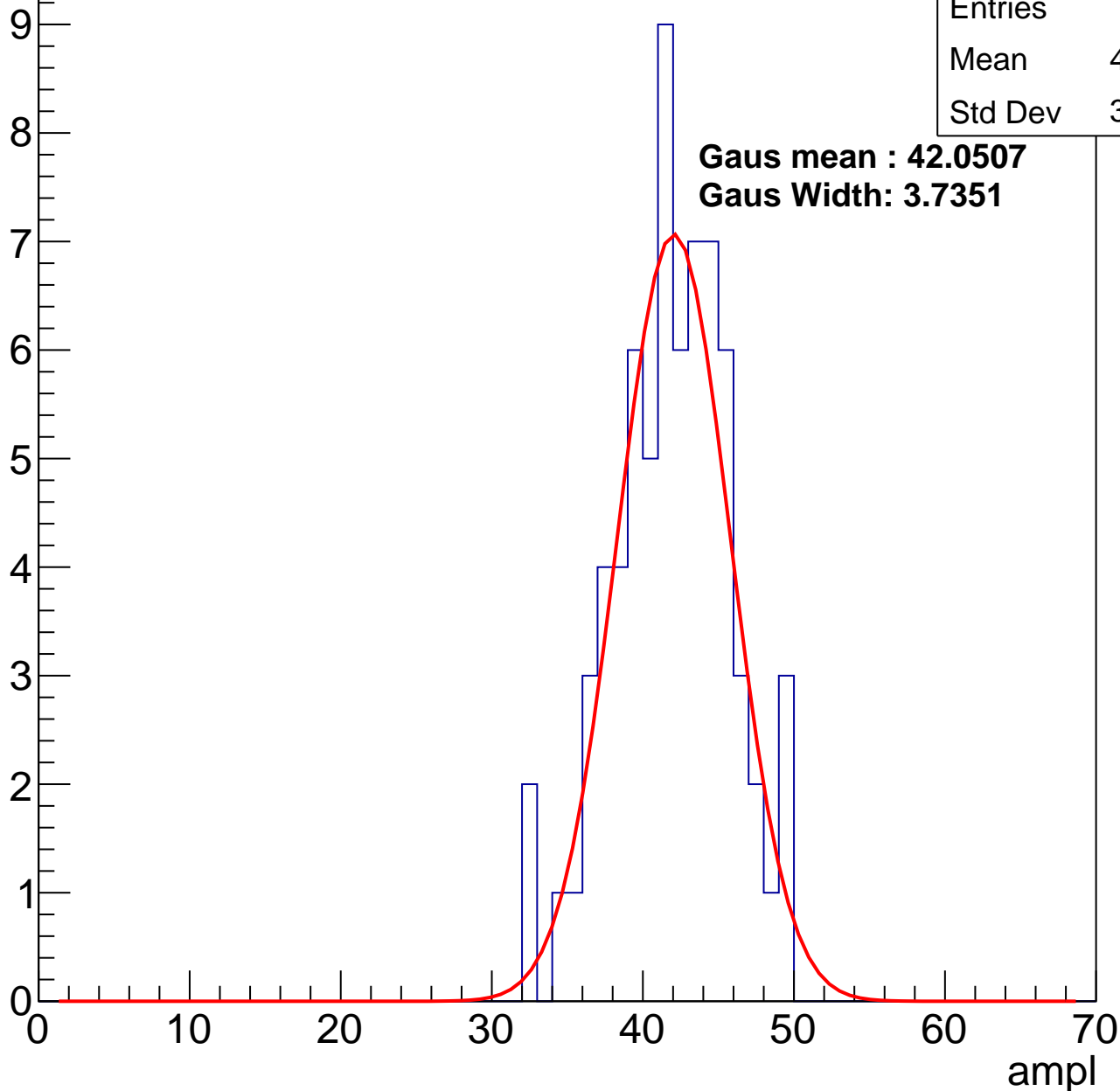
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	41.46
Std Dev	3.812

**Gaus mean : 42.0507**

**Gaus Width: 3.7351**

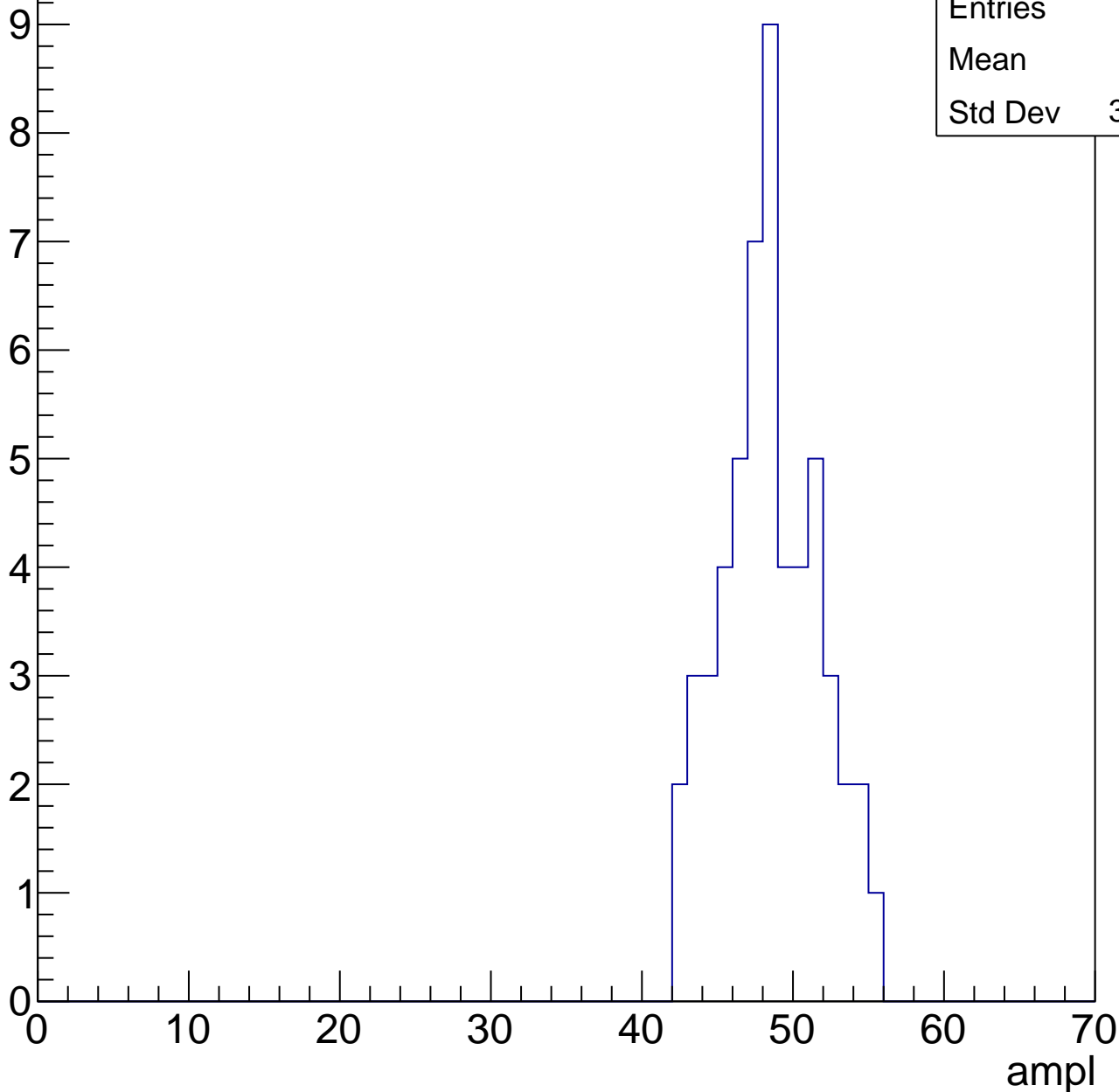


# B1L103S, U1-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	48
Std Dev	3.168

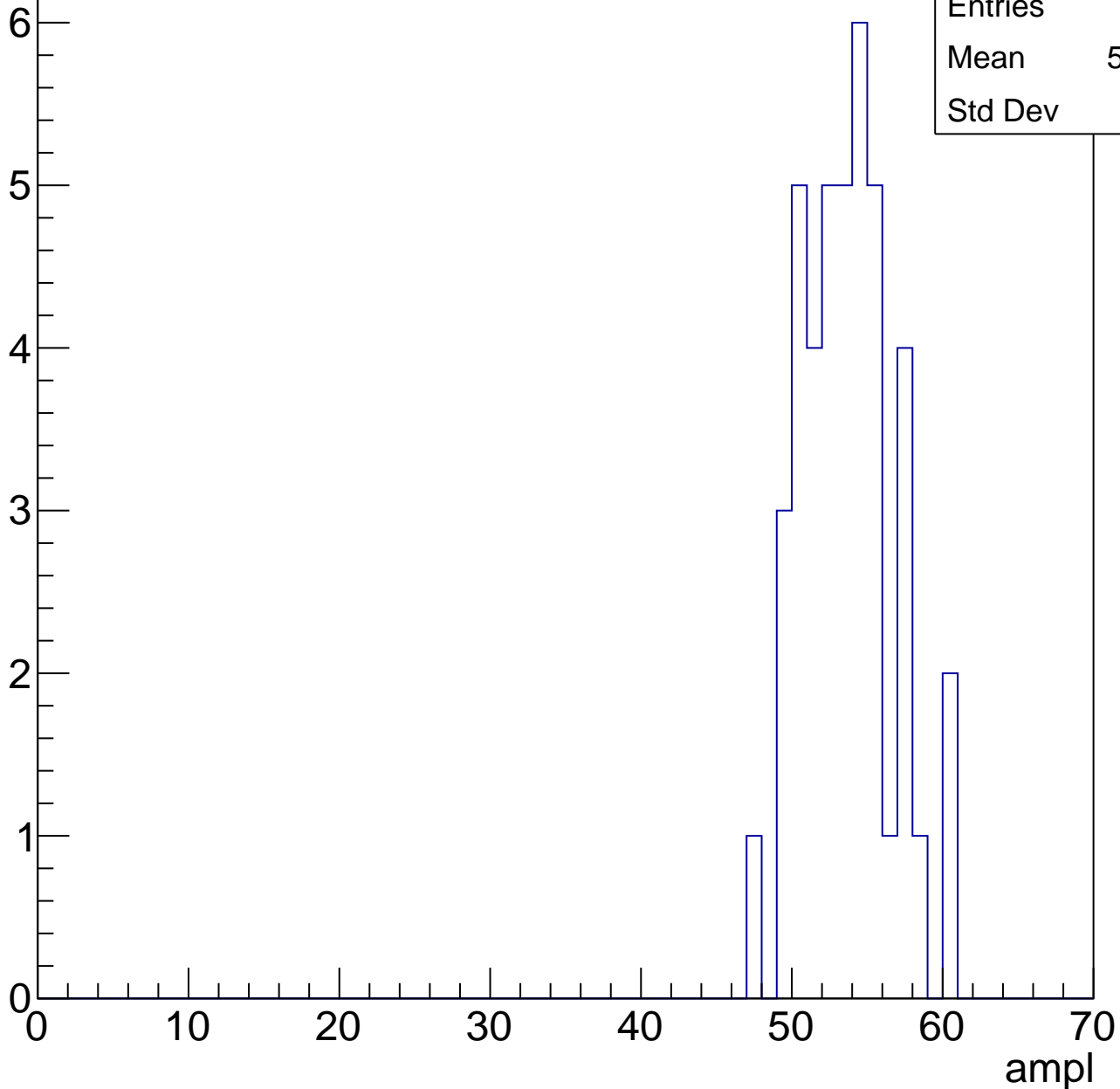


# B1L103S, U1-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

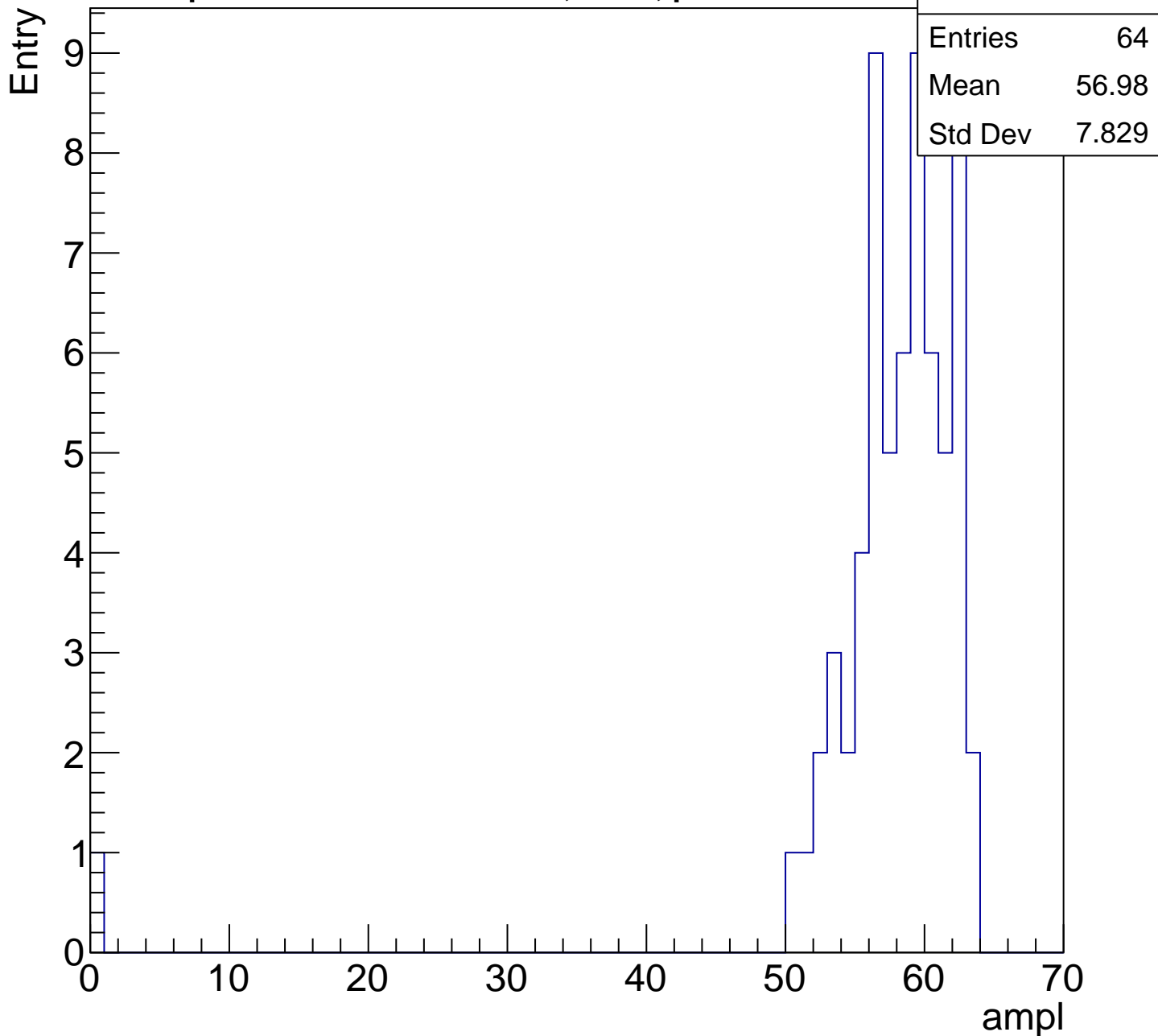
Entry

Entries	42
Mean	53.19
Std Dev	2.97



# B1L103S, U1-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

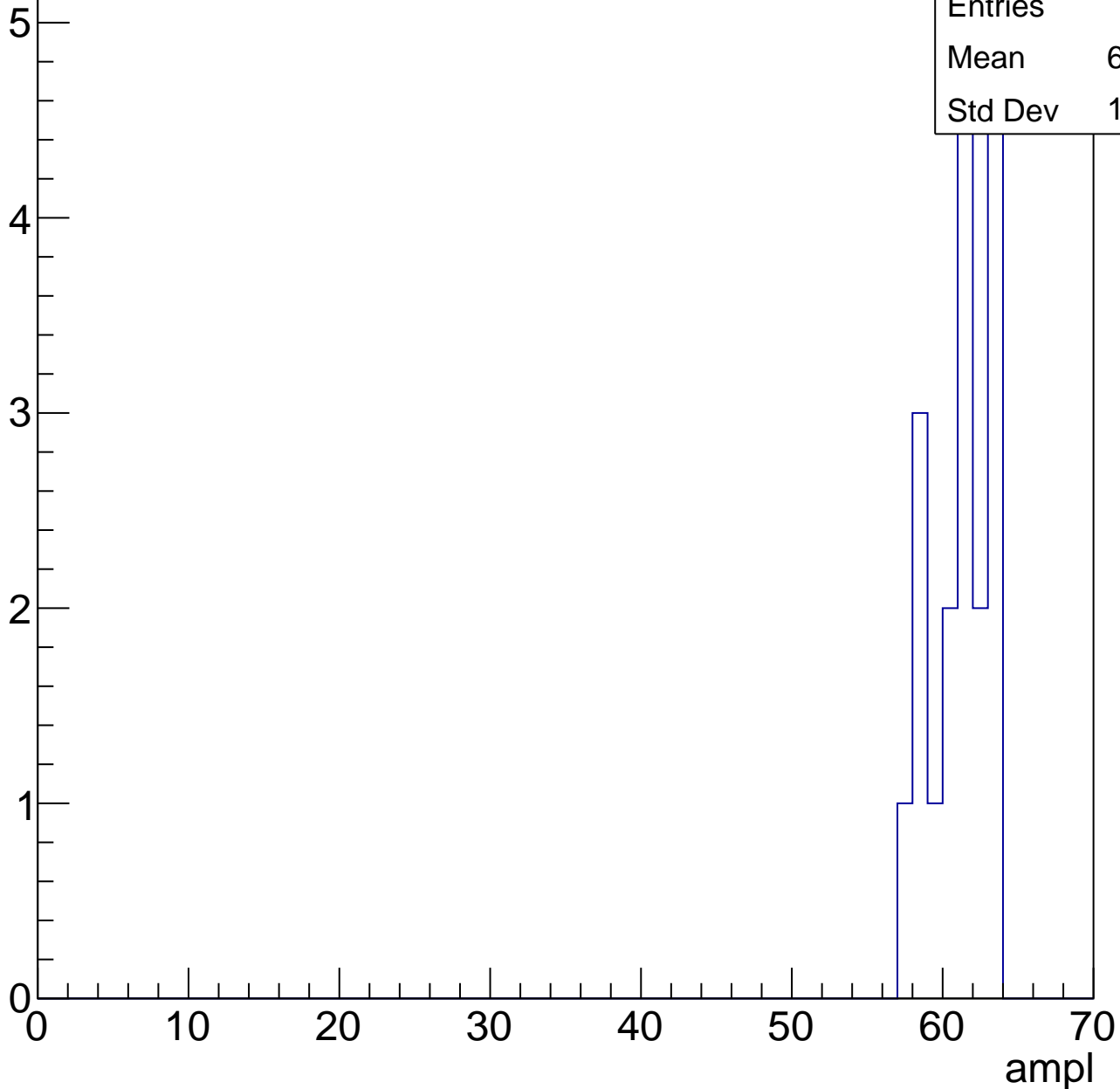


# B1L103S, U1-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	19
Mean	60.74
Std Dev	1.915

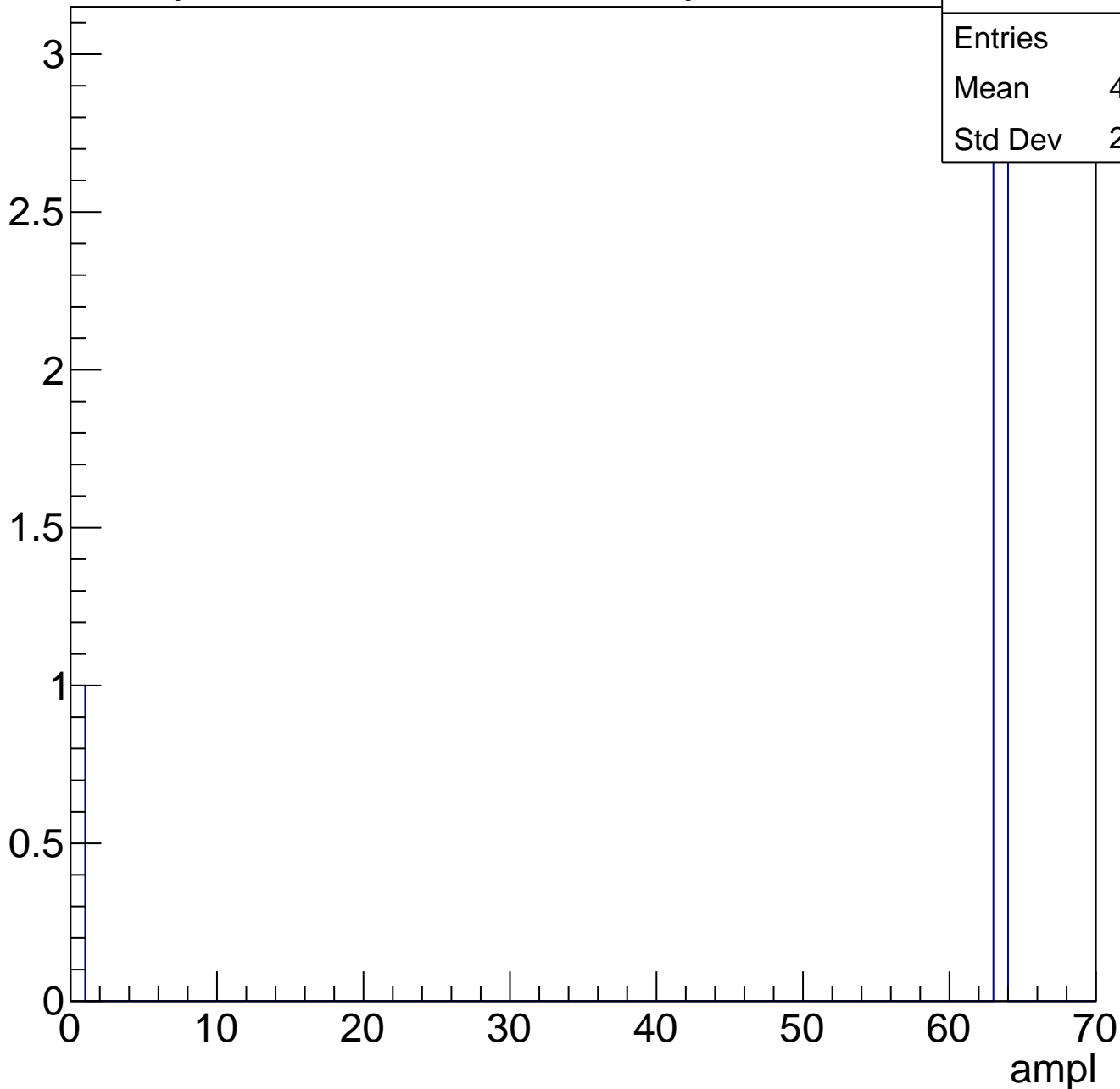




# B1L103S, U1-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch49, adc0

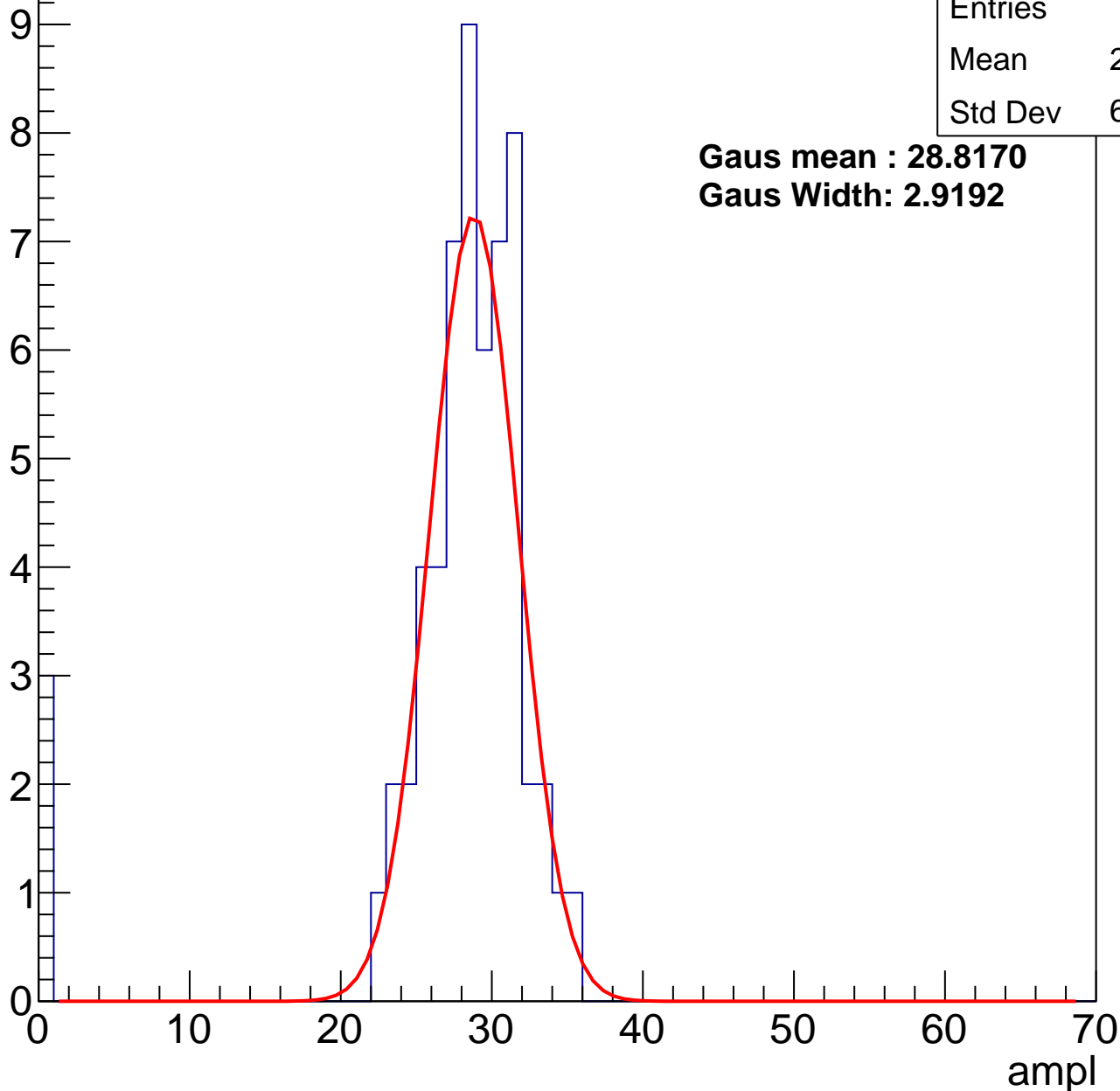
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	26.98
Std Dev	6.816

**Gaus mean : 28.8170**

**Gaus Width: 2.9192**



# B1L103S, U1-ch49, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	78
Mean	35
Std Dev	3.714

**Gaus mean : 35.4864**

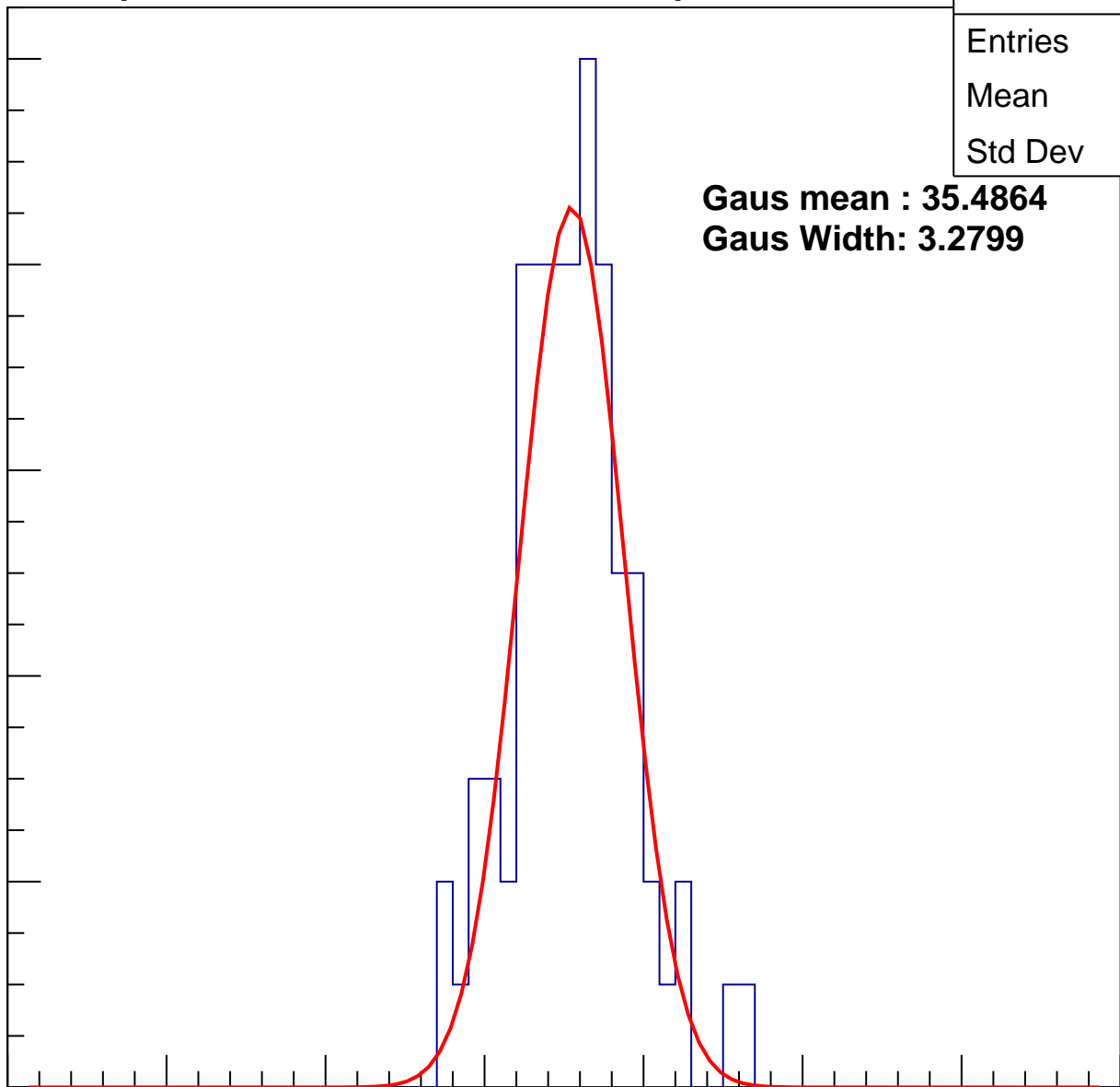
**Gaus Width: 3.2799**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U1-ch49, adc2

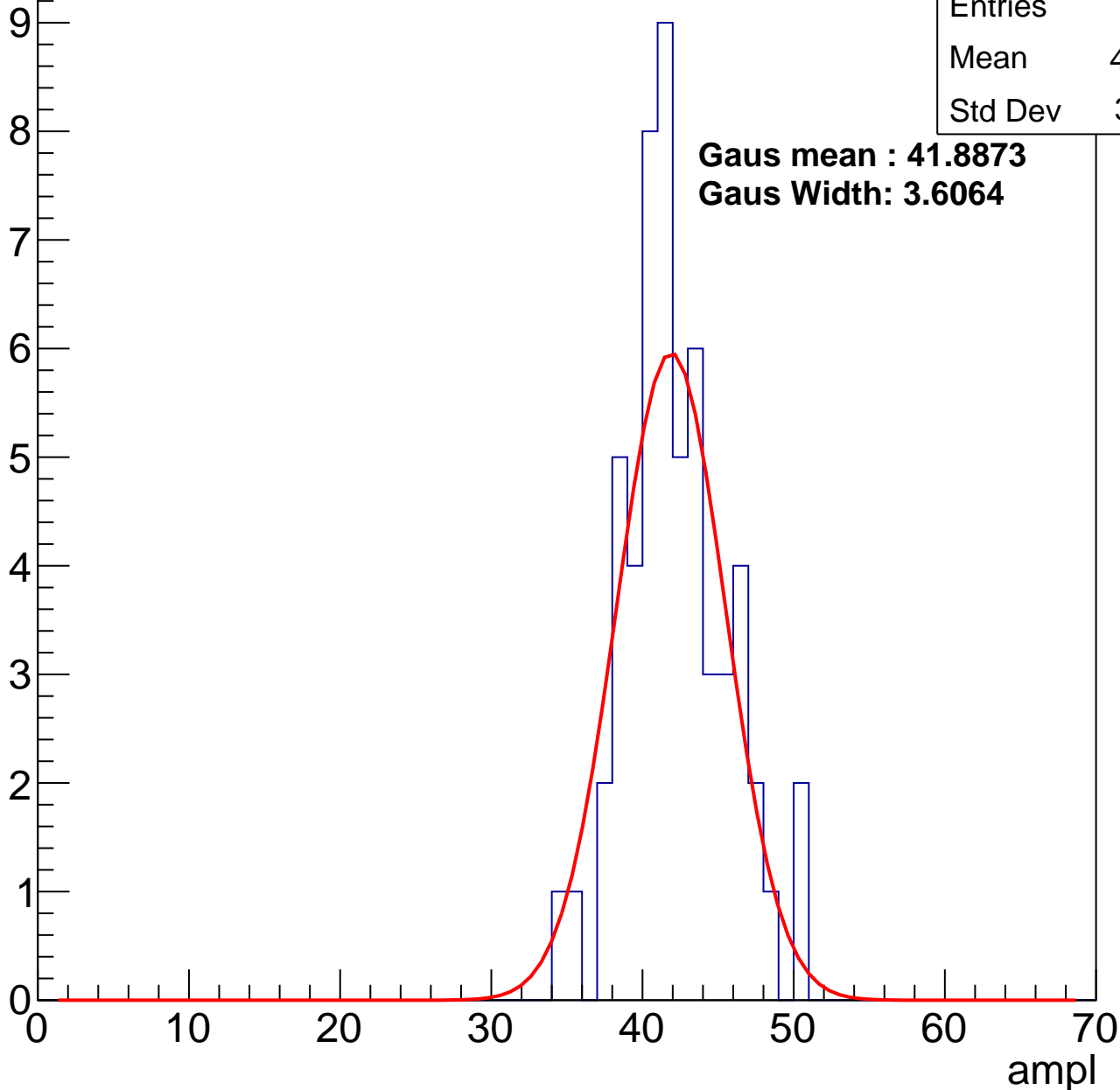
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	41.77
Std Dev	3.381

**Gaus mean : 41.8873**

**Gaus Width: 3.6064**

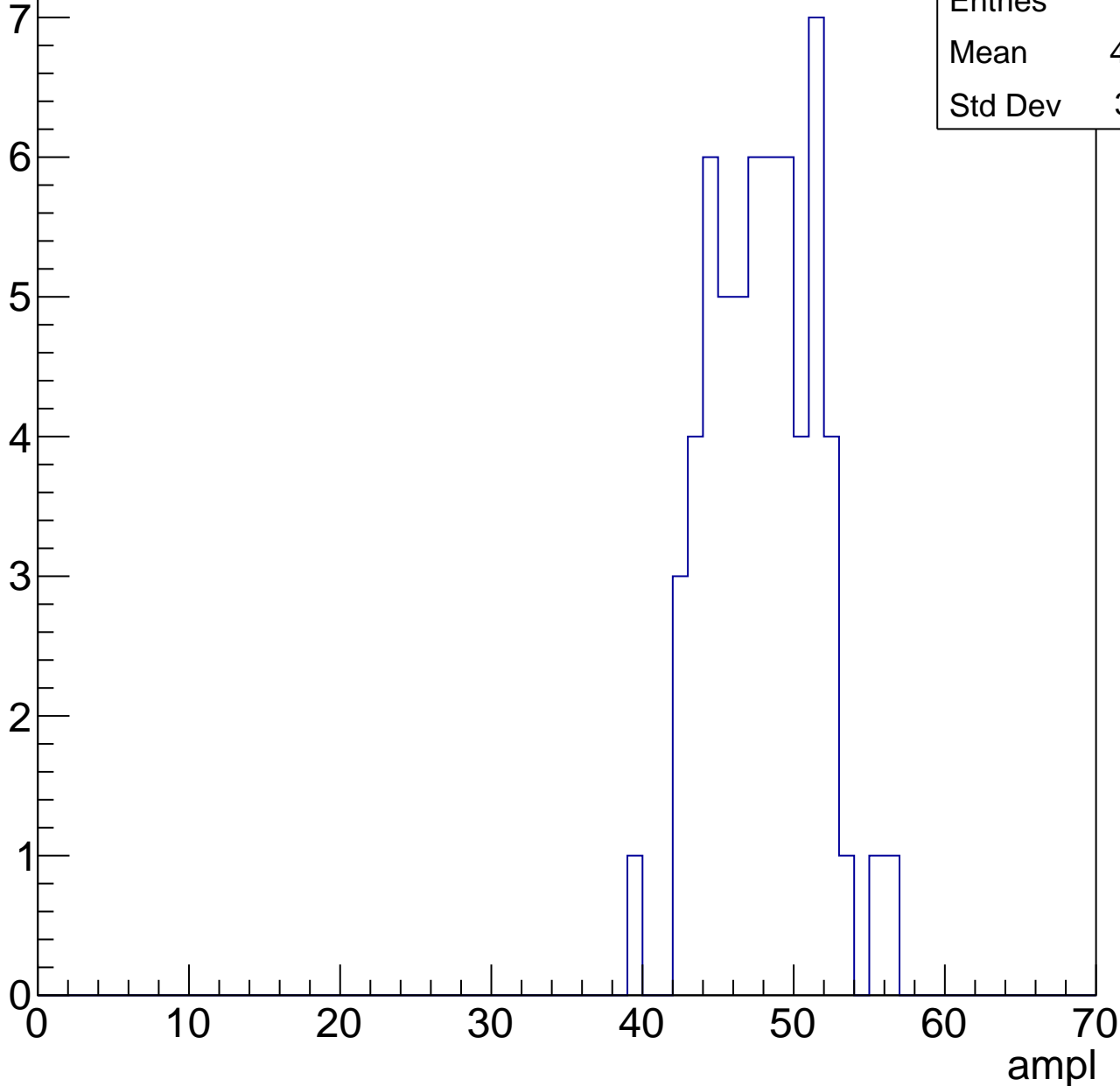


# B1L103S, U1-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	47.48
Std Dev	3.481

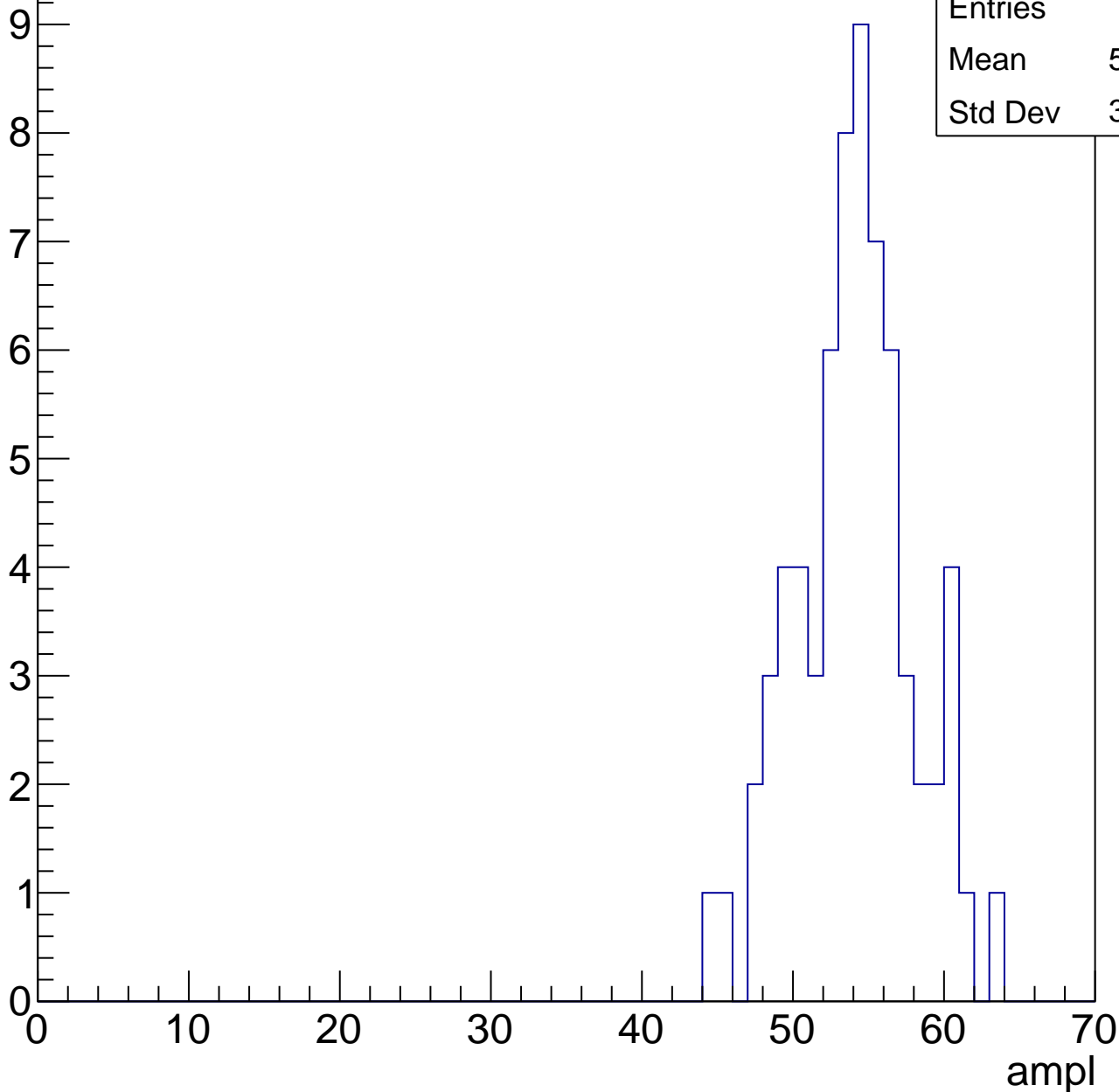


# B1L103S, U1-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

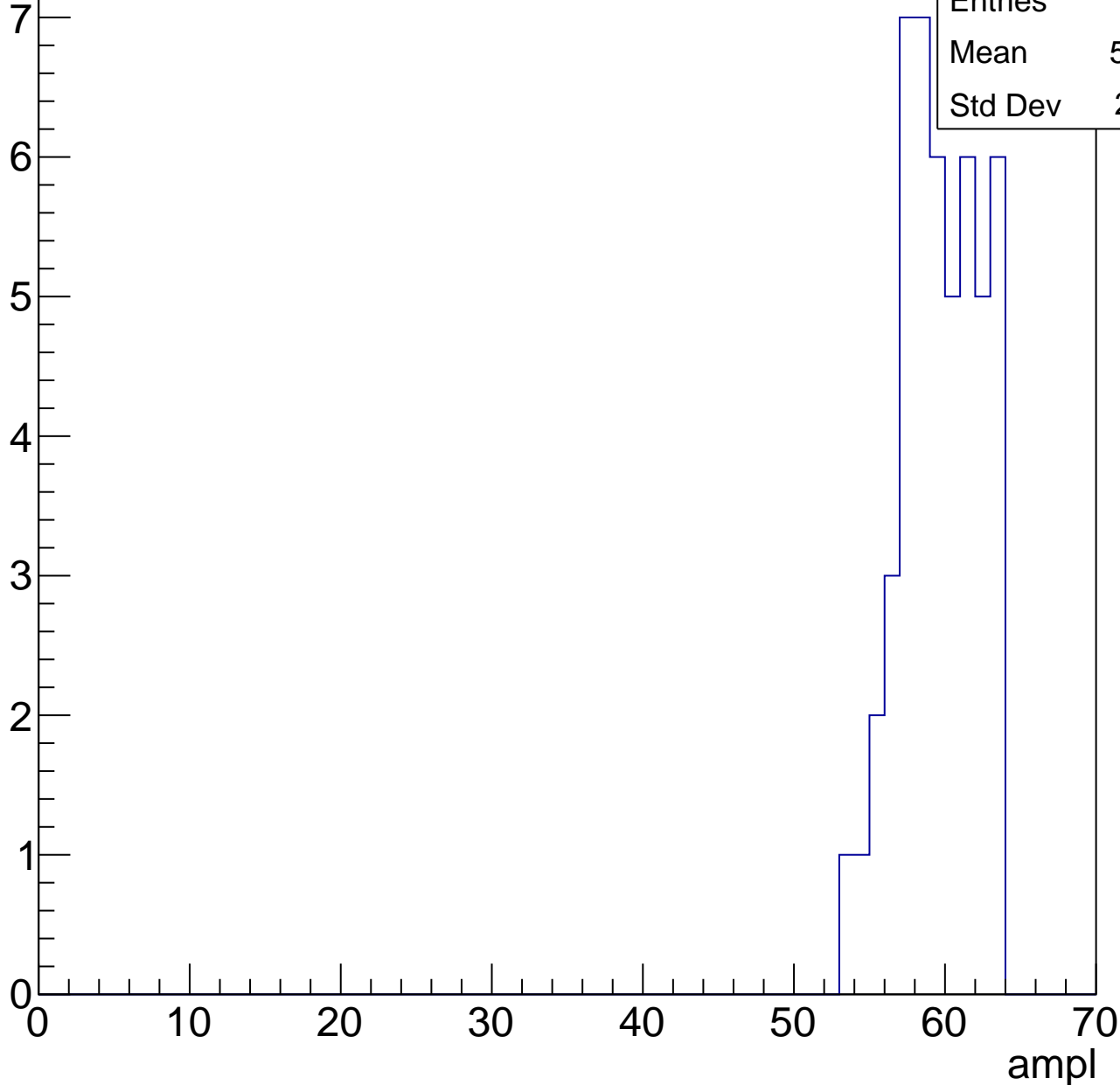
Entries	67
Mean	53.55
Std Dev	3.884



# B1L103S, U1-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

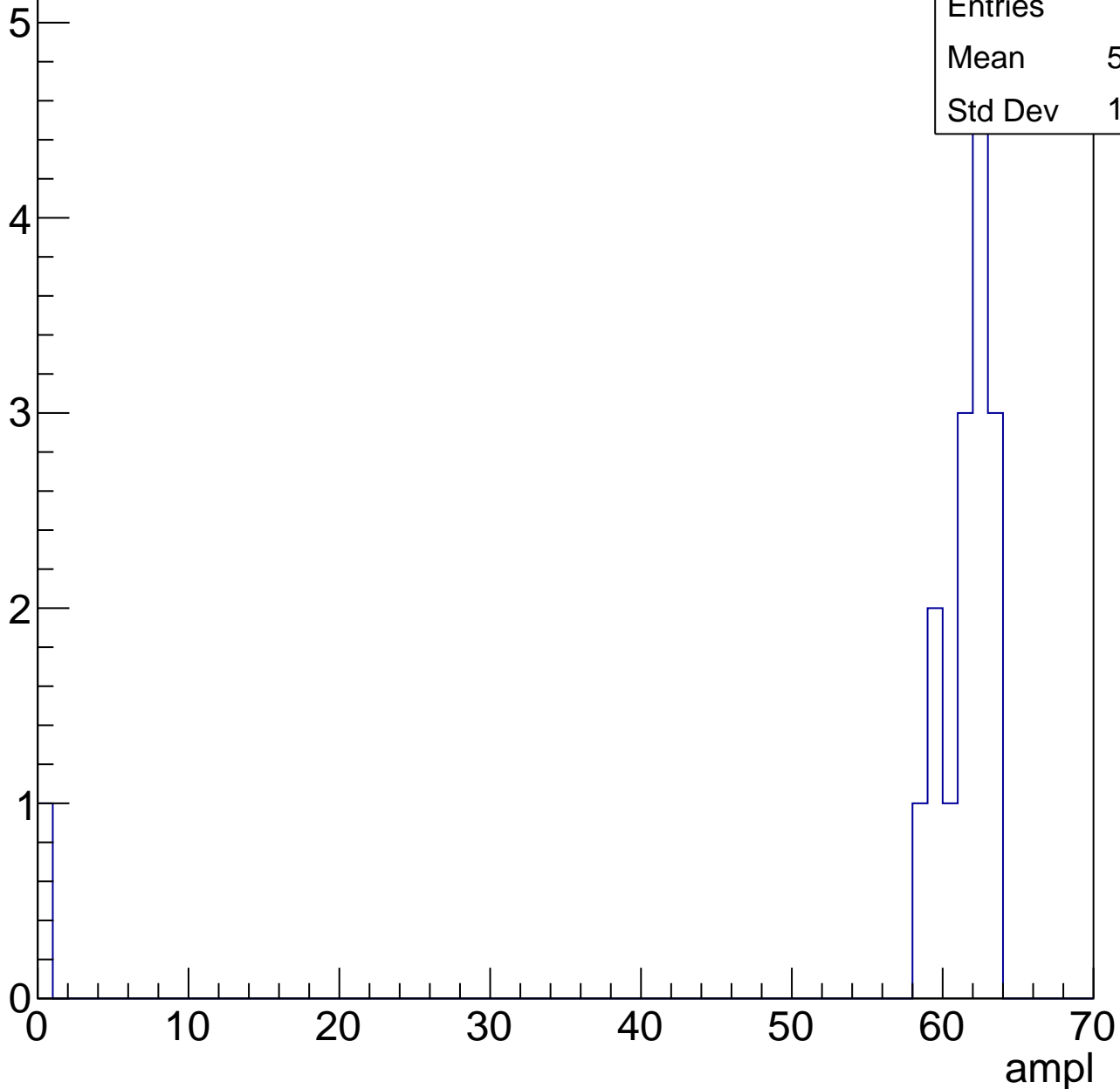


# B1L103S, U1-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	16
Mean	57.38
Std Dev	14.89





# B1L103S, U1-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U1-ch50, adc0

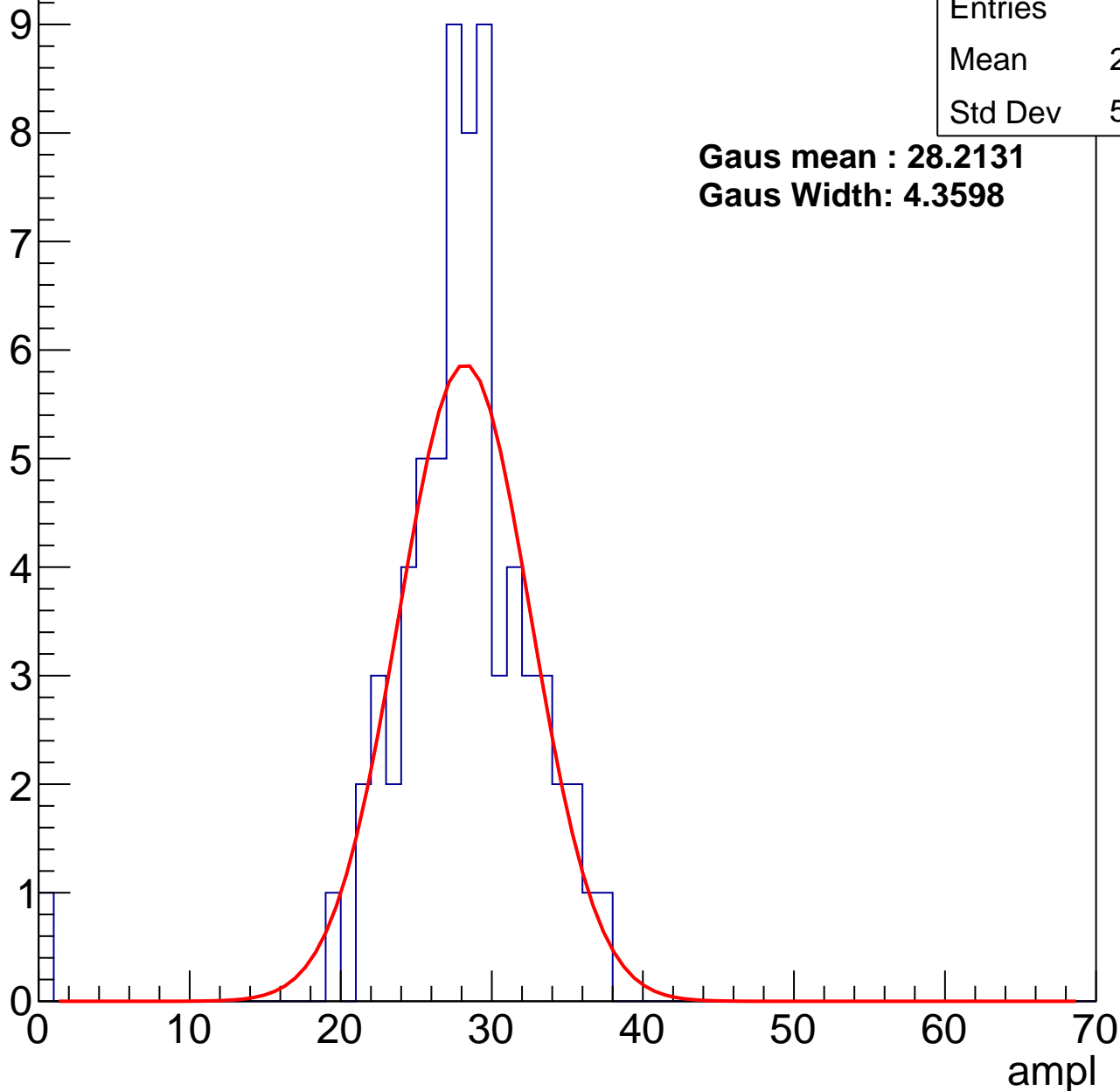
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	27.53
Std Dev	5.057

**Gaus mean : 28.2131**

**Gaus Width: 4.3598**



# B1L103S, U1-ch50, adc1

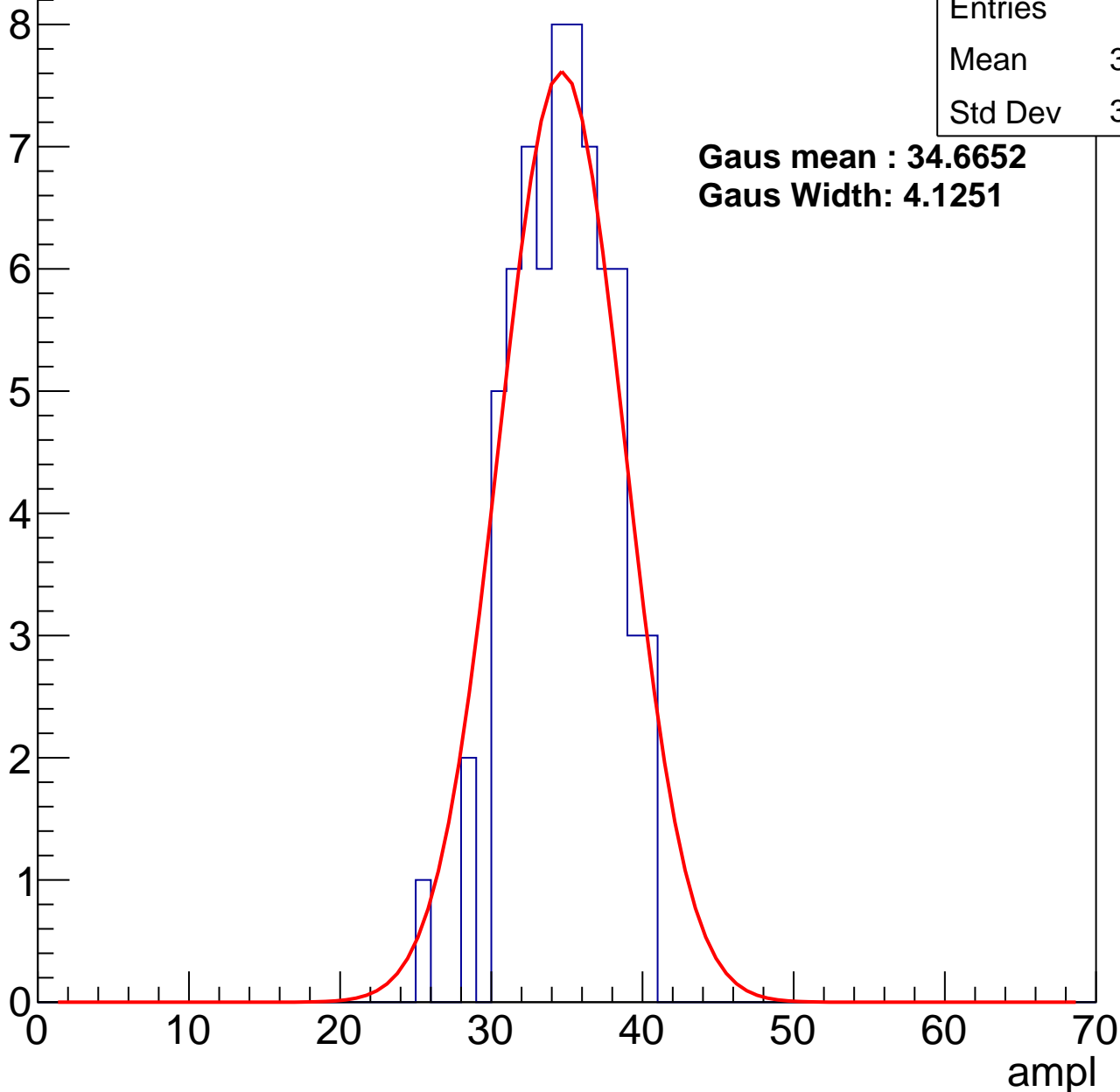
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	34.26
Std Dev	3.174

**Gaus mean : 34.6652**

**Gaus Width: 4.1251**



# B1L103S, U1-ch50, adc2

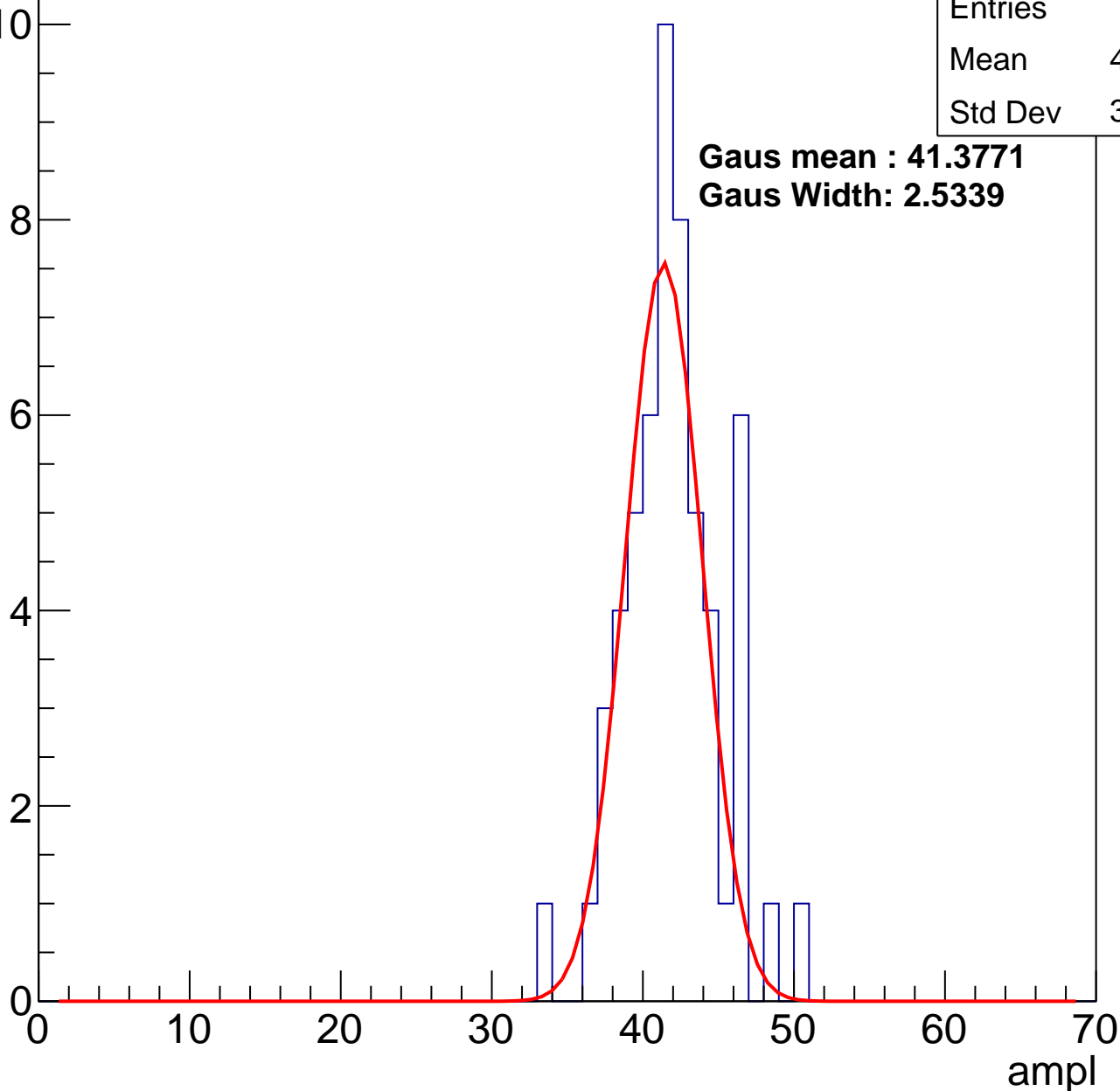
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	41.48
Std Dev	3.122

**Gaus mean : 41.3771**

**Gaus Width: 2.5339**

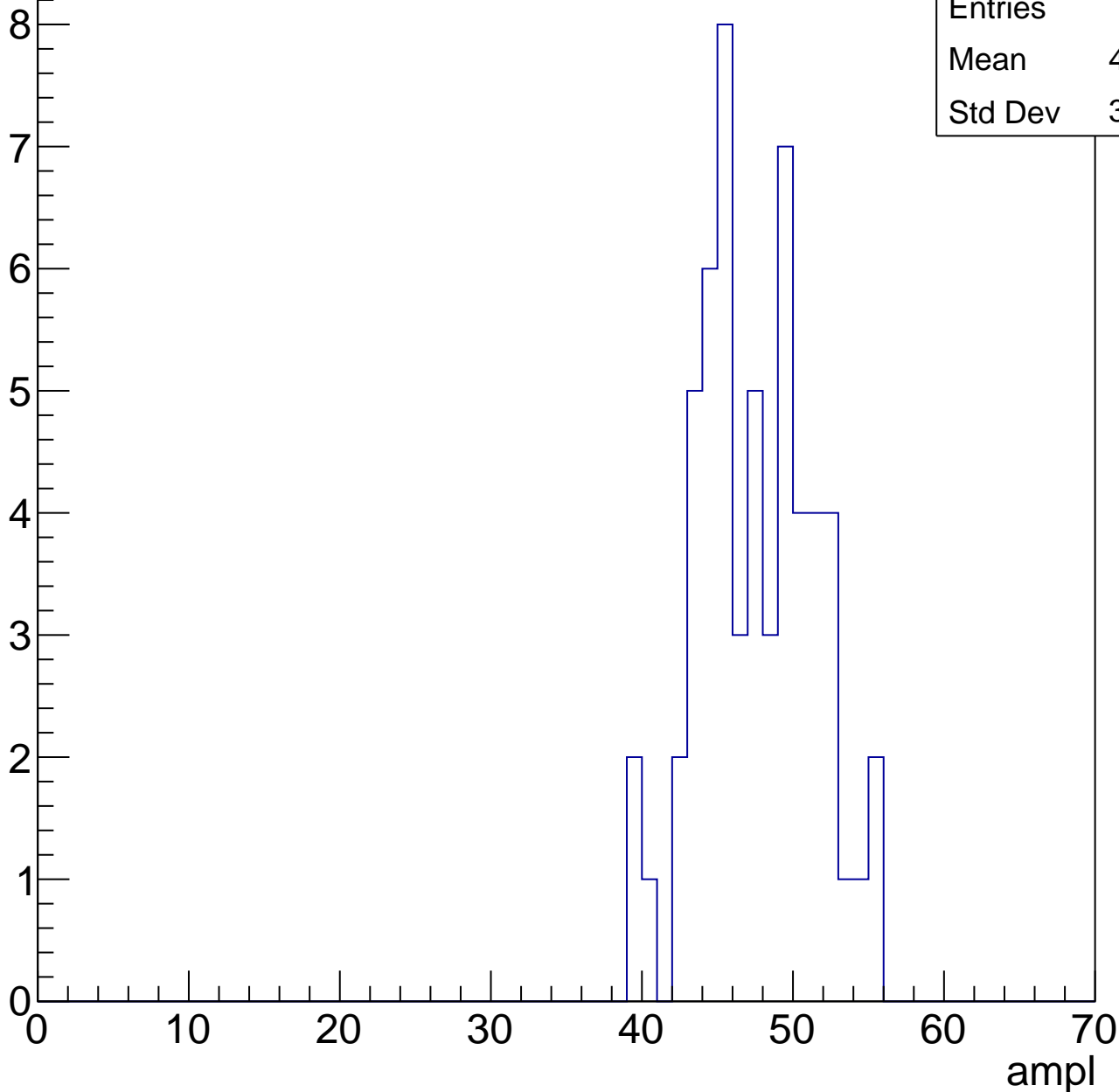


# B1L103S, U1-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	47.07
Std Dev	3.805

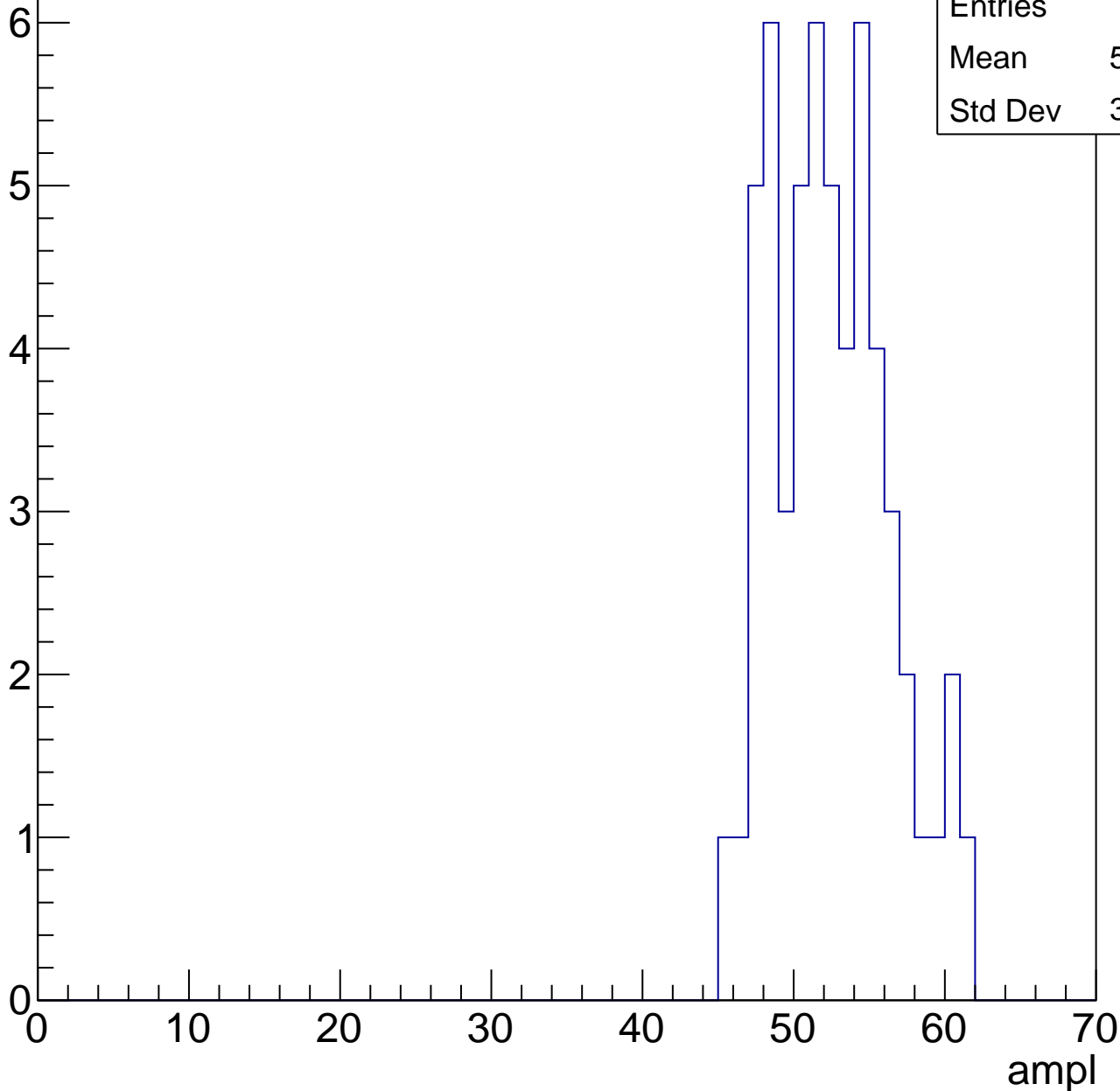


# B1L103S, U1-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

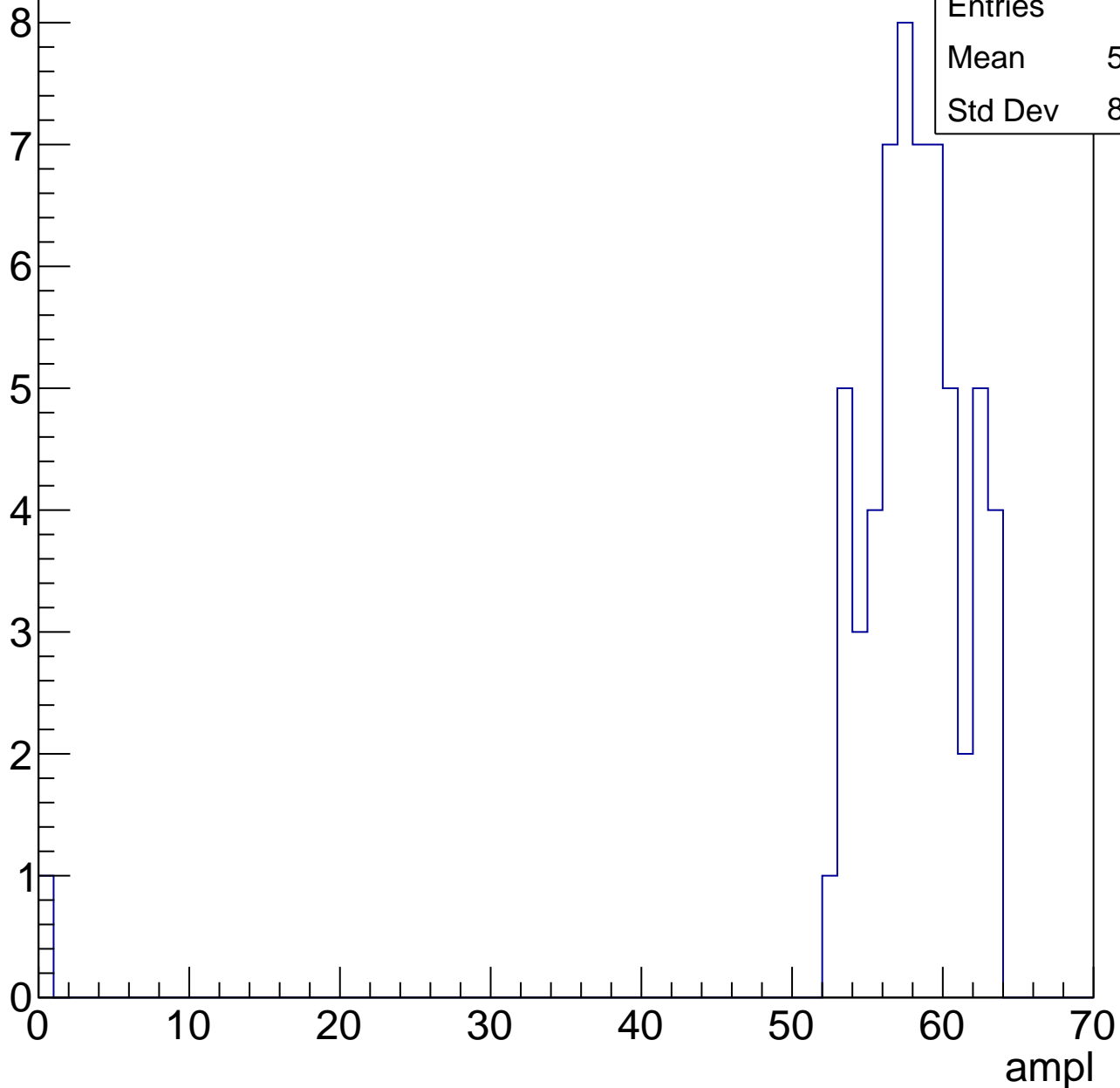
Entries	56
Mean	52.02
Std Dev	3.815



# B1L103S, U1-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

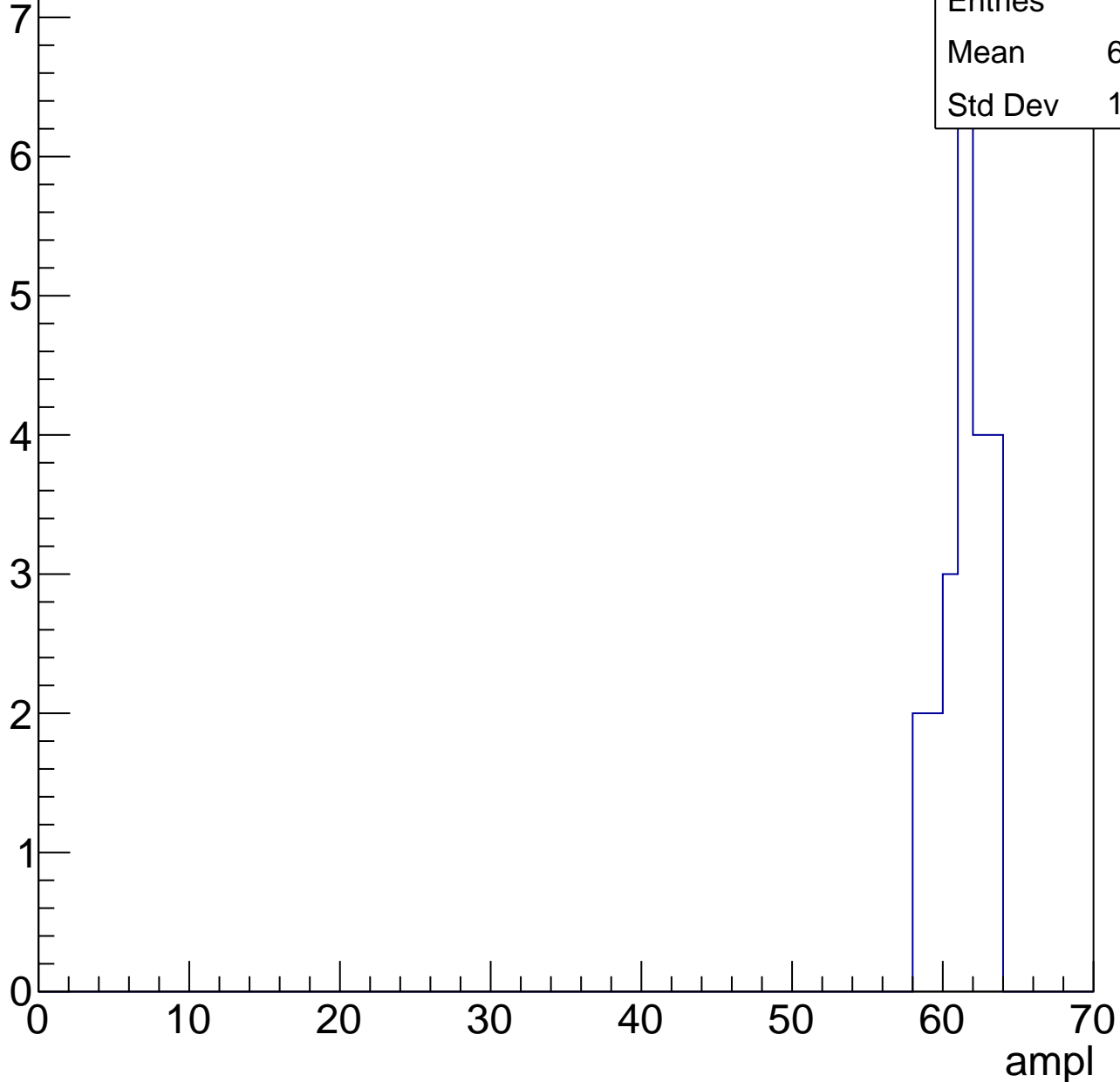


Entries	59
Mean	56.78
Std Dev	8.006

# B1L103S, U1-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

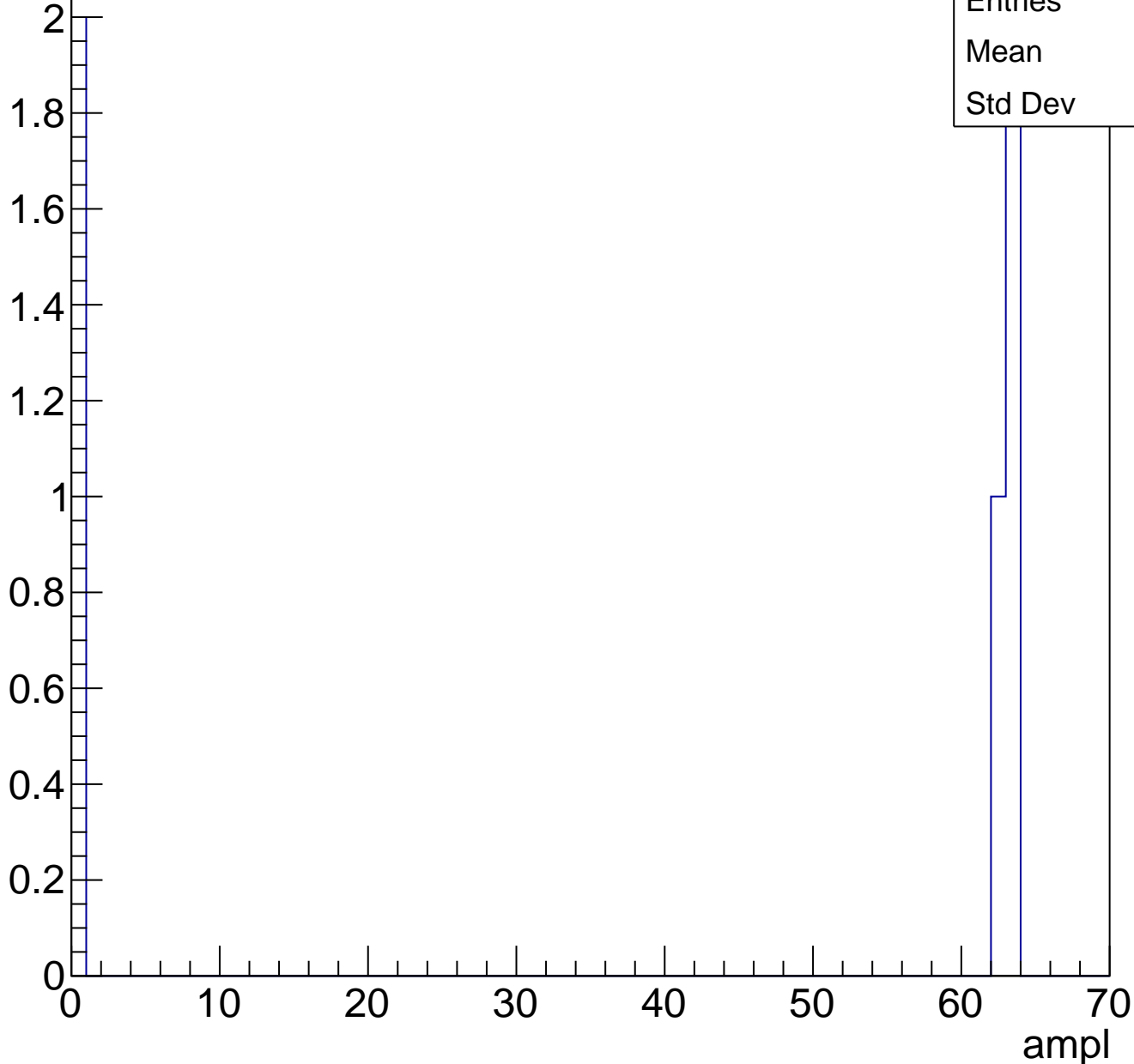




# B1L103S, U1-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch51, adc0

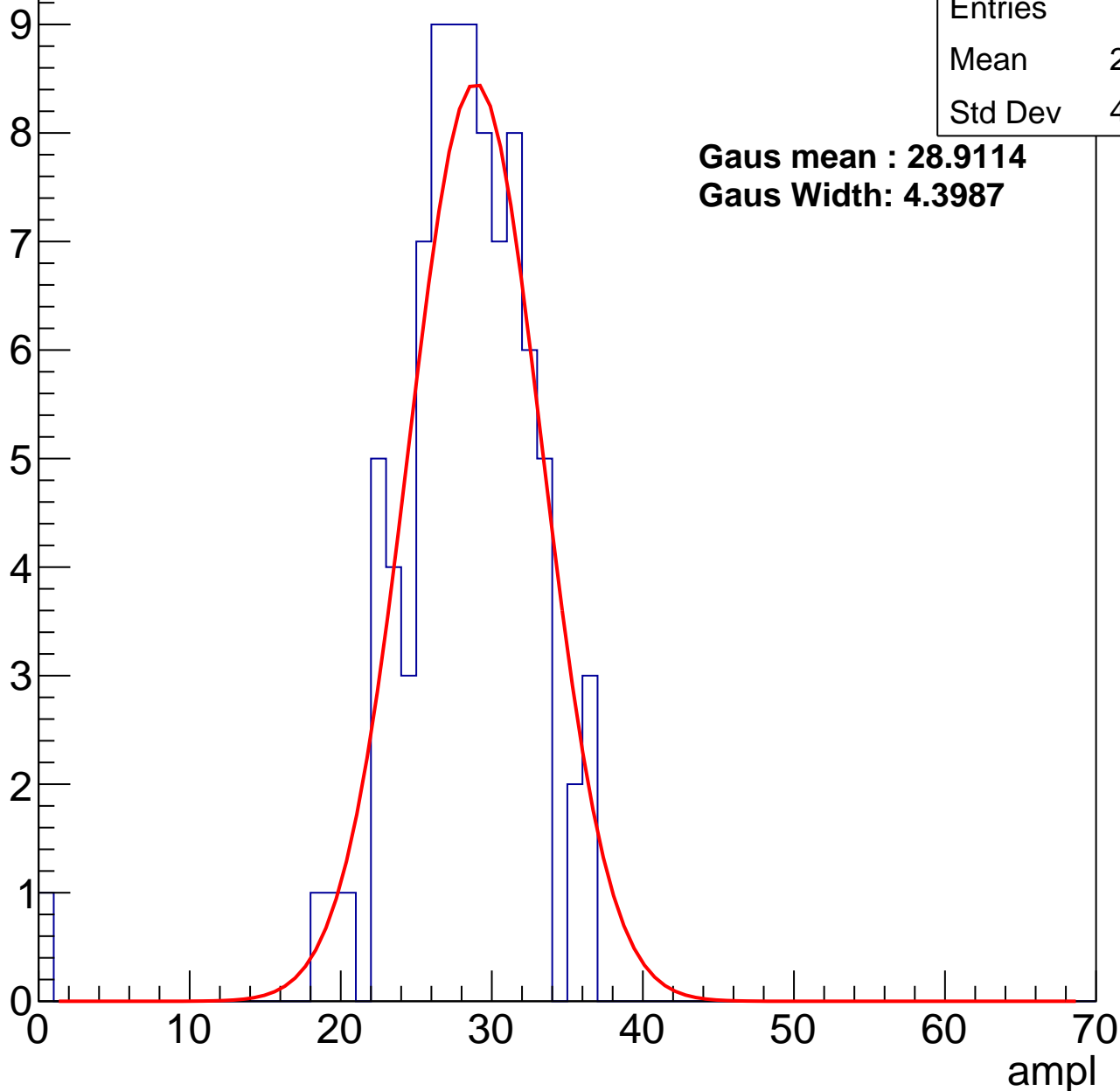
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	89
Mean	27.64
Std Dev	4.826

**Gaus mean : 28.9114**

**Gaus Width: 4.3987**



# B1L103S, U1-ch51, adc1

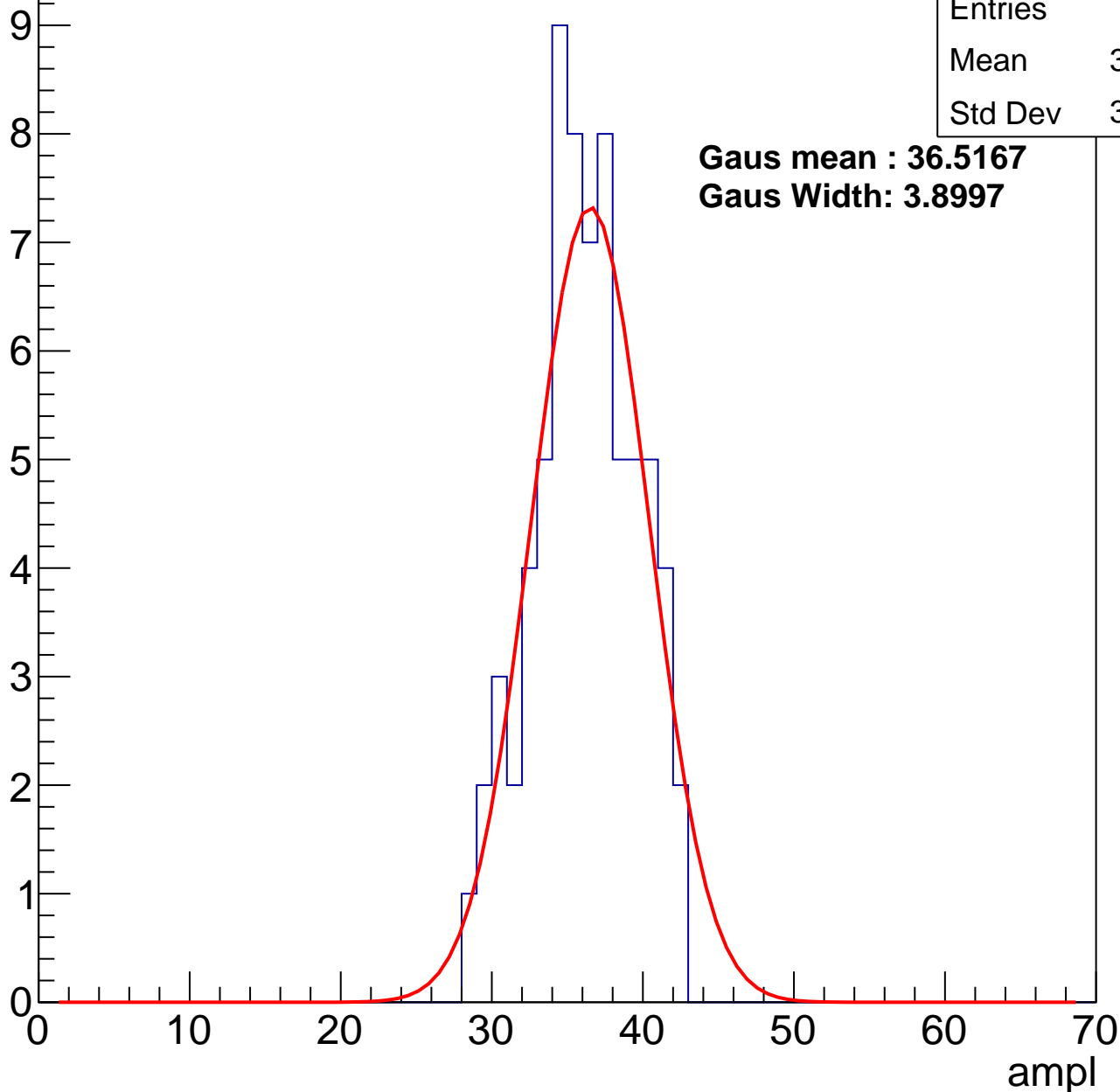
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	35.69
Std Dev	3.362

**Gaus mean : 36.5167**

**Gaus Width: 3.8997**



# B1L103S, U1-ch51, adc2

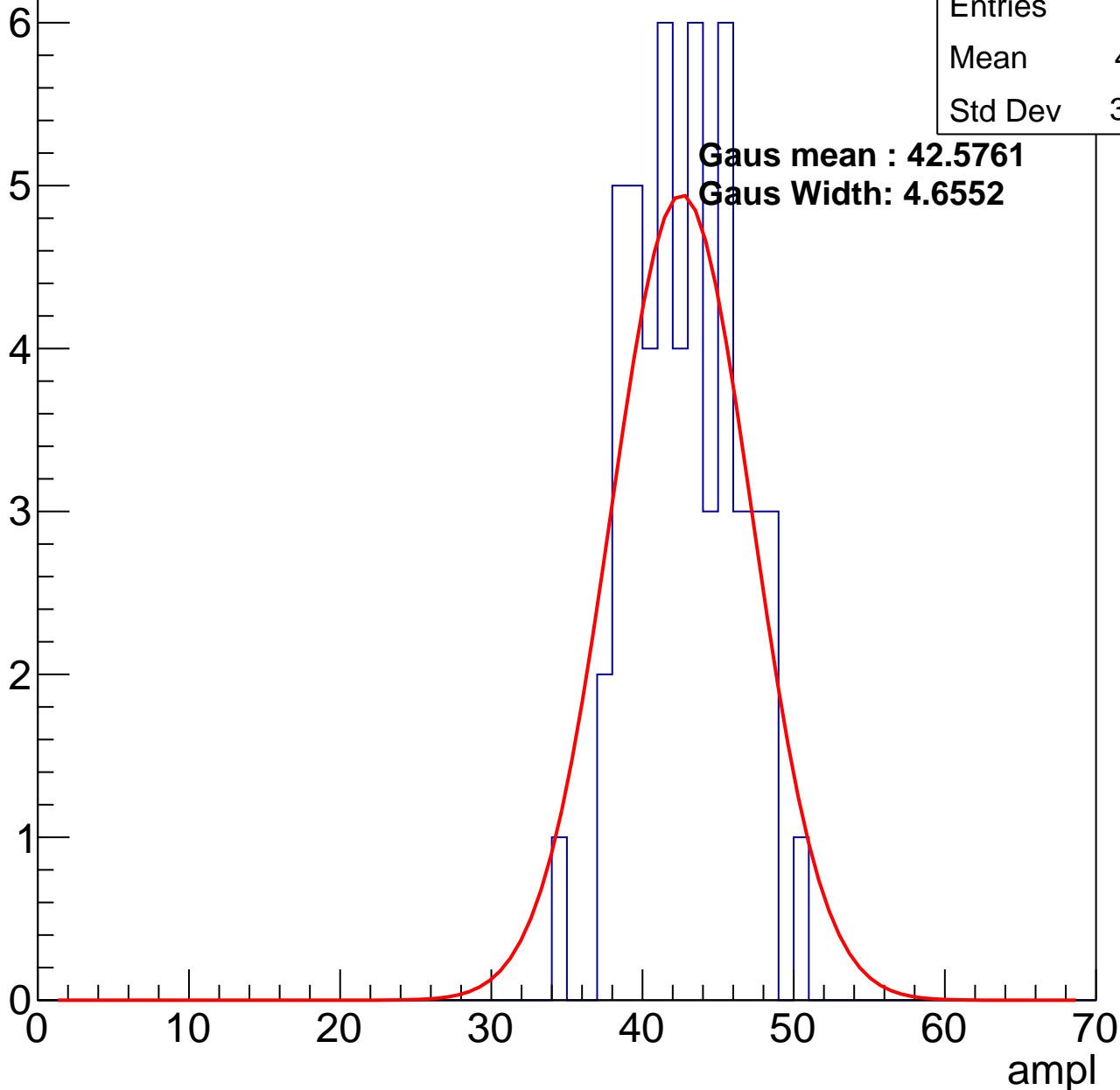
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	42.31
Std Dev	3.462

**Gaus mean : 42.5761**

**Gaus Width: 4.6552**

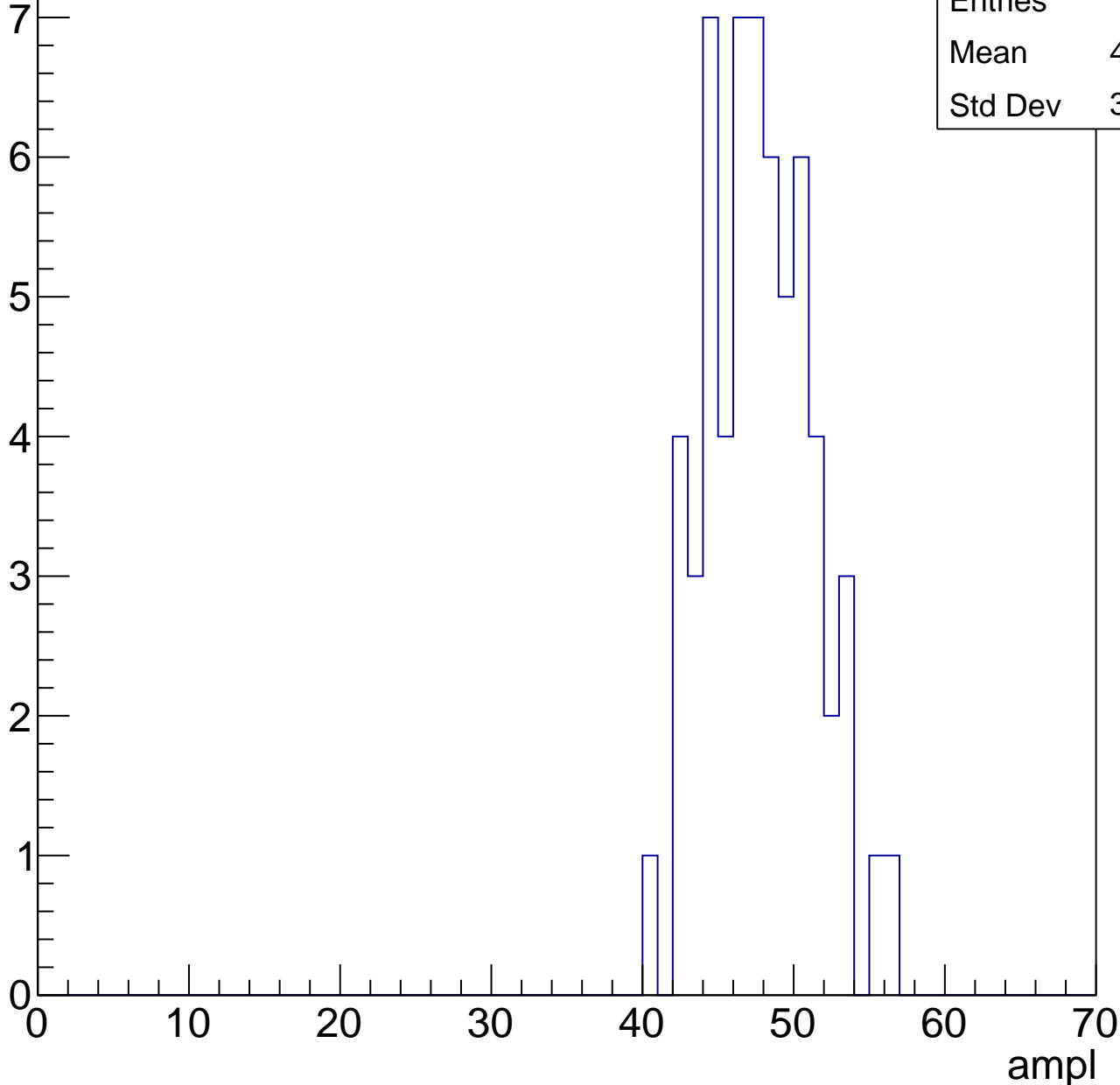


# B1L103S, U1-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

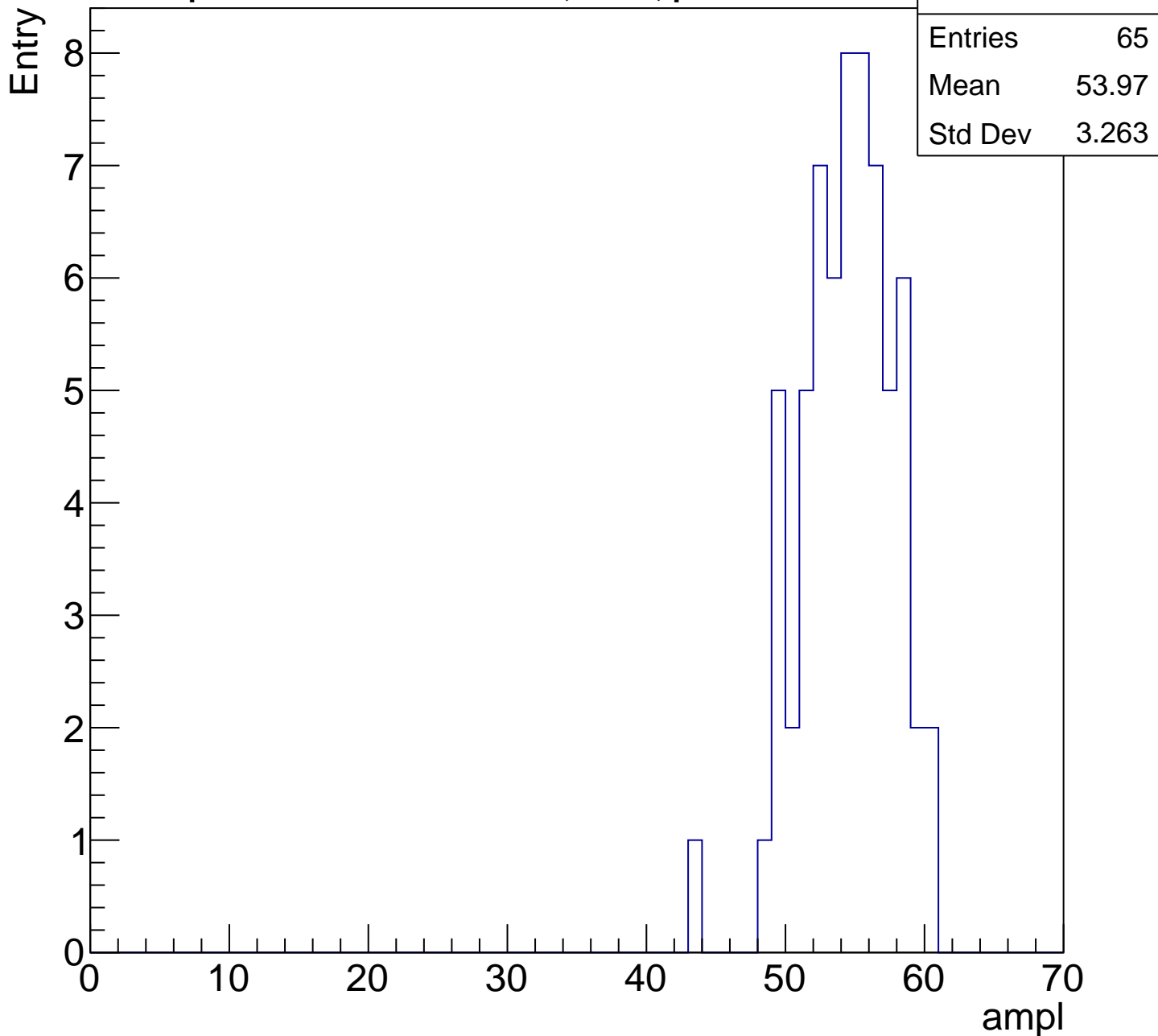
Entry

Entries	61
Mean	47.33
Std Dev	3.444



# B1L103S, U1-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

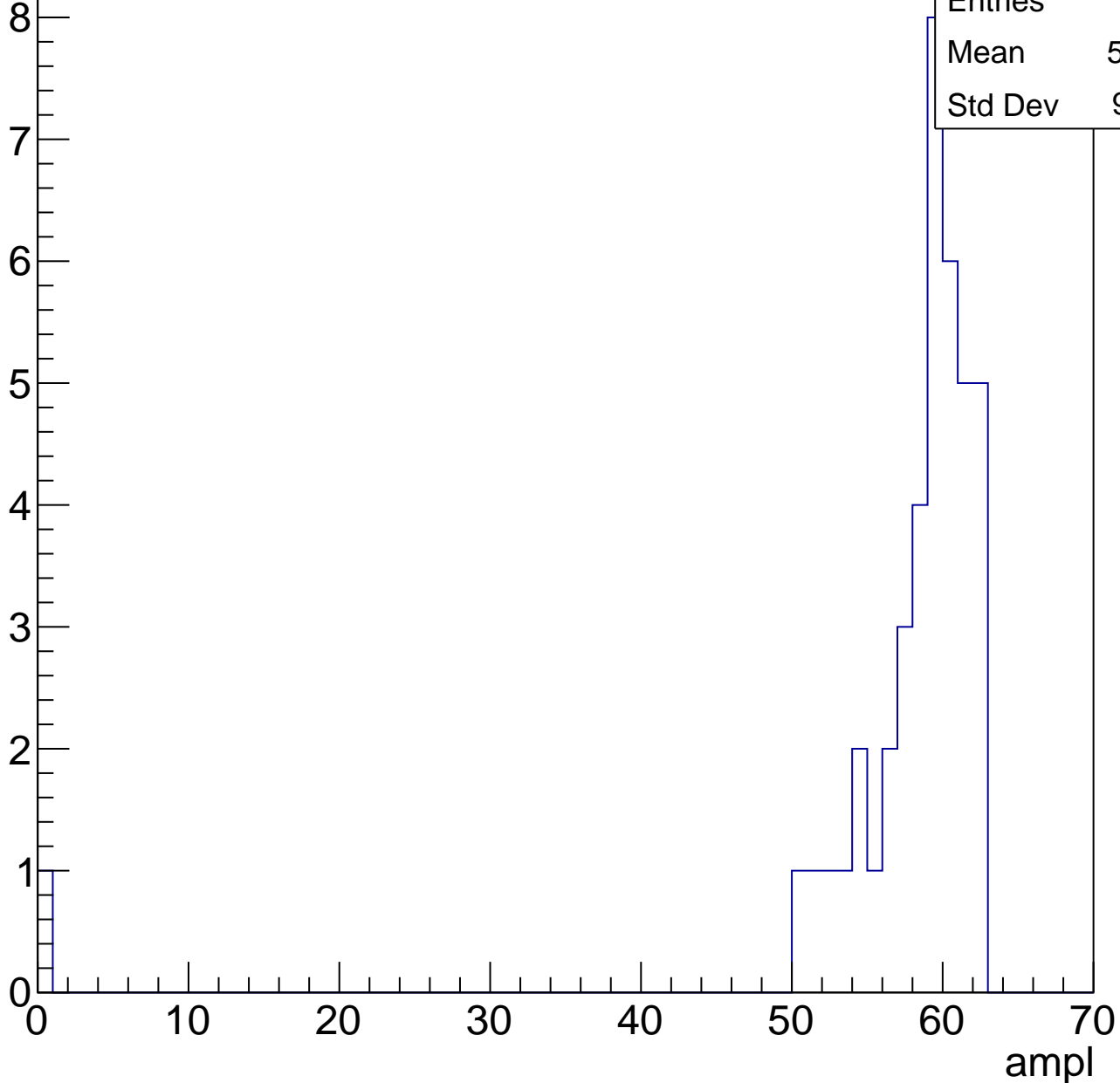


# B1L103S, U1-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	41
Mean	56.85
Std Dev	9.491

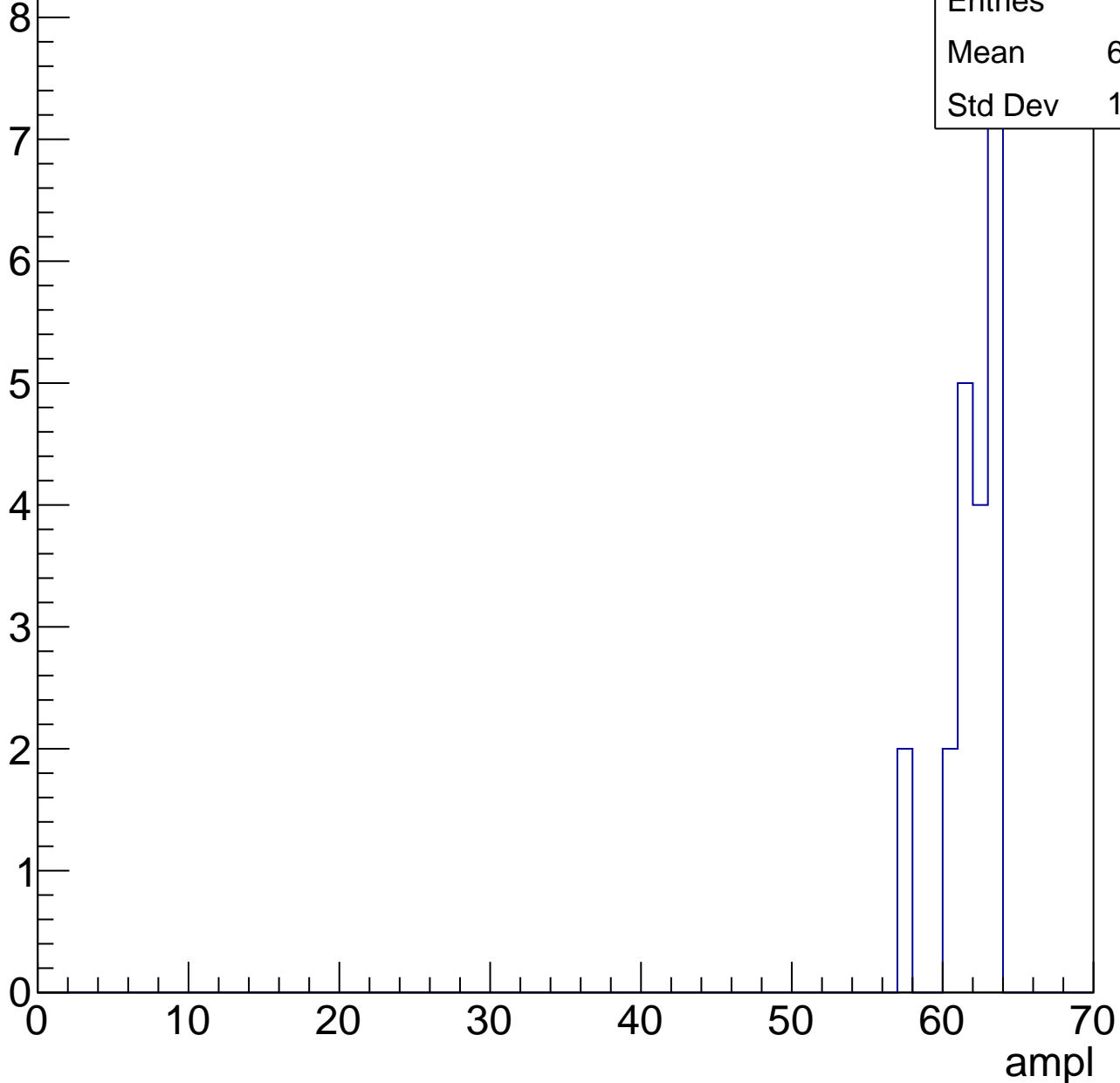


# B1L103S, U1-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	21
Mean	61.48
Std Dev	1.763





# B1L103S, U1-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch52, adc0

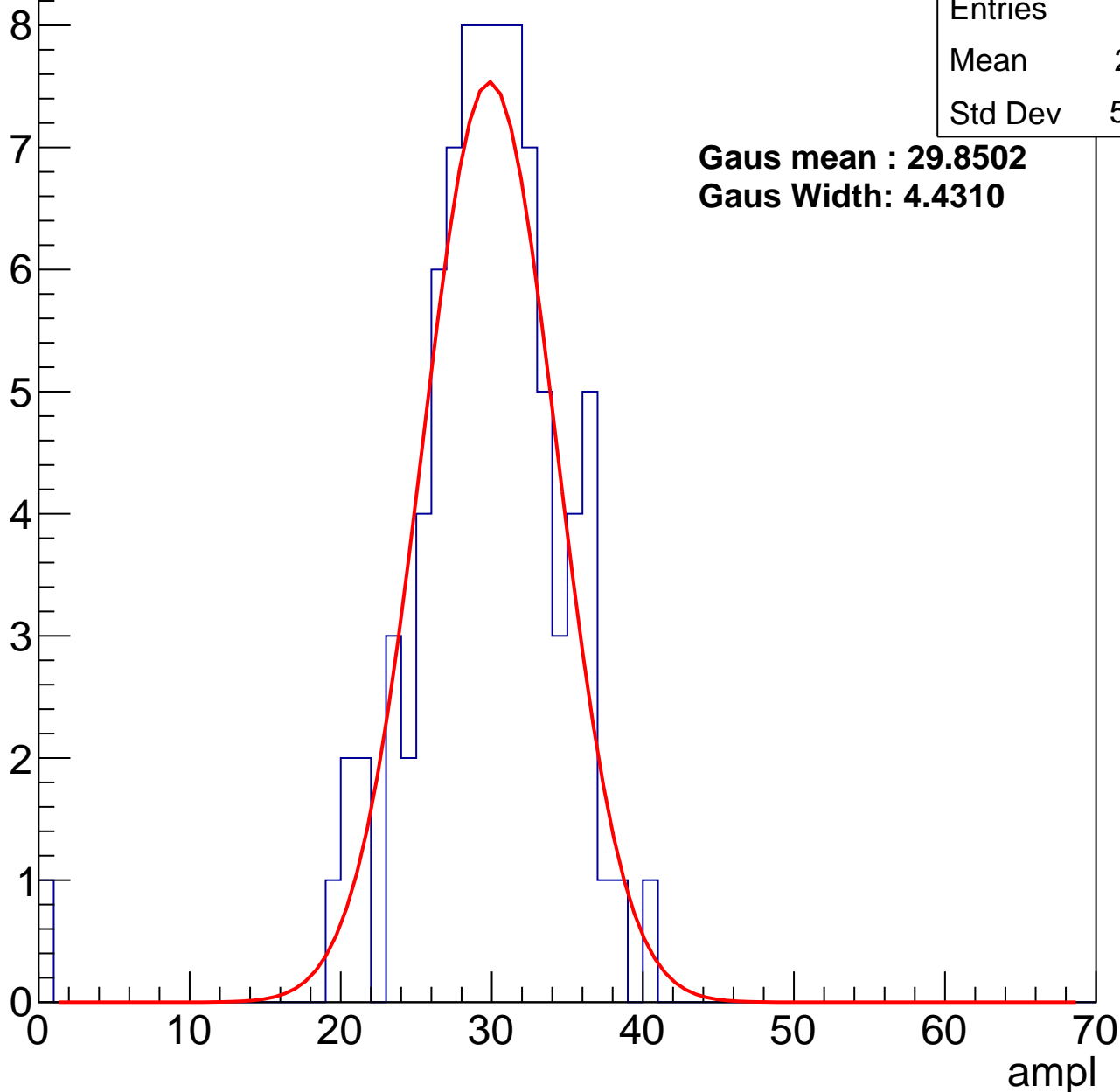
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	87
Mean	29.11
Std Dev	5.312

**Gaus mean : 29.8502**

**Gaus Width: 4.4310**



# B1L103S, U1-ch52, adc1

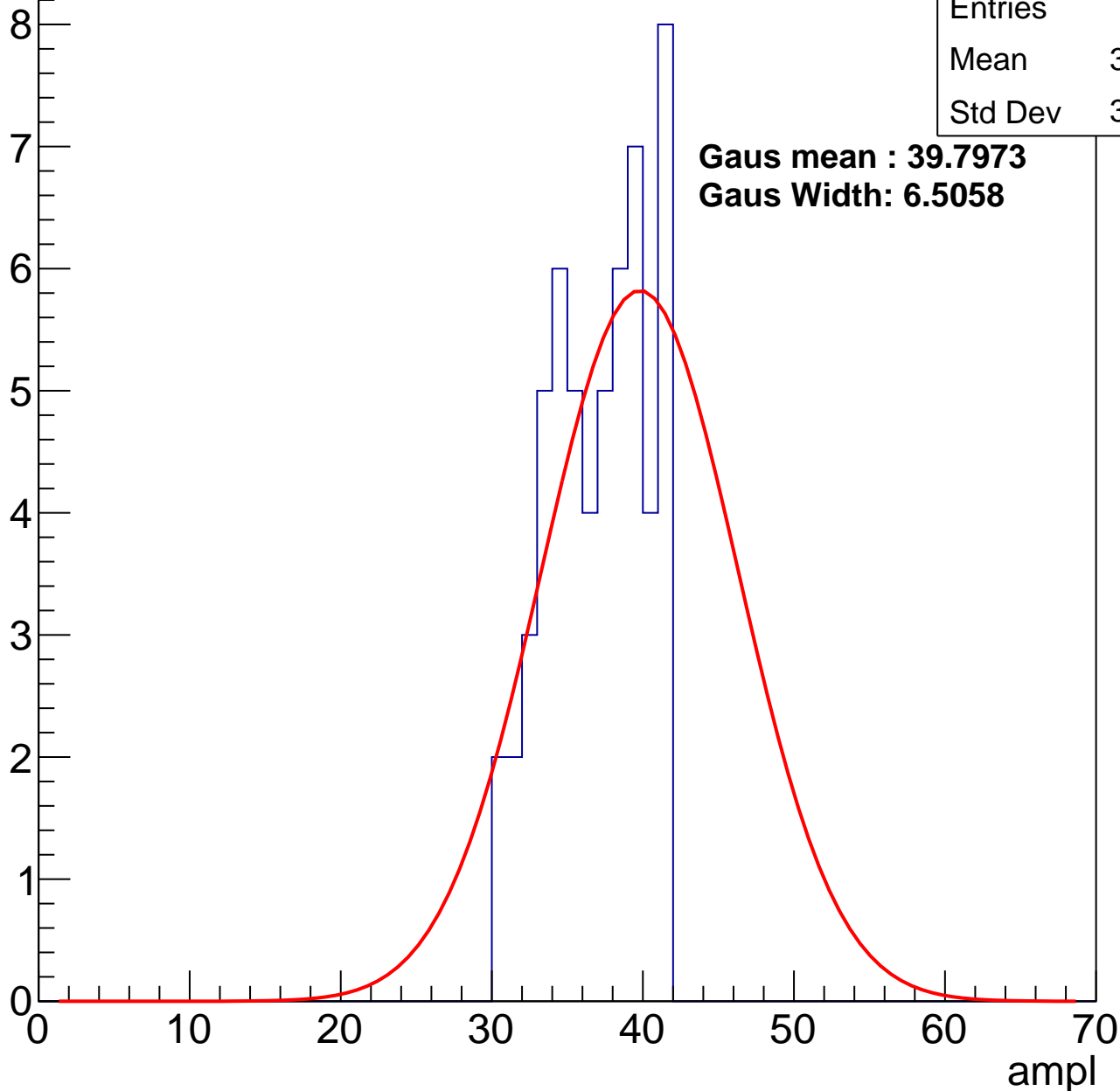
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	36.49
Std Dev	3.207

**Gaus mean : 39.7973**

**Gaus Width: 6.5058**



# B1L103S, U1-ch52, adc2

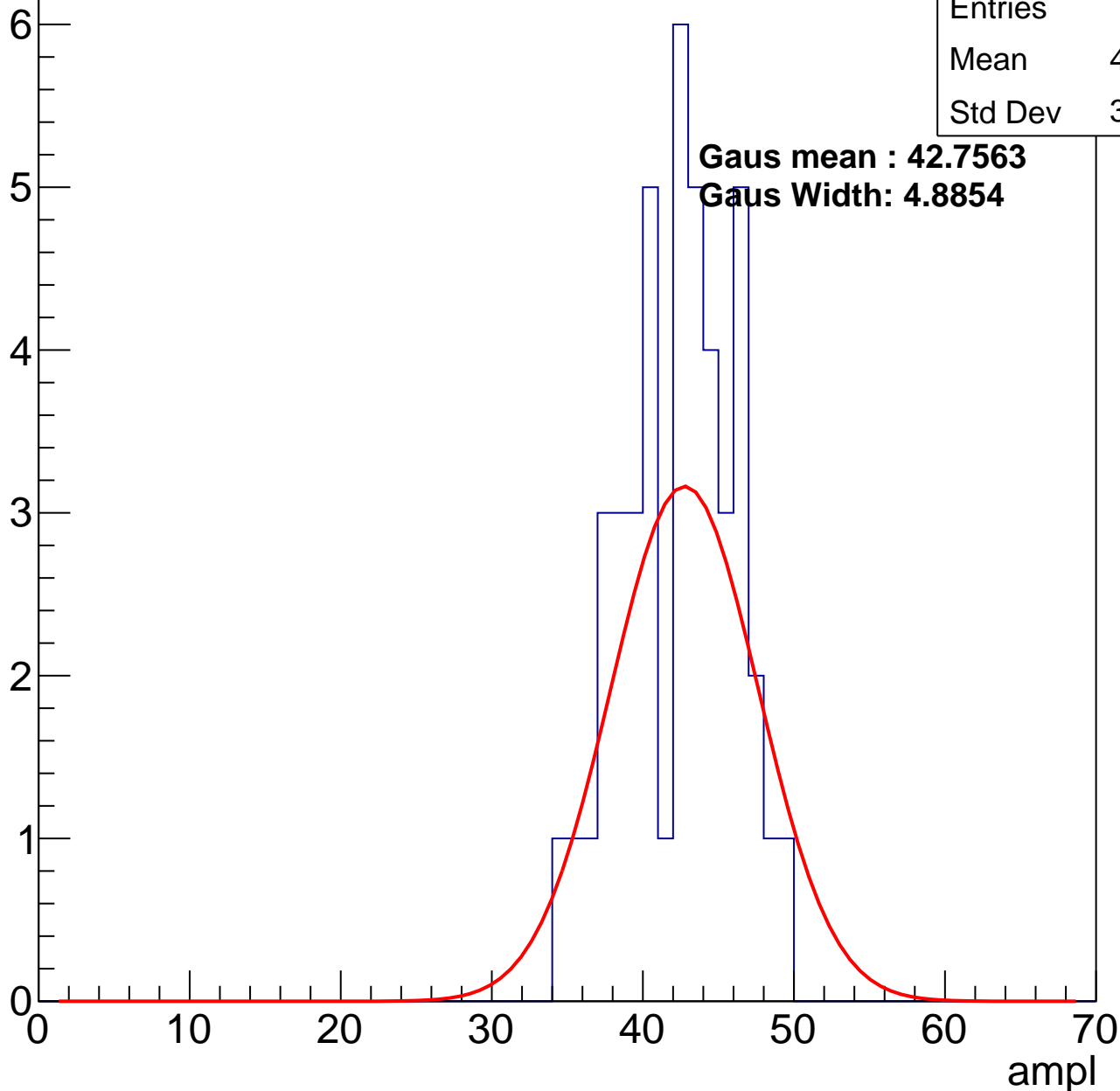
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	41.93
Std Dev	3.599

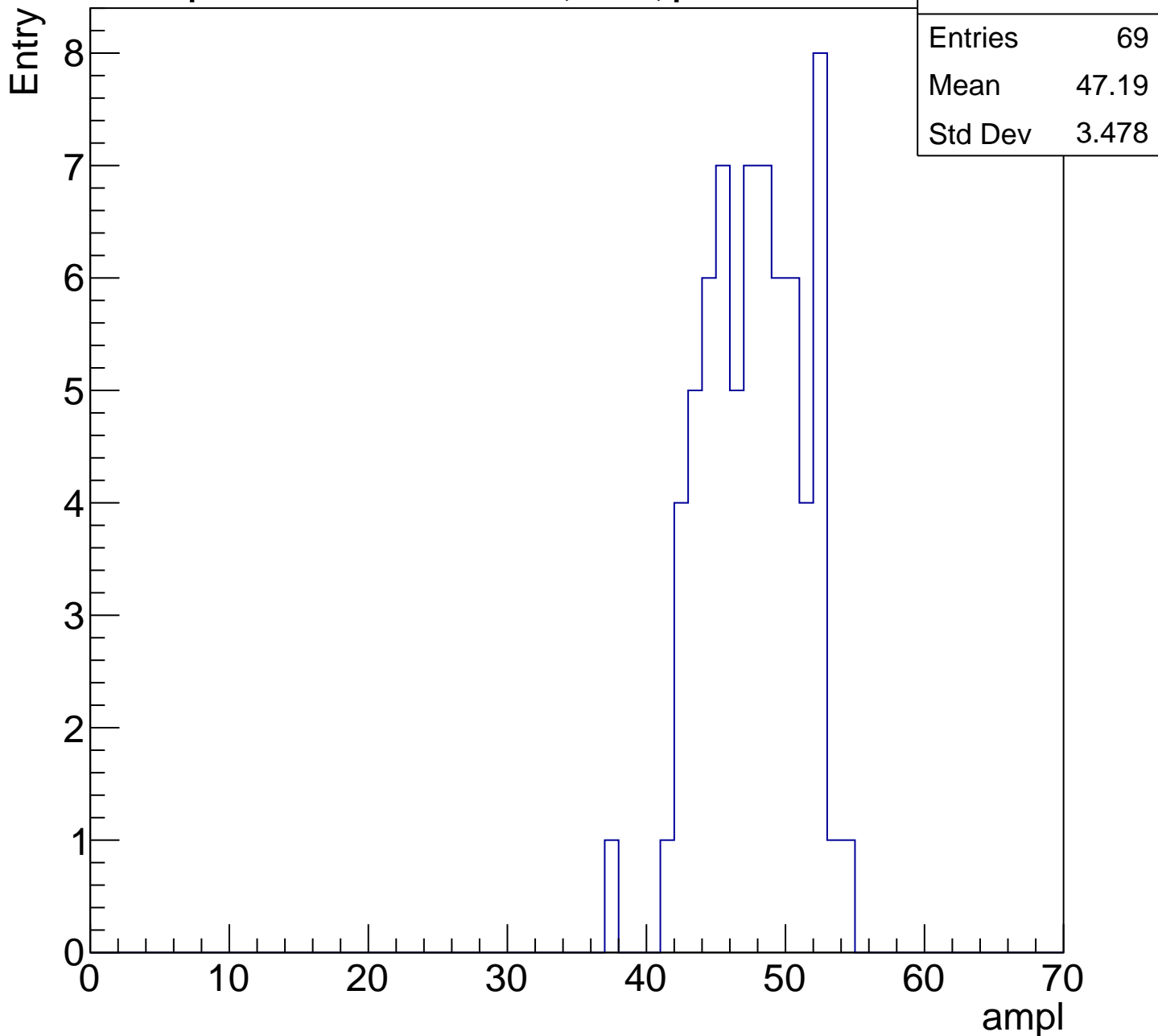
**Gaus mean : 42.7563**

**Gaus Width: 4.8854**



# B1L103S, U1-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

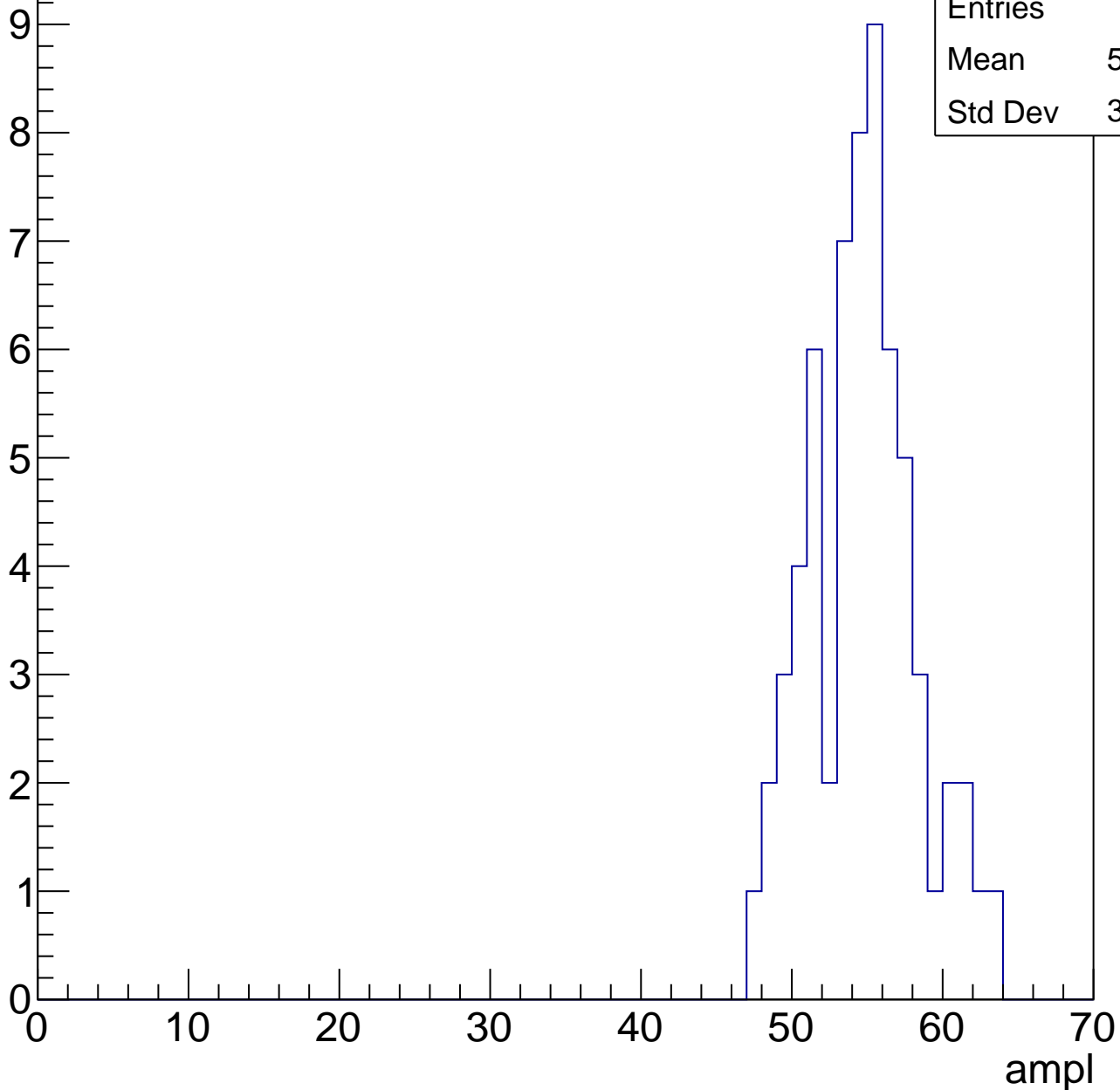


# B1L103S, U1-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	54.27
Std Dev	3.542

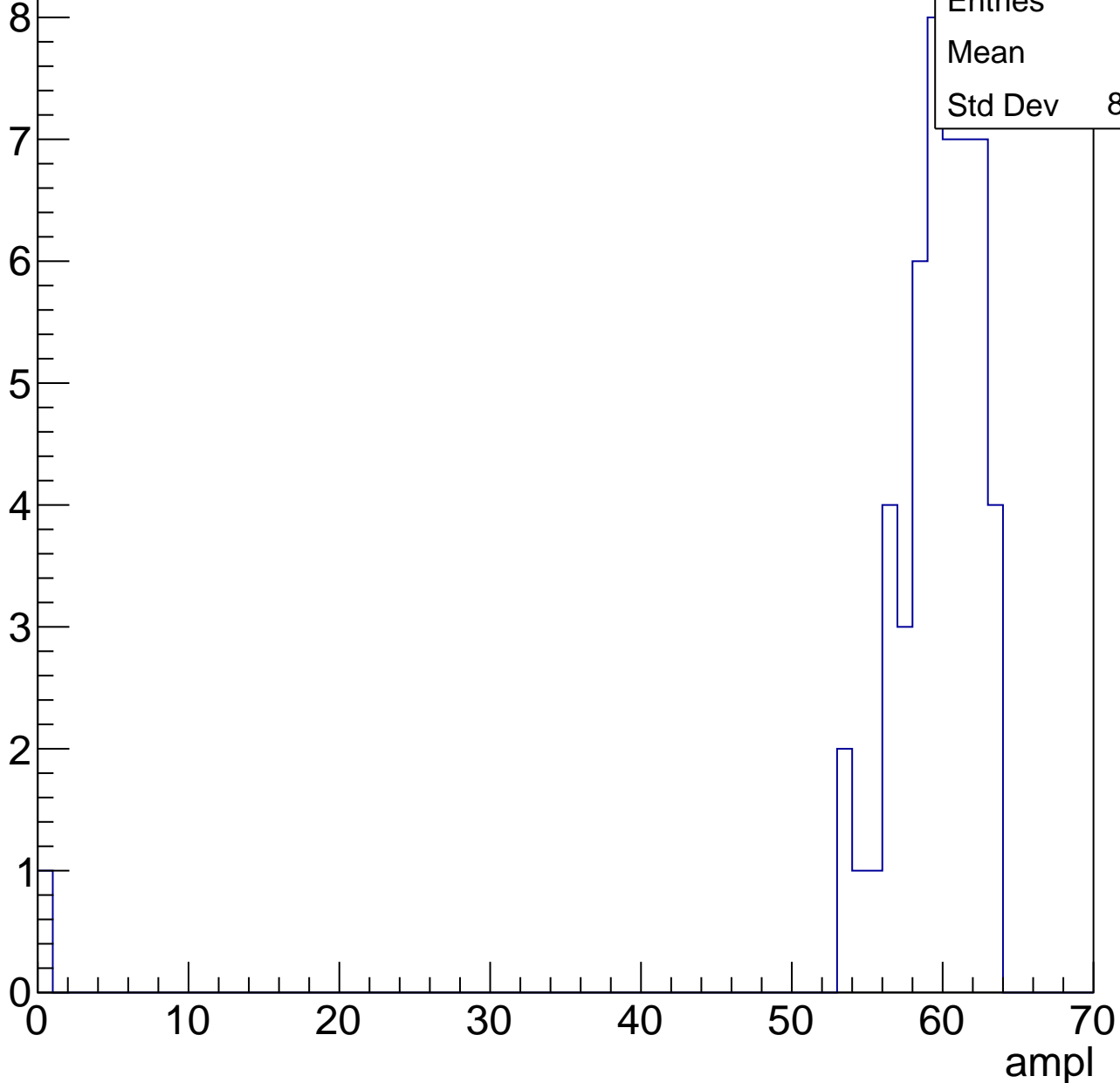


# B1L103S, U1-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	58.1
Std Dev	8.596



# B1L103S, U1-ch52, adc6

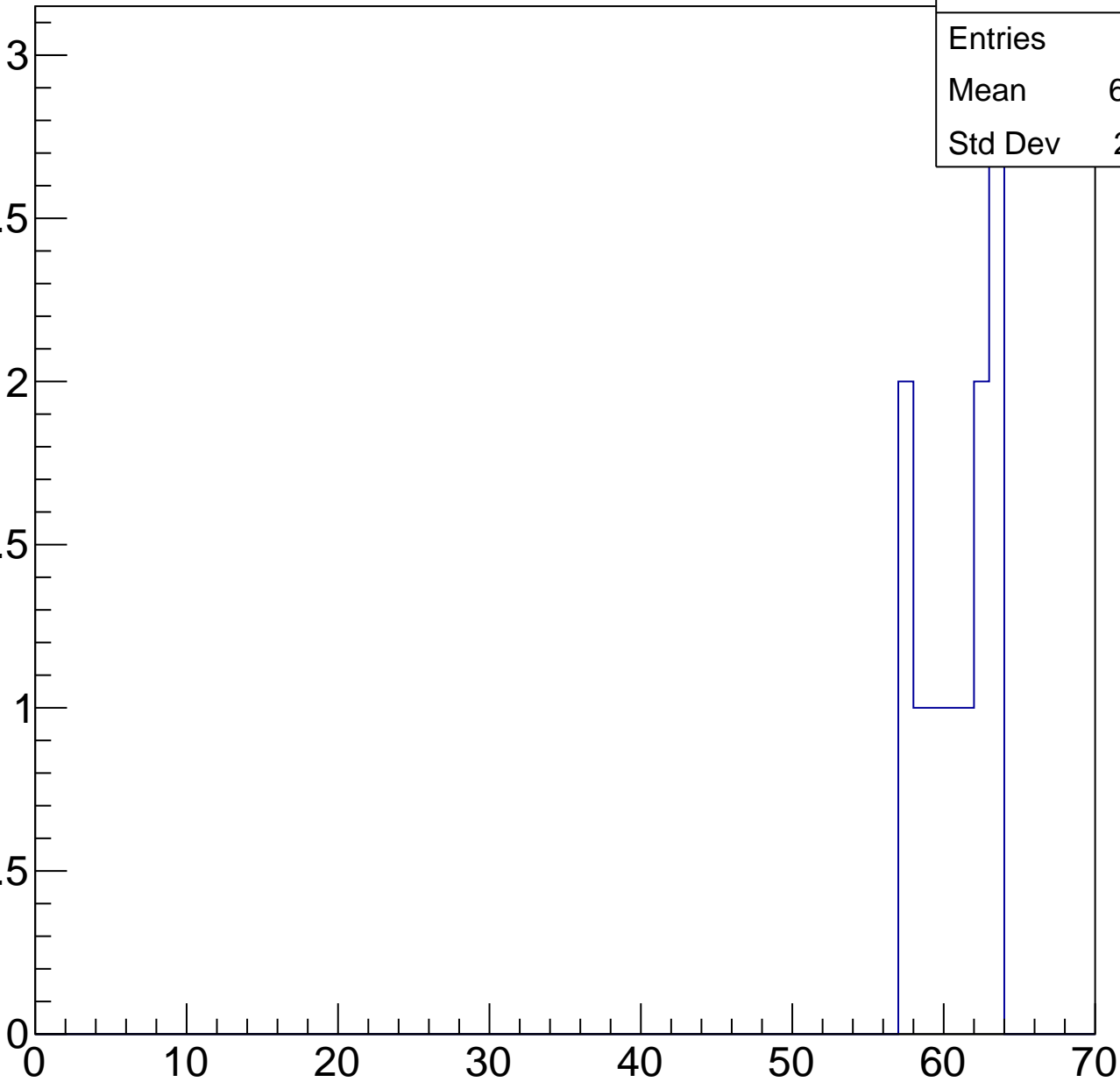
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	11
Mean	60.45
Std Dev	2.271

ampl





# B1L103S, U1-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch53, adc0

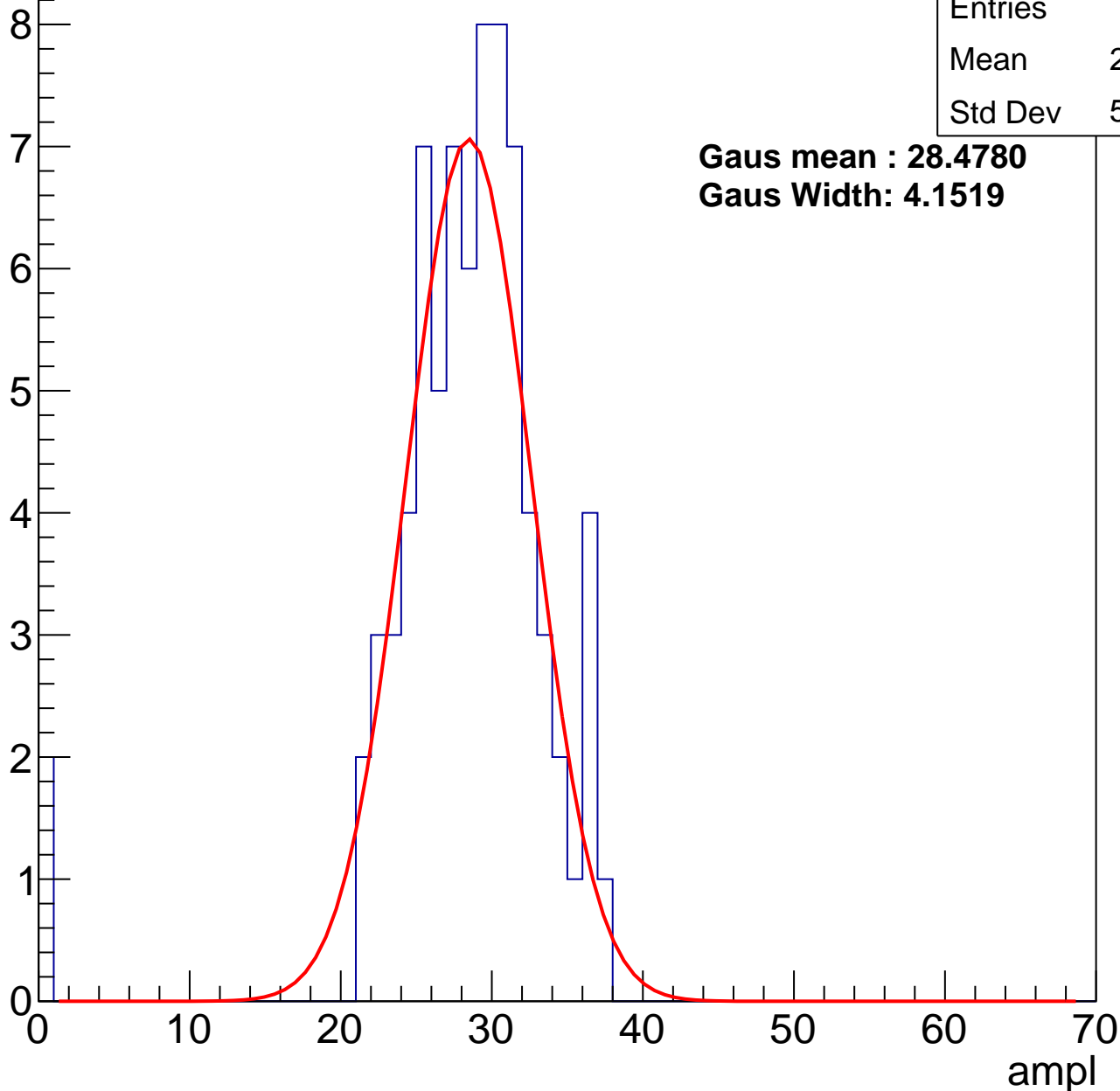
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	27.73
Std Dev	5.919

**Gaus mean : 28.4780**

**Gaus Width: 4.1519**



# B1L103S, U1-ch53, adc1

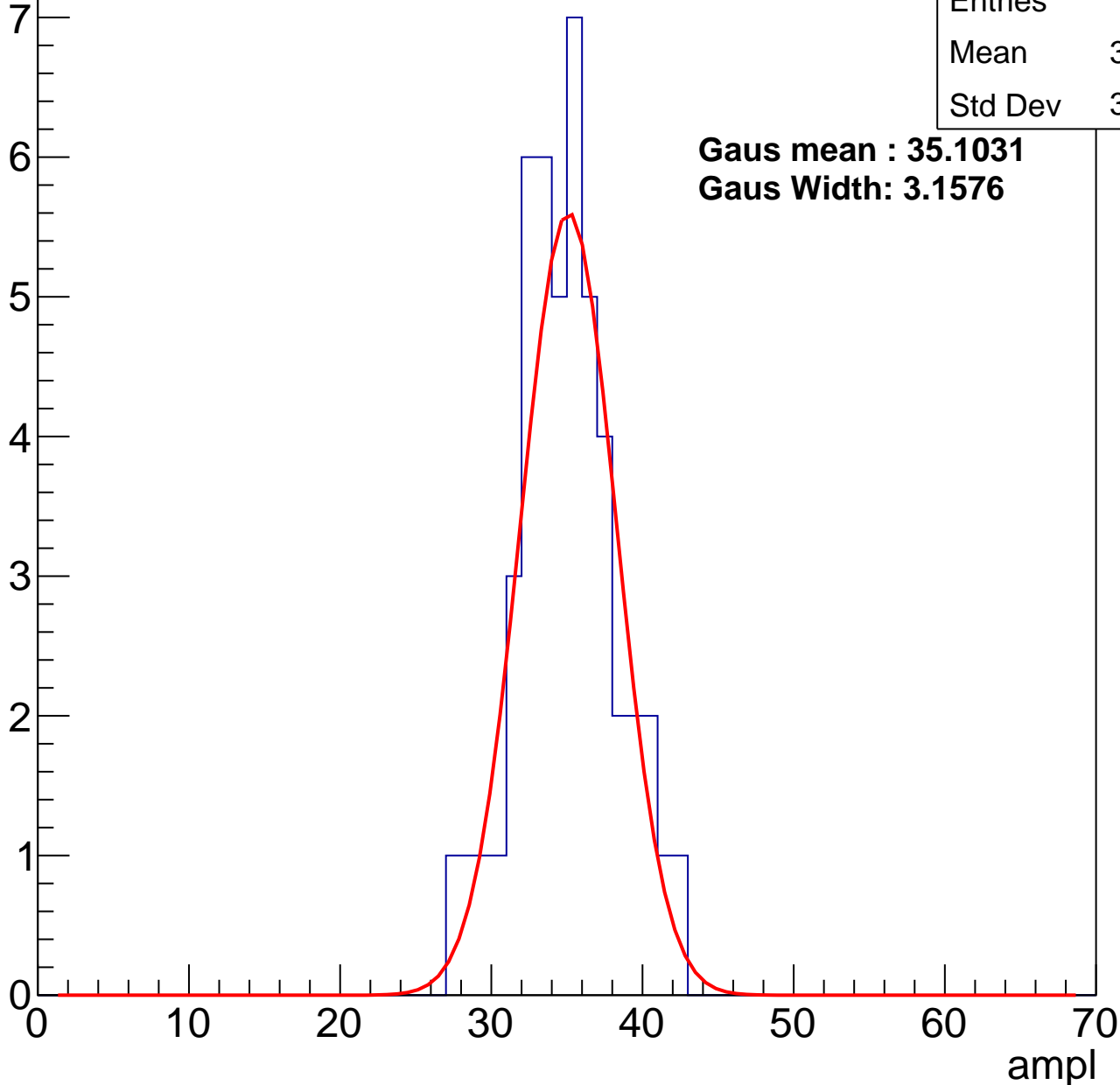
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	34.52
Std Dev	3.227

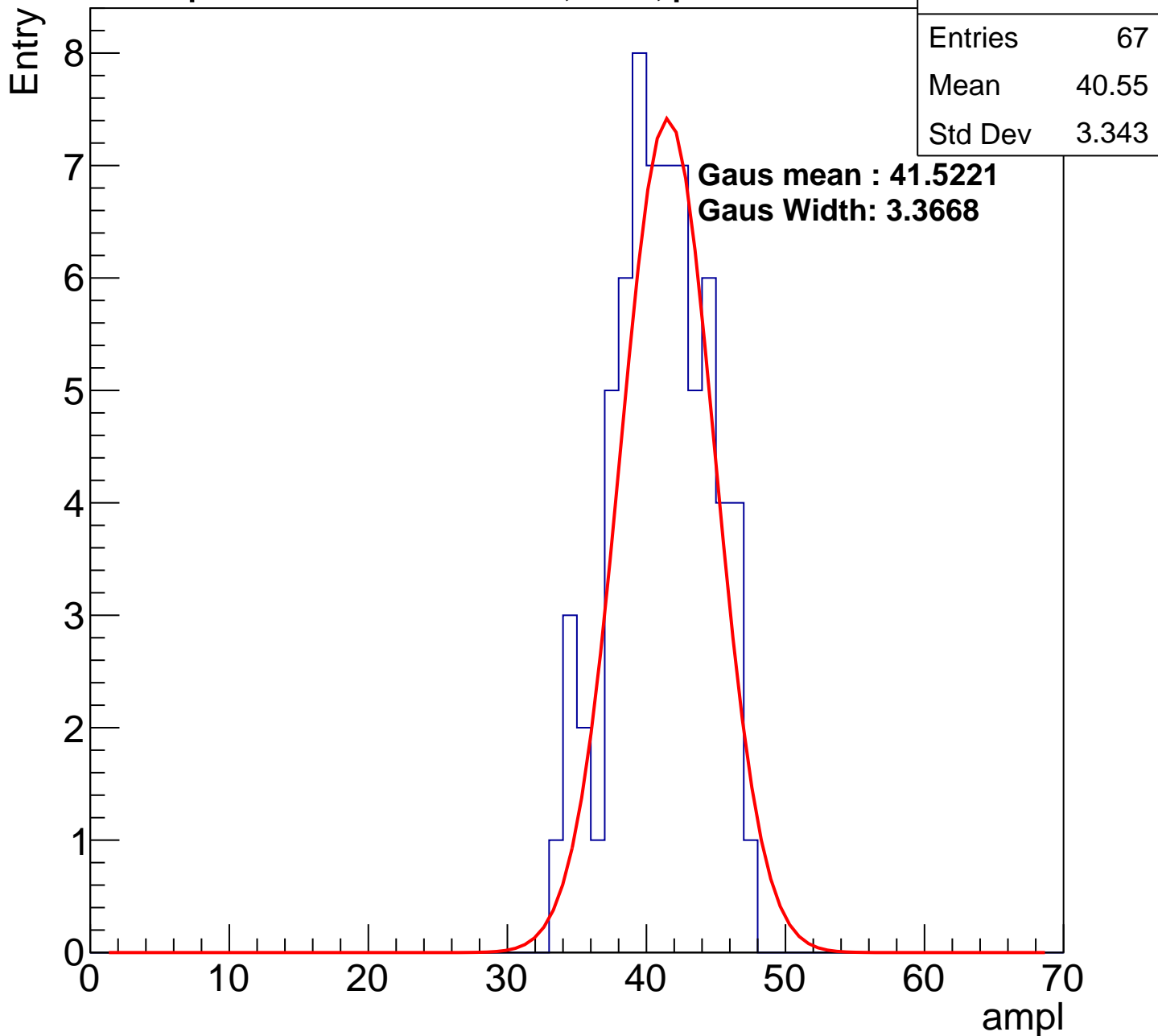
**Gaus mean : 35.1031**

**Gaus Width: 3.1576**



# B1L103S, U1-ch53, adc2

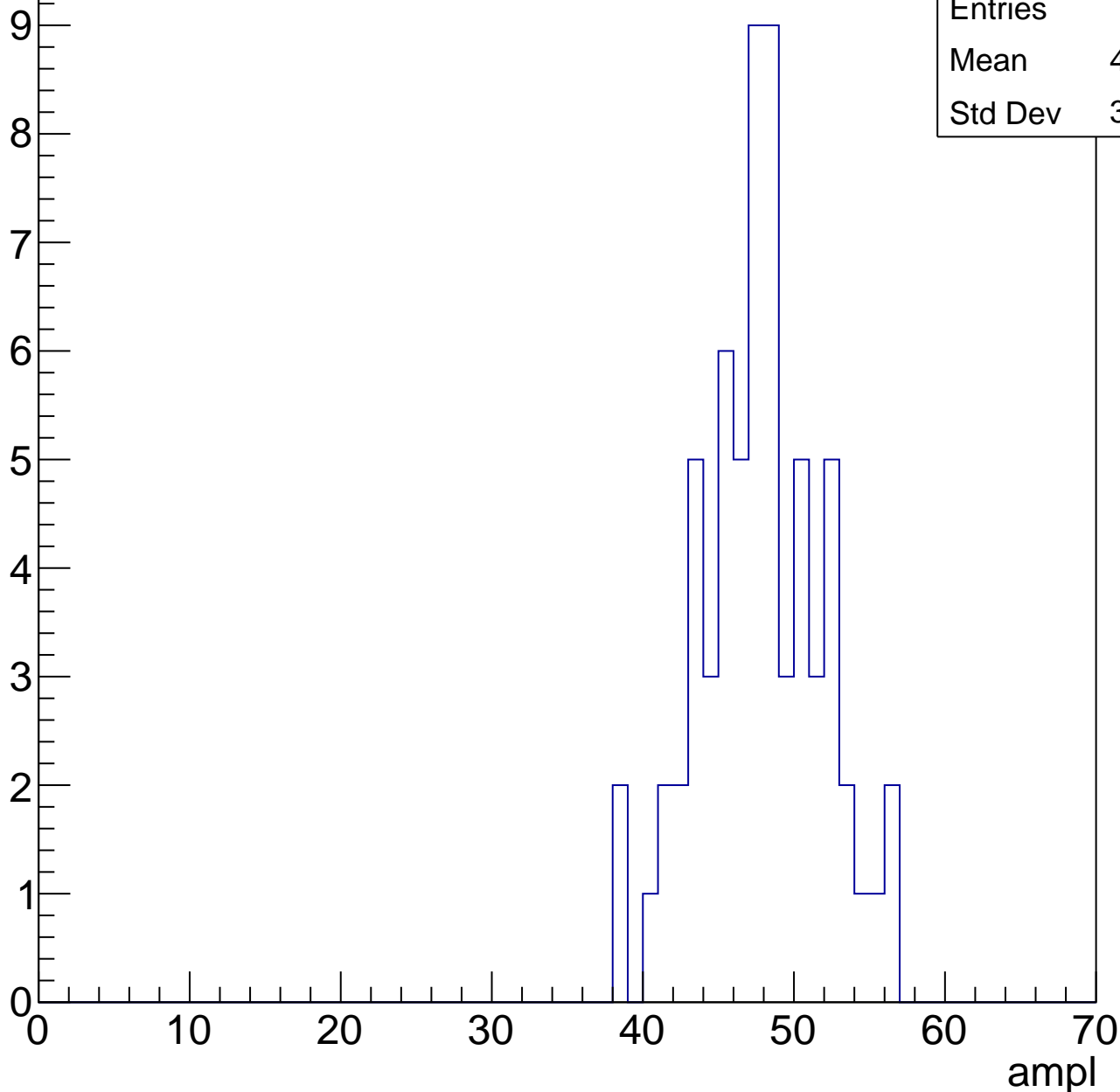
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U1-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



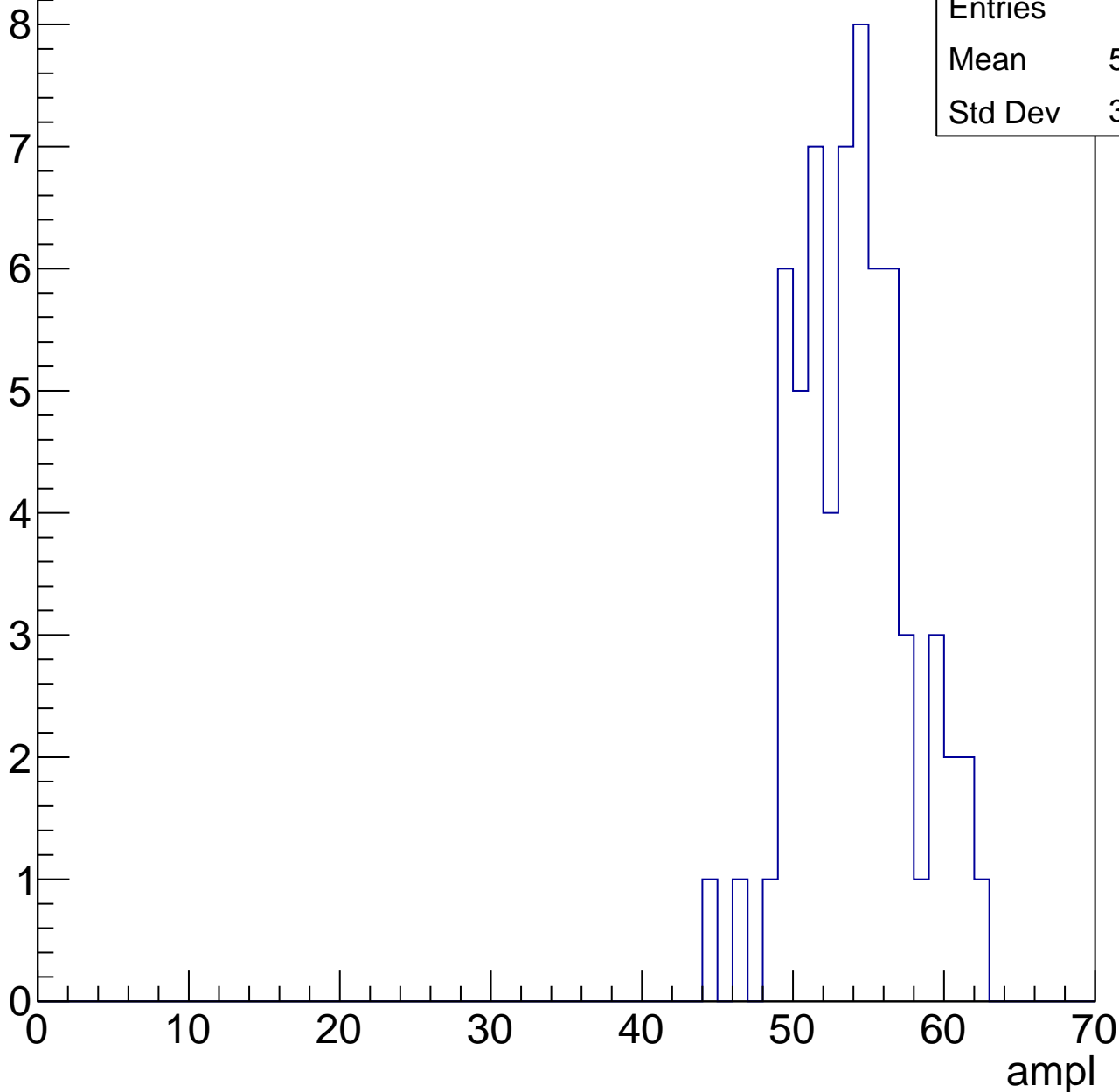
Entries	66
Mean	47.29
Std Dev	3.988

# B1L103S, U1-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	53.53
Std Dev	3.716

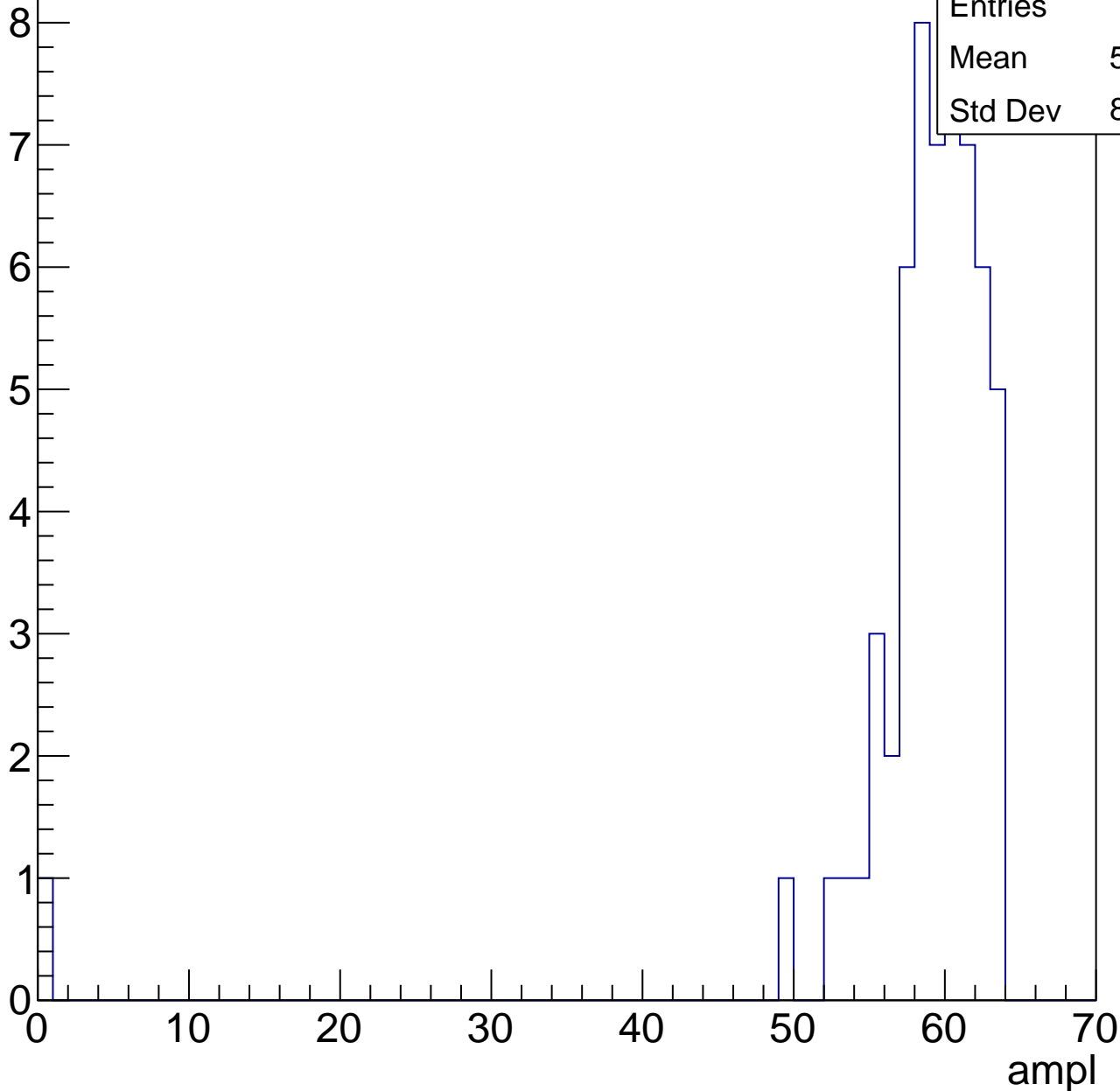


# B1L103S, U1-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

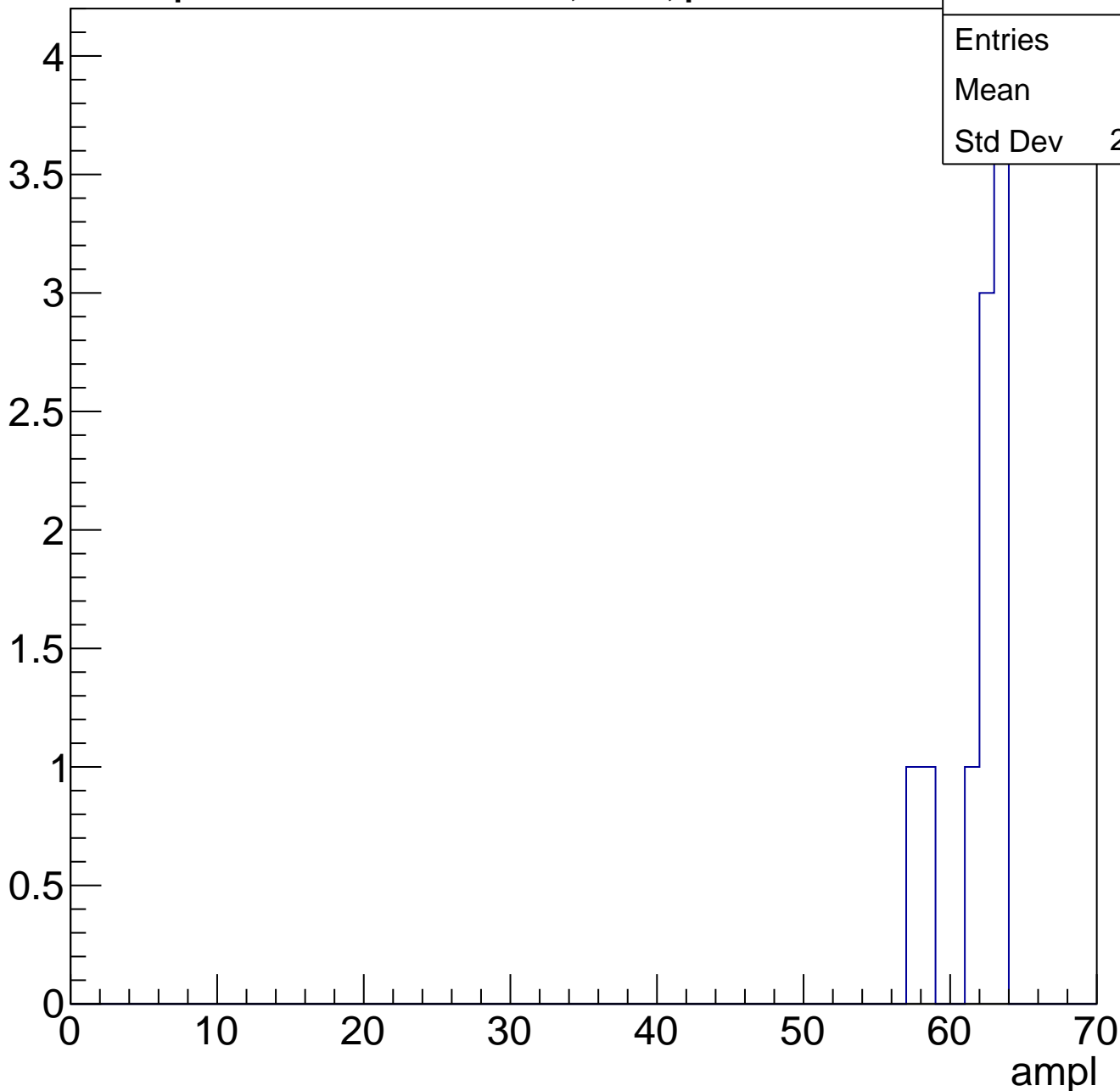
Entries	57
Mean	57.86
Std Dev	8.256



# B1L103S, U1-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U1-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch54, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	78
Mean	27.53
Std Dev	6.391

**Gaus mean : 28.6683**

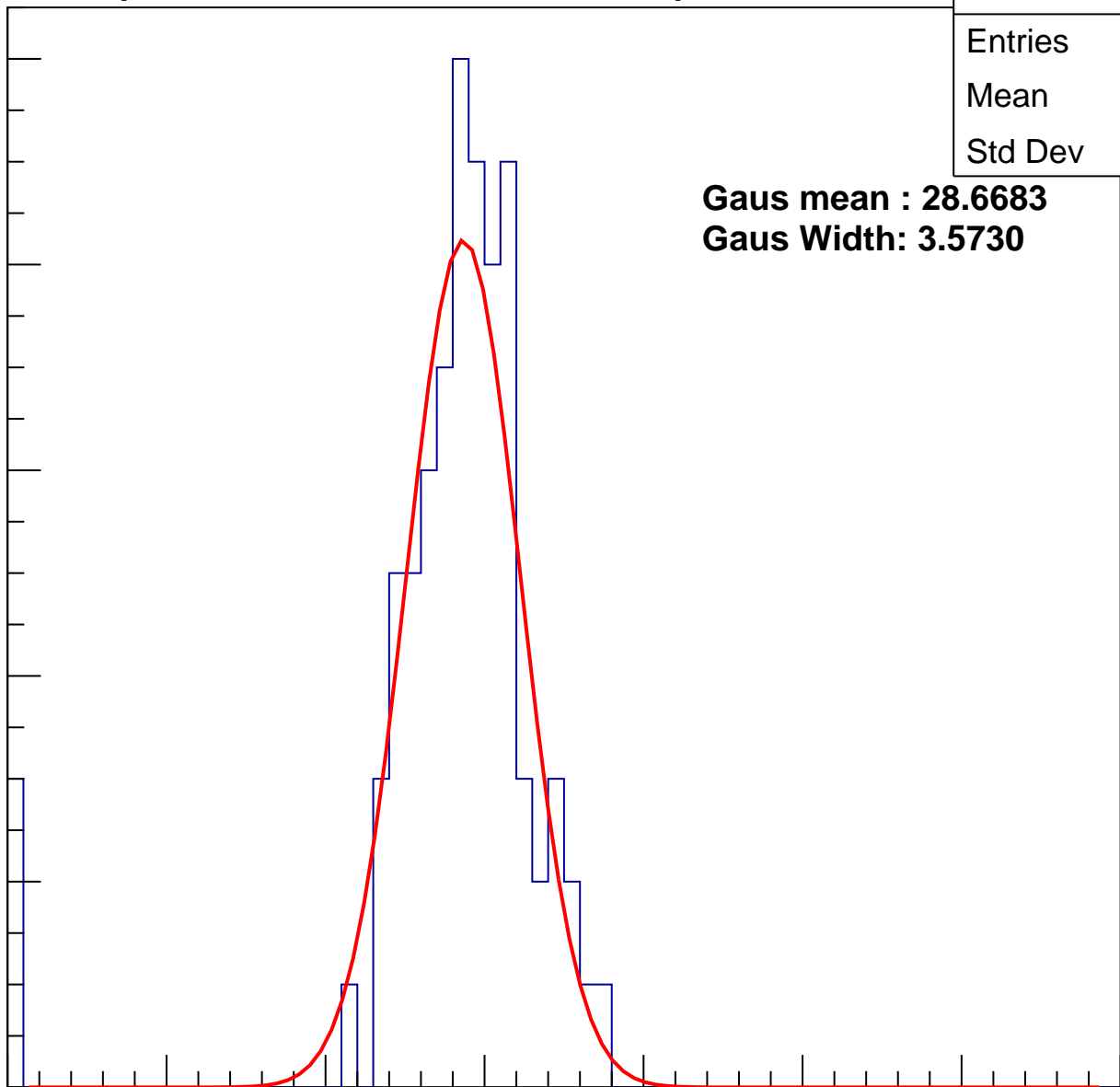
**Gaus Width: 3.5730**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U1-ch54, adc1

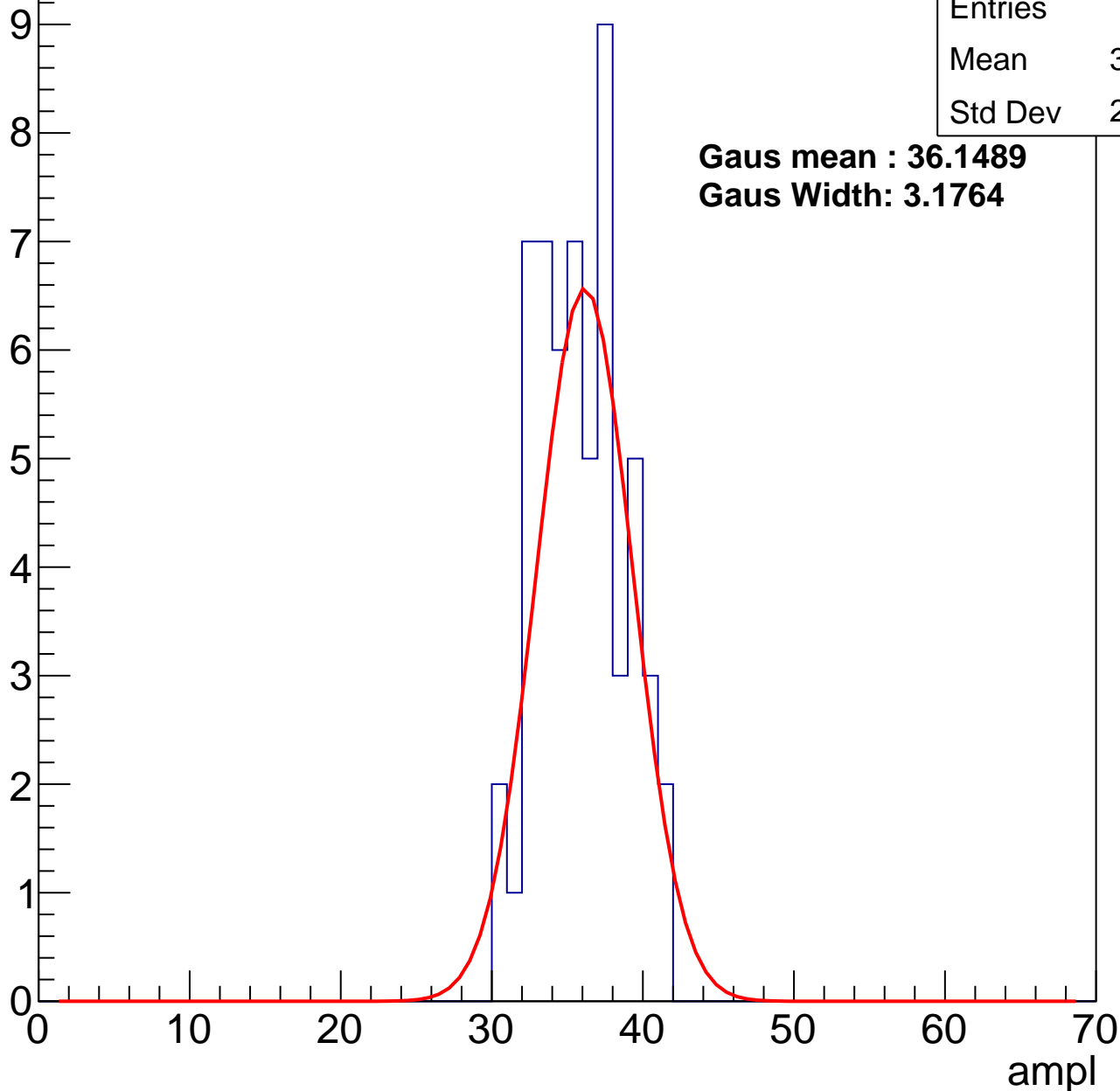
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	35.42
Std Dev	2.803

**Gaus mean : 36.1489**

**Gaus Width: 3.1764**



# B1L103S, U1-ch54, adc2

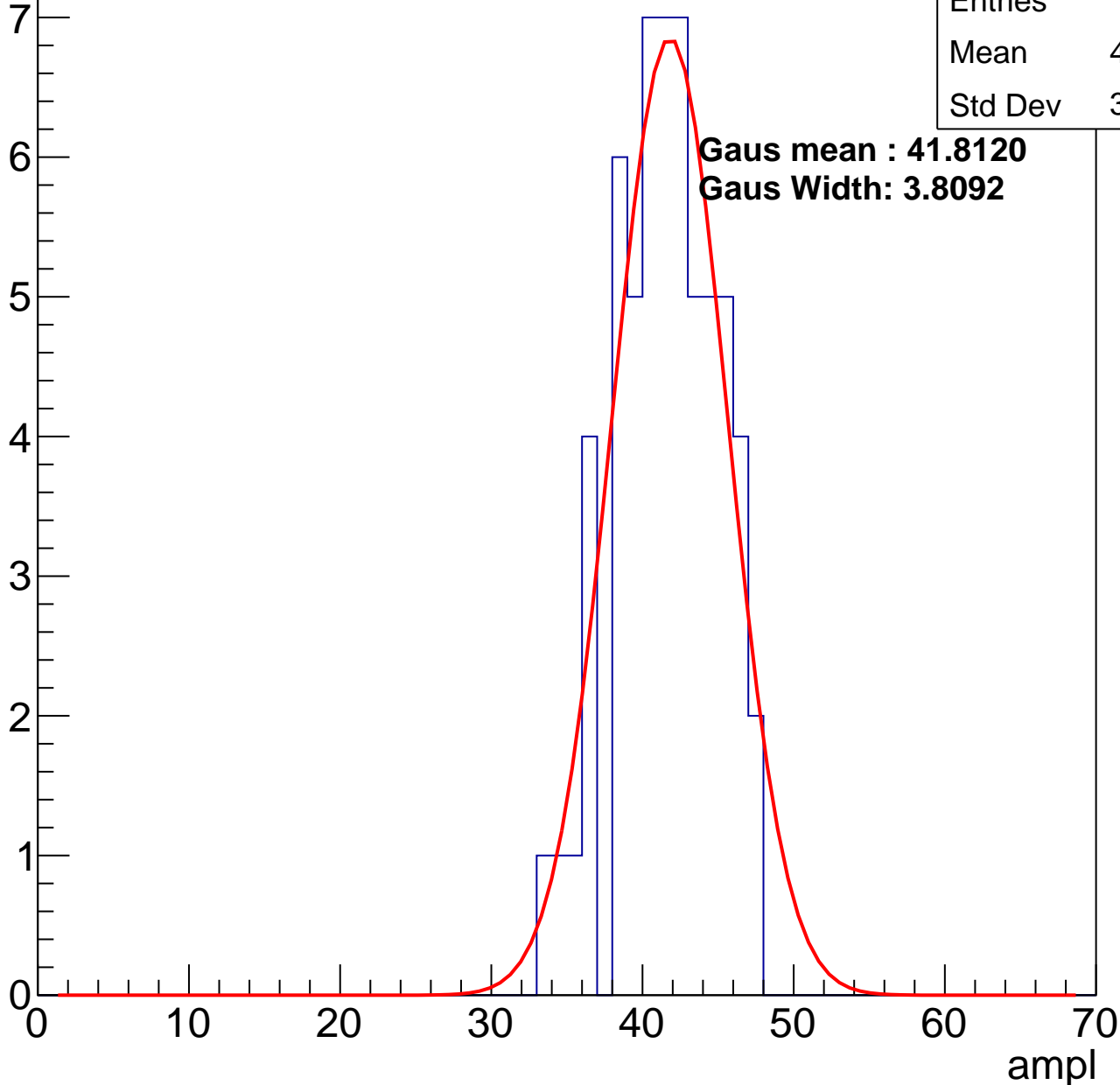
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	41.13
Std Dev	3.299

**Gaus mean : 41.8120**

**Gaus Width: 3.8092**

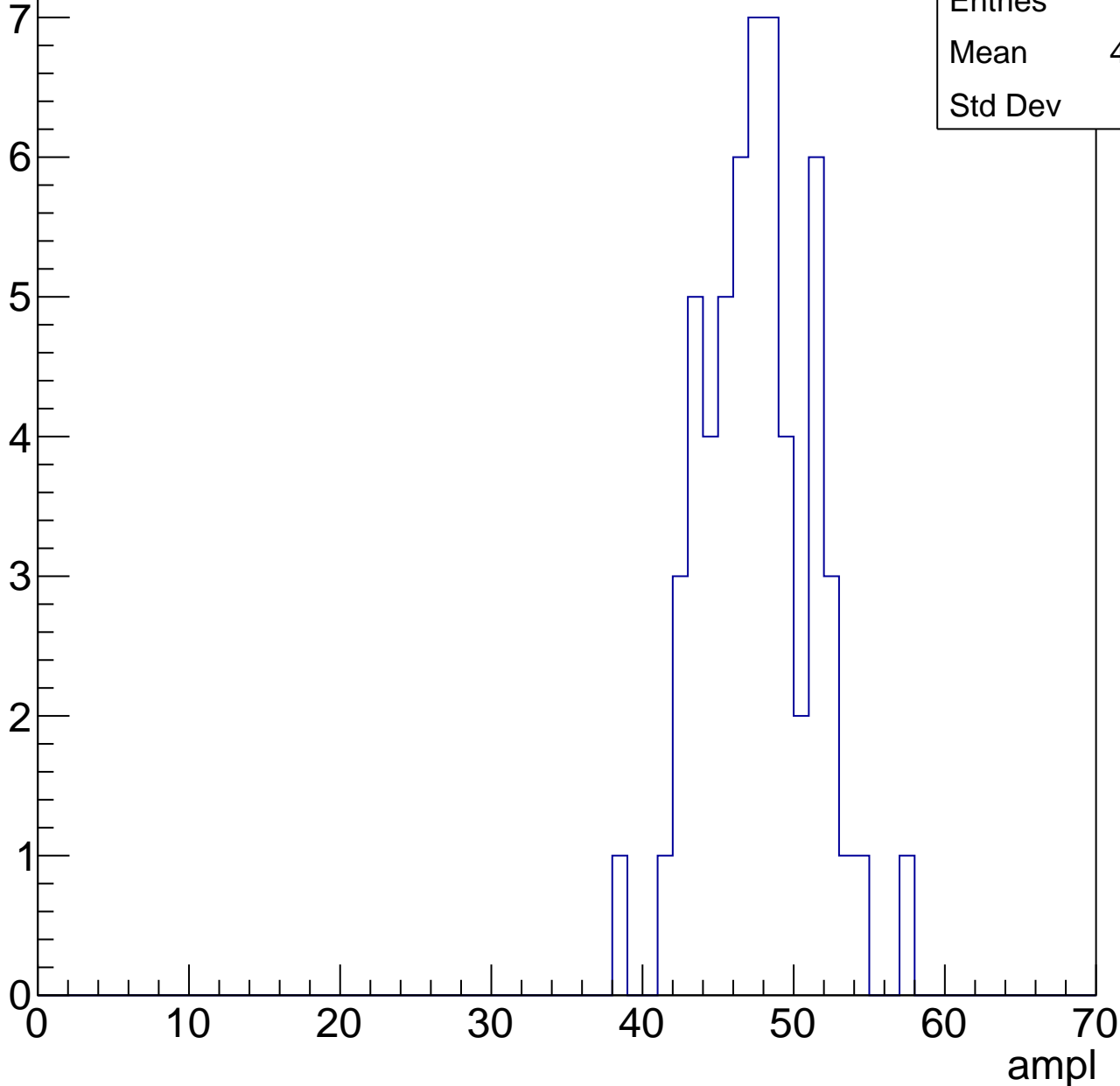


# B1L103S, U1-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

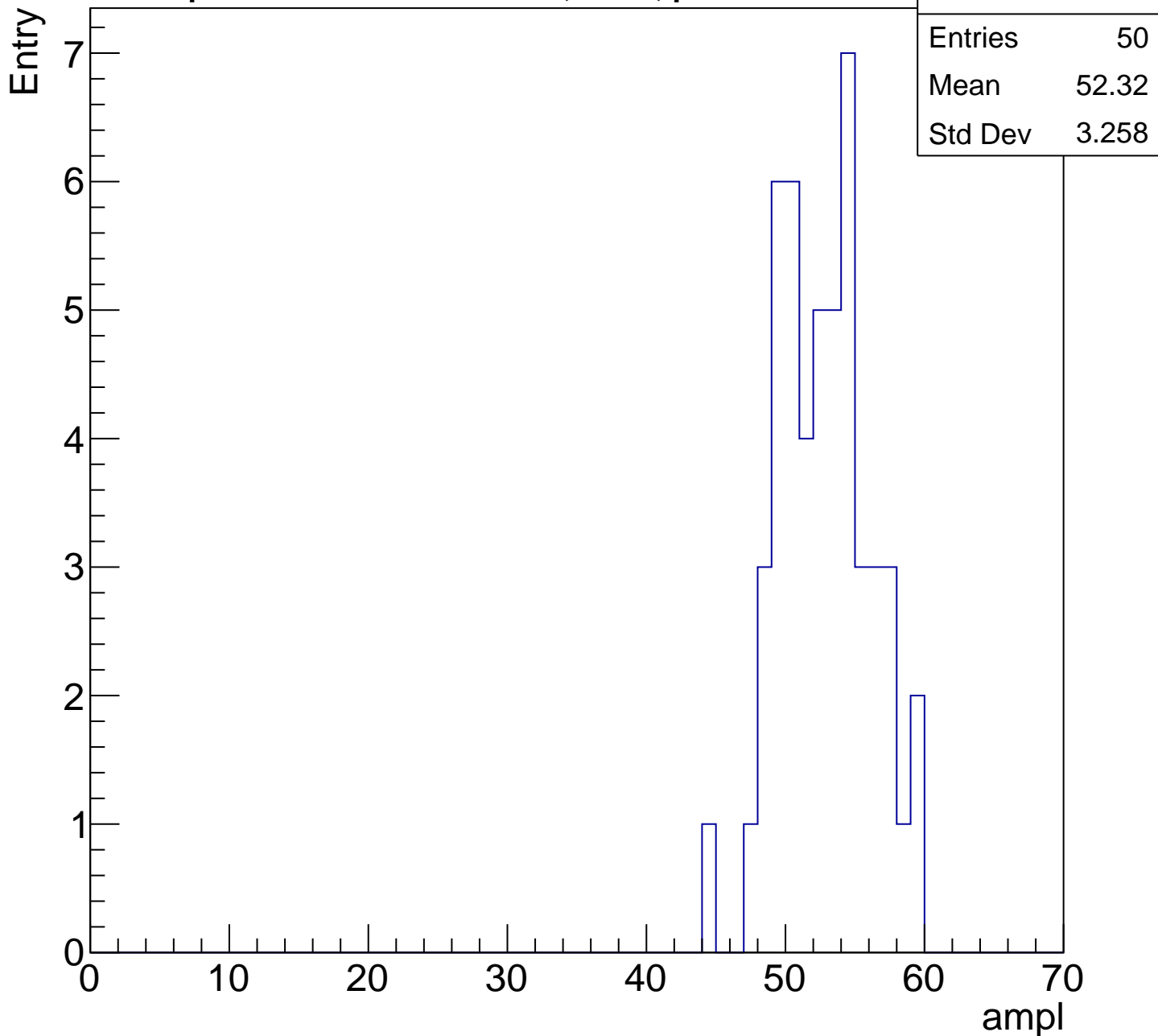
Entry

Entries	57
Mean	47.09
Std Dev	3.58



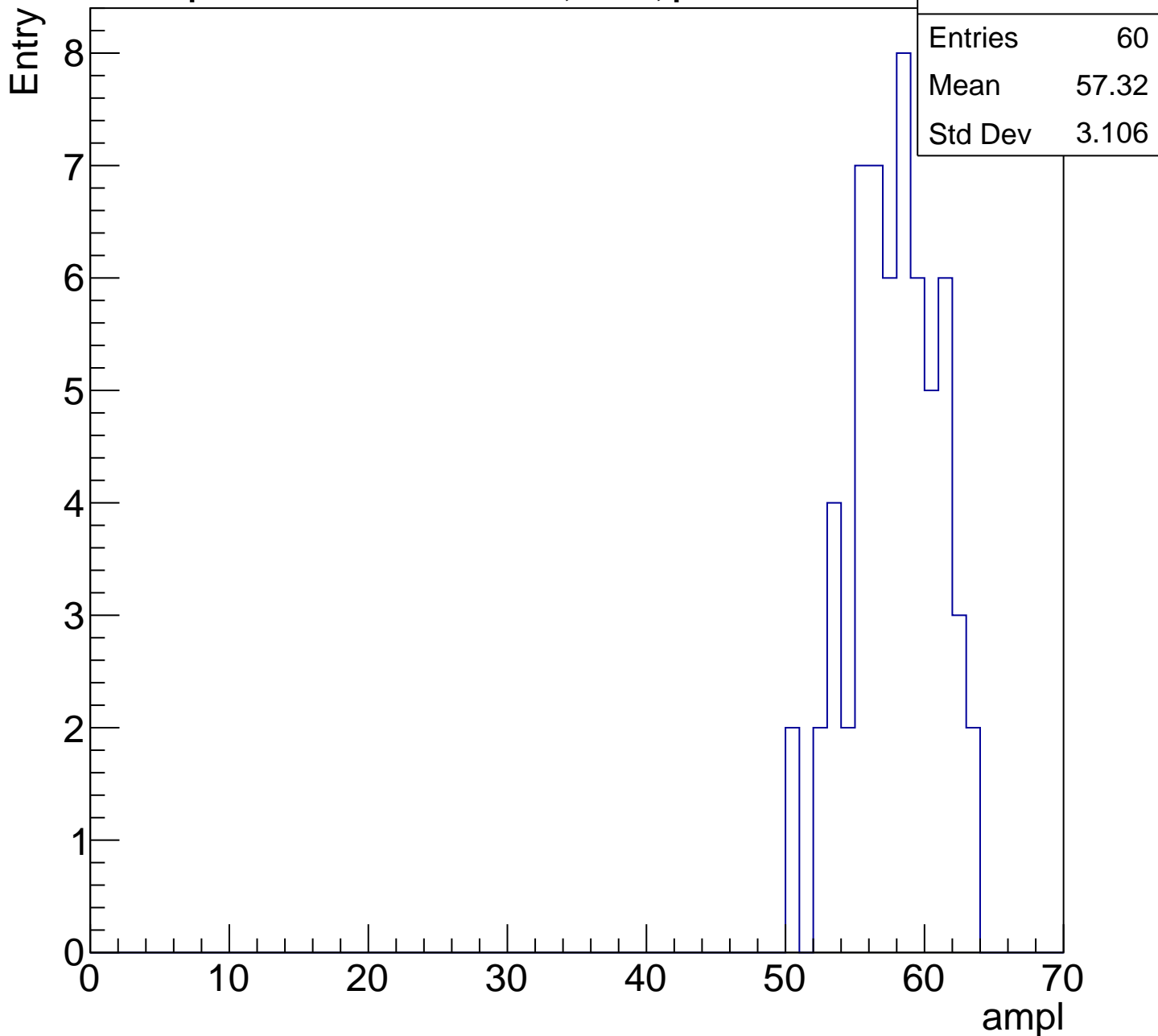
# B1L103S, U1-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U1-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

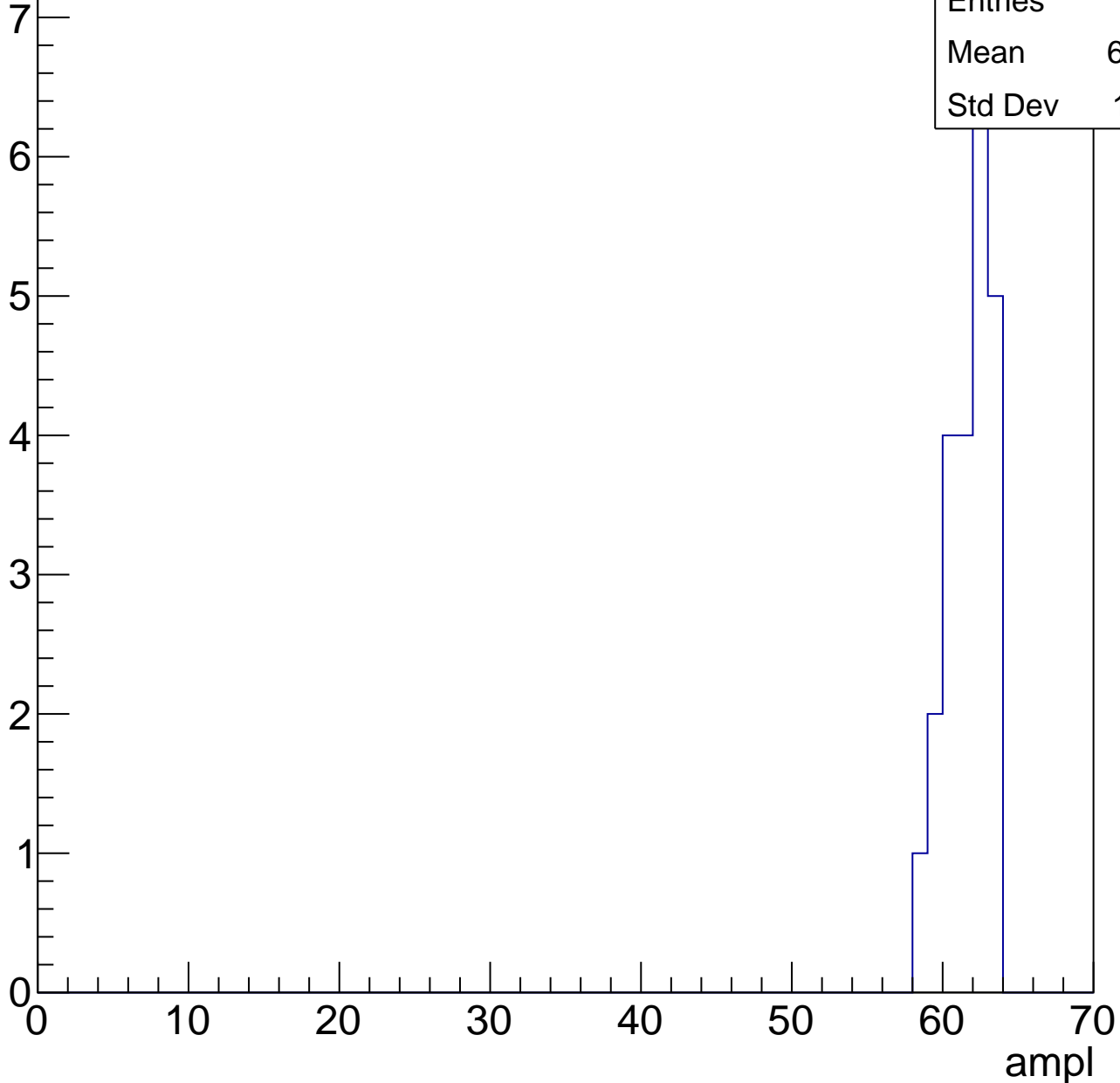


# B1L103S, U1-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	23
Mean	61.26
Std Dev	1.421

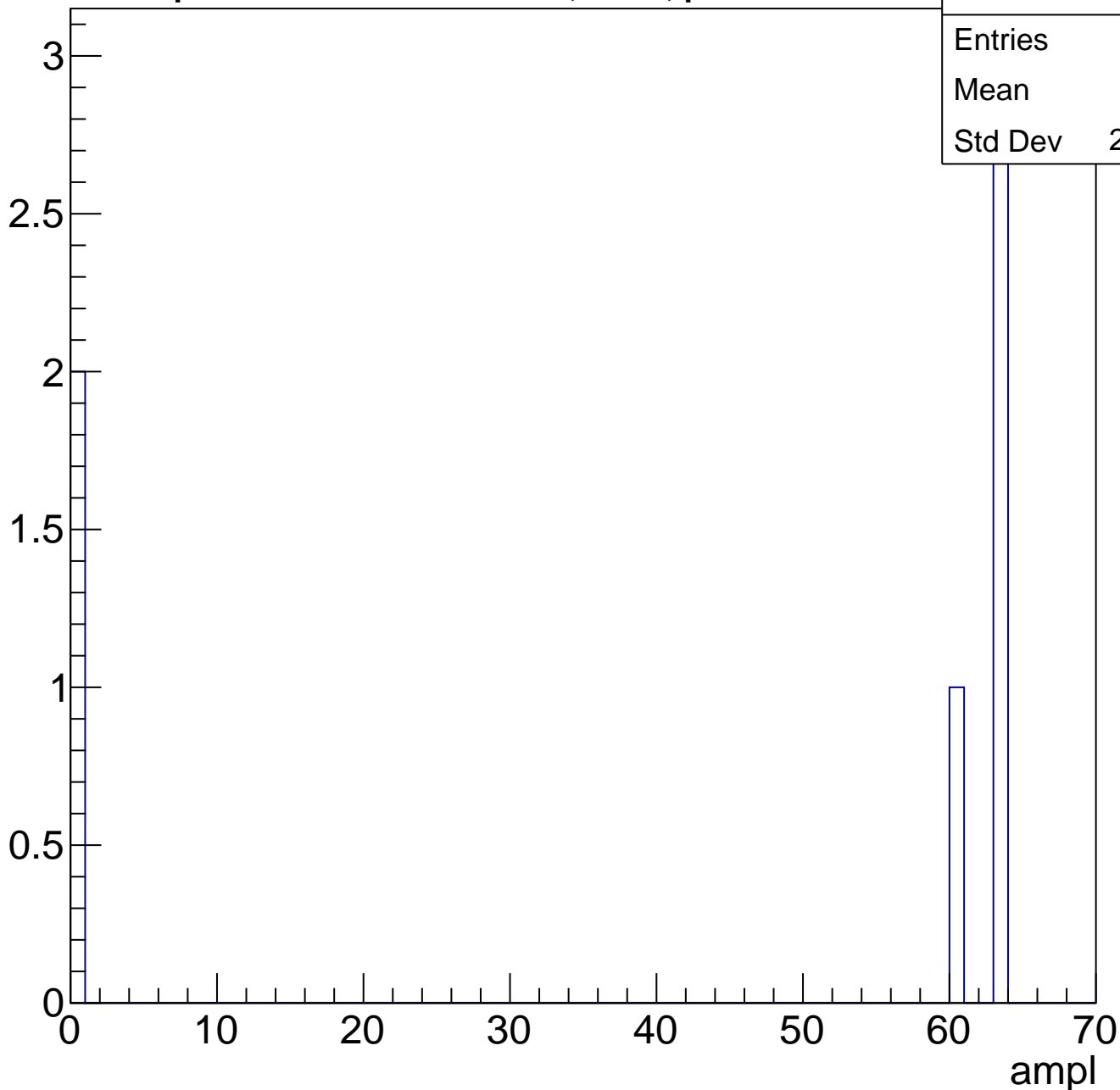




# B1L103S, U1-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch55, adc0

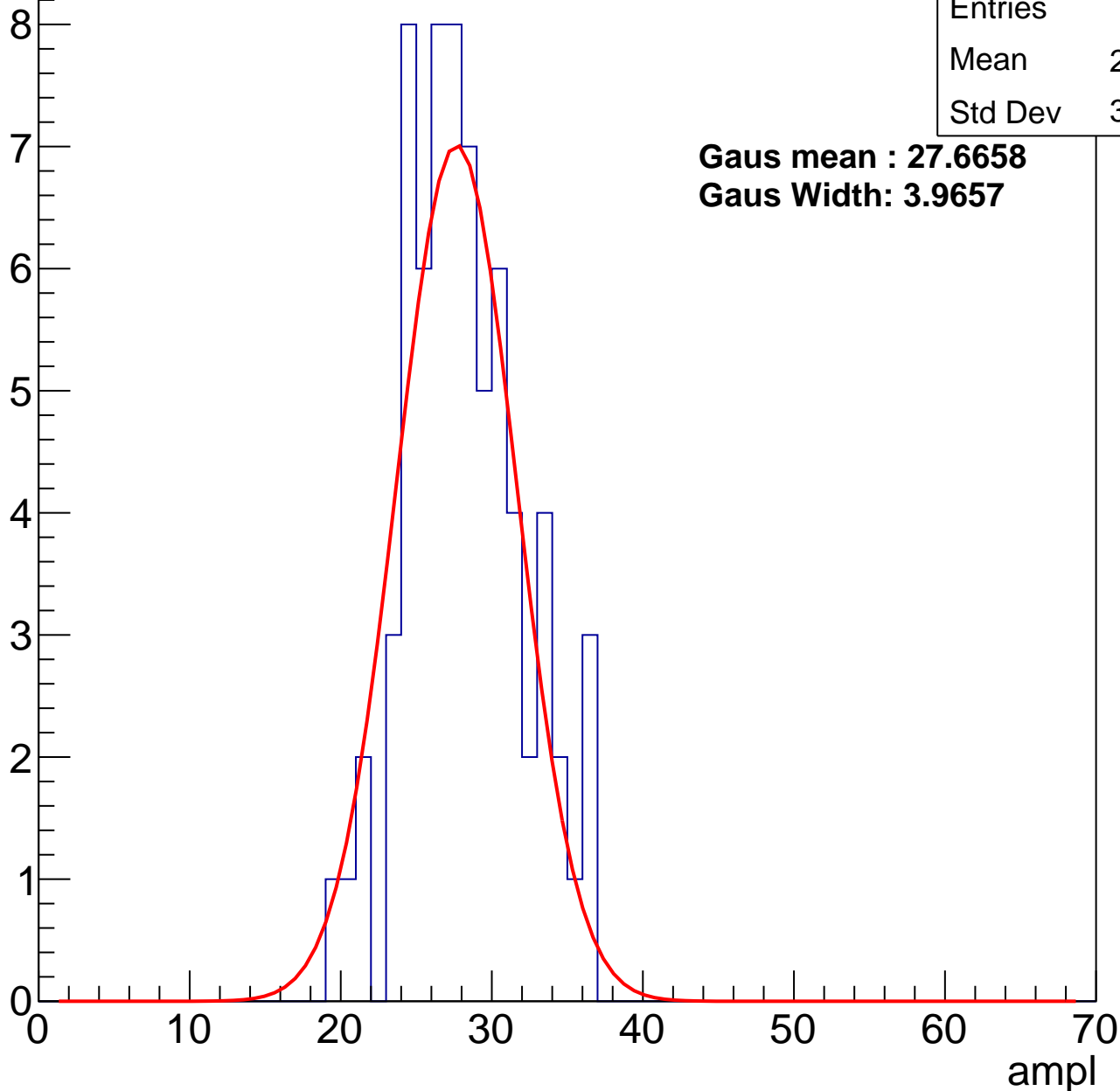
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	27.72
Std Dev	3.835

**Gaus mean : 27.6658**

**Gaus Width: 3.9657**



# B1L103S, U1-ch55, adc1

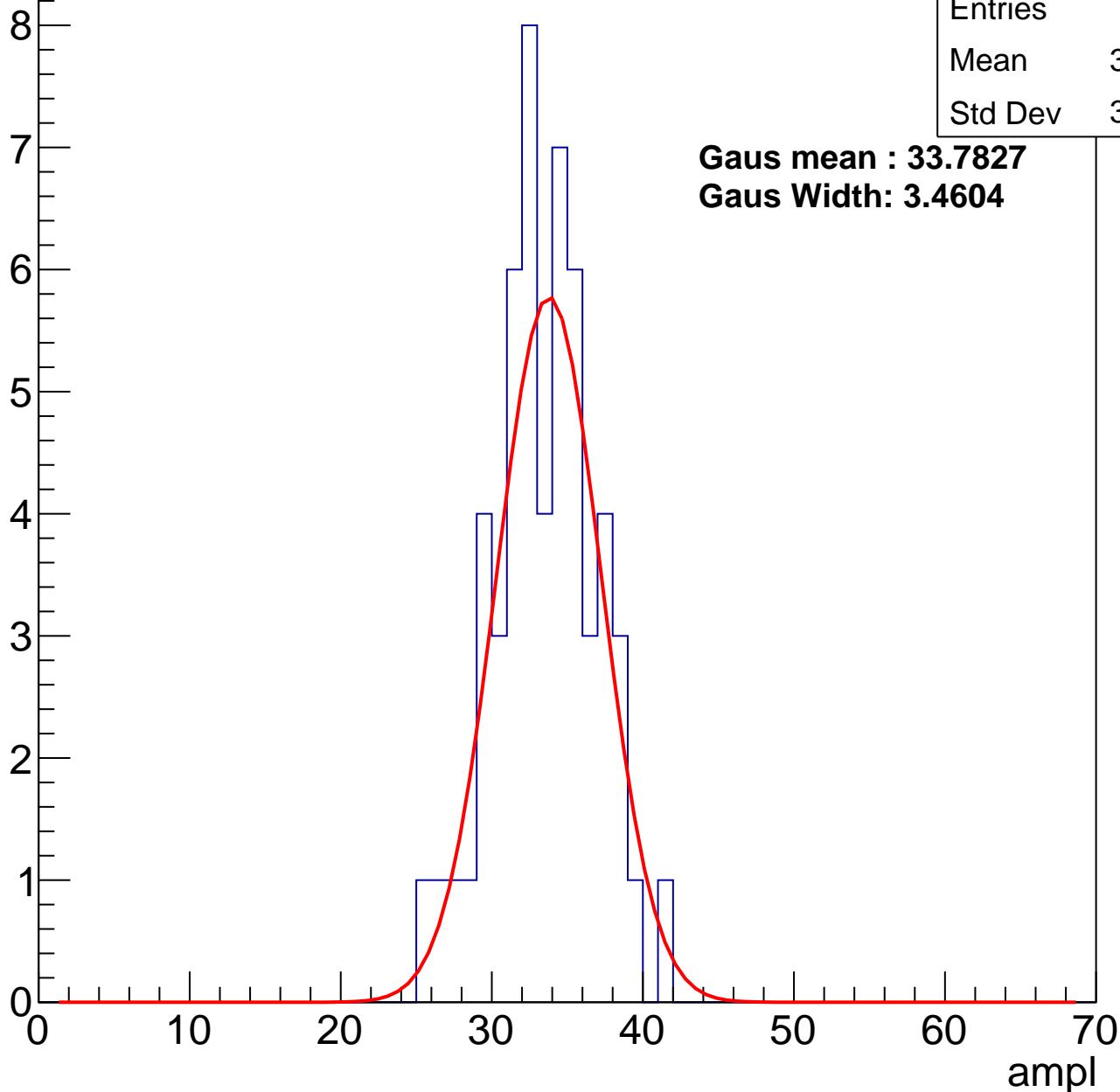
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	33.04
Std Dev	3.316

**Gaus mean : 33.7827**

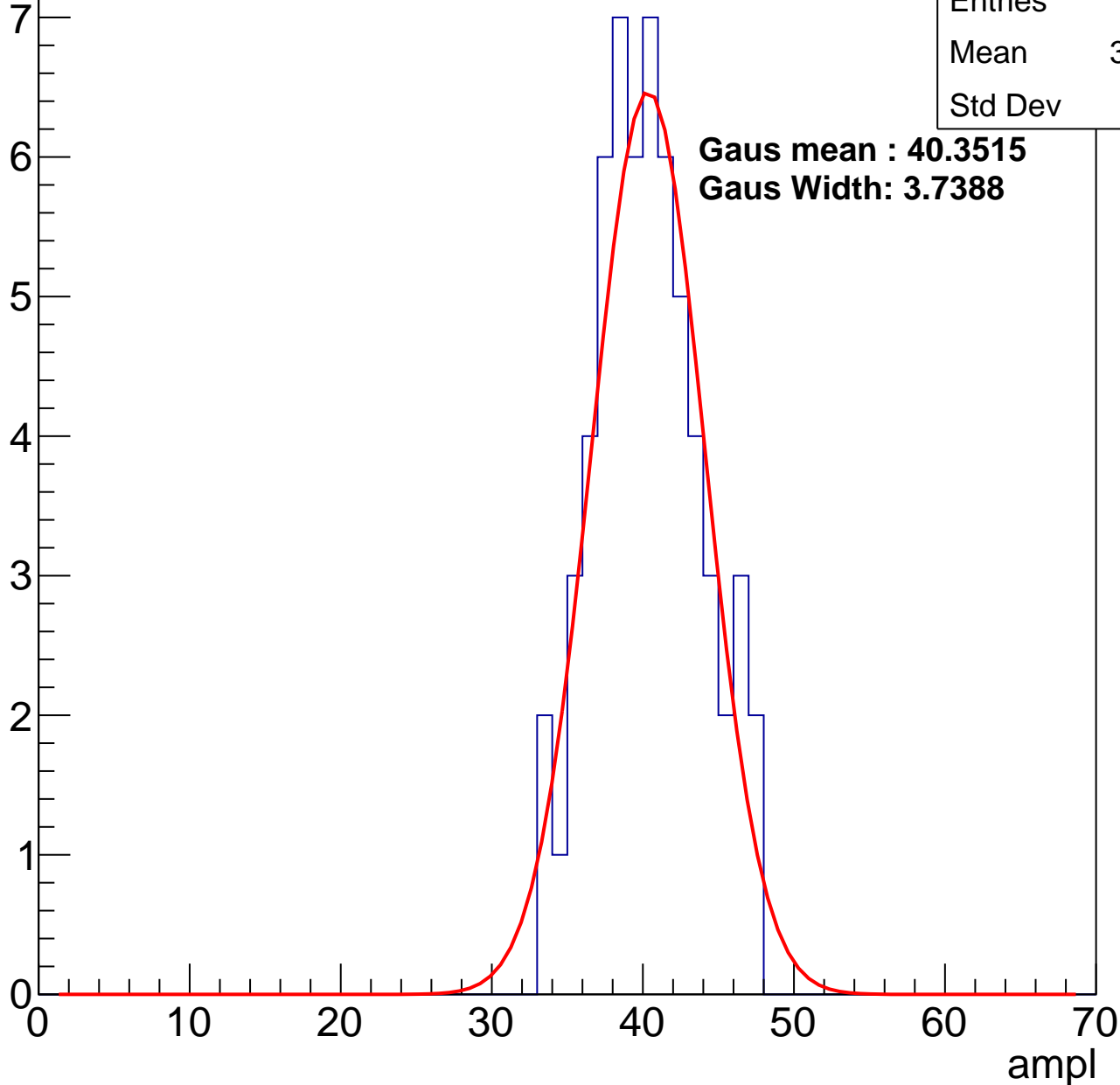
**Gaus Width: 3.4604**



# B1L103S, U1-ch55, adc2

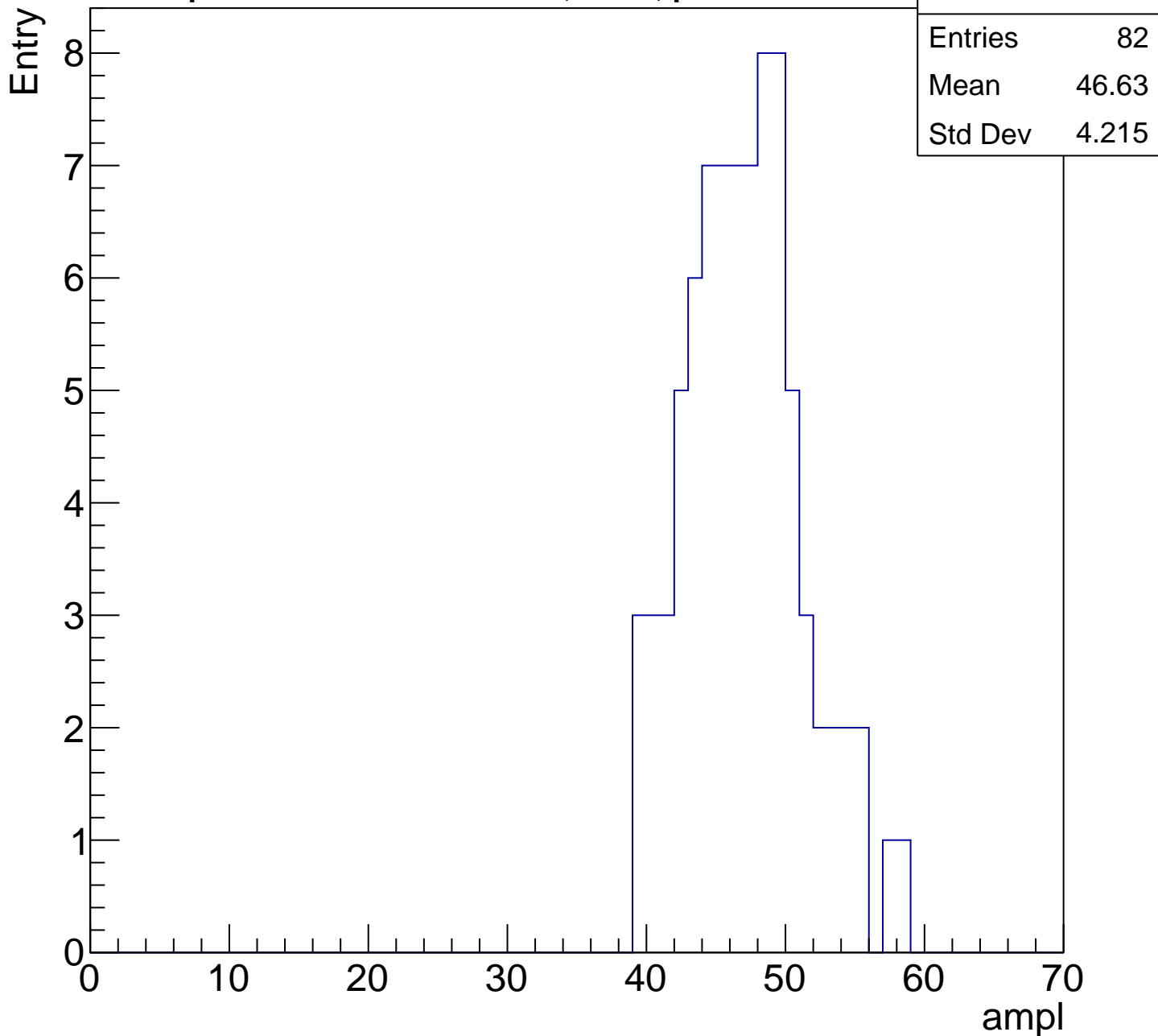
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

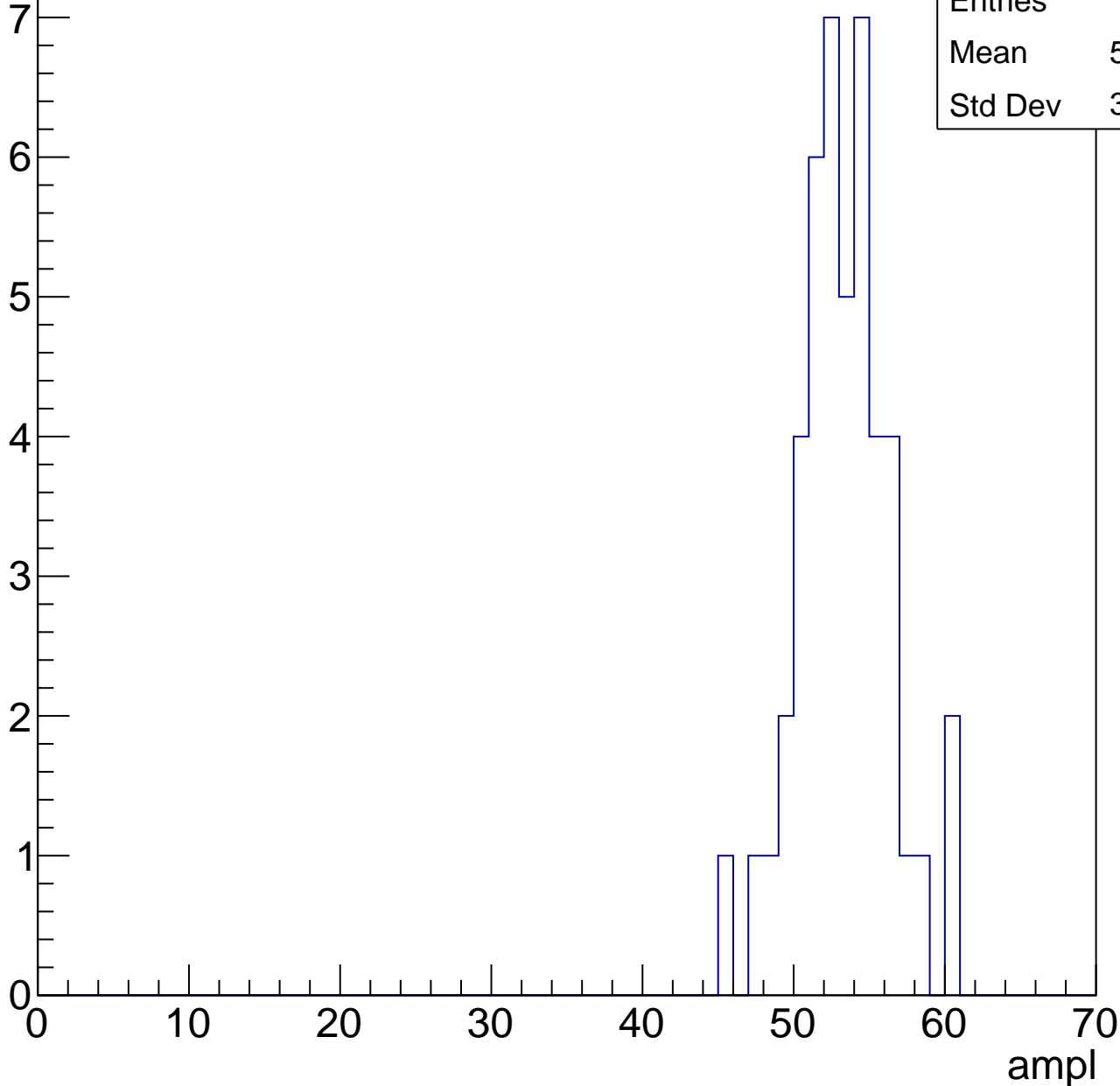


# B1L103S, U1-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

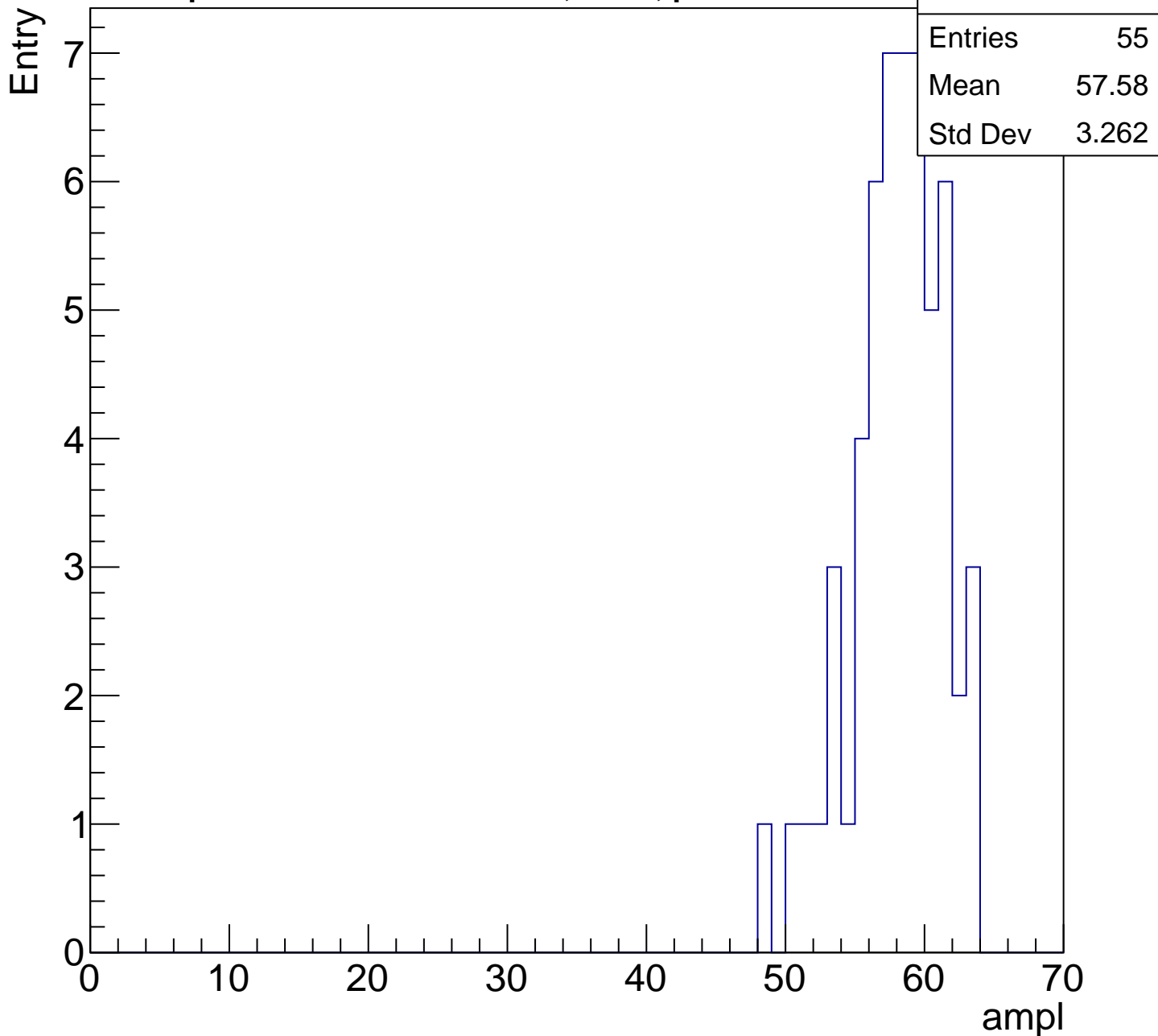
Entry

Entries	46
Mean	52.83
Std Dev	3.024



# B1L103S, U1-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

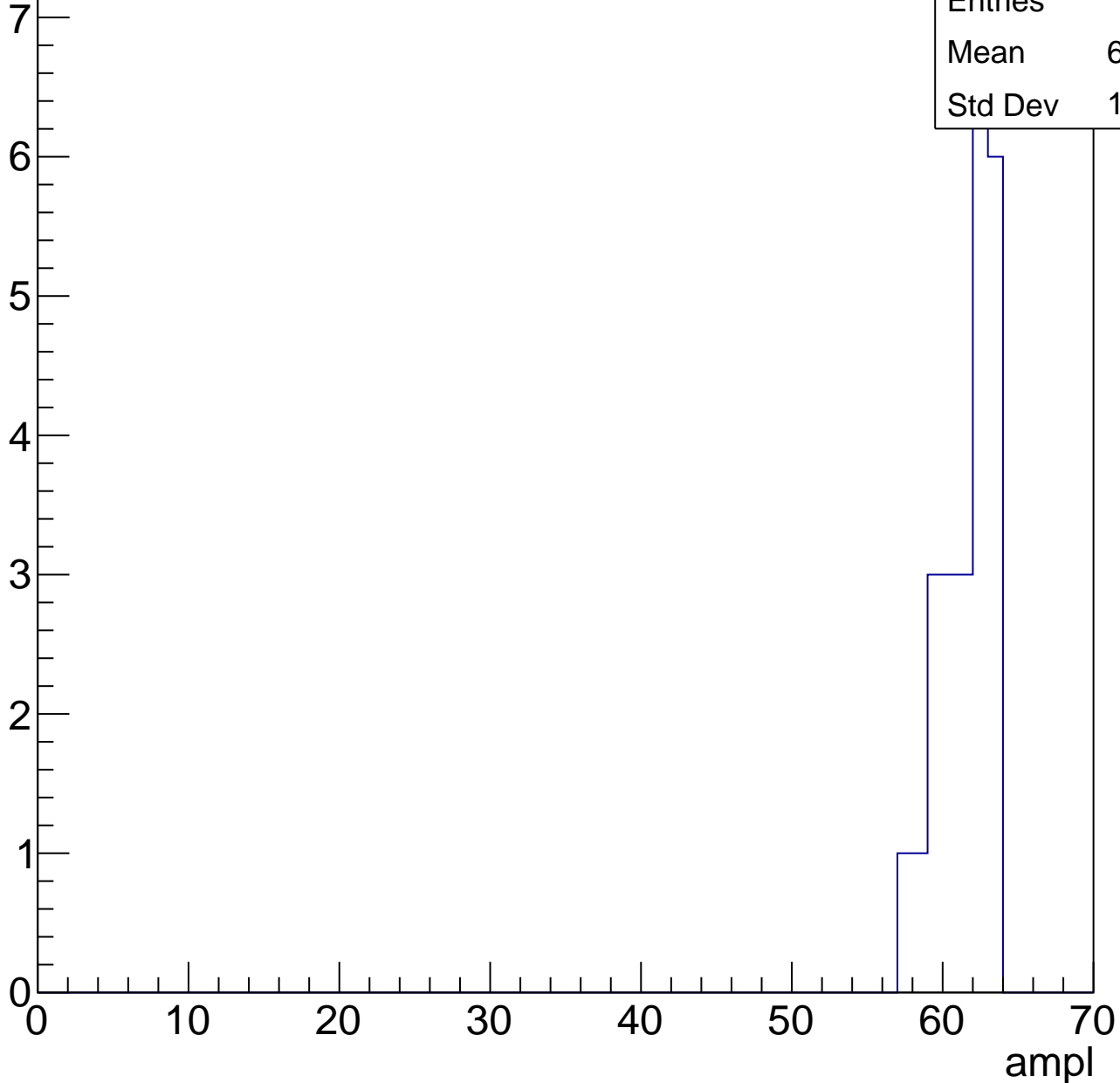


# B1L103S, U1-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	24
Mean	61.12
Std Dev	1.715

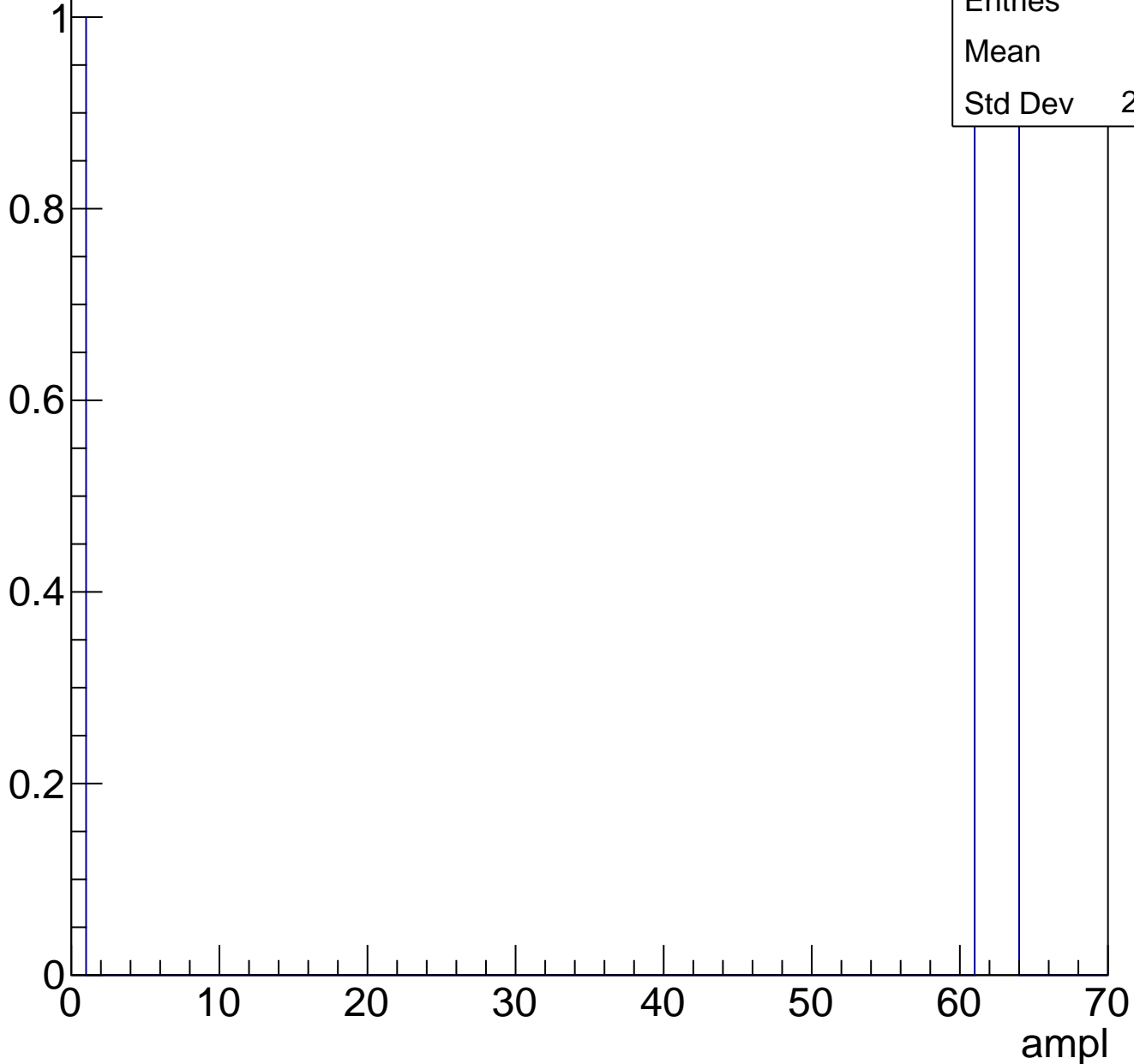




# B1L103S, U1-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch56, adc0

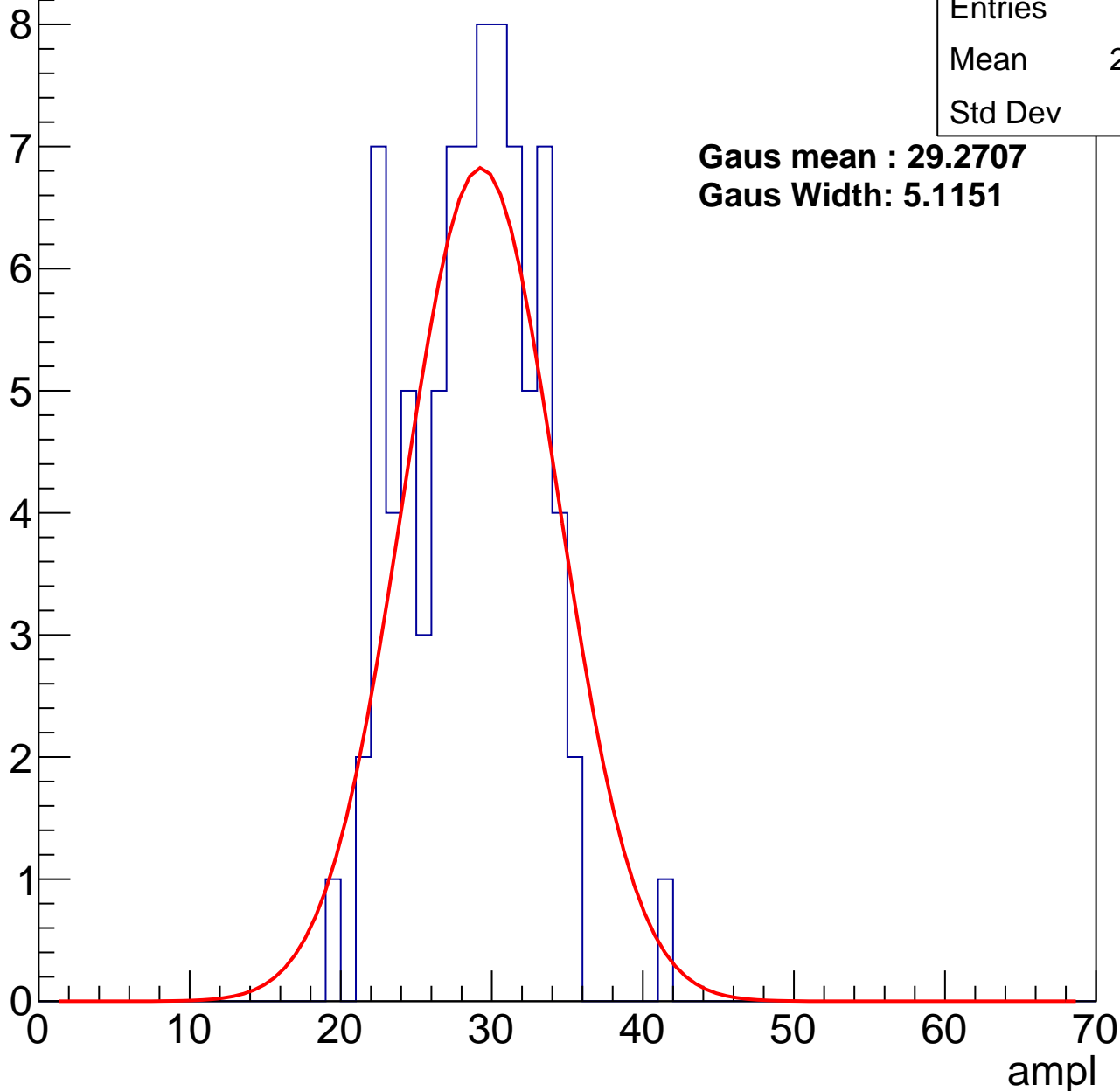
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	28.24
Std Dev	4.15

**Gaus mean : 29.2707**

**Gaus Width: 5.1151**



# B1L103S, U1-ch56, adc1

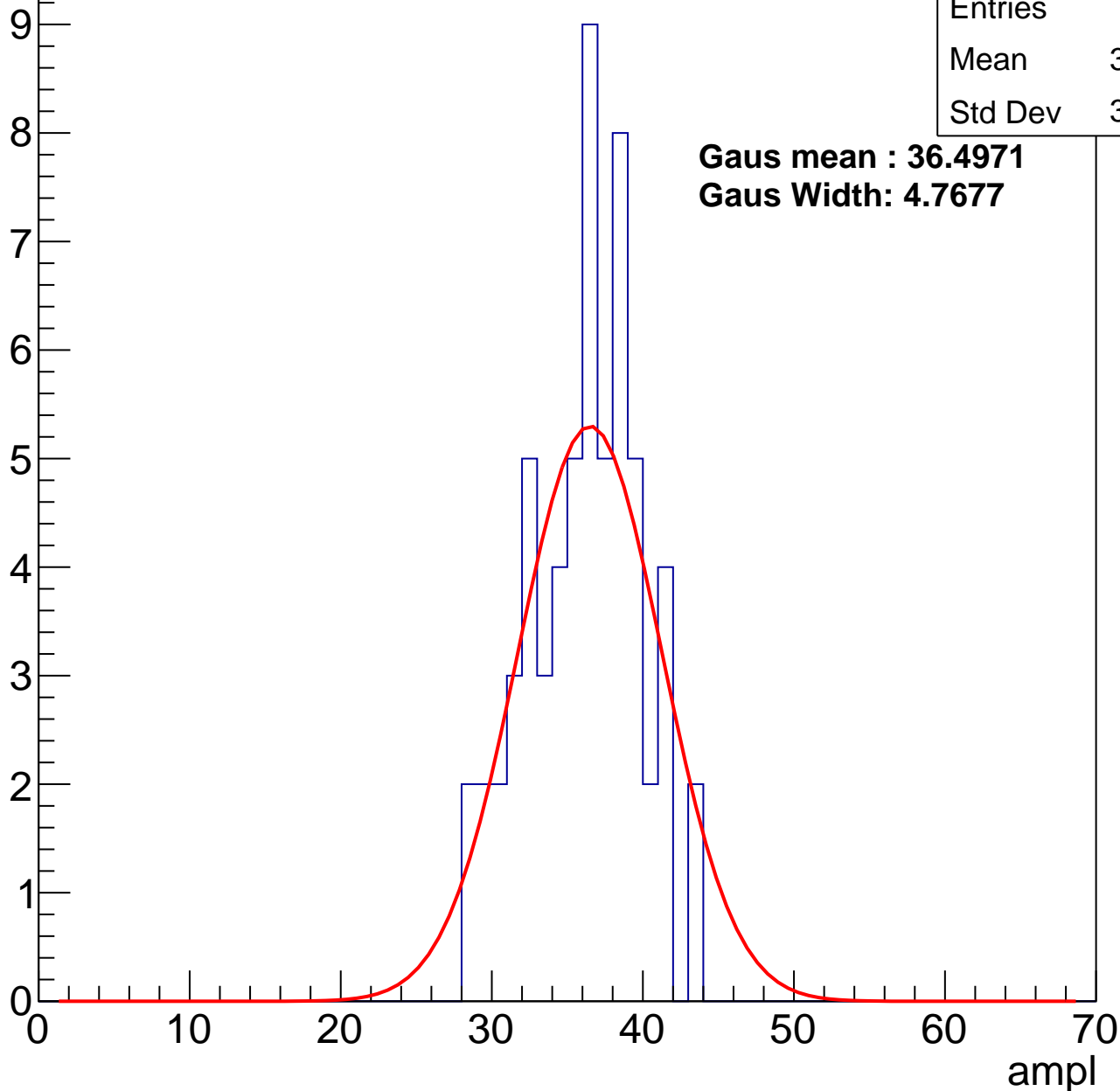
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	35.66
Std Dev	3.634

**Gaus mean : 36.4971**

**Gaus Width: 4.7677**



# B1L103S, U1-ch56, adc2

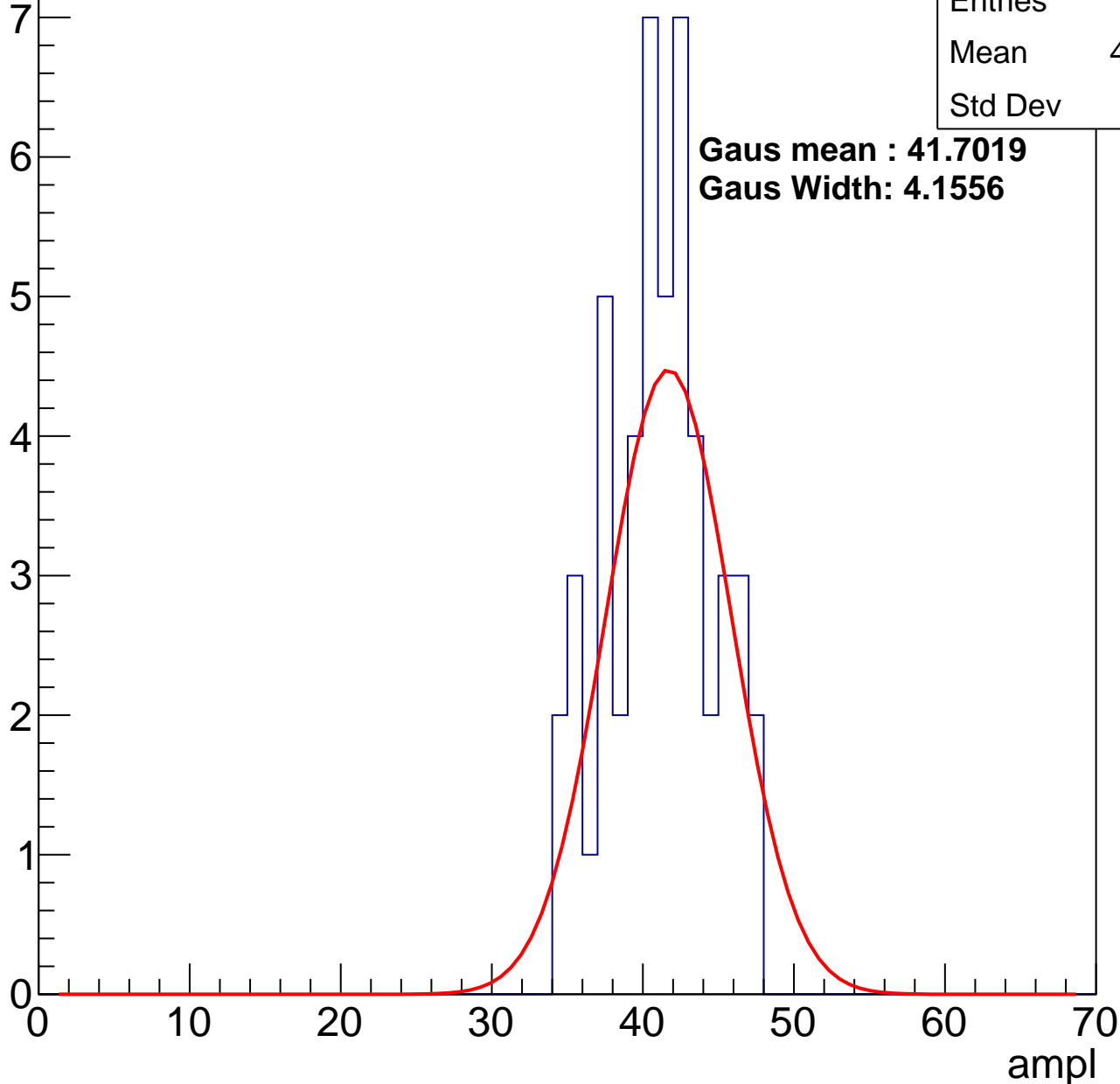
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	40.64
Std Dev	3.41

**Gaus mean : 41.7019**

**Gaus Width: 4.1556**

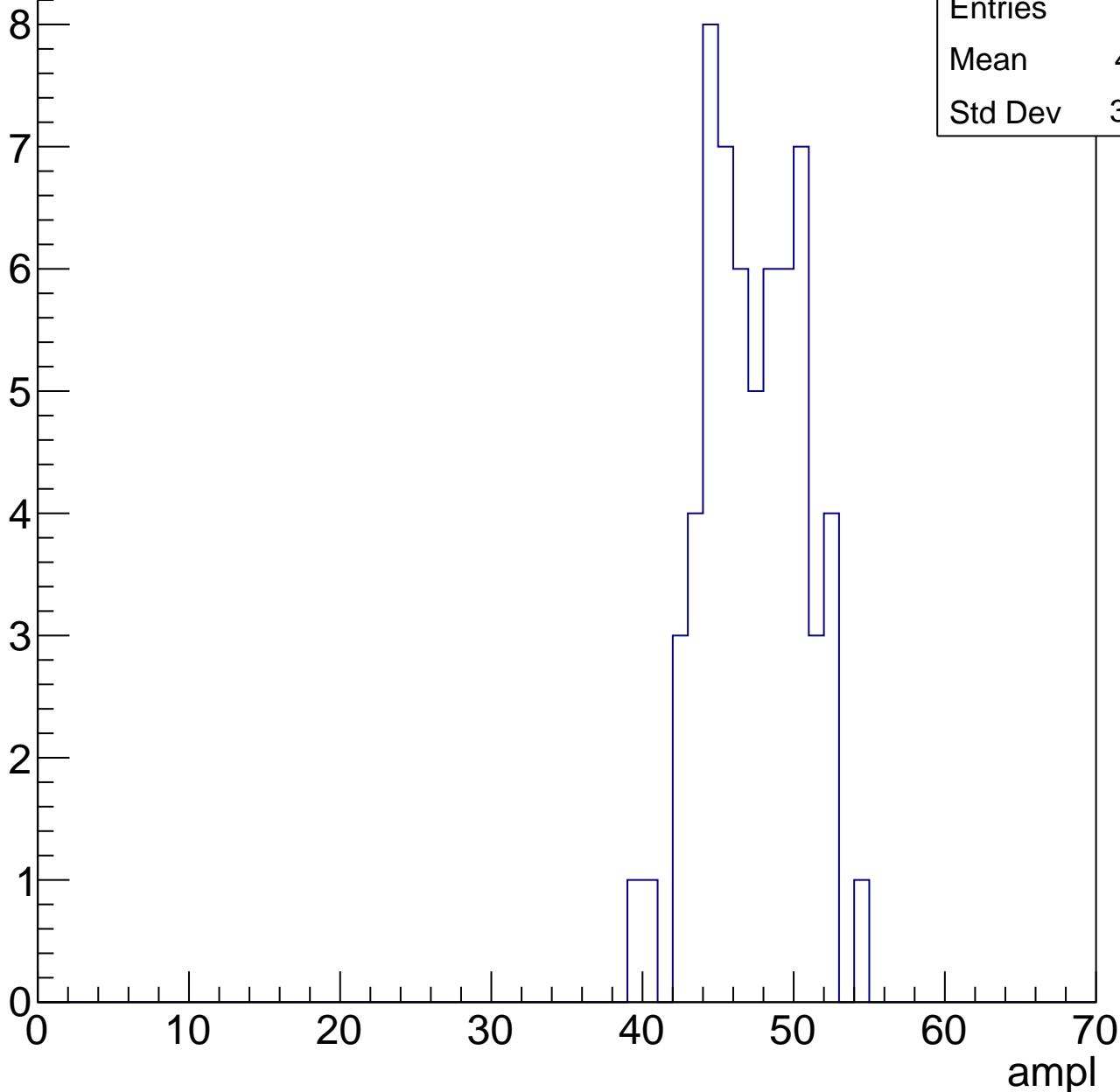


# B1L103S, U1-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

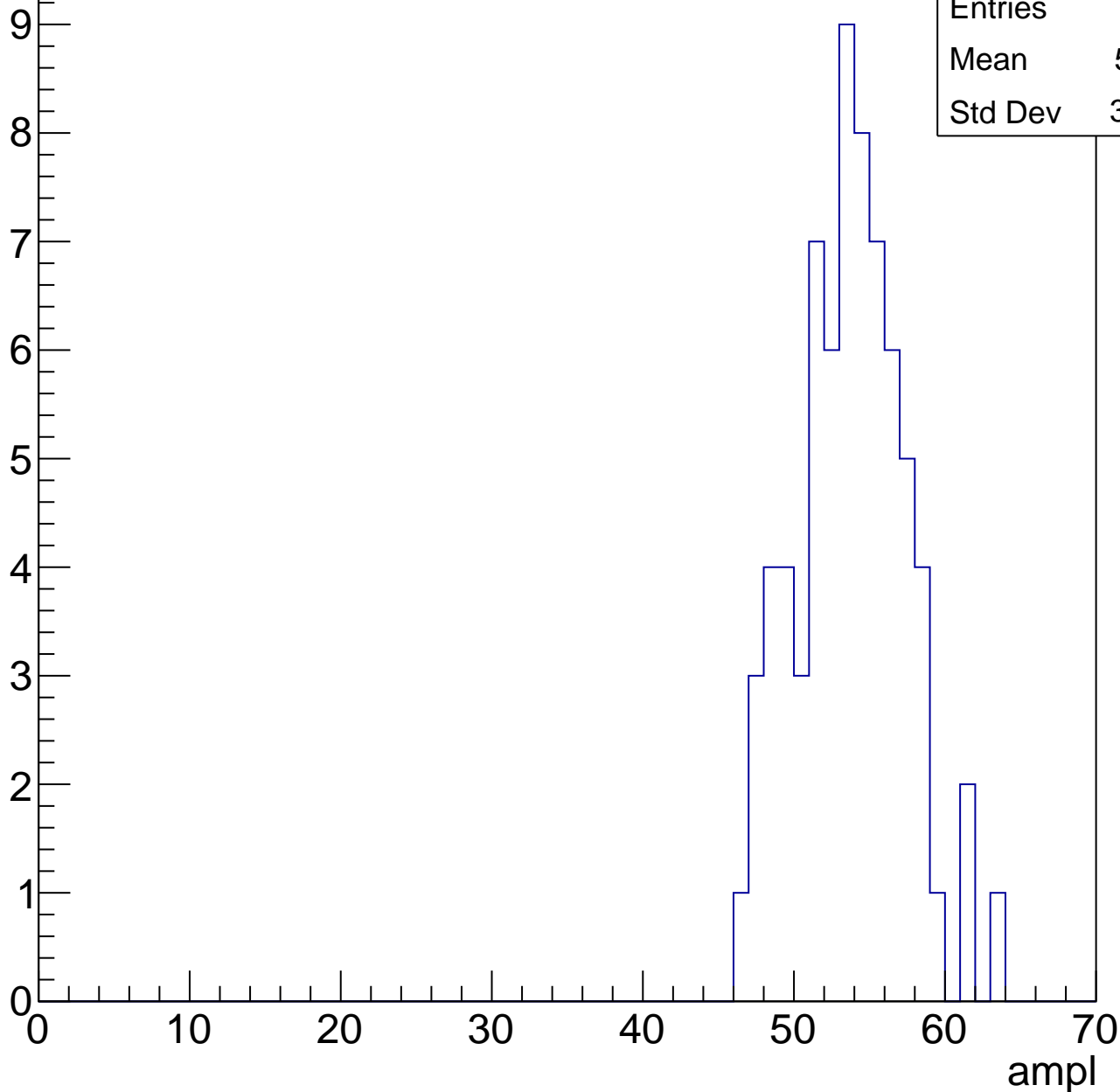
Entries	62
Mean	46.81
Std Dev	3.227



# B1L103S, U1-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

7

6

5

4

3

2

1

0

Entries

40

Mean

59

Std Dev

2.53

0

ampl

0

10

20

30

40

50

60

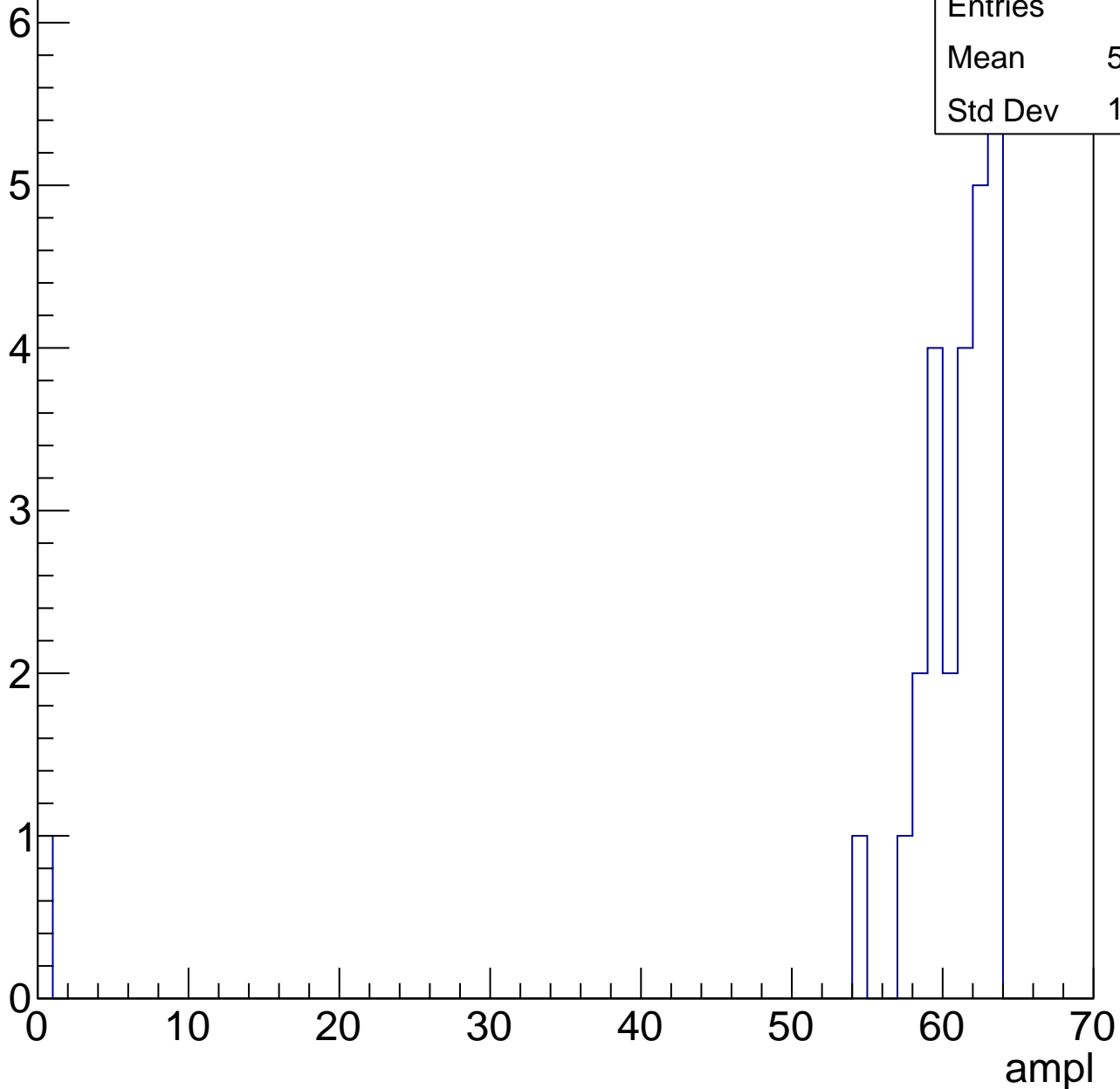
70

# B1L103S, U1-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	26
Mean	58.27
Std Dev	11.86





# B1L103S, U1-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch57, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	77
Mean	28.62
Std Dev	6.011

**Gaus mean : 29.5262**

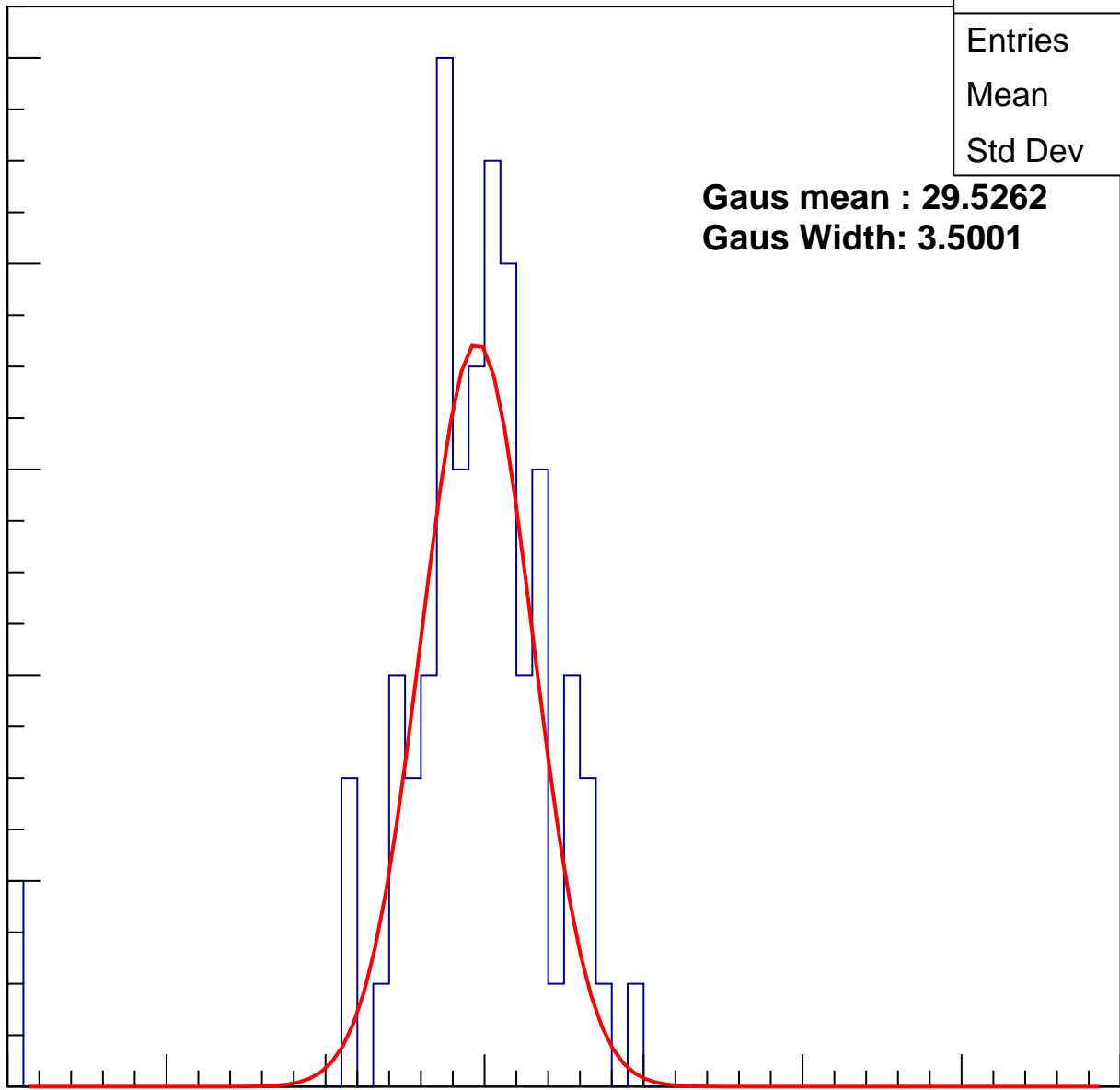
**Gaus Width: 3.5001**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U1-ch57, adc1

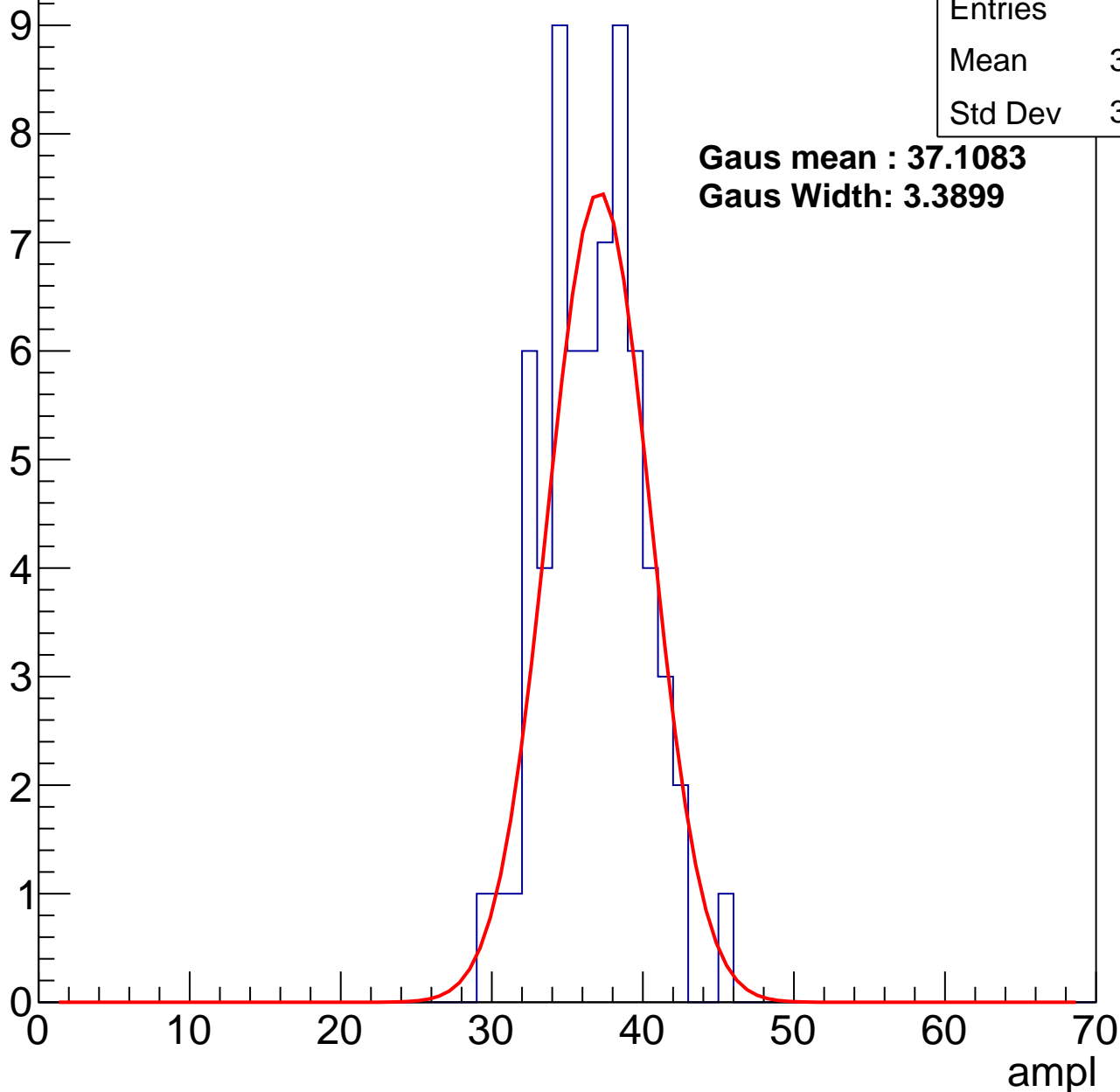
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	36.26
Std Dev	3.183

**Gaus mean : 37.1083**

**Gaus Width: 3.3899**



# B1L103S, U1-ch57, adc2

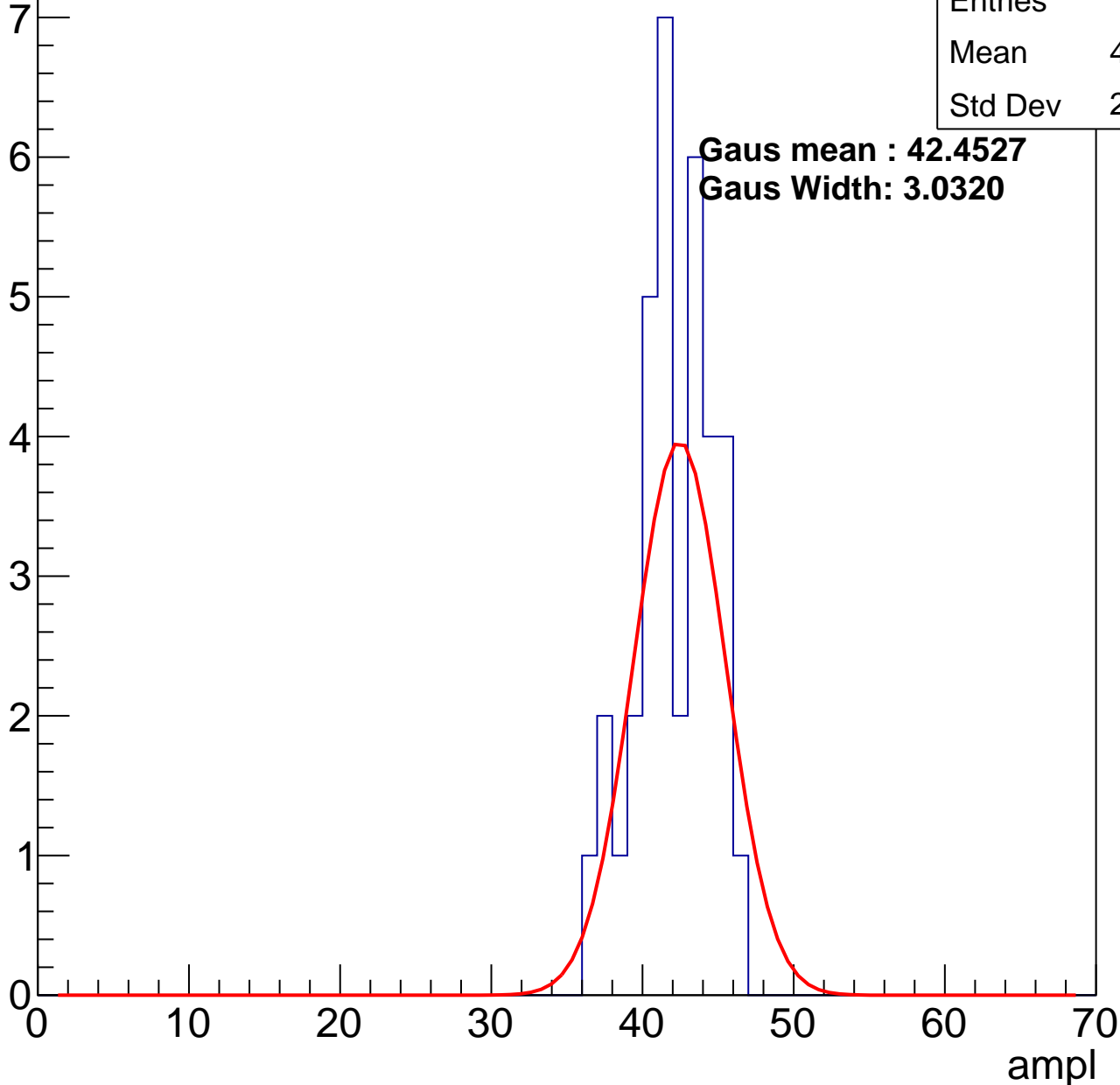
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	35
Mean	41.63
Std Dev	2.485

**Gaus mean : 42.4527**

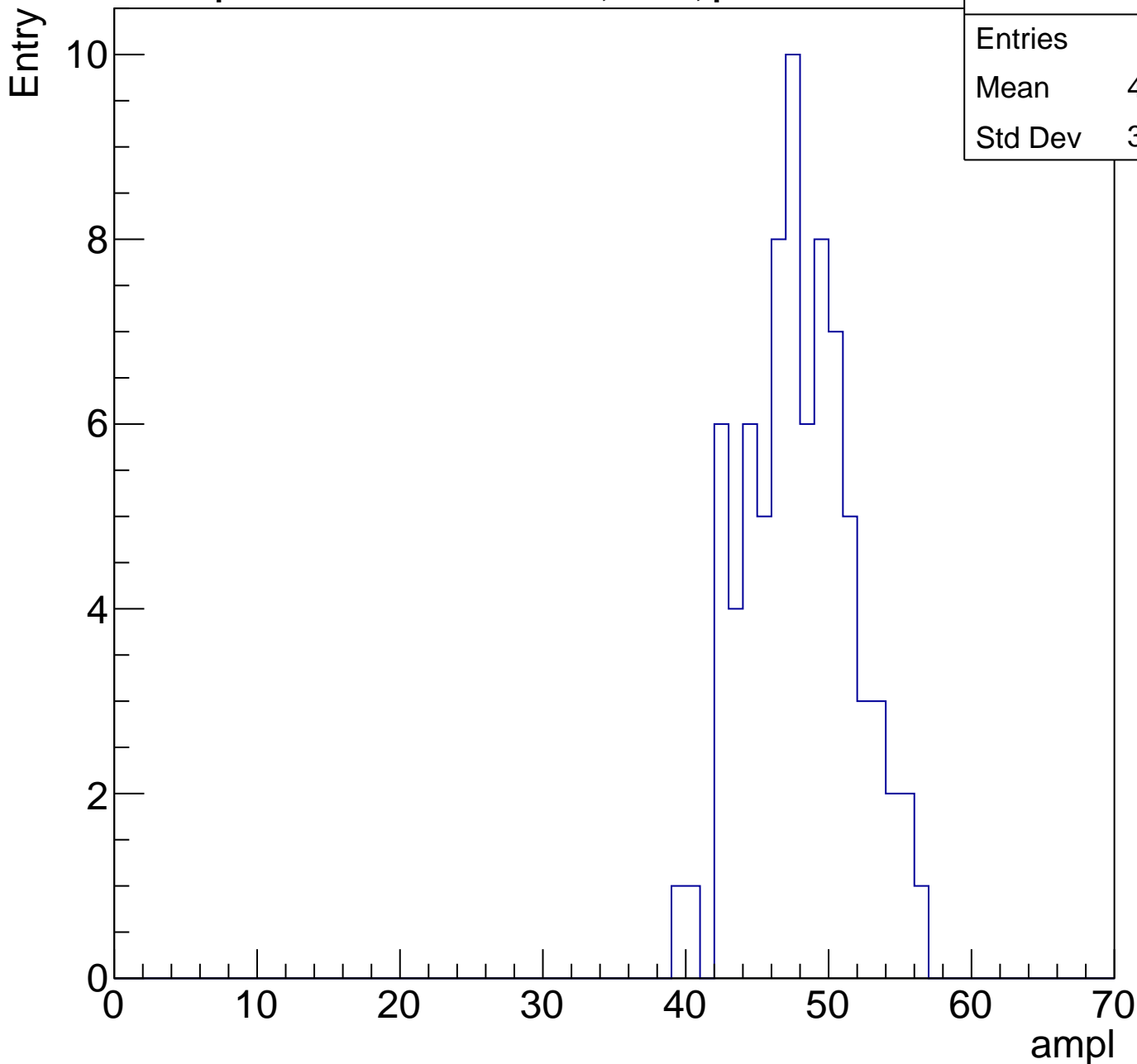
**Gaus Width: 3.0320**



# B1L103S, U1-ch57, adc3

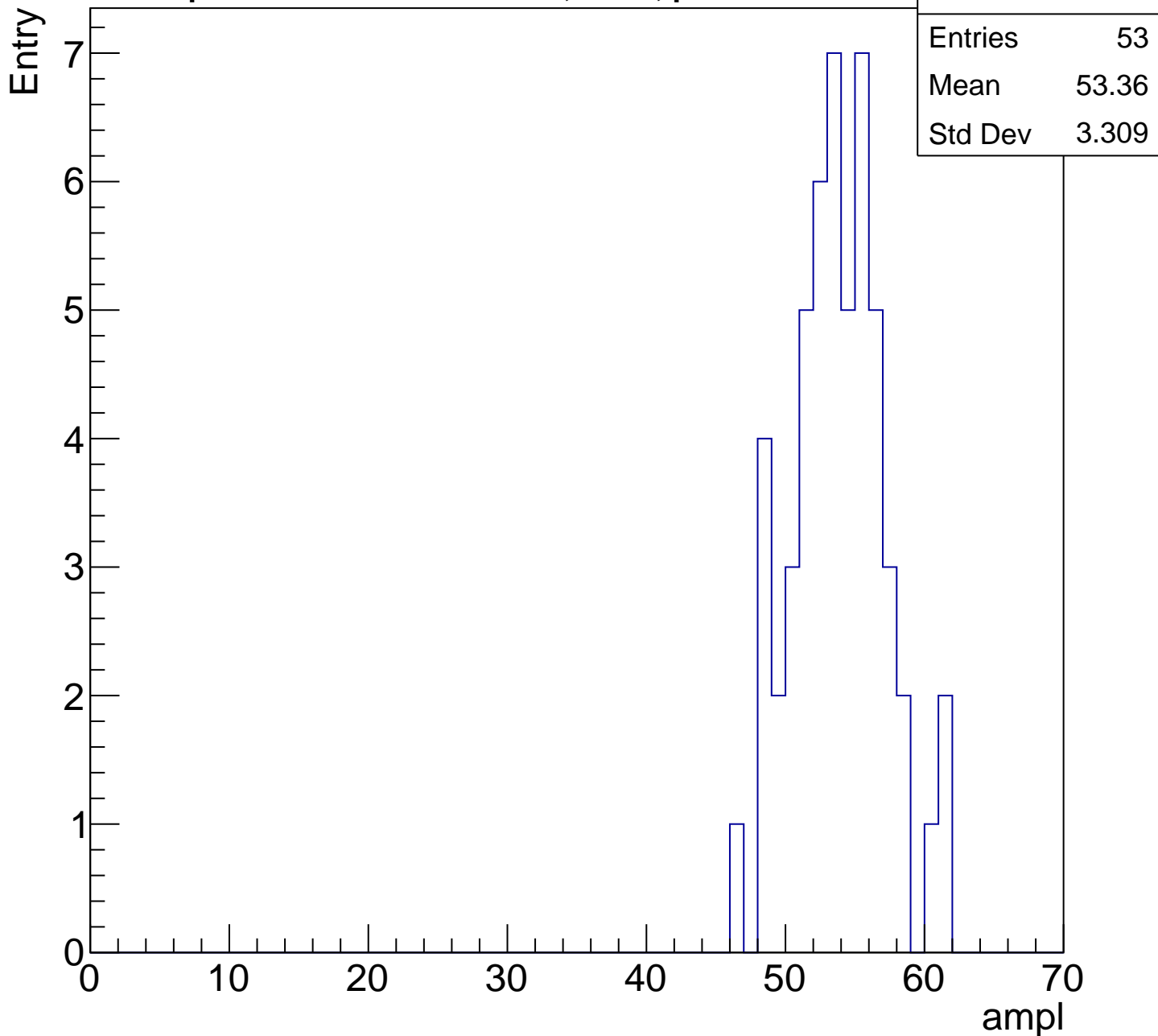
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	78
Mean	47.49
Std Dev	3.689



# B1L103S, U1-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

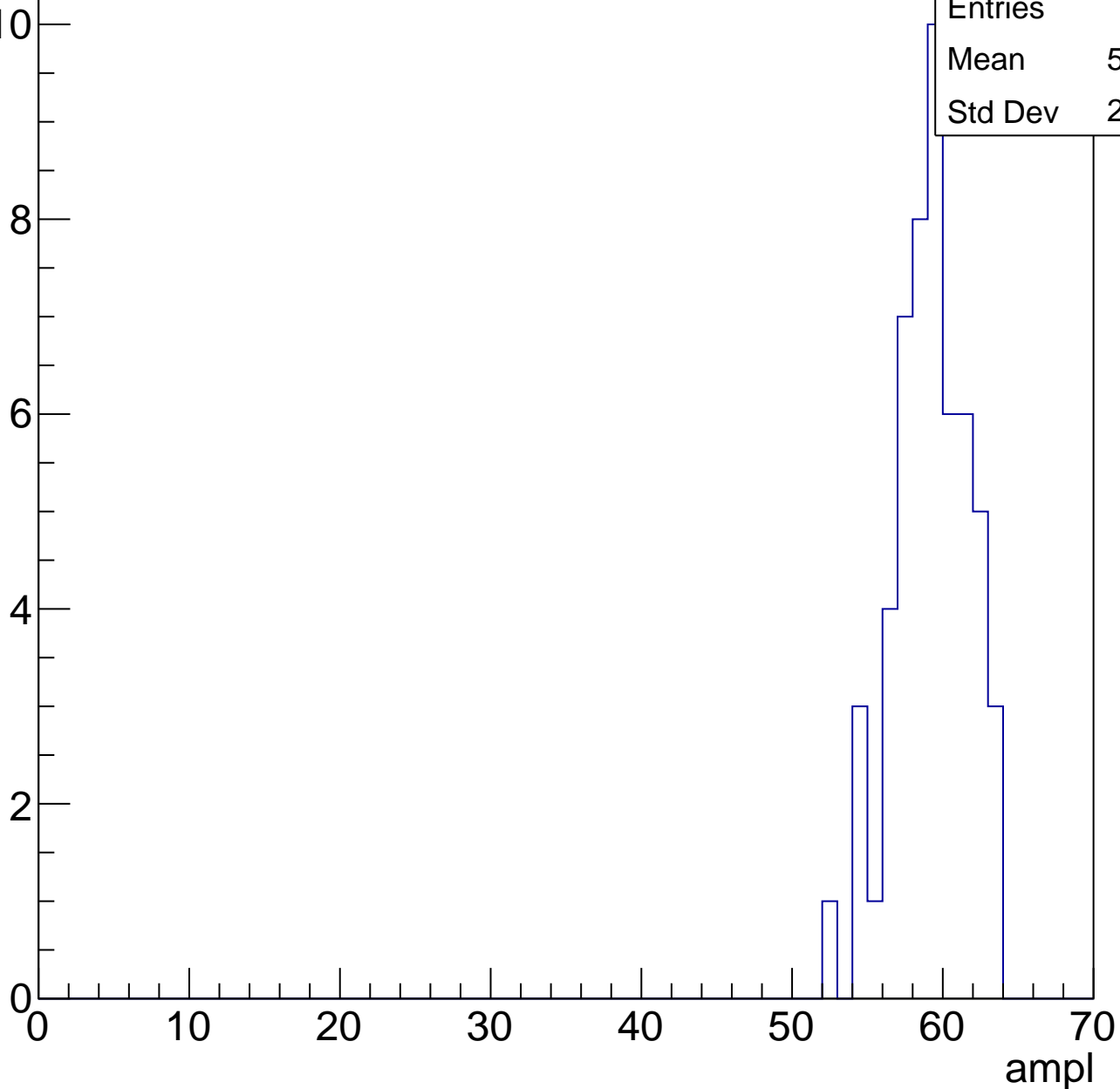


# B1L103S, U1-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

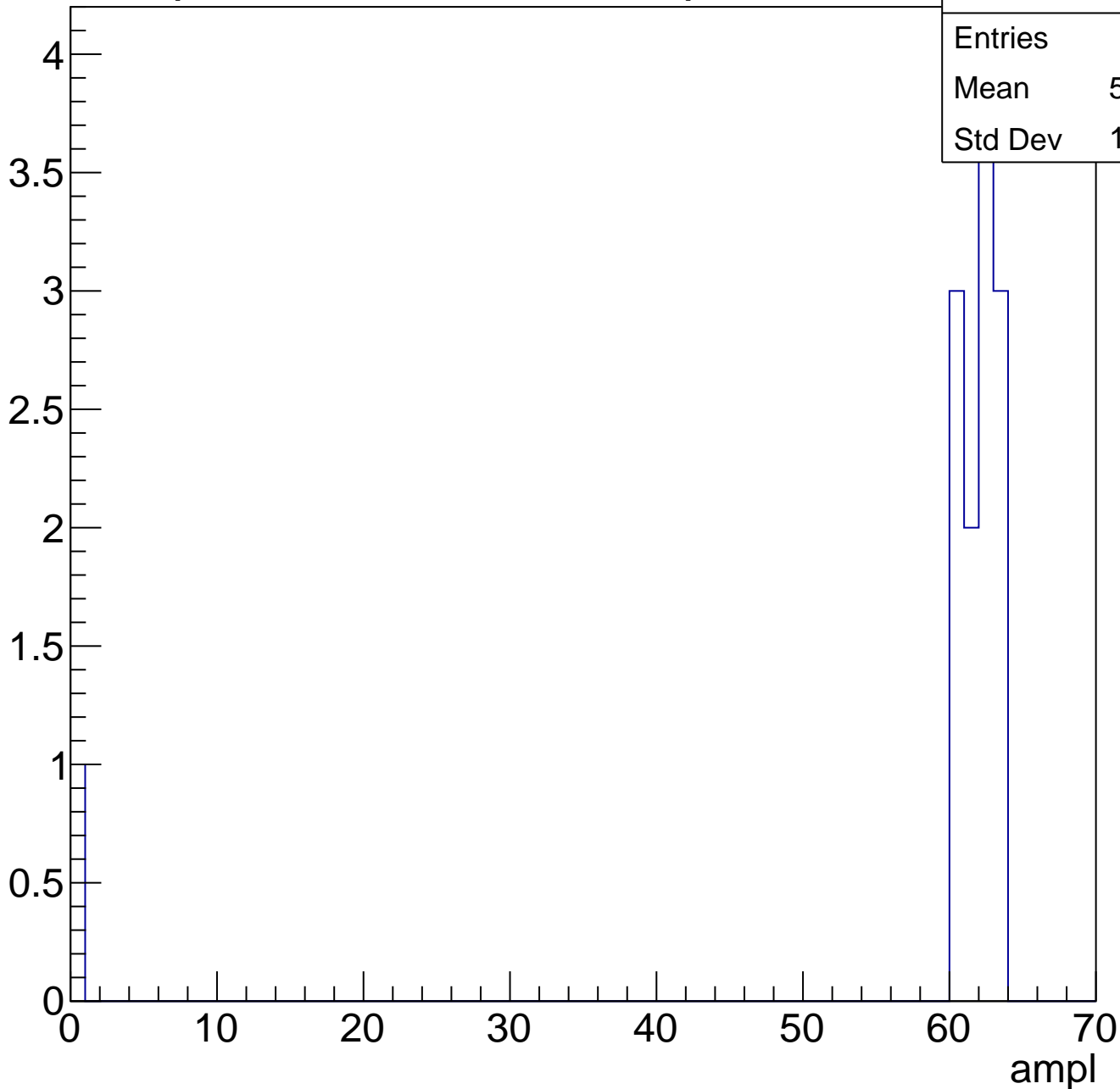
Entries	54
Mean	58.72
Std Dev	2.475



# B1L103S, U1-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

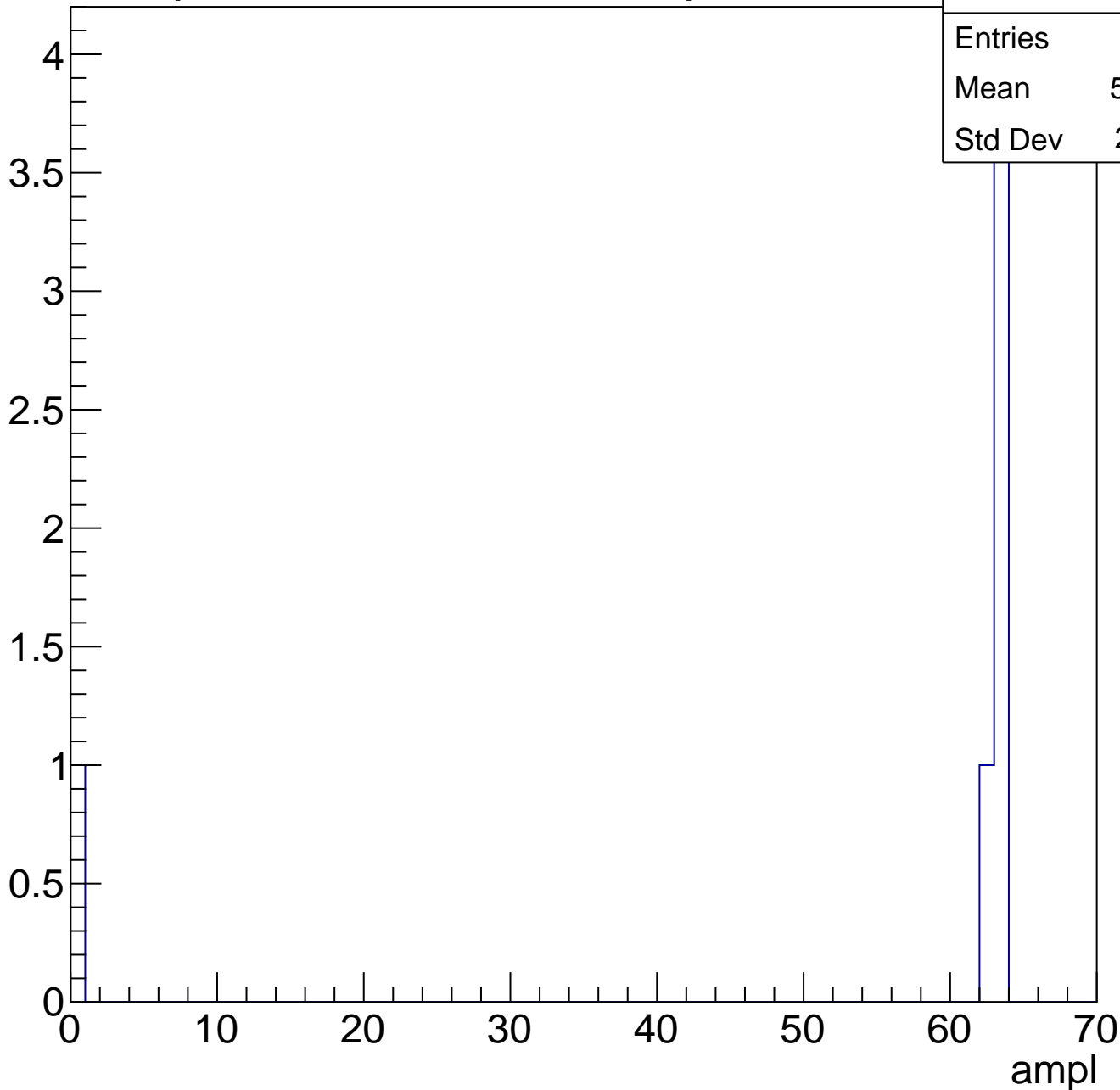




# B1L103S, U1-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch58, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	74
Mean	27.43
Std Dev	3.587

**Gaus mean : 28.0125**

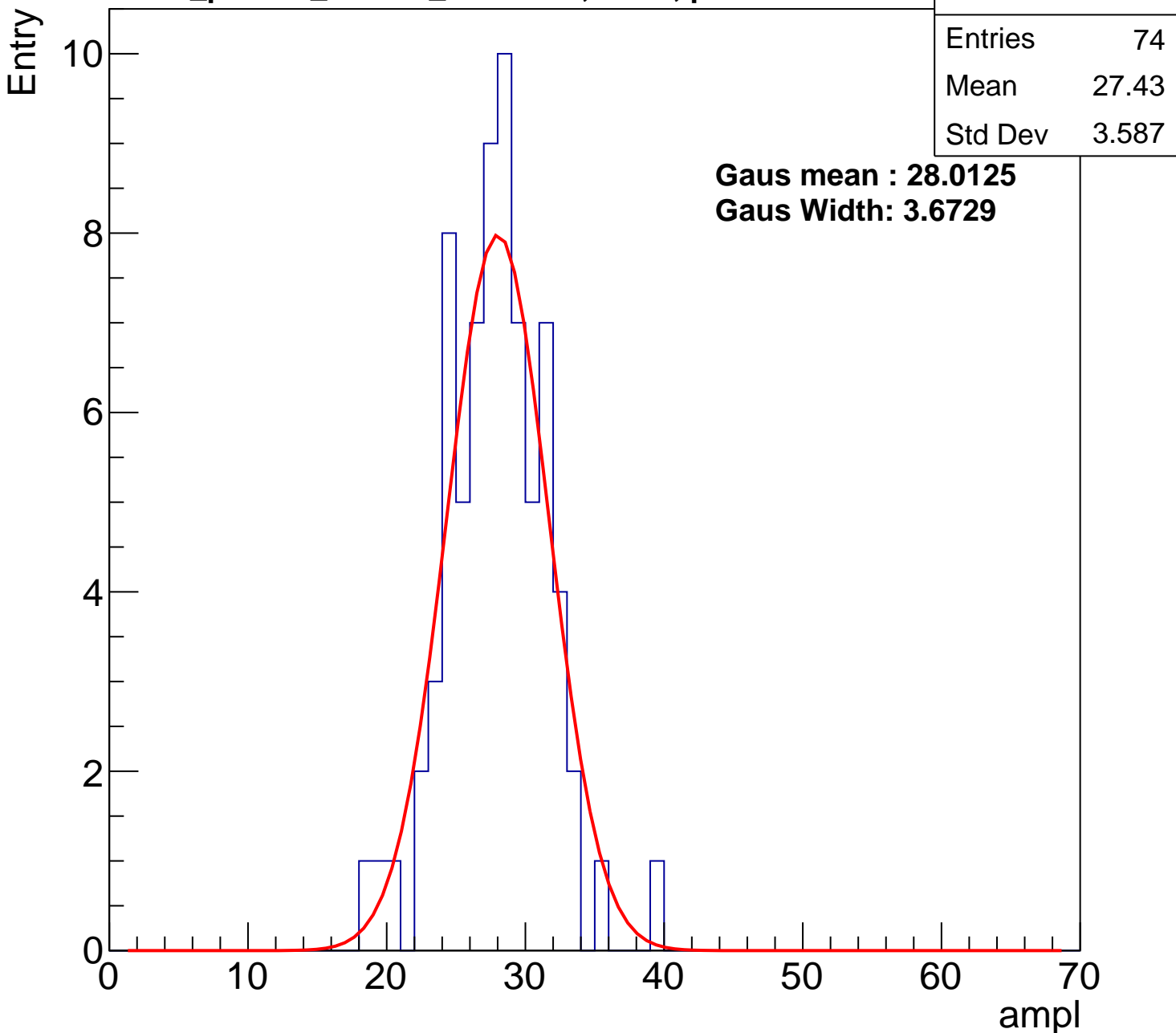
**Gaus Width: 3.6729**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U1-ch58, adc1

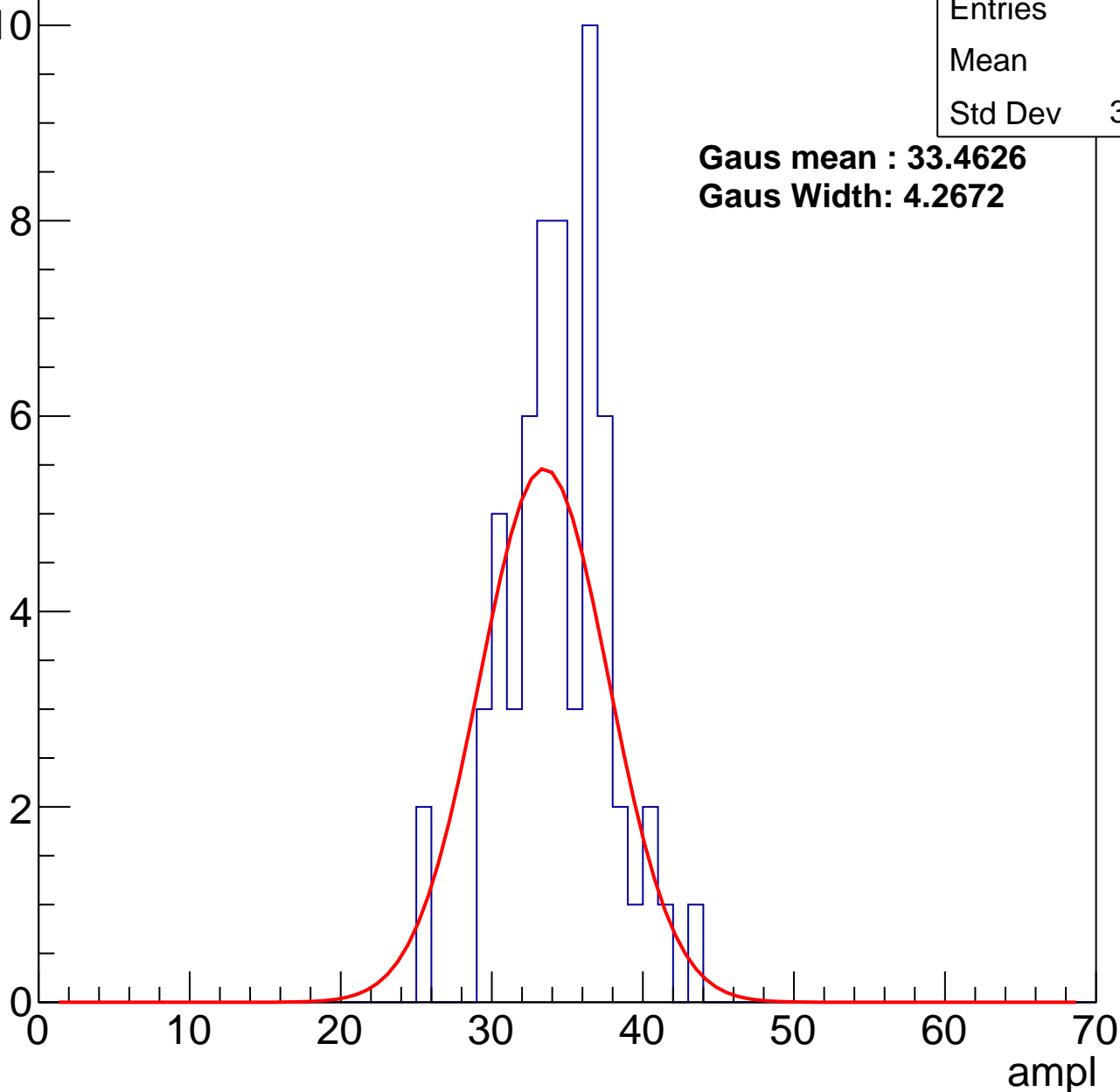
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	34
Std Dev	3.464

**Gaus mean : 33.4626**

**Gaus Width: 4.2672**



# B1L103S, U1-ch58, adc2

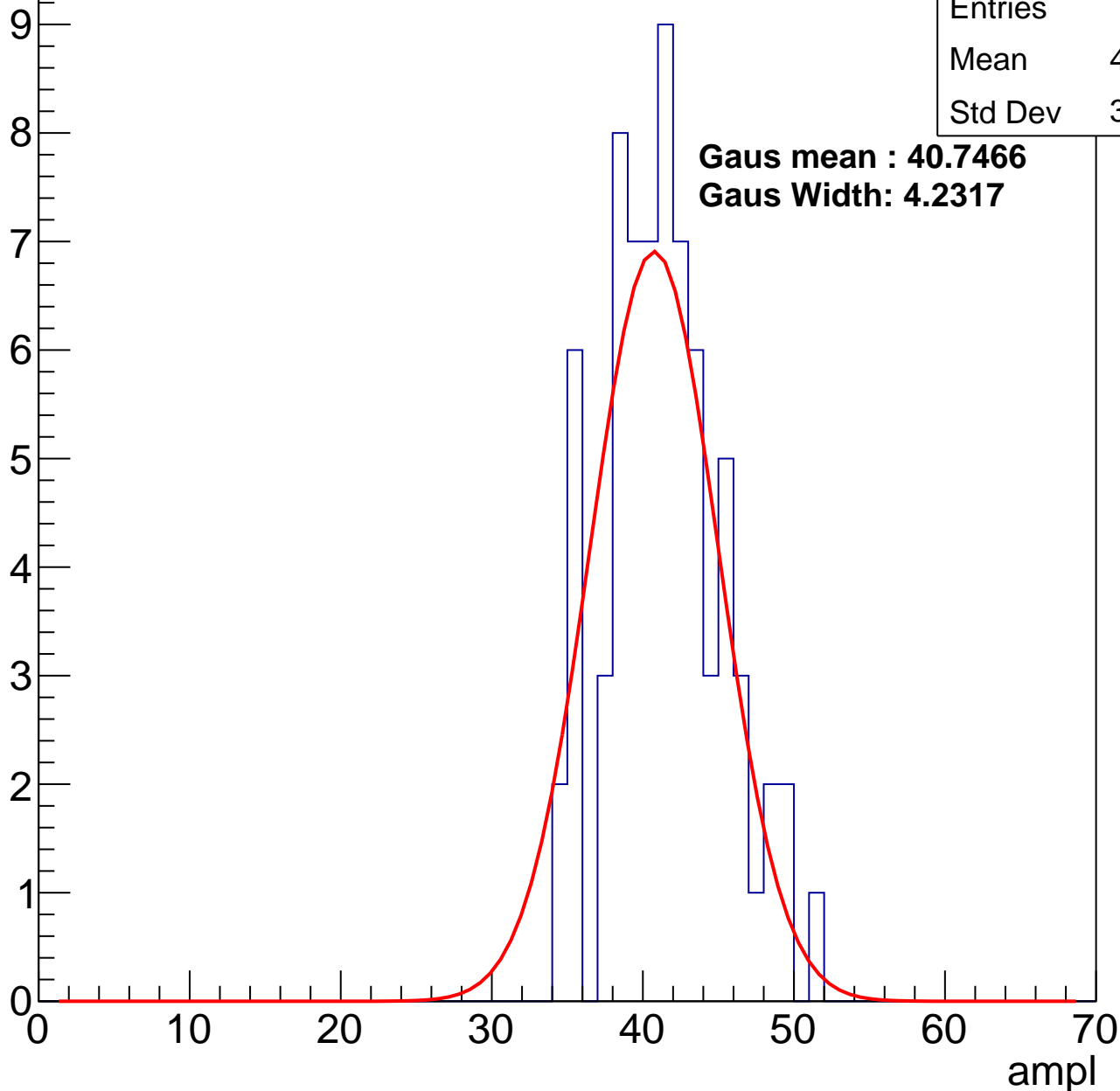
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	41.03
Std Dev	3.808

**Gaus mean : 40.7466**

**Gaus Width: 4.2317**

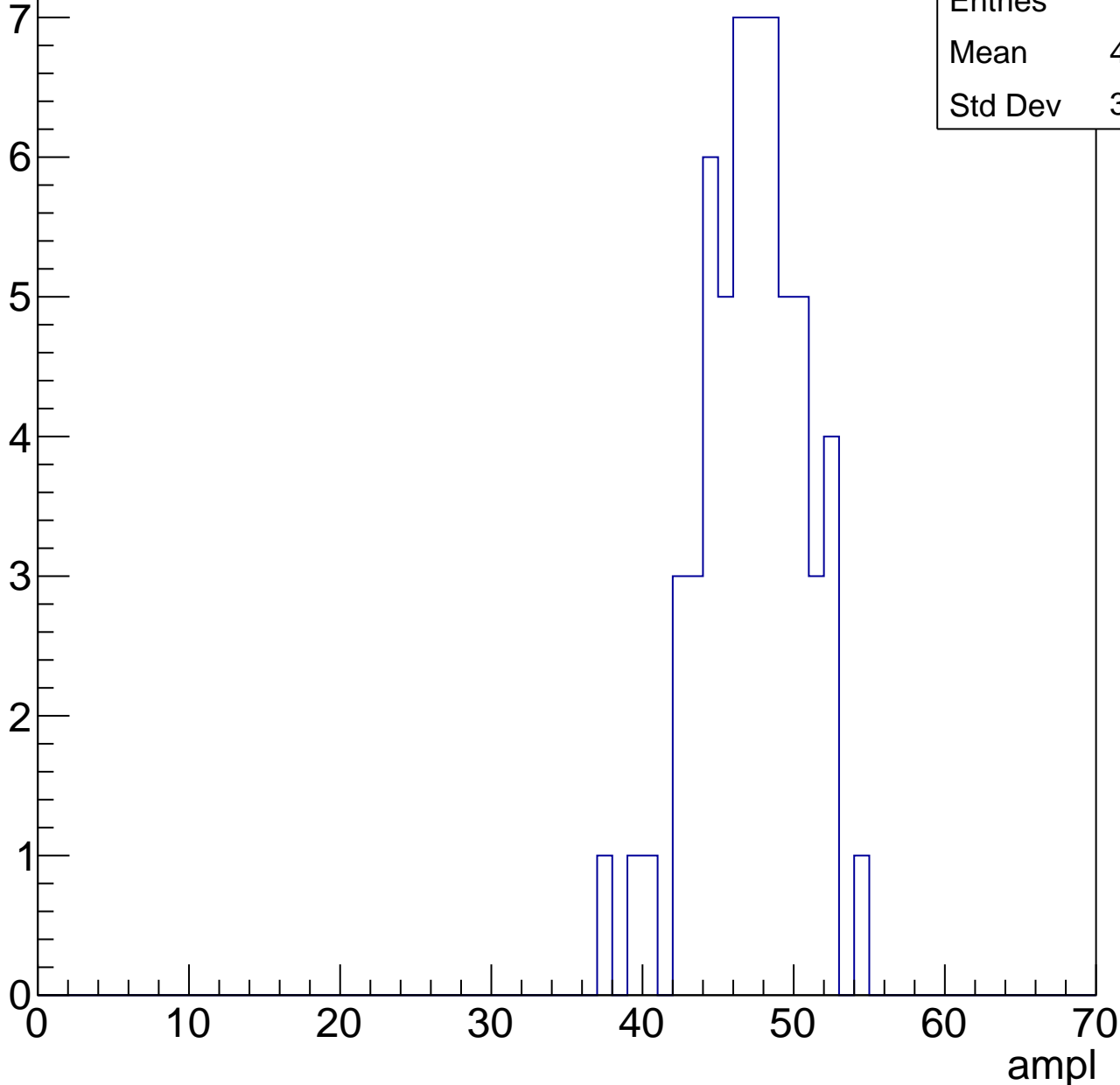


# B1L103S, U1-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

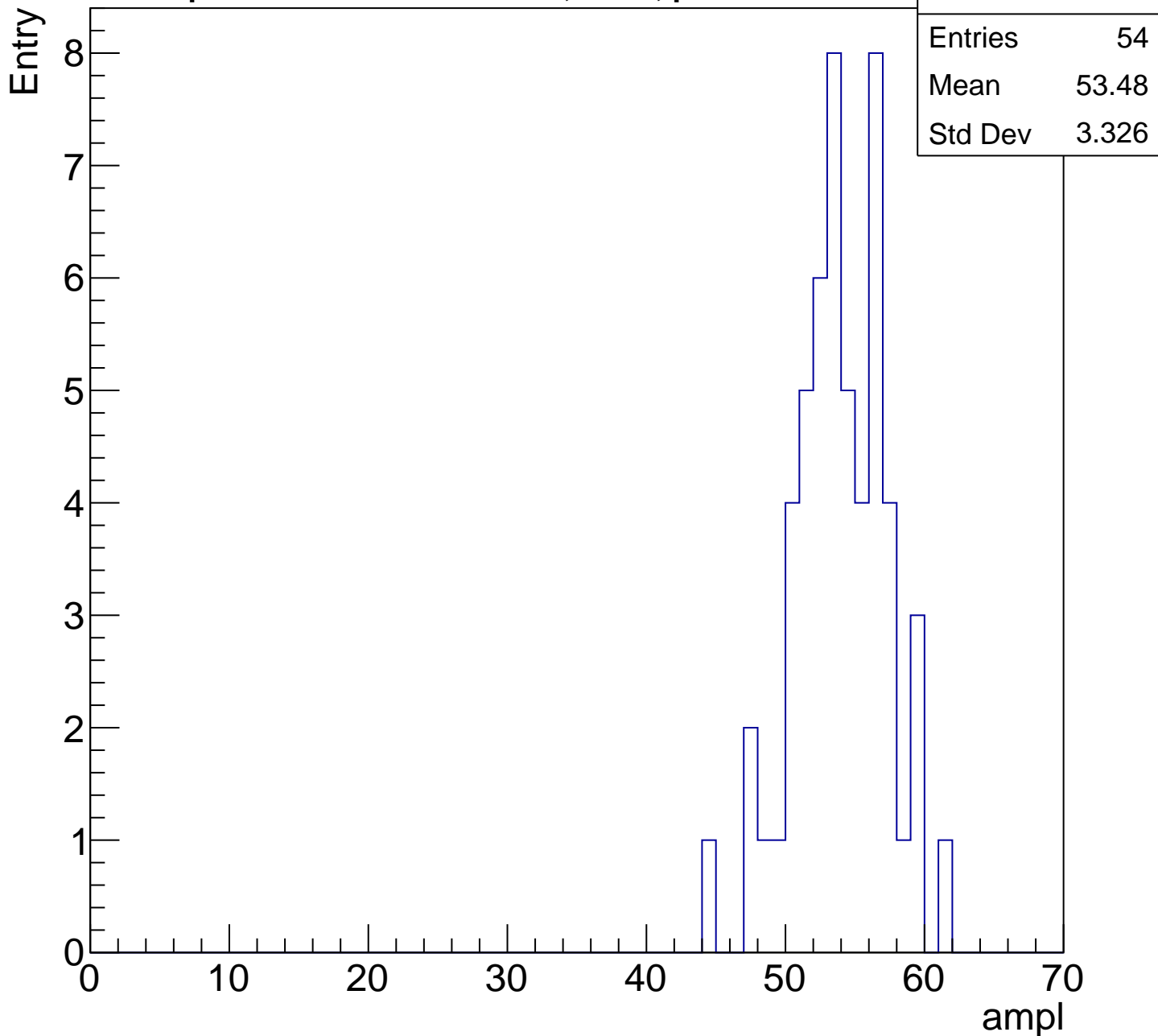
Entry

Entries	59
Mean	46.73
Std Dev	3.399



# B1L103S, U1-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

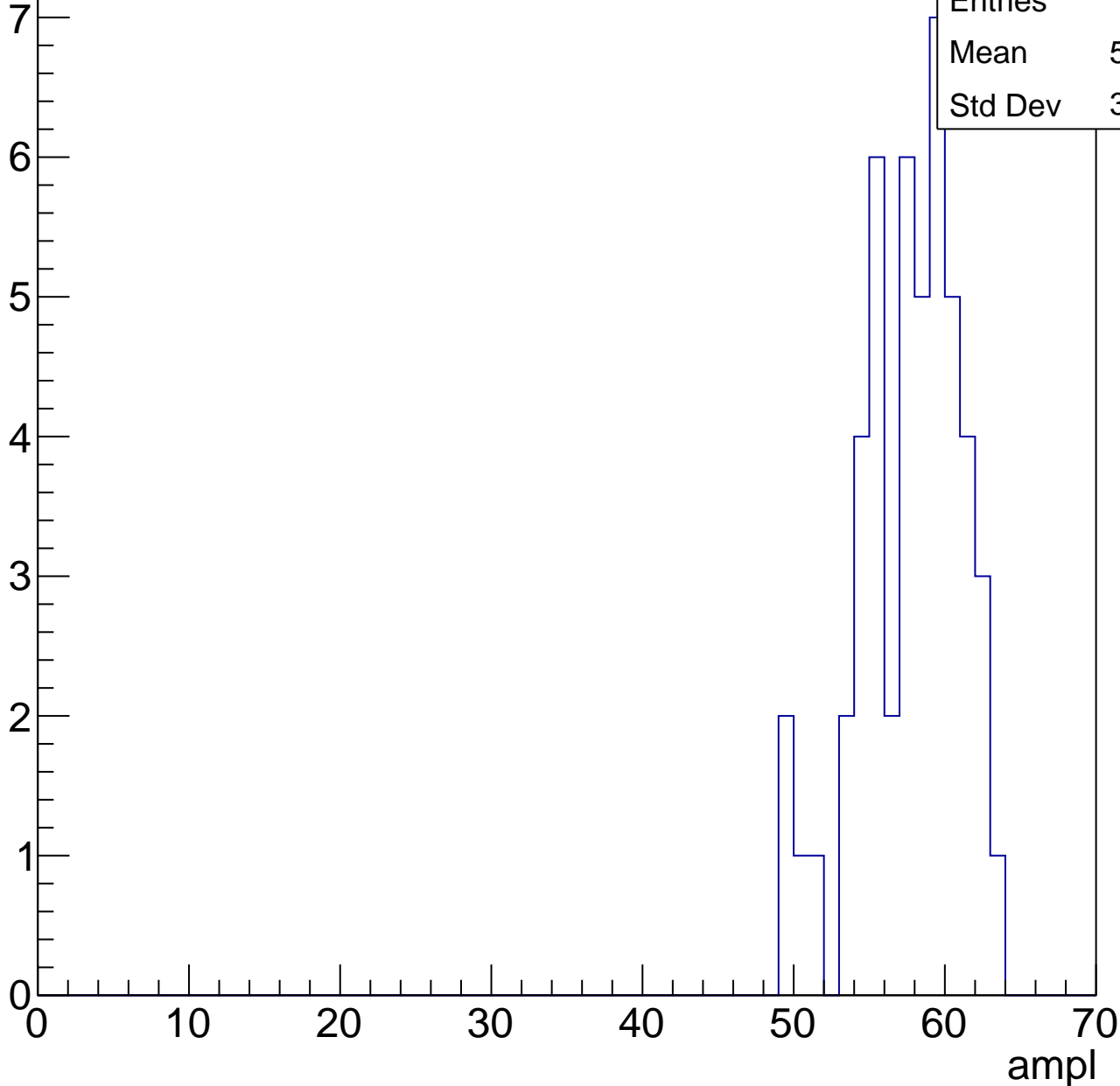


# B1L103S, U1-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	57.16
Std Dev	3.377

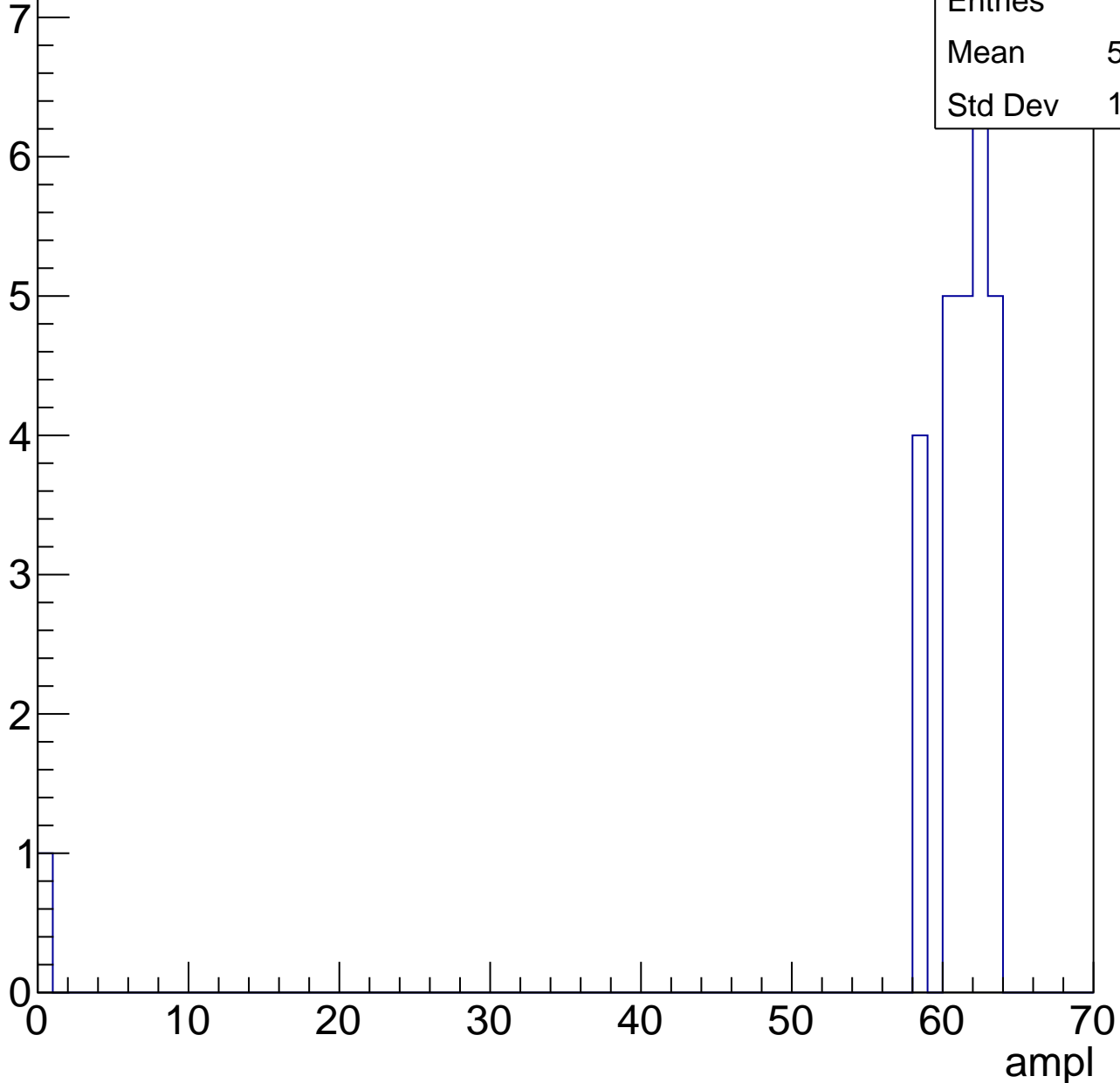


# B1L103S, U1-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	27
Mean	58.74
Std Dev	11.63

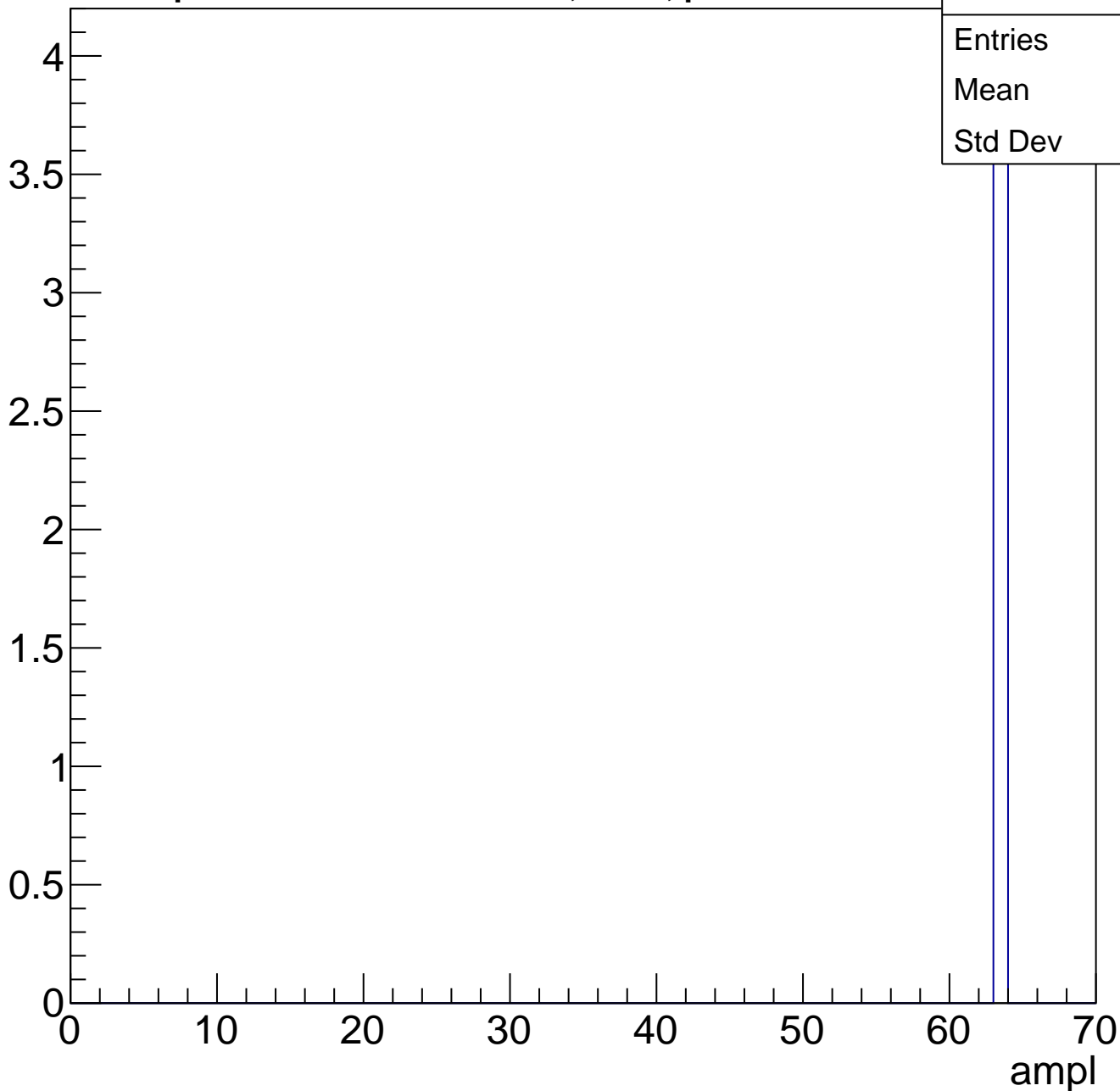




# B1L103S, U1-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch59, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	70
Mean	27.54
Std Dev	4.927

**Gaus mean : 28.0049**

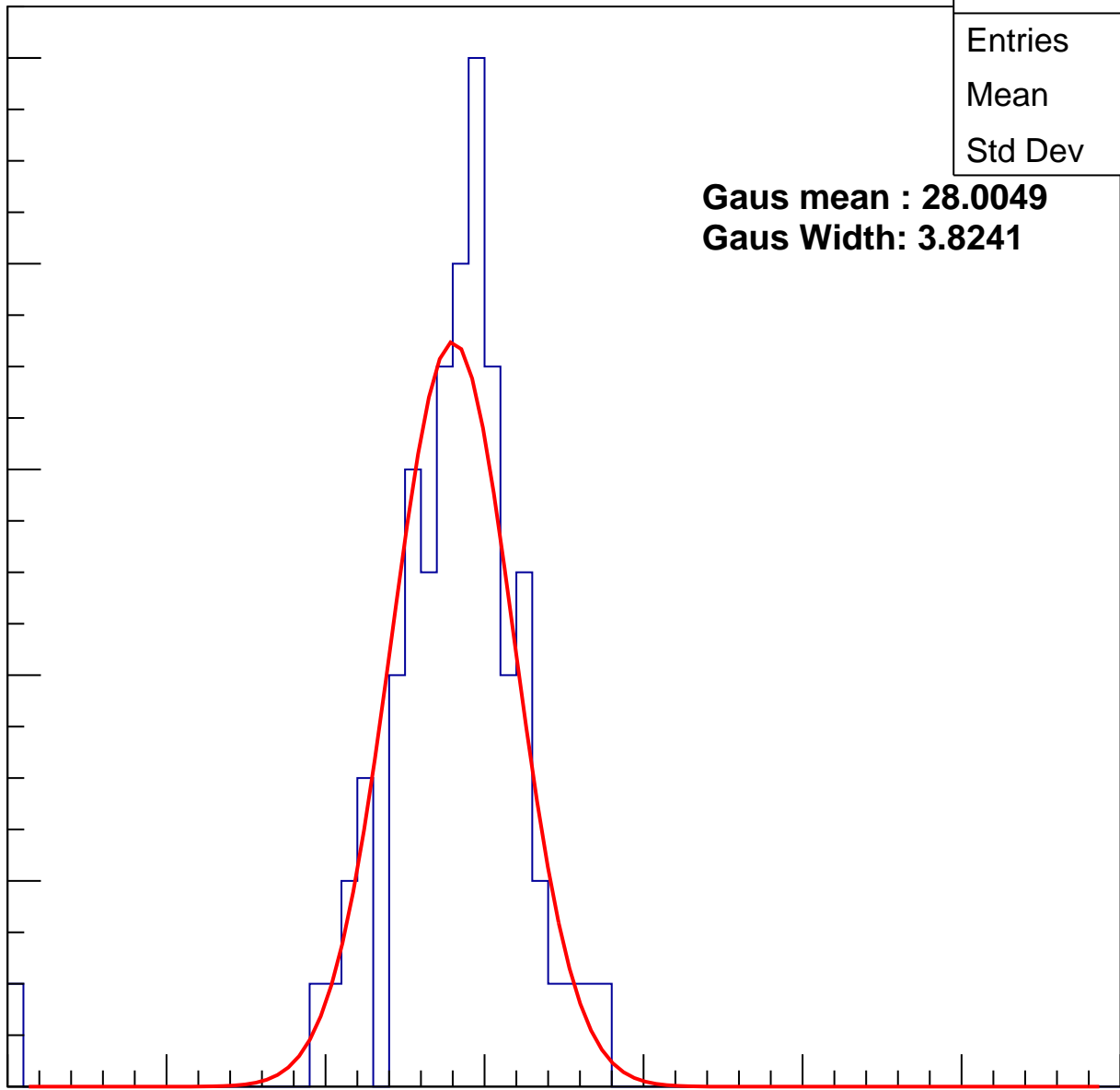
**Gaus Width: 3.8241**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U1-ch59, adc1

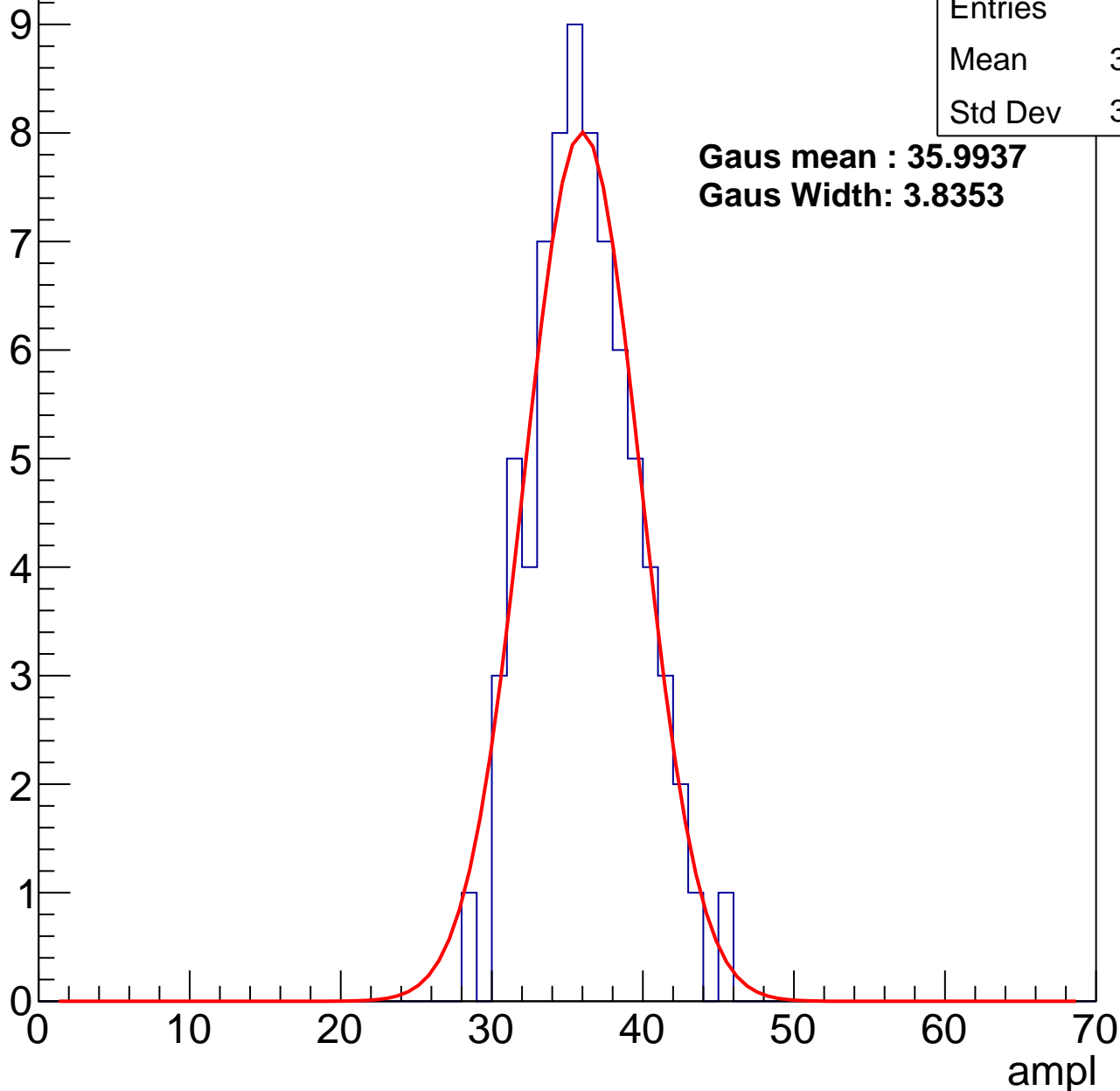
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	35.73
Std Dev	3.442

**Gaus mean : 35.9937**

**Gaus Width: 3.8353**



# B1L103S, U1-ch59, adc2

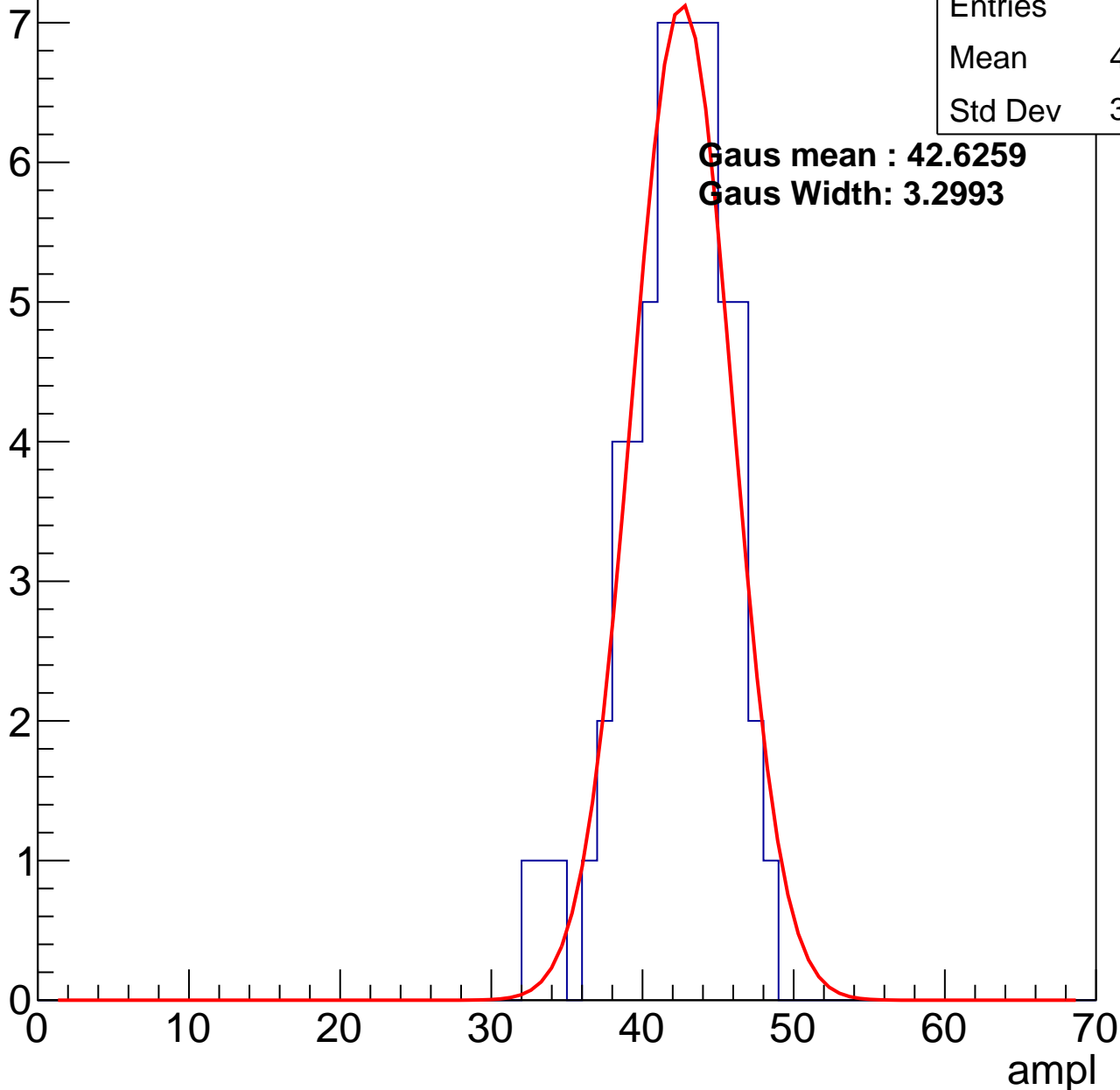
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	41.73
Std Dev	3.415

**Gaus mean : 42.6259**

**Gaus Width: 3.2993**



# B1L103S, U1-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

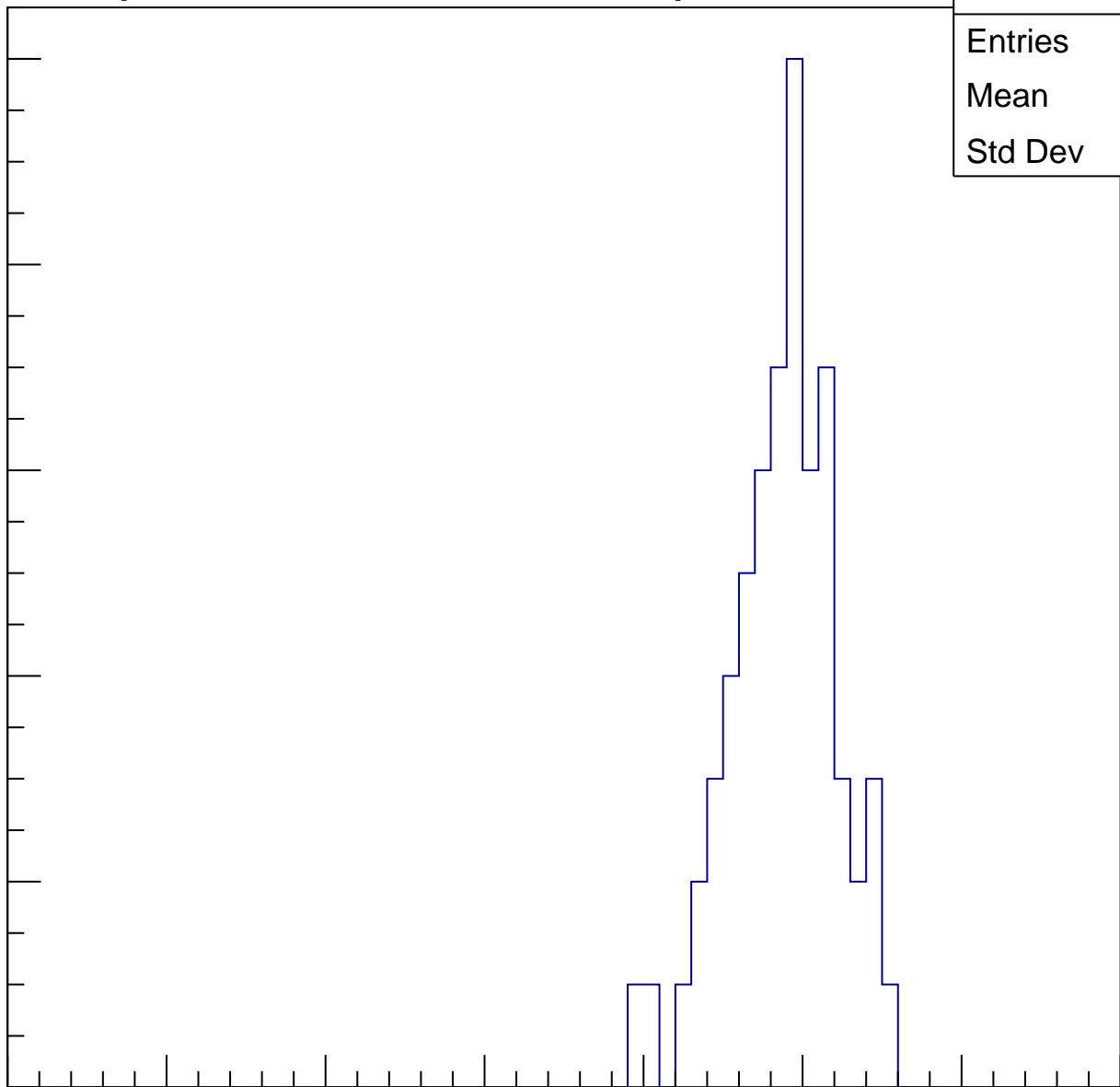
Entries	62
Mean	48.27
Std Dev	3.332

Entry

10  
8  
6  
4  
2  
0

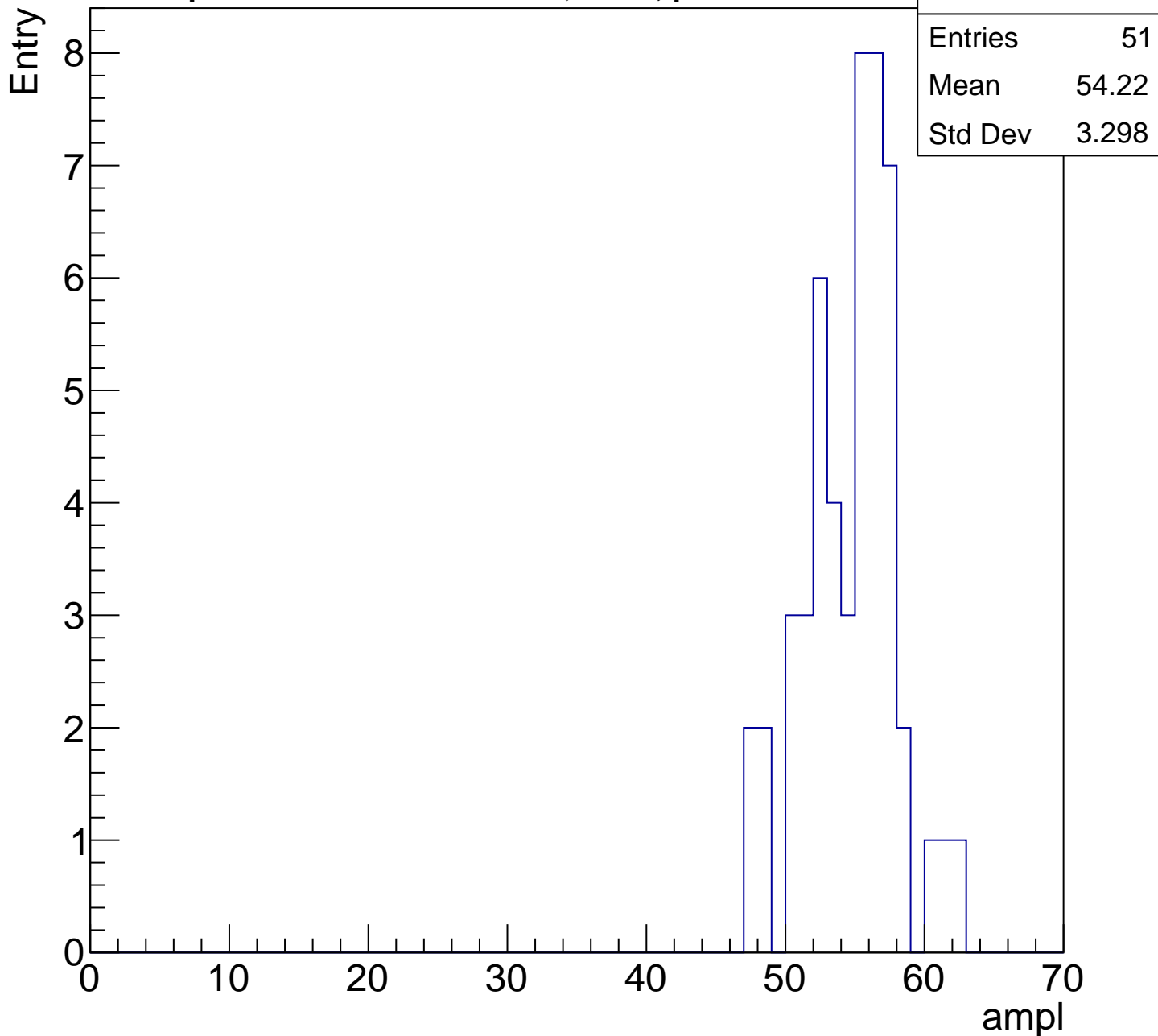
0 10 20 30 40 50 60 70

ampl



# B1L103S, U1-ch59, adc4

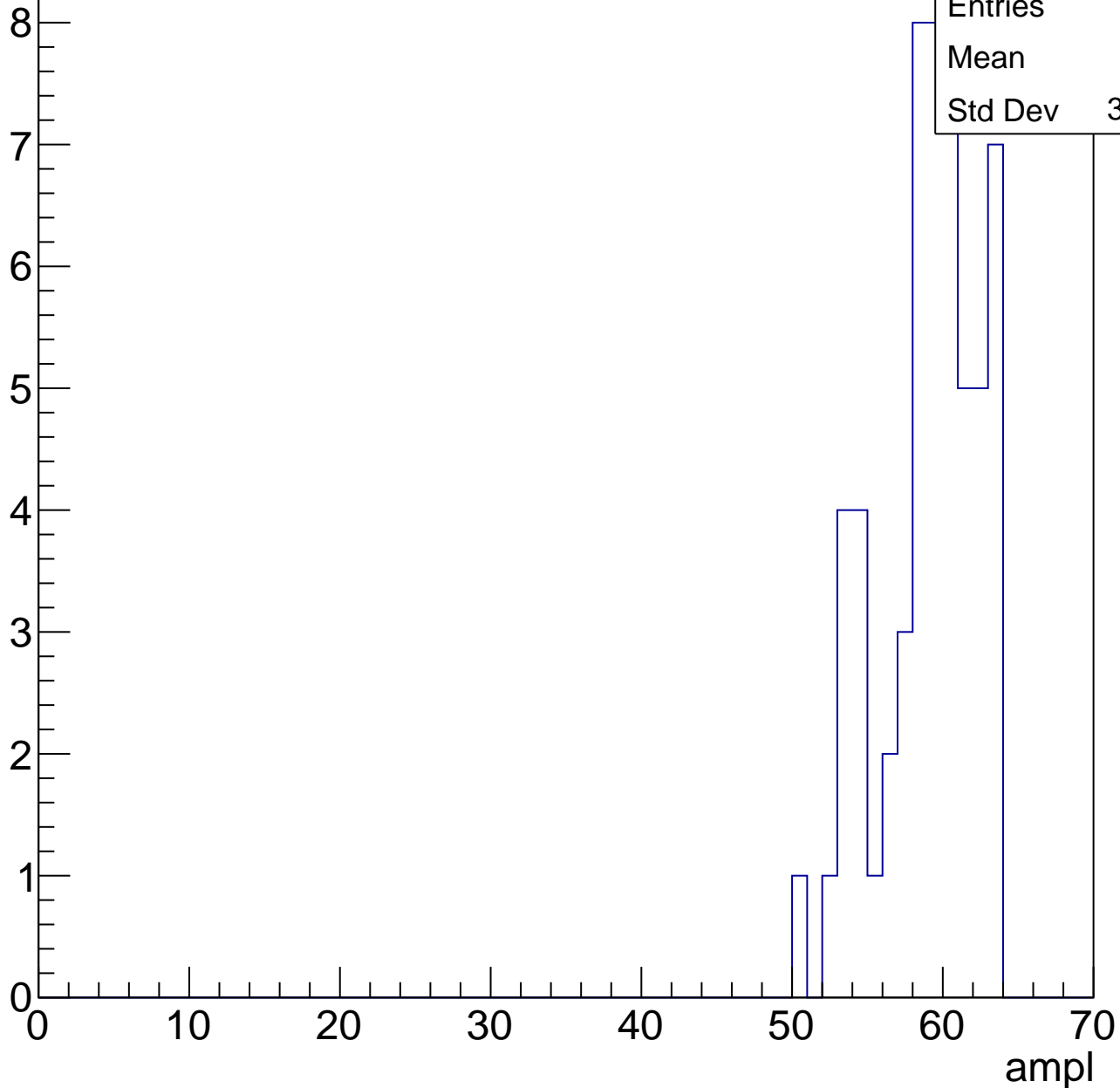
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U1-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

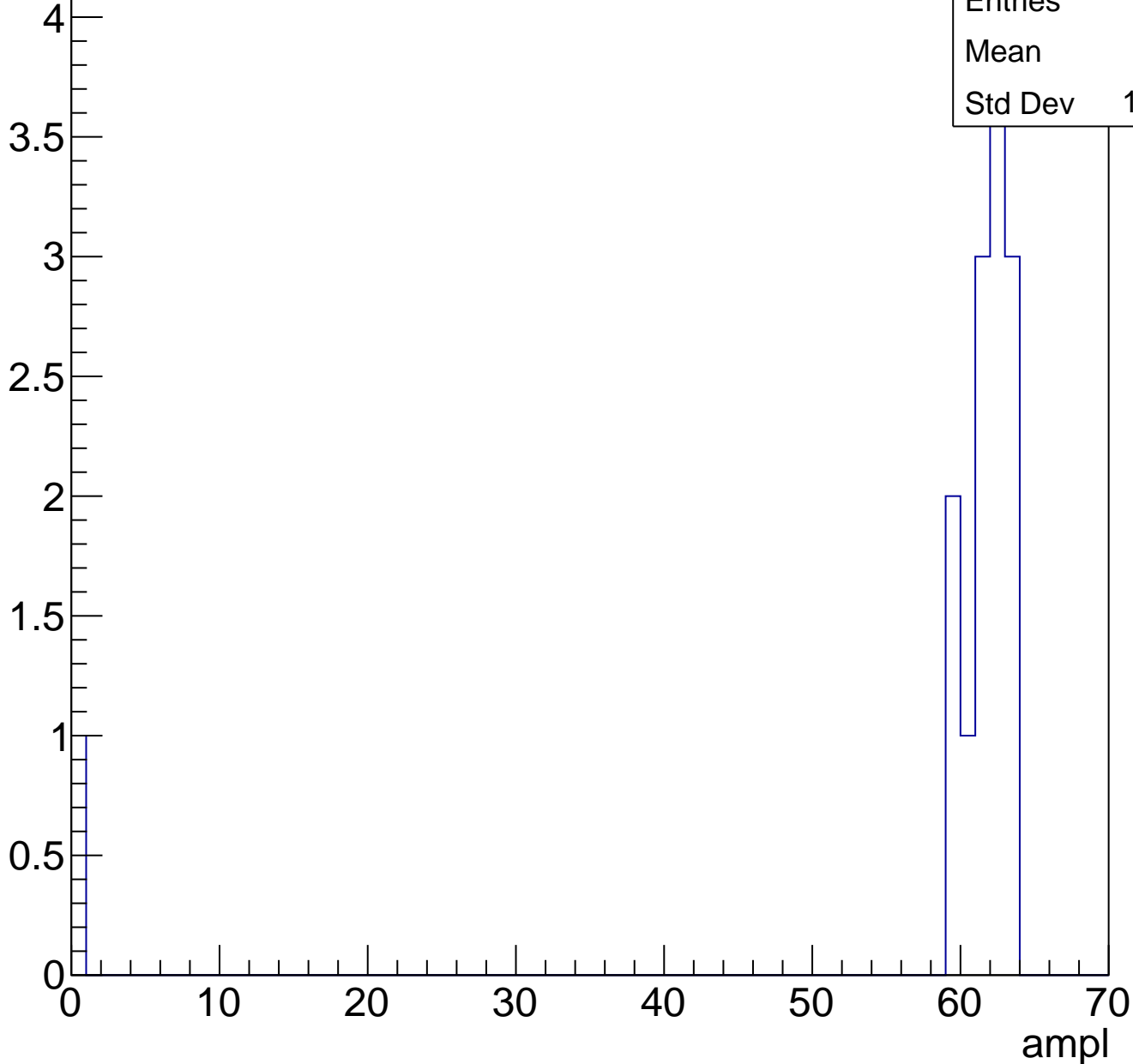


Entries	57
Mean	58.6
Std Dev	3.254

# B1L103S, U1-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U1-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch60, adc0

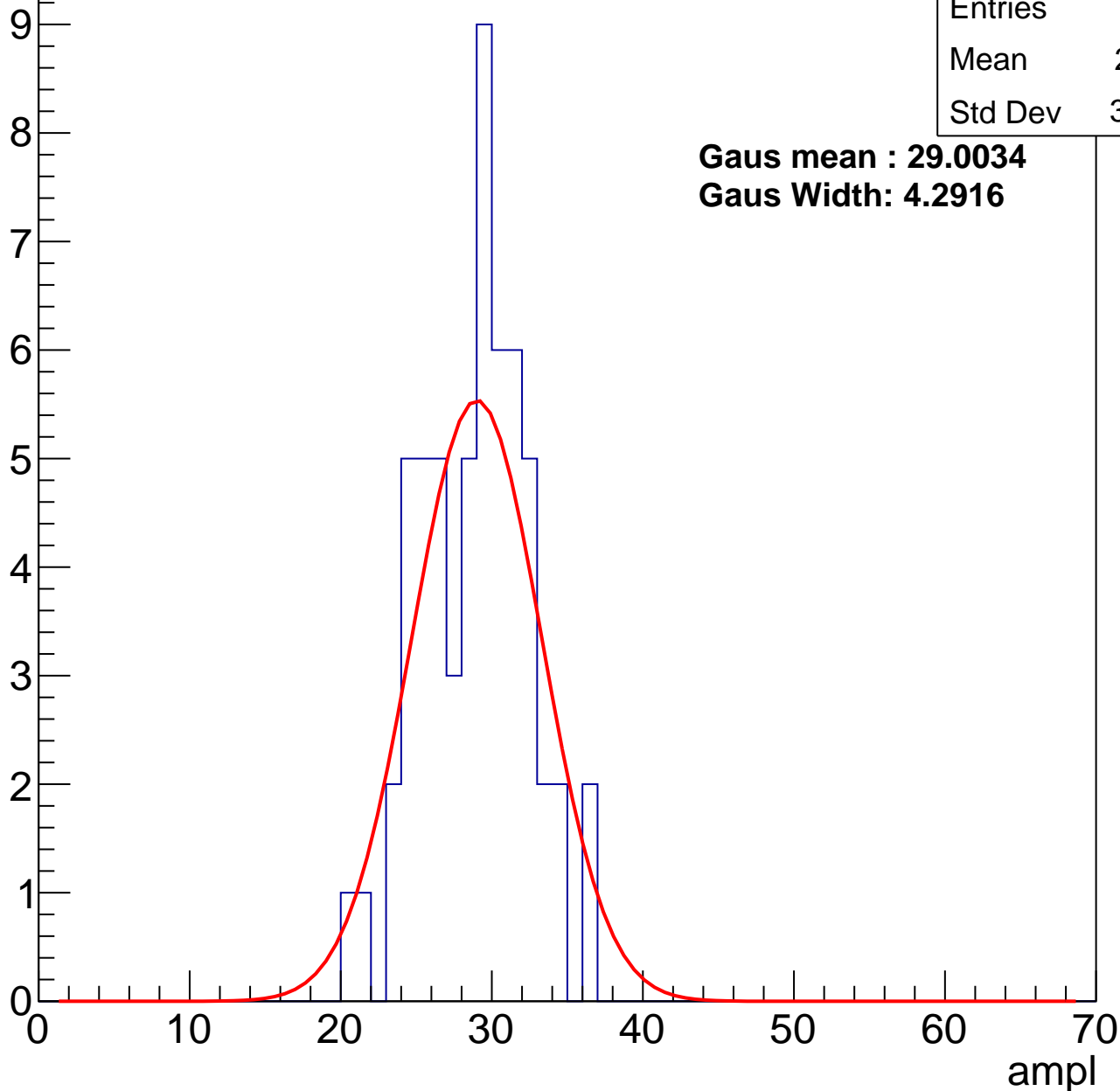
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	28.41
Std Dev	3.489

**Gaus mean : 29.0034**

**Gaus Width: 4.2916**



# B1L103S, U1-ch60, adc1

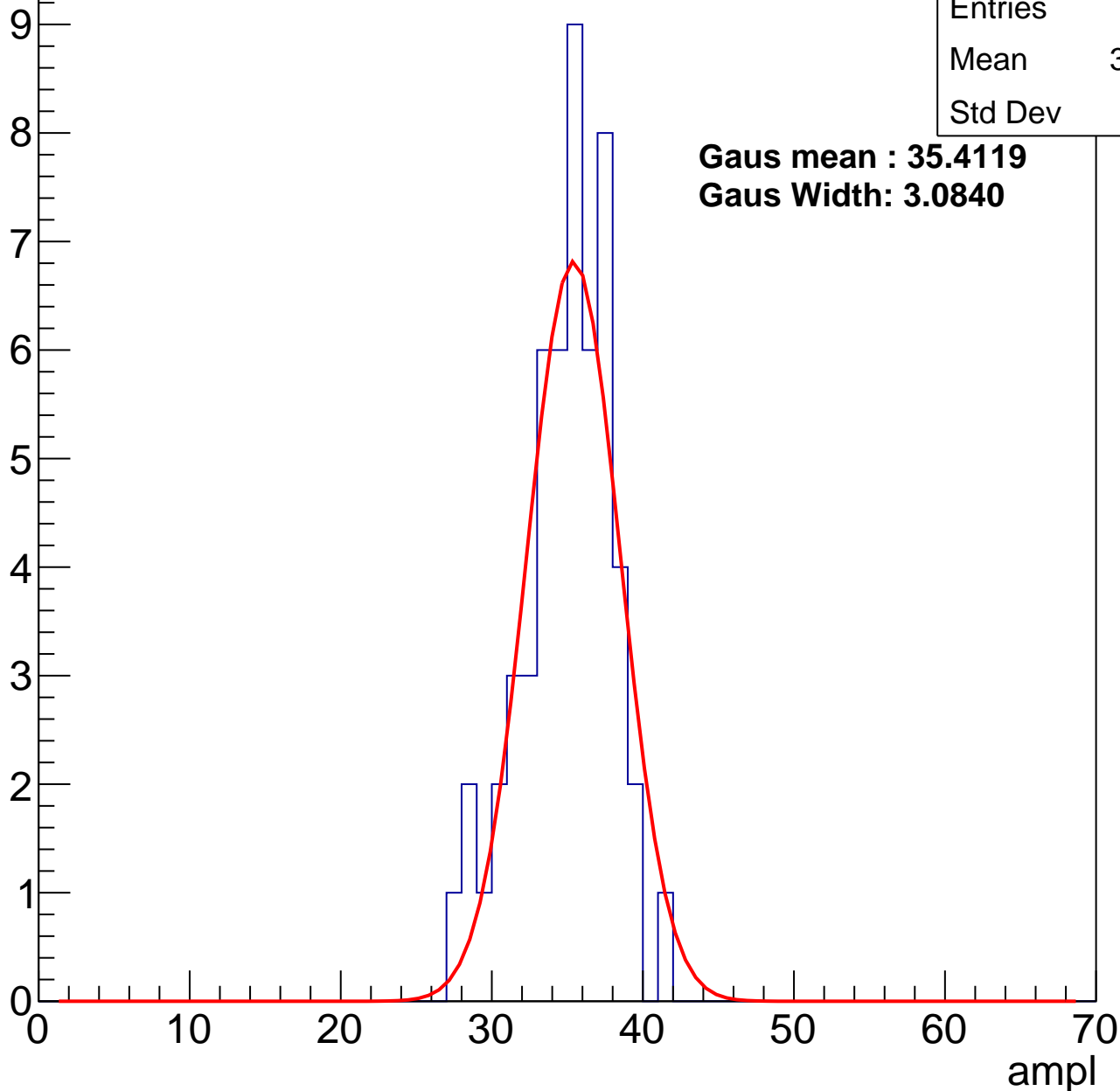
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	34.46
Std Dev	2.98

**Gaus mean : 35.4119**

**Gaus Width: 3.0840**



# B1L103S, U1-ch60, adc2

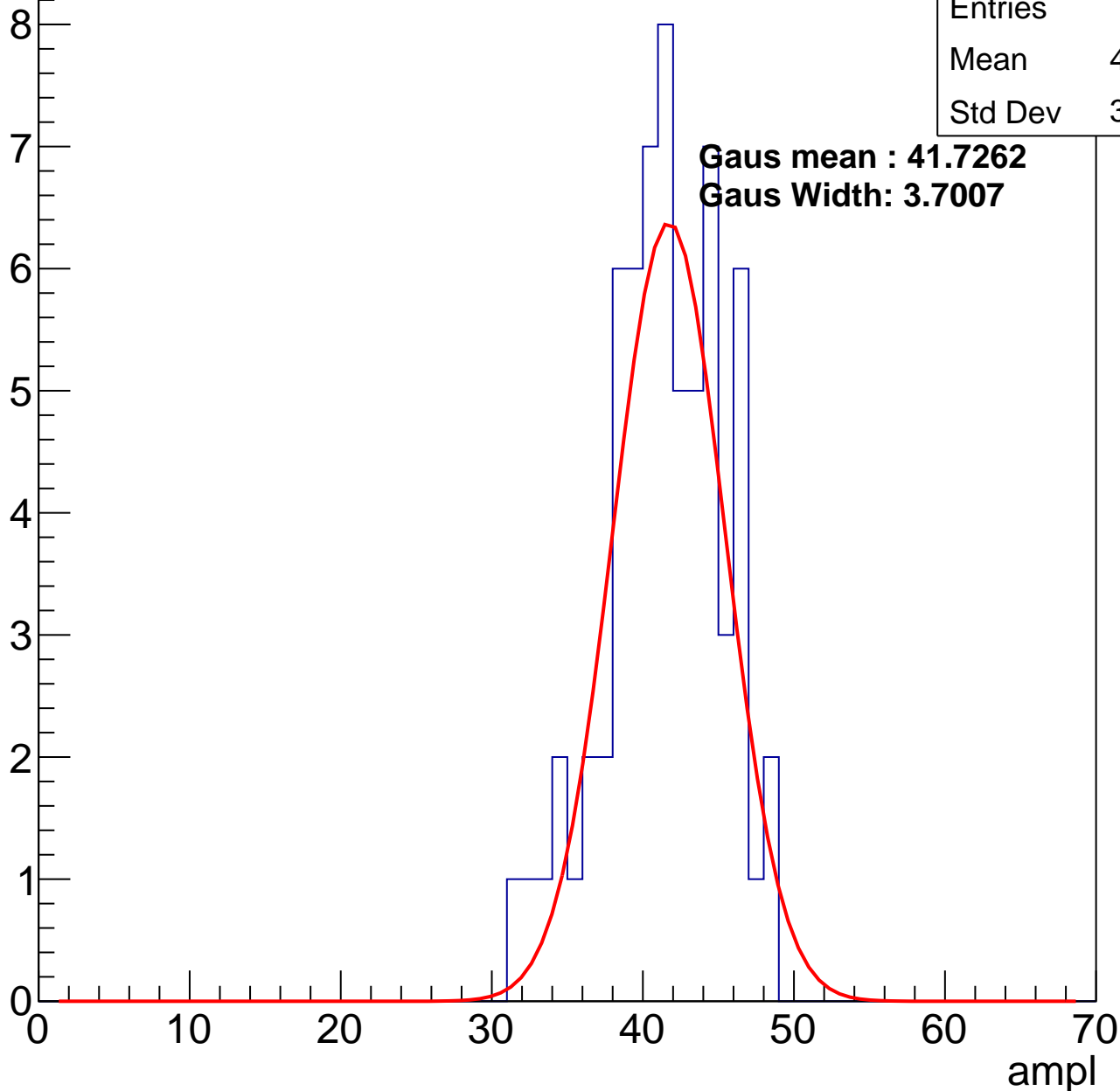
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	40.94
Std Dev	3.825

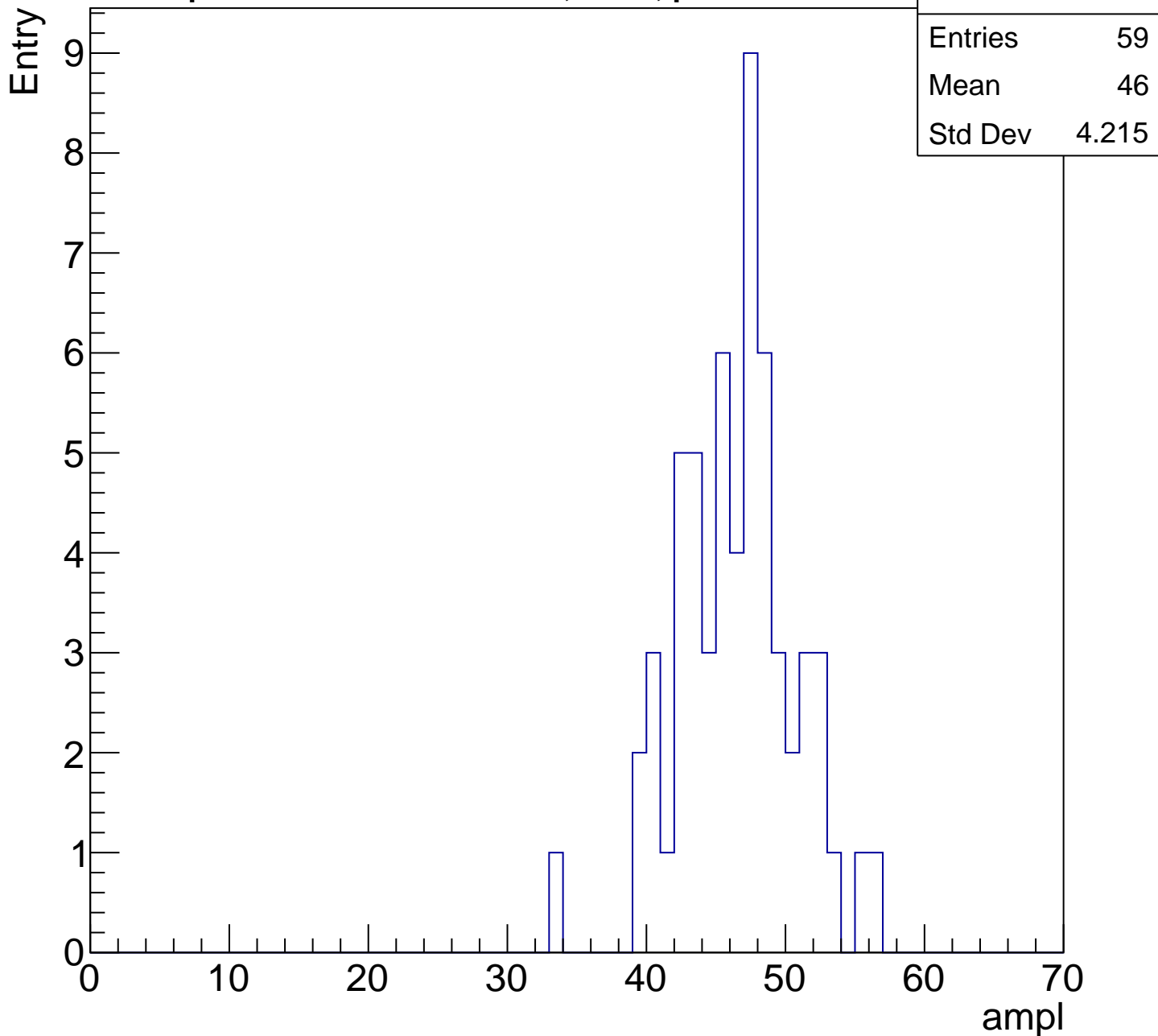
**Gaus mean : 41.7262**

**Gaus Width: 3.7007**



# B1L103S, U1-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

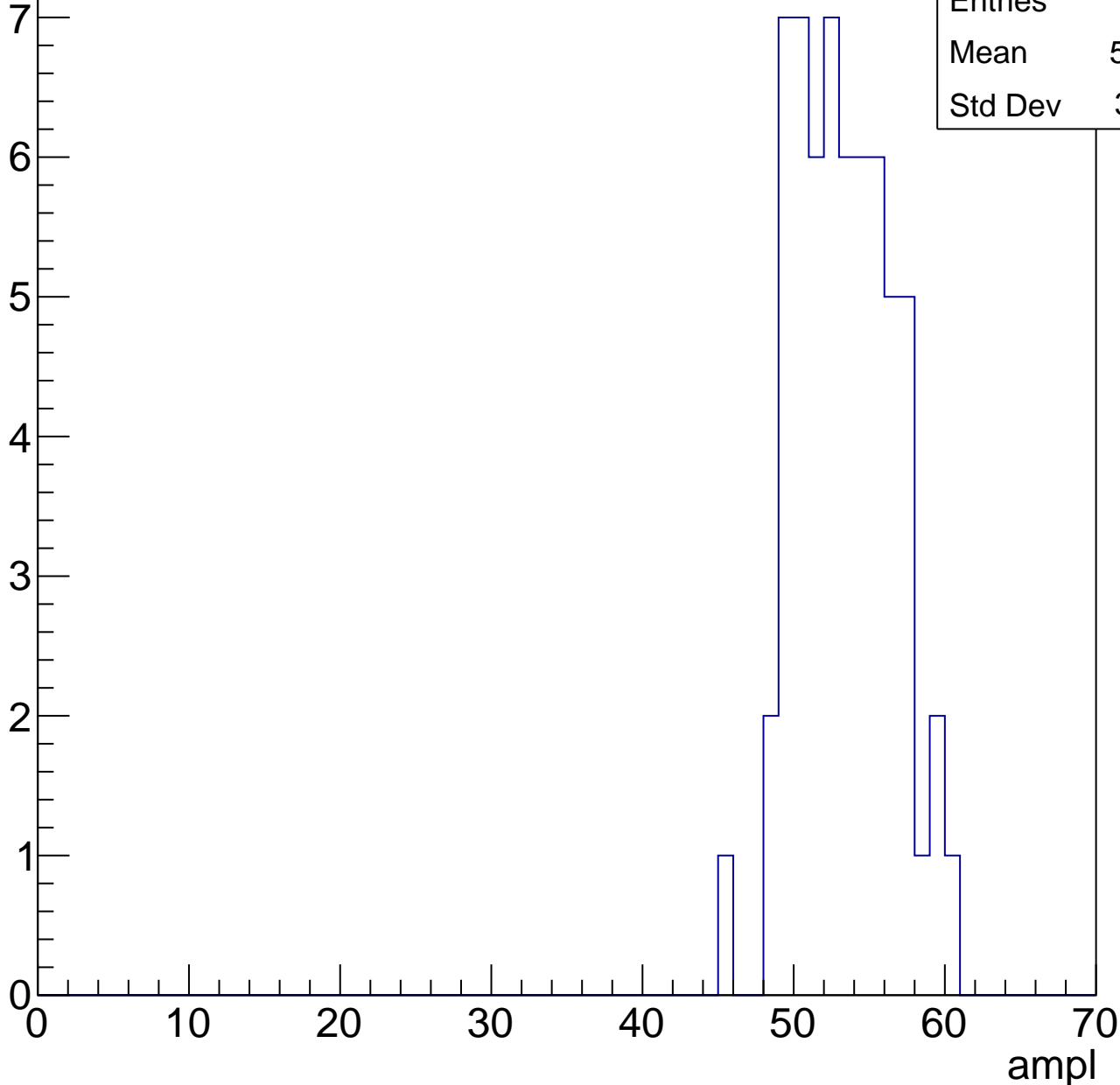


# B1L103S, U1-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

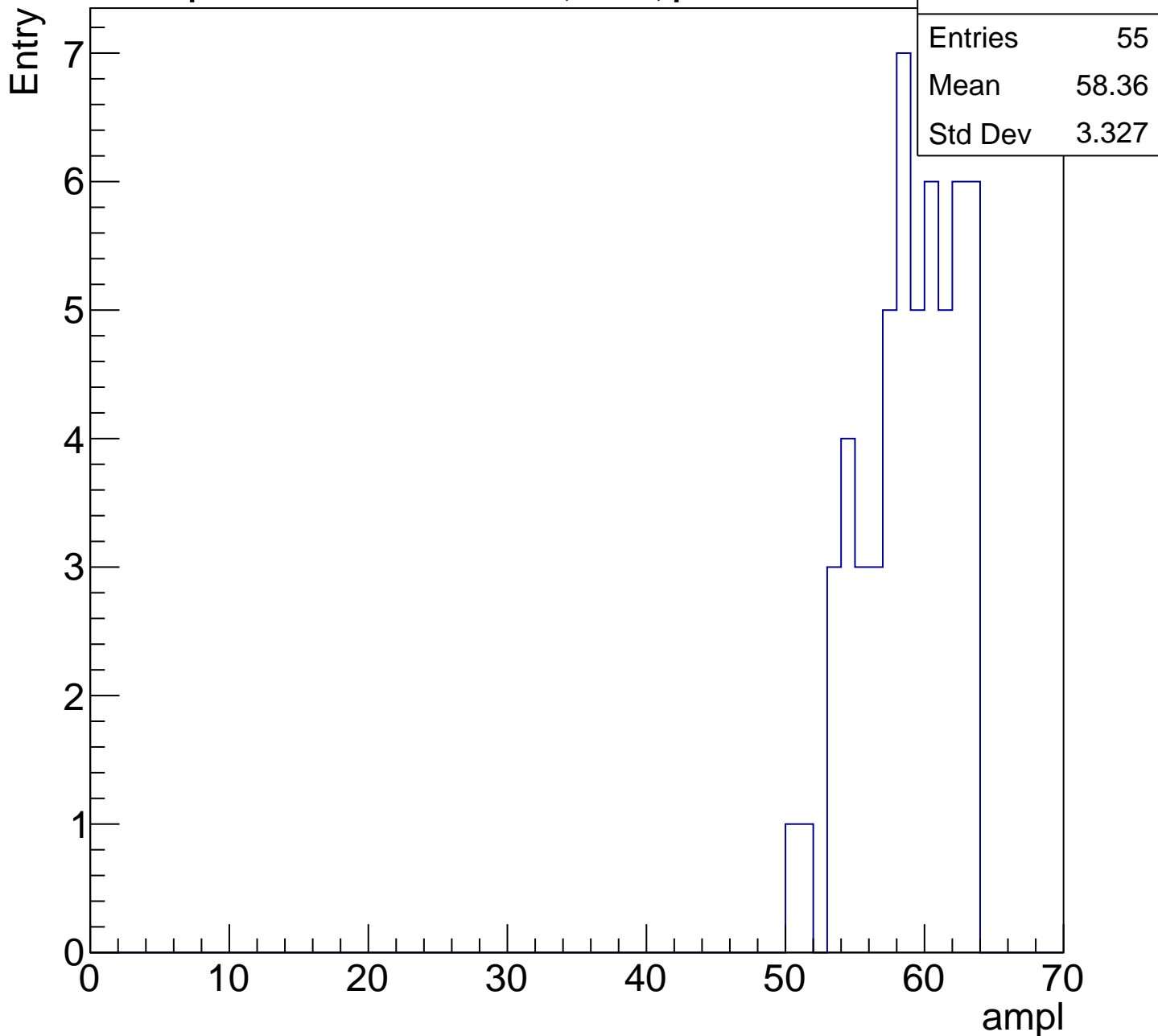
Entry

Entries	62
Mean	52.85
Std Dev	3.161



# B1L103S, U1-ch60, adc5

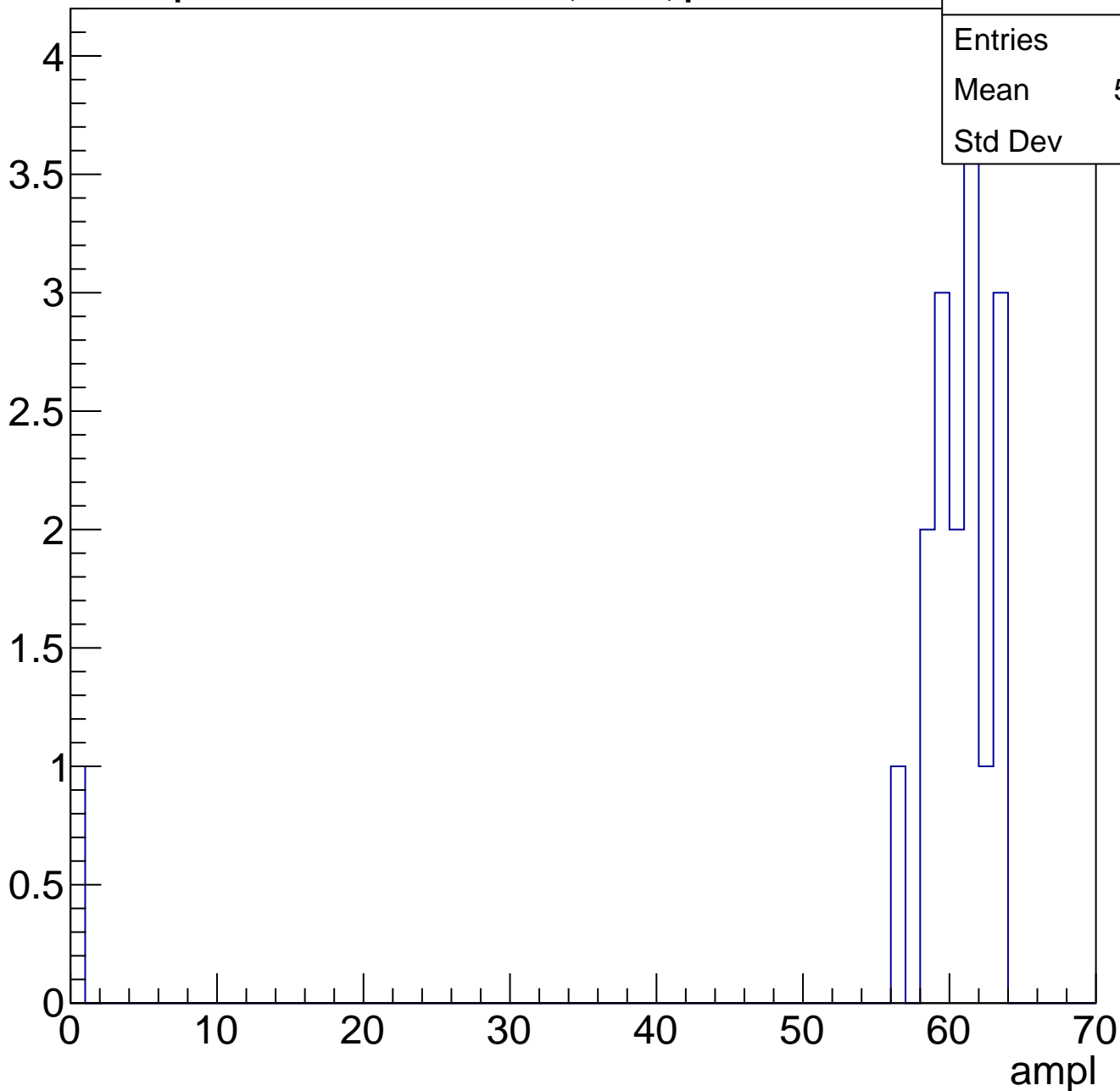
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U1-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



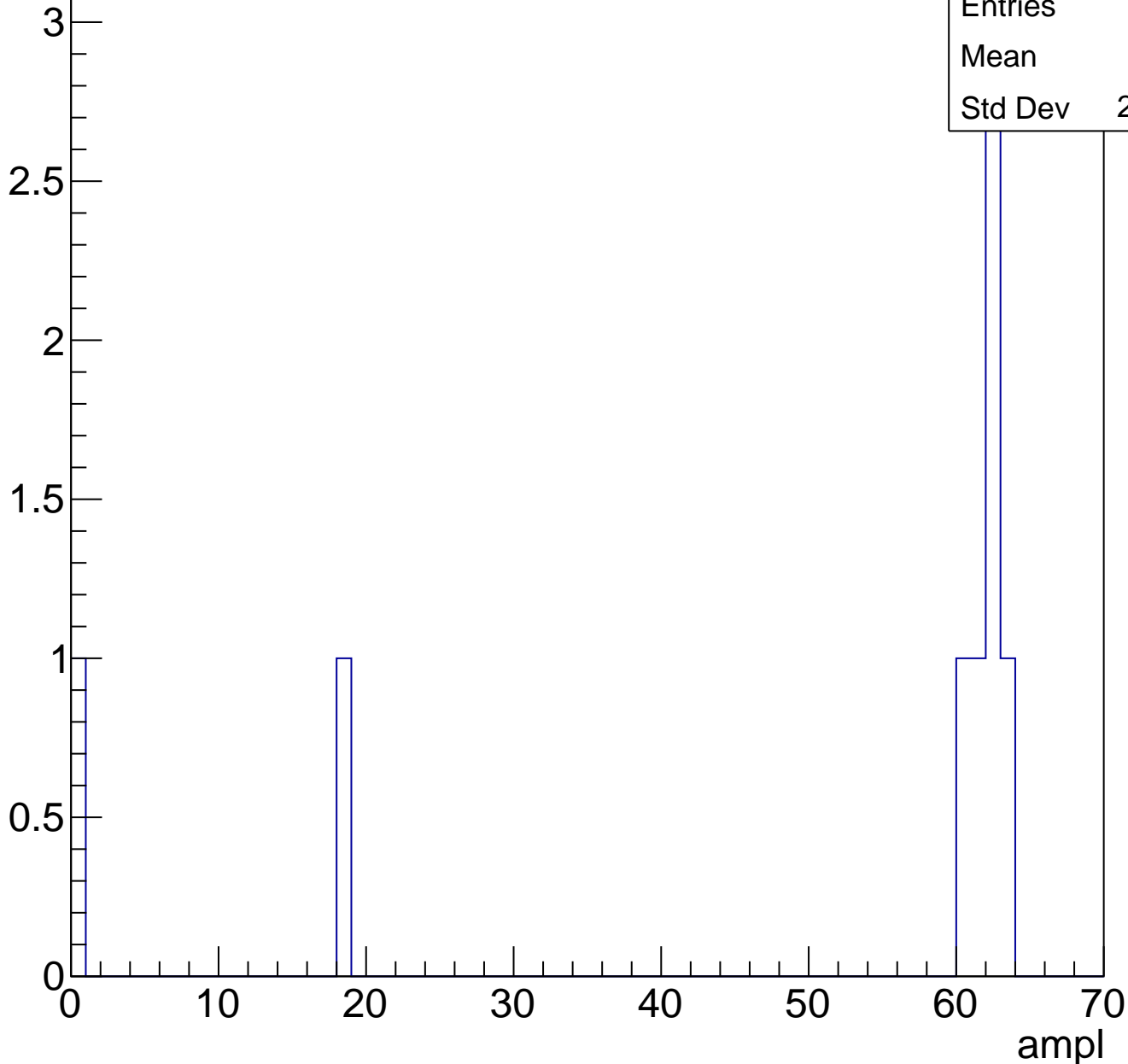
Entries	17
Mean	56.71
Std Dev	14.3



# B1L103S, U1-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch61, adc0

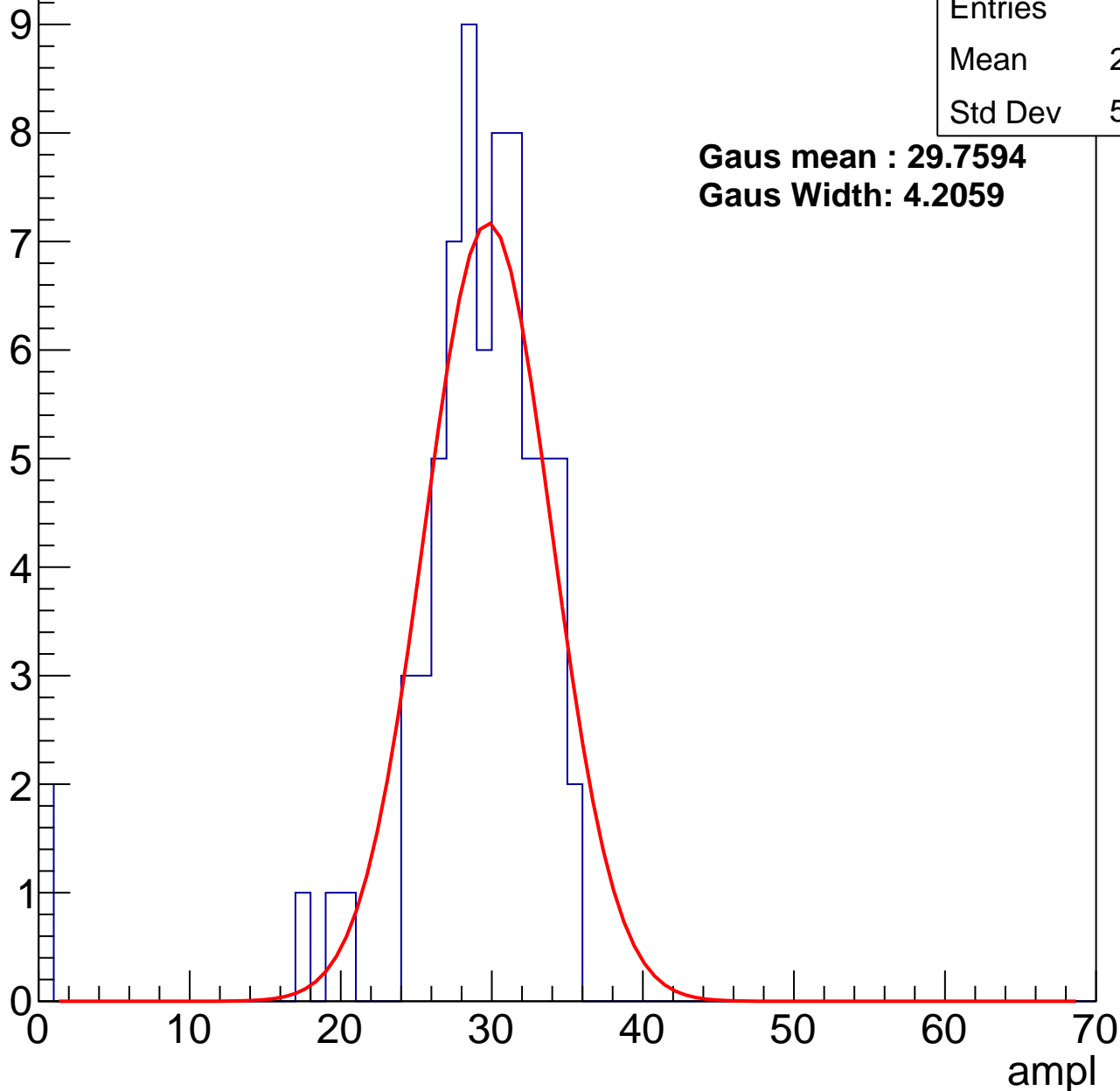
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	28.18
Std Dev	5.965

**Gaus mean : 29.7594**

**Gaus Width: 4.2059**



# B1L103S, U1-ch61, adc1

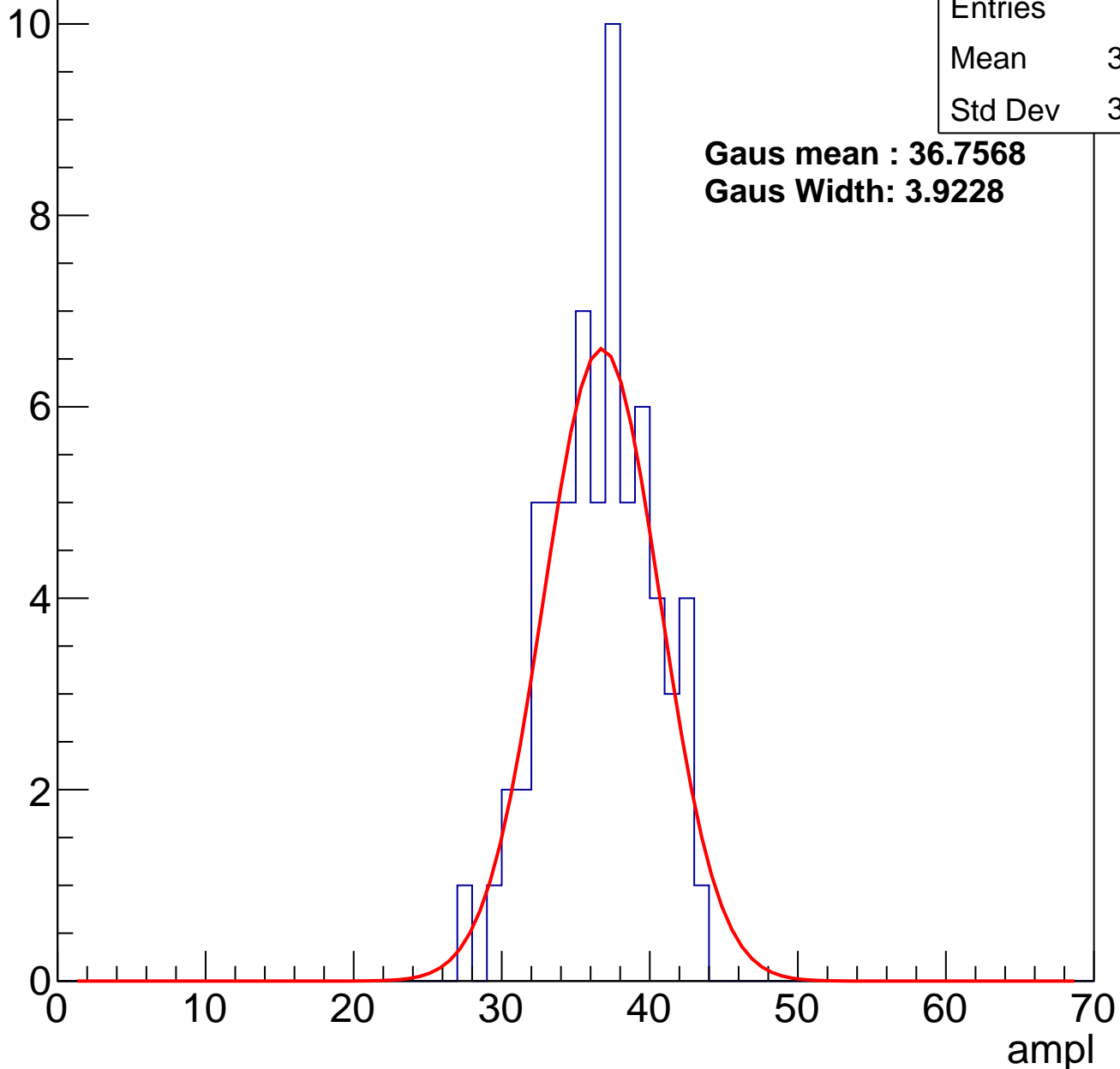
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	66
Mean	36.15
Std Dev	3.522

**Gaus mean : 36.7568**

**Gaus Width: 3.9228**

Entry



# B1L103S, U1-ch61, adc2

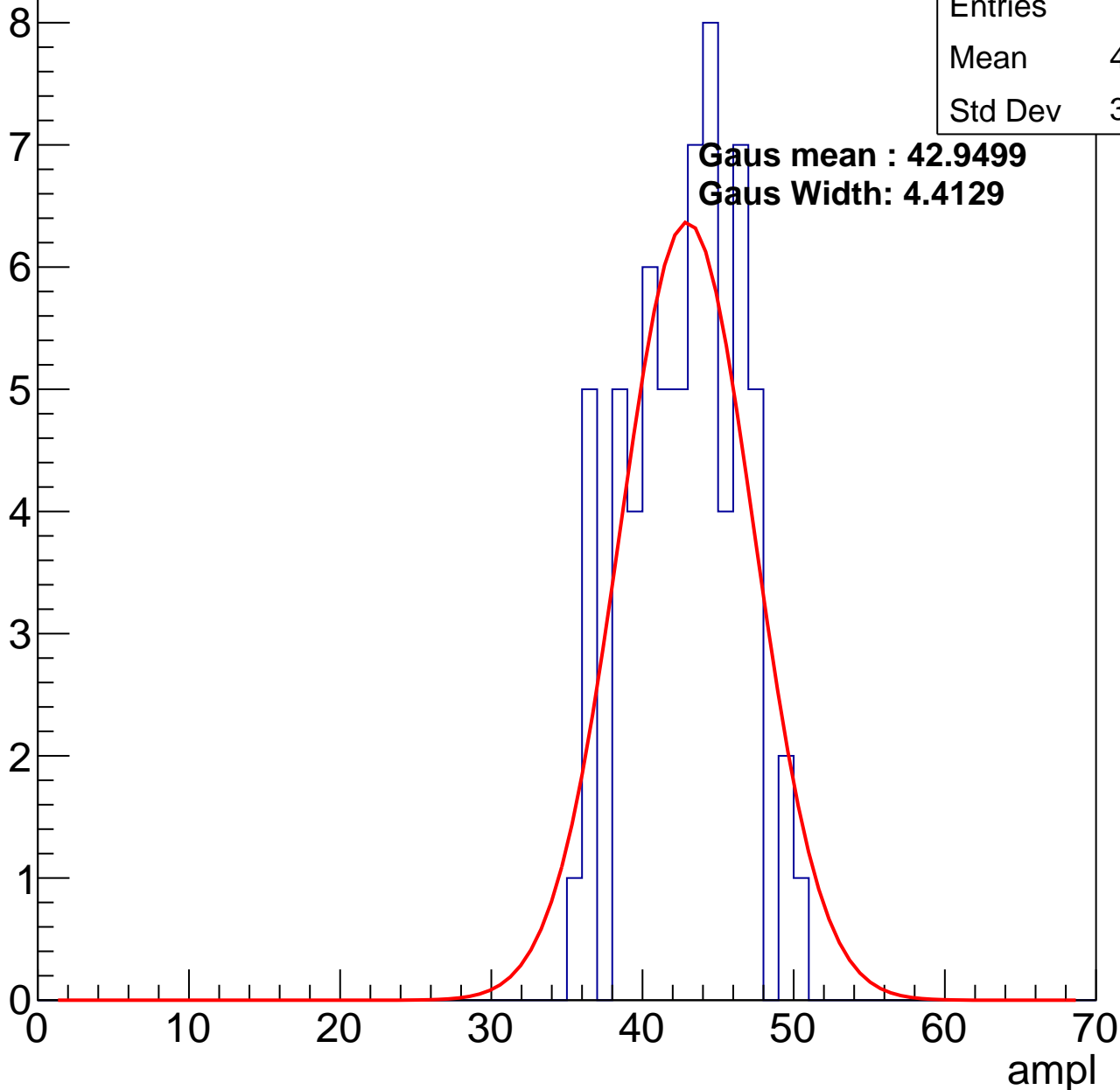
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	42.37
Std Dev	3.593

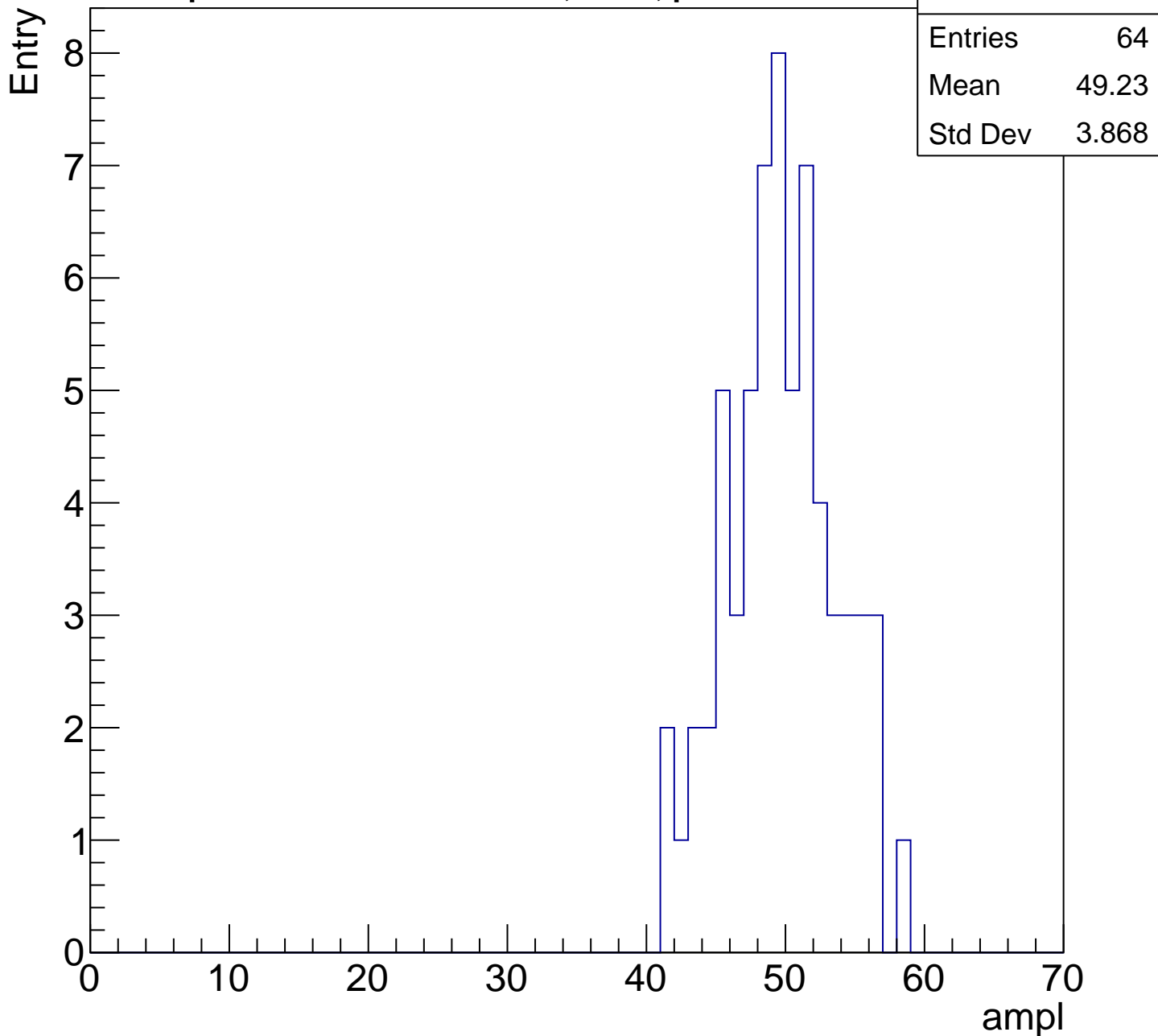
**Gaus mean : 42.9499**

**Gaus Width: 4.4129**



# B1L103S, U1-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

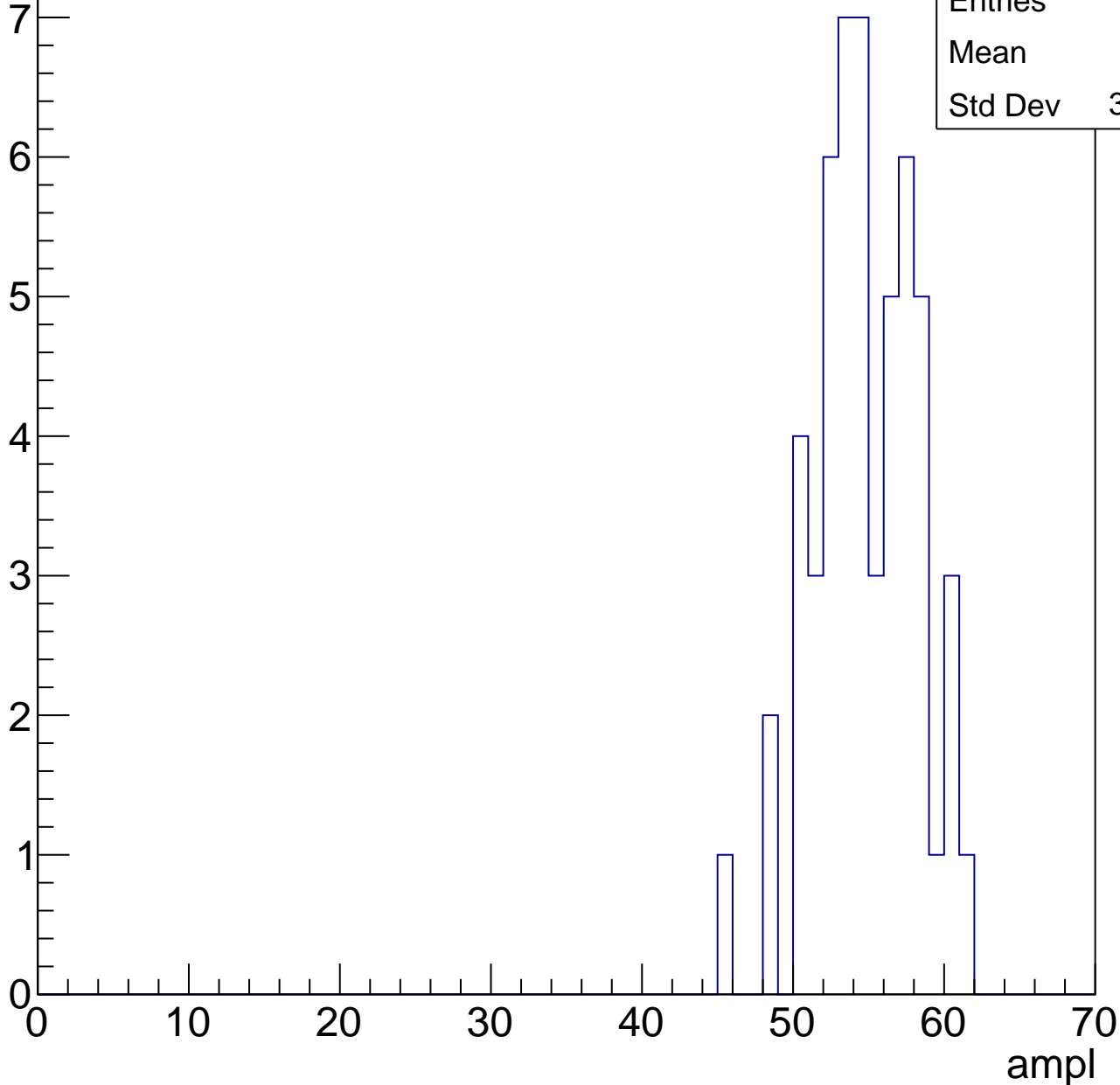


# B1L103S, U1-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	54.3
Std Dev	3.359

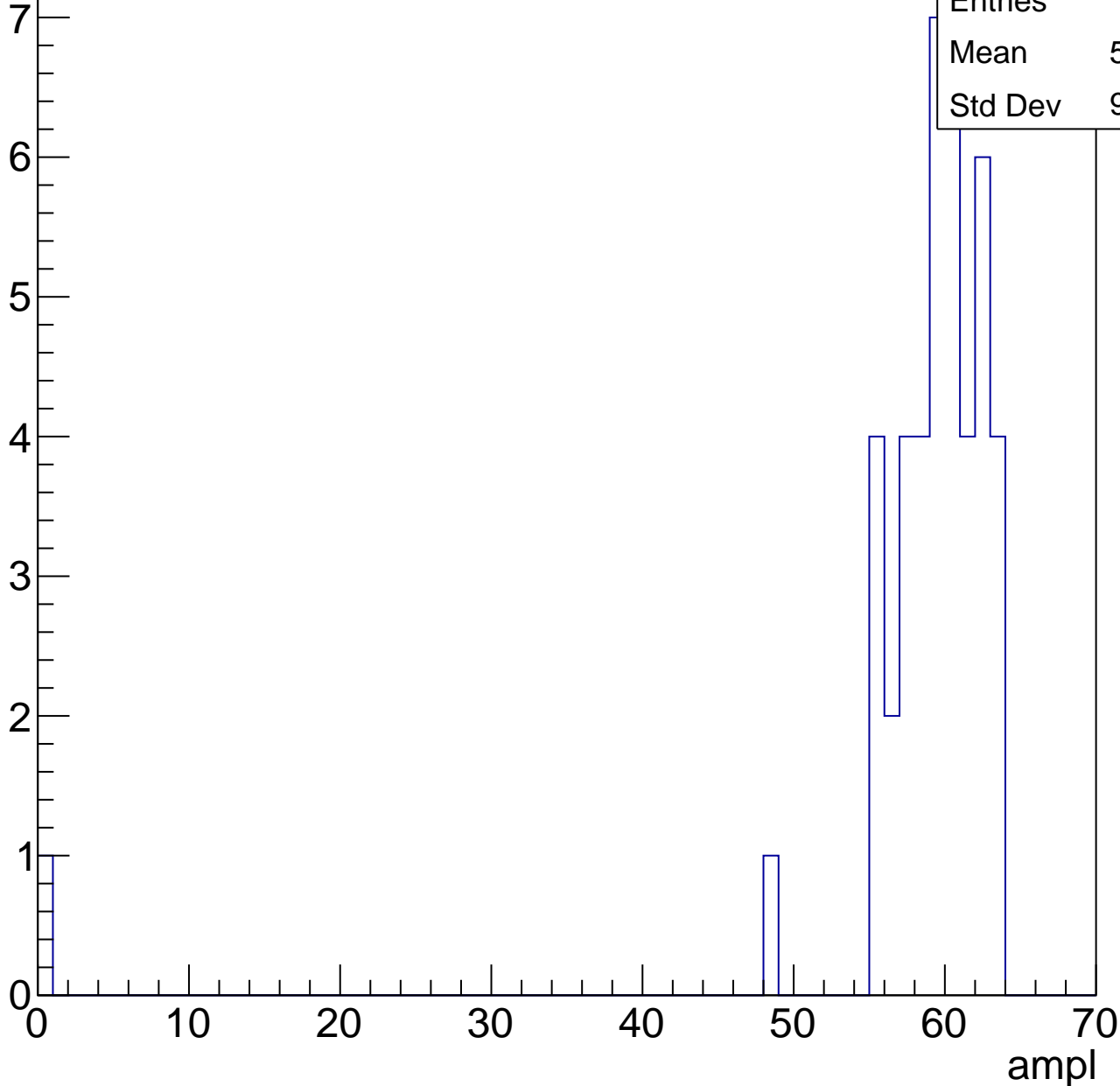


# B1L103S, U1-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	57.75
Std Dev	9.264

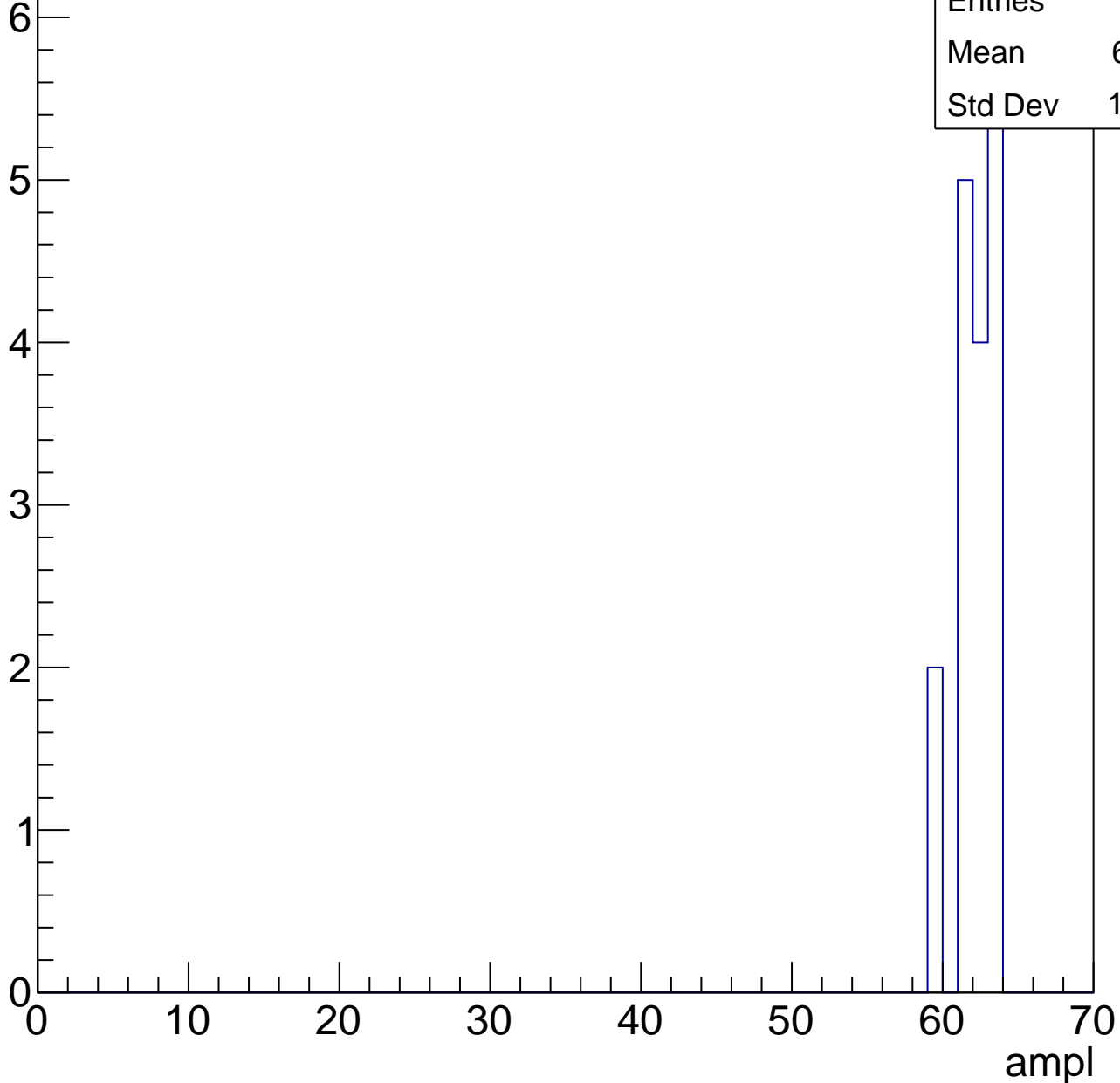


# B1L103S, U1-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	17
Mean	61.71
Std Dev	1.273





# B1L103S, U1-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch62, adc0

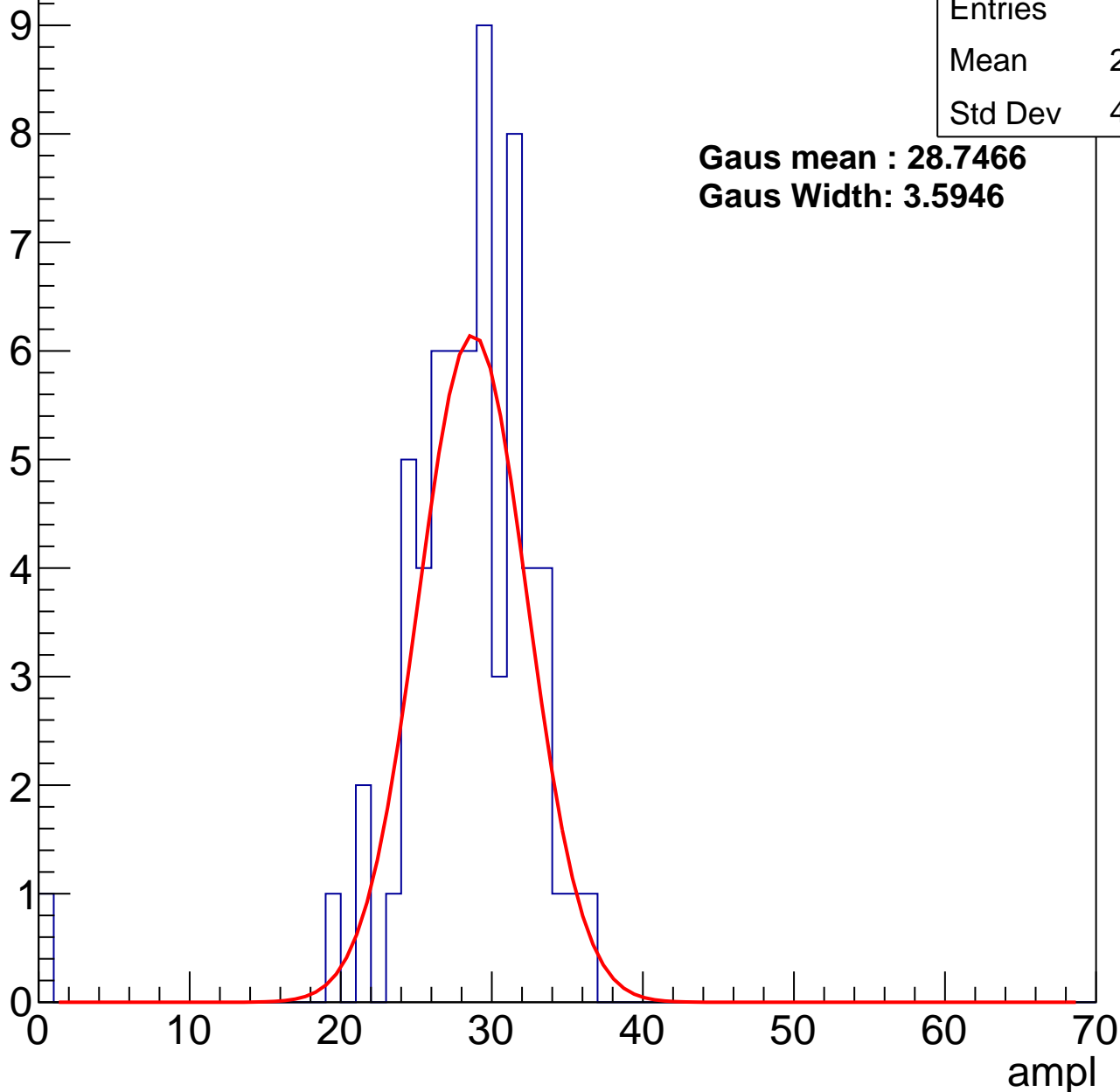
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	27.84
Std Dev	4.942

**Gaus mean : 28.7466**

**Gaus Width: 3.5946**



# B1L103S, U1-ch62, adc1

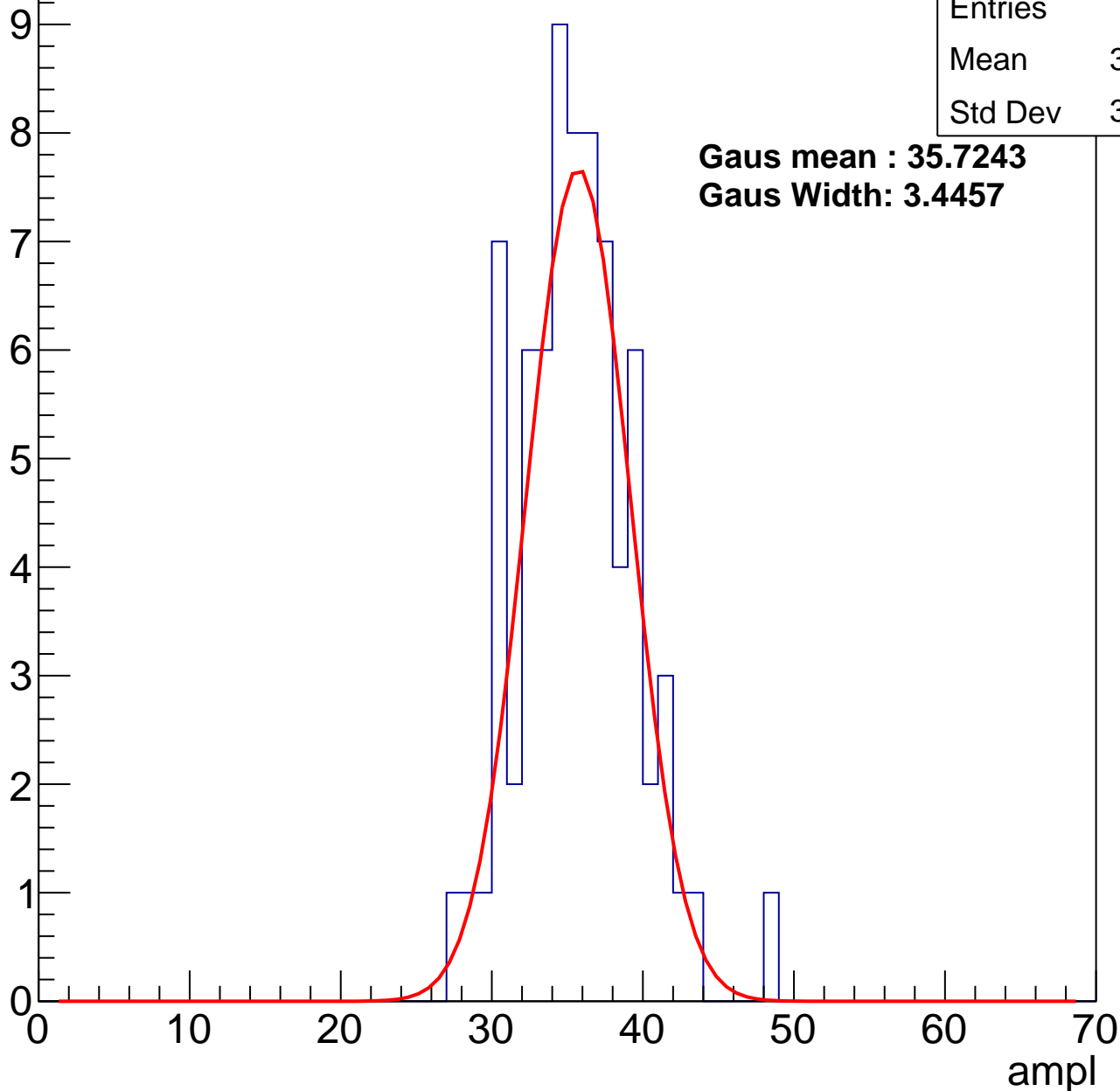
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	35.15
Std Dev	3.766

**Gaus mean : 35.7243**

**Gaus Width: 3.4457**



# B1L103S, U1-ch62, adc2

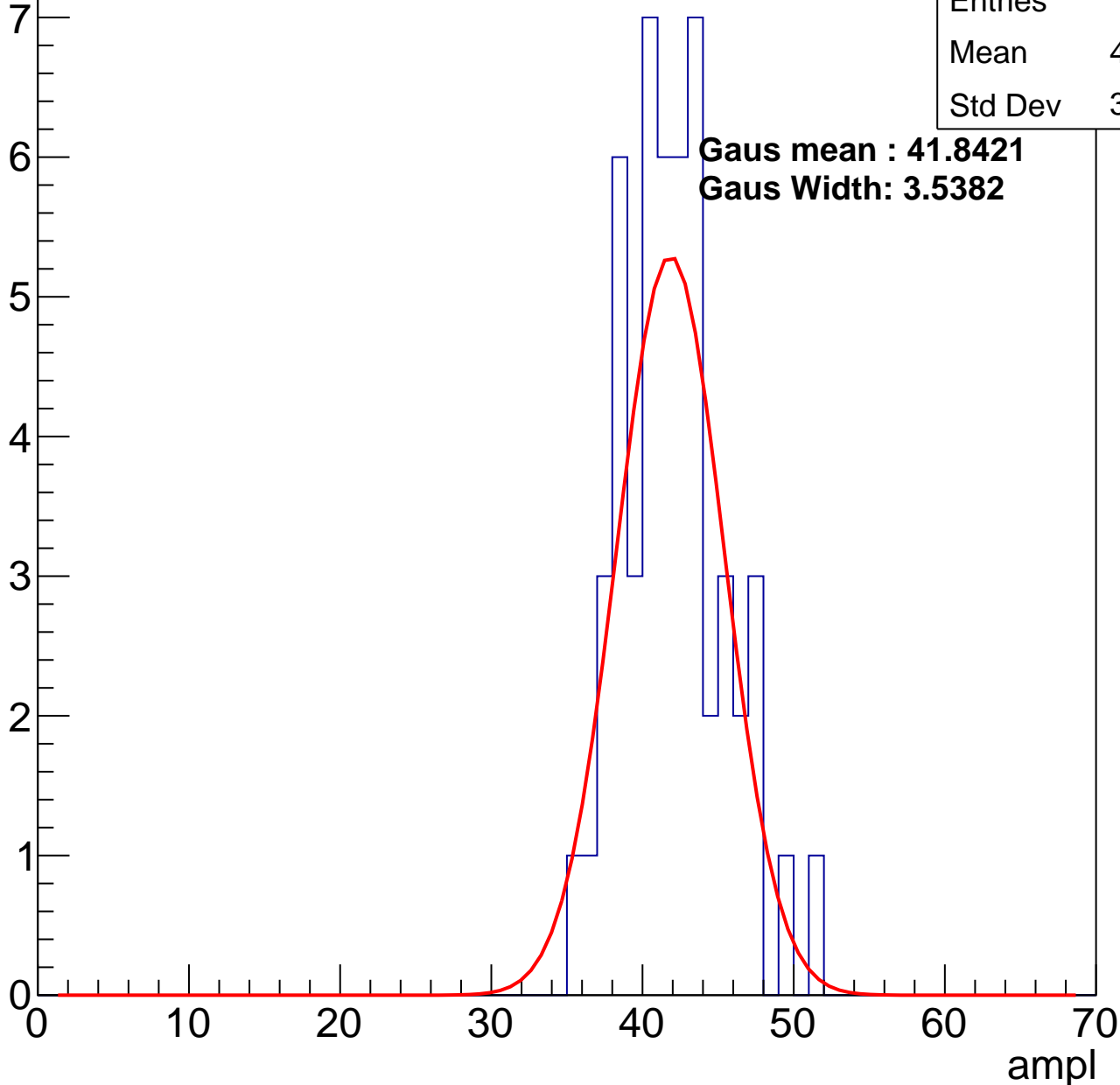
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	41.58
Std Dev	3.359

**Gaus mean : 41.8421**

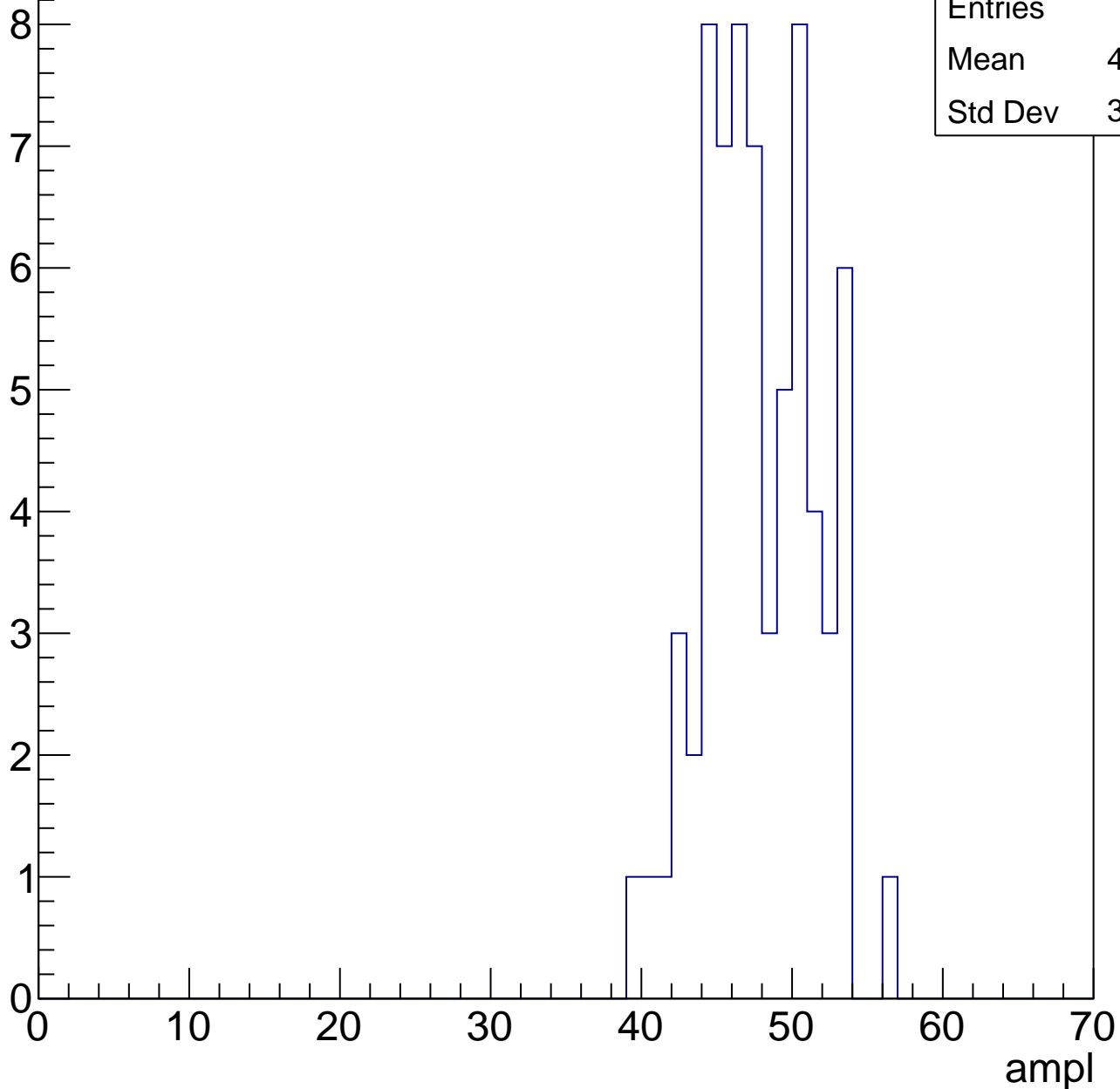
**Gaus Width: 3.5382**



# B1L103S, U1-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



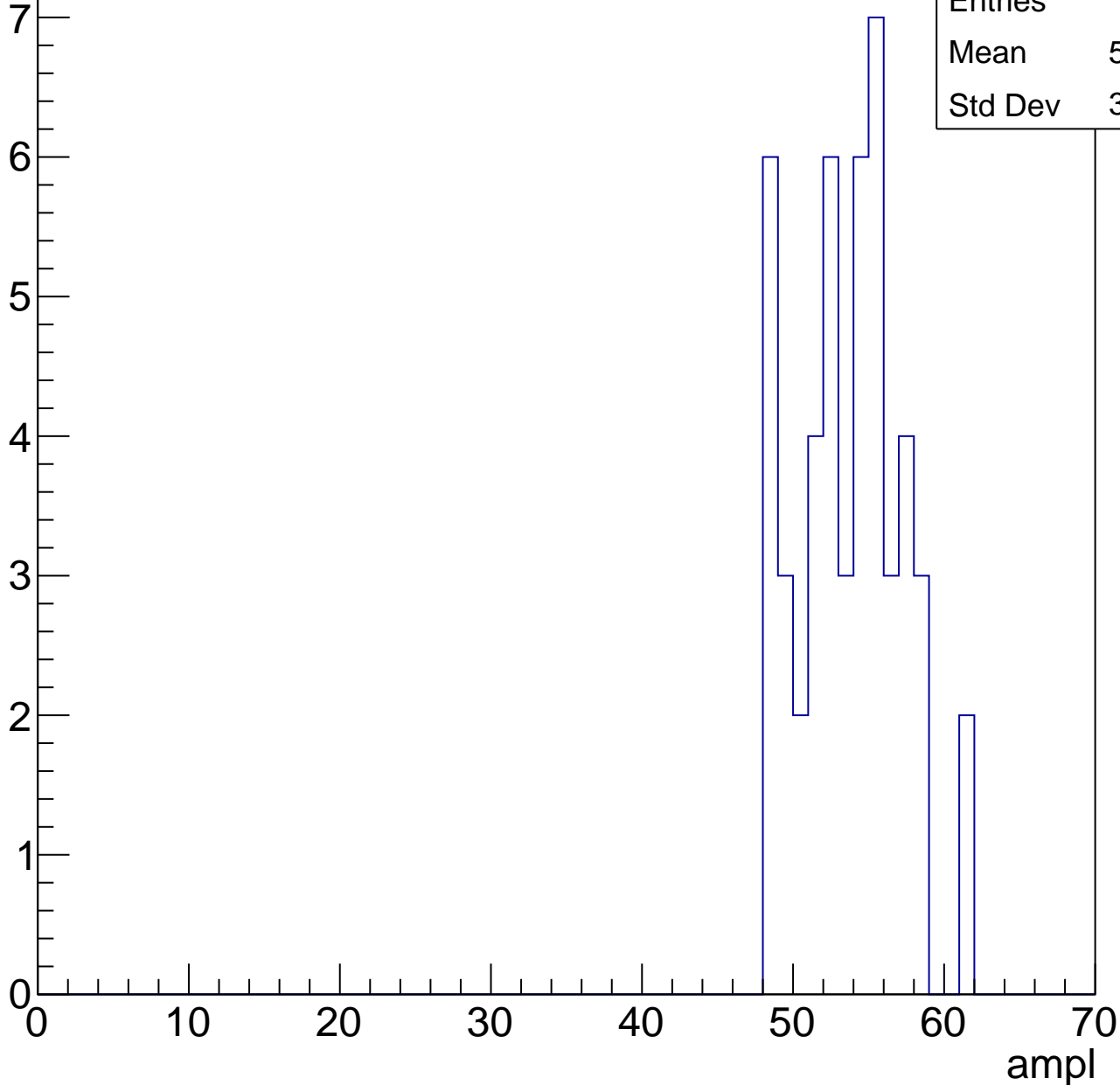
Entries	68
Mean	47.34
Std Dev	3.612

# B1L103S, U1-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	53.29
Std Dev	3.387

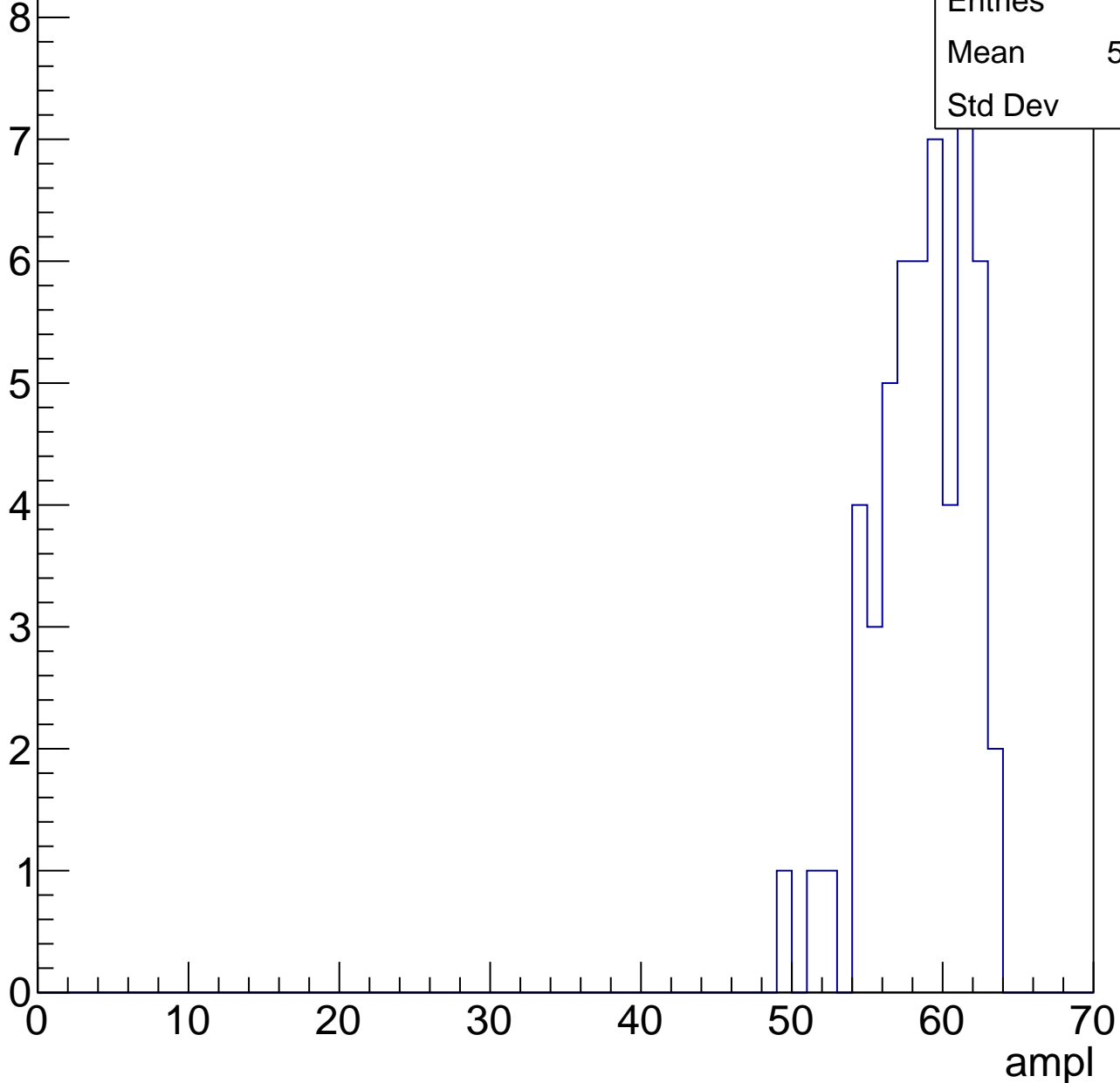


# B1L103S, U1-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	58.19
Std Dev	3.11

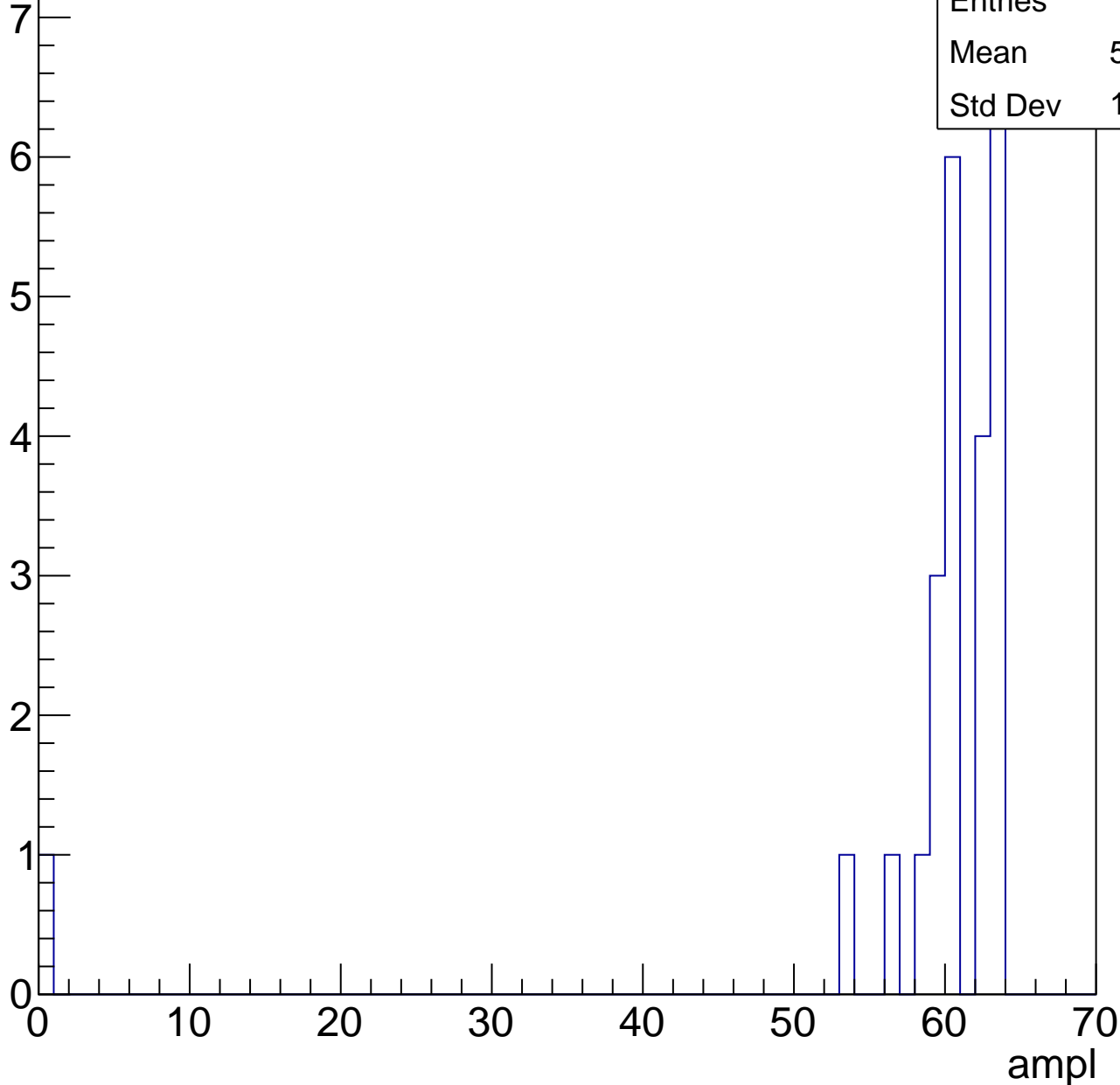


# B1L103S, U1-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	24
Mean	58.04
Std Dev	12.35





# B1L103S, U1-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch63, adc0

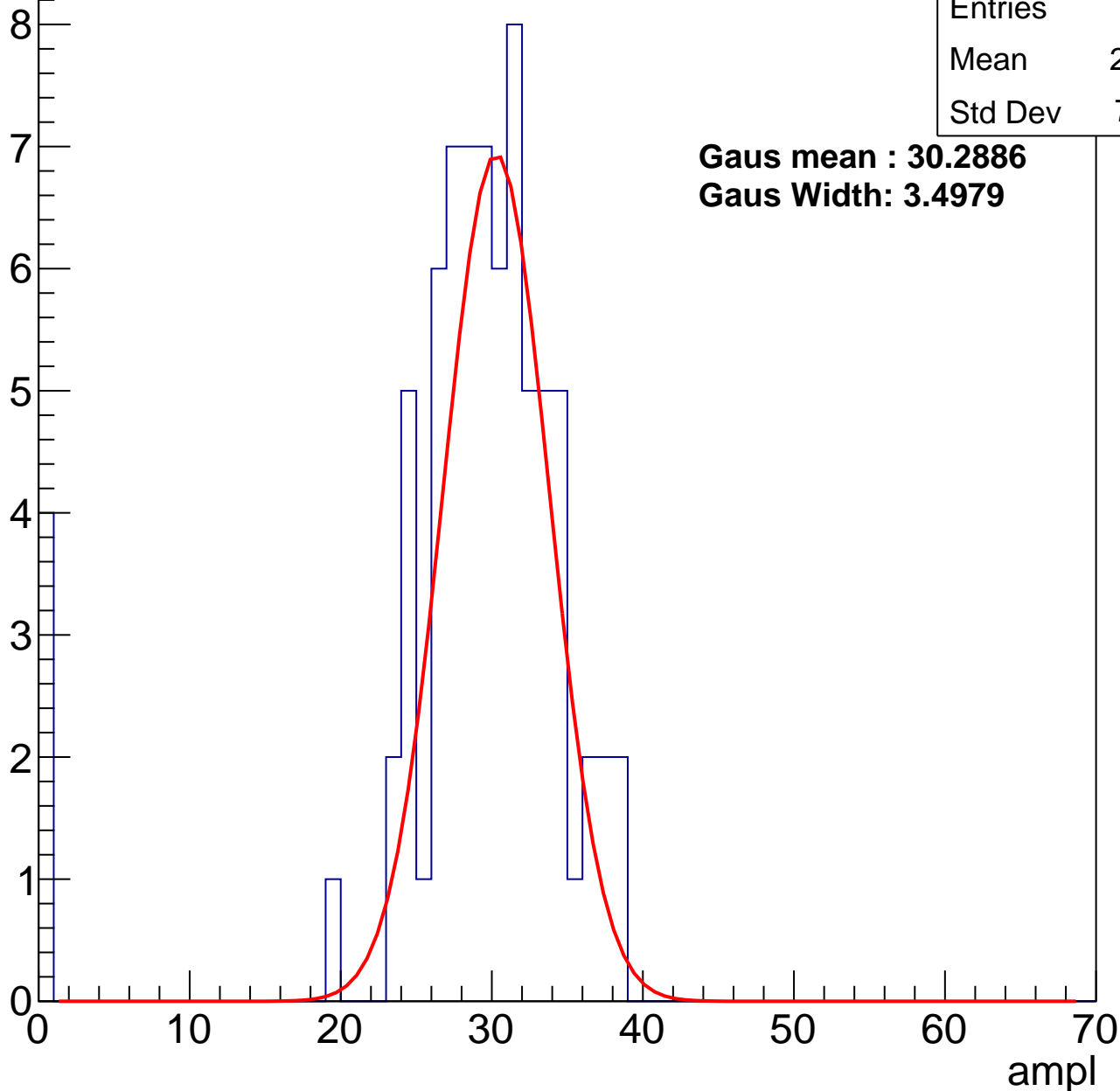
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	28.08
Std Dev	7.621

**Gaus mean : 30.2886**

**Gaus Width: 3.4979**



# B1L103S, U1-ch63, adc1

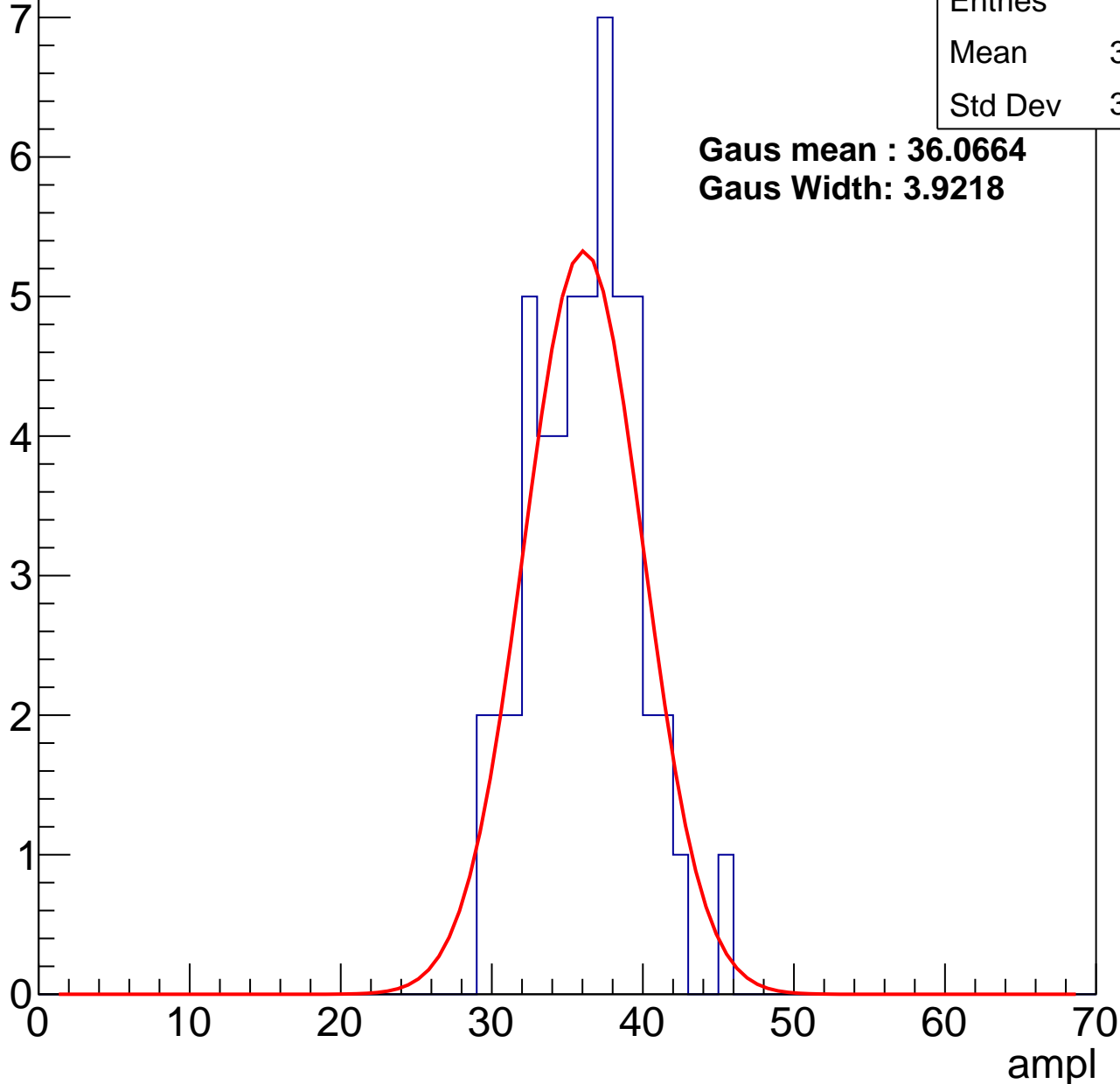
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	35.69
Std Dev	3.462

**Gaus mean : 36.0664**

**Gaus Width: 3.9218**



# B1L103S, U1-ch63, adc2

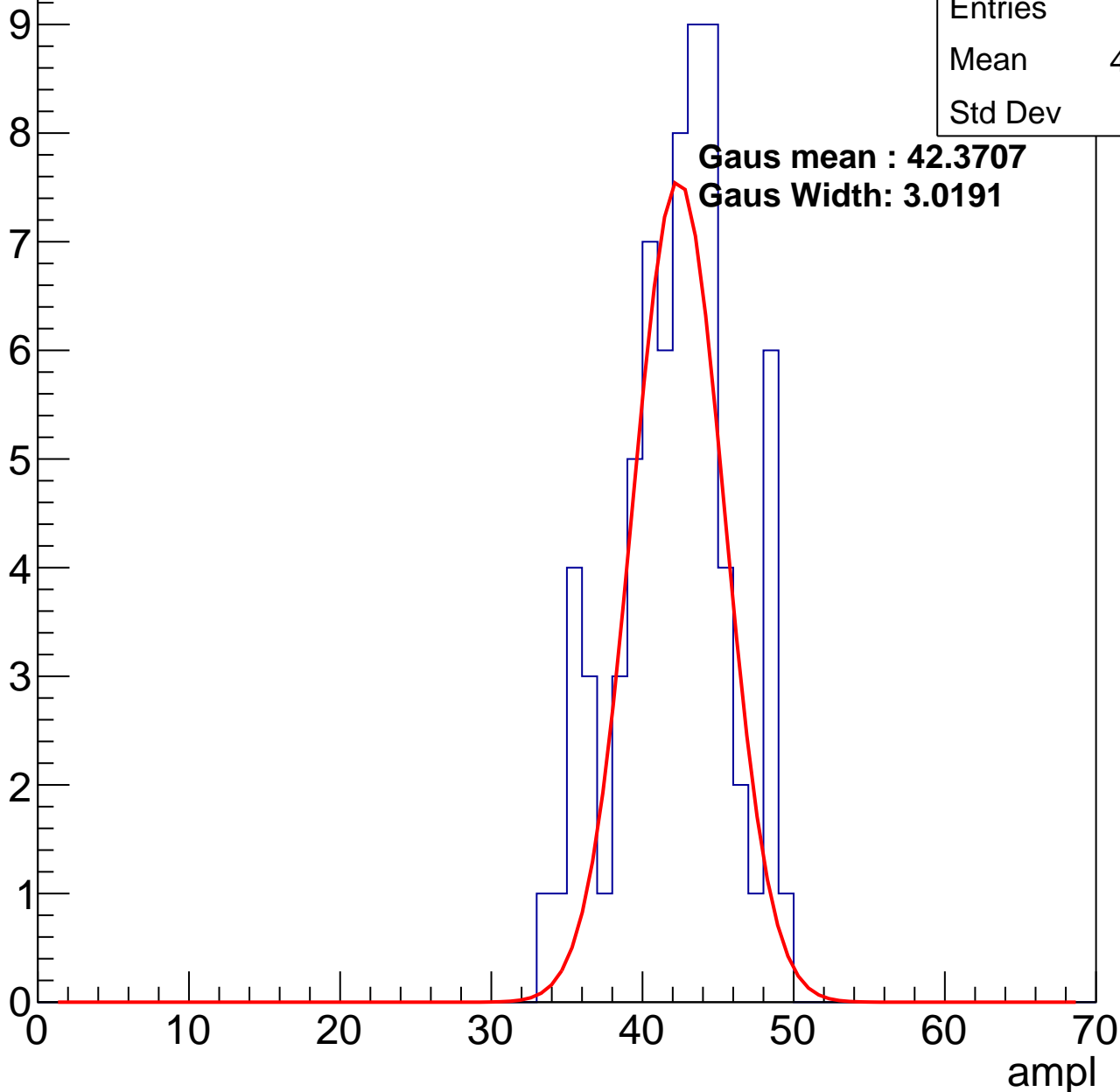
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	41.72
Std Dev	3.75

**Gaus mean : 42.3707**

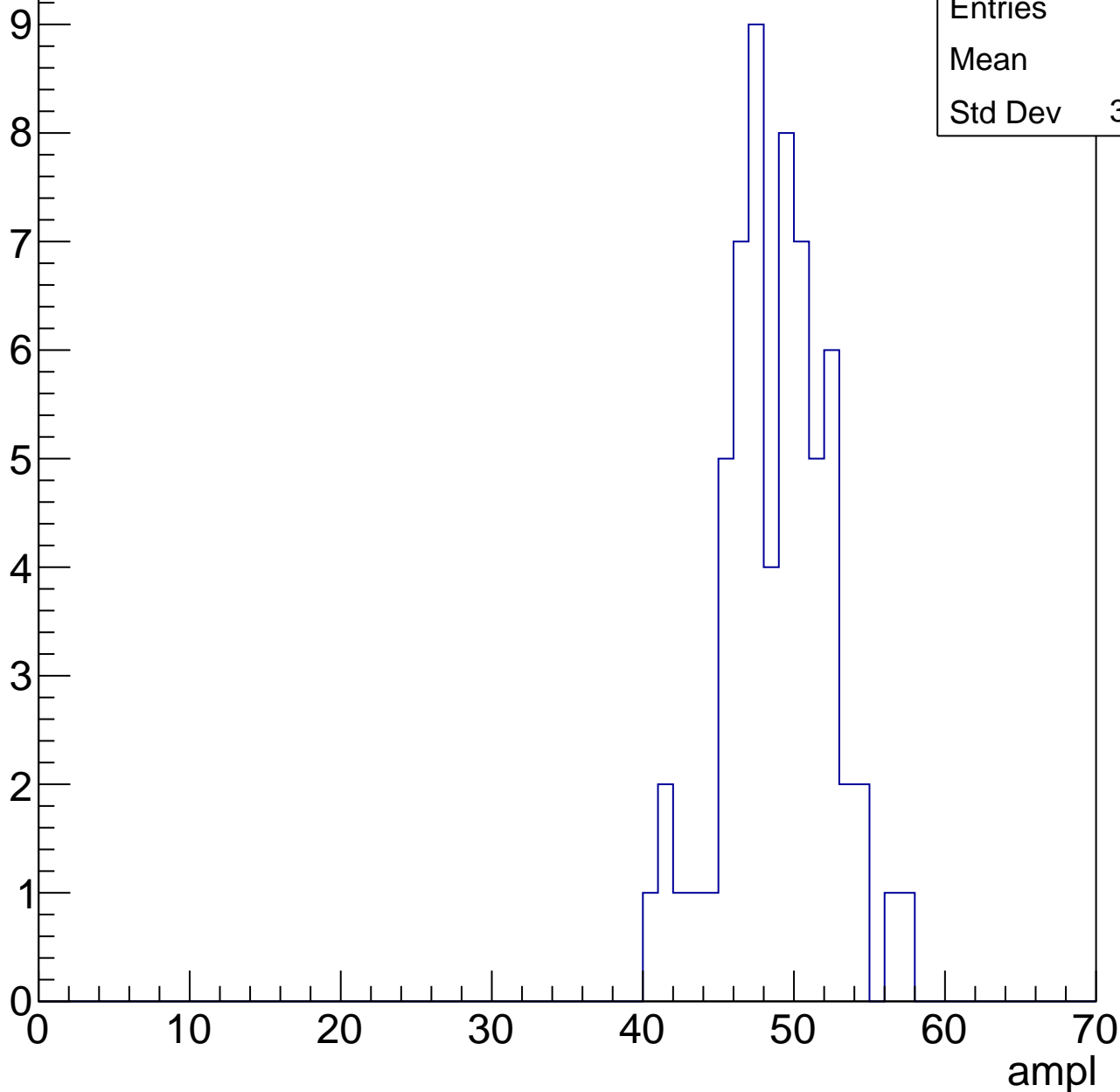
**Gaus Width: 3.0191**



# B1L103S, U1-ch63, adc3

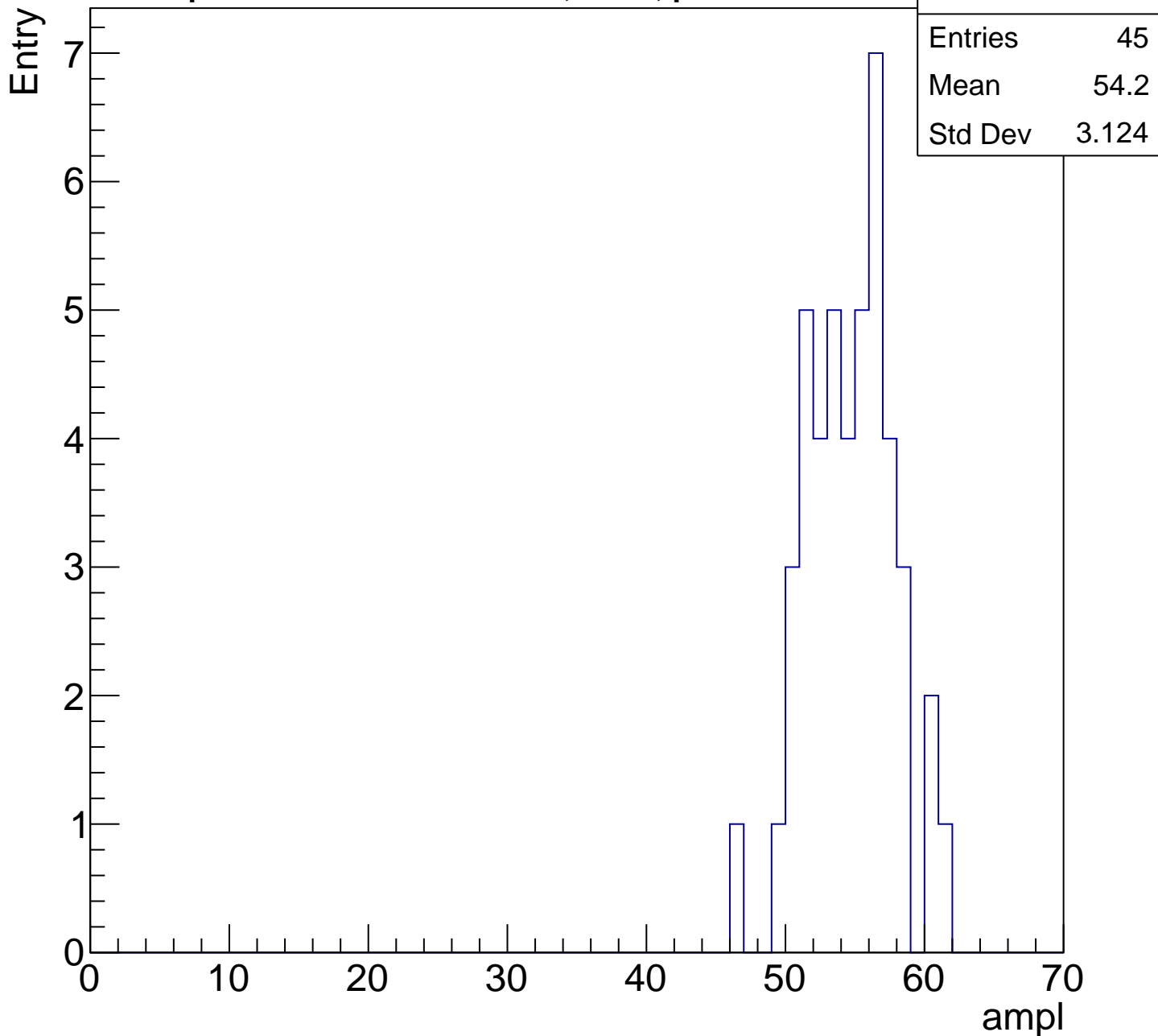
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U1-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

10

Entries 60

Mean 58.58

Std Dev 2.818

8

6

4

2

0

0

10

20

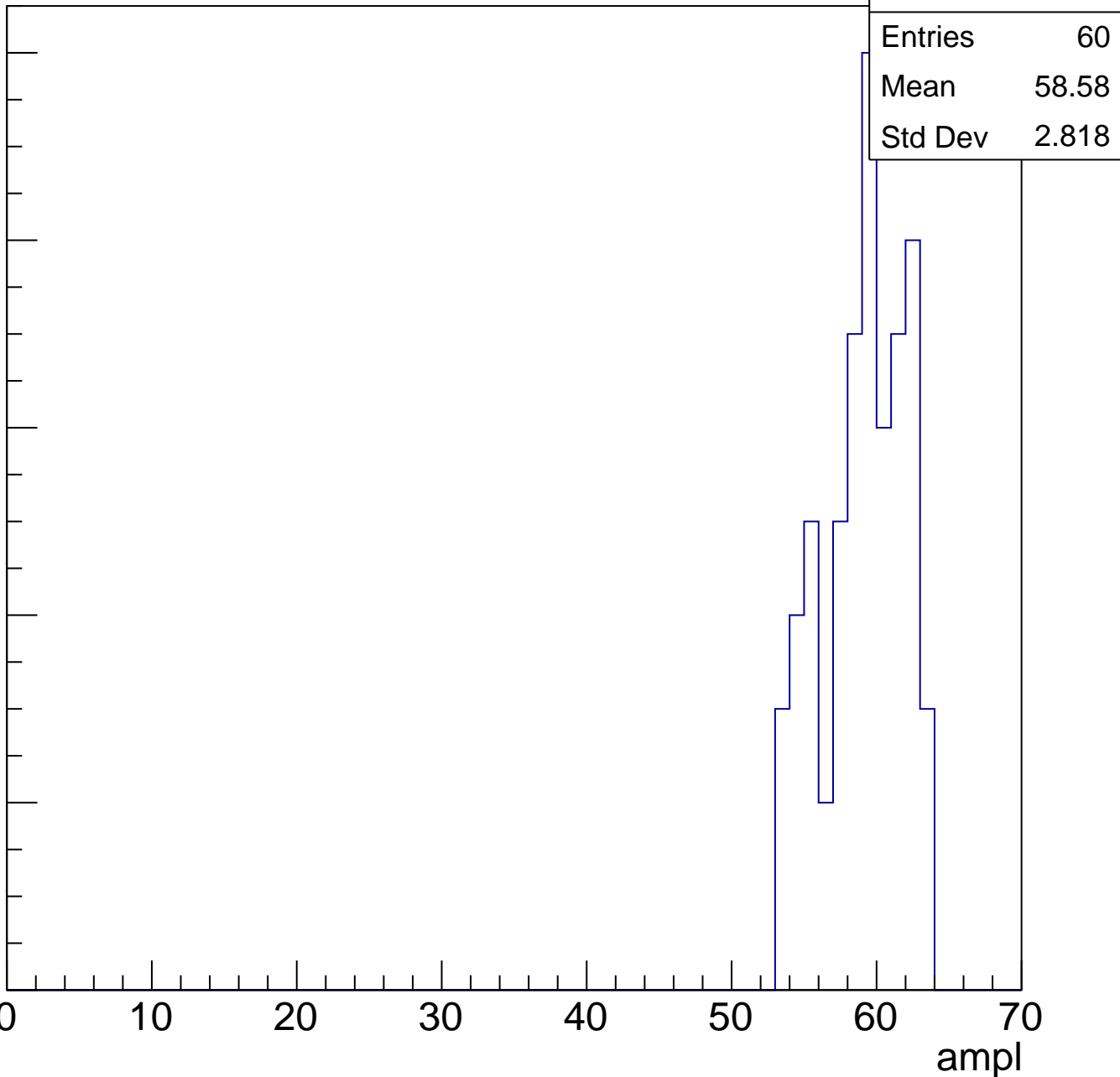
30

40

50

60

ampl

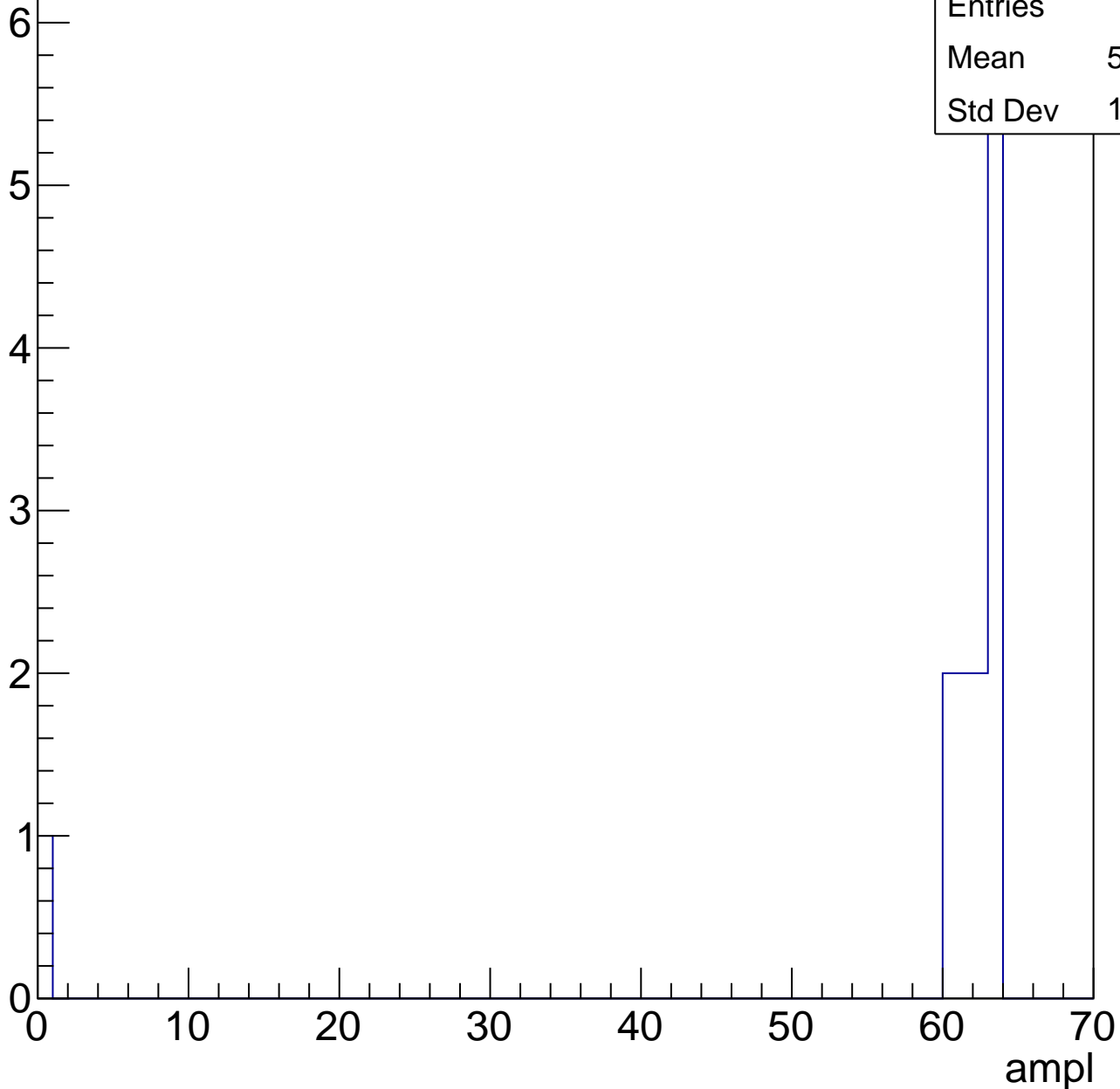


# B1L103S, U1-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	13
Mean	57.23
Std Dev	16.56





# B1L103S, U1-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L103S, U1-ch64, adc0

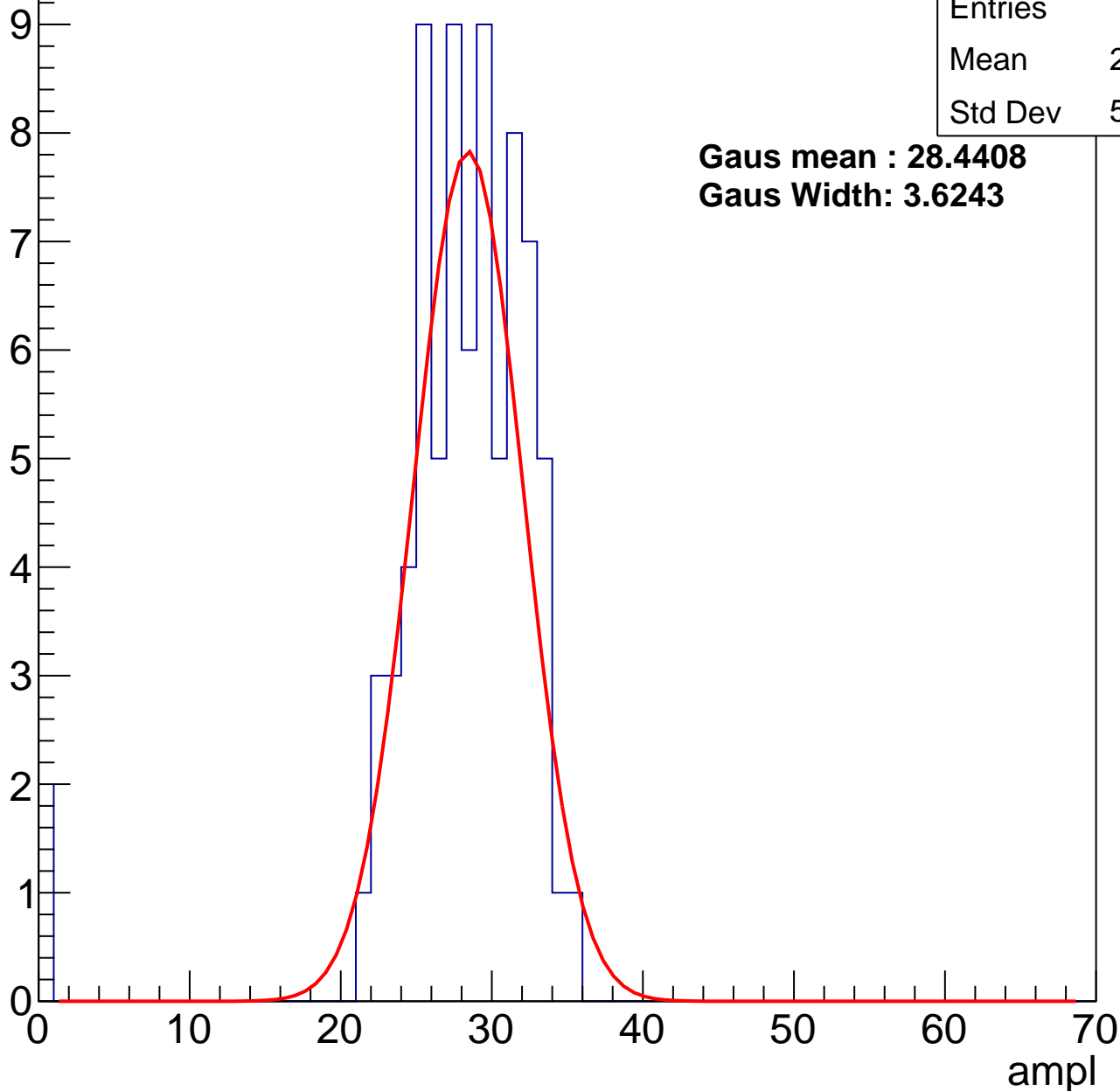
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	27.37
Std Dev	5.508

**Gaus mean : 28.4408**

**Gaus Width: 3.6243**



# B1L103S, U1-ch64, adc1

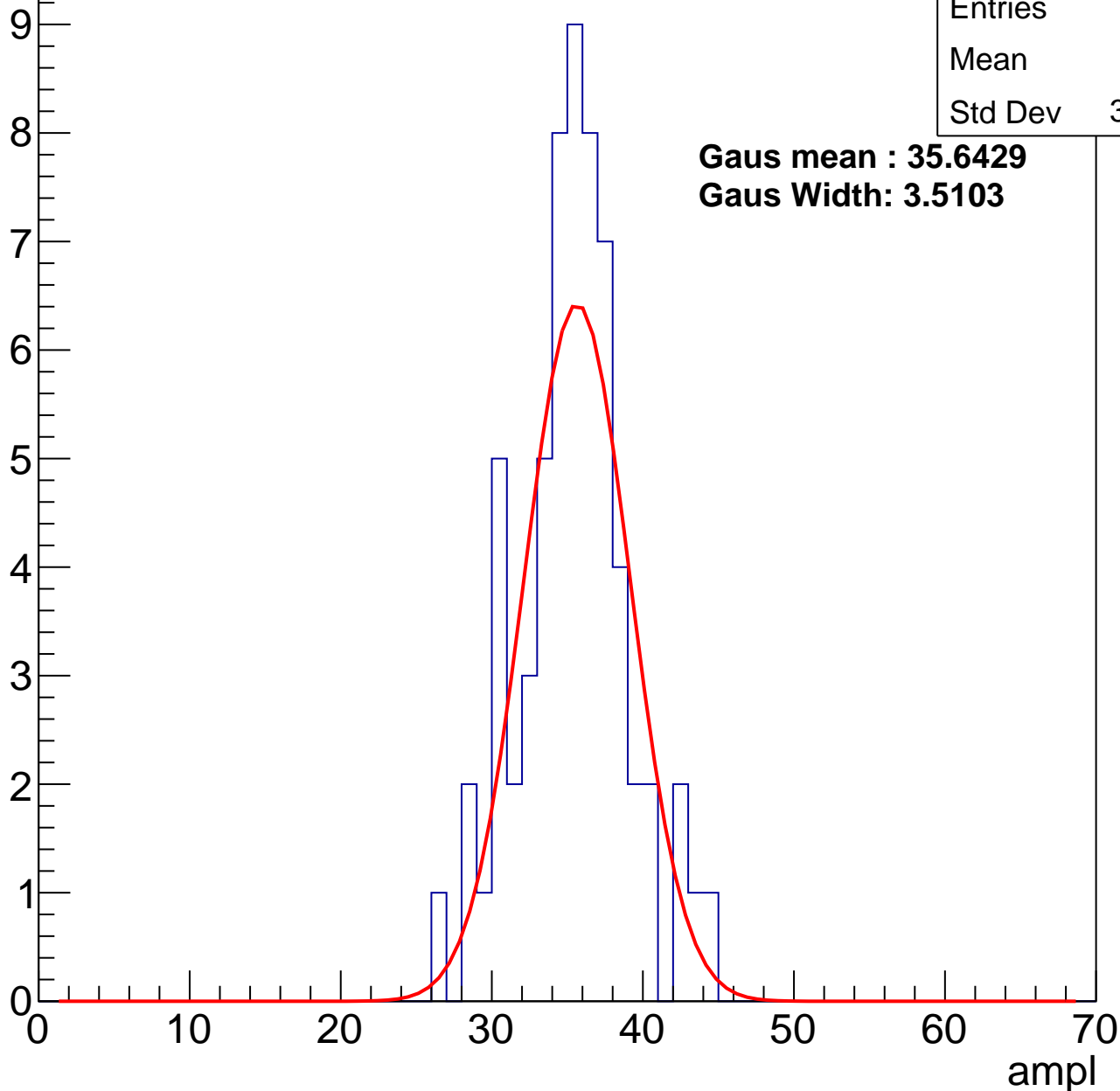
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	34.9
Std Dev	3.615

**Gaus mean : 35.6429**

**Gaus Width: 3.5103**



# B1L103S, U1-ch64, adc2

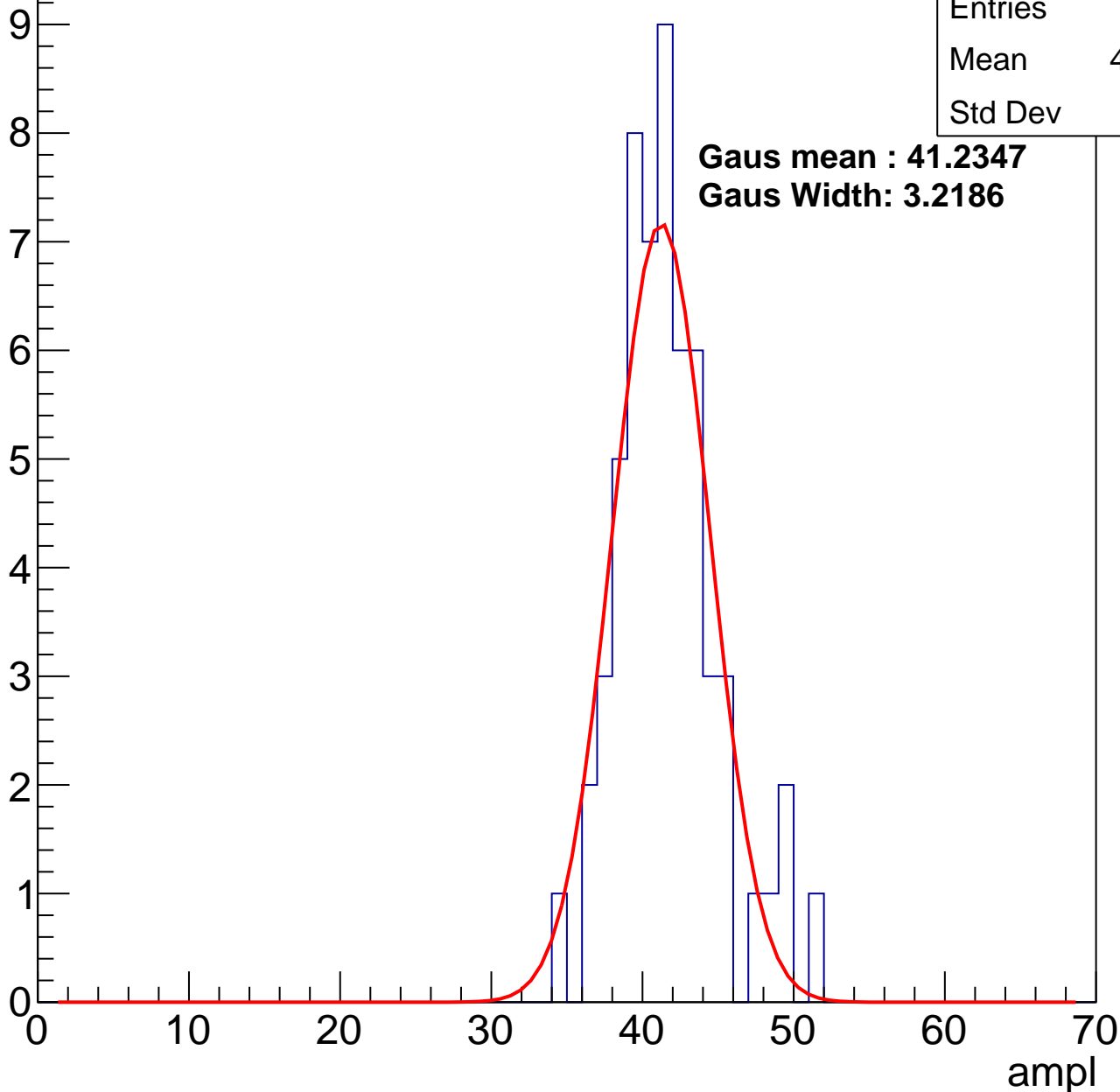
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	41.19
Std Dev	3.34

**Gaus mean : 41.2347**

**Gaus Width: 3.2186**



# B1L103S, U1-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

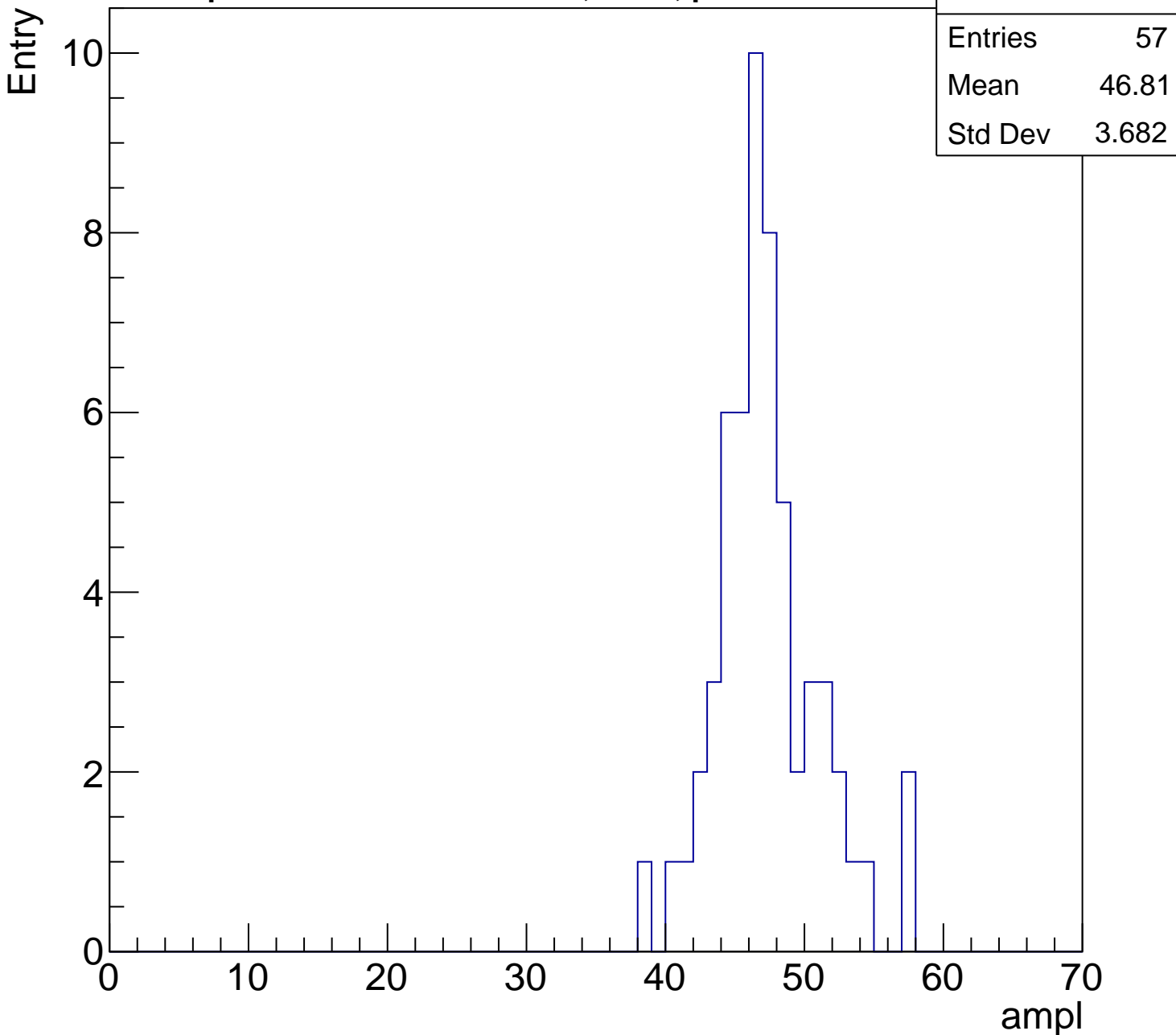
Entries	57
Mean	46.81
Std Dev	3.682

Entry

10  
8  
6  
4  
2  
0

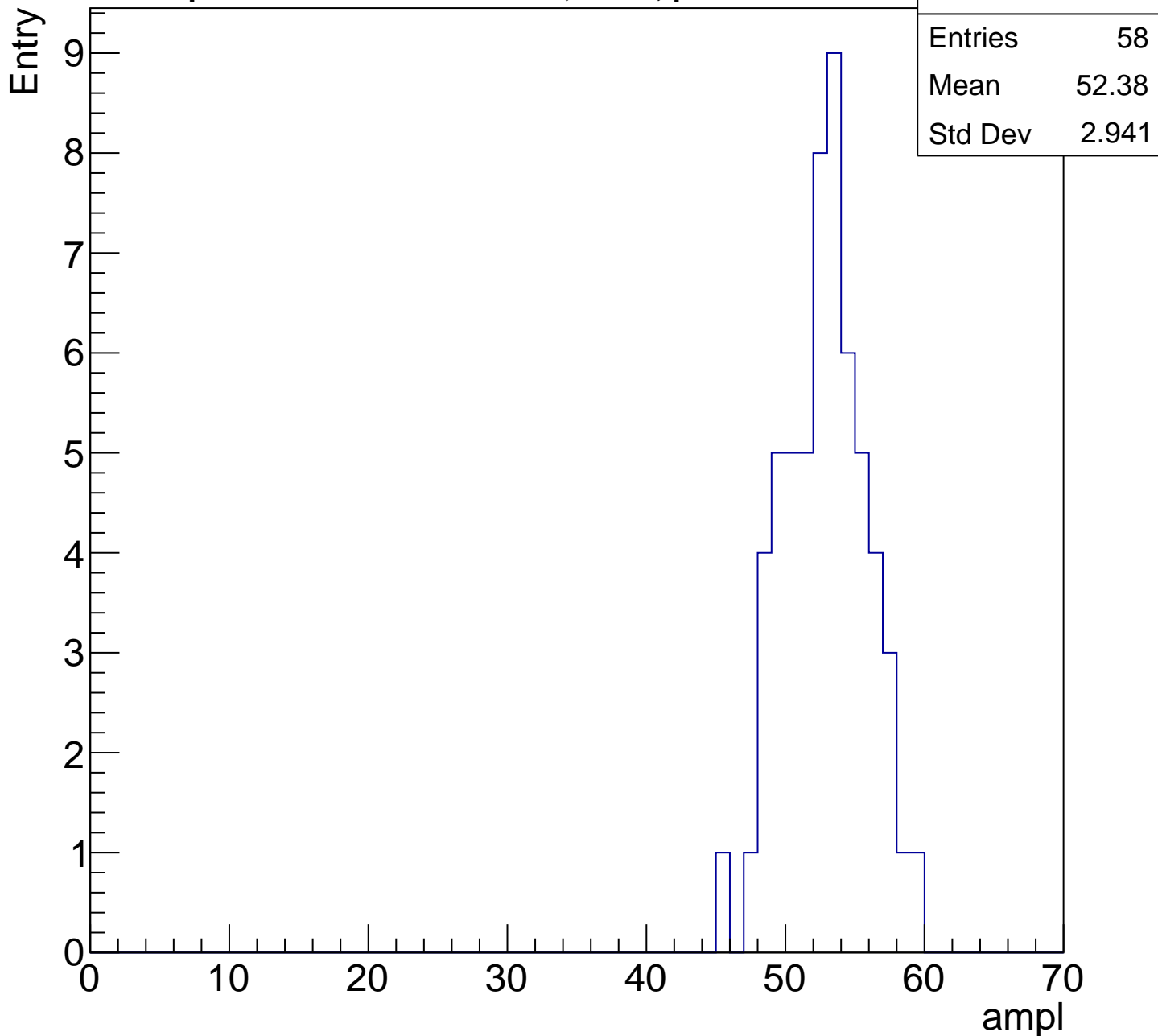
0 10 20 30 40 50 60 70

ampl



# B1L103S, U1-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

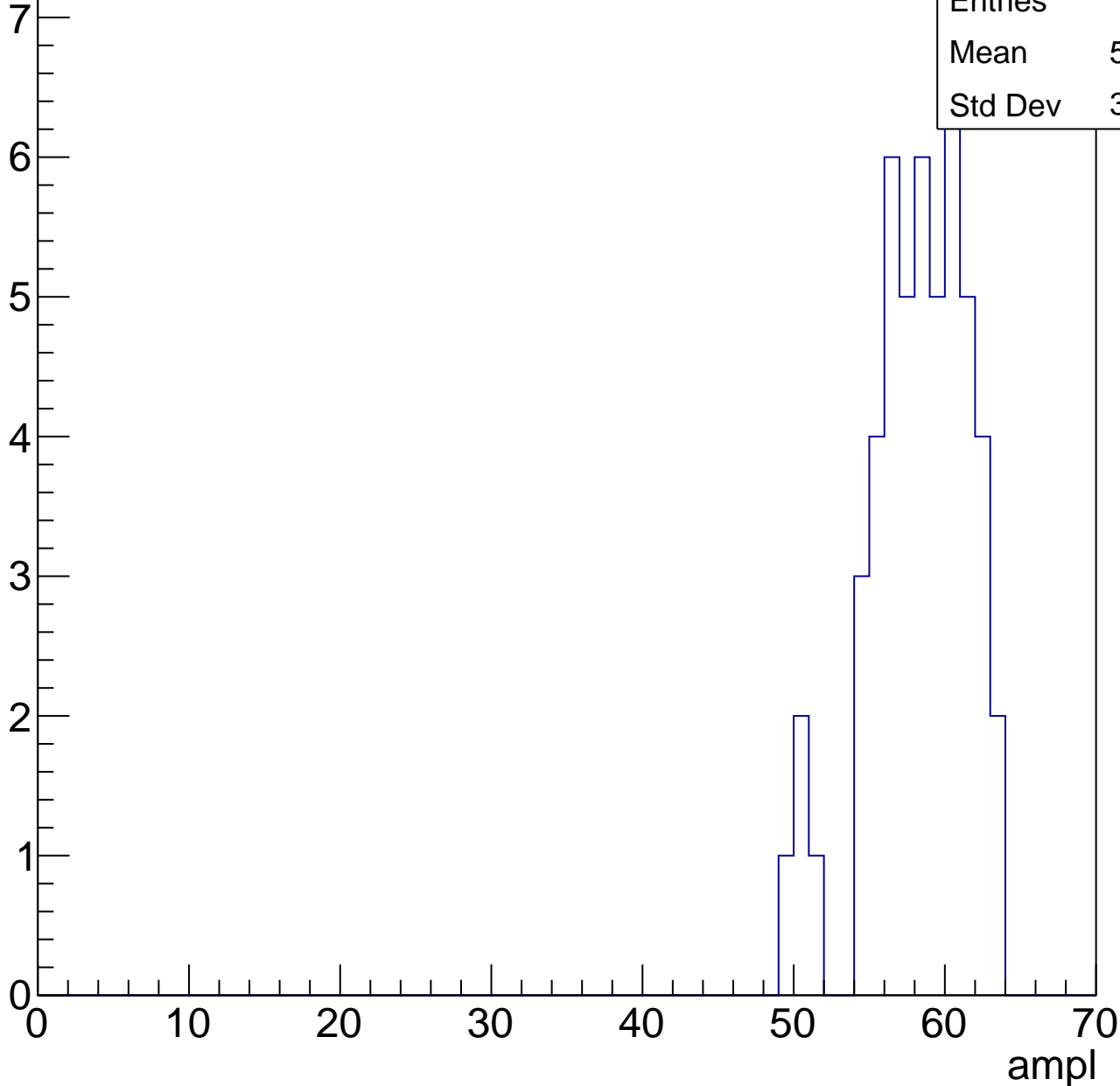


# B1L103S, U1-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	57.75
Std Dev	3.313

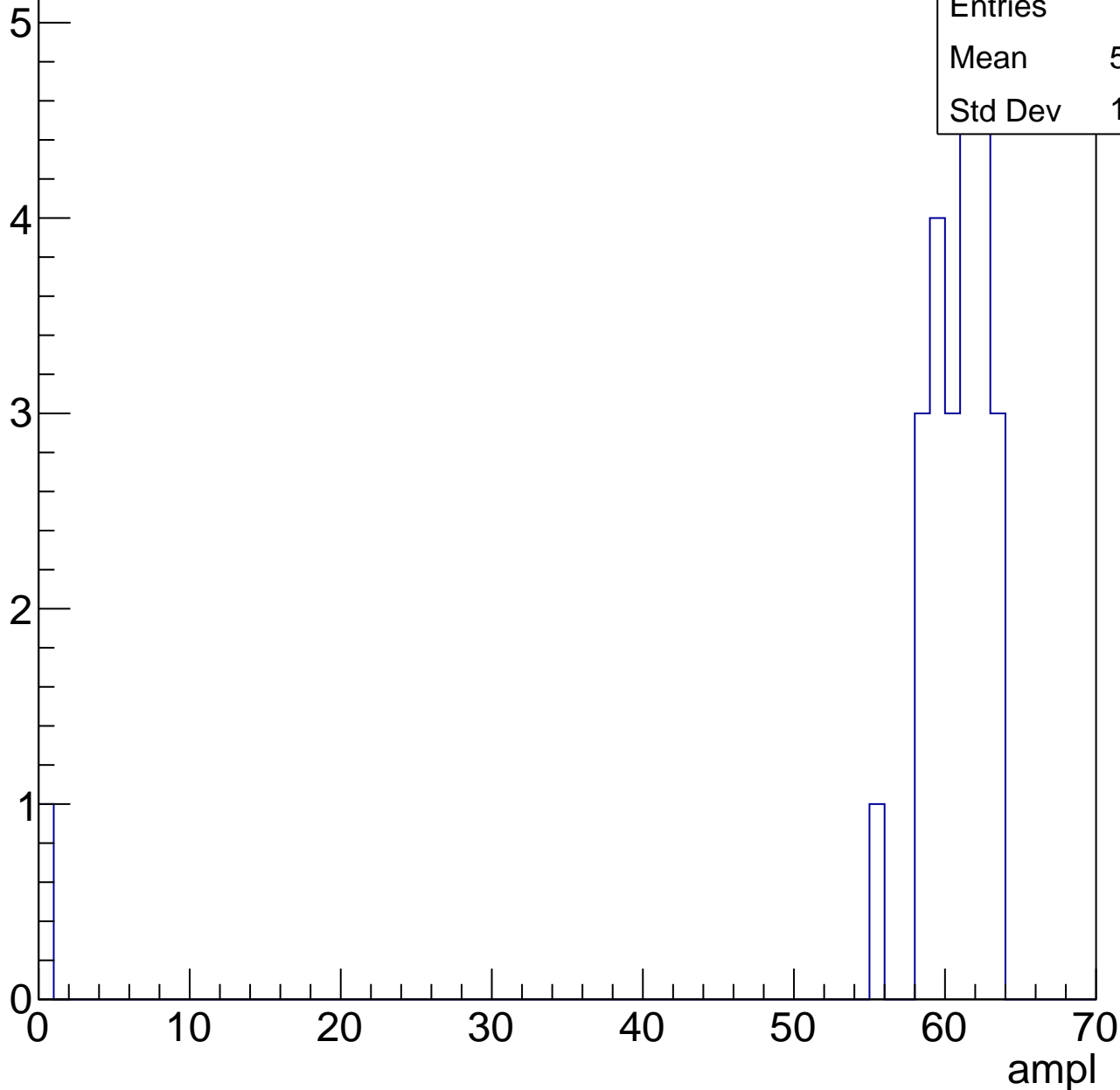


# B1L103S, U1-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	25
Mean	57.96
Std Dev	11.98



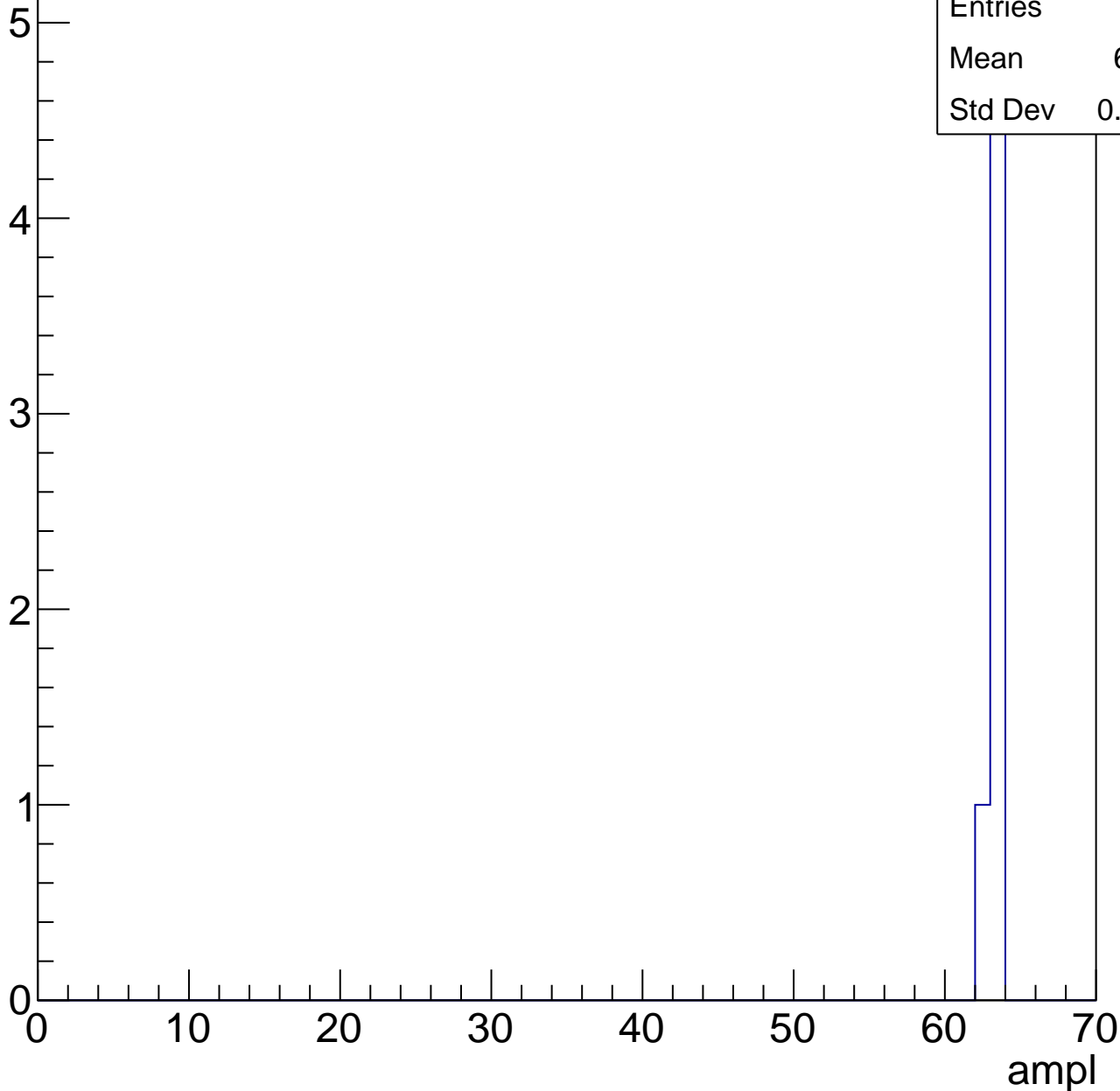


# B1L103S, U1-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	6
Mean	62.83
Std Dev	0.3727



# B1L103S, U1-ch65, adc0

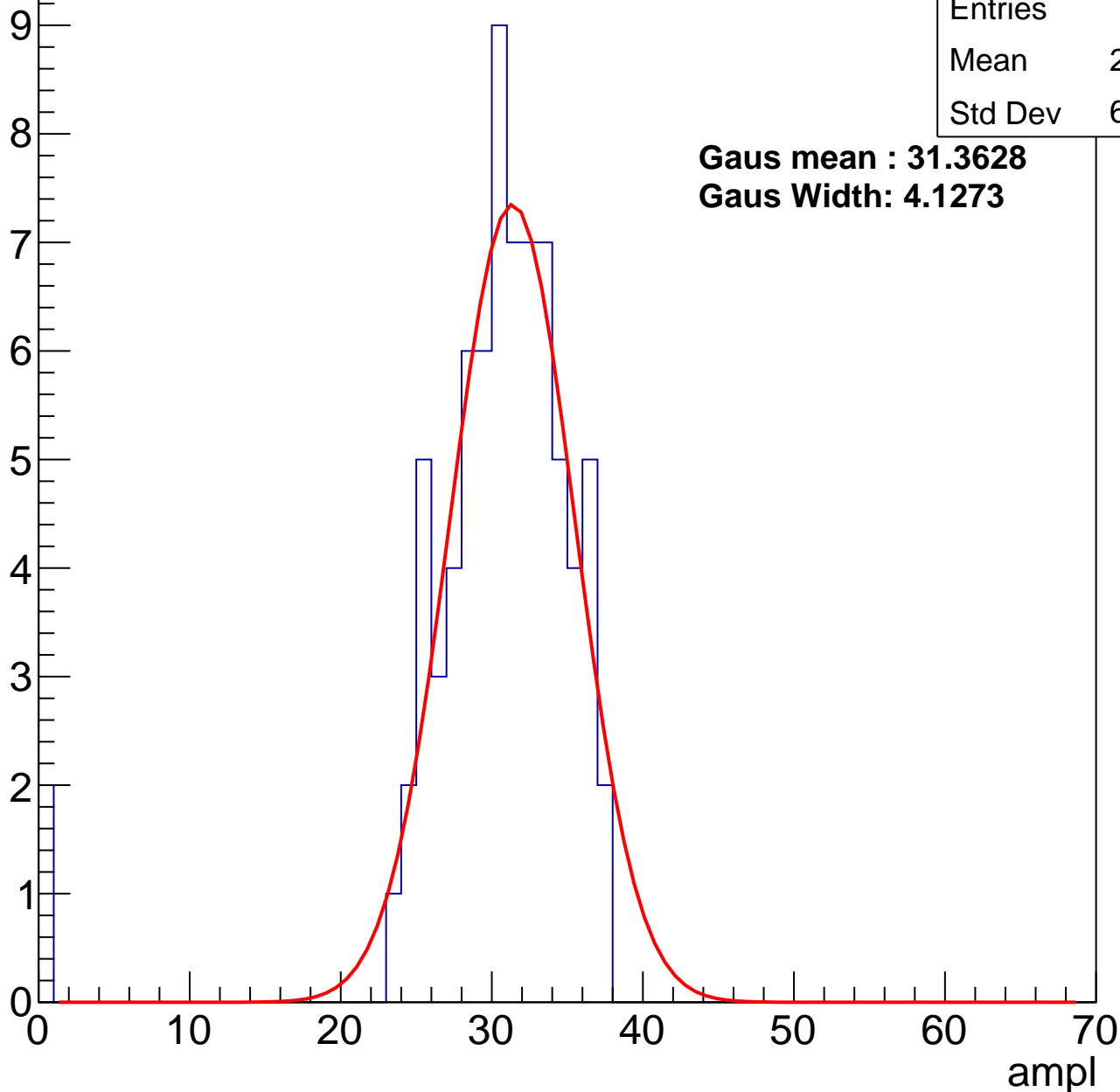
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	29.73
Std Dev	6.012

**Gaus mean : 31.3628**

**Gaus Width: 4.1273**



# B1L103S, U1-ch65, adc1

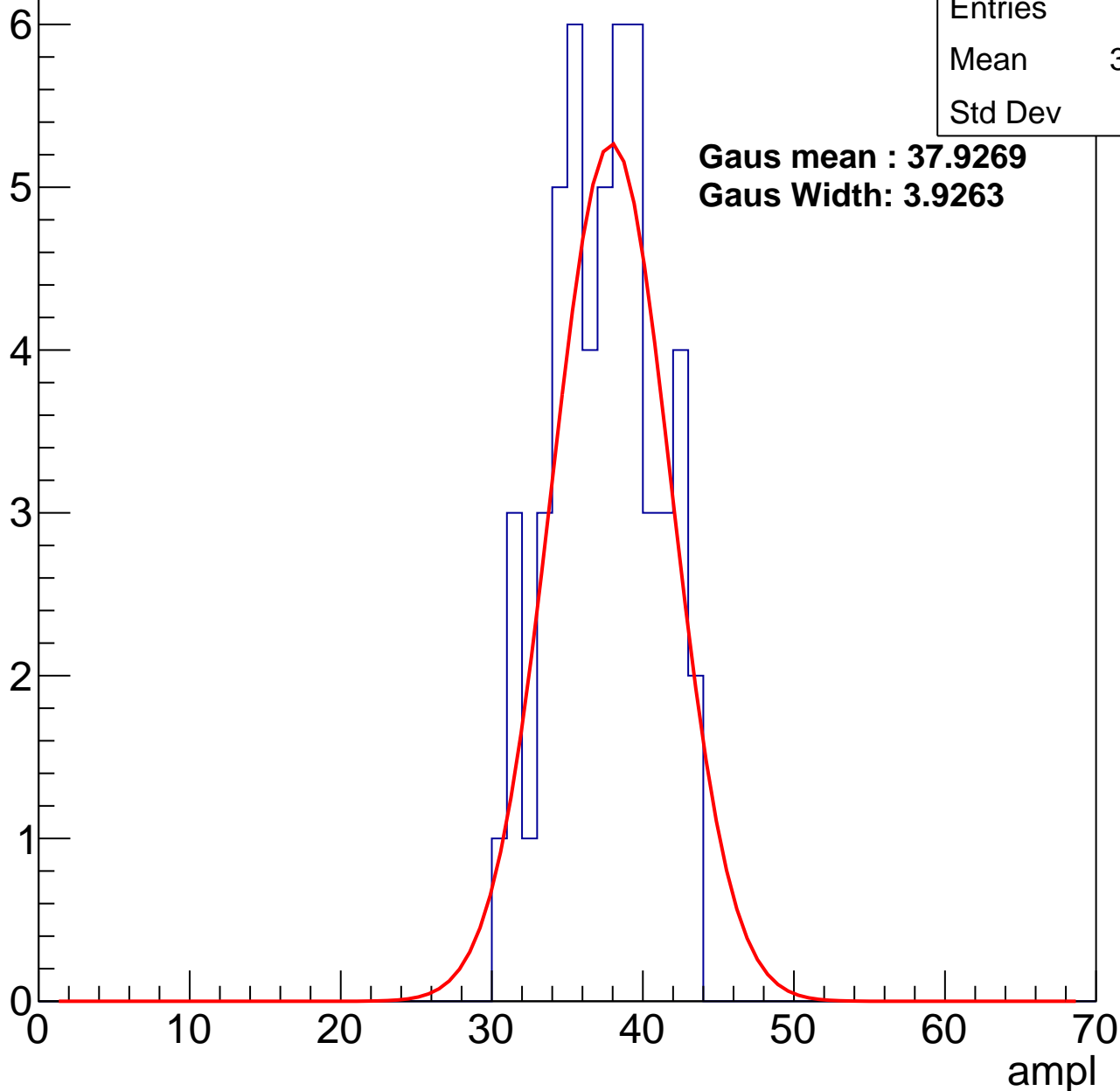
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	36.96
Std Dev	3.34

**Gaus mean : 37.9269**

**Gaus Width: 3.9263**



# B1L103S, U1-ch65, adc2

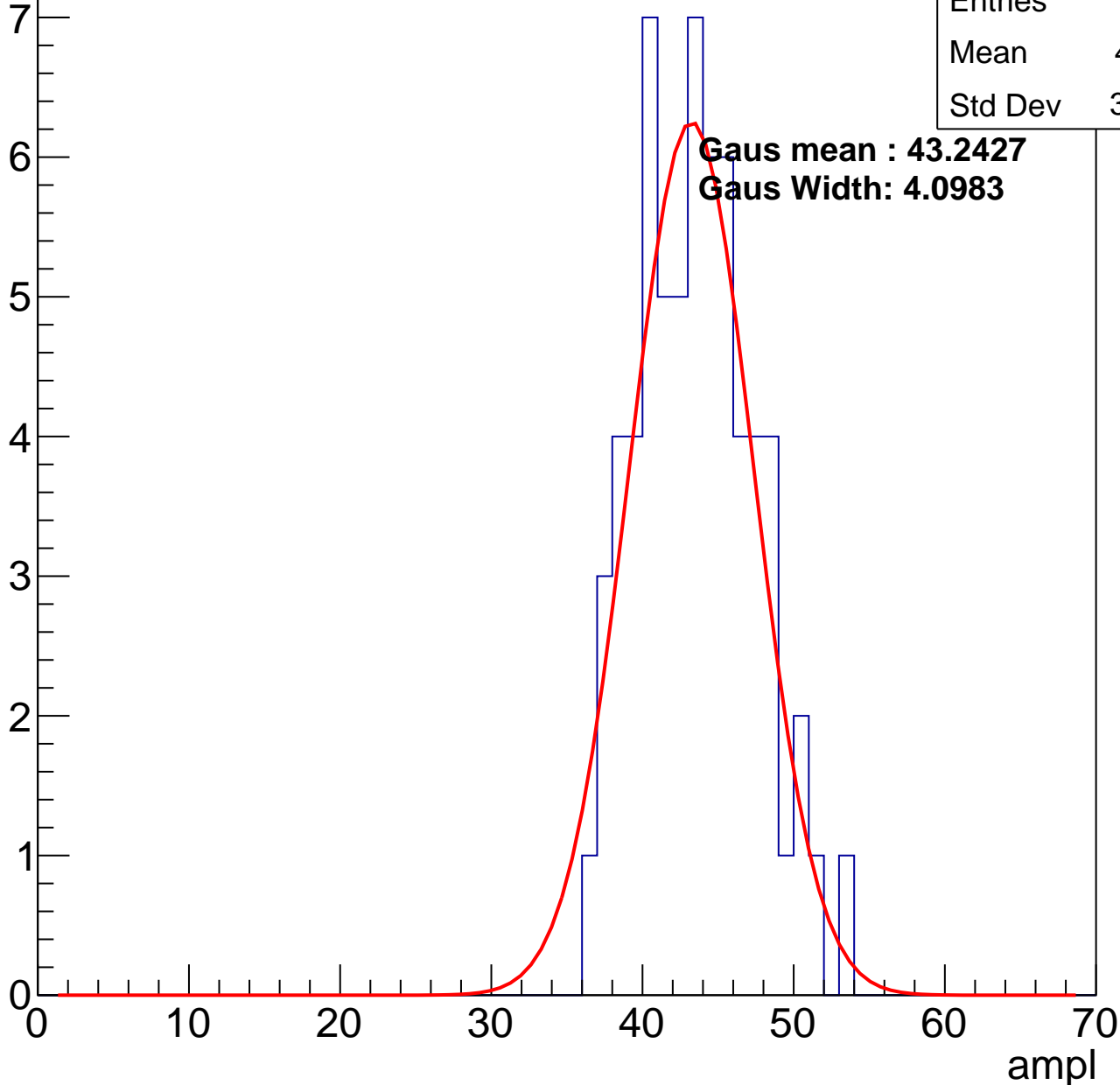
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	43.11
Std Dev	3.795

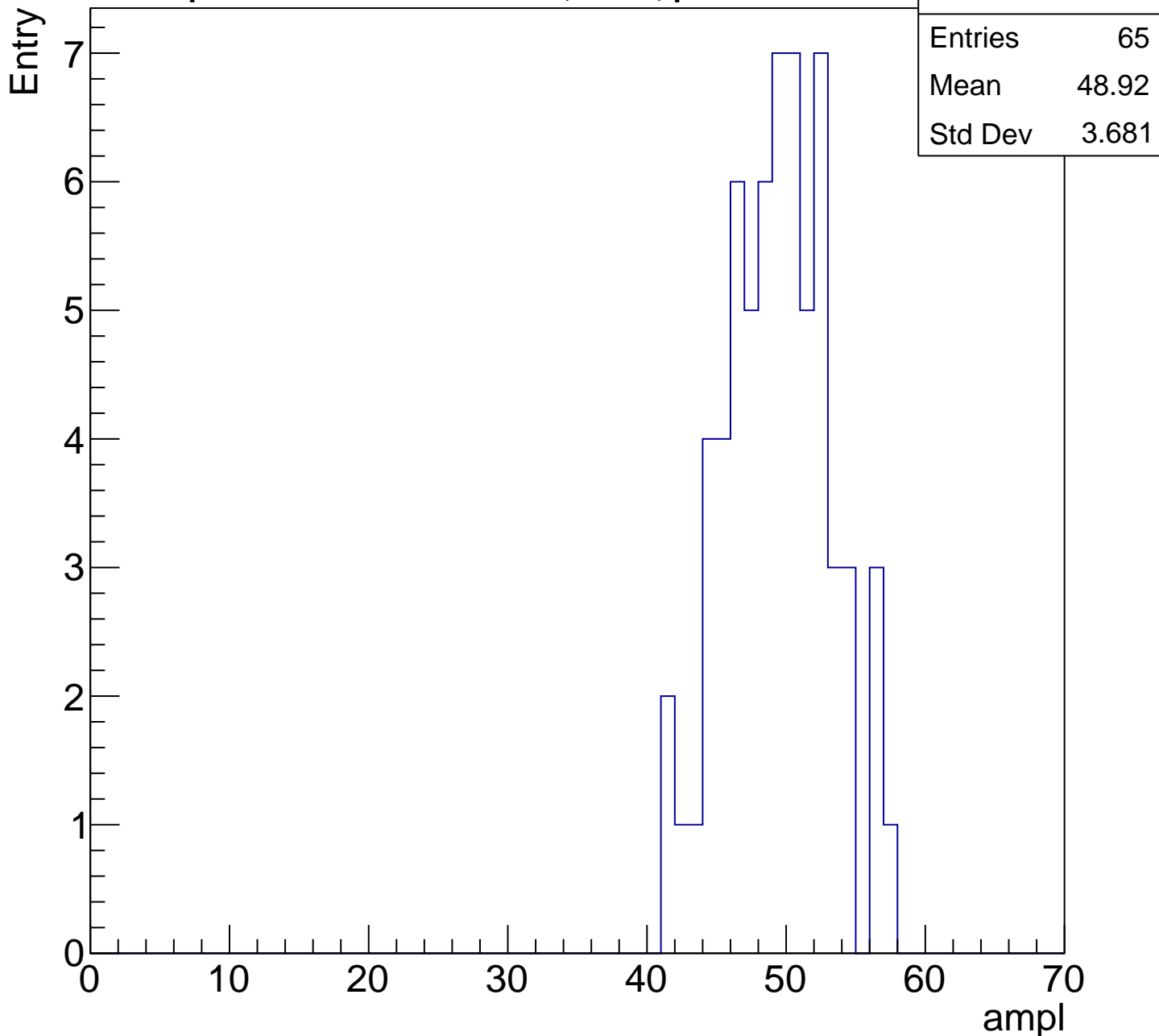
**Gaus mean : 43.2427**

**Gaus Width: 4.0983**



# B1L103S, U1-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

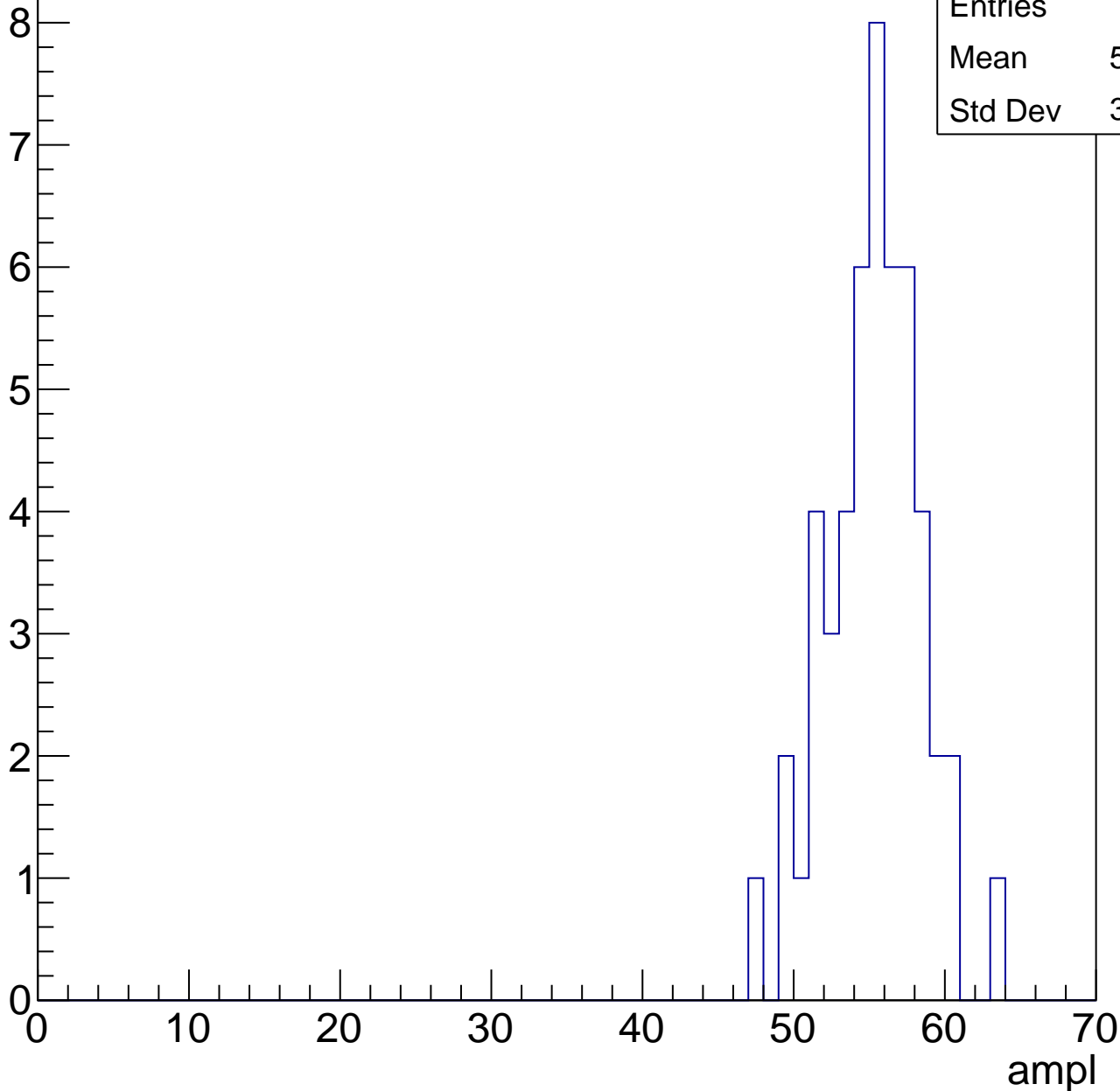


# B1L103S, U1-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	54.84
Std Dev	3.114

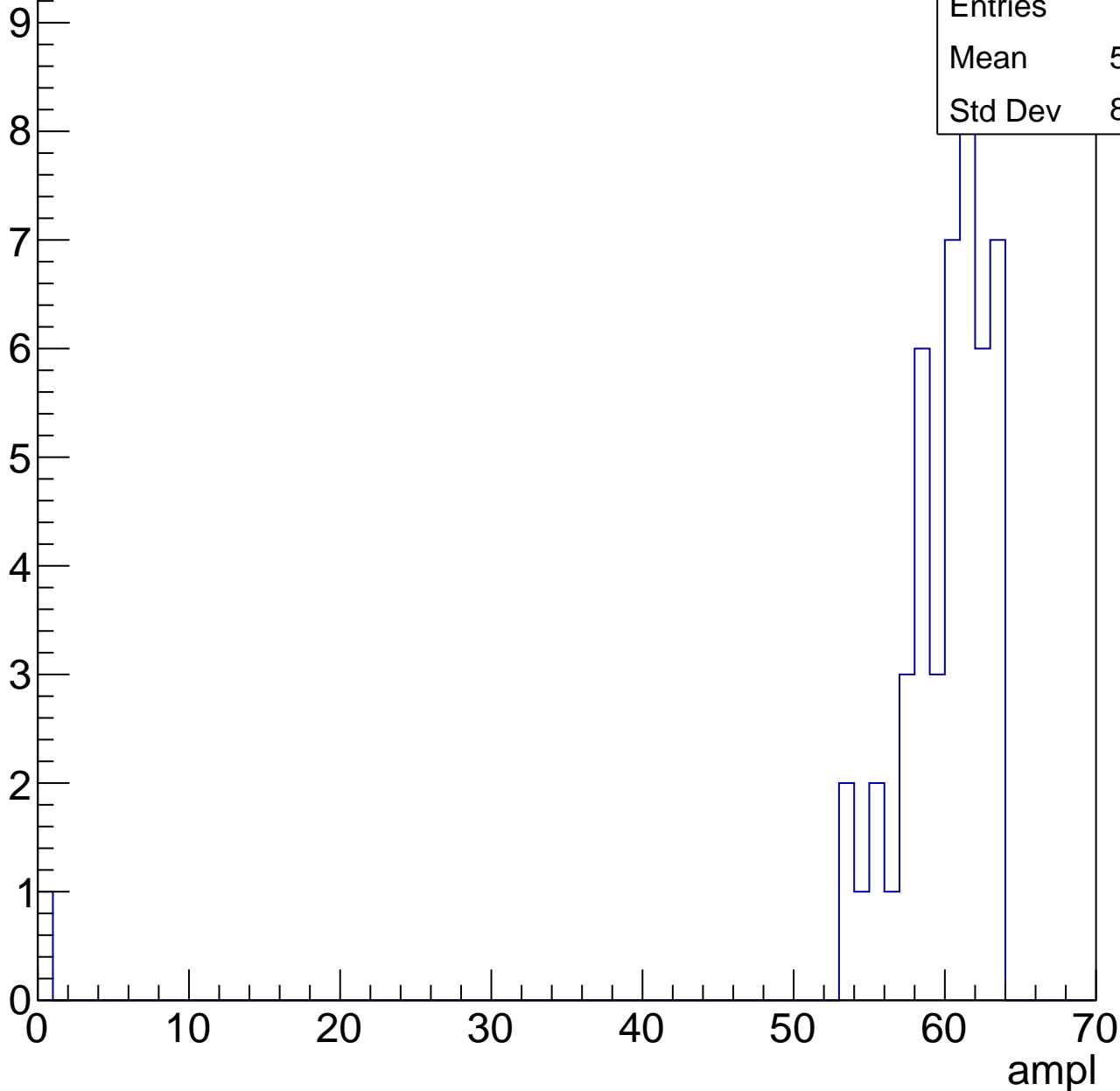


# B1L103S, U1-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	58.42
Std Dev	8.932

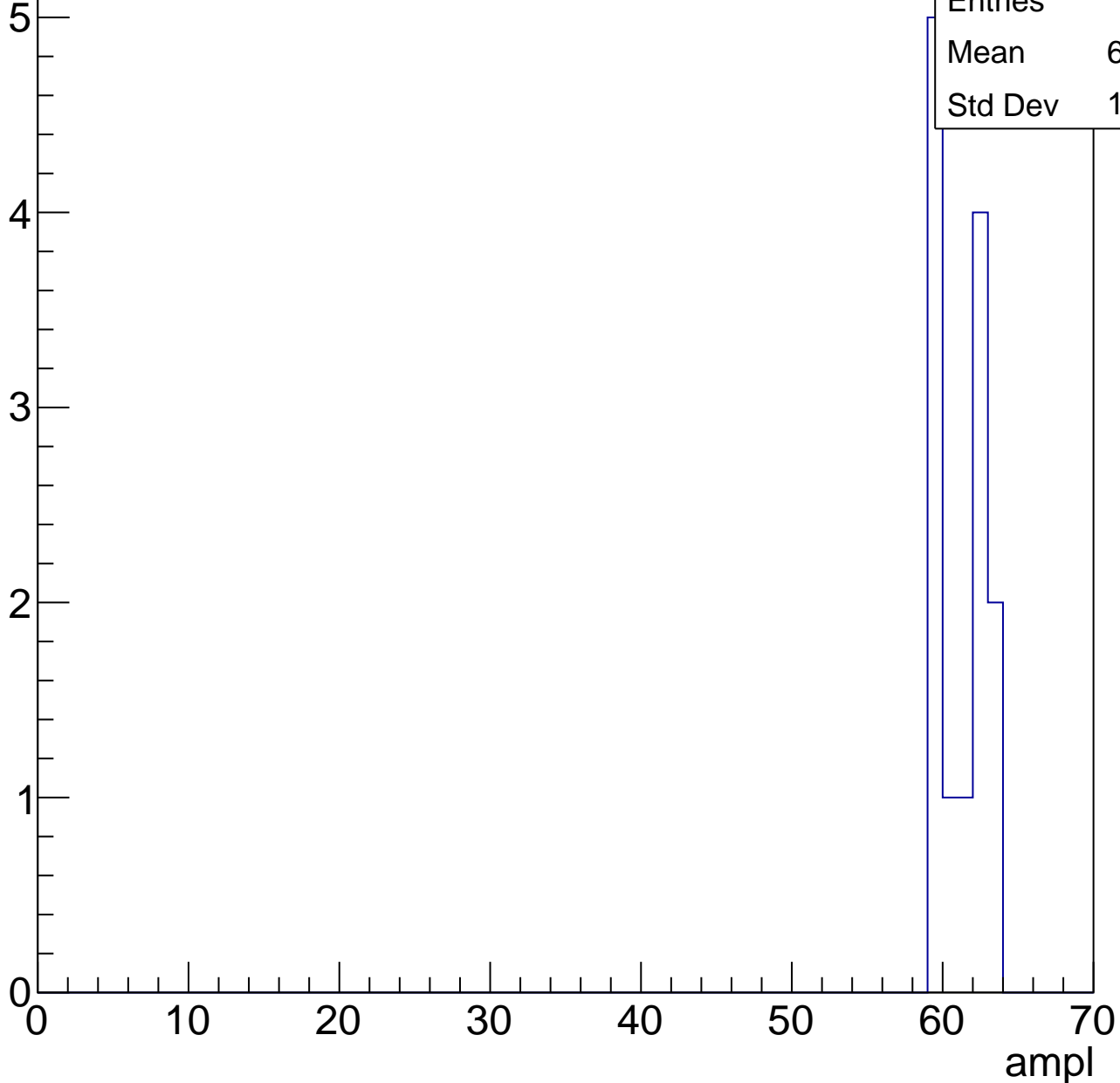


# B1L103S, U1-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	13
Mean	60.77
Std Dev	1.576





# B1L103S, U1-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch66, adc0

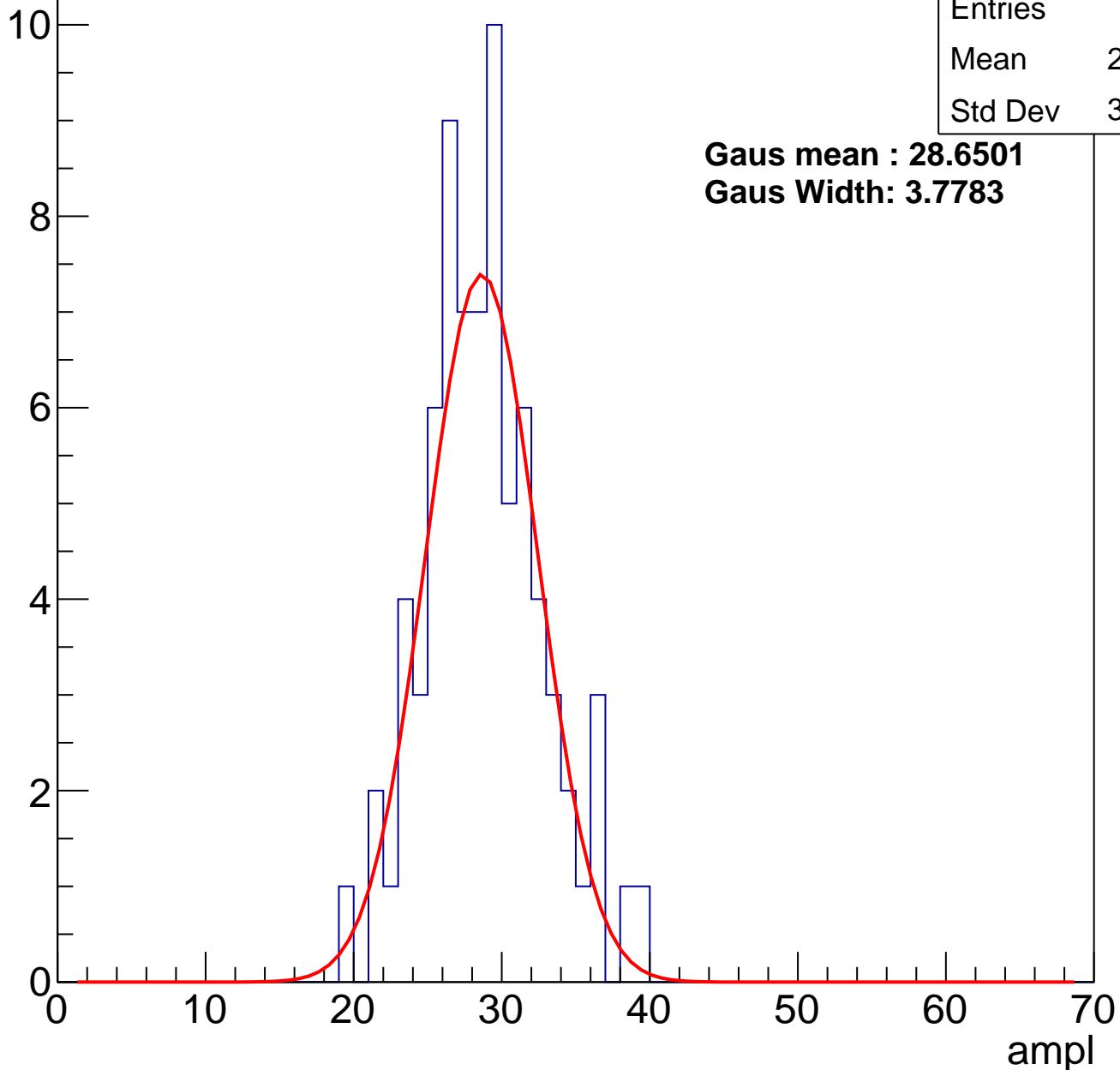
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	76
Mean	28.38
Std Dev	3.983

**Gaus mean : 28.6501**

**Gaus Width: 3.7783**

Entry



# B1L103S, U1-ch66, adc1

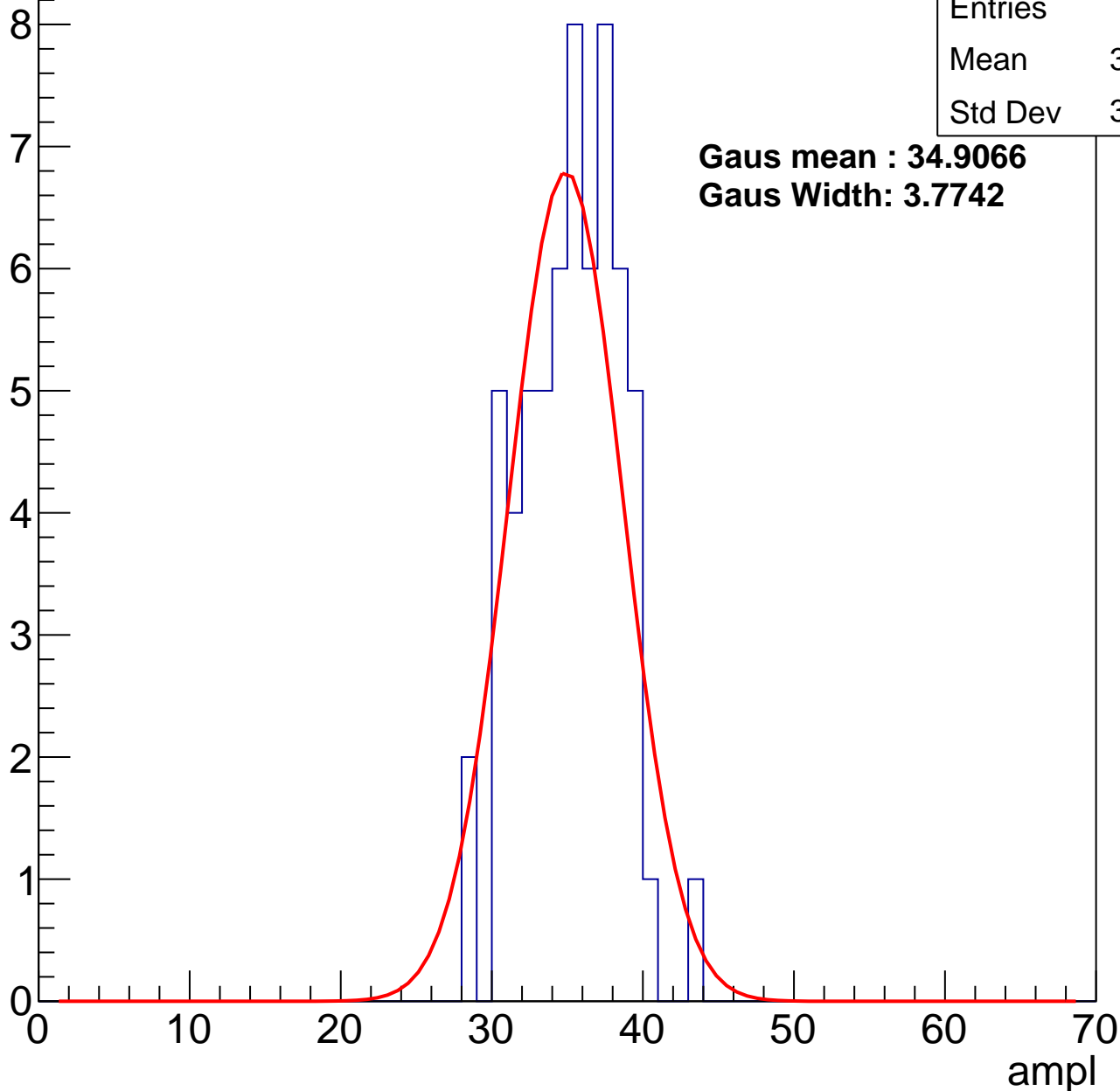
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	34.79
Std Dev	3.153

**Gaus mean : 34.9066**

**Gaus Width: 3.7742**



# B1L103S, U1-ch66, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	66
Mean	41.44
Std Dev	3.826

**Gaus mean : 42.3986**

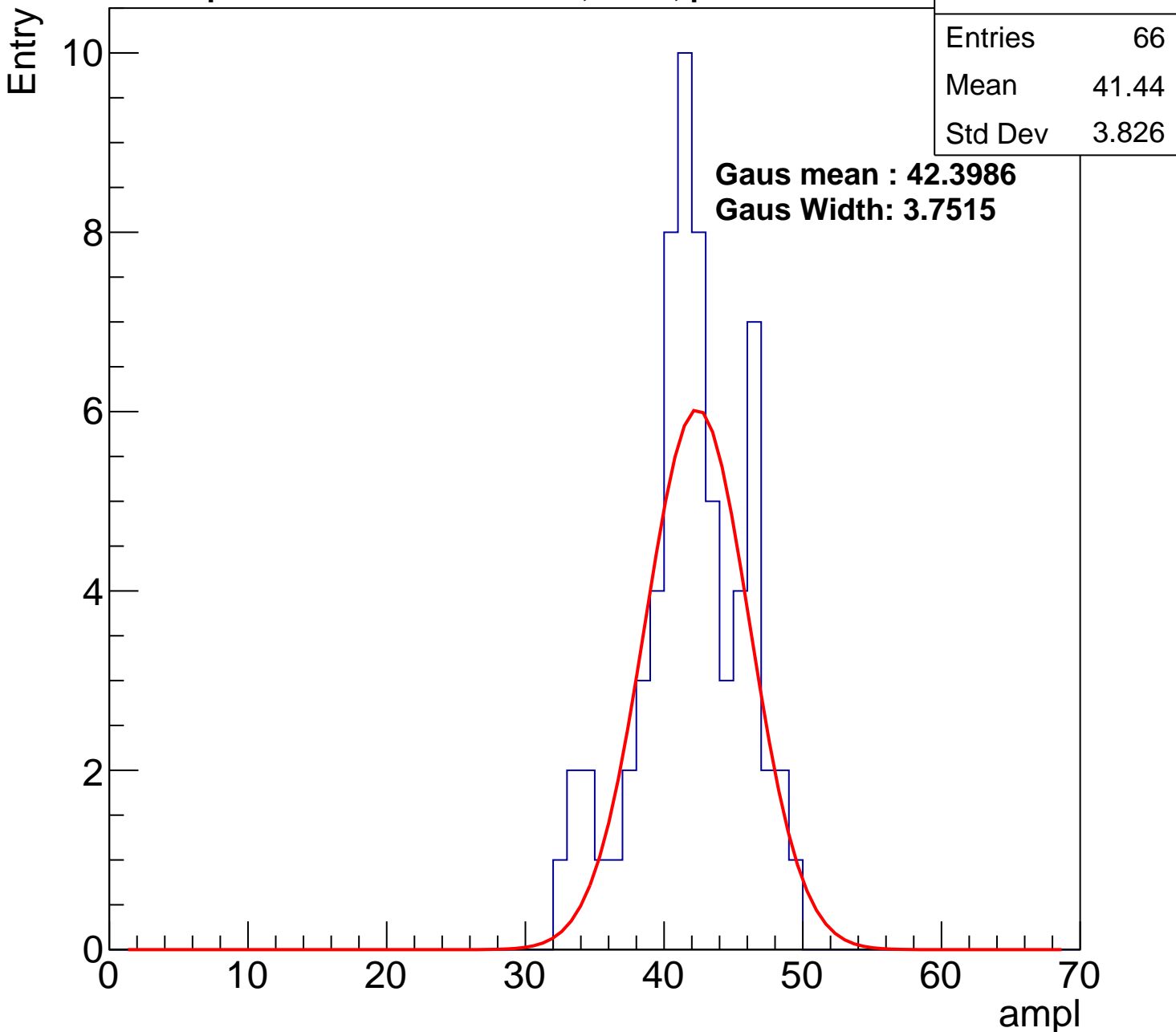
**Gaus Width: 3.7515**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

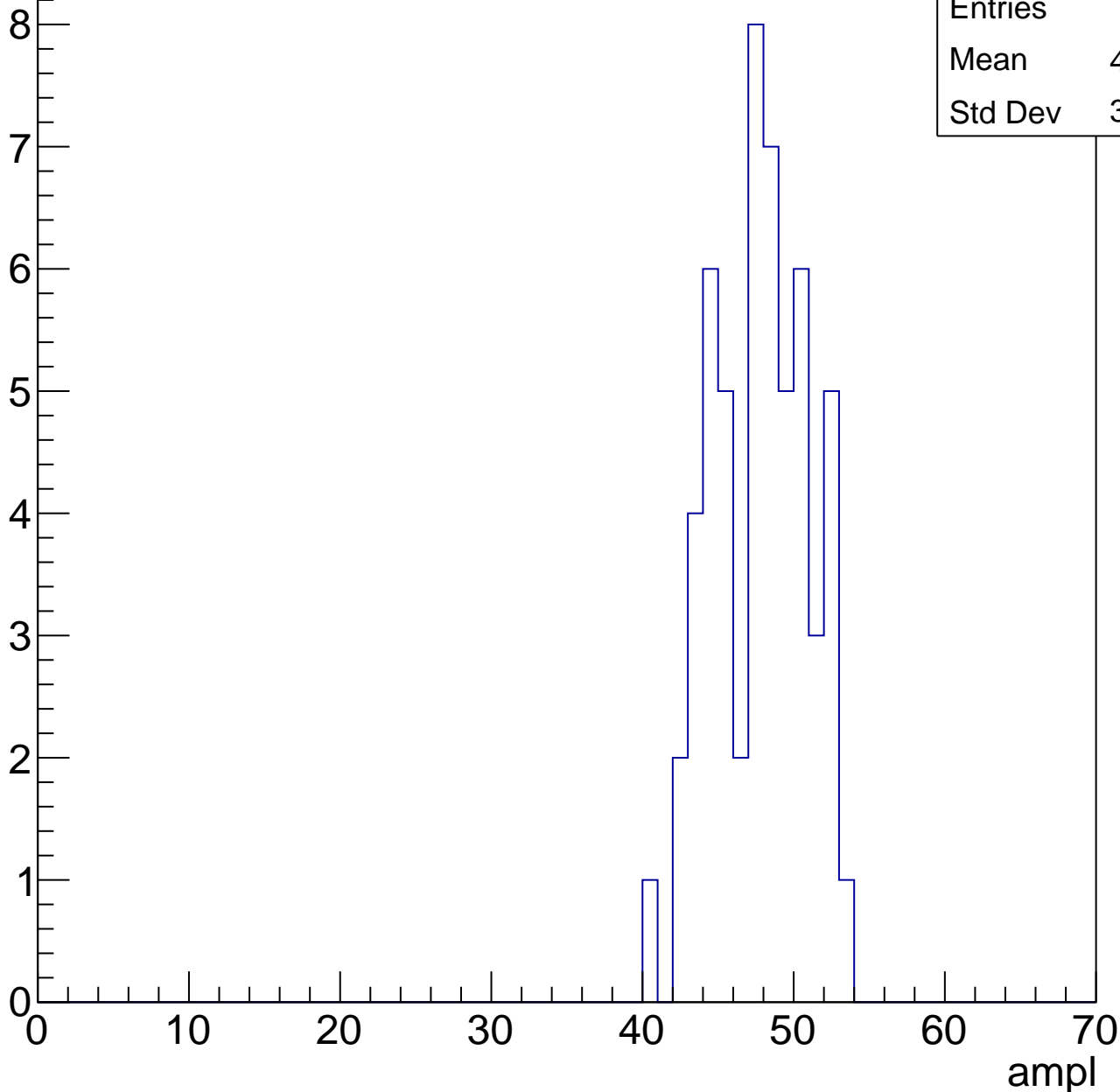


# B1L103S, U1-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	47.27
Std Dev	3.089

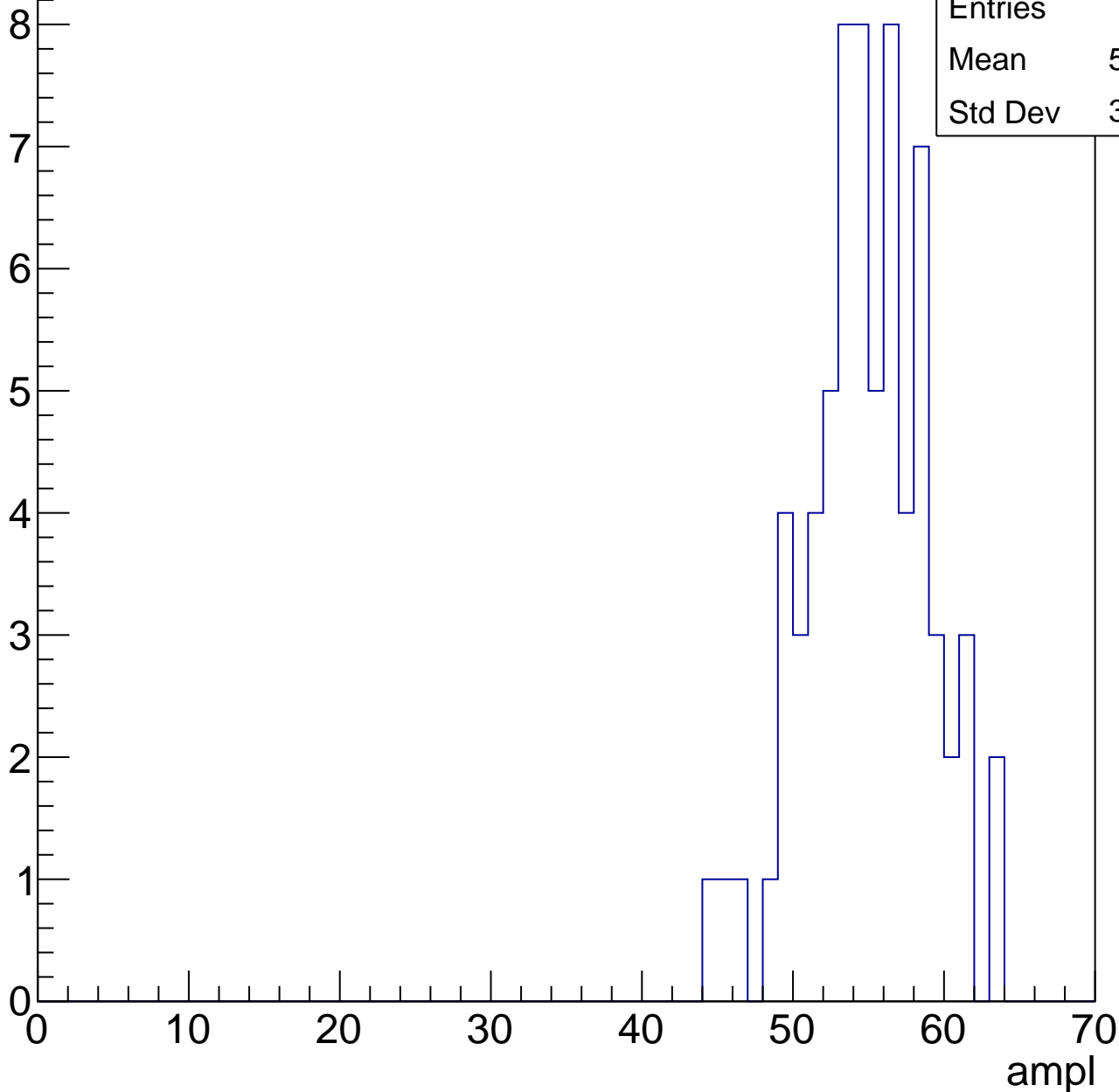


# B1L103S, U1-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	54.46
Std Dev	3.999

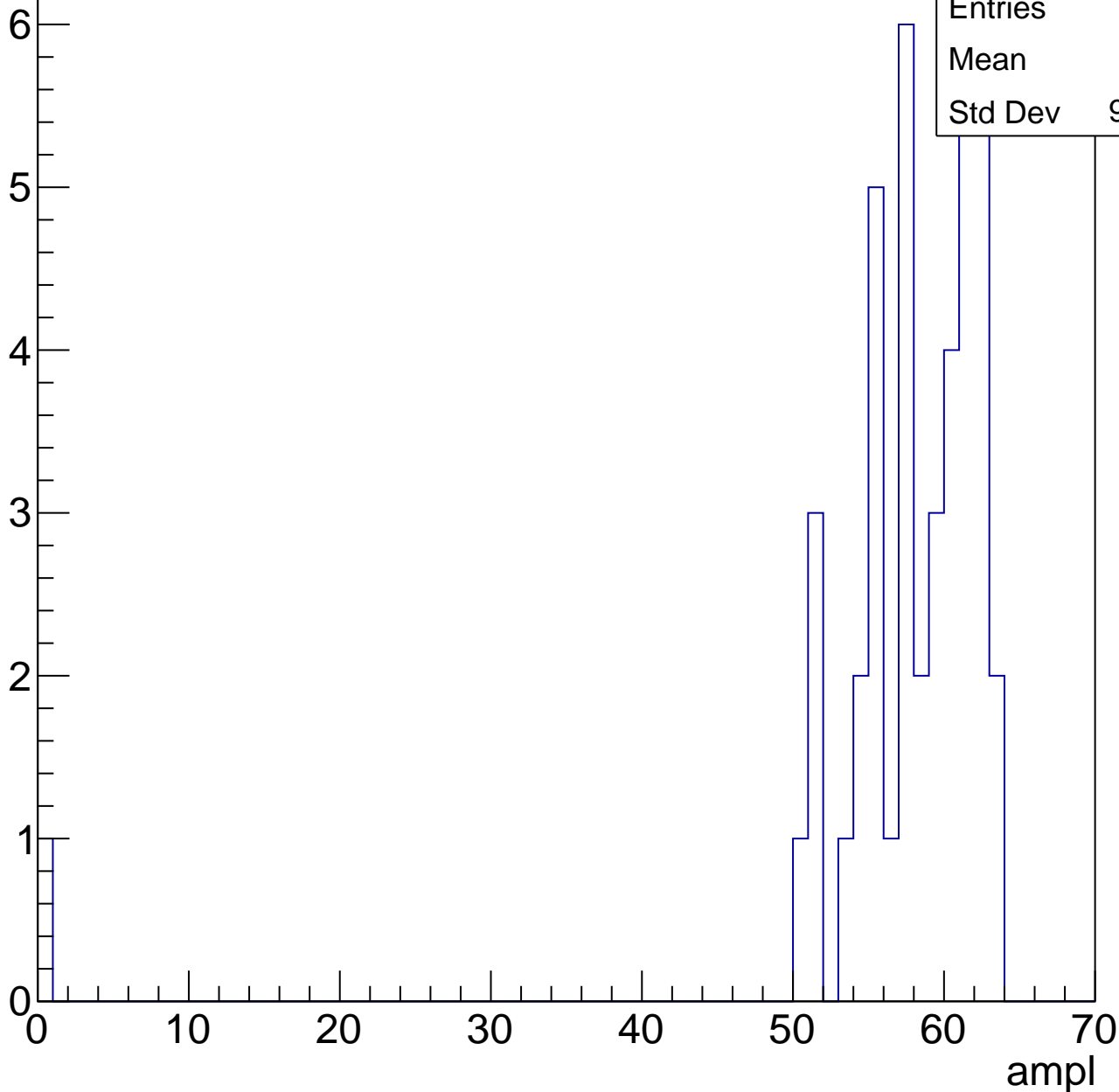


# B1L103S, U1-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	43
Mean	56.6
Std Dev	9.428

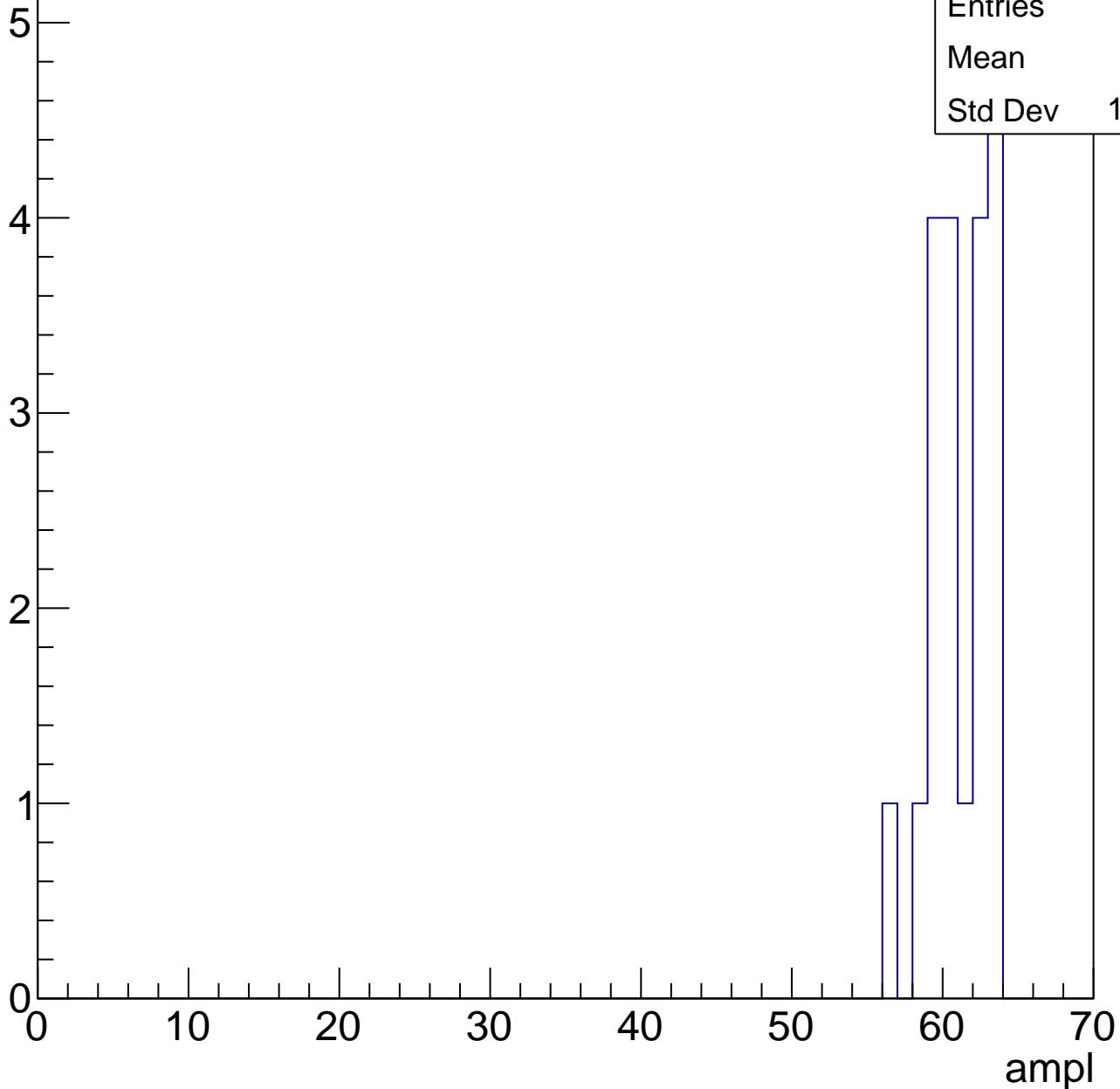


# B1L103S, U1-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	20
Mean	60.7
Std Dev	1.952





# B1L103S, U1-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch67, adc0

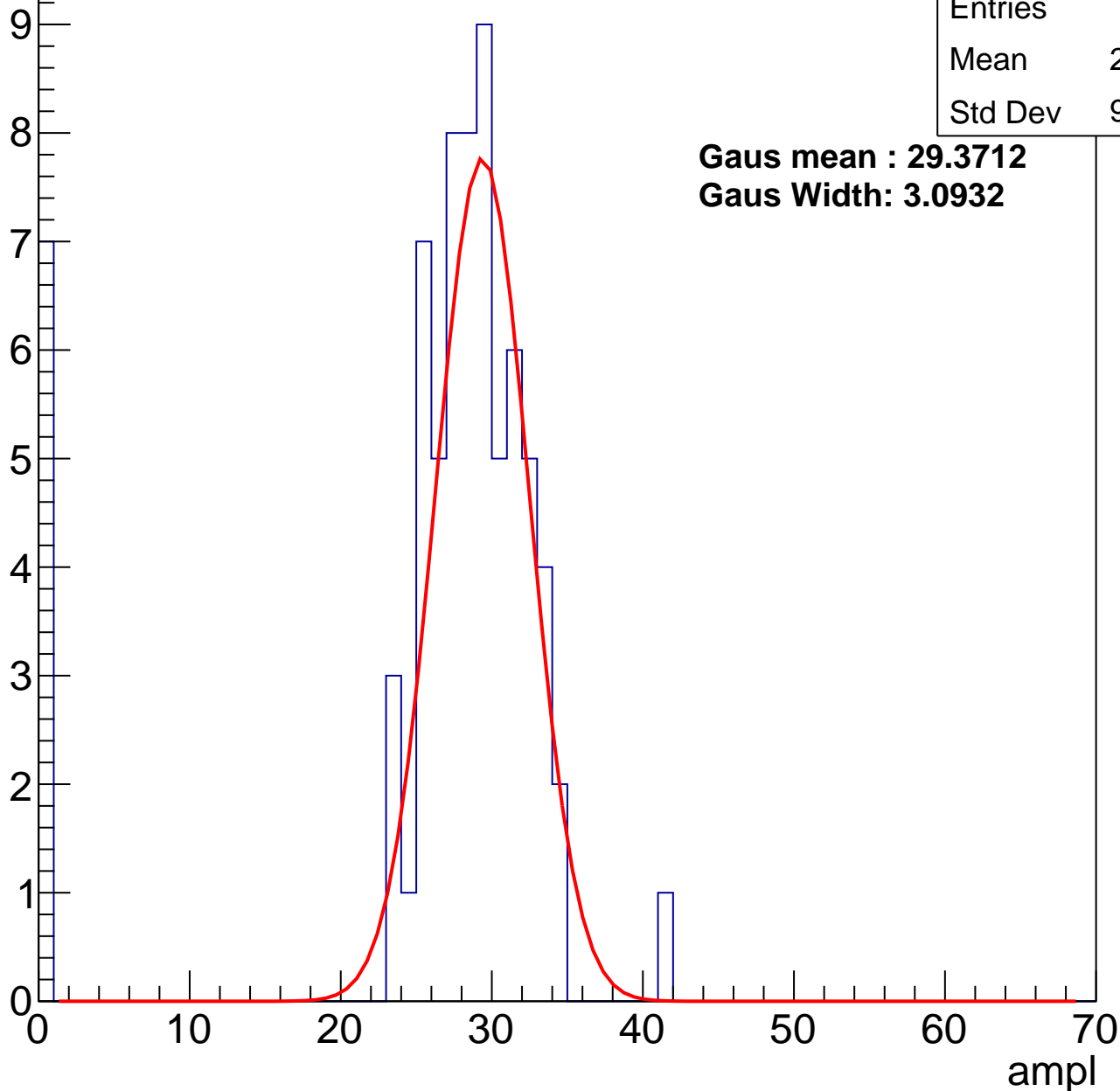
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	25.86
Std Dev	9.076

**Gaus mean : 29.3712**

**Gaus Width: 3.0932**



# B1L103S, U1-ch67, adc1

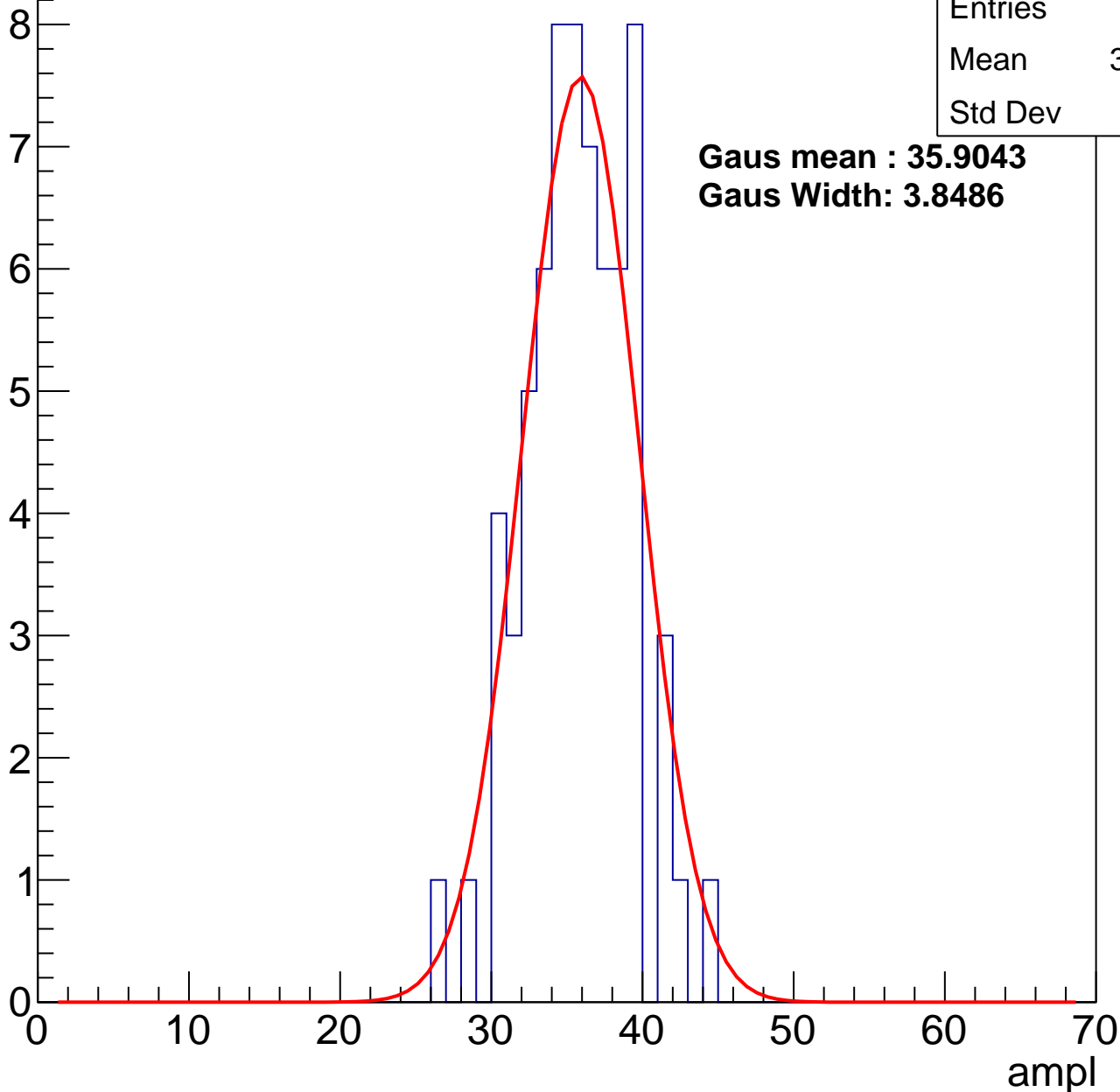
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	35.29
Std Dev	3.43

**Gaus mean : 35.9043**

**Gaus Width: 3.8486**



# B1L103S, U1-ch67, adc2

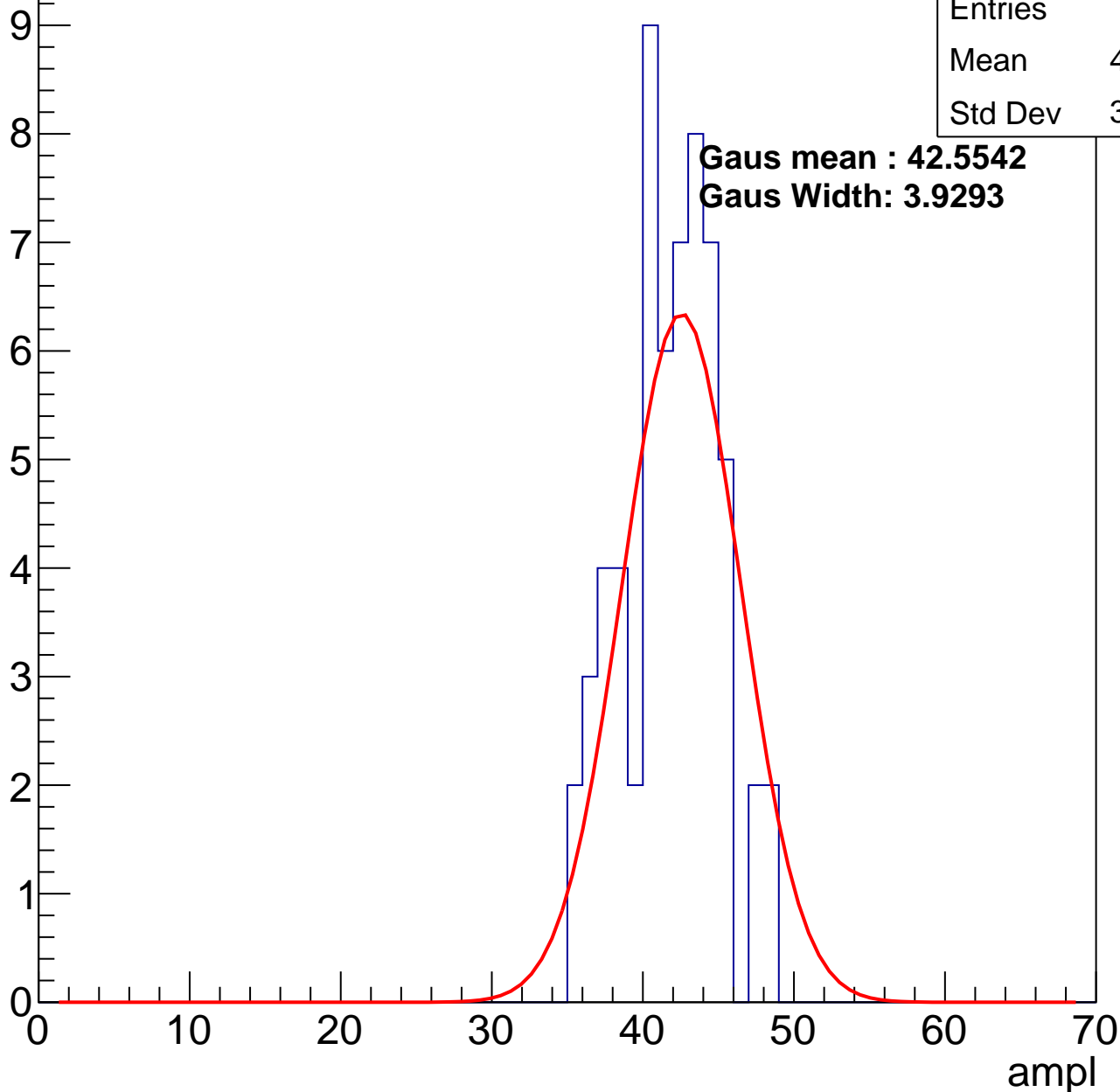
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	41.36
Std Dev	3.157

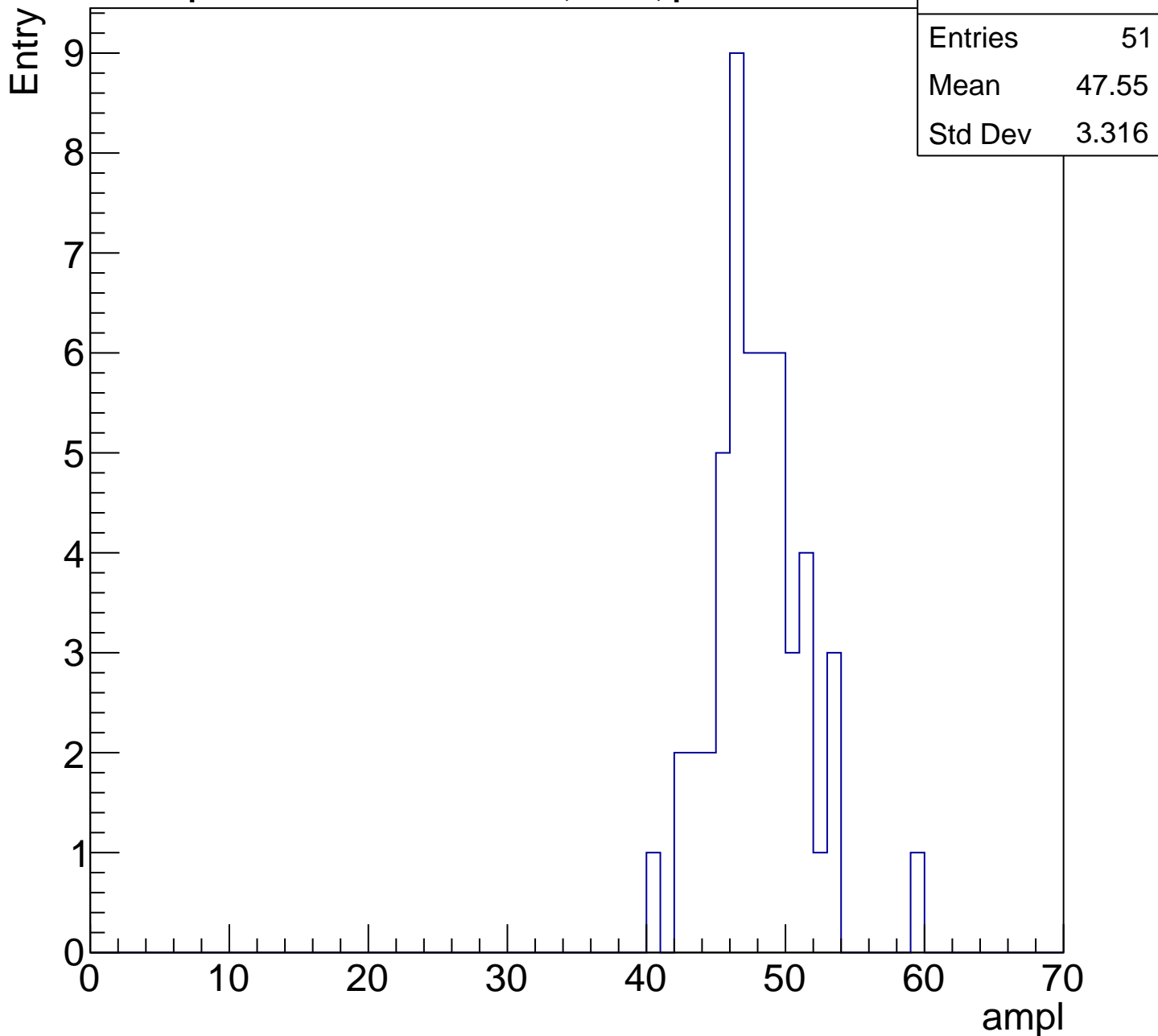
**Gaus mean : 42.5542**

**Gaus Width: 3.9293**



# B1L103S, U1-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

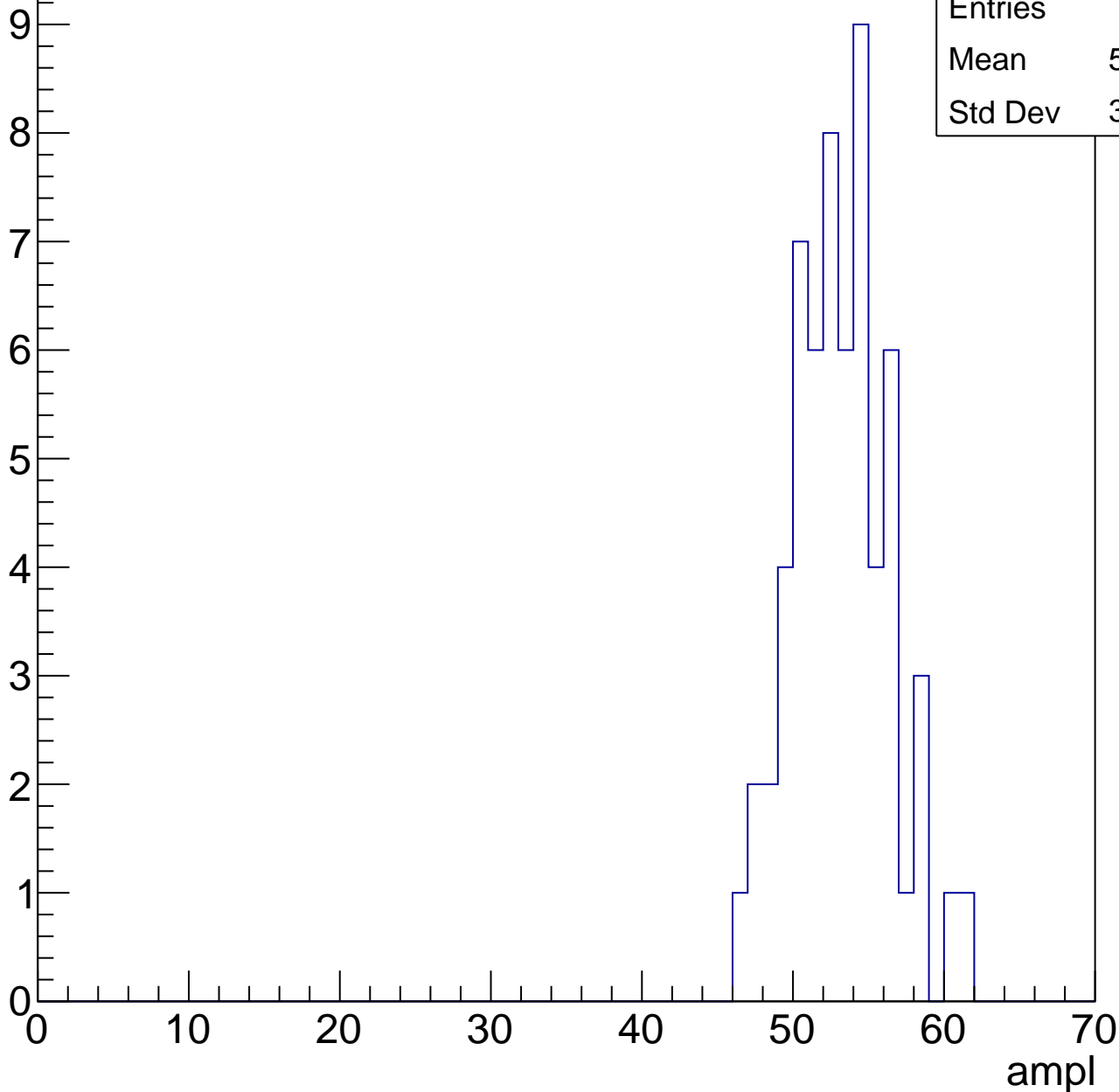


# B1L103S, U1-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

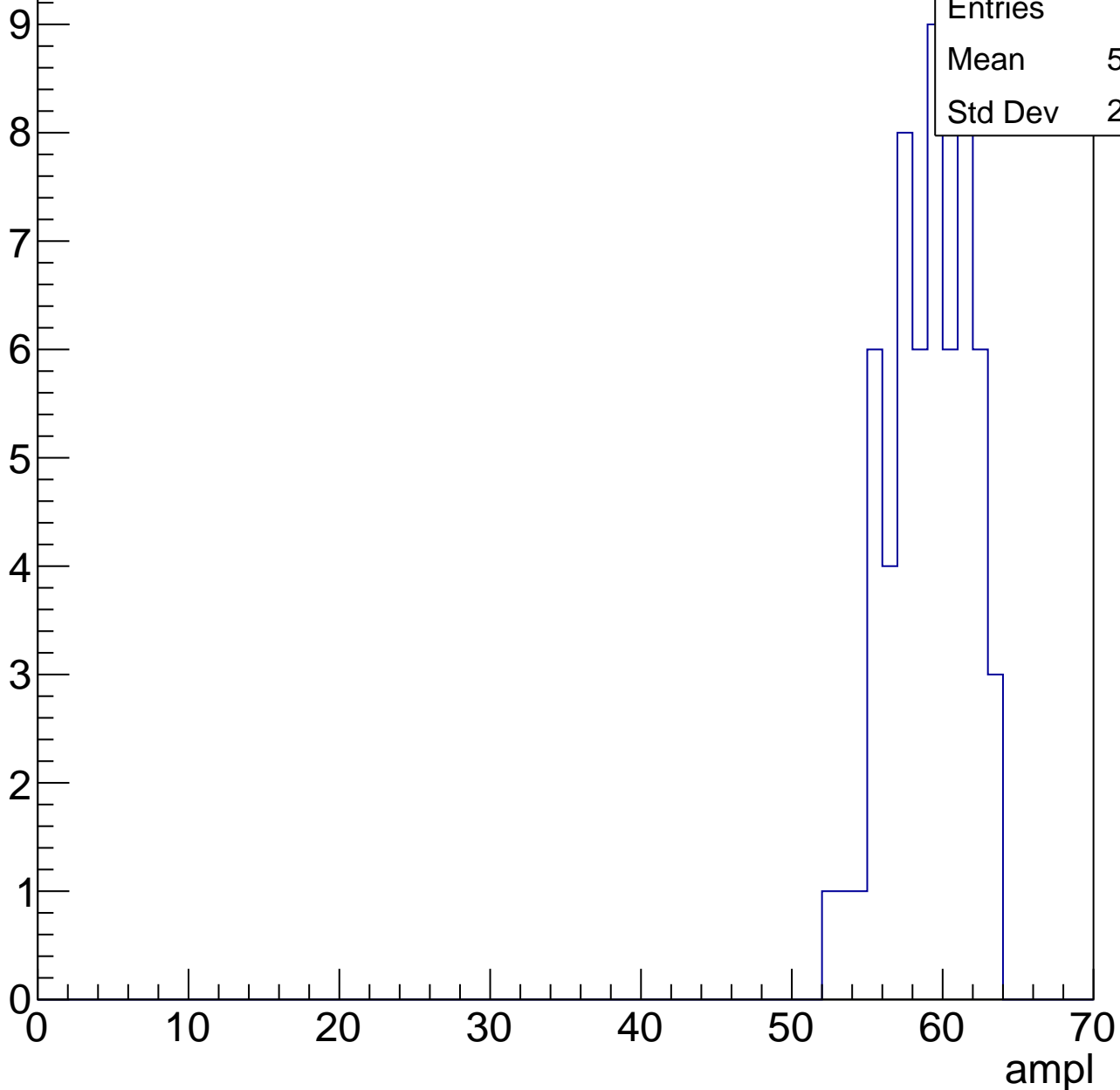
Entries	61
Mean	52.72
Std Dev	3.158



# B1L103S, U1-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



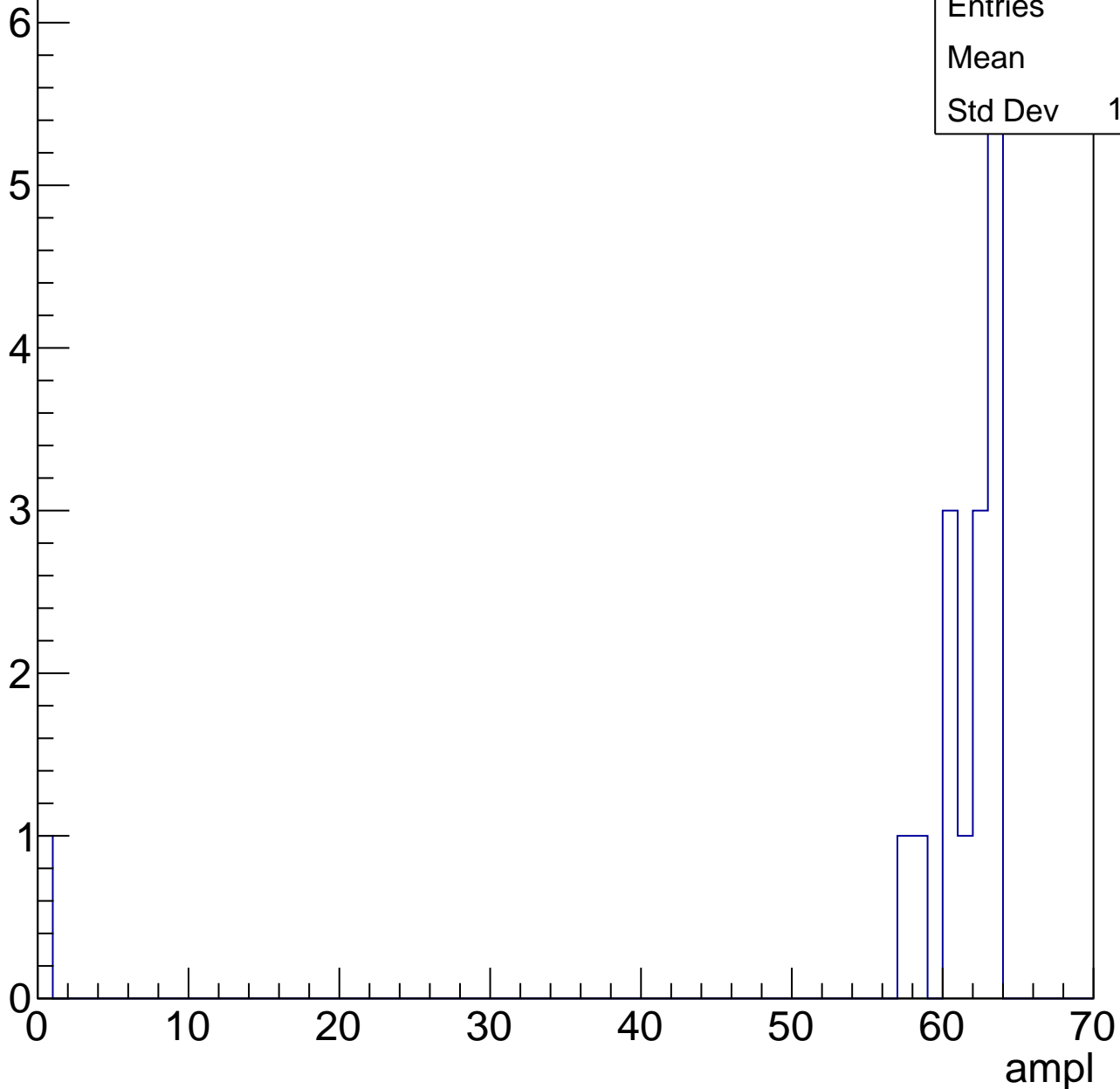
Entries	59
Mean	58.59
Std Dev	2.637

# B1L103S, U1-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	16
Mean	57.5
Std Dev	14.96

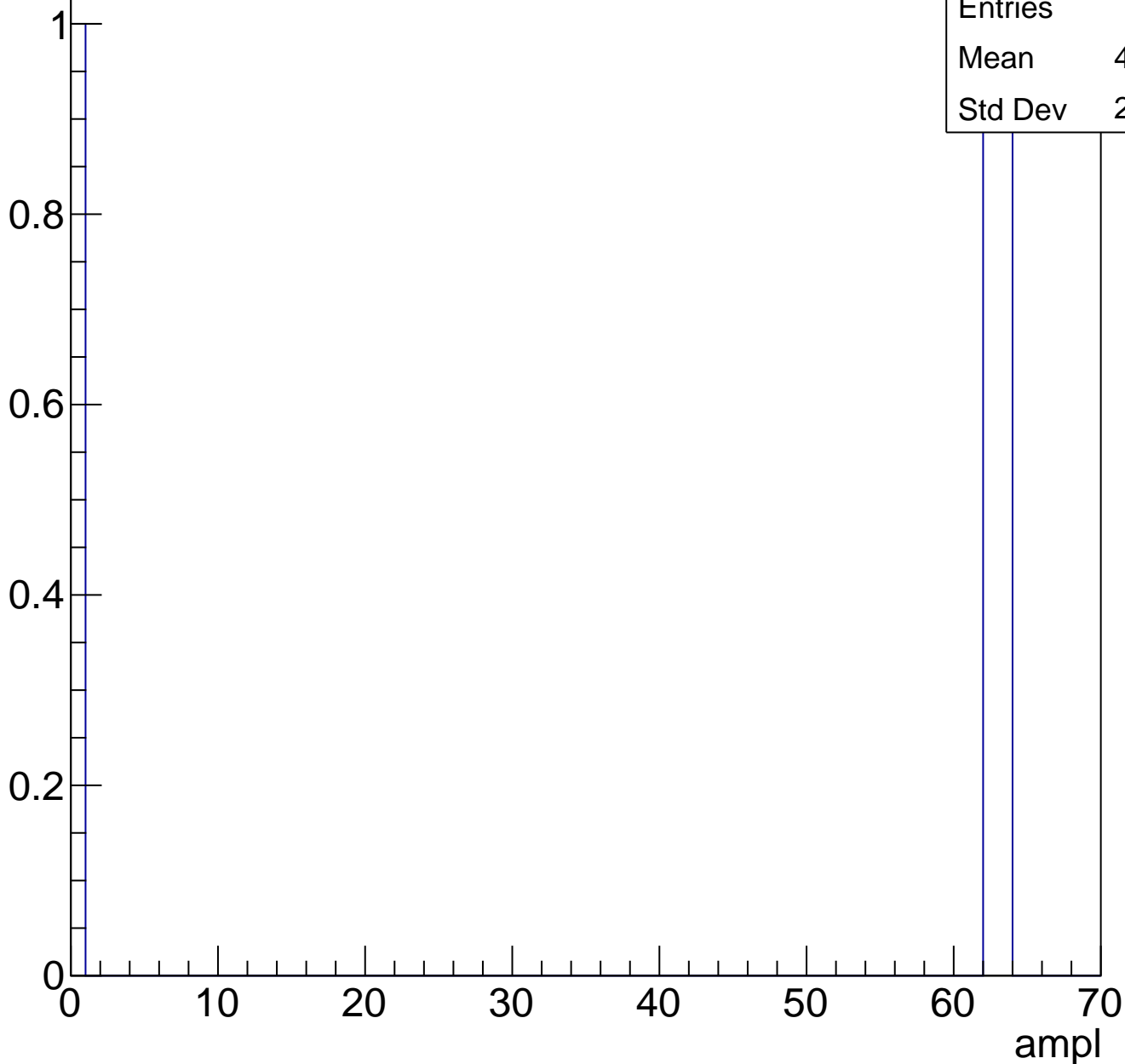




# B1L103S, U1-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch68, adc0

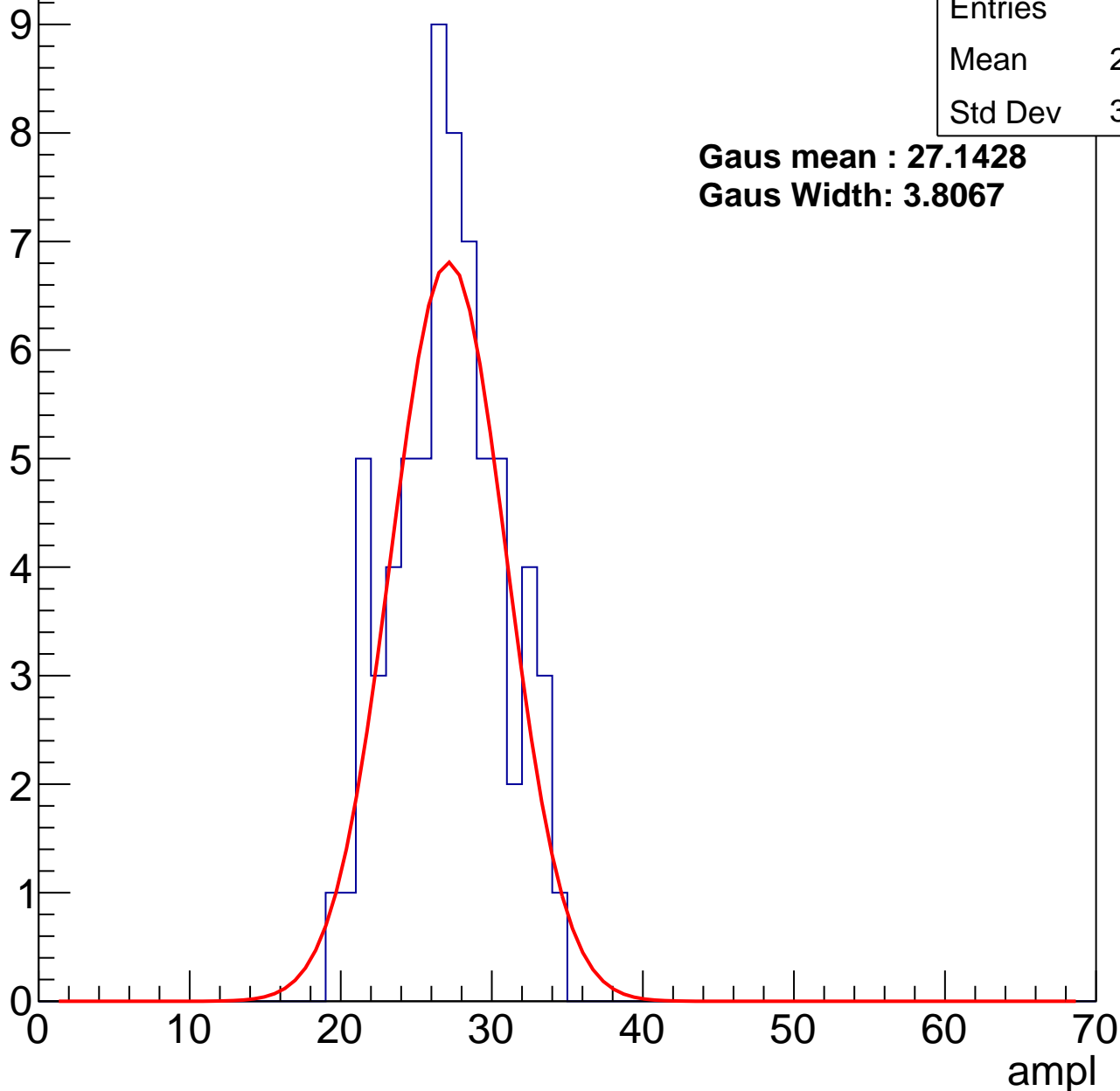
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	26.63
Std Dev	3.552

**Gaus mean : 27.1428**

**Gaus Width: 3.8067**



# B1L103S, U1-ch68, adc1

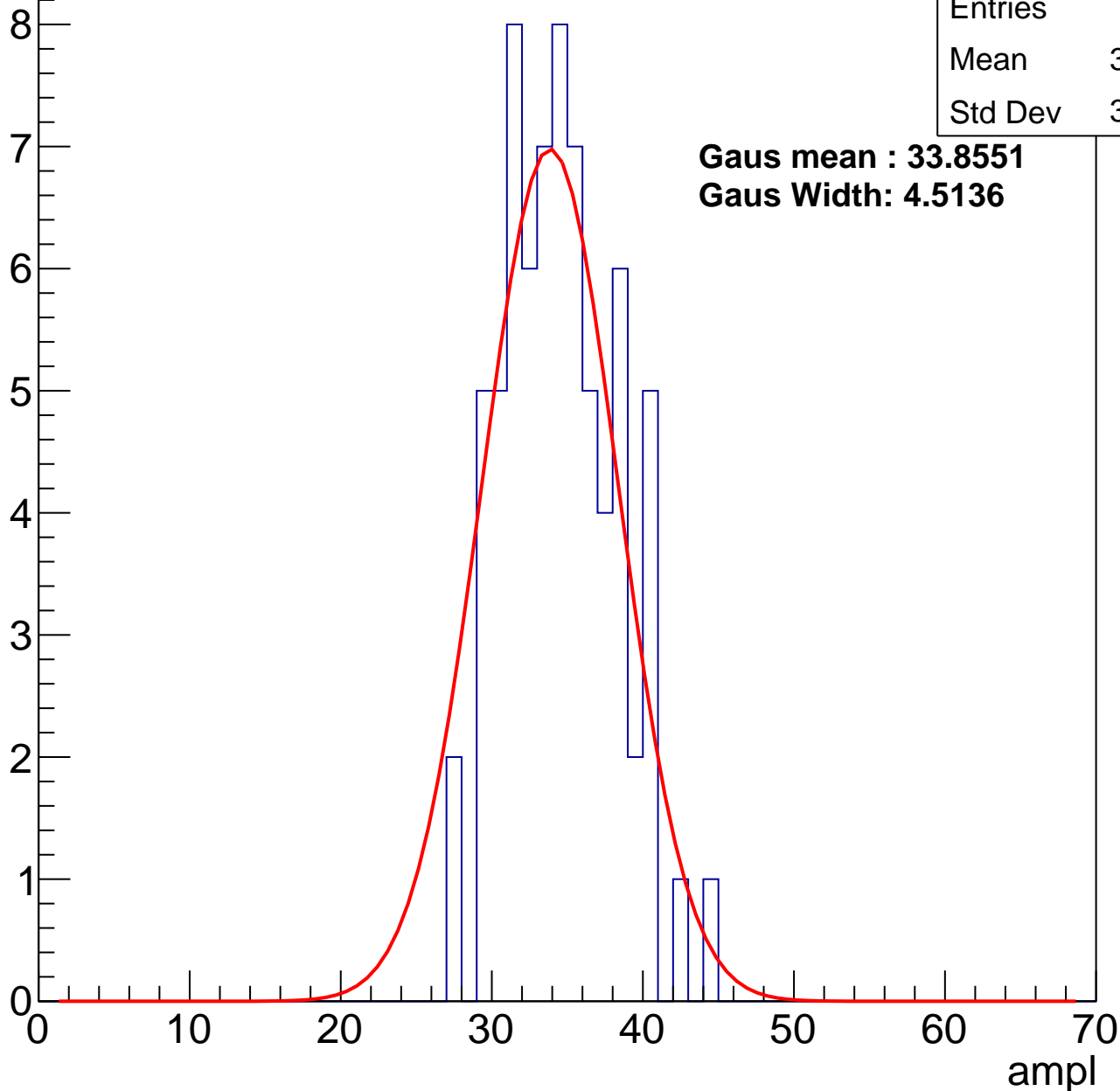
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	34.12
Std Dev	3.647

**Gaus mean : 33.8551**

**Gaus Width: 4.5136**



# B1L103S, U1-ch68, adc2

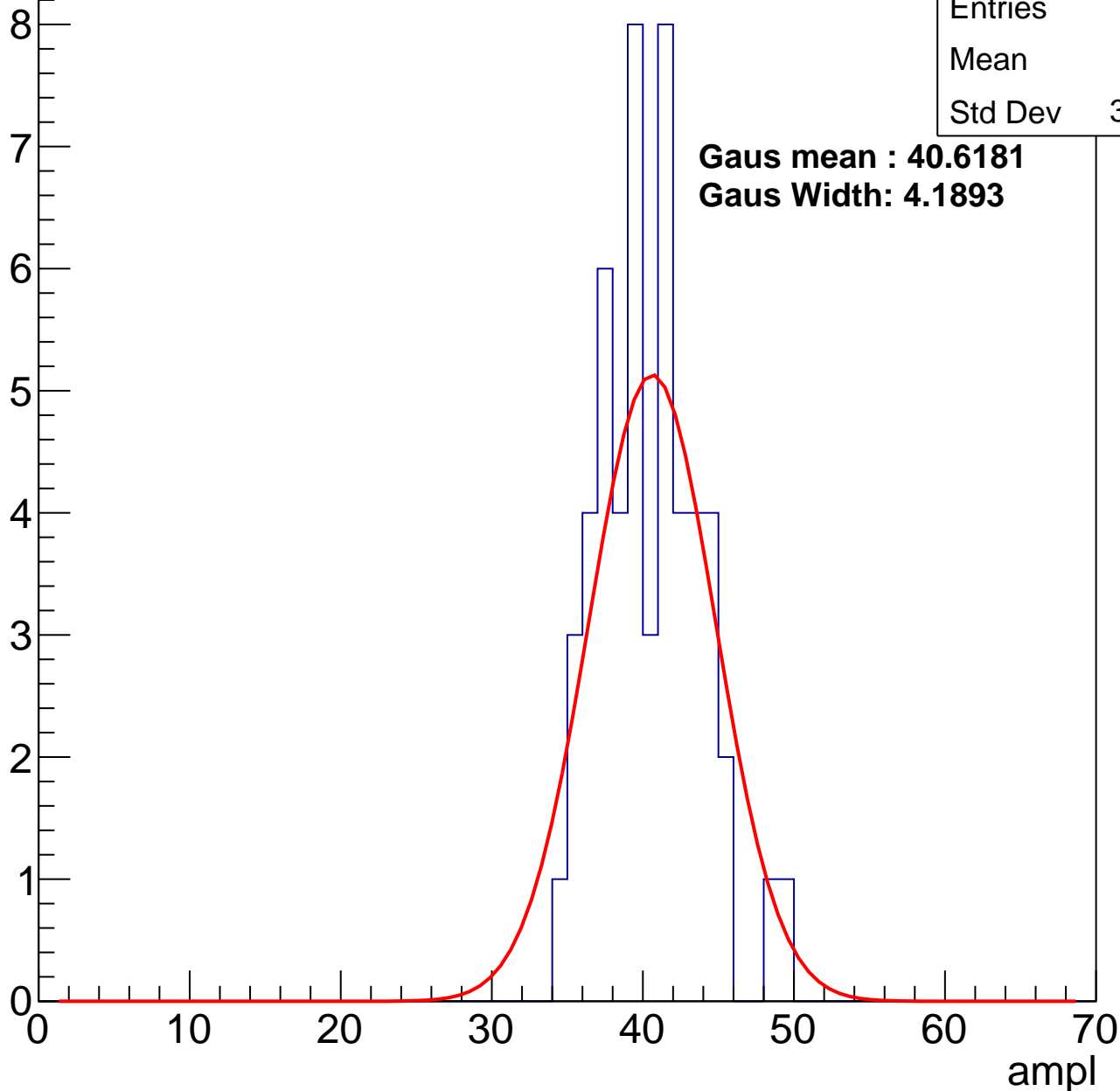
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	40
Std Dev	3.285

**Gaus mean : 40.6181**

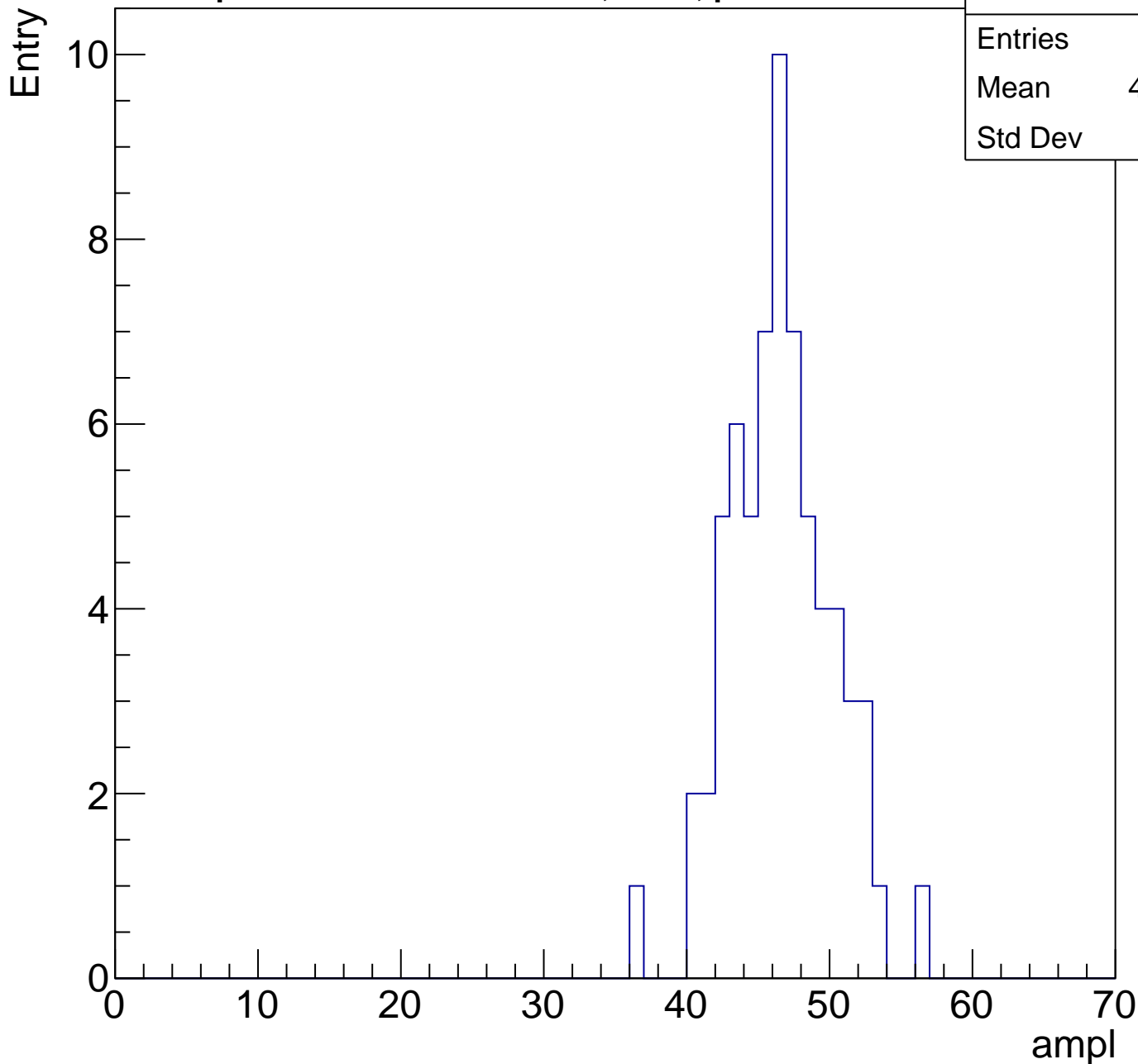
**Gaus Width: 4.1893**



# B1L103S, U1-ch68, adc3

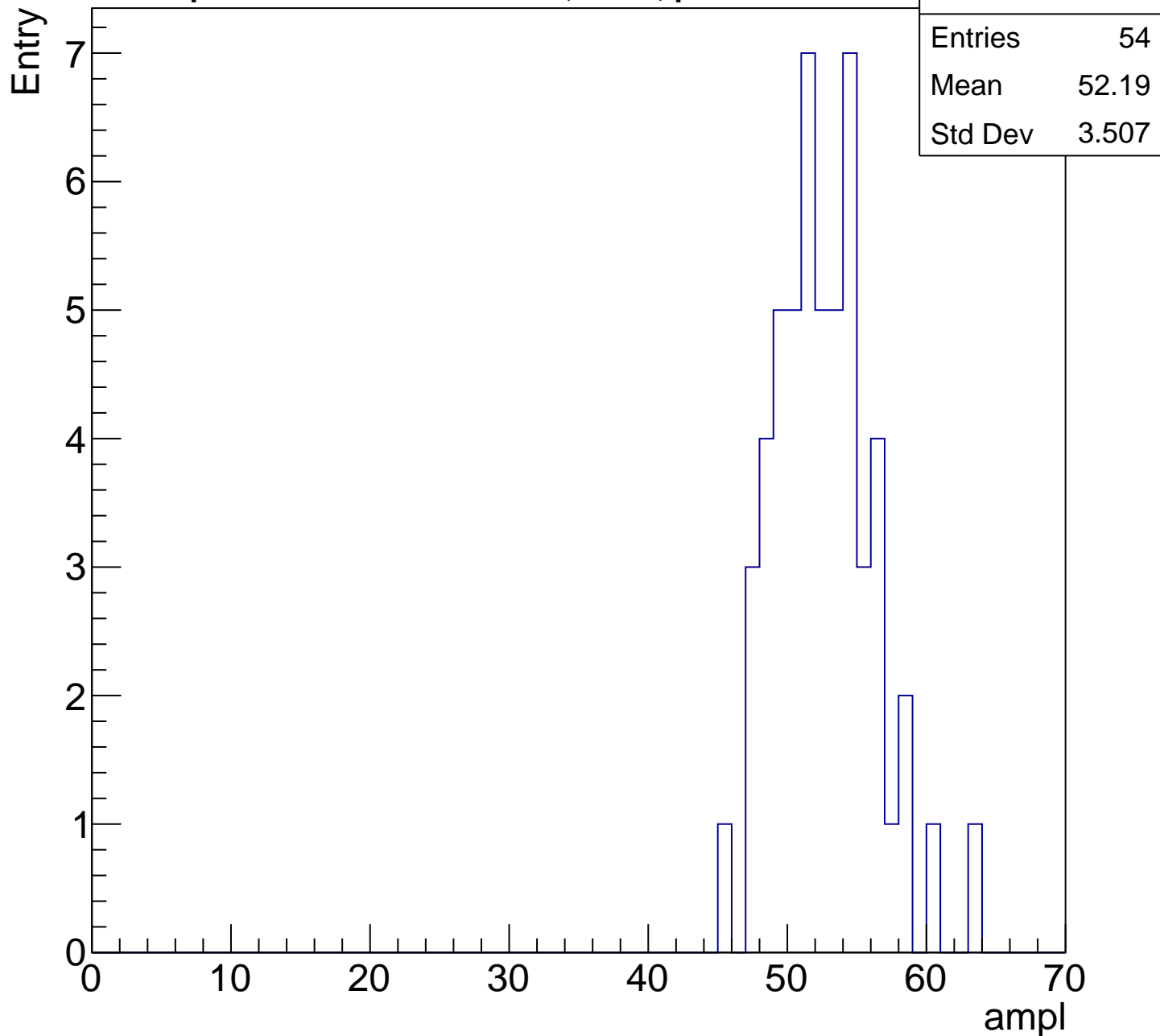
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	66
Mean	46.12
Std Dev	3.57



# B1L103S, U1-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

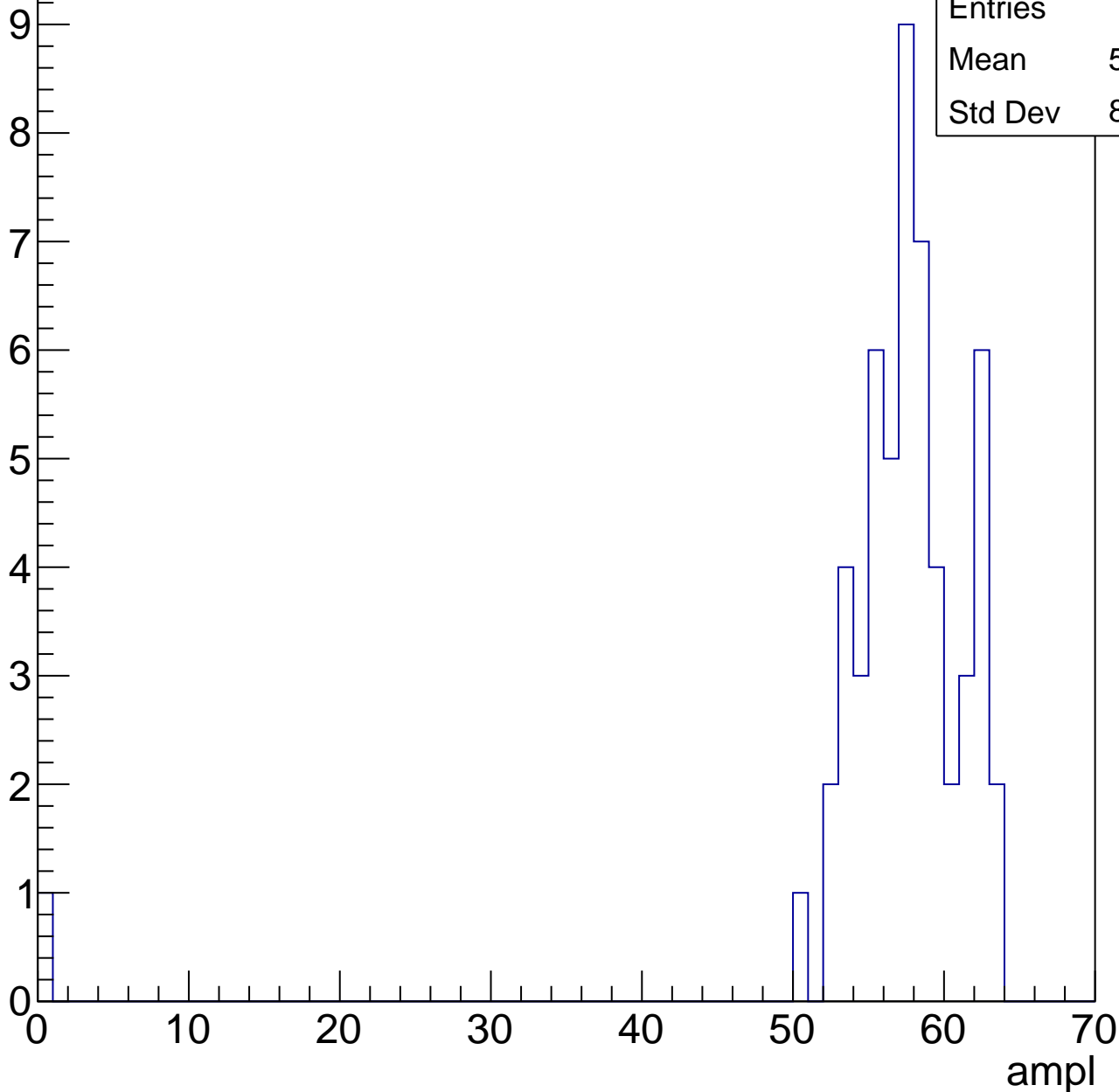


# B1L103S, U1-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

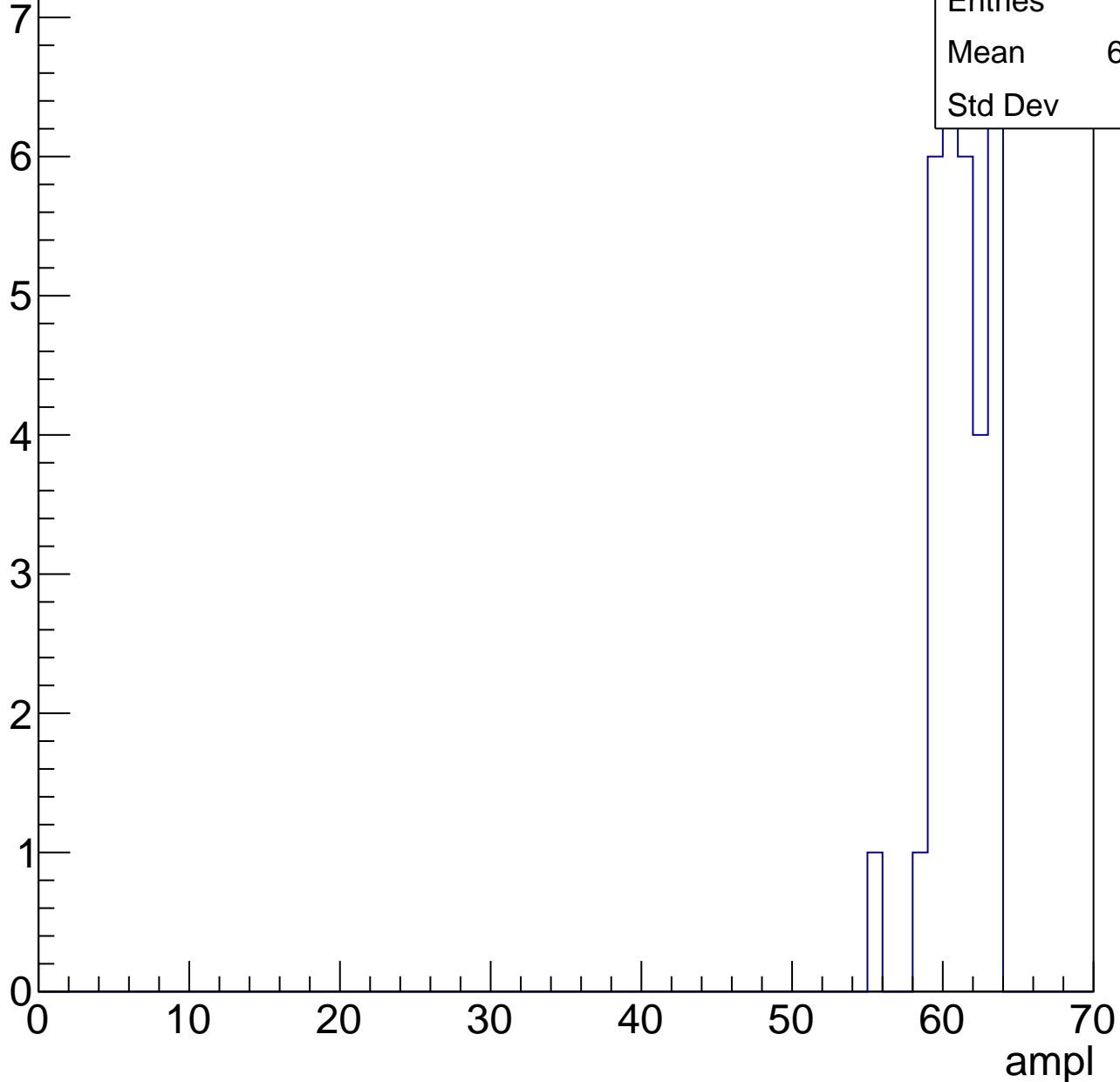
Entries	55
Mean	56.25
Std Dev	8.256



# B1L103S, U1-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U1-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch69, adc0

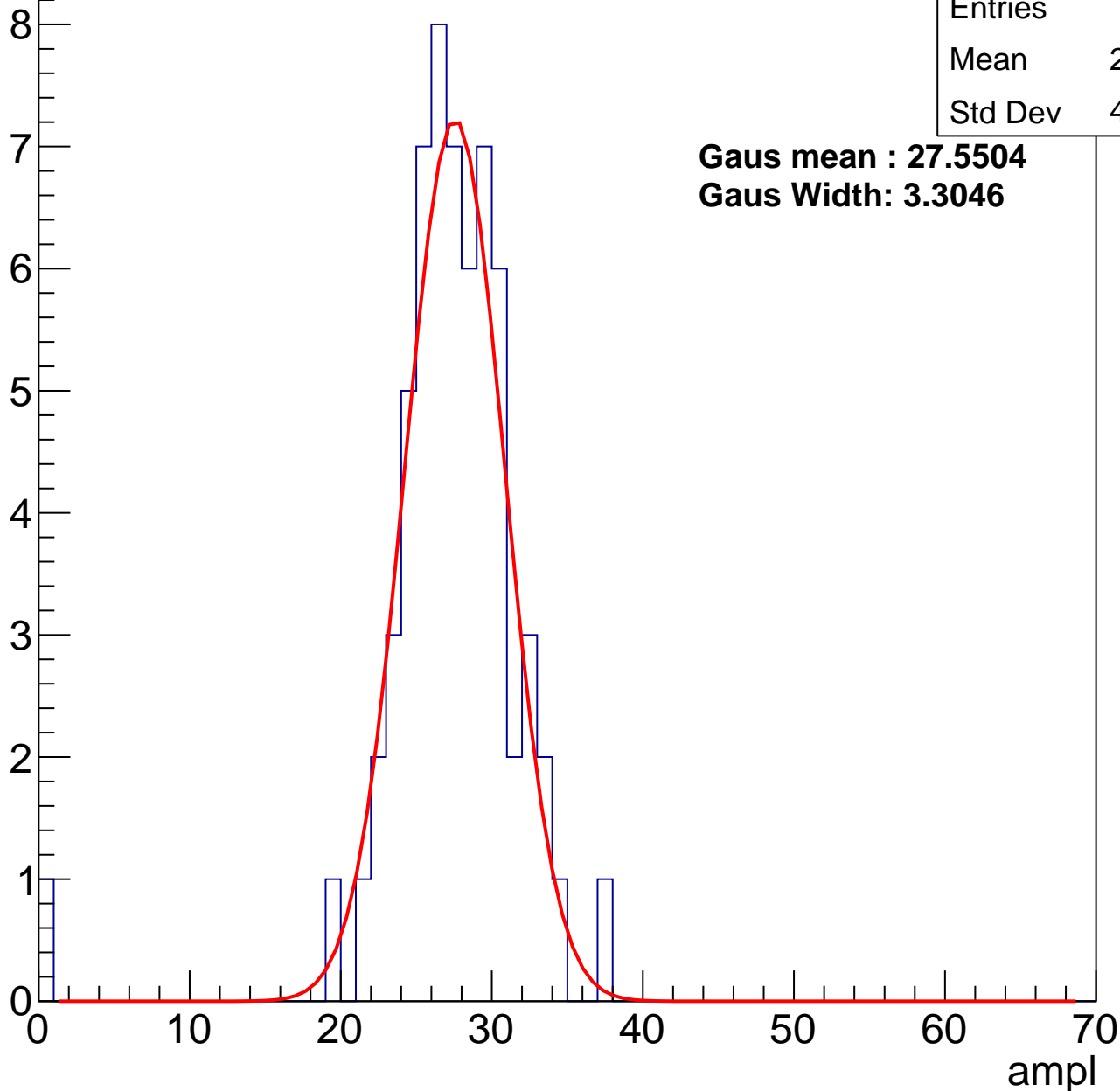
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	26.84
Std Dev	4.752

**Gaus mean : 27.5504**

**Gaus Width: 3.3046**



# B1L103S, U1-ch69, adc1

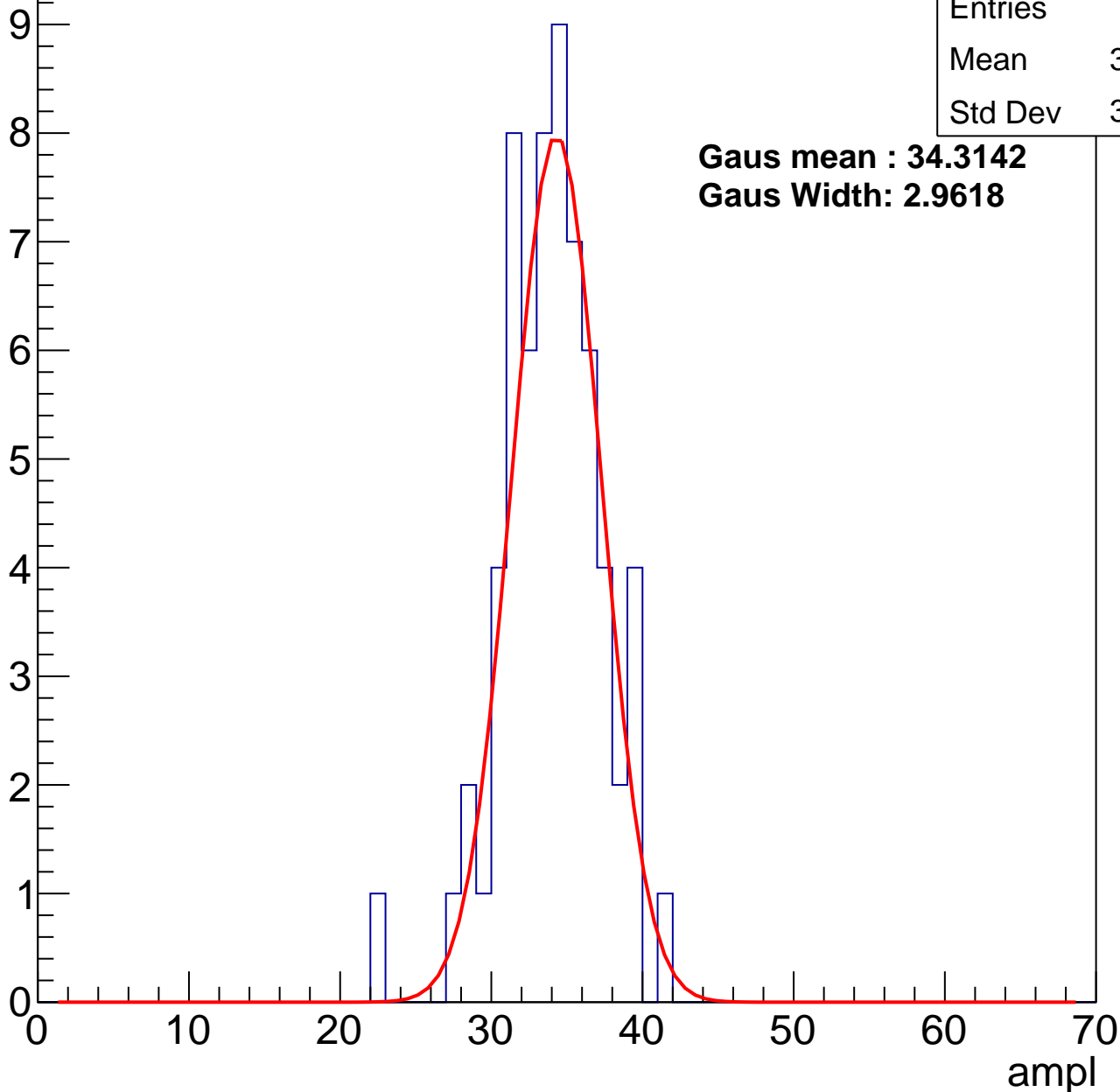
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	33.53
Std Dev	3.288

**Gaus mean : 34.3142**

**Gaus Width: 2.9618**



# B1L103S, U1-ch69, adc2

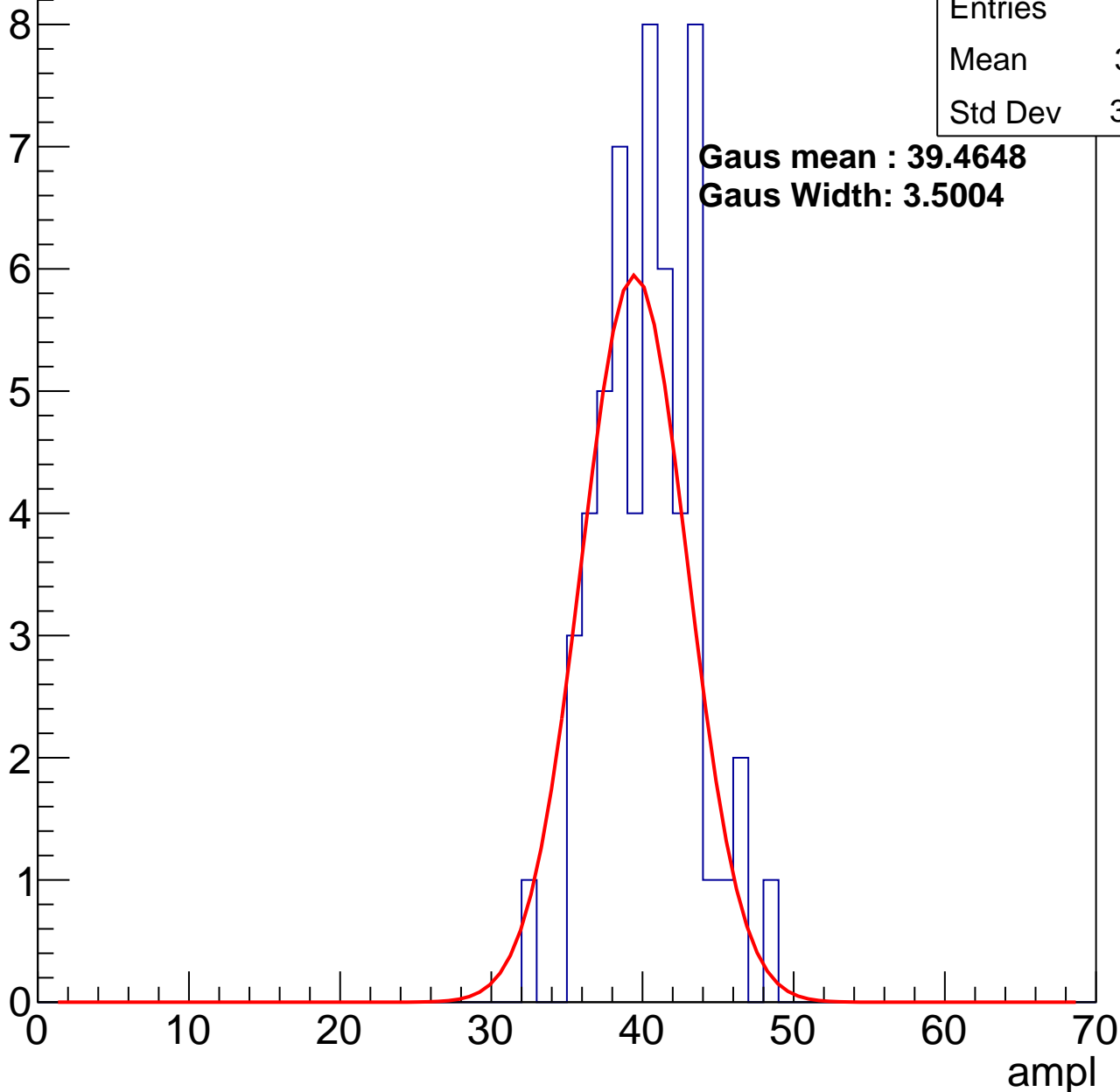
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	39.91
Std Dev	3.164

**Gaus mean : 39.4648**

**Gaus Width: 3.5004**

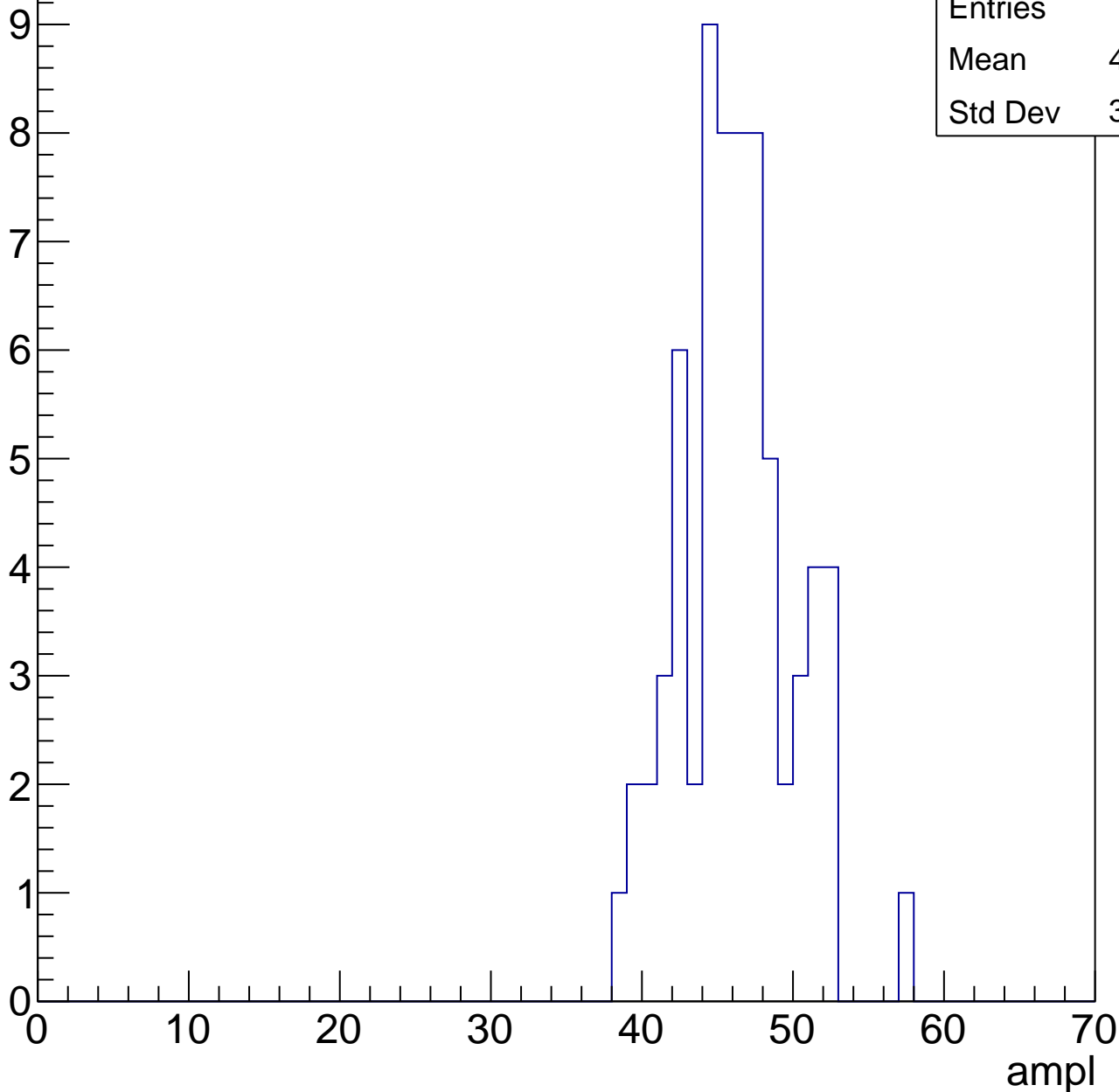


# B1L103S, U1-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	45.79
Std Dev	3.684

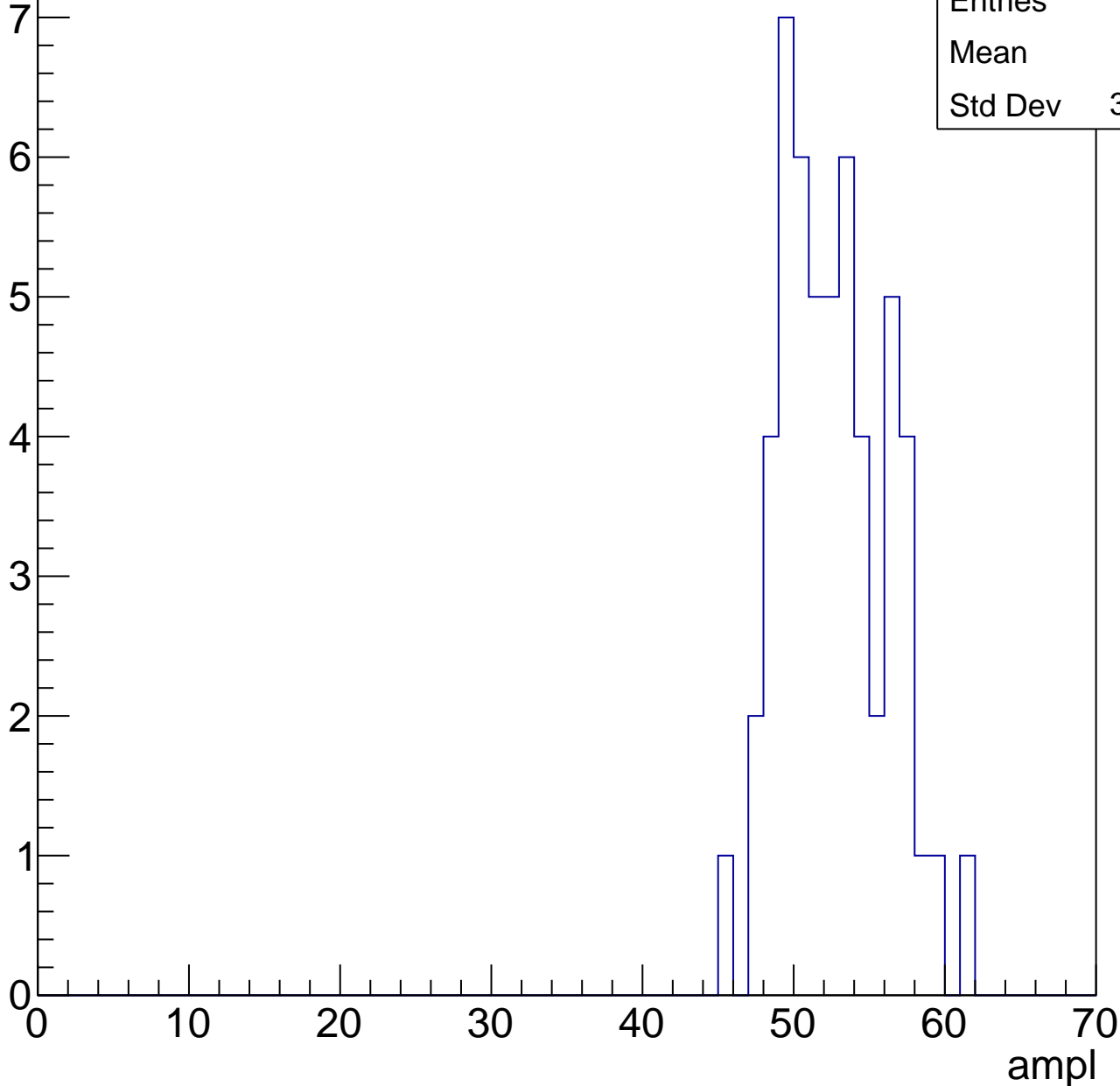


# B1L103S, U1-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

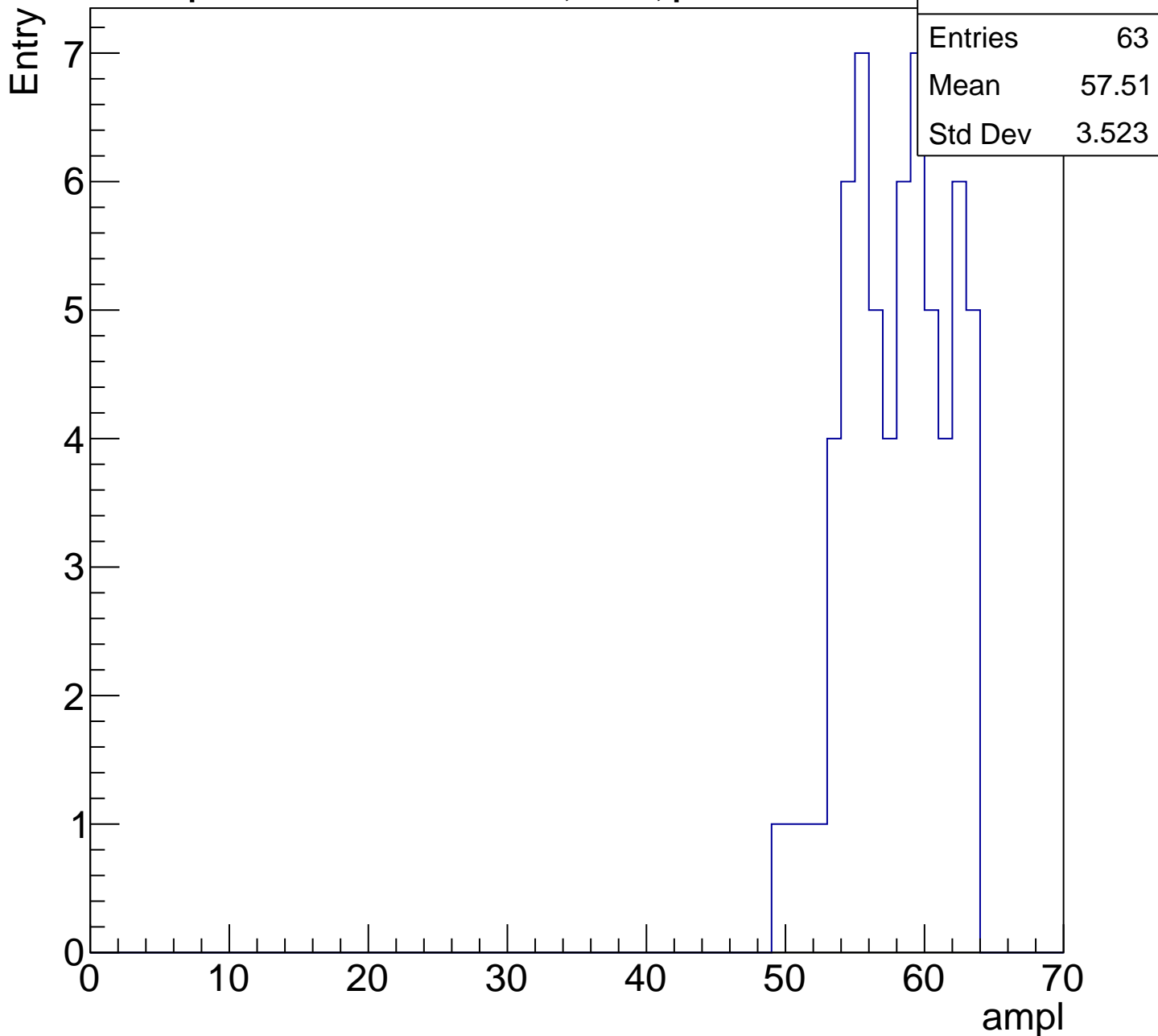
Entry

Entries	54
Mean	52.2
Std Dev	3.439



# B1L103S, U1-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

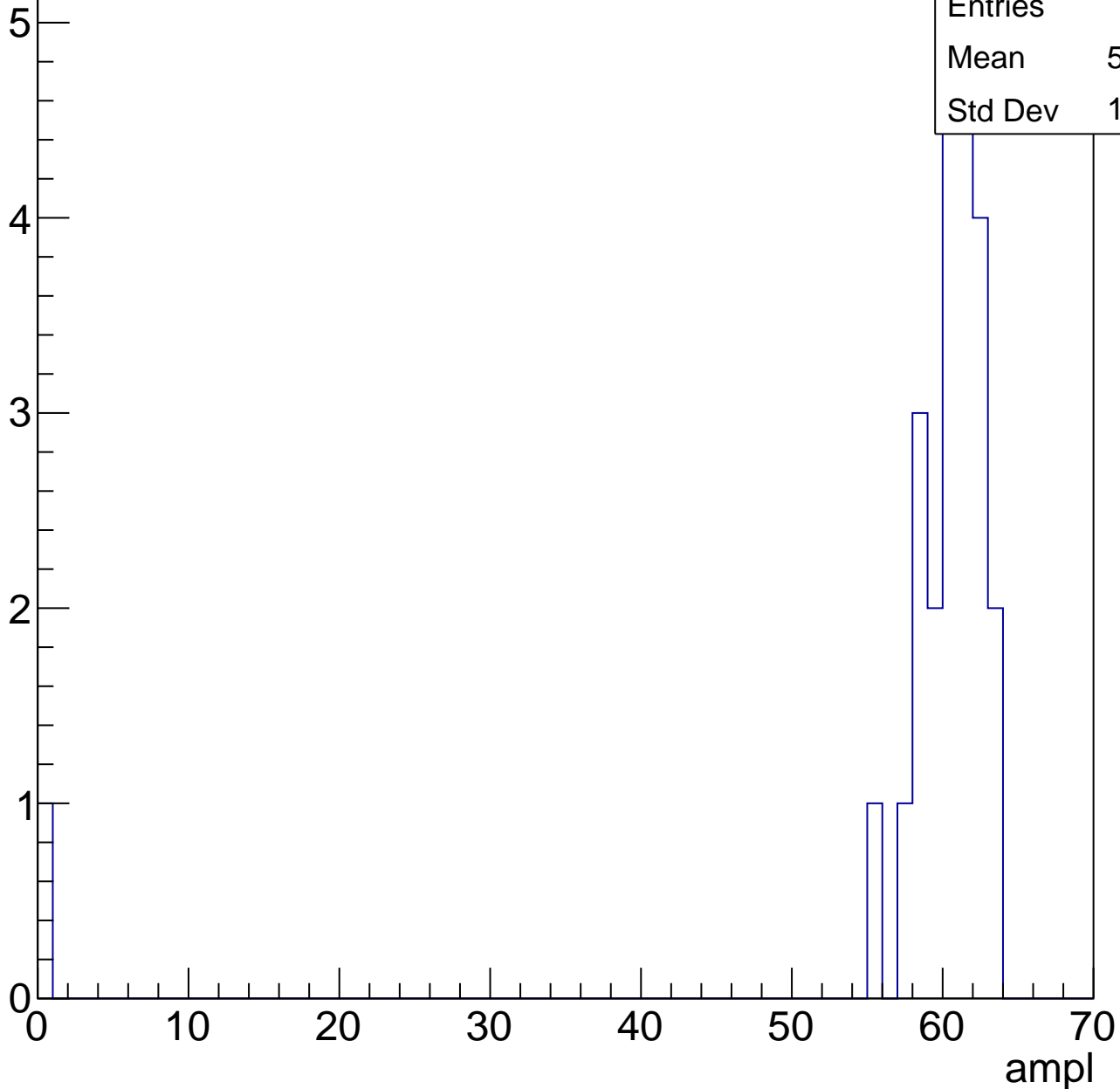


# B1L103S, U1-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	24
Mean	57.62
Std Dev	12.16

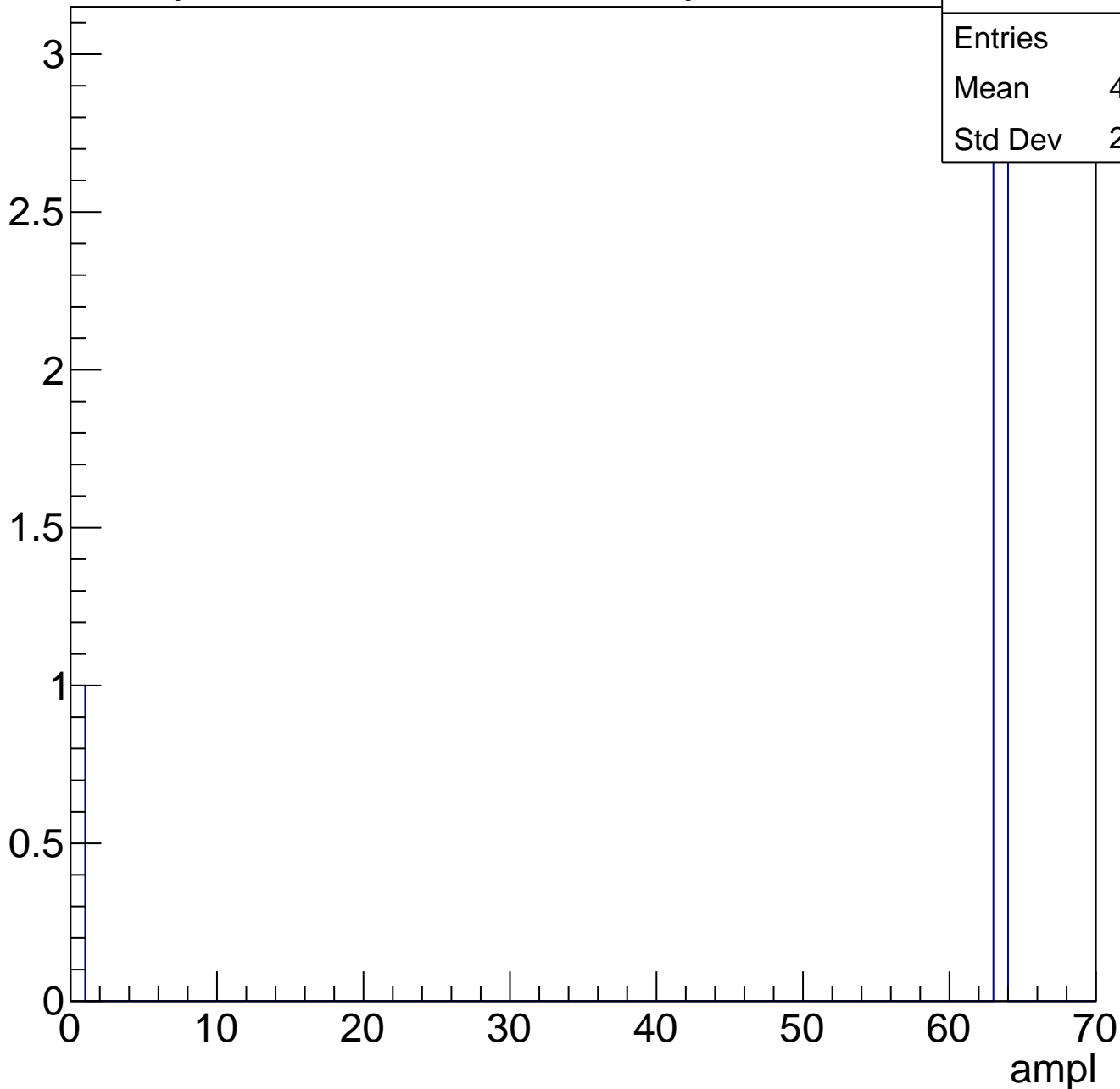




# B1L103S, U1-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch70, adc0

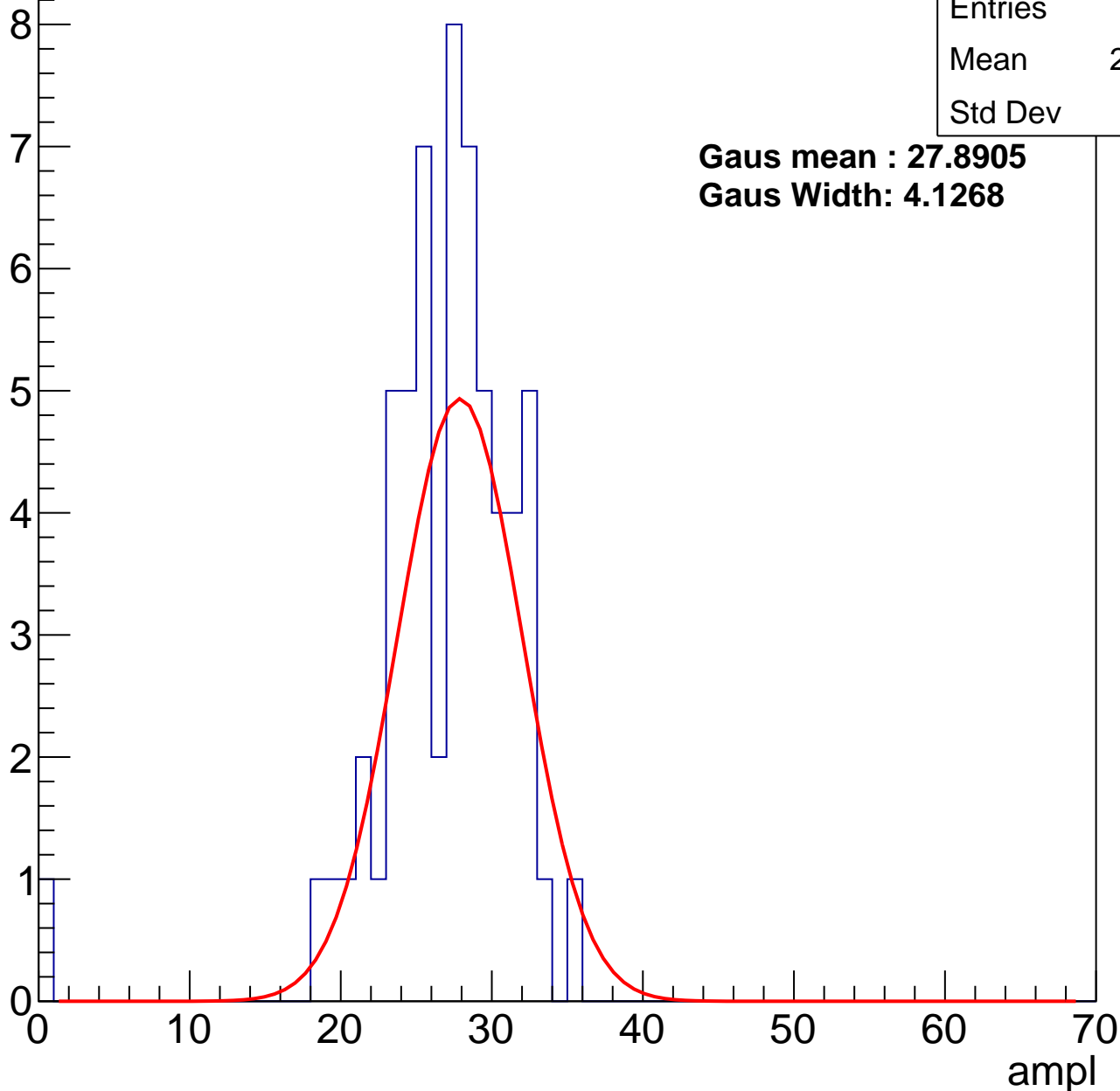
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	26.43
Std Dev	4.97

**Gaus mean : 27.8905**

**Gaus Width: 4.1268**



# B1L103S, U1-ch70, adc1

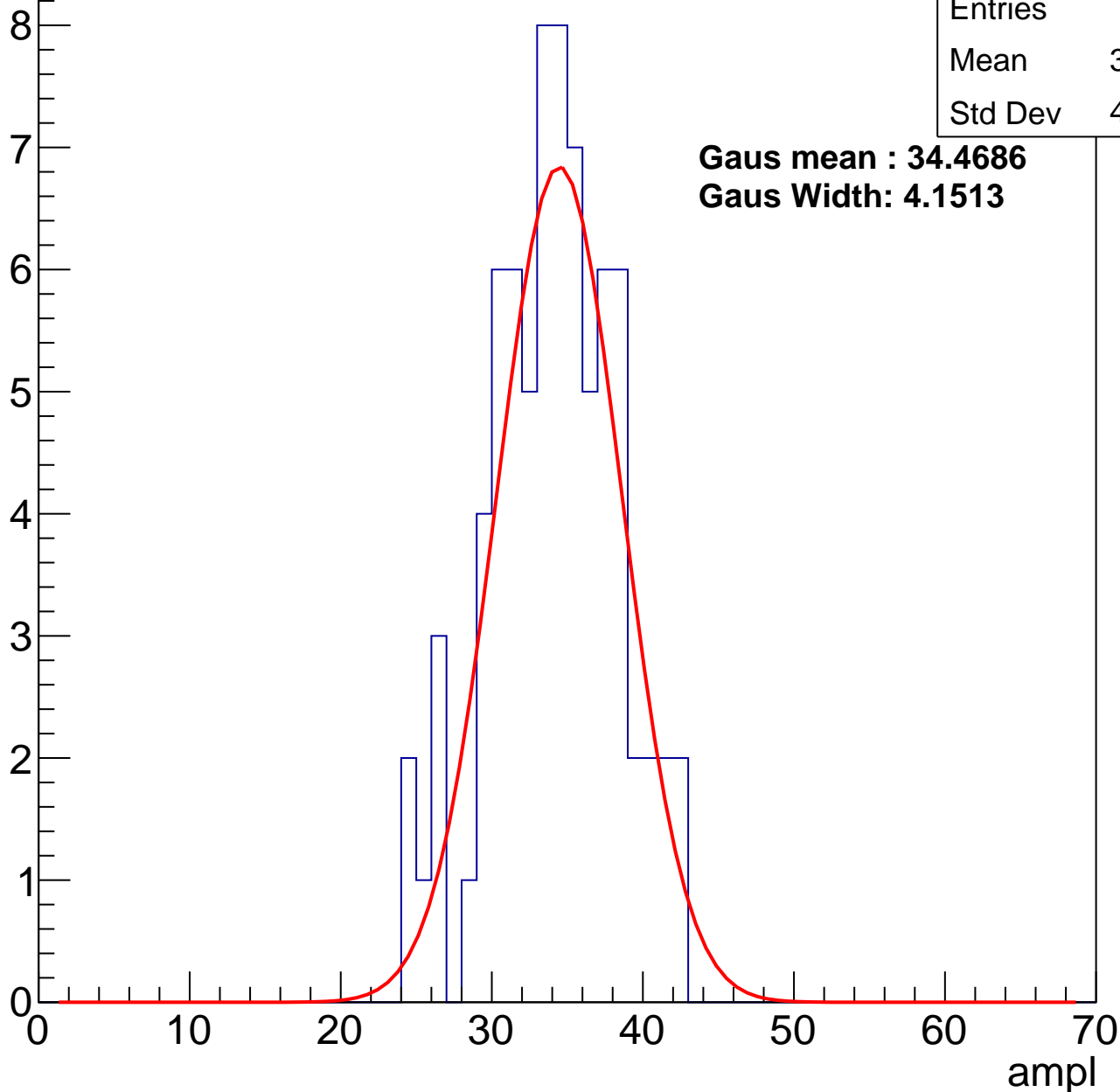
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	33.63
Std Dev	4.139

**Gaus mean : 34.4686**

**Gaus Width: 4.1513**



# B1L103S, U1-ch70, adc2

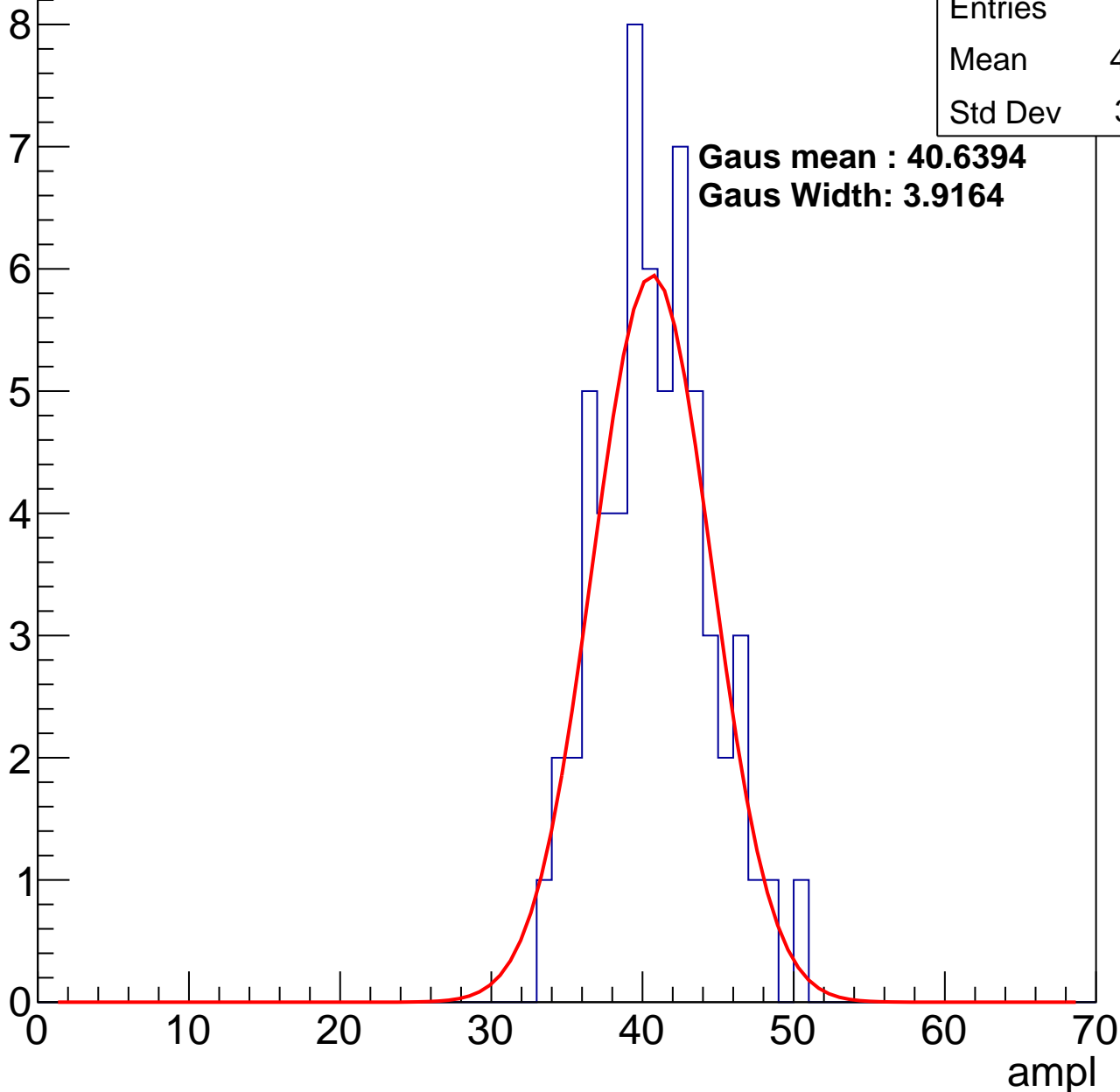
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	40.37
Std Dev	3.651

**Gaus mean : 40.6394**

**Gaus Width: 3.9164**

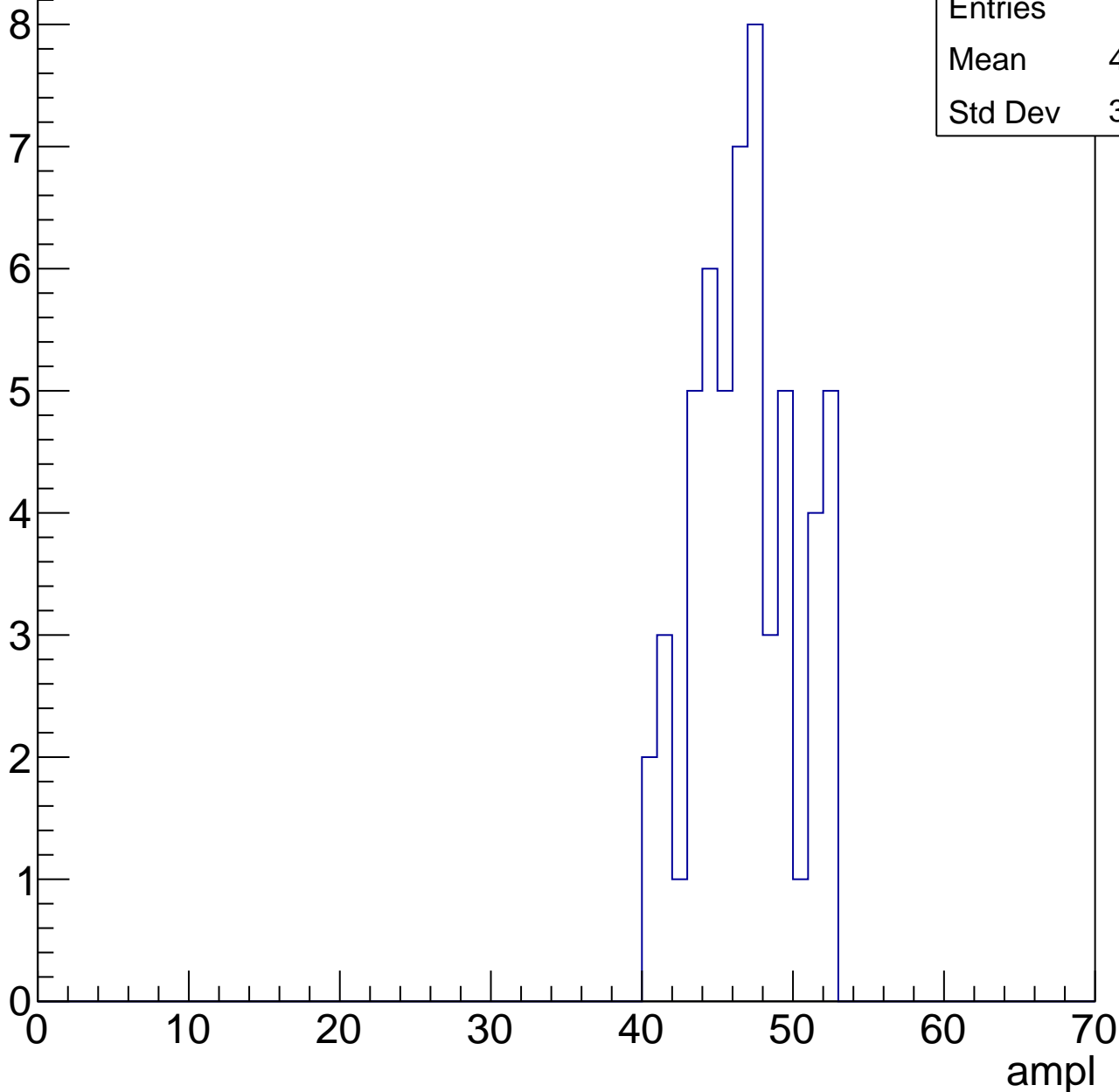


# B1L103S, U1-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

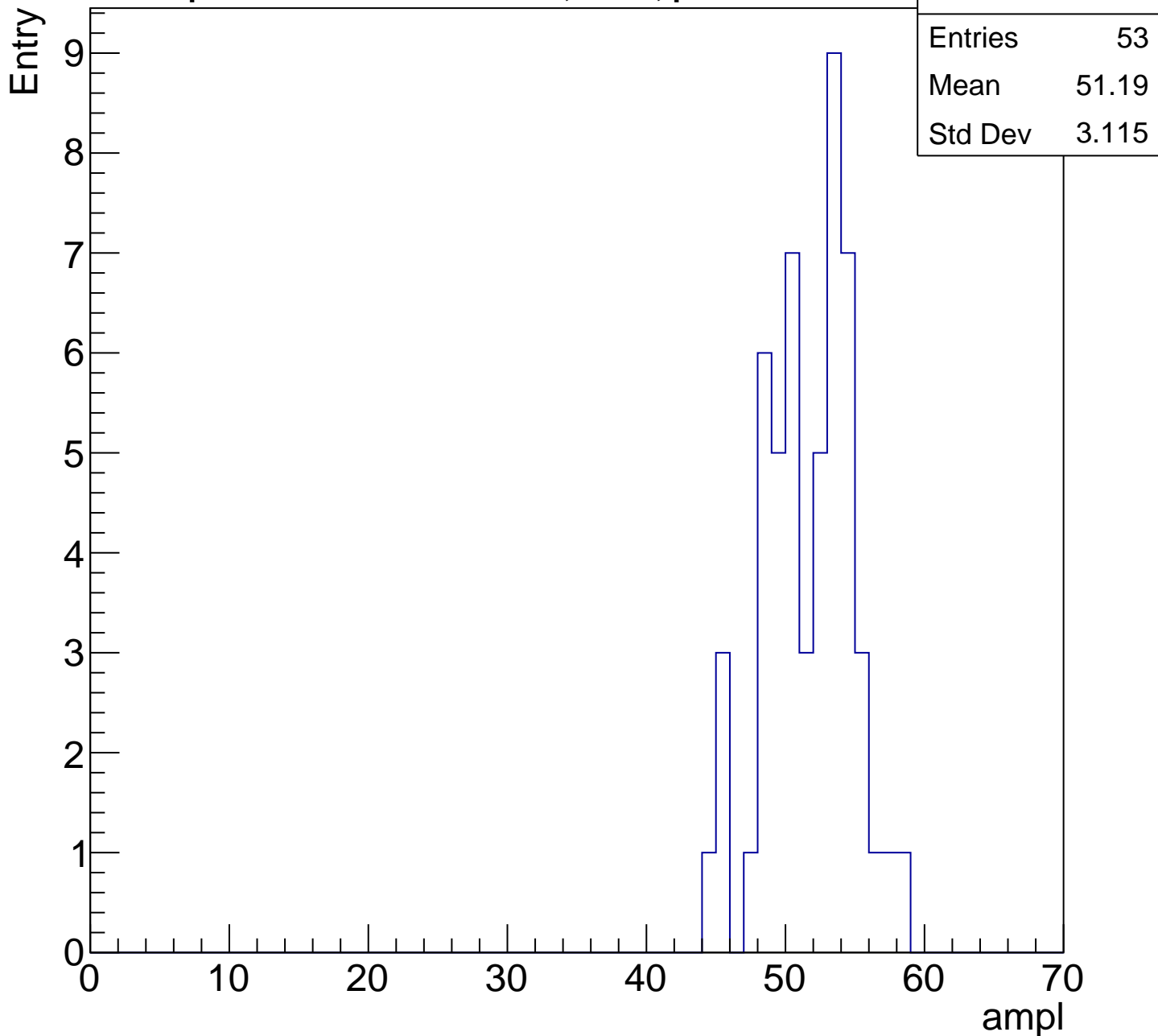
Entry

Entries	55
Mean	46.36
Std Dev	3.277



# B1L103S, U1-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

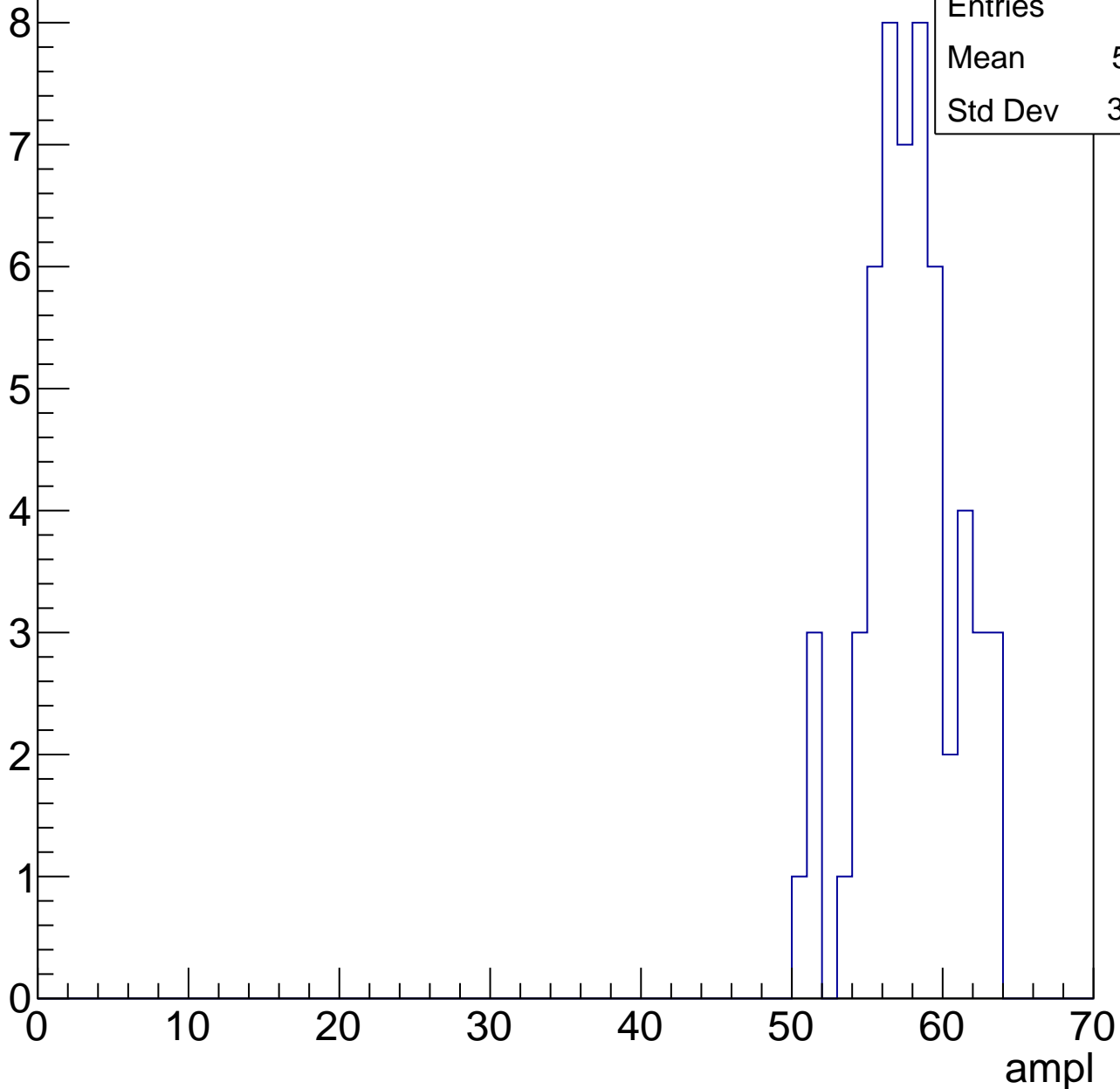


# B1L103S, U1-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	57.31
Std Dev	3.086

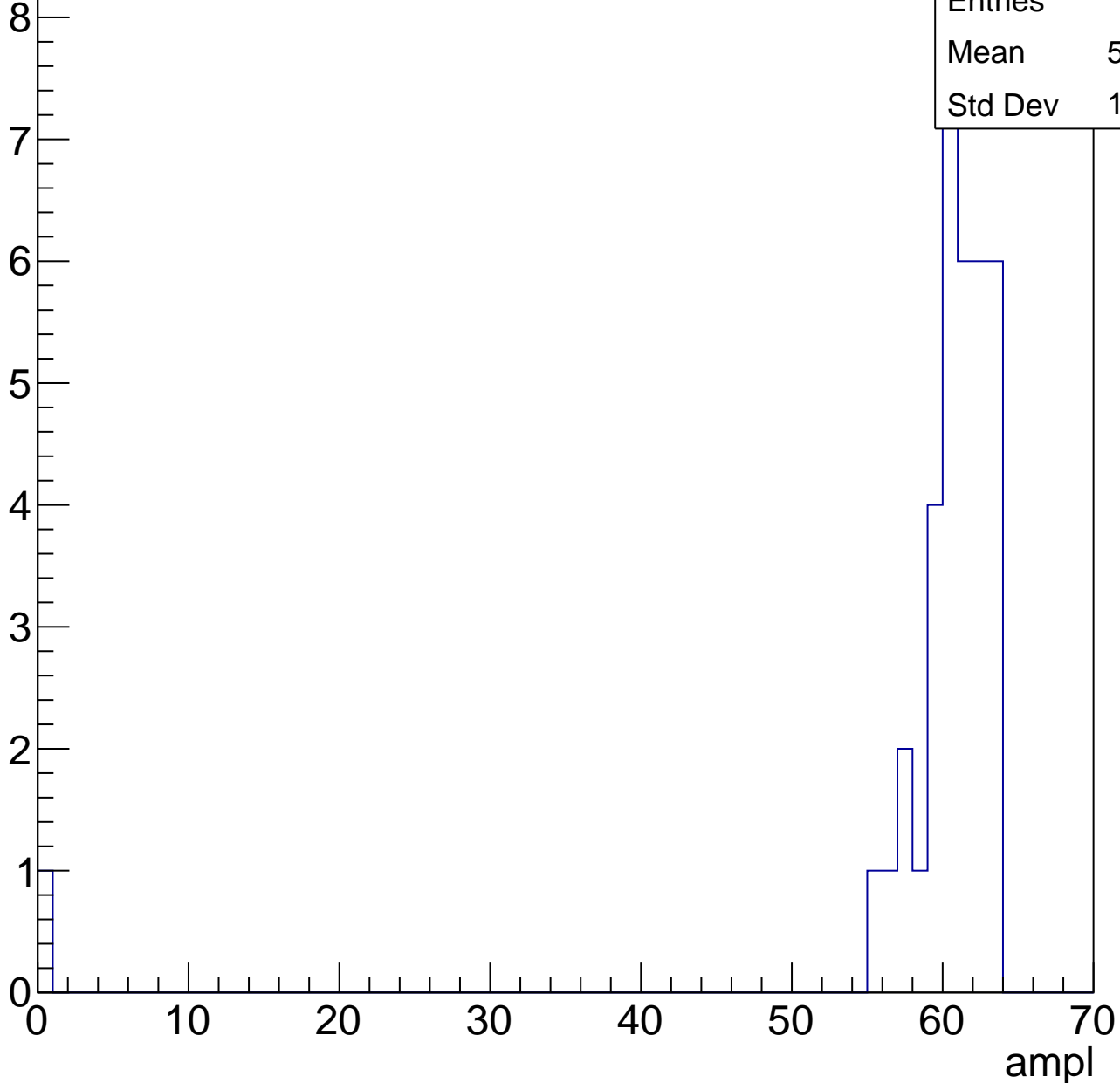


# B1L103S, U1-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	36
Mean	58.75
Std Dev	10.13





# B1L103S, U1-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch71, adc0

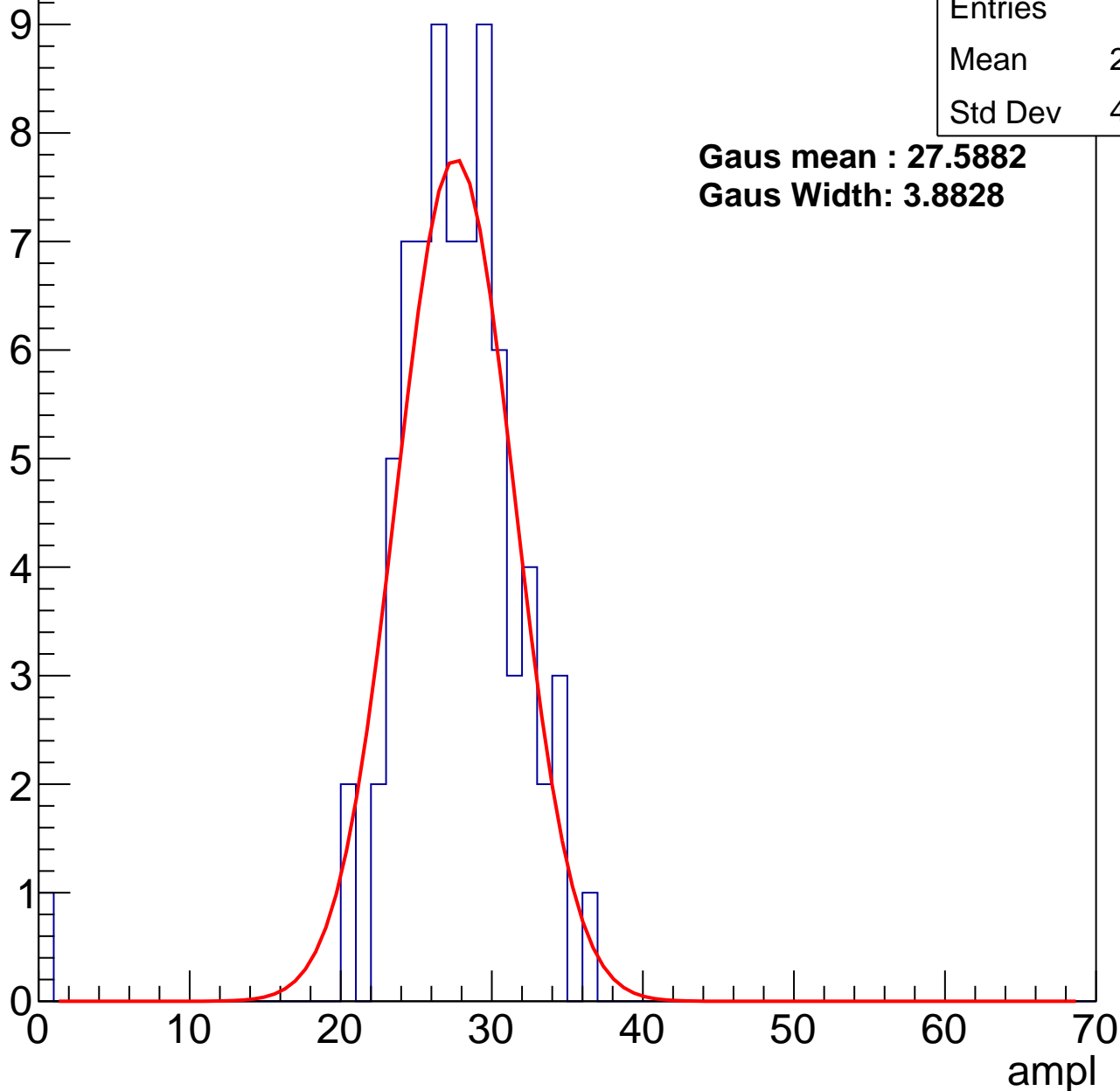
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	27.03
Std Dev	4.622

**Gaus mean : 27.5882**

**Gaus Width: 3.8828**



# B1L103S, U1-ch71, adc1

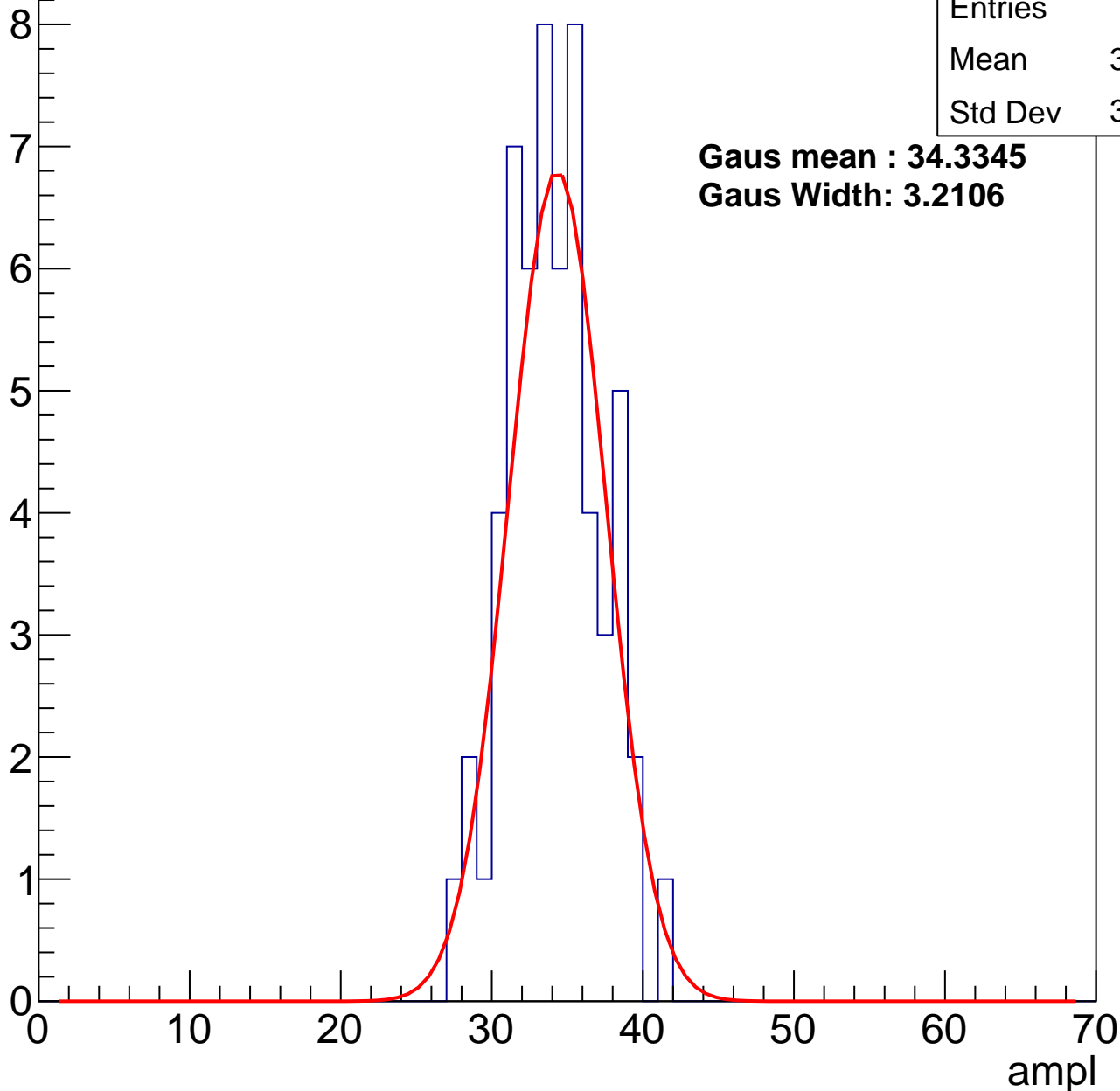
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	33.67
Std Dev	3.019

**Gaus mean : 34.3345**

**Gaus Width: 3.2106**



# B1L103S, U1-ch71, adc2

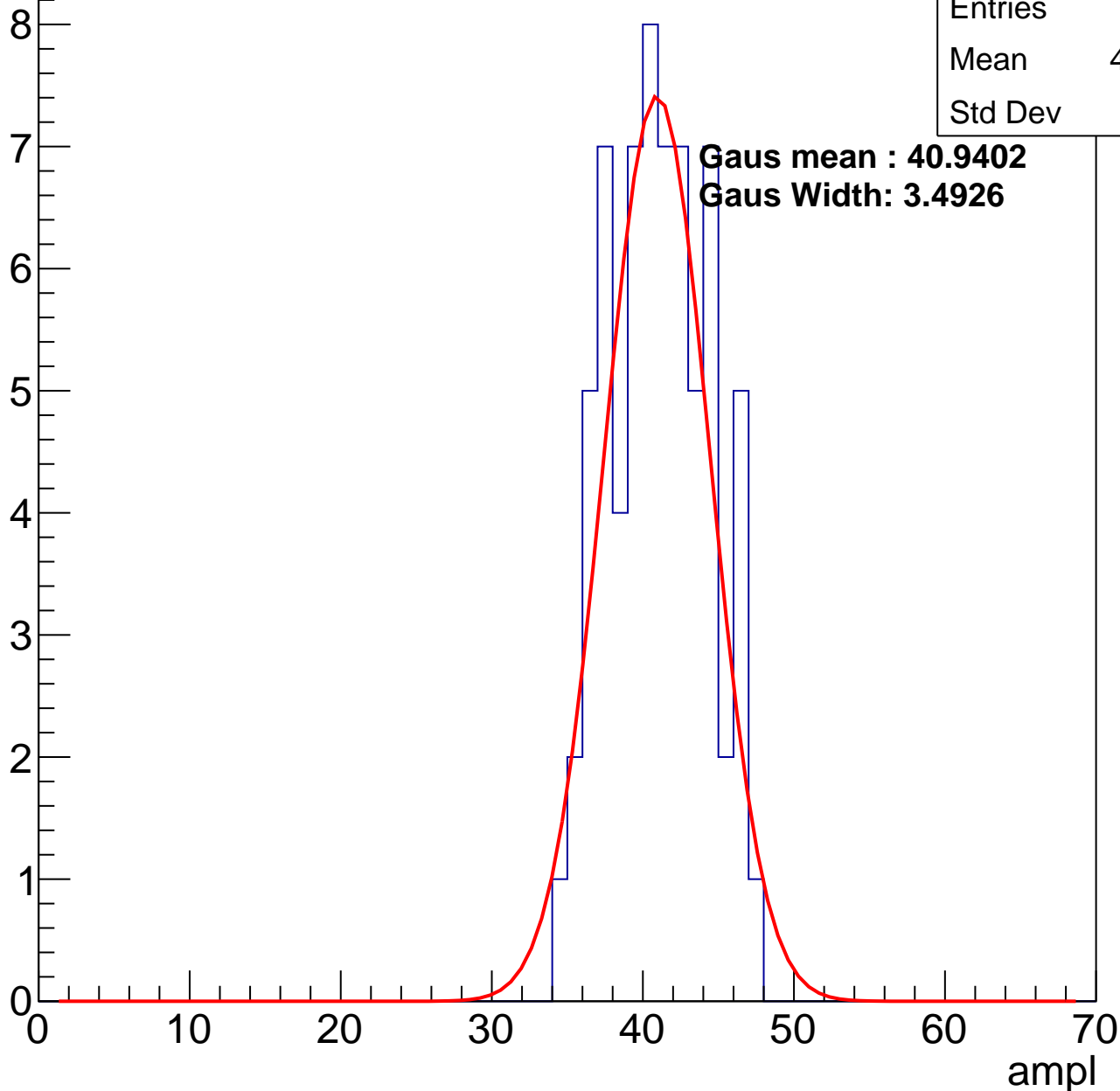
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	40.57
Std Dev	3.21

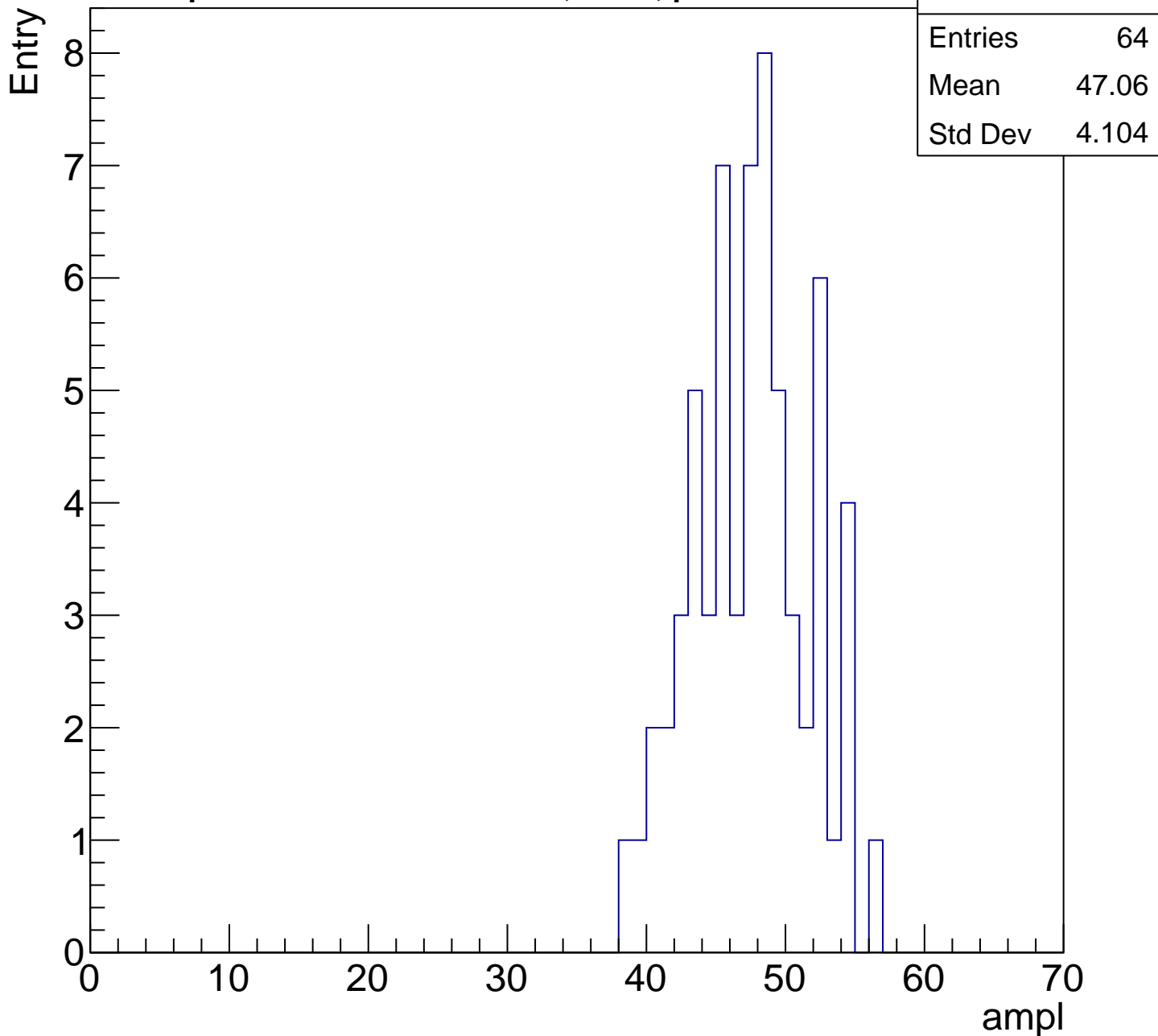
**Gaus mean : 40.9402**

**Gaus Width: 3.4926**



# B1L103S, U1-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

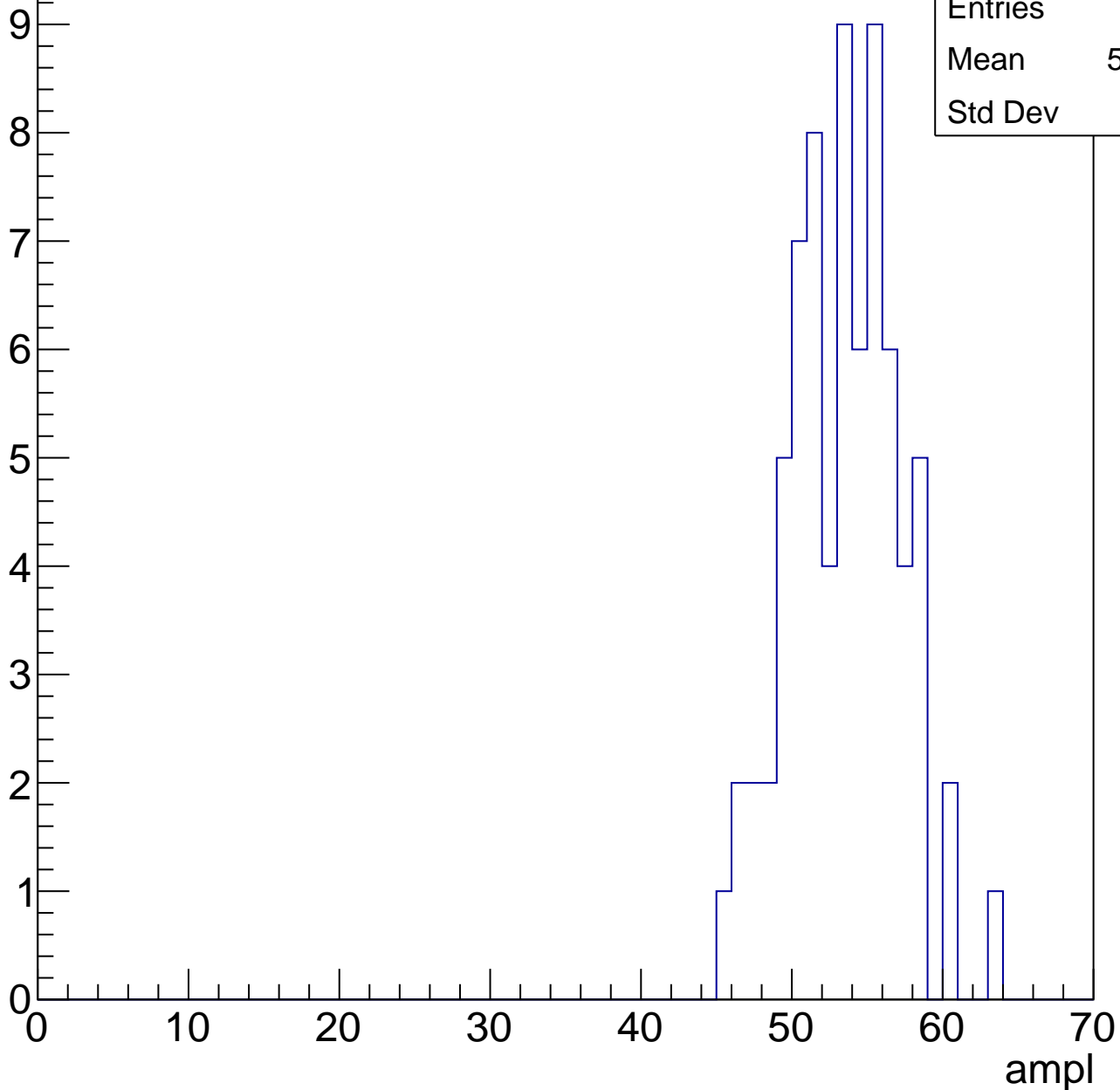


# B1L103S, U1-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	53.03
Std Dev	3.6



# B1L103S, U1-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

10

8

6

4

2

0

0

10

20

30

40

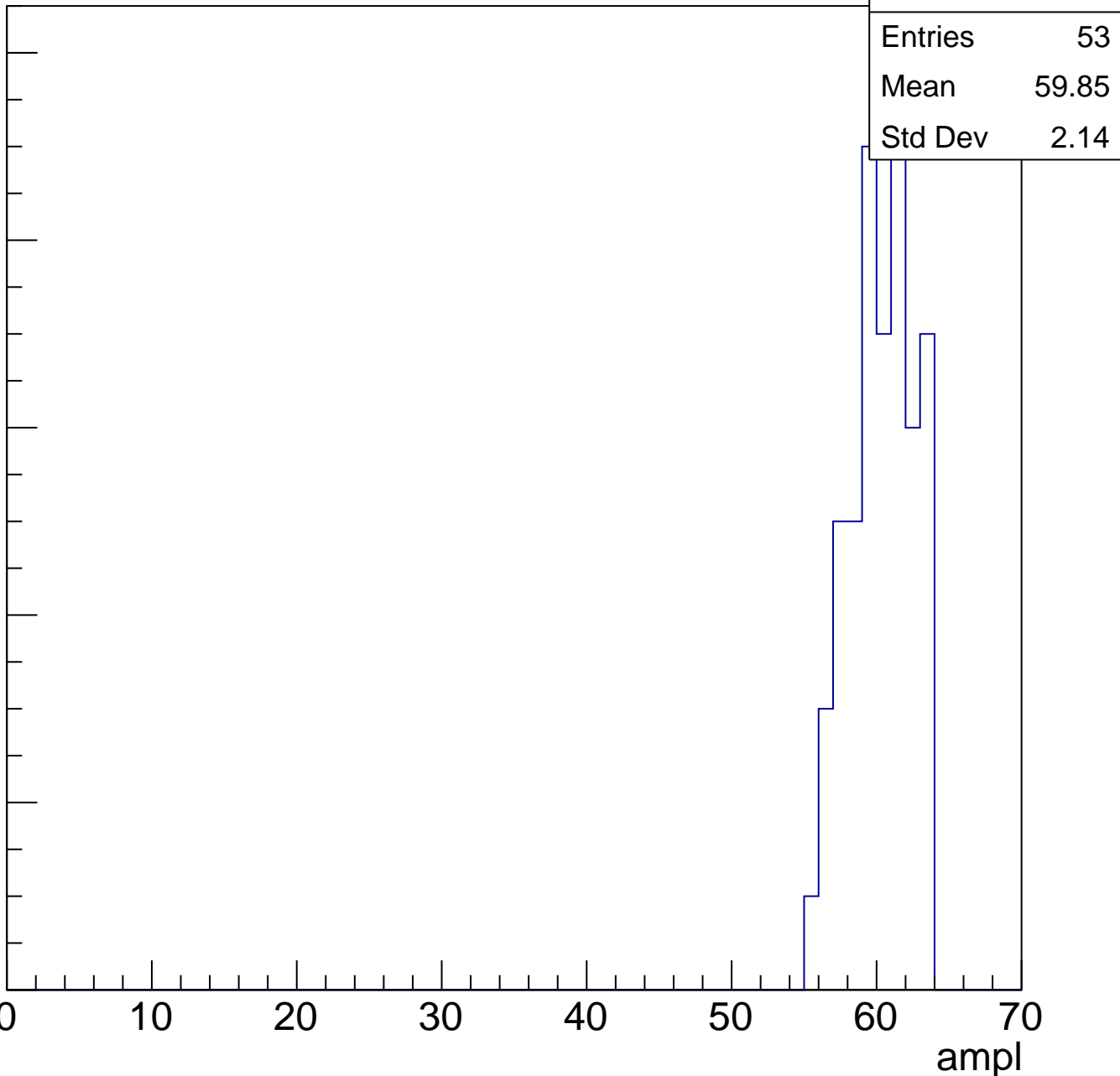
50

60

70

ampl

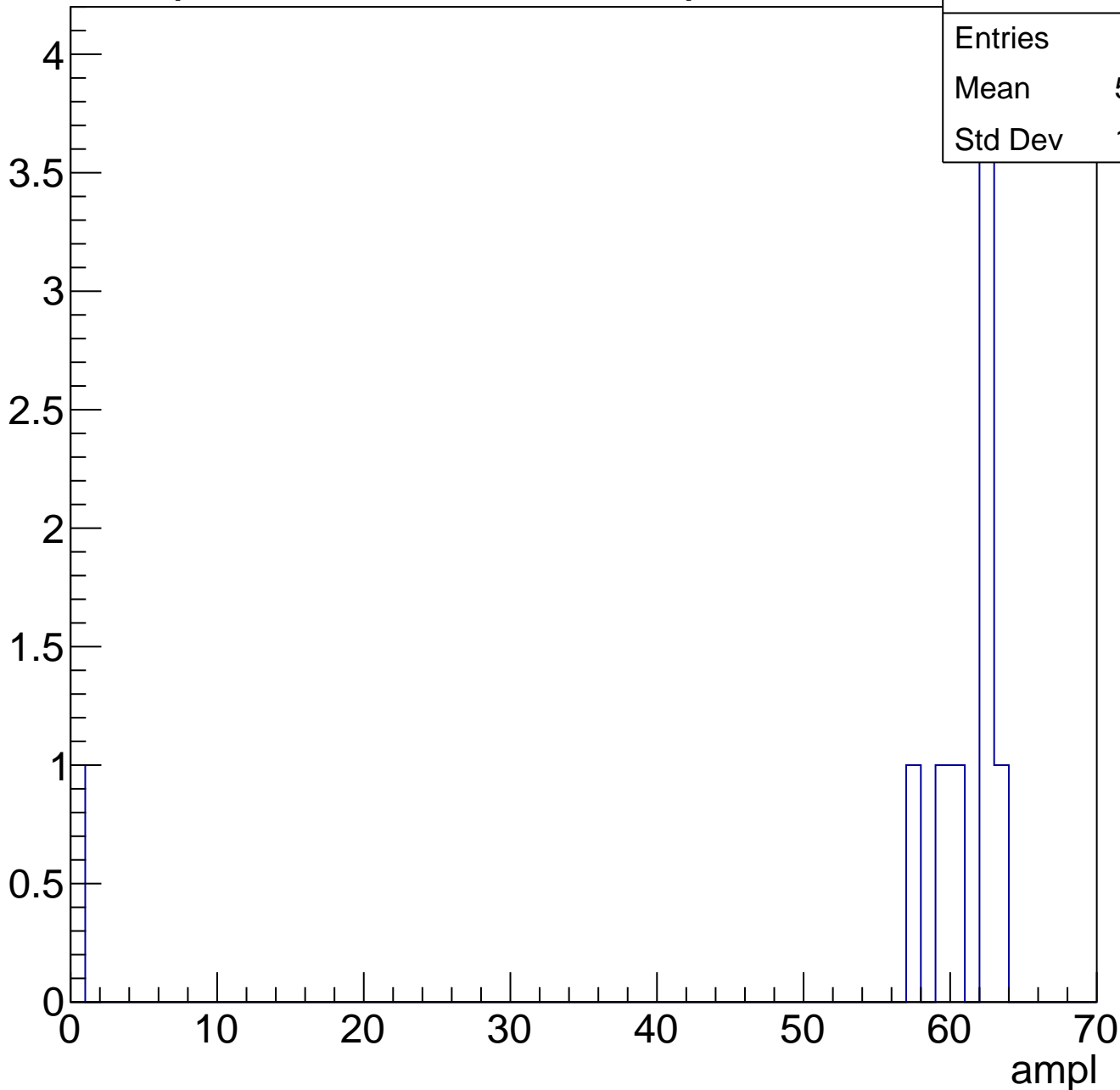
Entries	53
Mean	59.85
Std Dev	2.14



# B1L103S, U1-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U1-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch72, adc0

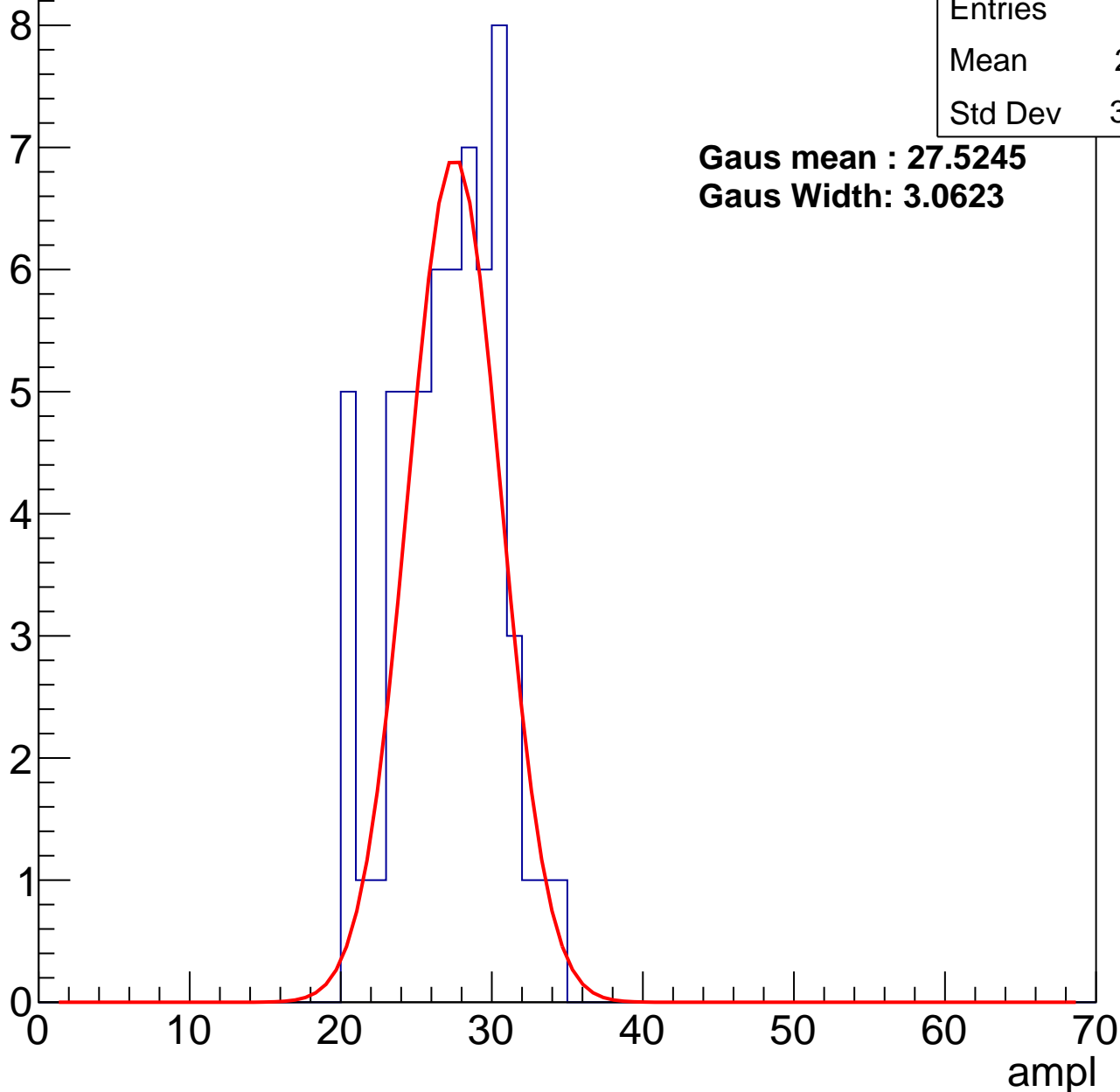
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	26.61
Std Dev	3.408

**Gaus mean : 27.5245**

**Gaus Width: 3.0623**



# B1L103S, U1-ch72, adc1

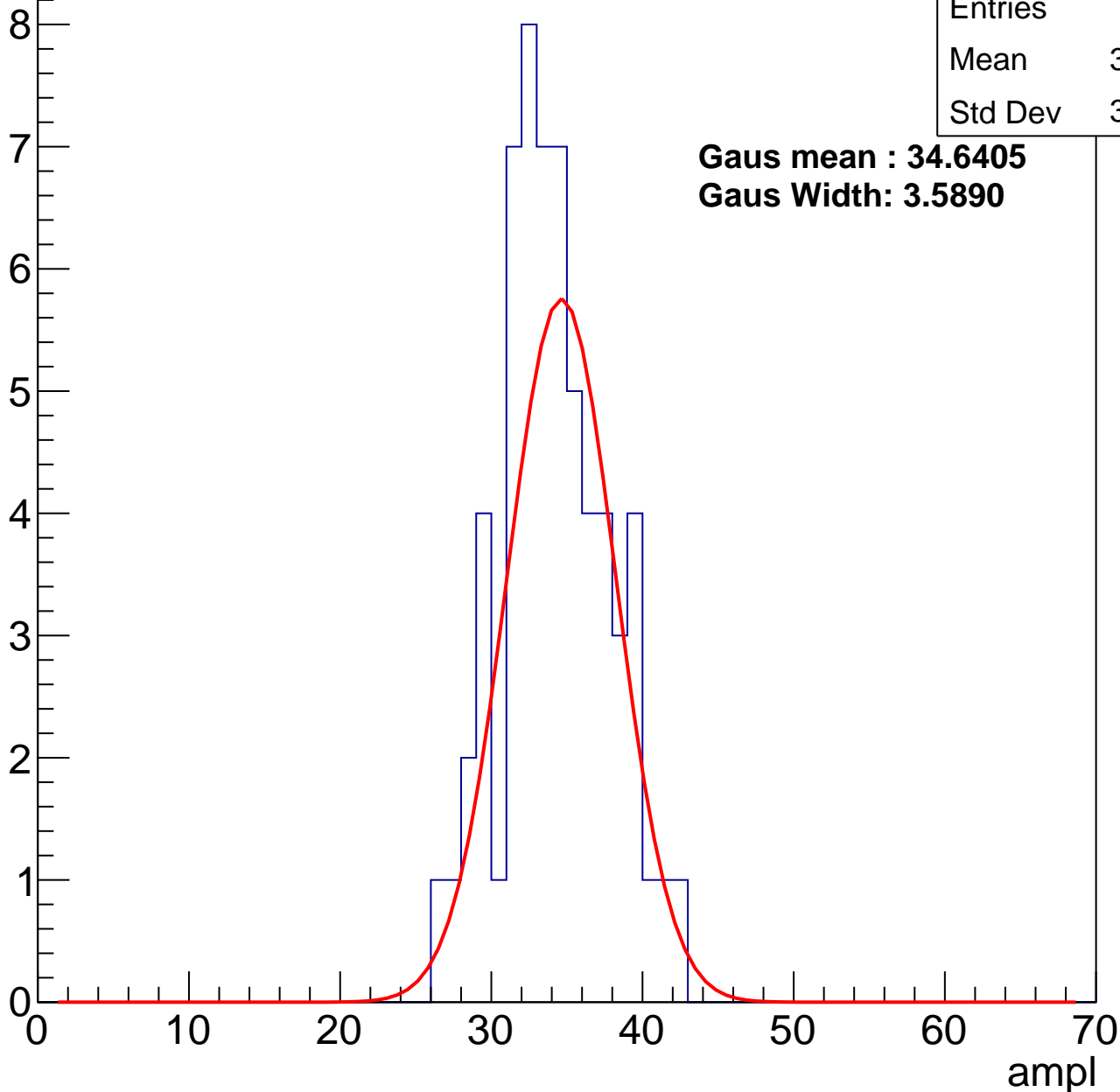
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	33.72
Std Dev	3.512

**Gaus mean : 34.6405**

**Gaus Width: 3.5890**



# B1L103S, U1-ch72, adc2

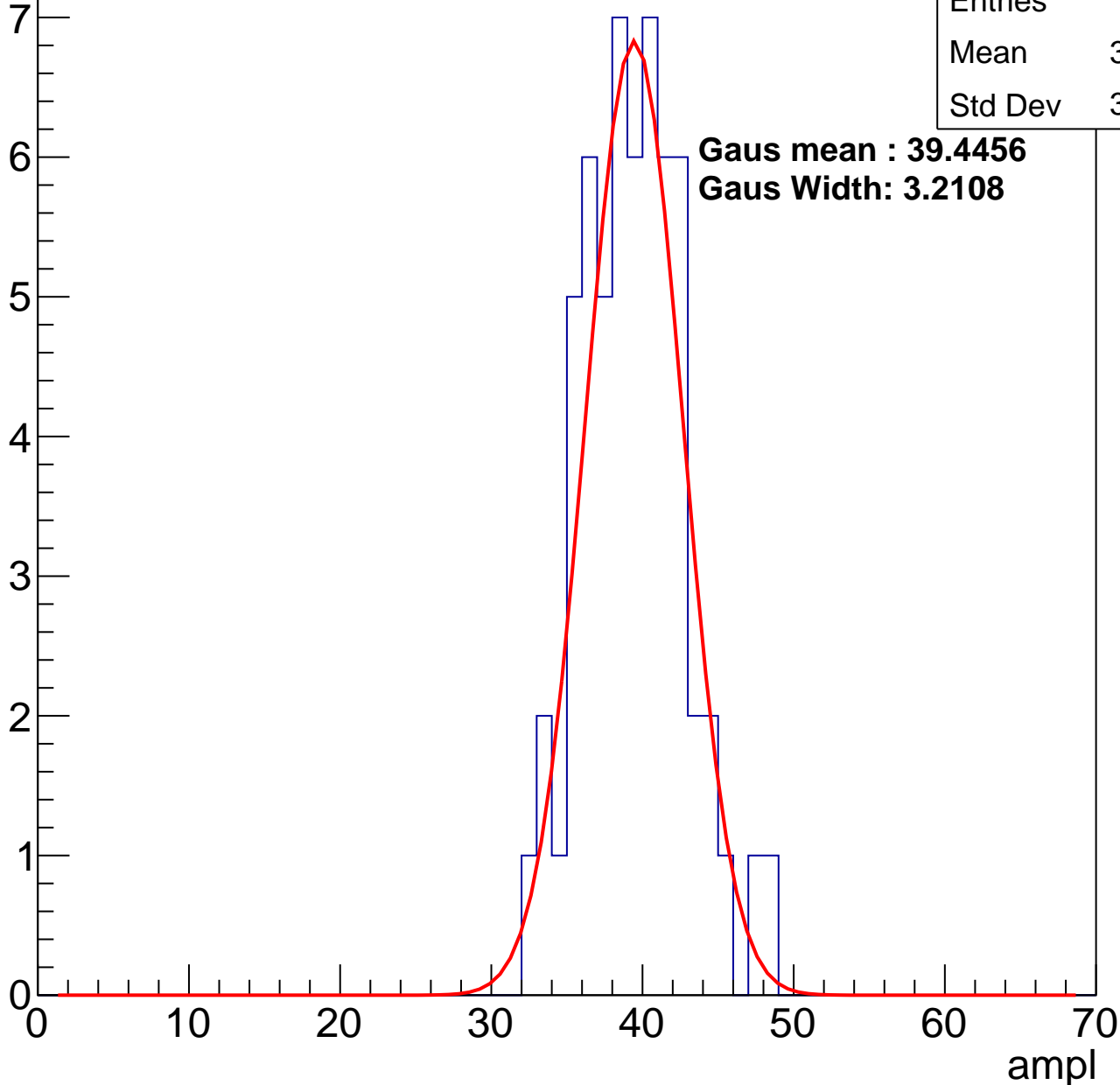
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	38.98
Std Dev	3.332

**Gaus mean : 39.4456**

**Gaus Width: 3.2108**

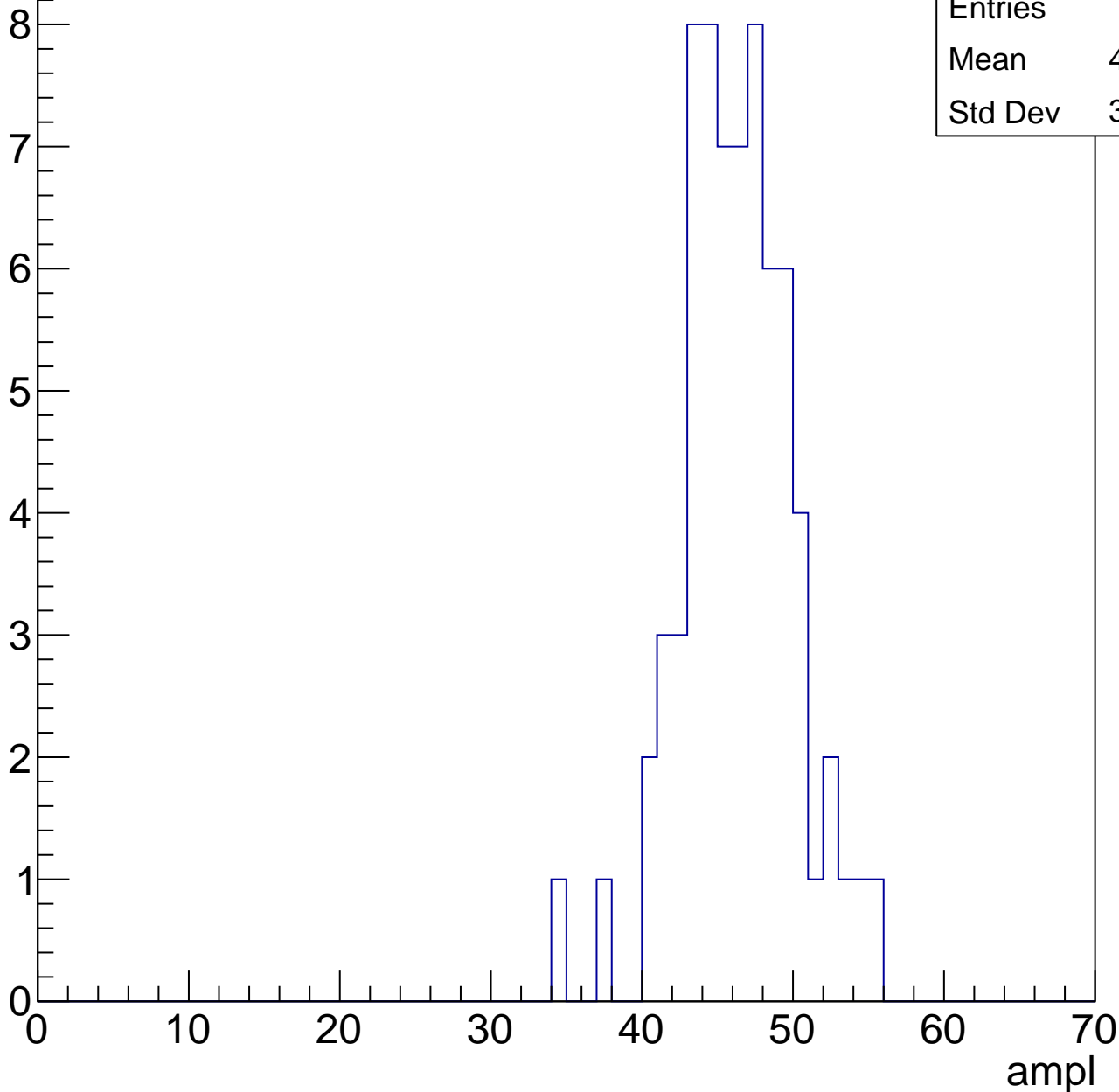


# B1L103S, U1-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	45.83
Std Dev	3.722

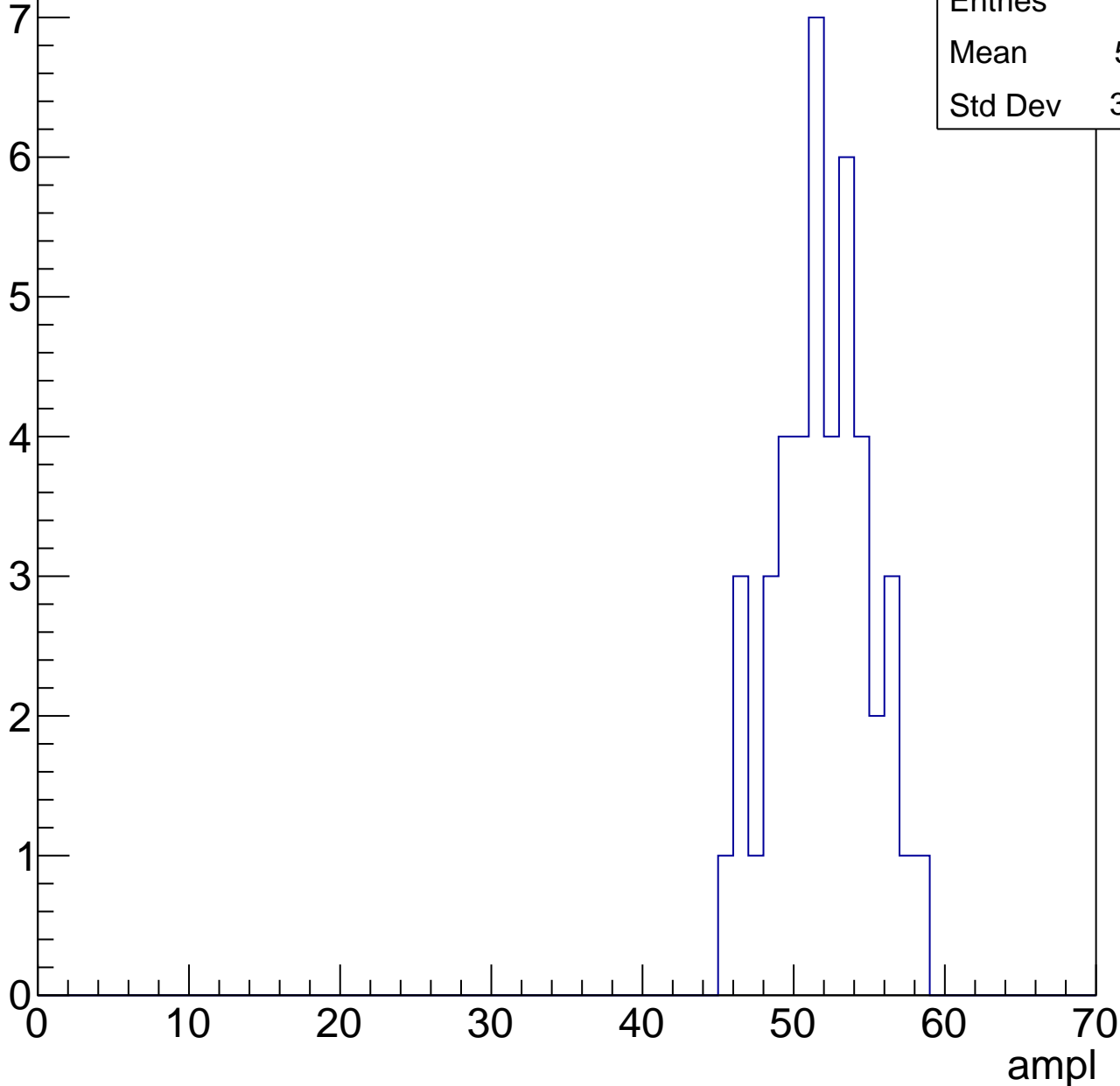


# B1L103S, U1-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	51.41
Std Dev	3.099

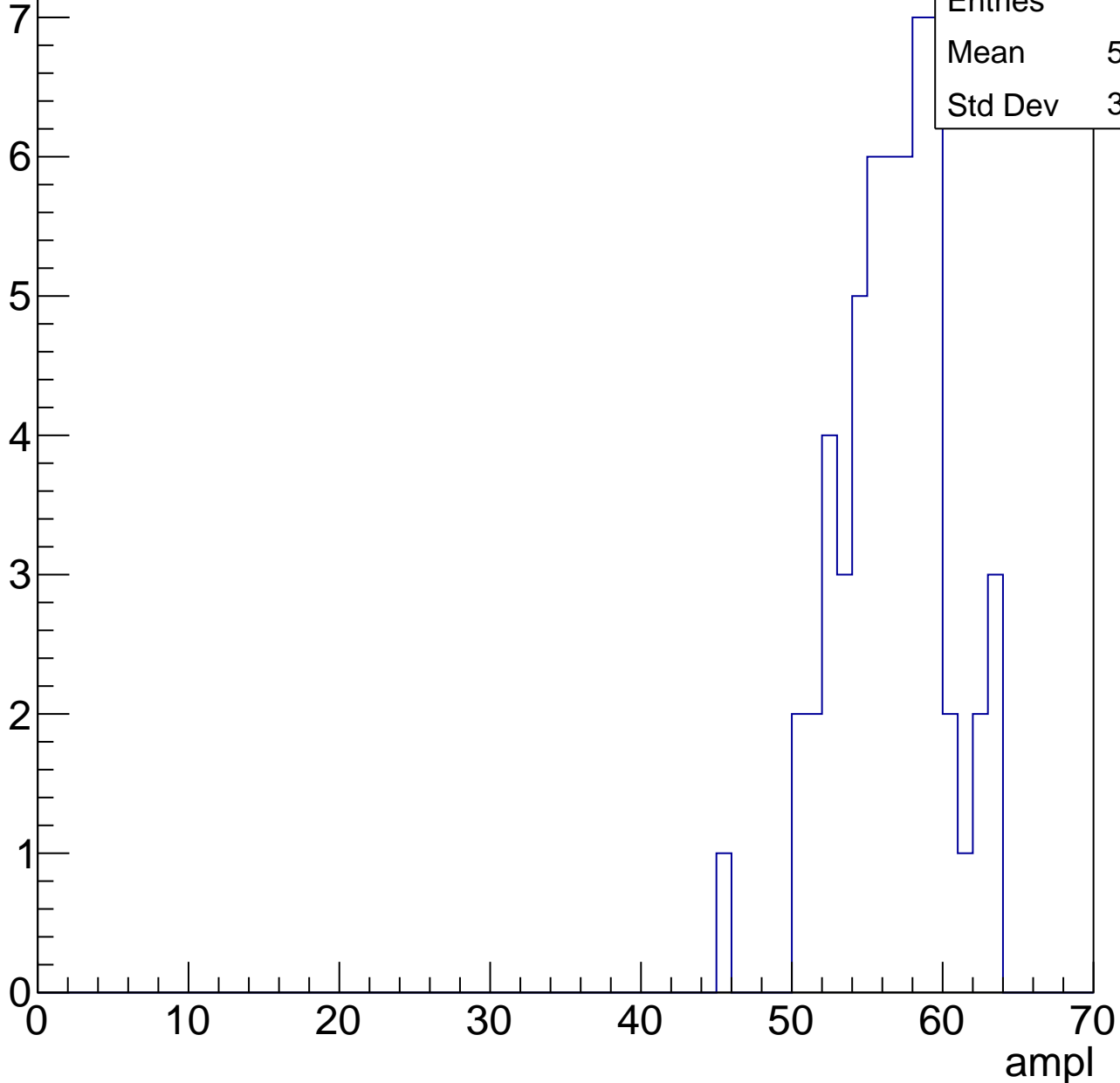


# B1L103S, U1-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	56.23
Std Dev	3.579

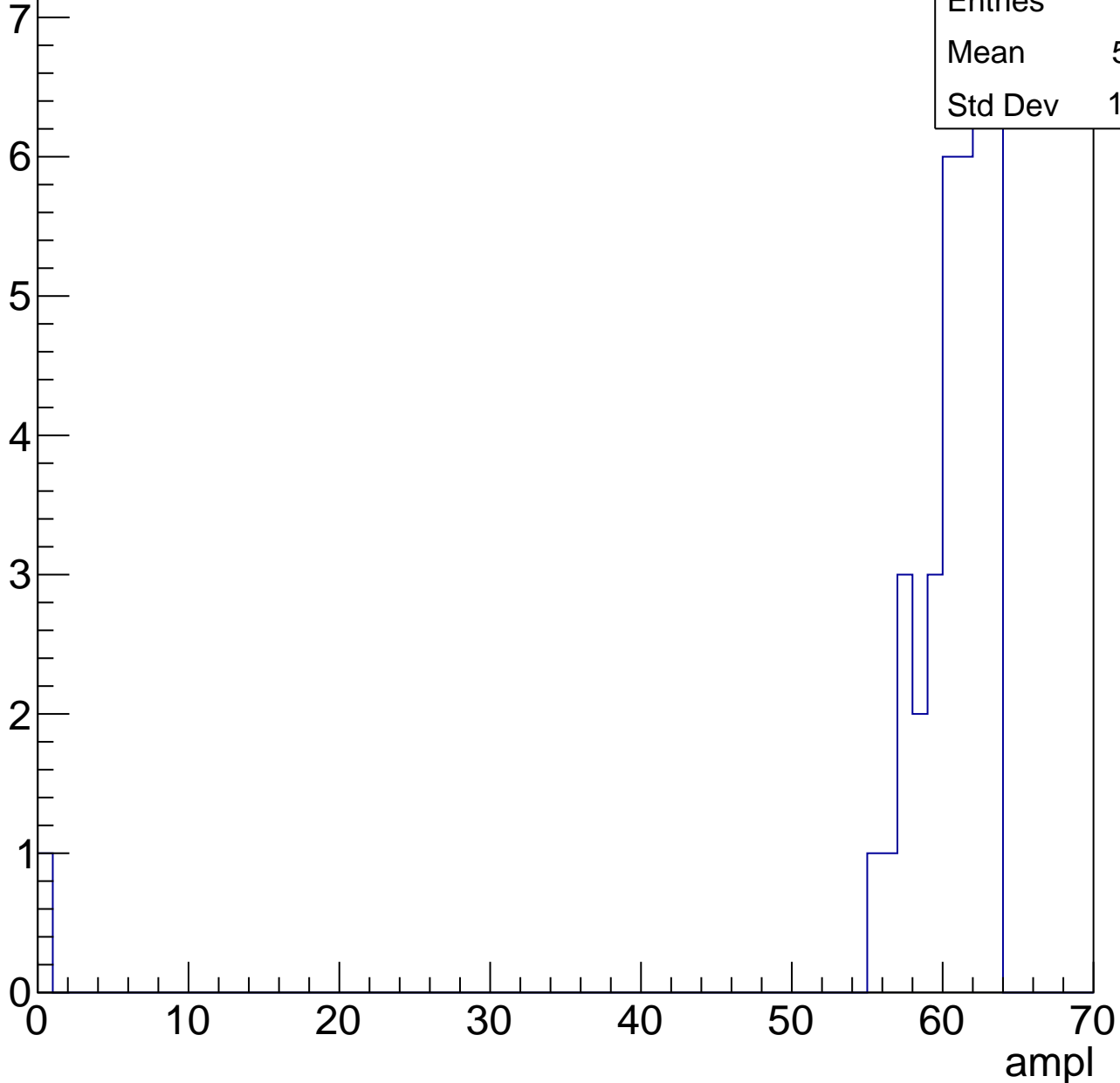


# B1L103S, U1-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	37
Mean	58.81
Std Dev	10.03

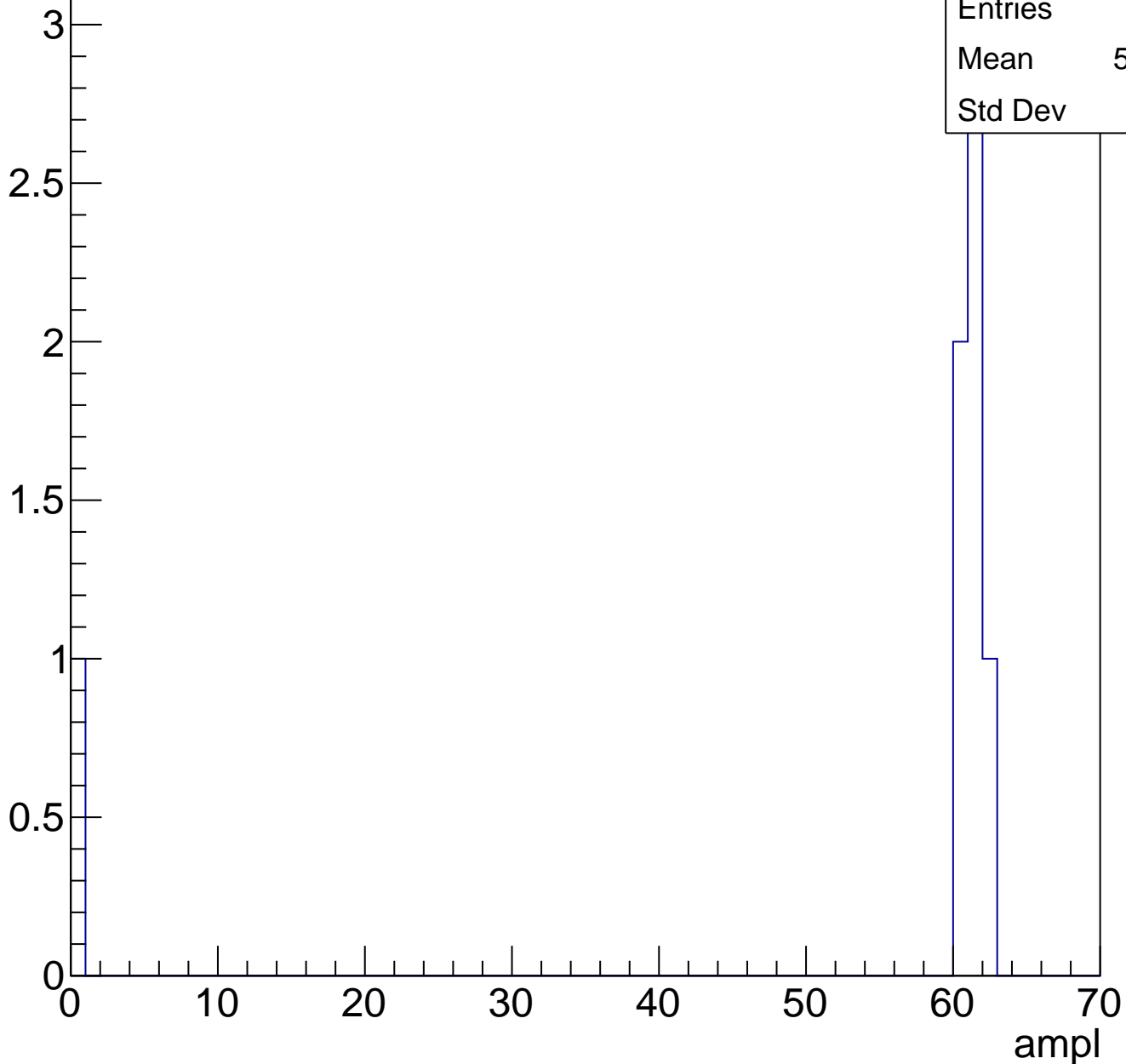




# B1L103S, U1-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch73, adc0

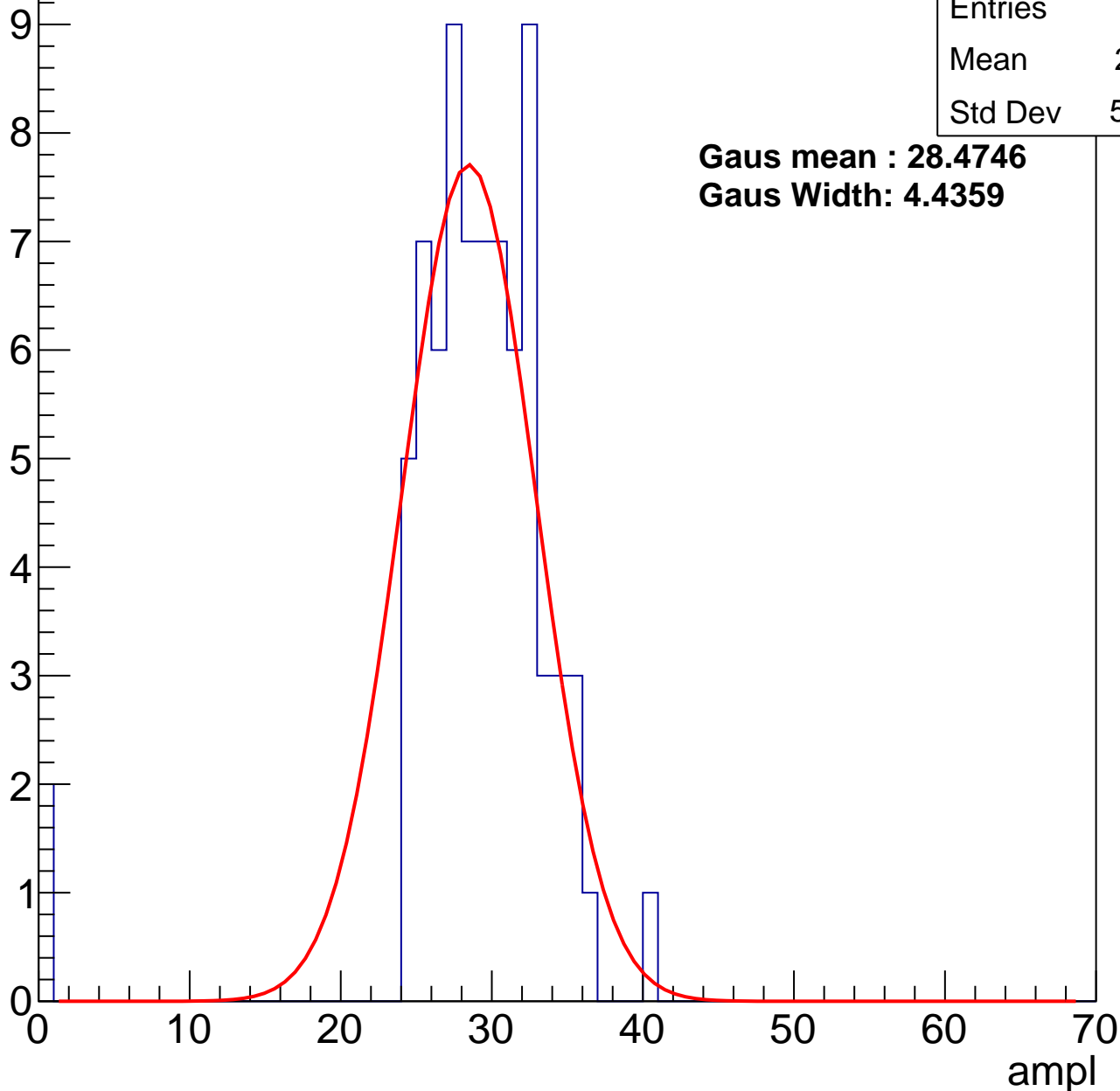
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	28.41
Std Dev	5.738

**Gaus mean : 28.4746**

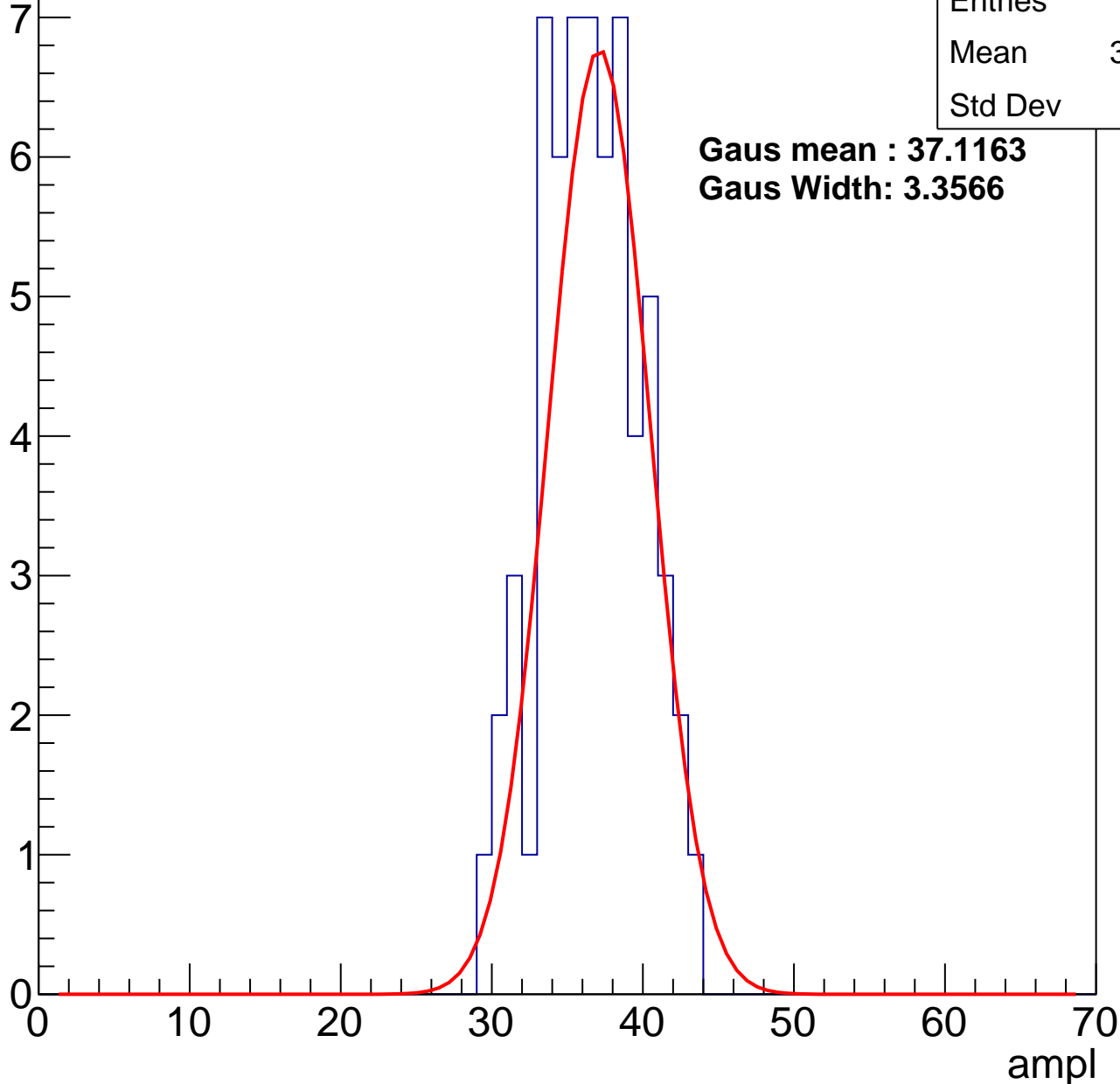
**Gaus Width: 4.4359**



# B1L103S, U1-ch73, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch73, adc2

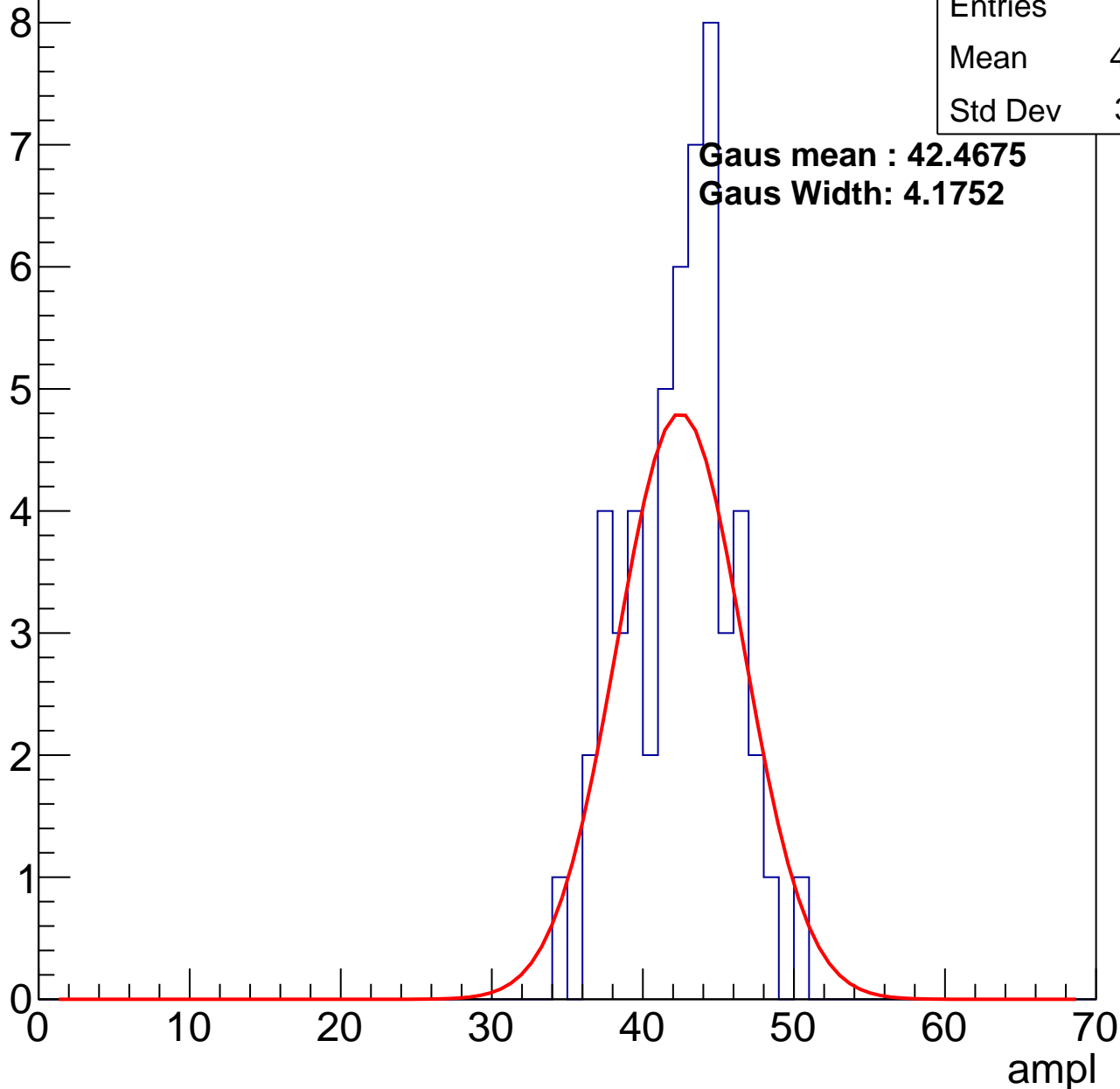
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	41.98
Std Dev	3.401

**Gaus mean : 42.4675**

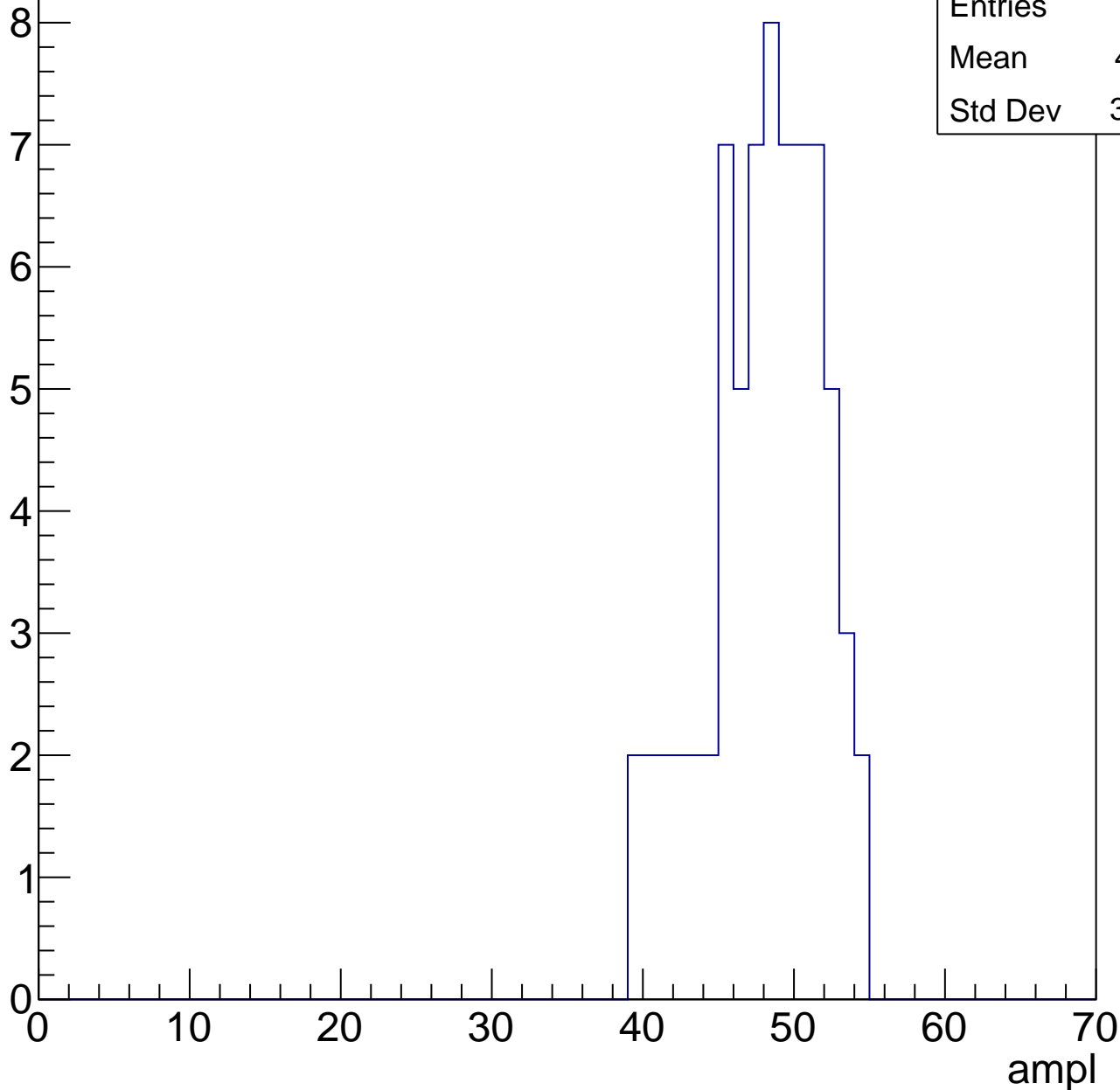
**Gaus Width: 4.1752**



# B1L103S, U1-ch73, adc3

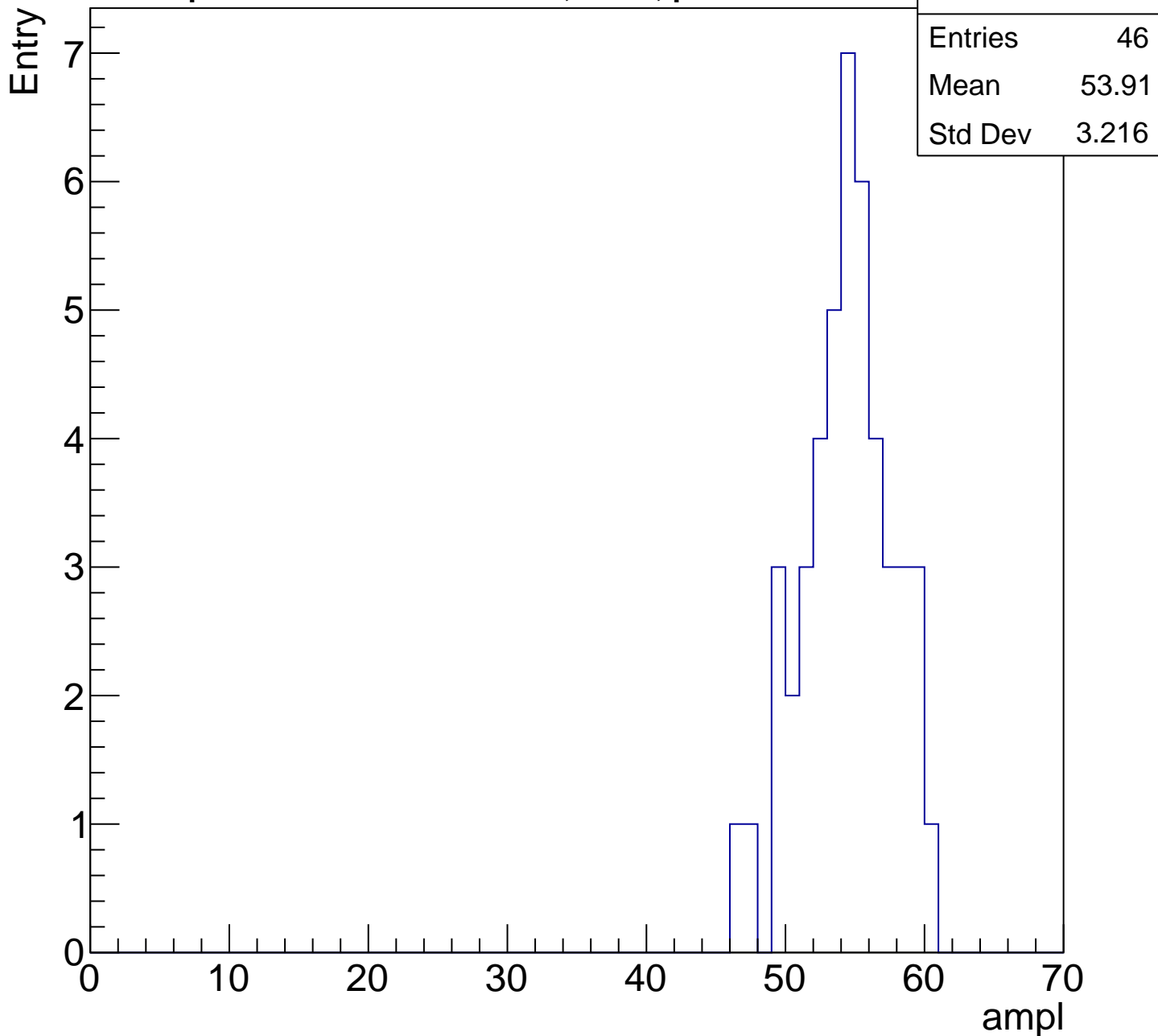
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

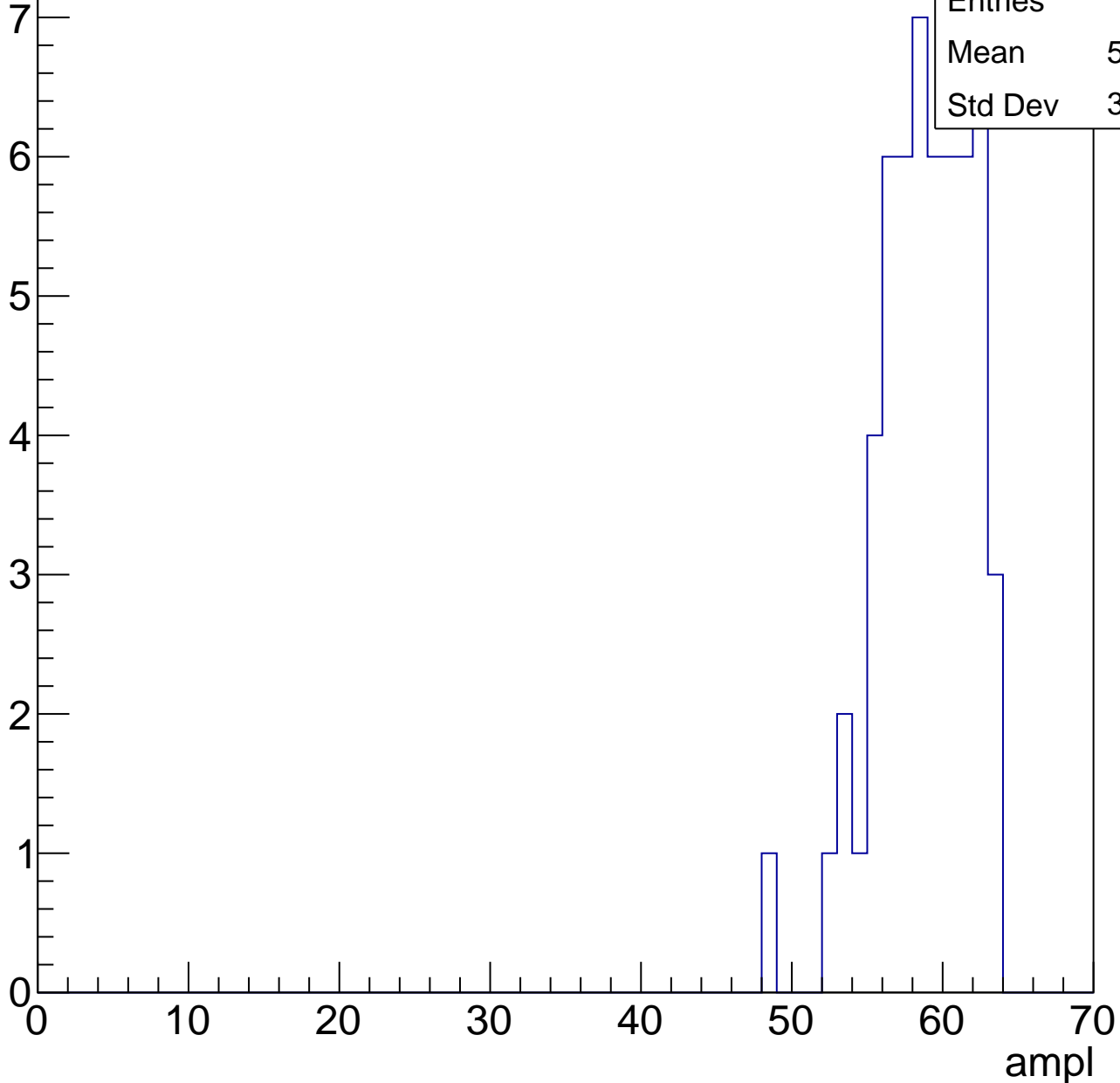


# B1L103S, U1-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	58.34
Std Dev	3.084

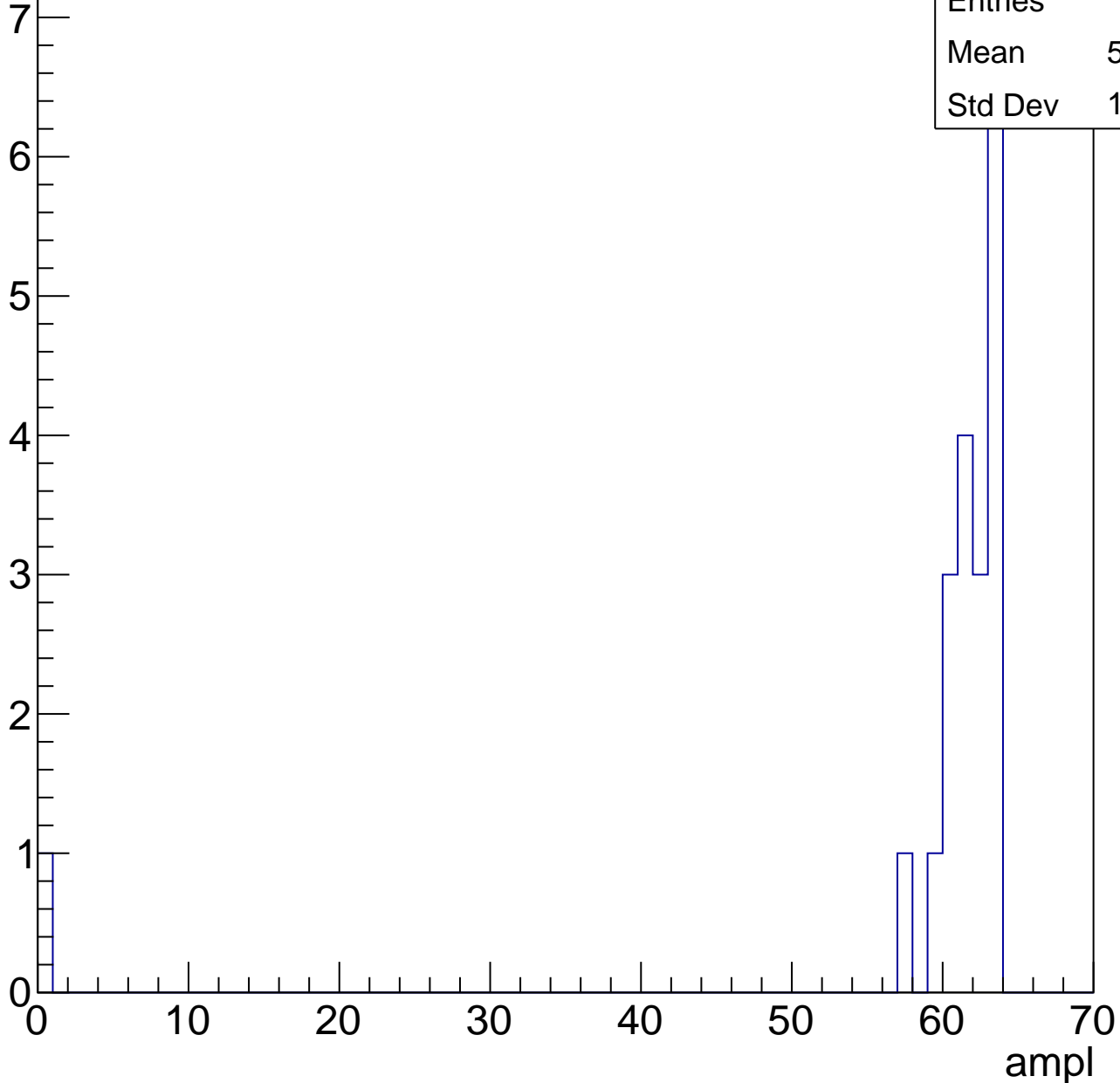


# B1L103S, U1-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	20
Mean	58.35
Std Dev	13.48





# B1L103S, U1-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U1-ch74, adc0

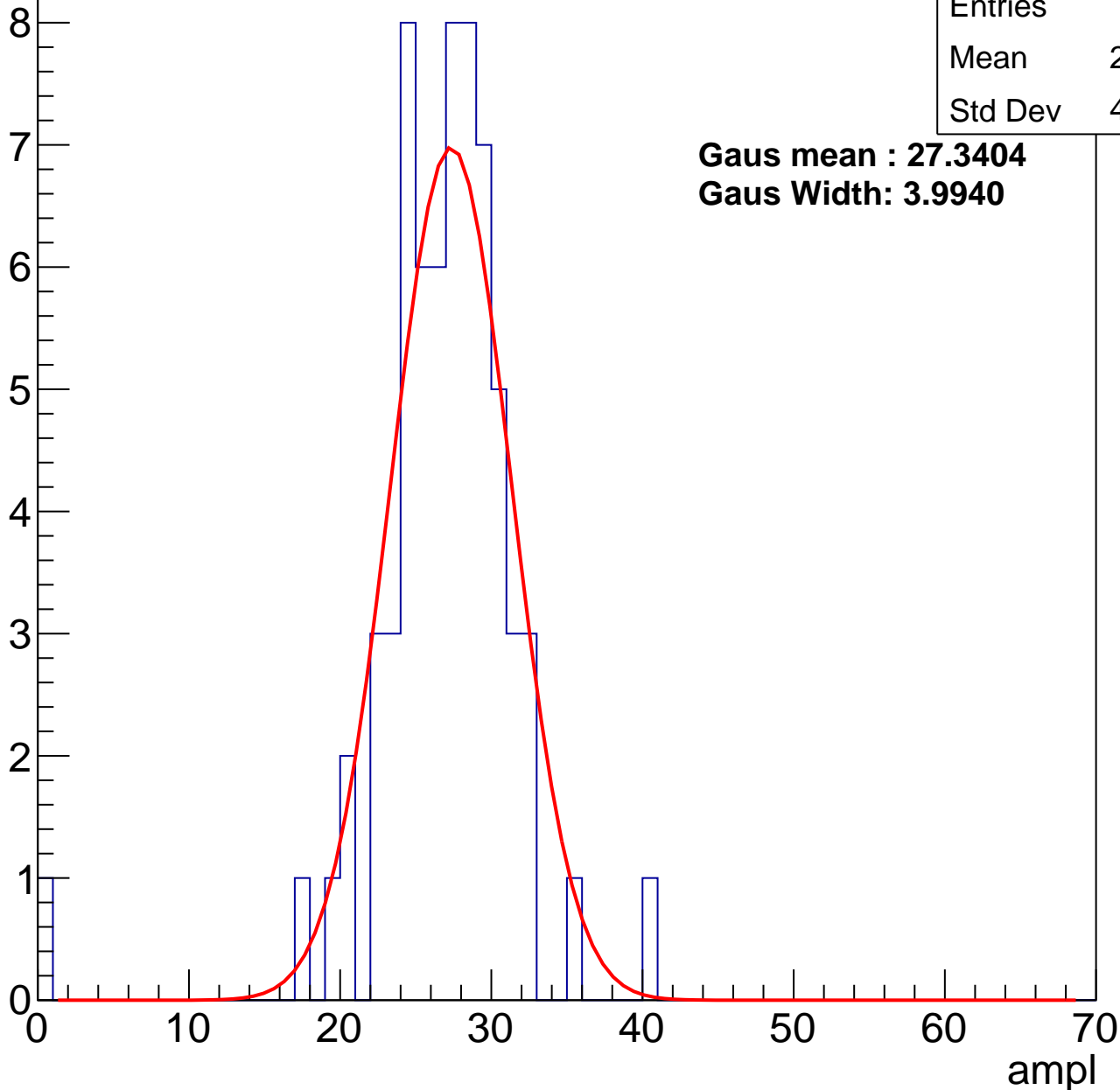
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	26.36
Std Dev	4.925

**Gaus mean : 27.3404**

**Gaus Width: 3.9940**



# B1L103S, U1-ch74, adc1

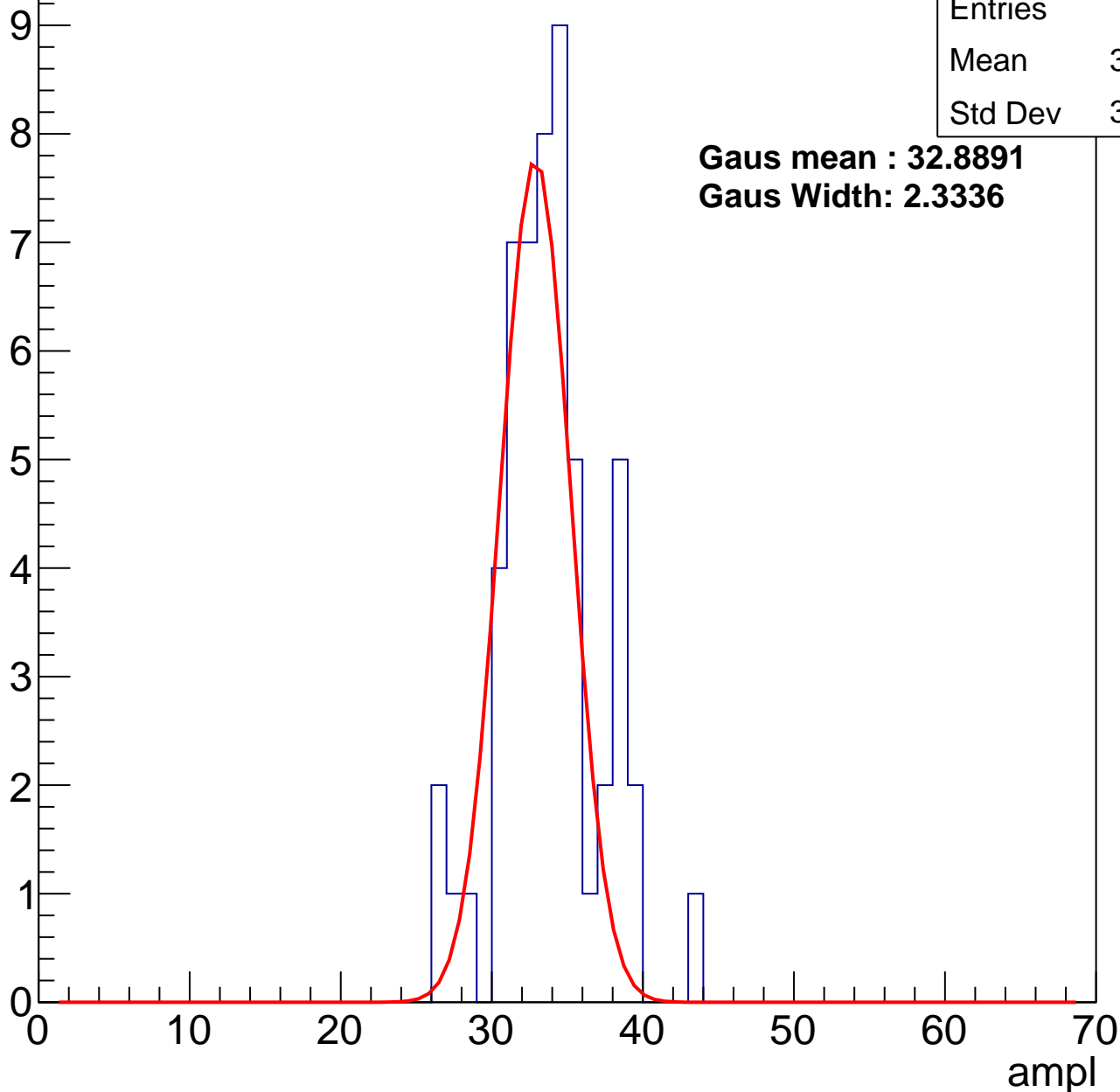
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	33.35
Std Dev	3.276

**Gaus mean : 32.8891**

**Gaus Width: 2.3336**



# B1L103S, U1-ch74, adc2

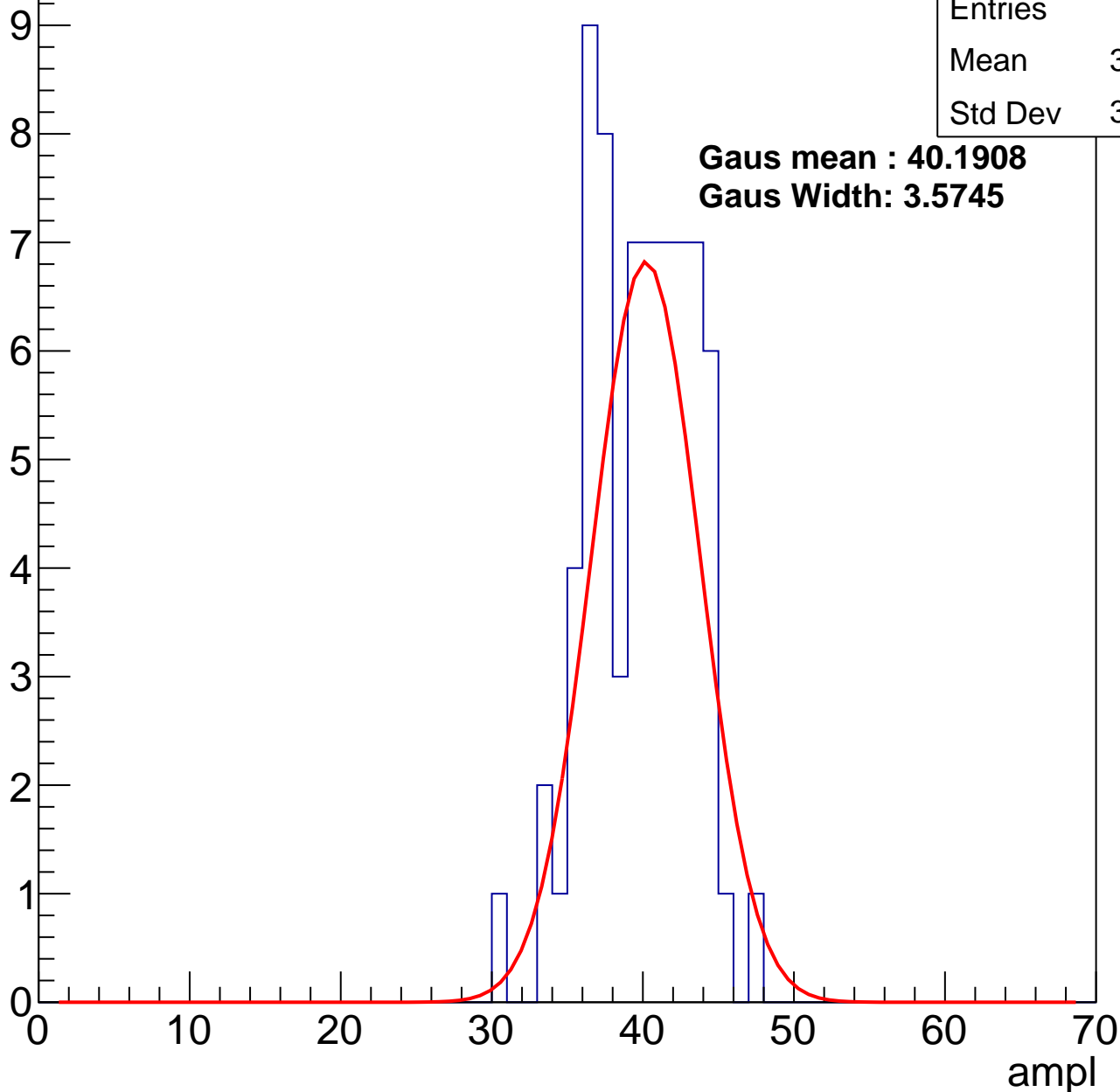
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	39.37
Std Dev	3.374

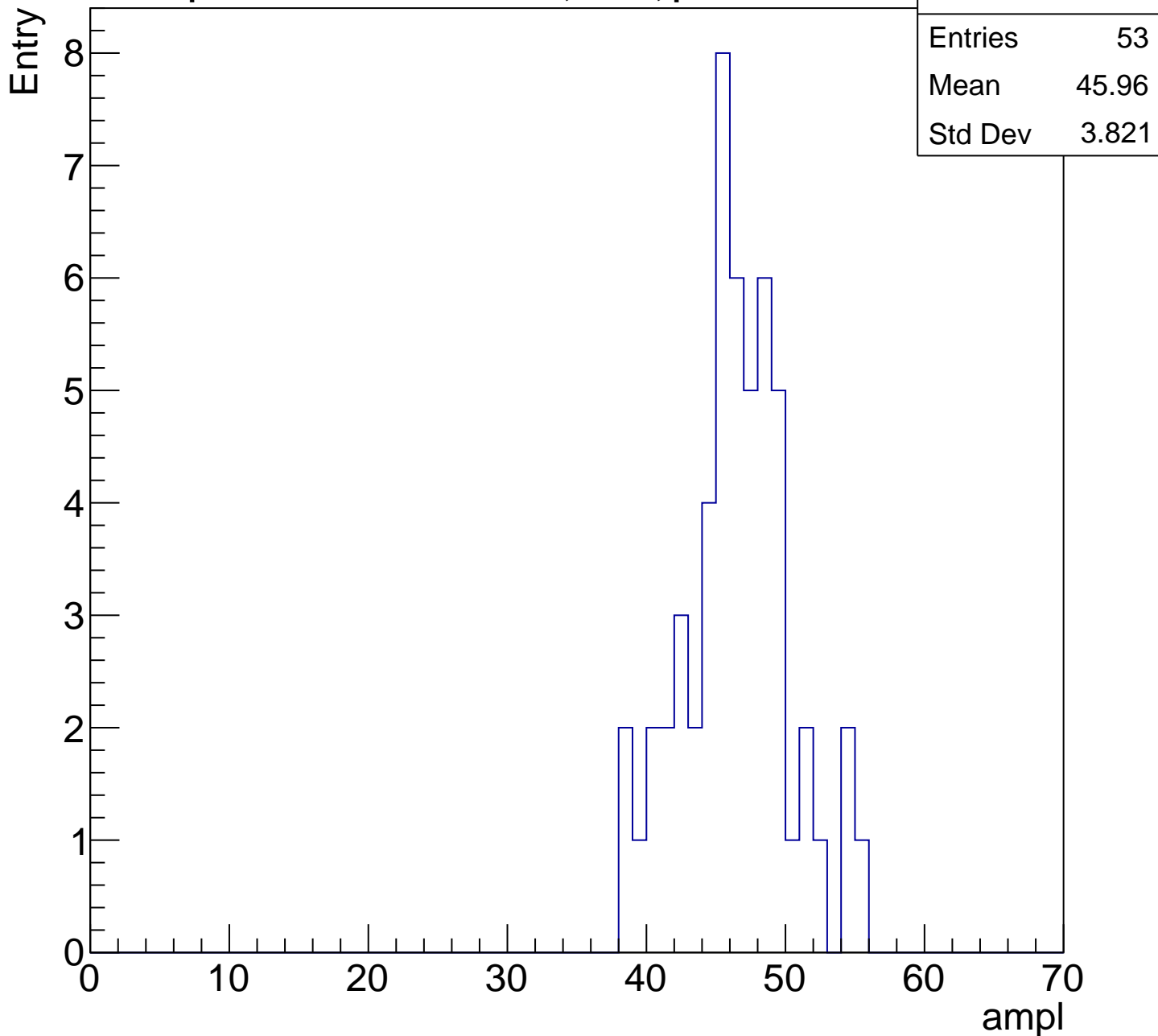
**Gaus mean : 40.1908**

**Gaus Width: 3.5745**



# B1L103S, U1-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

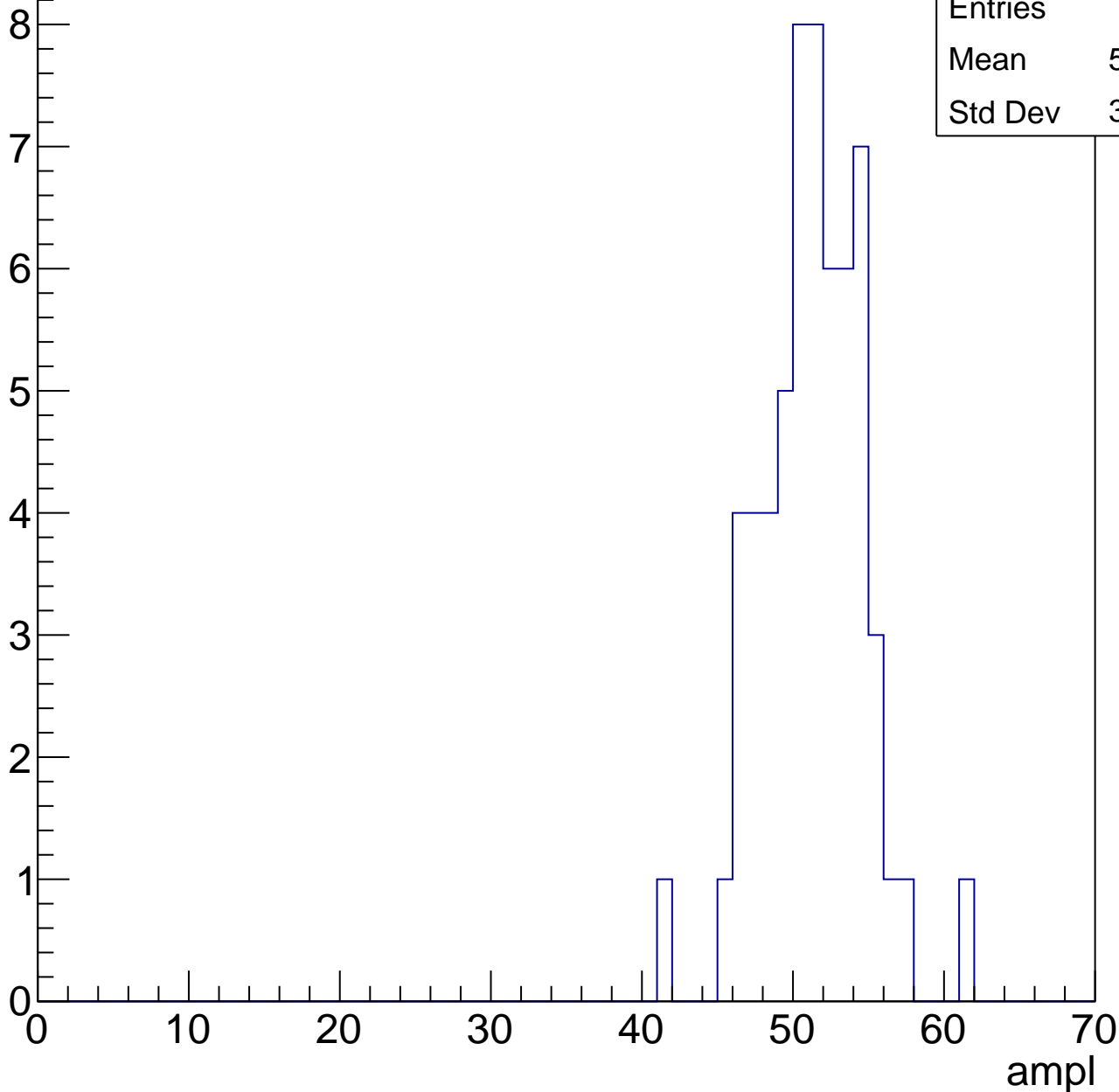


# B1L103S, U1-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

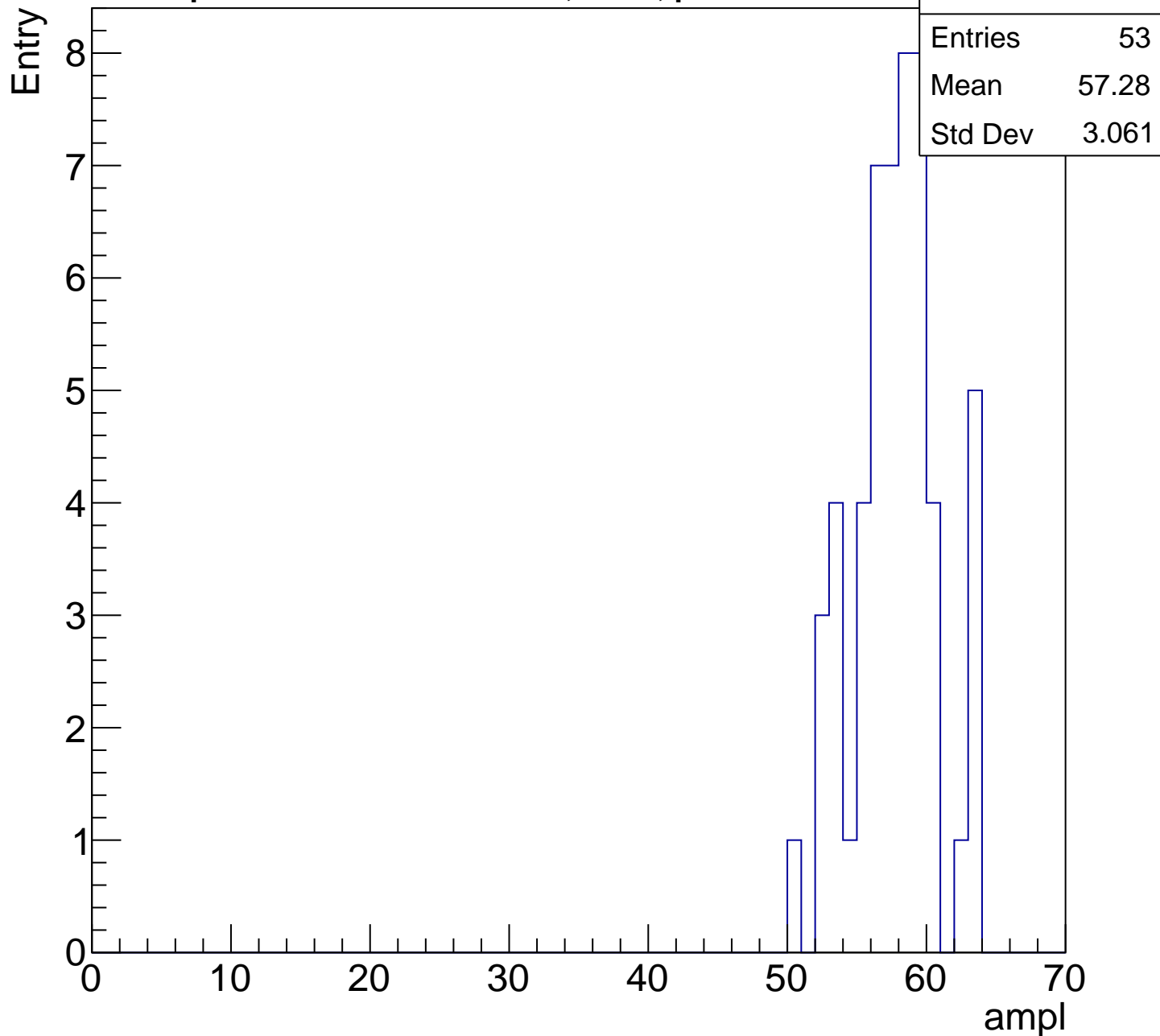
Entry

Entries	60
Mean	50.83
Std Dev	3.327



# B1L103S, U1-ch74, adc5

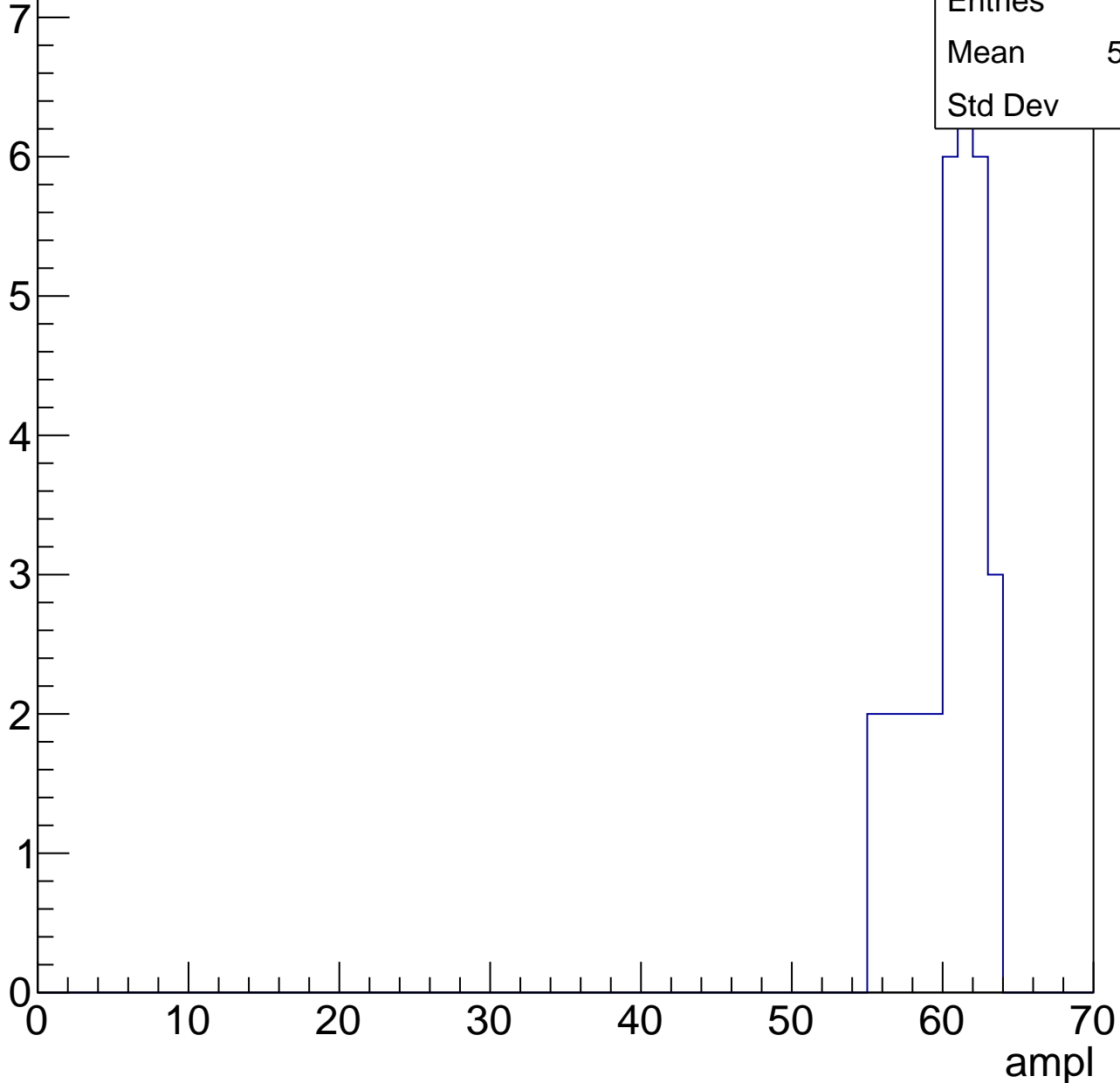
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U1-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

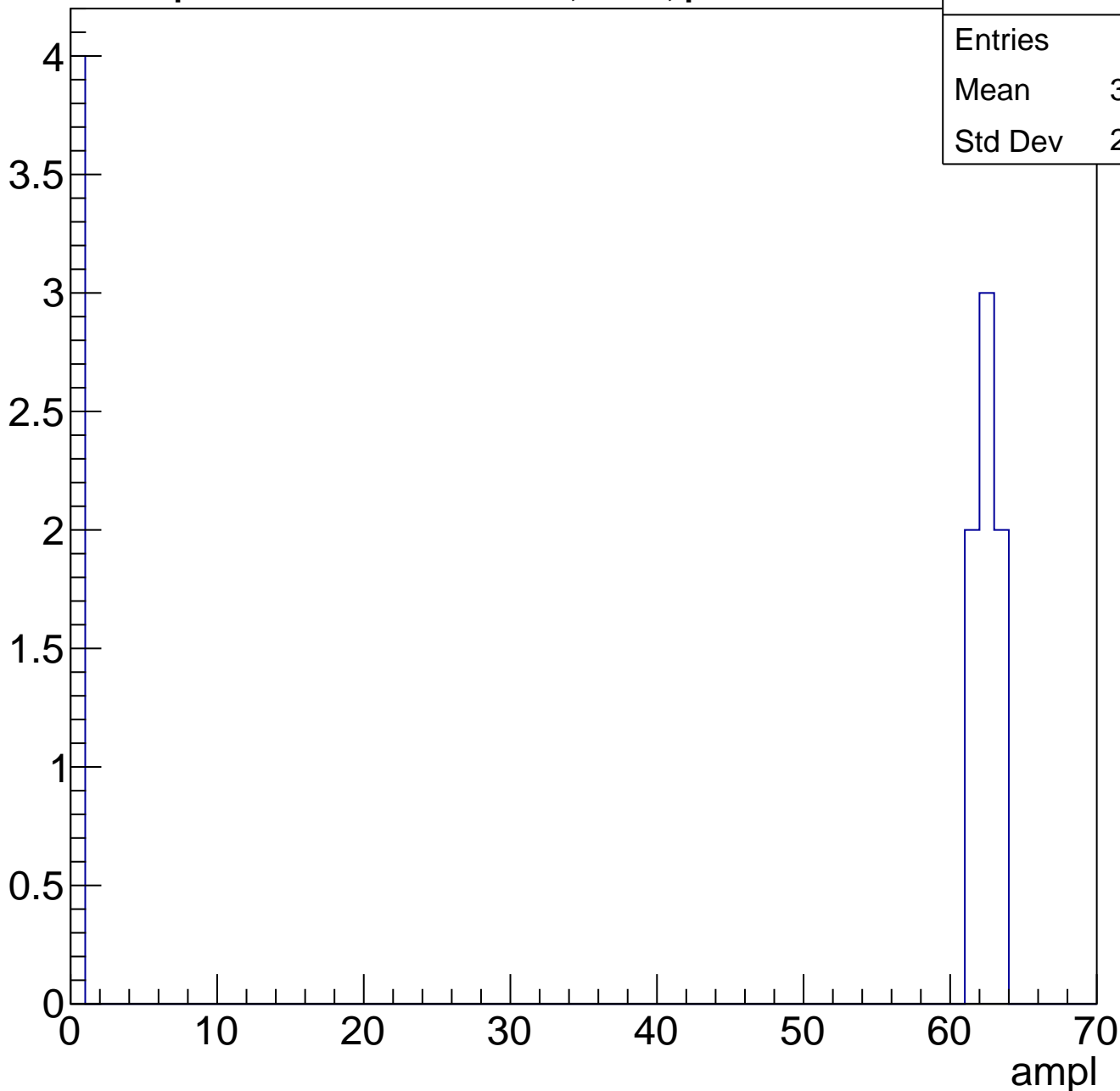




# B1L103S, U1-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	11
Mean	39.45
Std Dev	29.83

# B1L103S, U1-ch75, adc0

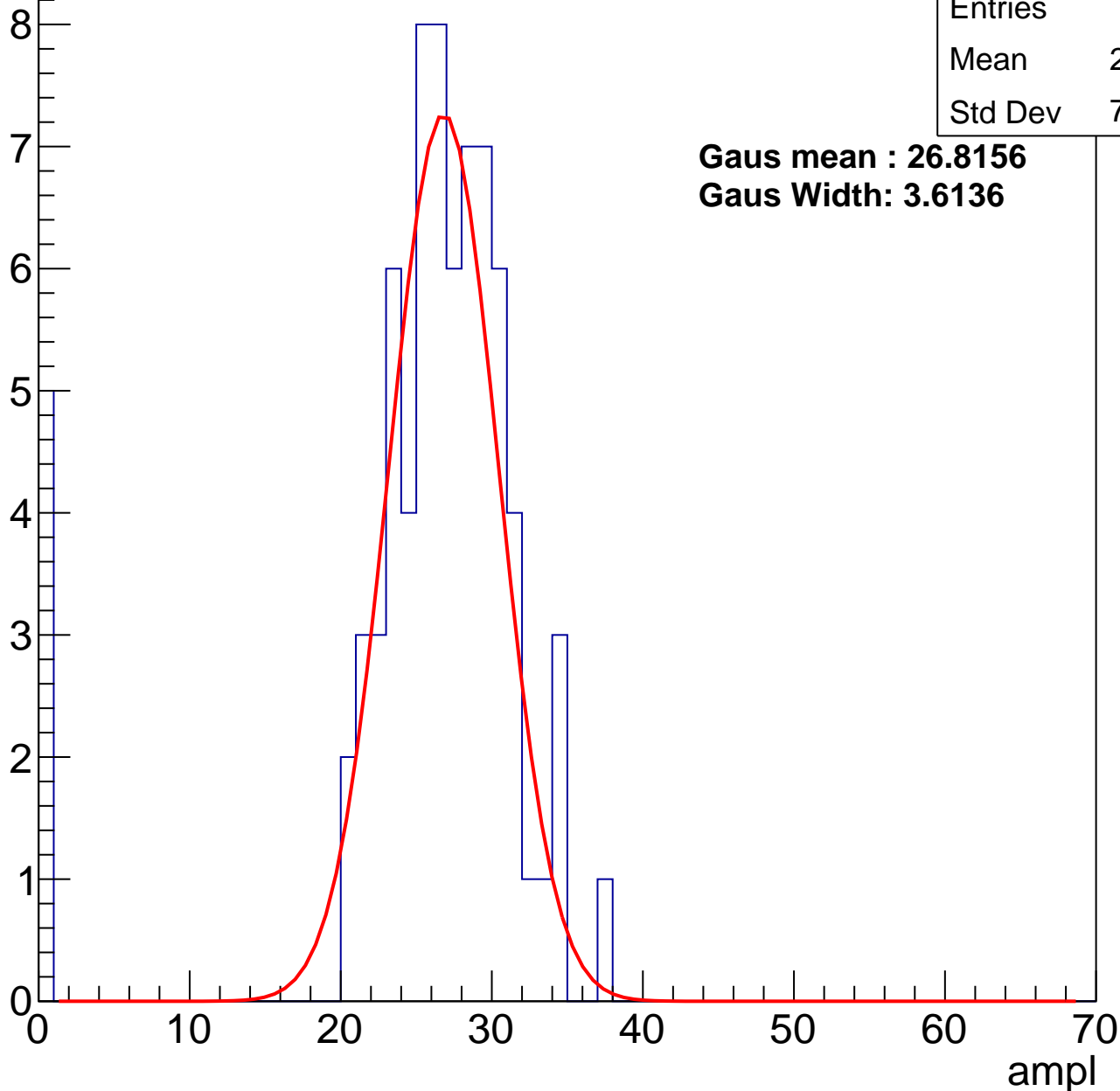
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	25.07
Std Dev	7.553

**Gaus mean : 26.8156**

**Gaus Width: 3.6136**



# B1L103S, U1-ch75, adc1

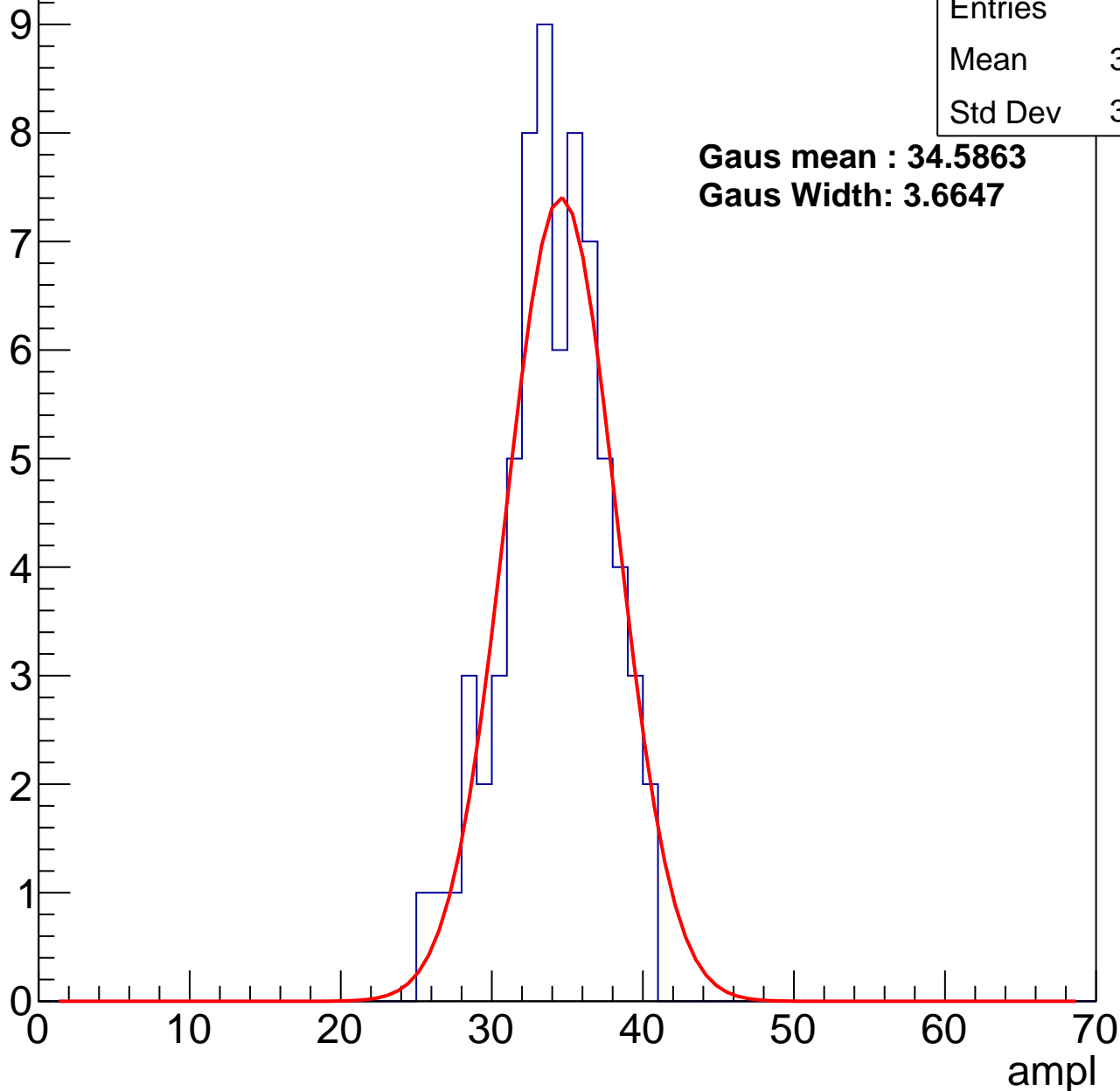
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	33.65
Std Dev	3.364

**Gaus mean : 34.5863**

**Gaus Width: 3.6647**



# B1L103S, U1-ch75, adc2

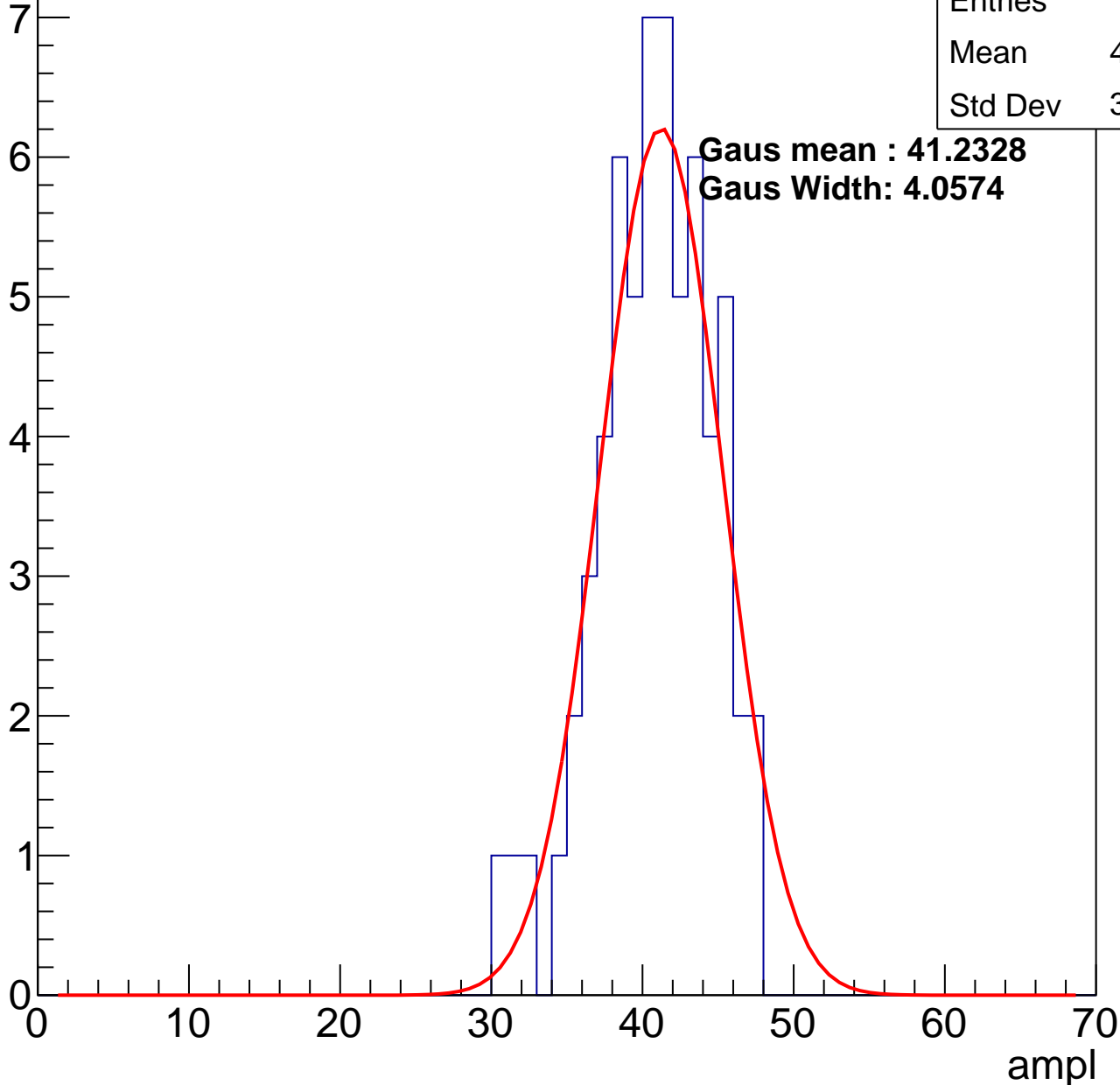
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	40.29
Std Dev	3.765

**Gaus mean : 41.2328**

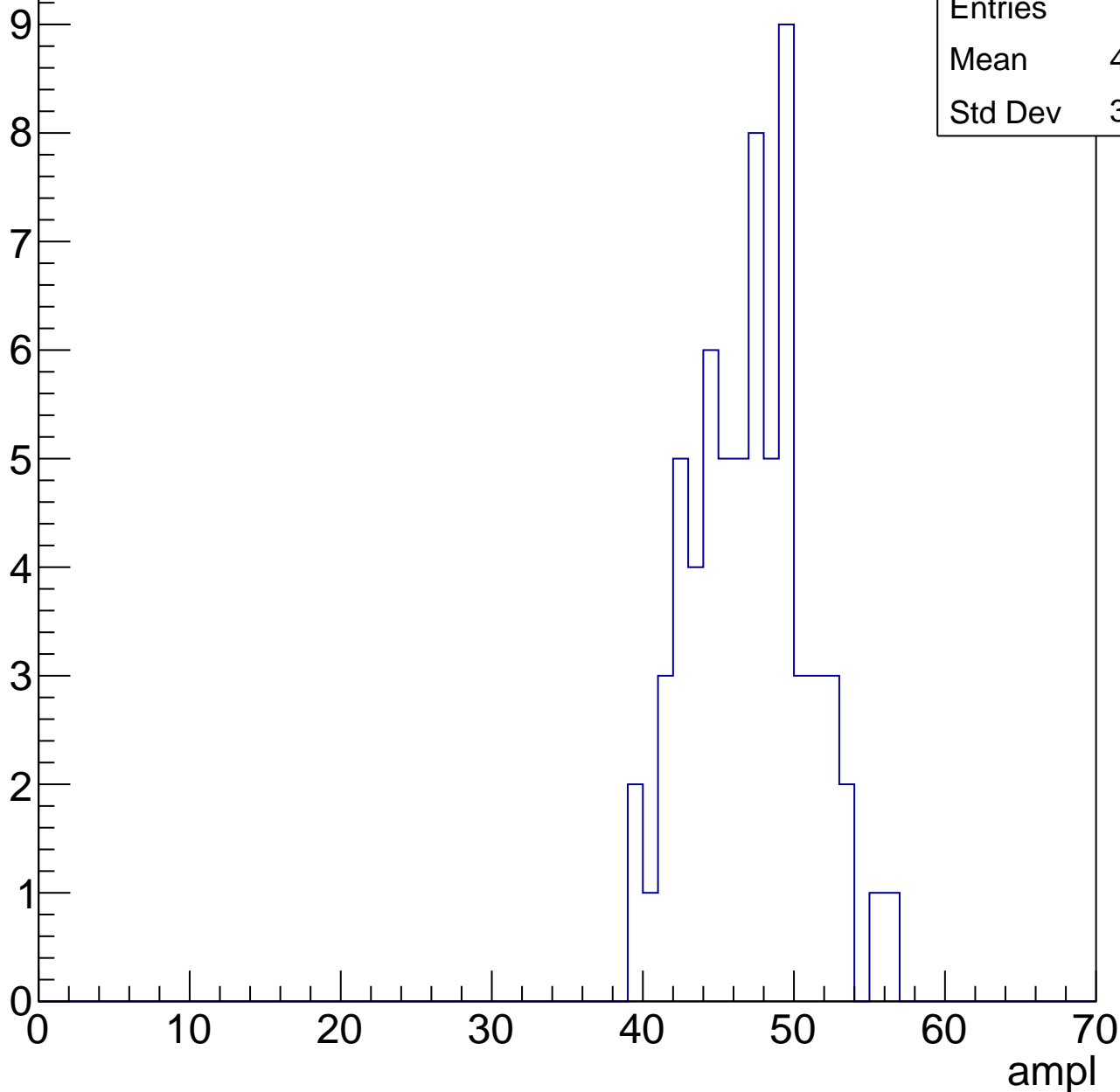
**Gaus Width: 4.0574**



# B1L103S, U1-ch75, adc3

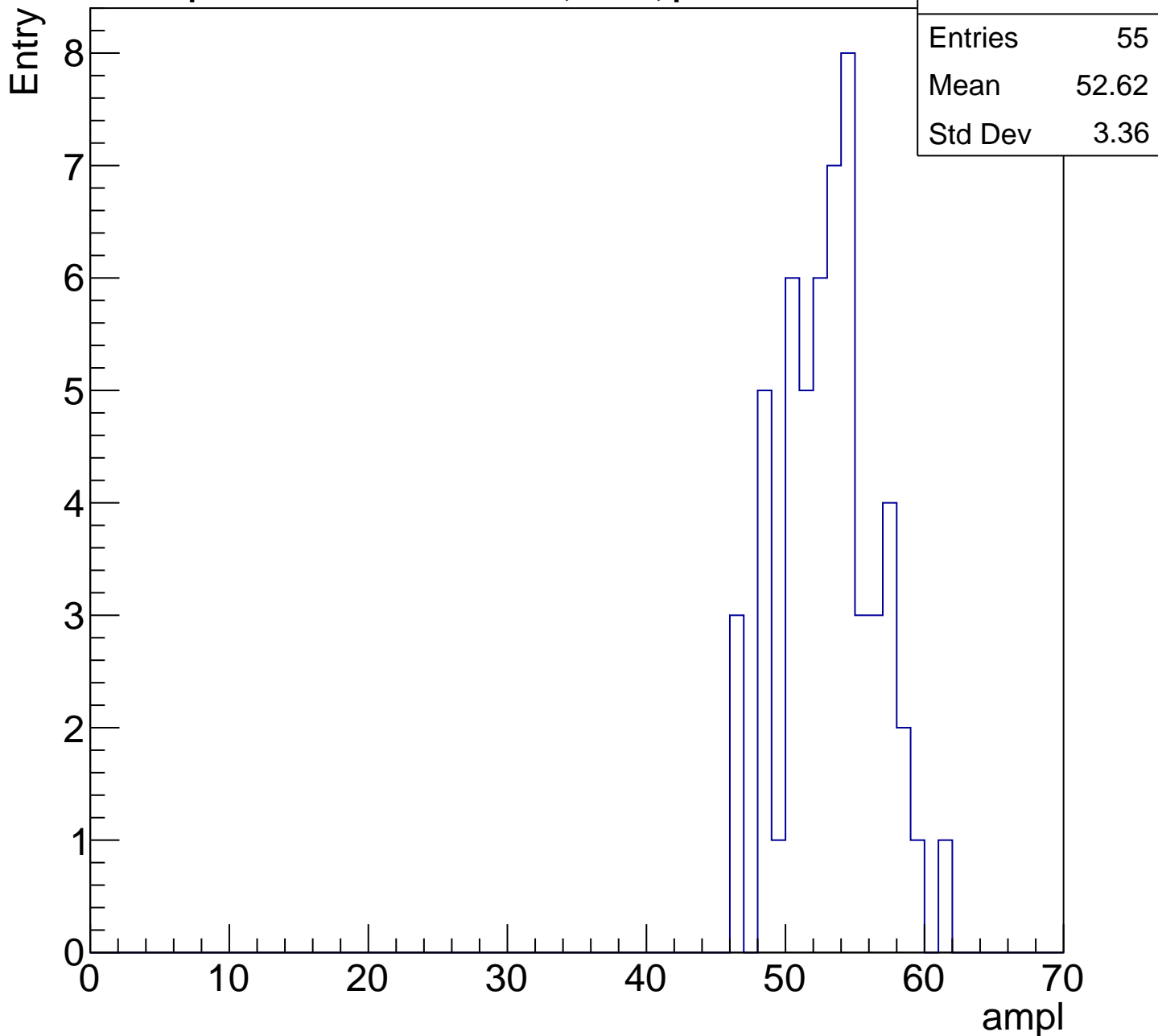
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

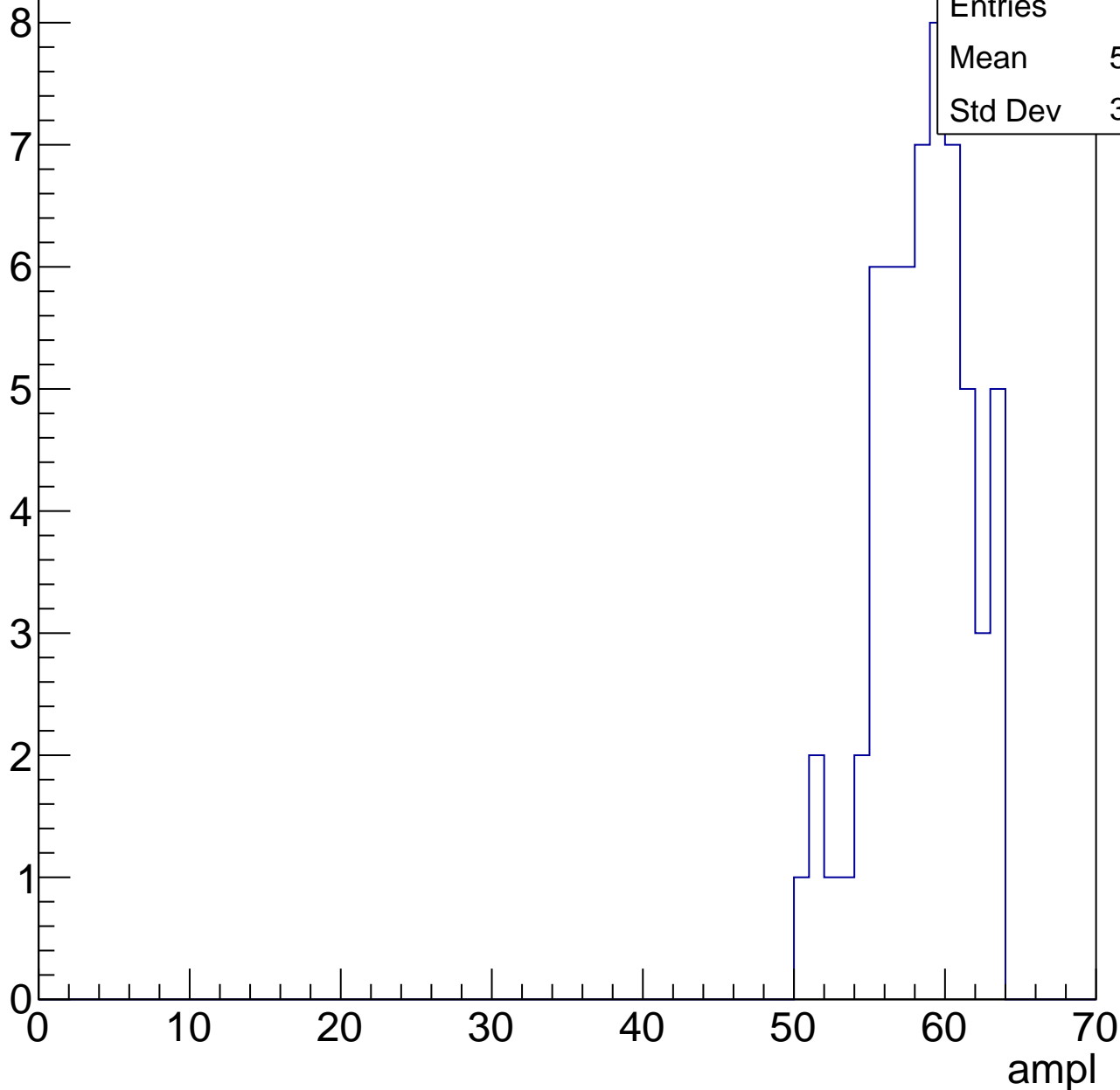


# B1L103S, U1-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	57.95
Std Dev	3.143

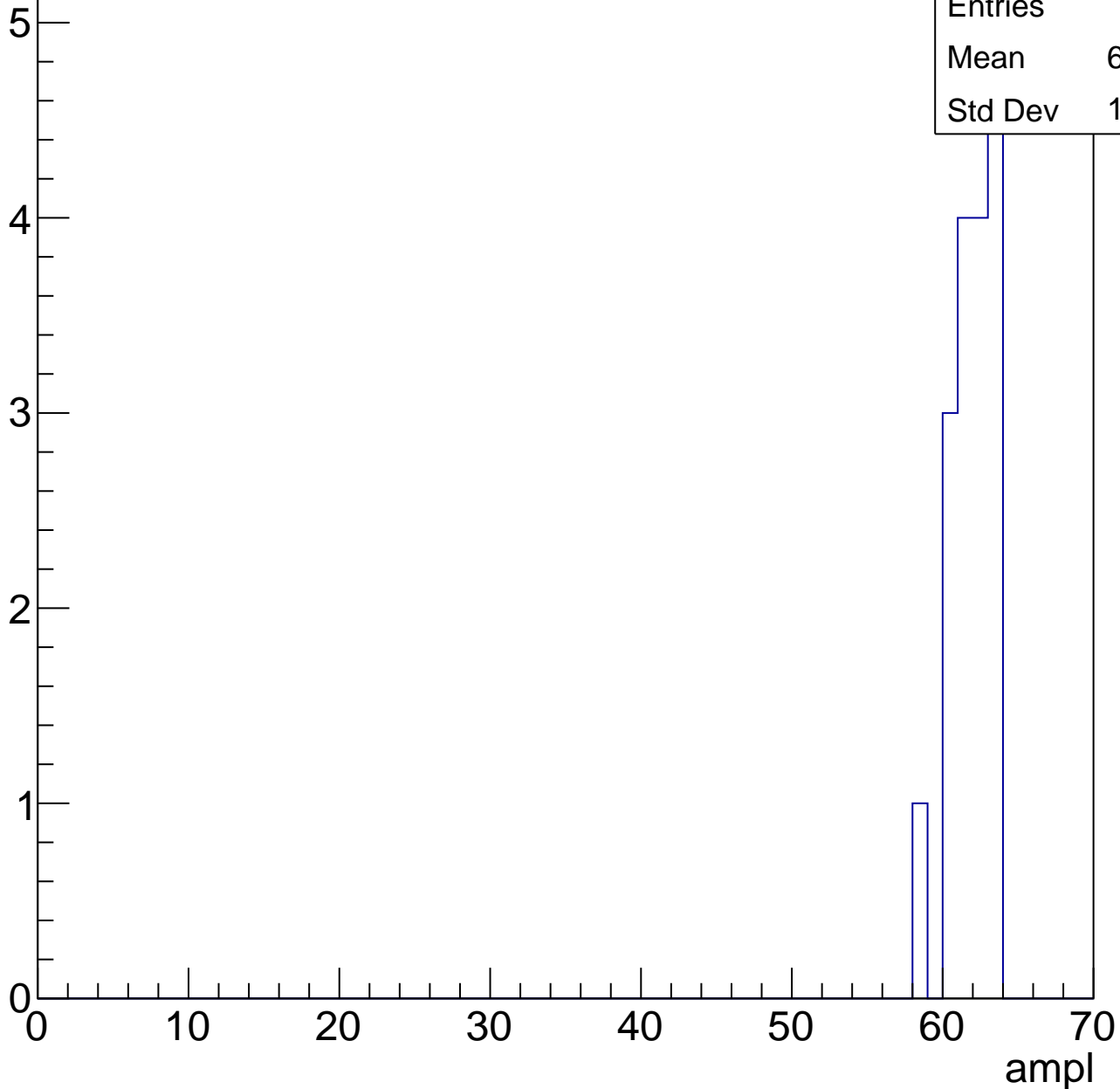


# B1L103S, U1-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	17
Mean	61.47
Std Dev	1.377

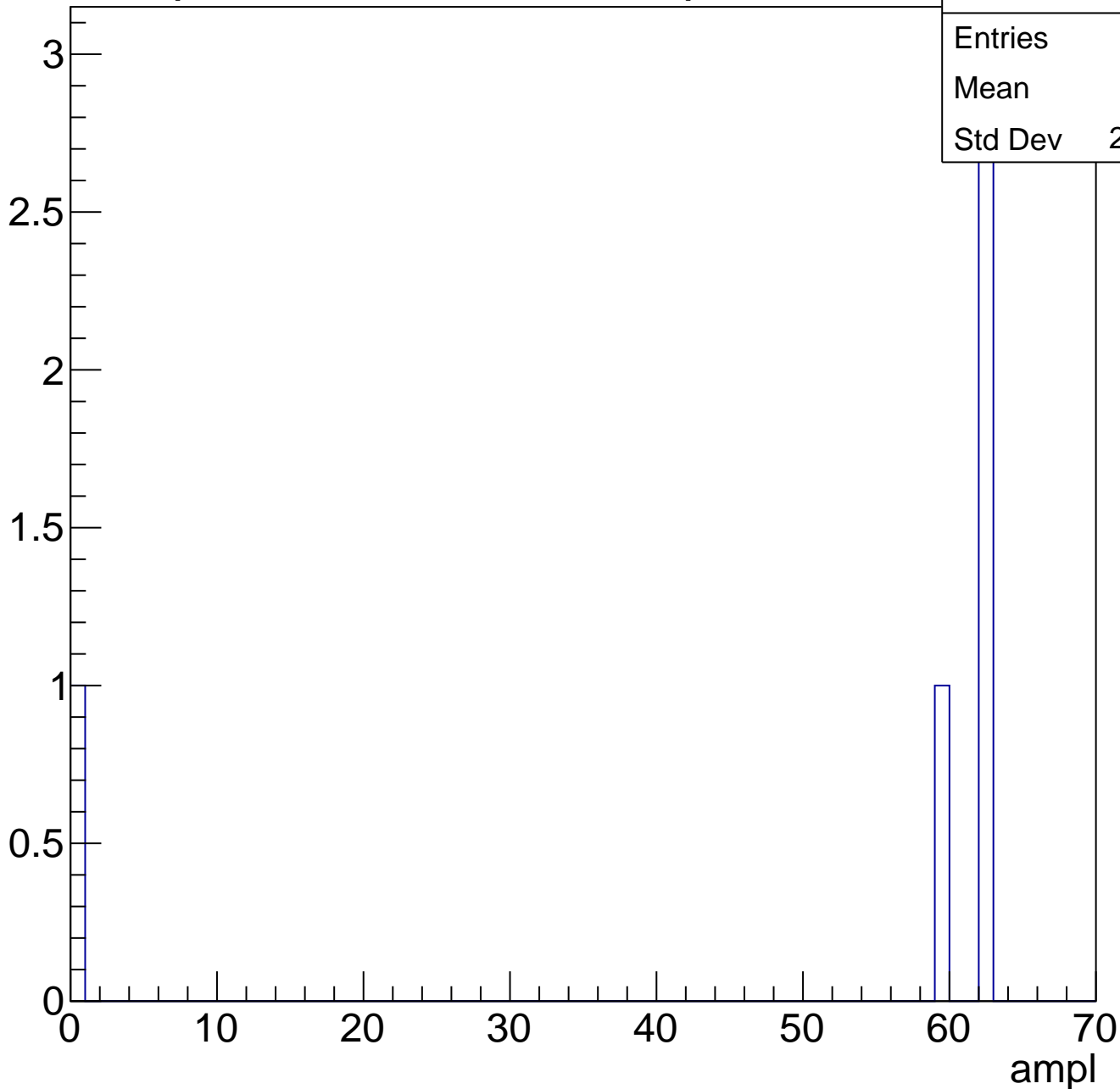




# B1L103S, U1-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch76, adc0

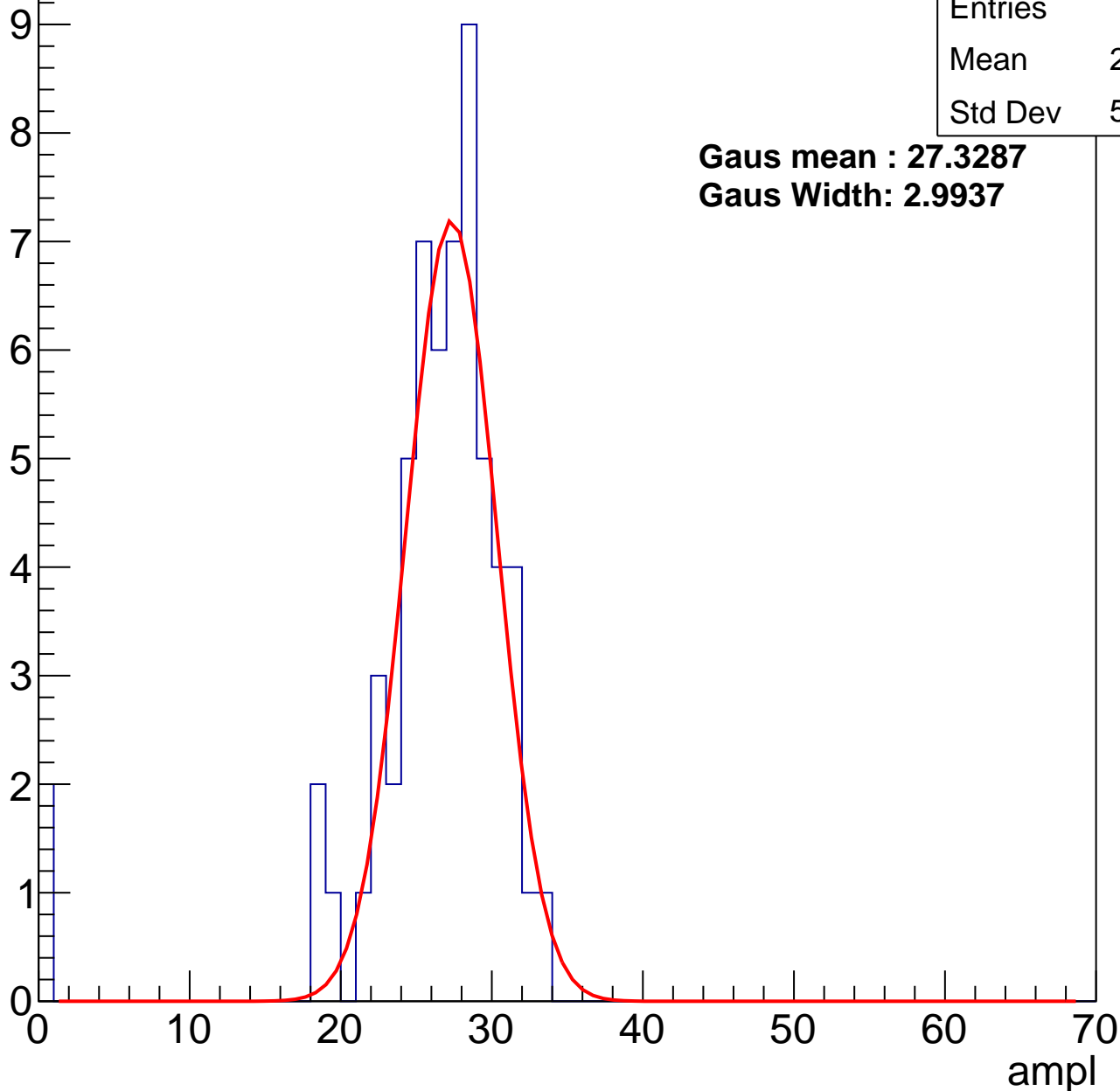
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	25.57
Std Dev	5.734

**Gaus mean : 27.3287**

**Gaus Width: 2.9937**



# B1L103S, U1-ch76, adc1

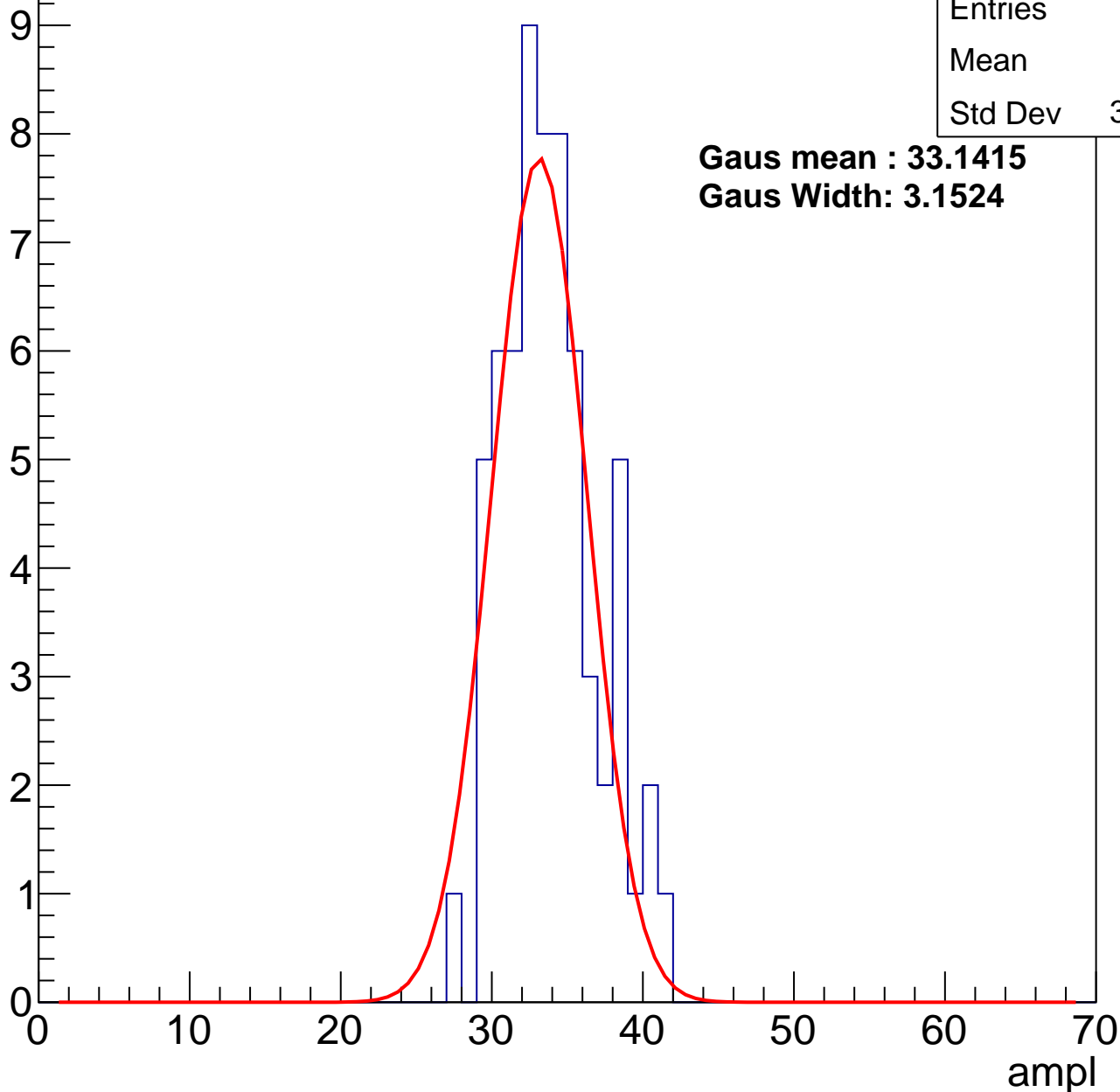
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	33.4
Std Dev	3.104

**Gaus mean : 33.1415**

**Gaus Width: 3.1524**



# B1L103S, U1-ch76, adc2

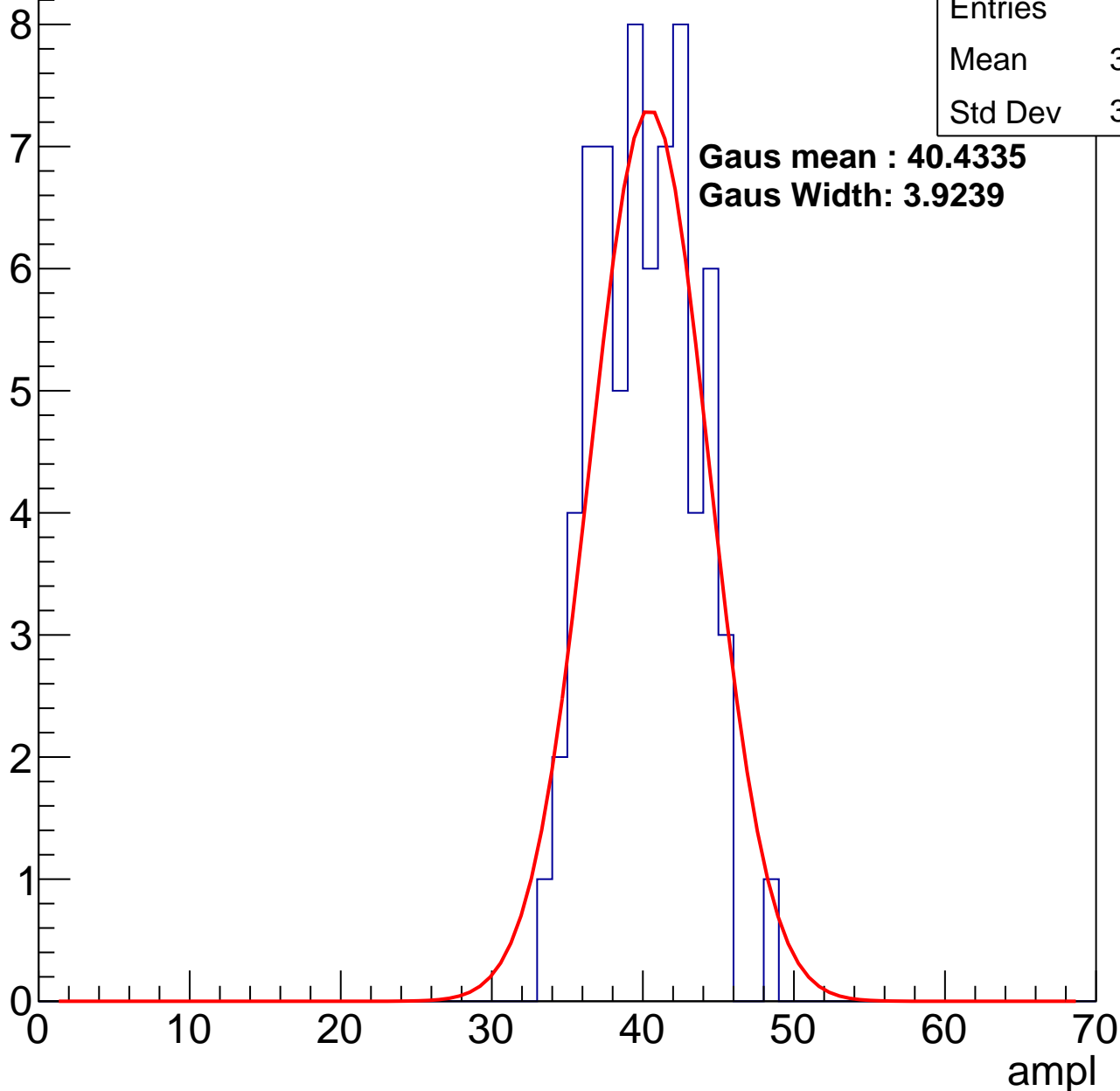
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	39.65
Std Dev	3.243

**Gaus mean : 40.4335**

**Gaus Width: 3.9239**

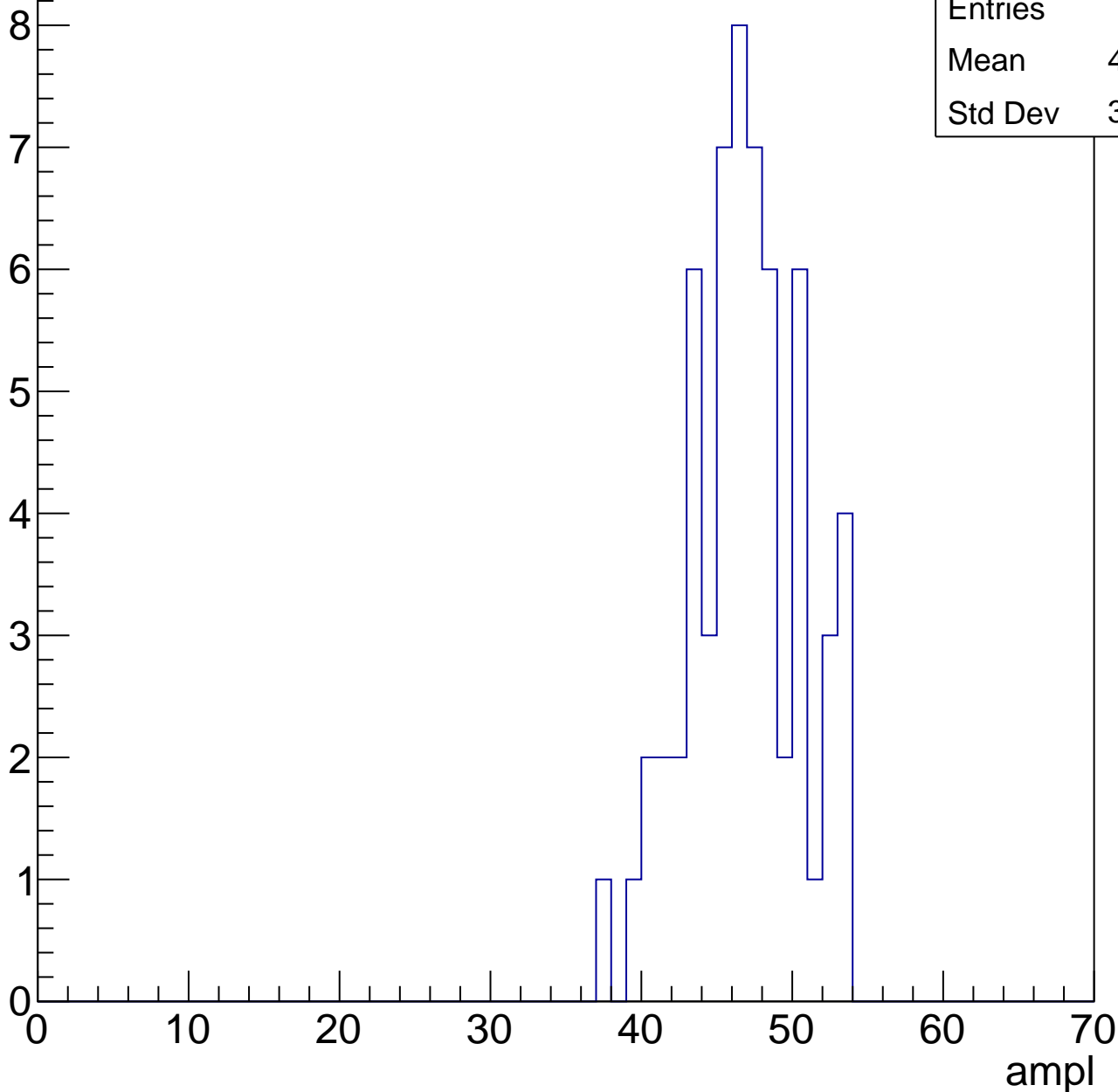


# B1L103S, U1-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	46.38
Std Dev	3.672

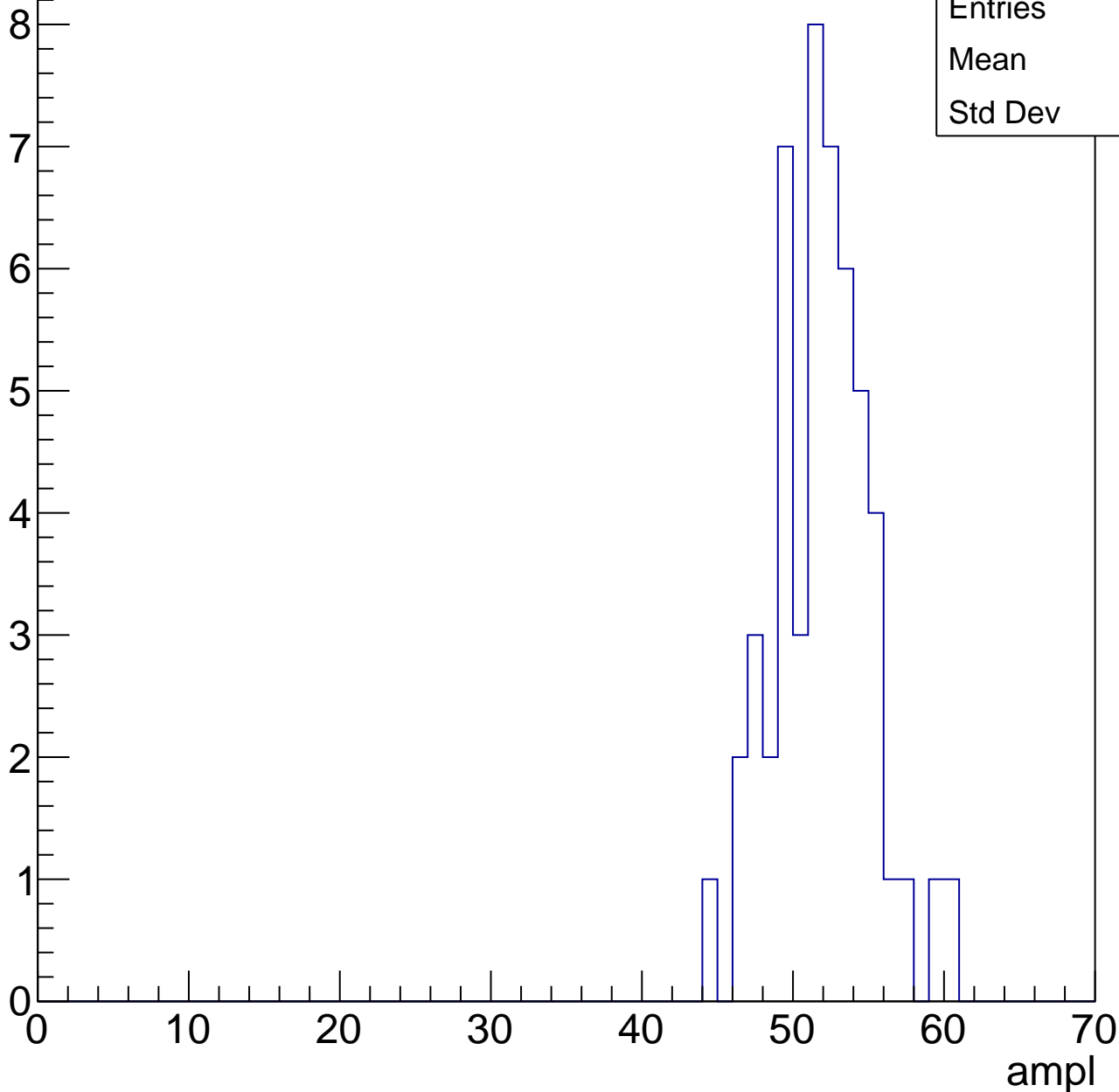


# B1L103S, U1-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	51.5
Std Dev	3.19



# B1L103S, U1-ch76, adc5

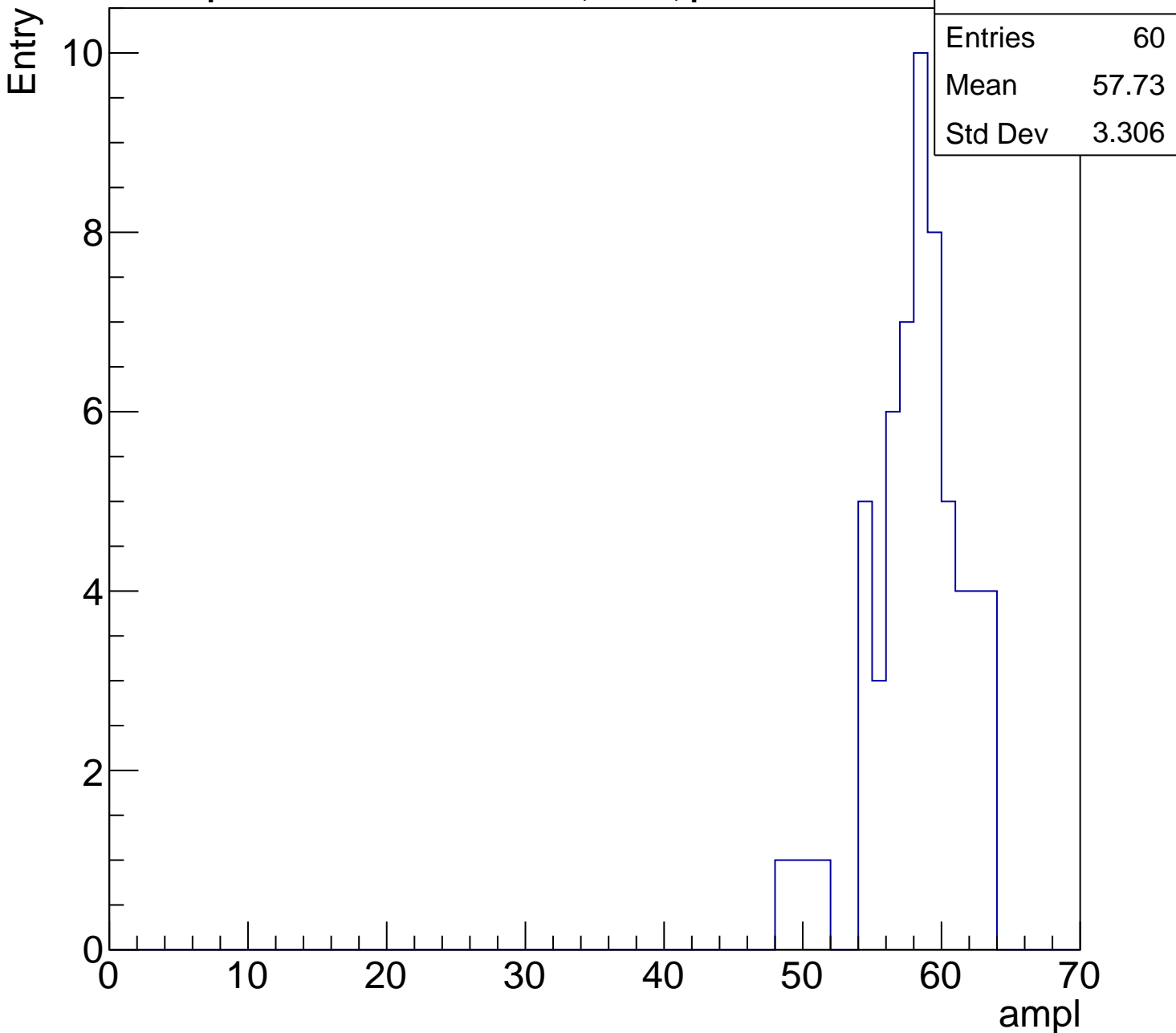
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

10  
8  
6  
4  
2  
0

Entries	60
Mean	57.73
Std Dev	3.306

ampl

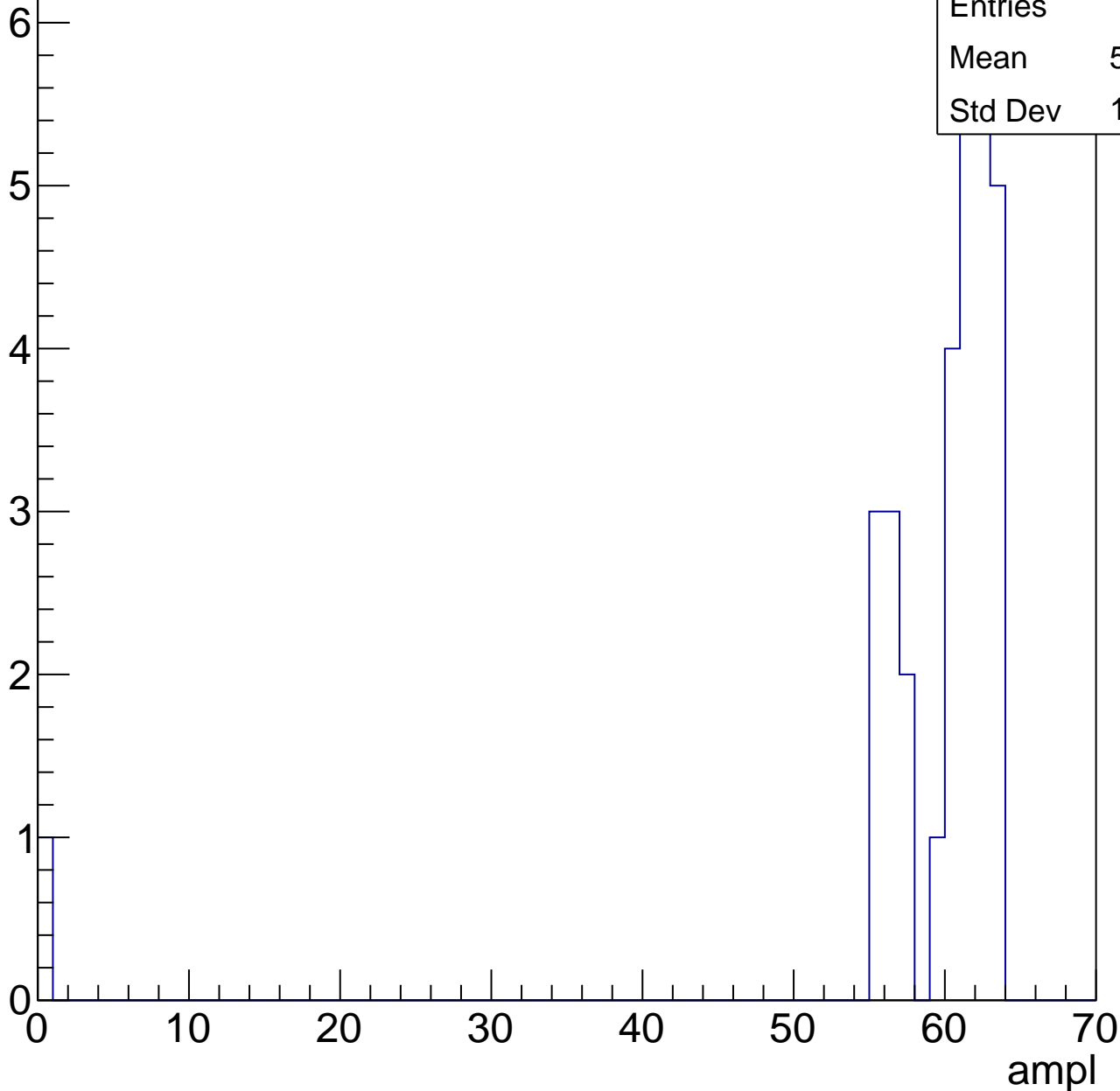


# B1L103S, U1-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	31
Mean	58.03
Std Dev	10.92





# B1L103S, U1-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L103S, U1-ch77, adc0

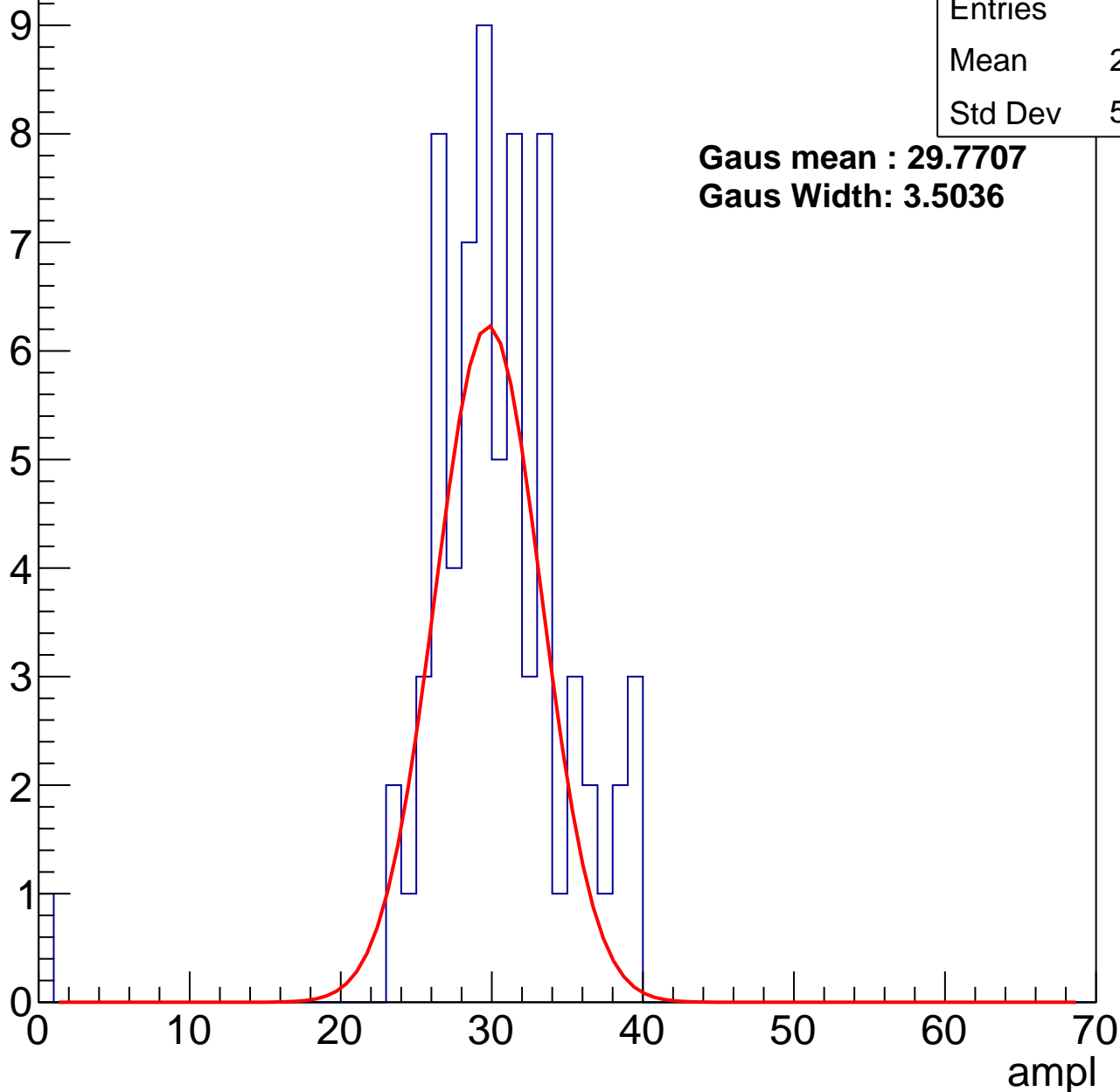
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	29.82
Std Dev	5.284

**Gaus mean : 29.7707**

**Gaus Width: 3.5036**



# B1L103S, U1-ch77, adc1

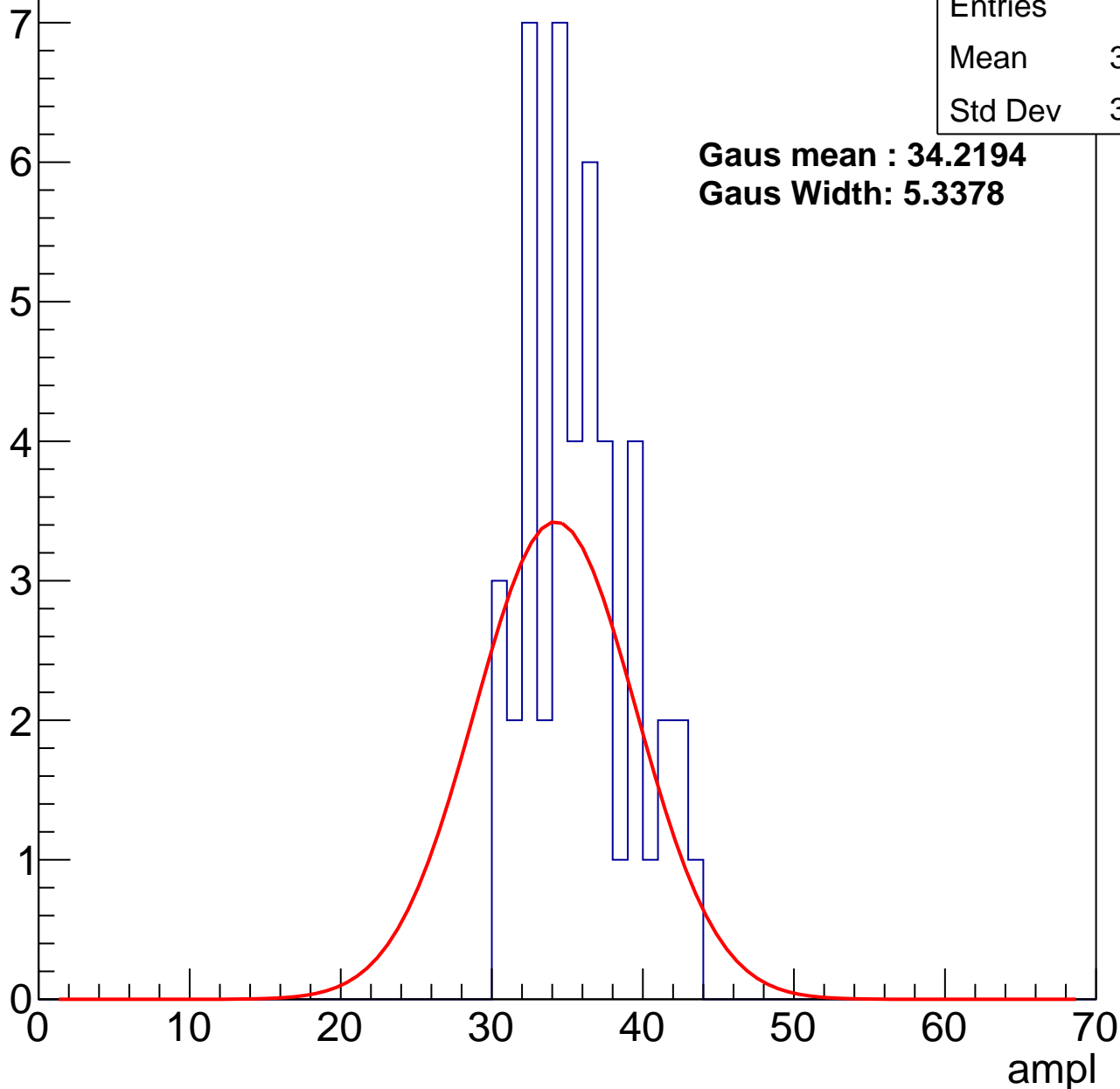
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	35.37
Std Dev	3.403

**Gaus mean : 34.2194**

**Gaus Width: 5.3378**



# B1L103S, U1-ch77, adc2

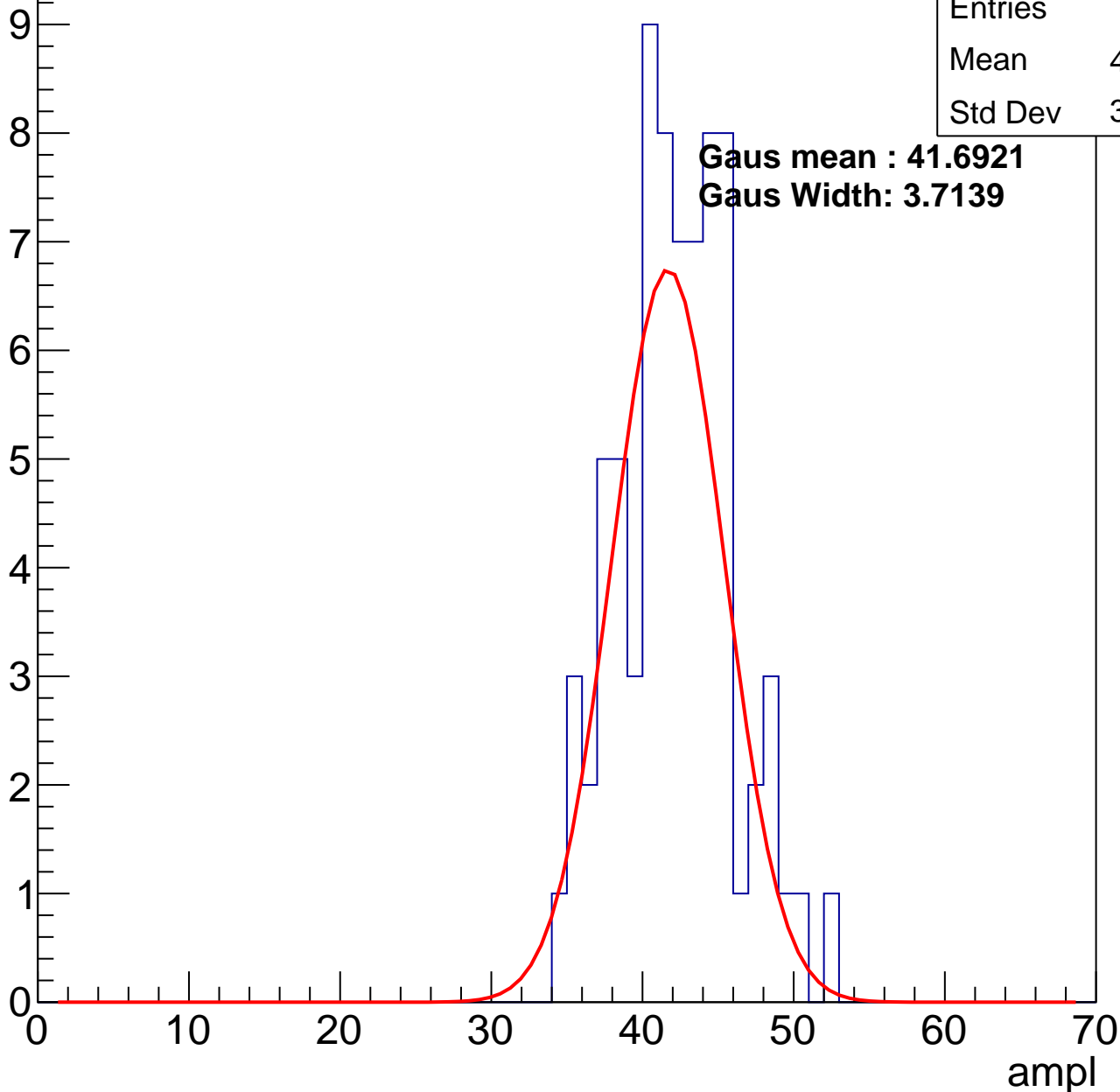
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	41.77
Std Dev	3.747

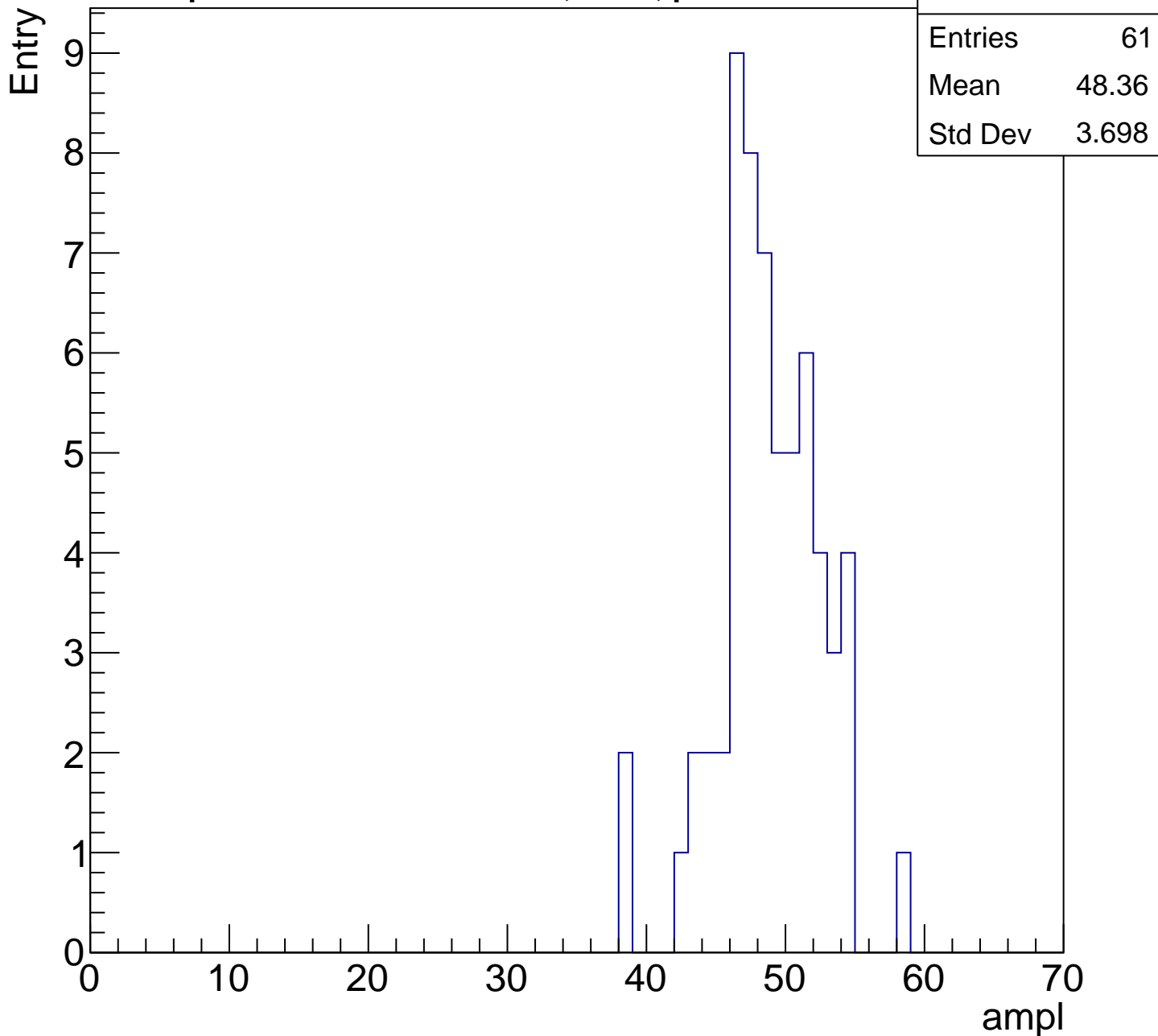
**Gaus mean : 41.6921**

**Gaus Width: 3.7139**



# B1L103S, U1-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

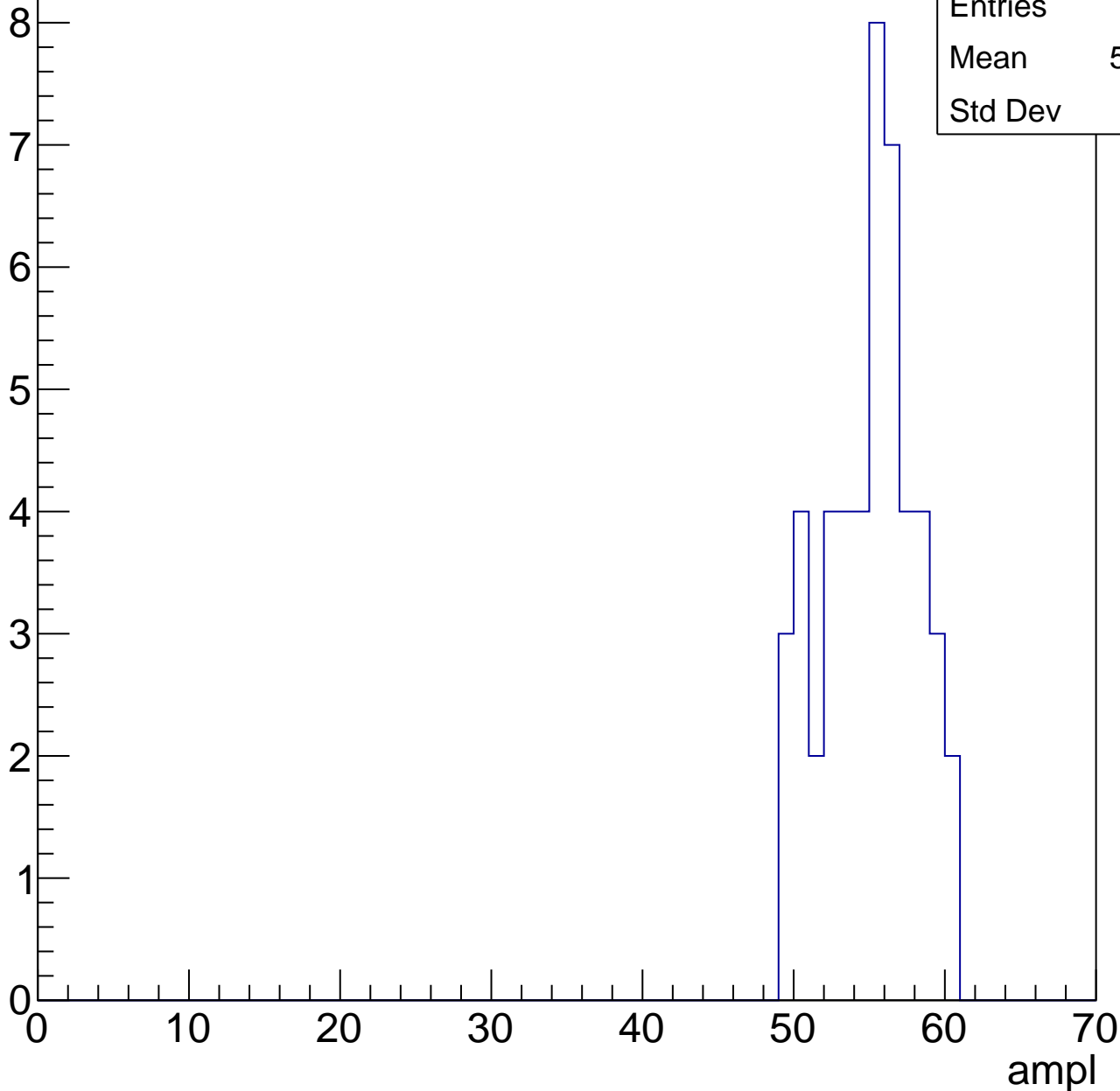


# B1L103S, U1-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

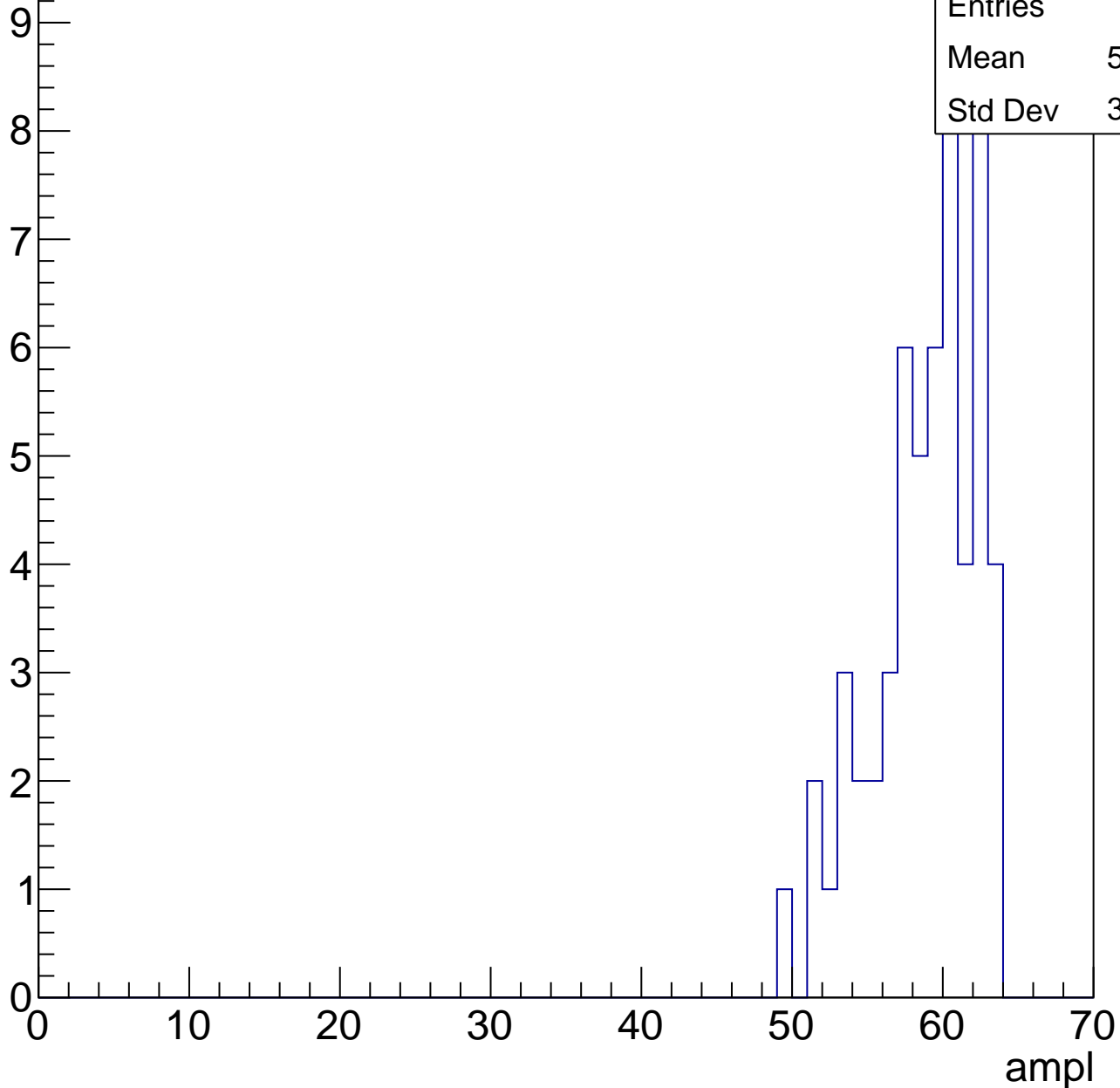
Entries	49
Mean	54.57
Std Dev	3.01



# B1L103S, U1-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

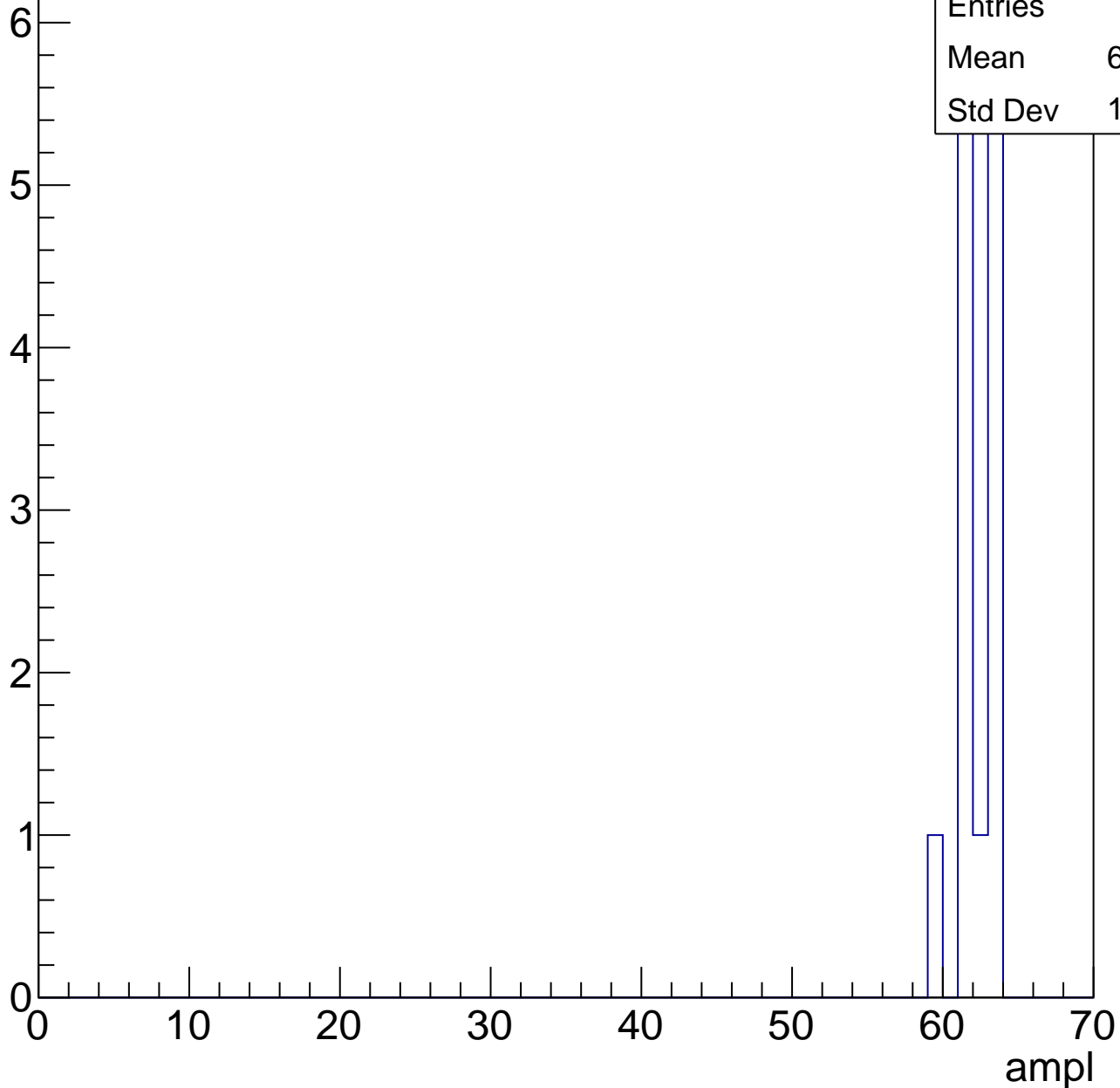
Entry



# B1L103S, U1-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U1-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch78, adc0

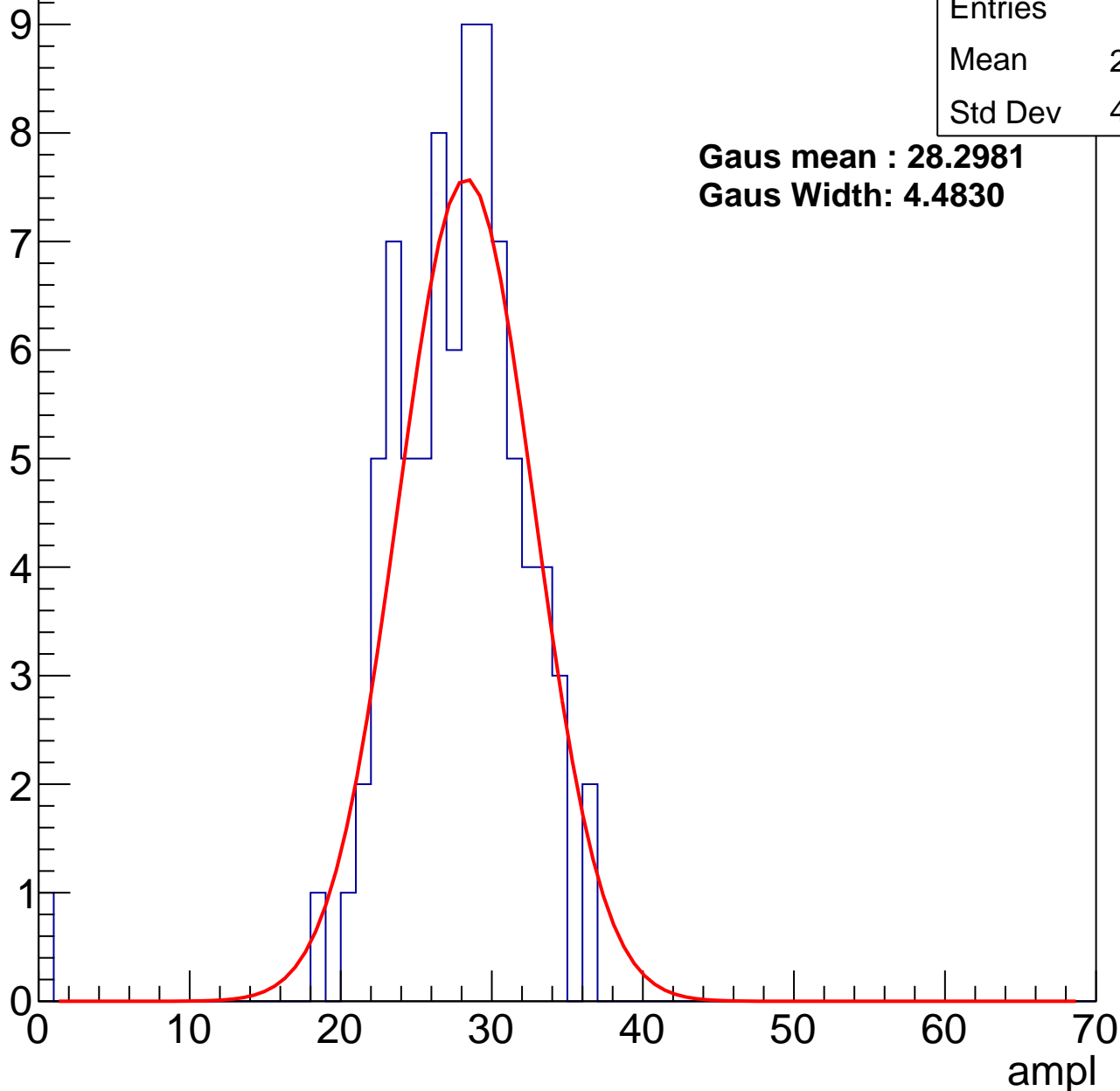
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	84
Mean	27.12
Std Dev	4.856

**Gaus mean : 28.2981**

**Gaus Width: 4.4830**



# B1L103S, U1-ch78, adc1

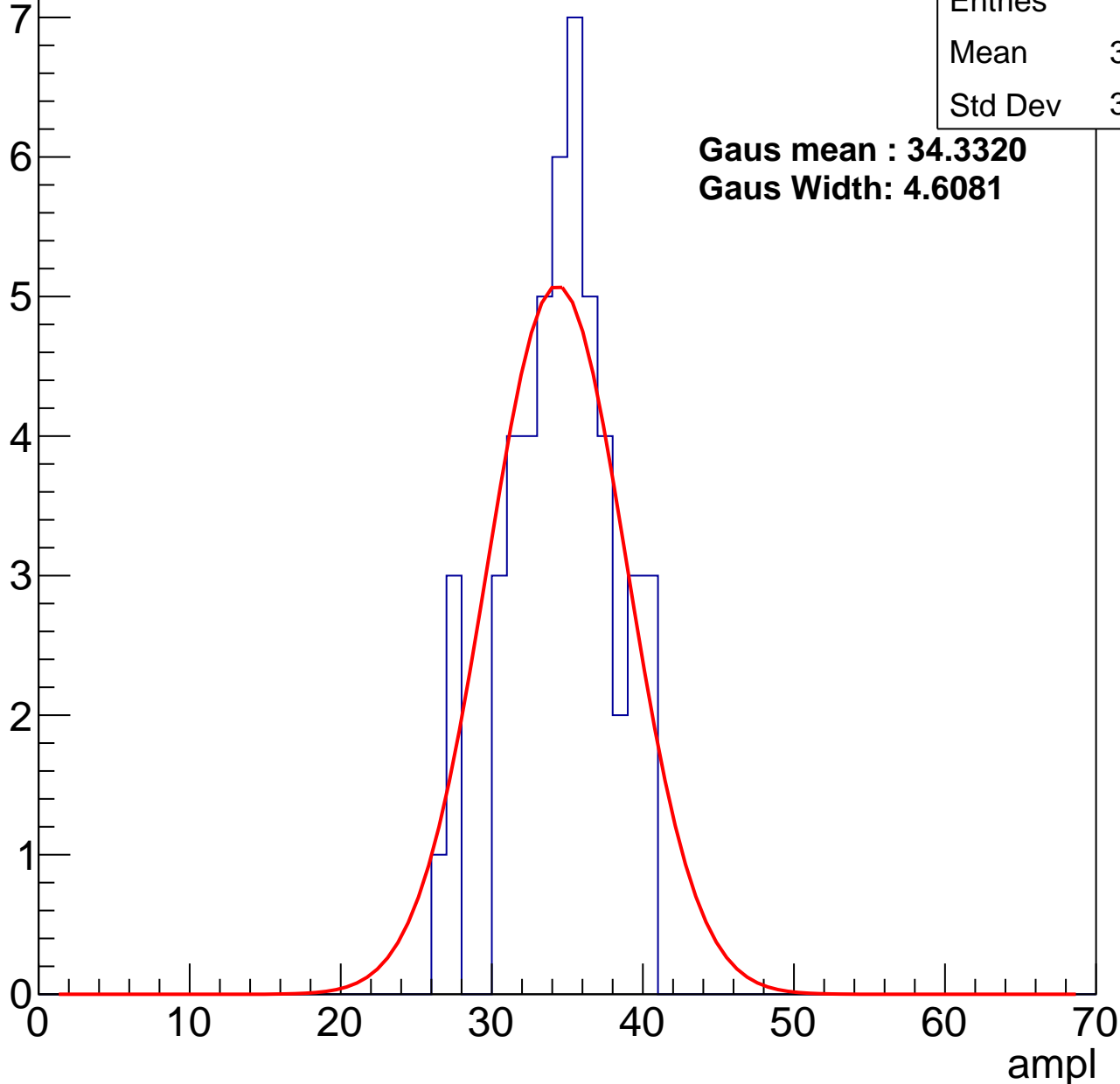
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	34.08
Std Dev	3.446

**Gaus mean : 34.3320**

**Gaus Width: 4.6081**



# B1L103S, U1-ch78, adc2

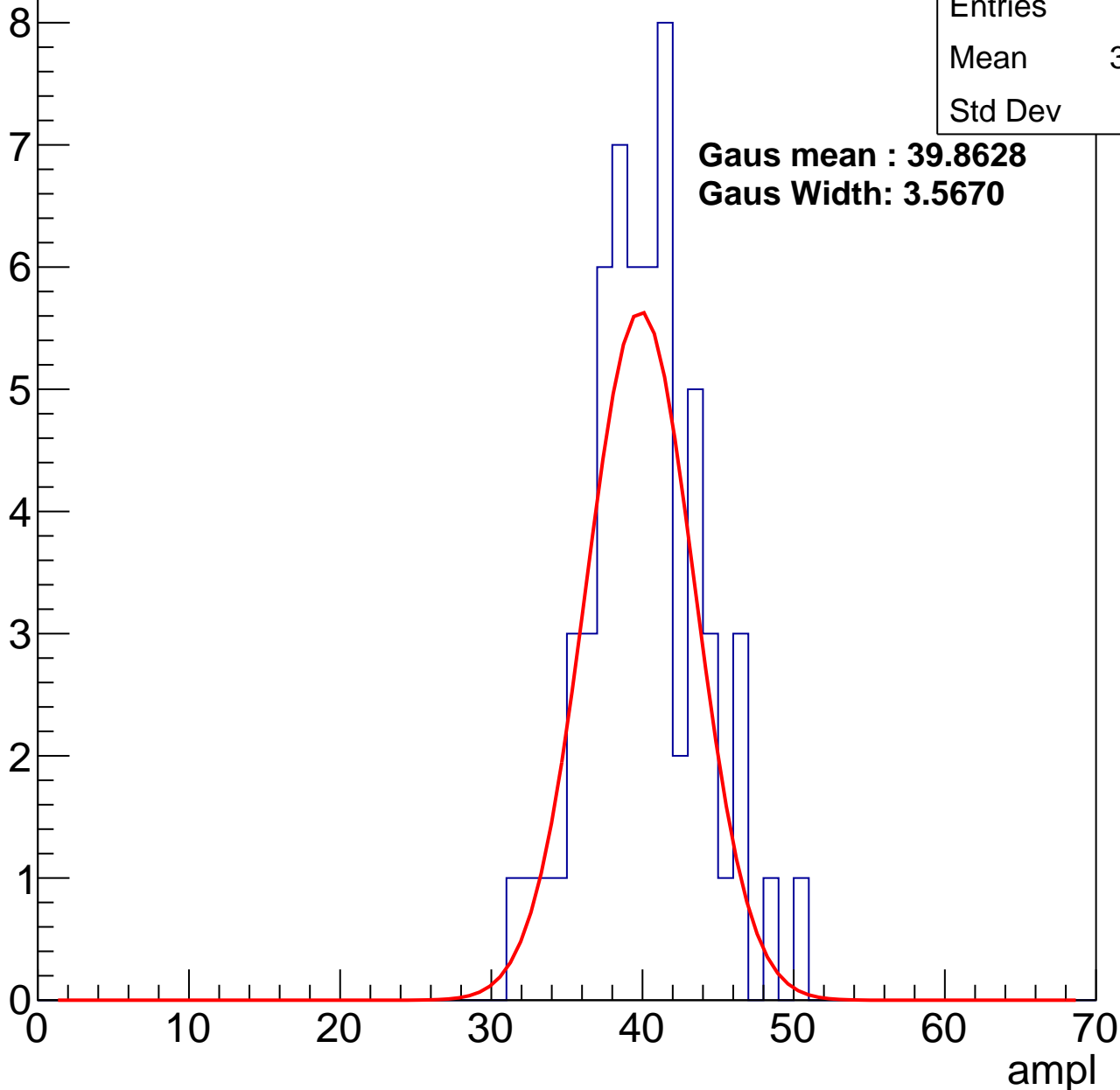
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	39.75
Std Dev	3.78

**Gaus mean : 39.8628**

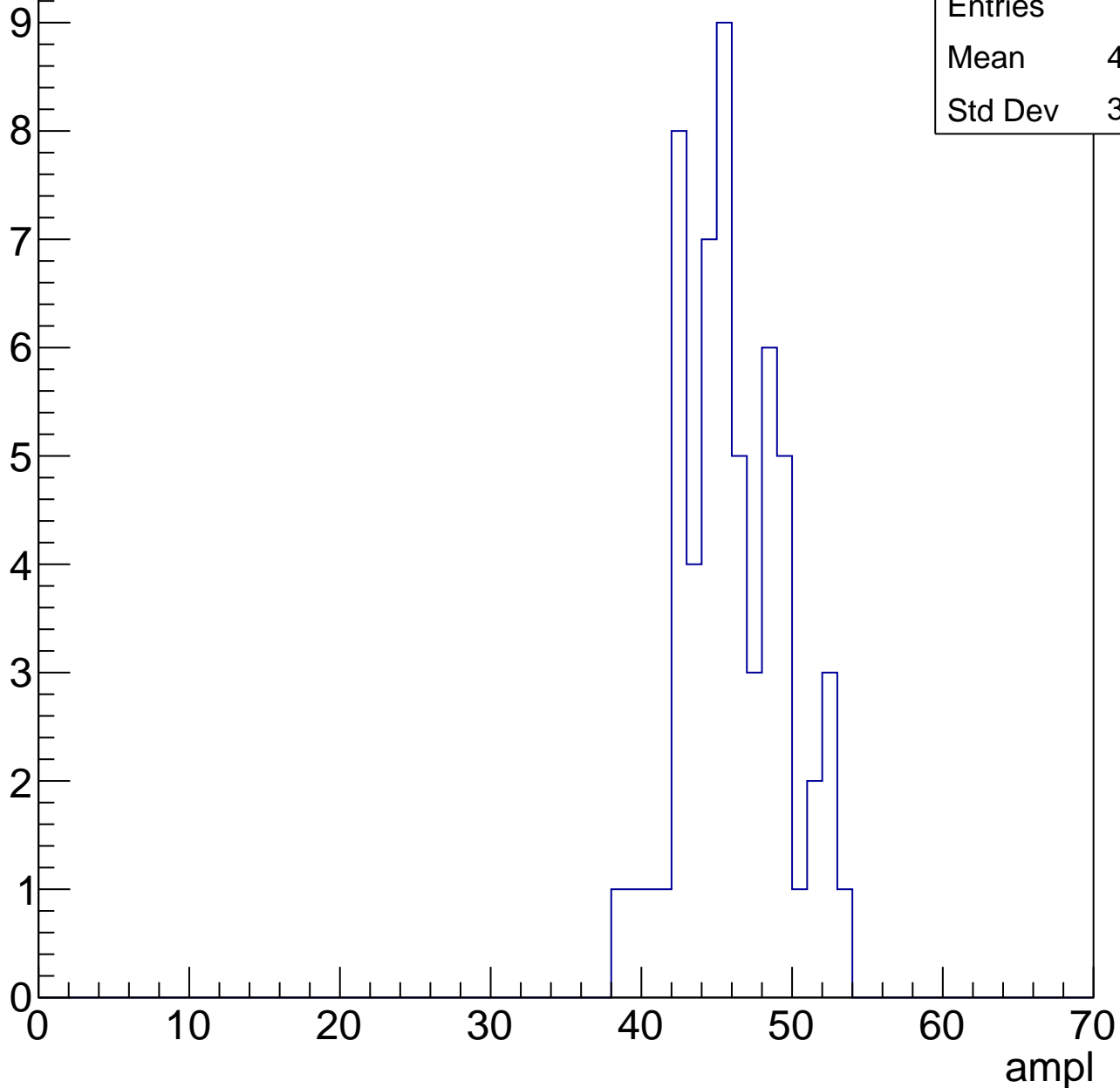
**Gaus Width: 3.5670**



# B1L103S, U1-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

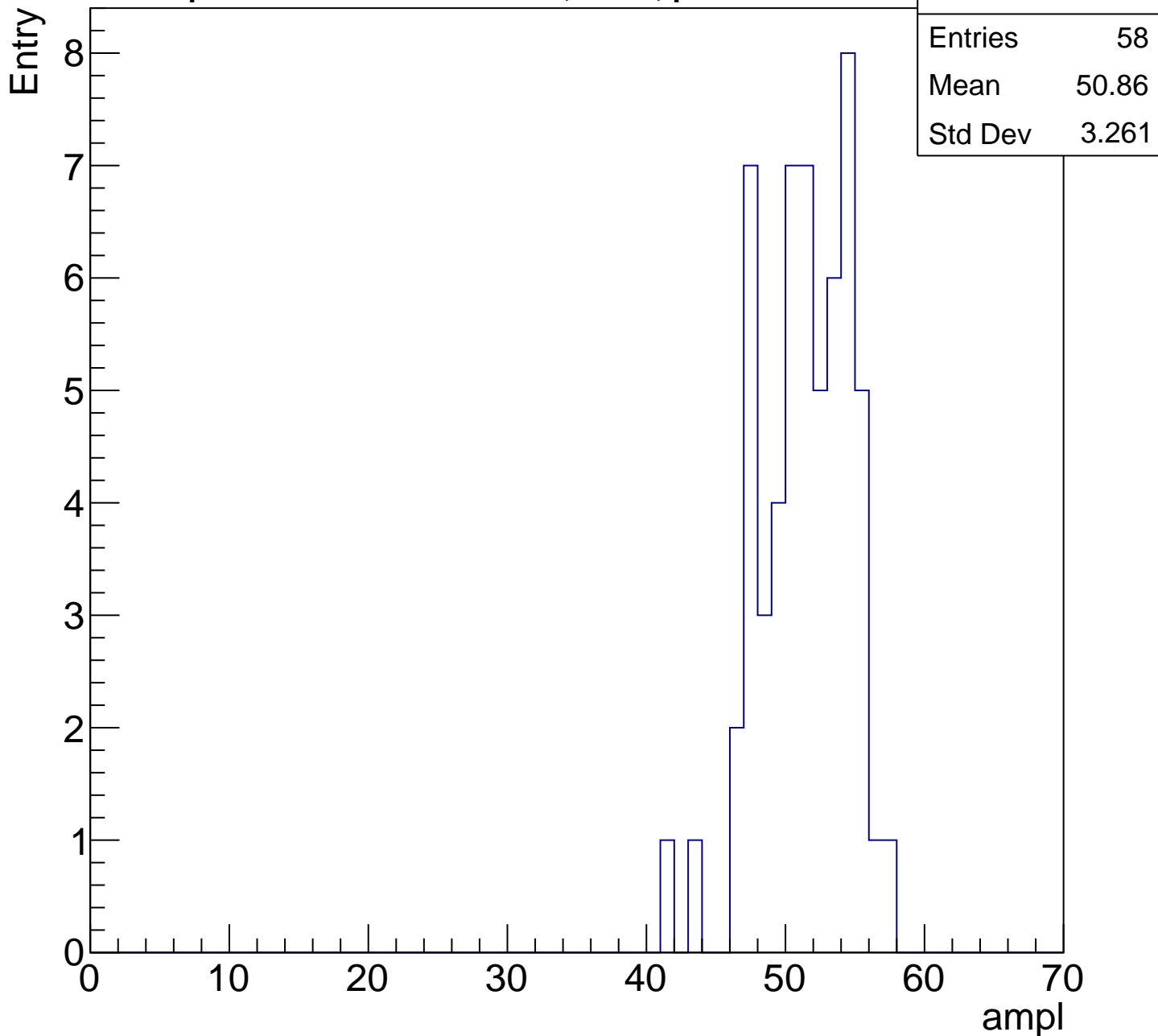
Entry



Entries	58
Mean	45.59
Std Dev	3.373

# B1L103S, U1-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

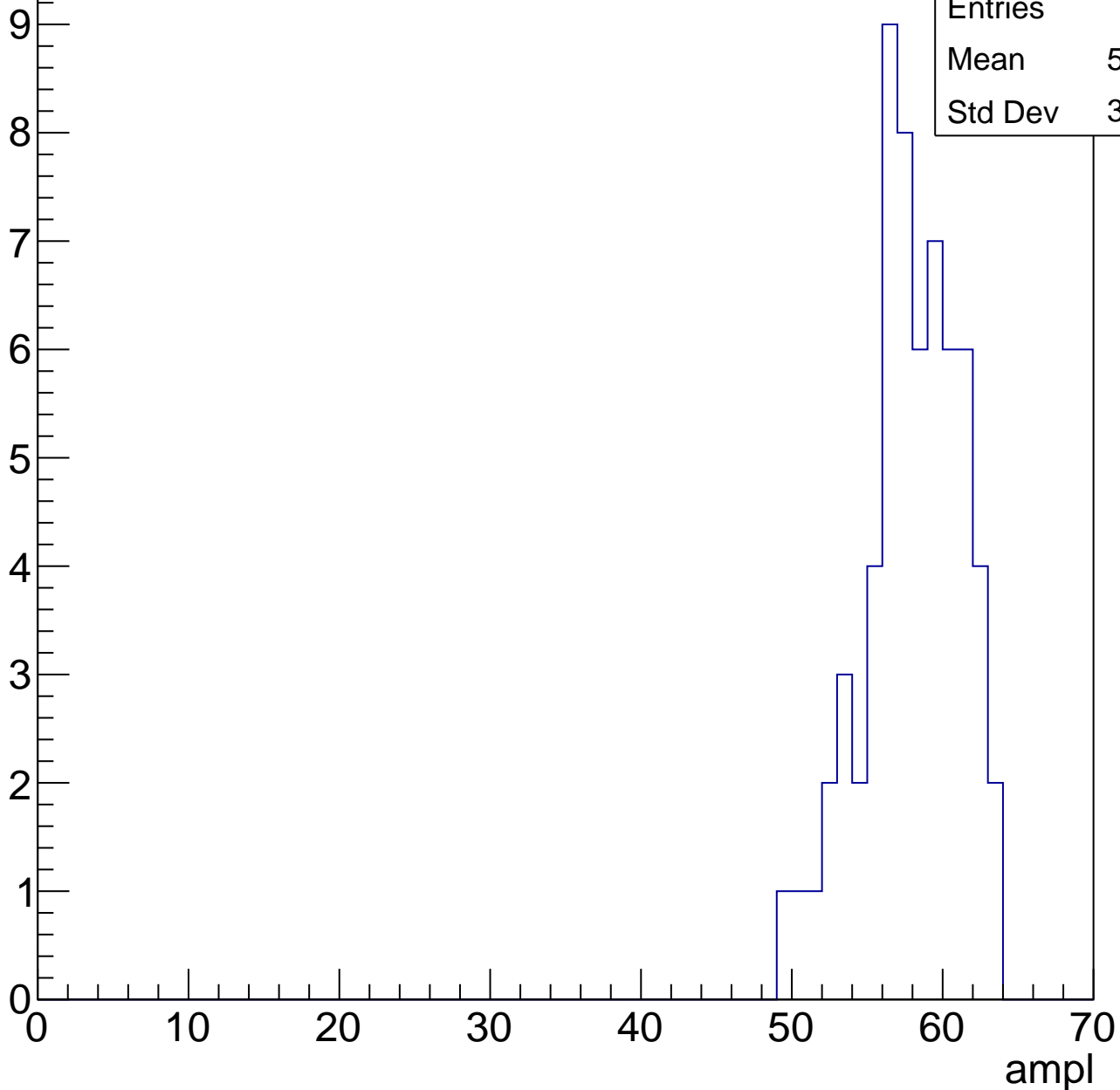


# B1L103S, U1-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	57.45
Std Dev	3.196

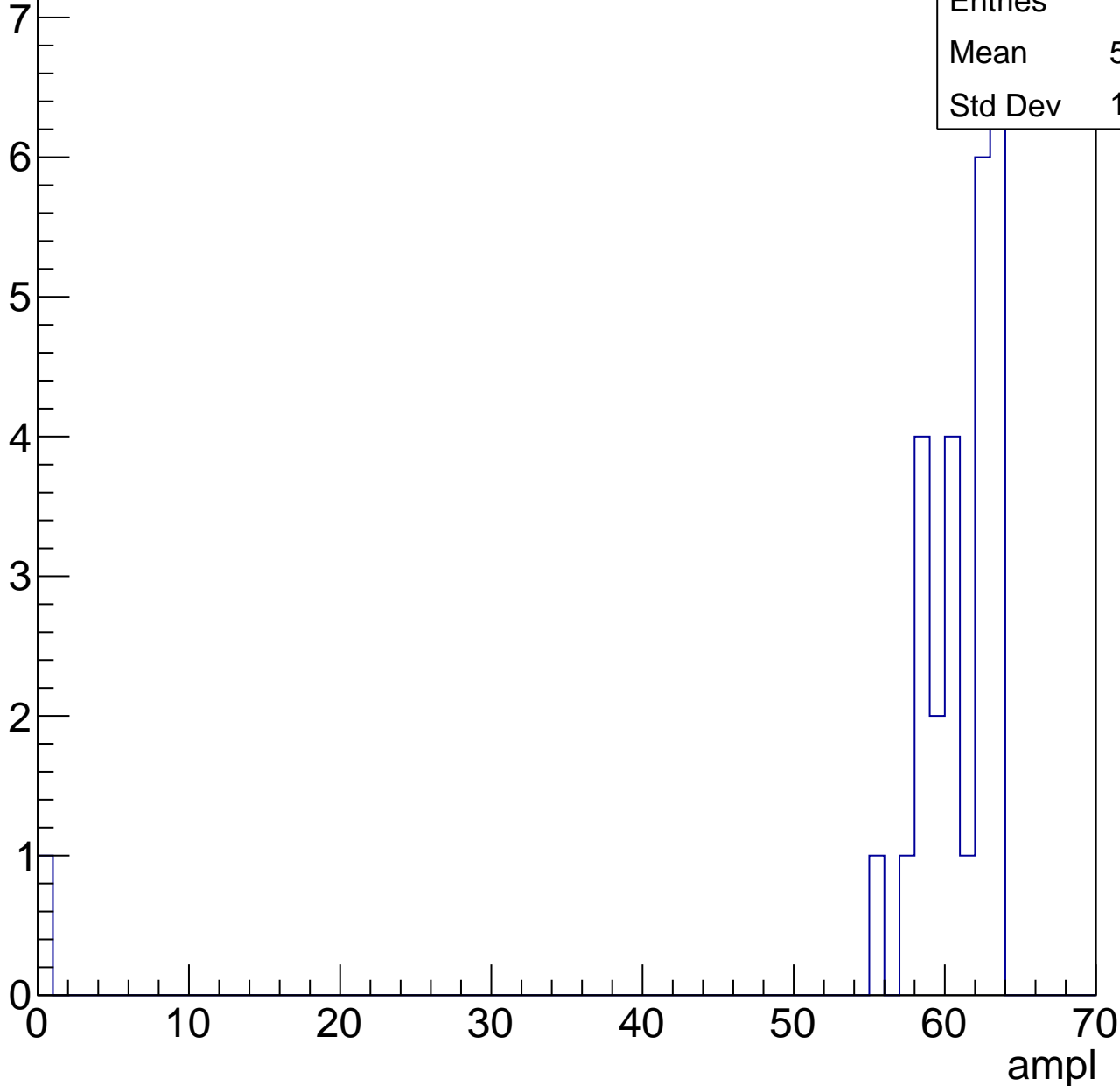


# B1L103S, U1-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	27
Mean	58.37
Std Dev	11.66

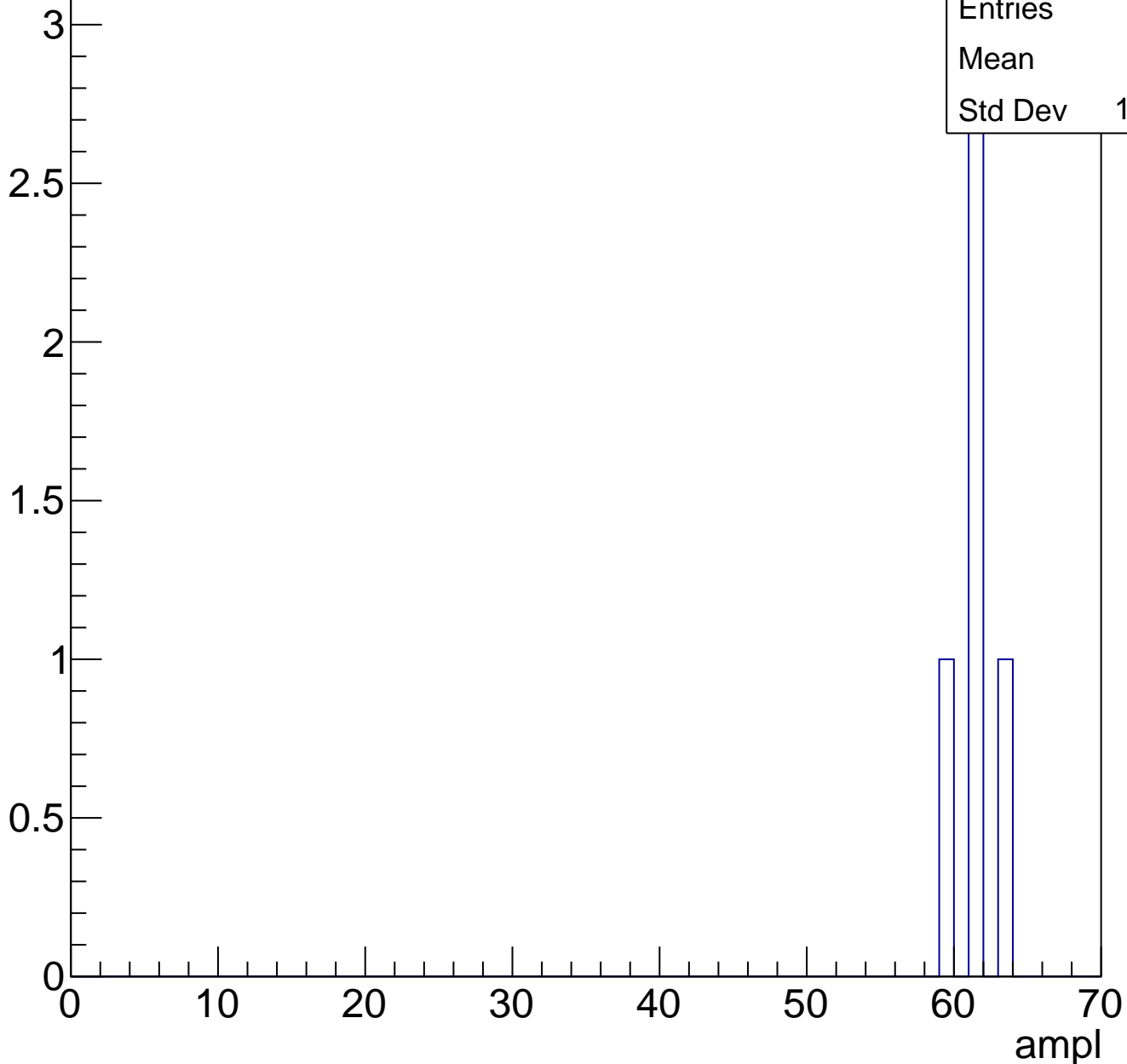




# B1L103S, U1-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch79, adc0

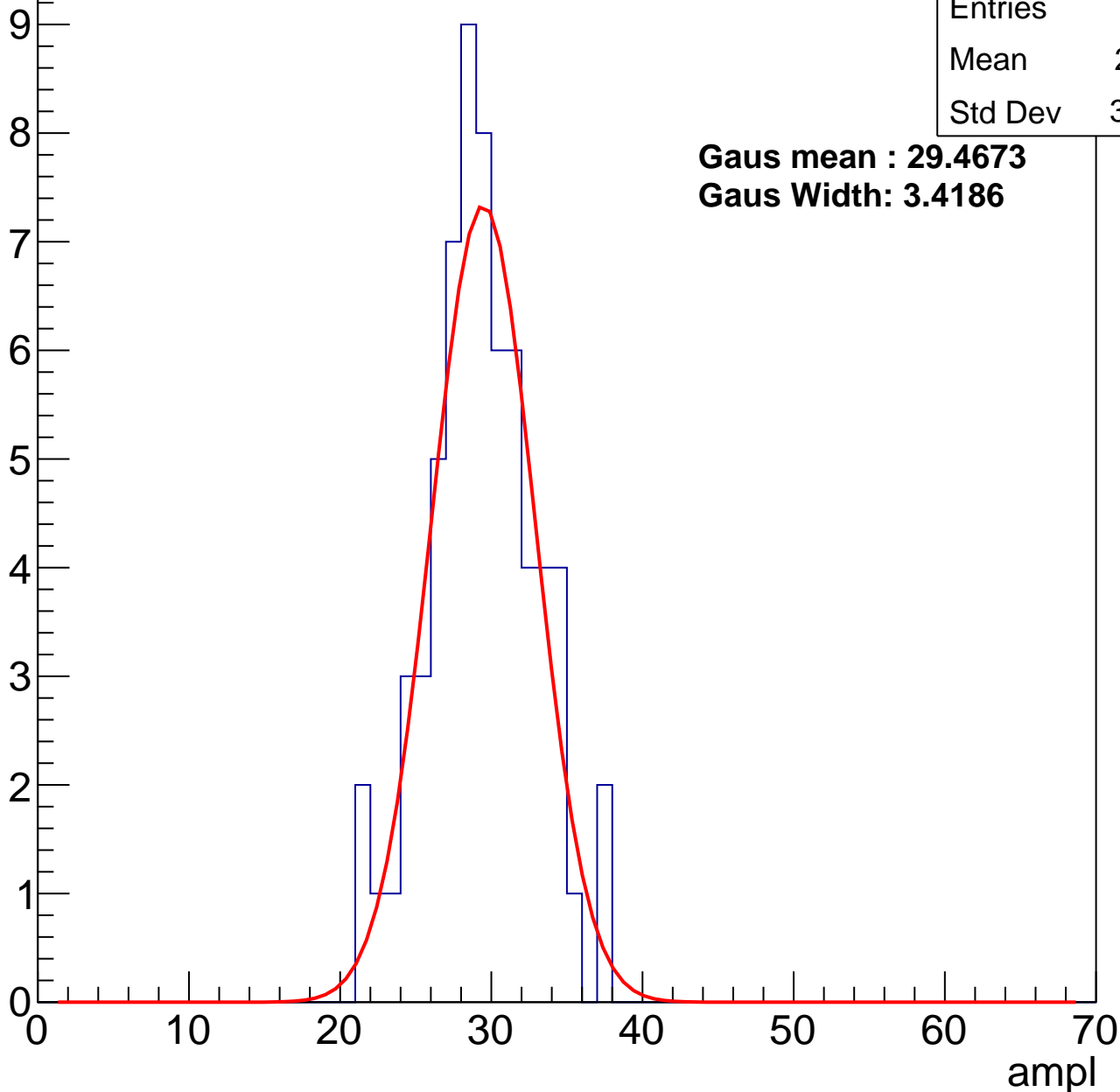
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	28.91
Std Dev	3.506

**Gaus mean : 29.4673**

**Gaus Width: 3.4186**



# B1L103S, U1-ch79, adc1

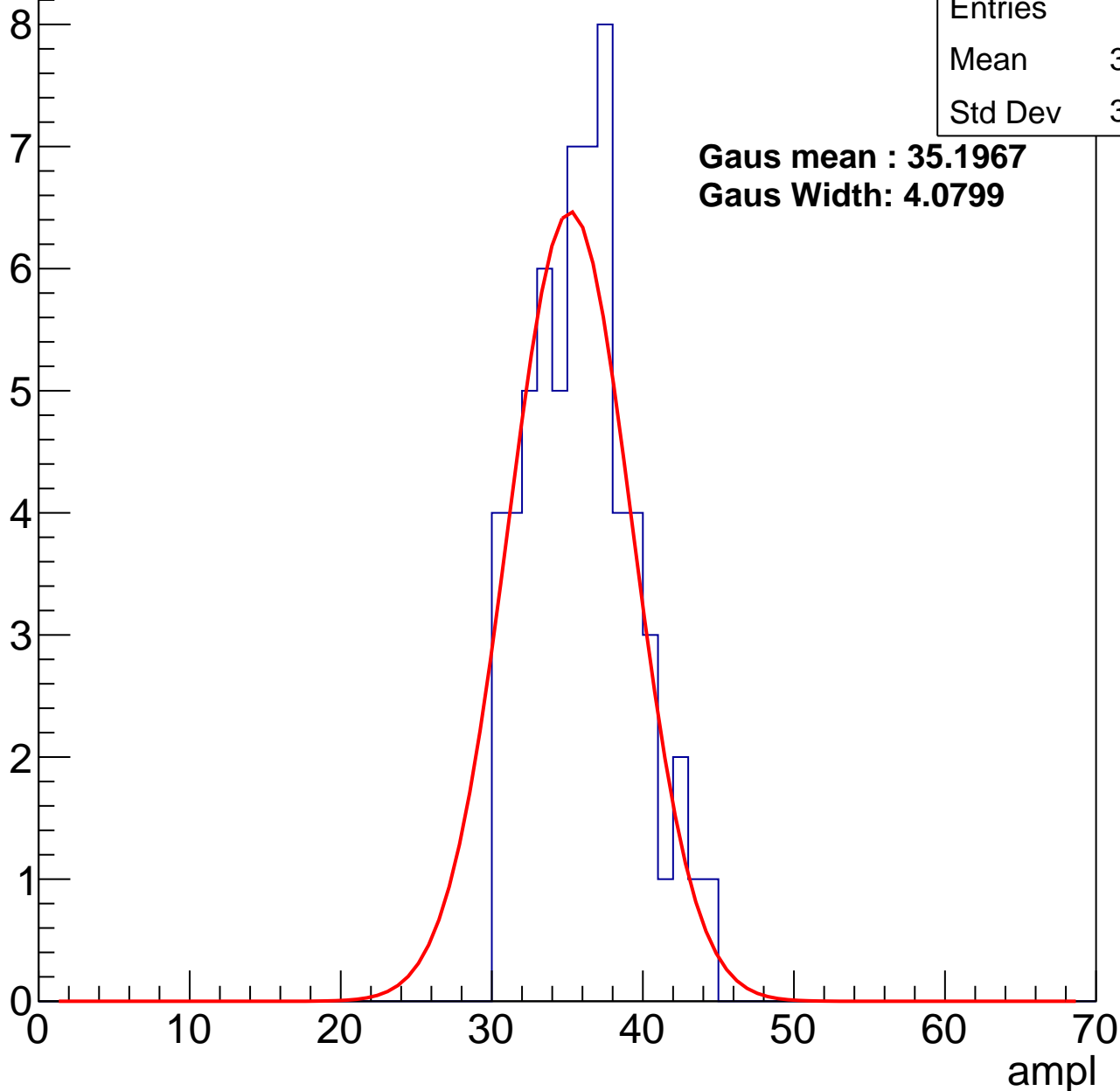
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	35.56
Std Dev	3.387

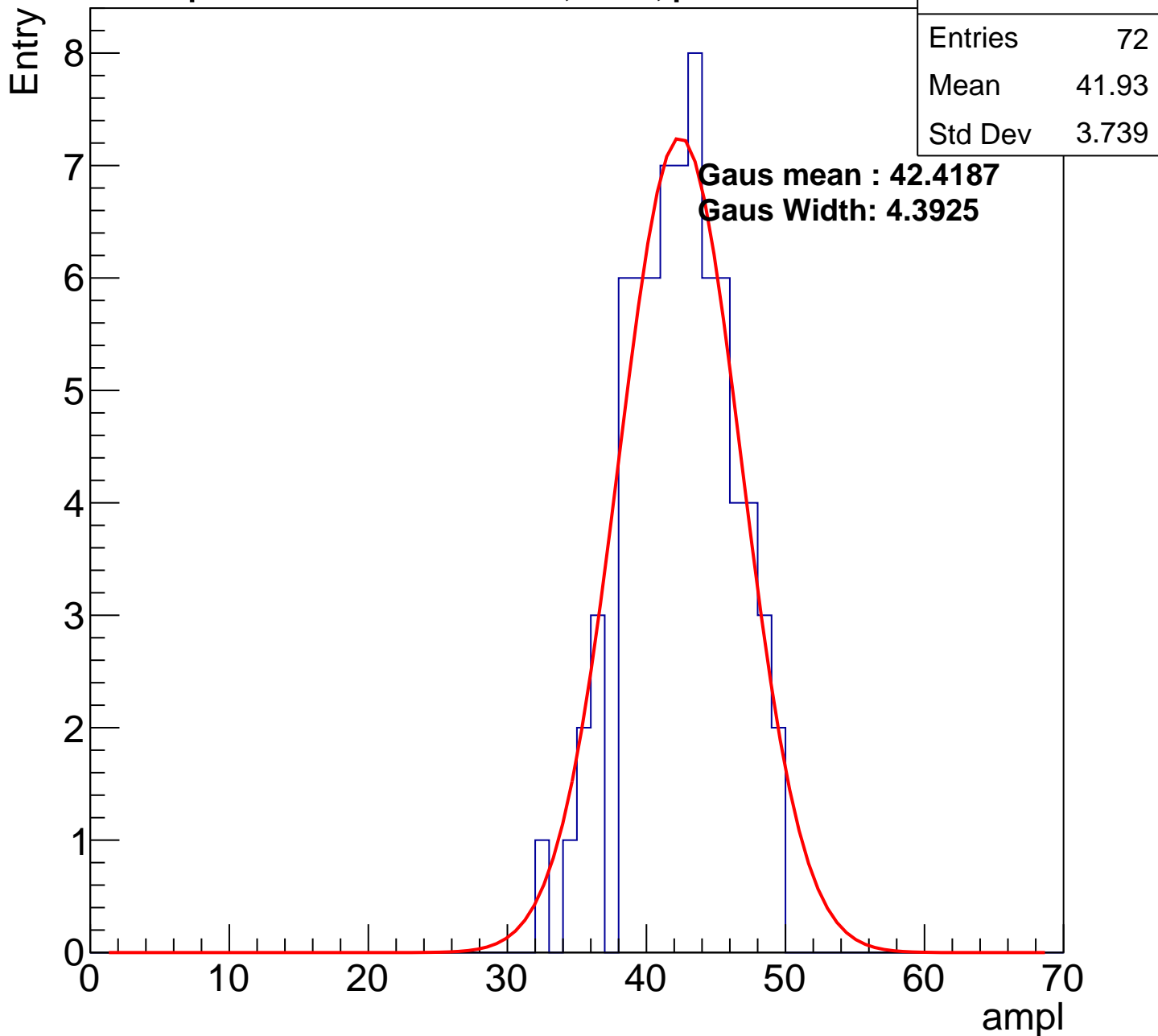
**Gaus mean : 35.1967**

**Gaus Width: 4.0799**



# B1L103S, U1-ch79, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

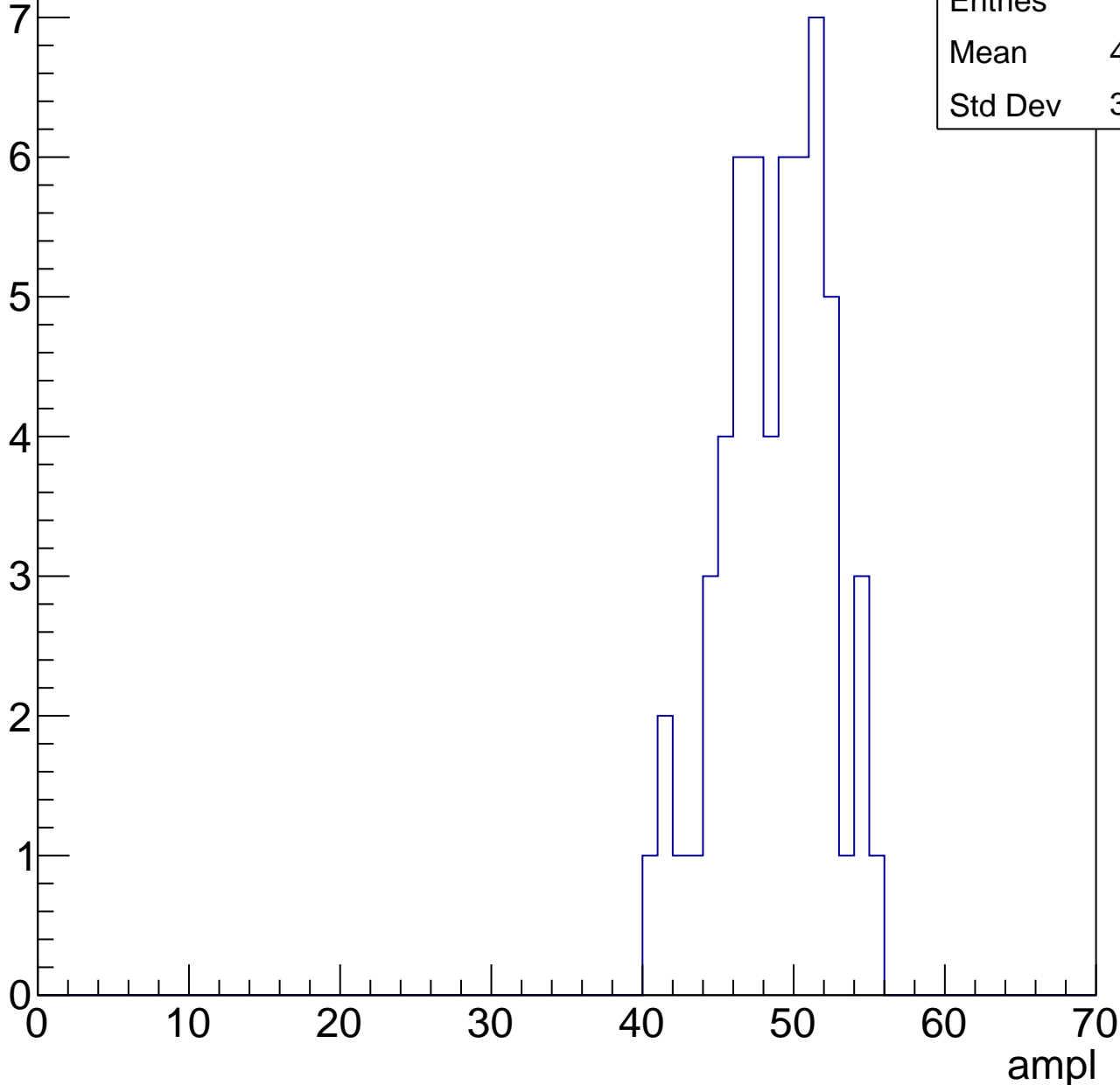


# B1L103S, U1-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

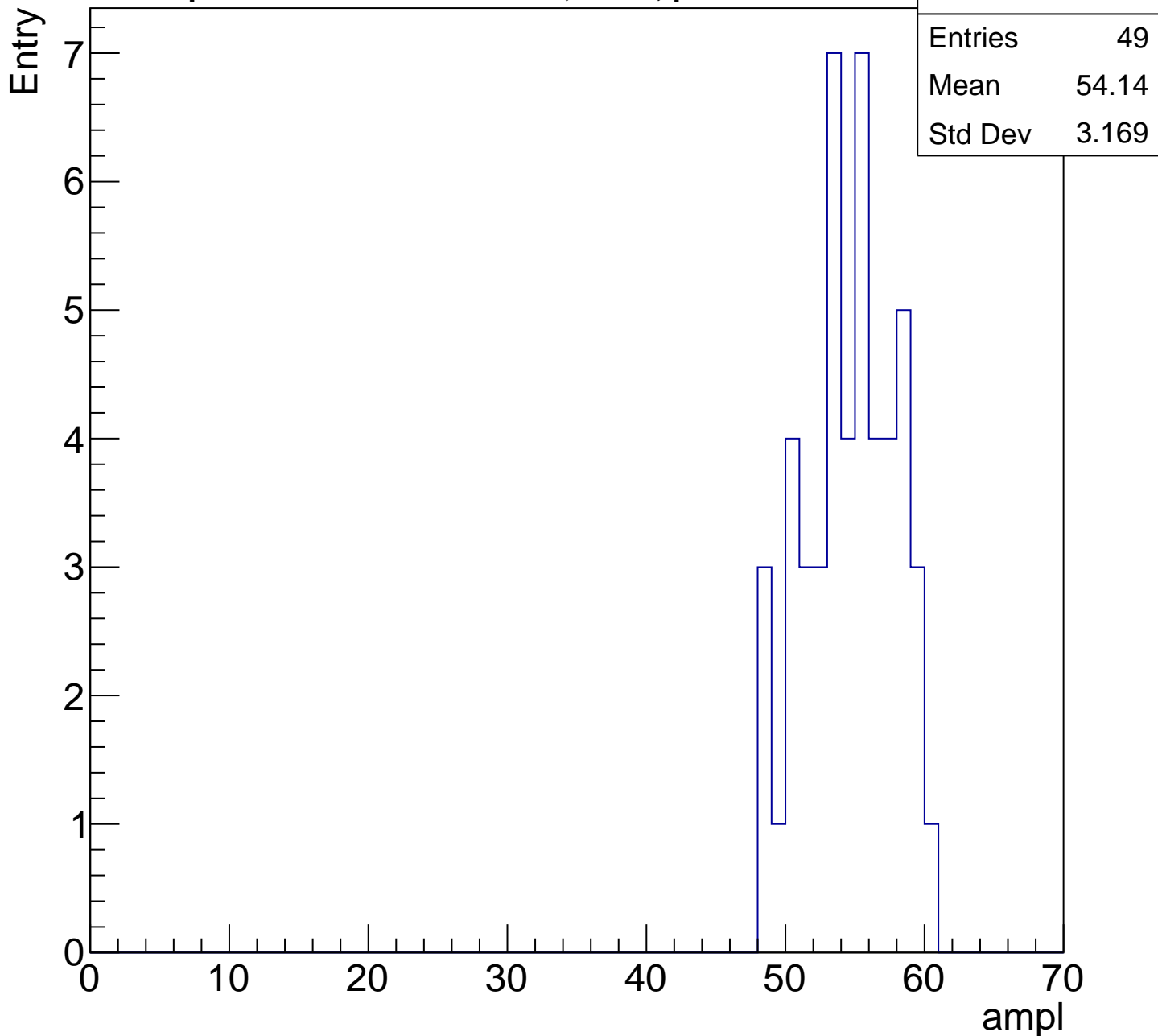
Entry

Entries	57
Mean	48.25
Std Dev	3.476



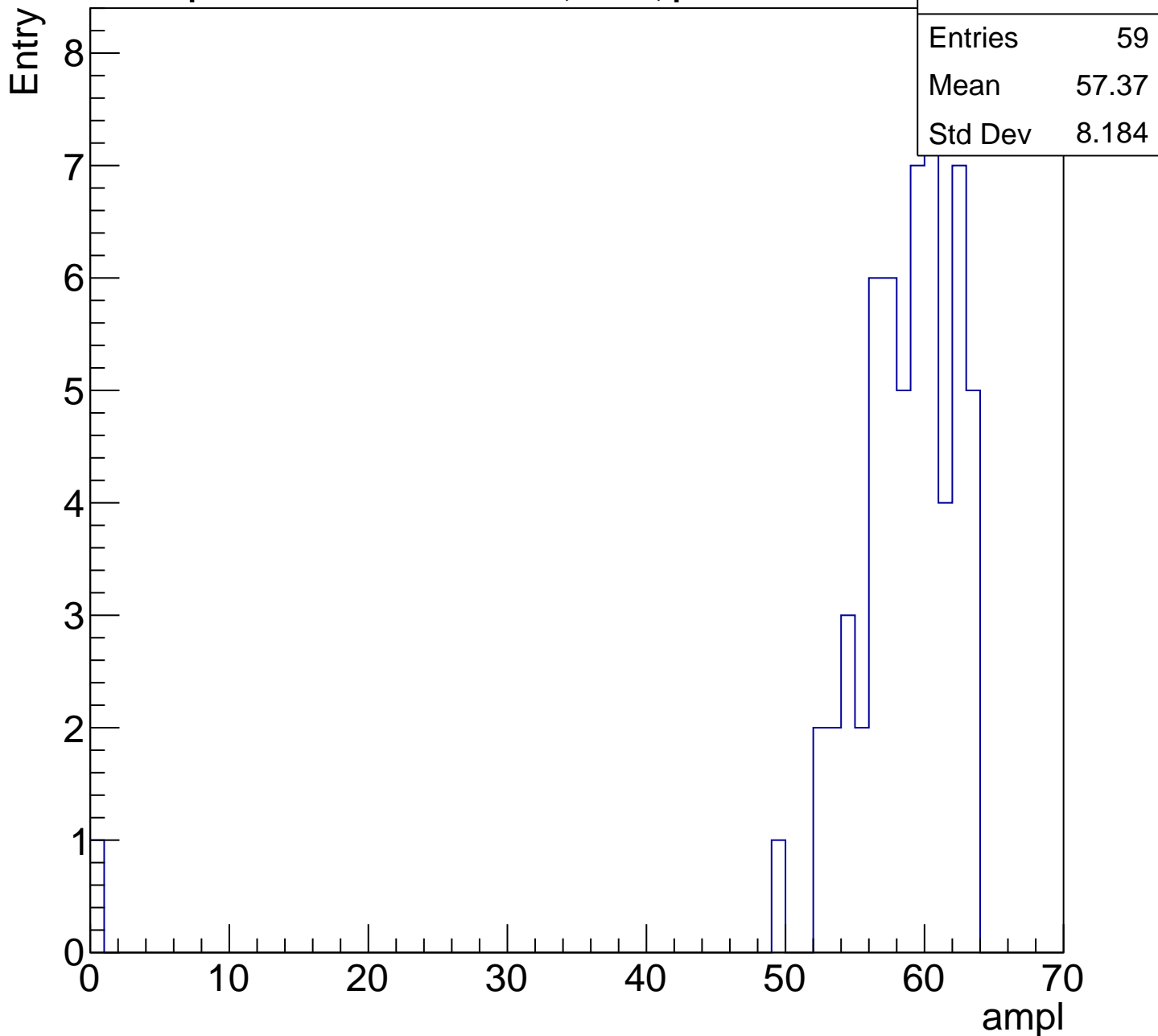
# B1L103S, U1-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U1-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

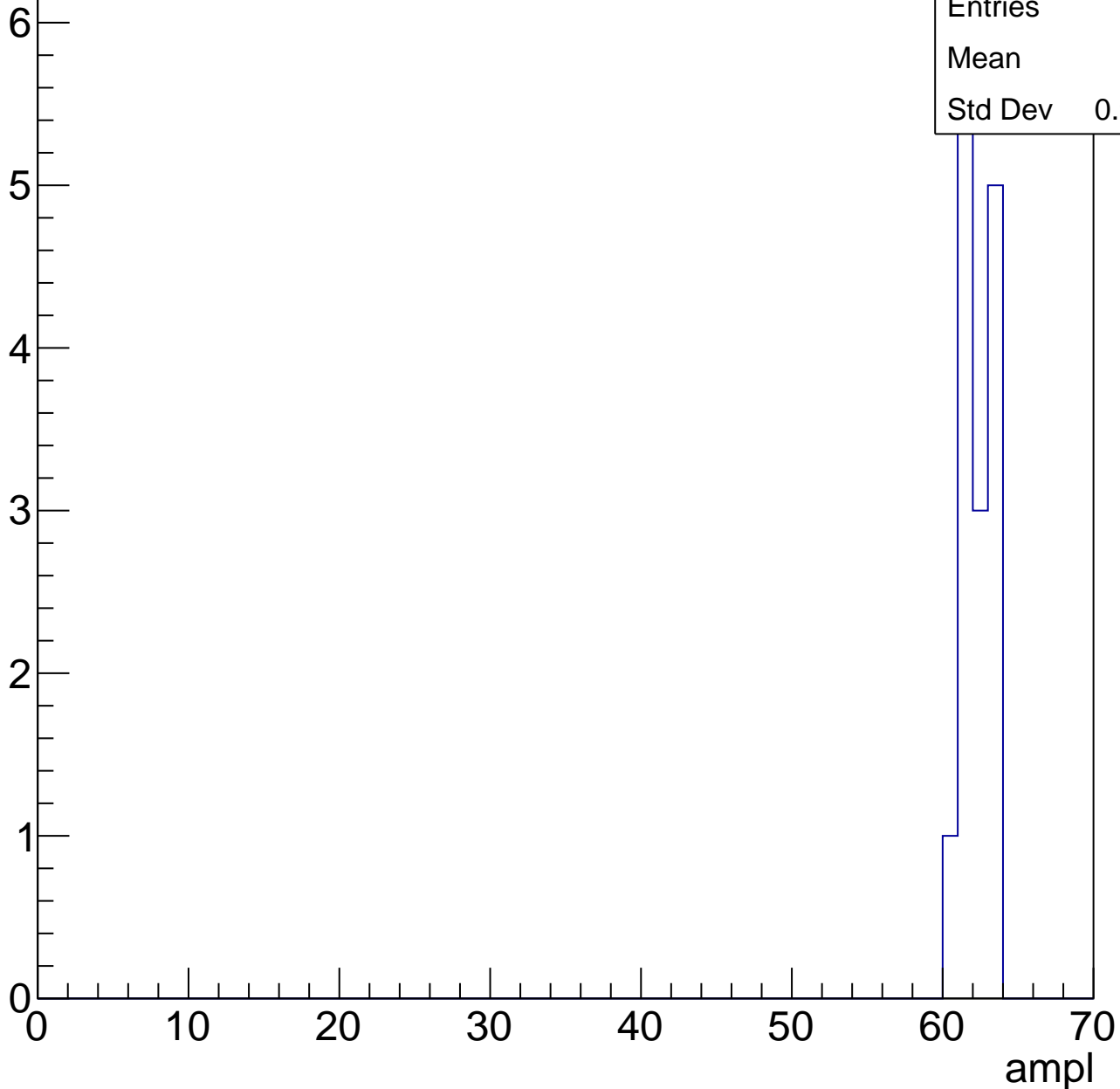


# B1L103S, U1-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	15
Mean	61.8
Std Dev	0.9798





# B1L103S, U1-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	10.5
Std Dev	10.5

# B1L103S, U1-ch80, adc0

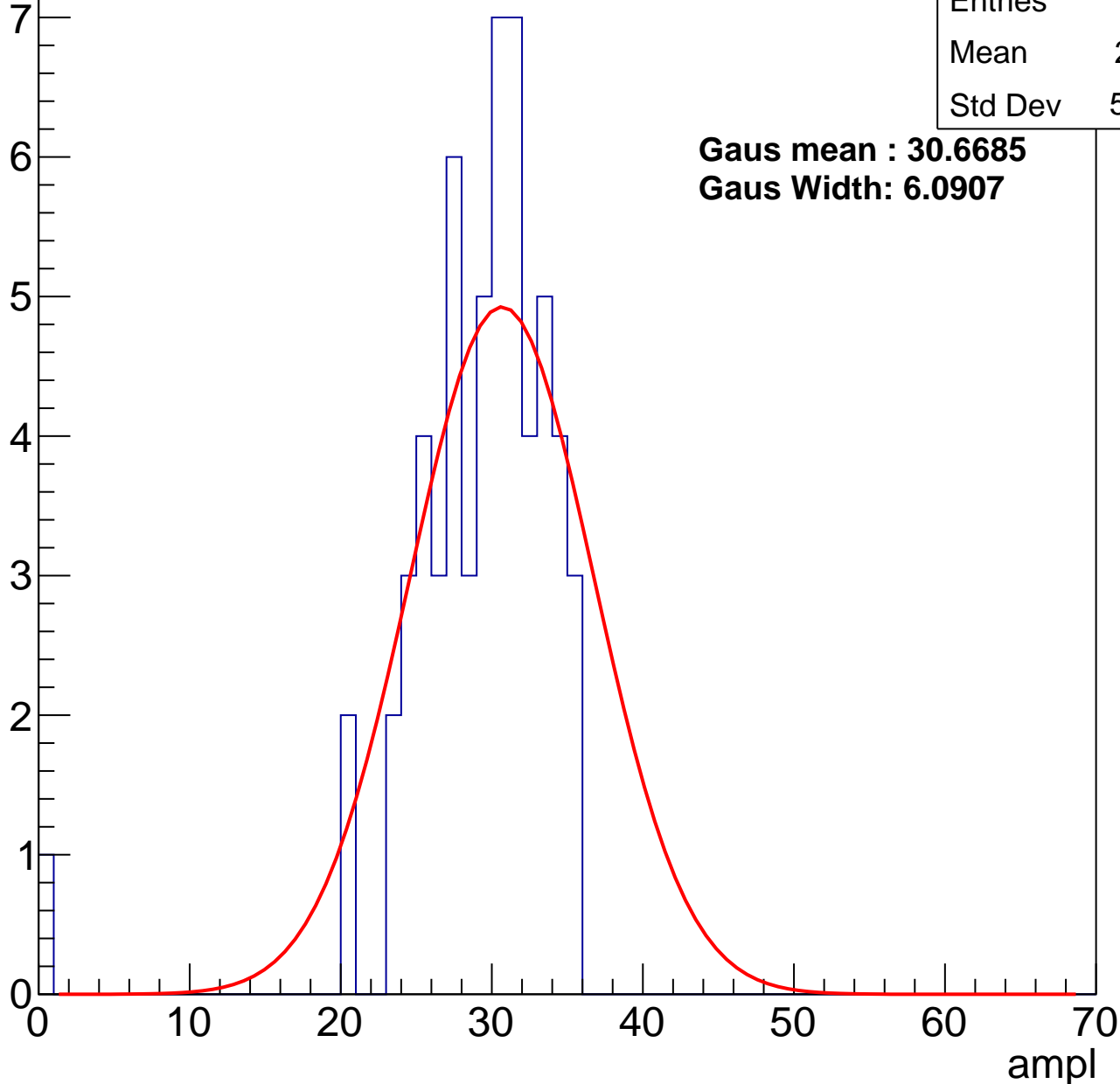
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	28.61
Std Dev	5.237

**Gaus mean : 30.6685**

**Gaus Width: 6.0907**



# B1L103S, U1-ch80, adc1

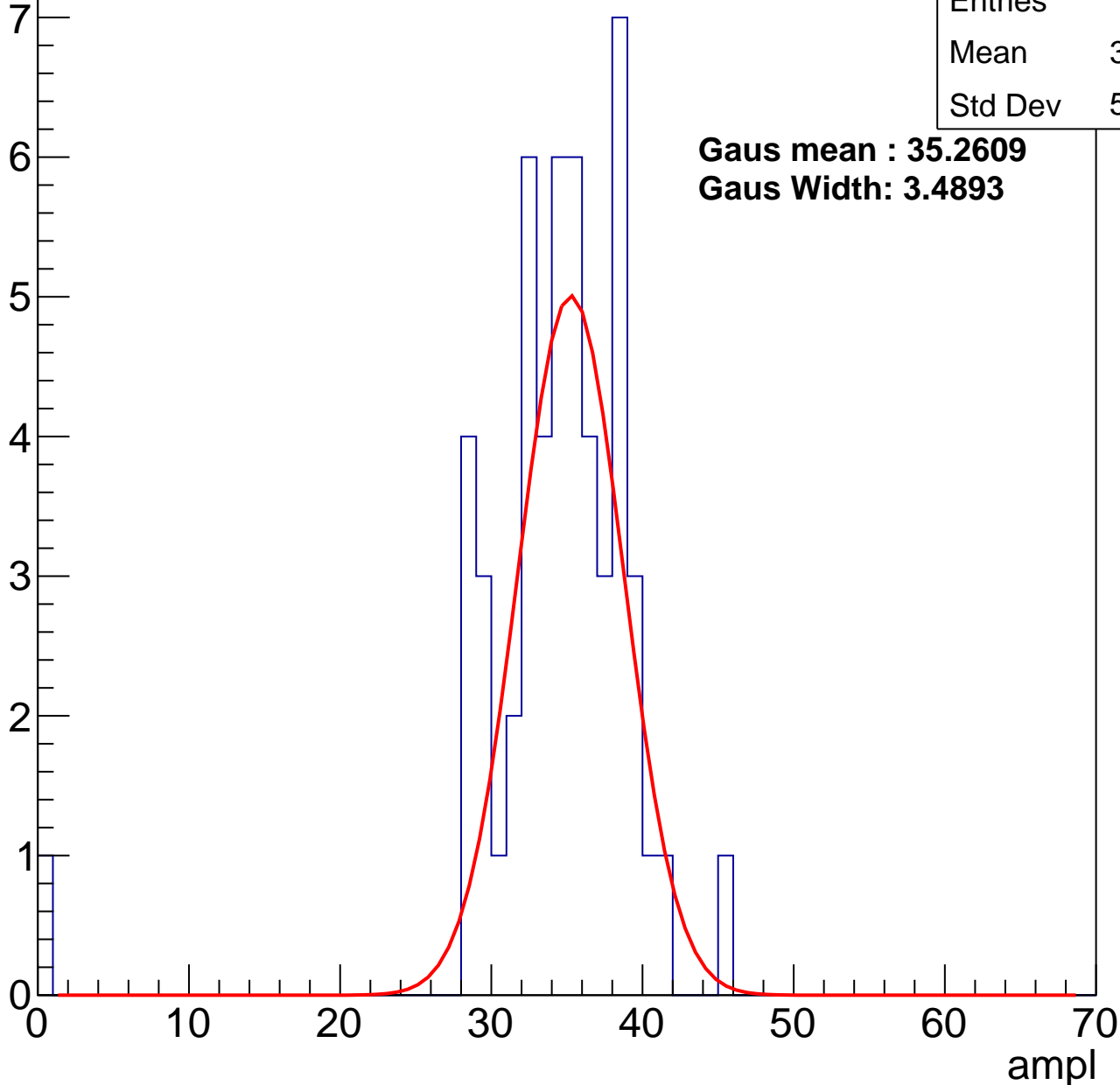
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	33.83
Std Dev	5.952

**Gaus mean : 35.2609**

**Gaus Width: 3.4893**



# B1L103S, U1-ch80, adc2

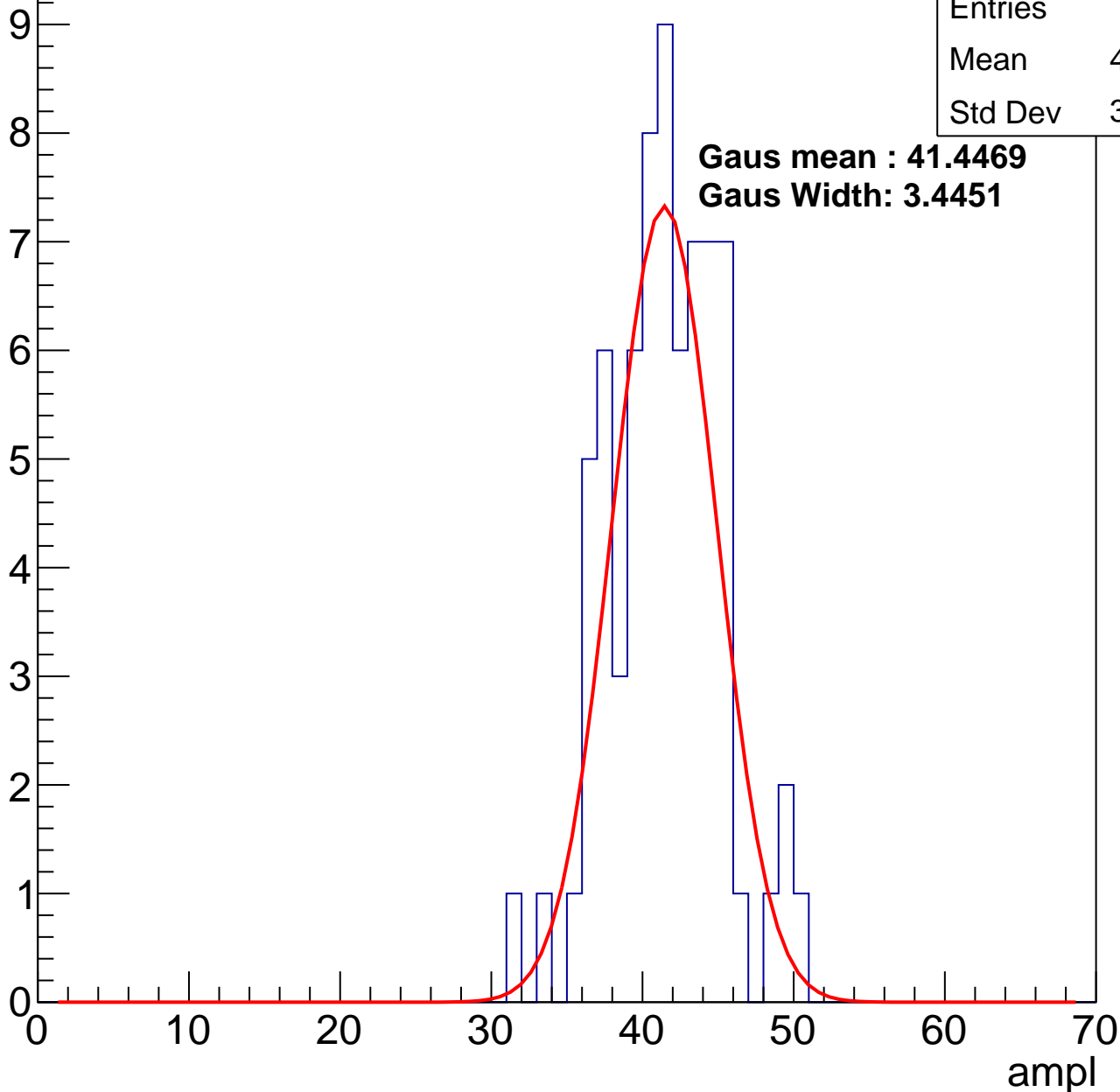
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	41.06
Std Dev	3.674

**Gaus mean : 41.4469**

**Gaus Width: 3.4451**

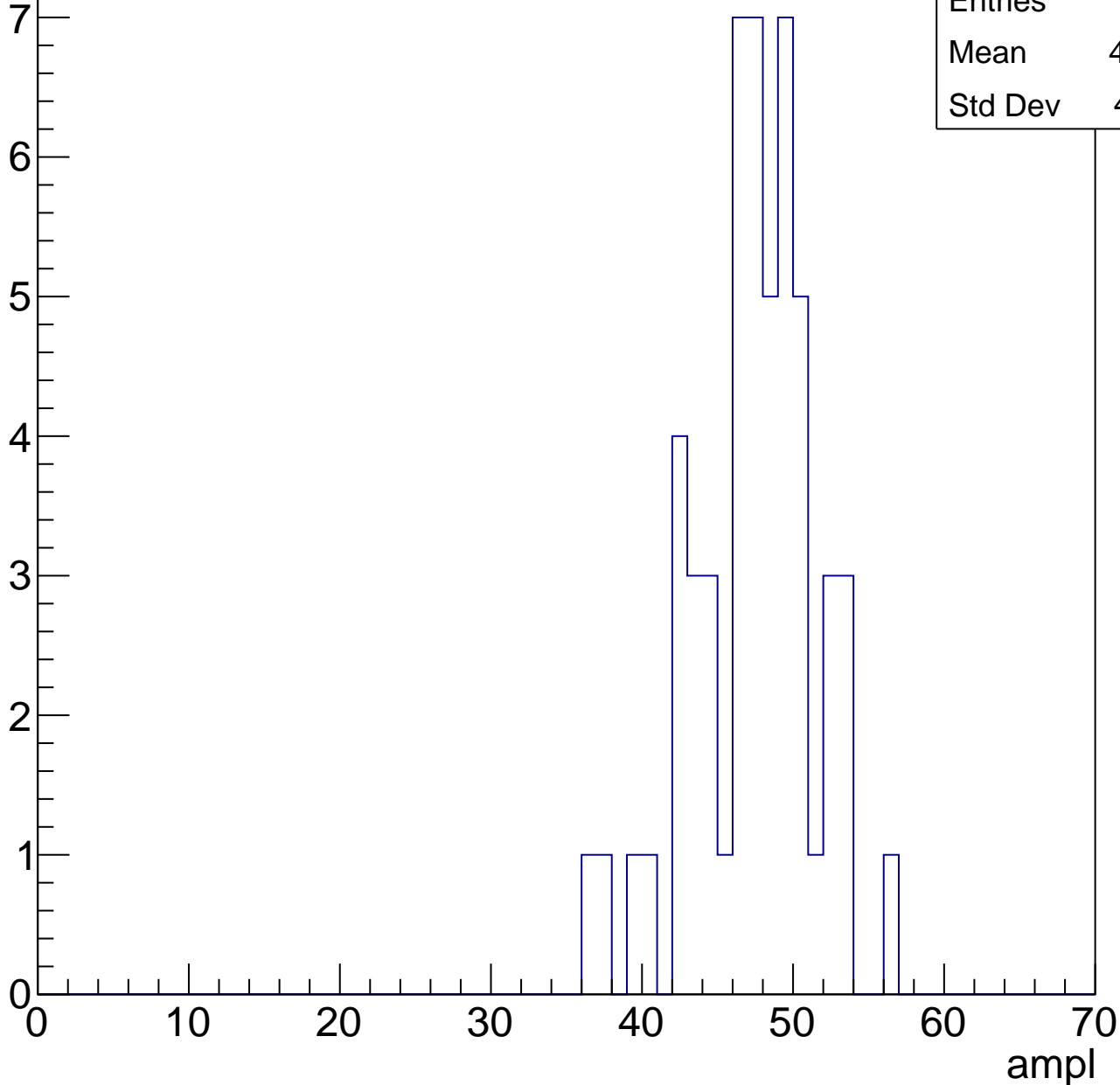


# B1L103S, U1-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

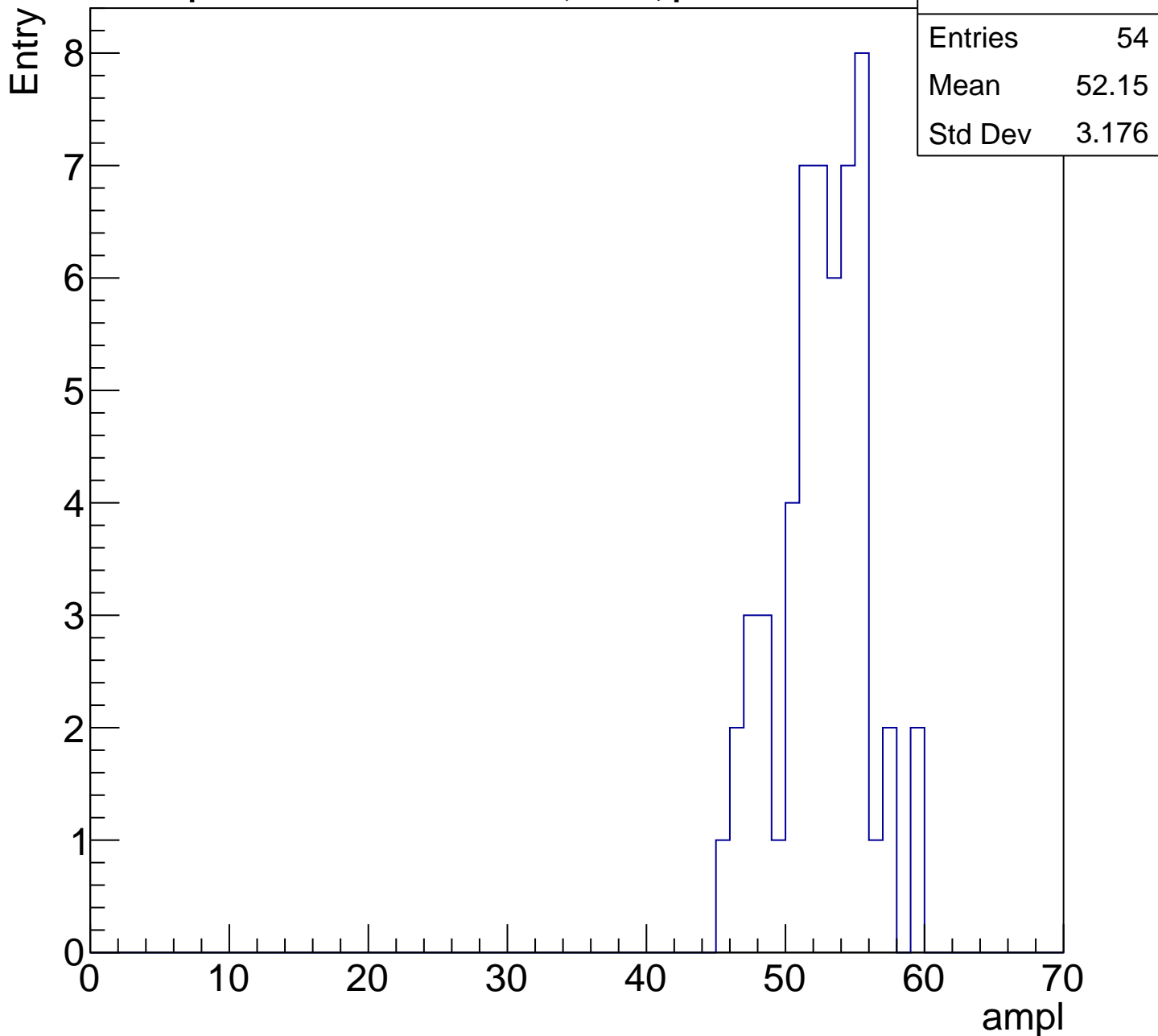
Entry

Entries	54
Mean	46.89
Std Dev	4.031



# B1L103S, U1-ch80, adc4

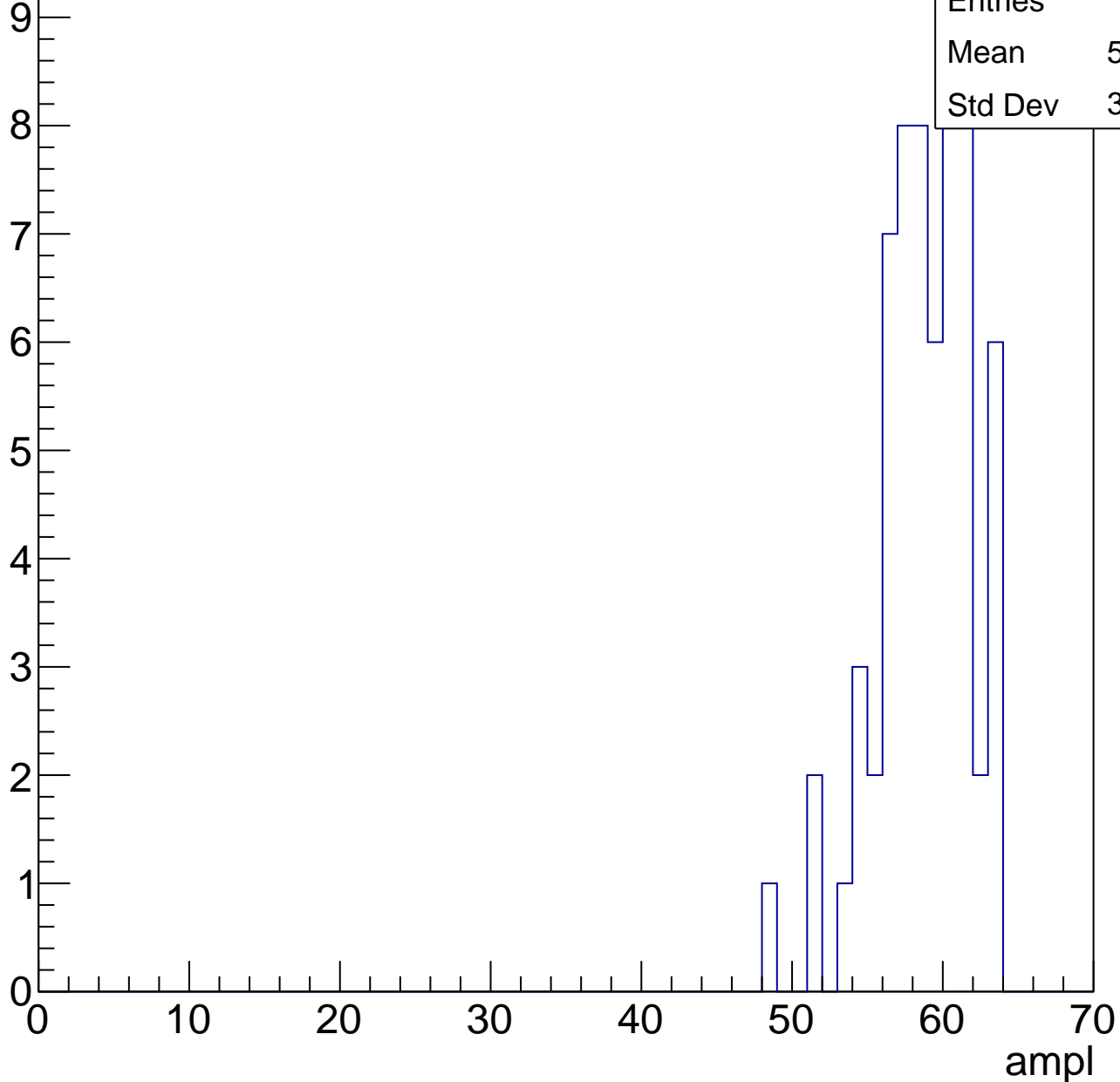
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U1-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

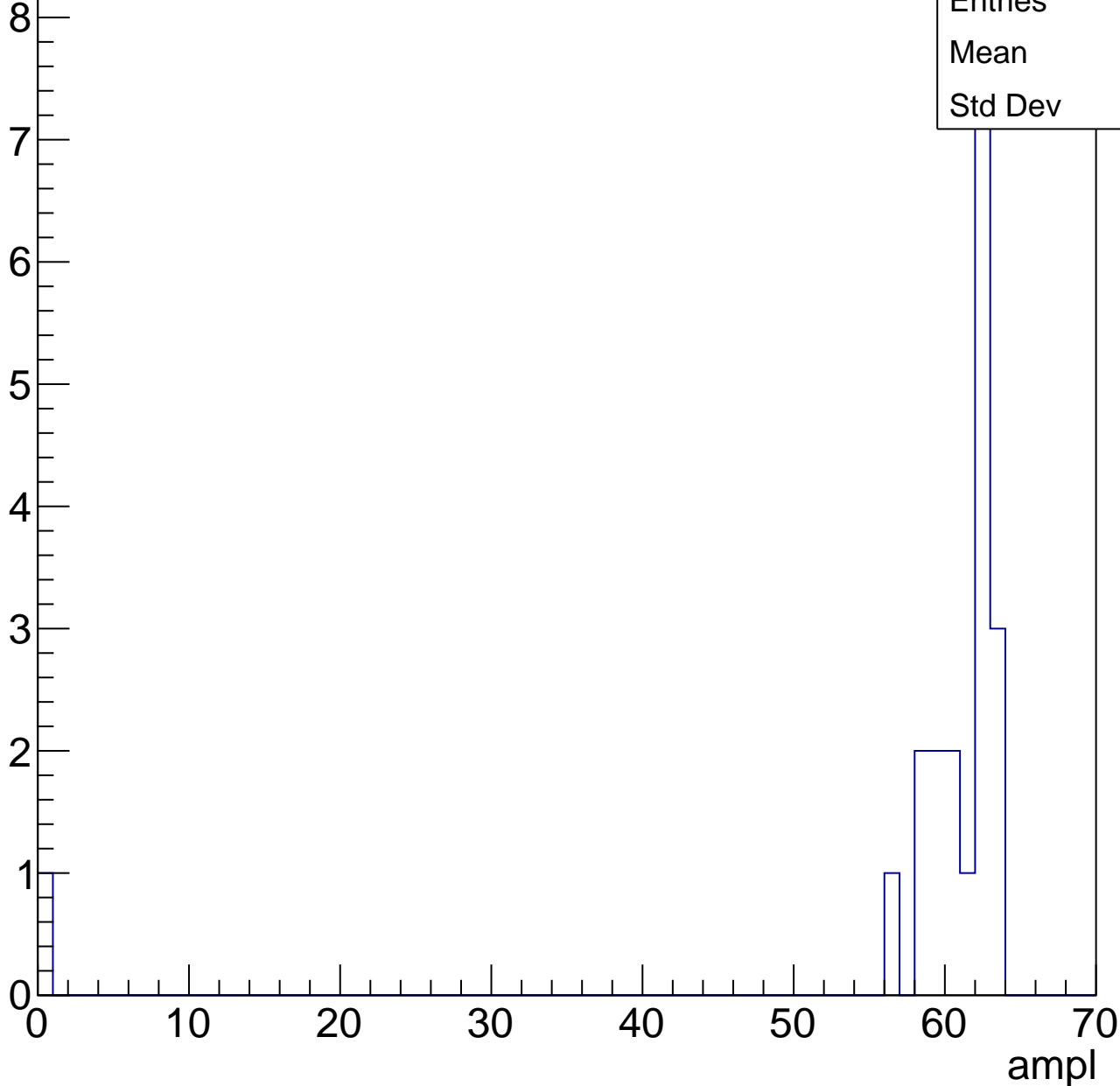


# B1L103S, U1-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	20
Mean	57.8
Std Dev	13.4





# B1L103S, U1-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch81, adc0

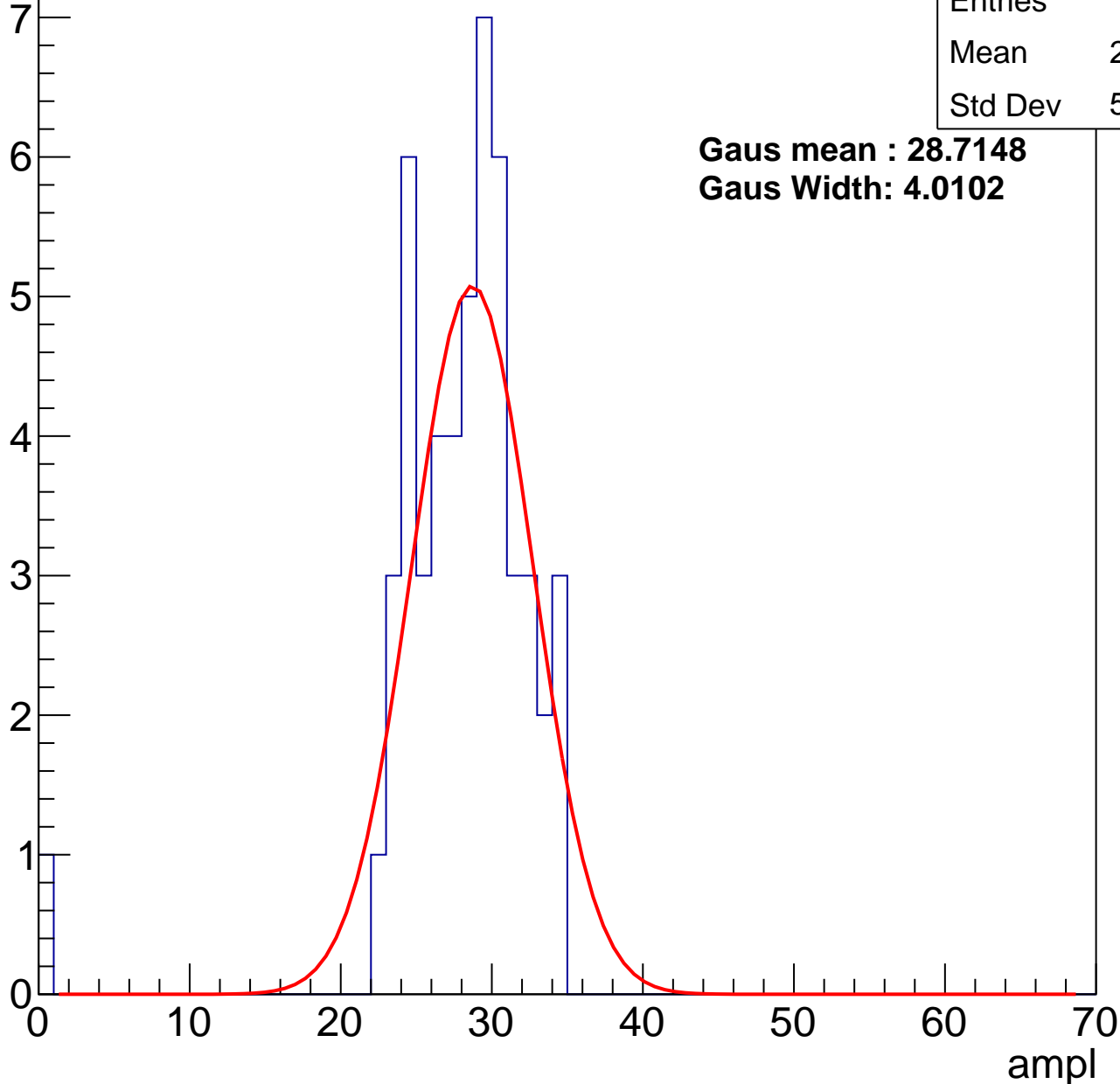
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	27.49
Std Dev	5.027

**Gaus mean : 28.7148**

**Gaus Width: 4.0102**



# B1L103S, U1-ch81, adc1

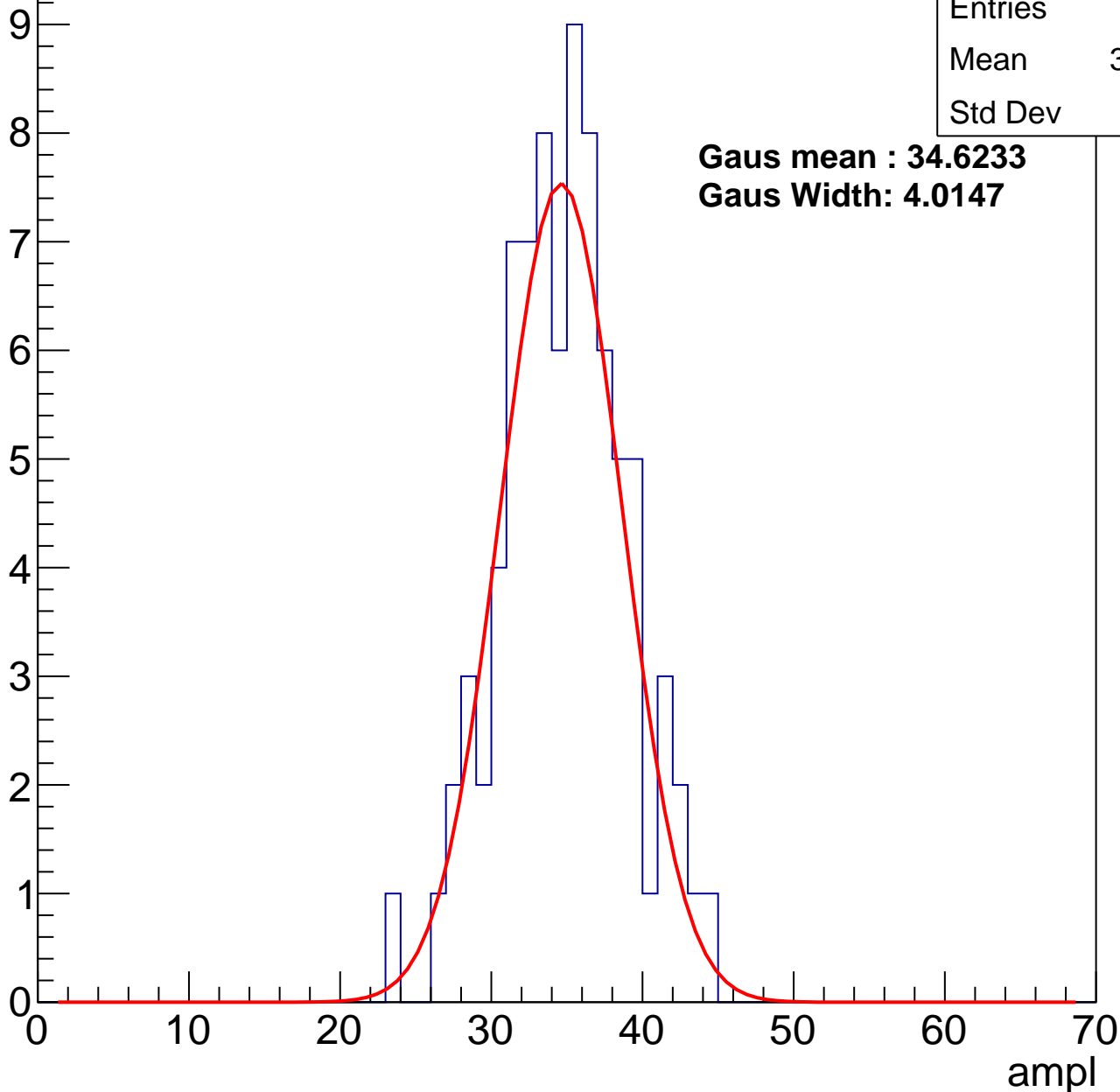
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	82
Mean	34.37
Std Dev	4.11

**Gaus mean : 34.6233**

**Gaus Width: 4.0147**



# B1L103S, U1-ch81, adc2

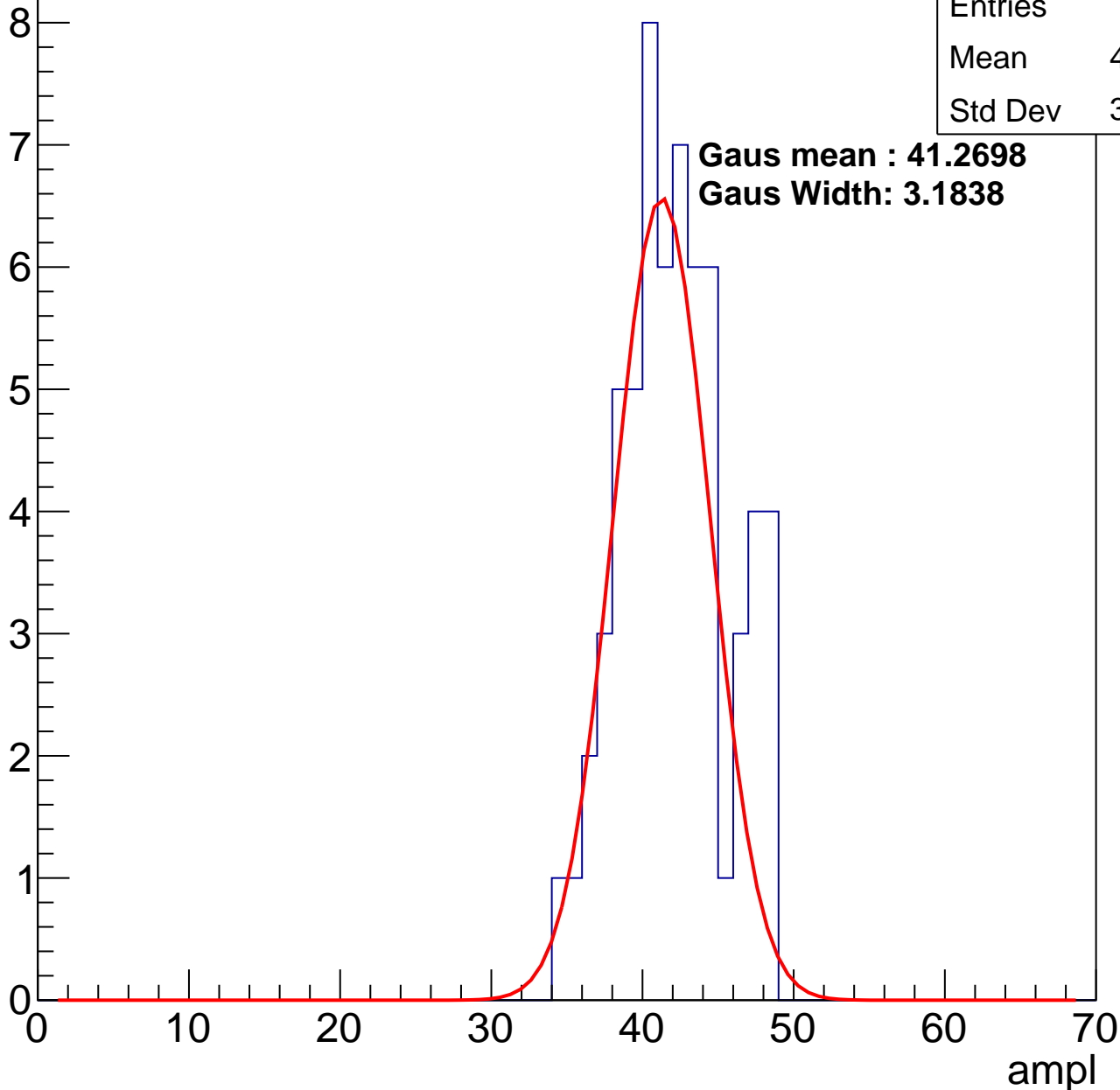
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	41.65
Std Dev	3.469

**Gaus mean : 41.2698**

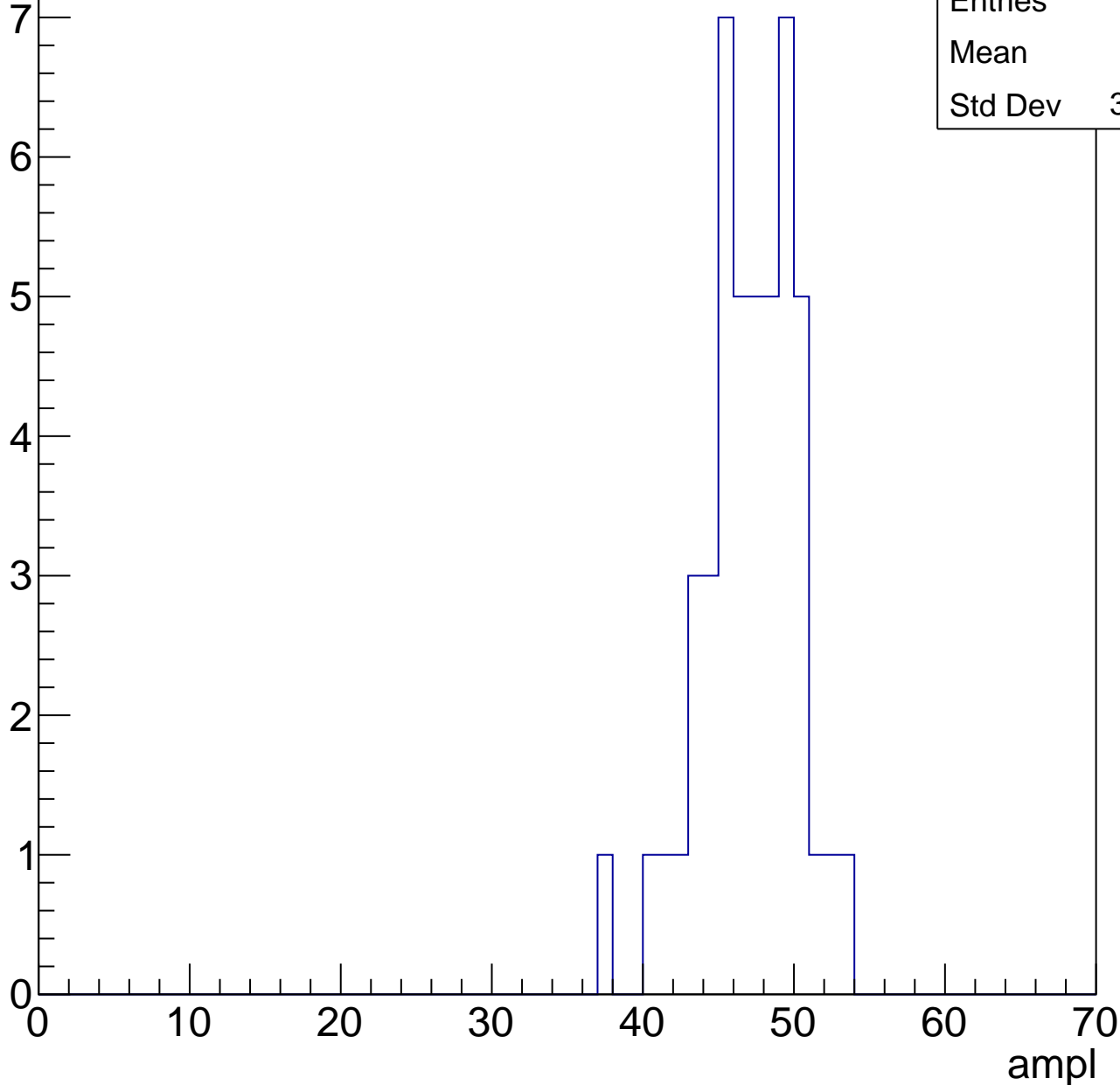
**Gaus Width: 3.1838**



# B1L103S, U1-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

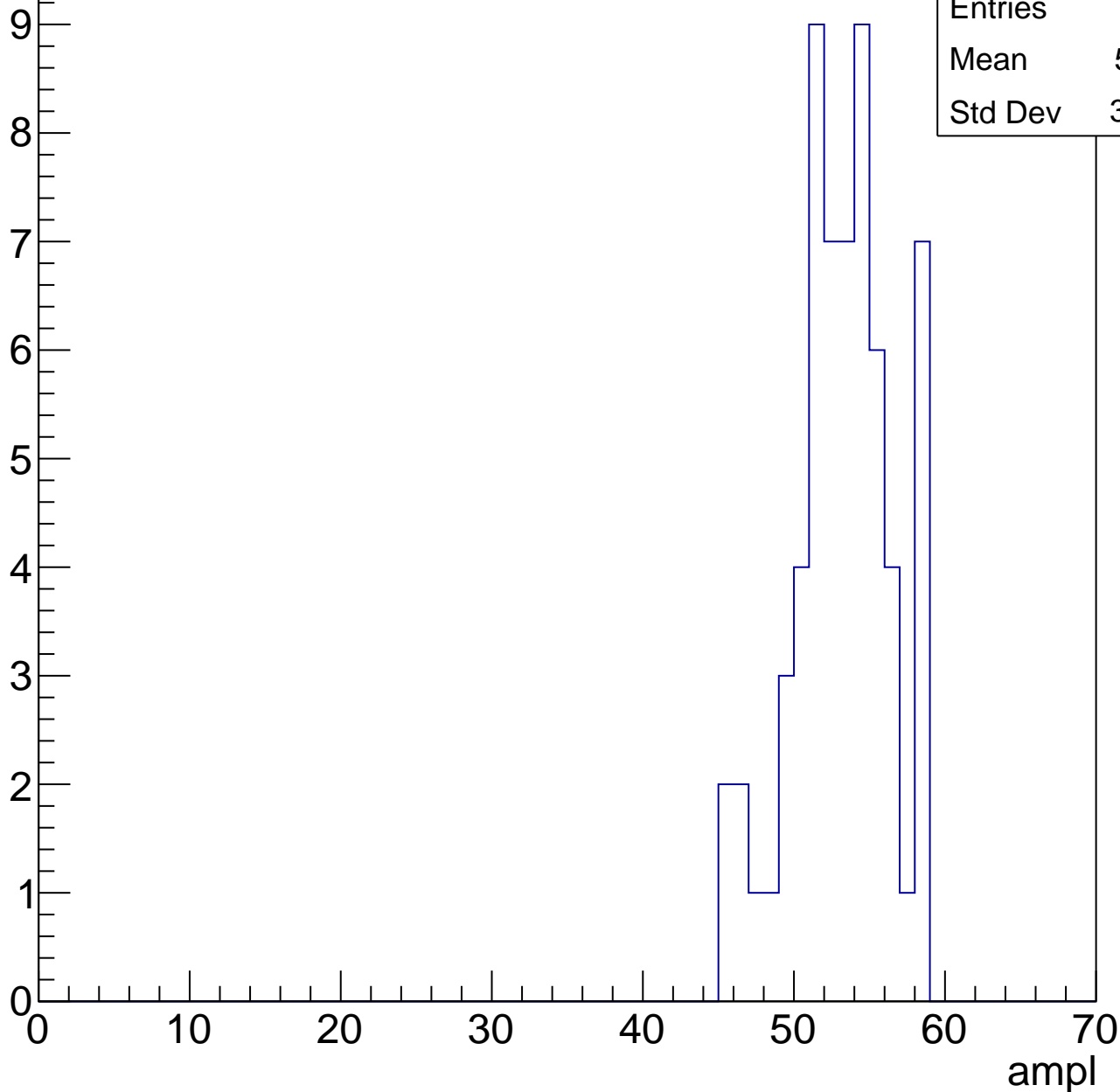
Entry



# B1L103S, U1-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



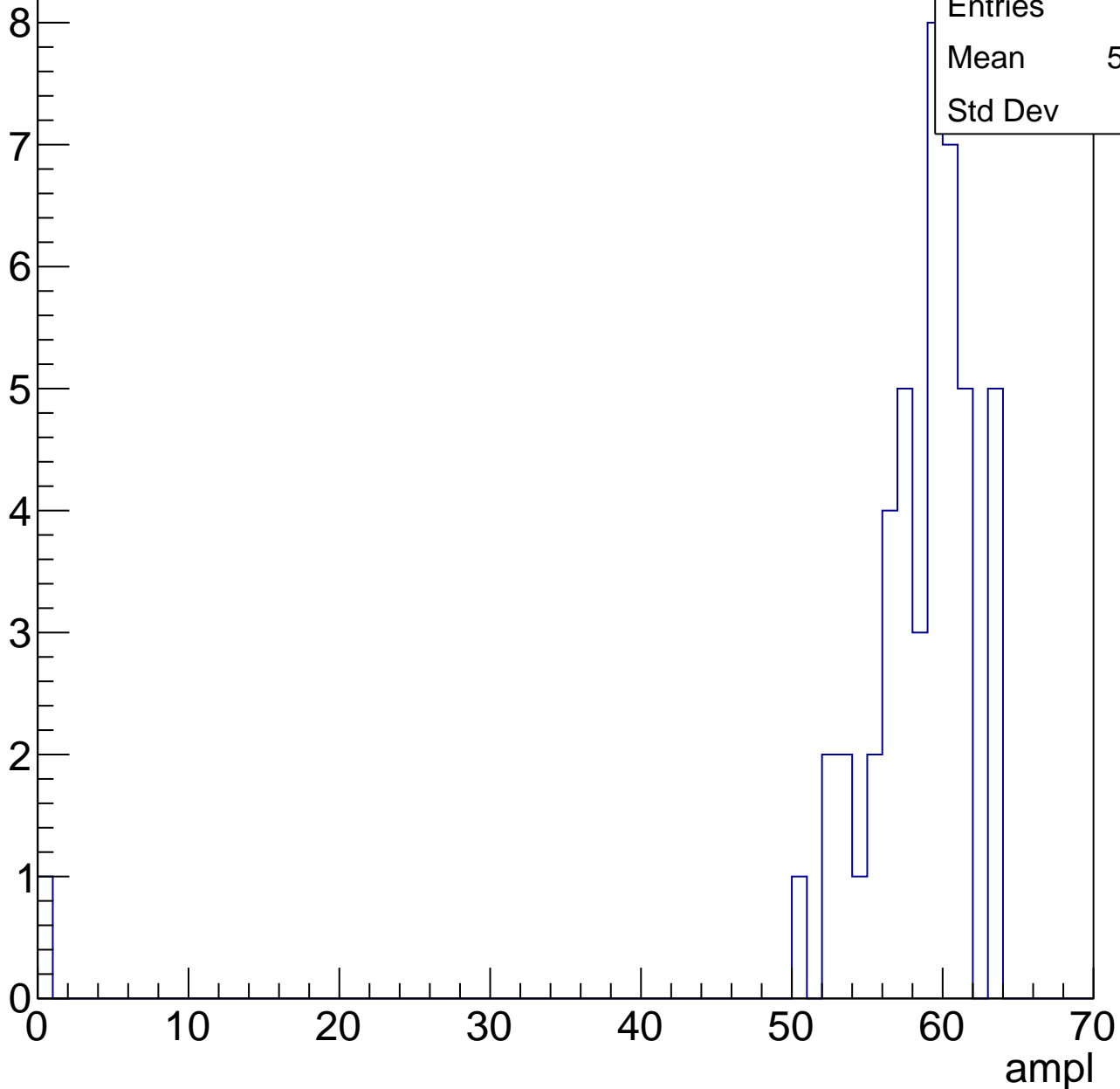
Entries	63
Mean	52.71
Std Dev	3.258

# B1L103S, U1-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	56.93
Std Dev	9.04

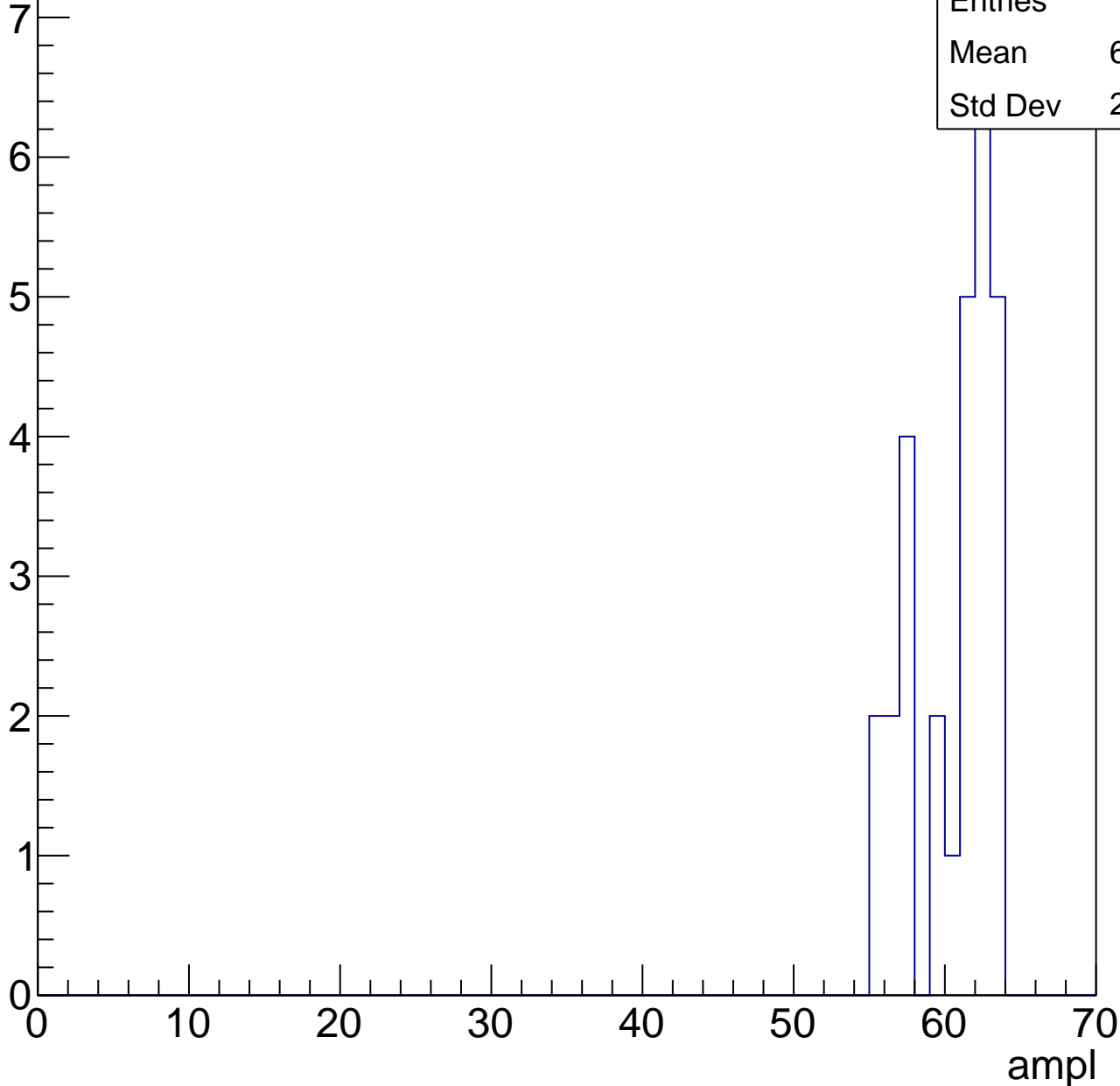


# B1L103S, U1-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	28
Mean	60.07
Std Dev	2.658

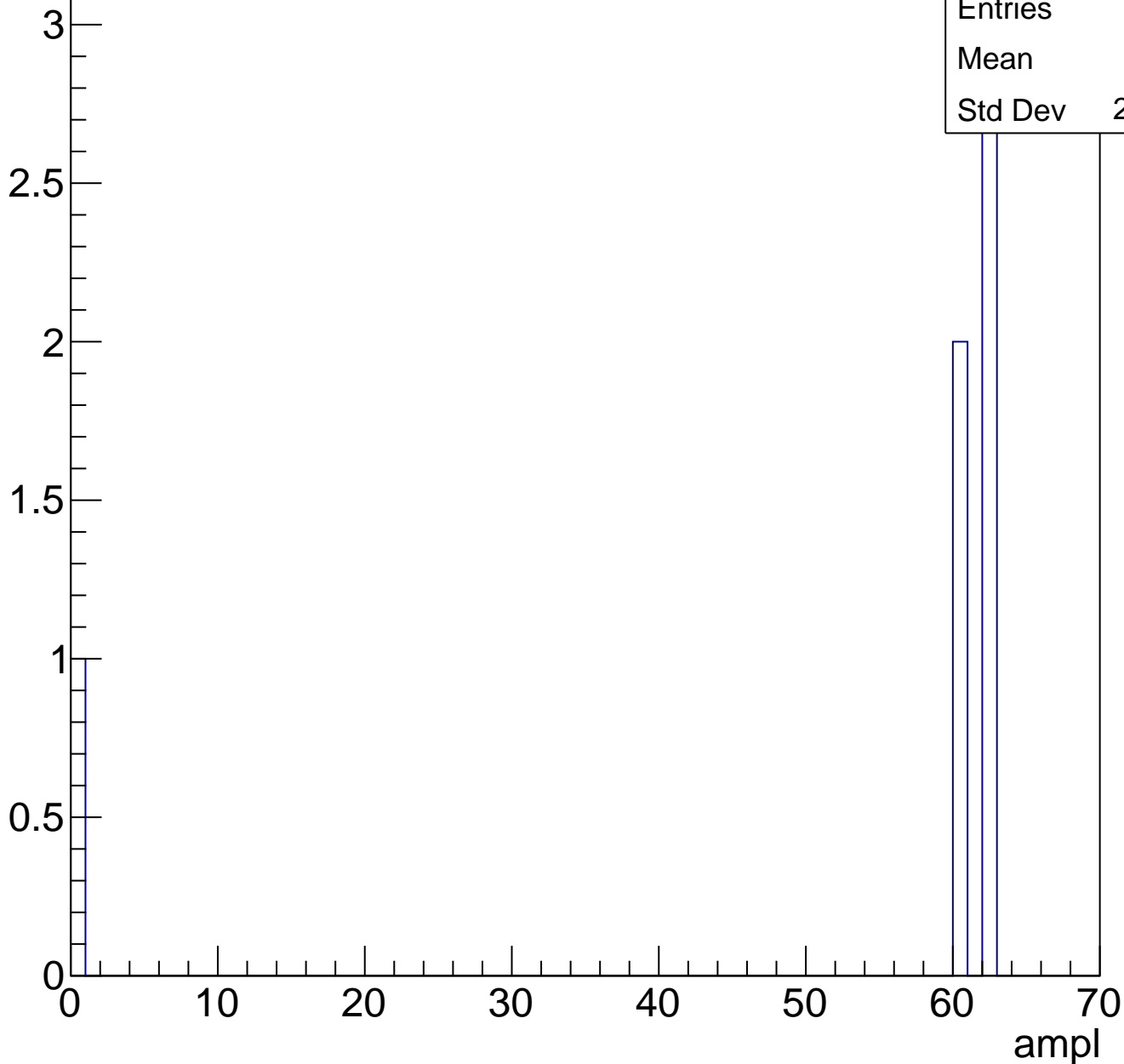




# B1L103S, U1-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch82, adc0

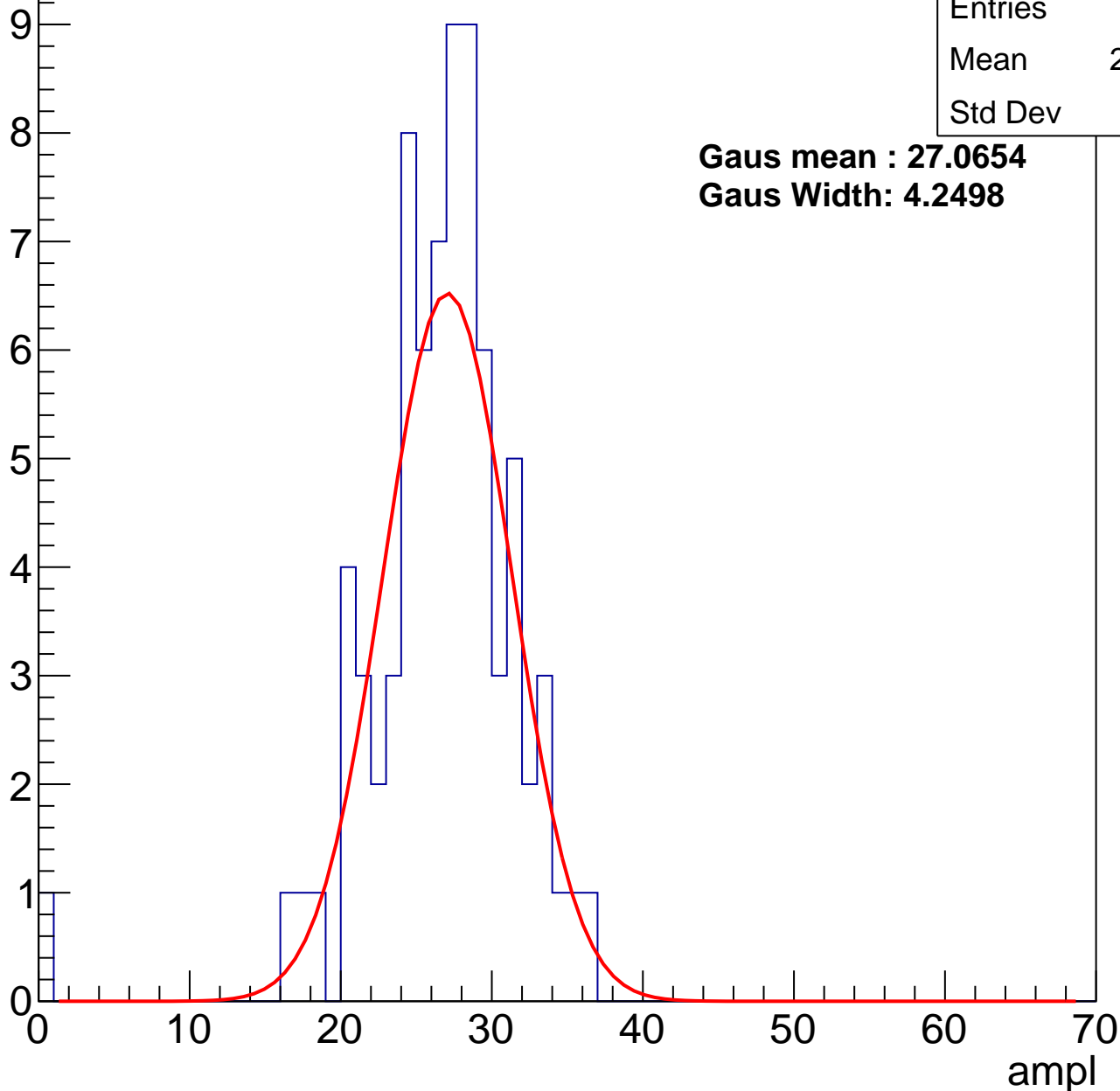
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	26.14
Std Dev	5.06

**Gaus mean : 27.0654**

**Gaus Width: 4.2498**



# B1L103S, U1-ch82, adc1

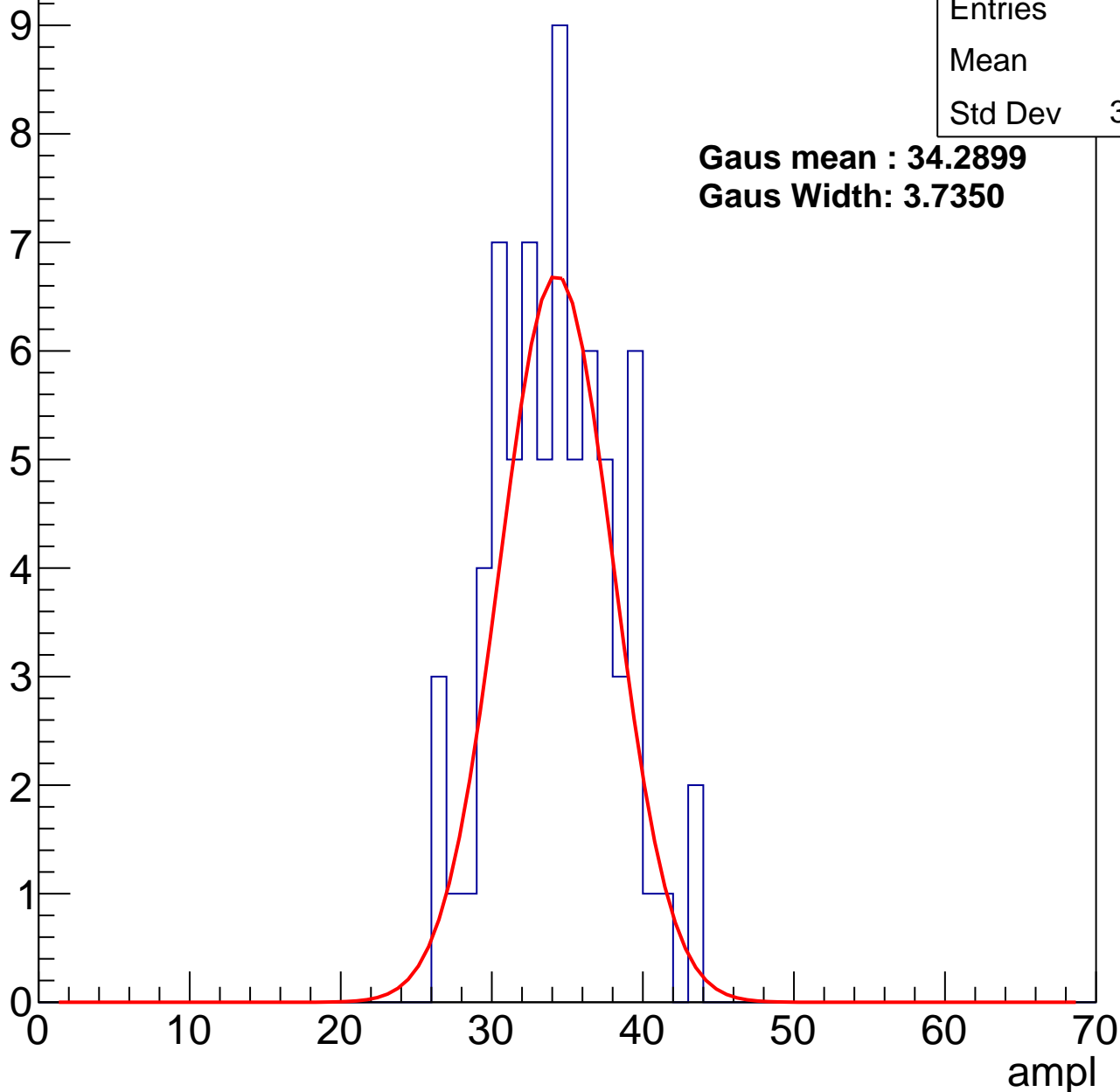
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	33.8
Std Dev	3.906

**Gaus mean : 34.2899**

**Gaus Width: 3.7350**



# B1L103S, U1-ch82, adc2

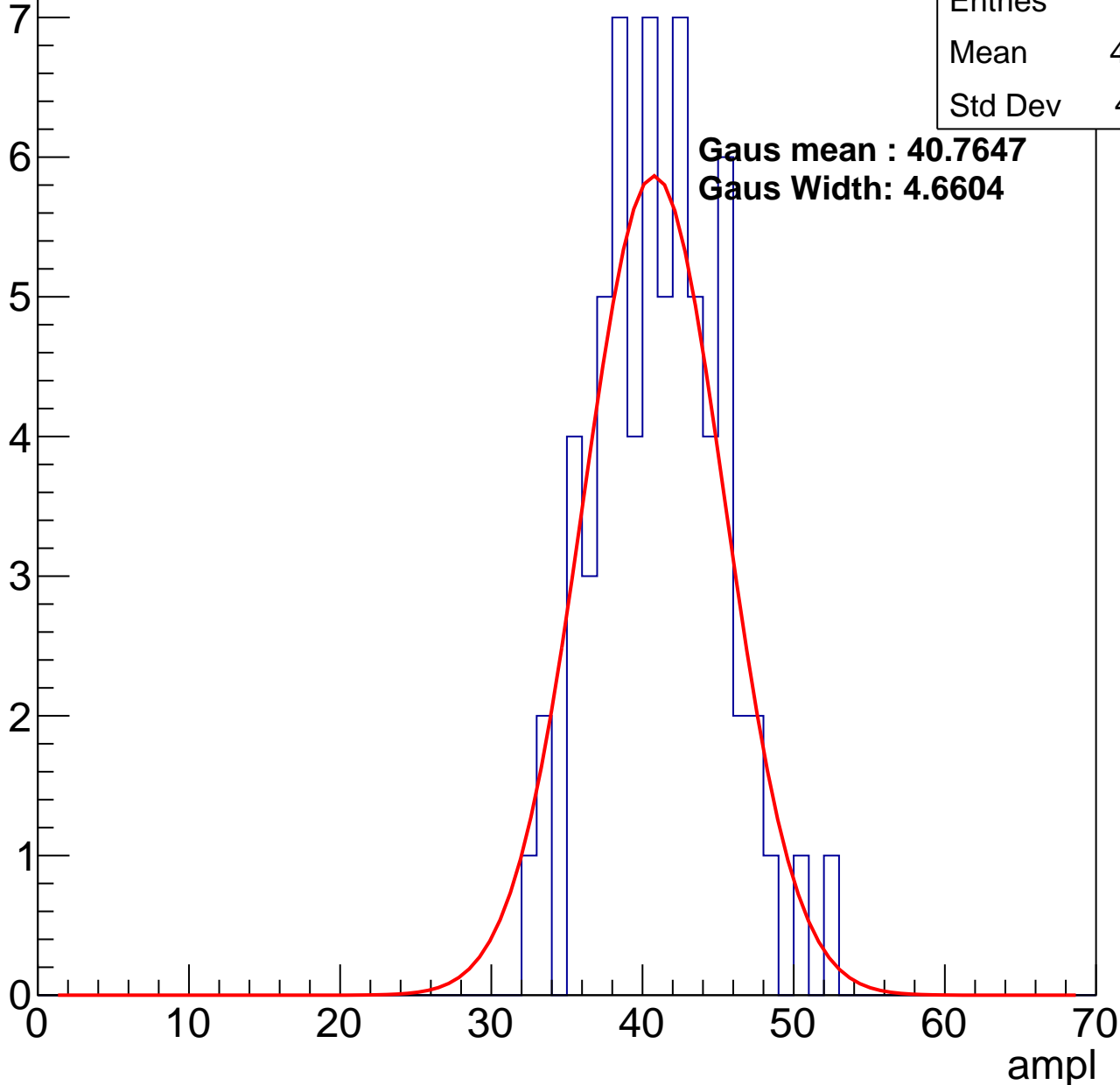
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	40.73
Std Dev	4.091

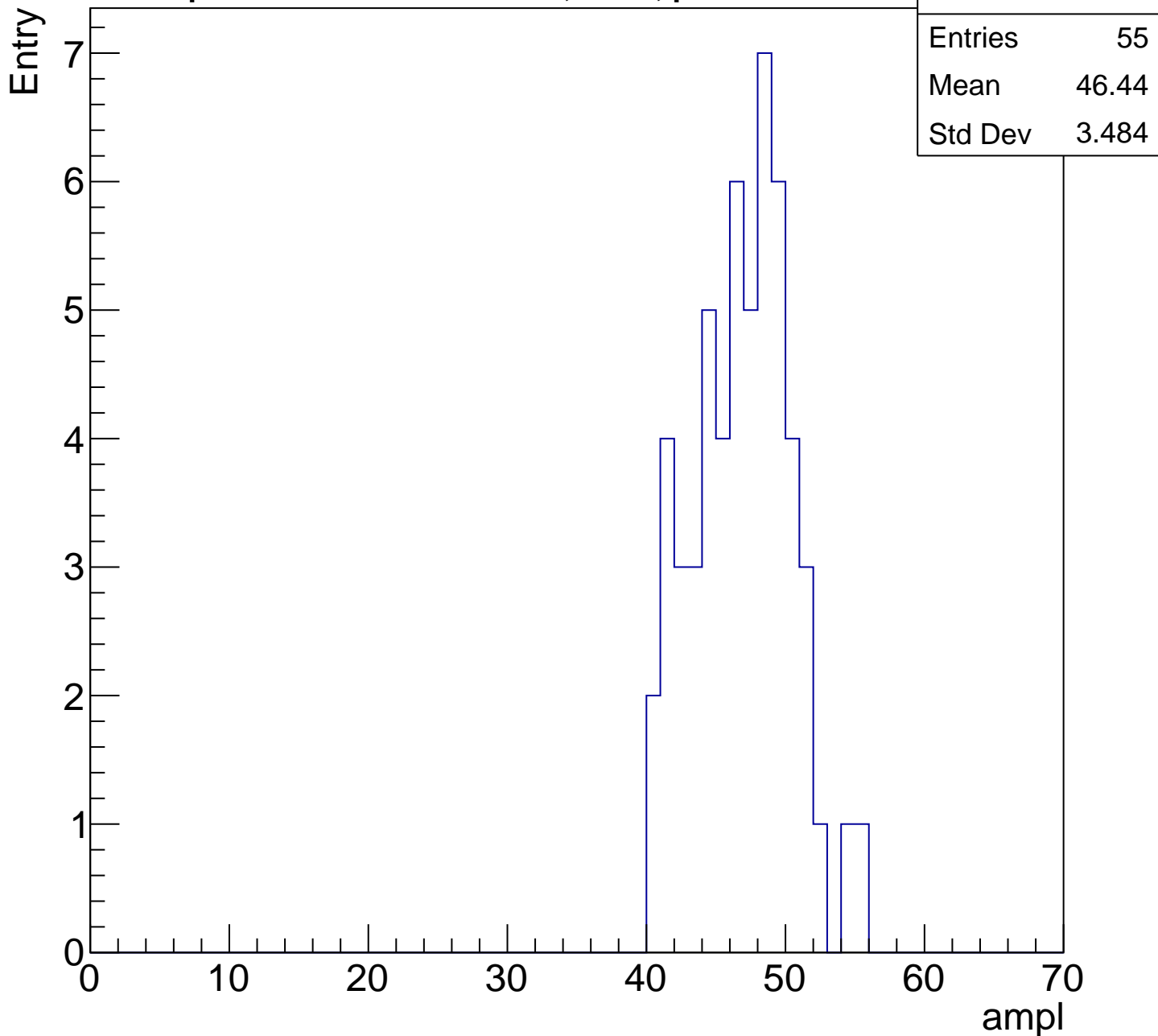
**Gaus mean : 40.7647**

**Gaus Width: 4.6604**



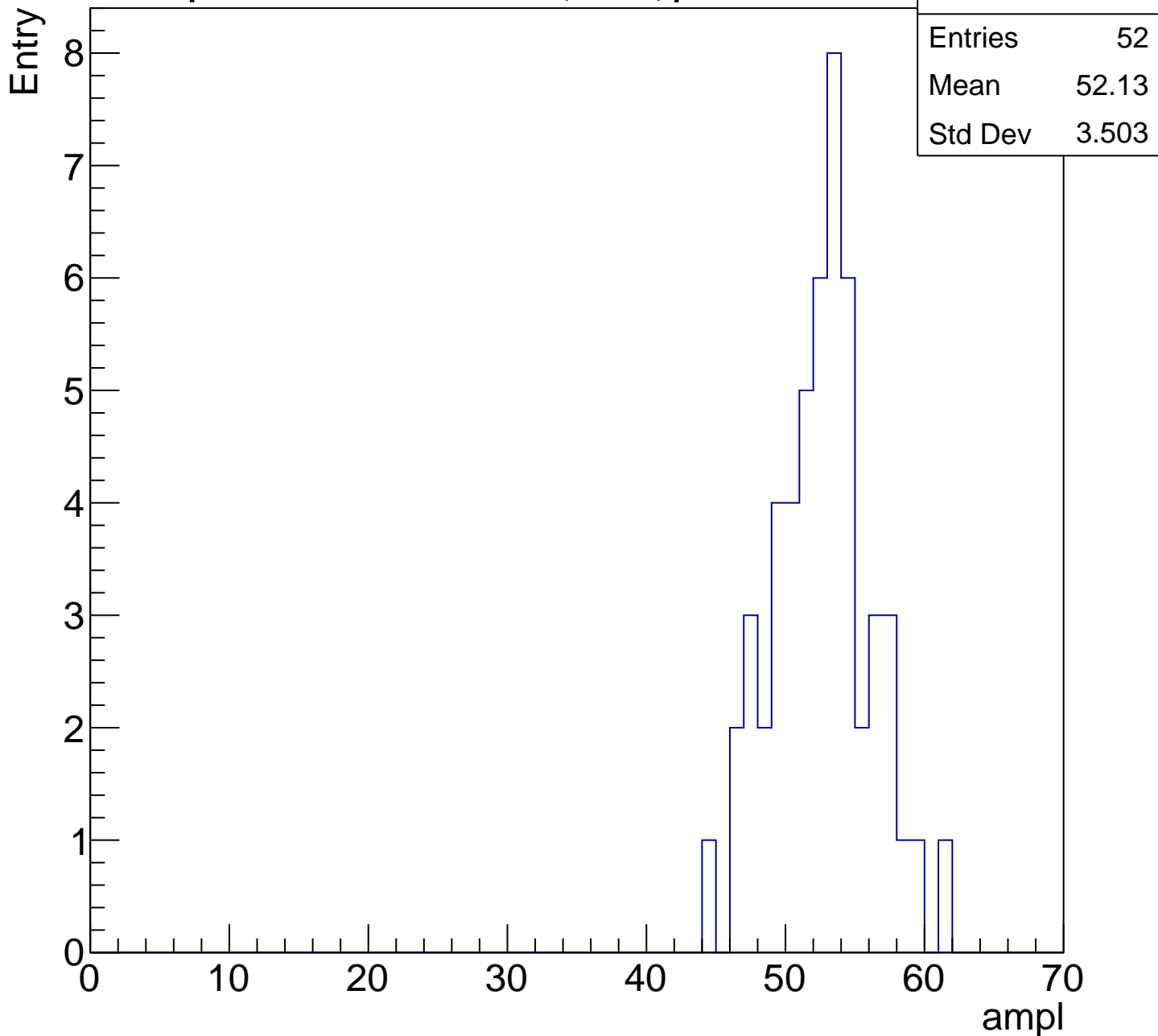
# B1L103S, U1-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2



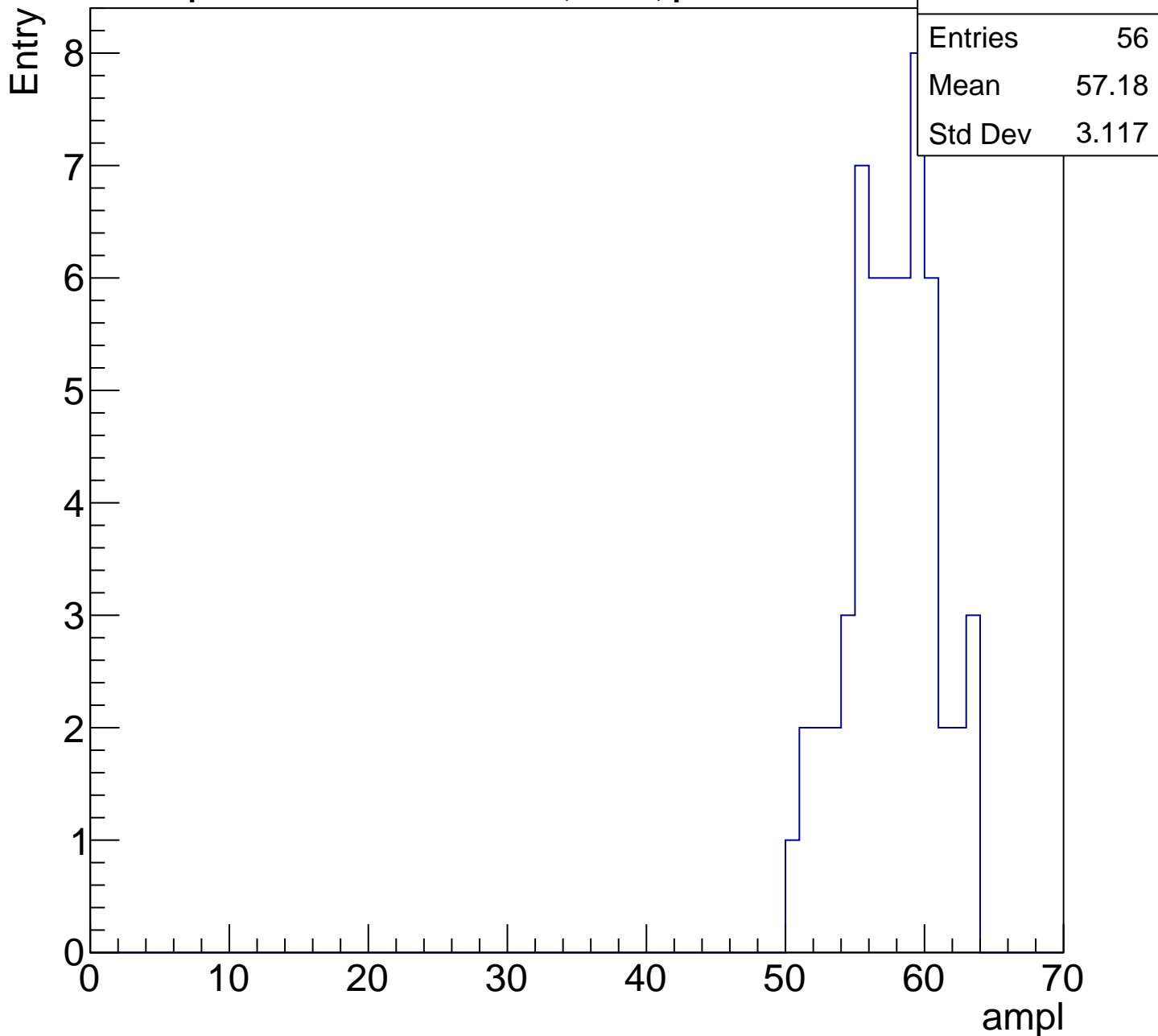
# B1L103S, U1-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U1-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

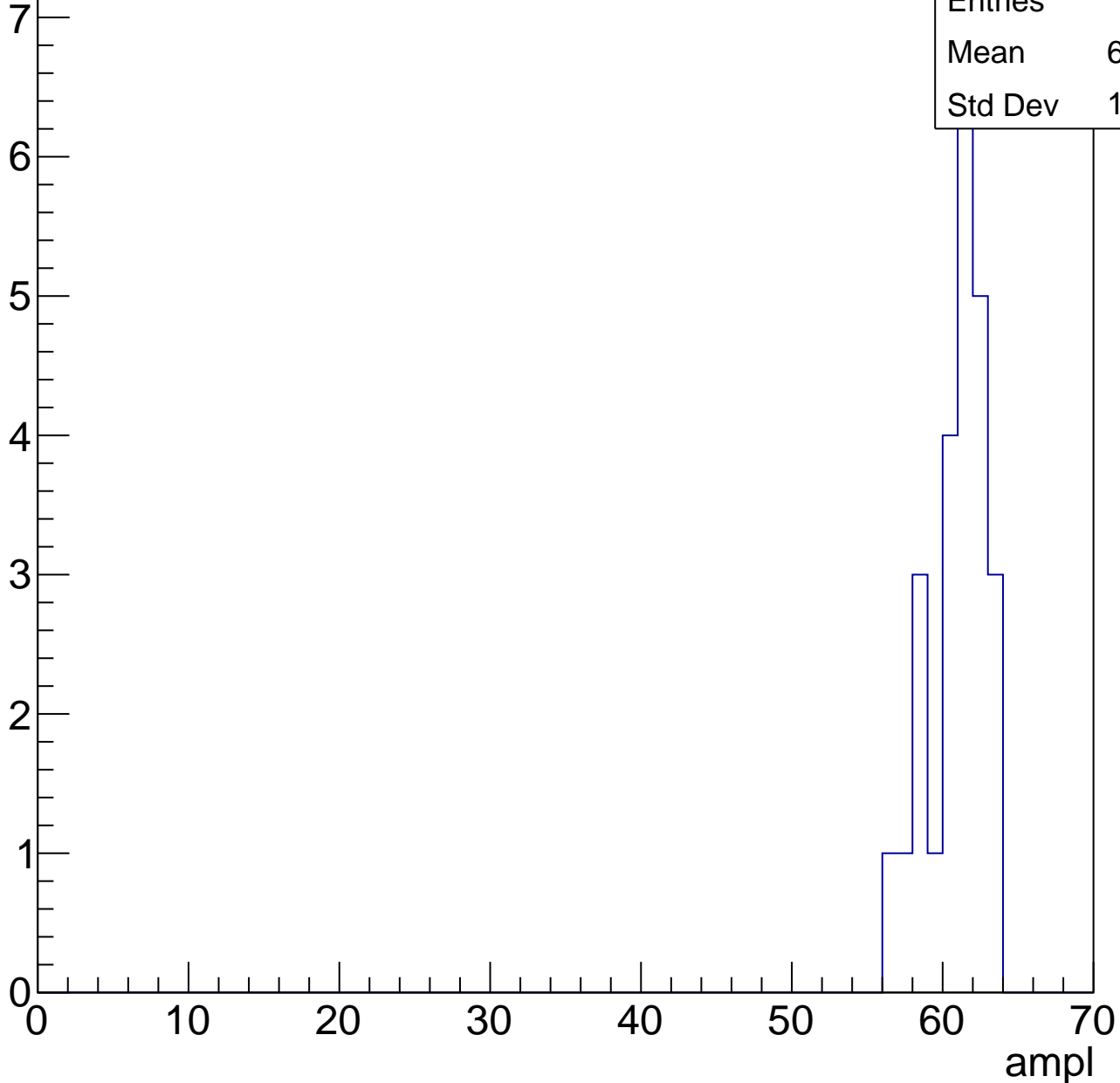


# B1L103S, U1-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	25
Mean	60.48
Std Dev	1.857

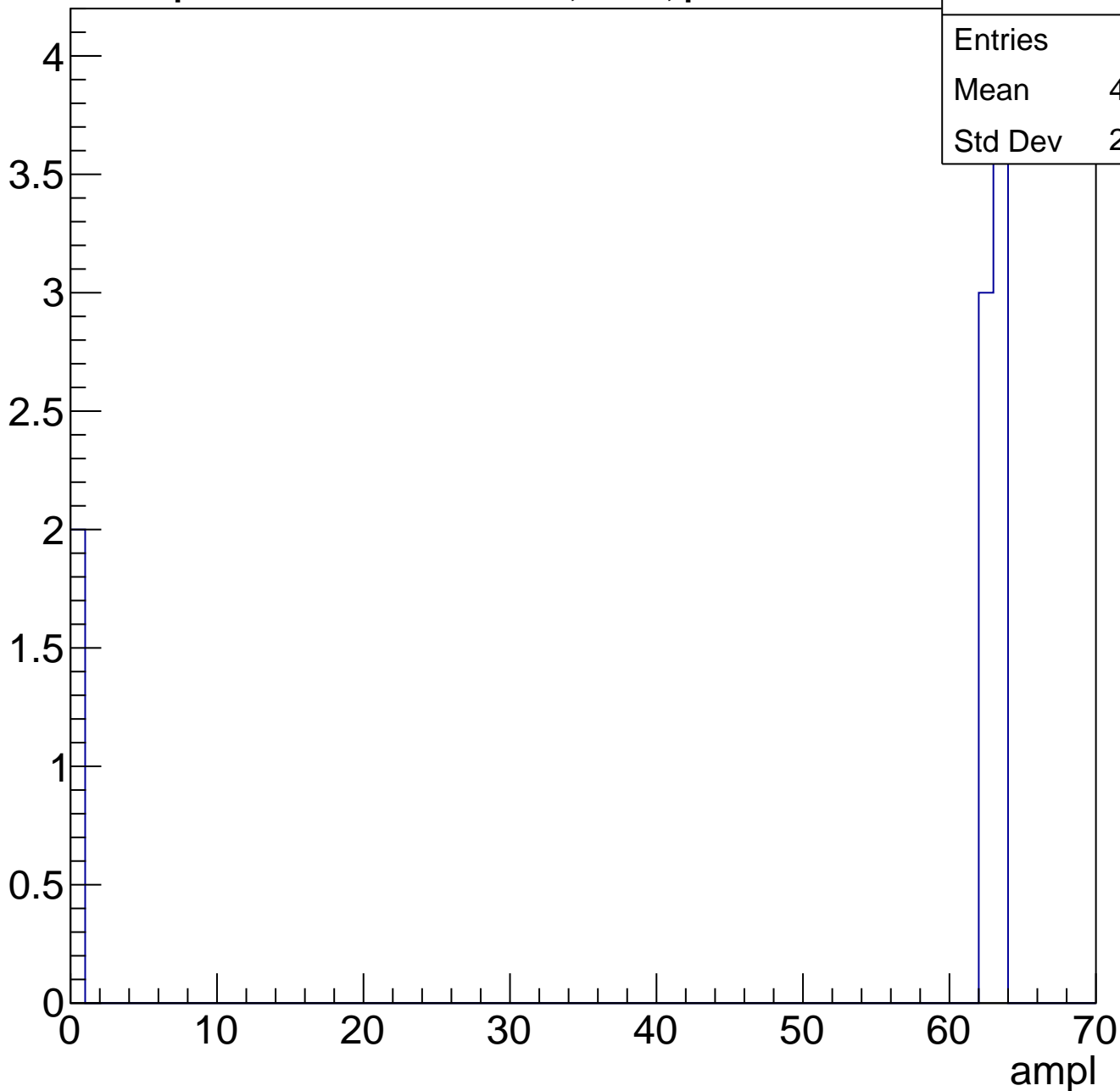




# B1L103S, U1-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch83, adc0

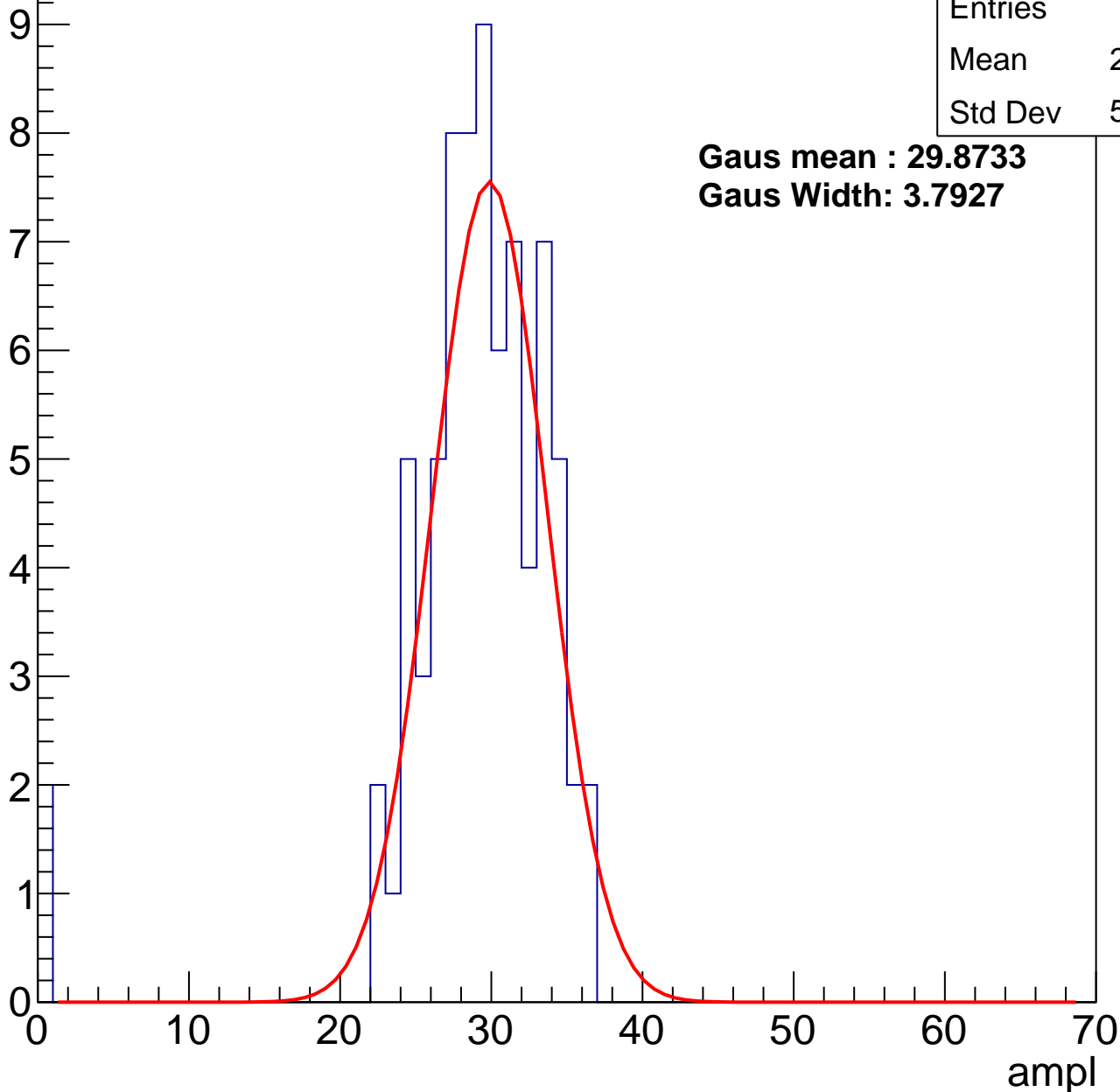
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	28.43
Std Dev	5.766

**Gaus mean : 29.8733**

**Gaus Width: 3.7927**



# B1L103S, U1-ch83, adc1

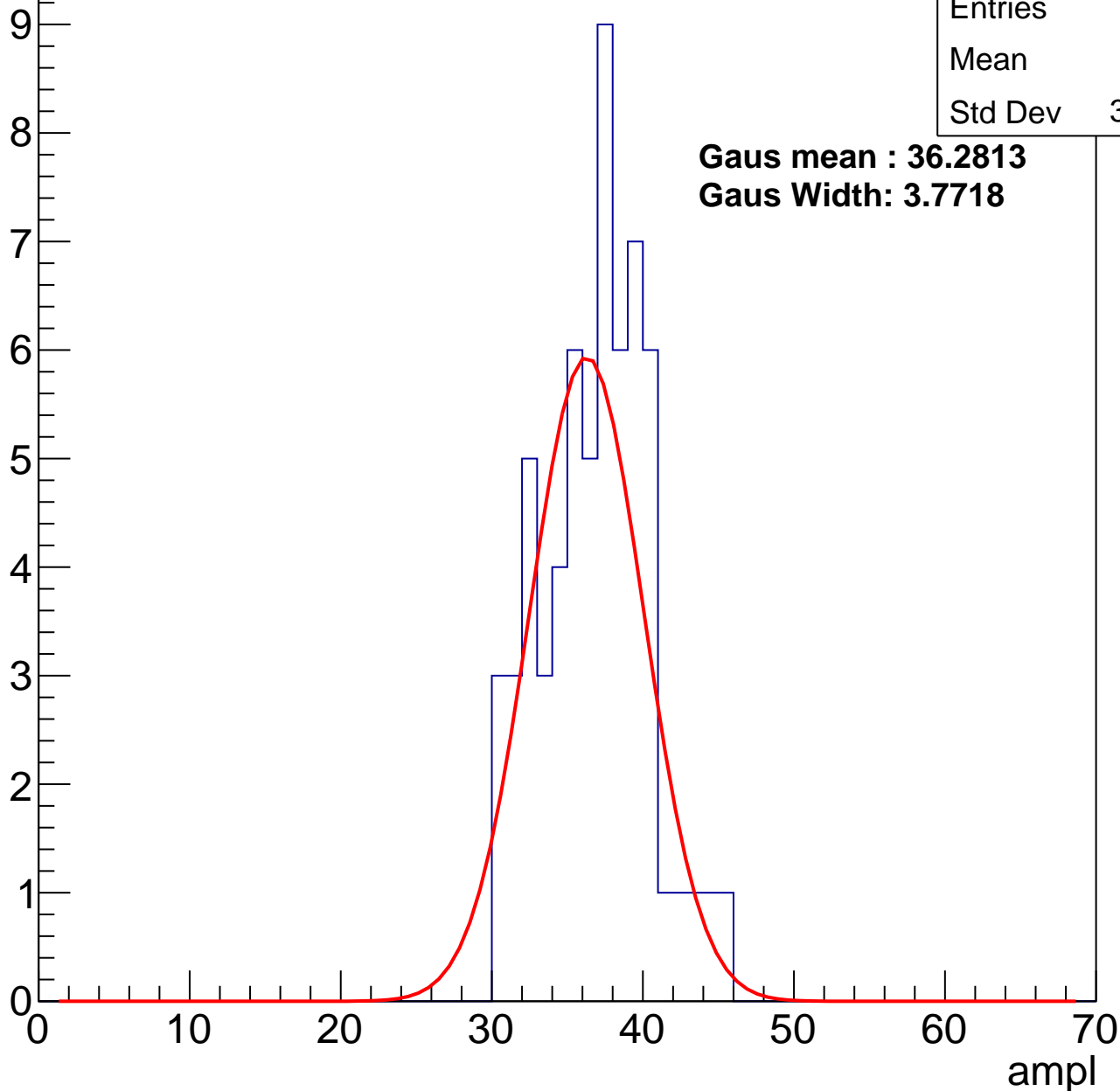
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	36.4
Std Dev	3.476

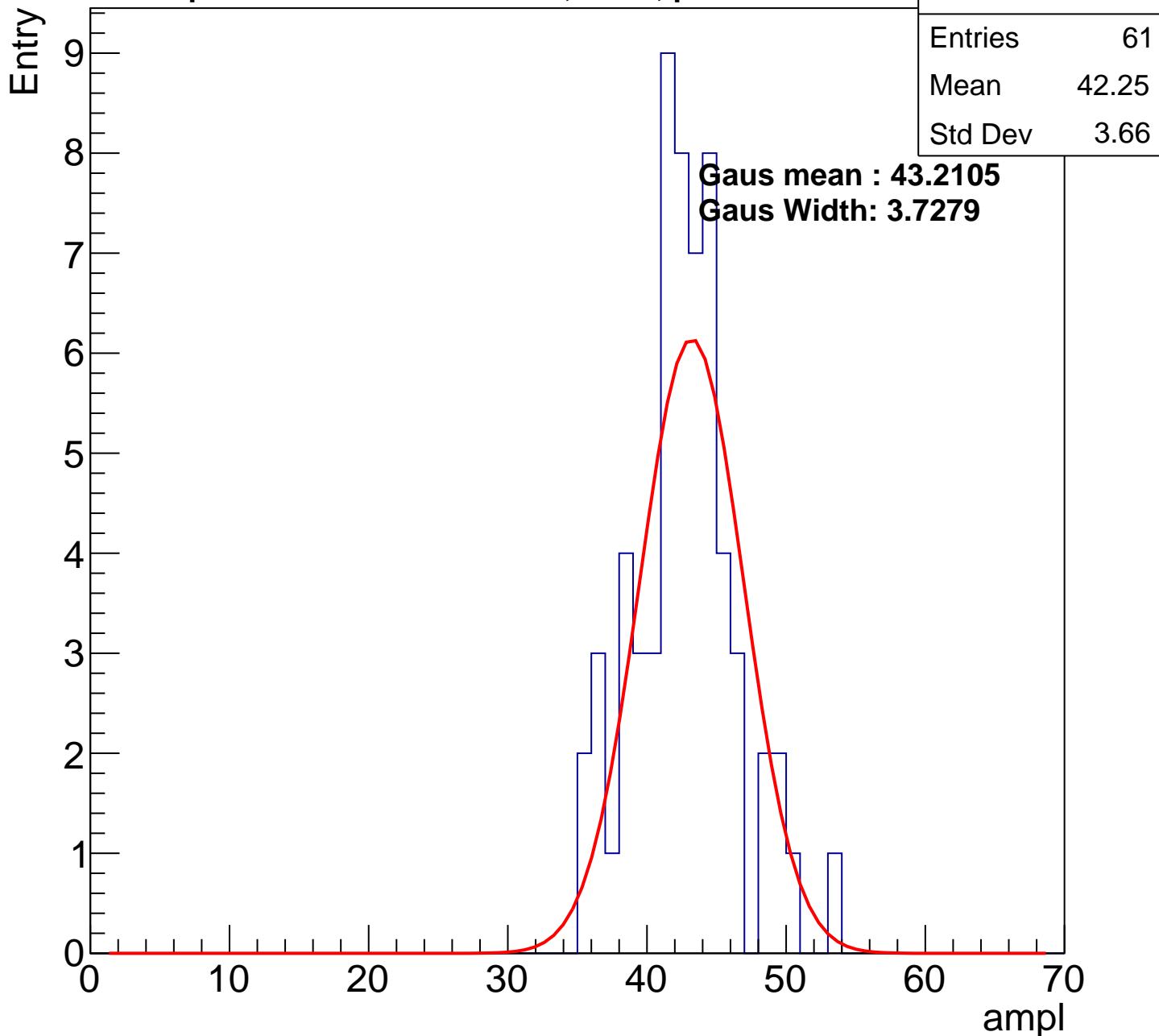
**Gaus mean : 36.2813**

**Gaus Width: 3.7718**



# B1L103S, U1-ch83, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

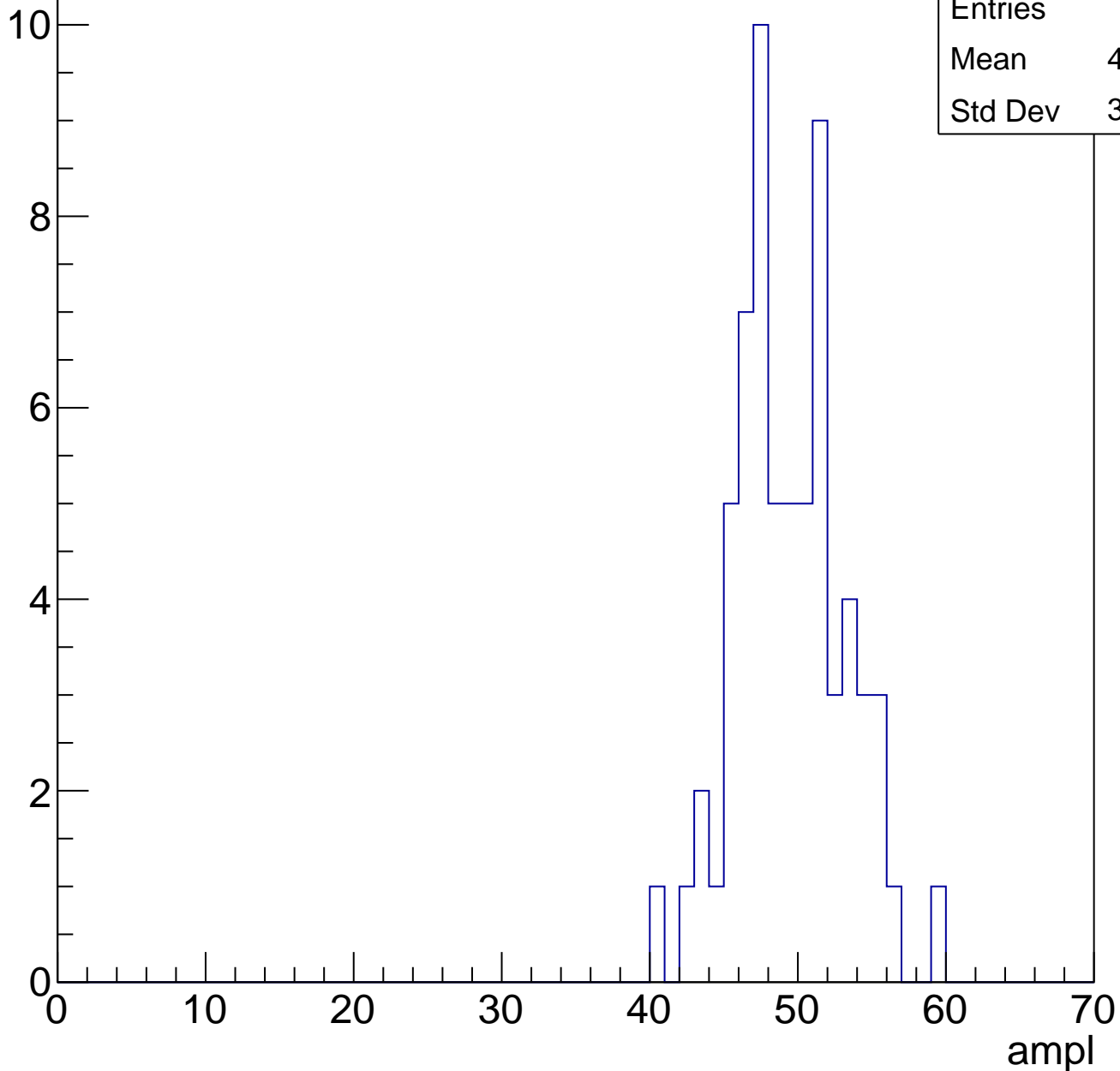


# B1L103S, U1-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	66
Mean	48.98
Std Dev	3.649

Entry

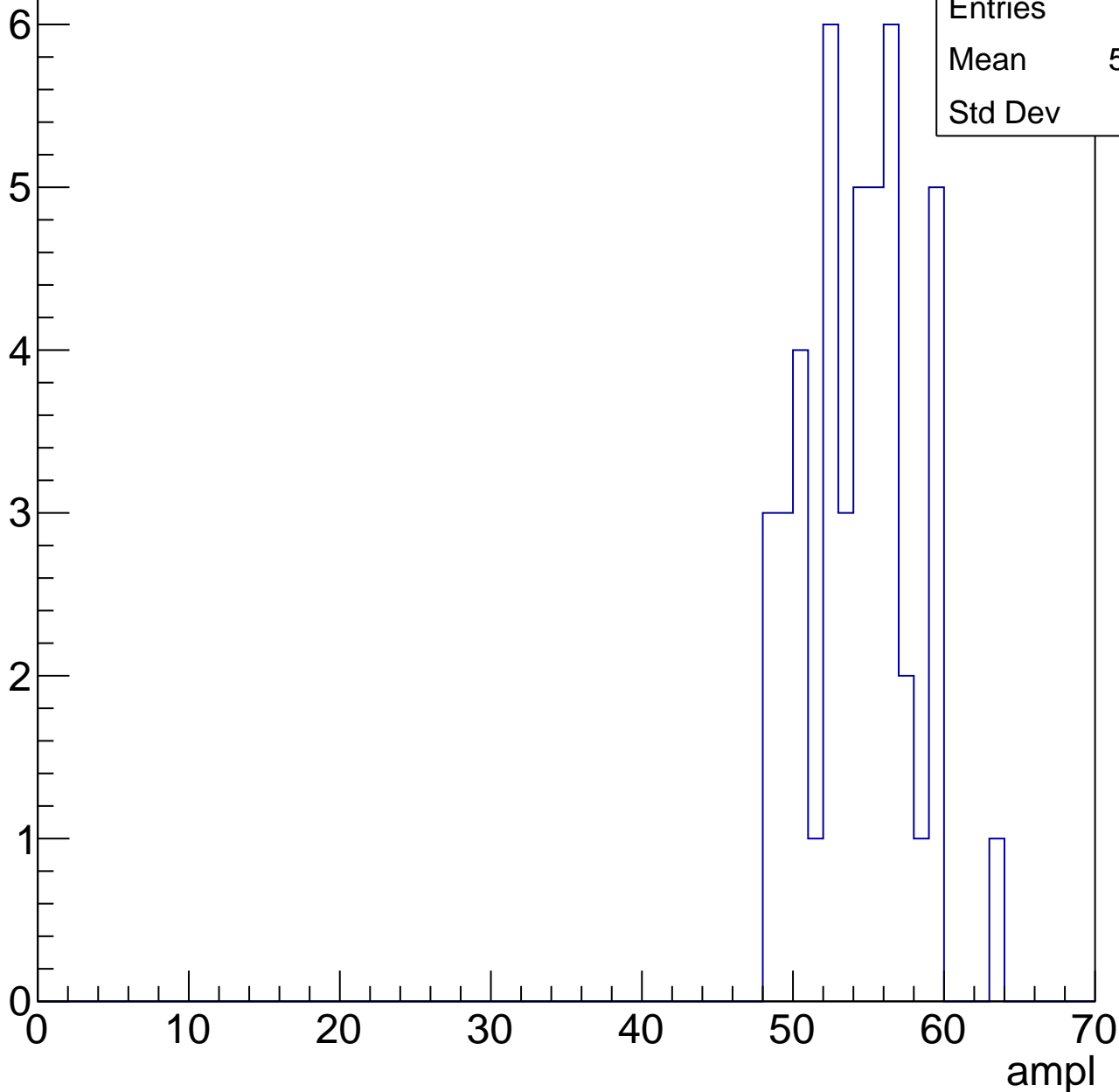


# B1L103S, U1-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

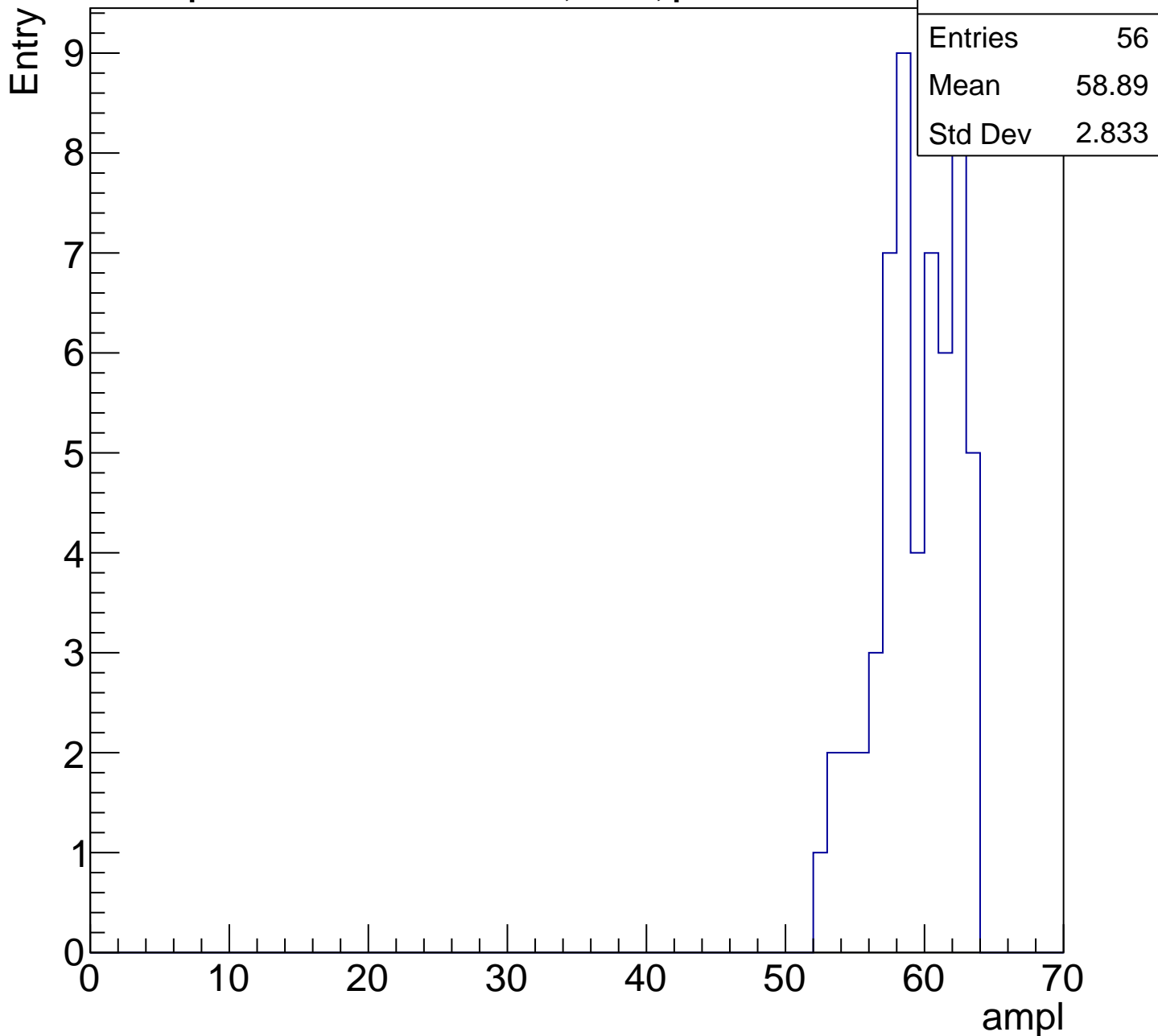
Entry

Entries	45
Mean	53.87
Std Dev	3.5



# B1L103S, U1-ch83, adc5

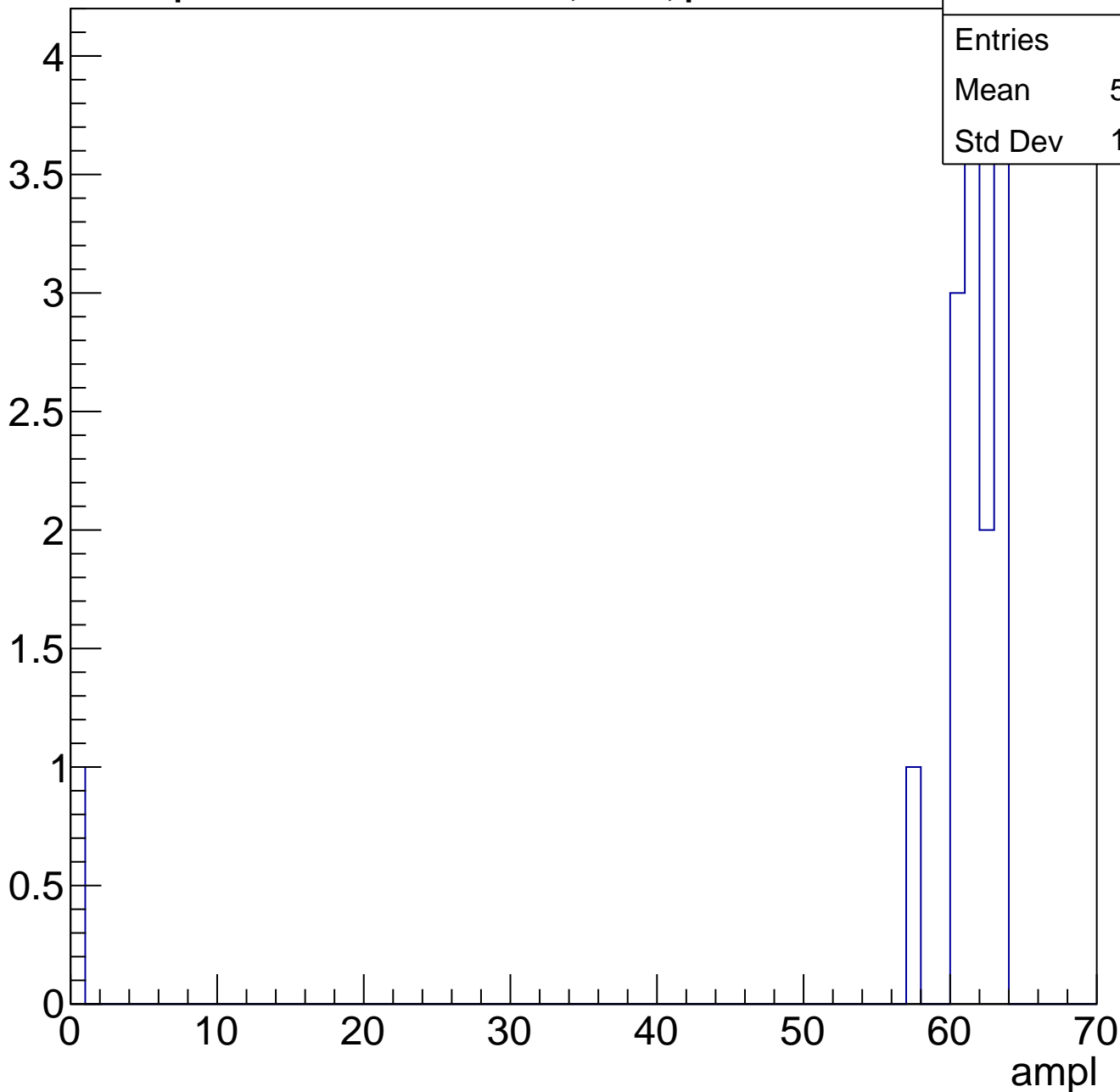
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U1-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	15
Mean	57.13
Std Dev	15.35



# B1L103S, U1-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch84, adc0

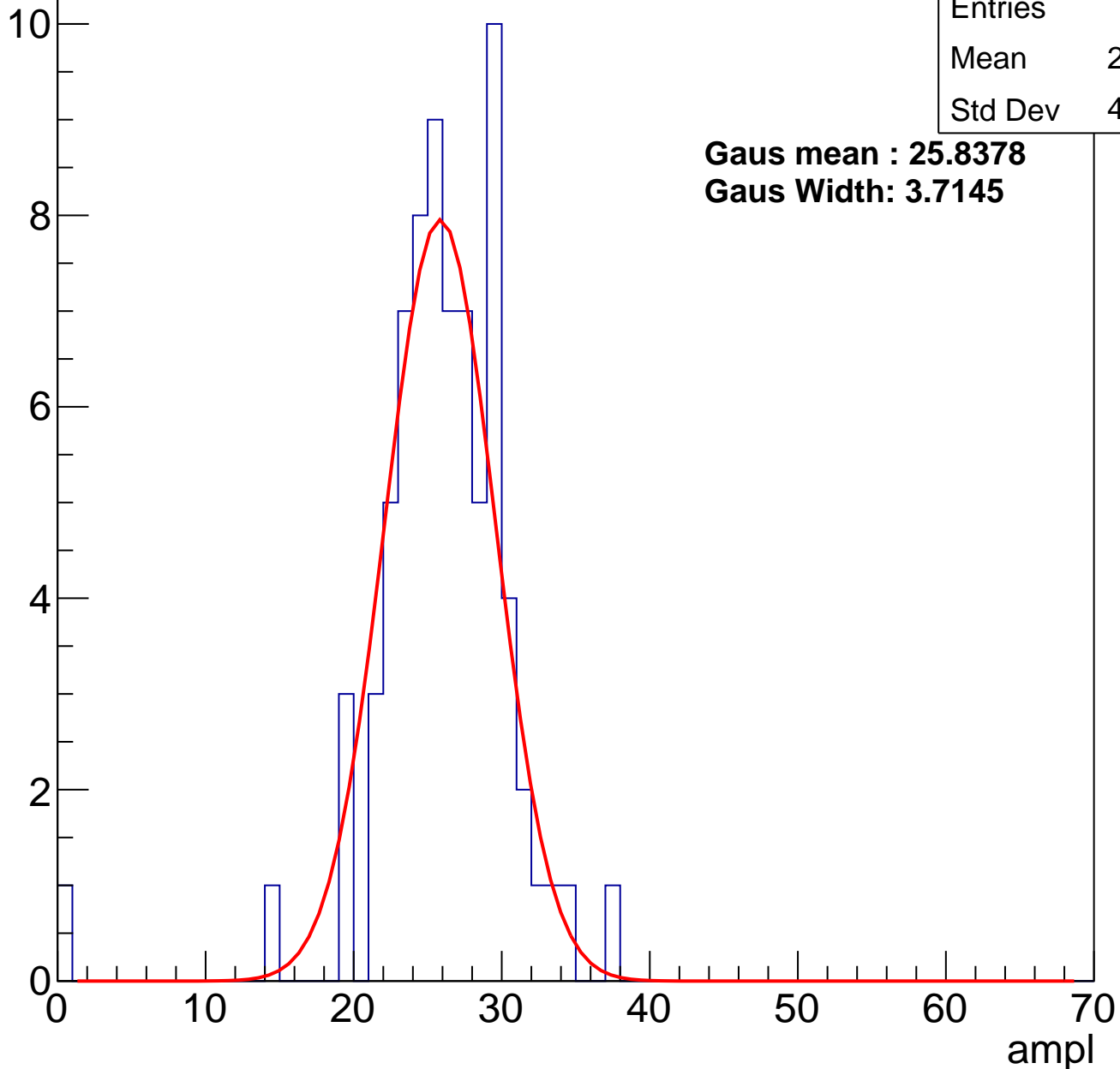
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	76
Mean	25.54
Std Dev	4.745

**Gaus mean : 25.8378**

**Gaus Width: 3.7145**

Entry



# B1L103S, U1-ch84, adc1

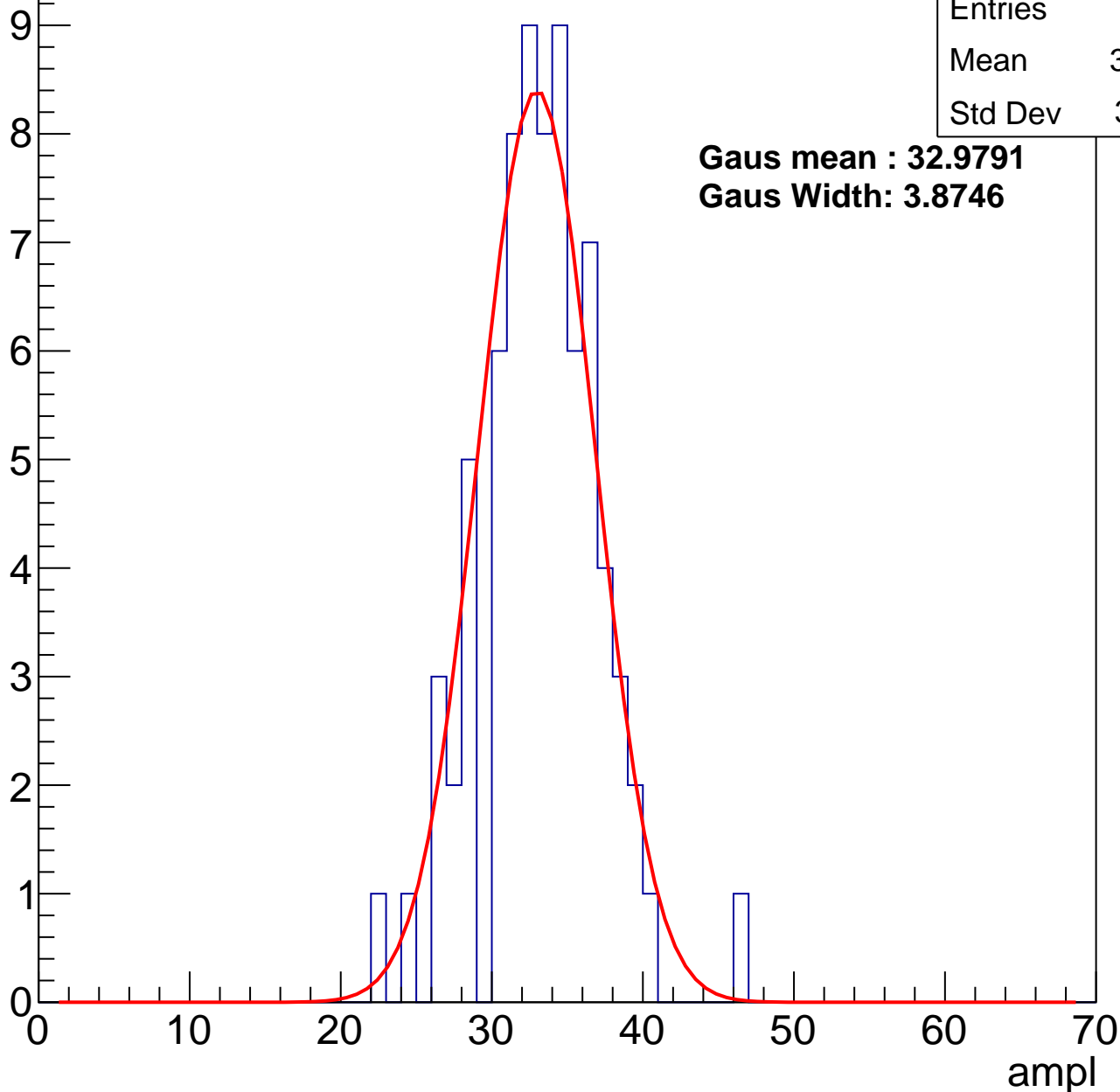
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	32.79
Std Dev	3.911

**Gaus mean : 32.9791**

**Gaus Width: 3.8746**



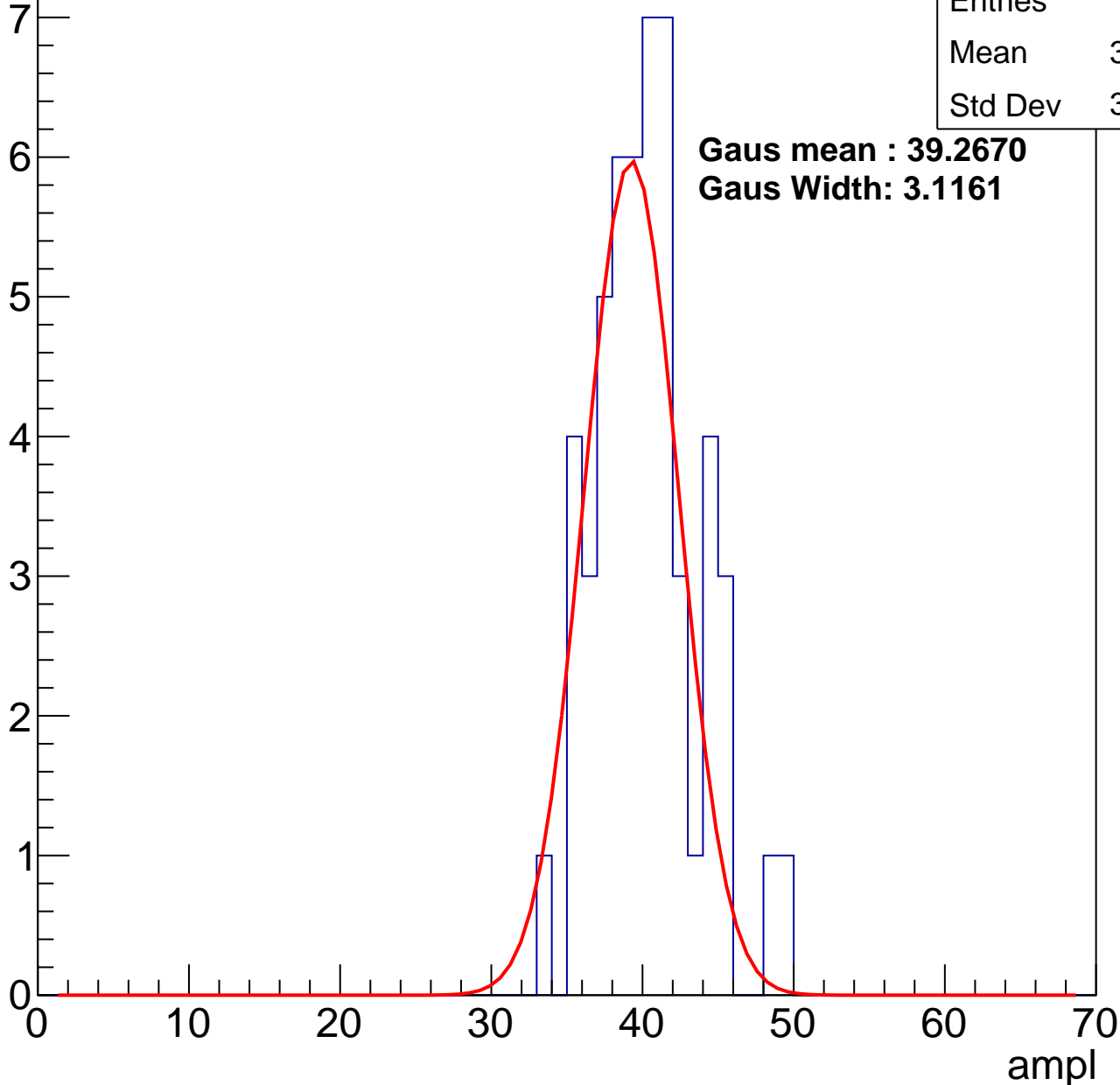
# B1L103S, U1-ch84, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	39.85
Std Dev	3.348

**Gaus mean : 39.2670**  
**Gaus Width: 3.1161**

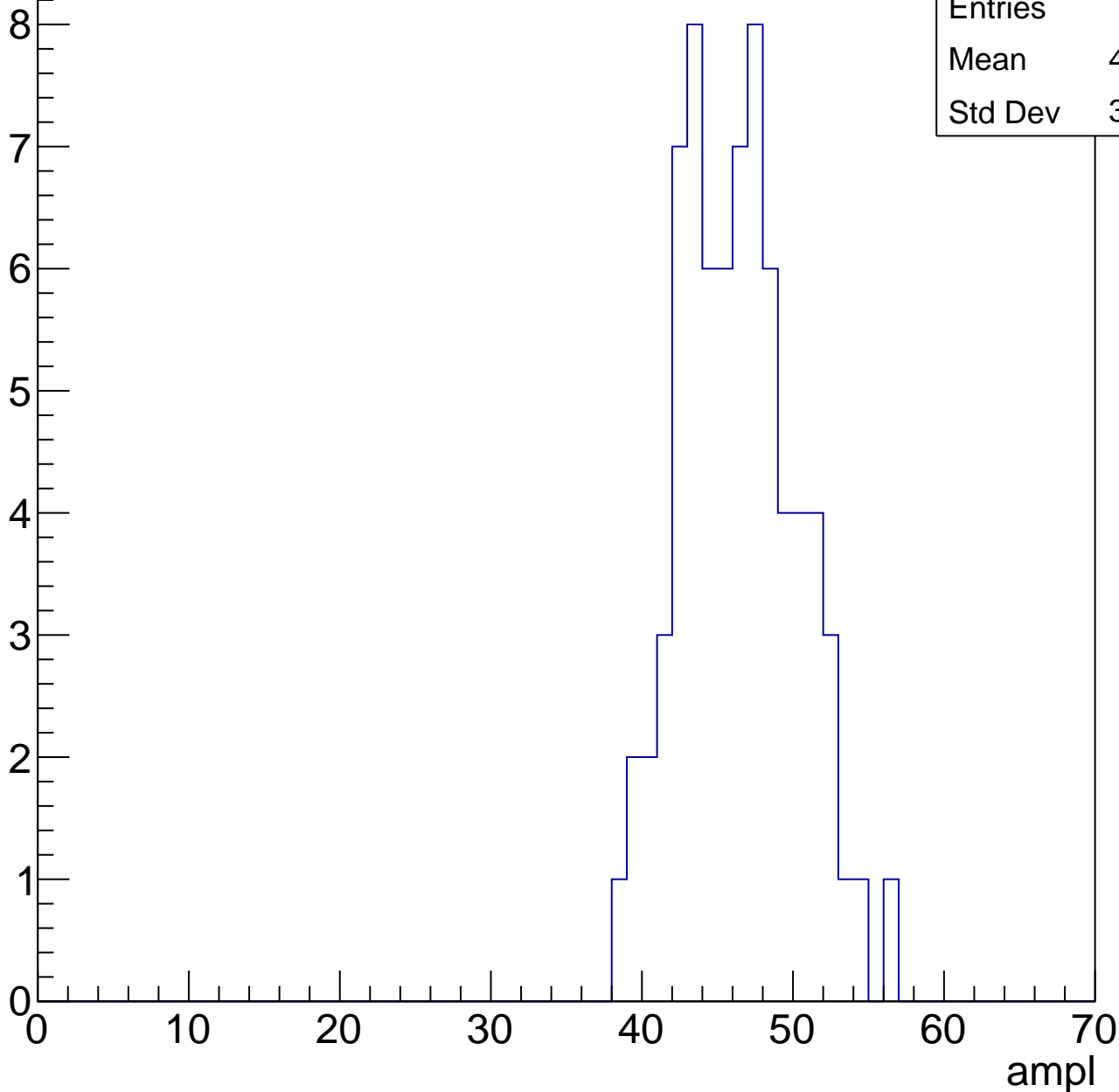


# B1L103S, U1-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	45.89
Std Dev	3.812

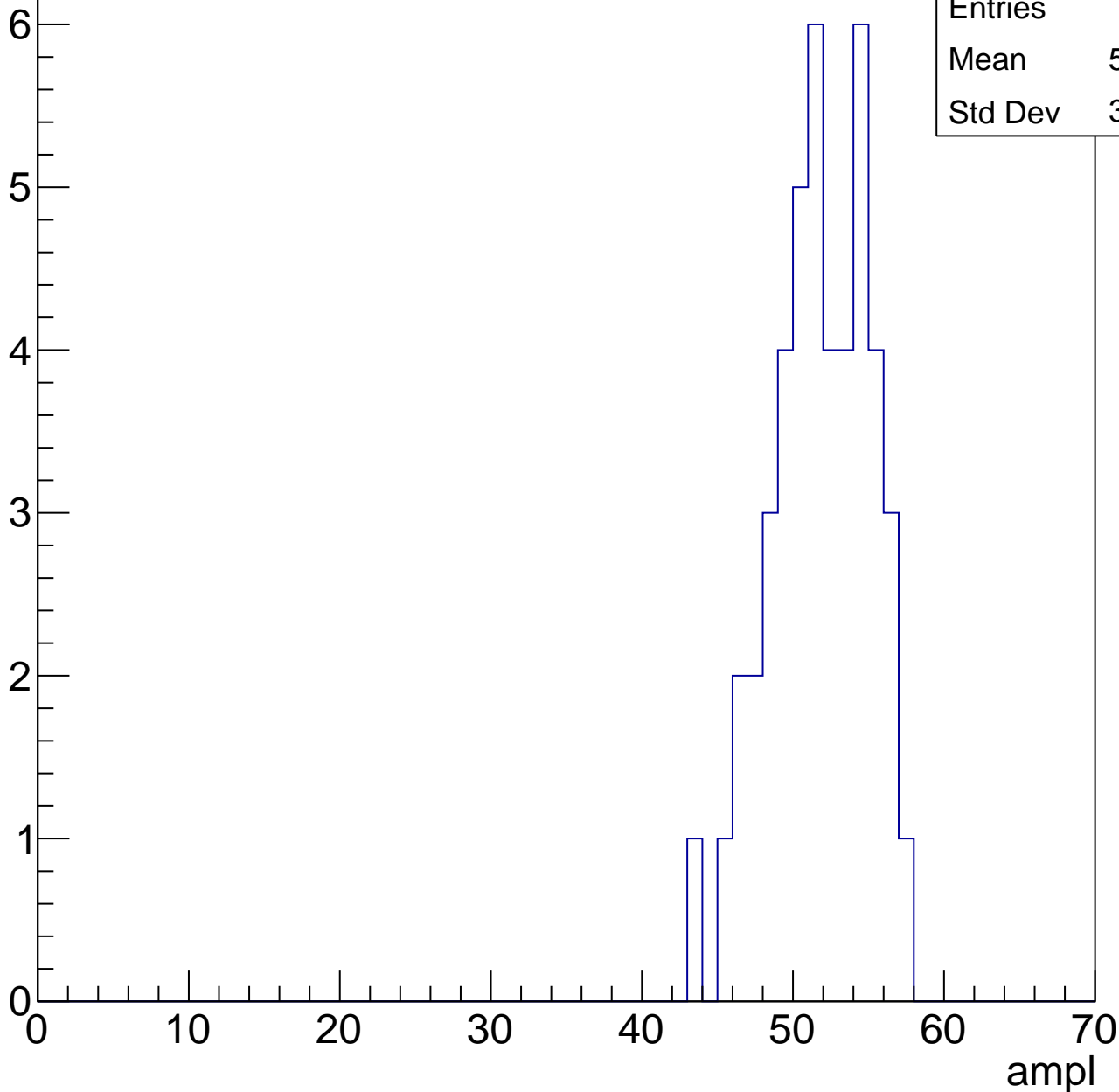


# B1L103S, U1-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

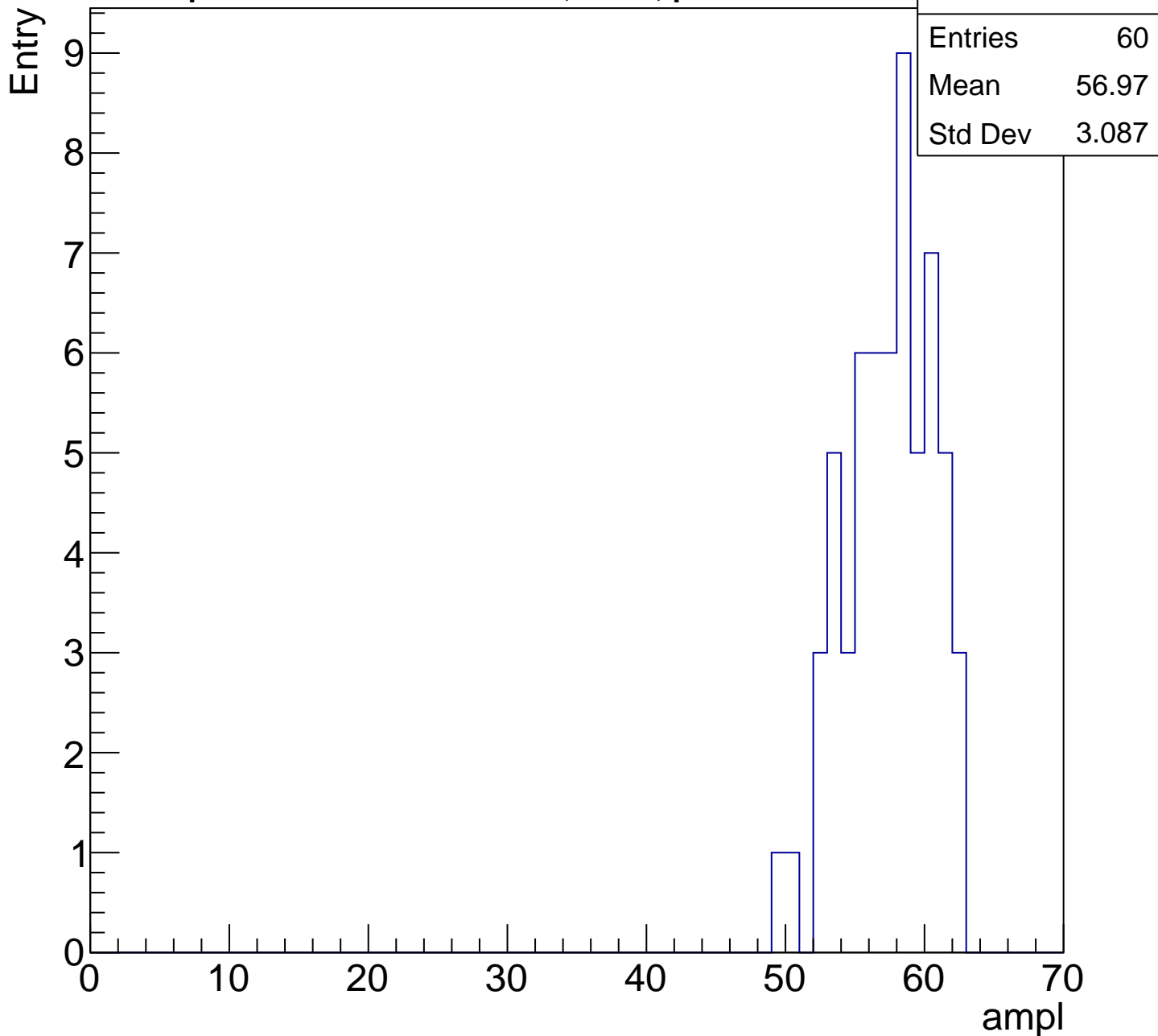
Entry

Entries	46
Mean	51.28
Std Dev	3.215



# B1L103S, U1-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

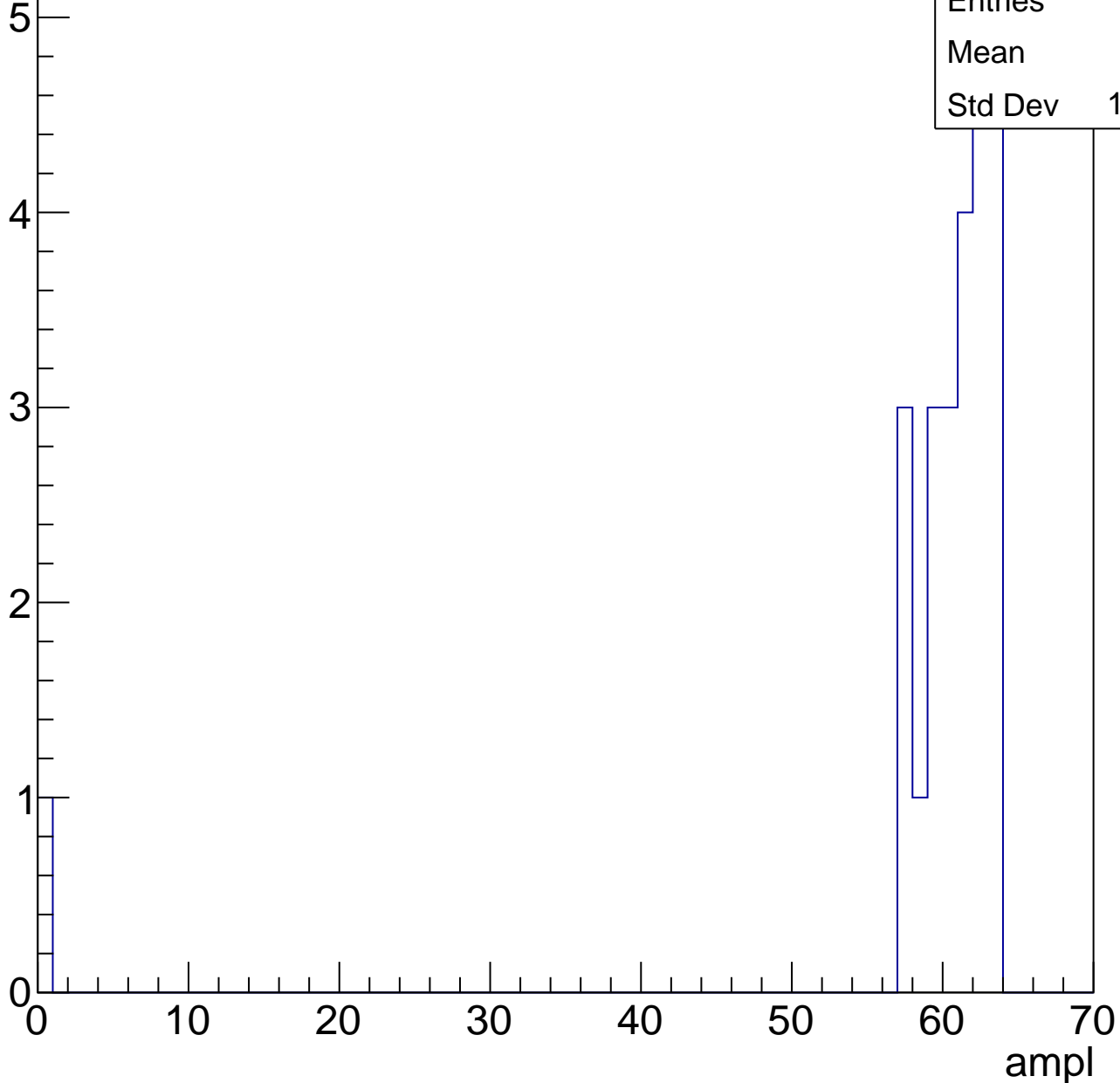


# B1L103S, U1-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	25
Mean	58.2
Std Dev	12.04



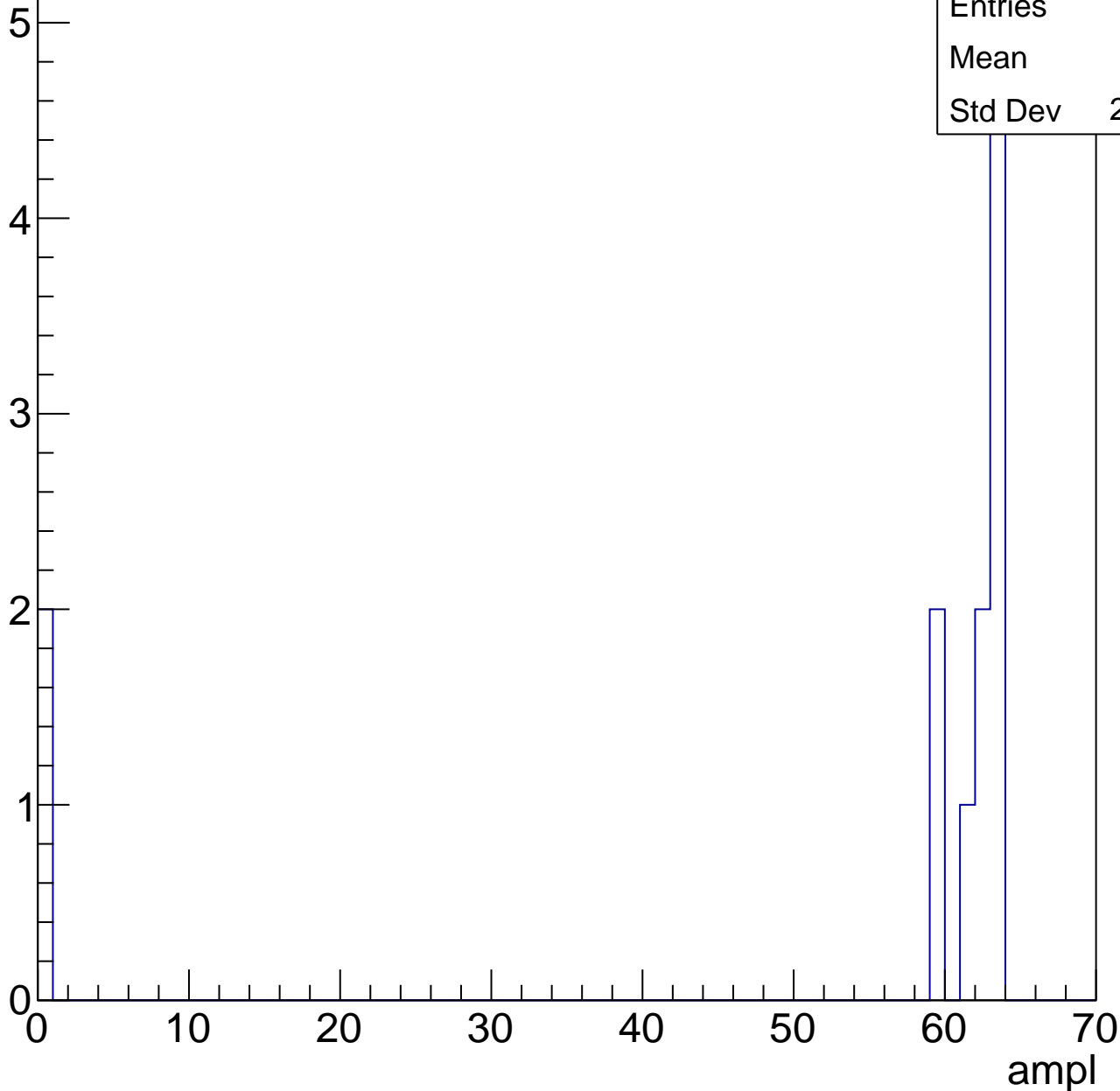


# B1L103S, U1-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	12
Mean	51.5
Std Dev	23.07



# B1L103S, U1-ch85, adc0

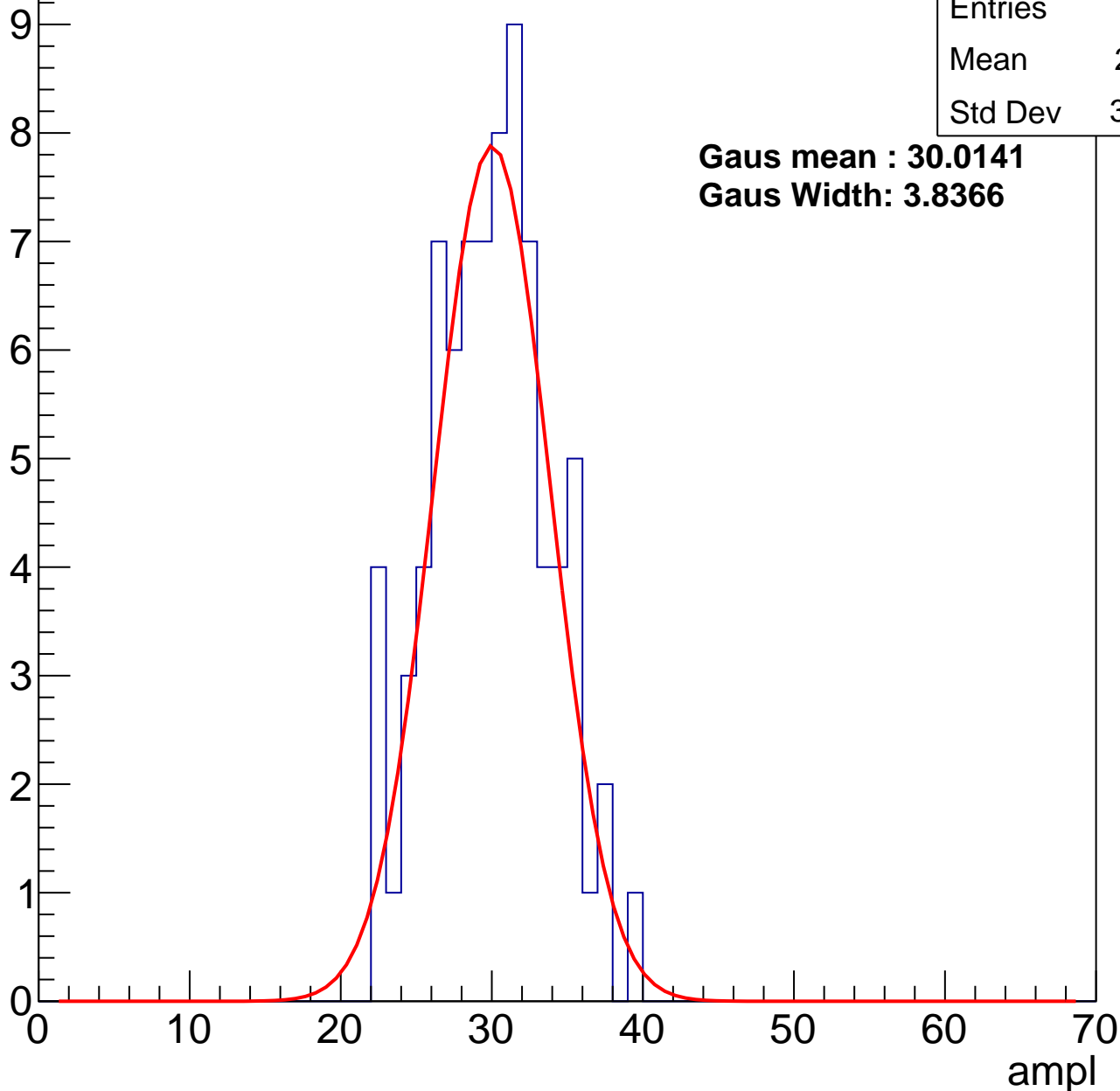
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	29.51
Std Dev	3.828

**Gaus mean : 30.0141**

**Gaus Width: 3.8366**



# B1L103S, U1-ch85, adc1

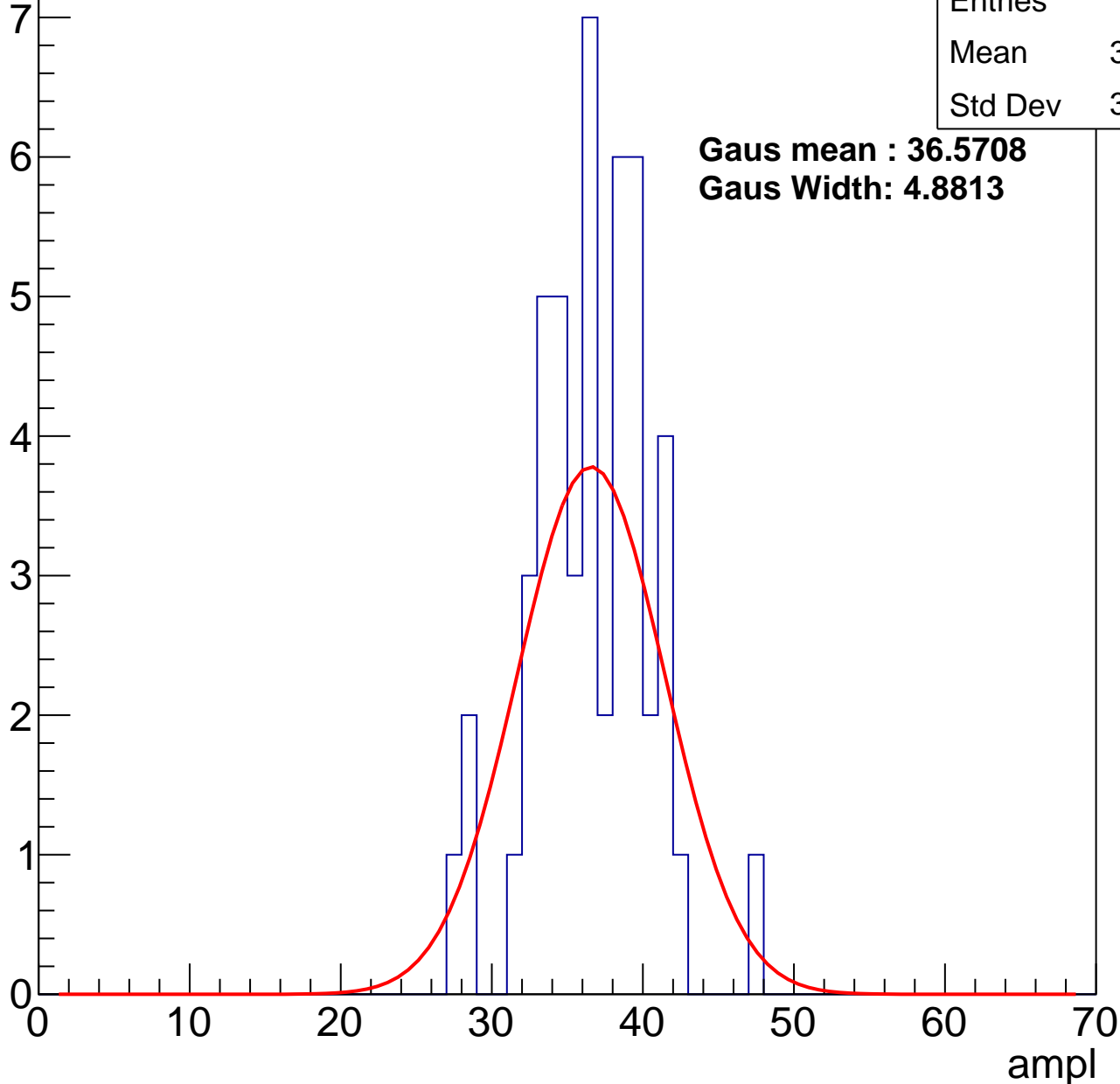
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	36.14
Std Dev	3.828

**Gaus mean : 36.5708**

**Gaus Width: 4.8813**



# B1L103S, U1-ch85, adc2

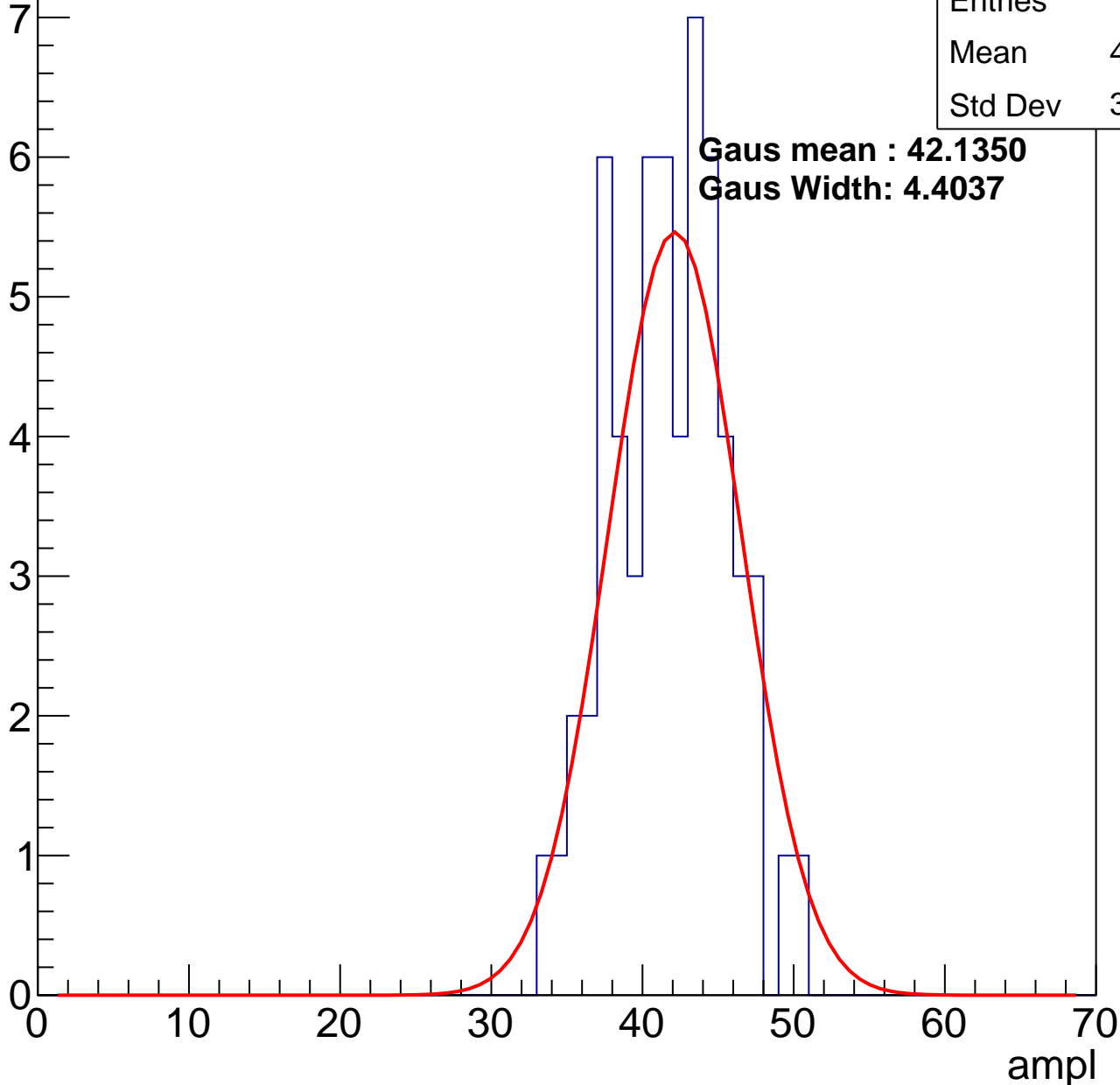
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	41.28
Std Dev	3.782

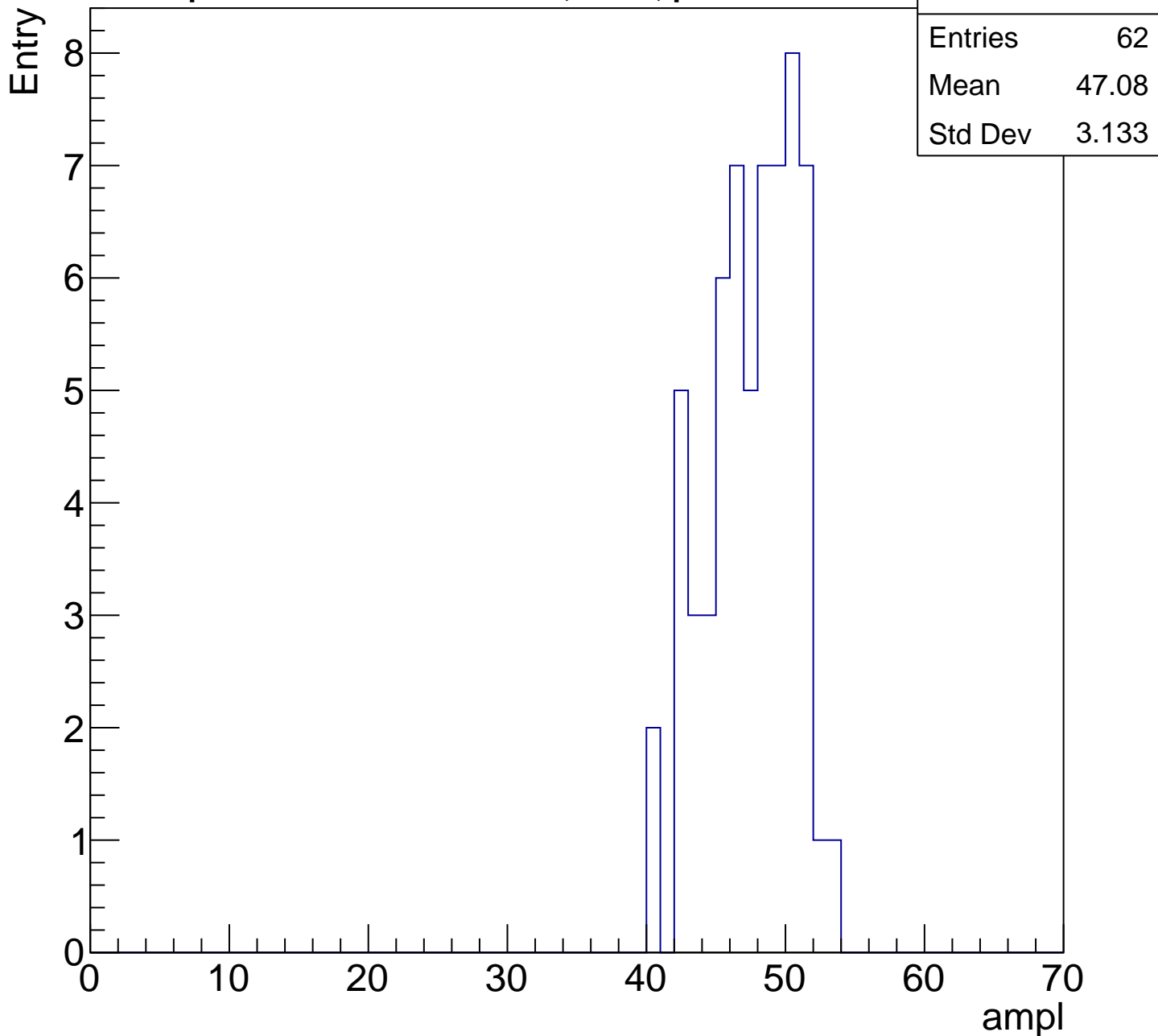
**Gaus mean : 42.1350**

**Gaus Width: 4.4037**



# B1L103S, U1-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

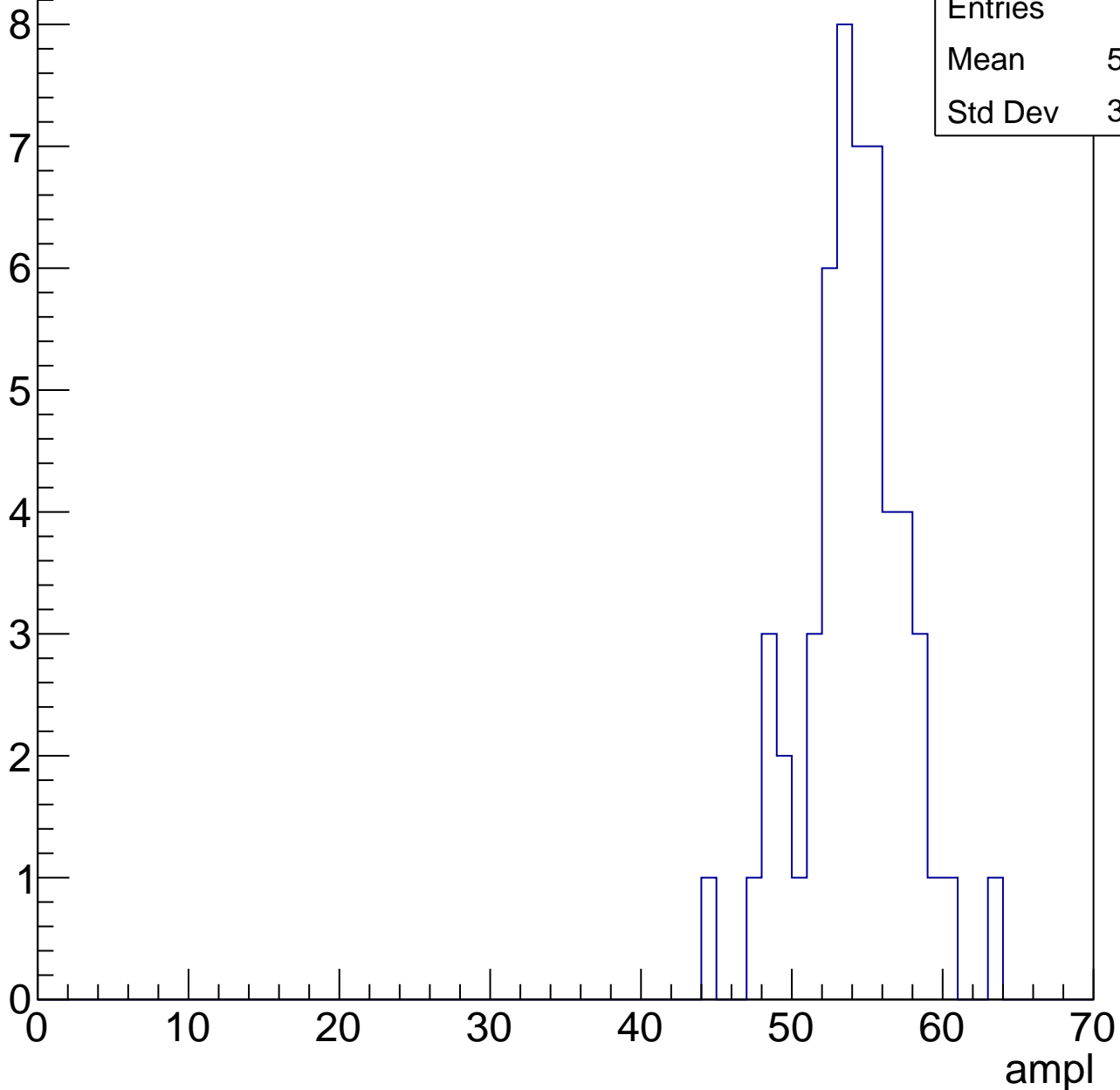


# B1L103S, U1-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

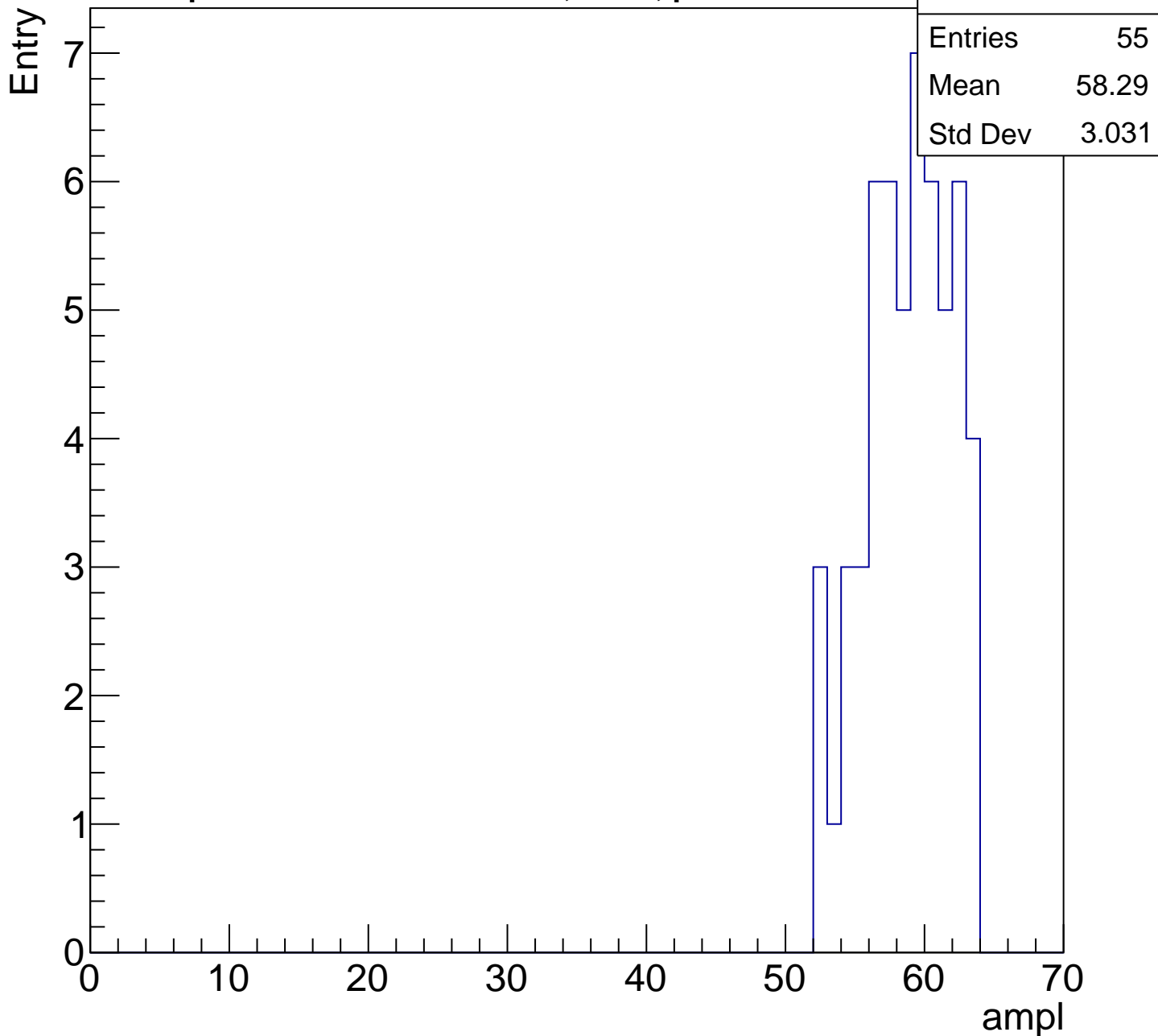
Entry

Entries	53
Mean	53.64
Std Dev	3.432



# B1L103S, U1-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

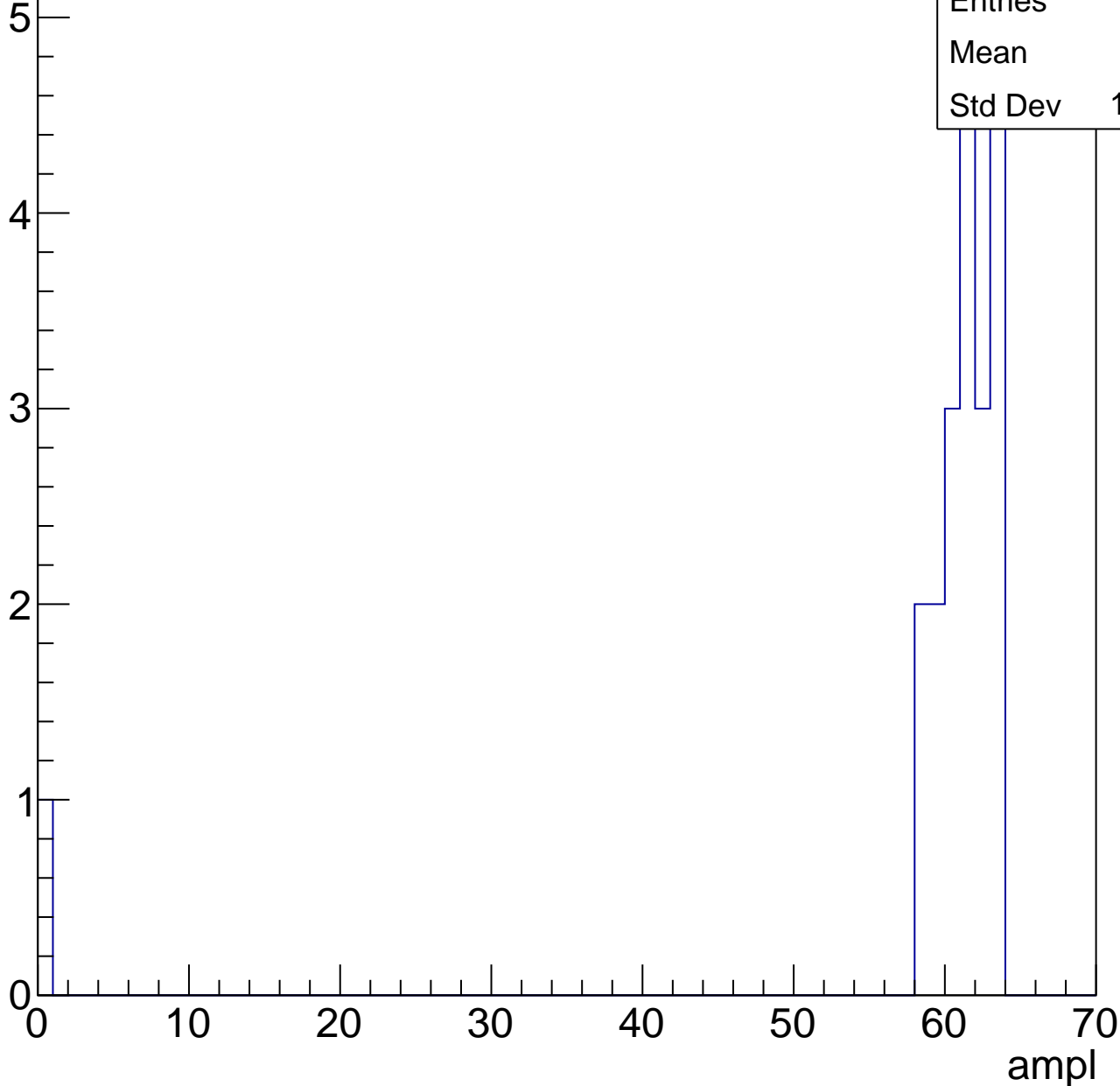


# B1L103S, U1-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	21
Mean	58.1
Std Dev	13.09

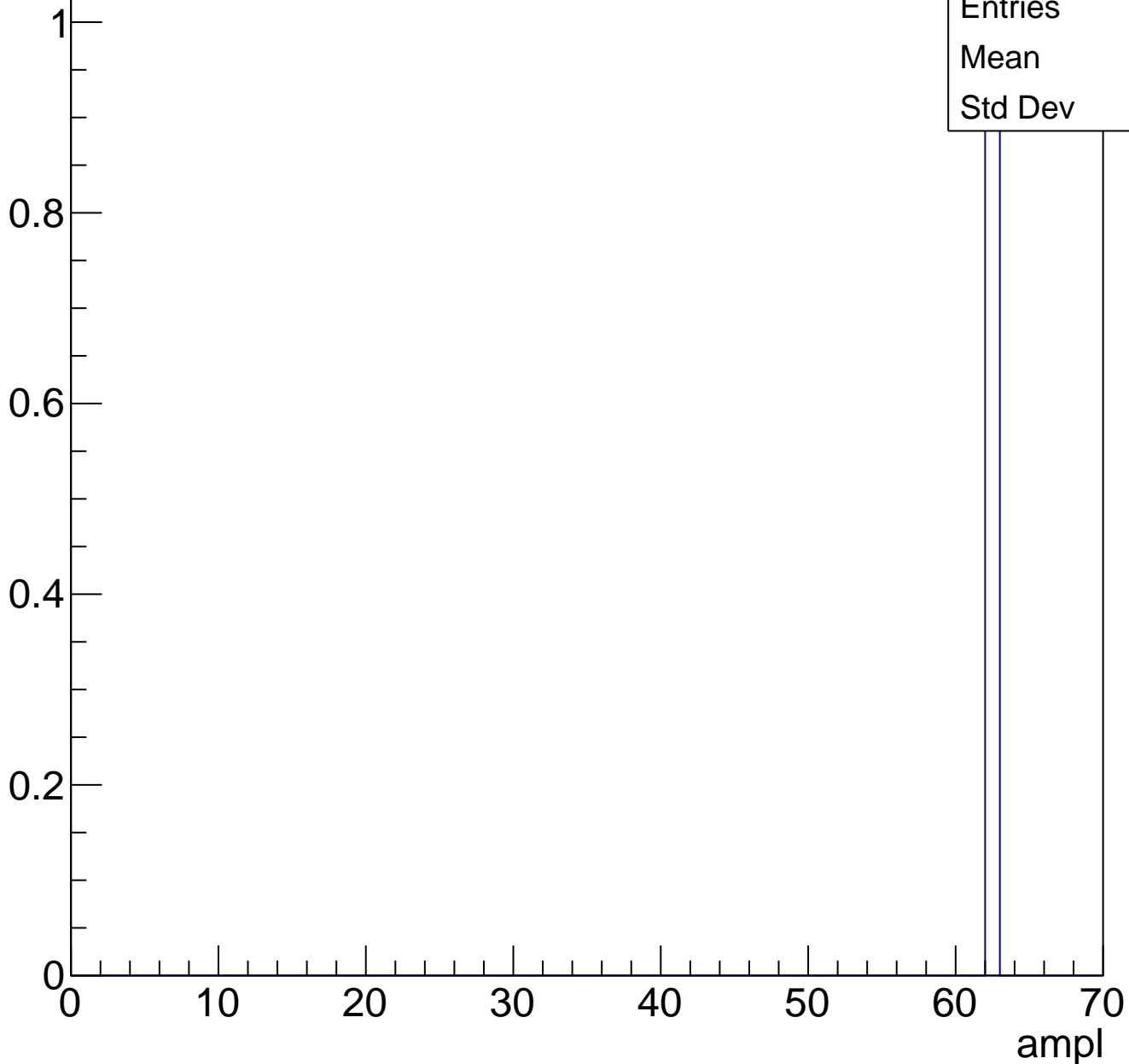




# B1L103S, U1-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch86, adc0

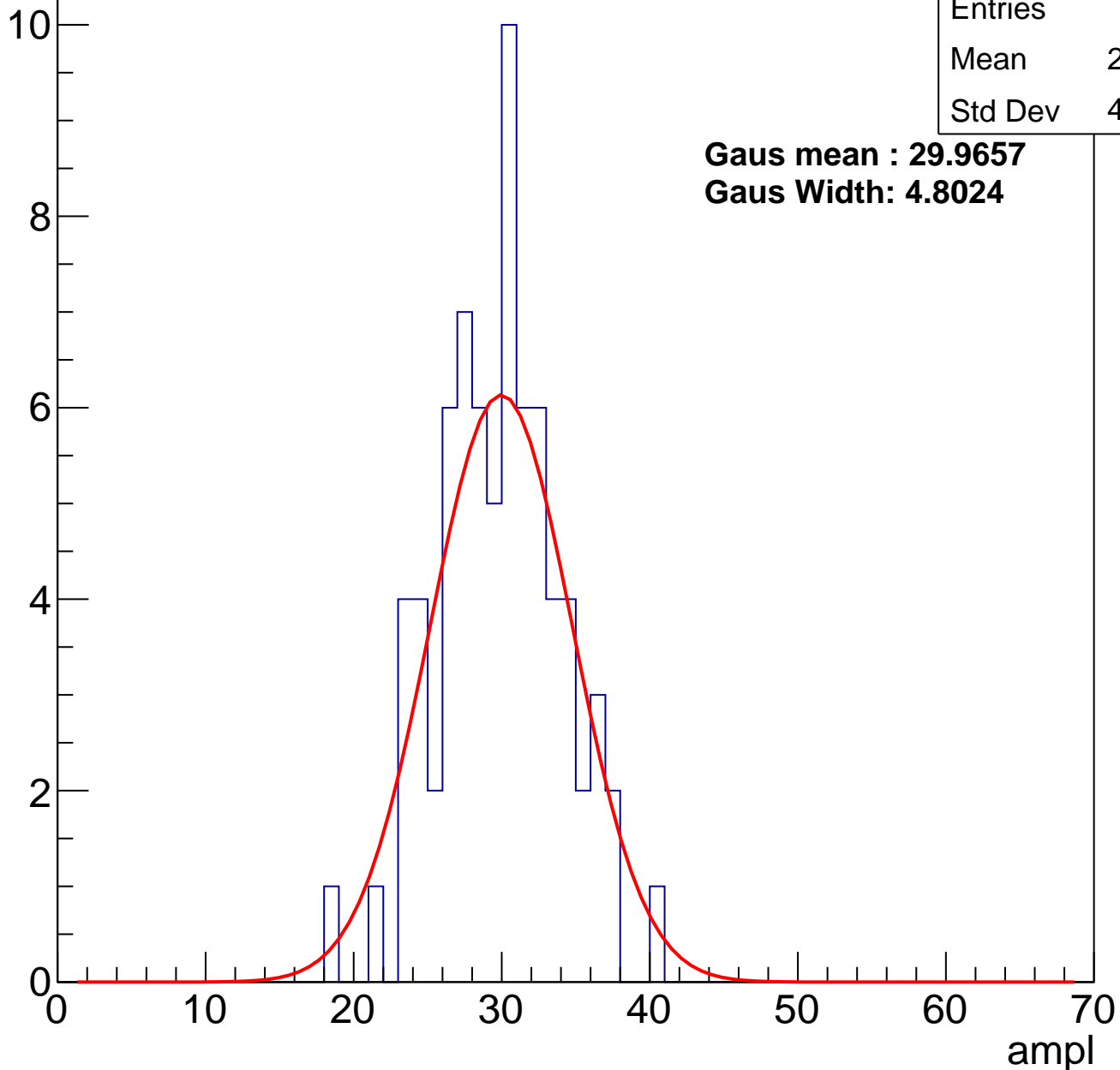
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	74
Mean	29.36
Std Dev	4.125

**Gaus mean : 29.9657**

**Gaus Width: 4.8024**

Entry



# B1L103S, U1-ch86, adc1

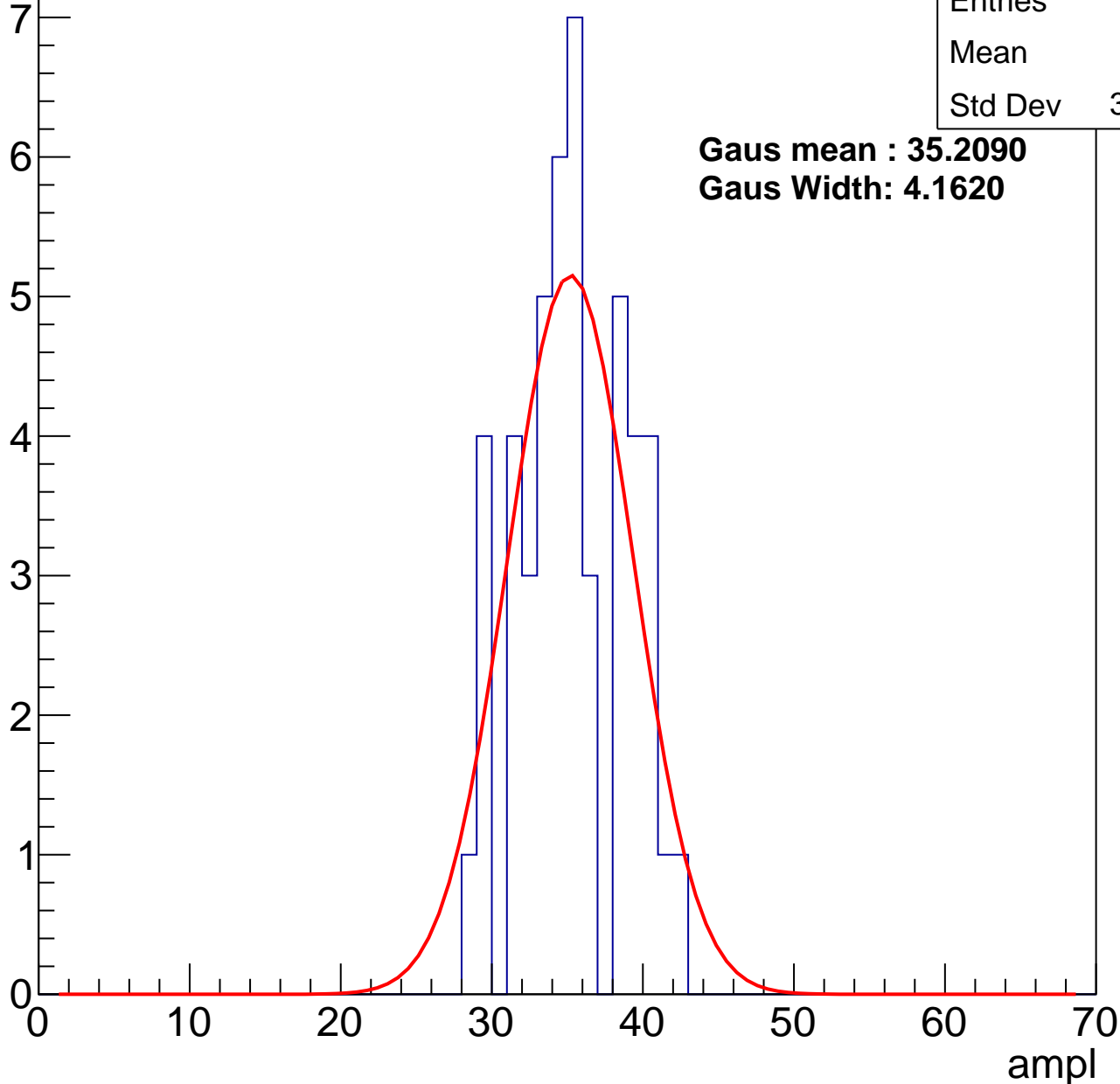
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	34.9
Std Dev	3.555

**Gaus mean : 35.2090**

**Gaus Width: 4.1620**



# B1L103S, U1-ch86, adc2

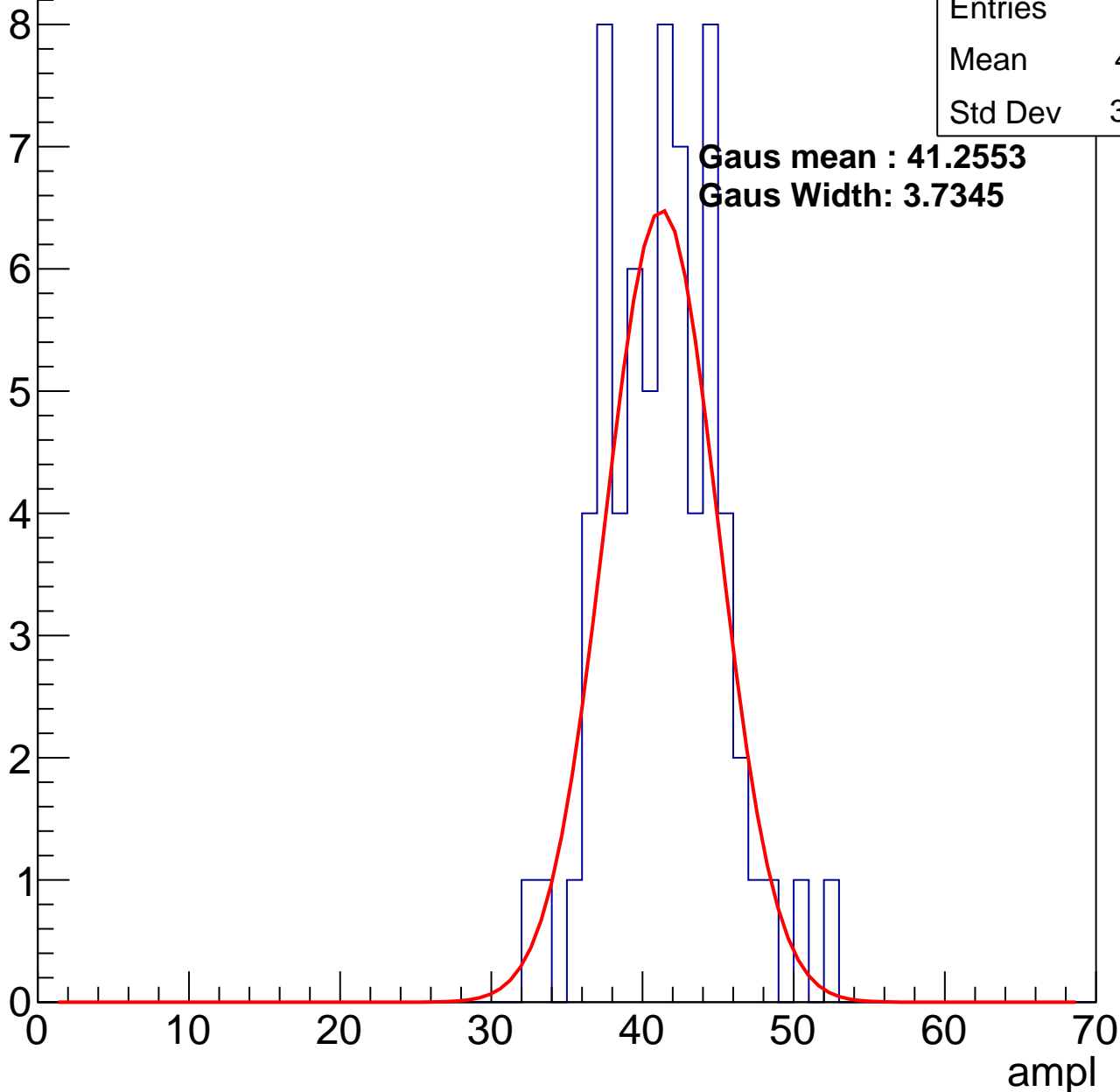
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	40.91
Std Dev	3.804

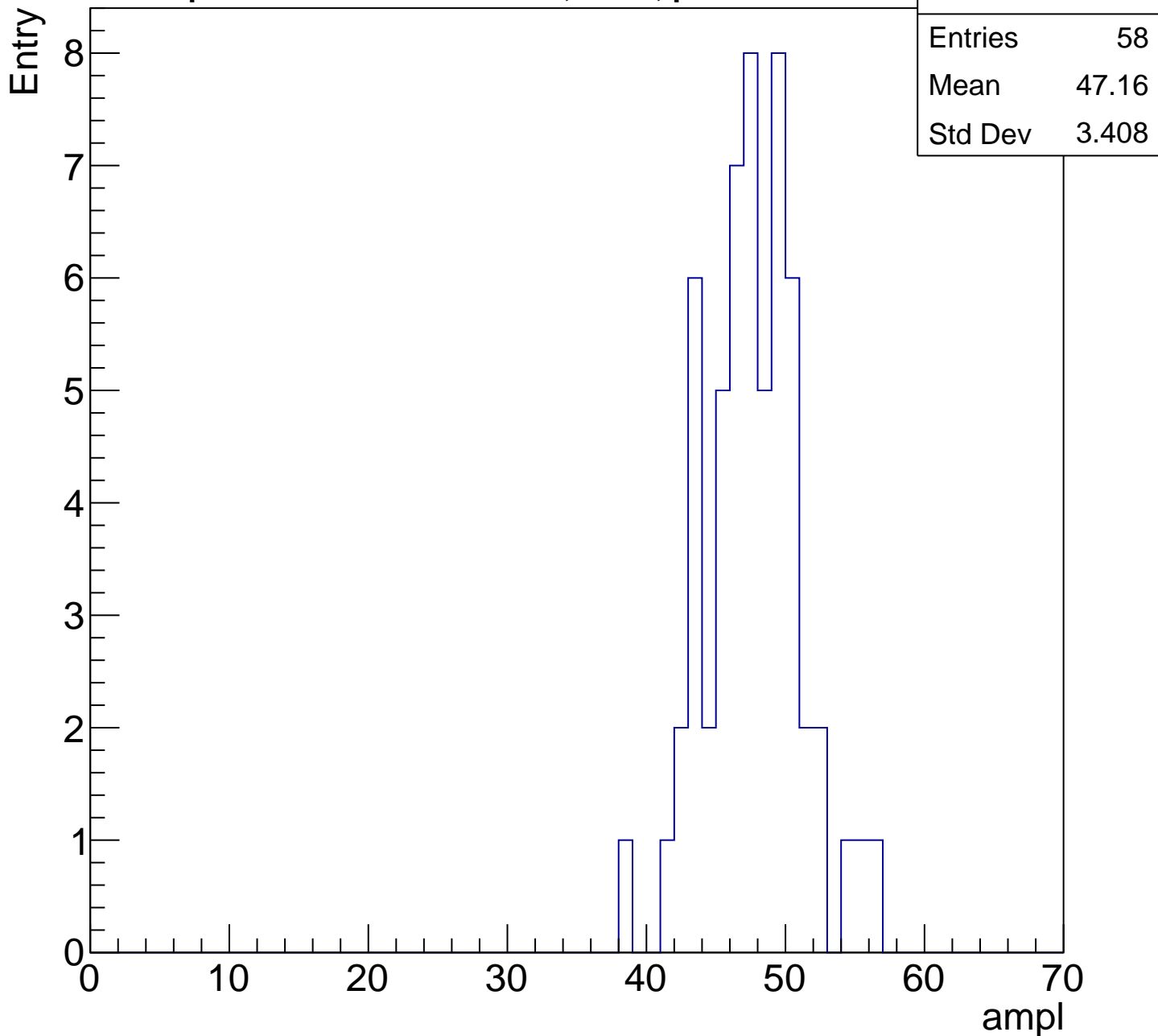
**Gaus mean : 41.2553**

**Gaus Width: 3.7345**



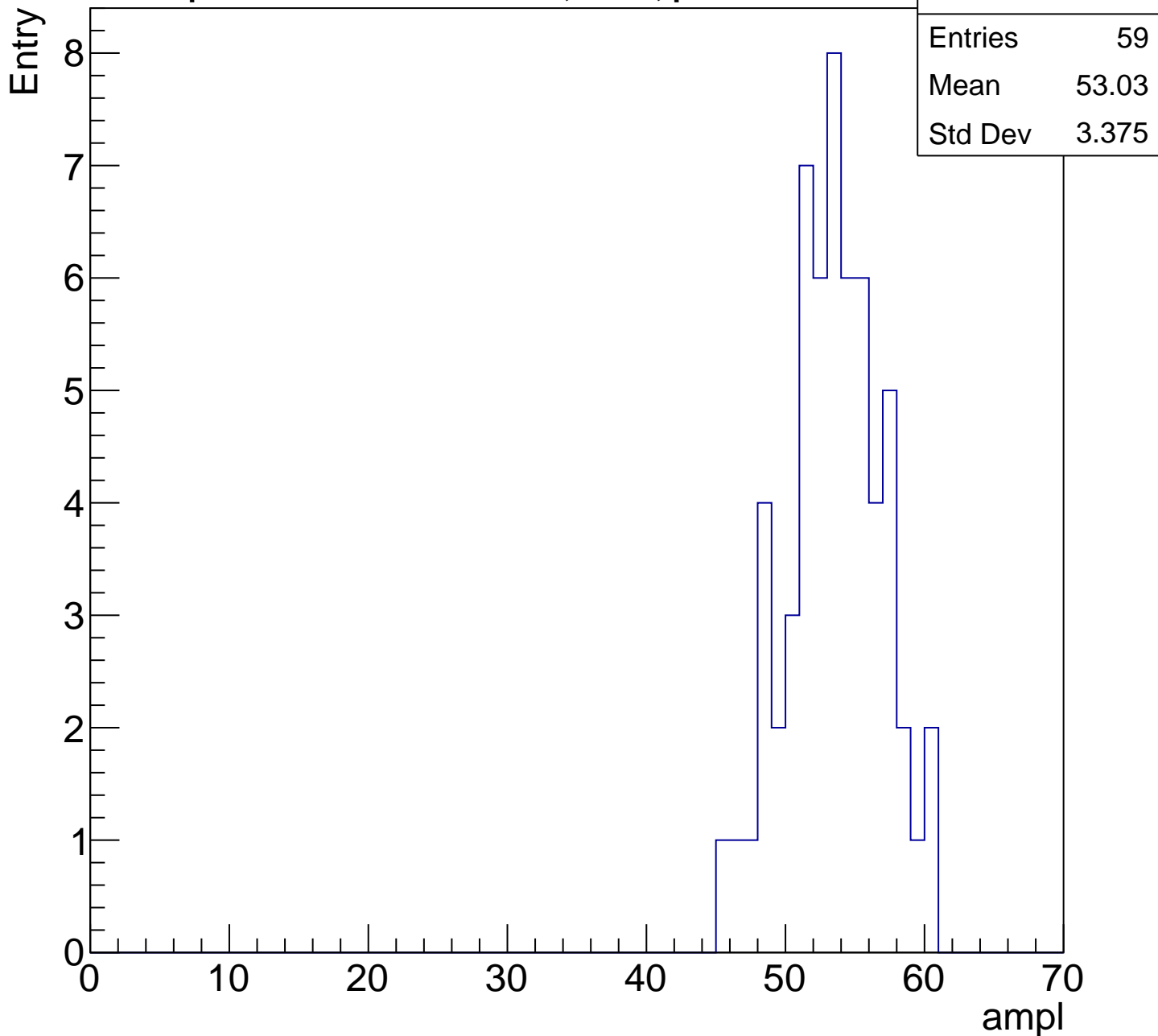
# B1L103S, U1-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U1-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

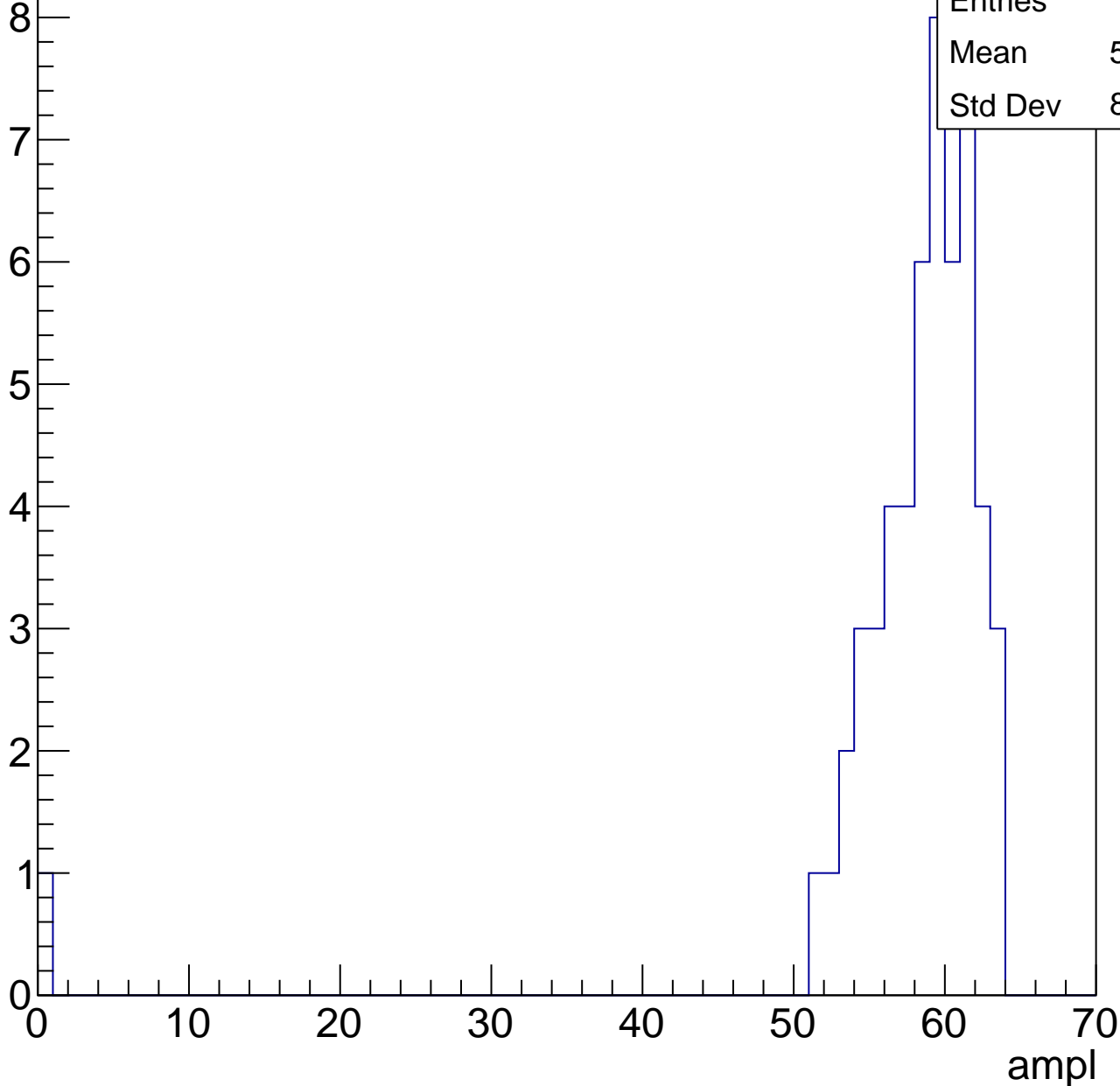


# B1L103S, U1-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	57.28
Std Dev	8.398

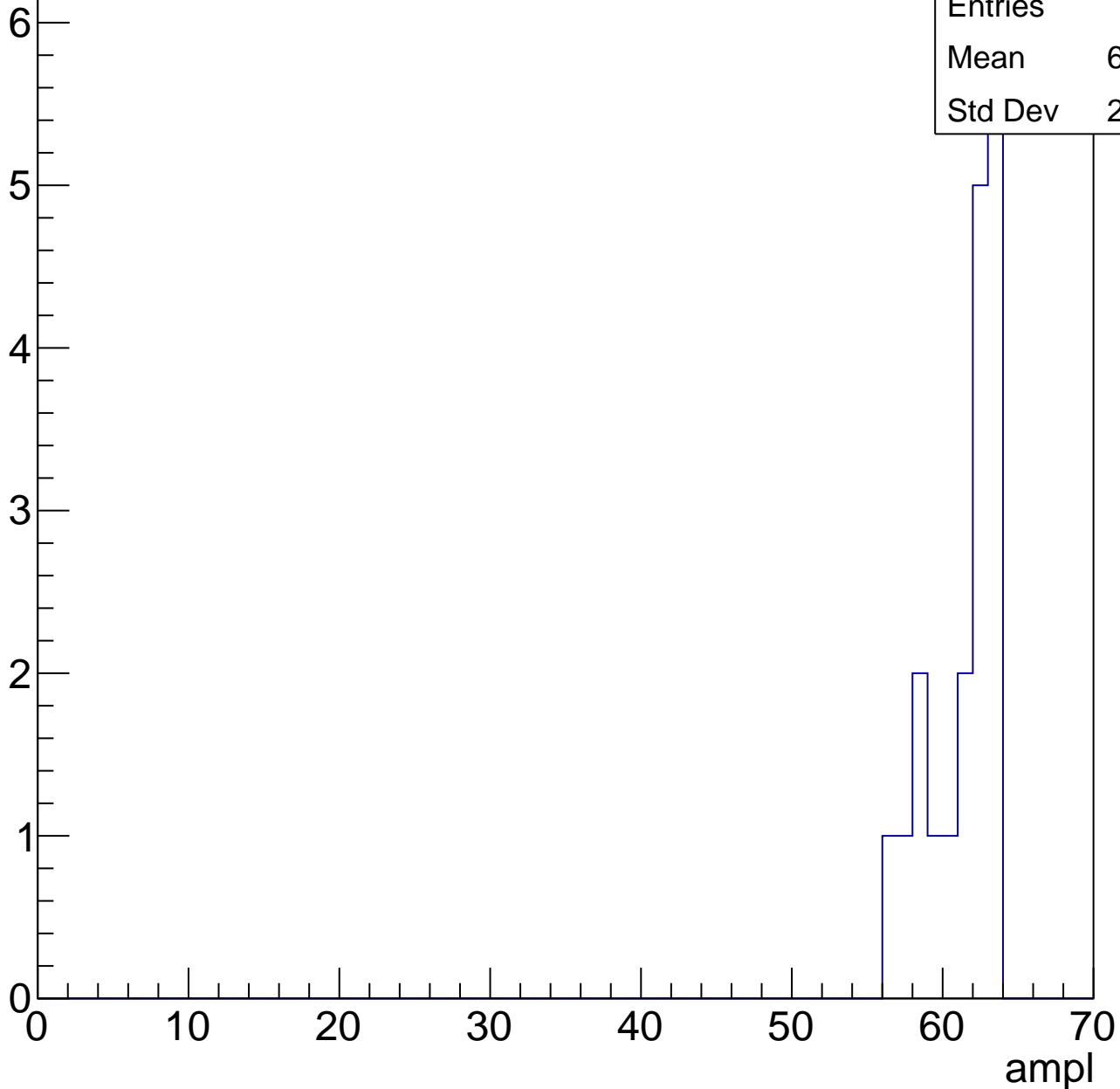


# B1L103S, U1-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	19
Mean	60.95
Std Dev	2.212

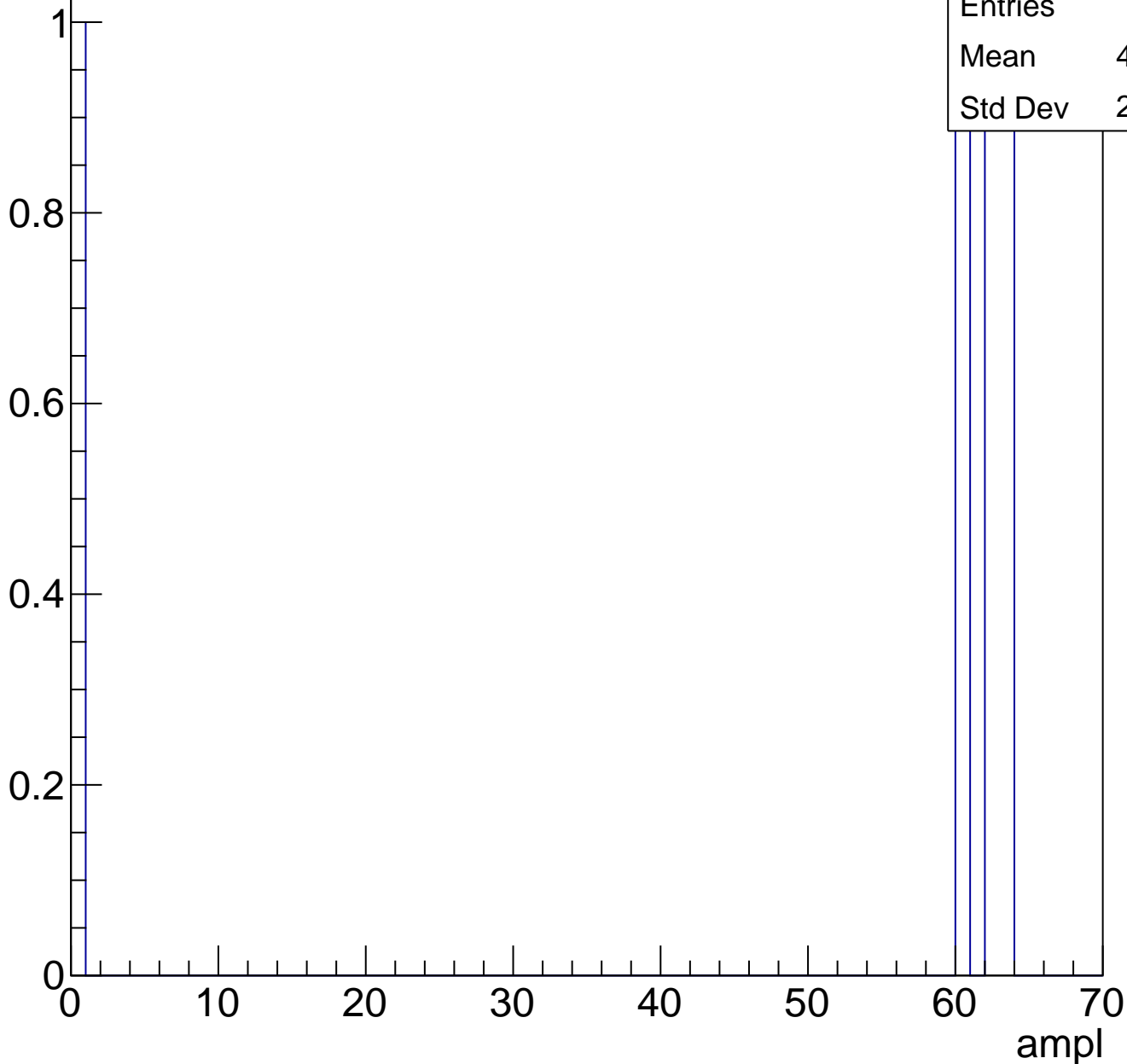




# B1L103S, U1-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch87, adc0

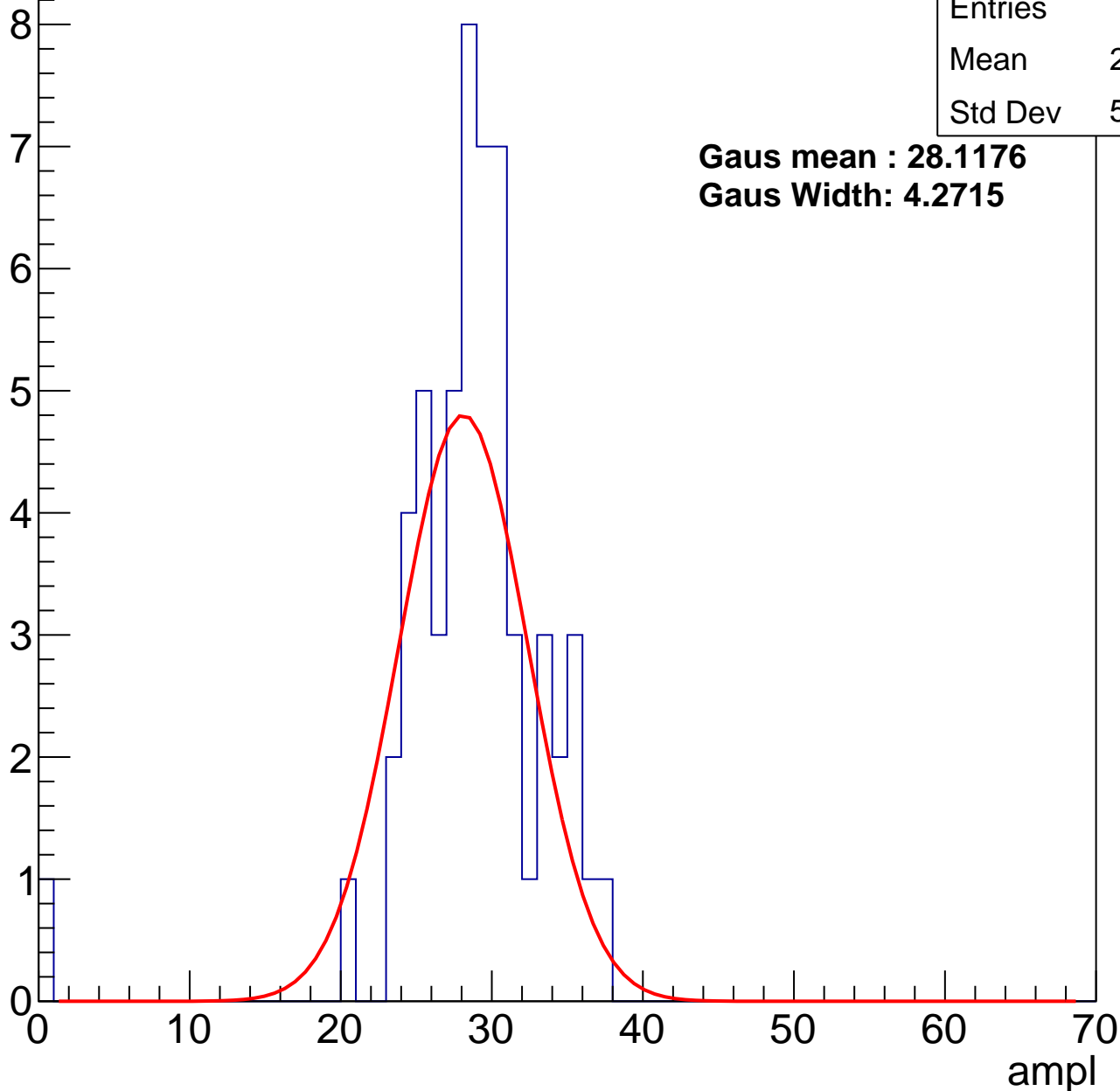
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	28.19
Std Dev	5.196

**Gaus mean : 28.1176**

**Gaus Width: 4.2715**



# B1L103S, U1-ch87, adc1

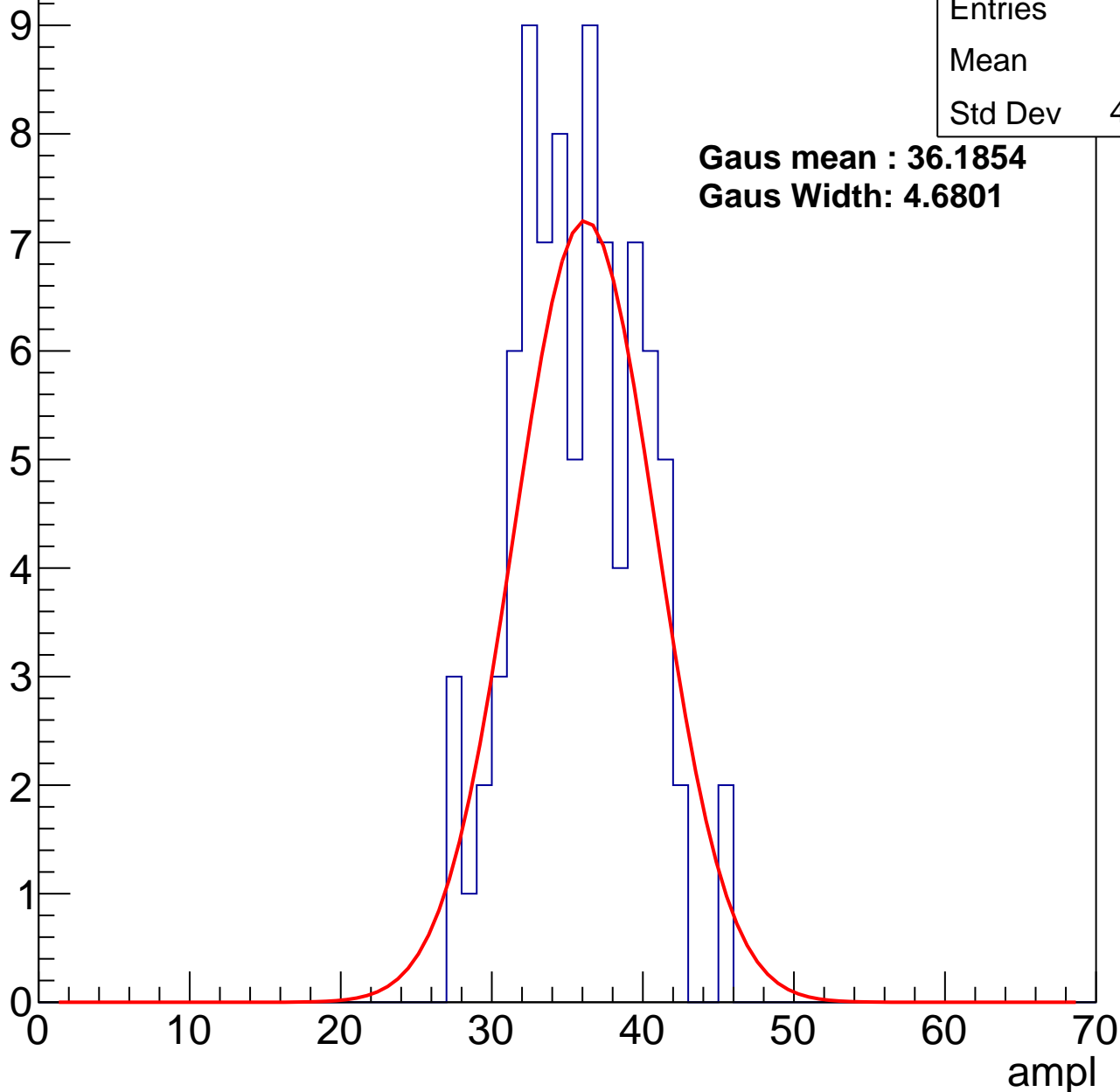
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	86
Mean	35.3
Std Dev	4.044

**Gaus mean : 36.1854**

**Gaus Width: 4.6801**



# B1L103S, U1-ch87, adc2

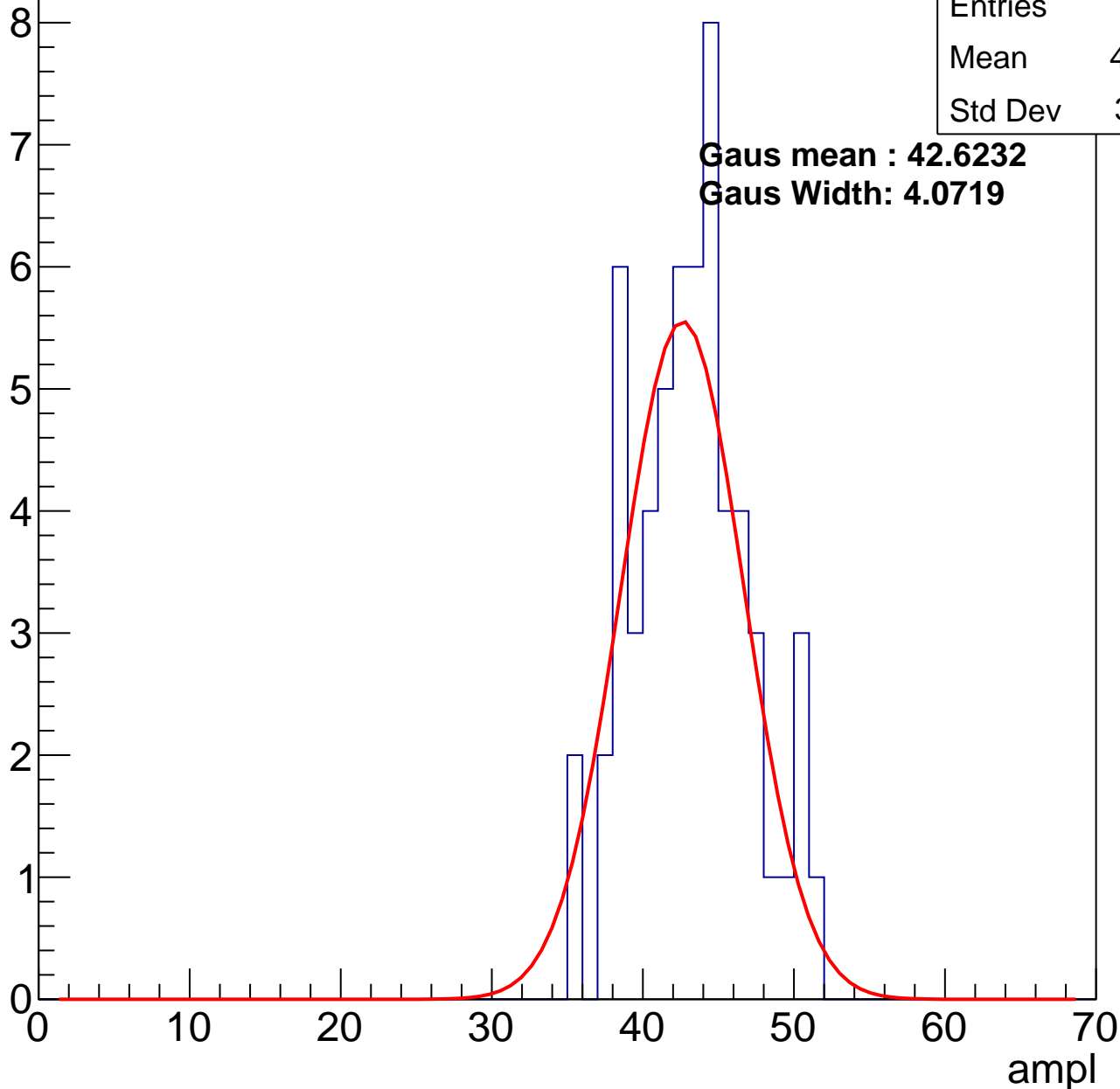
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	42.69
Std Dev	3.761

**Gaus mean : 42.6232**

**Gaus Width: 4.0719**

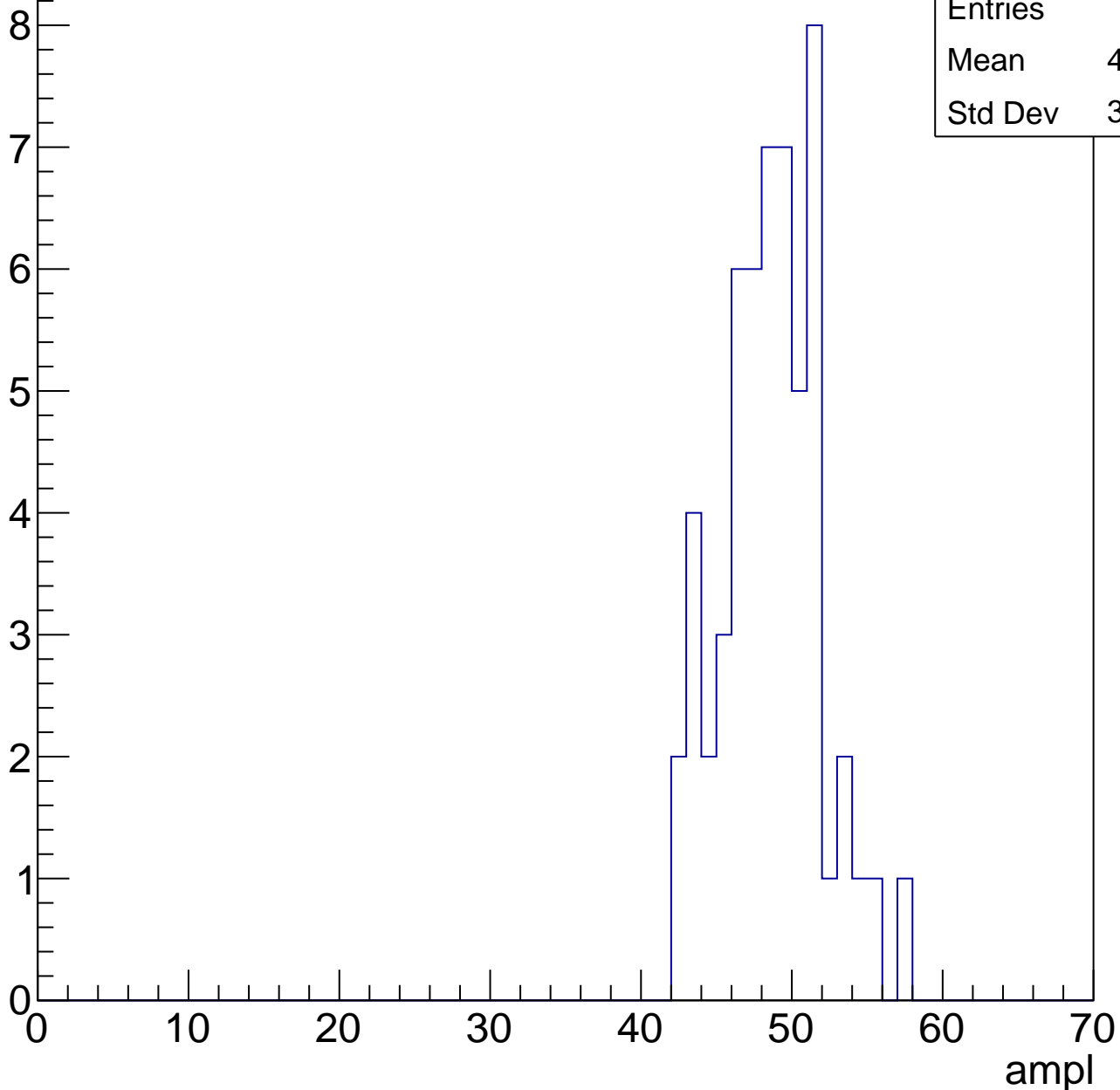


# B1L103S, U1-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

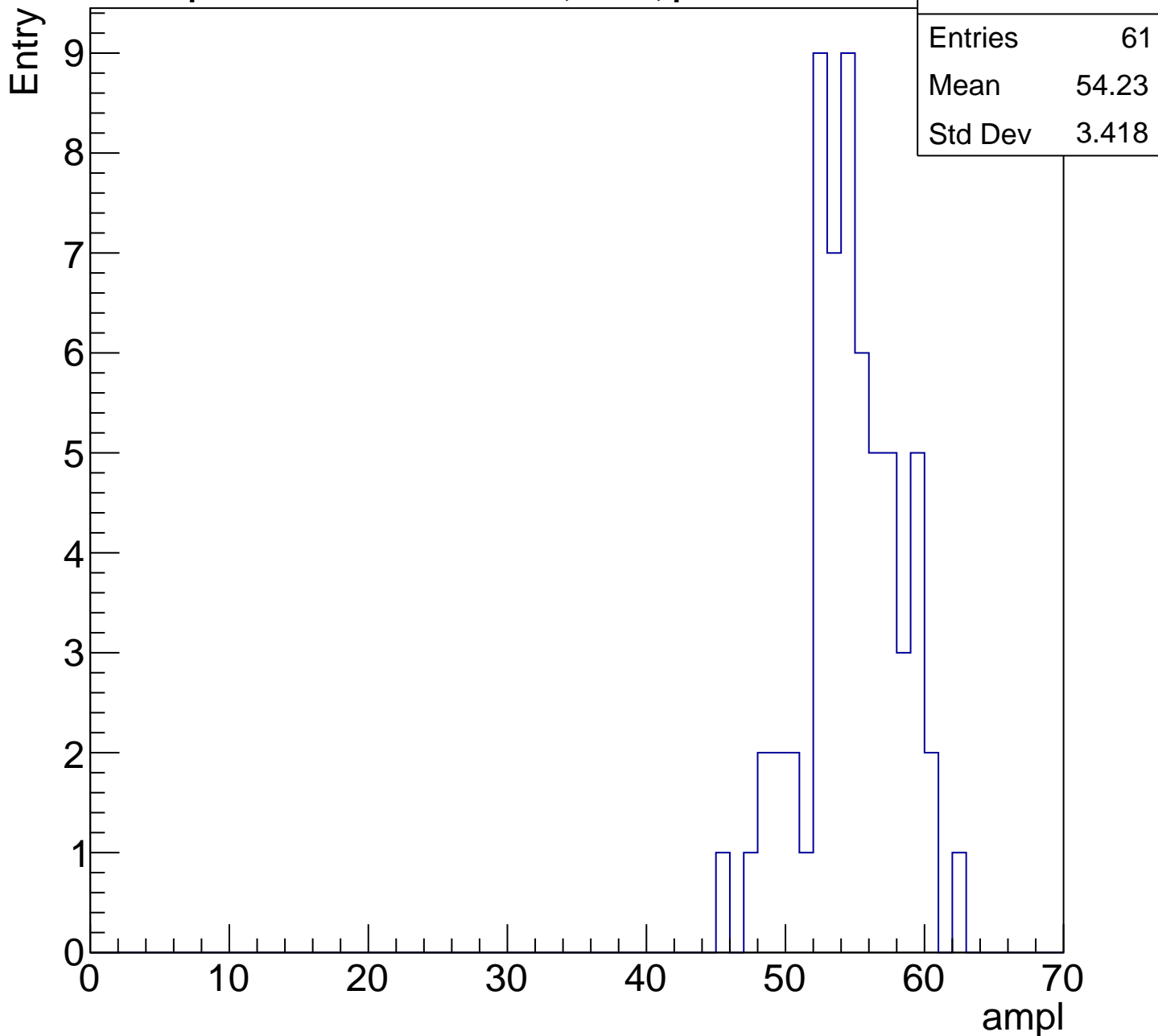
Entry

Entries	56
Mean	48.18
Std Dev	3.246



# B1L103S, U1-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

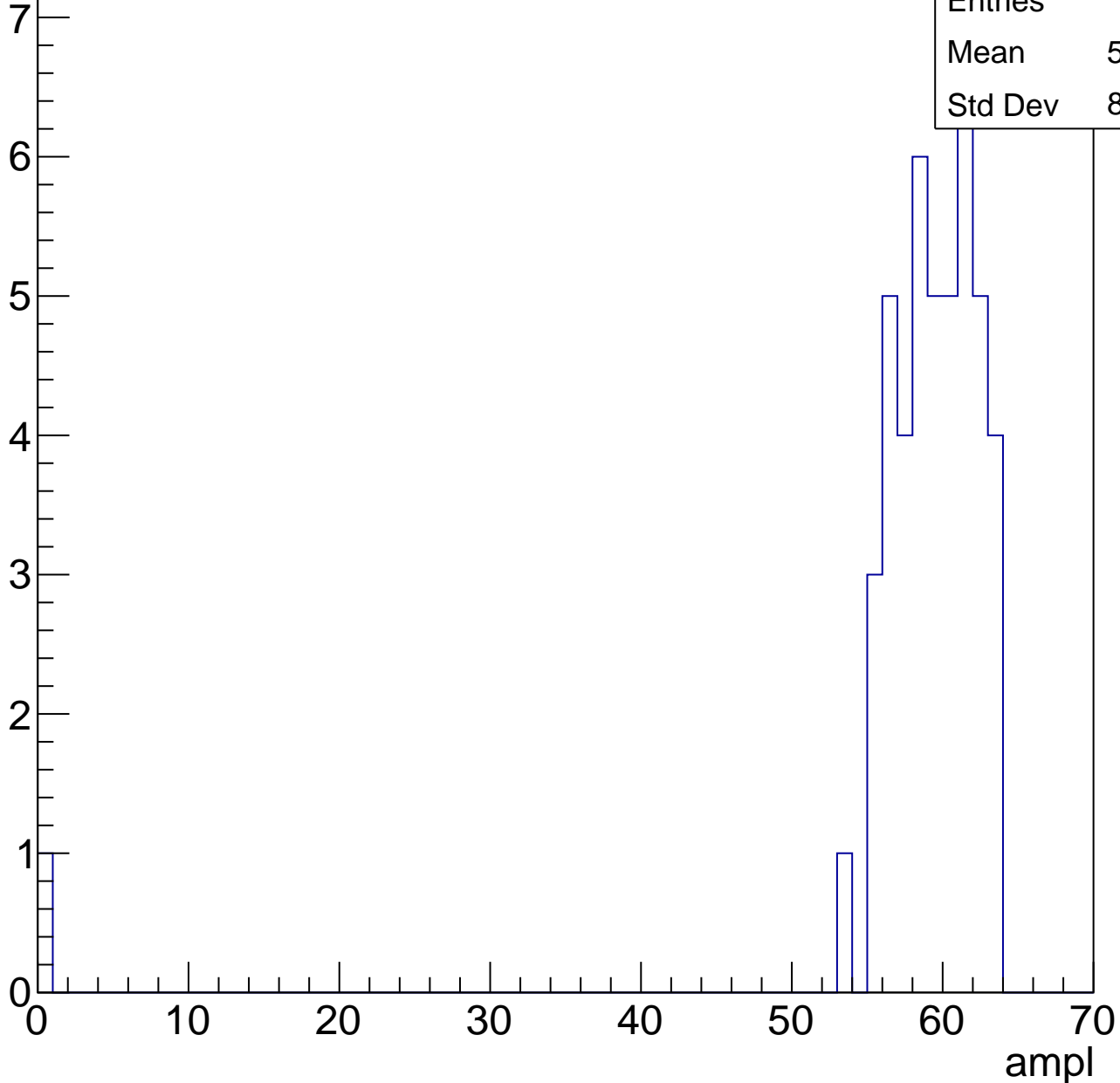


# B1L103S, U1-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	57.78
Std Dev	8.976

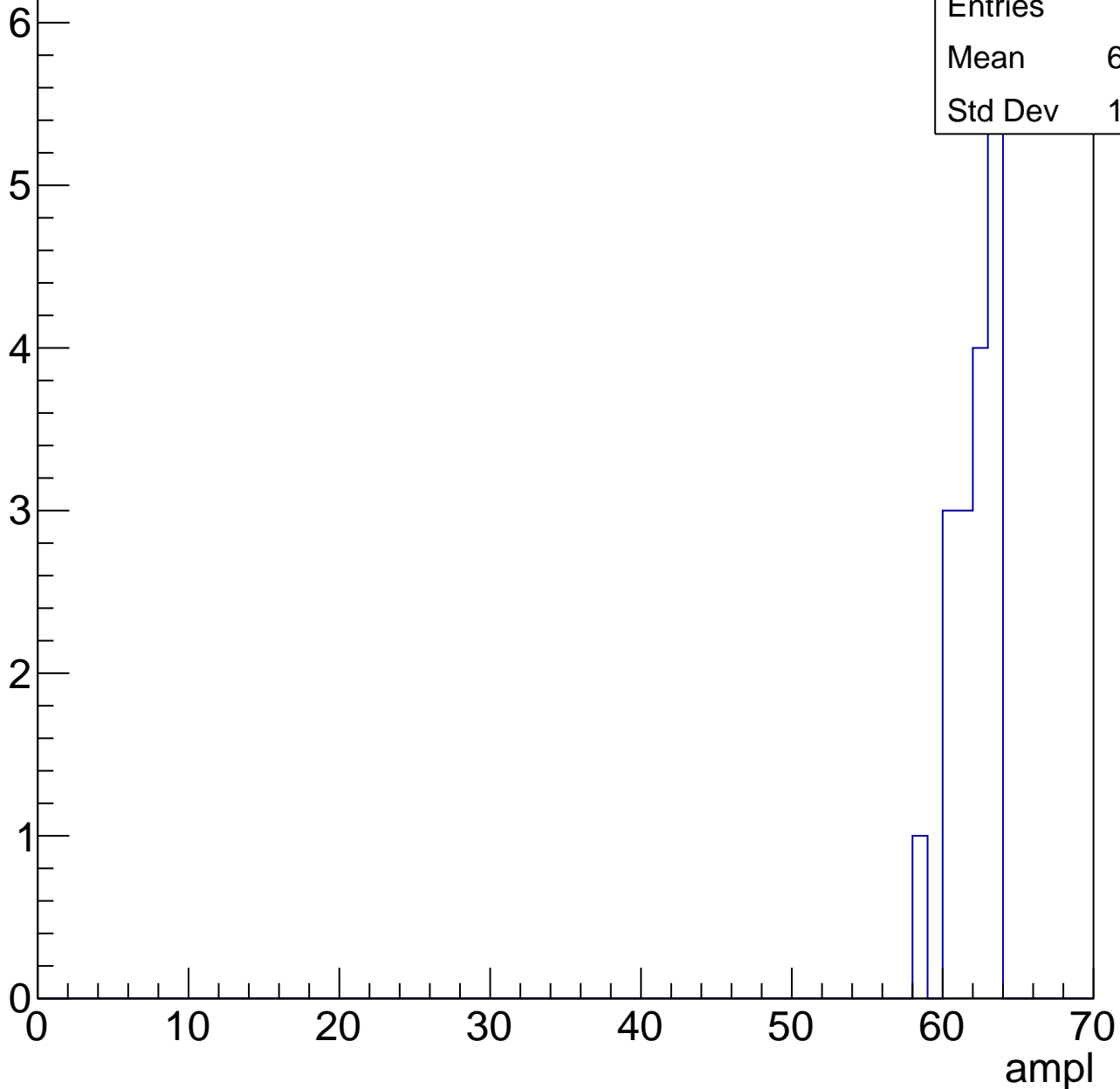


# B1L103S, U1-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	17
Mean	61.59
Std Dev	1.417





# B1L103S, U1-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U1-ch88, adc0

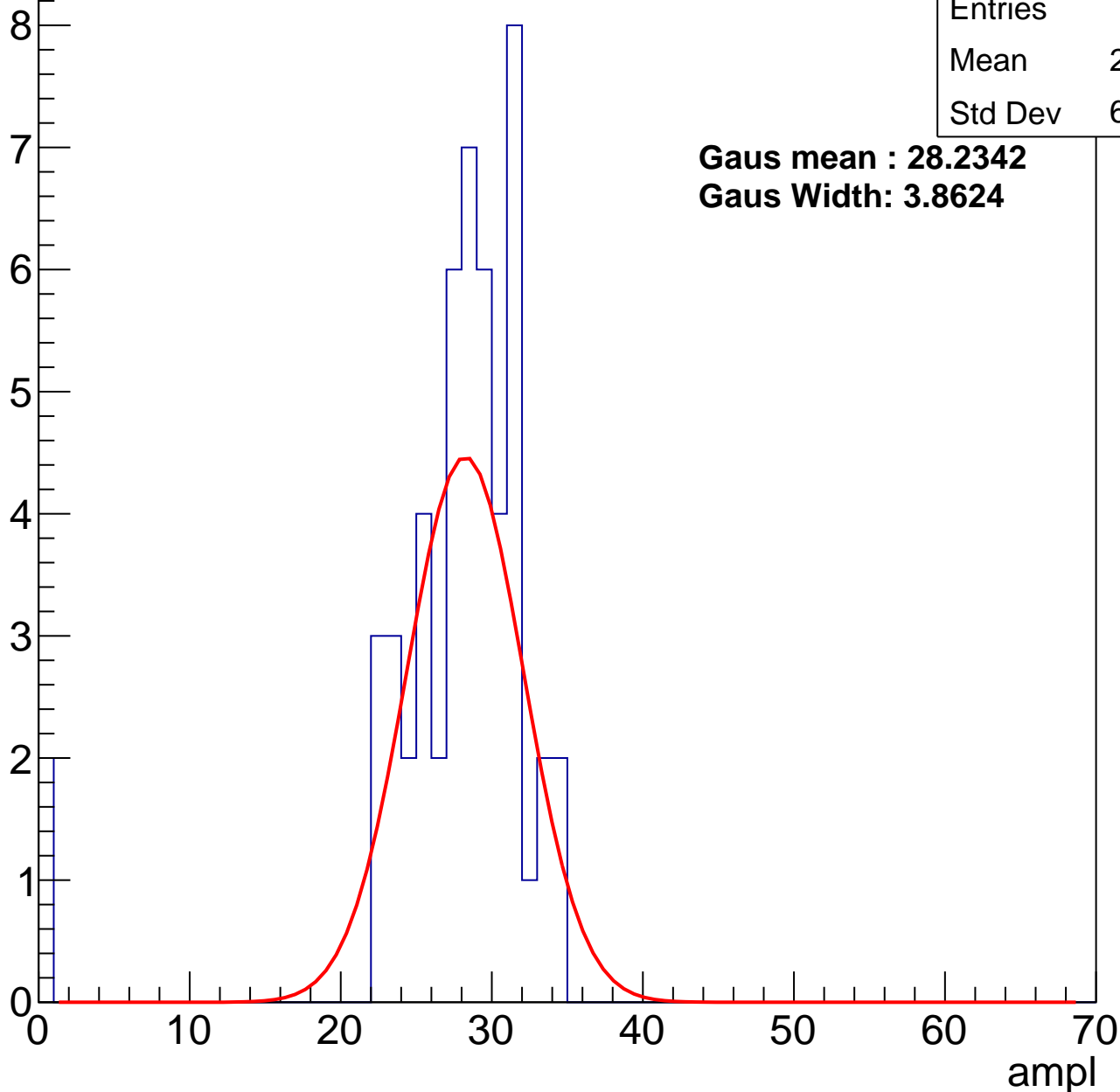
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	26.94
Std Dev	6.212

**Gaus mean : 28.2342**

**Gaus Width: 3.8624**



# B1L103S, U1-ch88, adc1

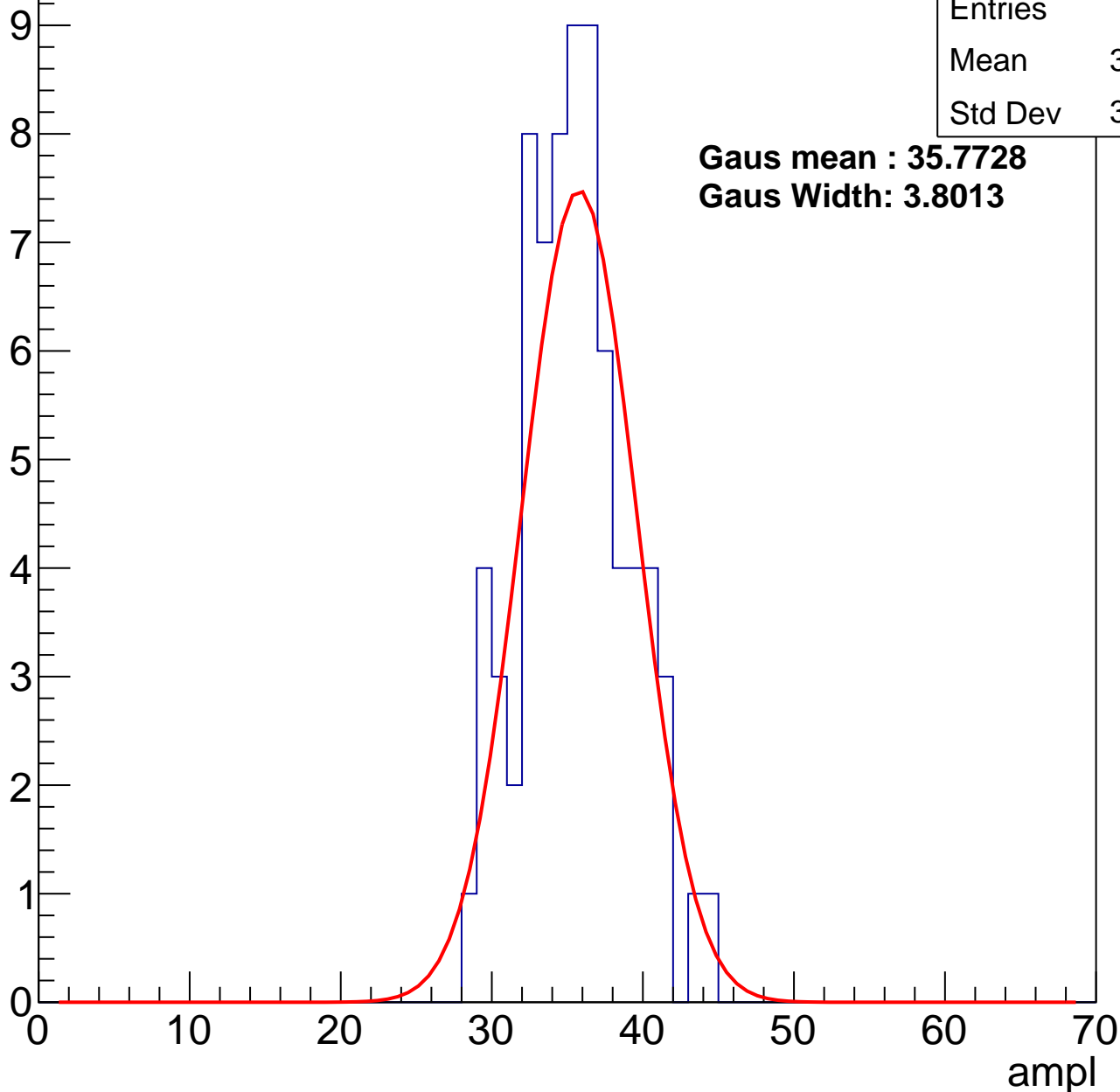
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	35.05
Std Dev	3.475

**Gaus mean : 35.7728**

**Gaus Width: 3.8013**



# B1L103S, U1-ch88, adc2

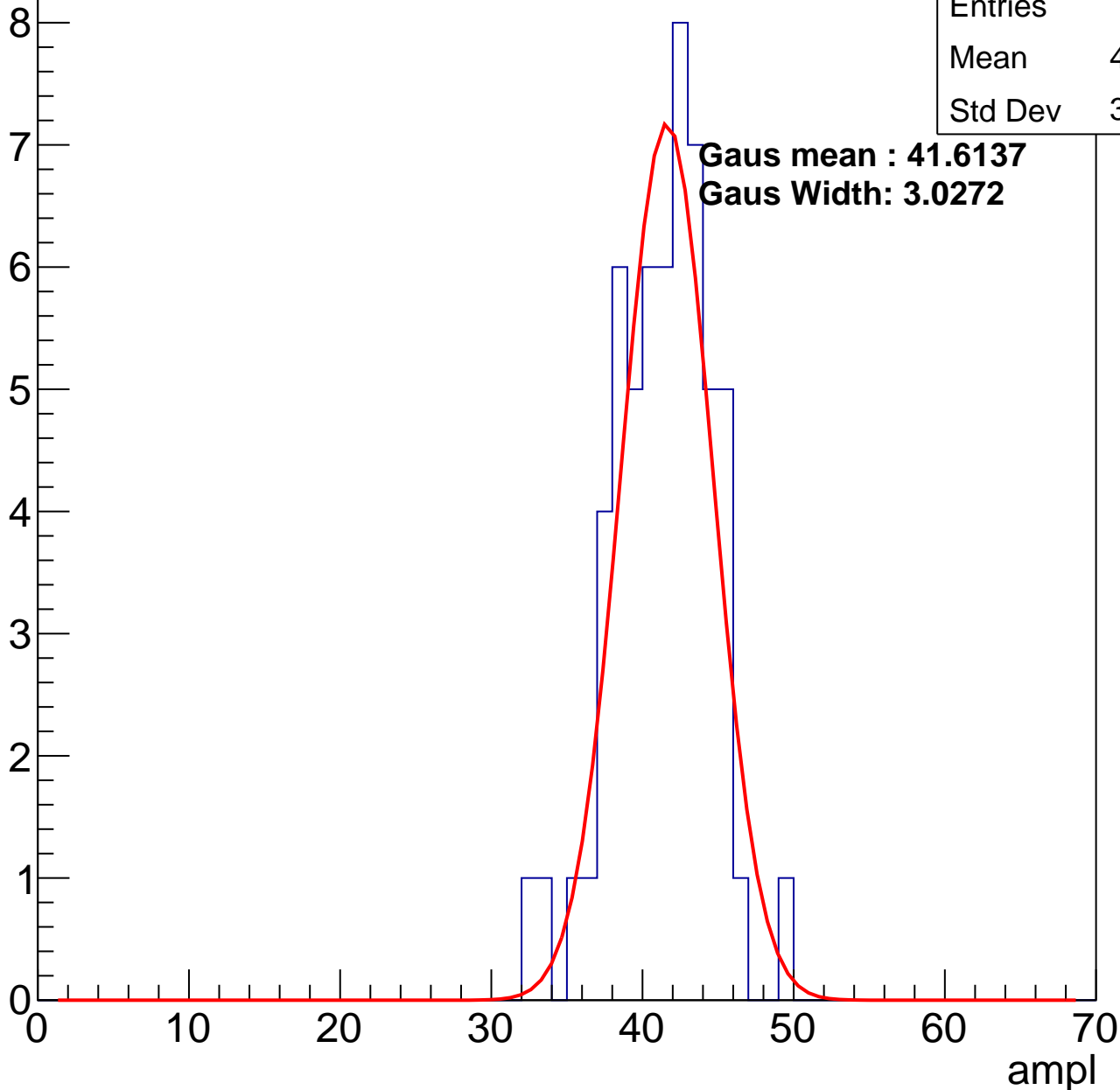
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	40.86
Std Dev	3.213

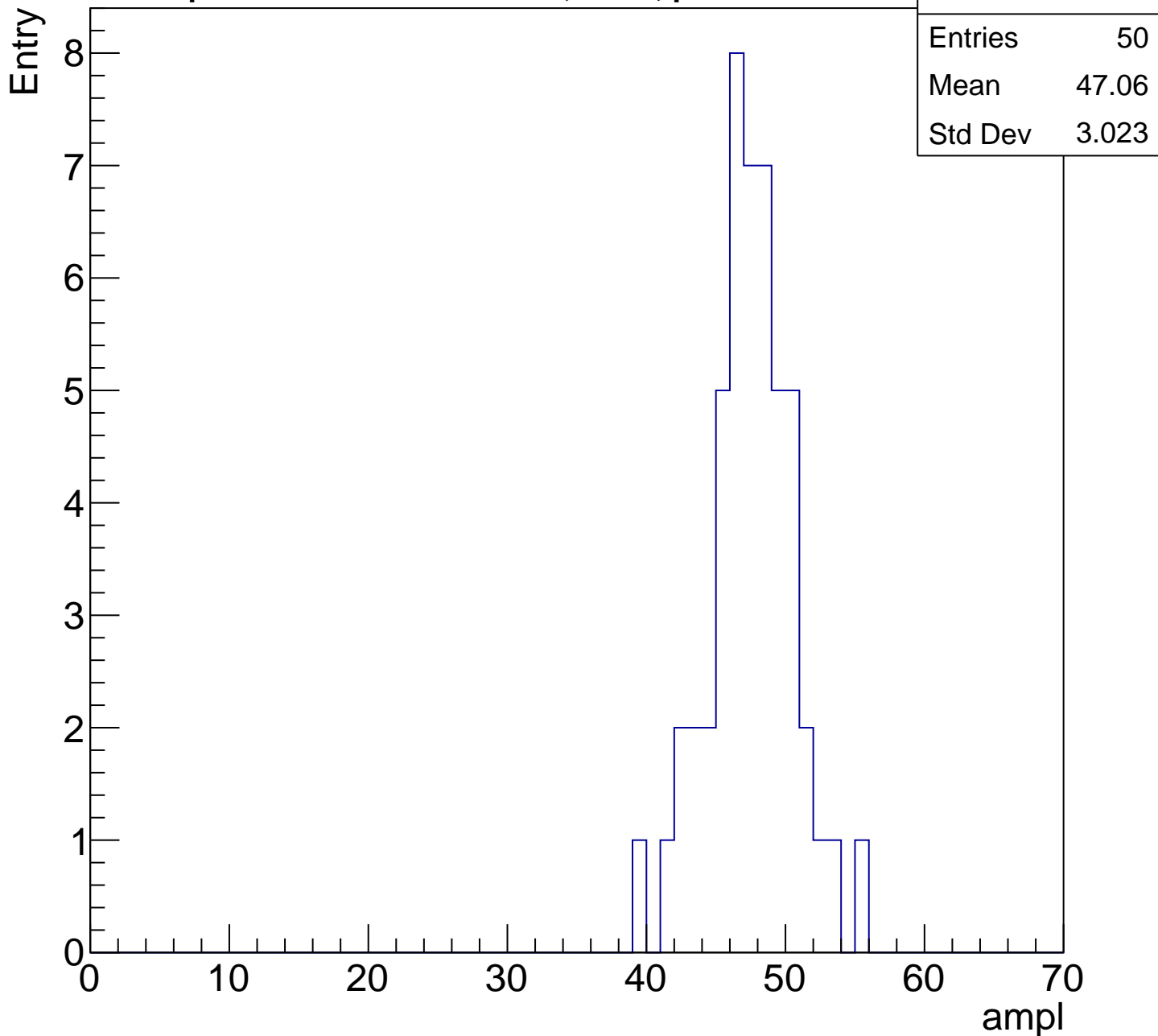
**Gaus mean : 41.6137**

**Gaus Width: 3.0272**



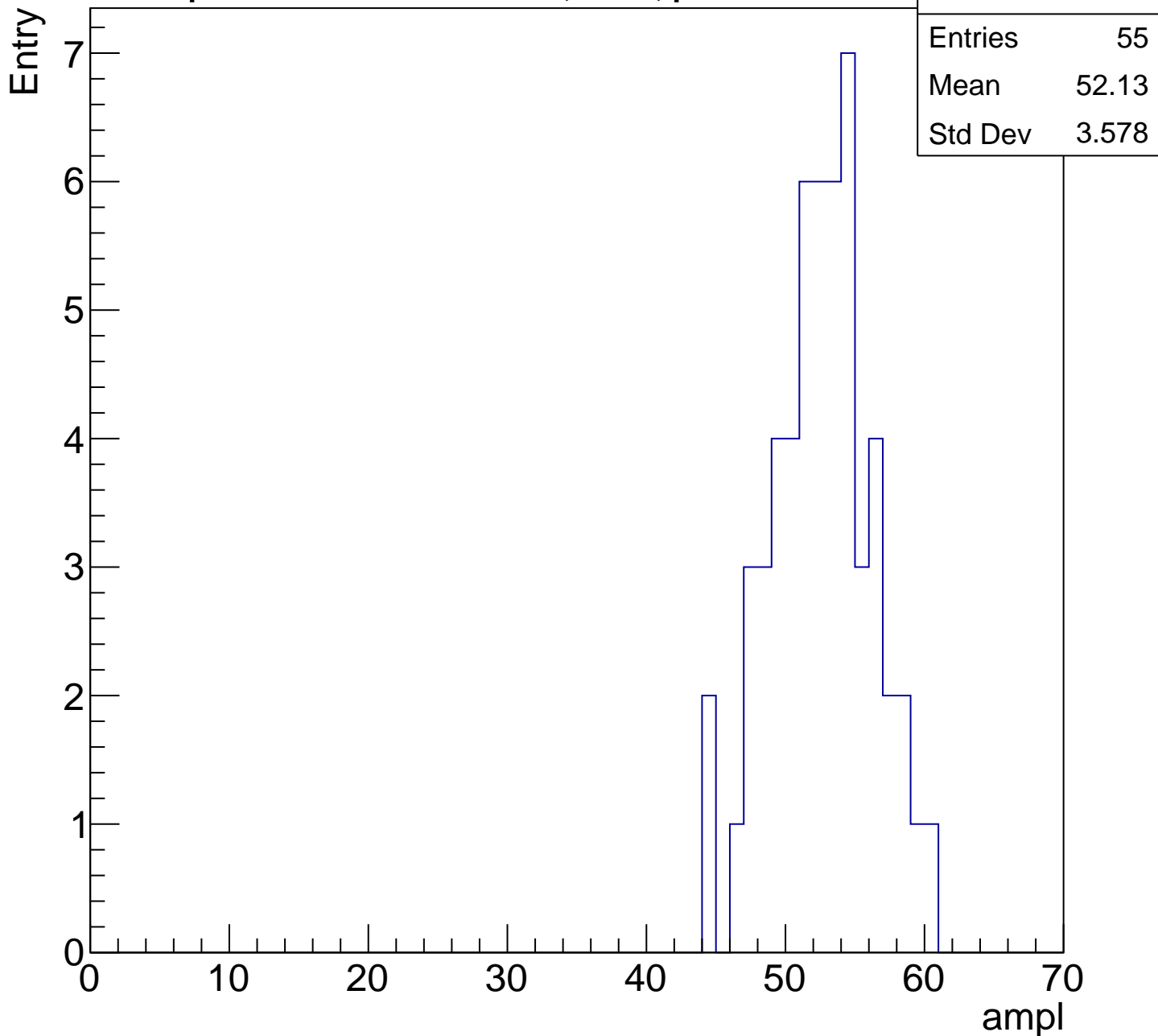
# B1L103S, U1-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U1-ch88, adc4

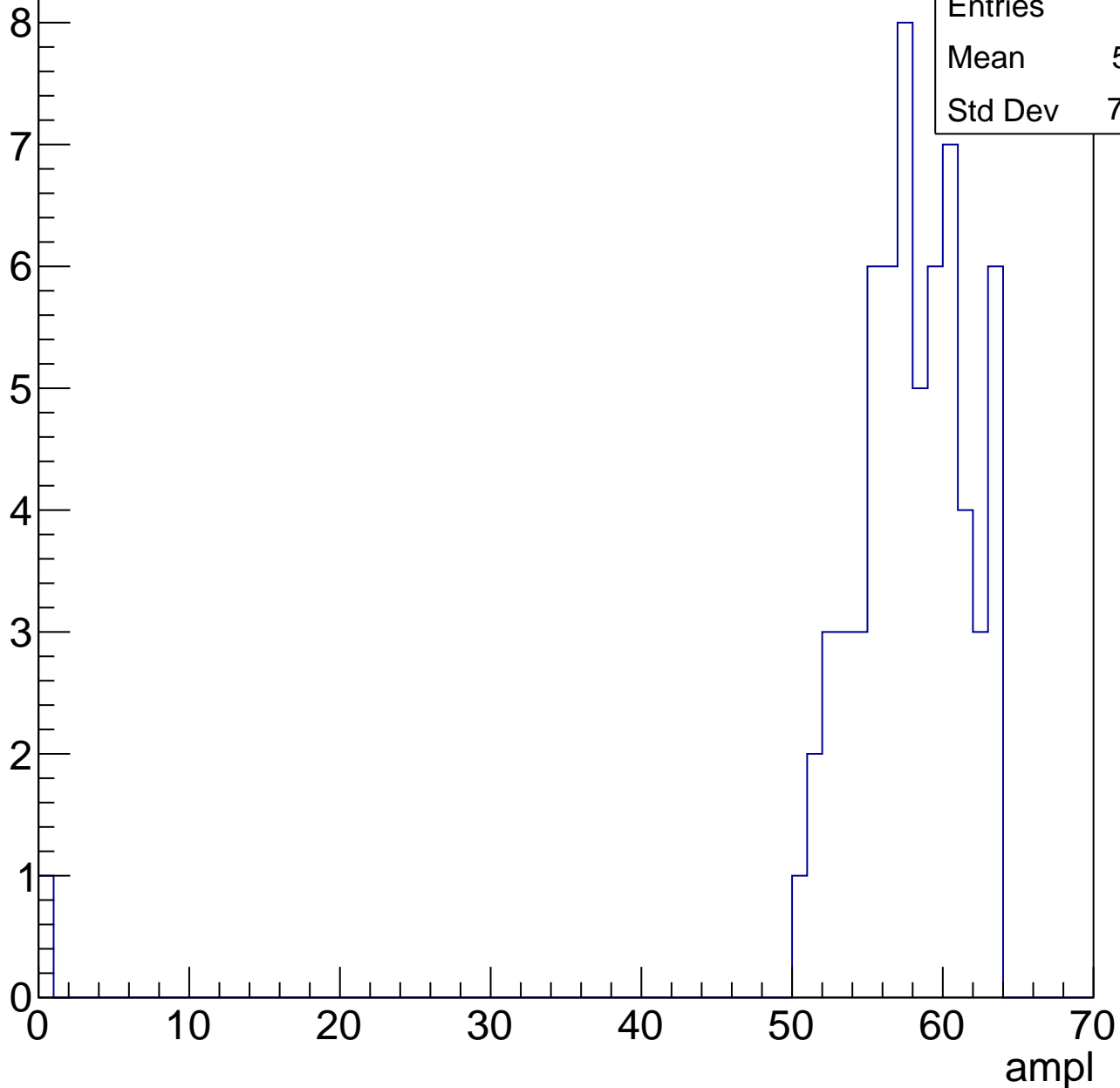
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U1-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

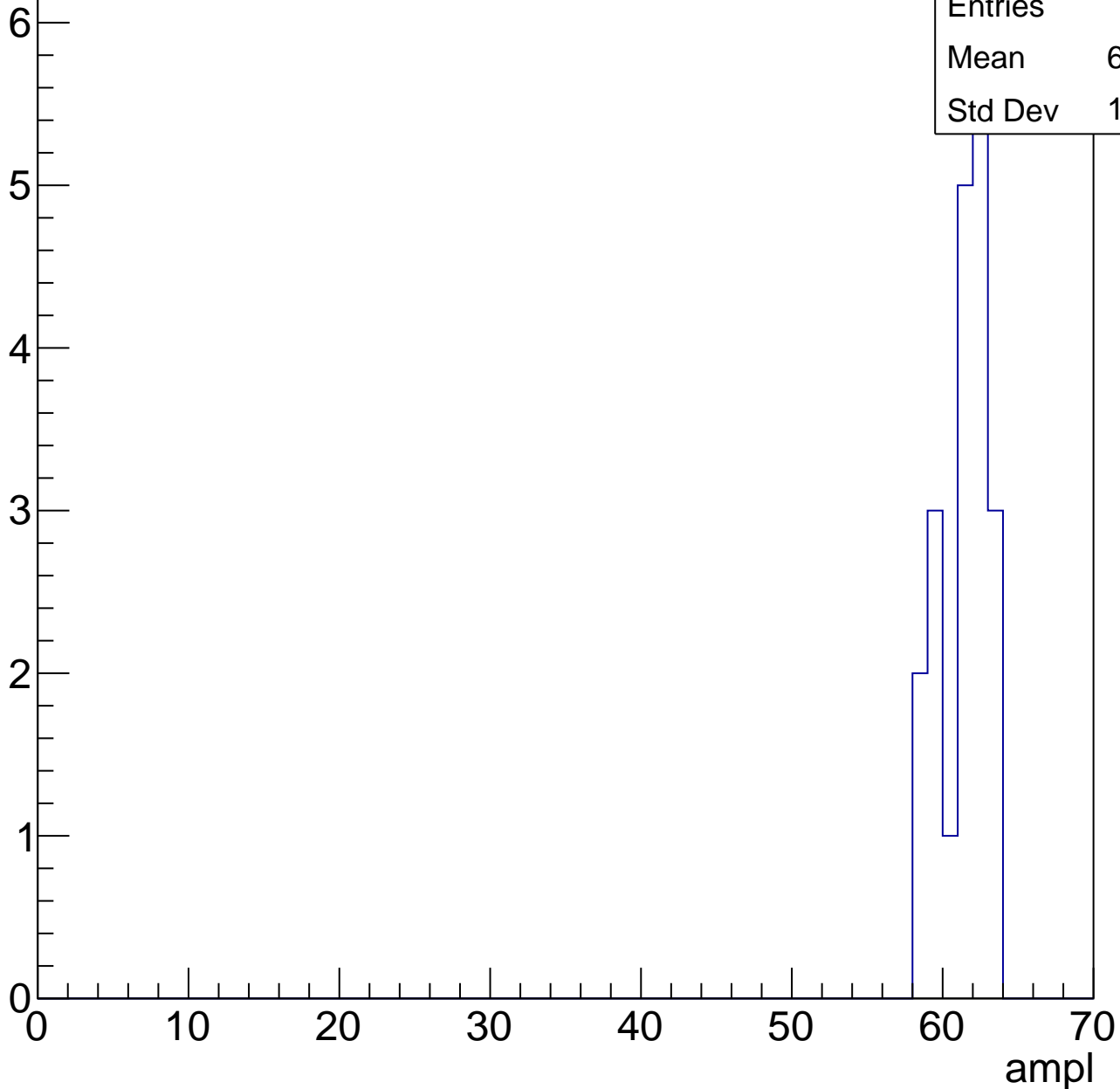


# B1L103S, U1-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	20
Mean	60.95
Std Dev	1.564

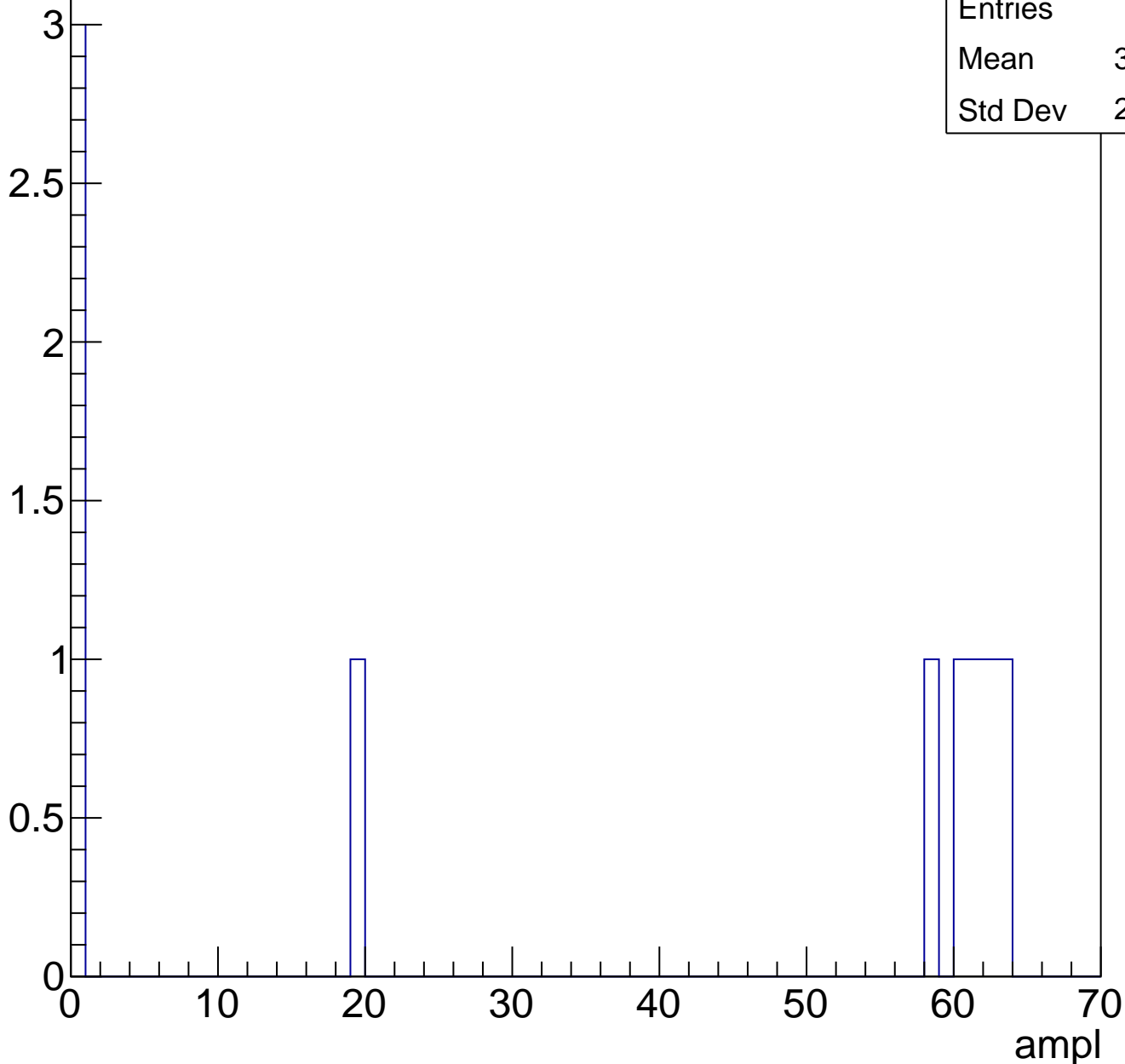




# B1L103S, U1-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	9
Mean	35.89
Std Dev	28.42

# B1L103S, U1-ch89, adc0

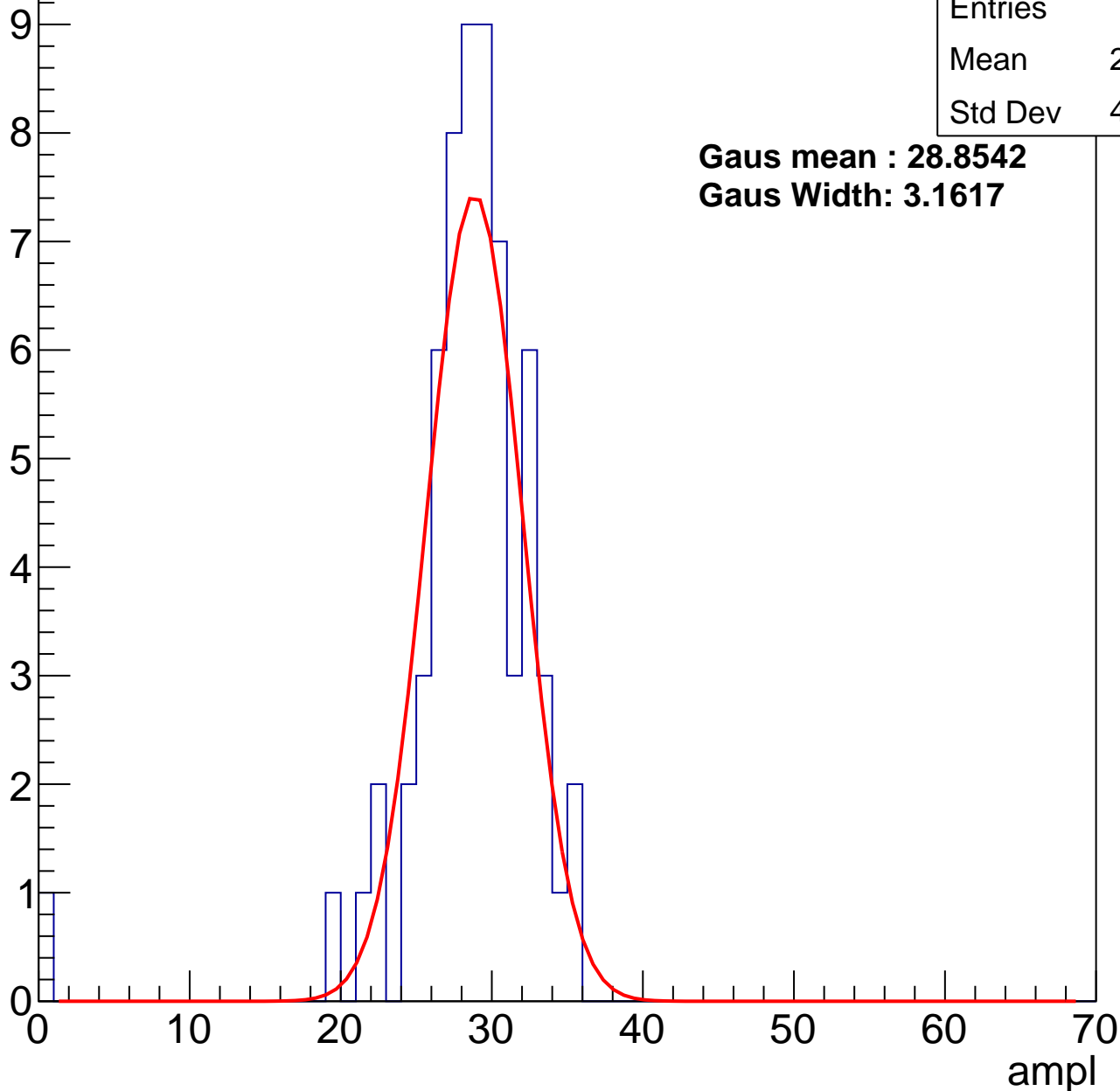
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	27.97
Std Dev	4.753

**Gaus mean : 28.8542**

**Gaus Width: 3.1617**



# B1L103S, U1-ch89, adc1

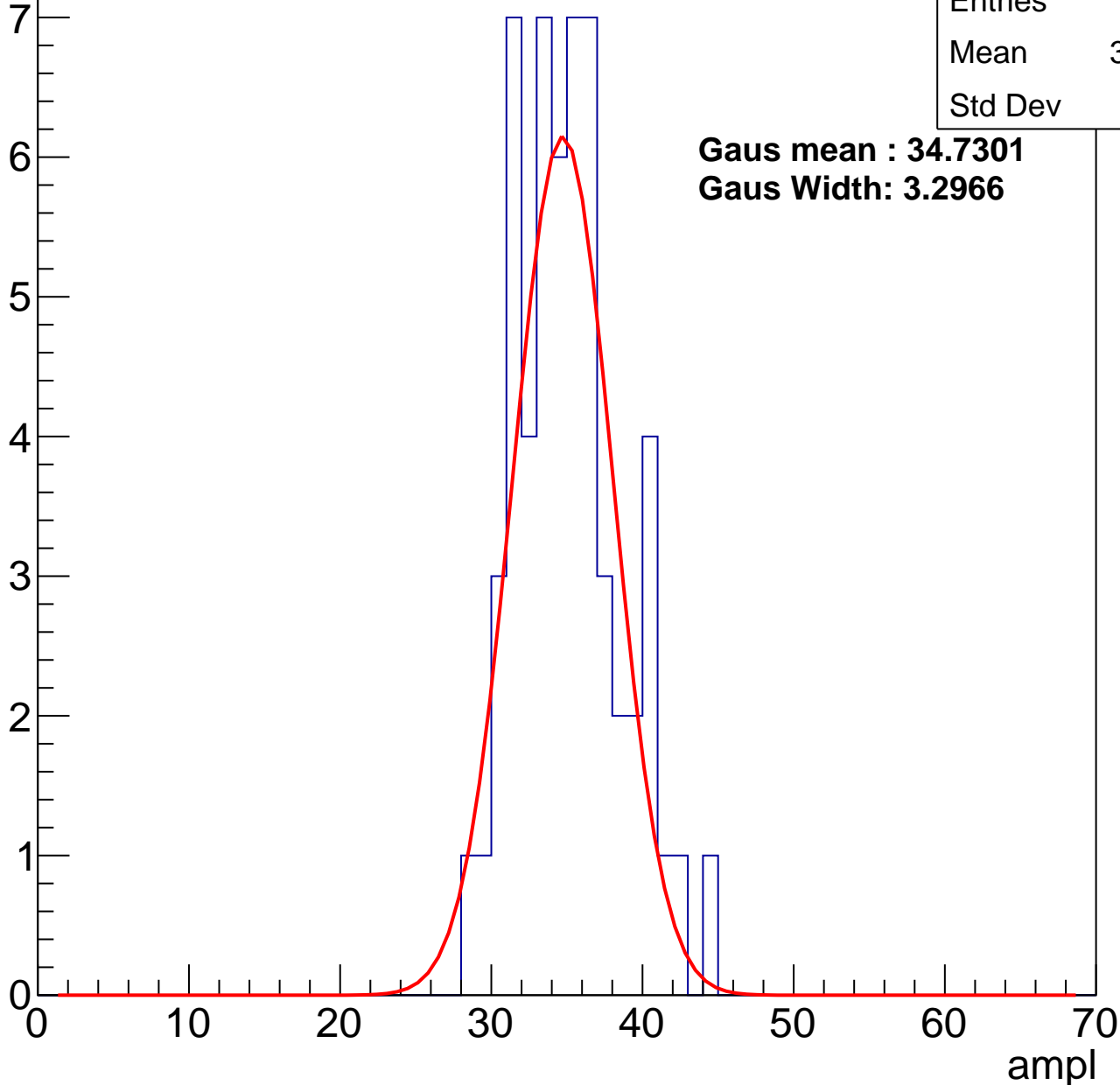
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	34.67
Std Dev	3.43

**Gaus mean : 34.7301**

**Gaus Width: 3.2966**



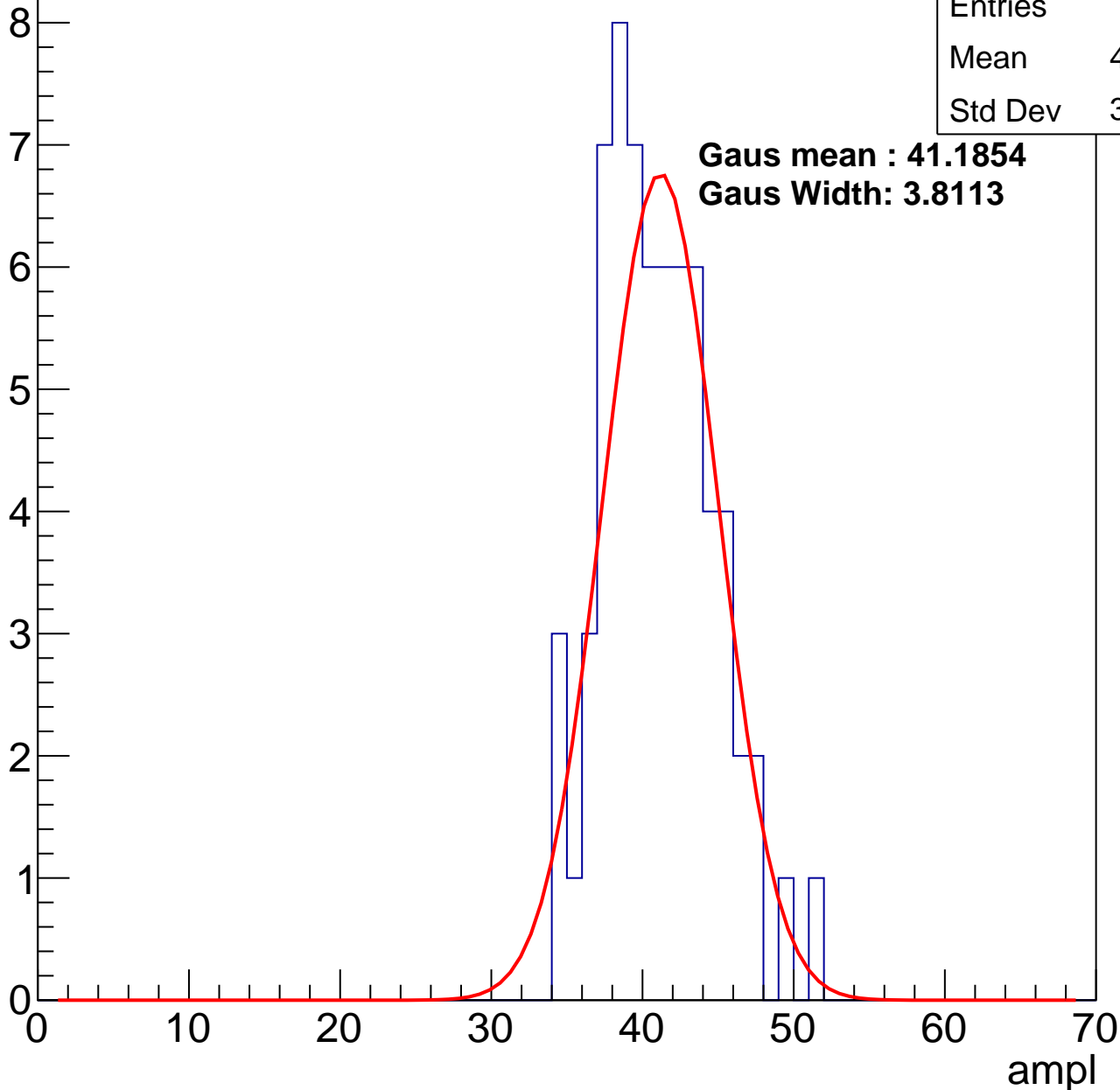
# B1L103S, U1-ch89, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	40.58
Std Dev	3.625

**Gaus mean : 41.1854**  
**Gaus Width: 3.8113**

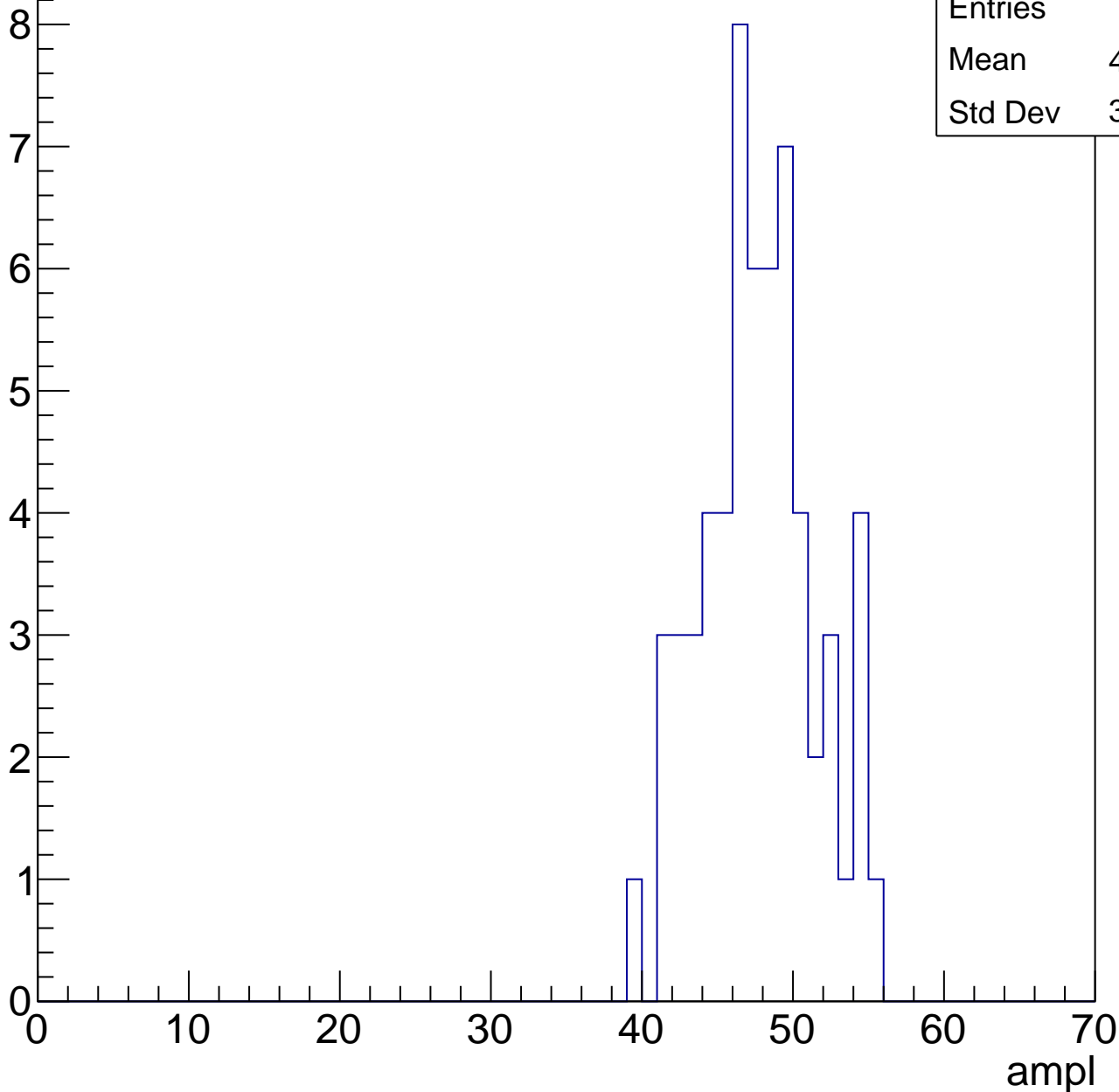


# B1L103S, U1-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	47.27
Std Dev	3.705

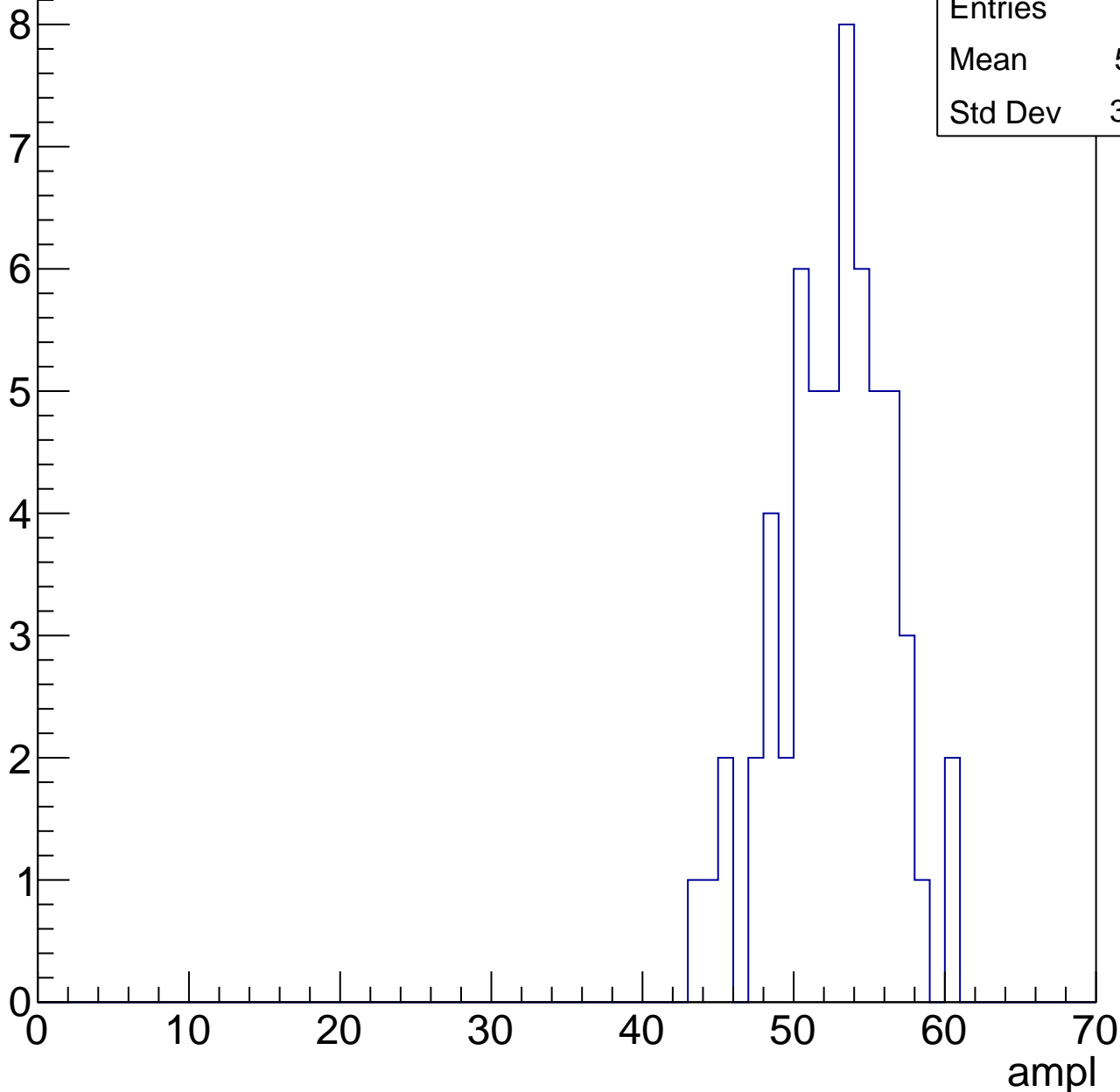


# B1L103S, U1-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

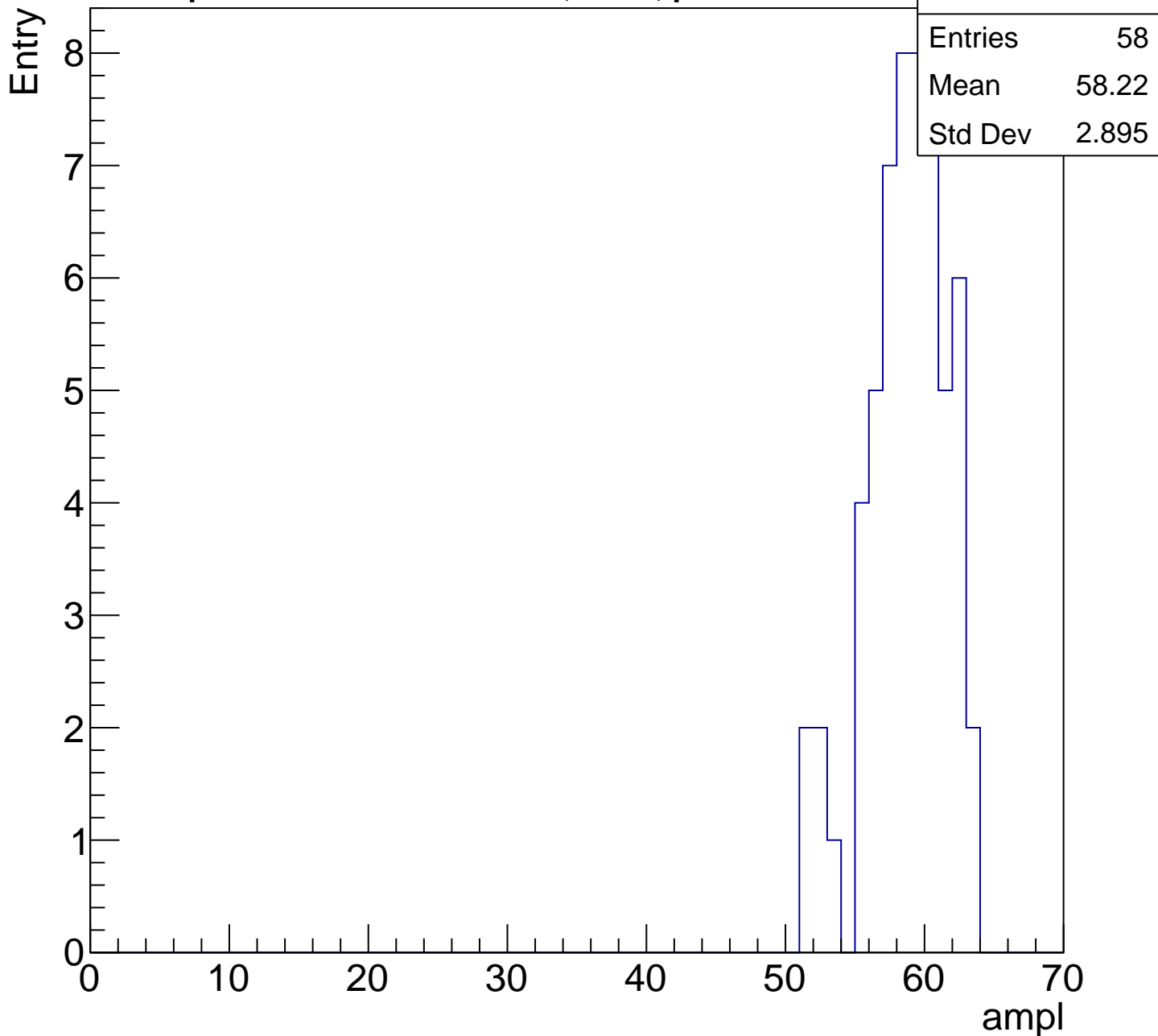
Entry

Entries	58
Mean	52.21
Std Dev	3.708



# B1L103S, U1-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

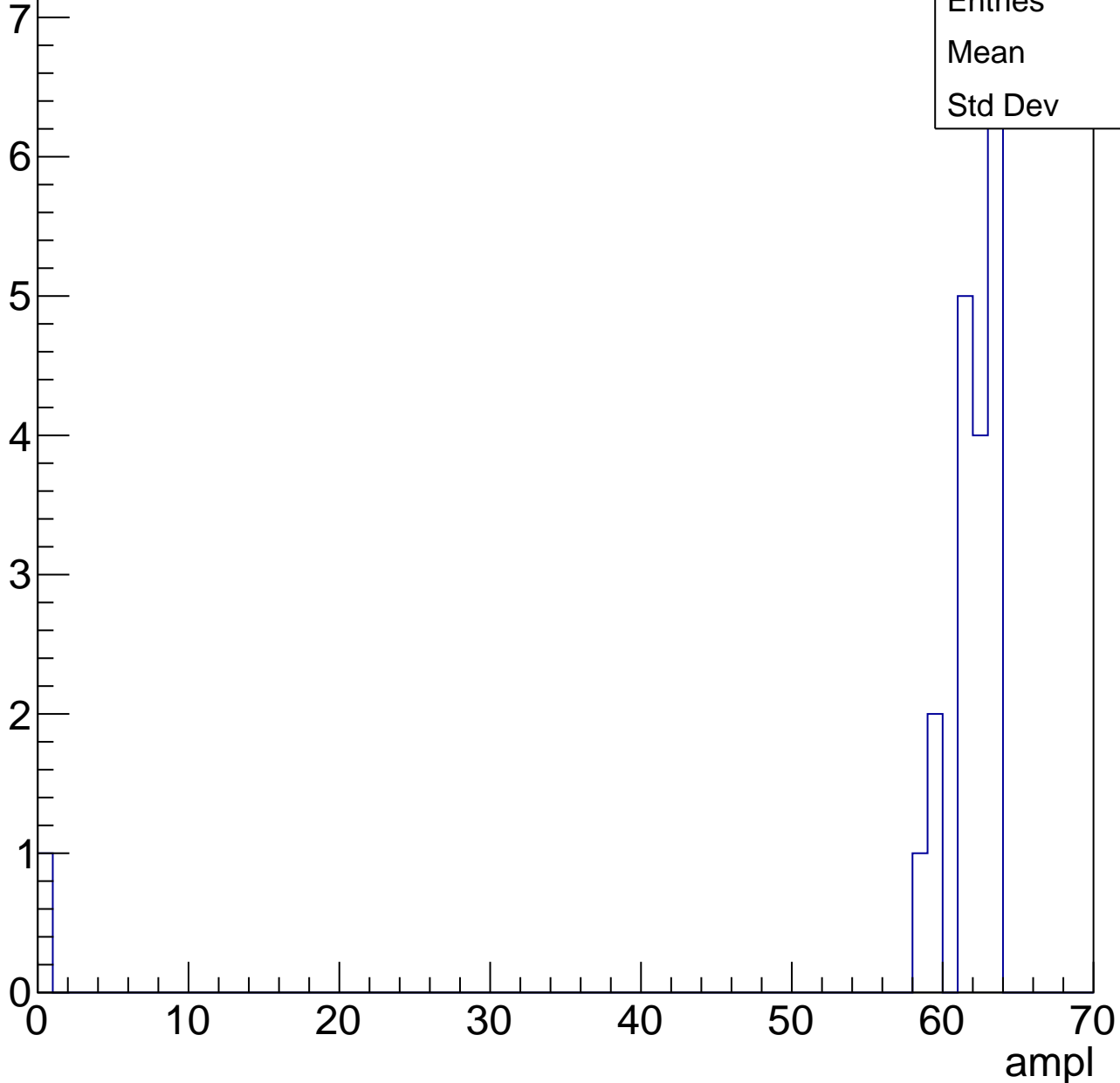


# B1L103S, U1-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	20
Mean	58.5
Std Dev	13.5





# B1L103S, U1-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	39.5
Std Dev	23.5

ampl

# B1L103S, U1-ch90, adc0

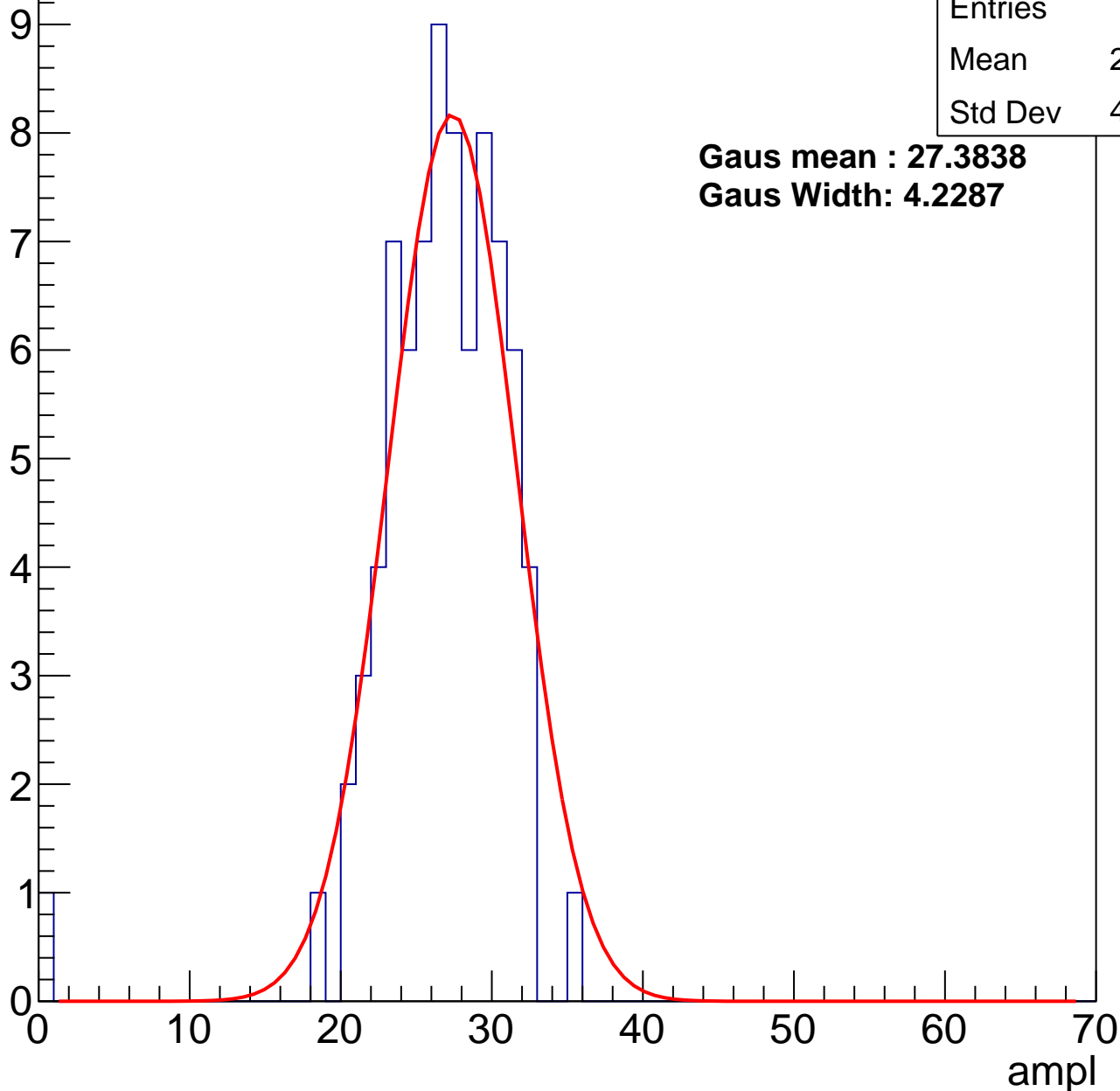
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	26.23
Std Dev	4.517

**Gaus mean : 27.3838**

**Gaus Width: 4.2287**



# B1L103S, U1-ch90, adc1

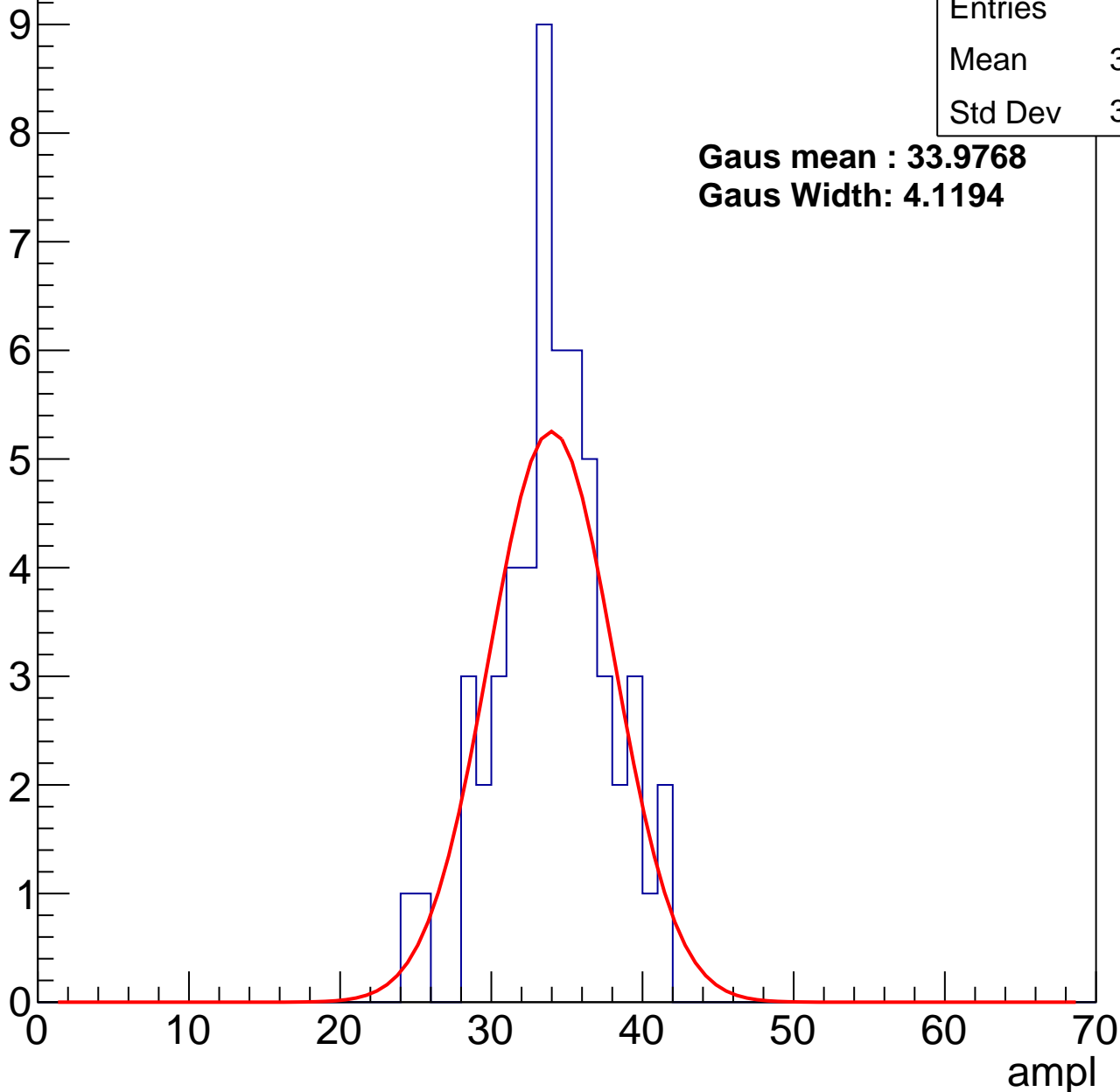
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	33.64
Std Dev	3.655

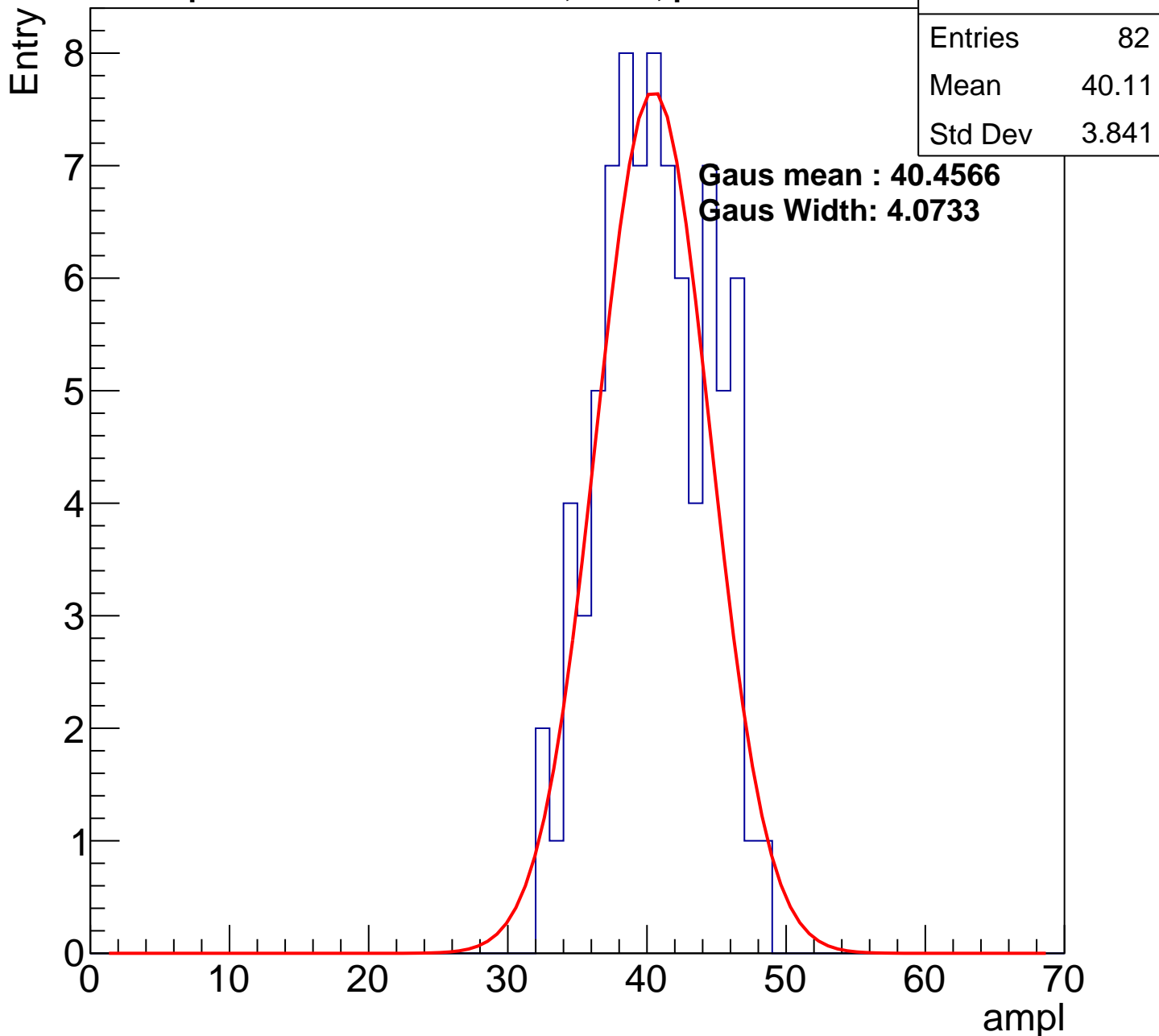
**Gaus mean : 33.9768**

**Gaus Width: 4.1194**



# B1L103S, U1-ch90, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

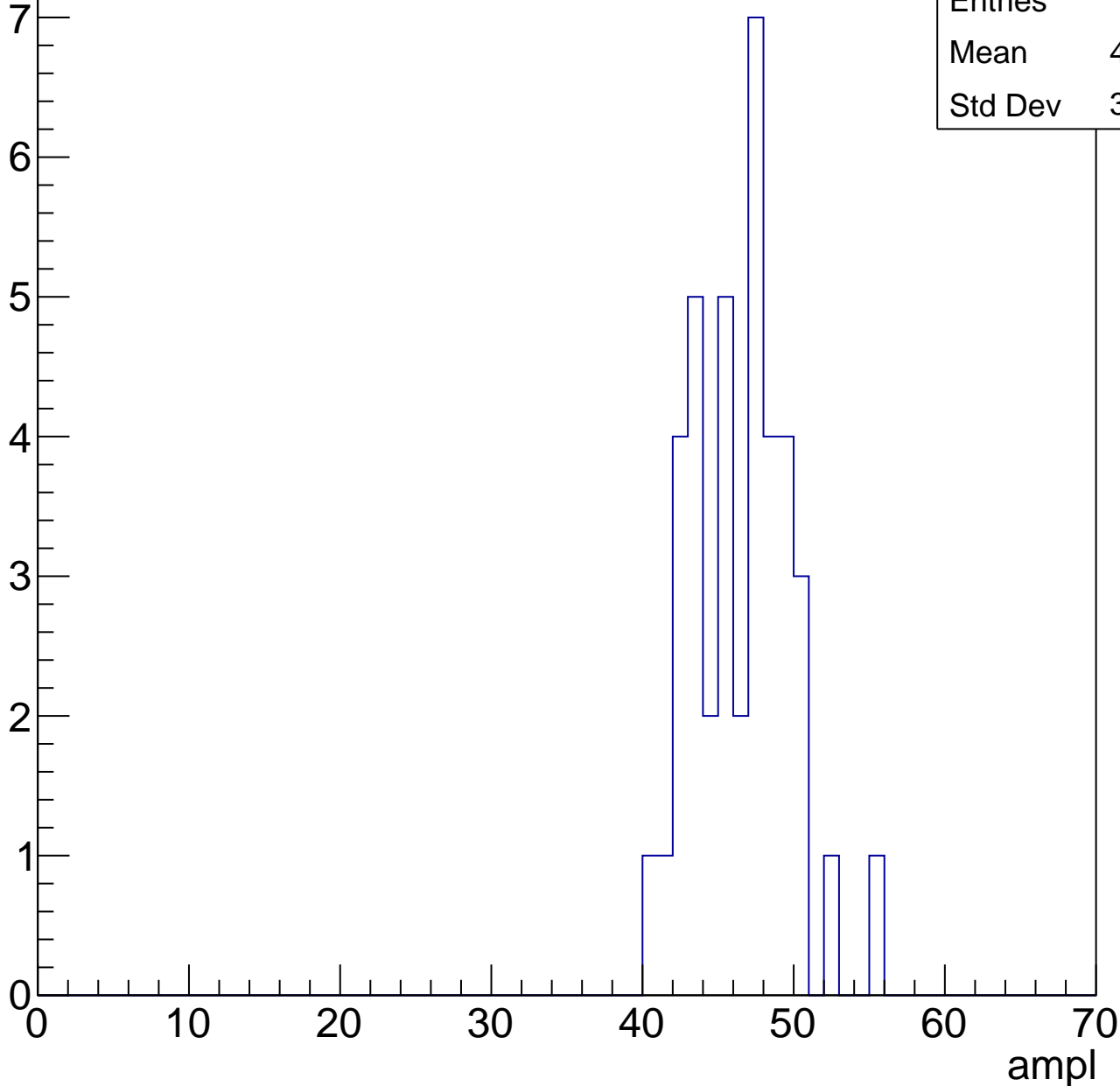


# B1L103S, U1-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	40
Mean	46.08
Std Dev	3.189

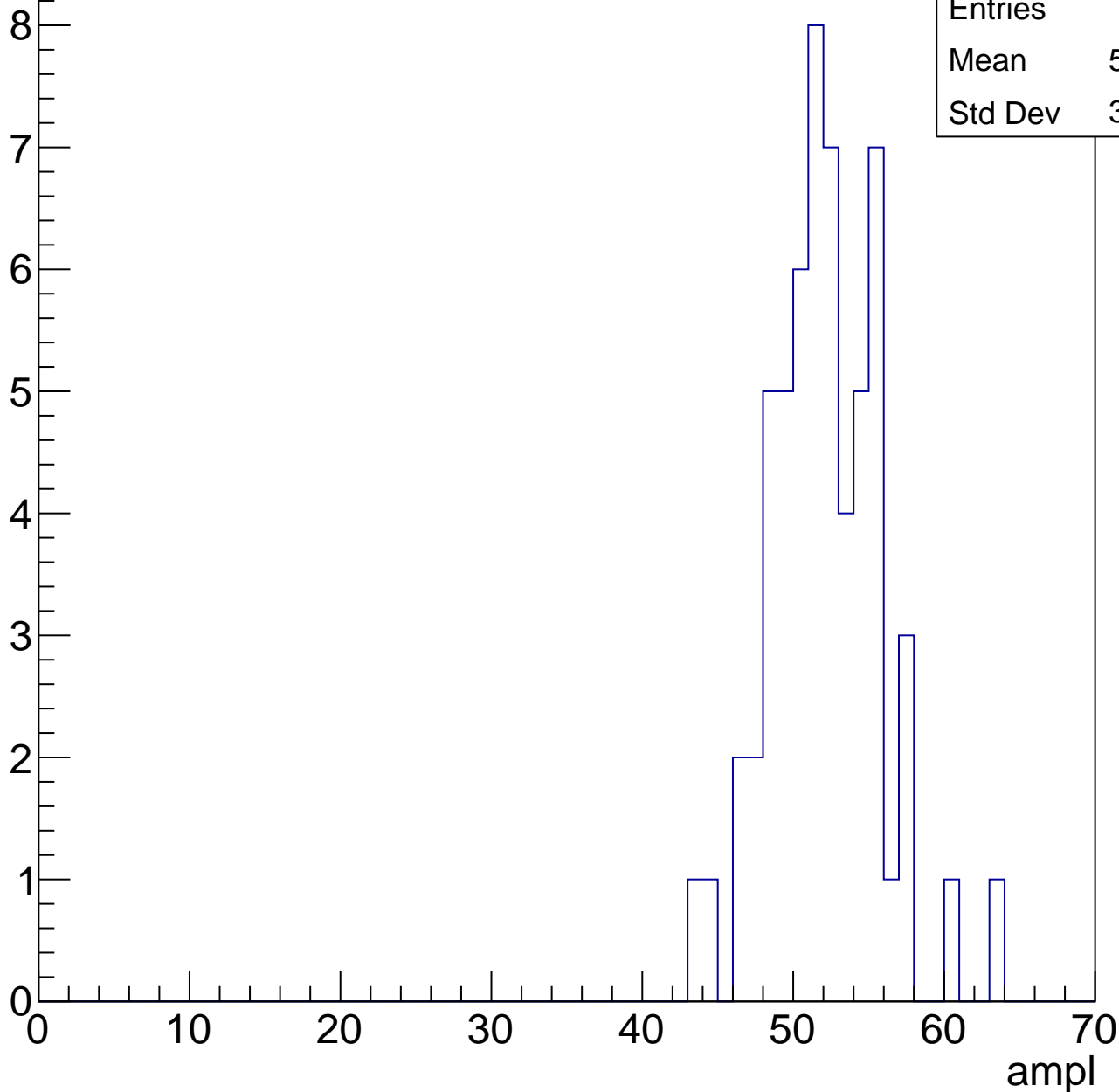


# B1L103S, U1-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

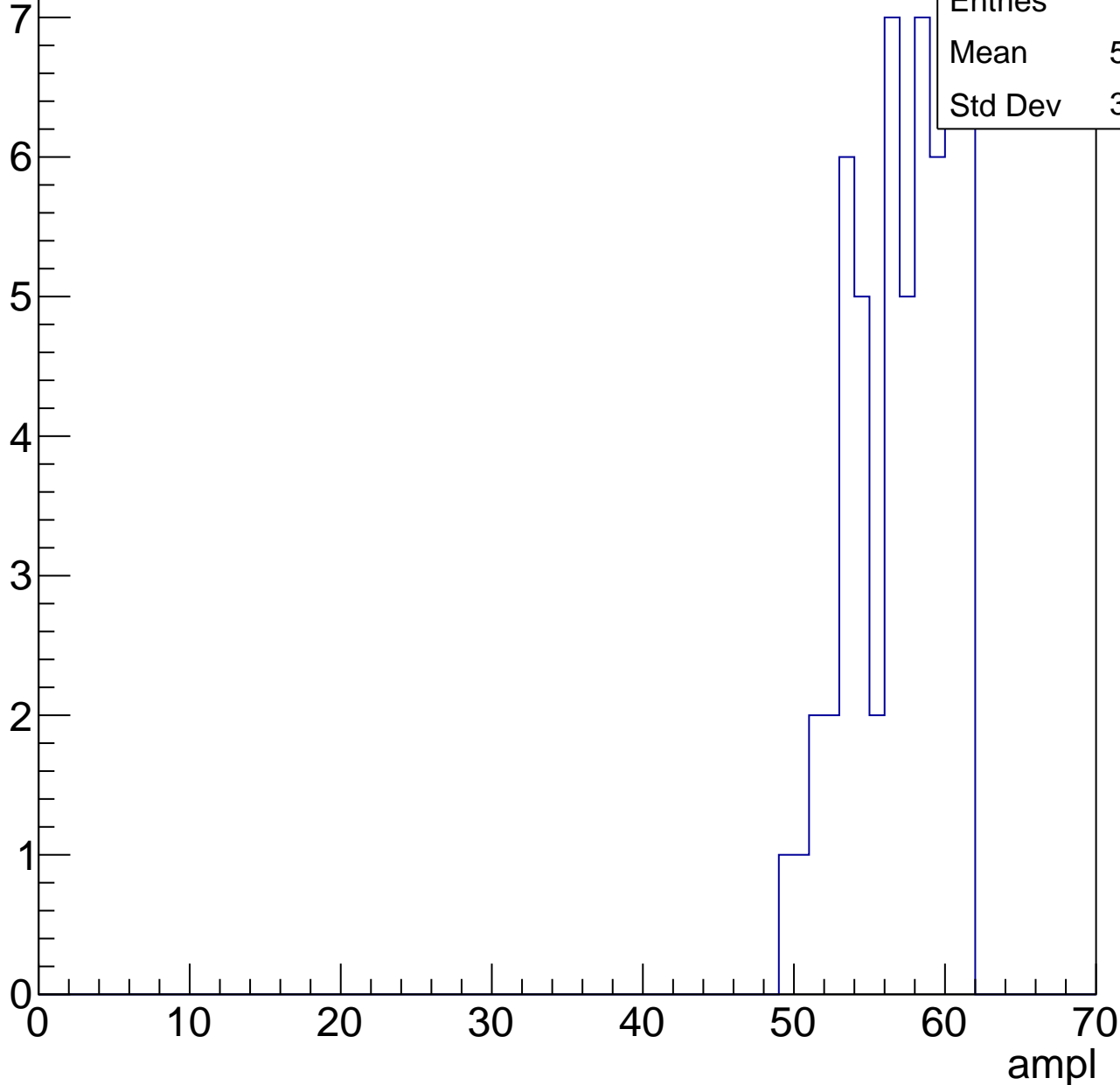
Entries	59
Mean	51.64
Std Dev	3.635



# B1L103S, U1-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

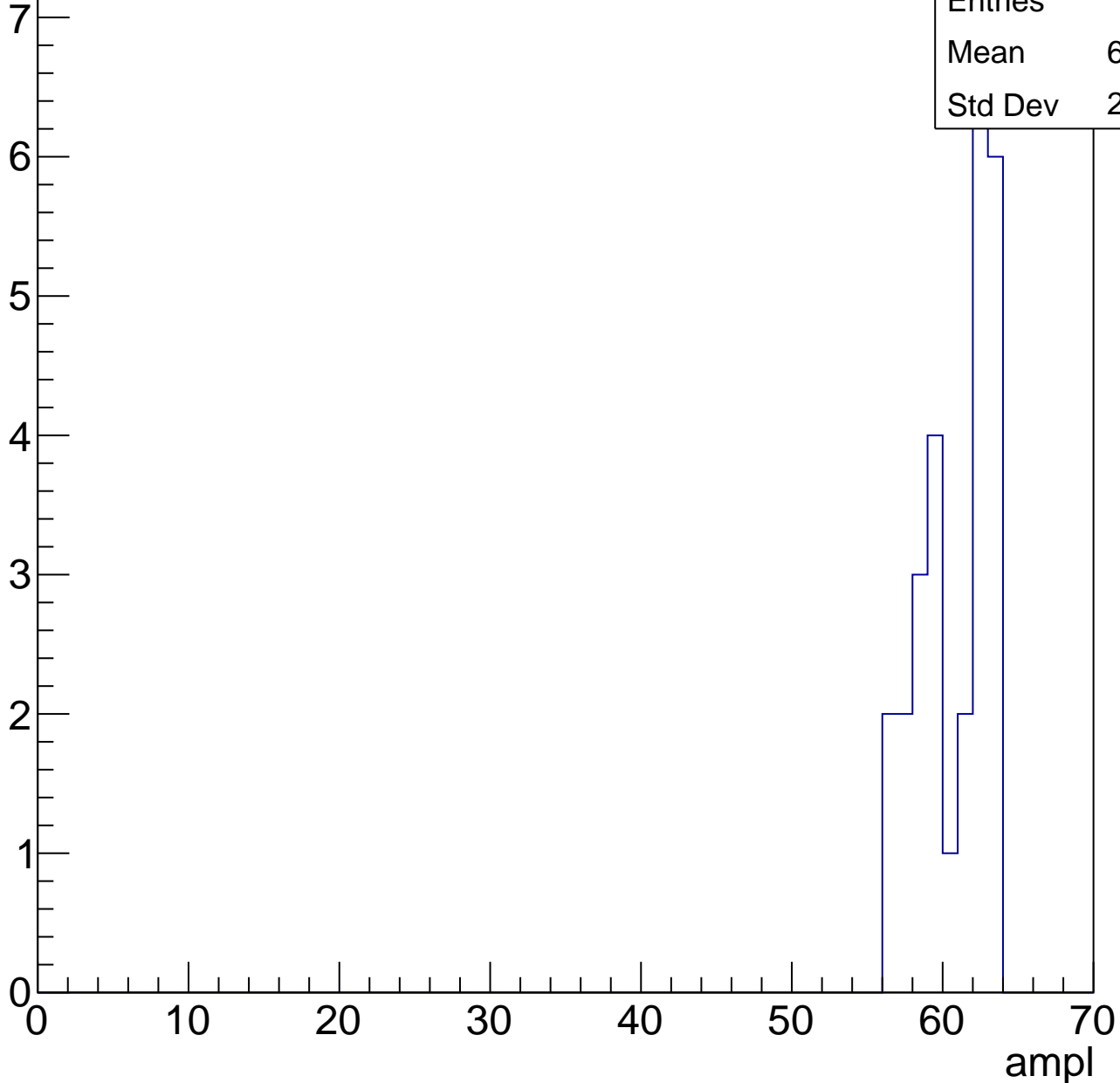


# B1L103S, U1-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	27
Mean	60.37
Std Dev	2.328





# B1L103S, U1-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

8

Mean

62

Std Dev

1

# B1L103S, U1-ch91, adc0

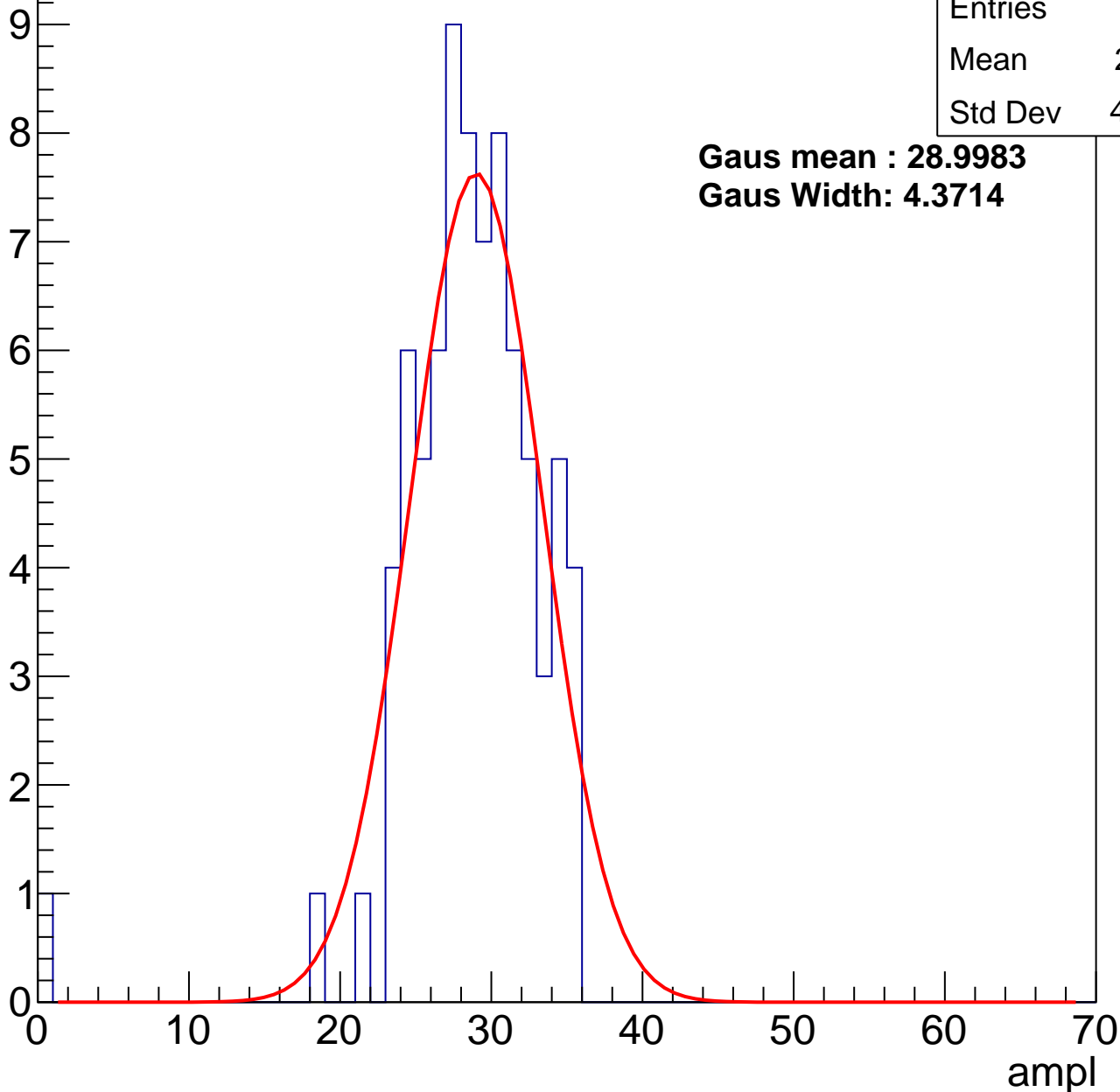
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	28.11
Std Dev	4.813

**Gaus mean : 28.9983**

**Gaus Width: 4.3714**



# B1L103S, U1-ch91, adc1

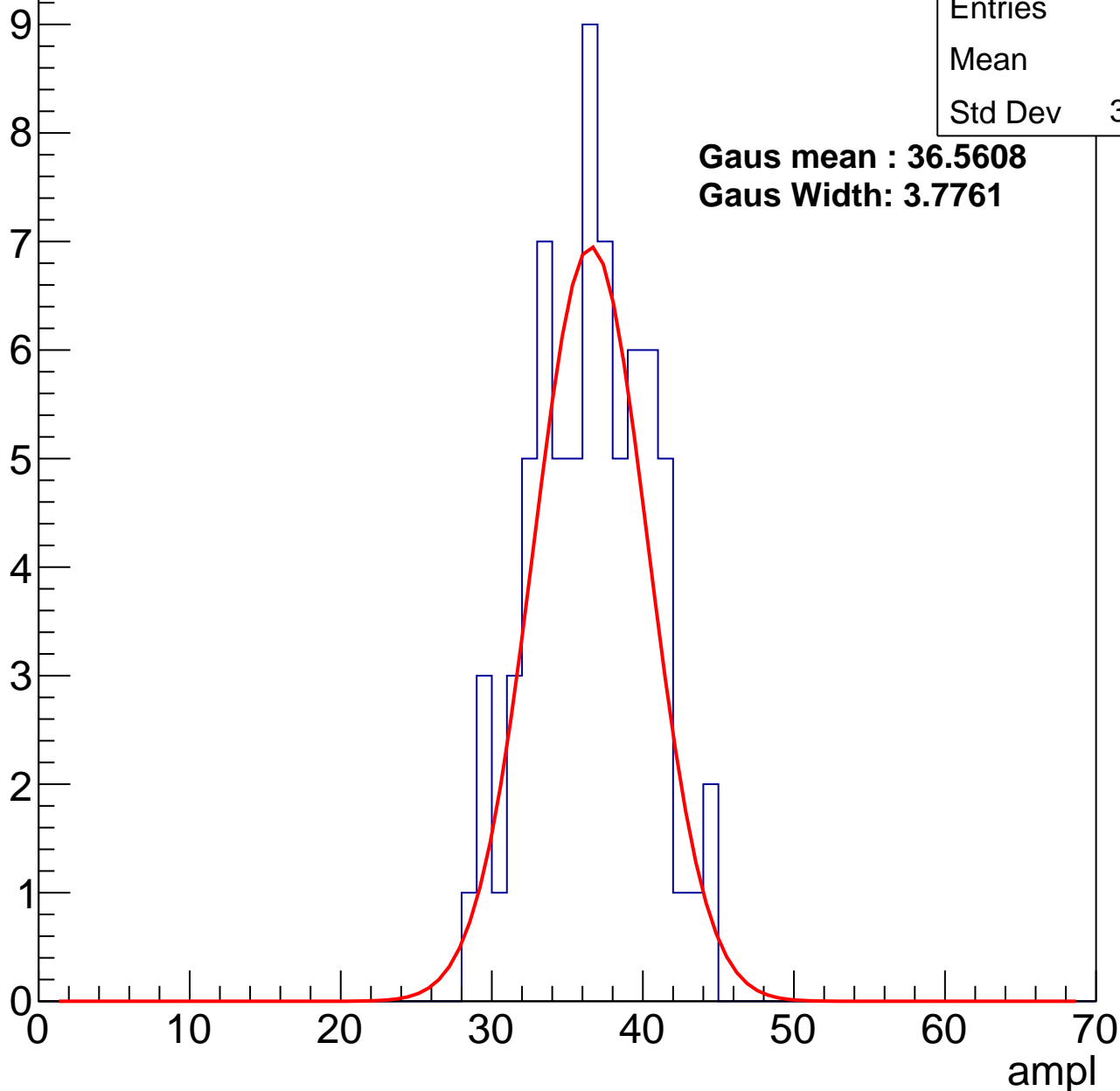
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	36.1
Std Dev	3.735

**Gaus mean : 36.5608**

**Gaus Width: 3.7761**



# B1L103S, U1-ch91, adc2

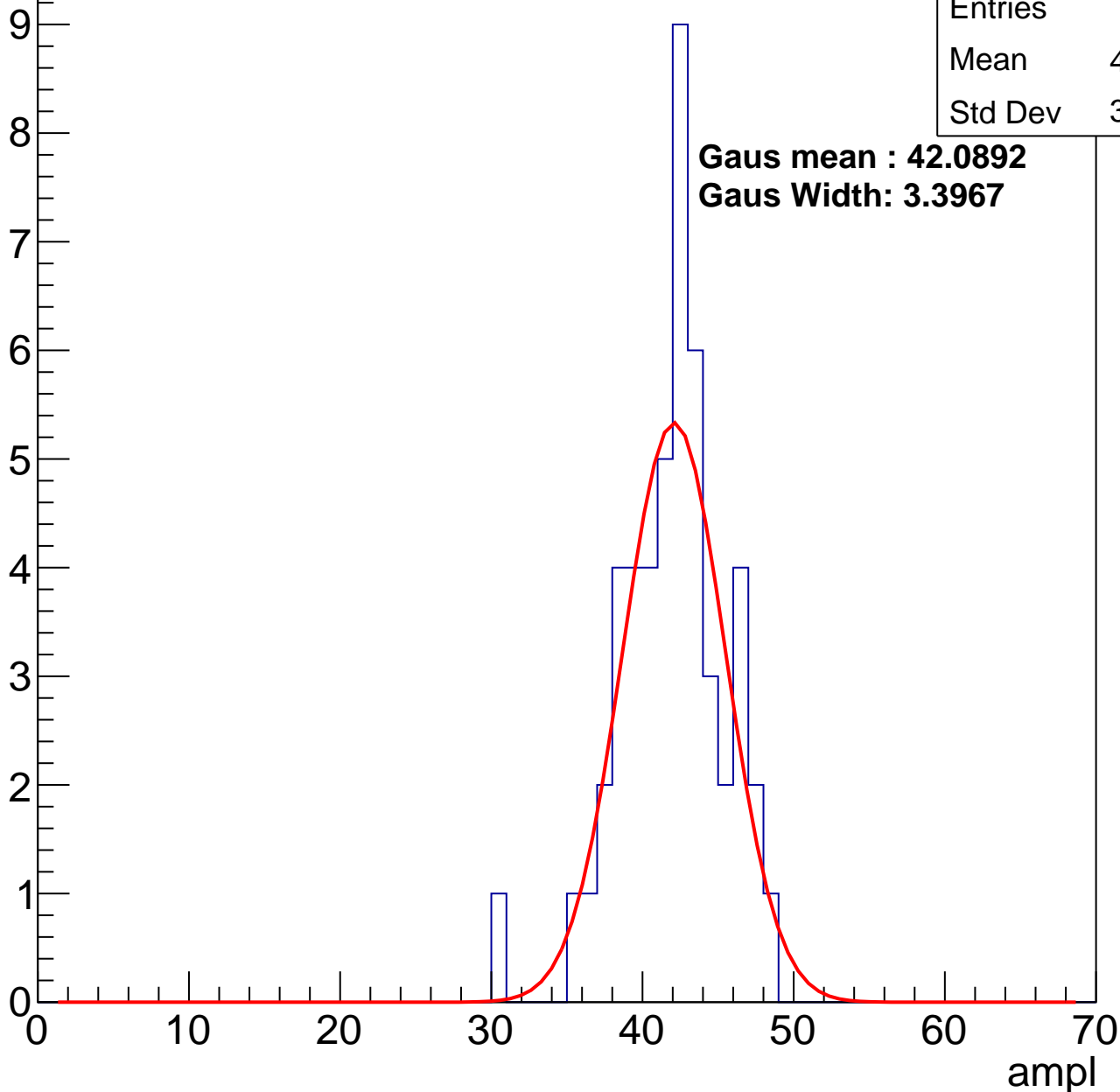
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	41.47
Std Dev	3.417

**Gaus mean : 42.0892**

**Gaus Width: 3.3967**

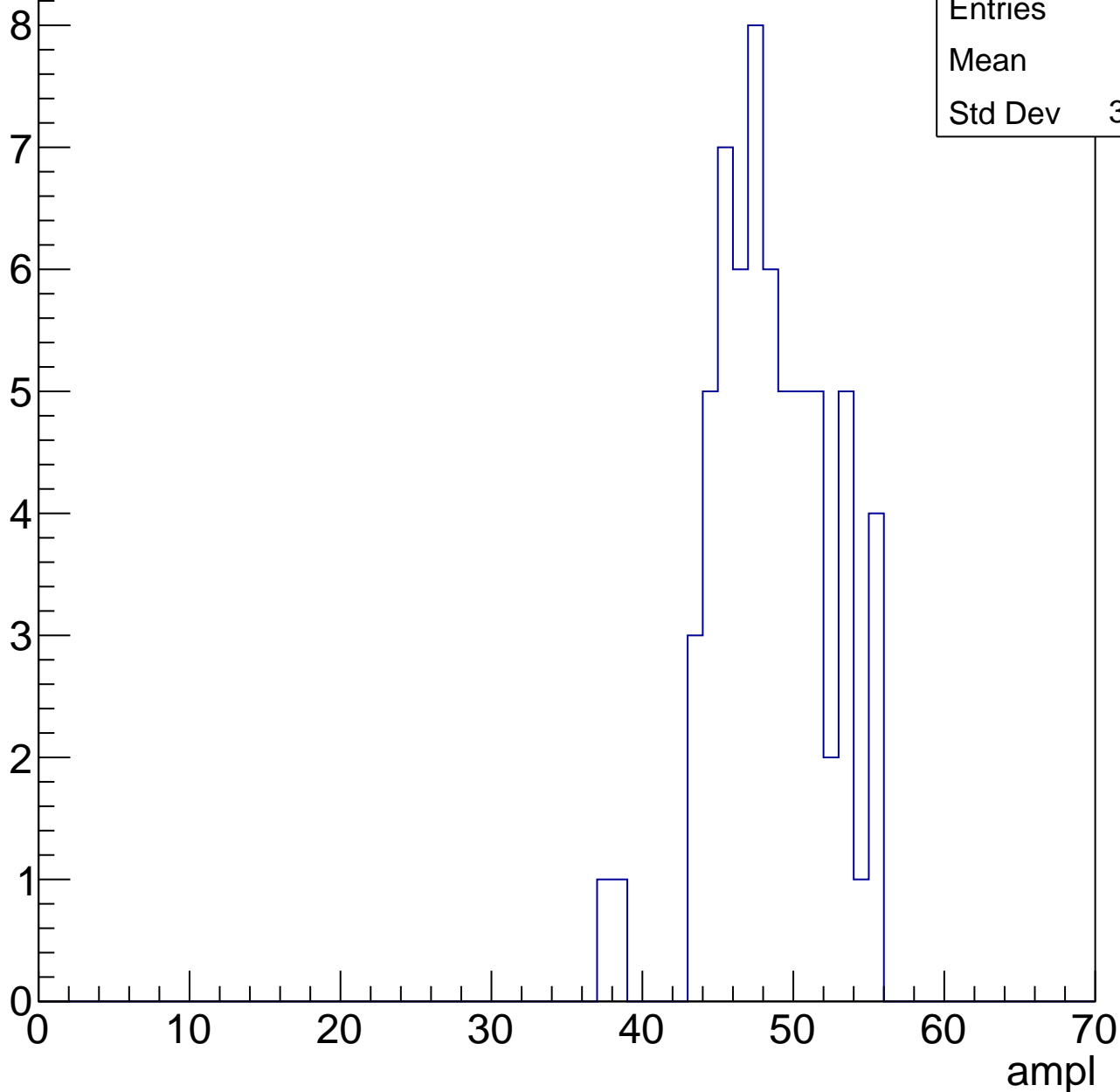


# B1L103S, U1-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

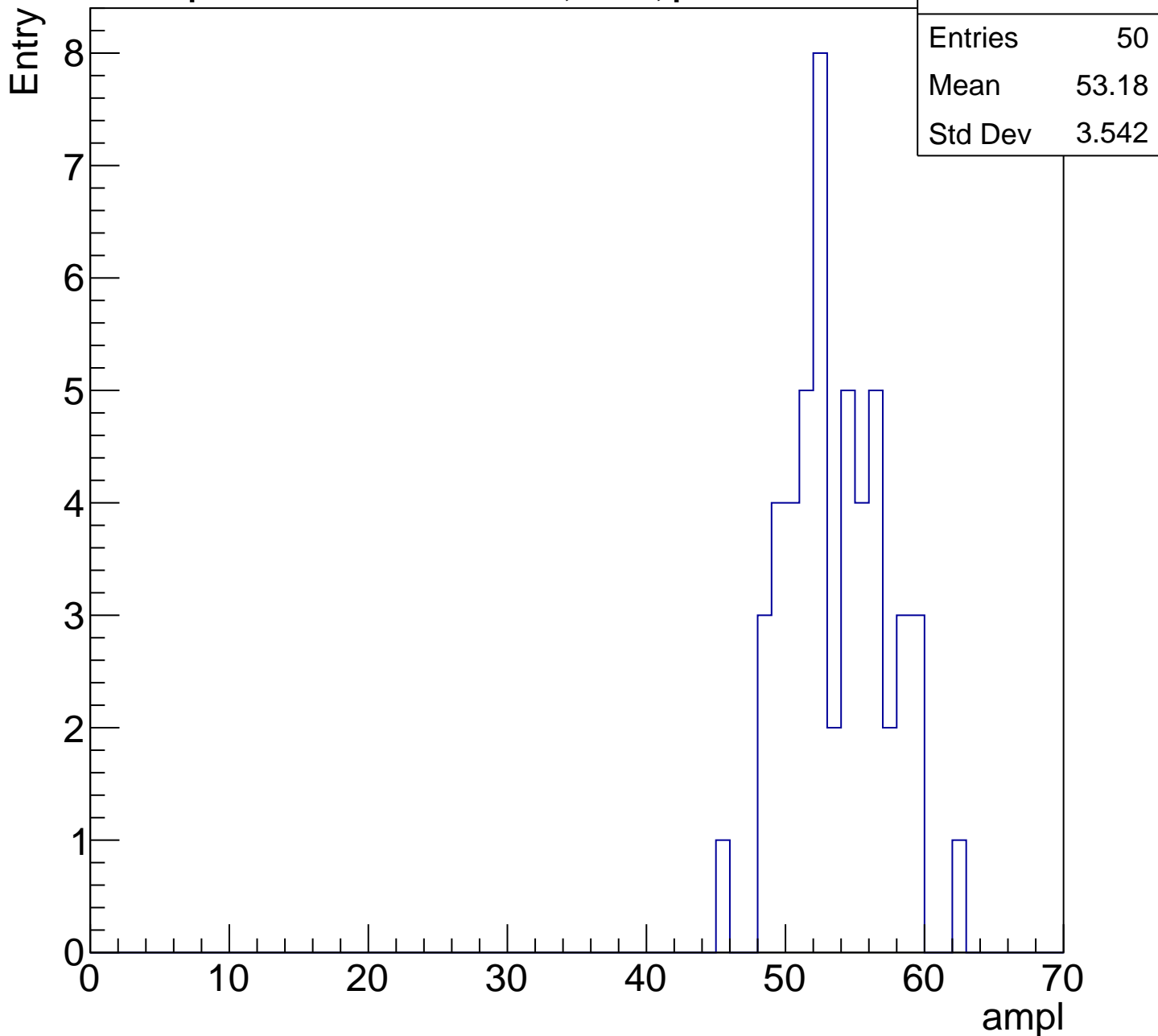
Entry

Entries	64
Mean	48
Std Dev	3.812



# B1L103S, U1-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

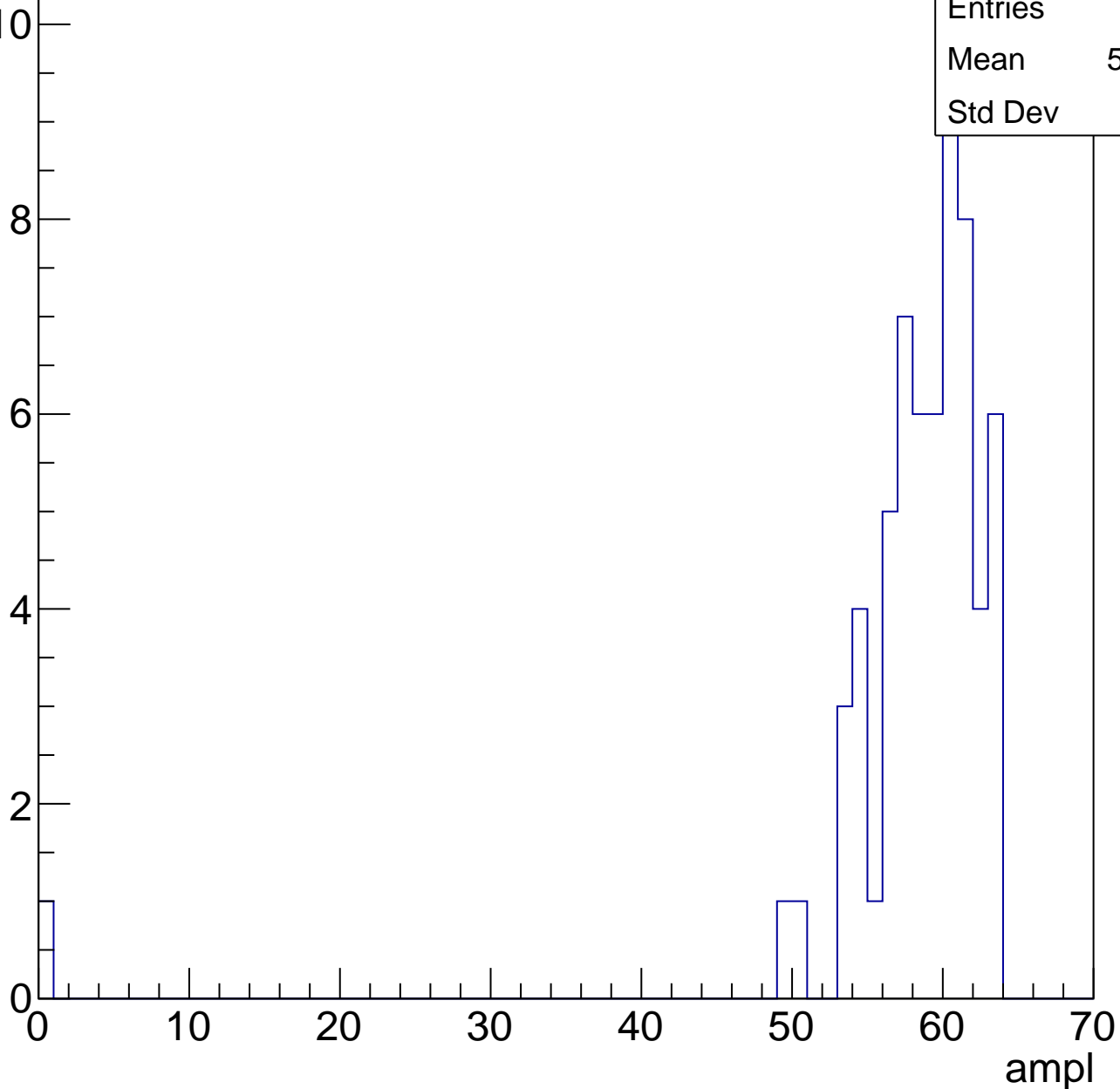


# B1L103S, U1-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

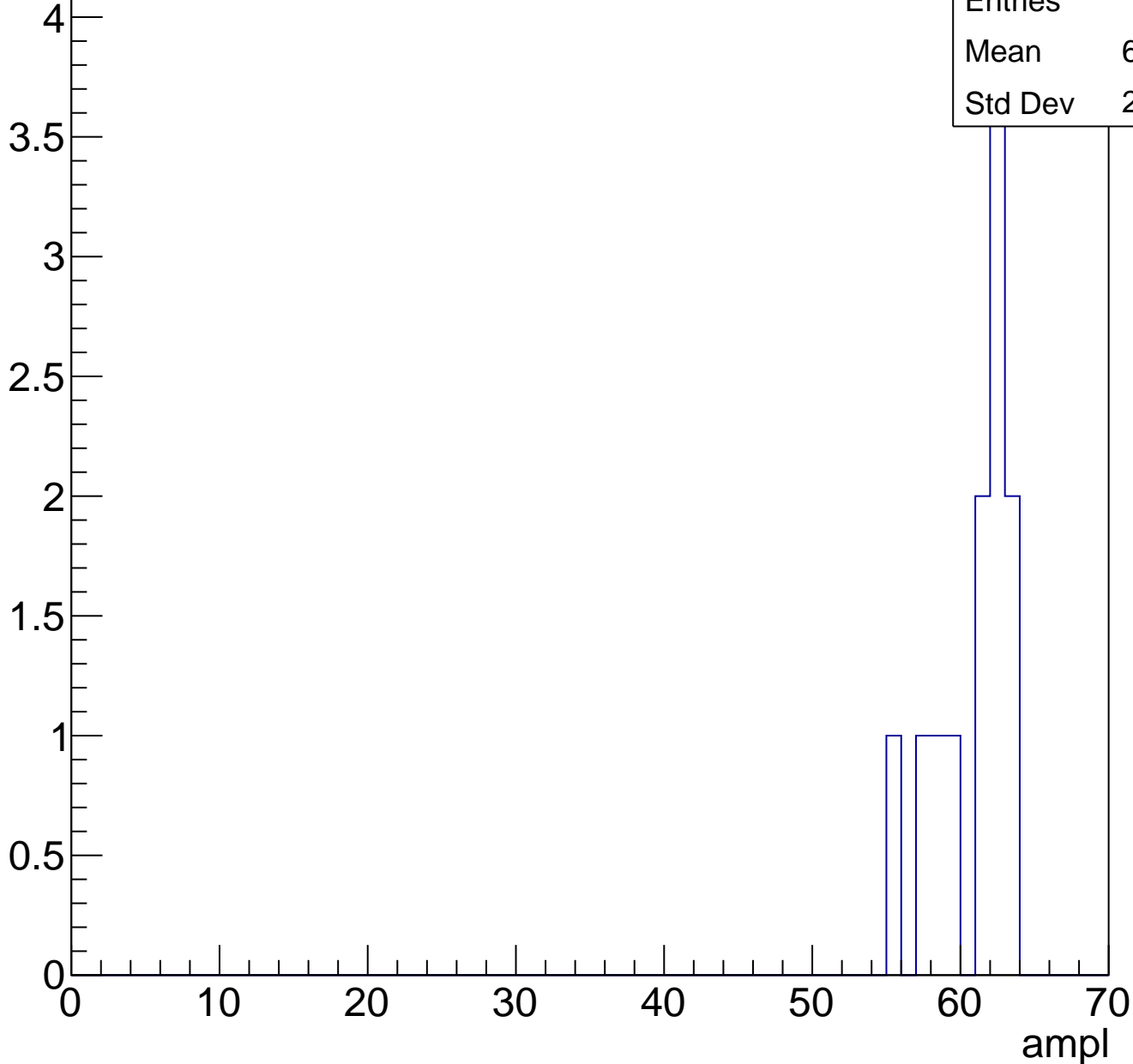
Entries	63
Mean	57.52
Std Dev	7.97



# B1L103S, U1-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



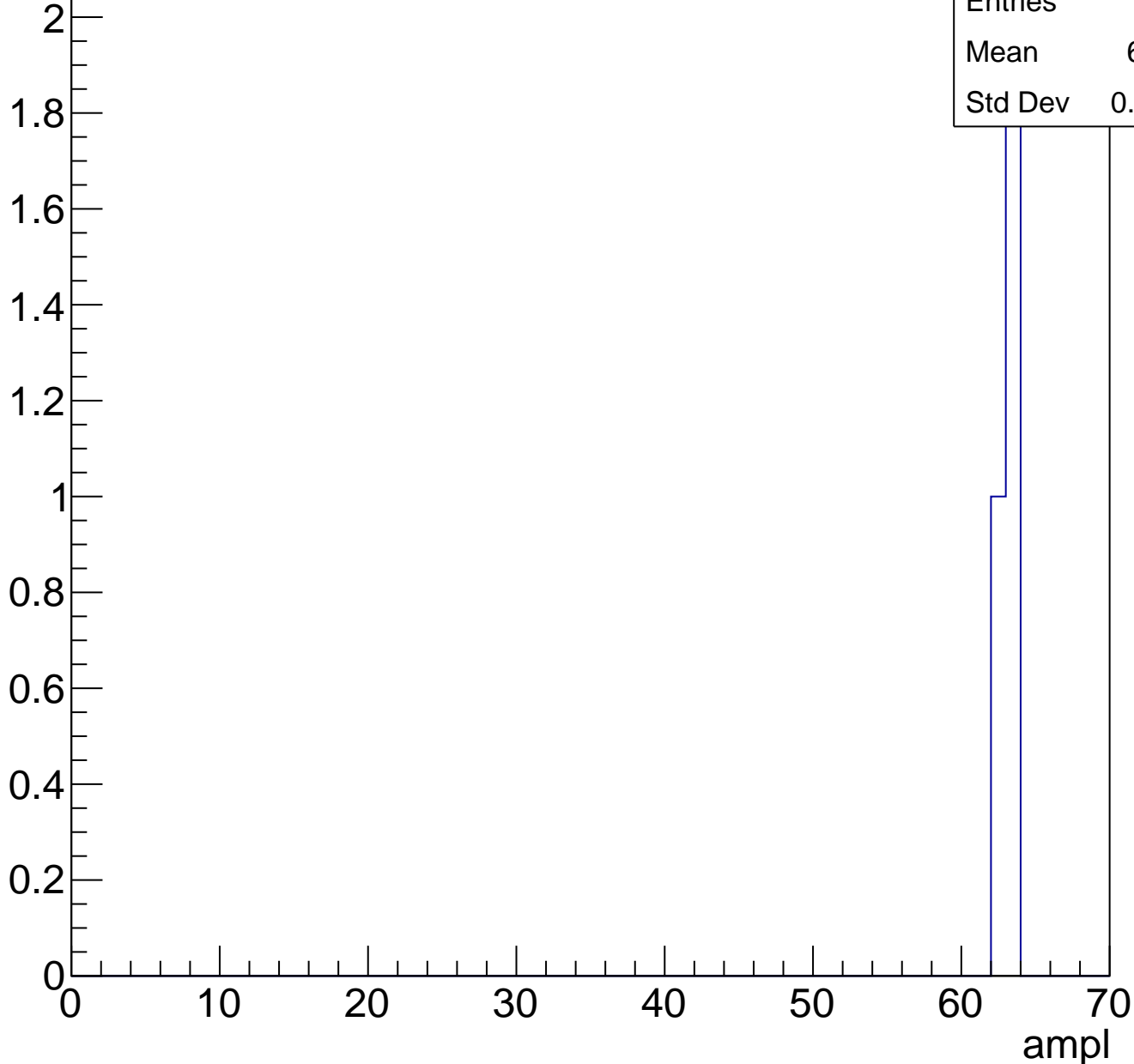
Entries	12
Mean	60.42
Std Dev	2.465



# B1L103S, U1-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch92, adc0

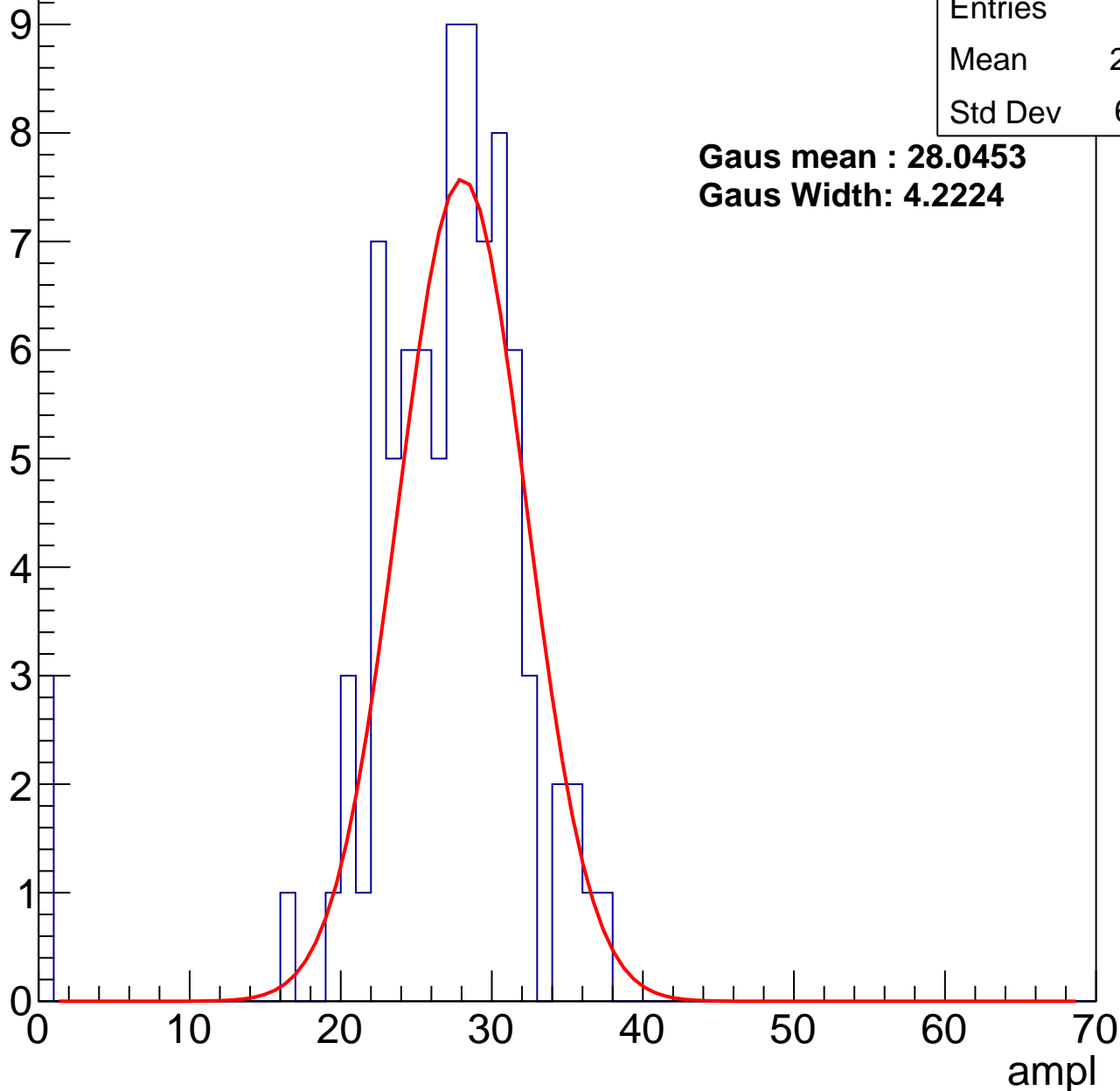
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	86
Mean	26.05
Std Dev	6.381

**Gaus mean : 28.0453**

**Gaus Width: 4.2224**



# B1L103S, U1-ch92, adc1

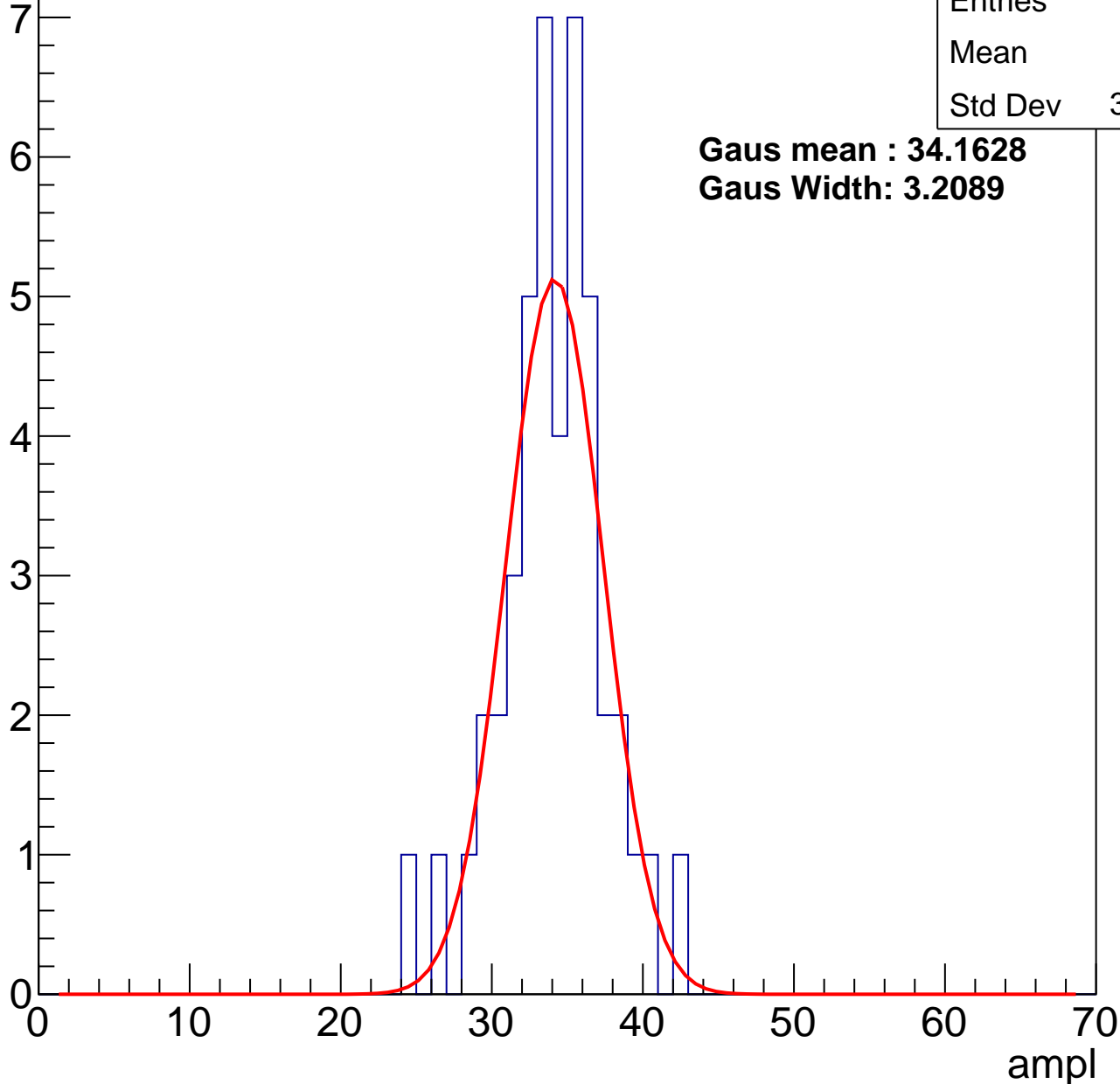
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	33.6
Std Dev	3.434

**Gaus mean : 34.1628**

**Gaus Width: 3.2089**



# B1L103S, U1-ch92, adc2

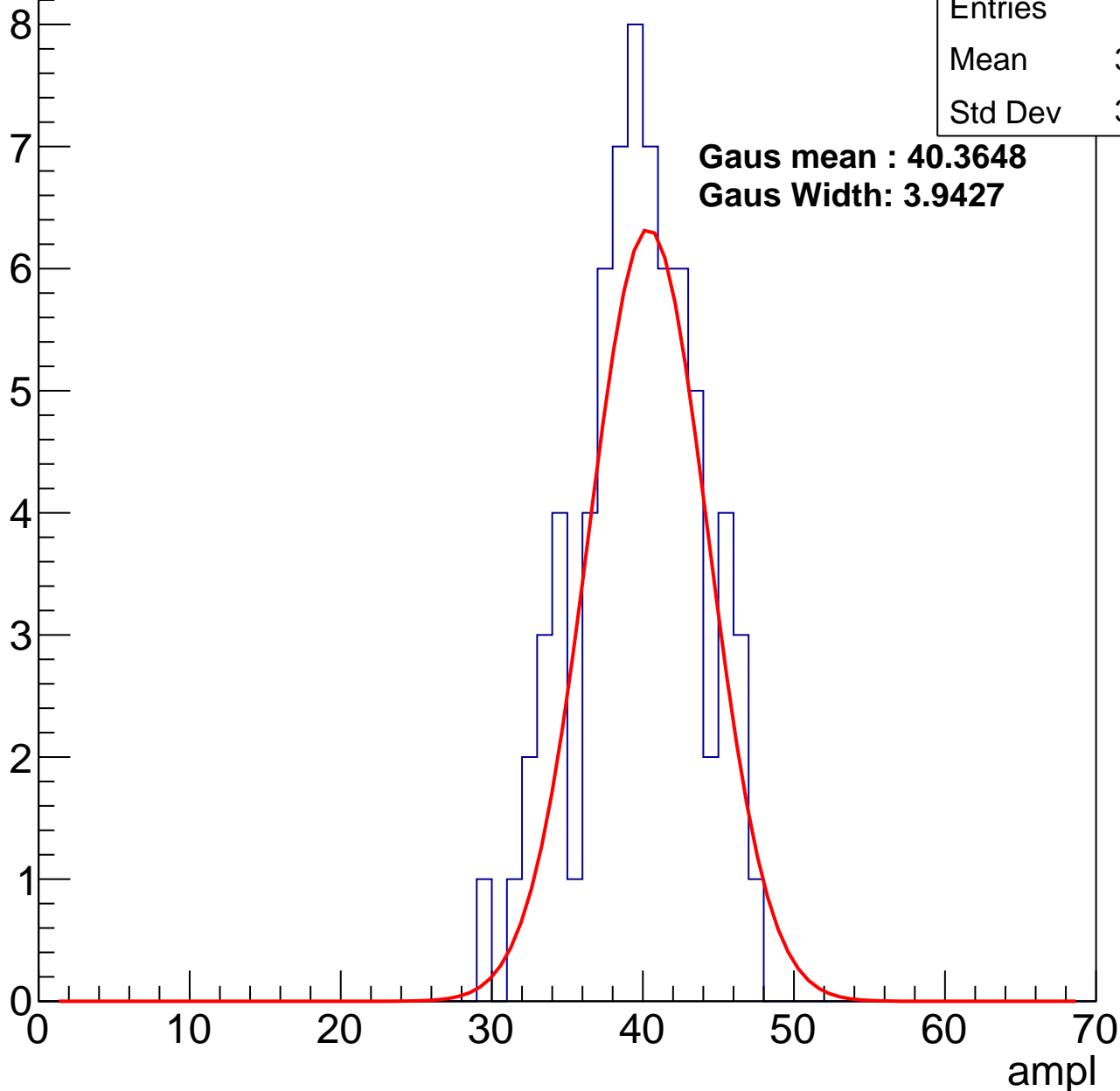
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	39.21
Std Dev	3.971

**Gaus mean : 40.3648**

**Gaus Width: 3.9427**

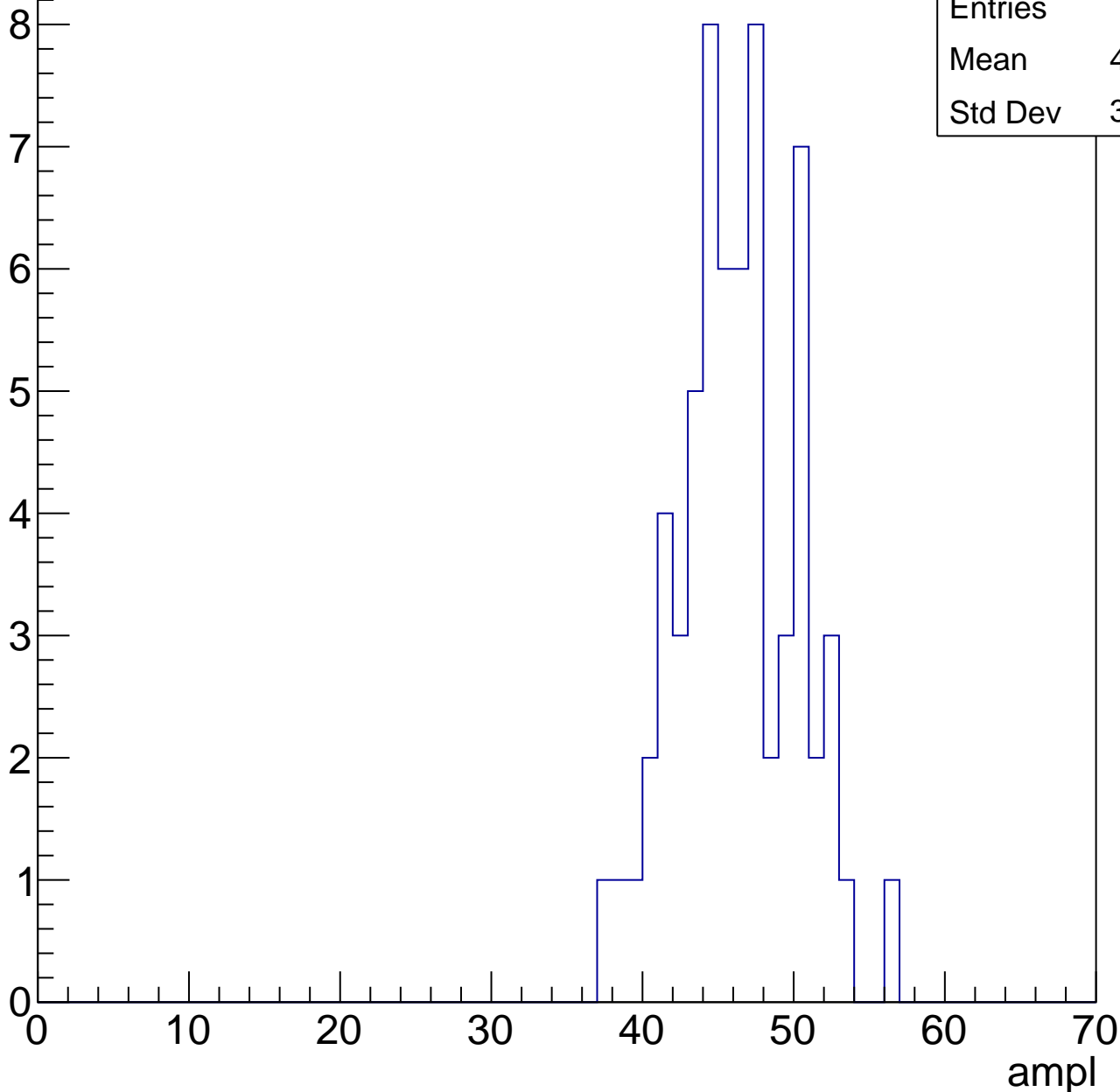


# B1L103S, U1-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	45.83
Std Dev	3.867

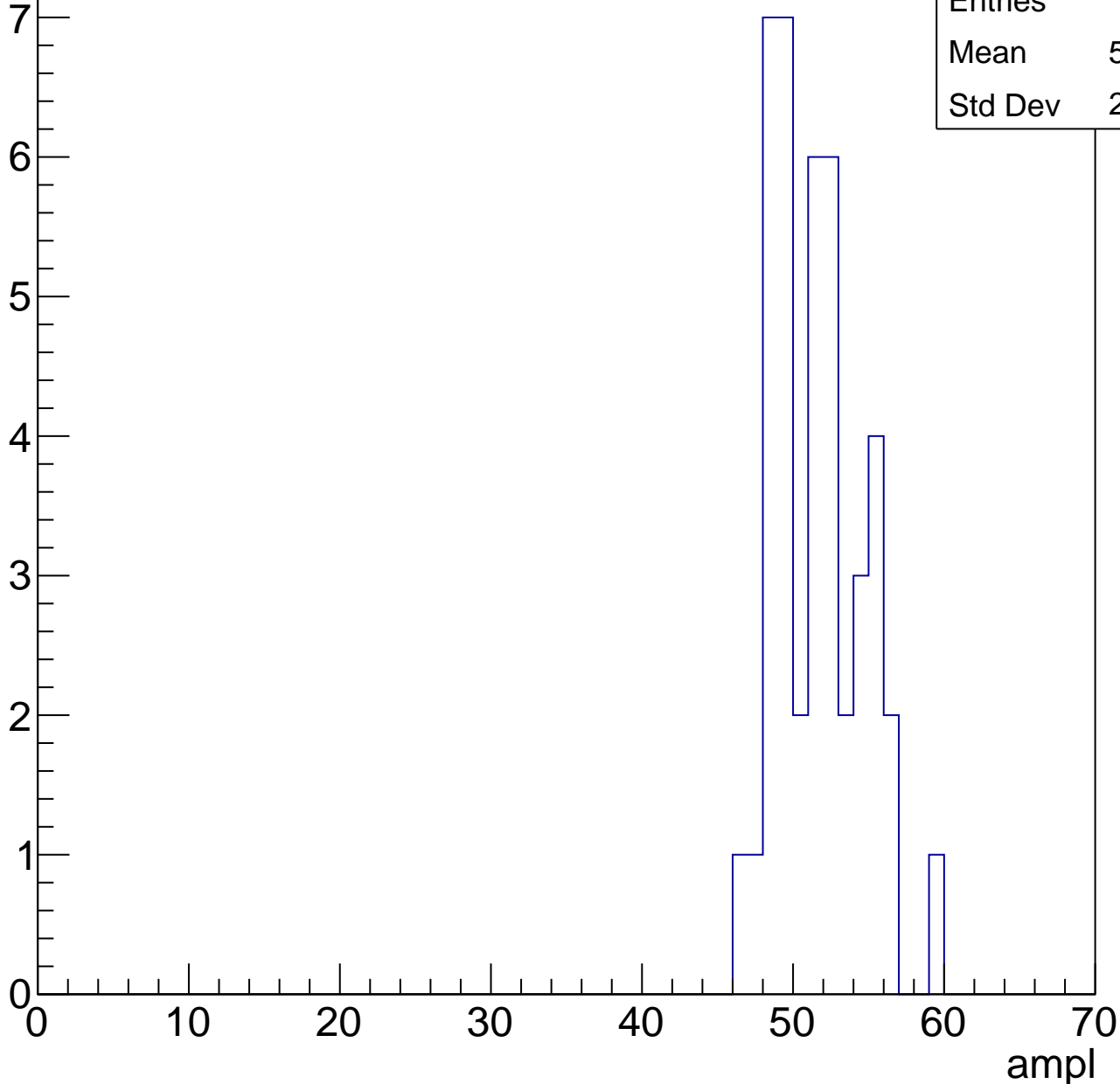


# B1L103S, U1-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

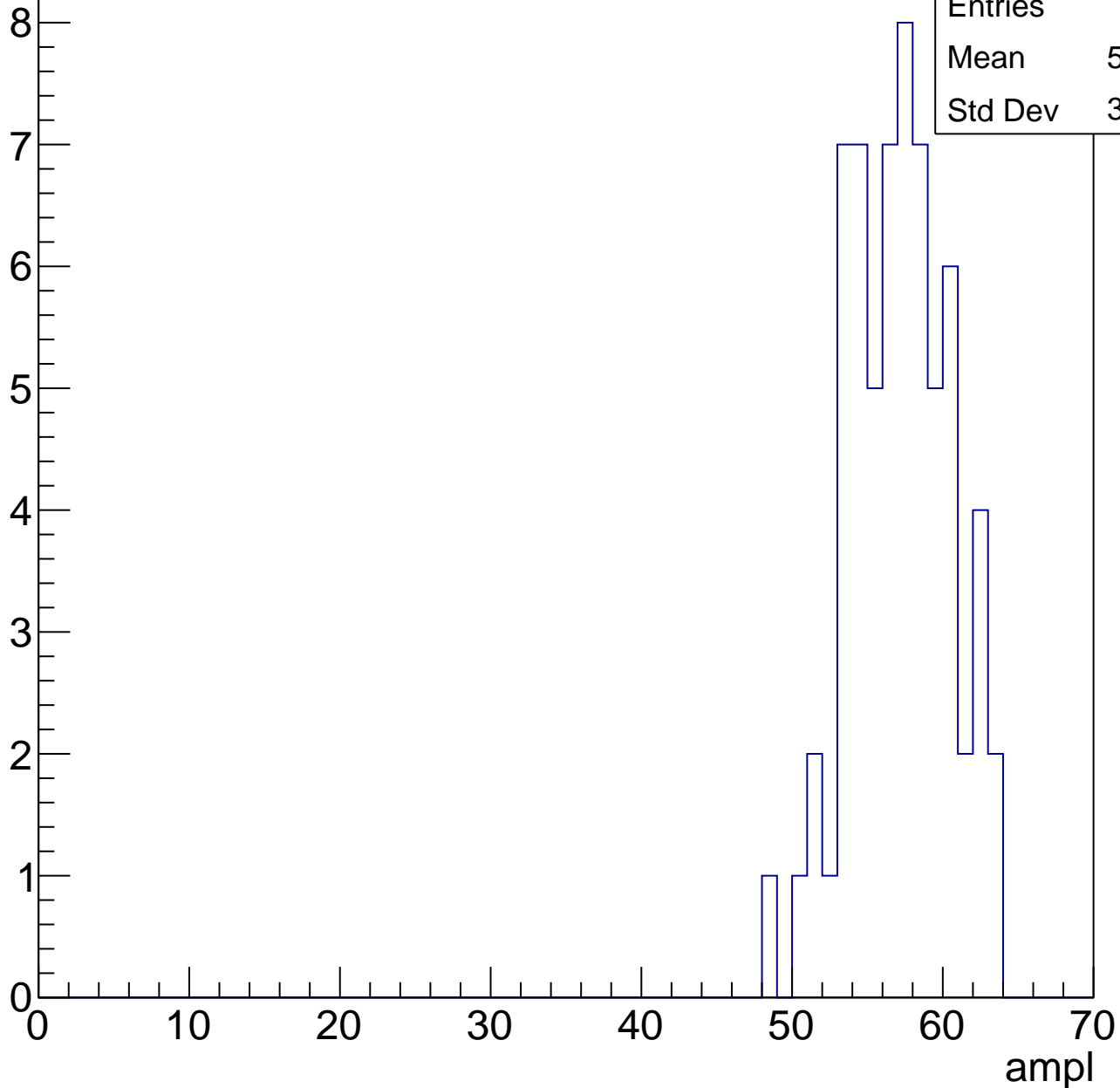
Entries	42
Mean	51.17
Std Dev	2.894



# B1L103S, U1-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



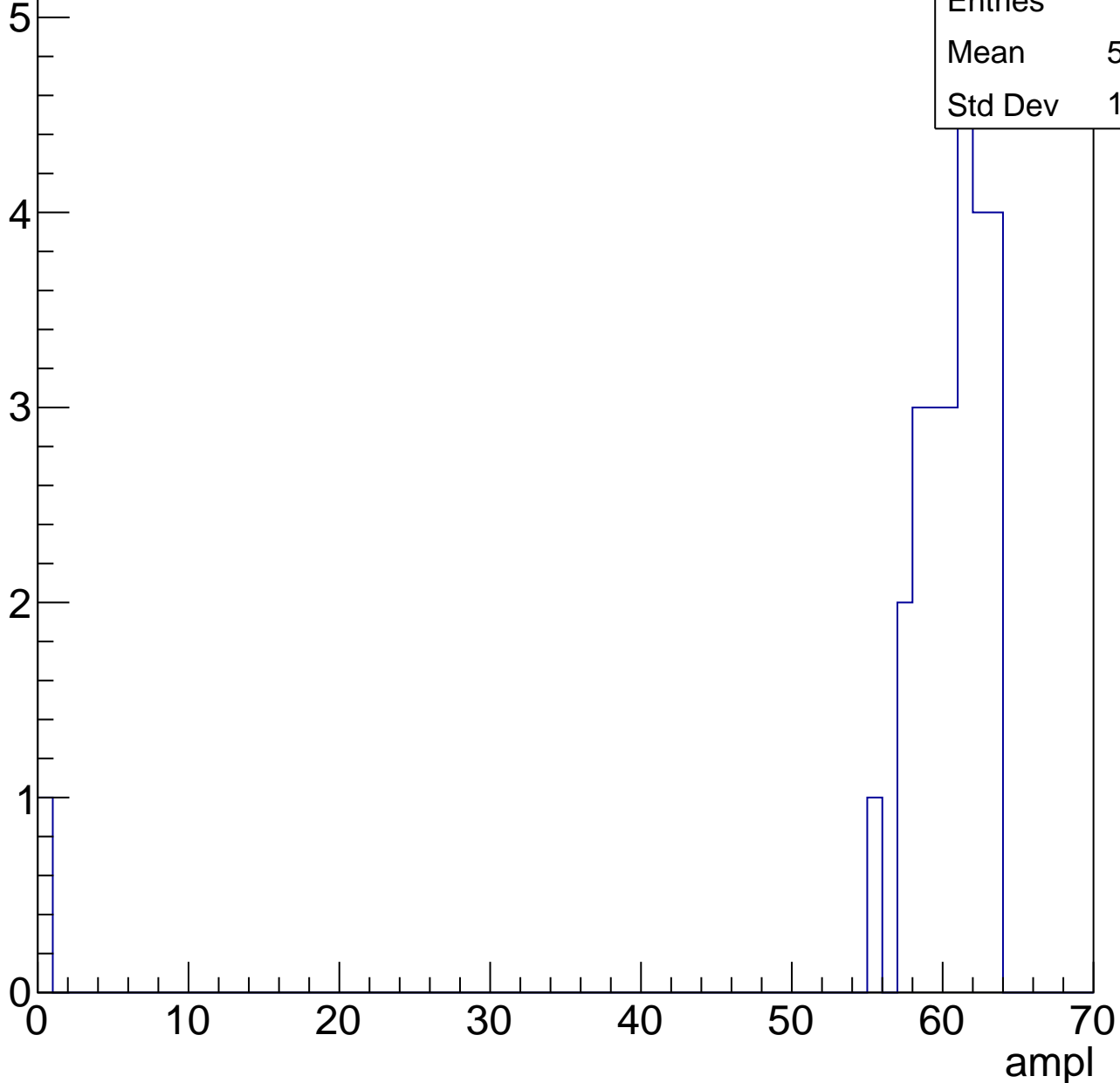
Entries	65
Mean	56.63
Std Dev	3.294

# B1L103S, U1-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	26
Mean	57.88
Std Dev	11.76

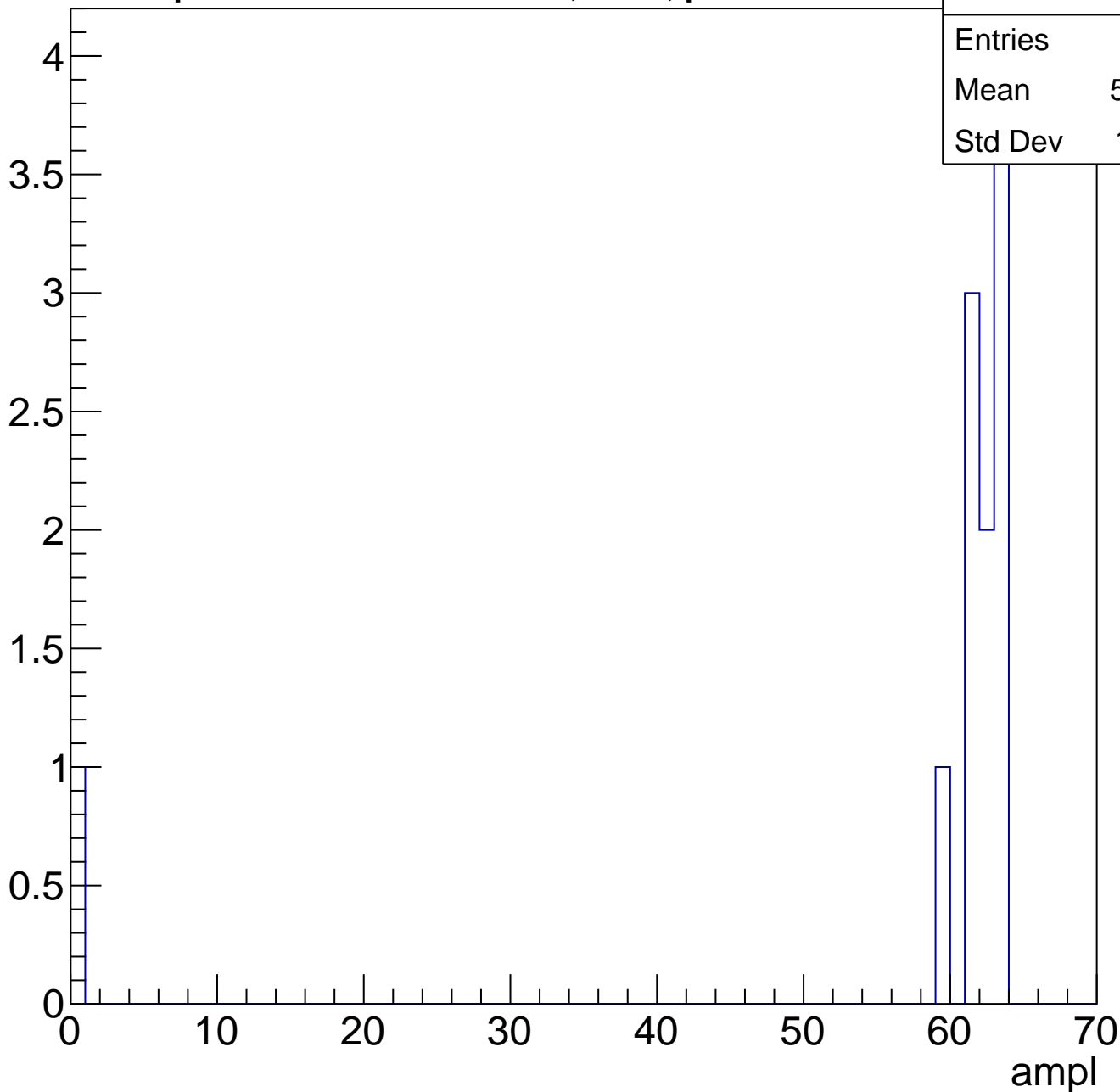




# B1L103S, U1-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch93, adc0

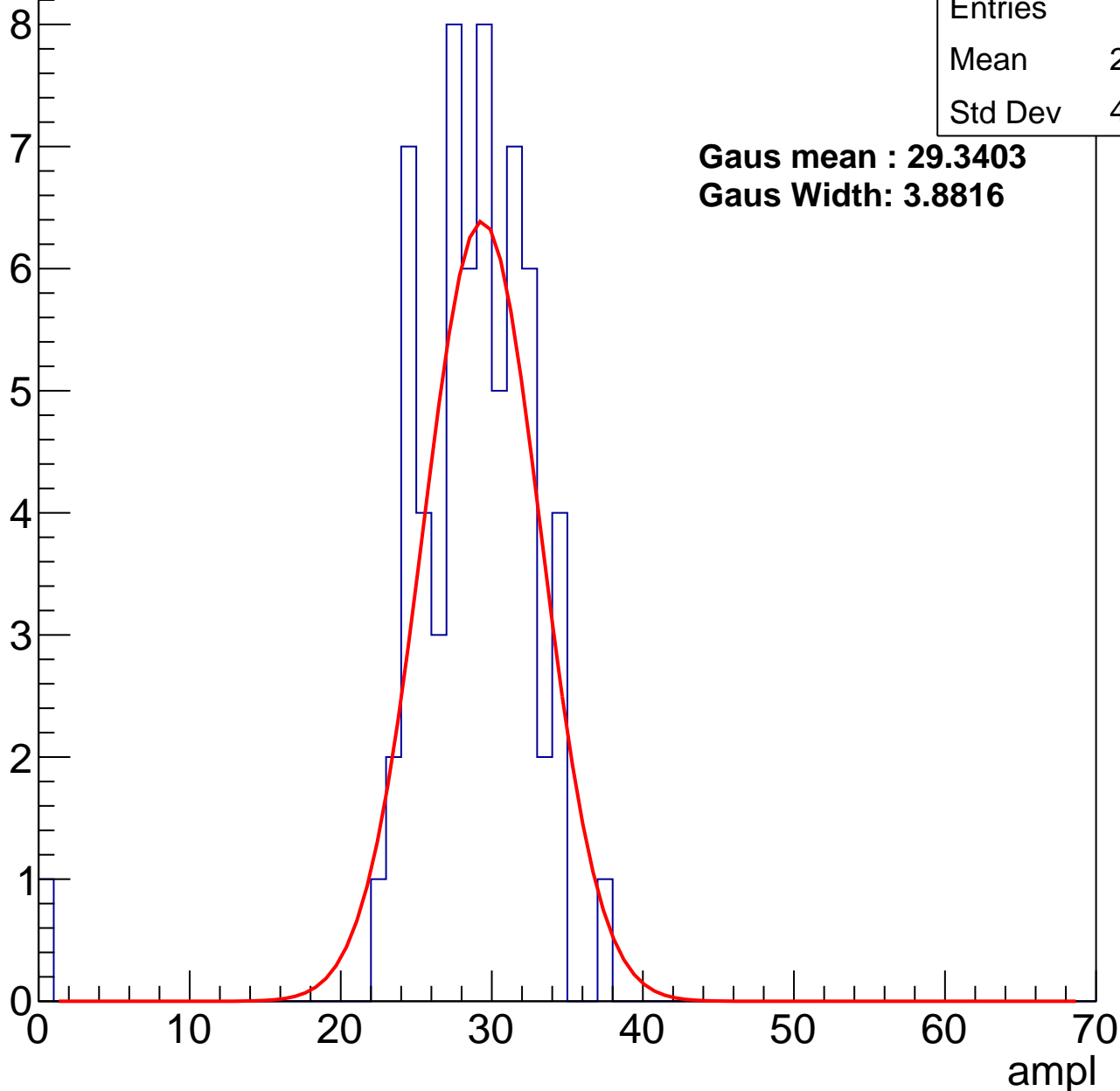
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	28.12
Std Dev	4.802

**Gaus mean : 29.3403**

**Gaus Width: 3.8816**



# B1L103S, U1-ch93, adc1

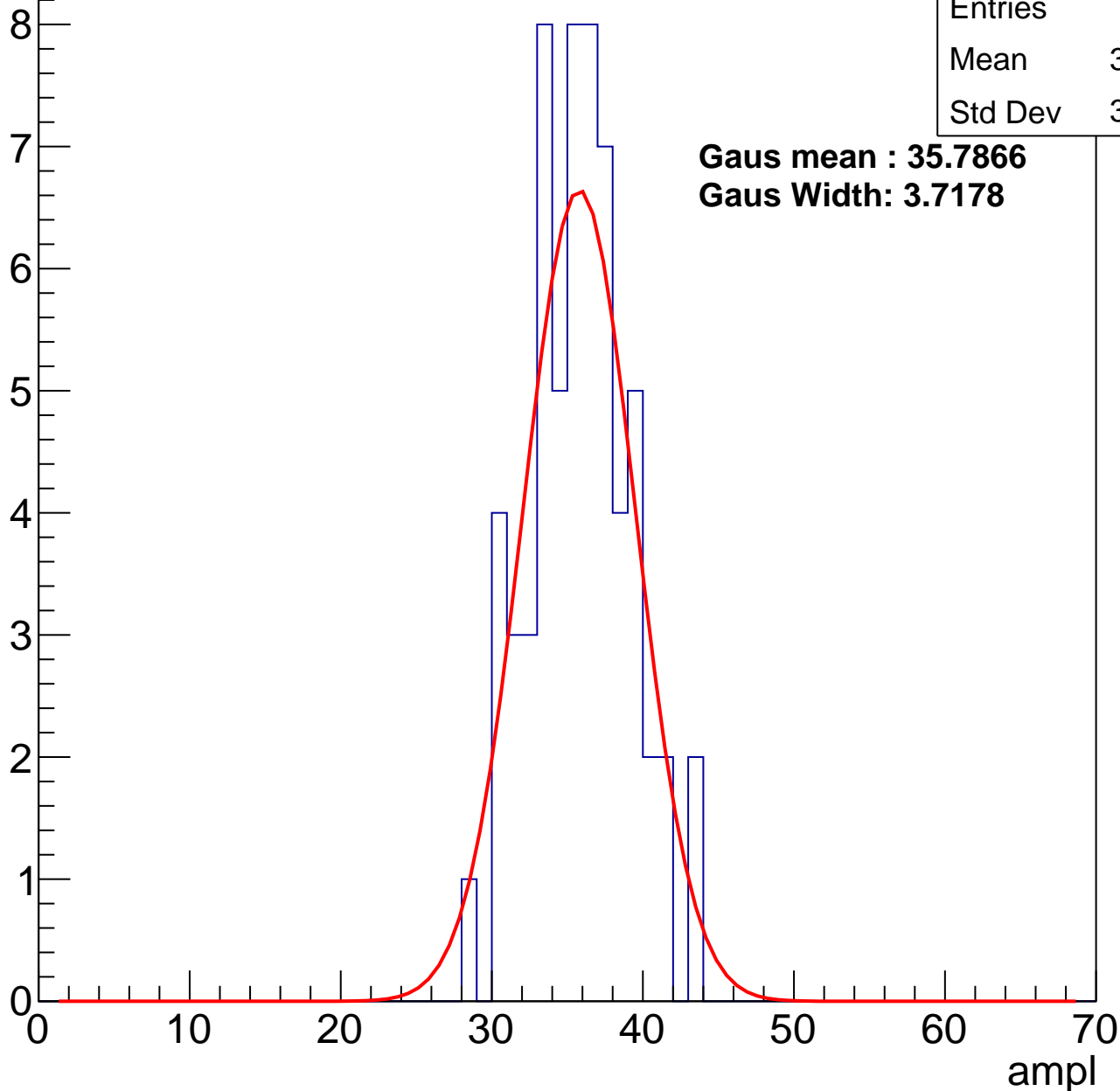
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	35.37
Std Dev	3.249

**Gaus mean : 35.7866**

**Gaus Width: 3.7178**



# B1L103S, U1-ch93, adc2

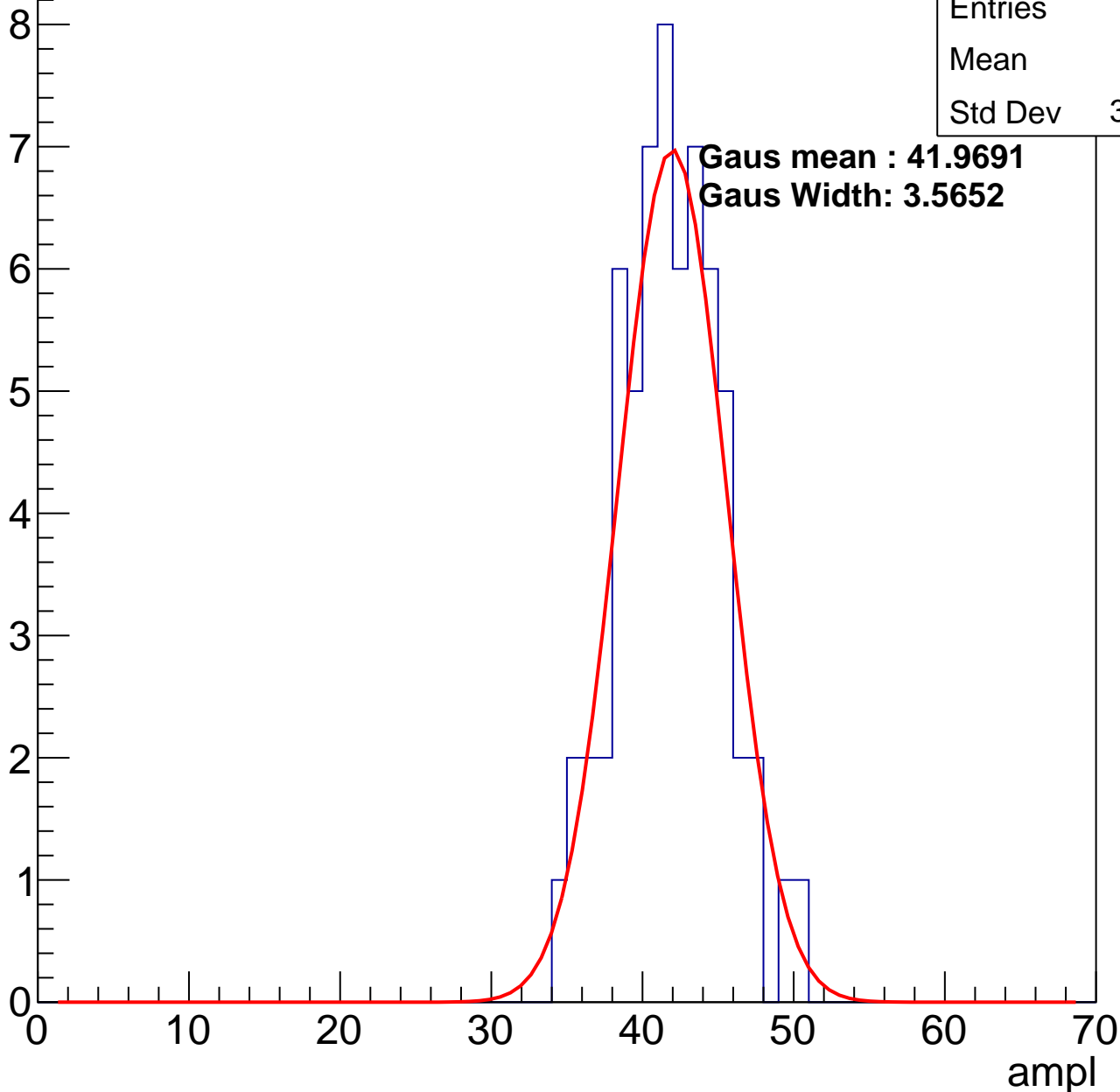
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	41.4
Std Dev	3.355

**Gaus mean : 41.9691**

**Gaus Width: 3.5652**

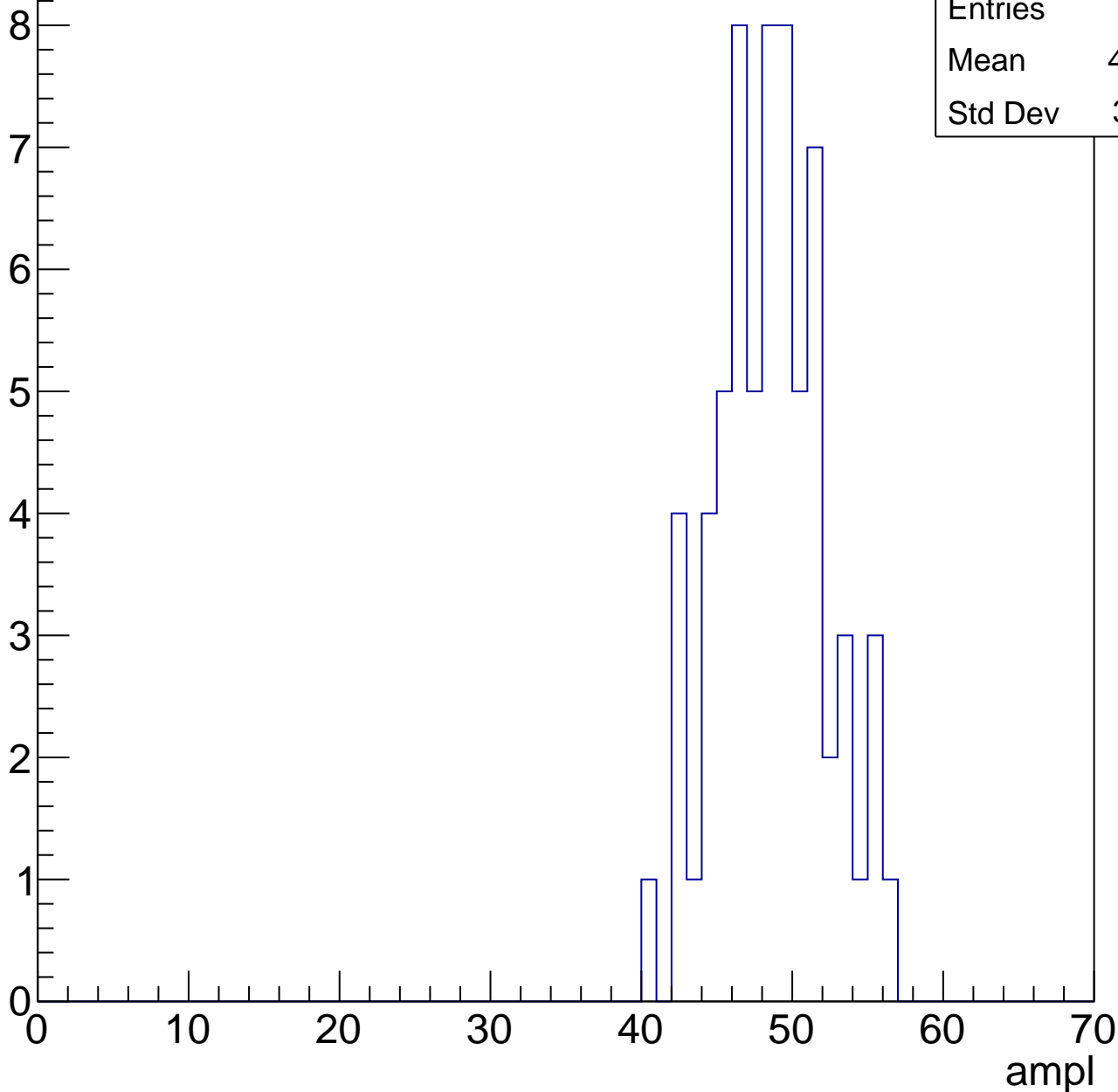


# B1L103S, U1-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	48.12
Std Dev	3.531

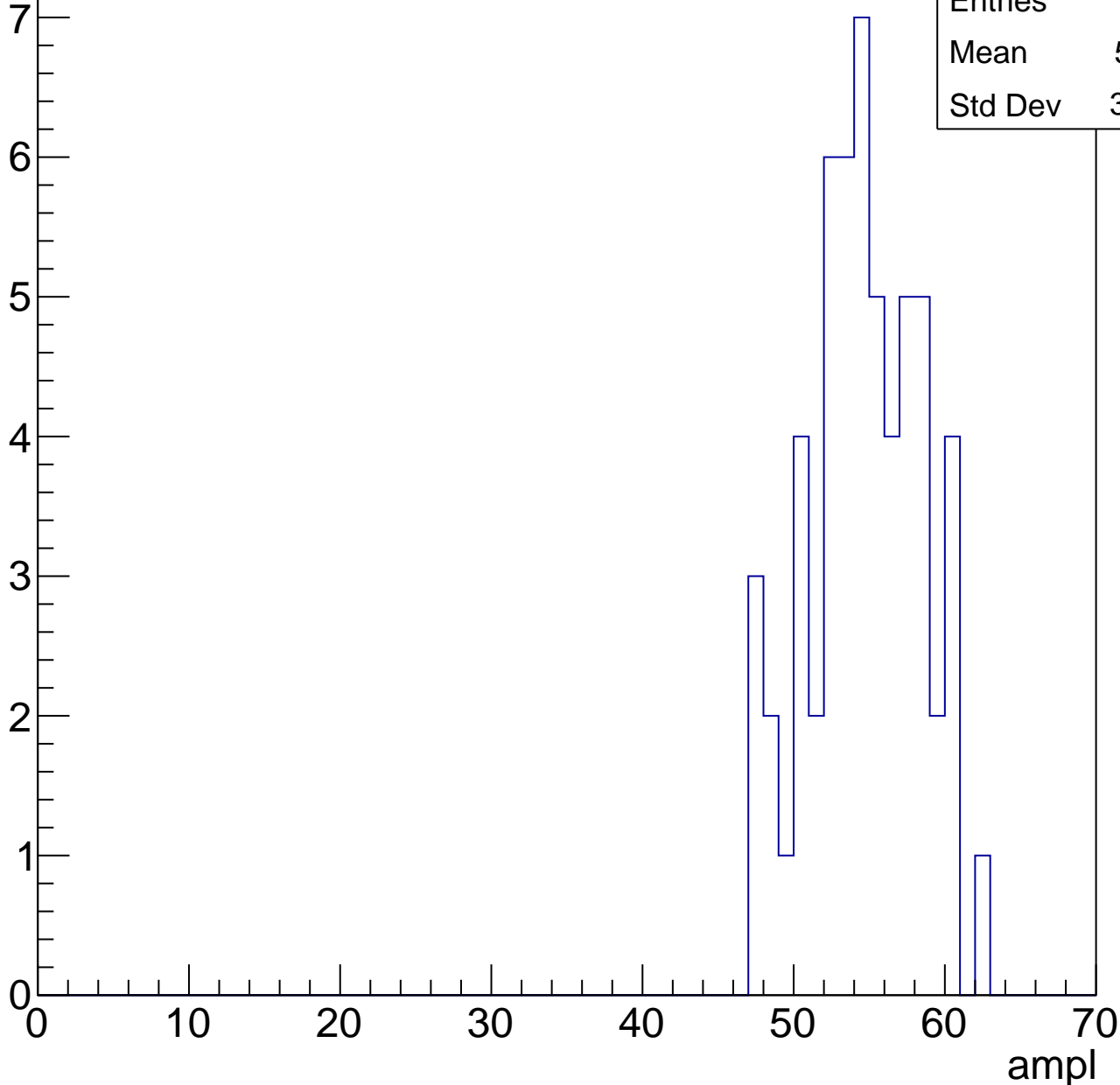


# B1L103S, U1-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	54.21
Std Dev	3.645

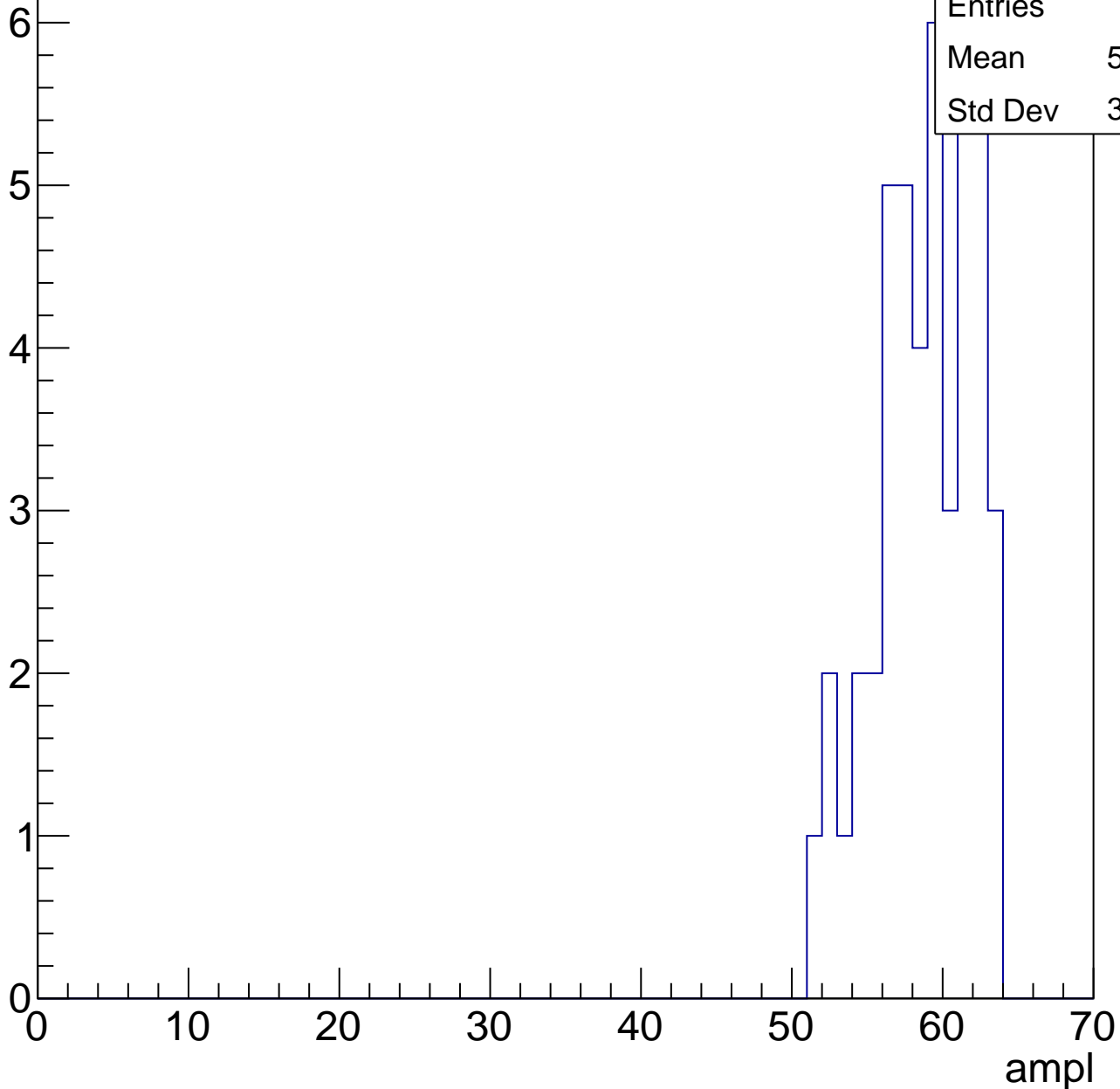


# B1L103S, U1-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	58.35
Std Dev	3.157

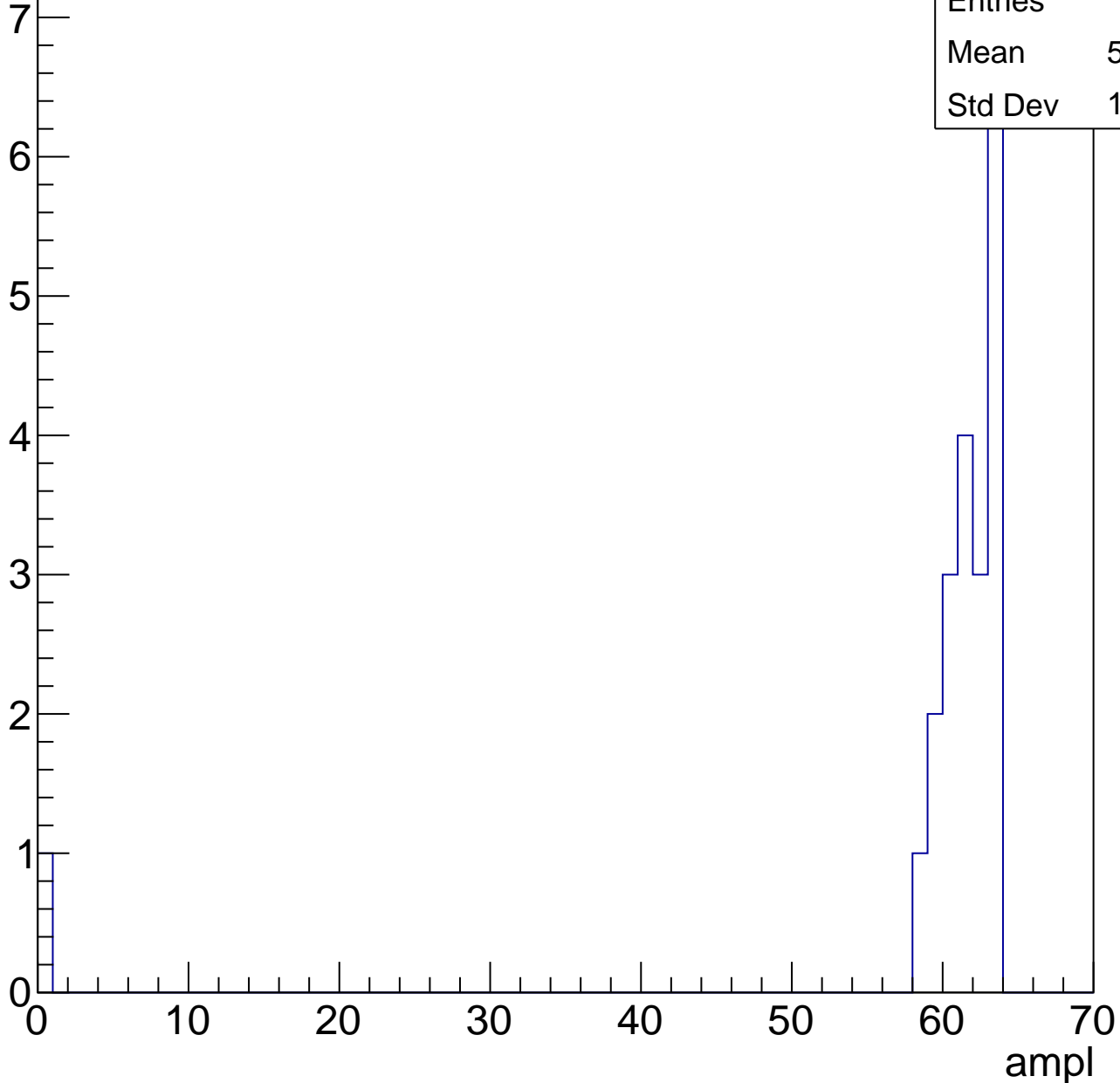


# B1L103S, U1-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	21
Mean	58.43
Std Dev	13.15





# B1L103S, U1-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U1-ch94, adc0

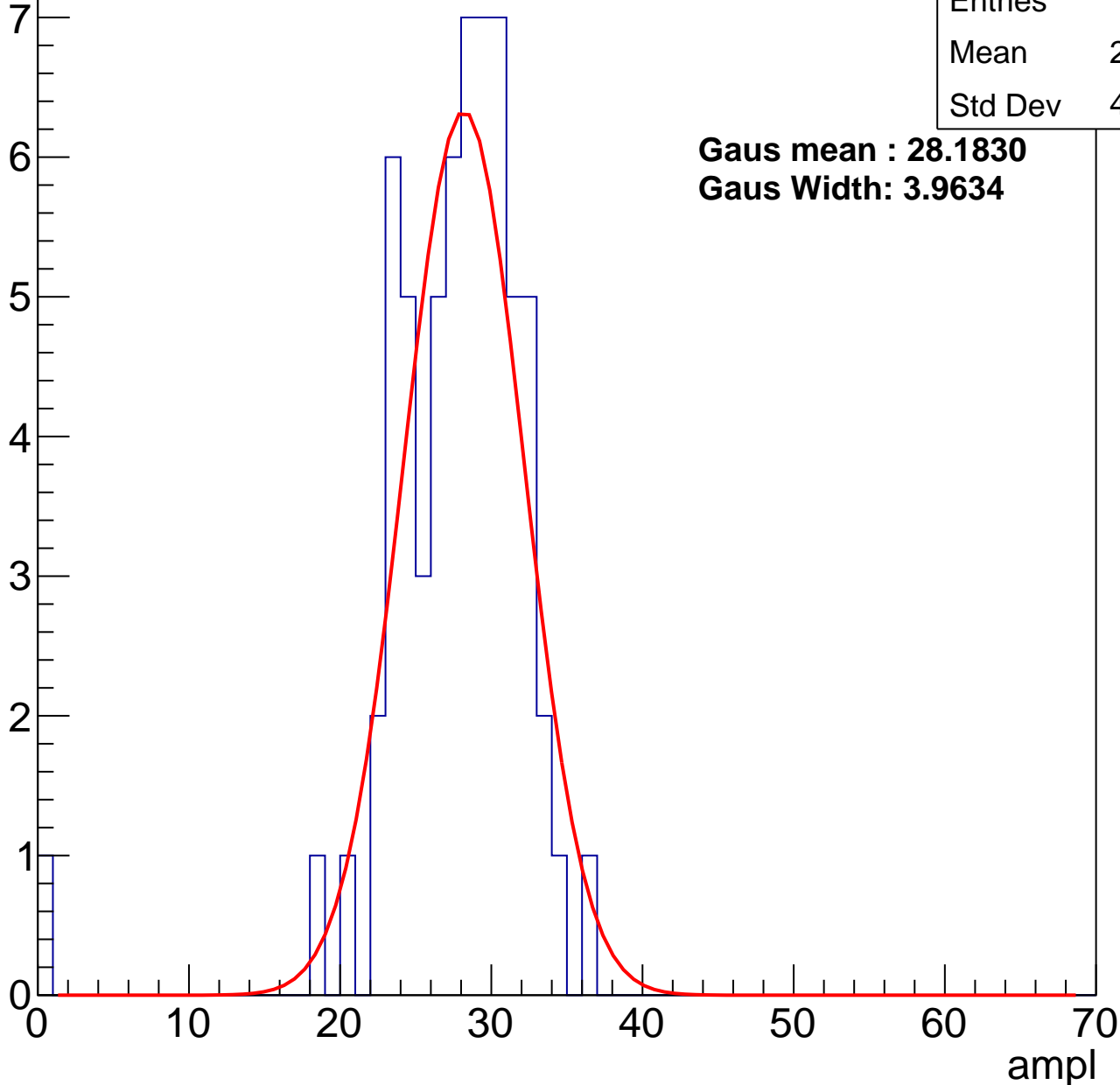
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	27.18
Std Dev	4.914

**Gaus mean : 28.1830**

**Gaus Width: 3.9634**



# B1L103S, U1-ch94, adc1

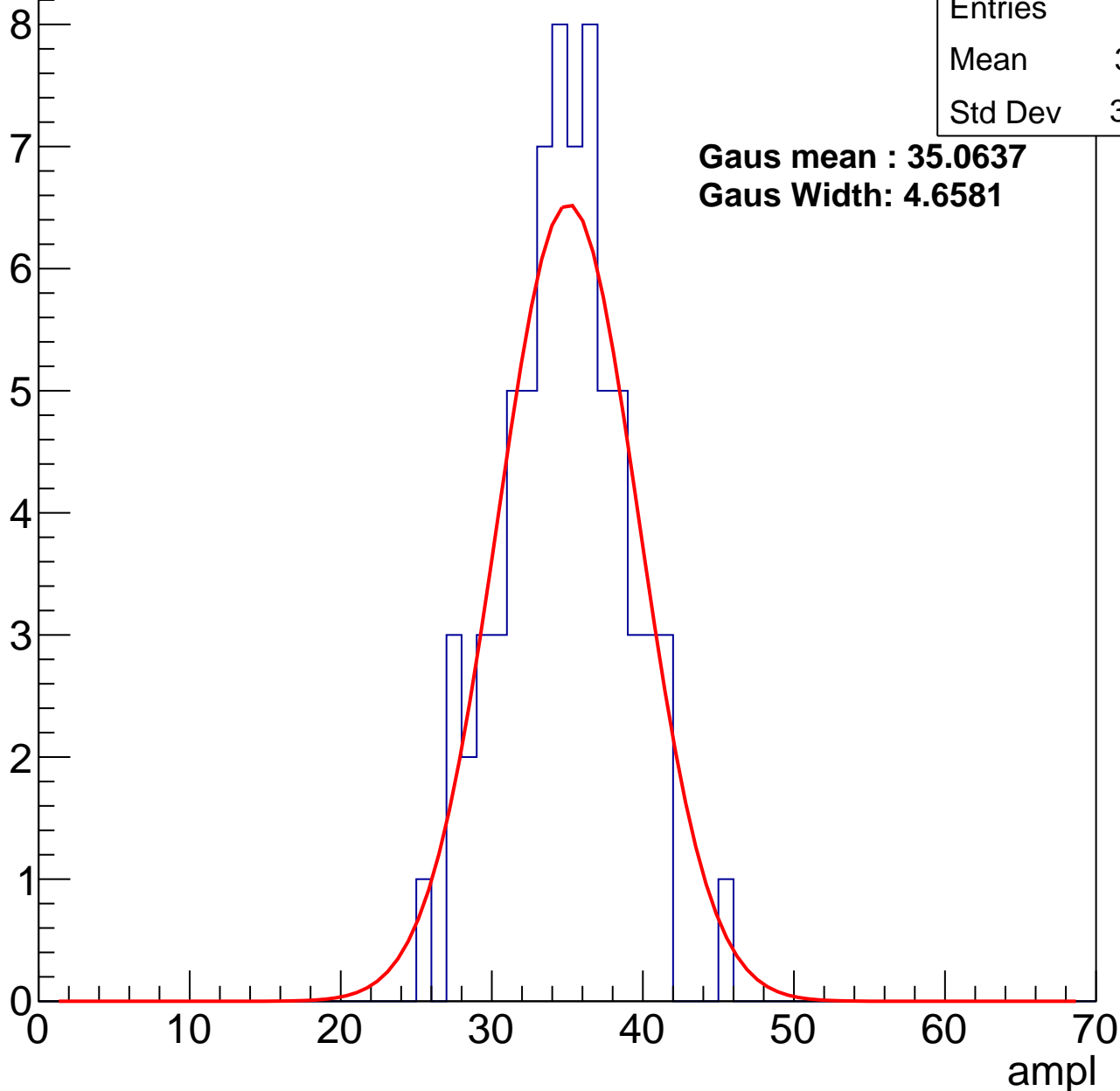
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	34.31
Std Dev	3.914

**Gaus mean : 35.0637**

**Gaus Width: 4.6581**



# B1L103S, U1-ch94, adc2

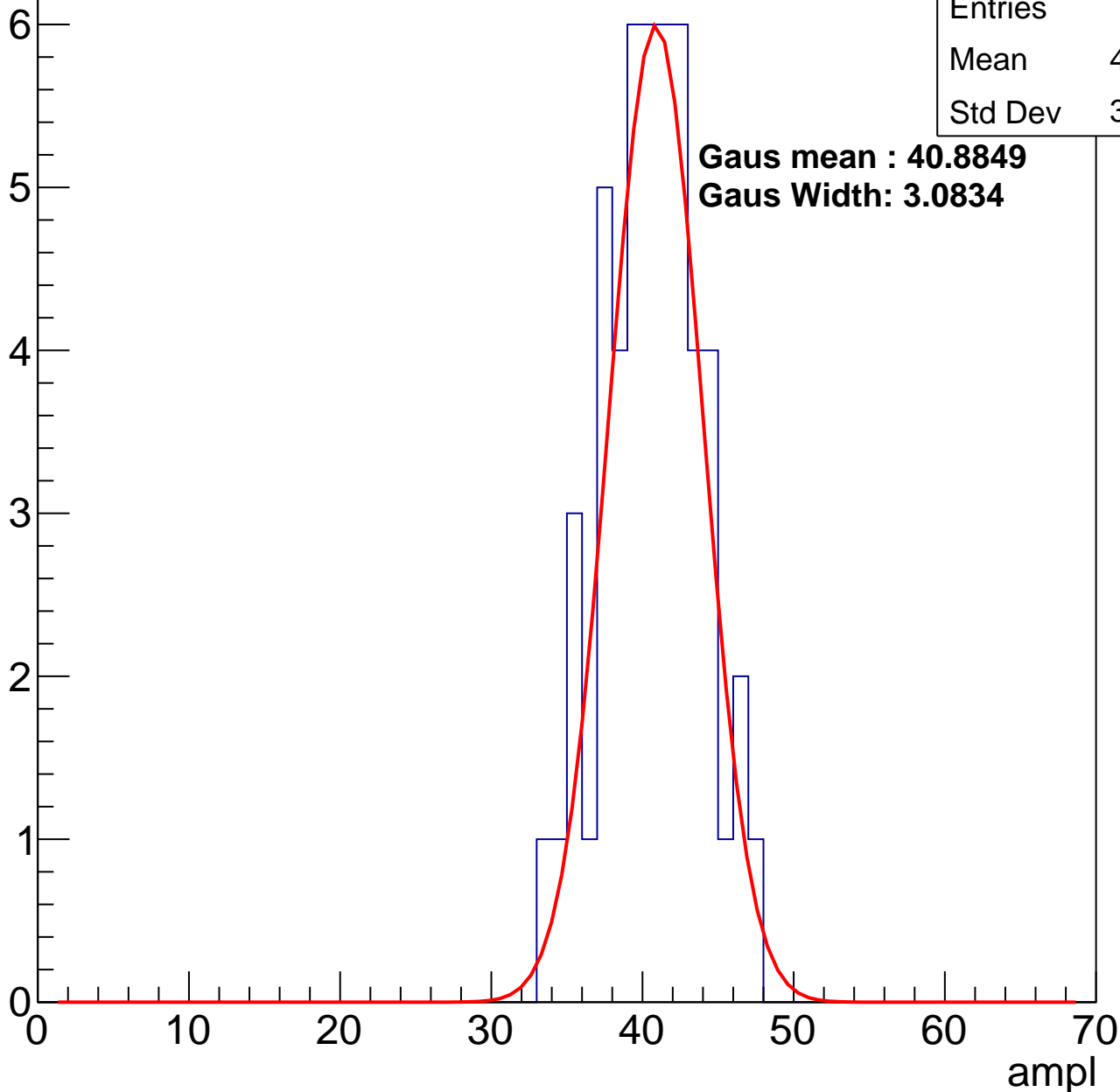
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	40.18
Std Dev	3.185

**Gaus mean : 40.8849**

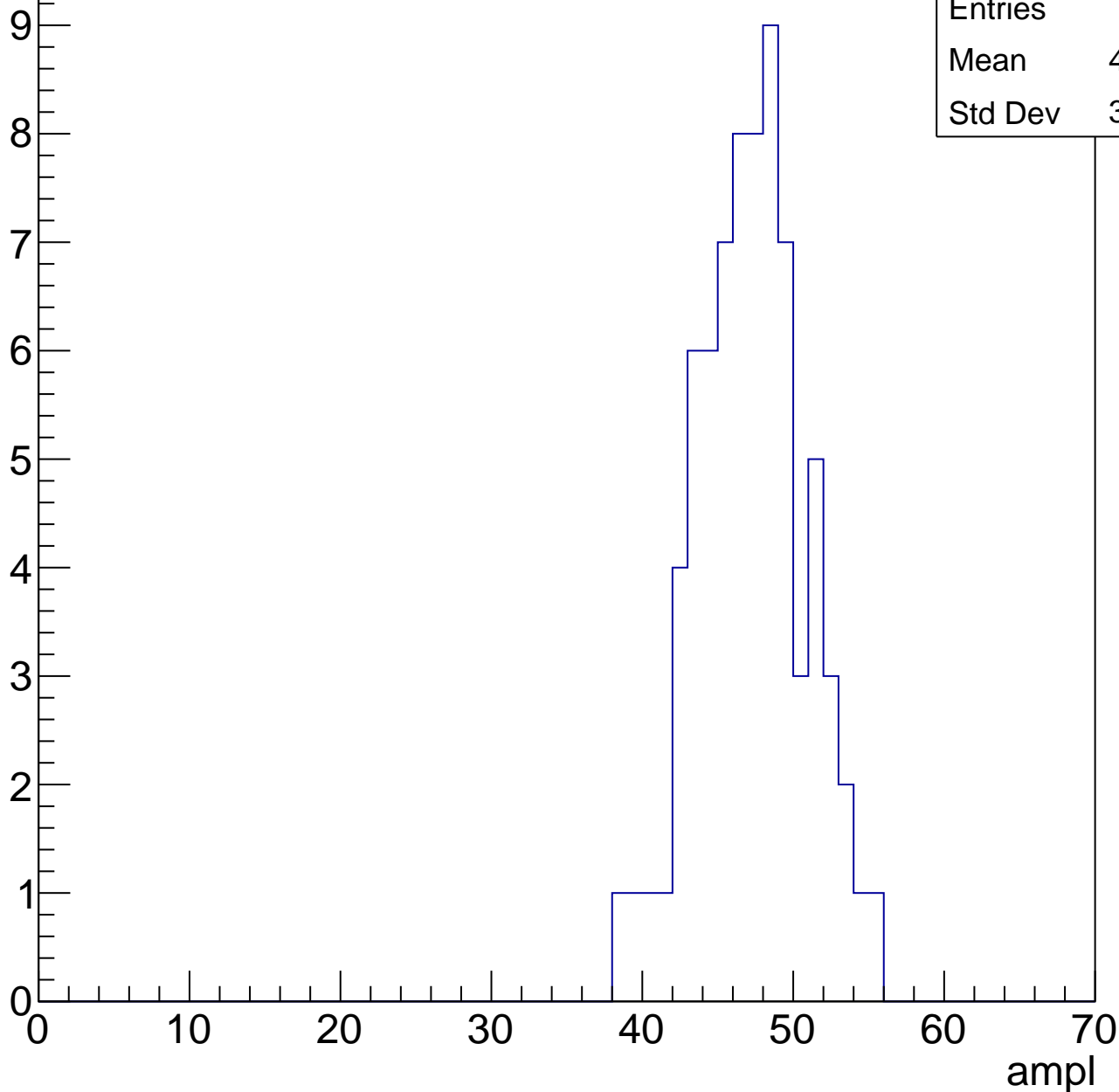
**Gaus Width: 3.0834**



# B1L103S, U1-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

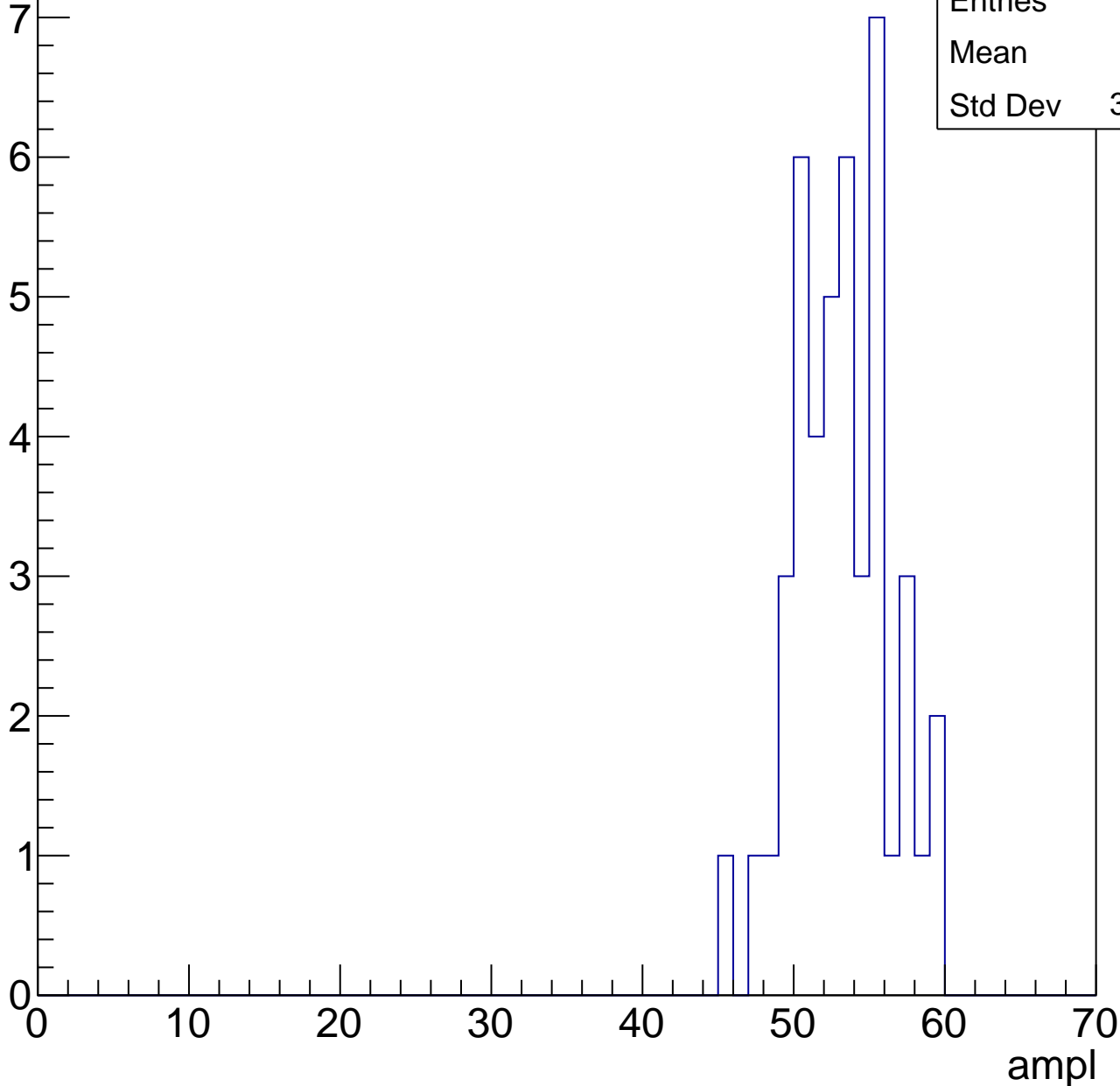


# B1L103S, U1-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	52.7
Std Dev	3.123

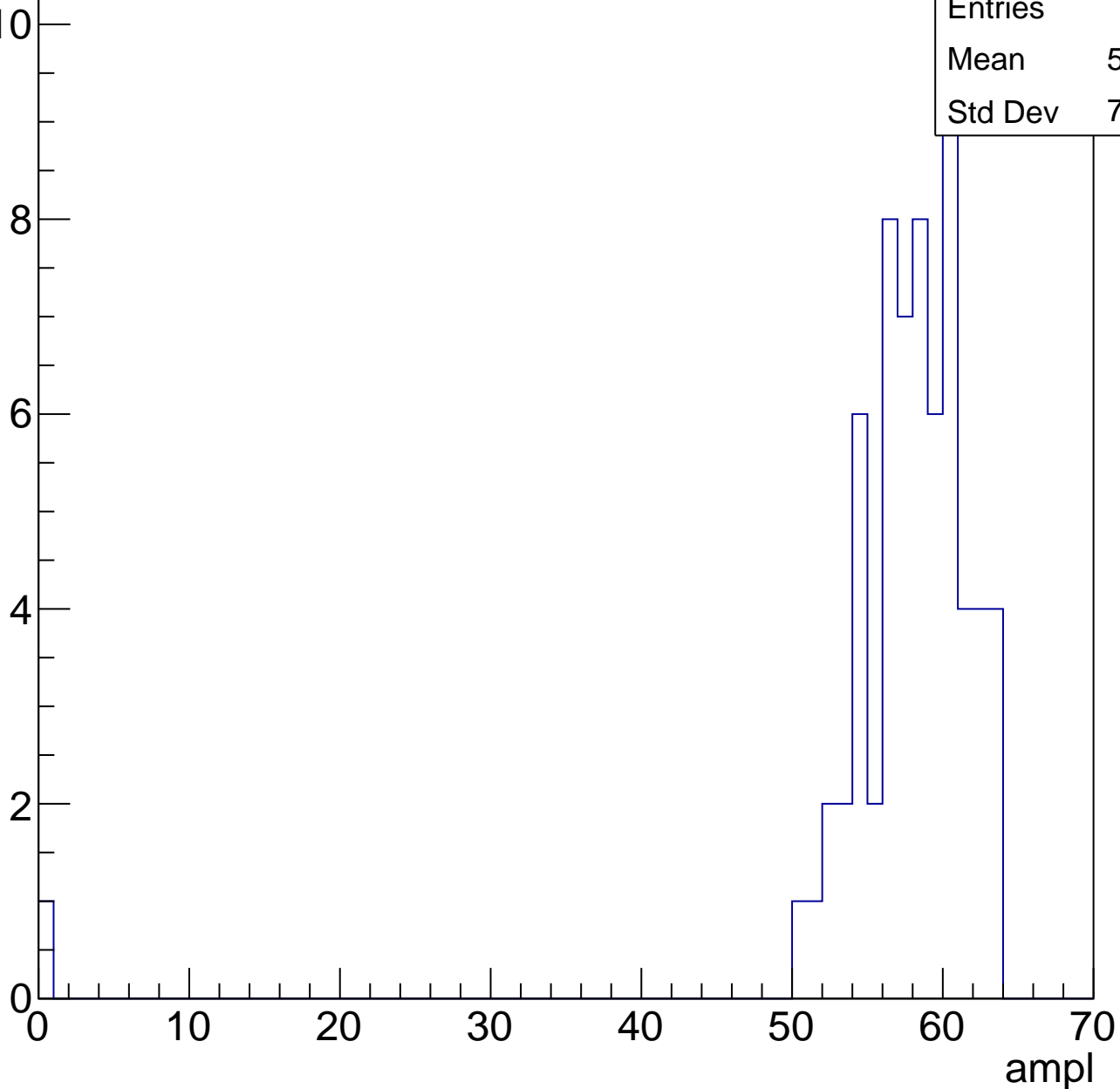


# B1L103S, U1-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	56.88
Std Dev	7.702

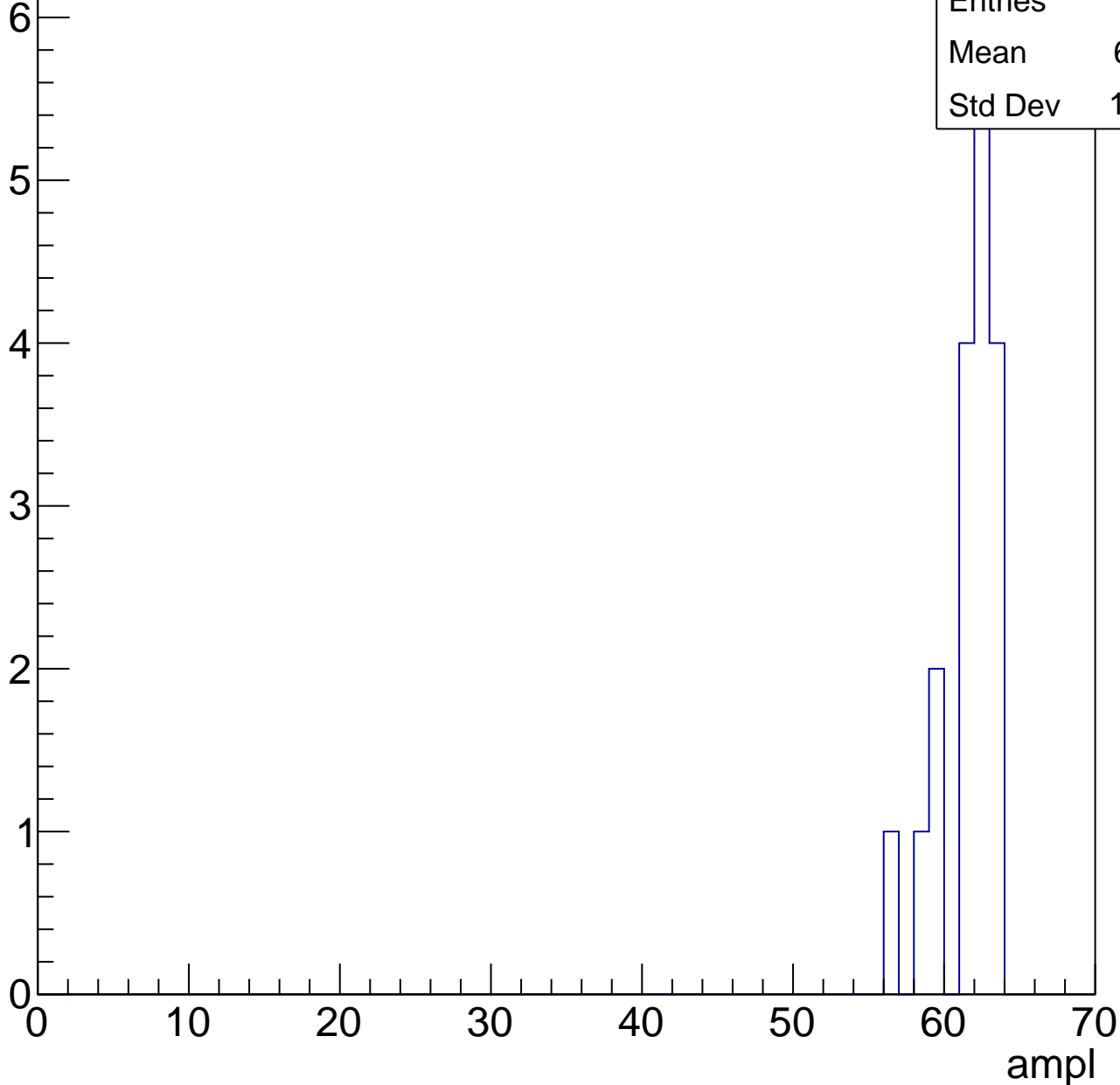


# B1L103S, U1-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	18
Mean	61.11
Std Dev	1.882

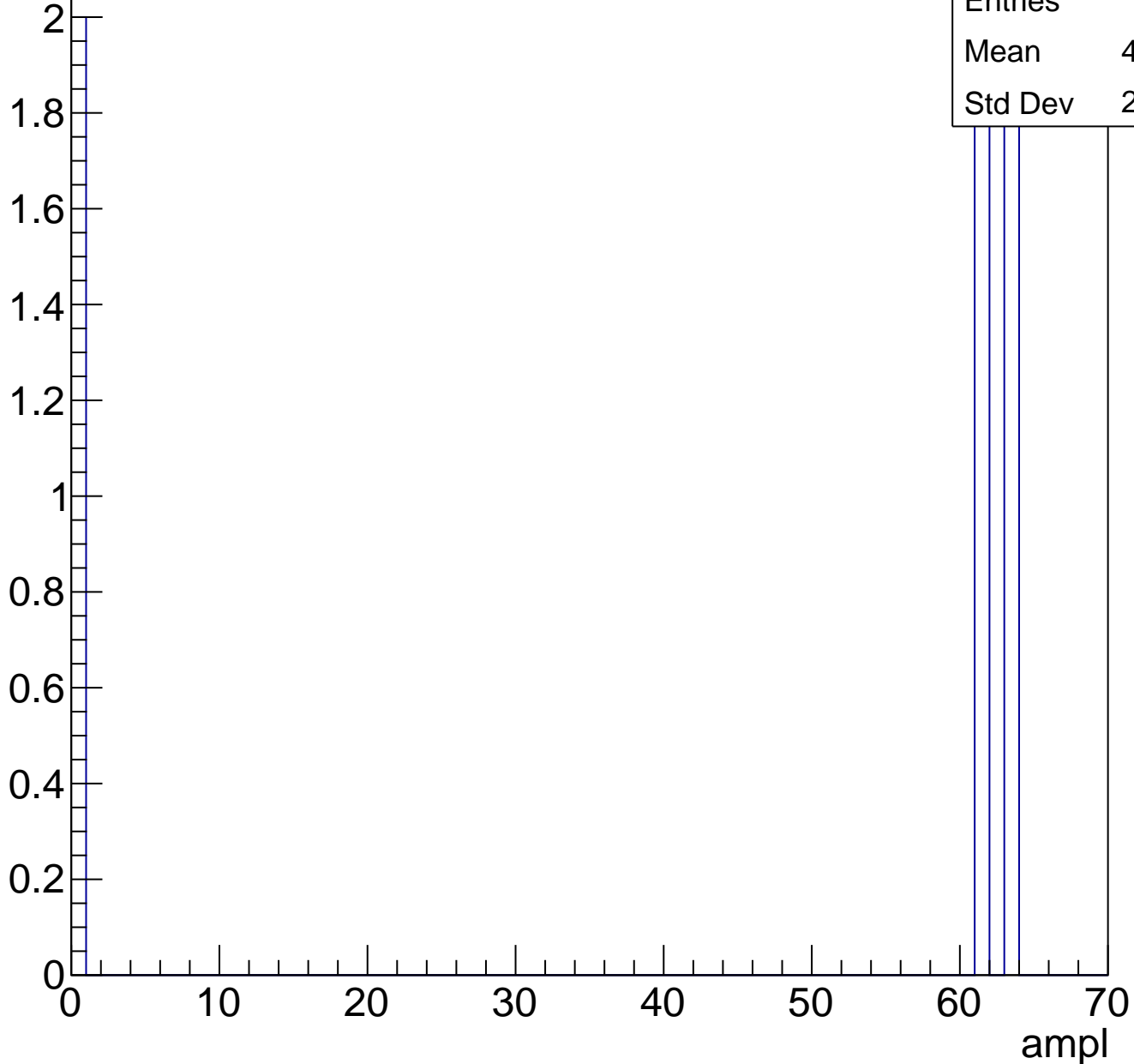




# B1L103S, U1-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch95, adc0

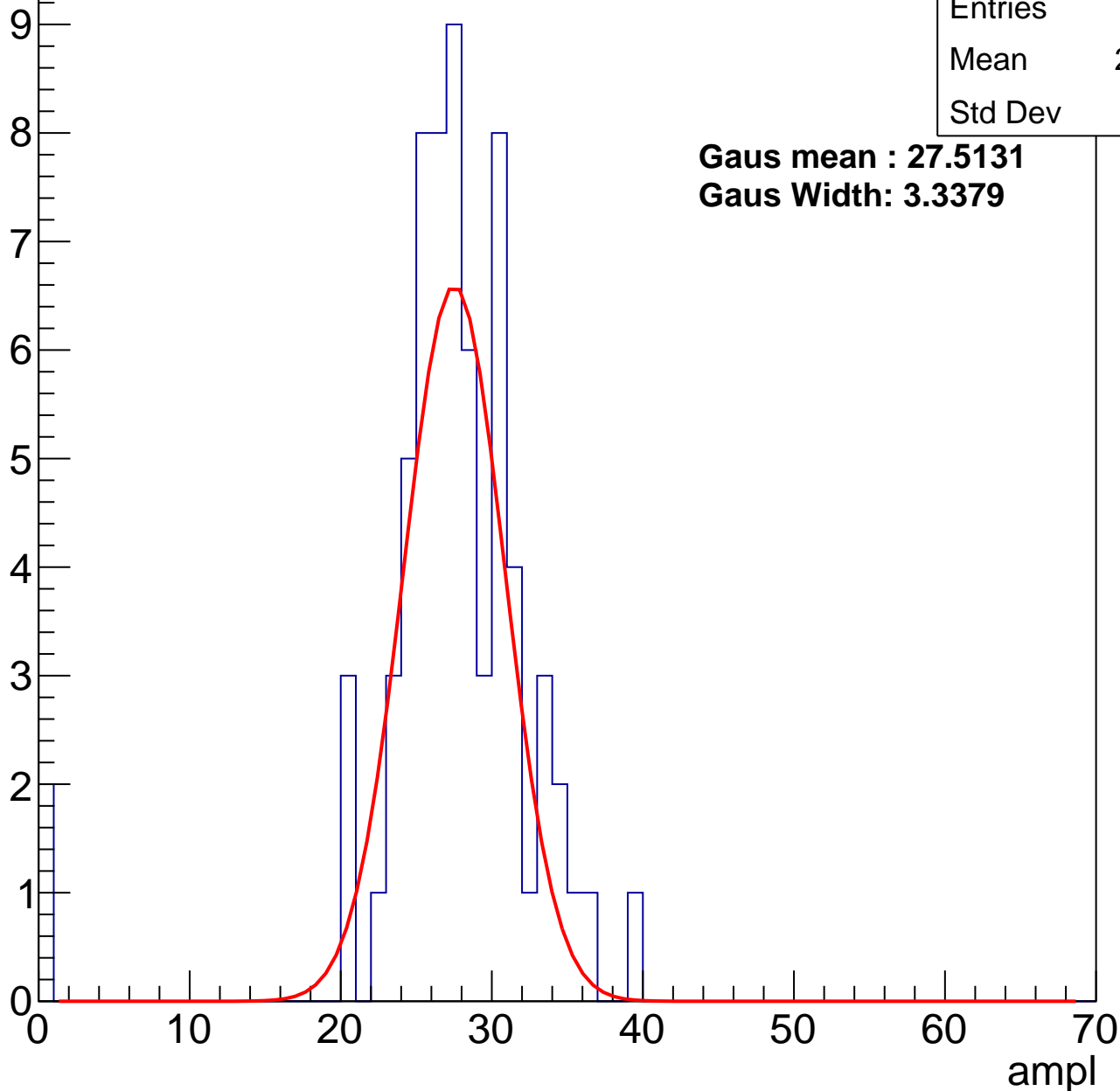
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	26.81
Std Dev	5.94

**Gaus mean : 27.5131**

**Gaus Width: 3.3379**



# B1L103S, U1-ch95, adc1

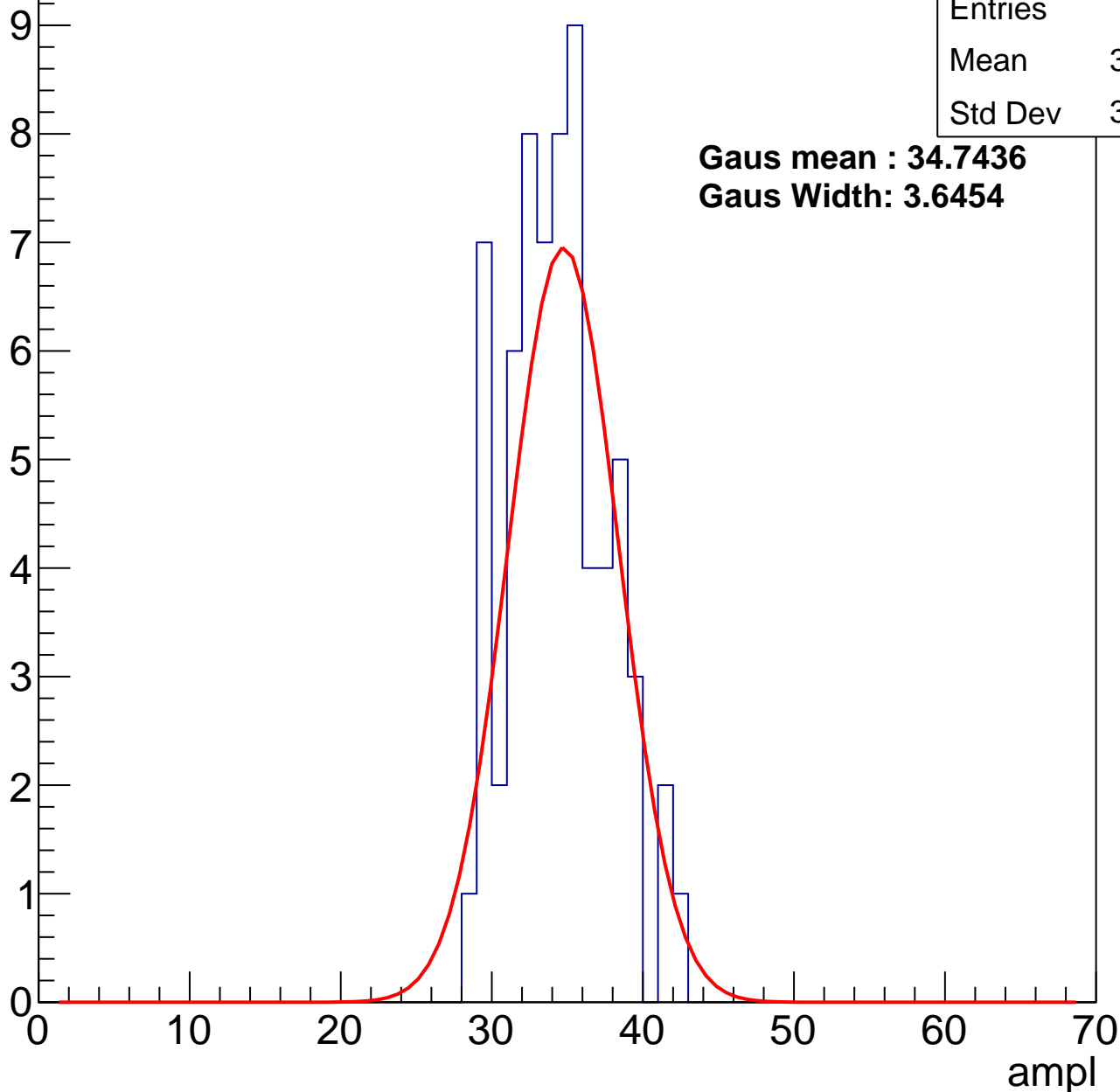
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	33.94
Std Dev	3.264

**Gaus mean : 34.7436**

**Gaus Width: 3.6454**



# B1L103S, U1-ch95, adc2

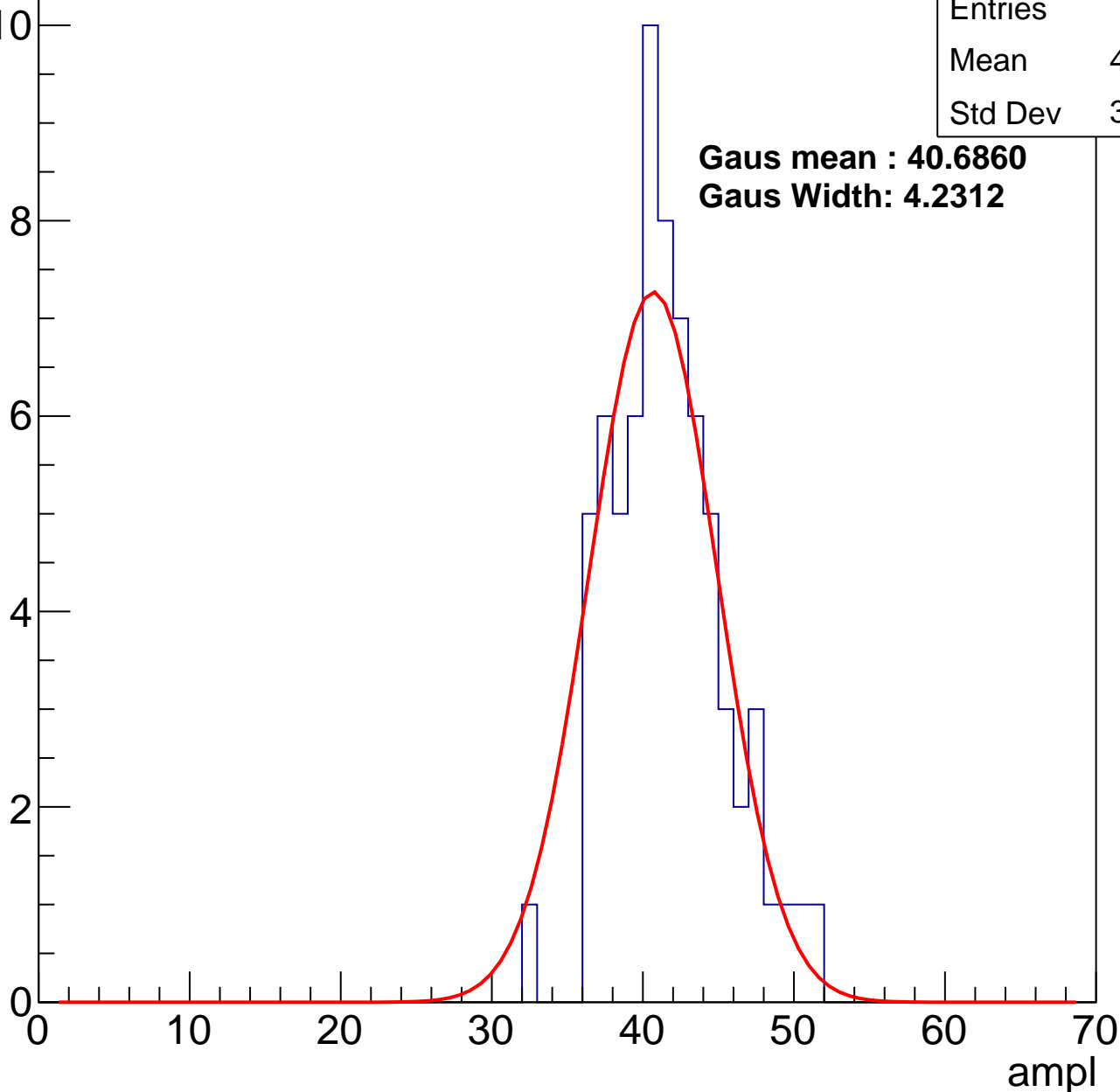
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	41.18
Std Dev	3.667

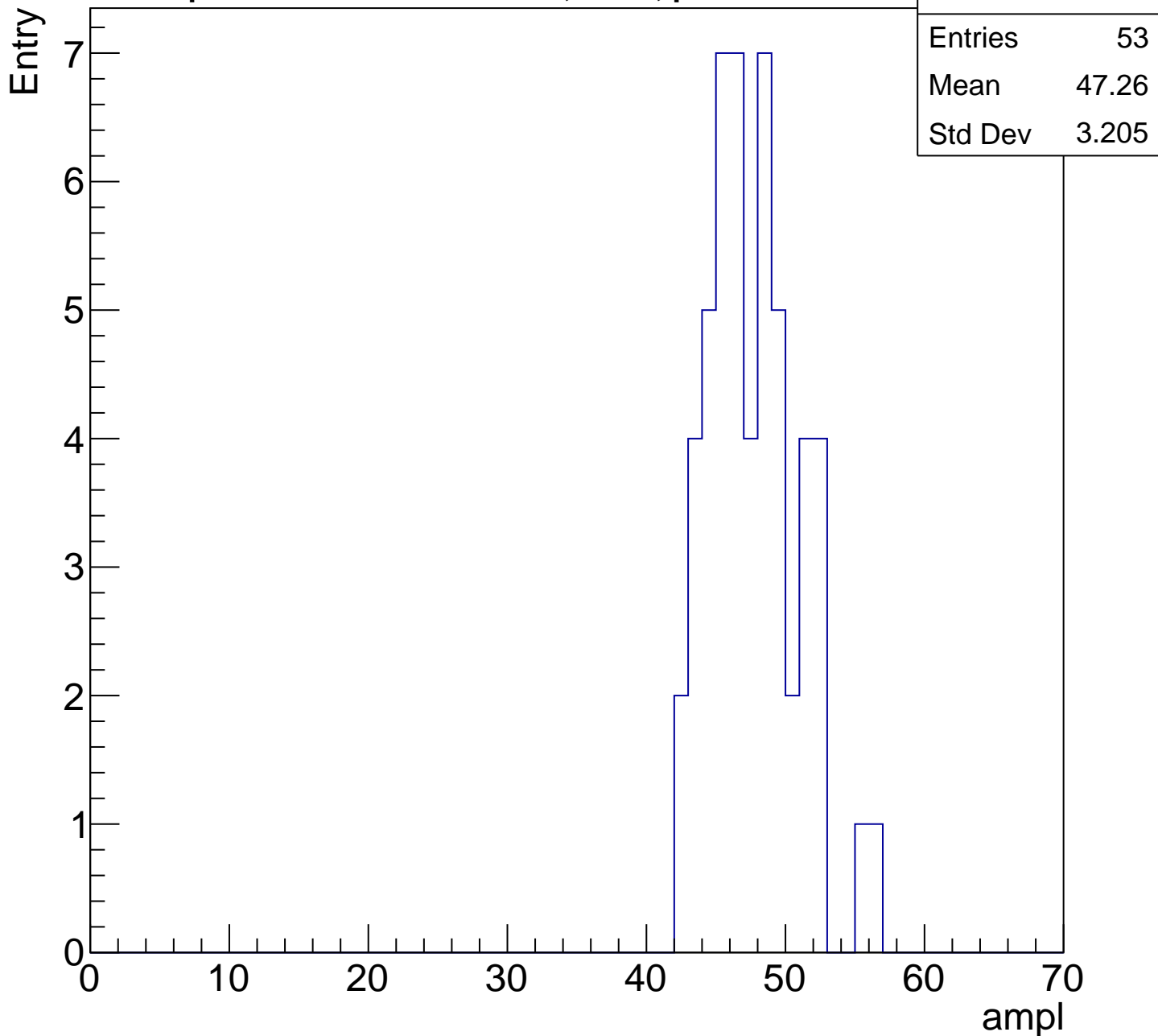
**Gaus mean : 40.6860**

**Gaus Width: 4.2312**



# B1L103S, U1-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

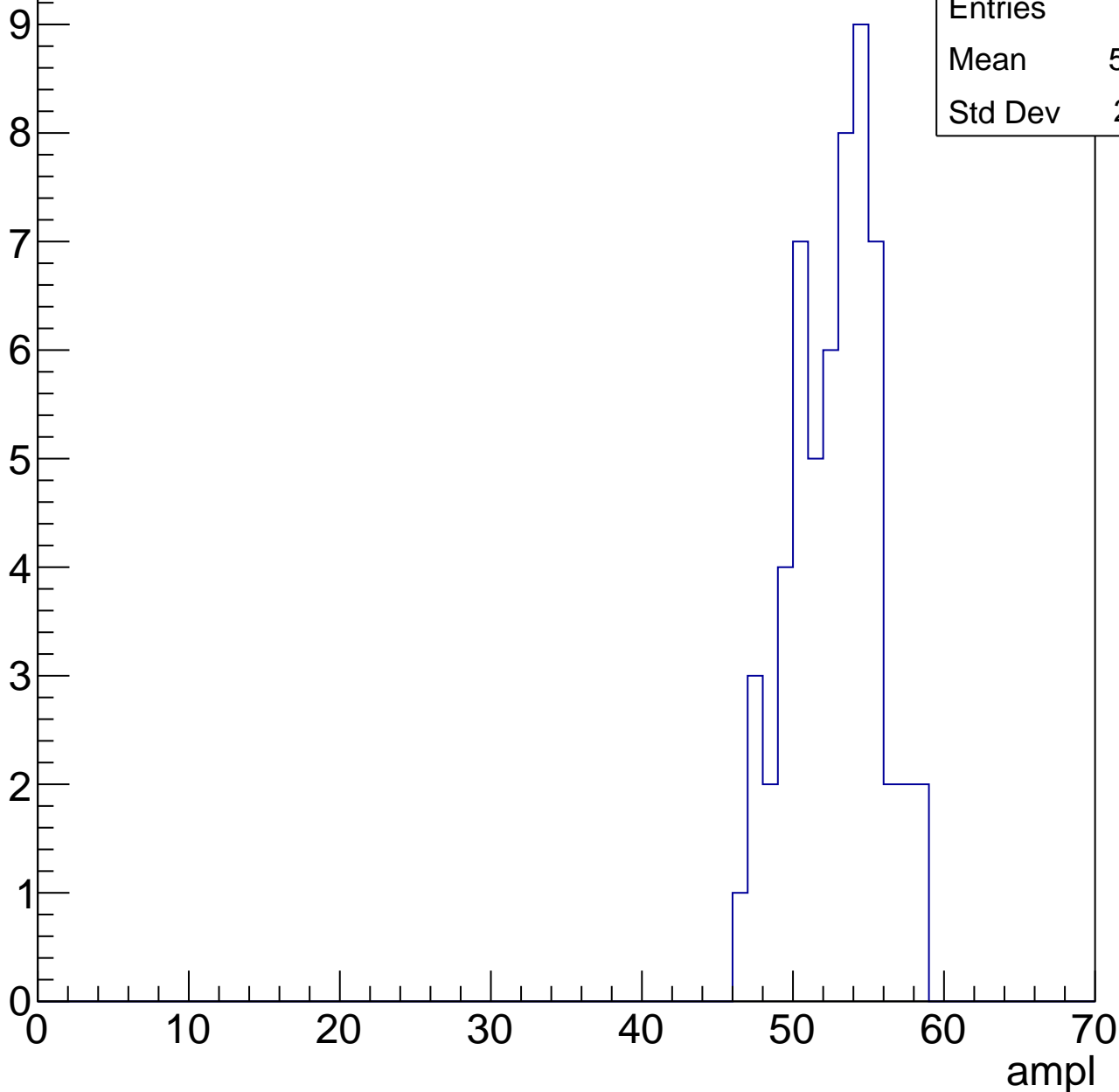


# B1L103S, U1-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	52.29
Std Dev	2.841

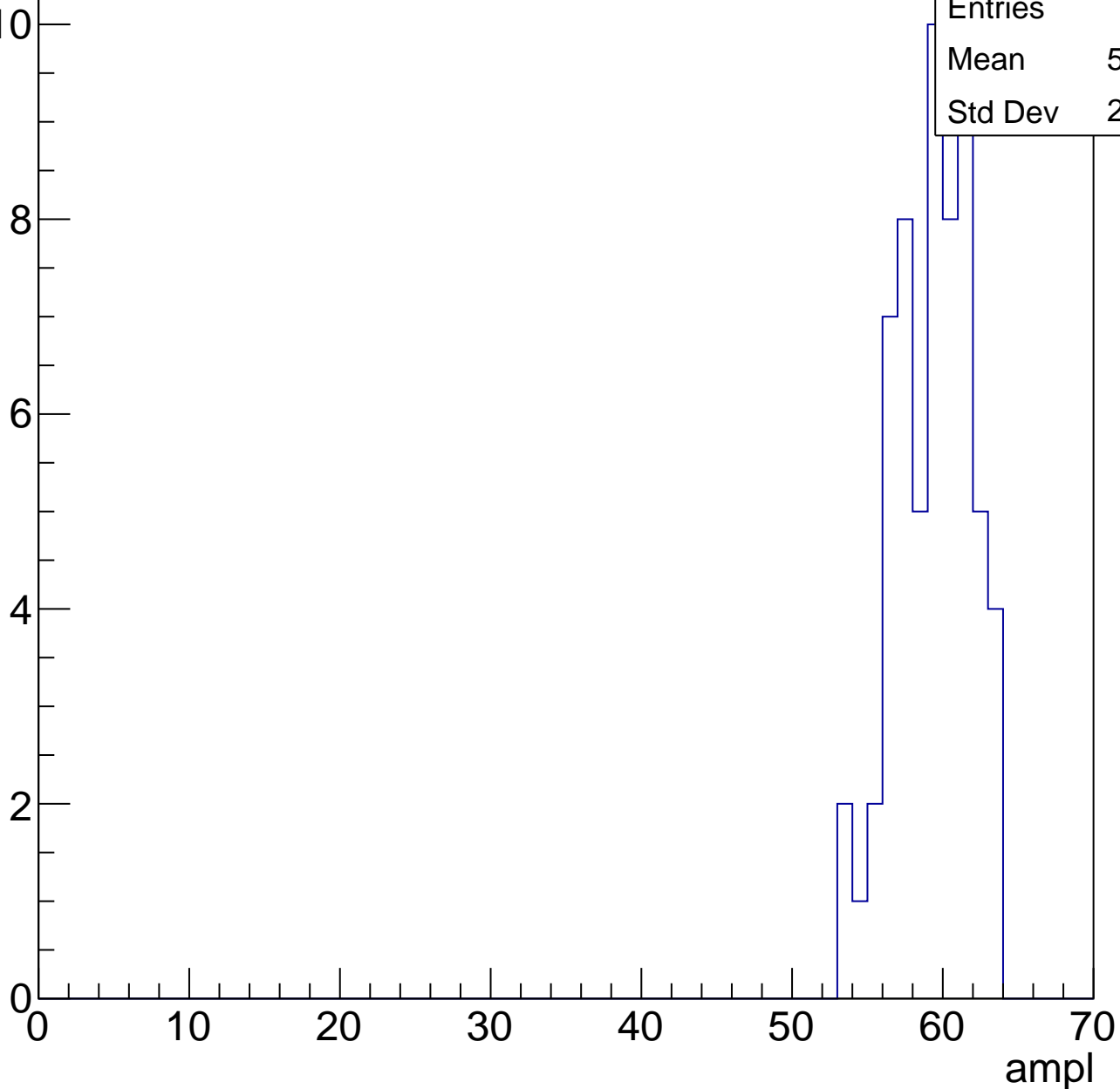


# B1L103S, U1-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	58.84
Std Dev	2.497

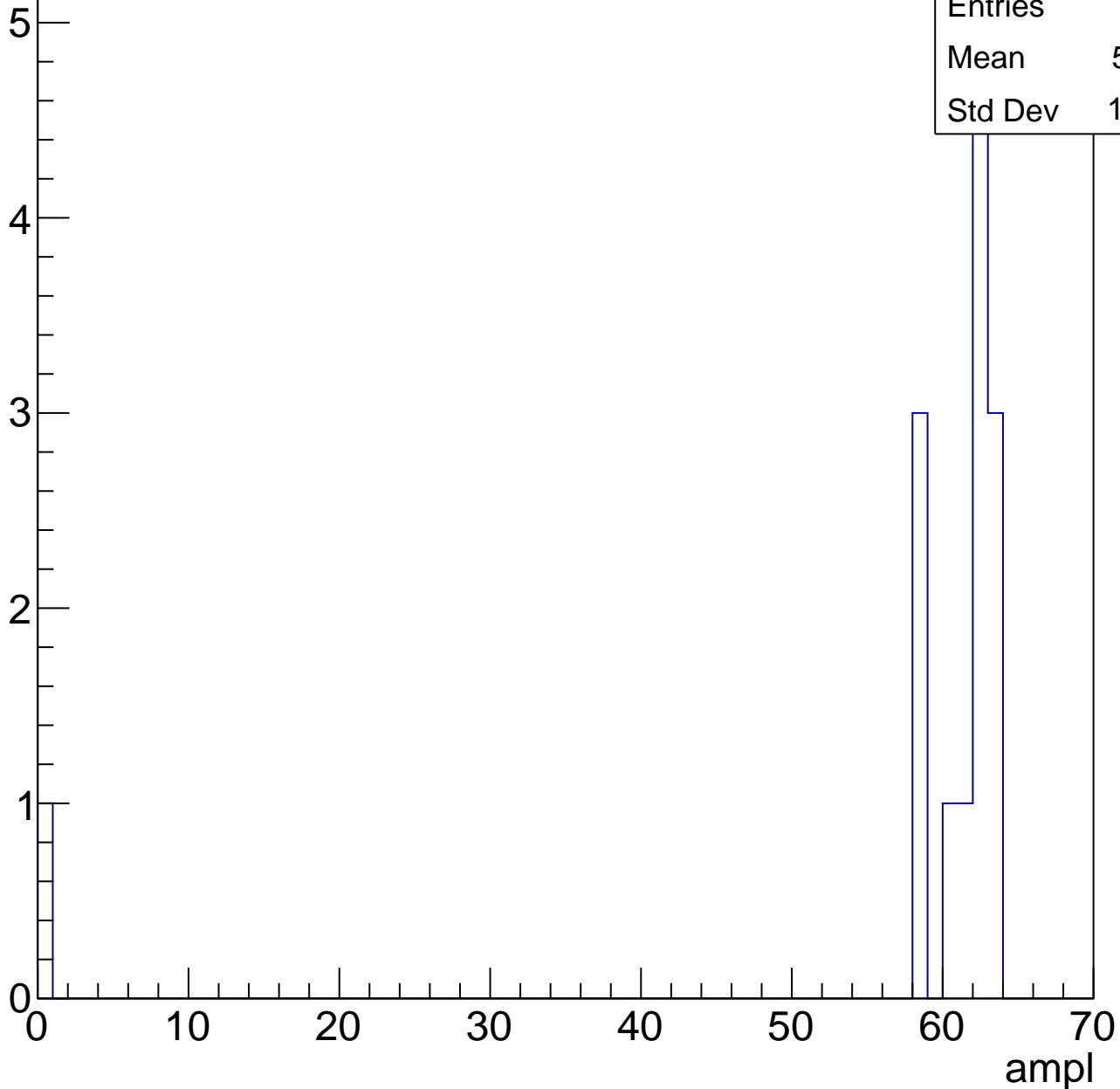


# B1L103S, U1-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	14
Mean	56.71
Std Dev	15.83

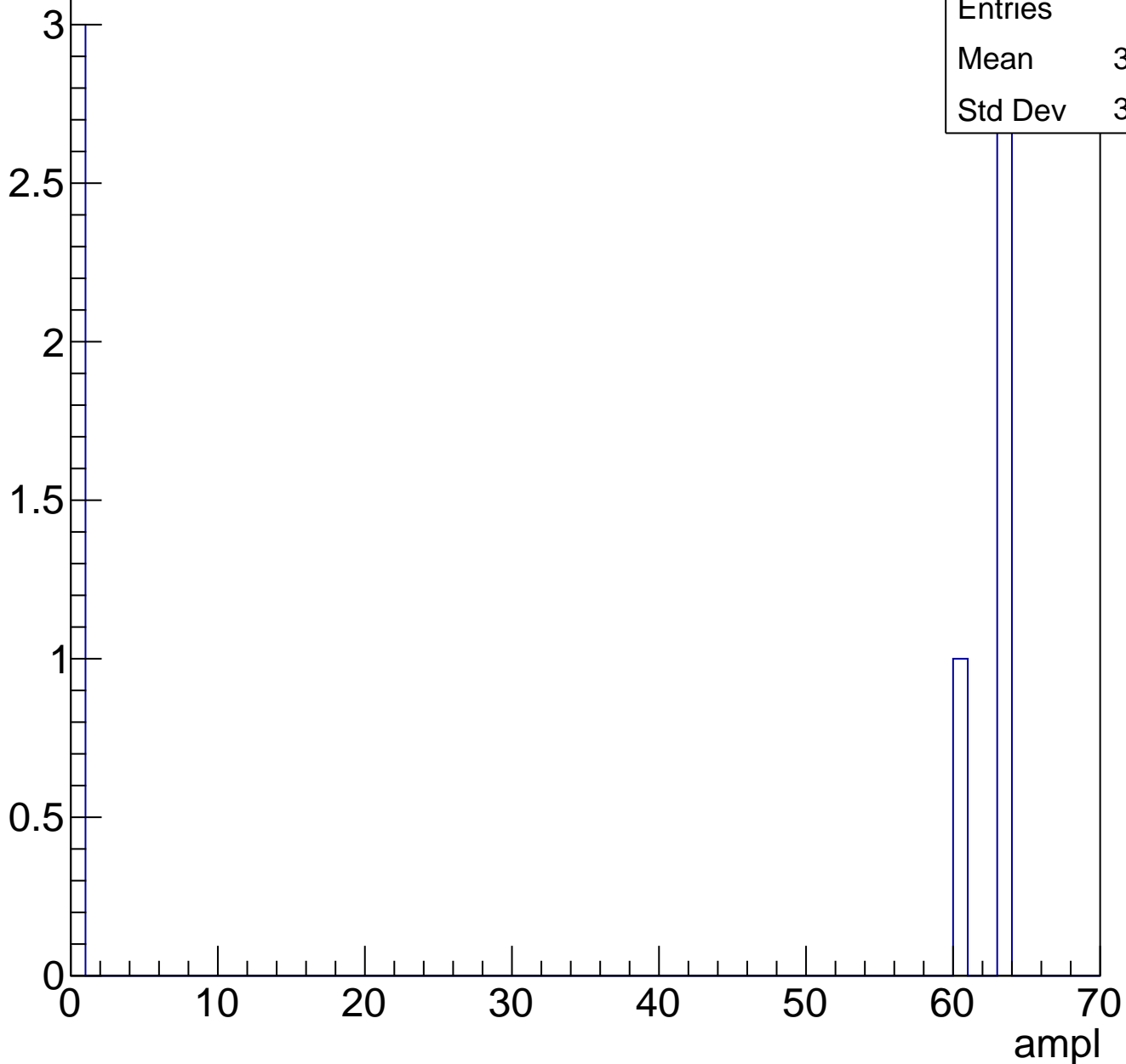




# B1L103S, U1-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch96, adc0

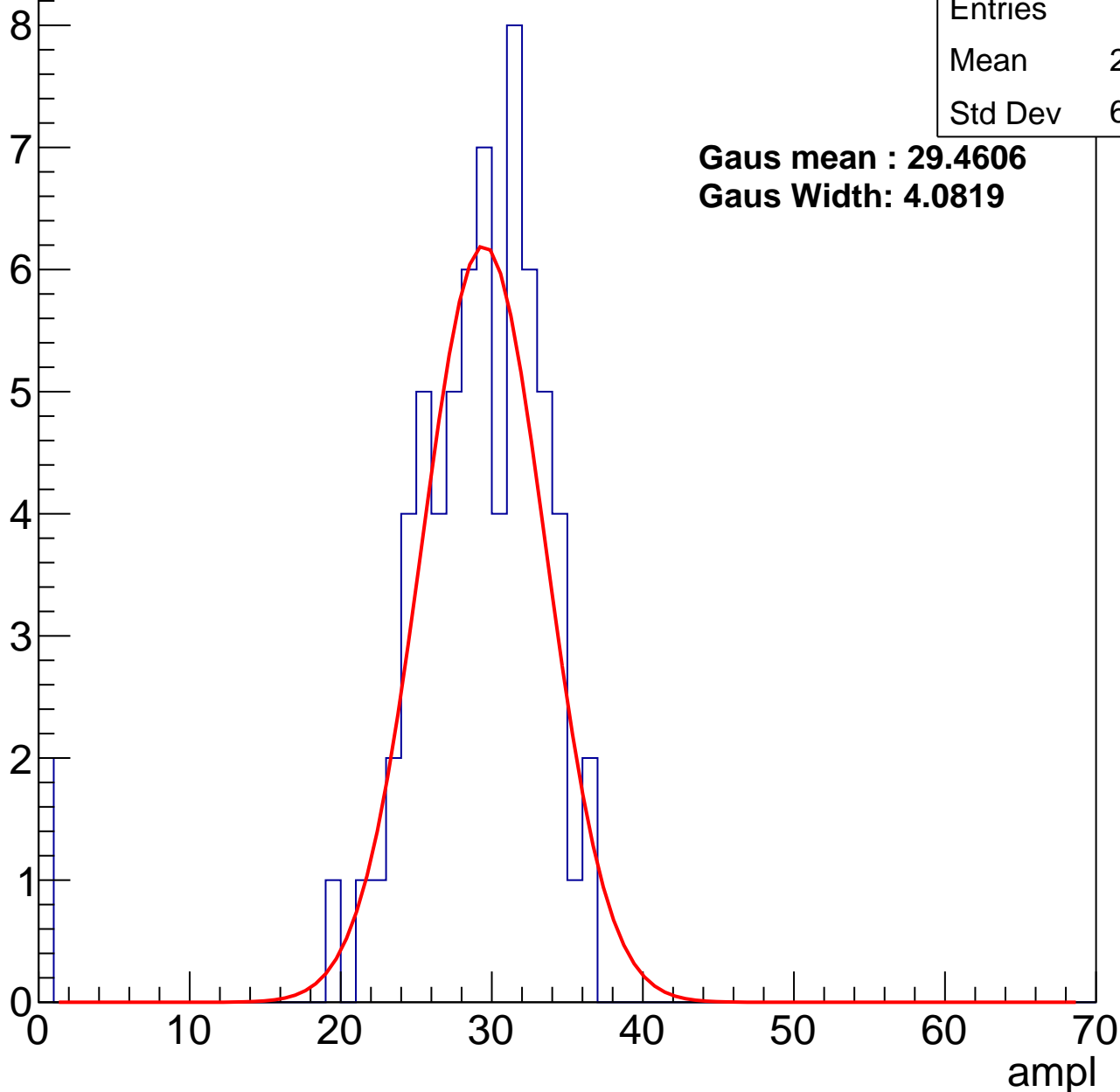
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	28.04
Std Dev	6.125

**Gaus mean : 29.4606**

**Gaus Width: 4.0819**



# B1L103S, U1-ch96, adc1

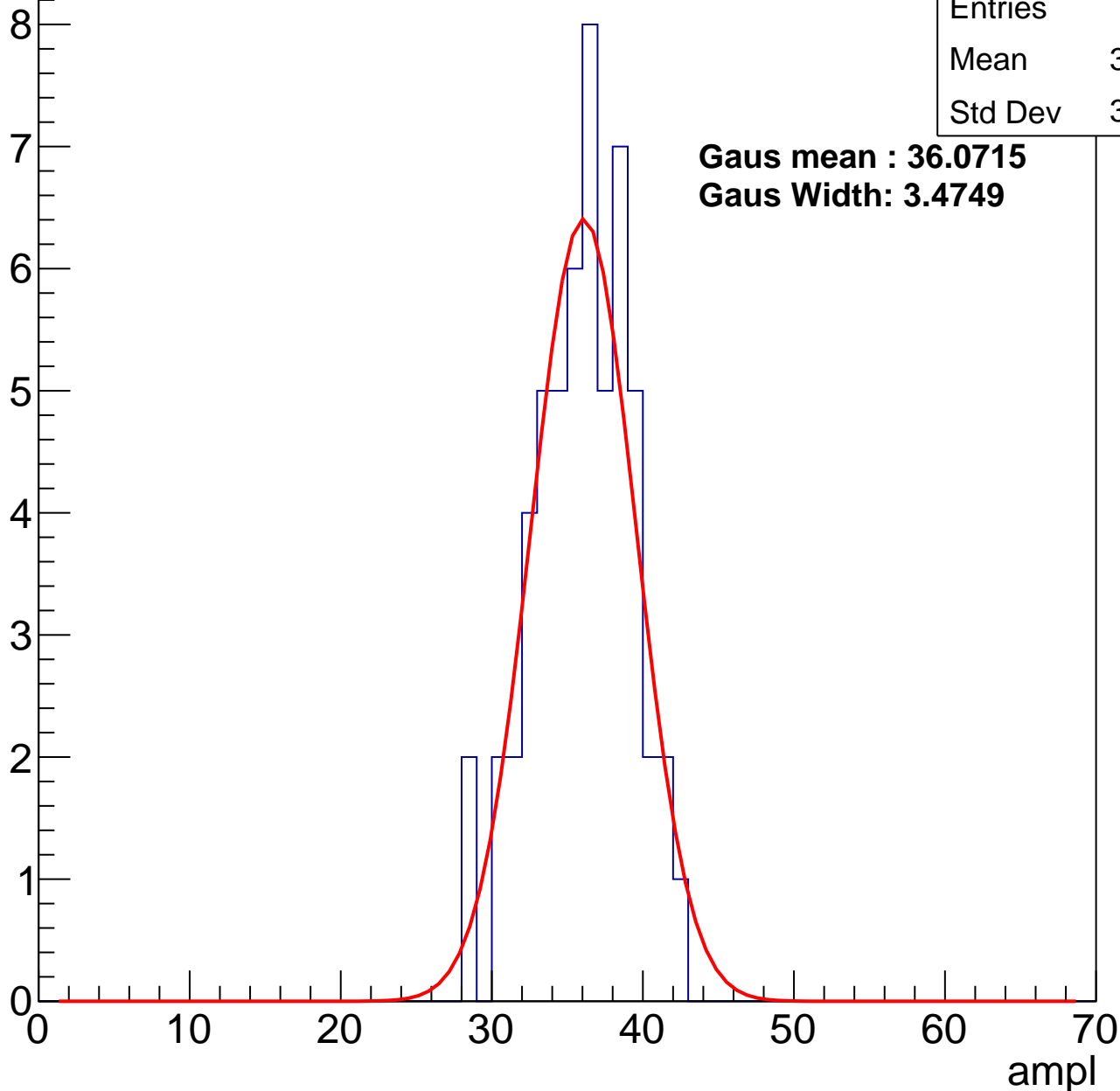
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	35.52
Std Dev	3.185

**Gaus mean : 36.0715**

**Gaus Width: 3.4749**

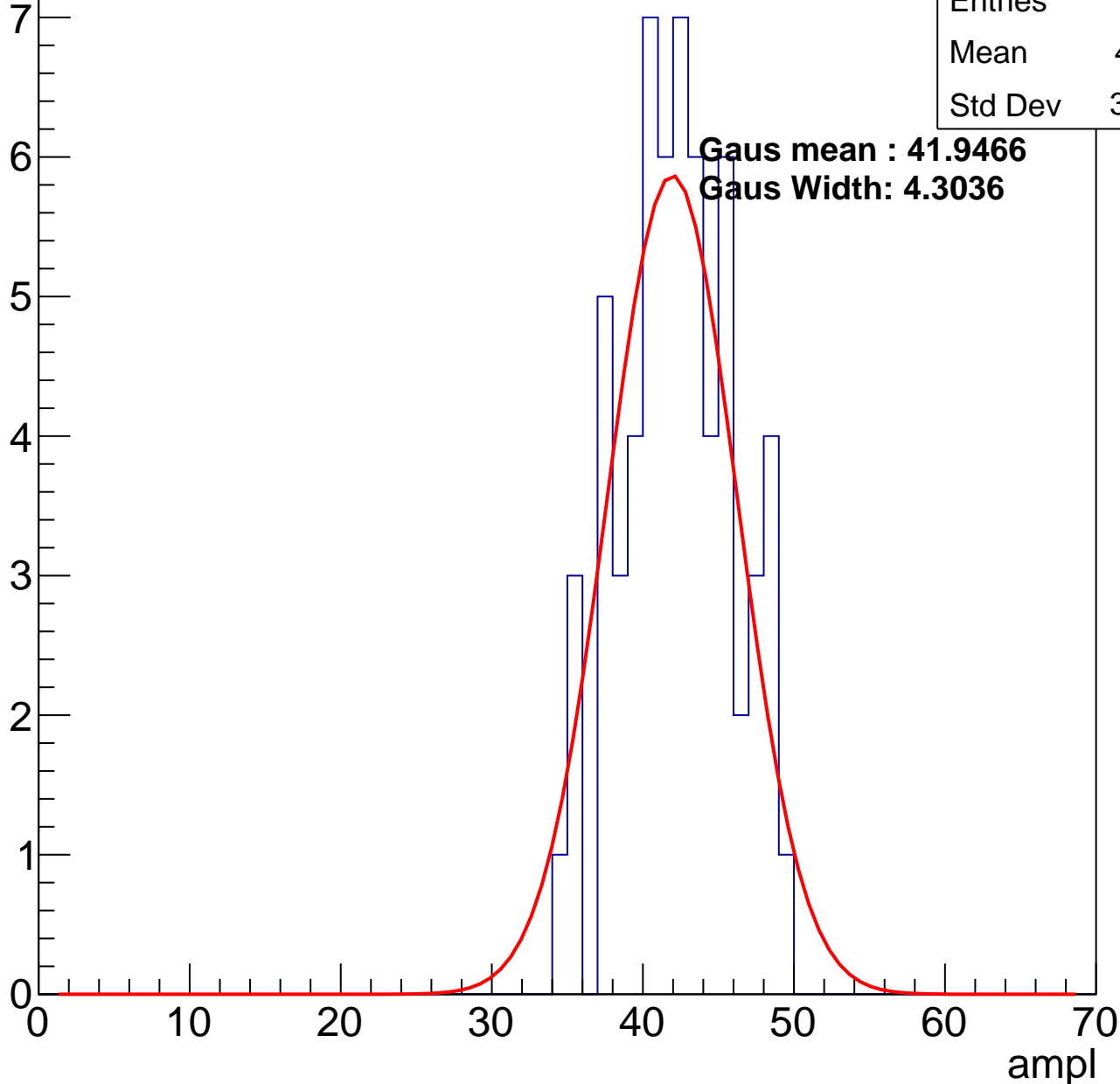


# B1L103S, U1-ch96, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	41.81
Std Dev	3.654

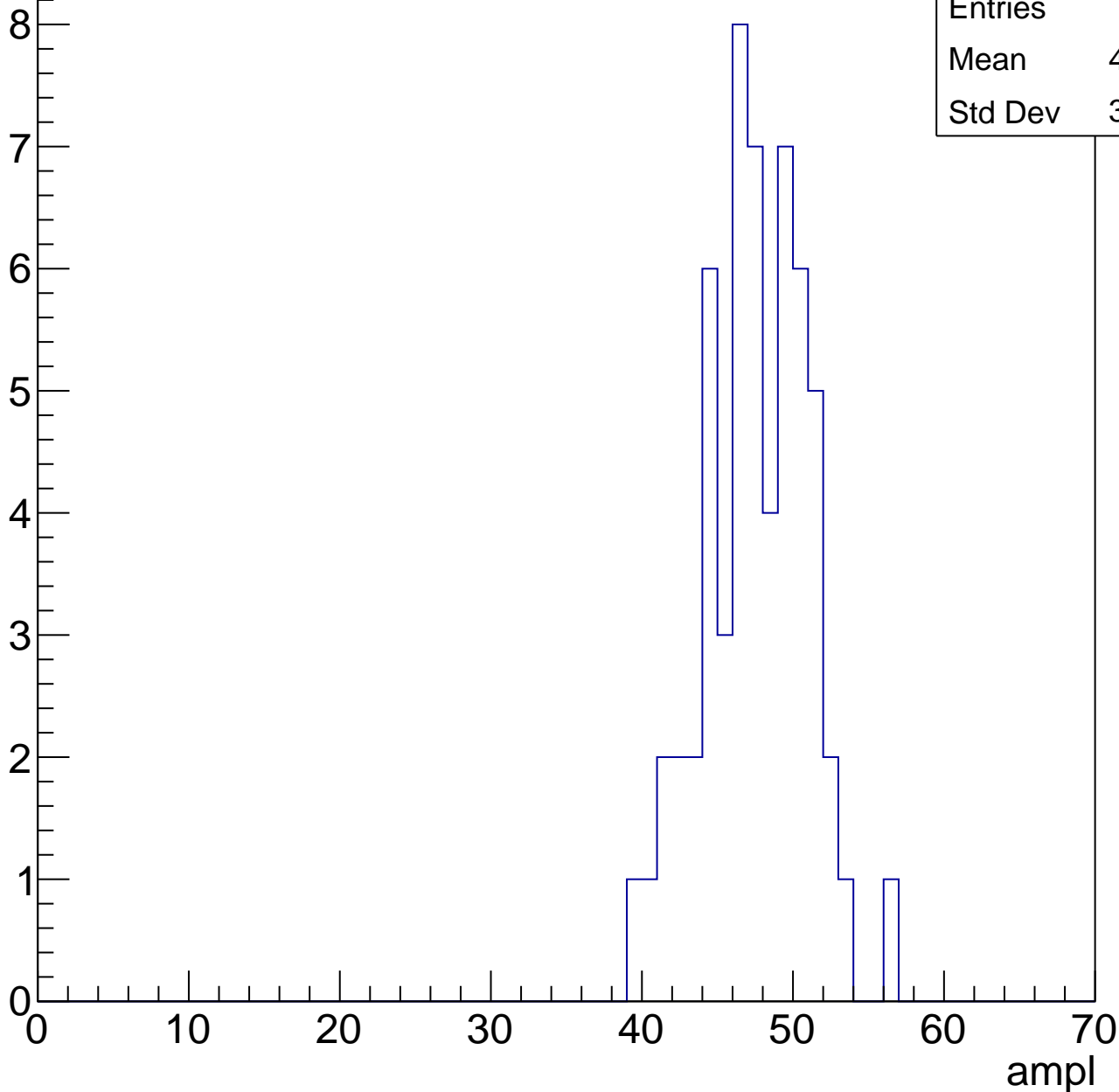


# B1L103S, U1-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	47.07
Std Dev	3.408

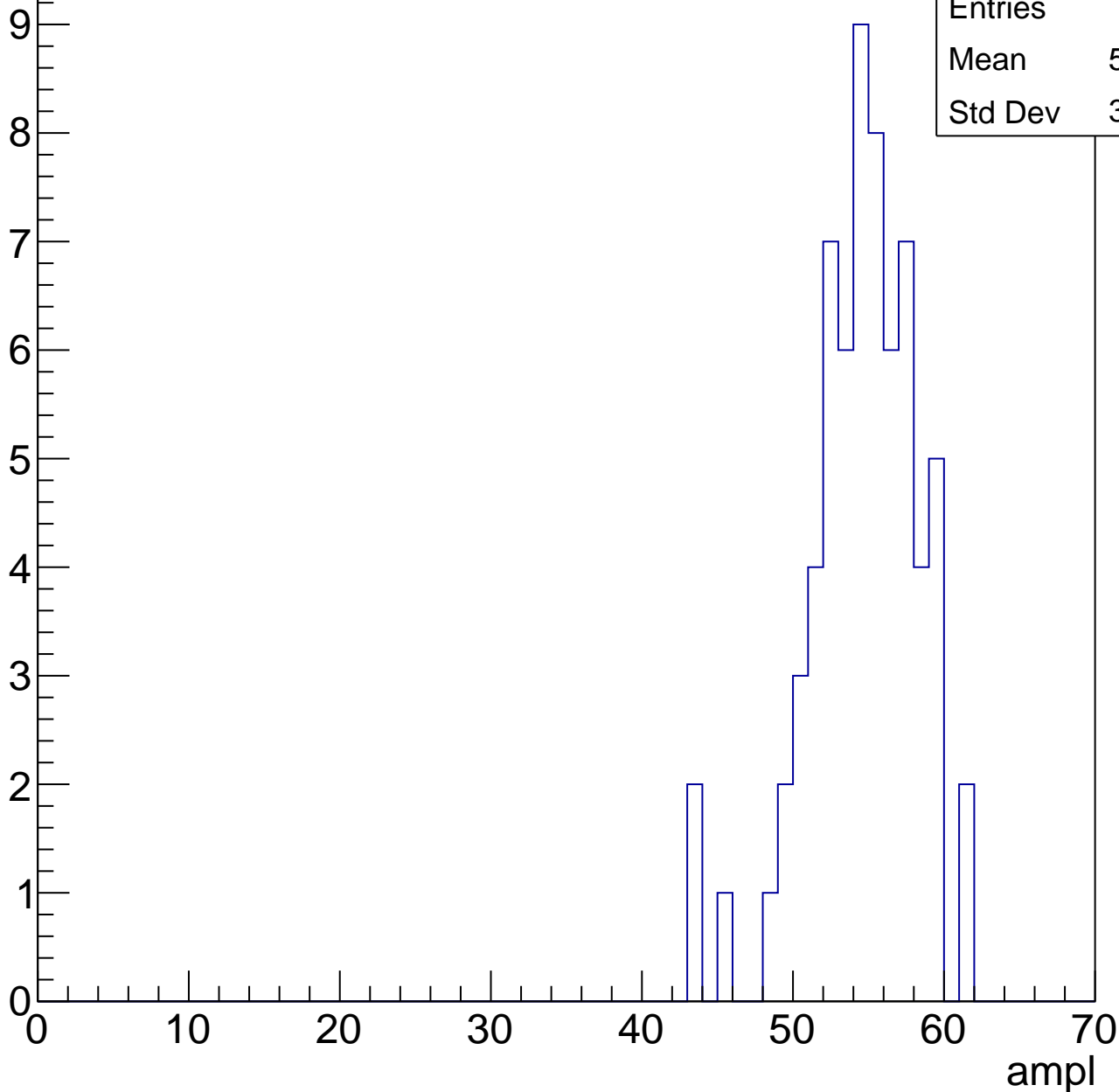


# B1L103S, U1-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	54.07
Std Dev	3.683

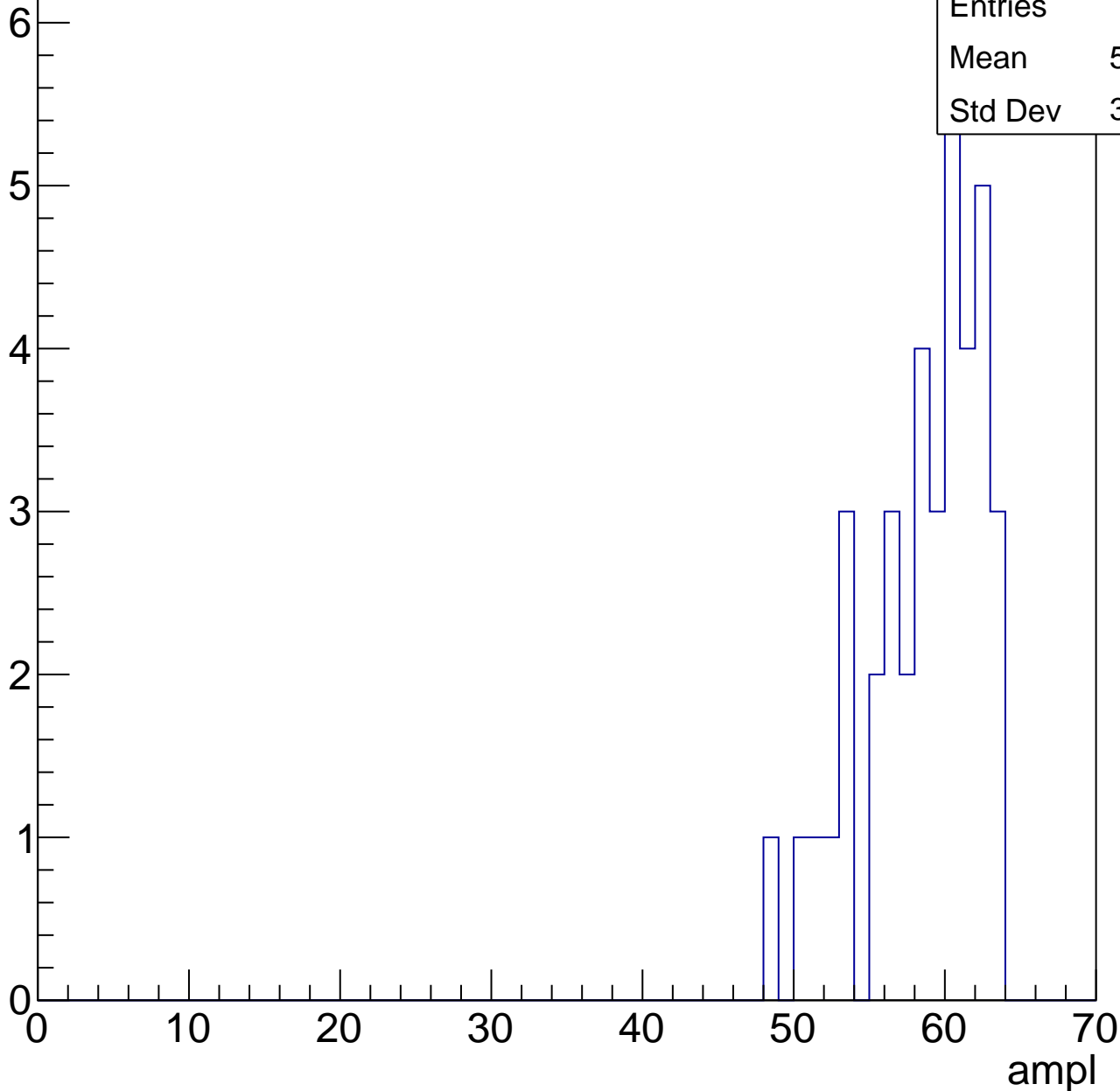


# B1L103S, U1-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

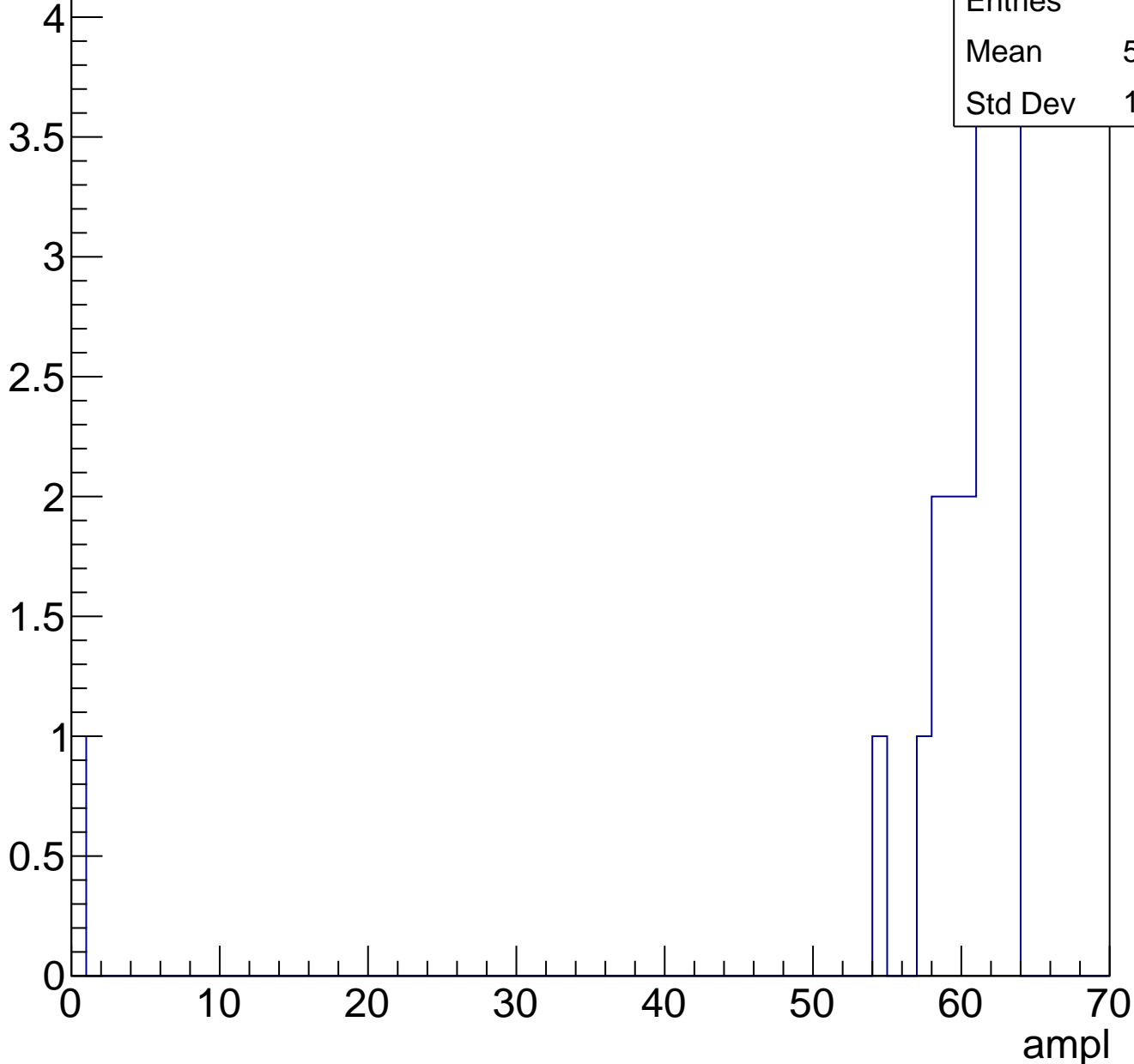
Entries	39
Mean	58.05
Std Dev	3.836



# B1L103S, U1-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

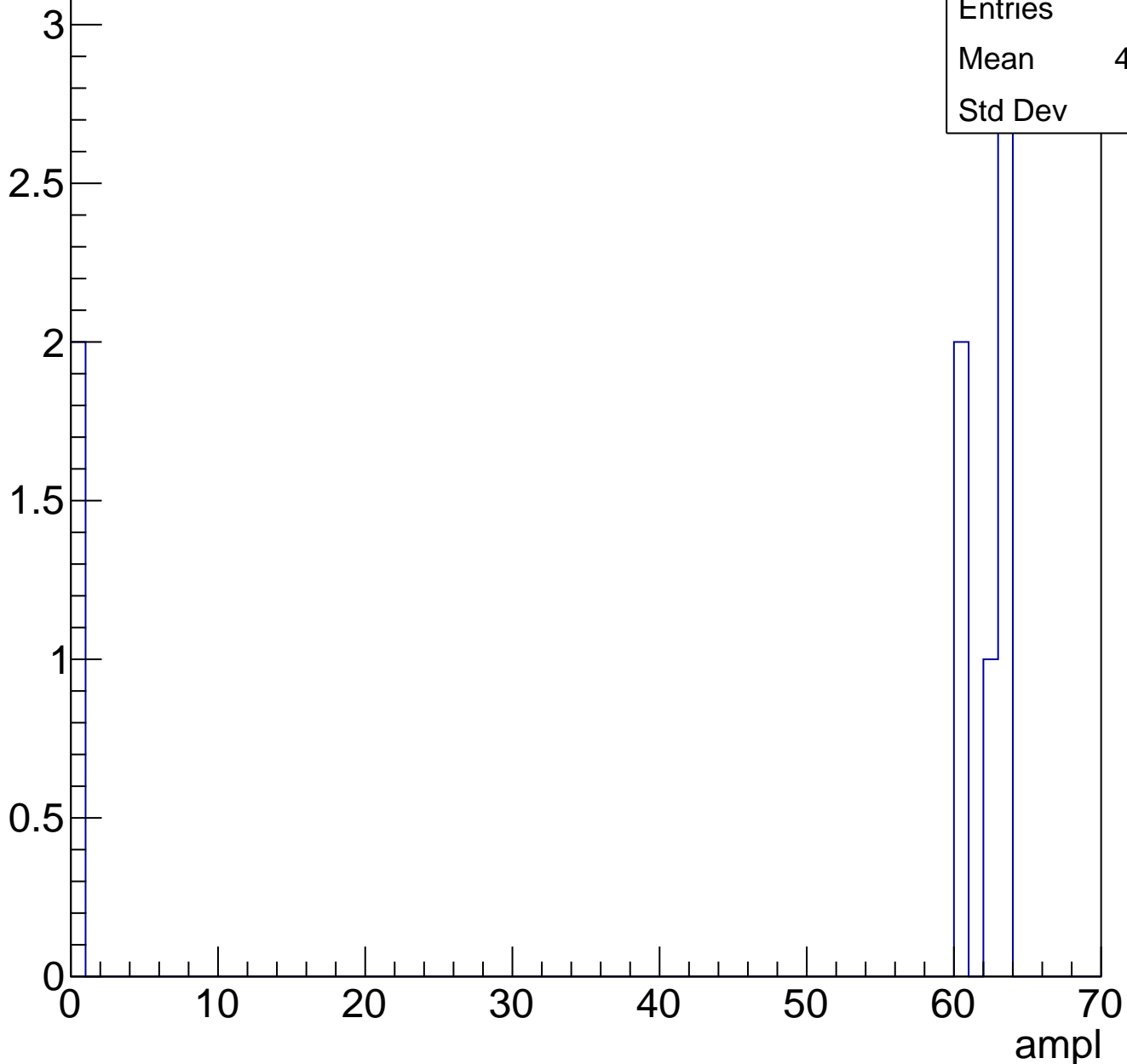




# B1L103S, U1-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch97, adc0

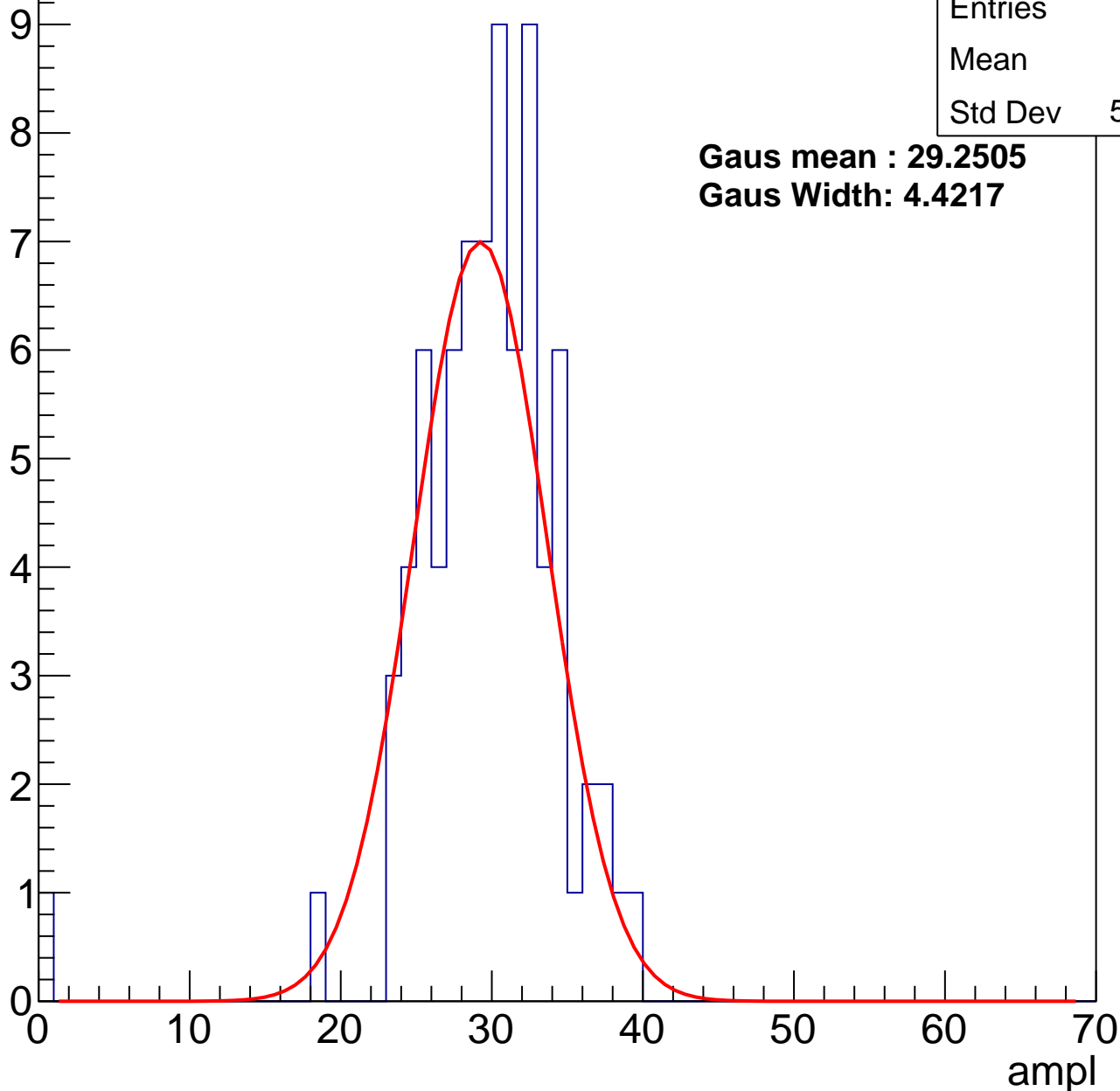
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	29.2
Std Dev	5.124

**Gaus mean : 29.2505**

**Gaus Width: 4.4217**



# B1L103S, U1-ch97, adc1

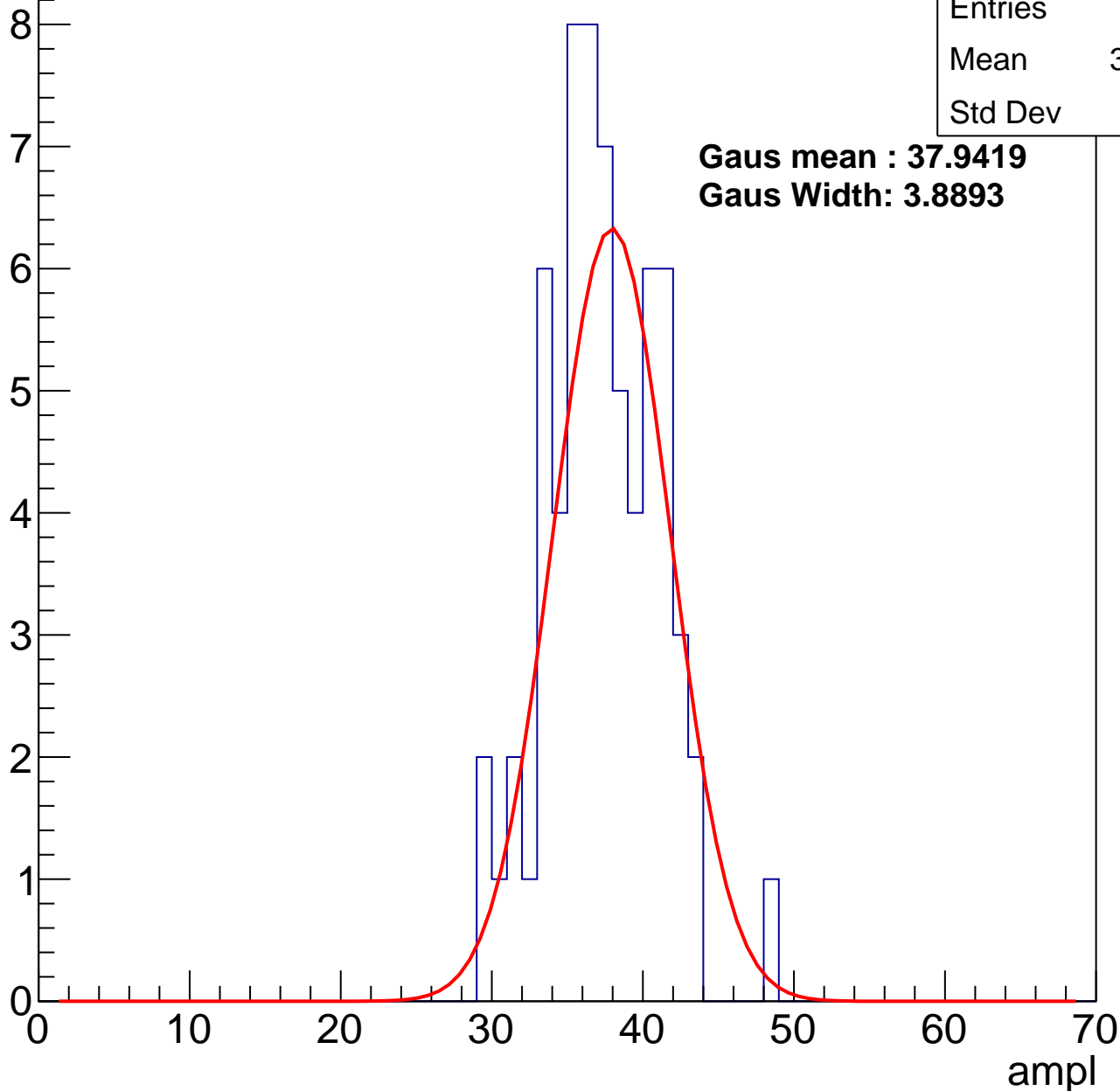
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	36.89
Std Dev	3.66

**Gaus mean : 37.9419**

**Gaus Width: 3.8893**



# B1L103S, U1-ch97, adc2

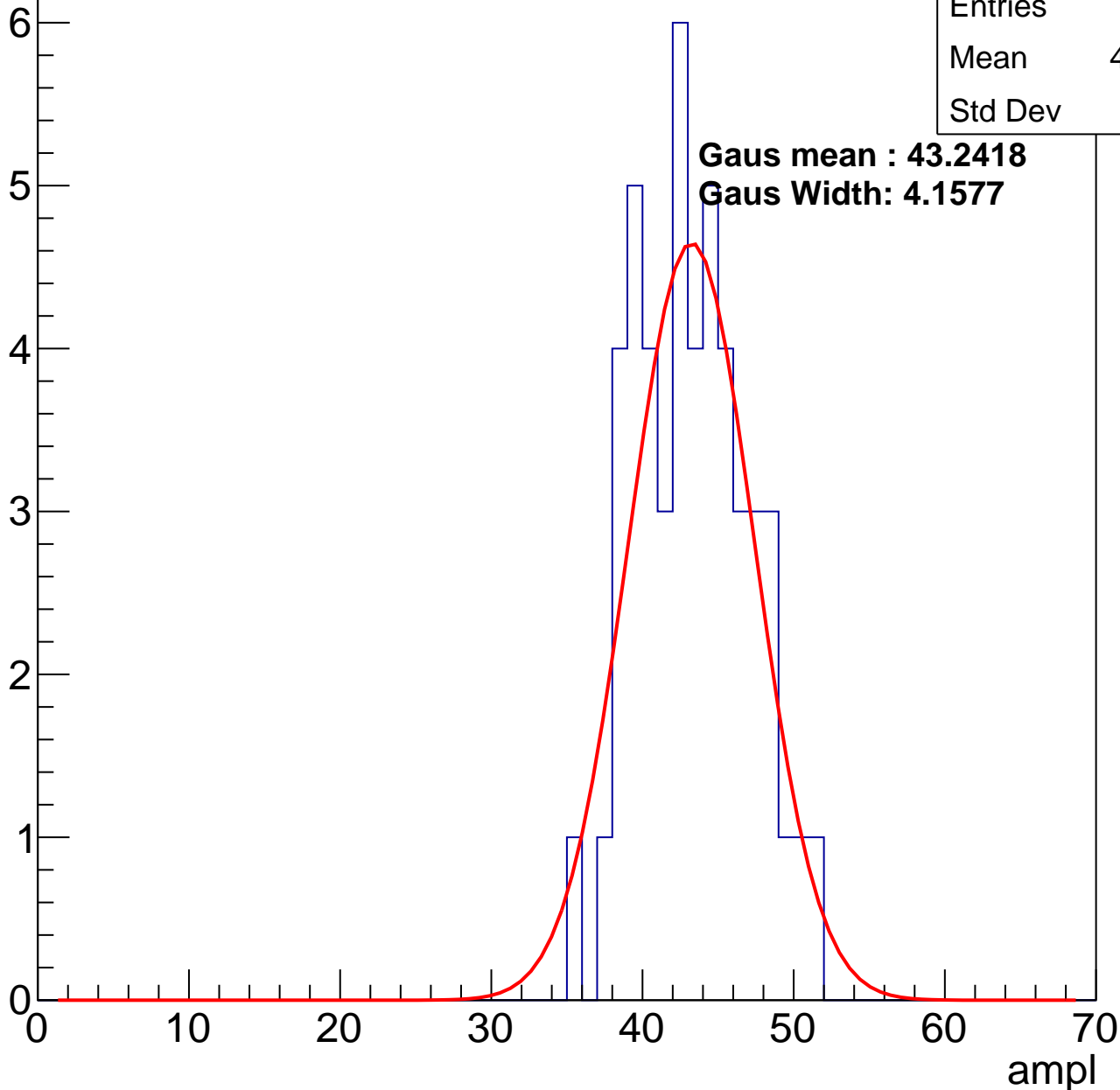
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	42.84
Std Dev	3.65

**Gaus mean : 43.2418**

**Gaus Width: 4.1577**

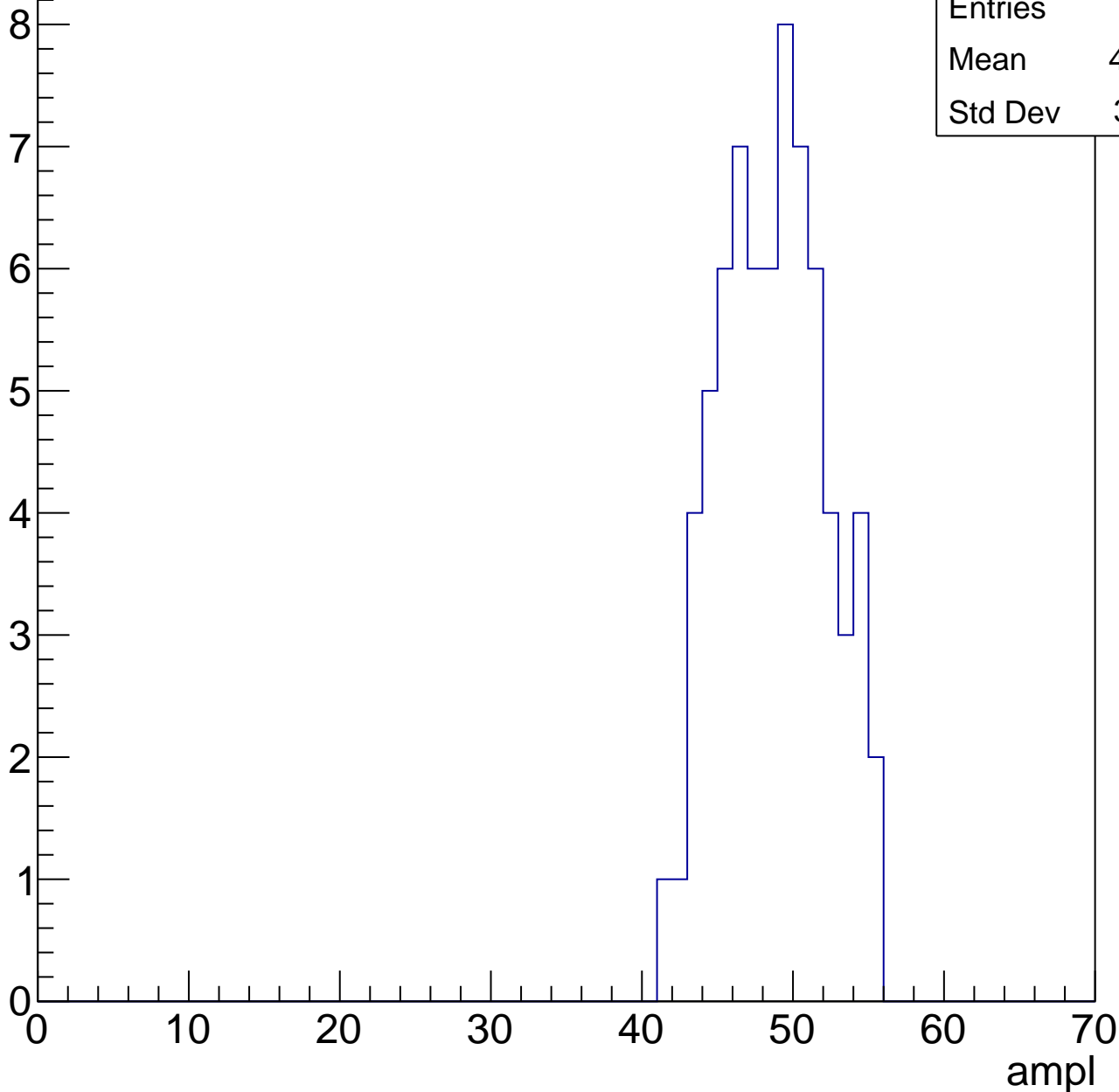


# B1L103S, U1-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	48.26
Std Dev	3.421

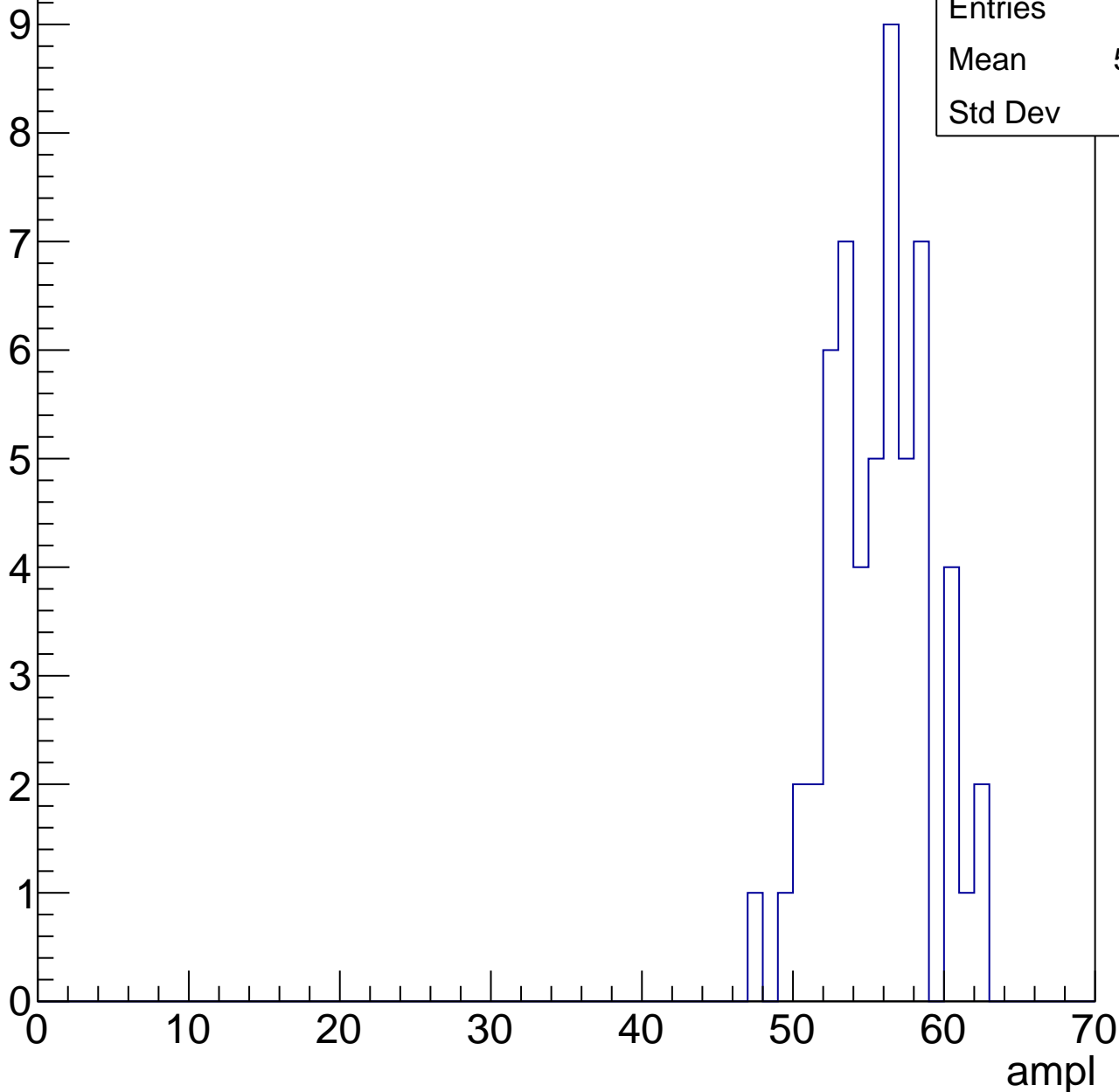


# B1L103S, U1-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	55.21
Std Dev	3.25

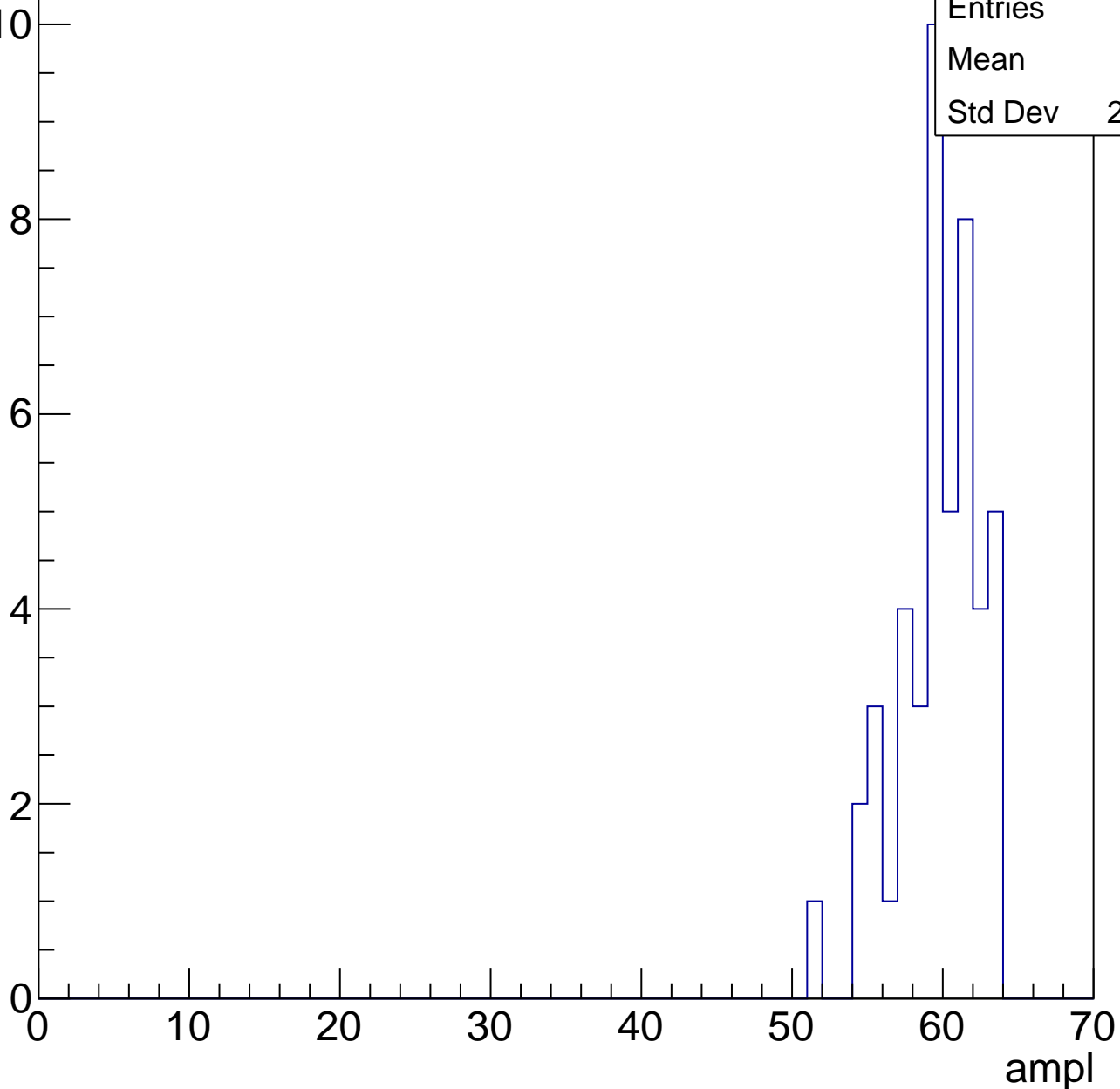


# B1L103S, U1-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	59.2
Std Dev	2.724

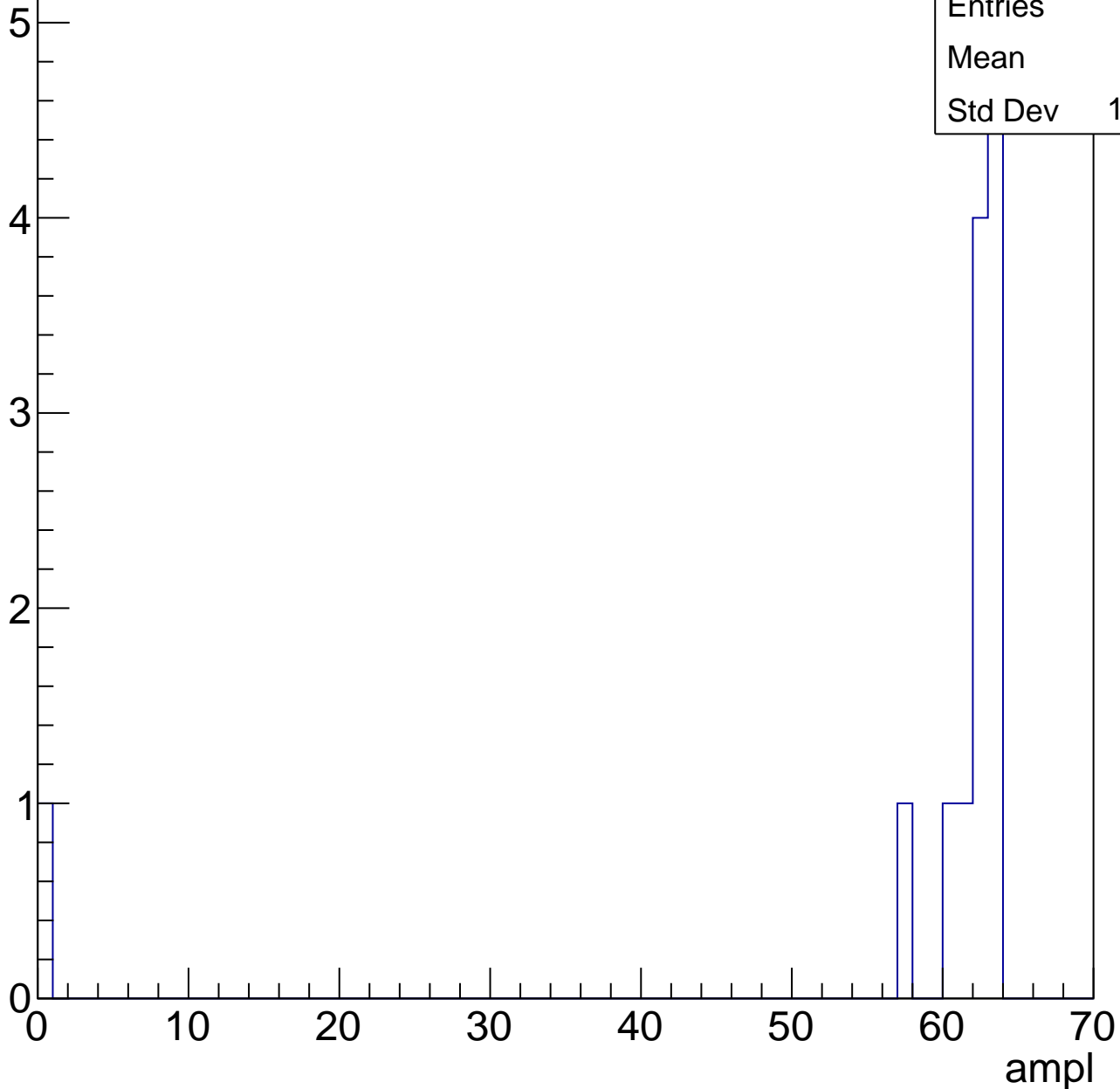


# B1L103S, U1-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	13
Mean	57
Std Dev	16.53





# B1L103S, U1-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch98, adc0

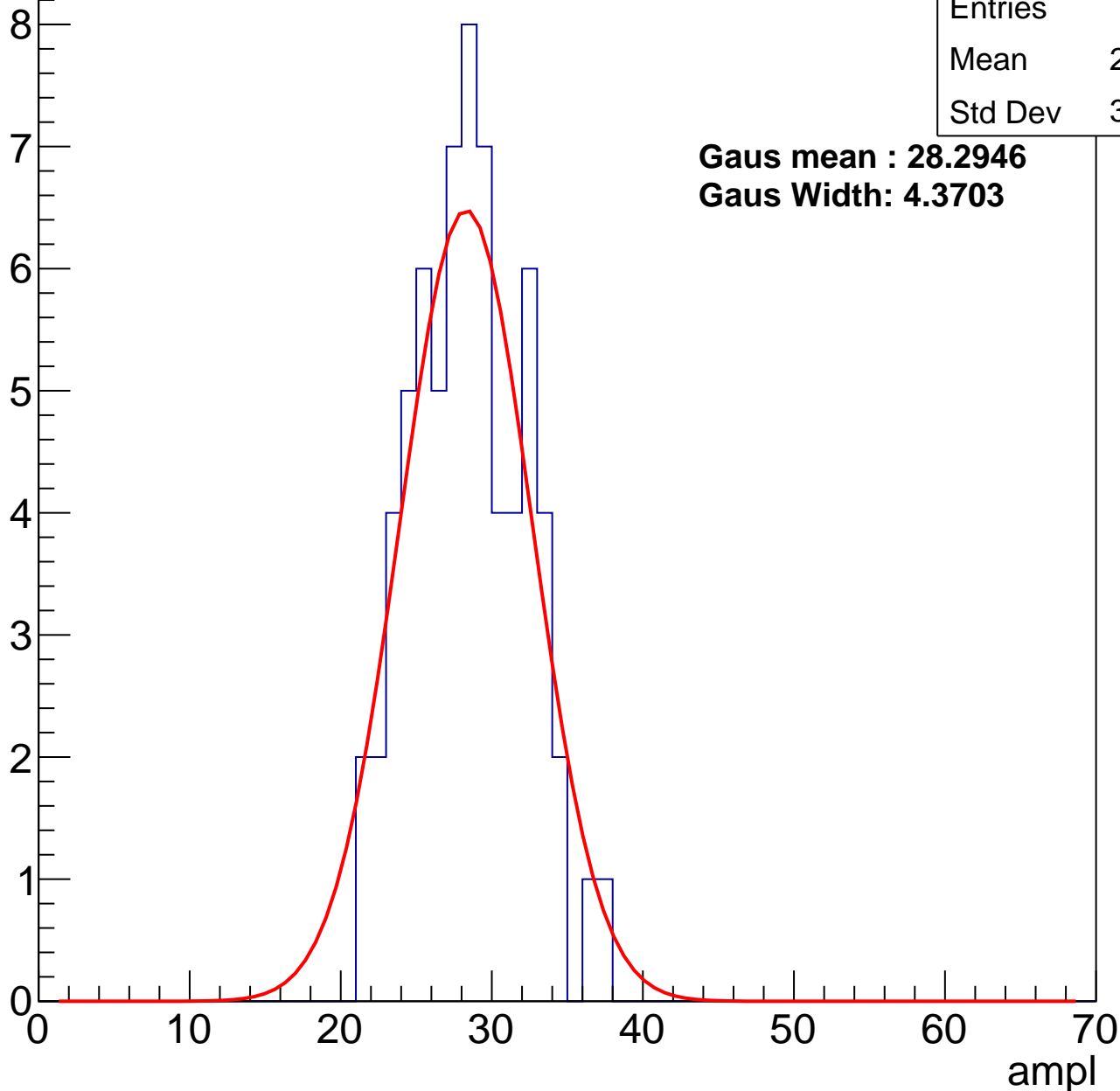
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	27.99
Std Dev	3.644

**Gaus mean : 28.2946**

**Gaus Width: 4.3703**



# B1L103S, U1-ch98, adc1

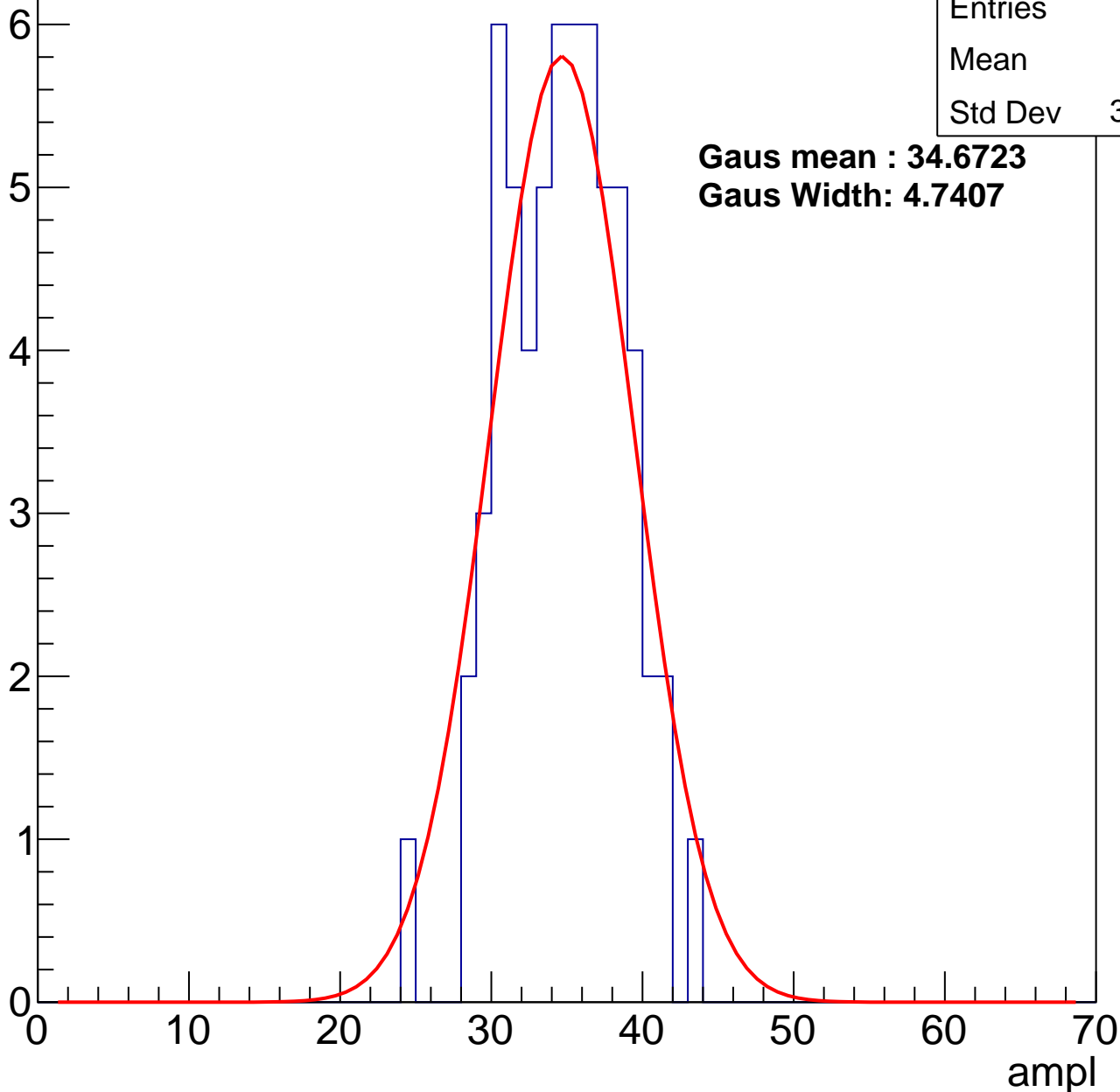
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	34.3
Std Dev	3.799

**Gaus mean : 34.6723**

**Gaus Width: 4.7407**



# B1L103S, U1-ch98, adc2

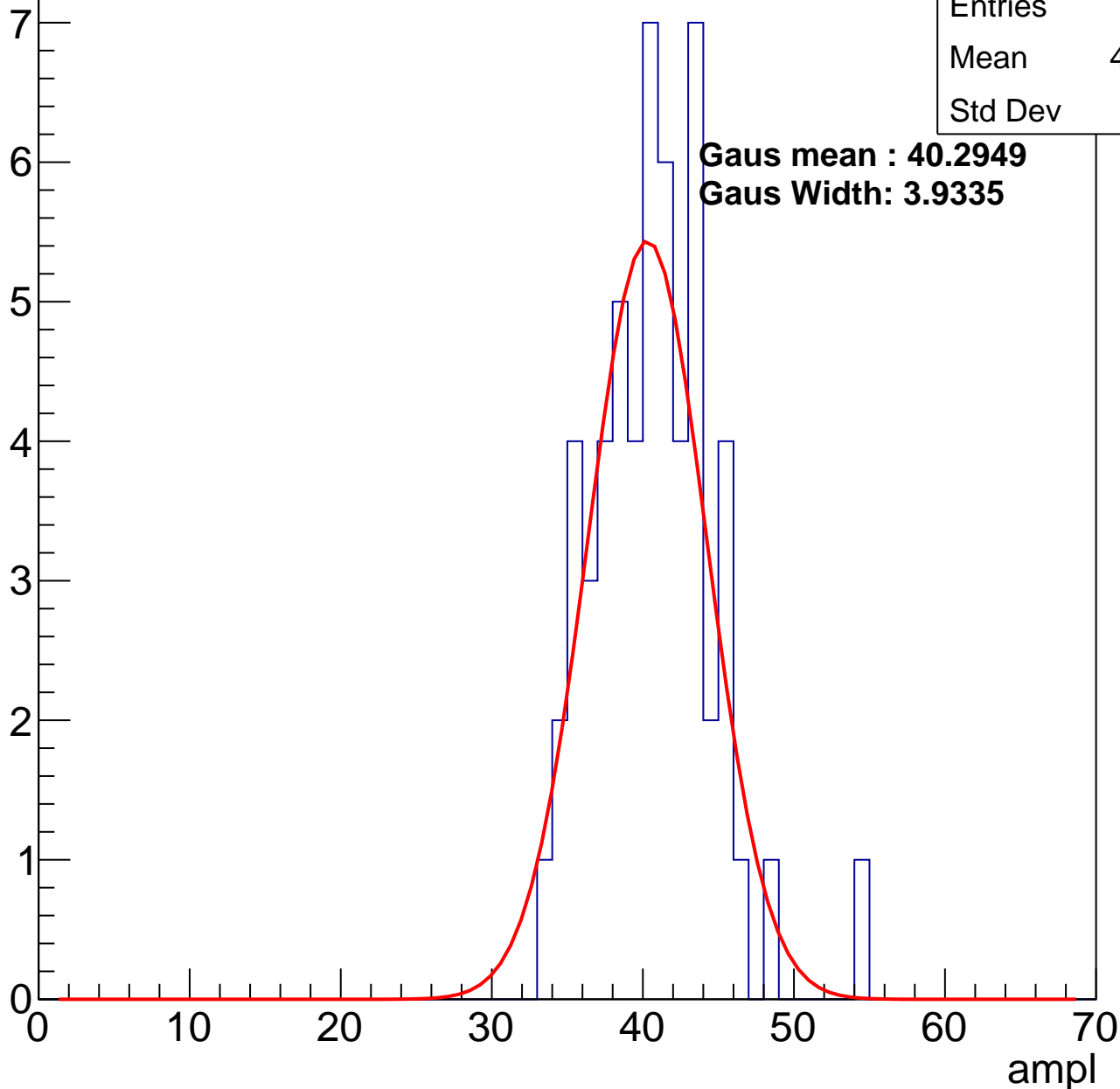
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	40.25
Std Dev	3.87

**Gaus mean : 40.2949**

**Gaus Width: 3.9335**

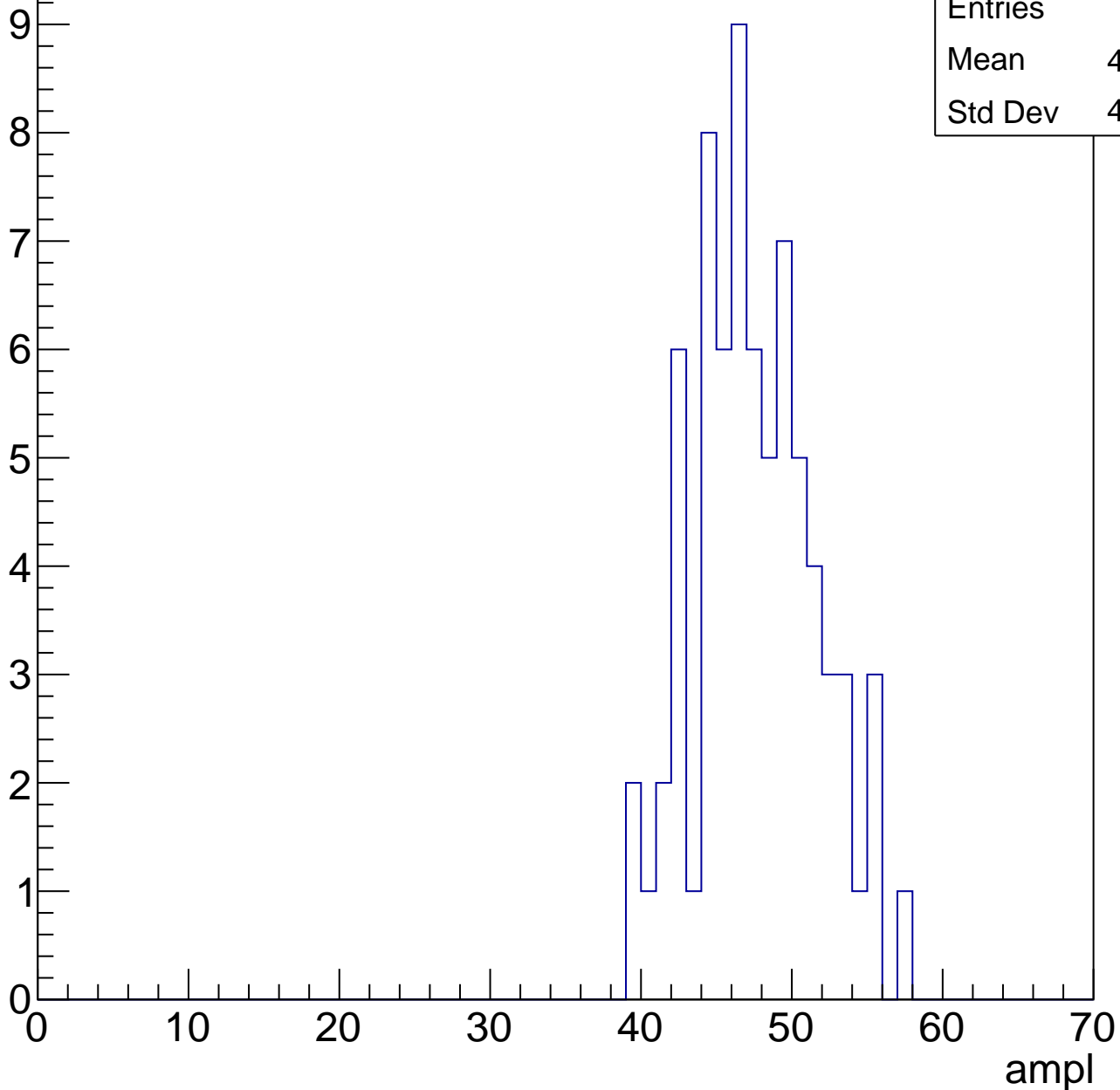


# B1L103S, U1-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	47.14
Std Dev	4.028

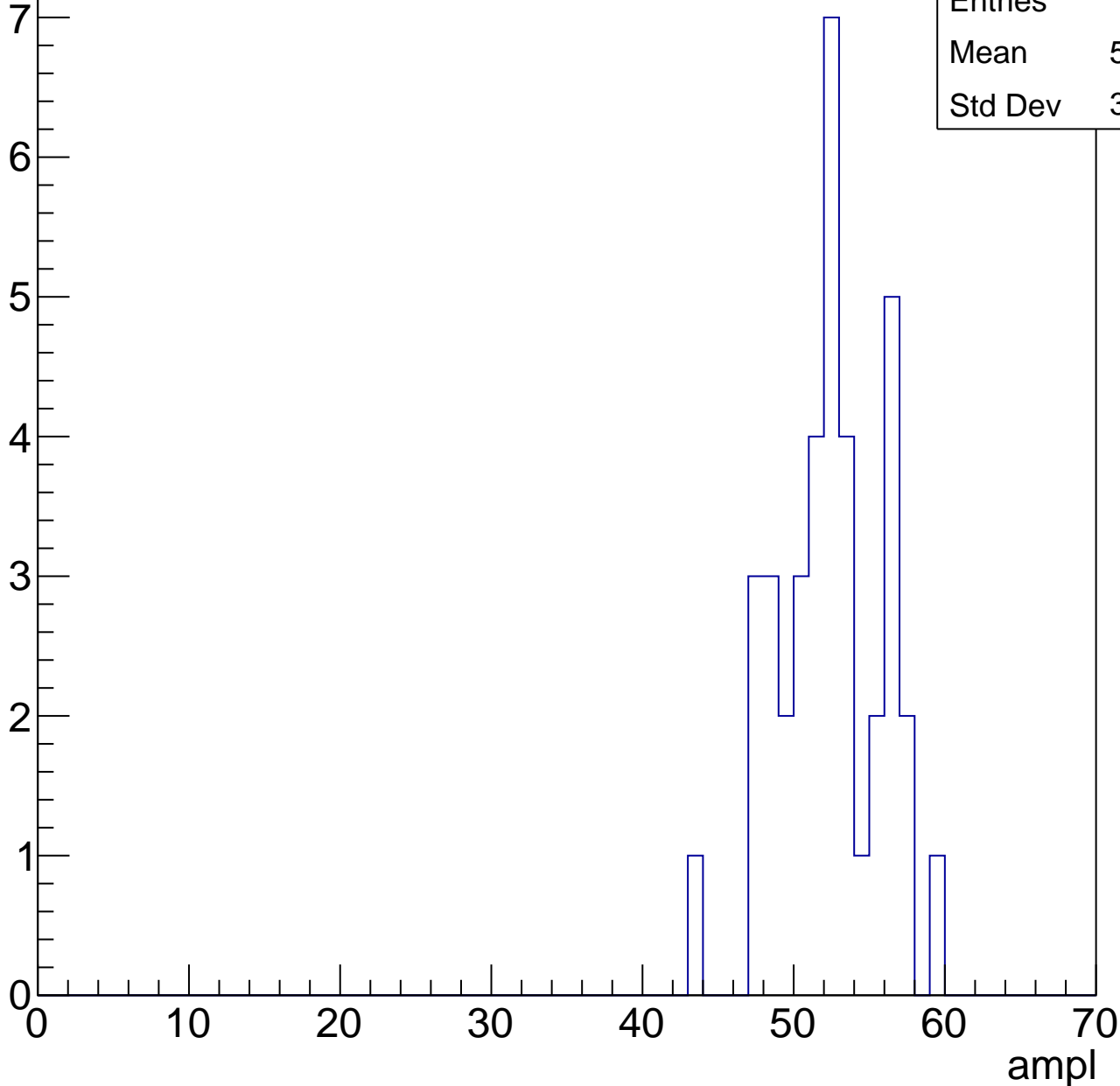


# B1L103S, U1-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	38
Mean	51.92
Std Dev	3.413

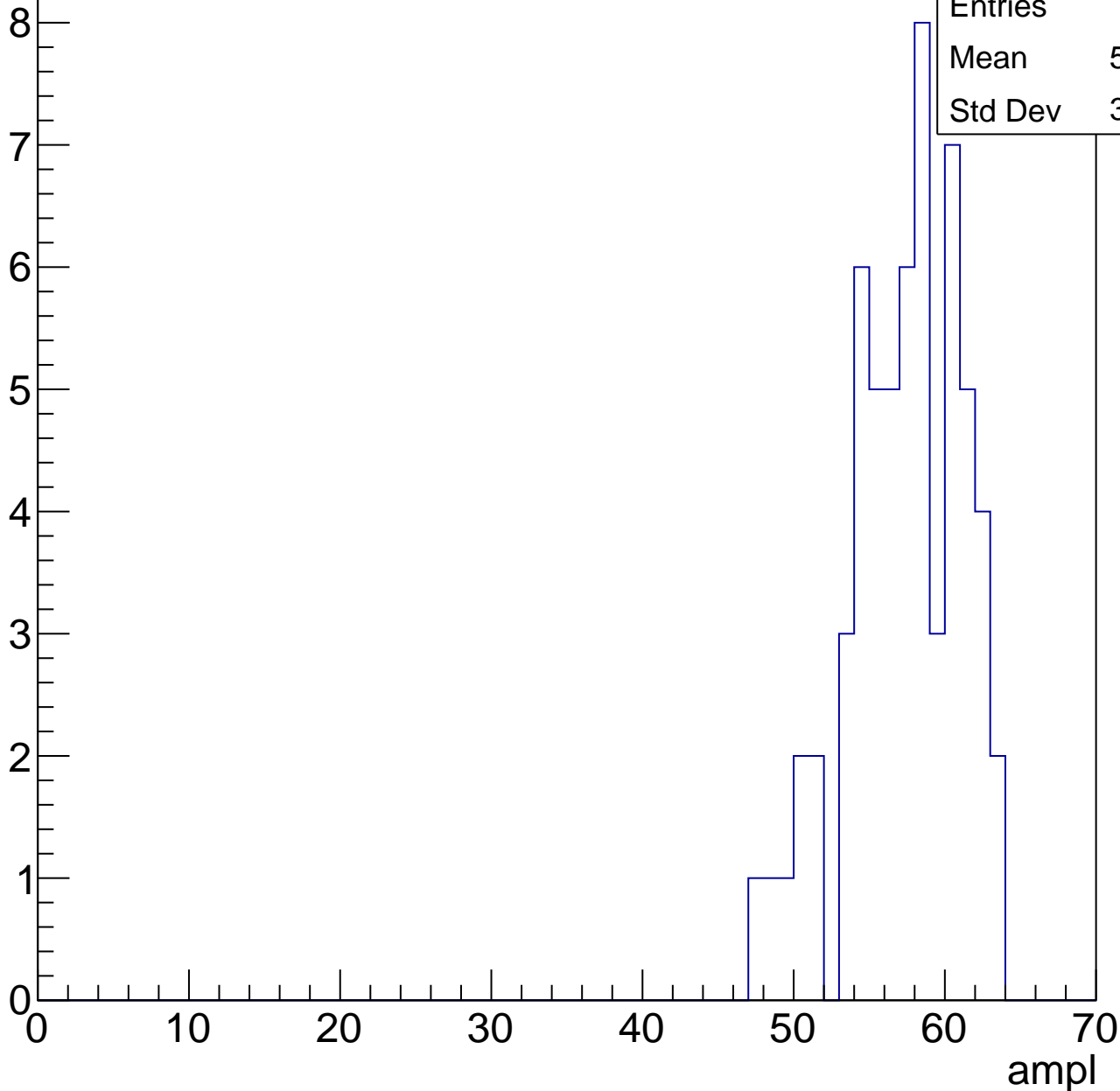


# B1L103S, U1-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	56.82
Std Dev	3.787

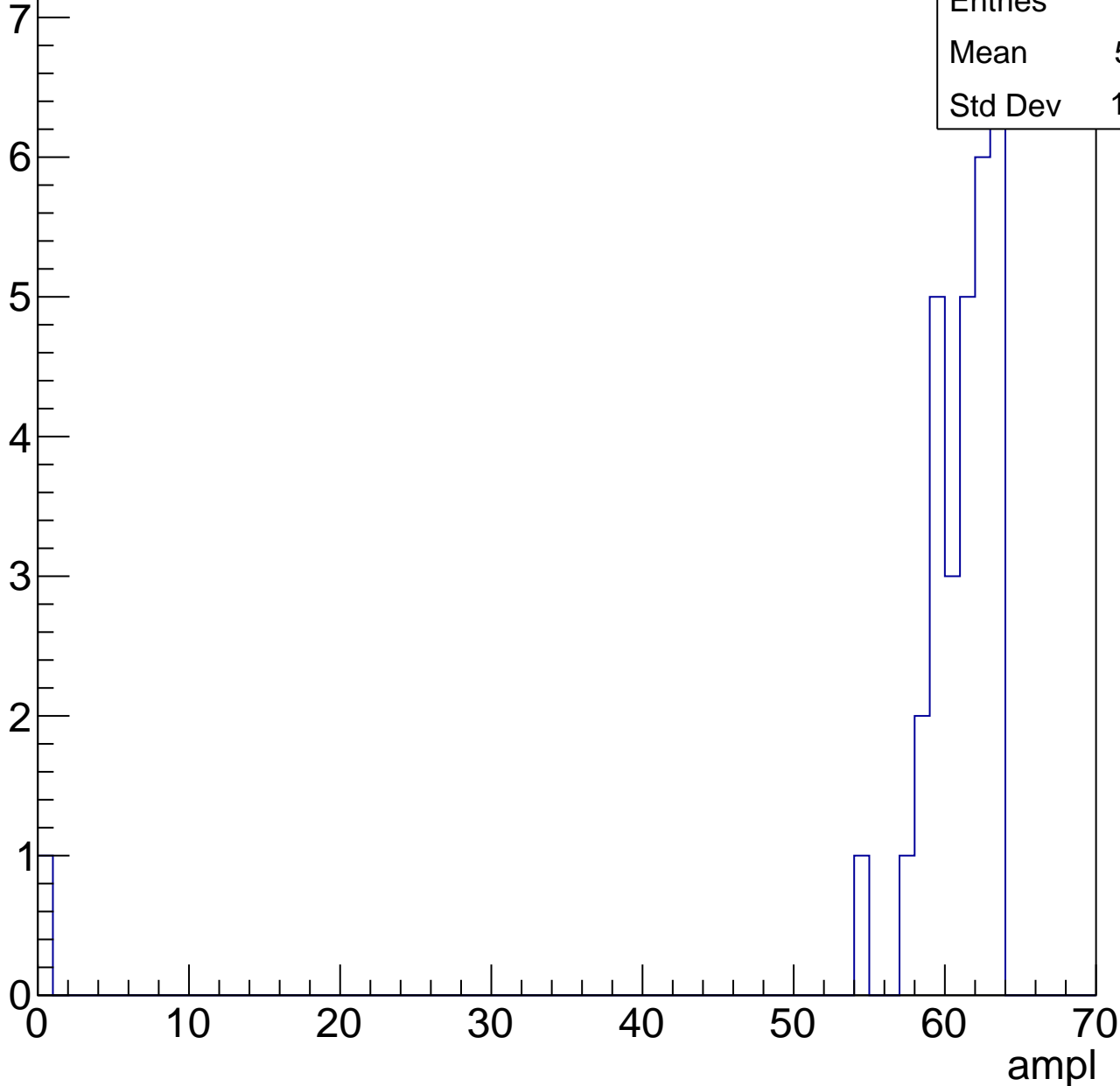


# B1L103S, U1-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	31
Mean	58.71
Std Dev	10.92





# B1L103S, U1-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1

0.8

0.6

0.4

0.2

0

0 10 20 30 40 50 60 70

ampl

Entries	2
Mean	61
Std Dev	2

# B1L103S, U1-ch99, adc0

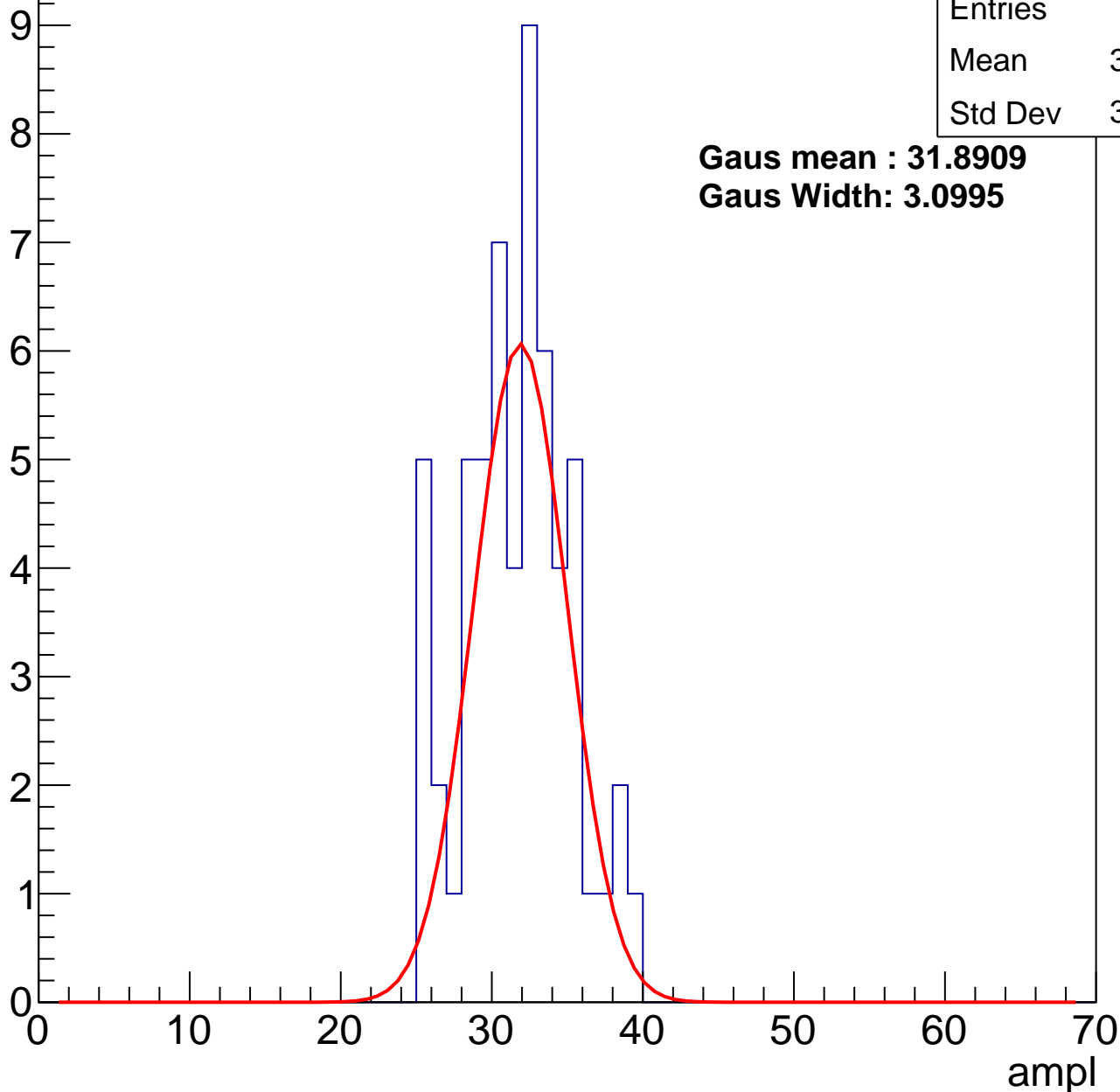
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	31.17
Std Dev	3.445

**Gaus mean : 31.8909**

**Gaus Width: 3.0995**



# B1L103S, U1-ch99, adc1

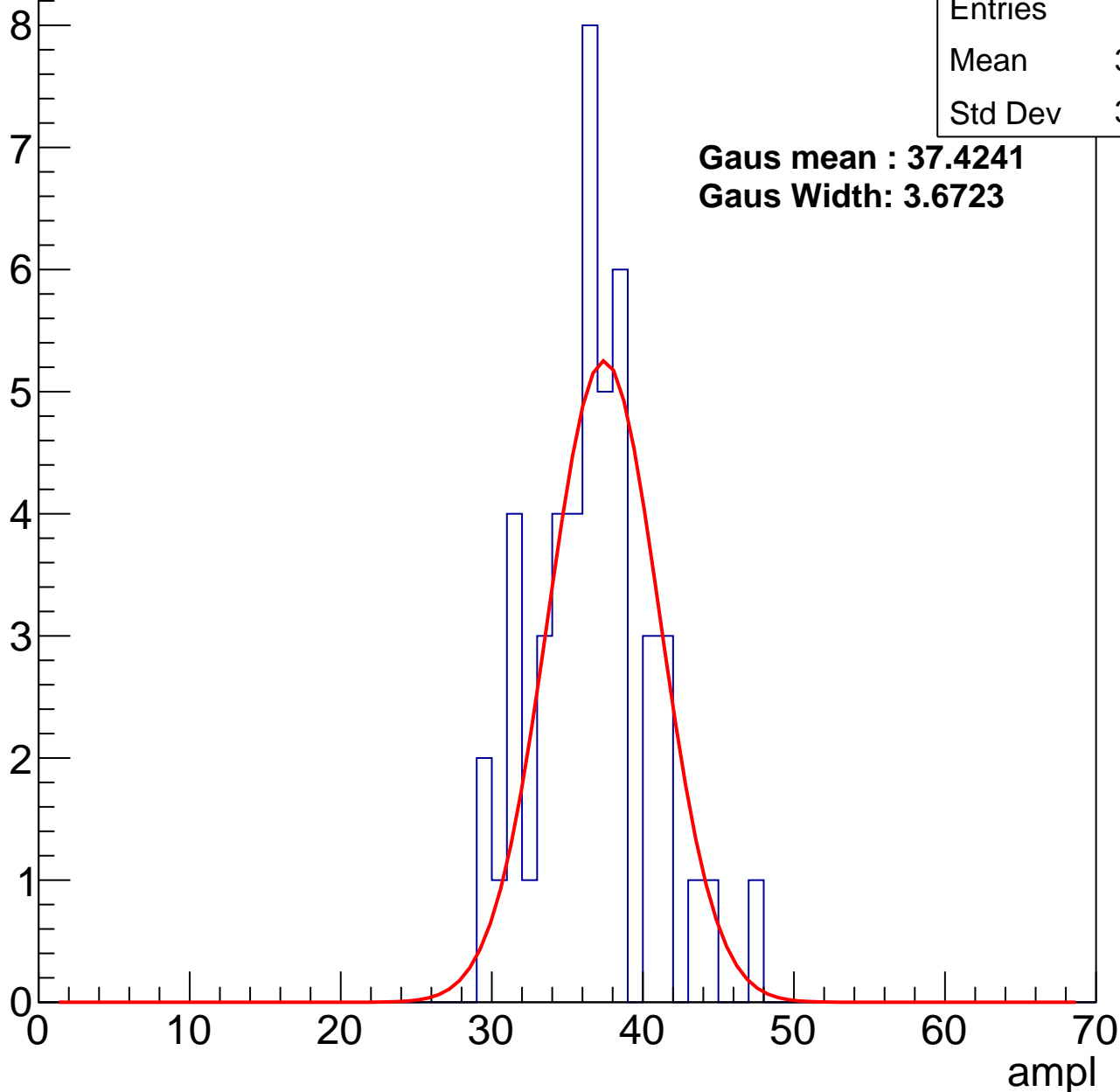
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	36.11
Std Dev	3.811

**Gaus mean : 37.4241**

**Gaus Width: 3.6723**



# B1L103S, U1-ch99, adc2

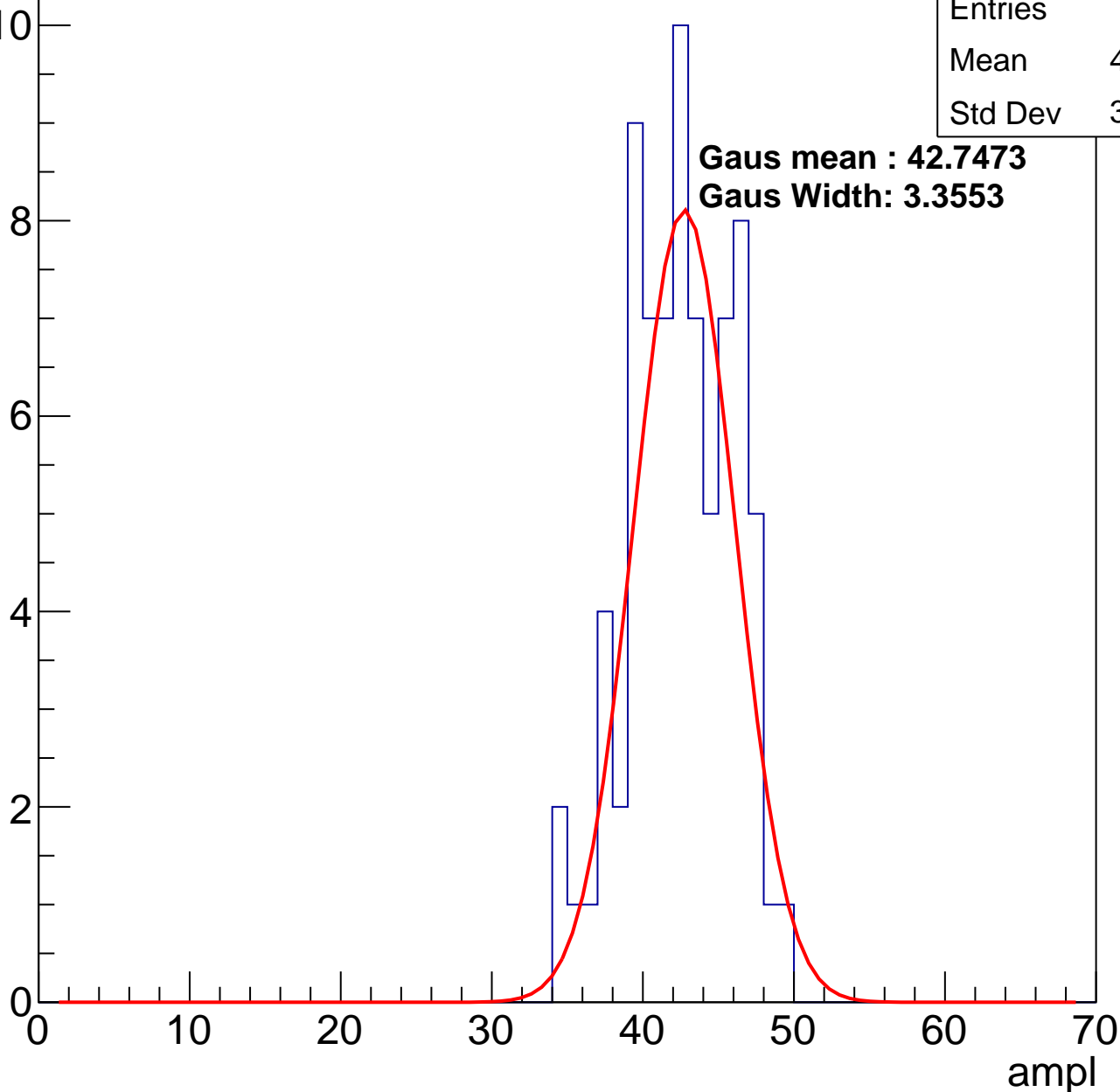
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	42.04
Std Dev	3.398

**Gaus mean : 42.7473**

**Gaus Width: 3.3553**

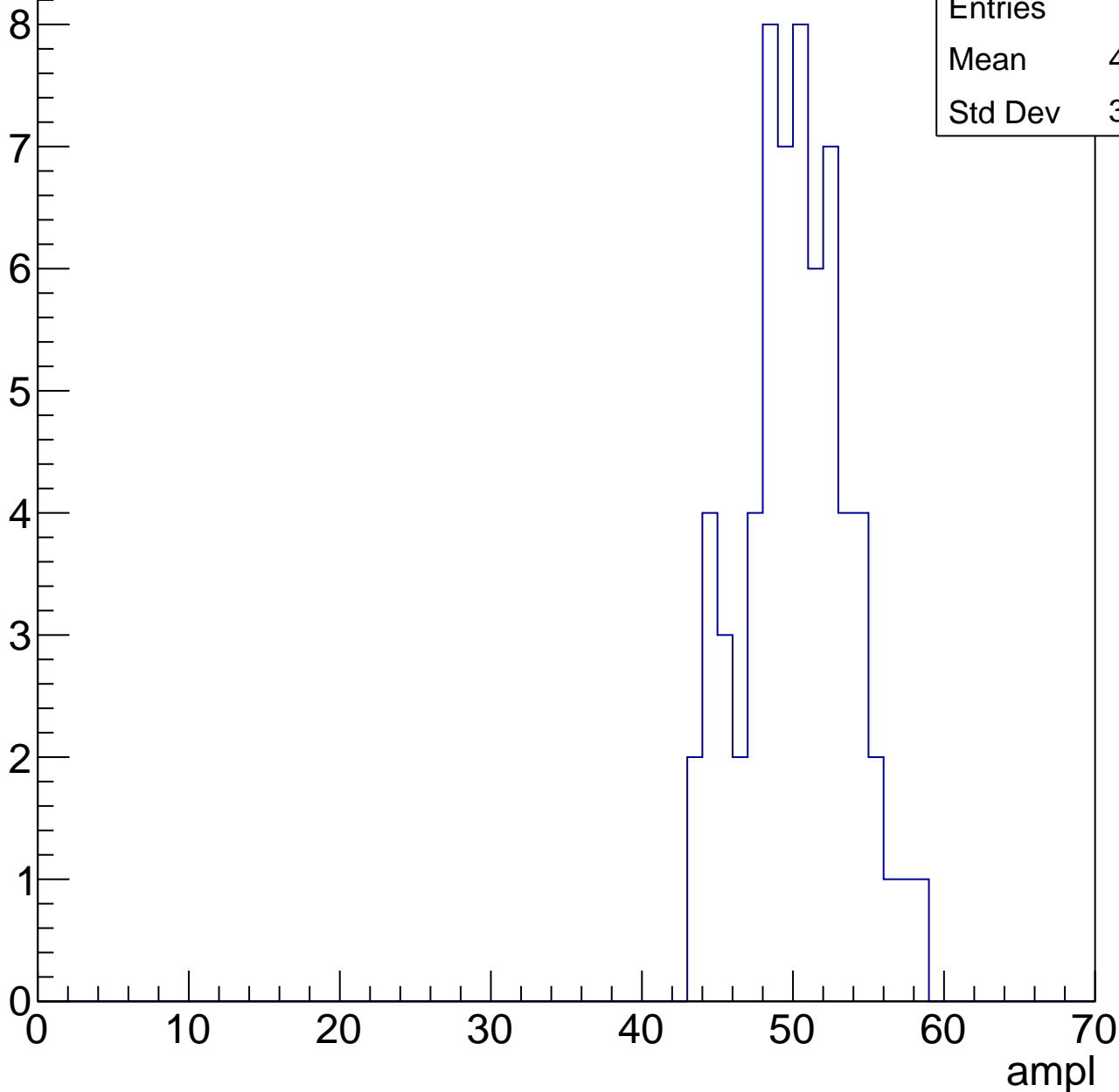


# B1L103S, U1-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	49.73
Std Dev	3.429

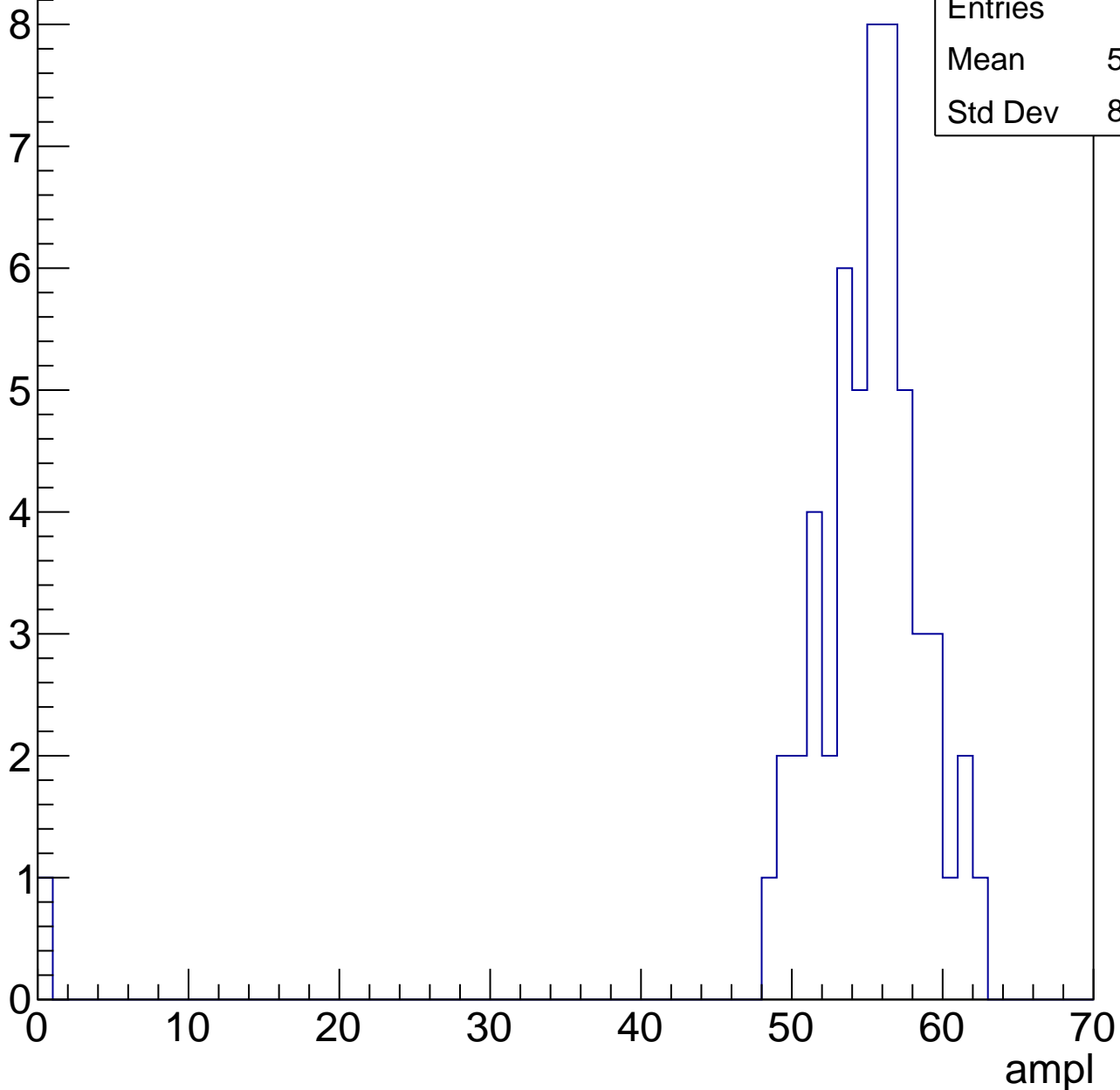


# B1L103S, U1-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	53.89
Std Dev	8.038

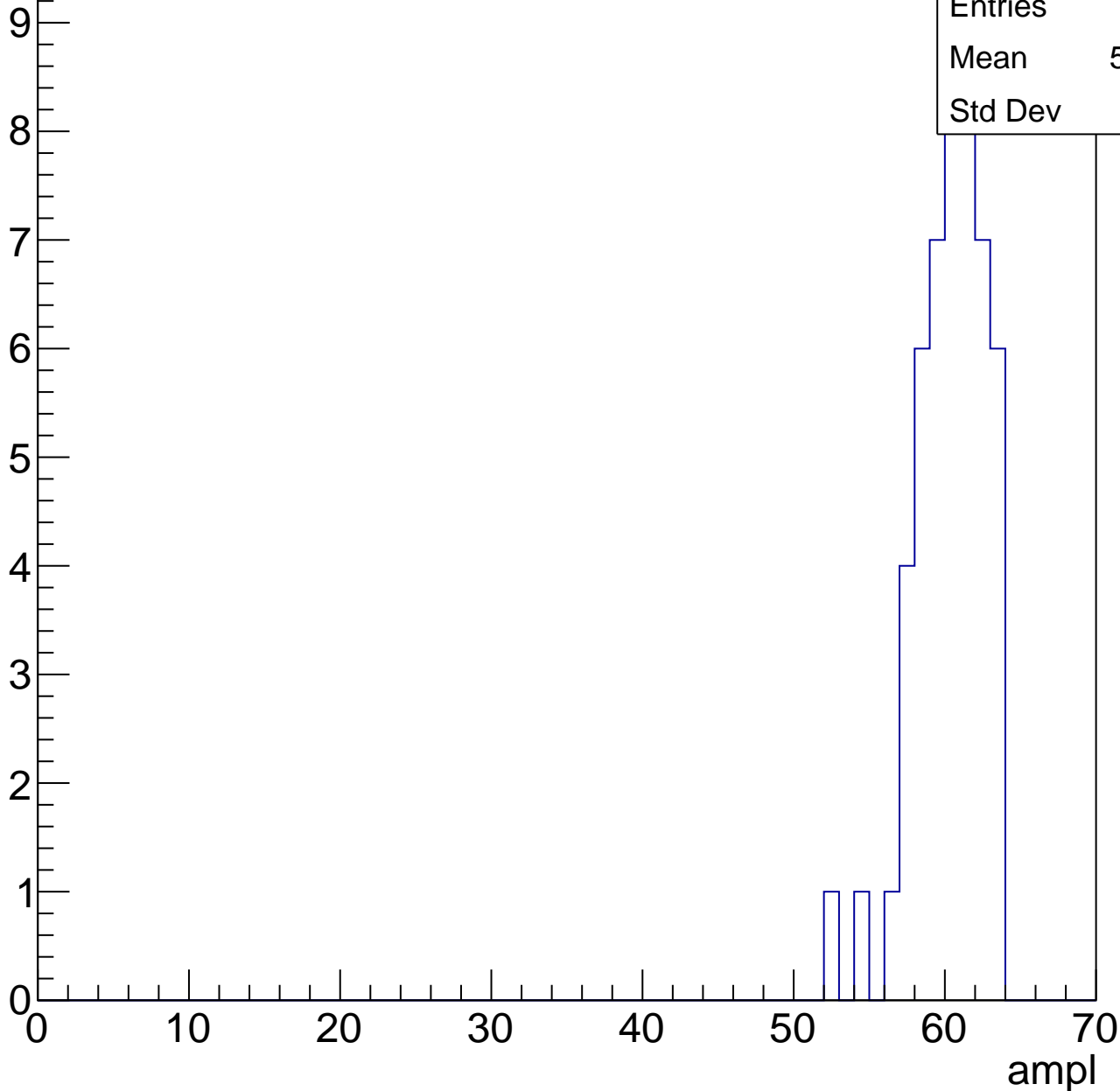


# B1L103S, U1-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

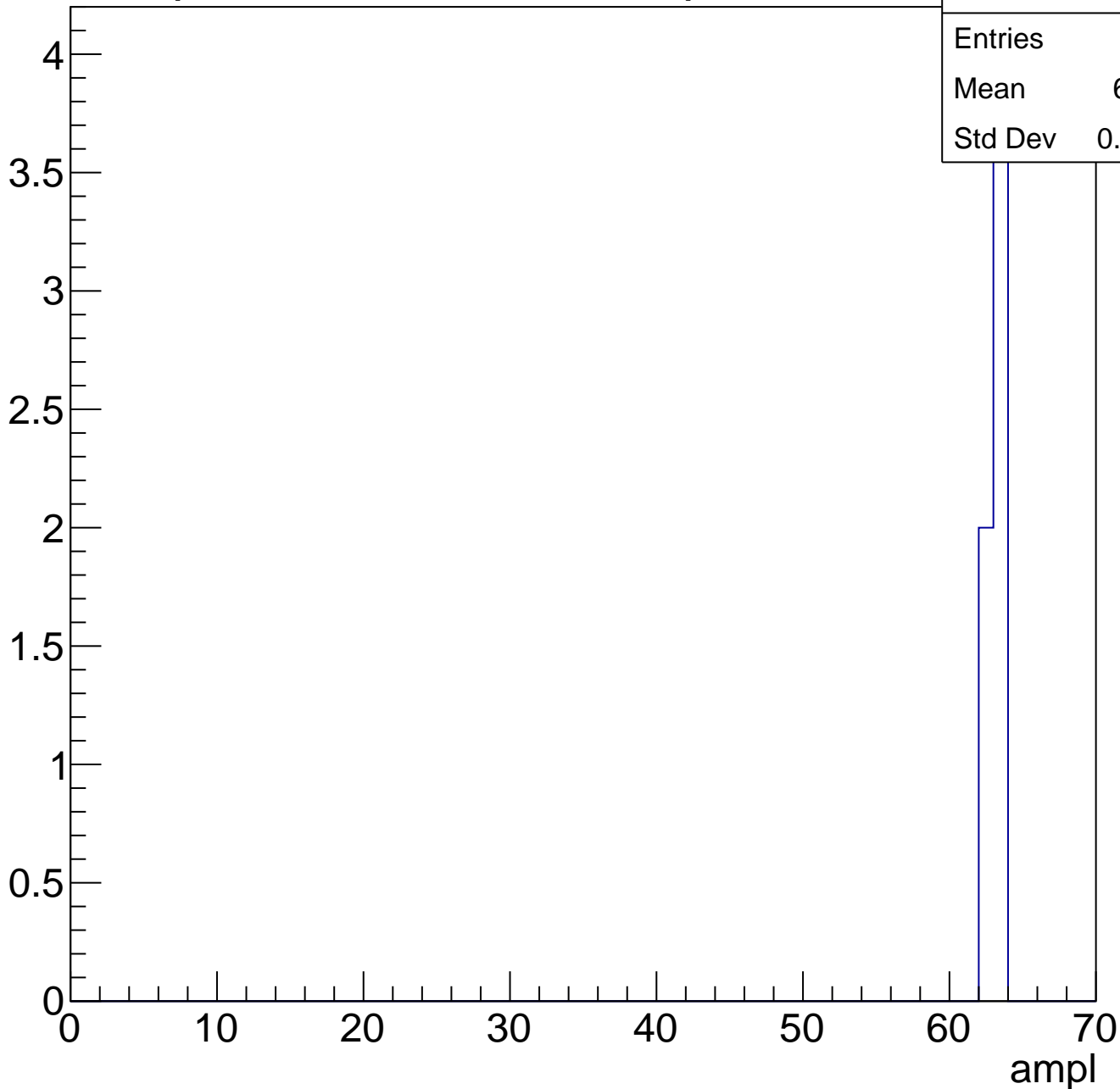
Entries	50
Mean	59.82
Std Dev	2.33



# B1L103S, U1-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U1-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U1-ch100, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	80
Mean	28.02
Std Dev	6.846

**Gaus mean : 28.9802**

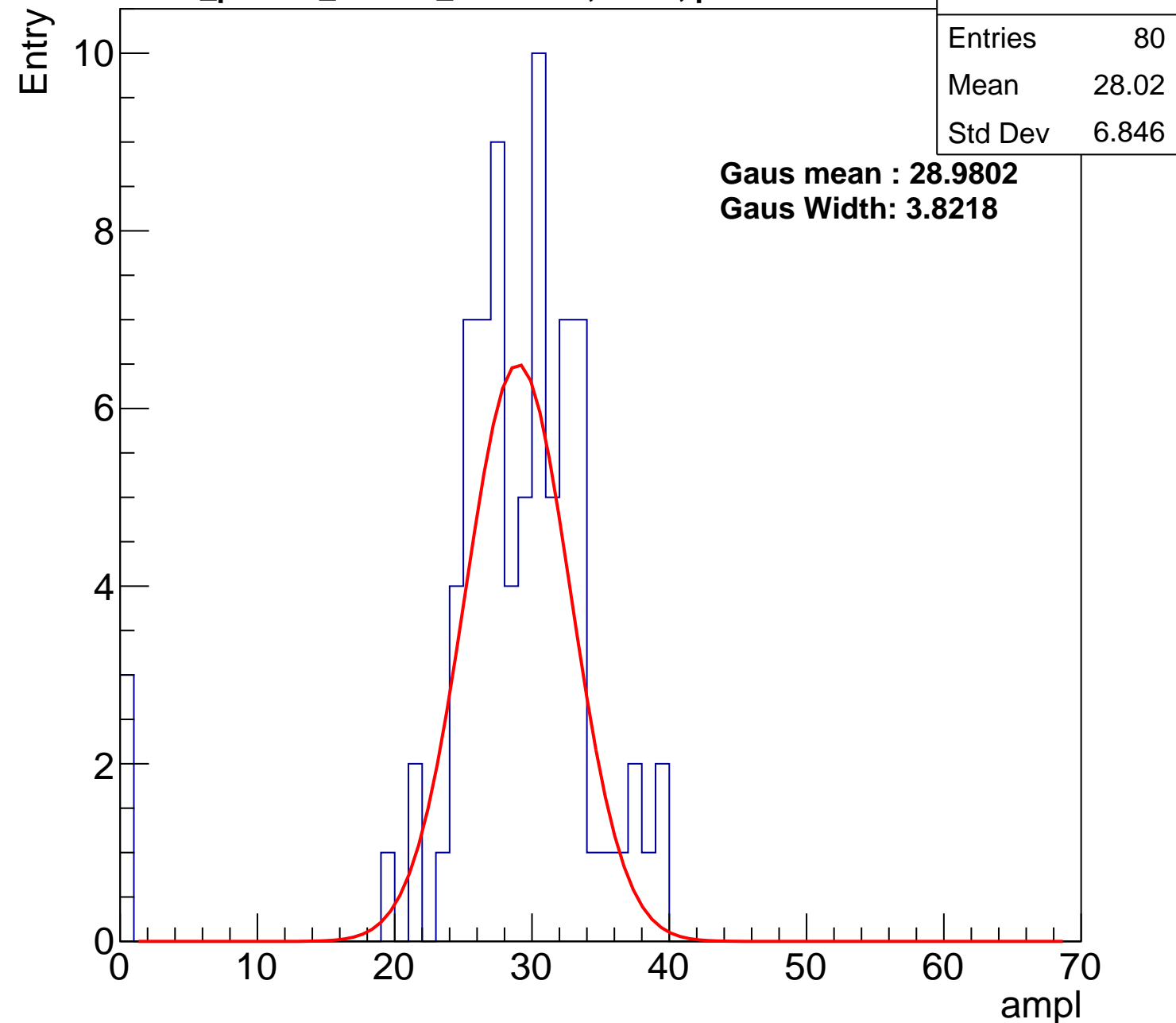
**Gaus Width: 3.8218**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U1-ch100, adc1

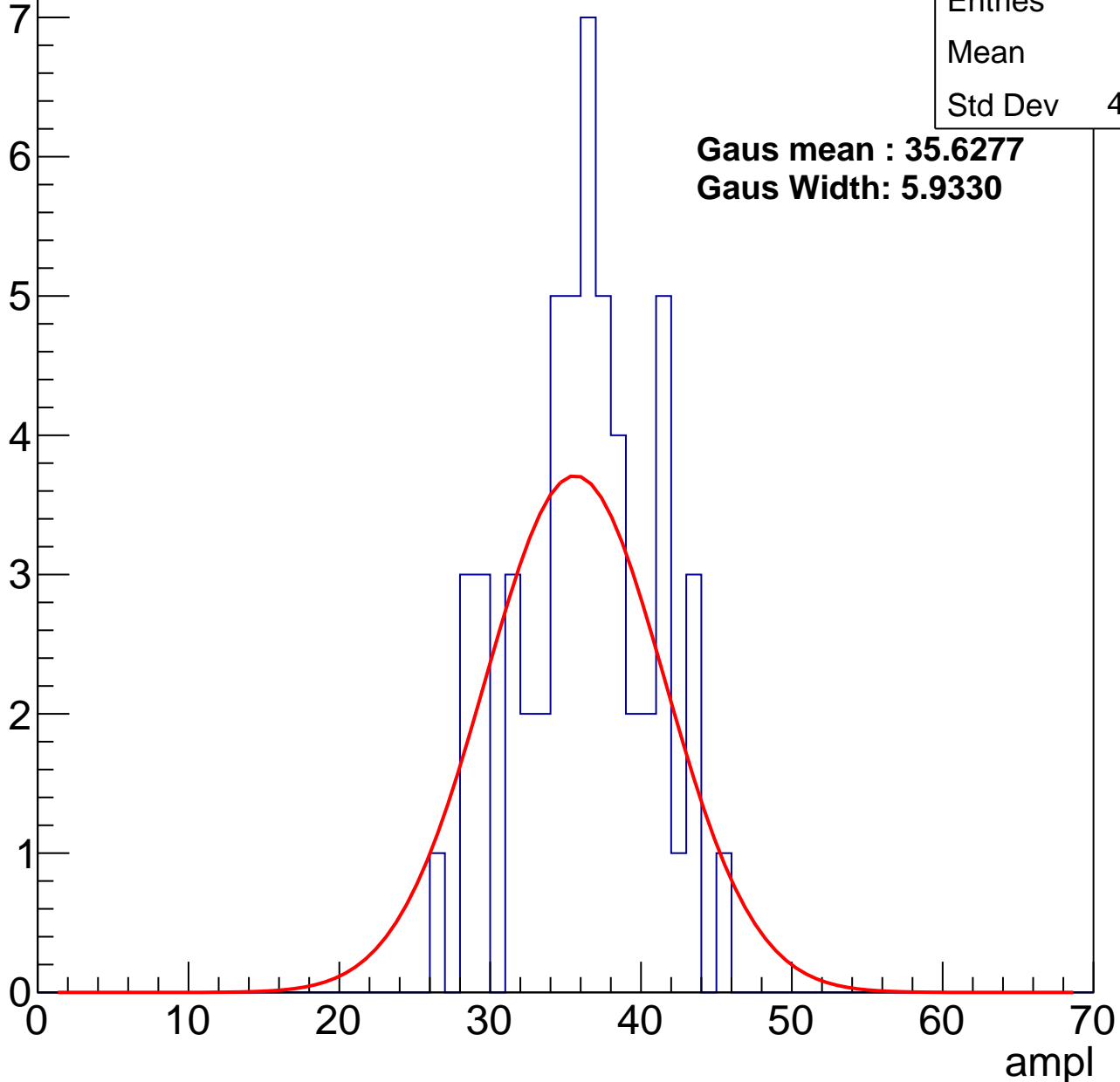
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	35.8
Std Dev	4.403

**Gaus mean : 35.6277**

**Gaus Width: 5.9330**



# B1L103S, U1-ch100, adc2

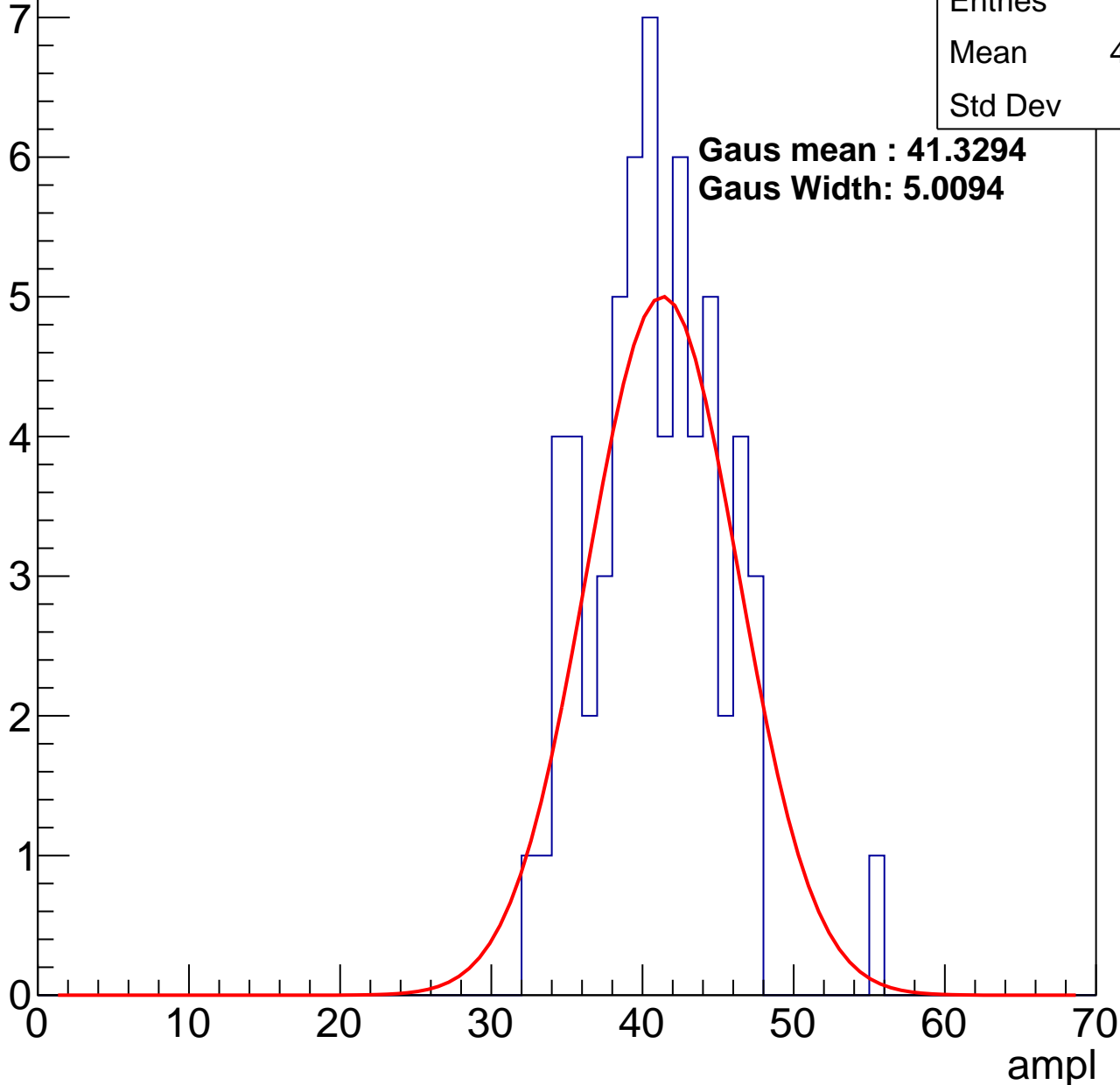
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	40.42
Std Dev	4.29

**Gaus mean : 41.3294**

**Gaus Width: 5.0094**

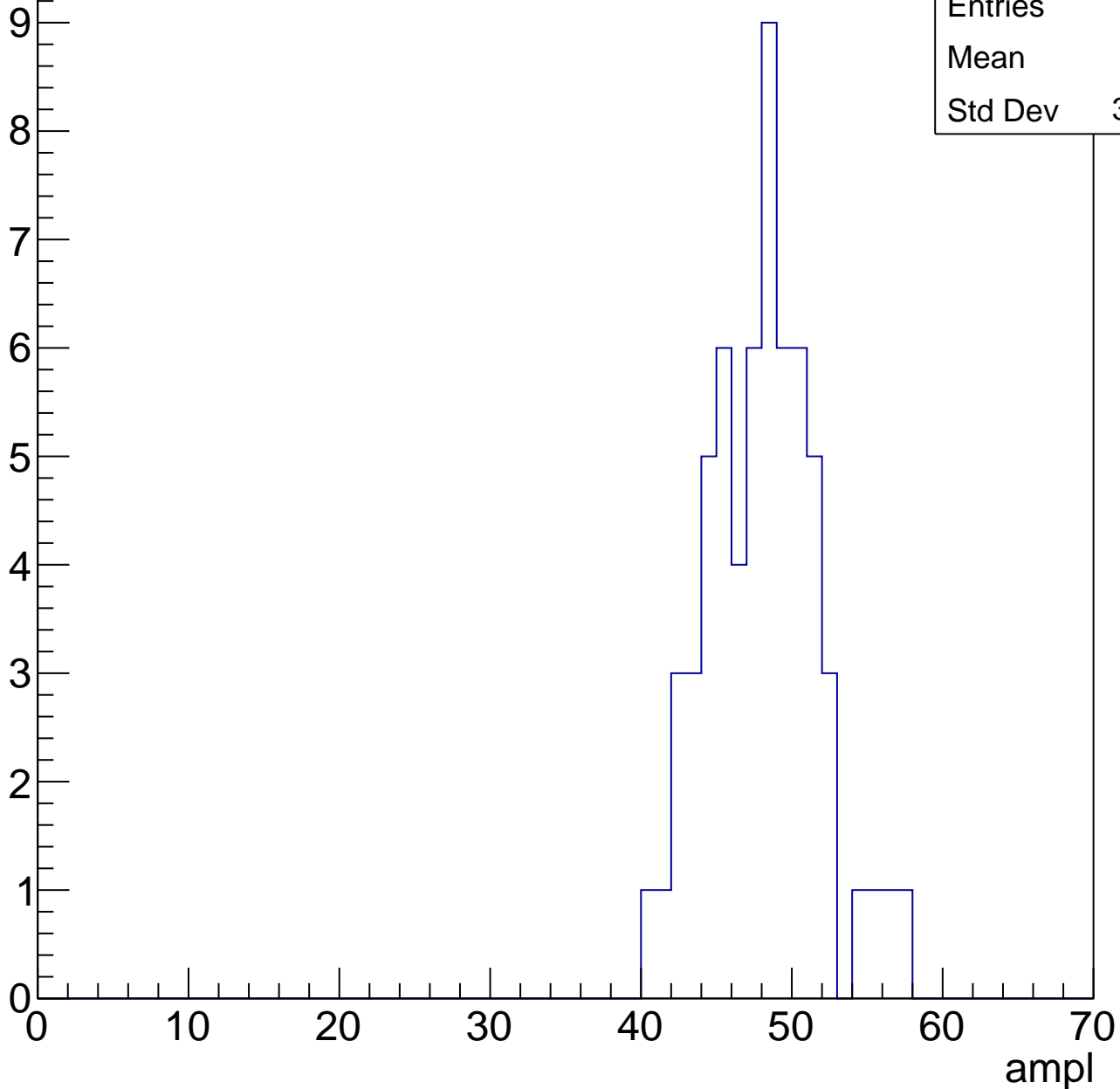


# B1L103S, U1-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	47.6
Std Dev	3.581

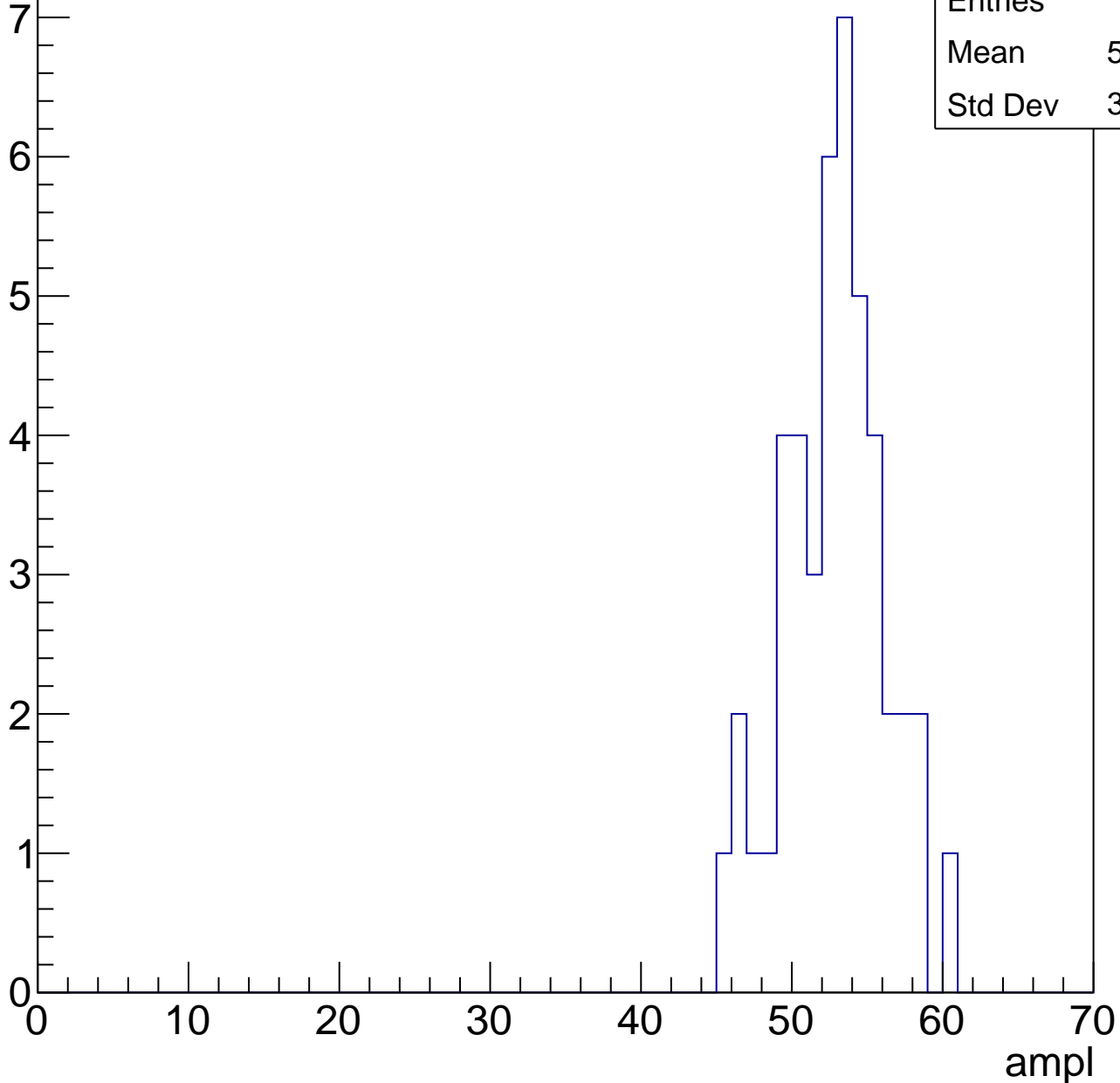


# B1L103S, U1-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	52.36
Std Dev	3.308

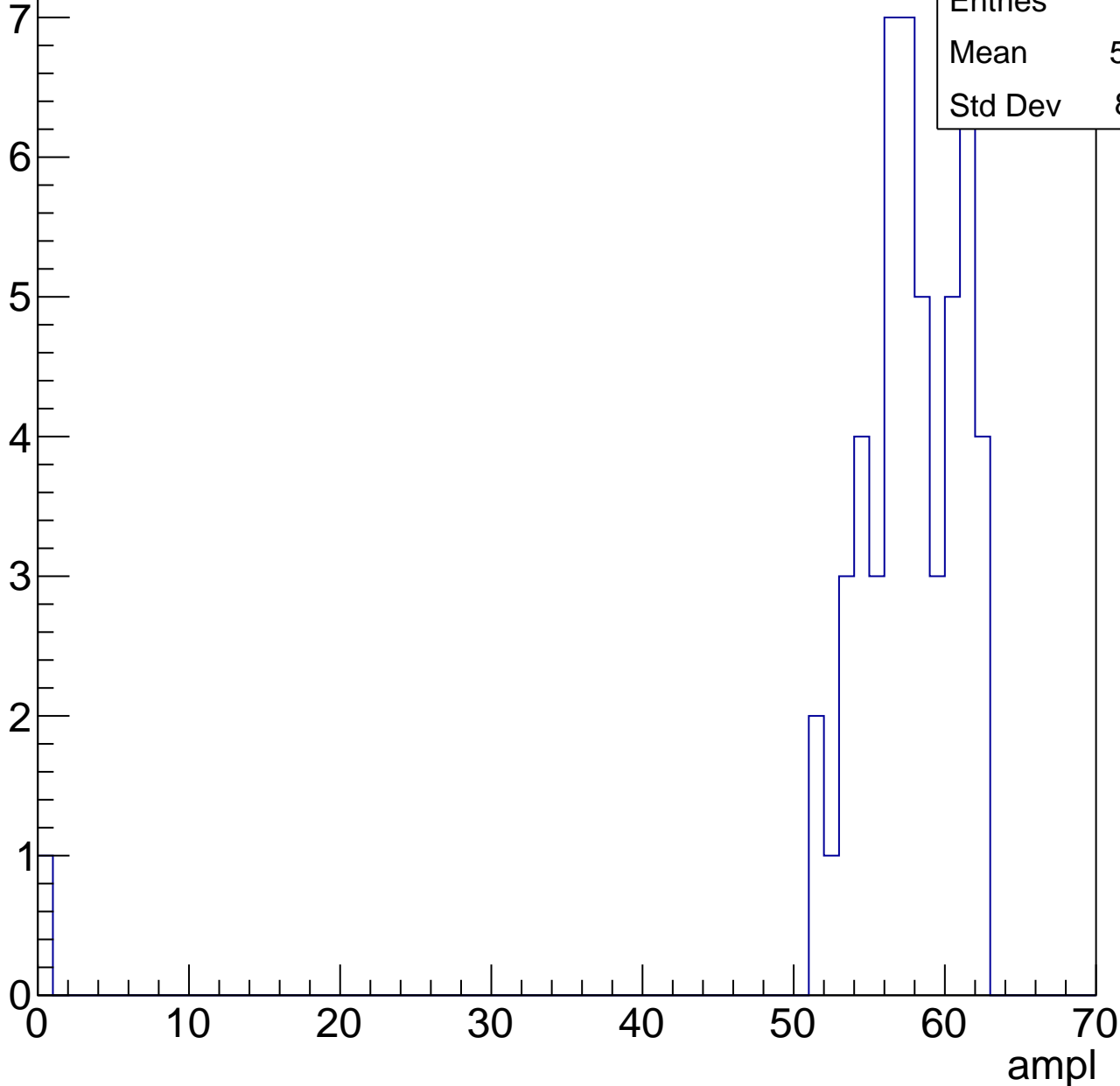


# B1L103S, U1-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	56.29
Std Dev	8.431

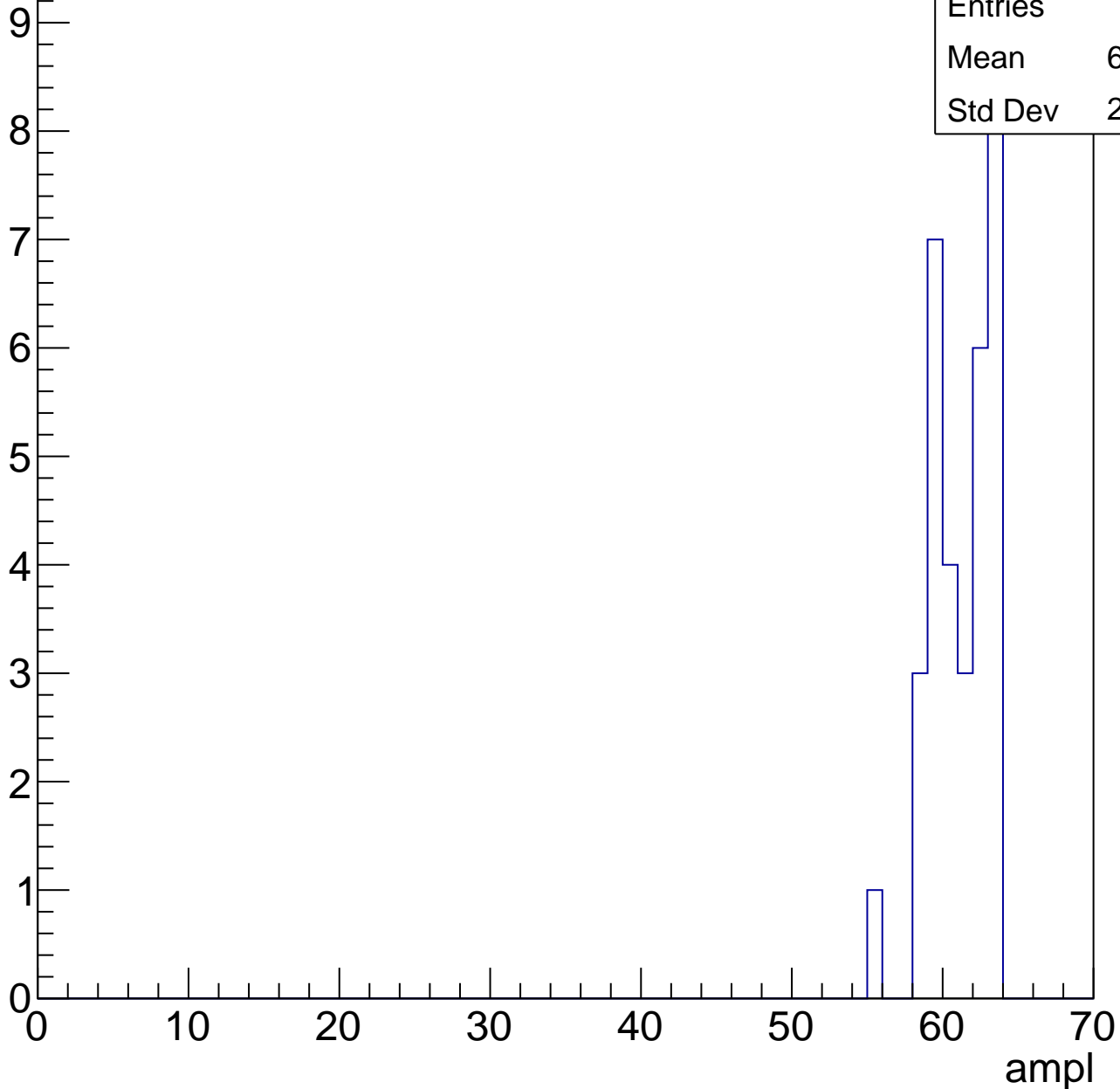


# B1L103S, U1-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	33
Mean	60.73
Std Dev	2.019





# B1L103S, U1-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	63
Std Dev	0

# B1L103S, U1-ch101, adc0

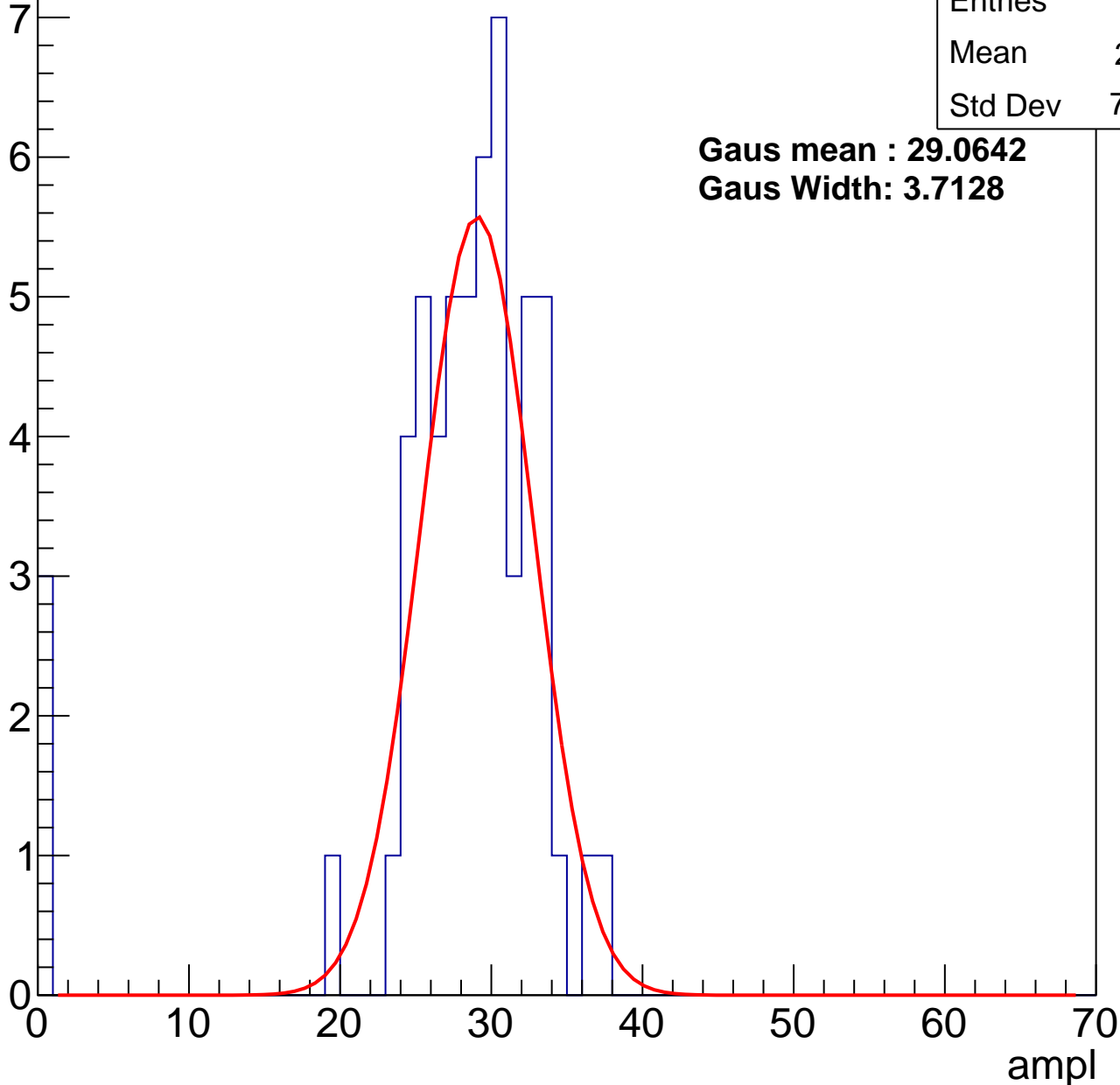
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	27.21
Std Dev	7.254

**Gaus mean : 29.0642**

**Gaus Width: 3.7128**



# B1L103S, U1-ch101, adc1

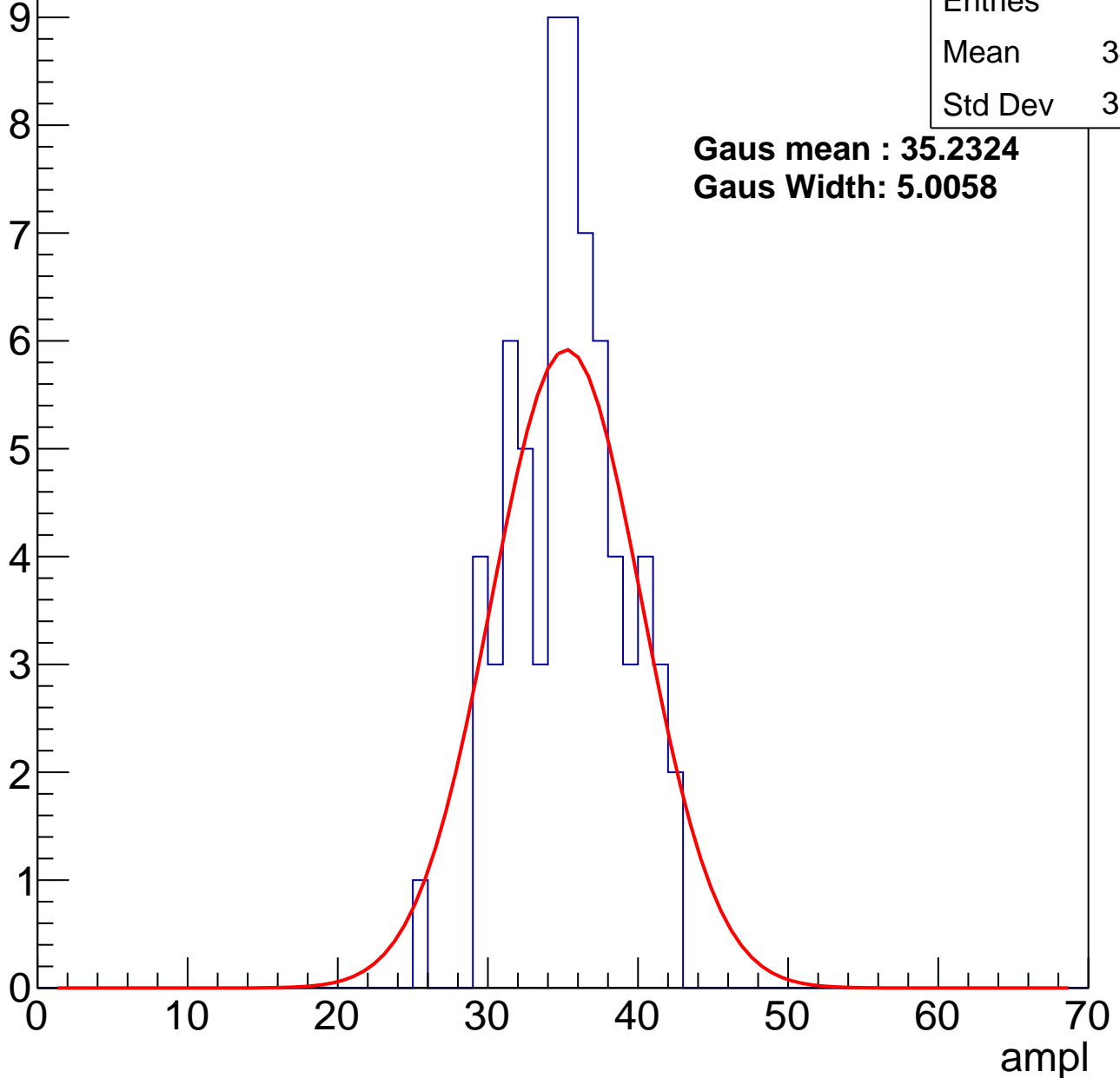
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	34.88
Std Dev	3.614

**Gaus mean : 35.2324**

**Gaus Width: 5.0058**



# B1L103S, U1-ch101, adc2

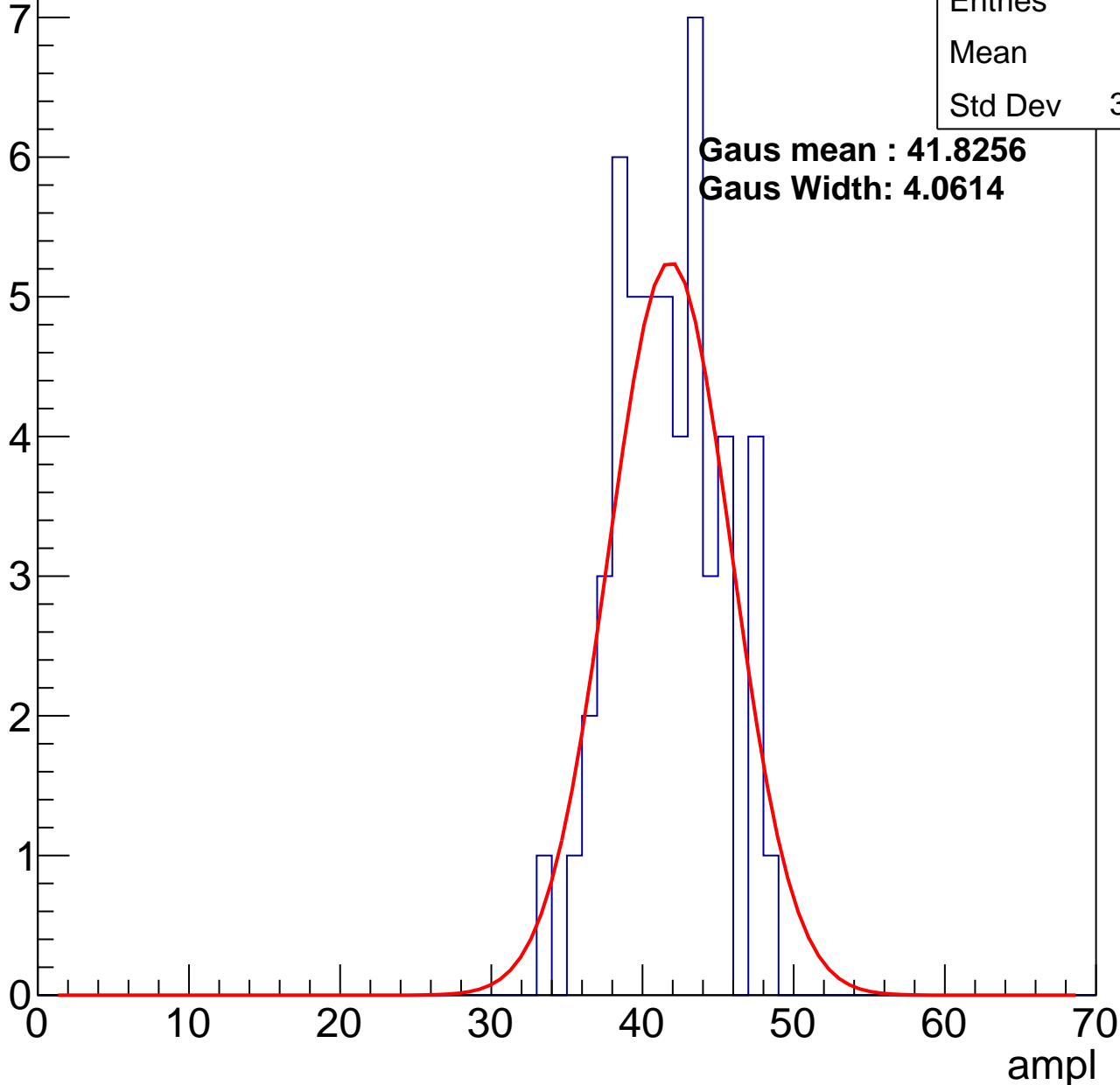
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	41.1
Std Dev	3.408

**Gaus mean : 41.8256**

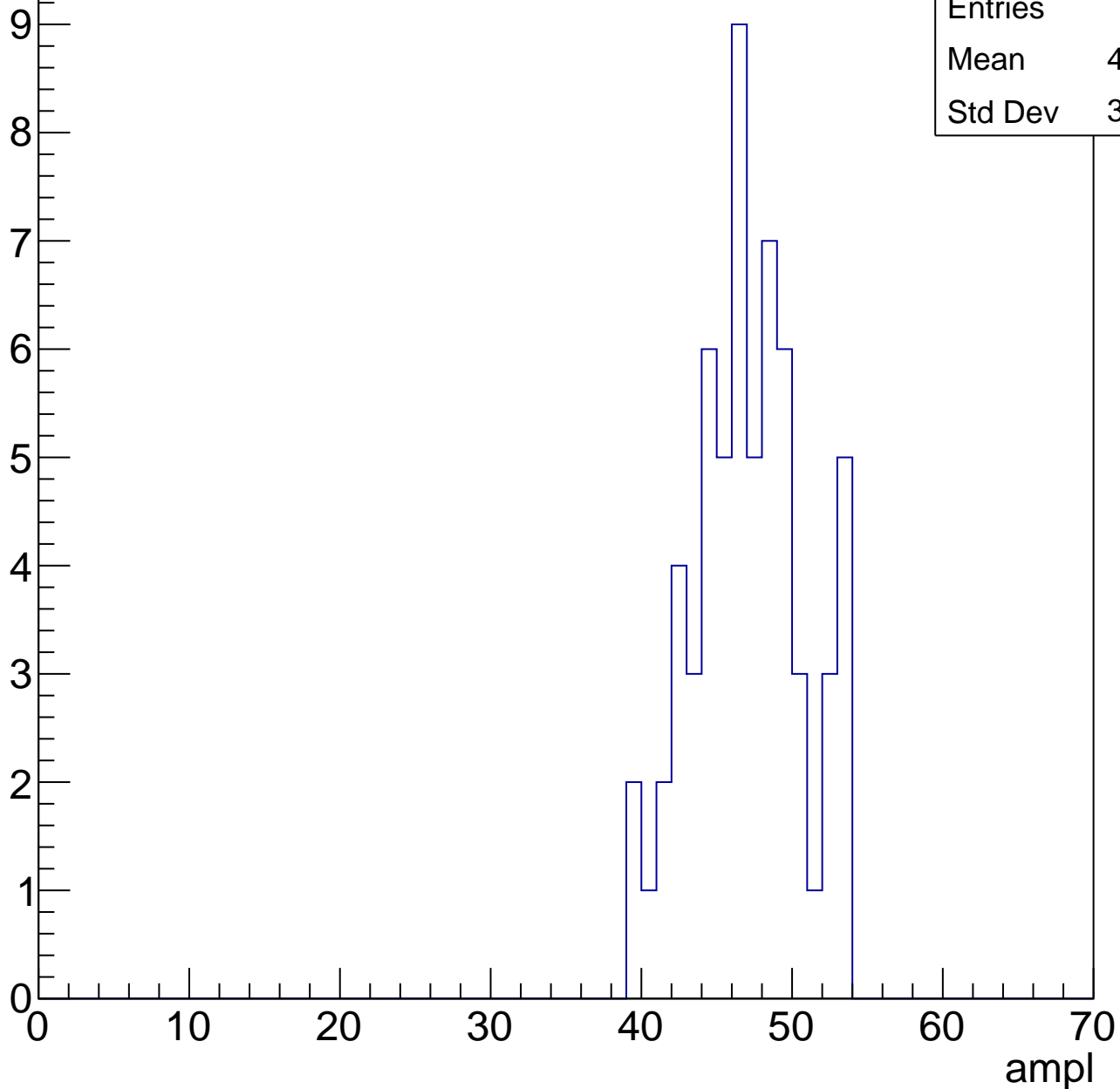
**Gaus Width: 4.0614**



# B1L103S, U1-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



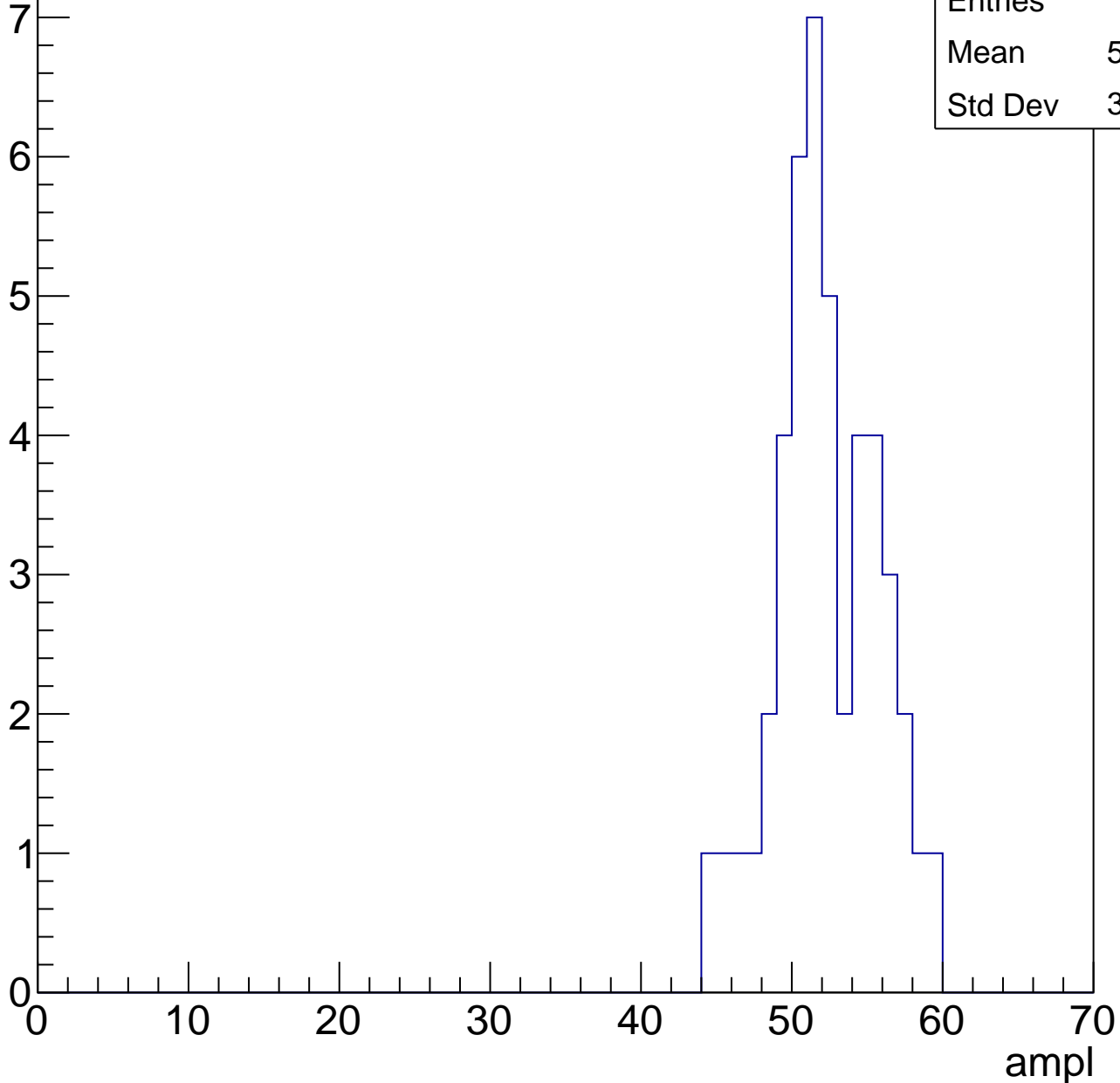
Entries	62
Mean	46.56
Std Dev	3.586

# B1L103S, U1-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

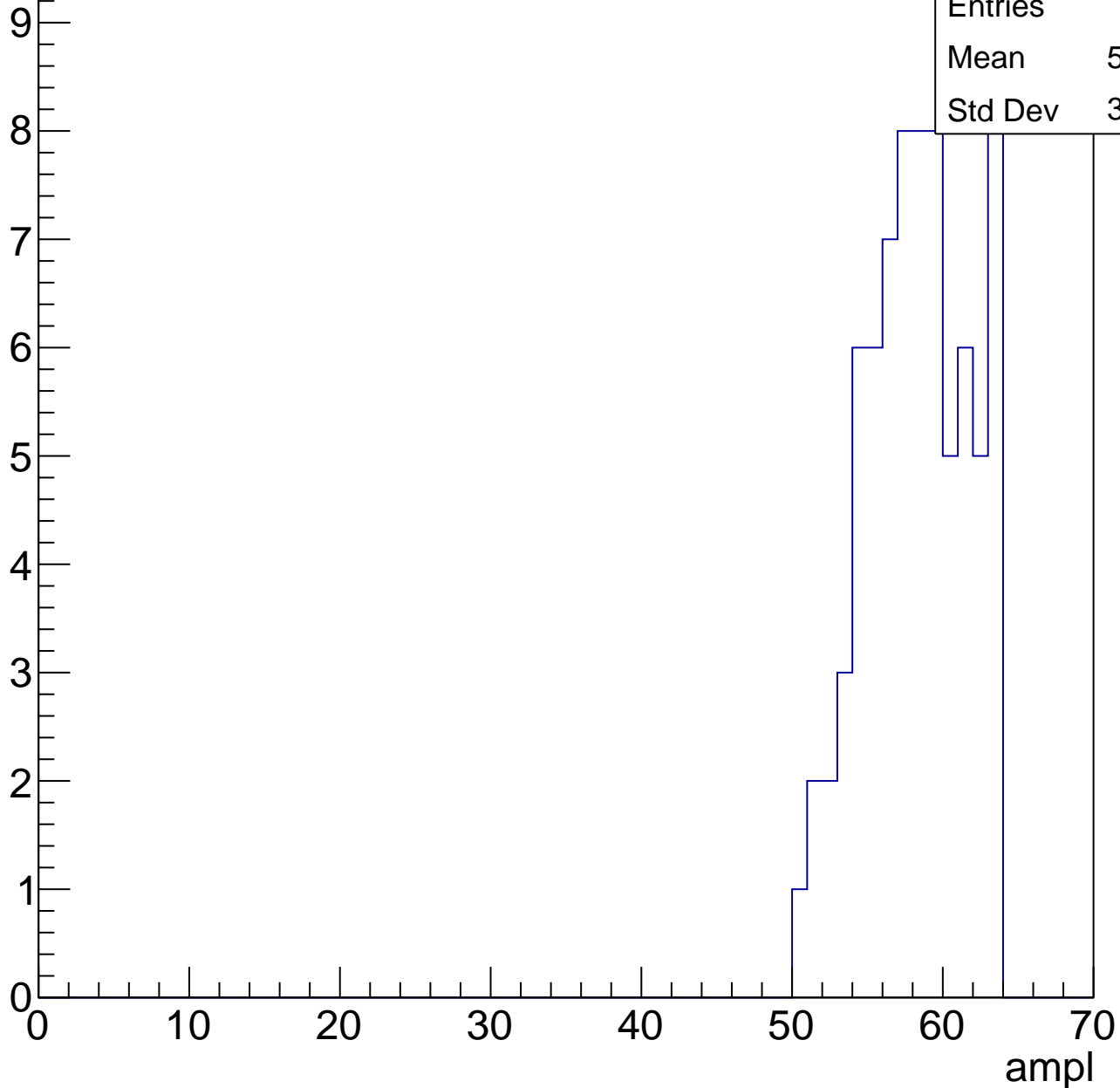
Entries	45
Mean	51.82
Std Dev	3.362



# B1L103S, U1-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

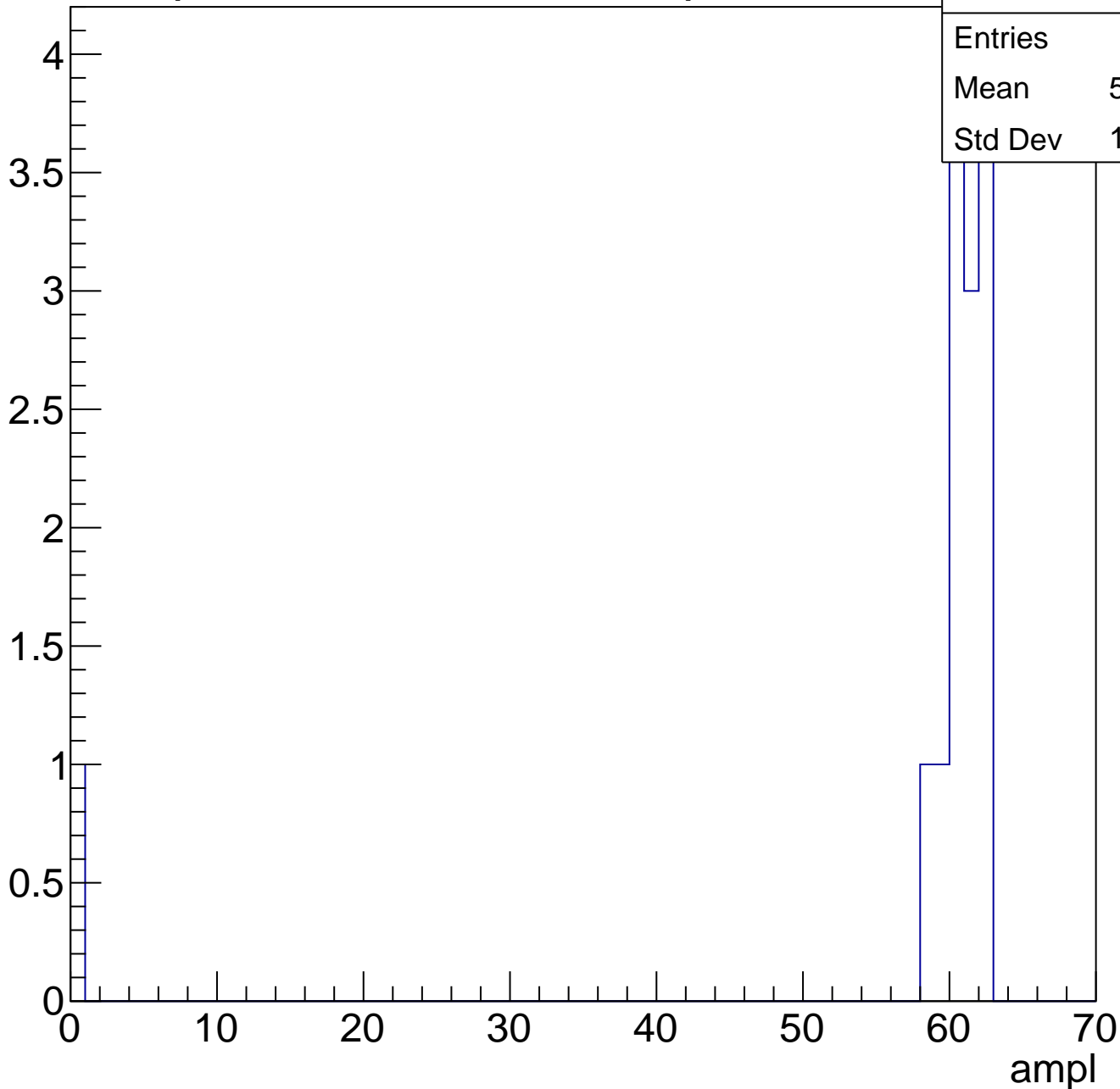
Entry



# B1L103S, U1-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

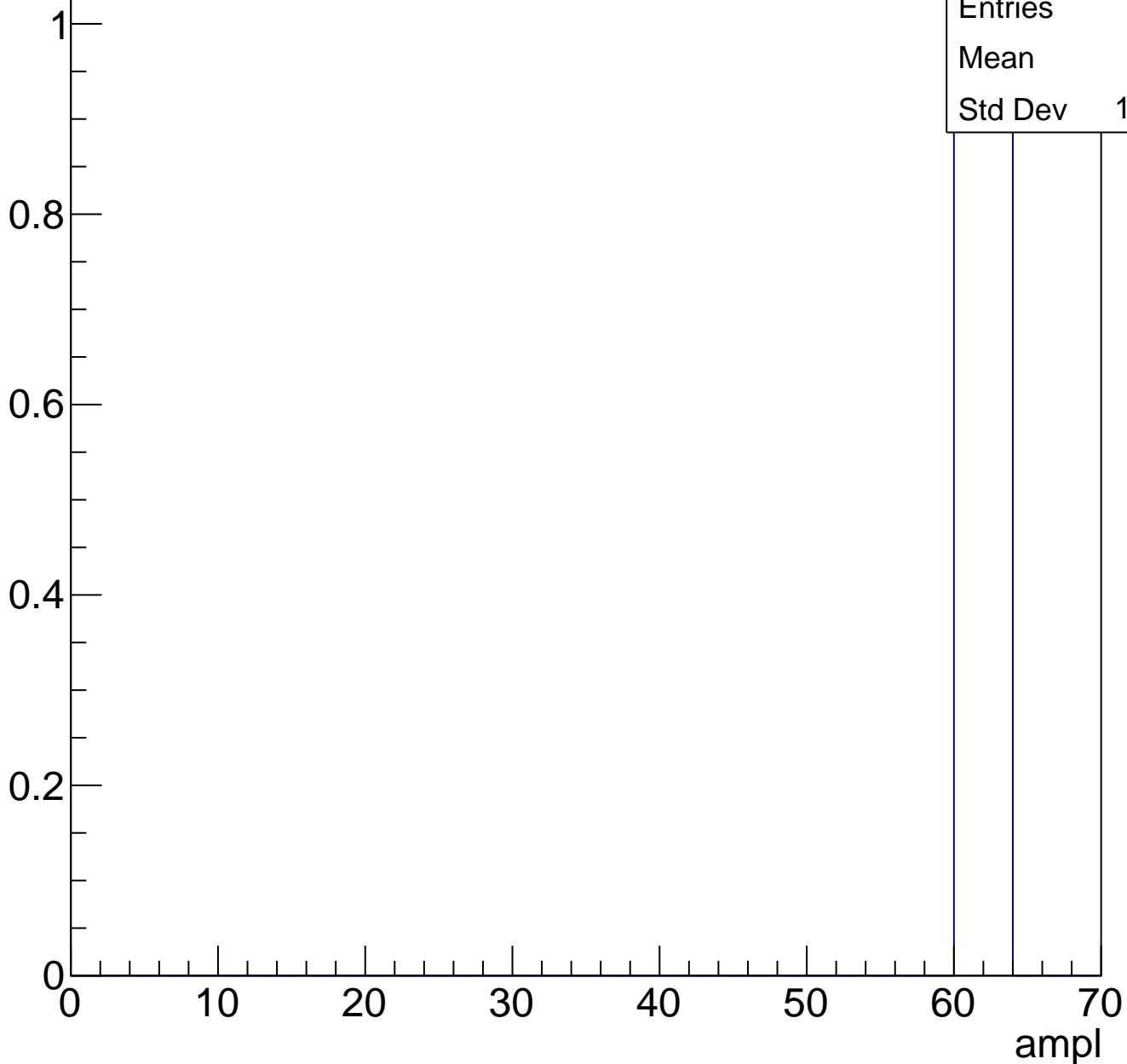




# B1L103S, U1-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch102, adc0

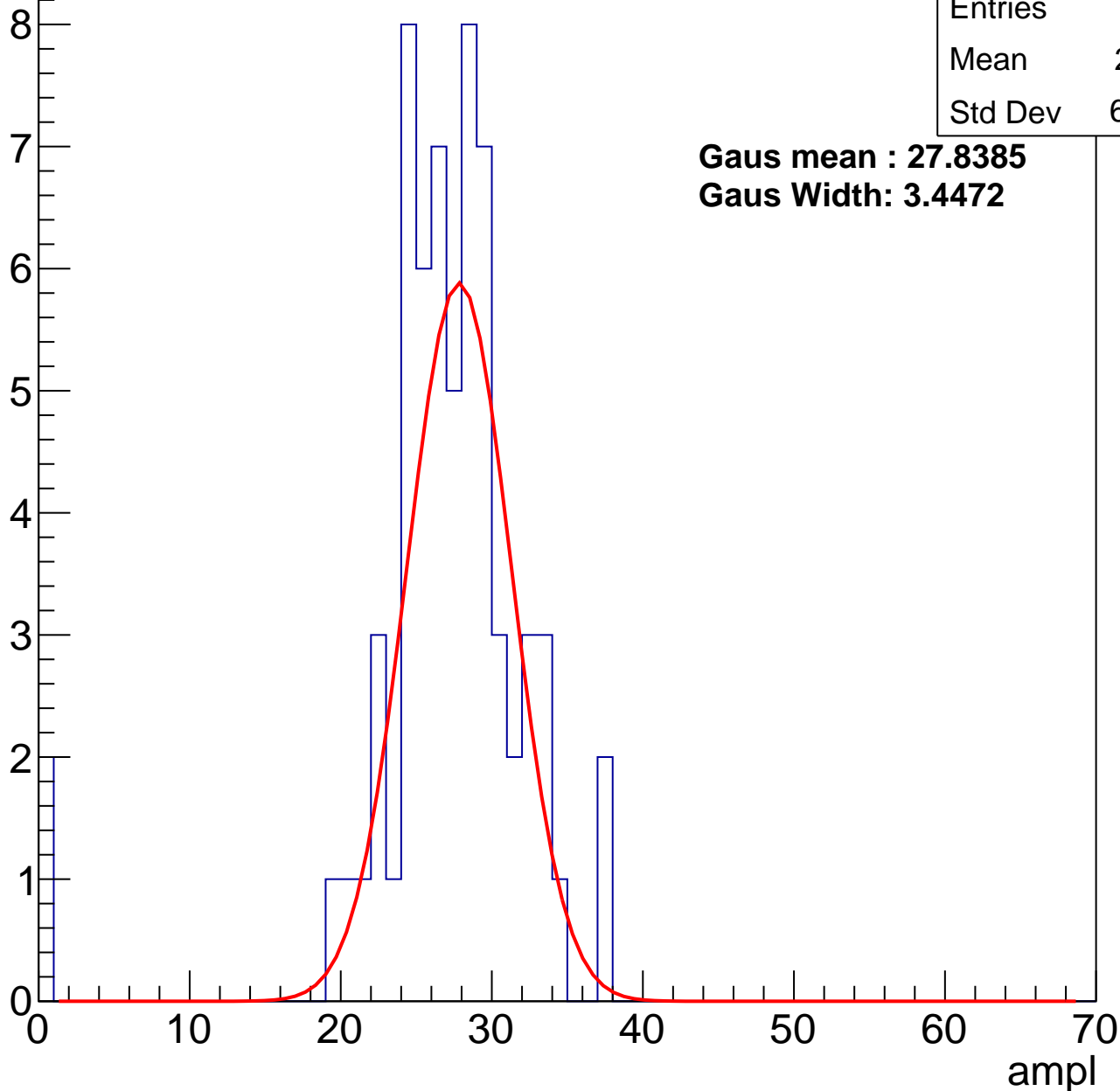
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	26.41
Std Dev	6.002

**Gaus mean : 27.8385**

**Gaus Width: 3.4472**



# B1L103S, U1-ch102, adc1

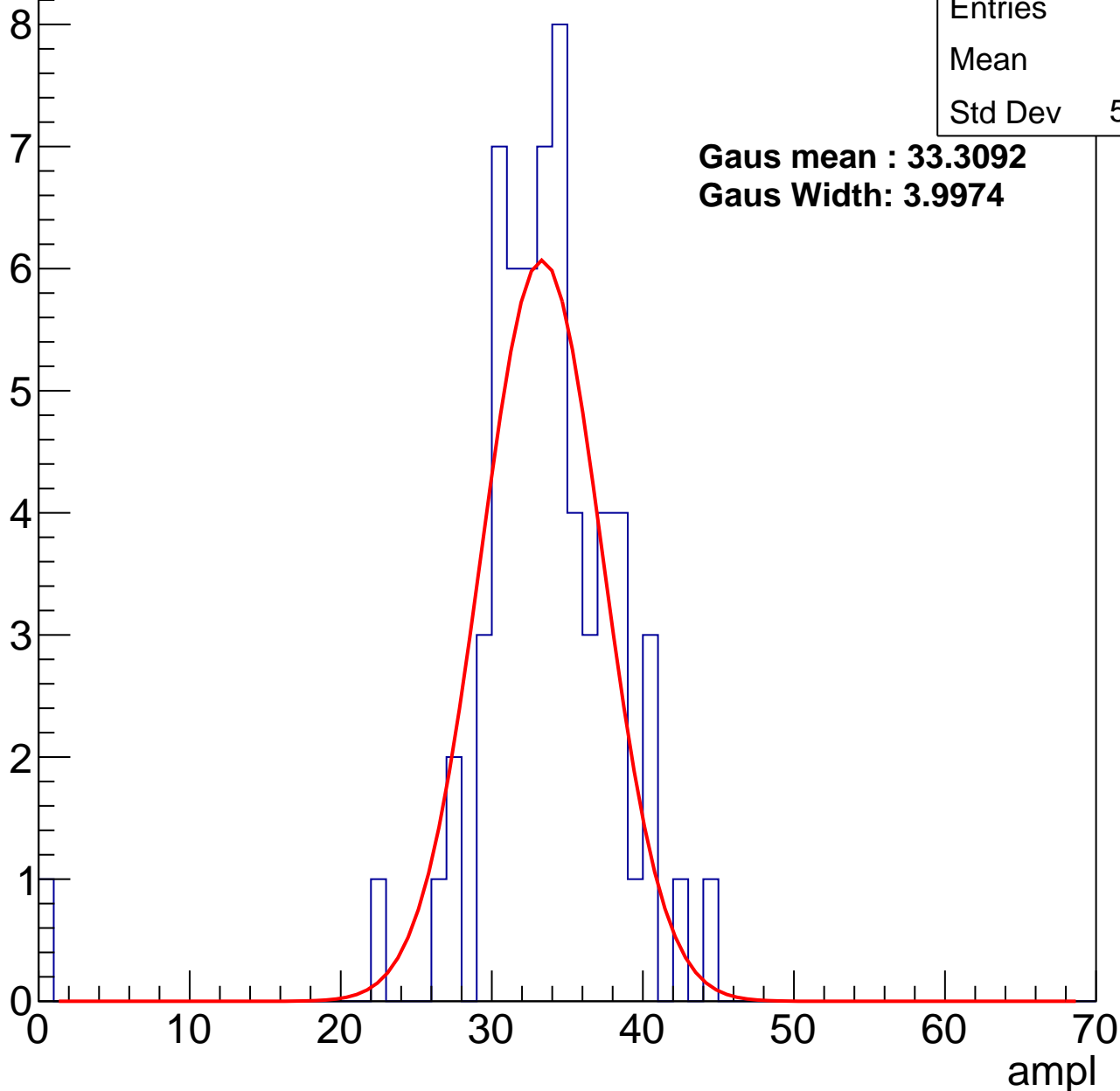
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	32.9
Std Dev	5.734

**Gaus mean : 33.3092**

**Gaus Width: 3.9974**



# B1L103S, U1-ch102, adc2

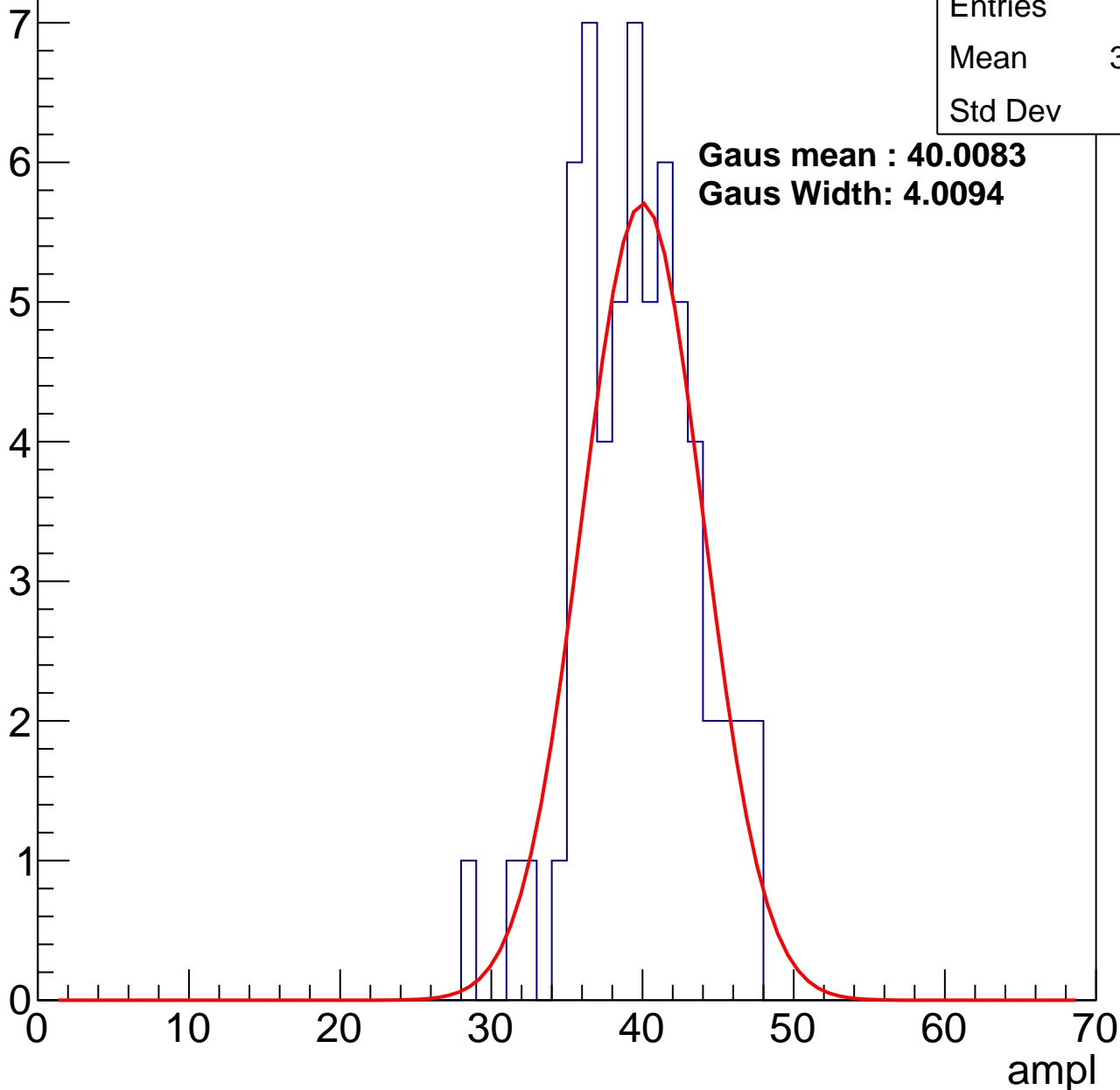
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	39.18
Std Dev	3.89

**Gaus mean : 40.0083**

**Gaus Width: 4.0094**

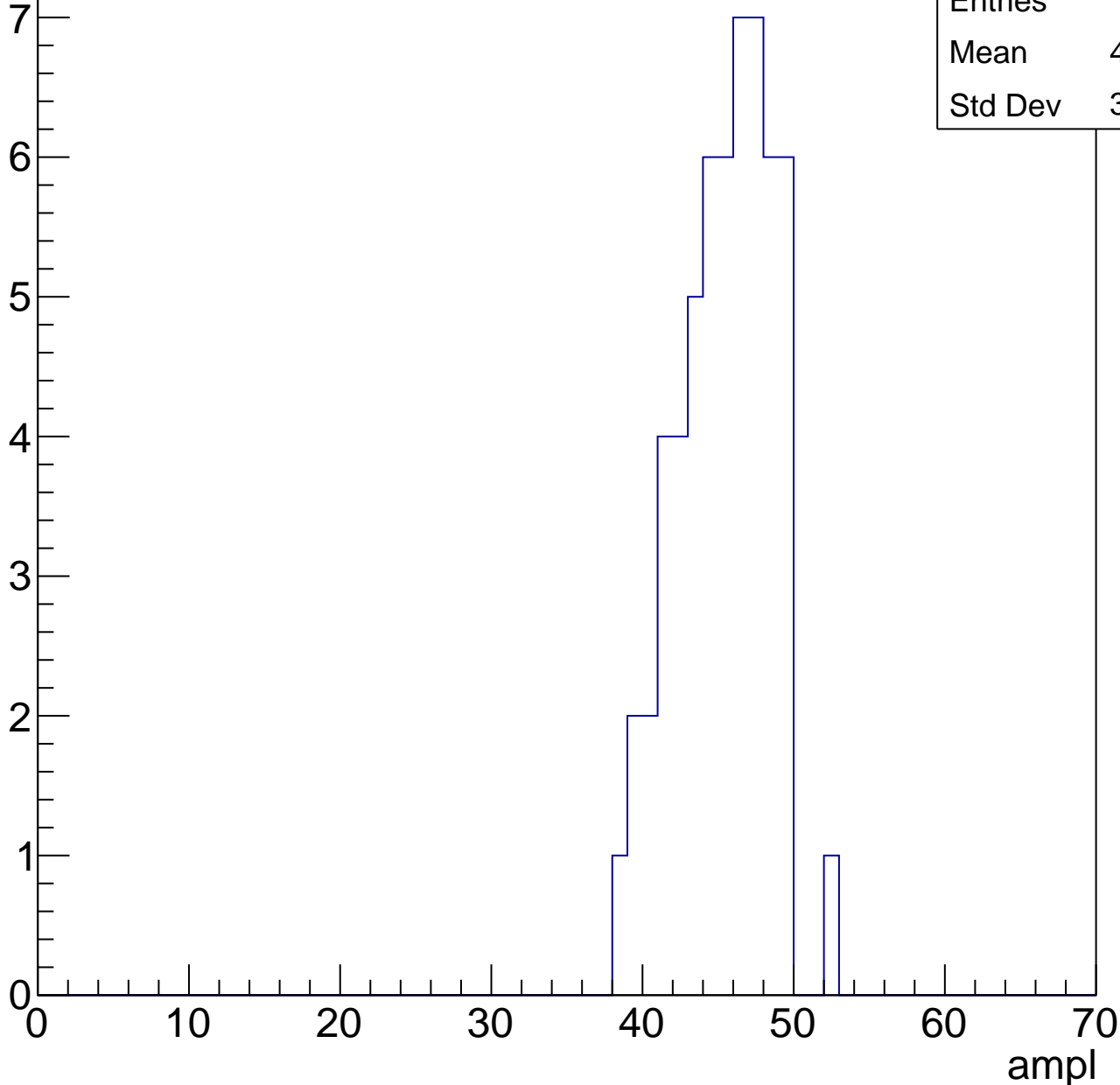


# B1L103S, U1-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	44.95
Std Dev	3.052

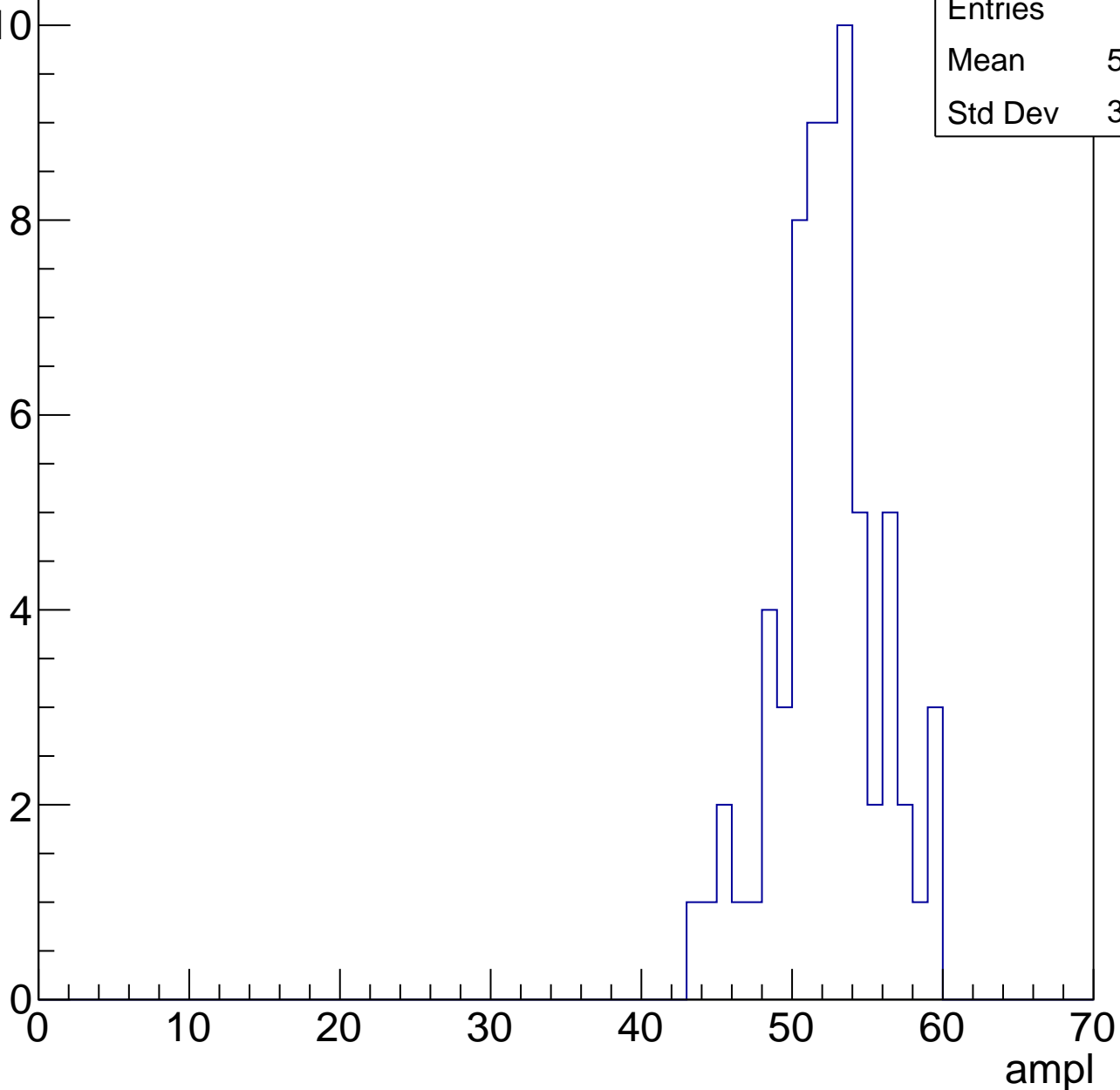


# B1L103S, U1-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	51.87
Std Dev	3.446

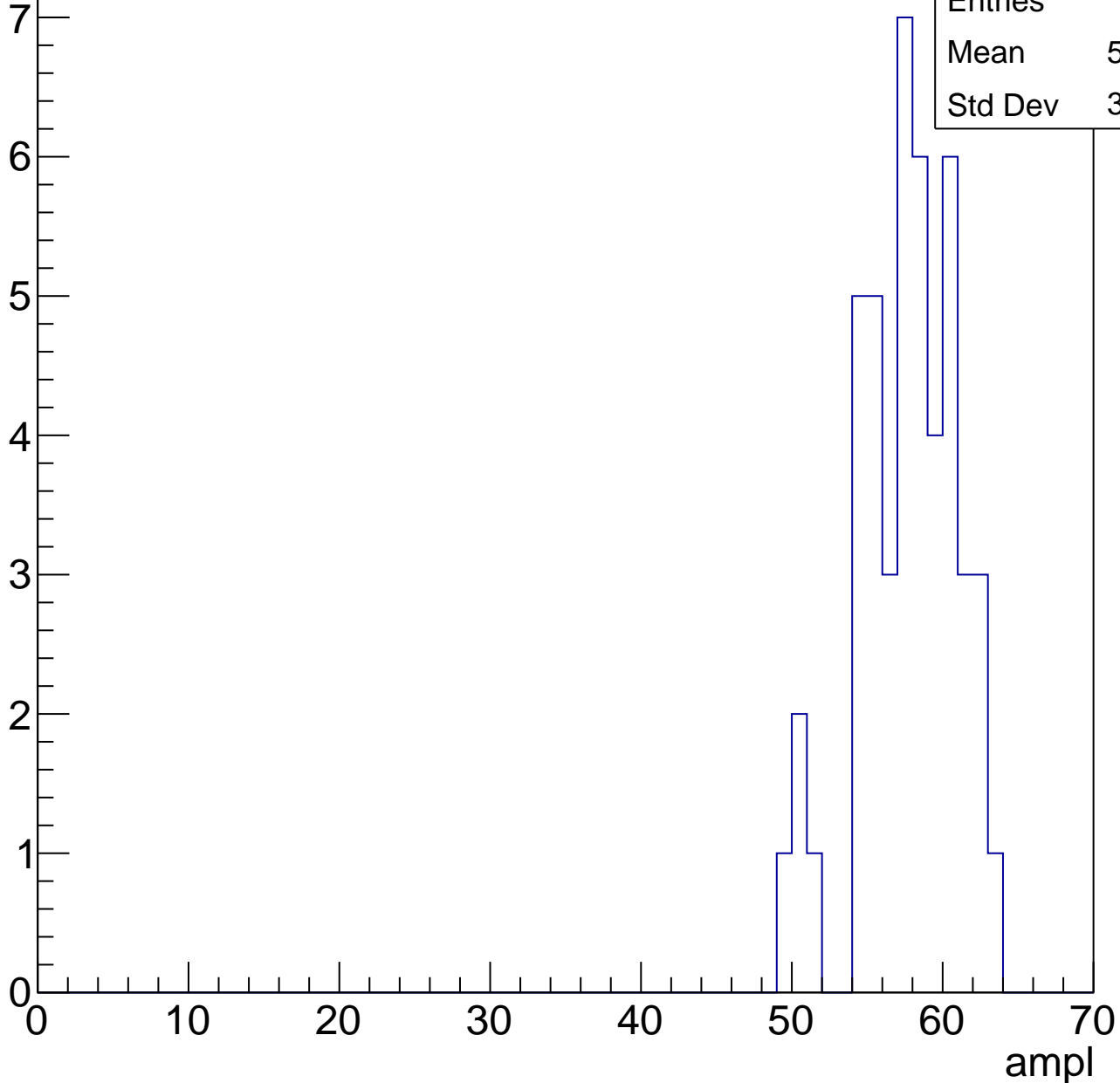


# B1L103S, U1-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

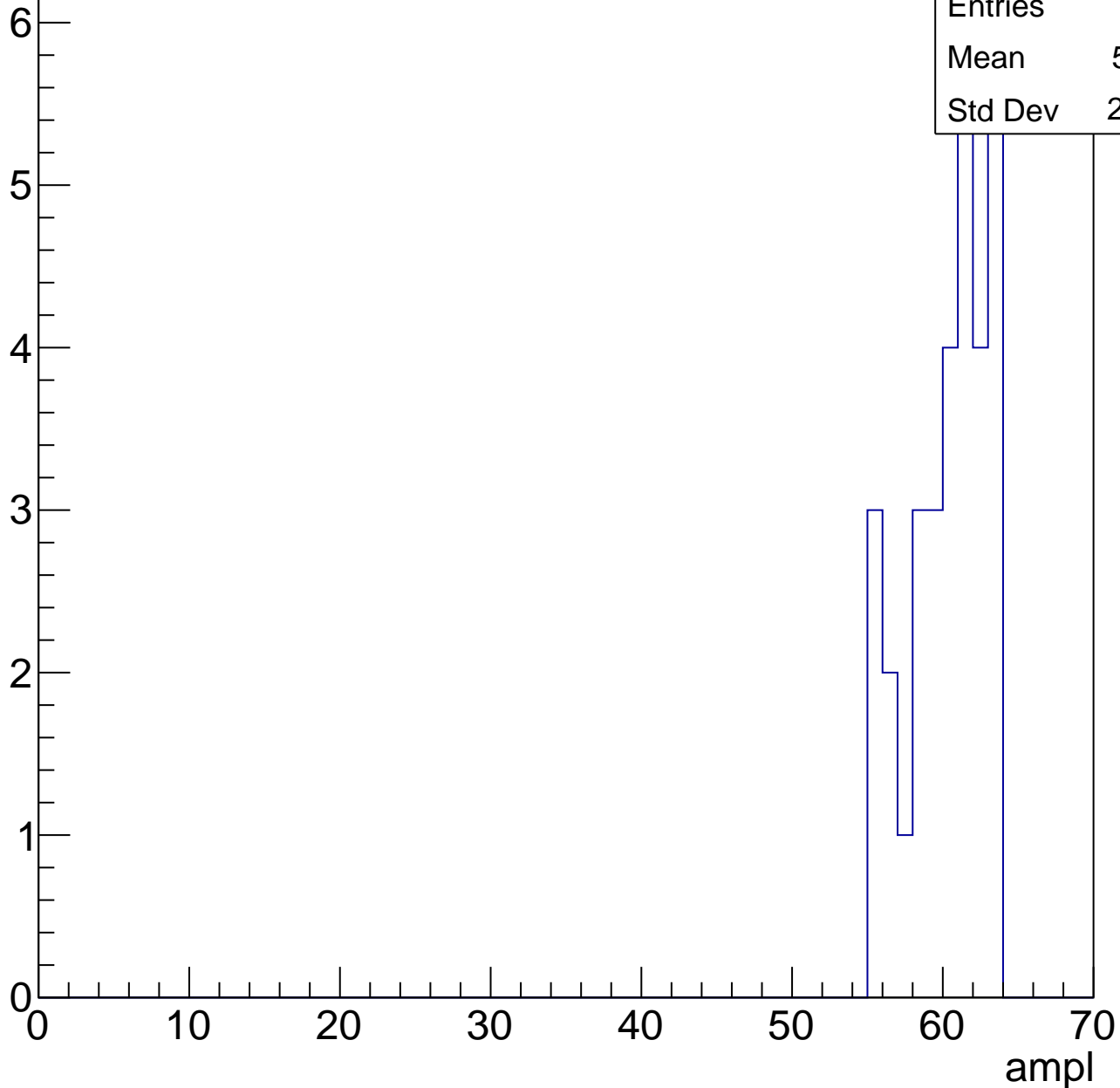
Entries	47
Mean	57.19
Std Dev	3.259



# B1L103S, U1-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

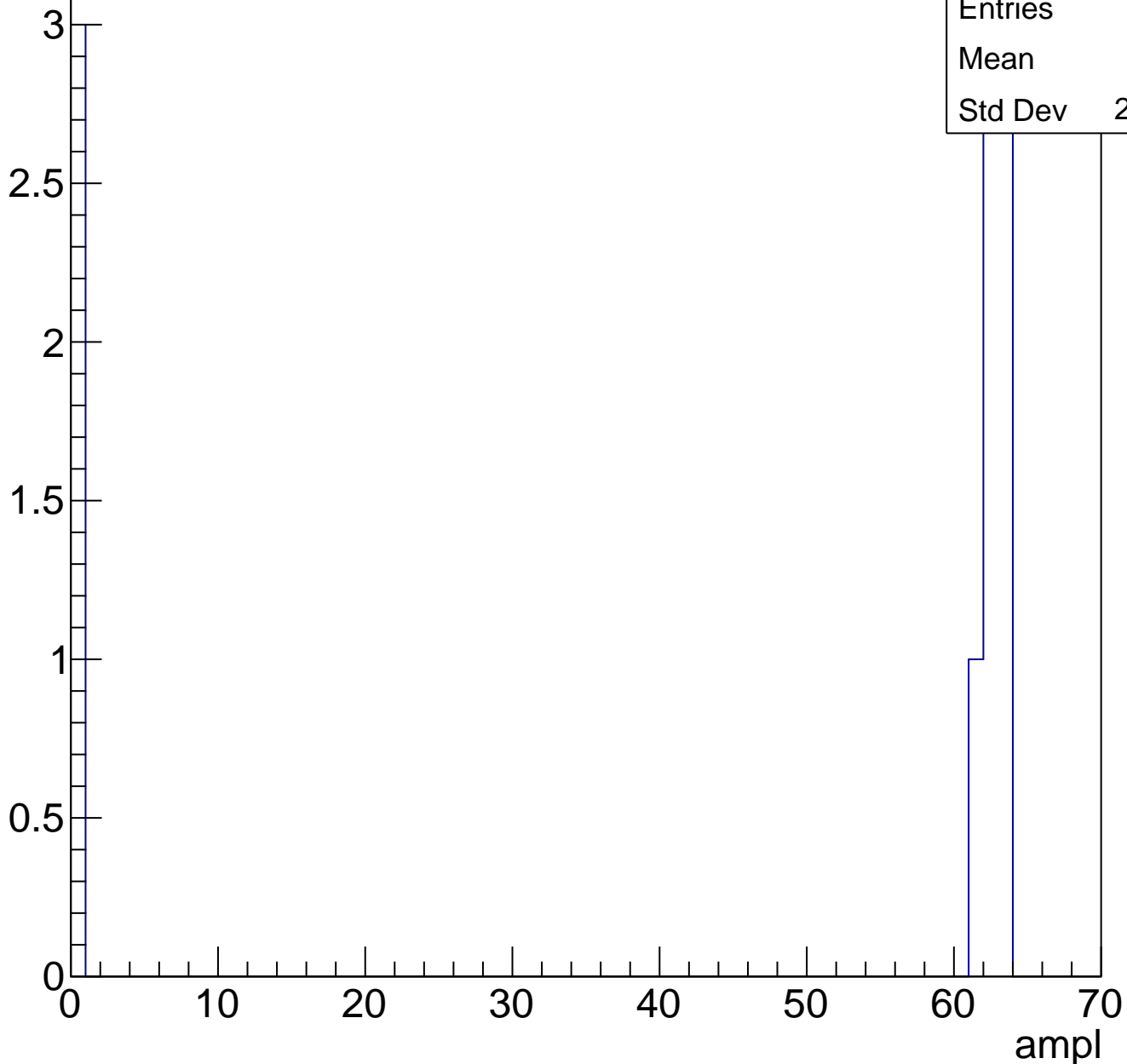




# B1L103S, U1-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch103, adc0

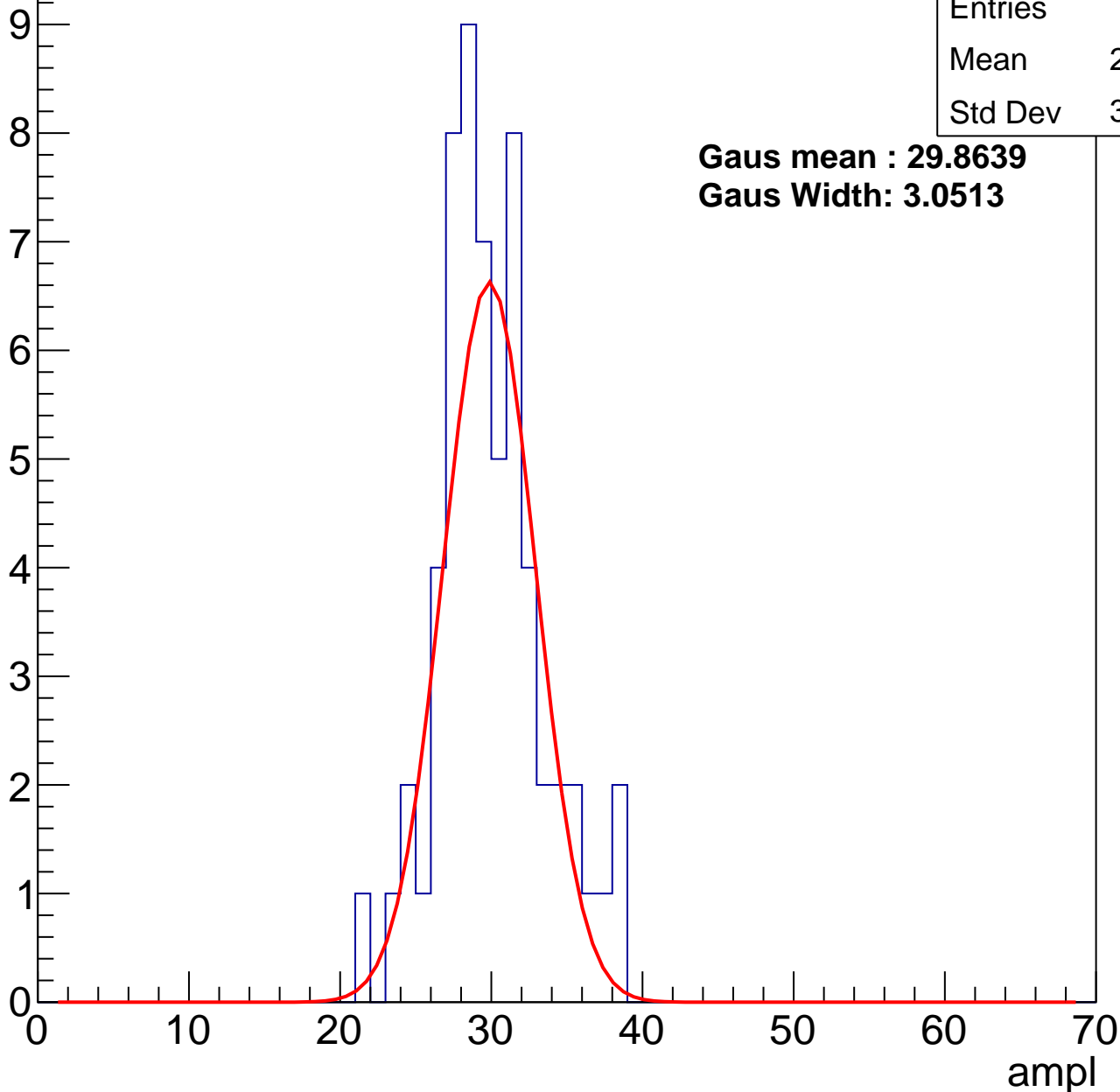
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	29.52
Std Dev	3.486

**Gaus mean : 29.8639**

**Gaus Width: 3.0513**



# B1L103S, U1-ch103, adc1

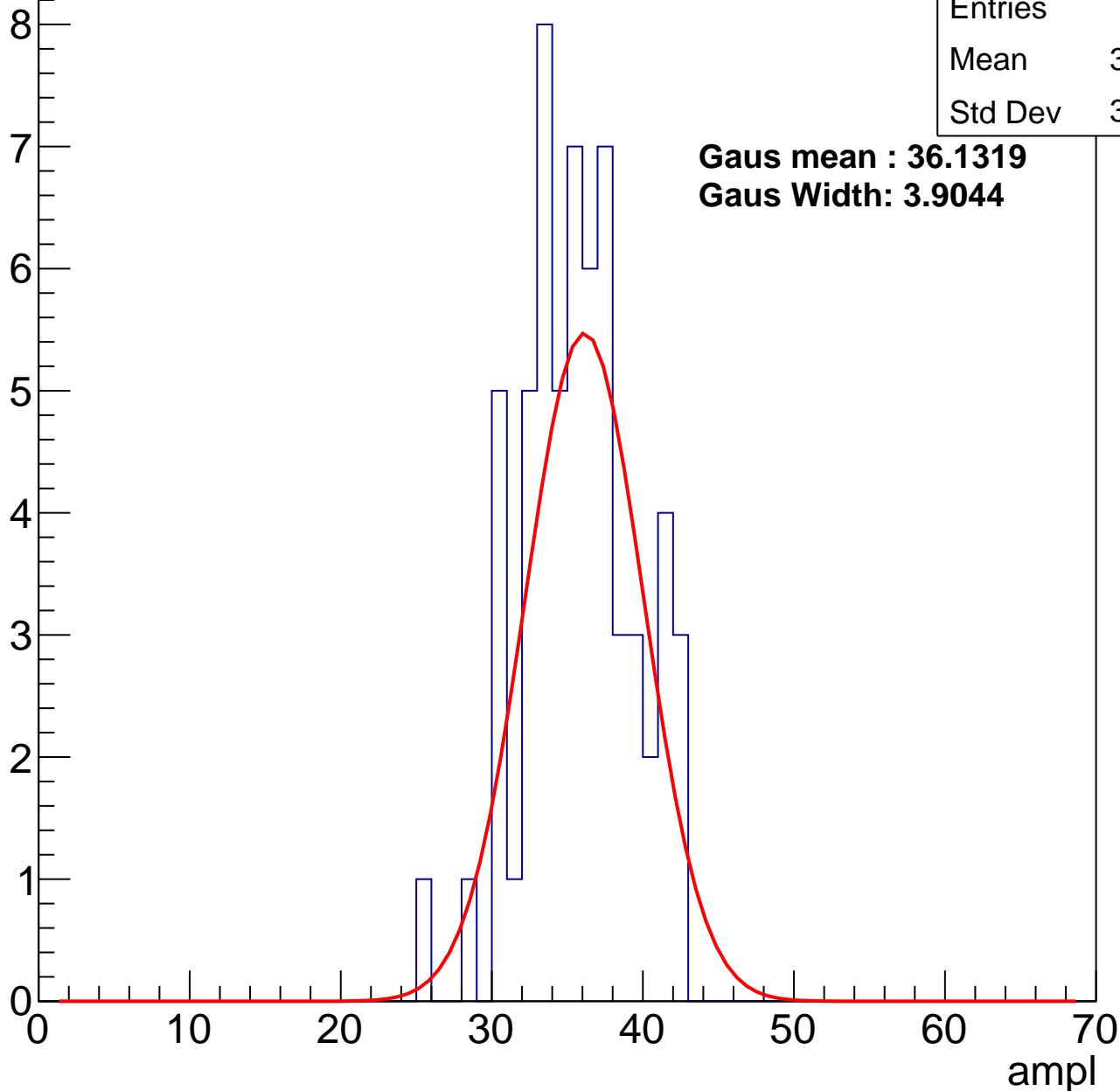
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	35.23
Std Dev	3.664

**Gaus mean : 36.1319**

**Gaus Width: 3.9044**



# B1L103S, U1-ch103, adc2

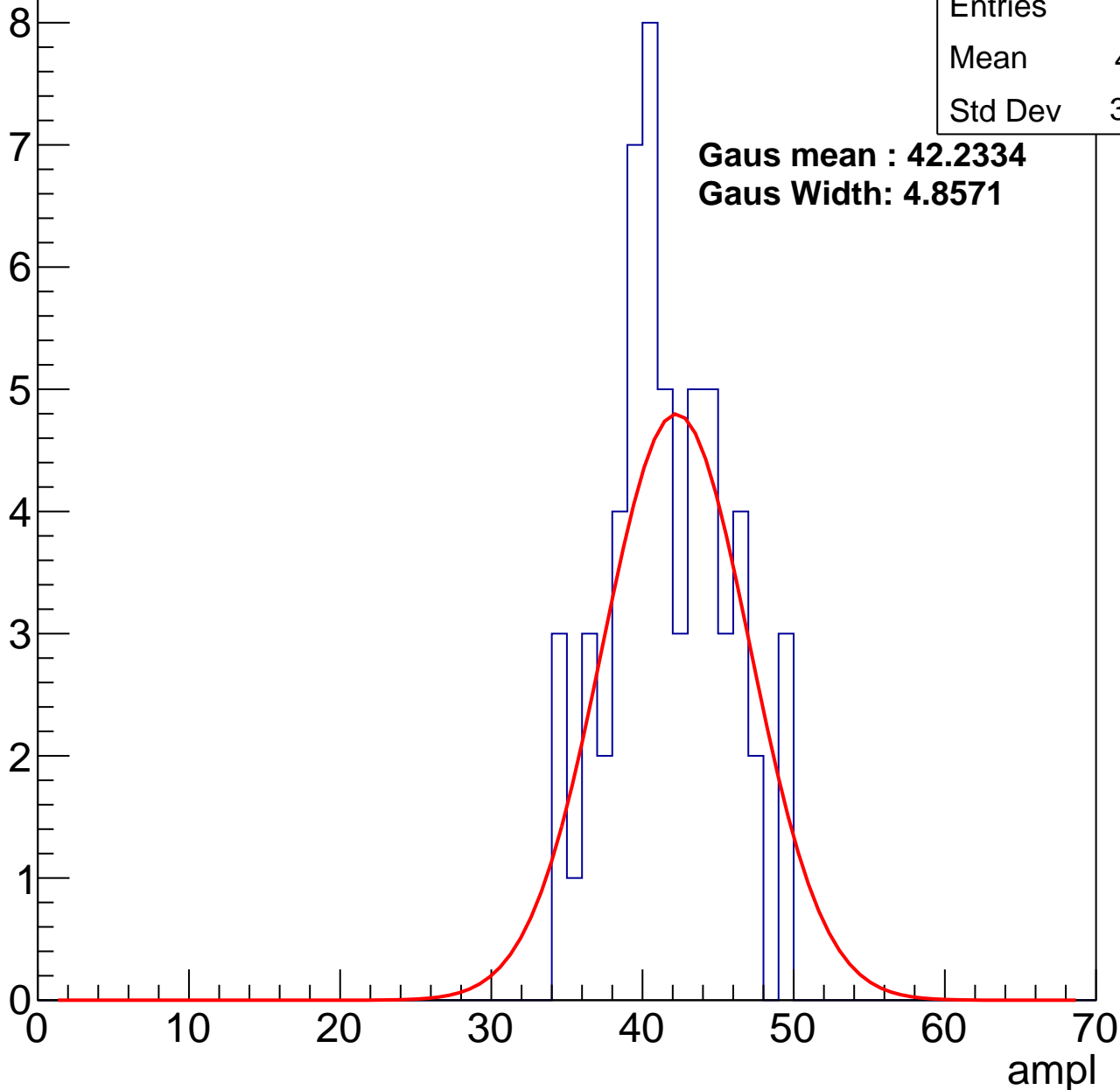
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	41.21
Std Dev	3.805

**Gaus mean : 42.2334**

**Gaus Width: 4.8571**

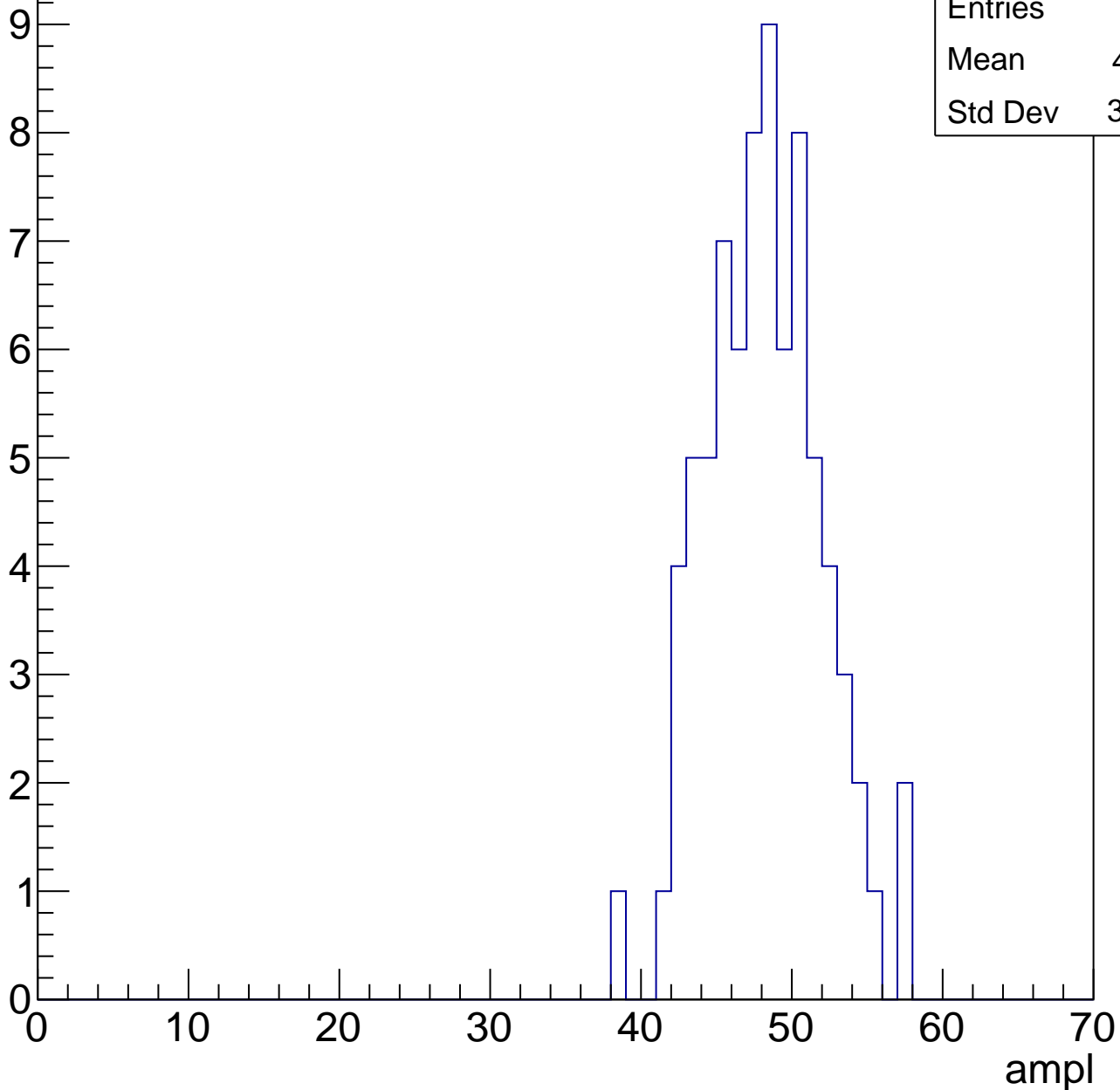


# B1L103S, U1-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	47.71
Std Dev	3.765

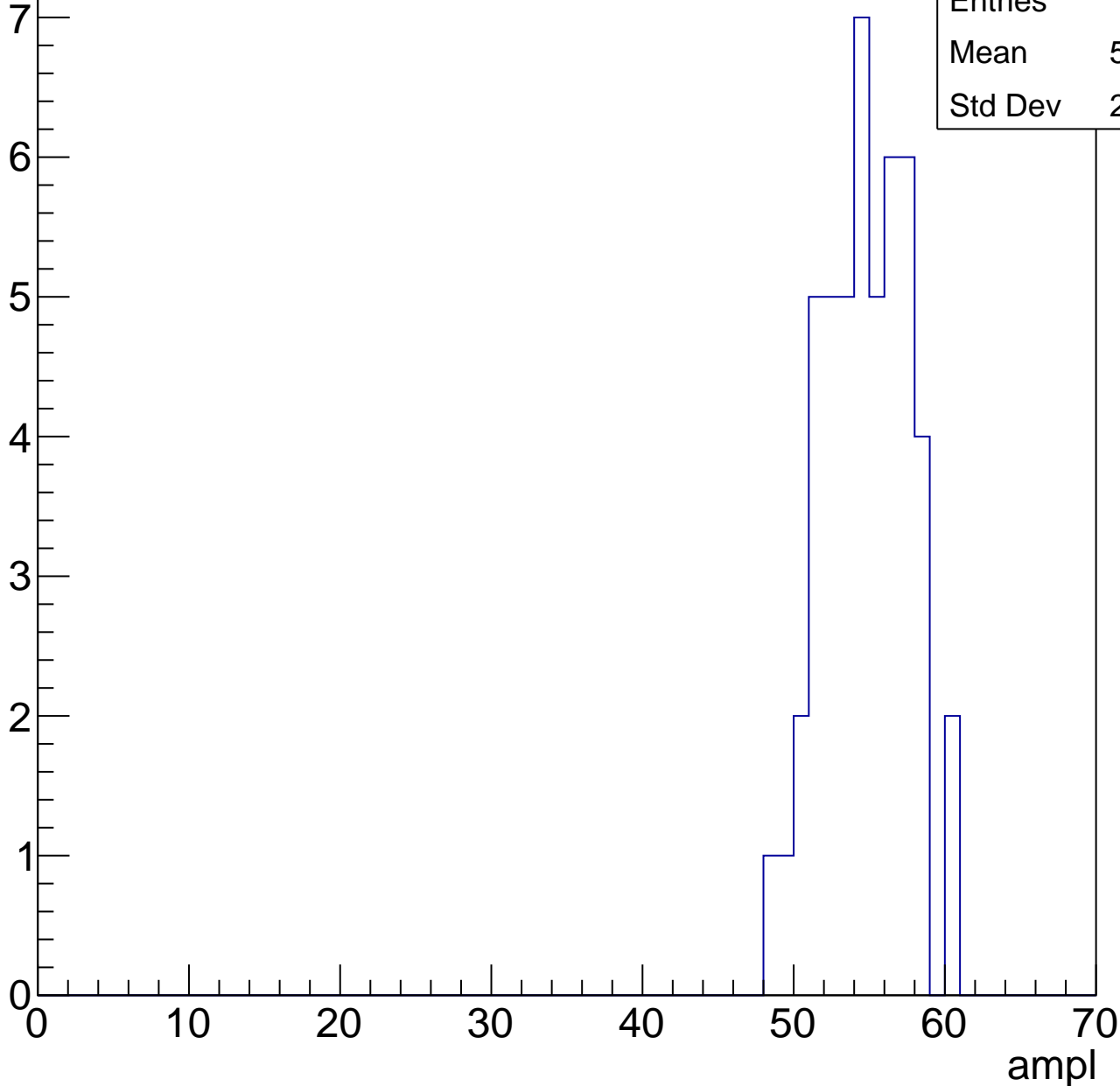


# B1L103S, U1-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	54.29
Std Dev	2.777

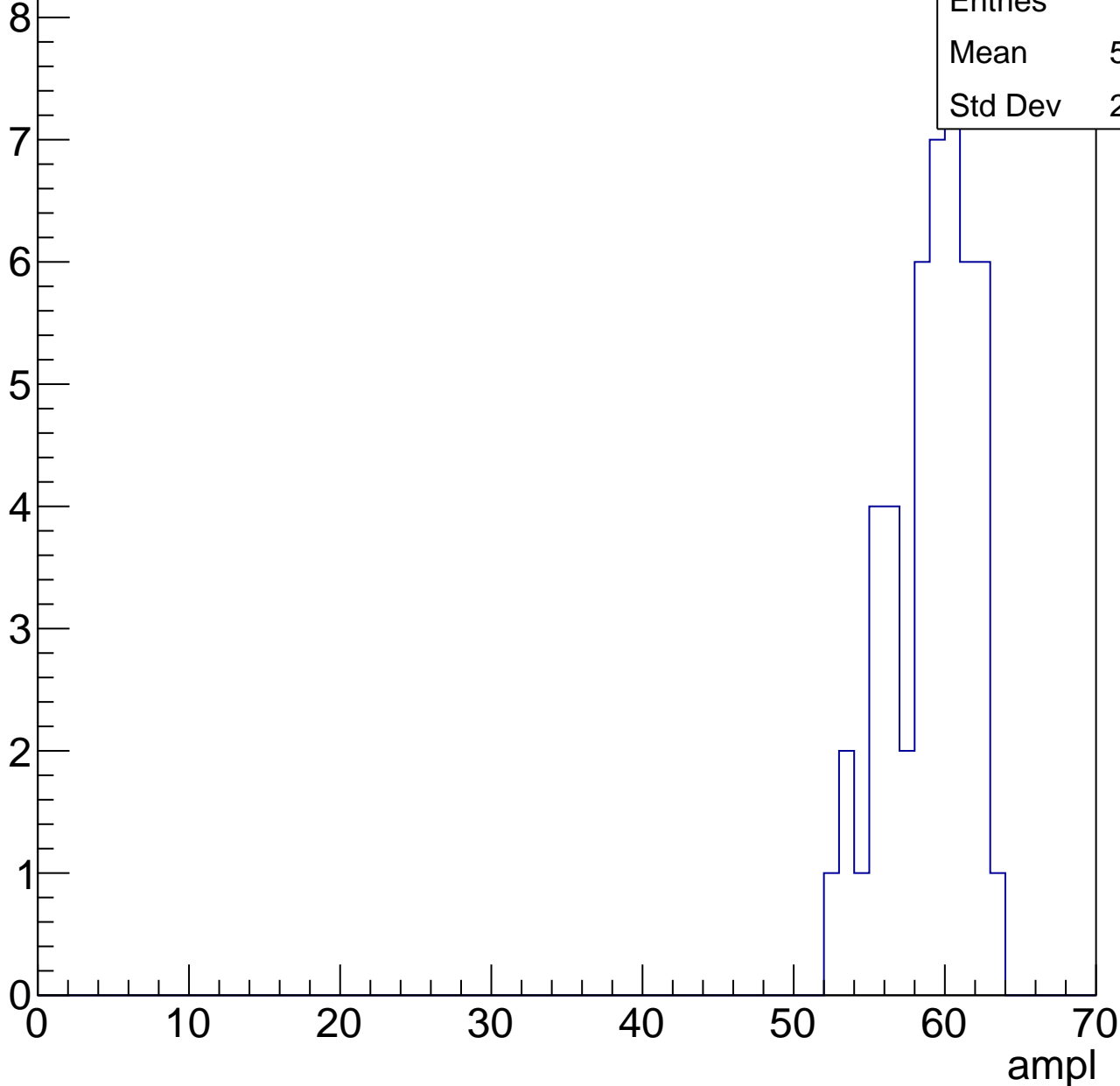


# B1L103S, U1-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	58.58
Std Dev	2.714

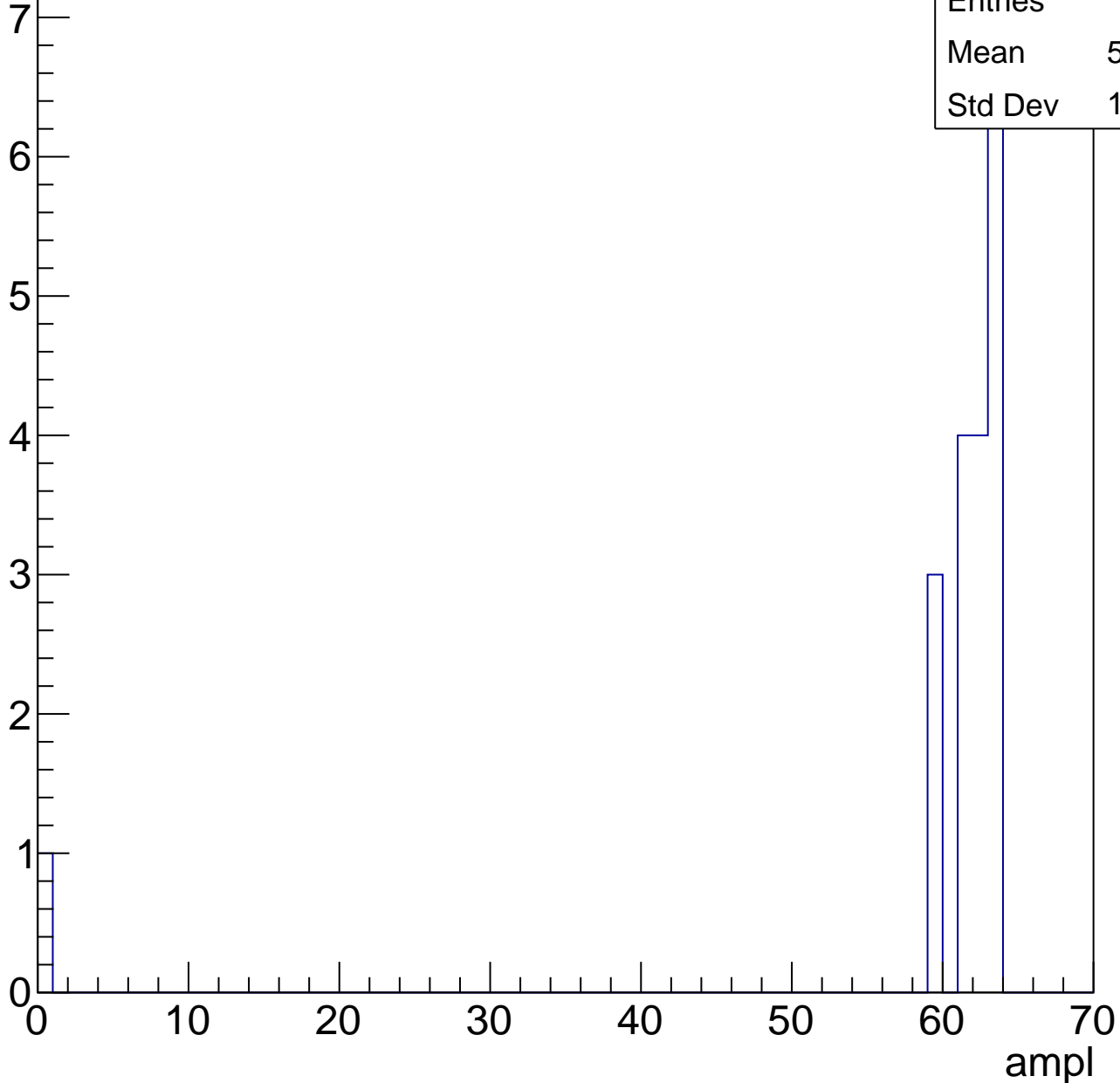


# B1L103S, U1-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	19
Mean	58.42
Std Dev	13.84





# B1L103S, U1-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch104, adc0

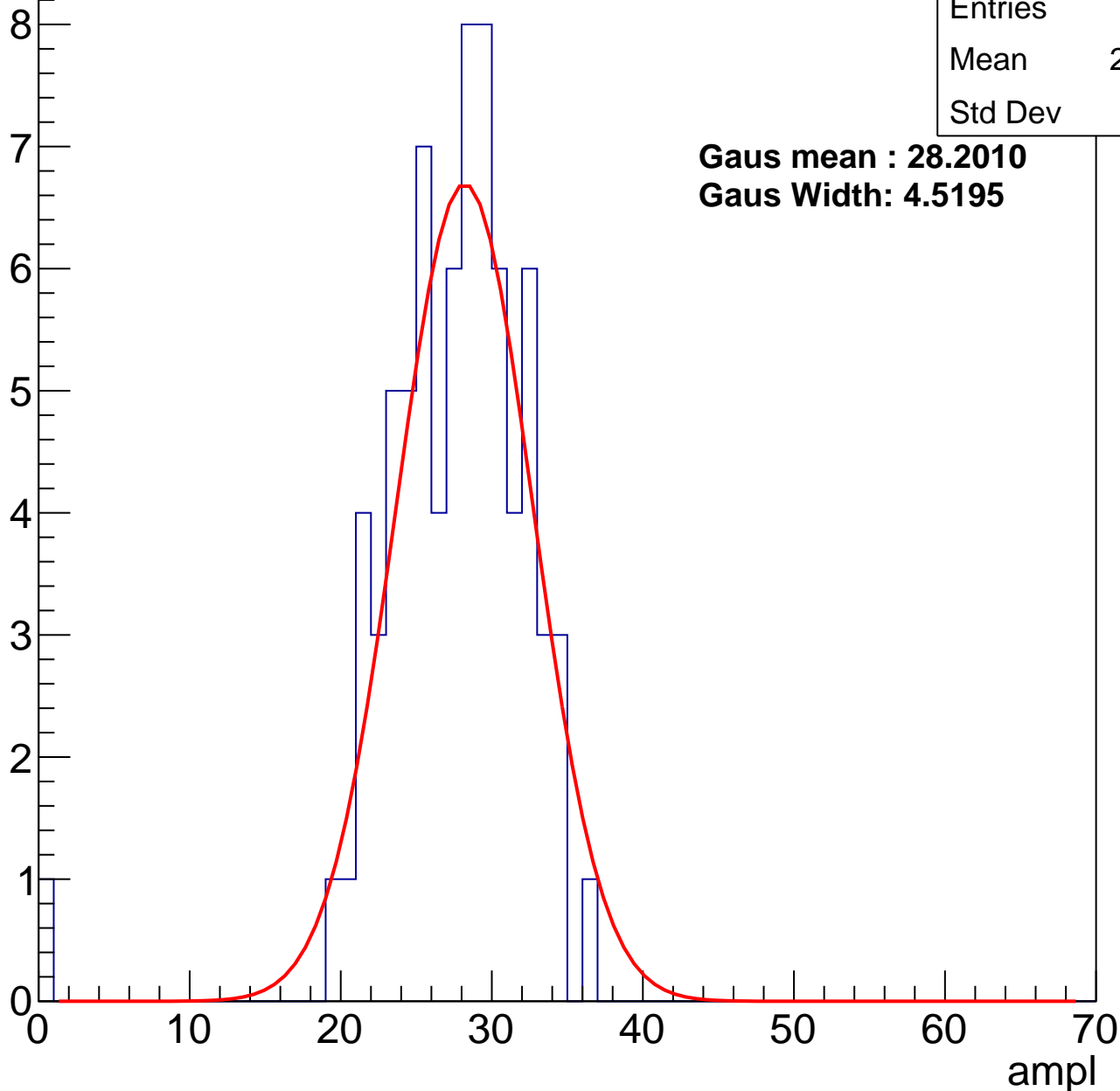
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	27.03
Std Dev	4.95

**Gaus mean : 28.2010**

**Gaus Width: 4.5195**



# B1L103S, U1-ch104, adc1

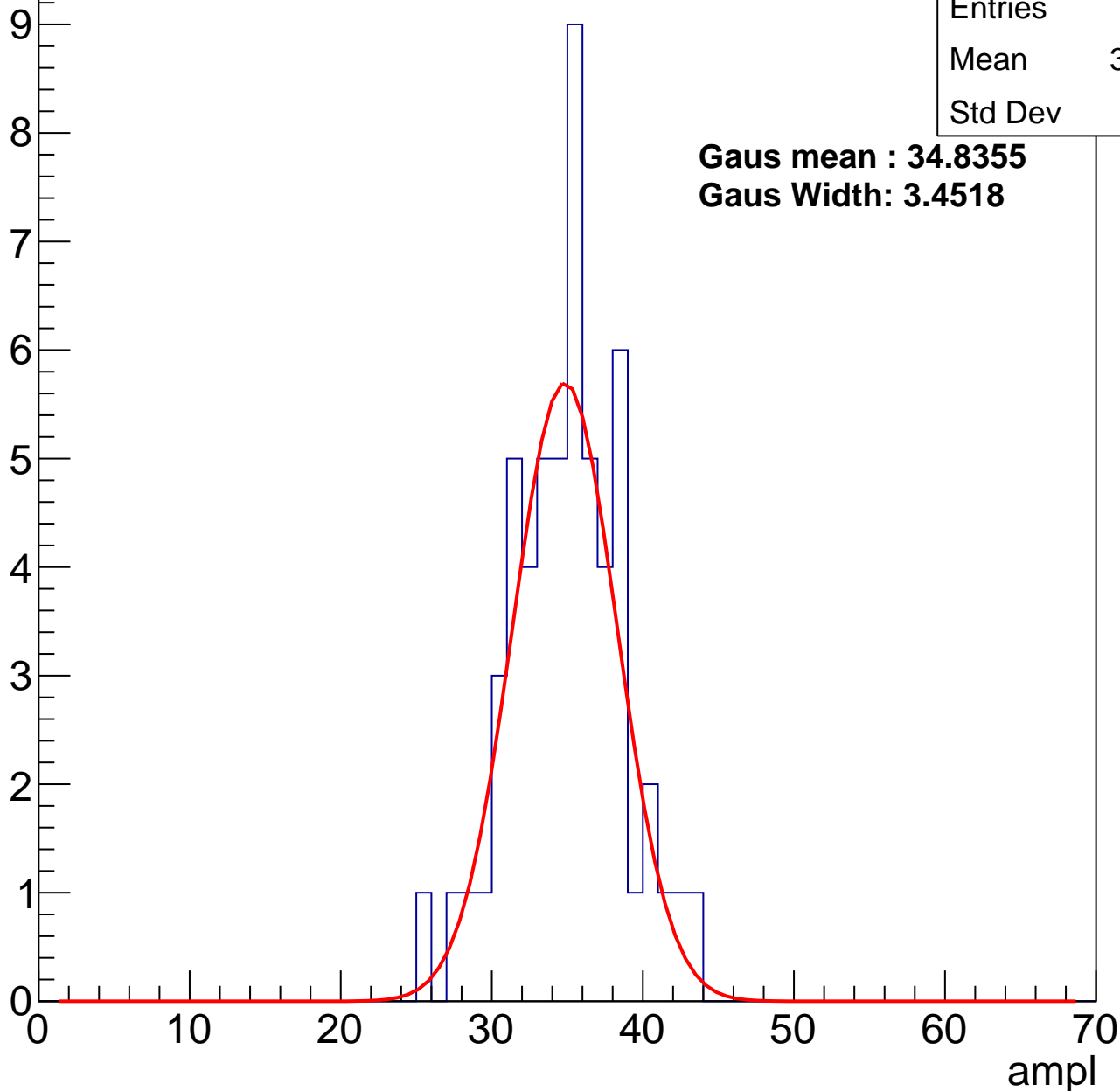
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	34.52
Std Dev	3.64

**Gaus mean : 34.8355**

**Gaus Width: 3.4518**



# B1L103S, U1-ch104, adc2

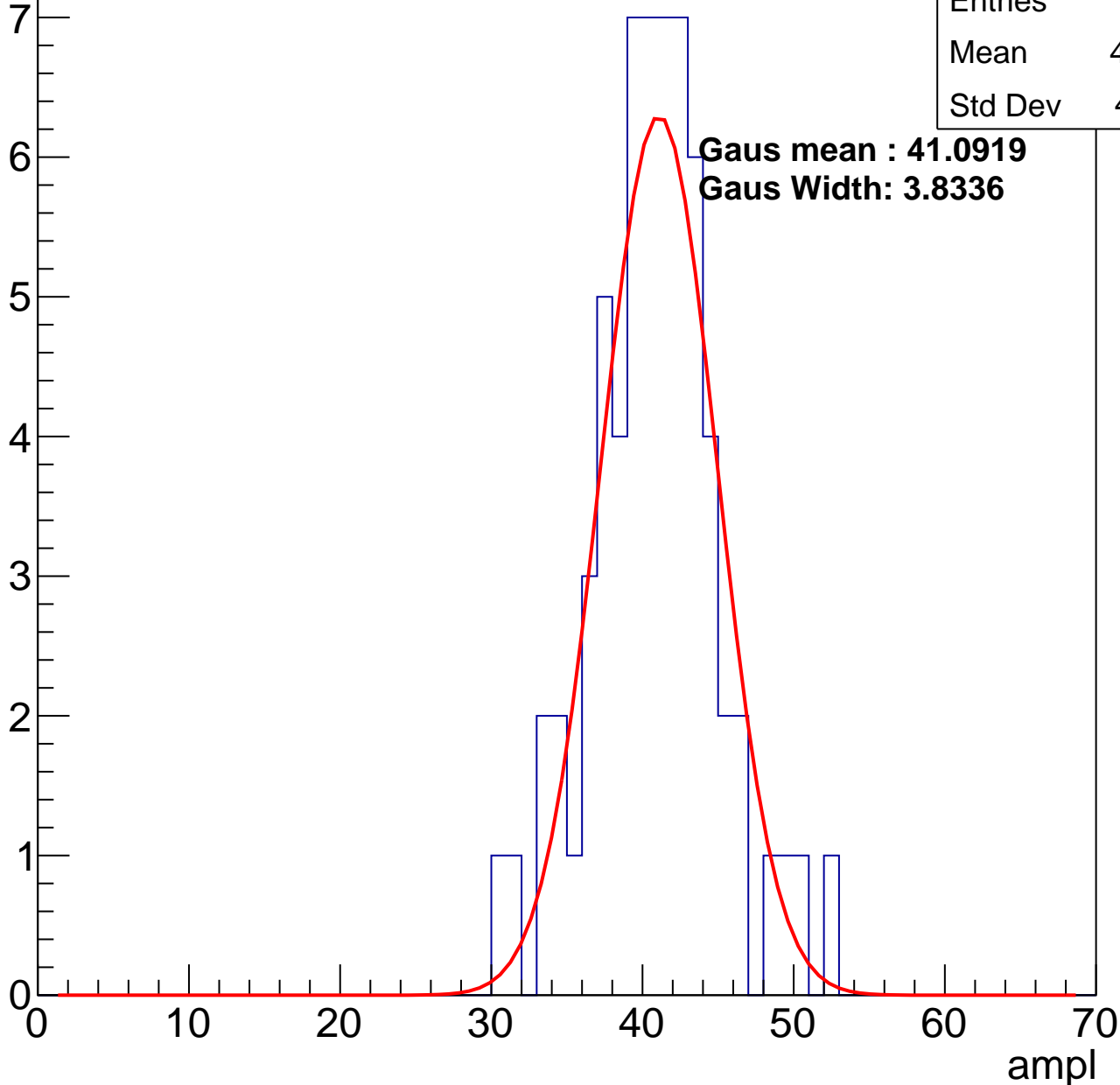
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	40.37
Std Dev	4.201

**Gaus mean : 41.0919**

**Gaus Width: 3.8336**

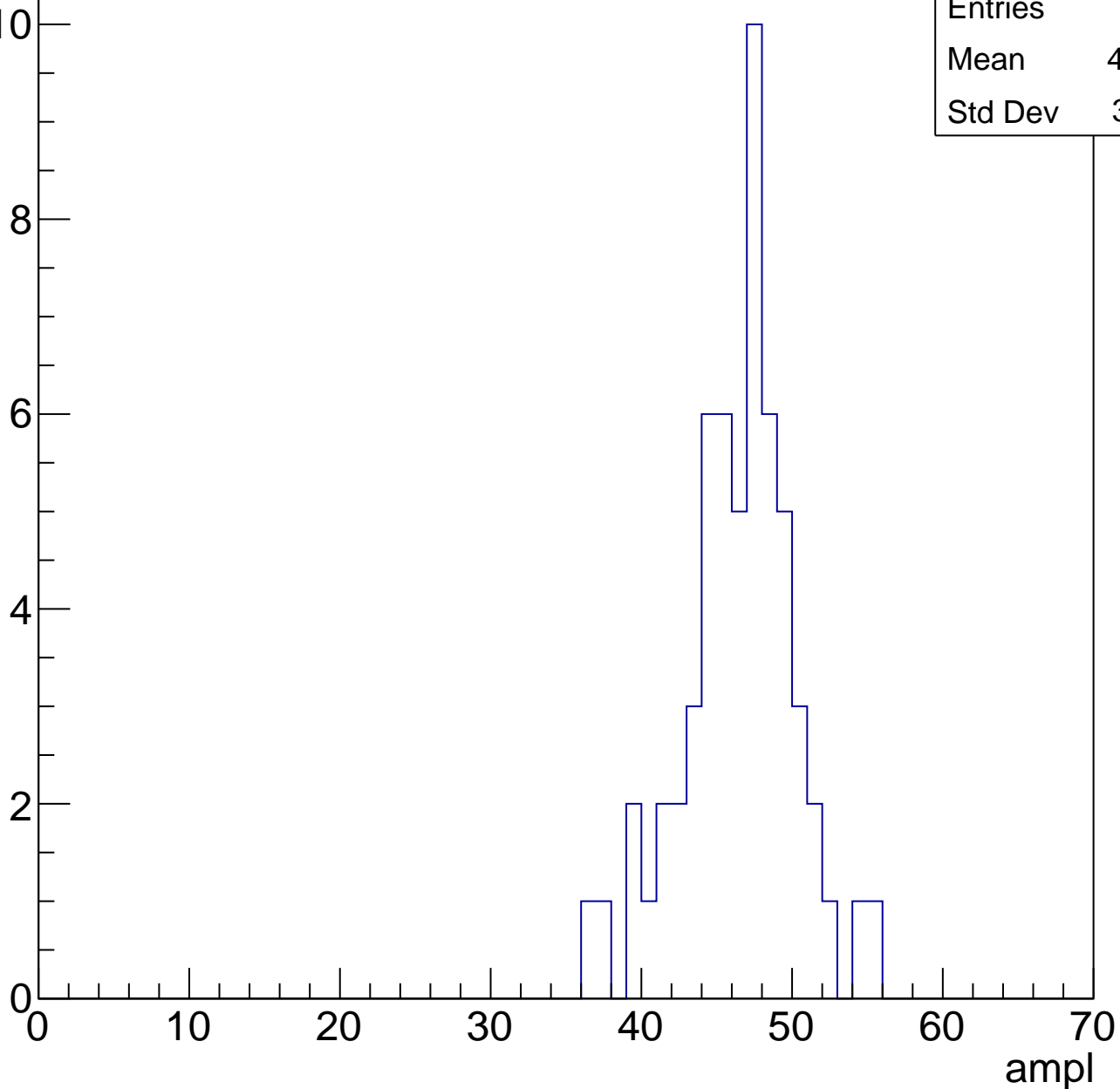


# B1L103S, U1-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	45.97
Std Dev	3.741

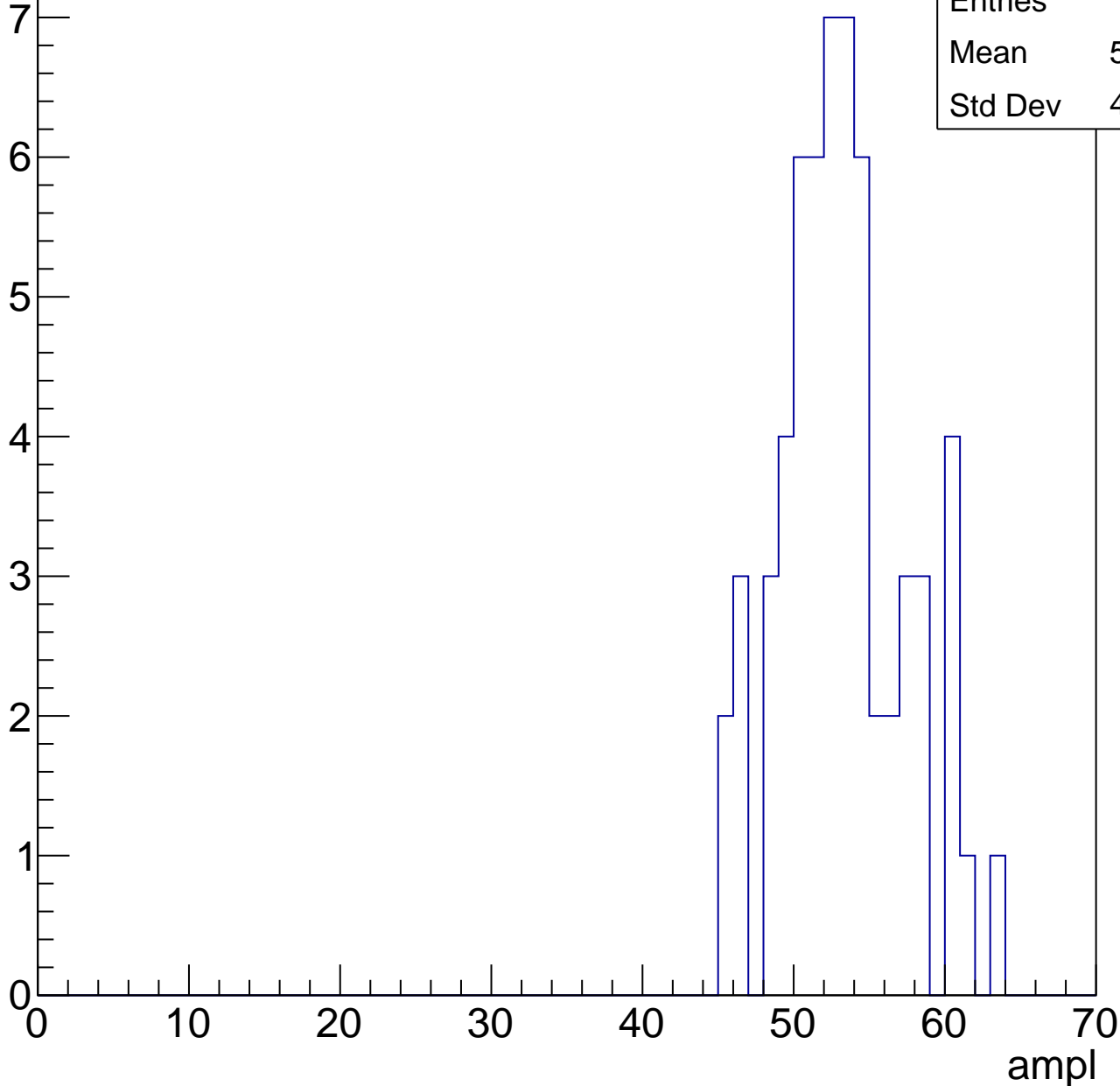


# B1L103S, U1-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

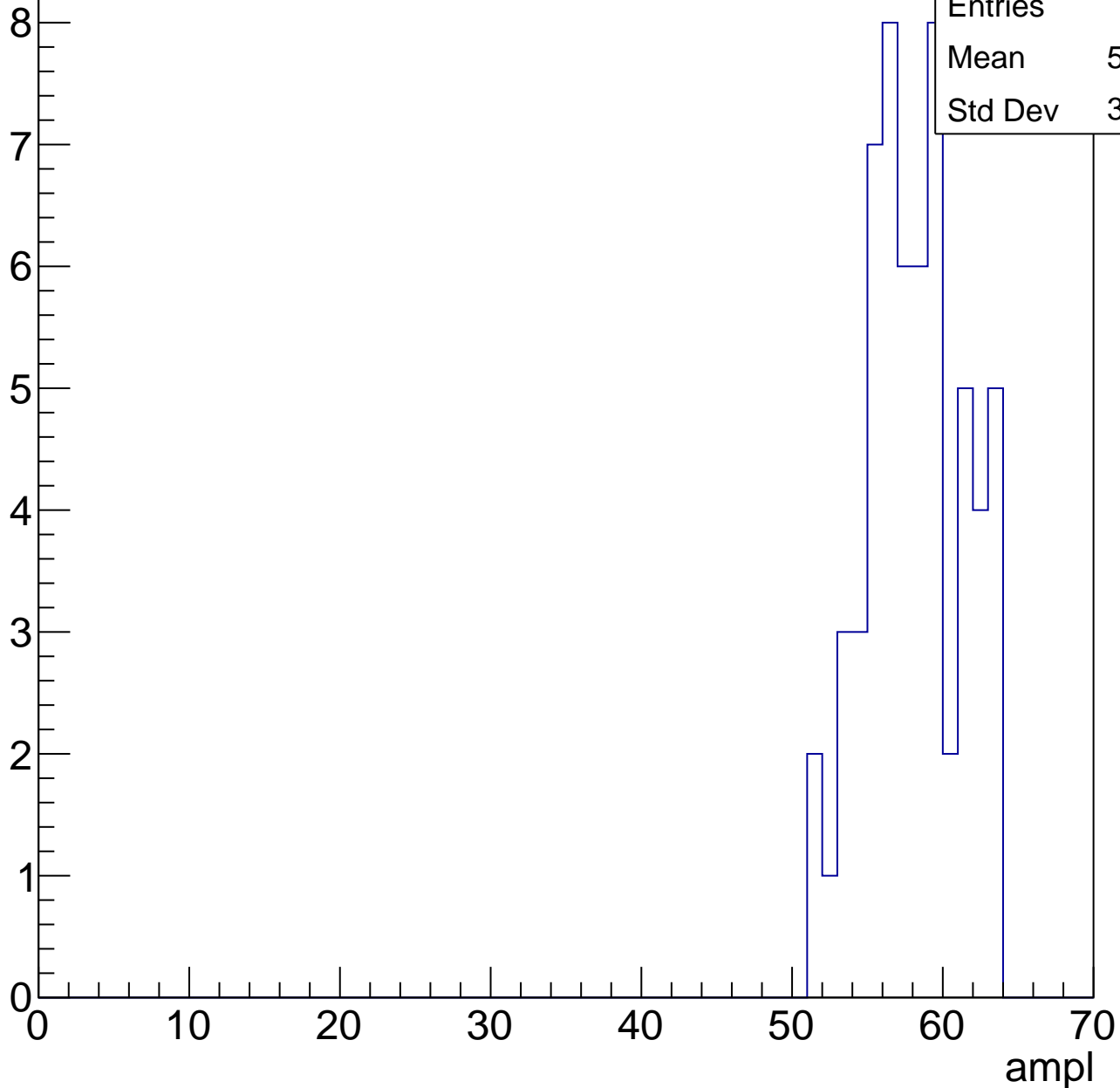
Entries	60
Mean	52.73
Std Dev	4.102



# B1L103S, U1-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

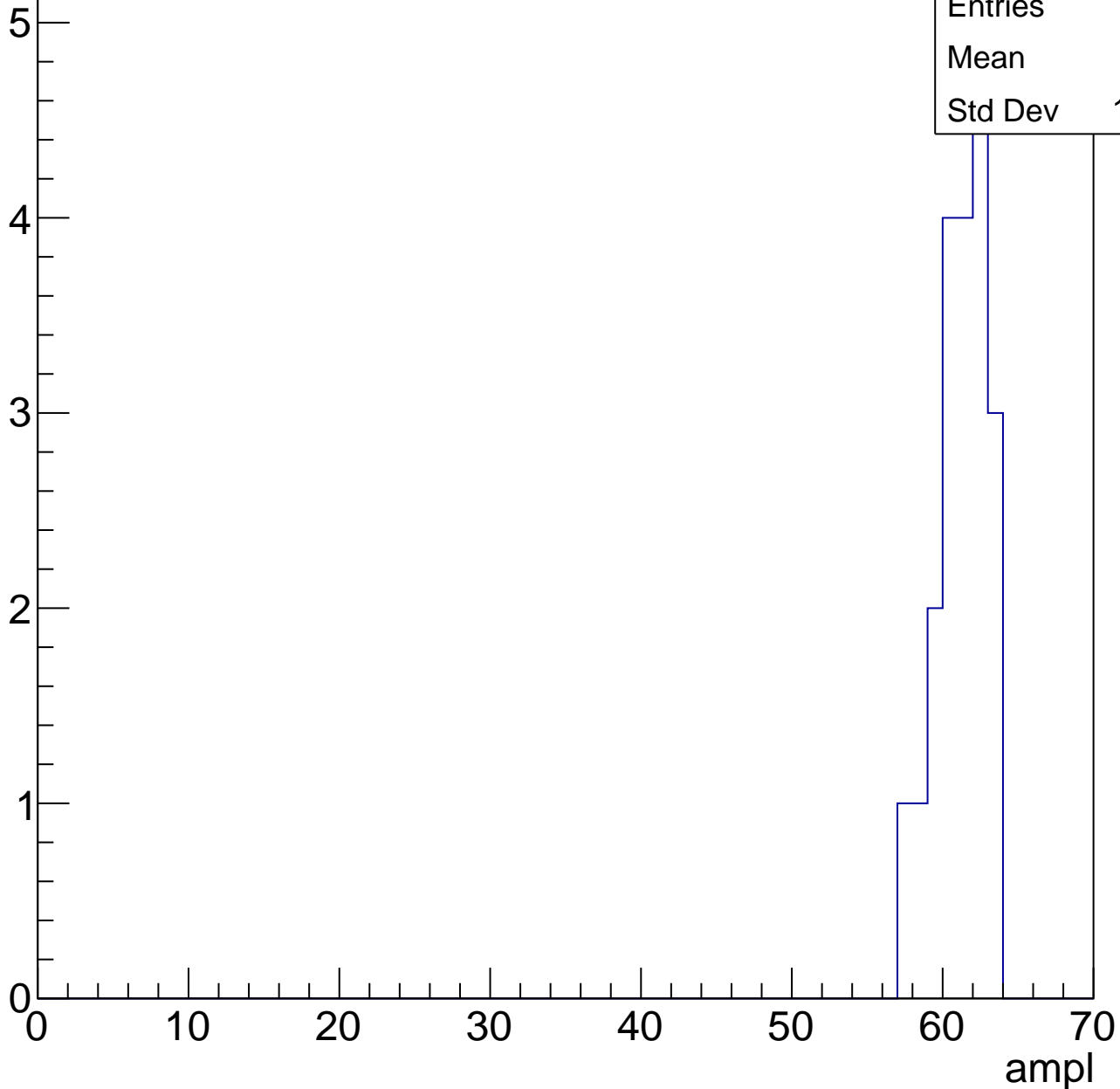


# B1L103S, U1-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	20
Mean	60.8
Std Dev	1.631

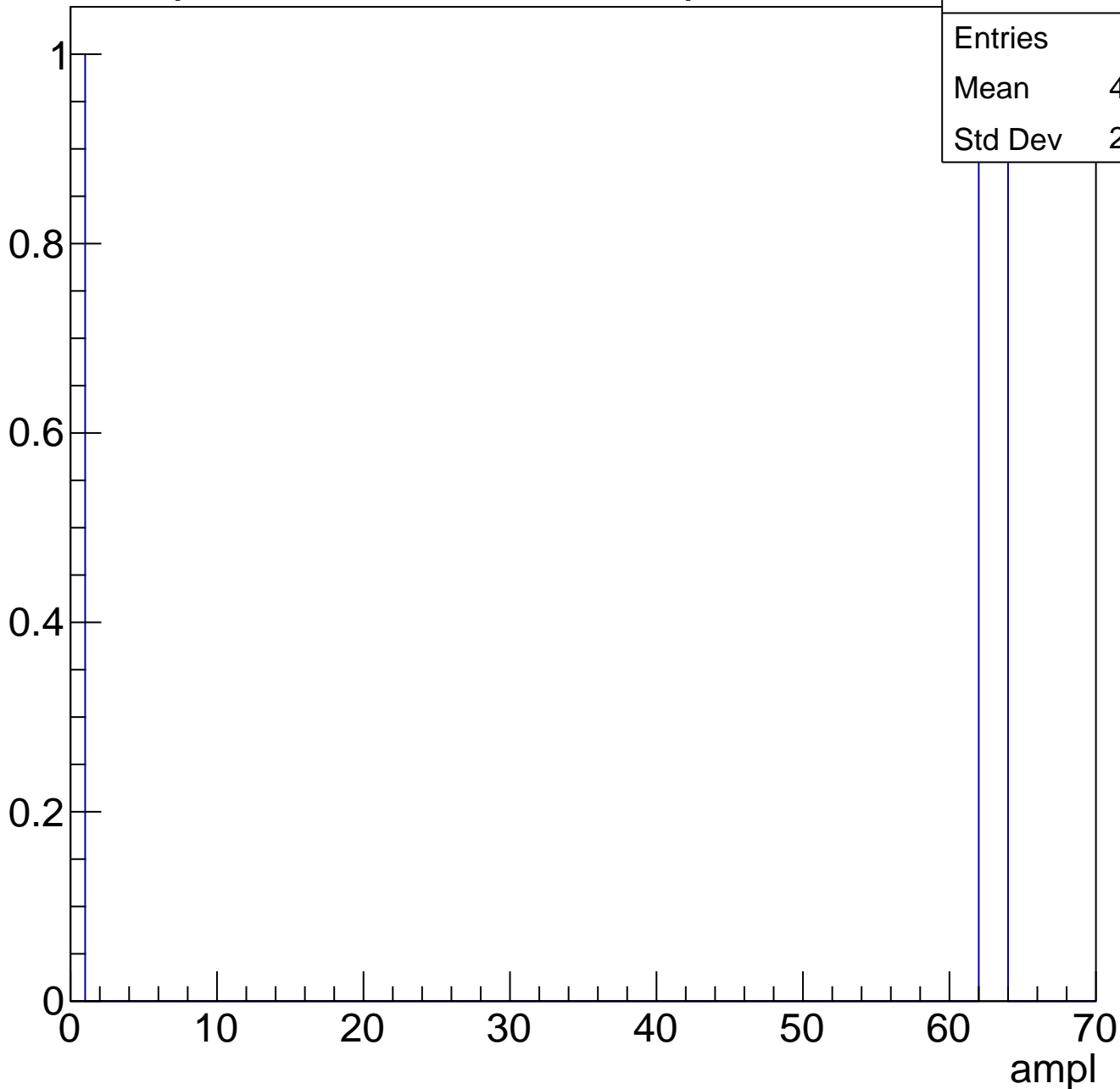




# B1L103S, U1-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch105, adc0

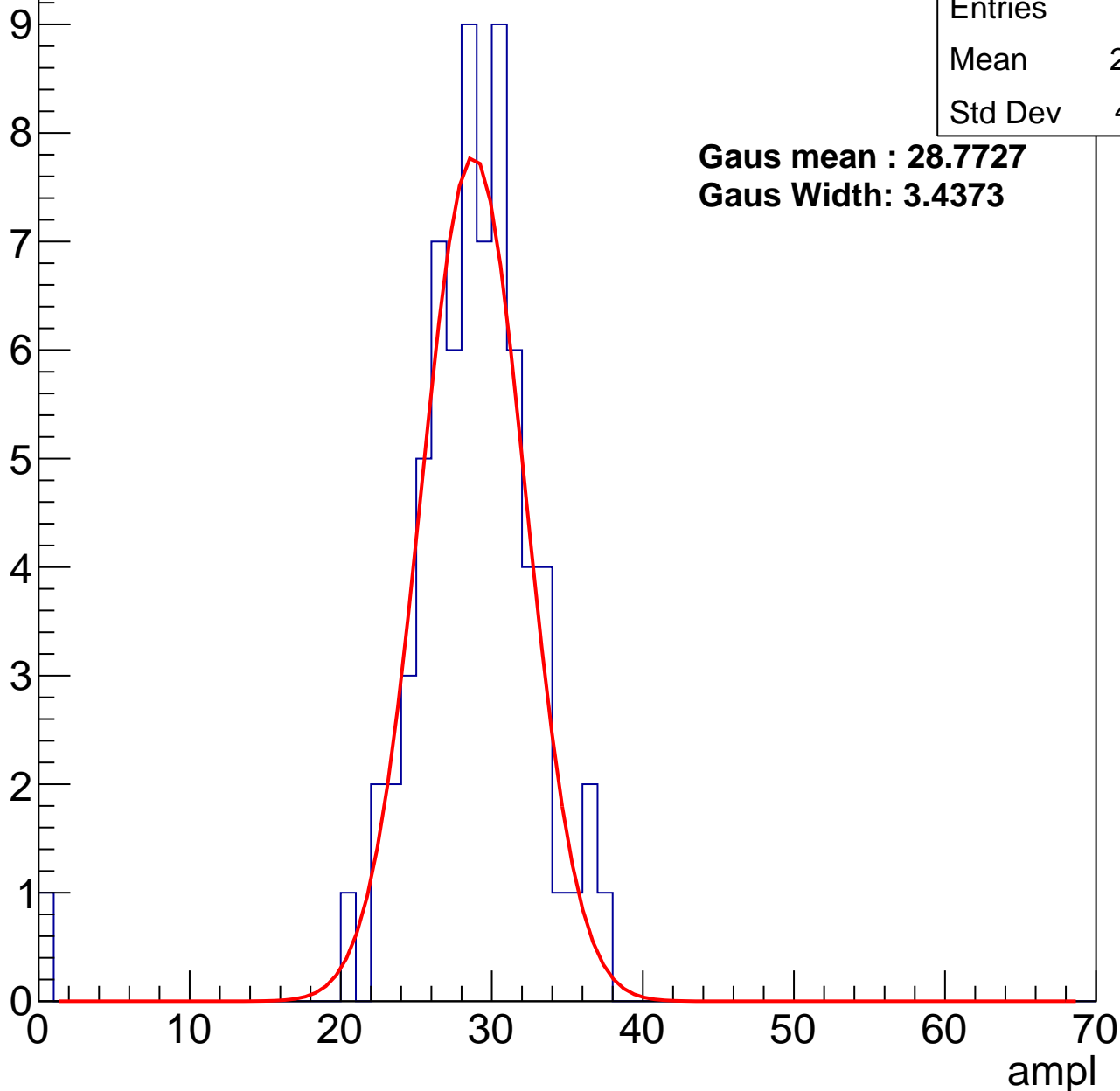
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	28.17
Std Dev	4.821

**Gaus mean : 28.7727**

**Gaus Width: 3.4373**



# B1L103S, U1-ch105, adc1

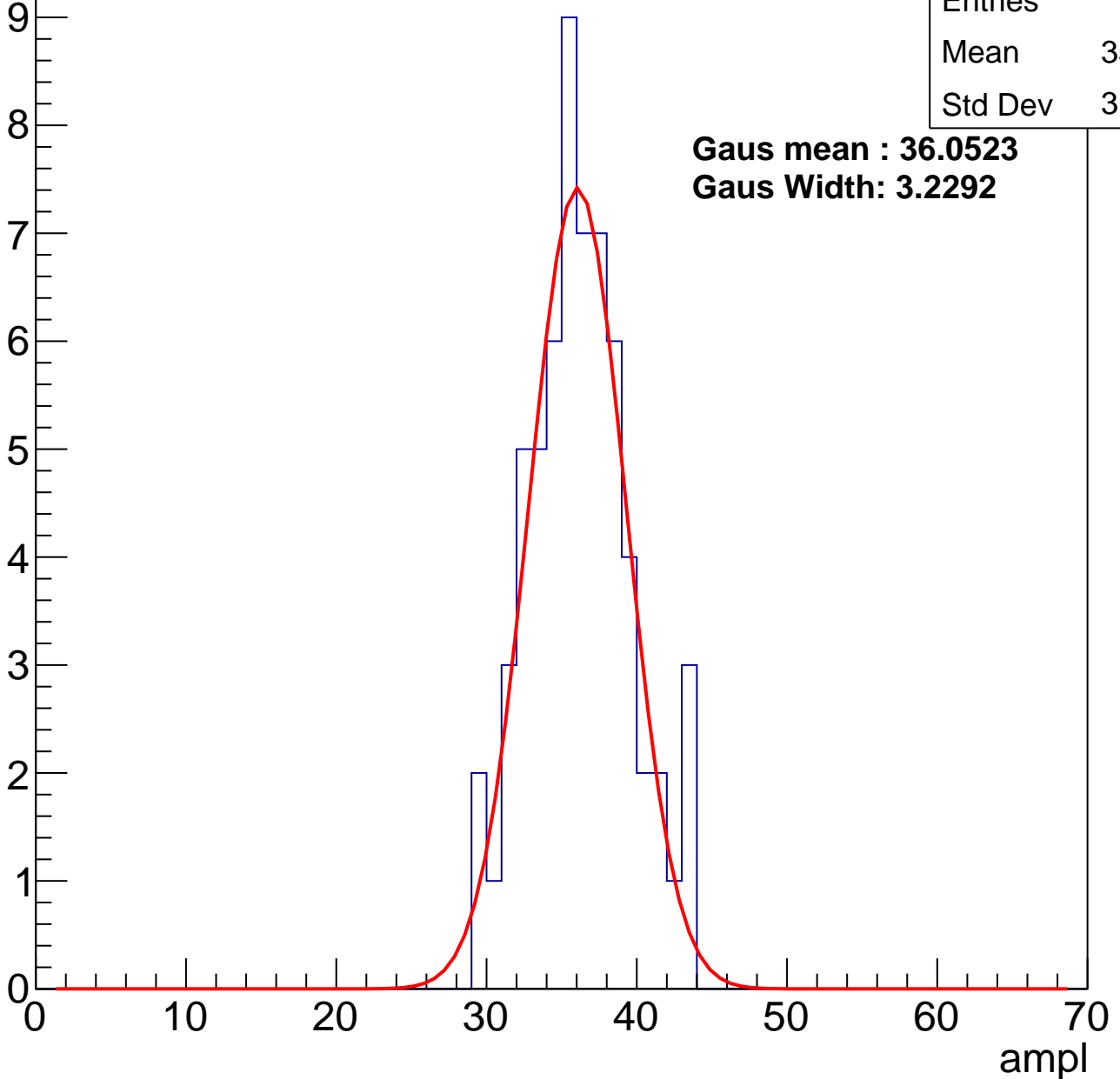
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	35.76
Std Dev	3.322

**Gaus mean : 36.0523**

**Gaus Width: 3.2292**



# B1L103S, U1-ch105, adc2

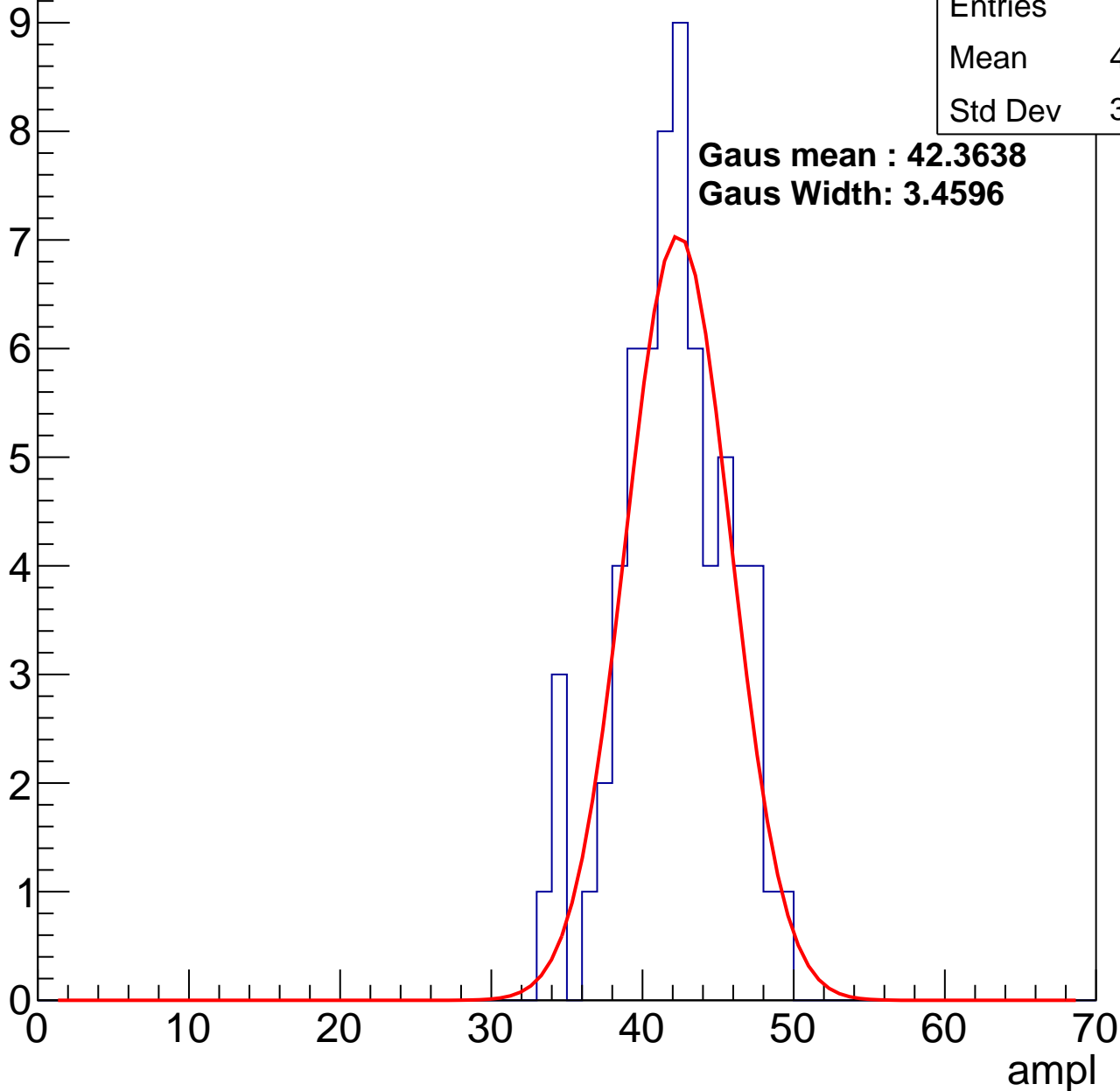
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	41.62
Std Dev	3.542

**Gaus mean : 42.3638**

**Gaus Width: 3.4596**

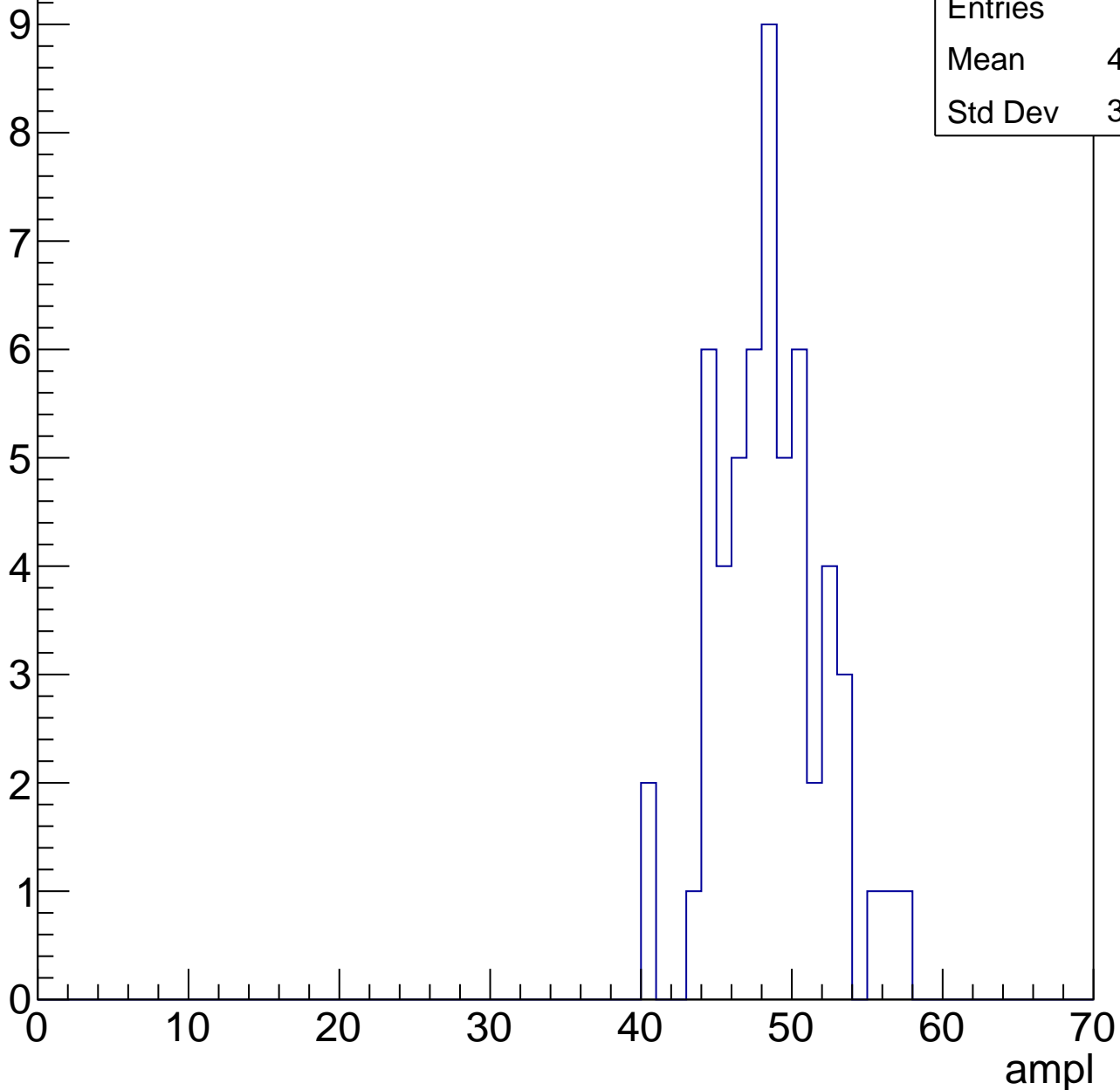


# B1L103S, U1-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	48.09
Std Dev	3.512

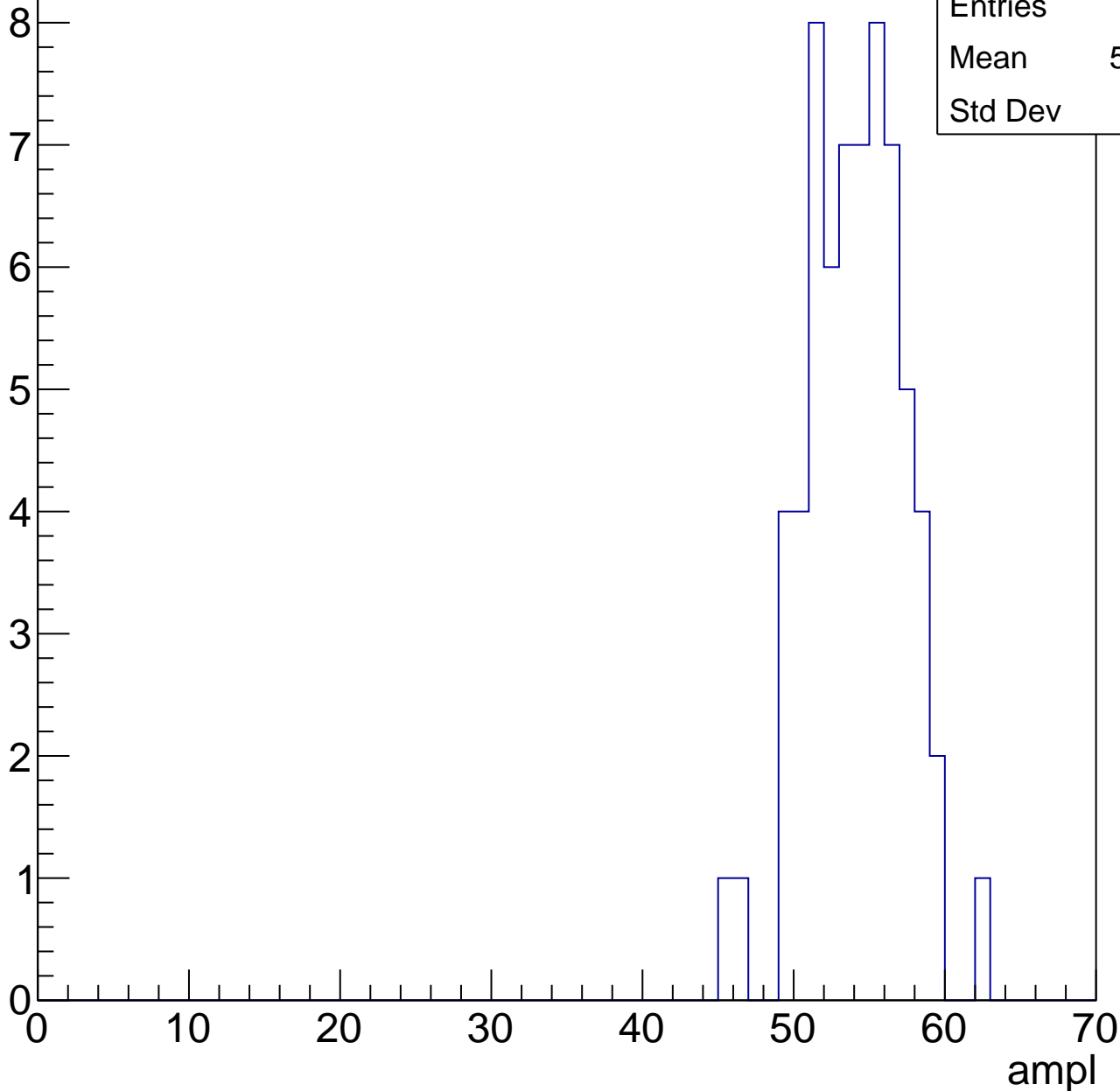


# B1L103S, U1-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

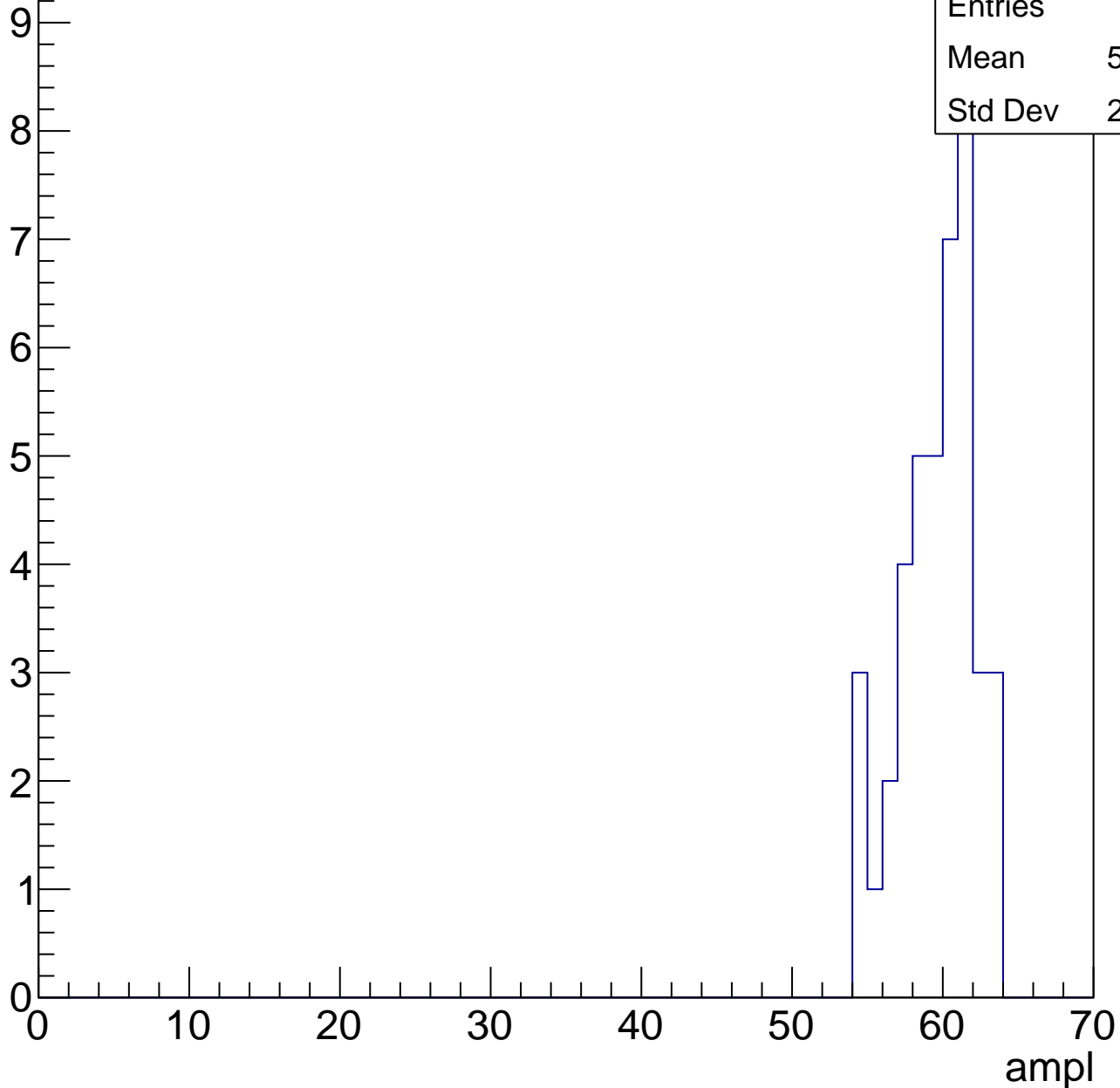
Entries	65
Mean	53.62
Std Dev	3.19



# B1L103S, U1-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



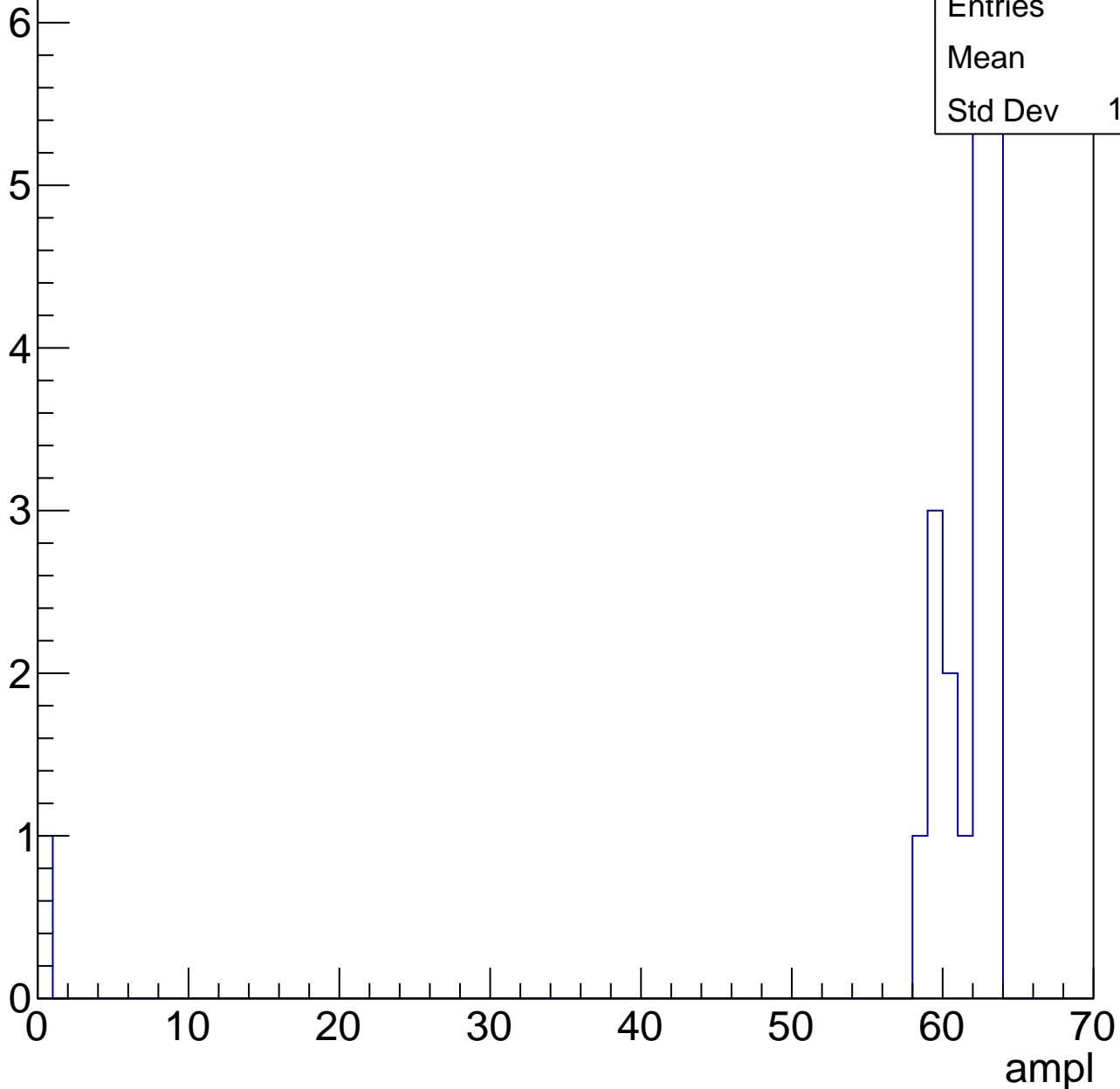
Entries	42
Mean	59.19
Std Dev	2.422

# B1L103S, U1-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	20
Mean	58.3
Std Dev	13.47

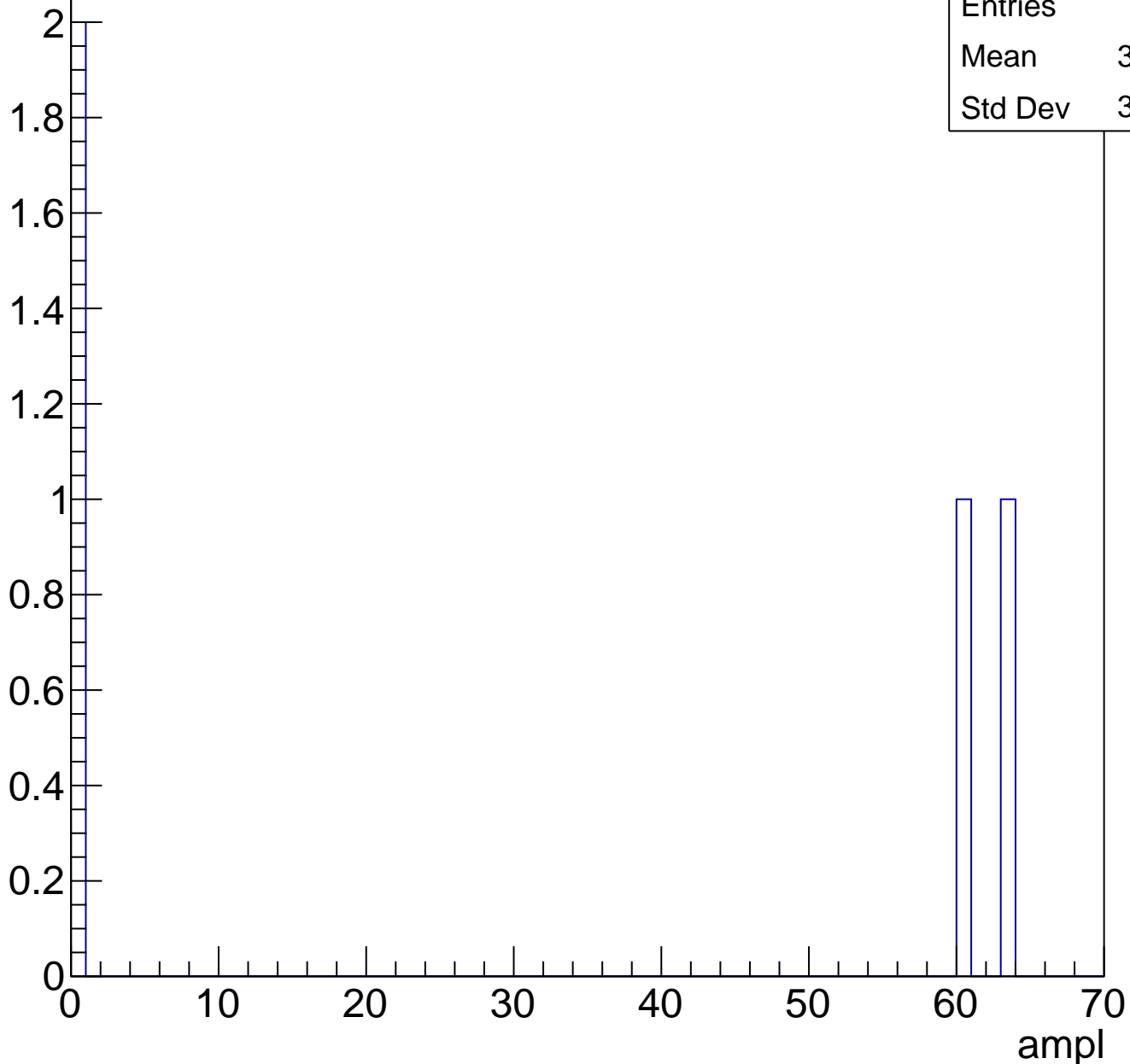




# B1L103S, U1-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	4
Mean	30.75
Std Dev	30.77

# B1L103S, U1-ch106, adc0

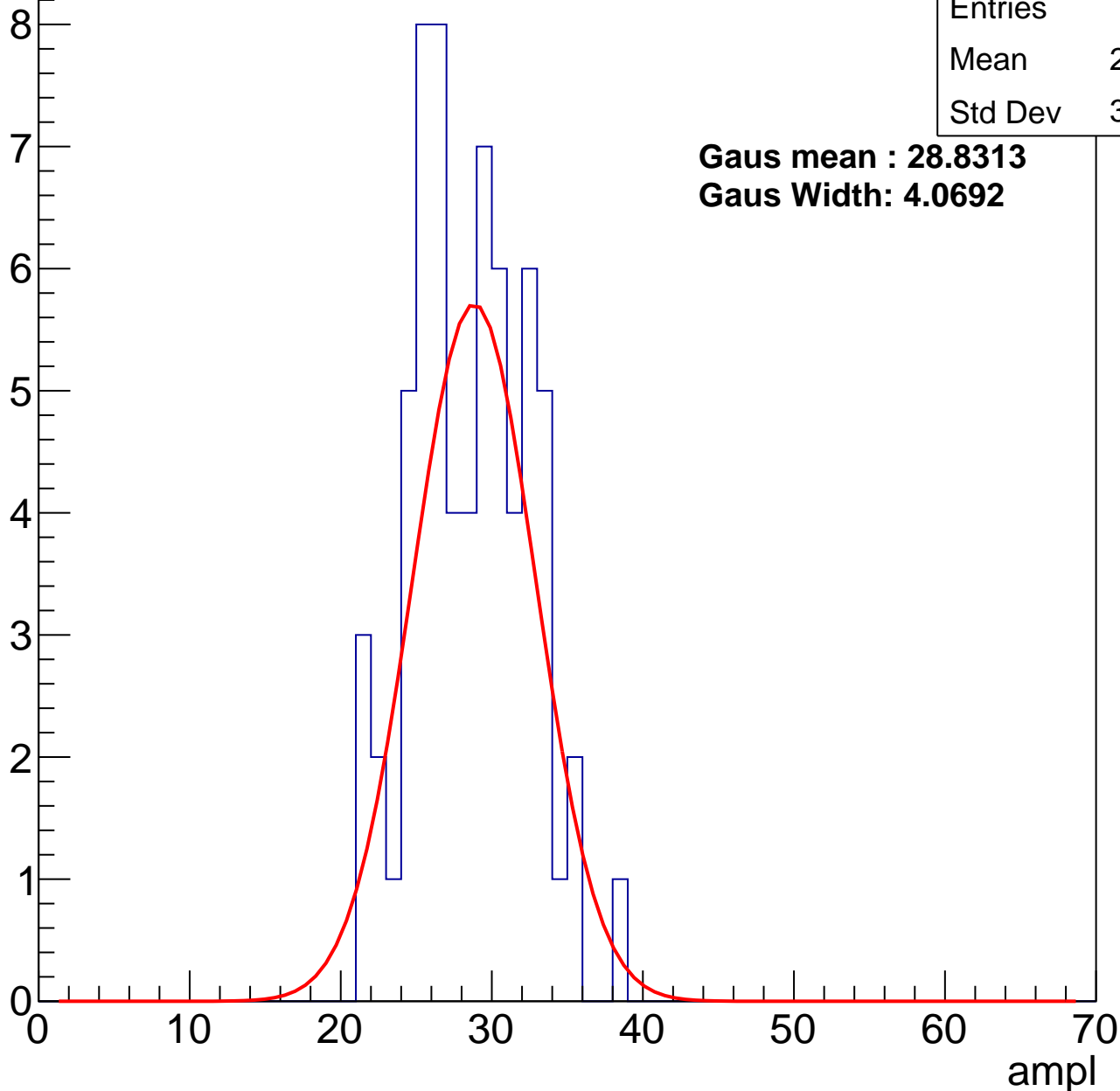
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	28.12
Std Dev	3.772

**Gaus mean : 28.8313**

**Gaus Width: 4.0692**



# B1L103S, U1-ch106, adc1

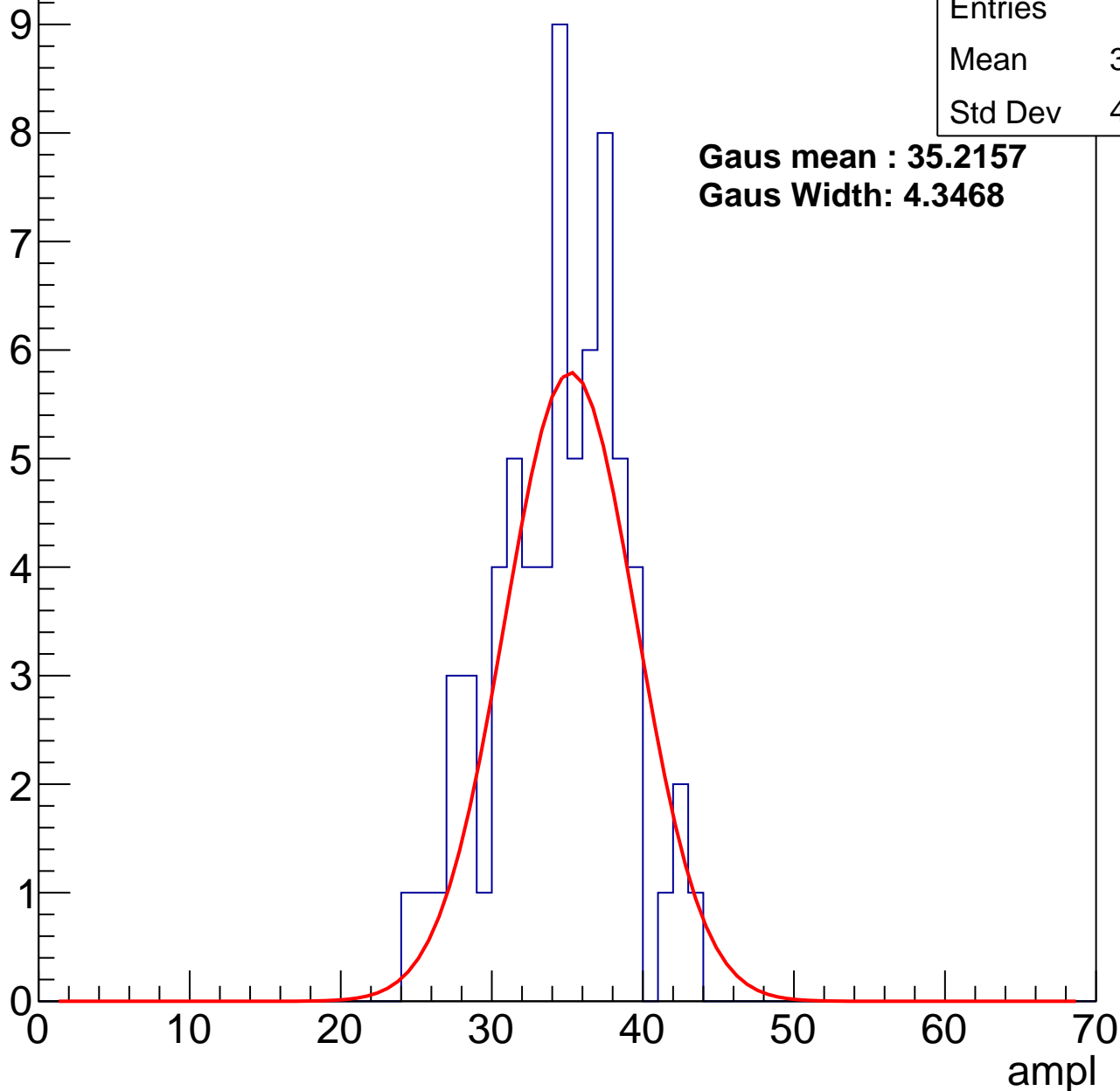
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	33.99
Std Dev	4.189

**Gaus mean : 35.2157**

**Gaus Width: 4.3468**



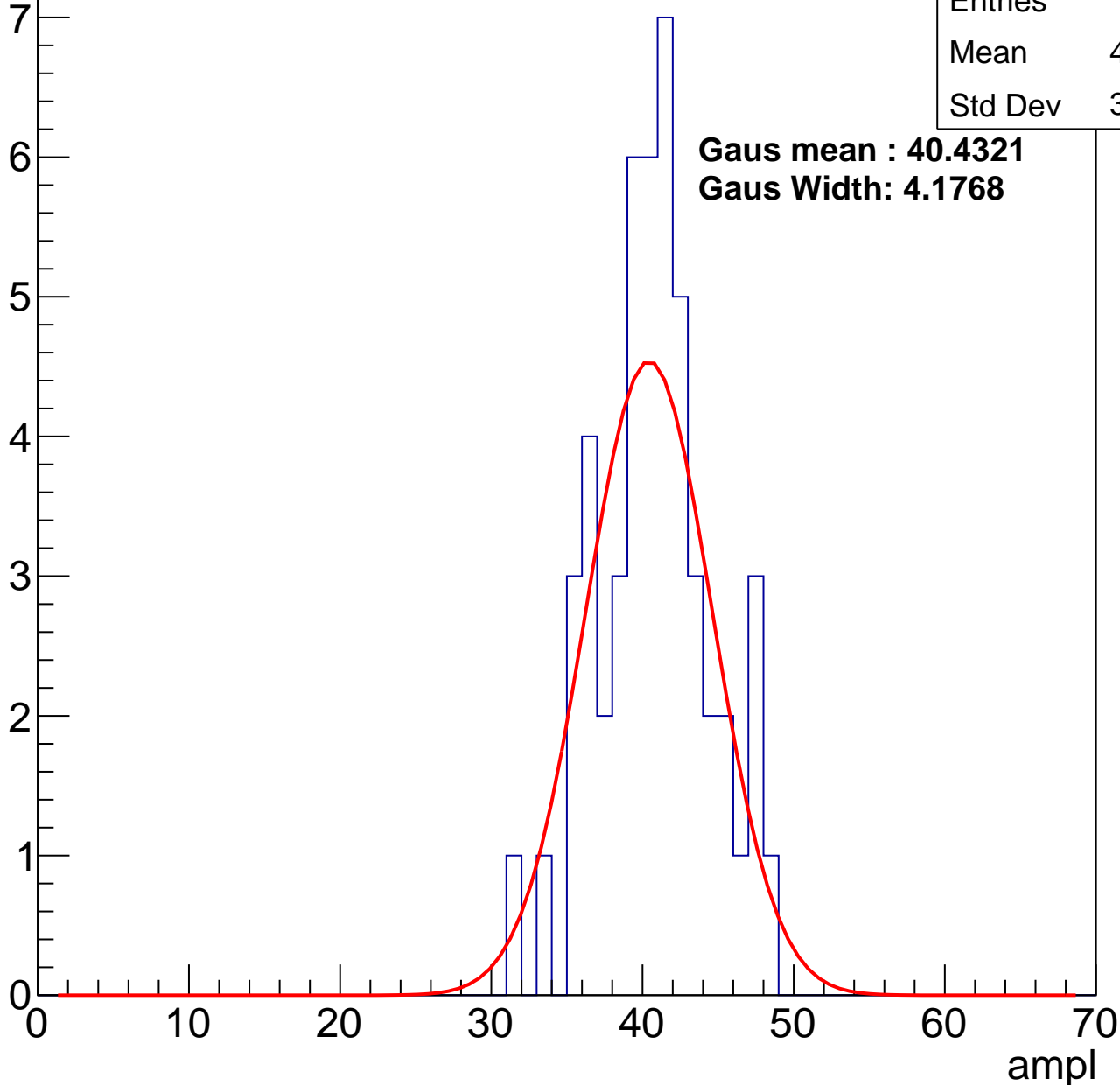
# B1L103S, U1-ch106, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	40.28
Std Dev	3.699

**Gaus mean : 40.4321**  
**Gaus Width: 4.1768**

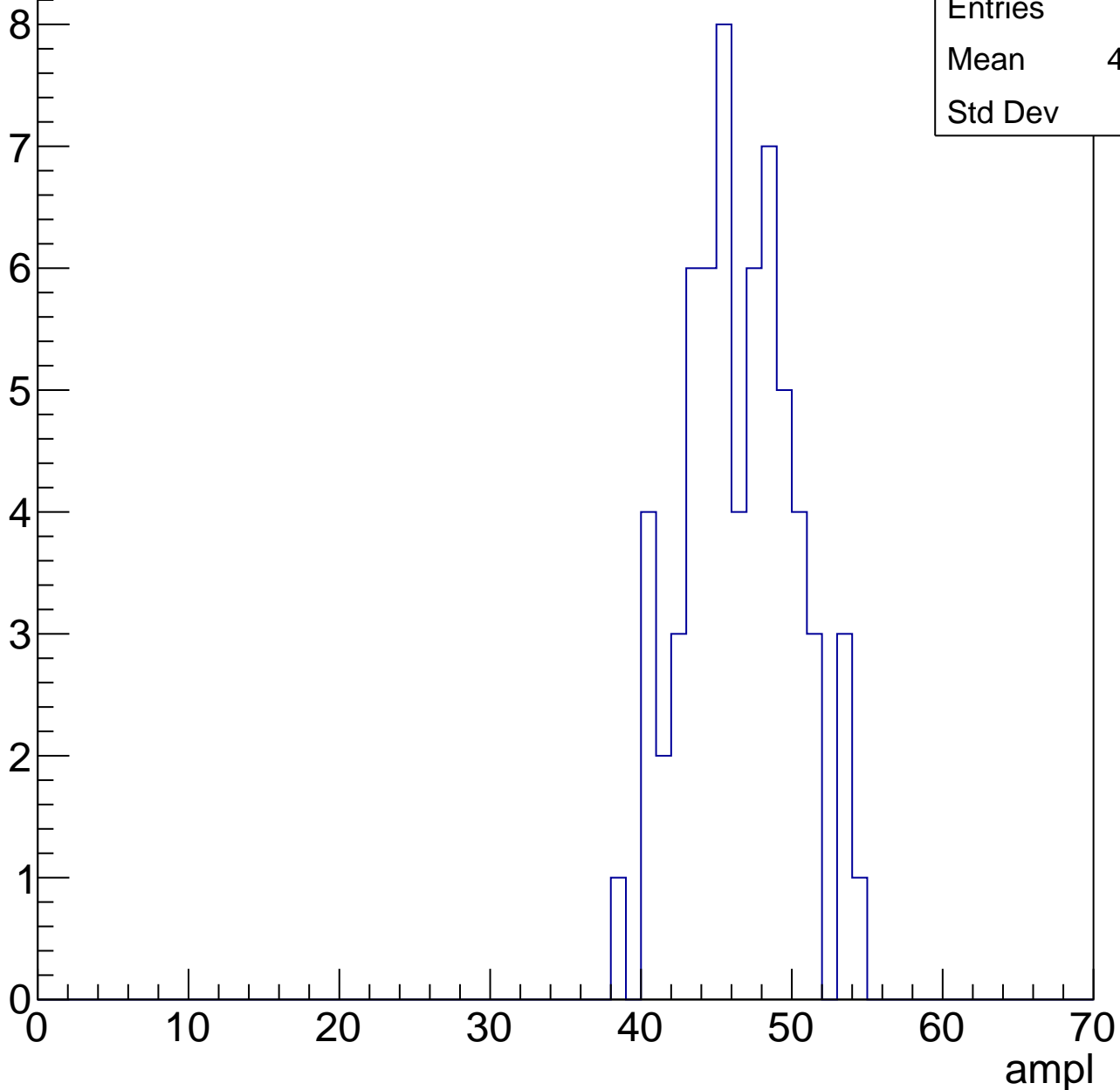


# B1L103S, U1-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	46.05
Std Dev	3.61

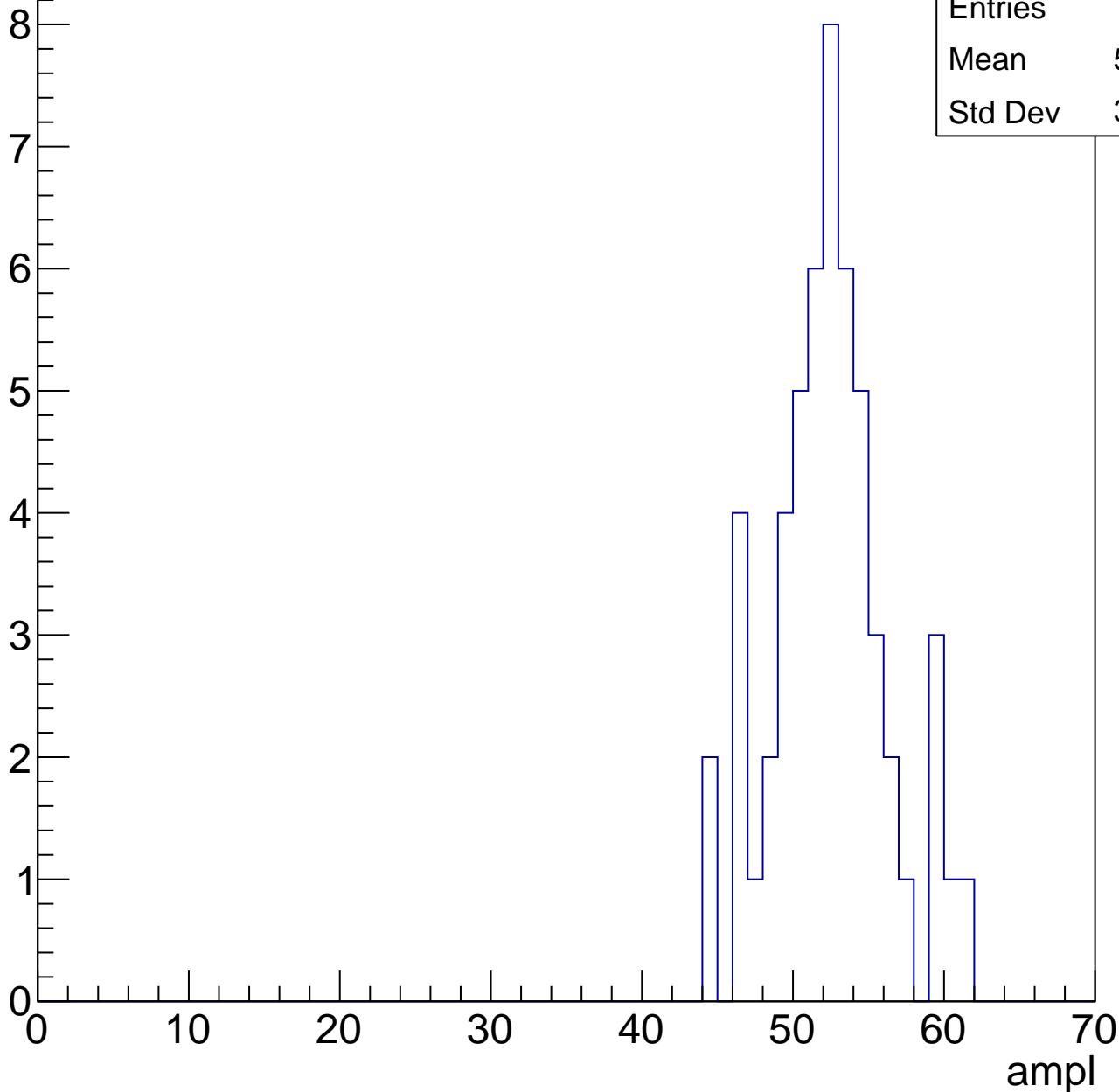


# B1L103S, U1-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	51.91
Std Dev	3.831

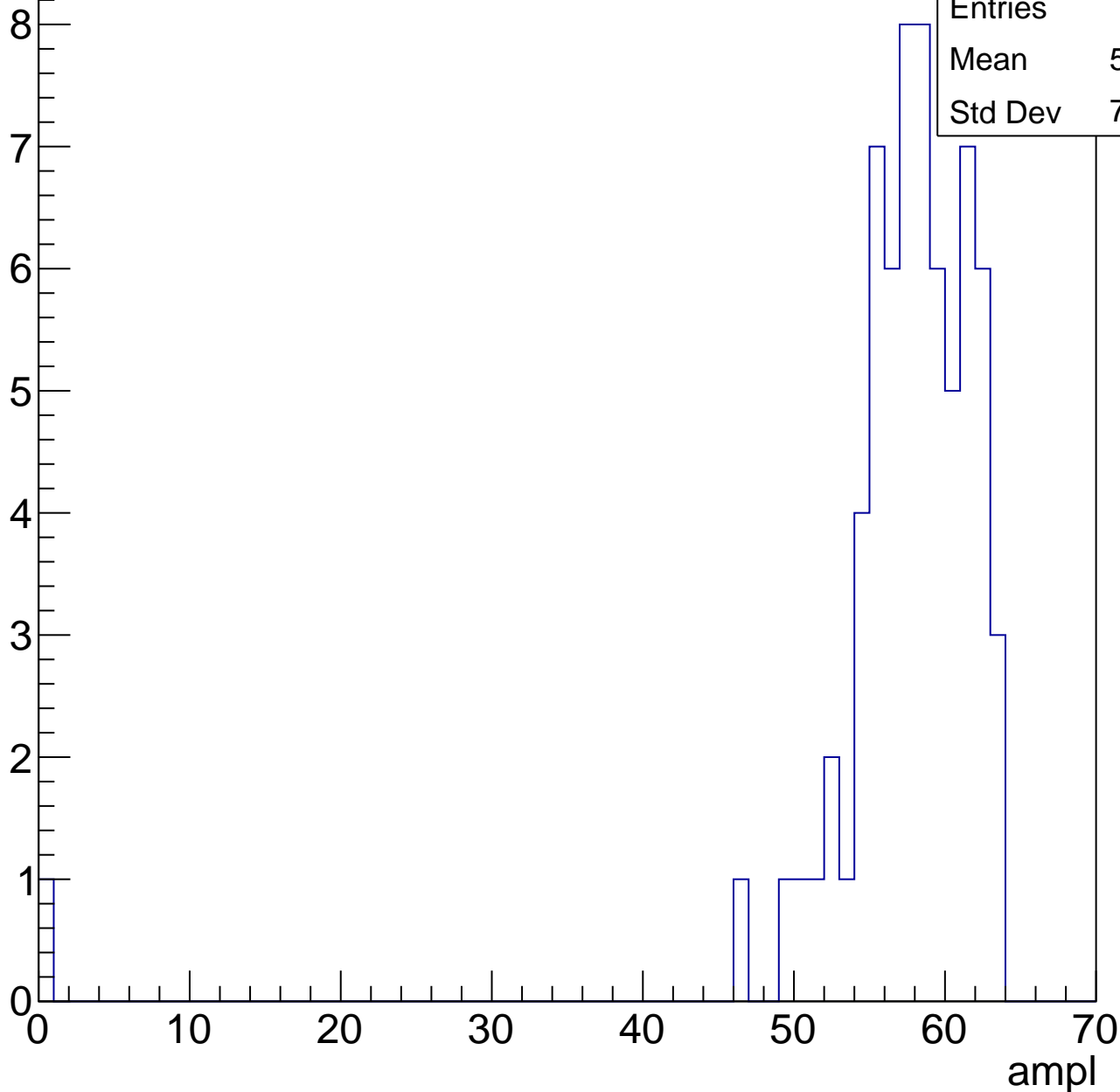


# B1L103S, U1-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	56.65
Std Dev	7.759

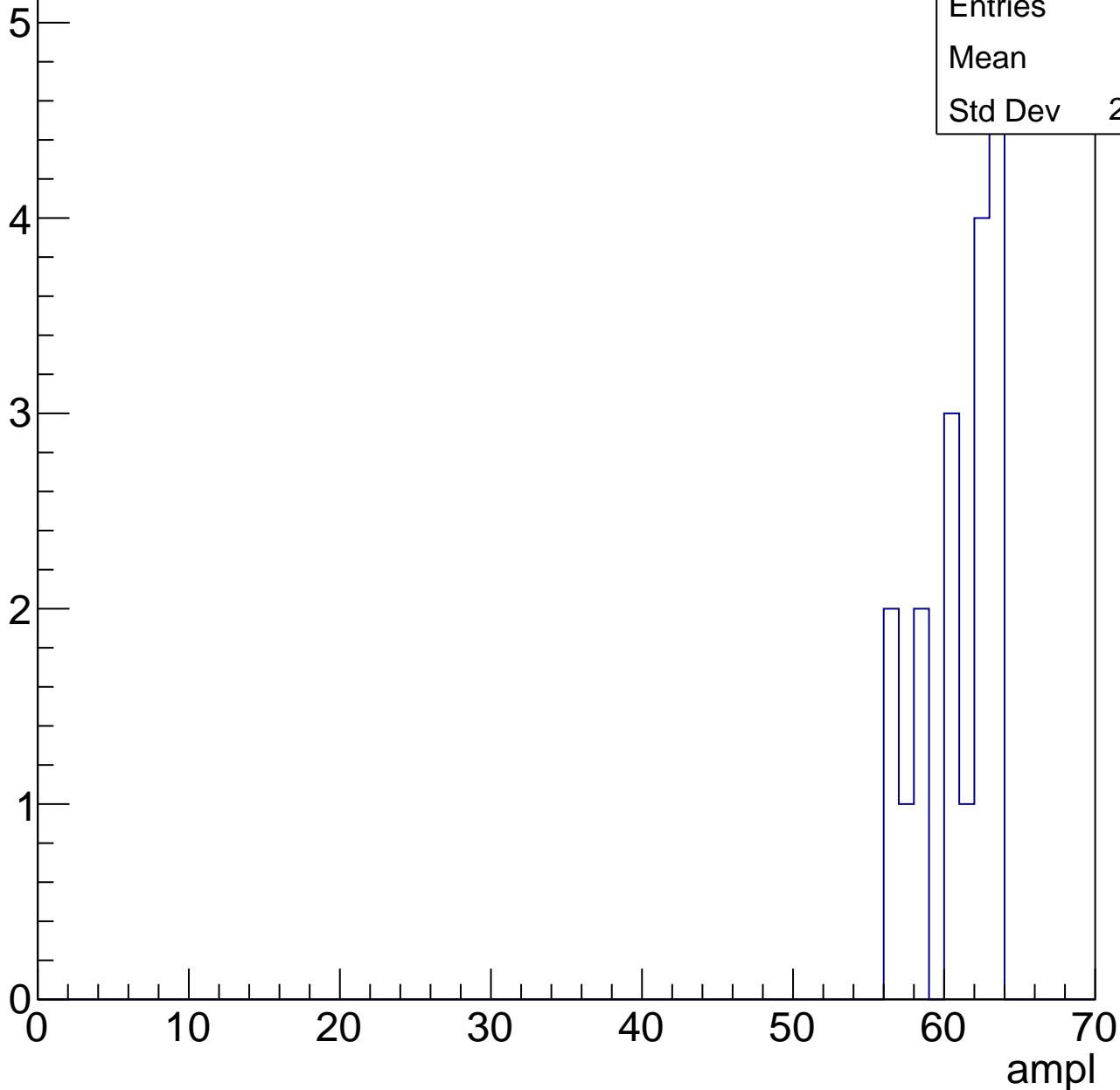


# B1L103S, U1-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	18
Mean	60.5
Std Dev	2.432





# B1L103S, U1-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

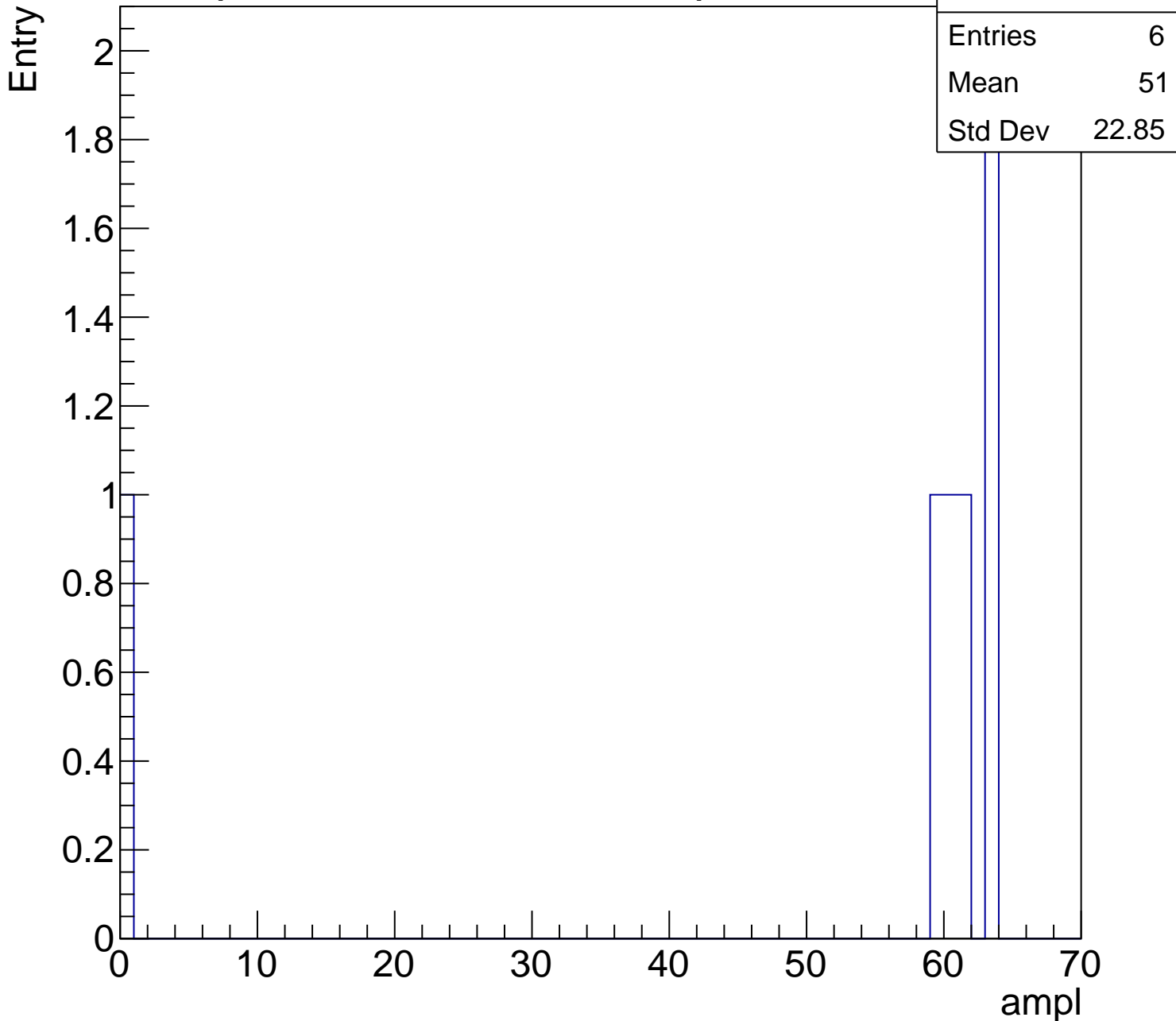
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	51
Std Dev	22.85

0 10 20 30 40 50 60 70

ampl



# B1L103S, U1-ch107, adc0

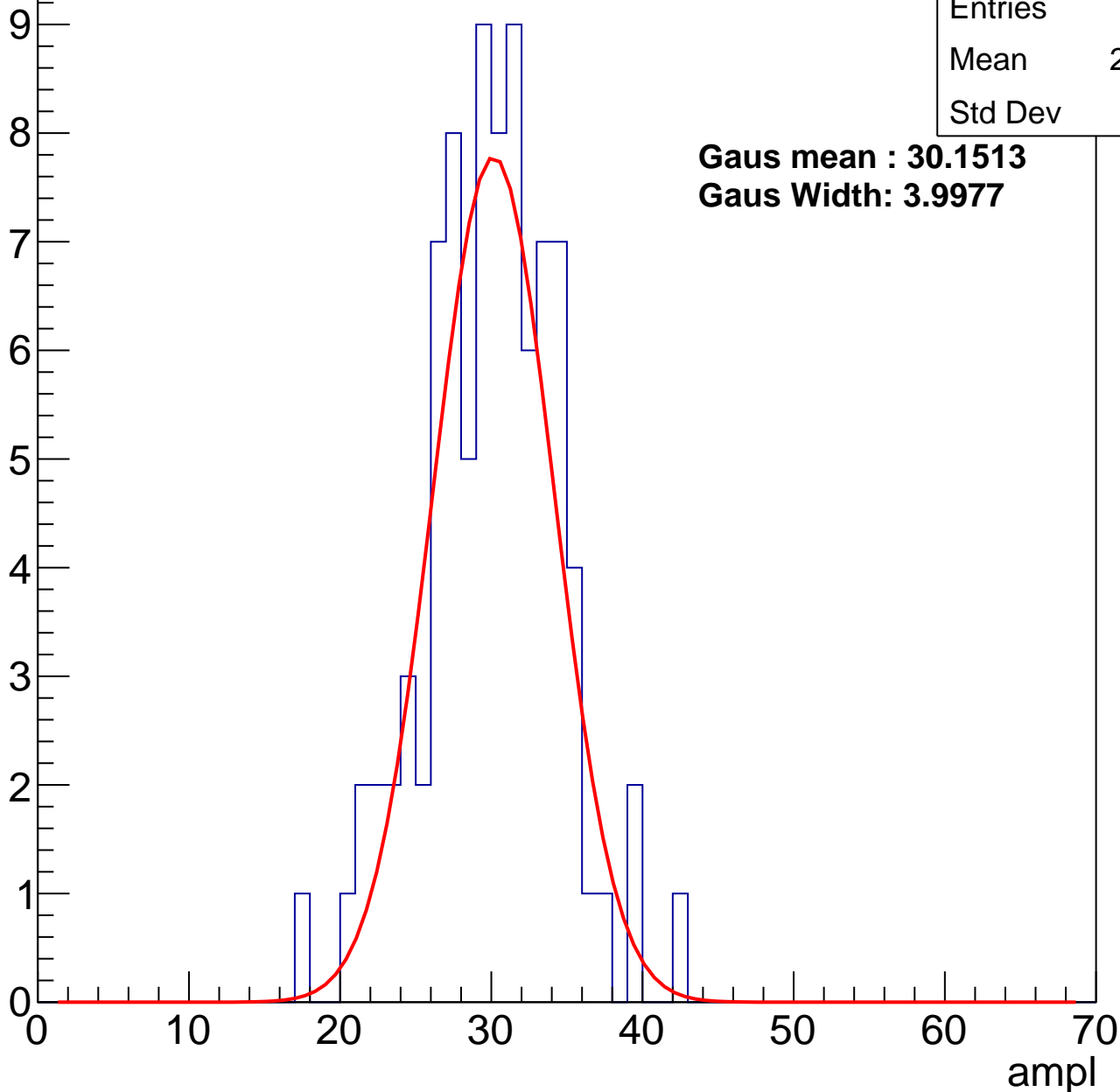
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	88
Mean	29.58
Std Dev	4.41

**Gaus mean : 30.1513**

**Gaus Width: 3.9977**



# B1L103S, U1-ch107, adc1

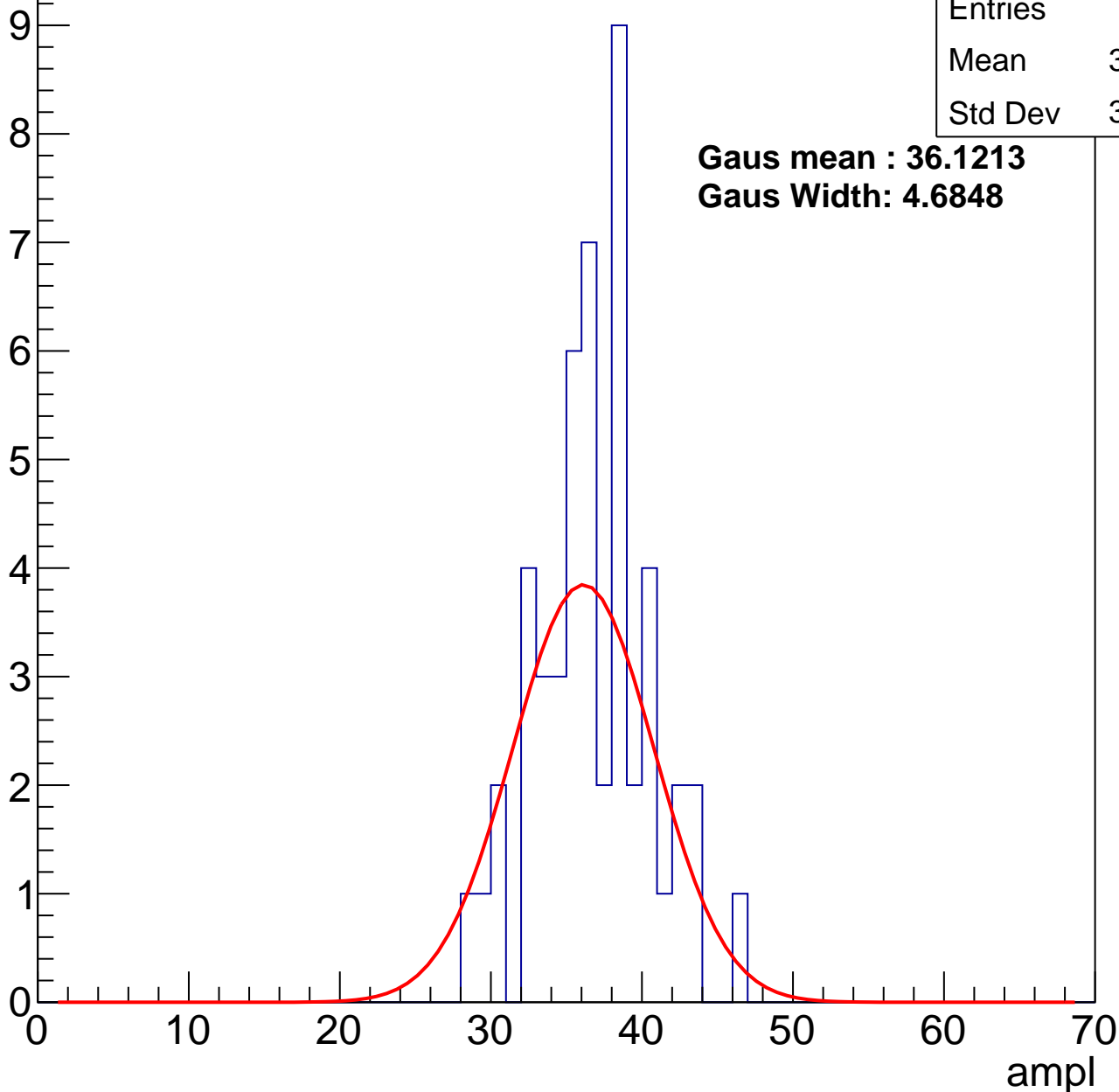
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	36.38
Std Dev	3.746

**Gaus mean : 36.1213**

**Gaus Width: 4.6848**



# B1L103S, U1-ch107, adc2

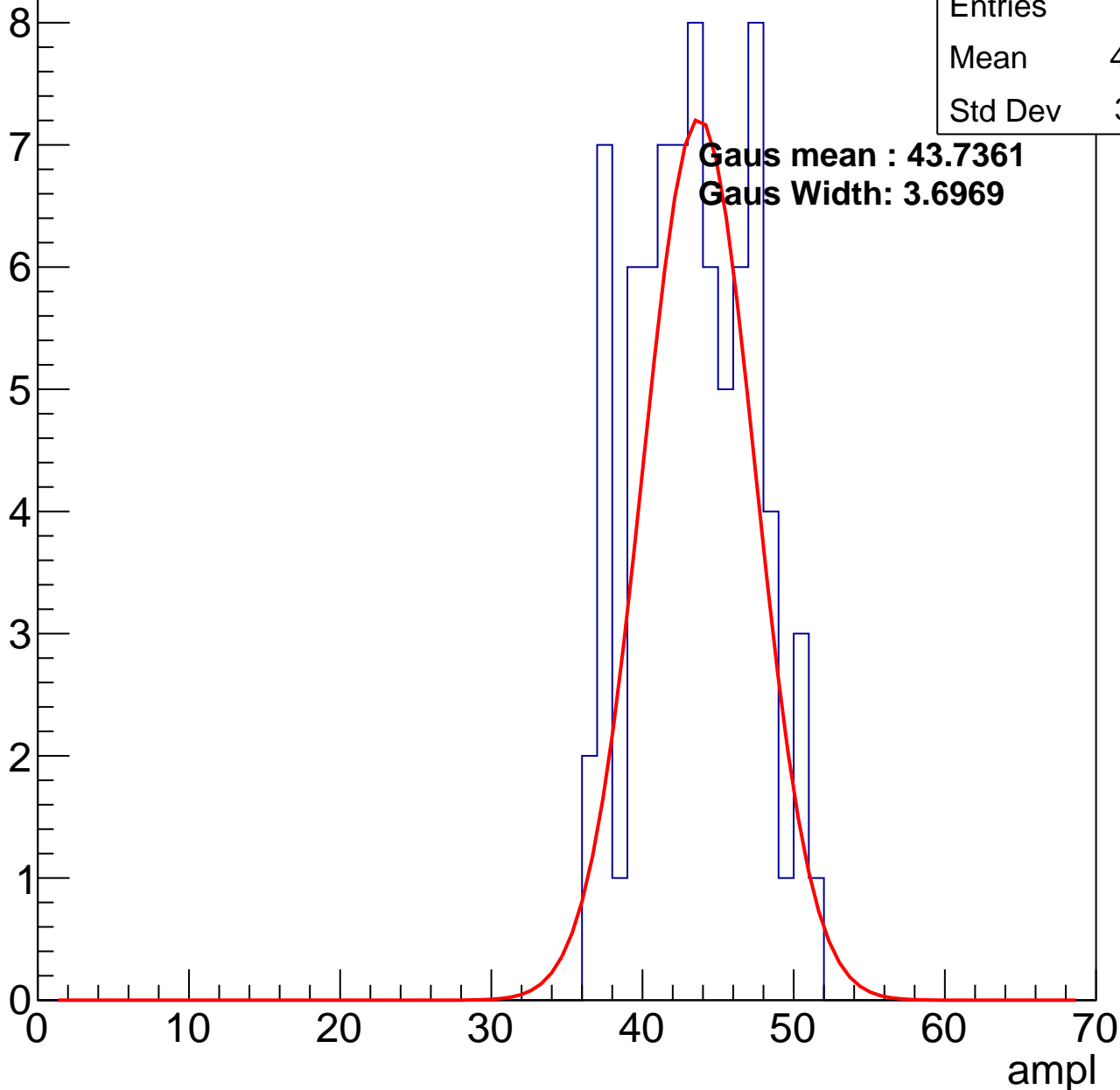
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	42.96
Std Dev	3.781

**Gaus mean : 43.7361**

**Gaus Width: 3.6969**

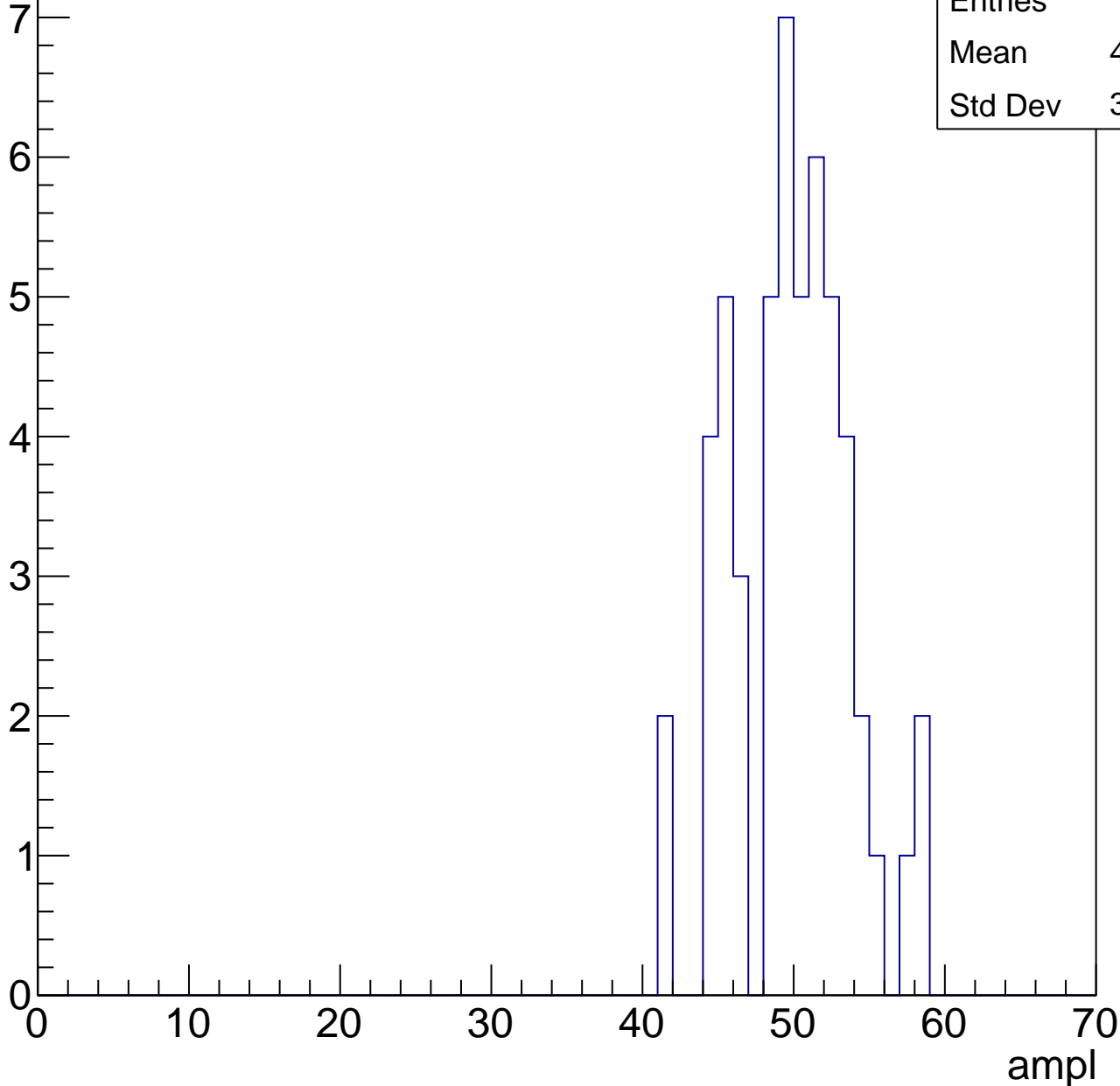


# B1L103S, U1-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	49.38
Std Dev	3.879

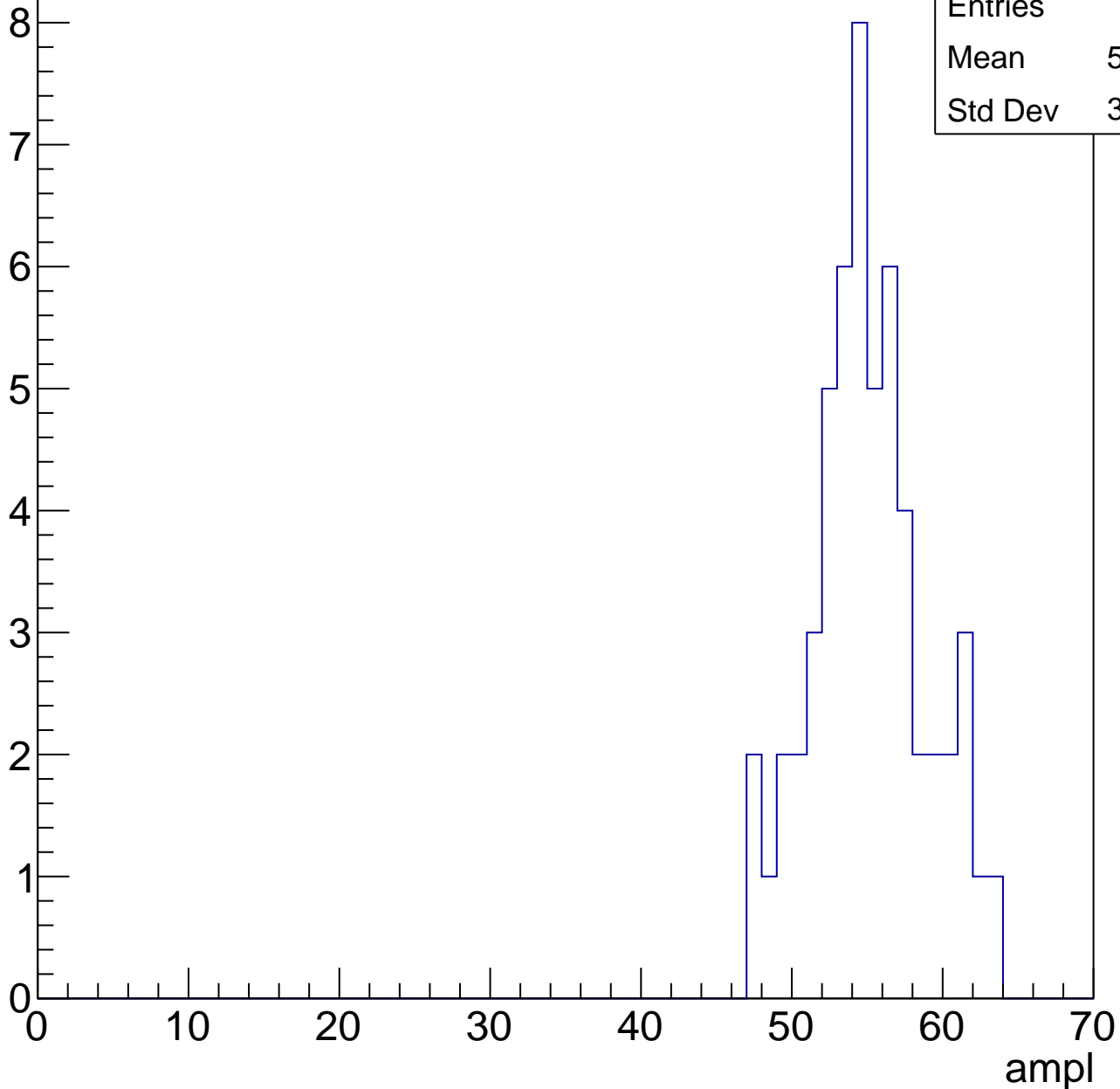


# B1L103S, U1-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	54.62
Std Dev	3.715

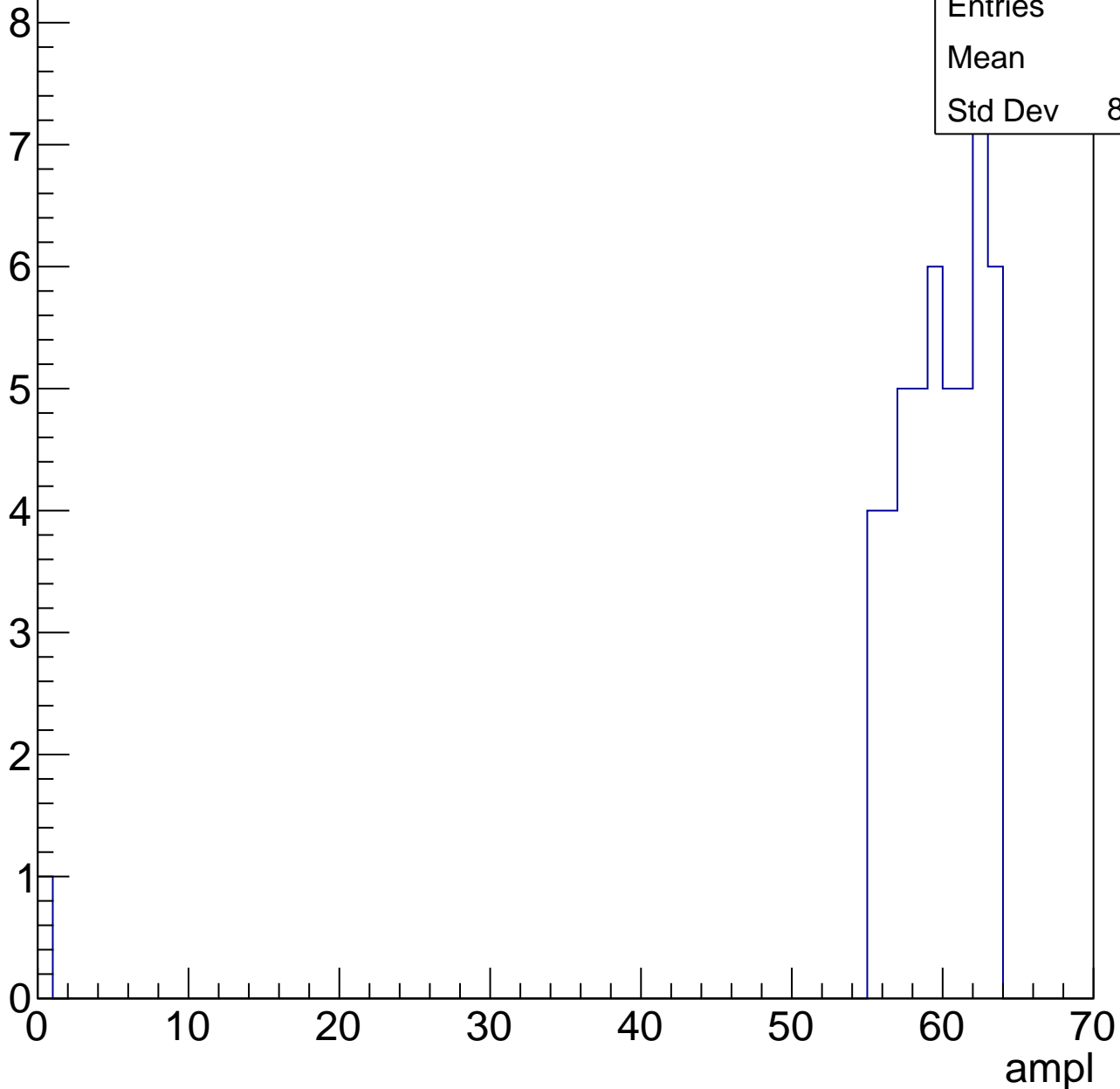


# B1L103S, U1-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

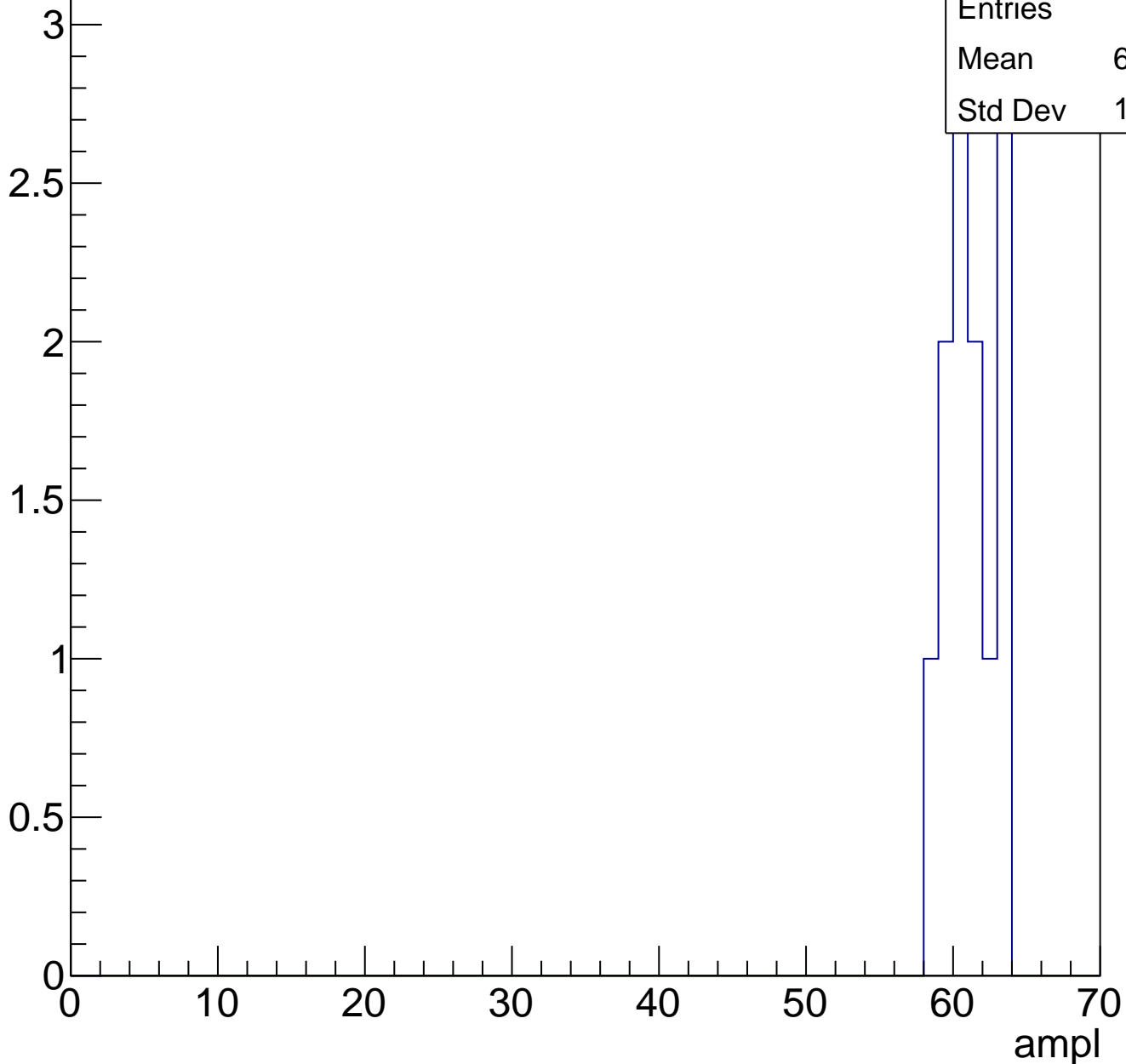
Entries	49
Mean	58.2
Std Dev	8.769



# B1L103S, U1-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U1-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U1-ch108, adc0

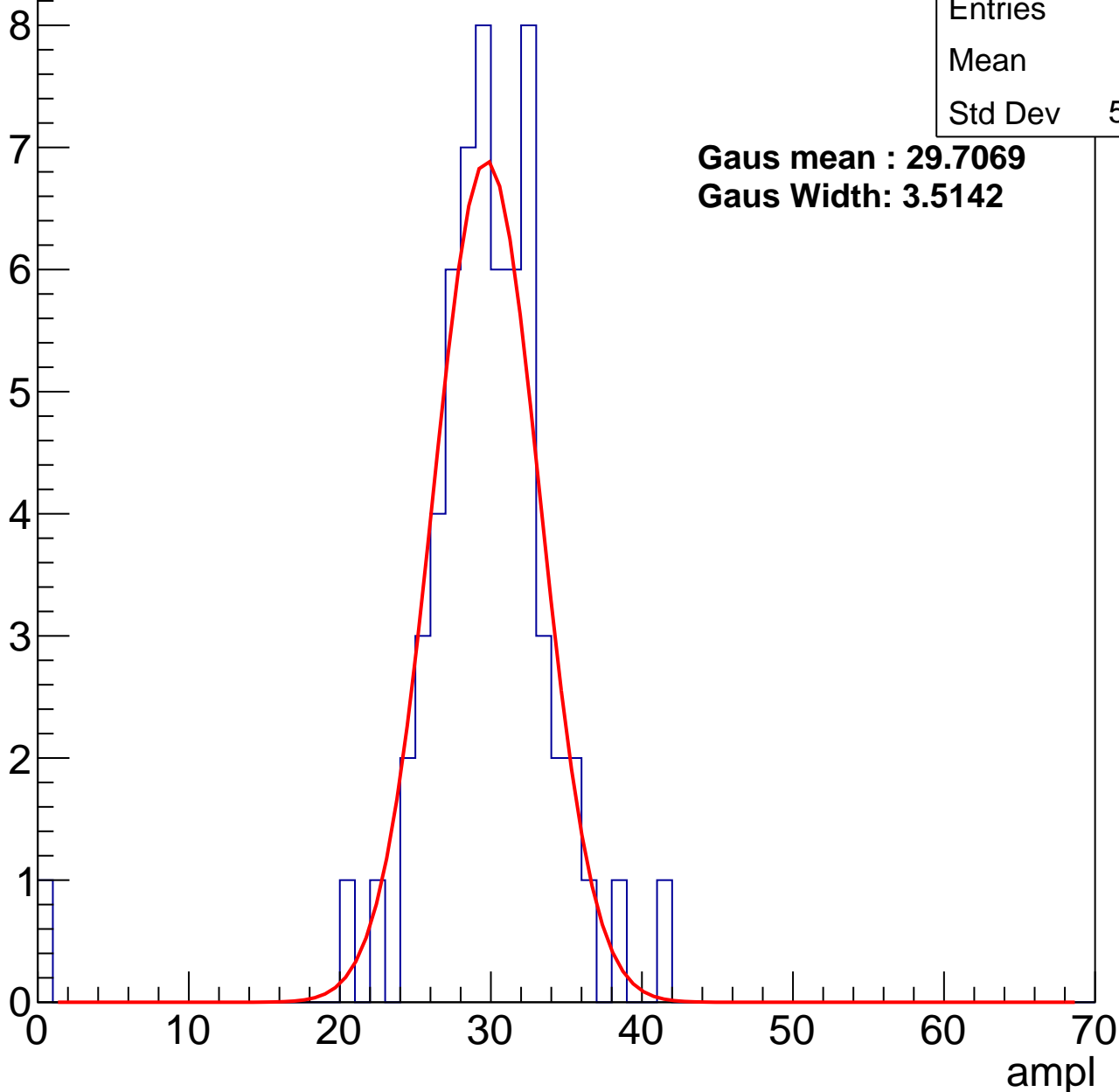
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	29.1
Std Dev	5.166

**Gaus mean : 29.7069**

**Gaus Width: 3.5142**



# B1L103S, U1-ch108, adc1

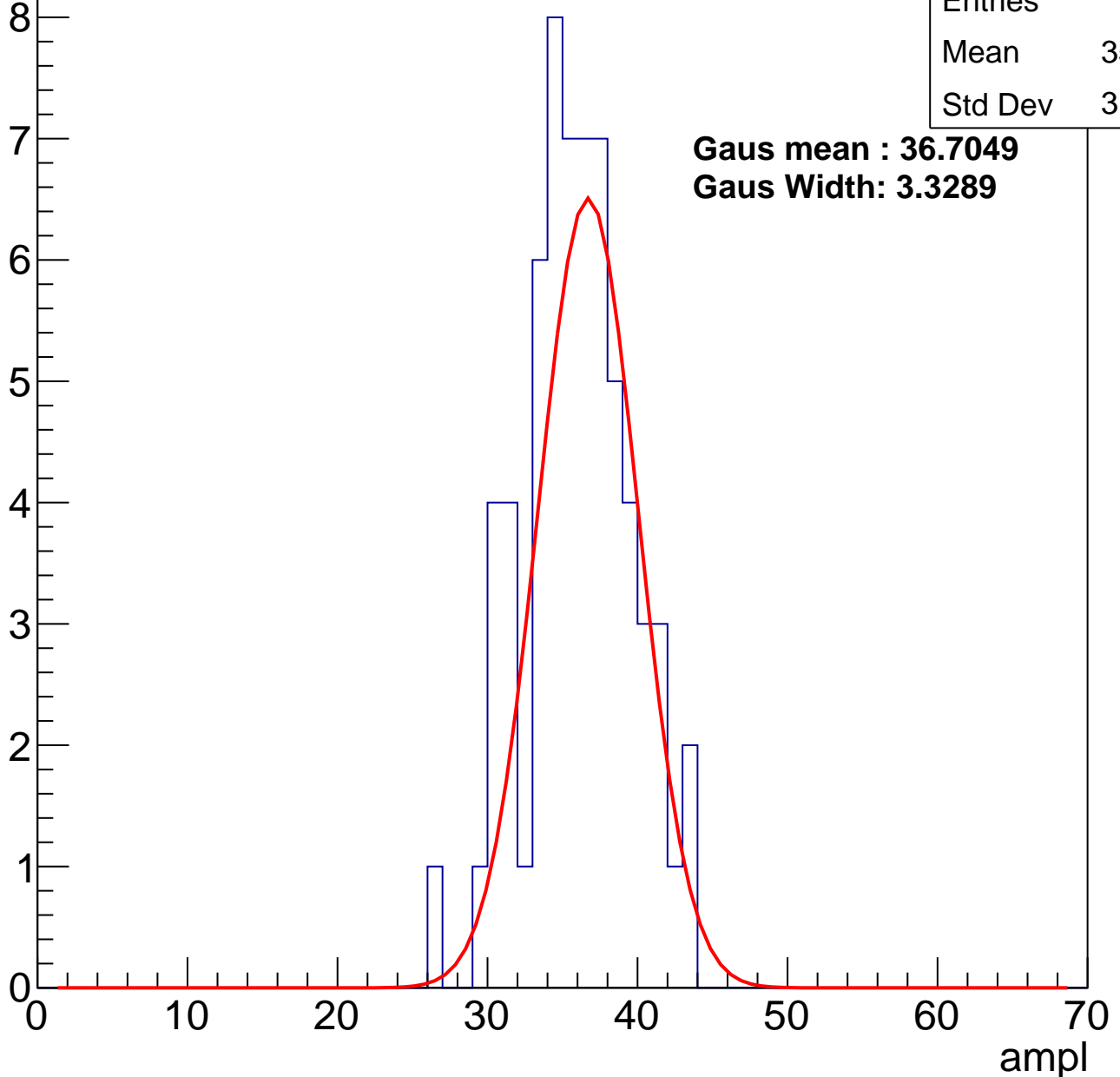
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	35.53
Std Dev	3.553

**Gaus mean : 36.7049**

**Gaus Width: 3.3289**



# B1L103S, U1-ch108, adc2

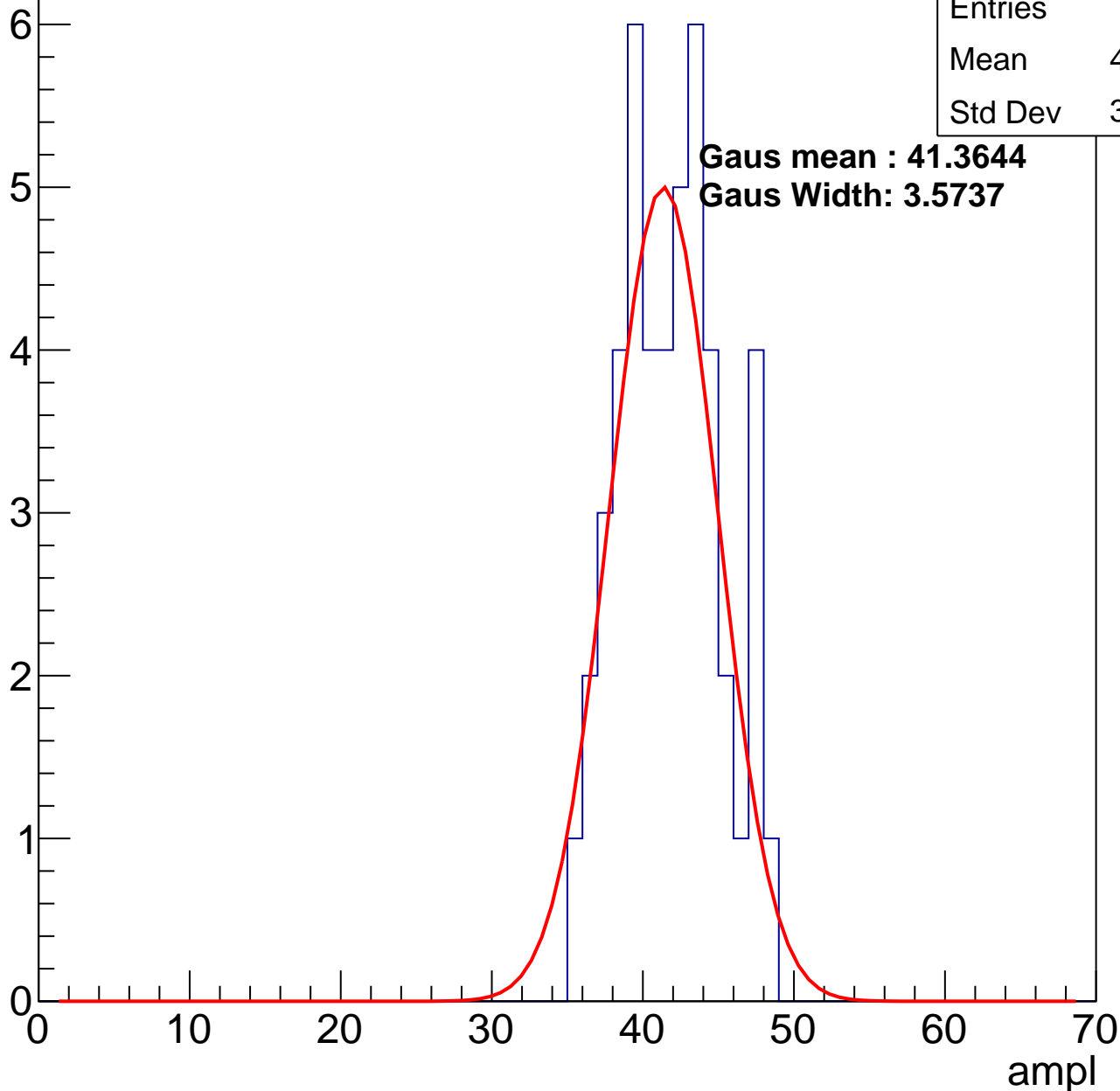
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	41.36
Std Dev	3.284

**Gaus mean : 41.3644**

**Gaus Width: 3.5737**

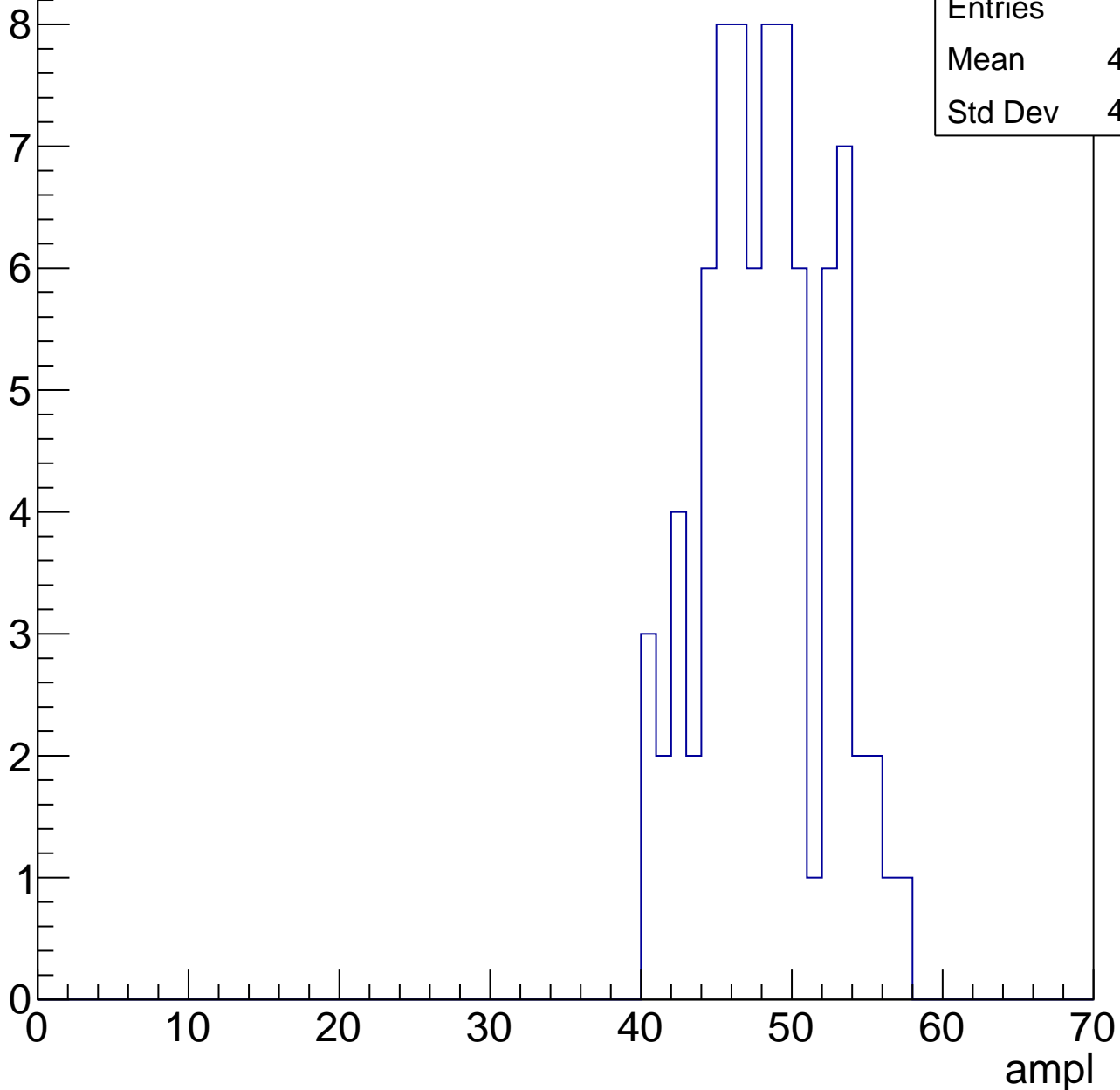


# B1L103S, U1-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	81
Mean	47.79
Std Dev	4.027

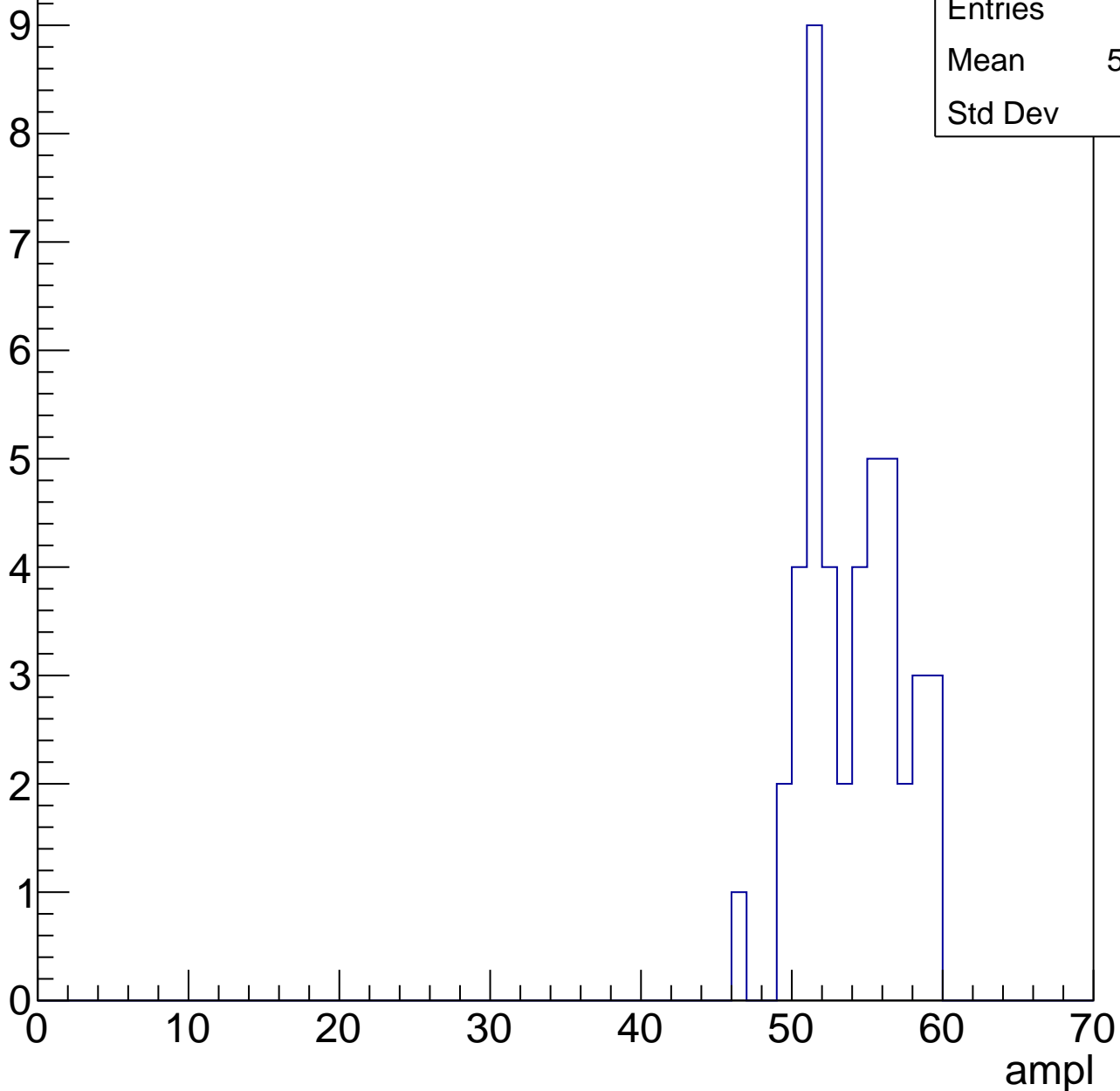


# B1L103S, U1-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	53.48
Std Dev	3.13

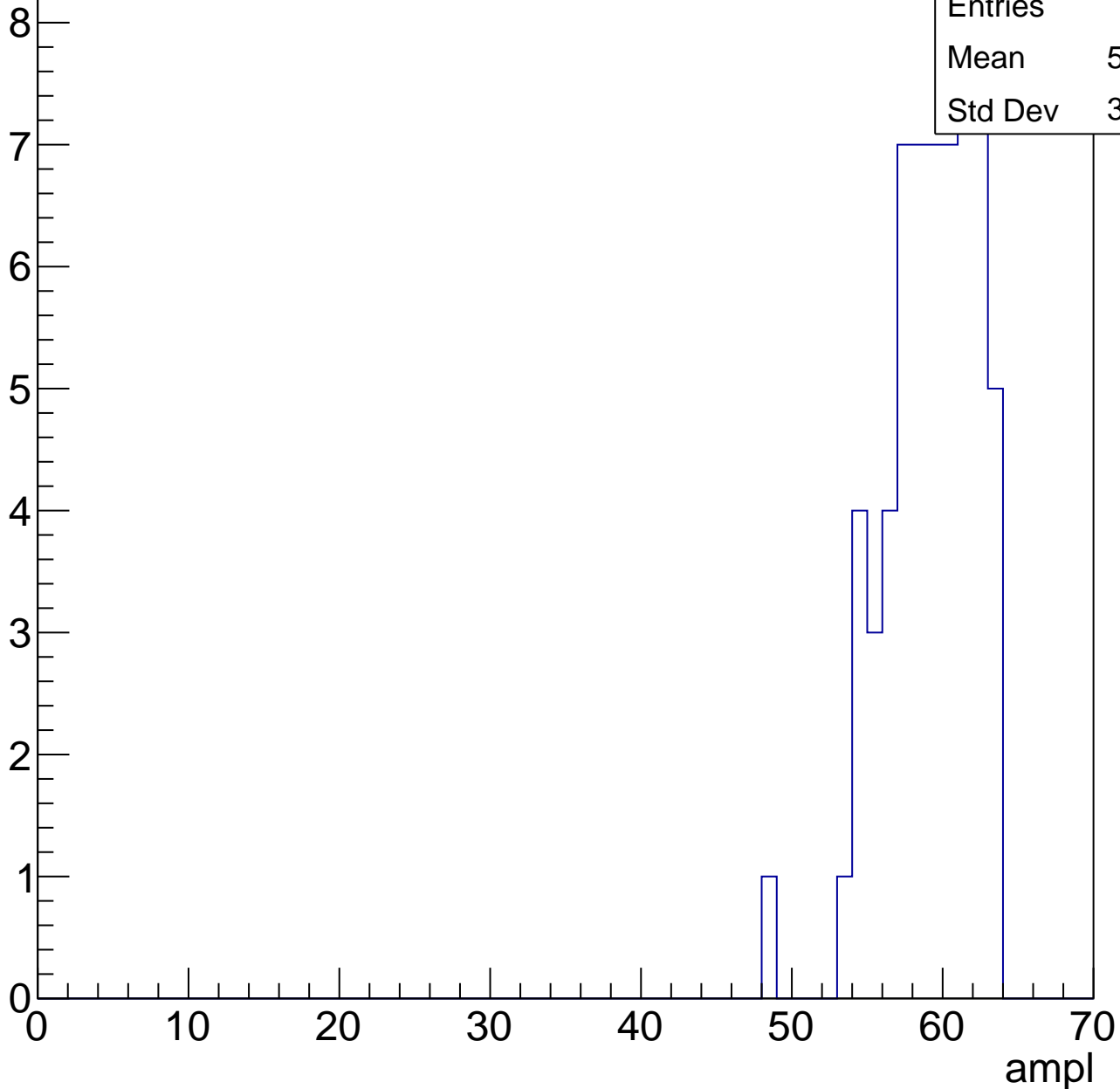


# B1L103S, U1-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

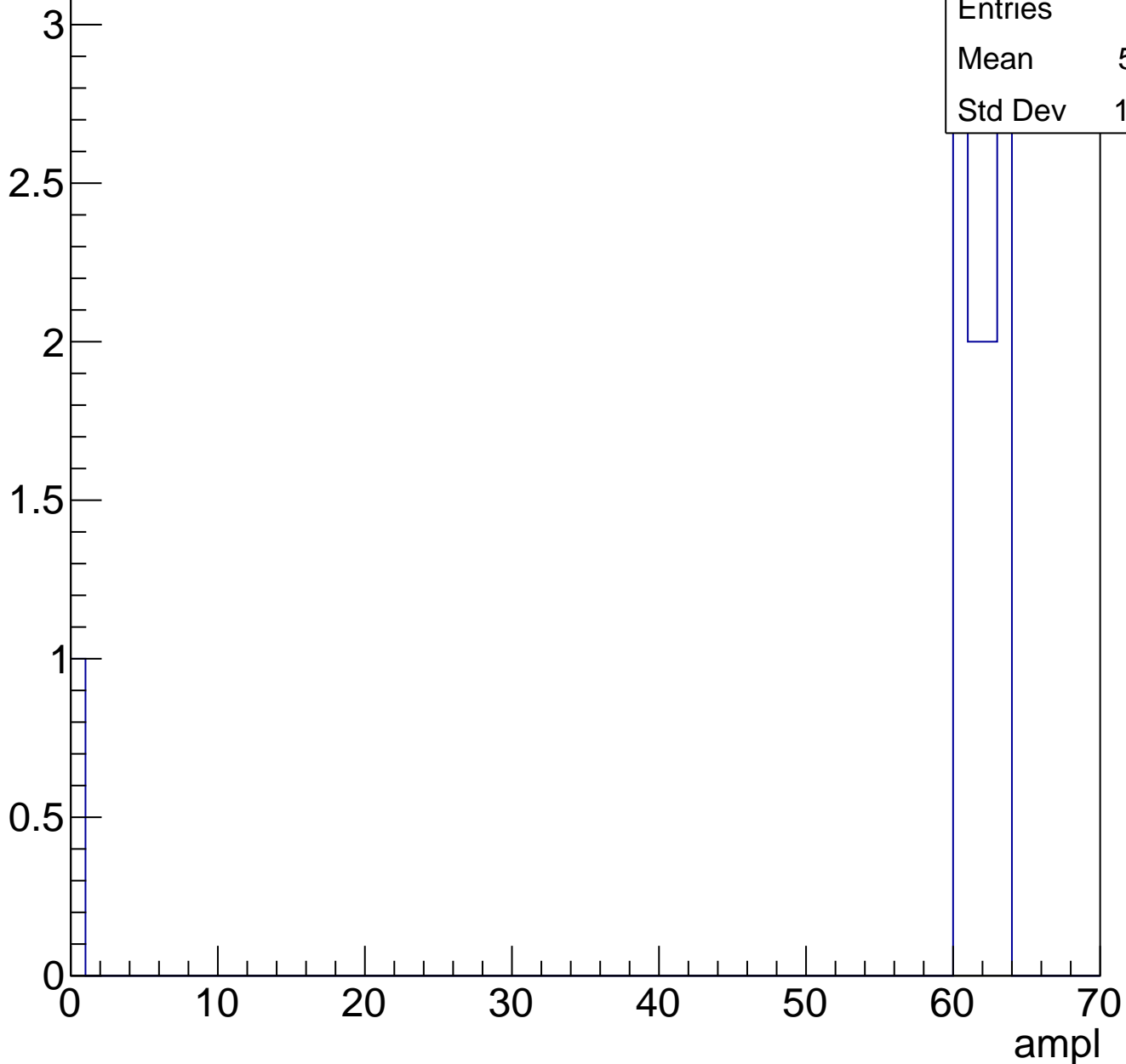
Entries	62
Mean	58.76
Std Dev	3.014



# B1L103S, U1-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

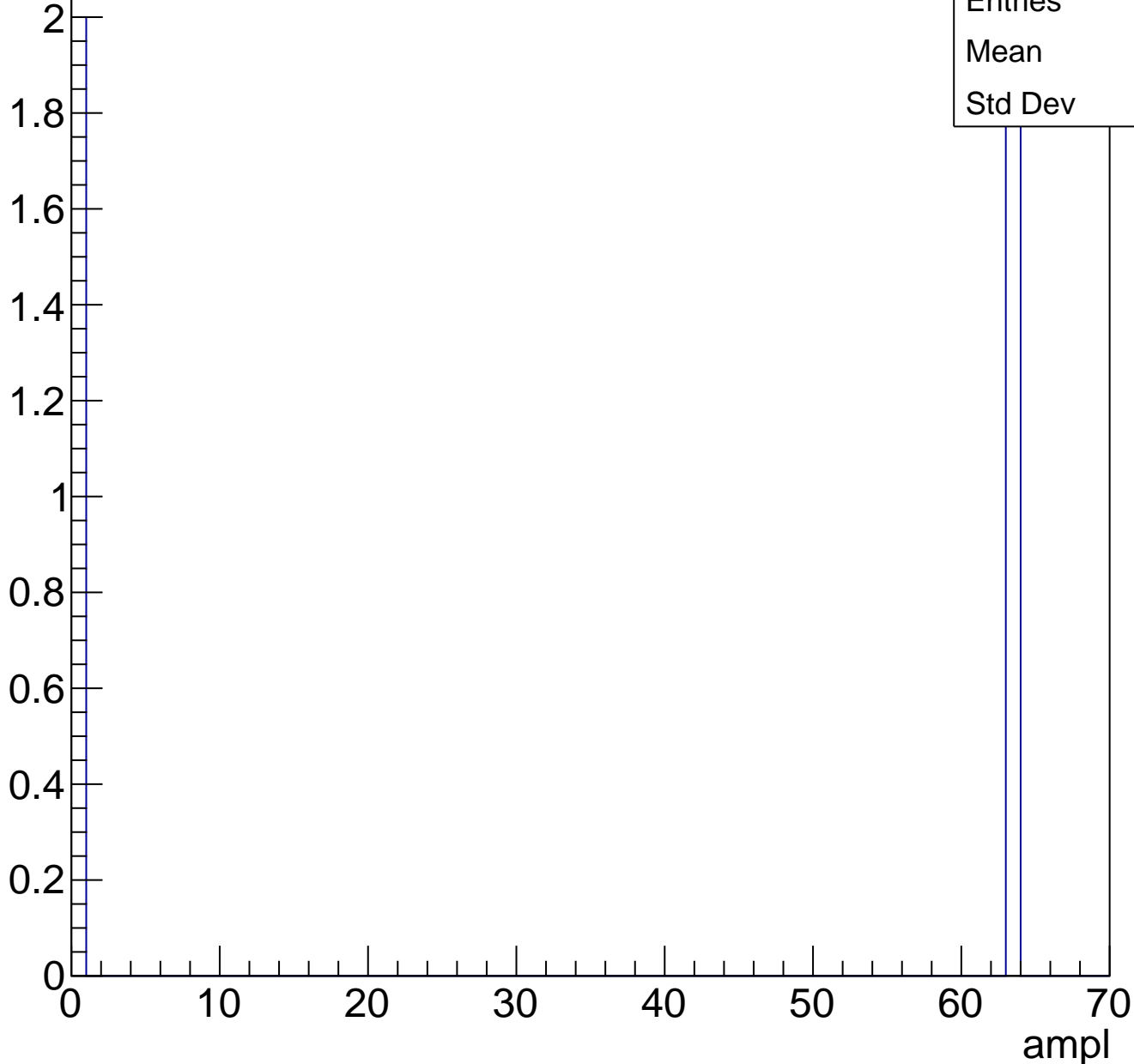




# B1L103S, U1-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch109, adc0

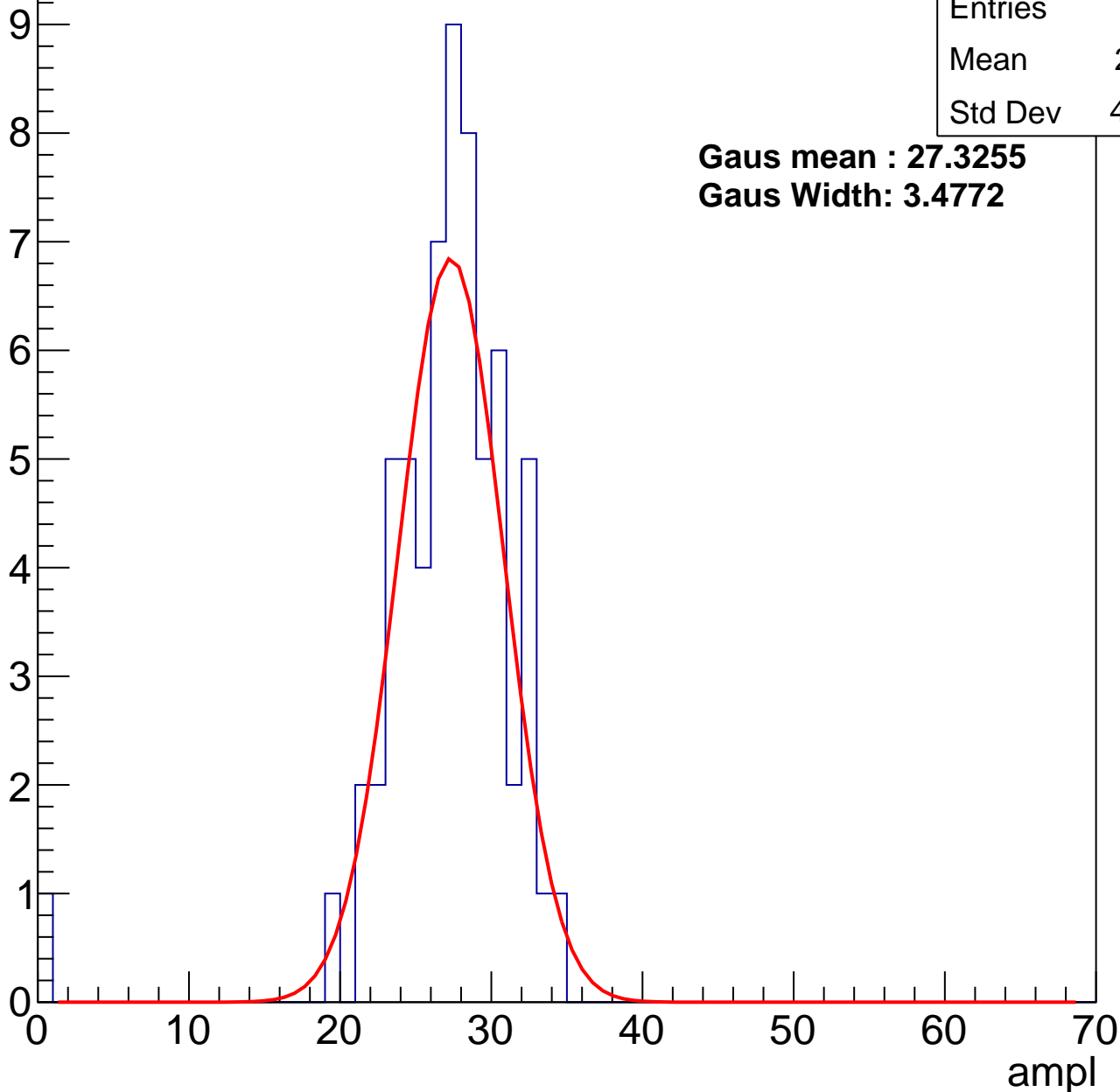
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	26.61
Std Dev	4.639

**Gaus mean : 27.3255**

**Gaus Width: 3.4772**



# B1L103S, U1-ch109, adc1

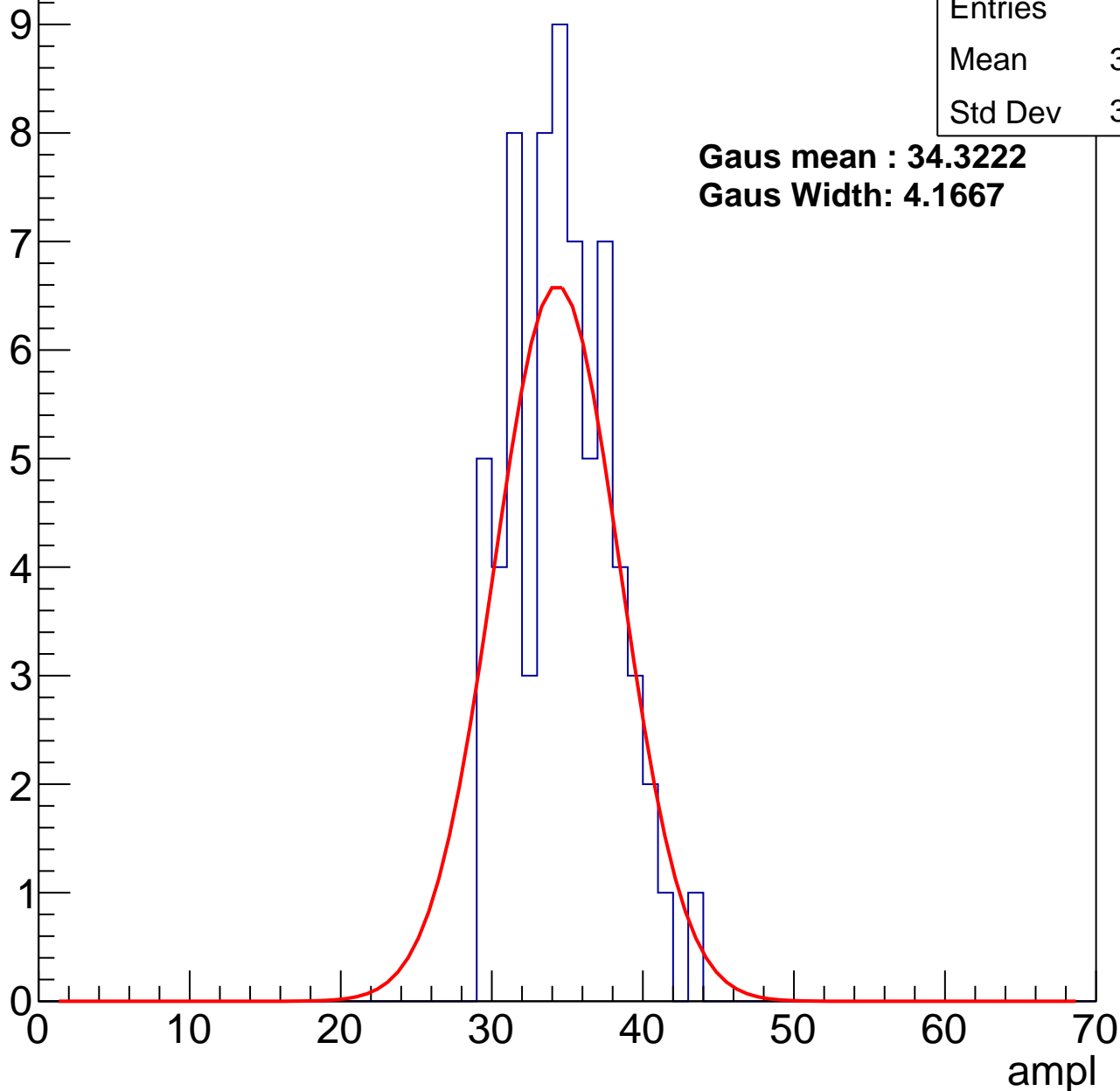
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	34.27
Std Dev	3.249

**Gaus mean : 34.3222**

**Gaus Width: 4.1667**



# B1L103S, U1-ch109, adc2

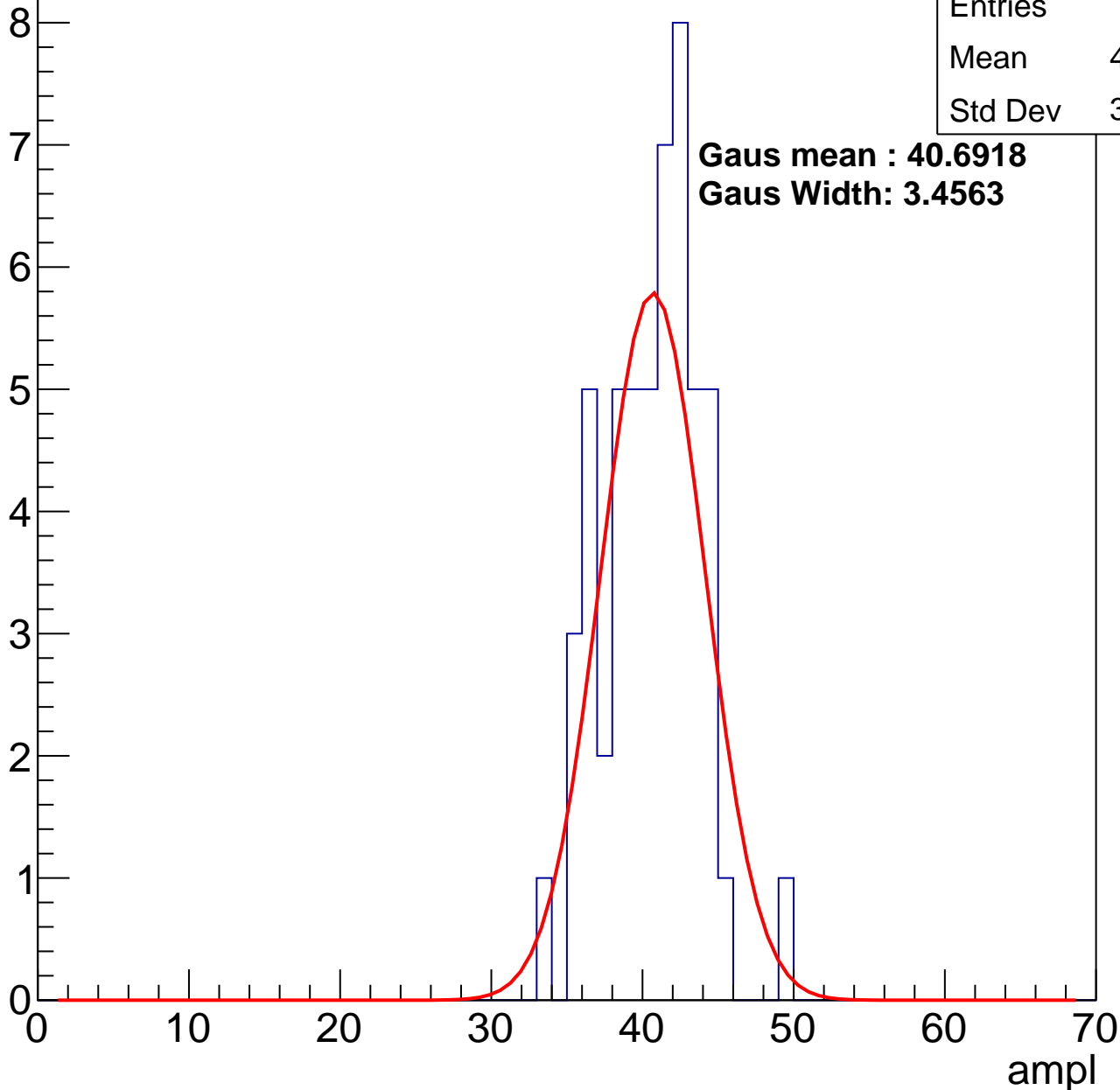
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	40.17
Std Dev	3.119

**Gaus mean : 40.6918**

**Gaus Width: 3.4563**

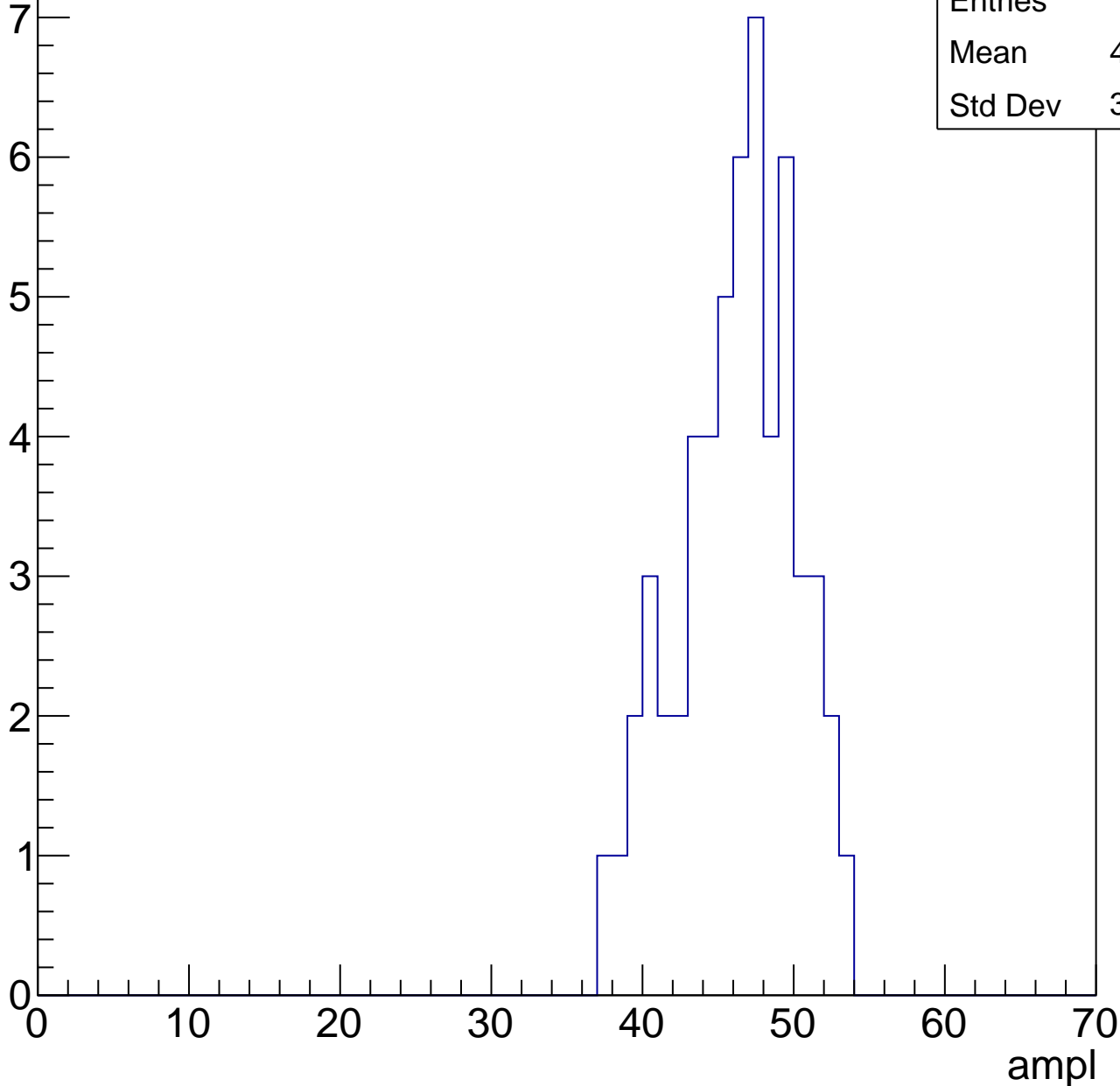


# B1L103S, U1-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	45.77
Std Dev	3.798

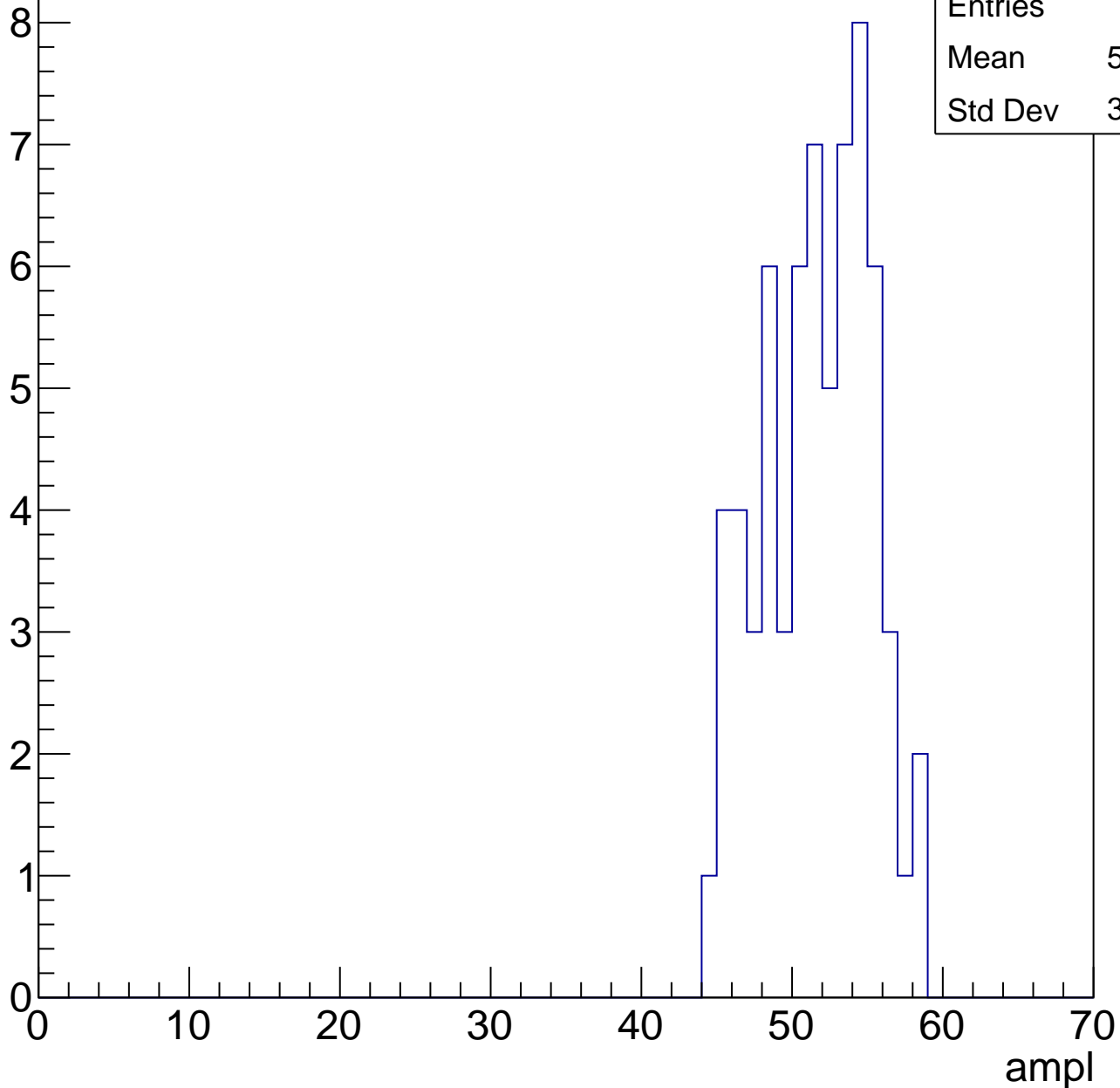


# B1L103S, U1-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	51.14
Std Dev	3.529

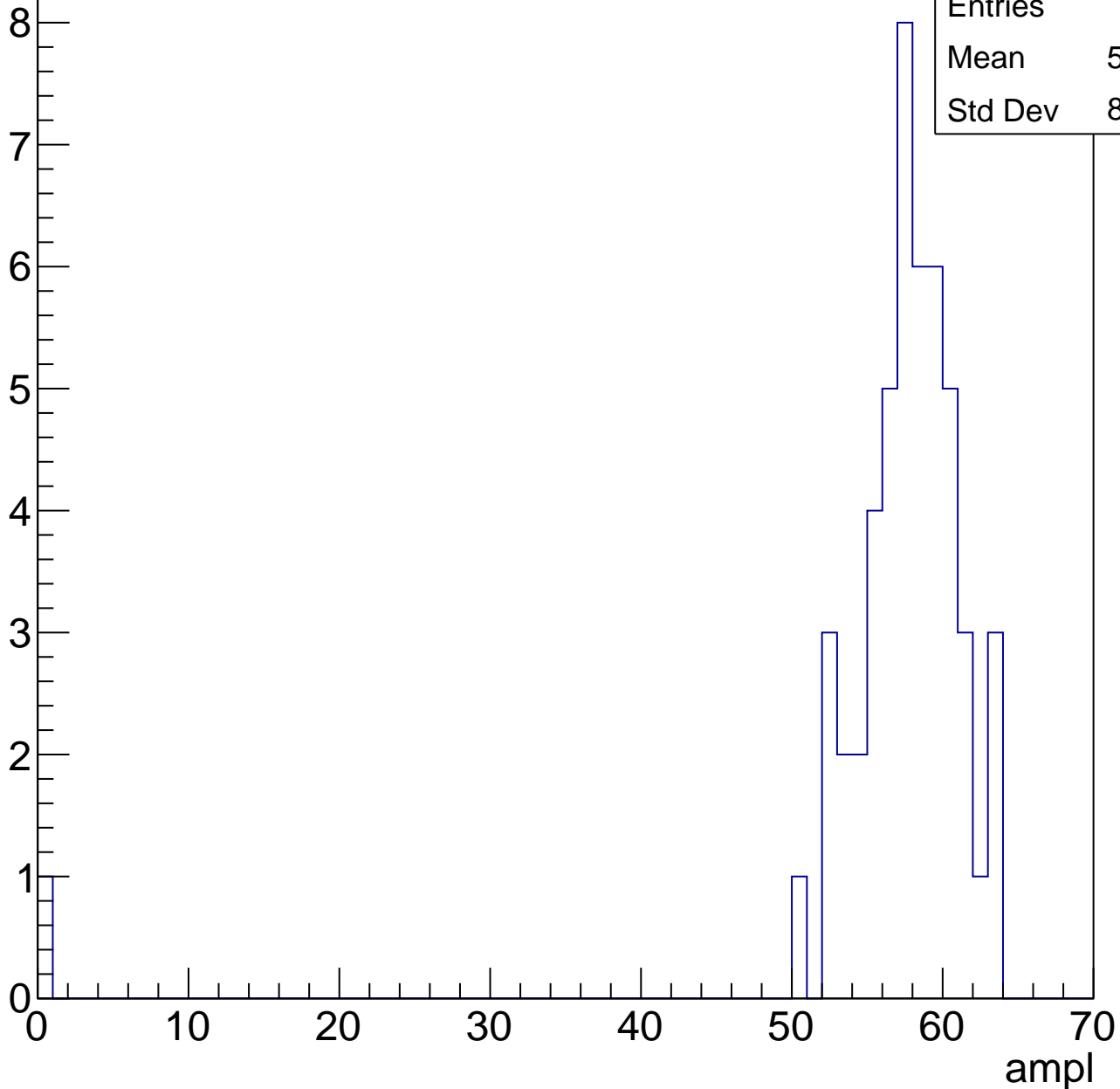


# B1L103S, U1-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	56.24
Std Dev	8.569

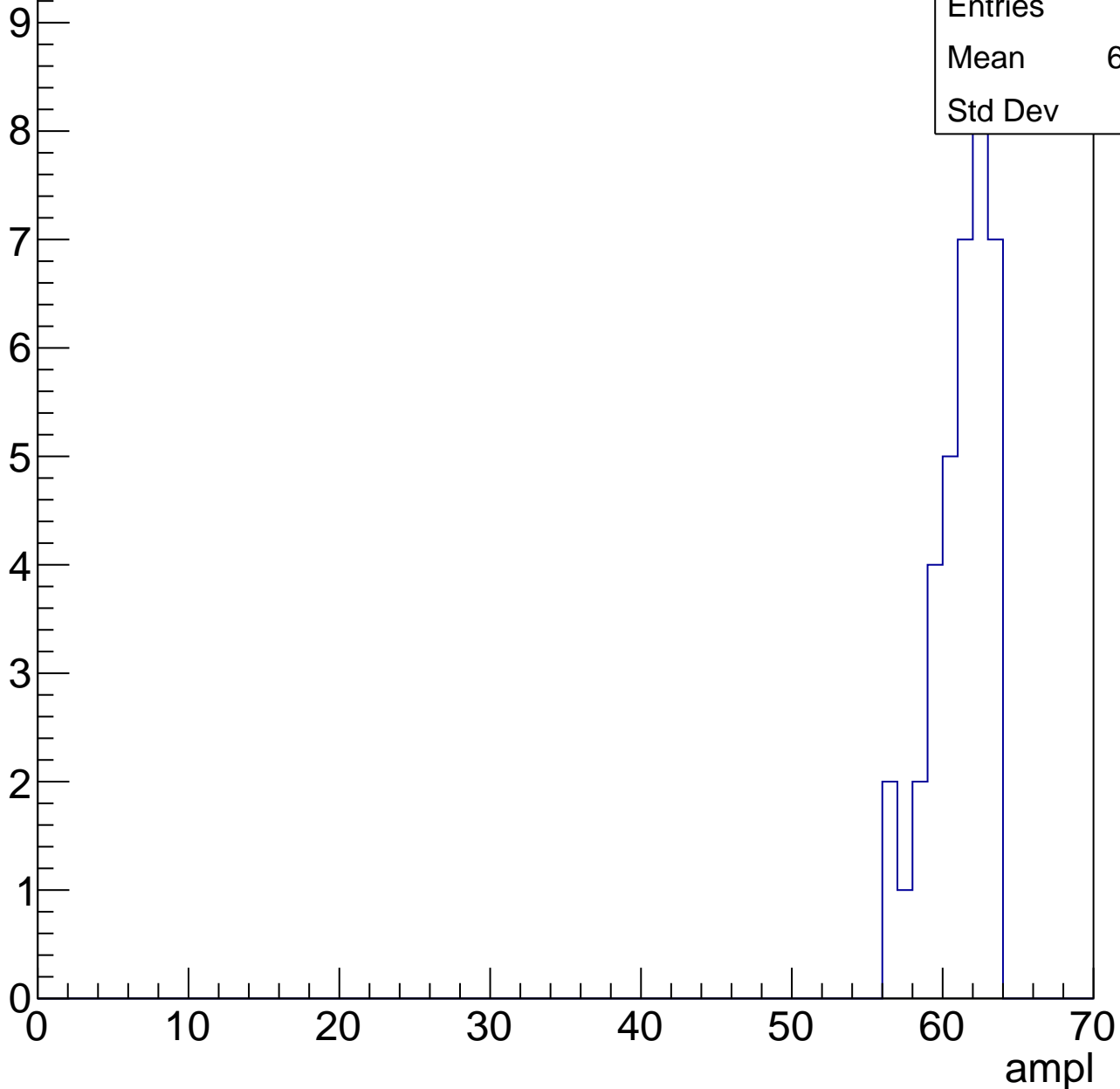


# B1L103S, U1-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	37
Mean	60.73
Std Dev	1.94





# B1L103S, U1-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U1-ch110, adc0

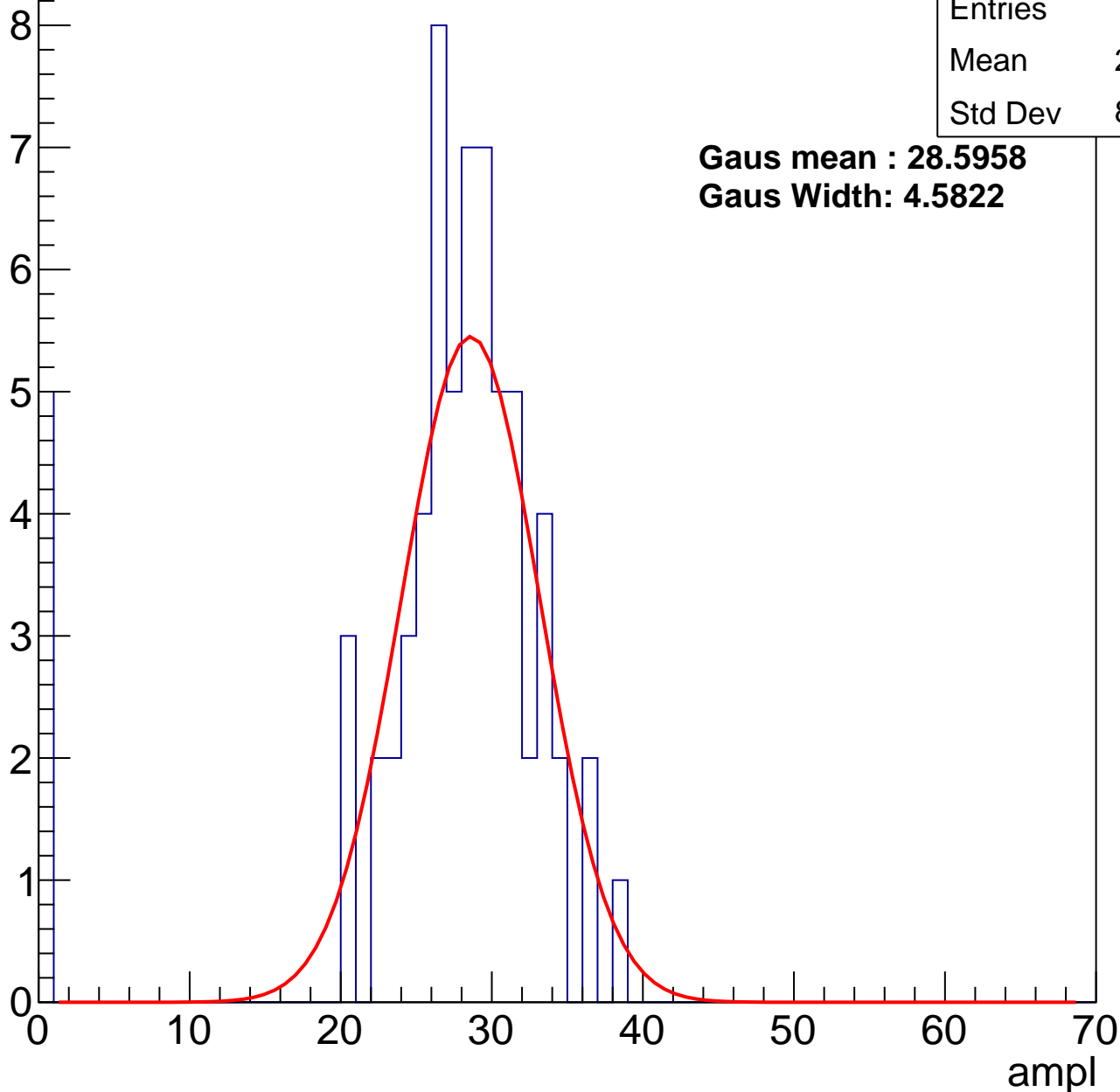
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	26.01
Std Dev	8.281

**Gaus mean : 28.5958**

**Gaus Width: 4.5822**



# B1L103S, U1-ch110, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	68
Mean	34.75
Std Dev	3.558

**Gaus mean : 34.7263**

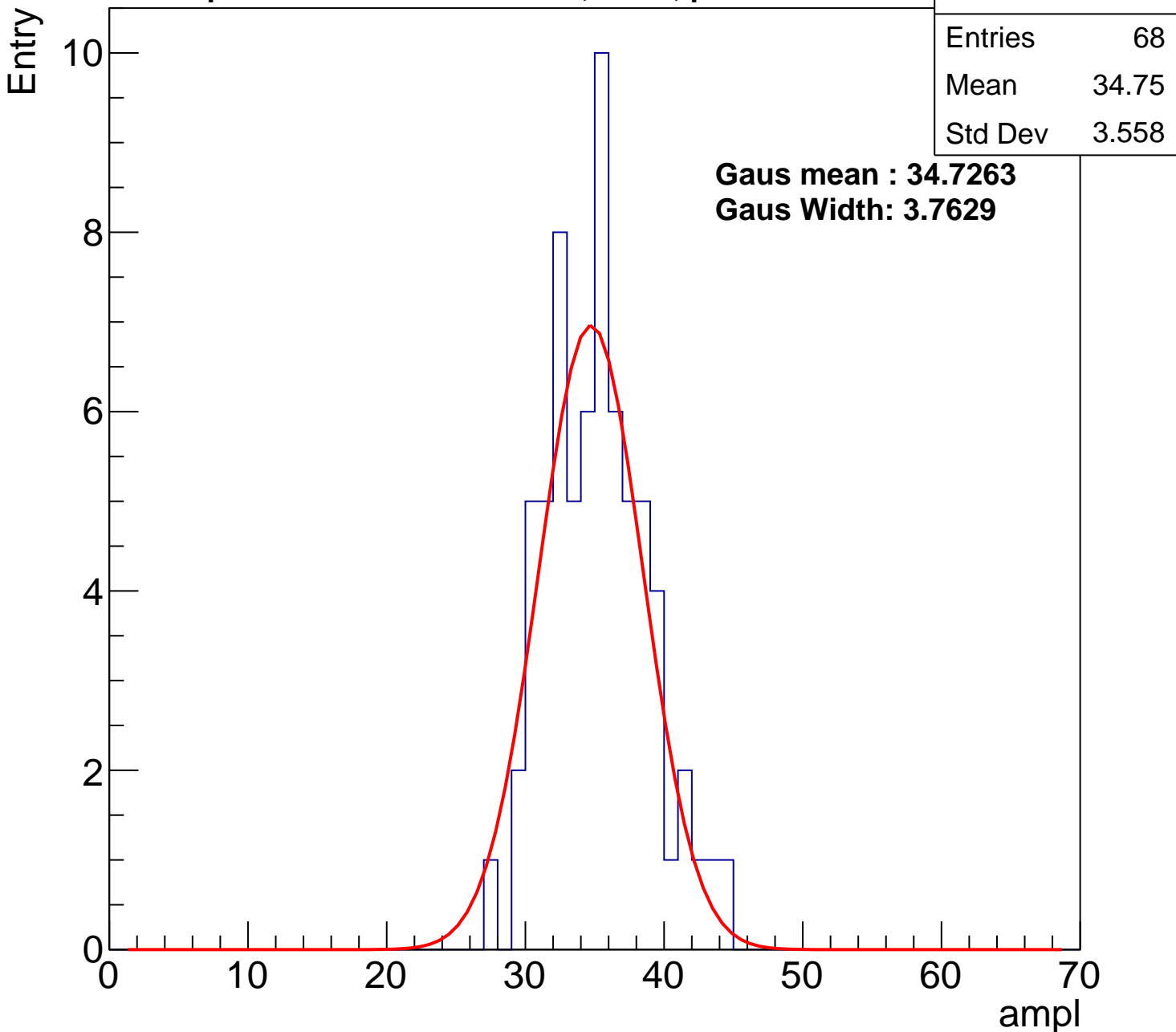
**Gaus Width: 3.7629**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U1-ch110, adc2

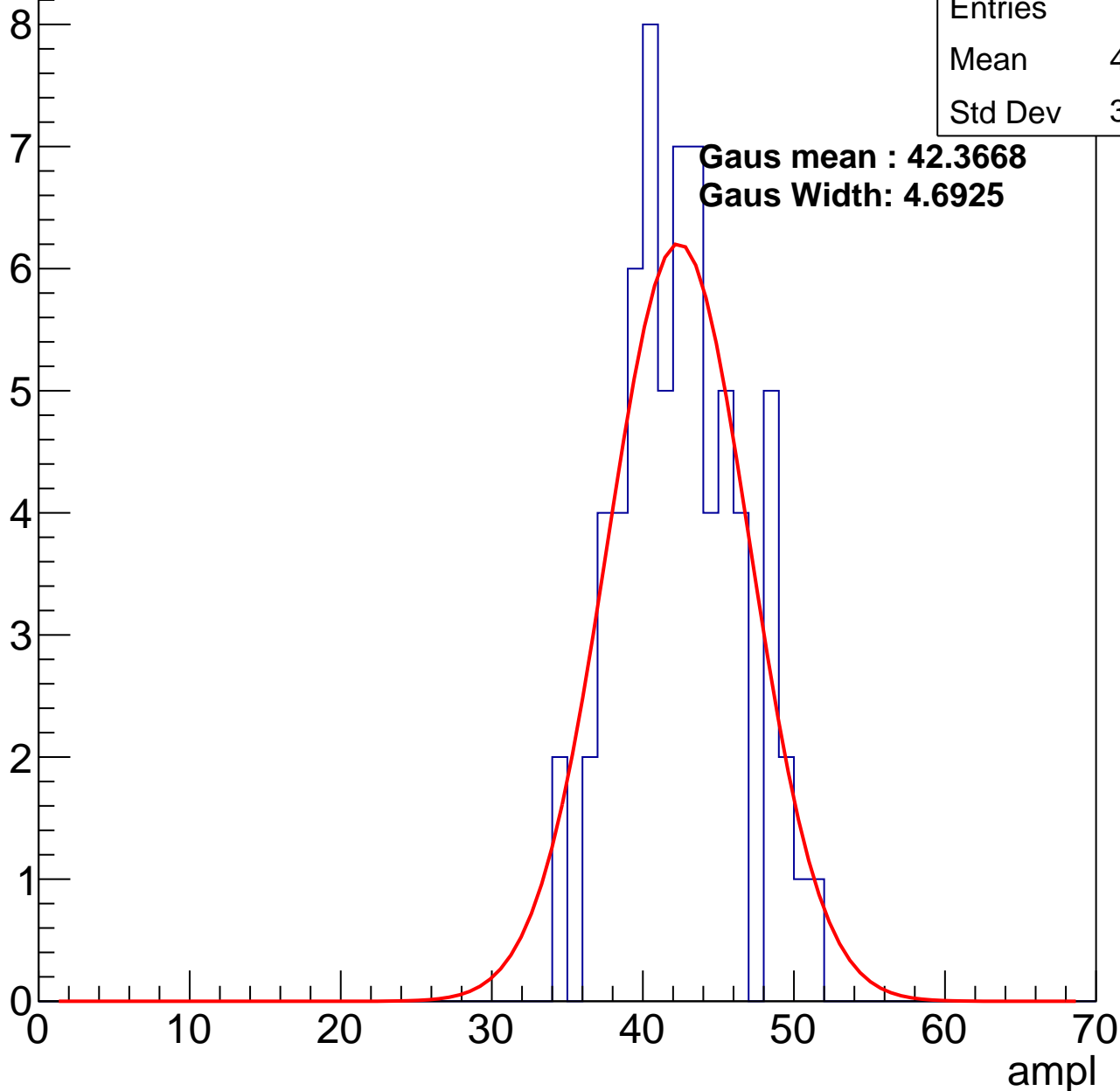
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	42.06
Std Dev	3.882

**Gaus mean : 42.3668**

**Gaus Width: 4.6925**

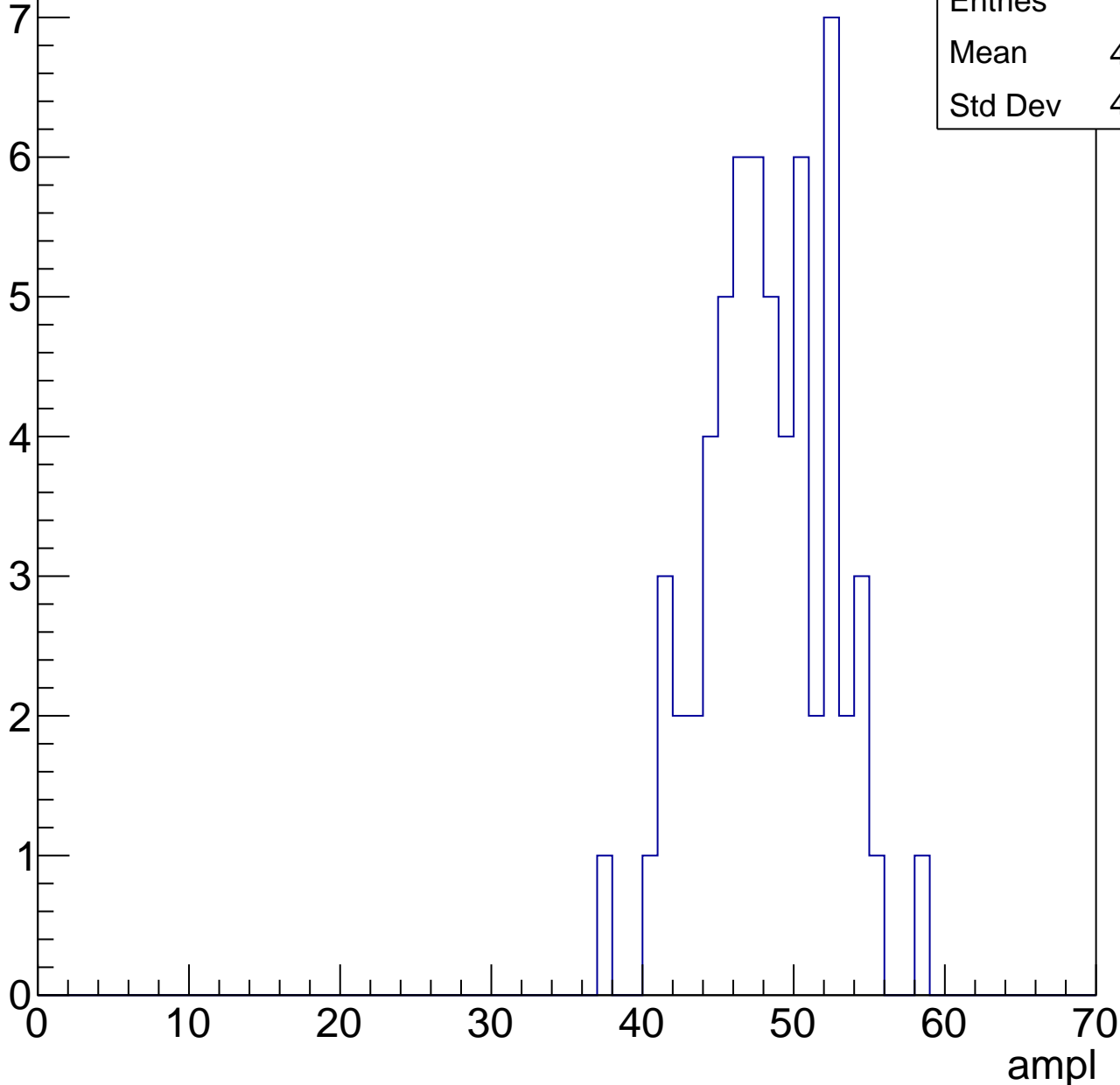


# B1L103S, U1-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	47.74
Std Dev	4.156

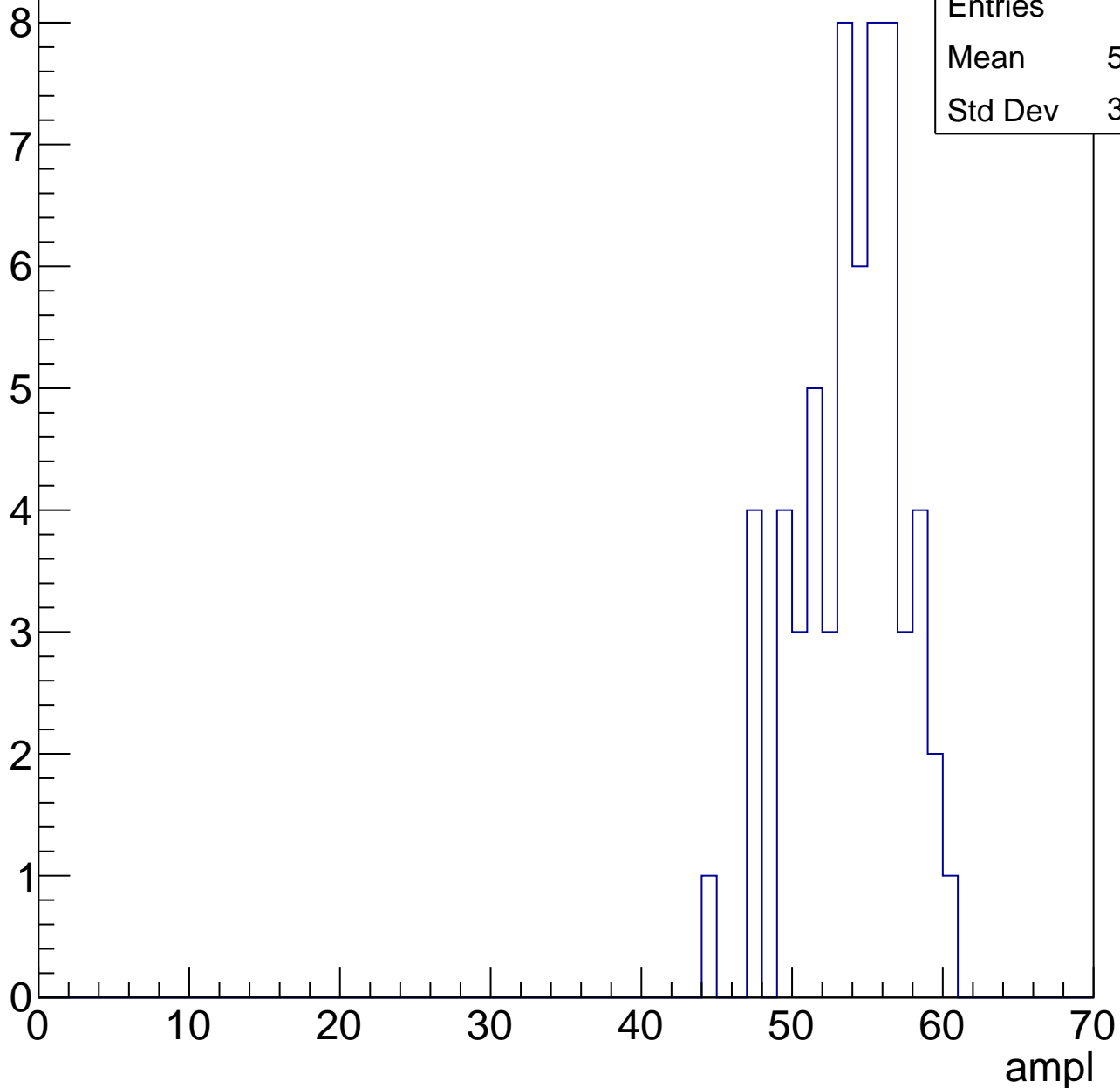


# B1L103S, U1-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	53.43
Std Dev	3.432

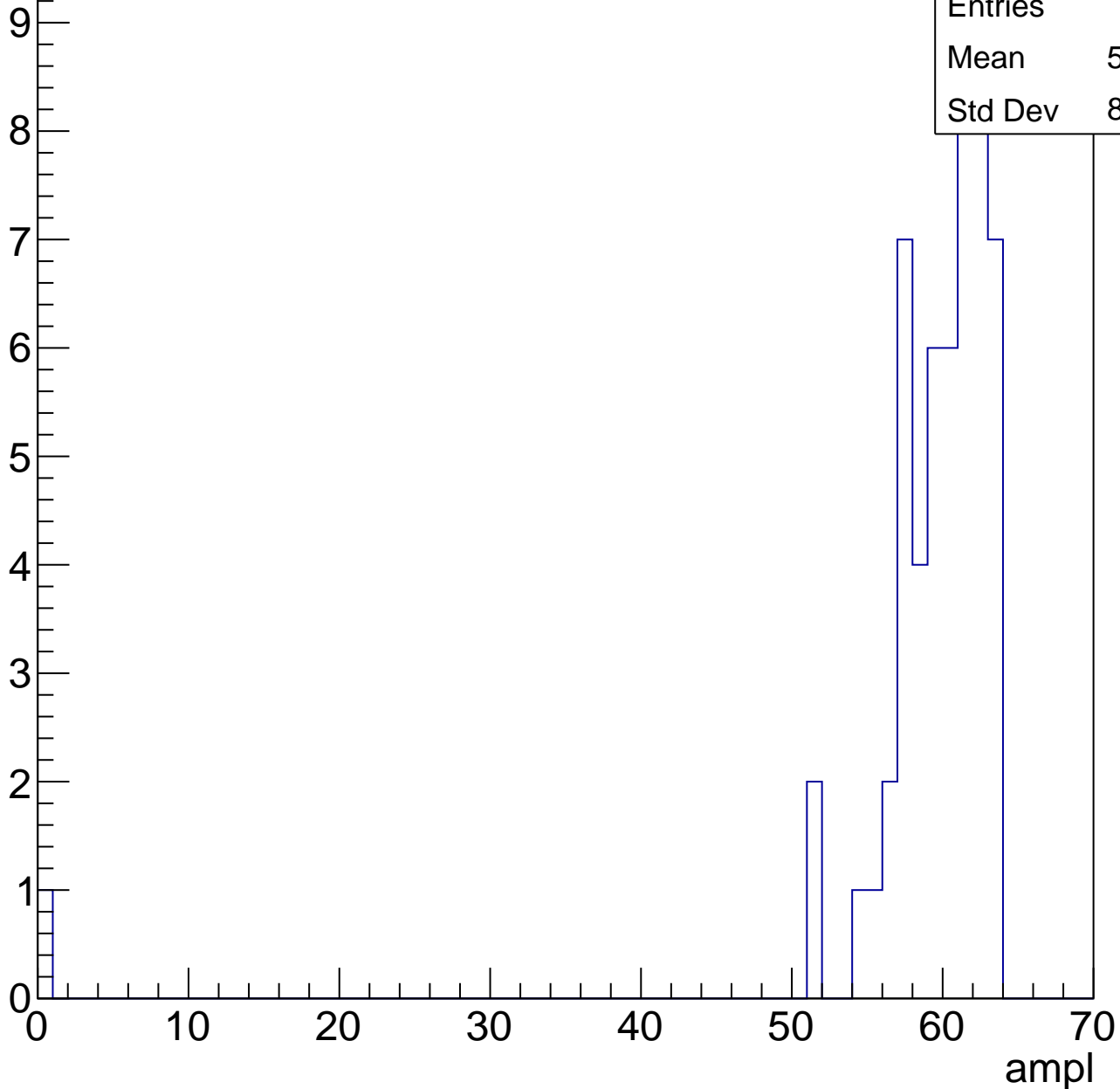


# B1L103S, U1-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	58.43
Std Dev	8.513



# B1L103S, U1-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries	11
Mean	60.64
Std Dev	1.666



# B1L103S, U1-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch111, adc0

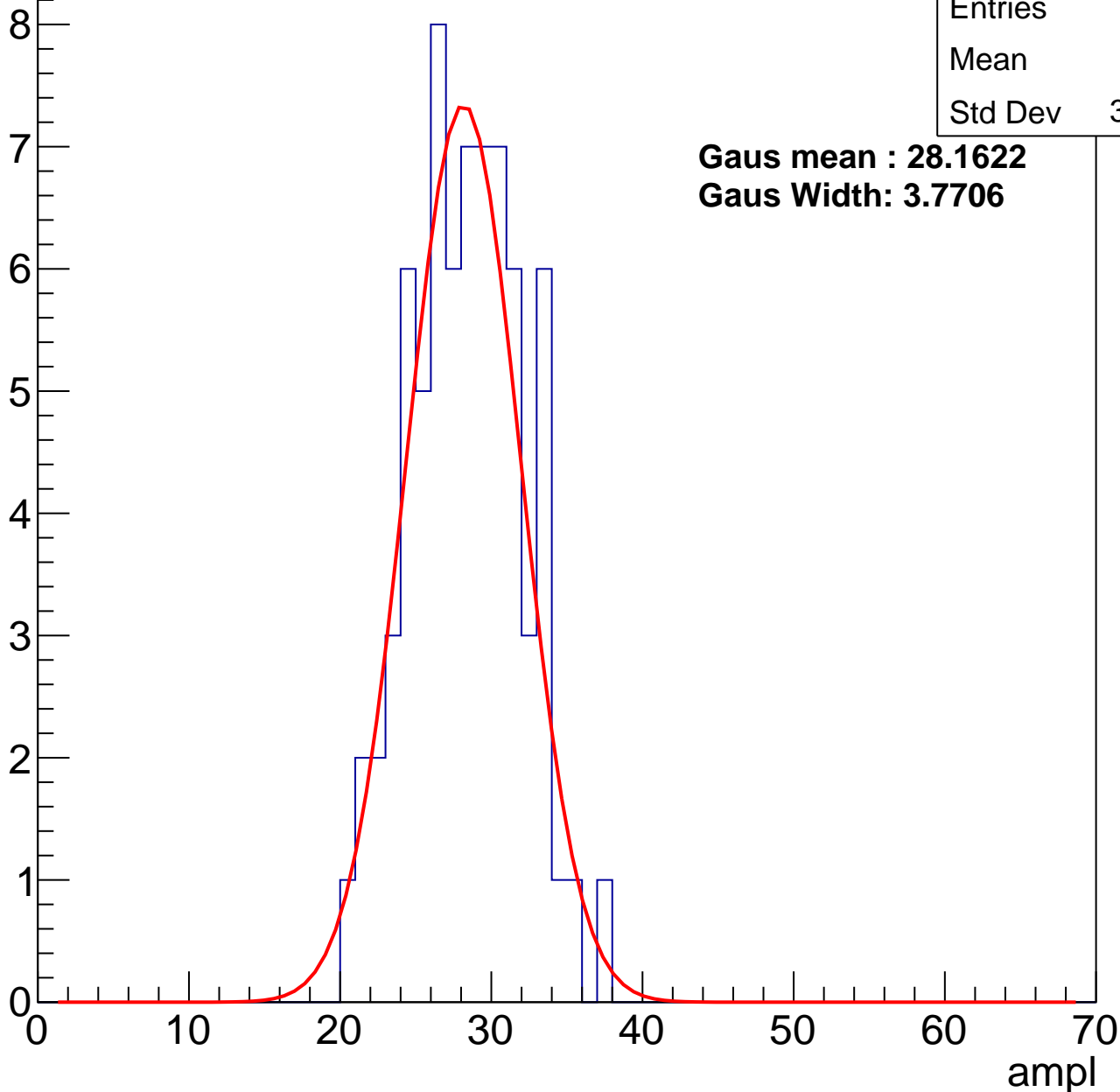
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	27.9
Std Dev	3.614

**Gaus mean : 28.1622**

**Gaus Width: 3.7706**



# B1L103S, U1-ch111, adc1

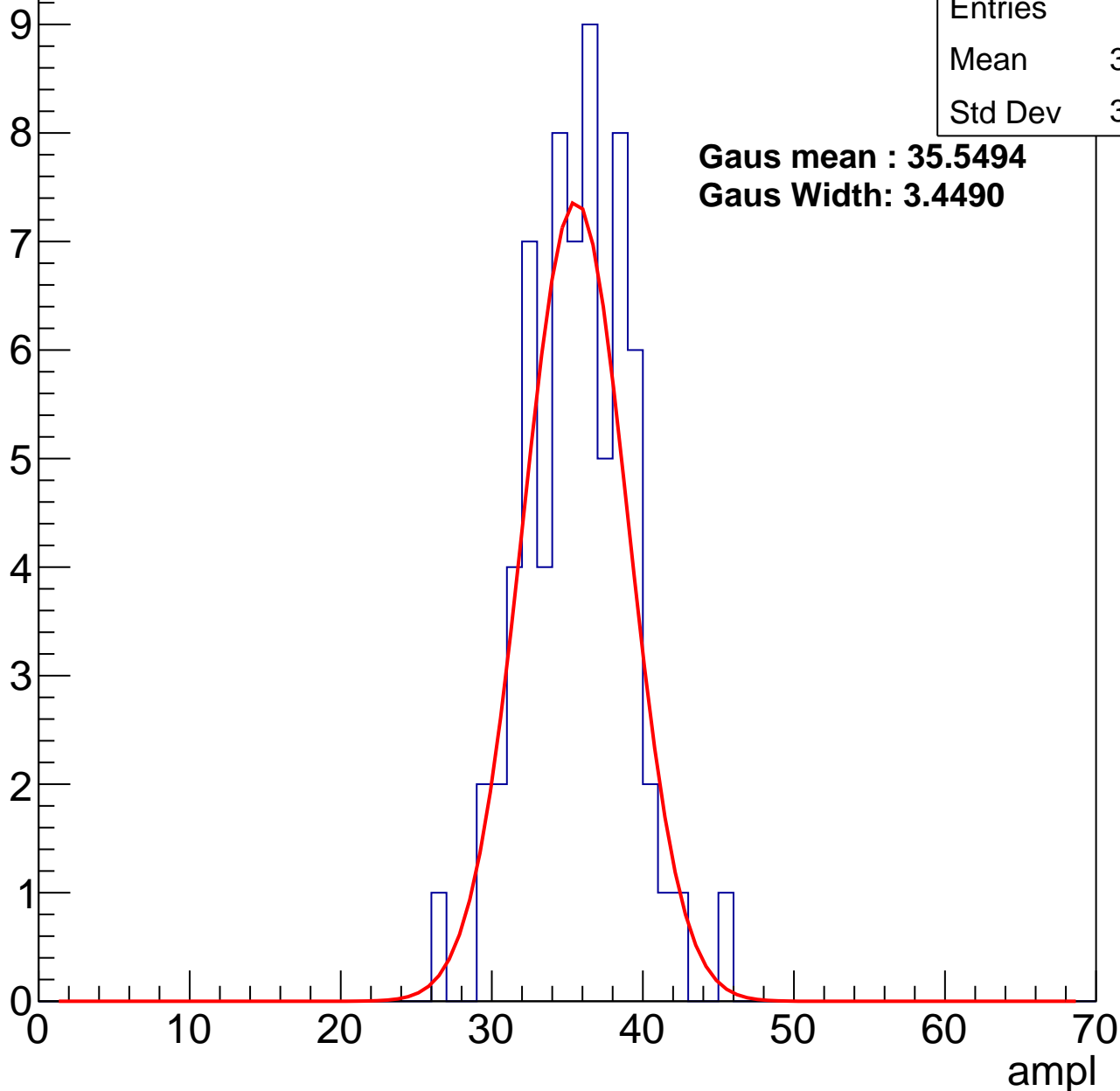
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	35.24
Std Dev	3.392

**Gaus mean : 35.5494**

**Gaus Width: 3.4490**



# B1L103S, U1-ch111, adc2

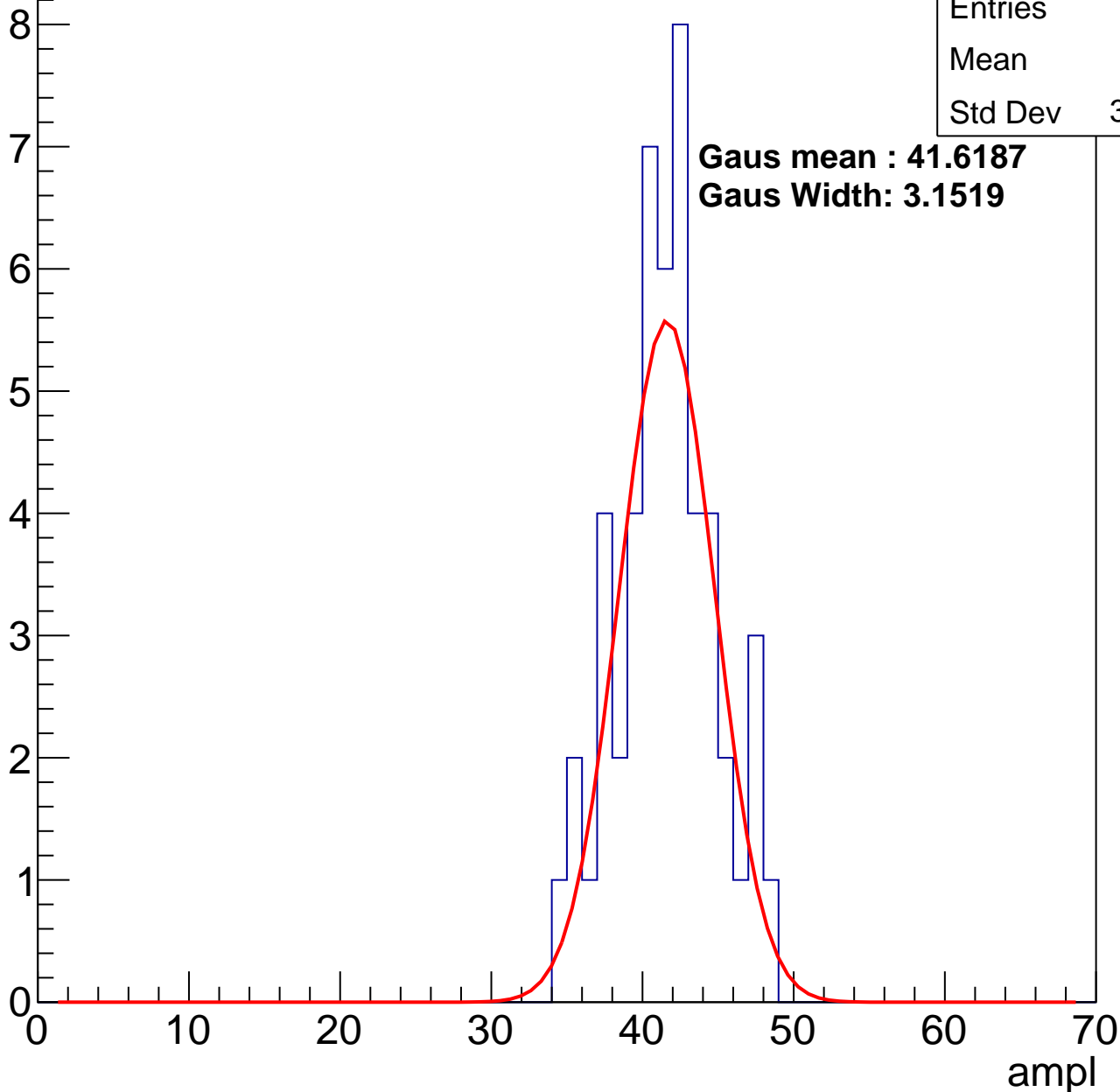
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	41.1
Std Dev	3.239

**Gaus mean : 41.6187**

**Gaus Width: 3.1519**

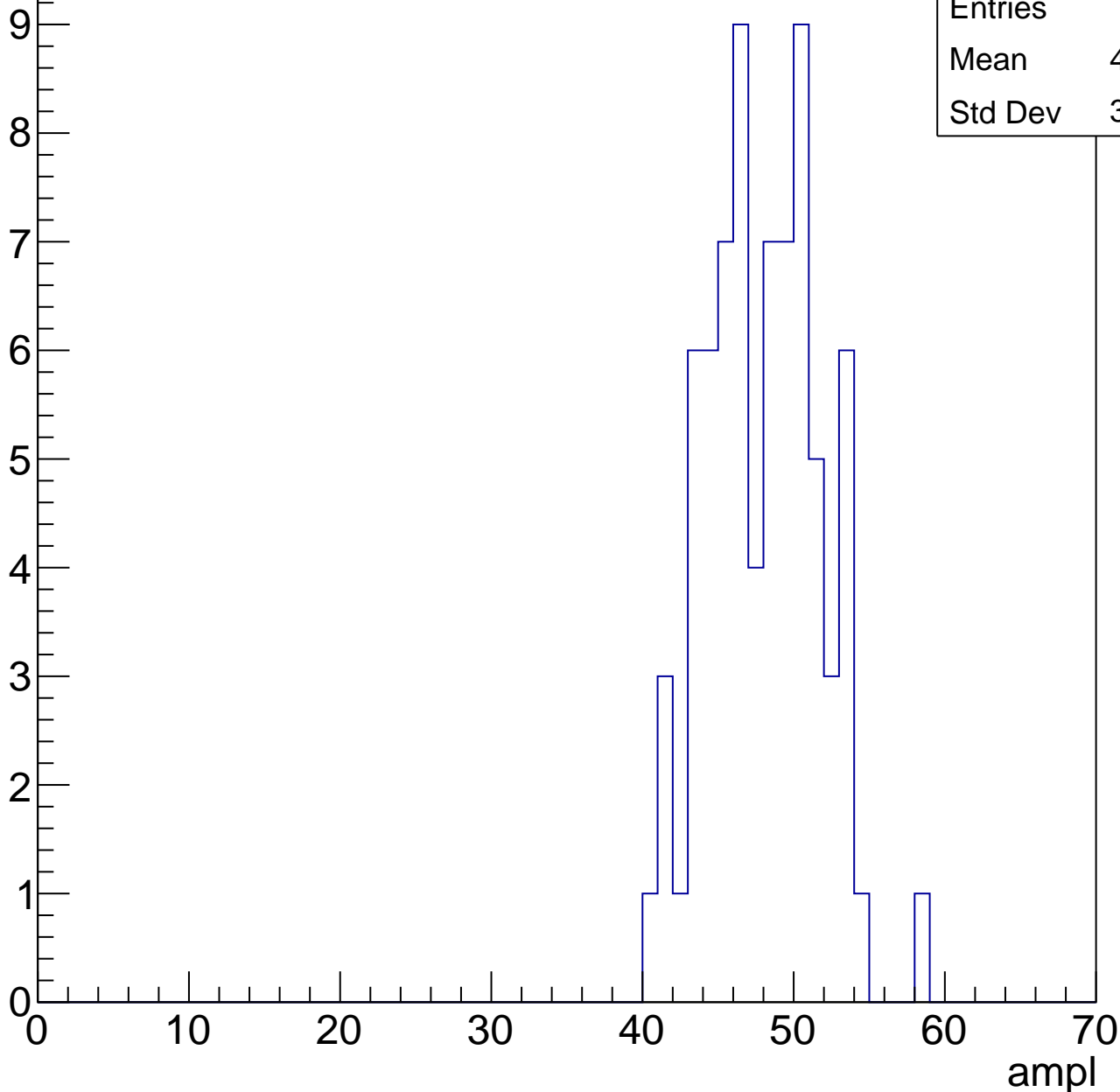


# B1L103S, U1-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	47.55
Std Dev	3.632

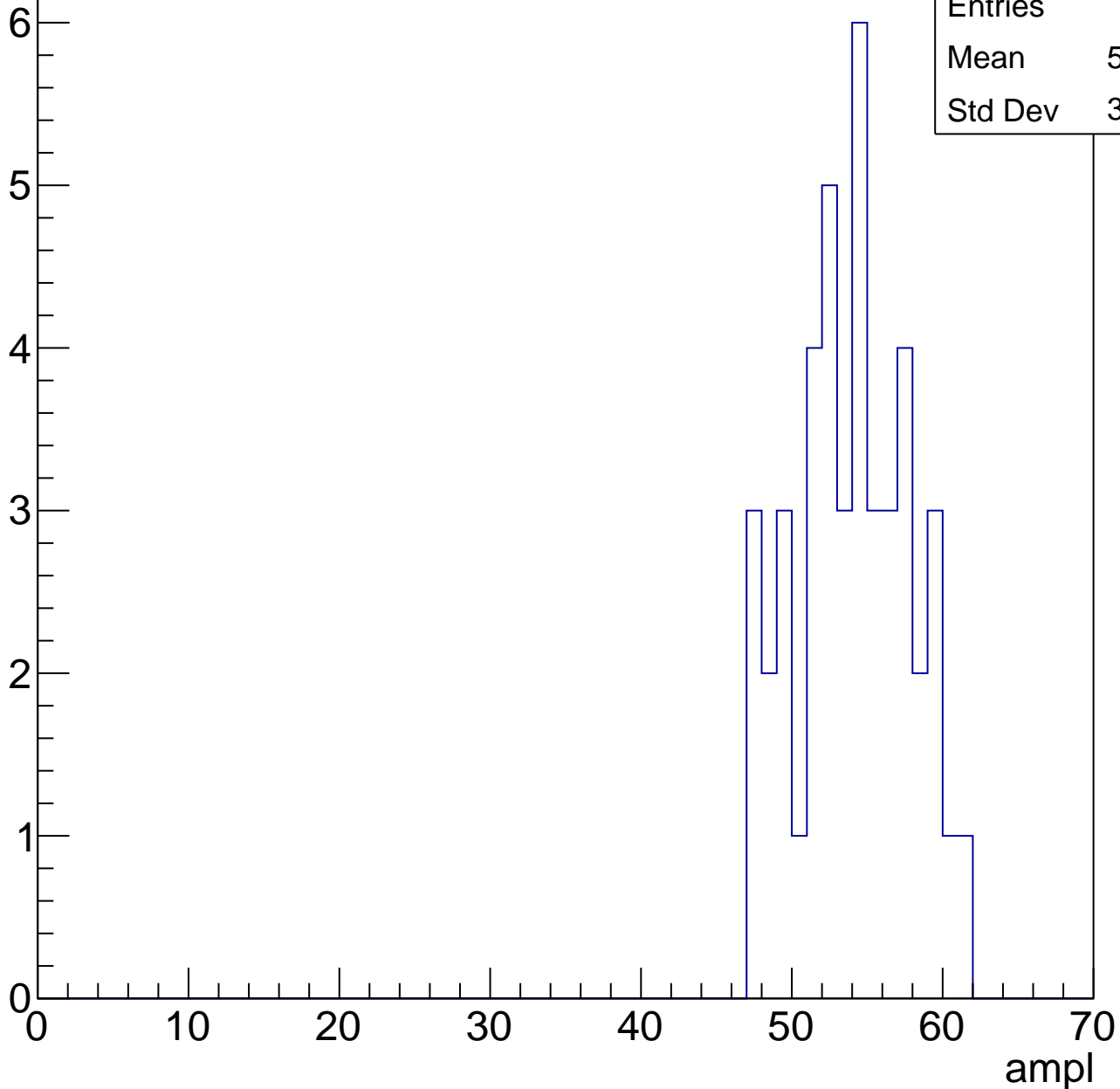


# B1L103S, U1-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	53.55
Std Dev	3.702

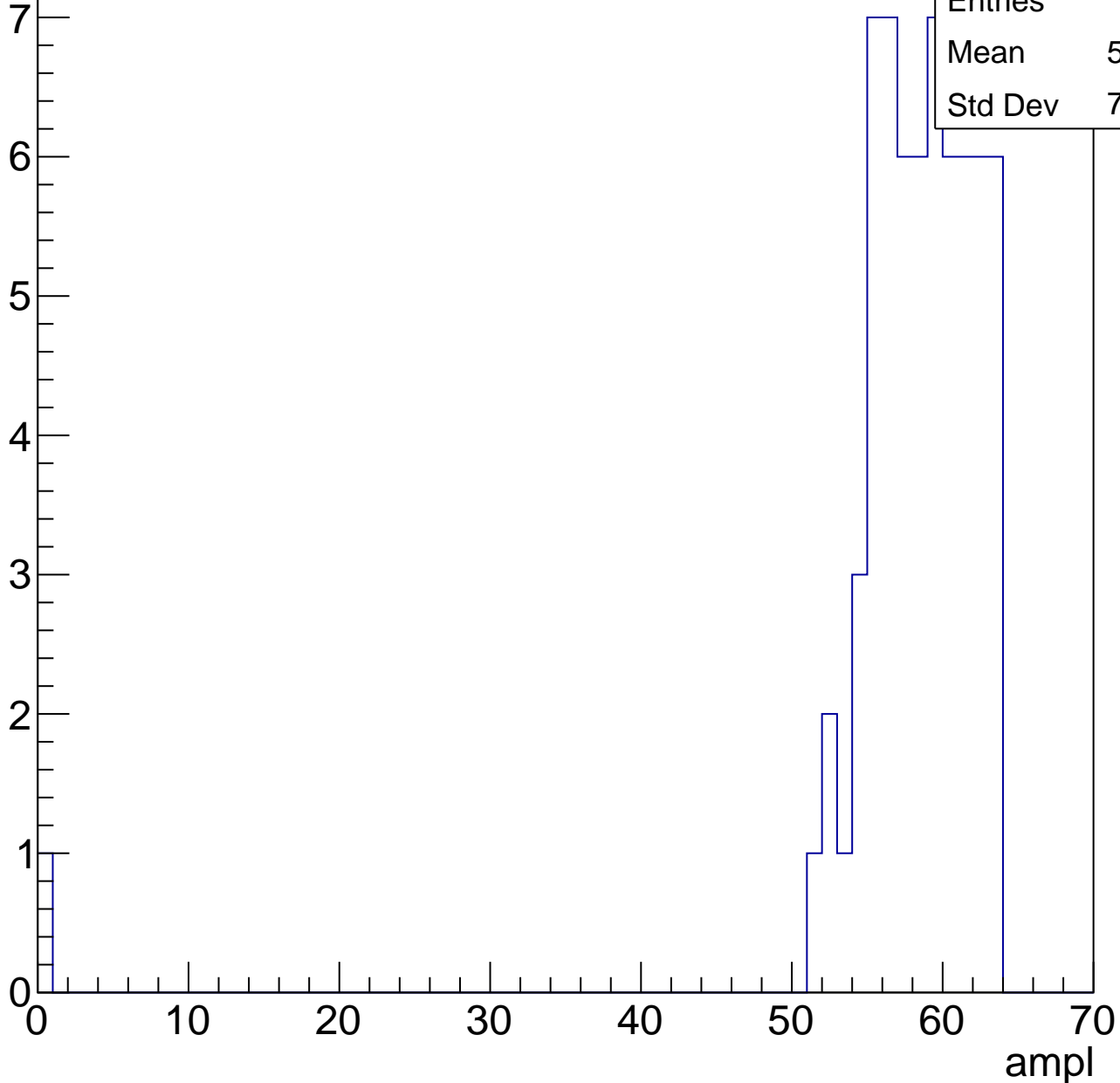


# B1L103S, U1-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

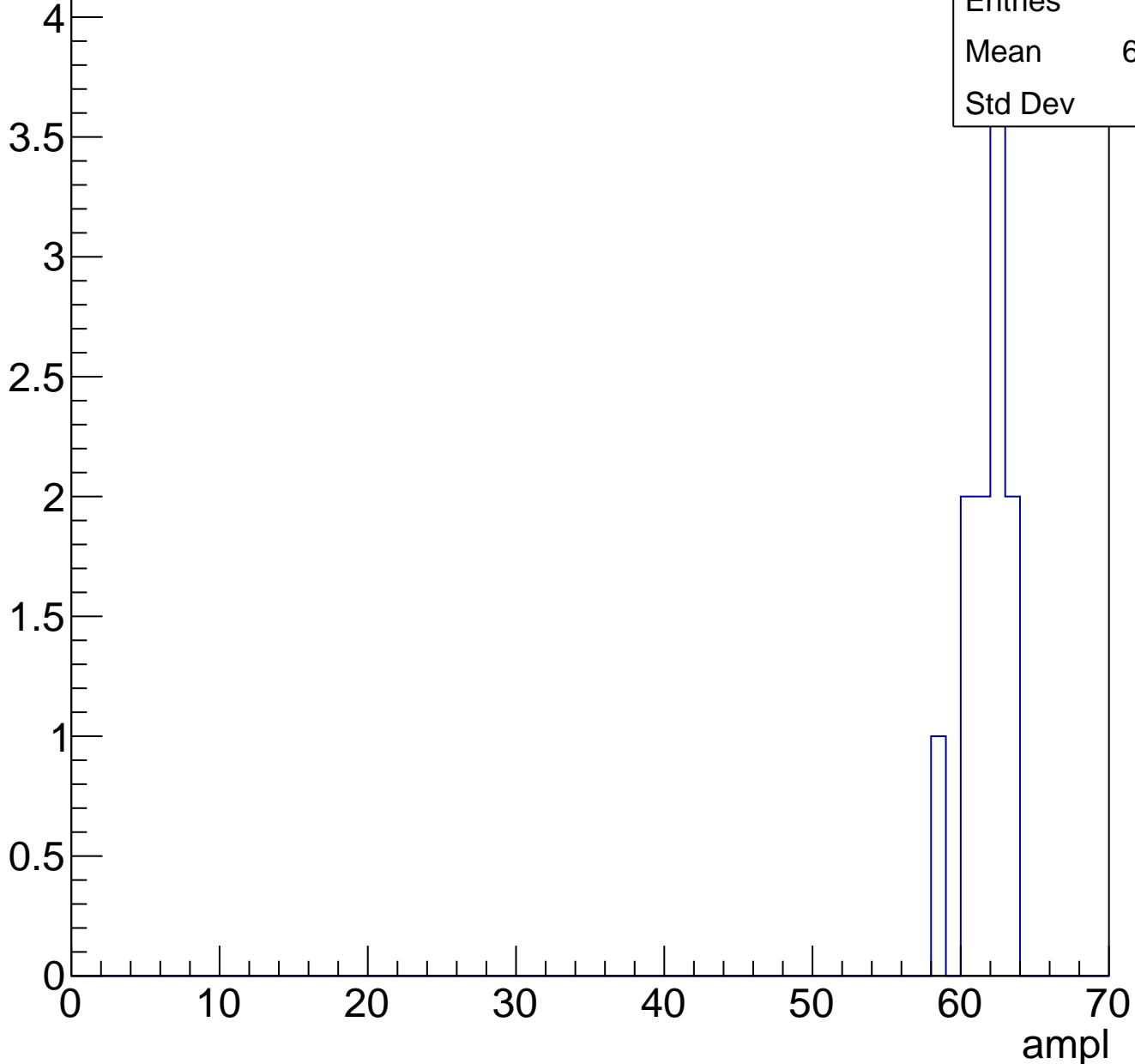
Entries	65
Mean	57.32
Std Dev	7.802



# B1L103S, U1-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

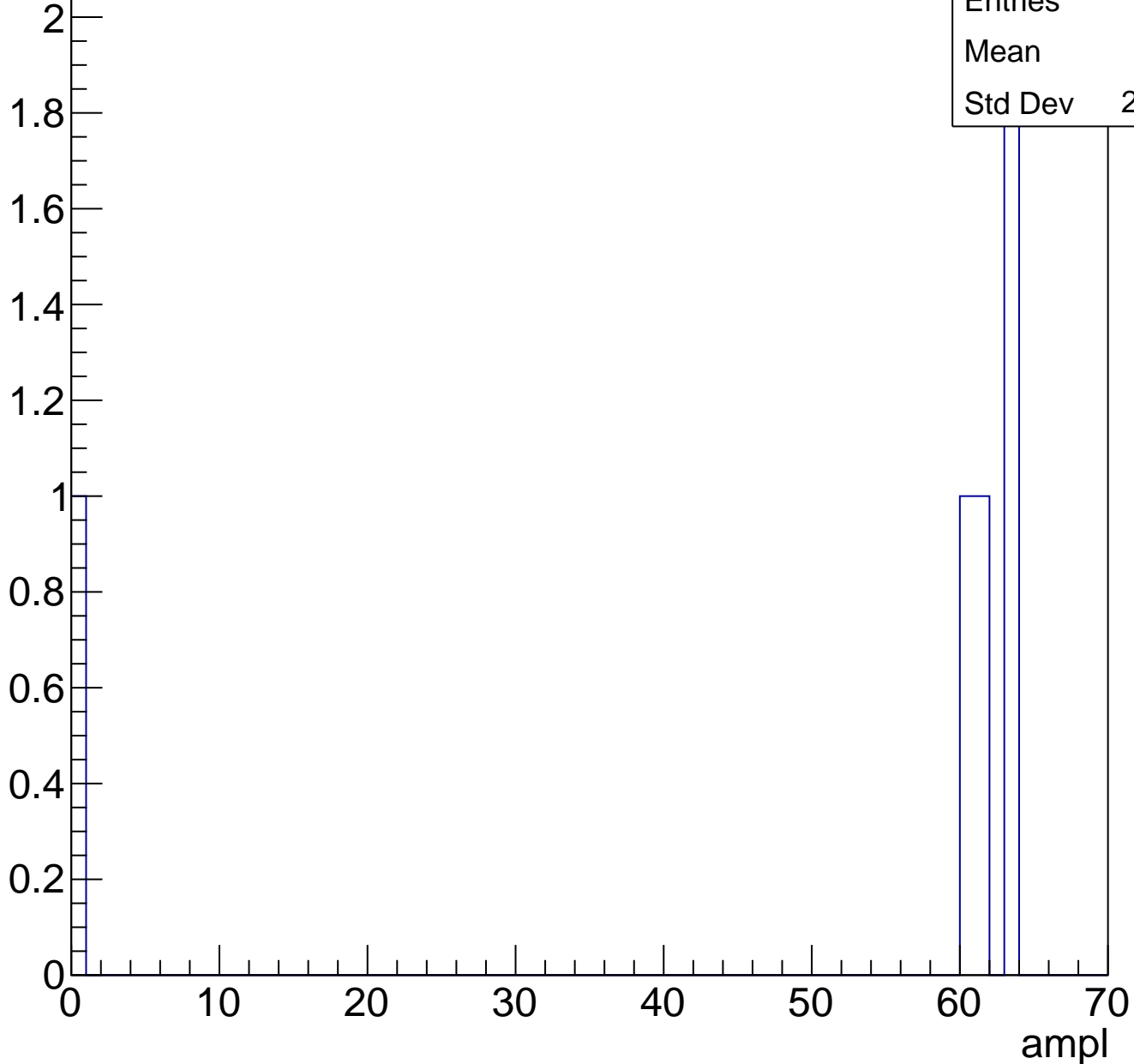




# B1L103S, U1-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch112, adc0

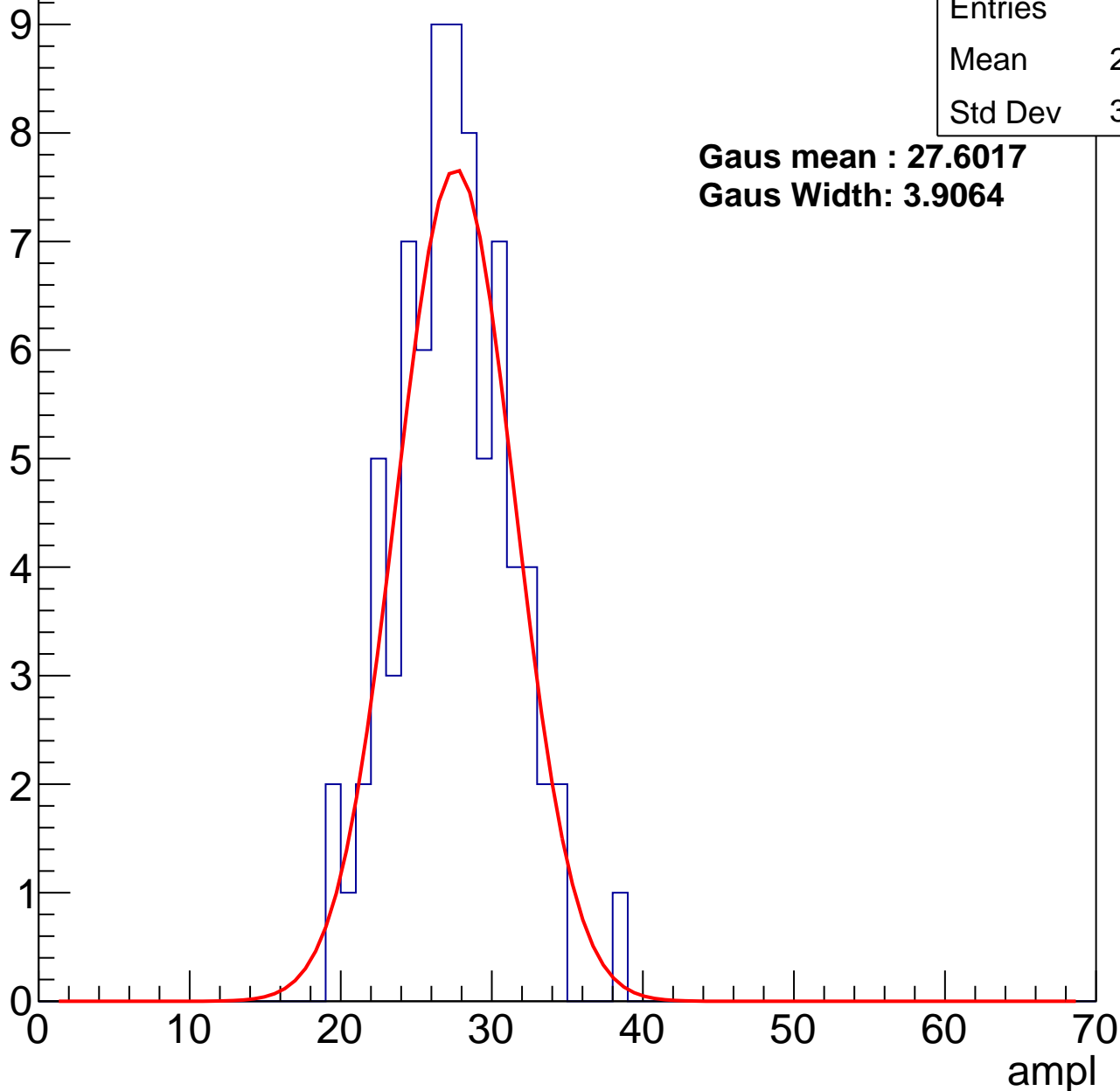
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	26.97
Std Dev	3.717

**Gaus mean : 27.6017**

**Gaus Width: 3.9064**



# B1L103S, U1-ch112, adc1

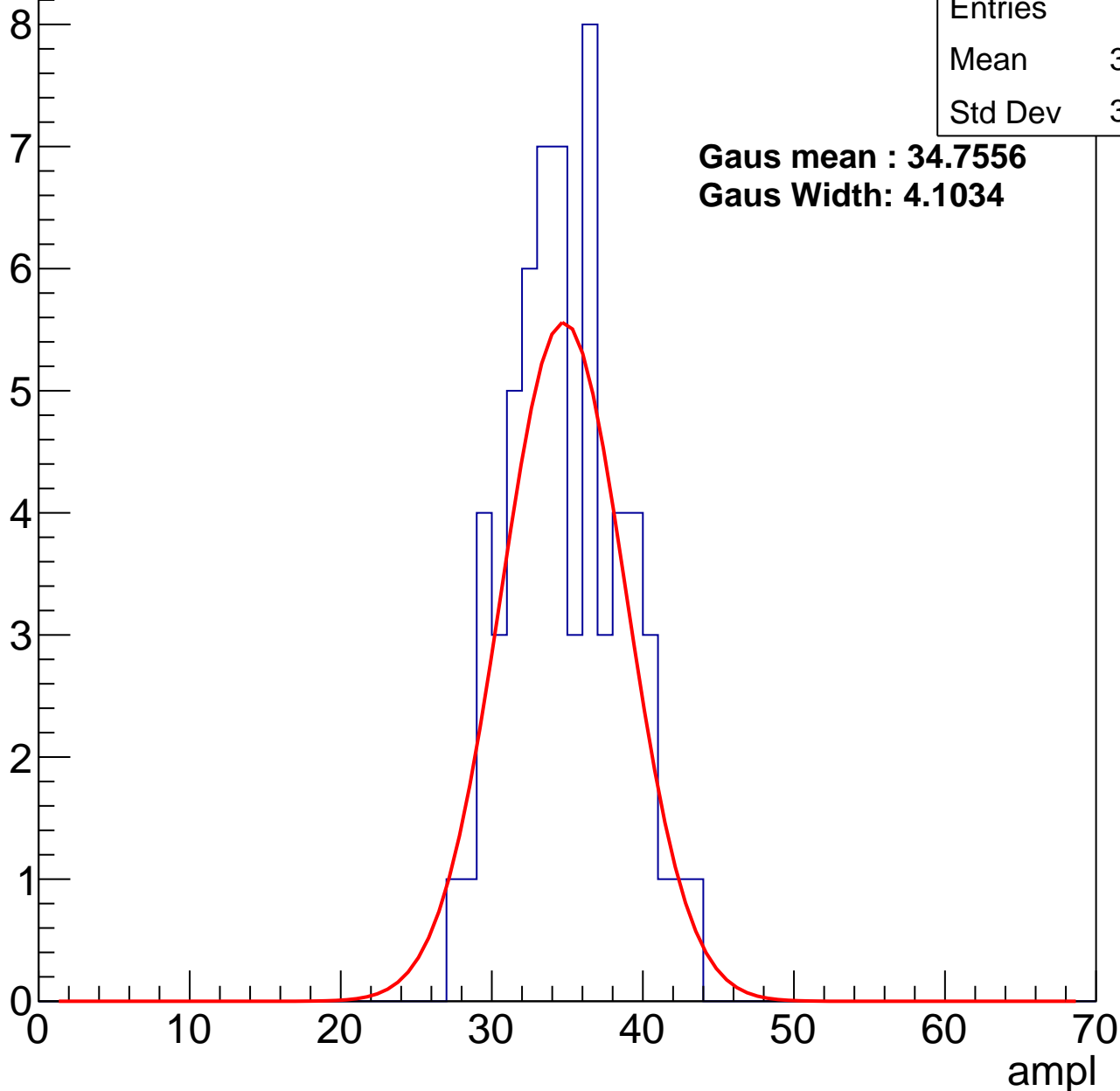
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	34.44
Std Dev	3.648

**Gaus mean : 34.7556**

**Gaus Width: 4.1034**



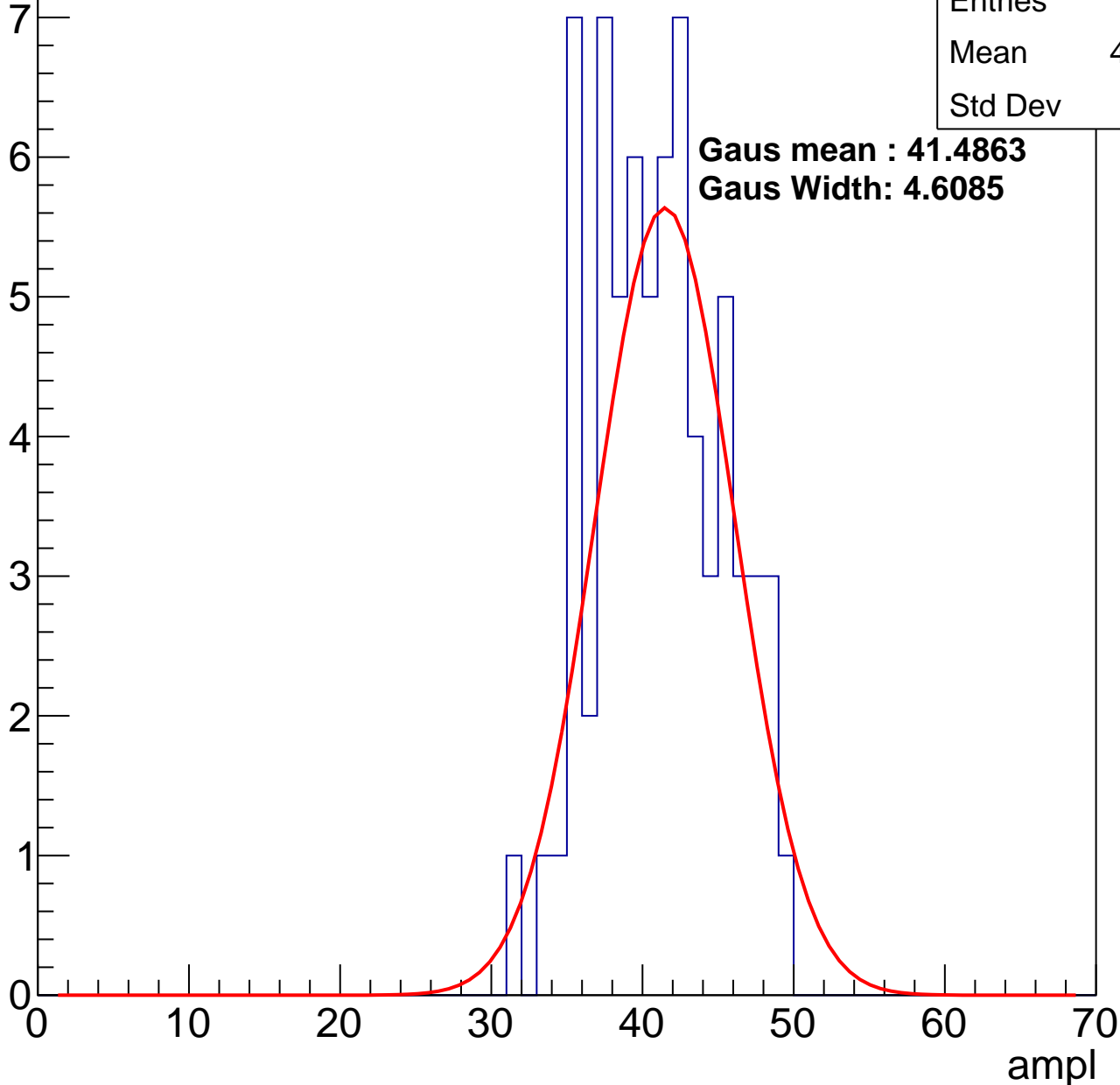
# B1L103S, U1-ch112, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	40.56
Std Dev	4.16

**Gaus mean : 41.4863**  
**Gaus Width: 4.6085**

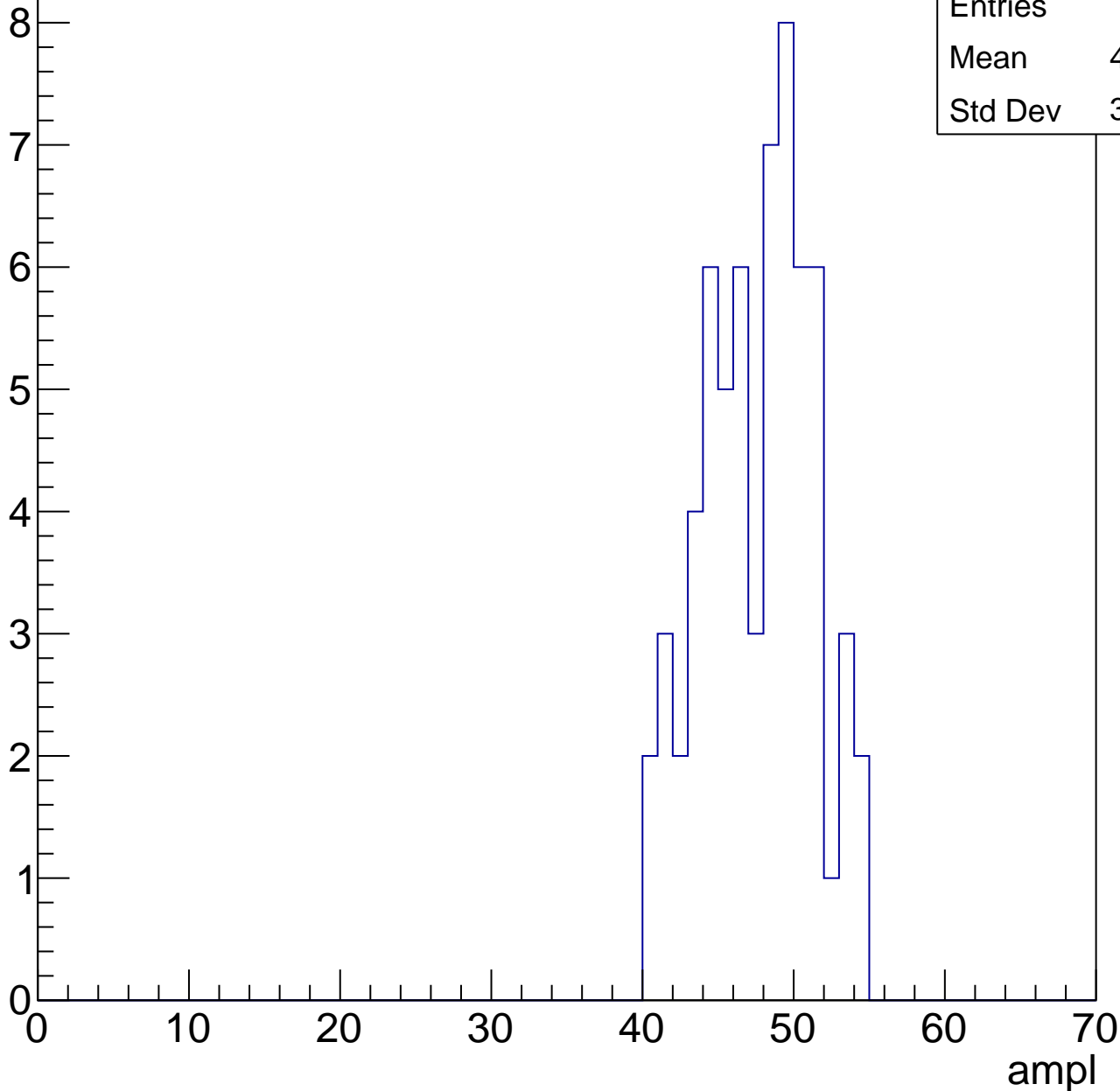


# B1L103S, U1-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	47.16
Std Dev	3.576

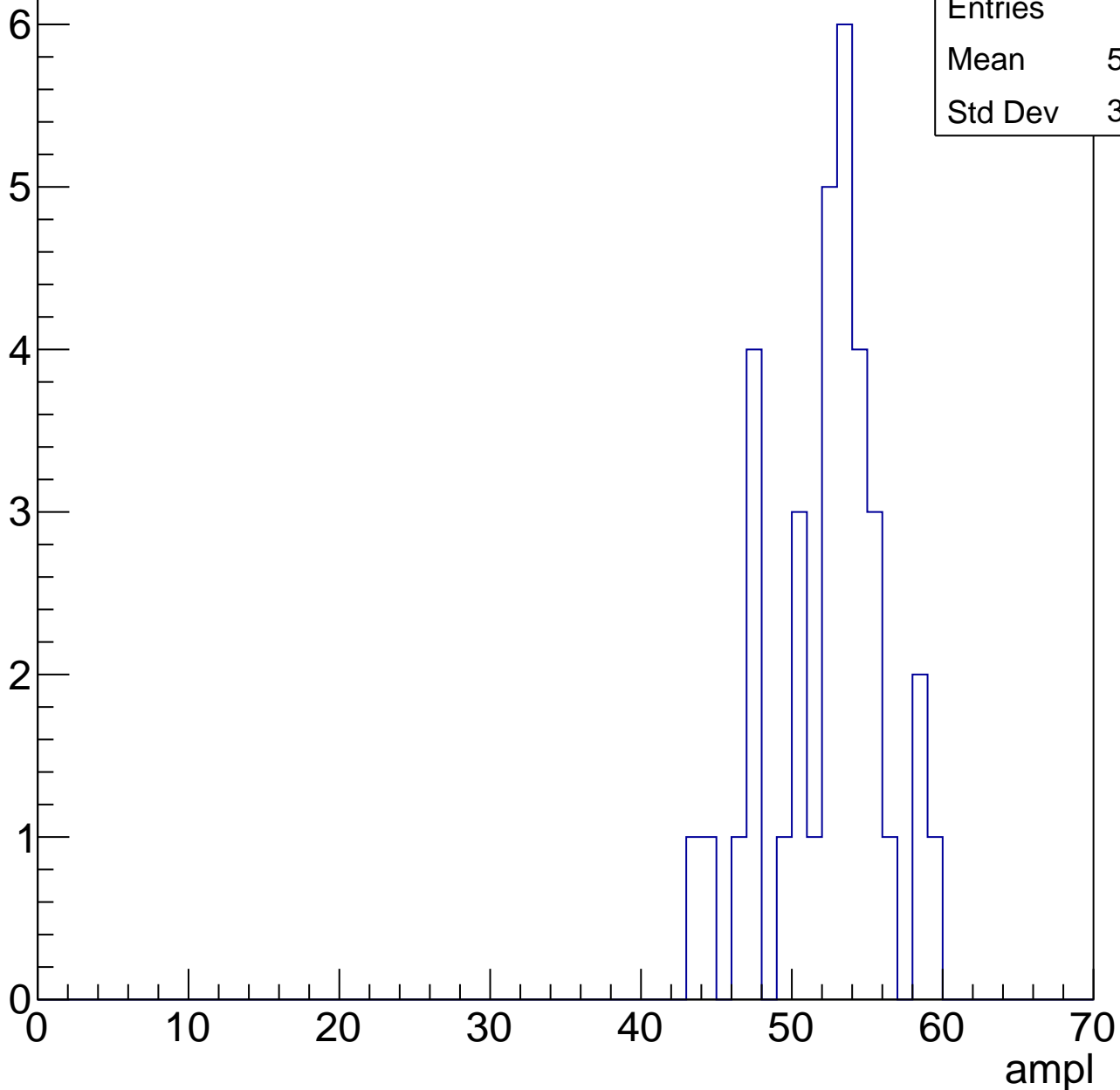


# B1L103S, U1-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

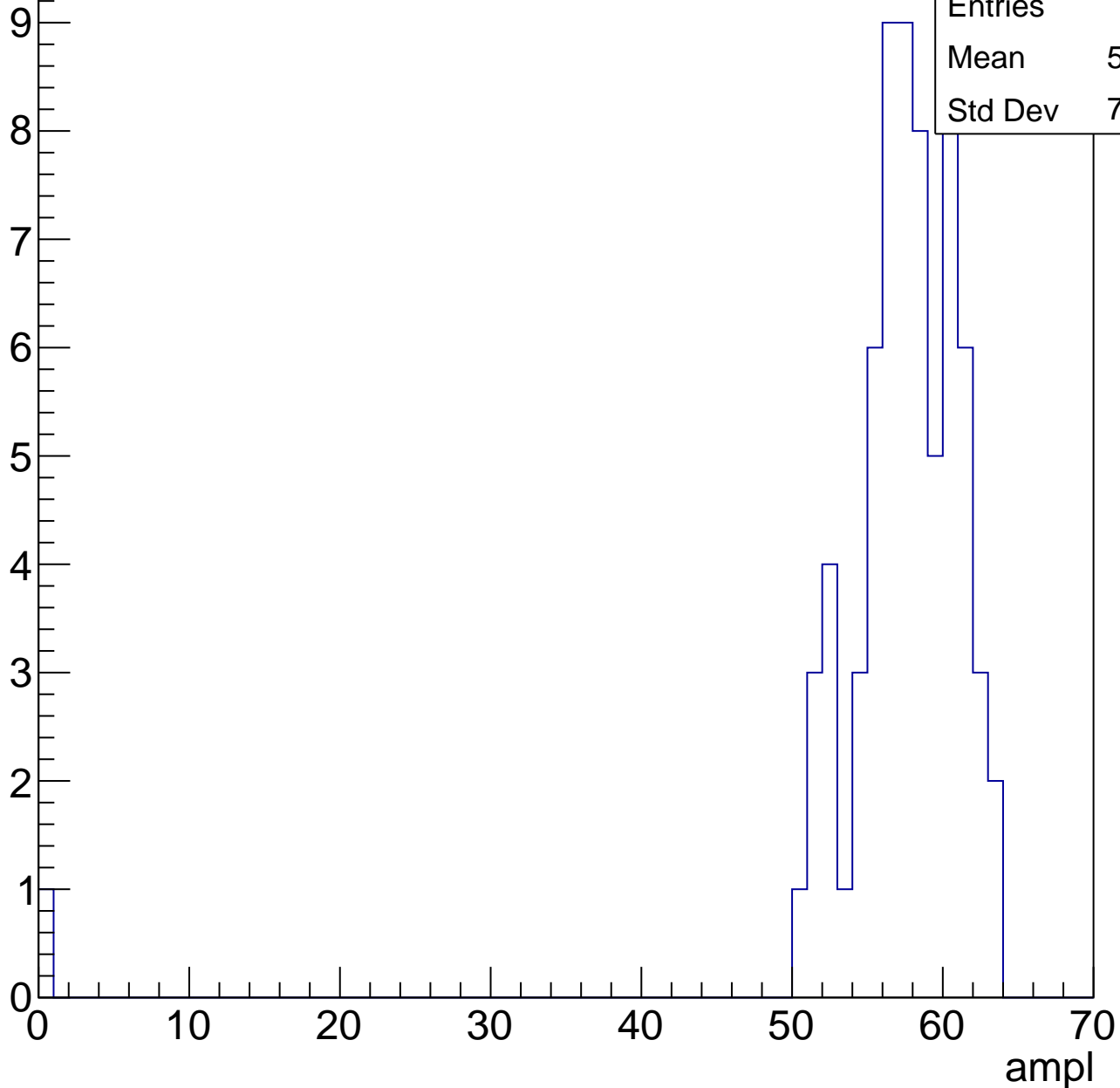
Entries	34
Mean	51.79
Std Dev	3.787



# B1L103S, U1-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

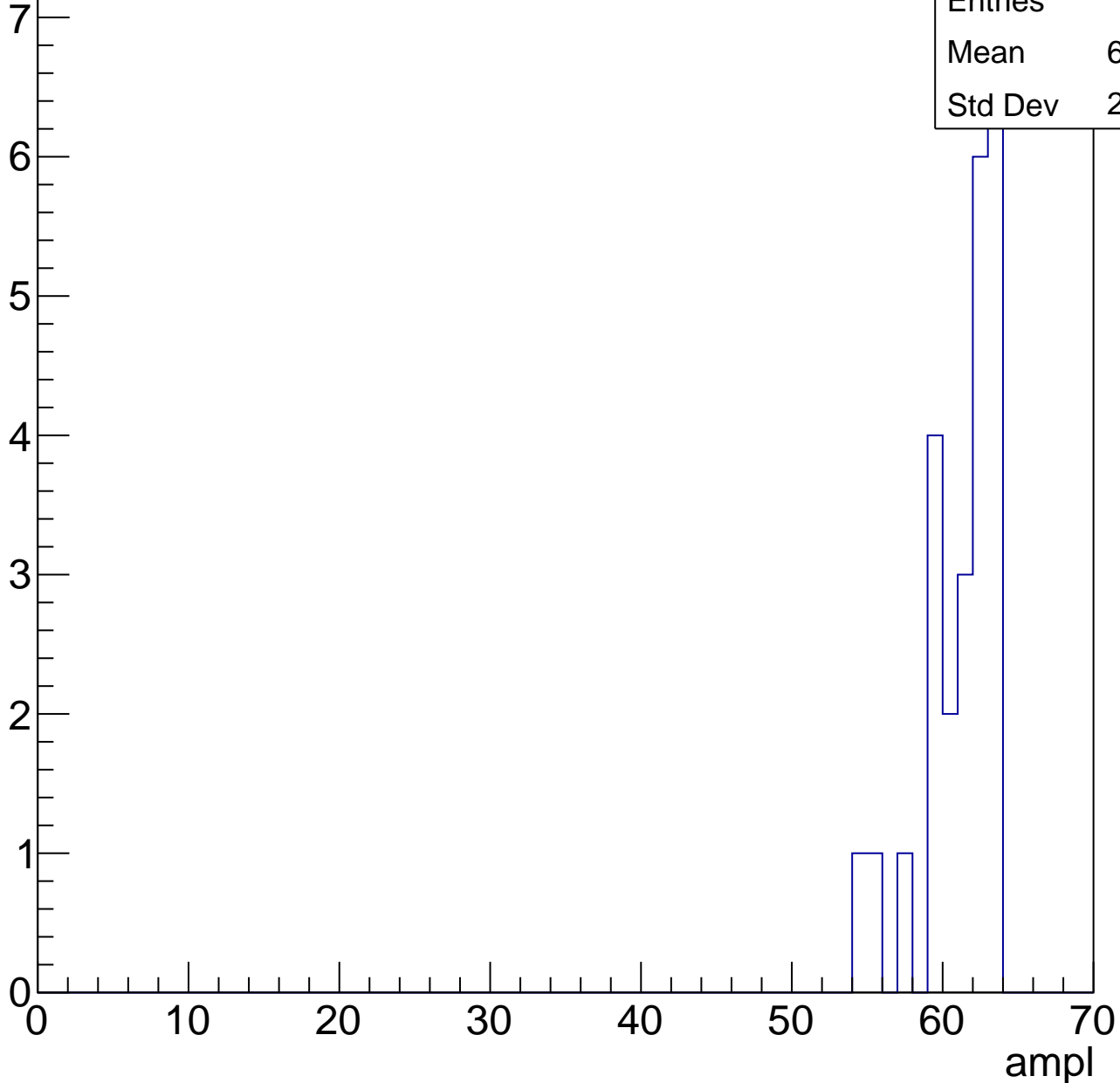


# B1L103S, U1-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	25
Mean	60.72
Std Dev	2.458

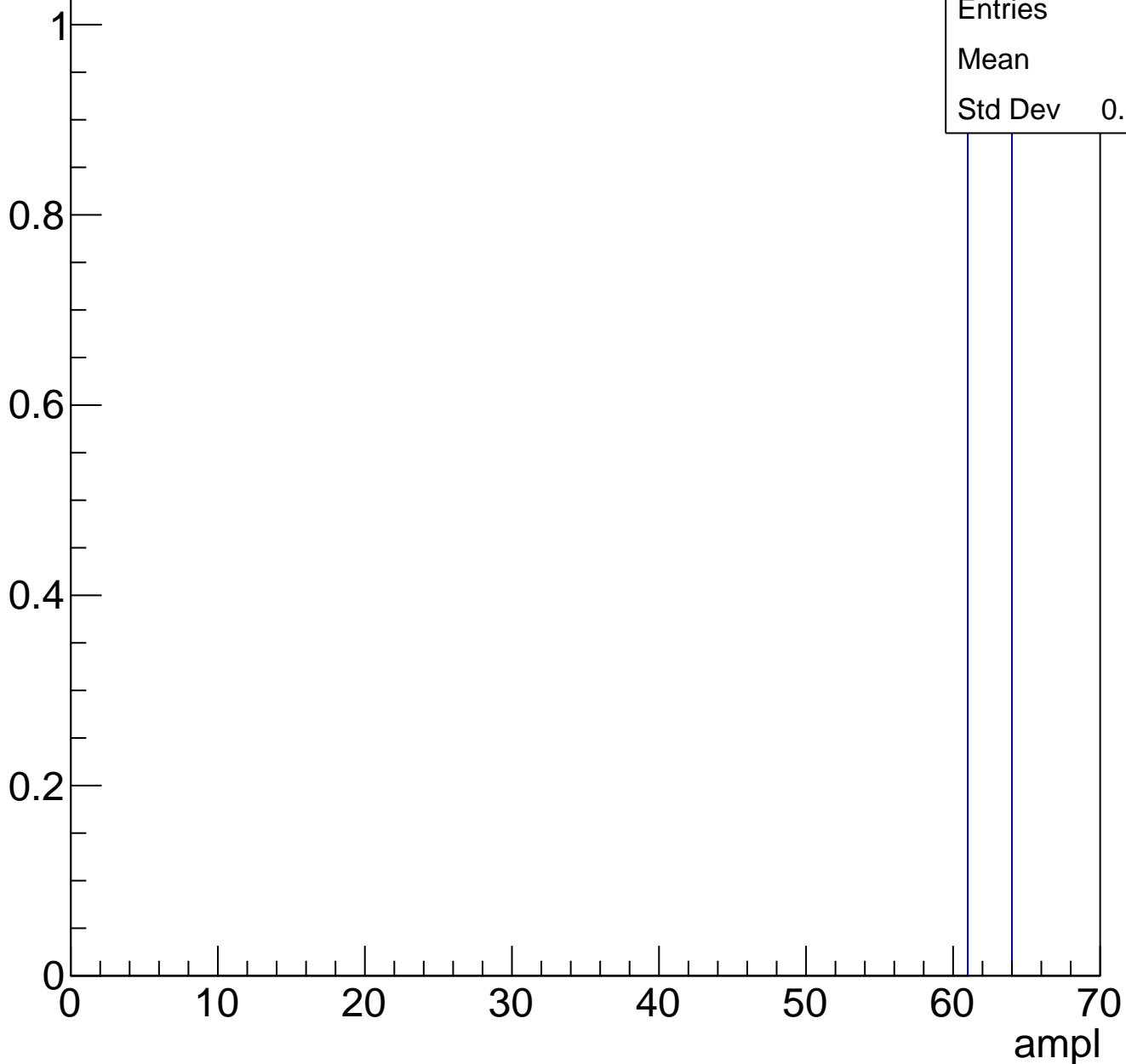




# B1L103S, U1-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch113, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	70
Mean	27.23
Std Dev	5.139

**Gaus mean : 28.4082**

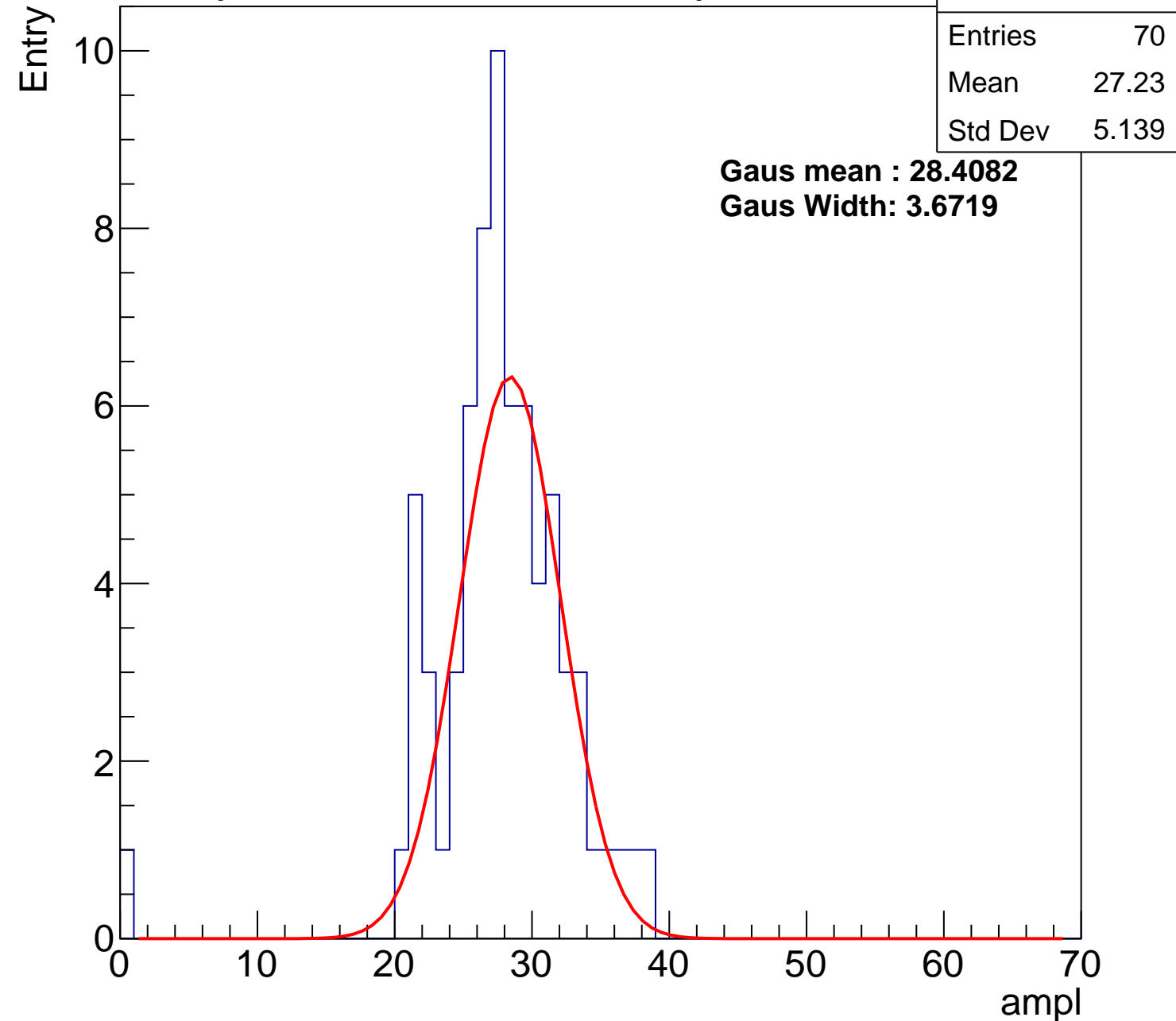
**Gaus Width: 3.6719**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U1-ch113, adc1

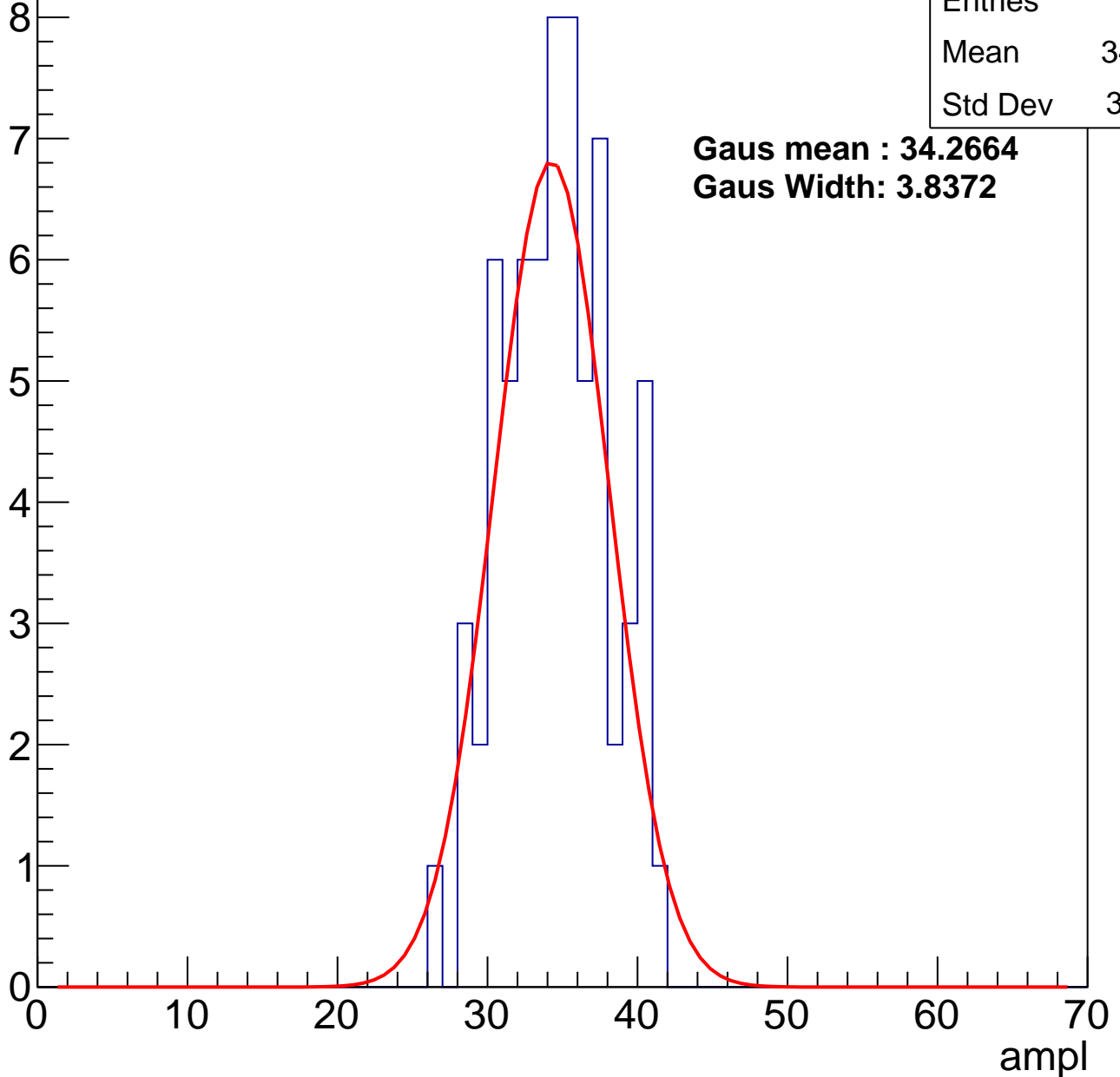
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	34.09
Std Dev	3.471

**Gaus mean : 34.2664**

**Gaus Width: 3.8372**



# B1L103S, U1-ch113, adc2

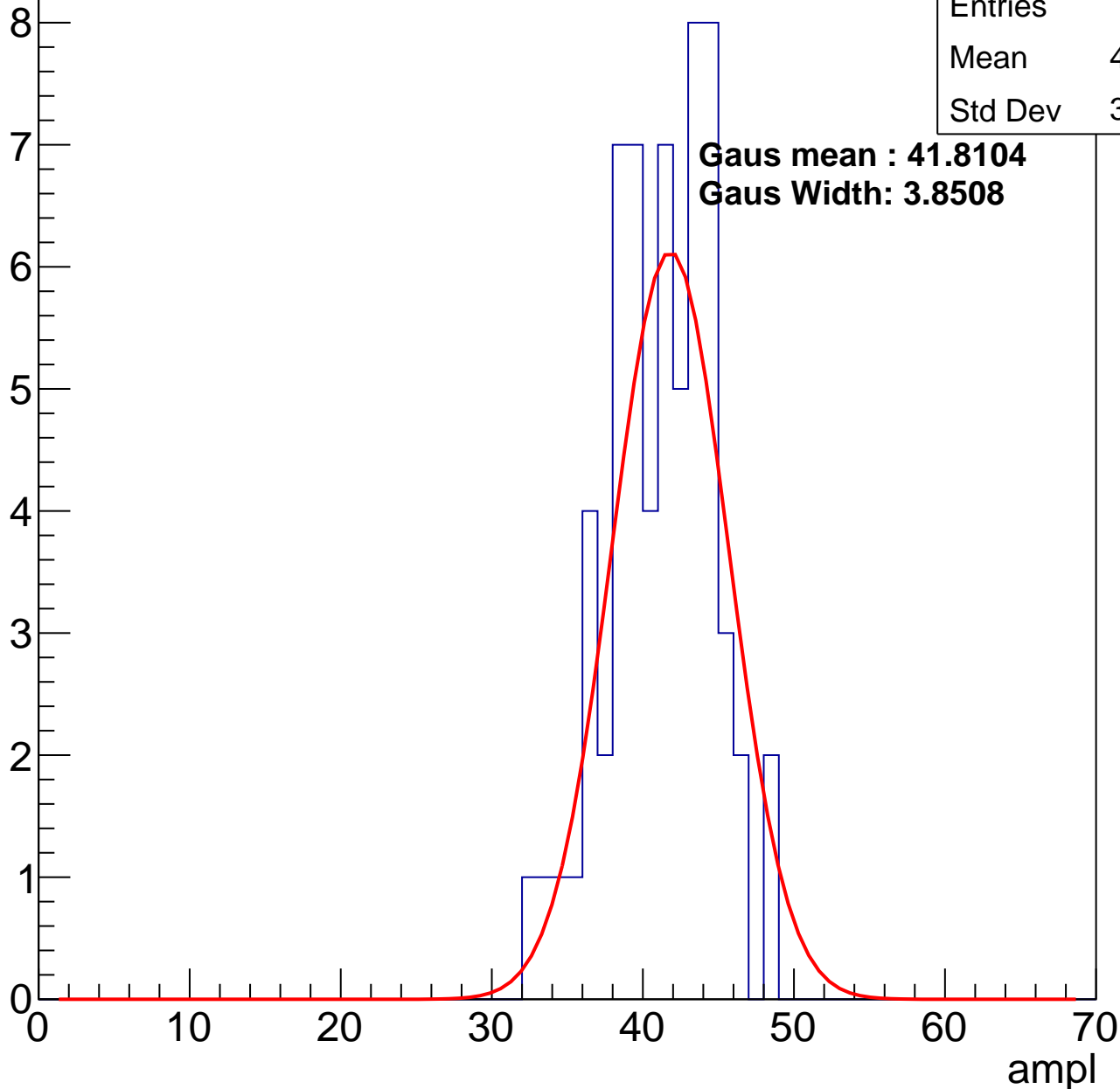
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	40.75
Std Dev	3.469

**Gaus mean : 41.8104**

**Gaus Width: 3.8508**

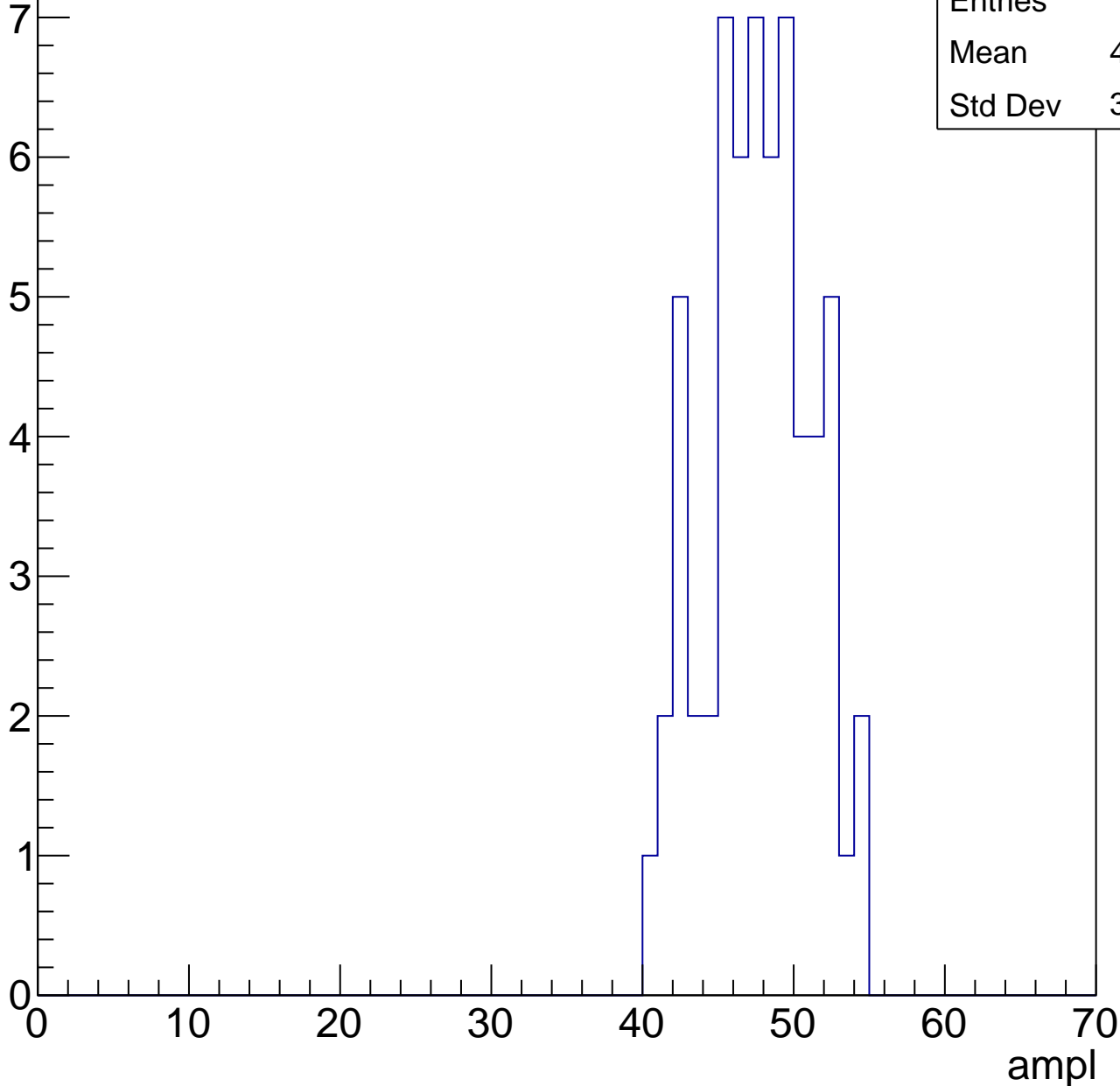


# B1L103S, U1-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	47.25
Std Dev	3.434

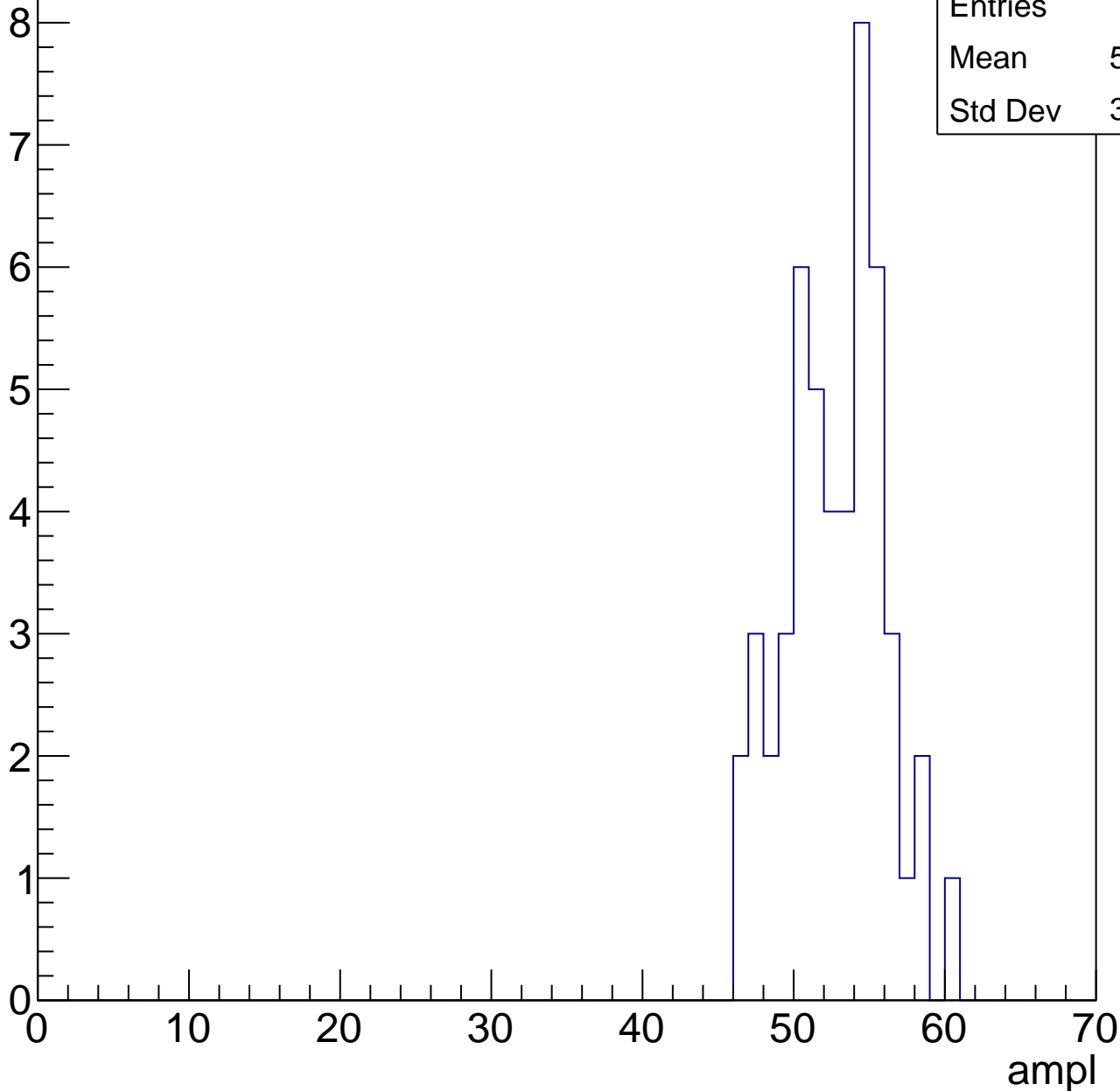


# B1L103S, U1-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	52.28
Std Dev	3.256

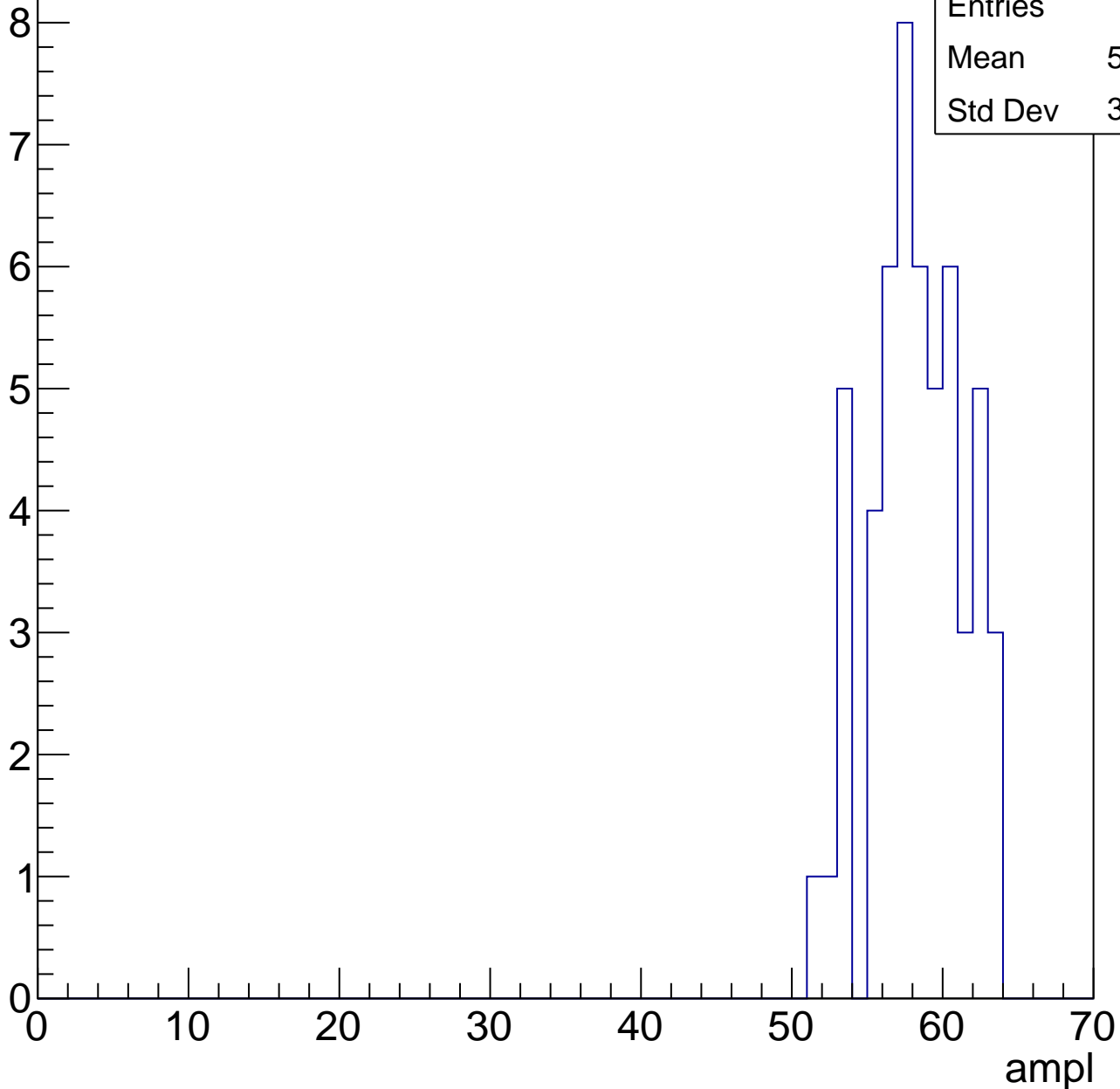


# B1L103S, U1-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	57.83
Std Dev	3.033

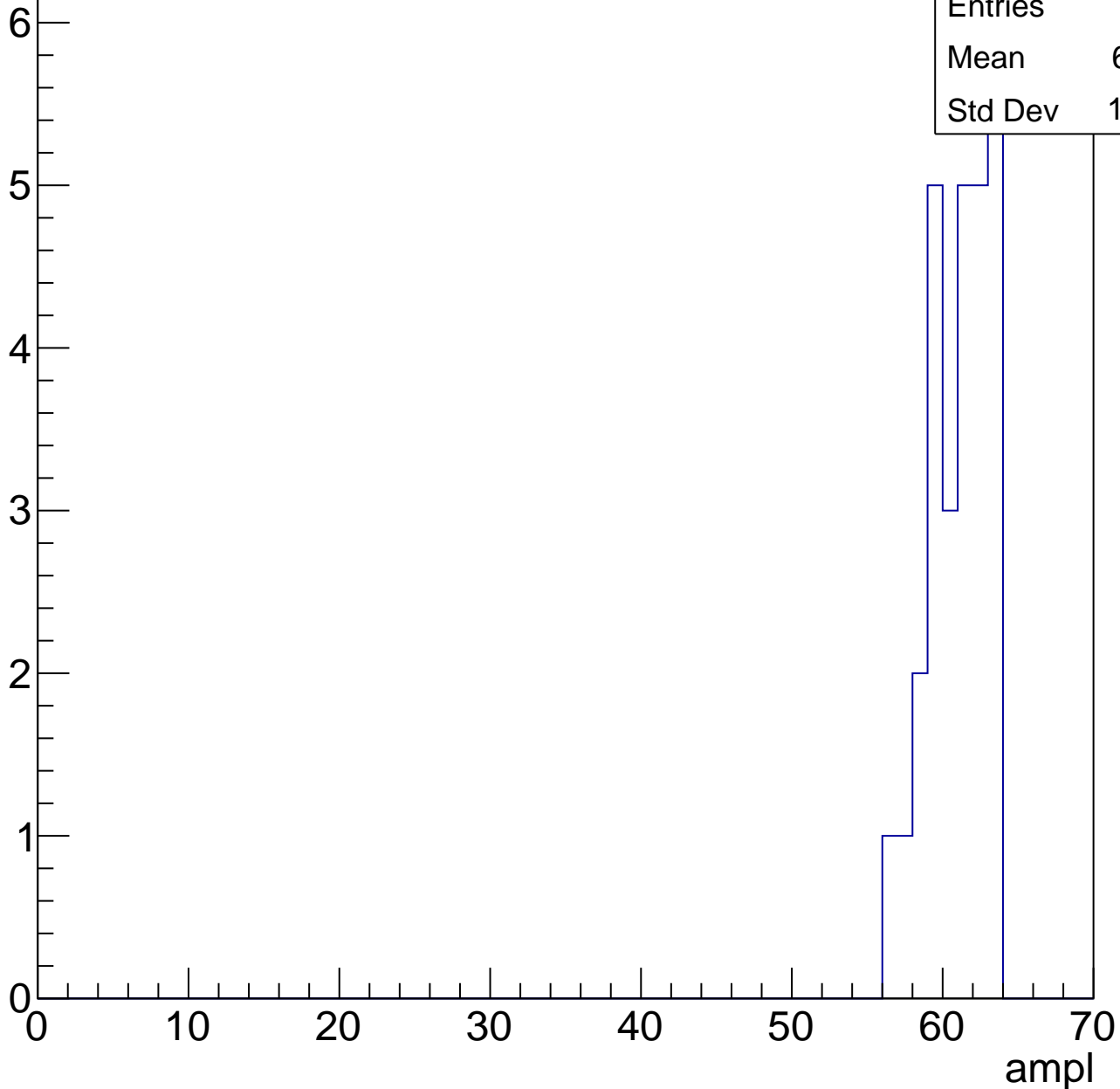


# B1L103S, U1-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	28
Mean	60.61
Std Dev	1.952

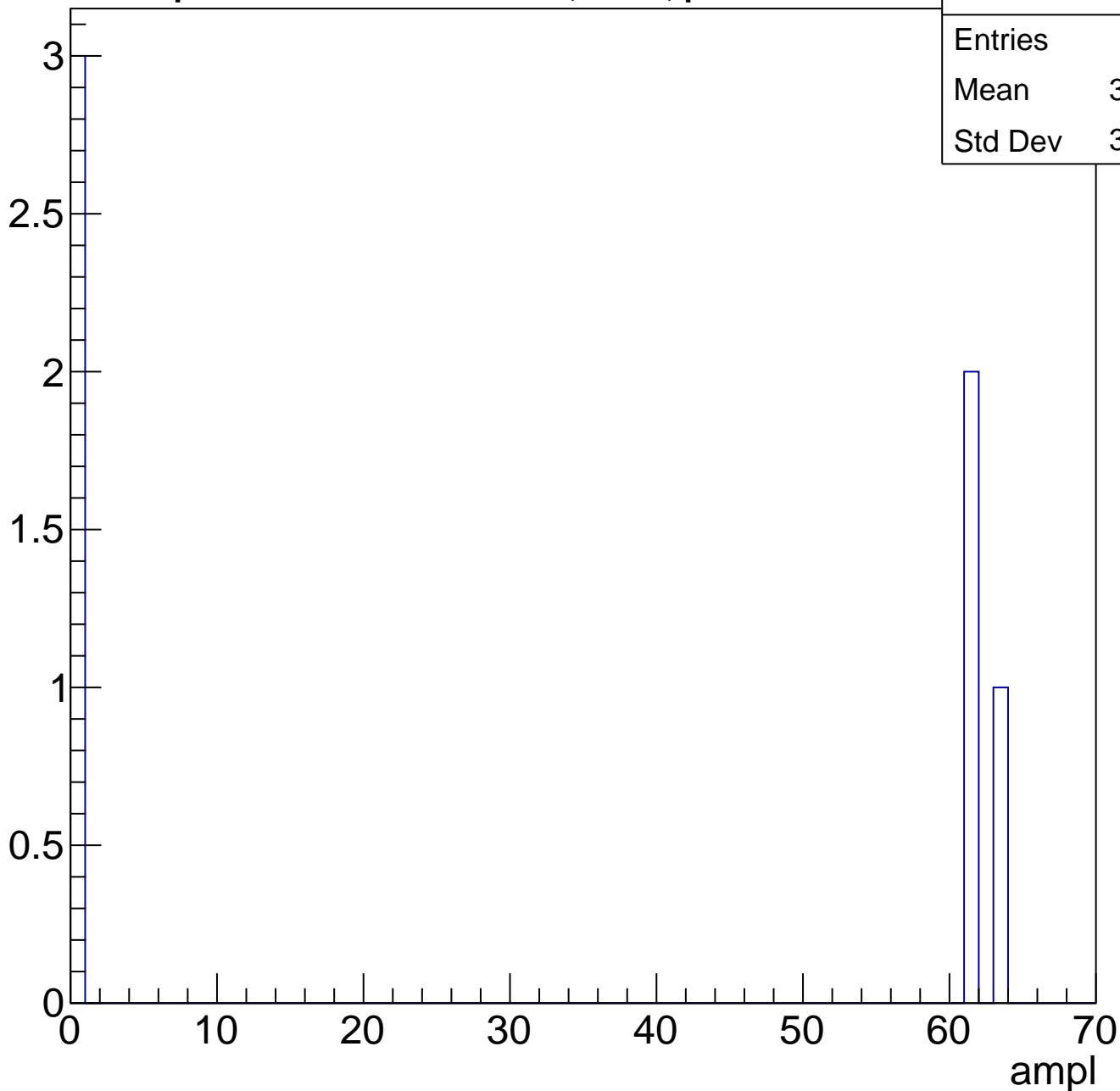




# B1L103S, U1-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	6
Mean	30.83
Std Dev	30.84

# B1L103S, U1-ch114, adc0

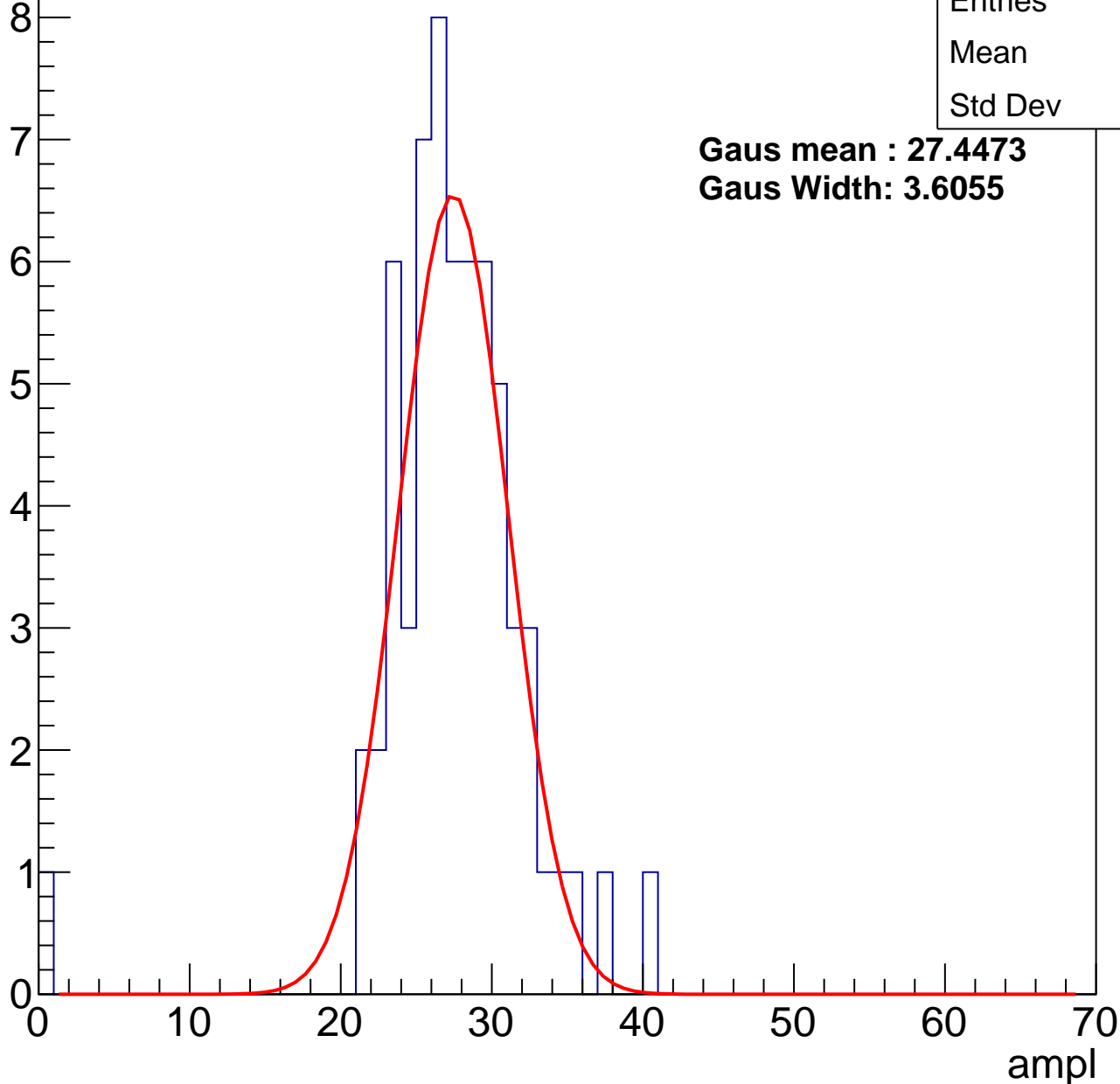
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	27
Std Dev	5.08

**Gaus mean : 27.4473**

**Gaus Width: 3.6055**



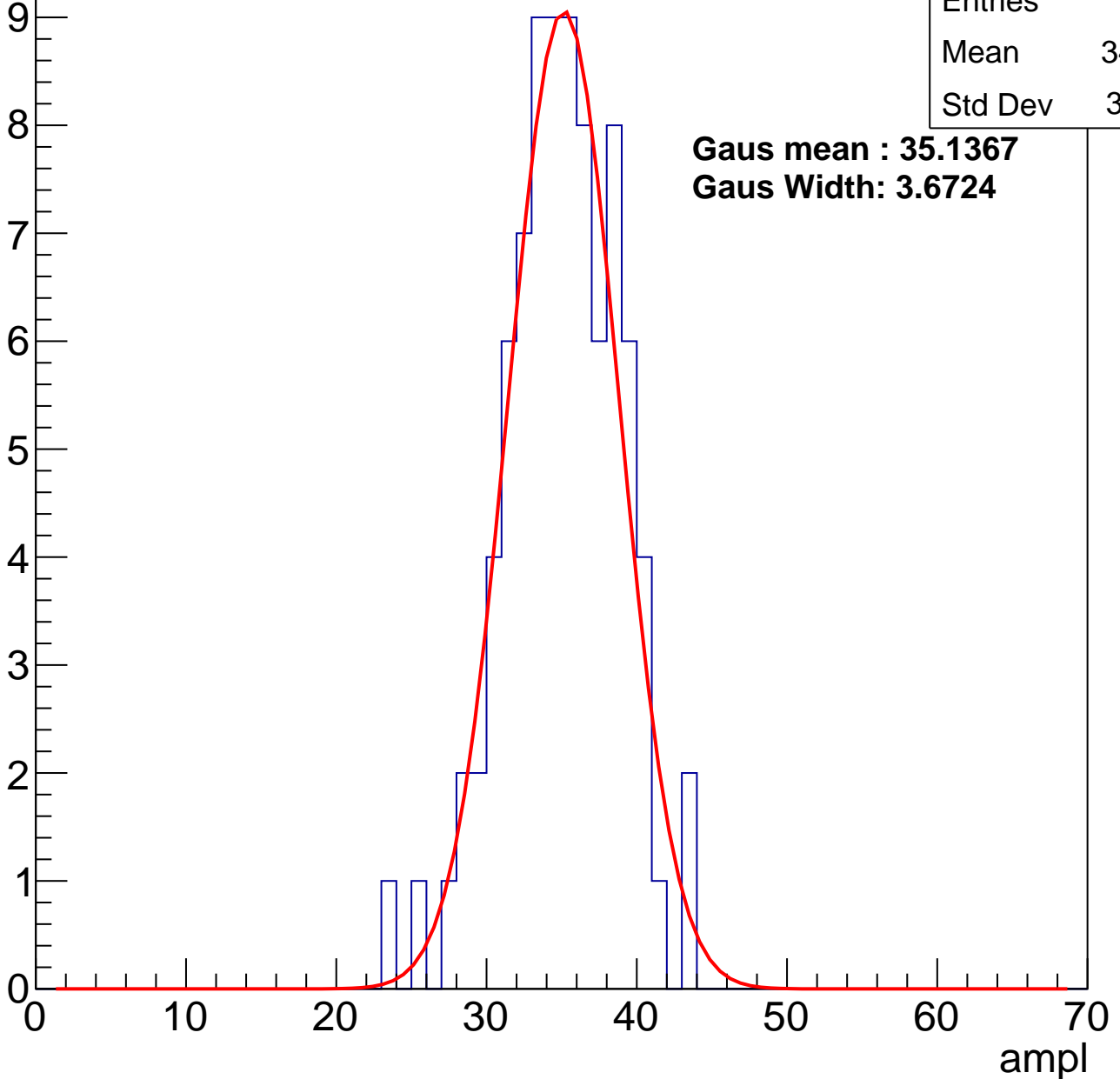
# B1L103S, U1-ch114, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	86
Mean	34.56
Std Dev	3.781

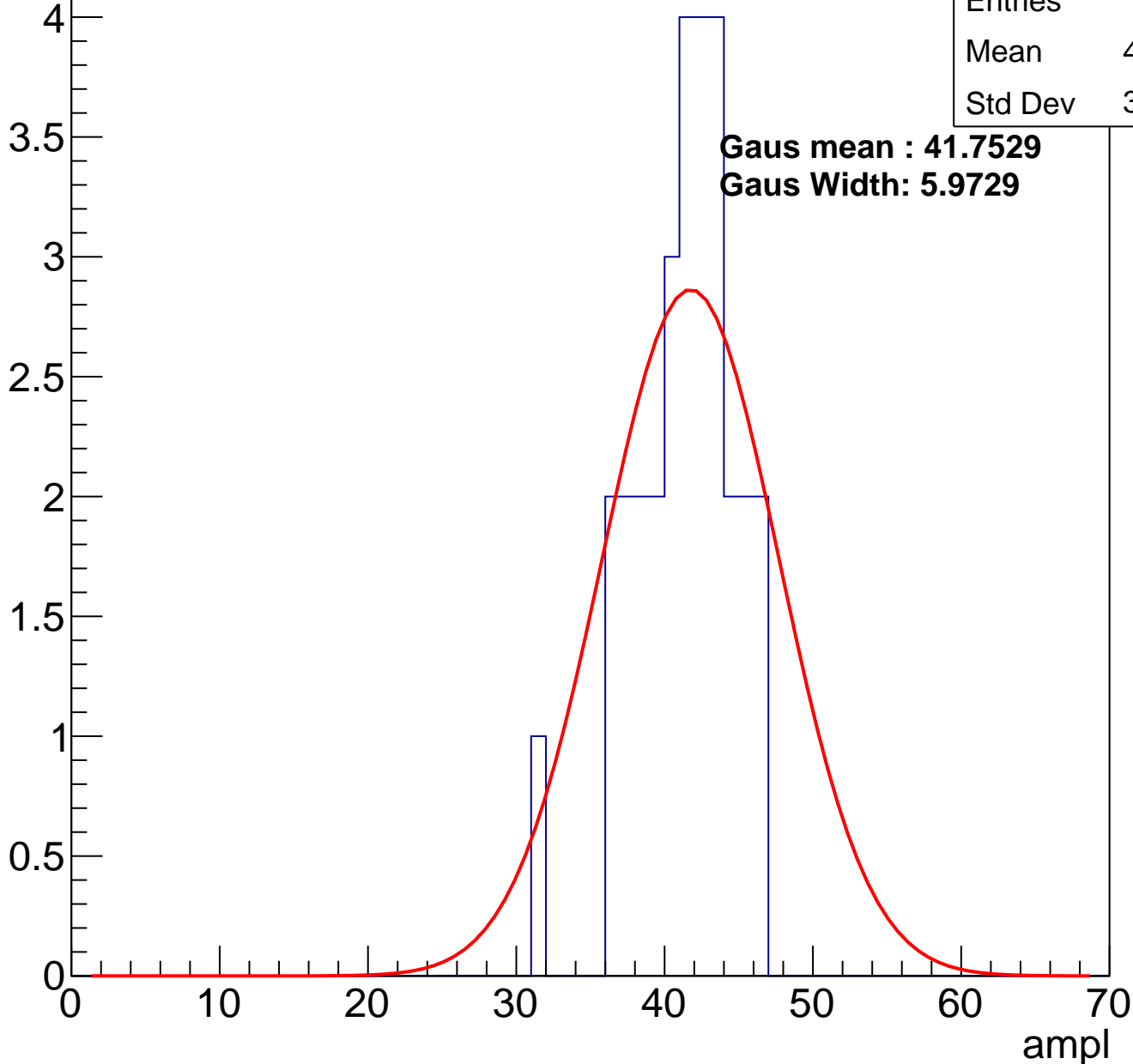
**Gaus mean : 35.1367**  
**Gaus Width: 3.6724**



# B1L103S, U1-ch114, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

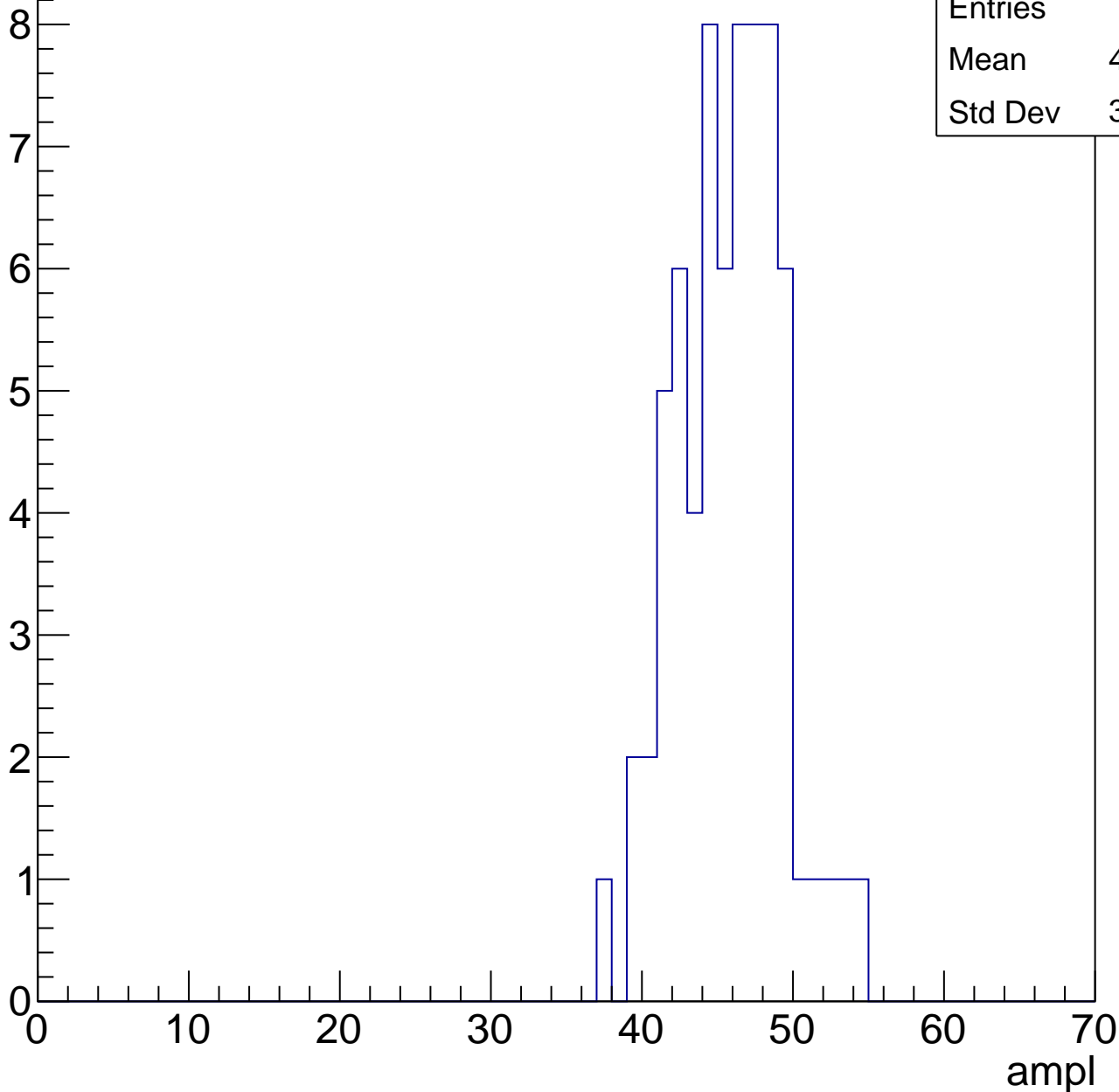


# B1L103S, U1-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	45.33
Std Dev	3.404

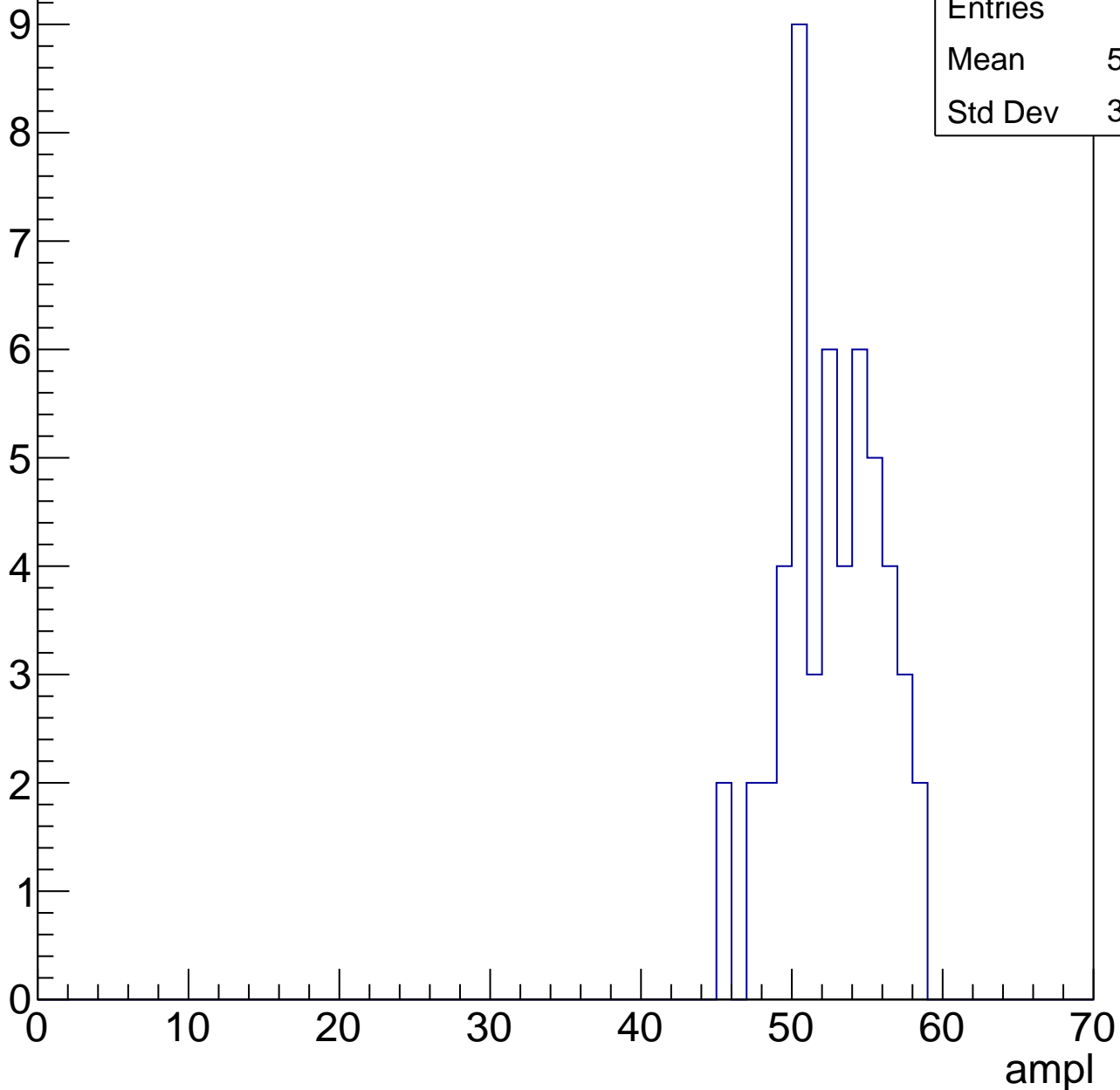


# B1L103S, U1-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

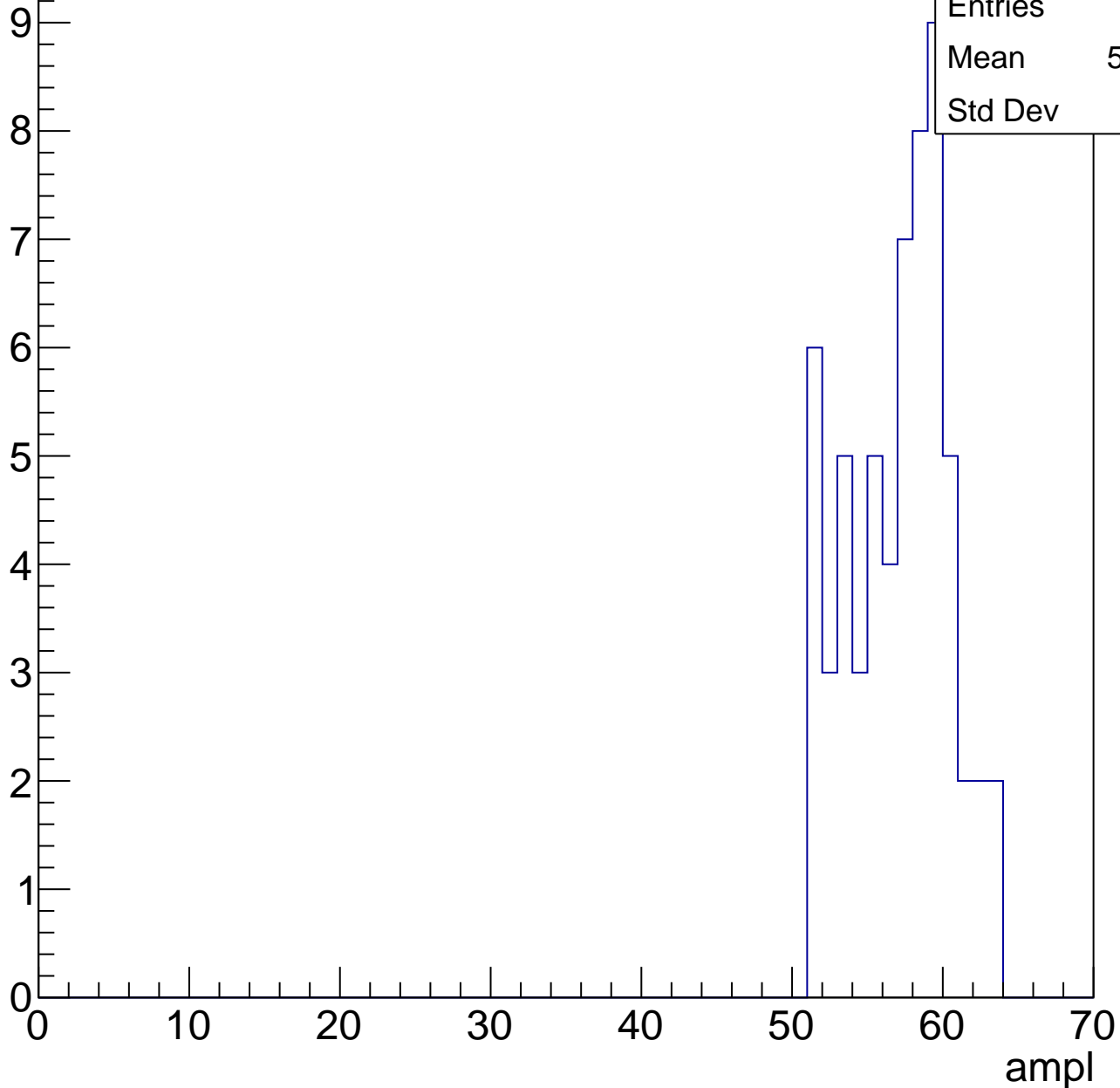
Entries	52
Mean	52.17
Std Dev	3.215



# B1L103S, U1-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



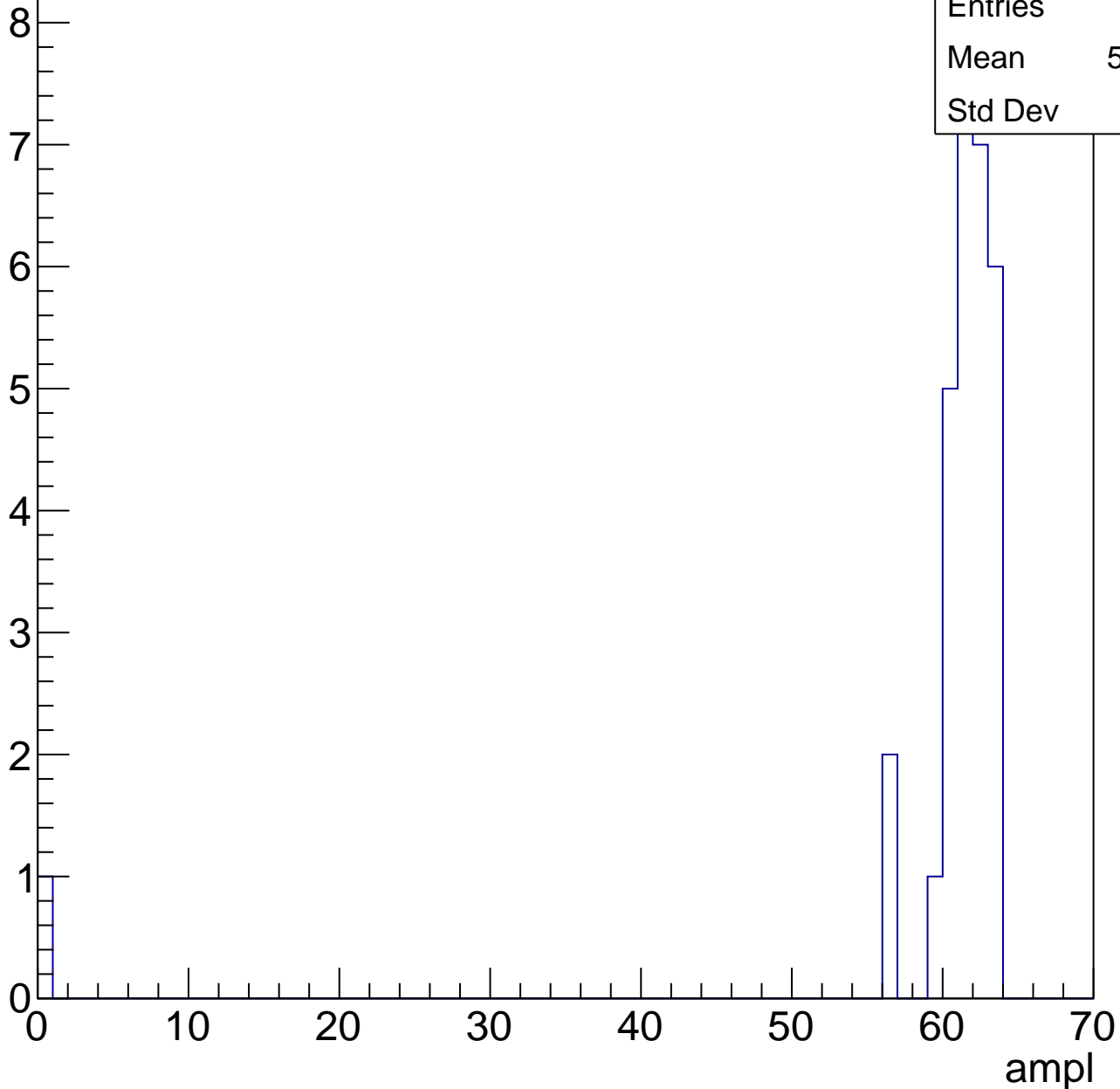
Entries	61
Mean	56.62
Std Dev	3.28

# B1L103S, U1-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	30
Mean	59.03
Std Dev	11.1





# B1L103S, U1-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch115, adc0

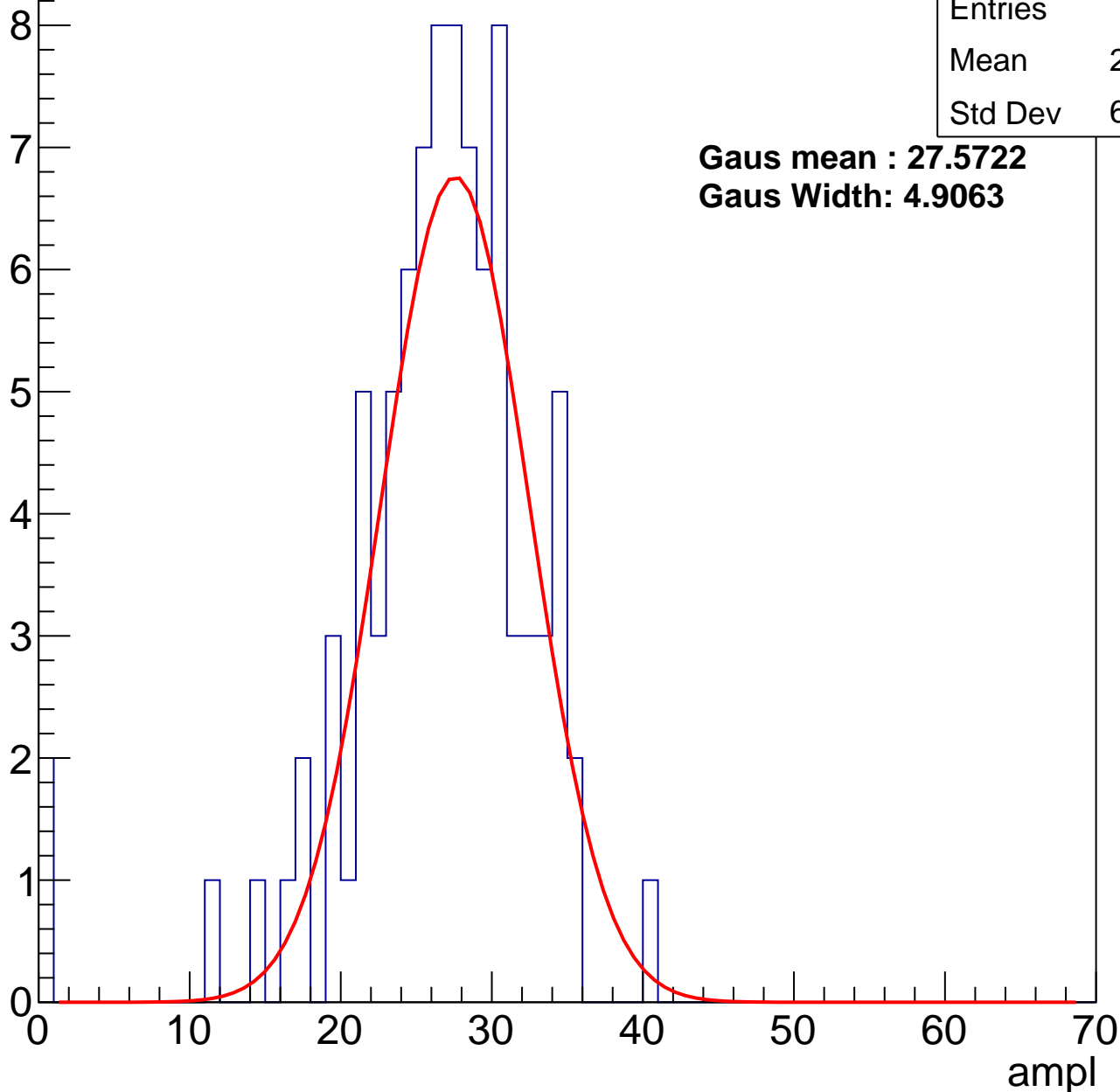
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	91
Mean	25.92
Std Dev	6.325

**Gaus mean : 27.5722**

**Gaus Width: 4.9063**



# B1L103S, U1-ch115, adc1

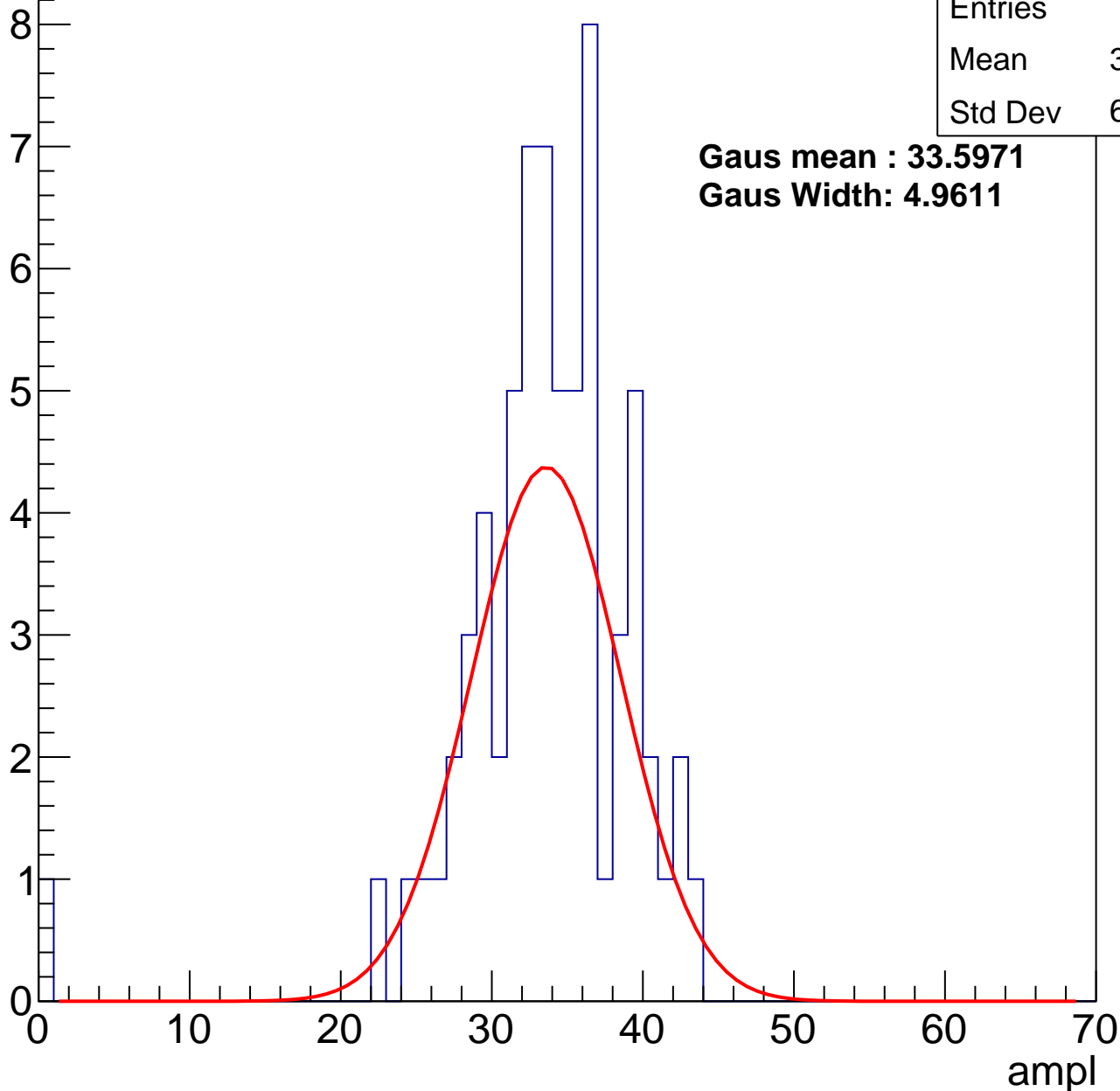
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	33.06
Std Dev	6.005

**Gaus mean : 33.5971**

**Gaus Width: 4.9611**



# B1L103S, U1-ch115, adc2

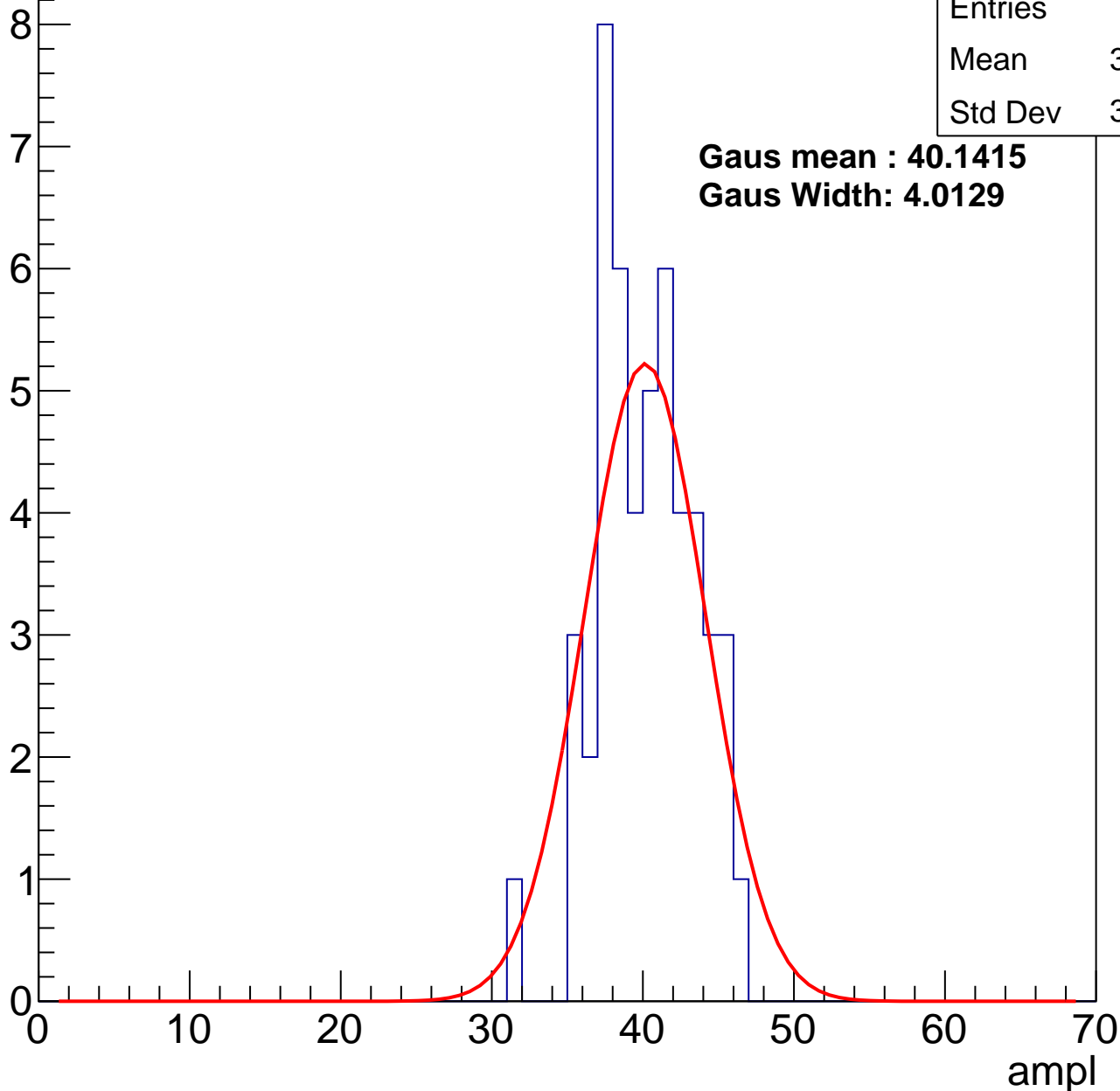
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	39.74
Std Dev	3.167

**Gaus mean : 40.1415**

**Gaus Width: 4.0129**

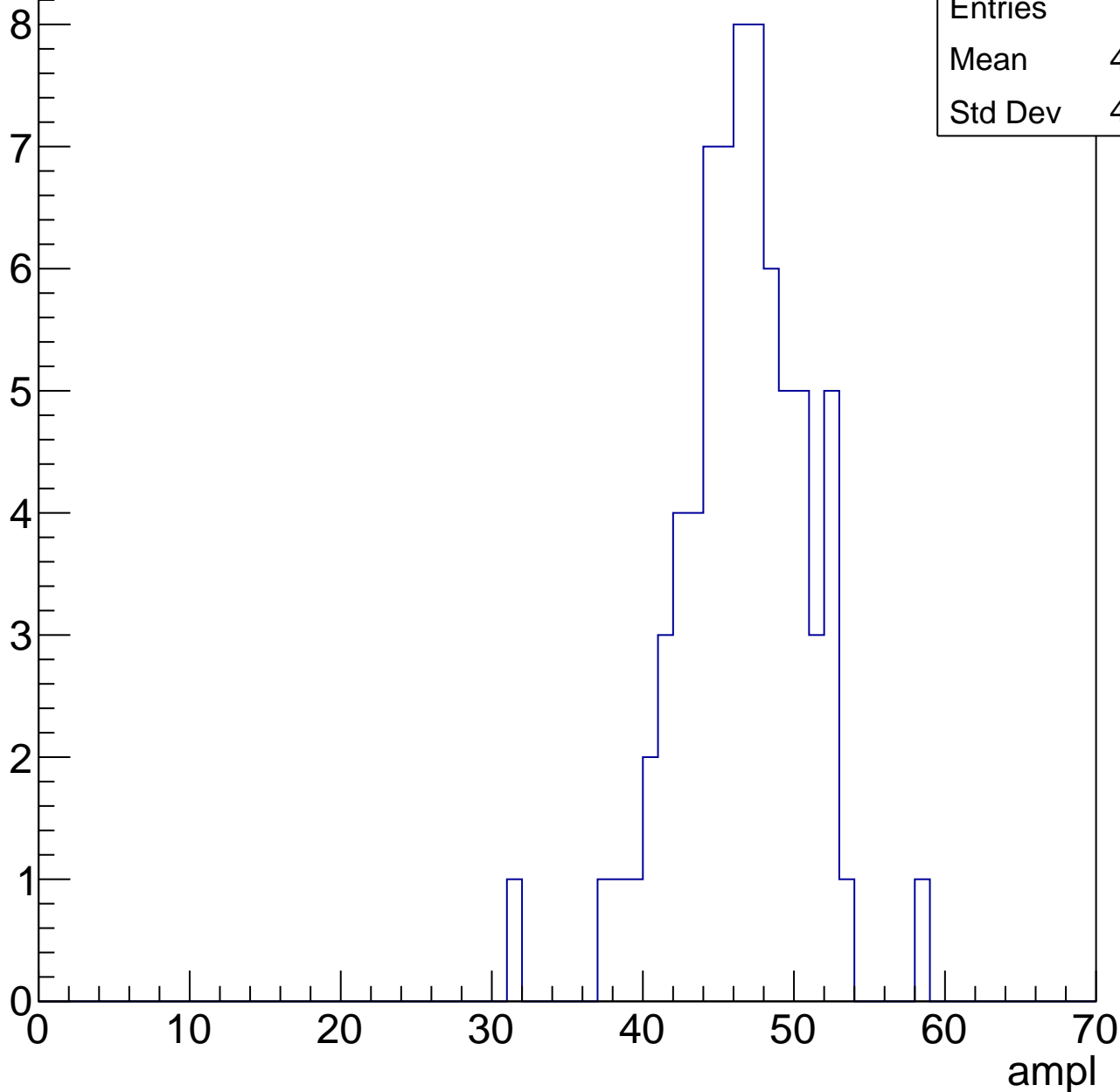


# B1L103S, U1-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	46.05
Std Dev	4.229

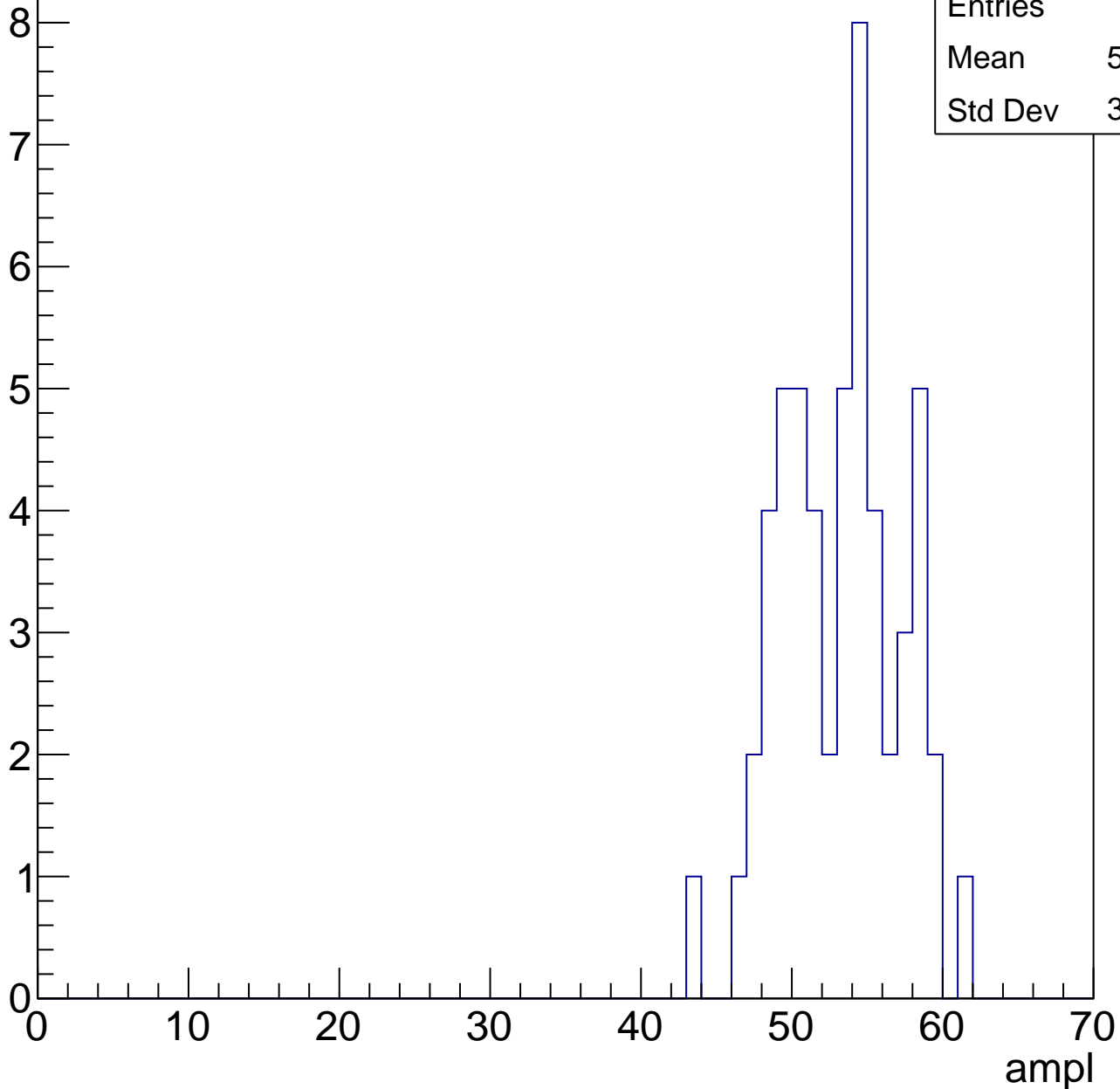


# B1L103S, U1-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	52.72
Std Dev	3.875

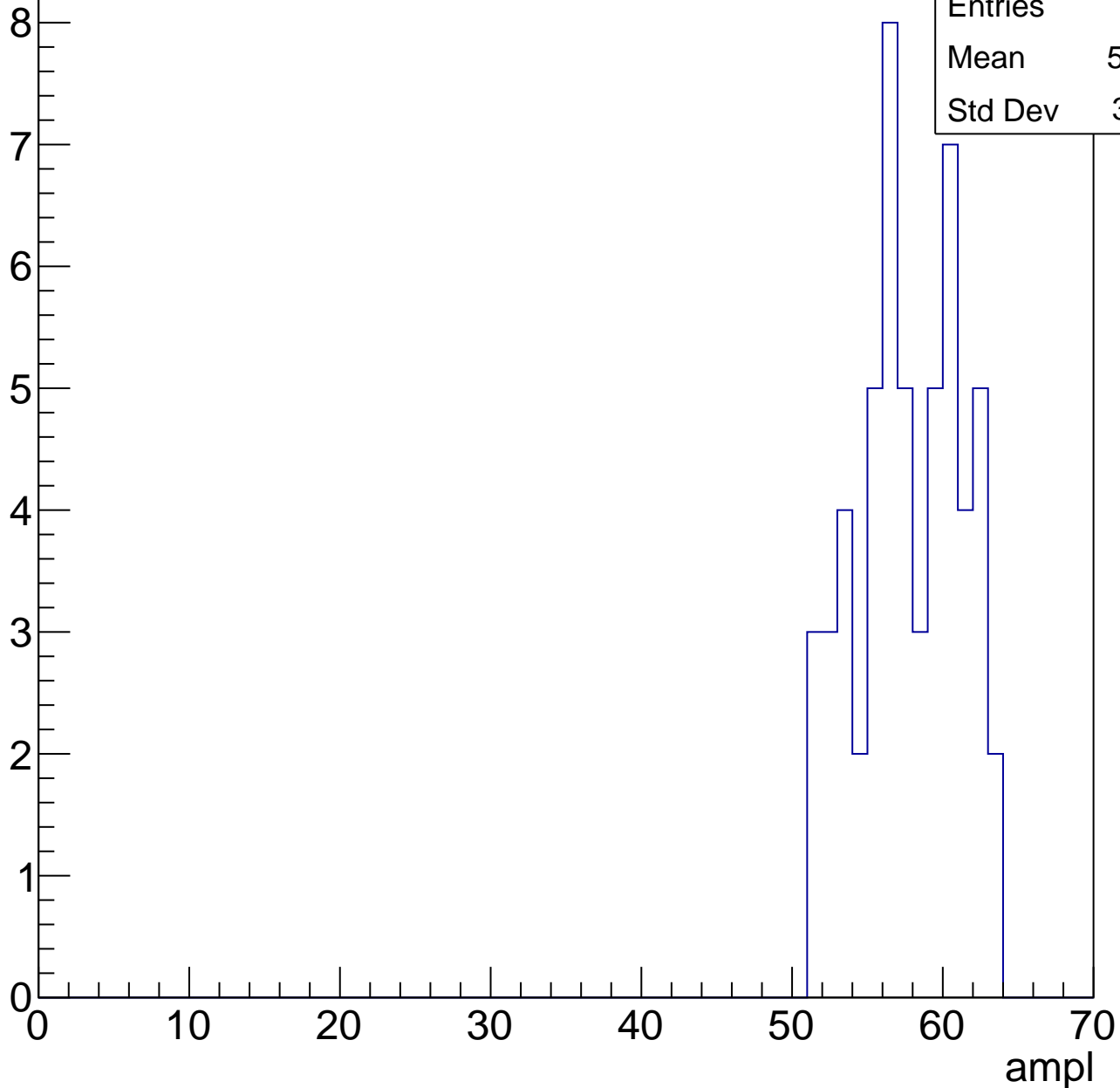


# B1L103S, U1-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	57.25
Std Dev	3.371

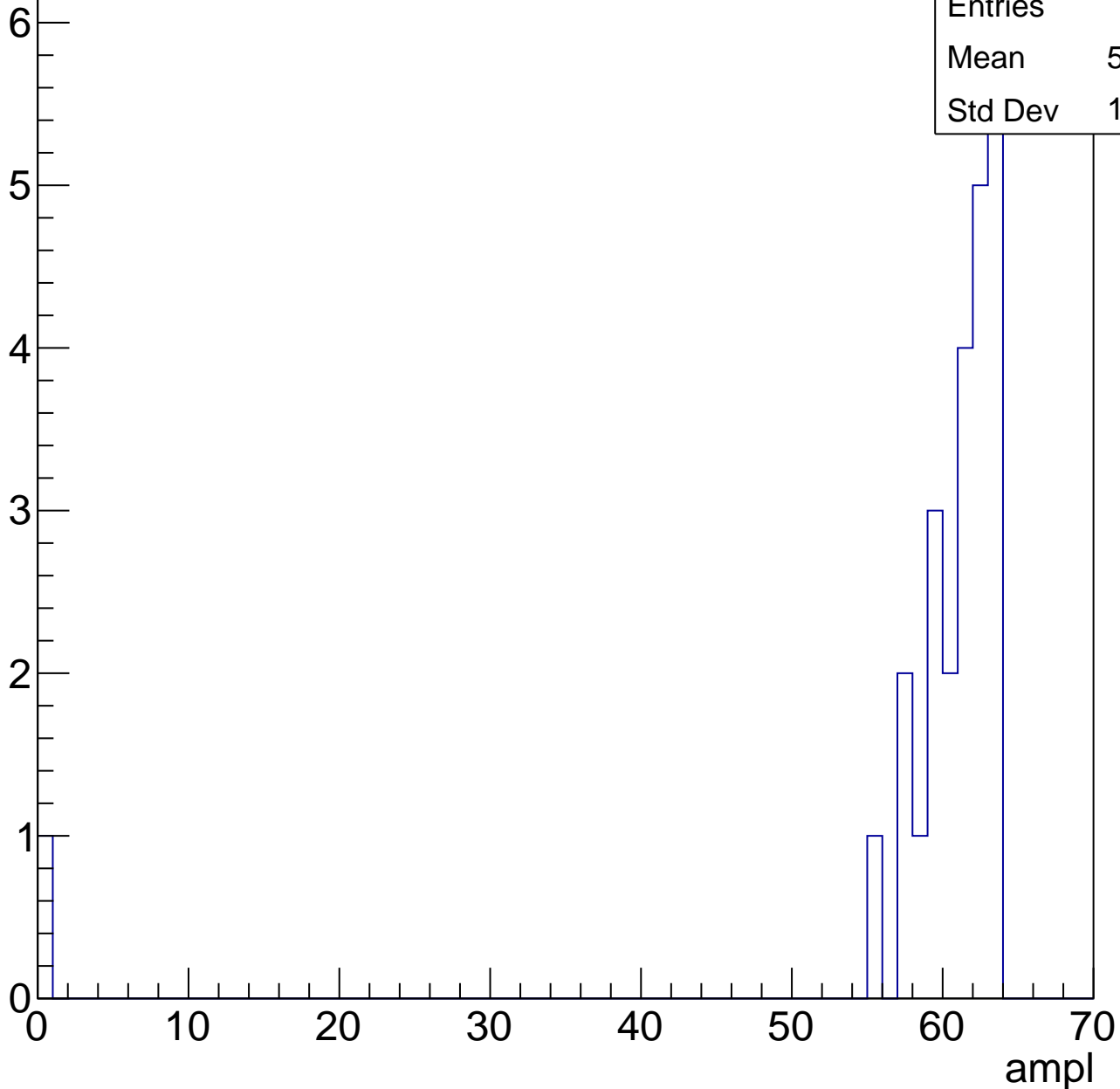


# B1L103S, U1-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	25
Mean	58.24
Std Dev	12.08

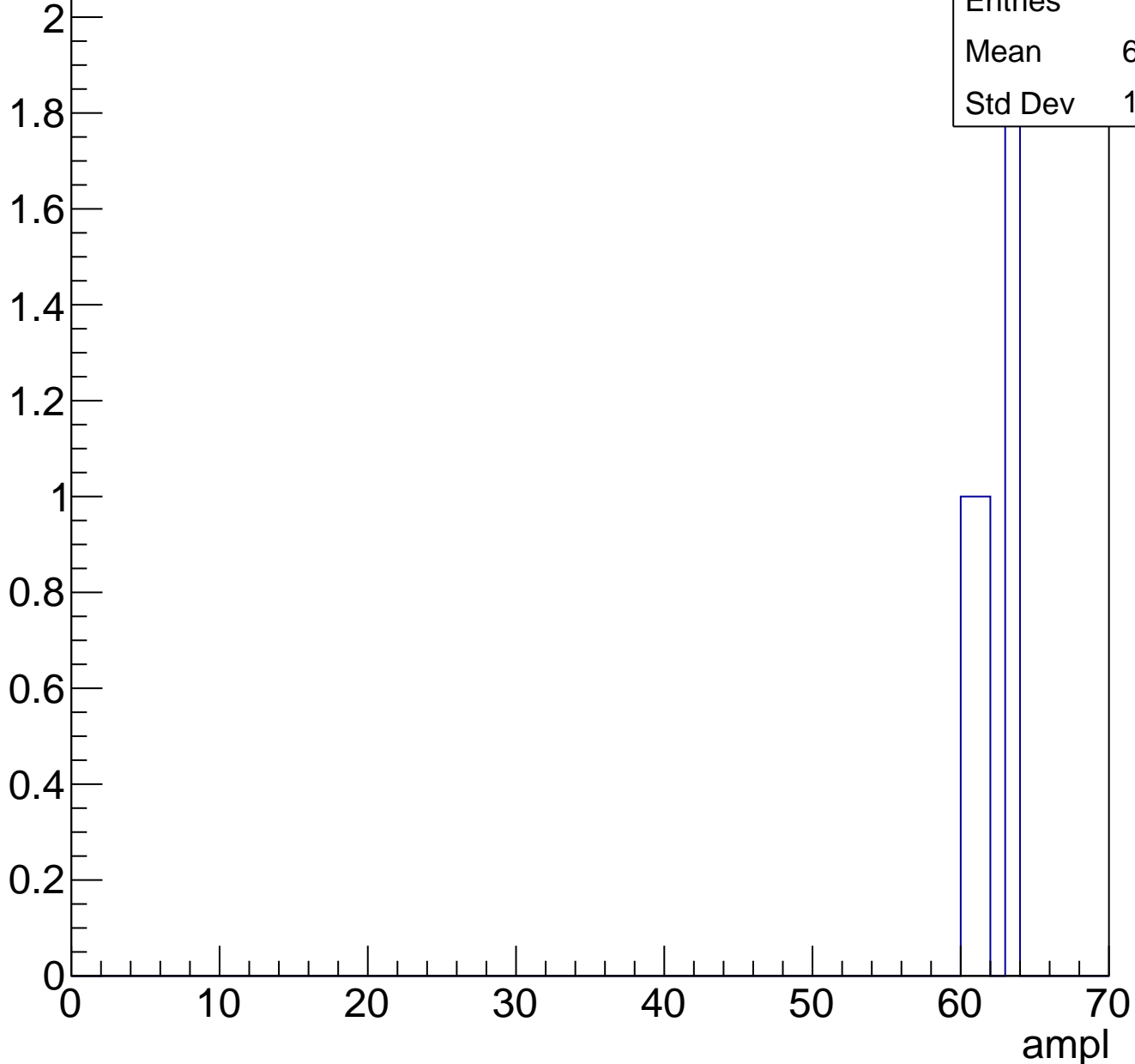




# B1L103S, U1-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	4
Mean	61.75
Std Dev	1.299

# B1L103S, U1-ch116, adc0

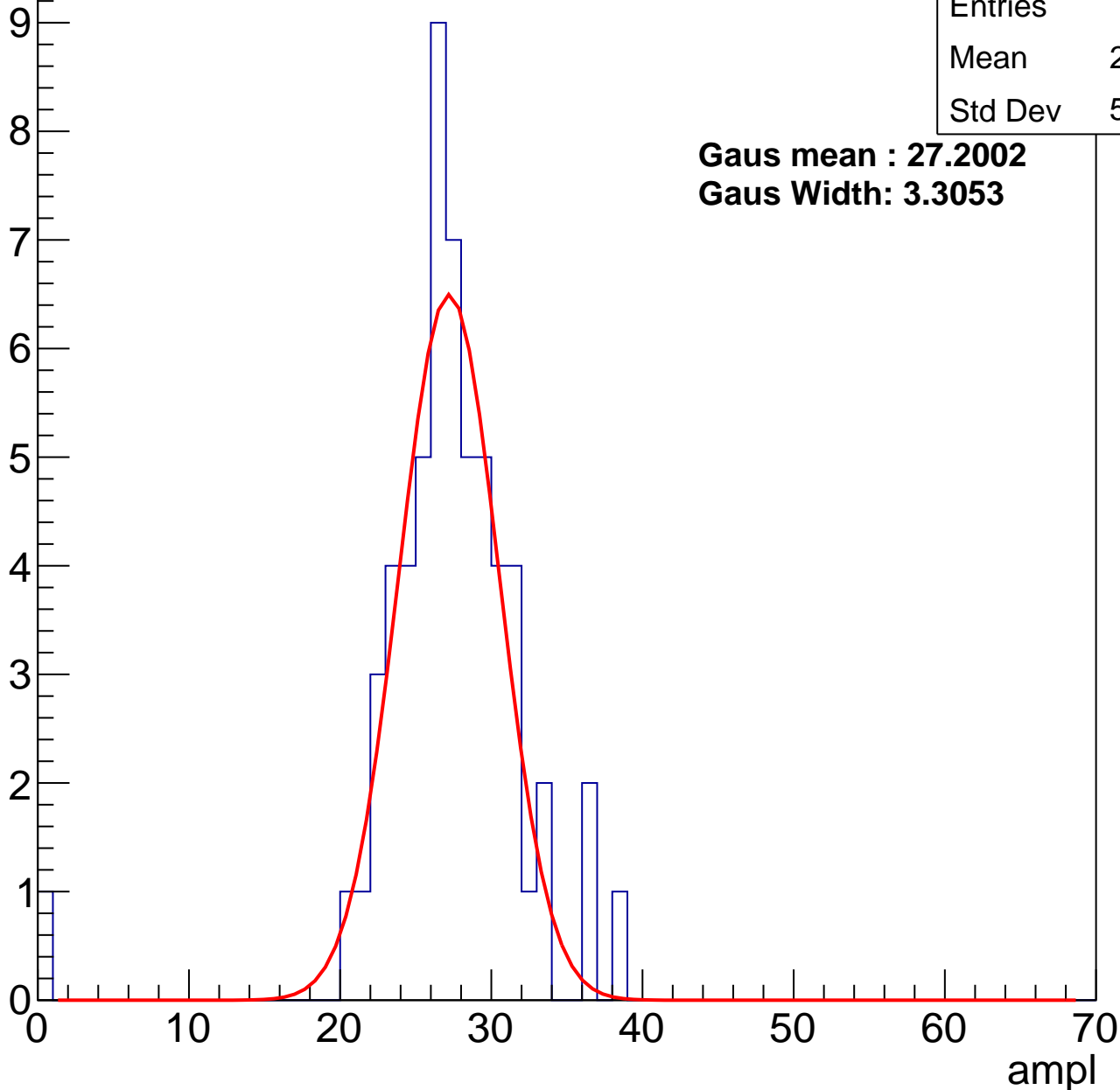
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	26.78
Std Dev	5.076

**Gaus mean : 27.2002**

**Gaus Width: 3.3053**



# B1L103S, U1-ch116, adc1

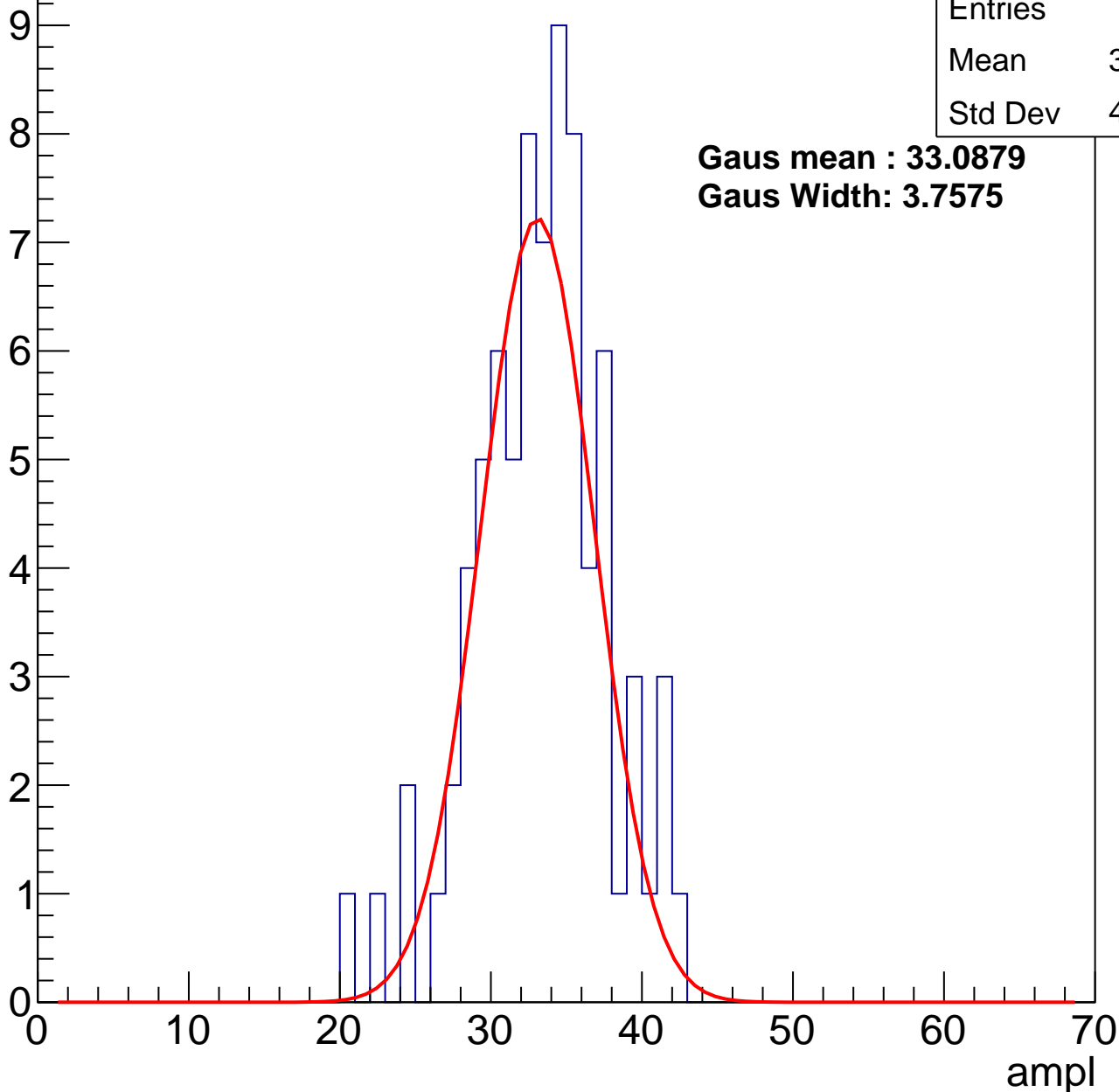
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	32.83
Std Dev	4.328

**Gaus mean : 33.0879**

**Gaus Width: 3.7575**



# B1L103S, U1-ch116, adc2

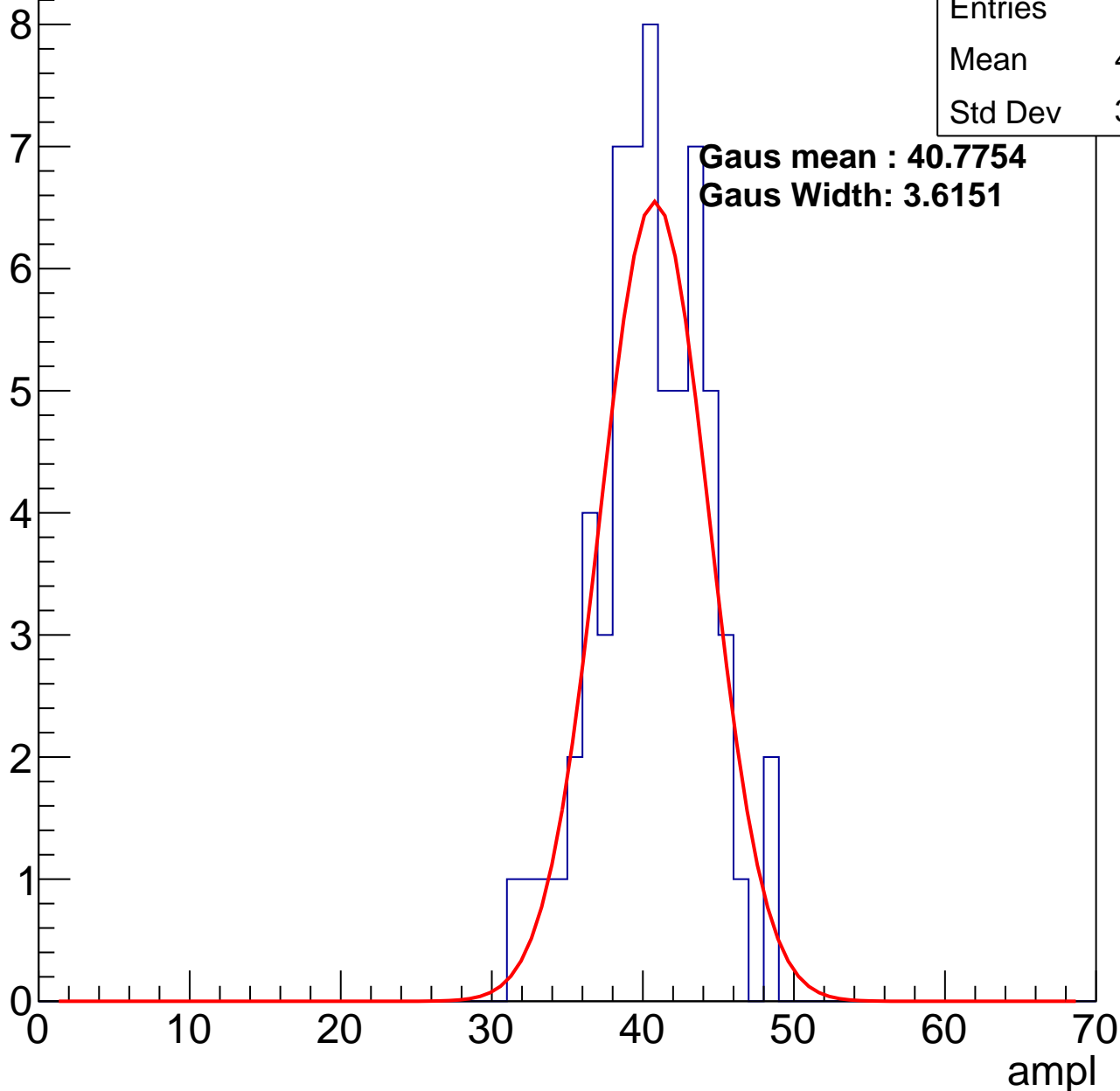
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	40.11
Std Dev	3.591

**Gaus mean : 40.7754**

**Gaus Width: 3.6151**

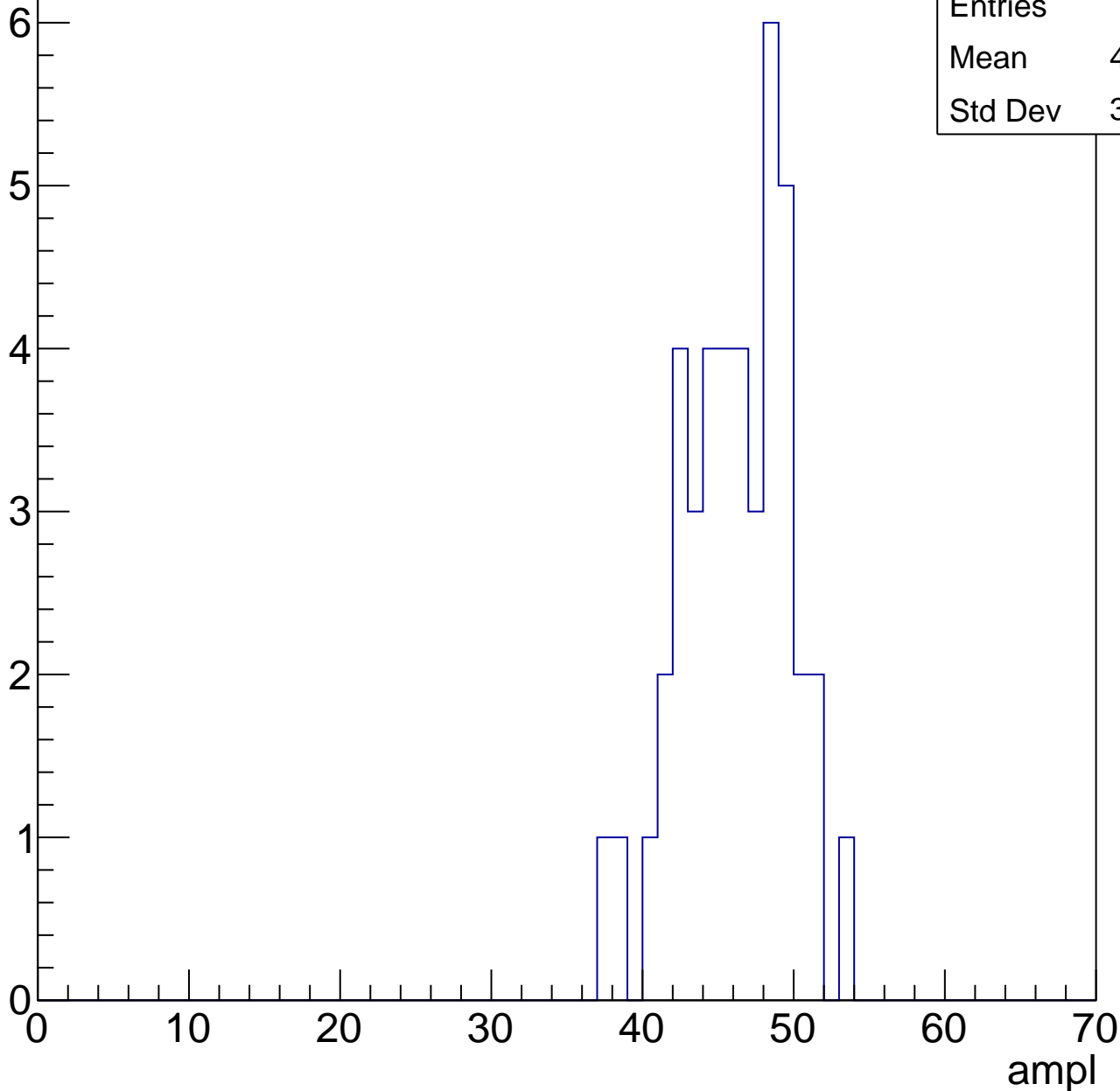


# B1L103S, U1-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	43
Mean	45.65
Std Dev	3.543

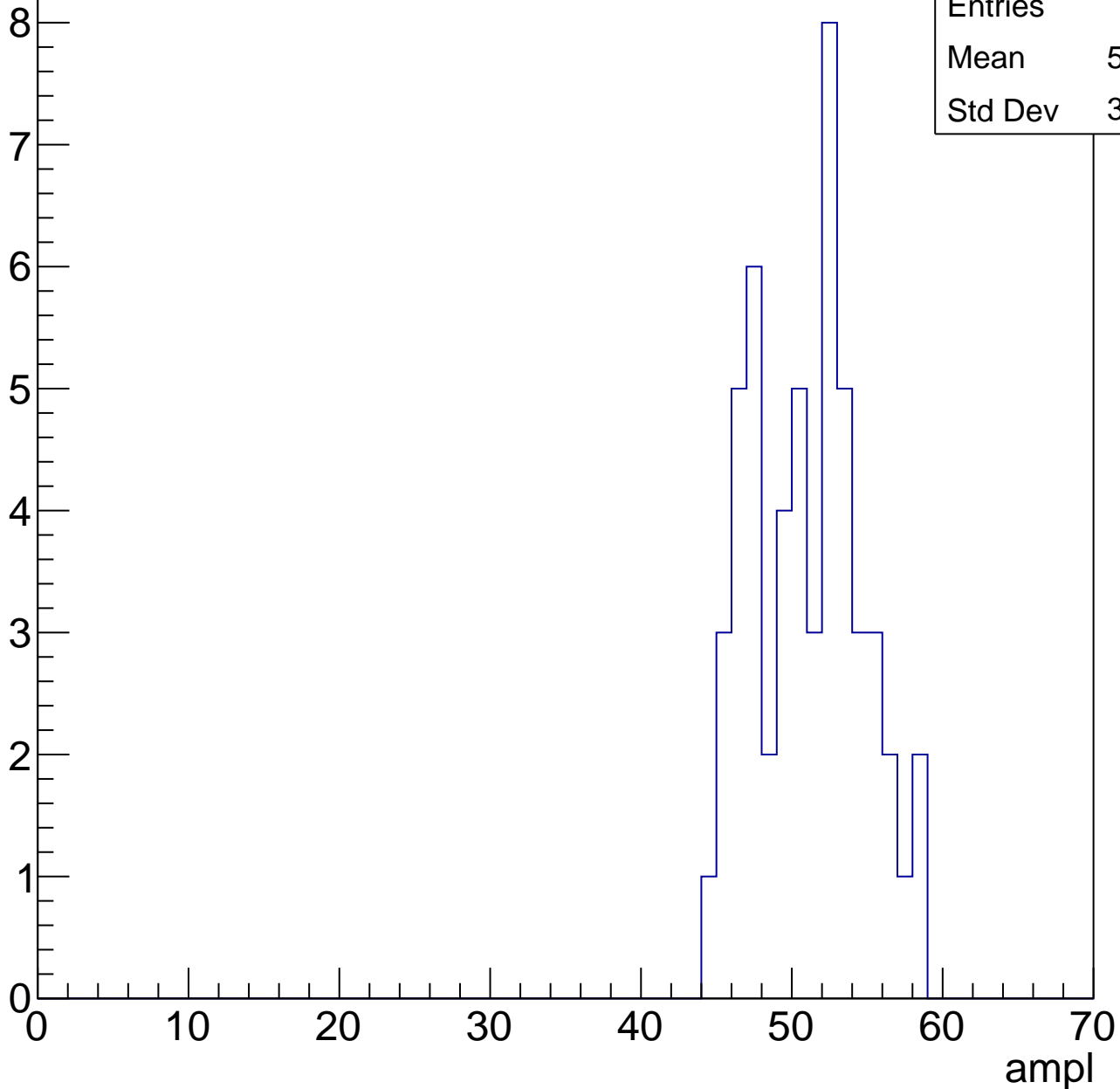


# B1L103S, U1-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	50.55
Std Dev	3.616

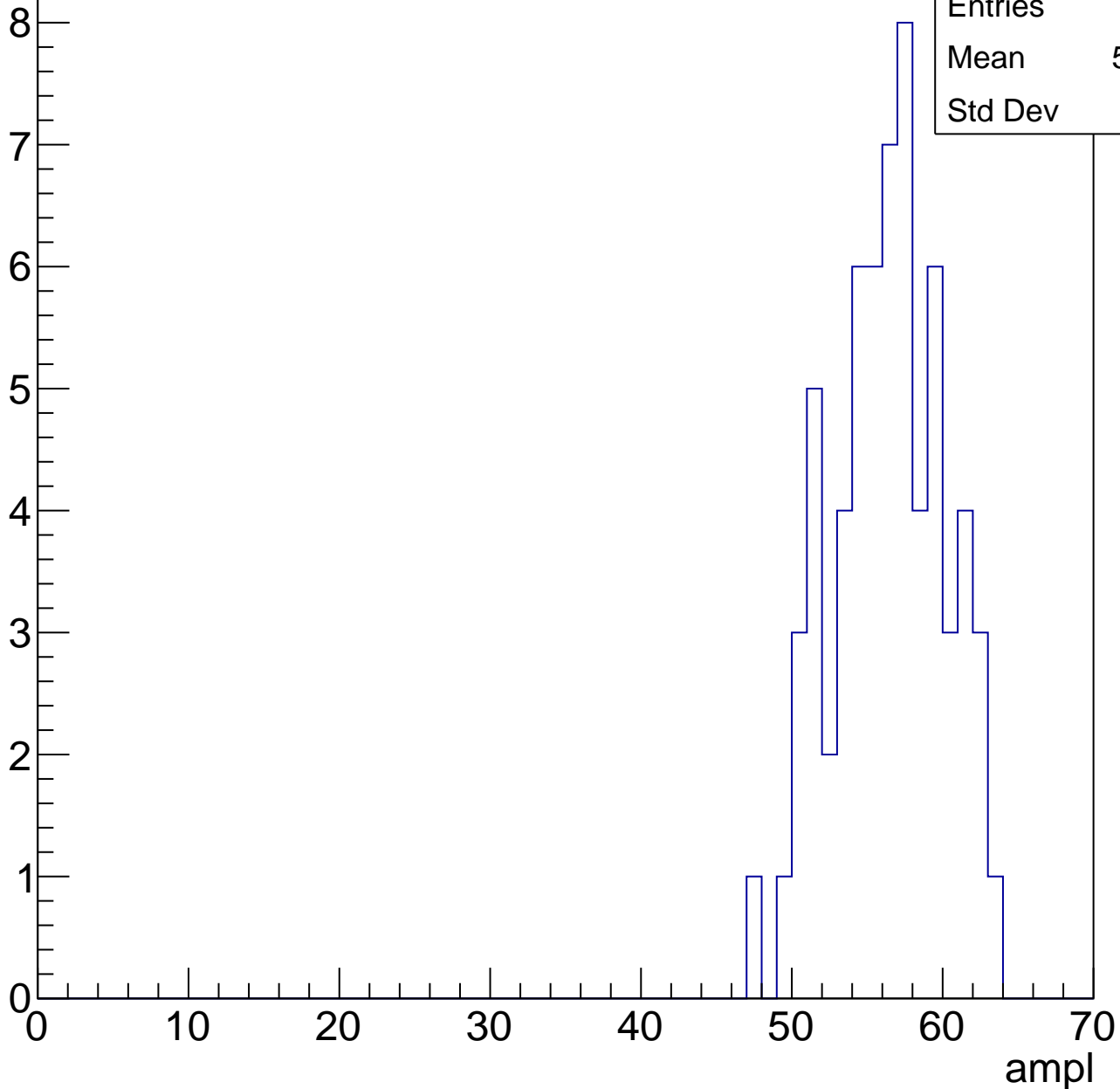


# B1L103S, U1-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	55.91
Std Dev	3.63

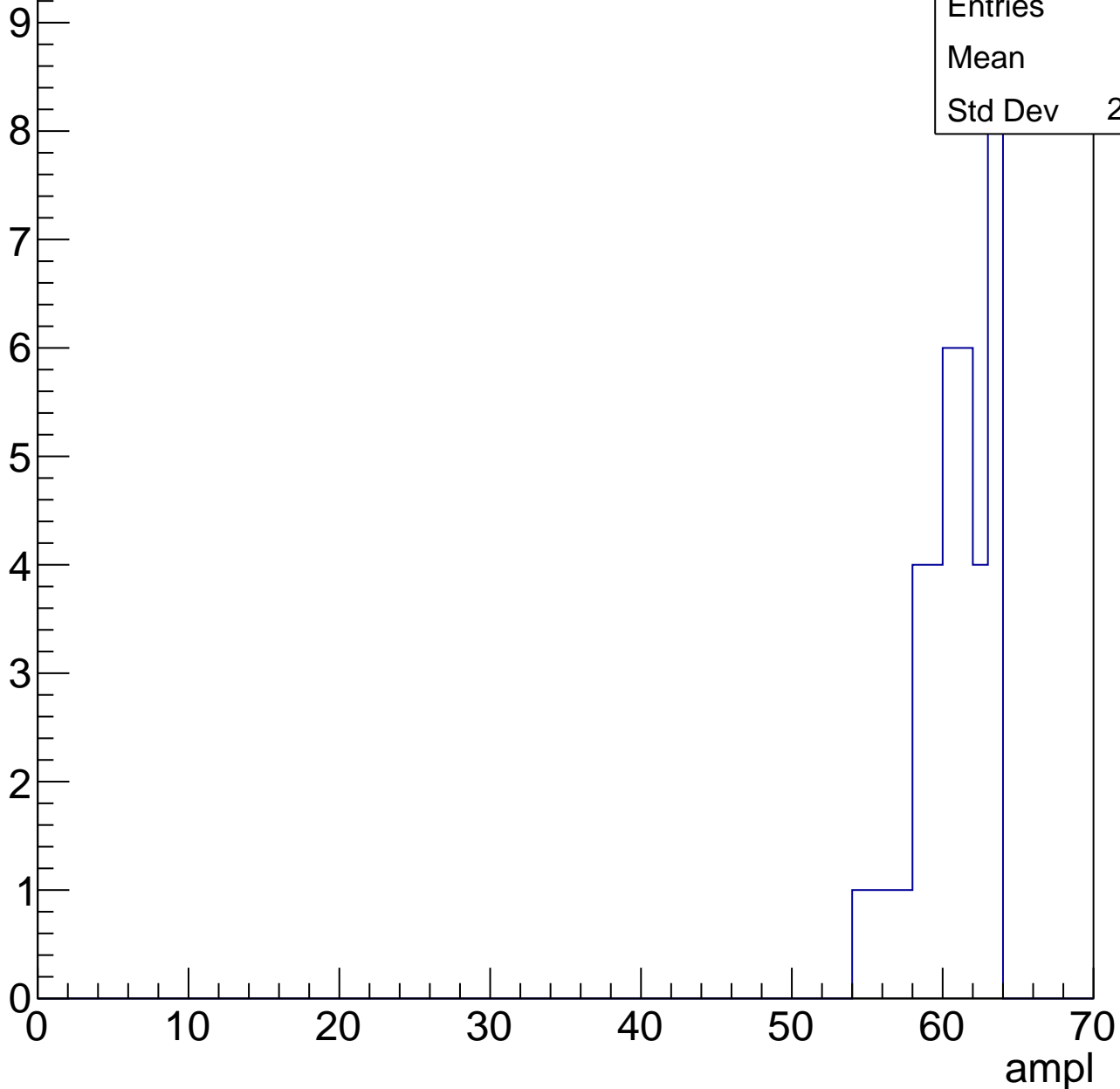


# B1L103S, U1-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	37
Mean	60.3
Std Dev	2.358

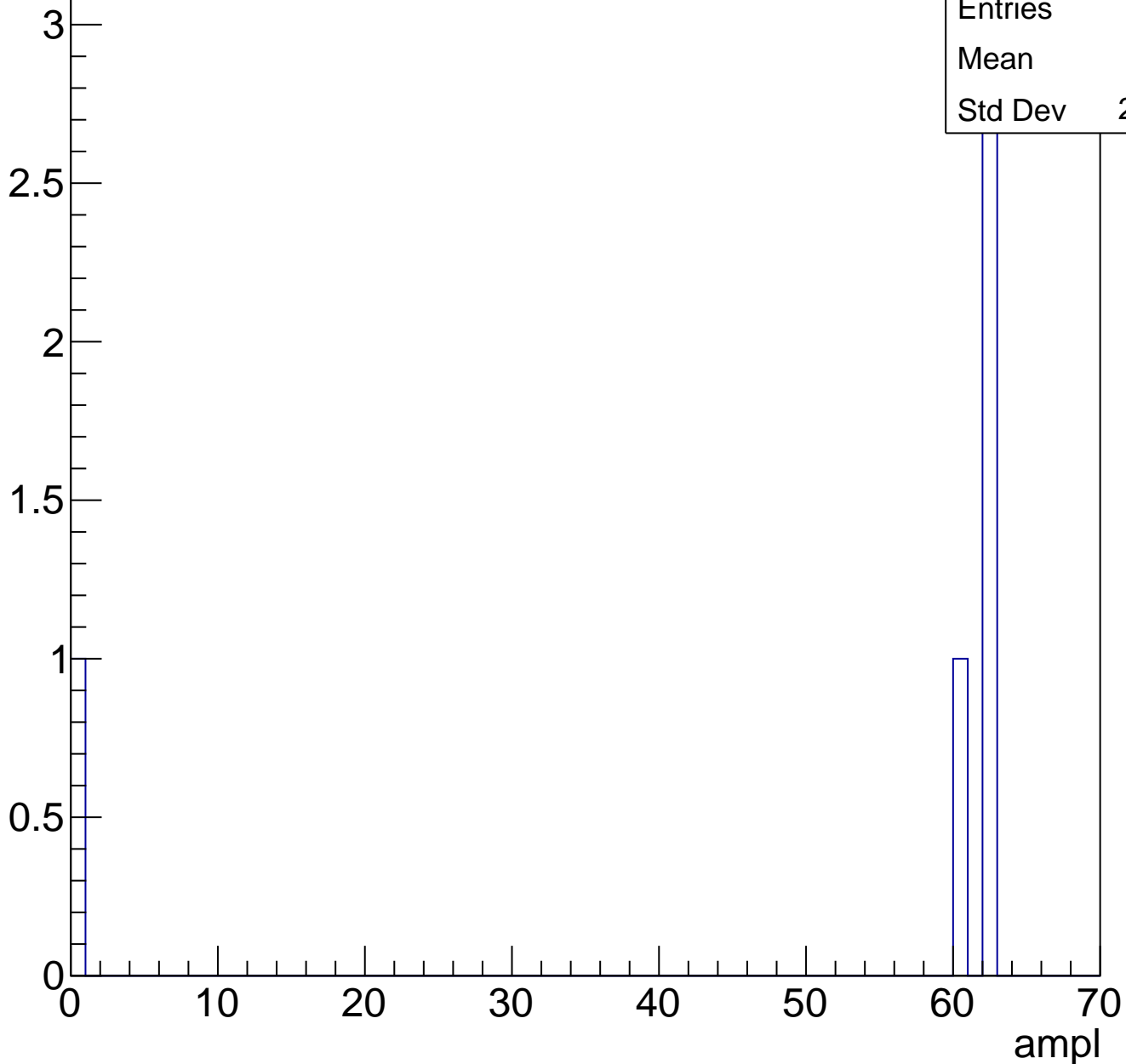




# B1L103S, U1-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch117, adc0

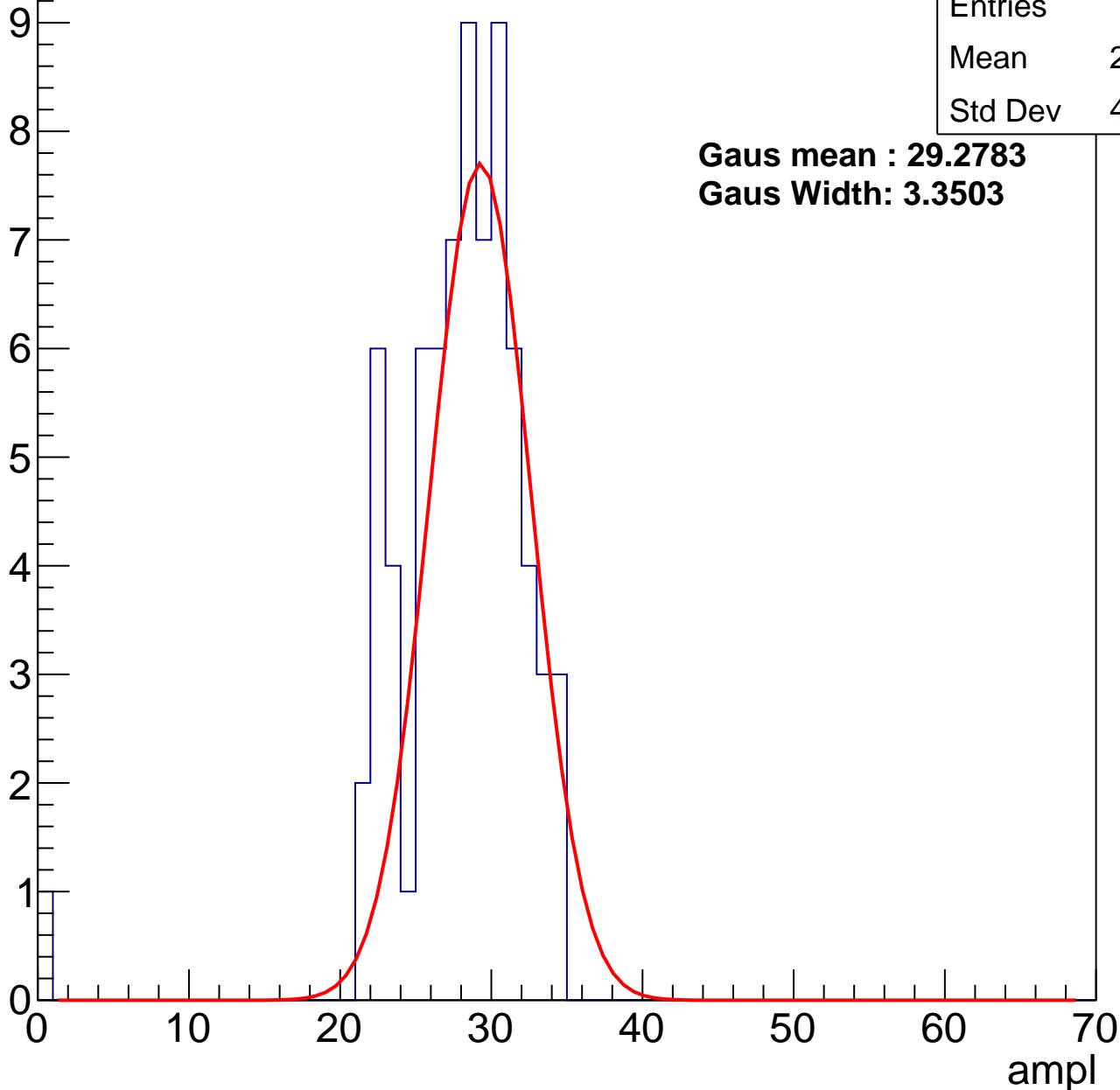
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	27.36
Std Dev	4.669

**Gaus mean : 29.2783**

**Gaus Width: 3.3503**



# B1L103S, U1-ch117, adc1

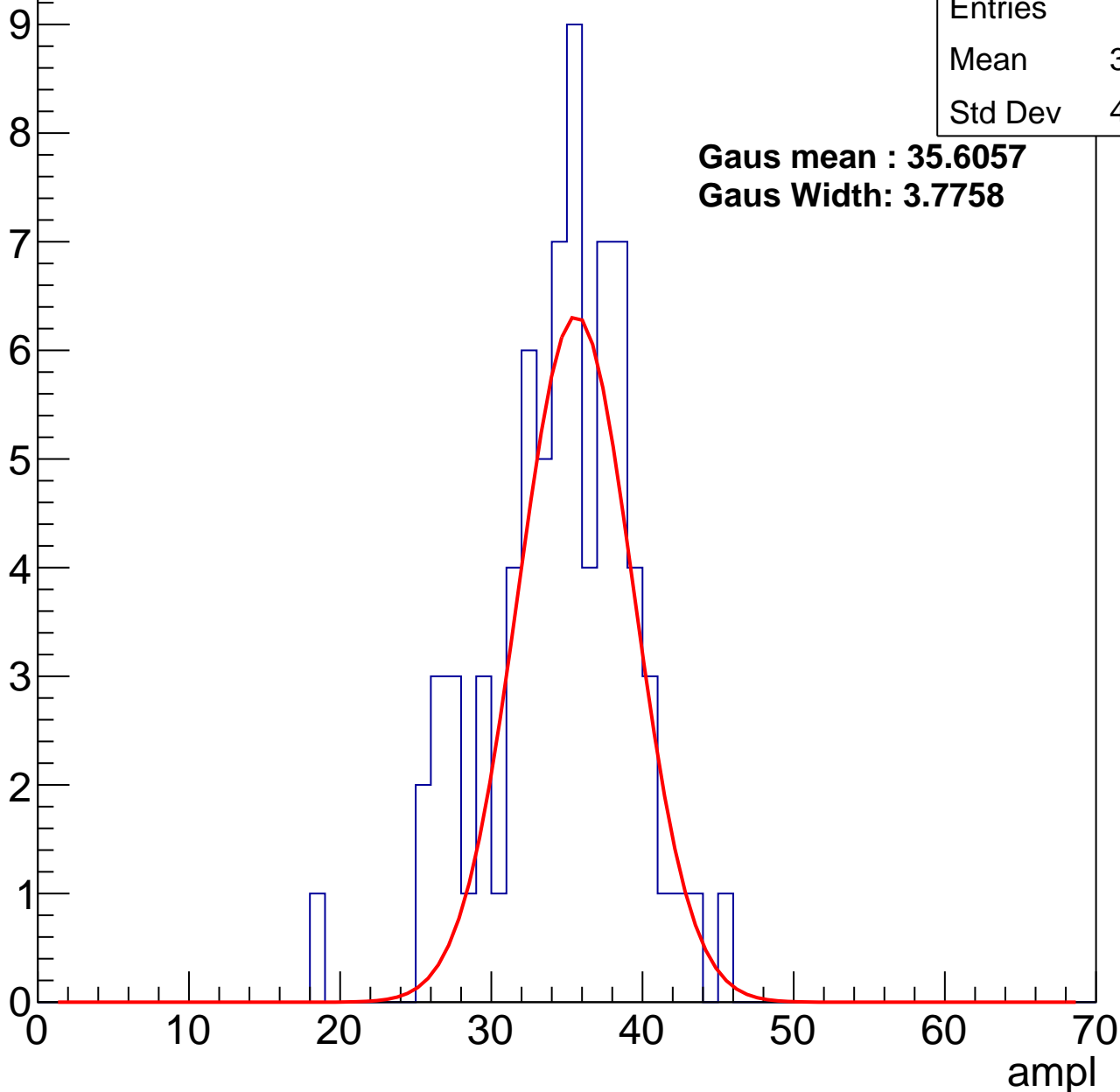
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	34.08
Std Dev	4.753

**Gaus mean : 35.6057**

**Gaus Width: 3.7758**



# B1L103S, U1-ch117, adc2

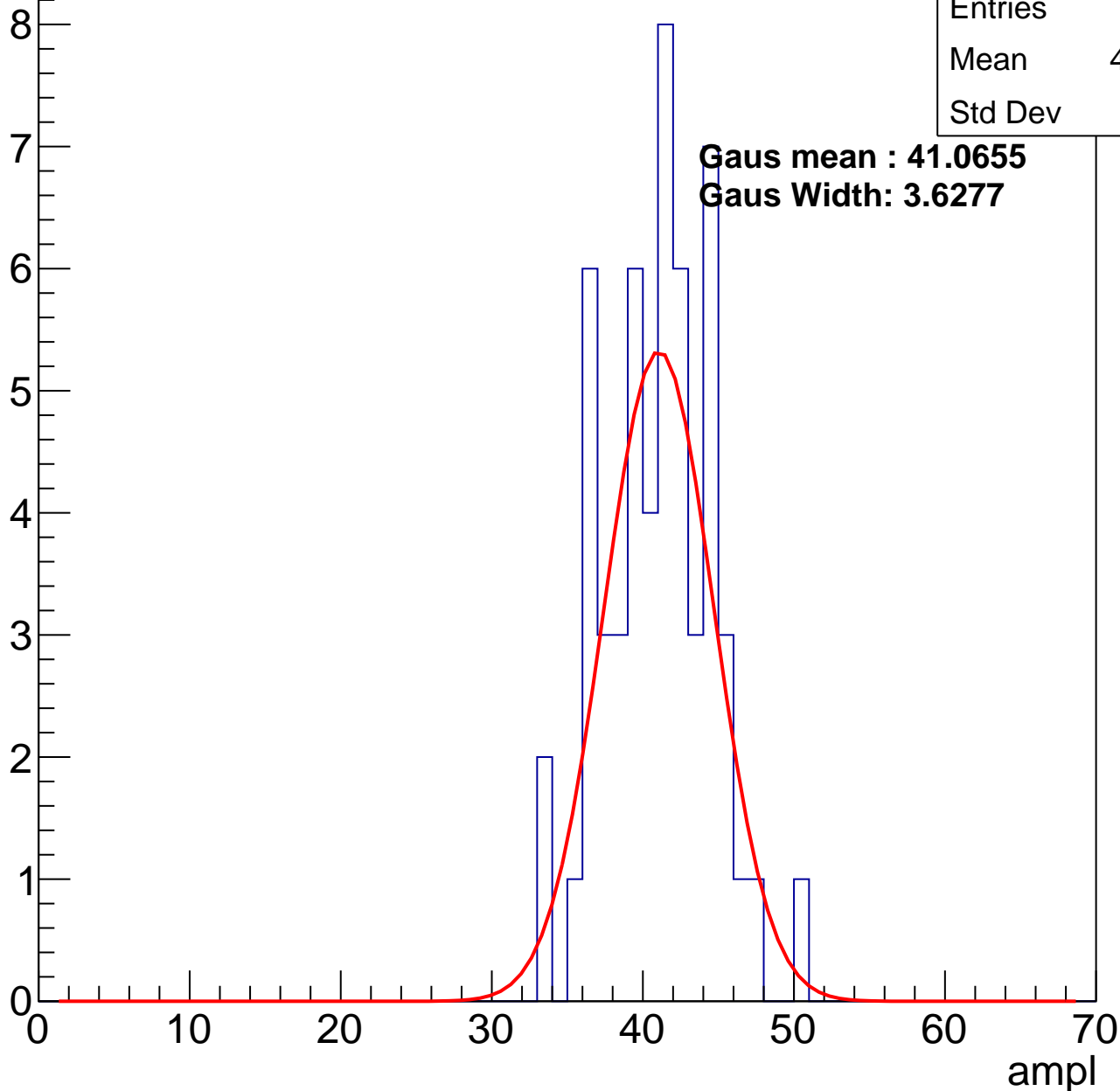
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	40.56
Std Dev	3.51

**Gaus mean : 41.0655**

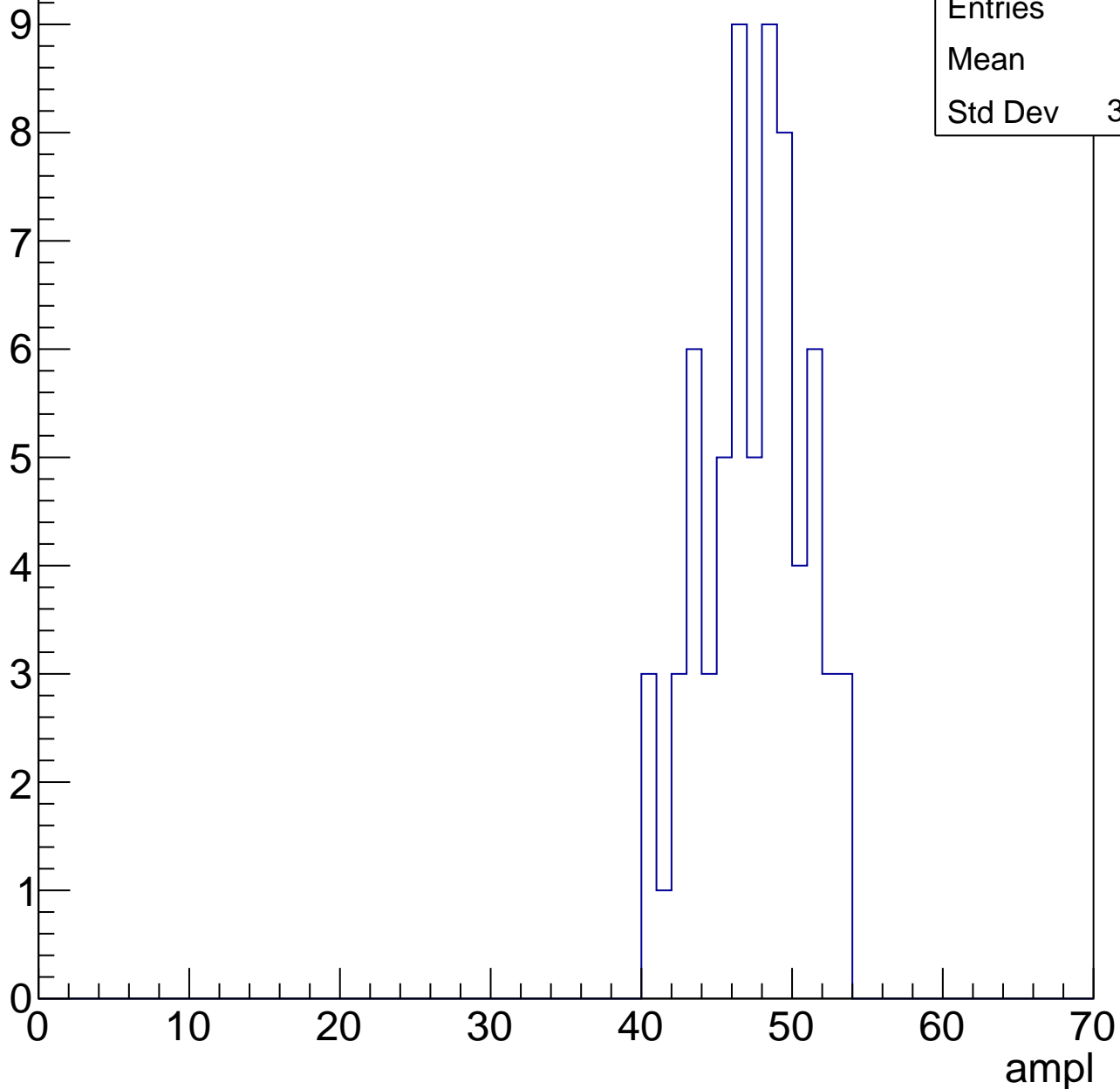
**Gaus Width: 3.6277**



# B1L103S, U1-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



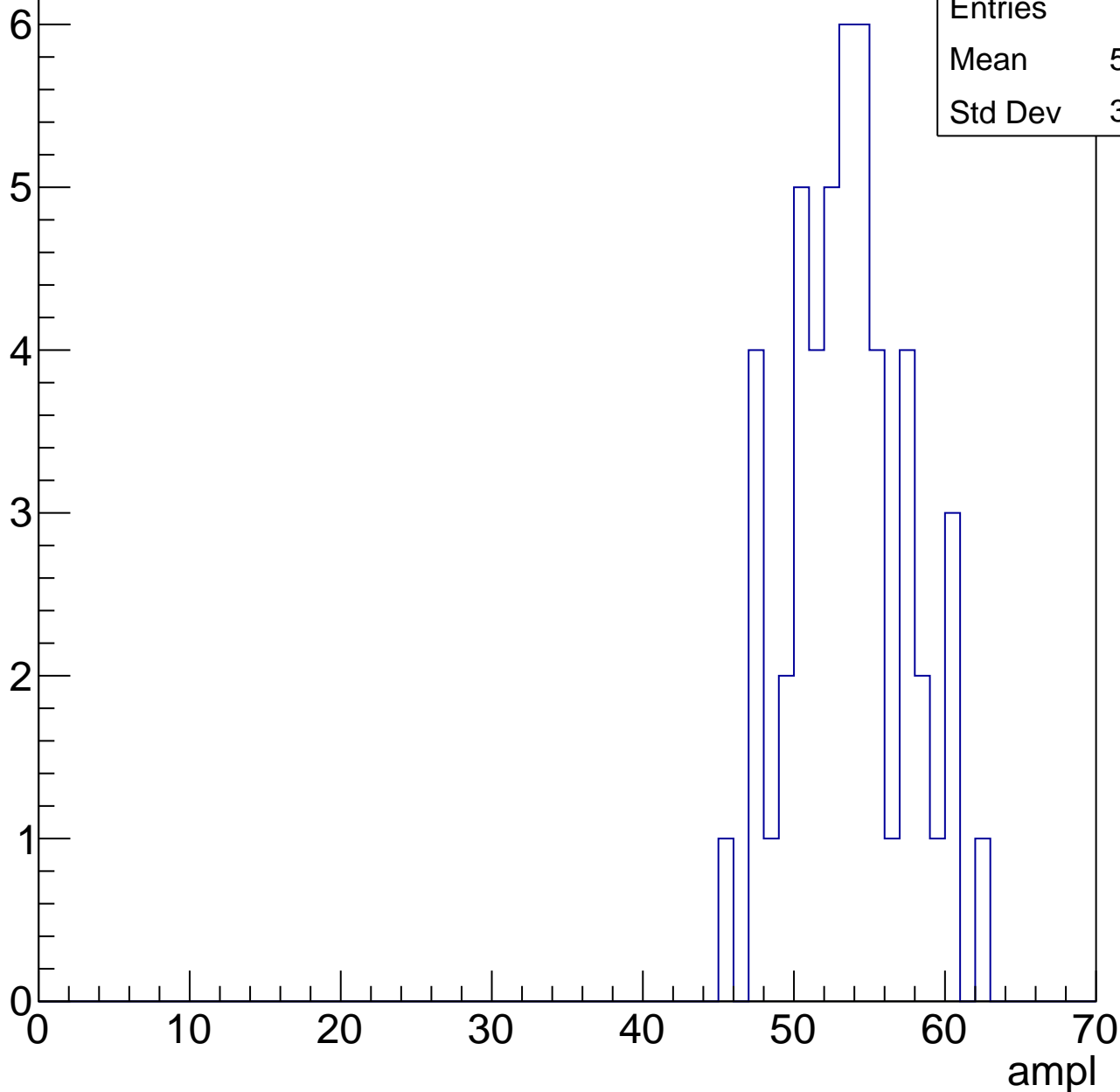
Entries	68
Mean	47
Std Dev	3.356

# B1L103S, U1-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	53.12
Std Dev	3.845

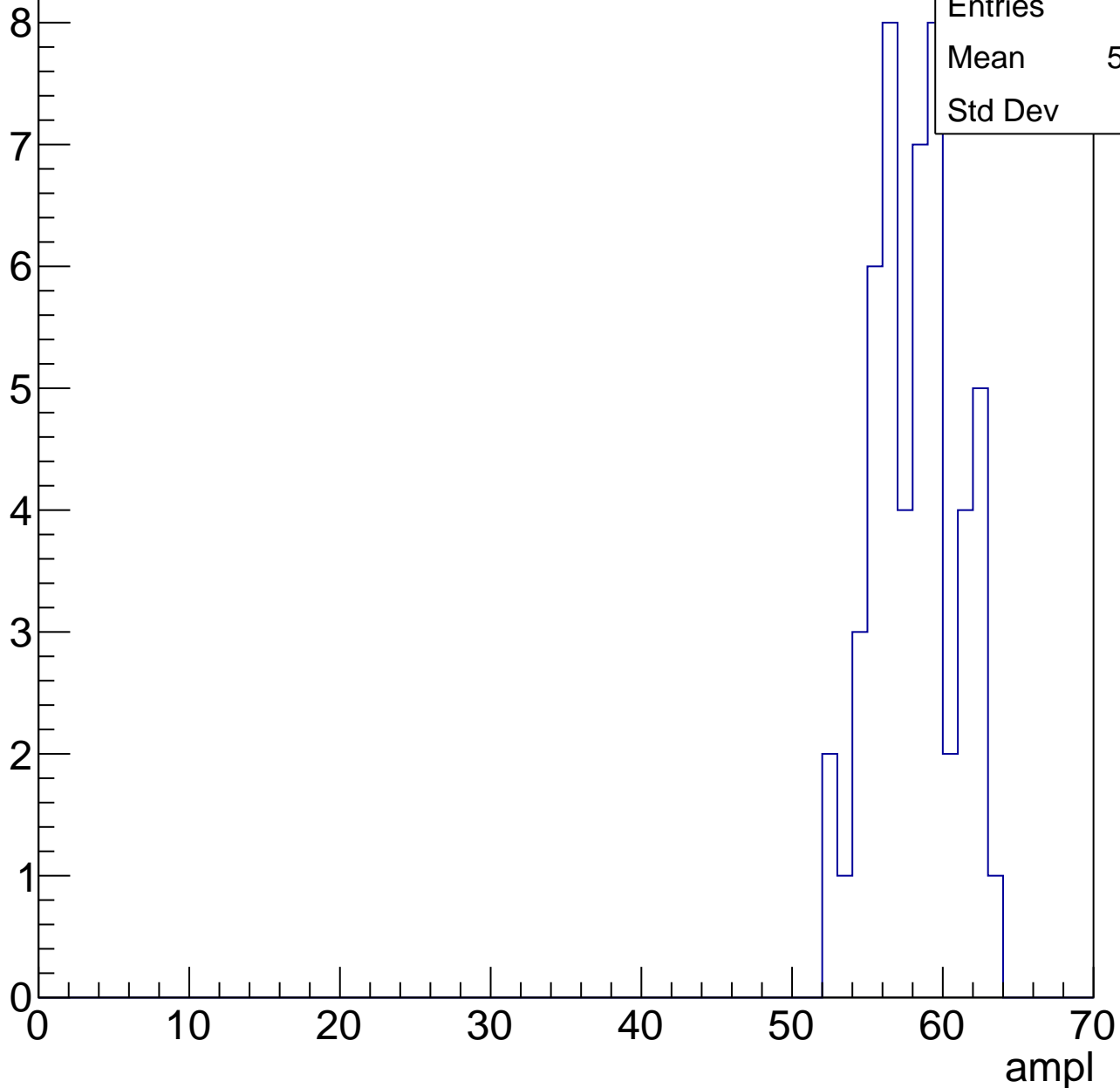


# B1L103S, U1-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	57.65
Std Dev	2.75

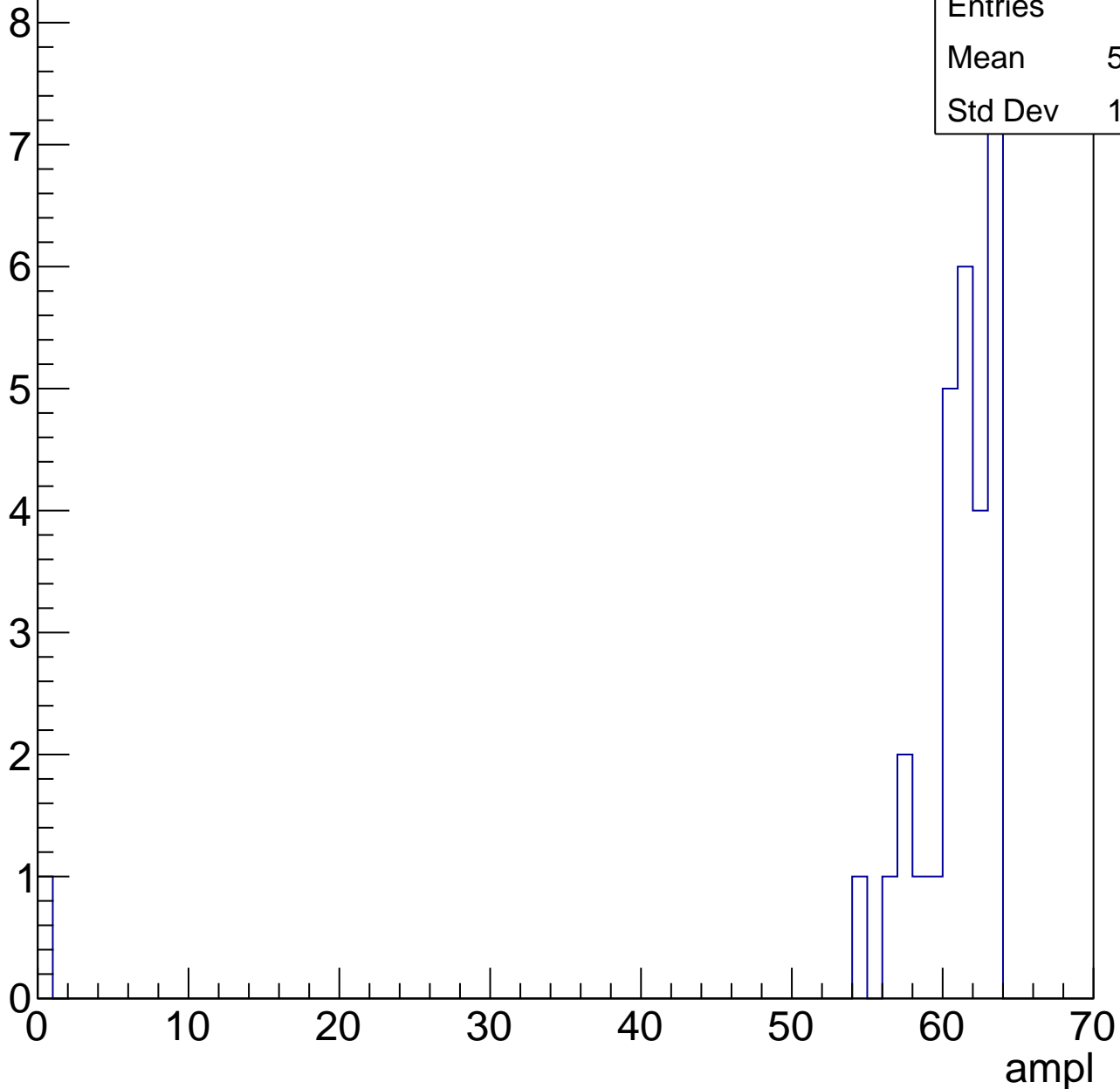


# B1L103S, U1-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	30
Mean	58.63
Std Dev	11.12

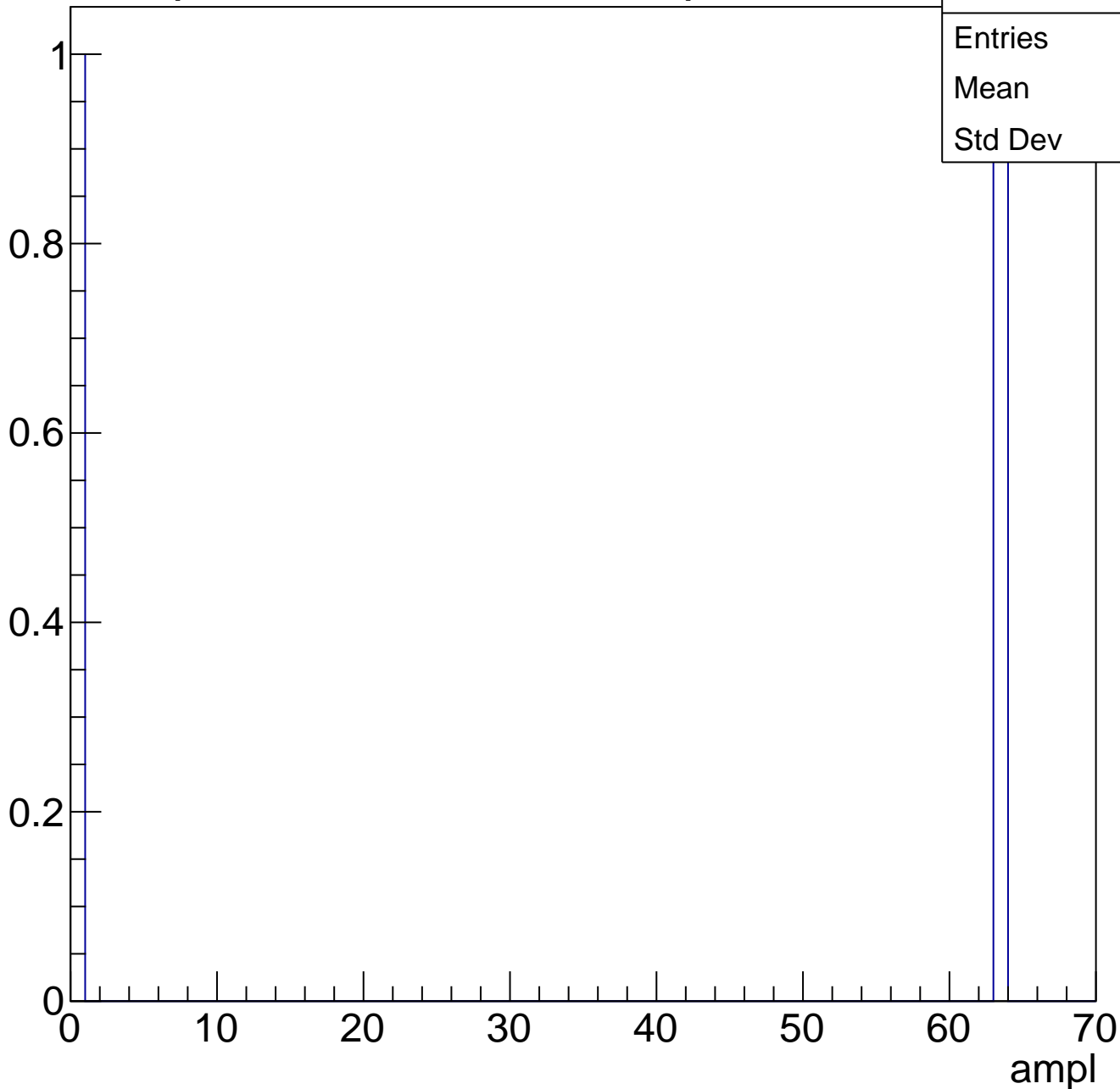




# B1L103S, U1-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch118, adc0

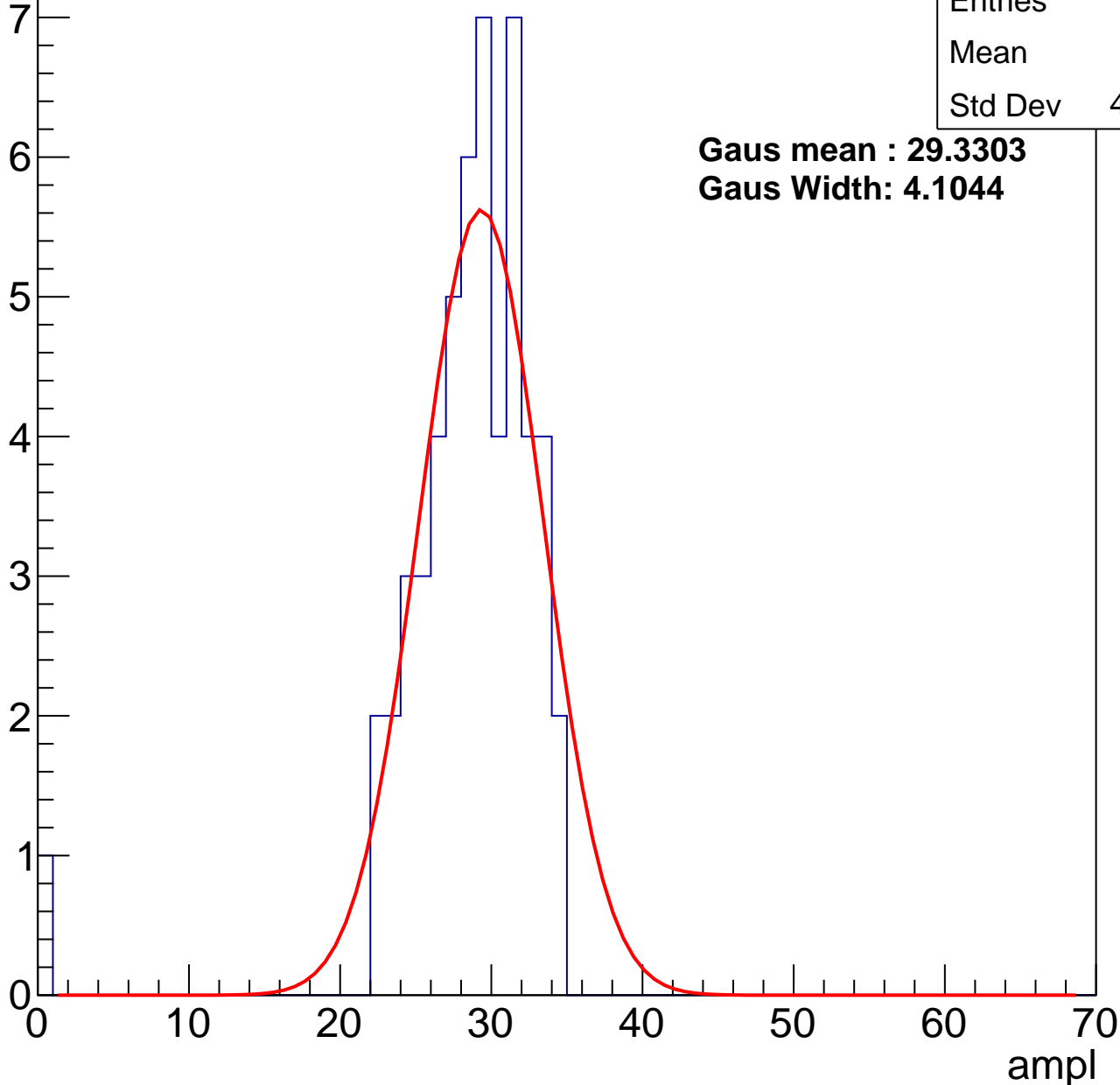
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	28
Std Dev	4.952

**Gaus mean : 29.3303**

**Gaus Width: 4.1044**



# B1L103S, U1-ch118, adc1

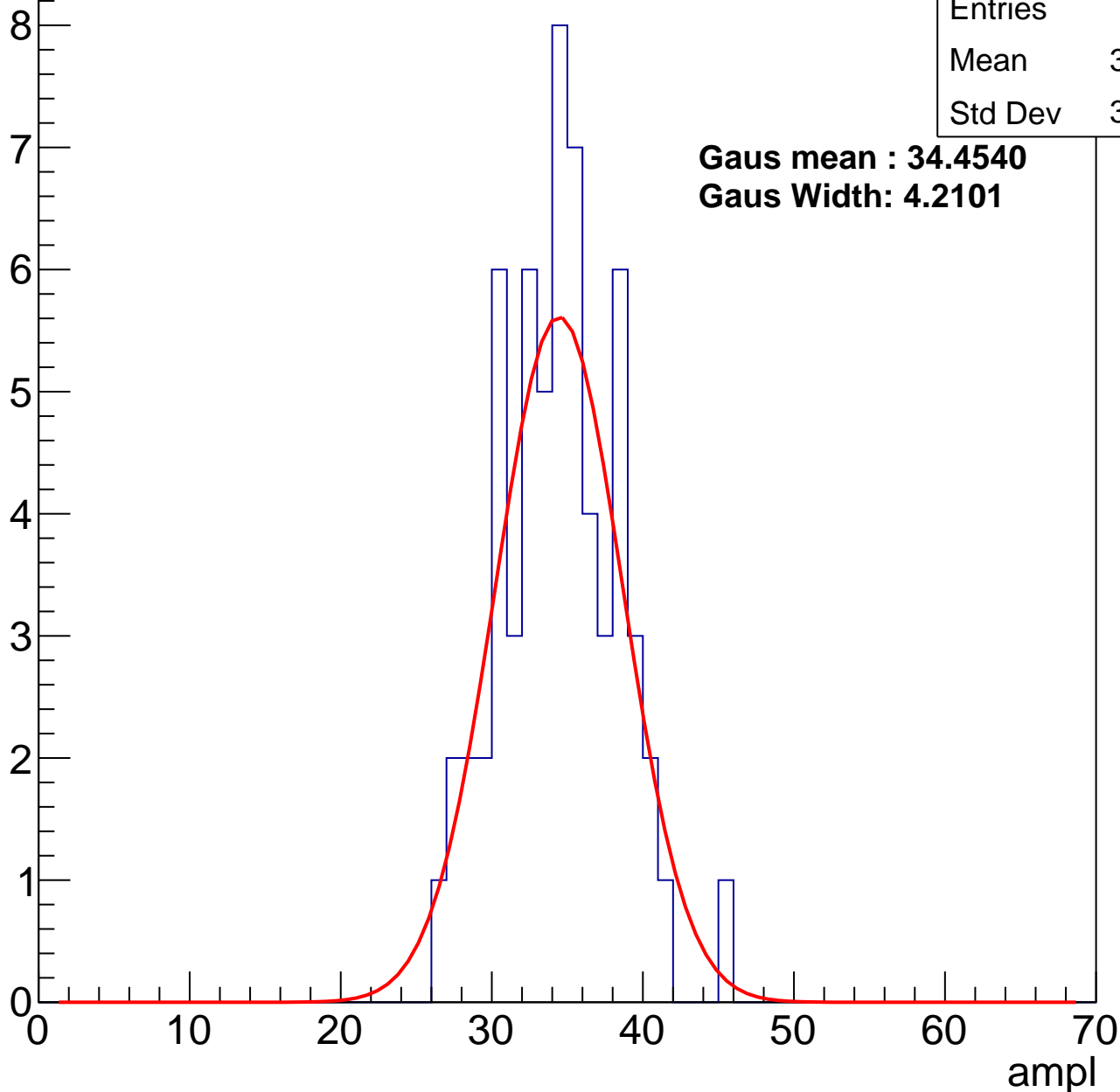
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	33.98
Std Dev	3.808

**Gaus mean : 34.4540**

**Gaus Width: 4.2101**

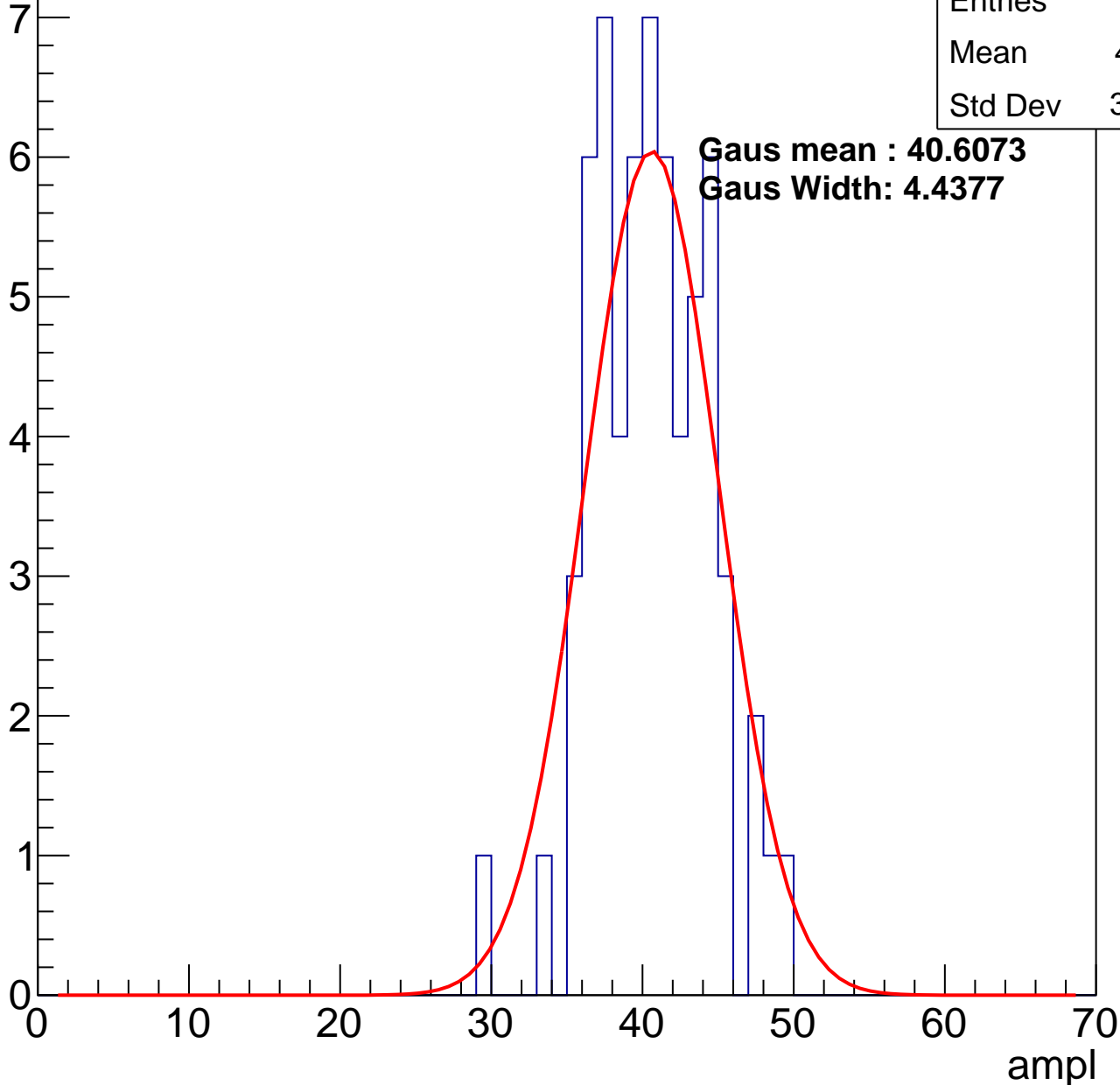


# B1L103S, U1-ch118, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	40.11
Std Dev	3.793

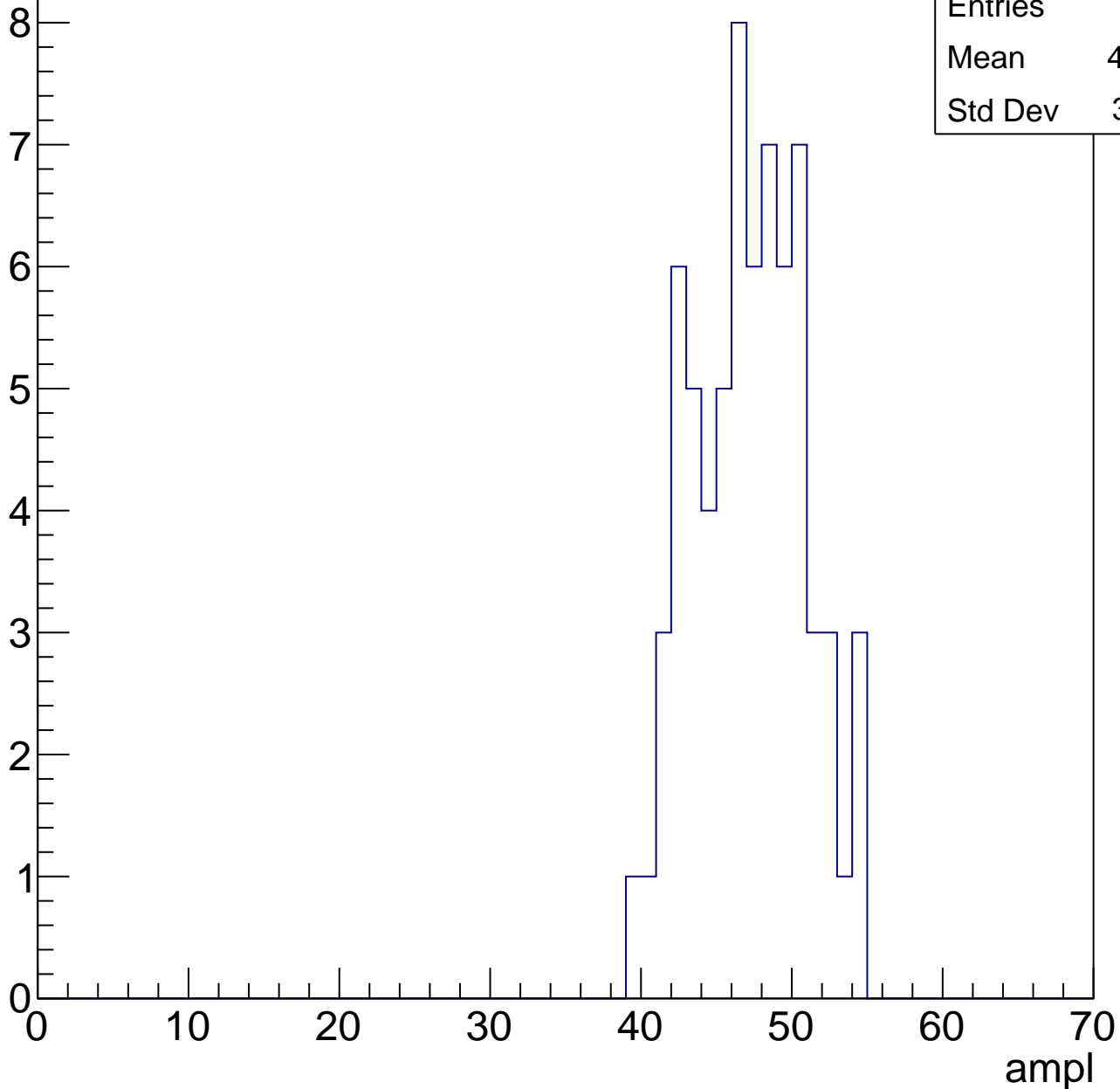


# B1L103S, U1-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	46.72
Std Dev	3.631

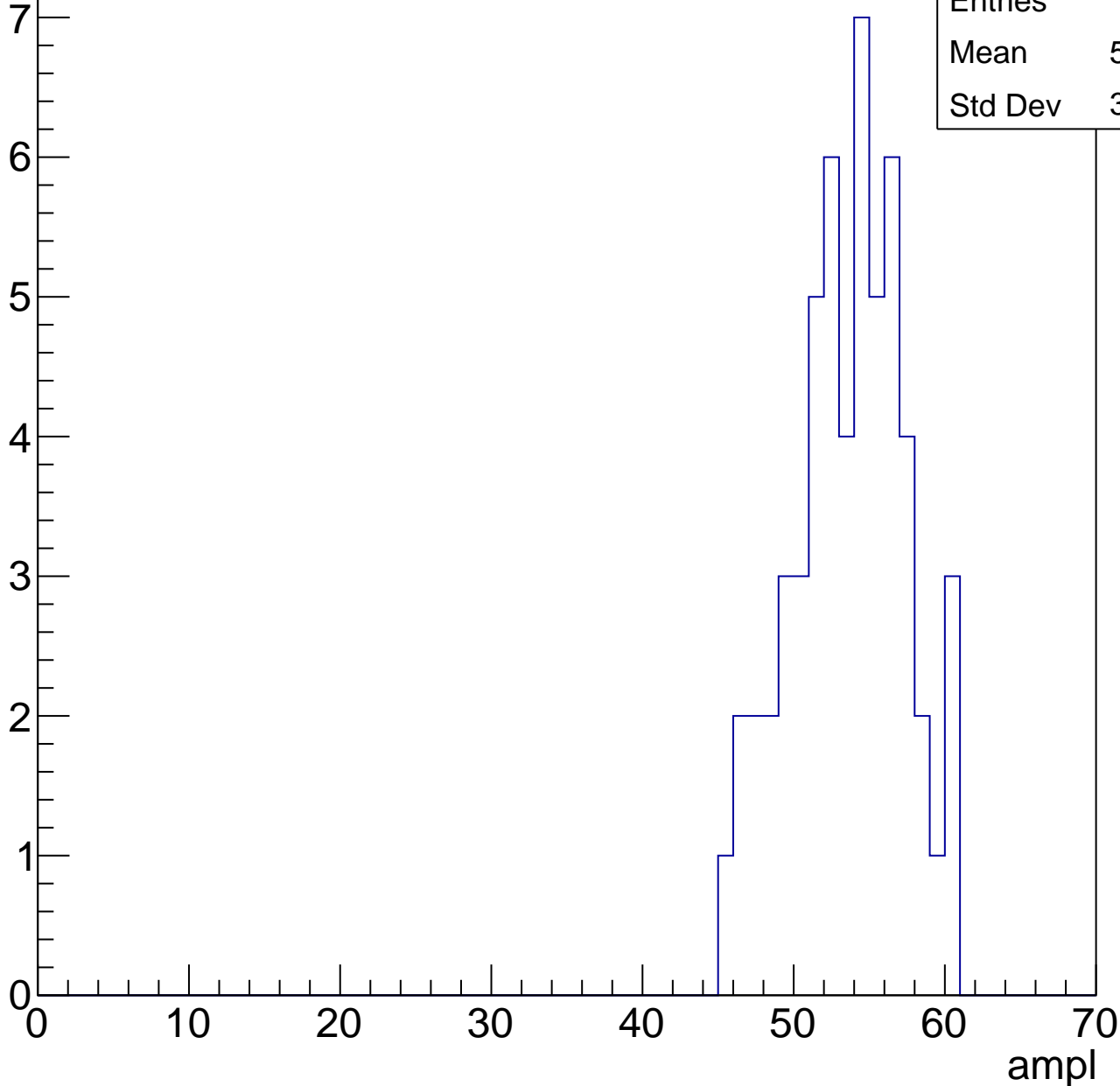


# B1L103S, U1-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	53.12
Std Dev	3.689

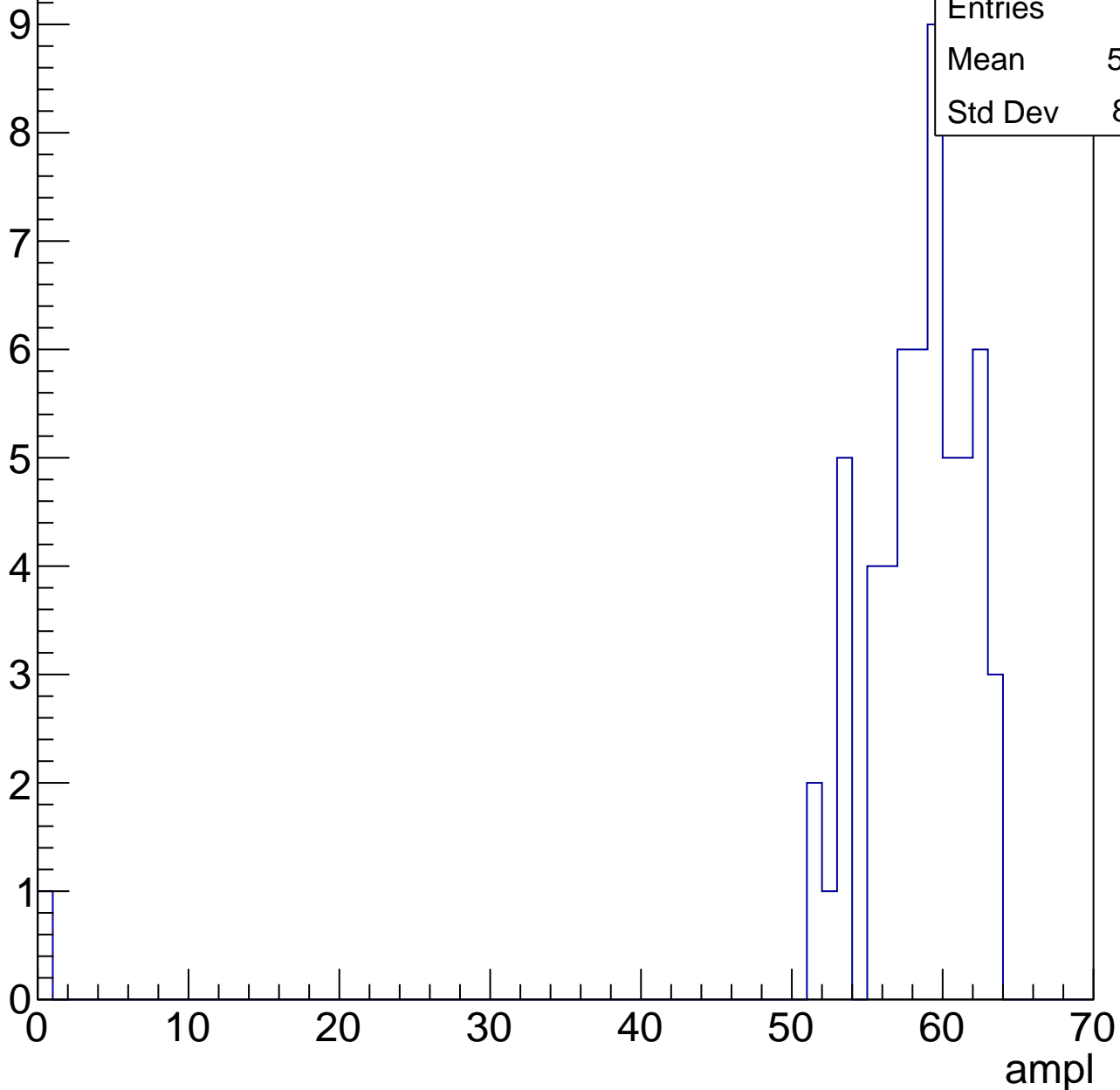


# B1L103S, U1-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	57.02
Std Dev	8.241

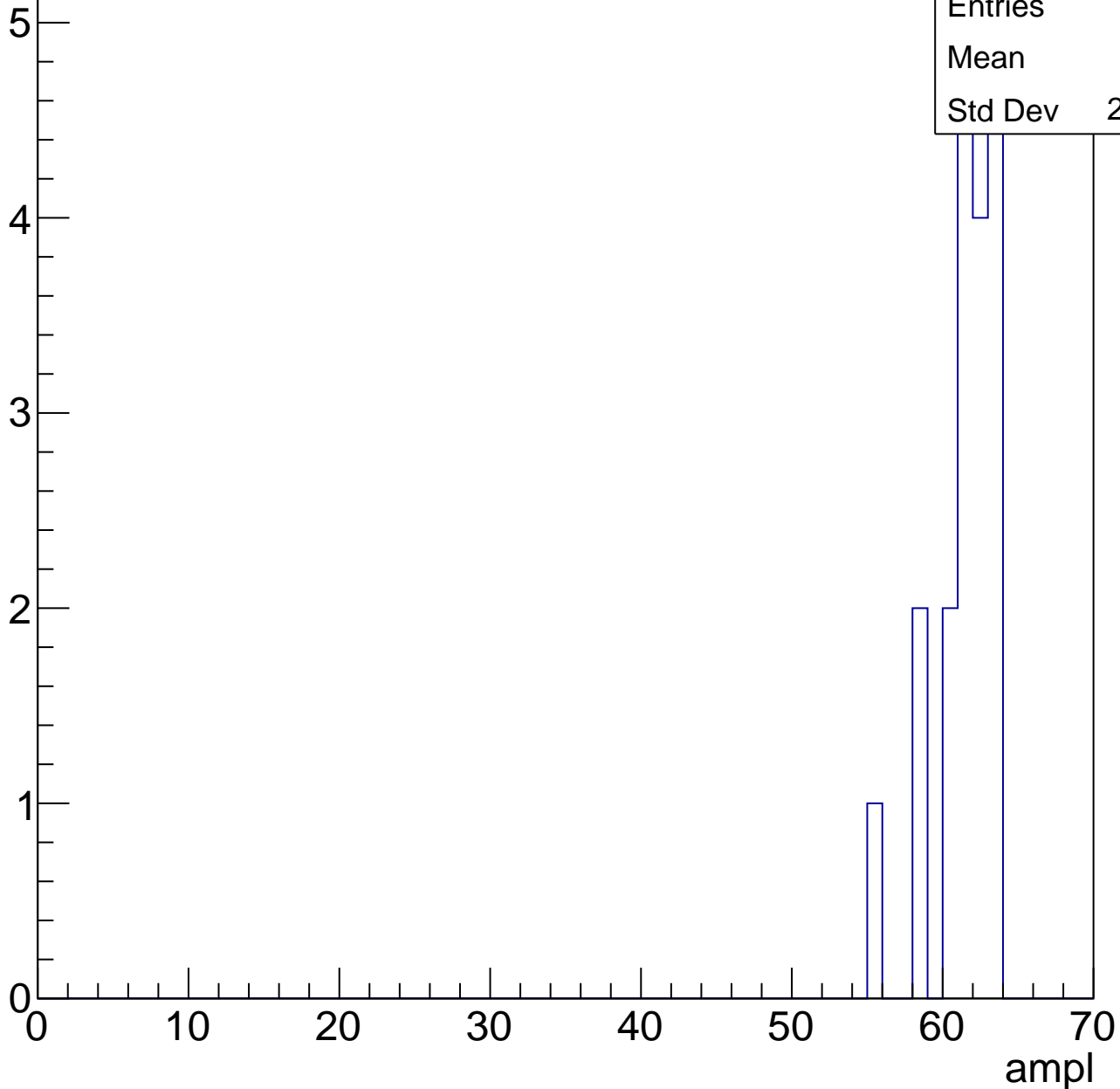


# B1L103S, U1-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	19
Mean	61
Std Dev	2.052





# B1L103S, U1-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	63
Std Dev	0

# B1L103S, U1-ch119, adc0

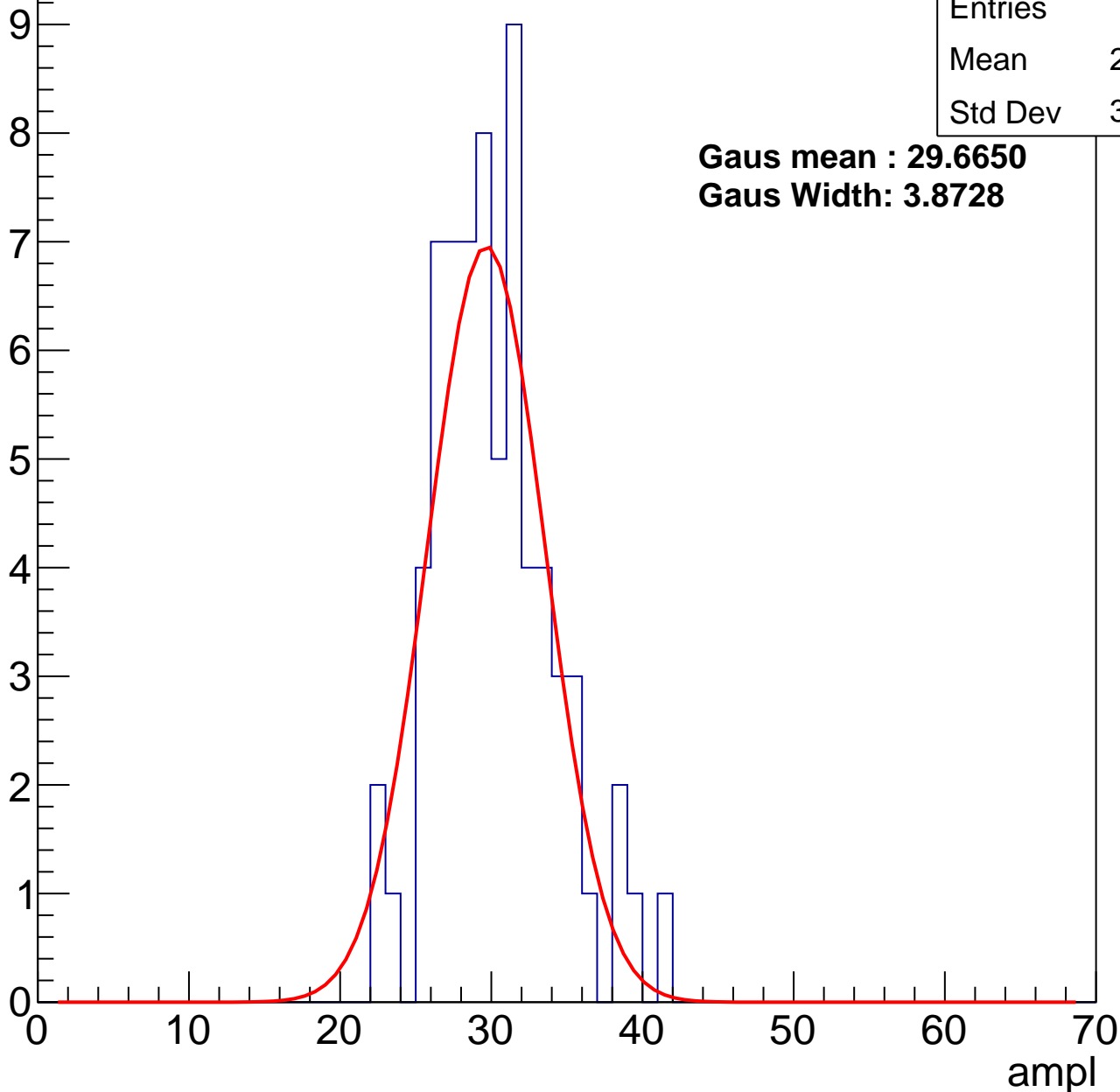
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	29.77
Std Dev	3.872

**Gaus mean : 29.6650**

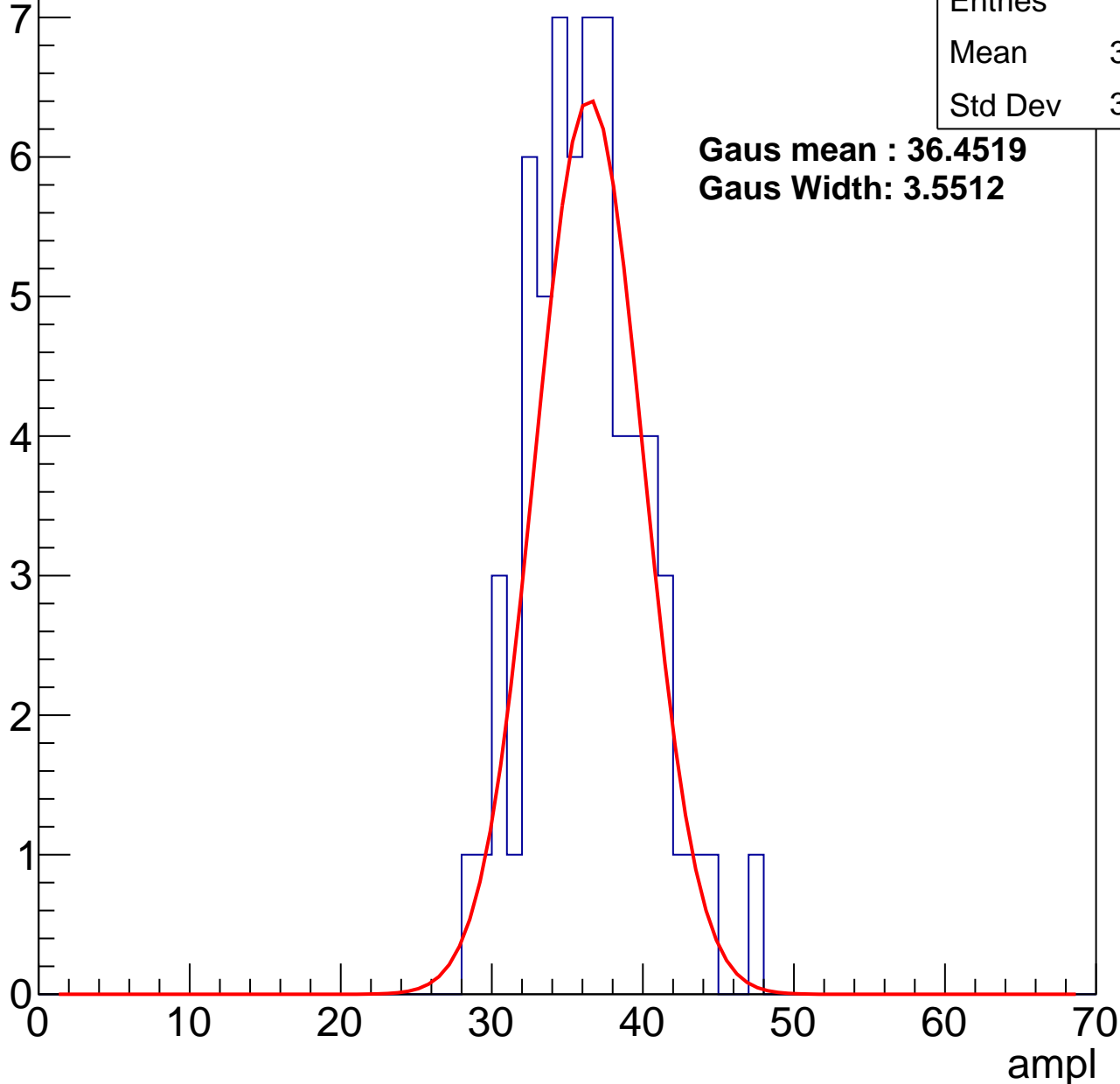
**Gaus Width: 3.8728**



# B1L103S, U1-ch119, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch119, adc2

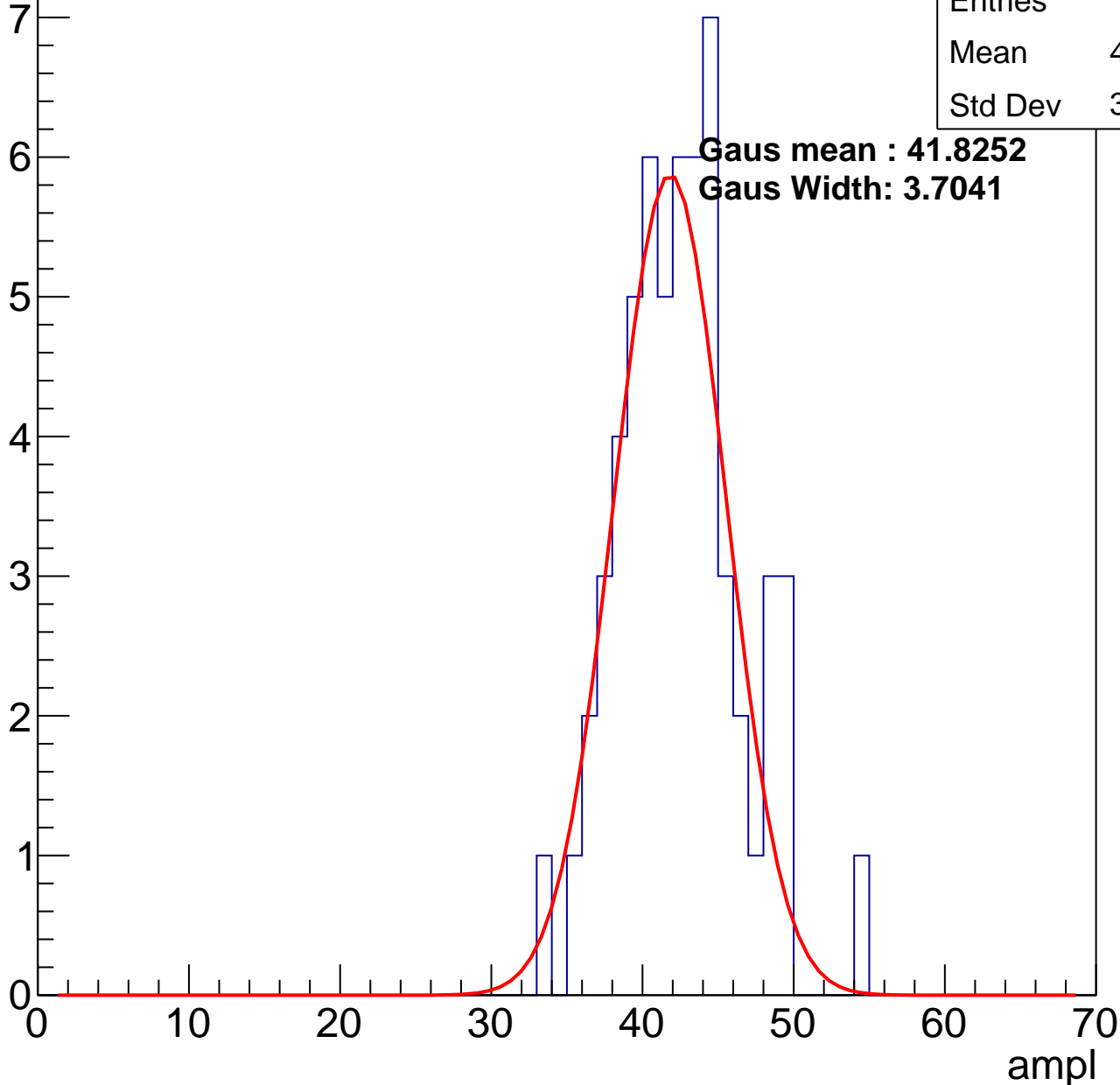
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	42.03
Std Dev	3.974

**Gaus mean : 41.8252**

**Gaus Width: 3.7041**

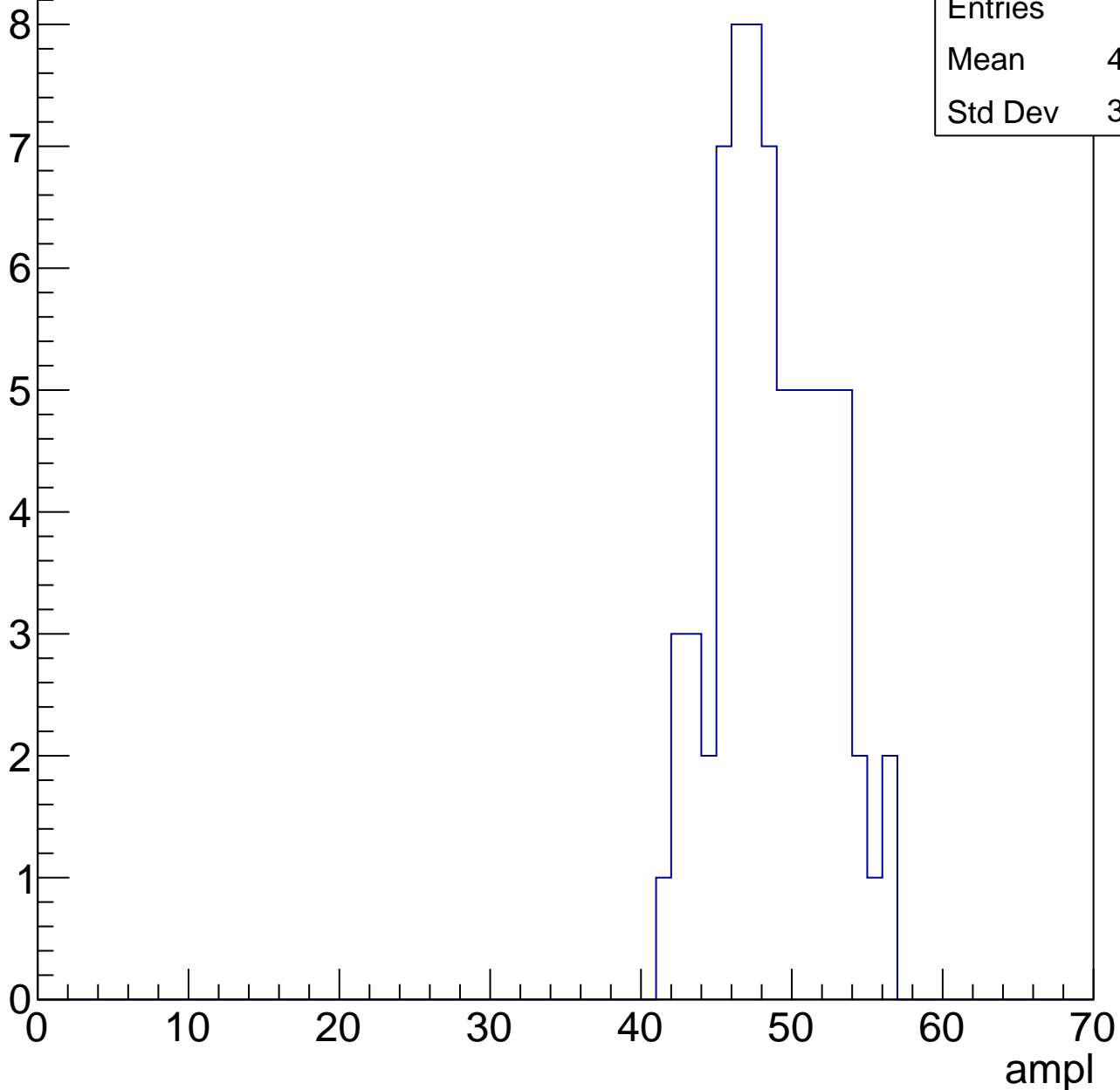


# B1L103S, U1-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	48.25
Std Dev	3.585

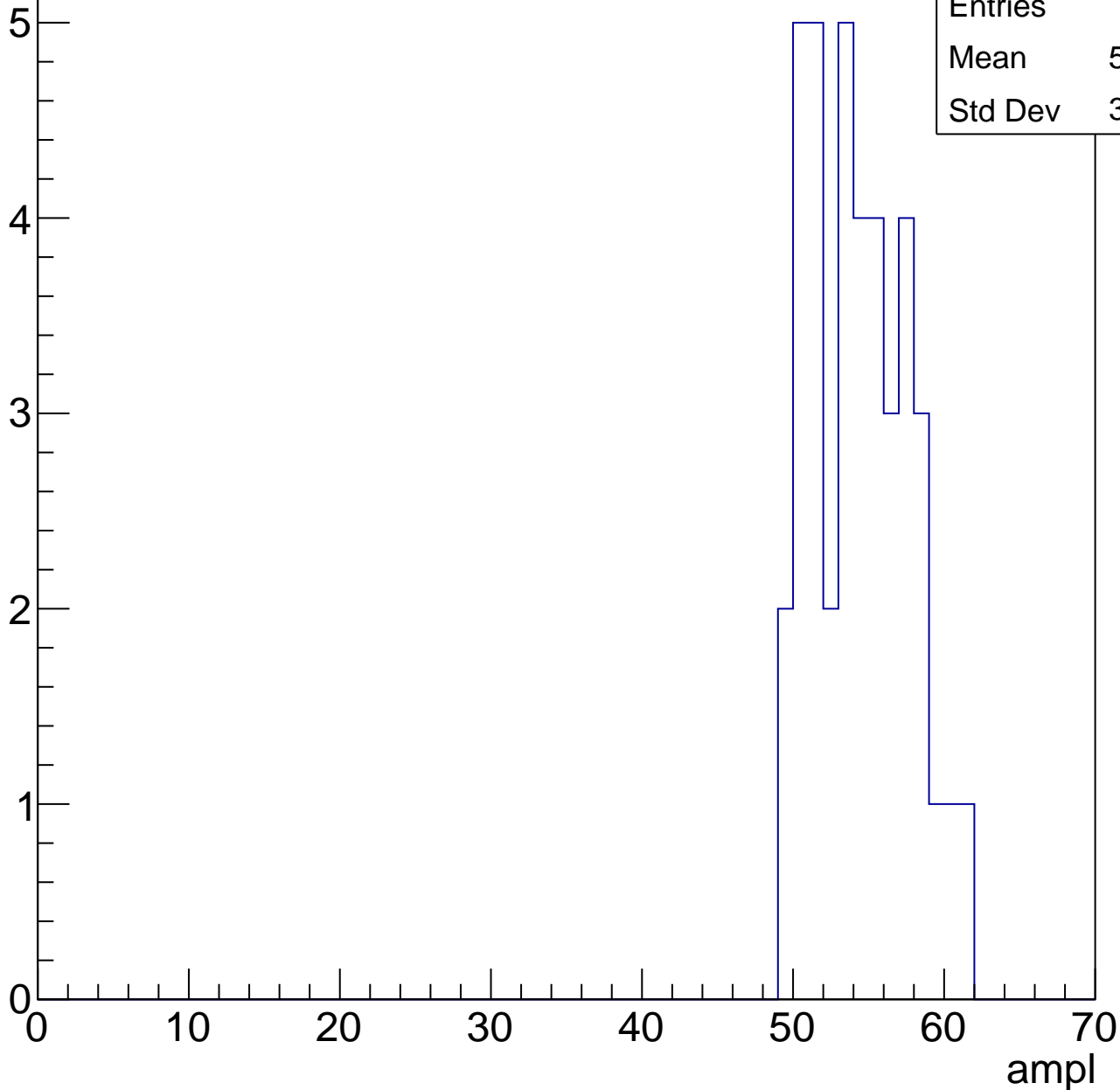


# B1L103S, U1-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	40
Mean	53.95
Std Dev	3.154

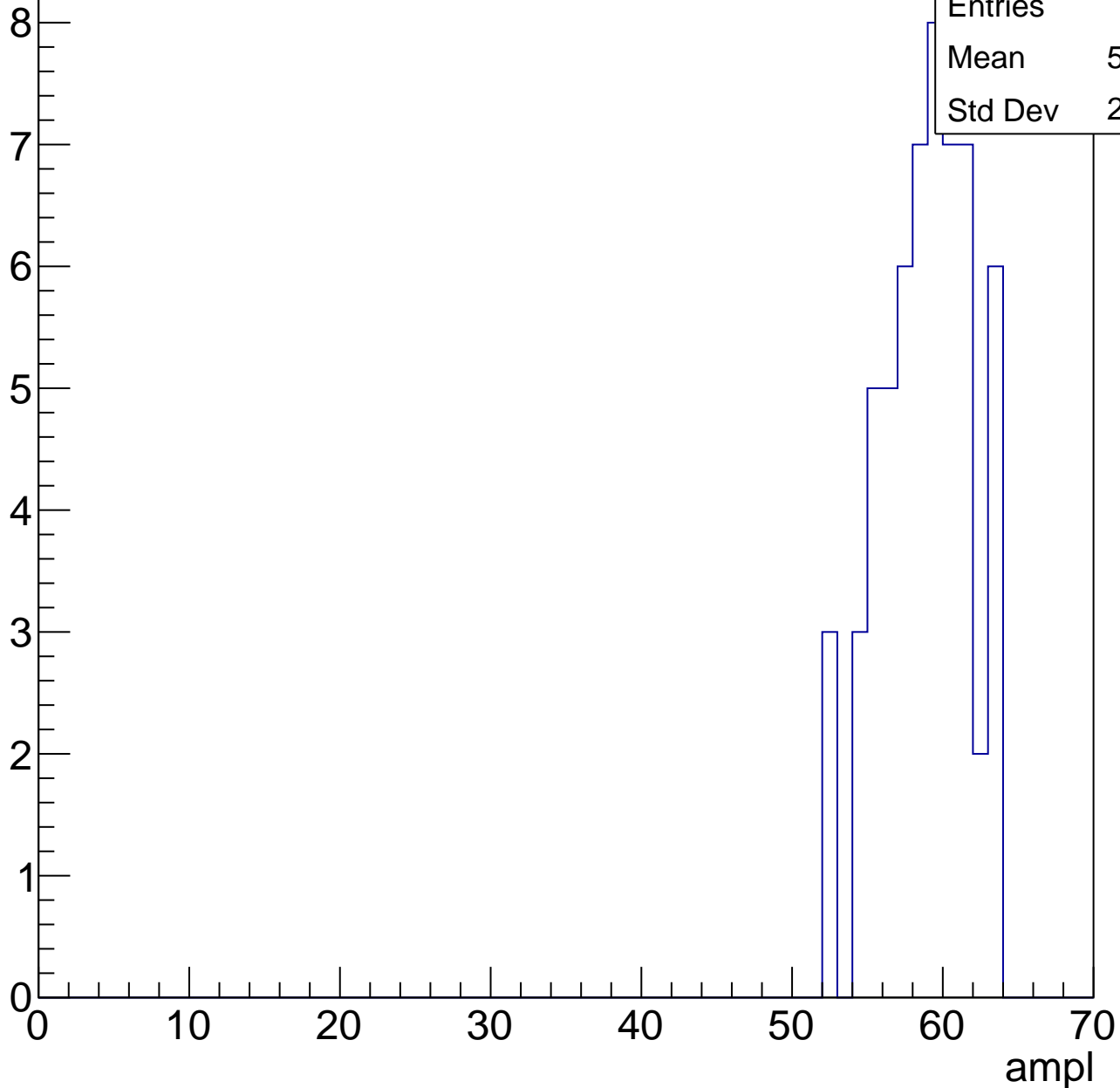


# B1L103S, U1-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	58.34
Std Dev	2.915

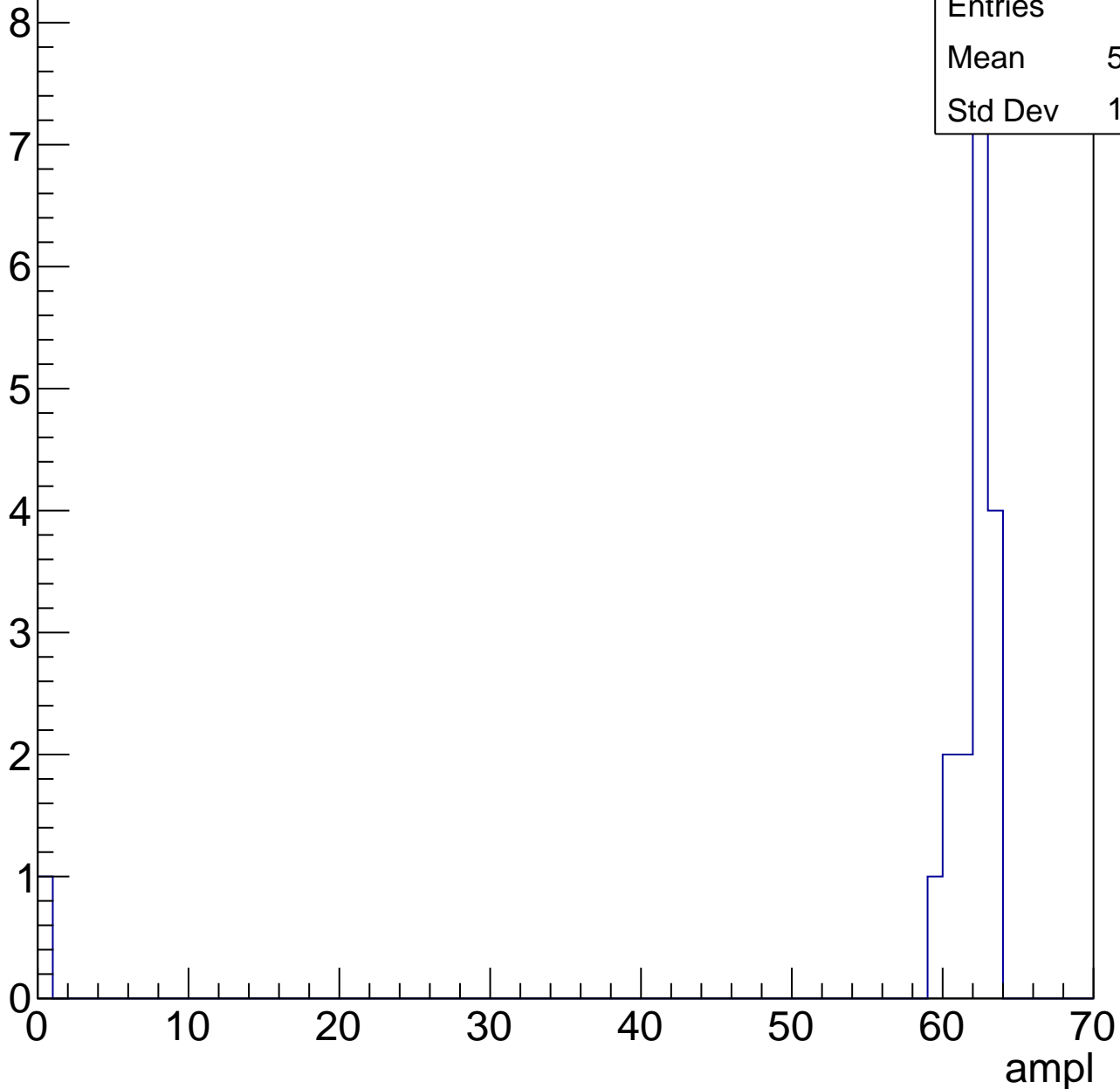


# B1L103S, U1-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	18
Mean	58.28
Std Dev	14.18





# B1L103S, U1-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	8.5
Std Dev	8.5

# B1L103S, U1-ch120, adc0

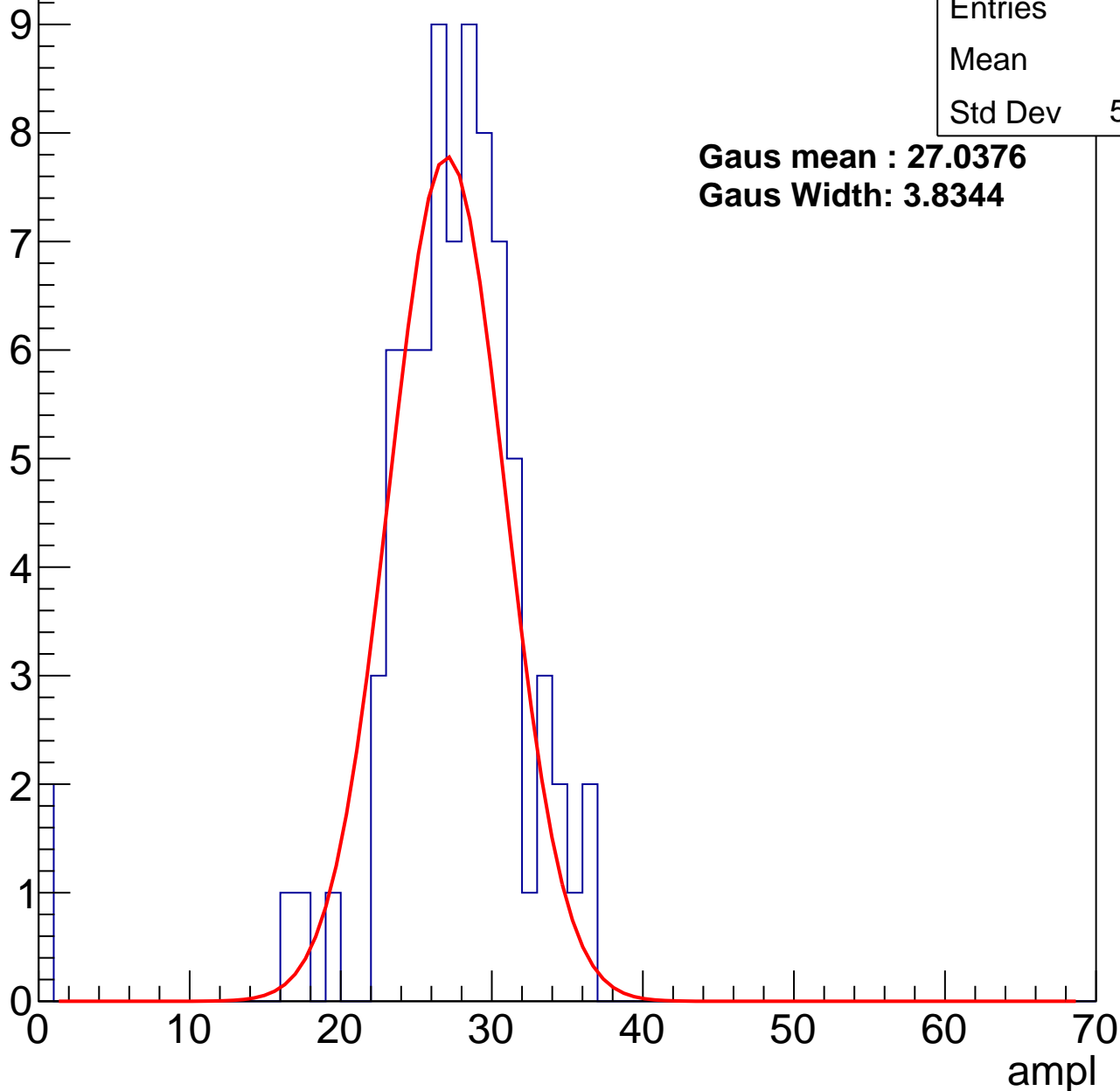
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	26.6
Std Dev	5.733

**Gaus mean : 27.0376**

**Gaus Width: 3.8344**



# B1L103S, U1-ch120, adc1

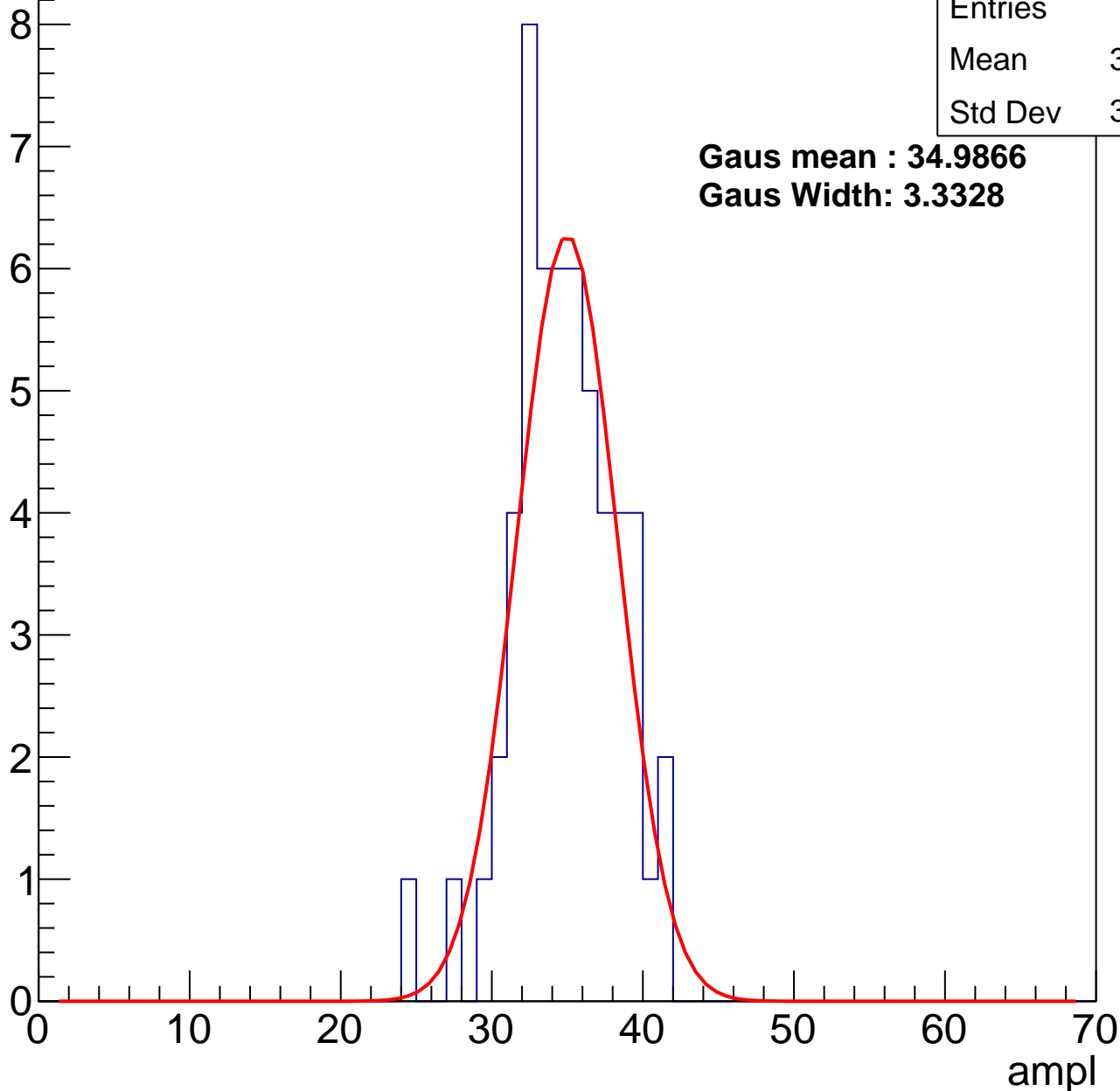
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	34.36
Std Dev	3.392

**Gaus mean : 34.9866**

**Gaus Width: 3.3328**



# B1L103S, U1-ch120, adc2

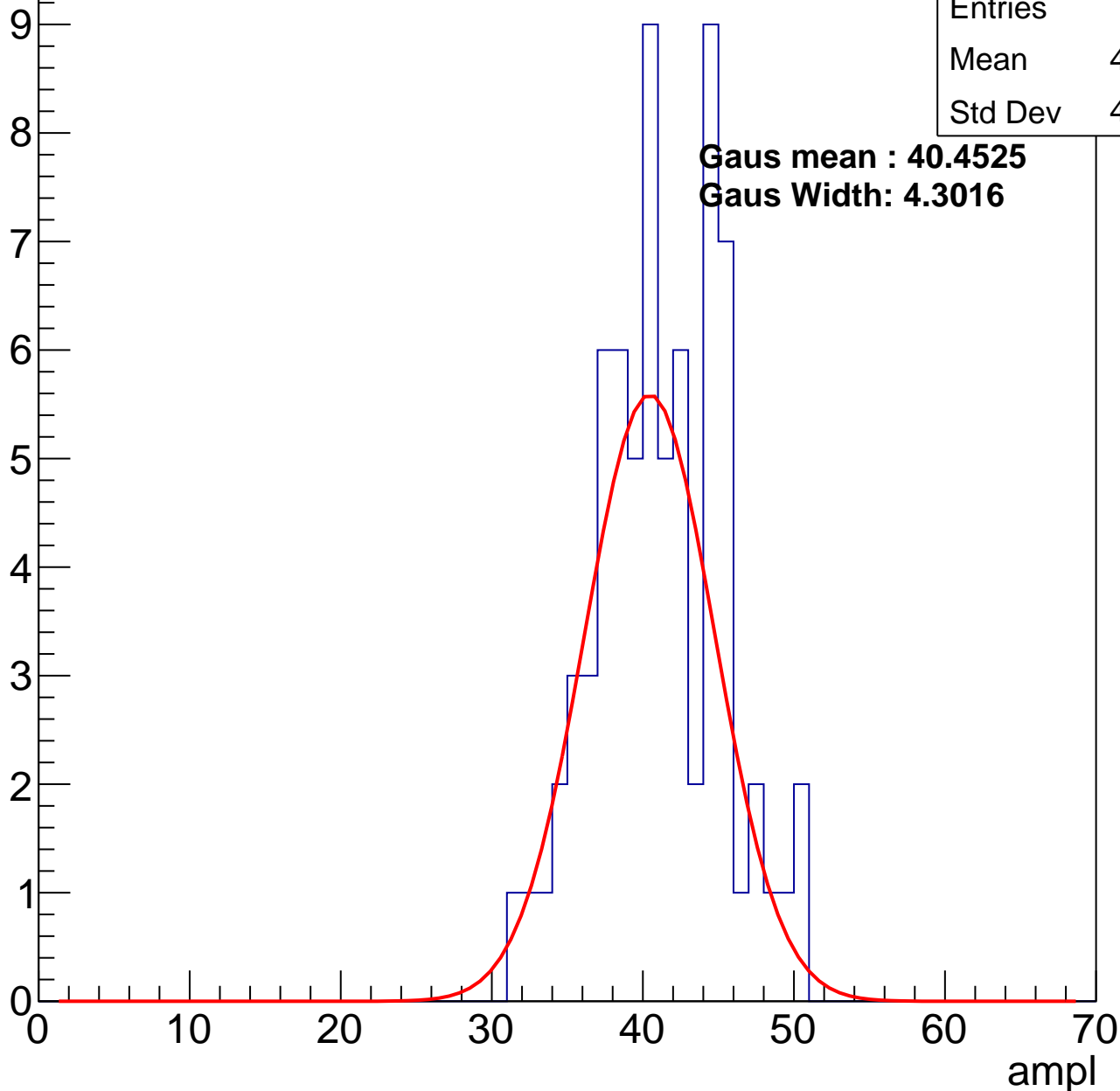
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	40.73
Std Dev	4.185

**Gaus mean : 40.4525**

**Gaus Width: 4.3016**

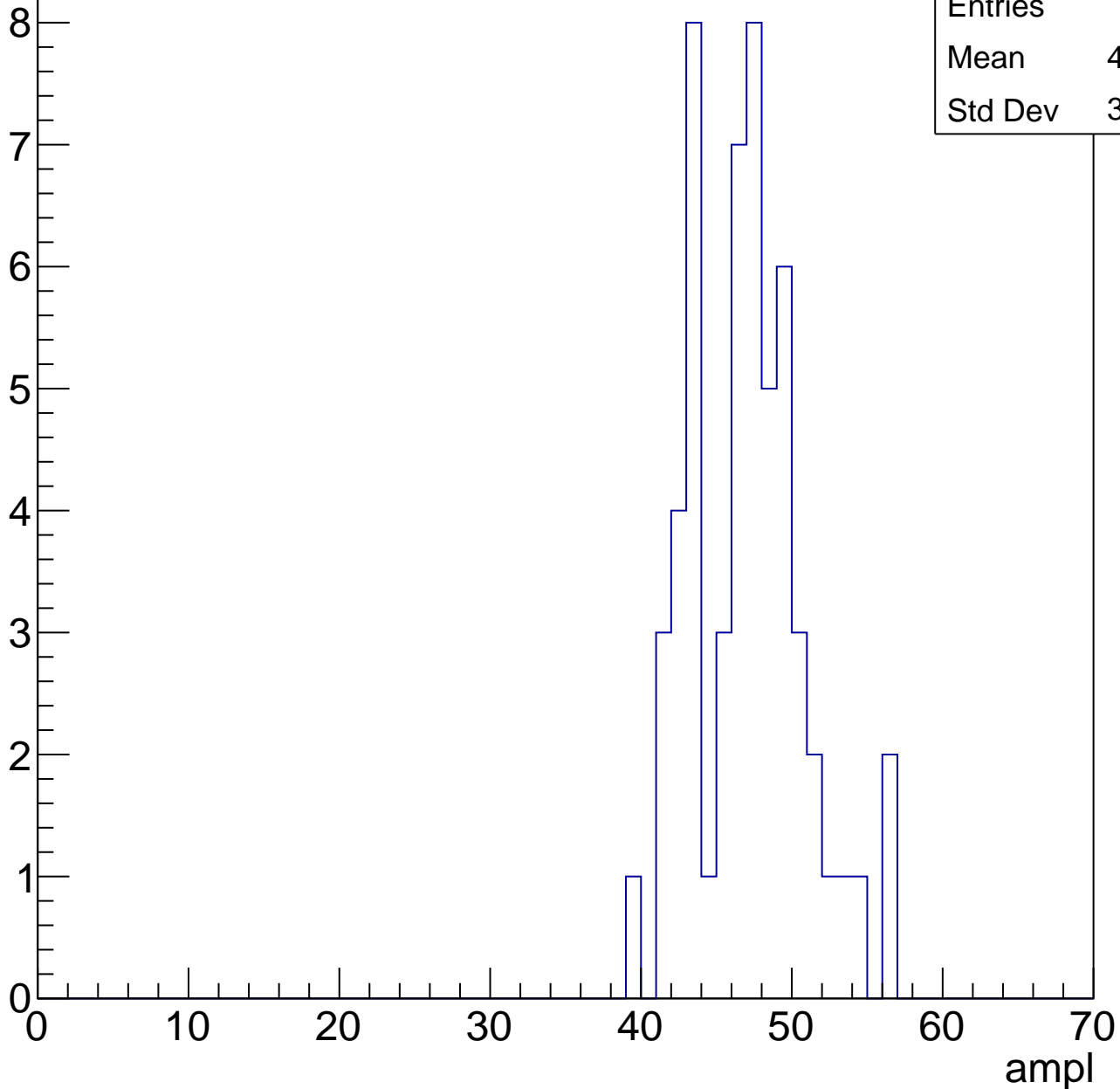


# B1L103S, U1-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	46.57
Std Dev	3.727

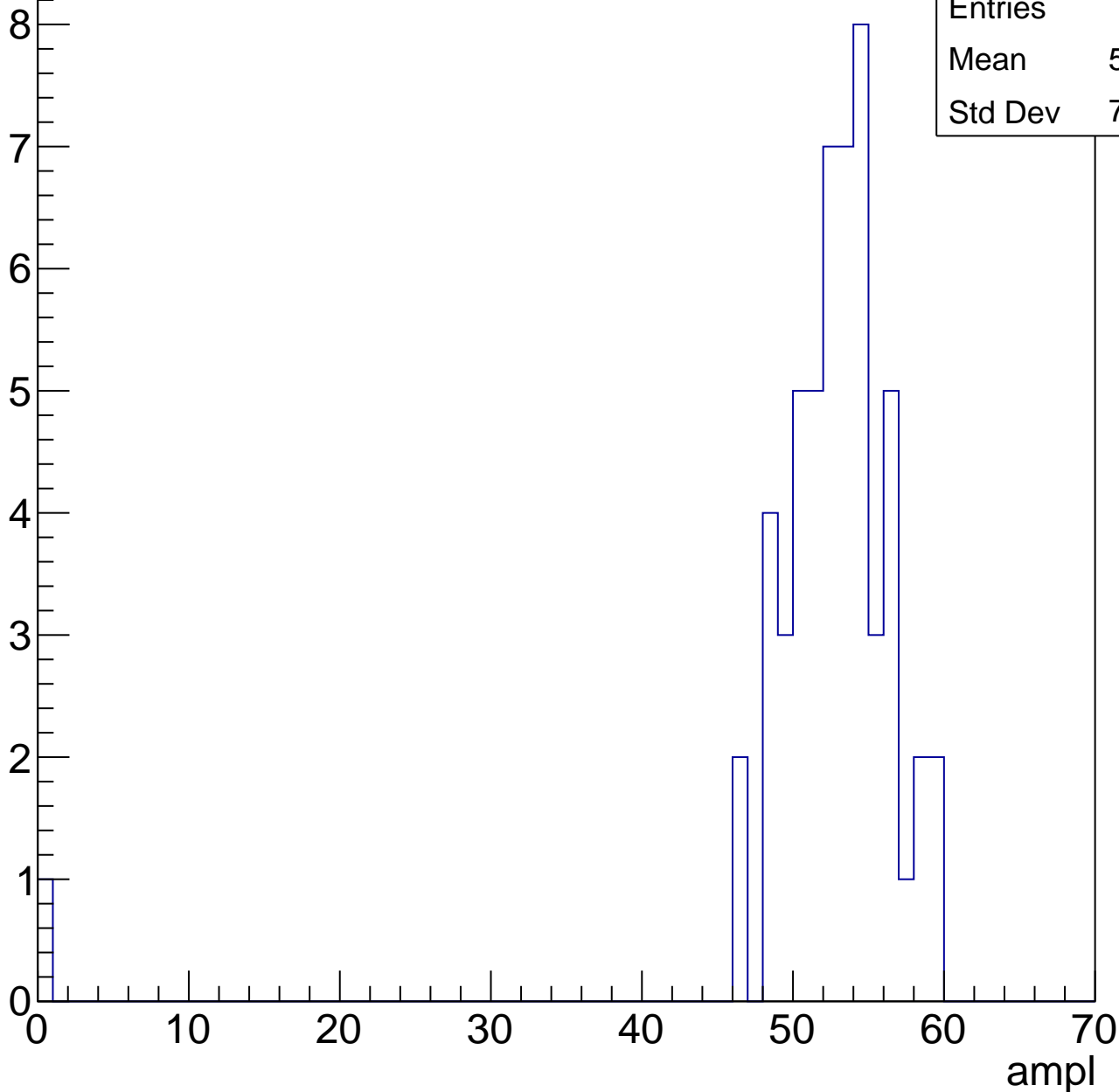


# B1L103S, U1-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

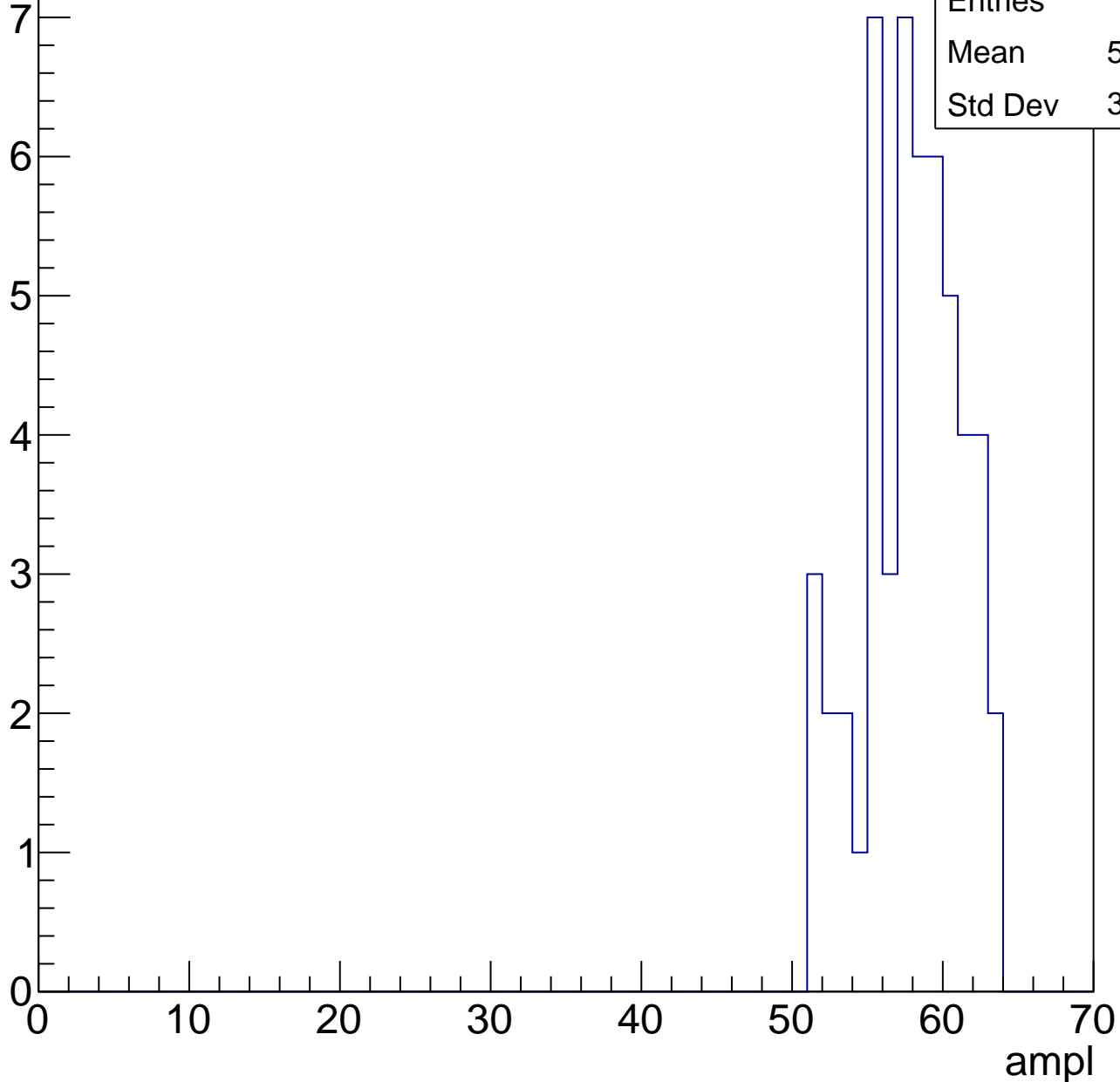
Entries	55
Mean	51.62
Std Dev	7.657



# B1L103S, U1-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



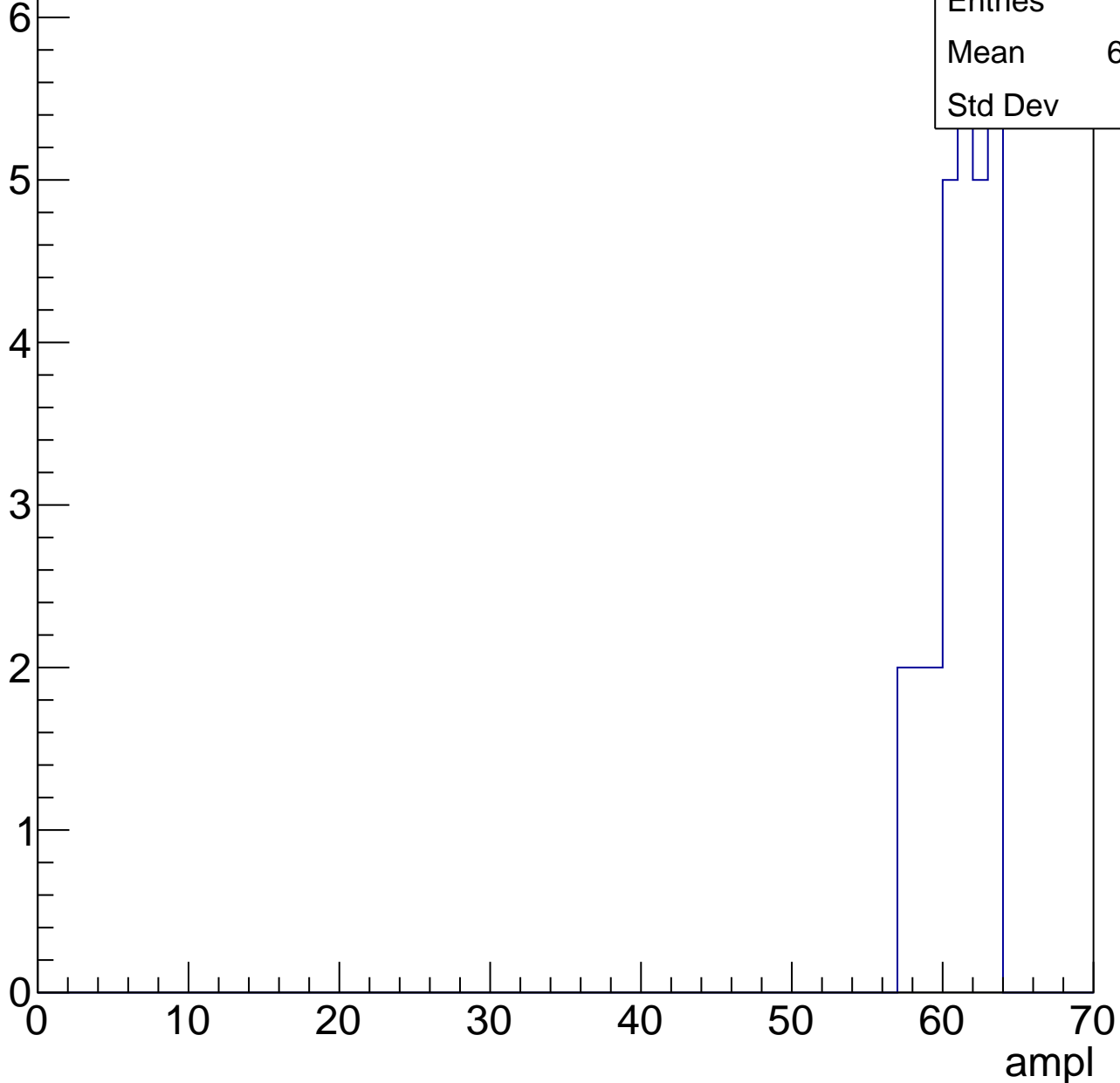
Entries	52
Mean	57.48
Std Dev	3.189

# B1L103S, U1-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	28
Mean	60.79
Std Dev	1.8





# B1L103S, U1-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch121, adc0

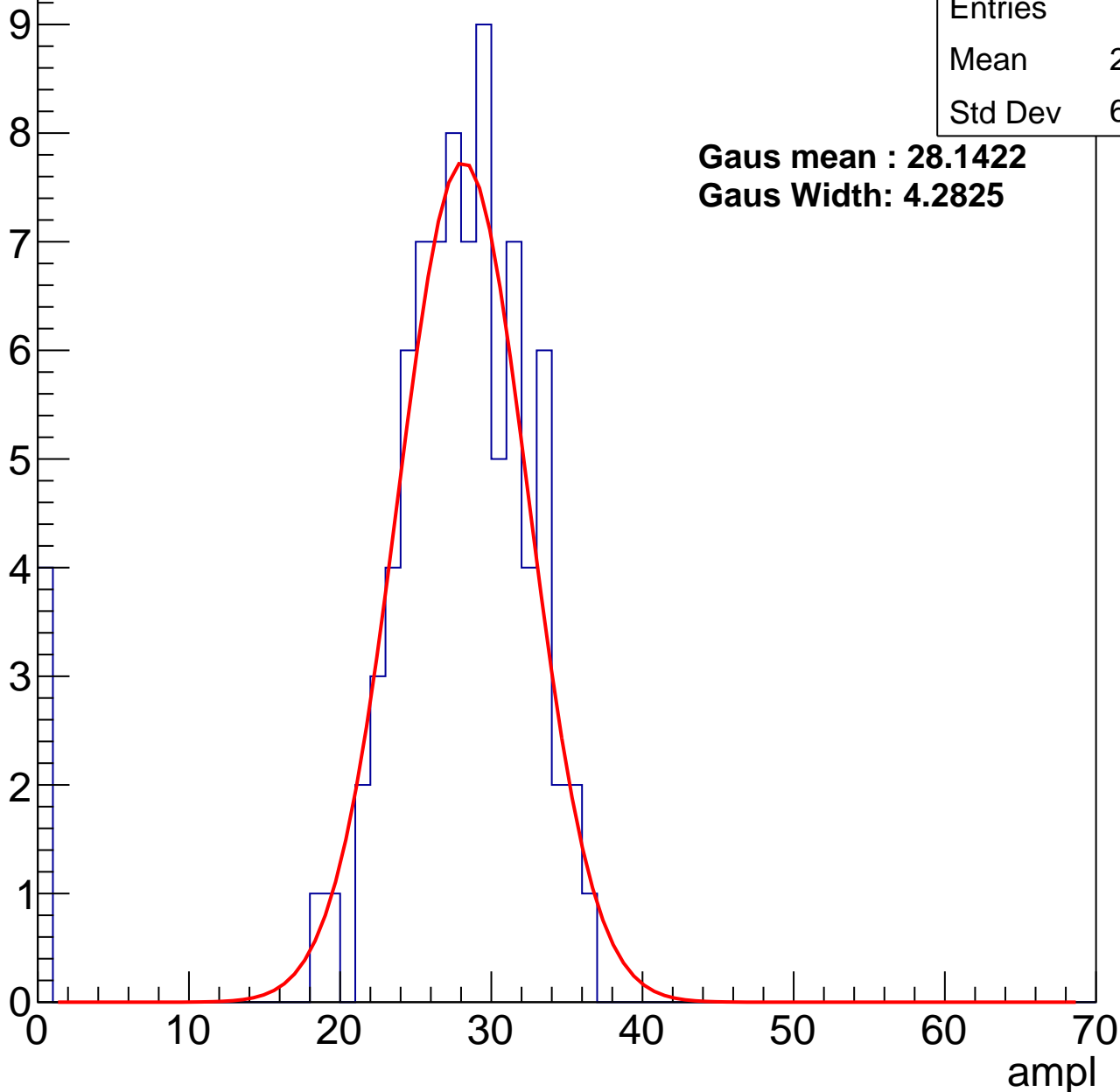
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	86
Mean	26.49
Std Dev	6.956

**Gaus mean : 28.1422**

**Gaus Width: 4.2825**



# B1L103S, U1-ch121, adc1

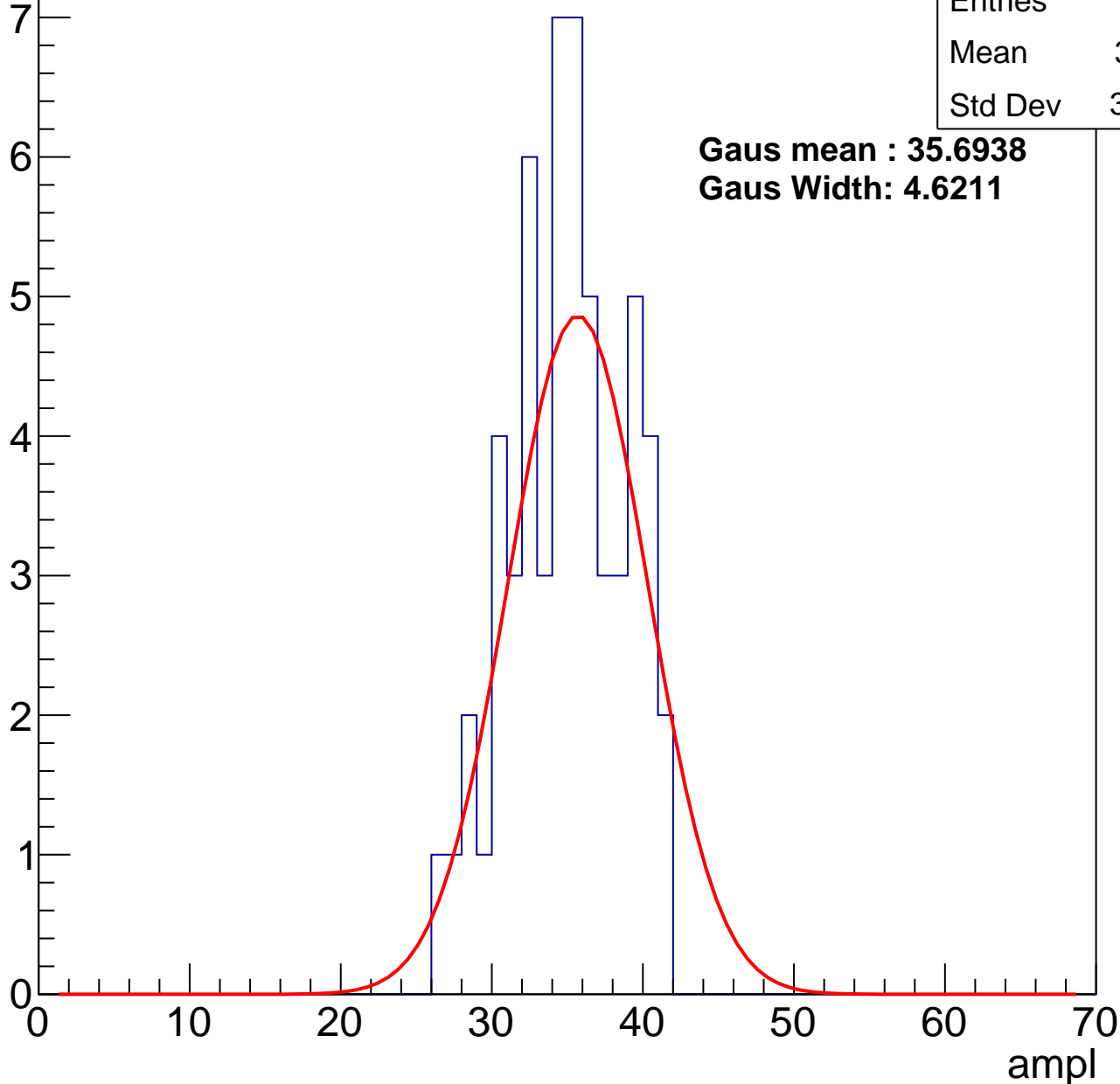
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	34.51
Std Dev	3.705

**Gaus mean : 35.6938**

**Gaus Width: 4.6211**



# B1L103S, U1-ch121, adc2

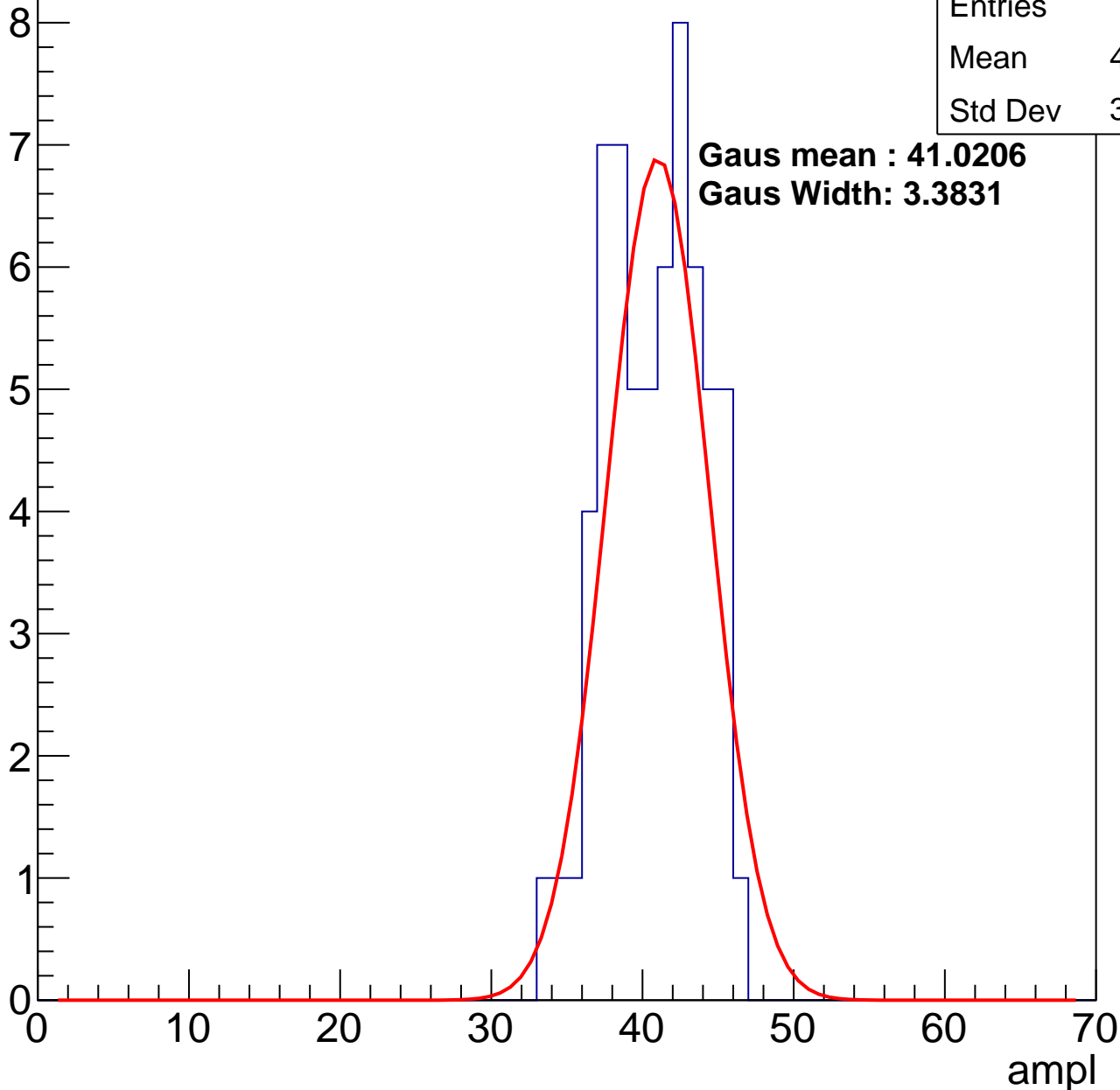
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	40.27
Std Dev	3.107

**Gaus mean : 41.0206**

**Gaus Width: 3.3831**



# B1L103S, U1-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

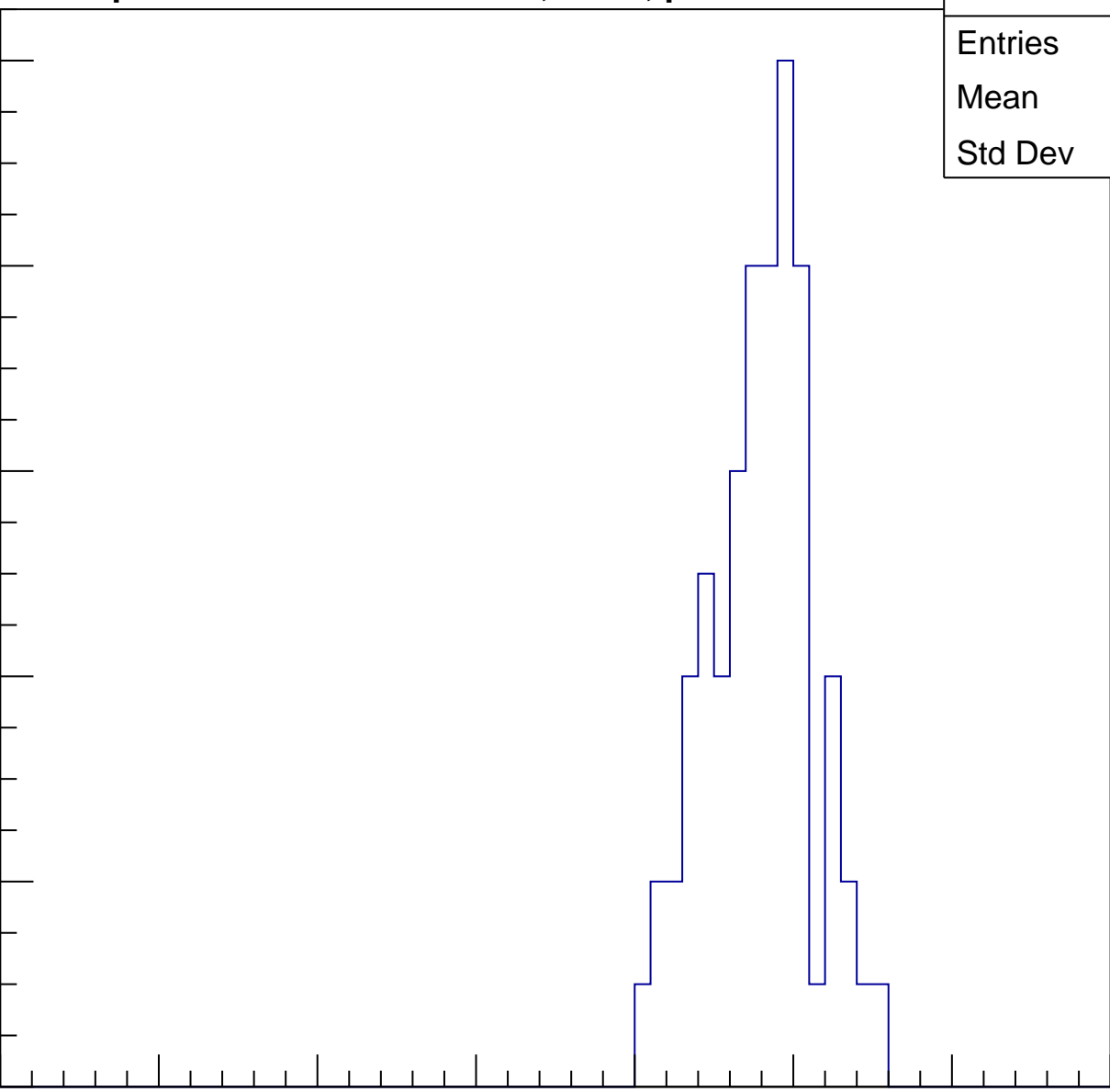
Entries	67
Mean	47.43
Std Dev	3.256

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

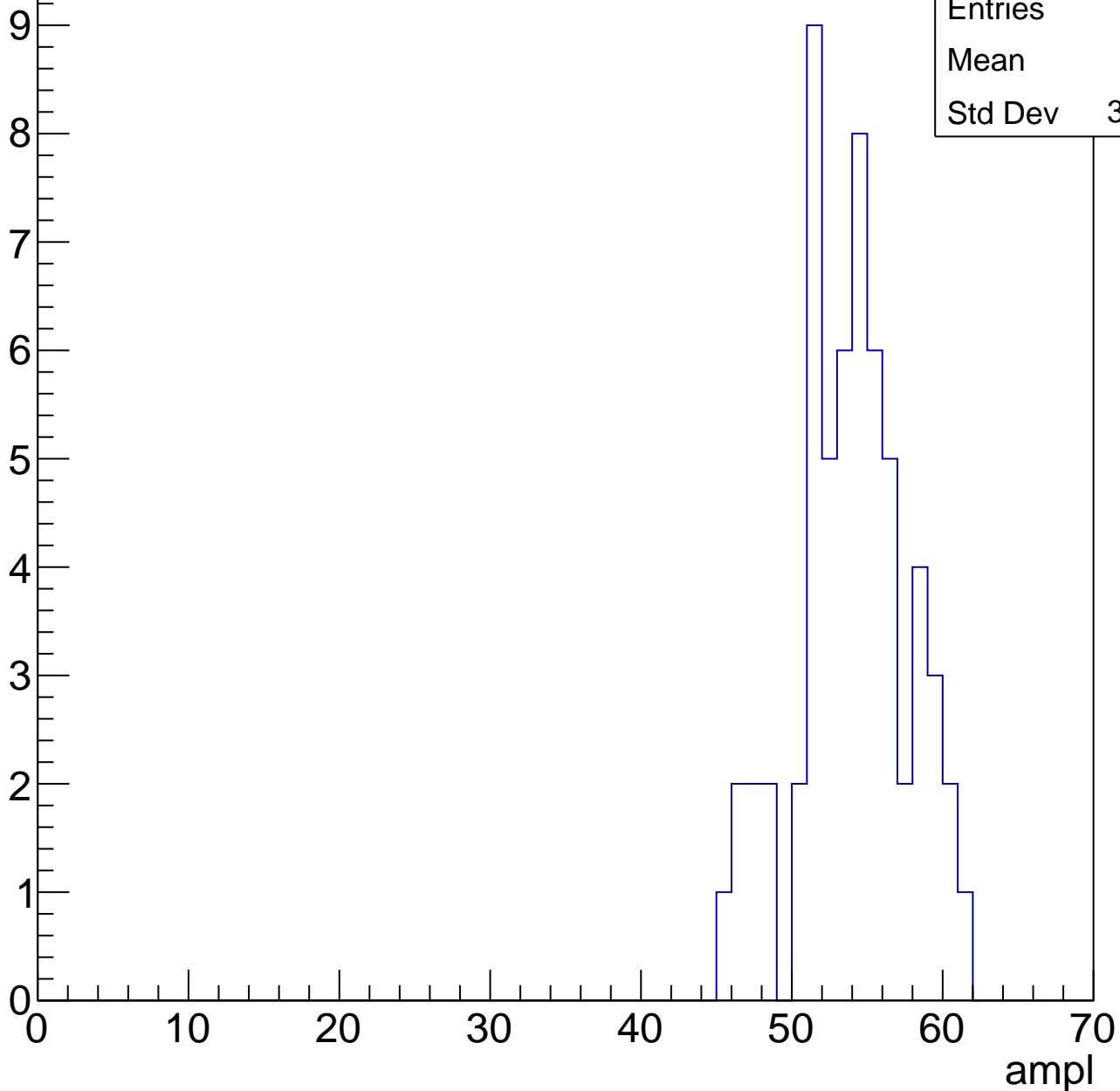


# B1L103S, U1-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	53.5
Std Dev	3.667

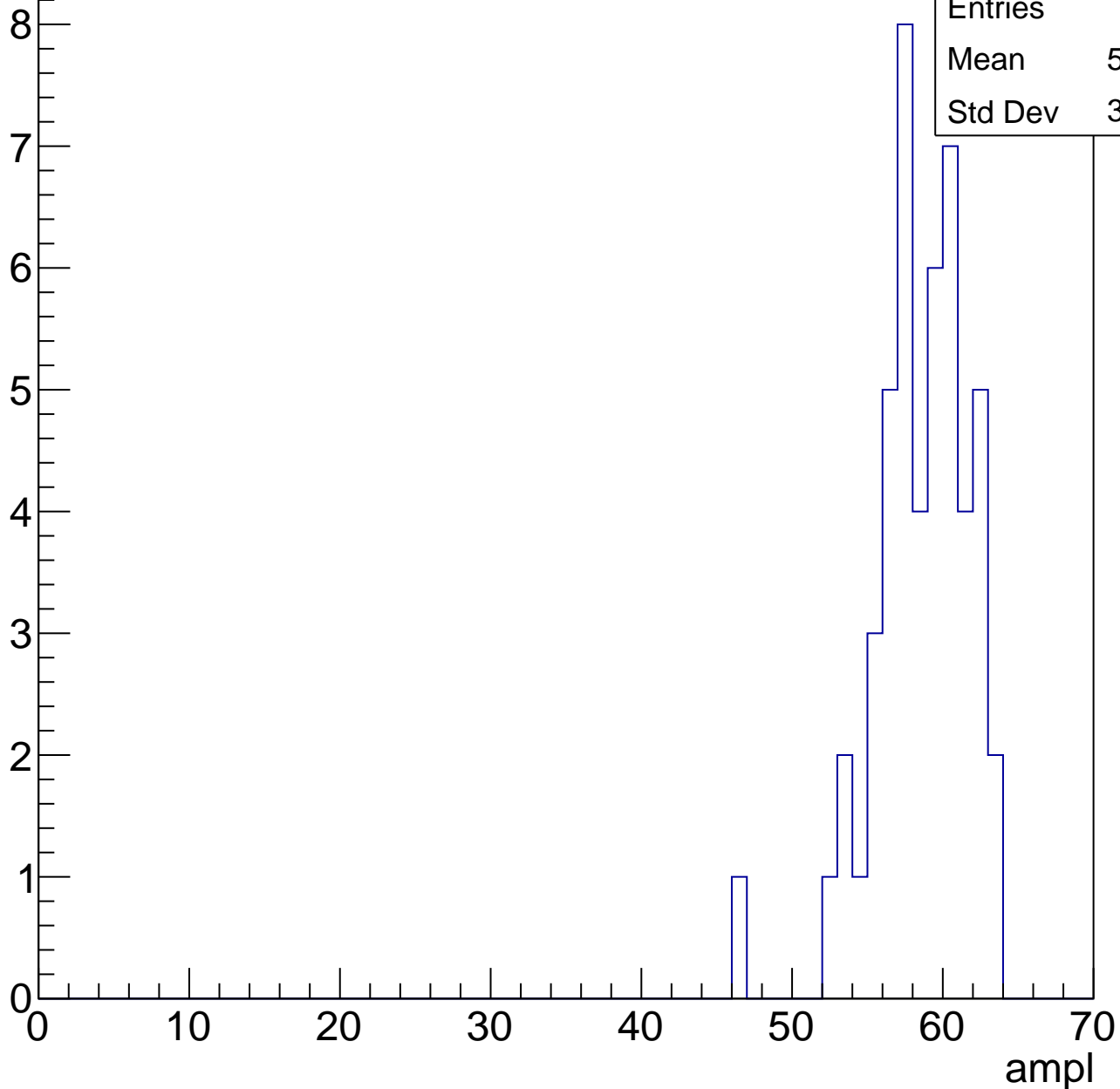


# B1L103S, U1-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	58.06
Std Dev	3.197

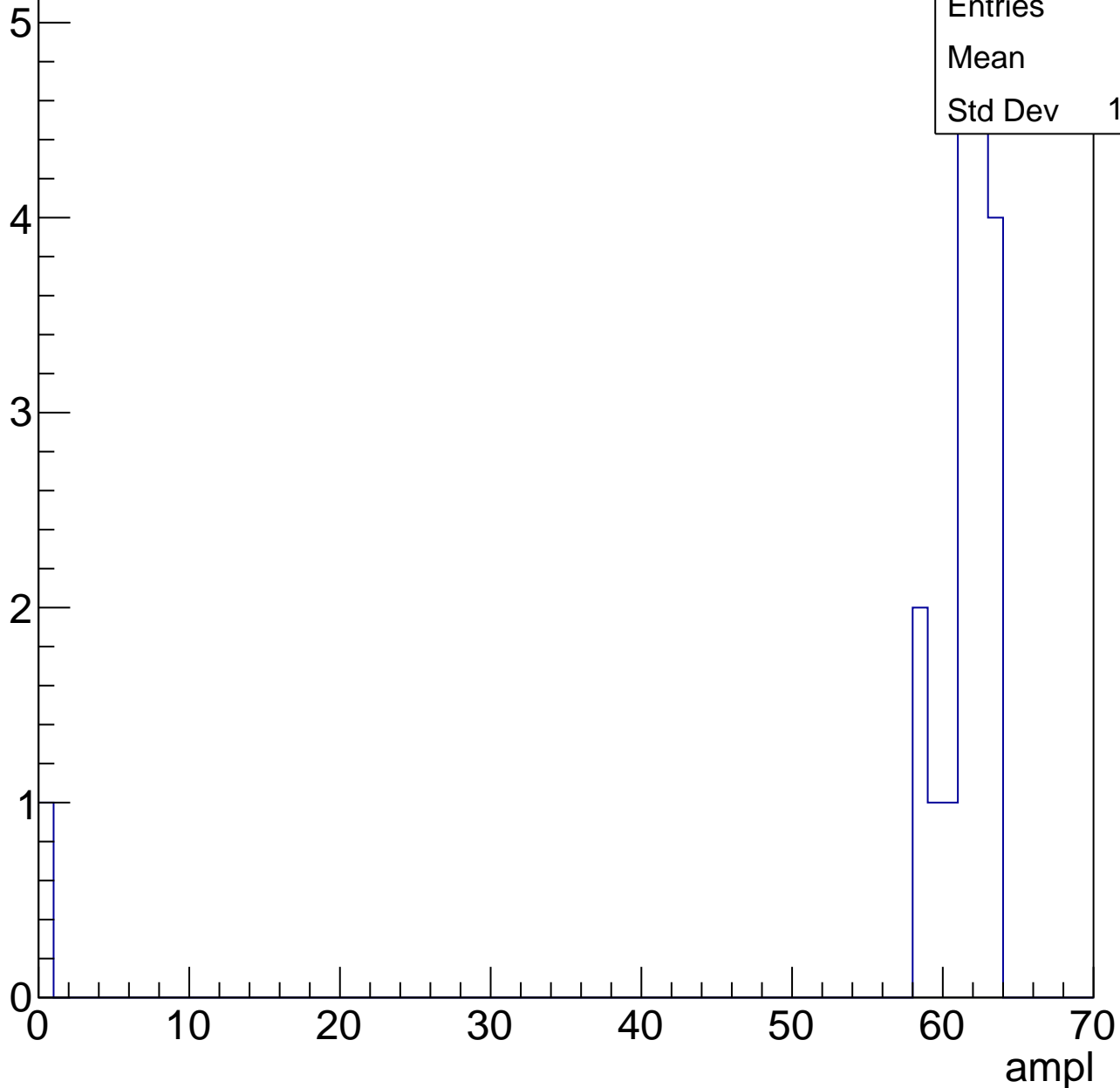


# B1L103S, U1-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	19
Mean	58
Std Dev	13.75

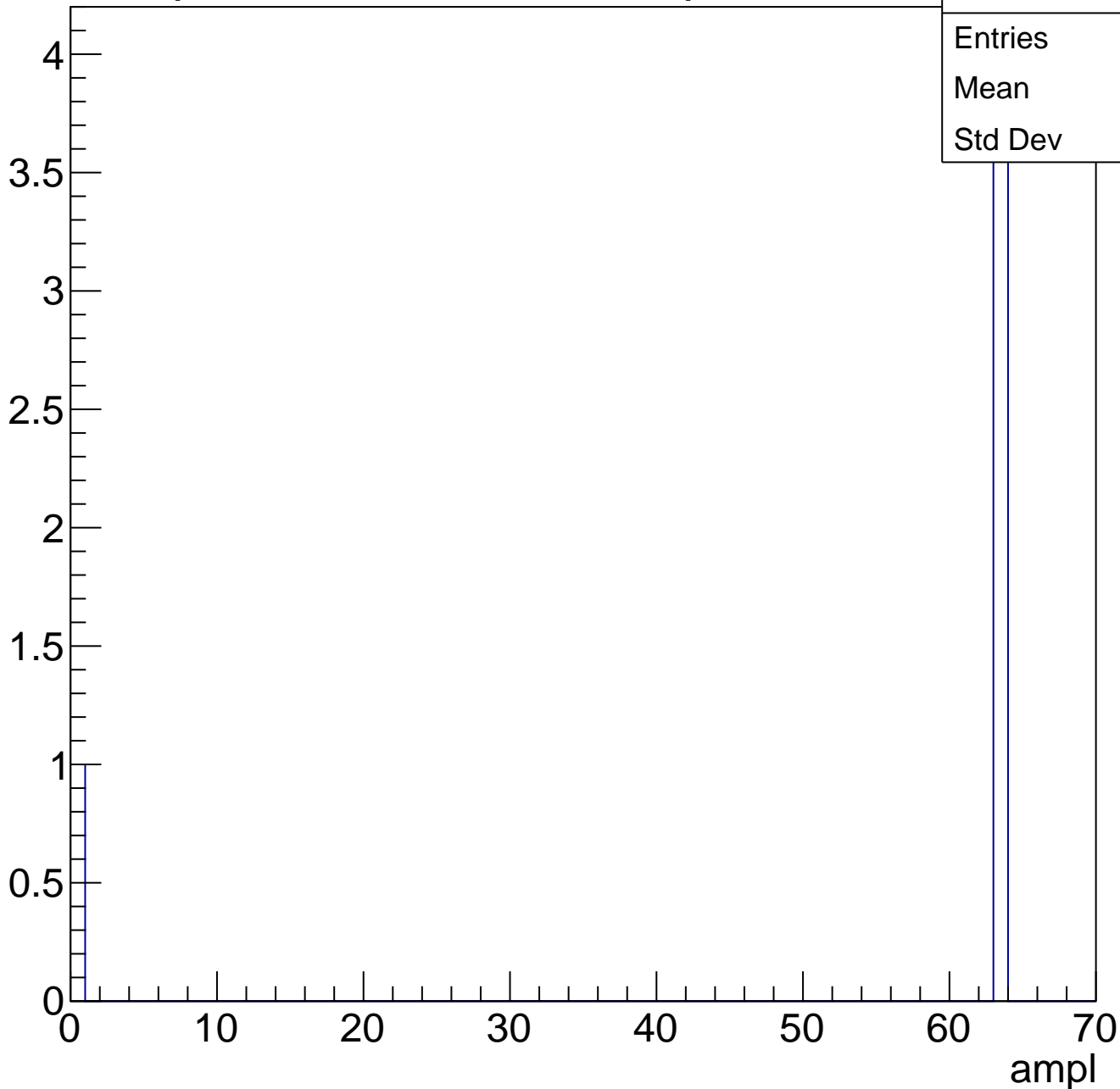




# B1L103S, U1-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch122, adc0

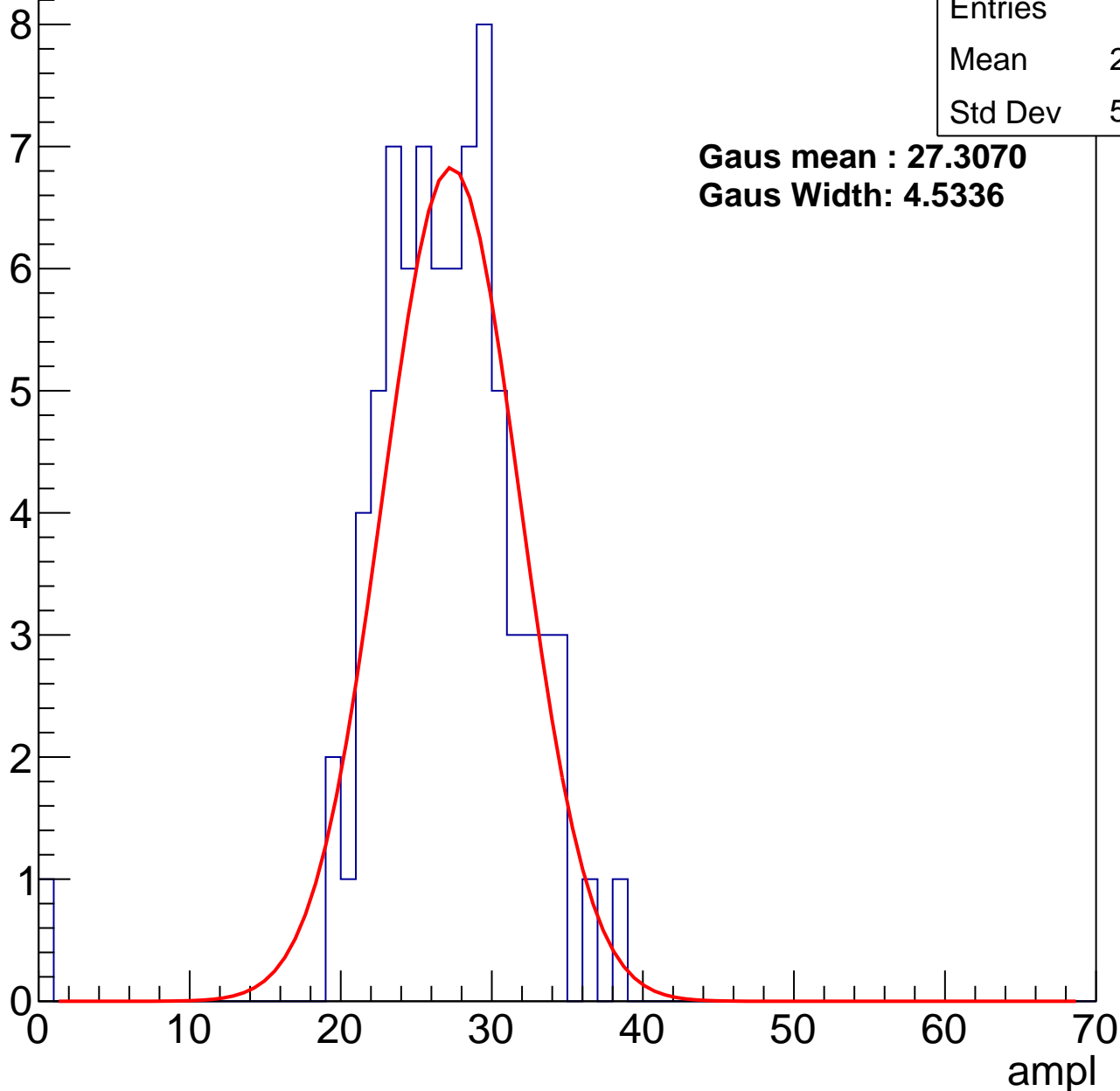
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	26.48
Std Dev	5.054

**Gaus mean : 27.3070**

**Gaus Width: 4.5336**



# B1L103S, U1-ch122, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	72
Mean	34.17
Std Dev	3.756

**Gaus mean : 34.2604**

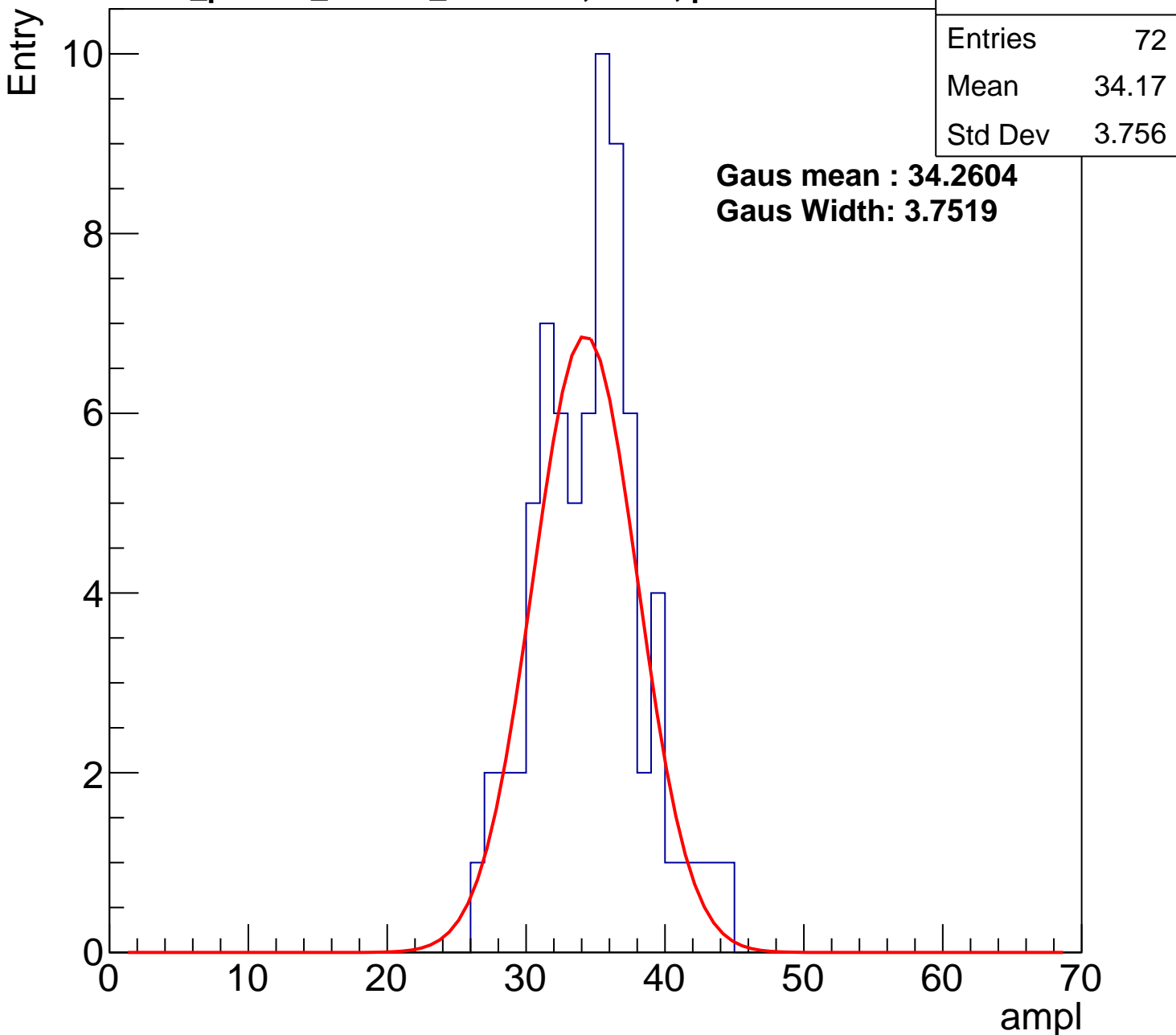
**Gaus Width: 3.7519**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U1-ch122, adc2

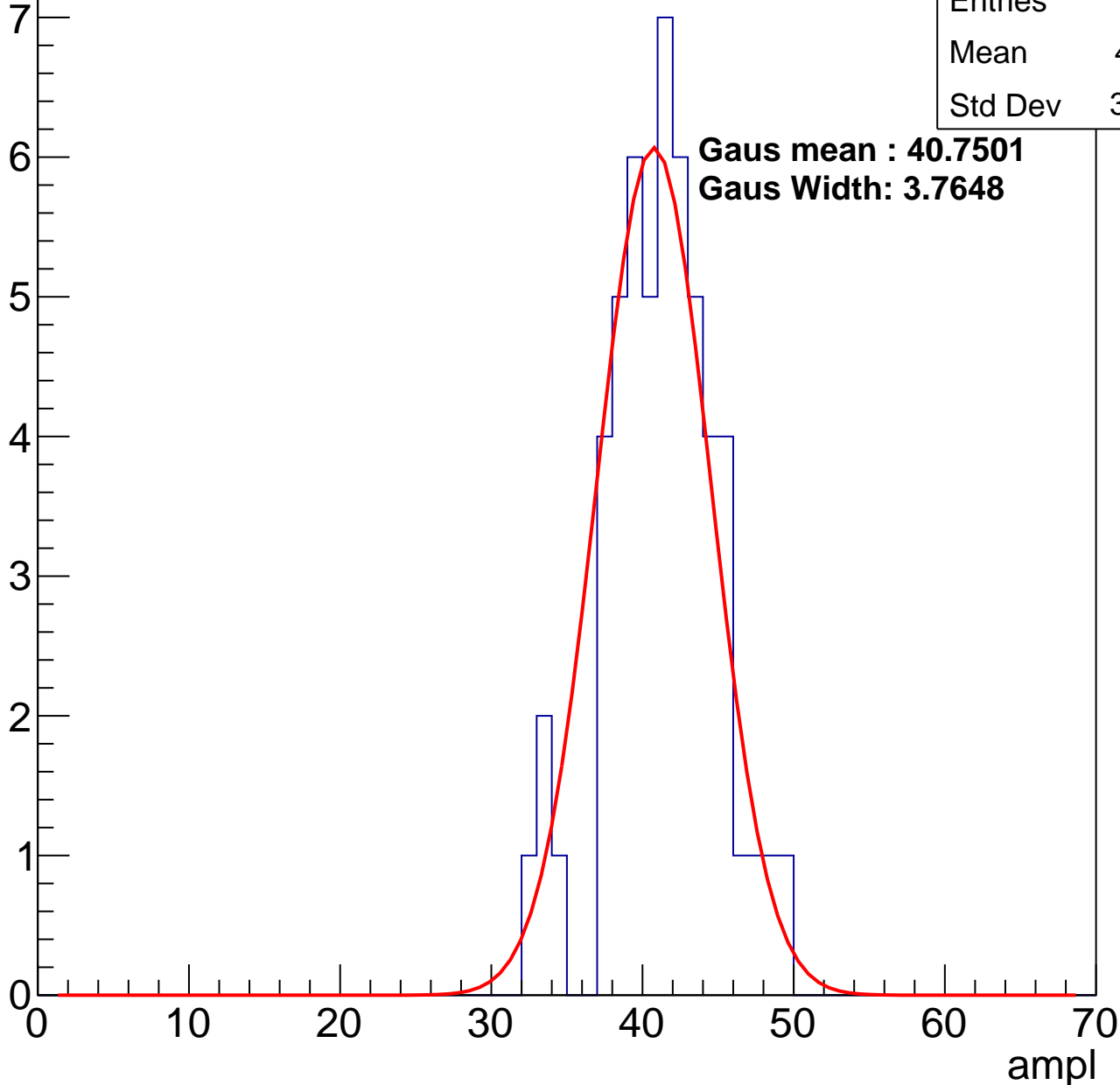
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	40.81
Std Dev	3.585

**Gaus mean : 40.7501**

**Gaus Width: 3.7648**

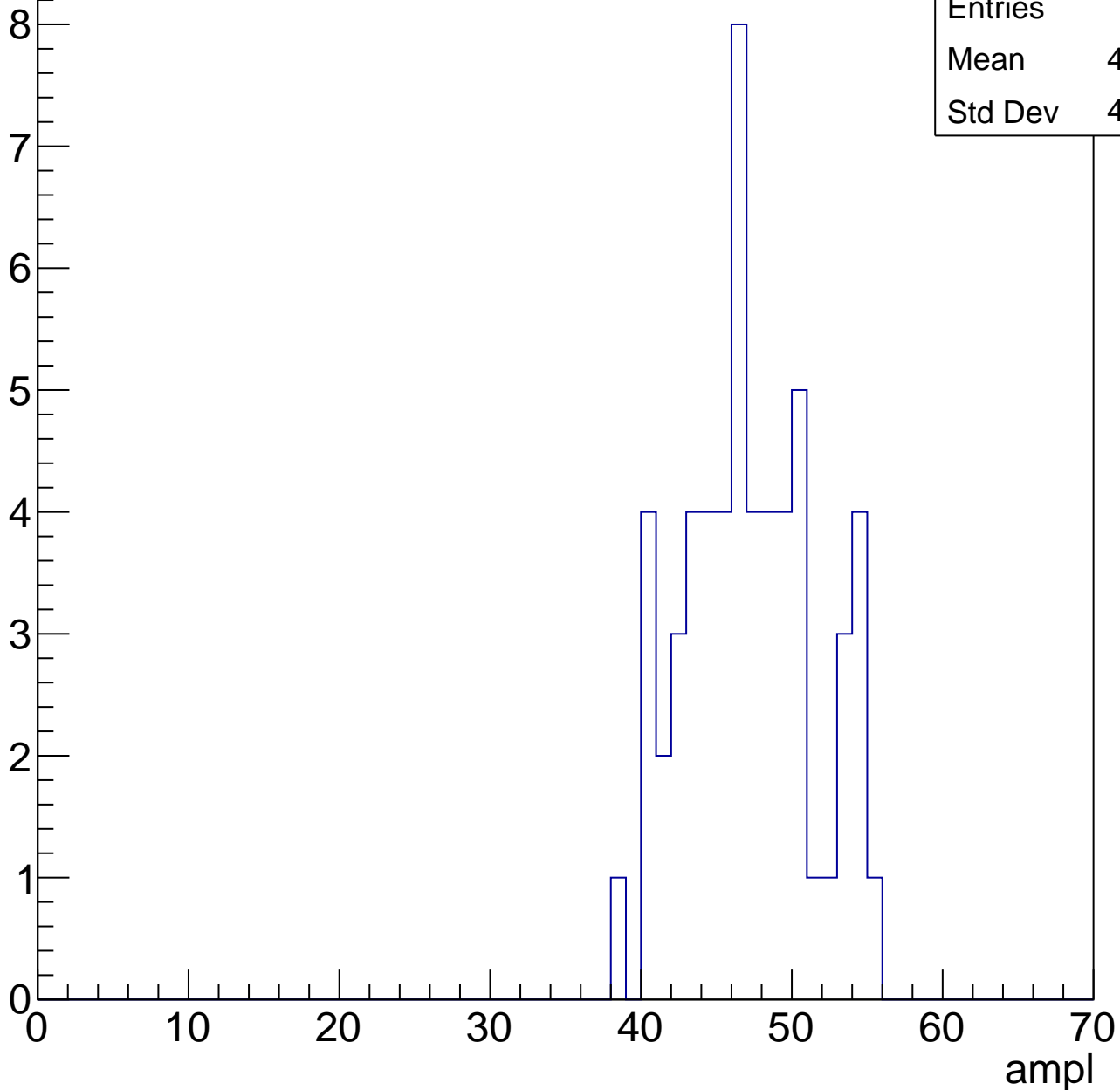


# B1L103S, U1-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	46.68
Std Dev	4.223

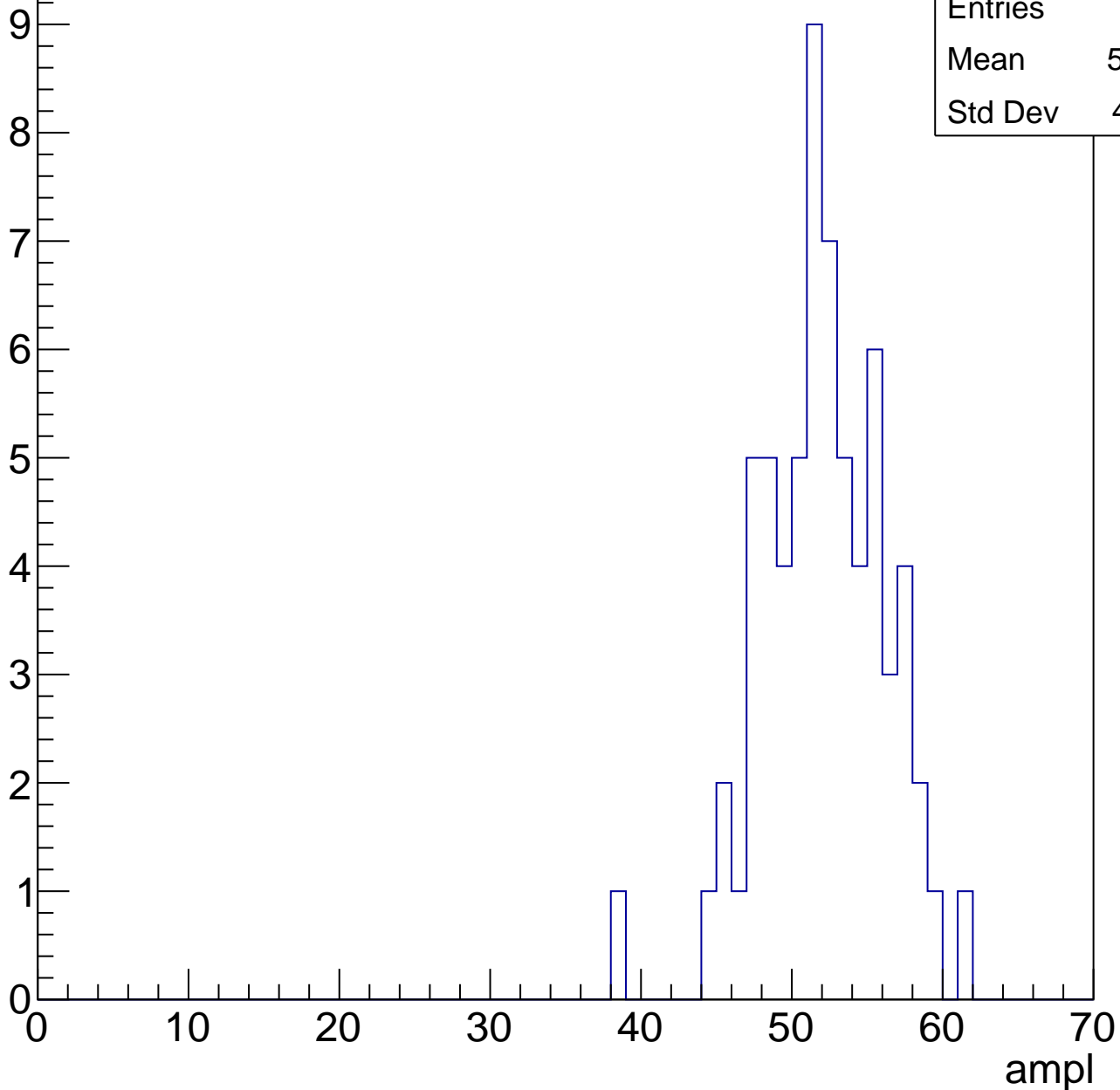


# B1L103S, U1-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	51.59
Std Dev	4.041

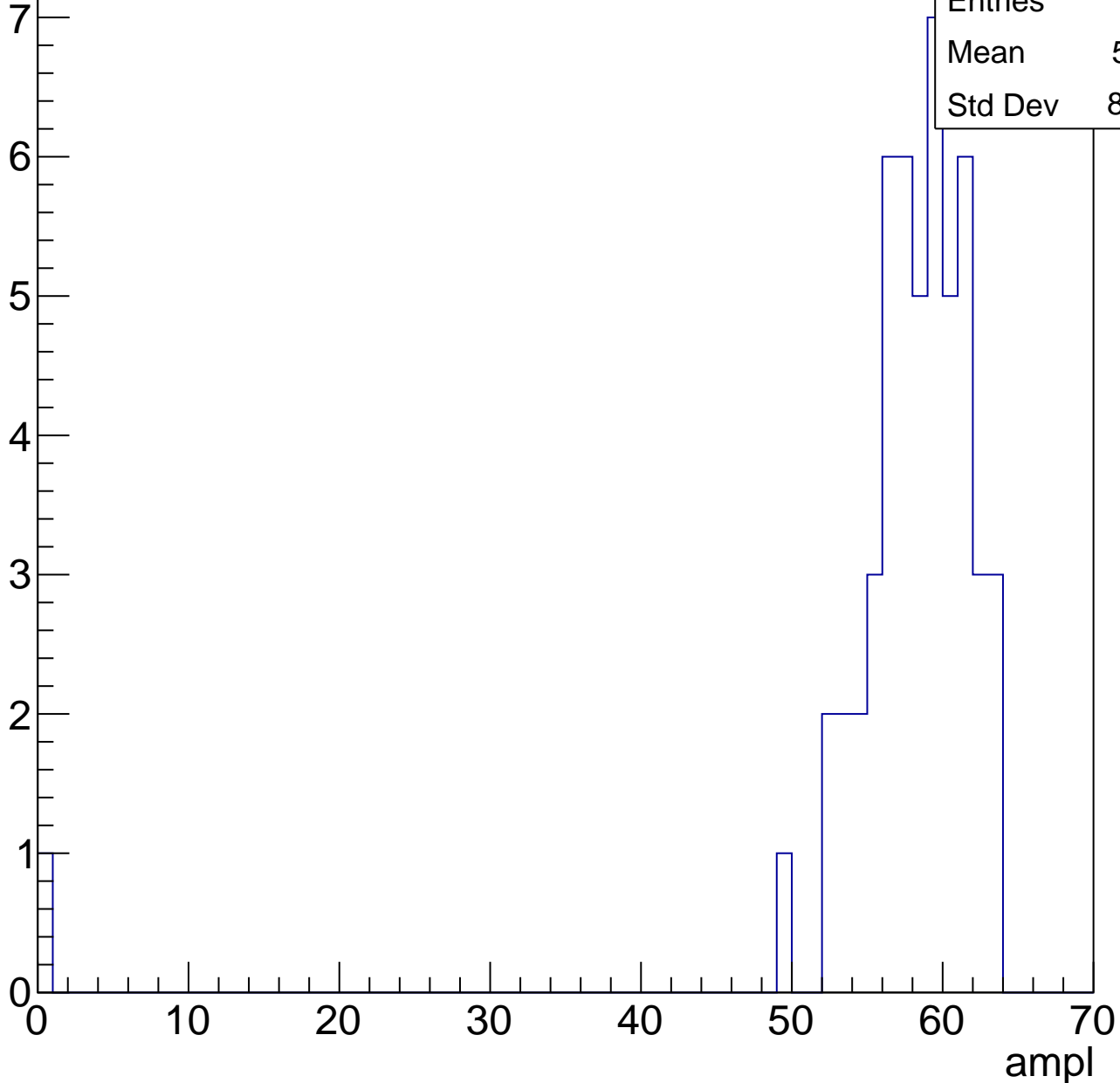


# B1L103S, U1-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	56.81
Std Dev	8.533

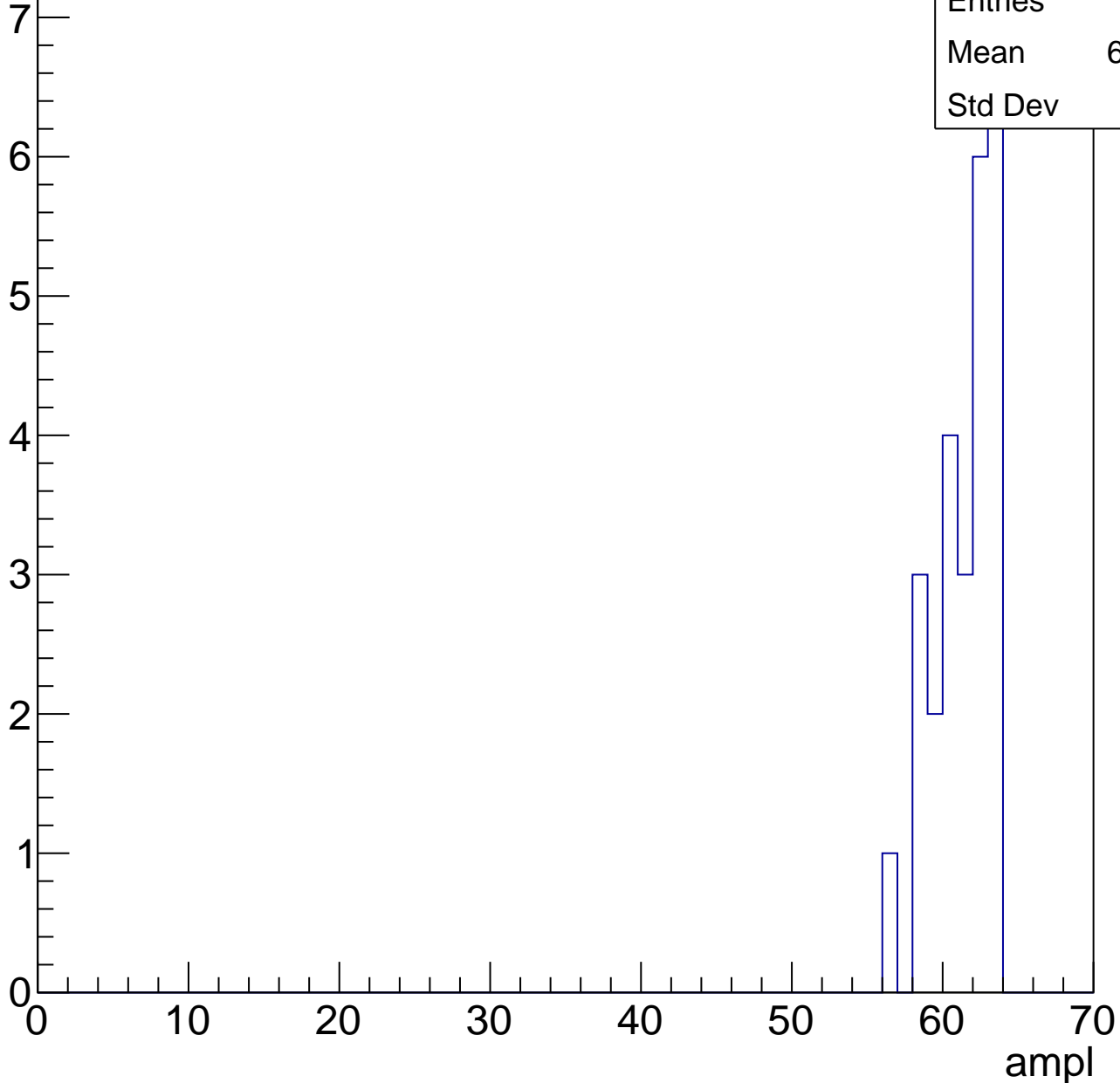


# B1L103S, U1-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	26
Mean	60.92
Std Dev	1.94

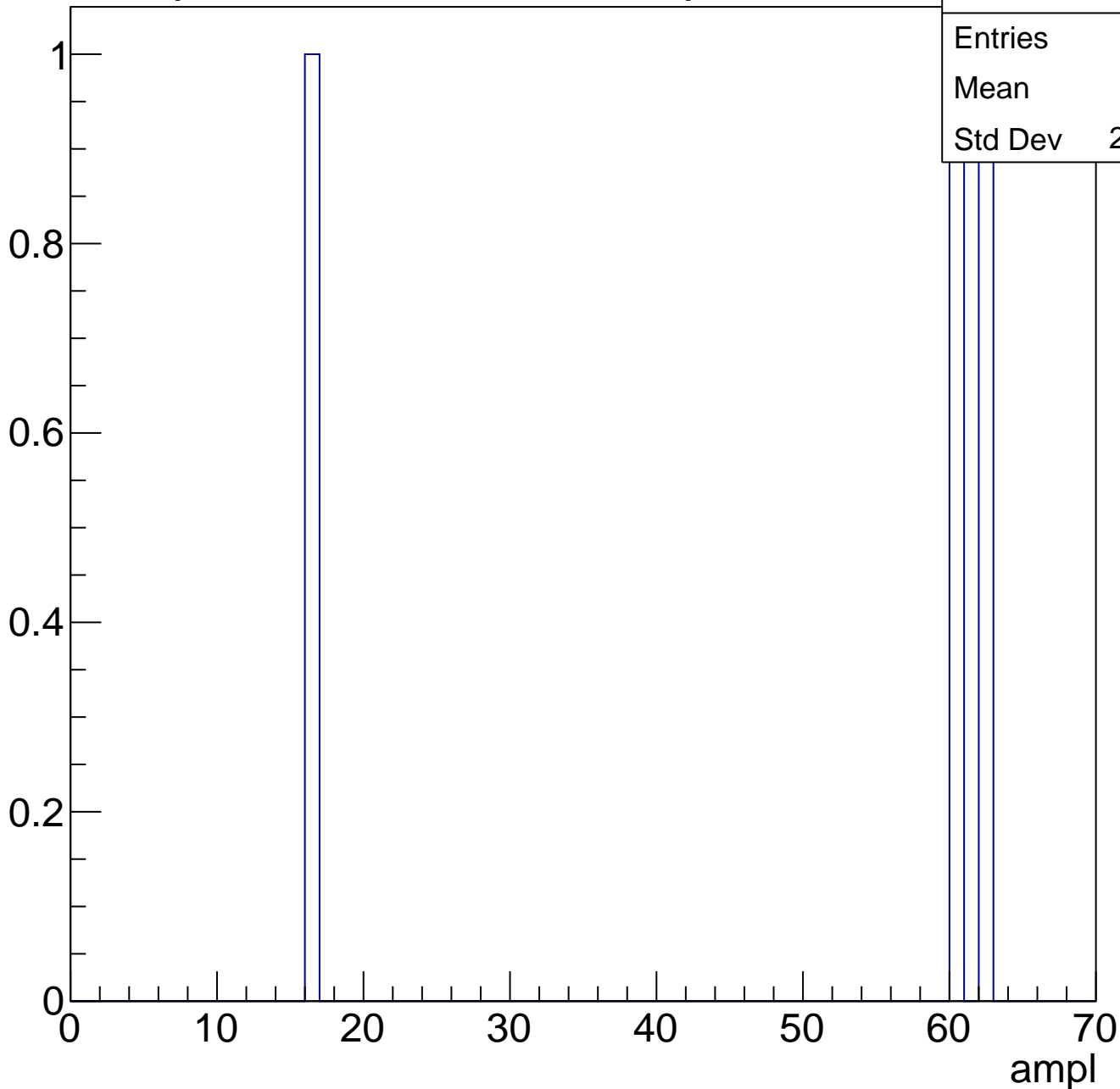




# B1L103S, U1-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch123, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	81
Mean	26.36
Std Dev	6.308

**Gaus mean : 27.6854**

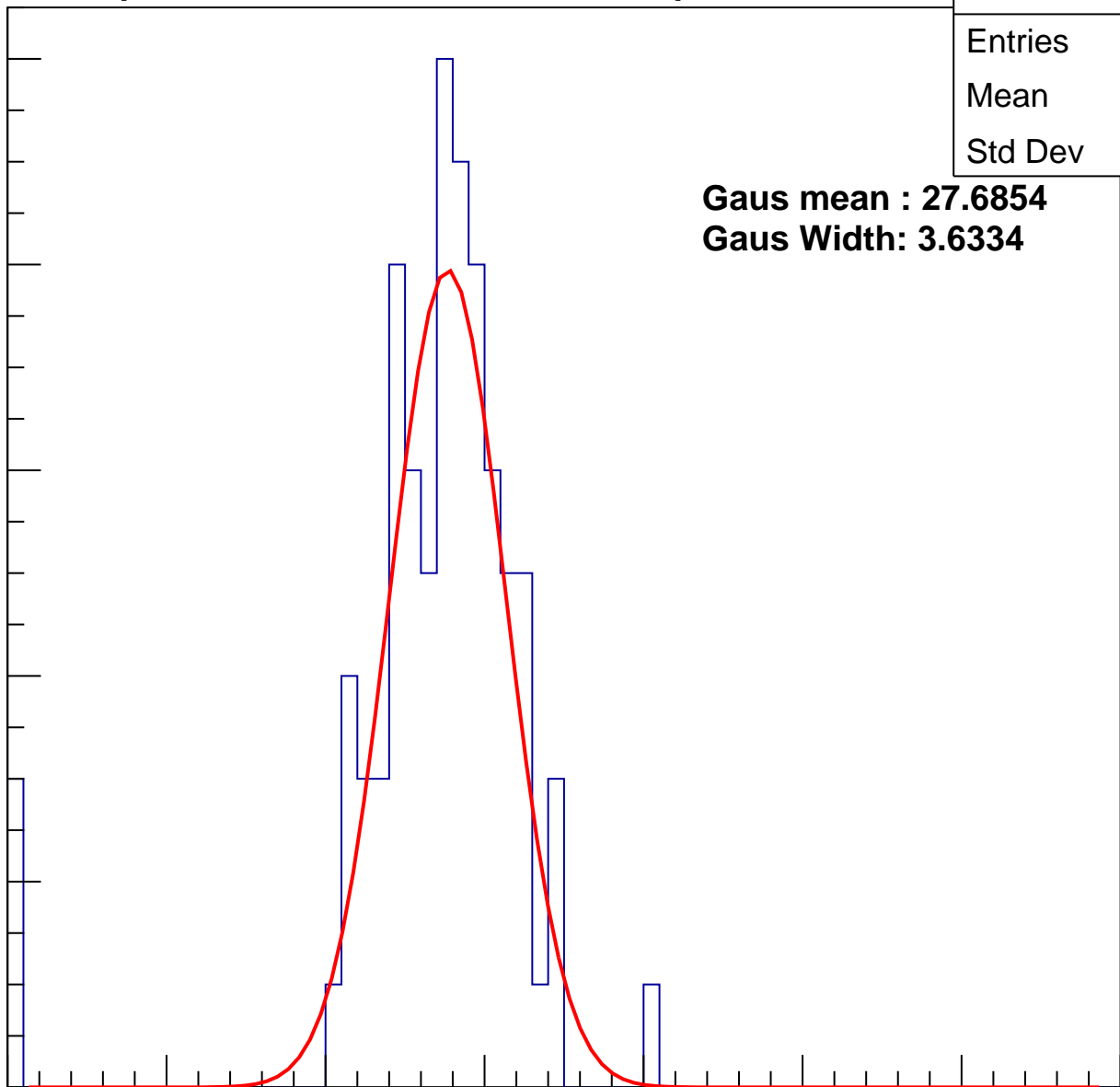
**Gaus Width: 3.6334**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U1-ch123, adc1

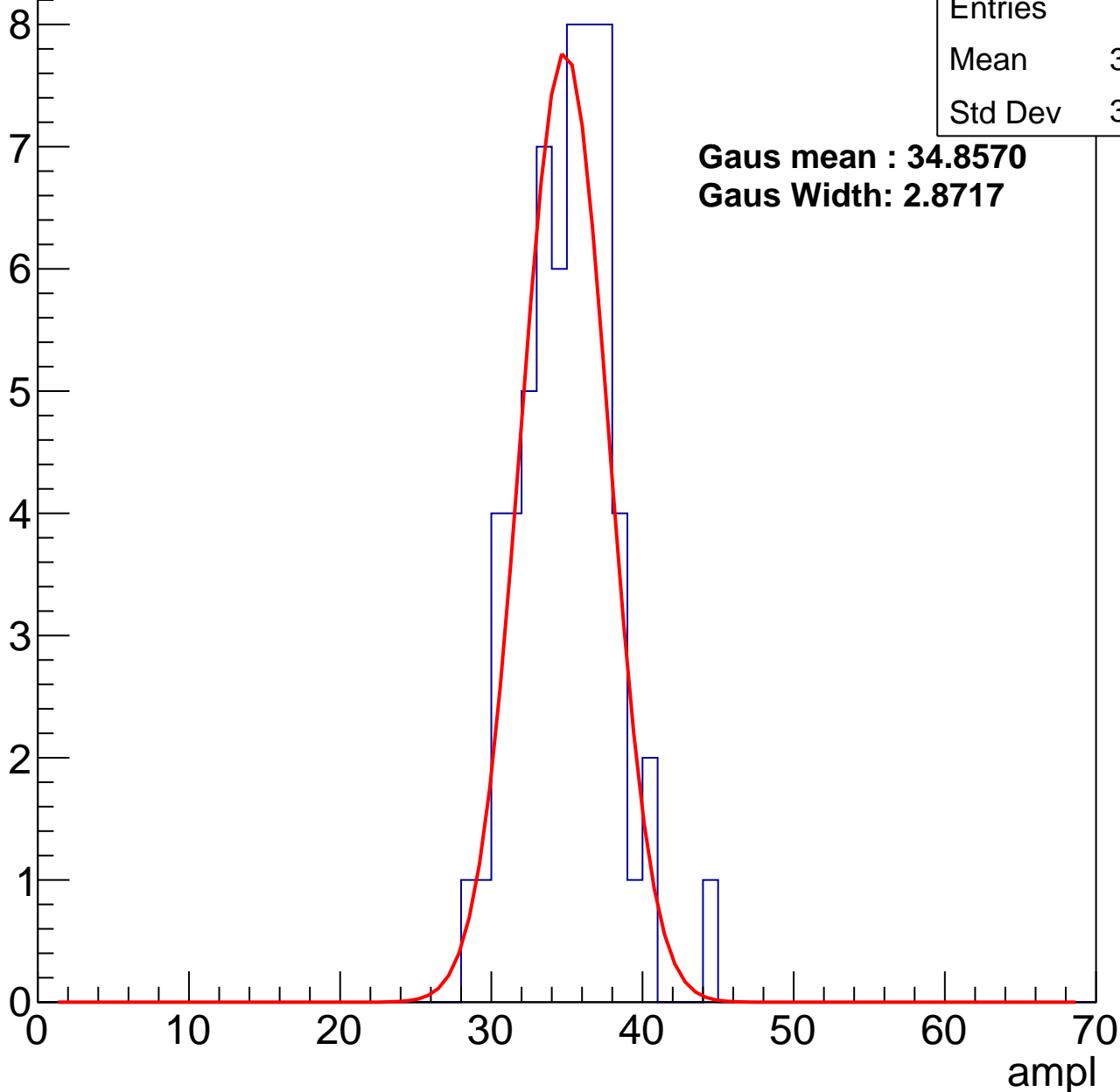
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	34.58
Std Dev	3.002

**Gaus mean : 34.8570**

**Gaus Width: 2.8717**



# B1L103S, U1-ch123, adc2

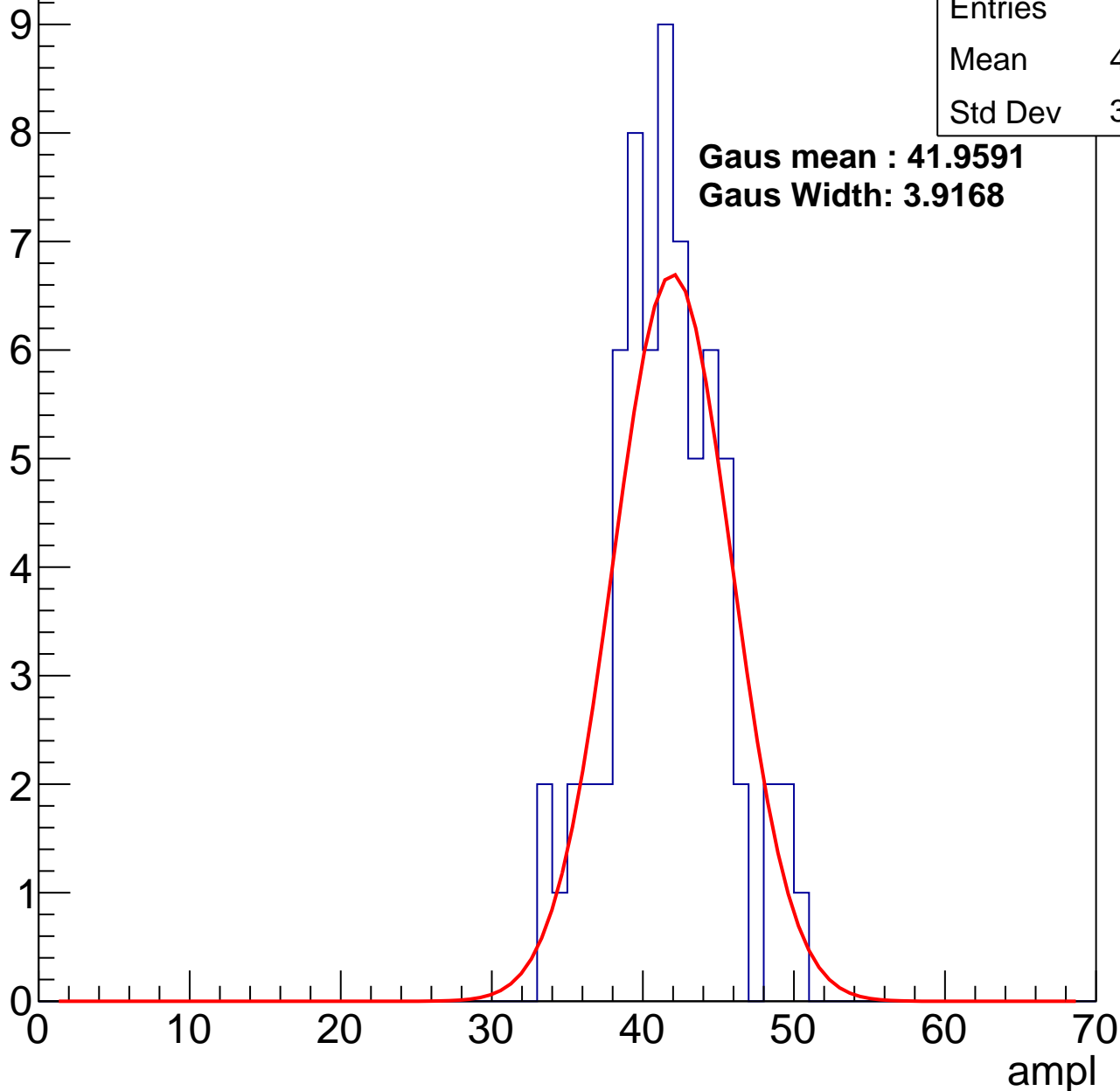
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	41.16
Std Dev	3.716

**Gaus mean : 41.9591**

**Gaus Width: 3.9168**

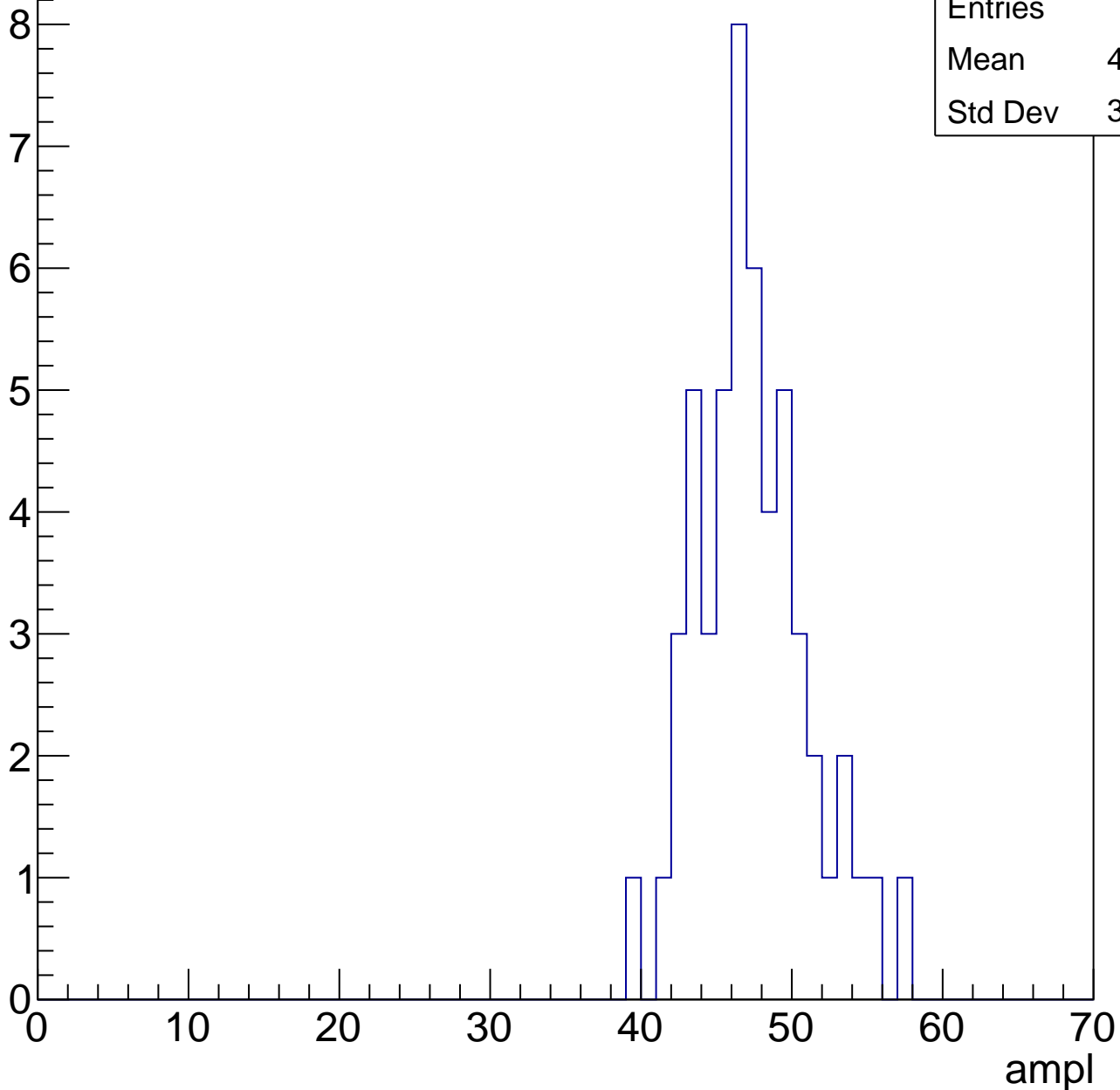


# B1L103S, U1-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	46.94
Std Dev	3.676

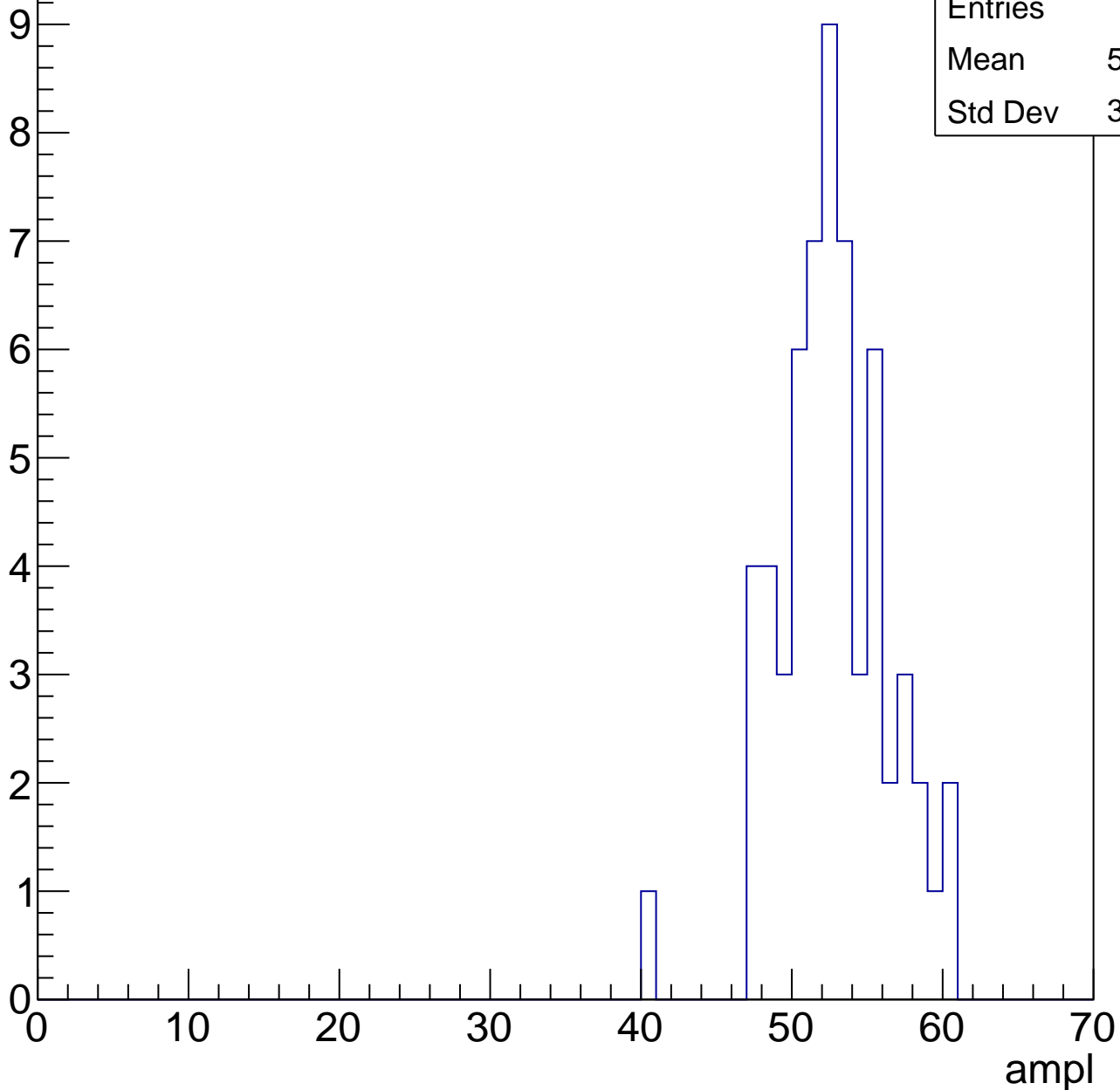


# B1L103S, U1-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	52.22
Std Dev	3.634

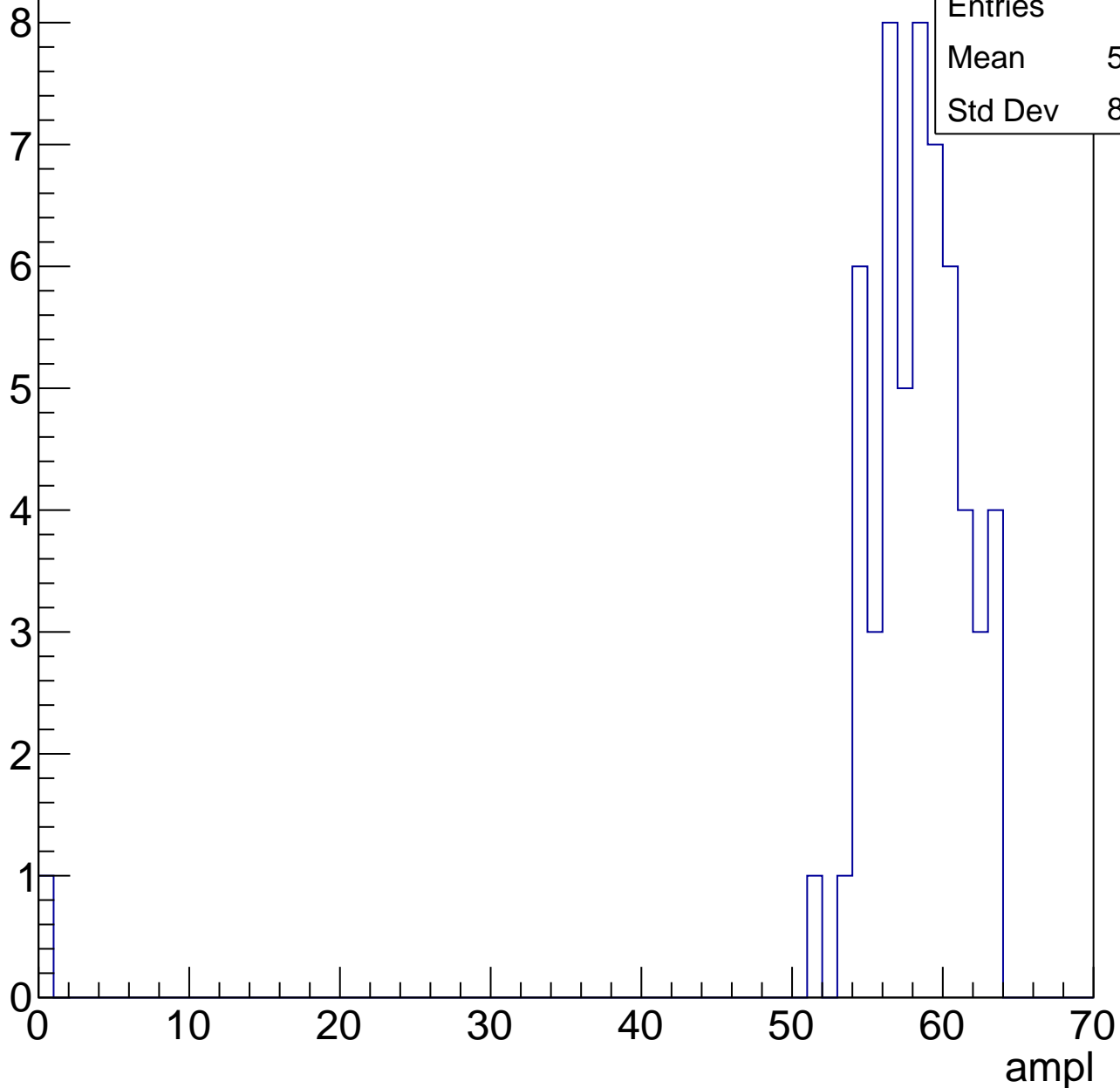


# B1L103S, U1-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	56.93
Std Dev	8.109

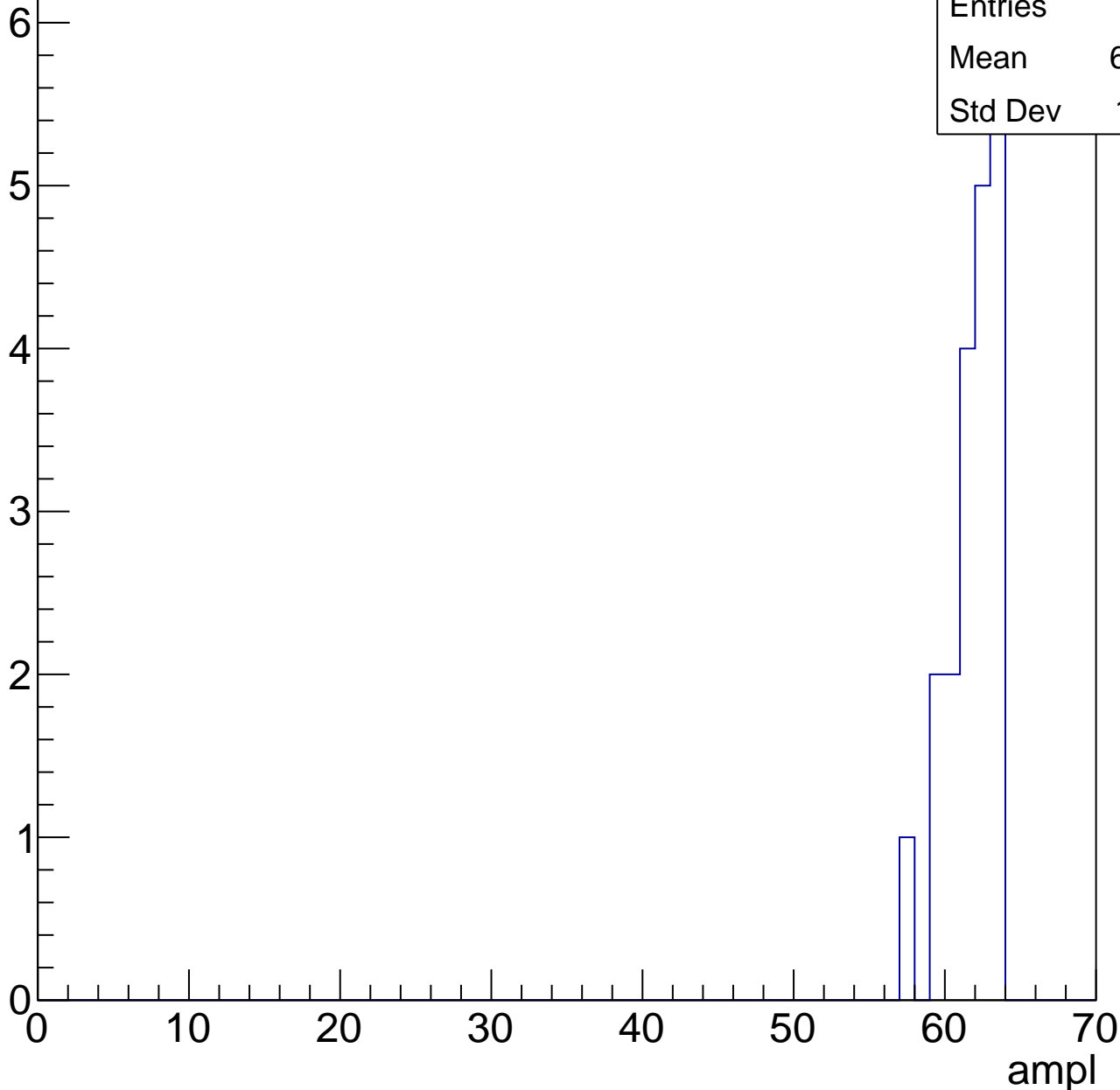


# B1L103S, U1-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	20
Mean	61.35
Std Dev	1.621

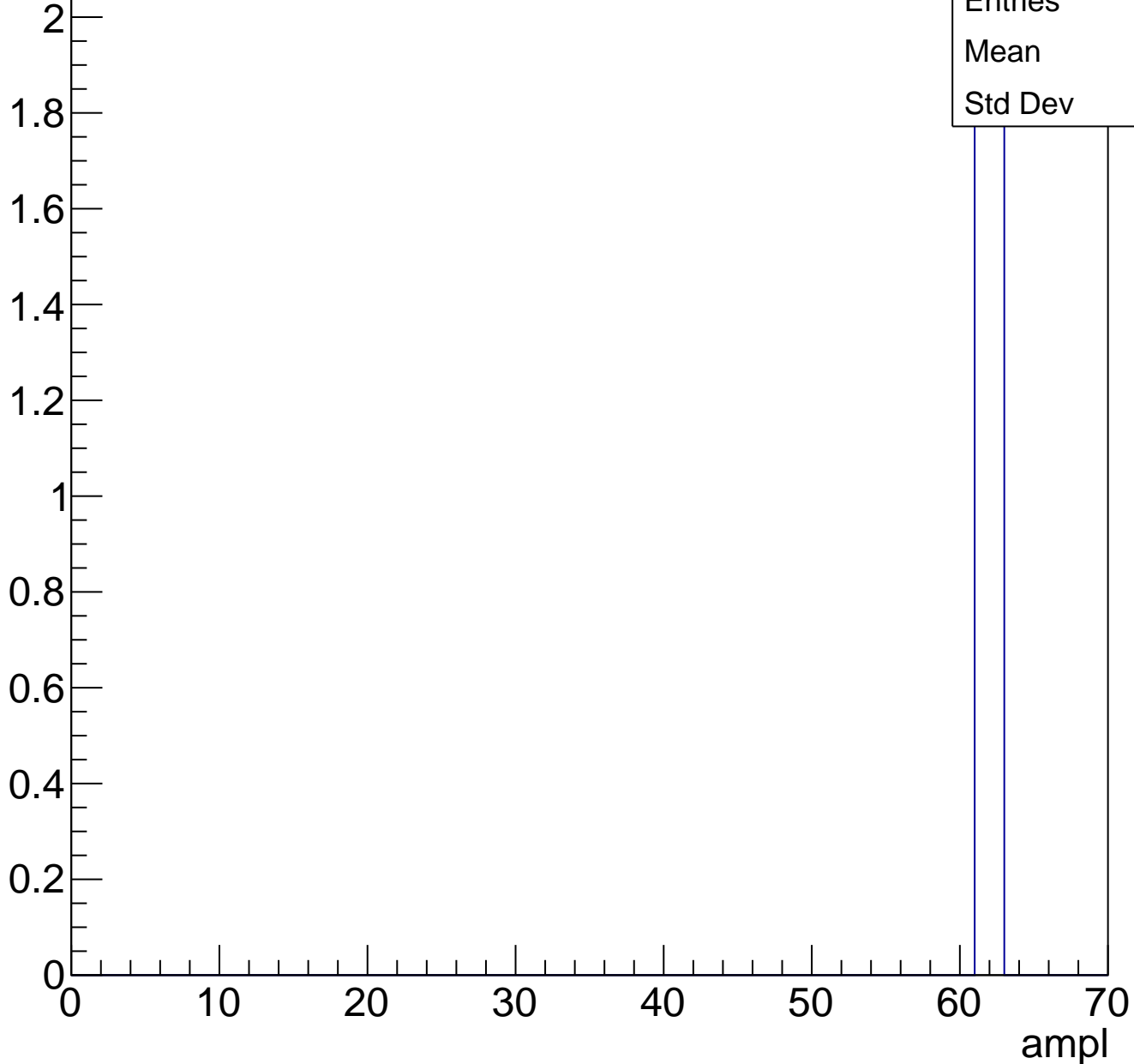




# B1L103S, U1-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch124, adc0

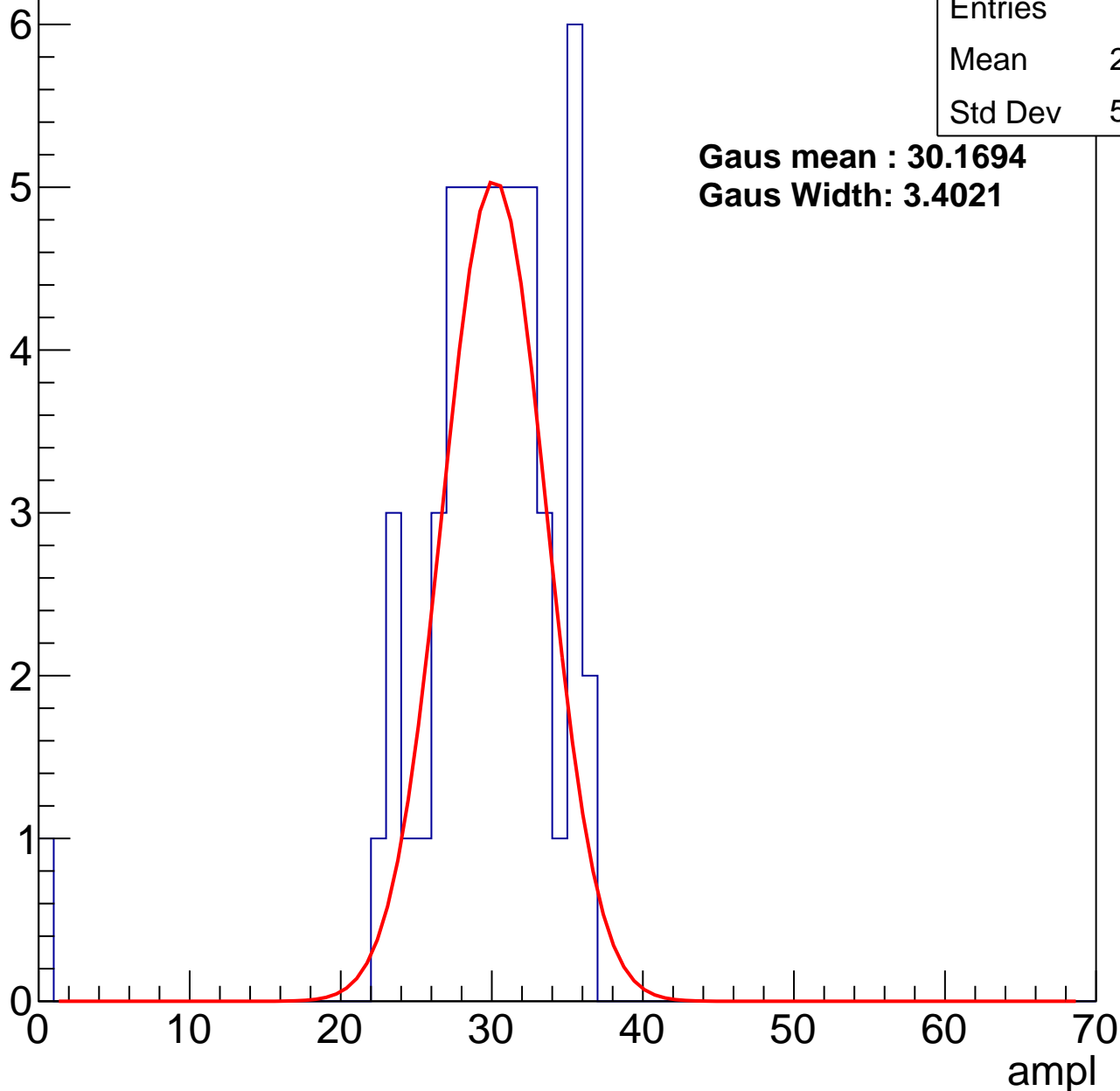
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	29.19
Std Dev	5.453

**Gaus mean : 30.1694**

**Gaus Width: 3.4021**



# B1L103S, U1-ch124, adc1

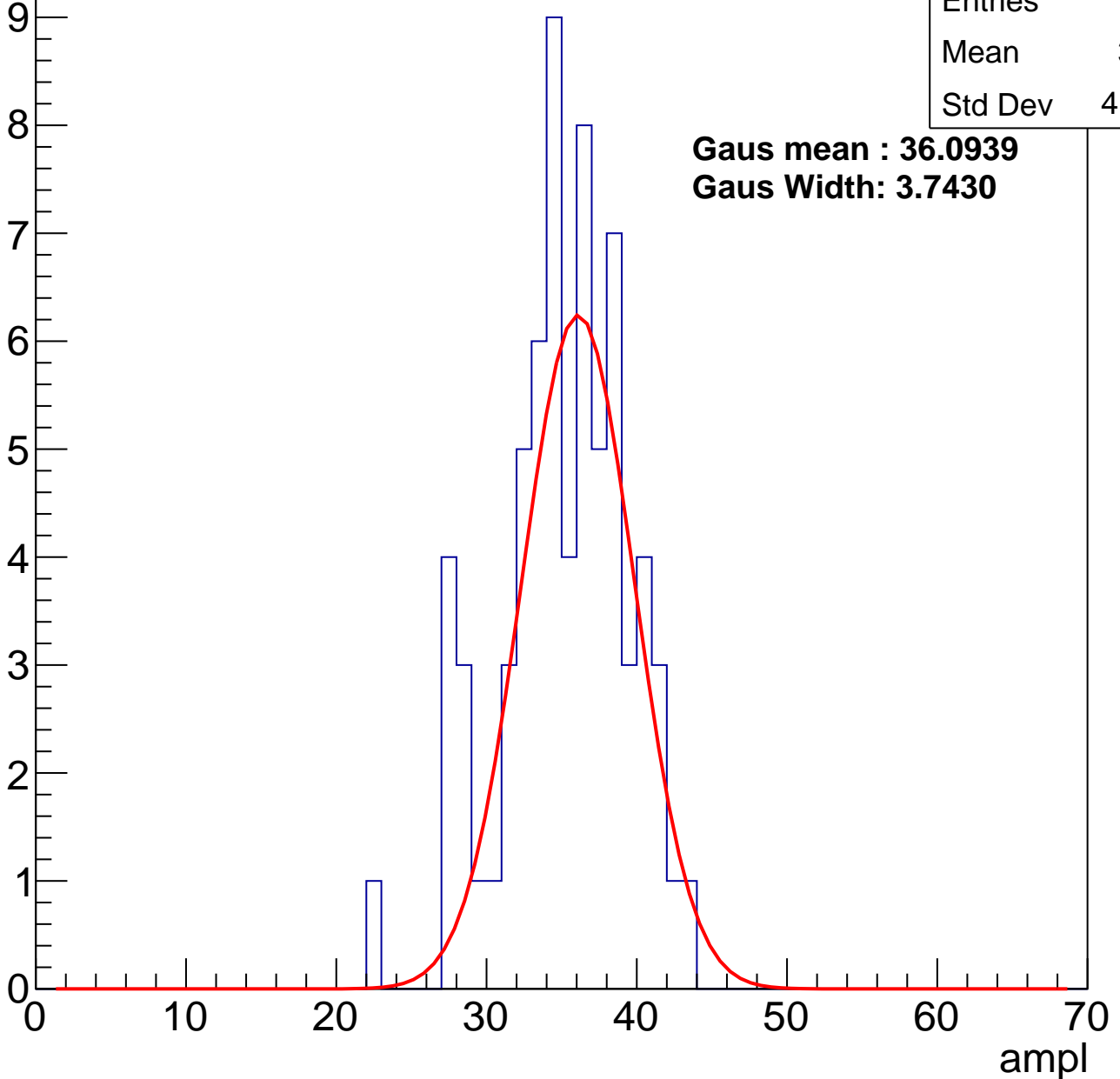
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	34.7
Std Dev	4.192

**Gaus mean : 36.0939**

**Gaus Width: 3.7430**



# B1L103S, U1-ch124, adc2

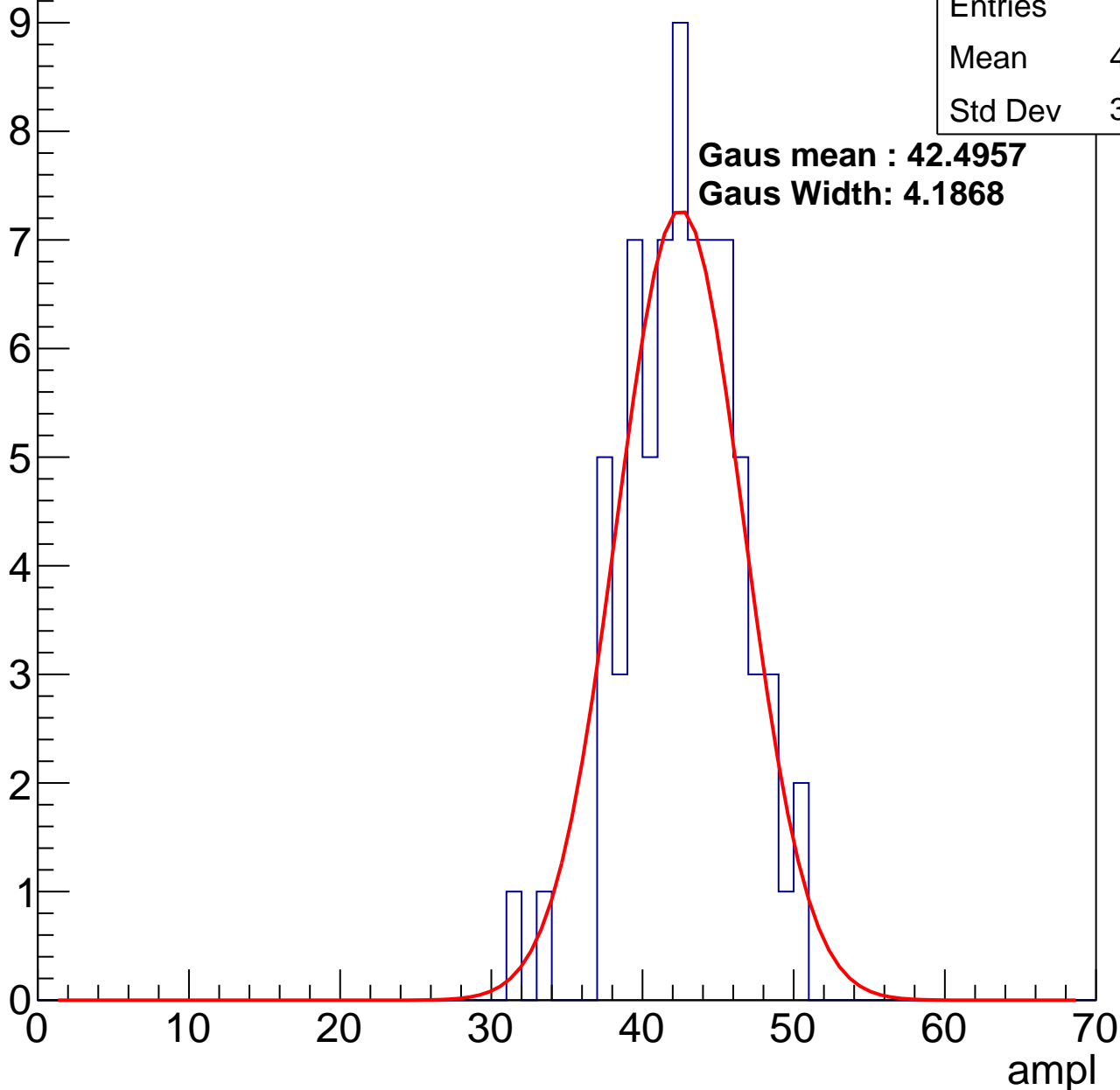
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	42.32
Std Dev	3.693

**Gaus mean : 42.4957**

**Gaus Width: 4.1868**

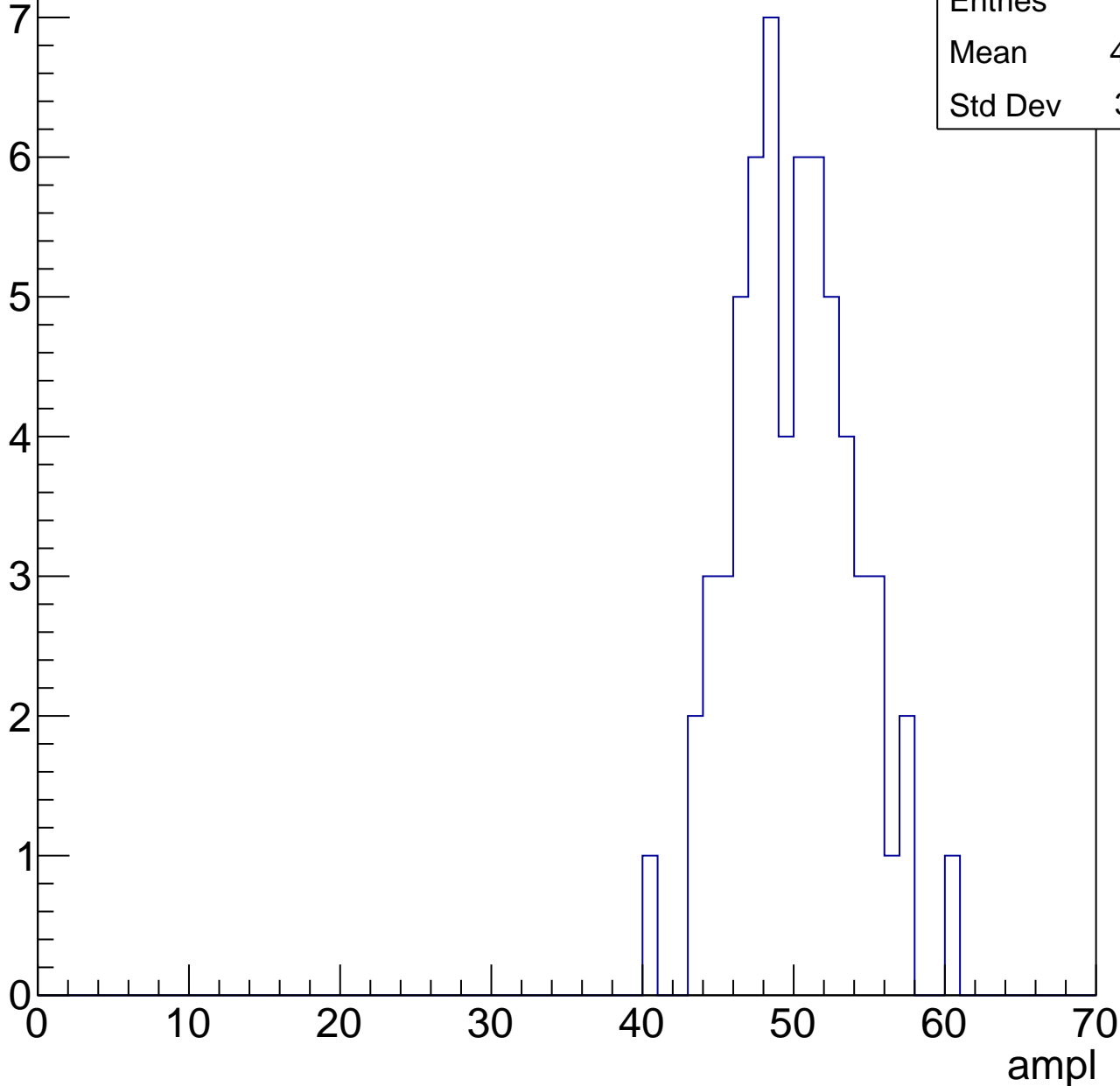


# B1L103S, U1-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	49.55
Std Dev	3.921

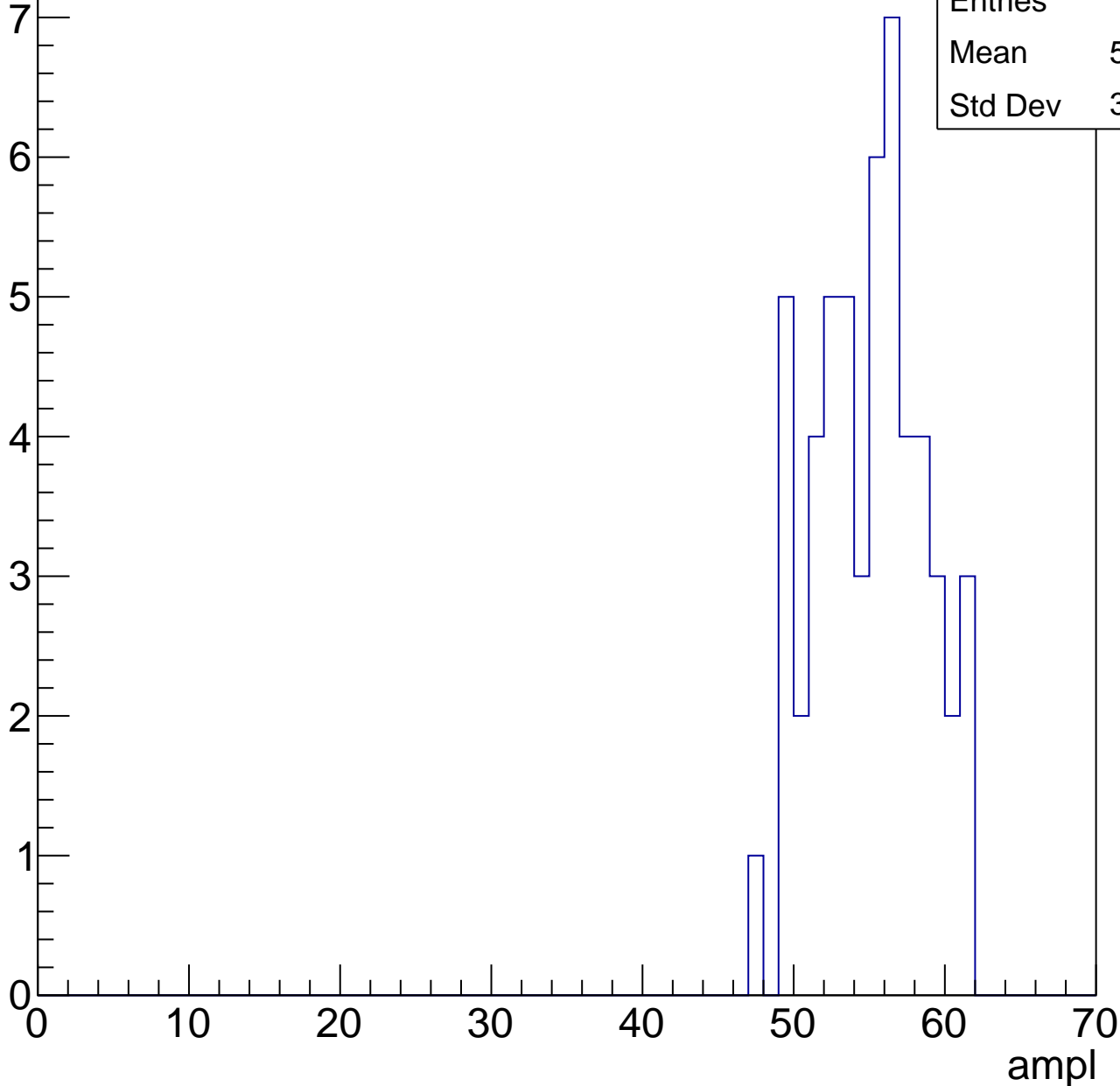


# B1L103S, U1-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	54.54
Std Dev	3.547

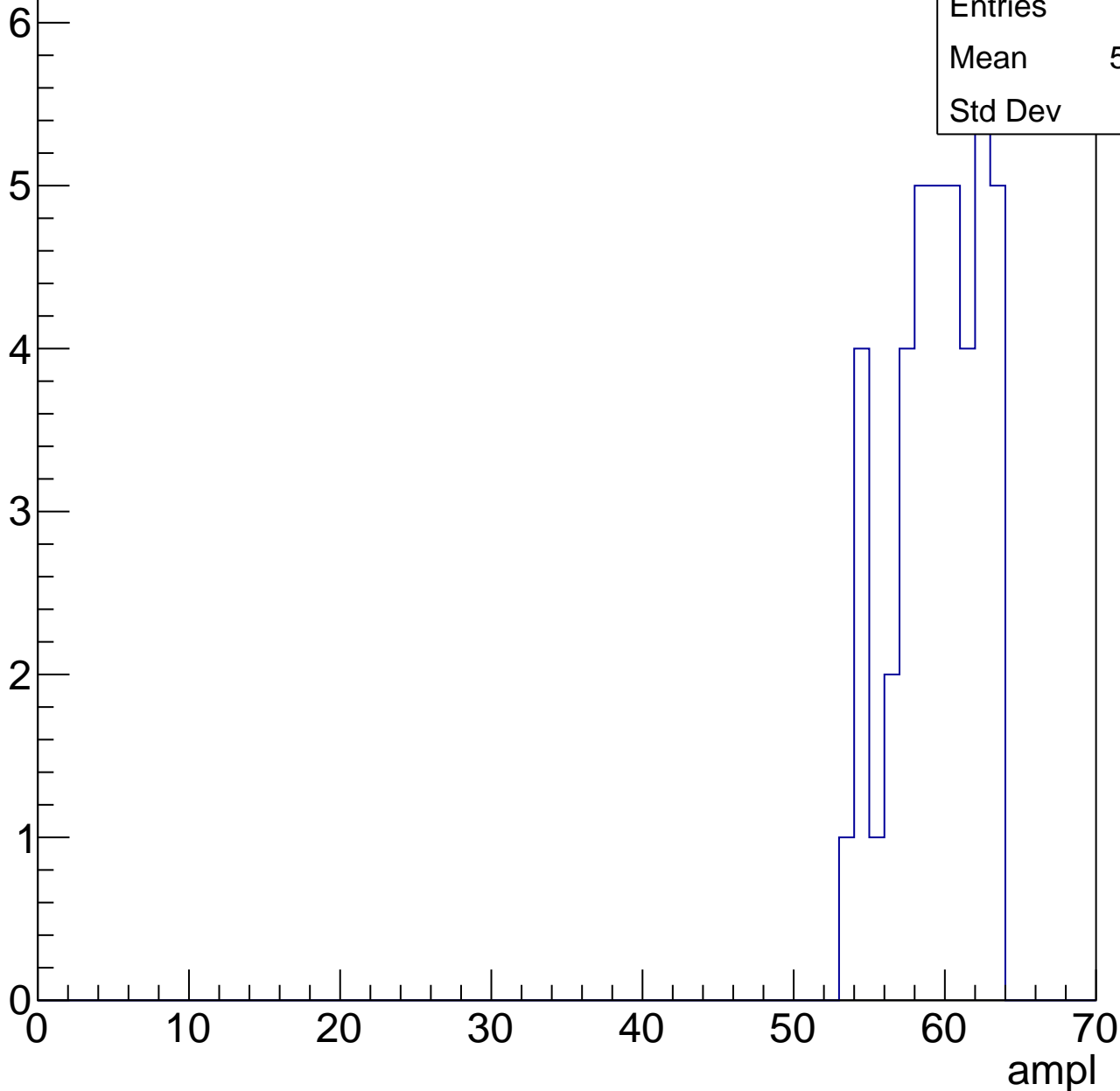


# B1L103S, U1-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

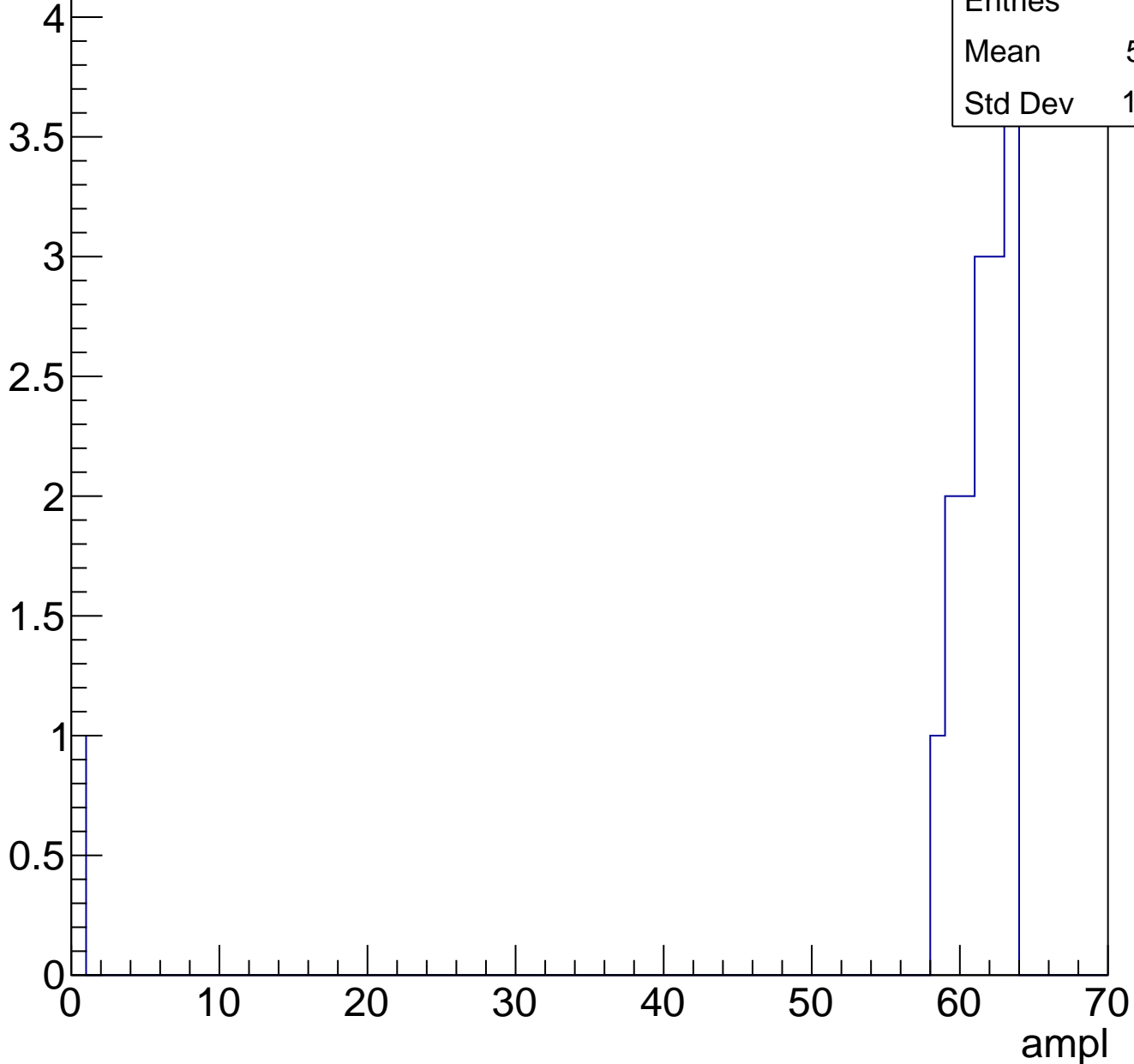
Entries	42
Mean	59.05
Std Dev	2.87



# B1L103S, U1-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	16
Mean	57.31
Std Dev	14.88



# B1L103S, U1-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	4
Mean	31.25
Std Dev	31.25

# B1L103S, U1-ch125, adc0

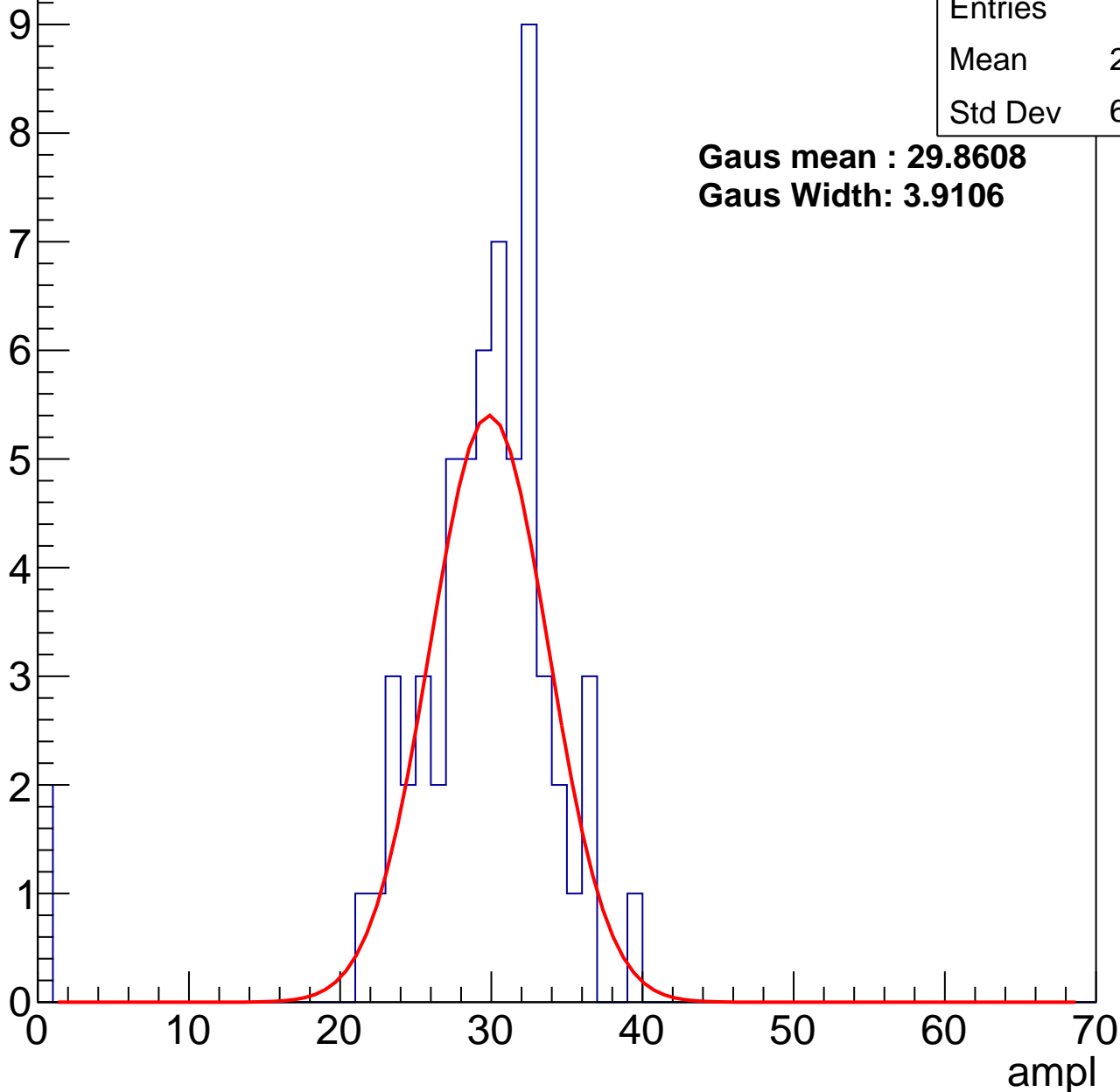
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	28.49
Std Dev	6.424

**Gaus mean : 29.8608**

**Gaus Width: 3.9106**



# B1L103S, U1-ch125, adc1

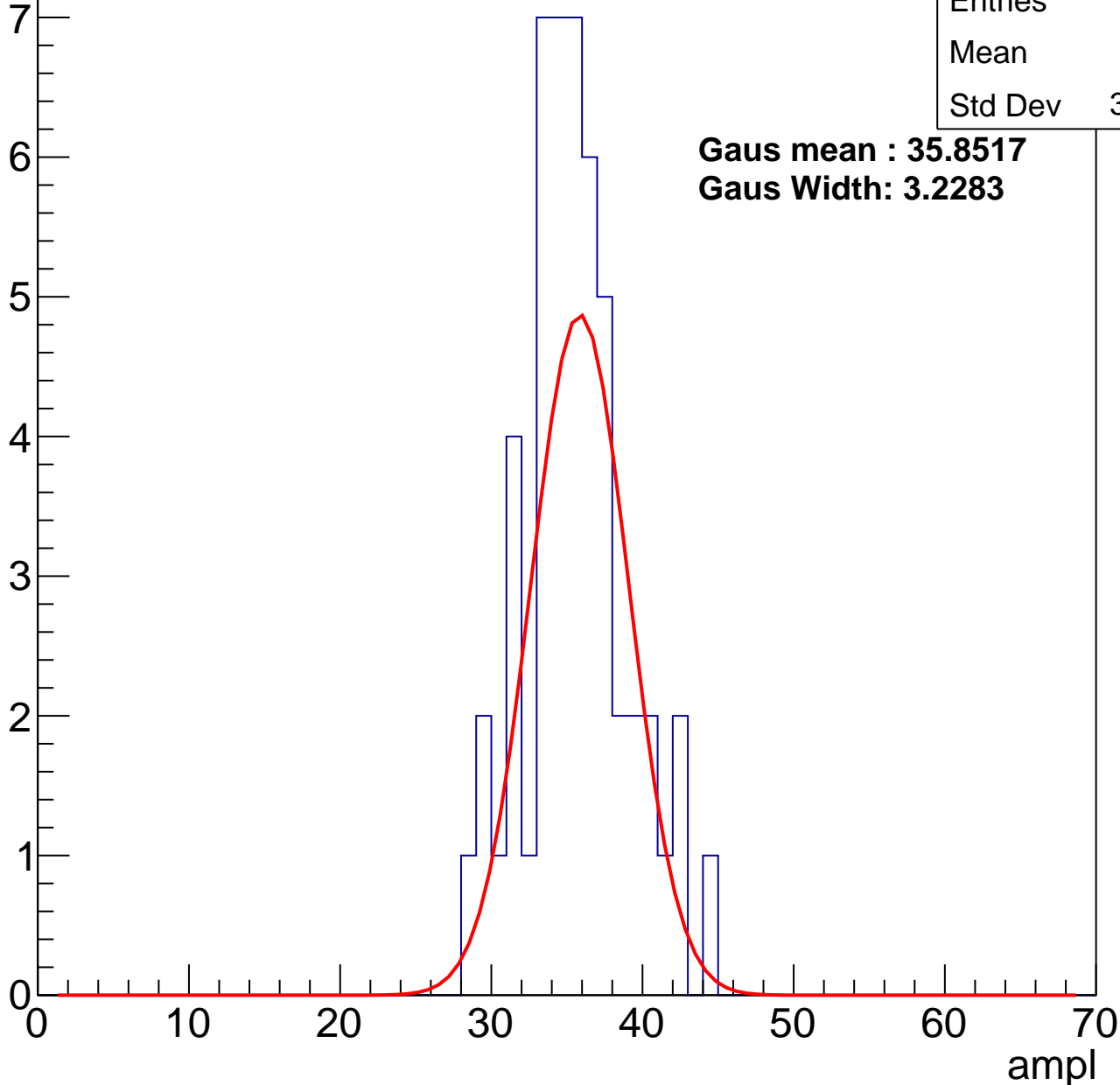
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	35.1
Std Dev	3.414

**Gaus mean : 35.8517**

**Gaus Width: 3.2283**



# B1L103S, U1-ch125, adc2

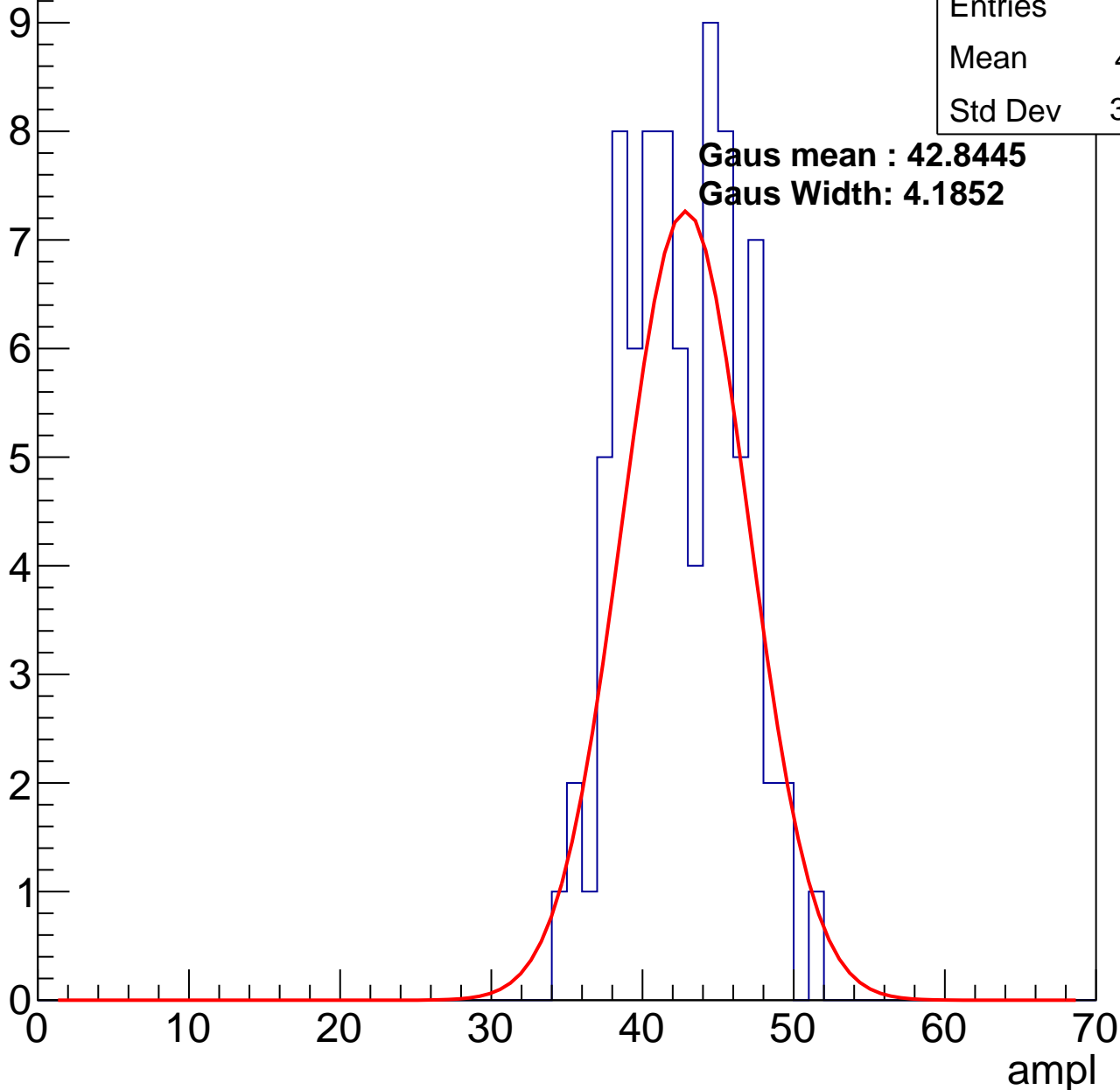
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	42.11
Std Dev	3.742

**Gaus mean : 42.8445**

**Gaus Width: 4.1852**

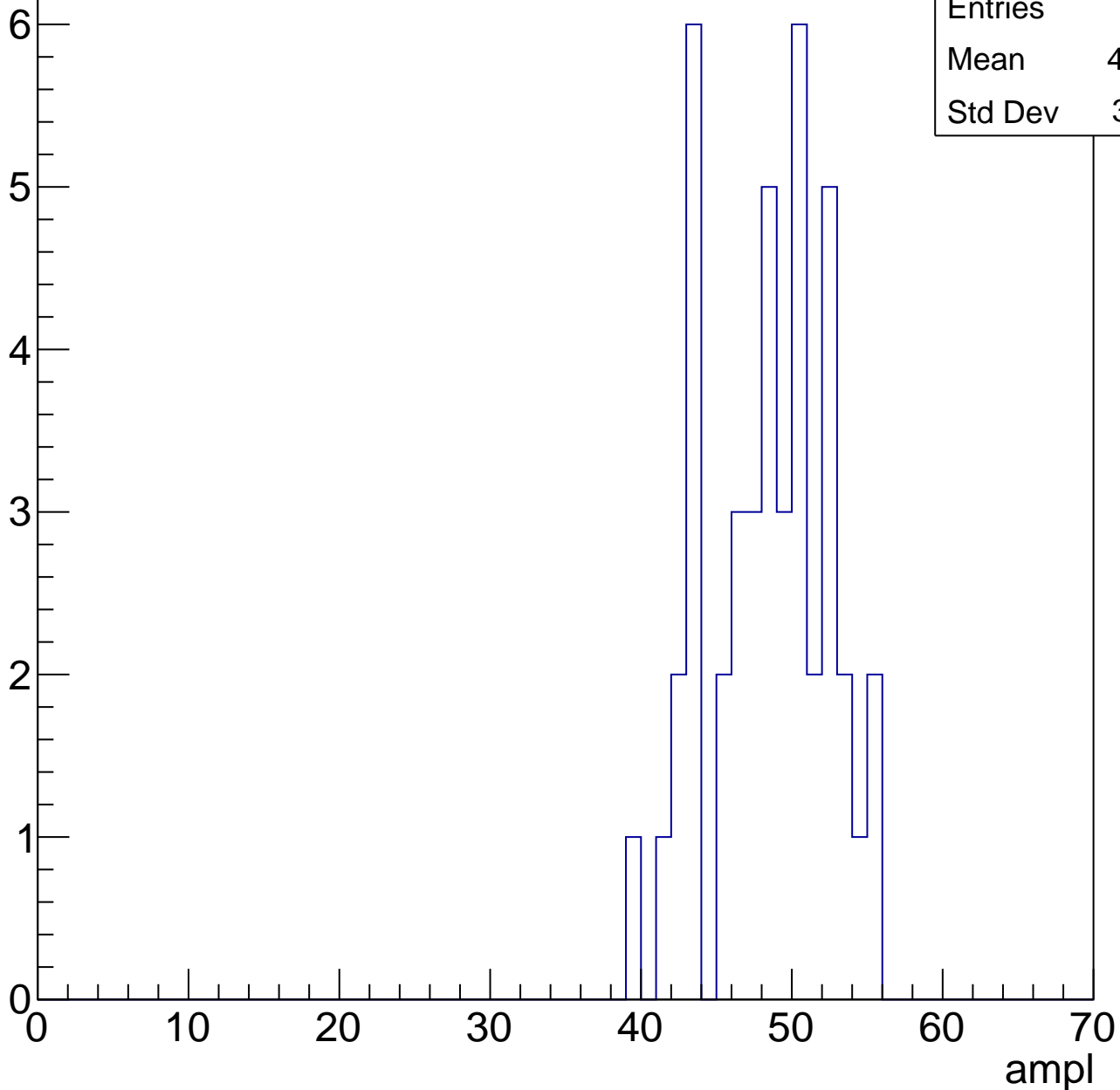


# B1L103S, U1-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

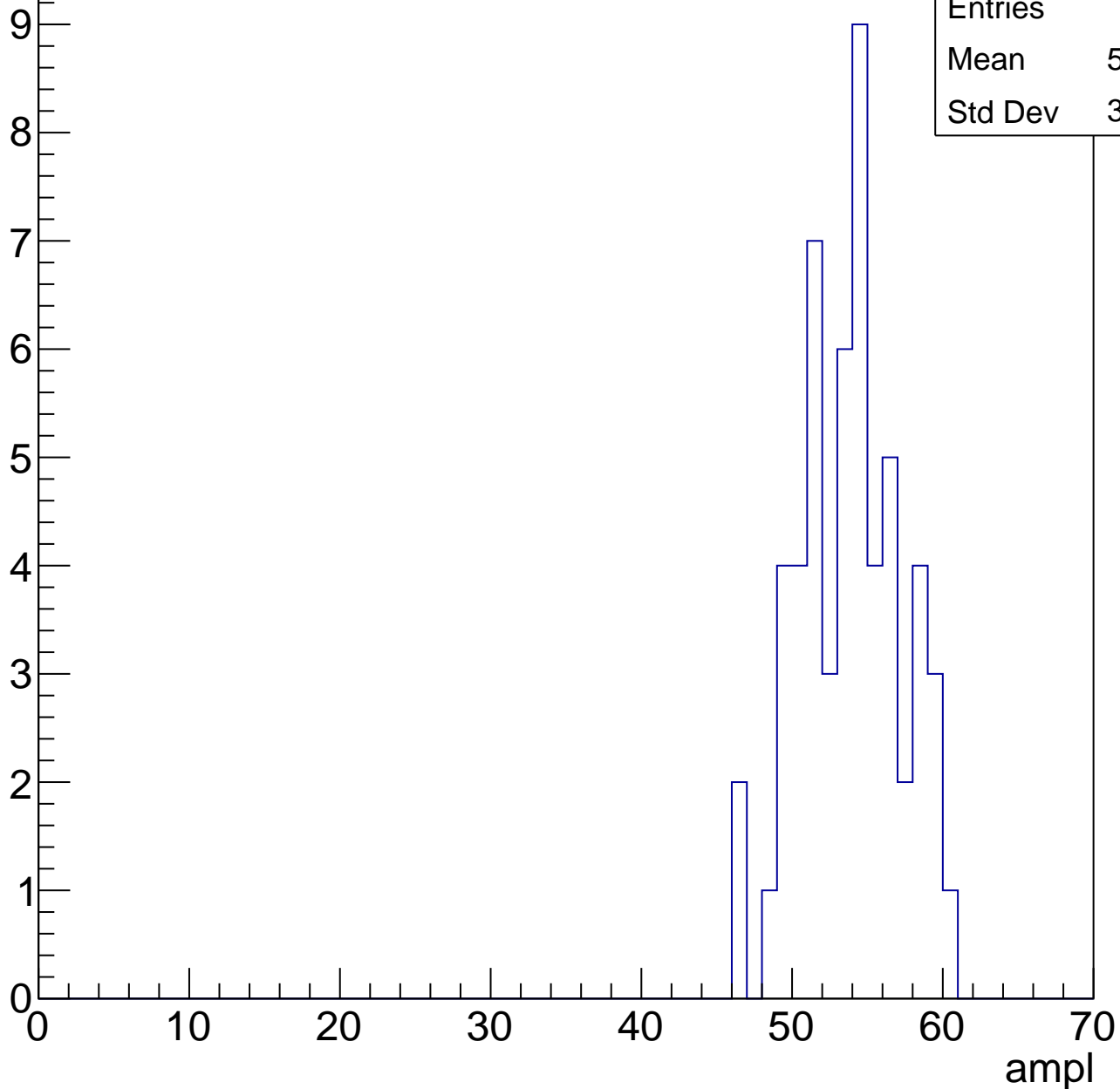
Entries	44
Mean	47.95
Std Dev	3.971



# B1L103S, U1-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

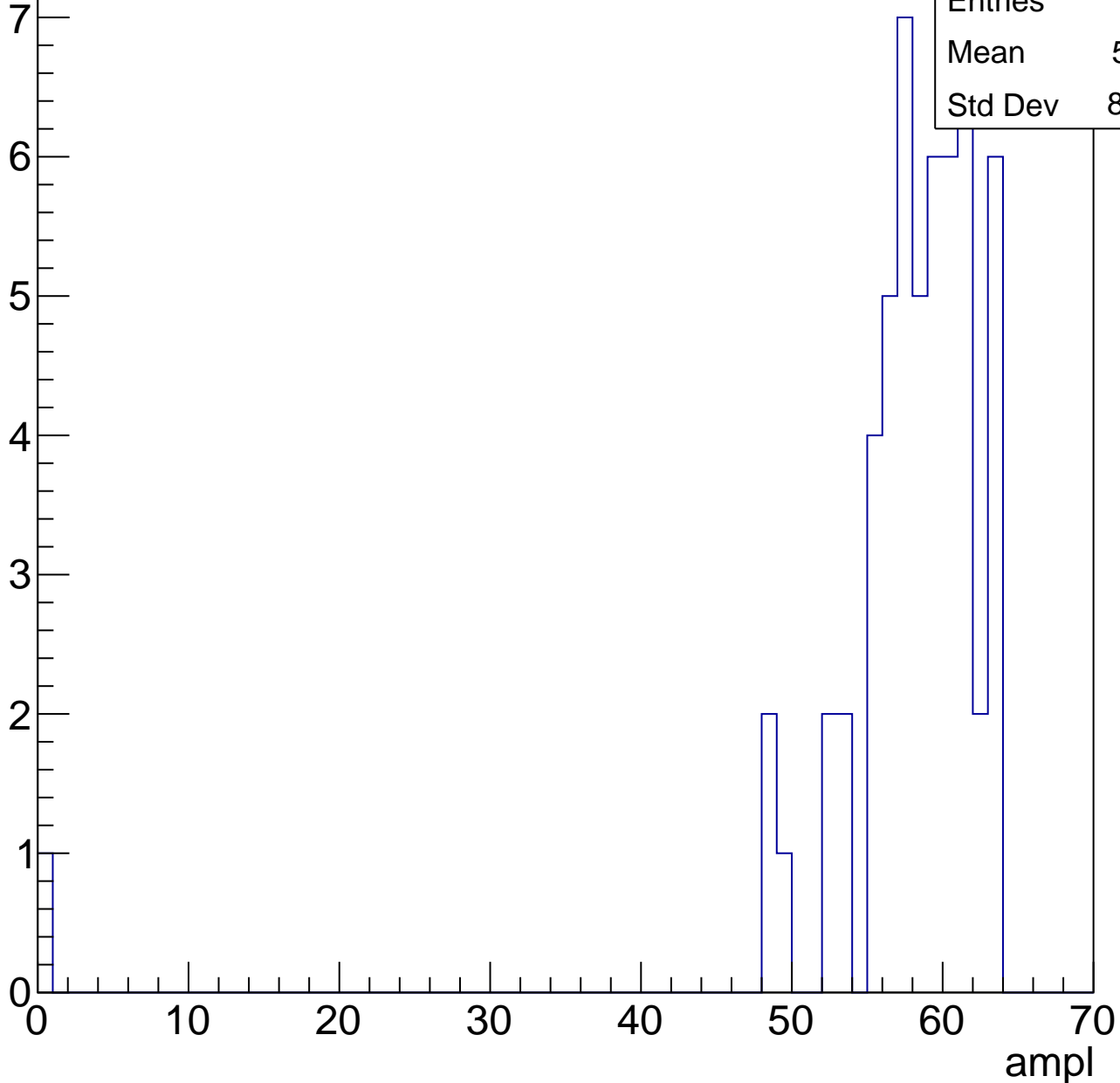


# B1L103S, U1-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	56.91
Std Dev	8.492

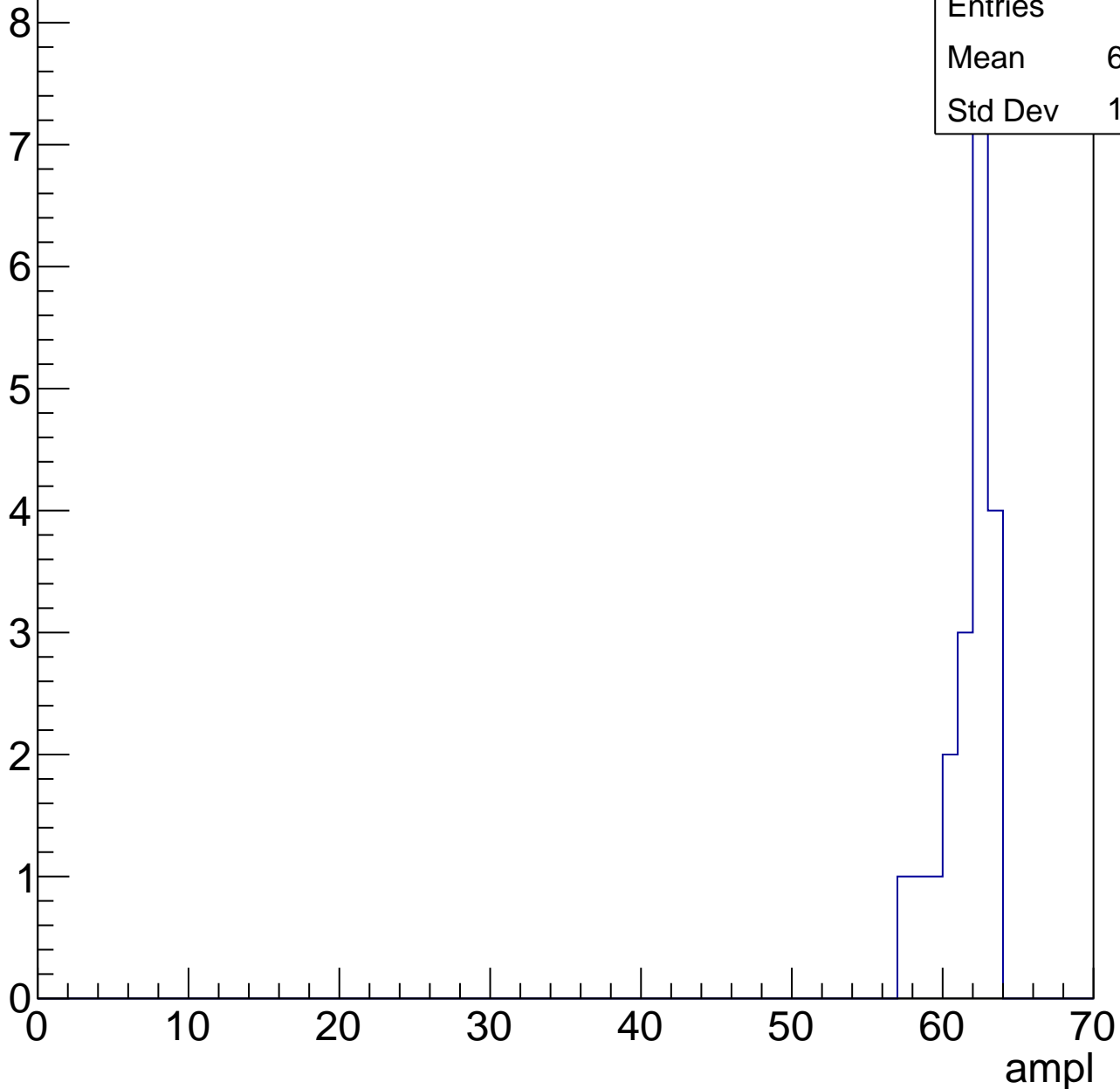


# B1L103S, U1-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	20
Mean	61.25
Std Dev	1.639

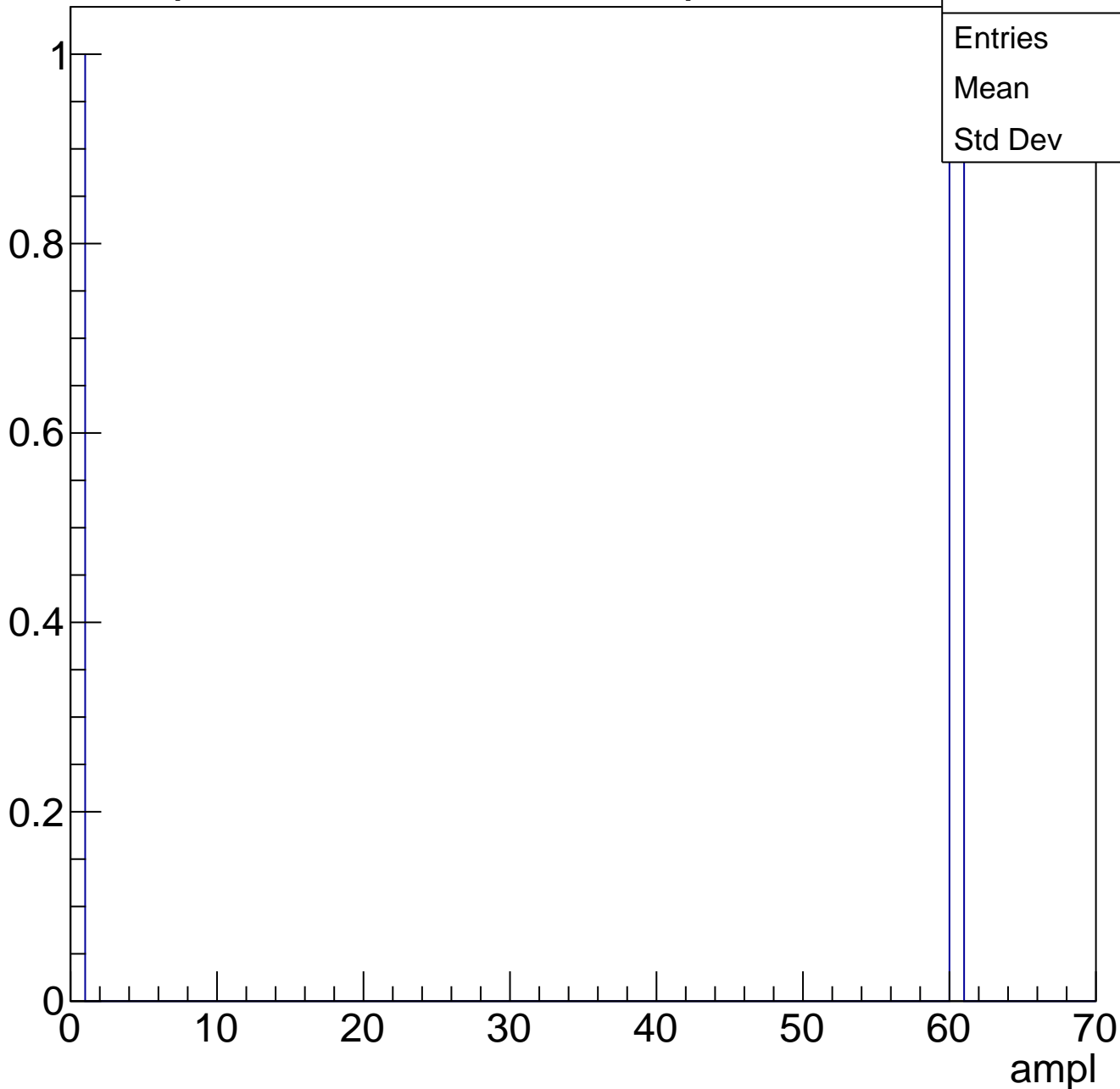




# B1L103S, U1-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch126, adc0

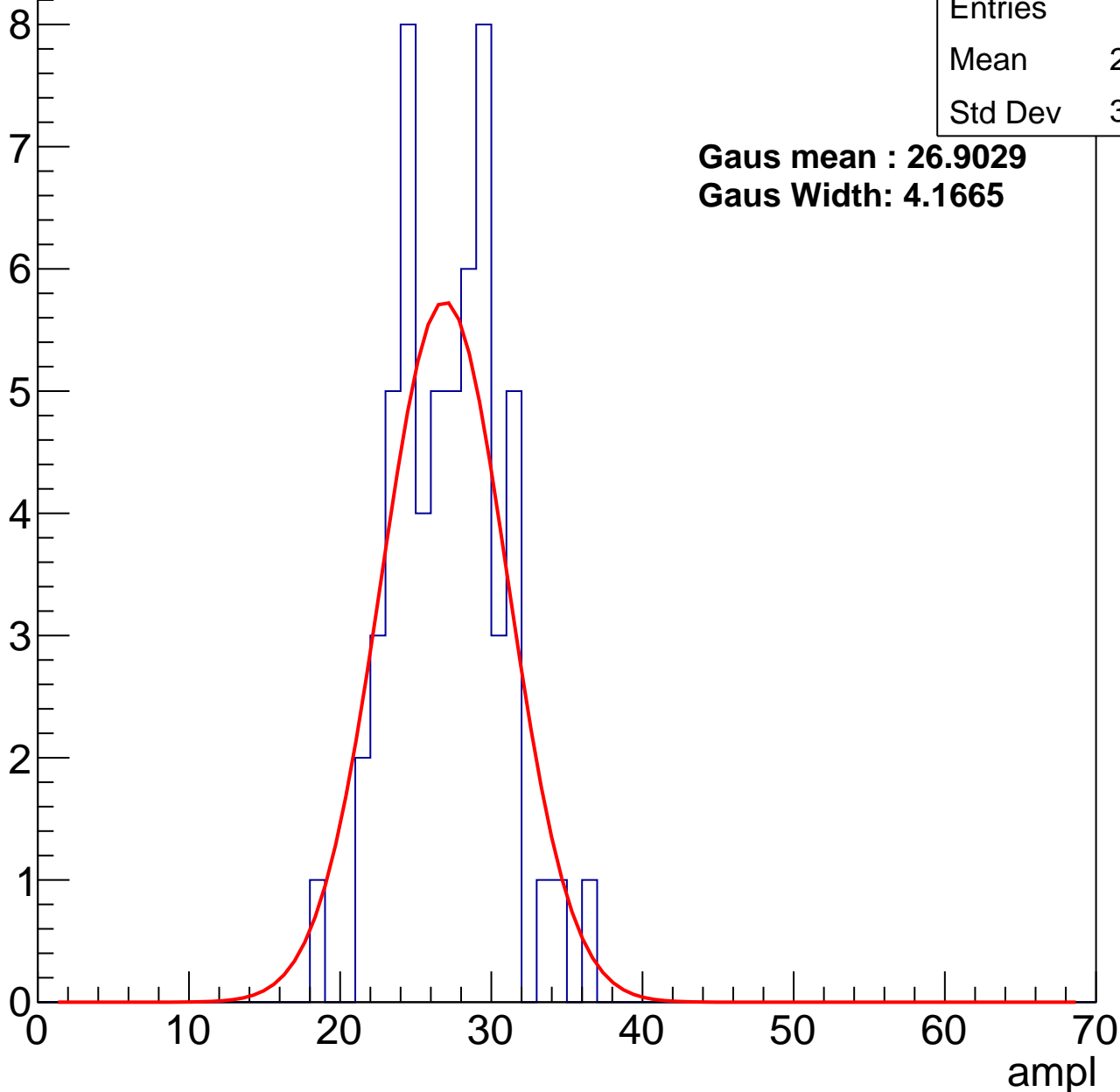
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	26.66
Std Dev	3.487

**Gaus mean : 26.9029**

**Gaus Width: 4.1665**



# B1L103S, U1-ch126, adc1

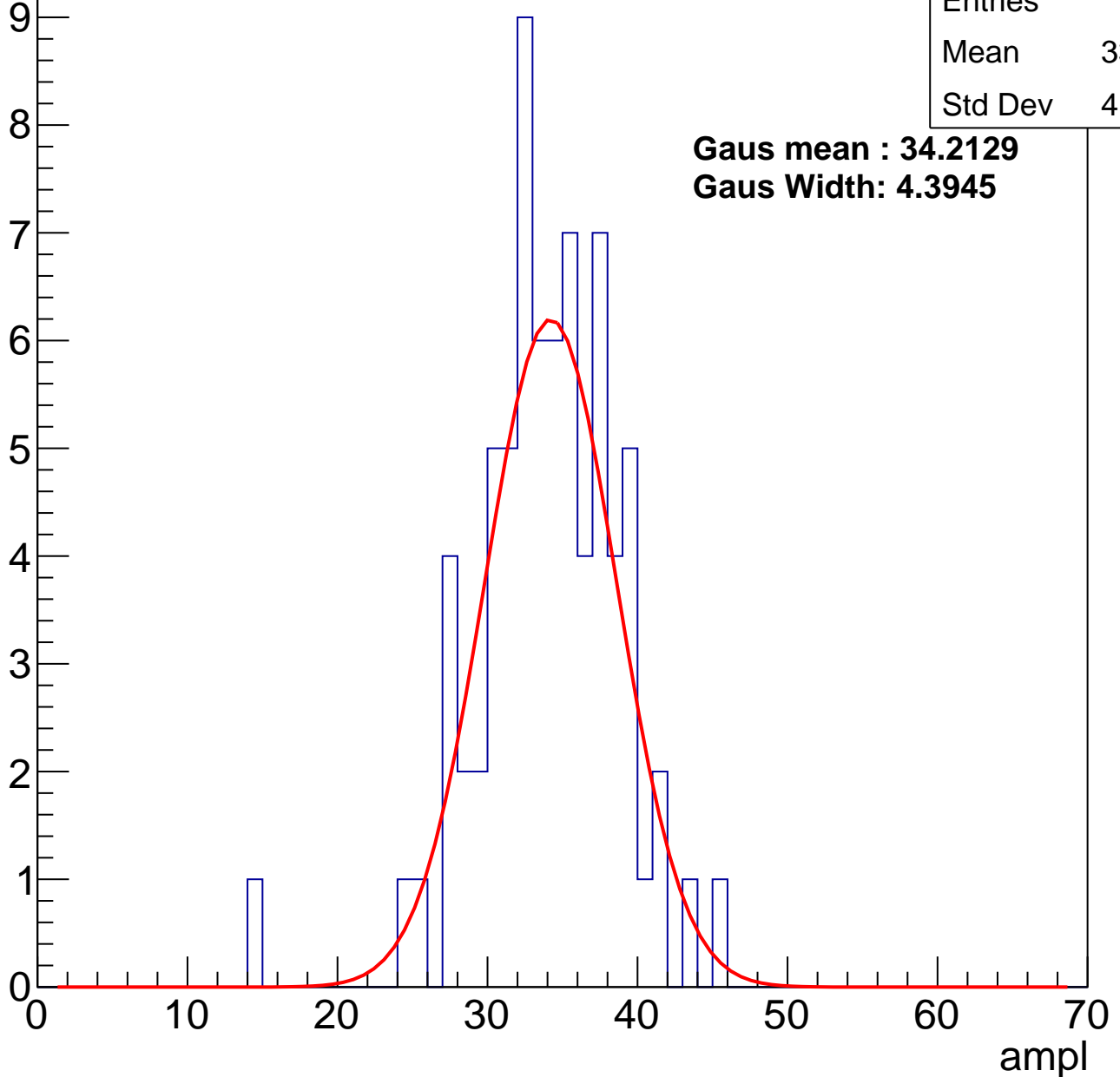
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	33.58
Std Dev	4.742

**Gaus mean : 34.2129**

**Gaus Width: 4.3945**



# B1L103S, U1-ch126, adc2

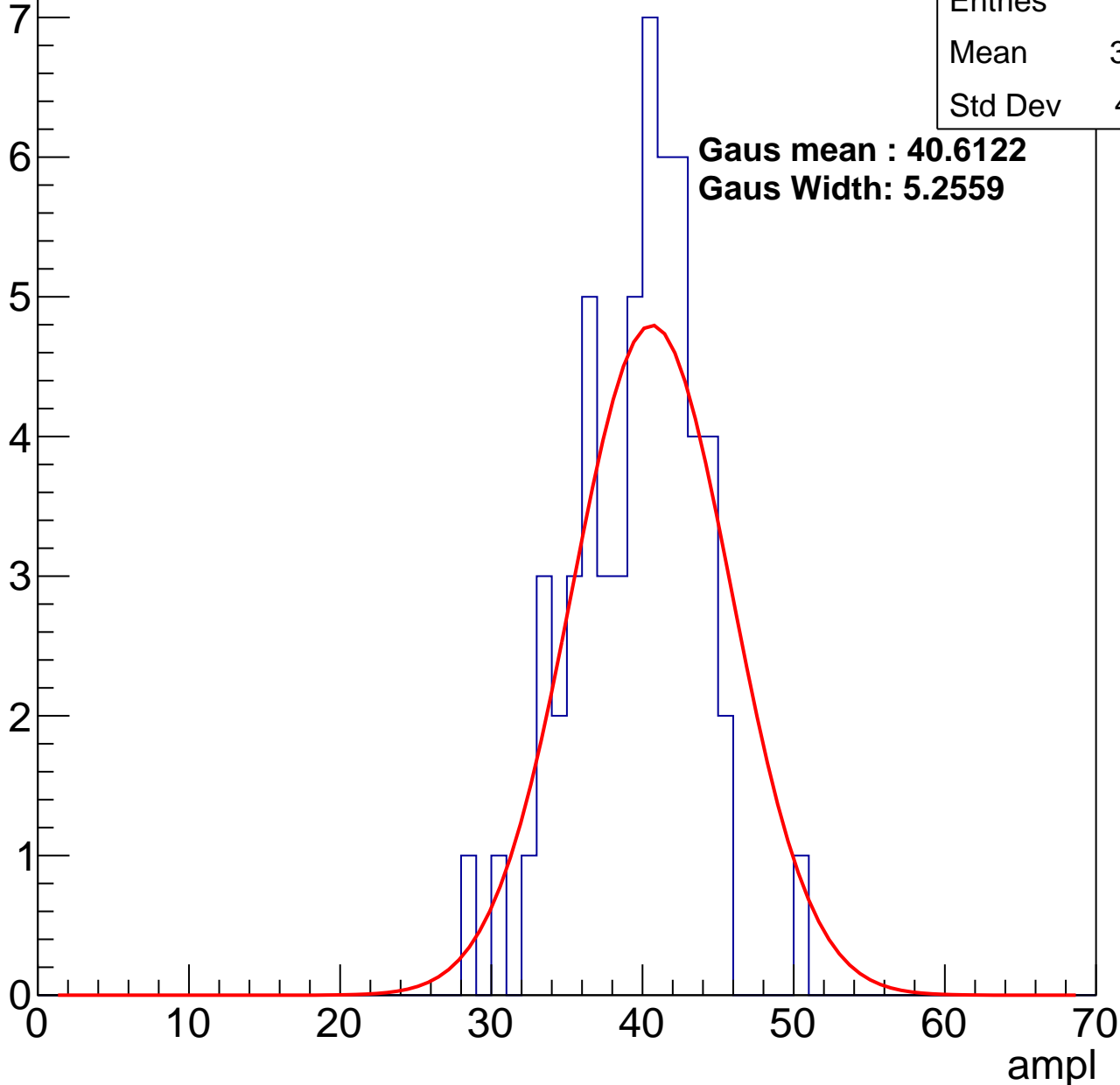
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	39.09
Std Dev	4.101

**Gaus mean : 40.6122**

**Gaus Width: 5.2559**

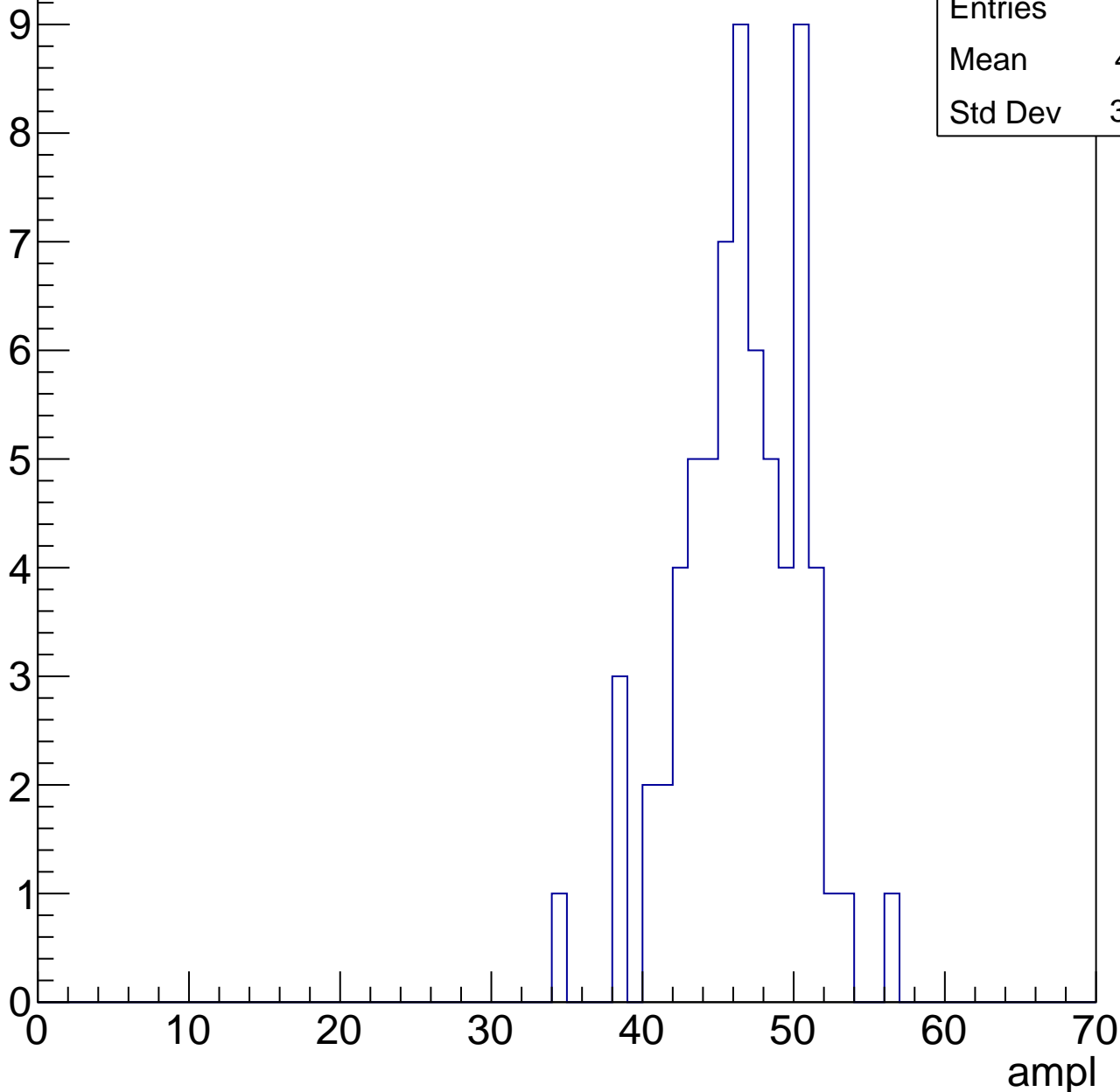


# B1L103S, U1-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	46.01
Std Dev	3.965

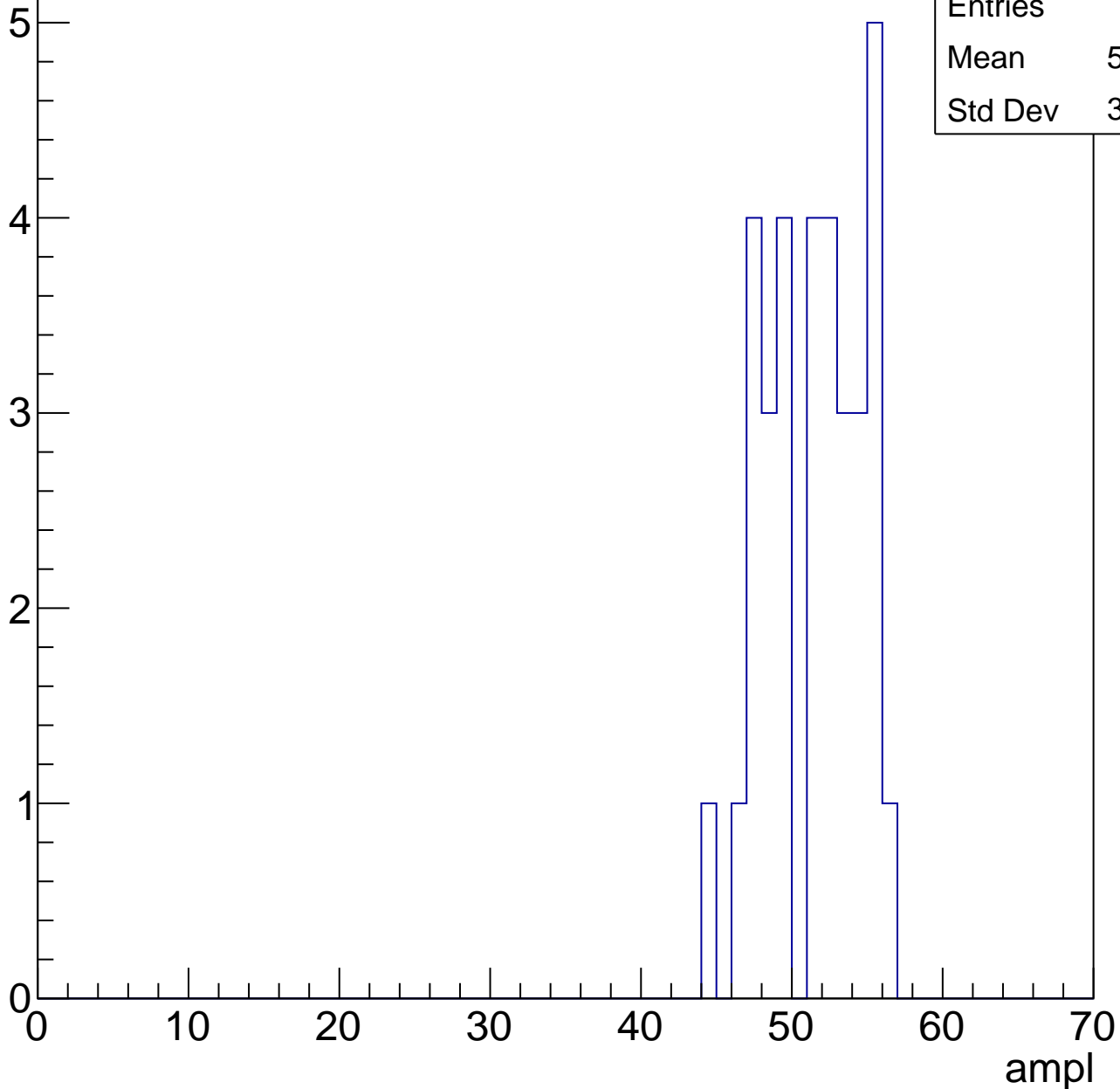


# B1L103S, U1-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	33
Mean	50.97
Std Dev	3.157

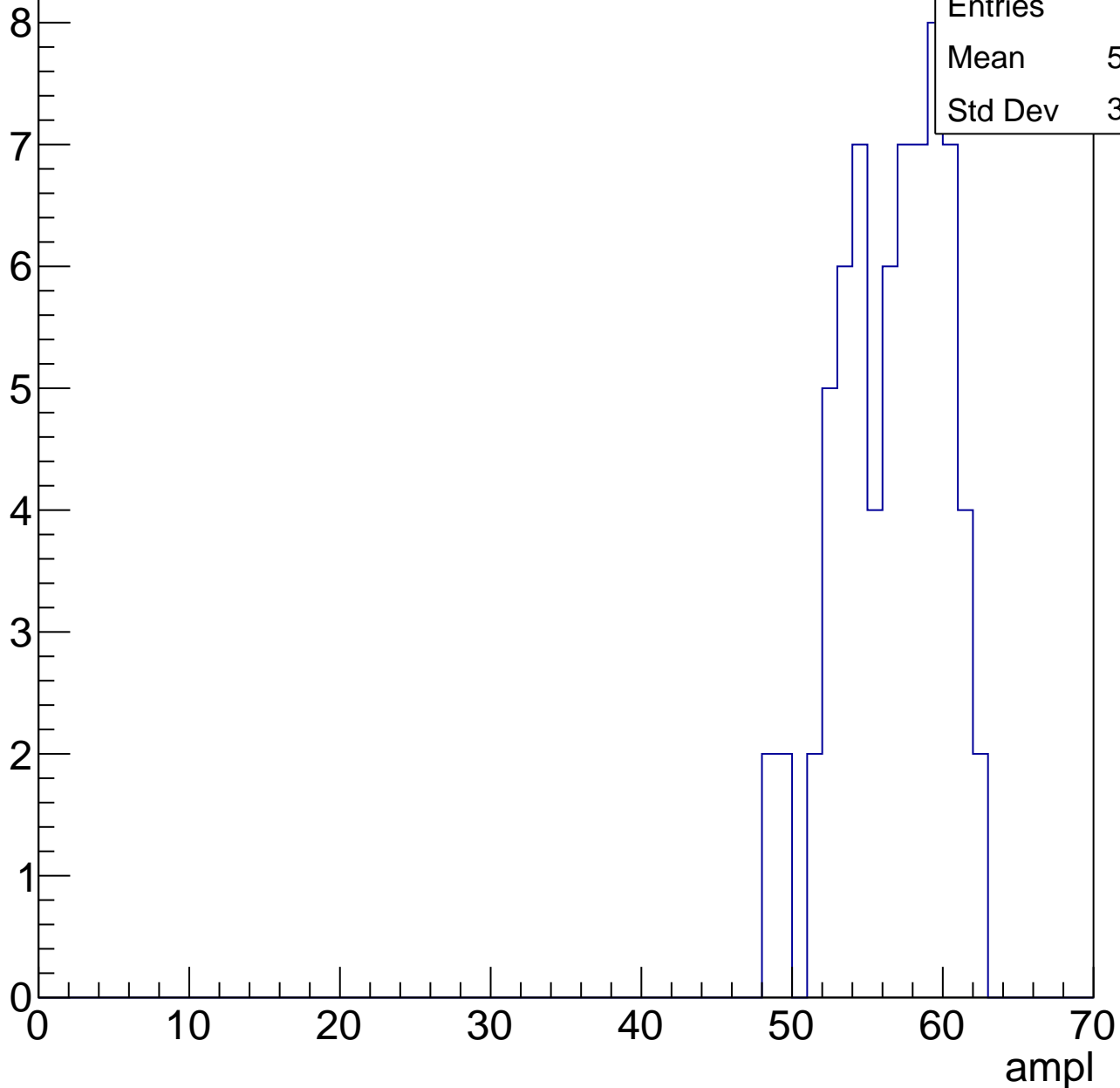


# B1L103S, U1-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	56.13
Std Dev	3.472

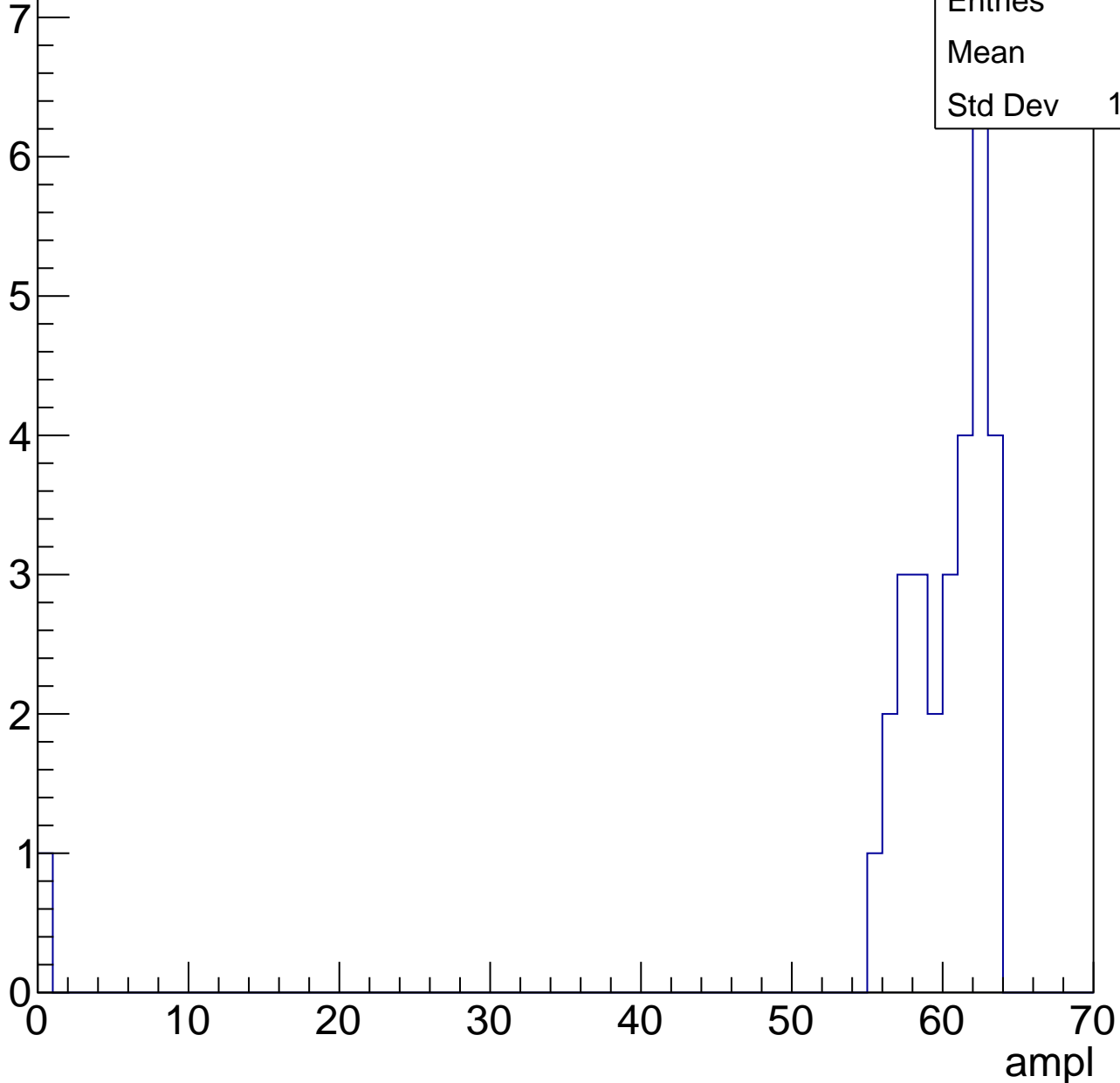


# B1L103S, U1-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	30
Mean	58
Std Dev	11.02

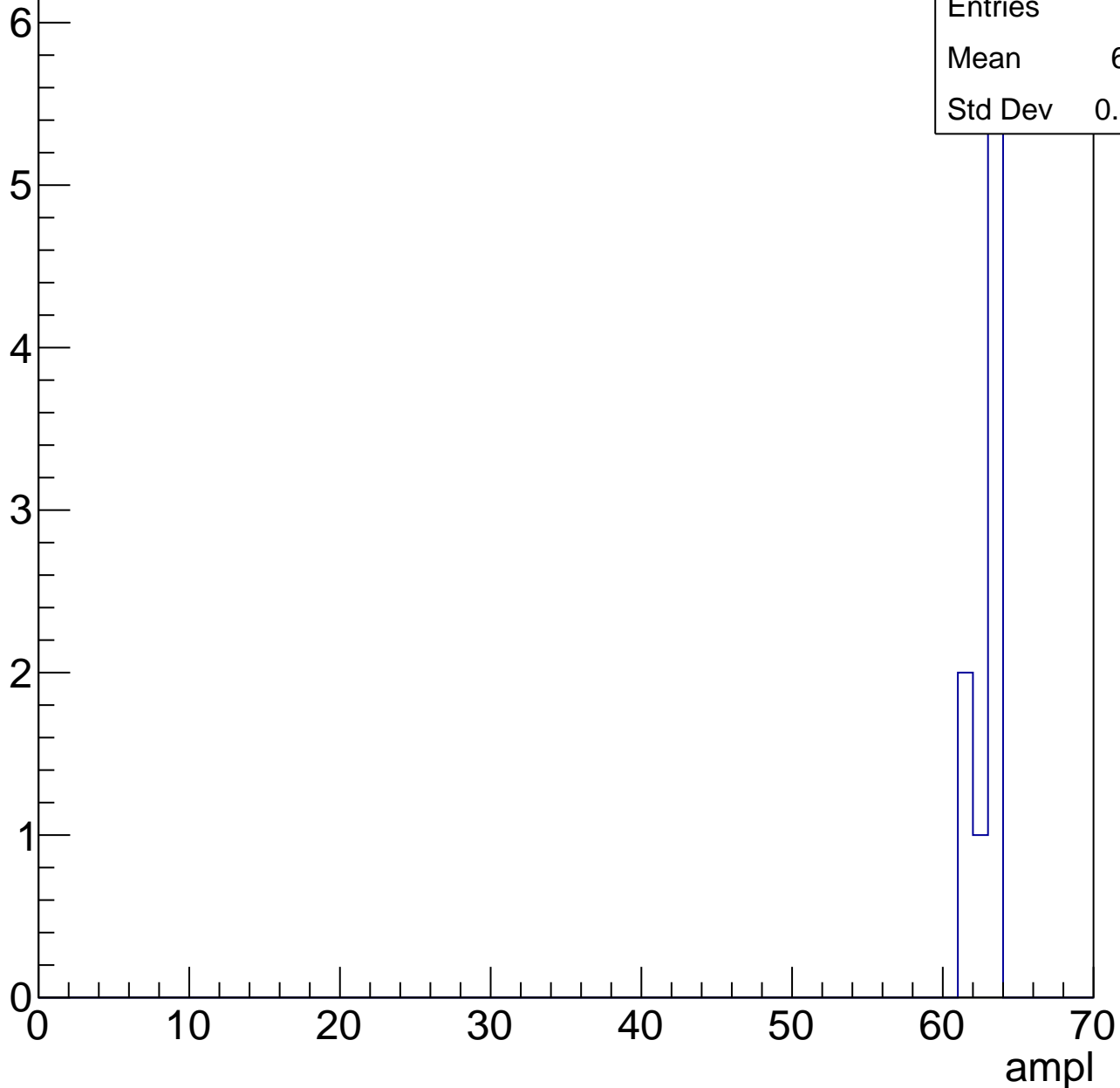




# B1L103S, U1-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch127, adc0

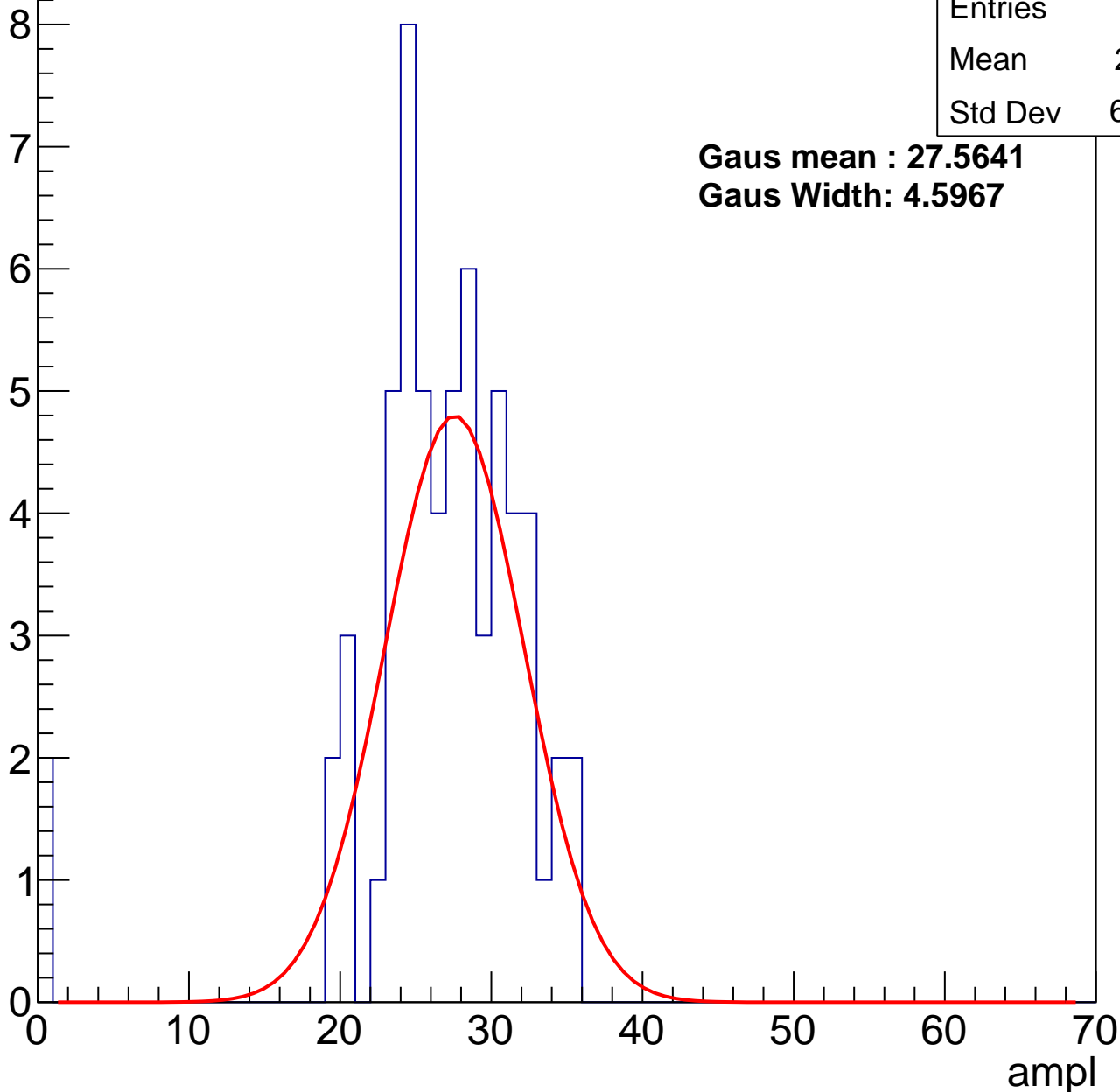
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	26.11
Std Dev	6.188

**Gaus mean : 27.5641**

**Gaus Width: 4.5967**



# B1L103S, U1-ch127, adc1

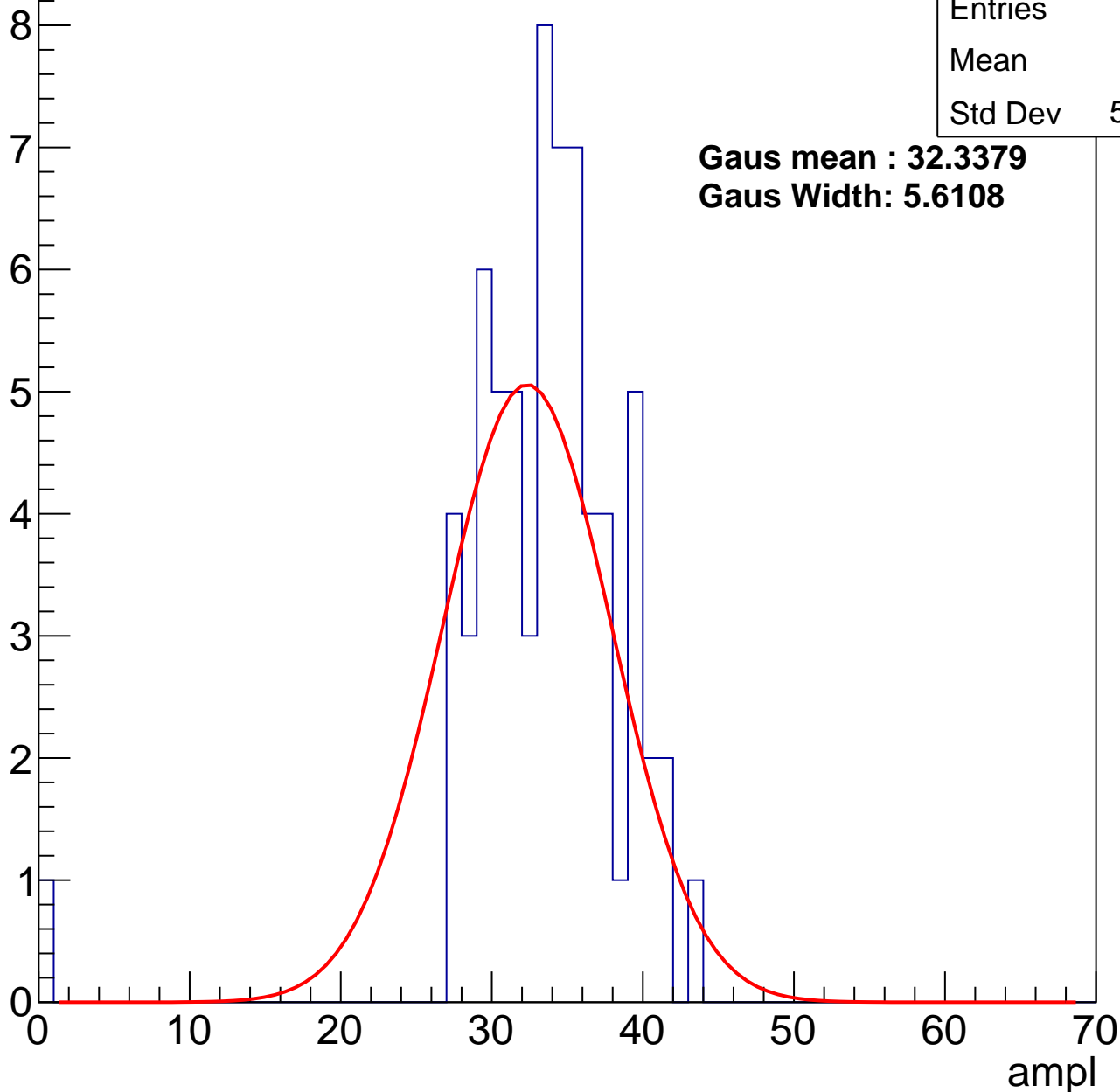
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	33
Std Dev	5.607

**Gaus mean : 32.3379**

**Gaus Width: 5.6108**



# B1L103S, U1-ch127, adc2

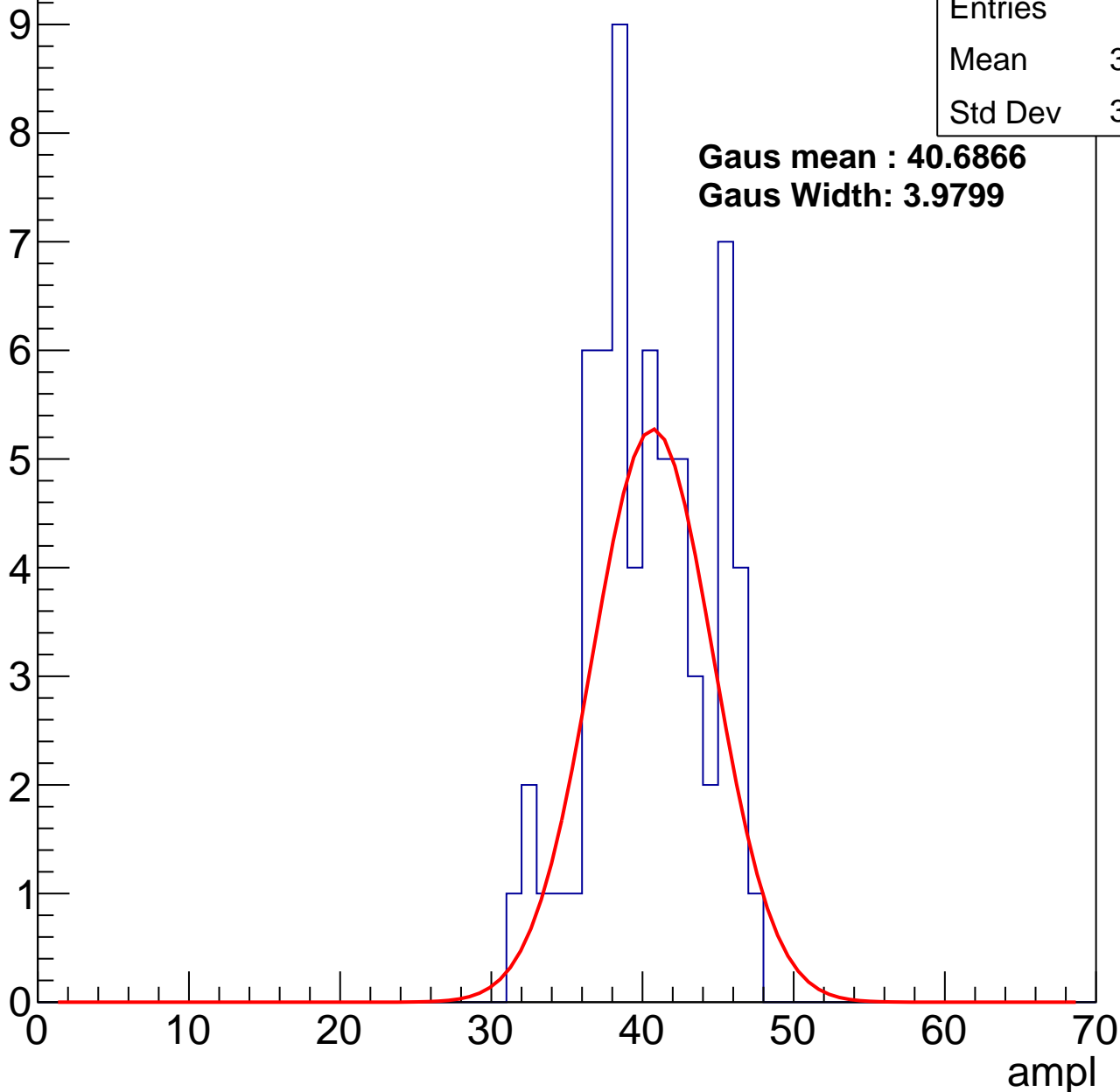
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	39.86
Std Dev	3.872

**Gaus mean : 40.6866**

**Gaus Width: 3.9799**

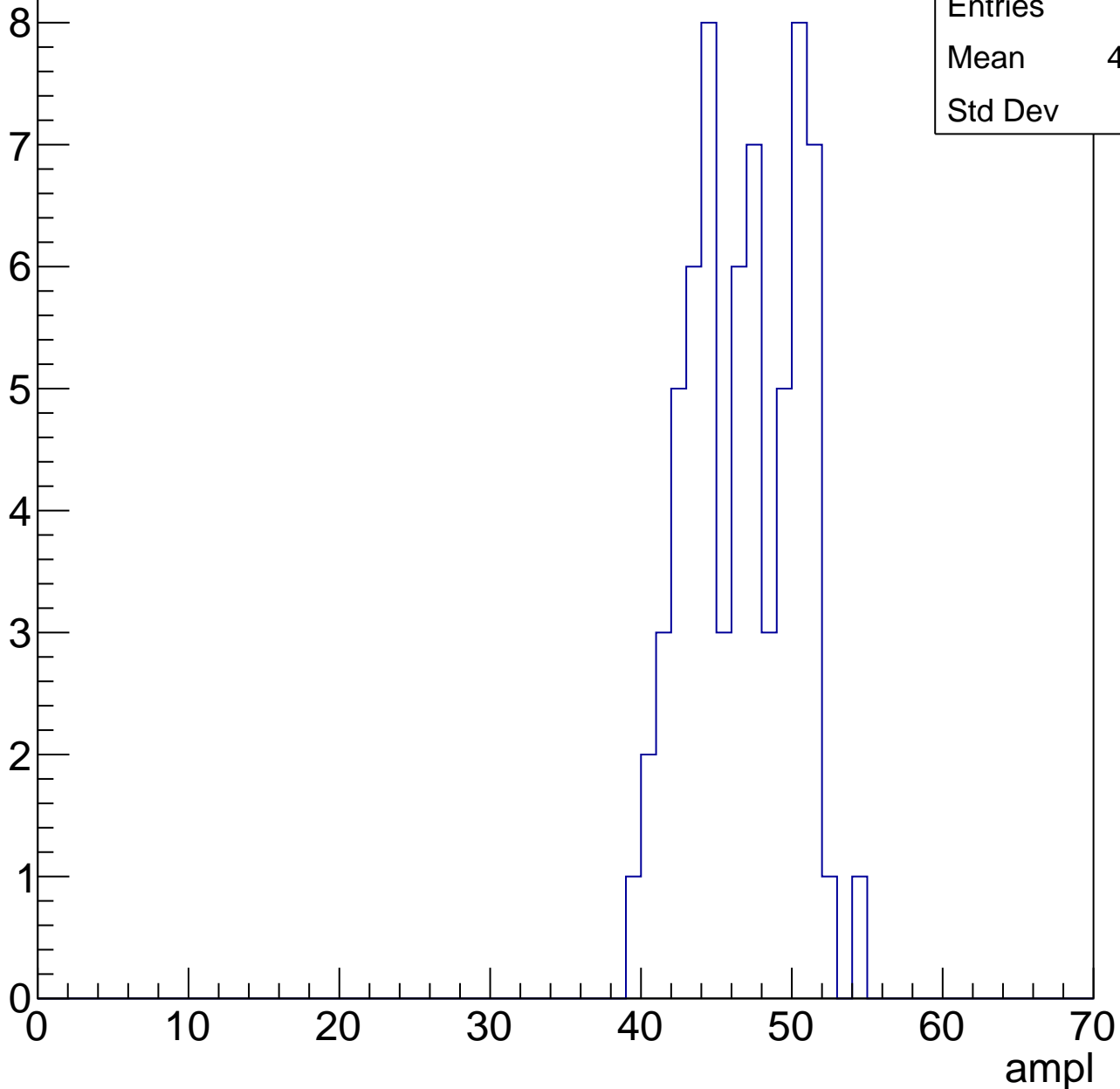


# B1L103S, U1-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	46.27
Std Dev	3.54

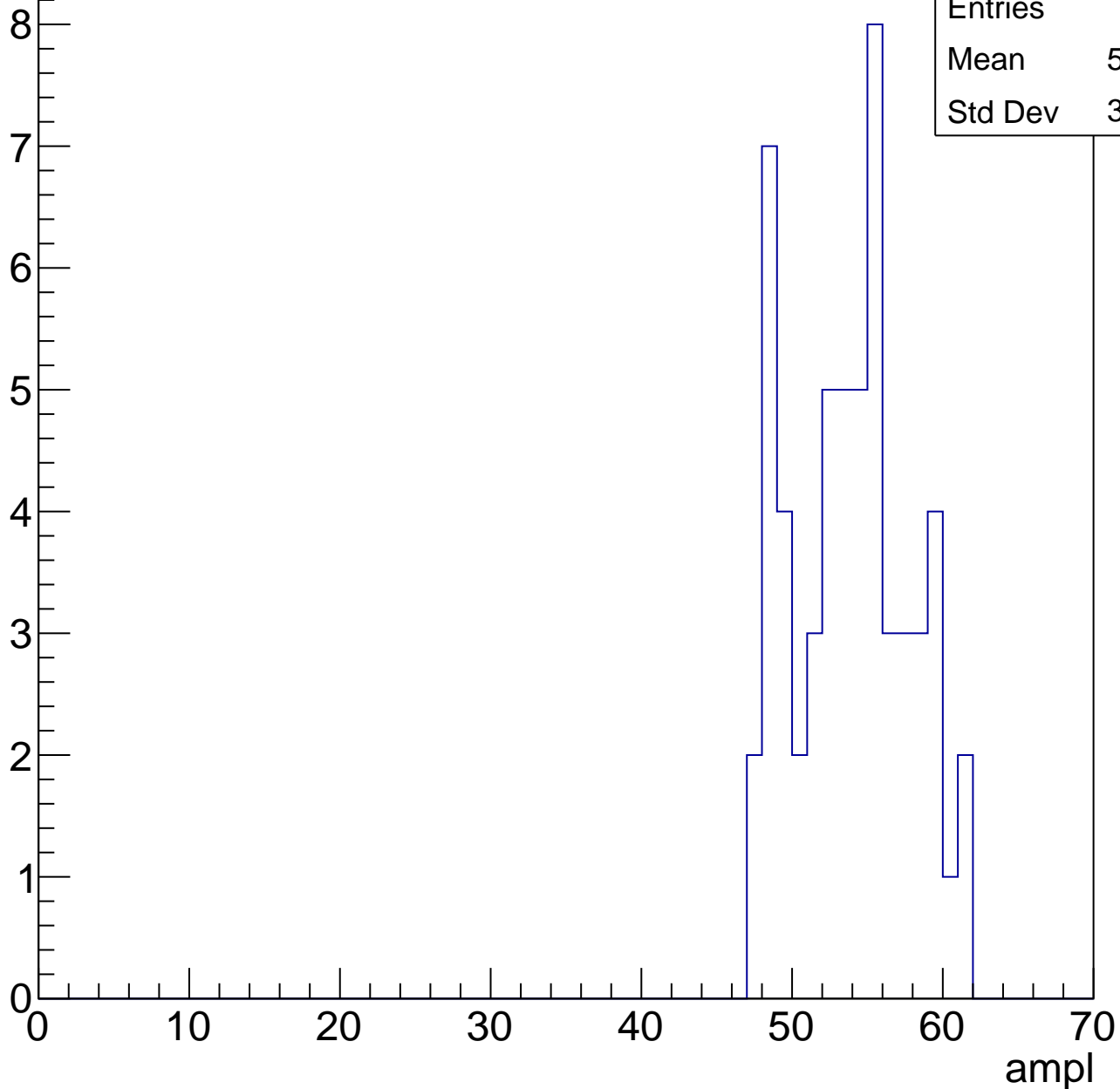


# B1L103S, U1-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

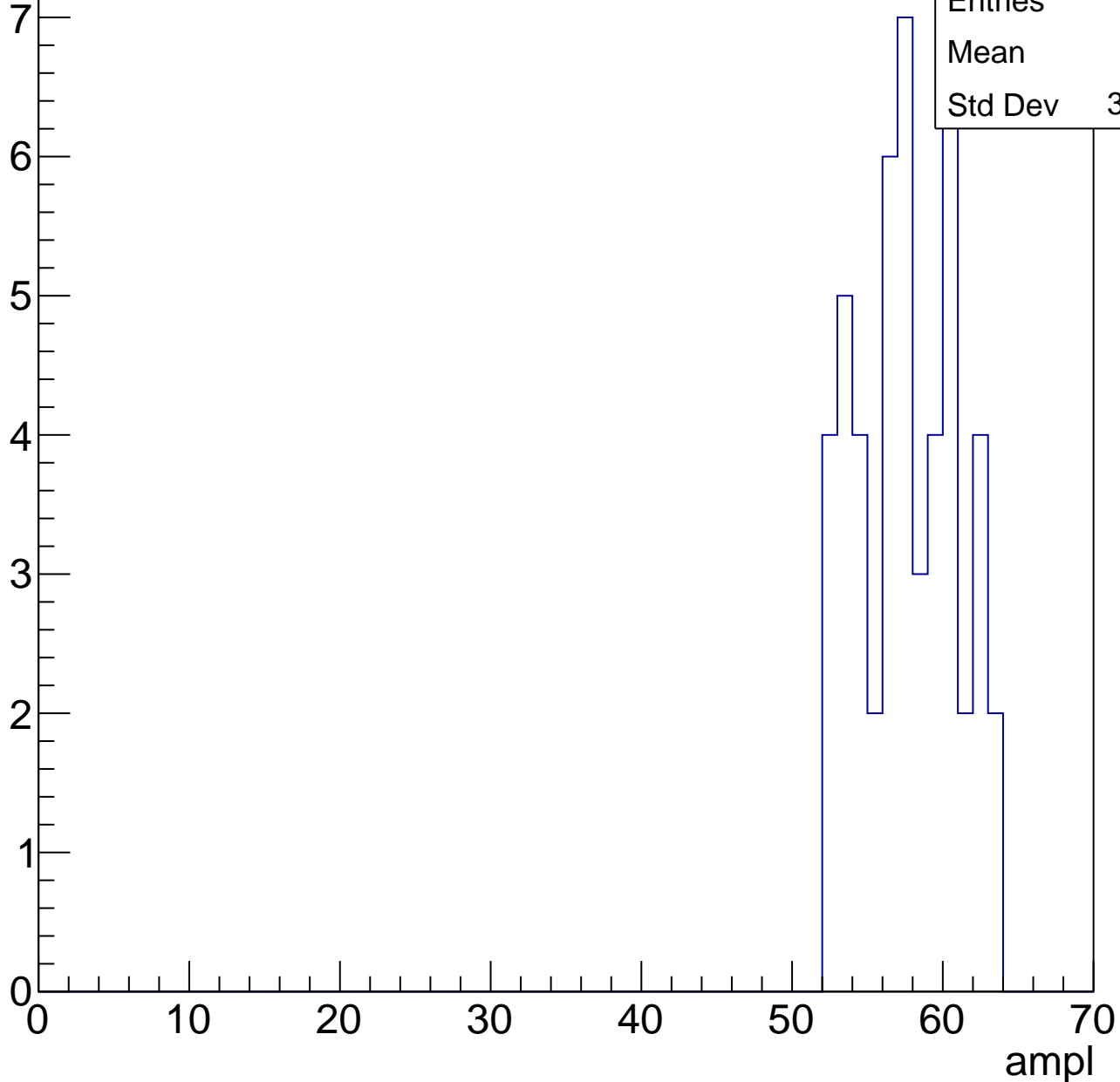
Entries	57
Mean	53.42
Std Dev	3.848



# B1L103S, U1-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

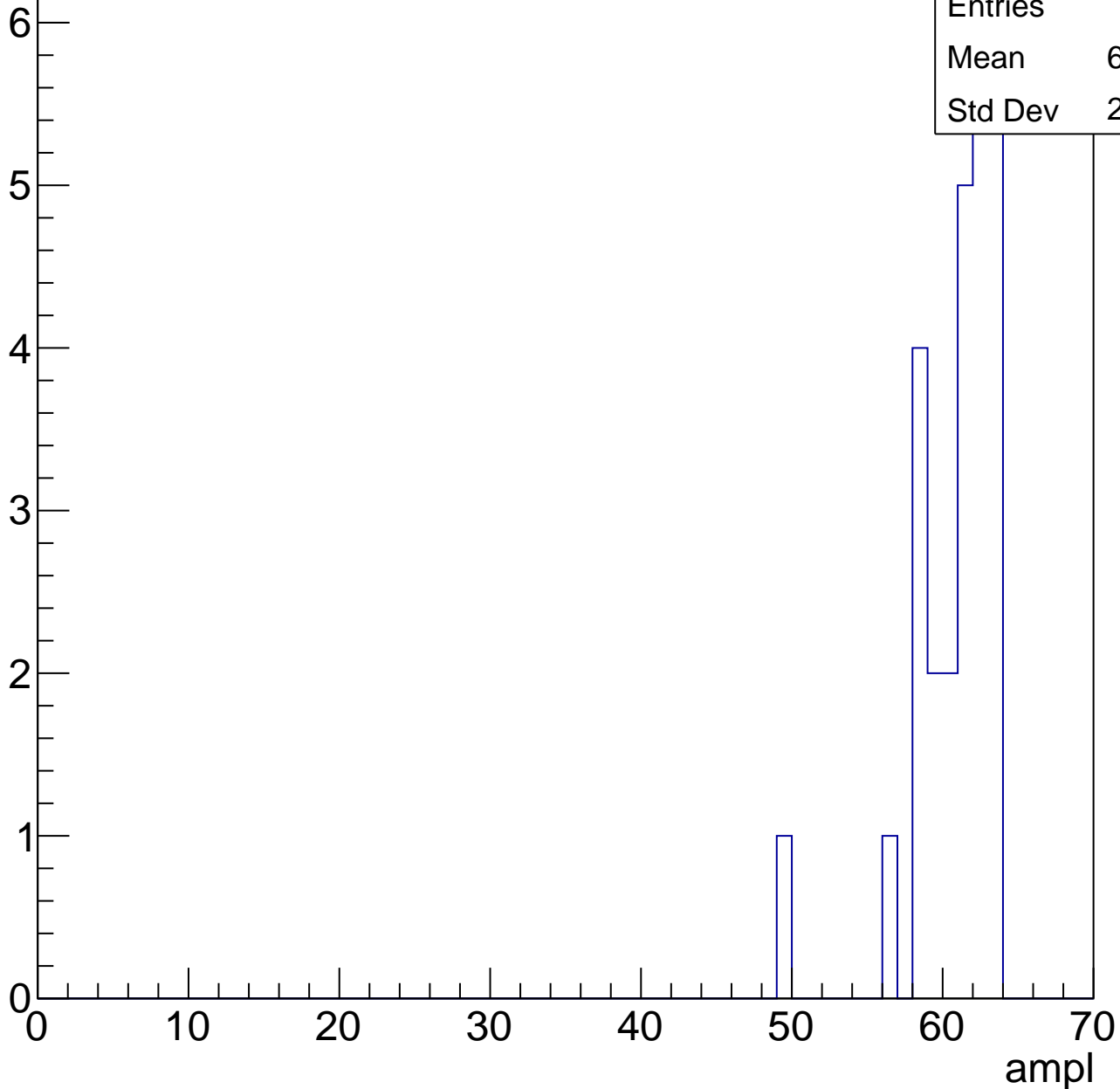


# B1L103S, U1-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	27
Mean	60.37
Std Dev	2.946

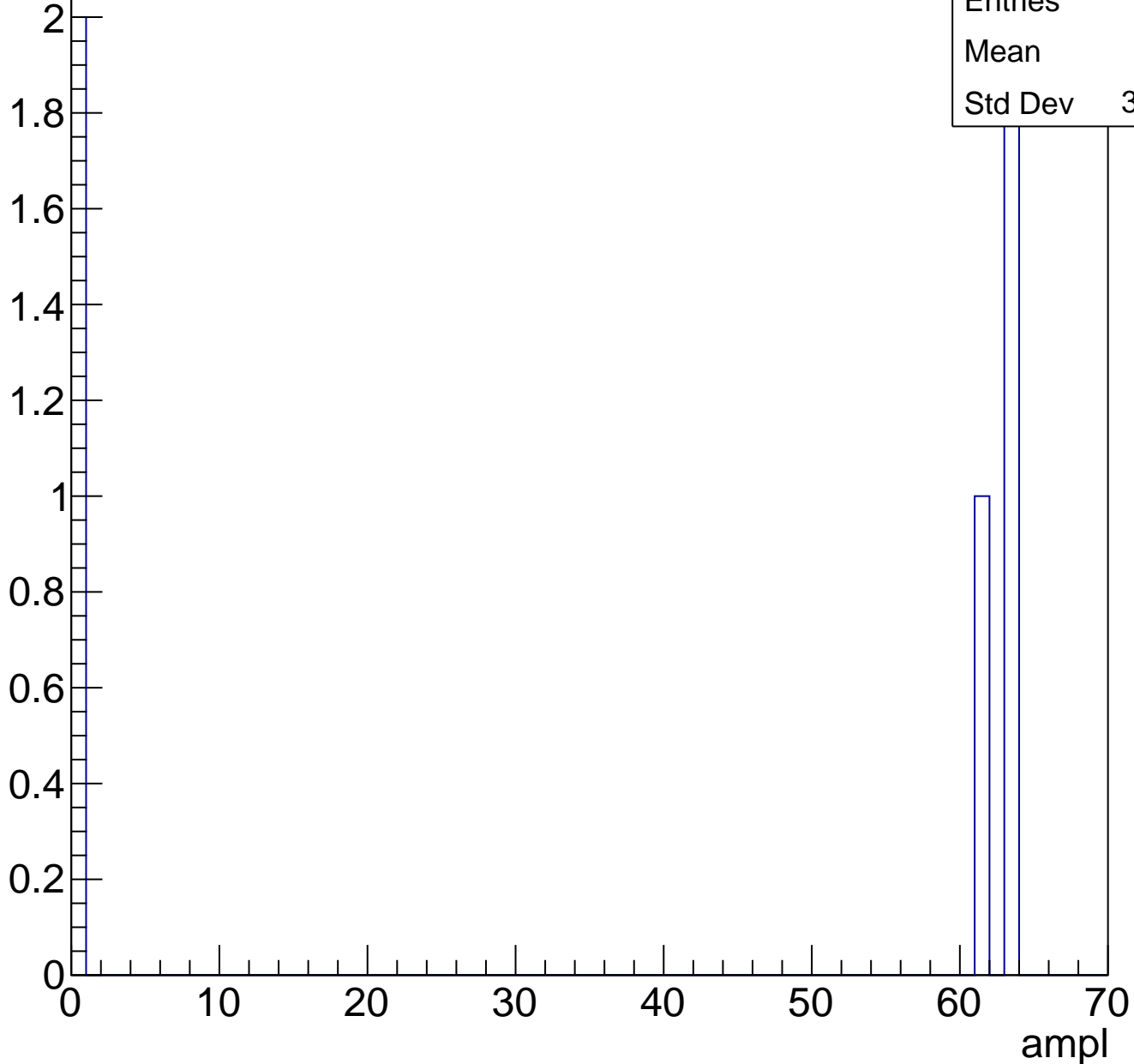




# B1L103S, U1-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U1-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

