



# B1L000S, U2-ch0

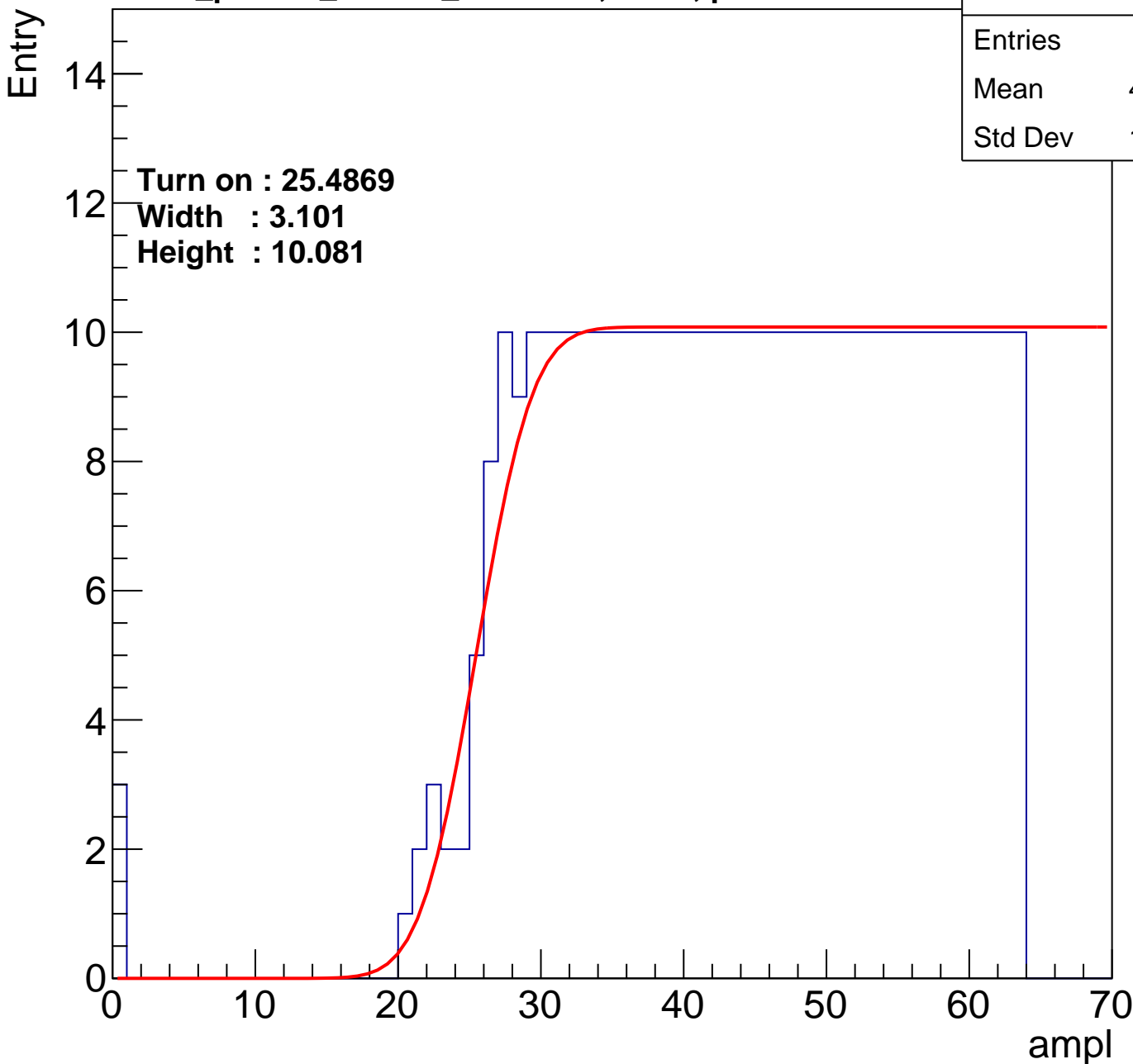
**calib\_packv5\_042523\_0143.root, FC#3, port B3**

Entries	395
Mean	43.49
Std Dev	12.03

**Turn on : 25.4869**

**Width : 3.101**

**Height : 10.081**



# B1L000S, U2-ch1

calib\_packv5\_042523\_0143.root, FC#3, port B3

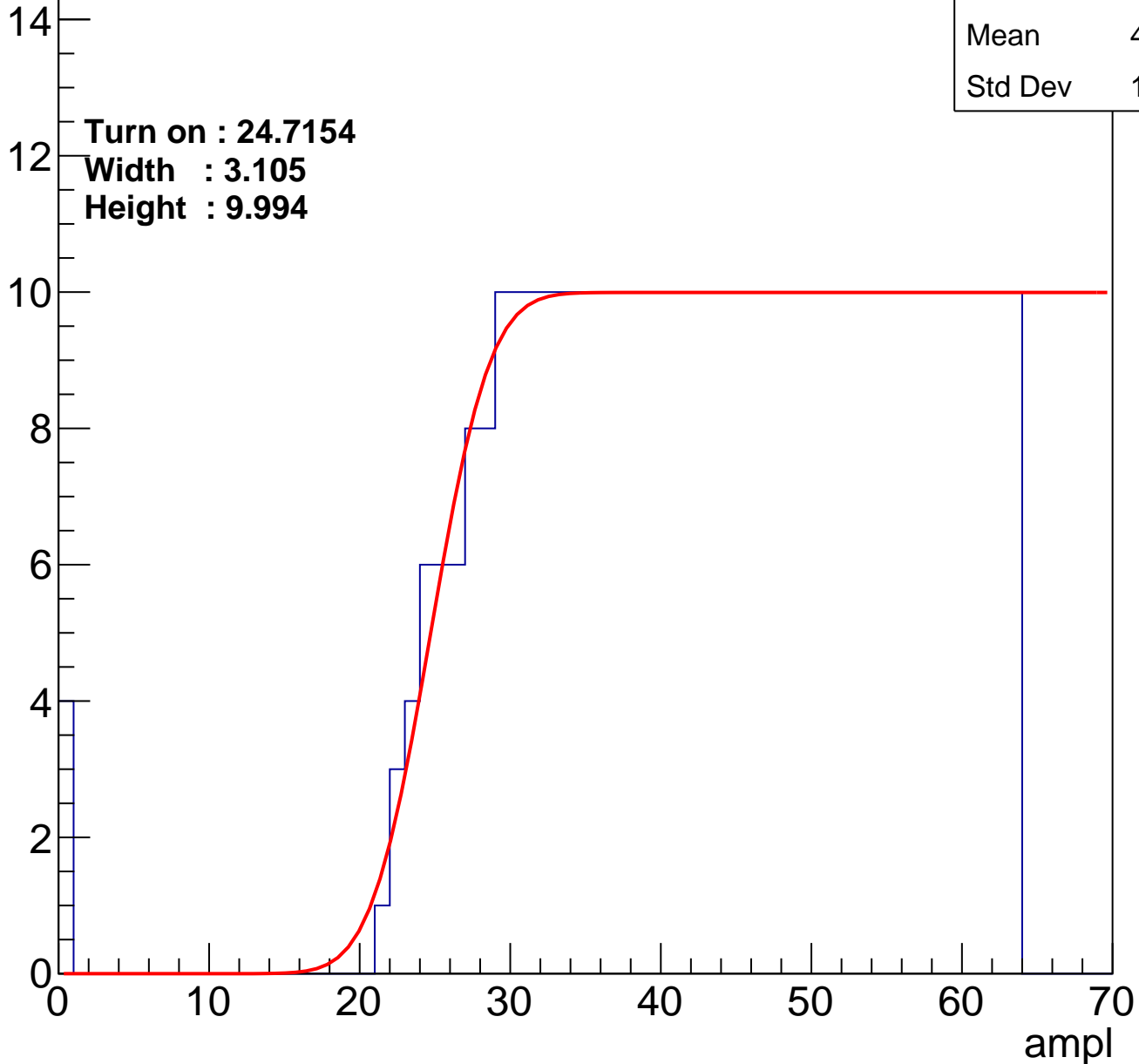
Entries	396
Mean	43.36
Std Dev	12.24

Turn on : 24.7154

Width : 3.105

Height : 9.994

Entry



# B1L000S, U2-ch2

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	394
Mean	43.62
Std Dev	11.73

Turn on : 24.6156

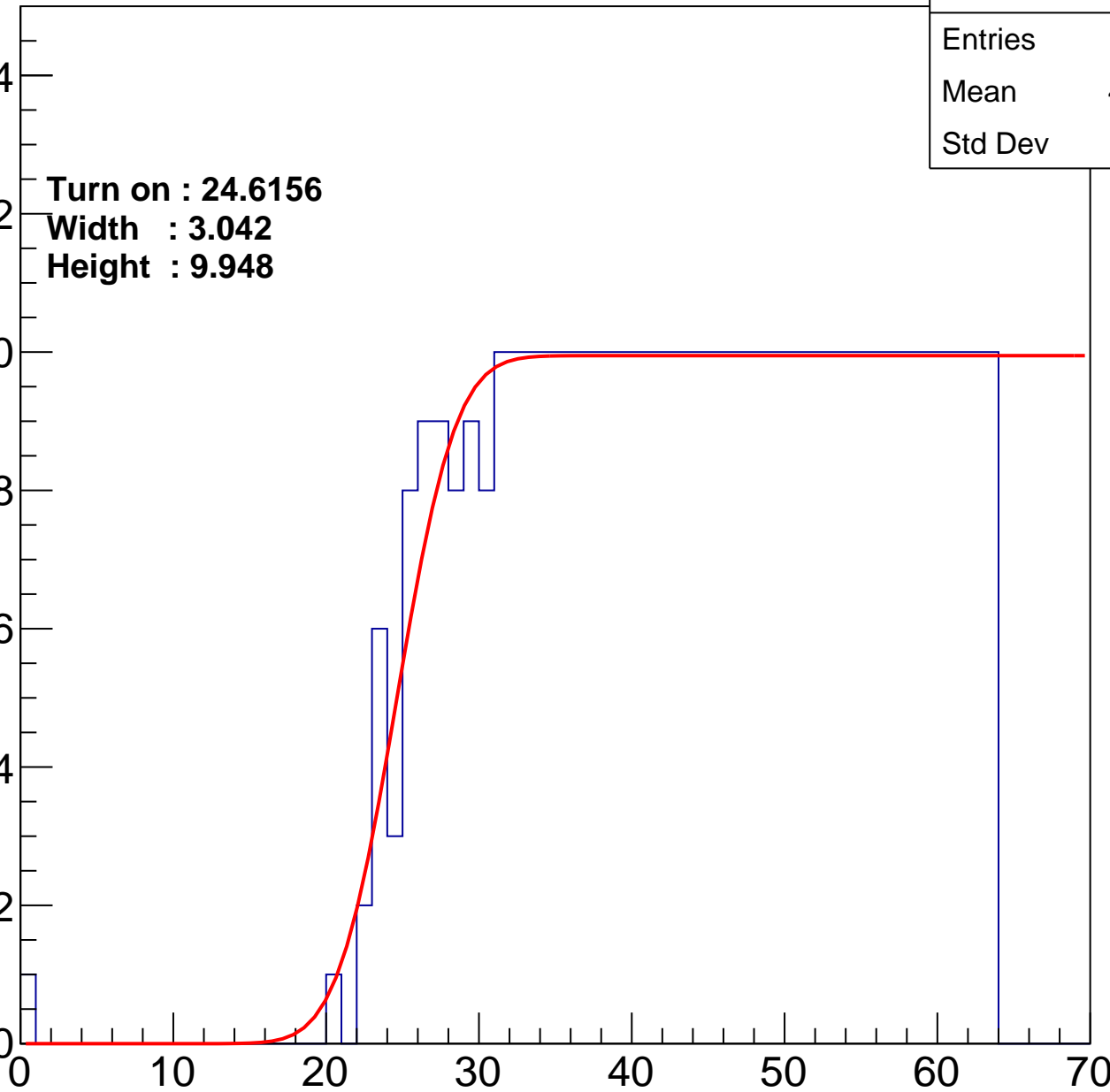
Width : 3.042

Height : 9.948

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch3

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	400
Mean	43.31
Std Dev	11.98

Turn on : 24.1266

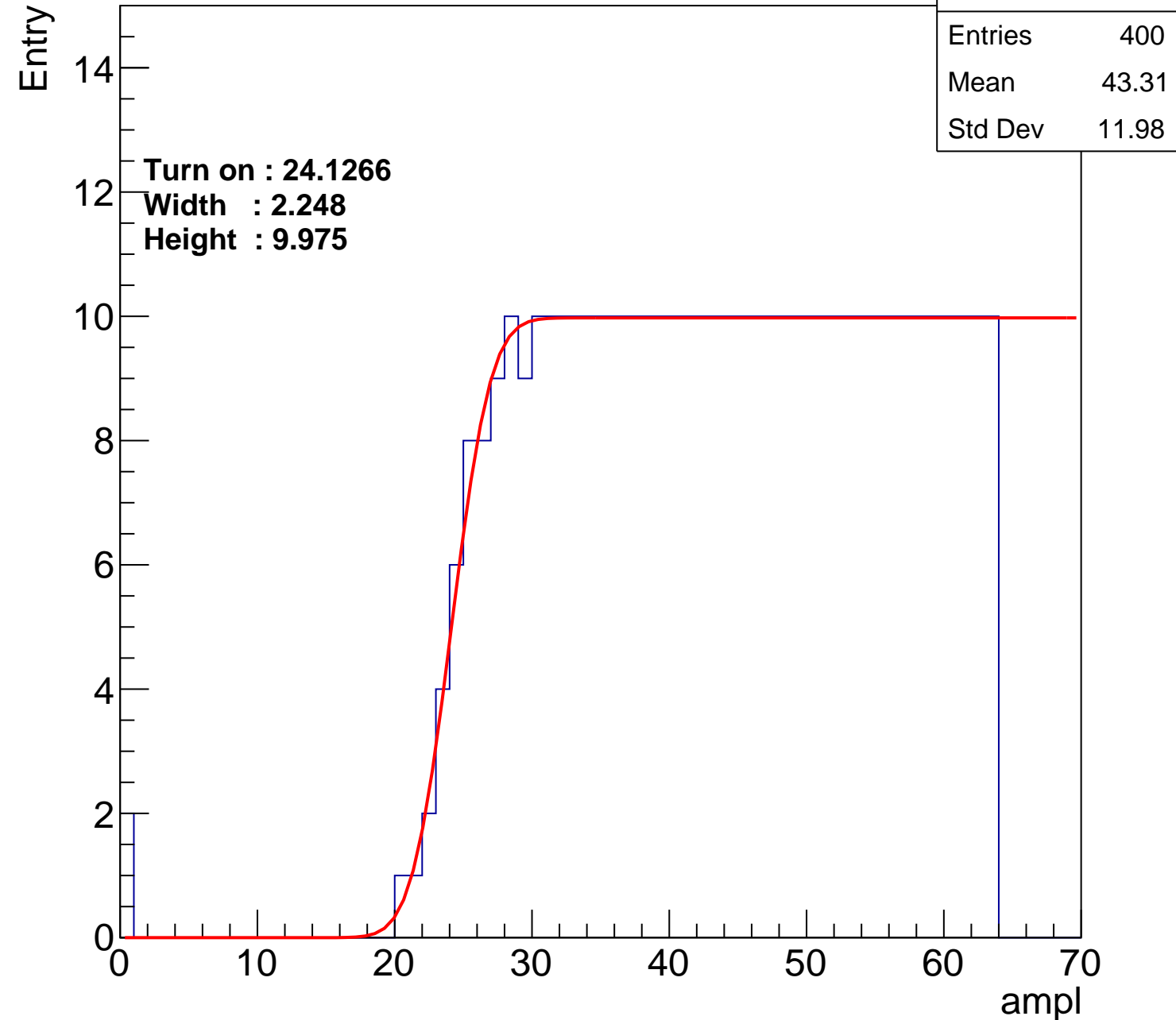
Width : 2.248

Height : 9.975

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch4

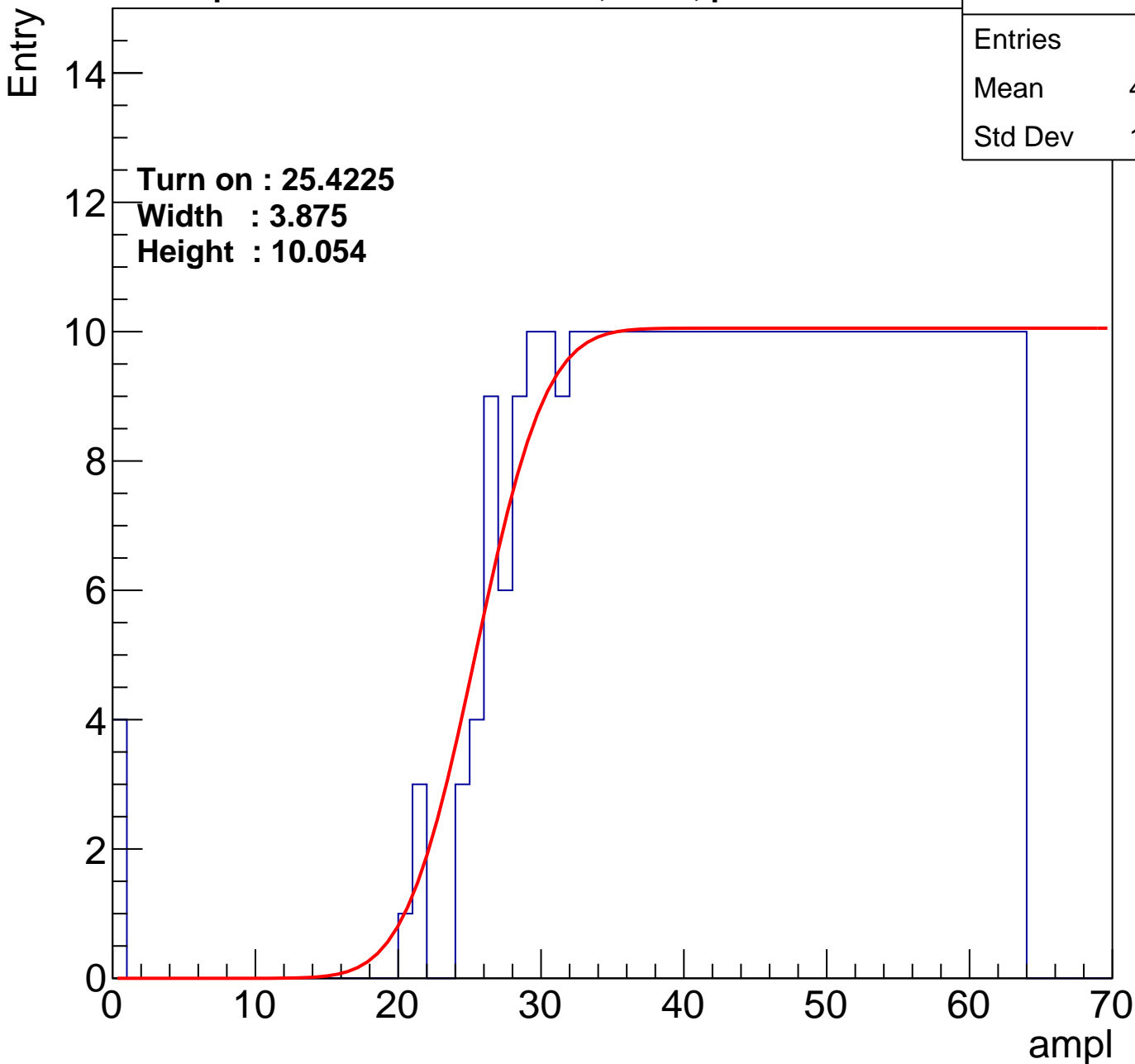
calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	388
Mean	43.74
Std Dev	12.06

Turn on : 25.4225

Width : 3.875

Height : 10.054



# B1L000S, U2-ch5

calib\_packv5\_042523\_0143.root, FC#3, port B3

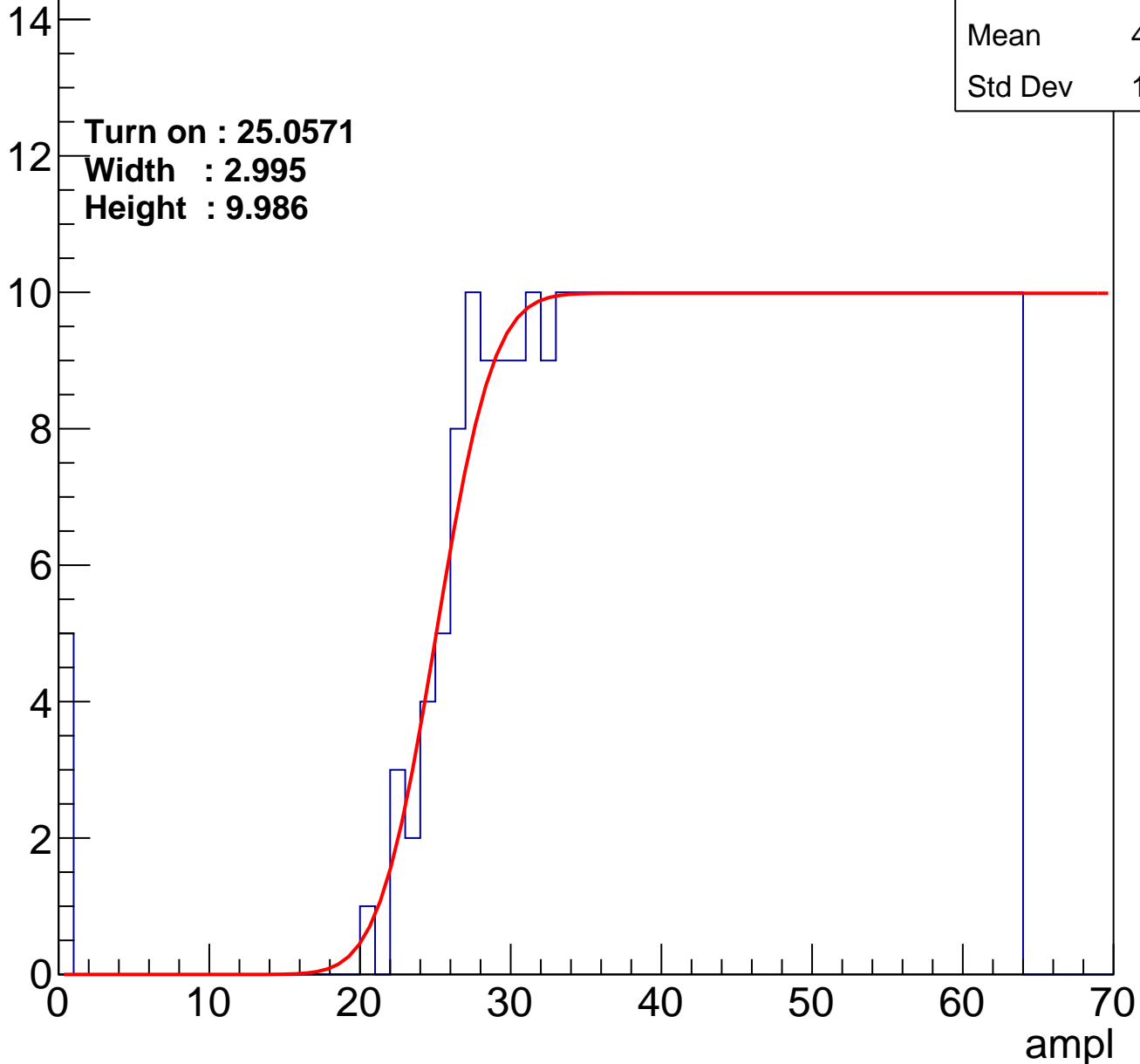
Entries	394
Mean	43.38
Std Dev	12.36

Turn on : 25.0571

Width : 2.995

Height : 9.986

Entry



# B1L000S, U2-ch6

calib\_packv5\_042523\_0143.root, FC#3, port B3

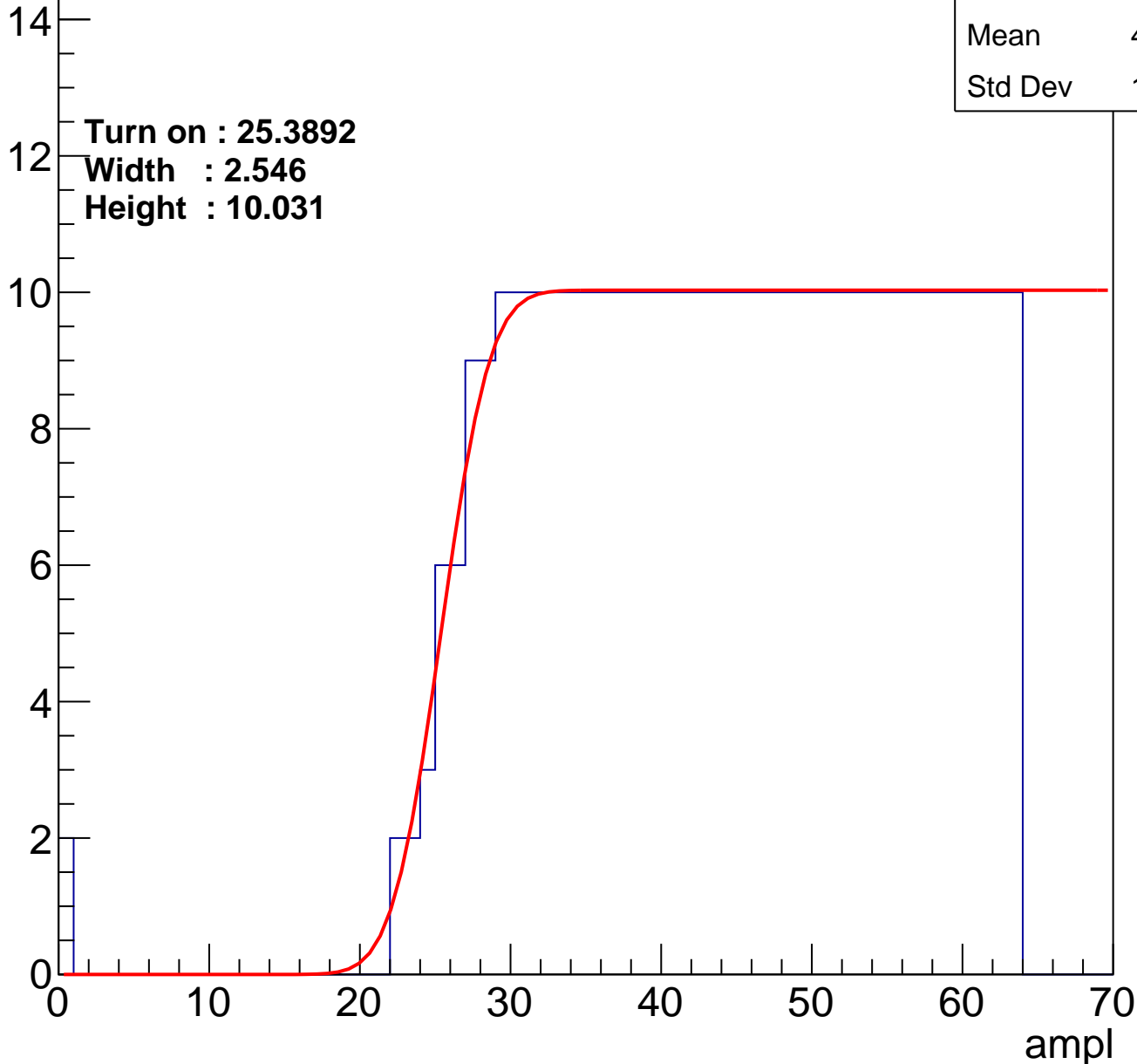
Entry

Entries	389
Mean	43.86
Std Dev	11.68

Turn on : 25.3892

Width : 2.546

Height : 10.031





# B1L000S, U2-ch7

calib\_packv5\_042523\_0143.root, FC#3, port B3

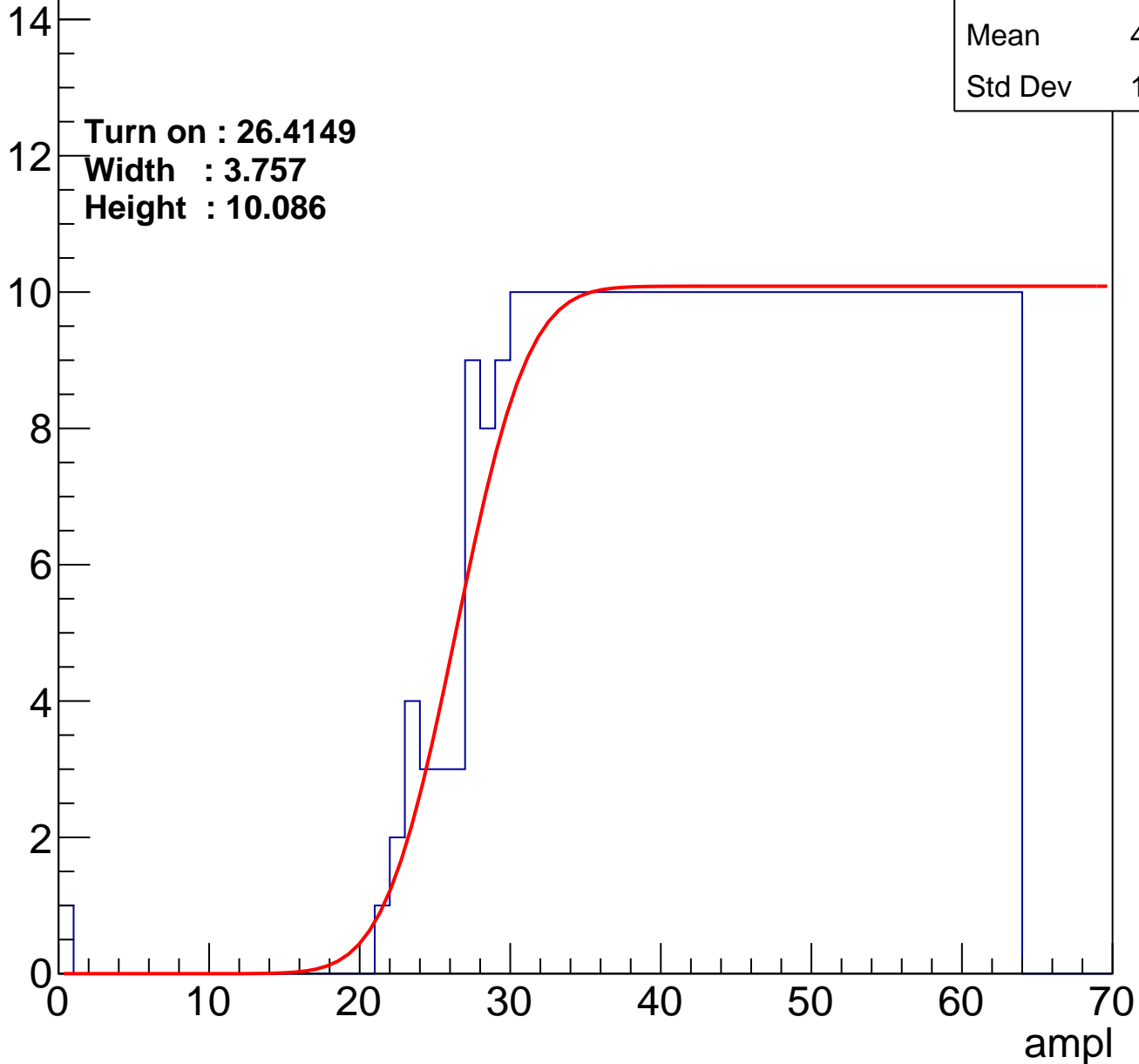
Entries	383
Mean	44.18
Std Dev	11.42

Turn on : 26.4149

Width : 3.757

Height : 10.086

Entry



# B1L000S, U2-ch8

calib\_packv5\_042523\_0143.root, FC#3, port B3

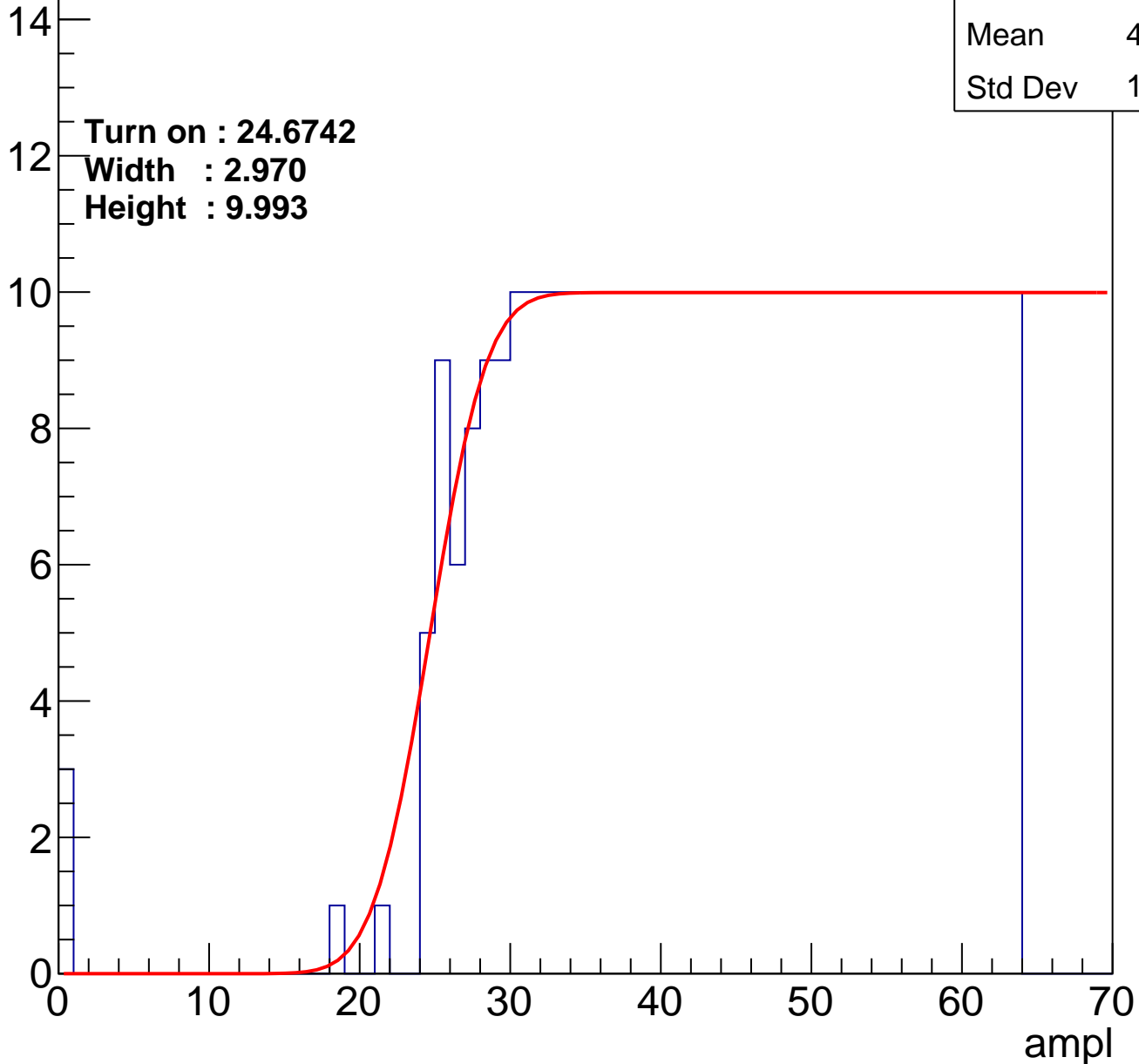
Entries	391
Mean	43.68
Std Dev	11.93

Turn on : 24.6742

Width : 2.970

Height : 9.993

Entry



# B1L000S, U2-ch9

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	397
Mean	43.38
Std Dev	12.08

Turn on : 24.8103

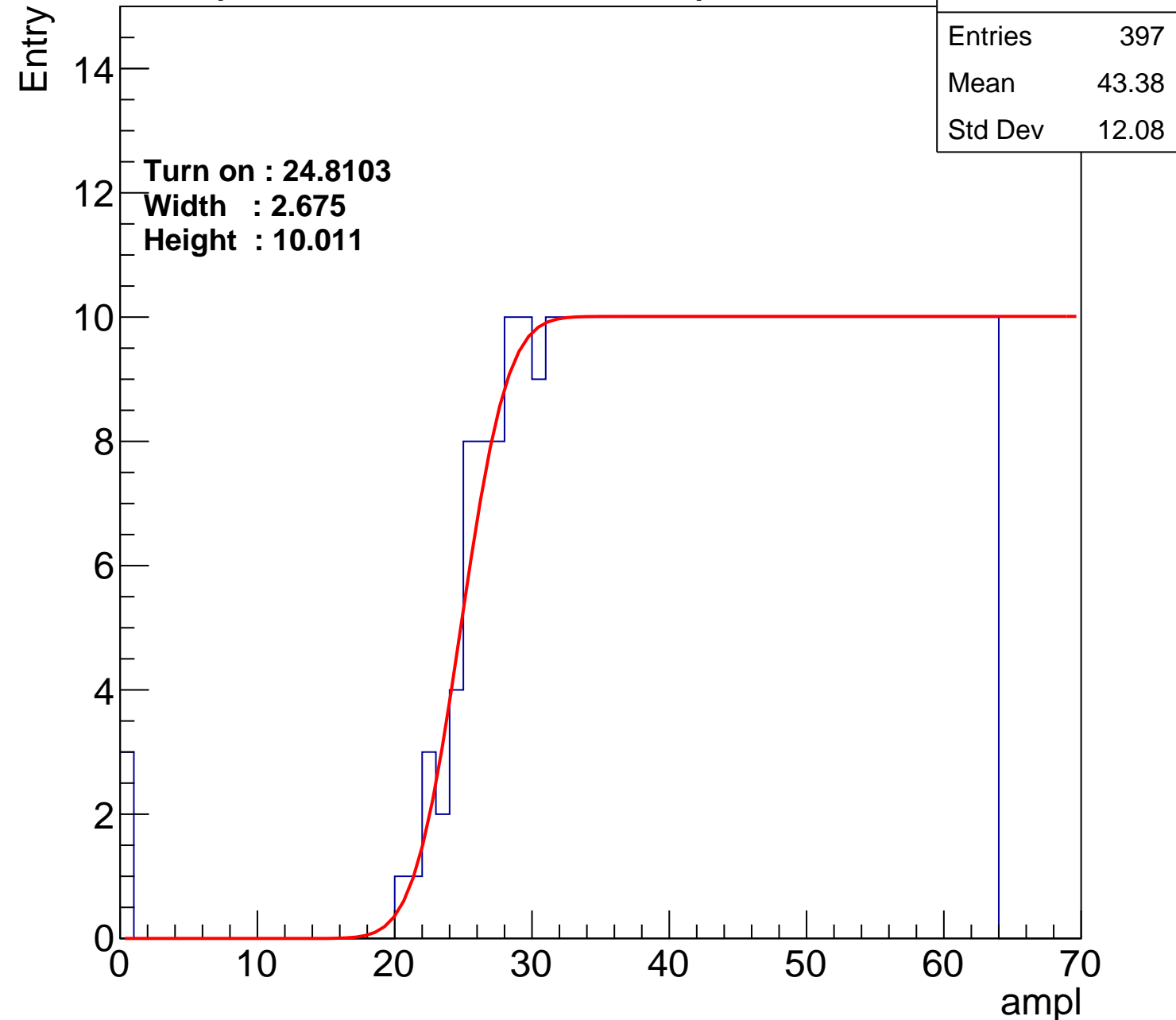
Width : 2.675

Height : 10.011

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch10

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	396
Mean	43.41
Std Dev	12.09

**Turn on : 24.9822**

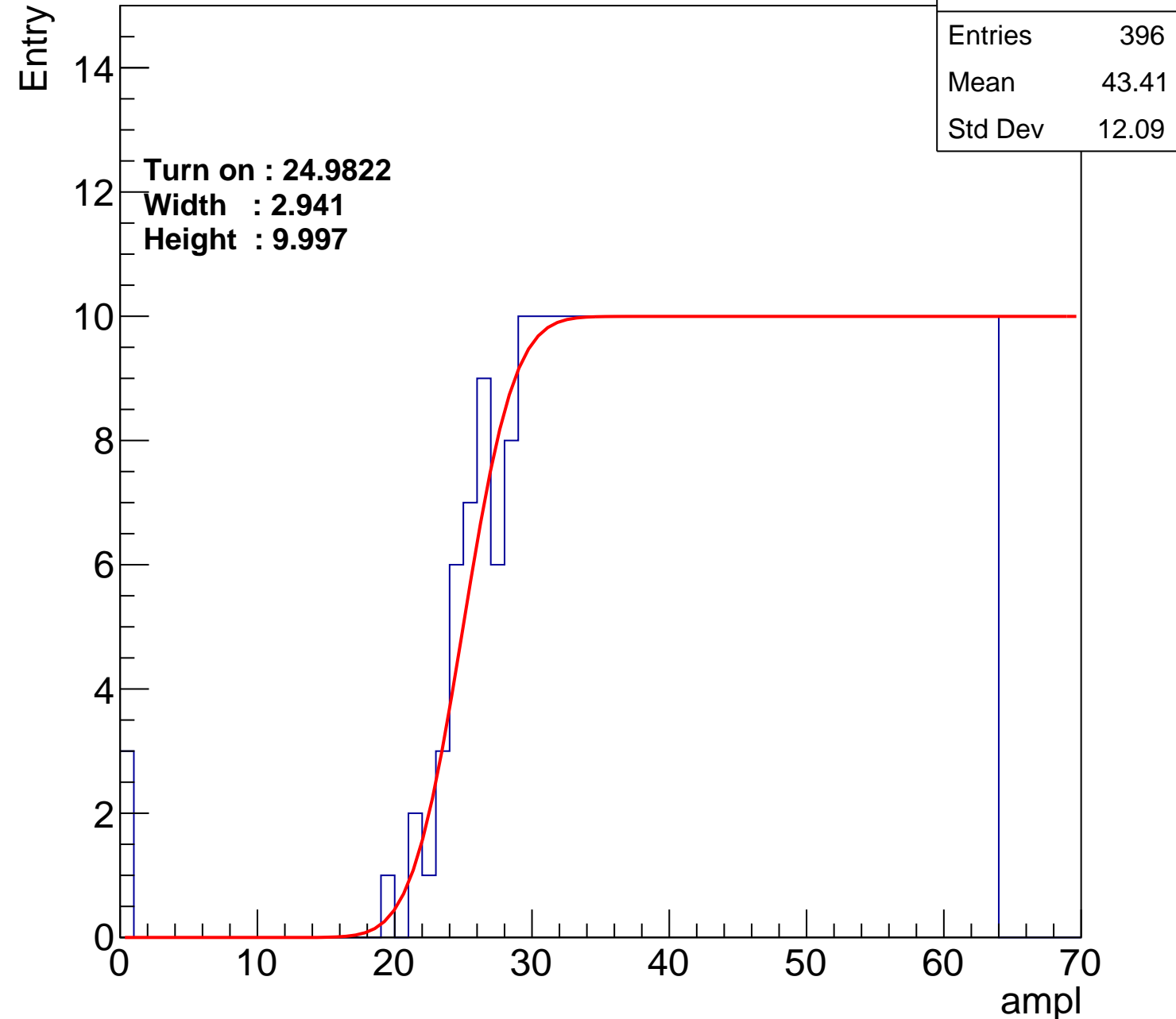
**Width : 2.941**

**Height : 9.997**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch11

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	372
Mean	44.54
Std Dev	11.66

Turn on : 27.4726

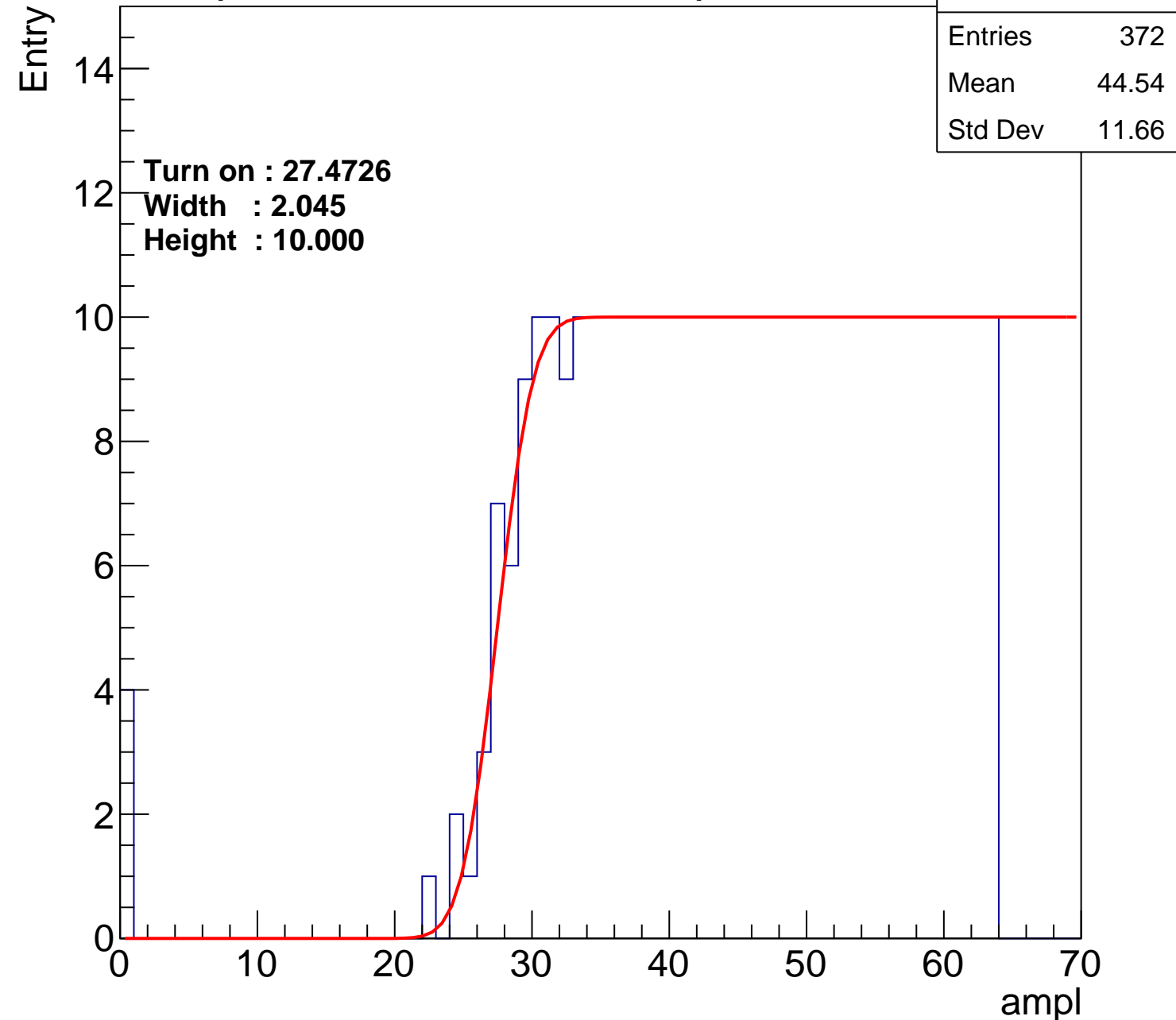
Width : 2.045

Height : 10.000

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch12

calib\_packv5\_042523\_0143.root, FC#3, port B3

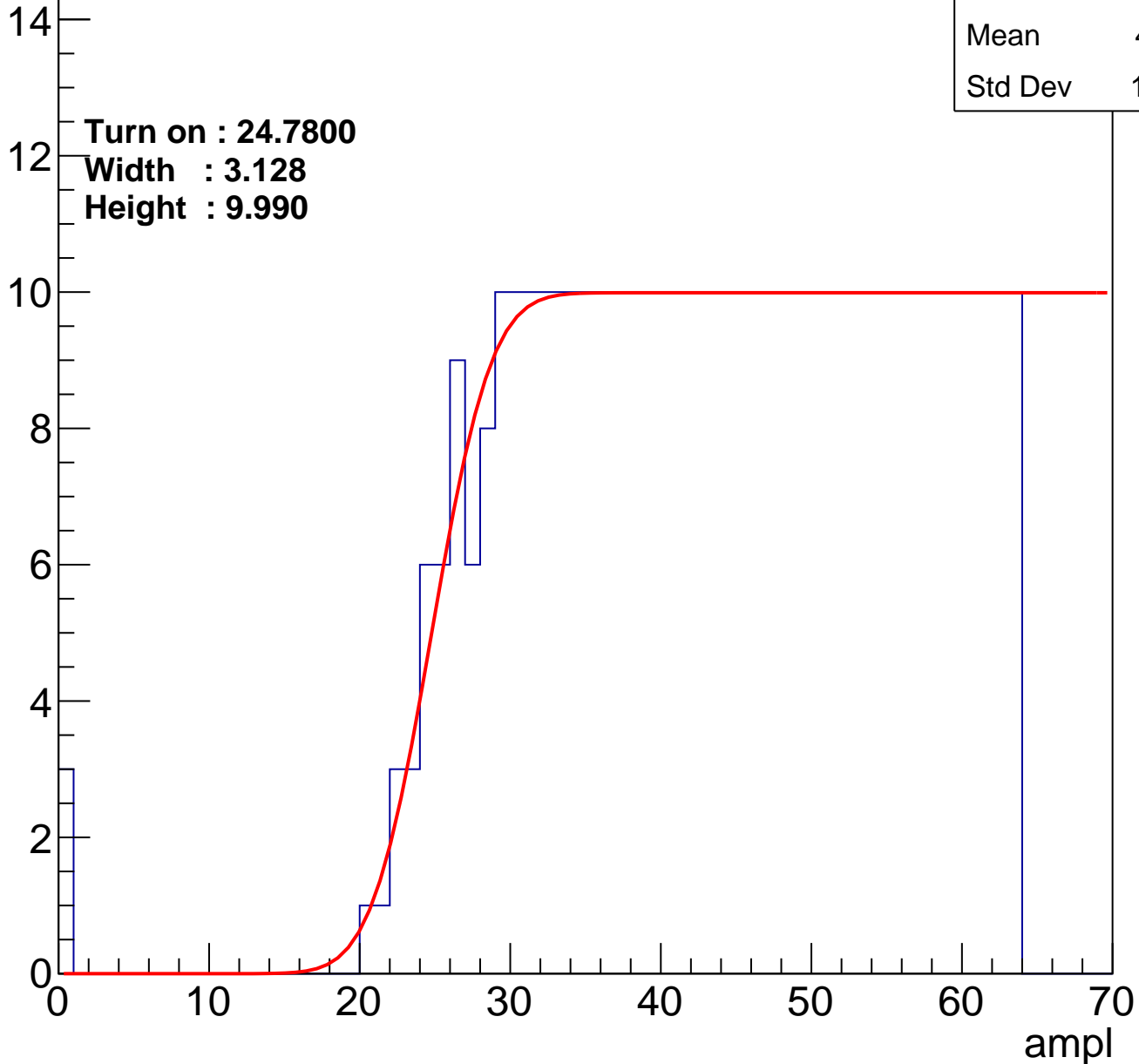
Entries	396
Mean	43.41
Std Dev	12.09

**Turn on : 24.7800**

**Width : 3.128**

**Height : 9.990**

Entry



# B1L000S, U2-ch13

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	378
Mean	44.42
Std Dev	11.38

**Turn on : 25.4814**

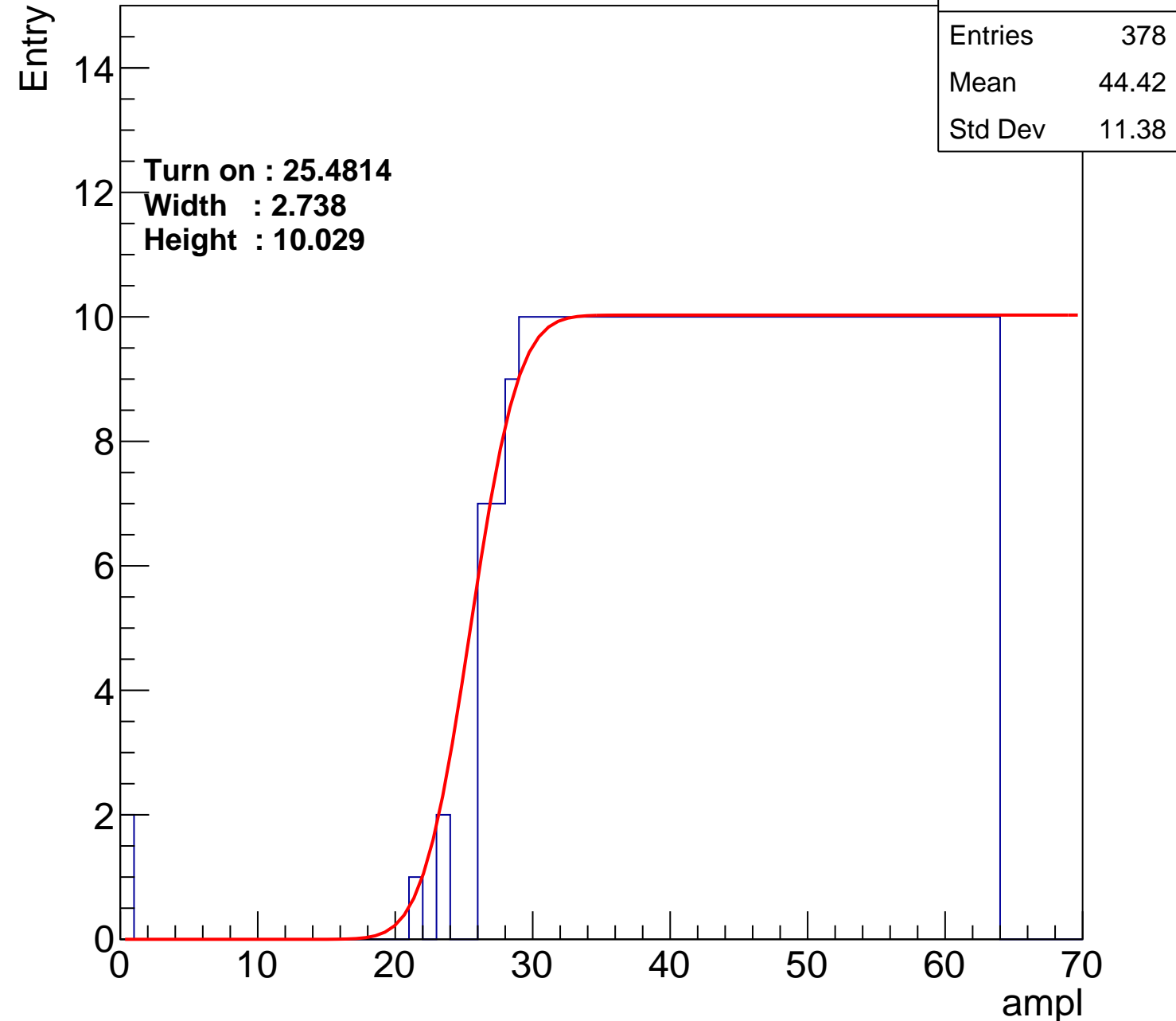
**Width : 2.738**

**Height : 10.029**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch14

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	380
Mean	44.37
Std Dev	11.26

Turn on : 26.4634

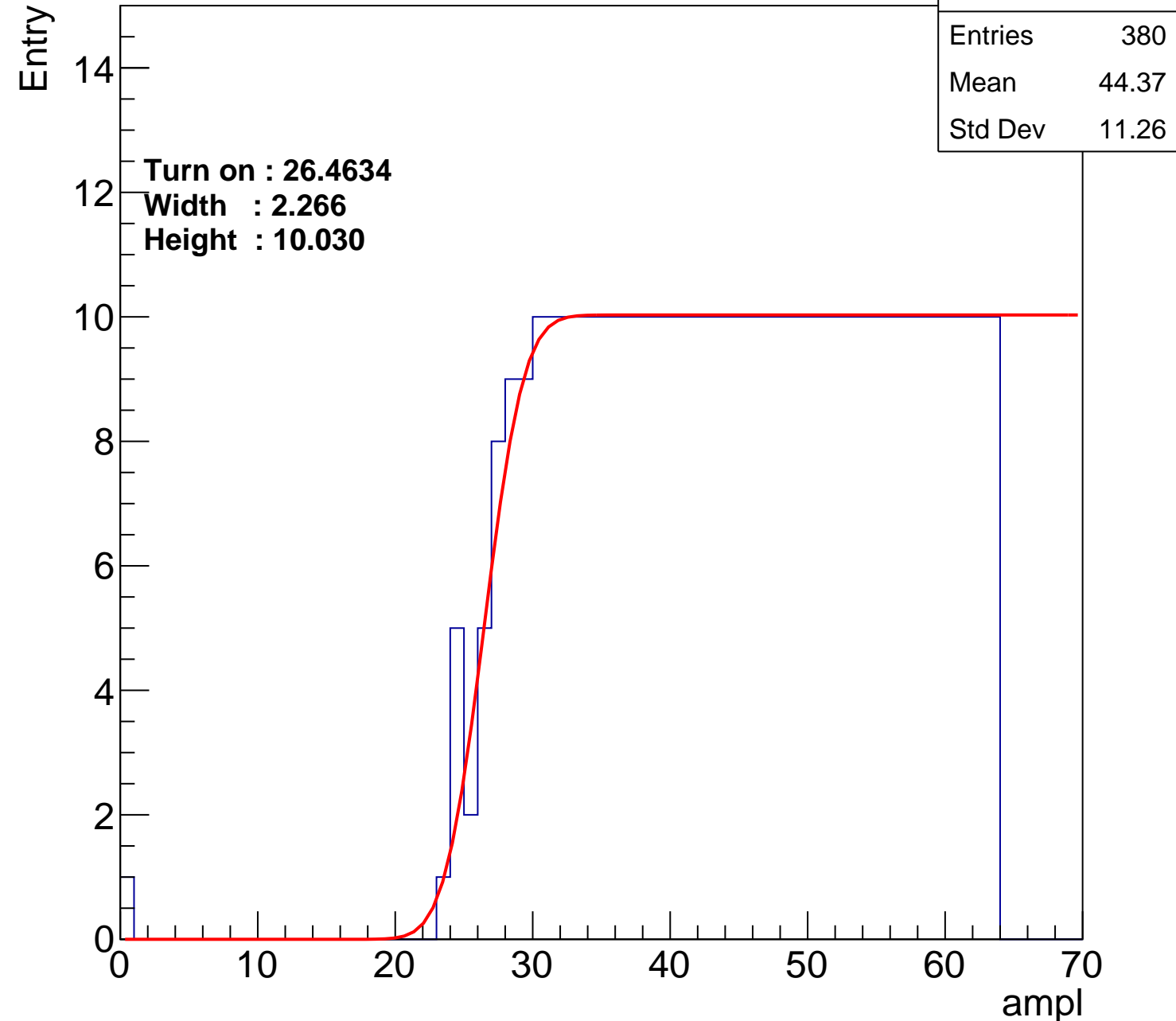
Width : 2.266

Height : 10.030

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L000S, U2-ch15

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	385
Mean	44.11
Std Dev	11.42

**Turn on : 25.8165**

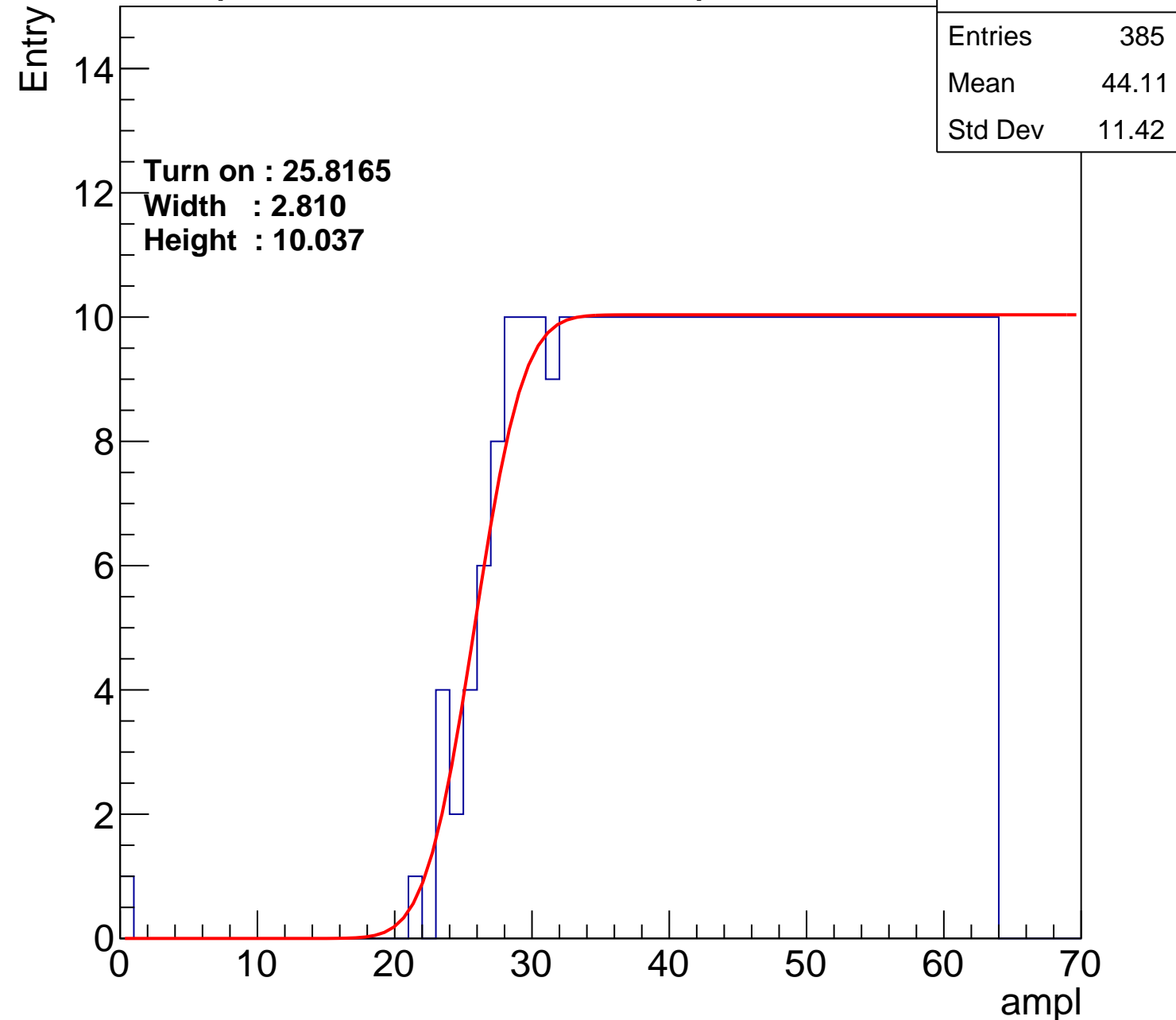
**Width : 2.810**

**Height : 10.037**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch16

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	406
Mean	42.96
Std Dev	12.23

**Turn on : 23.6899**

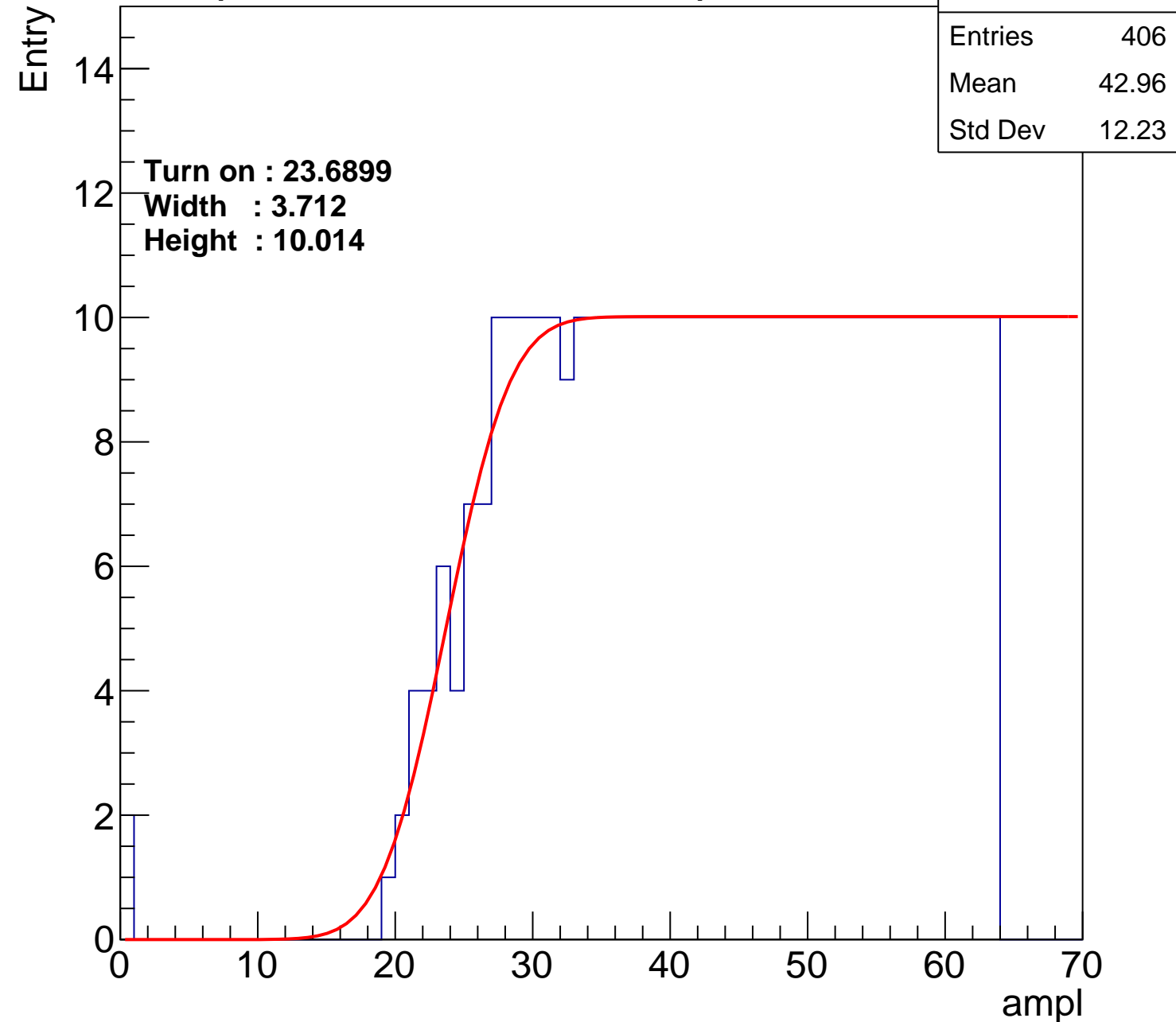
**Width : 3.712**

**Height : 10.014**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch17

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	380
Mean	44.16
Std Dev	11.82

**Turn on : 26.6043**

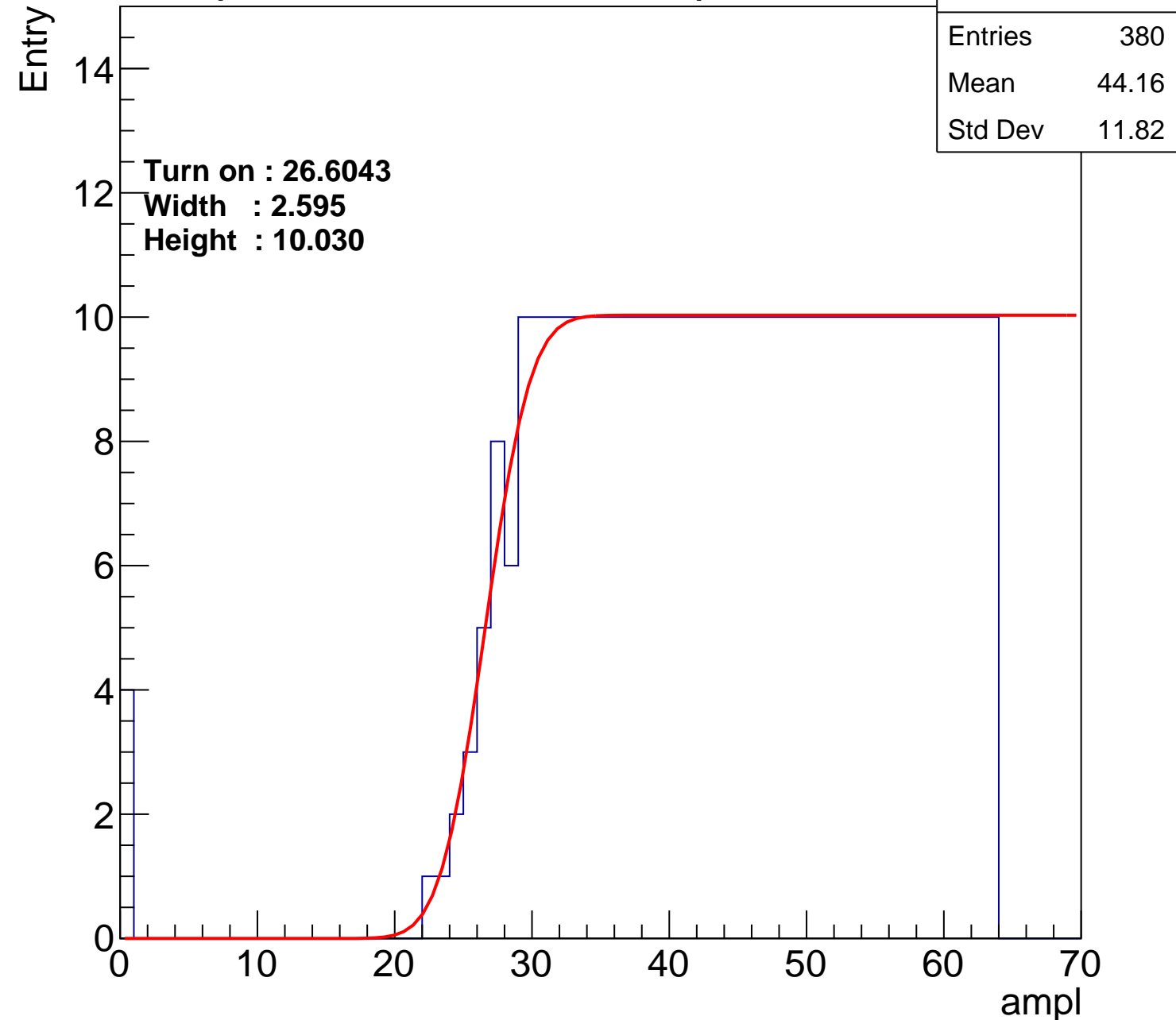
**Width : 2.595**

**Height : 10.030**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch18

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	390
Mean	43.86
Std Dev	11.56

**Turn on : 25.5852**

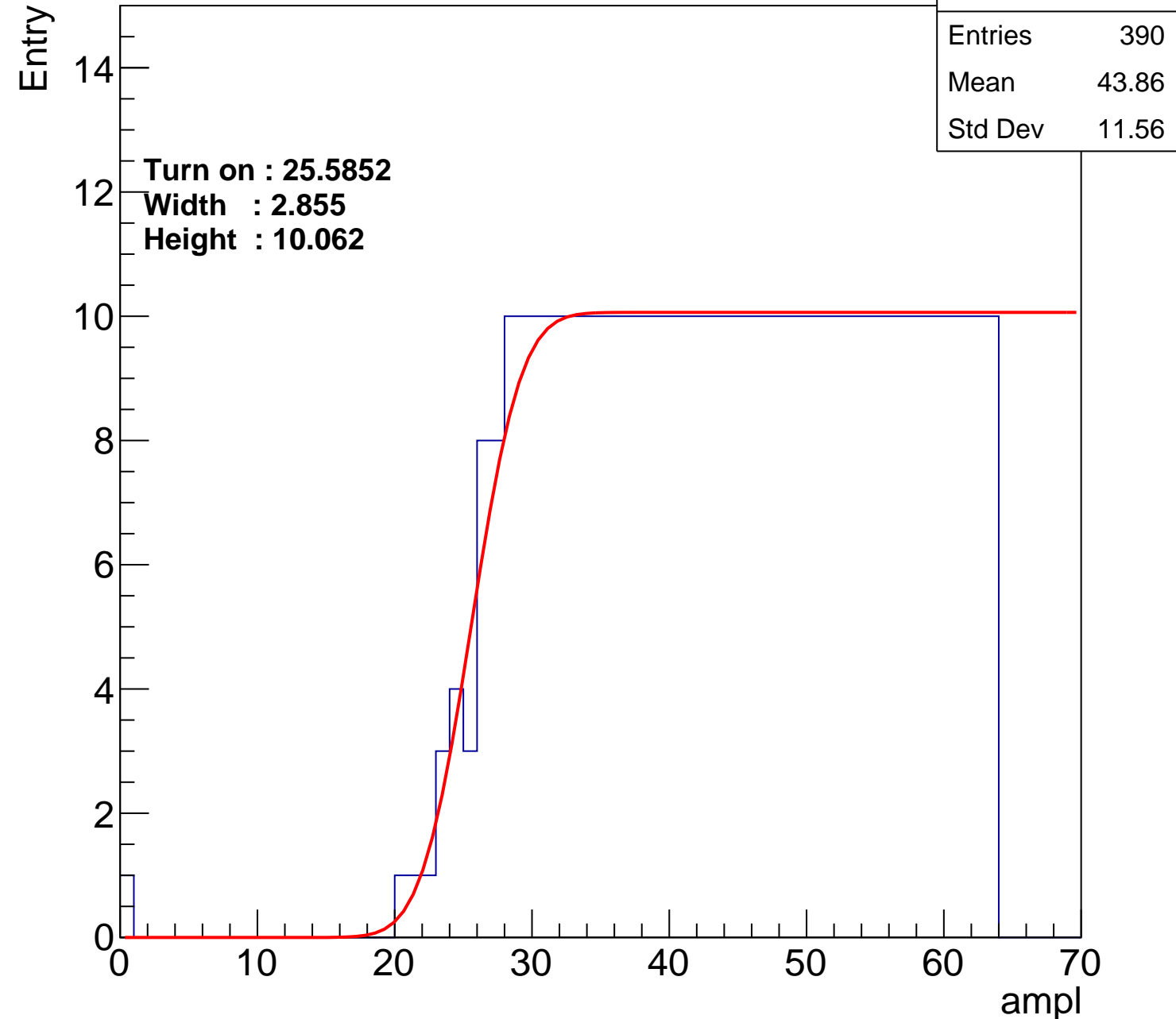
**Width : 2.855**

**Height : 10.062**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch19

calib\_packv5\_042523\_0143.root, FC#3, port B3

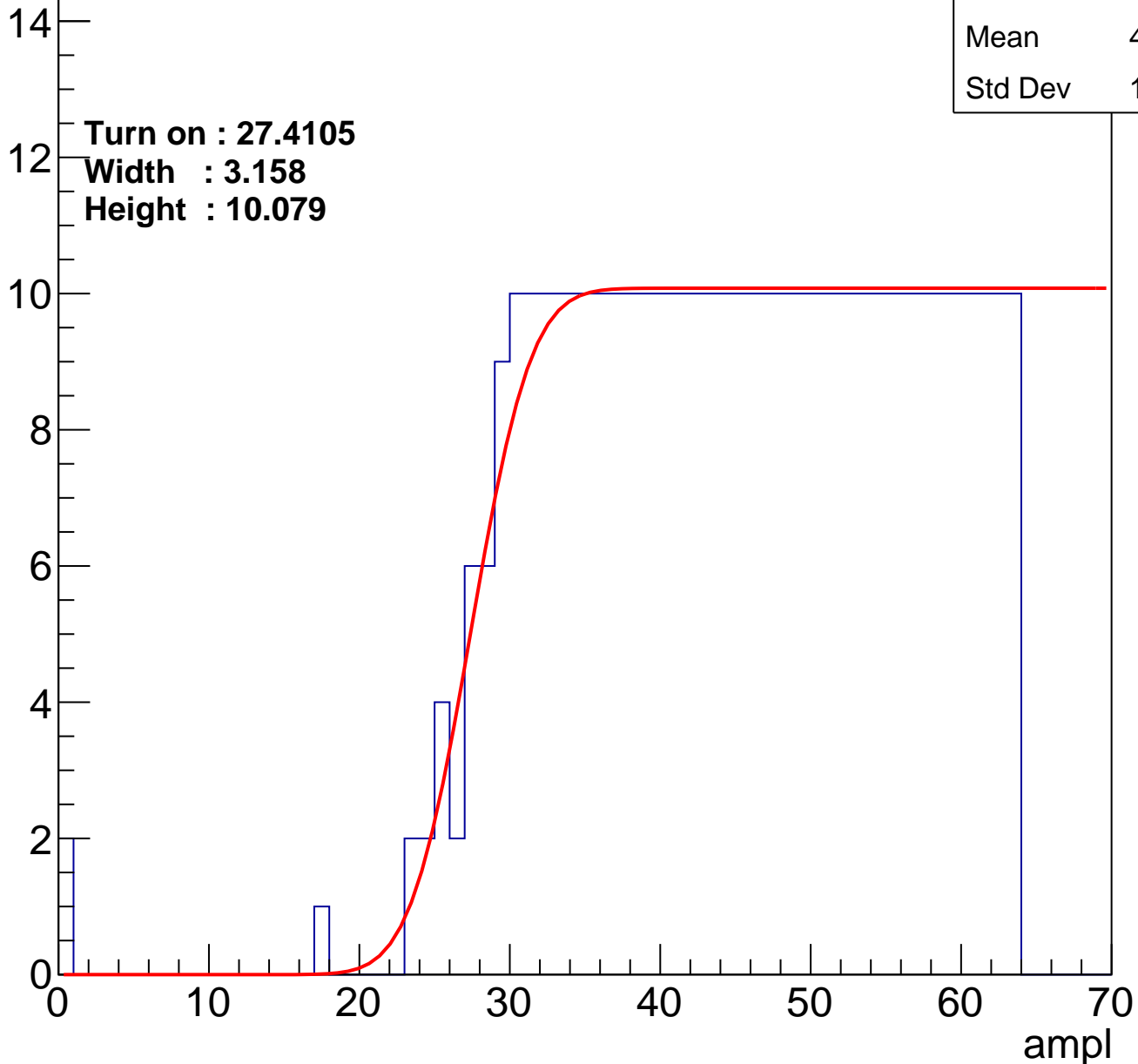
Entries	374
Mean	44.56
Std Dev	11.38

**Turn on : 27.4105**

**Width : 3.158**

**Height : 10.079**

Entry



# B1L000S, U2-ch20

calib\_packv5\_042523\_0143.root, FC#3, port B3

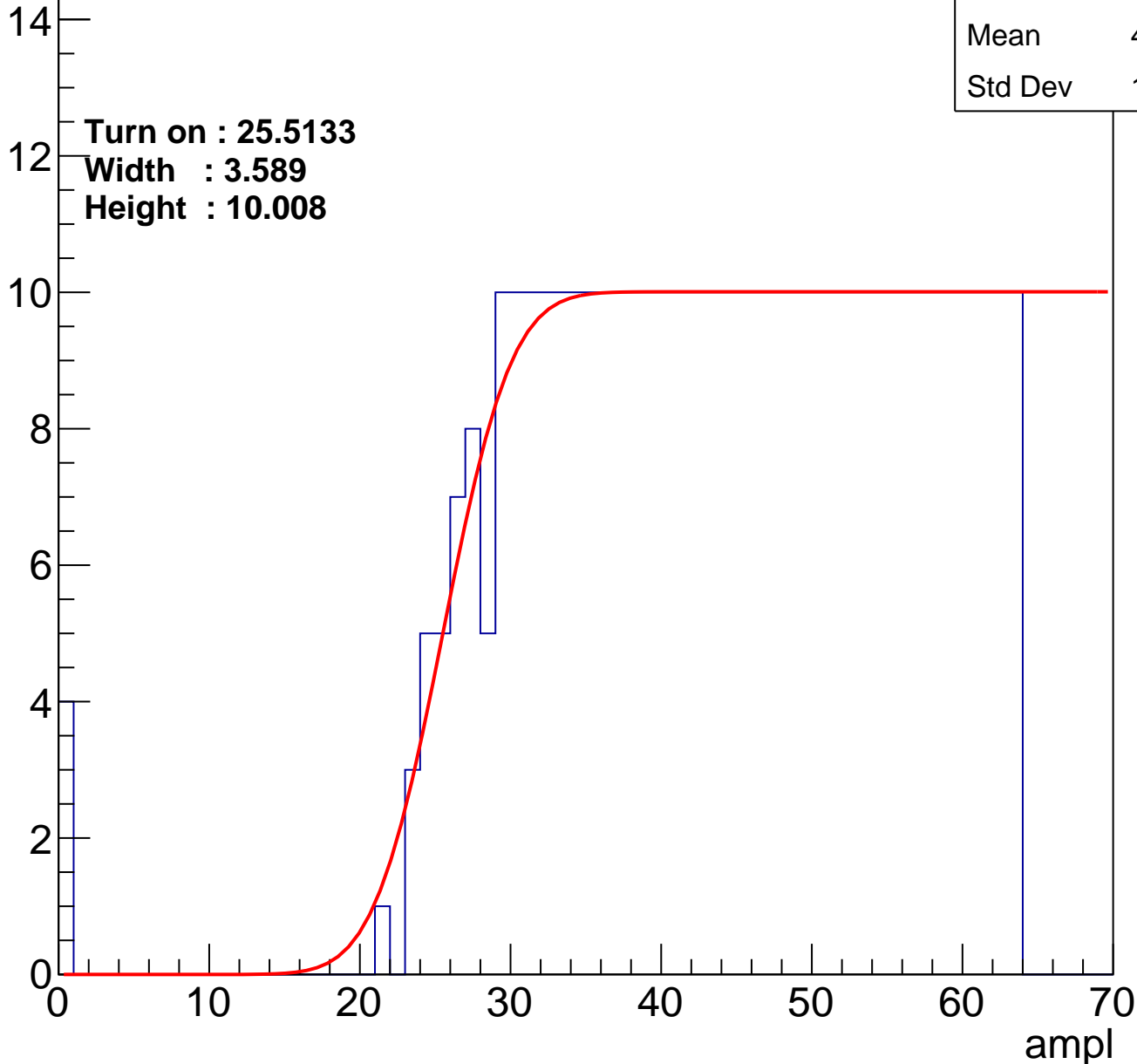
Entries	388
Mean	43.74
Std Dev	12.05

Turn on : 25.5133

Width : 3.589

Height : 10.008

Entry



# B1L000S, U2-ch21

calib\_packv5\_042523\_0143.root, FC#3, port B3

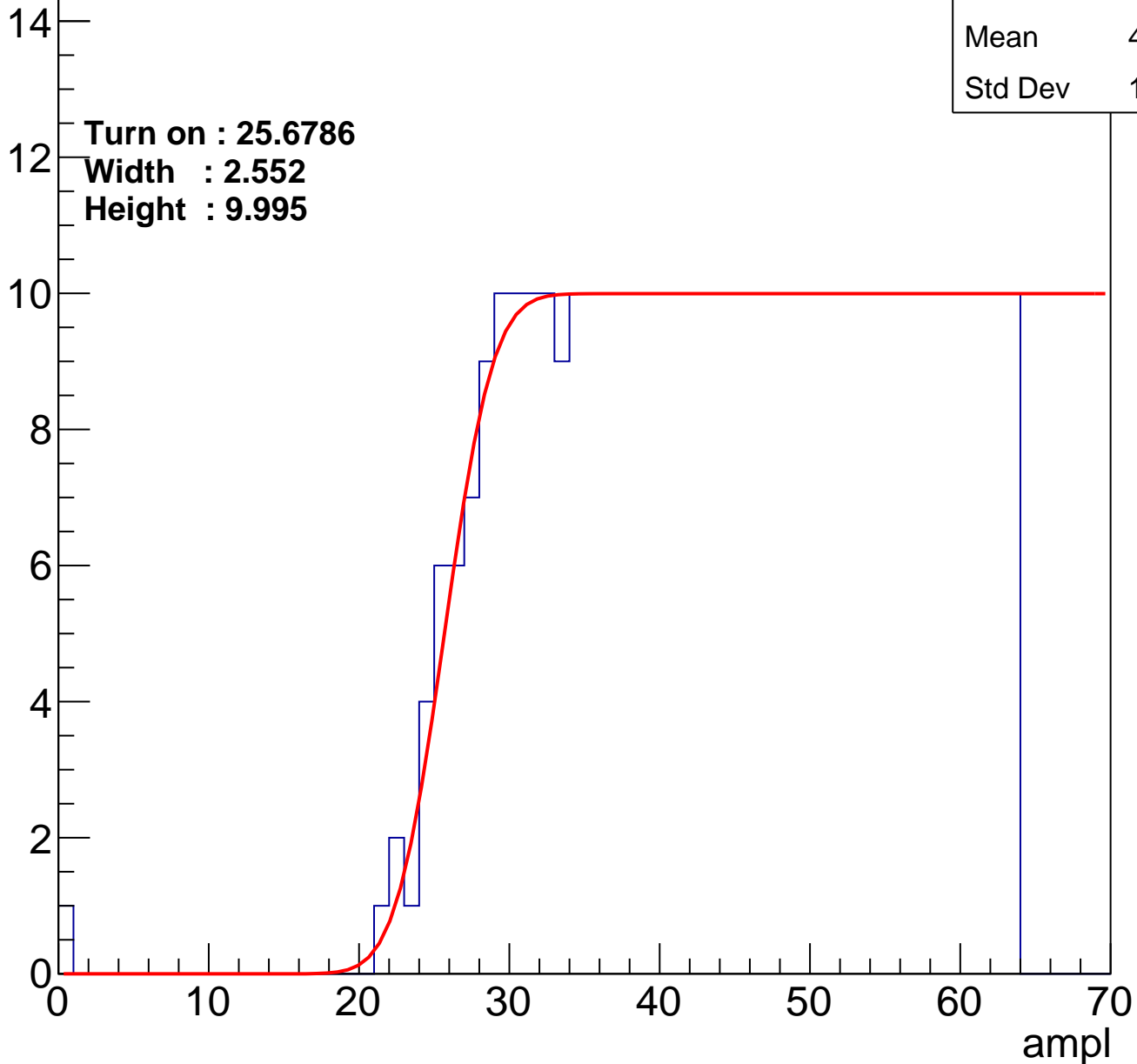
Entries	386
Mean	44.04
Std Dev	11.48

Turn on : 25.6786

Width : 2.552

Height : 9.995

Entry



# B1L000S, U2-ch22

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	394
Mean	43.52
Std Dev	12.02

Turn on : 25.3134

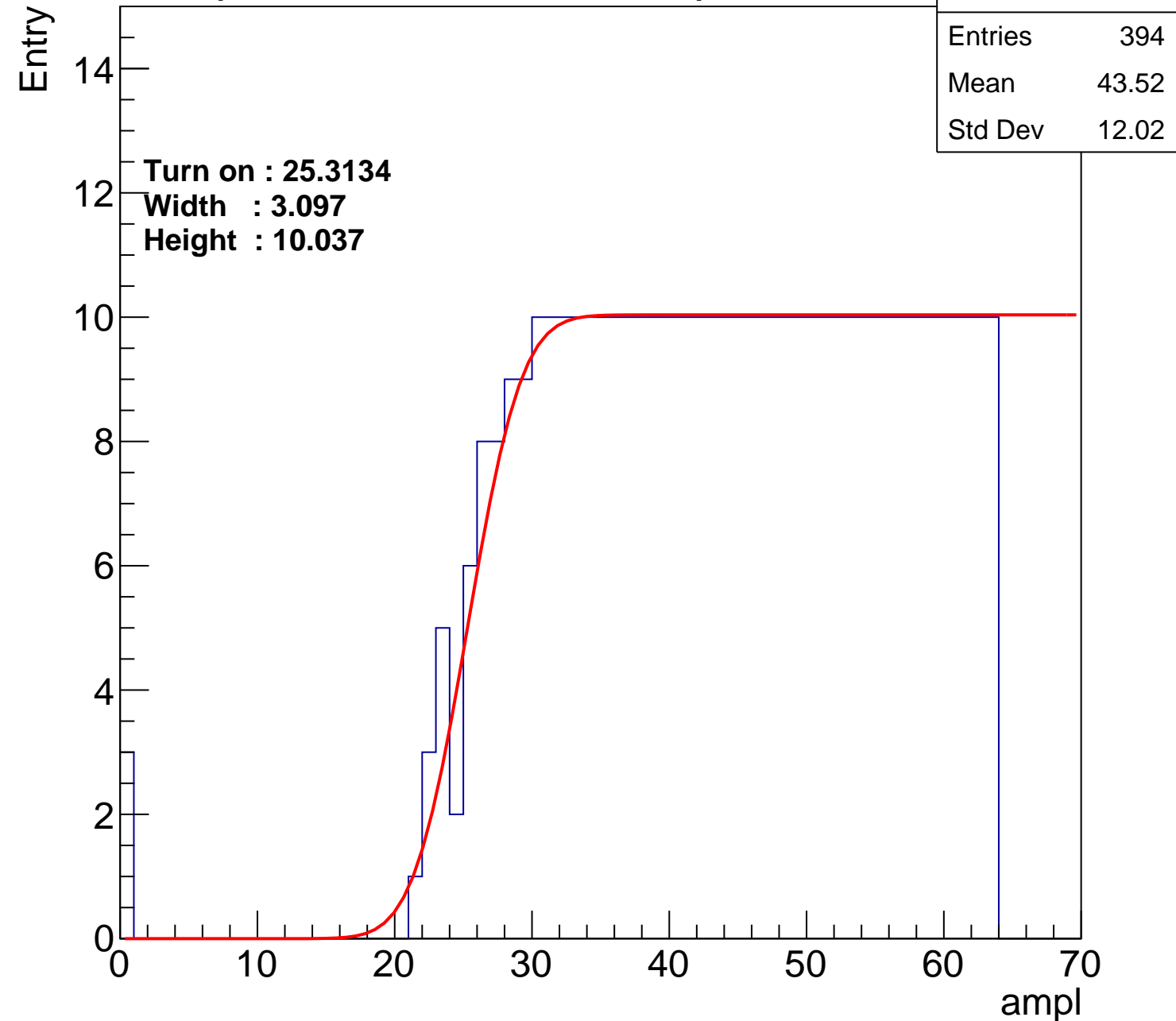
Width : 3.097

Height : 10.037

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L000S, U2-ch23

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	376
Mean	44.44
Std Dev	11.52

Turn on : 26.6679

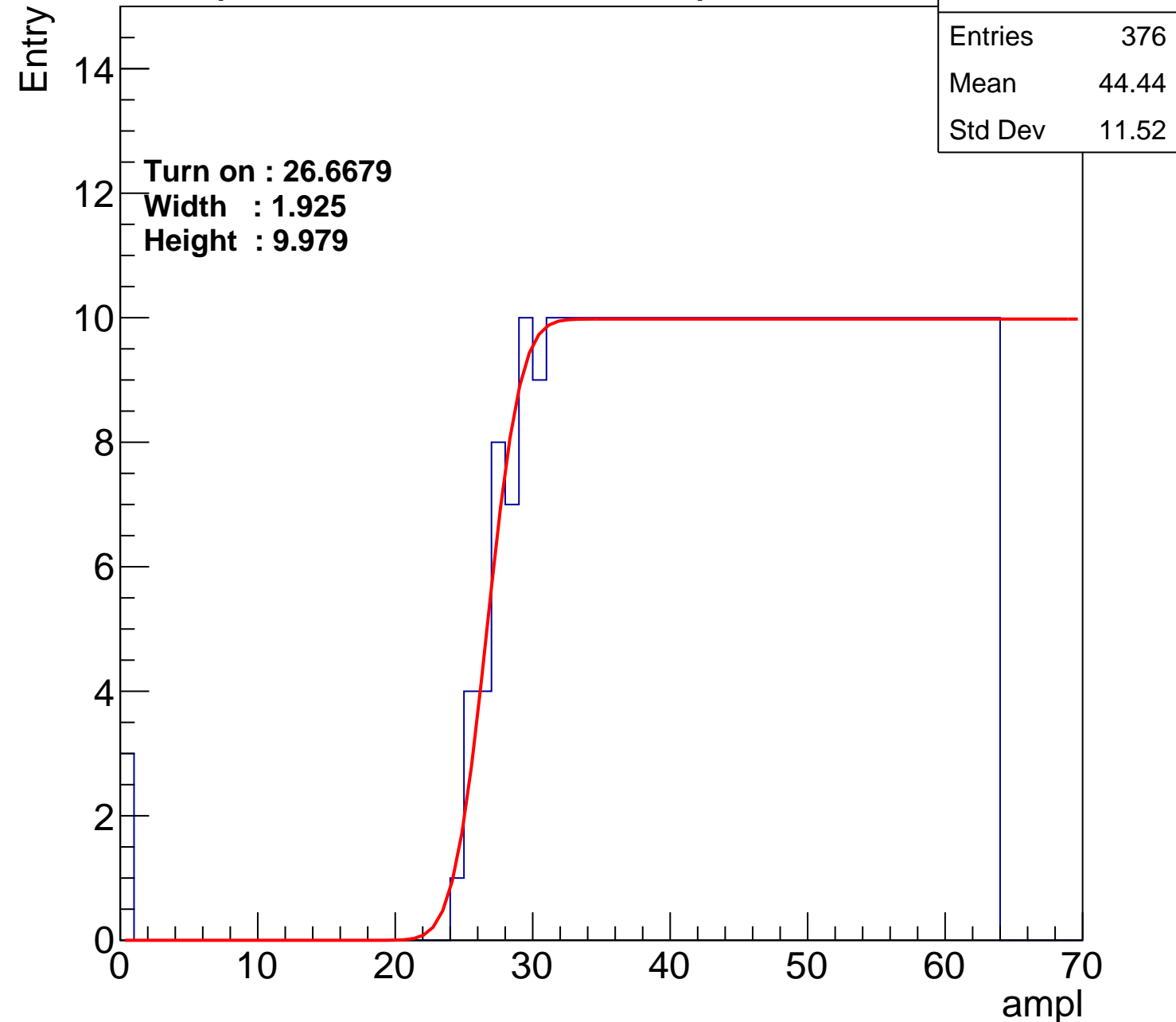
Width : 1.925

Height : 9.979

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch24

calib\_packv5\_042523\_0143.root, FC#3, port B3

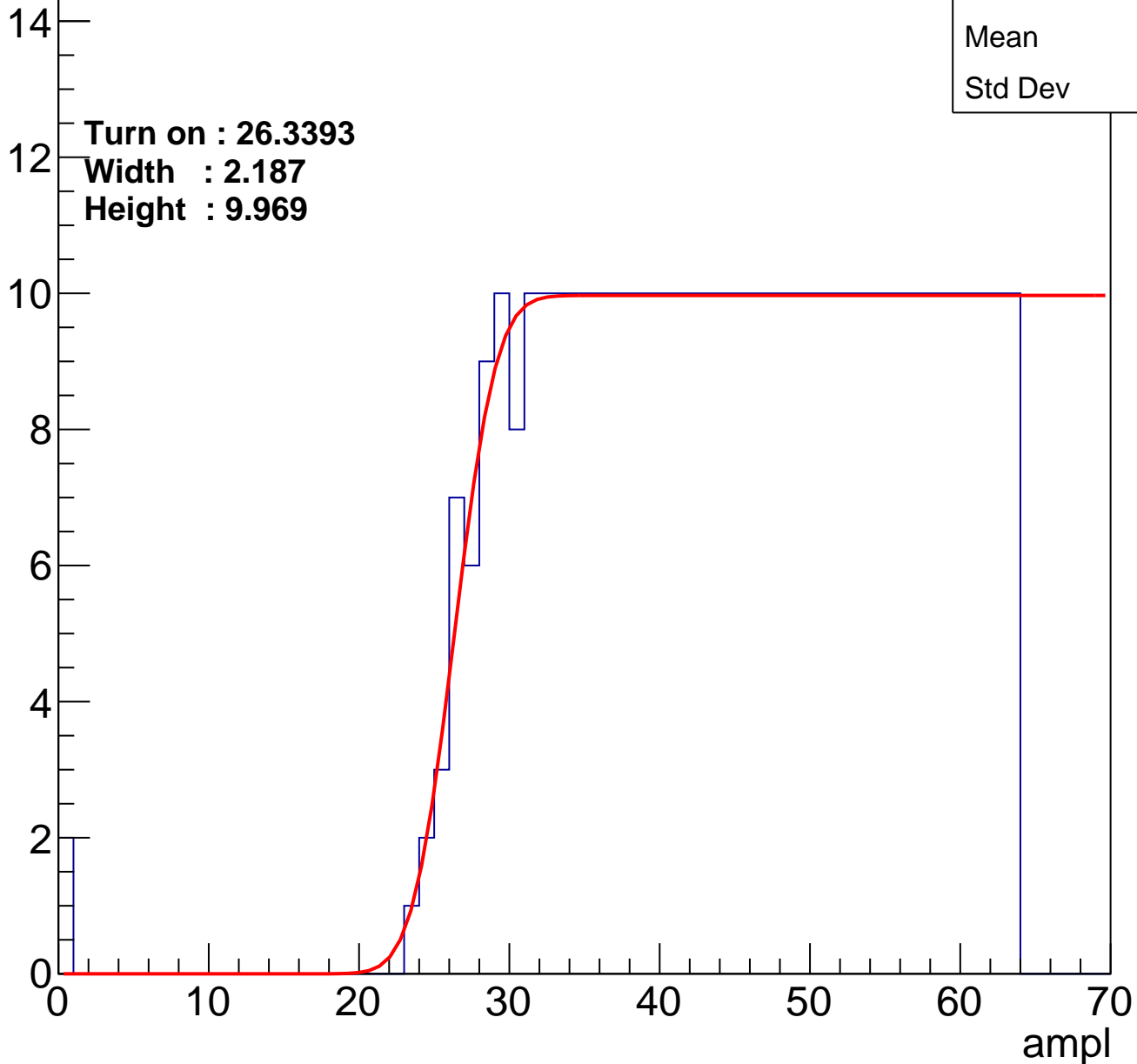
Entry

Entries	378
Mean	44.4
Std Dev	11.4

Turn on : 26.3393

Width : 2.187

Height : 9.969



# B1L000S, U2-ch25

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	396
Mean	43.35
Std Dev	12.24

**Turn on : 24.9404**

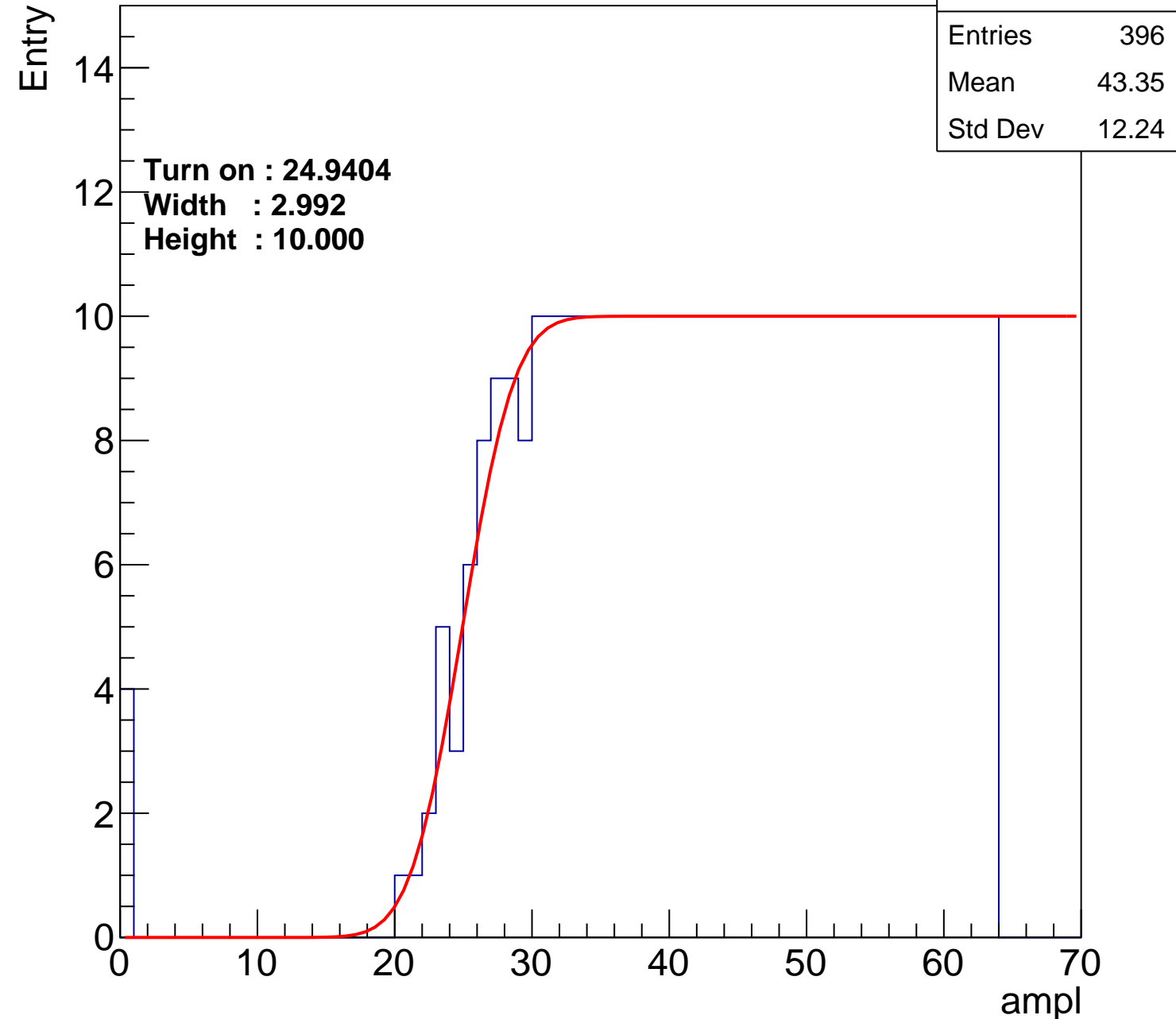
**Width : 2.992**

**Height : 10.000**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch26

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	379
Mean	44.32
Std Dev	11.48

Turn on : 26.2406

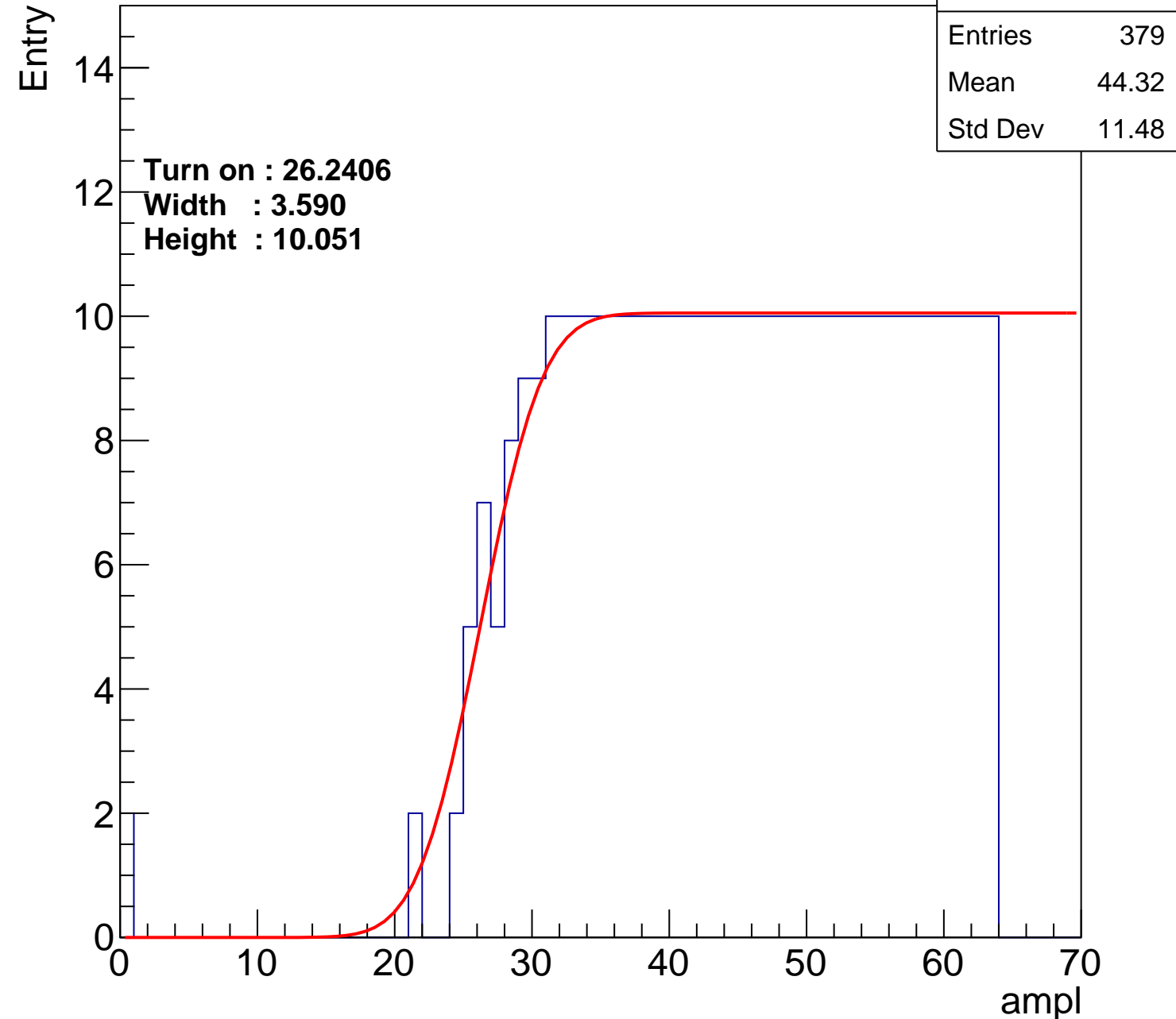
Width : 3.590

Height : 10.051

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch27

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	379
Mean	44.35
Std Dev	11.44

**Turn on : 26.3699**

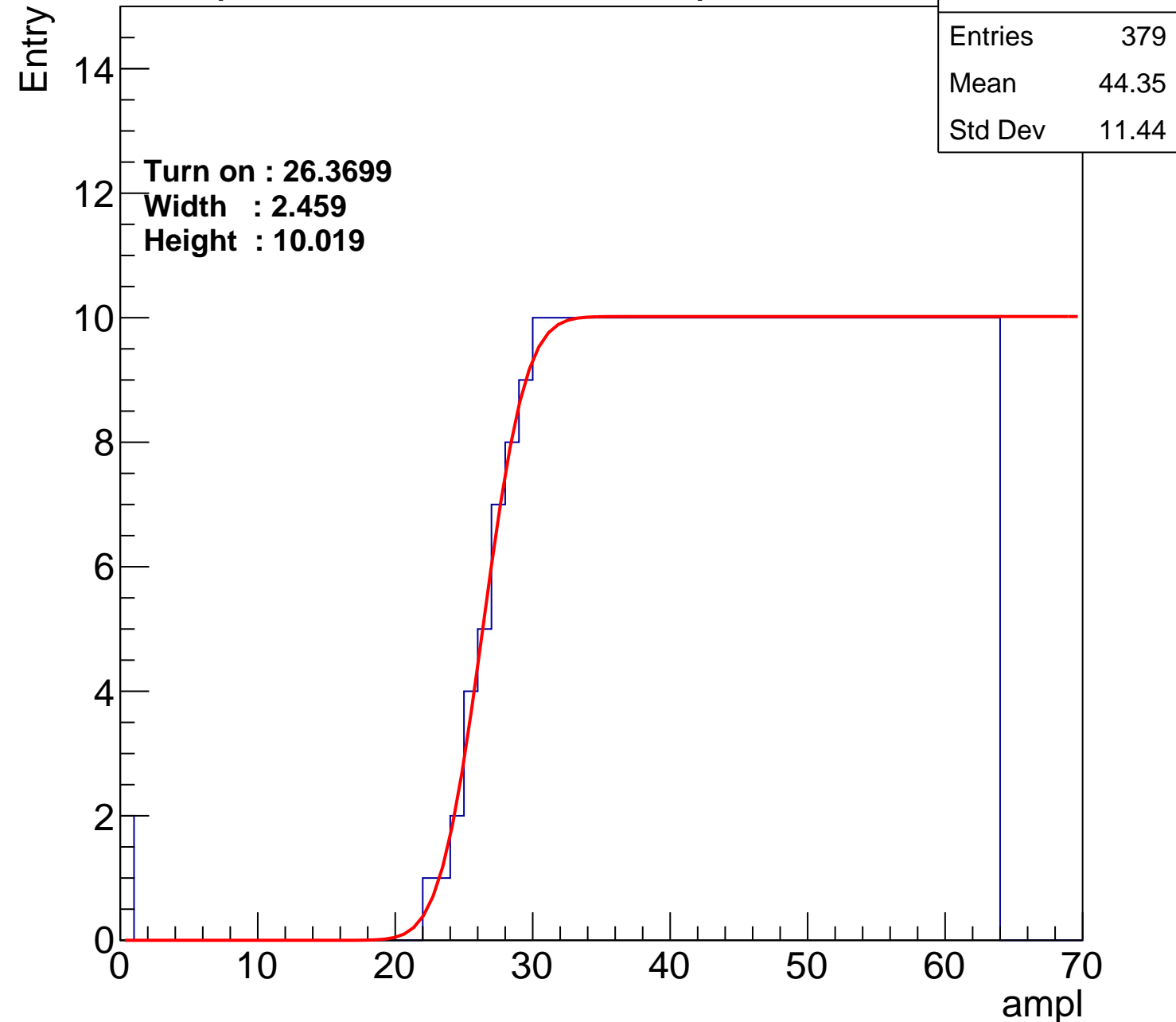
**Width : 2.459**

**Height : 10.019**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch28

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	381
Mean	44.28
Std Dev	11.35

Turn on : 26.3145

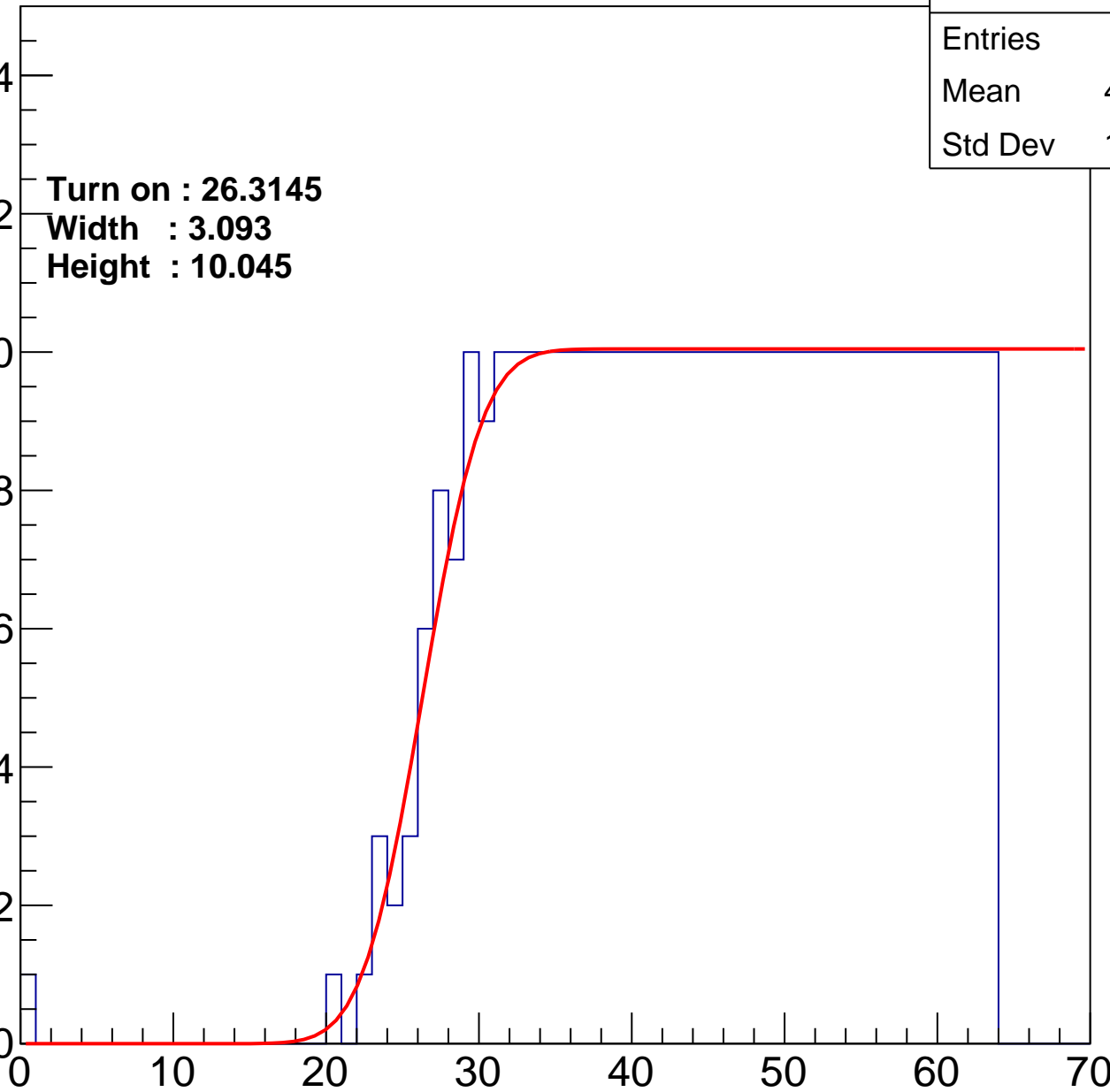
Width : 3.093

Height : 10.045

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch29

calib\_packv5\_042523\_0143.root, FC#3, port B3

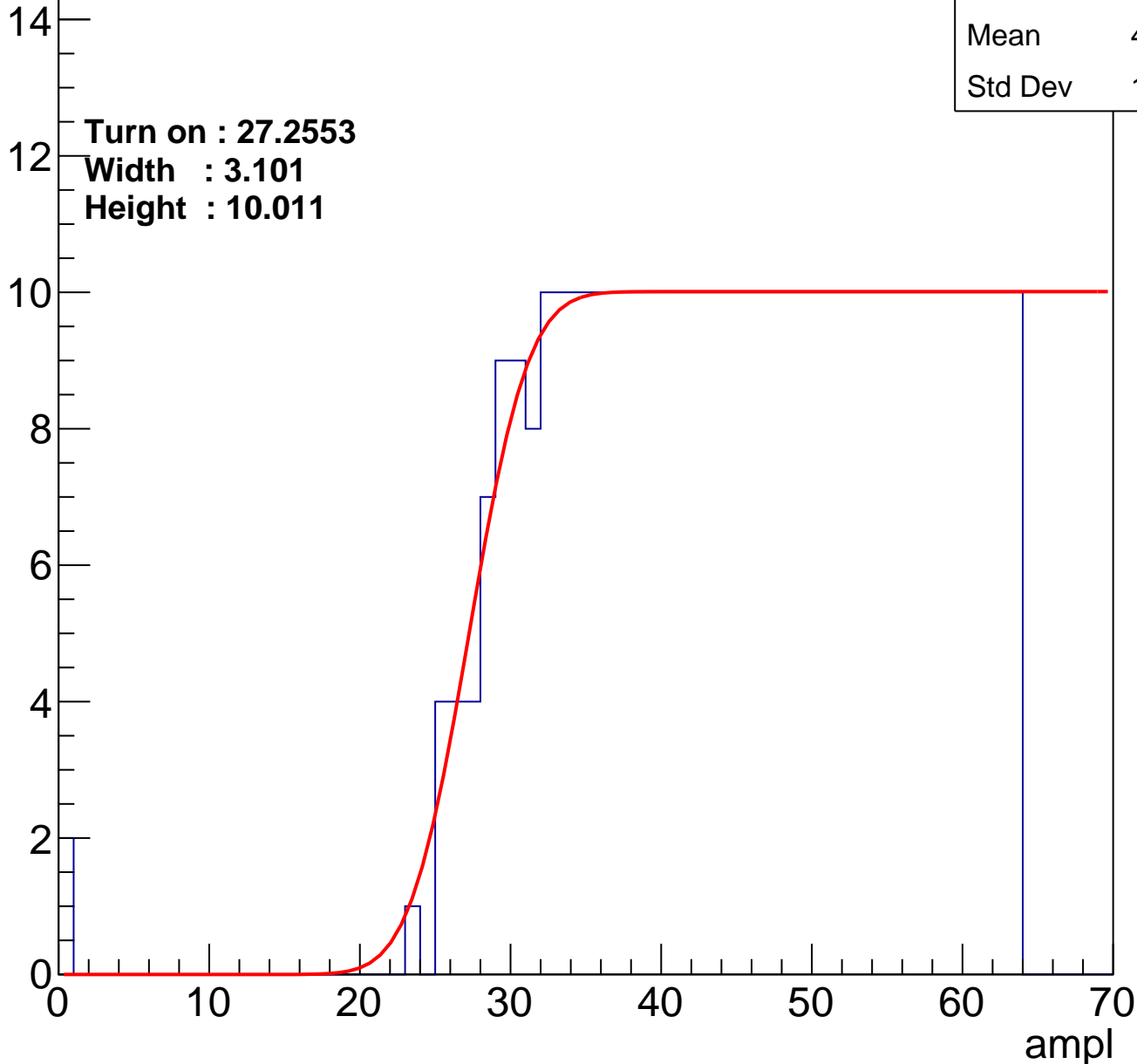
Entries	368
Mean	44.86
Std Dev	11.19

Turn on : 27.2553

Width : 3.101

Height : 10.011

Entry



# B1L000S, U2-ch30

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	411
Mean	42.83
Std Dev	12.12

**Turn on : 23.1907**

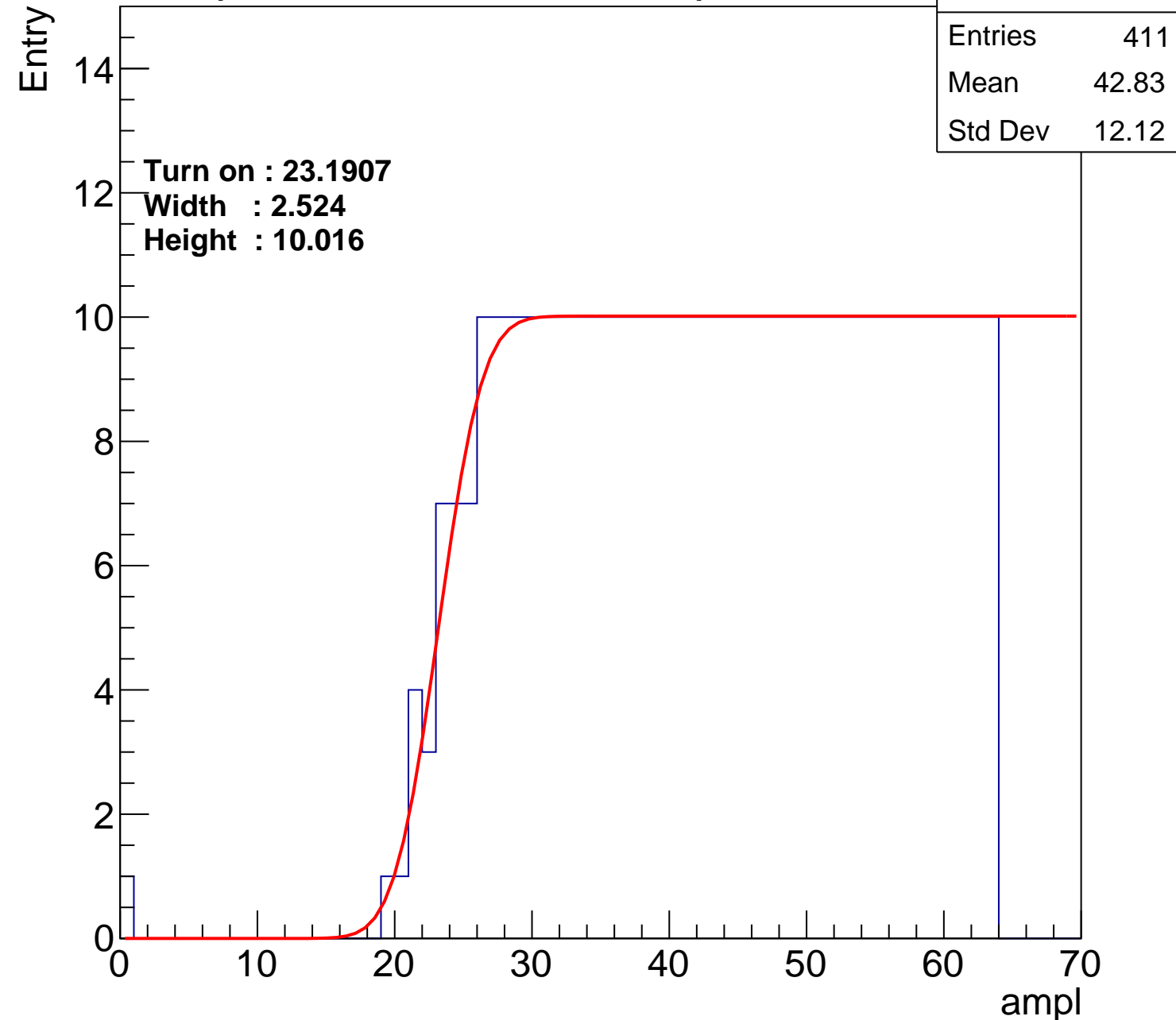
**Width : 2.524**

**Height : 10.016**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L000S, U2-ch31

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	387
Mean	43.89
Std Dev	11.8

Turn on : 25.8819

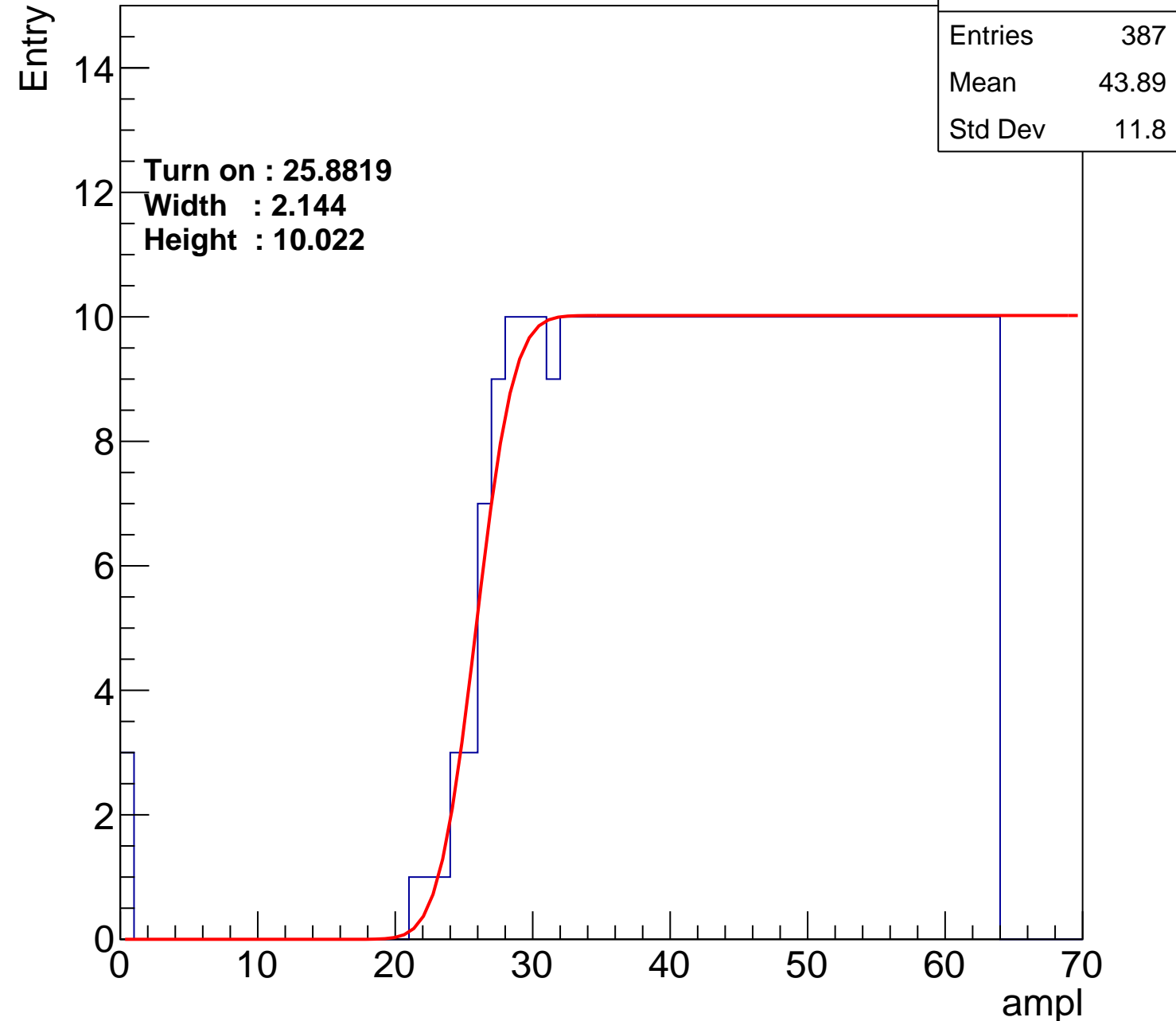
Width : 2.144

Height : 10.022

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch32

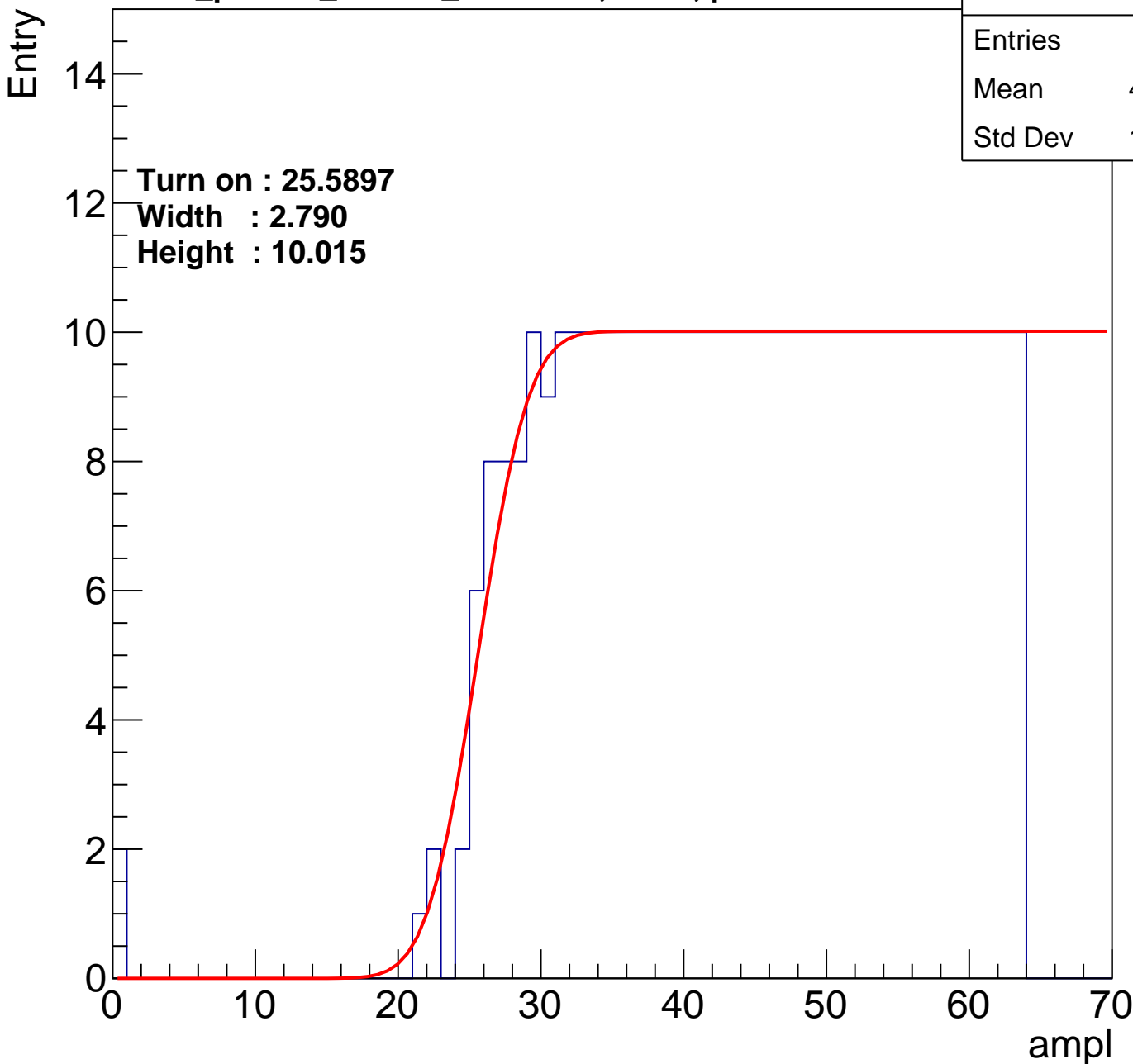
**calib\_packv5\_042523\_0143.root, FC#3, port B3**

Entries	386
Mean	43.99
Std Dev	11.63

**Turn on : 25.5897**

**Width : 2.790**

**Height : 10.015**



# B1L000S, U2-ch33

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	387
Mean	43.95
Std Dev	11.64

Turn on : 25.5141

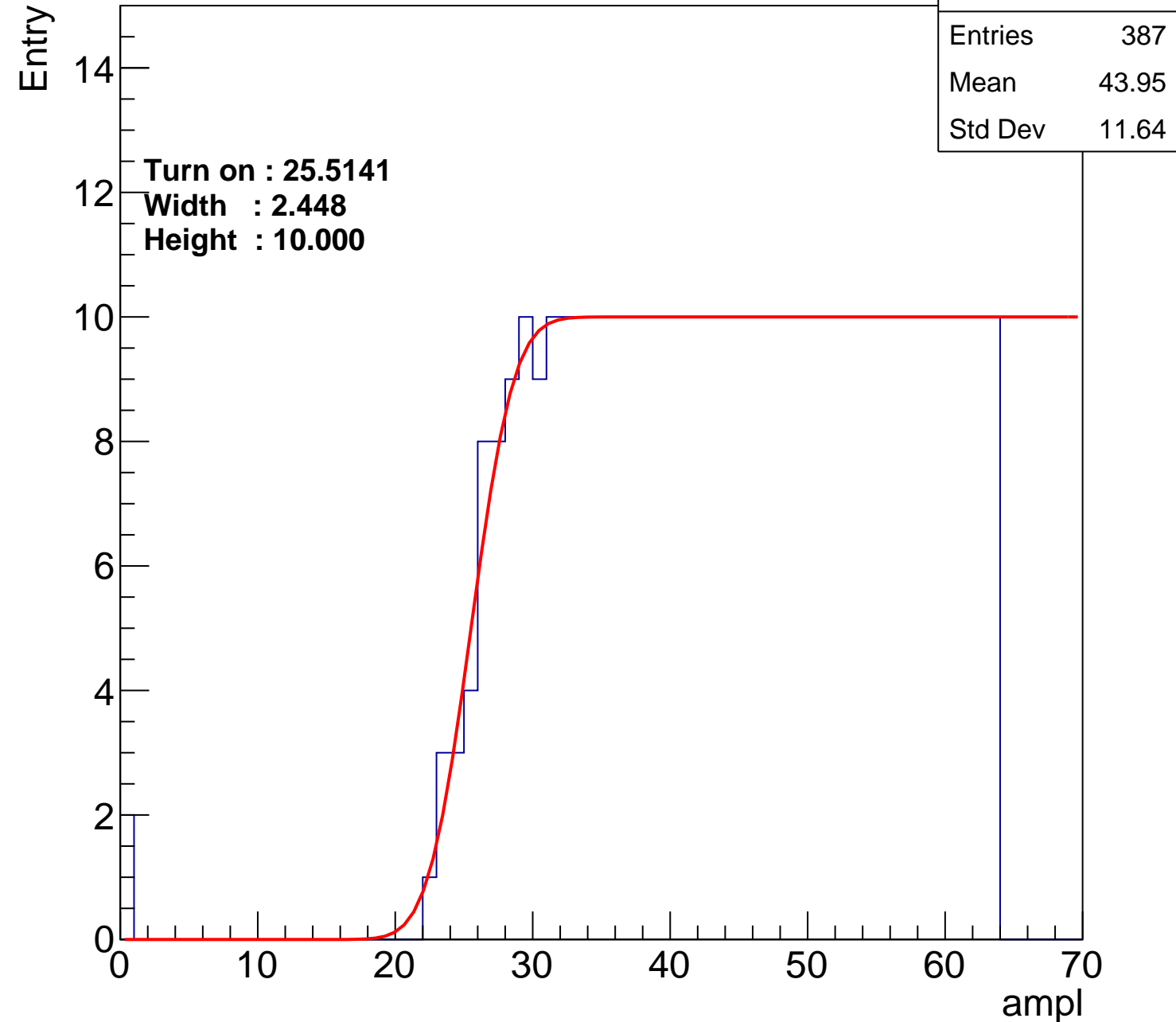
Width : 2.448

Height : 10.000

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch34

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	391
Mean	43.71
Std Dev	11.83

Turn on : 26.2636

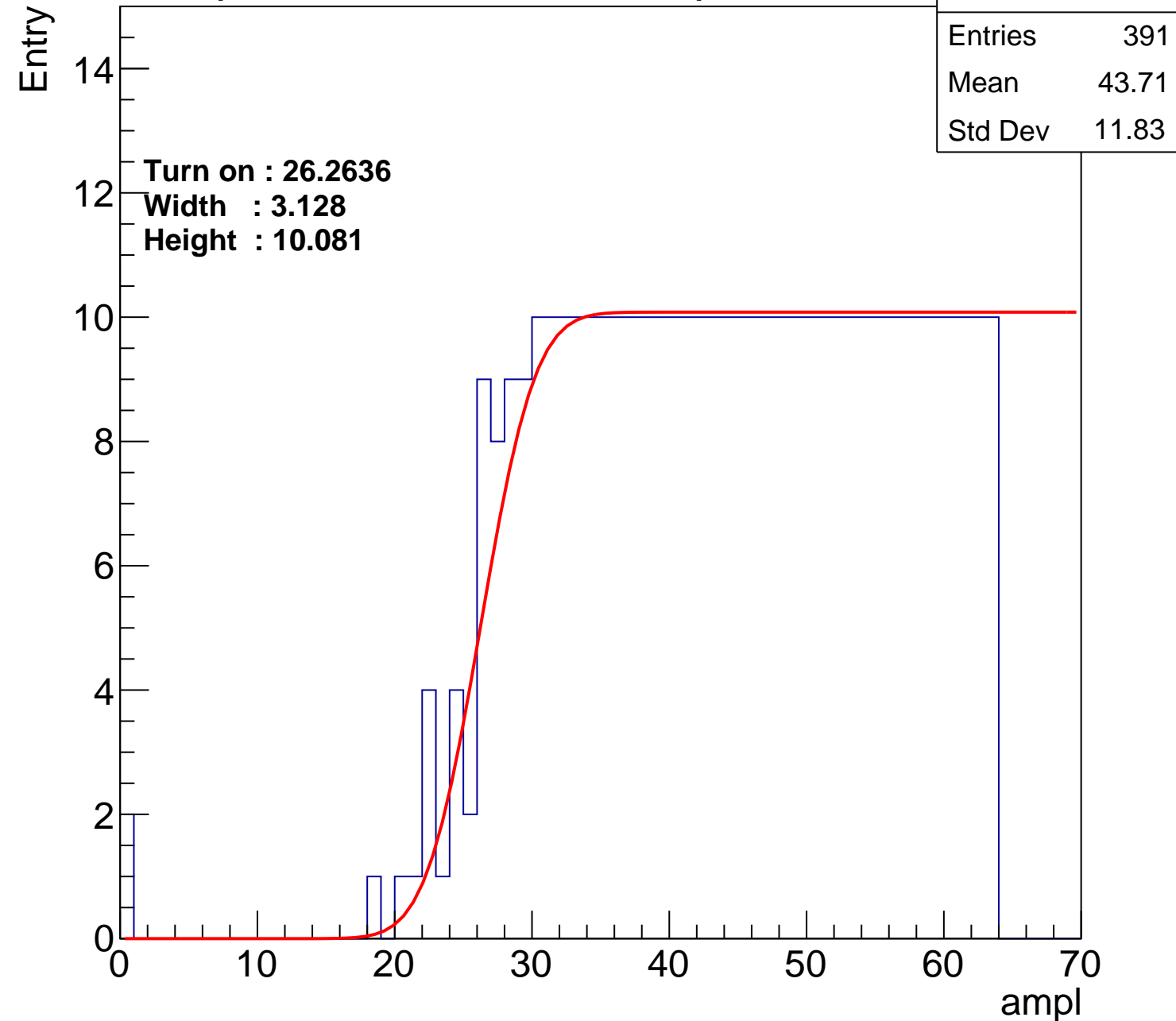
Width : 3.128

Height : 10.081

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch35

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	423
Mean	42.16
Std Dev	12.66

**Turn on : 22.0703**

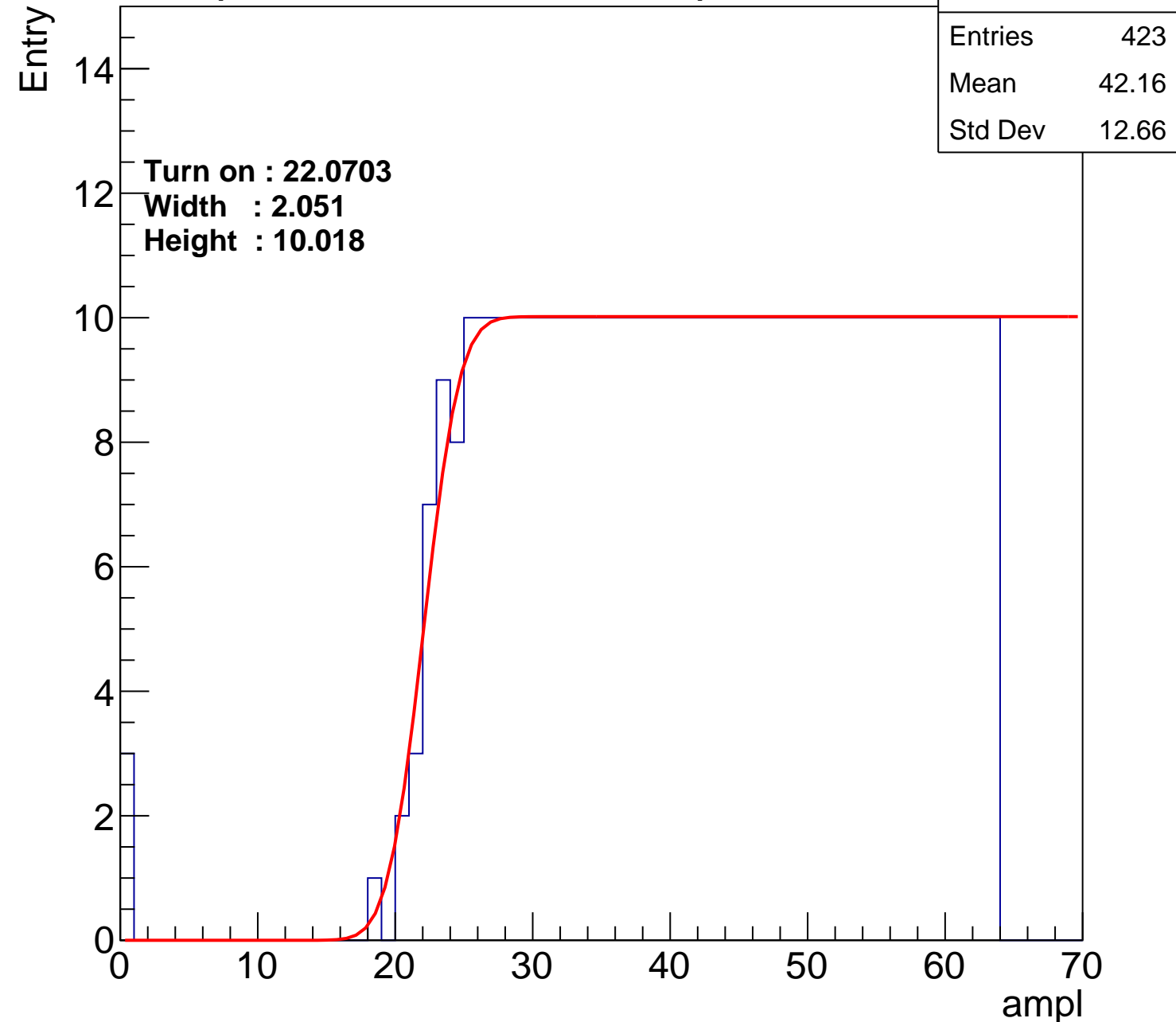
**Width : 2.051**

**Height : 10.018**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch36

calib\_packv5\_042523\_0143.root, FC#3, port B3

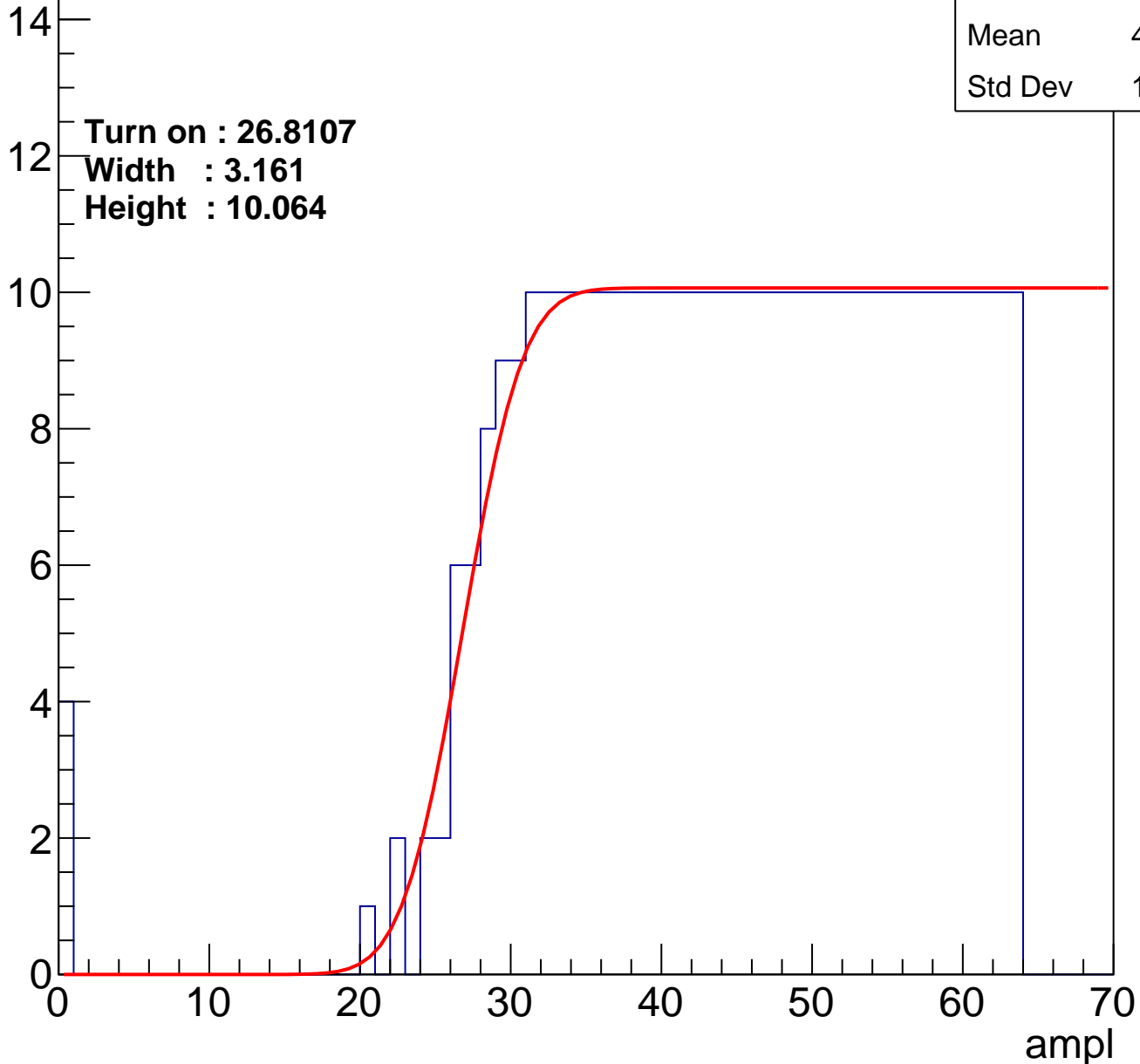
Entries	379
Mean	44.18
Std Dev	11.85

Turn on : 26.8107

Width : 3.161

Height : 10.064

Entry



# B1L000S, U2-ch37

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	394
Mean	43.69
Std Dev	11.62

Turn on : 24.6975

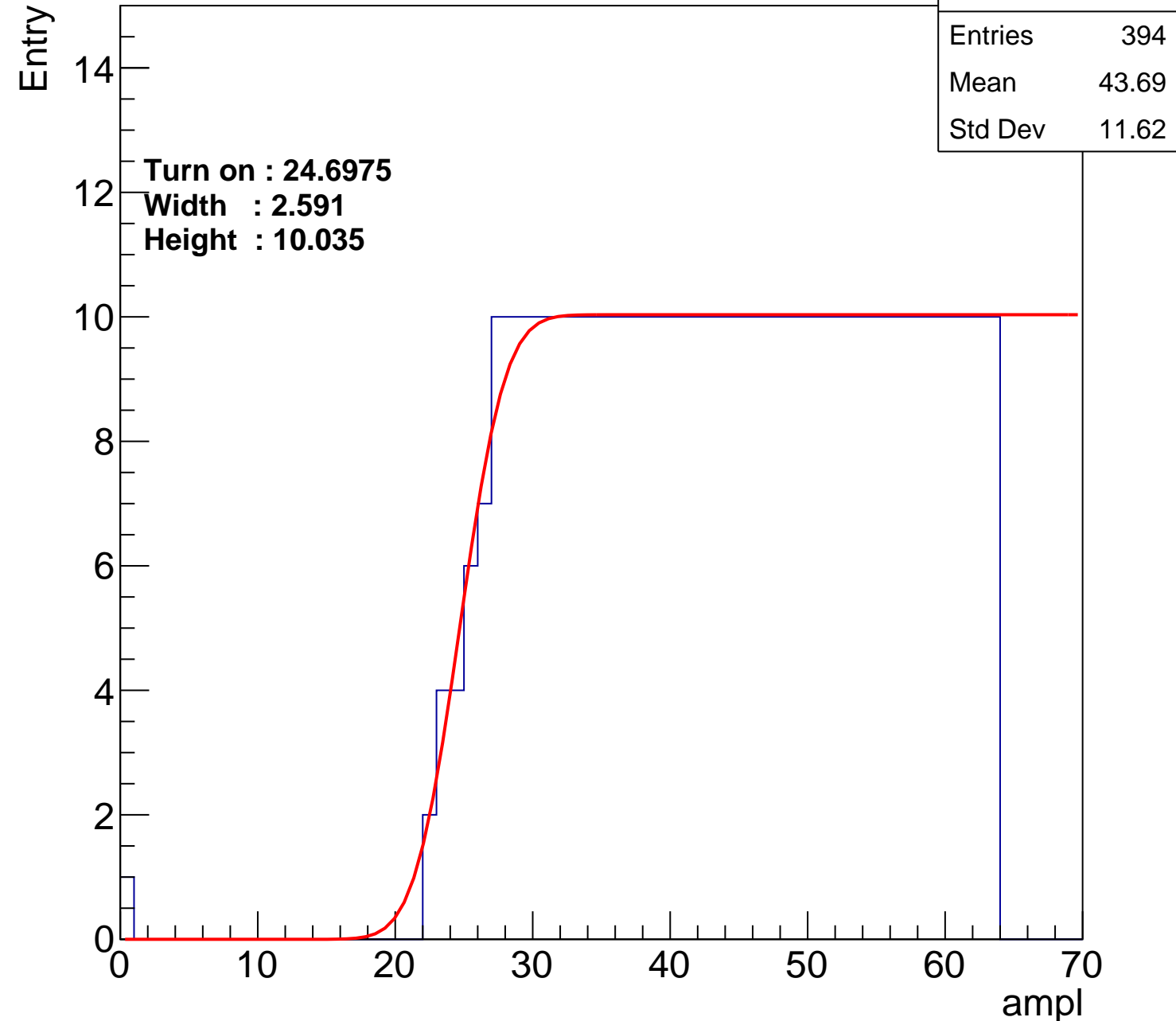
Width : 2.591

Height : 10.035

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch38

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	380
Mean	44.24
Std Dev	11.55

Turn on : 26.3296

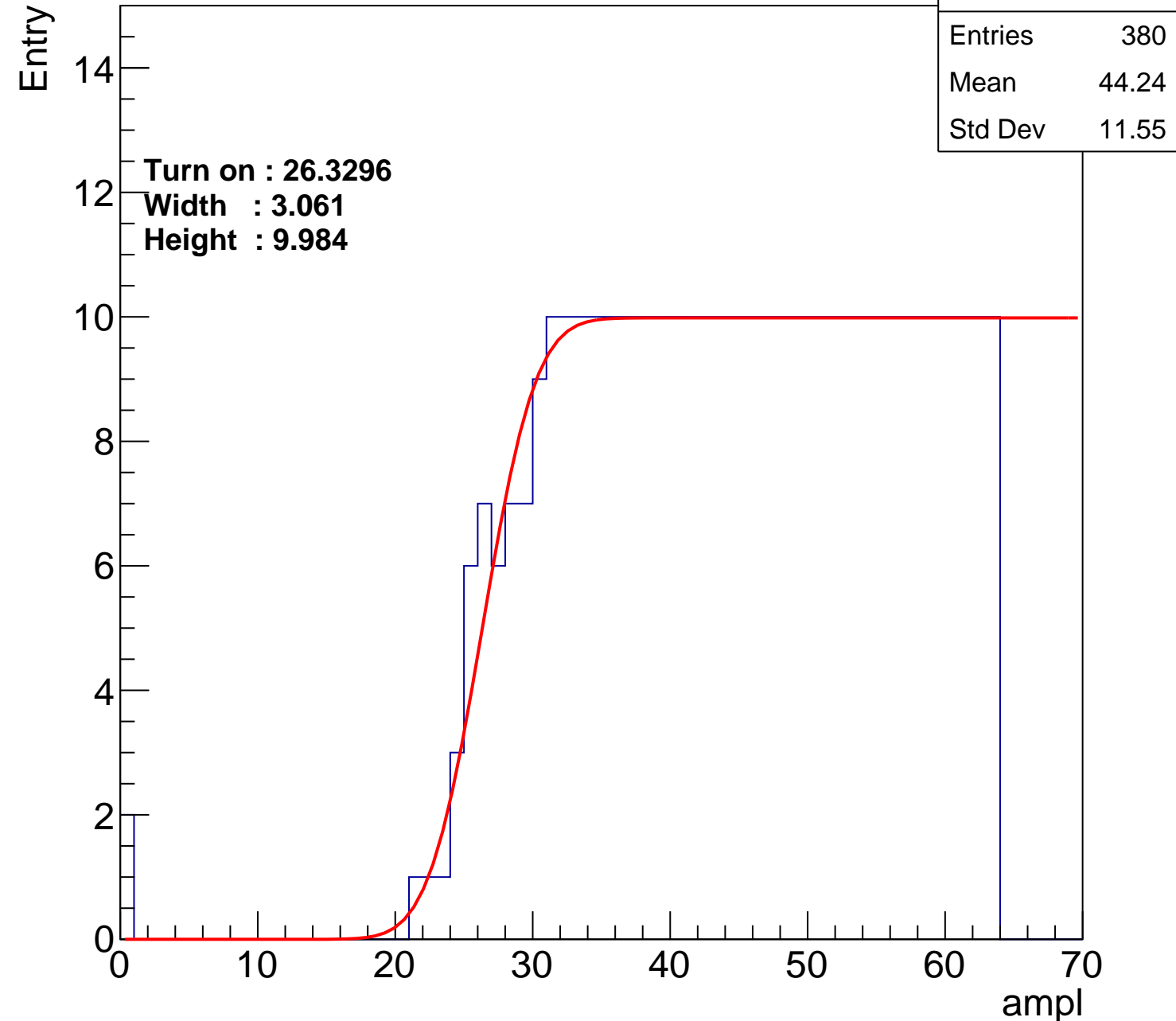
Width : 3.061

Height : 9.984

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L000S, U2-ch39

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	371
Mean	44.68
Std Dev	11.42

**Turn on : 27.3437**

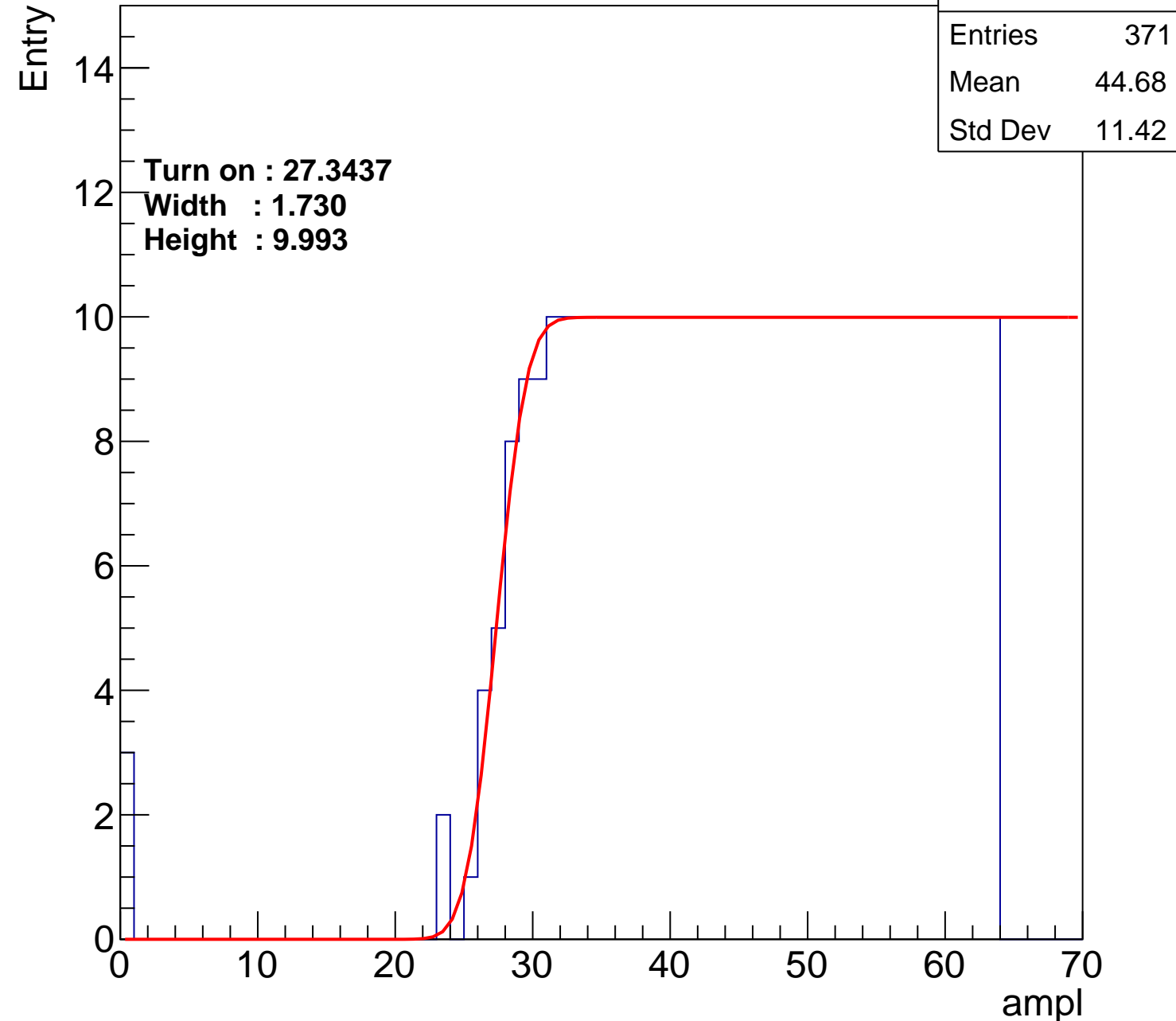
**Width : 1.730**

**Height : 9.993**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch40

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	385
Mean	43.93
Std Dev	11.92

Turn on : 25.5424

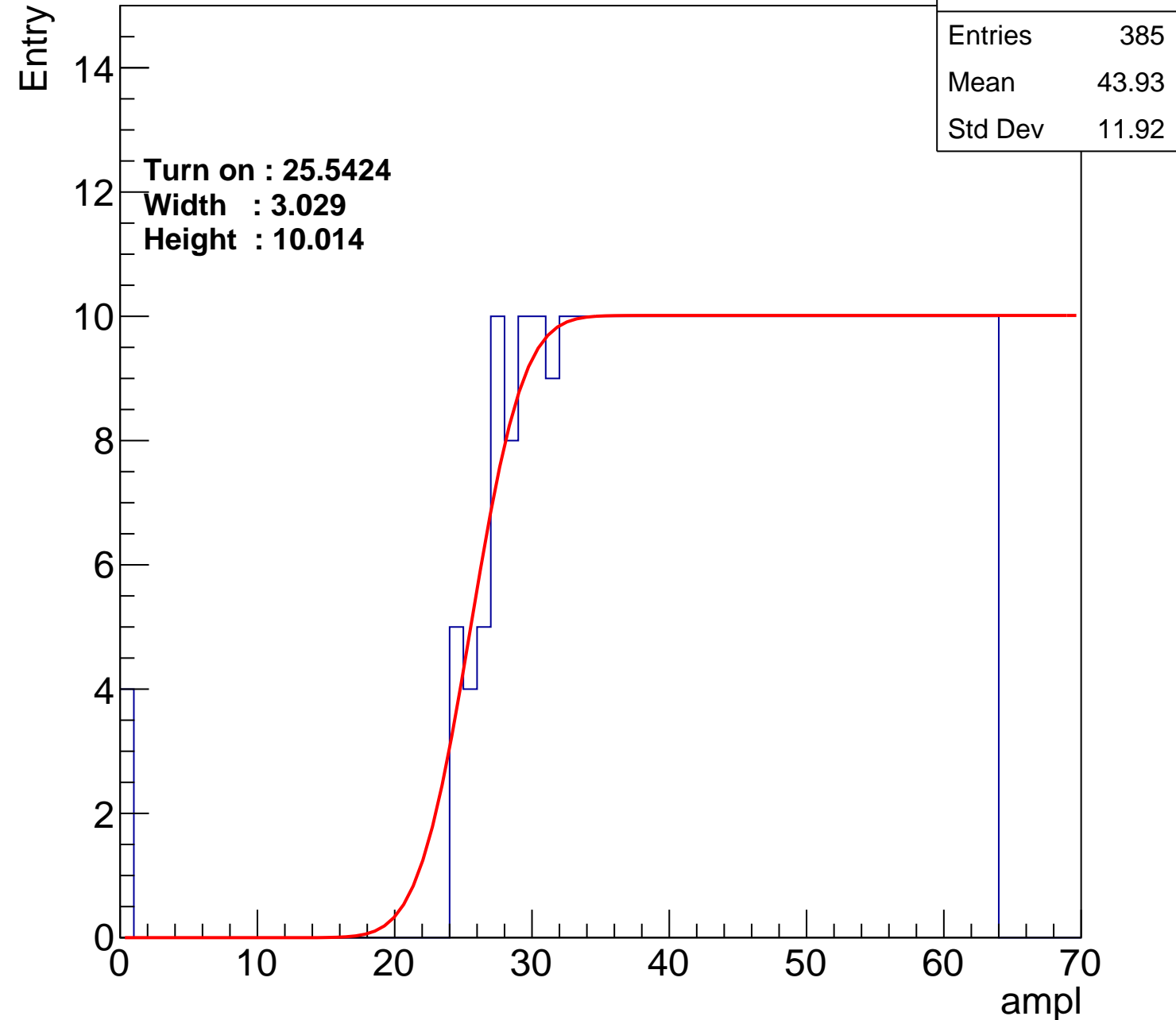
Width : 3.029

Height : 10.014

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch41

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	379
Mean	44.18
Std Dev	11.84

**Turn on : 26.8310**

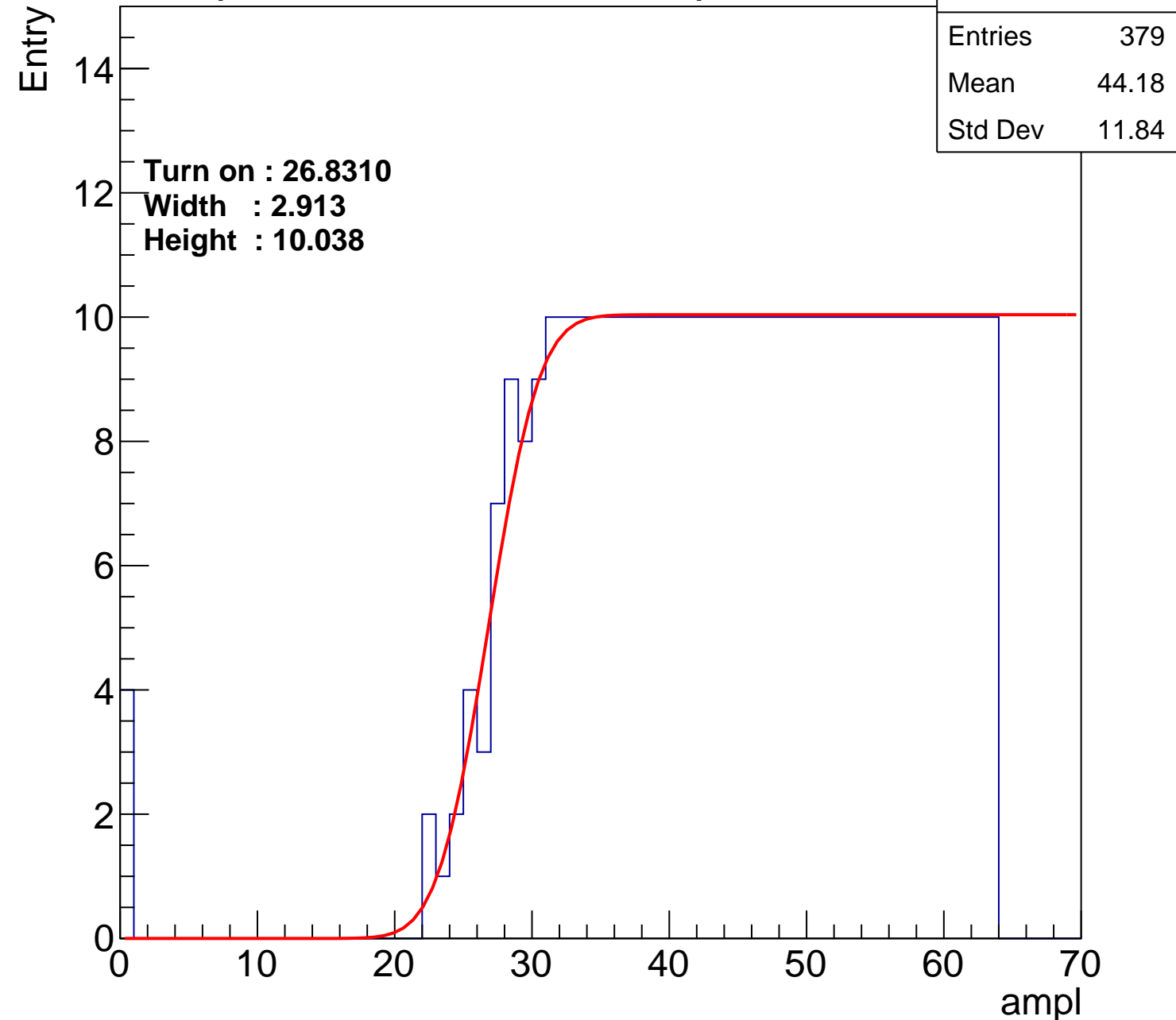
**Width : 2.913**

**Height : 10.038**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch42

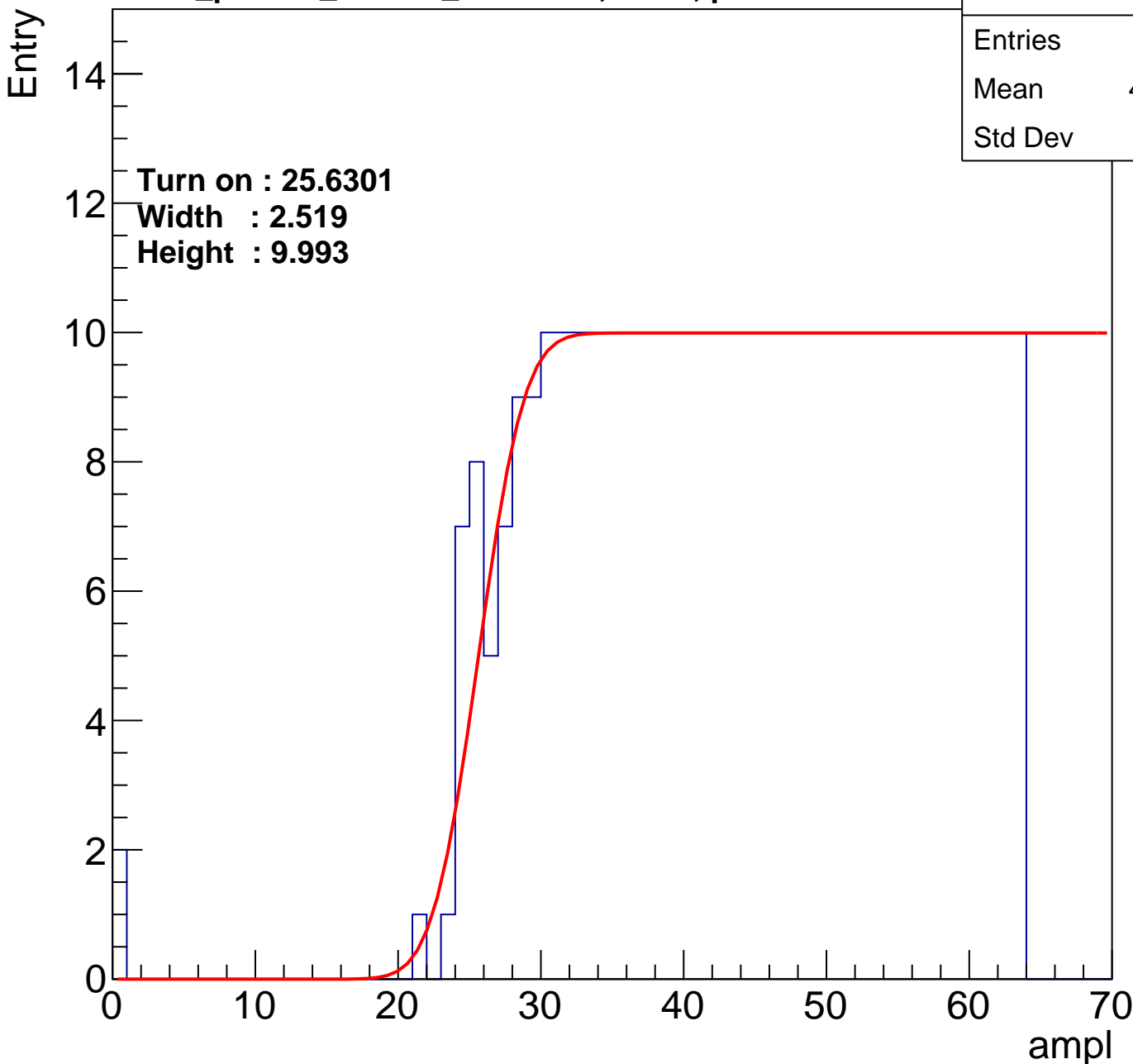
**calib\_packv5\_042523\_0143.root, FC#3, port B3**

Entries	389
Mean	43.84
Std Dev	11.71

**Turn on : 25.6301**

**Width : 2.519**

**Height : 9.993**



# B1L000S, U2-ch43

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	391
Mean	43.68
Std Dev	11.93

**Turn on : 25.5434**

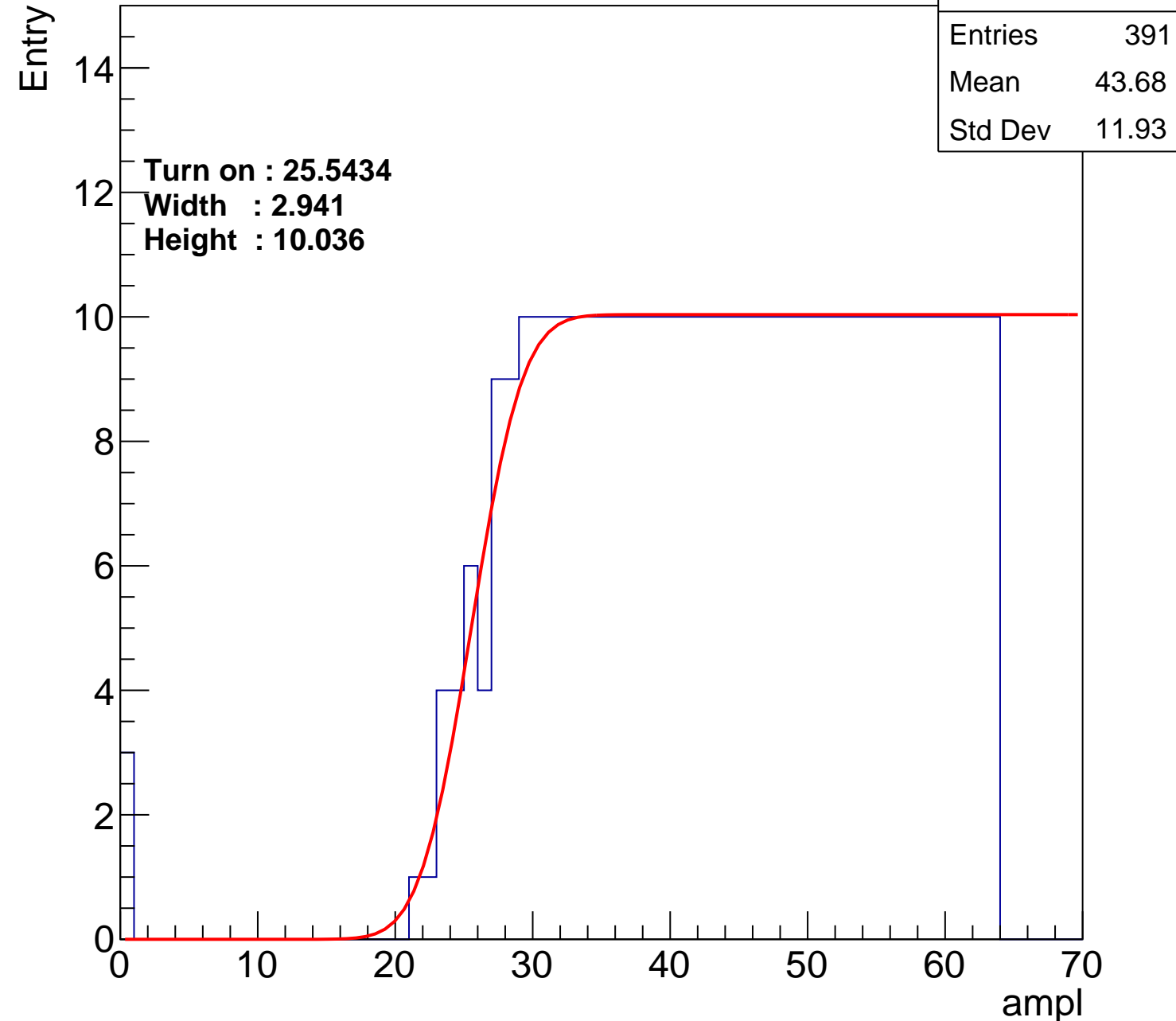
**Width : 2.941**

**Height : 10.036**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch44

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	398
Mean	43.3
Std Dev	12.22

Turn on : 24.9245

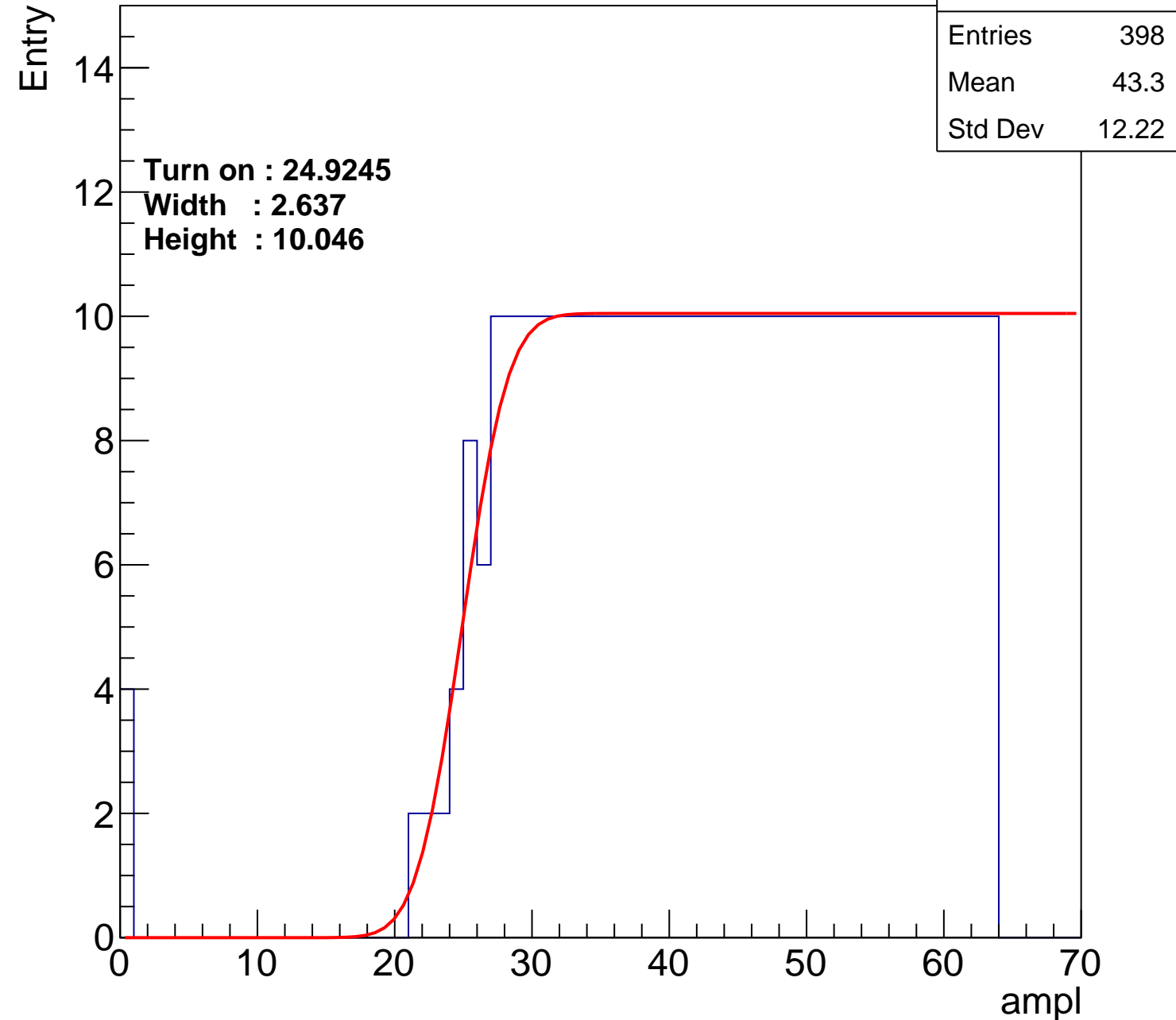
Width : 2.637

Height : 10.046

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch45

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	395
Mean	43.64
Std Dev	11.66

**Turn on : 24.5723**

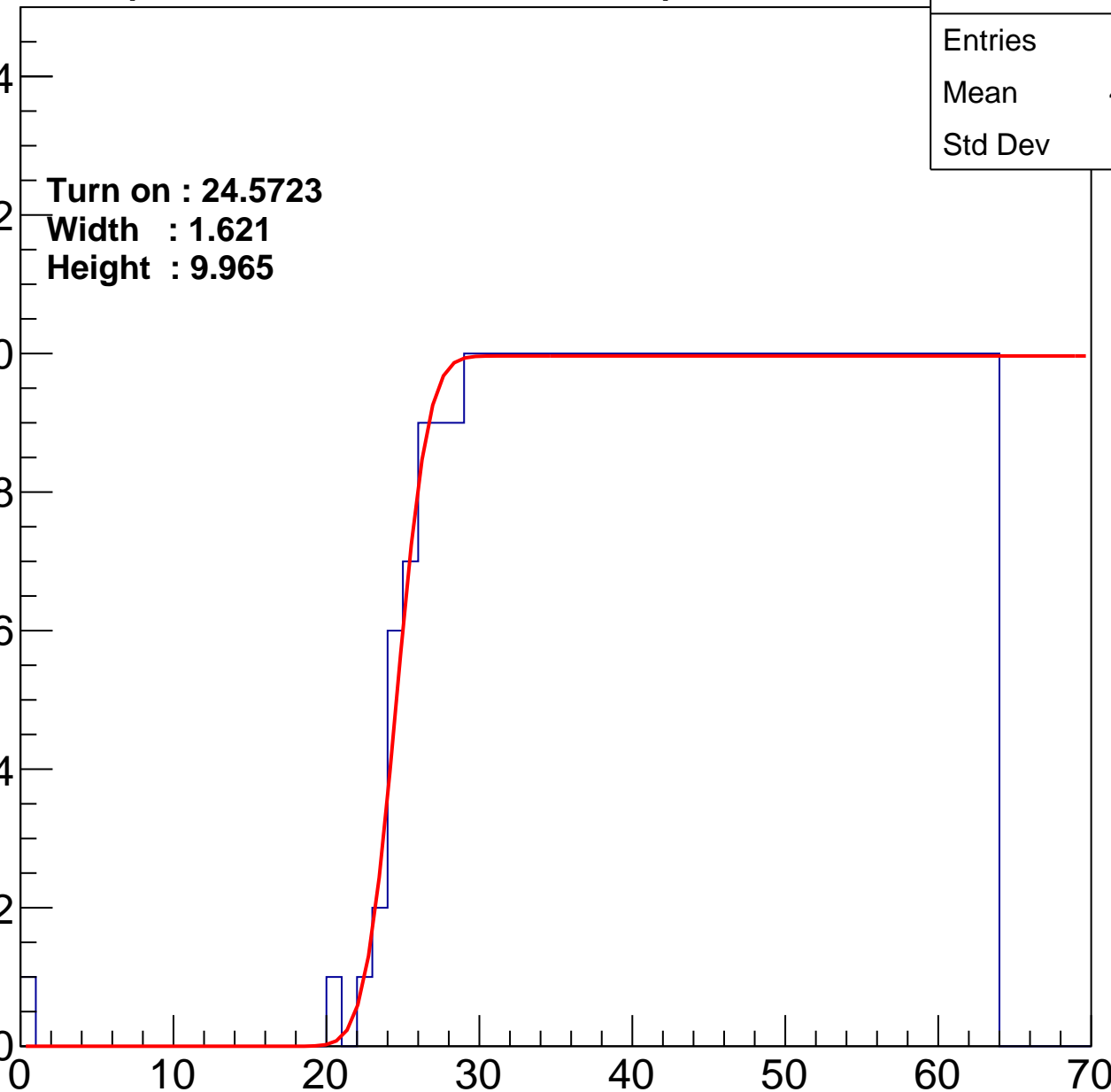
**Width : 1.621**

**Height : 9.965**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch46

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	386
Mean	43.79
Std Dev	12.15

**Turn on : 26.3735**

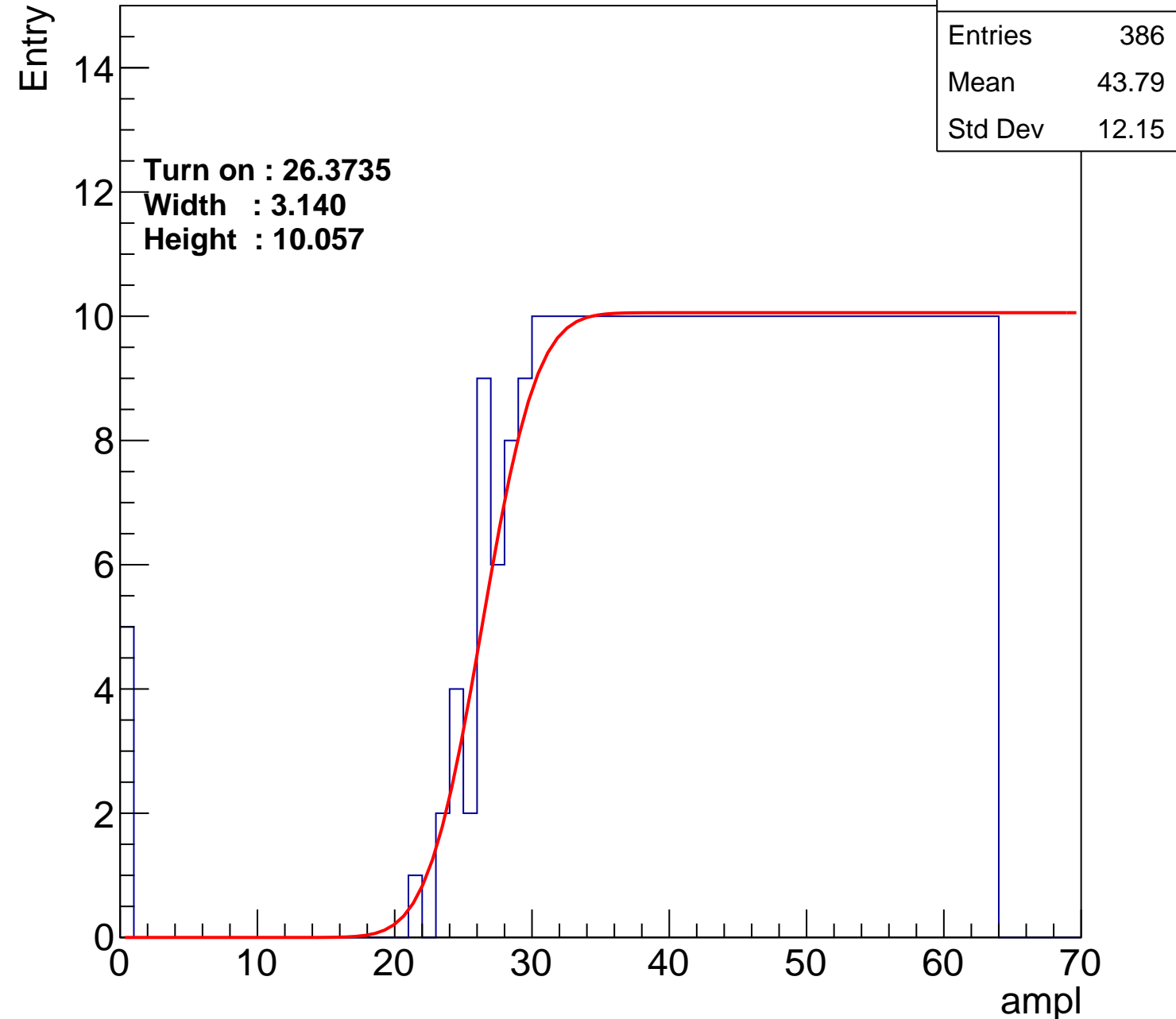
**Width : 3.140**

**Height : 10.057**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L000S, U2-ch47

calib\_packv5\_042523\_0143.root, FC#3, port B3

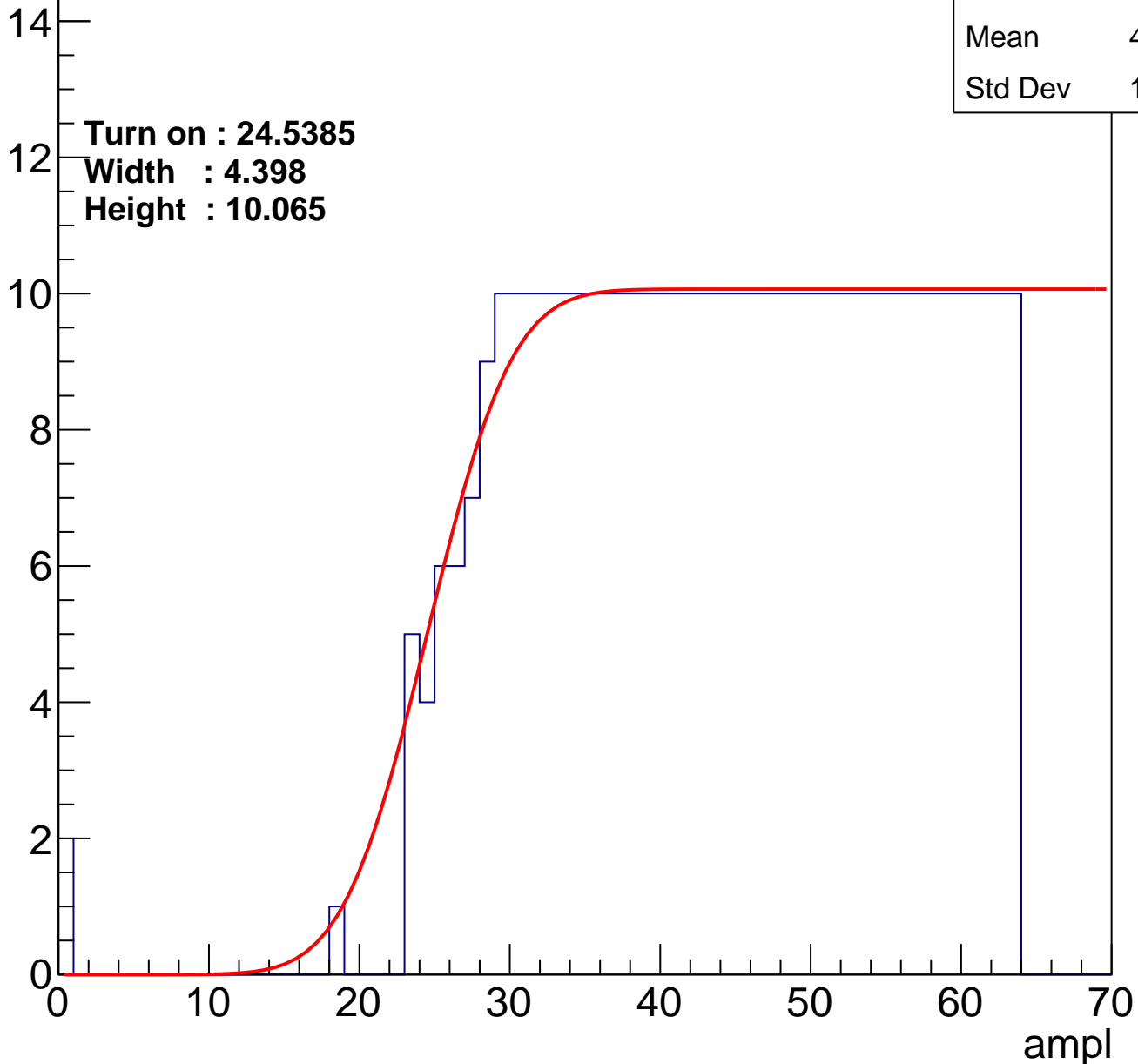
Entries	390
Mean	43.78
Std Dev	11.75

**Turn on : 24.5385**

**Width : 4.398**

**Height : 10.065**

Entry



# B1L000S, U2-ch48

calib\_packv5\_042523\_0143.root, FC#3, port B3

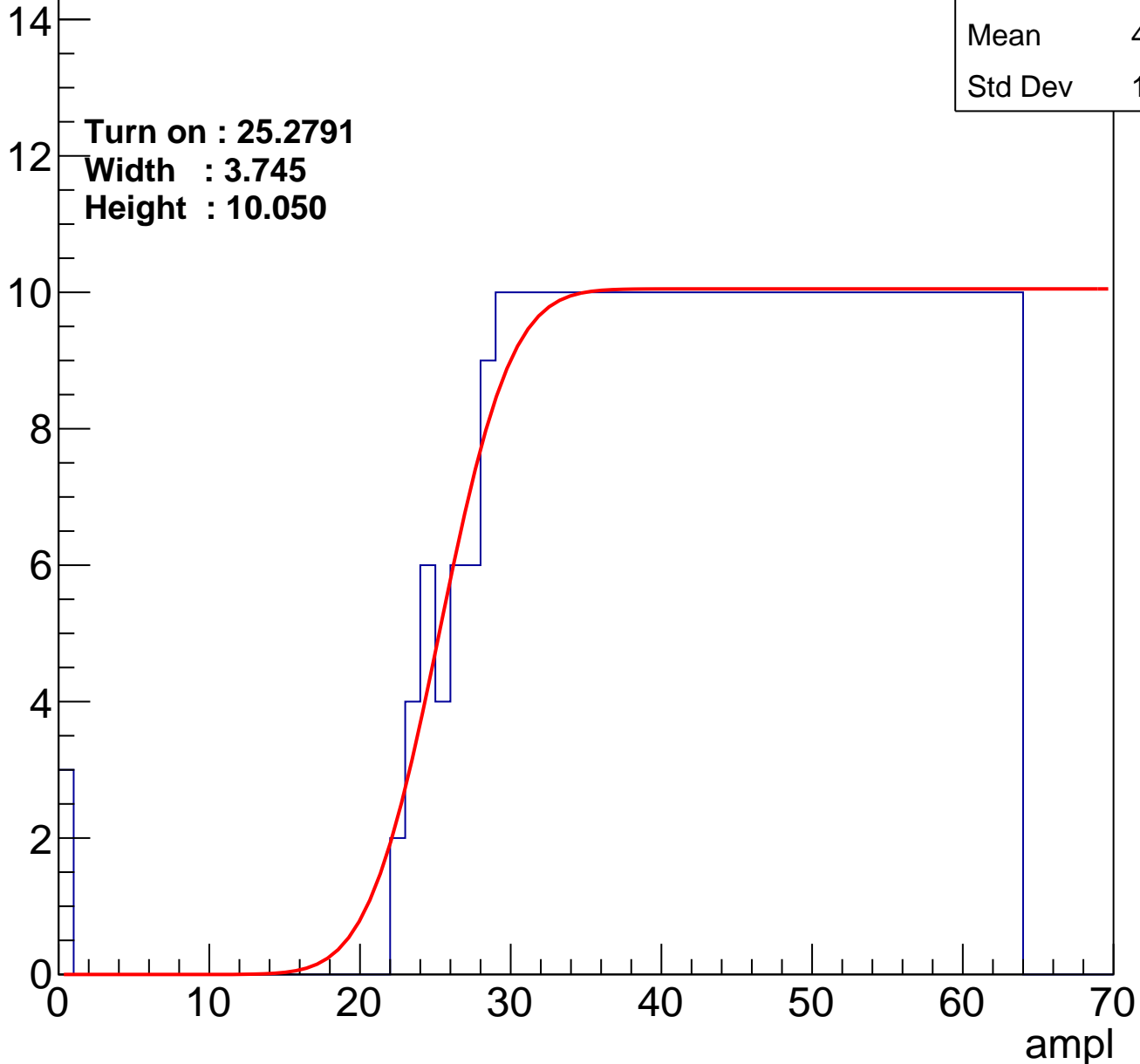
Entries	390
Mean	43.72
Std Dev	11.92

Turn on : 25.2791

Width : 3.745

Height : 10.050

Entry



# B1L000S, U2-ch49

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	374
Mean	44.54
Std Dev	11.4

Turn on : 27.2870

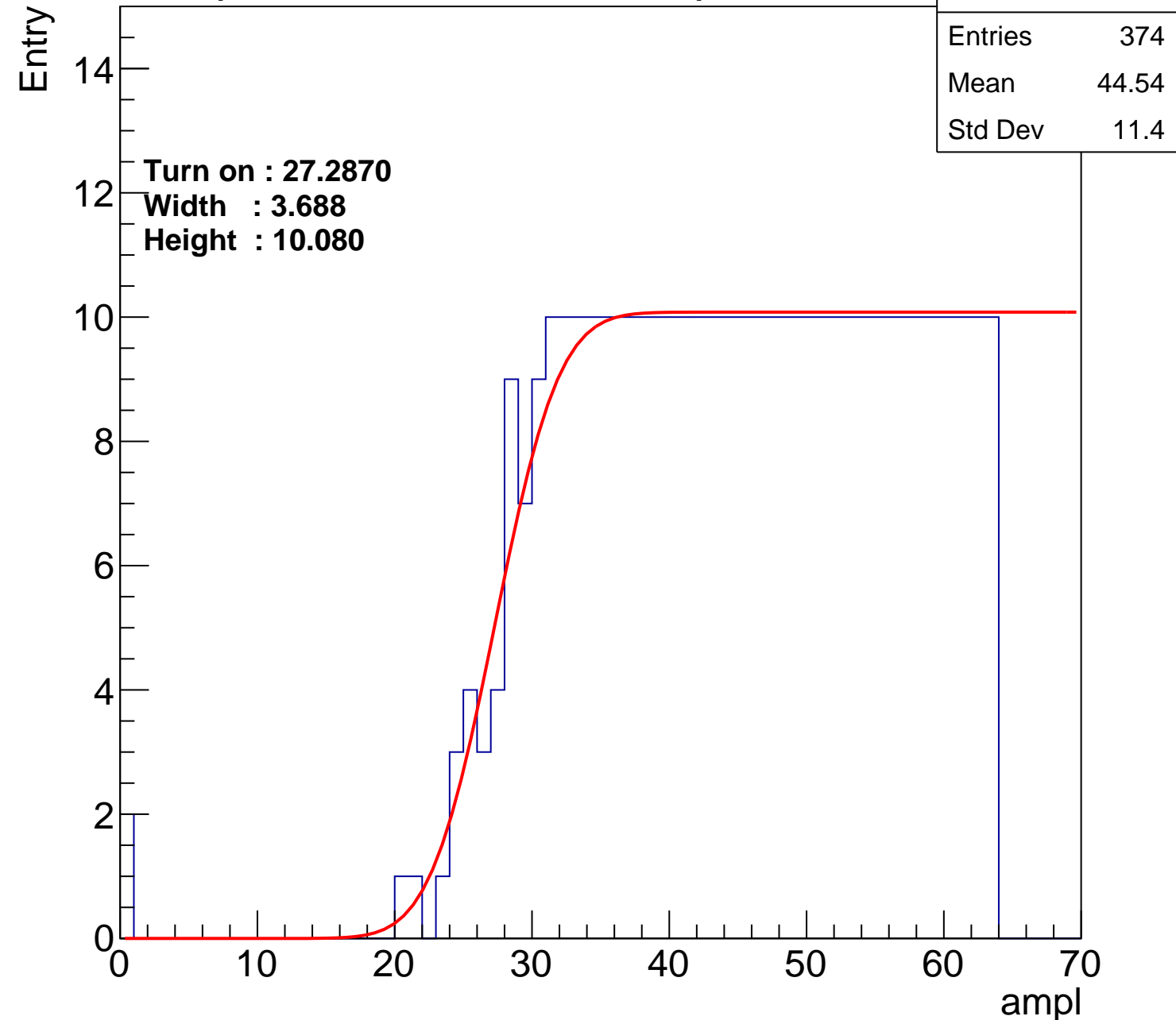
Width : 3.688

Height : 10.080

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch50

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	387
Mean	43.73
Std Dev	12.2

Turn on : 26.4913

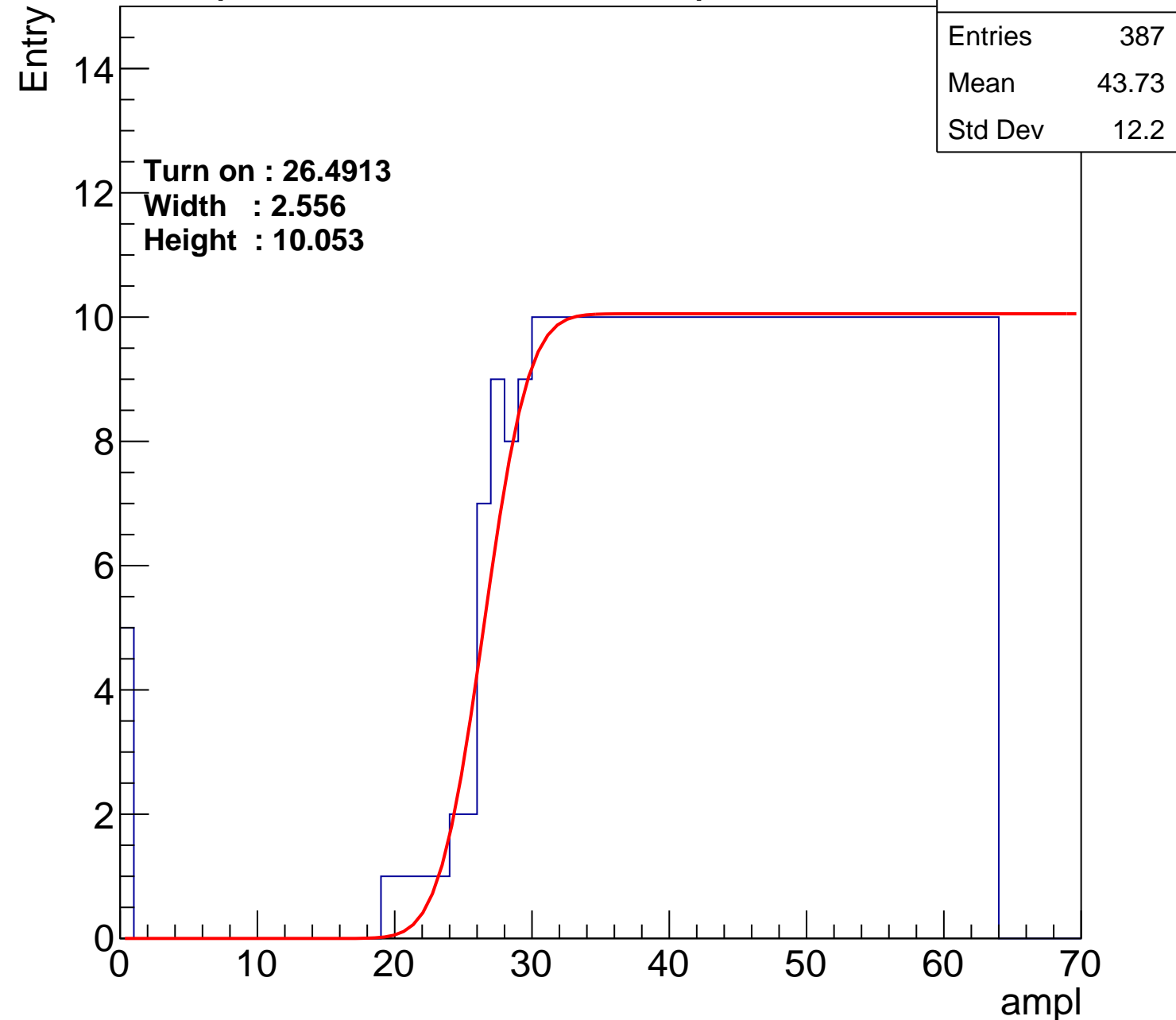
Width : 2.556

Height : 10.053

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch51

calib\_packv5\_042523\_0143.root, FC#3, port B3

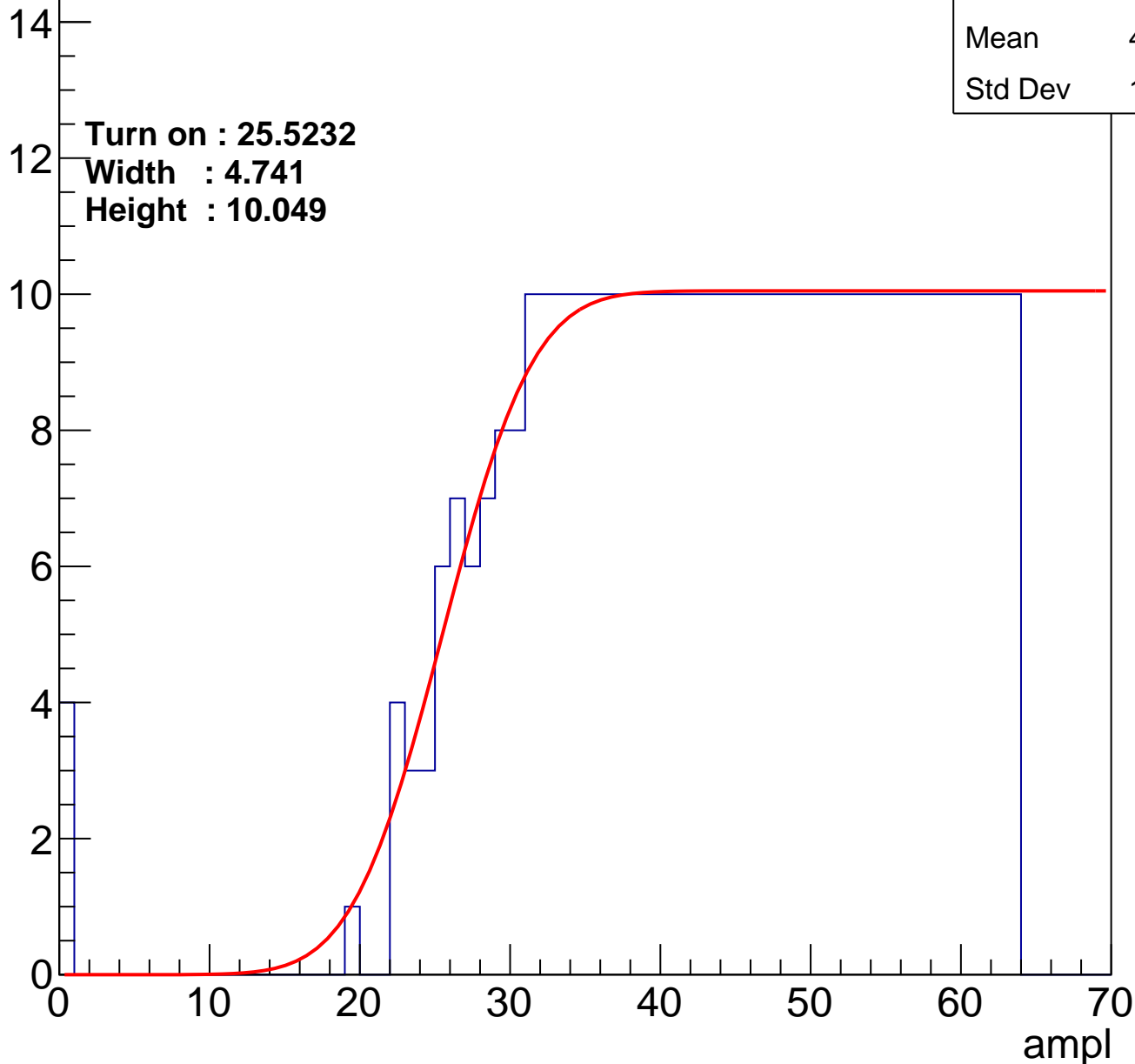
Entries	387
Mean	43.72
Std Dev	12.14

Turn on : 25.5232

Width : 4.741

Height : 10.049

Entry



# B1L000S, U2-ch52

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	386
Mean	43.94
Std Dev	11.78

Turn on : 25.7719

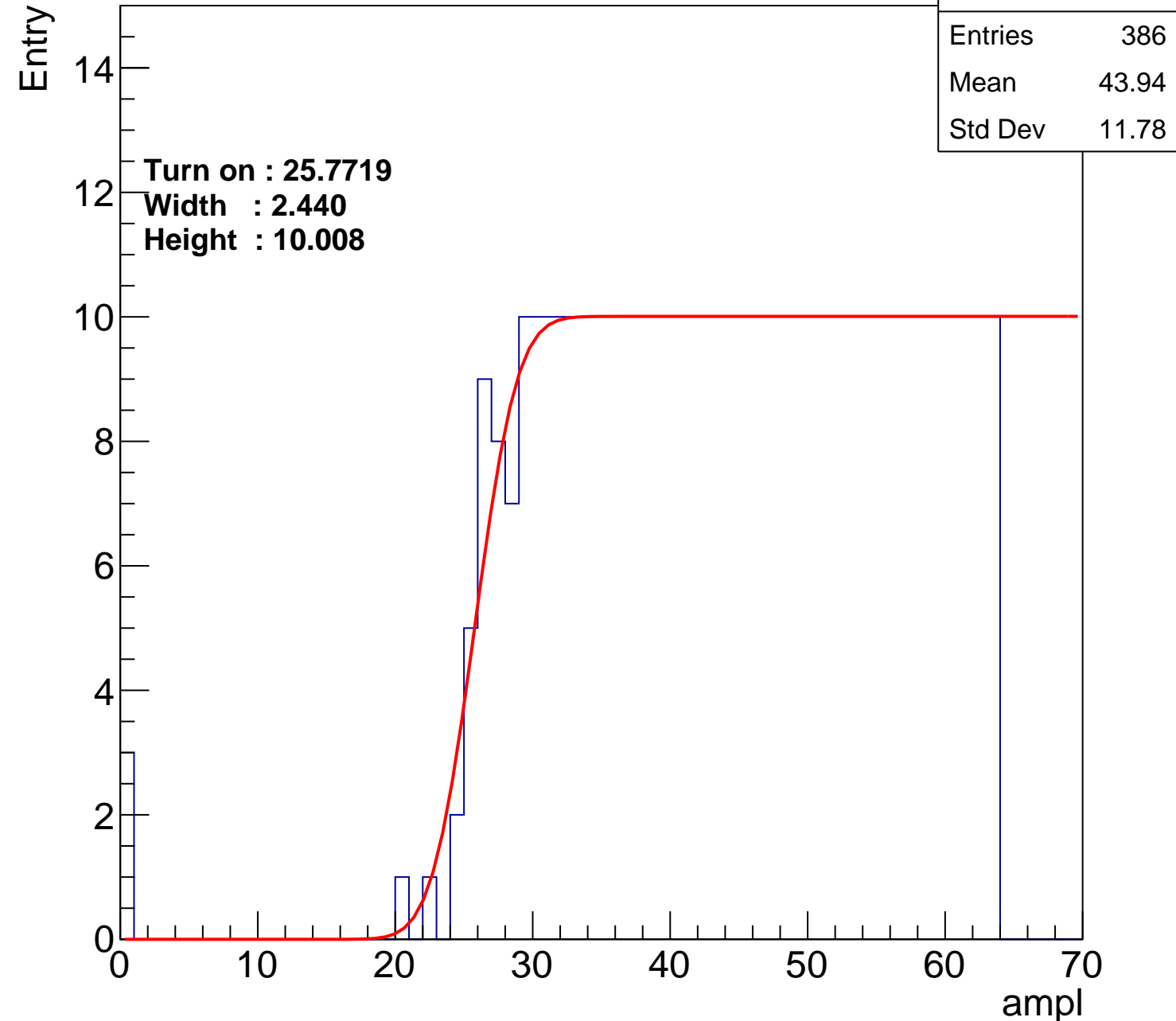
Width : 2.440

Height : 10.008

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch53

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	395
Mean	43.59
Std Dev	11.73

Turn on : 24.8131

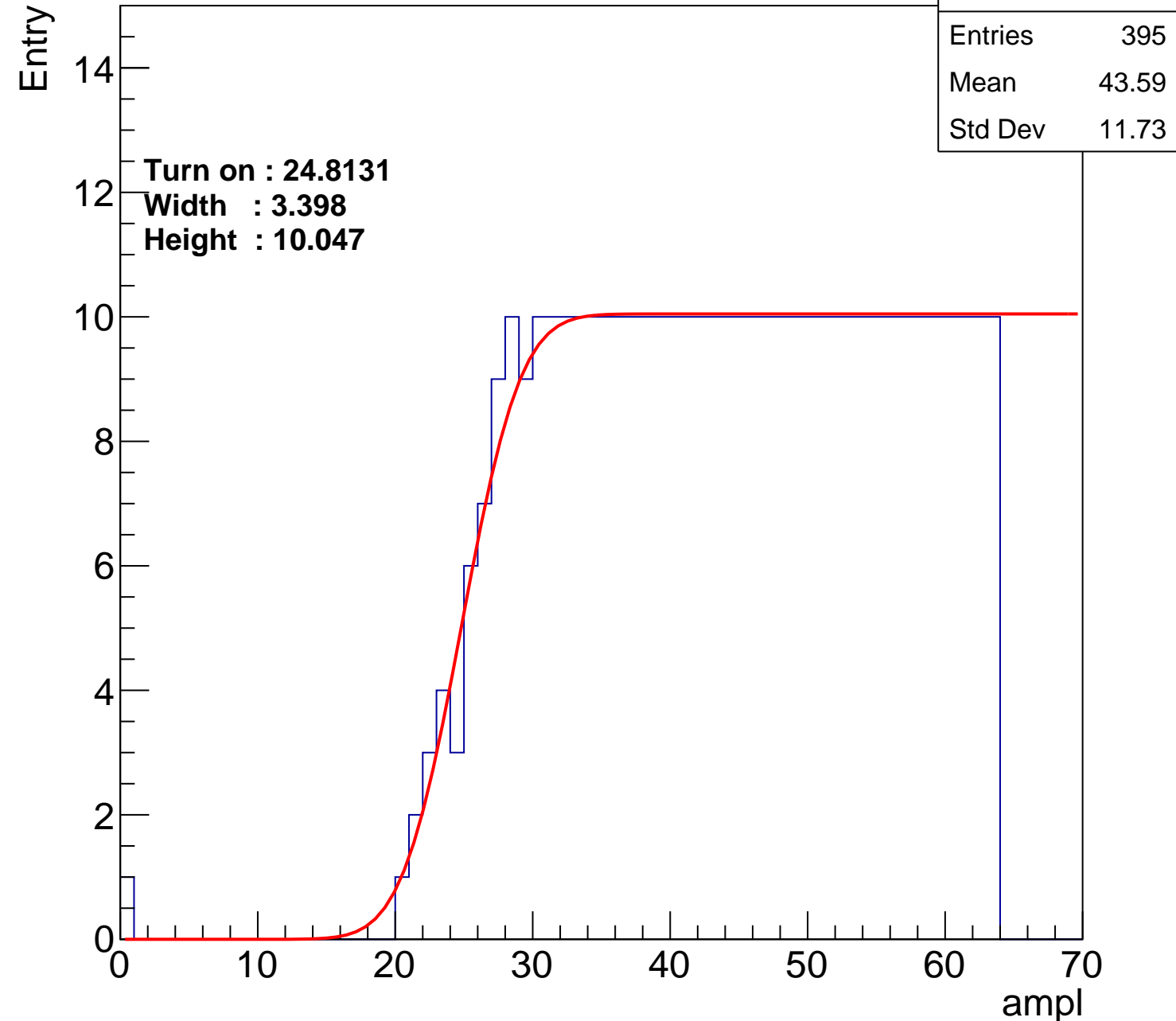
Width : 3.398

Height : 10.047

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch54

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	389
Mean	43.82
Std Dev	11.75

Turn on : 25.7174

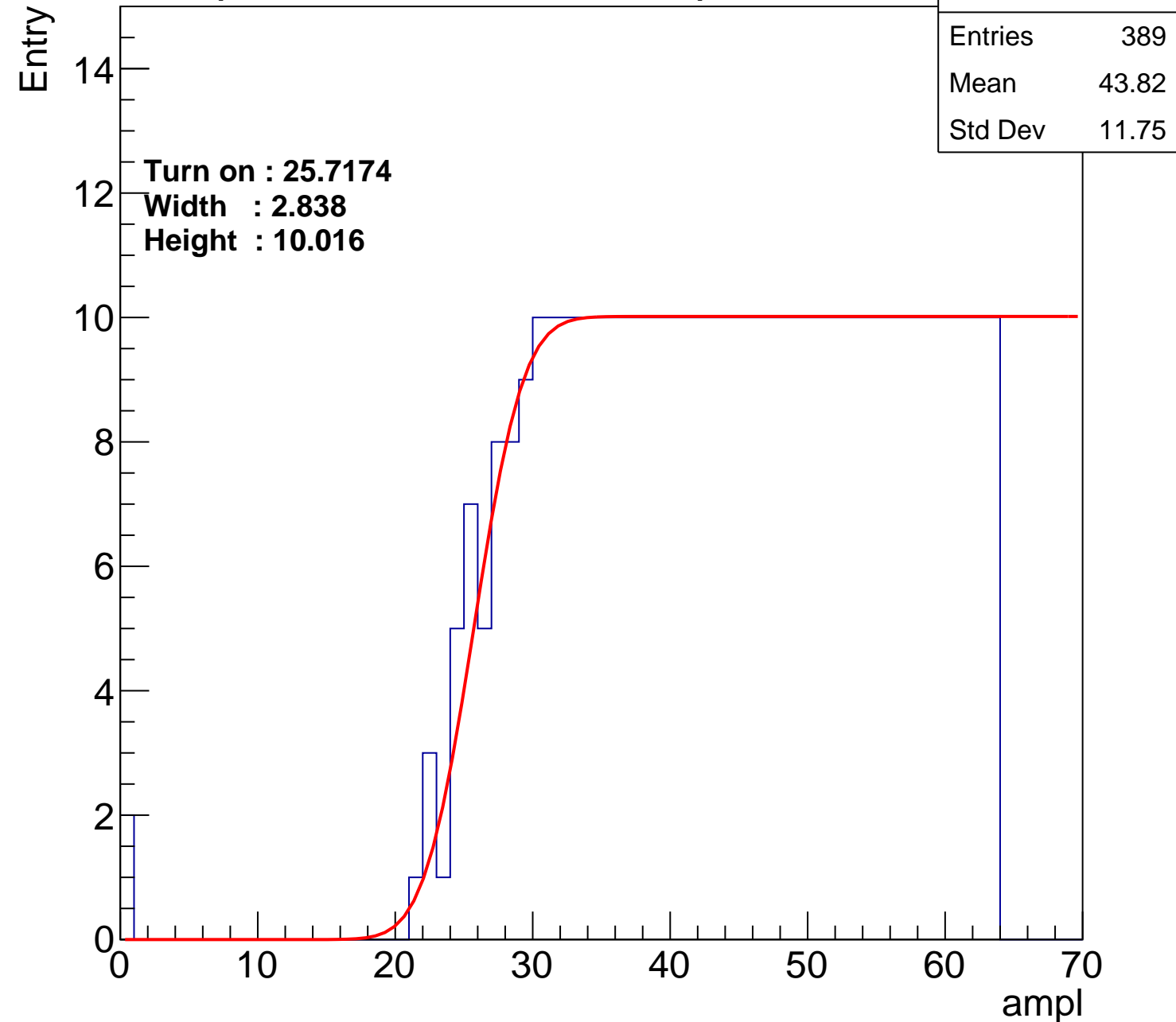
Width : 2.838

Height : 10.016

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L000S, U2-ch55

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	369
Mean	44.89
Std Dev	11.02

Turn on : 27.6759

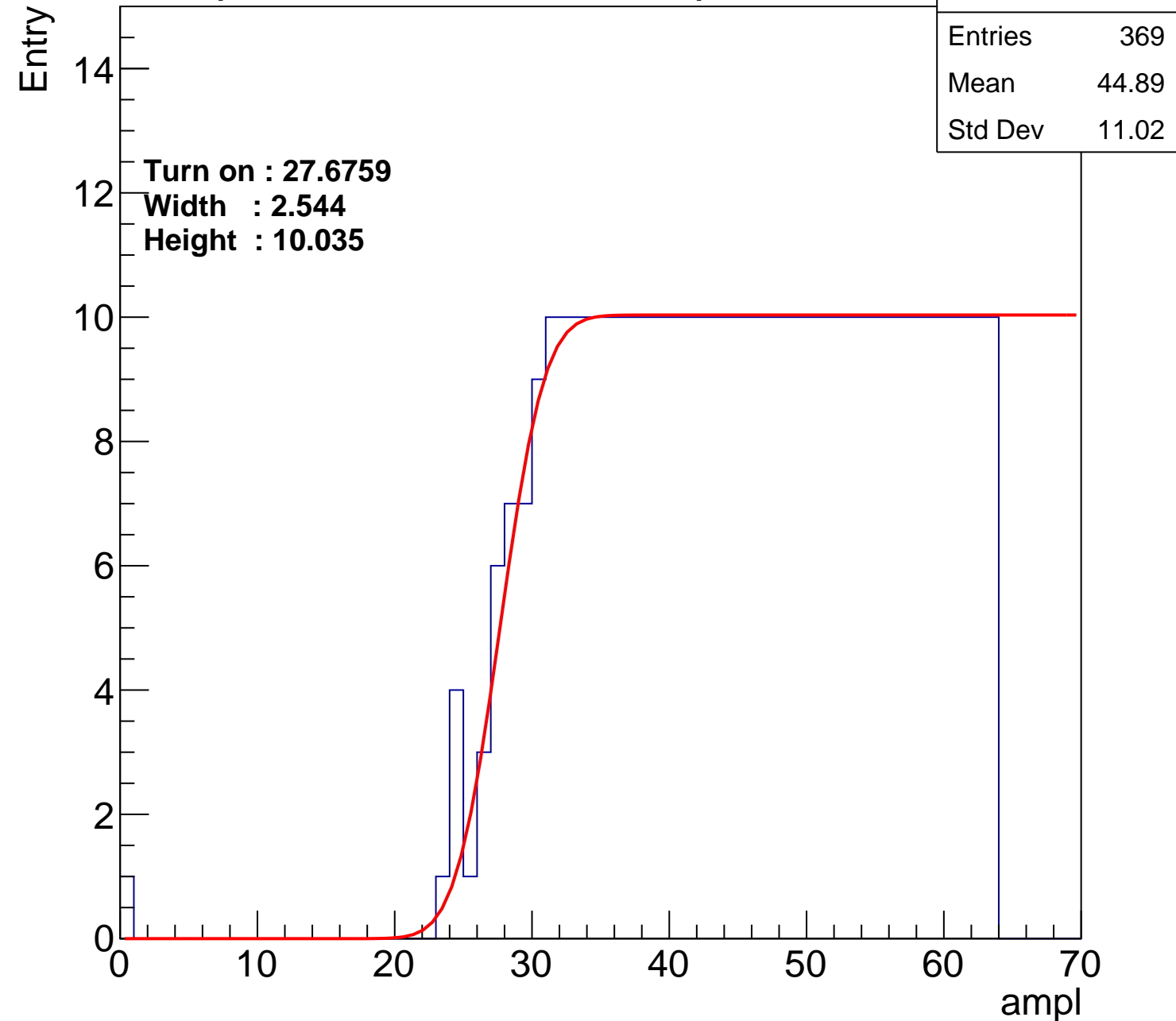
Width : 2.544

Height : 10.035

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch56

calib\_packv5\_042523\_0143.root, FC#3, port B3

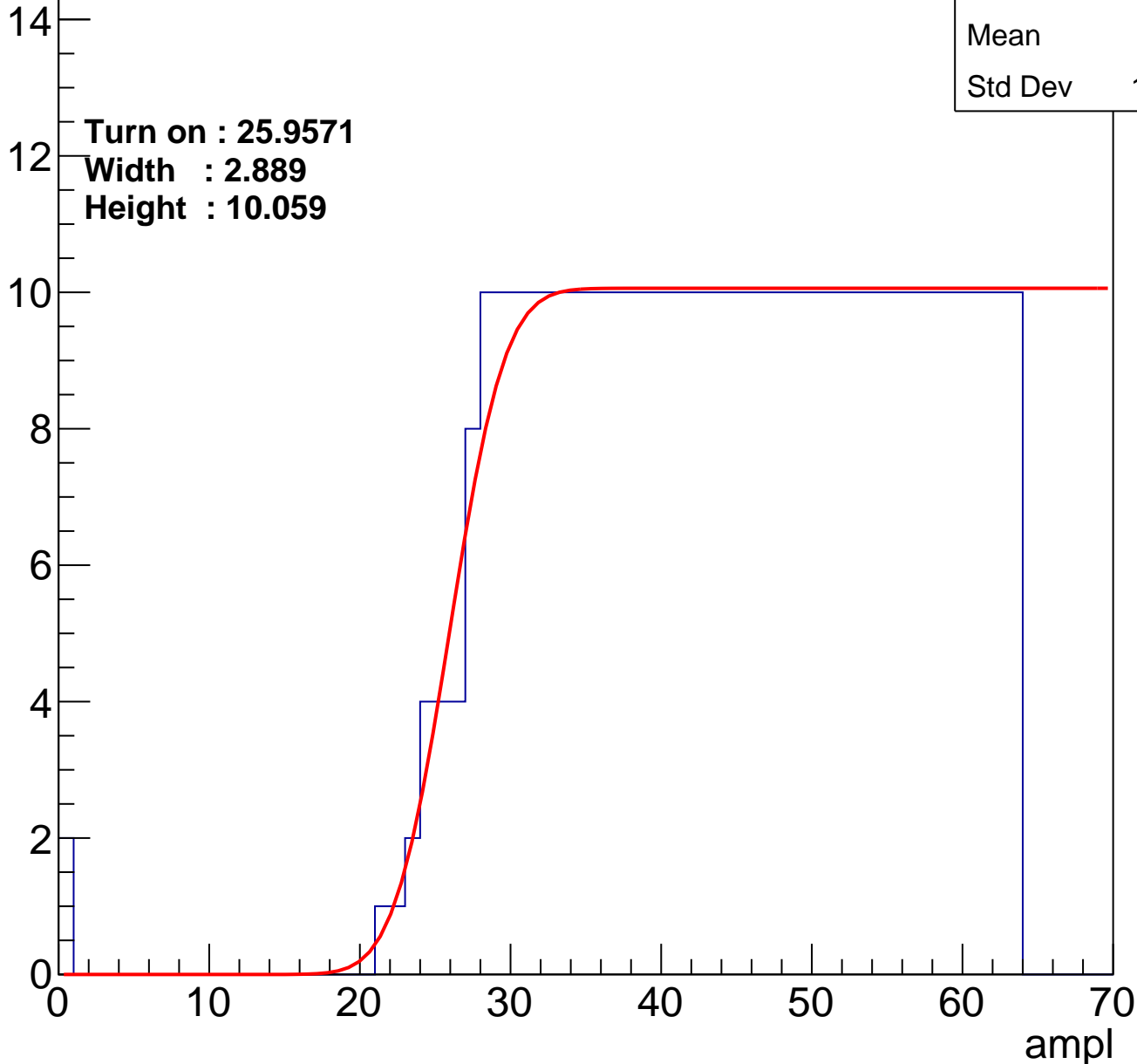
Entries	386
Mean	44
Std Dev	11.62

Turn on : 25.9571

Width : 2.889

Height : 10.059

Entry



# B1L000S, U2-ch57

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	397
Mean	43.54
Std Dev	11.71

Turn on : 24.4561

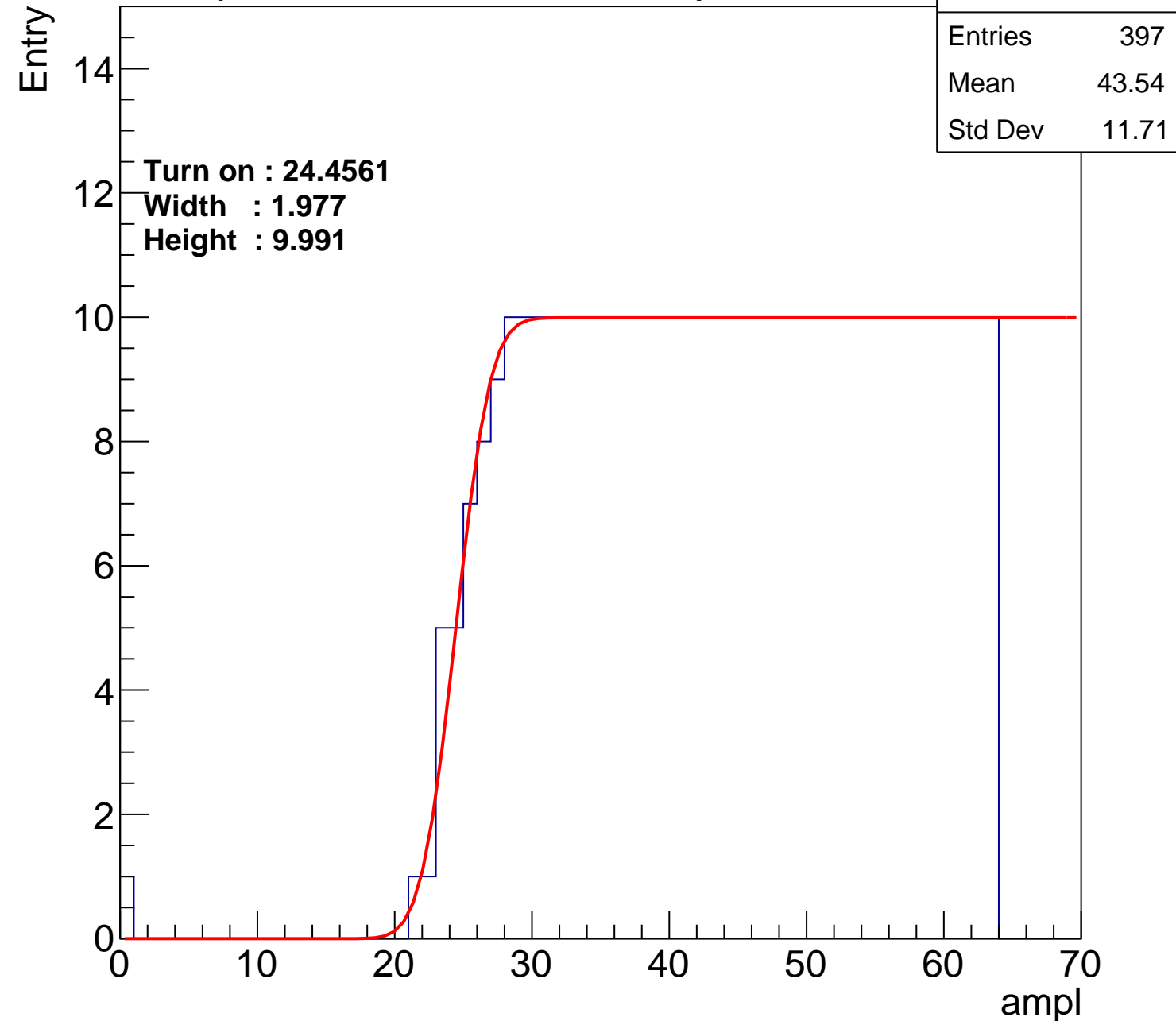
Width : 1.977

Height : 9.991

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch58

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	378
Mean	44.35
Std Dev	11.57

**Turn on : 26.8056**

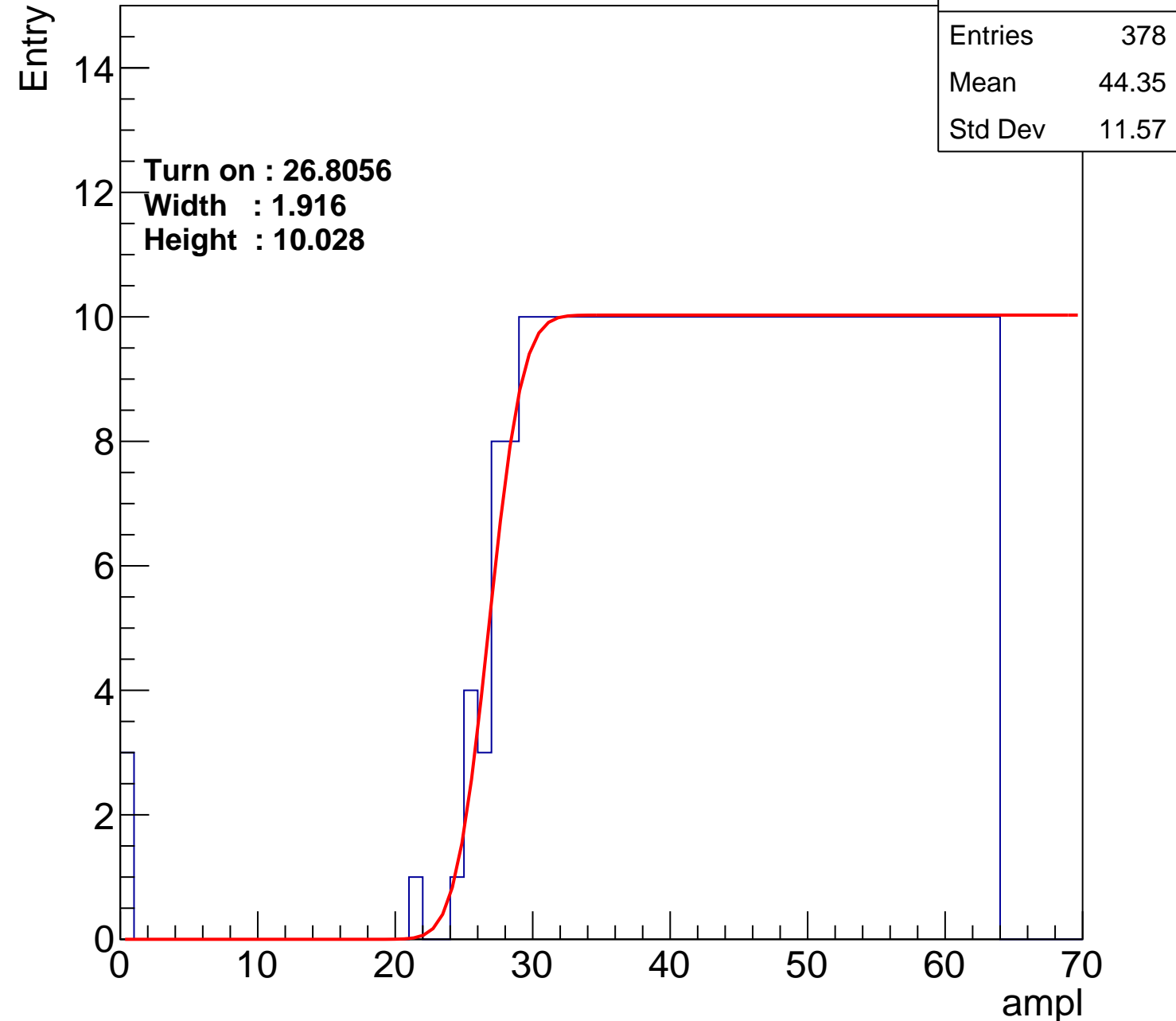
**Width : 1.916**

**Height : 10.028**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch59

calib\_packv5\_042523\_0143.root, FC#3, port B3

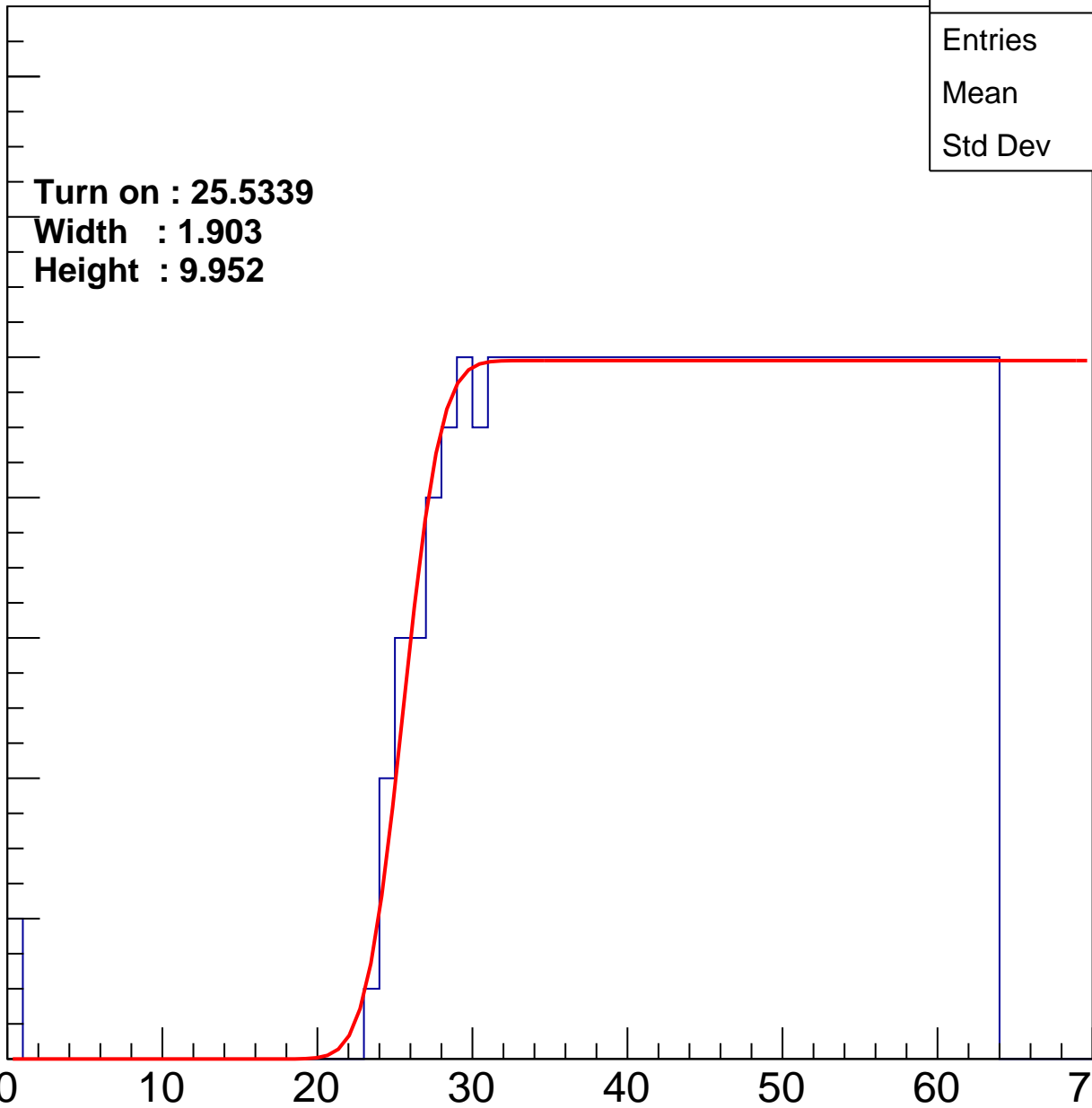
Entry

14  
12  
10  
8  
6  
4  
2  
0

Turn on : 25.5339  
Width : 1.903  
Height : 9.952

Entries	385
Mean	44.06
Std Dev	11.57

ampl



# B1L000S, U2-ch60

calib\_packv5\_042523\_0143.root, FC#3, port B3

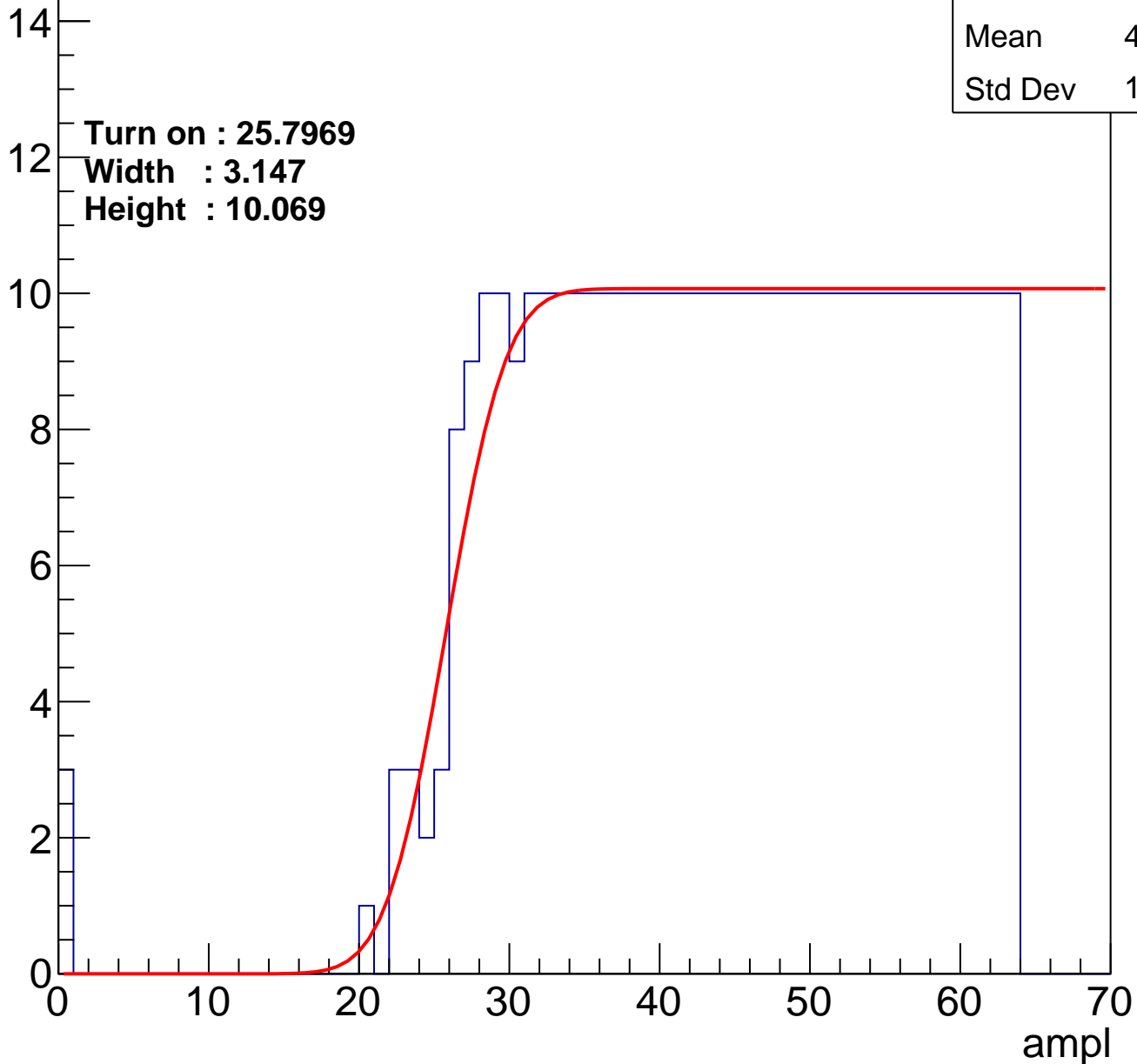
Entries	391
Mean	43.68
Std Dev	11.93

**Turn on : 25.7969**

**Width : 3.147**

**Height : 10.069**

Entry



# B1L000S, U2-ch61

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	387
Mean	44
Std Dev	11.49

Turn on : 25.4933

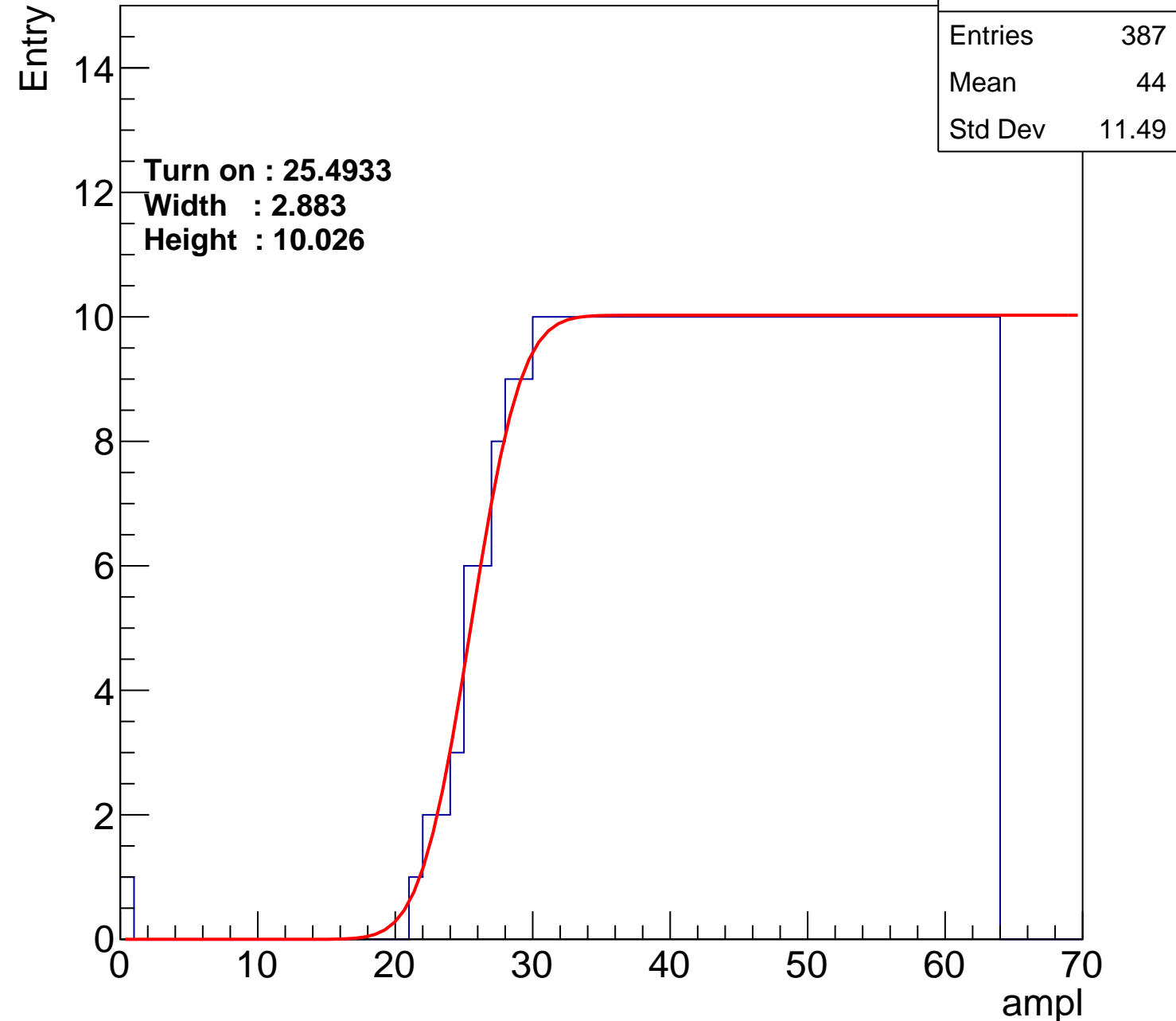
Width : 2.883

Height : 10.026

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch62

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	388
Mean	43.84
Std Dev	11.84

Turn on : 26.0518

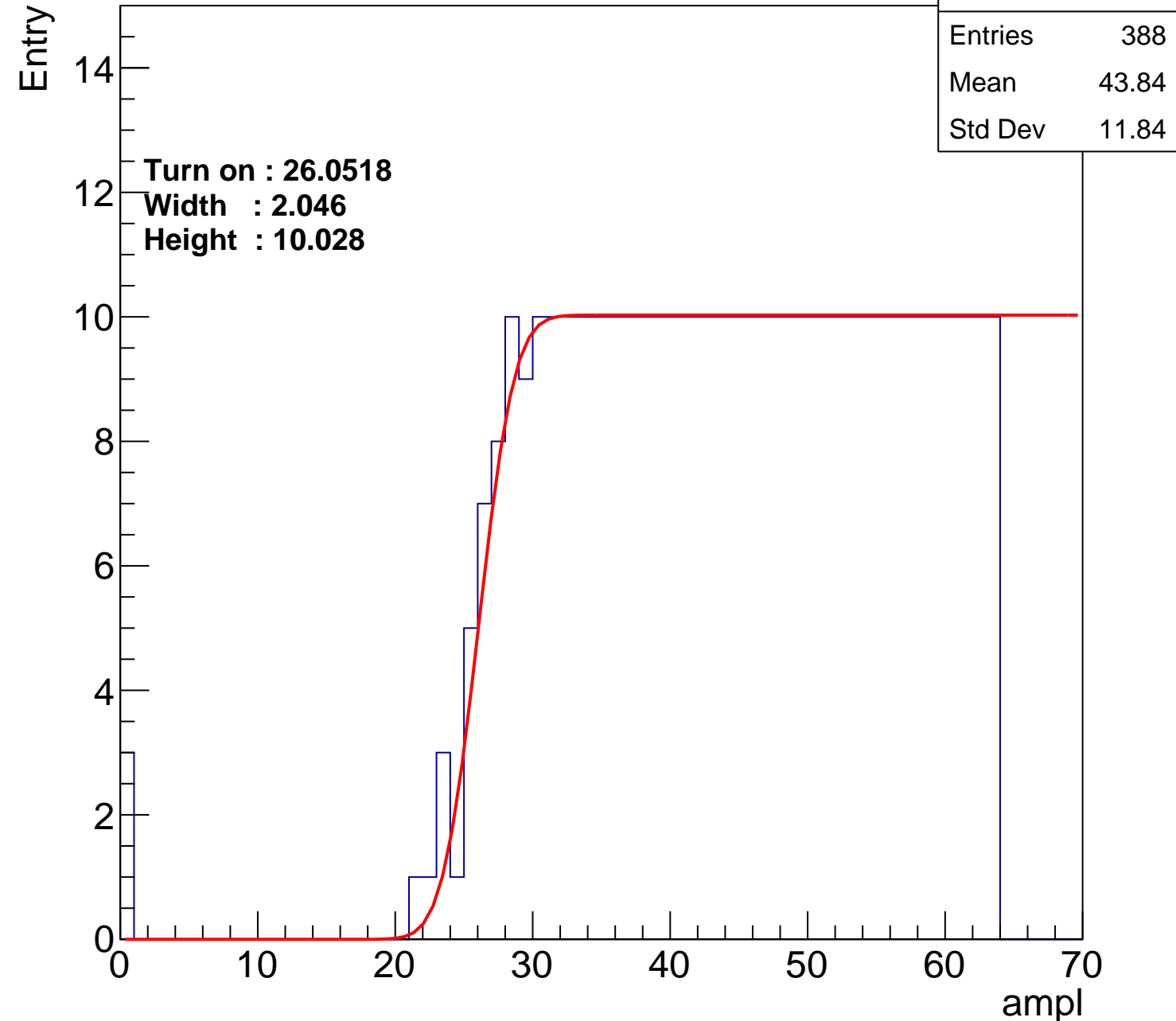
Width : 2.046

Height : 10.028

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L000S, U2-ch63

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	381
Mean	44.13
Std Dev	11.74

Turn on : 26.5794

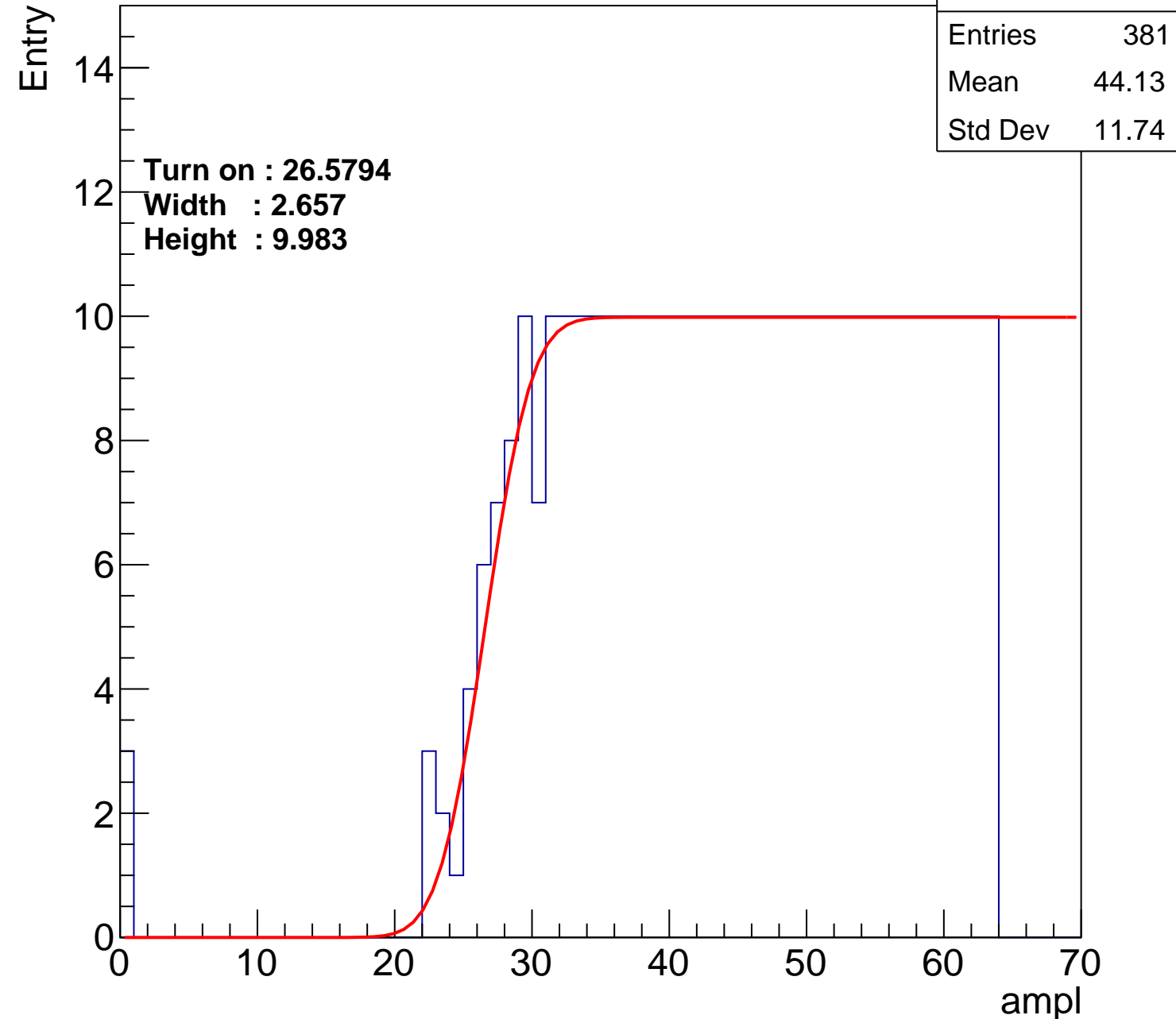
Width : 2.657

Height : 9.983

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch64

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	397
Mean	43.51
Std Dev	11.75

Turn on : 25.0571

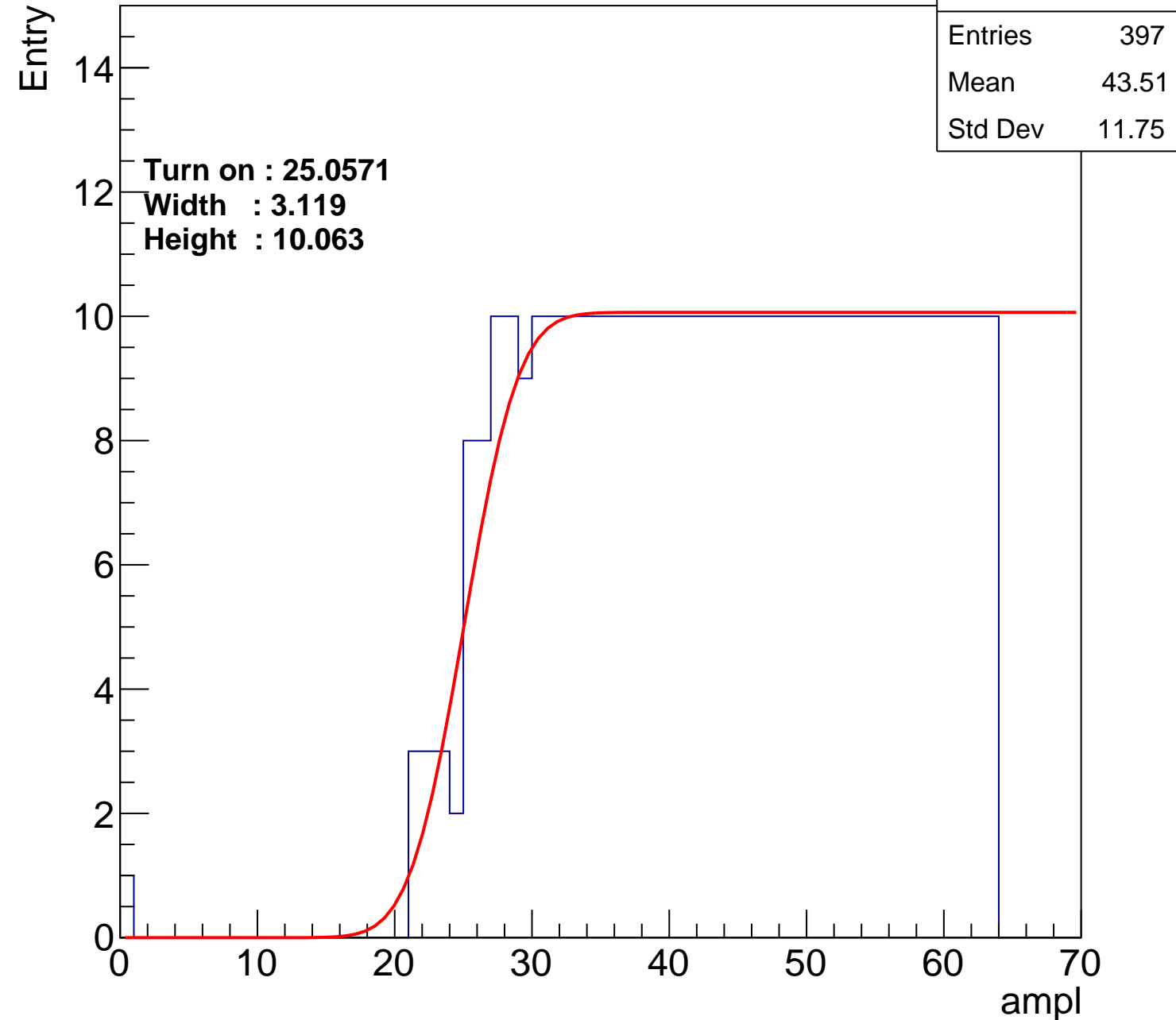
Width : 3.119

Height : 10.063

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch65

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	396
Mean	43.49
Std Dev	11.9

Turn on : 24.6890

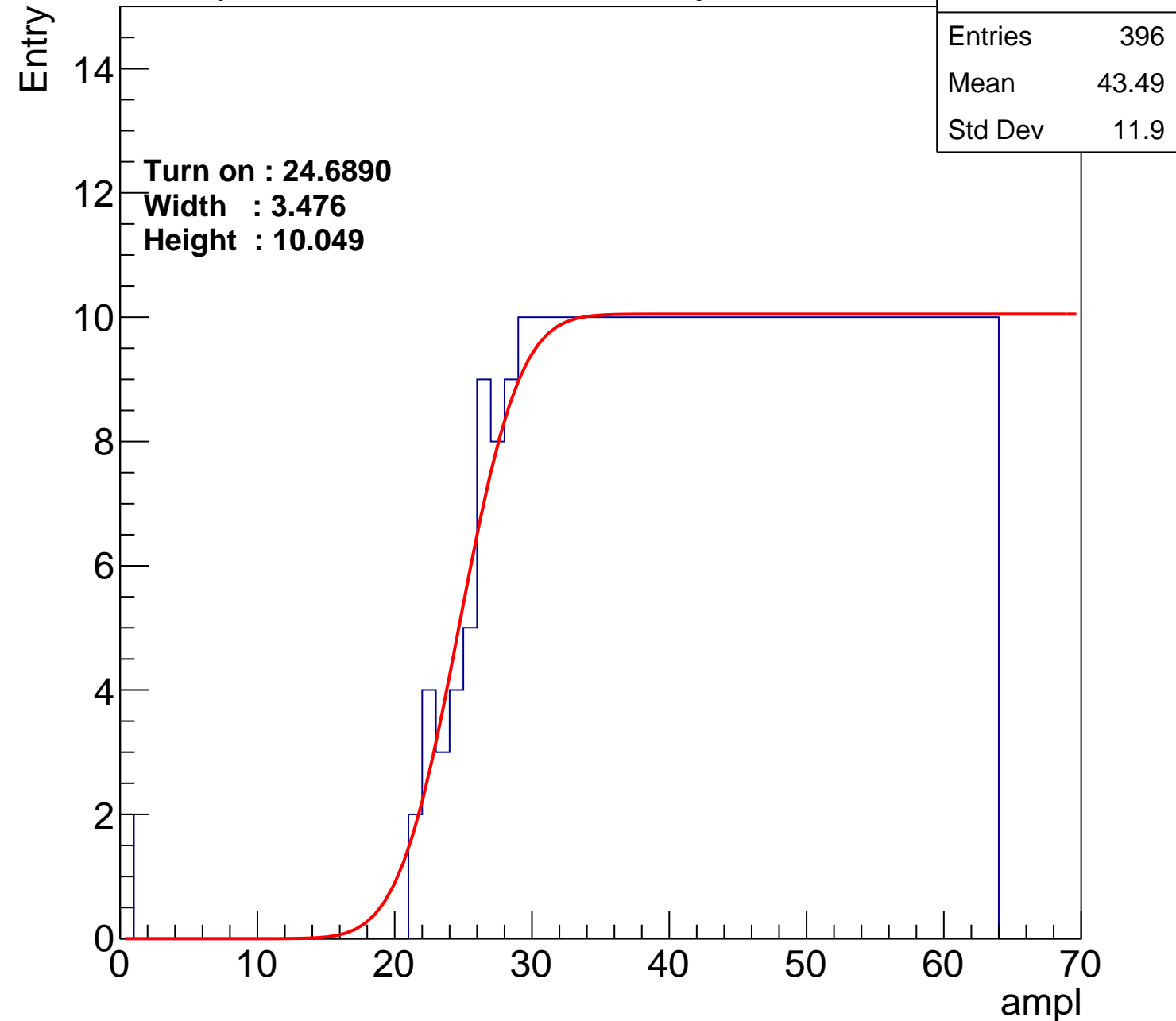
Width : 3.476

Height : 10.049

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch66

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	384
Mean	44.03
Std Dev	11.74

**Turn on : 26.0280**

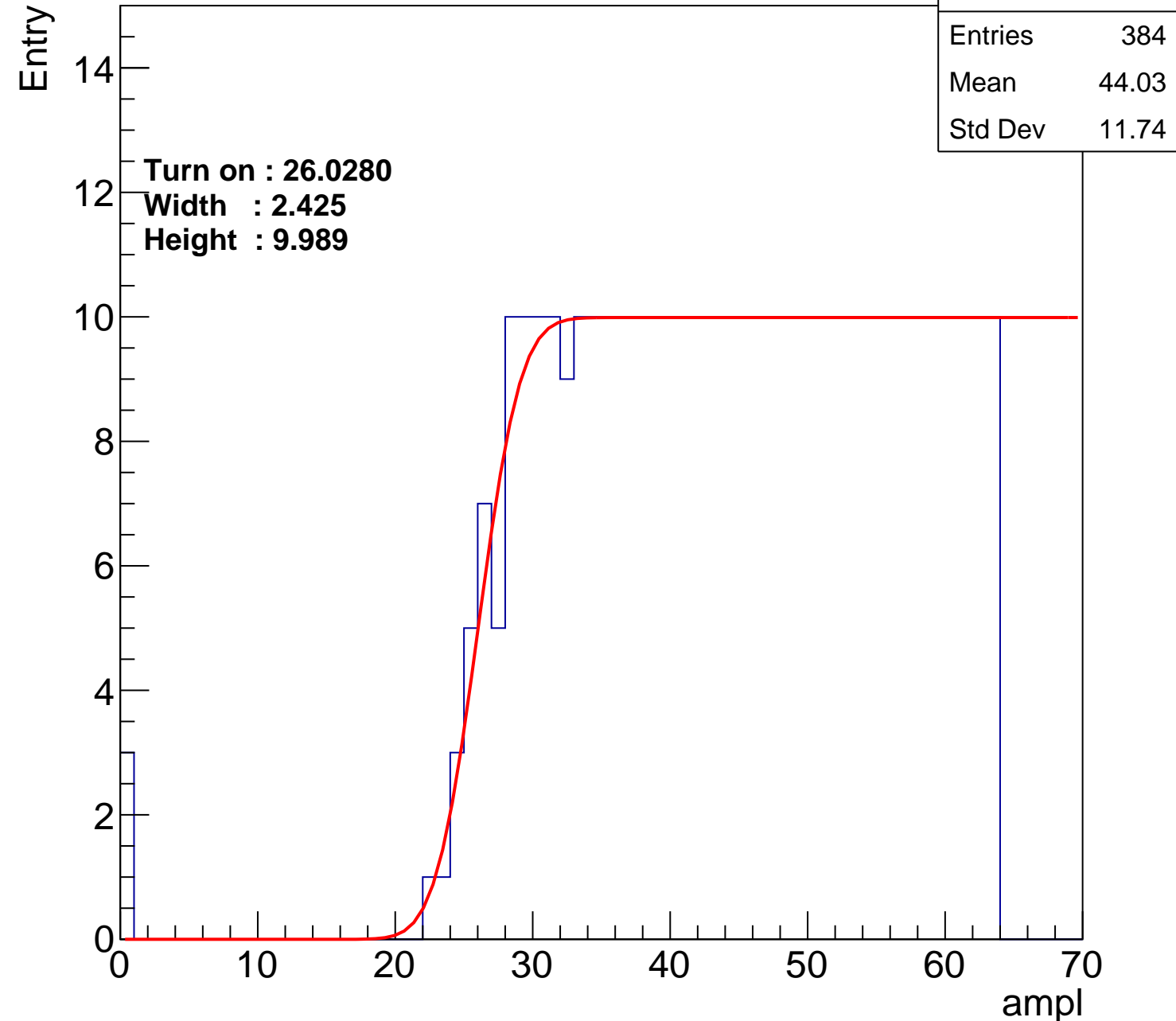
**Width : 2.425**

**Height : 9.989**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch67

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	392
Mean	43.56
Std Dev	12.13

Turn on : 25.3264

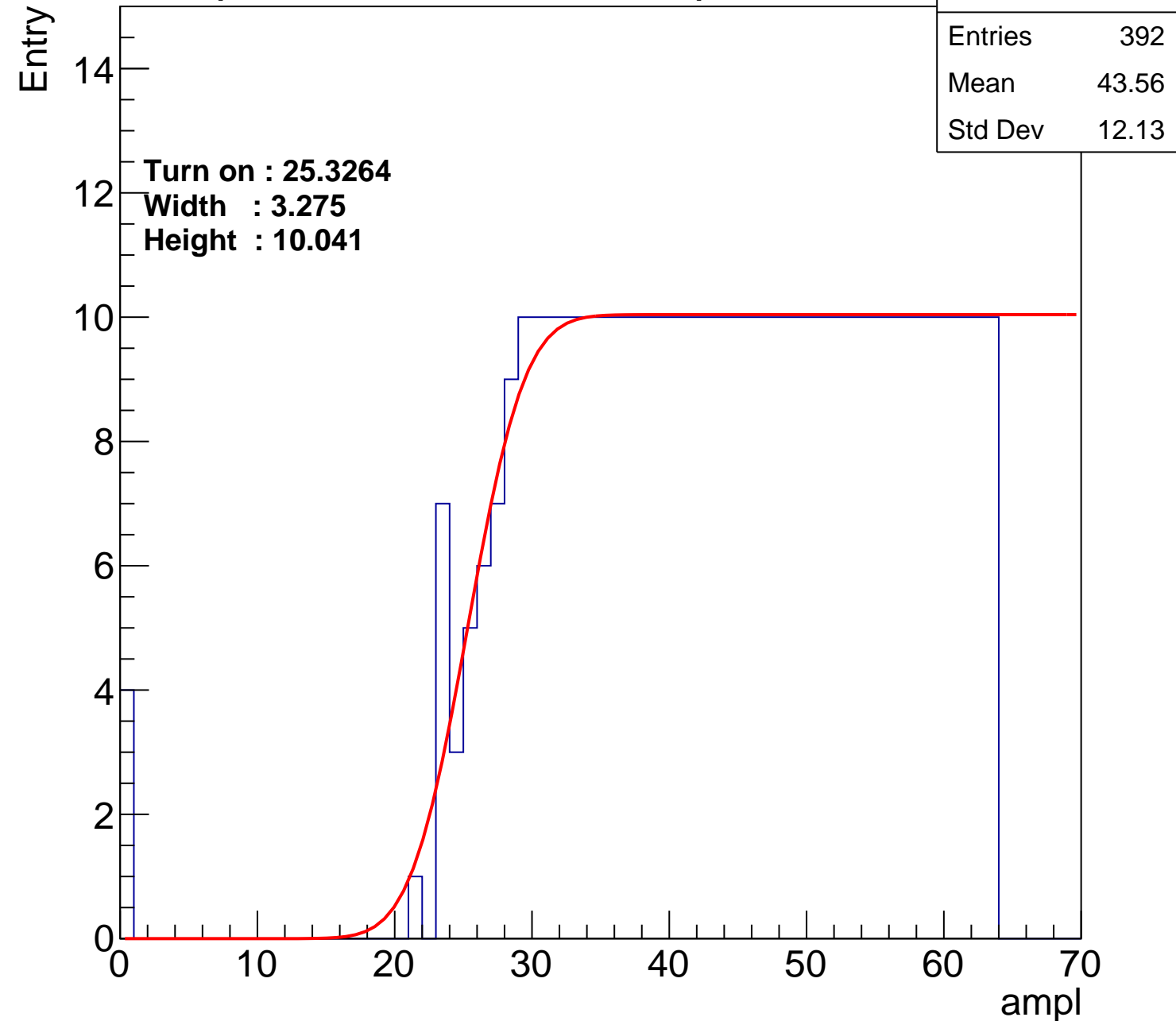
Width : 3.275

Height : 10.041

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch68

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	388
Mean	43.94
Std Dev	11.53

**Turn on : 25.5848**

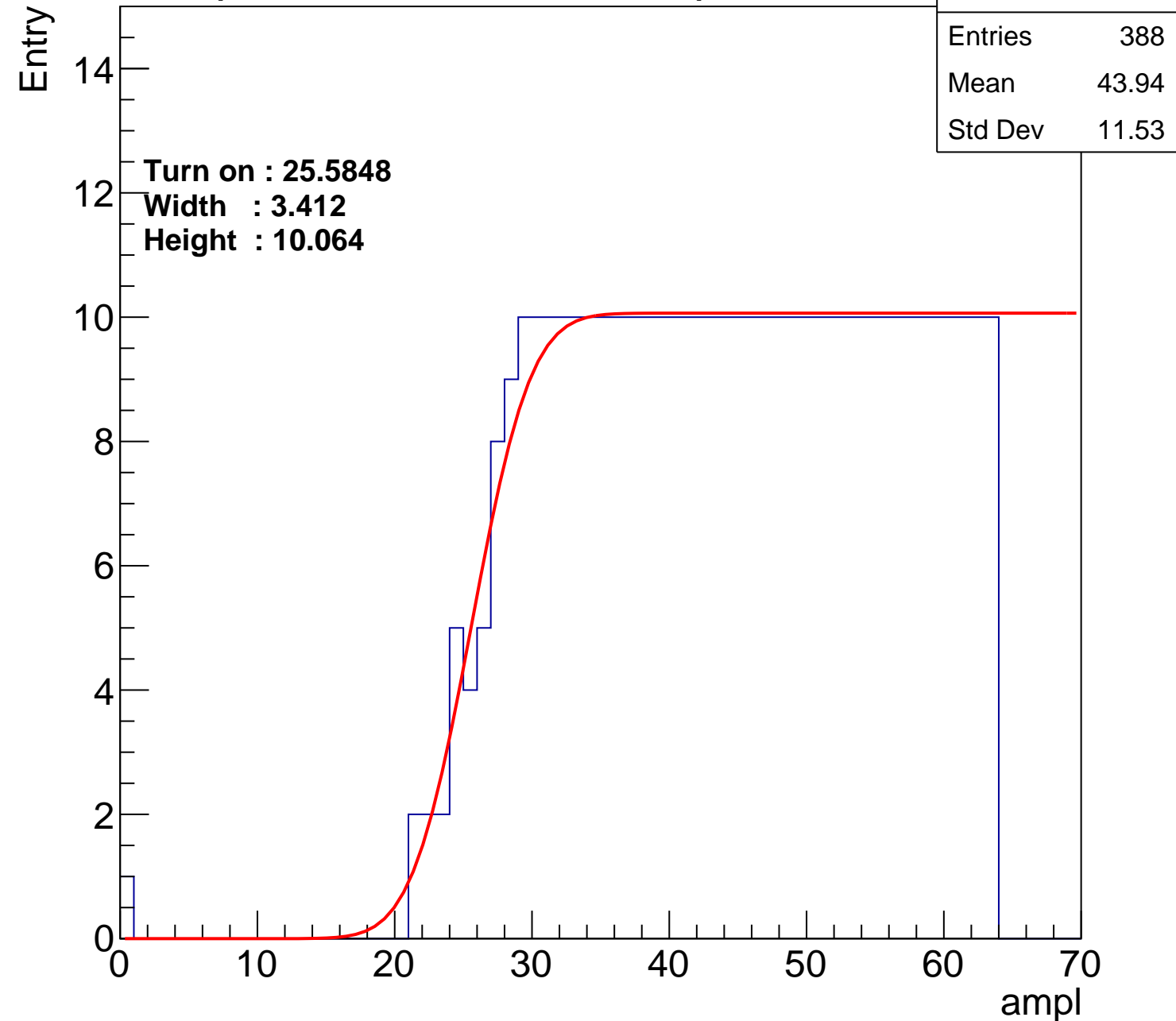
**Width : 3.412**

**Height : 10.064**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch69

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	411
Mean	42.84
Std Dev	12.11

Turn on : 23.3366

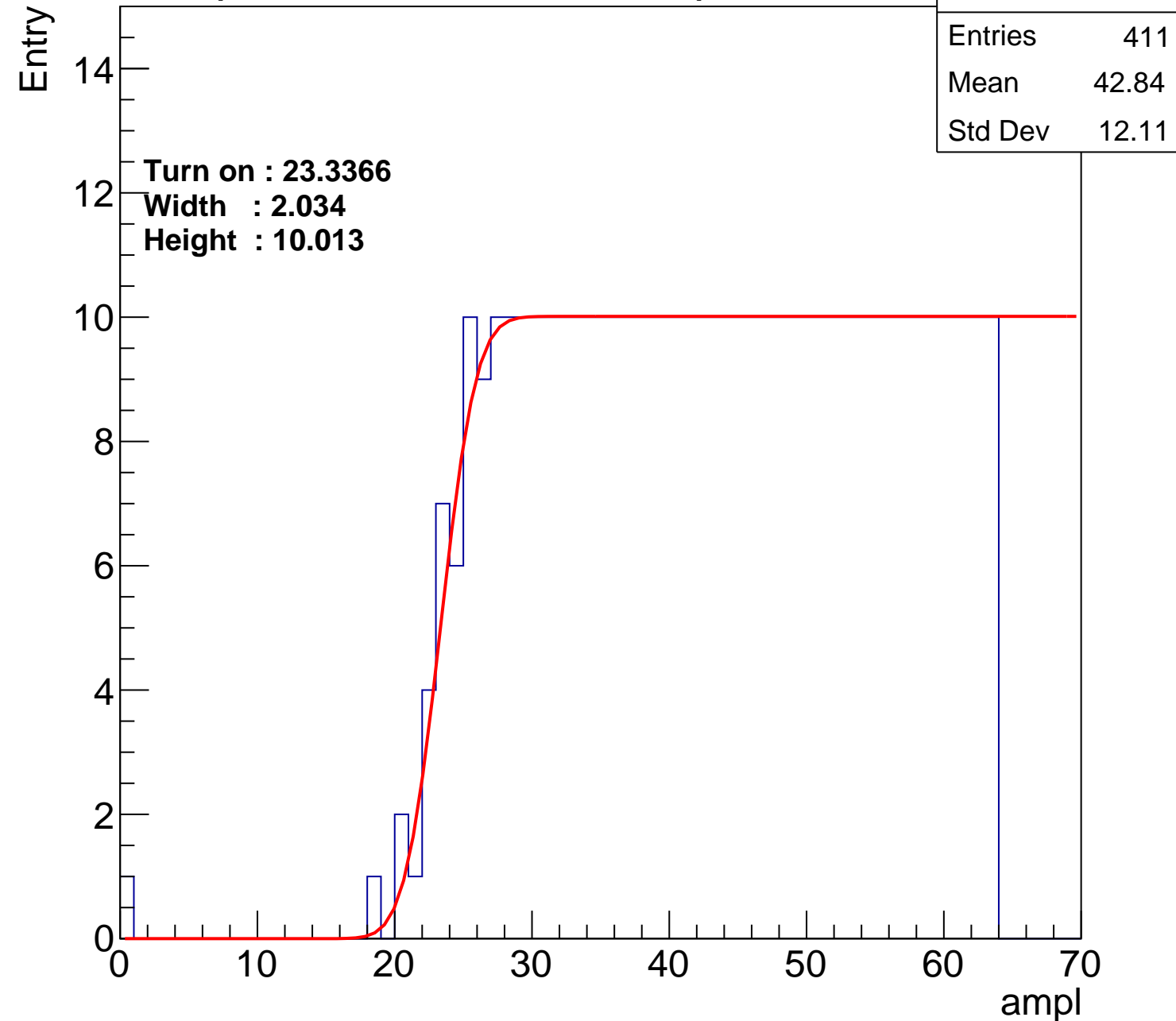
Width : 2.034

Height : 10.013

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch70

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	392
Mean	43.64
Std Dev	11.94

**Turn on : 25.4299**

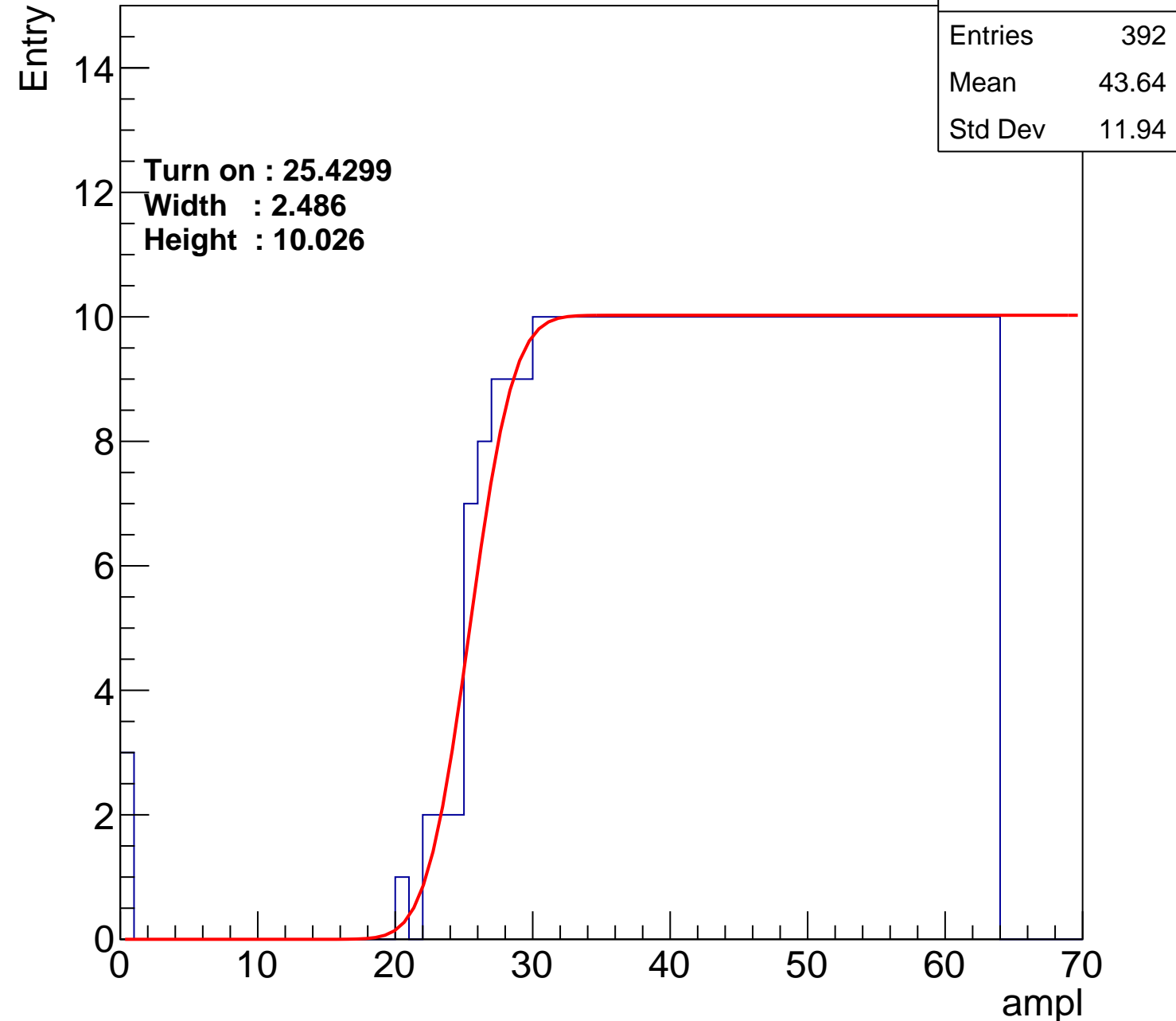
**Width : 2.486**

**Height : 10.026**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L000S, U2-ch71

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	383
Mean	43.89
Std Dev	12.22

**Turn on : 26.6903**

**Width : 2.466**

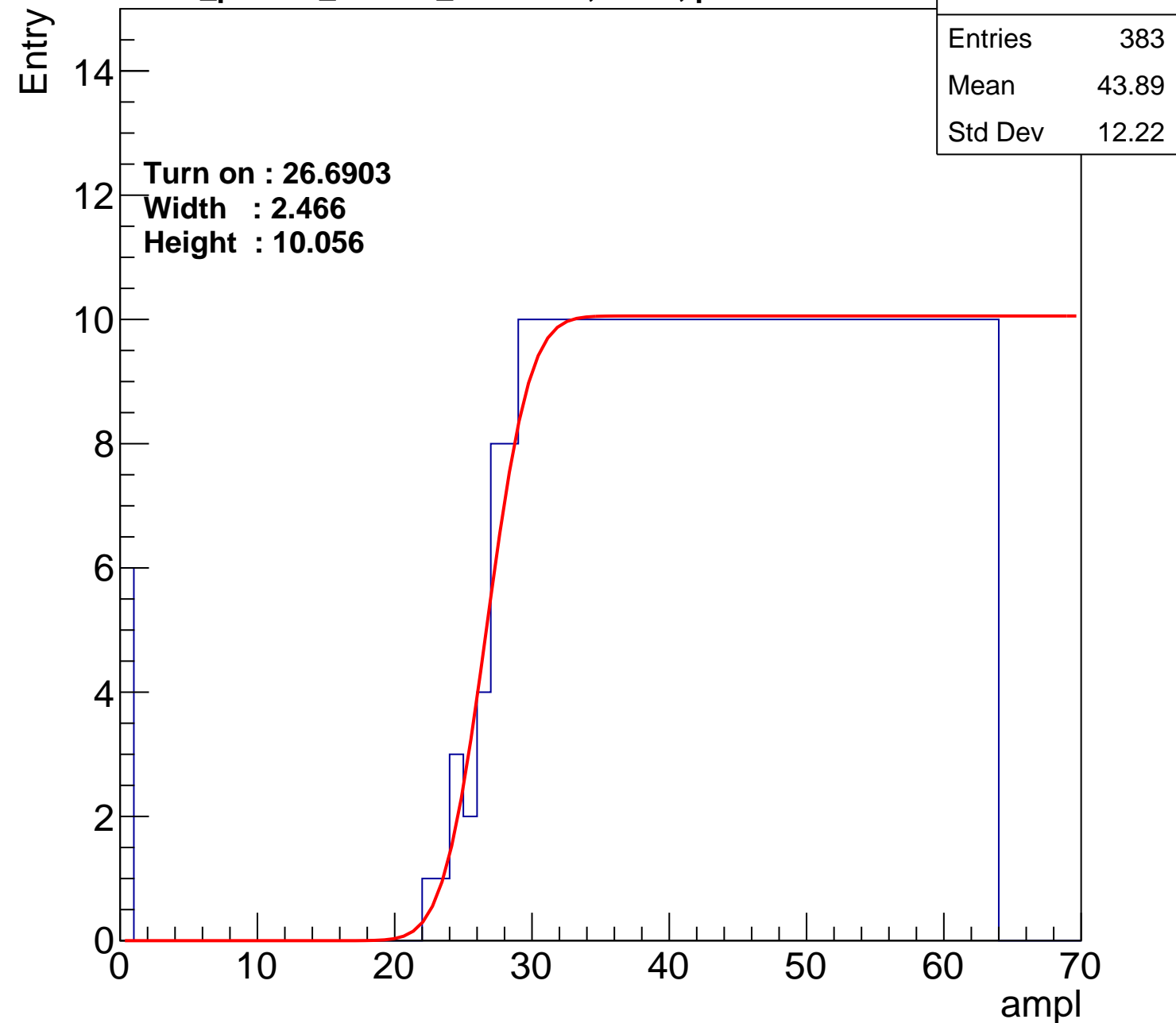
**Height : 10.056**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L000S, U2-ch72

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	390
Mean	43.57
Std Dev	12.29

**Turn on : 26.0728**

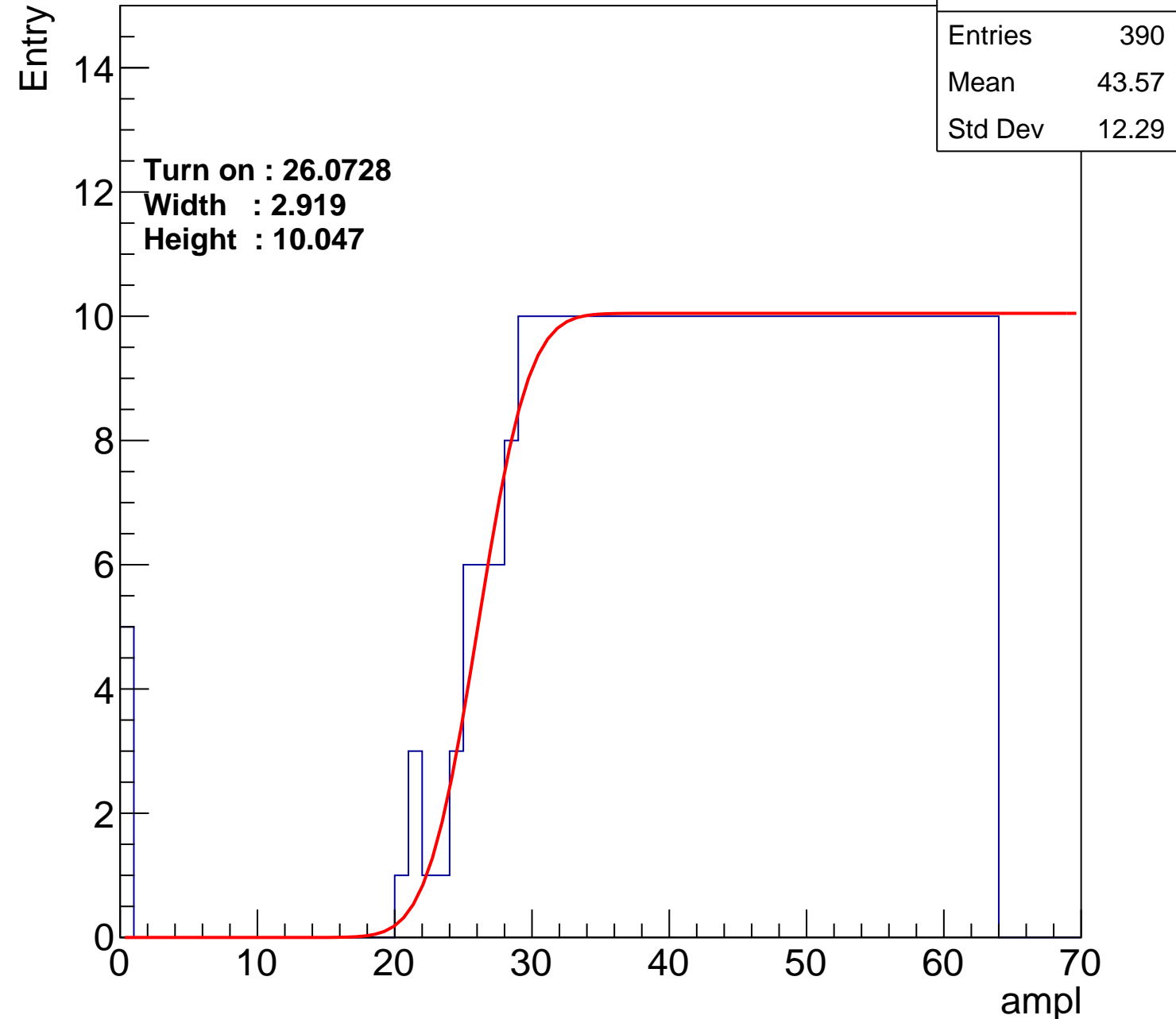
**Width : 2.919**

**Height : 10.047**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch73

calib\_packv5\_042523\_0143.root, FC#3, port B3

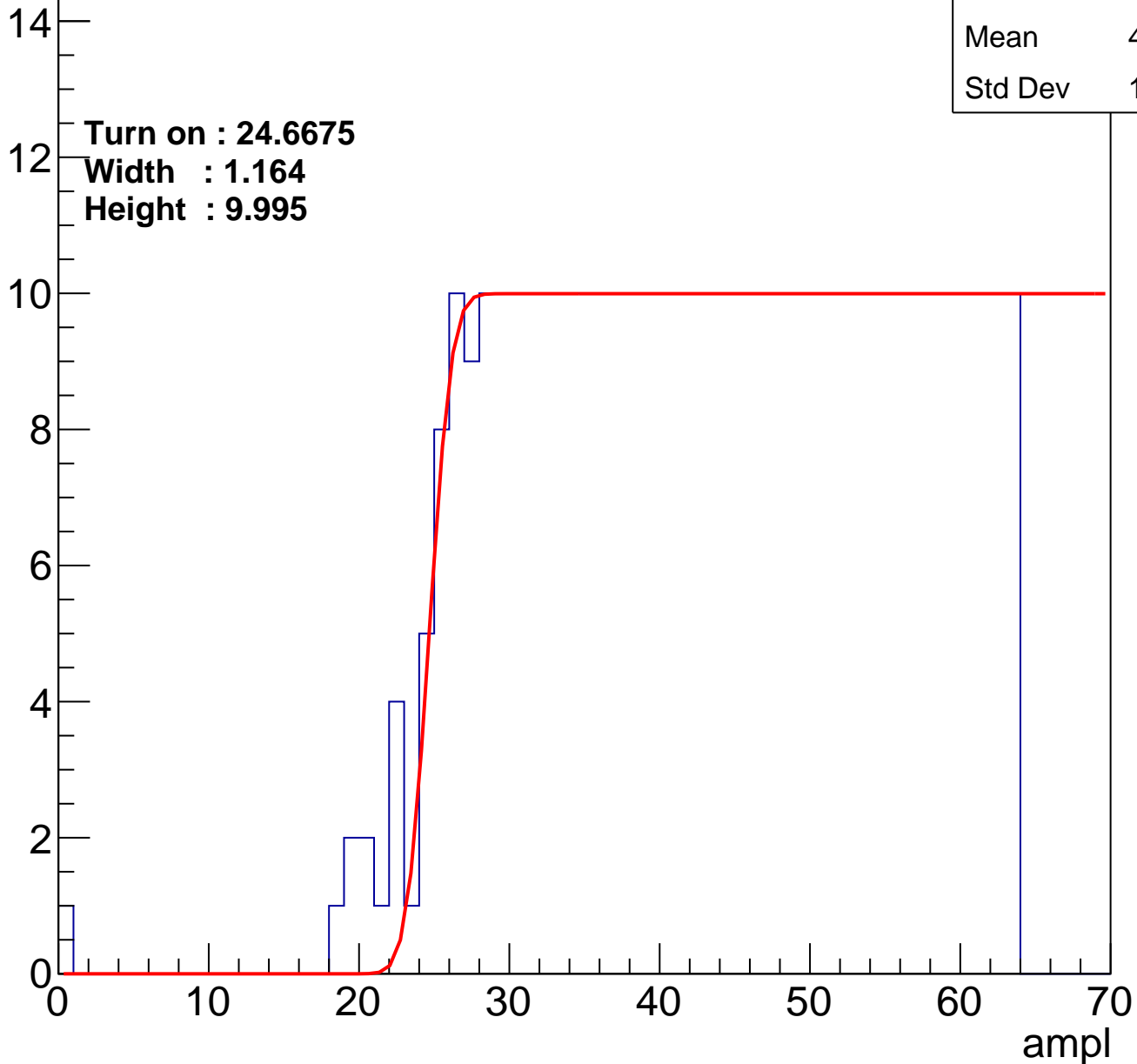
Entries	404
Mean	43.15
Std Dev	11.98

Turn on : 24.6675

Width : 1.164

Height : 9.995

Entry



# B1L000S, U2-ch74

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	370
Mean	44.83
Std Dev	11.05

Turn on : 27.5079

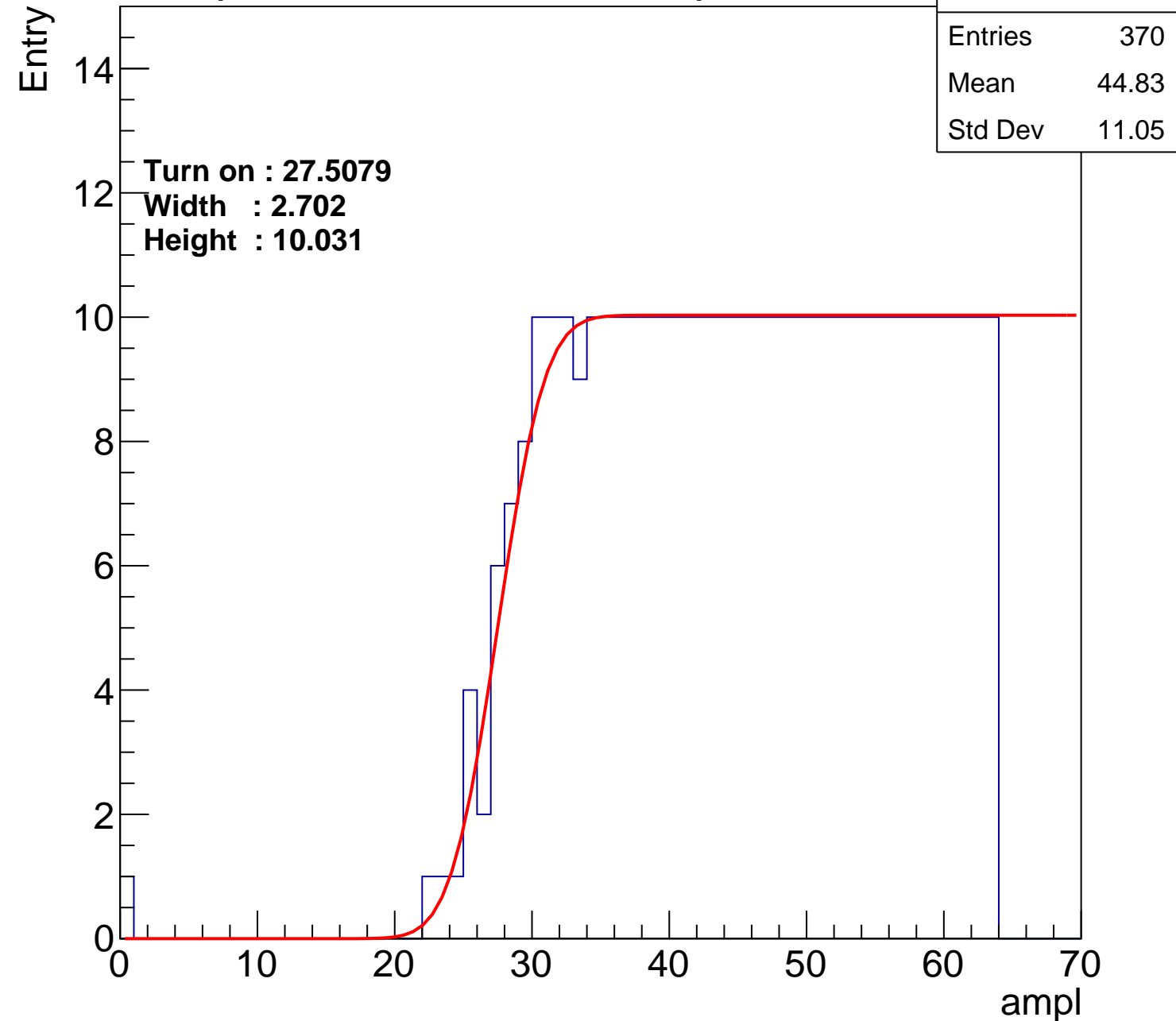
Width : 2.702

Height : 10.031

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch75

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	381
Mean	44.04
Std Dev	11.96

**Turn on : 26.1578**

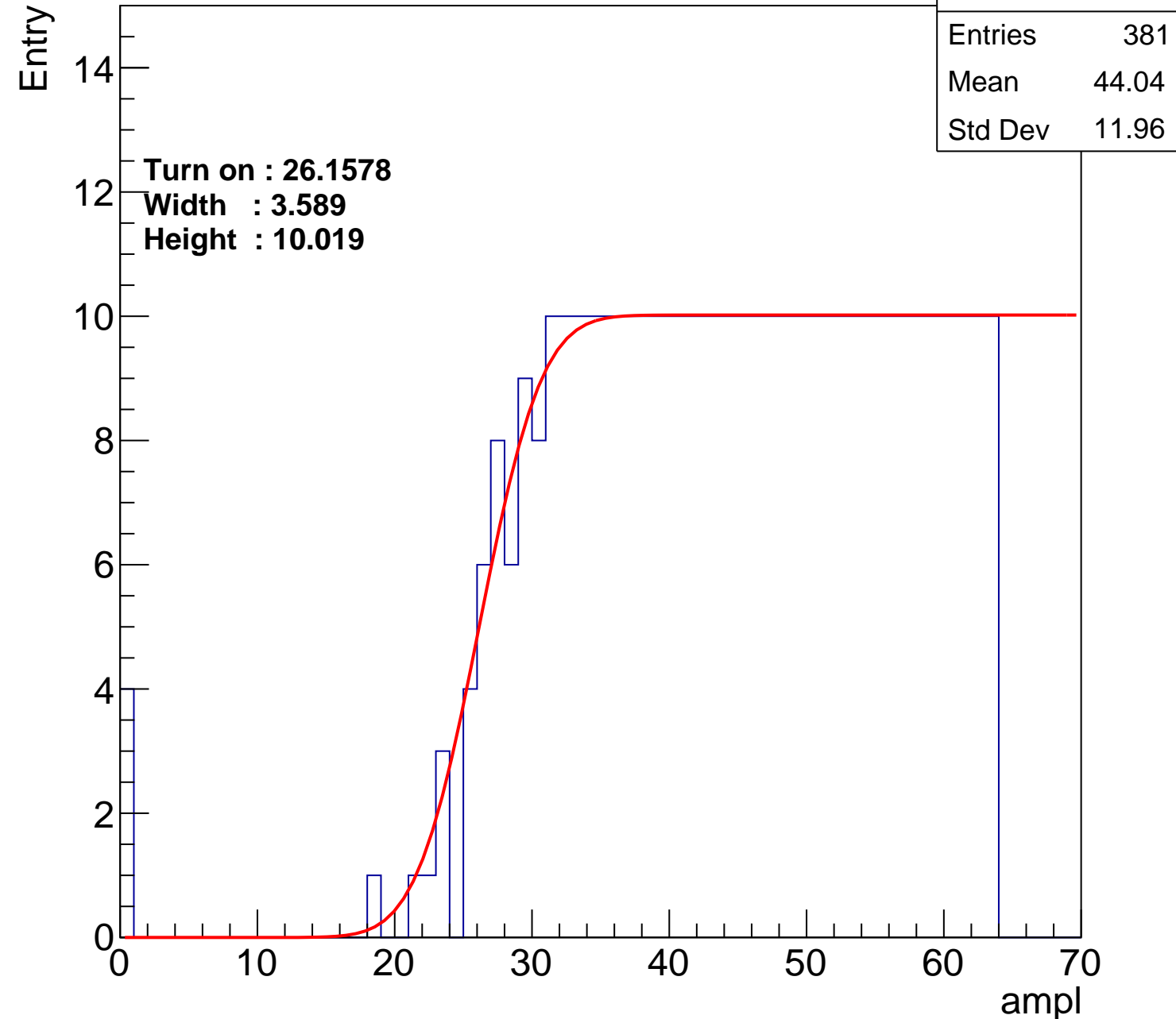
**Width : 3.589**

**Height : 10.019**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch76

calib\_packv5\_042523\_0143.root, FC#3, port B3

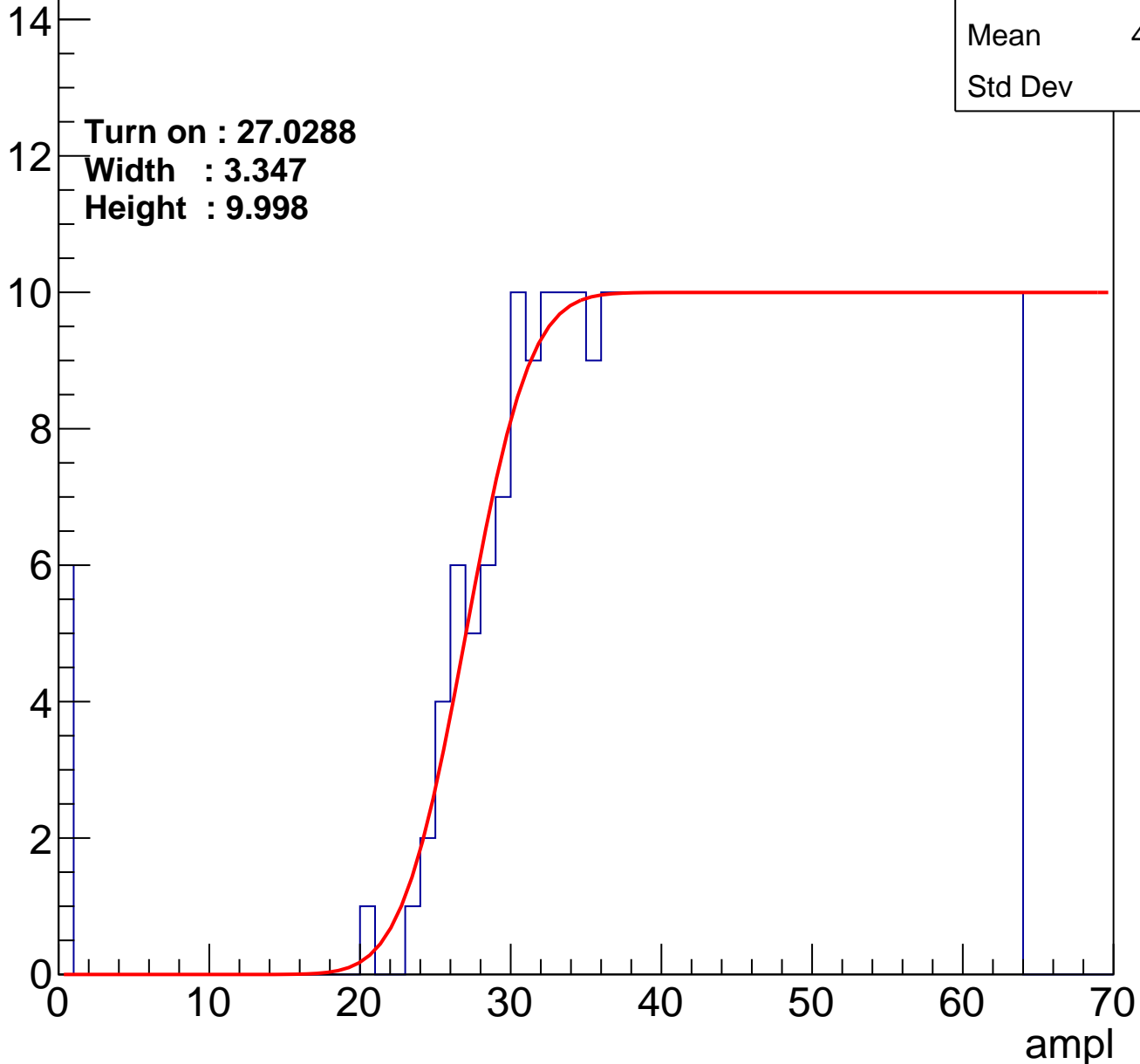
Entries	376
Mean	44.14
Std Dev	12.2

Turn on : 27.0288

Width : 3.347

Height : 9.998

Entry



# B1L000S, U2-ch77

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	387
Mean	43.95
Std Dev	11.64

Turn on : 25.6515

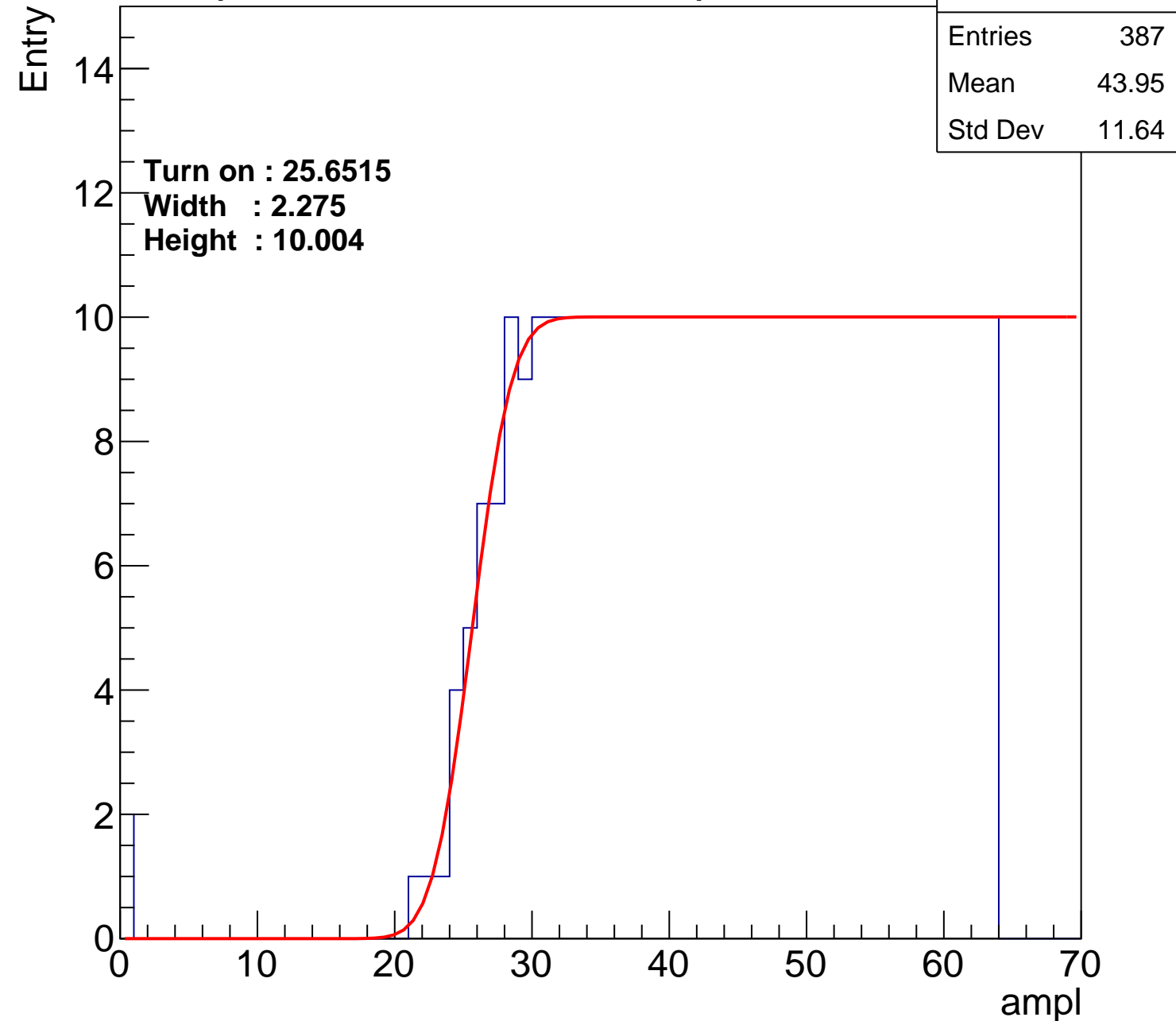
Width : 2.275

Height : 10.004

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch78

**calib\_packv5\_042523\_0143.root, FC#3, port B3**

Entries	389
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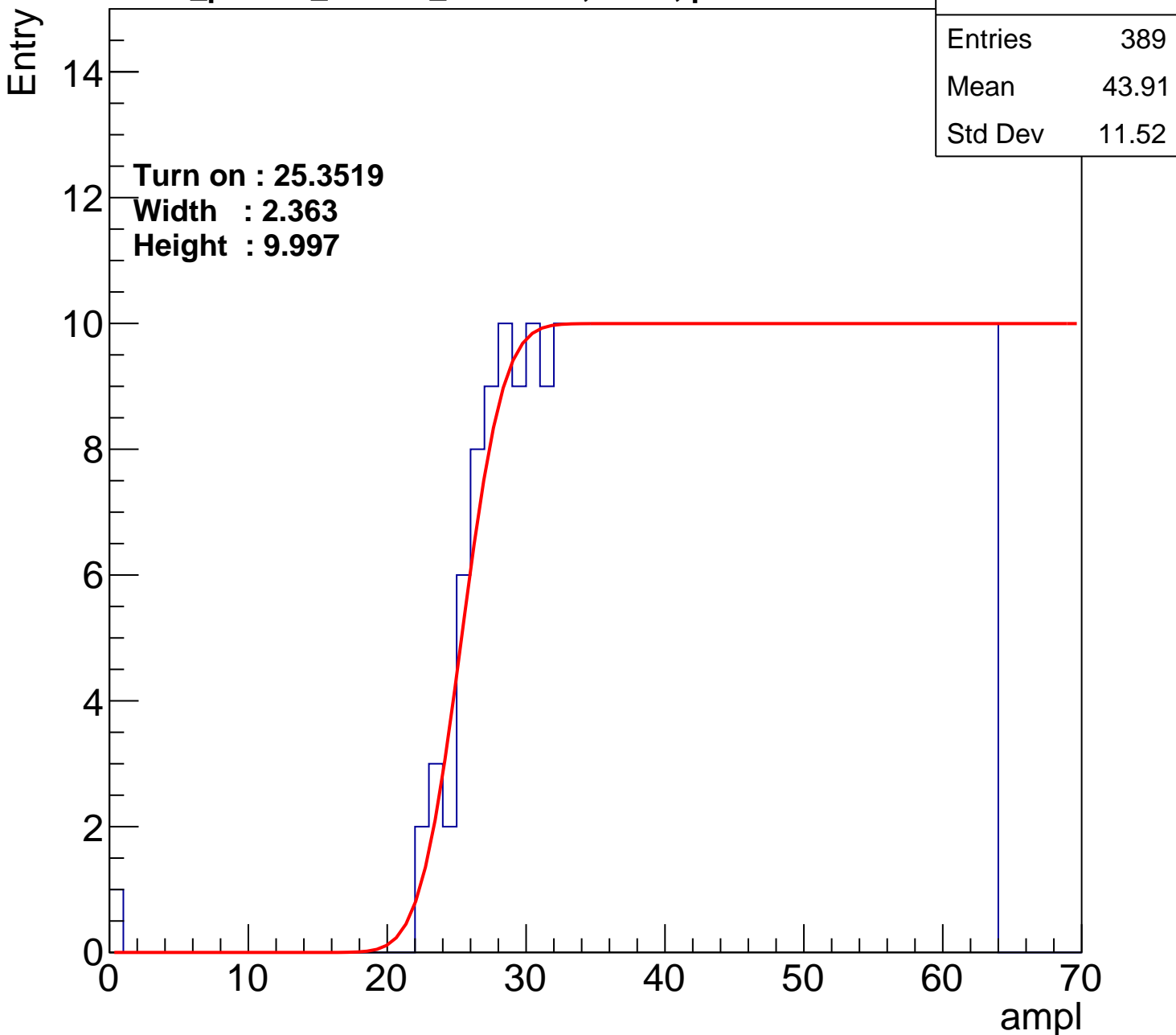
Mean	43.91
------	-------

Std Dev	11.52
---------	-------

**Turn on : 25.3519**

**Width : 2.363**

**Height : 9.997**





# B1L000S, U2-ch79

calib\_packv5\_042523\_0143.root, FC#3, port B3

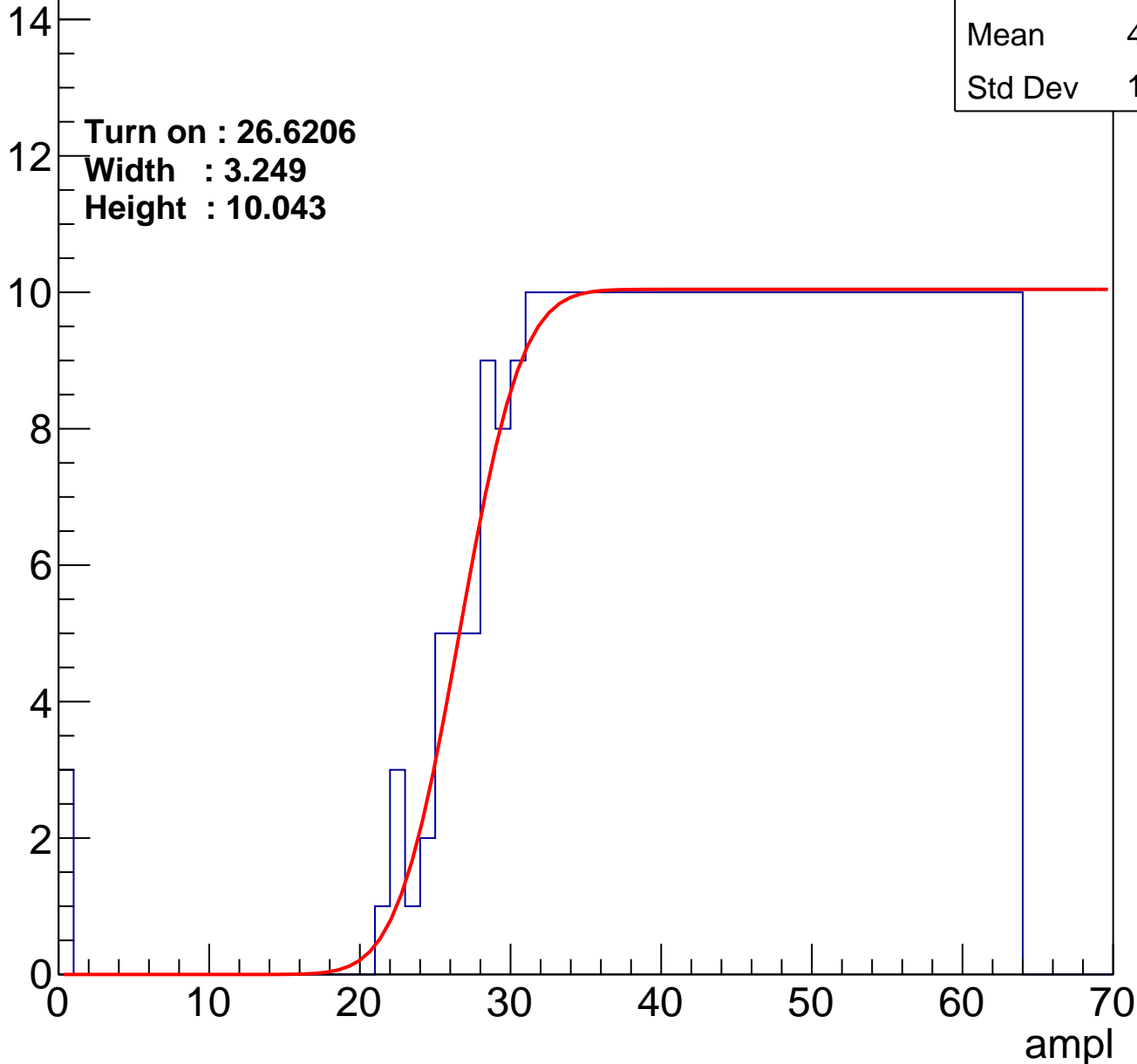
Entries	381
Mean	44.13
Std Dev	11.76

Turn on : 26.6206

Width : 3.249

Height : 10.043

Entry



# B1L000S, U2-ch80

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	386
Mean	44.06
Std Dev	11.44

**Turn on : 25.3338**

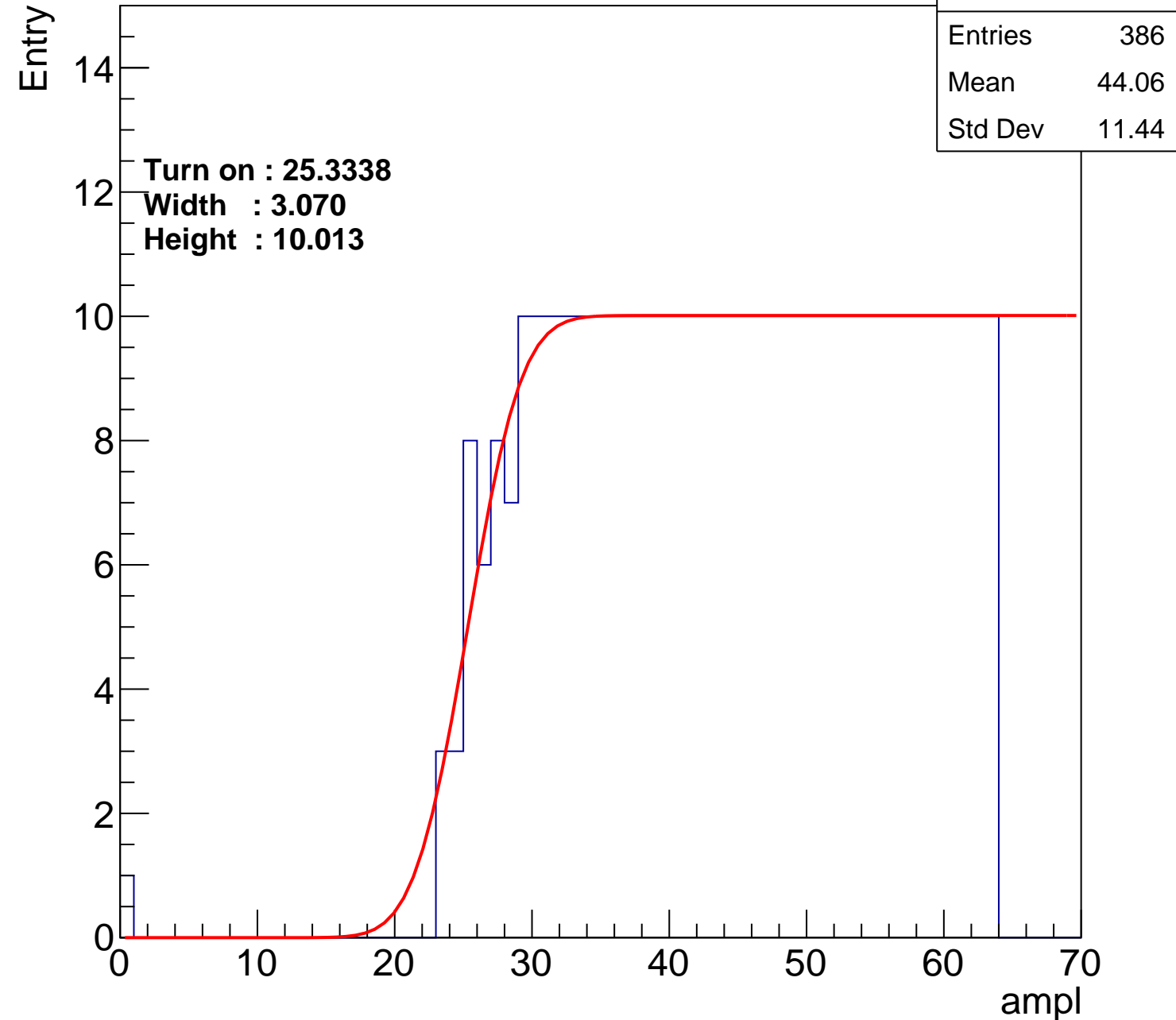
**Width : 3.070**

**Height : 10.013**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch81

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	369
Mean	44.86
Std Dev	11.14

**Turn on : 27.5334**

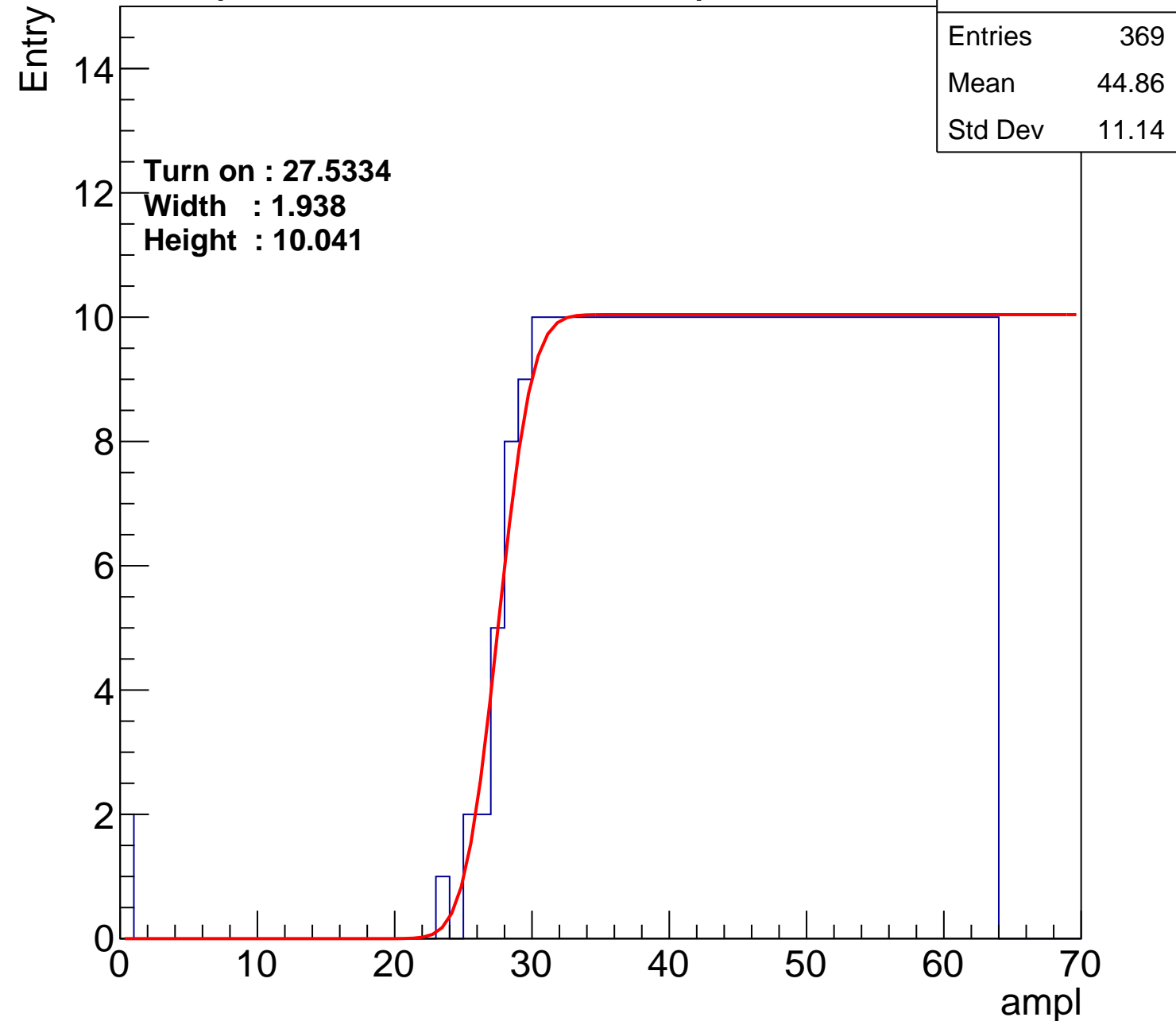
**Width : 1.938**

**Height : 10.041**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch82

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	374
Mean	44.34
Std Dev	11.86

Turn on : 27.4979

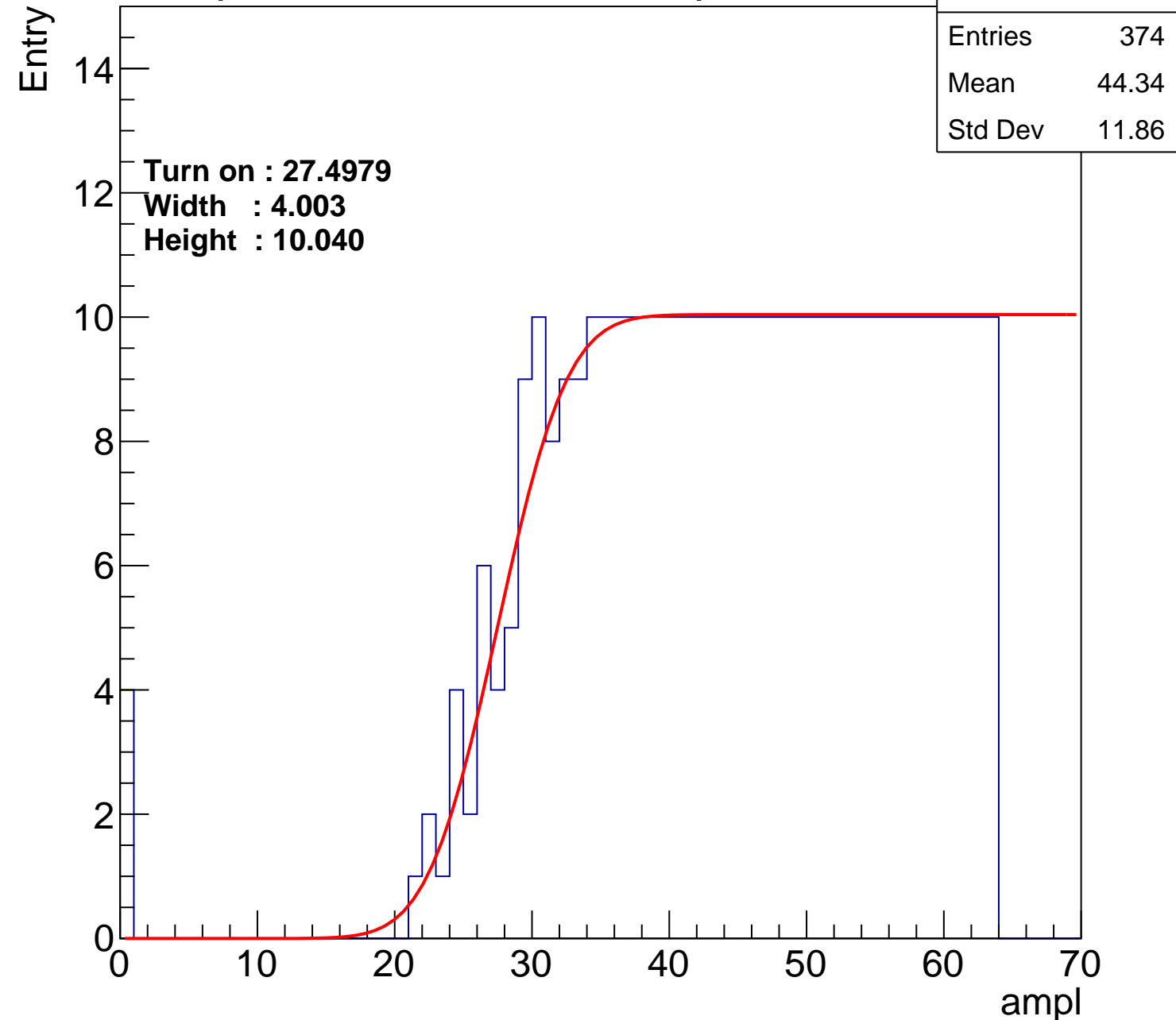
Width : 4.003

Height : 10.040

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch83

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	384
Mean	44.02
Std Dev	11.76

Turn on : 26.0069

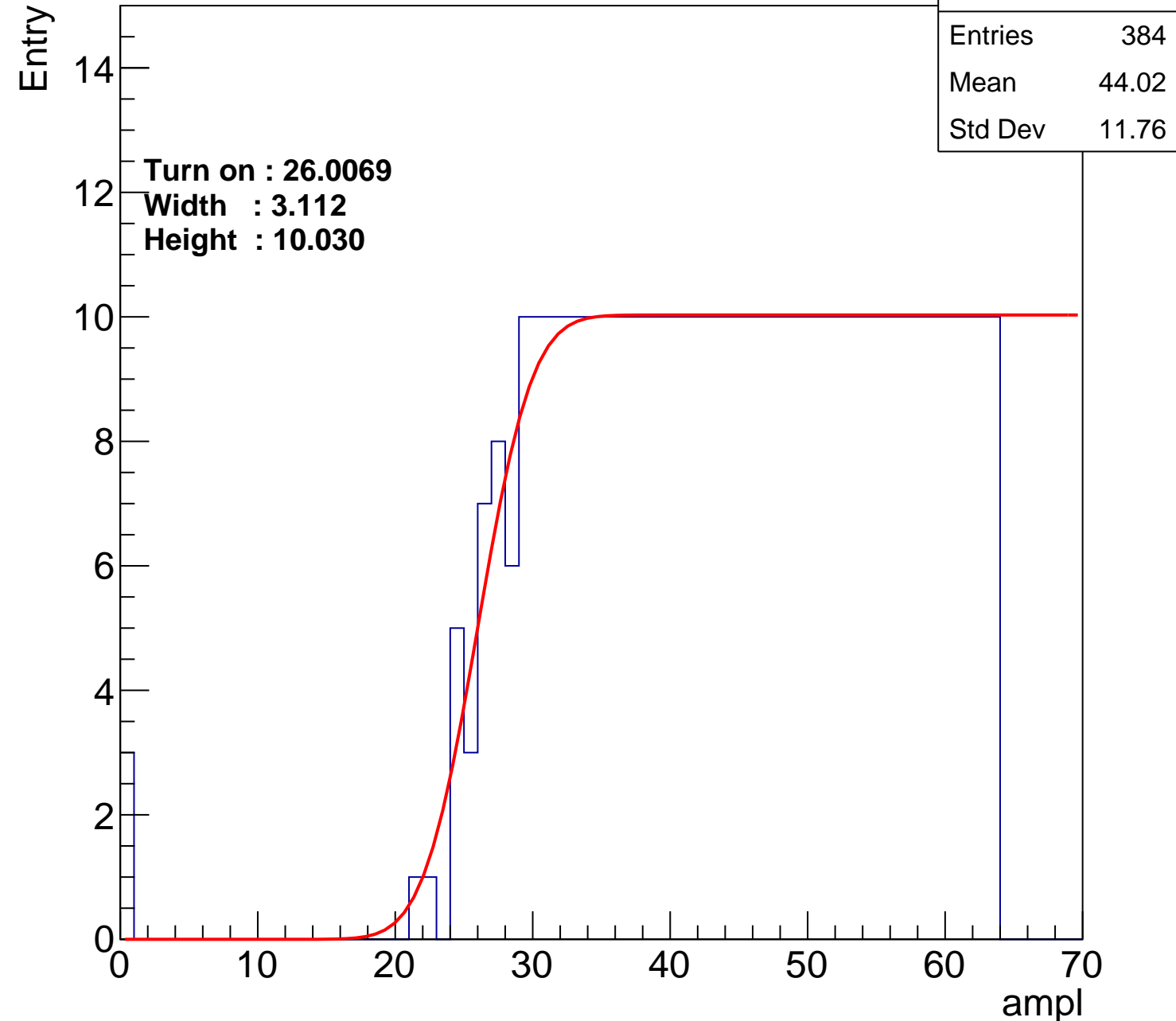
Width : 3.112

Height : 10.030

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch84

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	398
Mean	43.16
Std Dev	12.5

Turn on : 25.0518

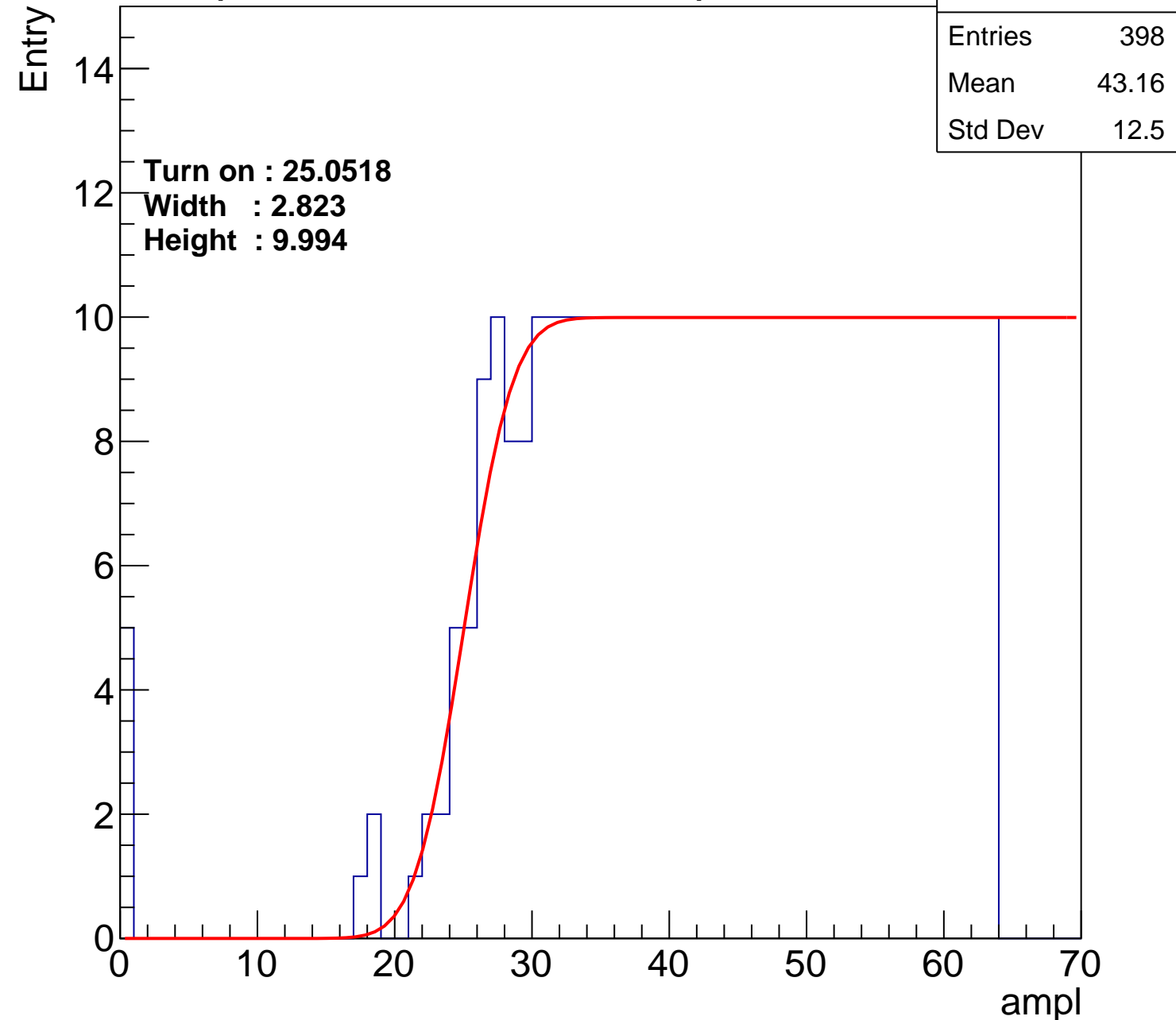
Width : 2.823

Height : 9.994

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch85

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	389
Mean	43.86
Std Dev	11.68

Turn on : 25.4417

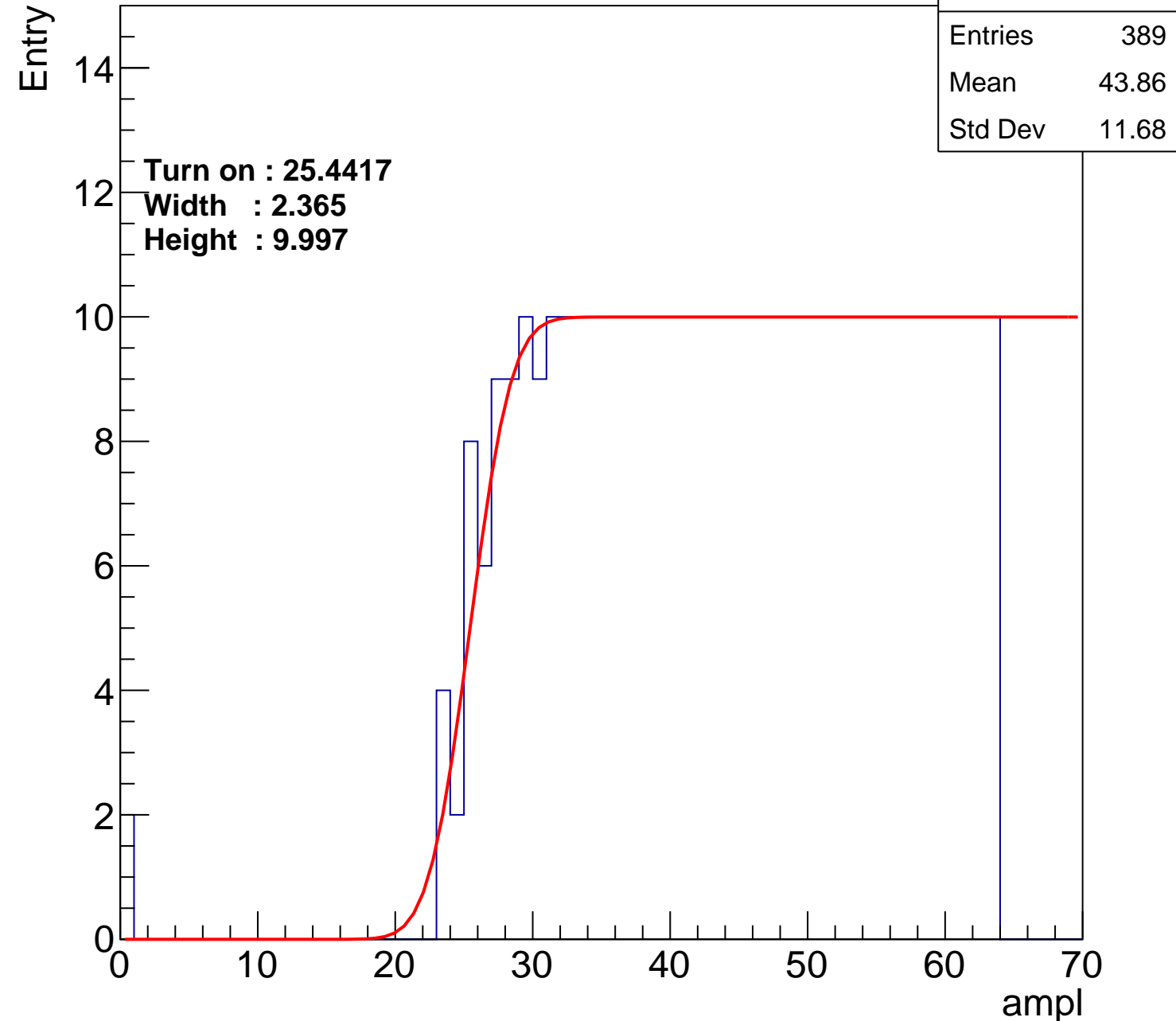
Width : 2.365

Height : 9.997

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch86

calib\_packv5\_042523\_0143.root, FC#3, port B3

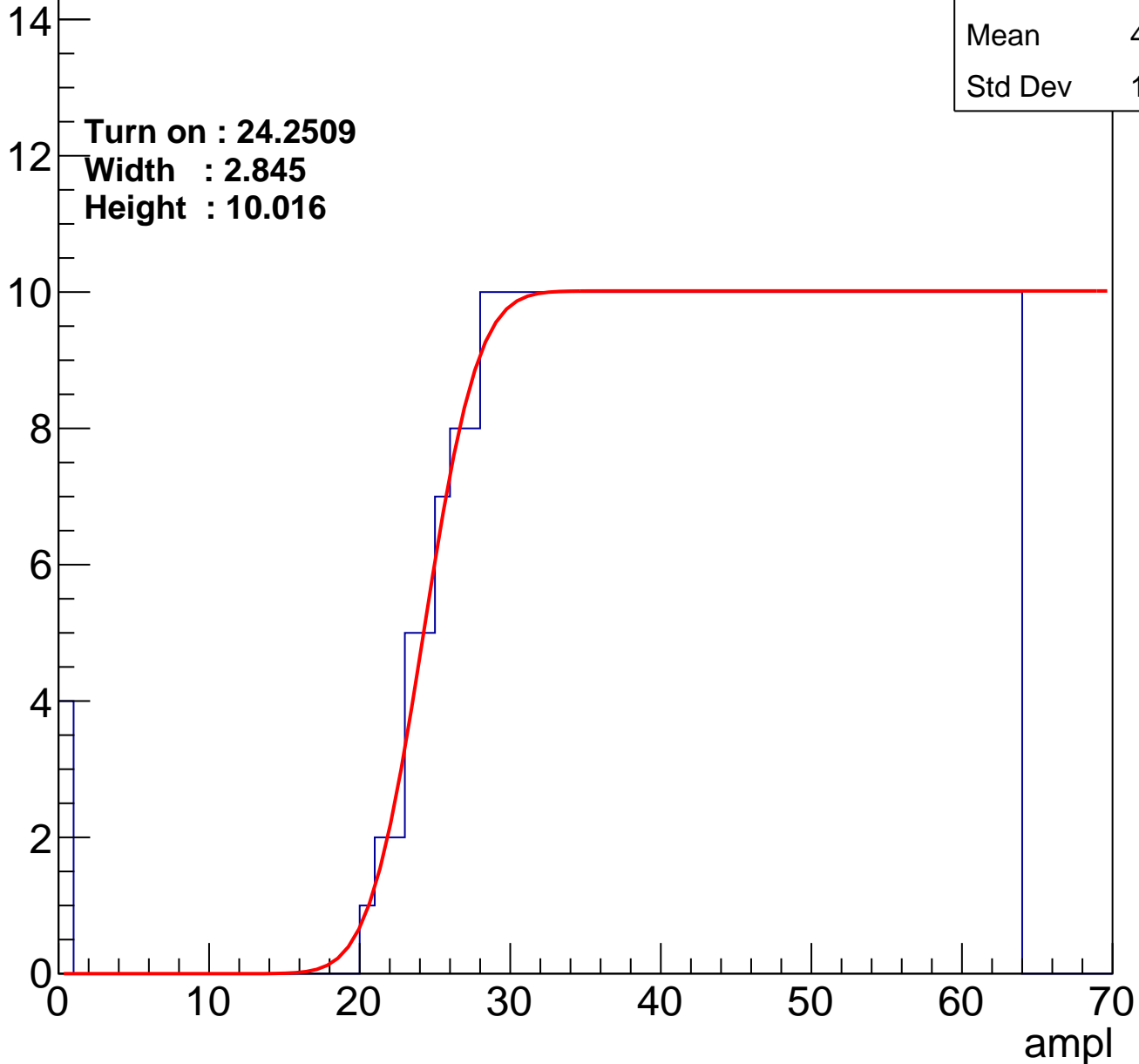
Entries	402
Mean	43.08
Std Dev	12.35

Turn on : 24.2509

Width : 2.845

Height : 10.016

Entry





# B1L000S, U2-ch87

calib\_packv5\_042523\_0143.root, FC#3, port B3

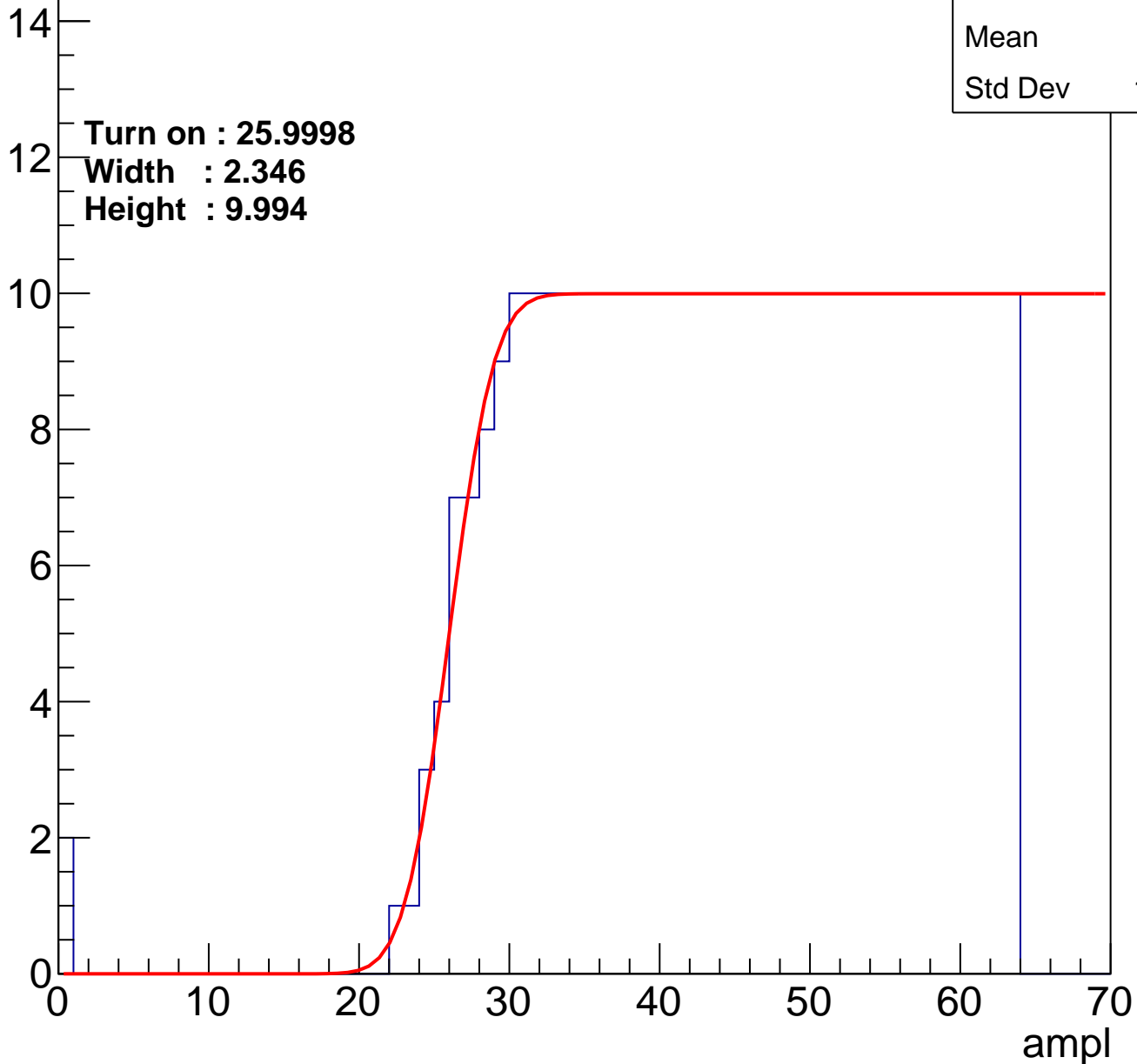
Entries	382
Mean	44.2
Std Dev	11.51

**Turn on : 25.9998**

**Width : 2.346**

**Height : 9.994**

Entry



# B1L000S, U2-ch88

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	393
Mean	43.68
Std Dev	11.69

Turn on : 25.1408

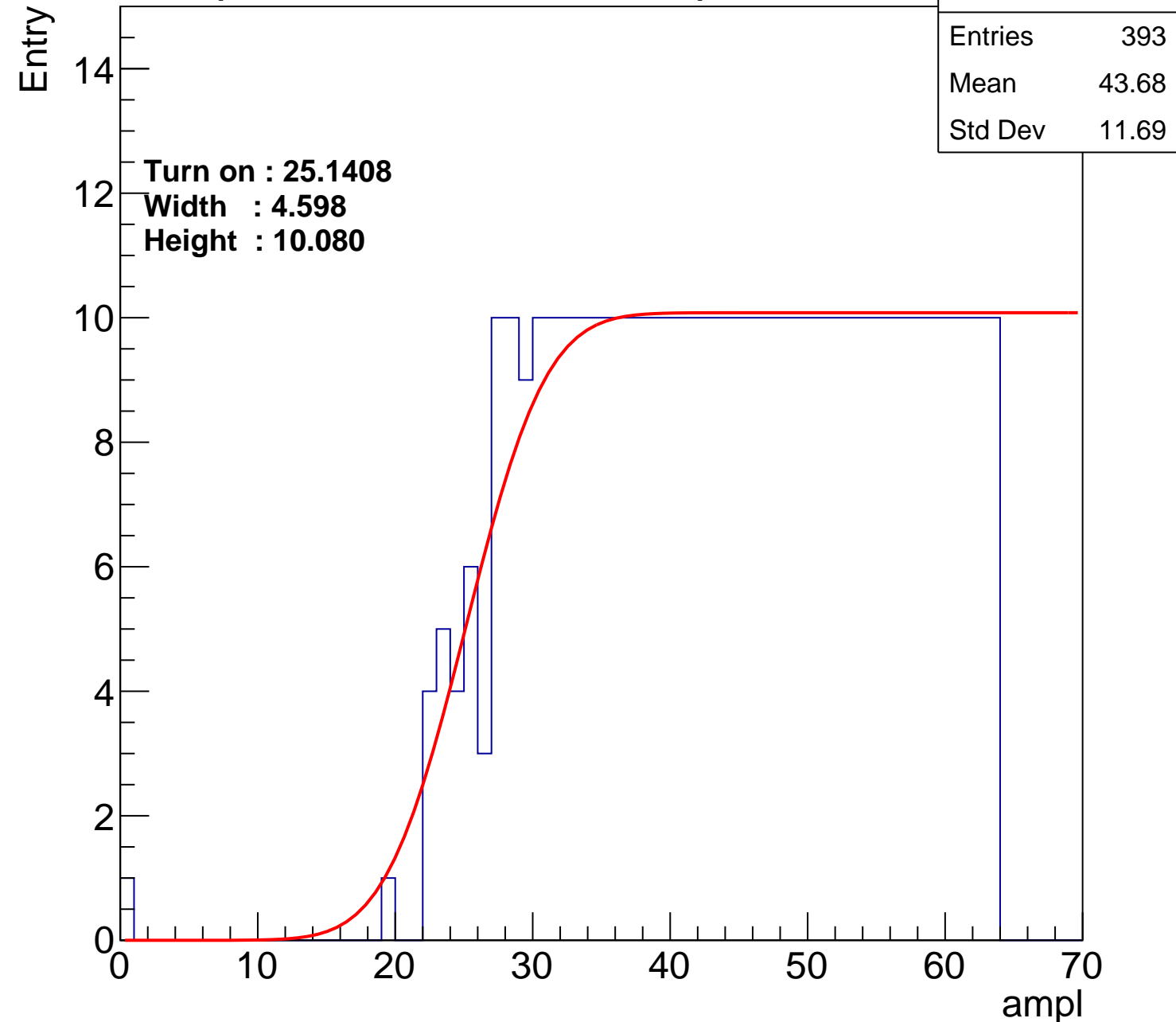
Width : 4.598

Height : 10.080

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch89

calib\_packv5\_042523\_0143.root, FC#3, port B3

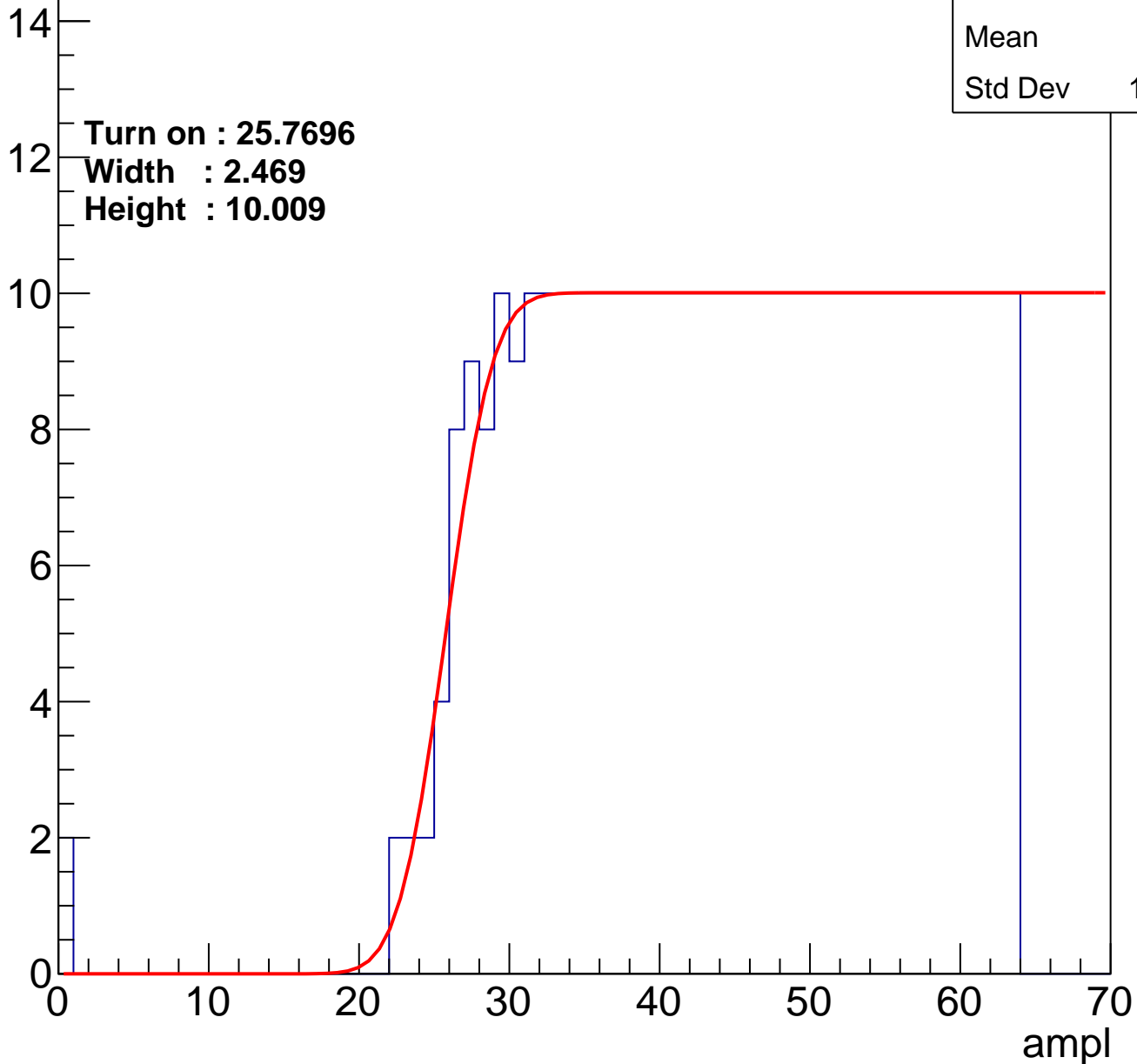
Entries	386
Mean	44
Std Dev	11.62

Turn on : 25.7696

Width : 2.469

Height : 10.009

Entry



# B1L000S, U2-ch90

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	395
Mean	43.49
Std Dev	12.02

**Turn on : 24.6987**

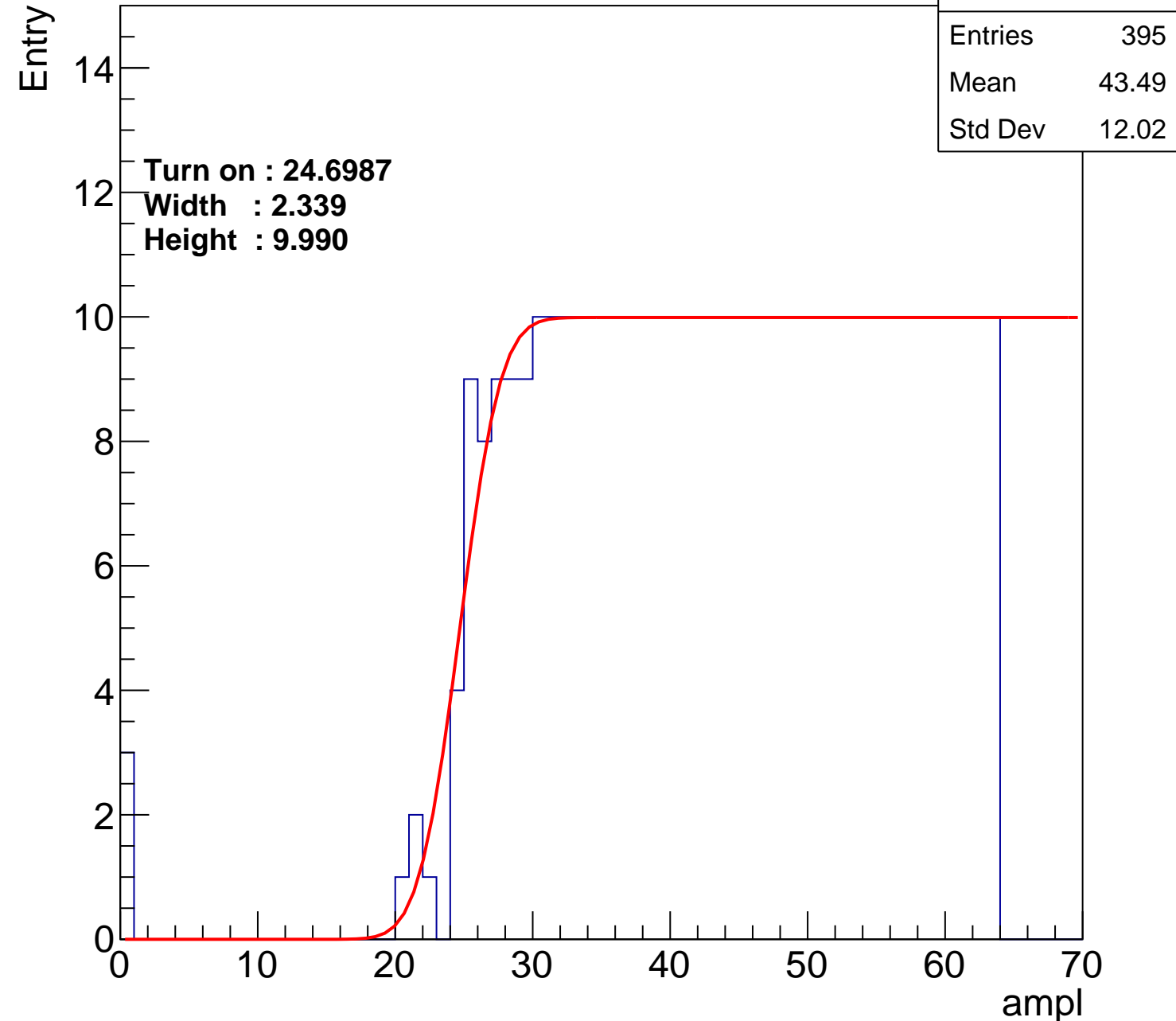
**Width : 2.339**

**Height : 9.990**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch91

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	397
Mean	43.27
Std Dev	12.31

**Turn on : 24.3897**

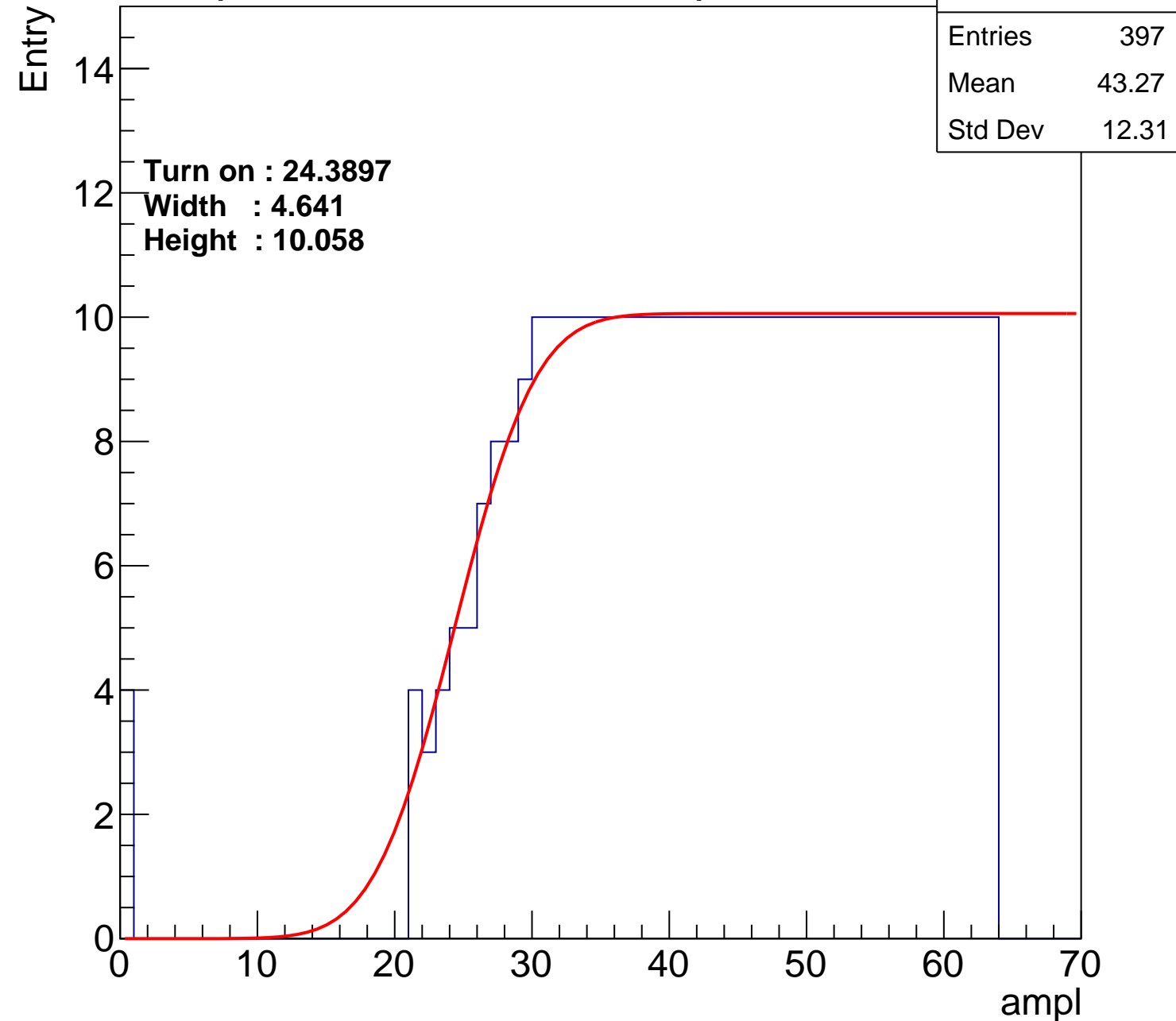
**Width : 4.641**

**Height : 10.058**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch92

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	371
Mean	44.71
Std Dev	11.27

**Turn on : 27.4642**

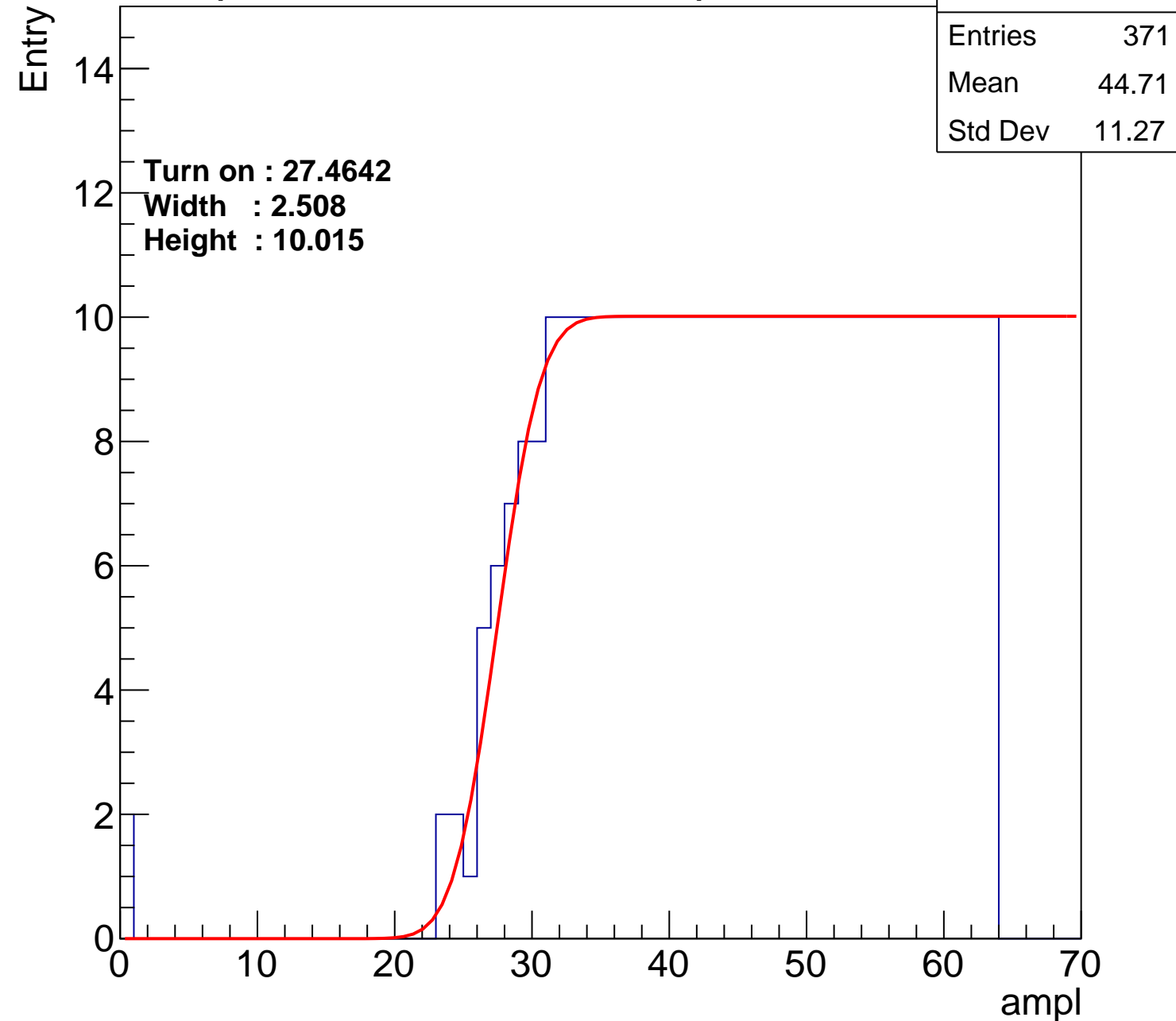
**Width : 2.508**

**Height : 10.015**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch93

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	374
Mean	44.53
Std Dev	11.48

Turn on : 27.0594

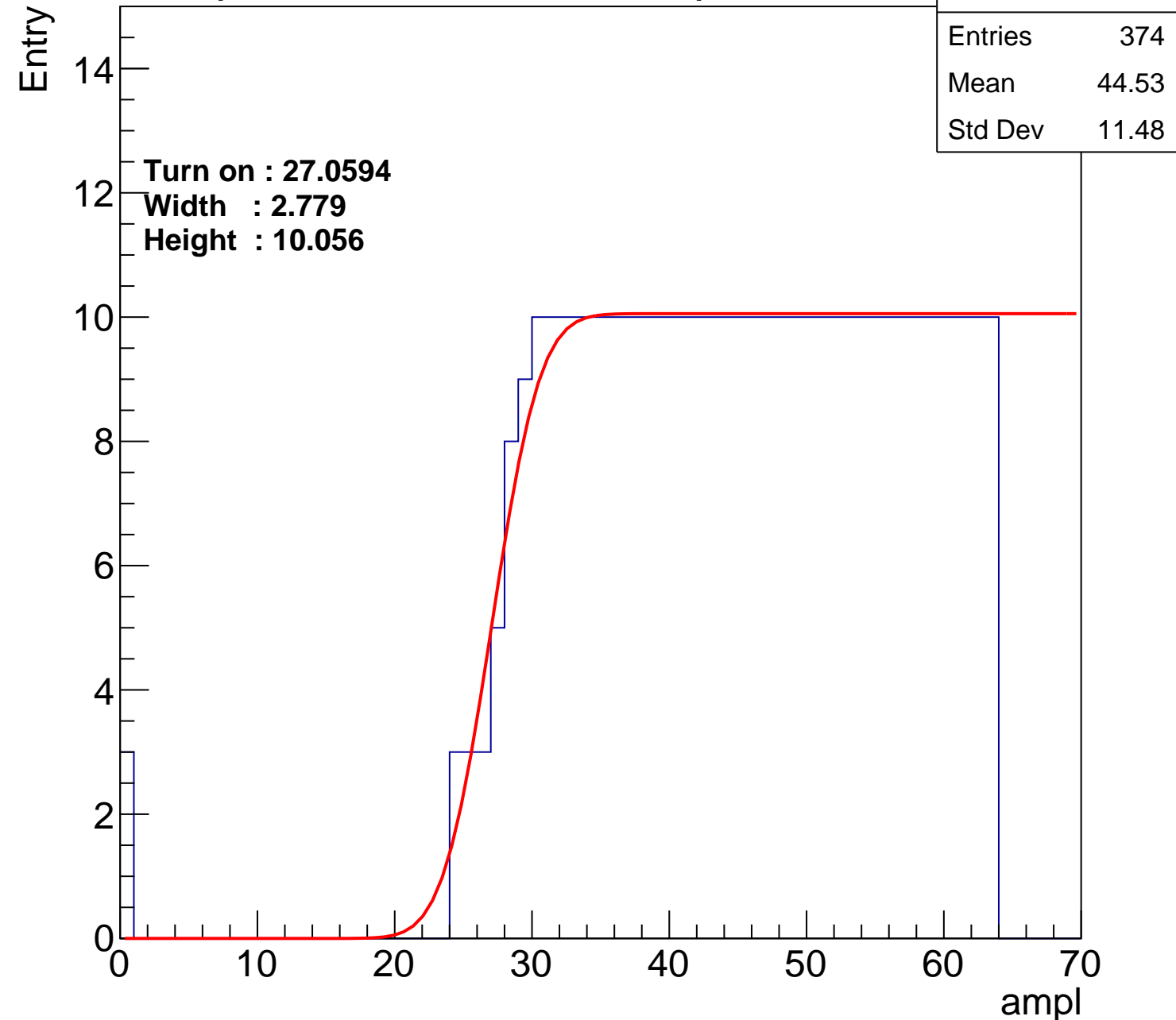
Width : 2.779

Height : 10.056

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch94

calib\_packv5\_042523\_0143.root, FC#3, port B3

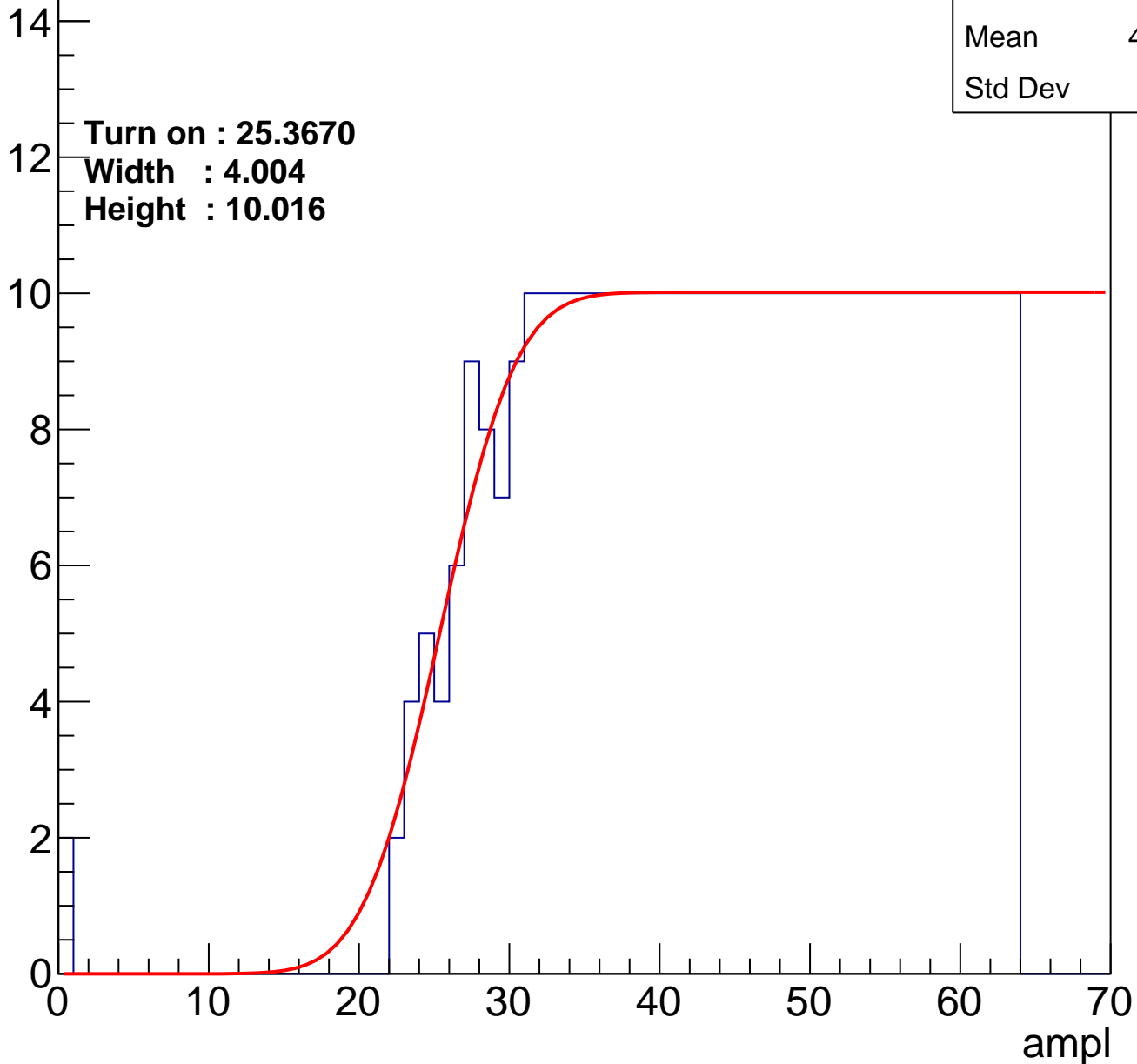
Entries	386
Mean	43.94
Std Dev	11.7

Turn on : 25.3670

Width : 4.004

Height : 10.016

Entry





# B1L000S, U2-ch95

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	397
Mean	43.43
Std Dev	11.96

**Turn on : 24.6753**

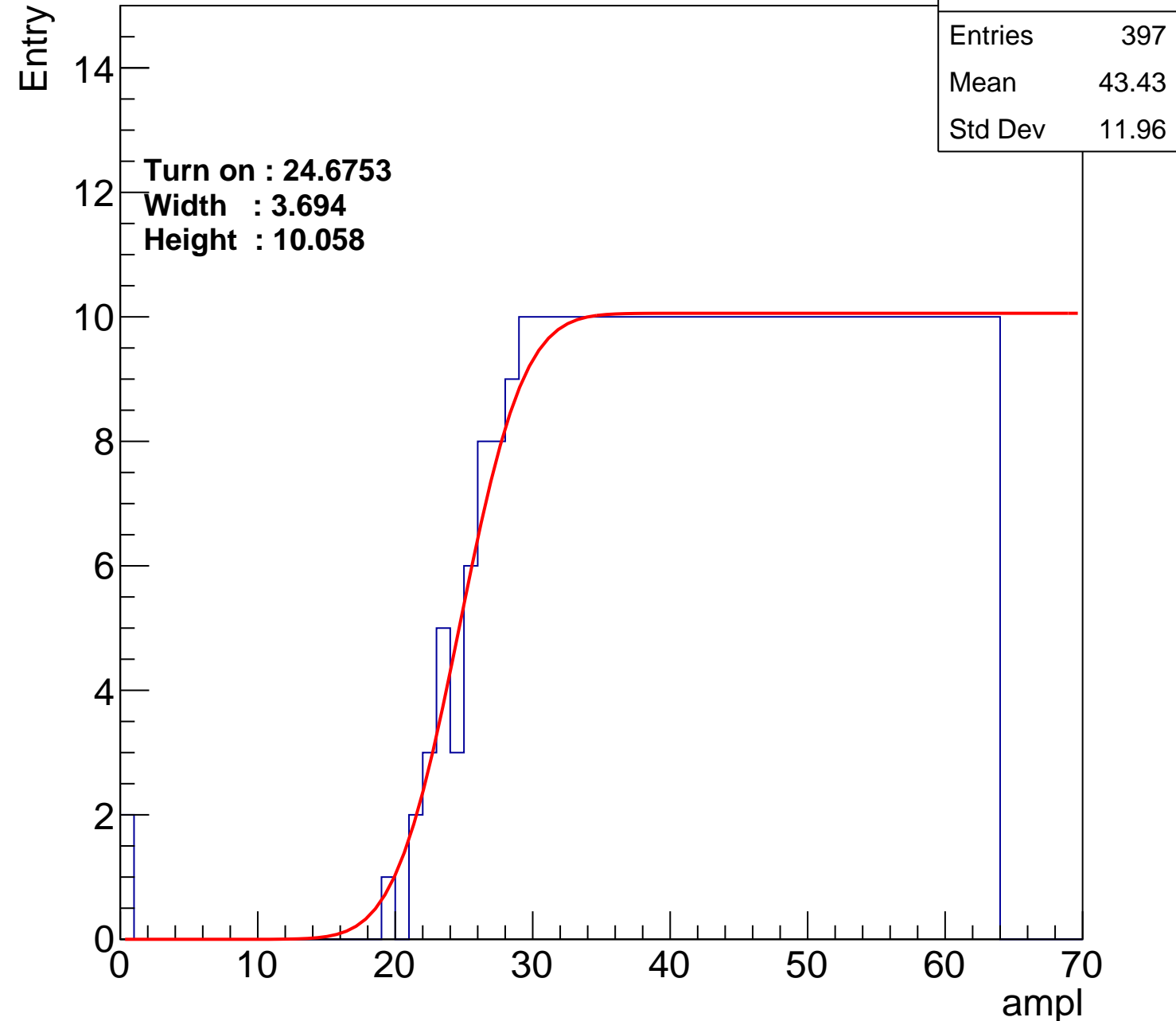
**Width : 3.694**

**Height : 10.058**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch96

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	390
Mean	43.63
Std Dev	12.13

**Turn on : 26.1339**

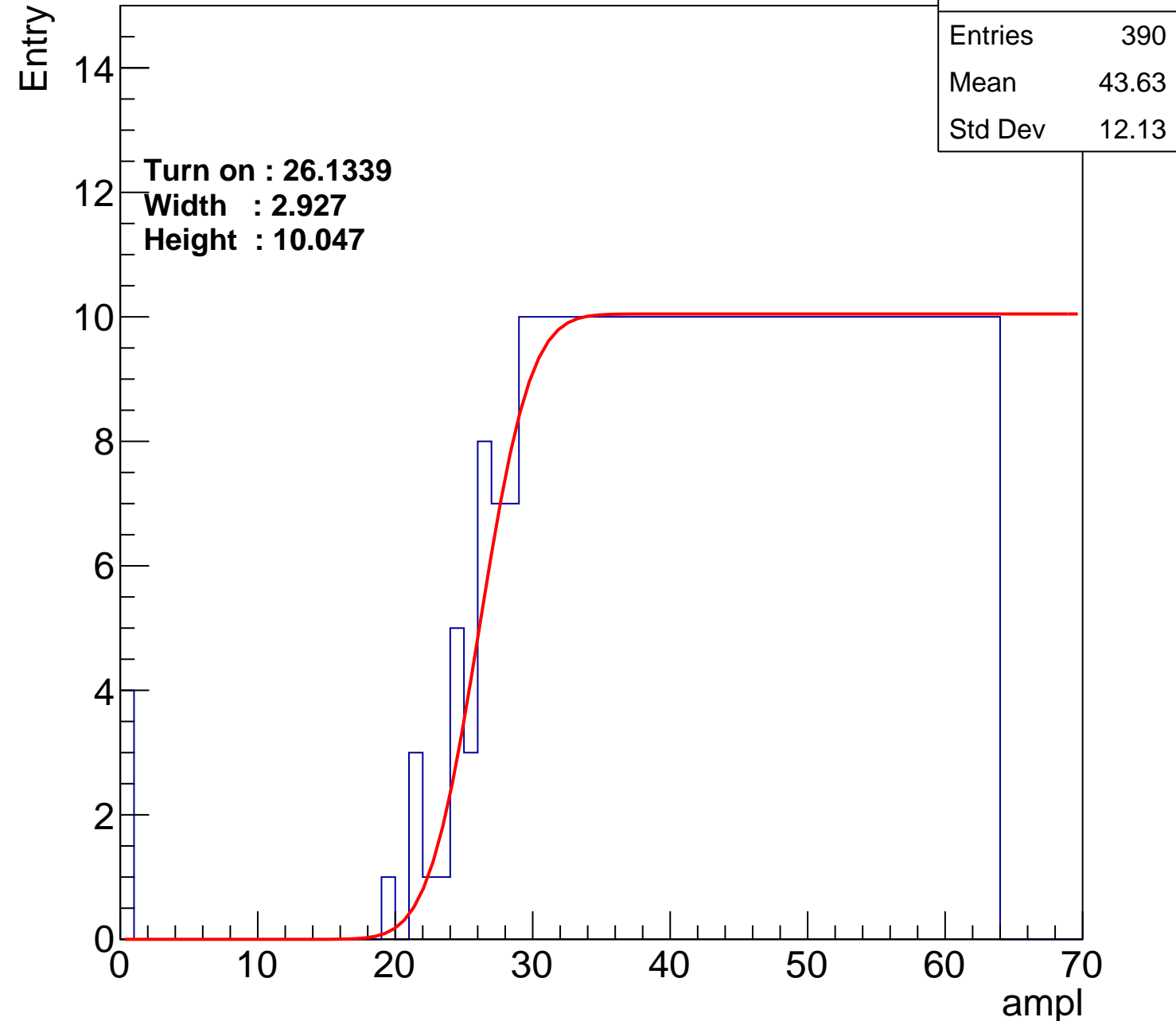
**Width : 2.927**

**Height : 10.047**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch97

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	372
Mean	44.74
Std Dev	11.08

**Turn on : 26.9188**

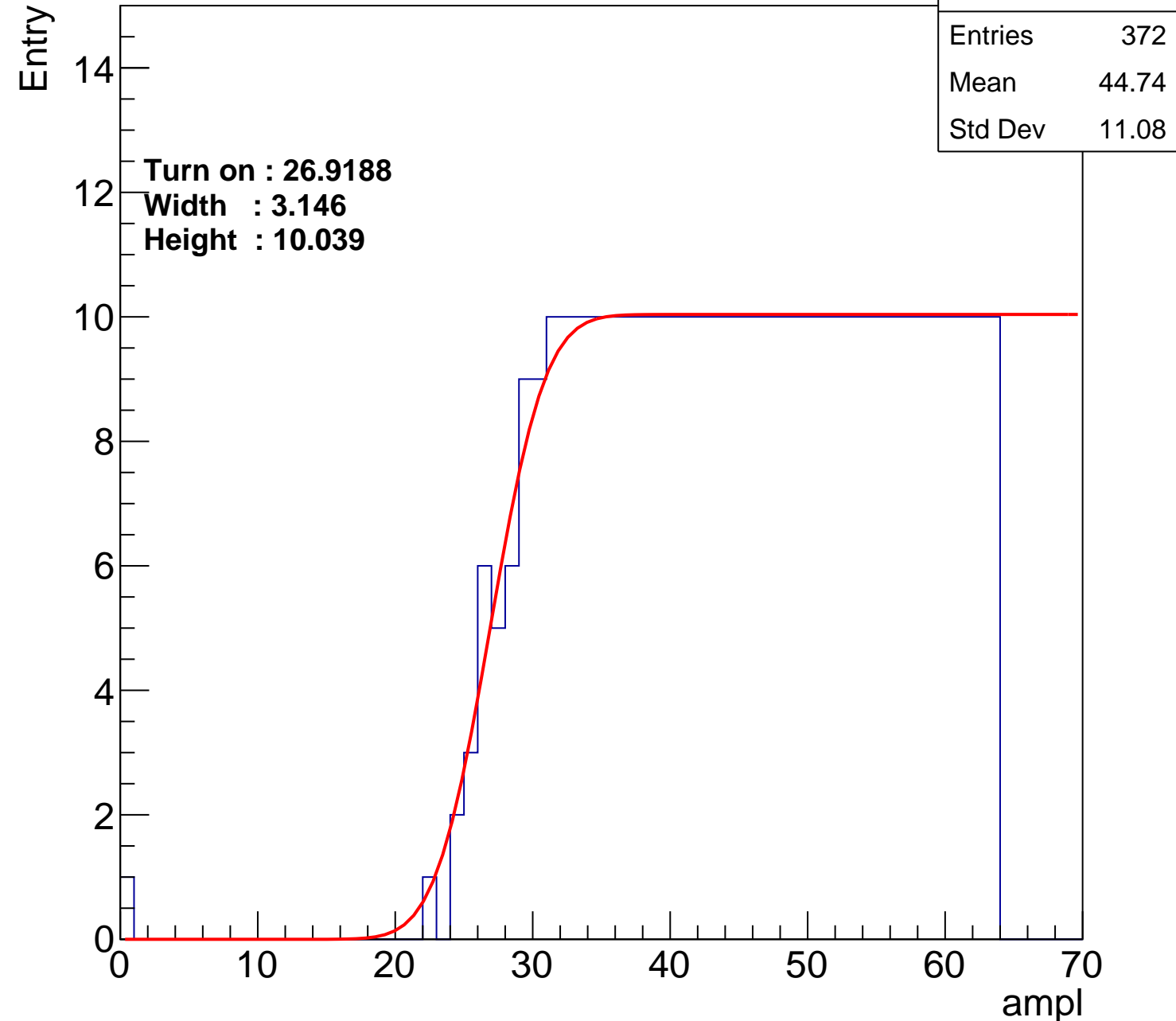
**Width : 3.146**

**Height : 10.039**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch98

calib\_packv5\_042523\_0143.root, FC#3, port B3

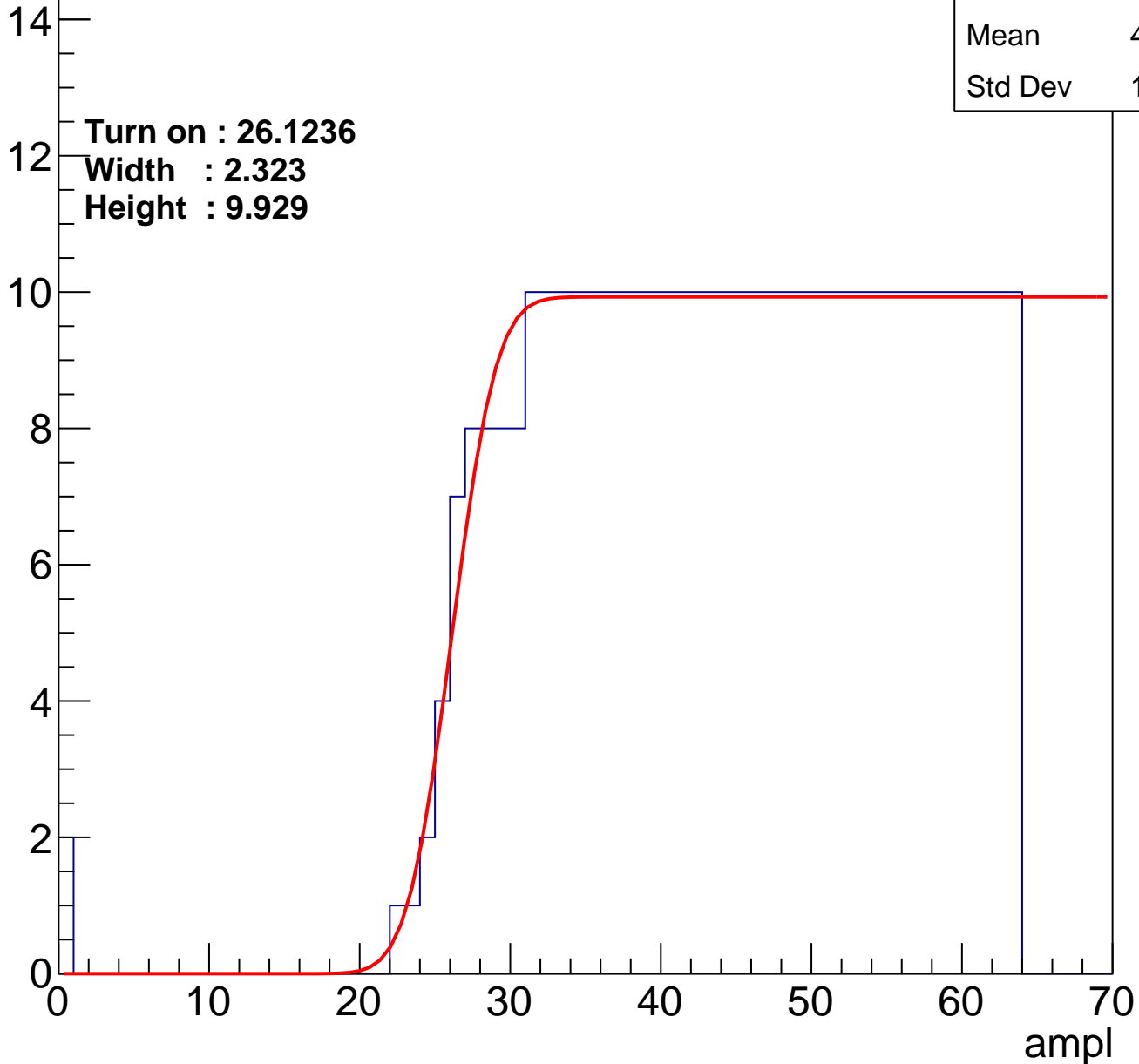
Entry

Entries	379
Mean	44.32
Std Dev	11.47

Turn on : 26.1236

Width : 2.323

Height : 9.929



# B1L000S, U2-ch99

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	384
Mean	43.93
Std Dev	11.98

Turn on : 26.1406

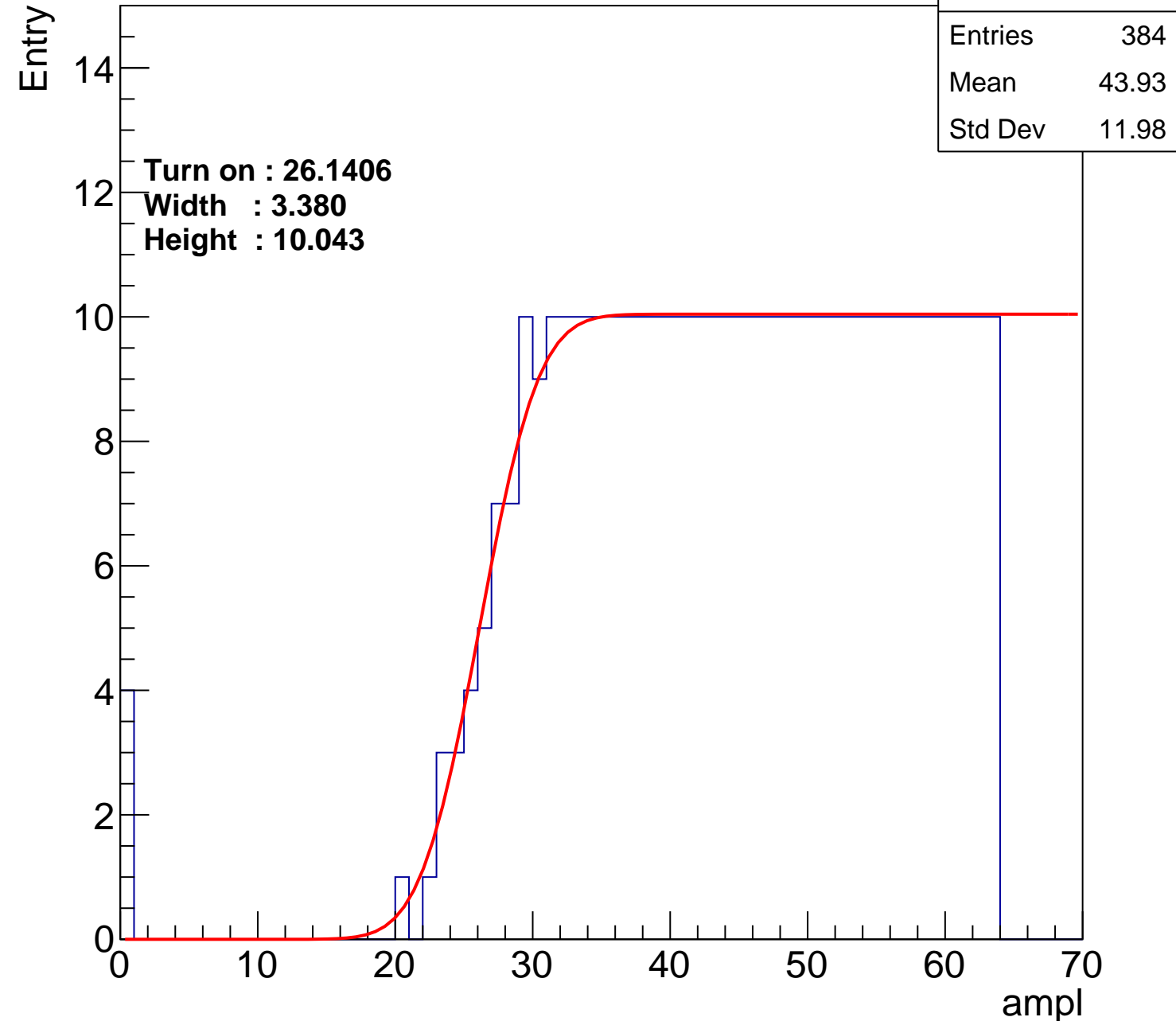
Width : 3.380

Height : 10.043

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch100

calib\_packv5\_042523\_0143.root, FC#3, port B3

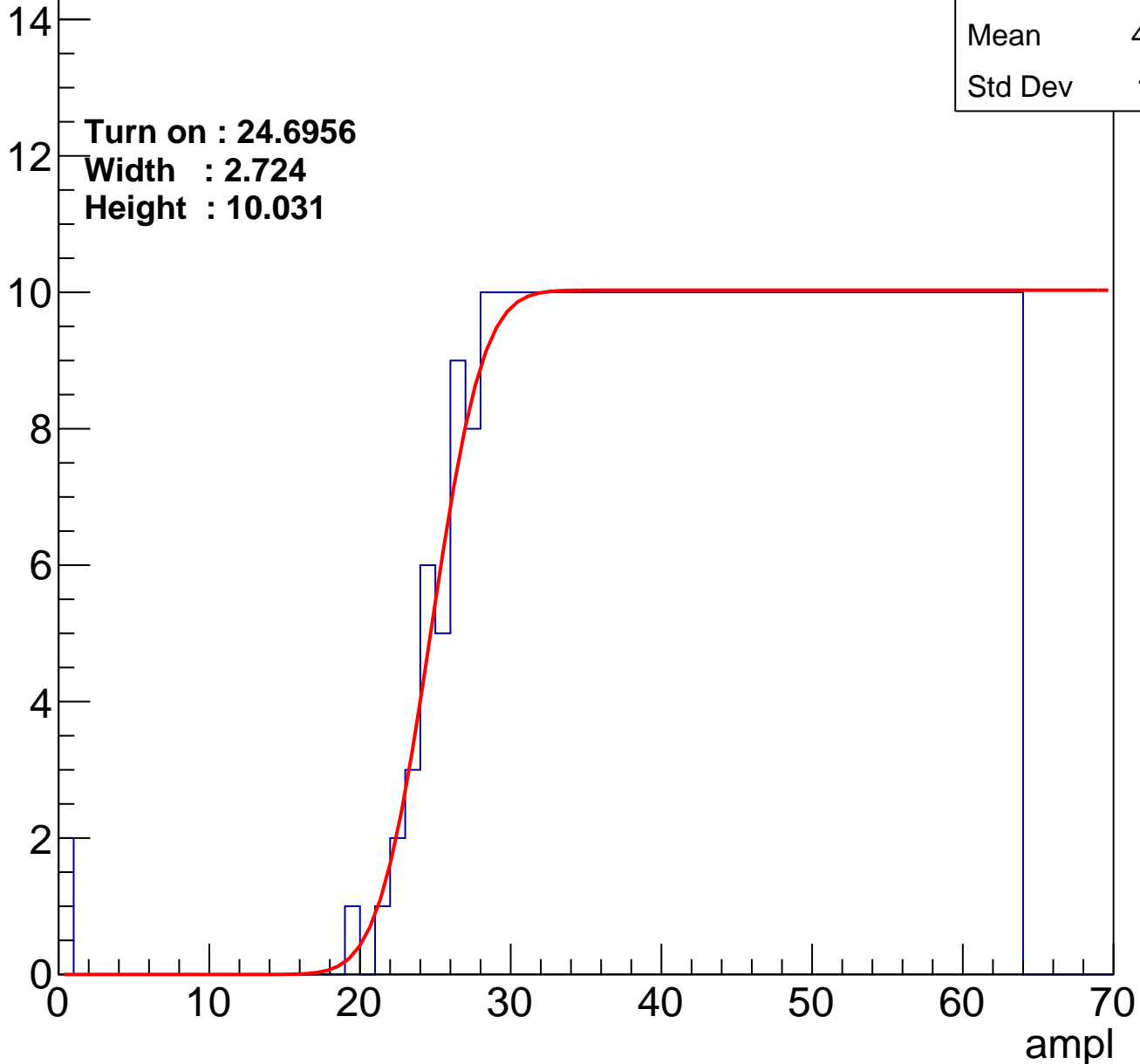
Entries	397
Mean	43.46
Std Dev	11.91

Turn on : 24.6956

Width : 2.724

Height : 10.031

Entry



# B1L000S, U2-ch101

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	379
Mean	44.24
Std Dev	11.68

Turn on : 26.6400

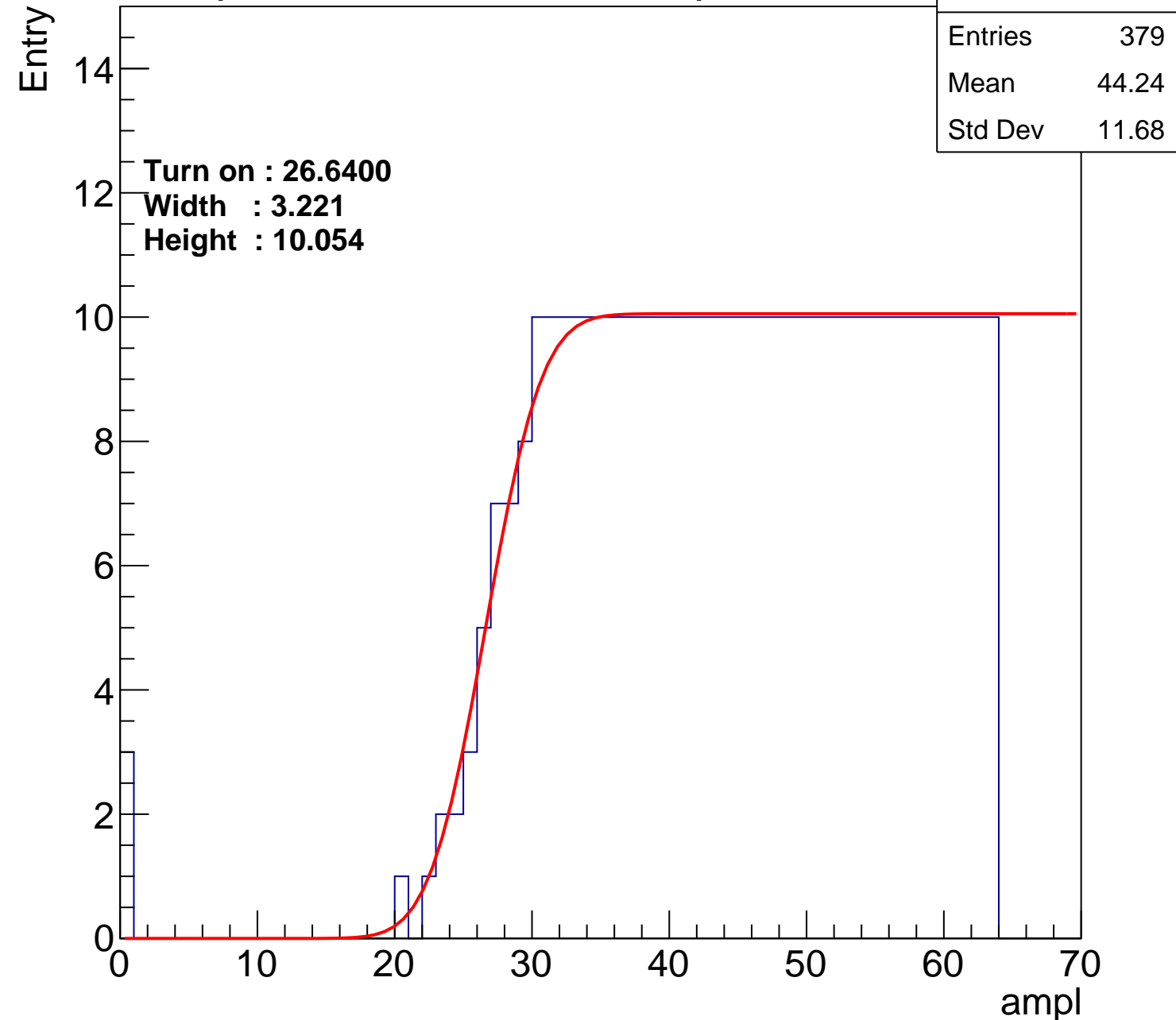
Width : 3.221

Height : 10.054

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch102

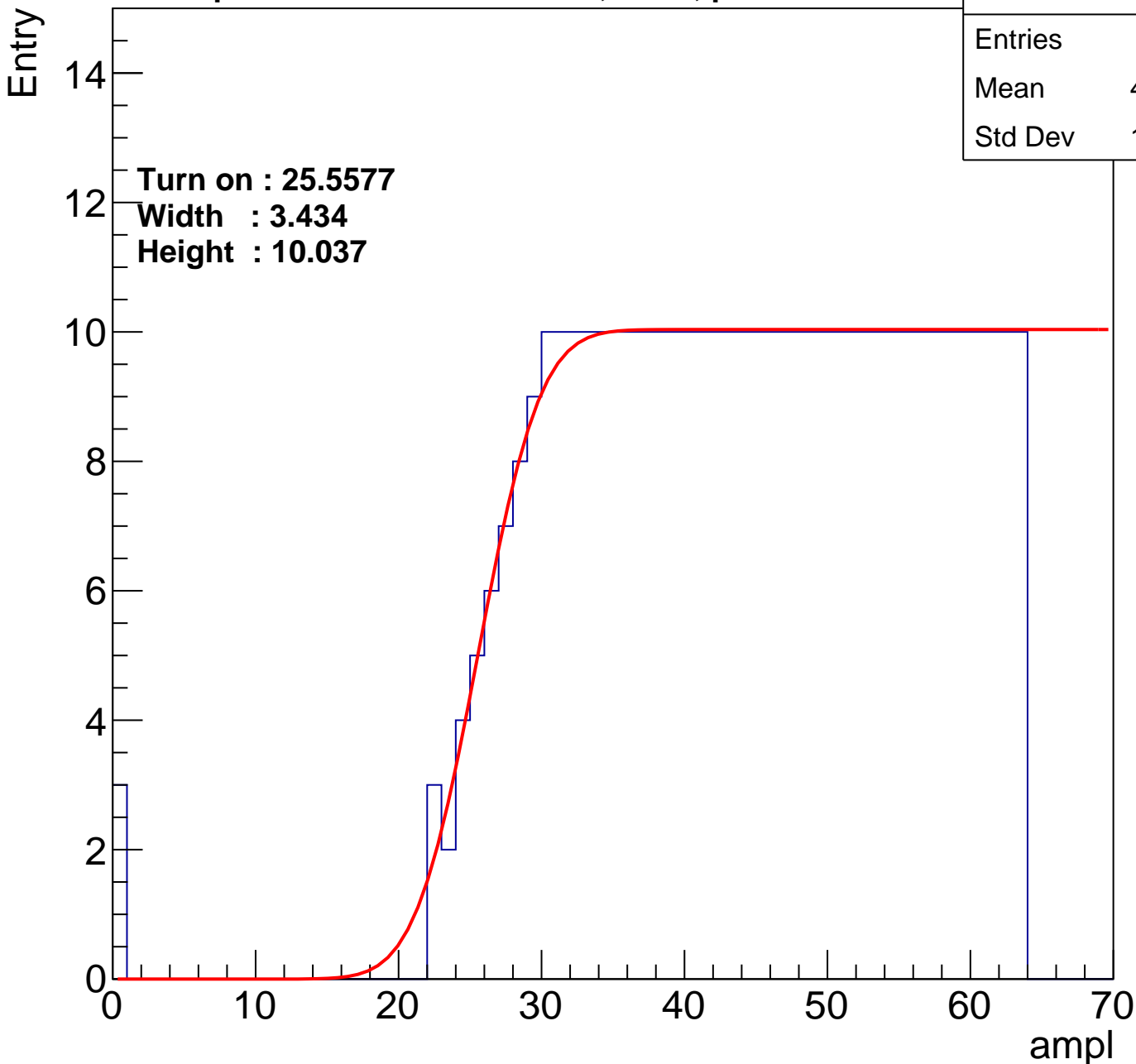
**calib\_packv5\_042523\_0143.root, FC#3, port B3**

Entries	387
Mean	43.86
Std Dev	11.86

**Turn on : 25.5577**

**Width : 3.434**

**Height : 10.037**





# B1L000S, U2-ch103

calib\_packv5\_042523\_0143.root, FC#3, port B3

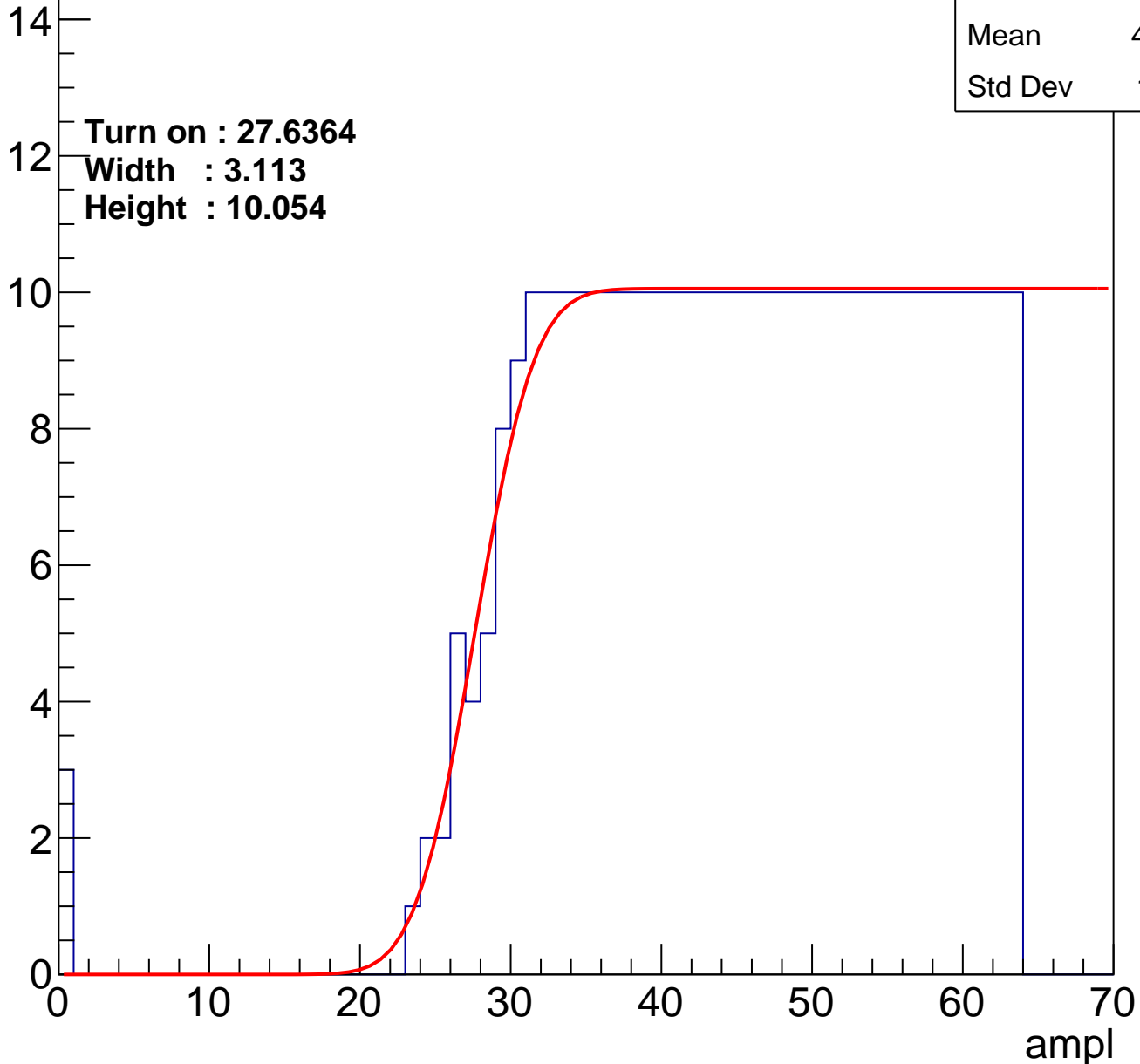
Entries	369
Mean	44.75
Std Dev	11.41

Turn on : 27.6364

Width : 3.113

Height : 10.054

Entry



# B1L000S, U2-ch104

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	385
Mean	43.98
Std Dev	11.7

**Turn on : 25.7668**

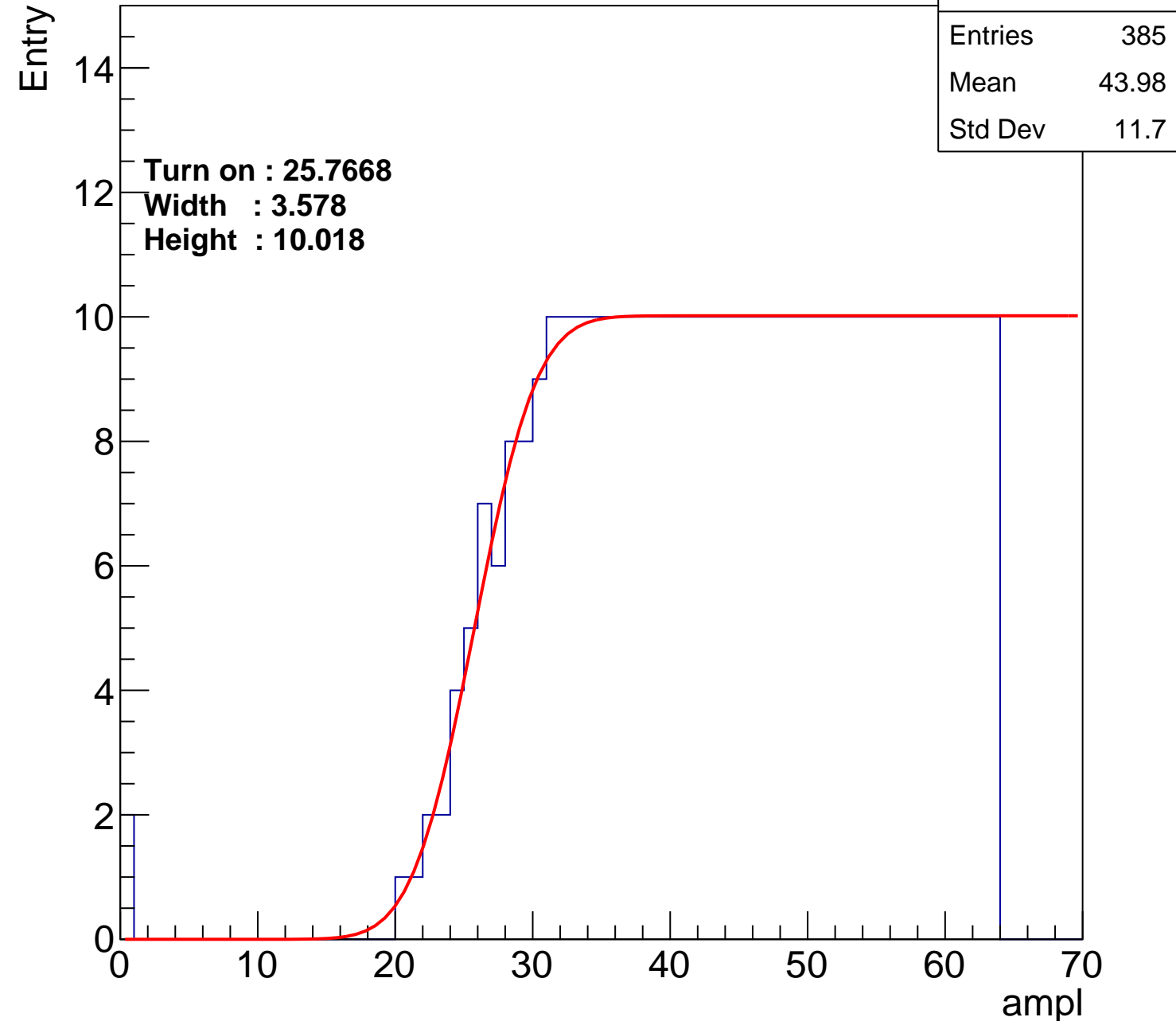
**Width : 3.578**

**Height : 10.018**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch105

calib\_packv5\_042523\_0143.root, FC#3, port B3

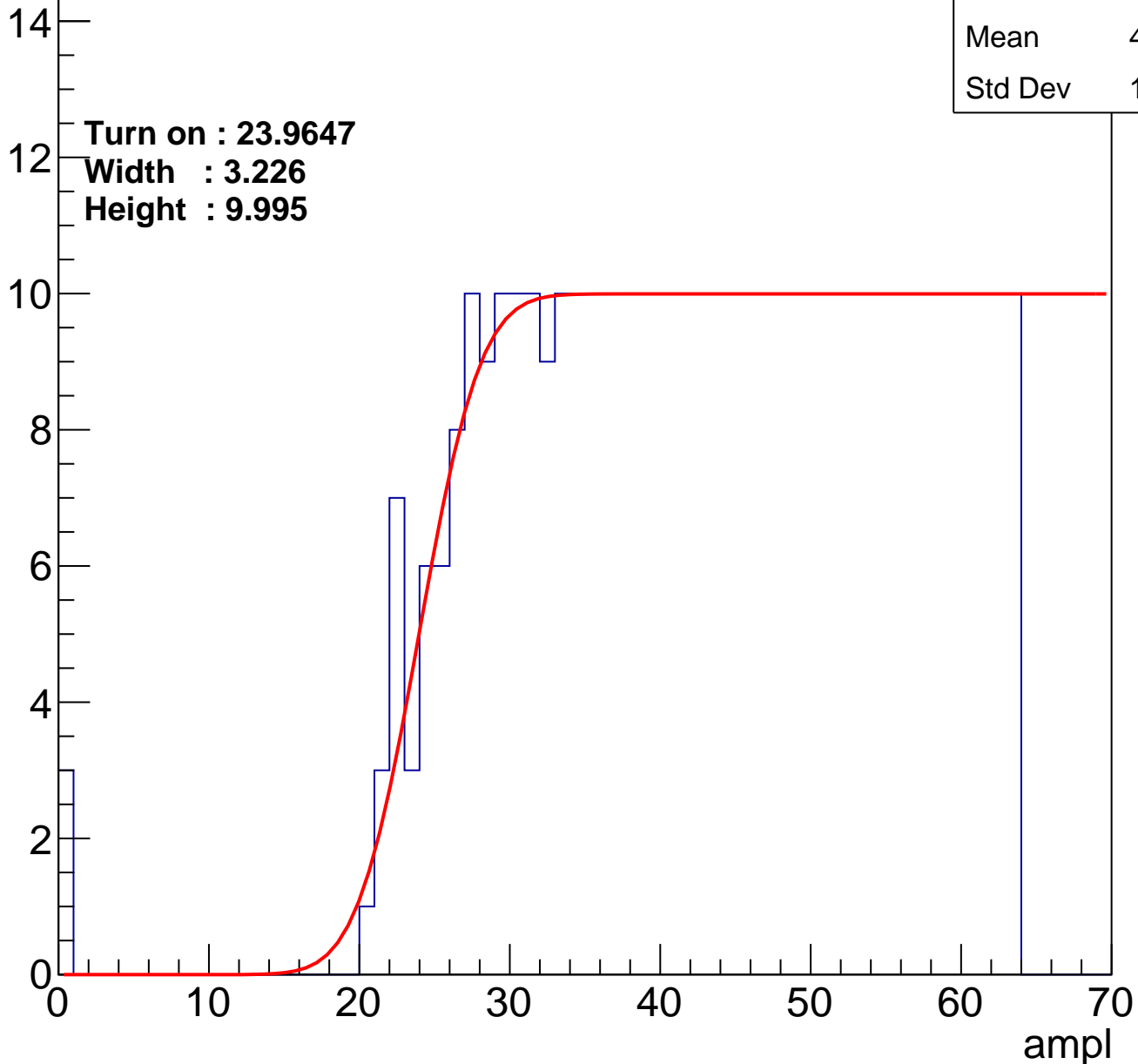
Entries	405
Mean	42.96
Std Dev	12.33

**Turn on : 23.9647**

**Width : 3.226**

**Height : 9.995**

Entry



# B1L000S, U2-ch106

calib\_packv5\_042523\_0143.root, FC#3, port B3

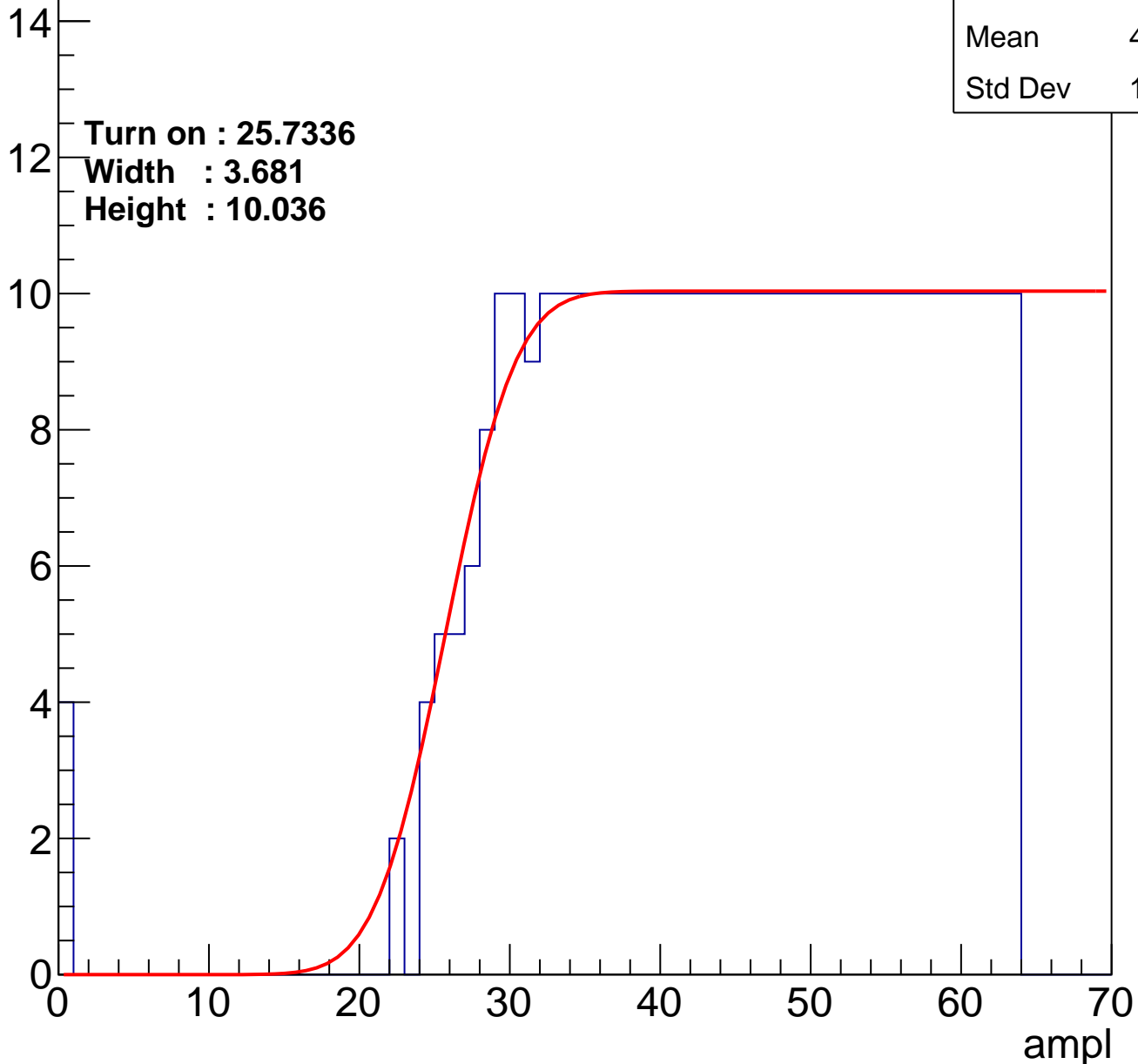
Entries	383
Mean	43.99
Std Dev	11.92

Turn on : 25.7336

Width : 3.681

Height : 10.036

Entry



# B1L000S, U2-ch107

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	370
Mean	44.85
Std Dev	11.02

Turn on : 27.2743

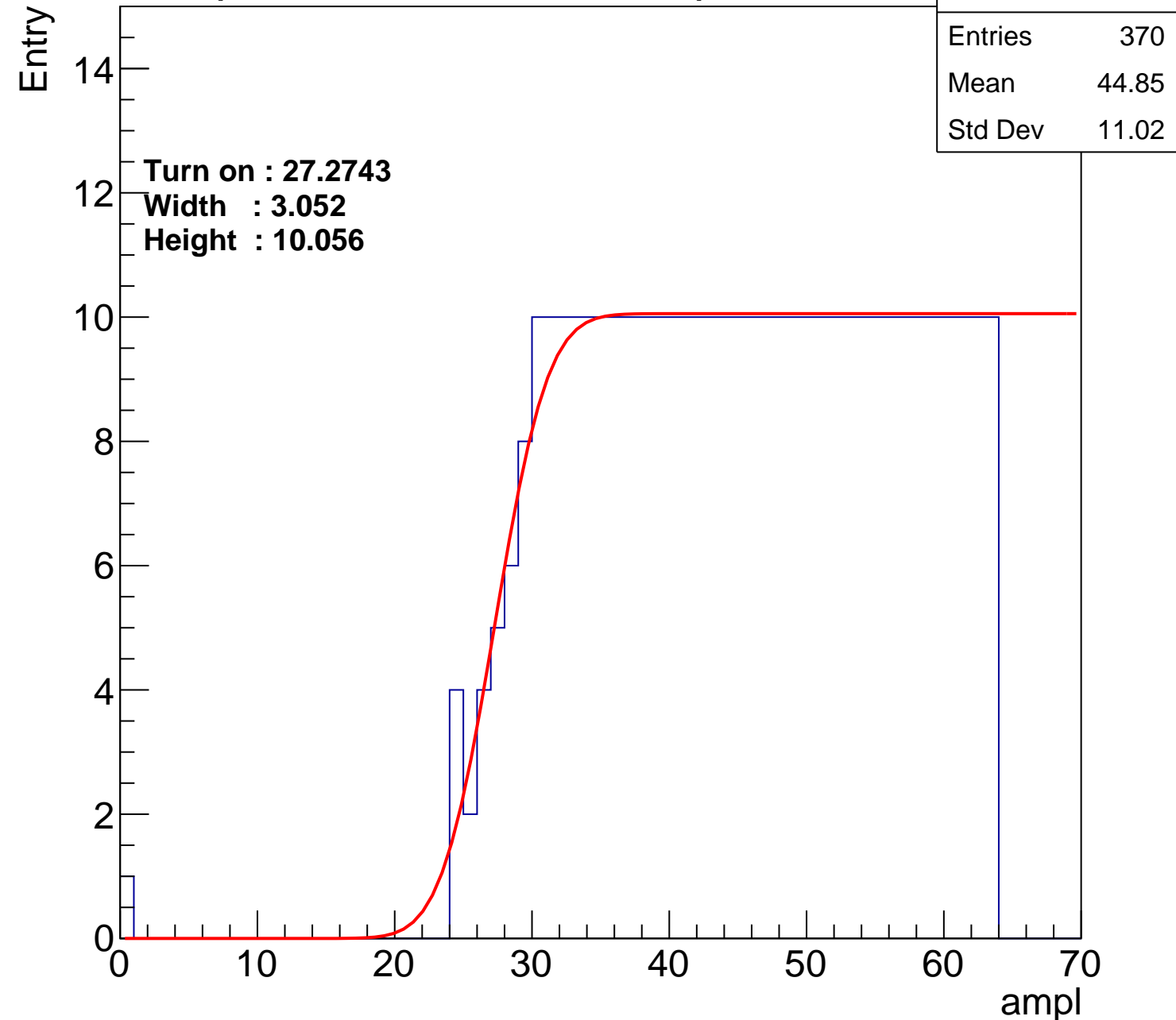
Width : 3.052

Height : 10.056

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch108

calib\_packv5\_042523\_0143.root, FC#3, port B3

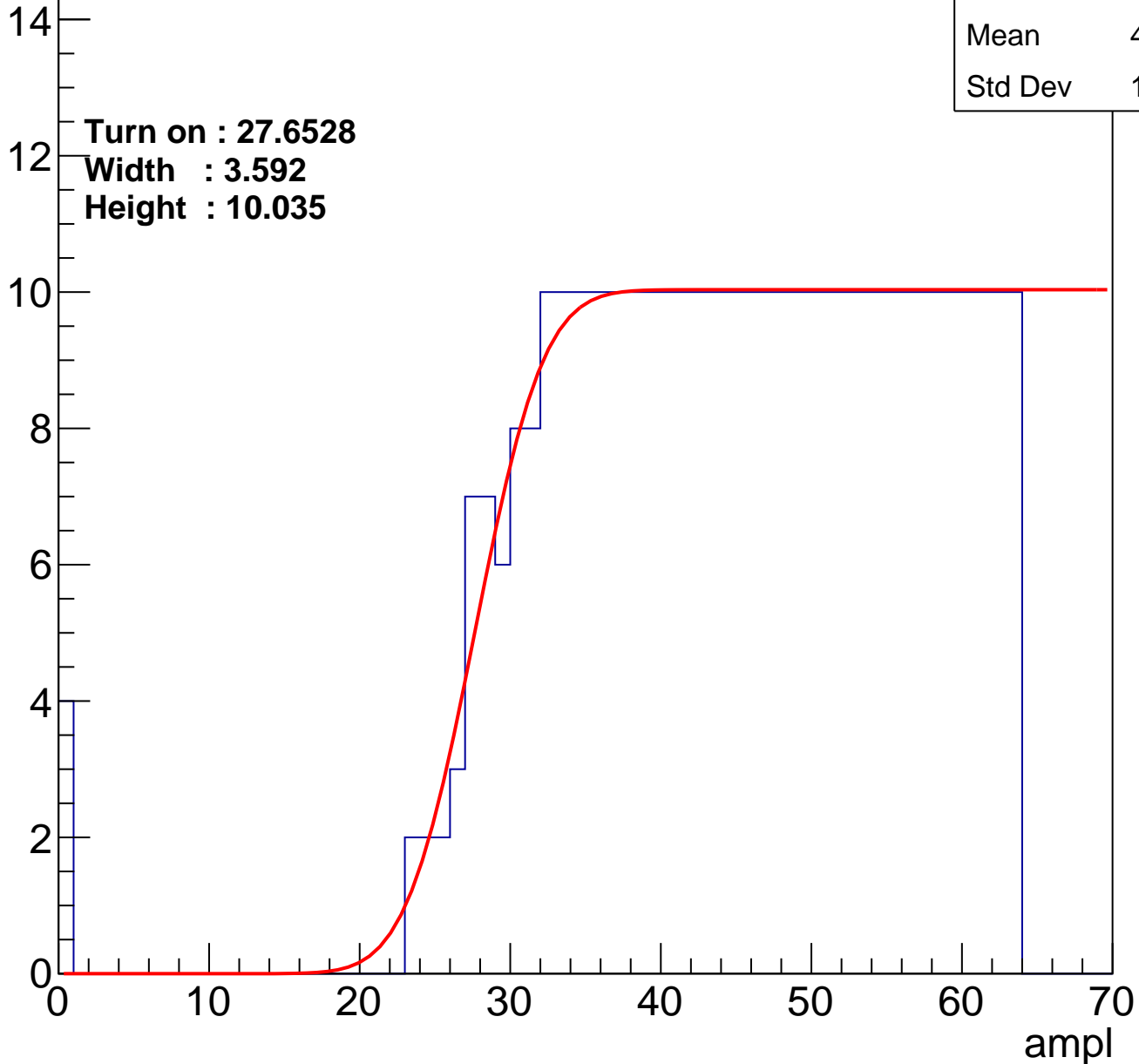
Entries	369
Mean	44.63
Std Dev	11.67

Turn on : 27.6528

Width : 3.592

Height : 10.035

Entry



# B1L000S, U2-ch109

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	360
Mean	45.27
Std Dev	10.97

Turn on : 28.3417

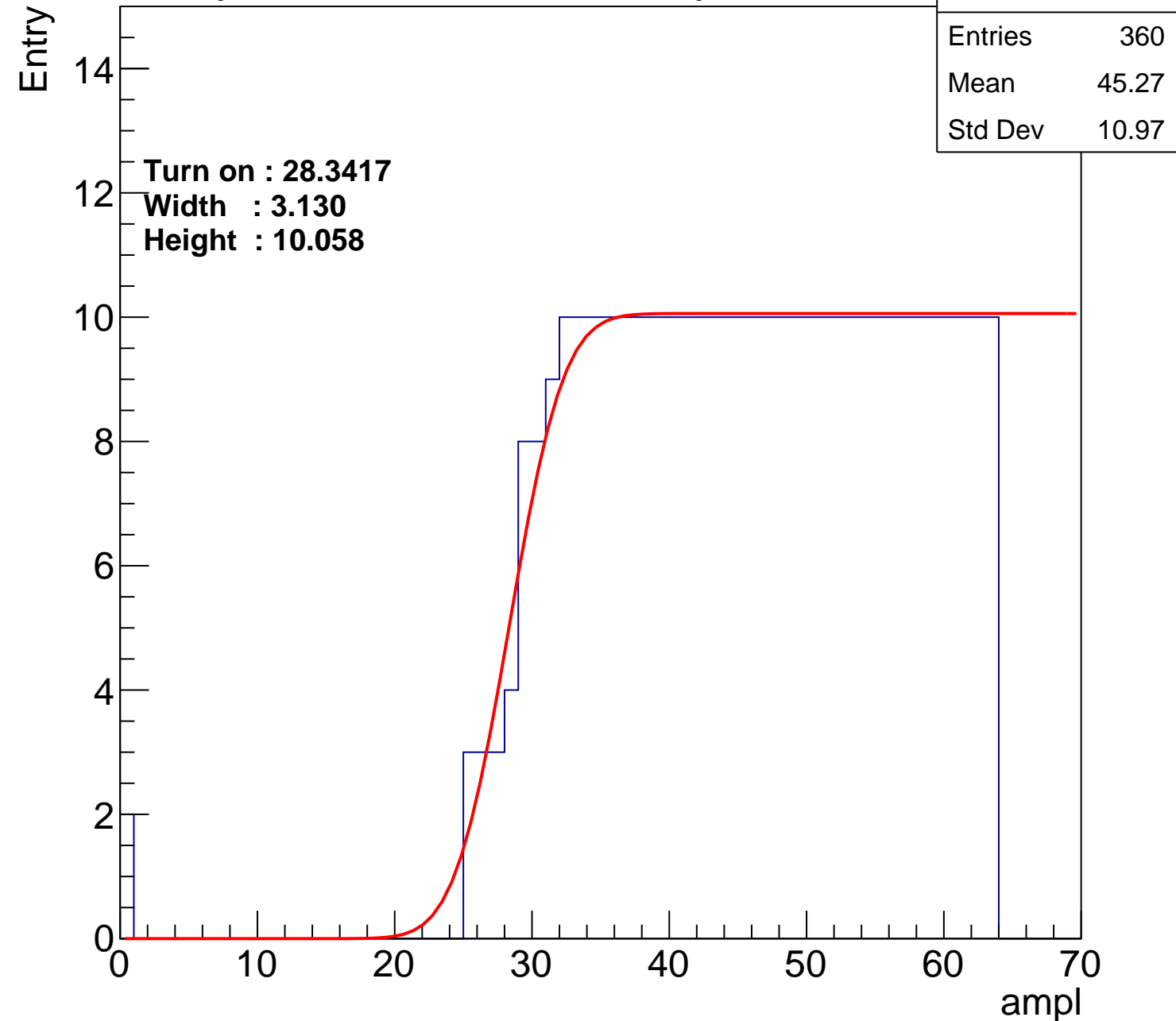
Width : 3.130

Height : 10.058

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch110

calib\_packv5\_042523\_0143.root, FC#3, port B3

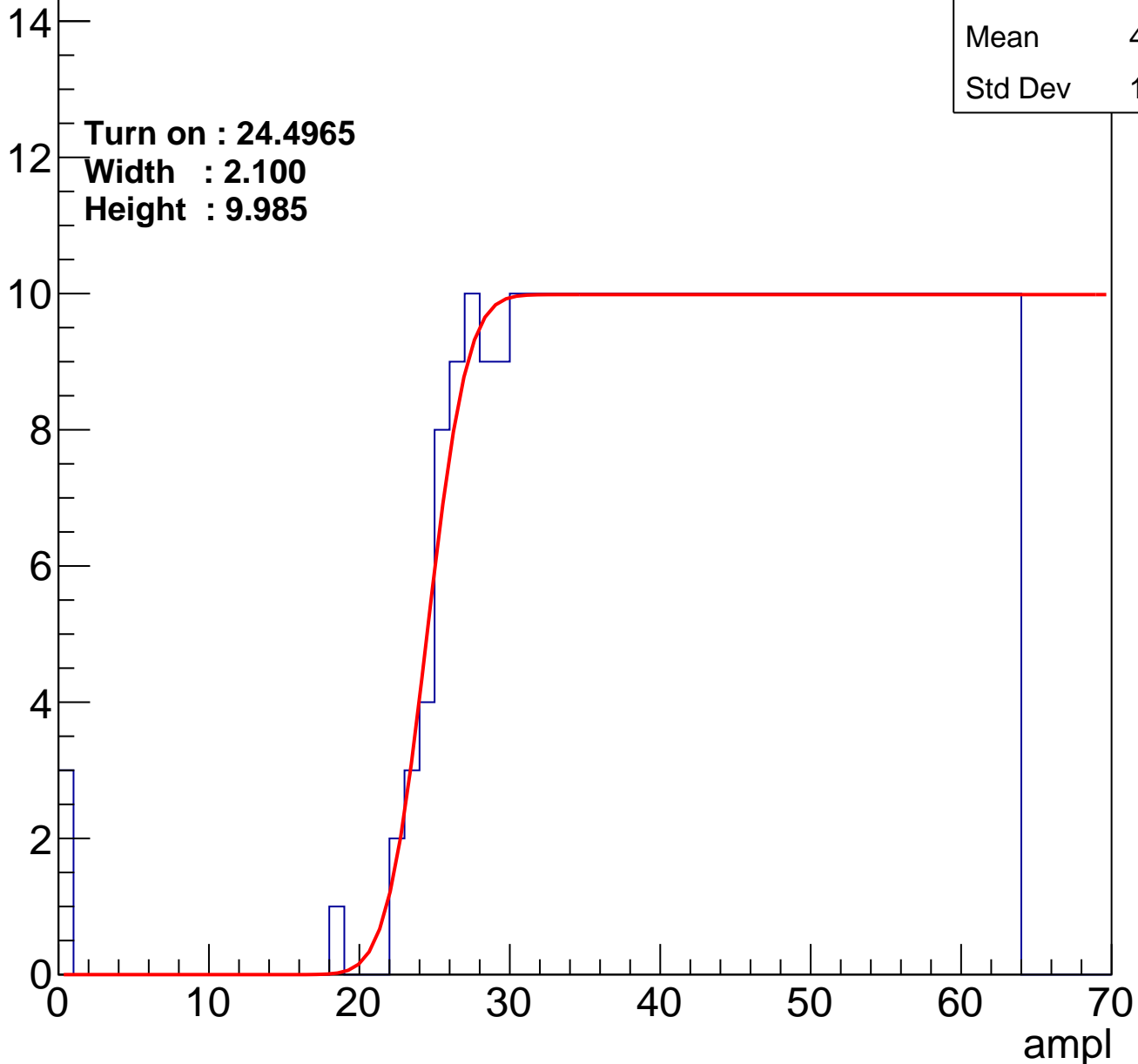
Entries	398
Mean	43.35
Std Dev	12.08

Turn on : 24.4965

Width : 2.100

Height : 9.985

Entry





# B1L000S, U2-ch111

calib\_packv5\_042523\_0143.root, FC#3, port B3

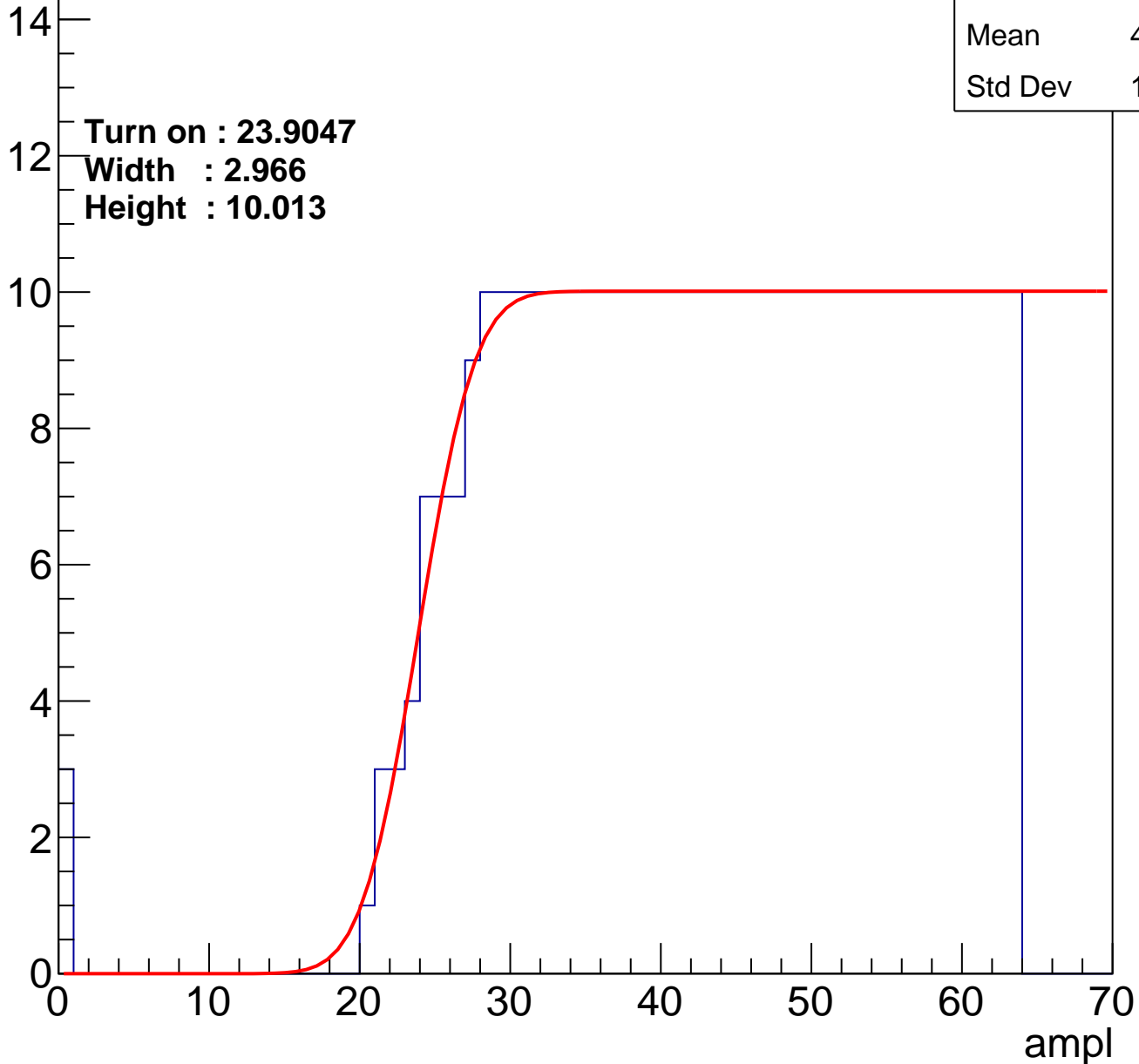
Entries	404
Mean	43.04
Std Dev	12.25

**Turn on : 23.9047**

**Width : 2.966**

**Height : 10.013**

Entry



# B1L000S, U2-ch112

calib\_packv5\_042523\_0143.root, FC#3, port B3

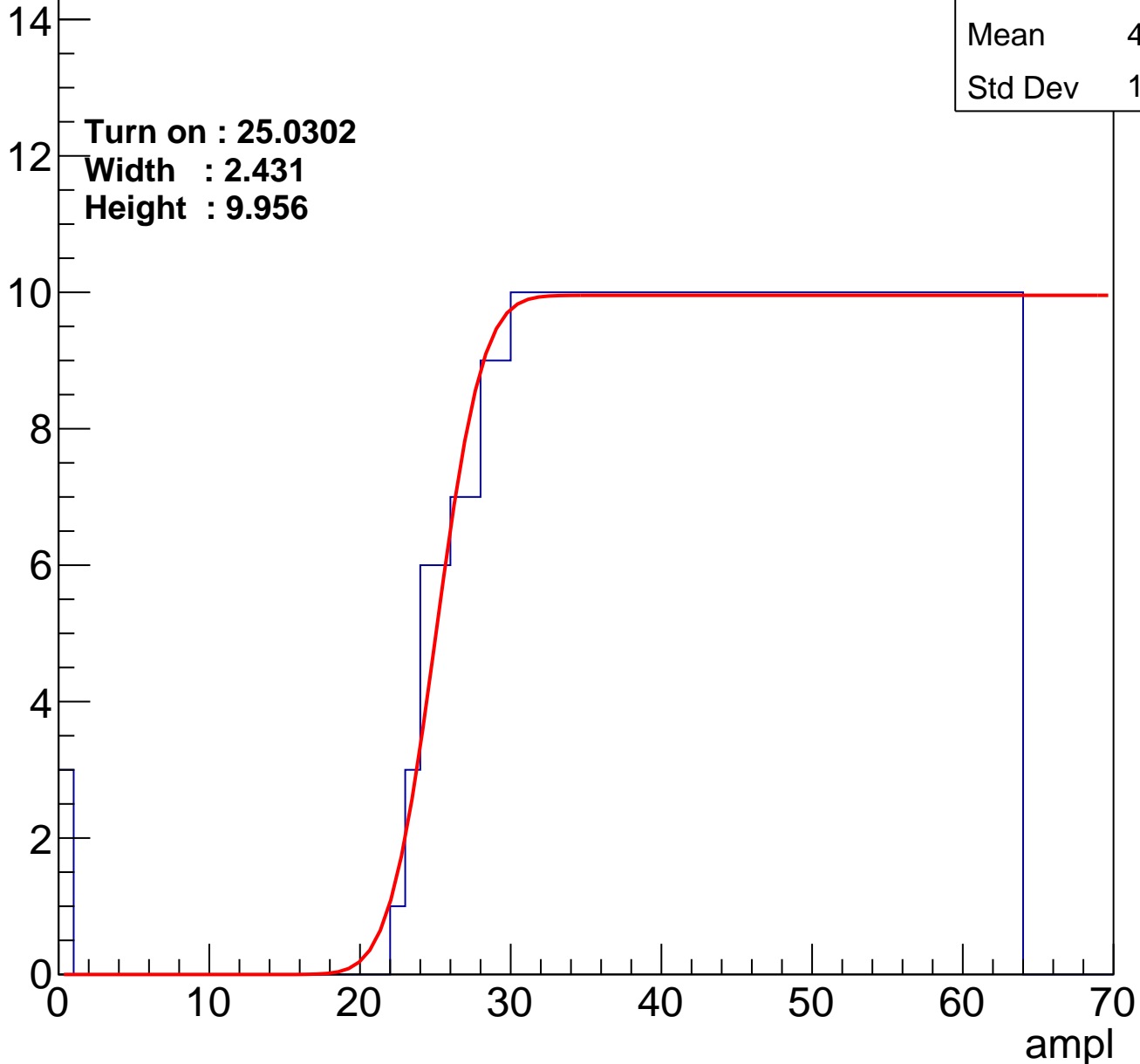
Entries	391
Mean	43.68
Std Dev	11.93

Turn on : 25.0302

Width : 2.431

Height : 9.956

Entry



# B1L000S, U2-ch113

calib\_packv5\_042523\_0143.root, FC#3, port B3

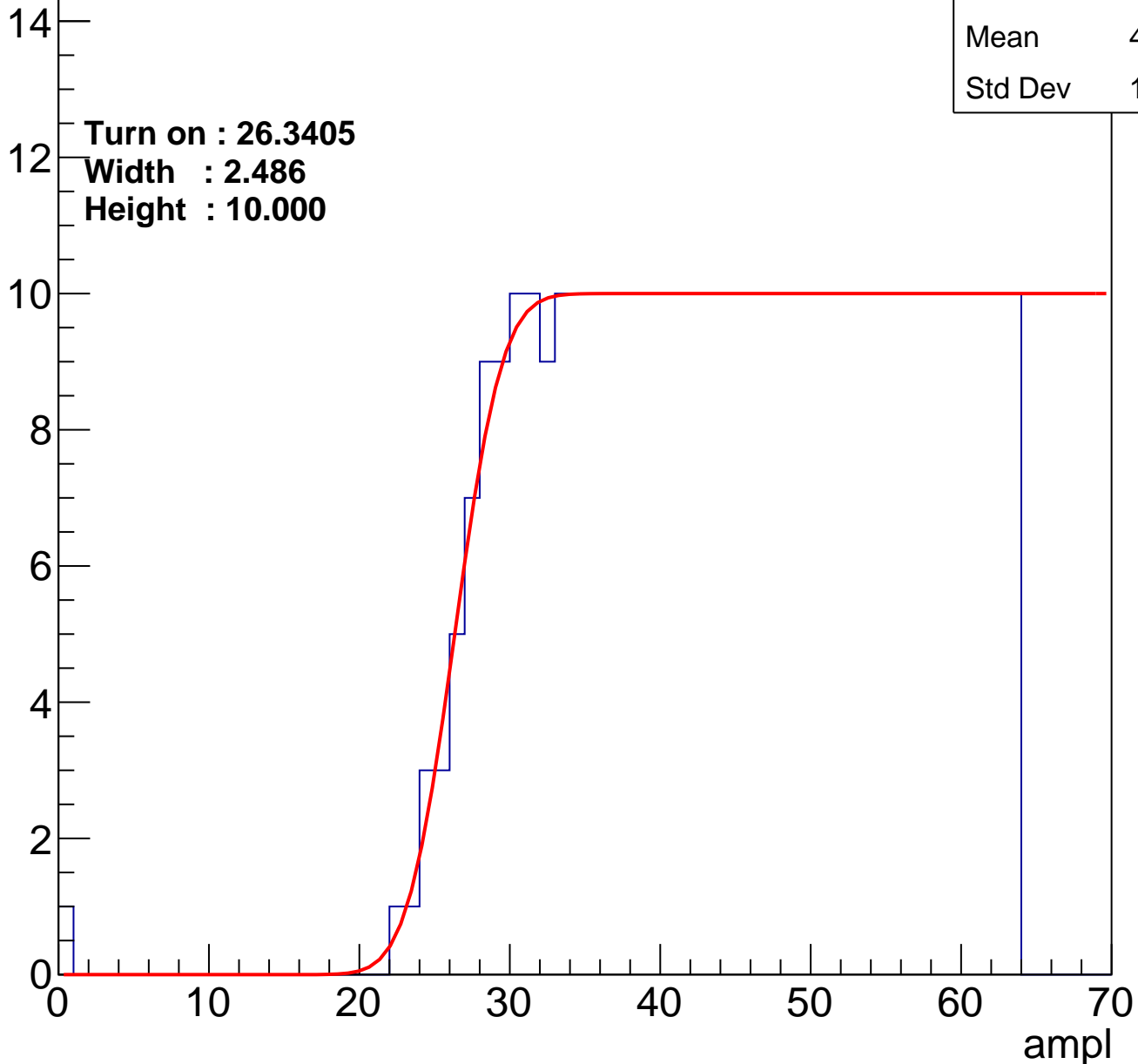
Entries	378
Mean	44.45
Std Dev	11.24

Turn on : 26.3405

Width : 2.486

Height : 10.000

Entry



# B1L000S, U2-ch114

calib\_packv5\_042523\_0143.root, FC#3, port B3

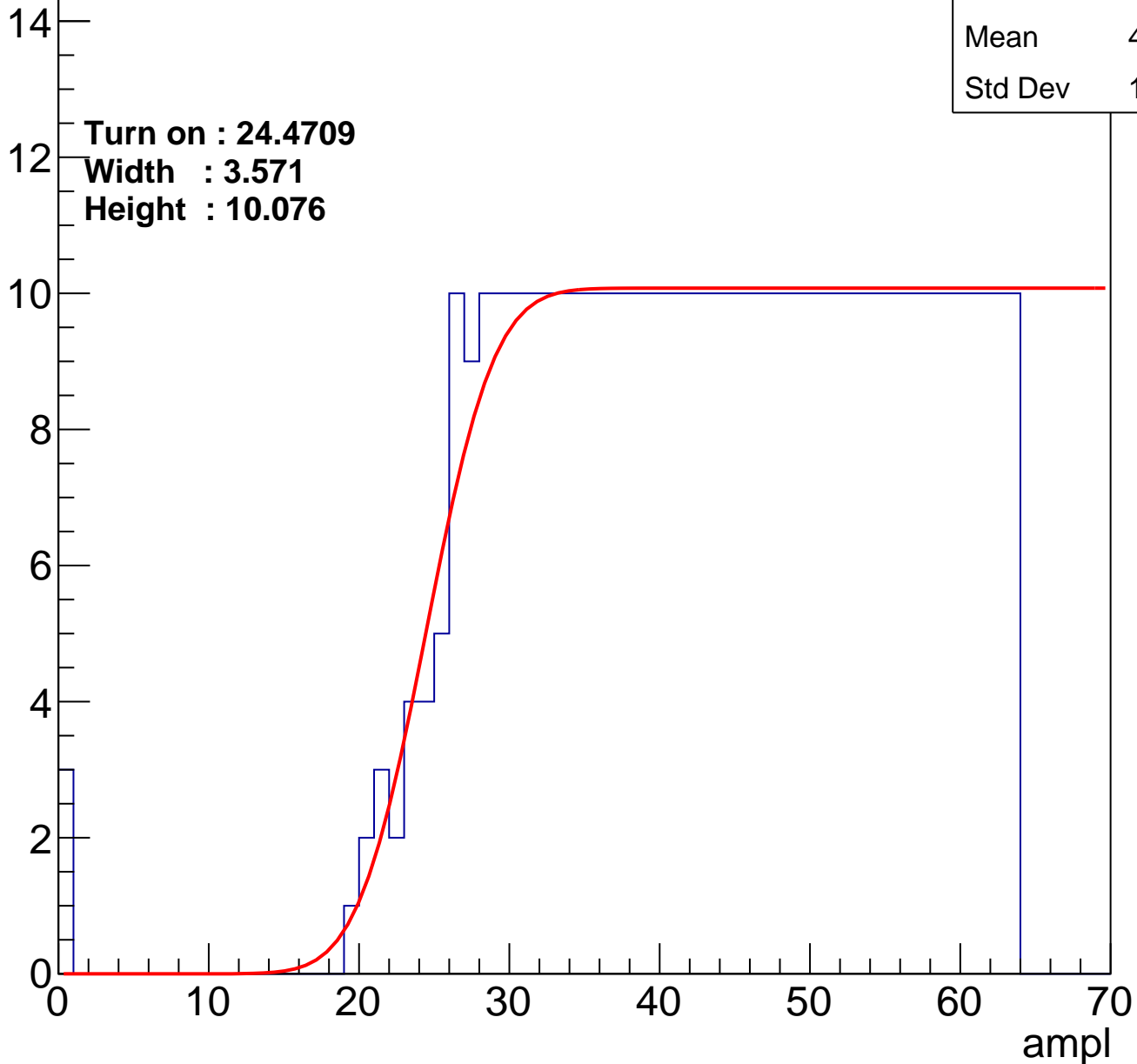
Entries	403
Mean	43.08
Std Dev	12.25

Turn on : 24.4709

Width : 3.571

Height : 10.076

Entry



# B1L000S, U2-ch115

calib\_packv5\_042523\_0143.root, FC#3, port B3

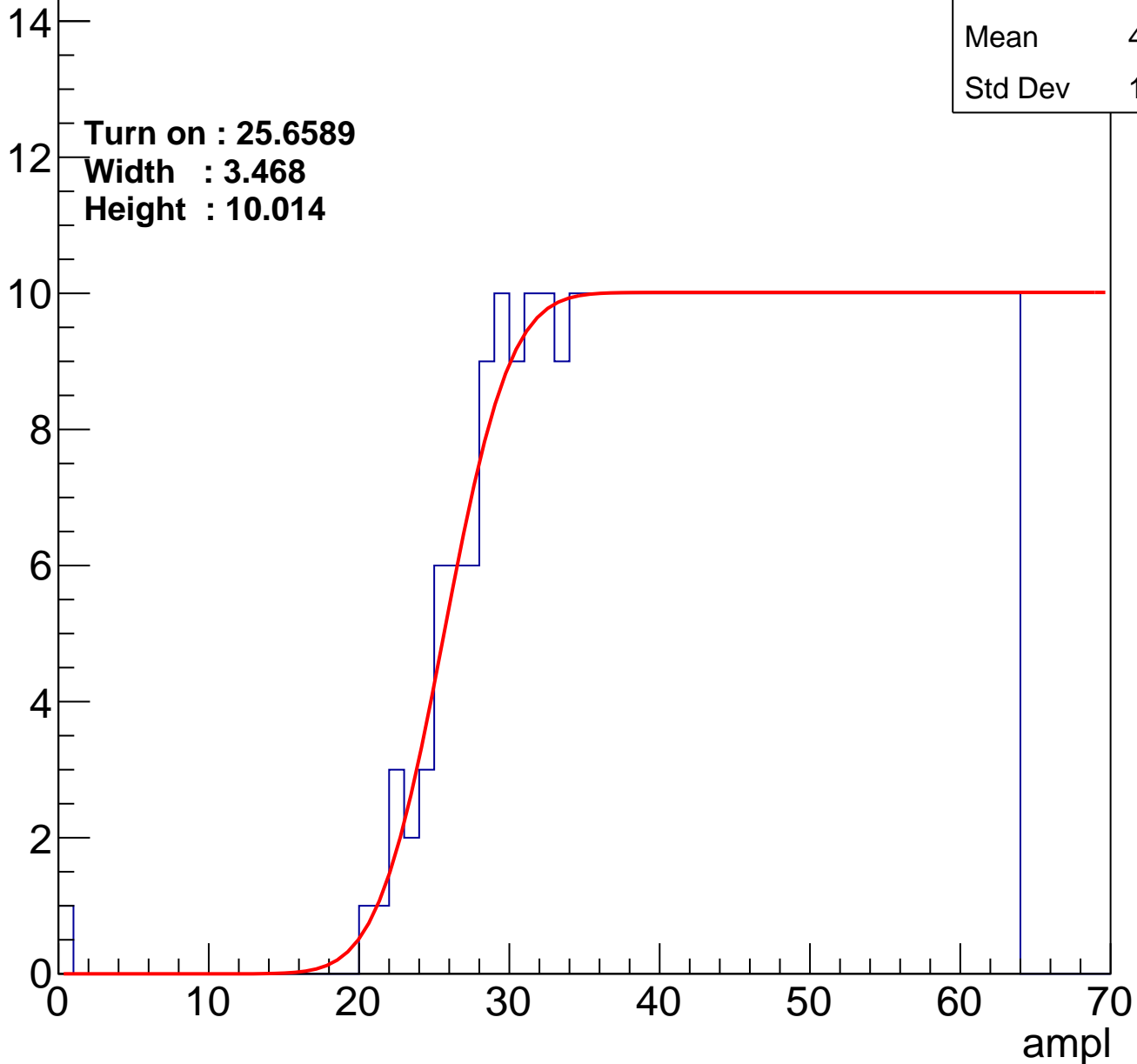
Entries	386
Mean	43.99
Std Dev	11.55

Turn on : 25.6589

Width : 3.468

Height : 10.014

Entry



# B1L000S, U2-ch116

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	401
Mean	43.3
Std Dev	11.88

**Turn on : 23.3374**

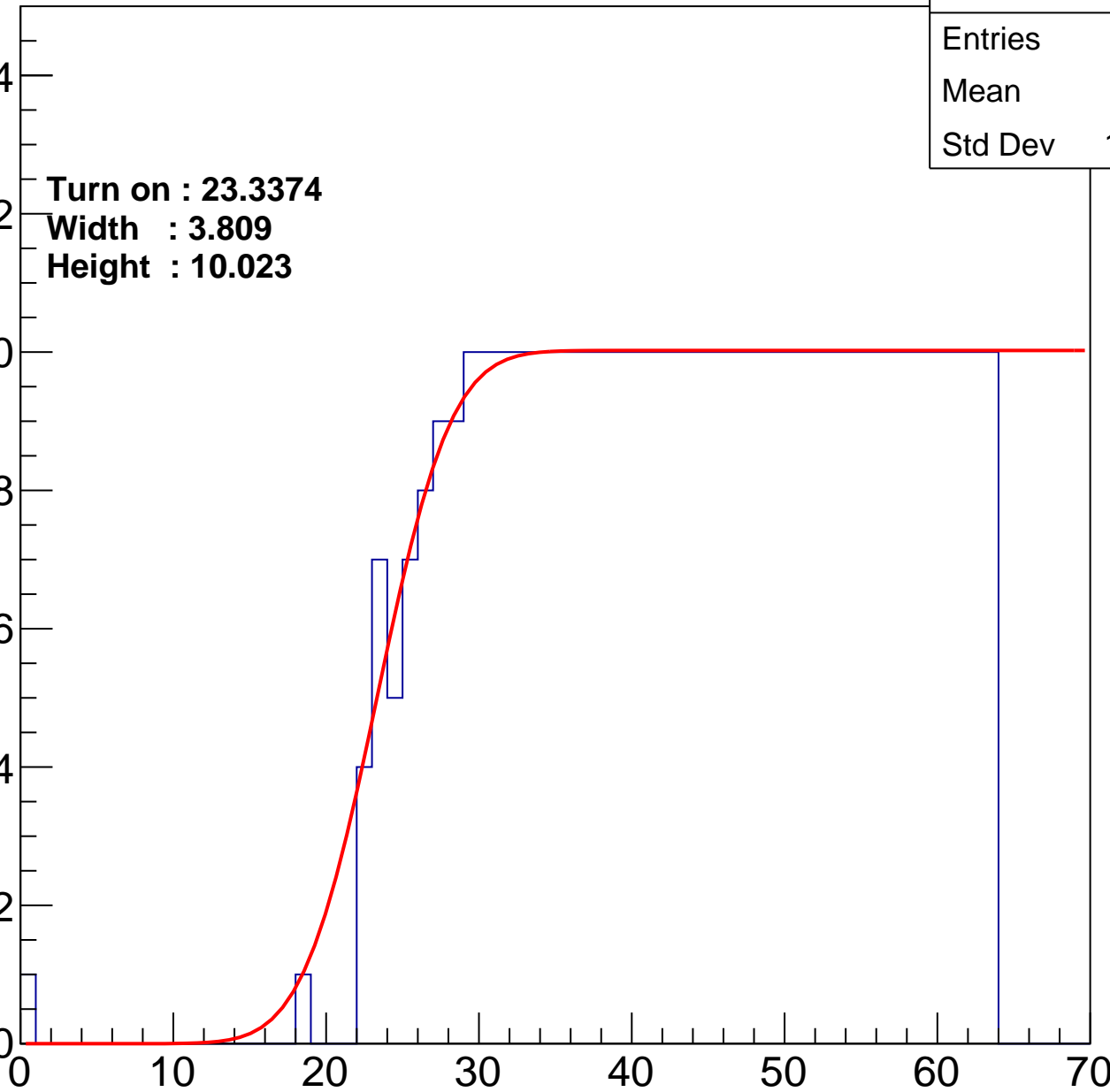
**Width : 3.809**

**Height : 10.023**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch117

calib\_packv5\_042523\_0143.root, FC#3, port B3

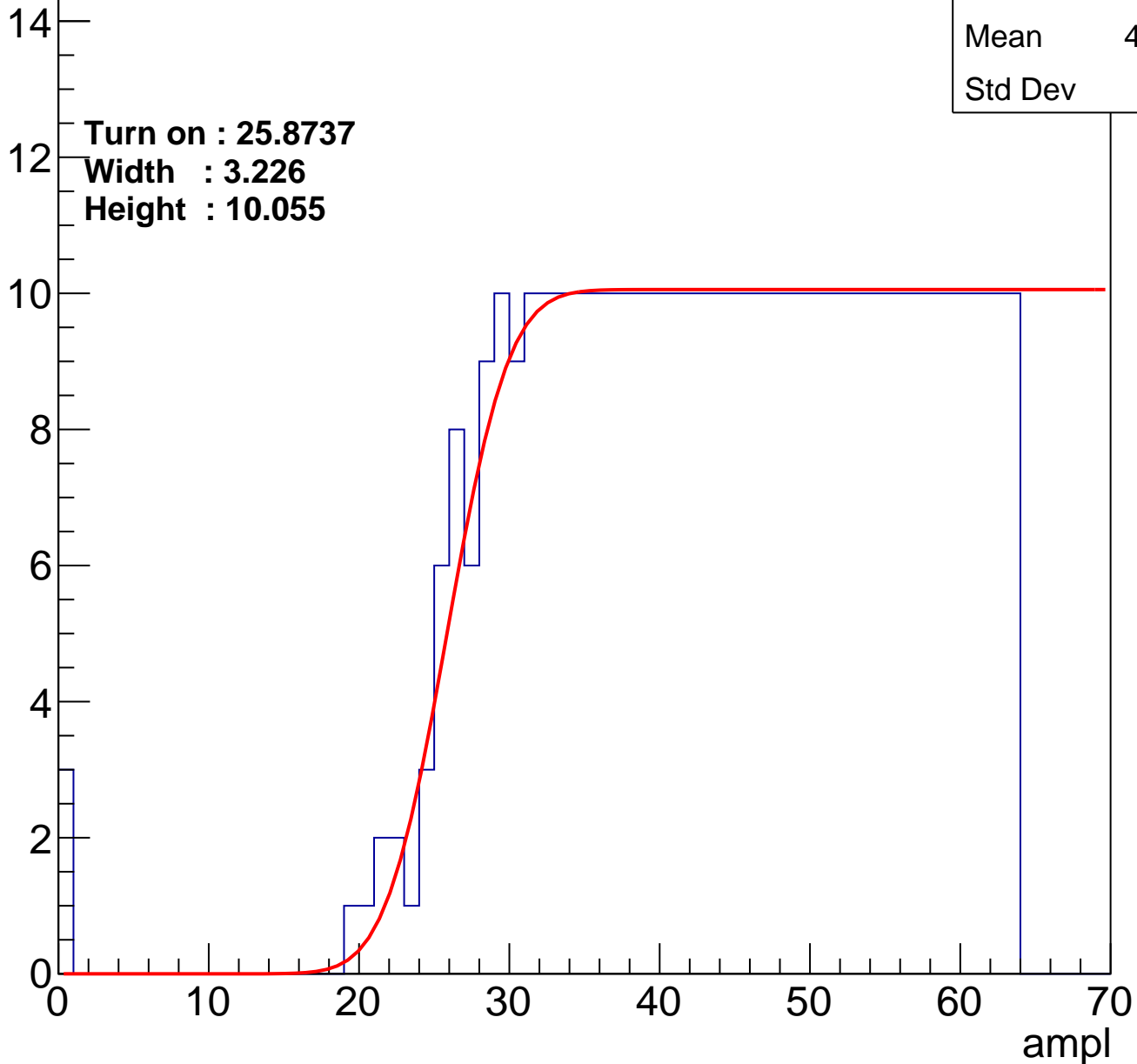
Entries	391
Mean	43.64
Std Dev	12

Turn on : 25.8737

Width : 3.226

Height : 10.055

Entry



# B1L000S, U2-ch118

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	388
Mean	43.81
Std Dev	11.88

Turn on : 25.6834

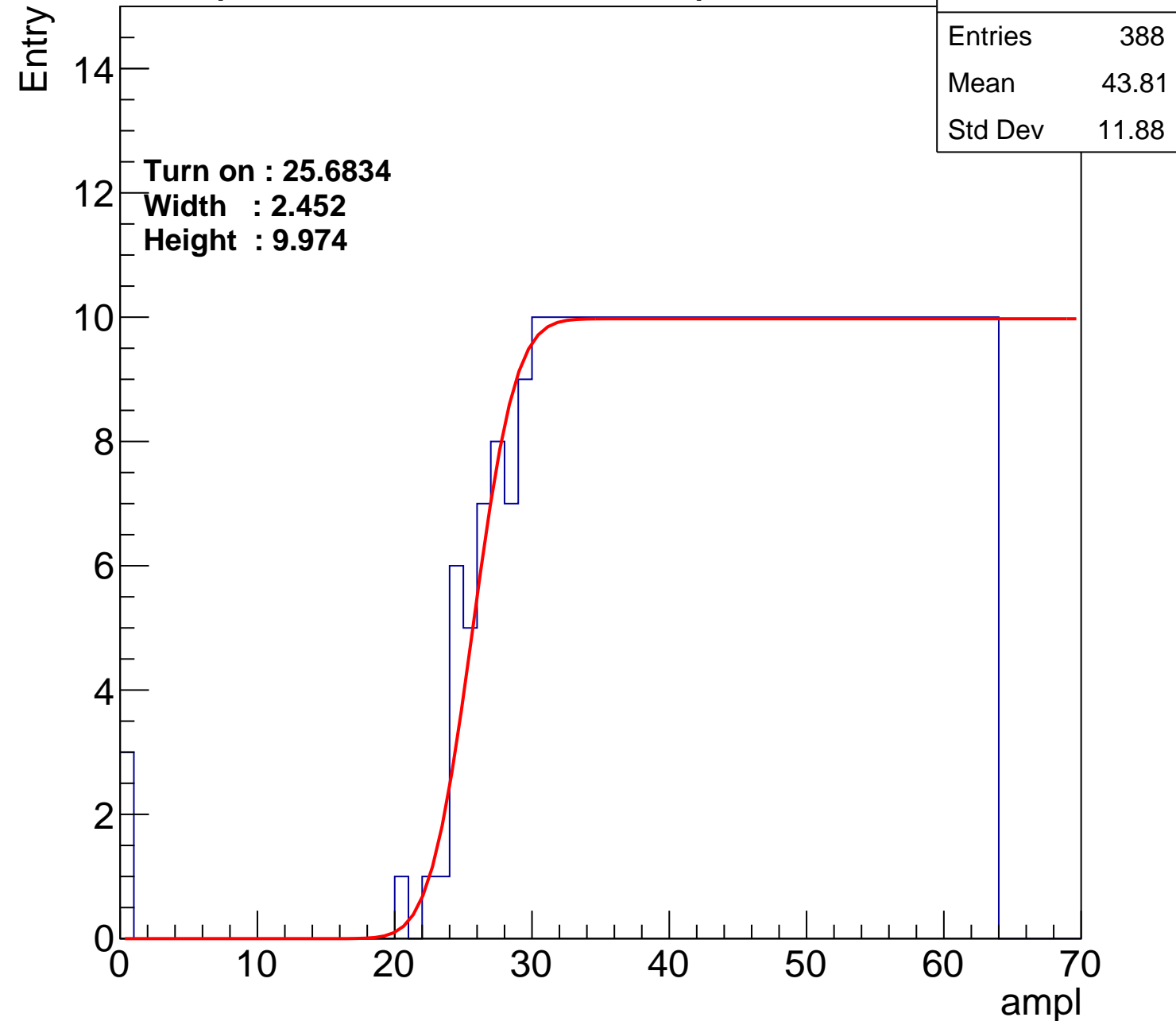
Width : 2.452

Height : 9.974

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L000S, U2-ch119

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	388
Mean	43.95
Std Dev	11.52

Turn on : 25.5546

Width : 3.472

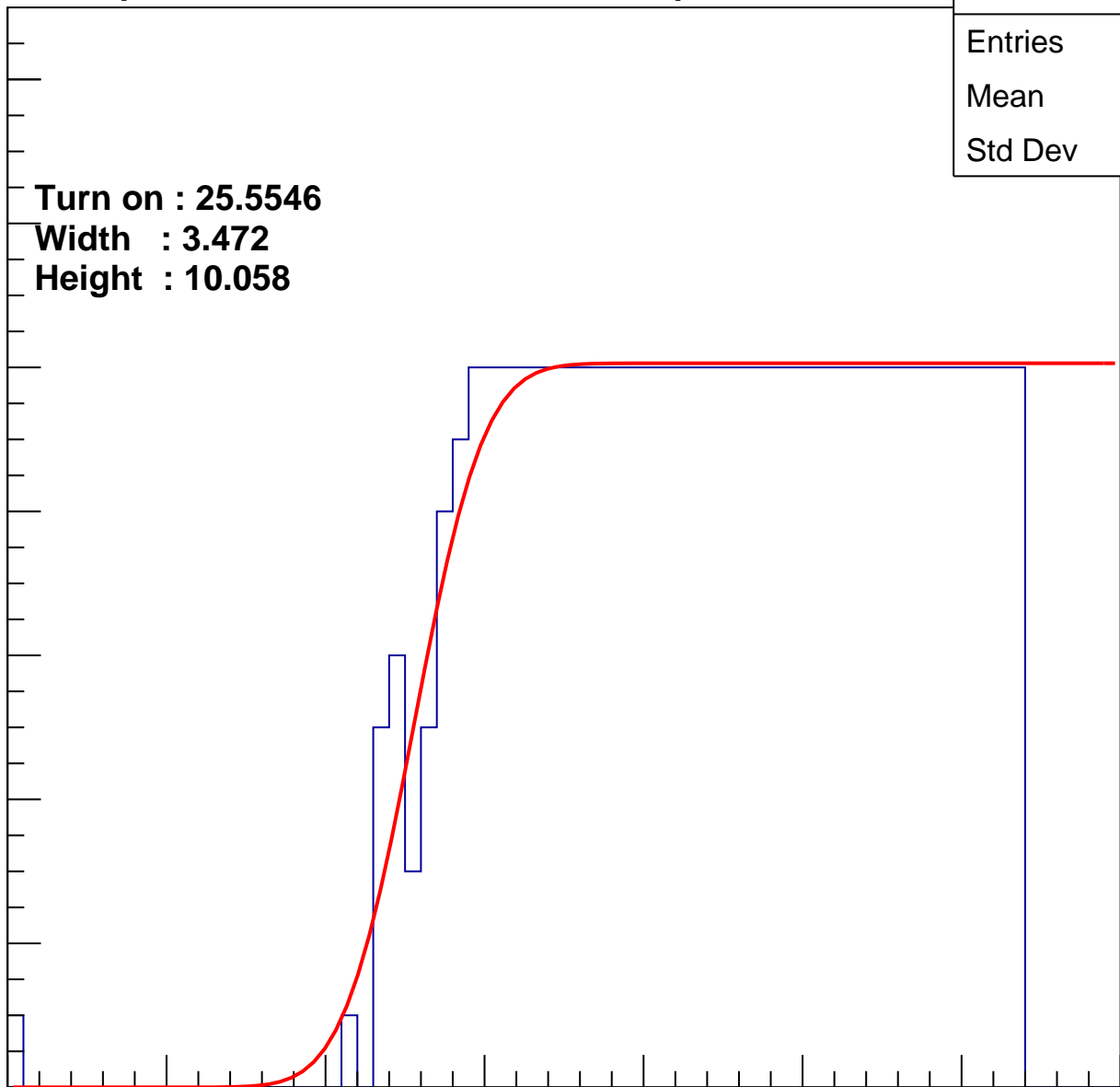
Height : 10.058

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L000S, U2-ch120

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	410
Mean	42.75
Std Dev	12.41

Turn on : 23.6030

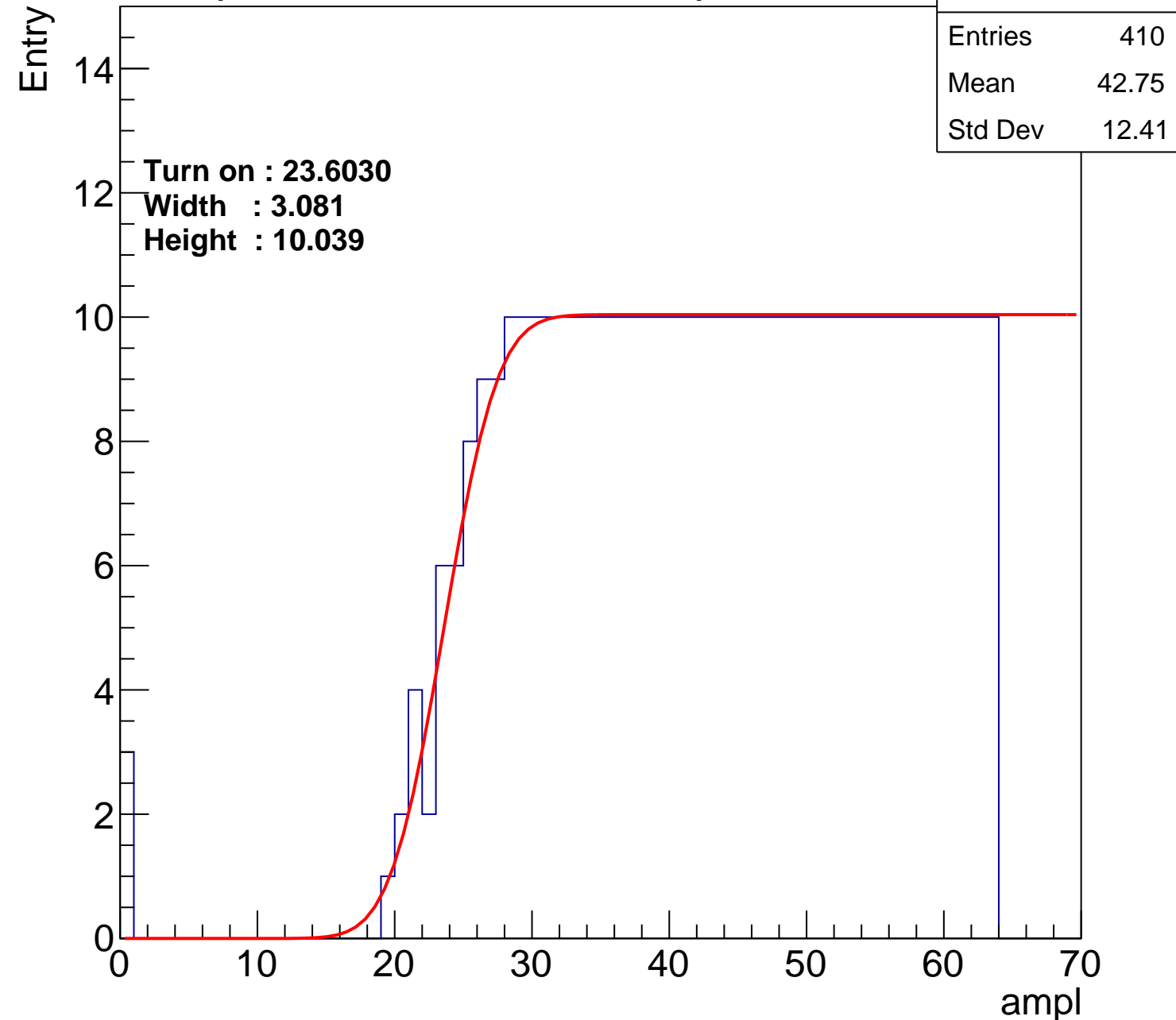
Width : 3.081

Height : 10.039

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch121

calib\_packv5\_042523\_0143.root, FC#3, port B3

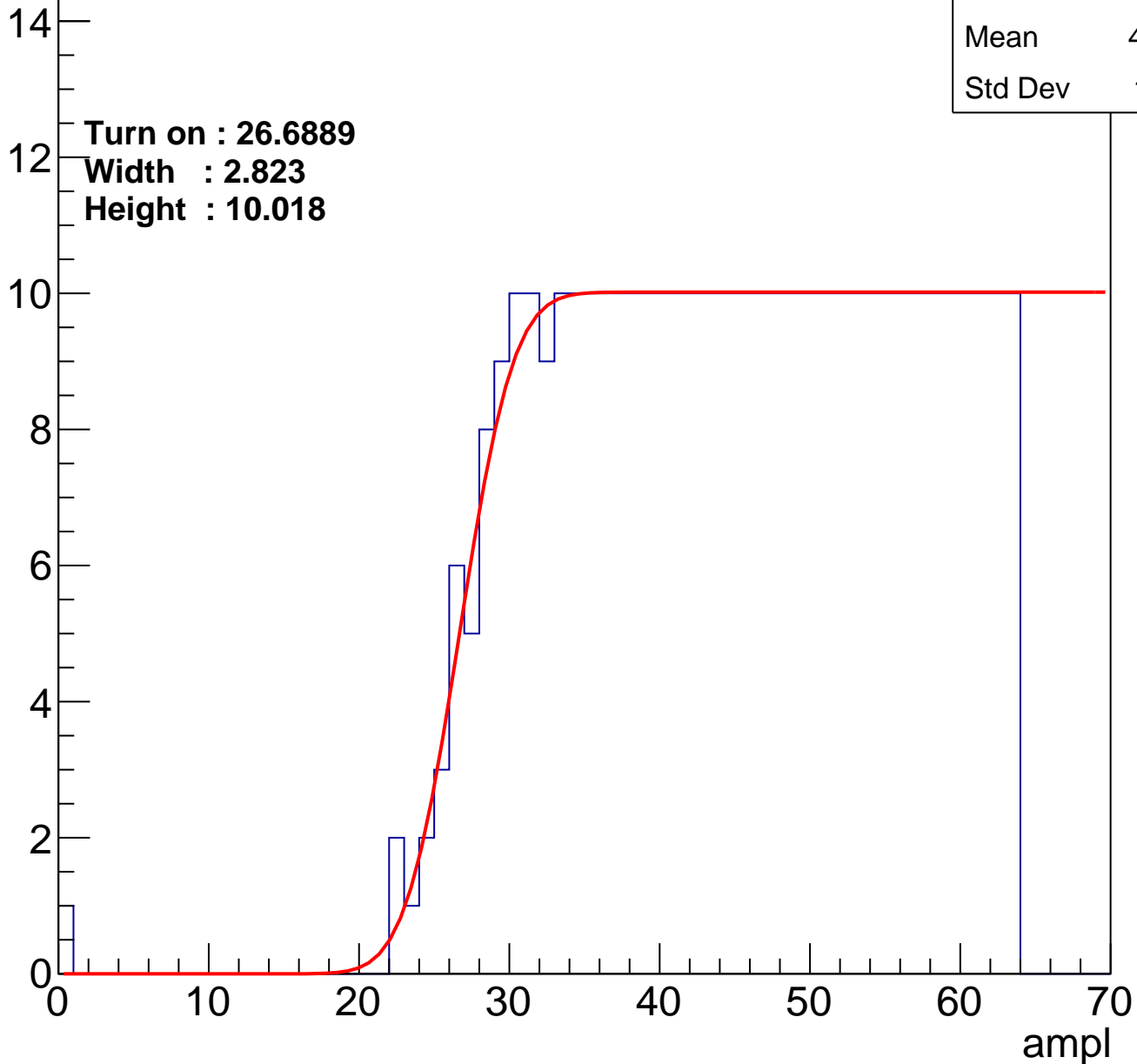
Entry

Entries	376
Mean	44.53
Std Dev	11.21

**Turn on : 26.6889**

**Width : 2.823**

**Height : 10.018**



# B1L000S, U2-ch122

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	393
Mean	43.59
Std Dev	11.9

Turn on : 25.5344

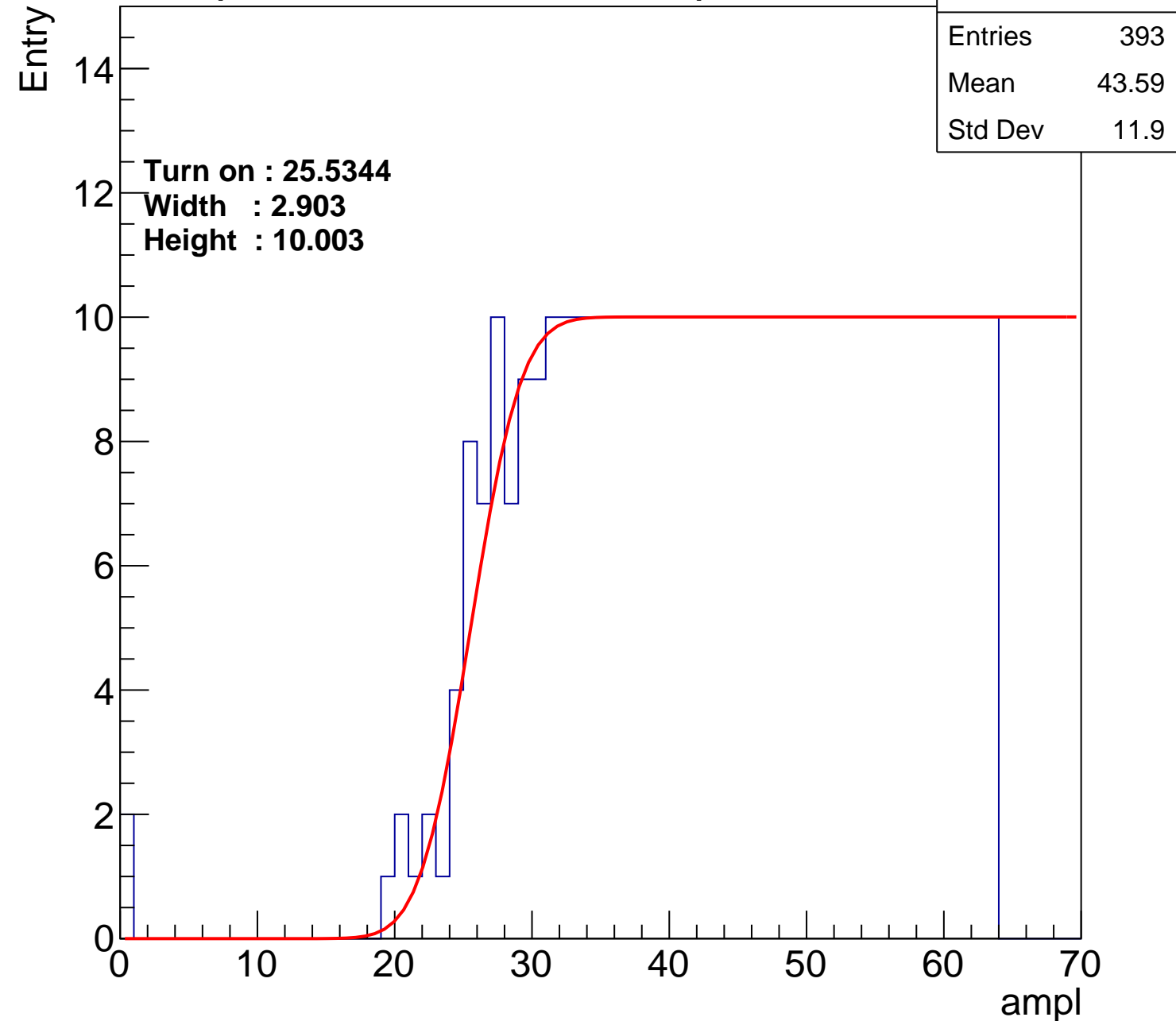
Width : 2.903

Height : 10.003

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch123

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	376
Mean	44.55
Std Dev	11.18

Turn on : 26.6294

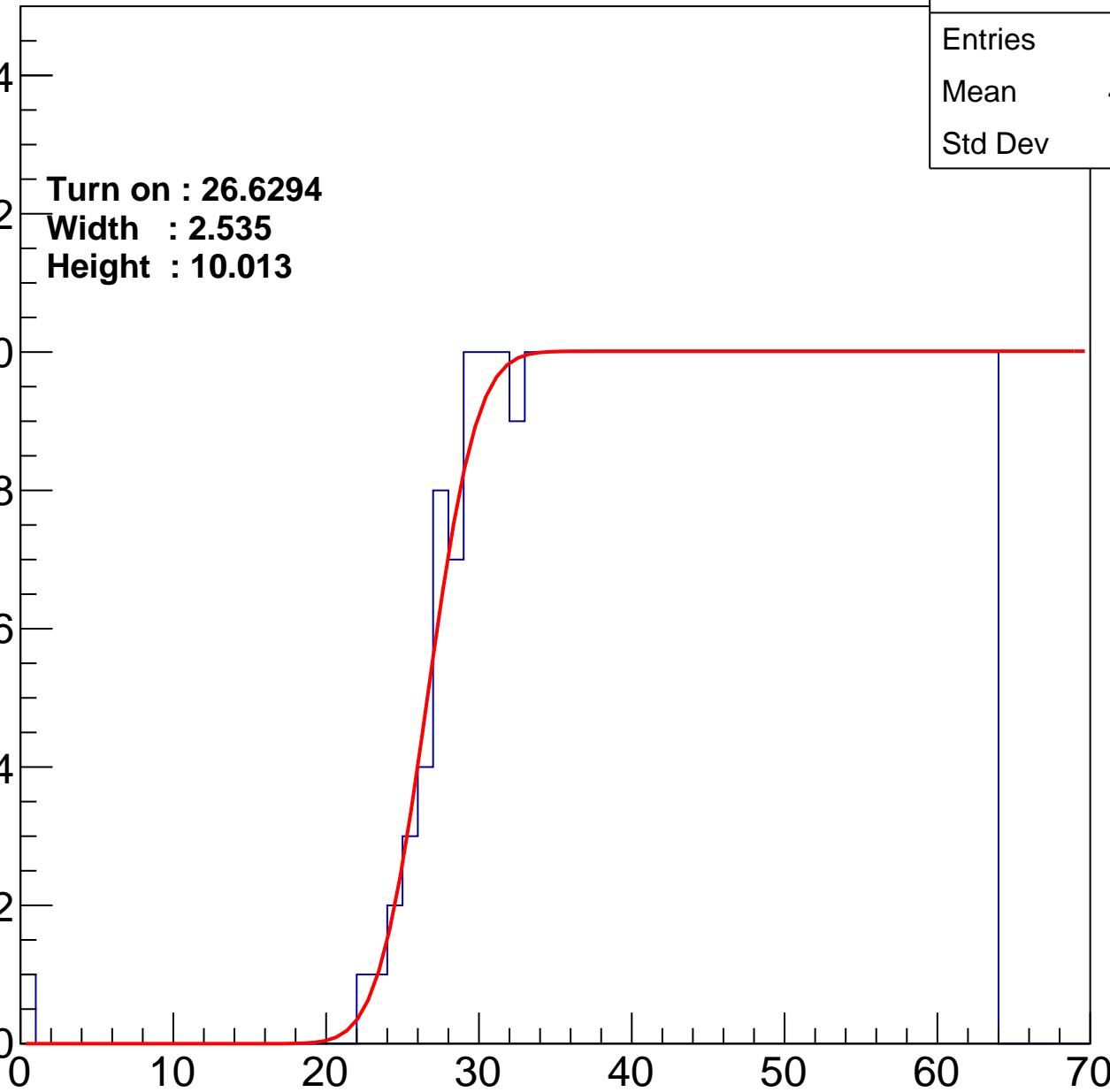
Width : 2.535

Height : 10.013

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch124

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	391
Mean	43.68
Std Dev	11.87

**Turn on : 25.6952**

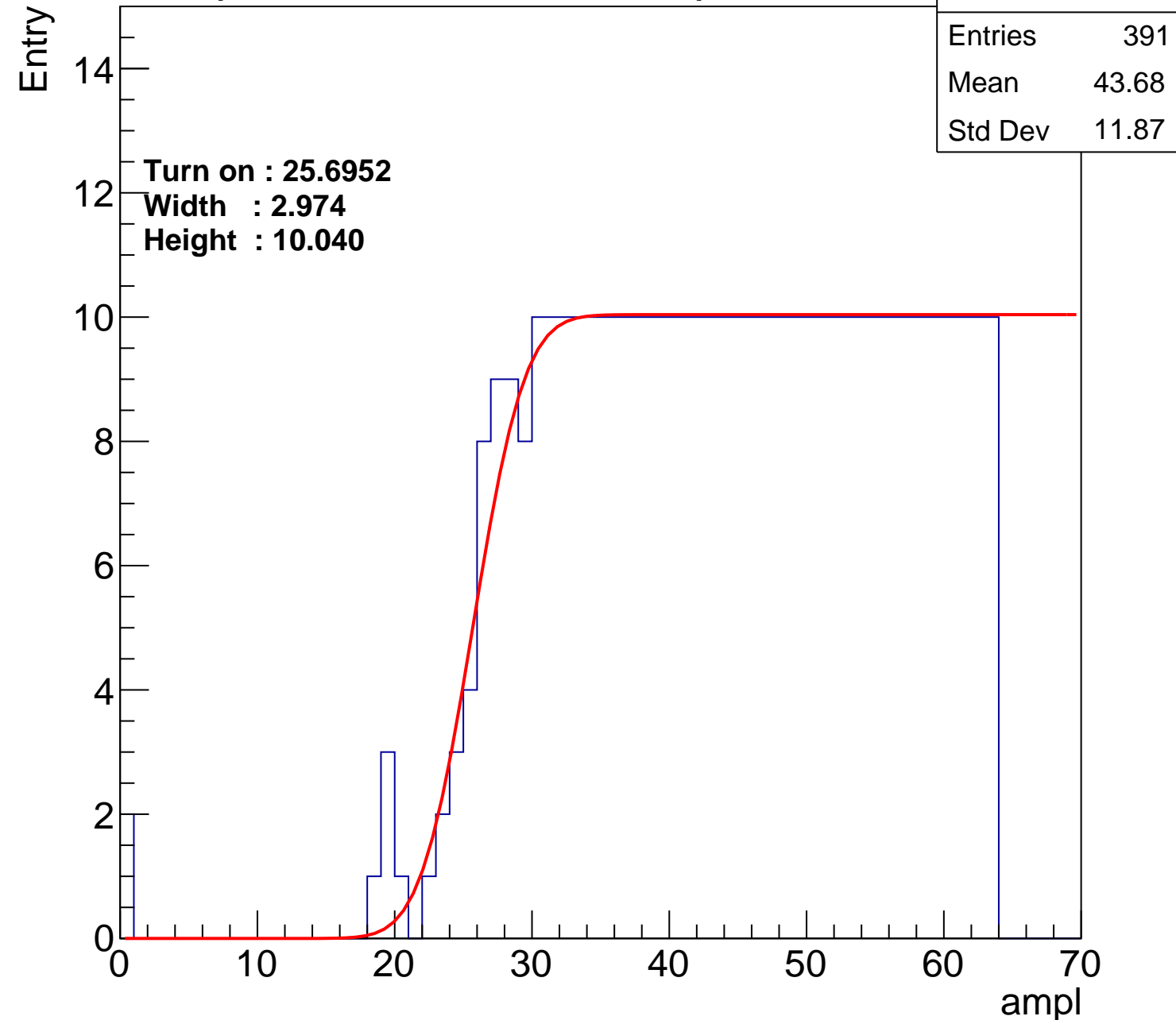
**Width : 2.974**

**Height : 10.040**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch125

calib\_packv5\_042523\_0143.root, FC#3, port B3

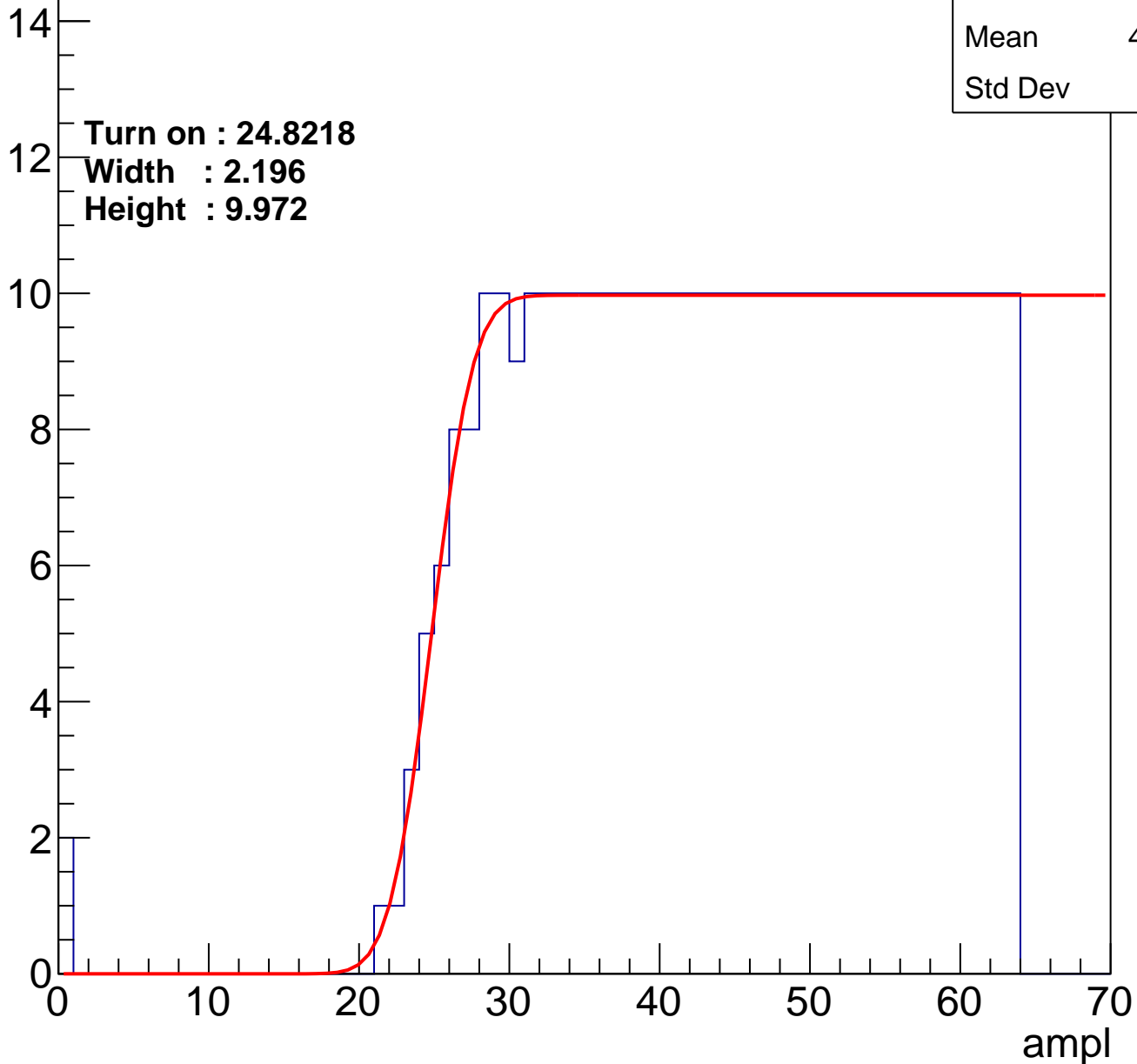
Entries	393
Mean	43.65
Std Dev	11.8

Turn on : 24.8218

Width : 2.196

Height : 9.972

Entry



# B1L000S, U2-ch126

calib\_packv5\_042523\_0143.root, FC#3, port B3

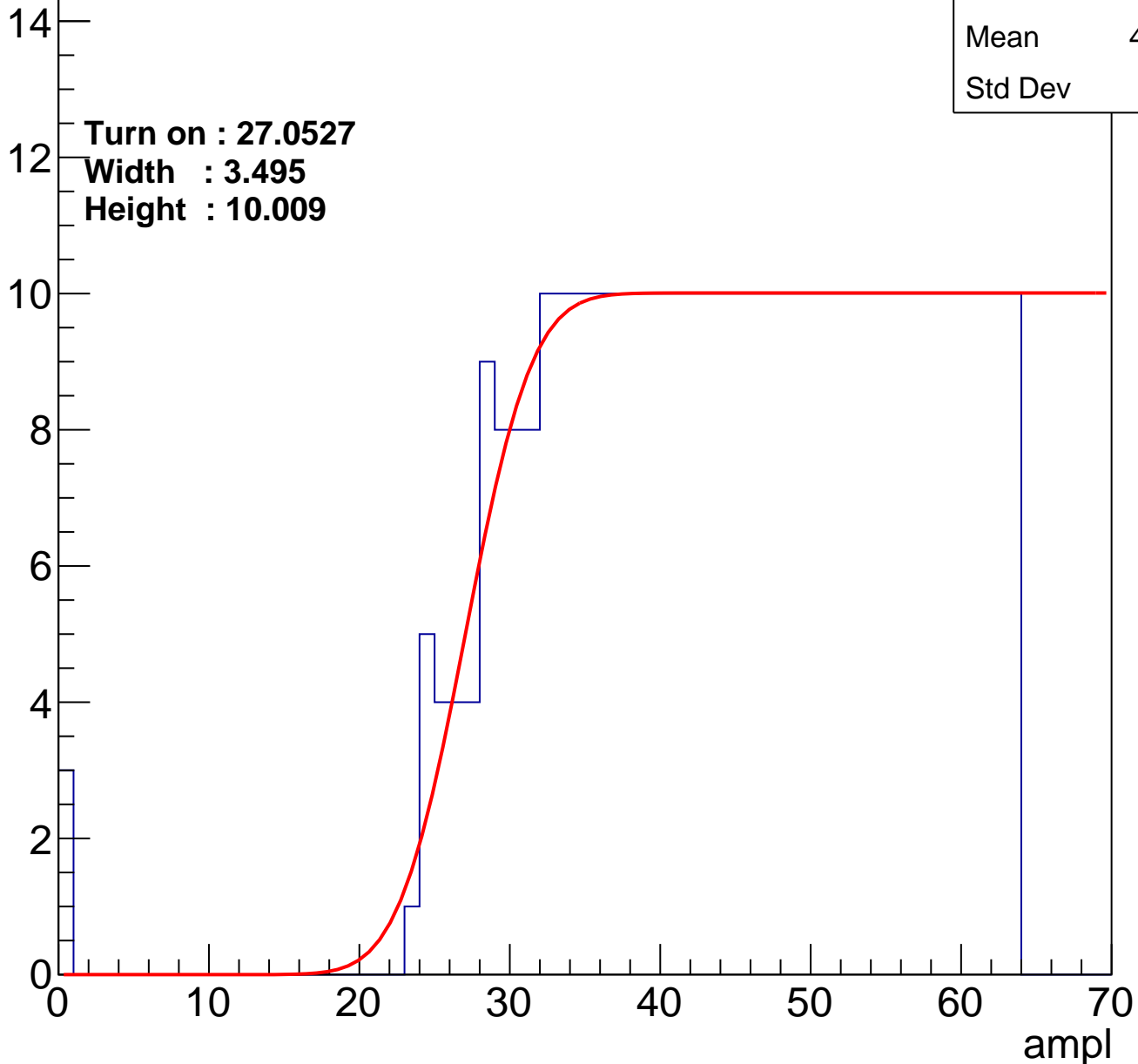
Entries	374
Mean	44.46
Std Dev	11.6

Turn on : 27.0527

Width : 3.495

Height : 10.009

Entry





# B1L000S, U2-ch127

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	389
Mean	43.72
Std Dev	12.04

Turn on : 25.6777

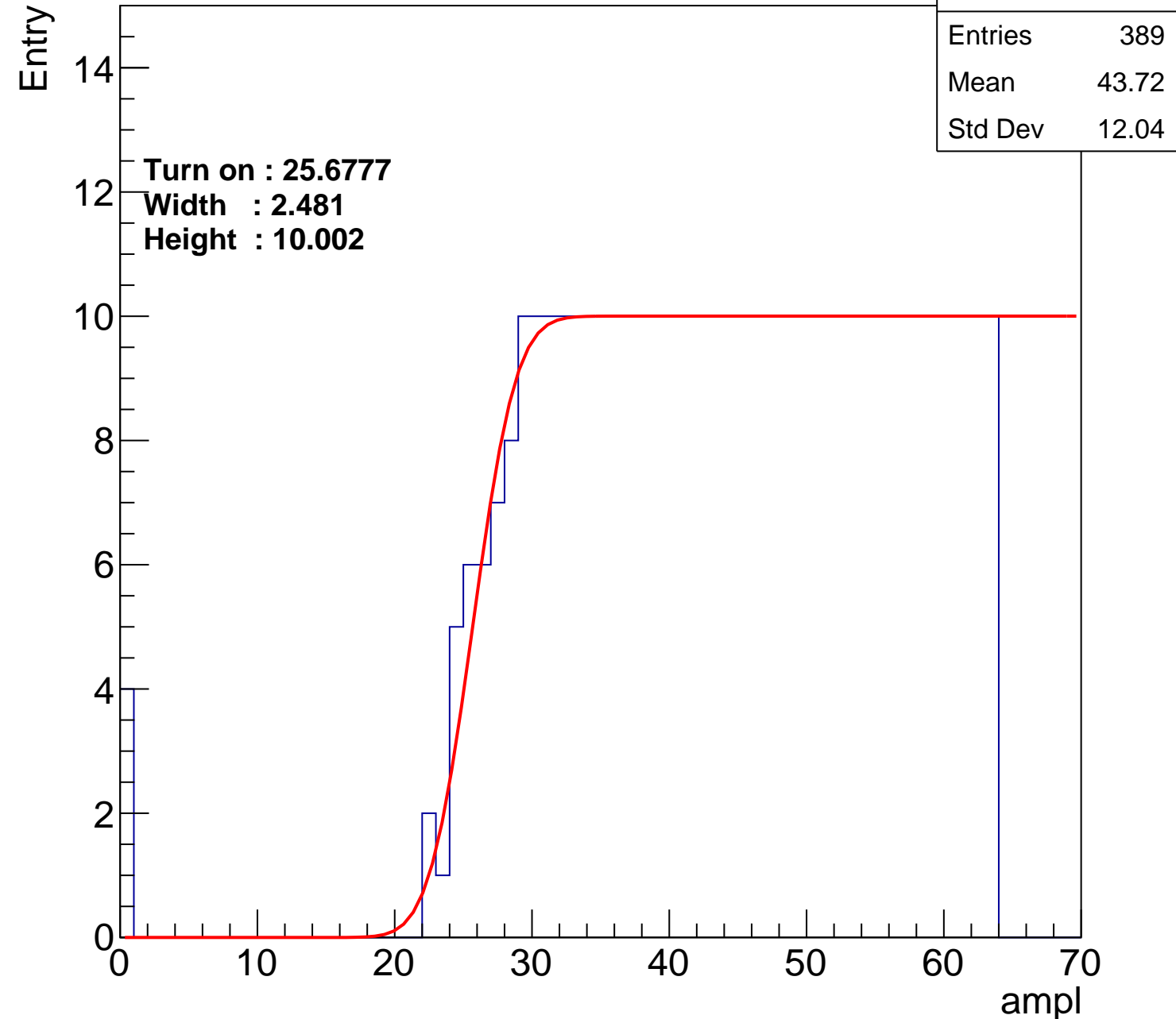
Width : 2.481

Height : 10.002

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L000S, U2-ch127

calib\_packv5\_042523\_0143.root, FC#3, port B3

Entries	389
Mean	43.72
Std Dev	12.04

Turn on : 25.6777

Width : 2.481

Height : 10.002

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

