

B1L101S, U20-ch0

calib_packv5_042523_0143.root, FC#0, port D2

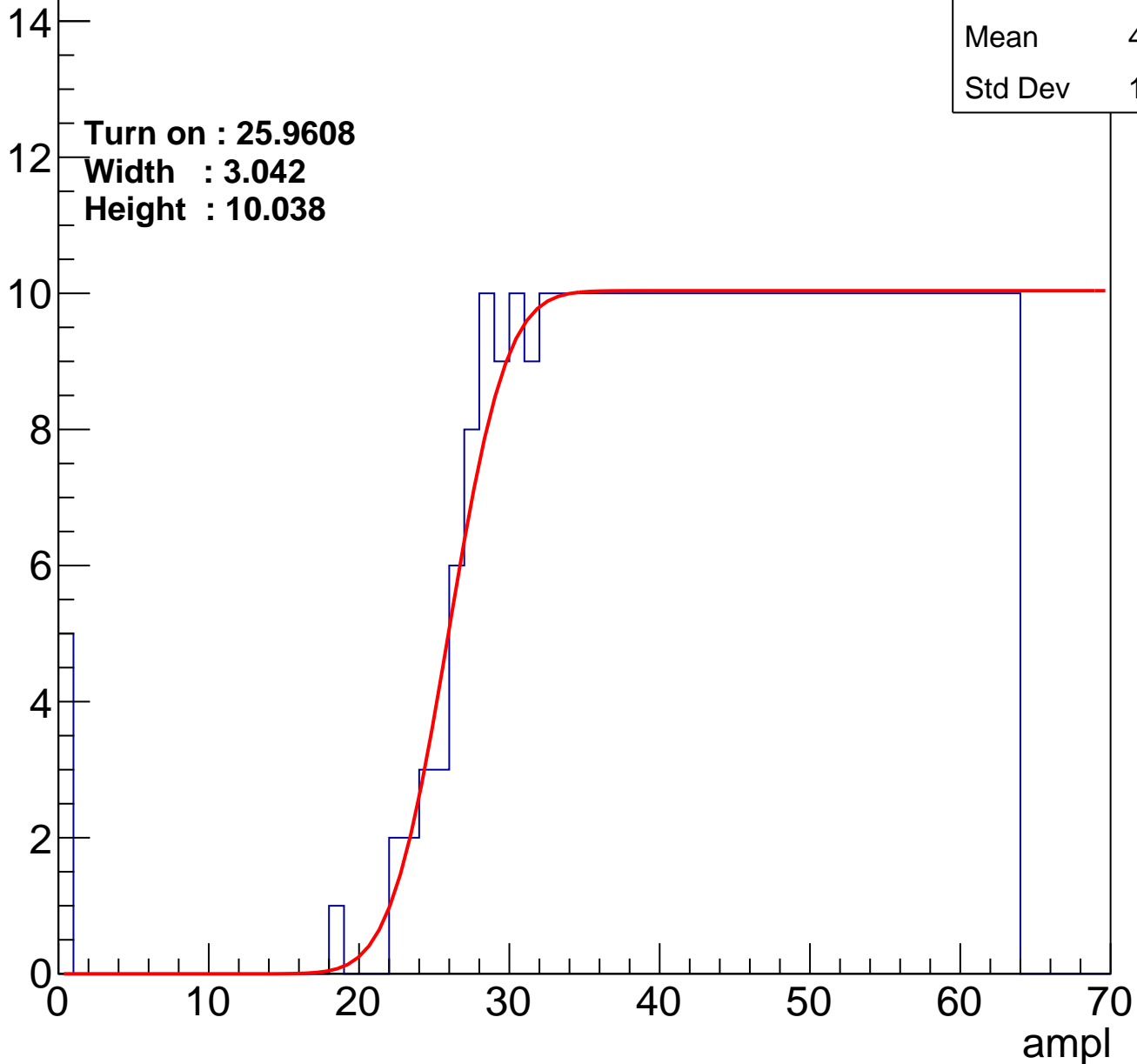
Entries	388
Mean	43.68
Std Dev	12.22

Turn on : 25.9608

Width : 3.042

Height : 10.038

Entry



B1L101S, U20-ch1

calib_packv5_042523_0143.root, FC#0, port D2

Entries	357
Mean	45.49
Std Dev	10.67

Turn on : 28.2088

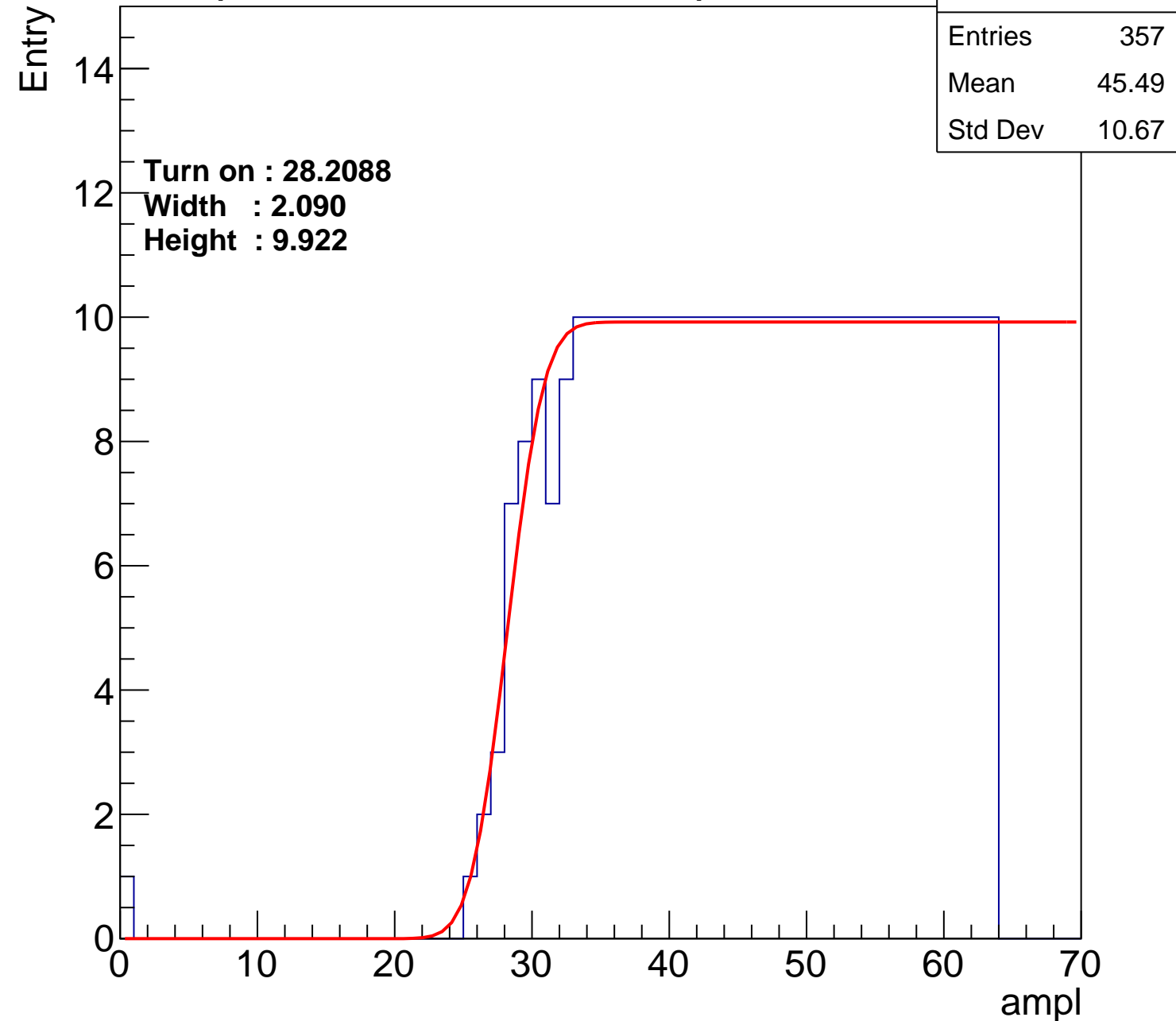
Width : 2.090

Height : 9.922

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch2

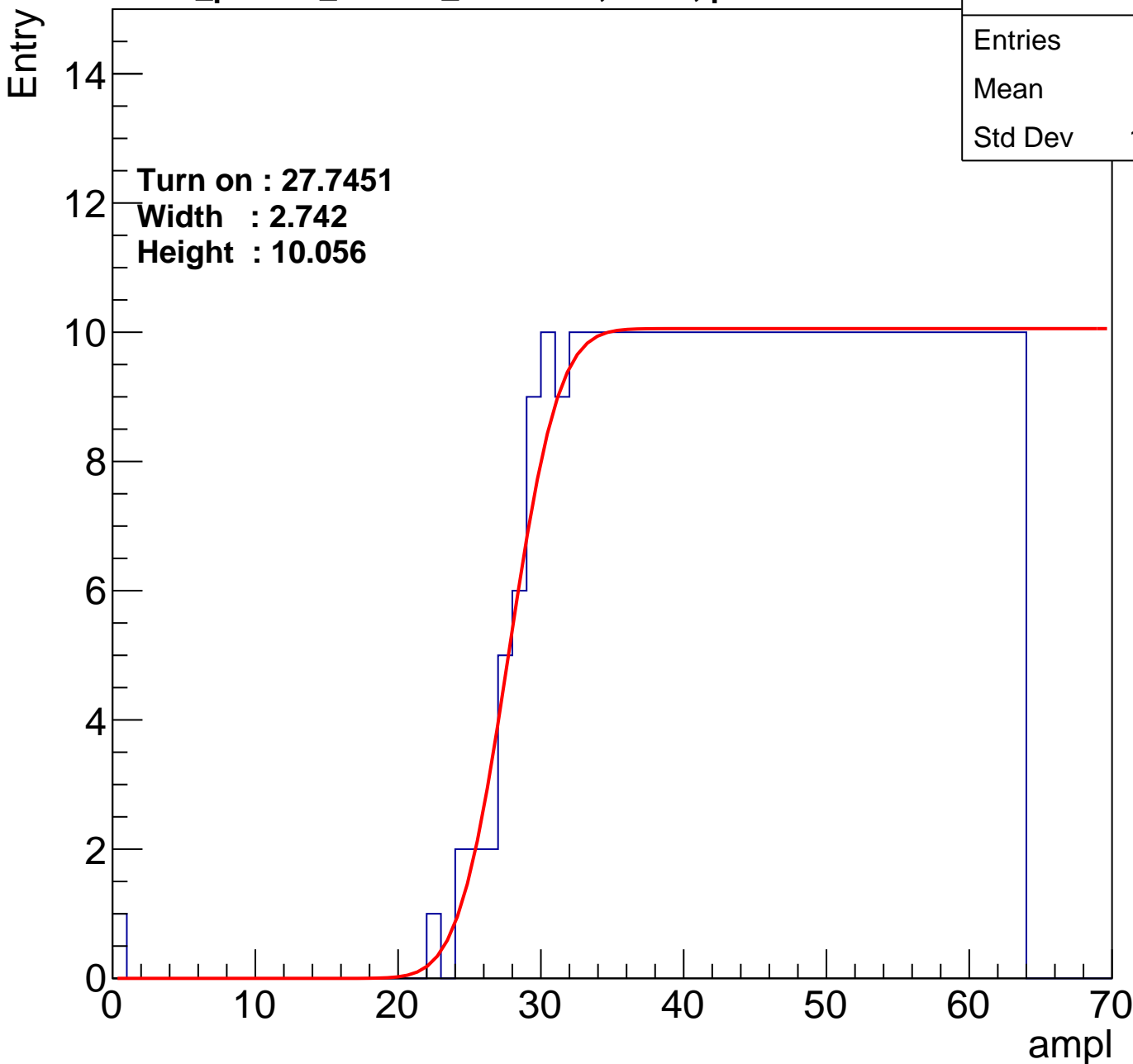
calib_packv5_042523_0143.root, FC#0, port D2

Turn on : 27.7451

Width : 2.742

Height : 10.056

Entries	367
Mean	45
Std Dev	10.94



B1L101S, U20-ch3

calib_packv5_042523_0143.root, FC#0, port D2

Entries	372
Mean	44.51
Std Dev	11.7

Turn on : 27.2668

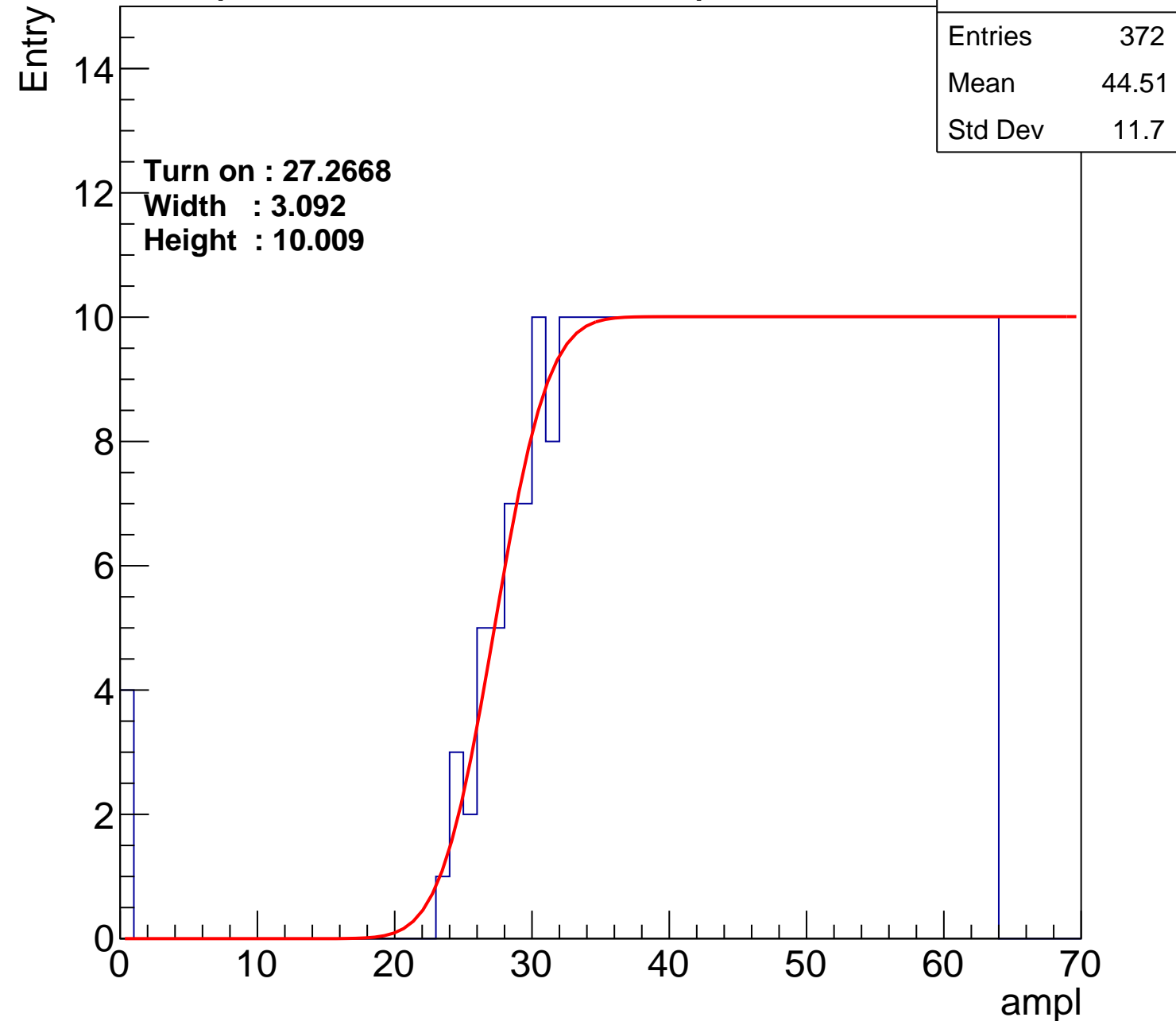
Width : 3.092

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch4

calib_packv5_042523_0143.root, FC#0, port D2

Entries	372
Mean	44.64
Std Dev	11.33

Turn on : 26.2857

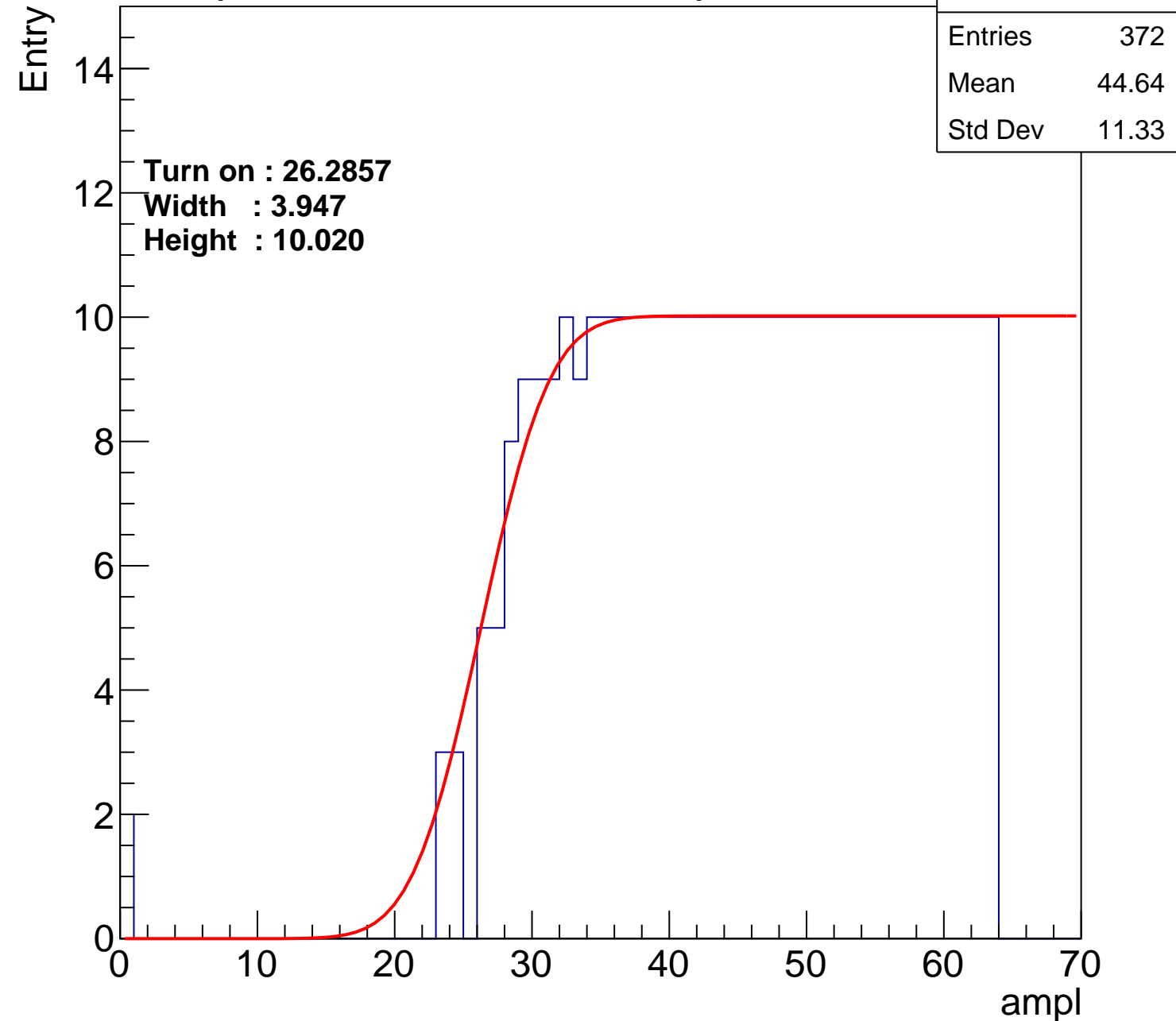
Width : 3.947

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch5

calib_packv5_042523_0143.root, FC#0, port D2

Entries	355
Mean	45.39
Std Dev	11.13

Turn on : 28.3283

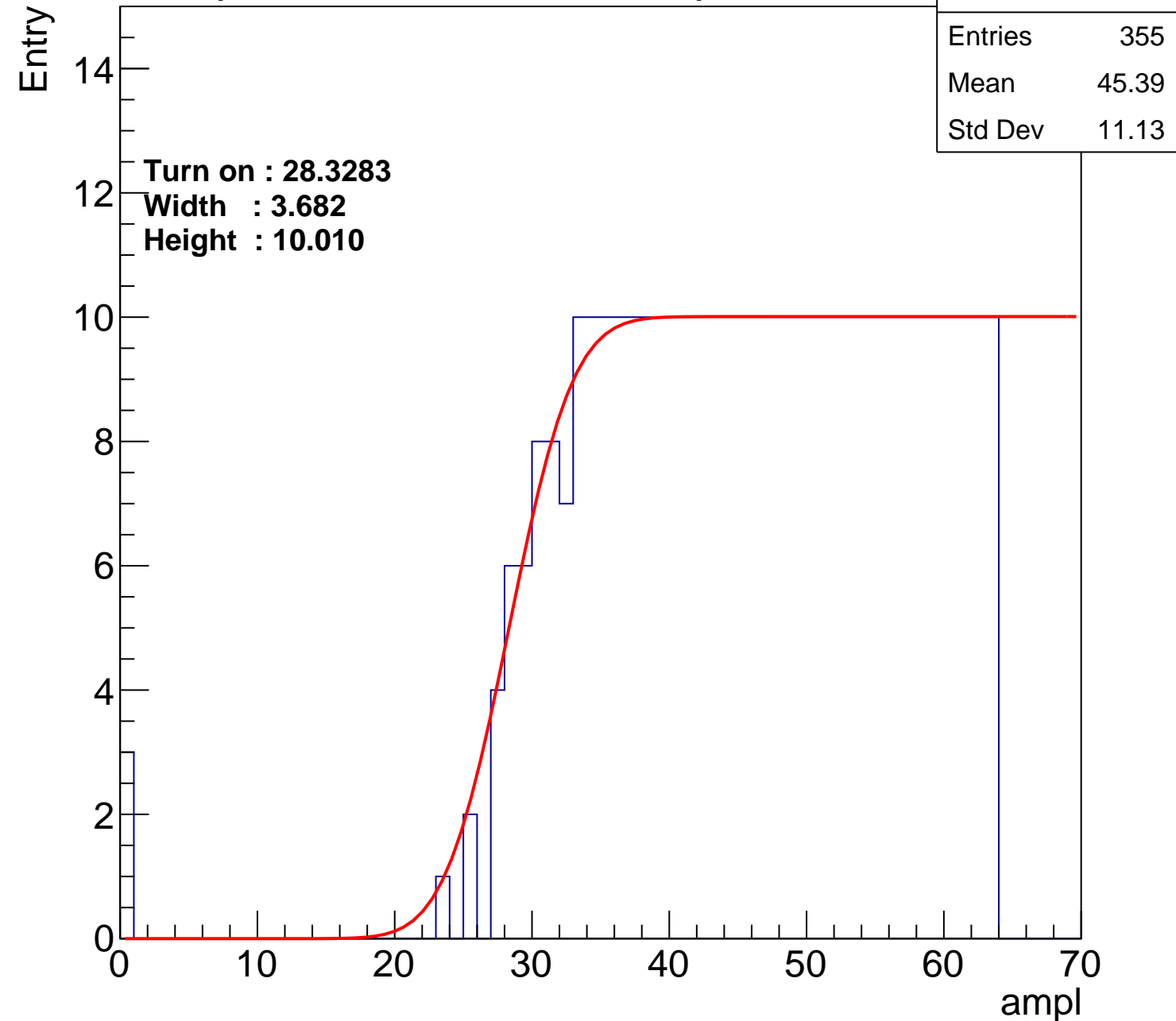
Width : 3.682

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch6

calib_packv5_042523_0143.root, FC#0, port D2

Entries	370
Mean	44.72
Std Dev	11.33

Turn on : 27.7583

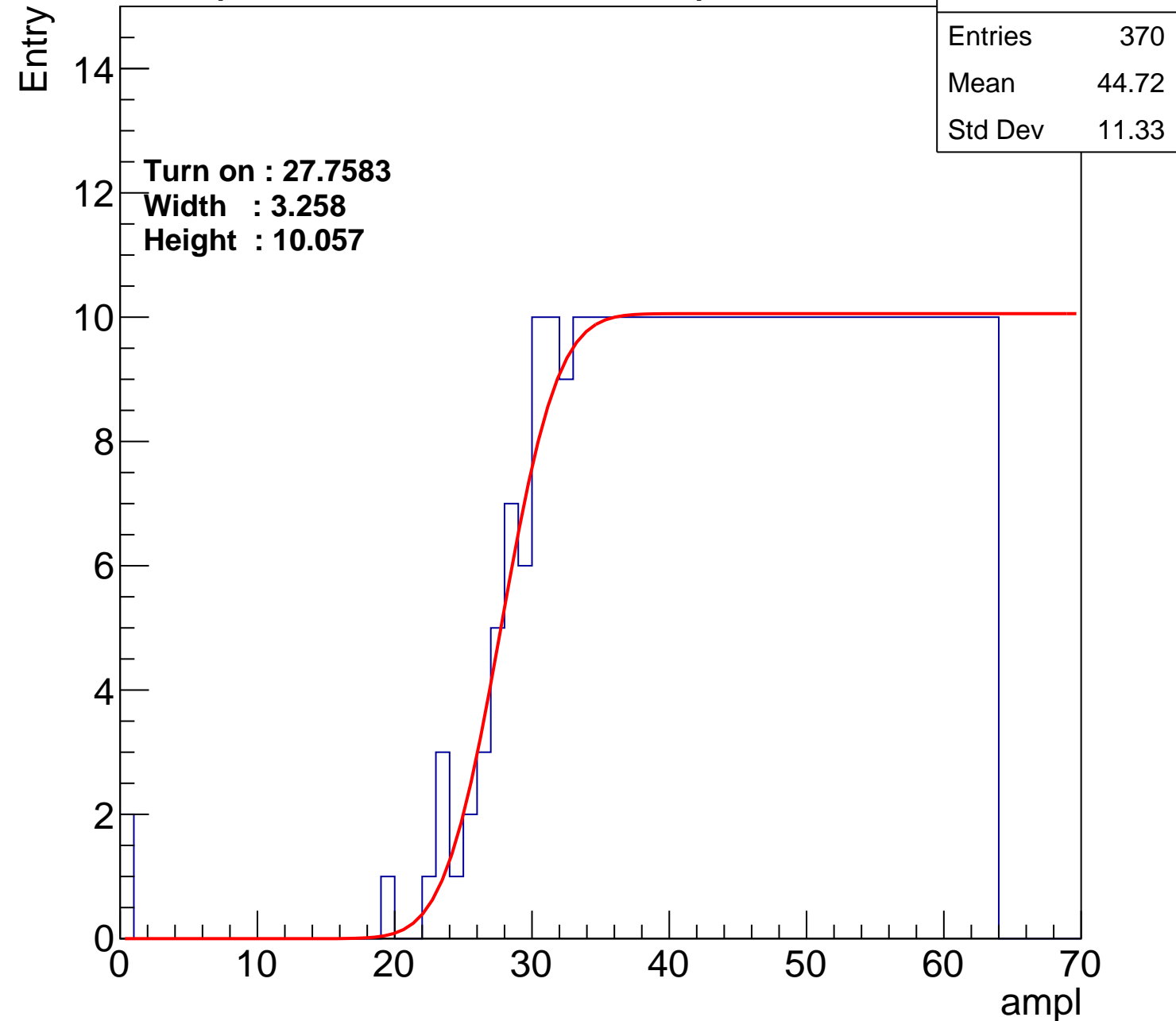
Width : 3.258

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch7

calib_packv5_042523_0143.root, FC#0, port D2

Entries	382
Mean	44.05
Std Dev	11.89

Turn on : 26.8798

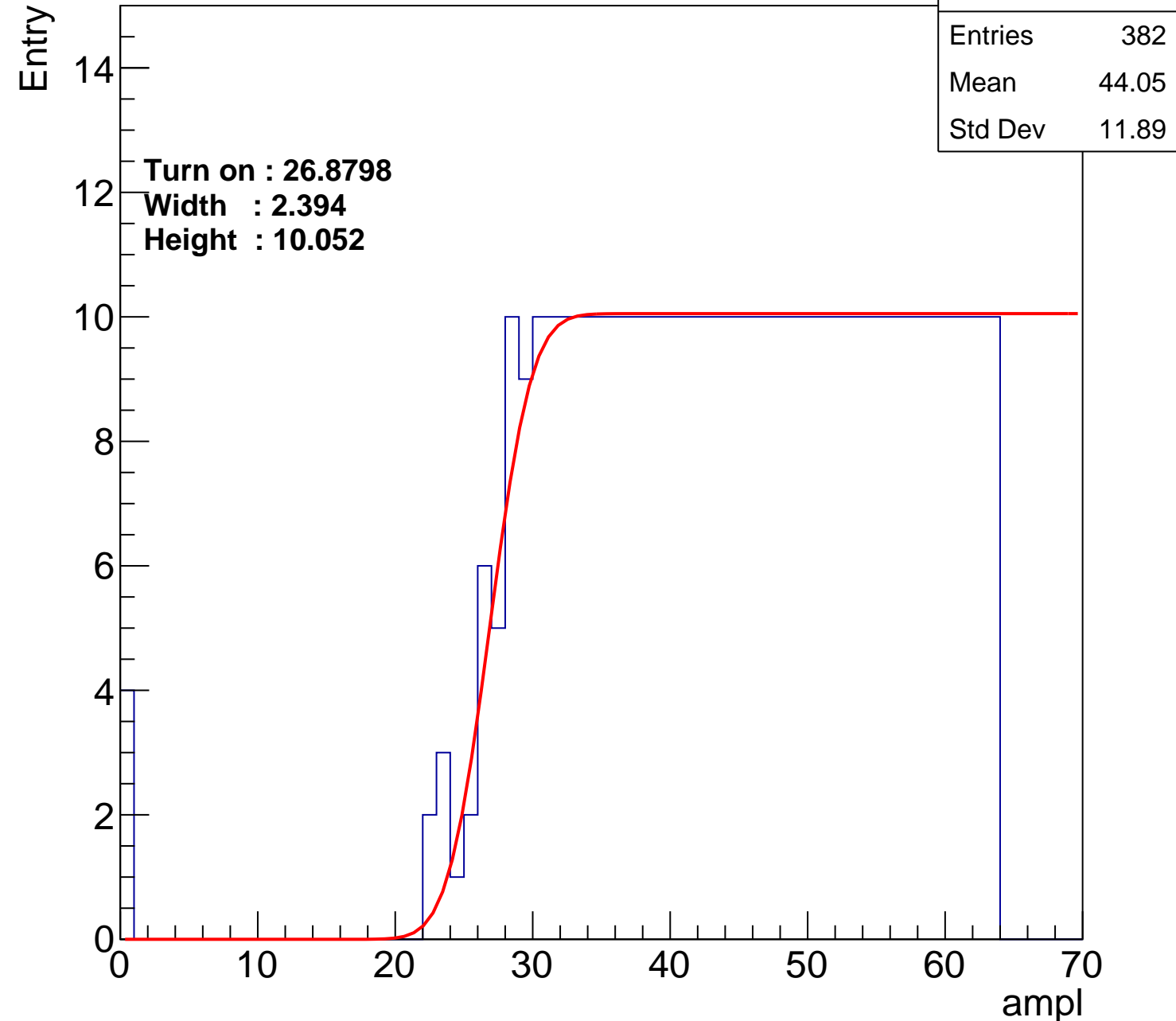
Width : 2.394

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch8

calib_packv5_042523_0143.root, FC#0, port D2

Entries	380
Mean	44.25
Std Dev	11.53

Turn on : 26.6222

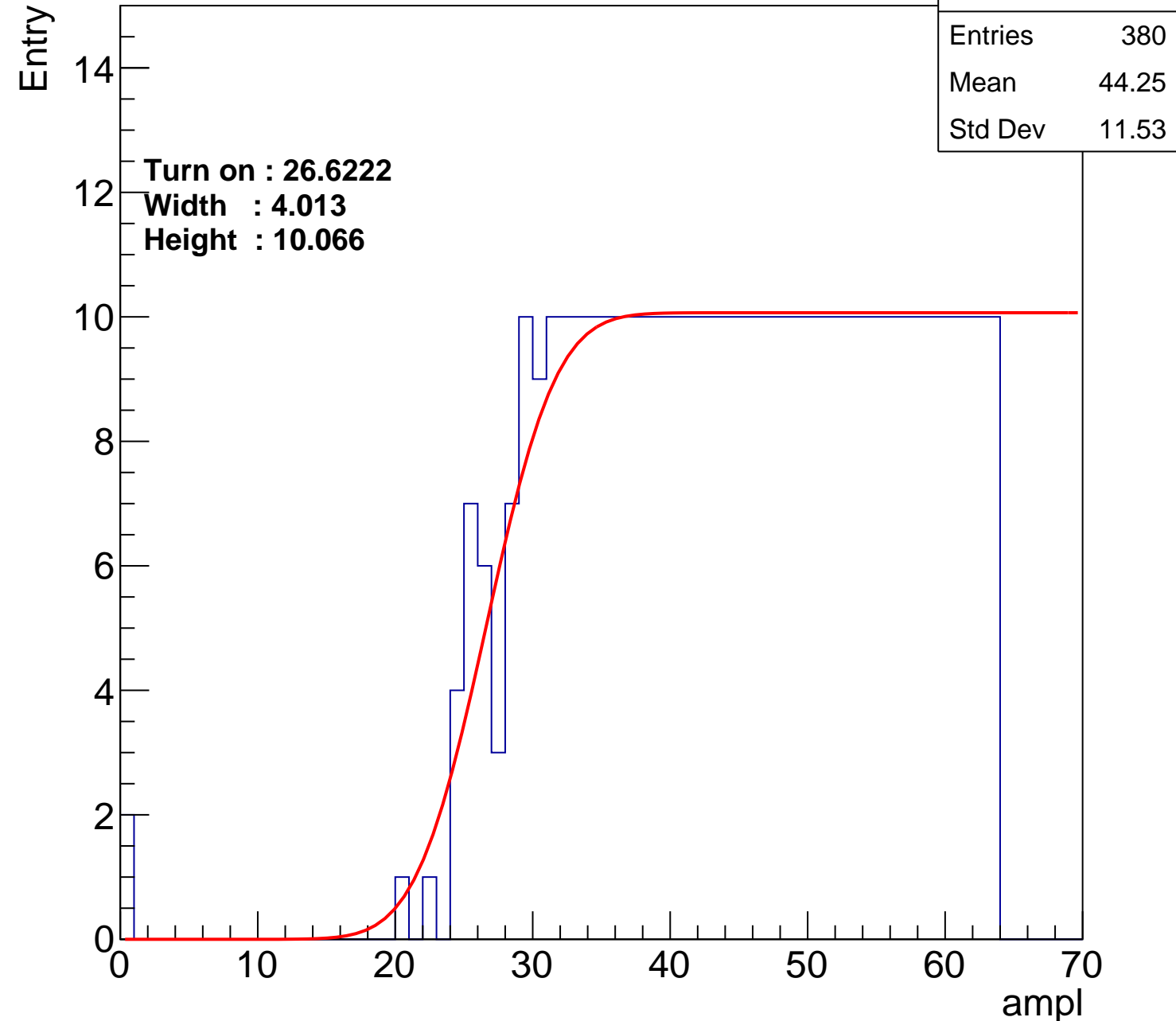
Width : 4.013

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch9

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.49
Std Dev	11.23

Turn on : 26.5797

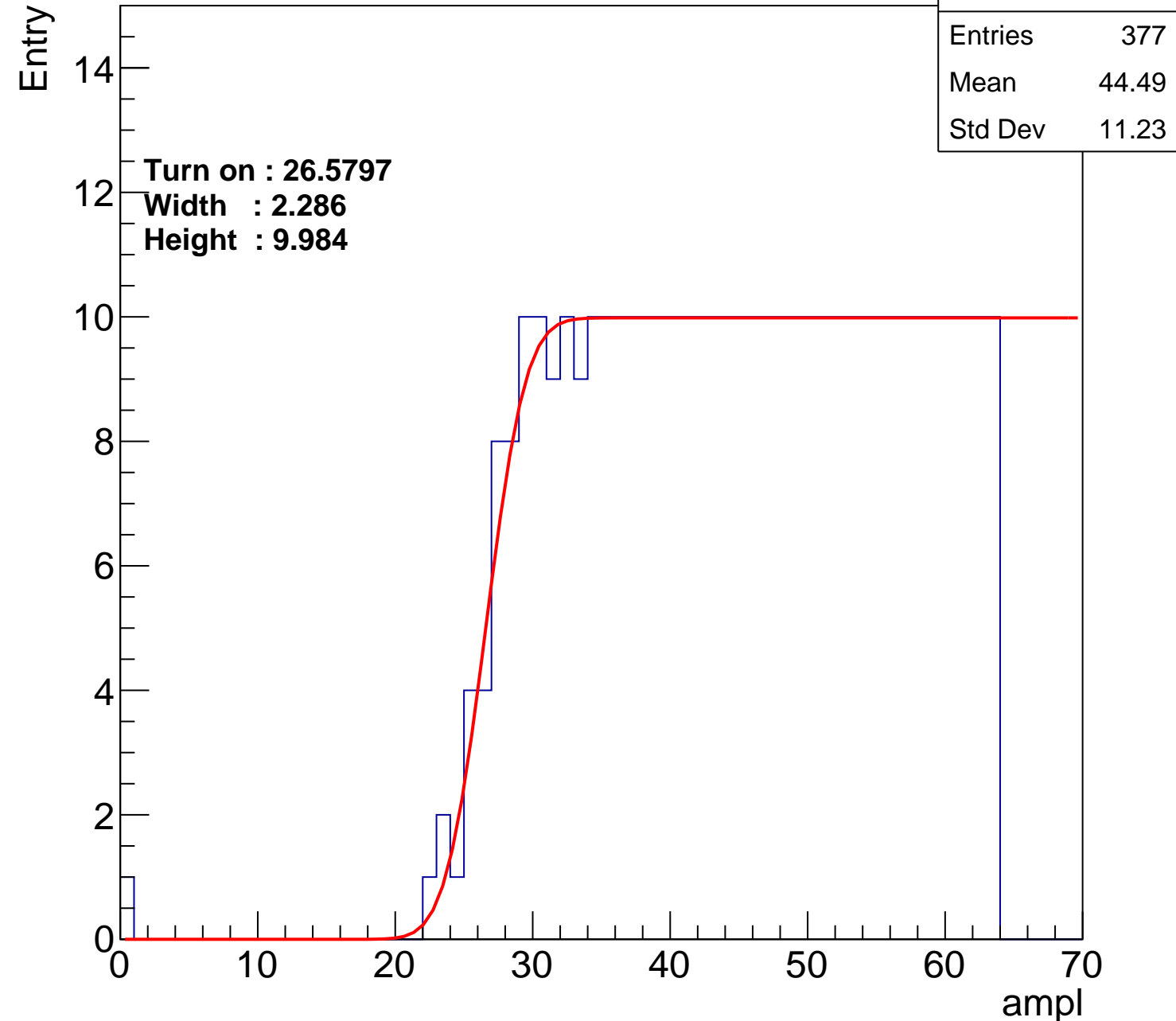
Width : 2.286

Height : 9.984

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch10

calib_packv5_042523_0143.root, FC#0, port D2

Entries	378
Mean	44.32
Std Dev	11.6

Turn on : 26.7230

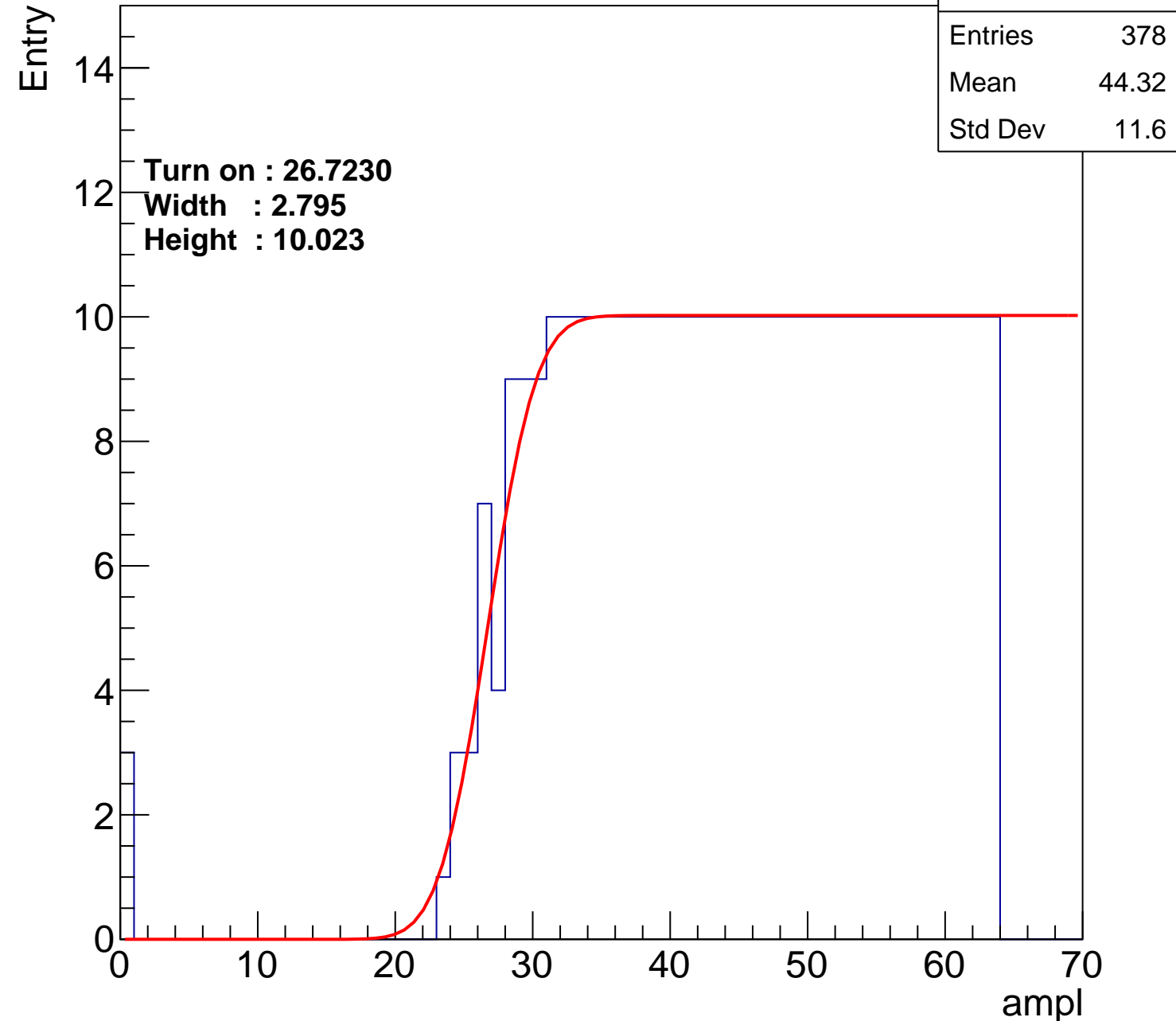
Width : 2.795

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch11

calib_packv5_042523_0143.root, FC#0, port D2

Entries	355
Mean	45.39
Std Dev	11.13

Turn on : 28.8215

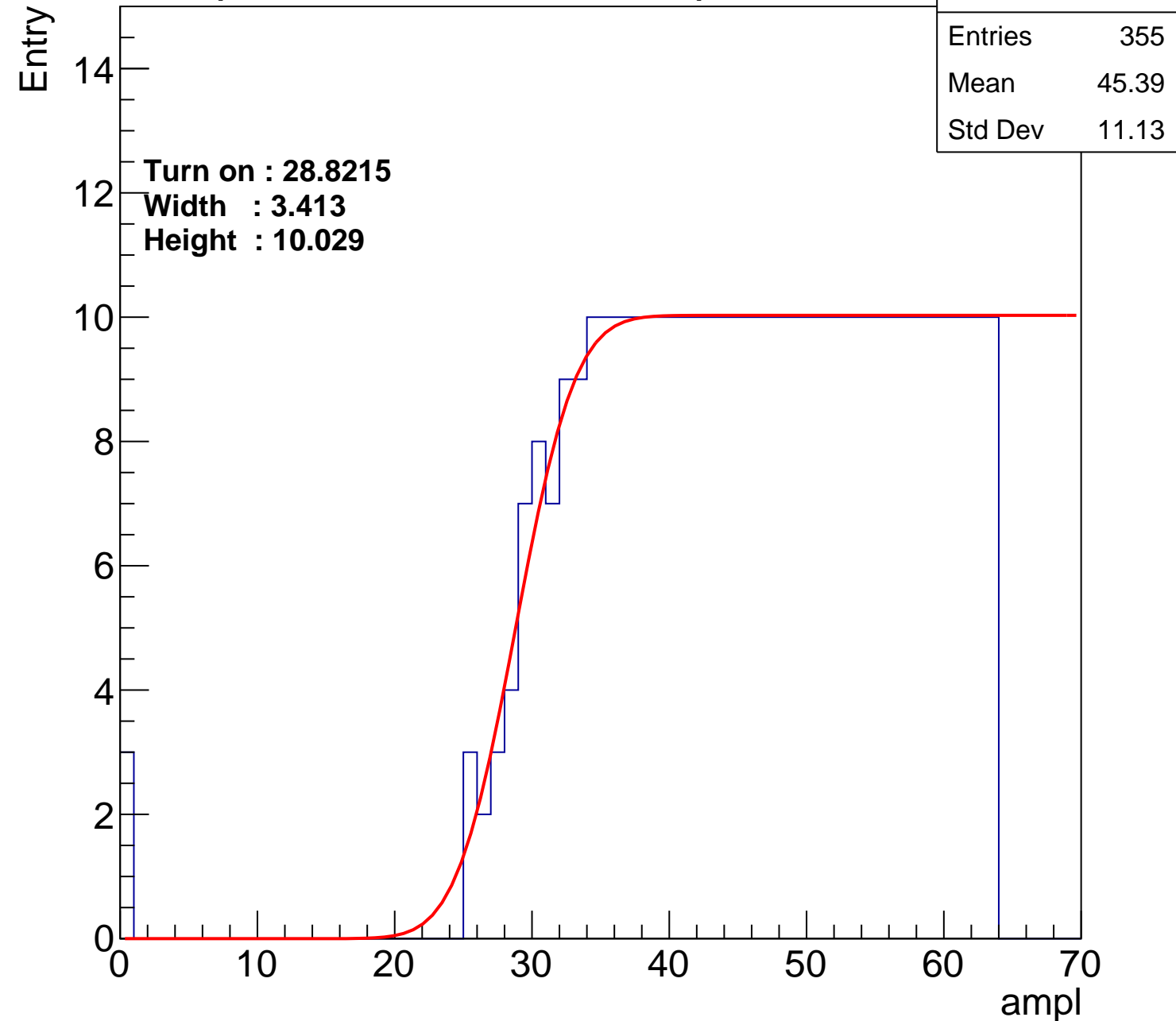
Width : 3.413

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch12

calib_packv5_042523_0143.root, FC#0, port D2

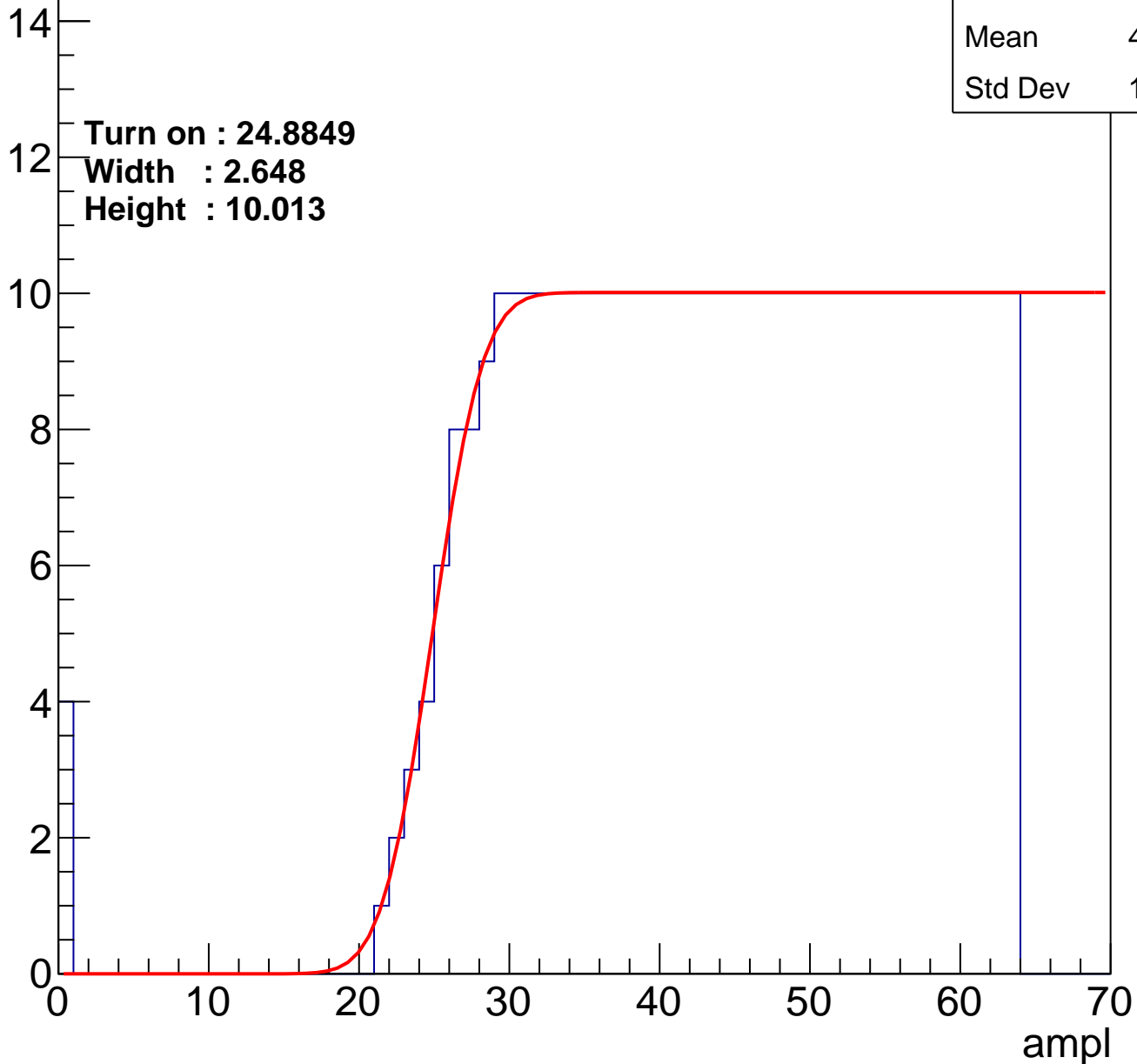
Entries	395
Mean	43.43
Std Dev	12.17

Turn on : 24.8849

Width : 2.648

Height : 10.013

Entry



B1L101S, U20-ch13

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.42
Std Dev	11.48

Turn on : 27.0843

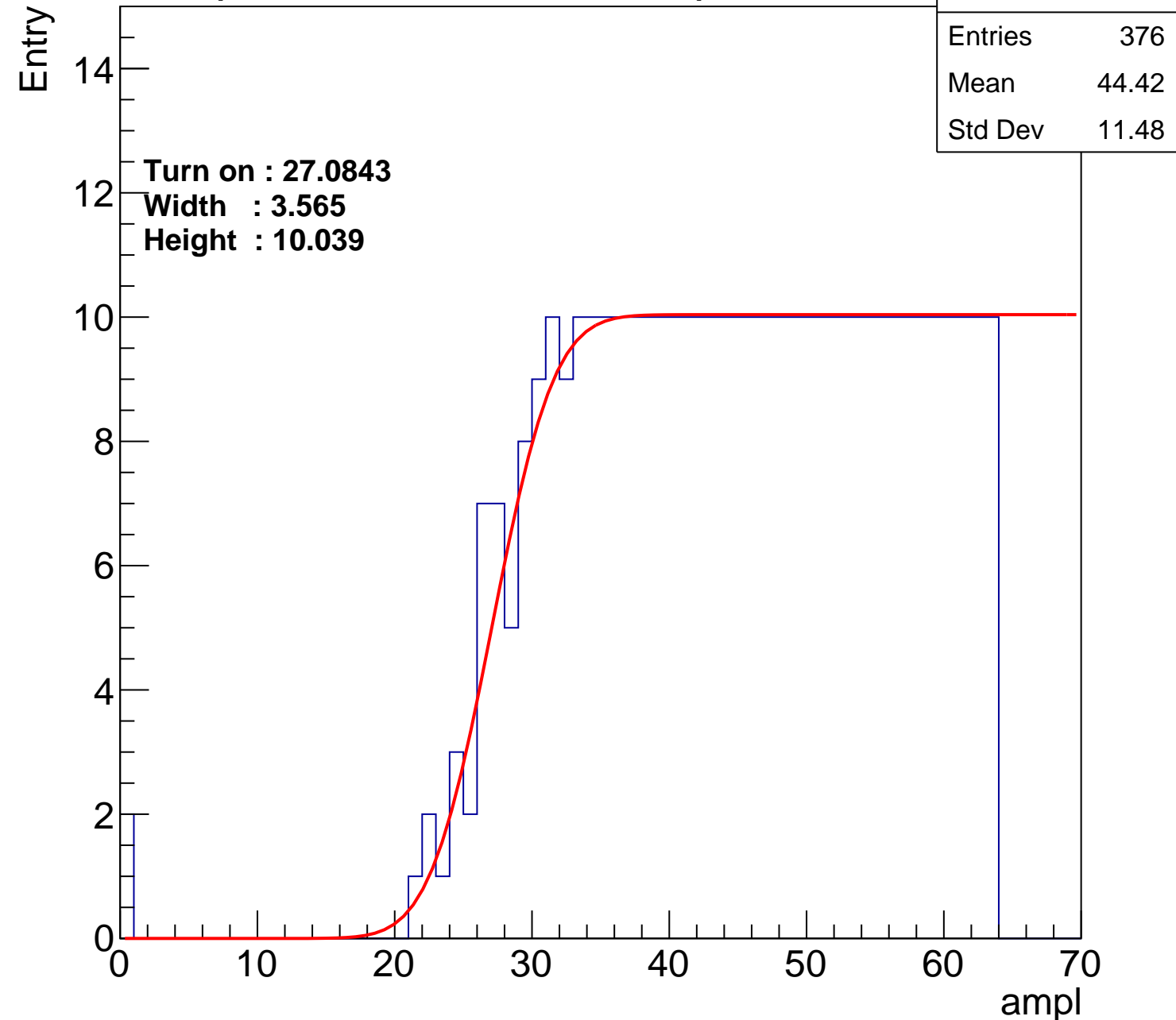
Width : 3.565

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch14

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.41
Std Dev	11.44

Turn on : 26.9407

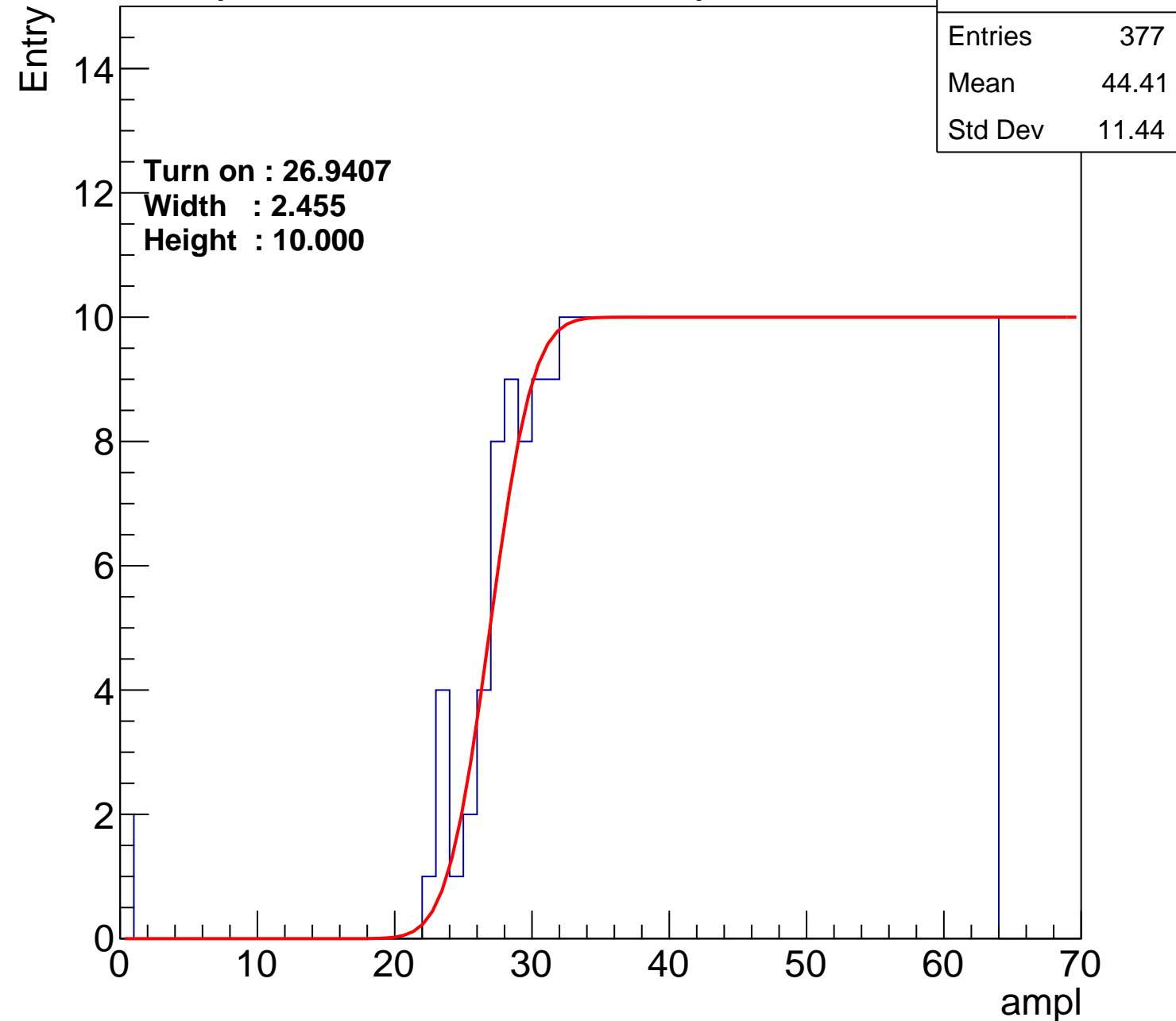
Width : 2.455

Height : 10.000

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch15

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.42
Std Dev	11.74

Turn on : 27.5676

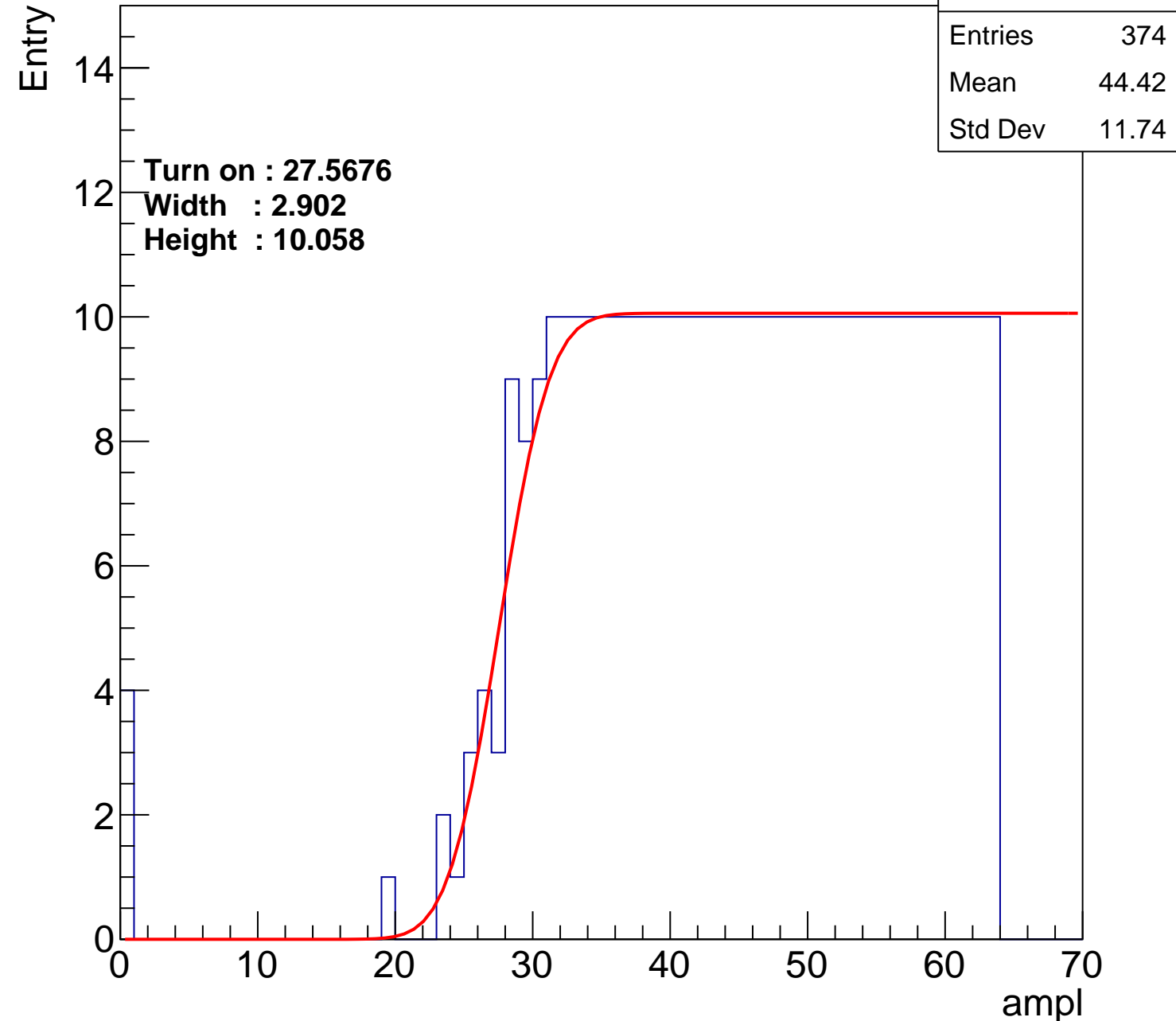
Width : 2.902

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch16

calib_packv5_042523_0143.root, FC#0, port D2

Entries	376
Mean	44.39
Std Dev	11.6

Turn on : 27.0451

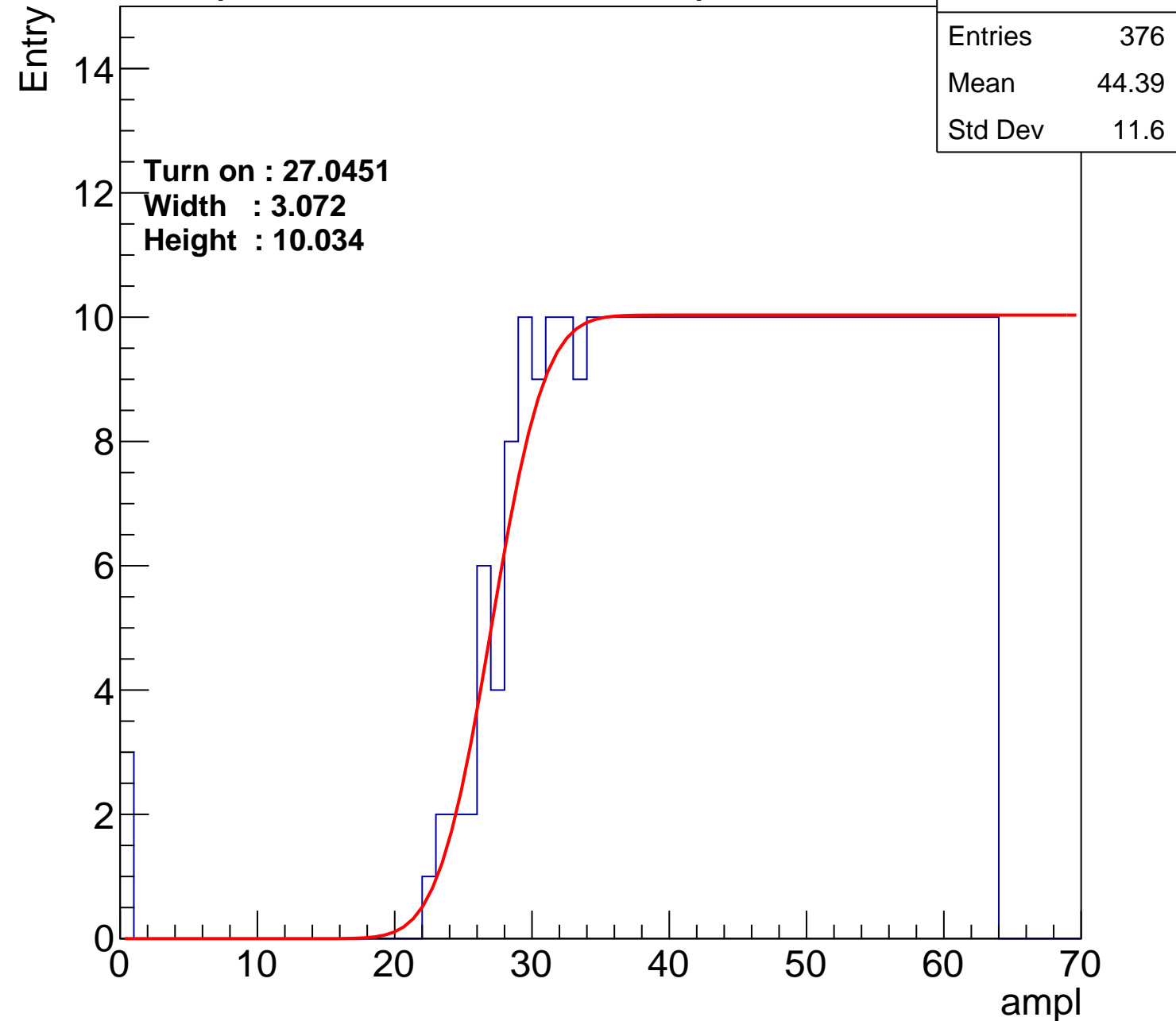
Width : 3.072

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch17

calib_packv5_042523_0143.root, FC#0, port D2

Entries	373
Mean	44.53
Std Dev	11.63

Turn on : 27.1782

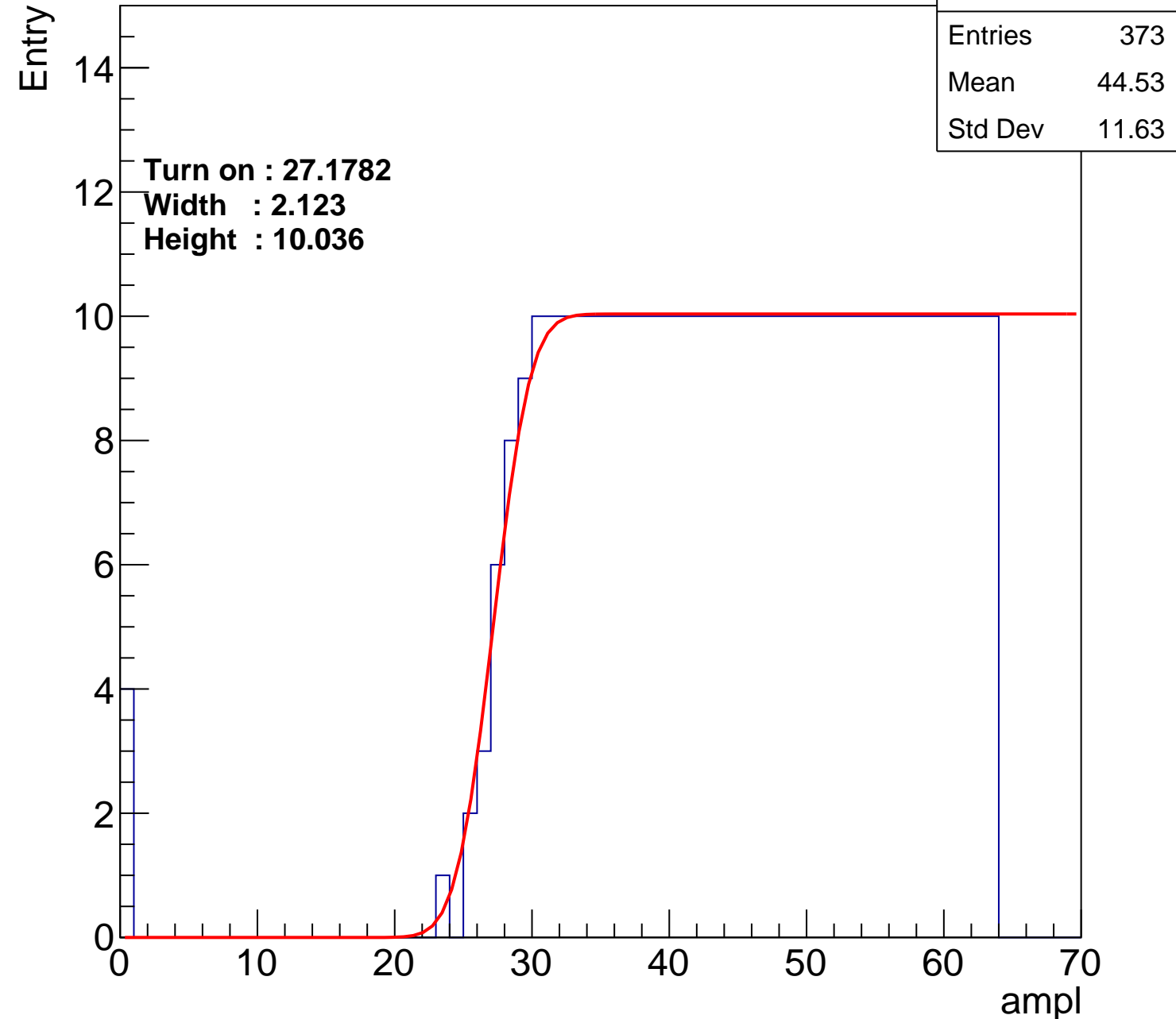
Width : 2.123

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch18

calib_packv5_042523_0143.root, FC#0, port D2

Entries	369
Mean	44.77
Std Dev	11.29

Turn on : 27.7324

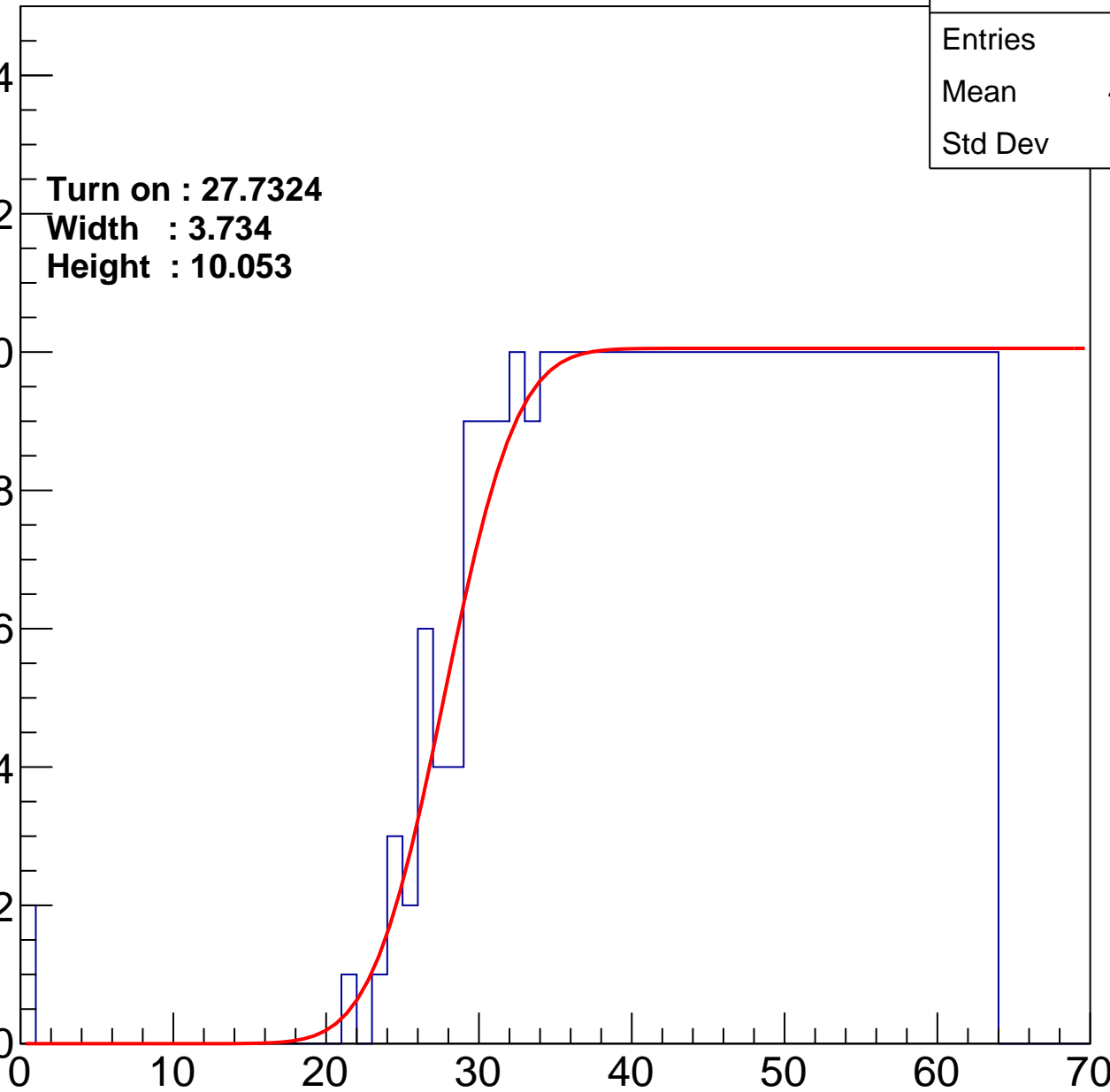
Width : 3.734

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch19

calib_packv5_042523_0143.root, FC#0, port D2

Entries	370
Mean	44.72
Std Dev	11.4

Turn on : 27.2613

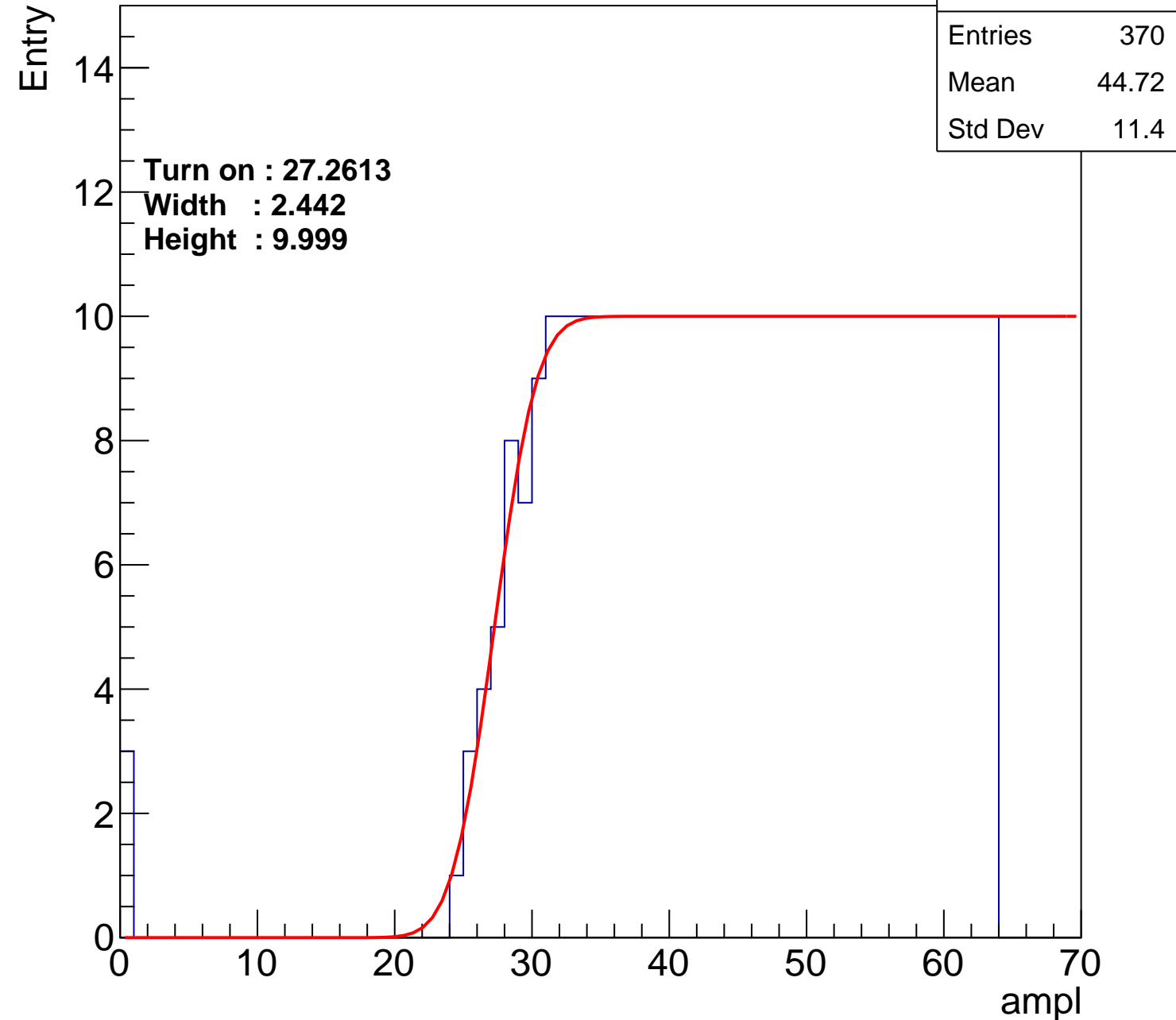
Width : 2.442

Height : 9.999

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch20

calib_packv5_042523_0143.root, FC#0, port D2

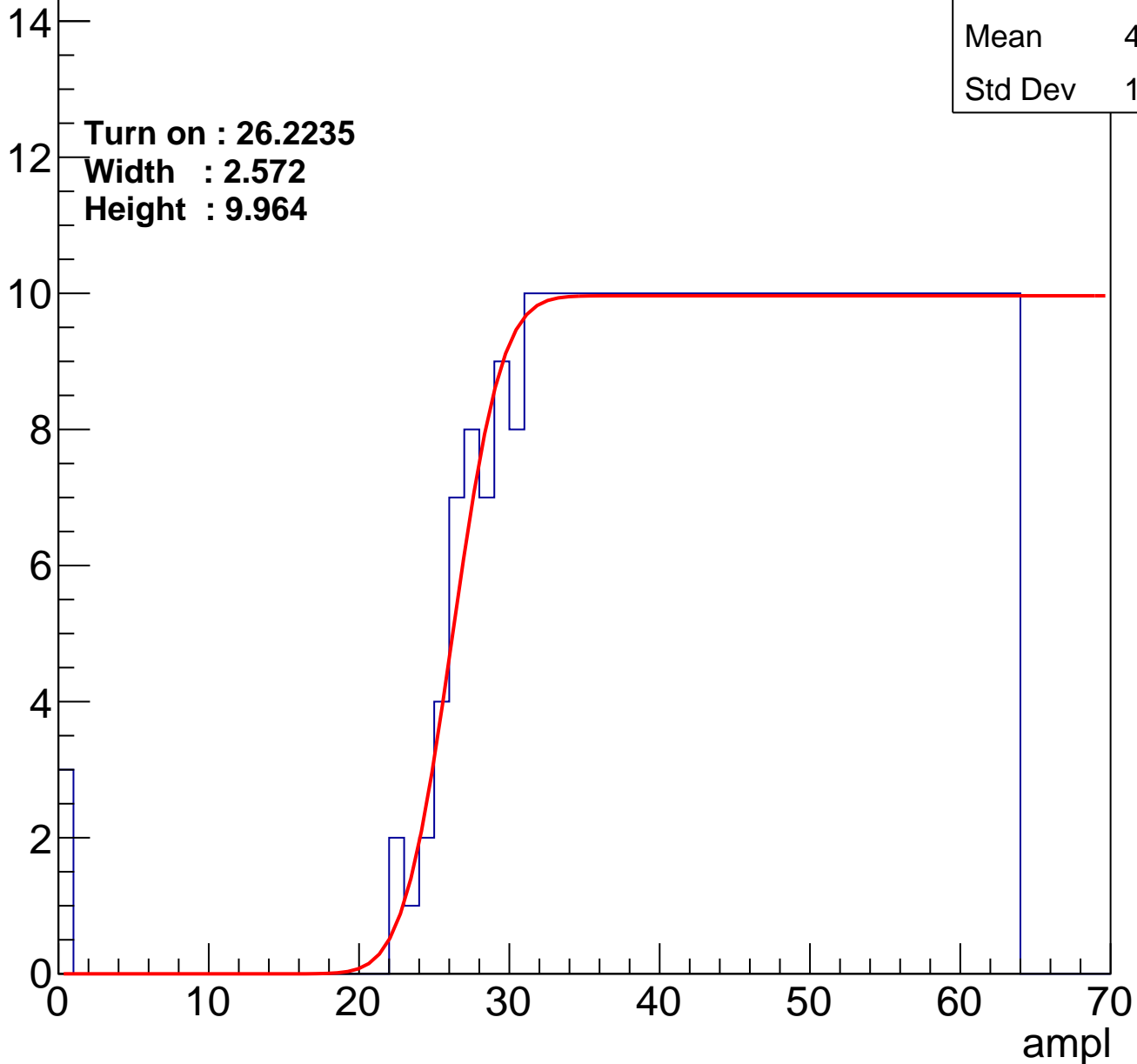
Entries	381
Mean	44.15
Std Dev	11.72

Turn on : 26.2235

Width : 2.572

Height : 9.964

Entry



B1L101S, U20-ch21

calib_packv5_042523_0143.root, FC#0, port D2

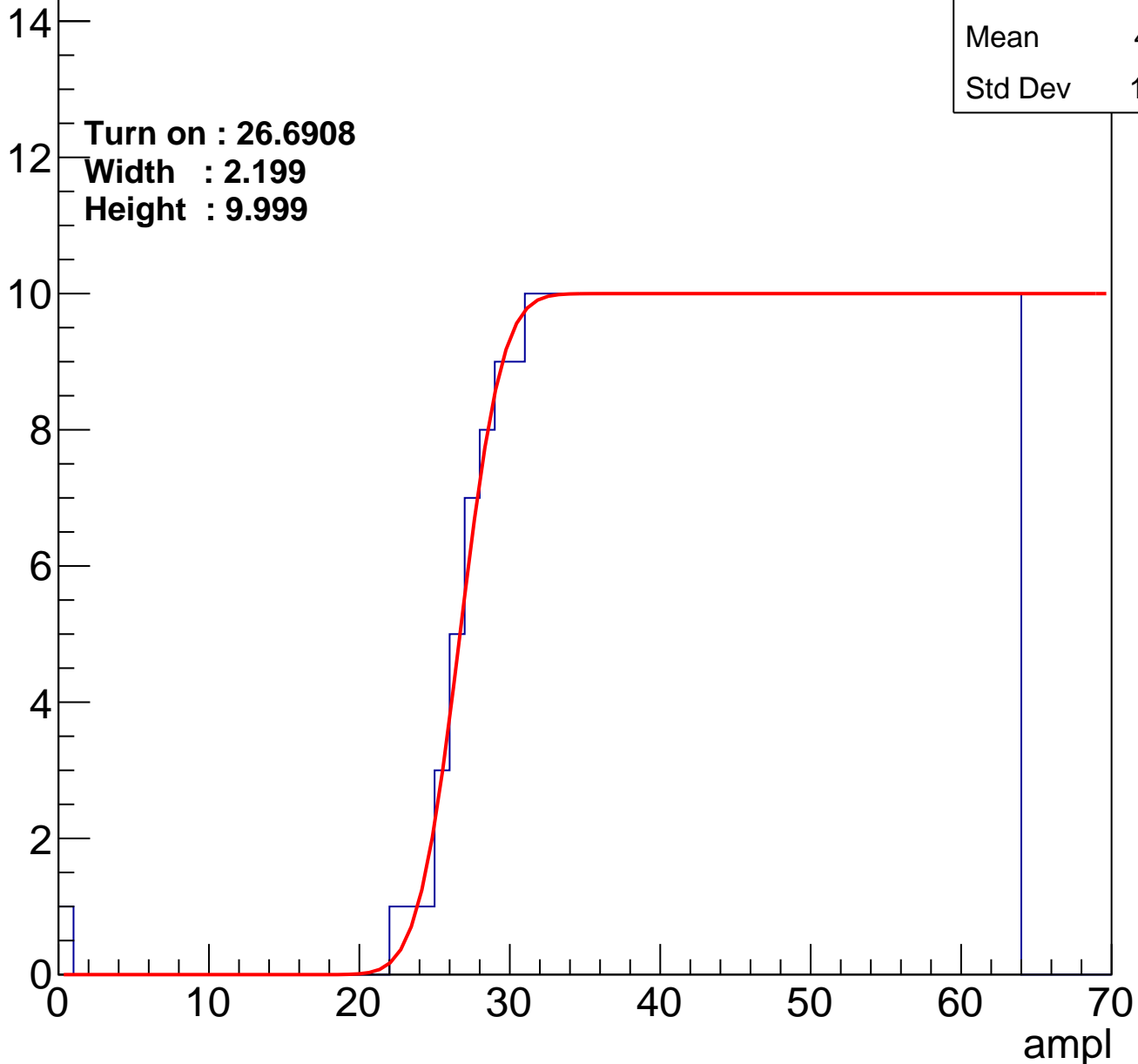
Entries	375
Mean	44.61
Std Dev	11.14

Turn on : 26.6908

Width : 2.199

Height : 9.999

Entry



B1L101S, U20-ch22

calib_packv5_042523_0143.root, FC#0, port D2

Entries	382
Mean	44.07
Std Dev	11.86

Turn on : 25.9862

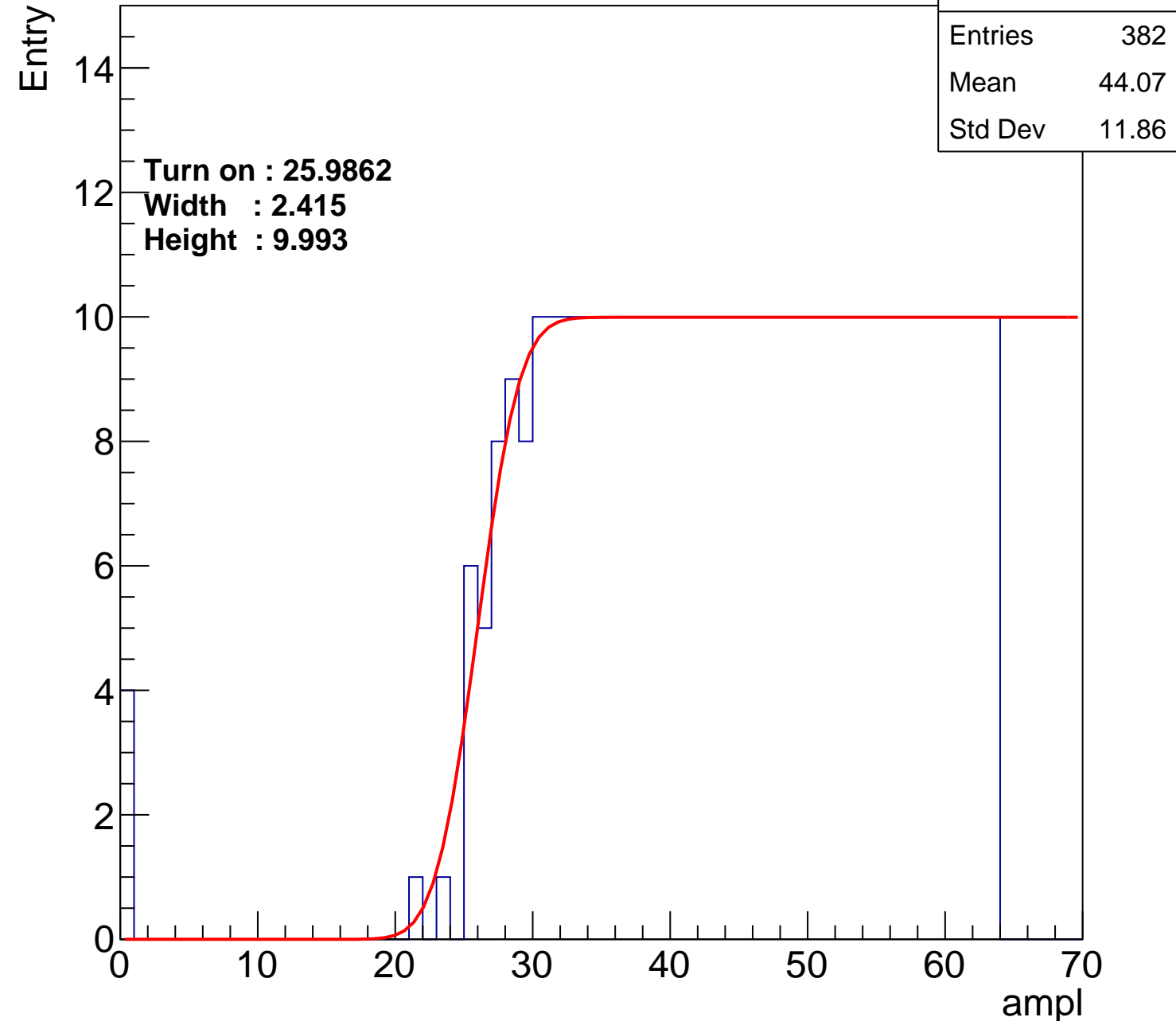
Width : 2.415

Height : 9.993

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch23

calib_packv5_042523_0143.root, FC#0, port D2

Entries	370
Mean	44.59
Std Dev	11.69

Turn on : 27.1771

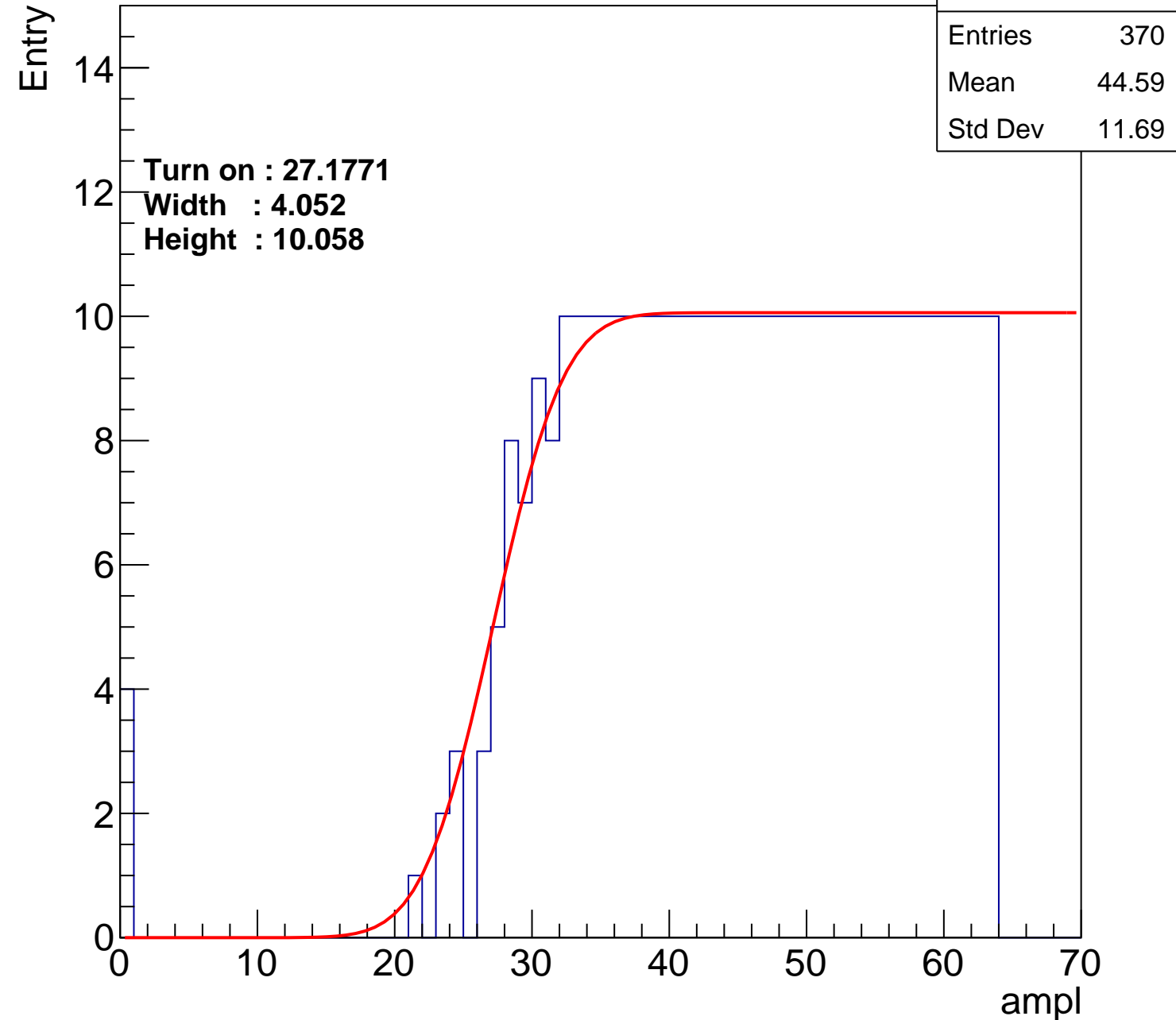
Width : 4.052

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch24

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.5
Std Dev	11.4

Turn on : 26.5812

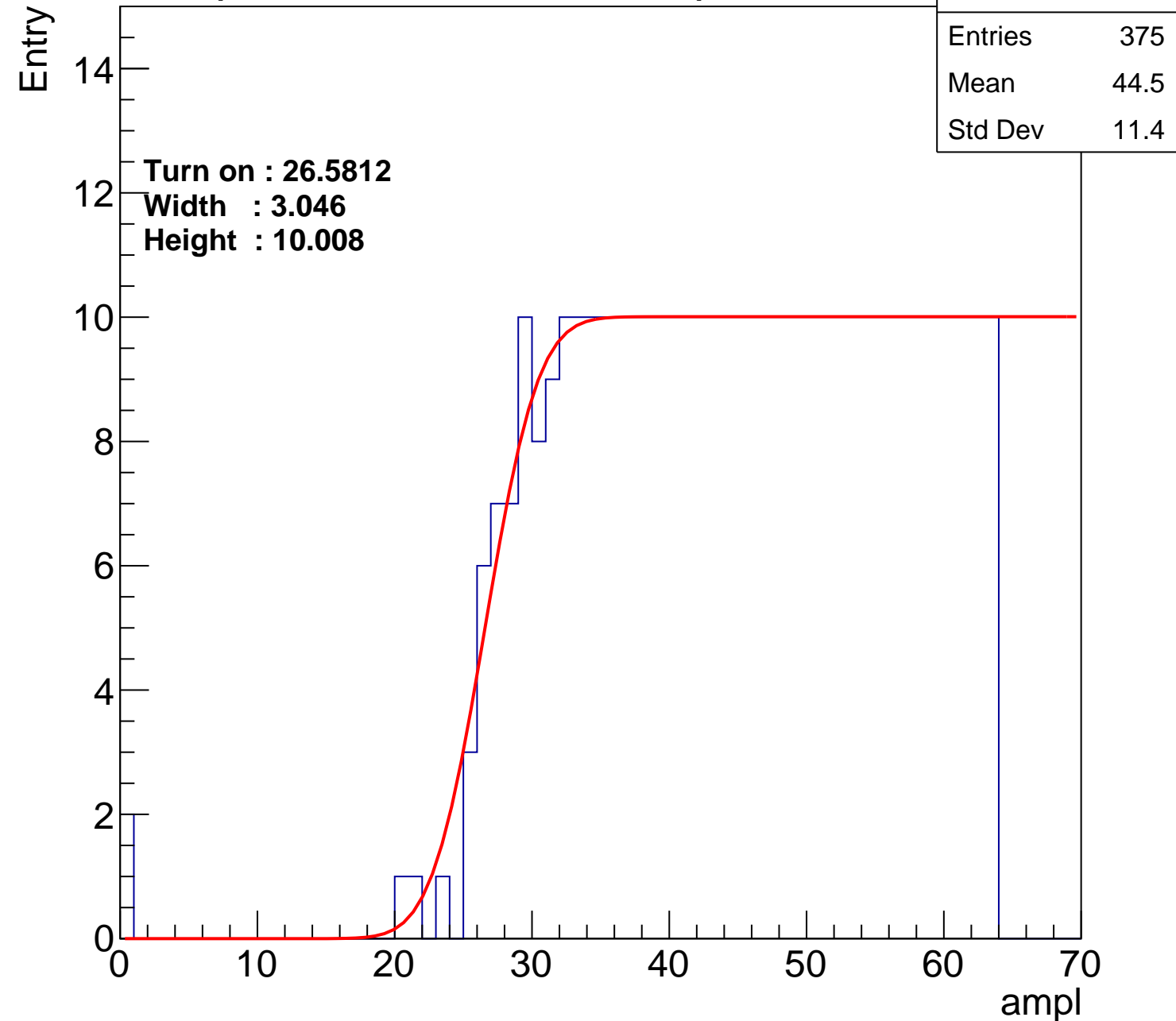
Width : 3.046

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch25

calib_packv5_042523_0143.root, FC#0, port D2

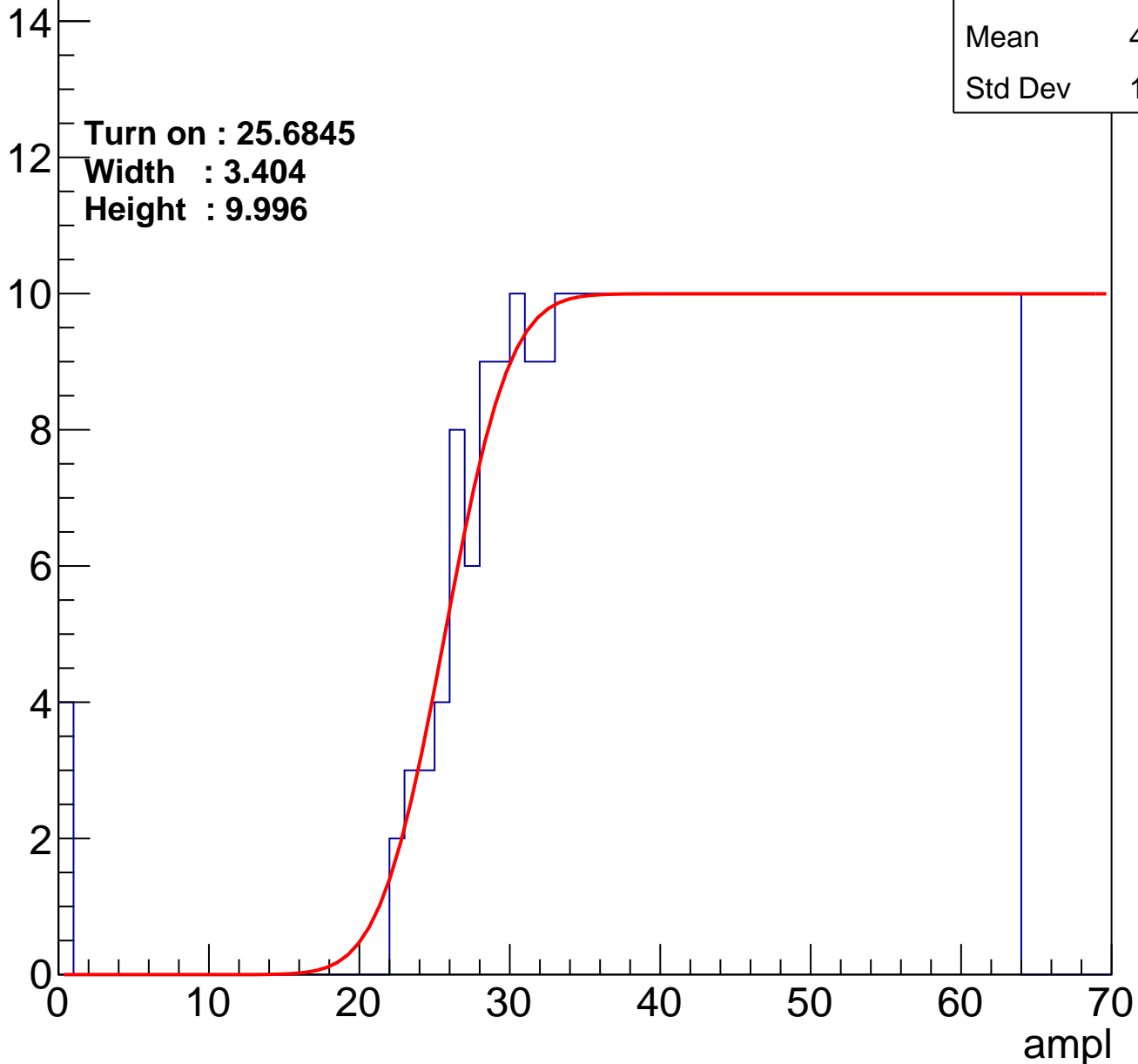
Entries	386
Mean	43.82
Std Dev	12.03

Turn on : 25.6845

Width : 3.404

Height : 9.996

Entry



B1L101S, U20-ch26

calib_packv5_042523_0143.root, FC#0, port D2

Entries	394
Mean	43.52
Std Dev	12.02

Turn on : 25.5033

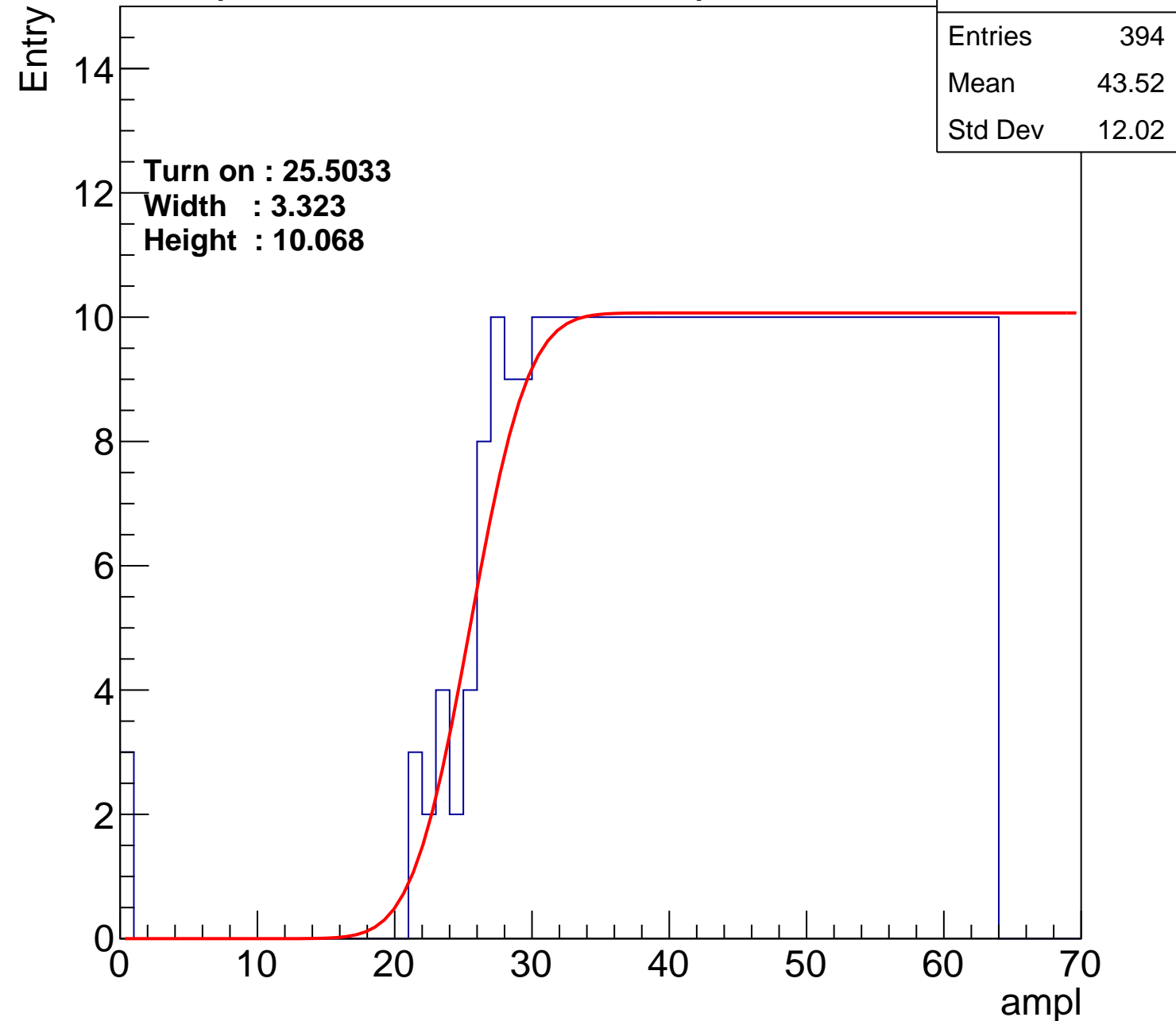
Width : 3.323

Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch27

calib_packv5_042523_0143.root, FC#0, port D2

Entries	387
Mean	43.93
Std Dev	11.68

Turn on : 25.6103

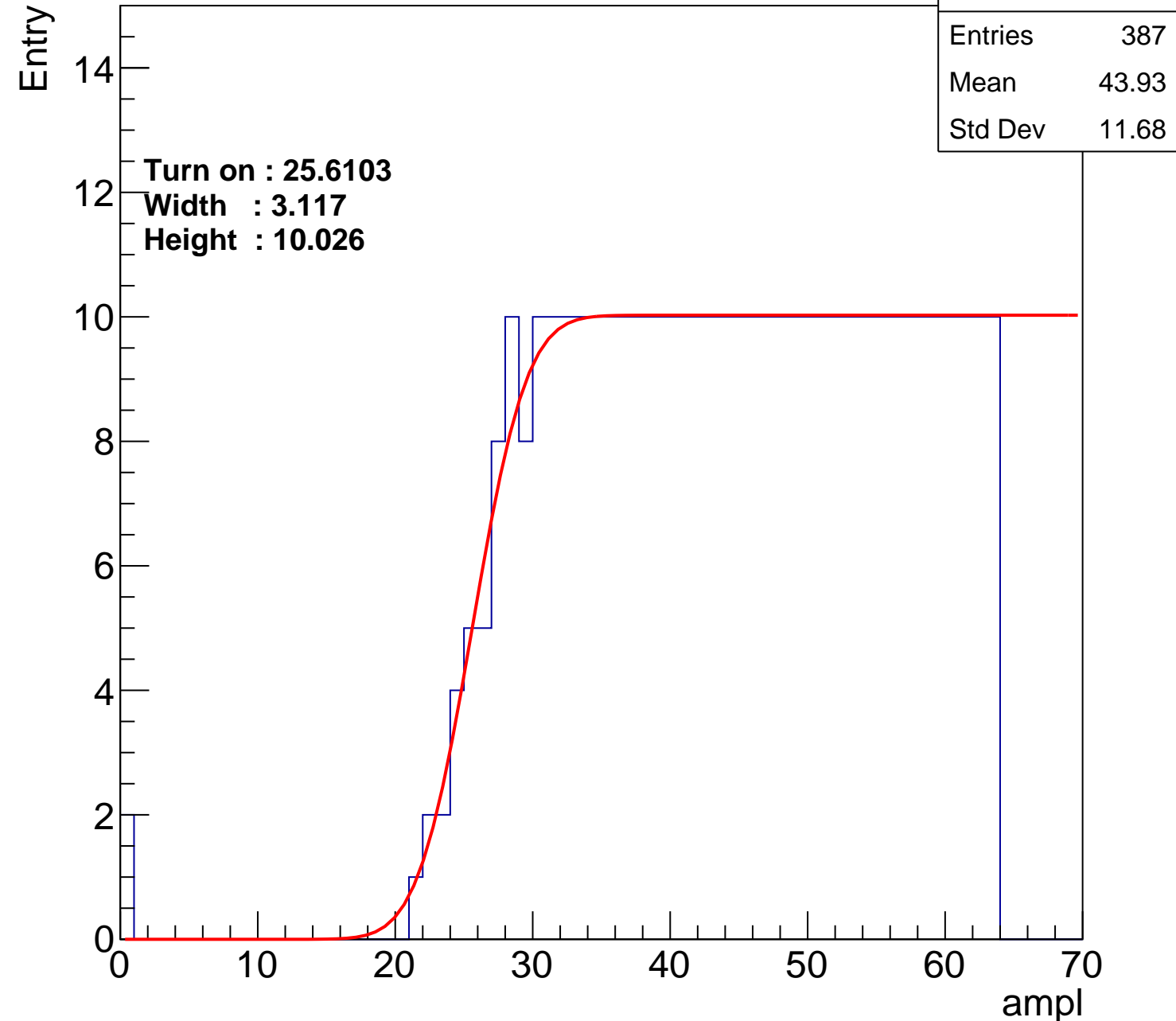
Width : 3.117

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch28

calib_packv5_042523_0143.root, FC#0, port D2

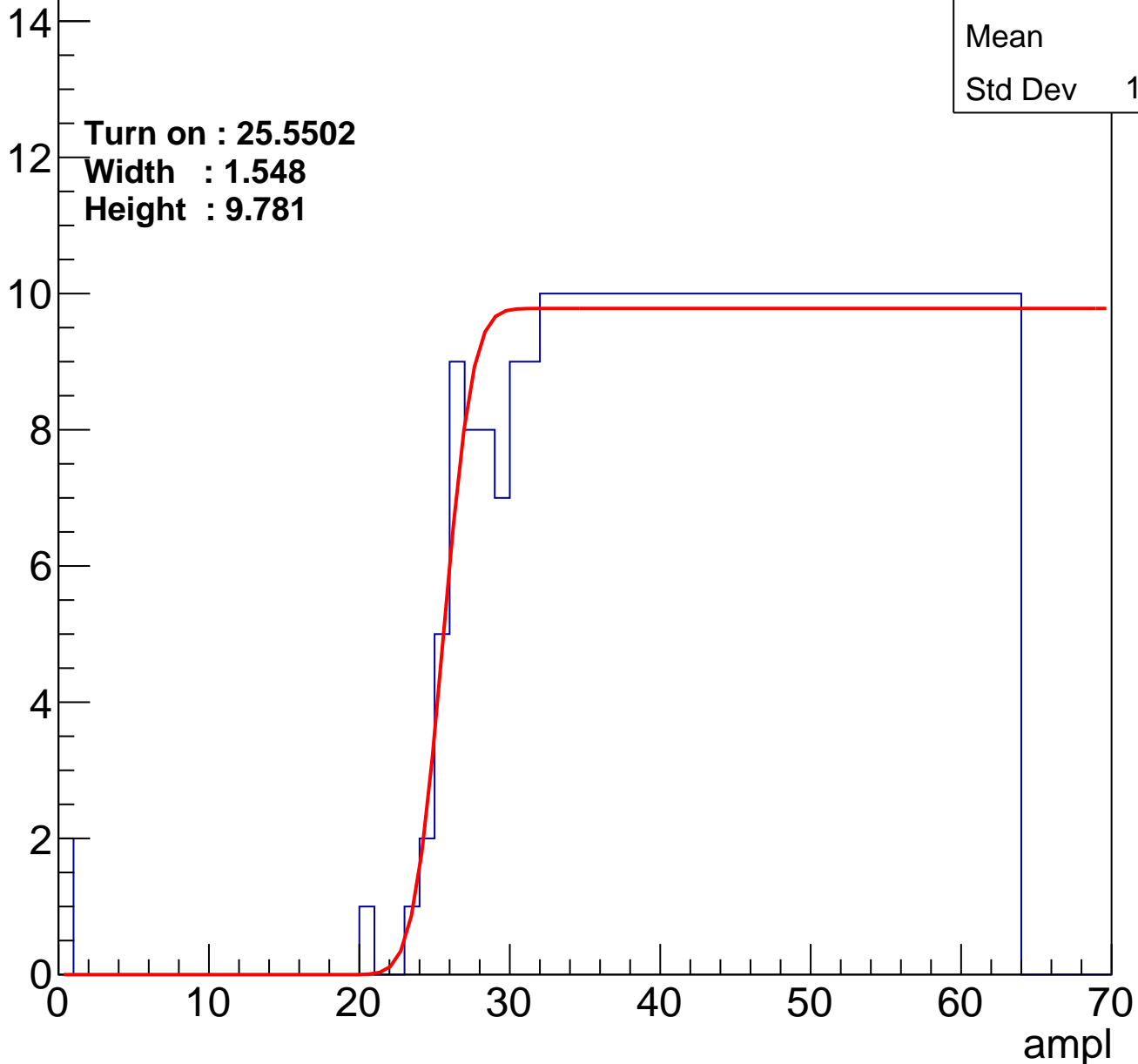
Entries	381
Mean	44.2
Std Dev	11.55

Turn on : 25.5502

Width : 1.548

Height : 9.781

Entry



B1L101S, U20-ch29

calib_packv5_042523_0143.root, FC#0, port D2

Entries	354
Mean	45.52
Std Dev	10.89

Turn on : 29.1795

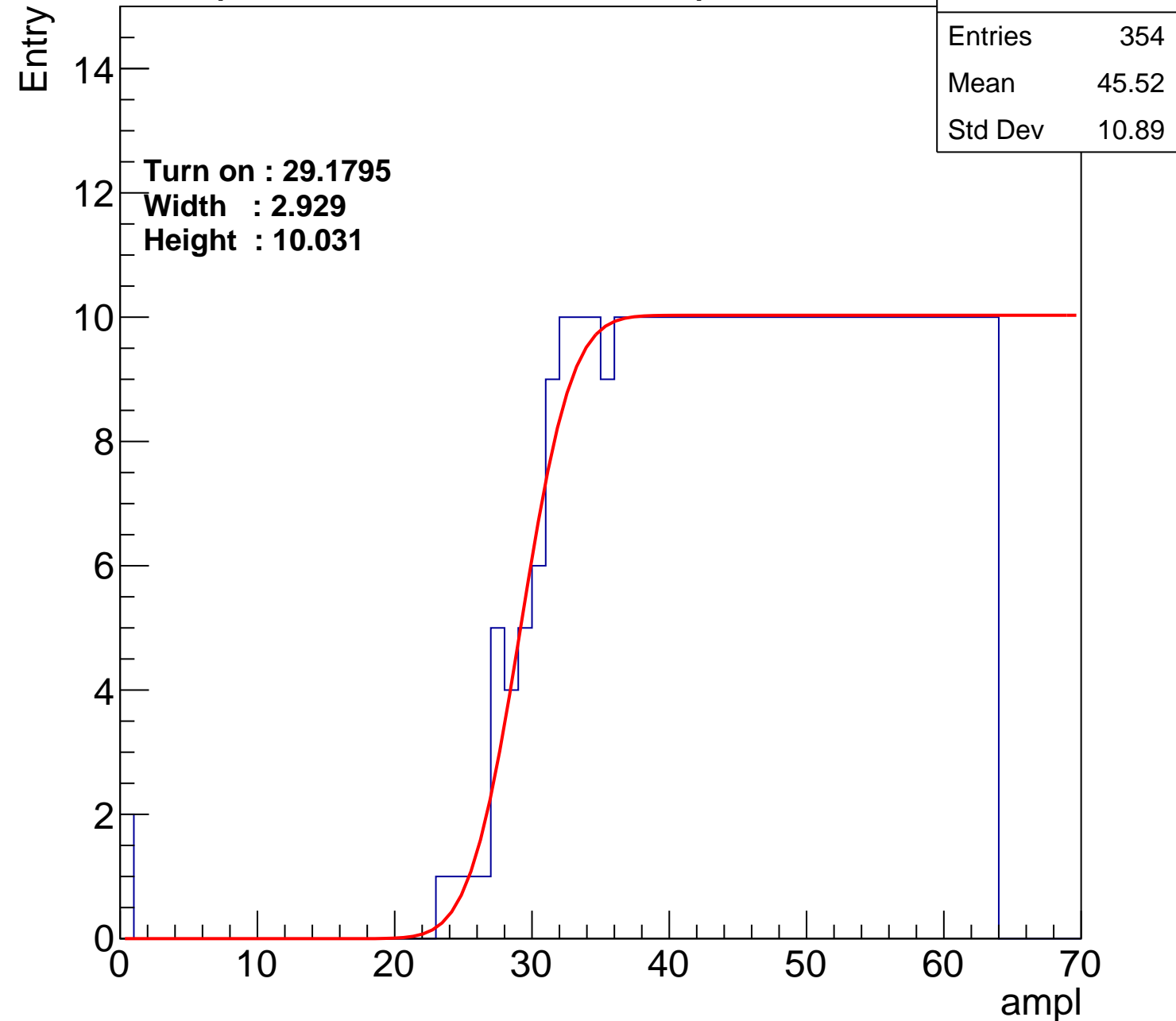
Width : 2.929

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch30

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.39
Std Dev	11.73

Turn on : 26.8337

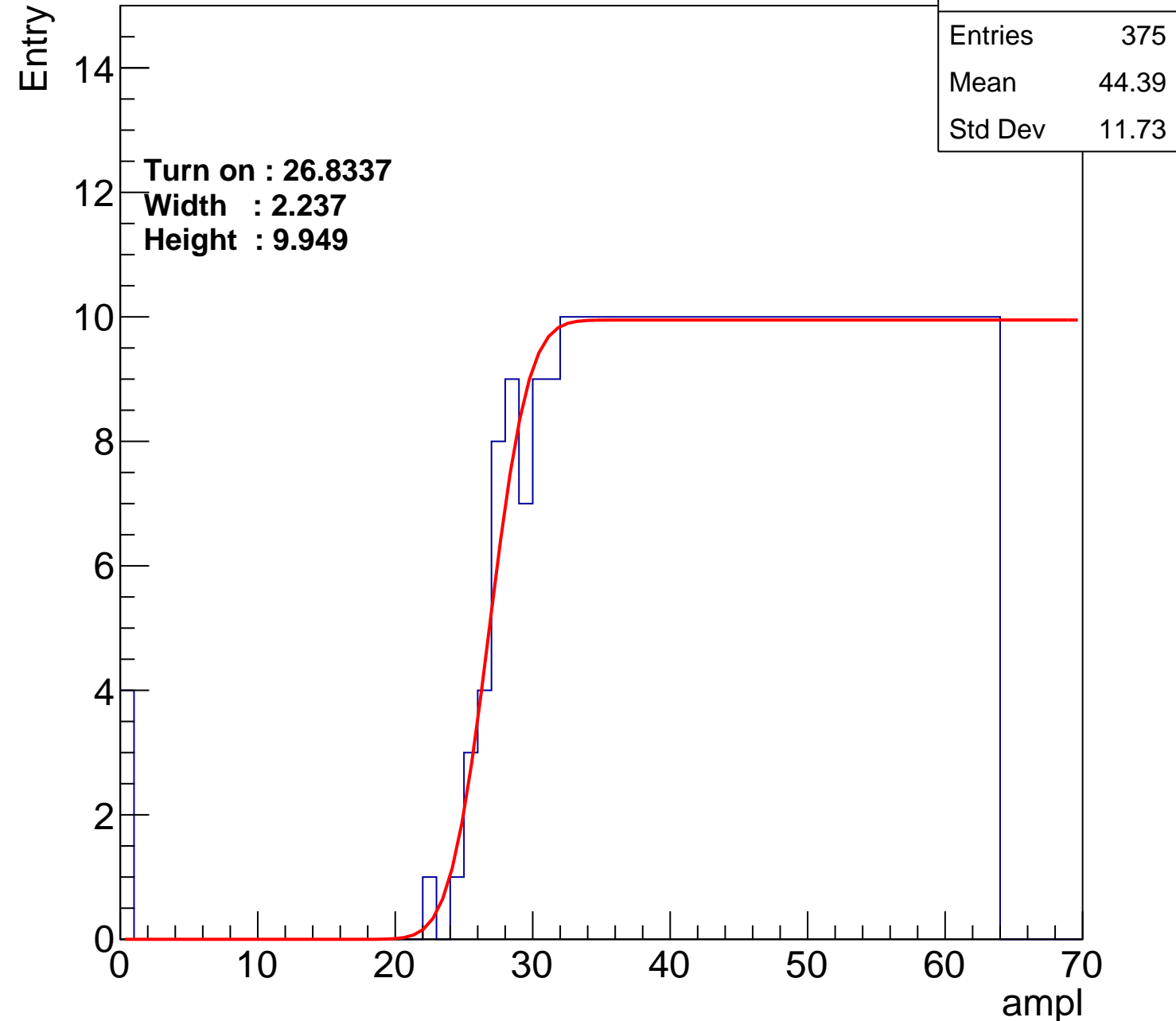
Width : 2.237

Height : 9.949

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch31

calib_packv5_042523_0143.root, FC#0, port D2

Entries	366
Mean	44.98
Std Dev	11.12

Turn on : 27.2001

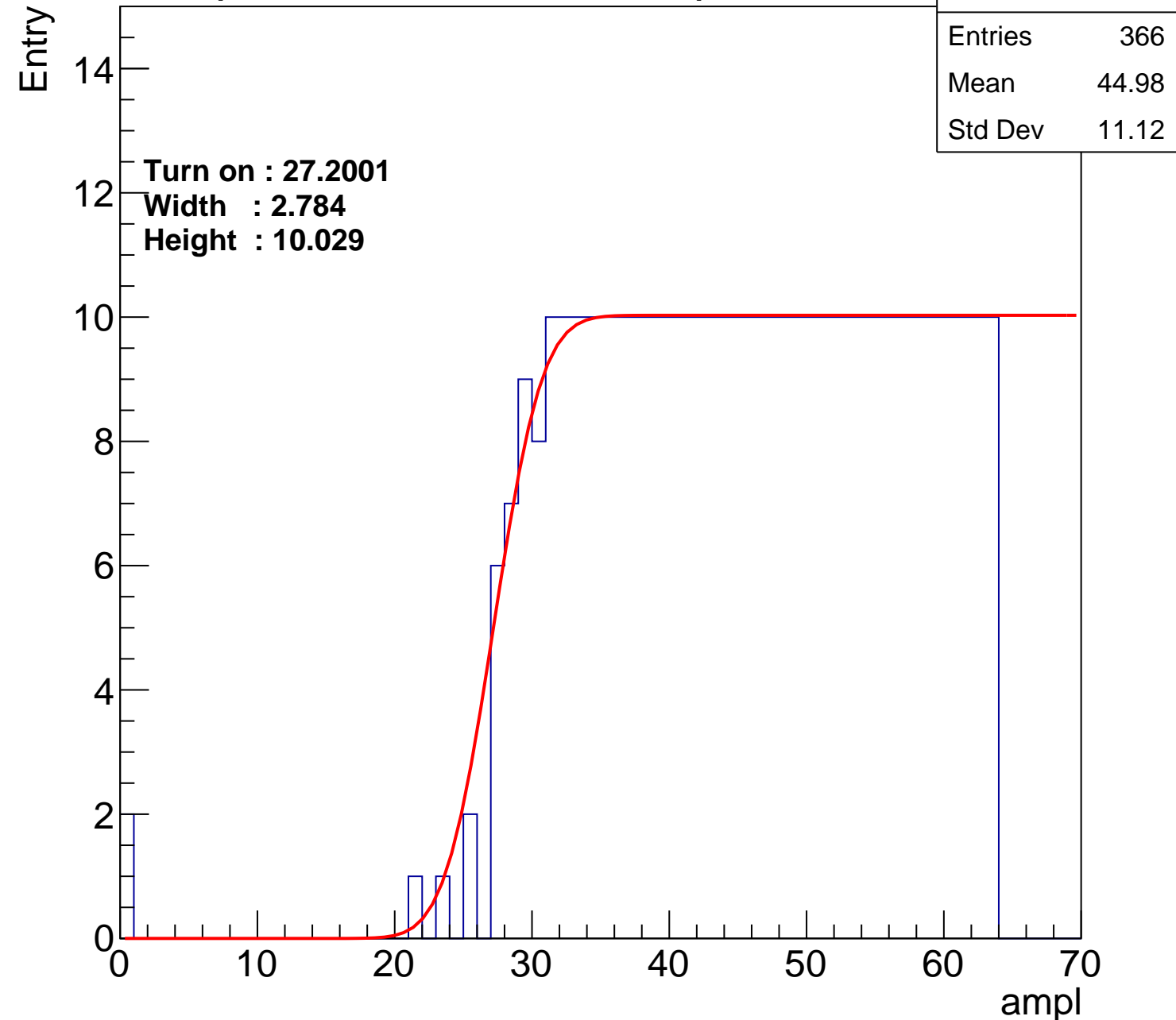
Width : 2.784

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch32

calib_packv5_042523_0143.root, FC#0, port D2

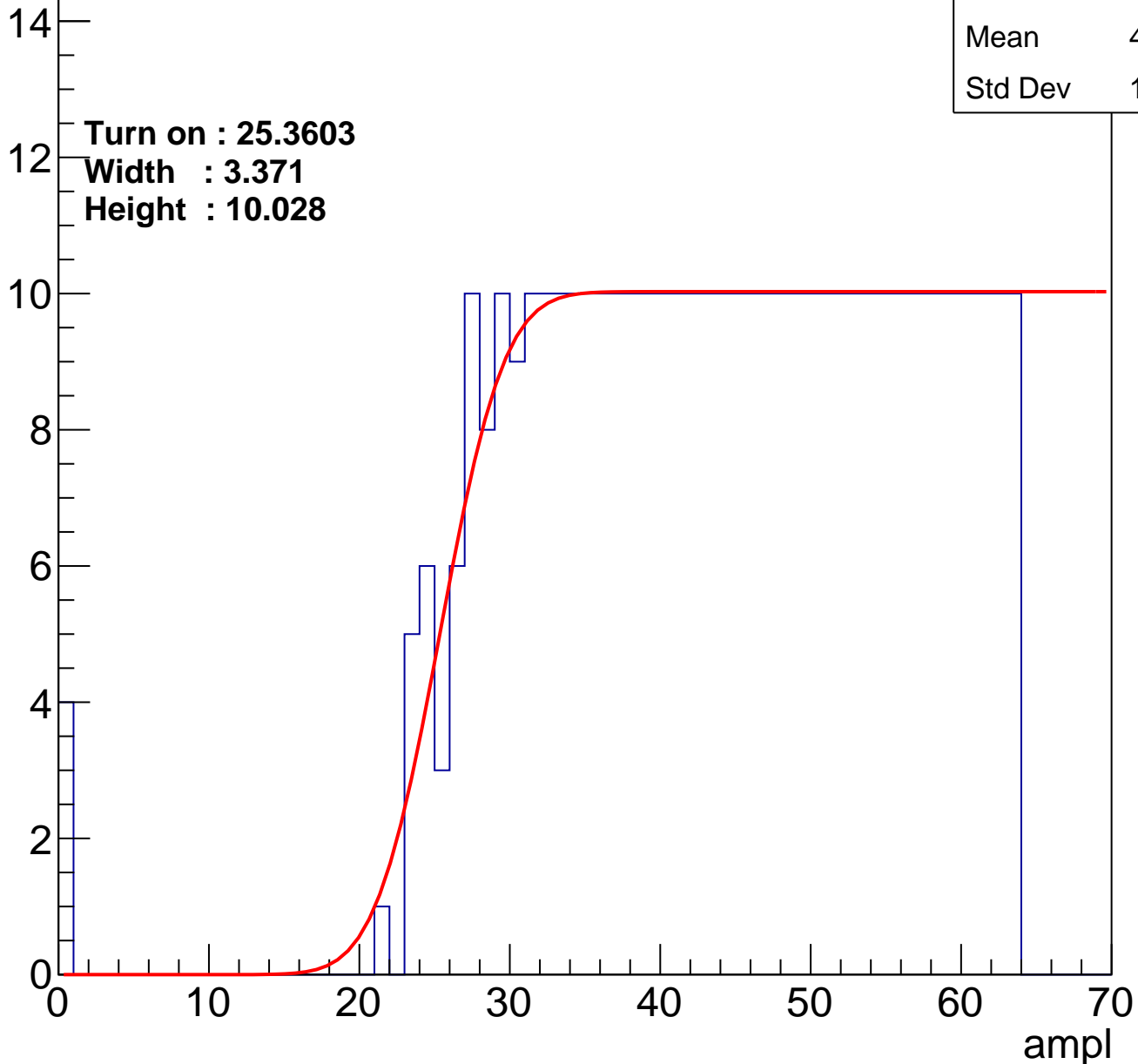
Entries	392
Mean	43.56
Std Dev	12.13

Turn on : 25.3603

Width : 3.371

Height : 10.028

Entry



B1L101S, U20-ch33

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.58
Std Dev	11.19

Turn on : 26.1685

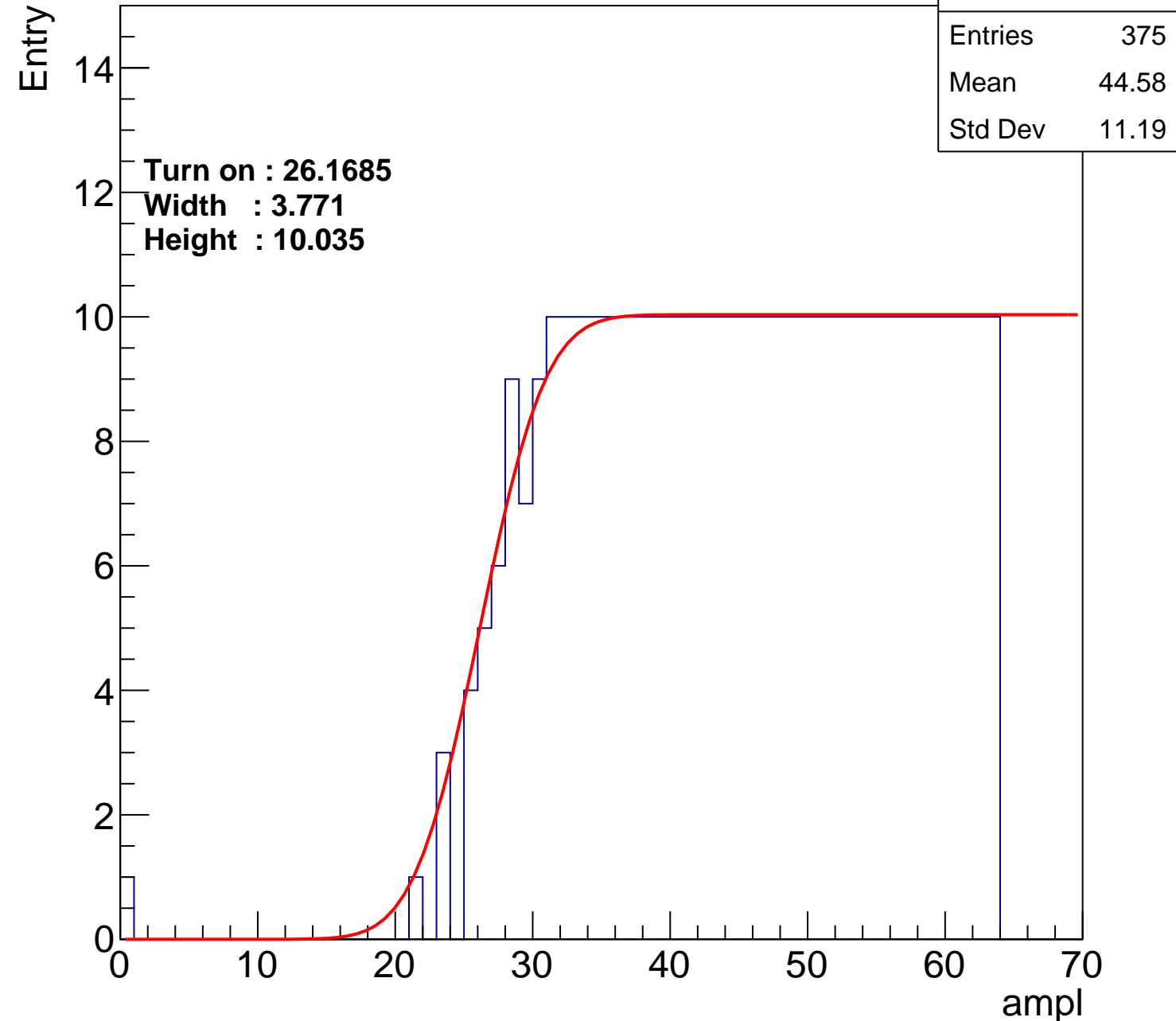
Width : 3.771

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch34

calib_packv5_042523_0143.root, FC#0, port D2

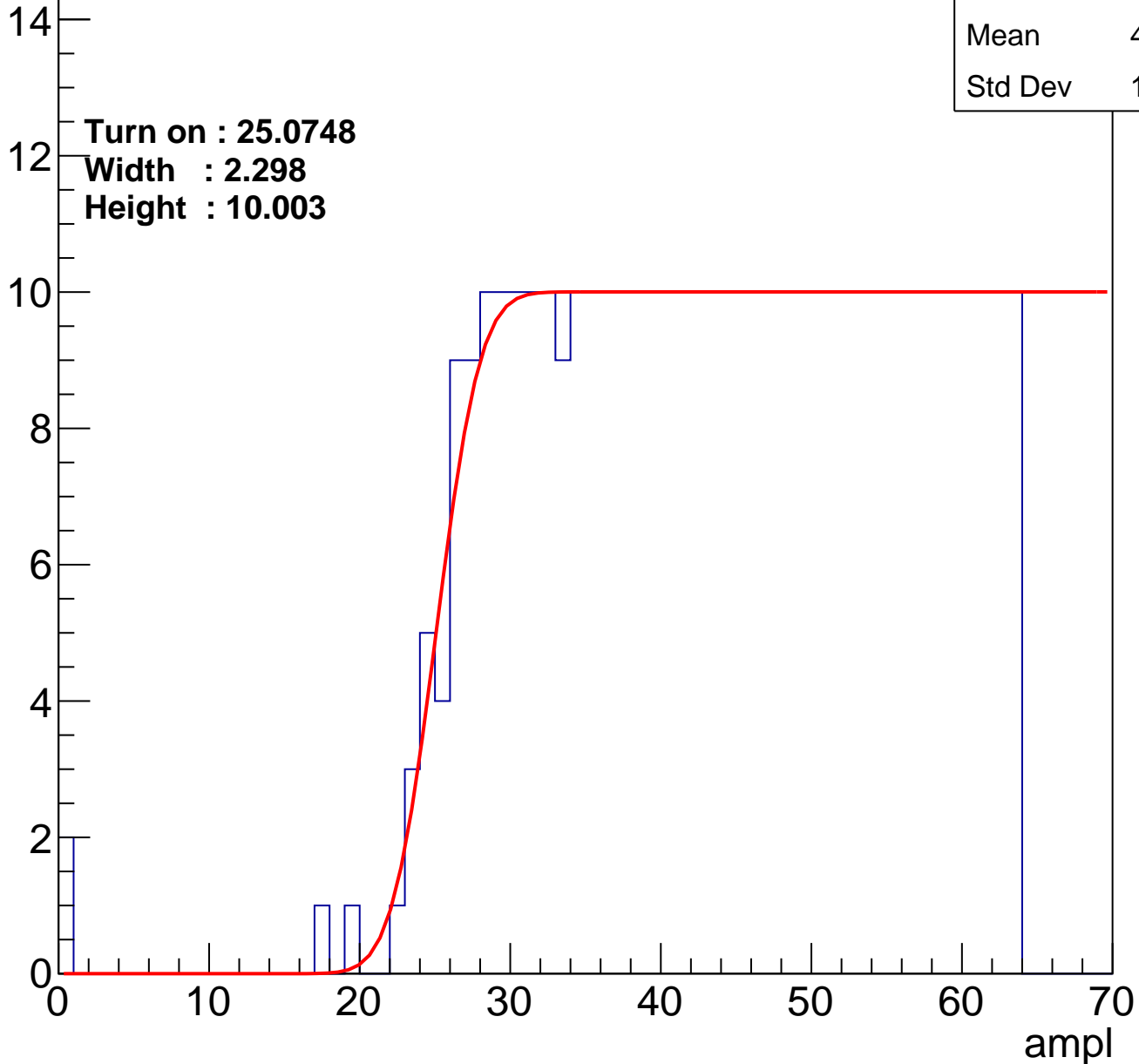
Entries	394
Mean	43.58
Std Dev	11.86

Turn on : 25.0748

Width : 2.298

Height : 10.003

Entry



B1L101S, U20-ch35

calib_packv5_042523_0143.root, FC#0, port D2

Entries	368
Mean	44.88
Std Dev	11.35

Turn on : 24.7384

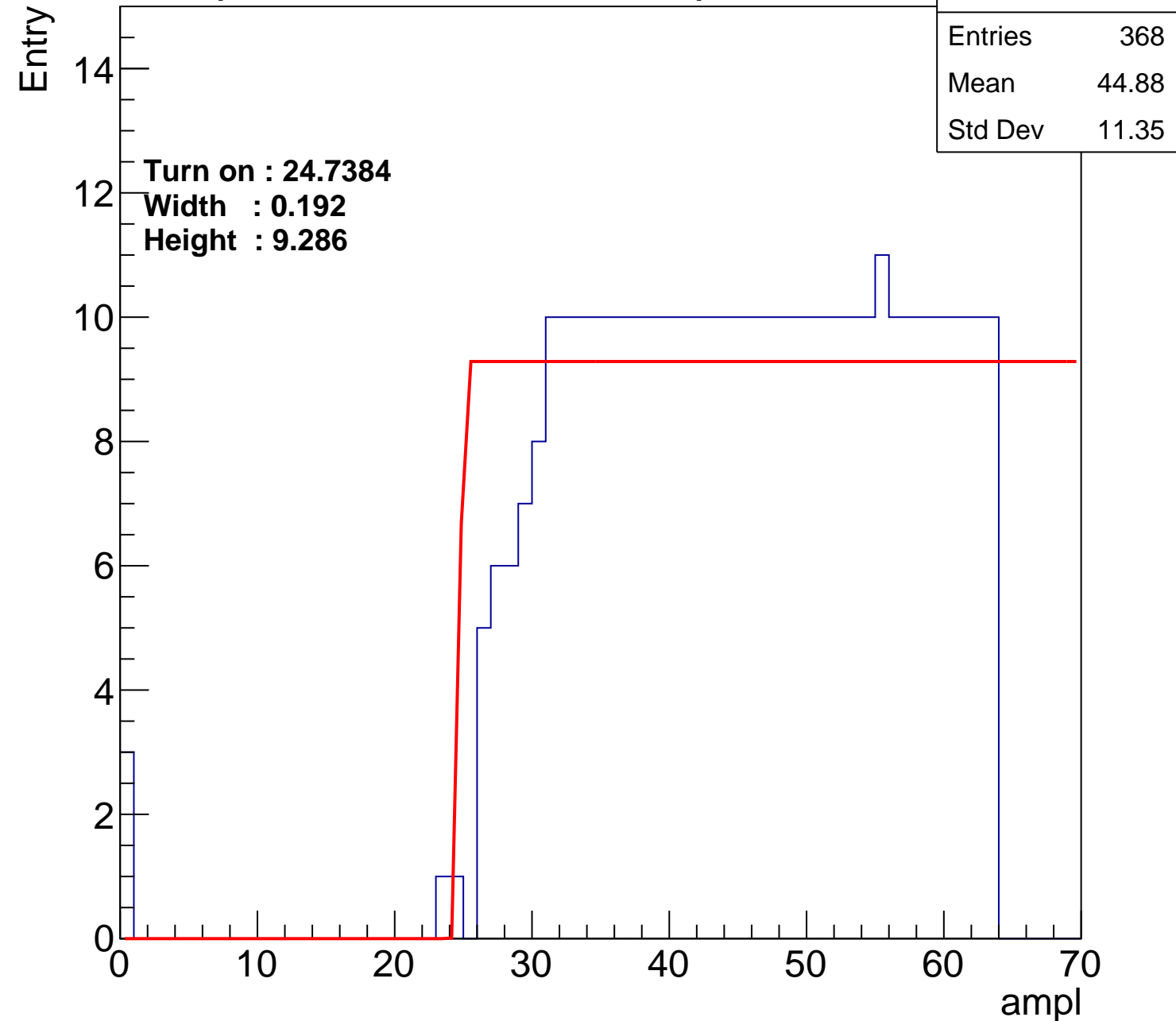
Width : 0.192

Height : 9.286

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch36

calib_packv5_042523_0143.root, FC#0, port D2

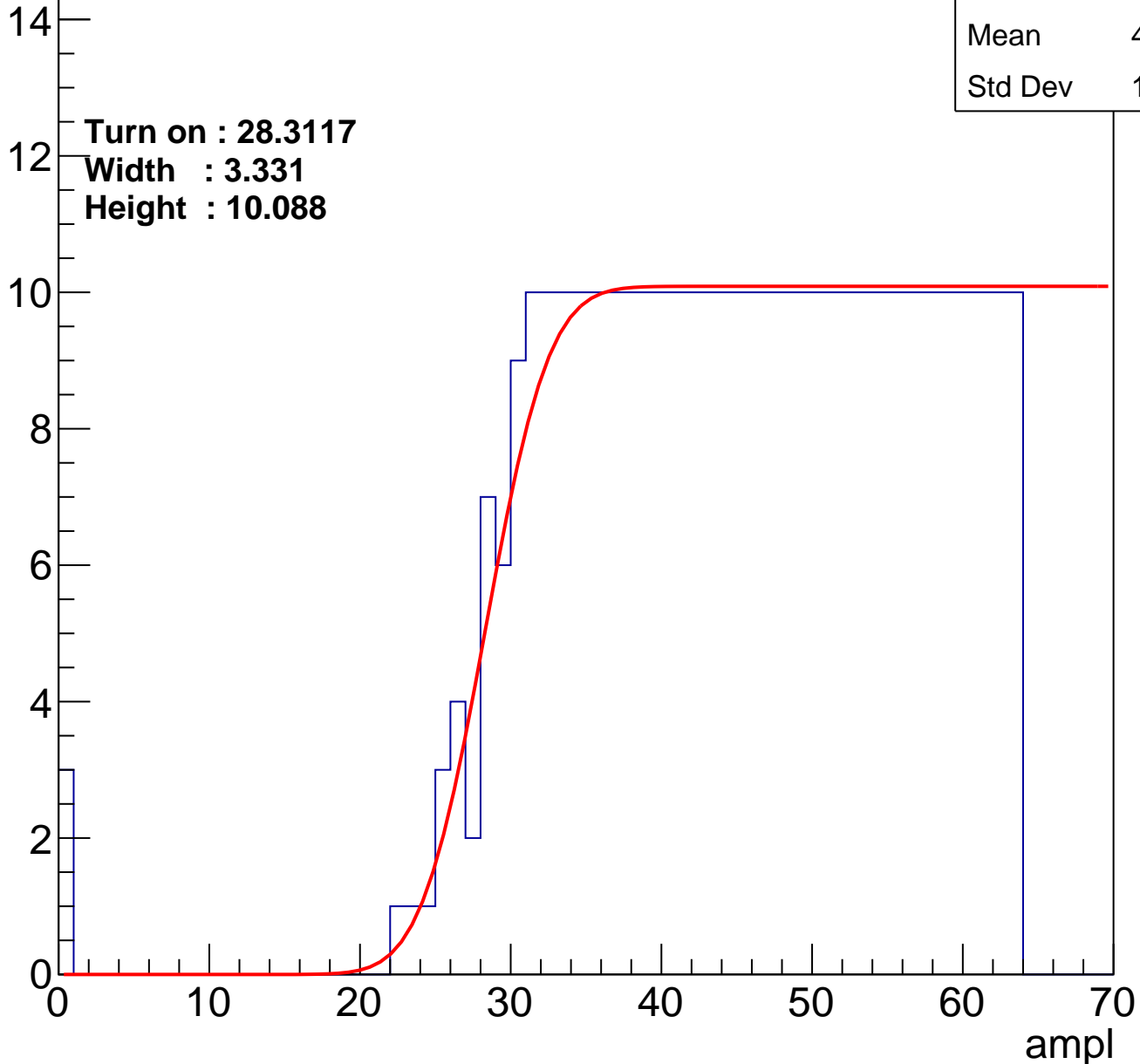
Entries	367
Mean	44.83
Std Dev	11.39

Turn on : 28.3117

Width : 3.331

Height : 10.088

Entry



B1L101S, U20-ch37

calib_packv5_042523_0143.root, FC#0, port D2

Entries	368
Mean	44.51
Std Dev	12.06

Turn on : 27.4131

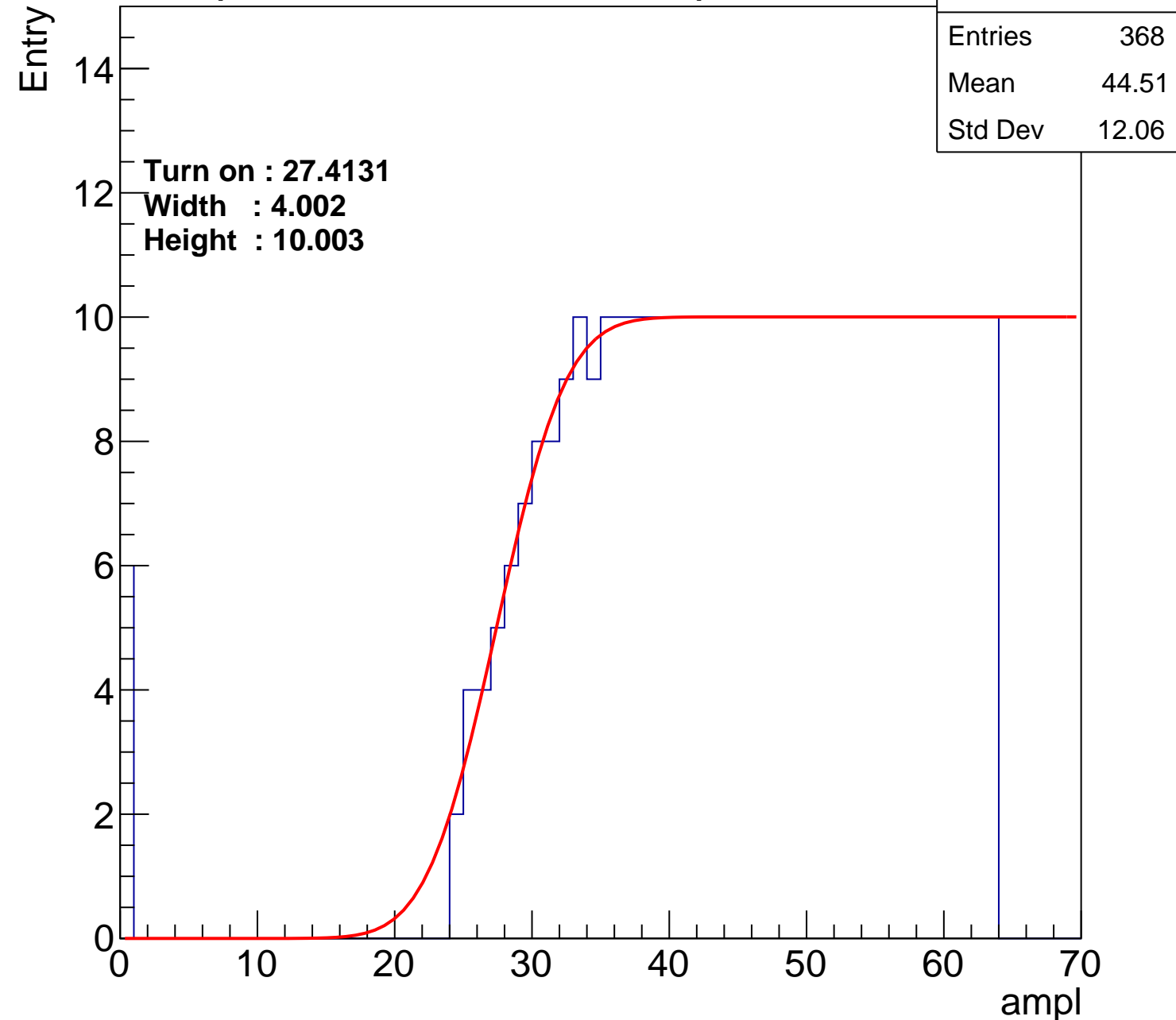
Width : 4.002

Height : 10.003

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch38

calib_packv5_042523_0143.root, FC#0, port D2

Entries	387
Mean	43.86
Std Dev	11.85

Turn on : 26.0741

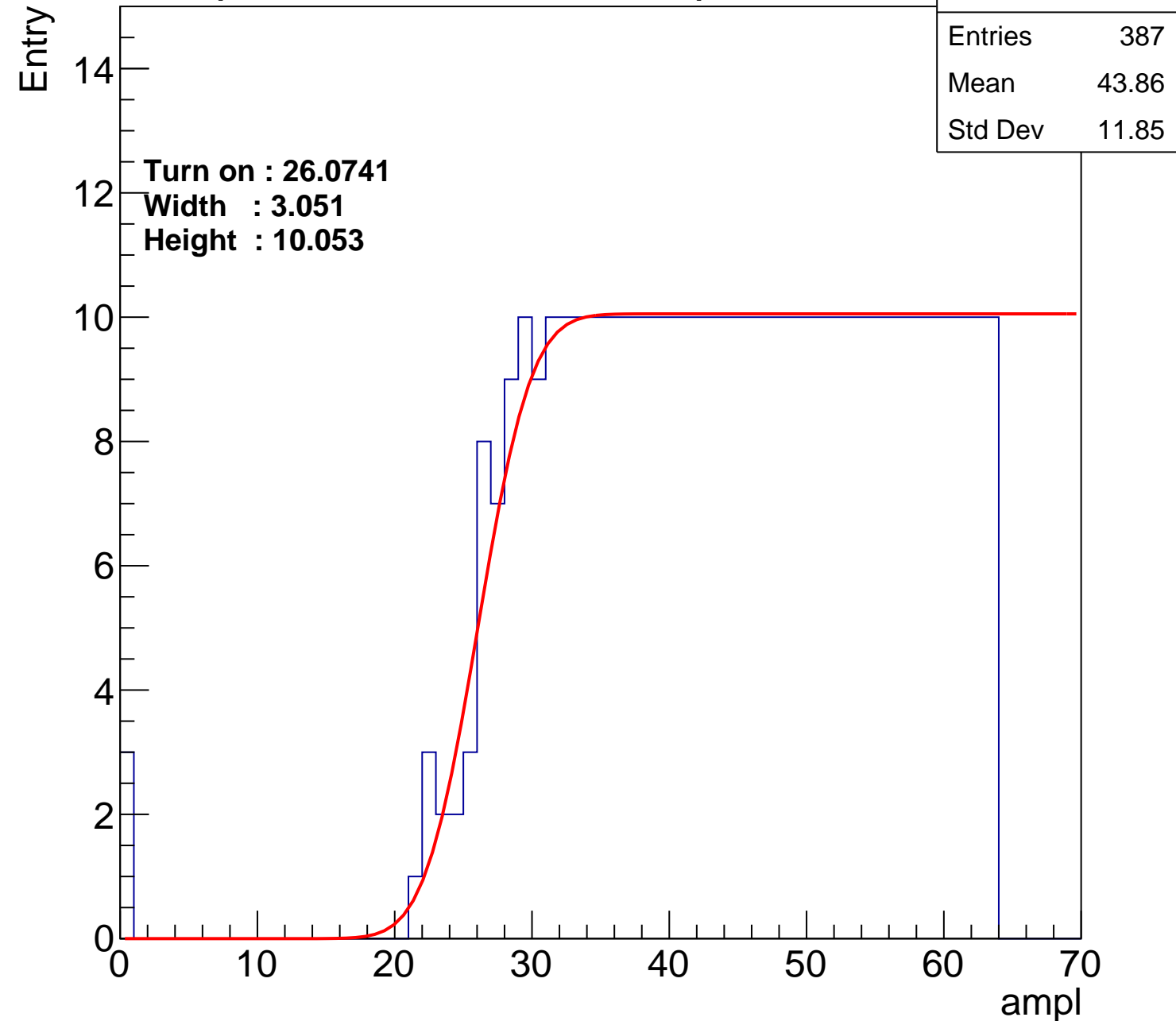
Width : 3.051

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch39

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.48
Std Dev	11.58

Turn on : 27.7083

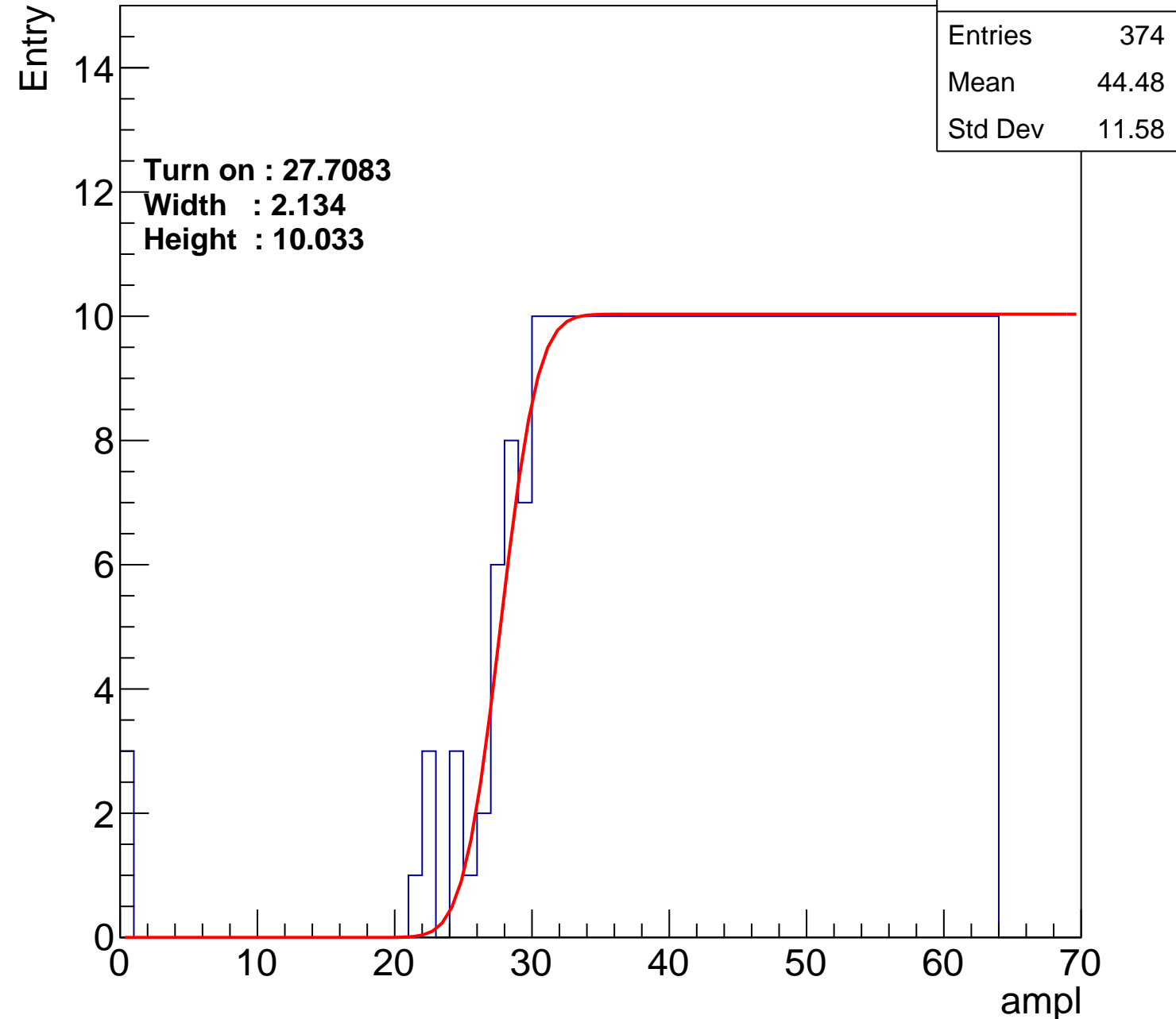
Width : 2.134

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch40

calib_packv5_042523_0143.root, FC#0, port D2

Entries	369
Mean	44.41
Std Dev	12.24

Turn on : 28.5912

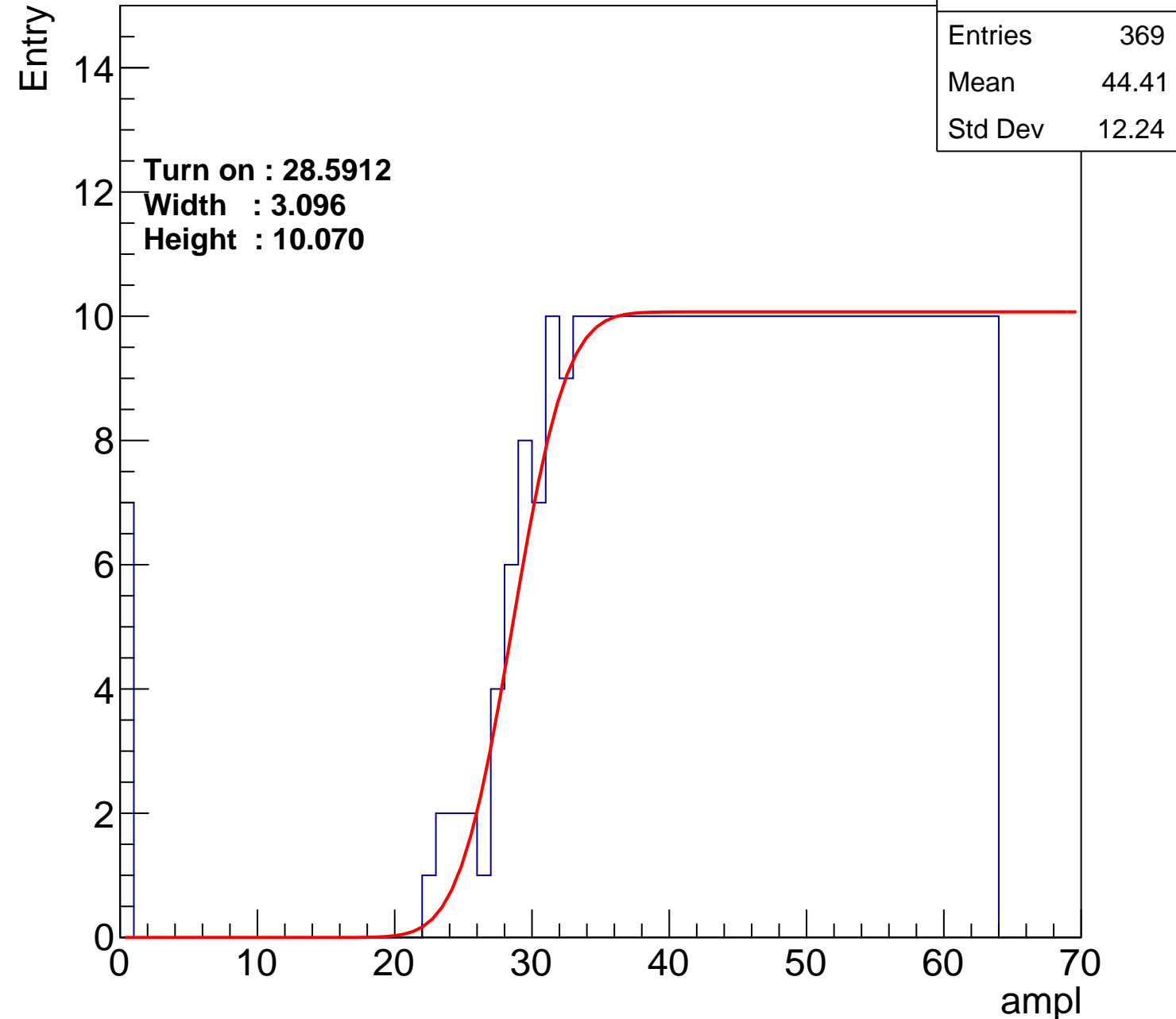
Width : 3.096

Height : 10.070

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch41

calib_packv5_042523_0143.root, FC#0, port D2

Entries	373
Mean	44.51
Std Dev	11.56

Turn on : 27.6079

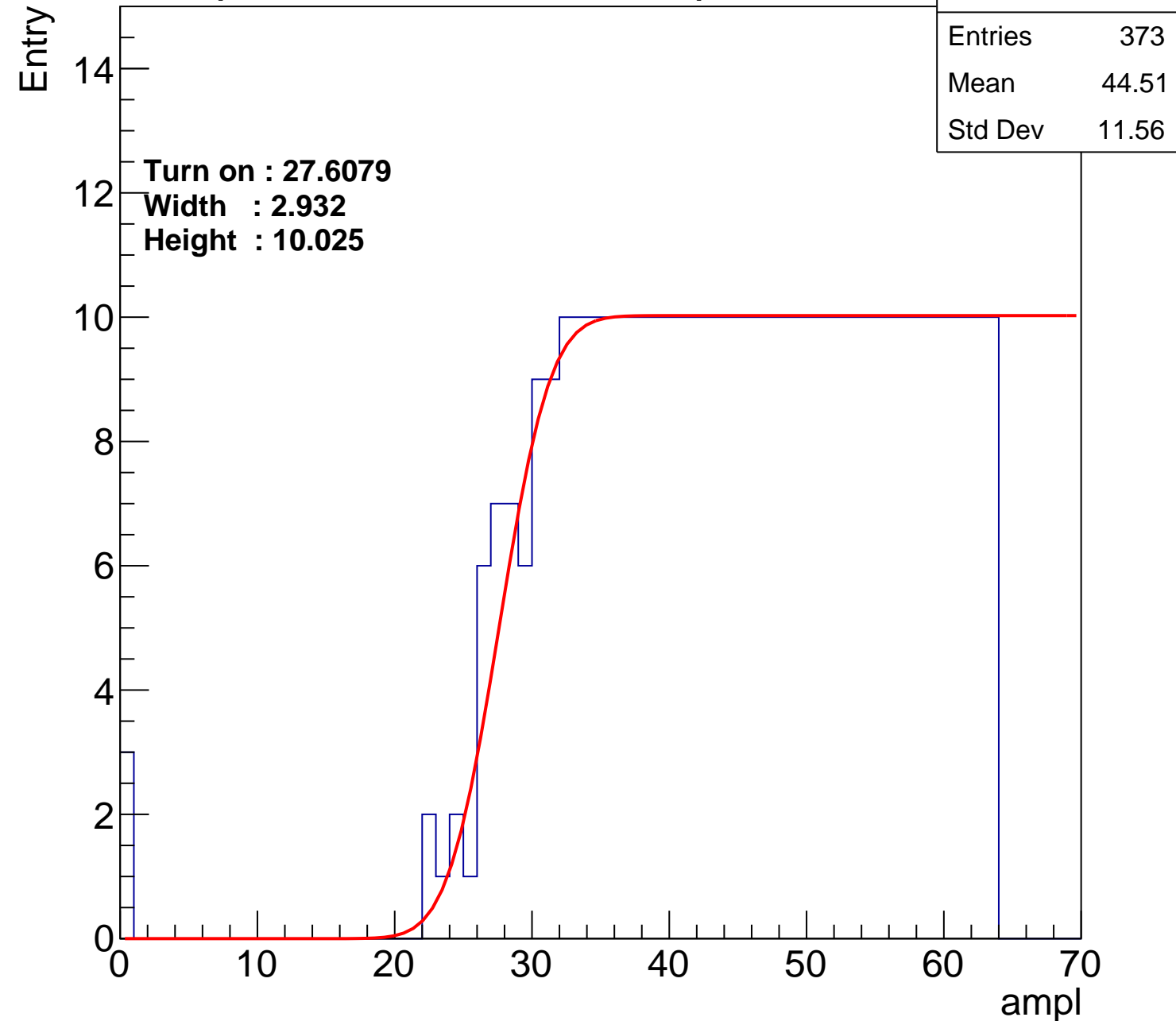
Width : 2.932

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch42

calib_packv5_042523_0143.root, FC#0, port D2

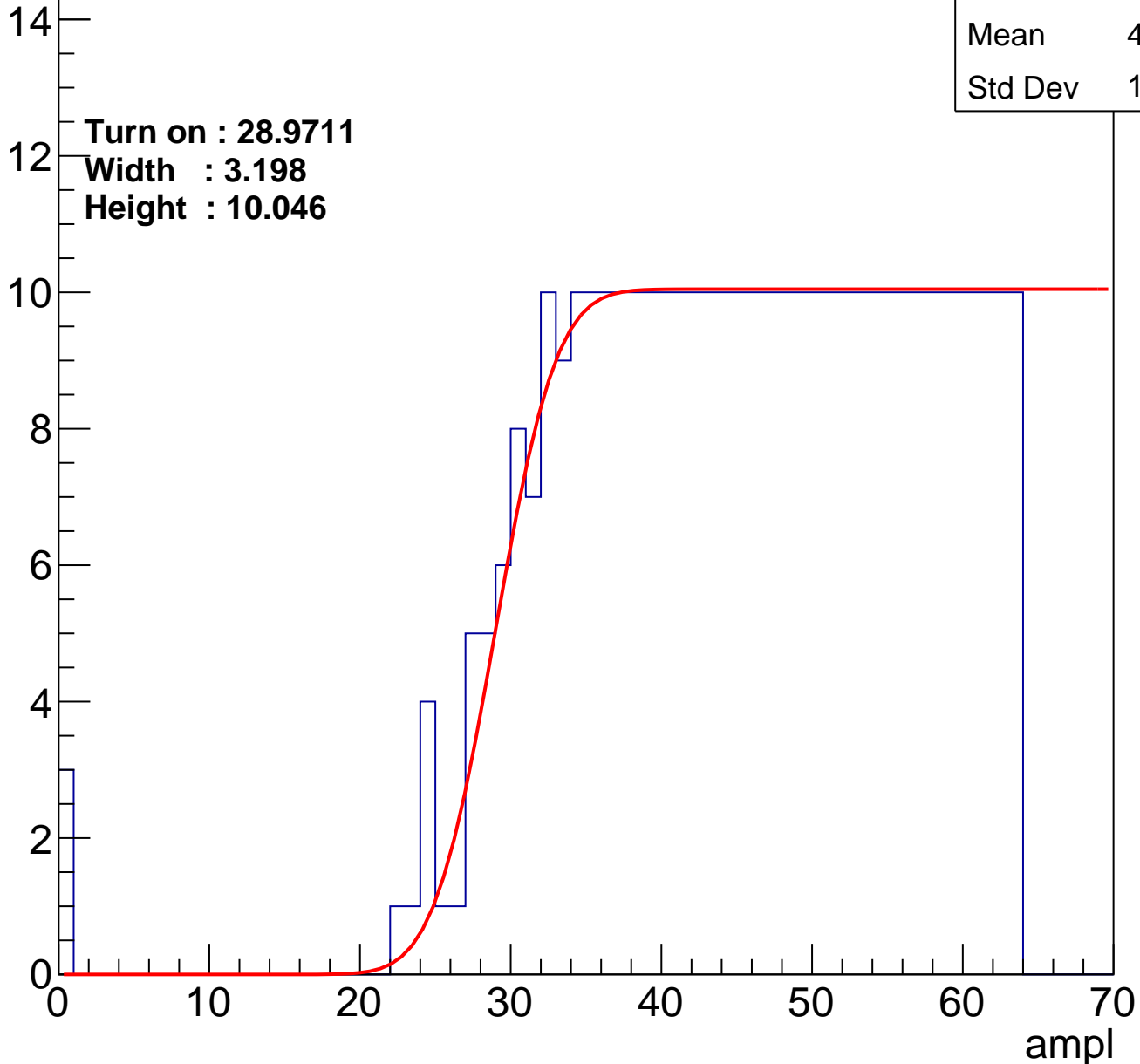
Entries	361
Mean	45.06
Std Dev	11.35

Turn on : 28.9711

Width : 3.198

Height : 10.046

Entry



B1L101S, U20-ch43

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.4
Std Dev	11.46

Turn on : 26.1900

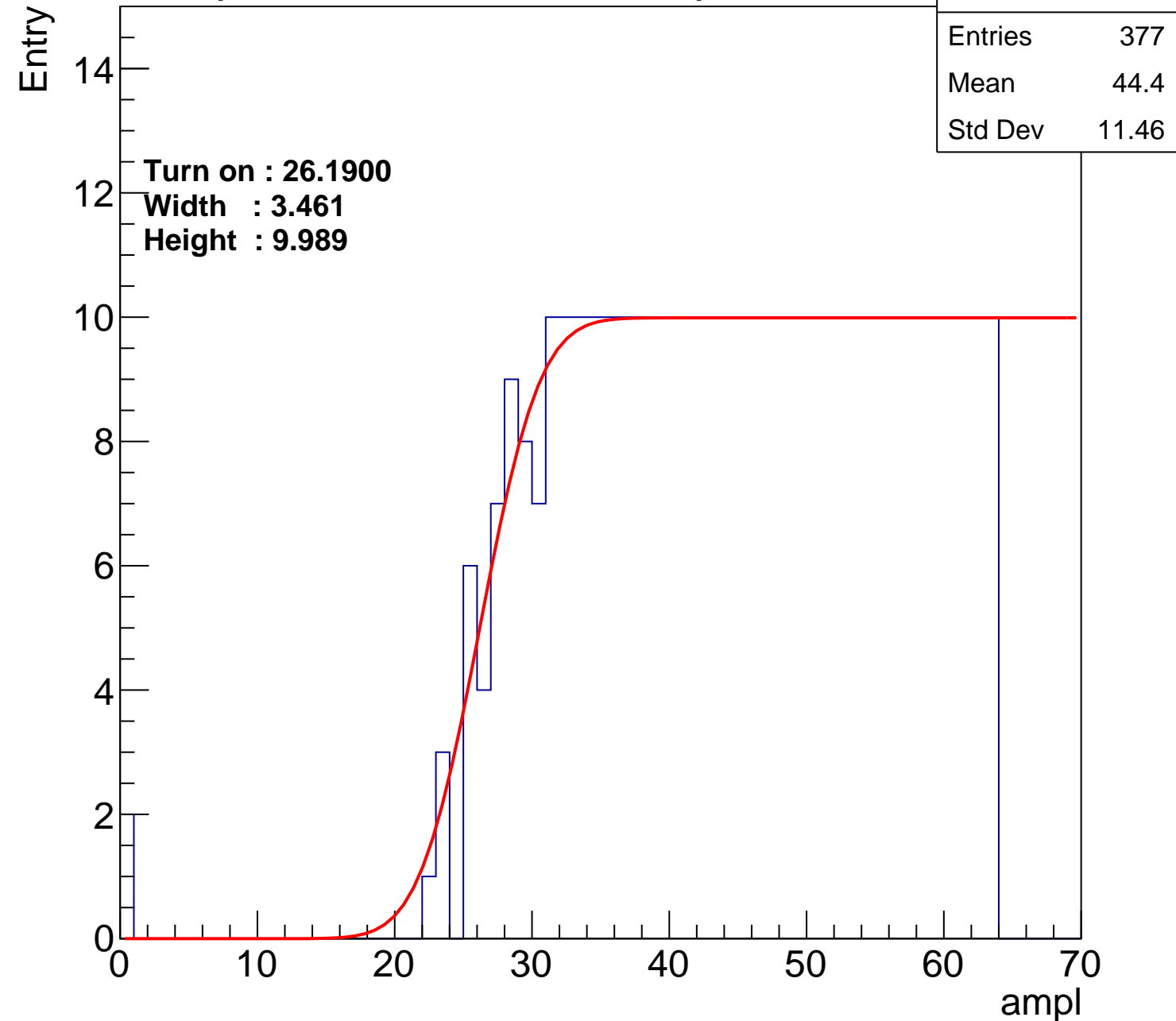
Width : 3.461

Height : 9.989

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch44

calib_packv5_042523_0143.root, FC#0, port D2

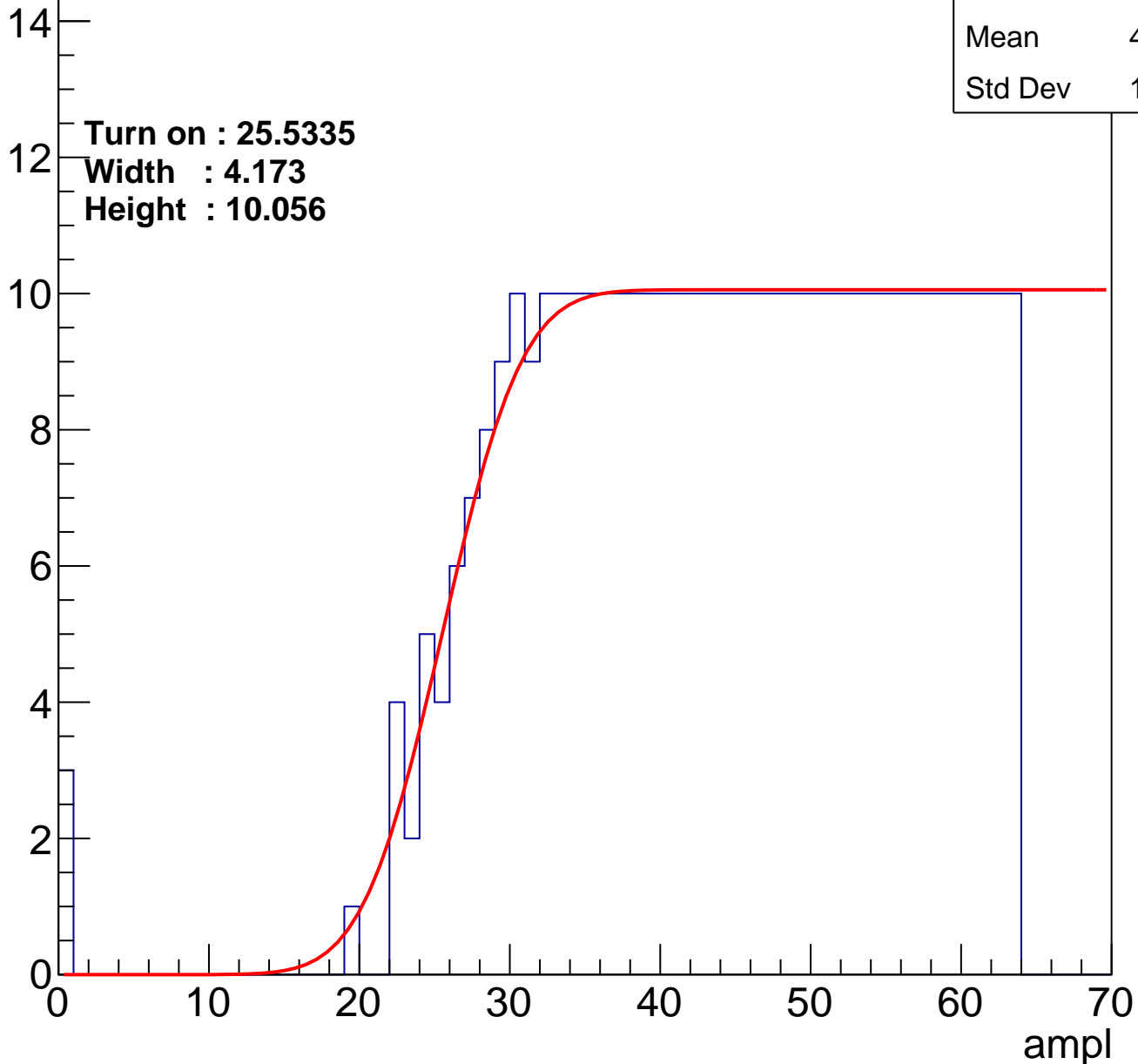
Entries	388
Mean	43.77
Std Dev	11.95

Turn on : 25.5335

Width : 4.173

Height : 10.056

Entry



B1L101S, U20-ch45

calib_packv5_042523_0143.root, FC#0, port D2

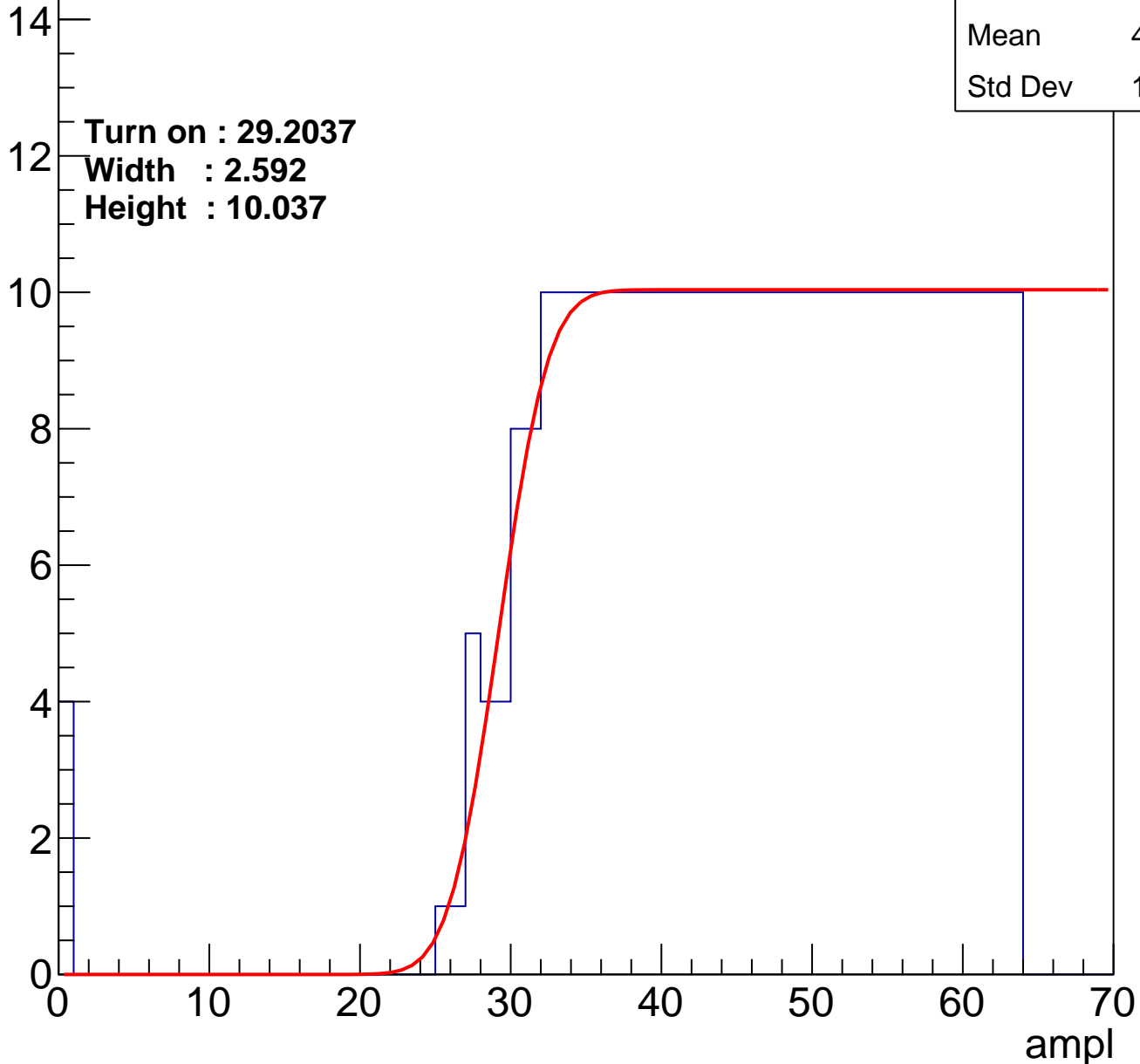
Entries	355
Mean	45.36
Std Dev	11.29

Turn on : 29.2037

Width : 2.592

Height : 10.037

Entry



B1L101S, U20-ch46

calib_packv5_042523_0143.root, FC#0, port D2

Entries	384
Mean	43.86
Std Dev	12.15

Turn on : 26.3520

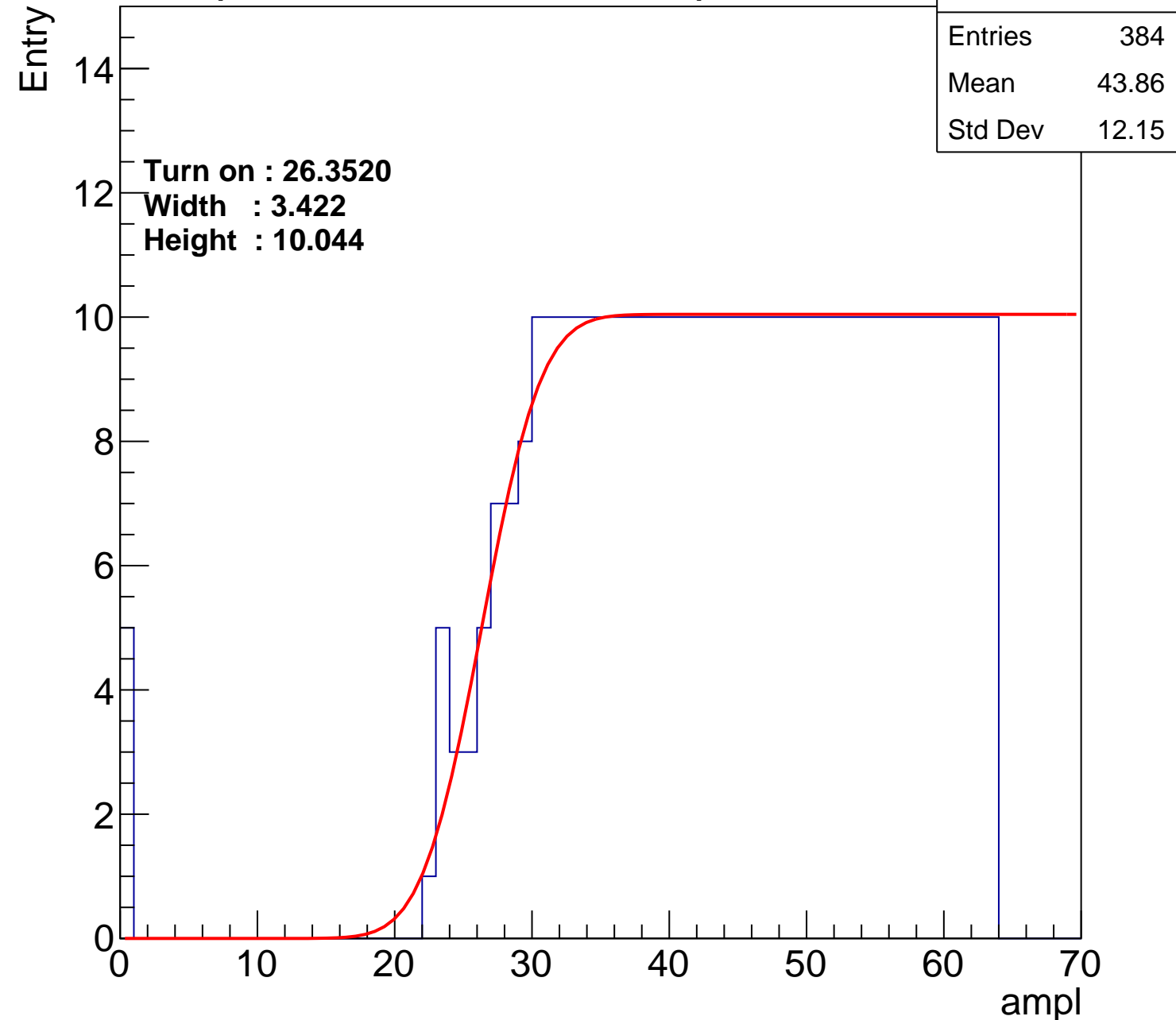
Width : 3.422

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



calib_packv5_042523_0143.root, FC#0, port D2

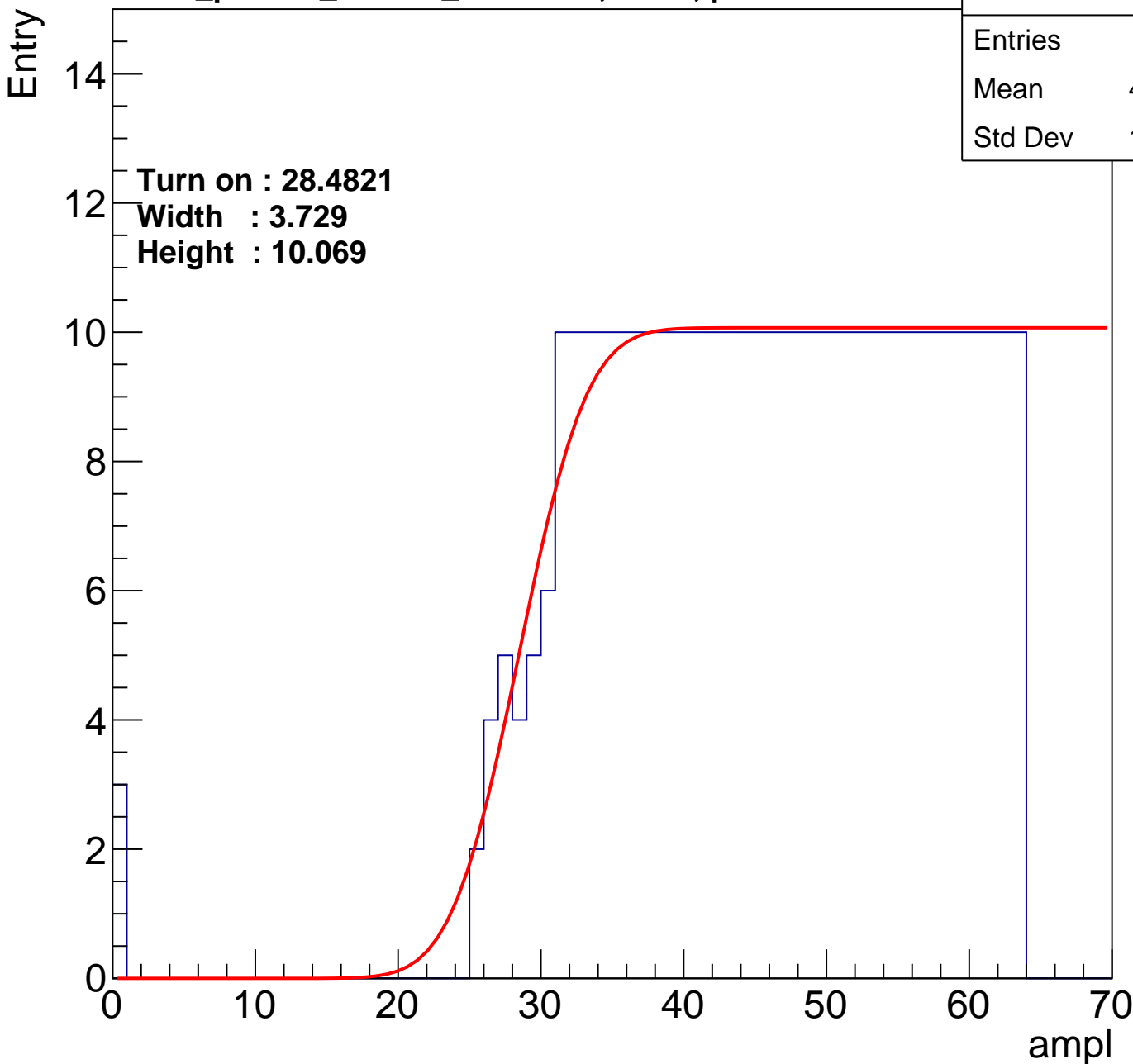
Entries	359
Mean	45.23
Std Dev	11.19

Mean	45.23
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Std Dev	11.19
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Width : 3.729

Height : 10.069



B1L101S, U20-ch48

calib_packv5_042523_0143.root, FC#0, port D2

Entries	396
Mean	43.29
Std Dev	12.4

Turn on : 26.0661

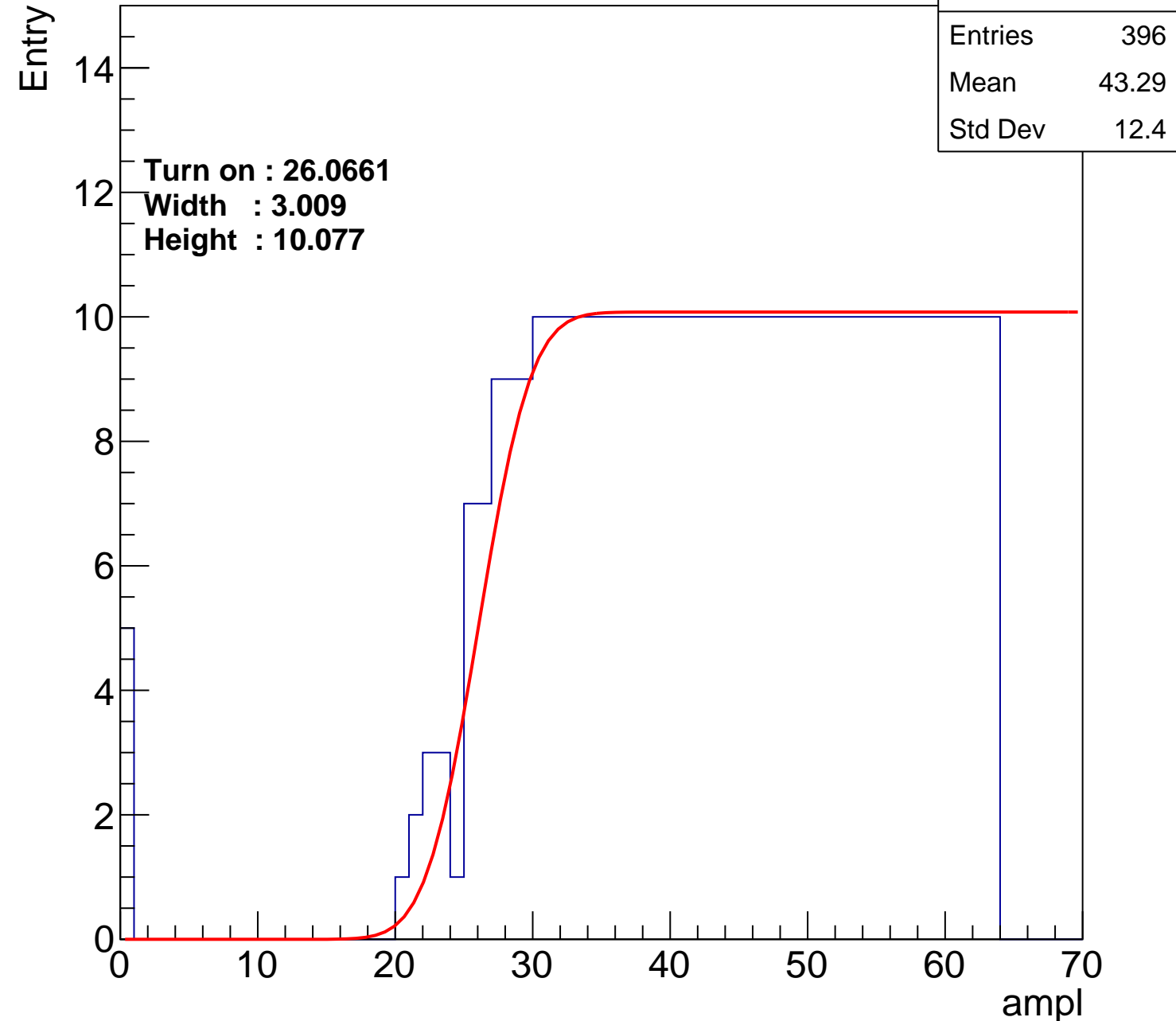
Width : 3.009

Height : 10.077

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch49

calib_packv5_042523_0143.root, FC#0, port D2

Entries	352
Mean	45.51
Std Dev	11.11

Turn on : 30.3794

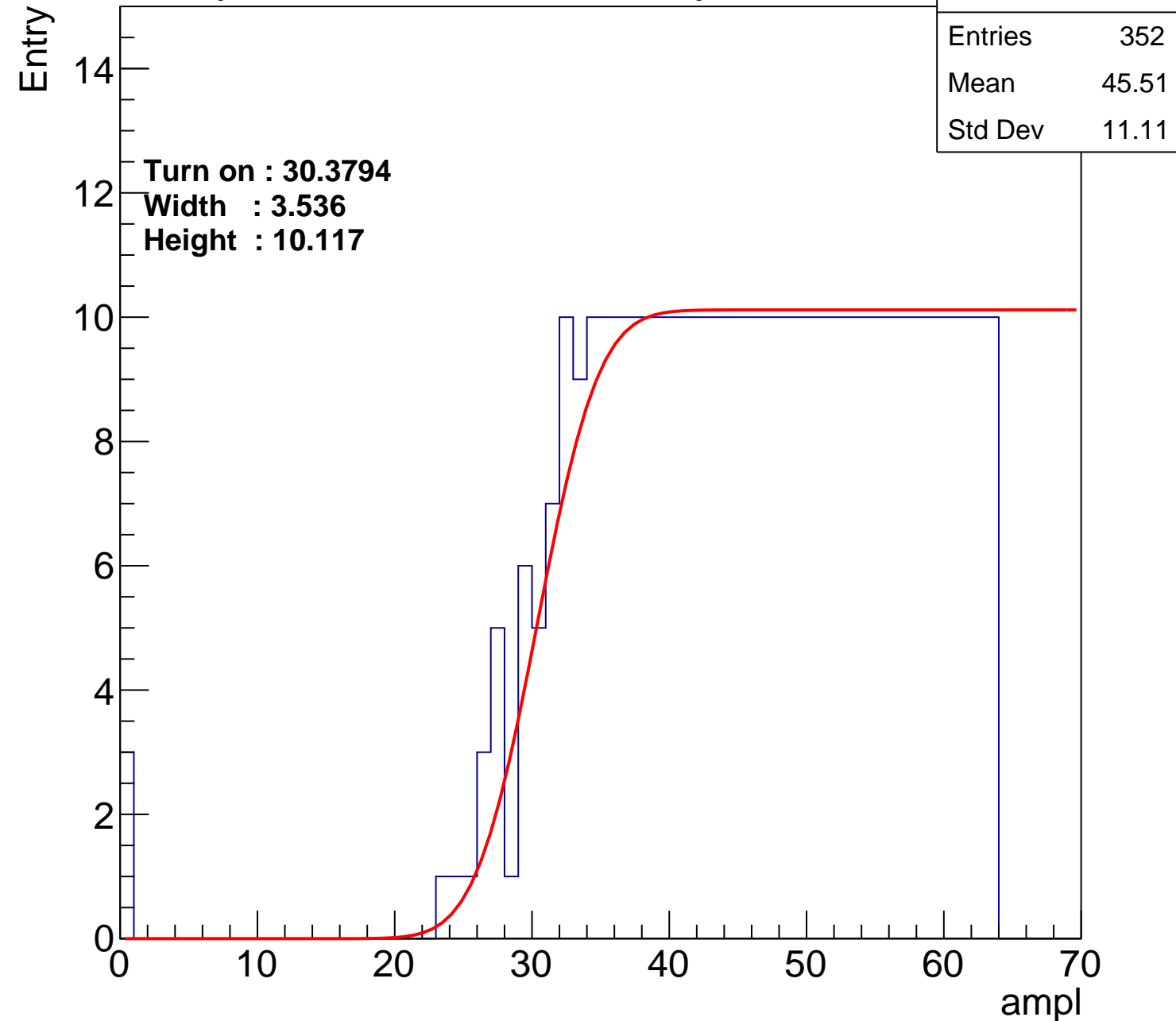
Width : 3.536

Height : 10.117

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch50

calib_packv5_042523_0143.root, FC#0, port D2

Entries	366
Mean	44.93
Std Dev	11.18

Turn on : 27.6488

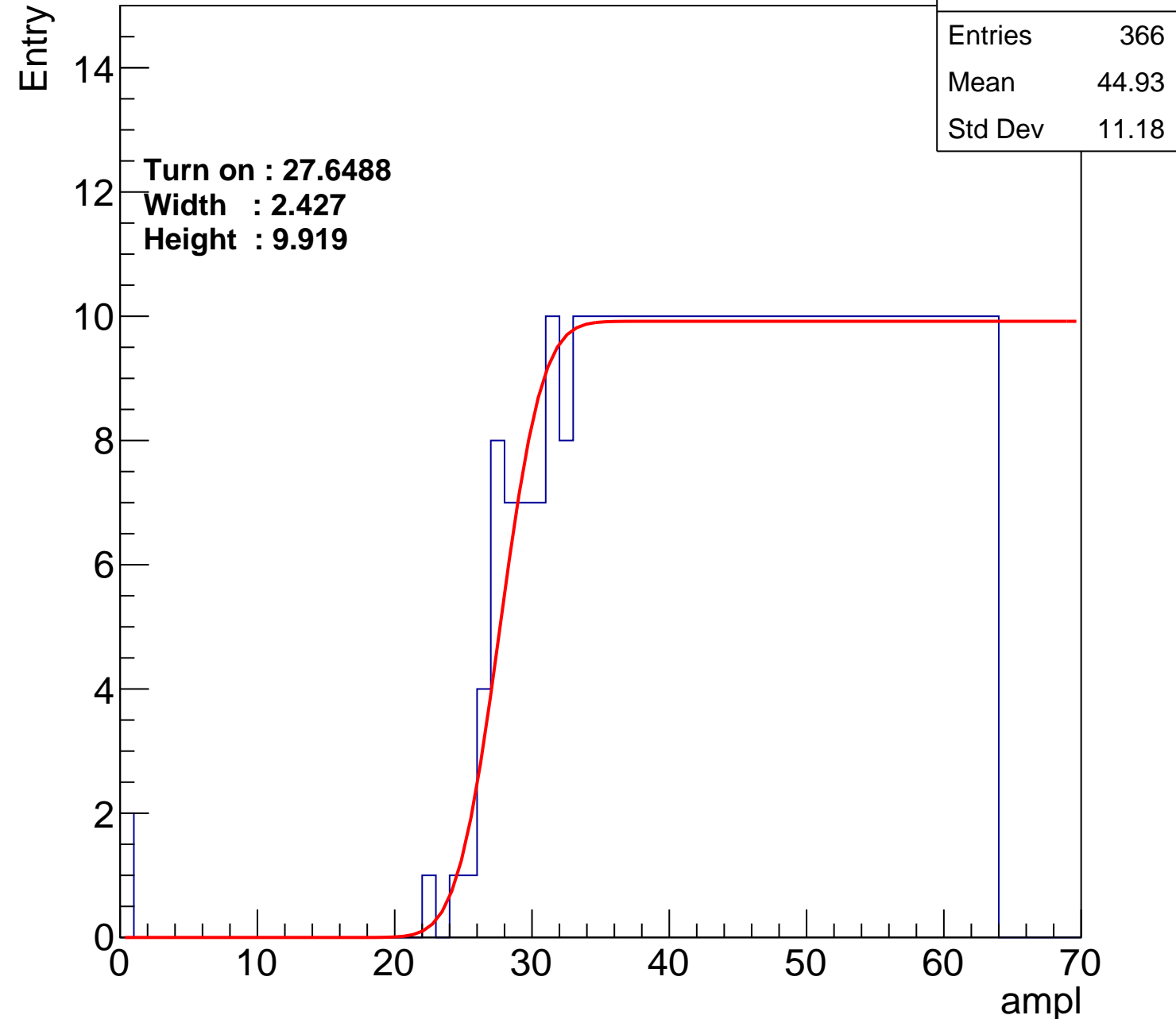
Width : 2.427

Height : 9.919

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch51

calib_packv5_042523_0143.root, FC#0, port D2

Entries	367
Mean	44.85
Std Dev	11.35

Turn on : 27.6662

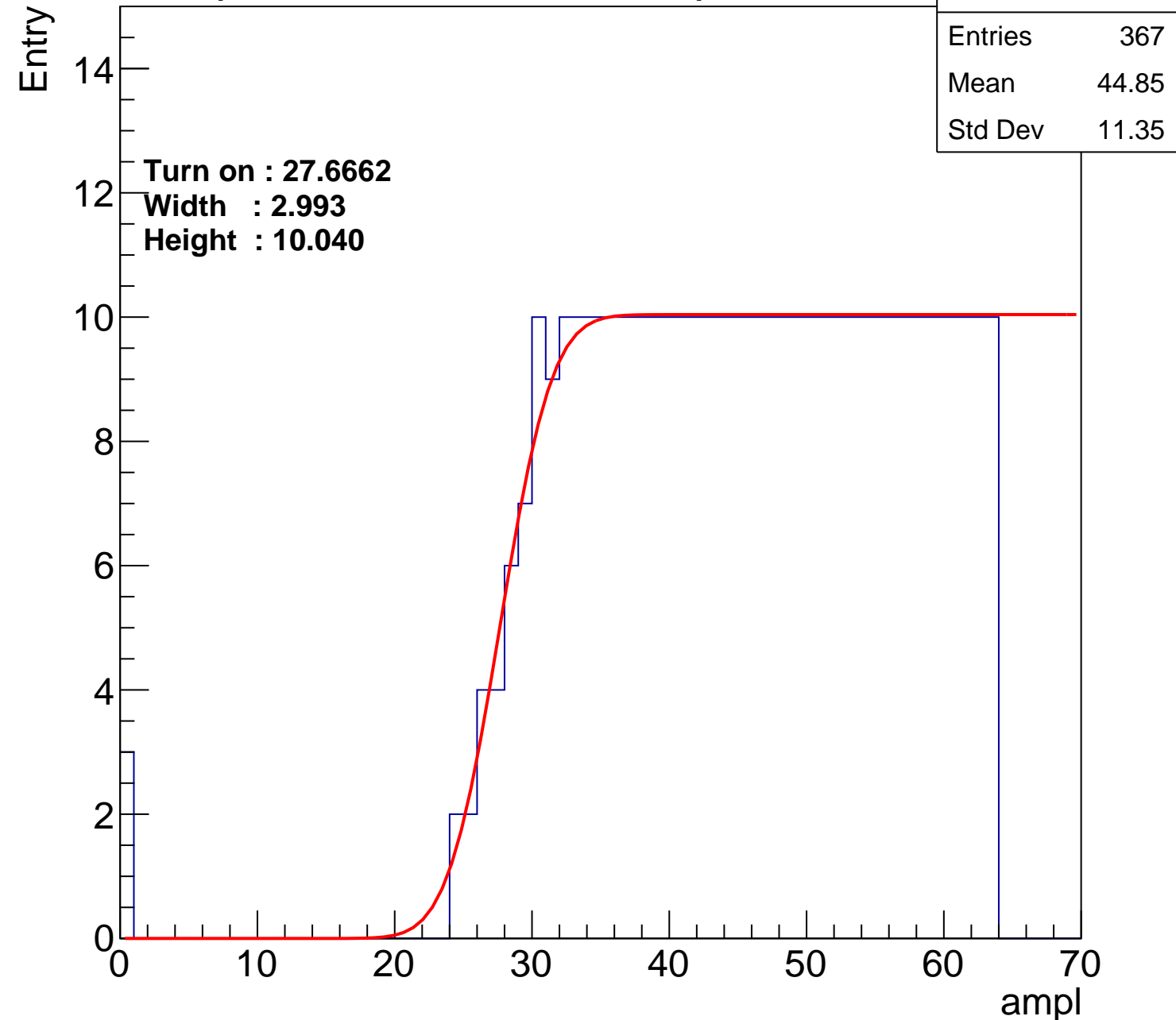
Width : 2.993

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch52

calib_packv5_042523_0143.root, FC#0, port D2

Entries	381
Mean	44.21
Std Dev	11.54

Turn on : 26.5310

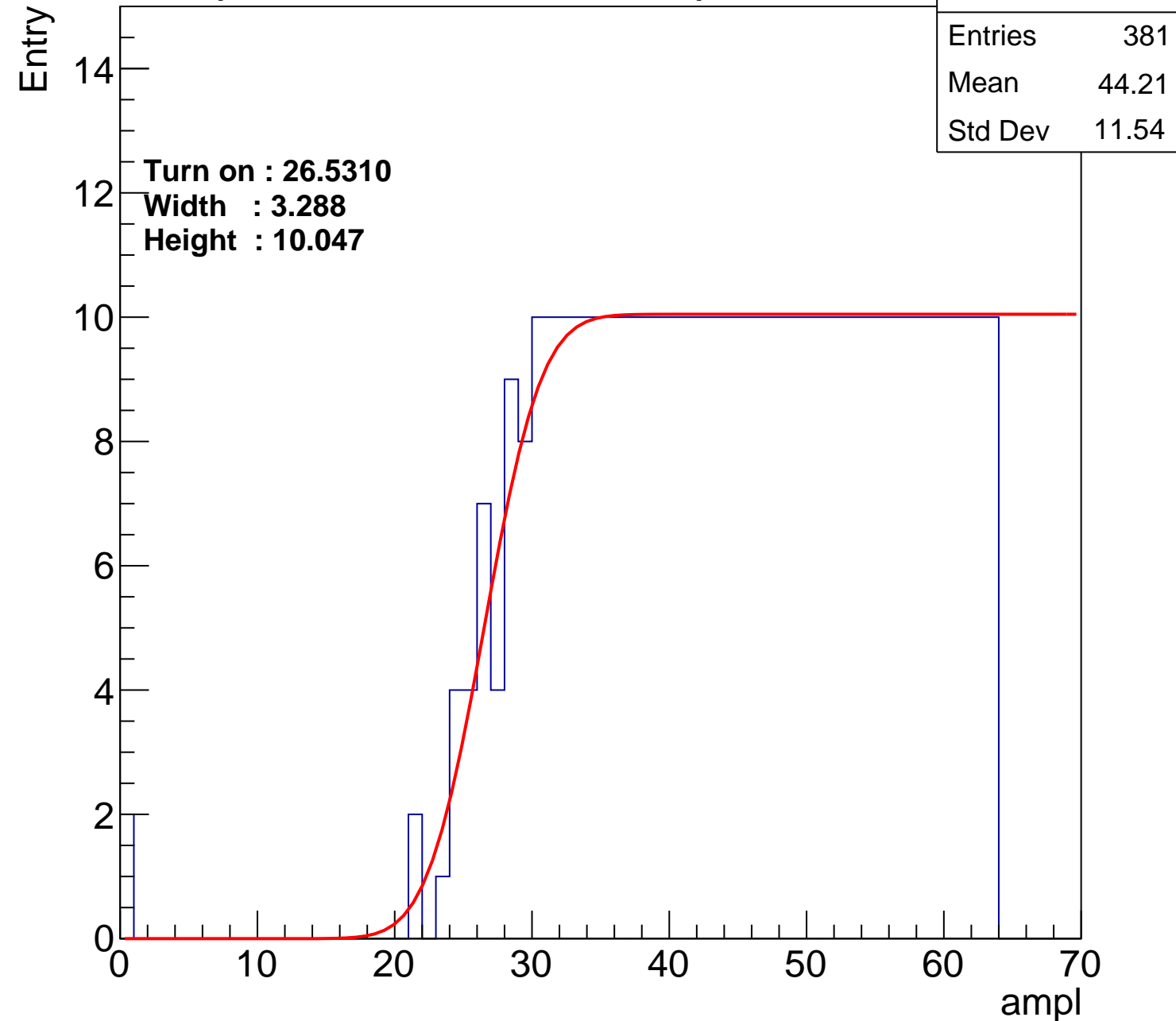
Width : 3.288

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch53

calib_packv5_042523_0143.root, FC#0, port D2

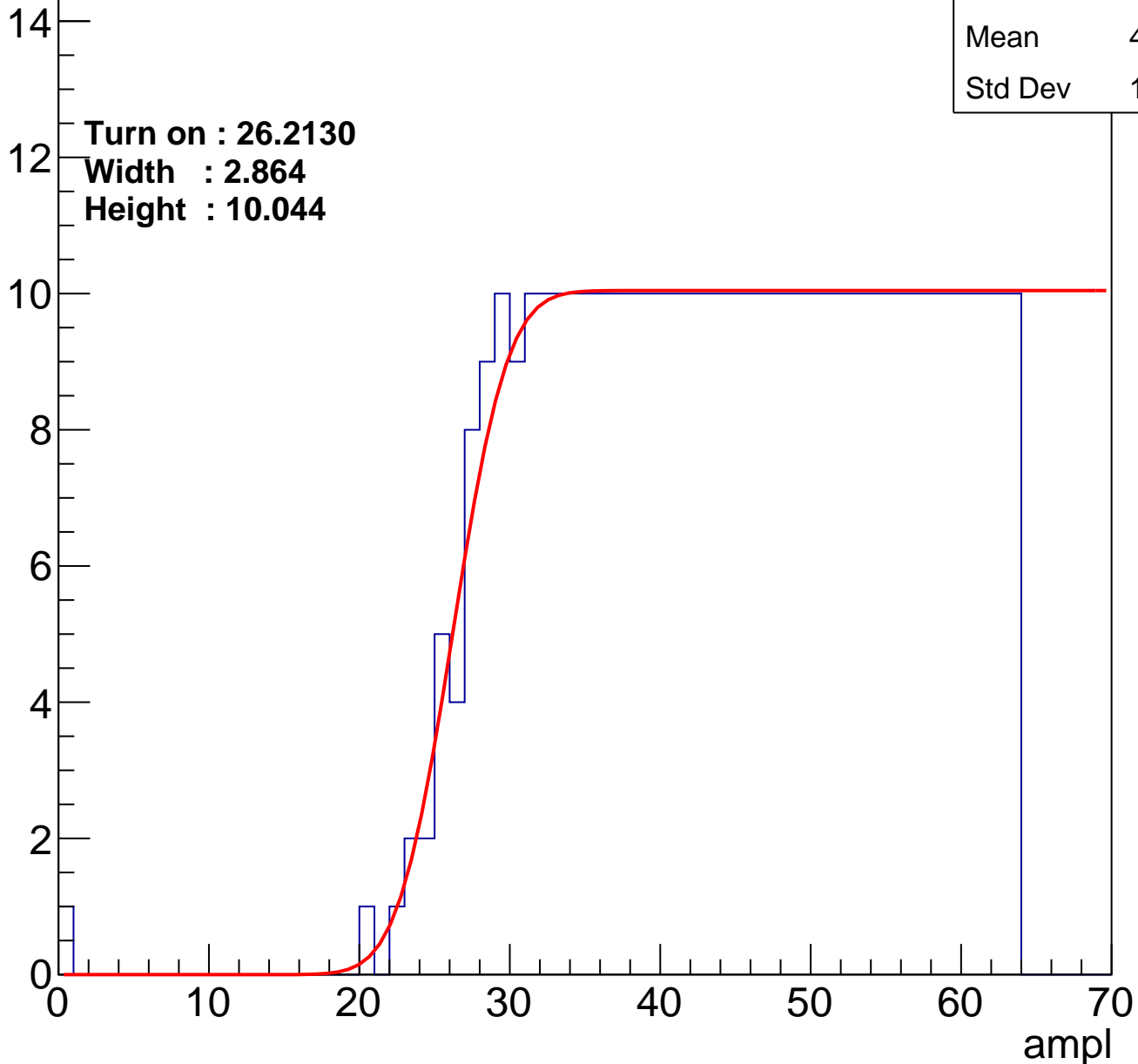
Entries	382
Mean	44.25
Std Dev	11.36

Turn on : 26.2130

Width : 2.864

Height : 10.044

Entry



B1L101S, U20-ch54

calib_packv5_042523_0143.root, FC#0, port D2

Entries	366
Mean	45.02
Std Dev	10.96

Turn on : 28.1617

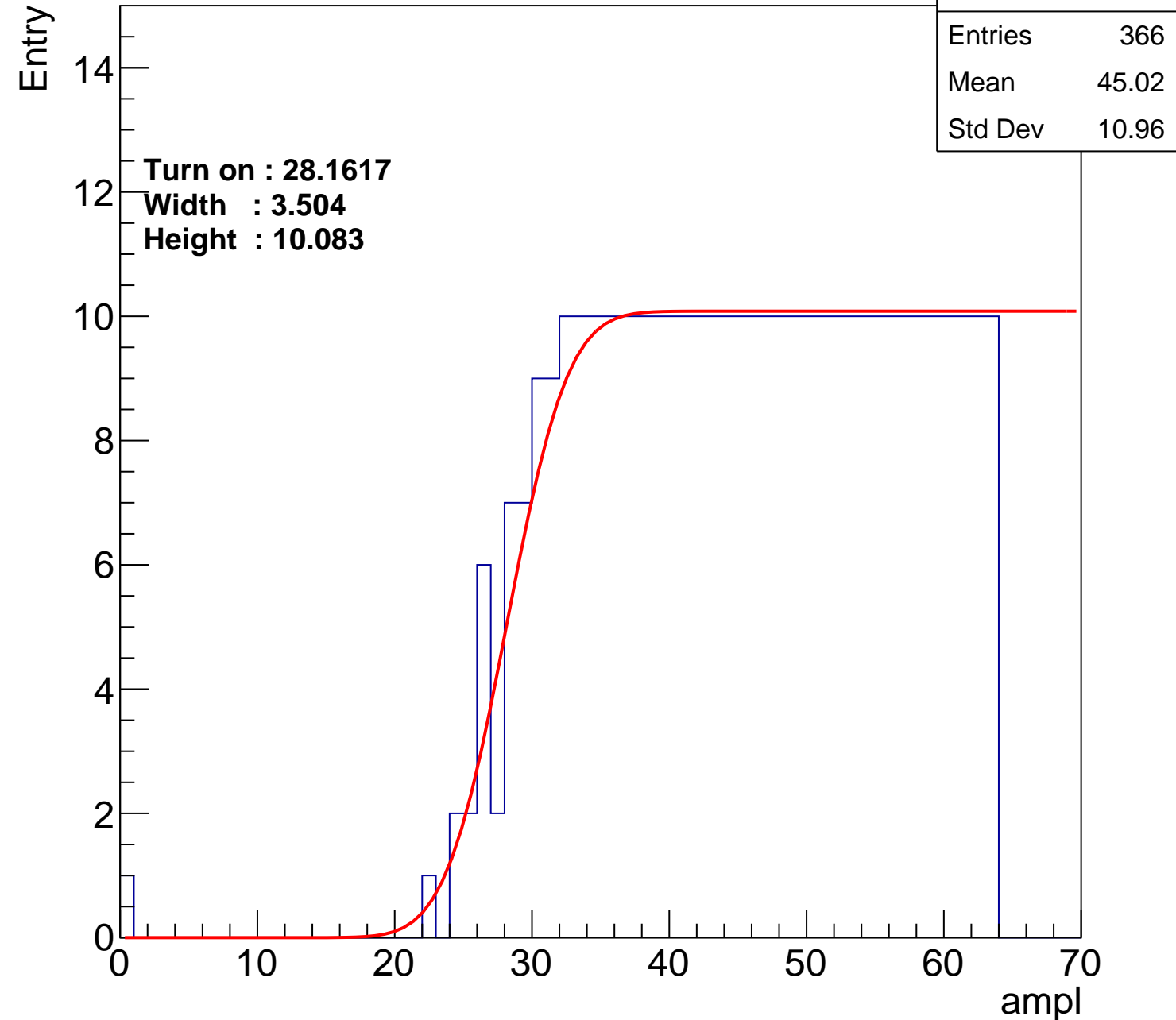
Width : 3.504

Height : 10.083

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch55

calib_packv5_042523_0143.root, FC#0, port D2

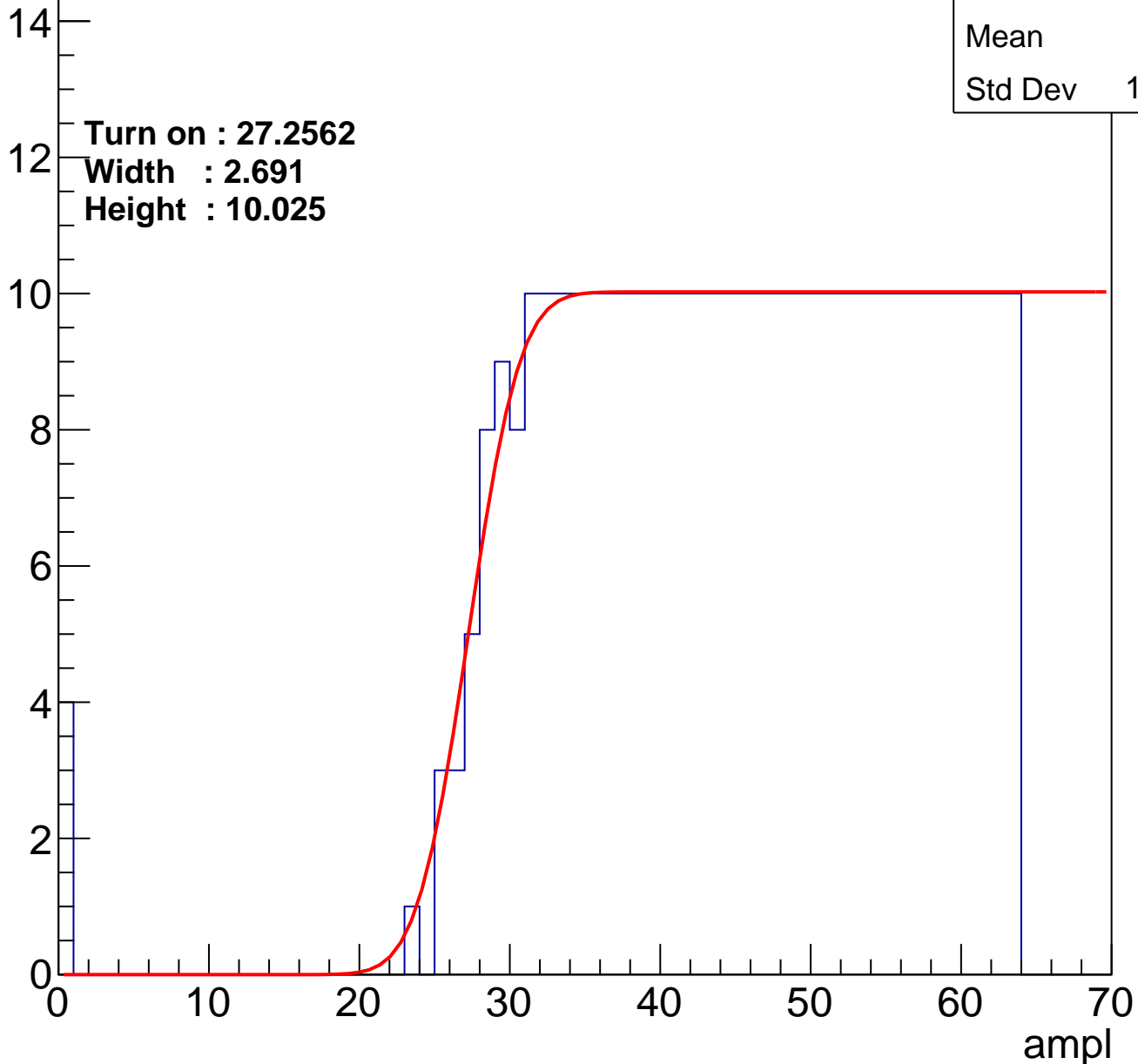
Entries	371
Mean	44.6
Std Dev	11.62

Turn on : 27.2562

Width : 2.691

Height : 10.025

Entry



B1L101S, U20-ch56

calib_packv5_042523_0143.root, FC#0, port D2

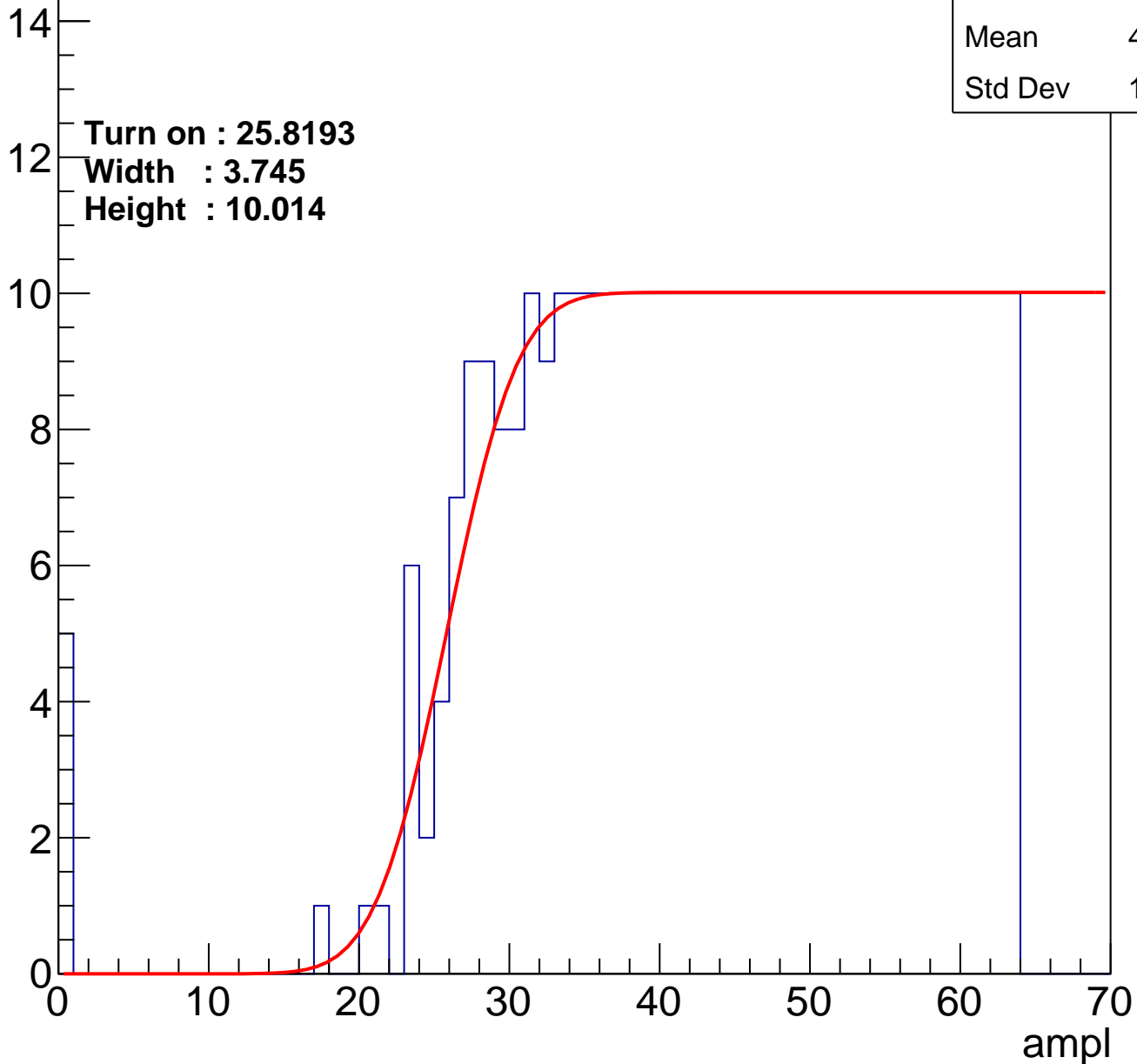
Entries	390
Mean	43.52
Std Dev	12.36

Turn on : 25.8193

Width : 3.745

Height : 10.014

Entry



B1L101S, U20-ch57

calib_packv5_042523_0143.root, FC#0, port D2

Entries	386
Mean	43.96
Std Dev	11.68

Turn on : 26.1642

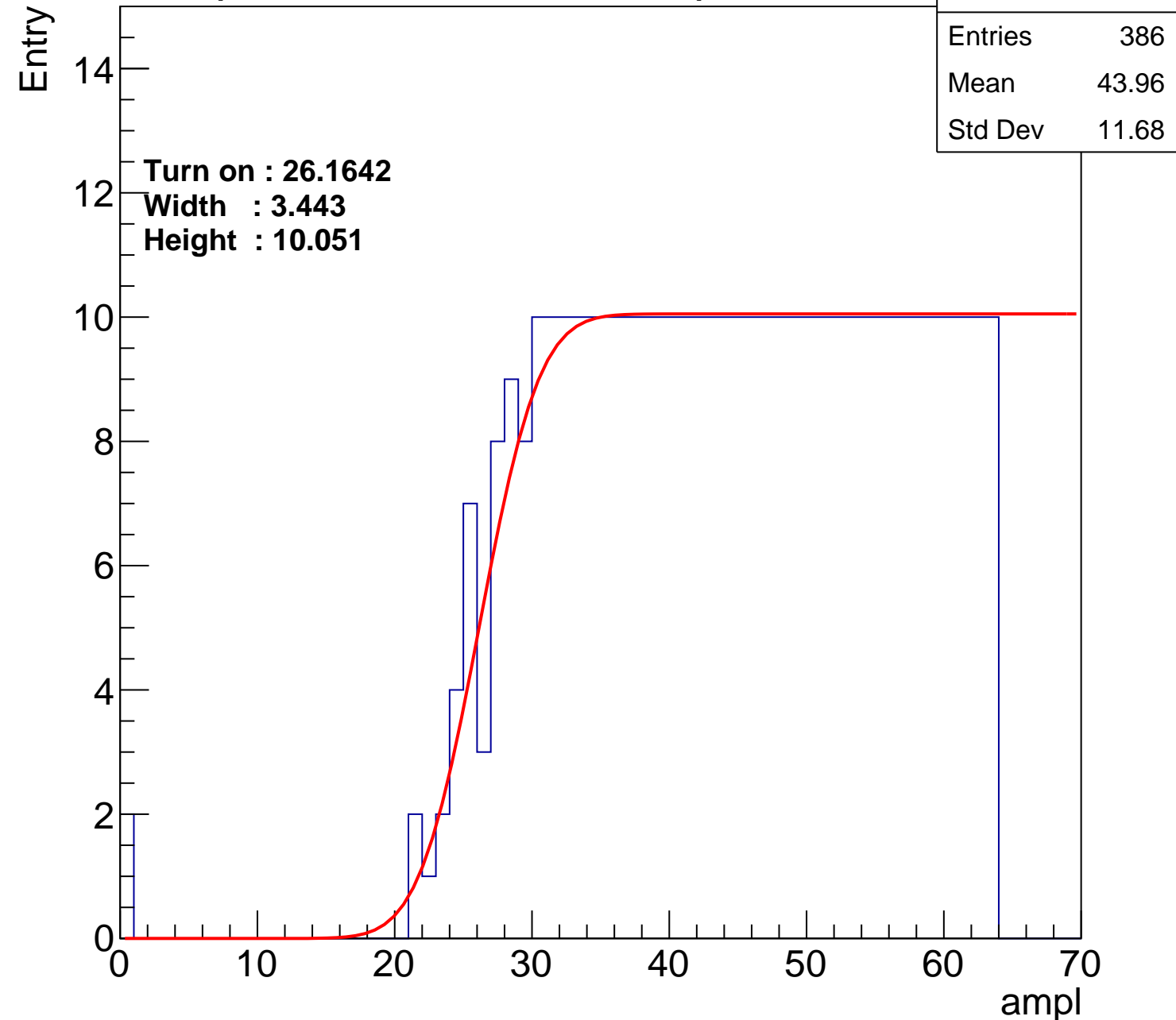
Width : 3.443

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch58

calib_packv5_042523_0143.root, FC#0, port D2

Entries	394
Mean	43.34
Std Dev	12.43

Turn on : 25.4398

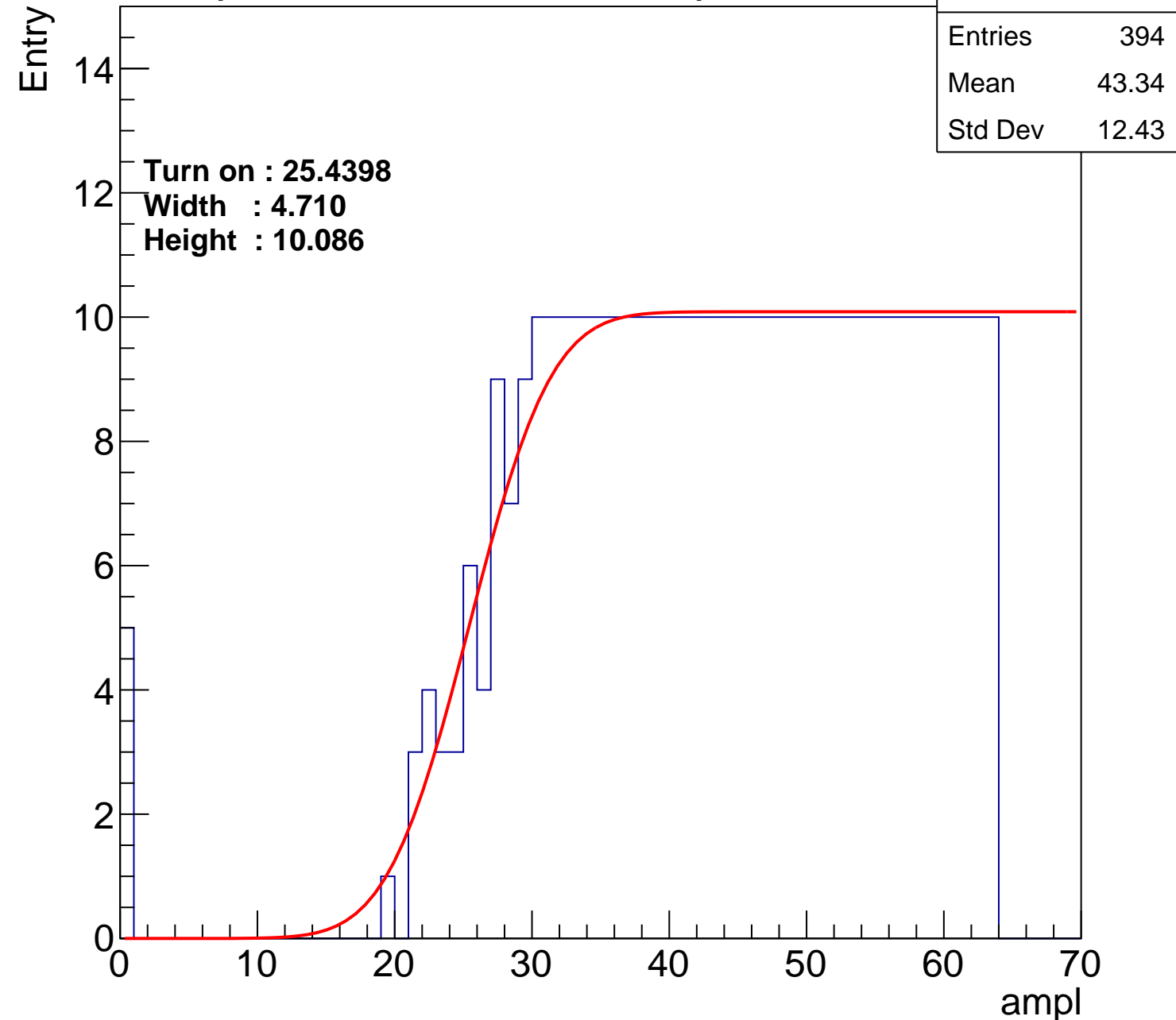
Width : 4.710

Height : 10.086

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch59

calib_packv5_042523_0143.root, FC#0, port D2

Entries	369
Mean	44.84
Std Dev	11.17

Turn on : 27.3680

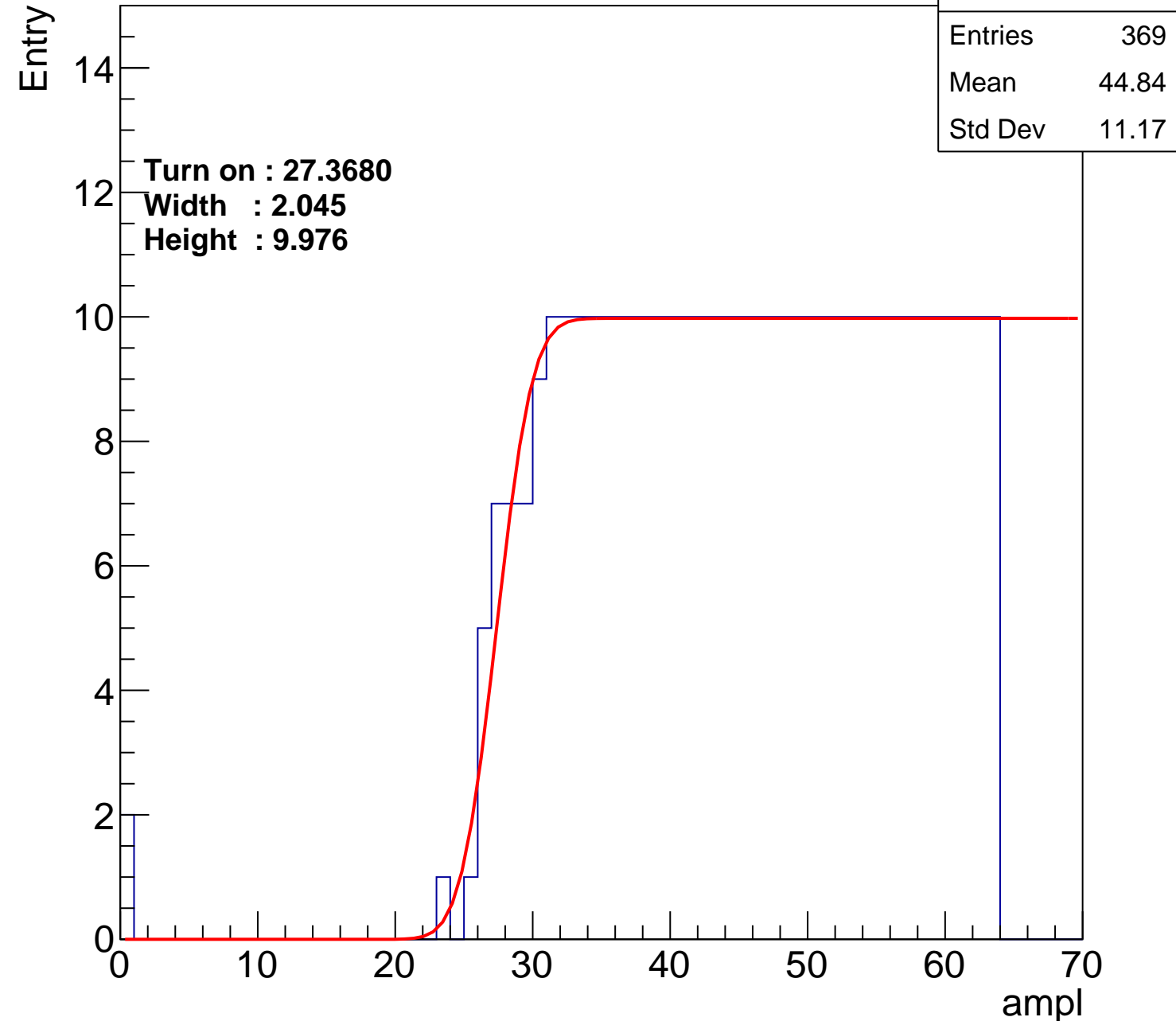
Width : 2.045

Height : 9.976

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch60

calib_packv5_042523_0143.root, FC#0, port D2

Entries	368
Mean	44.76
Std Dev	11.43

Turn on : 27.6631

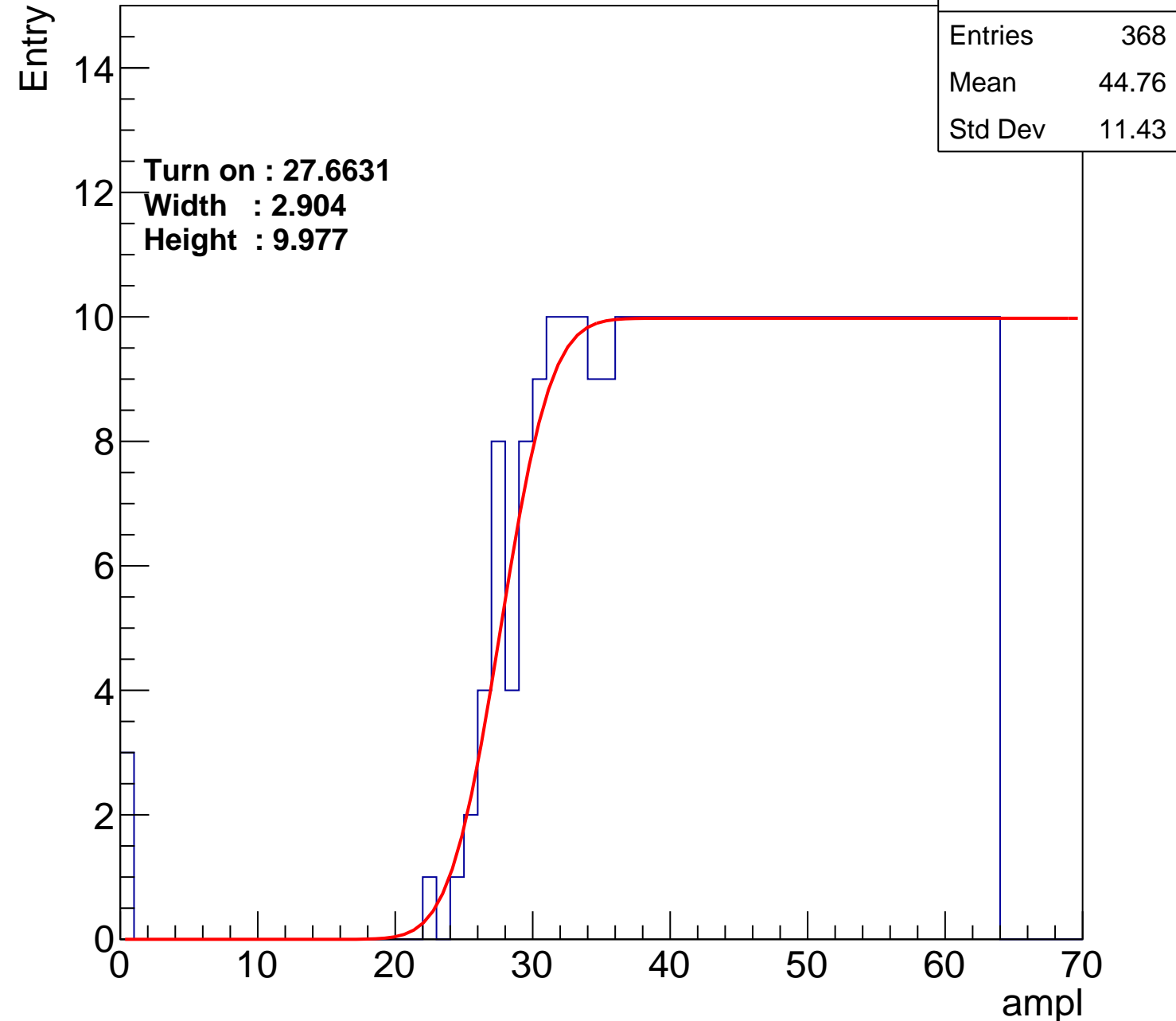
Width : 2.904

Height : 9.977

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch61

calib_packv5_042523_0143.root, FC#0, port D2

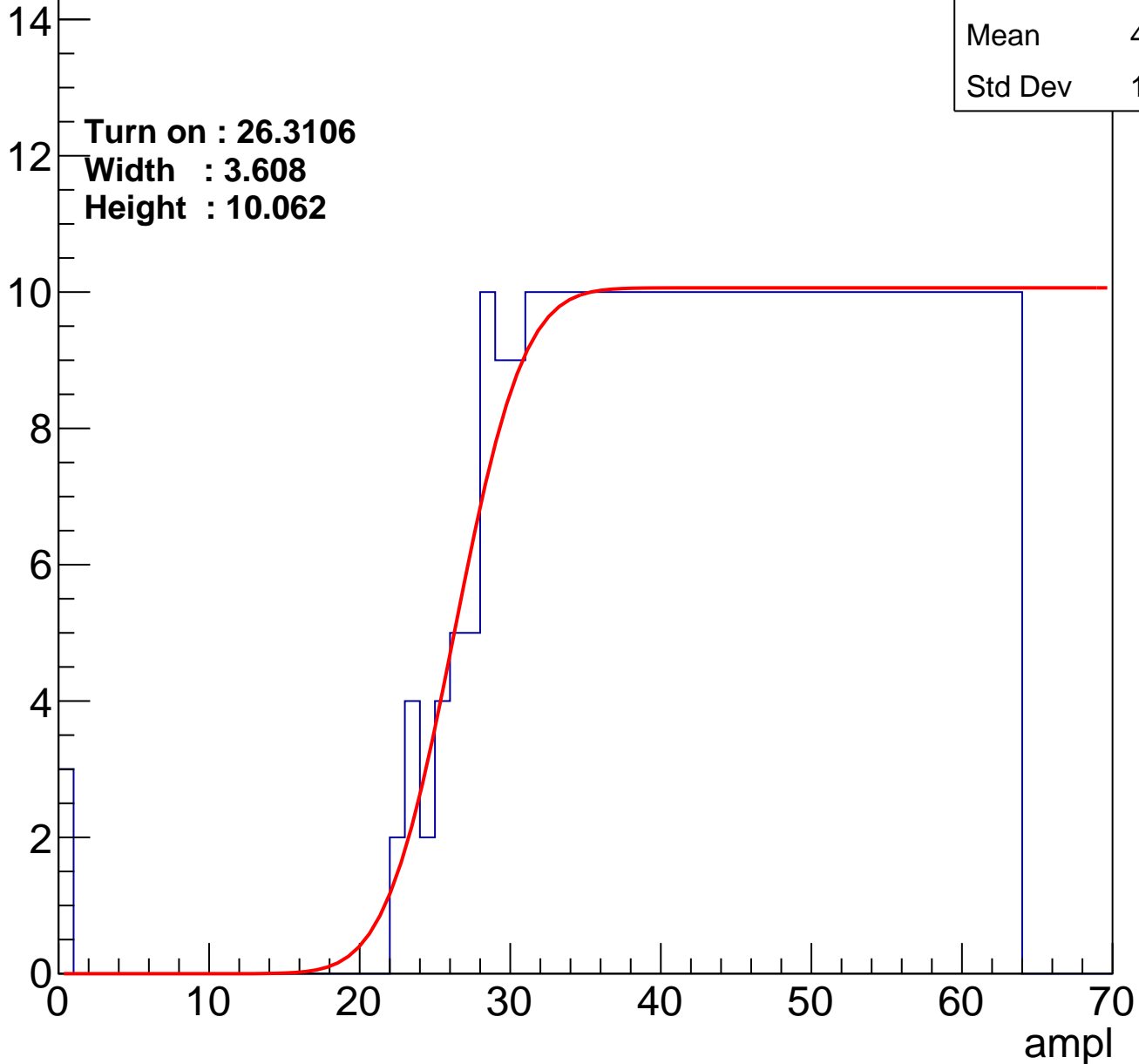
Entries	383
Mean	44.05
Std Dev	11.77

Turn on : 26.3106

Width : 3.608

Height : 10.062

Entry



B1L101S, U20-ch62

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.25
Std Dev	11.84

Turn on : 27.1946

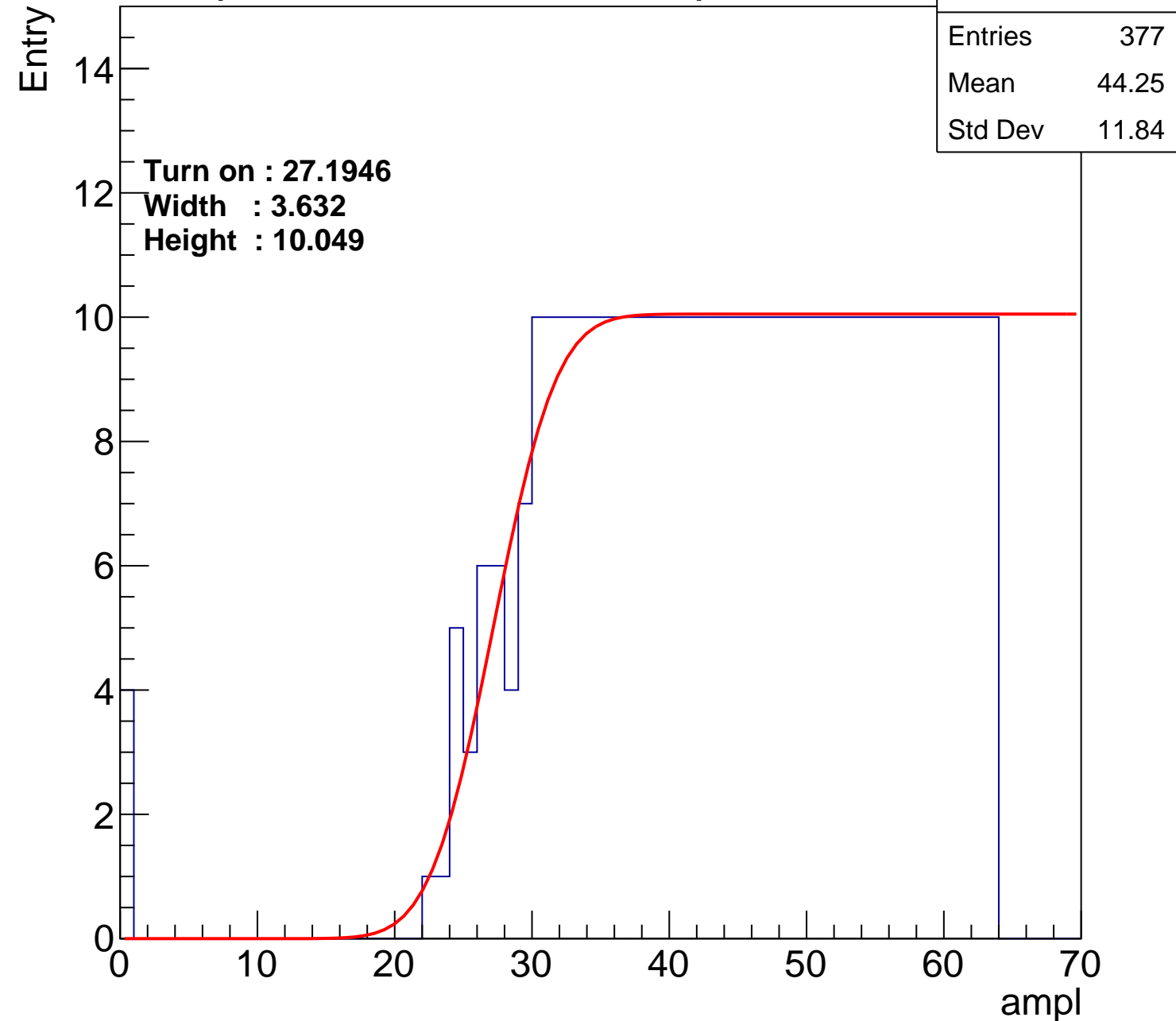
Width : 3.632

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch63

calib_packv5_042523_0143.root, FC#0, port D2

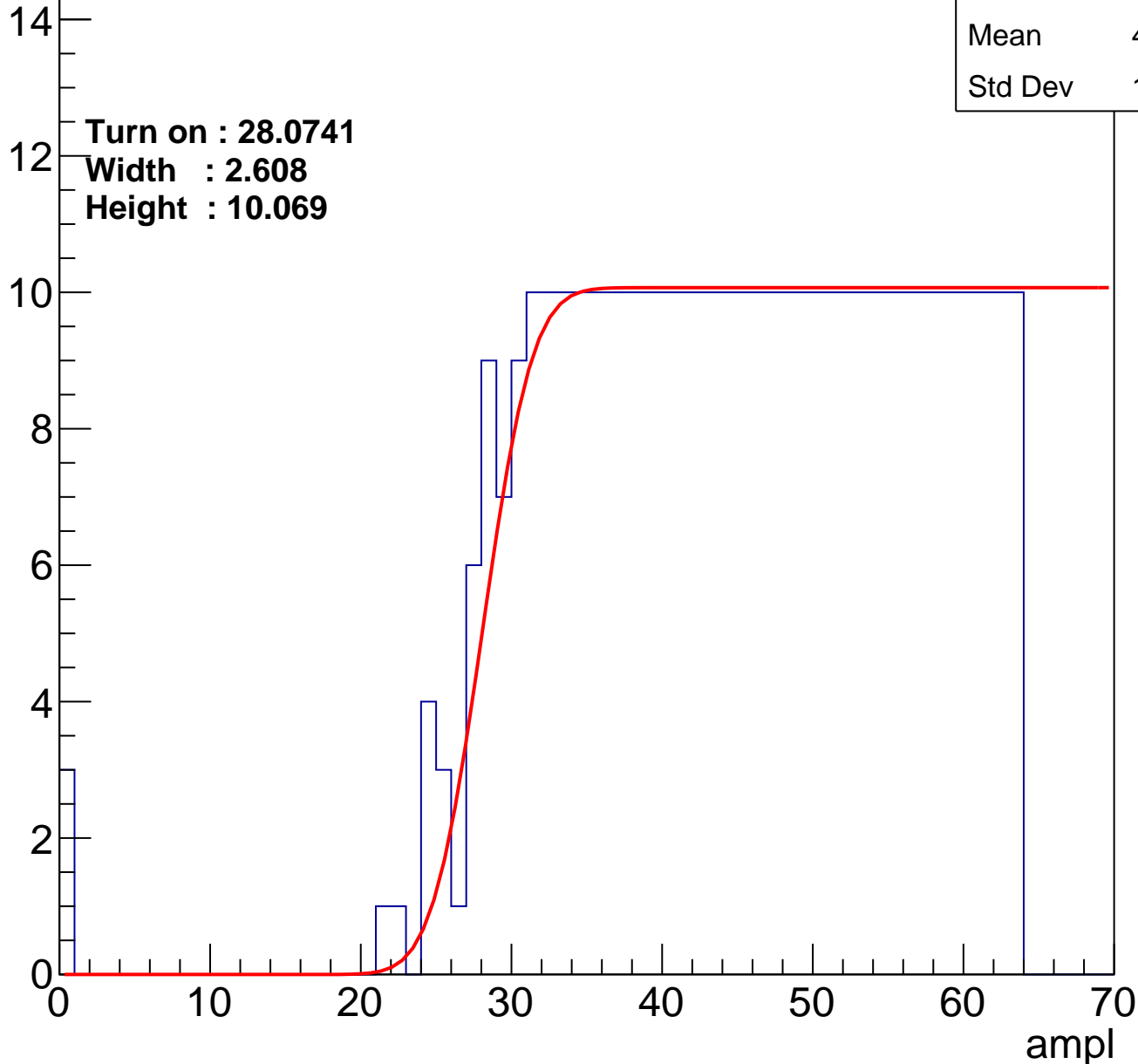
Entries	374
Mean	44.48
Std Dev	11.56

Turn on : 28.0741

Width : 2.608

Height : 10.069

Entry



B1L101S, U20-ch64

calib_packv5_042523_0143.root, FC#0, port D2

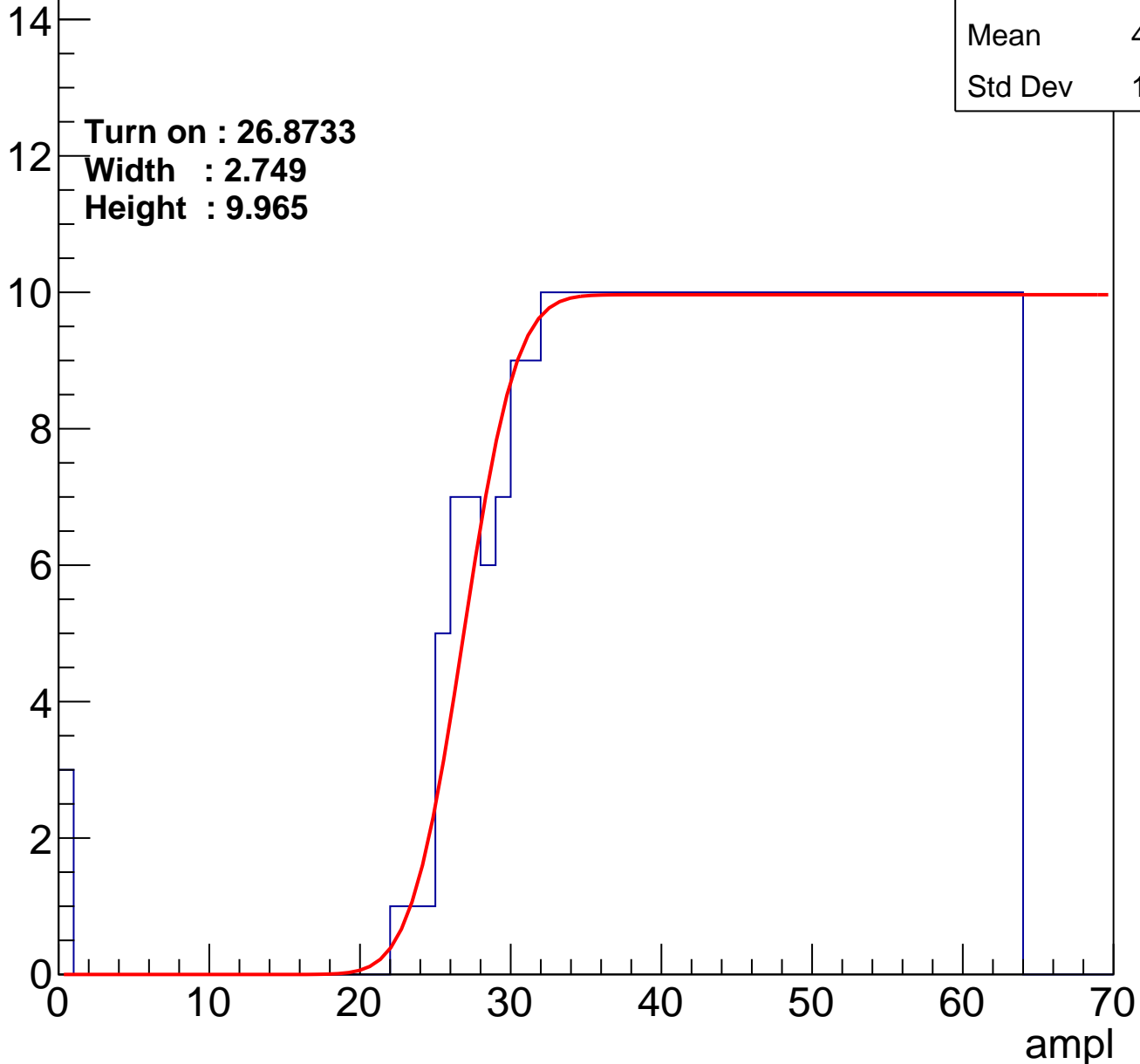
Entries	376
Mean	44.38
Std Dev	11.62

Turn on : 26.8733

Width : 2.749

Height : 9.965

Entry



B1L101S, U20-ch65

calib_packv5_042523_0143.root, FC#0, port D2

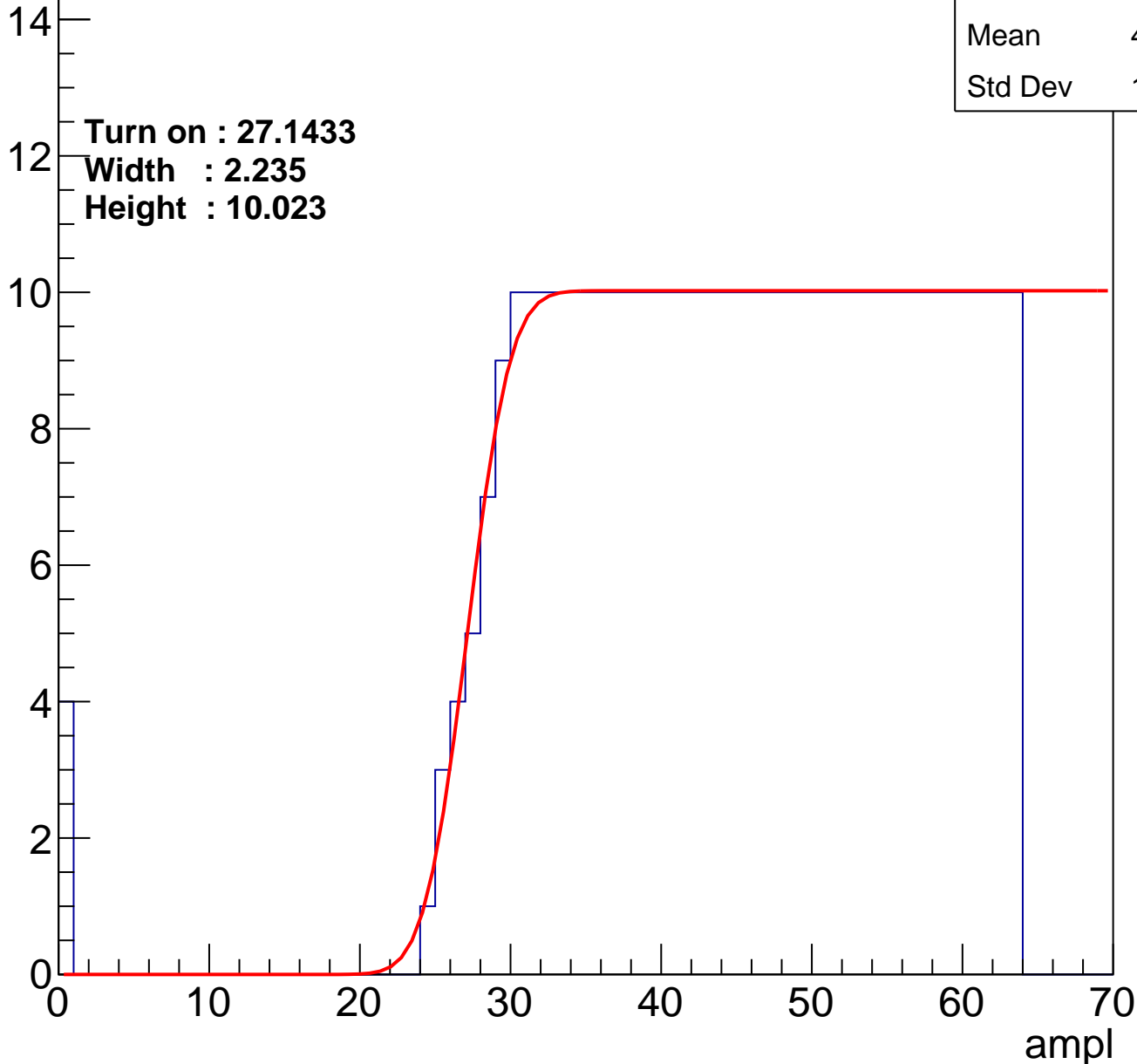
Entries	373
Mean	44.52
Std Dev	11.64

Turn on : 27.1433

Width : 2.235

Height : 10.023

Entry



B1L101S, U20-ch66

calib_packv5_042523_0143.root, FC#0, port D2

Entries	379
Mean	44.31
Std Dev	11.5

Turn on : 26.7373

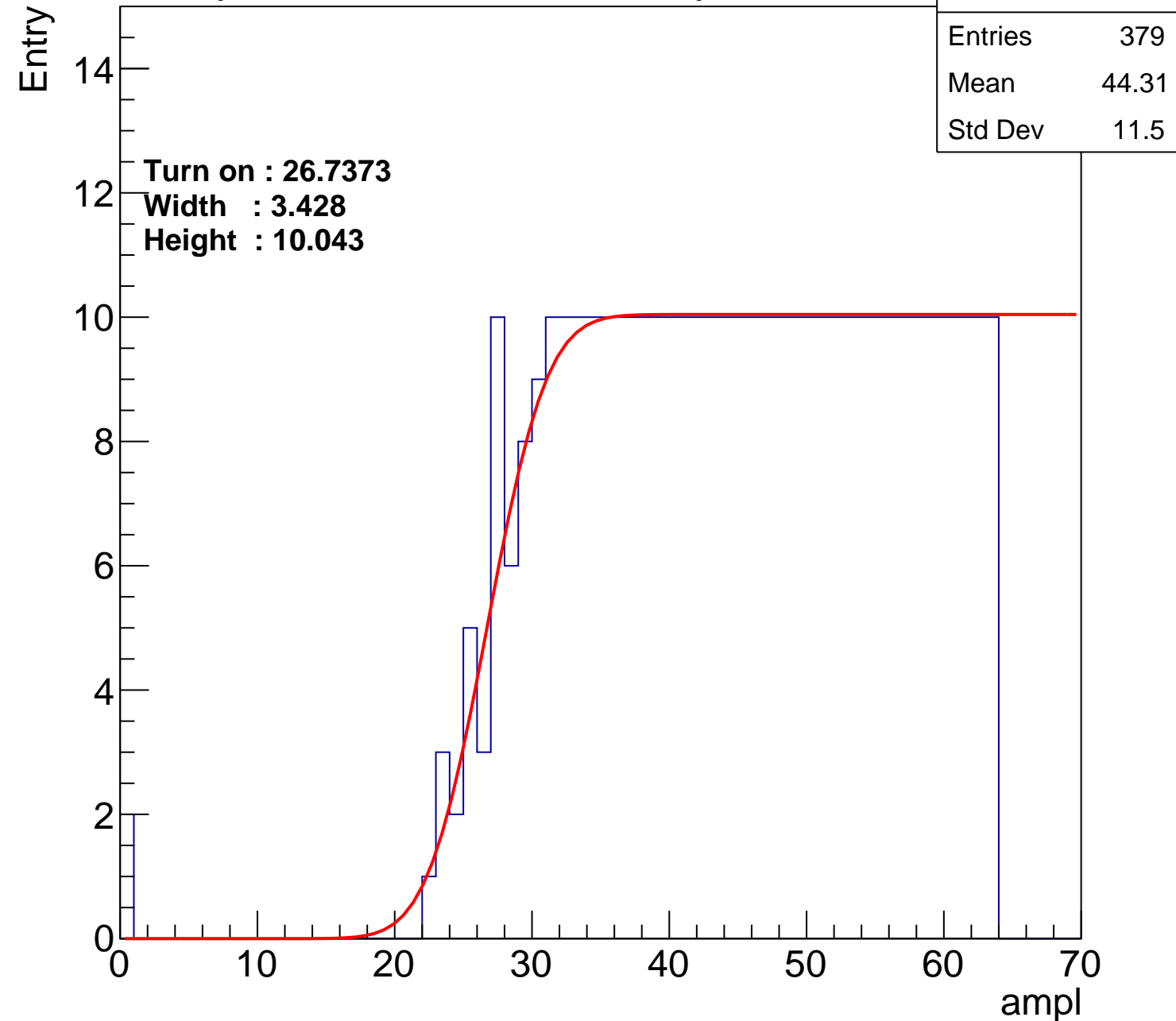
Width : 3.428

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch67

calib_packv5_042523_0143.root, FC#0, port D2

Entries	371
Mean	44.64
Std Dev	11.47

Turn on : 27.2388

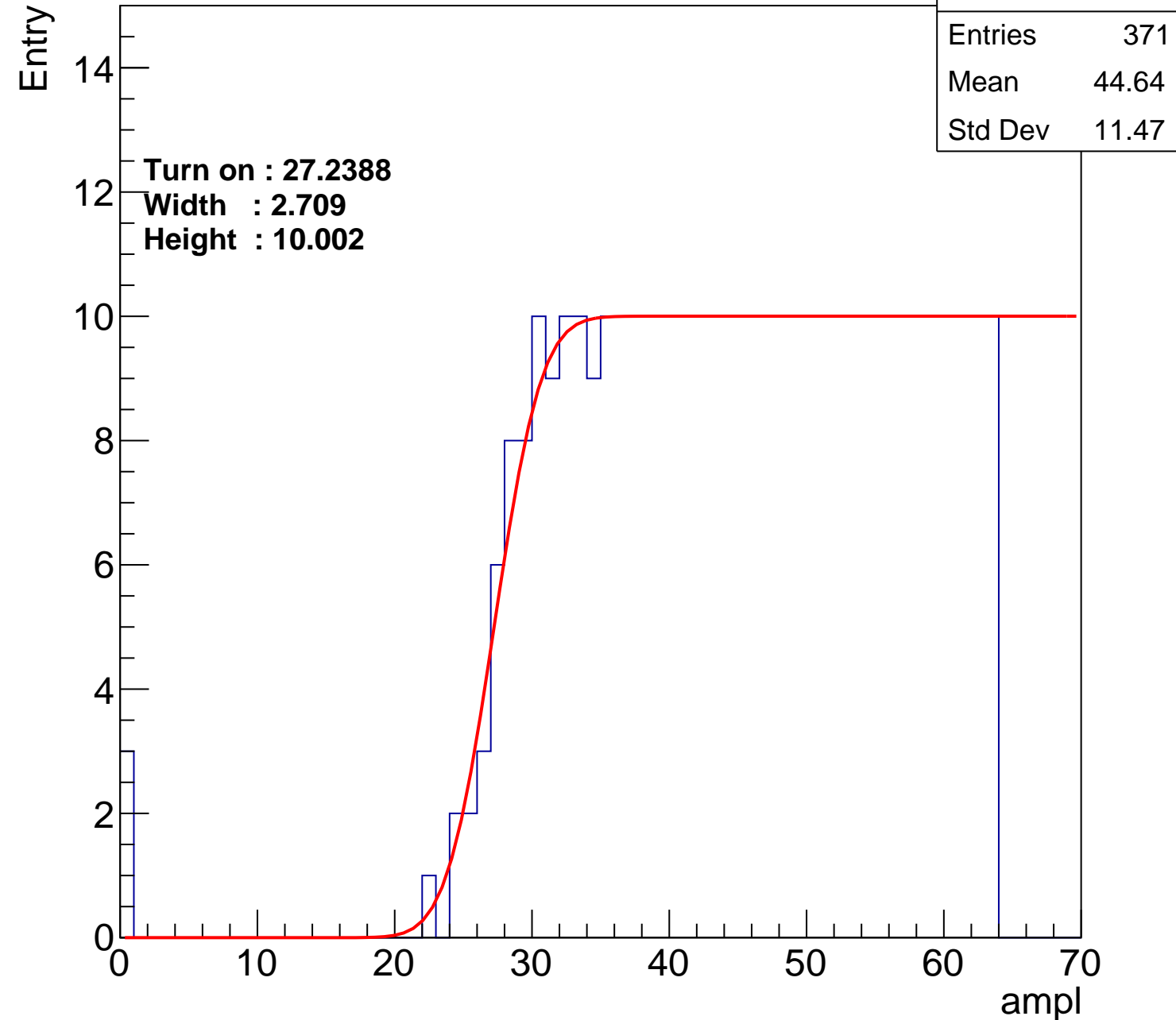
Width : 2.709

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch68

calib_packv5_042523_0143.root, FC#0, port D2

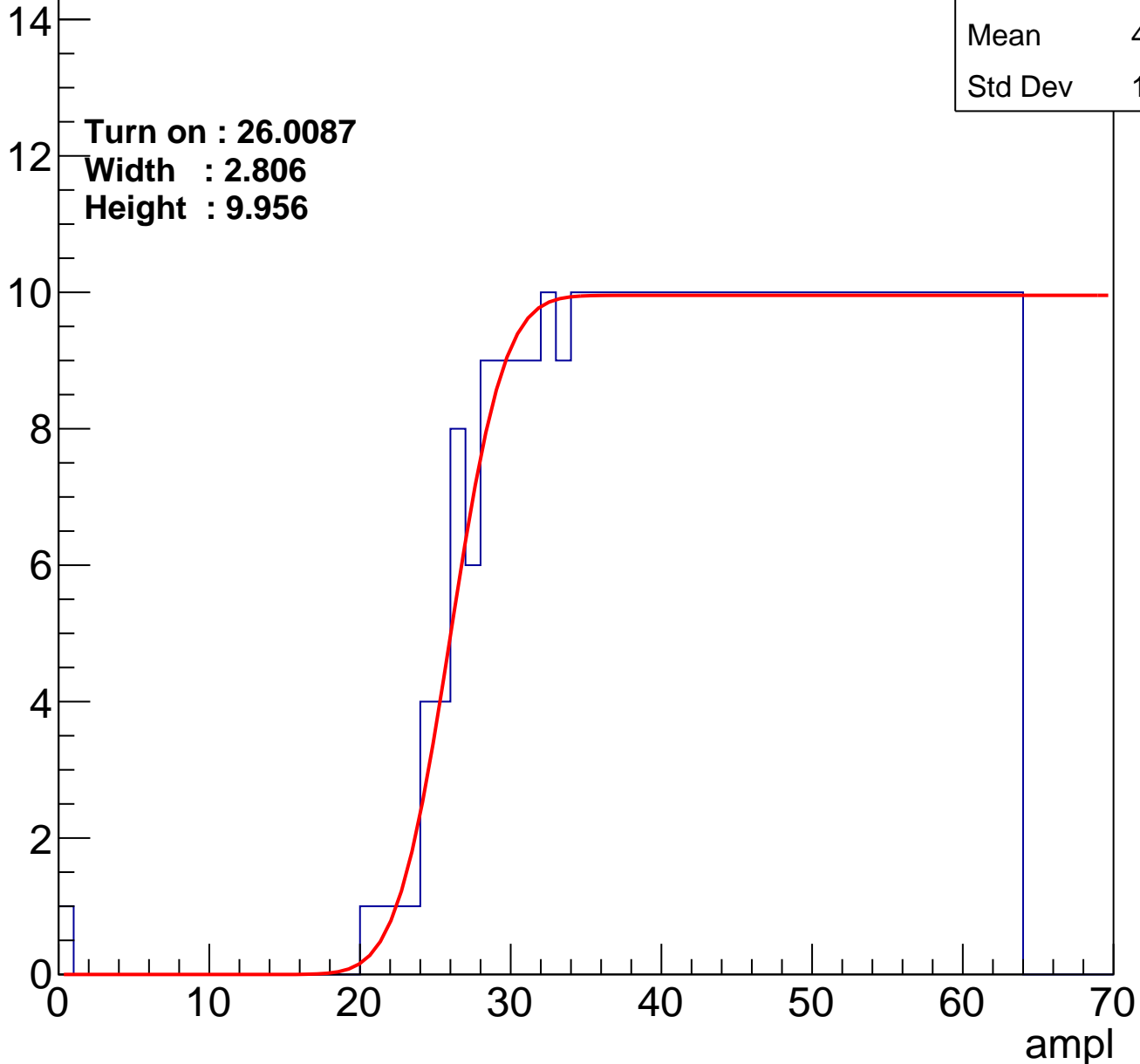
Entries	382
Mean	44.19
Std Dev	11.44

Turn on : 26.0087

Width : 2.806

Height : 9.956

Entry



B1L101S, U20-ch69

calib_packv5_042523_0143.root, FC#0, port D2

Entries	379
Mean	44.17
Std Dev	11.8

Turn on : 27.1933

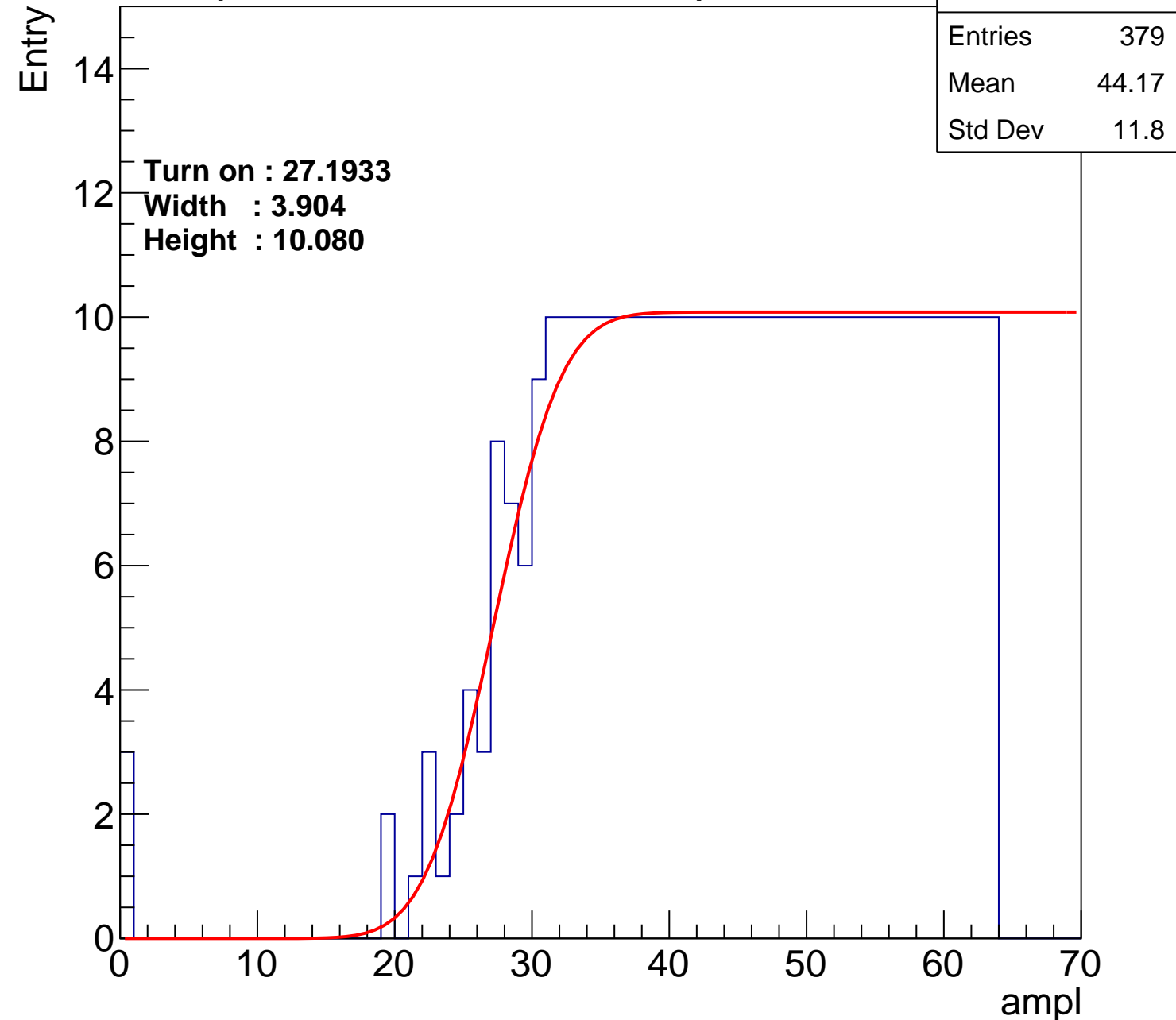
Width : 3.904

Height : 10.080

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch70

calib_packv5_042523_0143.root, FC#0, port D2

Entries	384
Mean	44.07
Std Dev	11.63

Turn on : 27.1160

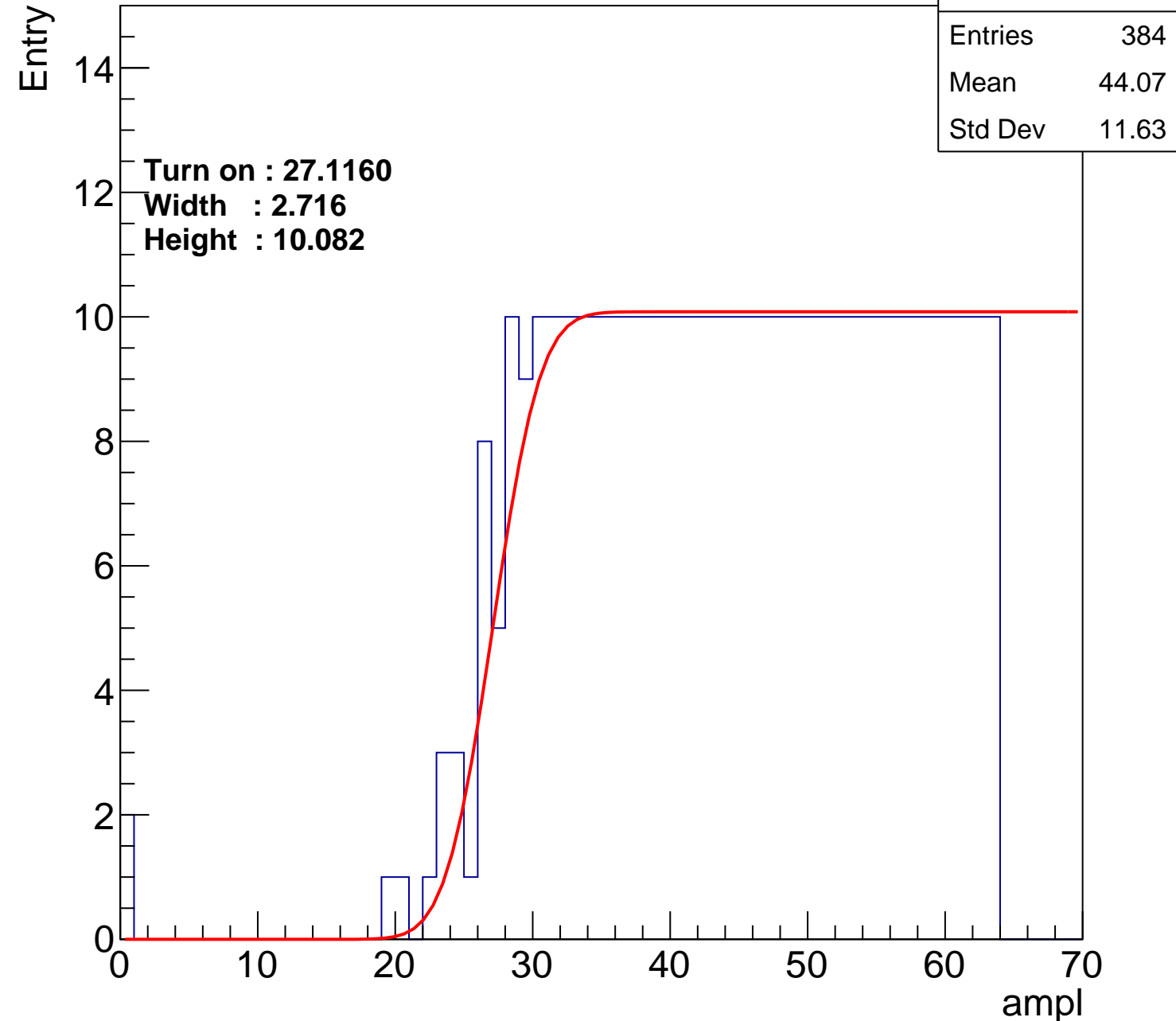
Width : 2.716

Height : 10.082

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch71

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.2
Std Dev	11.99

Turn on : 26.9787

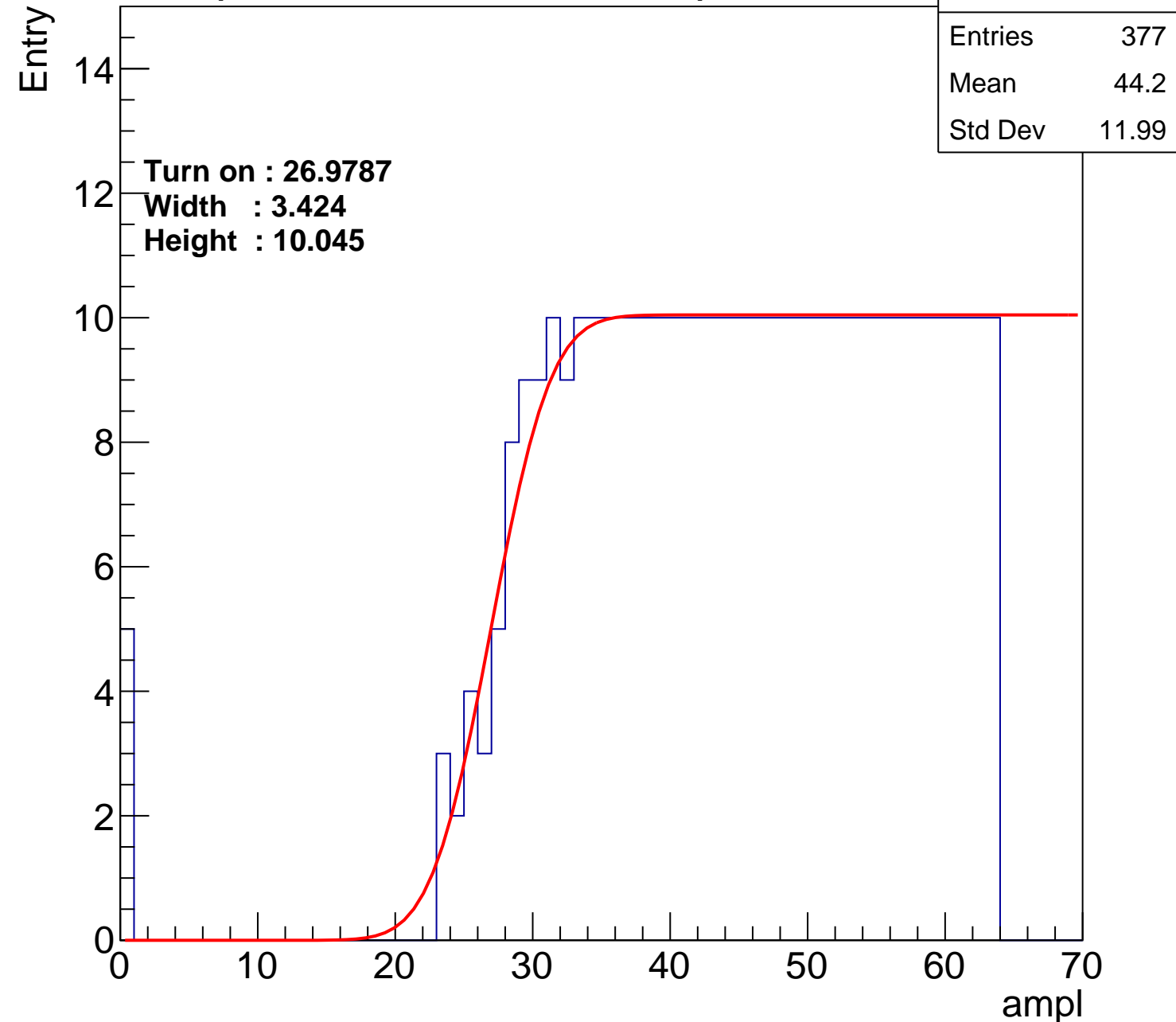
Width : 3.424

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch72

calib_packv5_042523_0143.root, FC#0, port D2

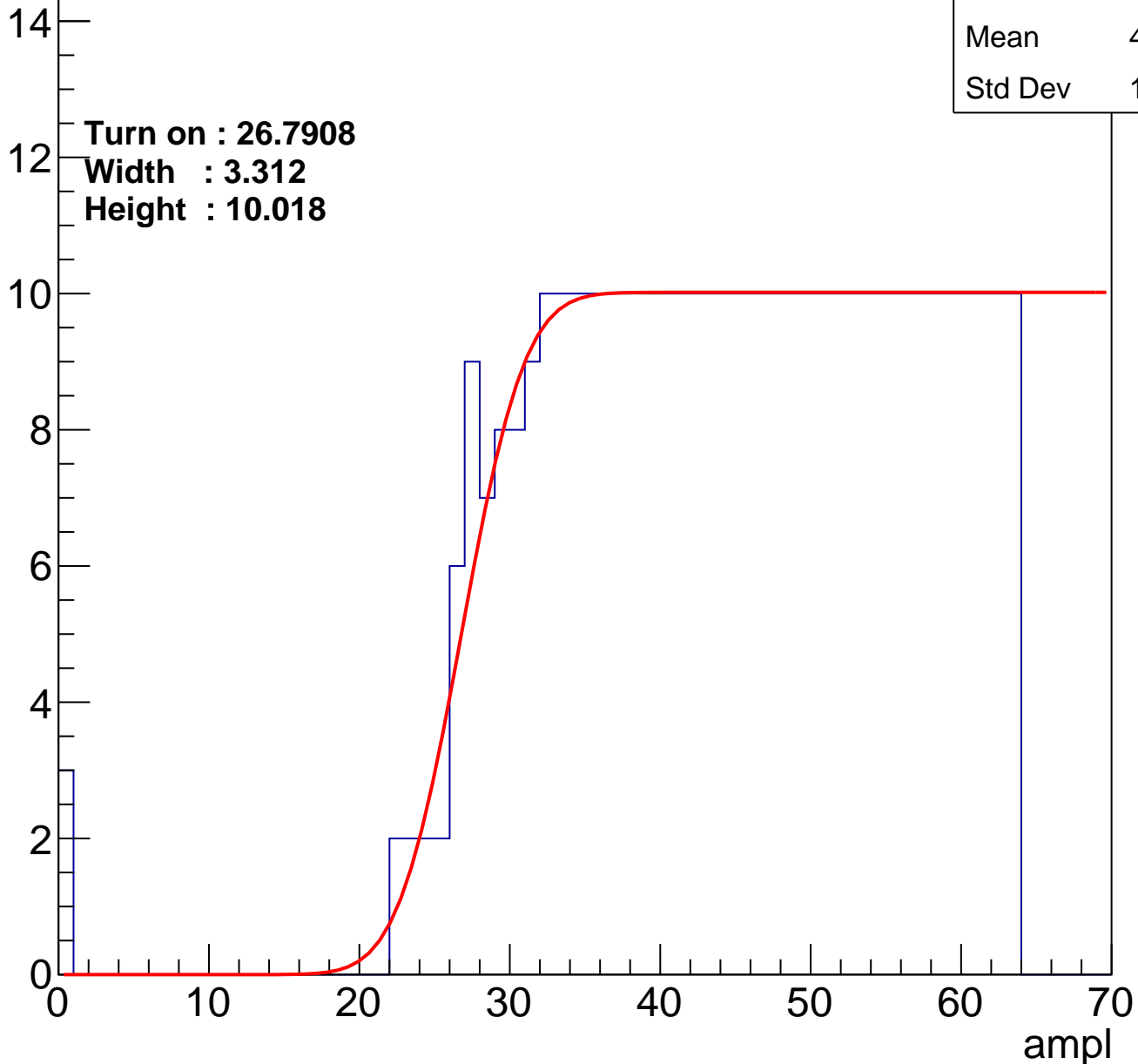
Entries	378
Mean	44.27
Std Dev	11.68

Turn on : 26.7908

Width : 3.312

Height : 10.018

Entry



B1L101S, U20-ch73

calib_packv5_042523_0143.root, FC#0, port D2

Entries	364
Mean	44.77
Std Dev	11.89

Turn on : 28.3815

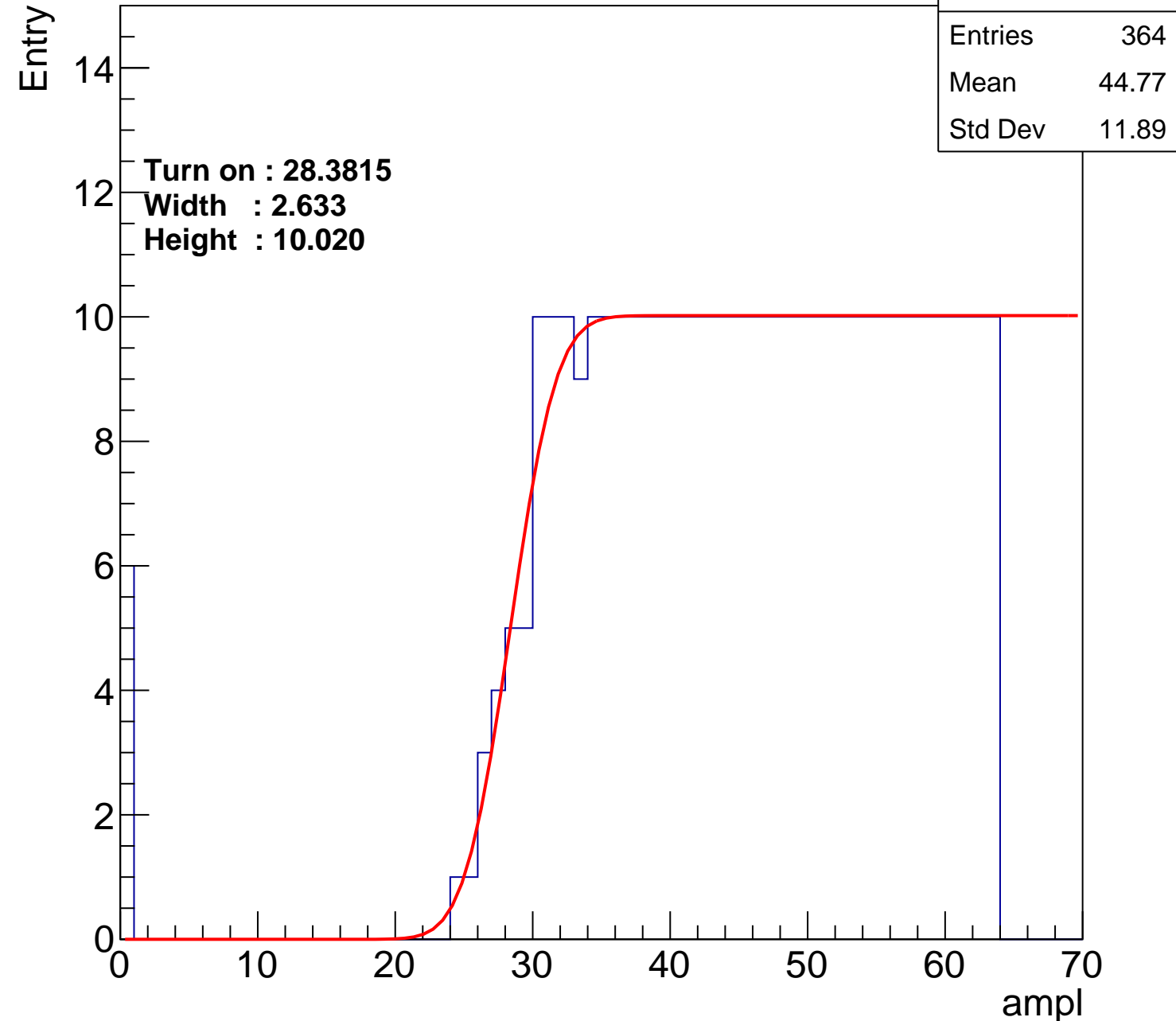
Width : 2.633

Height : 10.020

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch74

calib_packv5_042523_0143.root, FC#0, port D2

Entries	382
Mean	44.17
Std Dev	11.56

Turn on : 26.3153

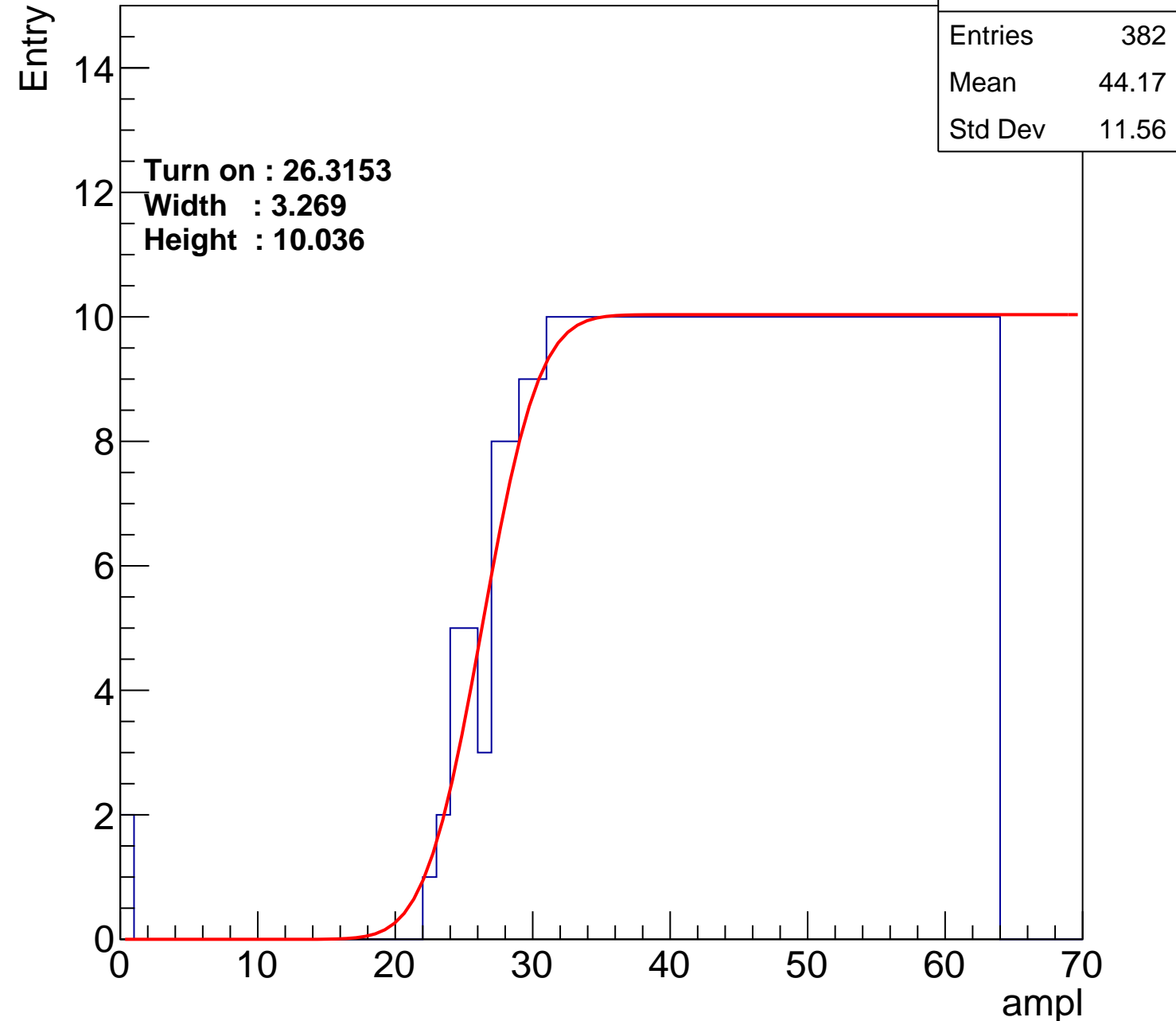
Width : 3.269

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



calib_packv5_042523_0143.root, FC#0, port D2

calib_packv5_042523_0143.root, FC#0, port D2

Turn on : 28.4737
Width : 3.804
Height : 10.029



B1L101S, U20-ch76

calib_packv5_042523_0143.root, FC#0, port D2

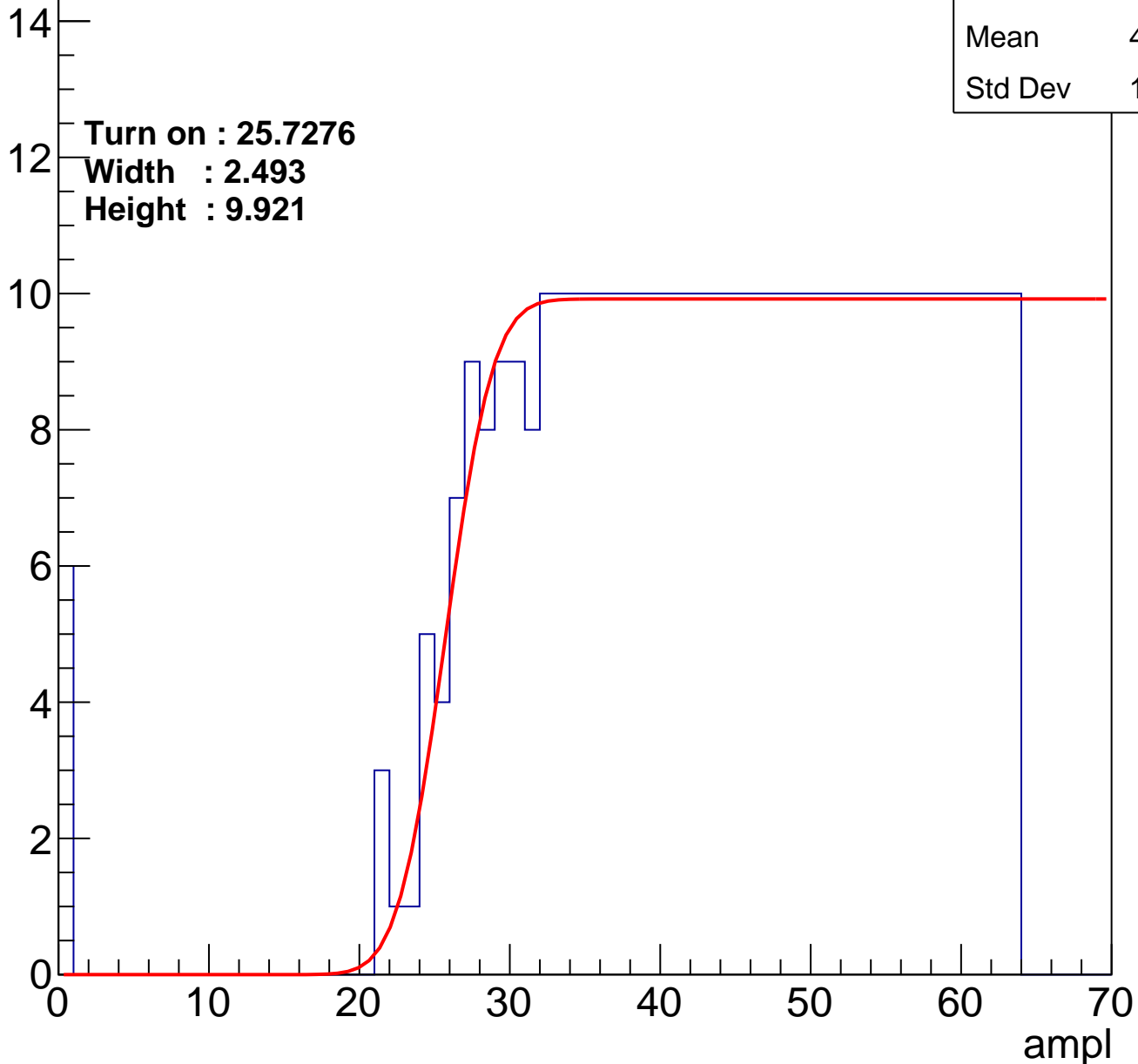
Entries	390
Mean	43.48
Std Dev	12.48

Turn on : 25.7276

Width : 2.493

Height : 9.921

Entry



B1L101S, U20-ch77

calib_packv5_042523_0143.root, FC#0, port D2

Entries	373
Mean	44.6
Std Dev	11.34

Turn on : 26.6060

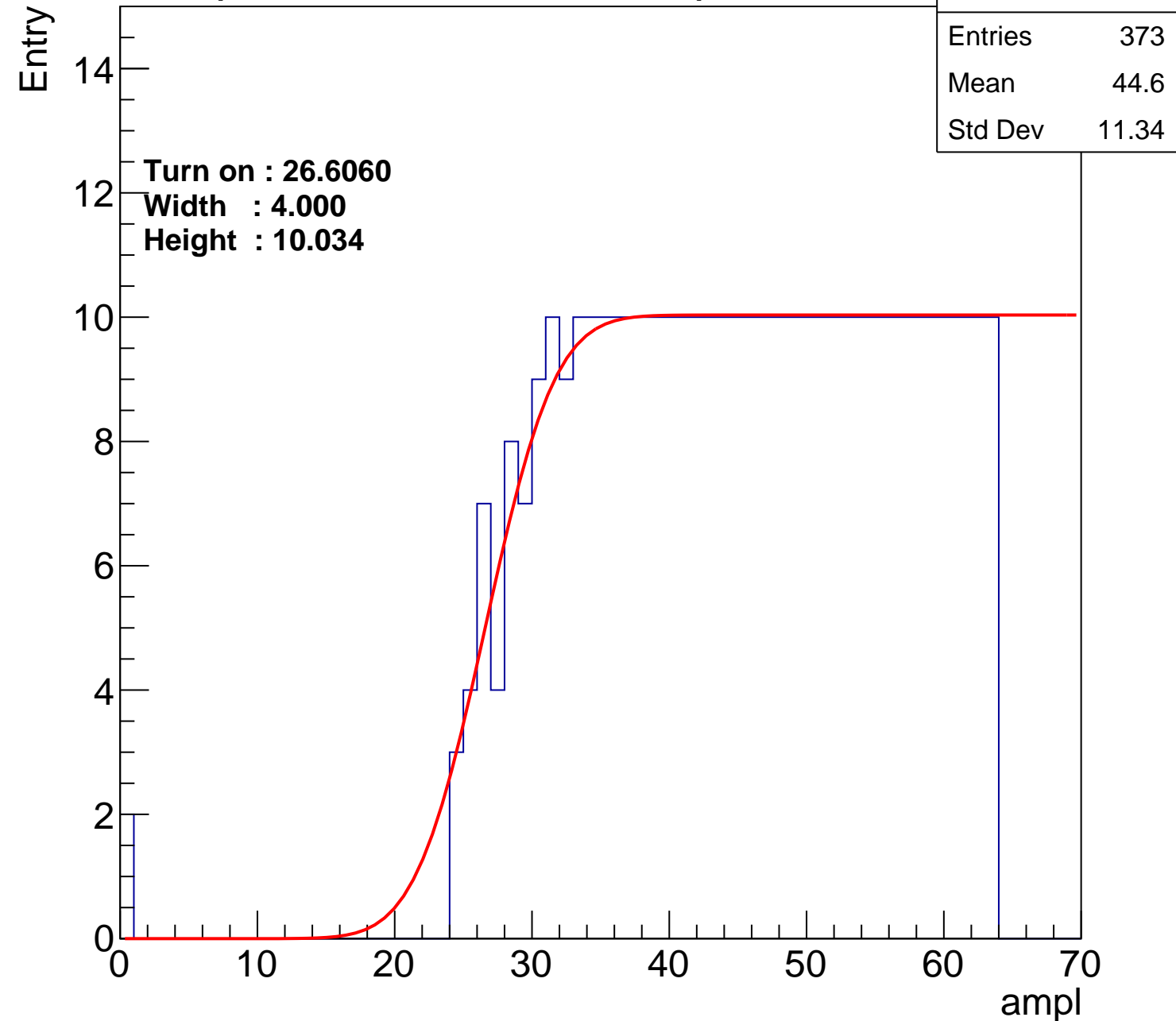
Width : 4.000

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch78

calib_packv5_042523_0143.root, FC#0, port D2

Entries	384
Mean	43.74
Std Dev	12.47

Turn on : 26.7197

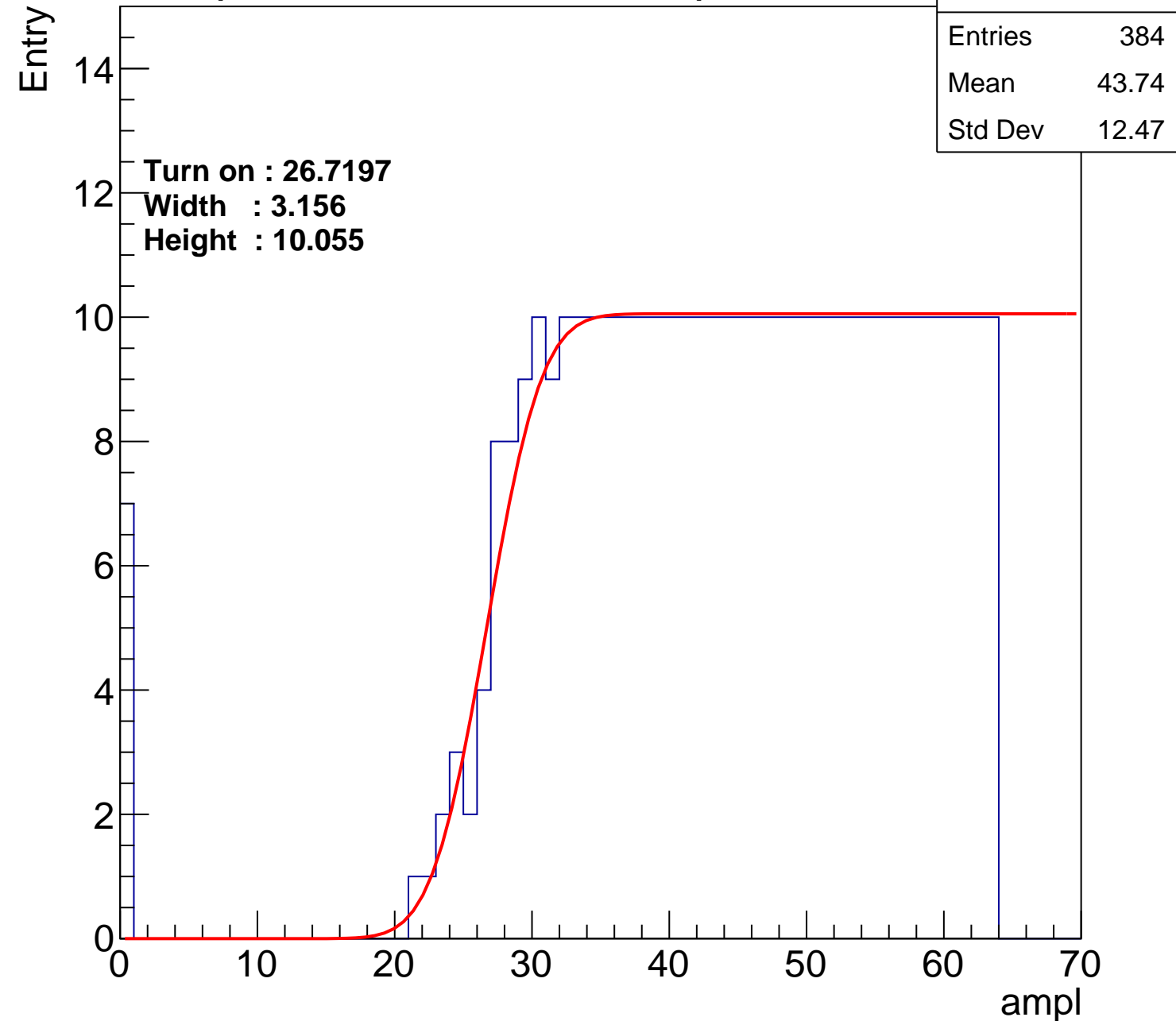
Width : 3.156

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch79

calib_packv5_042523_0143.root, FC#0, port D2

Entries	371
Mean	44.66
Std Dev	11.45

Turn on : 27.4384

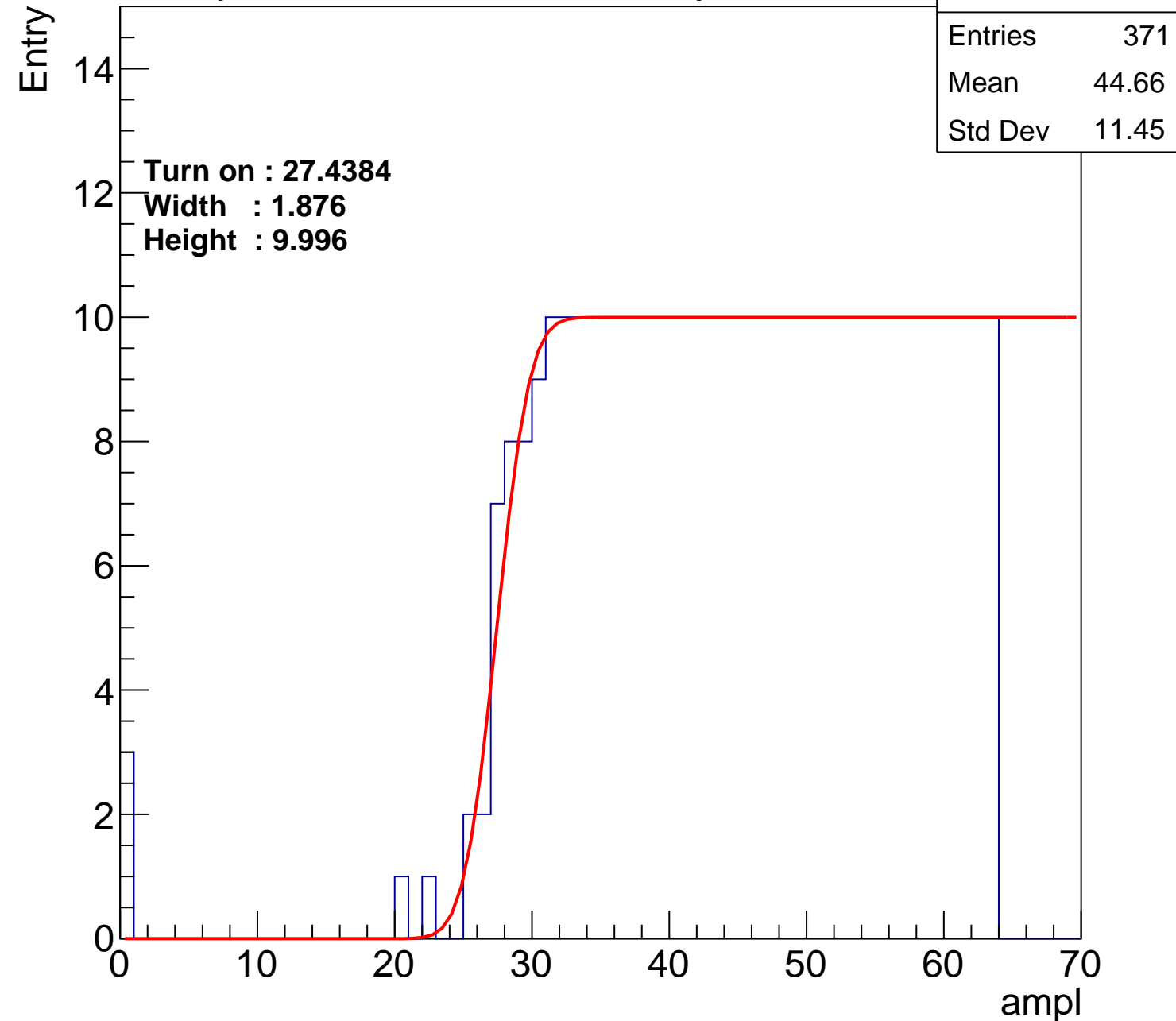
Width : 1.876

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch80

calib_packv5_042523_0143.root, FC#0, port D2

Entries	397
Mean	43.35
Std Dev	12.13

Turn on : 24.4391

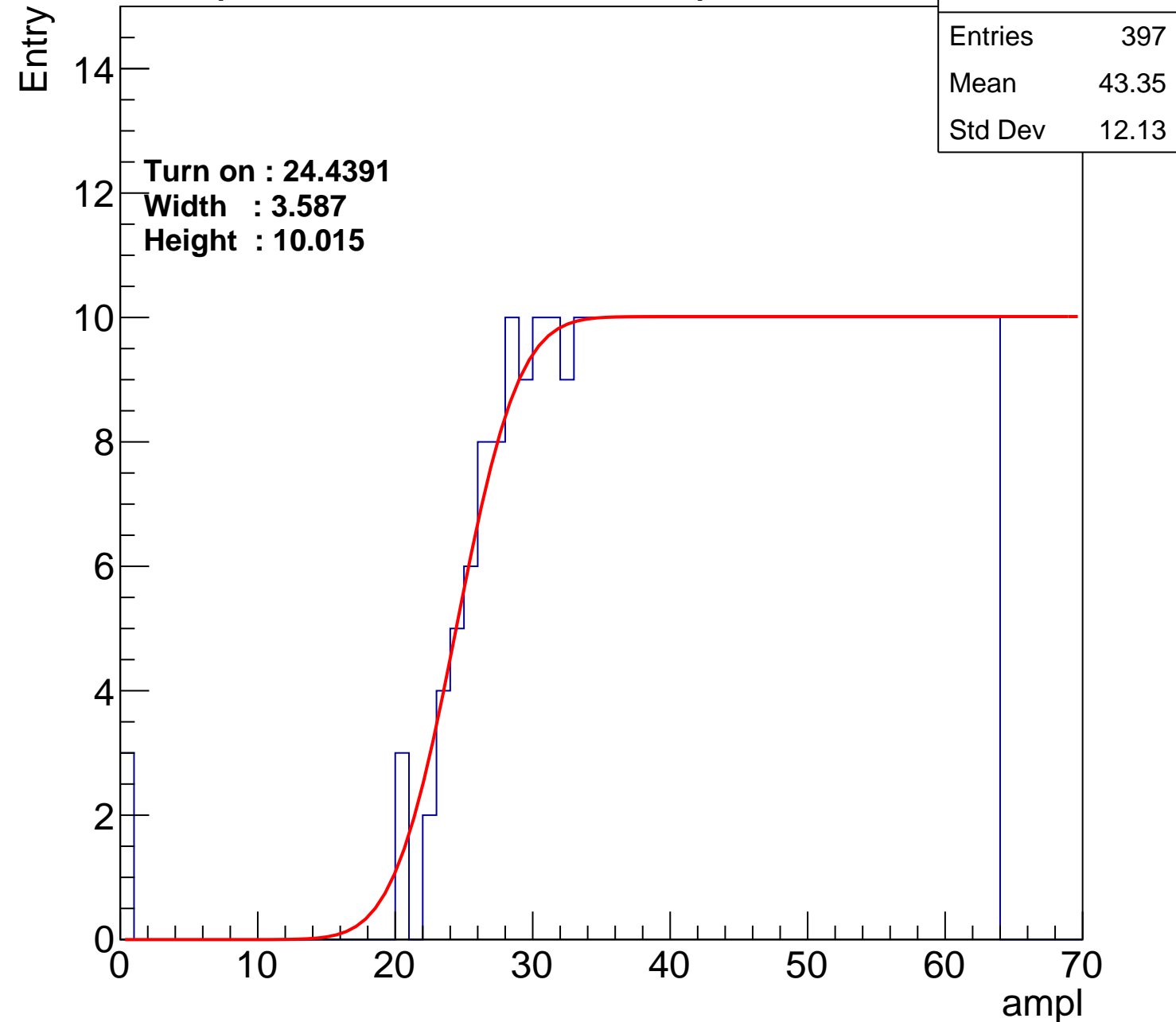
Width : 3.587

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch81

calib_packv5_042523_0143.root, FC#0, port D2

Entries	384
Mean	44.12
Std Dev	11.45

Turn on : 25.6914

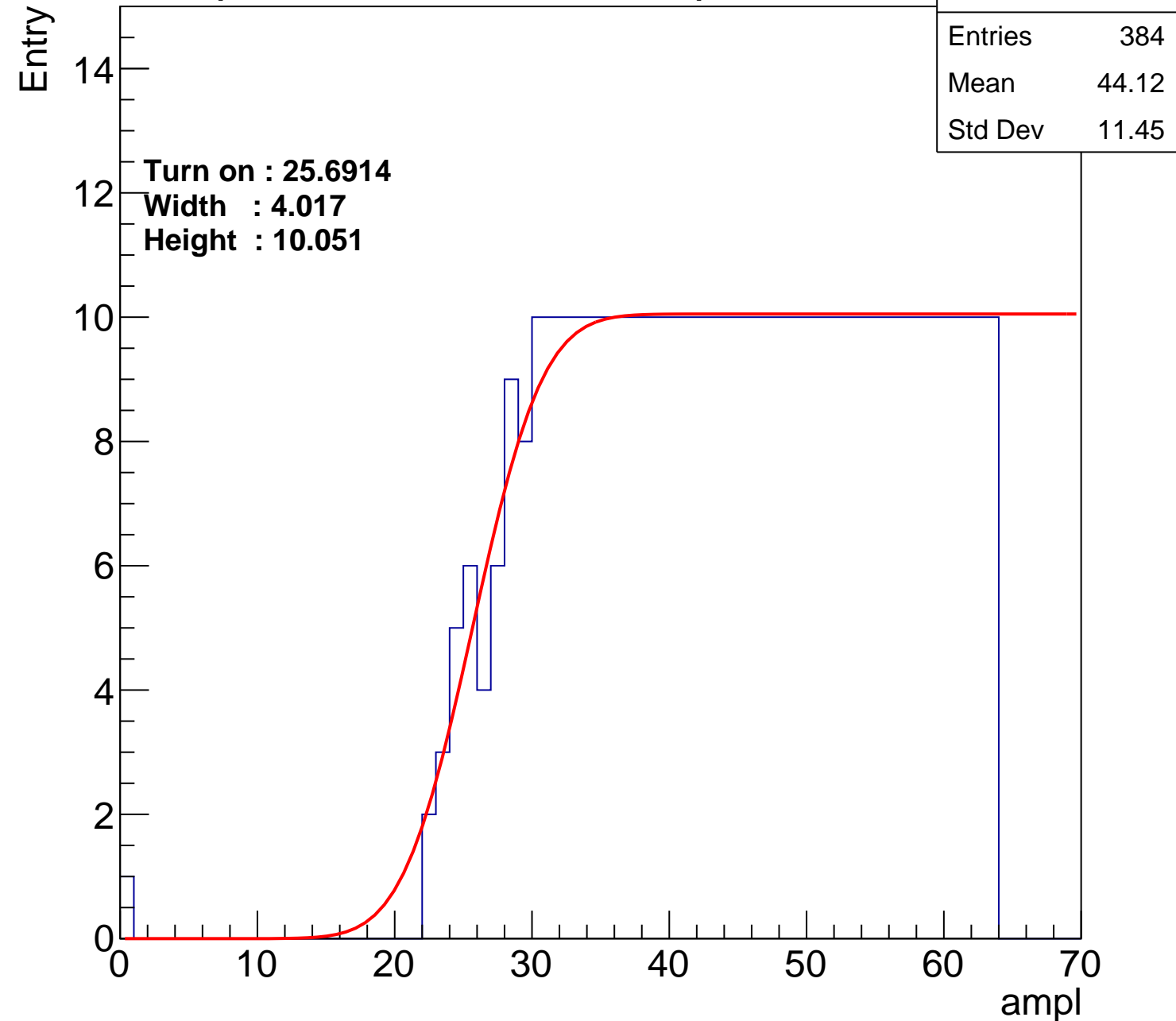
Width : 4.017

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch82

calib_packv5_042523_0143.root, FC#0, port D2

Entries	410
Mean	42.66
Std Dev	12.59

Turn on : 23.9722

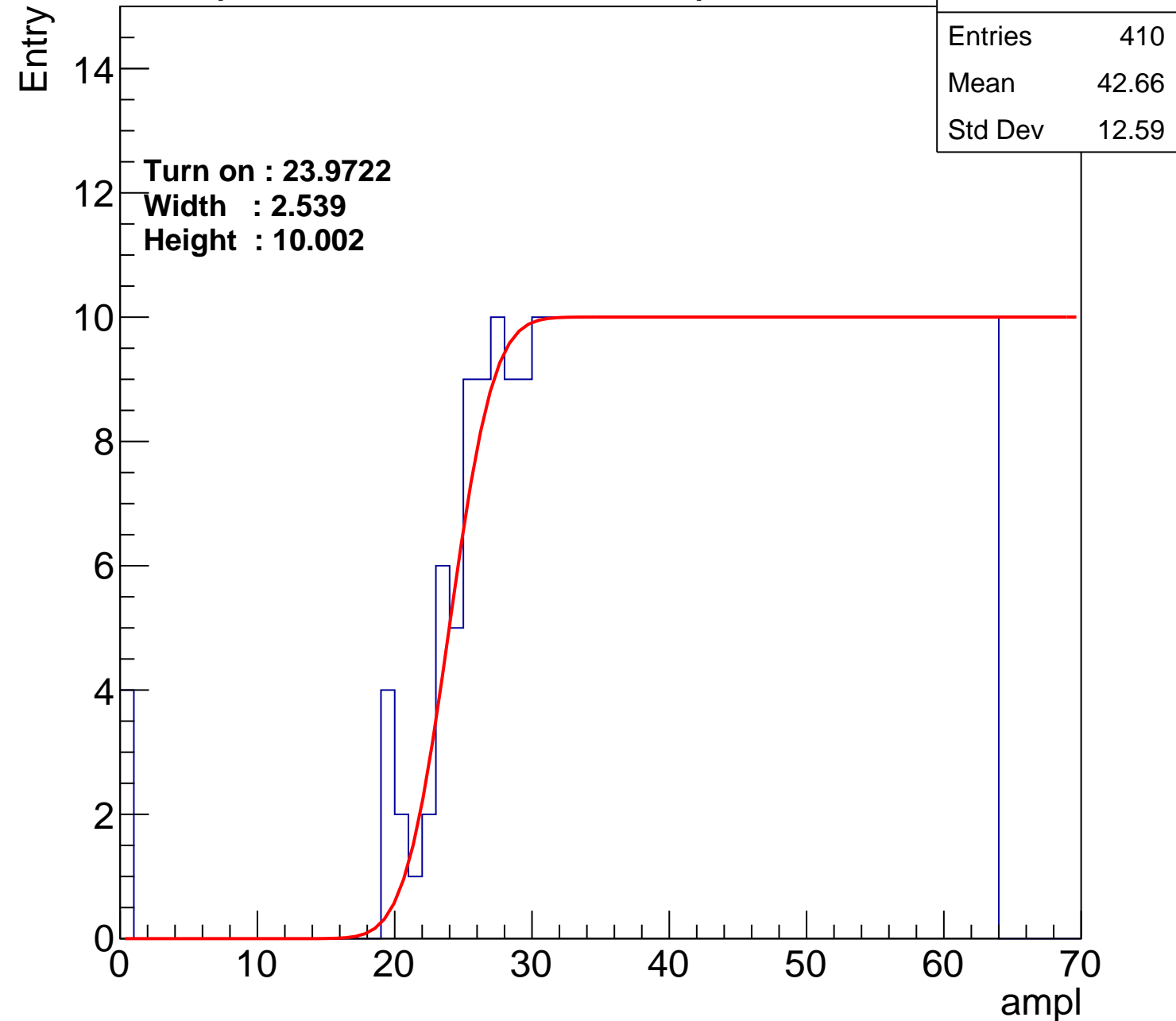
Width : 2.539

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch83

calib_packv5_042523_0143.root, FC#0, port D2

Entries	368
Mean	44.48
Std Dev	12.19

Turn on : 28.3337

Width : 3.546

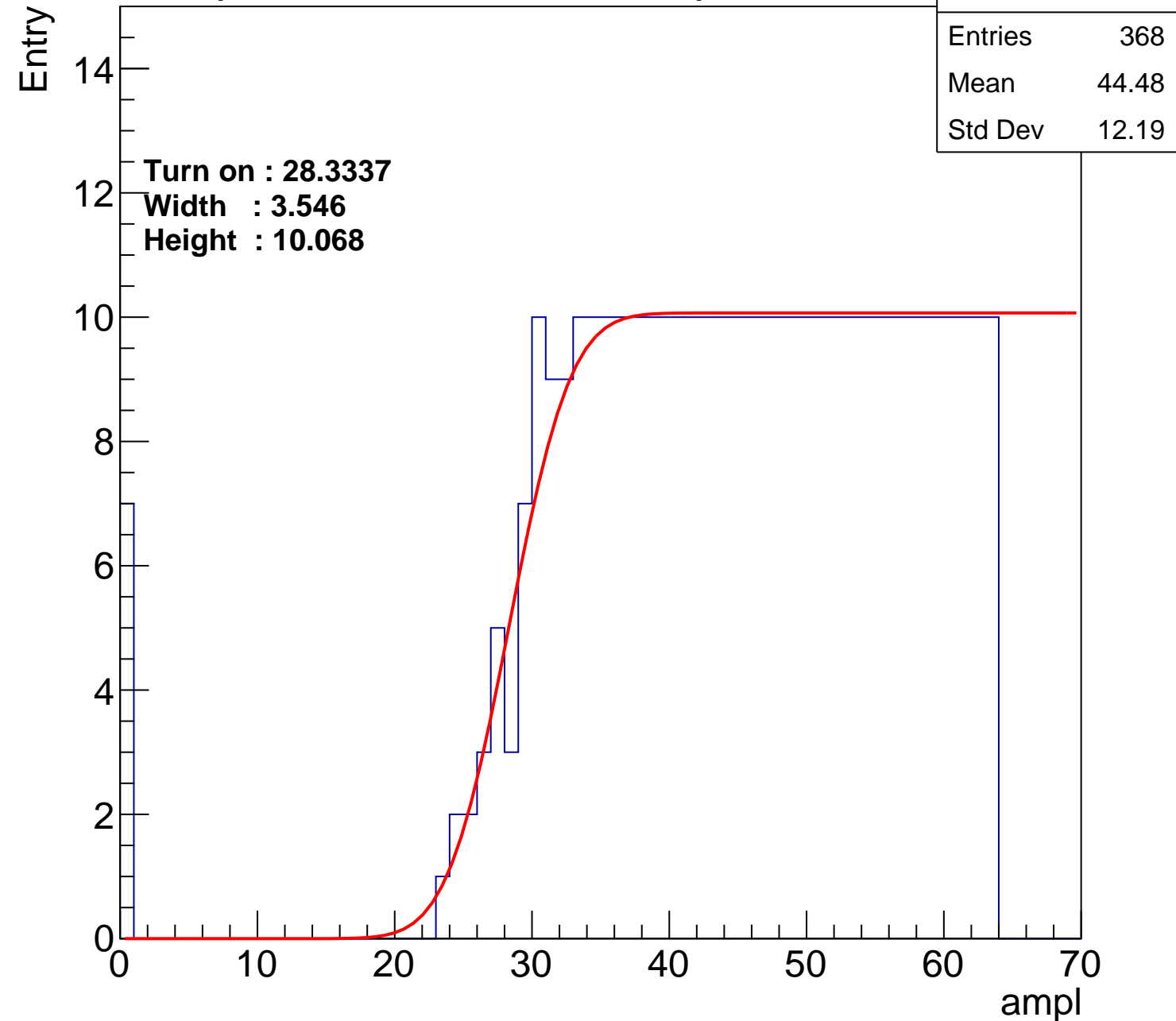
Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L101S, U20-ch84

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.39
Std Dev	11.65

Turn on : 27.4761

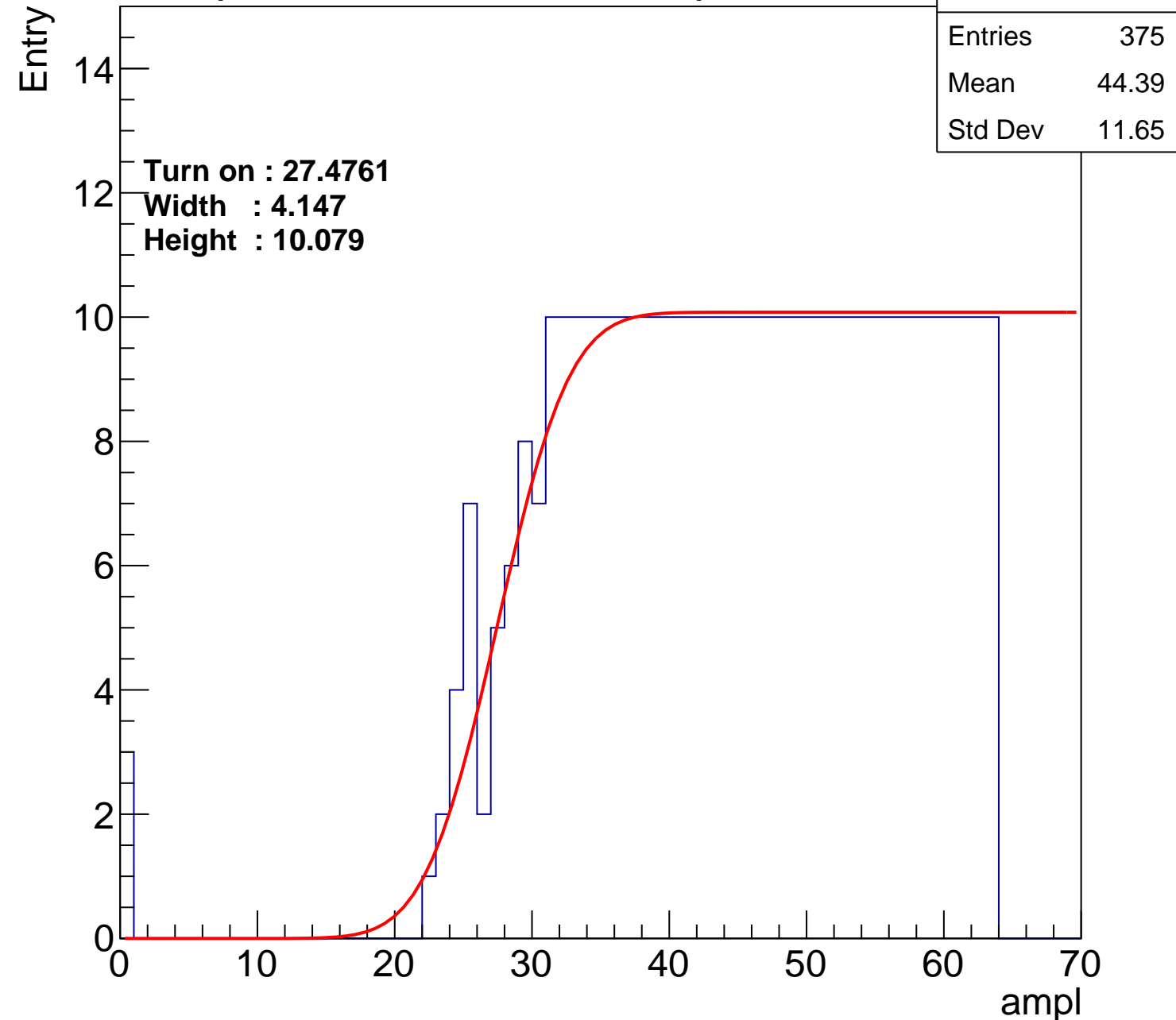
Width : 4.147

Height : 10.079

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch85

calib_packv5_042523_0143.root, FC#0, port D2

Entries	355
Mean	45.52
Std Dev	10.73

Turn on : 29.0335

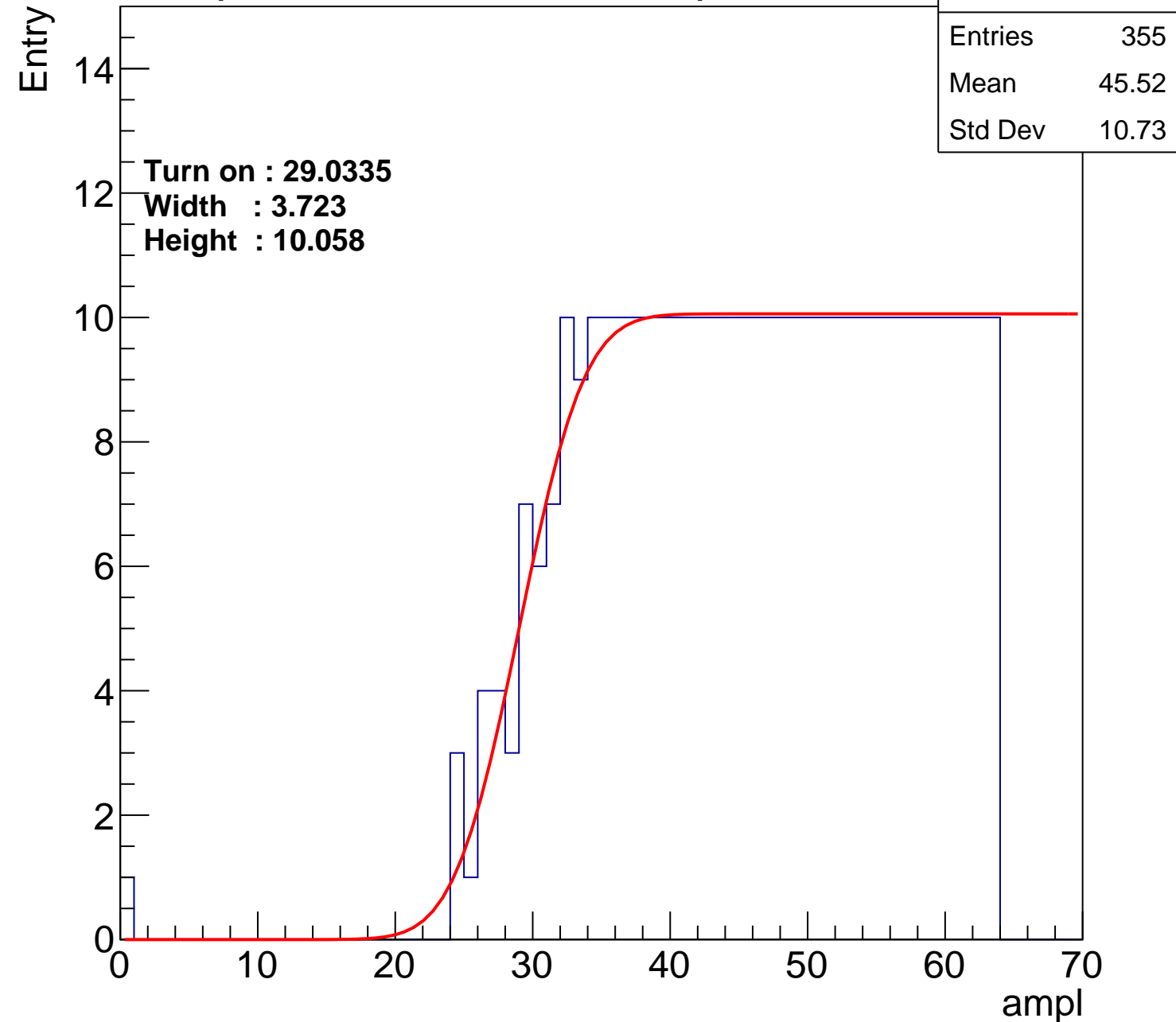
Width : 3.723

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch86

calib_packv5_042523_0143.root, FC#0, port D2

Entries	371
Mean	44.71
Std Dev	11.27

Turn on : 27.3322

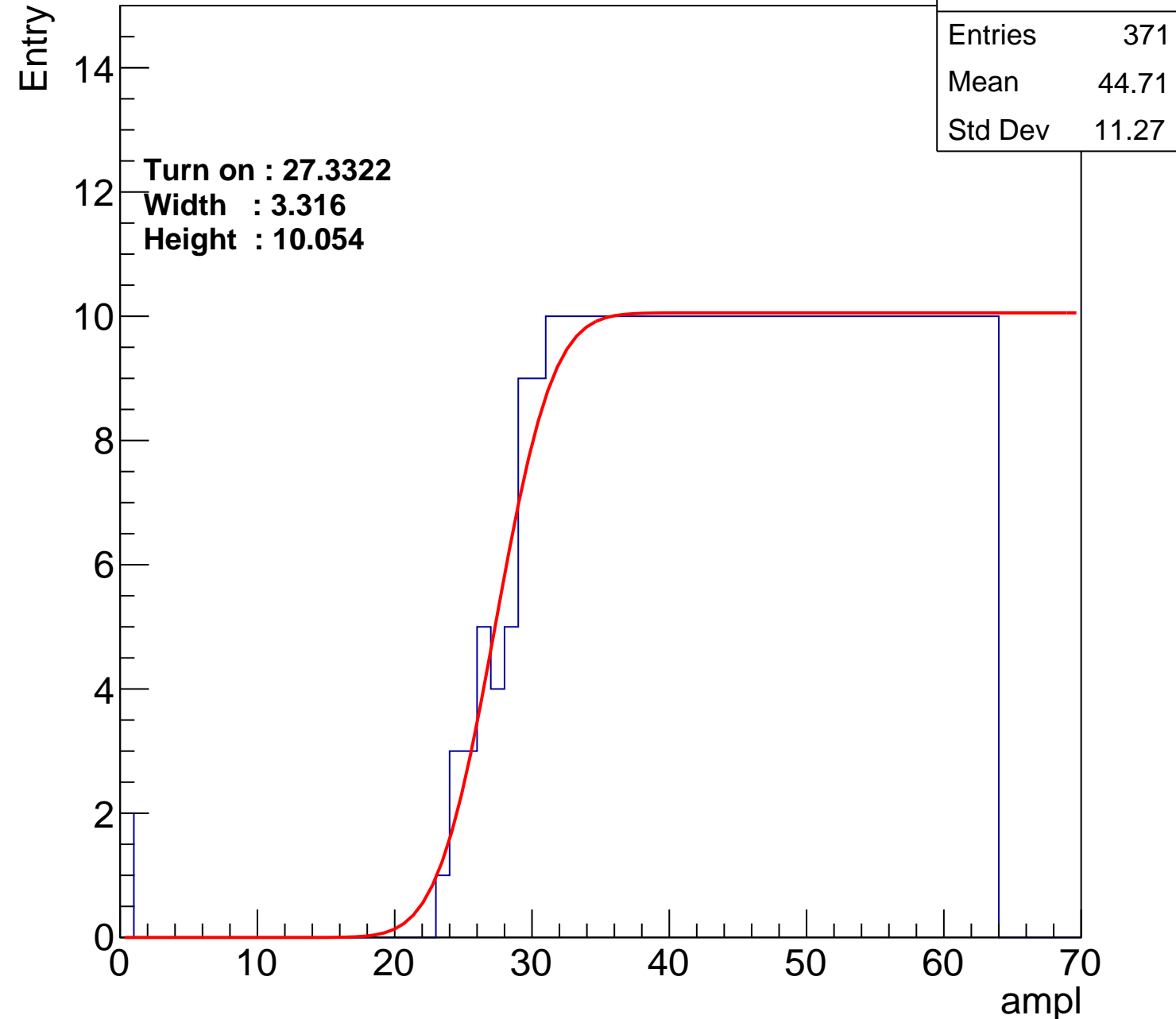
Width : 3.316

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch87

calib_packv5_042523_0143.root, FC#0, port D2

Entries	364
Mean	44.96
Std Dev	11.34

Turn on : 28.2814

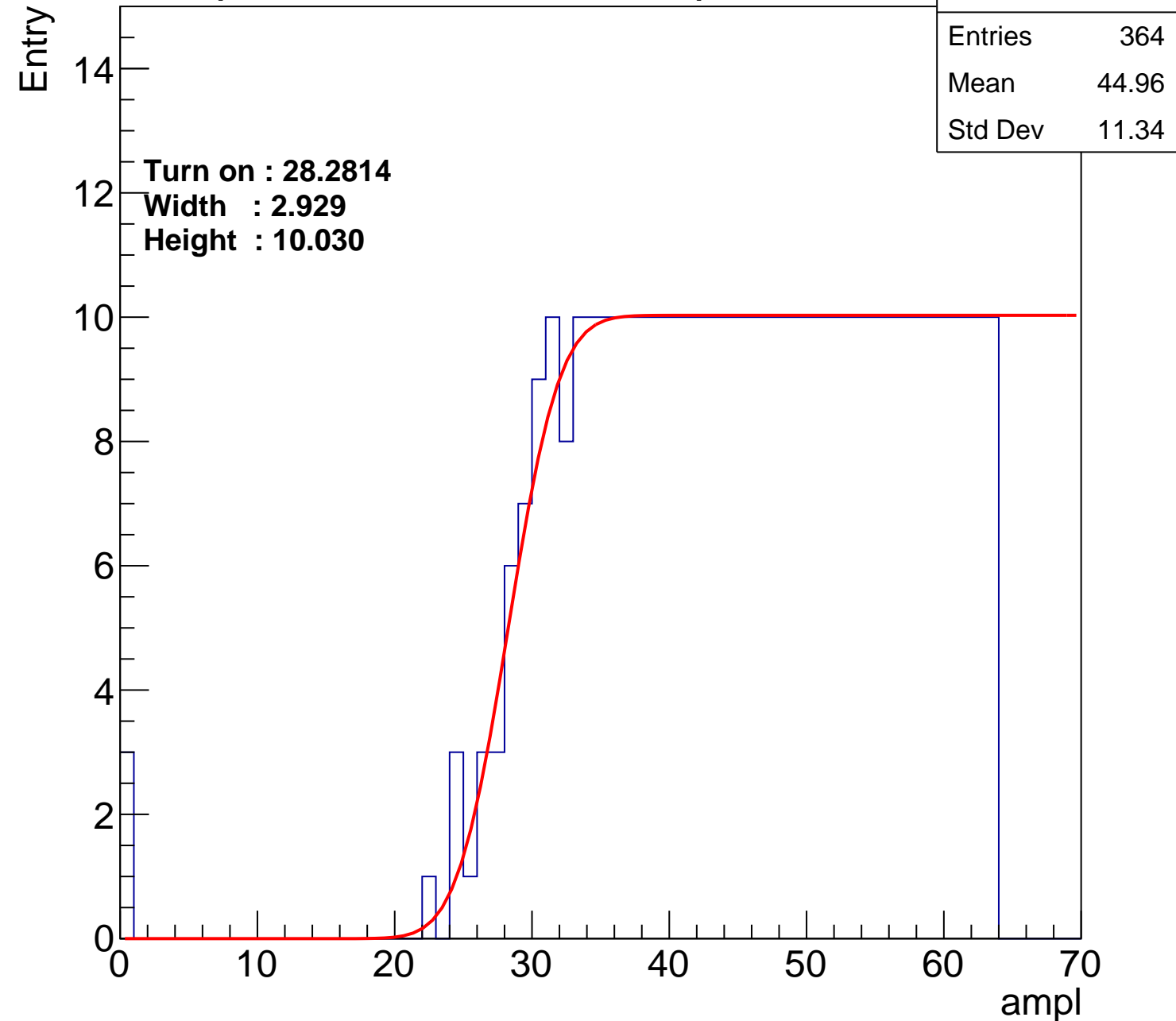
Width : 2.929

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch88

calib_packv5_042523_0143.root, FC#0, port D2

Entries	395
Mean	43.45
Std Dev	12.08

Turn on : 24.3854

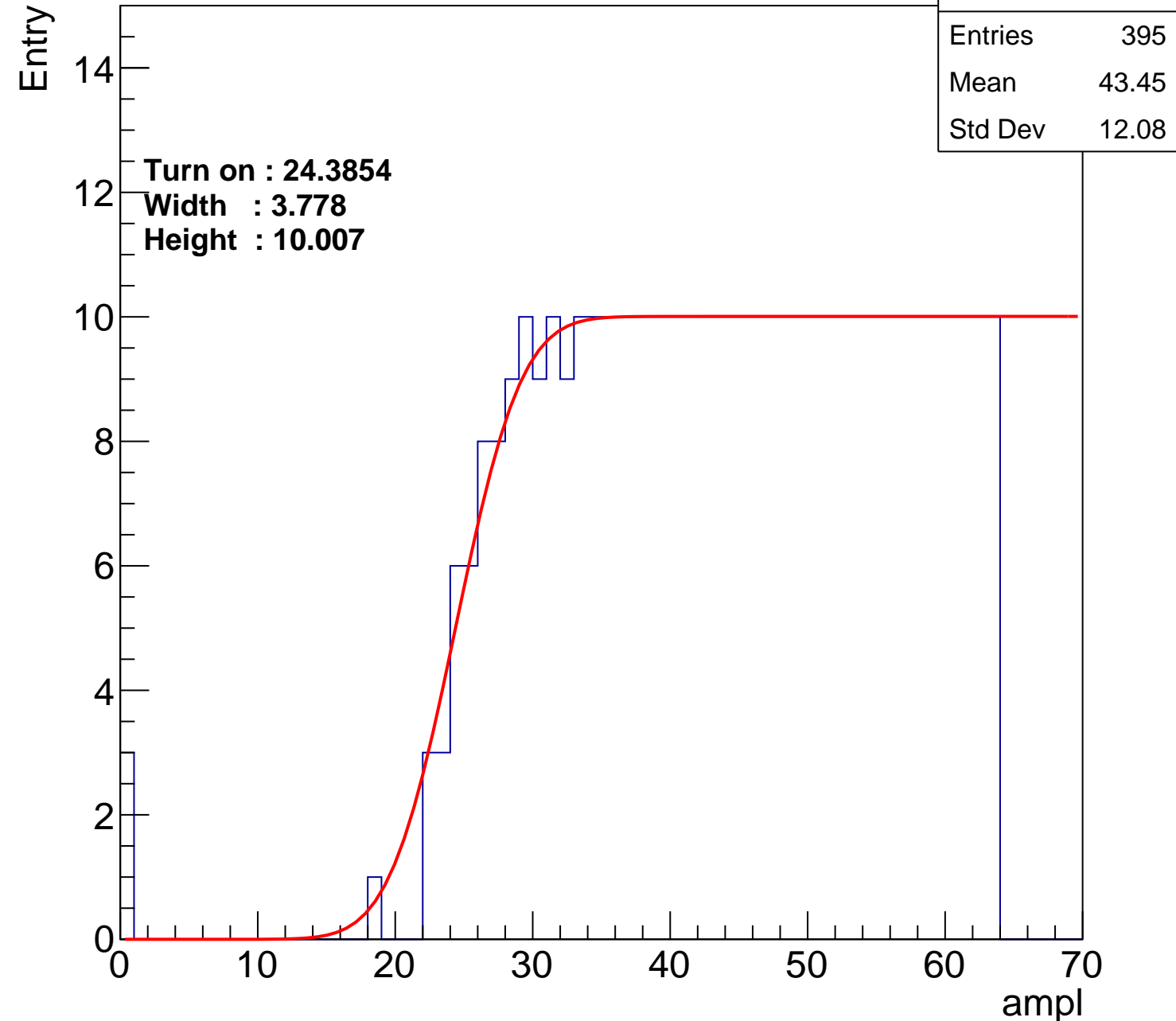
Width : 3.778

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch89

calib_packv5_042523_0143.root, FC#0, port D2

Entries	393
Mean	43.68
Std Dev	11.69

Turn on : 24.1676

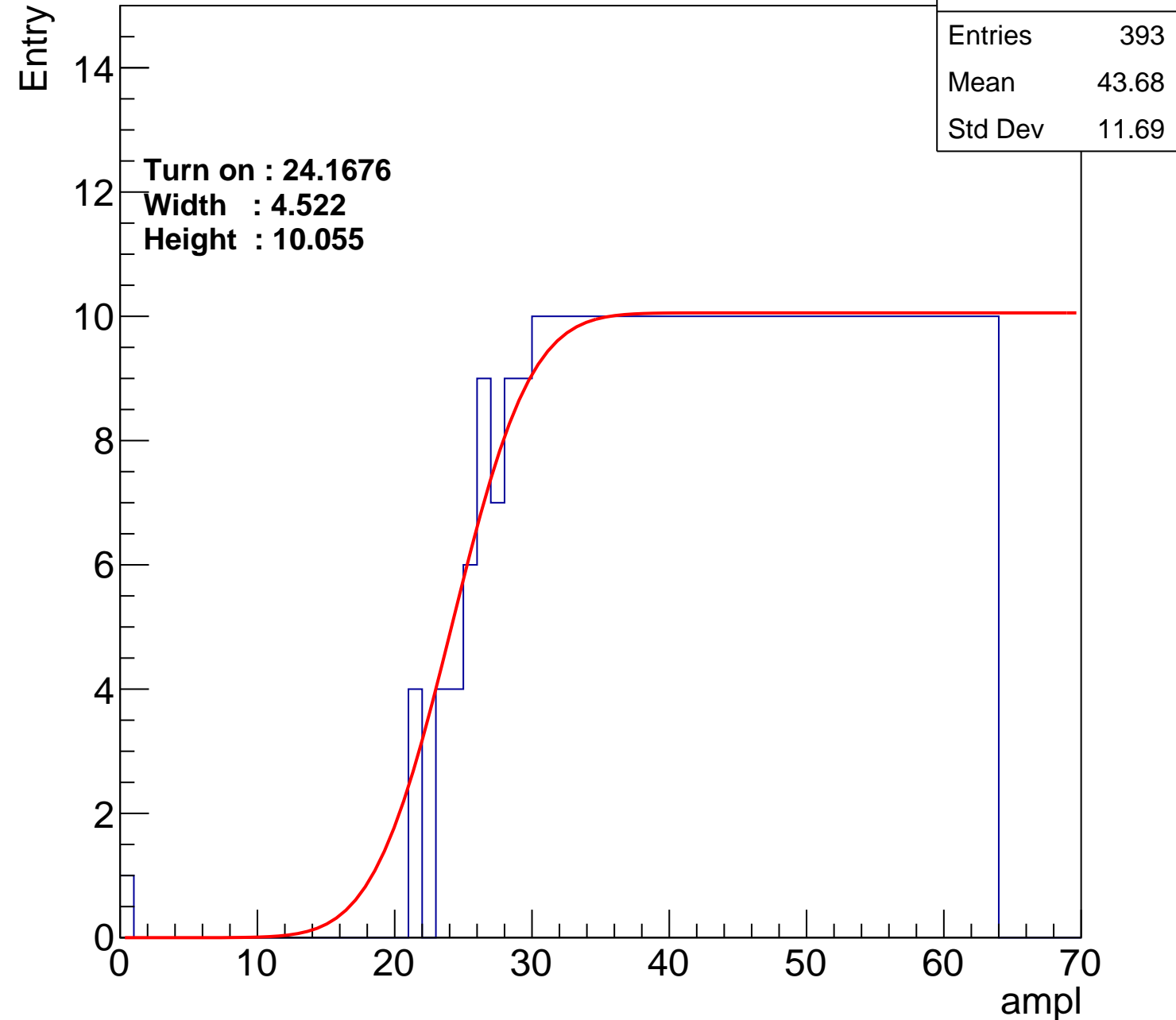
Width : 4.522

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch90

calib_packv5_042523_0143.root, FC#0, port D2

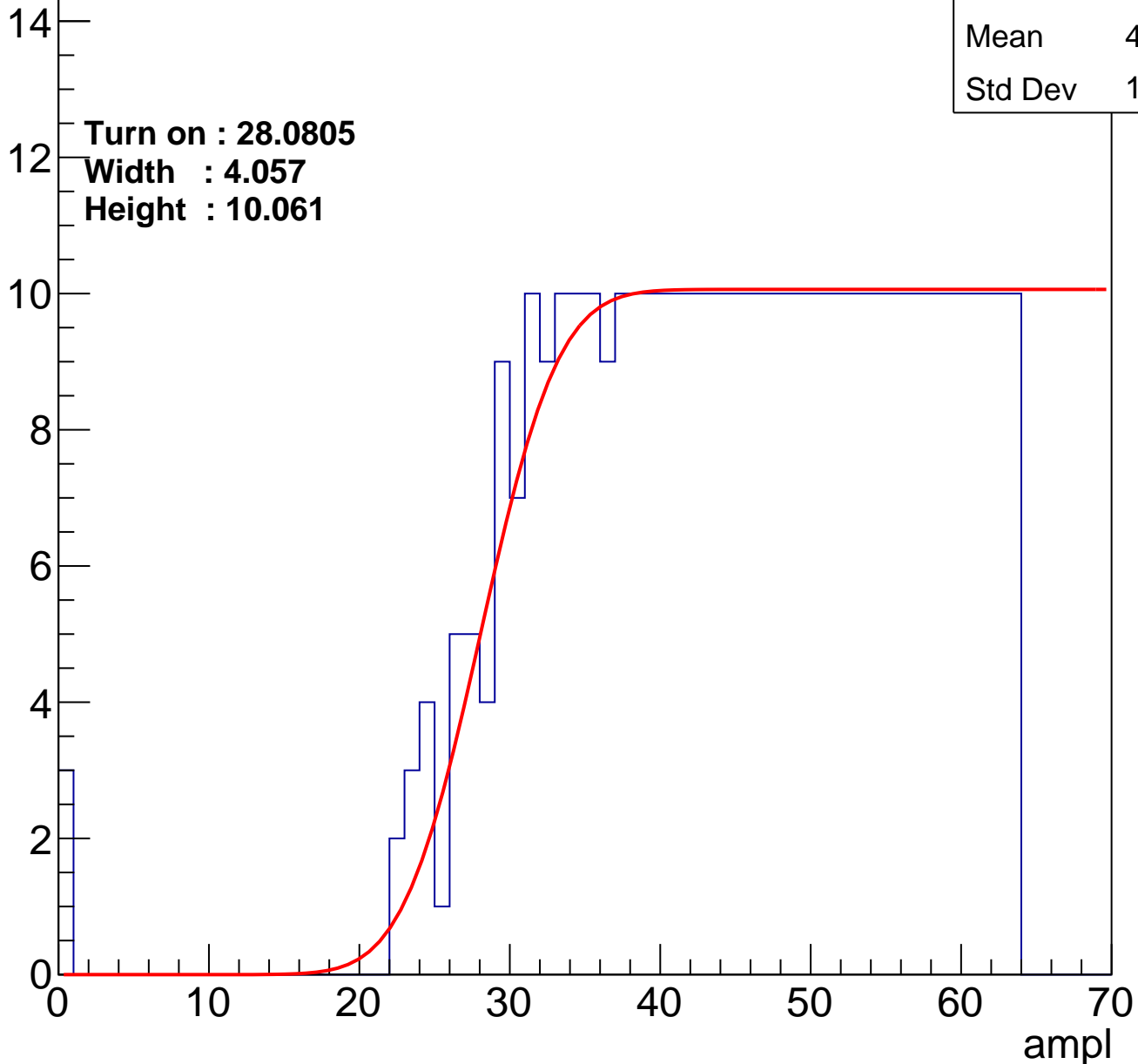
Entries	371
Mean	44.54
Std Dev	11.62

Turn on : 28.0805

Width : 4.057

Height : 10.061

Entry



B1L101S, U20-ch91

calib_packv5_042523_0143.root, FC#0, port D2

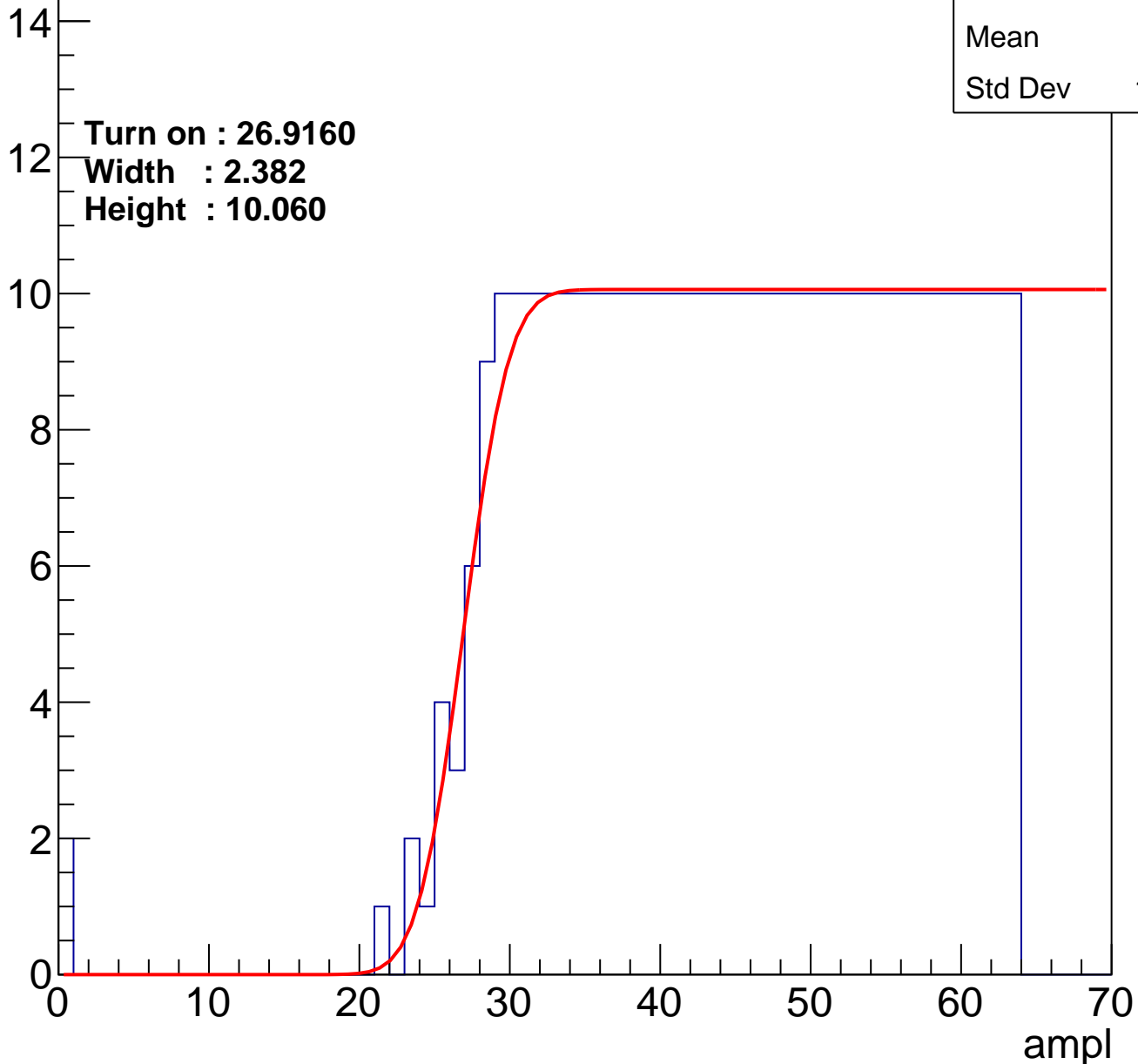
Entries	378
Mean	44.4
Std Dev	11.41

Turn on : 26.9160

Width : 2.382

Height : 10.060

Entry



B1L101S, U20-ch92

calib_packv5_042523_0143.root, FC#0, port D2

Entries	379
Mean	44.31
Std Dev	11.49

Turn on : 26.5071

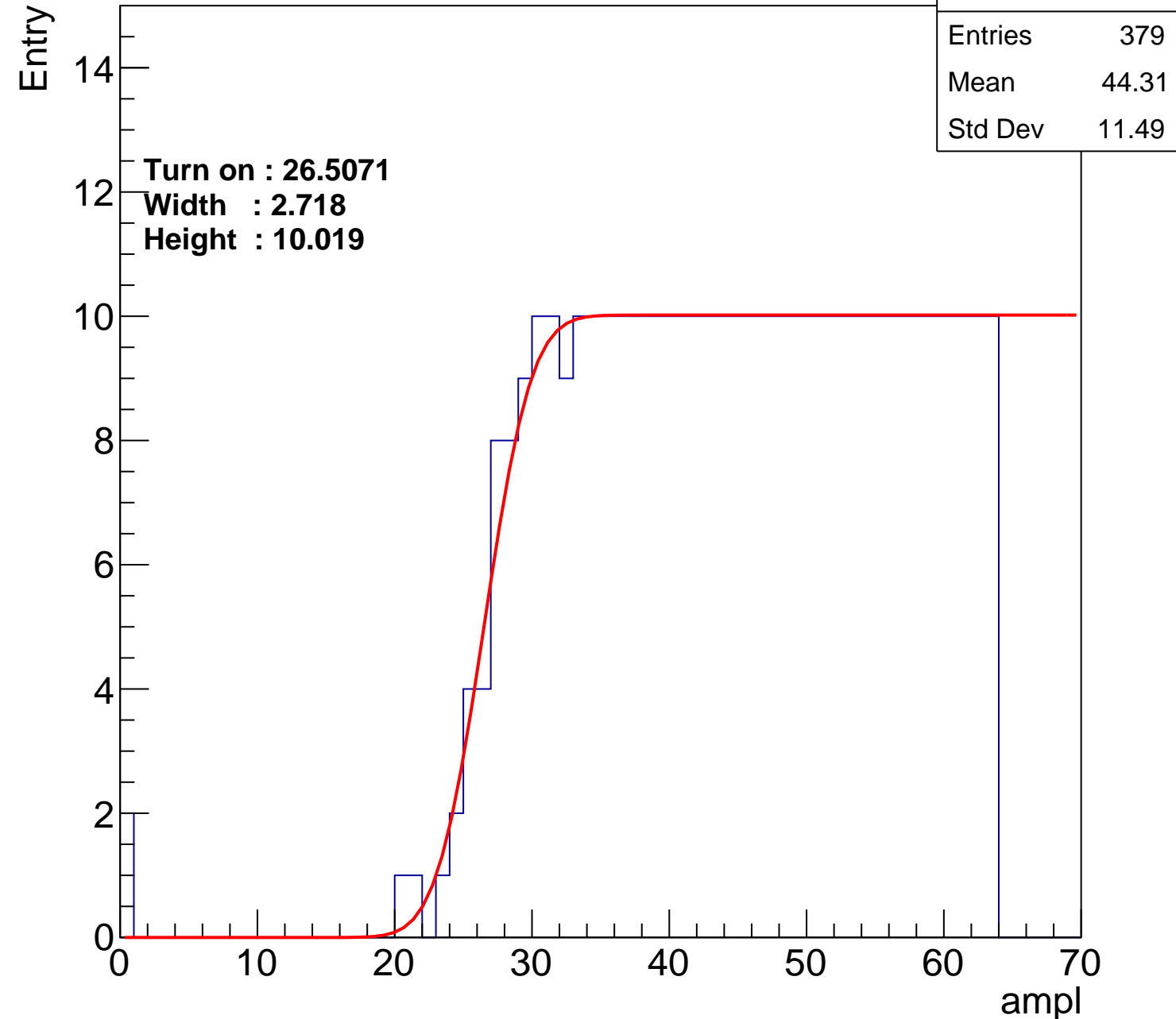
Width : 2.718

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch93

calib_packv5_042523_0143.root, FC#0, port D2

Entries	348
Mean	45.93
Std Dev	10.45

Turn on : 29.4994

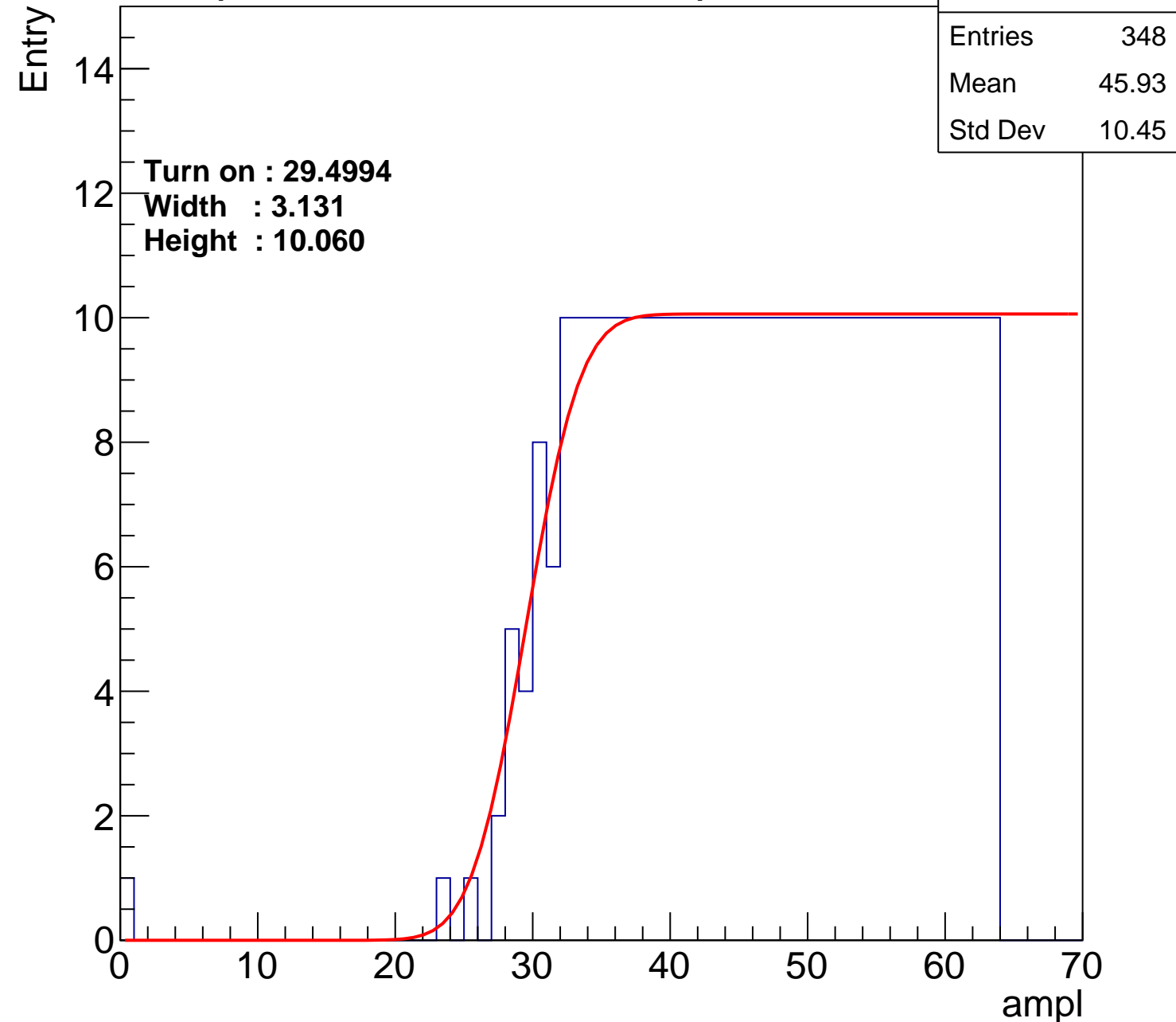
Width : 3.131

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch94

calib_packv5_042523_0143.root, FC#0, port D2

Entries	374
Mean	44.39
Std Dev	11.78

Turn on : 27.2085

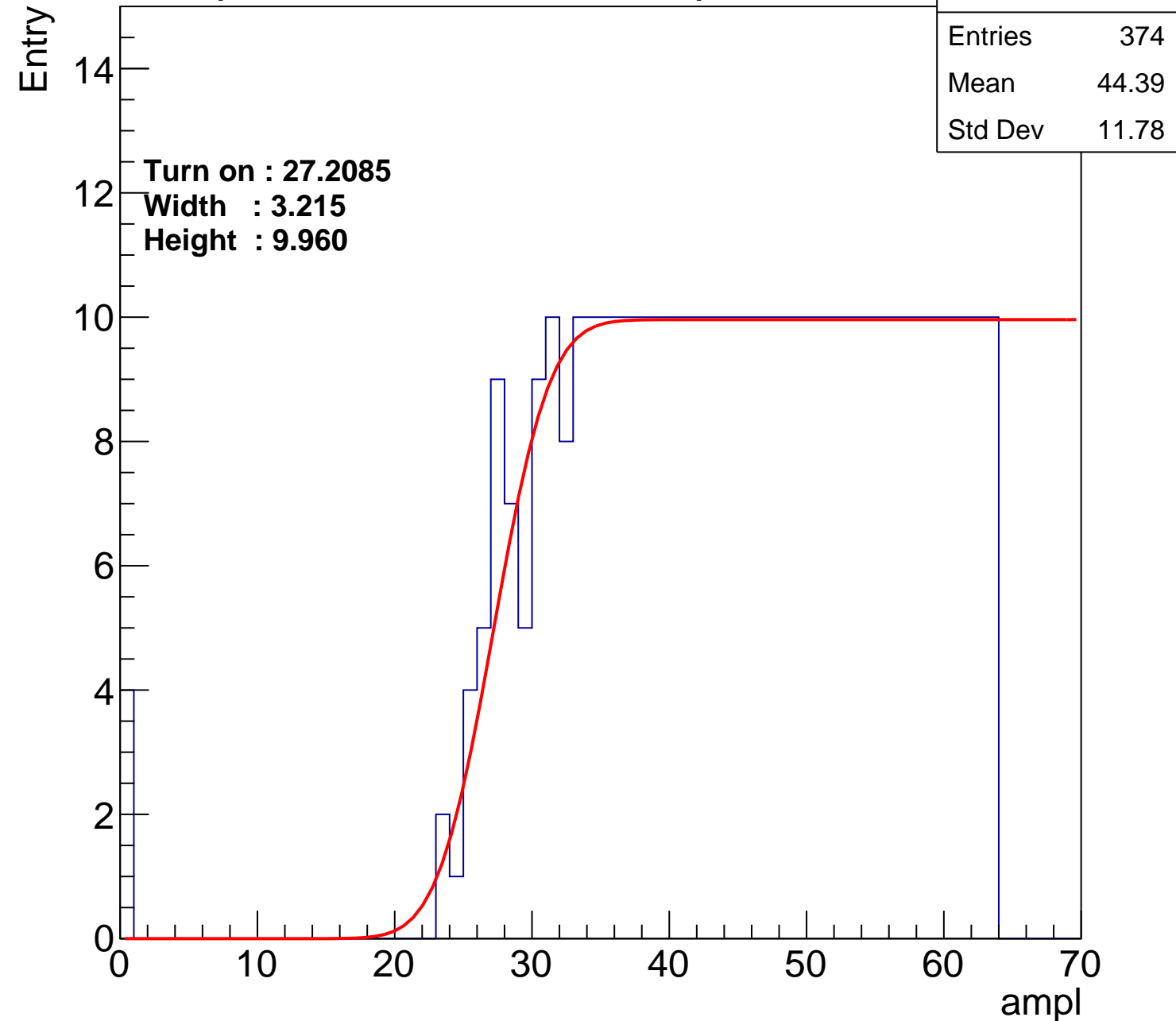
Width : 3.215

Height : 9.960

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch95

calib_packv5_042523_0143.root, FC#0, port D2

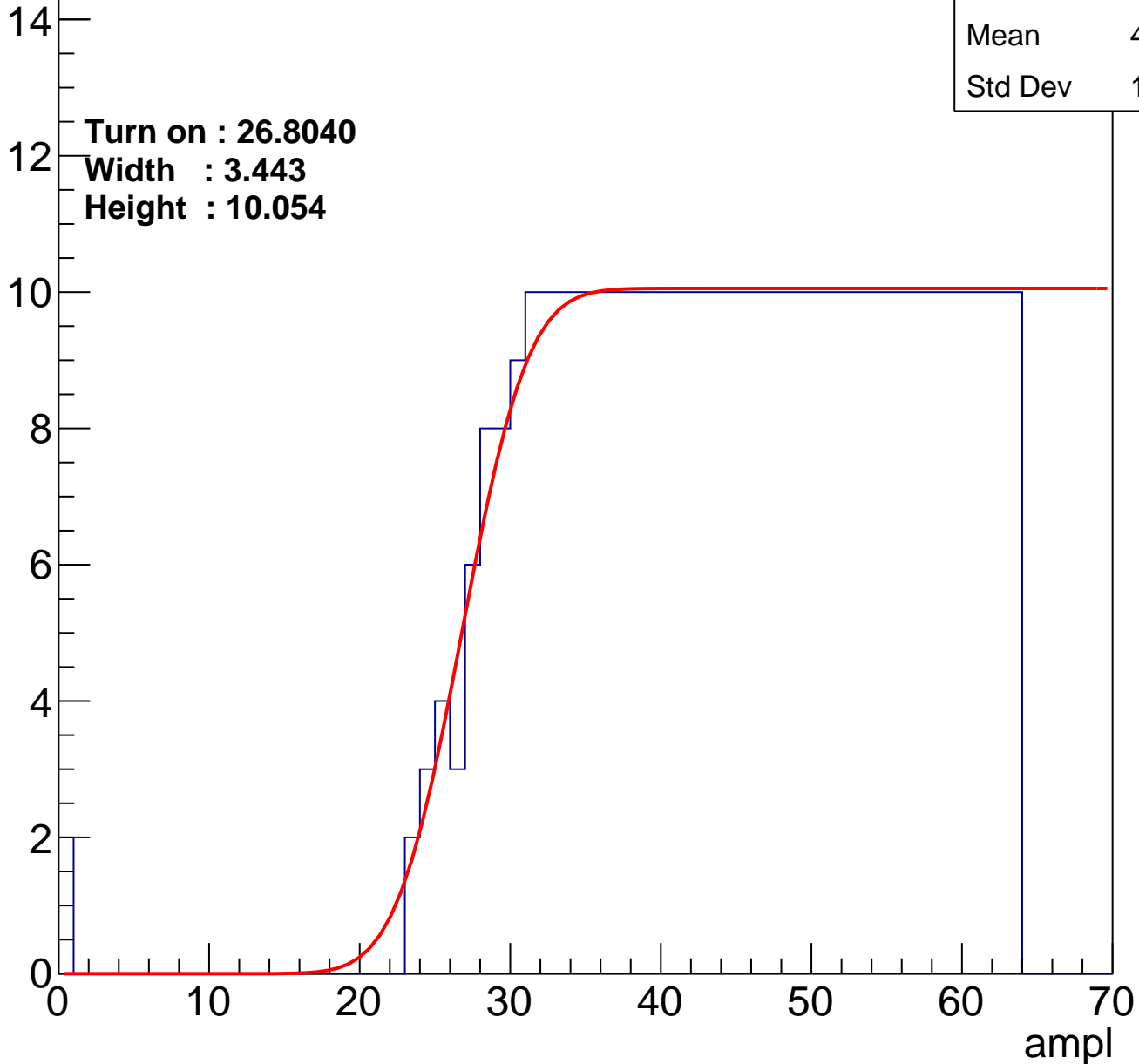
Entries	375
Mean	44.52
Std Dev	11.37

Turn on : 26.8040

Width : 3.443

Height : 10.054

Entry



B1L101S, U20-ch96

calib_packv5_042523_0143.root, FC#0, port D2

Entries	383
Mean	43.99
Std Dev	11.93

Turn on : 26.4805

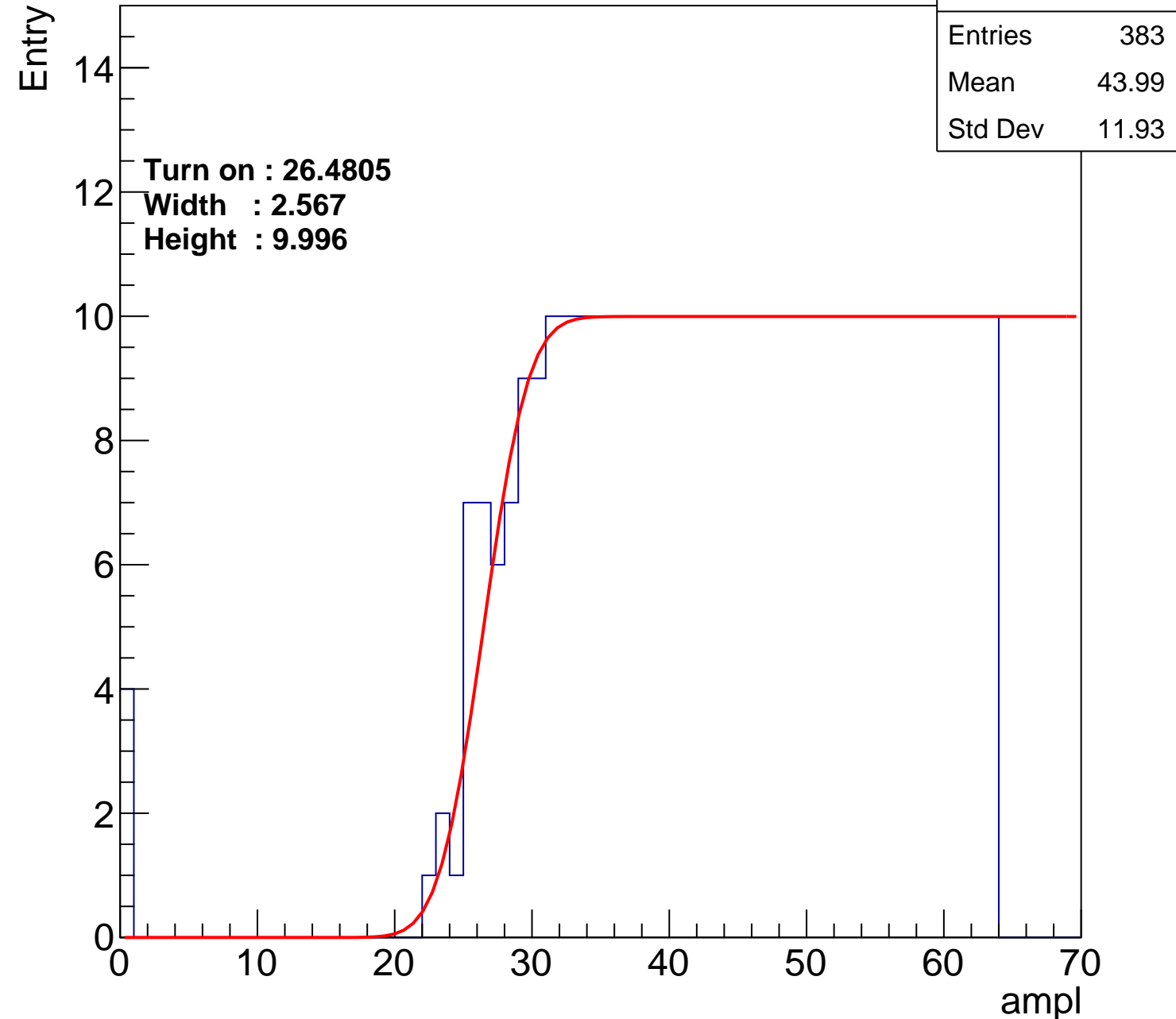
Width : 2.567

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch97

calib_packv5_042523_0143.root, FC#0, port D2

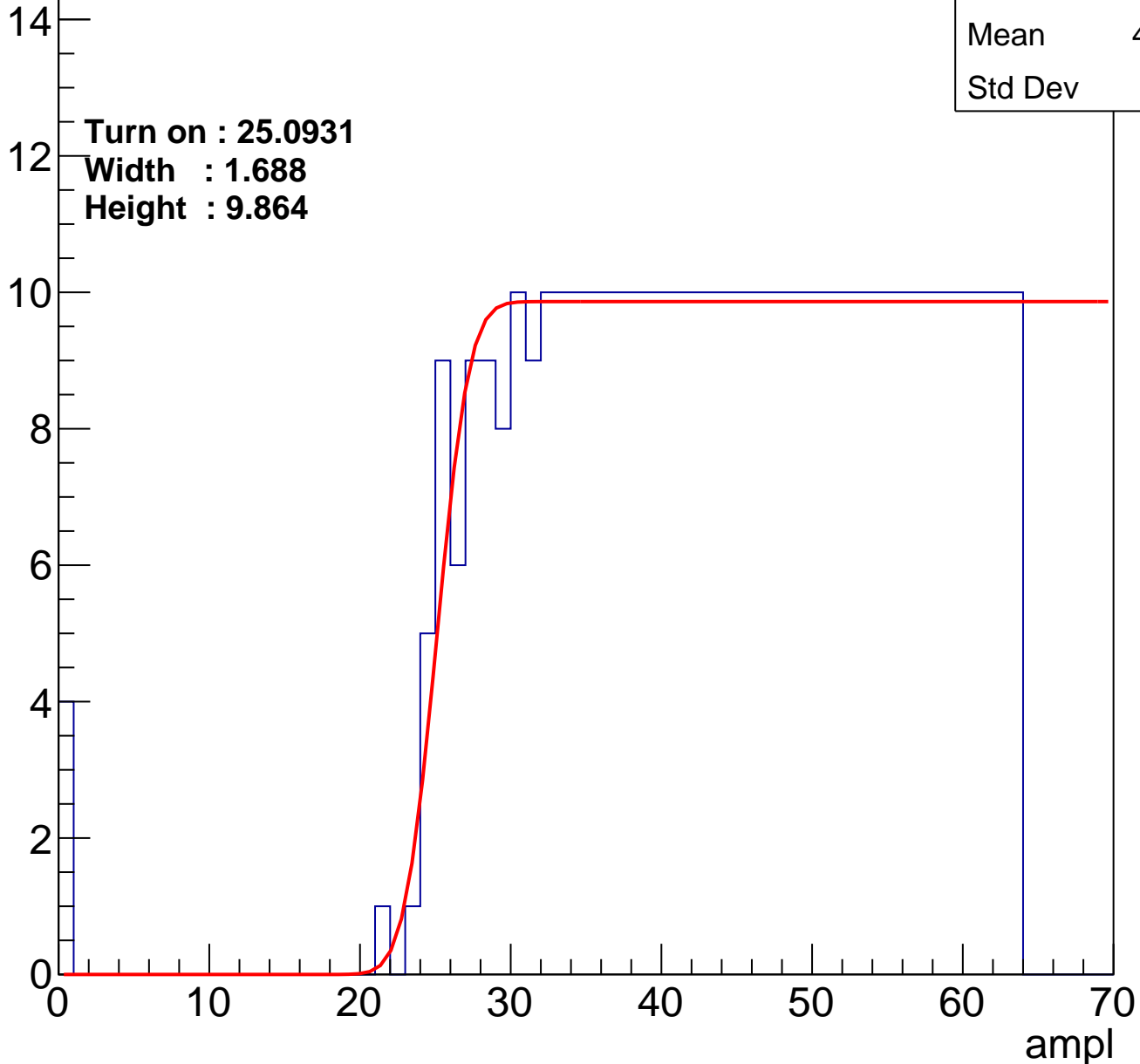
Entries	391
Mean	43.61
Std Dev	12.1

Turn on : 25.0931

Width : 1.688

Height : 9.864

Entry



B1L101S, U20-ch98

calib_packv5_042523_0143.root, FC#0, port D2

Entries	377
Mean	44.41
Std Dev	11.43

Turn on : 26.7769

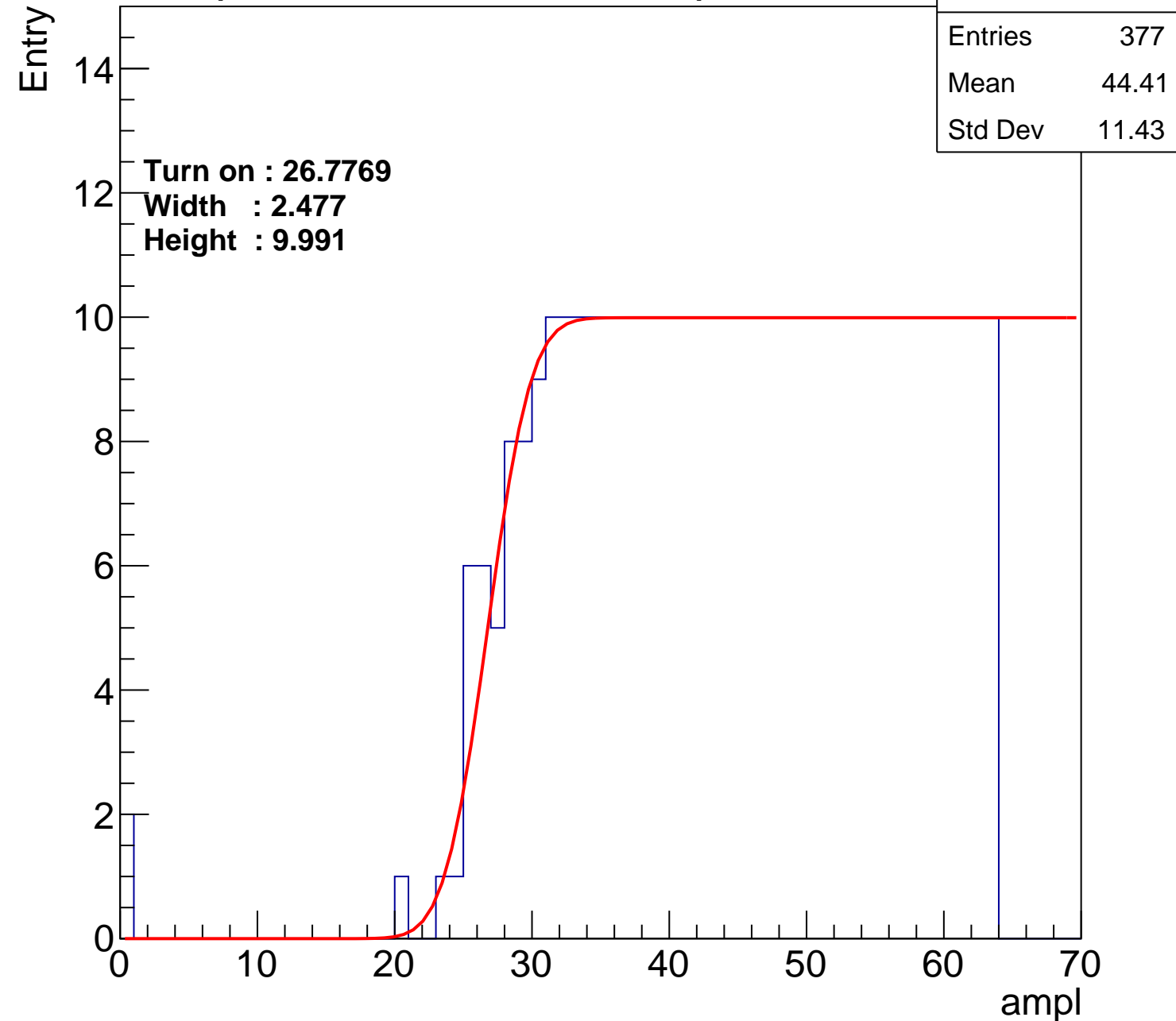
Width : 2.477

Height : 9.991

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch99

calib_packv5_042523_0143.root, FC#0, port D2

Entries	375
Mean	44.25
Std Dev	12.02

Turn on : 27.7447

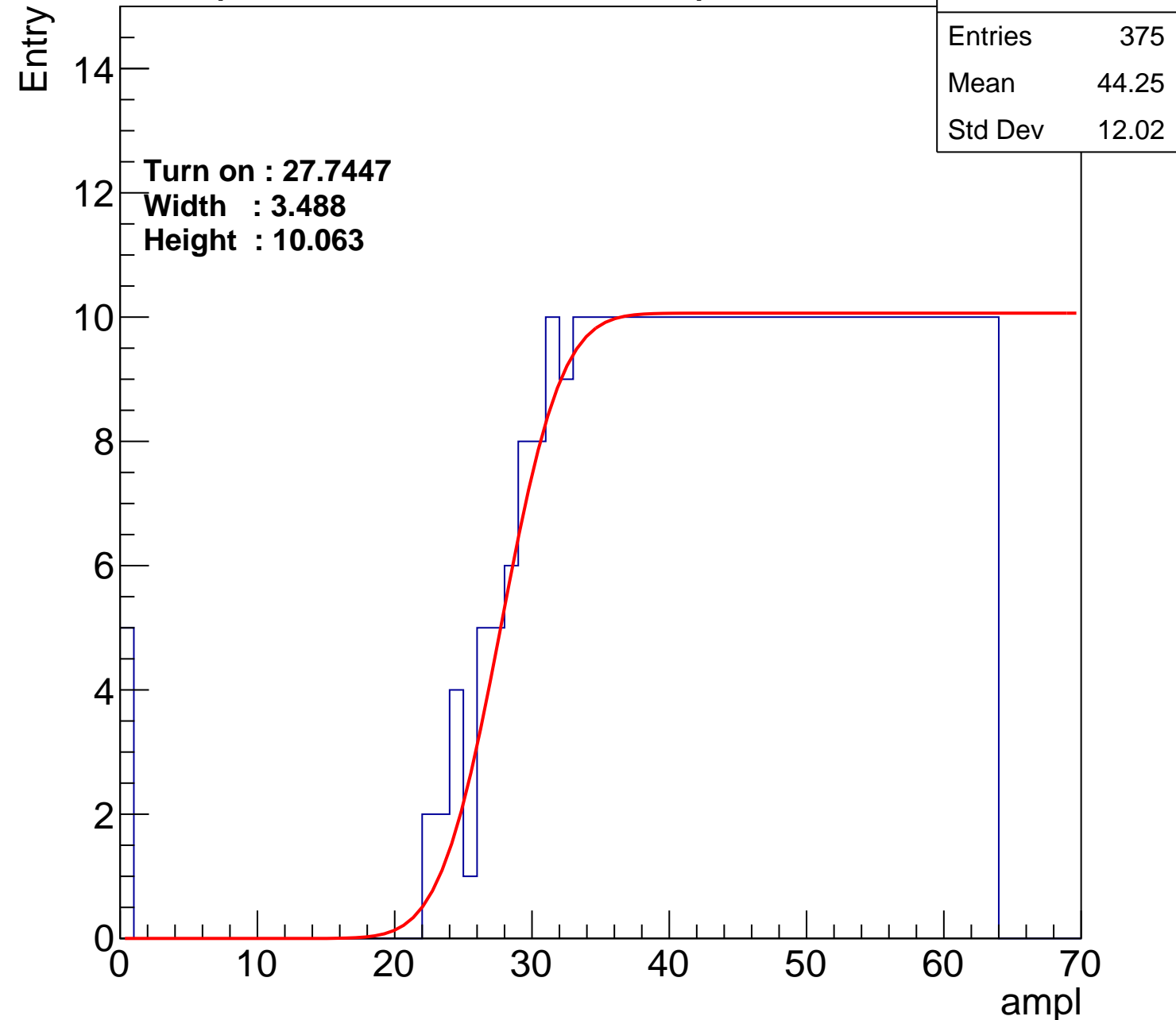
Width : 3.488

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch100

calib_packv5_042523_0143.root, FC#0, port D2

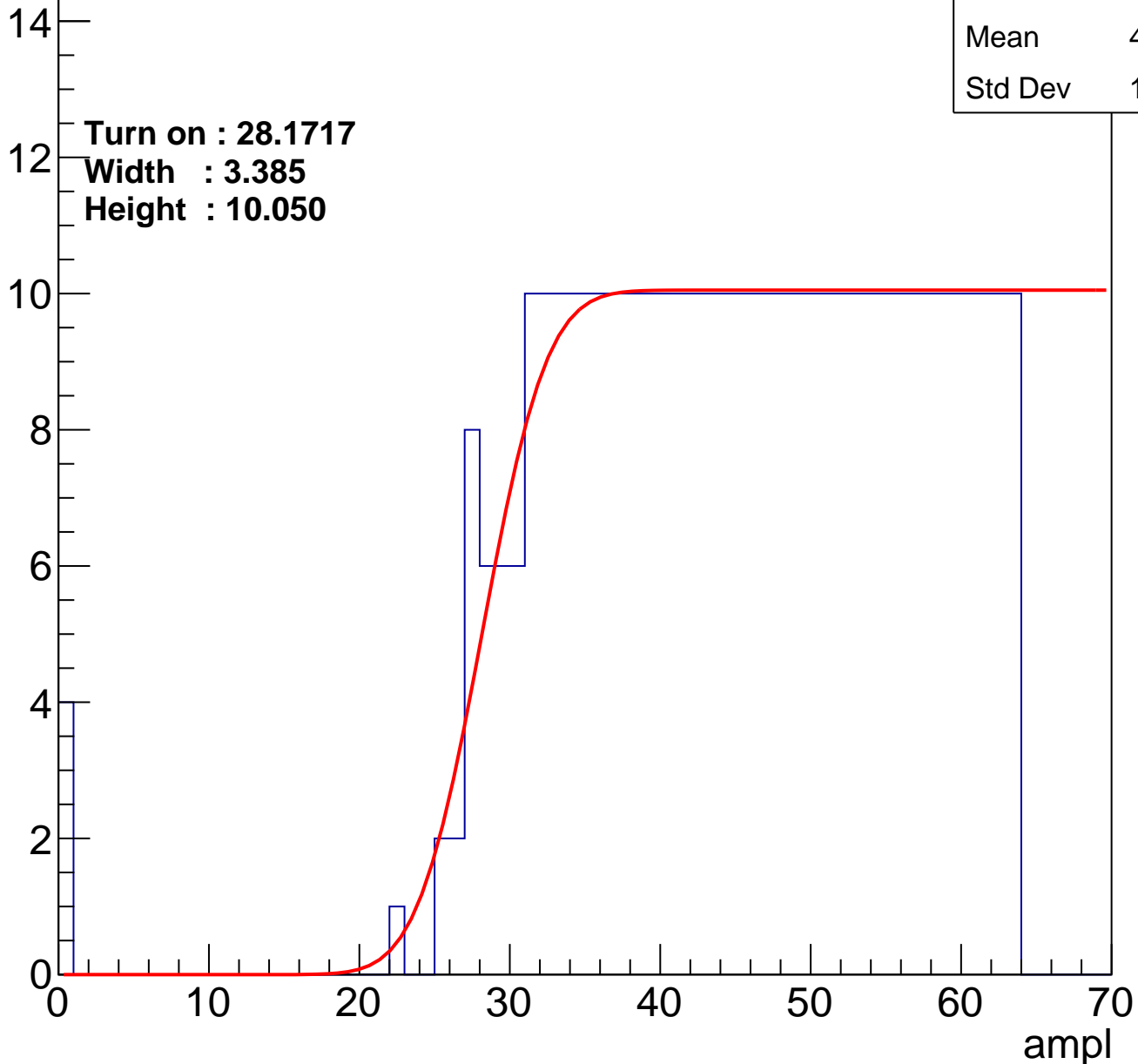
Entries	365
Mean	44.85
Std Dev	11.54

Turn on : 28.1717

Width : 3.385

Height : 10.050

Entry



B1L101S, U20-ch101

calib_packv5_042523_0143.root, FC#0, port D2

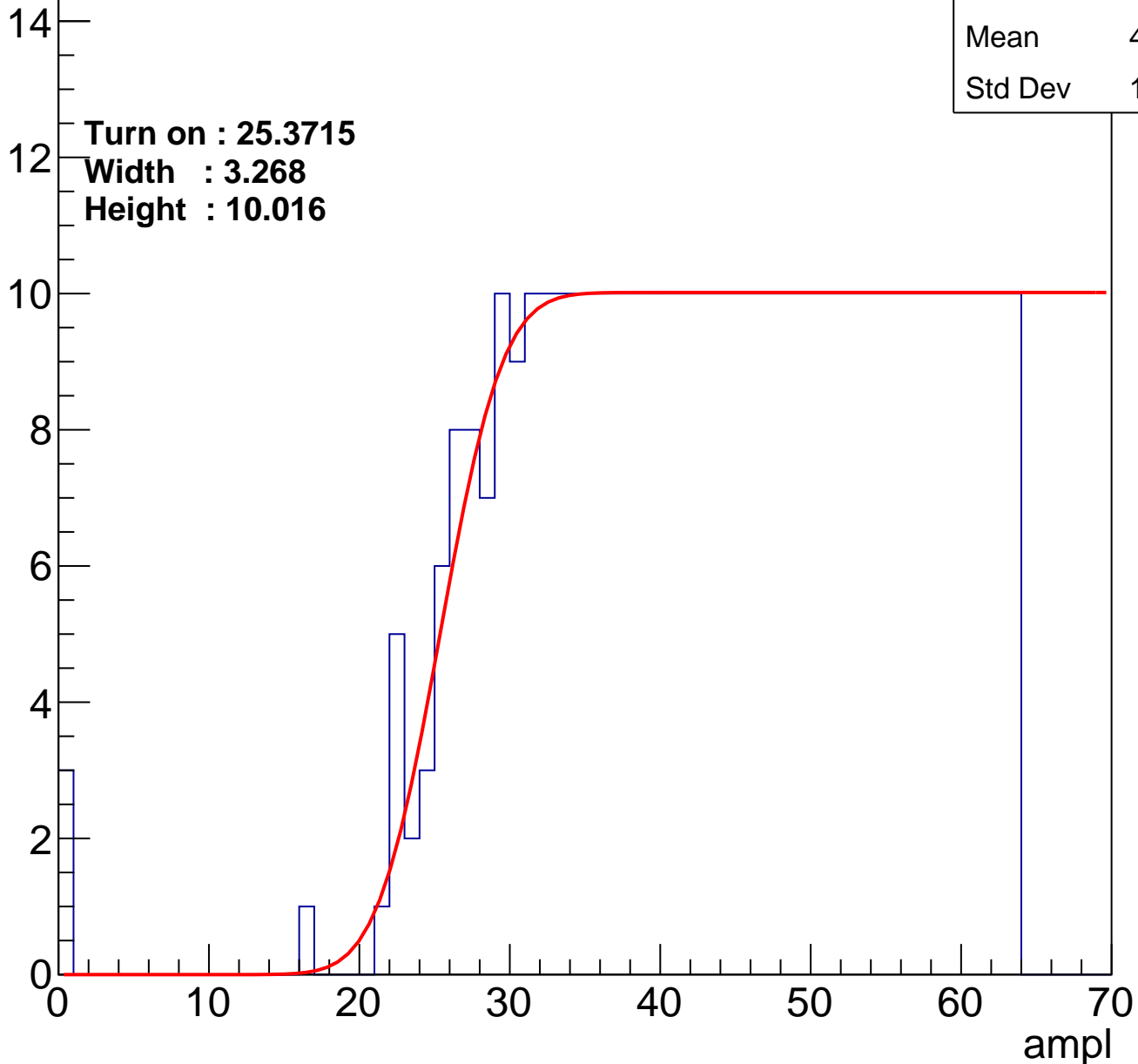
Entries	393
Mean	43.52
Std Dev	12.07

Turn on : 25.3715

Width : 3.268

Height : 10.016

Entry



B1L101S, U20-ch102

calib_packv5_042523_0143.root, FC#0, port D2

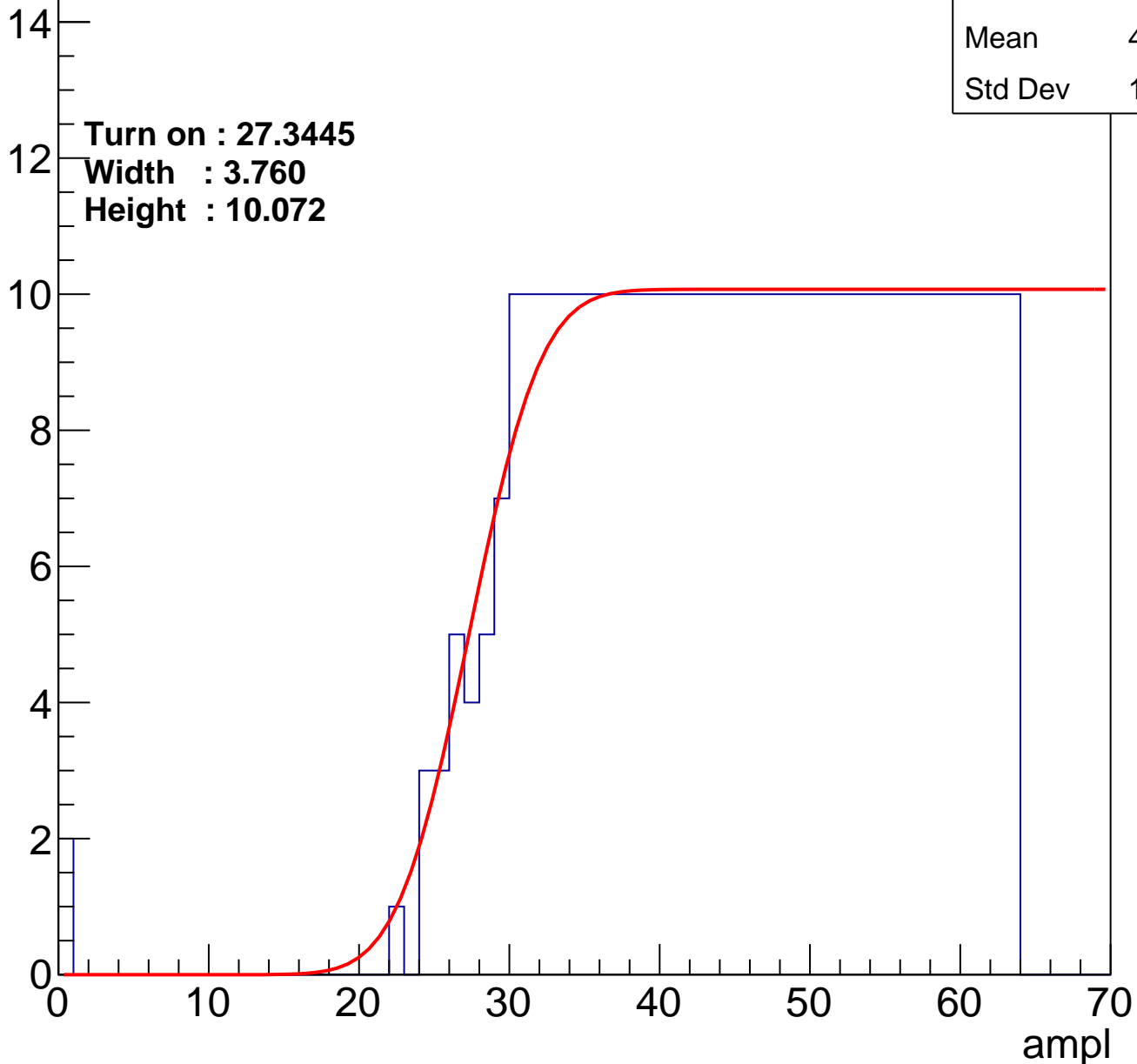
Entries	370
Mean	44.76
Std Dev	11.26

Turn on : 27.3445

Width : 3.760

Height : 10.072

Entry



B1L101S, U20-ch103

calib_packv5_042523_0143.root, FC#0, port D2

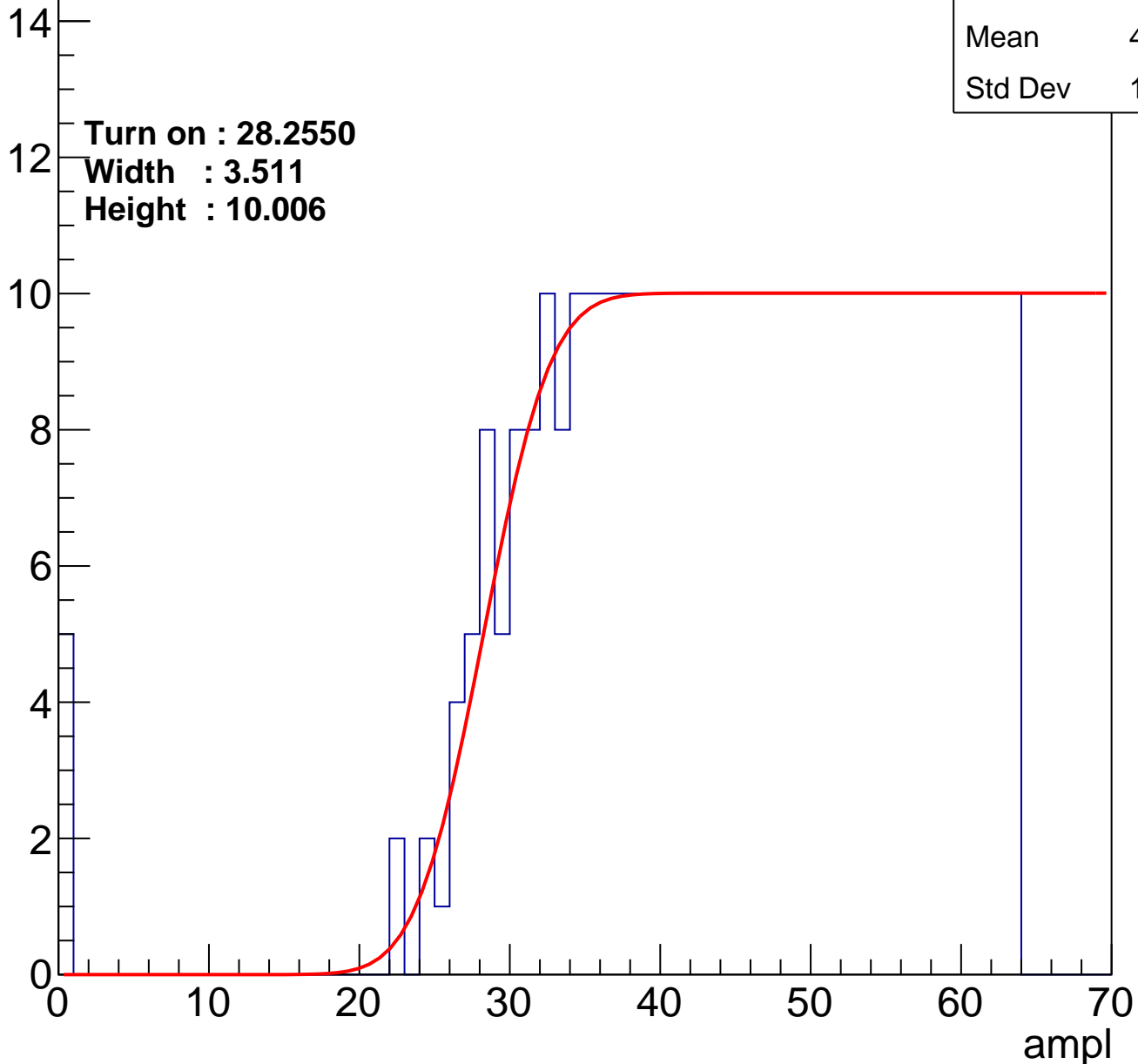
Entries	366
Mean	44.66
Std Dev	11.86

Turn on : 28.2550

Width : 3.511

Height : 10.006

Entry



B1L101S, U20-ch104

calib_packv5_042523_0143.root, FC#0, port D2

Entries	386
Mean	43.83
Std Dev	12.02

Turn on : 26.1675

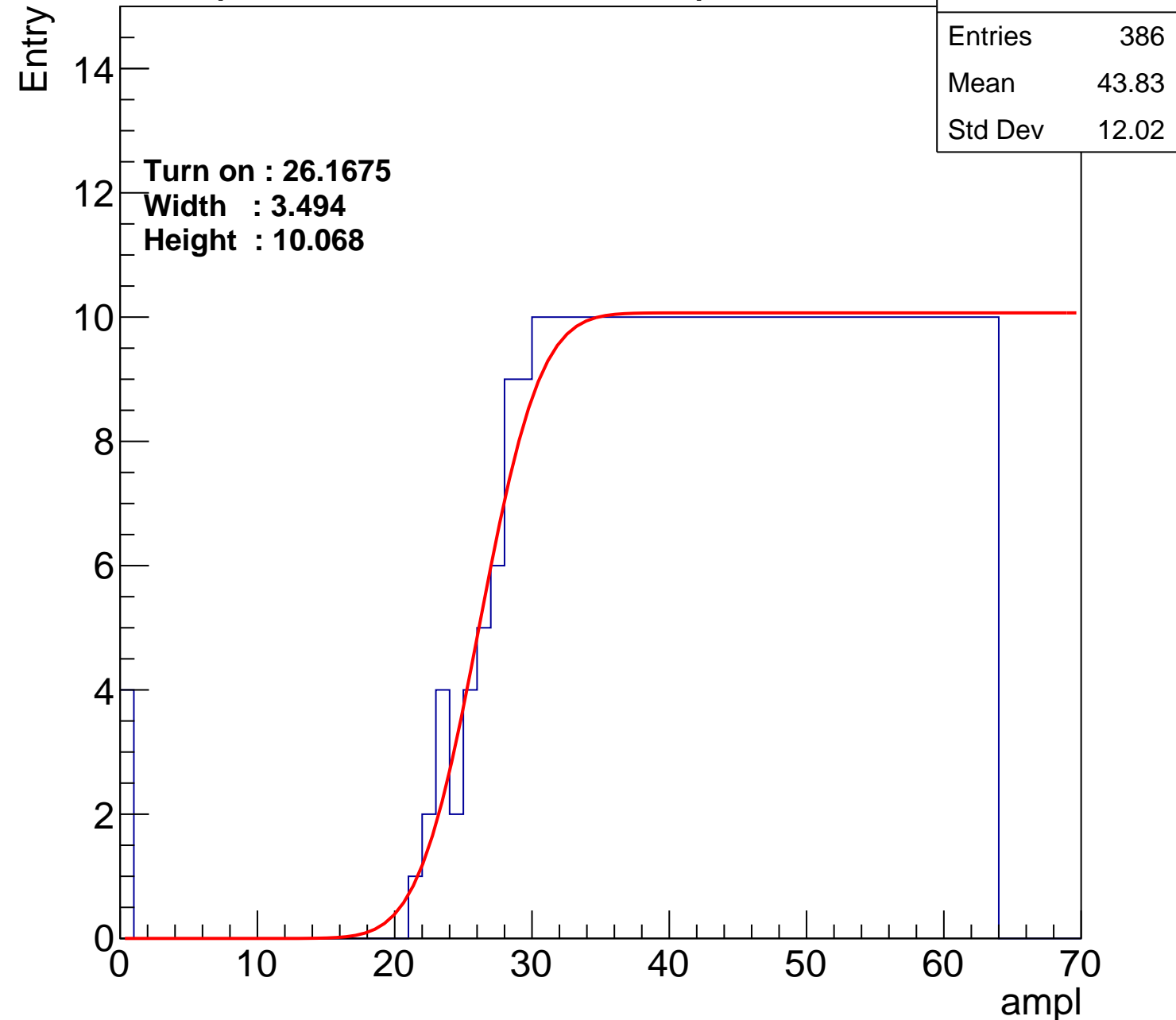
Width : 3.494

Height : 10.068

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch105

calib_packv5_042523_0143.root, FC#0, port D2

Entries	372
Mean	44.48
Std Dev	11.76

Turn on : 28.1351

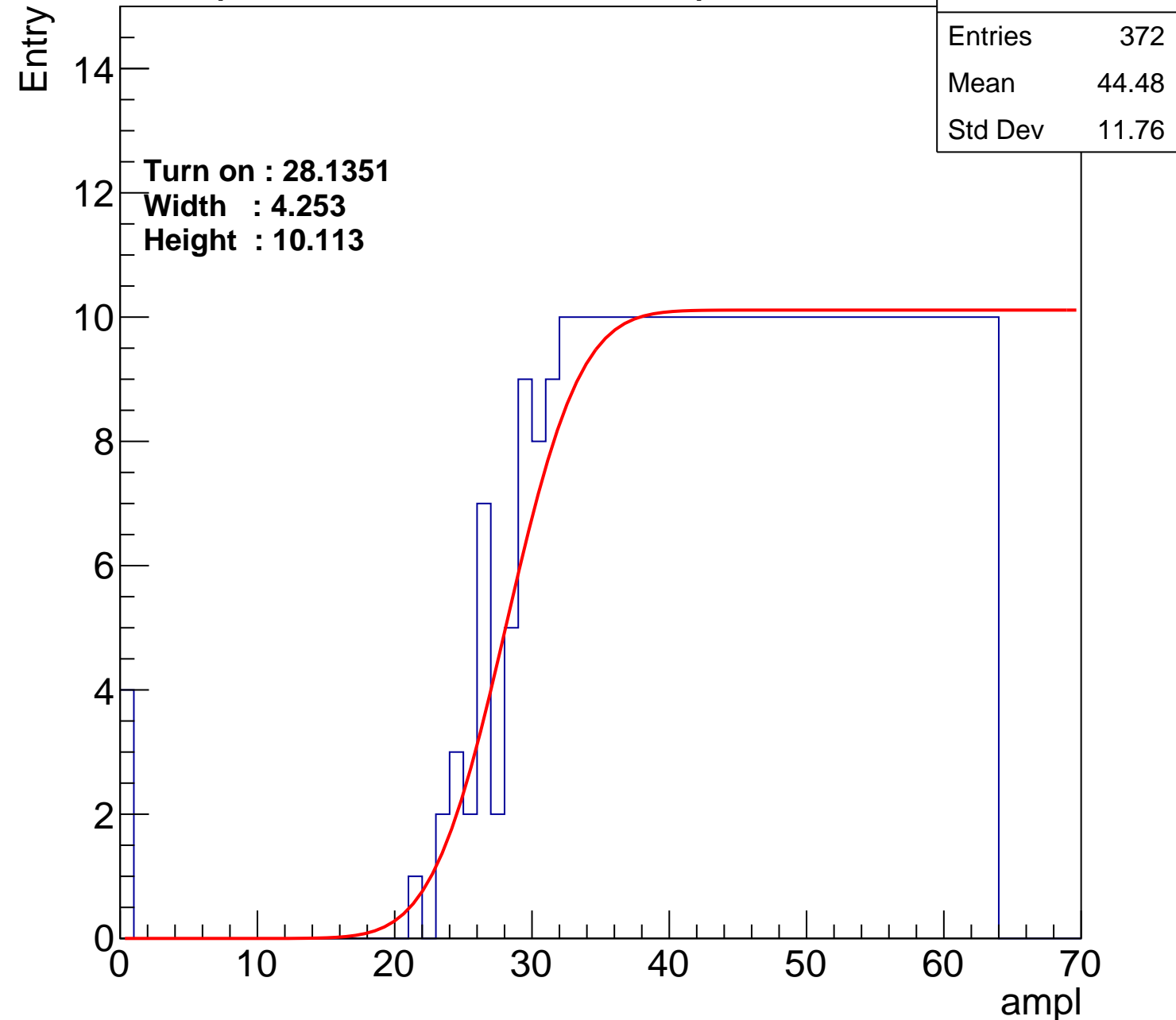
Width : 4.253

Height : 10.113

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch106

calib_packv5_042523_0143.root, FC#0, port D2

Entries	386
Mean	43.97
Std Dev	11.67

Turn on : 25.9769

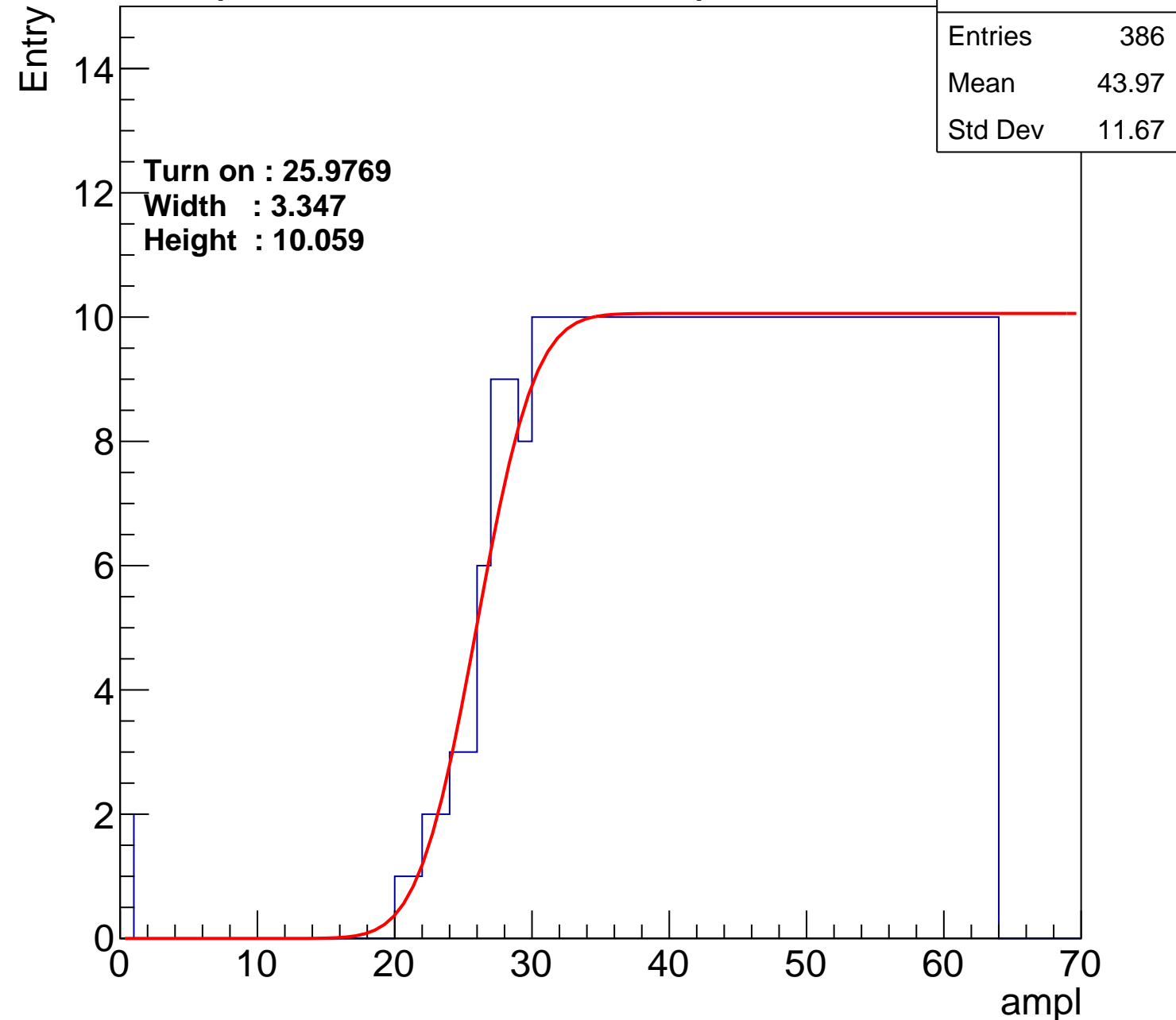
Width : 3.347

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch107

calib_packv5_042523_0143.root, FC#0, port D2

Entries	367
Mean	44.88
Std Dev	11.22

Turn on : 28.0669

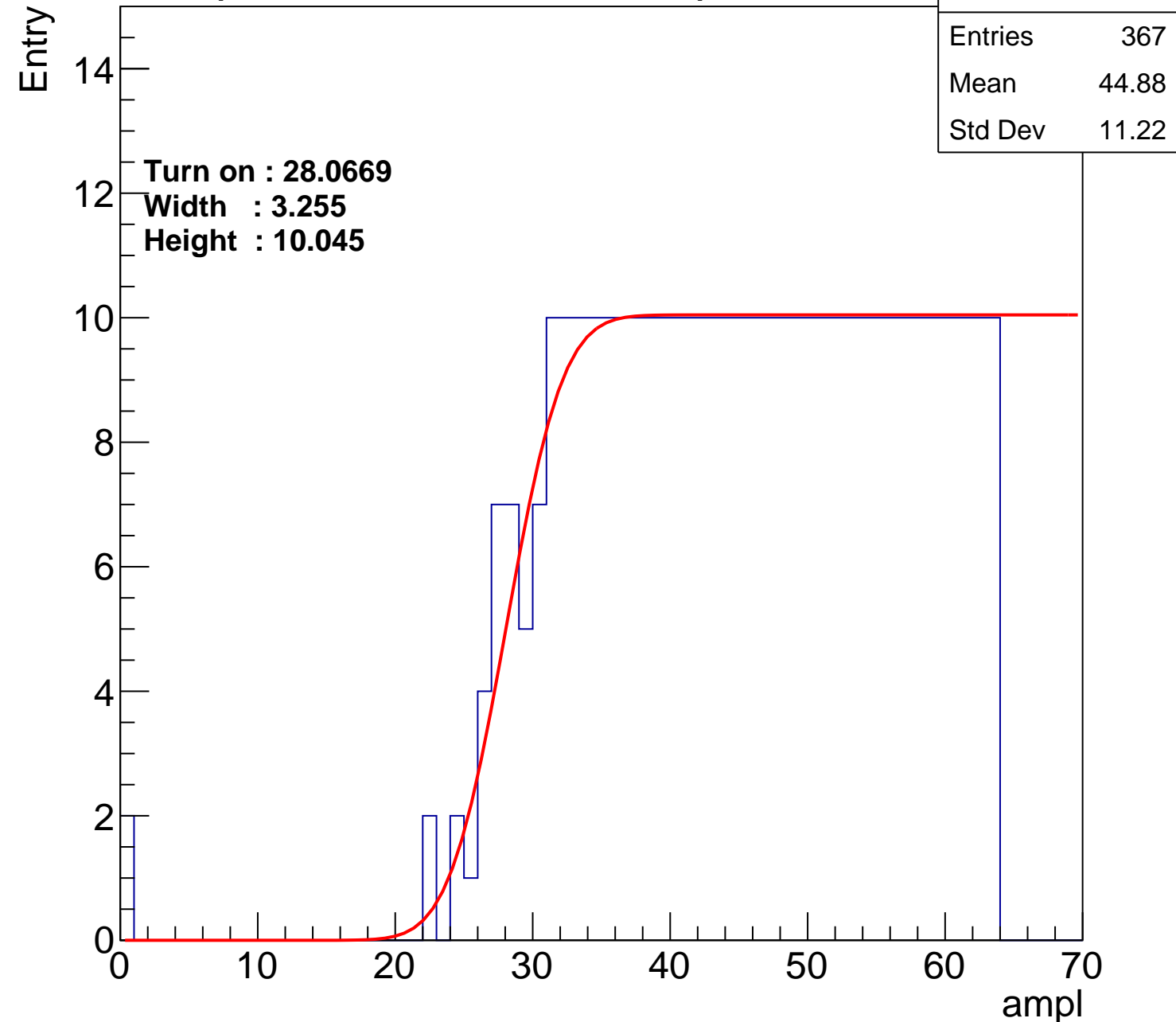
Width : 3.255

Height : 10.045

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch108

calib_packv5_042523_0143.root, FC#0, port D2

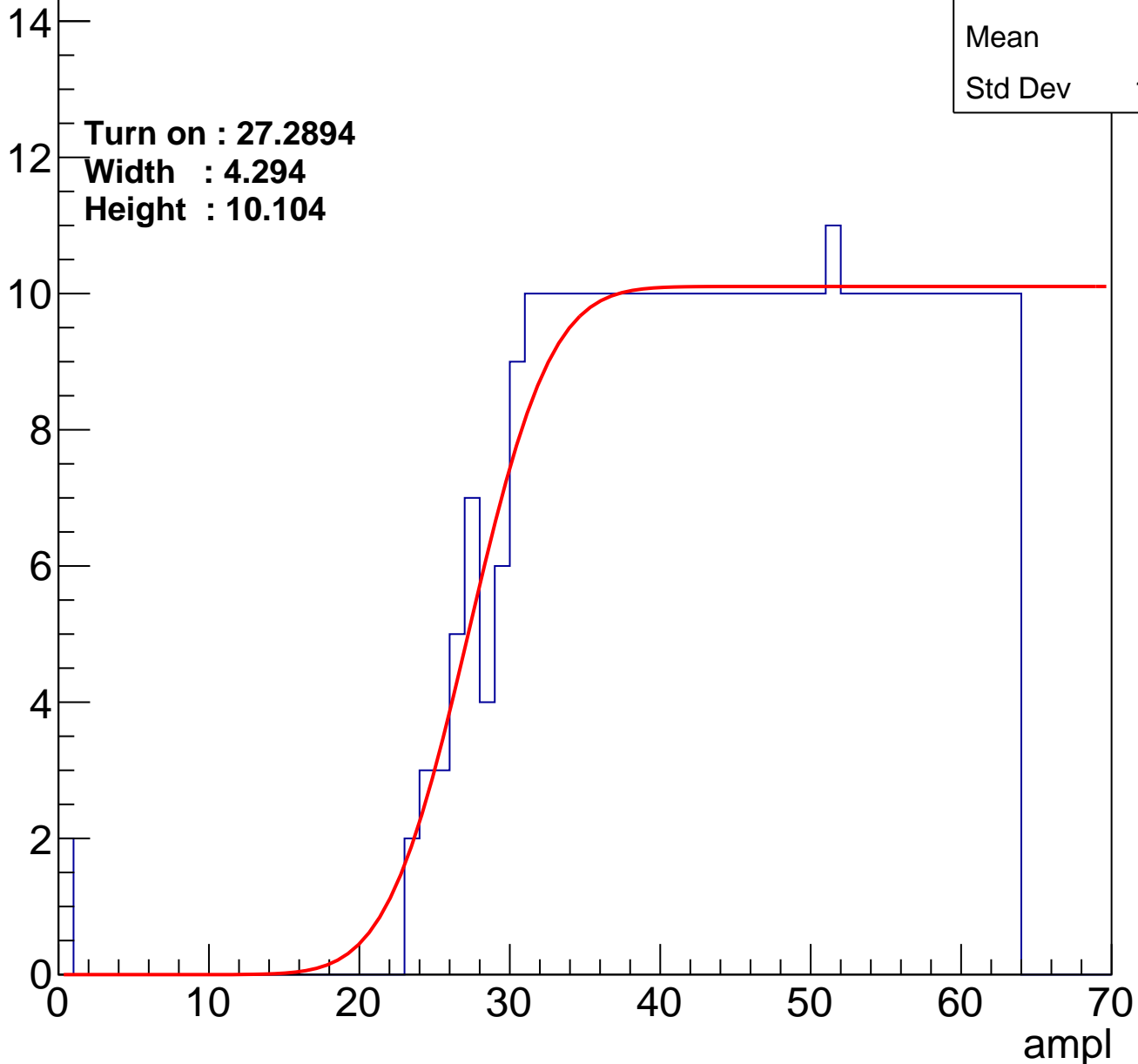
Entries	372
Mean	44.7
Std Dev	11.31

Turn on : 27.2894

Width : 4.294

Height : 10.104

Entry



B1L101S, U20-ch109

calib_packv5_042523_0143.root, FC#0, port D2

Entries	371
Mean	44.55
Std Dev	11.69

Turn on : 27.7143

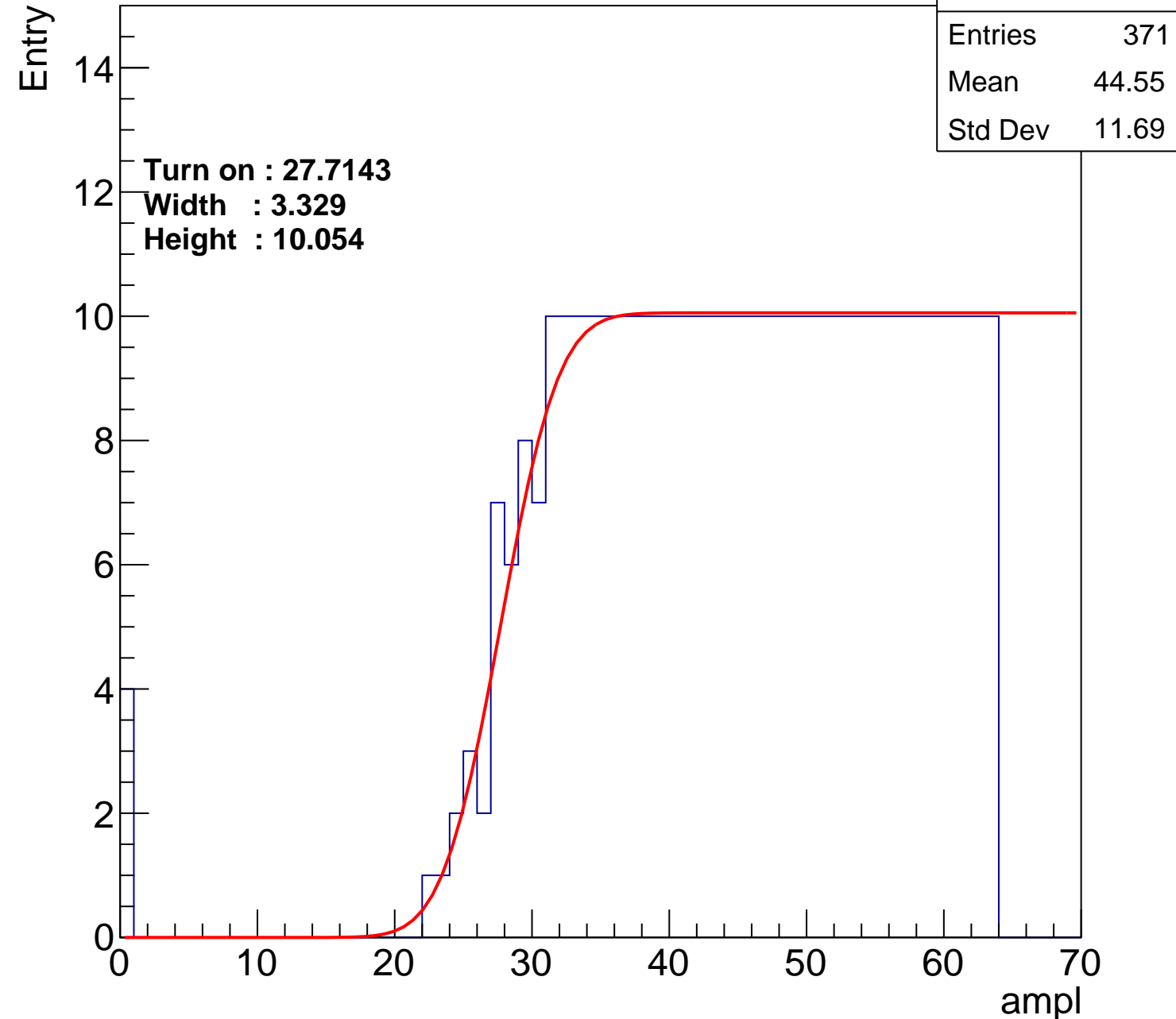
Width : 3.329

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch110

calib_packv5_042523_0143.root, FC#0, port D2

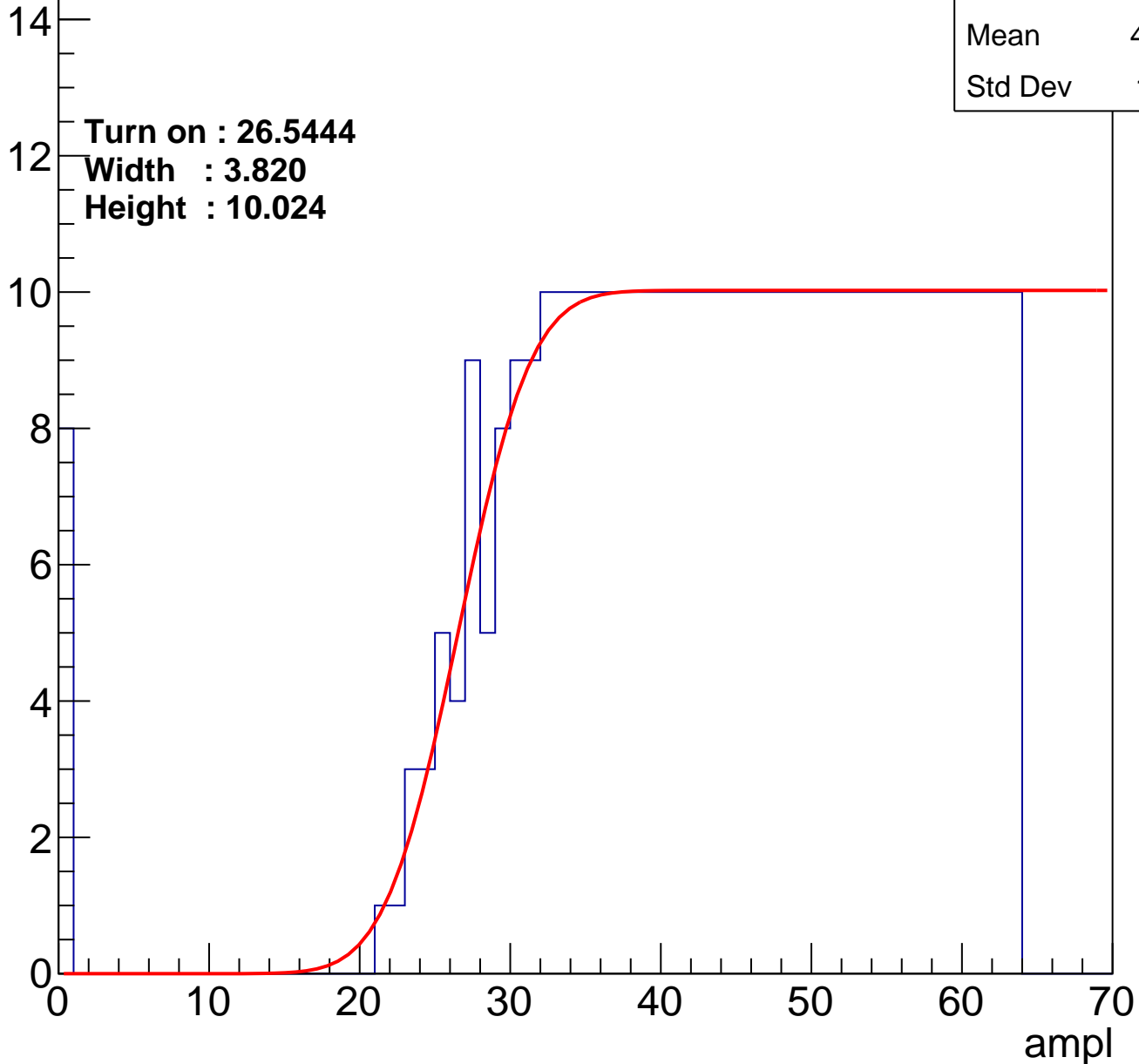
Entries	385
Mean	43.58
Std Dev	12.71

Turn on : 26.5444

Width : 3.820

Height : 10.024

Entry



B1L101S, U20-ch111

calib_packv5_042523_0143.root, FC#0, port D2

Entries	385
Mean	43.78
Std Dev	12.29

Turn on : 26.3973

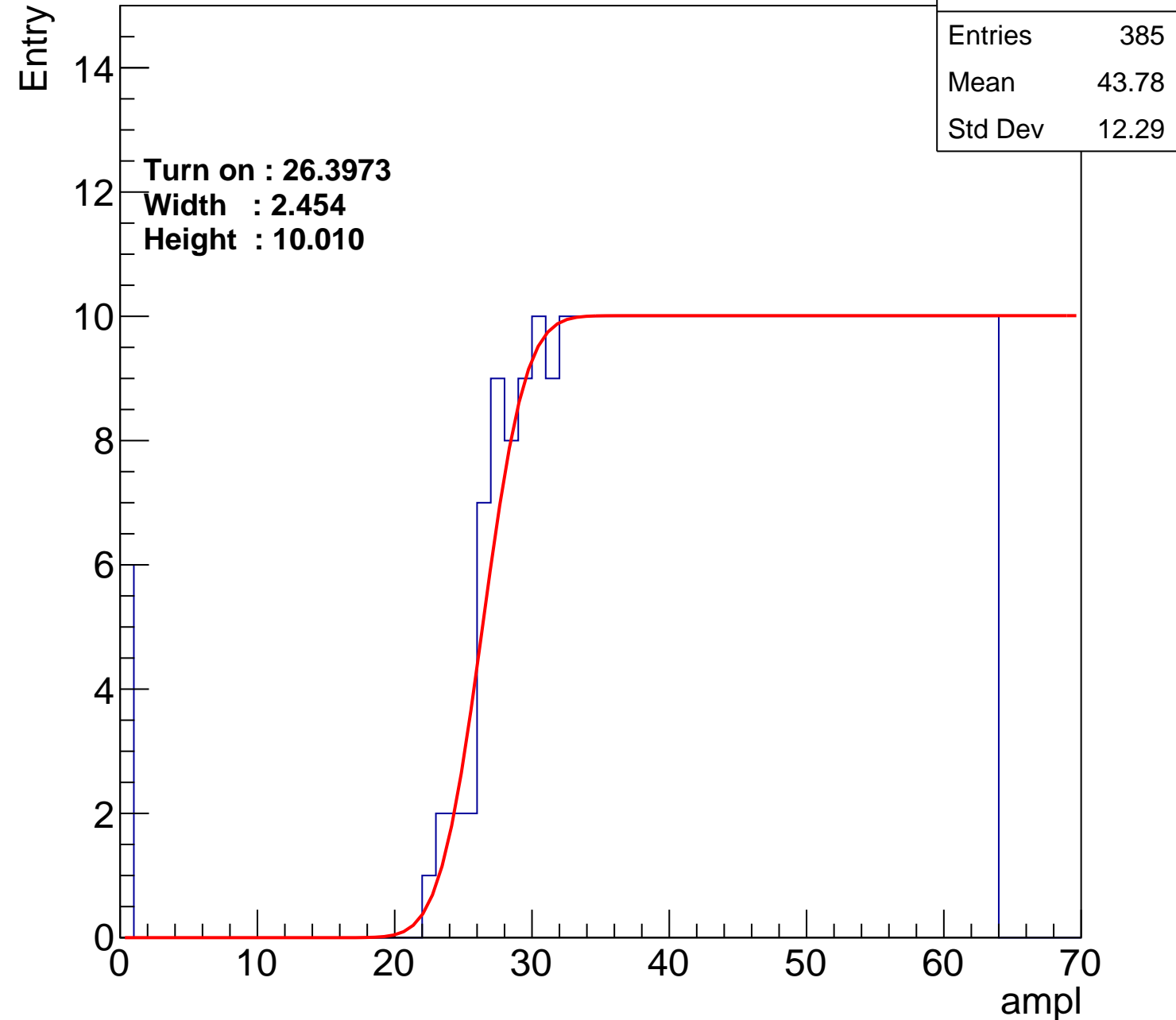
Width : 2.454

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch112

calib_packv5_042523_0143.root, FC#0, port D2

Entries	348
Mean	45.52
Std Dev	11.49

Turn on : 29.3705

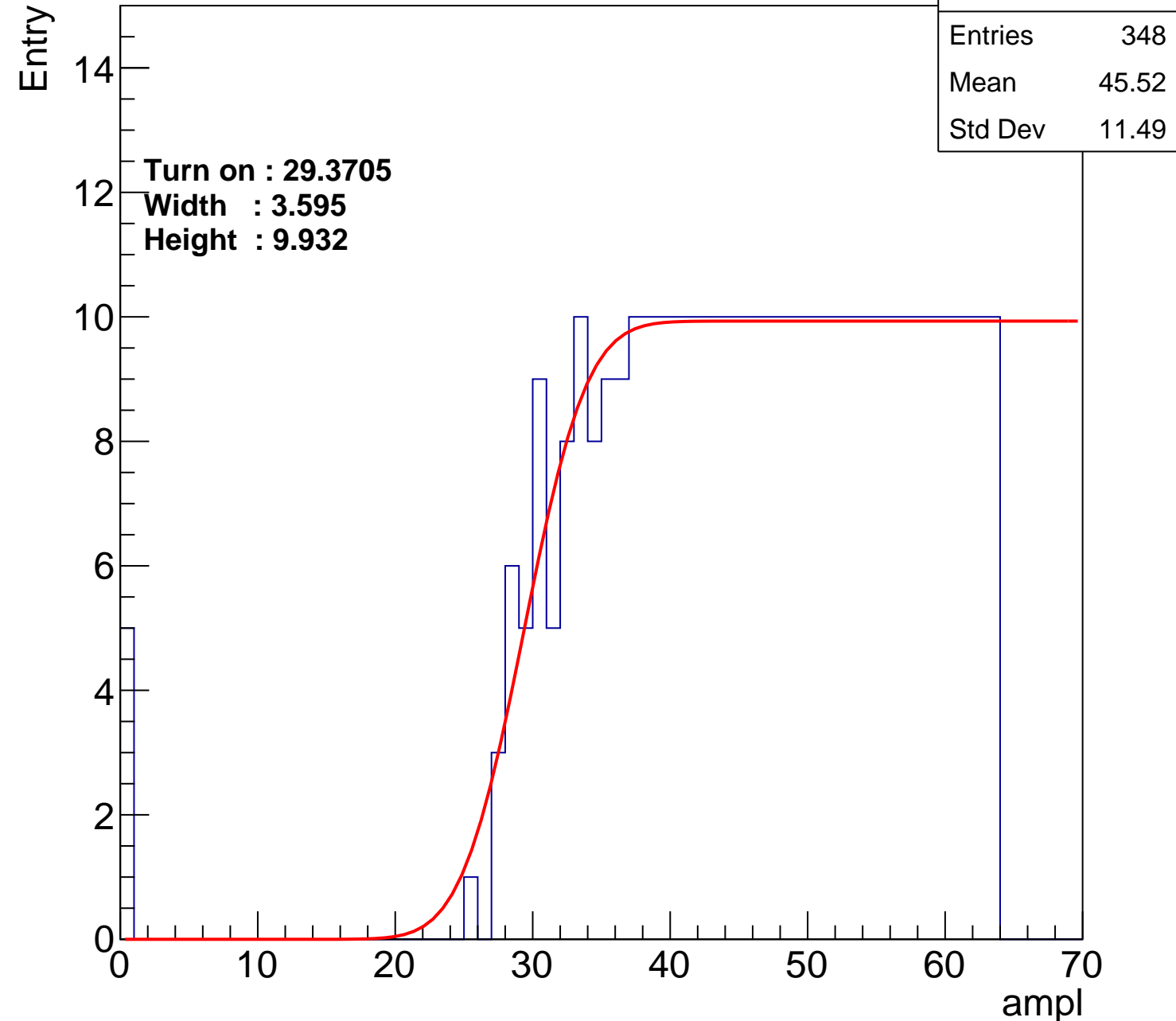
Width : 3.595

Height : 9.932

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch113

calib_packv5_042523_0143.root, FC#0, port D2

Entries	373
Mean	44.53
Std Dev	11.55

Turn on : 27.4161

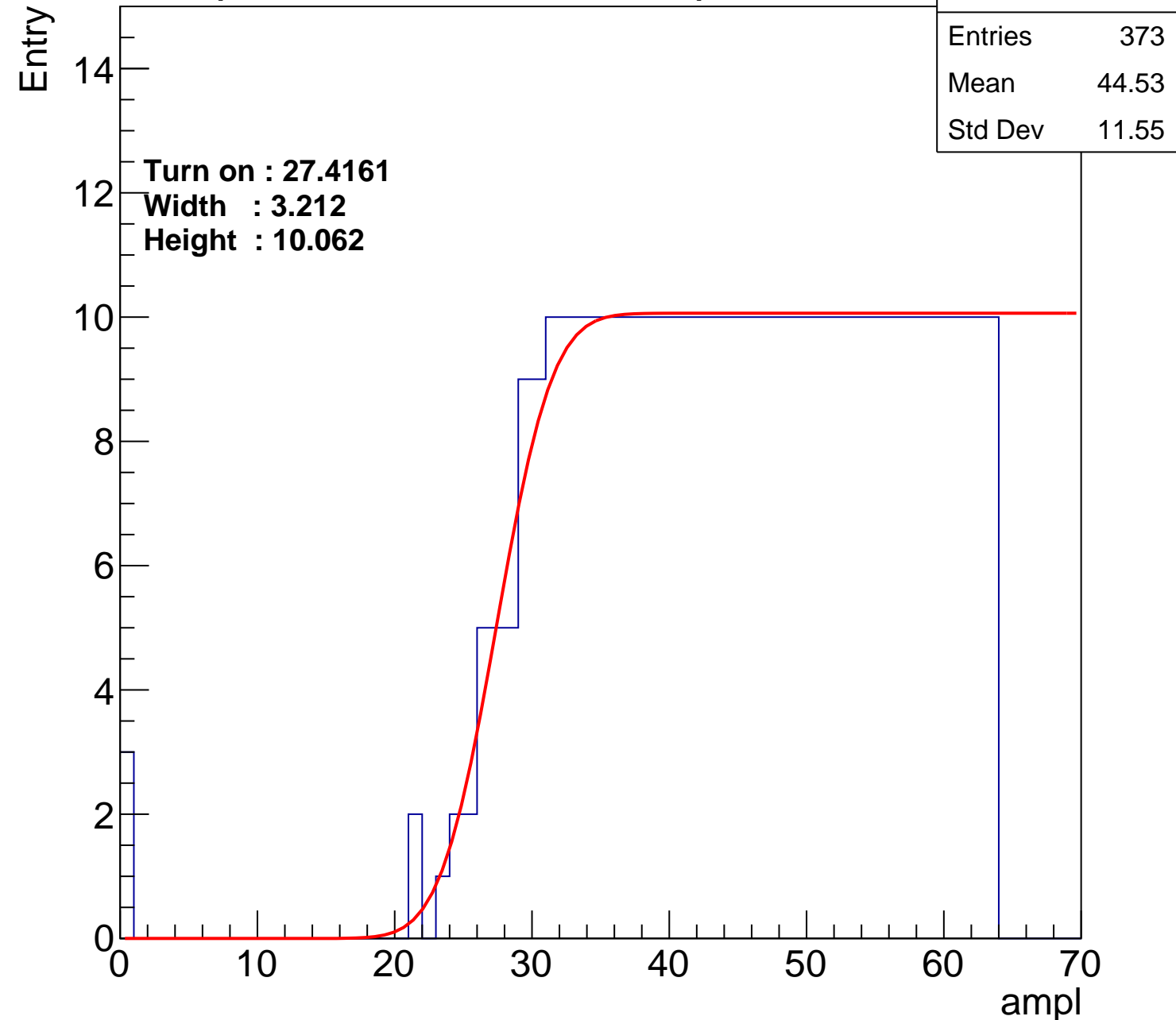
Width : 3.212

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch114

calib_packv5_042523_0143.root, FC#0, port D2

Entries	379
Mean	44.26
Std Dev	11.58

Turn on : 26.6622

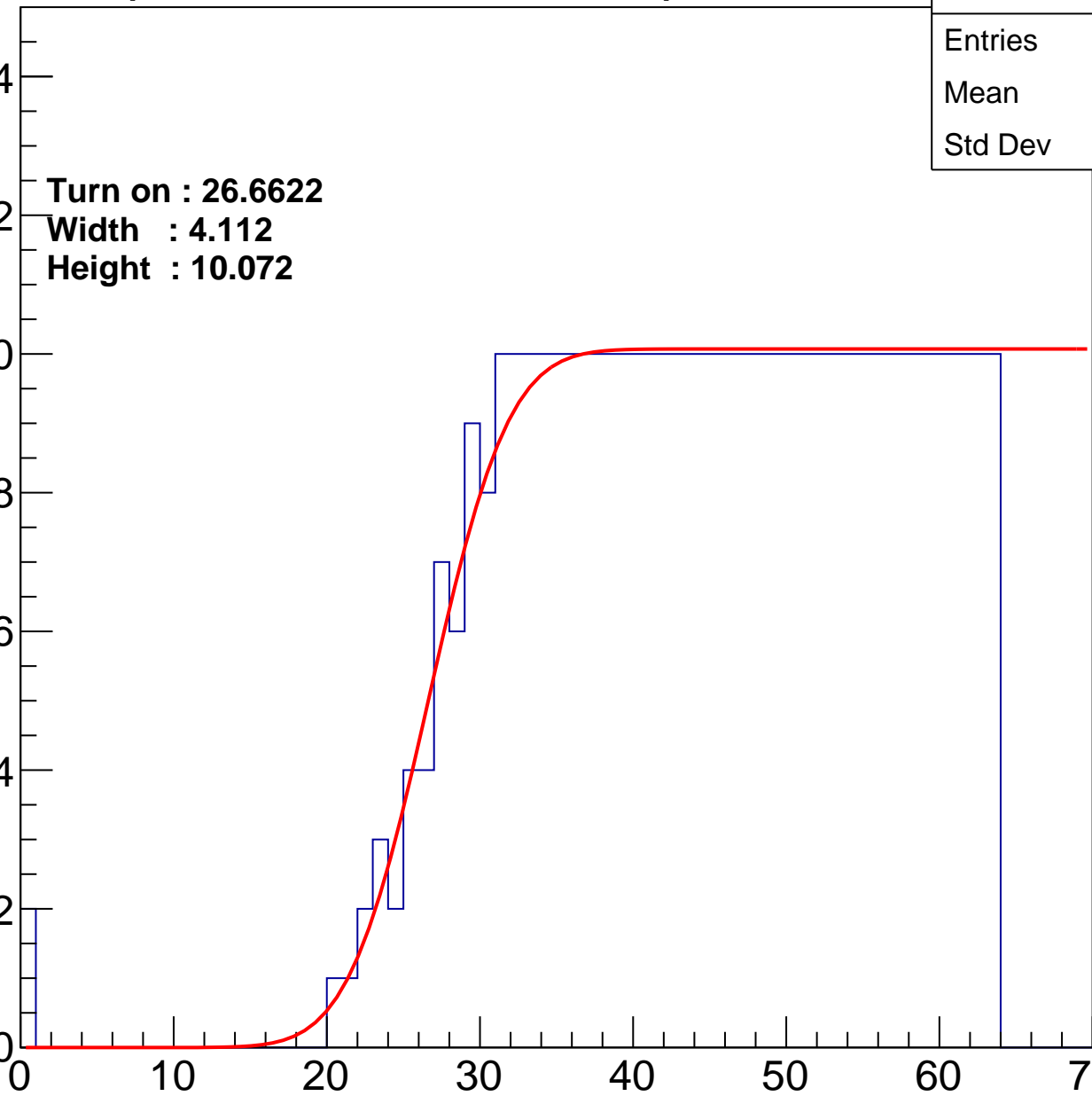
Width : 4.112

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch115

calib_packv5_042523_0143.root, FC#0, port D2

Entries	364
Mean	45.07
Std Dev	11.07

Turn on : 27.9353

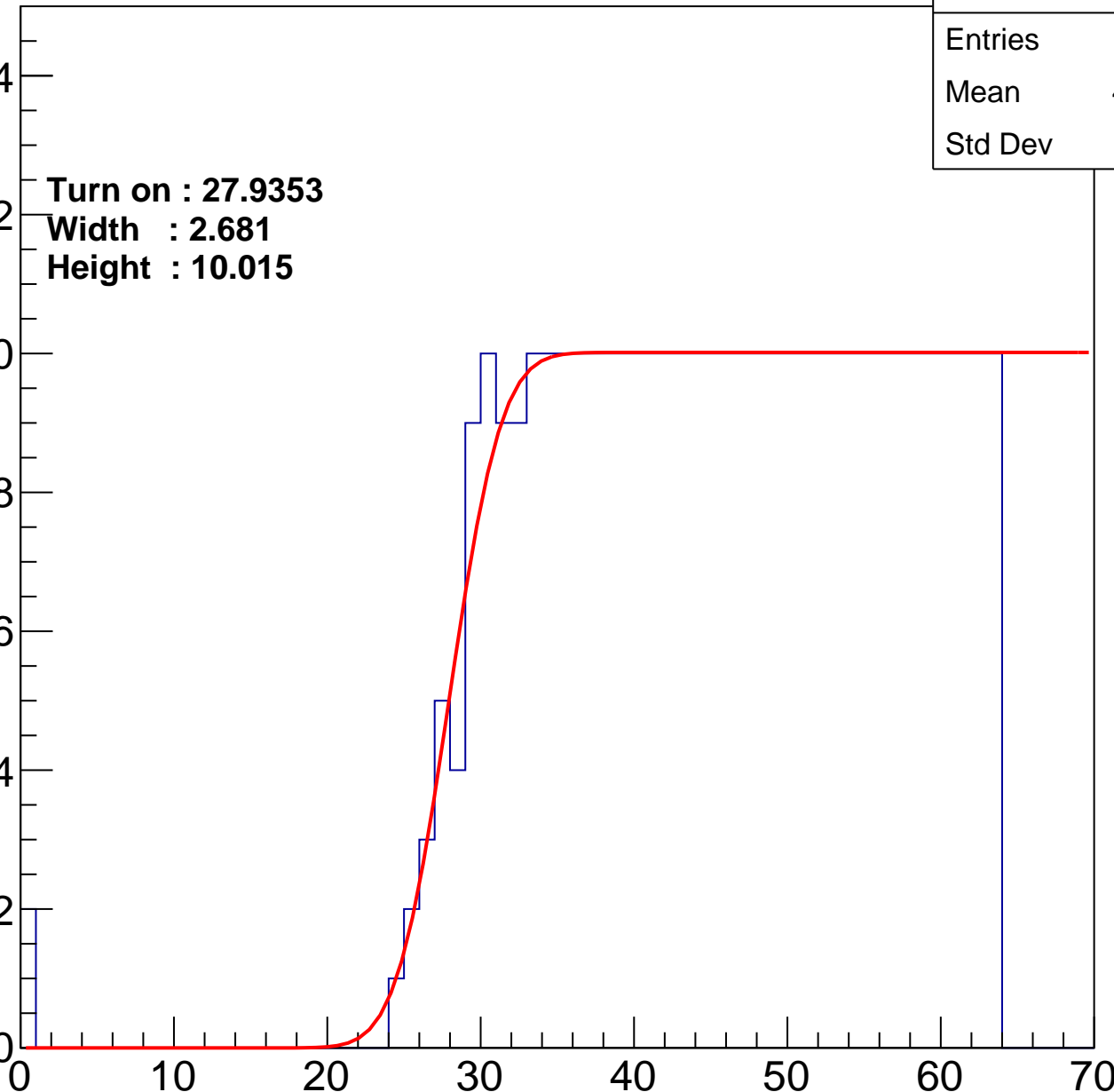
Width : 2.681

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch116

calib_packv5_042523_0143.root, FC#0, port D2

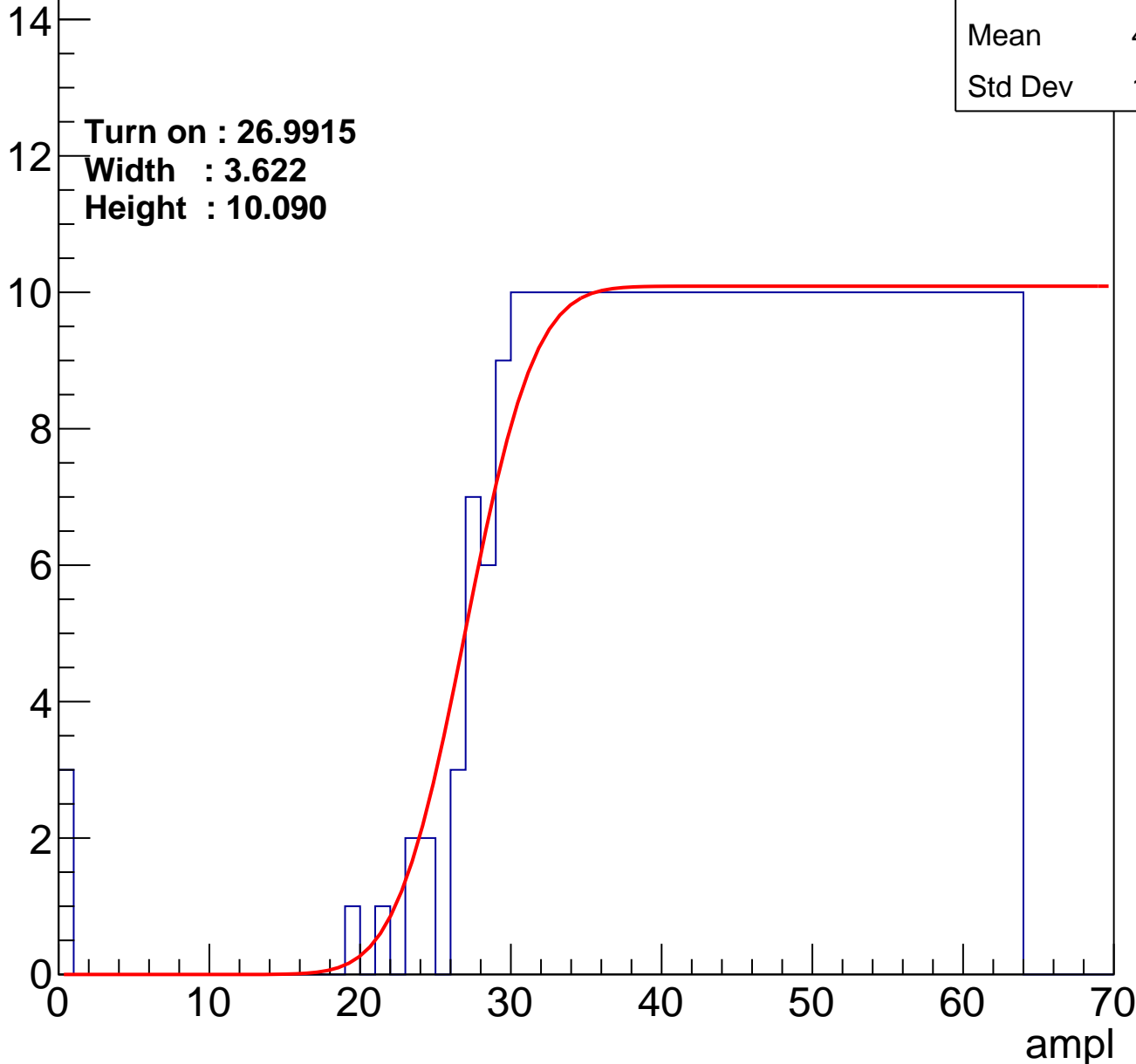
Entries	374
Mean	44.49
Std Dev	11.56

Turn on : 26.9915

Width : 3.622

Height : 10.090

Entry



B1L101S, U20-ch117

calib_packv5_042523_0143.root, FC#0, port D2

Entries	380
Mean	44.07
Std Dev	12.16

Turn on : 26.9026

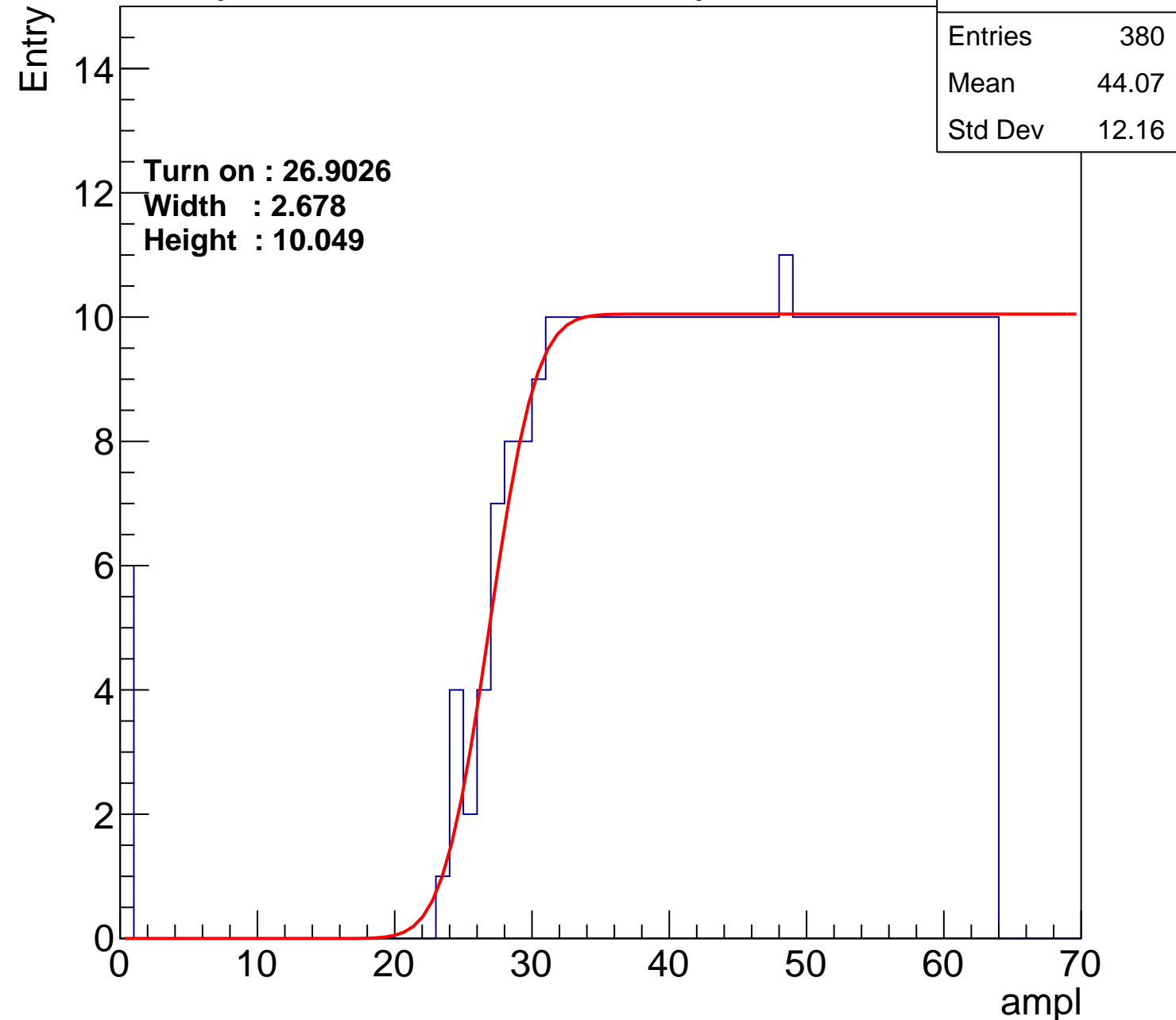
Width : 2.678

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch118

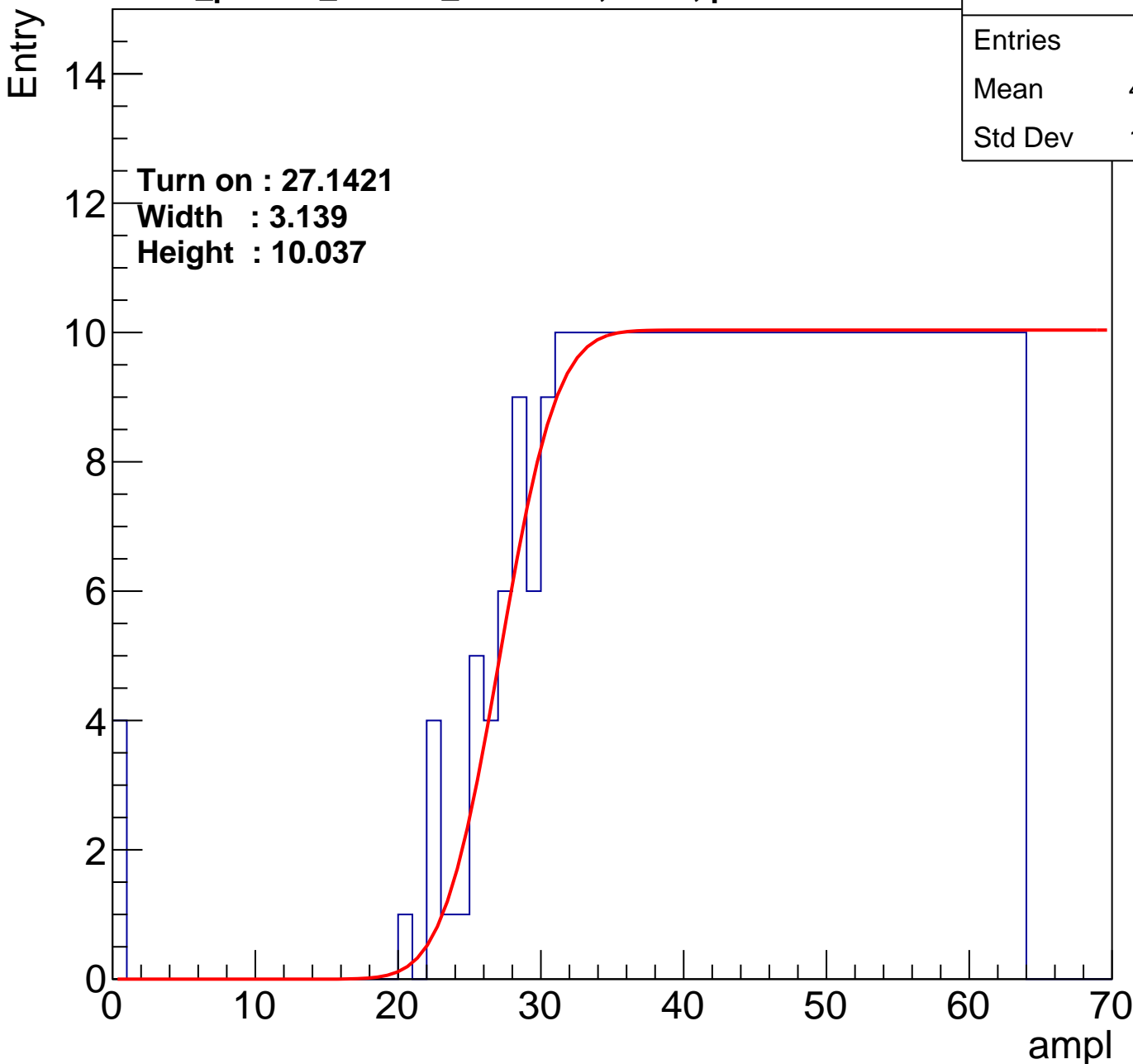
calib_packv5_042523_0143.root, FC#0, port D2

Entries	380
Mean	44.08
Std Dev	11.95

Turn on : 27.1421

Width : 3.139

Height : 10.037



B1L101S, U20-ch119

calib_packv5_042523_0143.root, FC#0, port D2

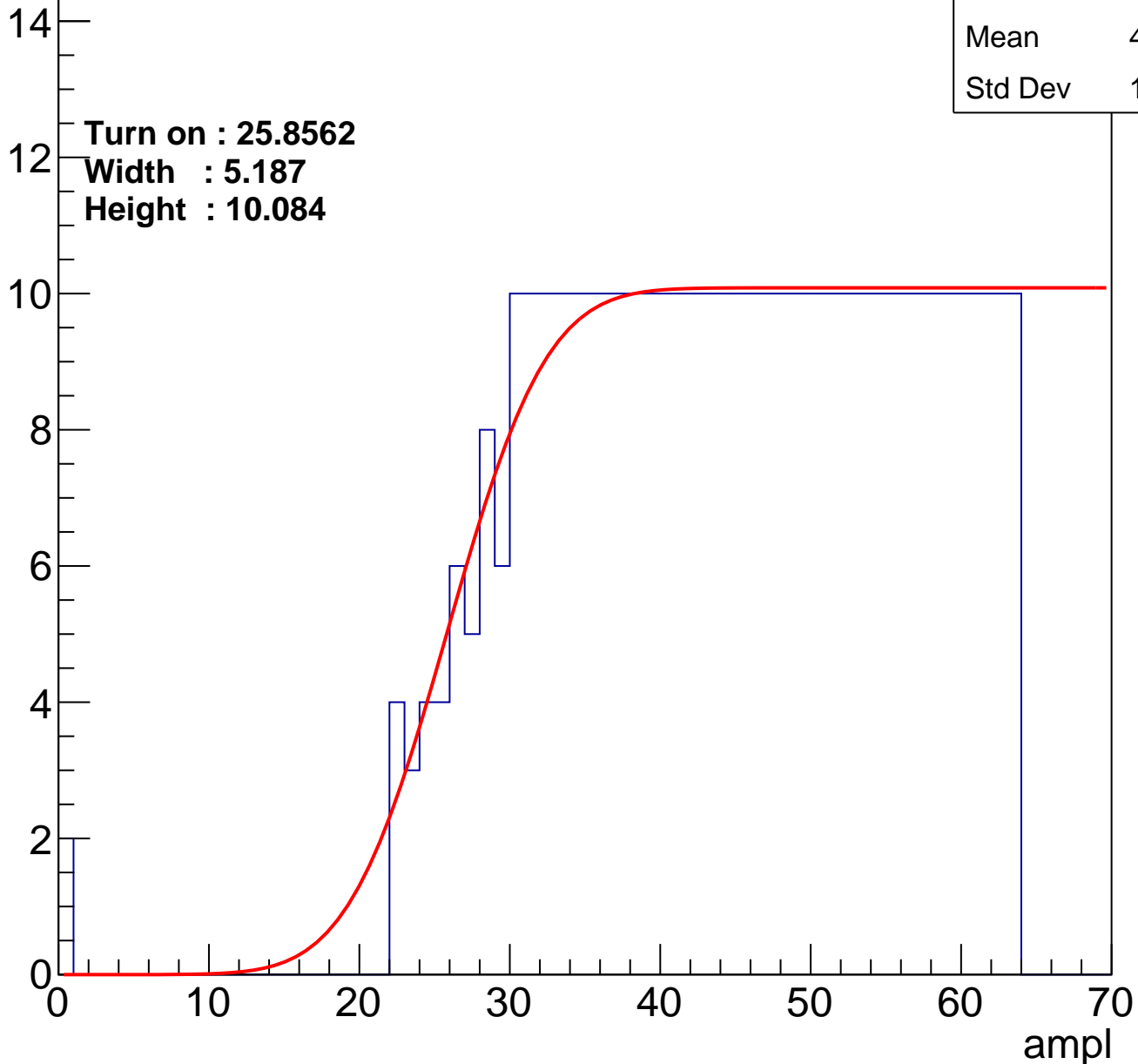
Entries	382
Mean	44.12
Std Dev	11.65

Turn on : 25.8562

Width : 5.187

Height : 10.084

Entry



B1L101S, U20-ch120

calib_packv5_042523_0143.root, FC#0, port D2

Entries	385
Mean	43.96
Std Dev	11.79

Turn on : 25.4421

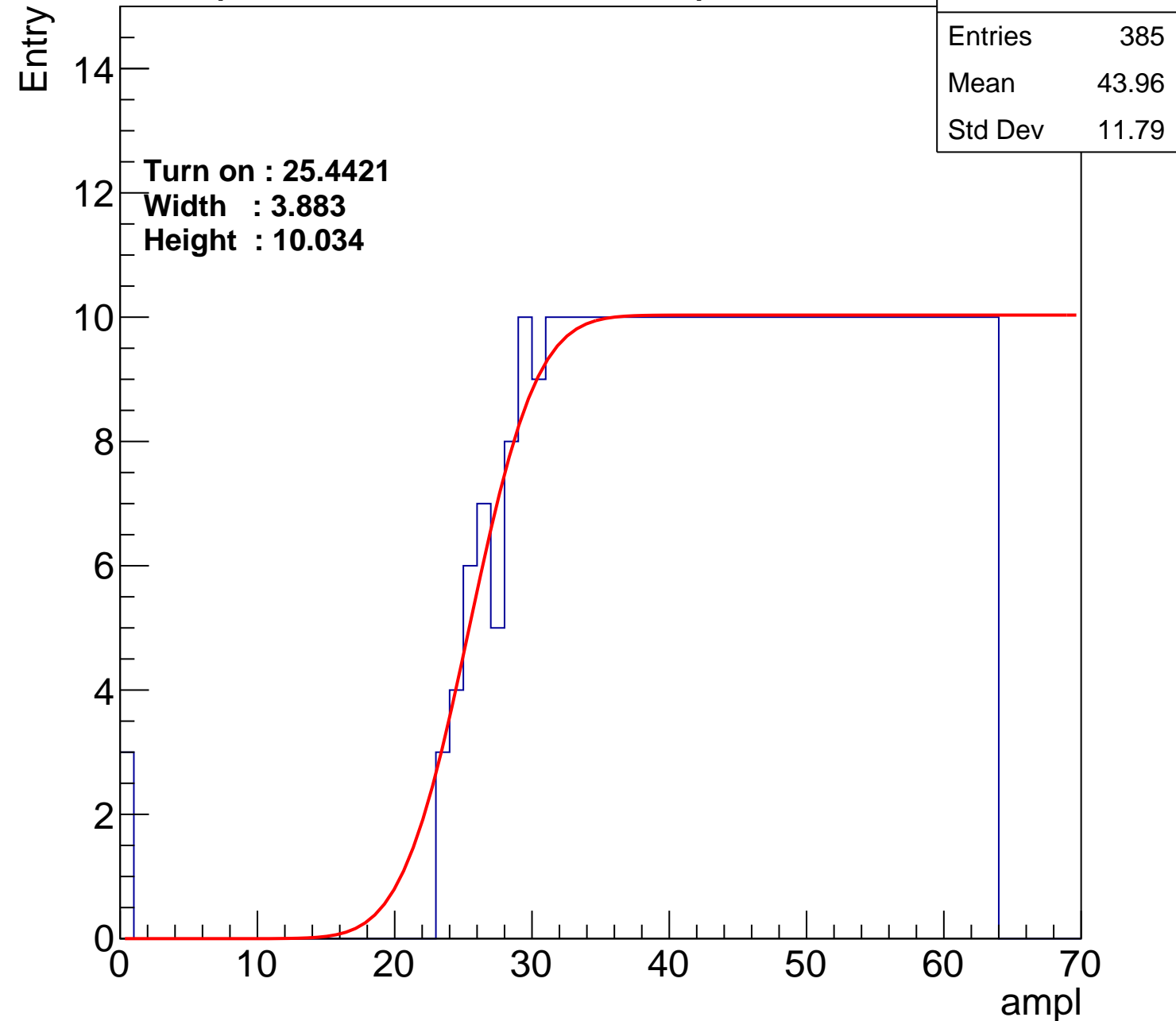
Width : 3.883

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch121

calib_packv5_042523_0143.root, FC#0, port D2

Entries	372
Mean	44.32
Std Dev	12.15

Turn on : 28.1610

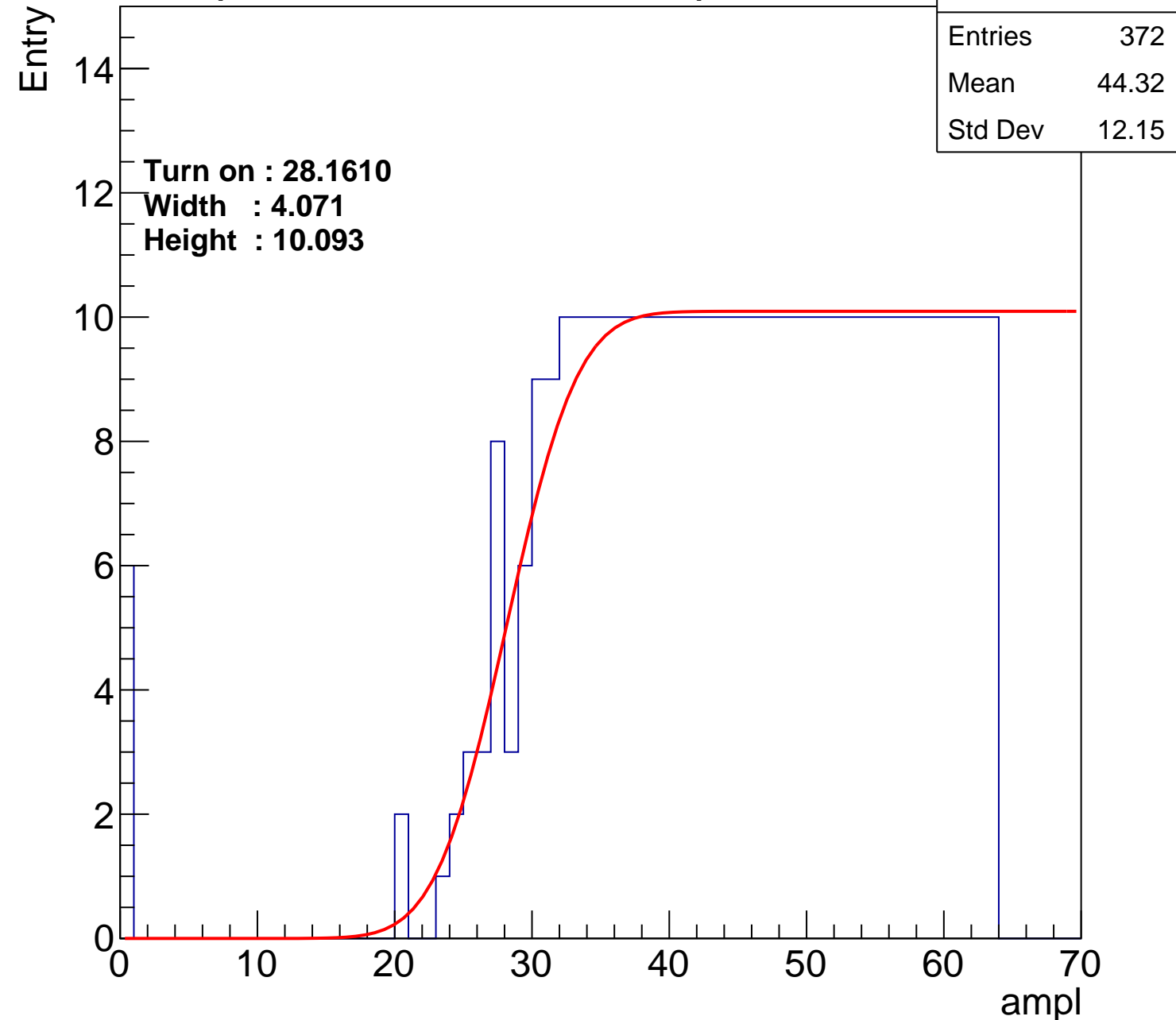
Width : 4.071

Height : 10.093

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch122

calib_packv5_042523_0143.root, FC#0, port D2

Entries	384
Mean	44.05
Std Dev	11.64

Turn on : 26.0527

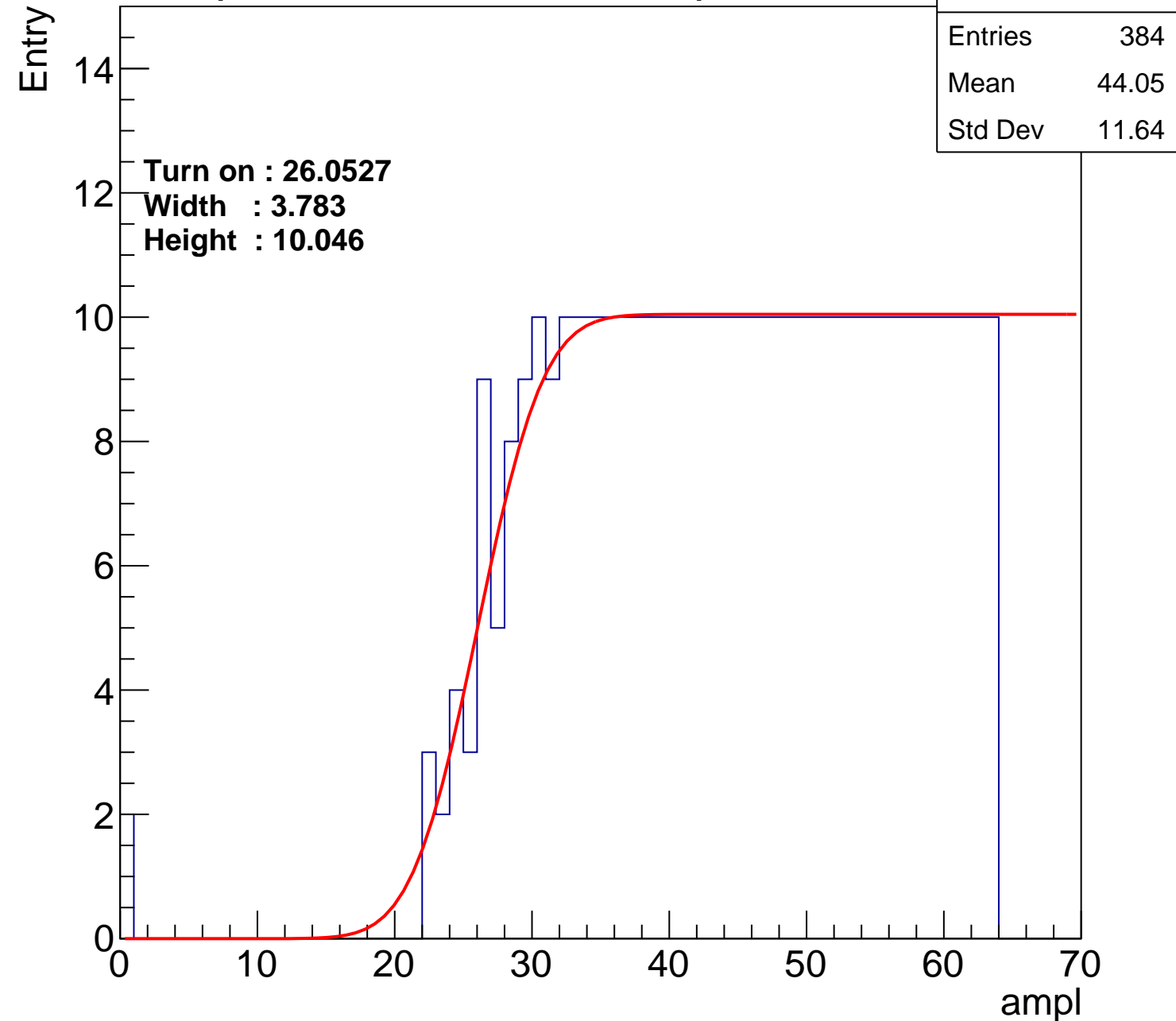
Width : 3.783

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch123

calib_packv5_042523_0143.root, FC#0, port D2

Entries	369
Mean	44.8
Std Dev	11.34

Turn on : 28.2361

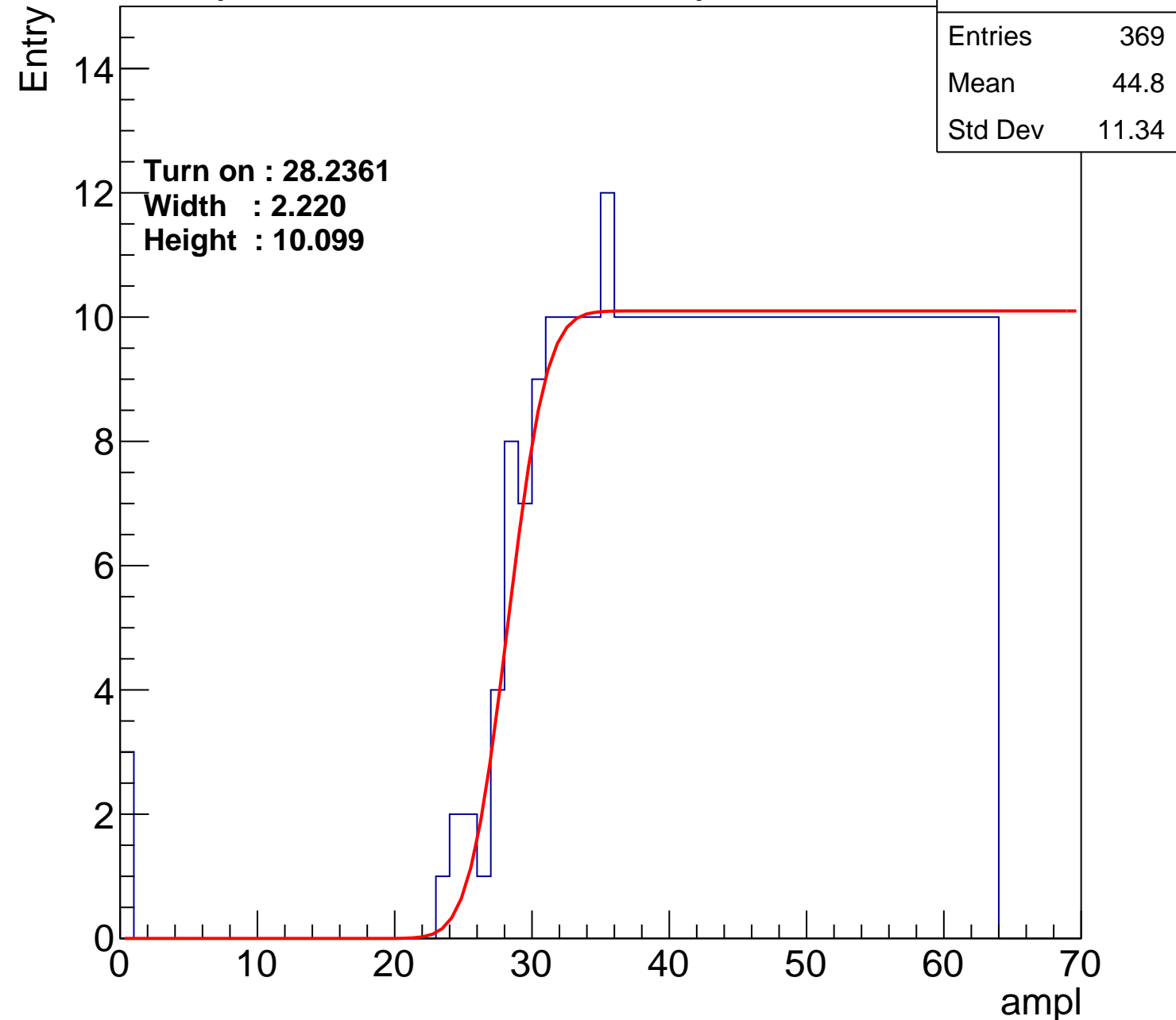
Width : 2.220

Height : 10.099

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch124

calib_packv5_042523_0143.root, FC#0, port D2

Entries	378
Mean	44.33
Std Dev	11.5

Turn on : 26.3067

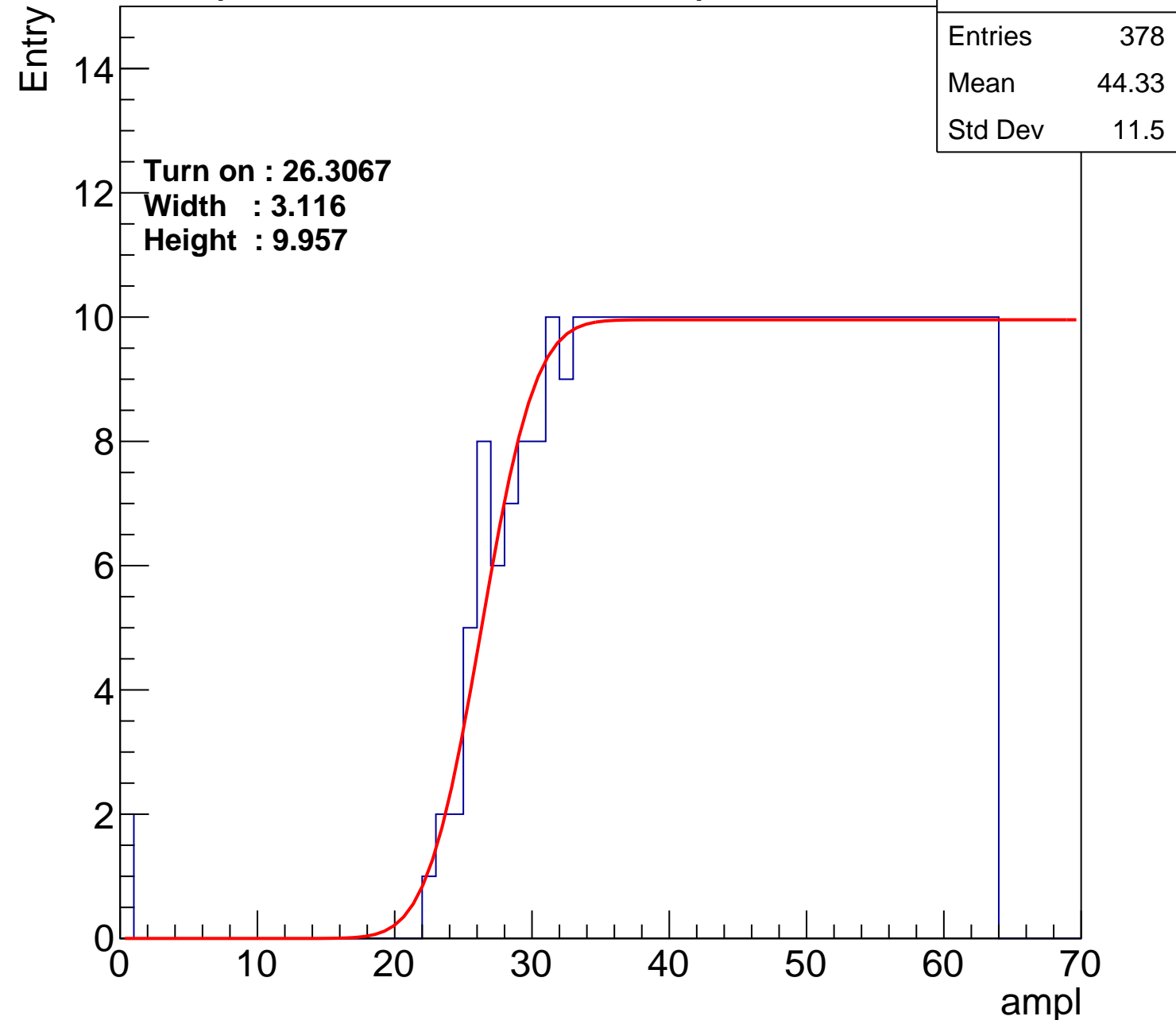
Width : 3.116

Height : 9.957

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch125

calib_packv5_042523_0143.root, FC#0, port D2

Entries	363
Mean	45.09
Std Dev	11.1

Turn on : 28.3471

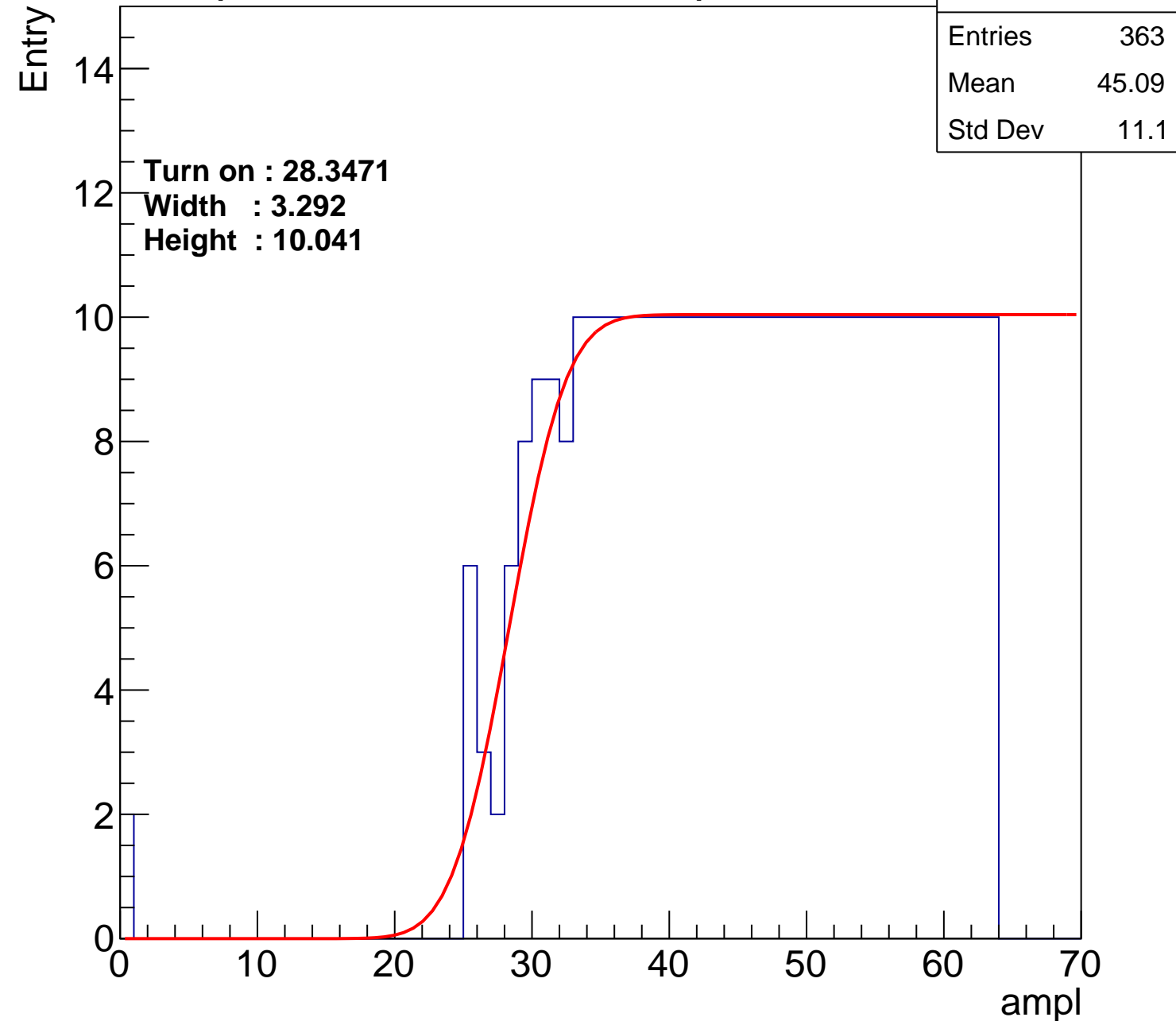
Width : 3.292

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L101S, U20-ch126

calib_packv5_042523_0143.root, FC#0, port D2

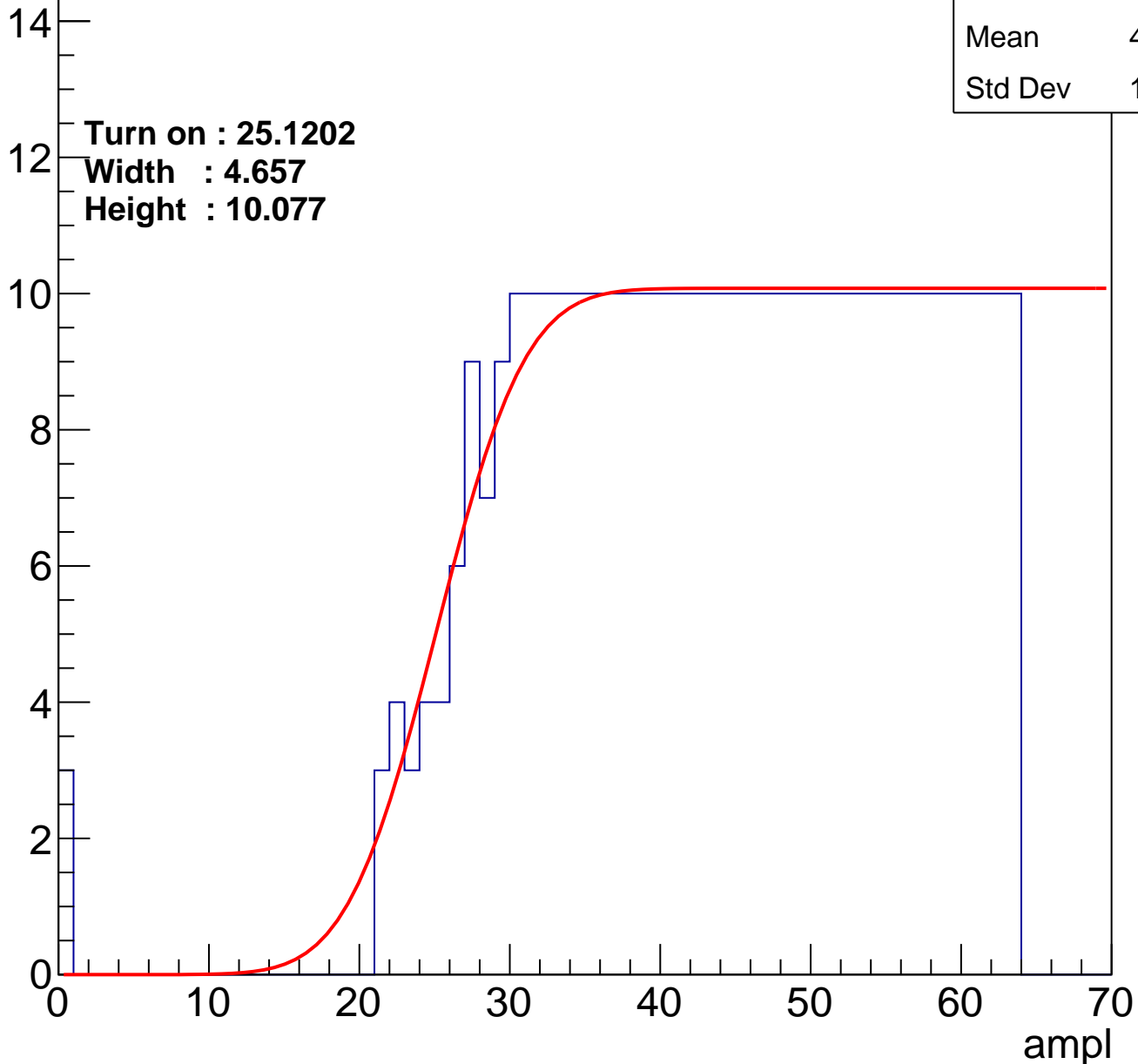
Entries	392
Mean	43.58
Std Dev	12.04

Turn on : 25.1202

Width : 4.657

Height : 10.077

Entry



B1L101S, U20-ch127

calib_packv5_042523_0143.root, FC#0, port D2

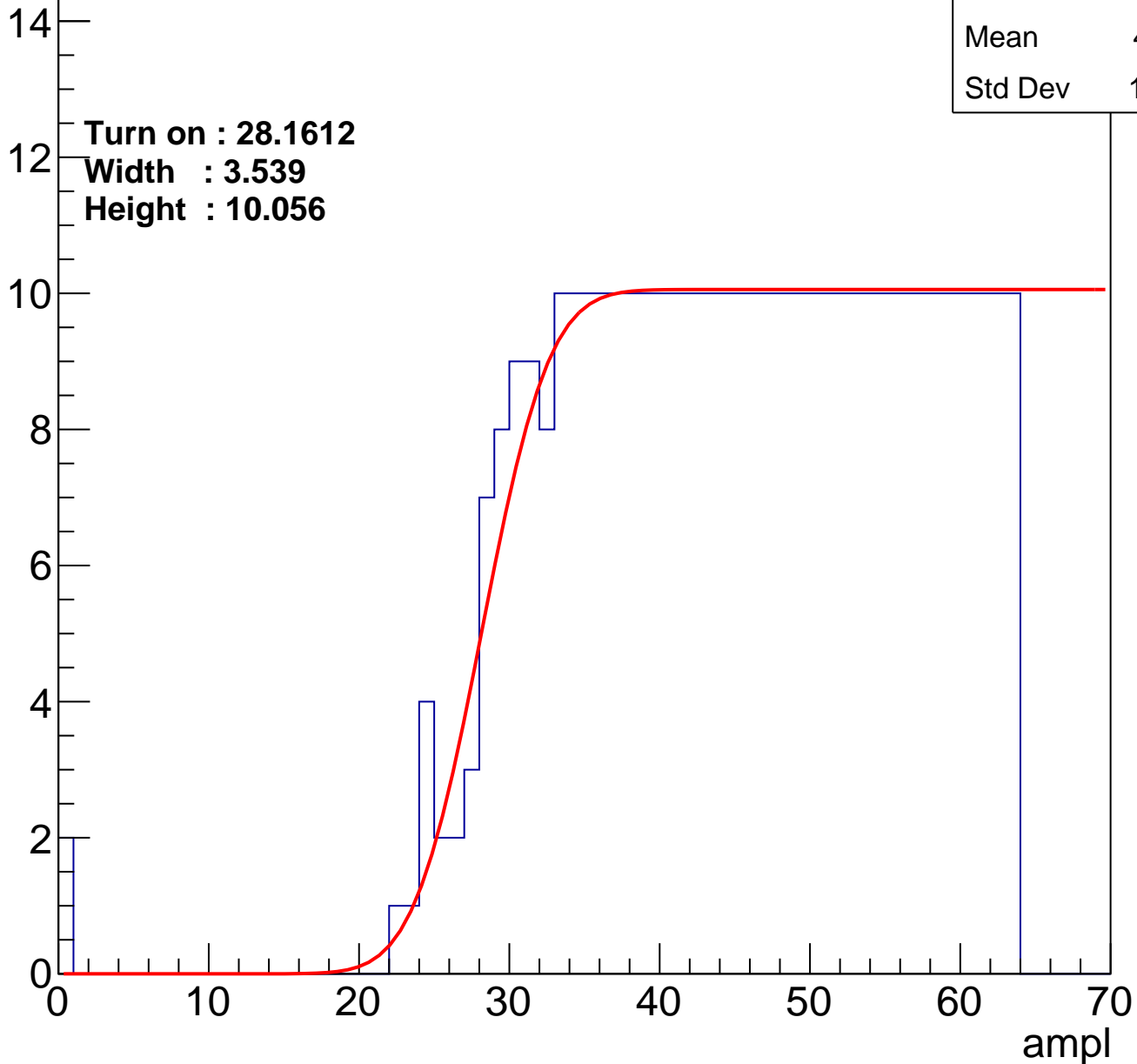
Entries	366
Mean	44.91
Std Dev	11.23

Turn on : 28.1612

Width : 3.539

Height : 10.056

Entry



B1L101S, U20-ch127

calib_packv5_042523_0143.root, FC#0, port D2

Entries	366
Mean	44.91
Std Dev	11.23

Turn on : 28.1612

Width : 3.539

Height : 10.056

Entry

