

B1L103S, U24-ch0

calib_packv5_041523_1651.root, FC#0, port C2

Entries	476
Mean	37.12
Std Dev	18.37

Turn on : 23.2198

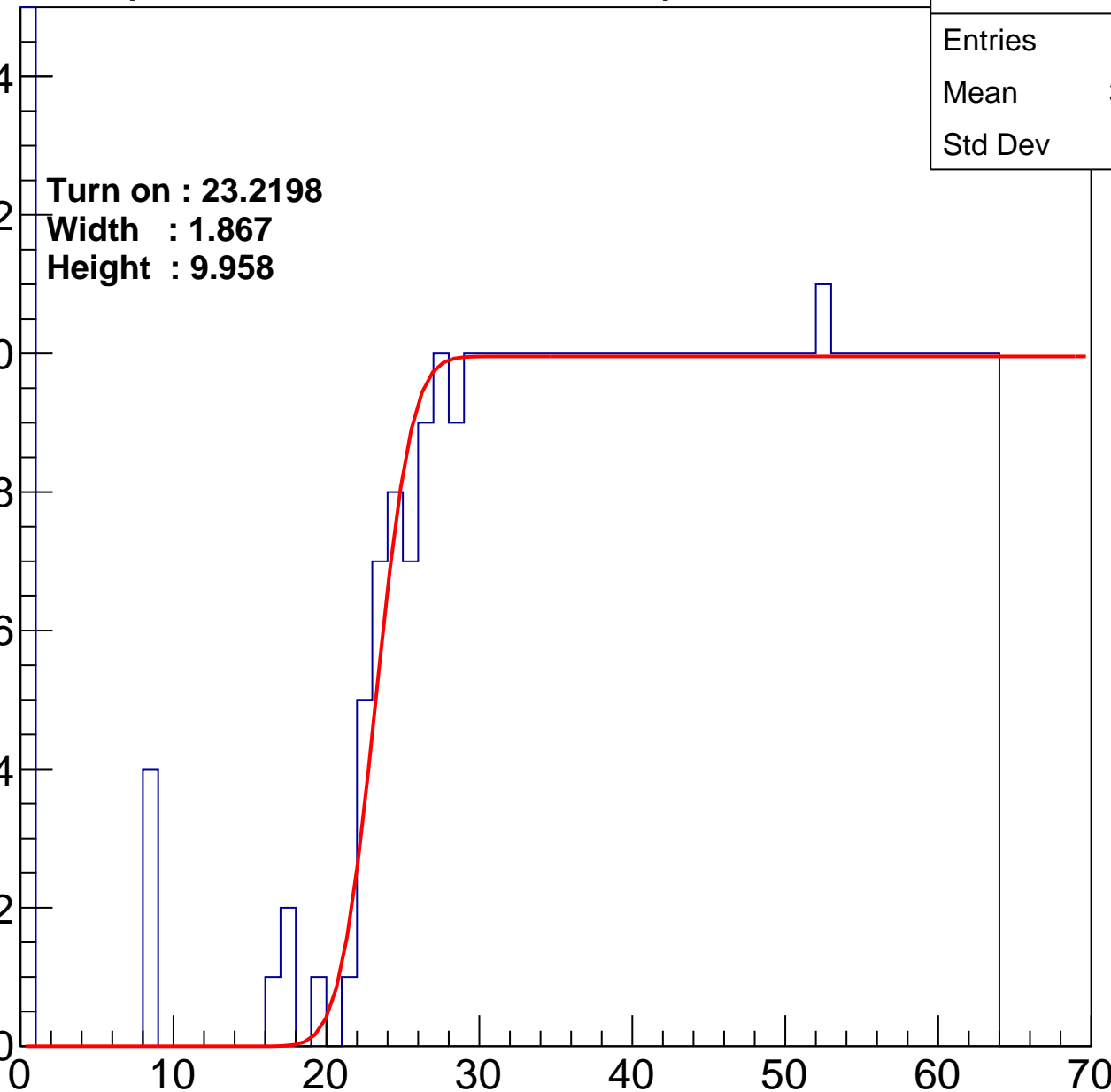
Width : 1.867

Height : 9.958

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch1

calib_packv5_041523_1651.root, FC#0, port C2

Entries	409
Mean	40.35
Std Dev	17.17

Turn on : 27.6118

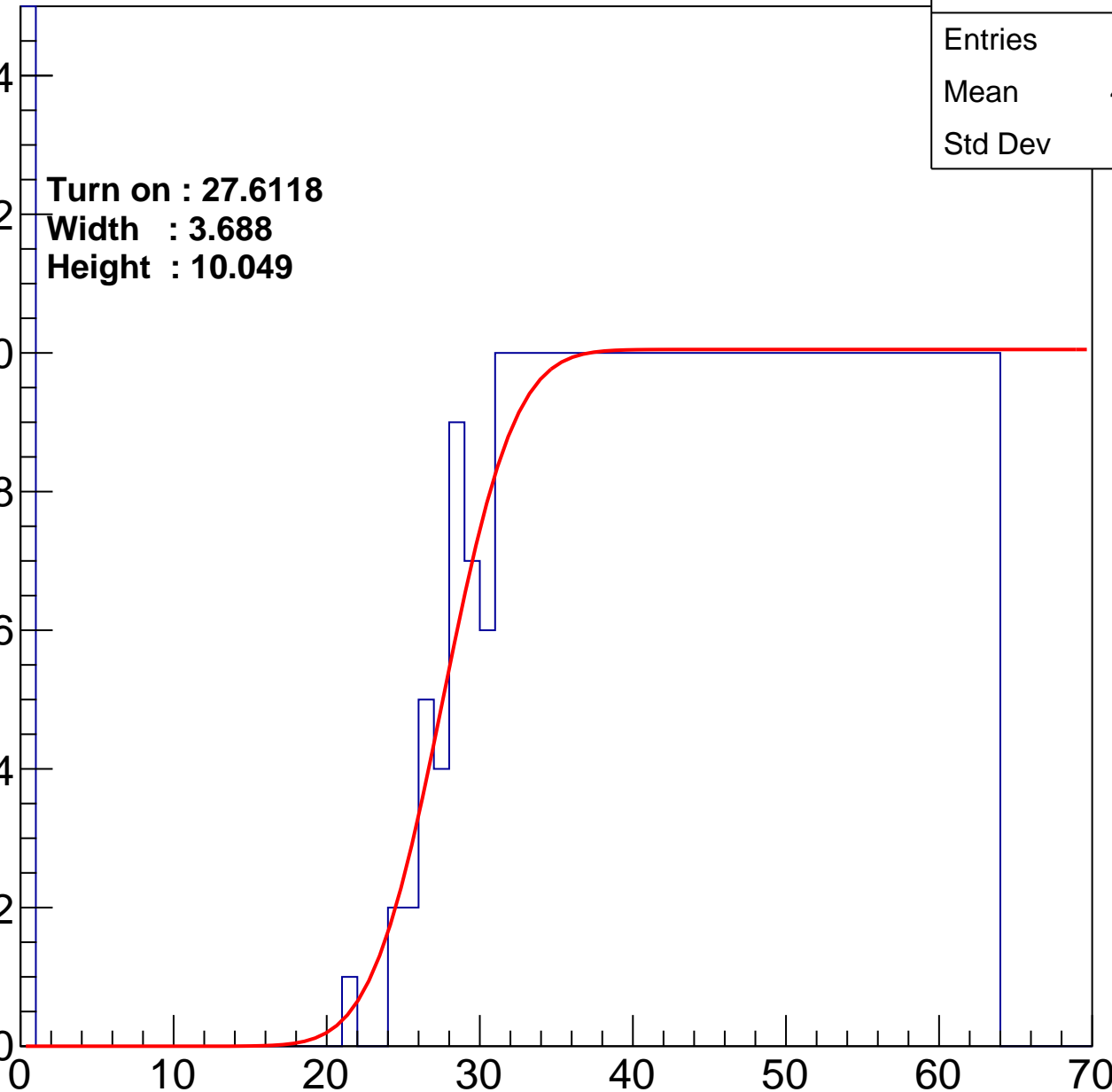
Width : 3.688

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch2

calib_packv5_041523_1651.root, FC#0, port C2

Entries	462
Mean	38.06
Std Dev	17.67

Turn on : 23.1194

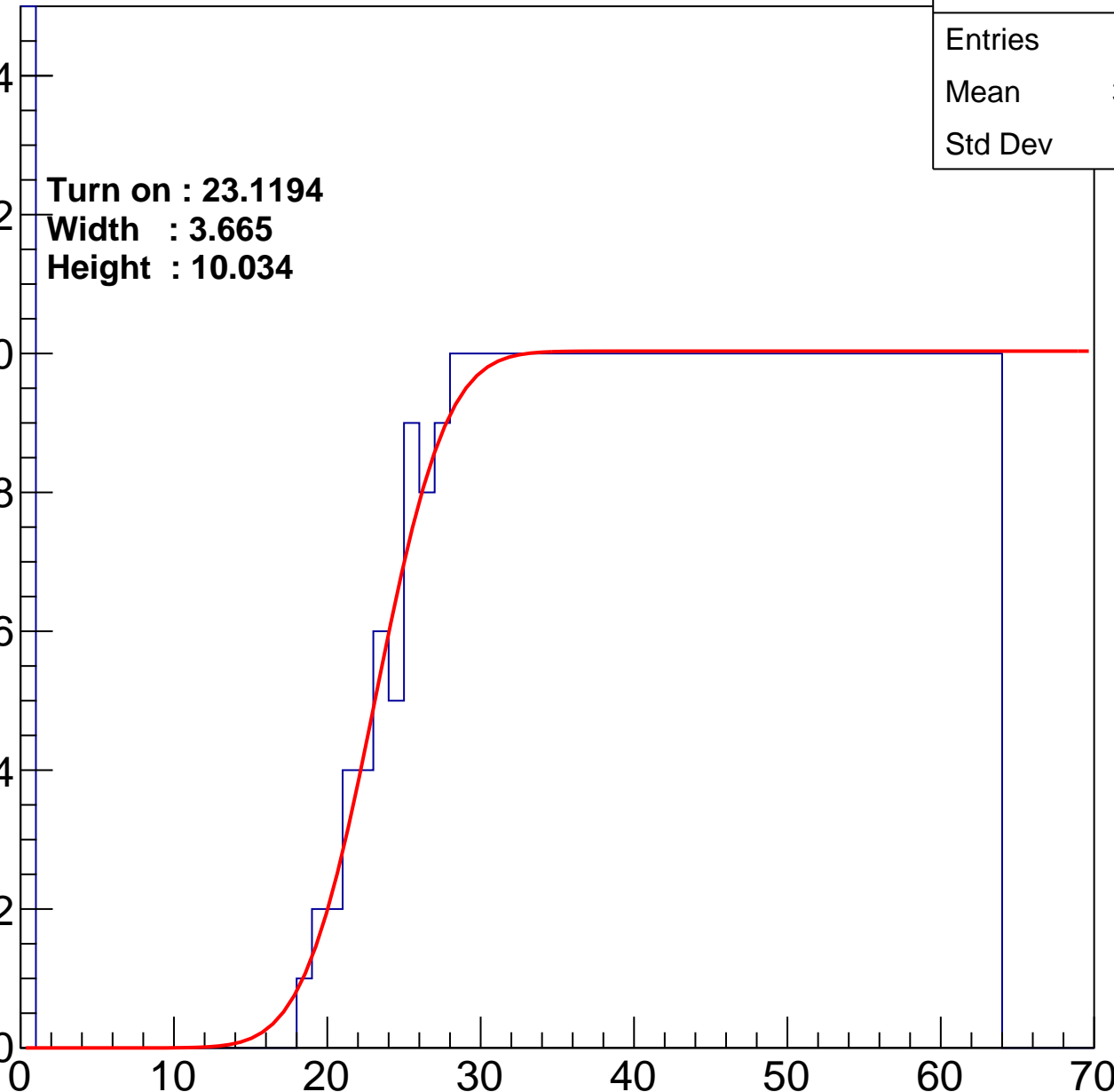
Width : 3.665

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch3

calib_packv5_041523_1651.root, FC#0, port C2

Entries	397
Mean	41.13
Std Dev	16.68

Turn on : 27.9017

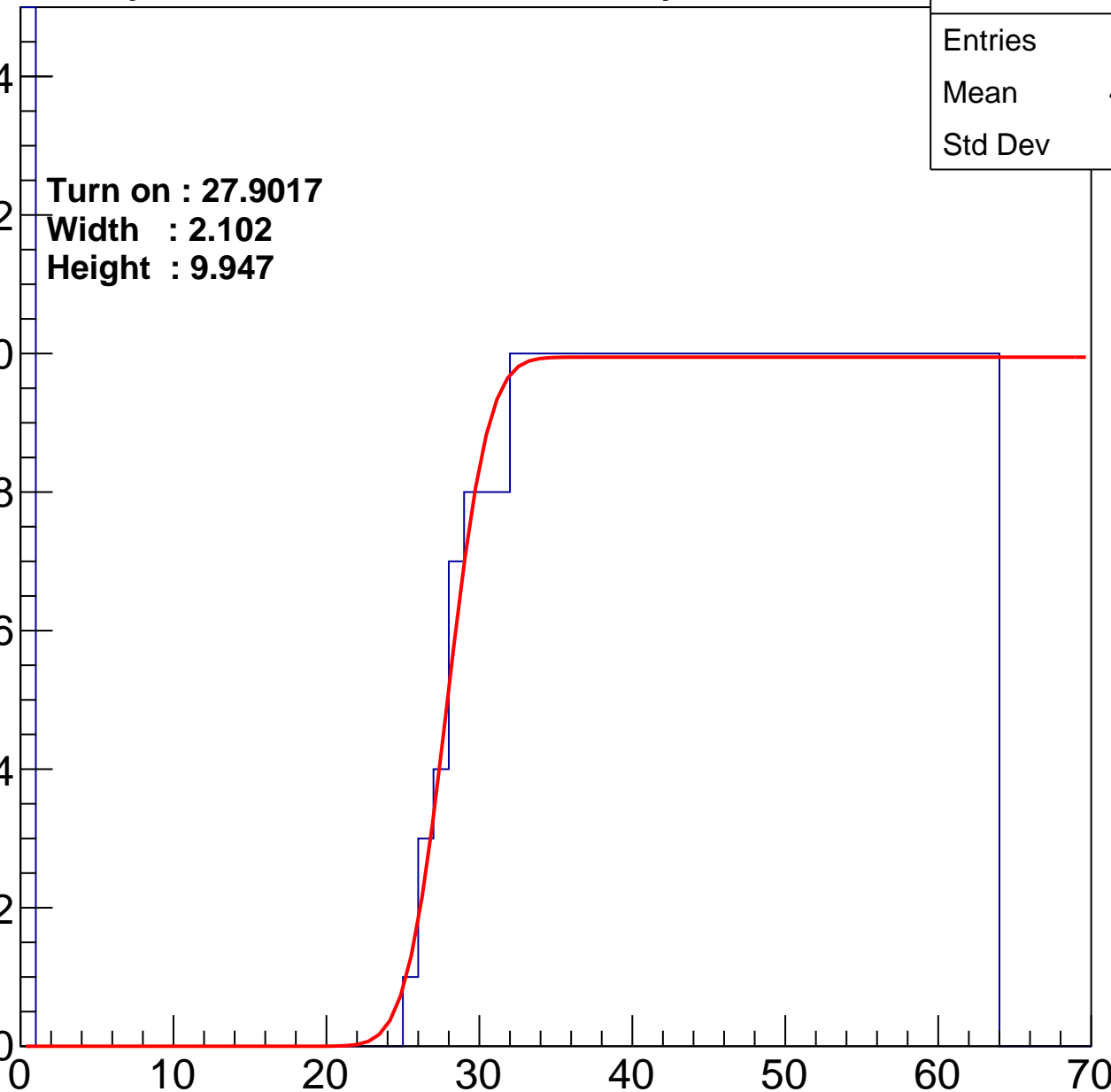
Width : 2.102

Height : 9.947

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch4

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	38.51
Std Dev	18.29

Turn on : 26.0258

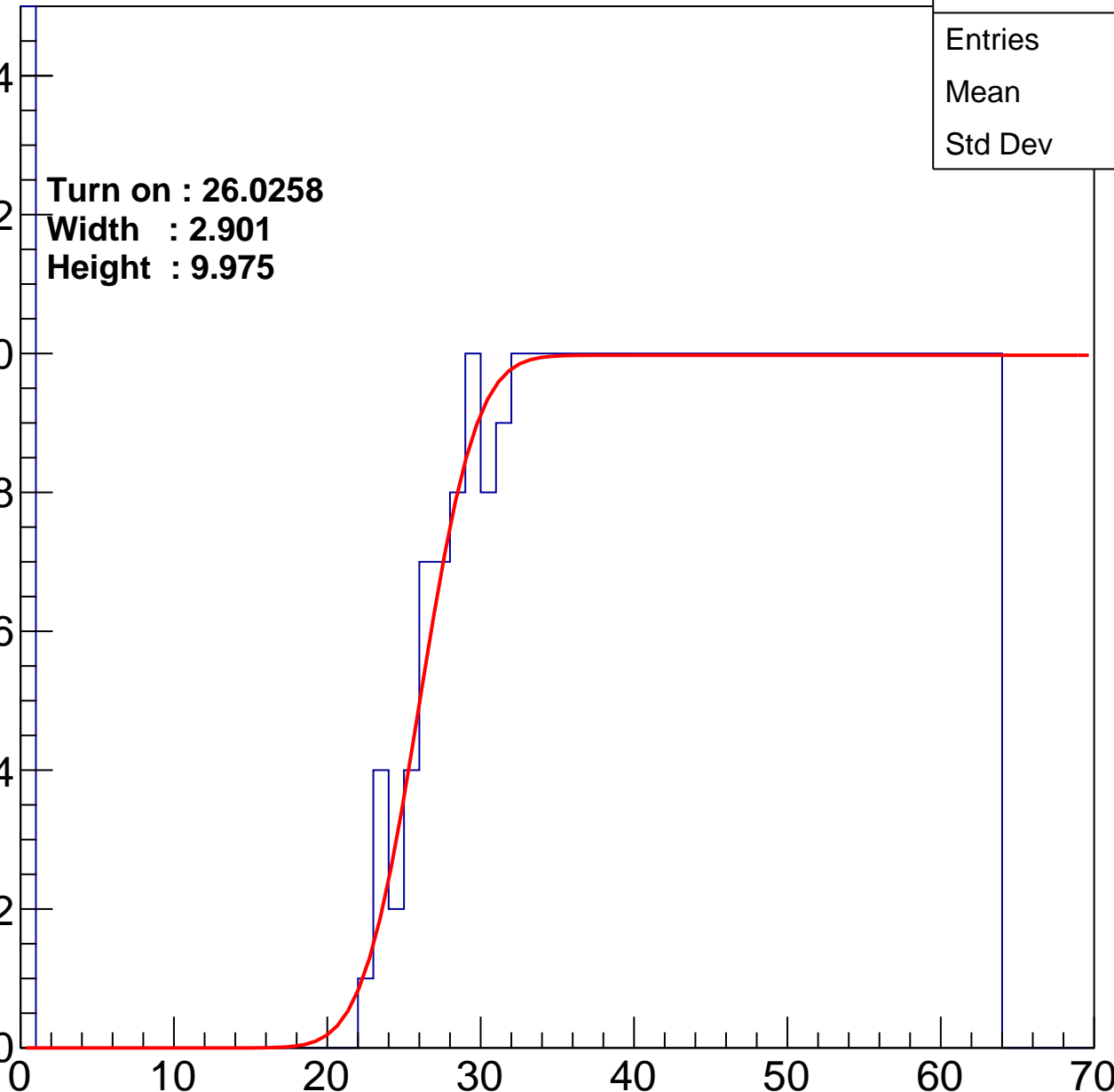
Width : 2.901

Height : 9.975

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch5

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	40.15
Std Dev	16.36

Turn on : 25.2244

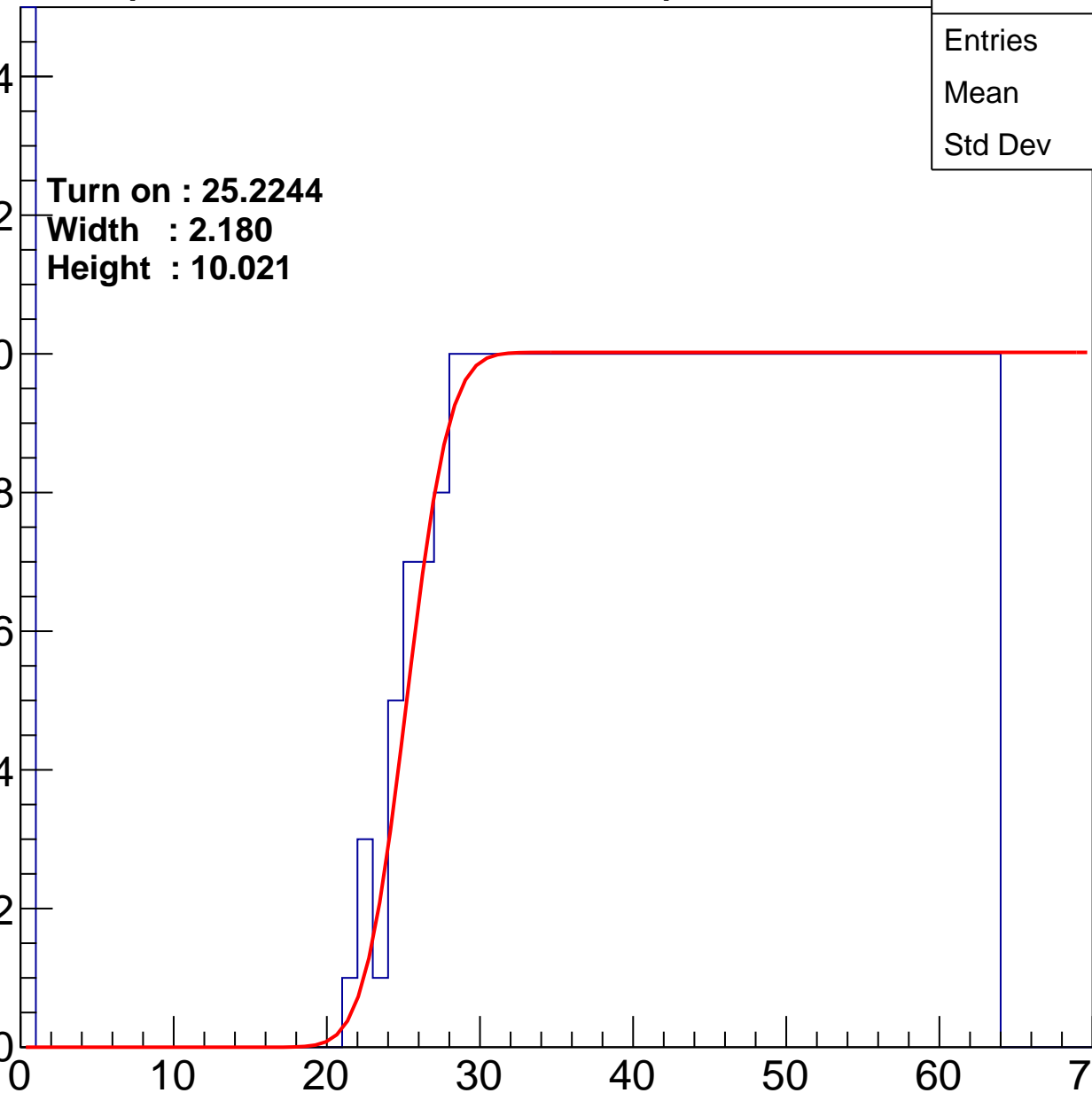
Width : 2.180

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch6

calib_packv5_041523_1651.root, FC#0, port C2

Entries	460
Mean	37.7
Std Dev	18.31

Turn on : 24.4083

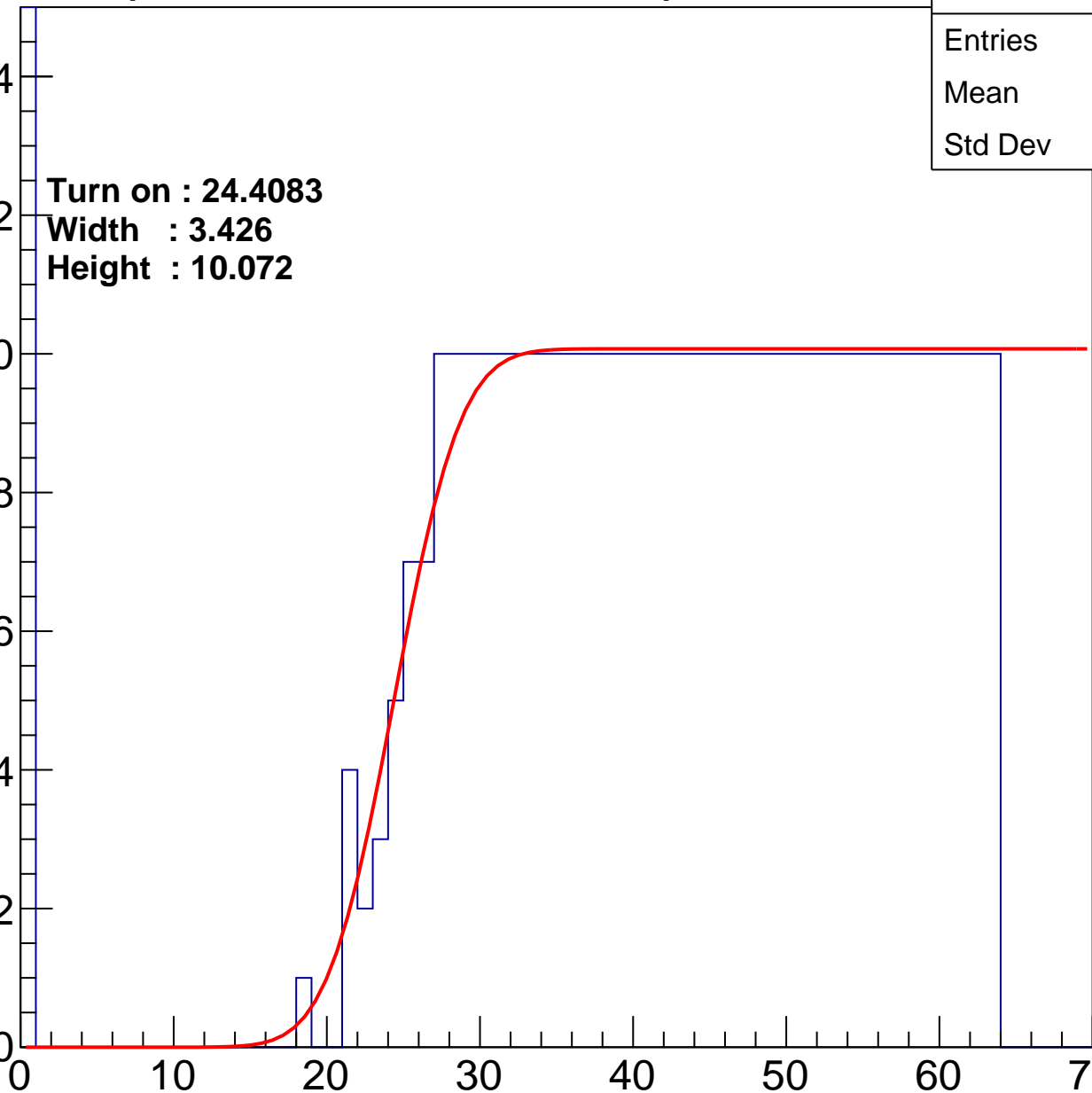
Width : 3.426

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch7

calib_packv5_041523_1651.root, FC#0, port C2

Entries	392
Mean	40.84
Std Dev	17.42

Turn on : 29.0834

Width : 2.088

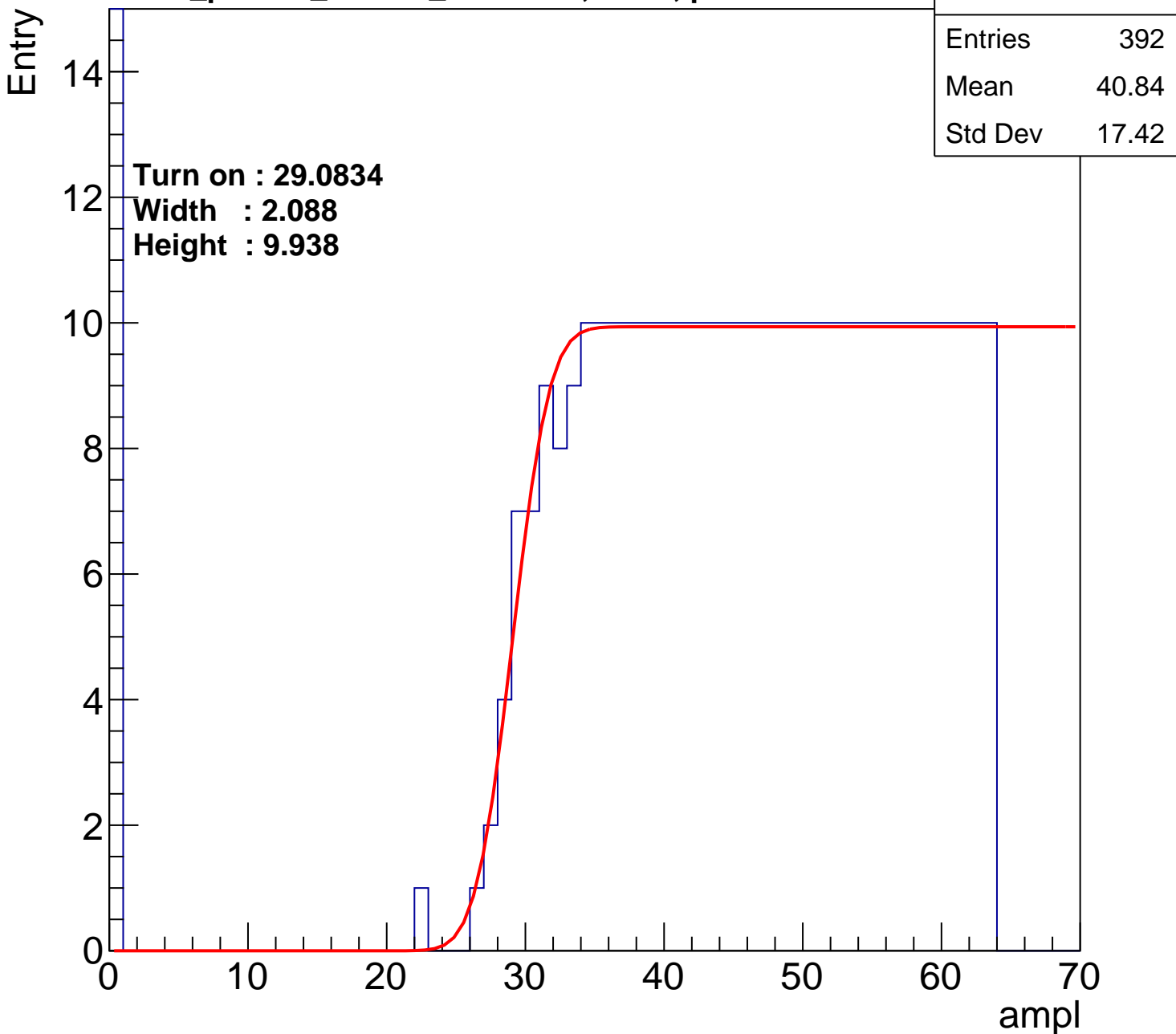
Height : 9.938

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U24-ch8

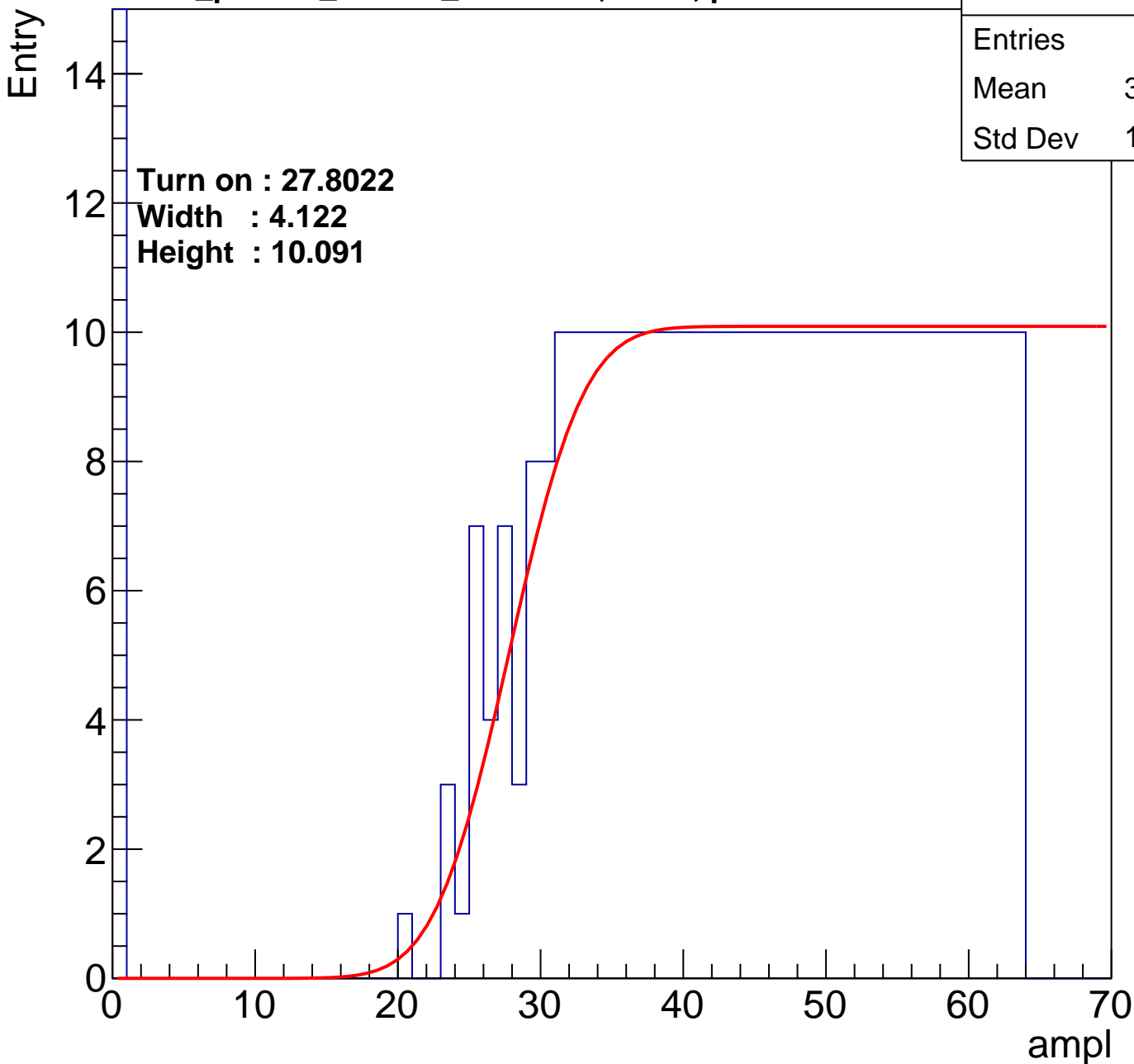
calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	38.62
Std Dev	18.46

Turn on : 27.8022

Width : 4.122

Height : 10.091



B1L103S, U24-ch9

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	39.64
Std Dev	17.76

Turn on : 27.0021

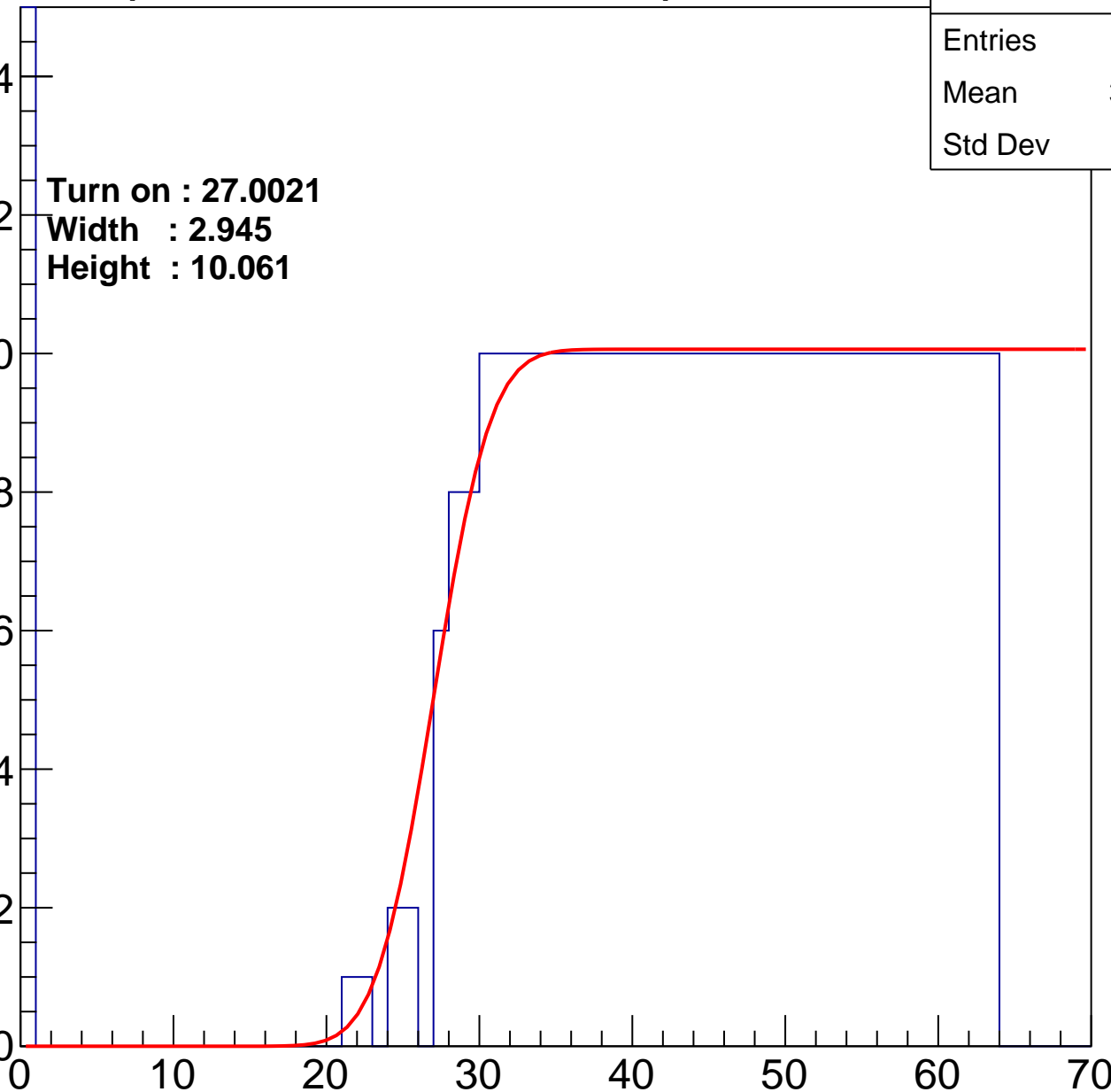
Width : 2.945

Height : 10.061

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch10

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	38.75
Std Dev	17.98

Turn on : 26.4801

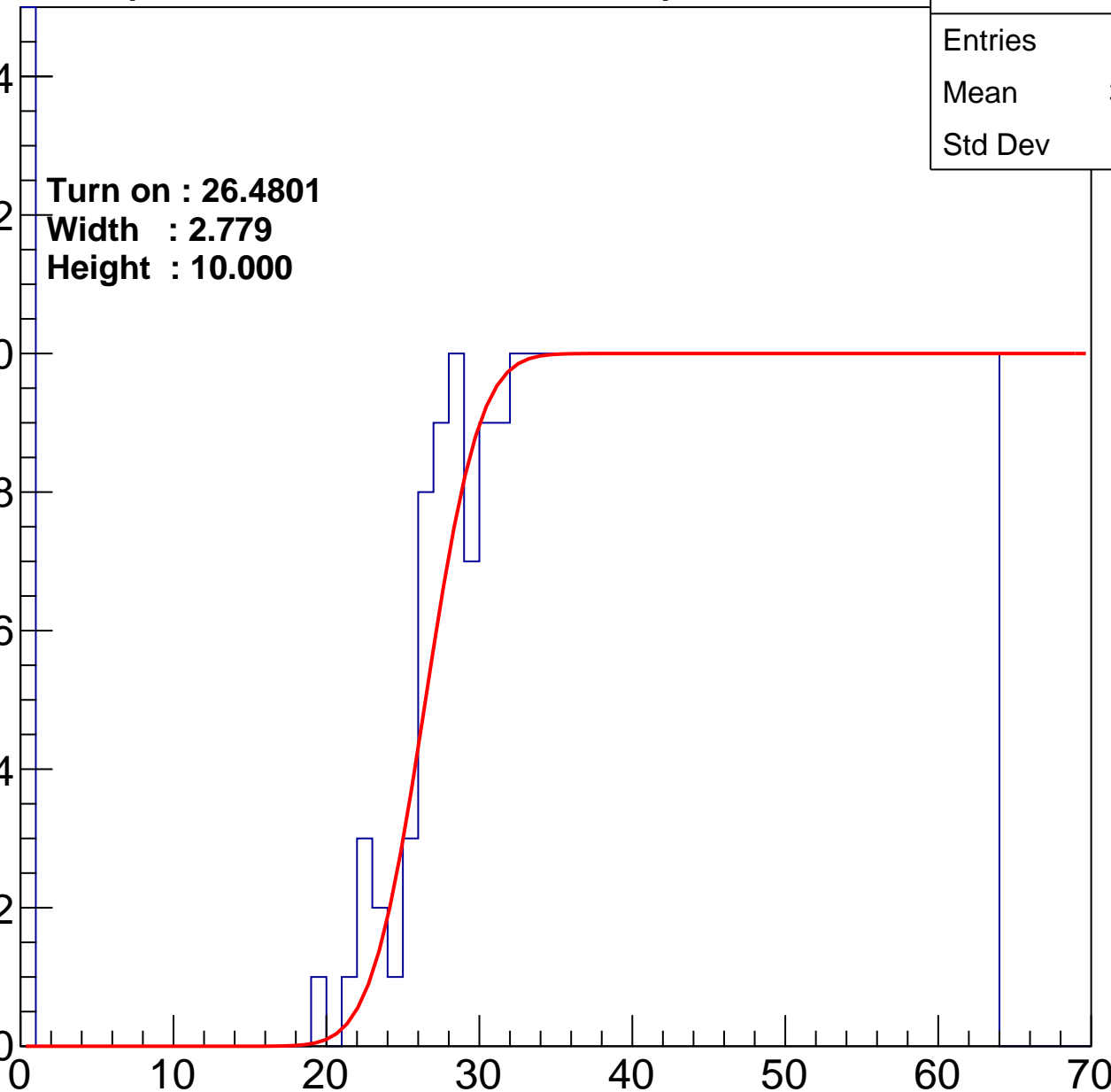
Width : 2.779

Height : 10.000

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch11

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	38.71
Std Dev	18.78

Turn on : 27.6595

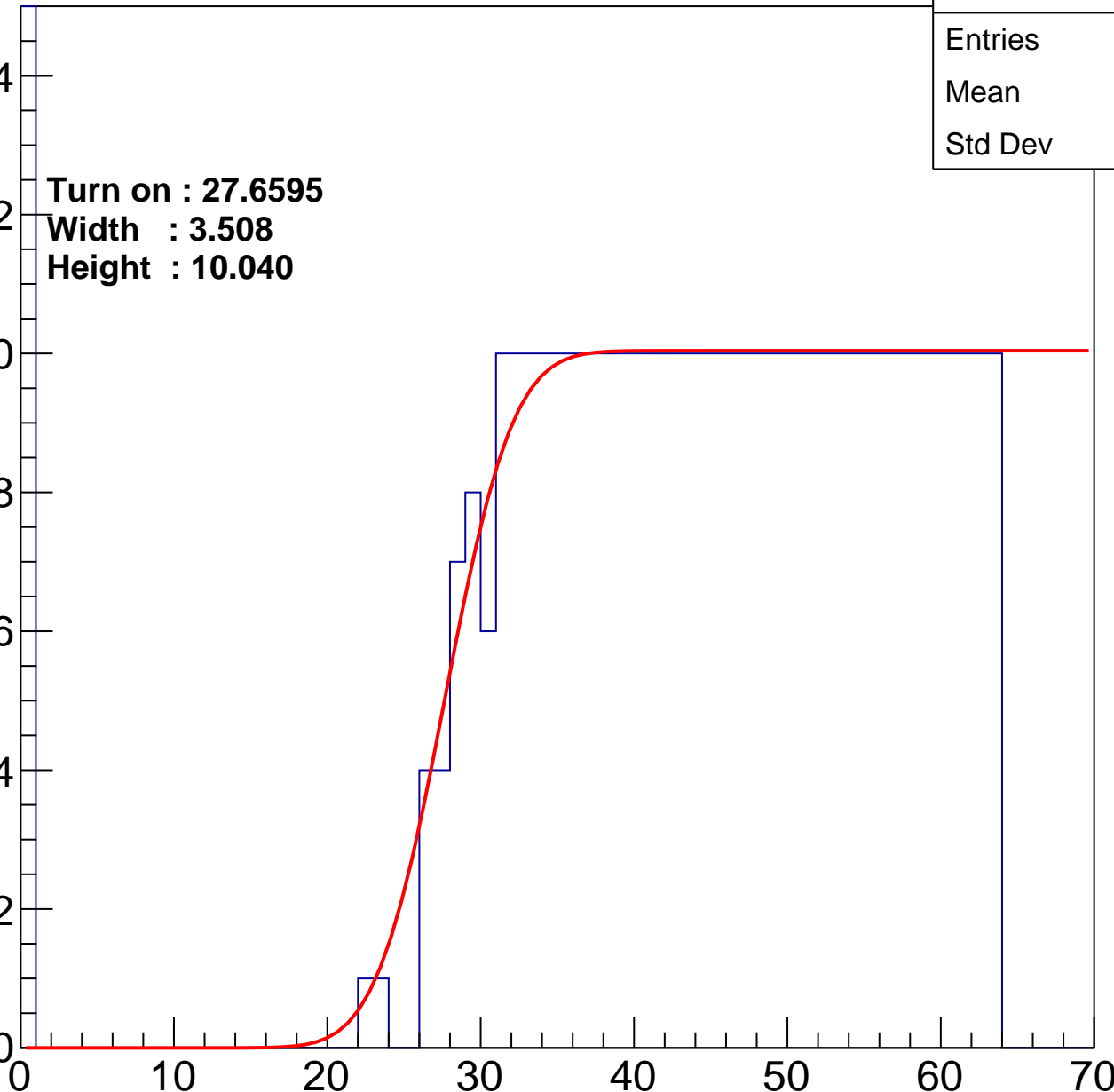
Width : 3.508

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch12

calib_packv5_041523_1651.root, FC#0, port C2

Entries	462
Mean	37.59
Std Dev	18.33

Turn on : 24.0138

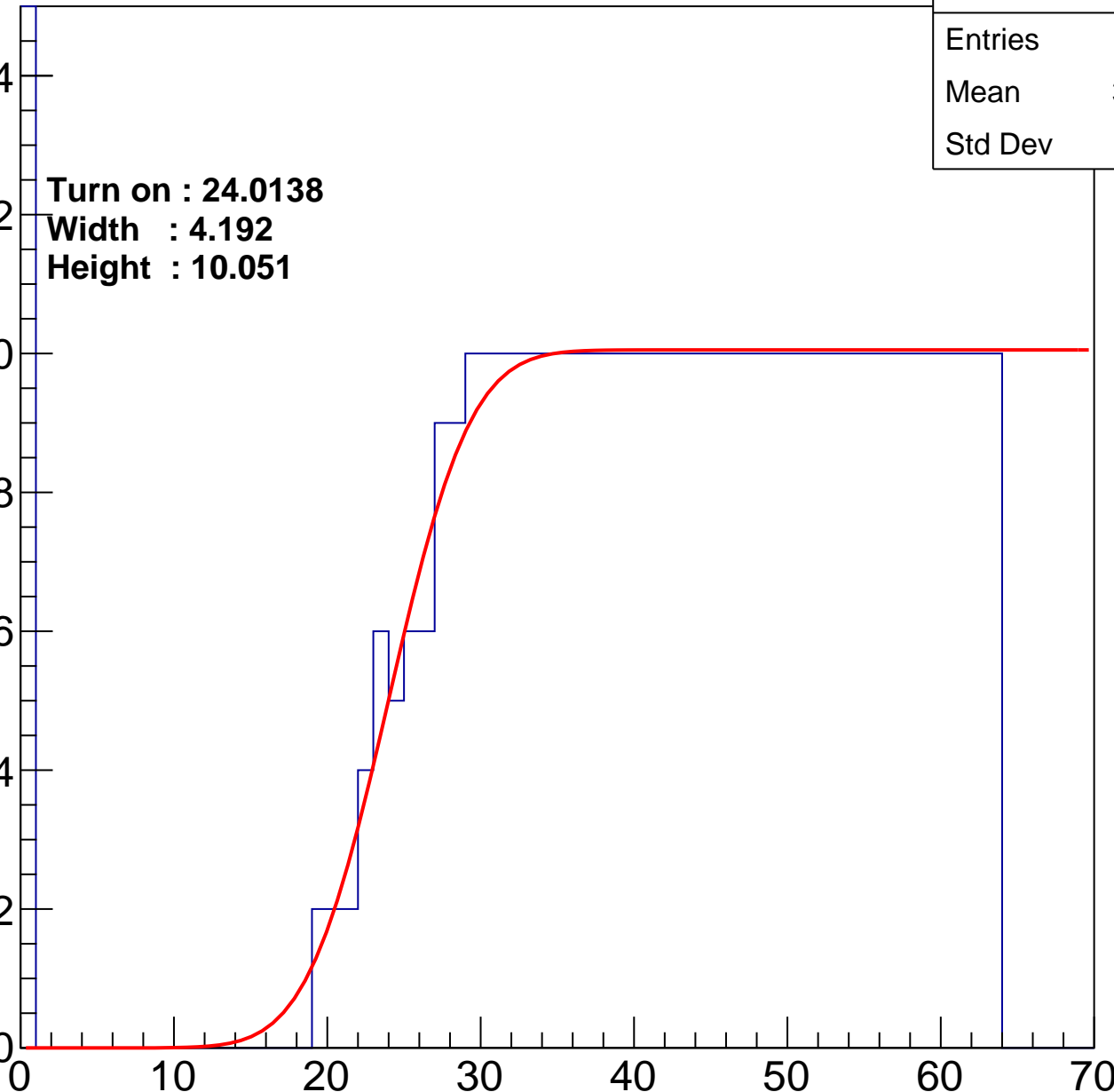
Width : 4.192

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch13

calib_packv5_041523_1651.root, FC#0, port C2

Entries	404
Mean	41.12
Std Dev	16.23

Turn on : 27.2138

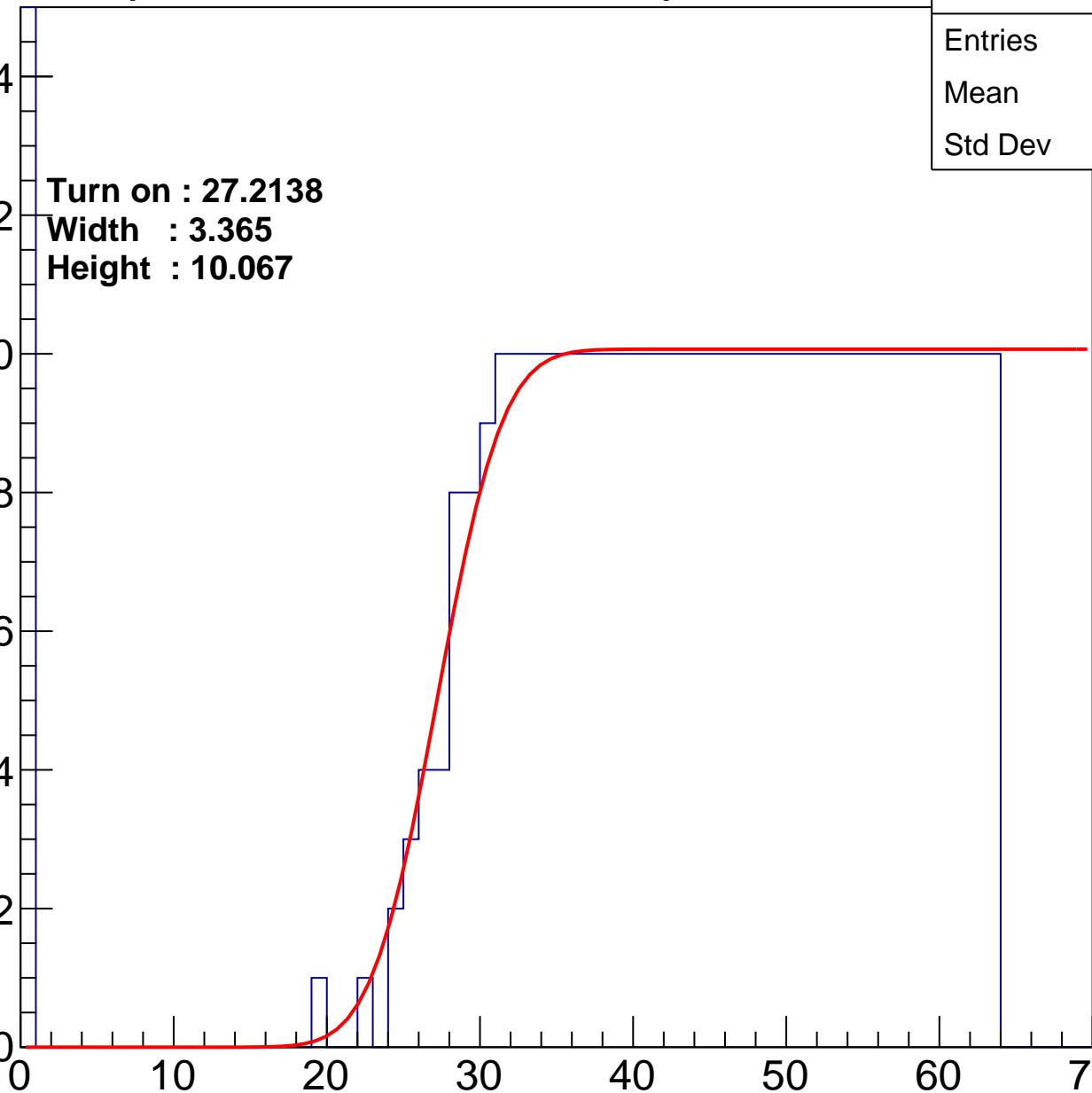
Width : 3.365

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch14

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	40.64
Std Dev	16.07

Turn on : 25.3182

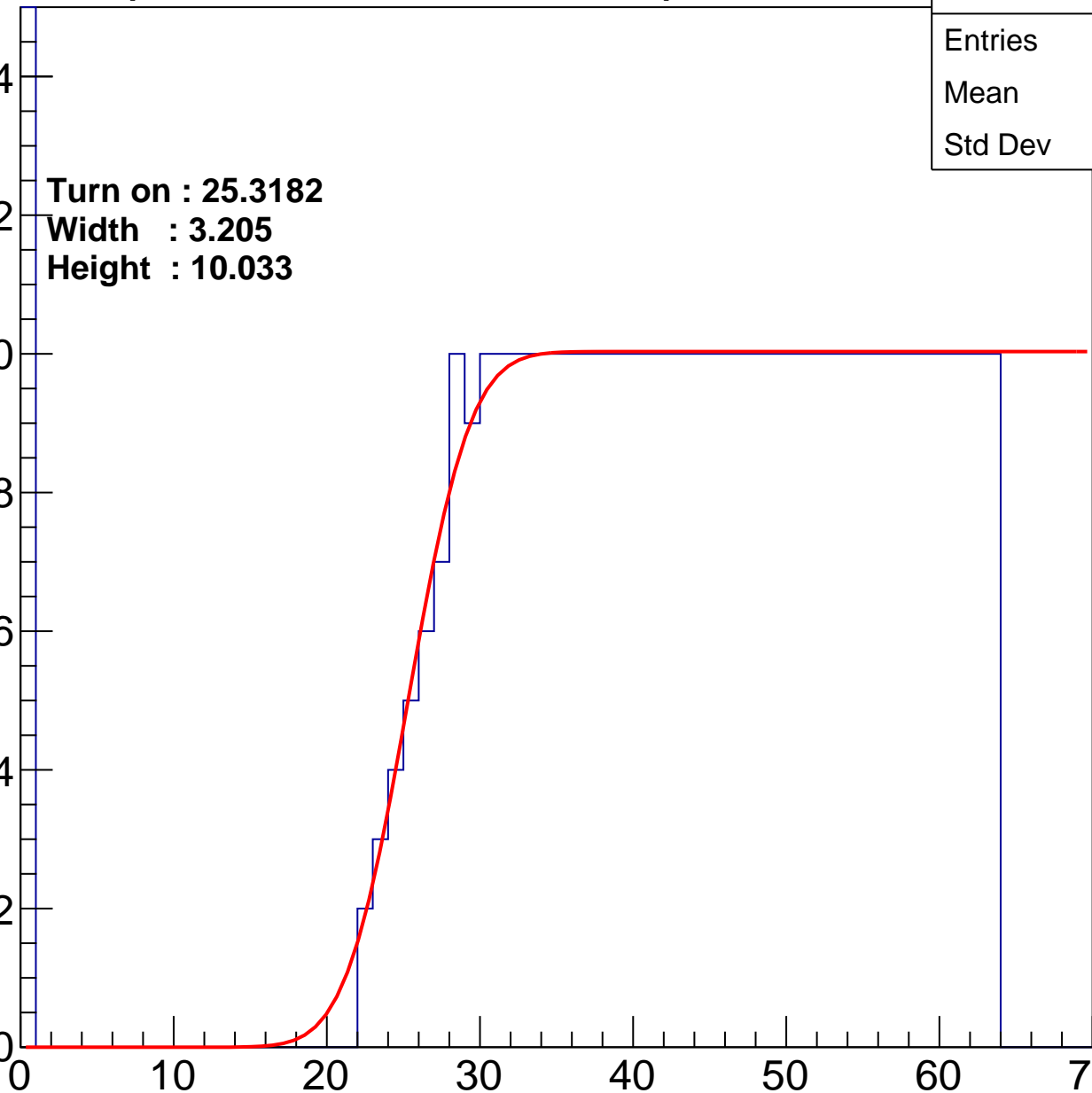
Width : 3.205

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch15

calib_packv5_041523_1651.root, FC#0, port C2

Entries	411
Mean	40.05
Std Dev	17.53

Turn on : 27.3505

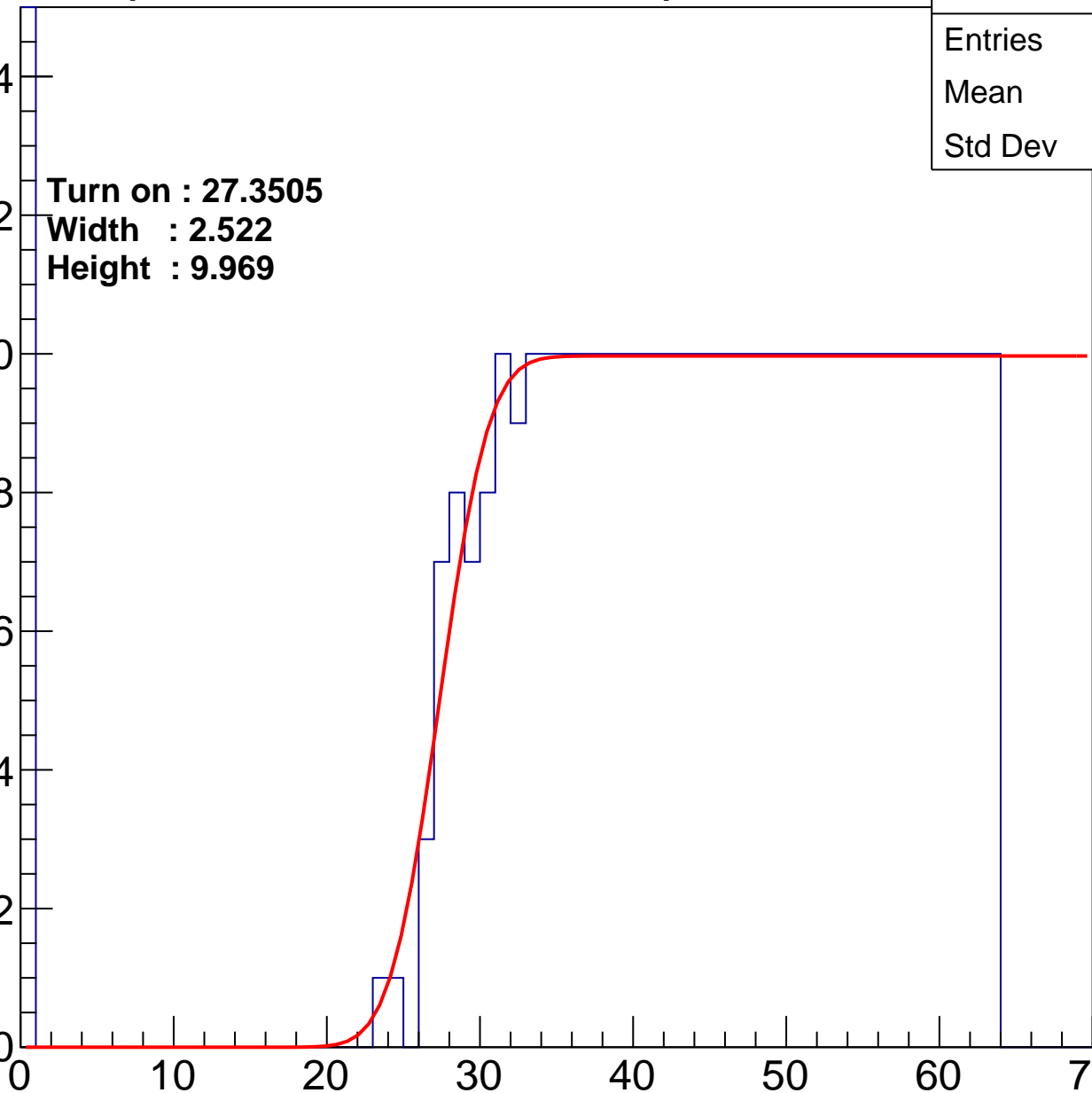
Width : 2.522

Height : 9.969

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch16

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	39.42
Std Dev	17.72

Turn on : 27.4460

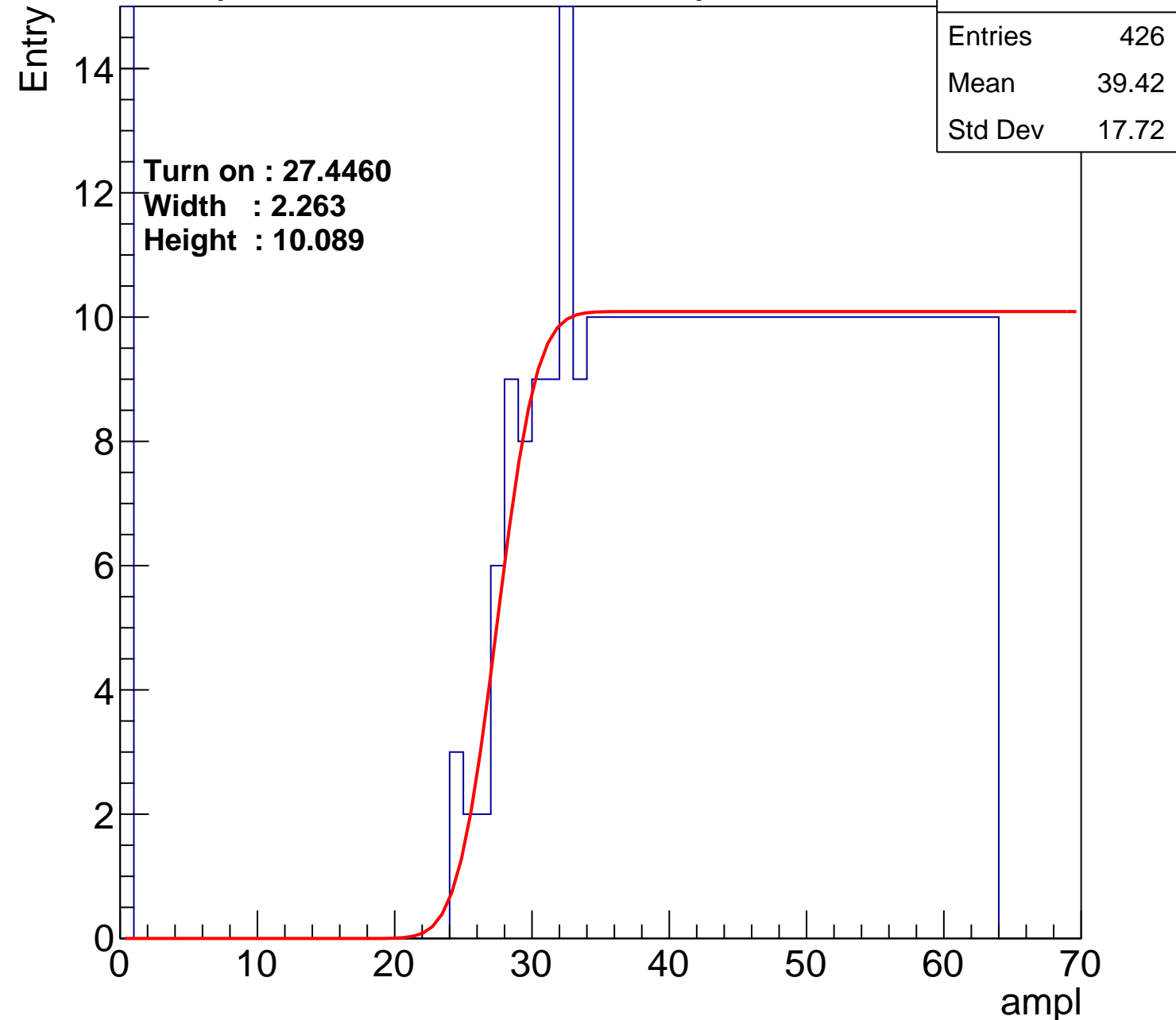
Width : 2.263

Height : 10.089

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch17

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.38
Std Dev	17.51

Turn on : 25.7613

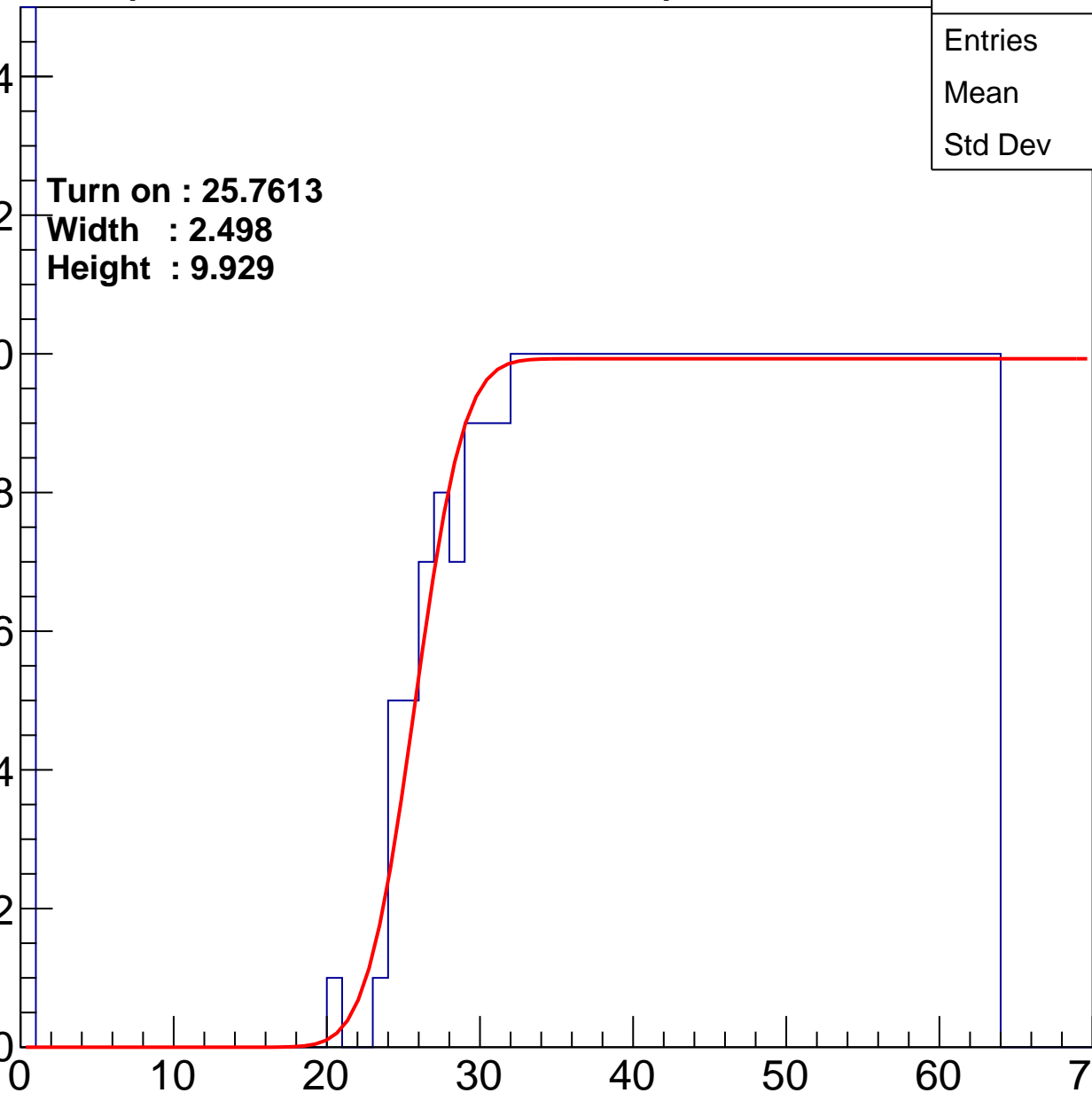
Width : 2.498

Height : 9.929

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch18

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	39.38
Std Dev	17.26

Turn on : 25.1507

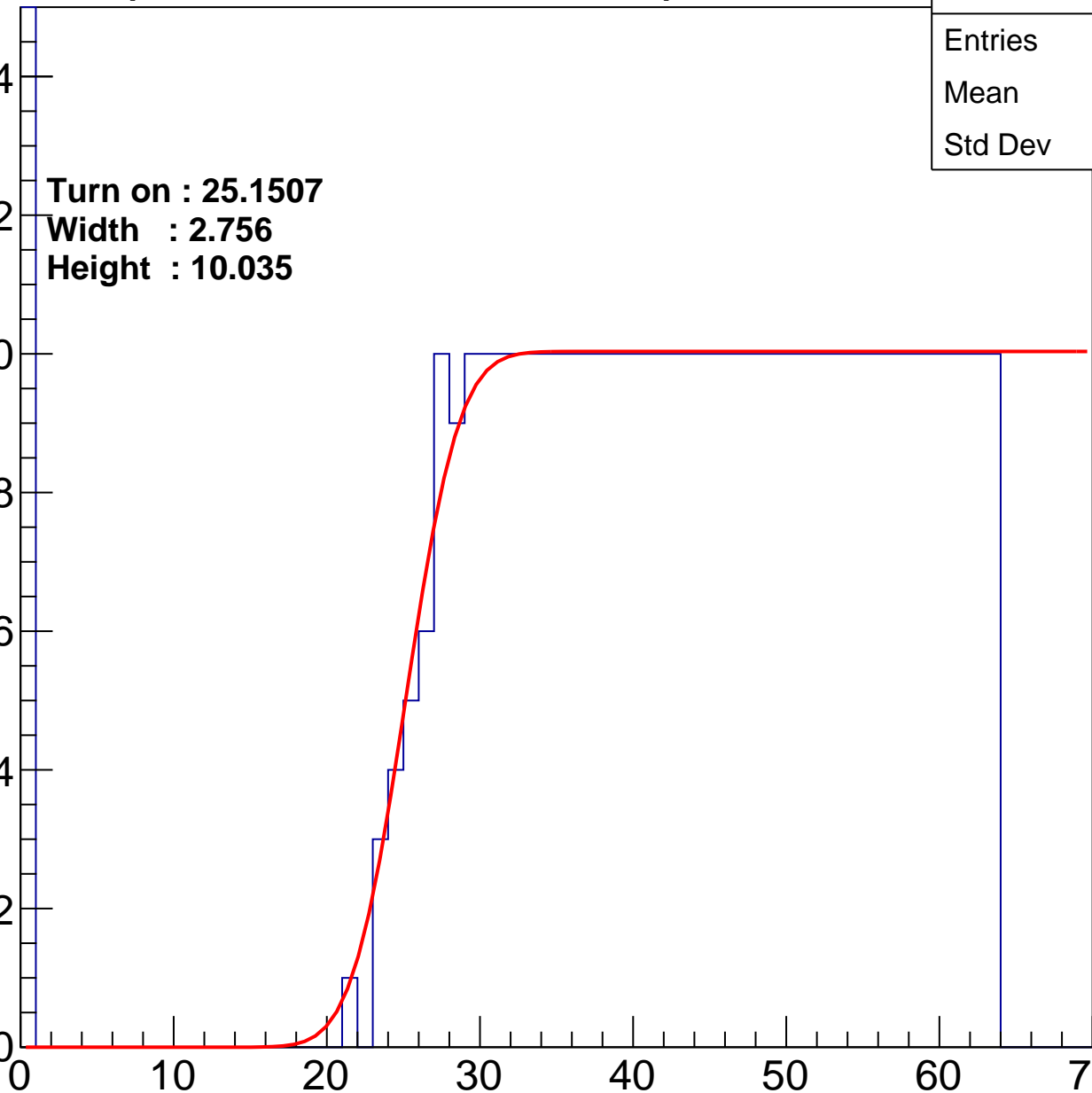
Width : 2.756

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch19

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	39.94
Std Dev	17.29

Turn on : 26.9580

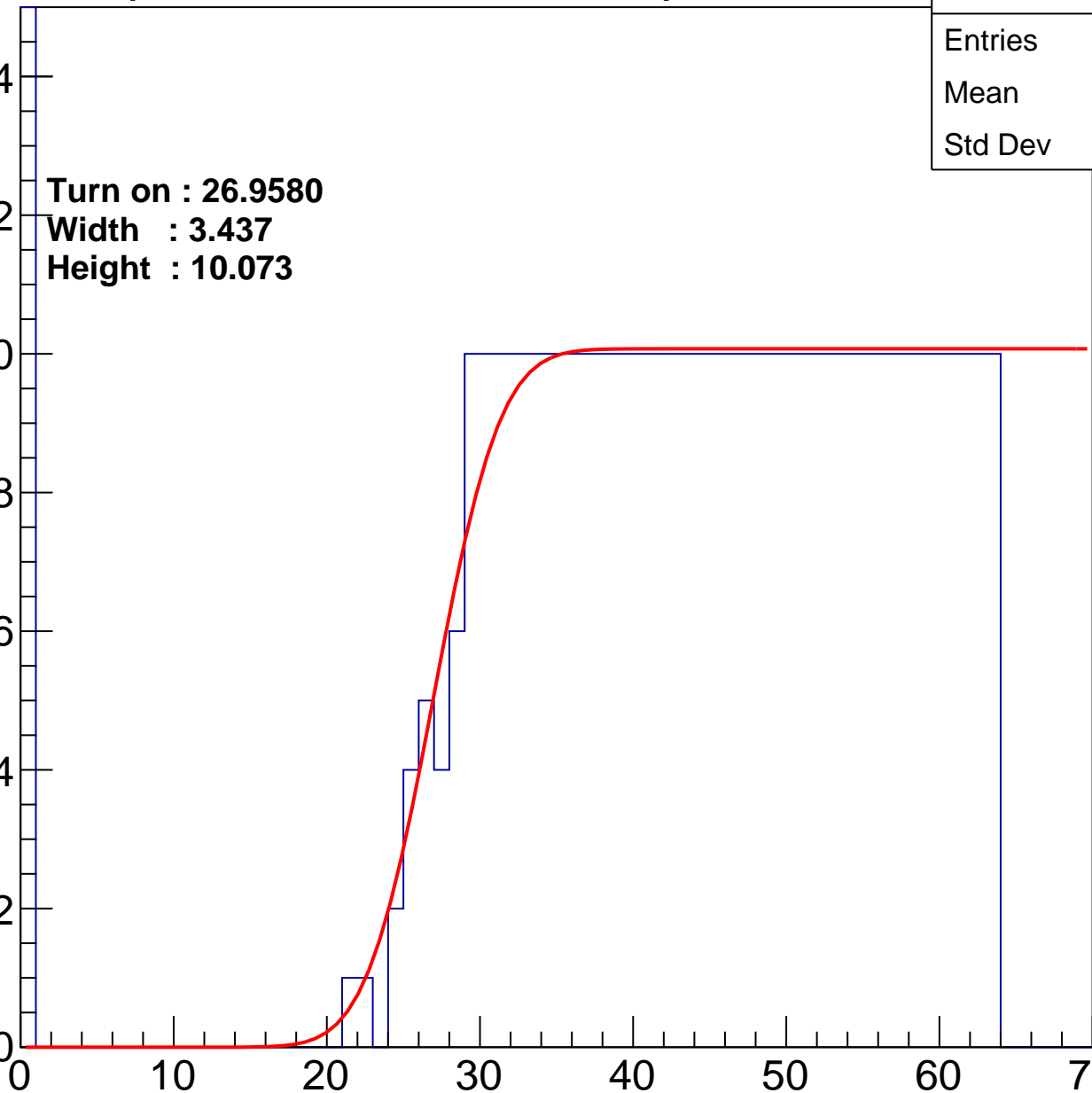
Width : 3.437

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch20

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	39.84
Std Dev	16.97

Turn on : 25.5392

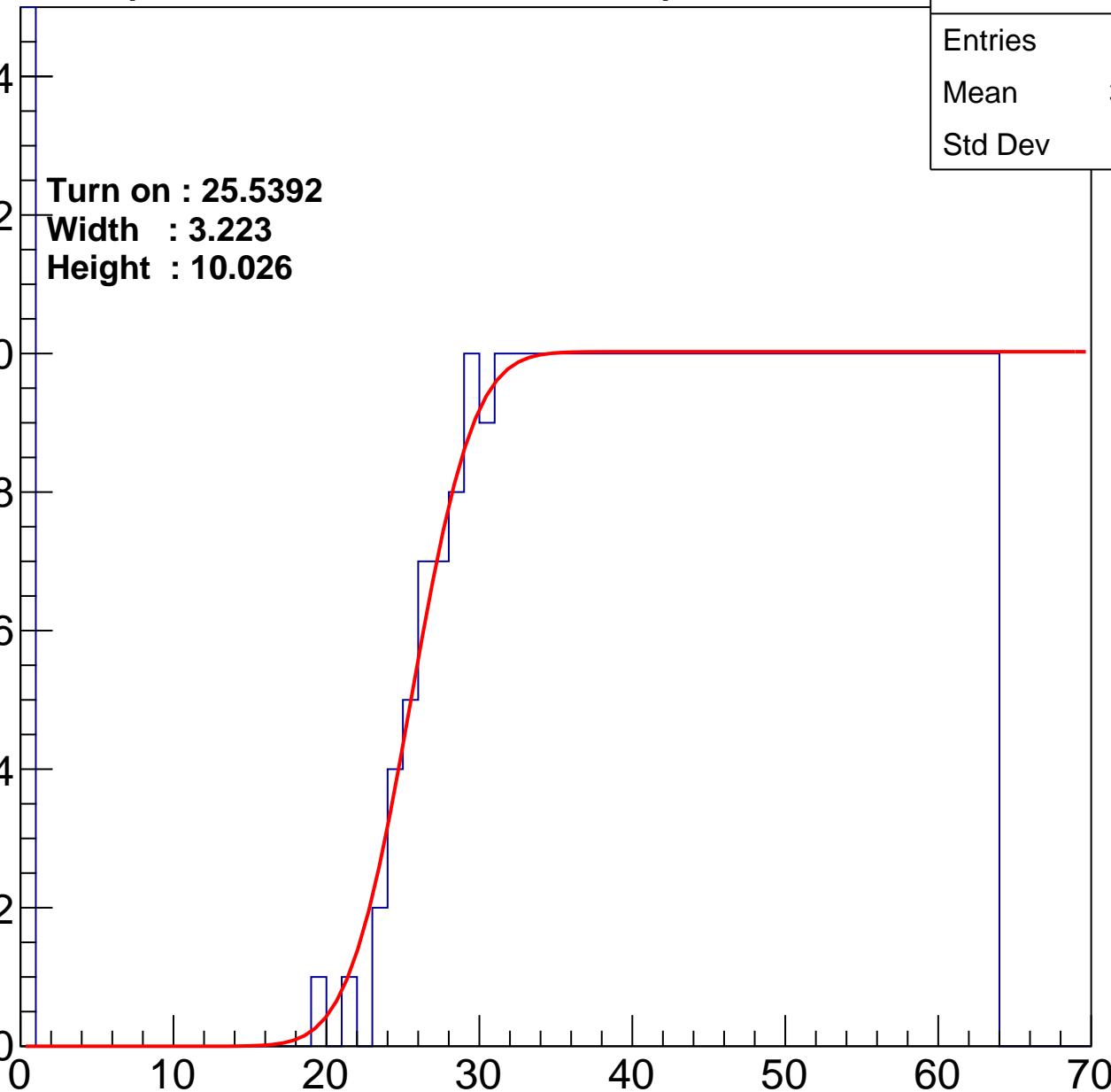
Width : 3.223

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch21

calib_packv5_041523_1651.root, FC#0, port C2

Entries	411
Mean	39.74
Std Dev	17.96

Turn on : 28.7334

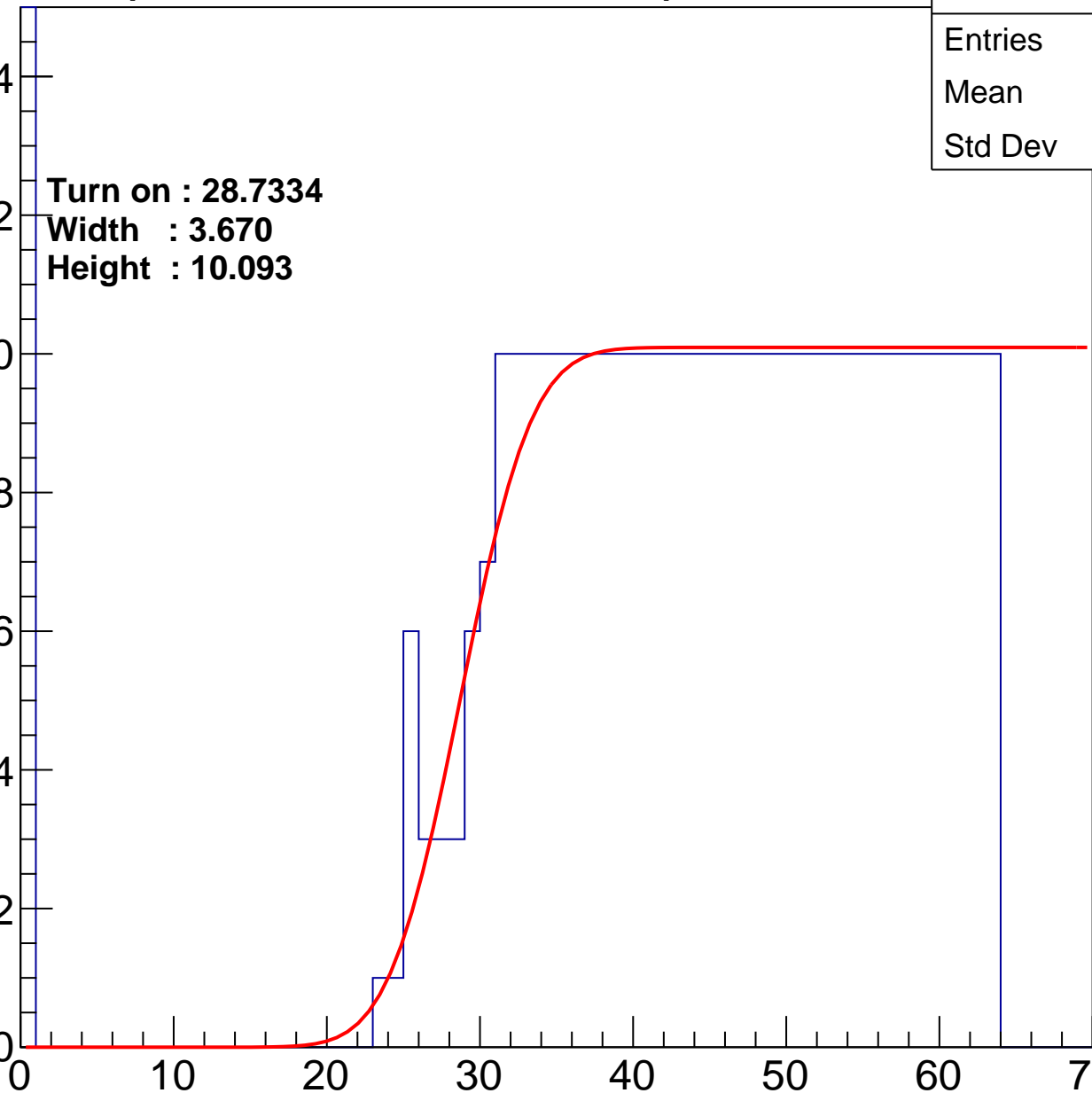
Width : 3.670

Height : 10.093

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch22

calib_packv5_041523_1651.root, FC#0, port C2

Entries	450
Mean	38.22
Std Dev	18.09

Turn on : 25.3405

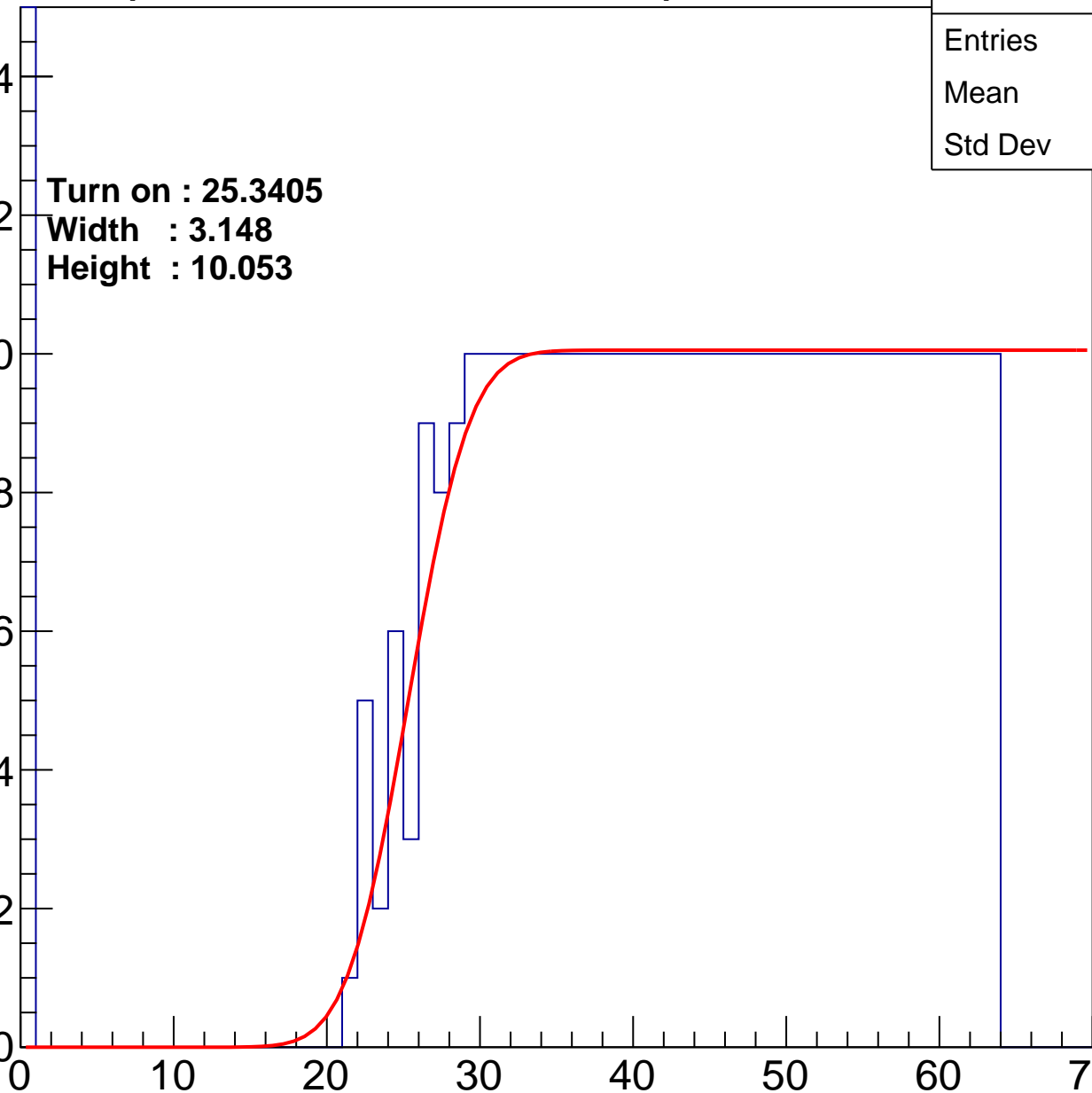
Width : 3.148

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch23

calib_packv5_041523_1651.root, FC#0, port C2

Entries	422
Mean	39.93
Std Dev	17.07

Turn on : 26.2365

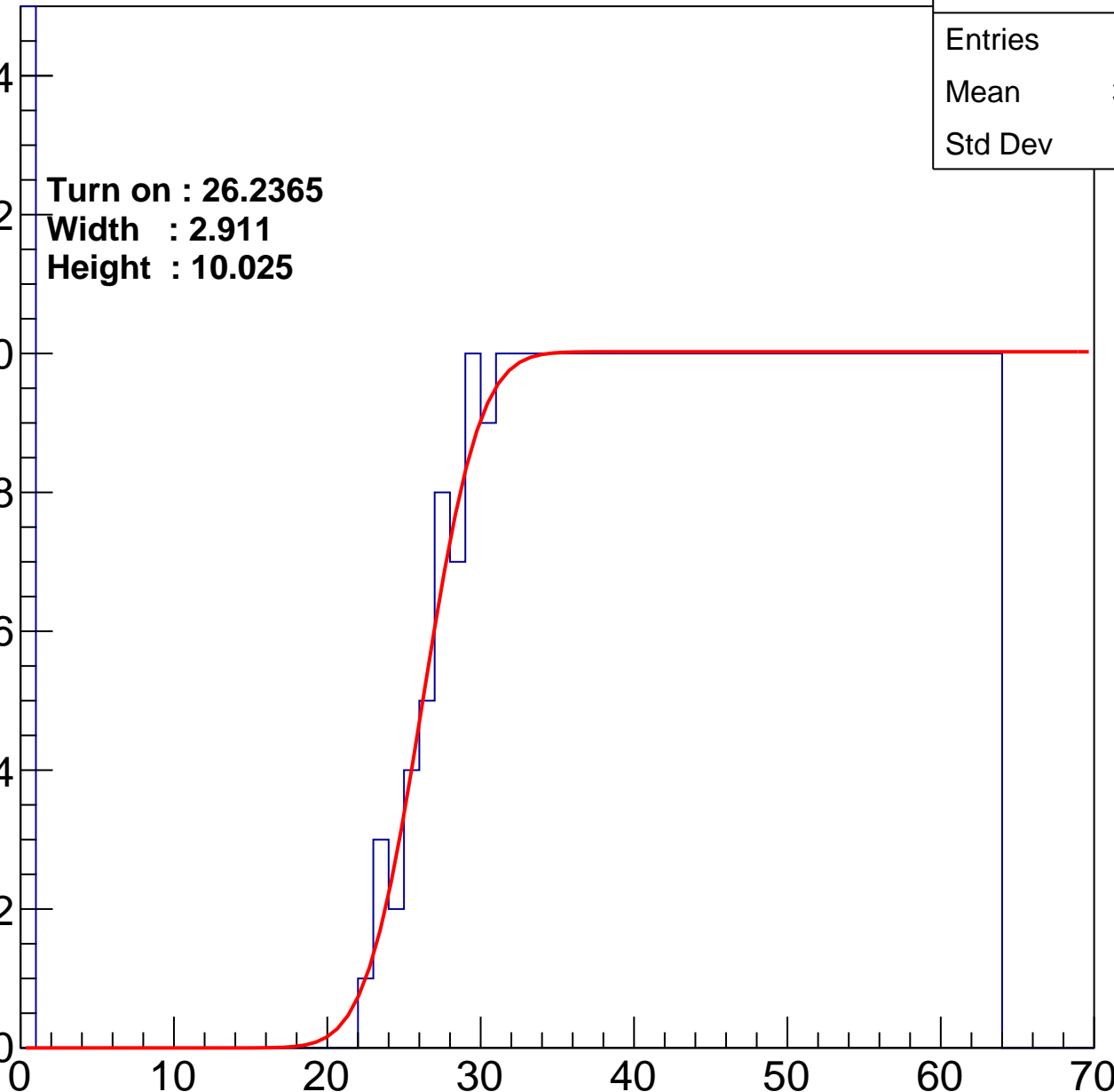
Width : 2.911

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch24

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	39.94
Std Dev	16.84

Turn on : 25.5133

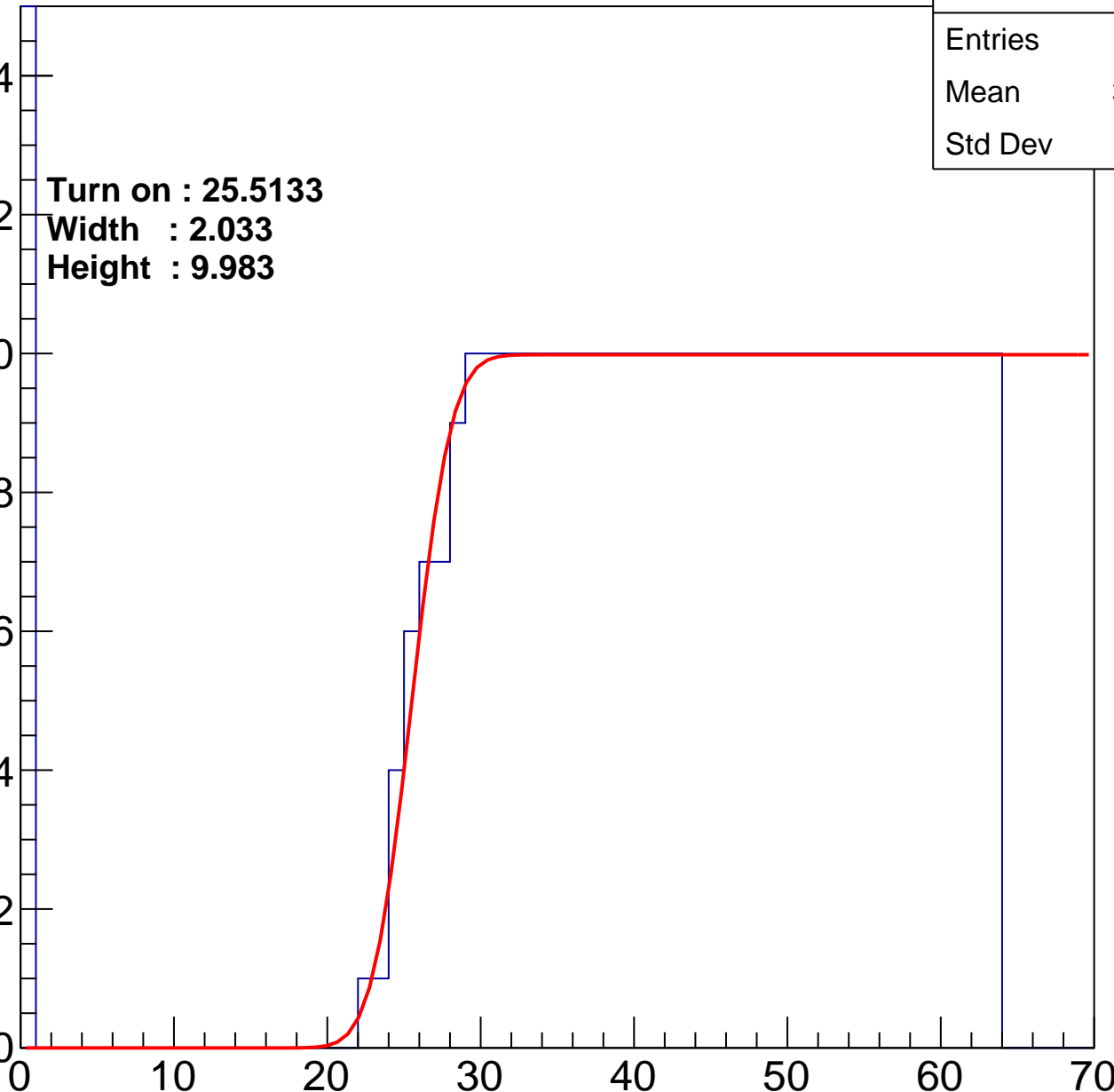
Width : 2.033

Height : 9.983

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch25

calib_packv5_041523_1651.root, FC#0, port C2

Entries	429
Mean	39.63
Std Dev	17.13

Turn on : 26.2771

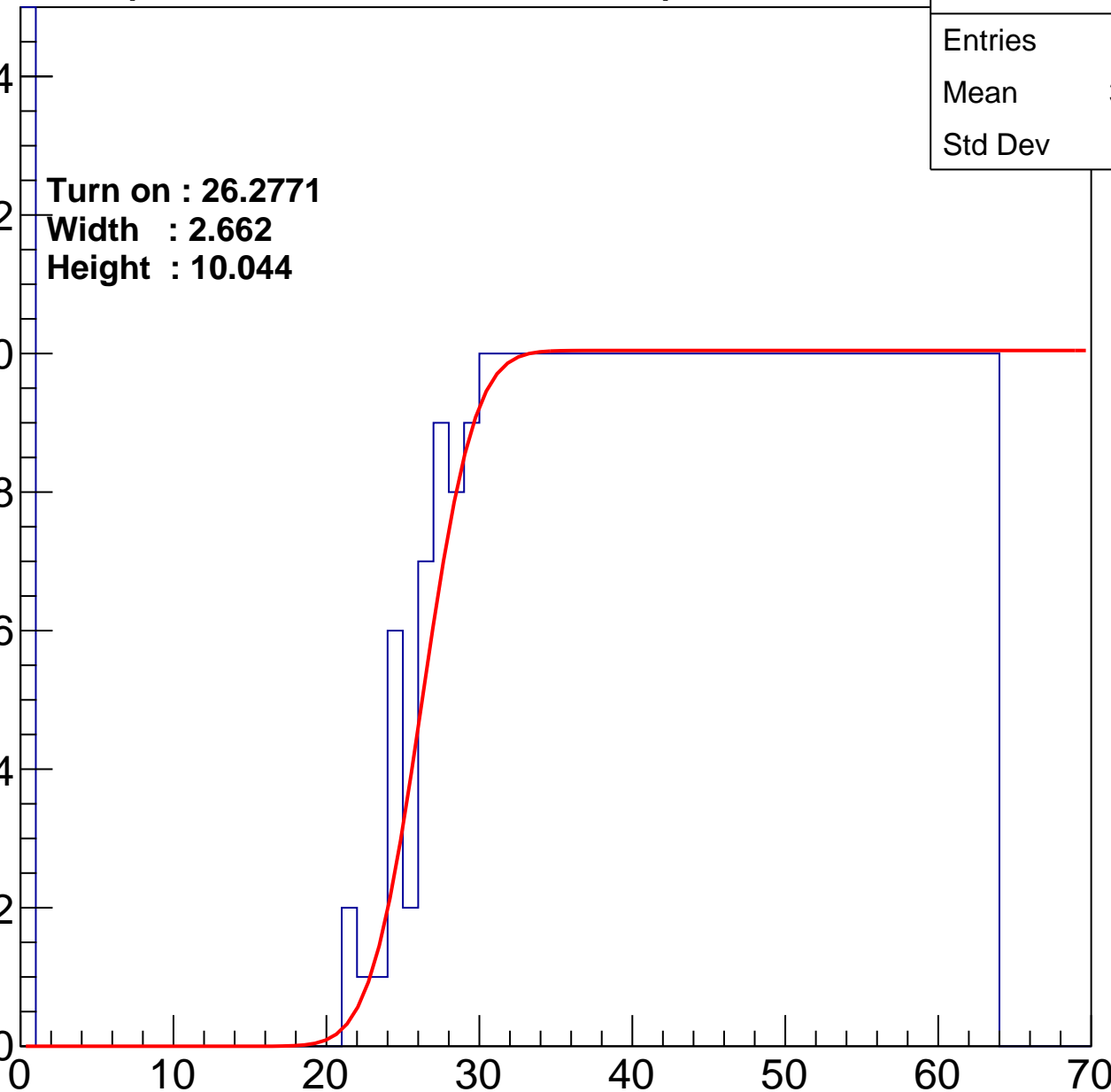
Width : 2.662

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch26

calib_packv5_041523_1651.root, FC#0, port C2

Entries	434
Mean	39.87
Std Dev	16.42

Turn on : 25.2149

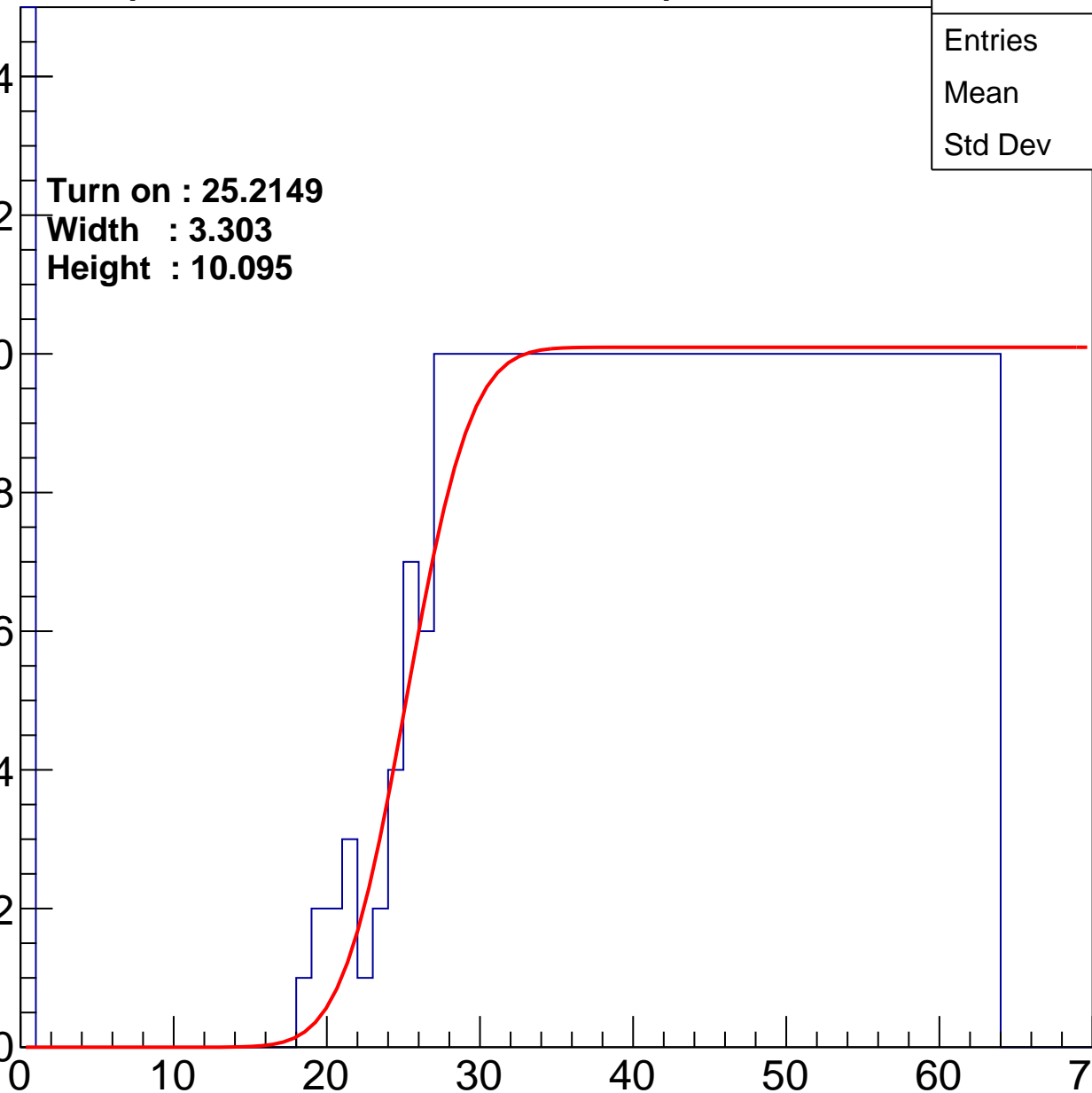
Width : 3.303

Height : 10.095

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch27

calib_packv5_041523_1651.root, FC#0, port C2

Entries	423
Mean	39.01
Std Dev	18.36

Turn on : 27.4718

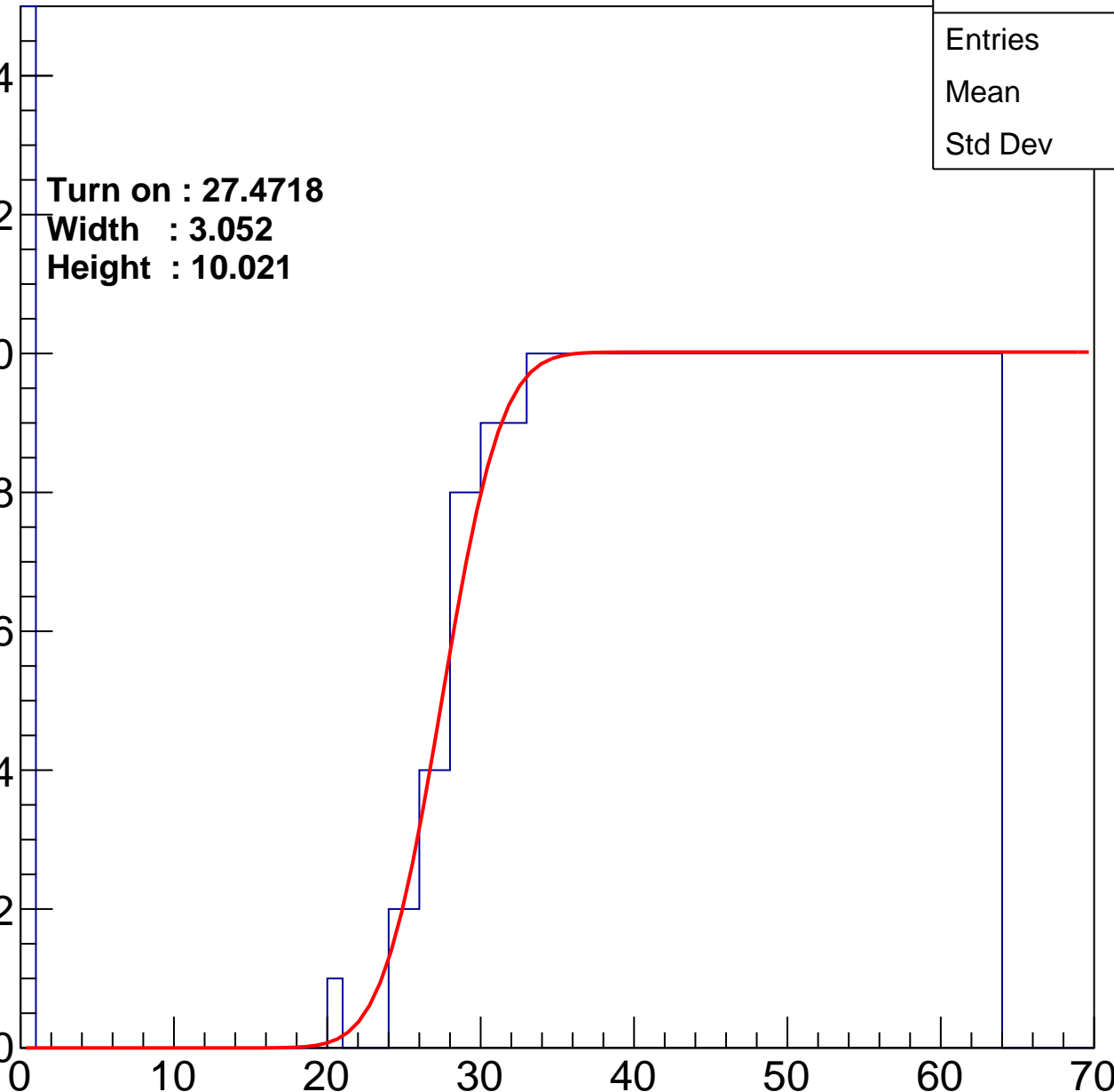
Width : 3.052

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch28

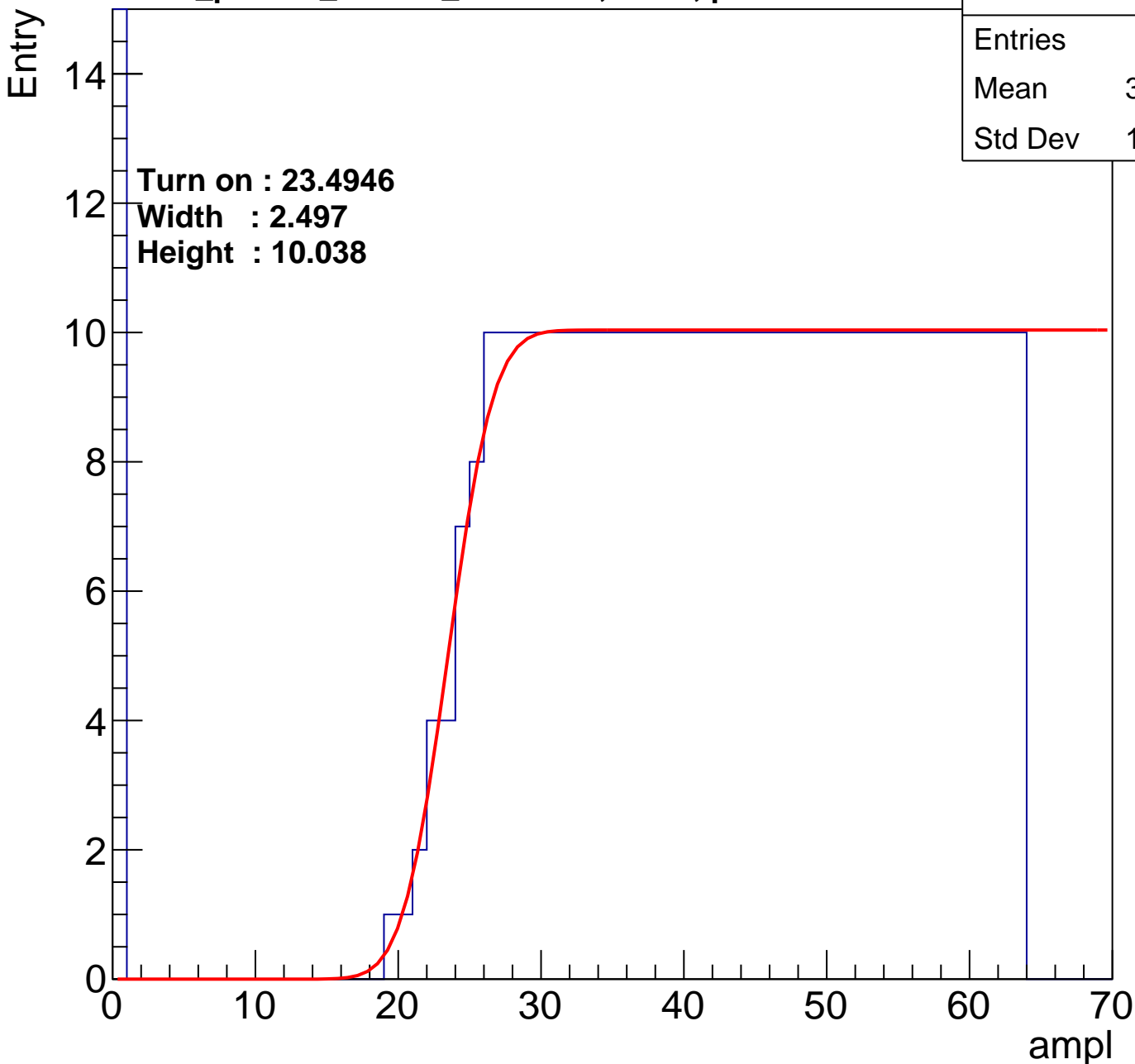
calib_packv5_041523_1651.root, FC#0, port C2

Entries	461
Mean	38.05
Std Dev	17.77

Turn on : 23.4946

Width : 2.497

Height : 10.038



B1L103S, U24-ch29

calib_packv5_041523_1651.root, FC#0, port C2

Entries	441
Mean	37.91
Std Dev	18.95

Turn on : 26.6613

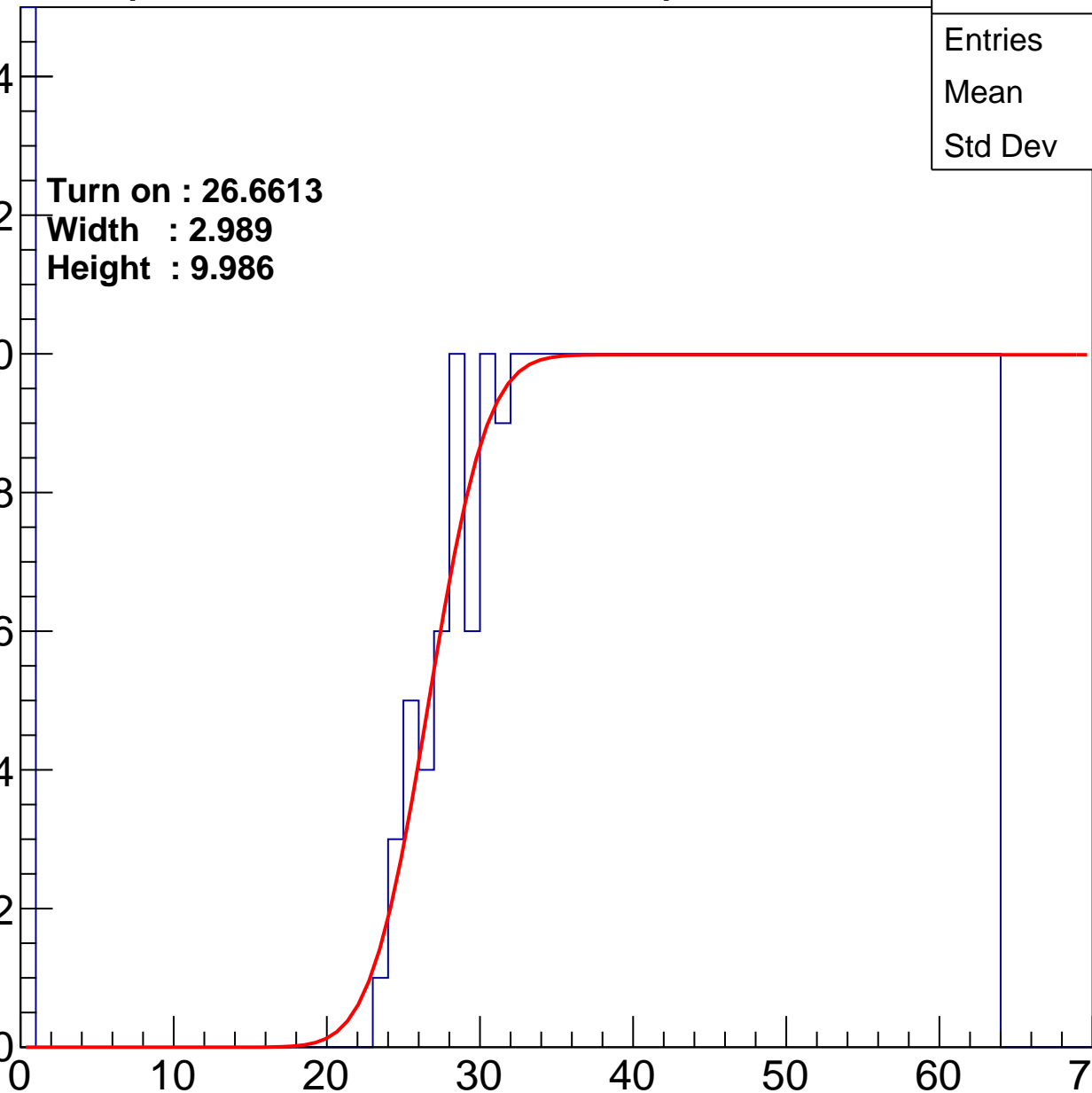
Width : 2.989

Height : 9.986

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch30

calib_packv5_041523_1651.root, FC#0, port C2

Entries	454
Mean	38.74
Std Dev	17.06

Turn on : 23.2440

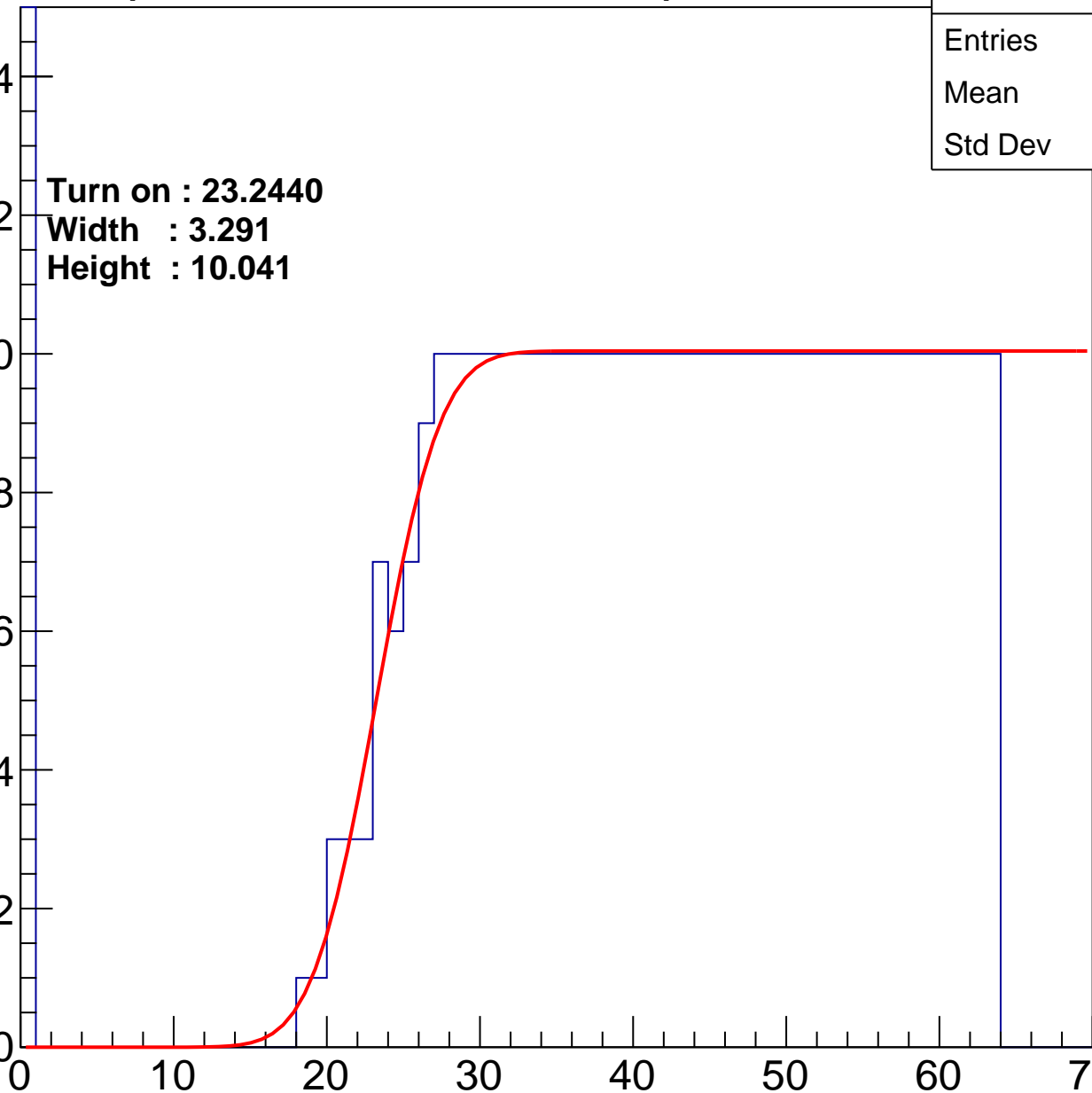
Width : 3.291

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch31

calib_packv5_041523_1651.root, FC#0, port C2

Entries	454
Mean	38
Std Dev	18.2

Turn on : 25.2231

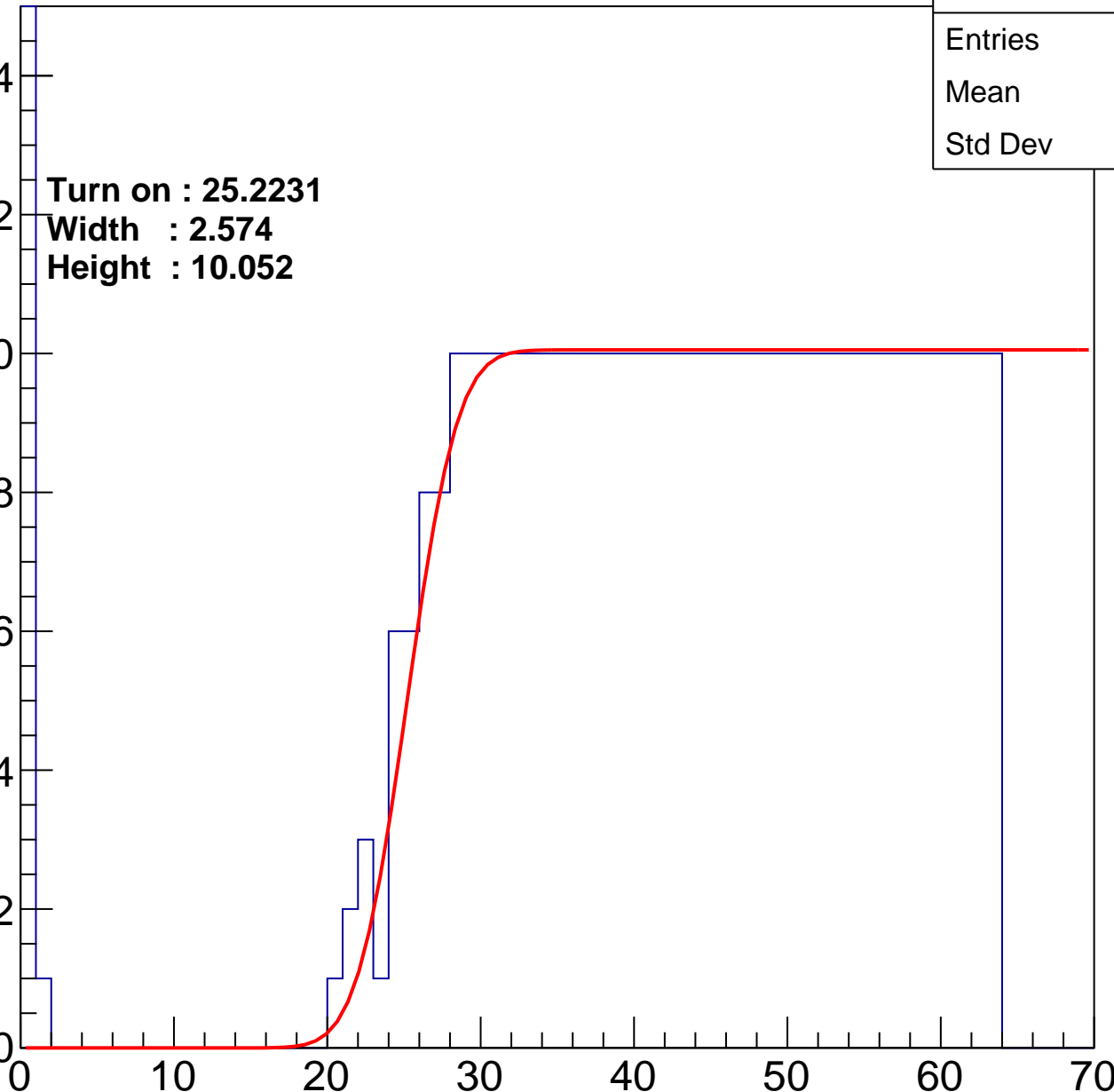
Width : 2.574

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch32

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	39.85
Std Dev	16.95

Turn on : 25.6871

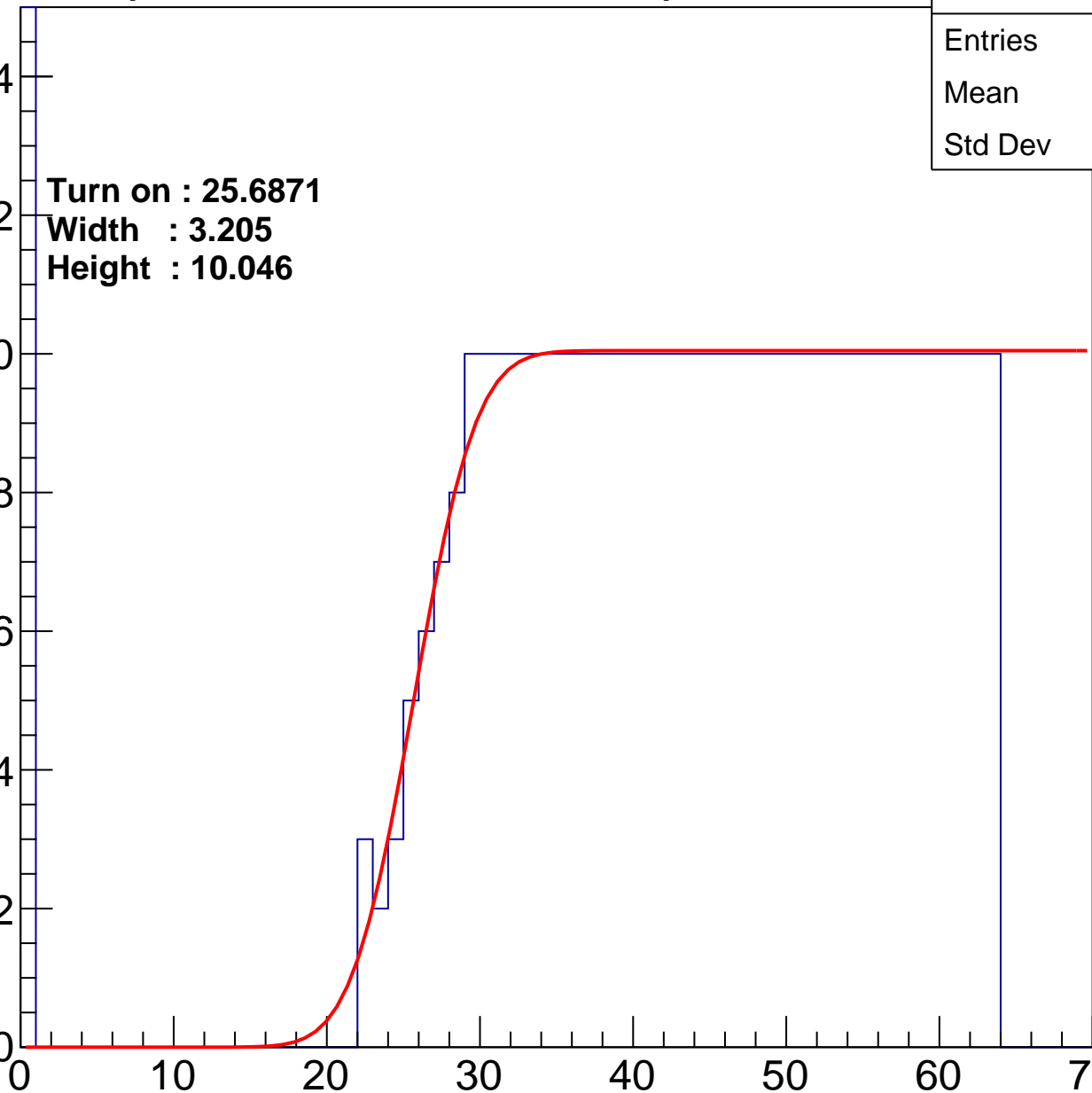
Width : 3.205

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch33

calib_packv5_041523_1651.root, FC#0, port C2

Entries	400
Mean	41.41
Std Dev	16

Turn on : 27.3038

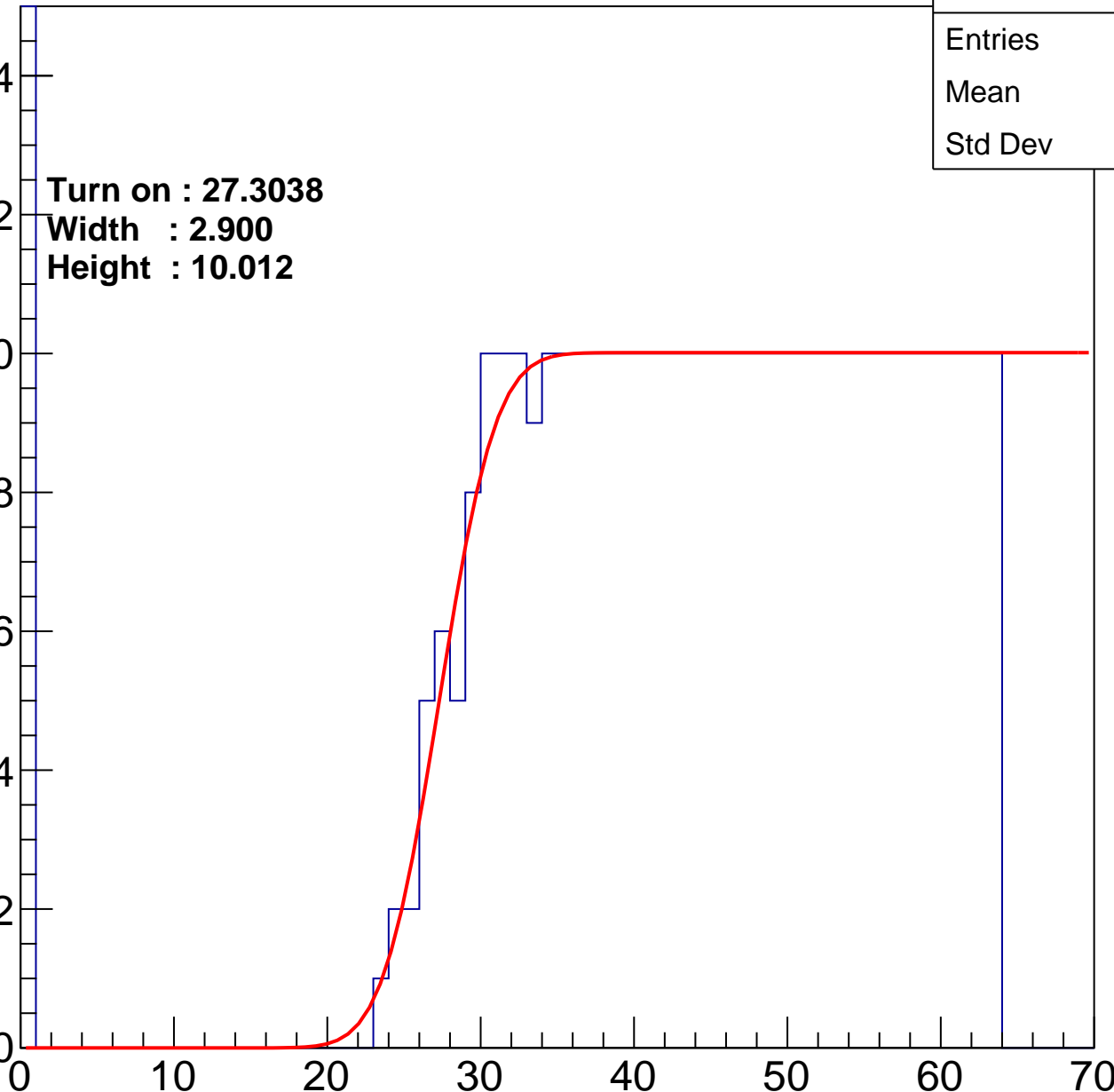
Width : 2.900

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch34

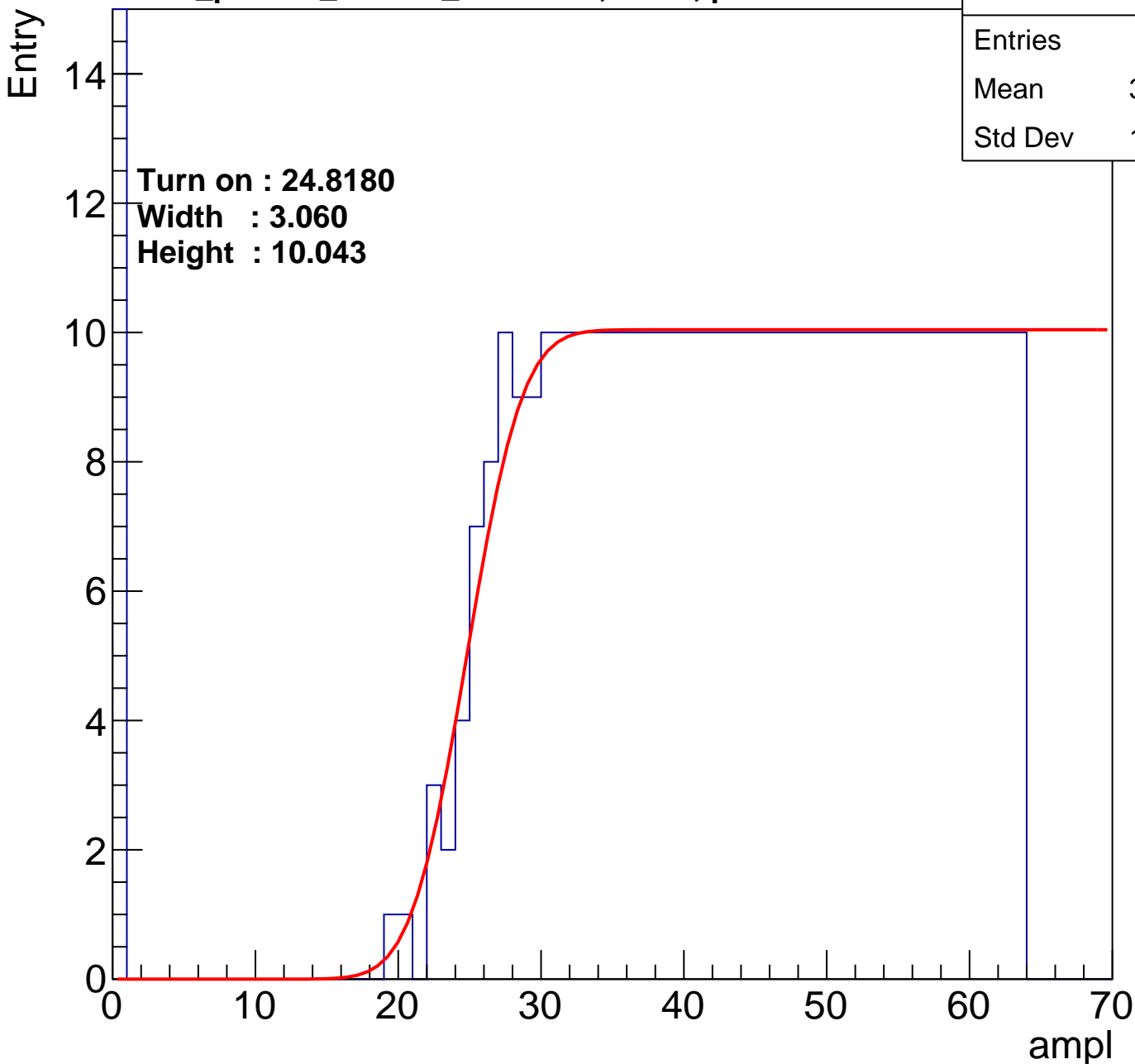
calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	39.32
Std Dev	17.09

Turn on : 24.8180

Width : 3.060

Height : 10.043



B1L103S, U24-ch35

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	38.07
Std Dev	18.84

Turn on : 27.2907

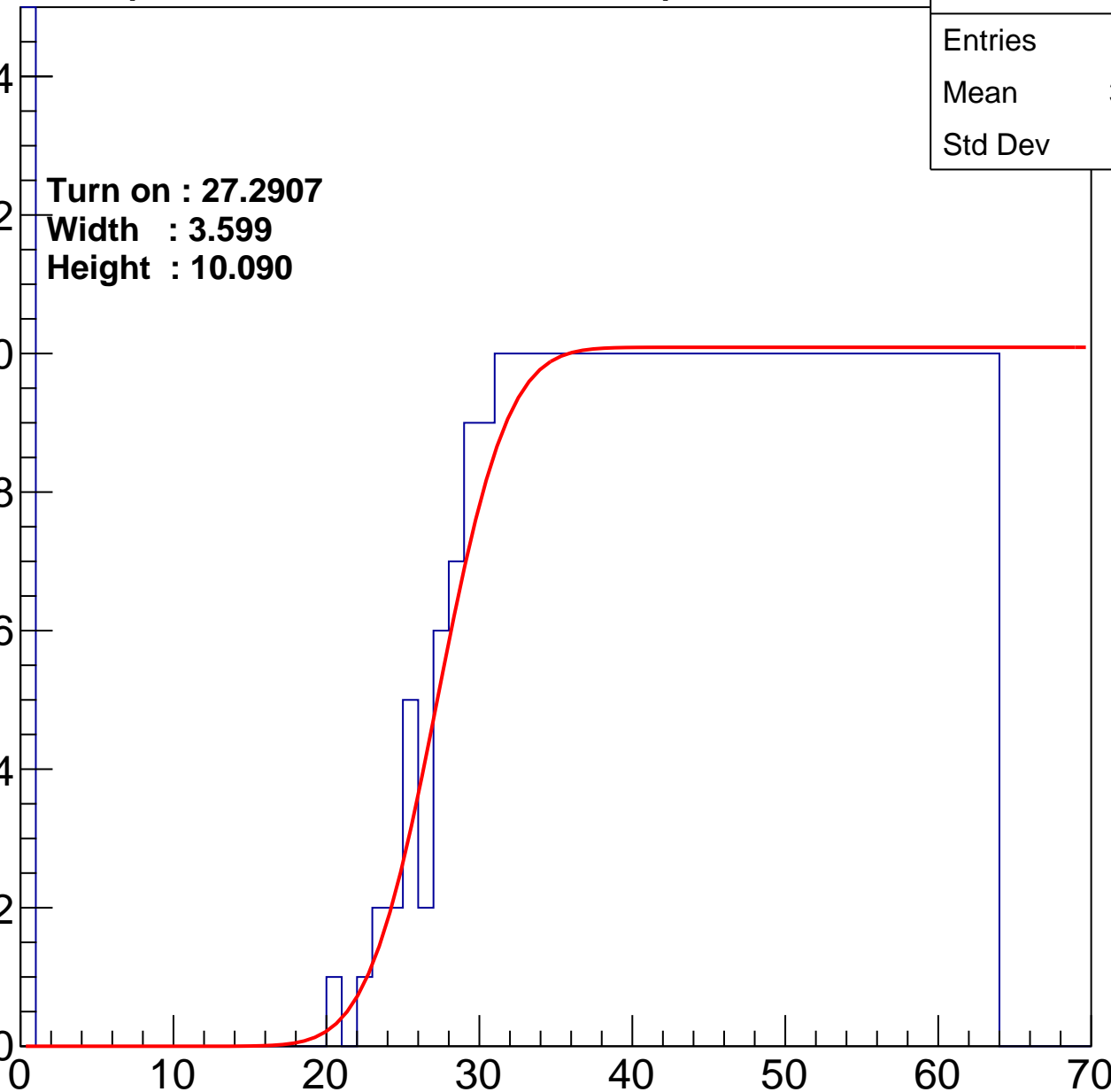
Width : 3.599

Height : 10.090

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch36

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	39.35
Std Dev	17.06

Turn on : 25.3325

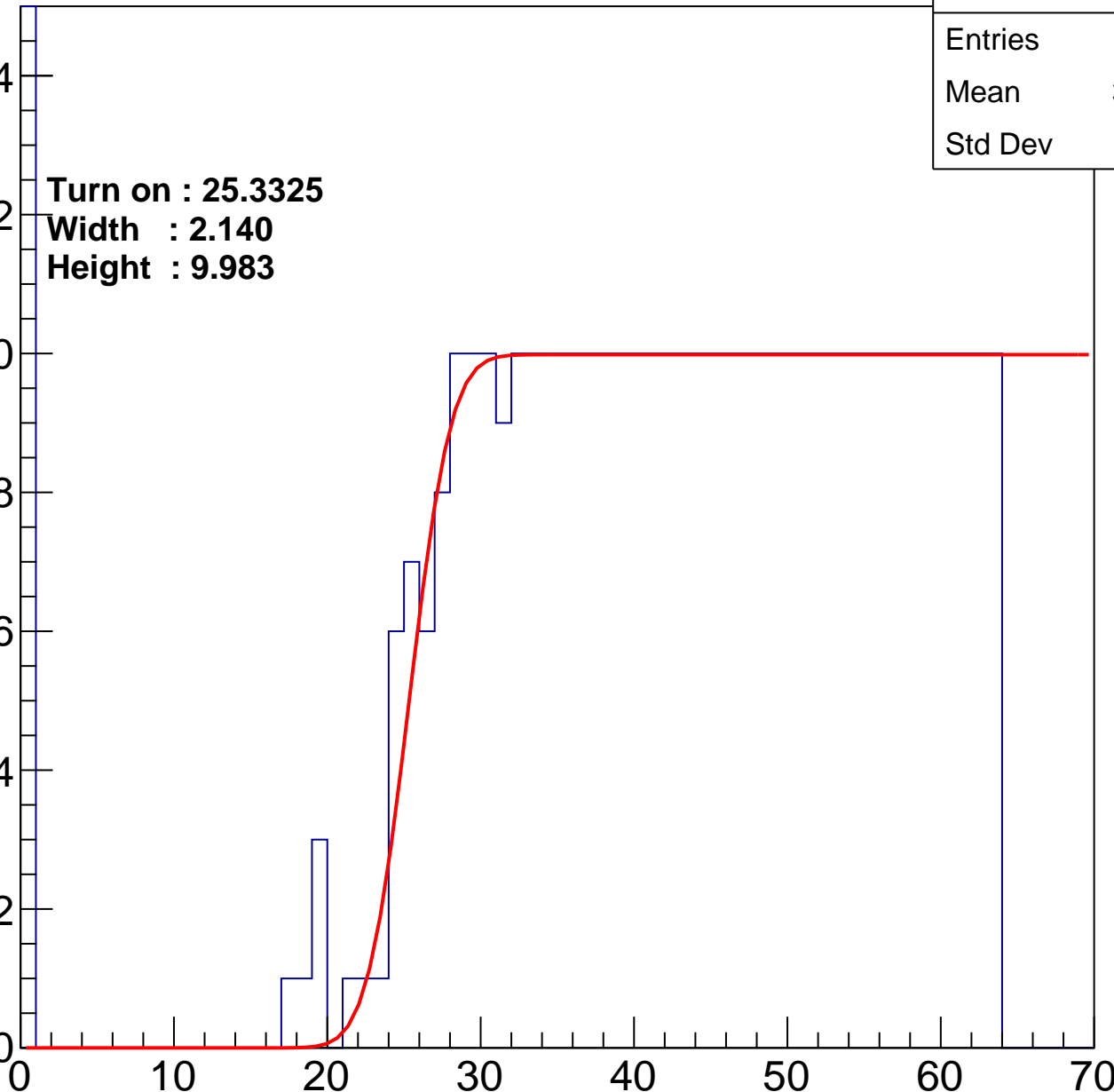
Width : 2.140

Height : 9.983

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch37

calib_packv5_041523_1651.root, FC#0, port C2

Entries	427
Mean	40.01
Std Dev	16.65

Turn on : 25.1959

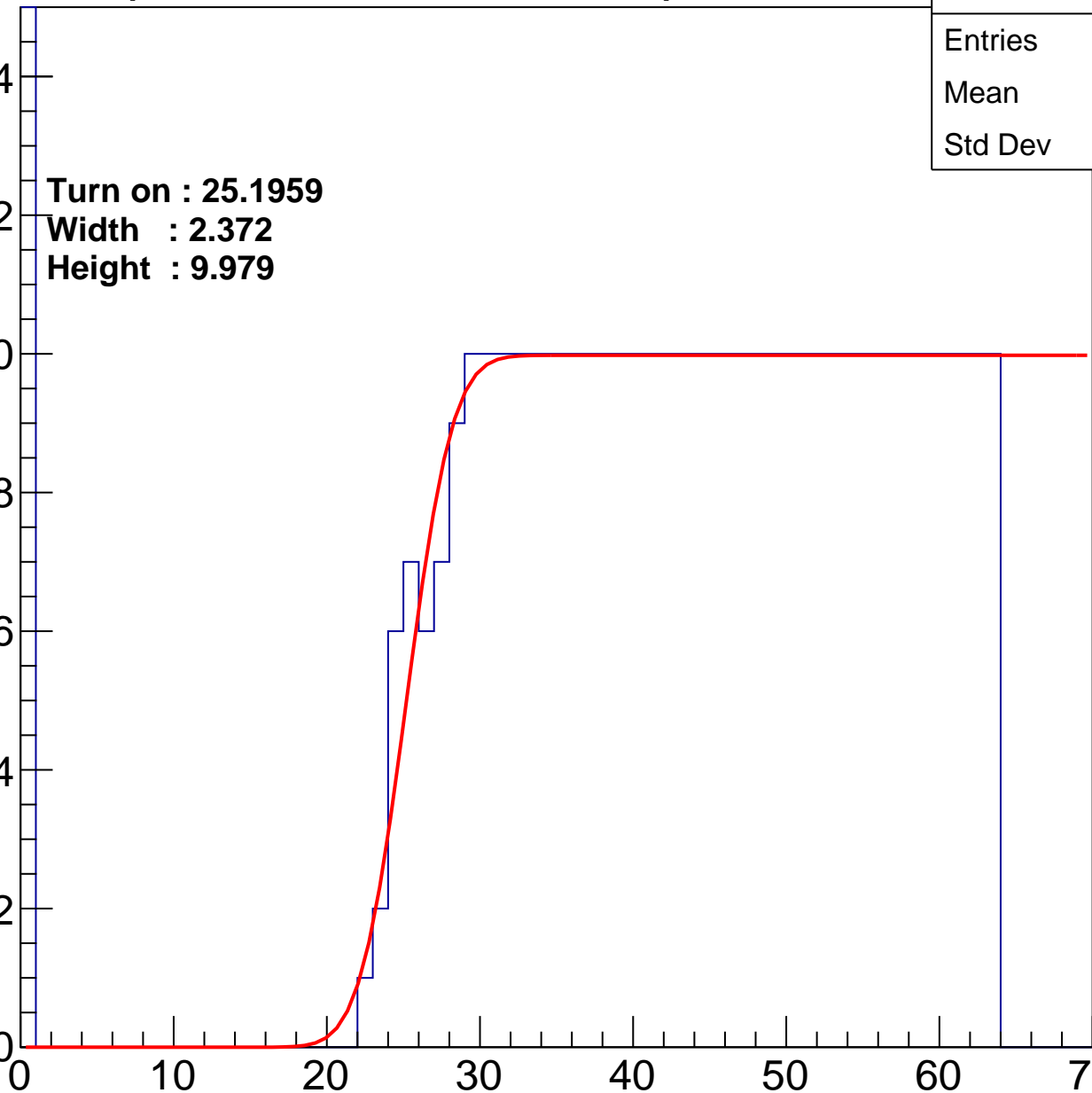
Width : 2.372

Height : 9.979

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch38

calib_packv5_041523_1651.root, FC#0, port C2

Entries	458
Mean	38.14
Std Dev	17.75

Turn on : 23.9120

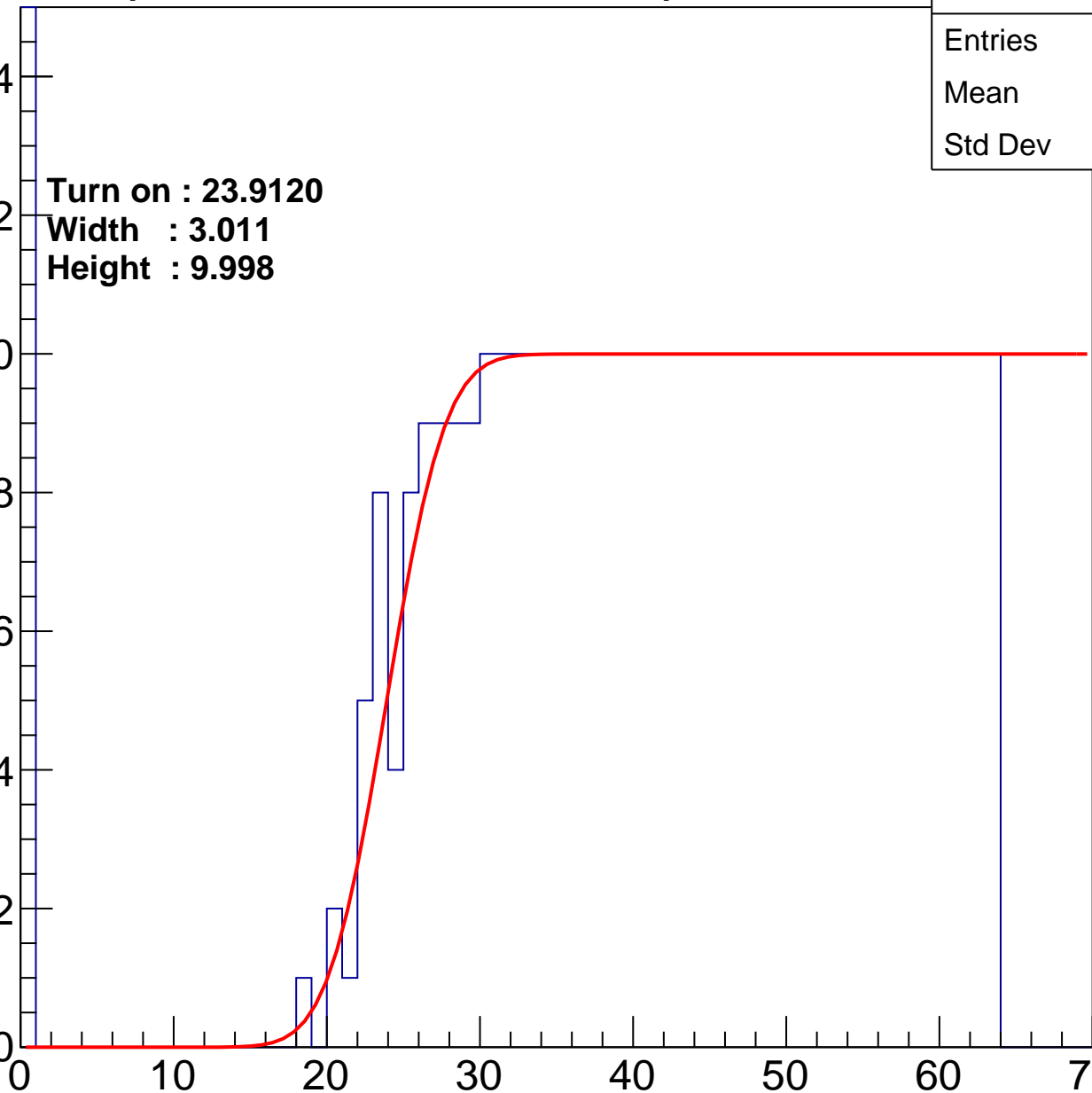
Width : 3.011

Height : 9.998

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch39

calib_packv5_041523_1651.root, FC#0, port C2

Entries	414
Mean	40.04
Std Dev	17.34

Turn on : 27.6075

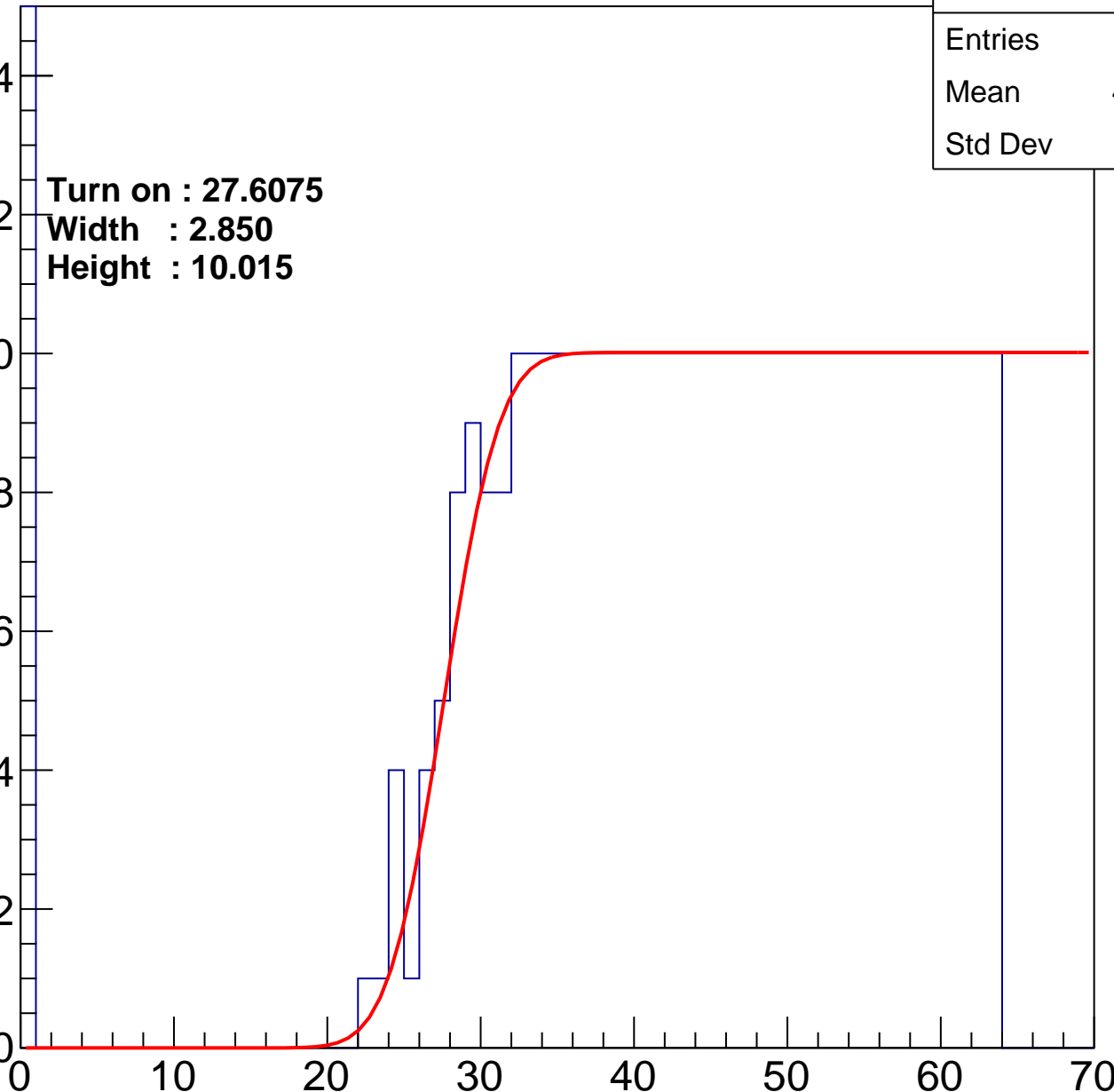
Width : 2.850

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch40

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	39.83
Std Dev	16.84

Turn on : 25.5588

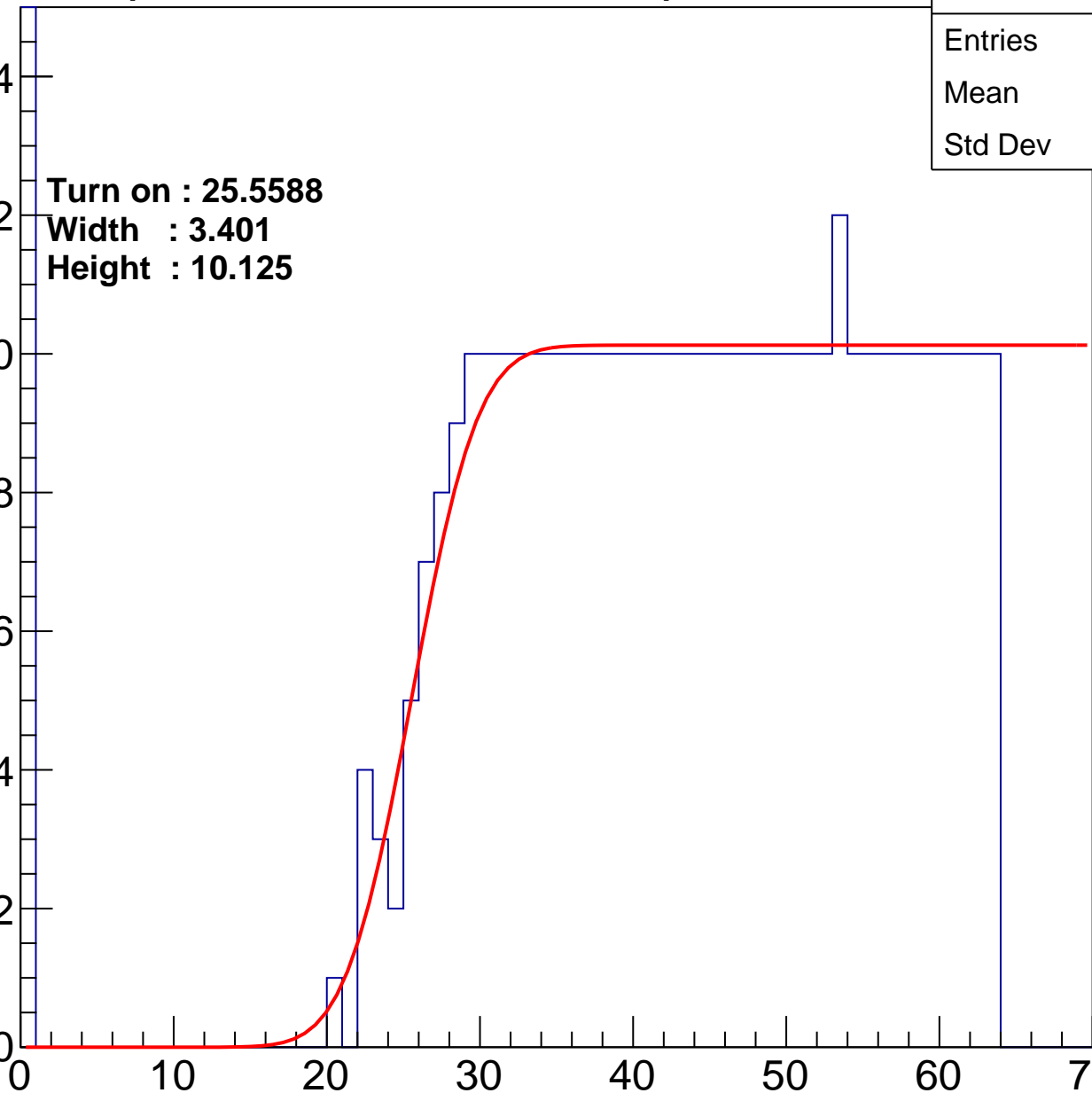
Width : 3.401

Height : 10.125

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch41

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	38.33
Std Dev	18.71

Turn on : 26.9328

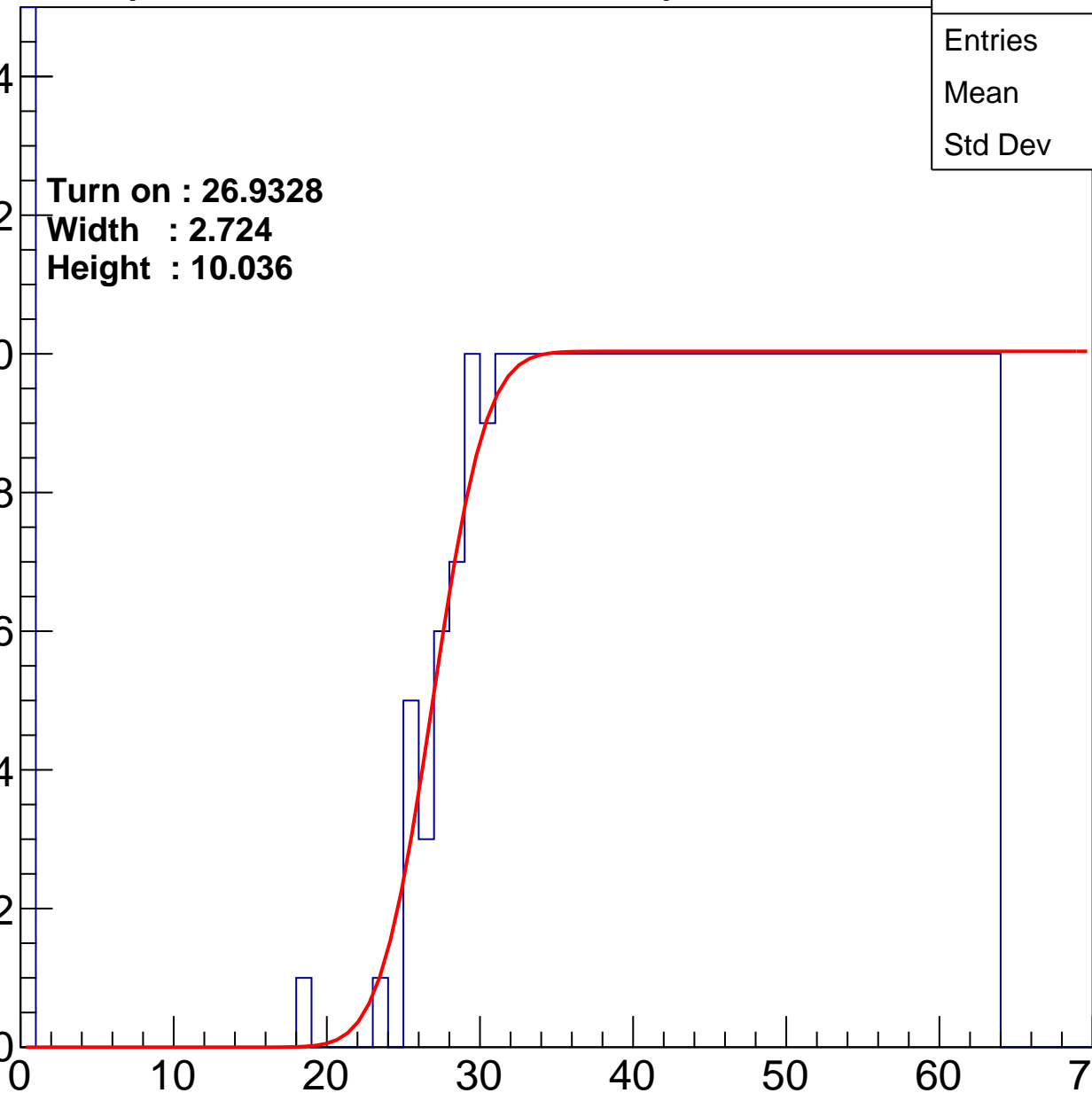
Width : 2.724

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch42

calib_packv5_041523_1651.root, FC#0, port C2

Entries	445
Mean	39
Std Dev	17.21

Turn on : 23.9406

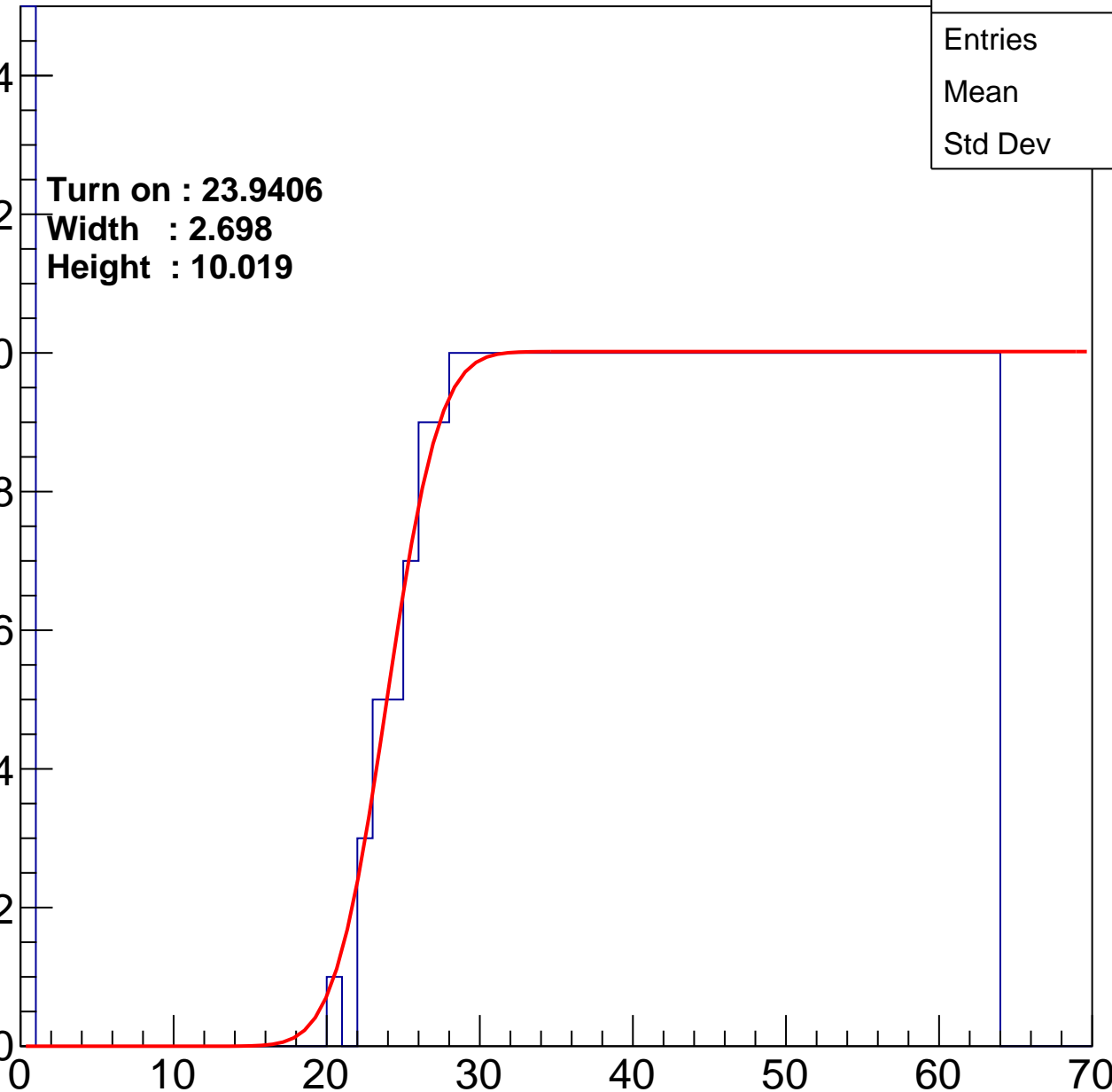
Width : 2.698

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch43

calib_packv5_041523_1651.root, FC#0, port C2

Entries	417
Mean	40.34
Std Dev	16.71

Turn on : 27.1850

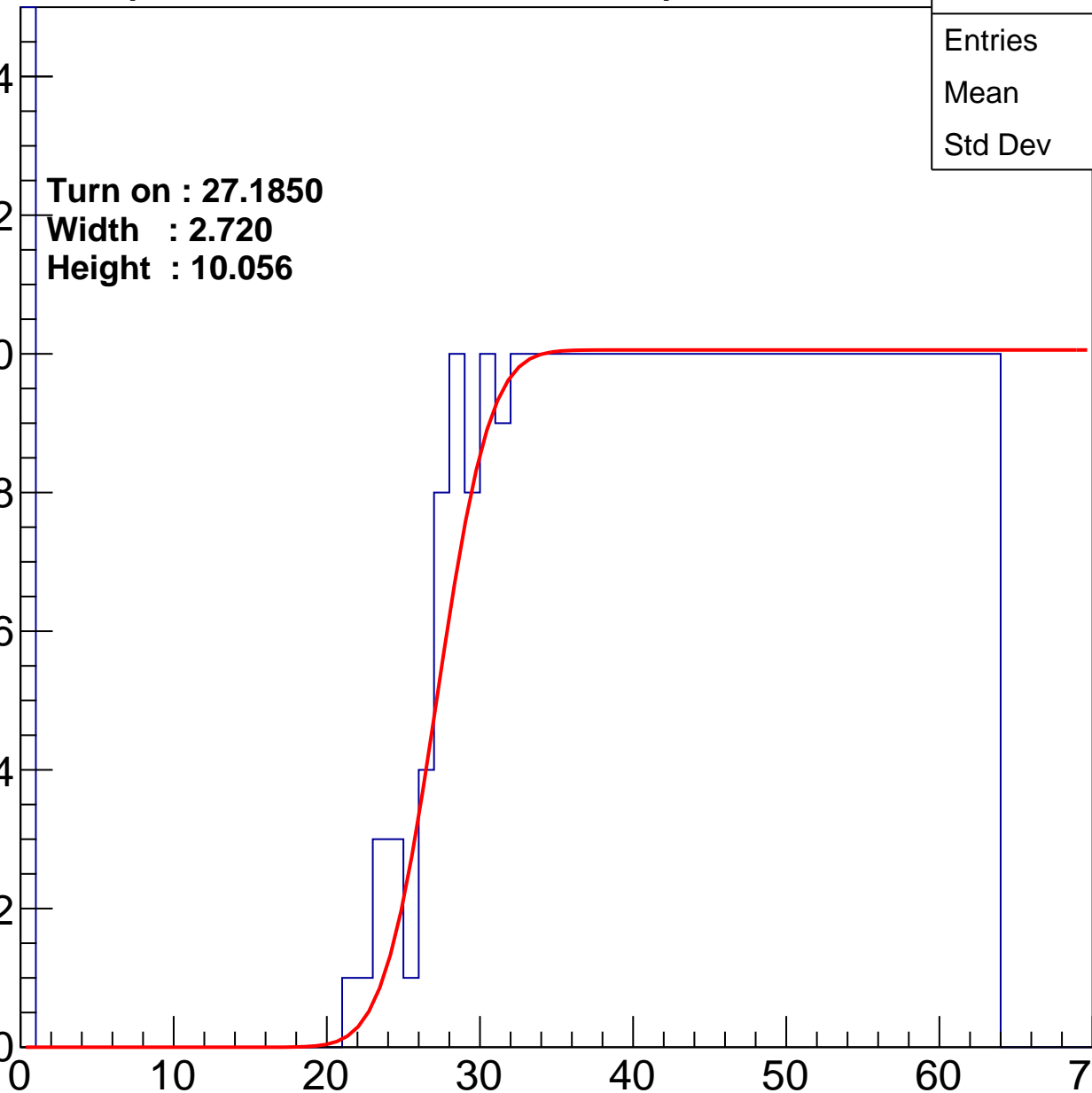
Width : 2.720

Height : 10.056

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch44

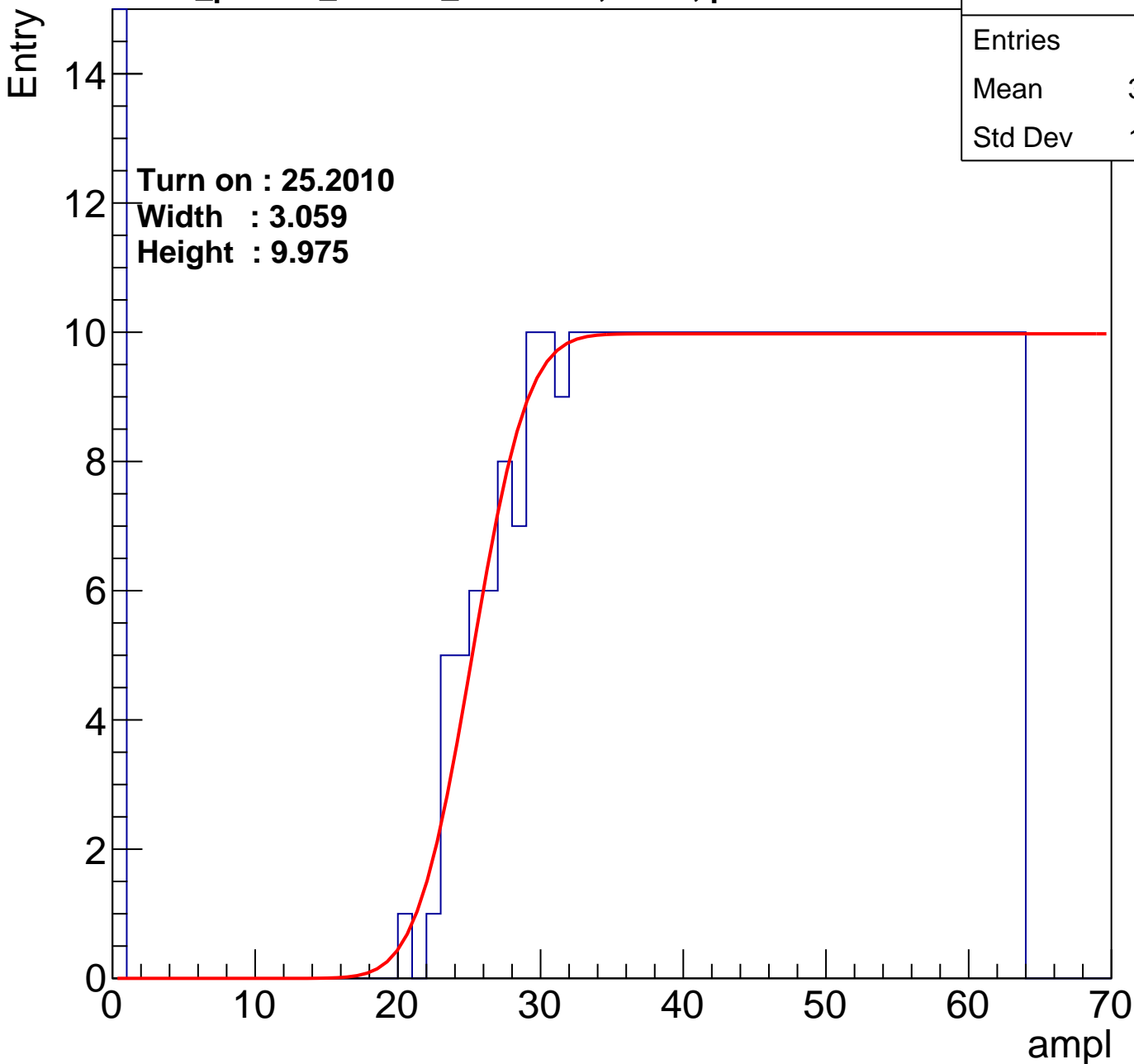
calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	39.68
Std Dev	16.96

Turn on : 25.2010

Width : 3.059

Height : 9.975



B1L103S, U24-ch45

calib_packv5_041523_1651.root, FC#0, port C2

Entries	414
Mean	40.17
Std Dev	17.14

Turn on : 26.8482

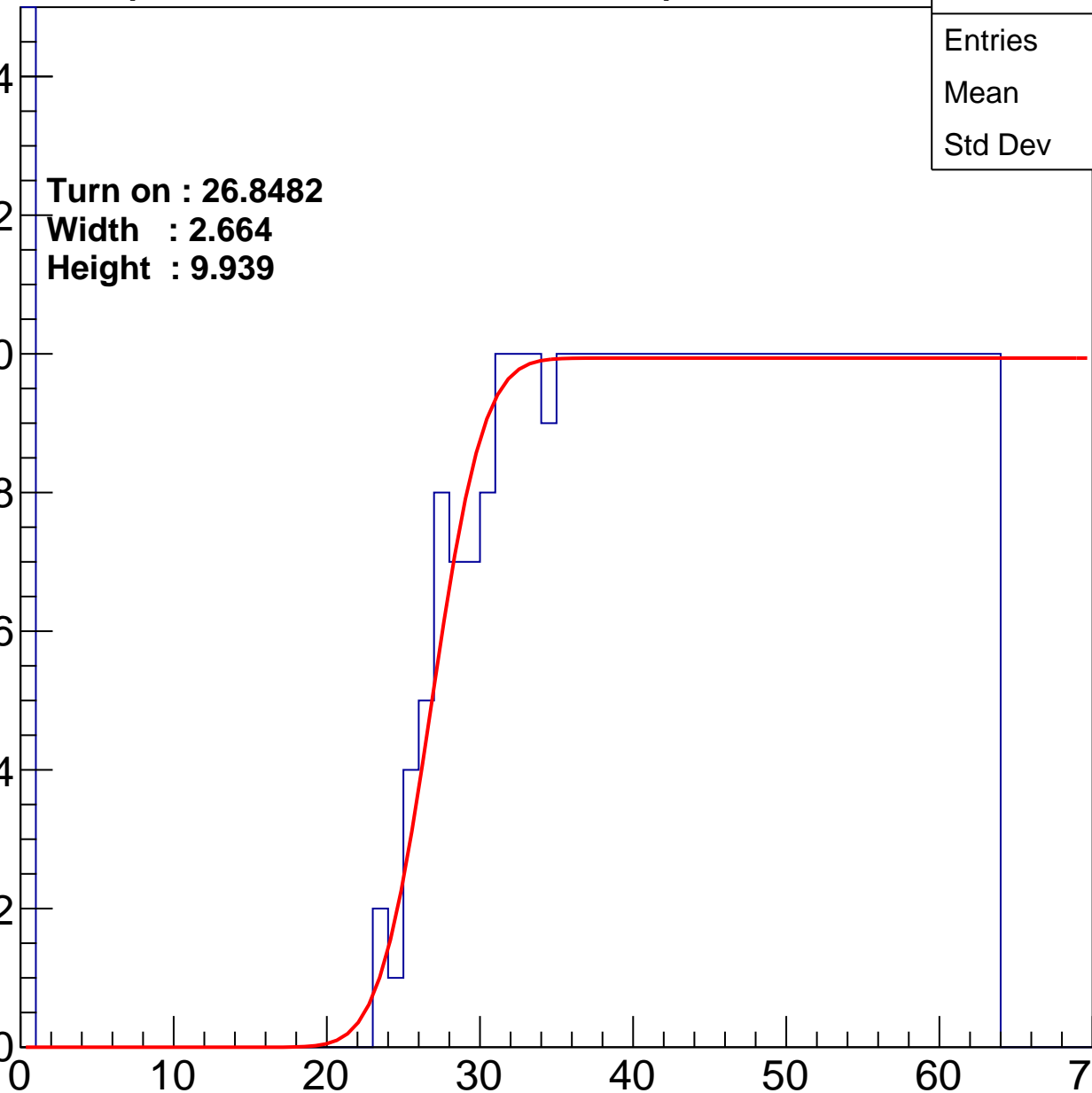
Width : 2.664

Height : 9.939

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch46

calib_packv5_041523_1651.root, FC#0, port C2

Entries	444
Mean	38.57
Std Dev	17.9

Turn on : 25.5070

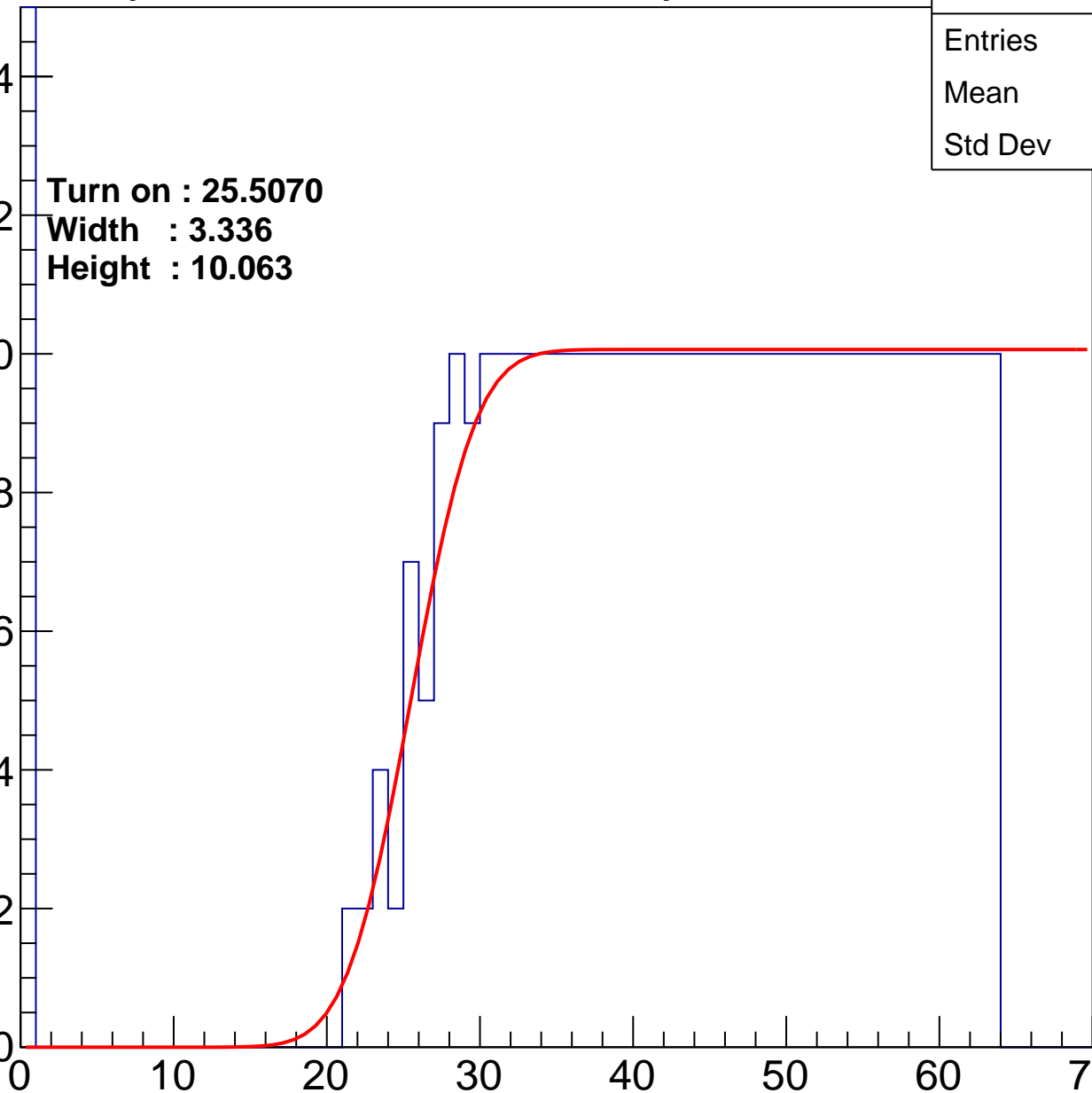
Width : 3.336

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch47

calib_packv5_041523_1651.root, FC#0, port C2

Entries	447
Mean	38.14
Std Dev	18.35

Turn on : 25.6446

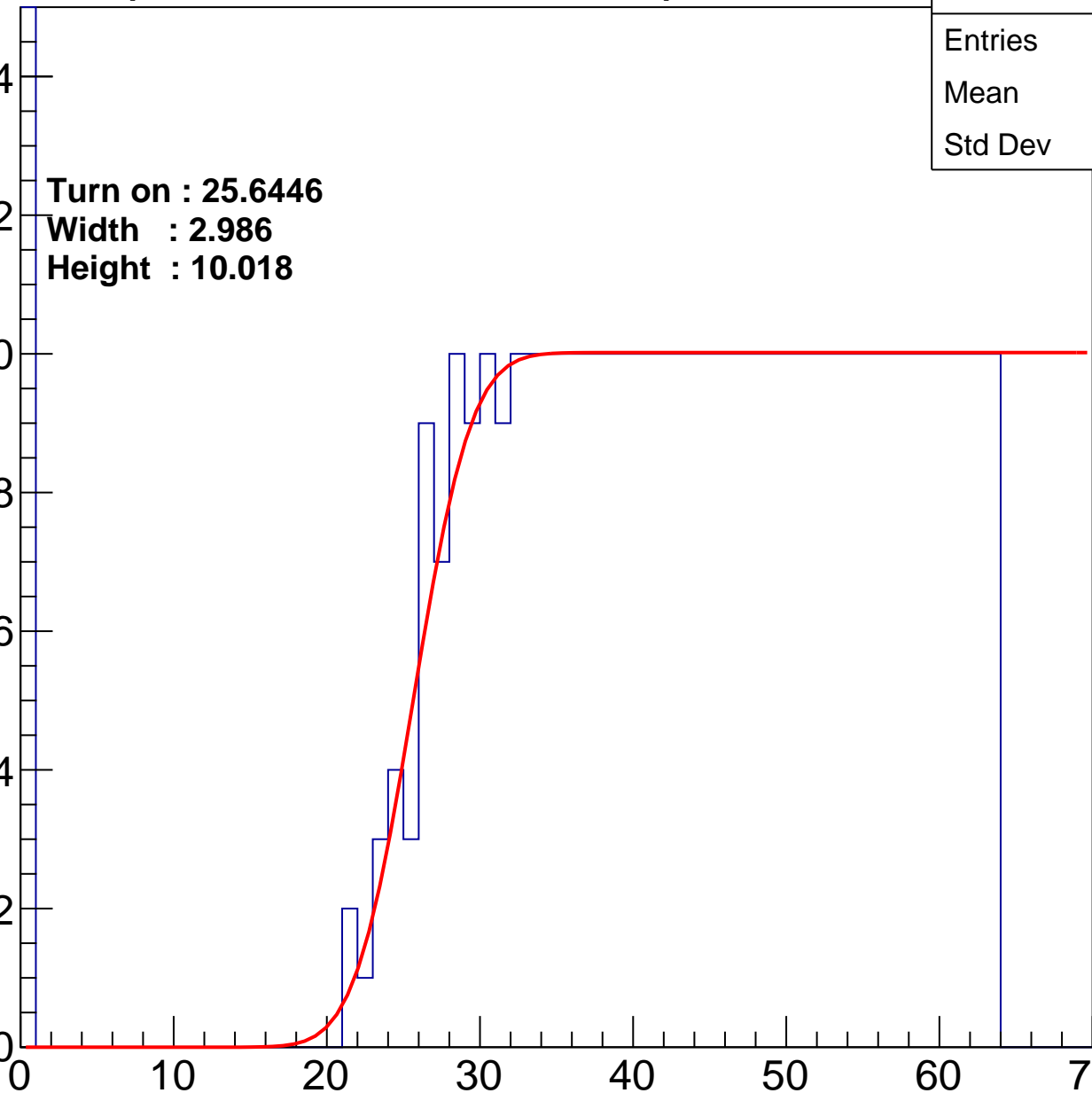
Width : 2.986

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch48

calib_packv5_041523_1651.root, FC#0, port C2

Entries	450
Mean	38.68
Std Dev	17.39

Turn on : 23.8689

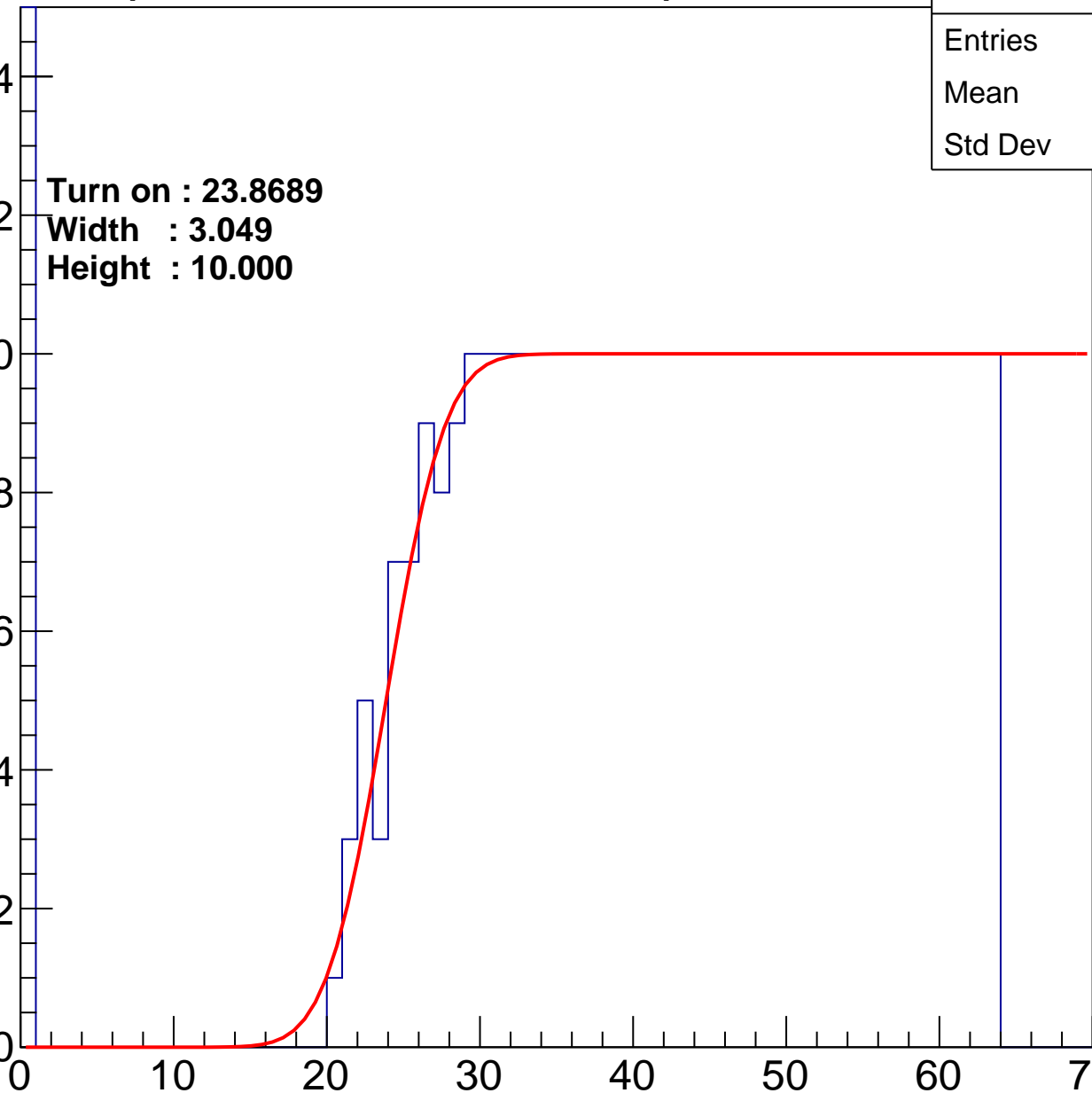
Width : 3.049

Height : 10.000

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch49

calib_packv5_041523_1651.root, FC#0, port C2

Entries	427
Mean	39.4
Std Dev	17.6

Turn on : 26.3201

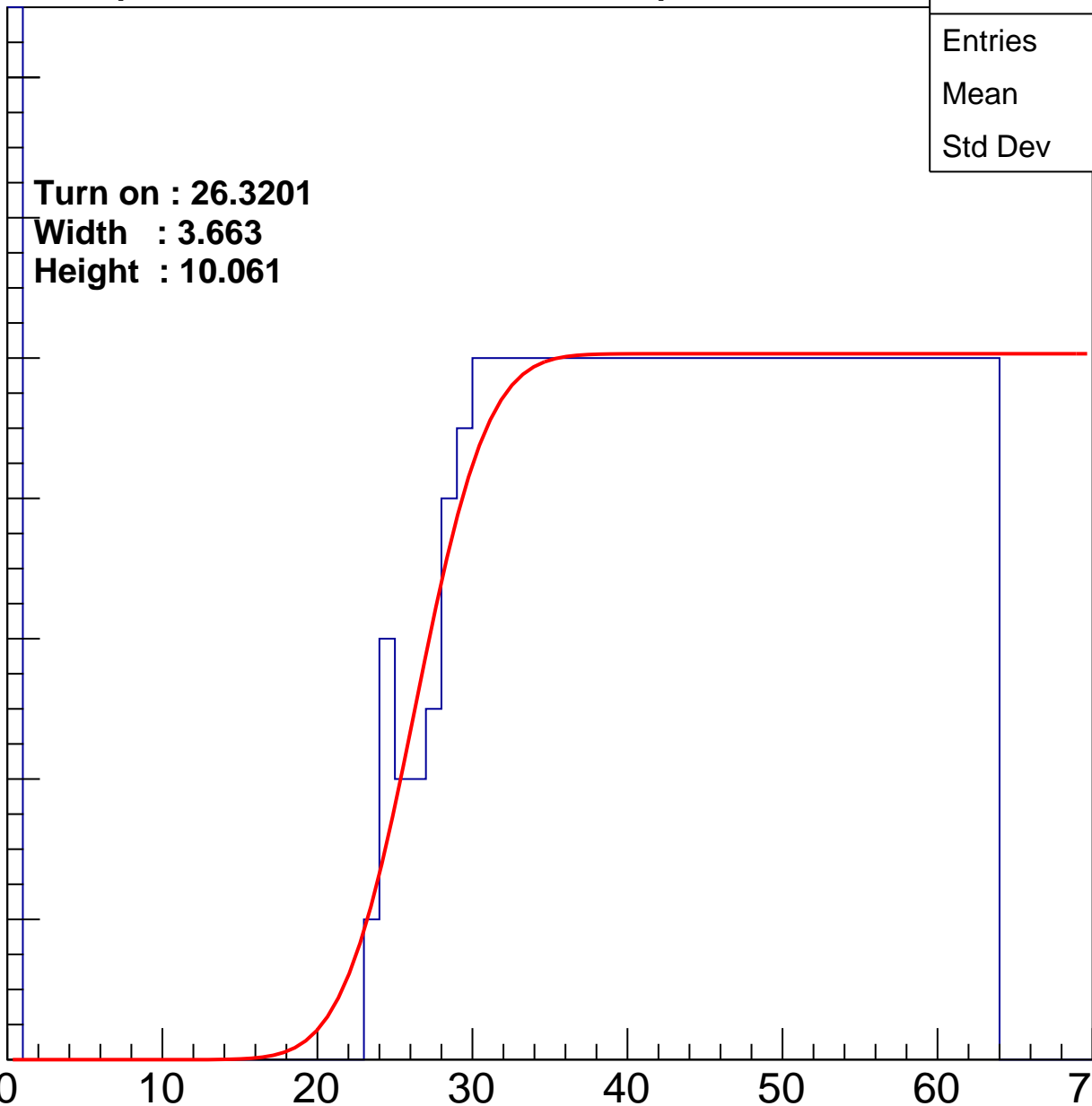
Width : 3.663

Height : 10.061

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch50

calib_packv5_041523_1651.root, FC#0, port C2

Entries	452
Mean	37.96
Std Dev	18.37

Turn on : 25.2788

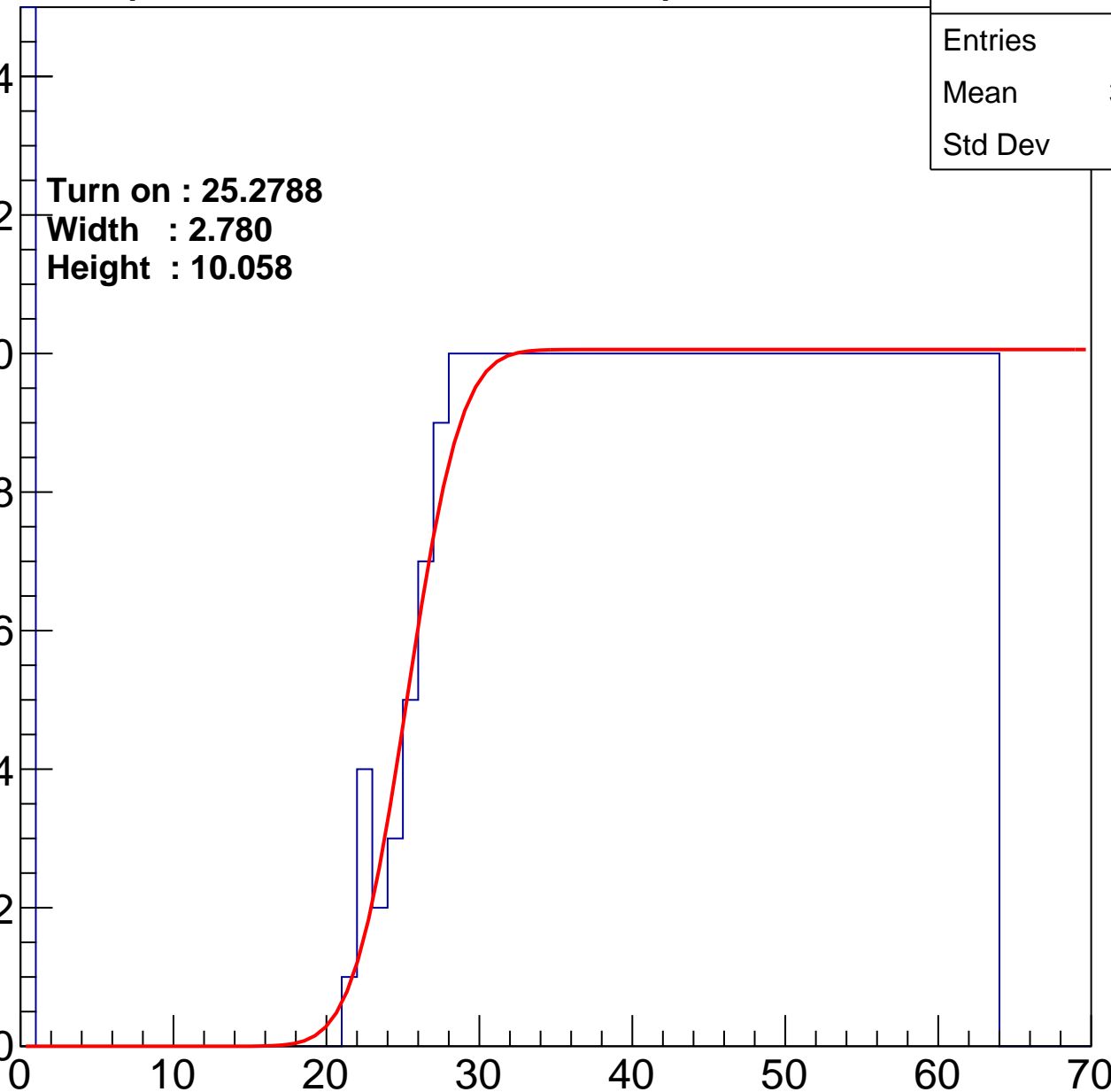
Width : 2.780

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch51

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	39.52
Std Dev	17.12

Turn on : 25.3542

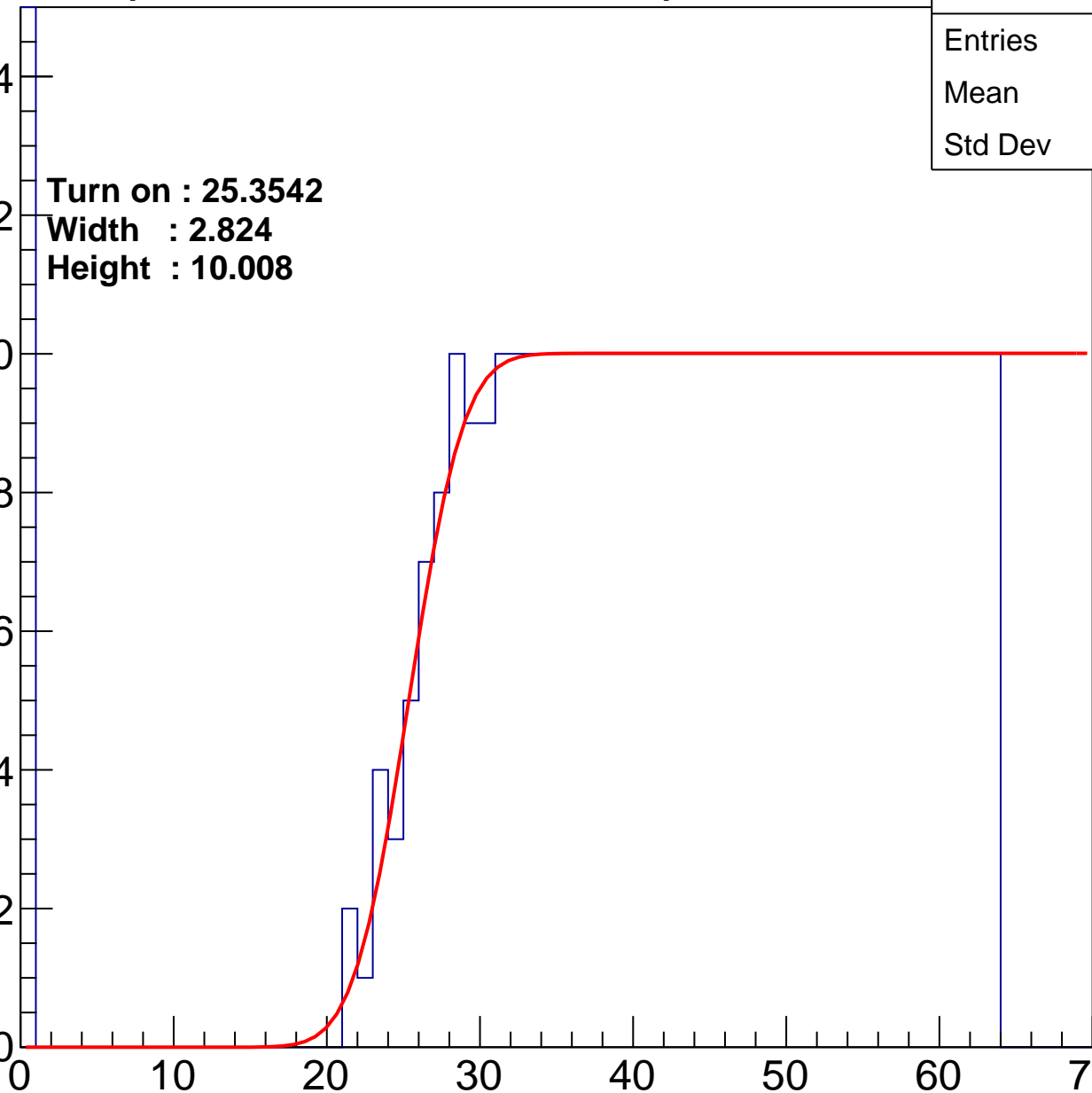
Width : 2.824

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch52

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	39.25
Std Dev	17.27

Turn on : 25.3645

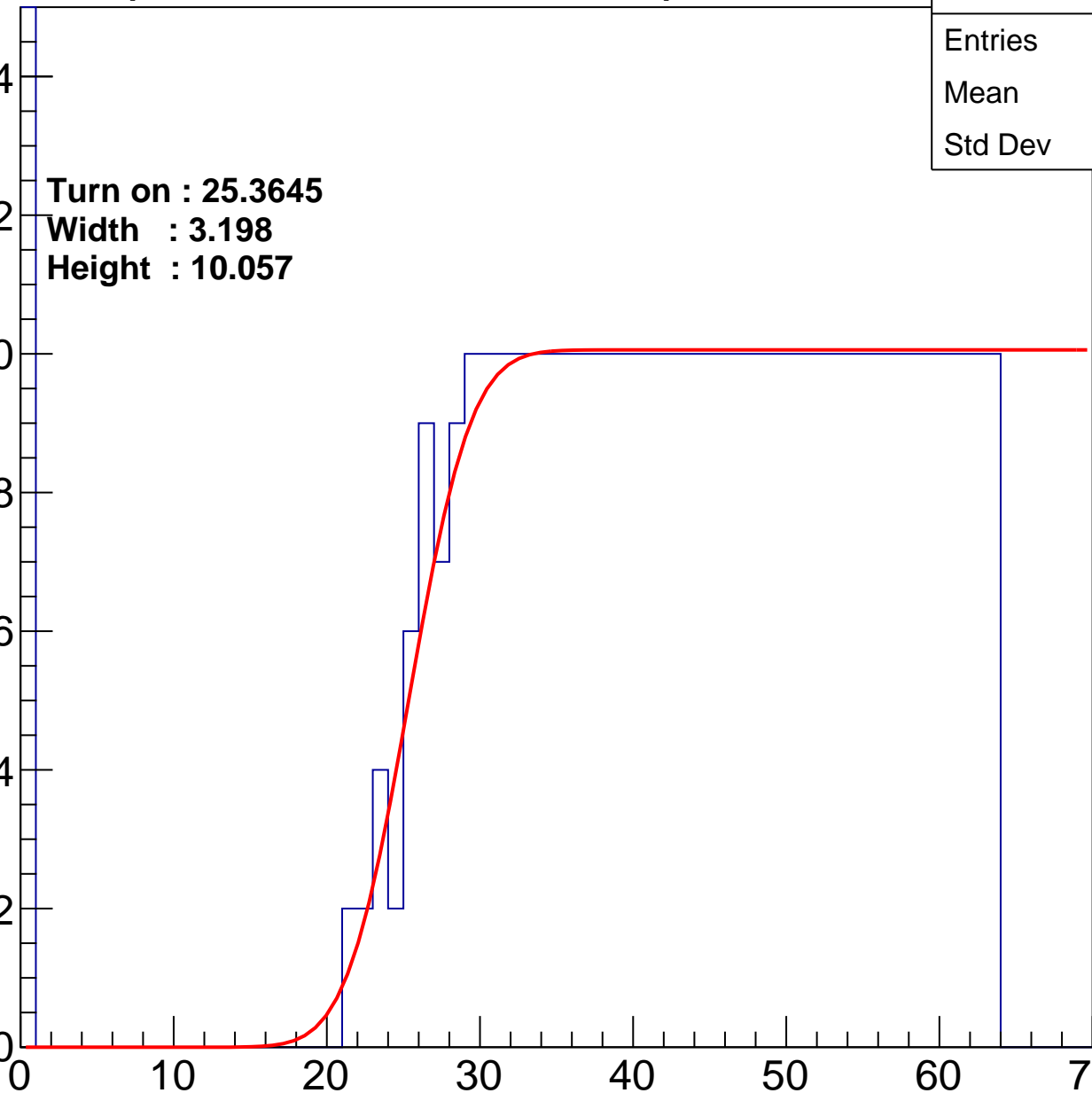
Width : 3.198

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch53

calib_packv5_041523_1651.root, FC#0, port C2

Entries	419
Mean	40.46
Std Dev	16.39

Turn on : 25.9391

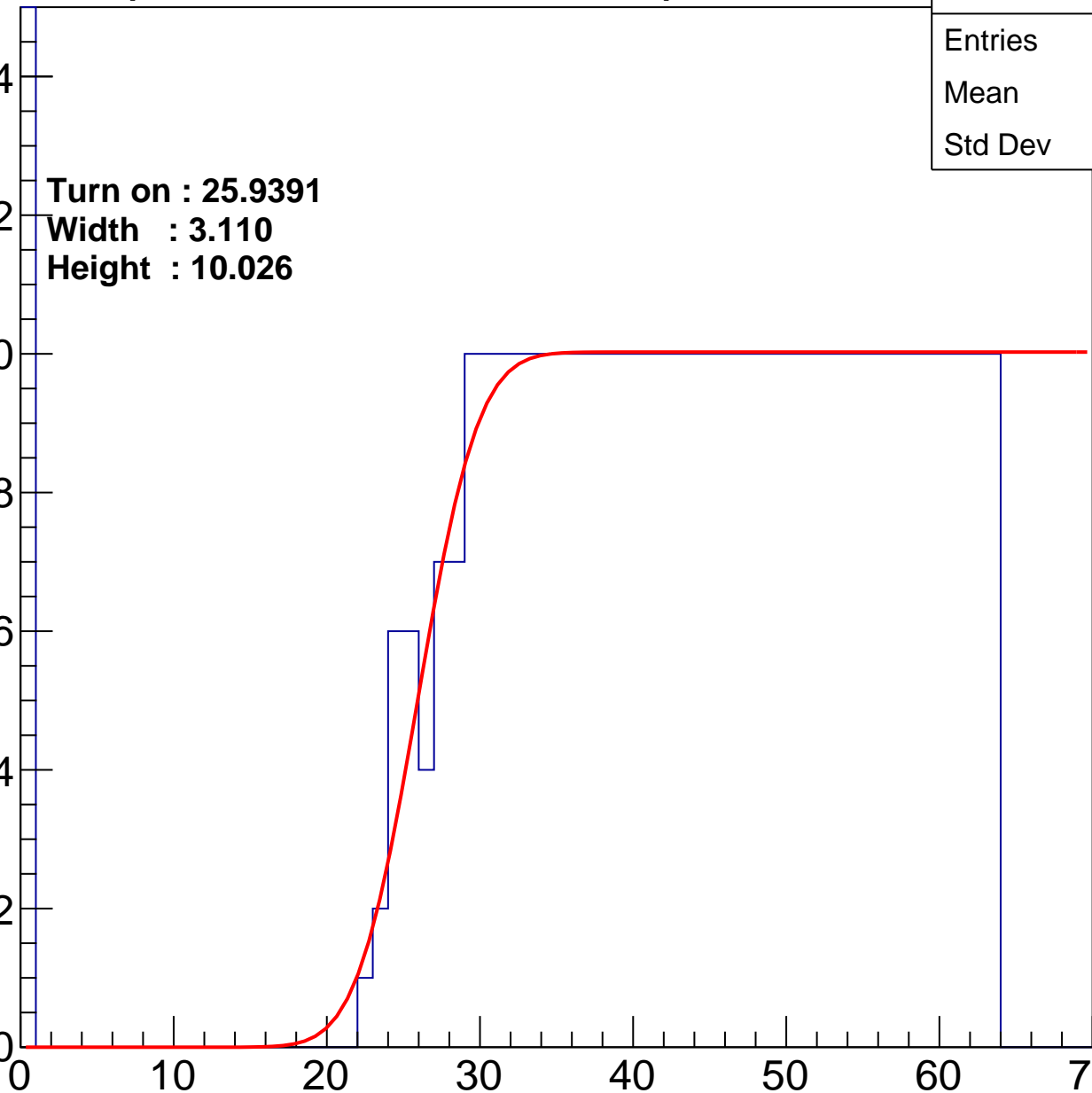
Width : 3.110

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch54

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	39.08
Std Dev	17.87

Turn on : 27.0400

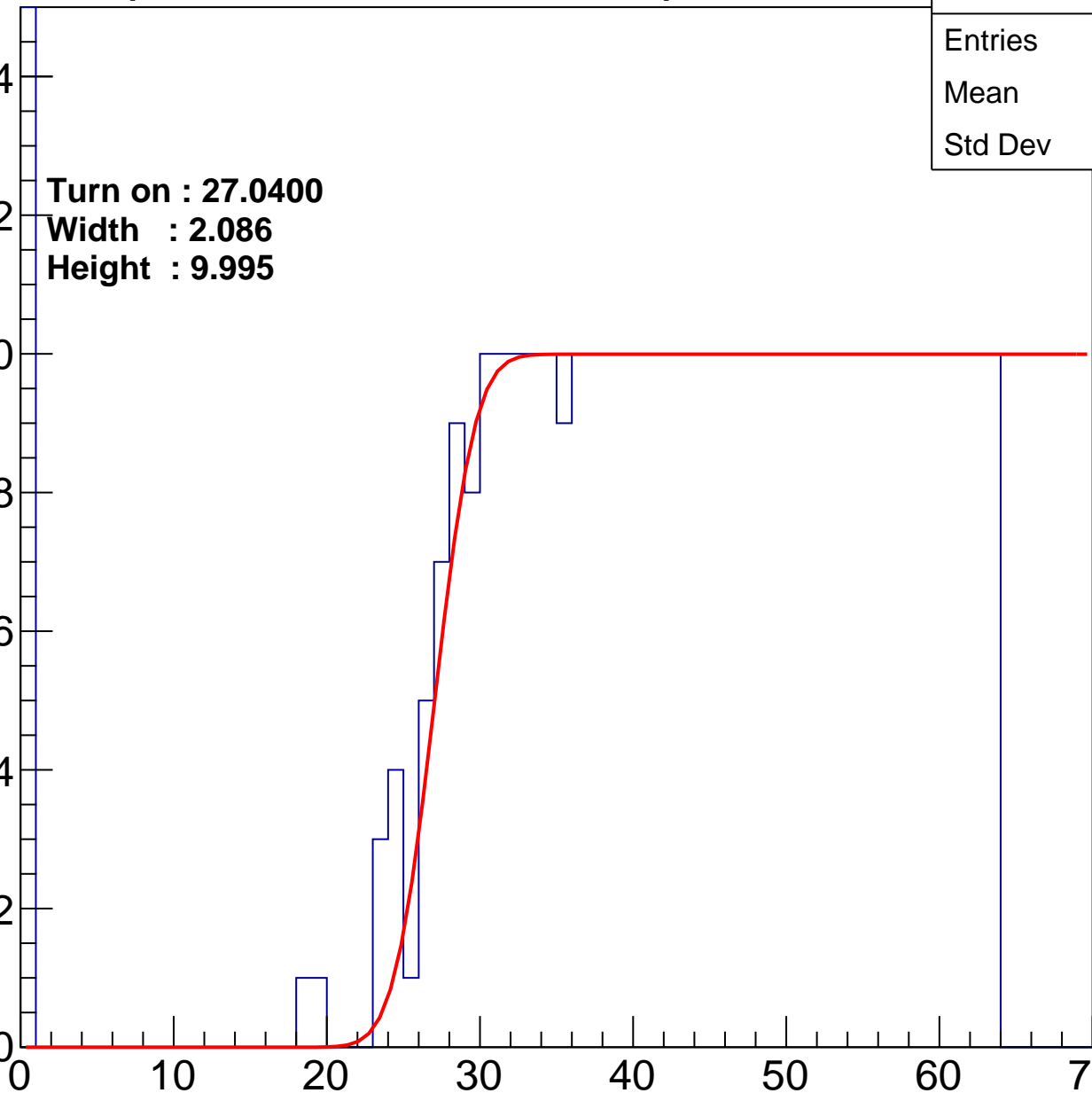
Width : 2.086

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch55

calib_packv5_041523_1651.root, FC#0, port C2

Entries	424
Mean	39.43
Std Dev	17.72

Turn on : 26.8826

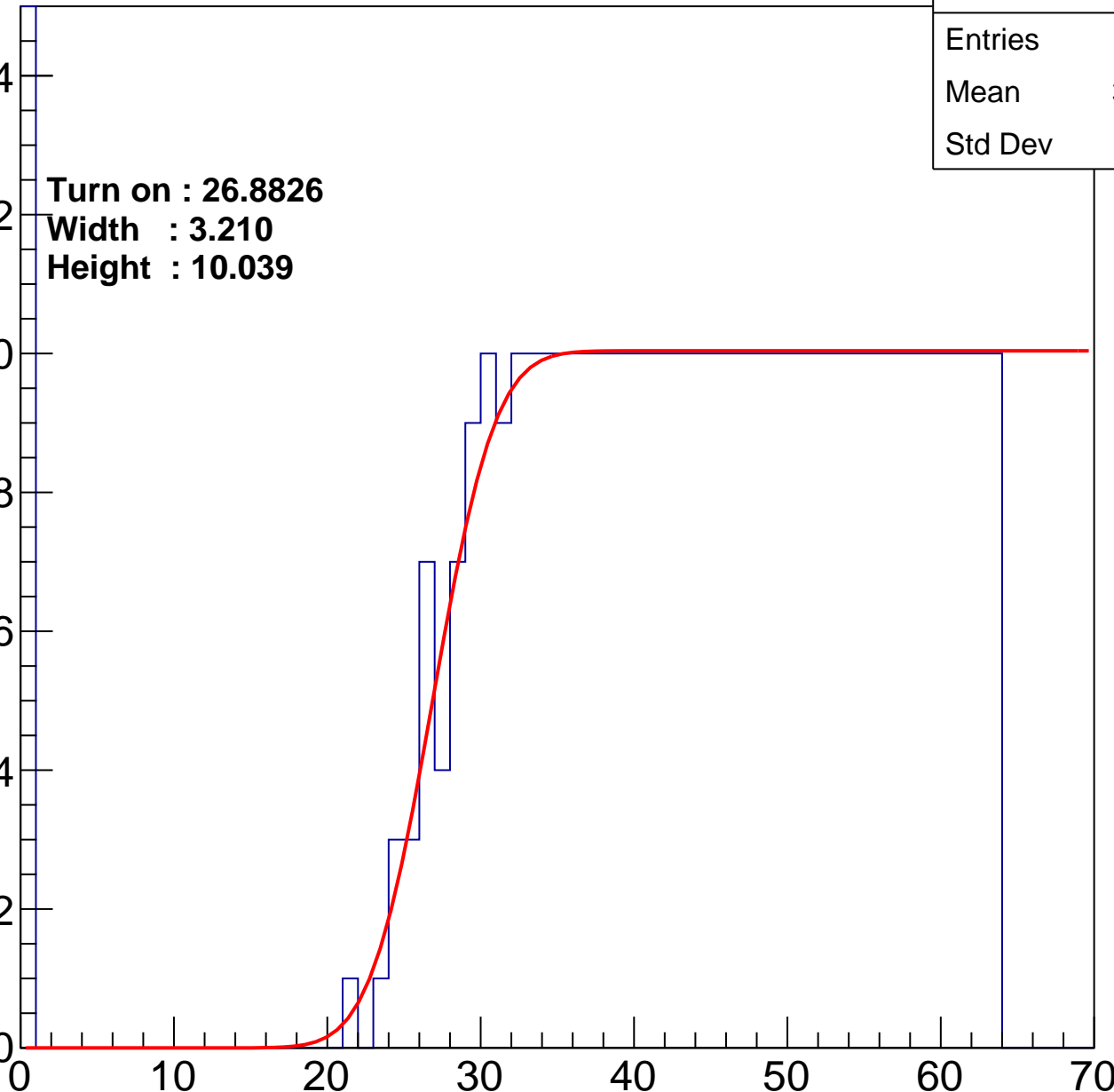
Width : 3.210

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch56

calib_packv5_041523_1651.root, FC#0, port C2

Entries	449
Mean	38.57
Std Dev	17.62

Turn on : 24.1428

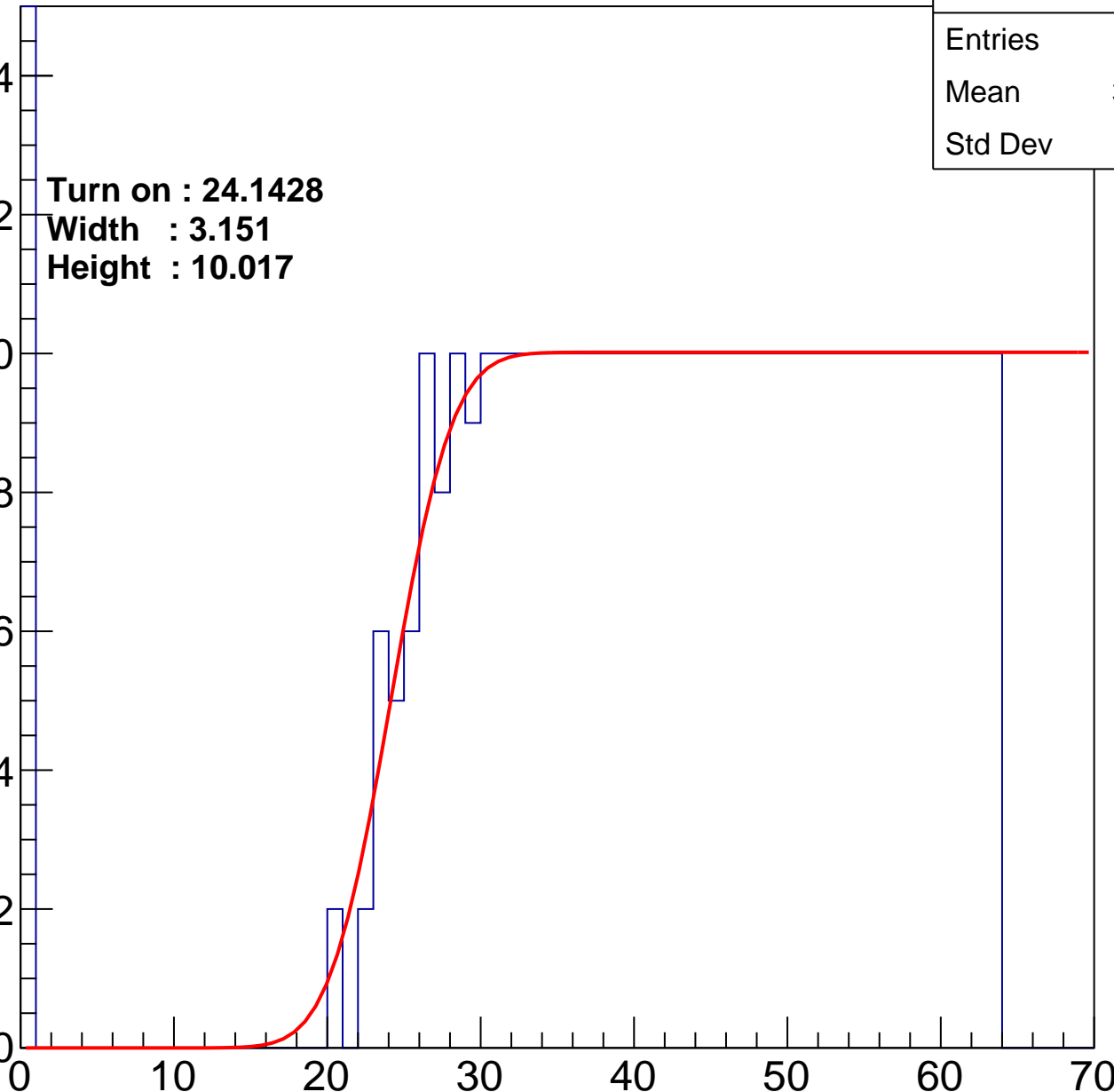
Width : 3.151

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch57

calib_packv5_041523_1651.root, FC#0, port C2

Entries	416
Mean	40.22
Std Dev	16.94

Turn on : 26.9033

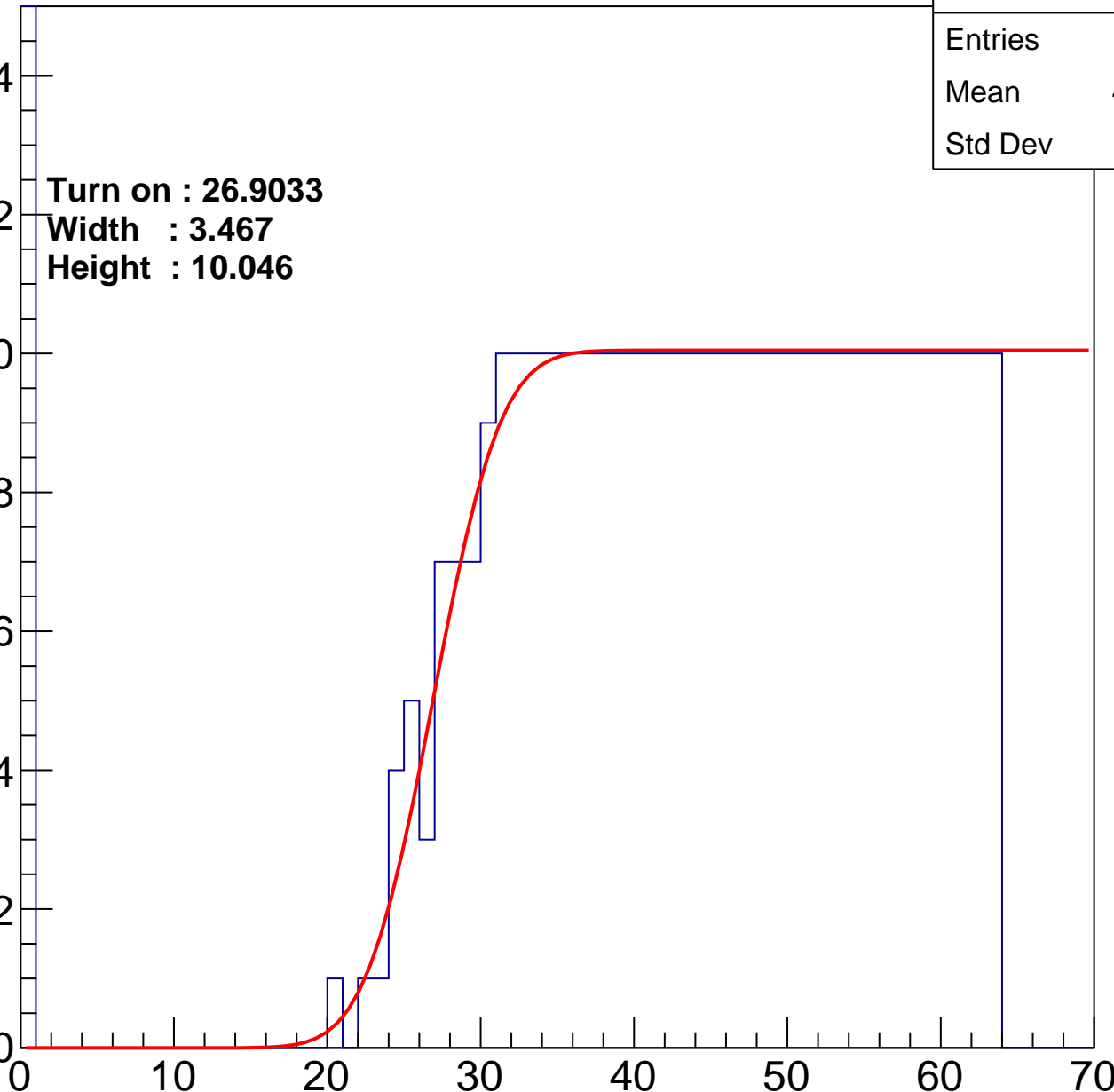
Width : 3.467

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch58

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	39.04
Std Dev	17.42

Turn on : 25.2779

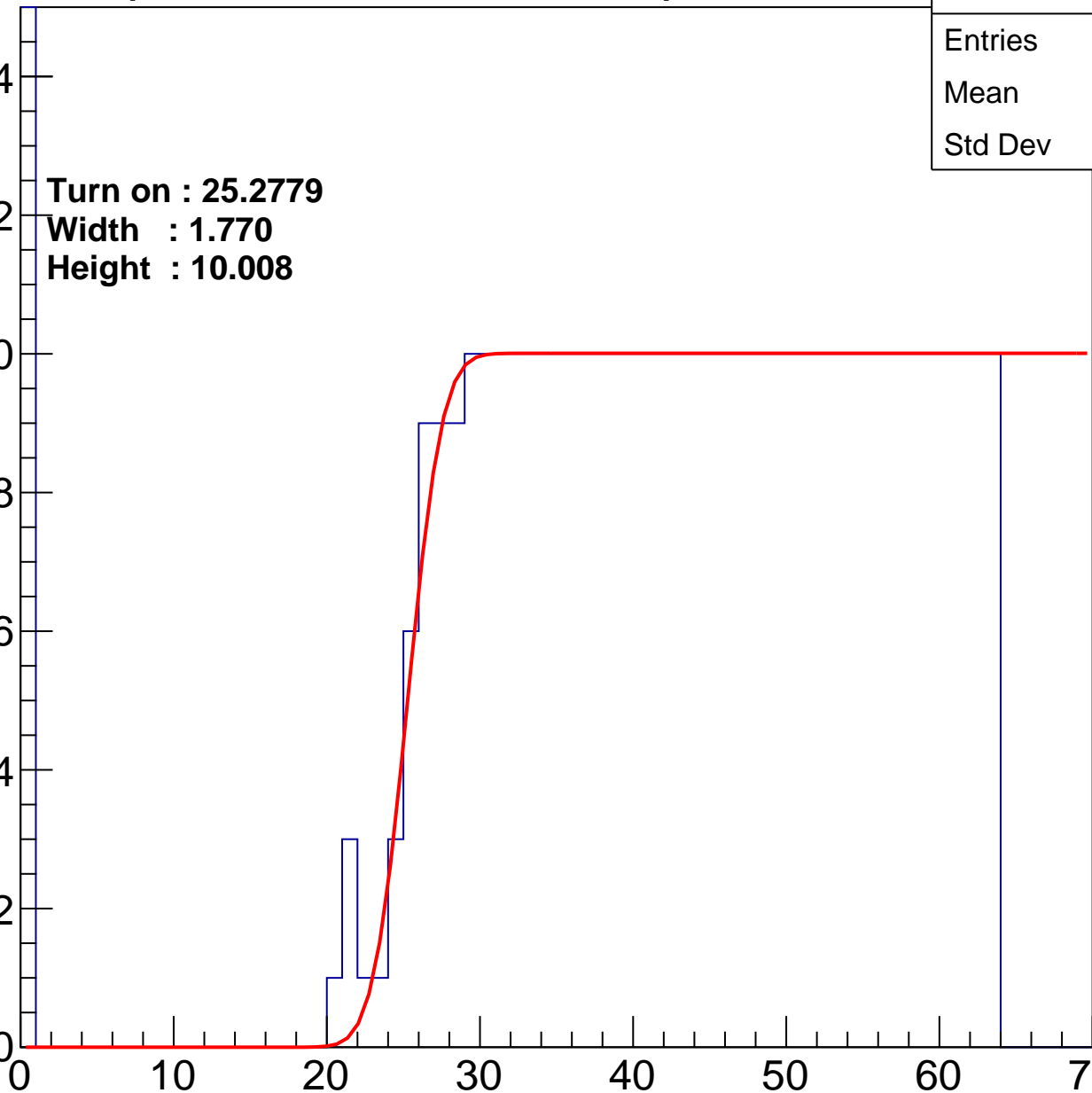
Width : 1.770

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch59

calib_packv5_041523_1651.root, FC#0, port C2

Entries	441
Mean	38.36
Std Dev	18.34

Turn on : 26.2105

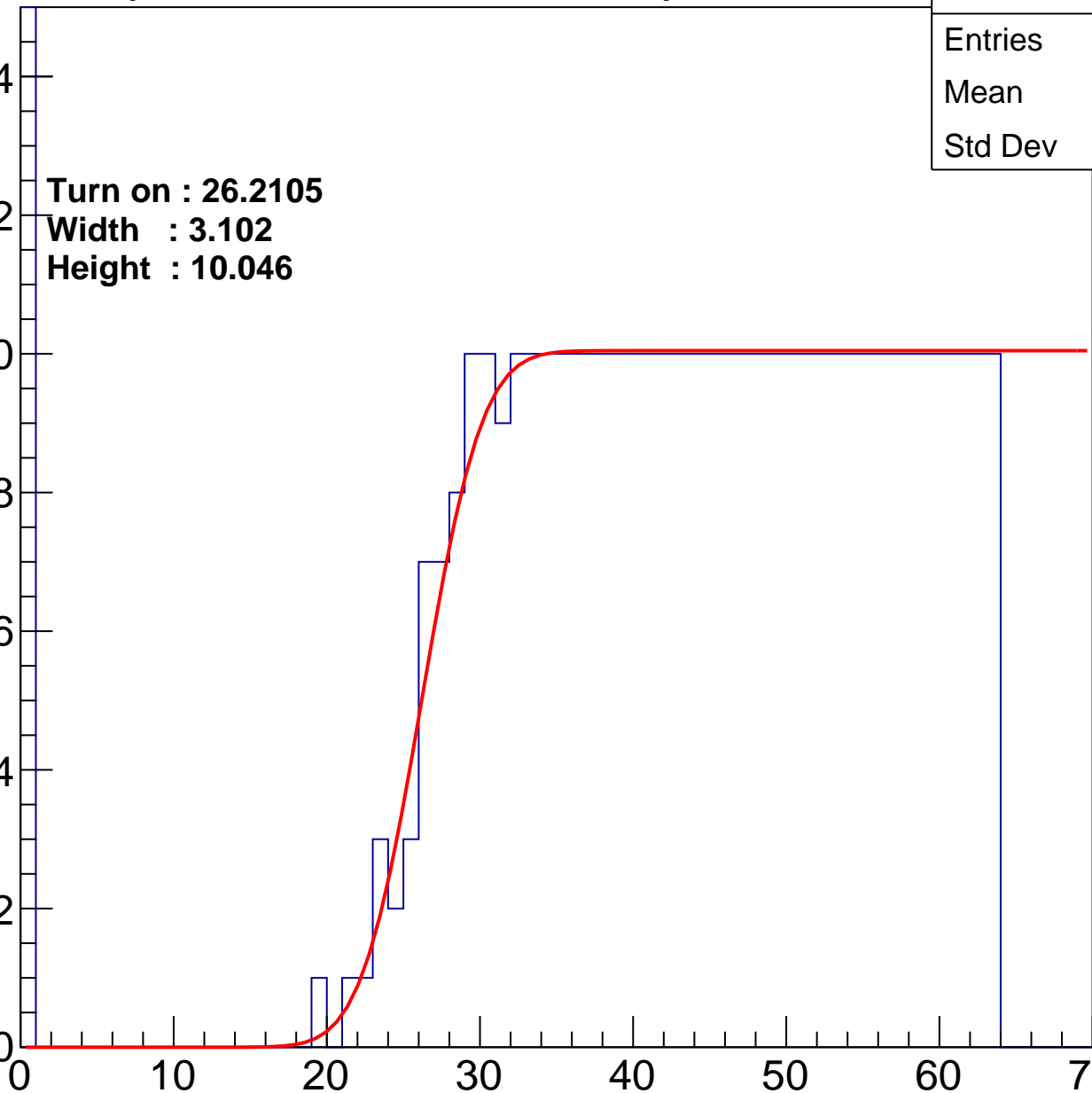
Width : 3.102

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch60

calib_packv5_041523_1651.root, FC#0, port C2

Entries	443
Mean	38.49
Std Dev	18.07

Turn on : 25.3166

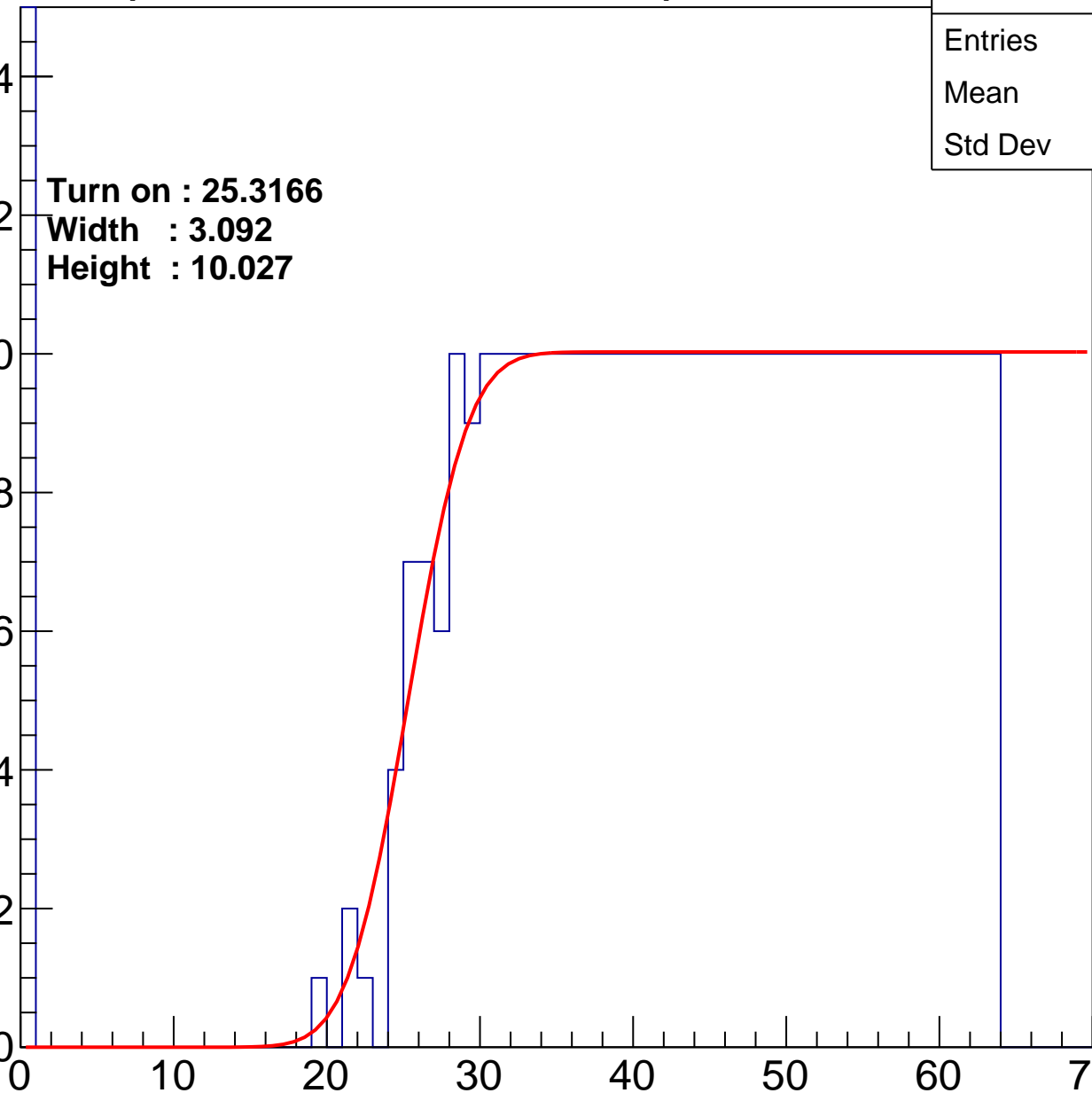
Width : 3.092

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch61

calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.29
Std Dev	17.69

Turn on : 26.1685

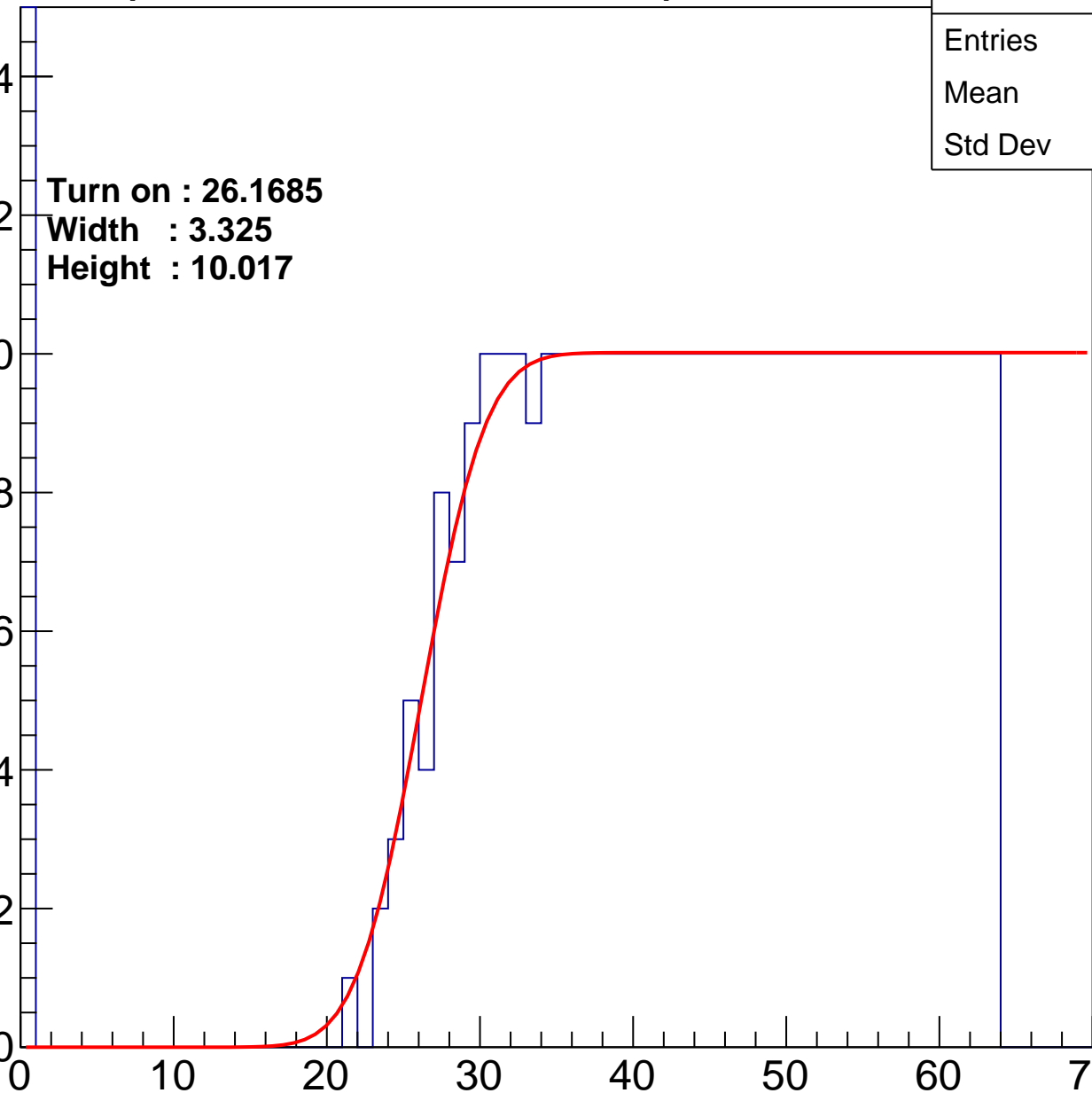
Width : 3.325

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch62

calib_packv5_041523_1651.root, FC#0, port C2

Entries	448
Mean	37.67
Std Dev	18.9

Turn on : 26.4512

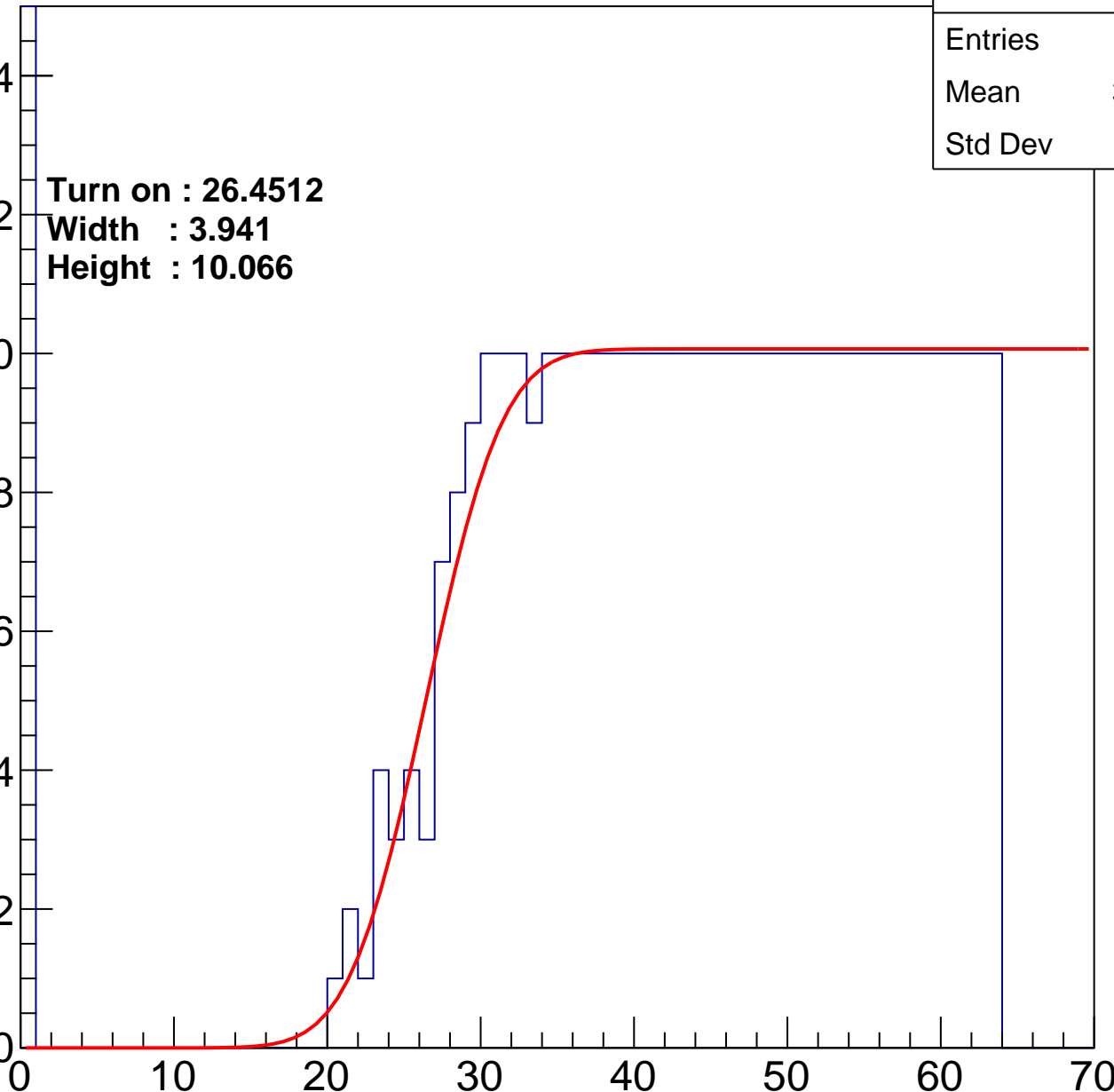
Width : 3.941

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch63

calib_packv5_041523_1651.root, FC#0, port C2

Entries	425
Mean	39.56
Std Dev	17.45

Turn on : 26.0233

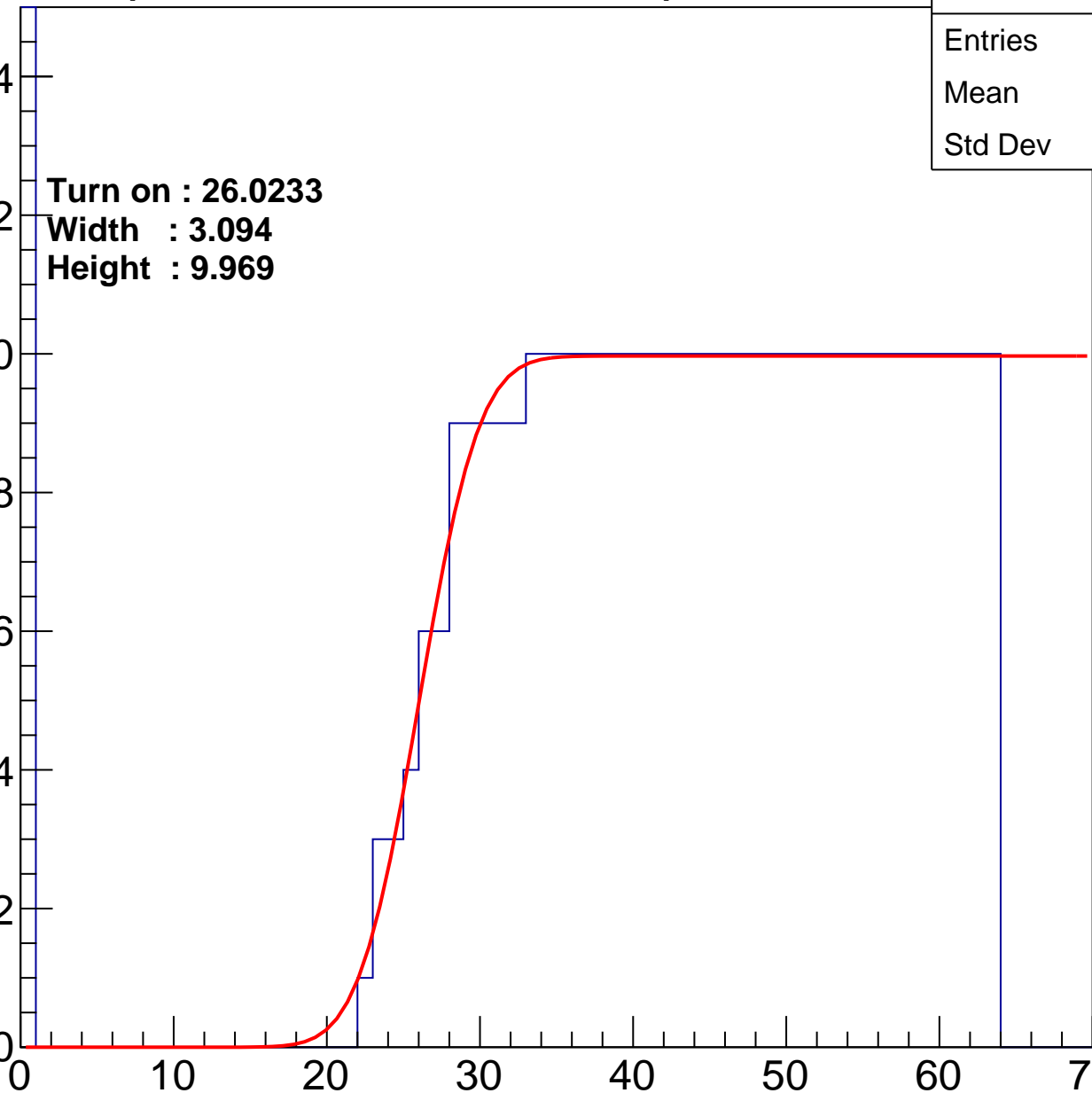
Width : 3.094

Height : 9.969

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch64

calib_packv5_041523_1651.root, FC#0, port C2

Entries	456
Mean	37.71
Std Dev	18.5

Turn on : 25.1010

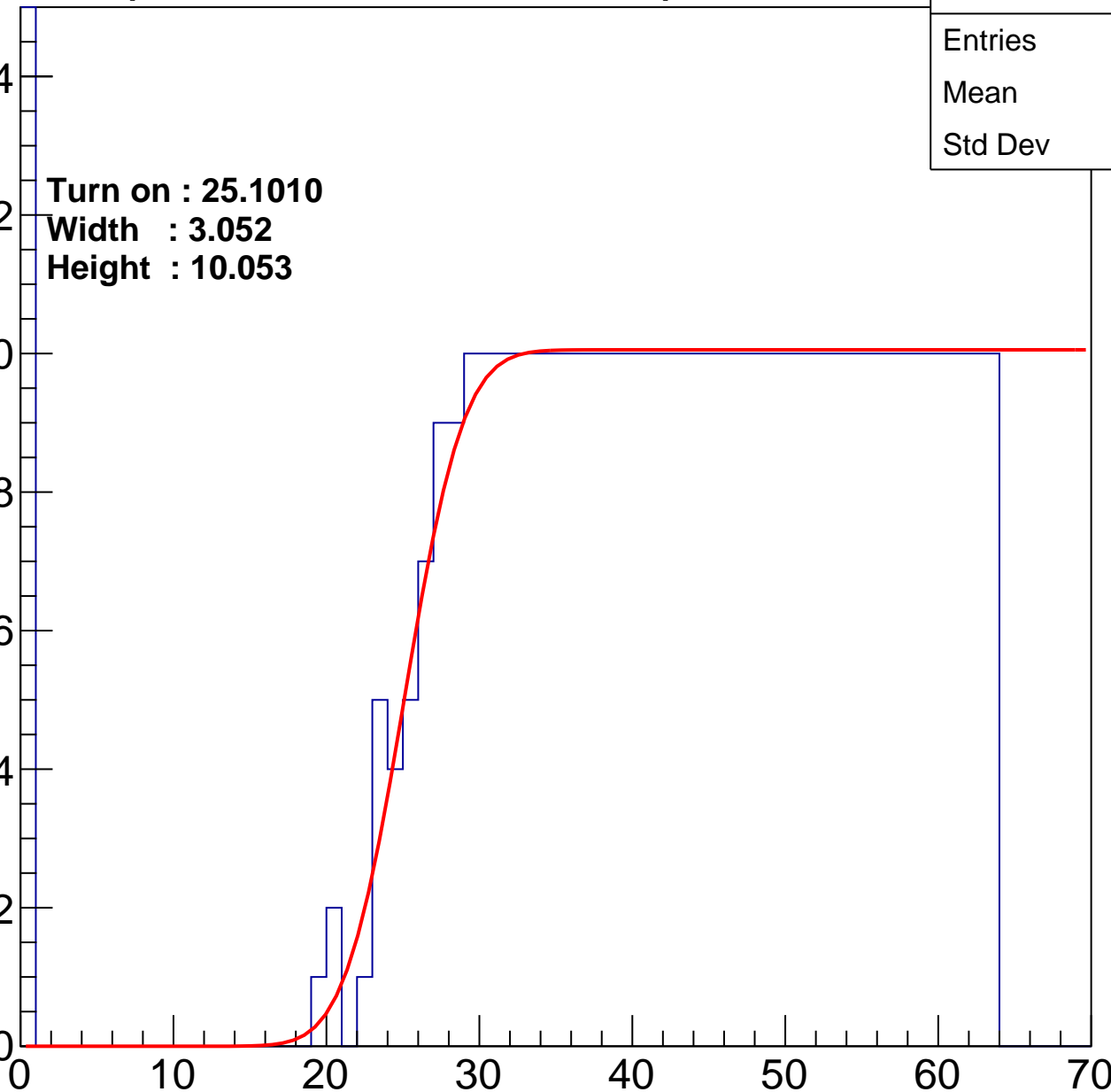
Width : 3.052

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch65

calib_packv5_041523_1651.root, FC#0, port C2

Entries	449
Mean	38.05
Std Dev	18.39

Turn on : 25.8094

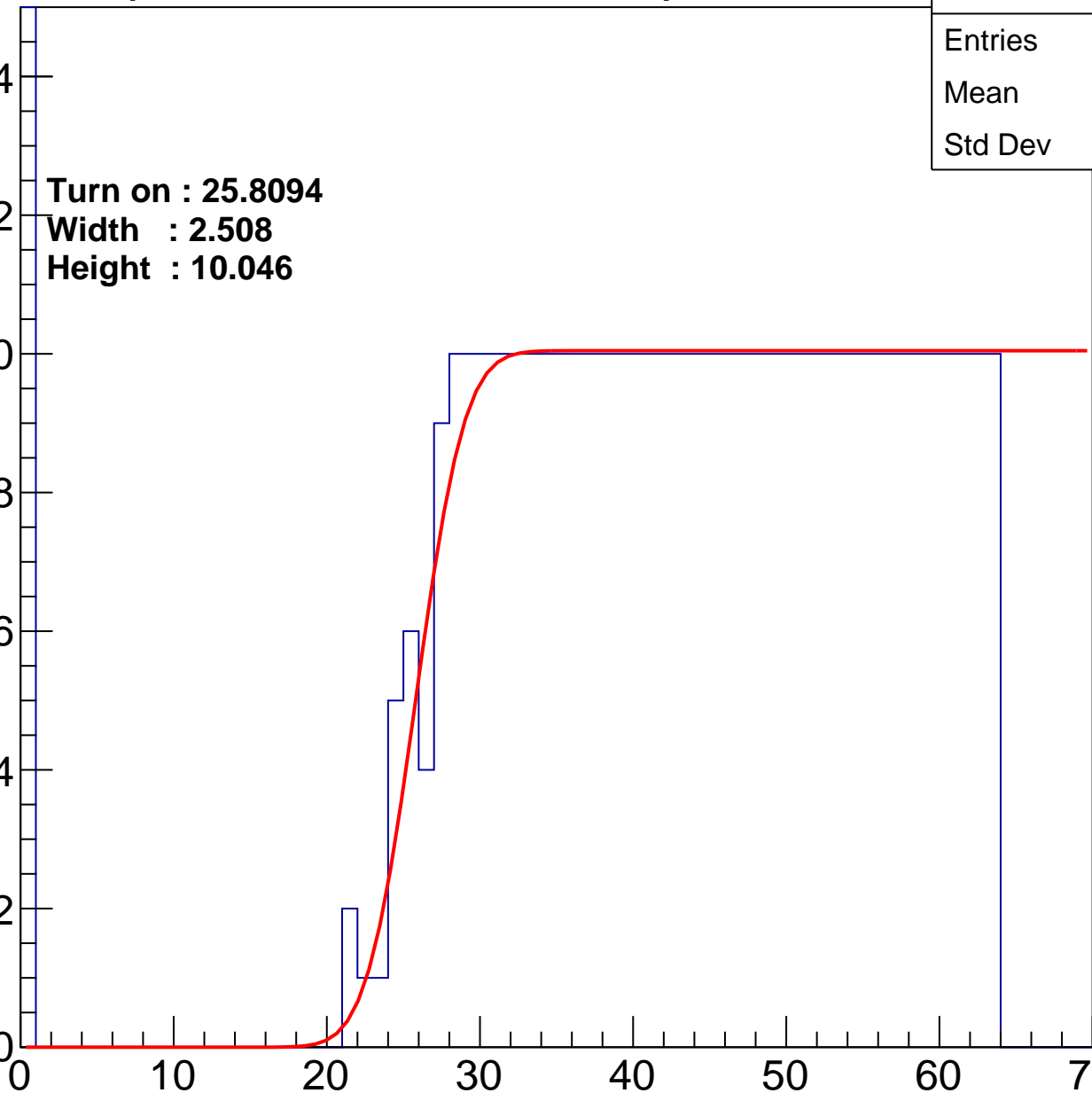
Width : 2.508

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch66

calib_packv5_041523_1651.root, FC#0, port C2

Entries	450
Mean	37.76
Std Dev	18.71

Turn on : 26.1260

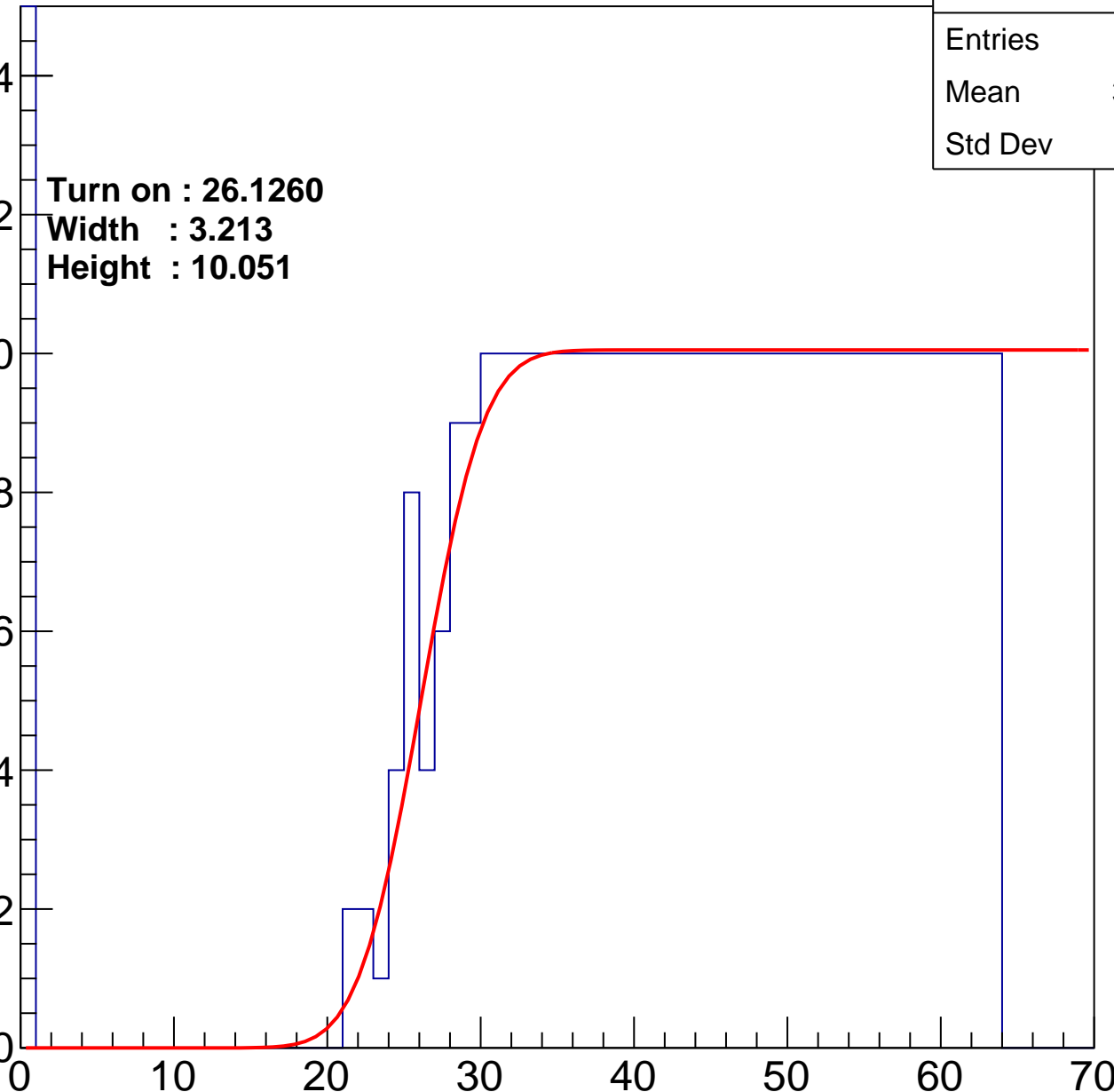
Width : 3.213

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch67

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	39.53
Std Dev	16.75

Turn on : 24.4659

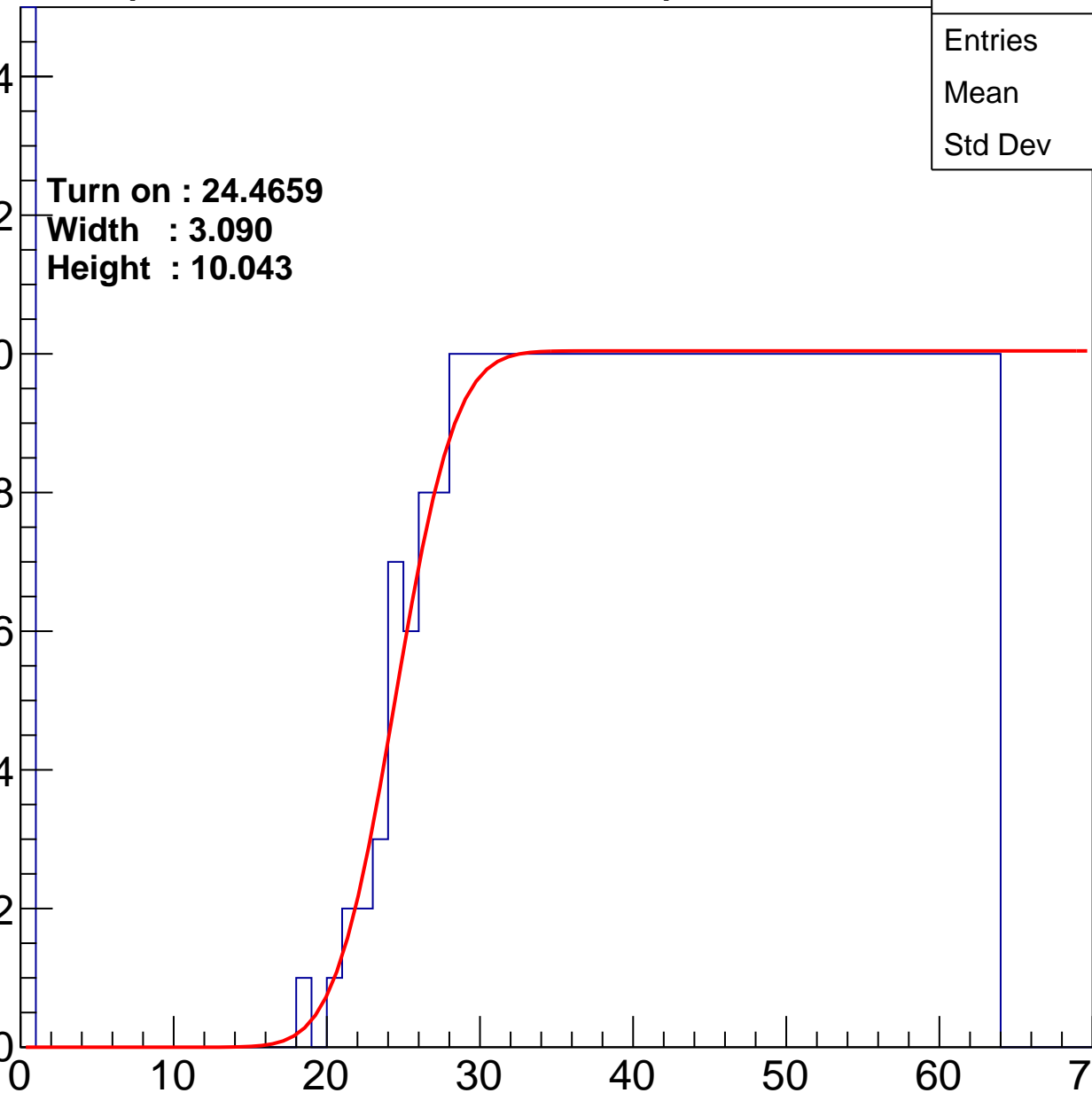
Width : 3.090

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch68

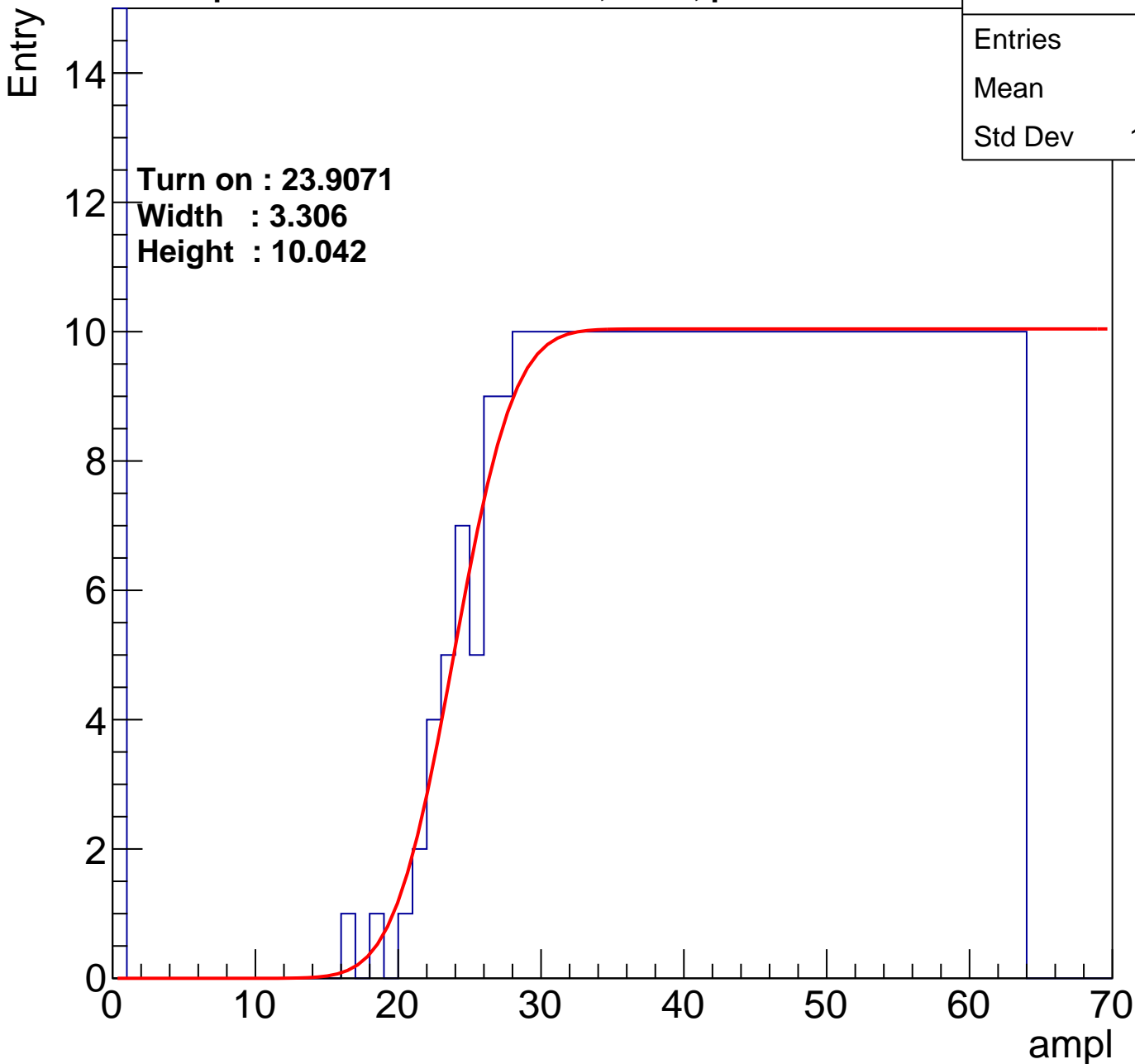
calib_packv5_041523_1651.root, FC#0, port C2

Entries	458
Mean	38.1
Std Dev	17.83

Turn on : 23.9071

Width : 3.306

Height : 10.042



B1L103S, U24-ch69

calib_packv5_041523_1651.root, FC#0, port C2

Entries	400
Mean	40.1
Std Dev	18.06

Turn on : 29.0313

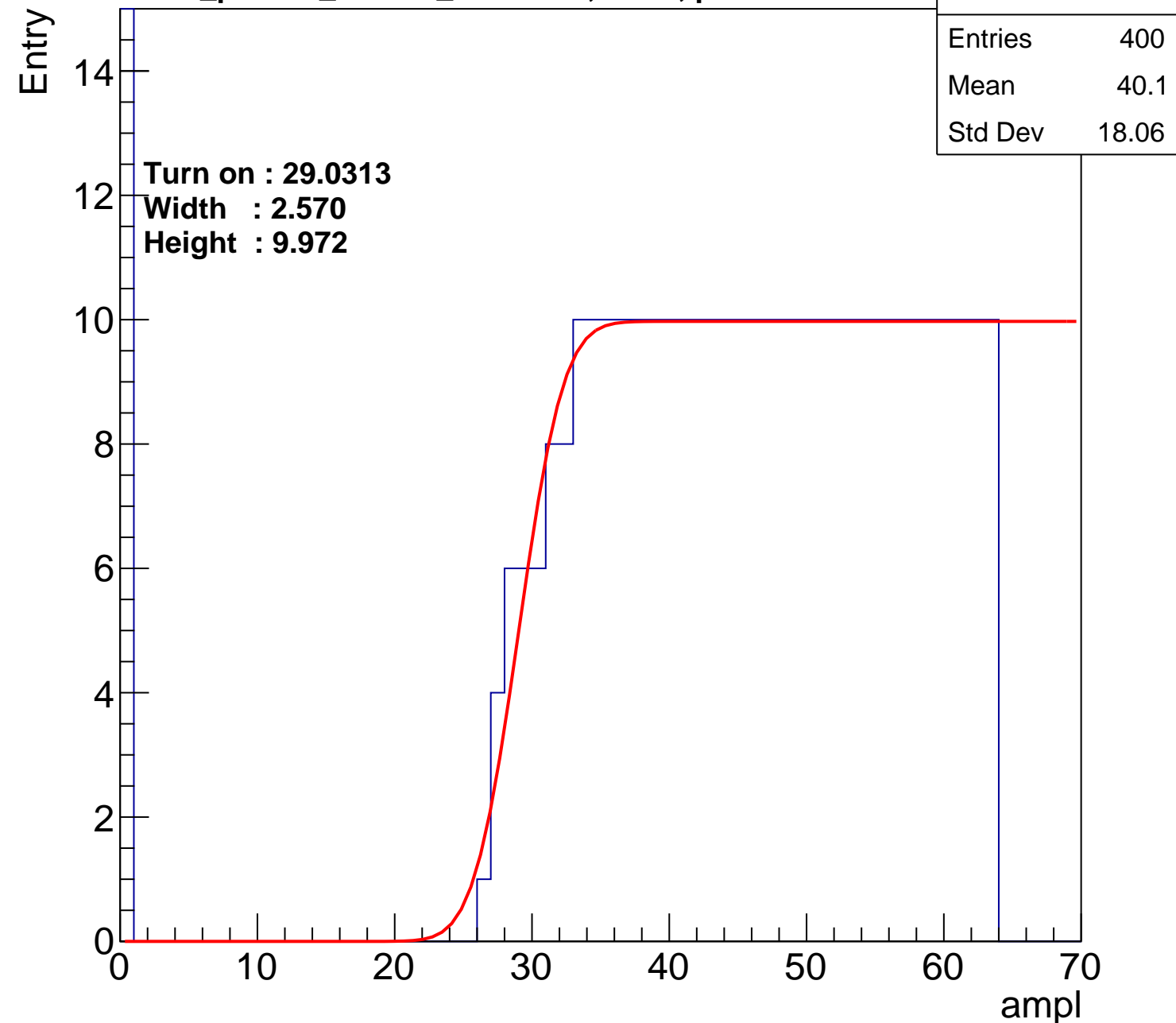
Width : 2.570

Height : 9.972

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch70

calib_packv5_041523_1651.root, FC#0, port C2

Entries	465
Mean	37.58
Std Dev	18.19

Turn on : 24.0951

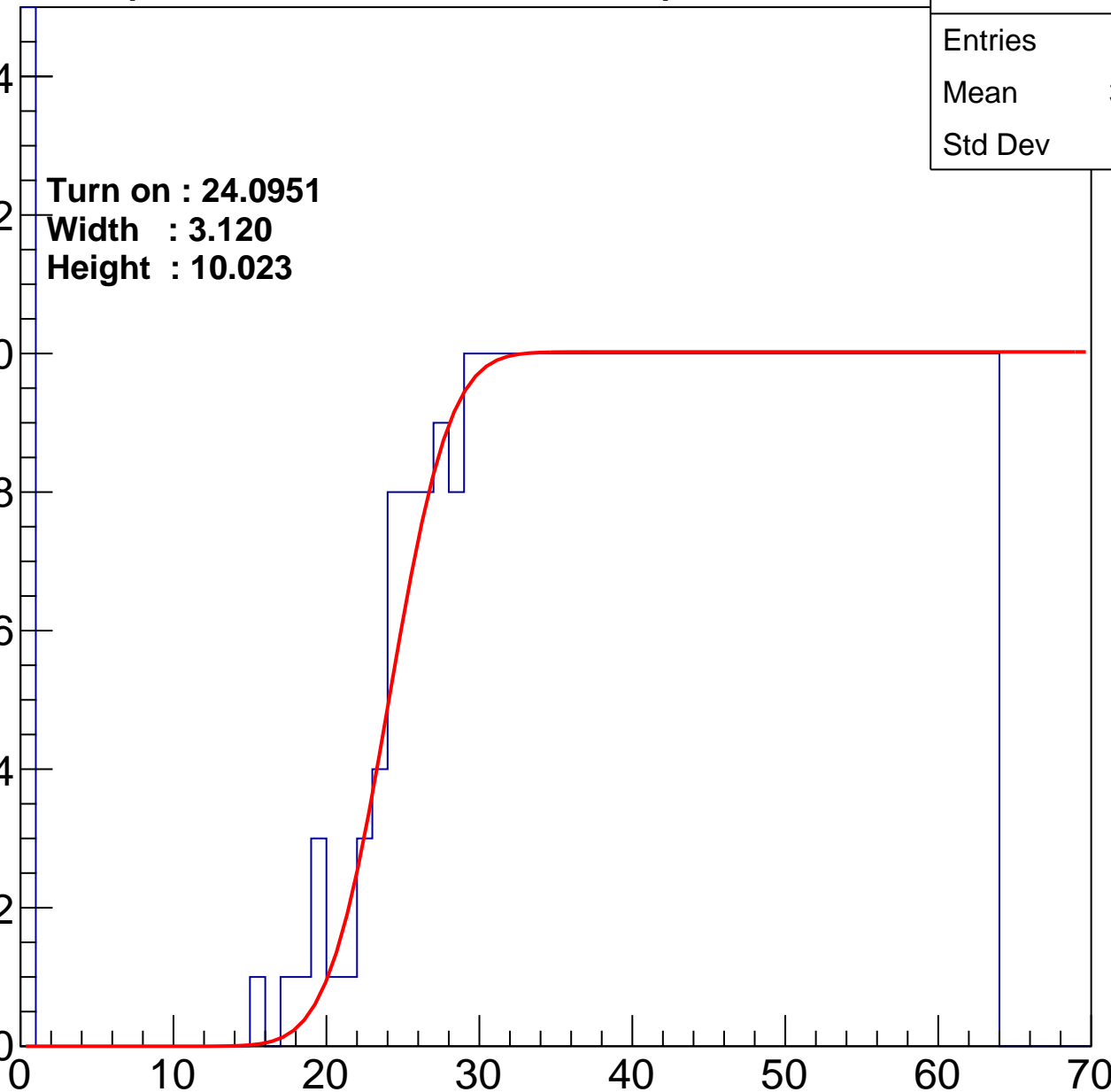
Width : 3.120

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch71

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	38.86
Std Dev	17.58

Turn on : 24.9813

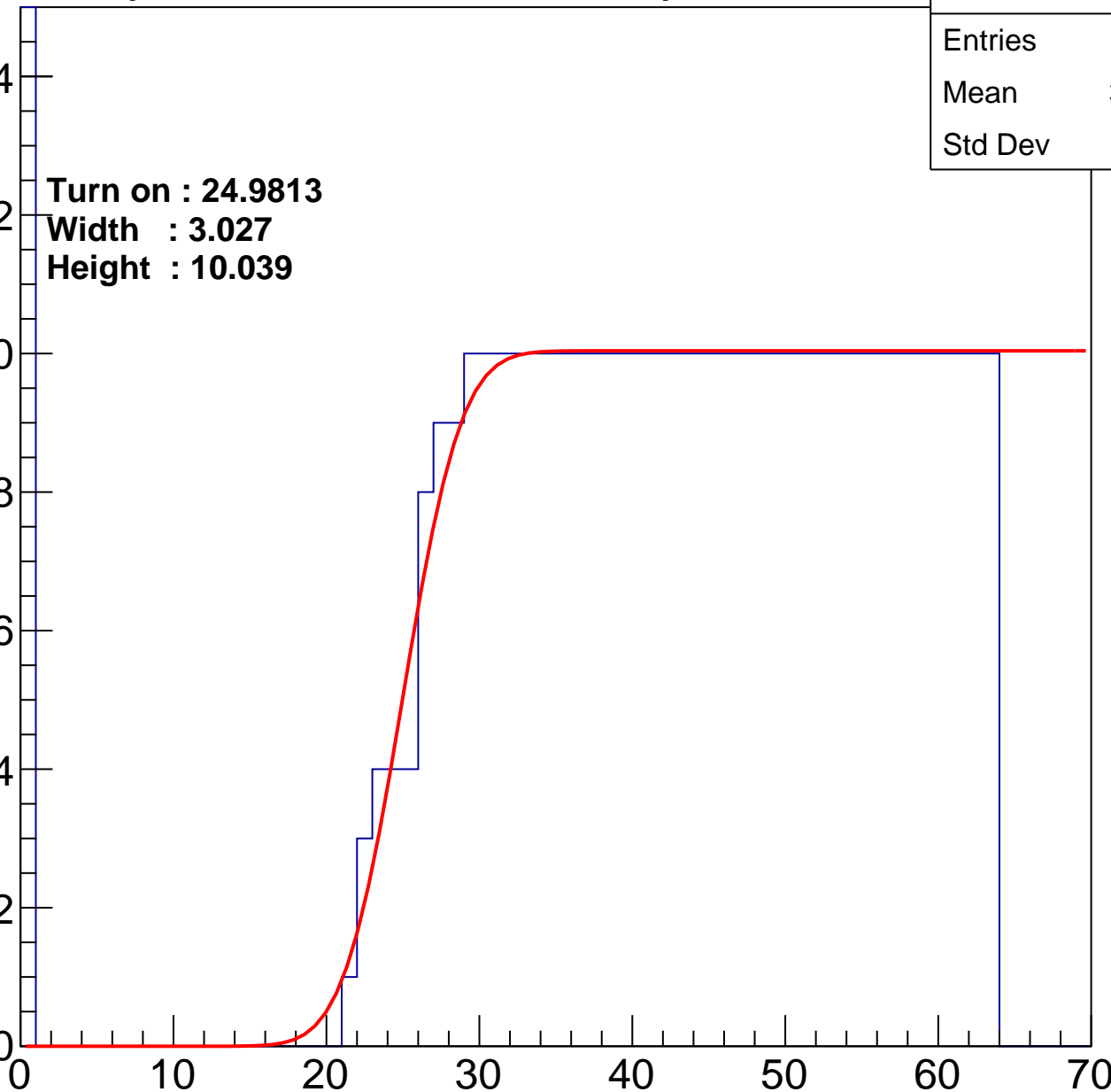
Width : 3.027

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch72

calib_packv5_041523_1651.root, FC#0, port C2

Entries	438
Mean	39.35
Std Dev	17.13

Turn on : 24.8808

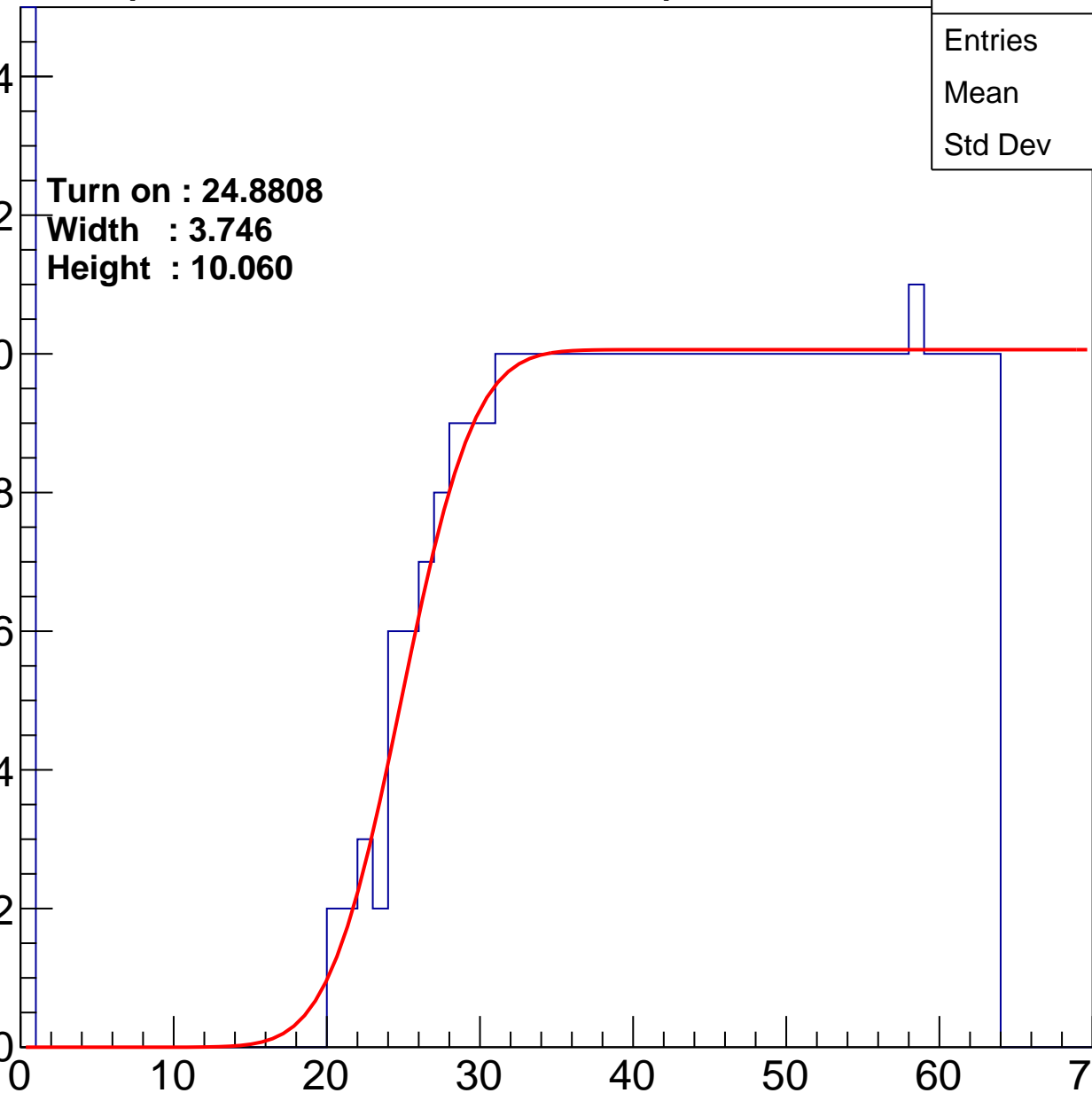
Width : 3.746

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch73

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	39.27
Std Dev	17.21

Turn on : 25.3795

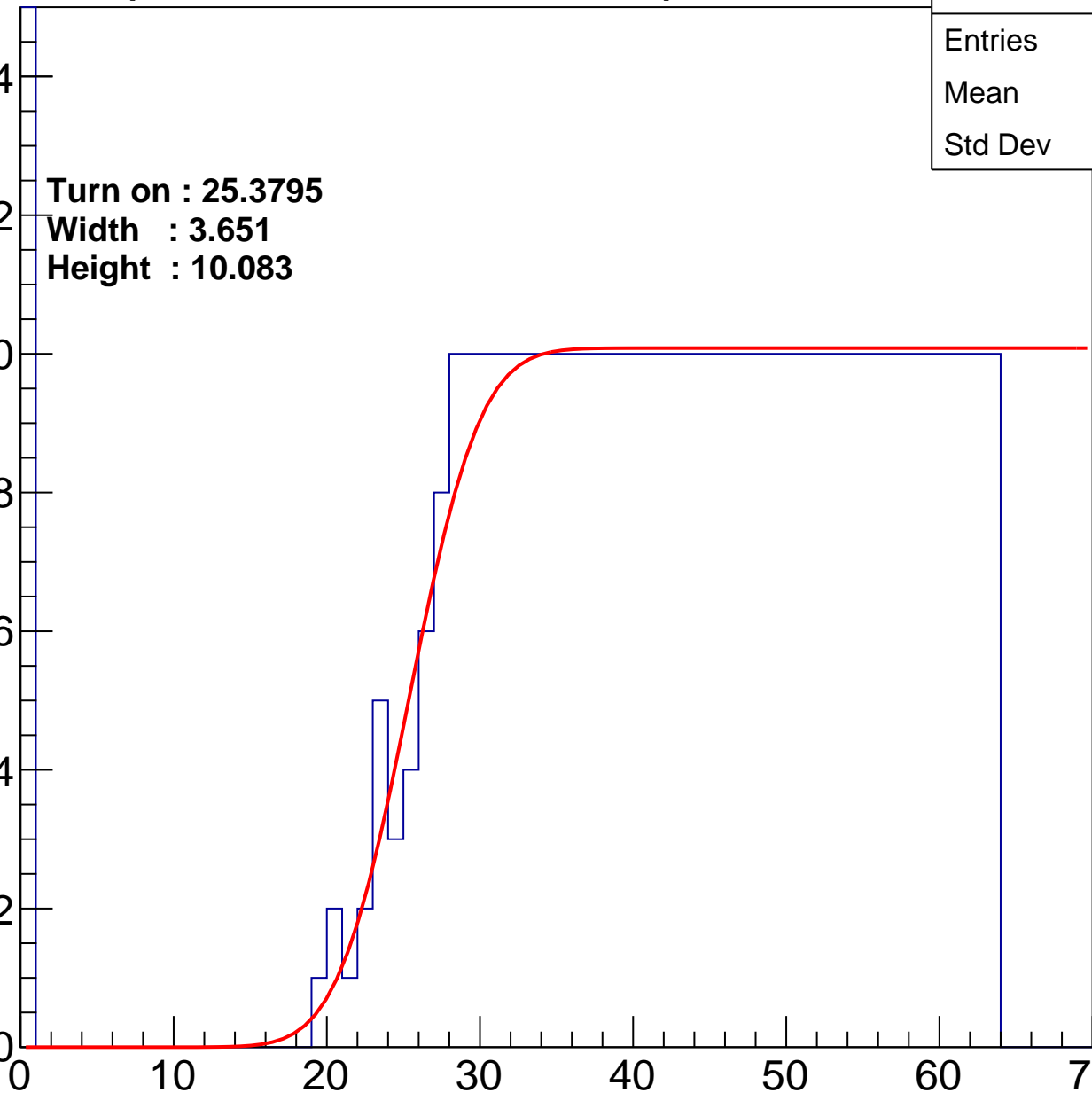
Width : 3.651

Height : 10.083

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch74

calib_packv5_041523_1651.root, FC#0, port C2

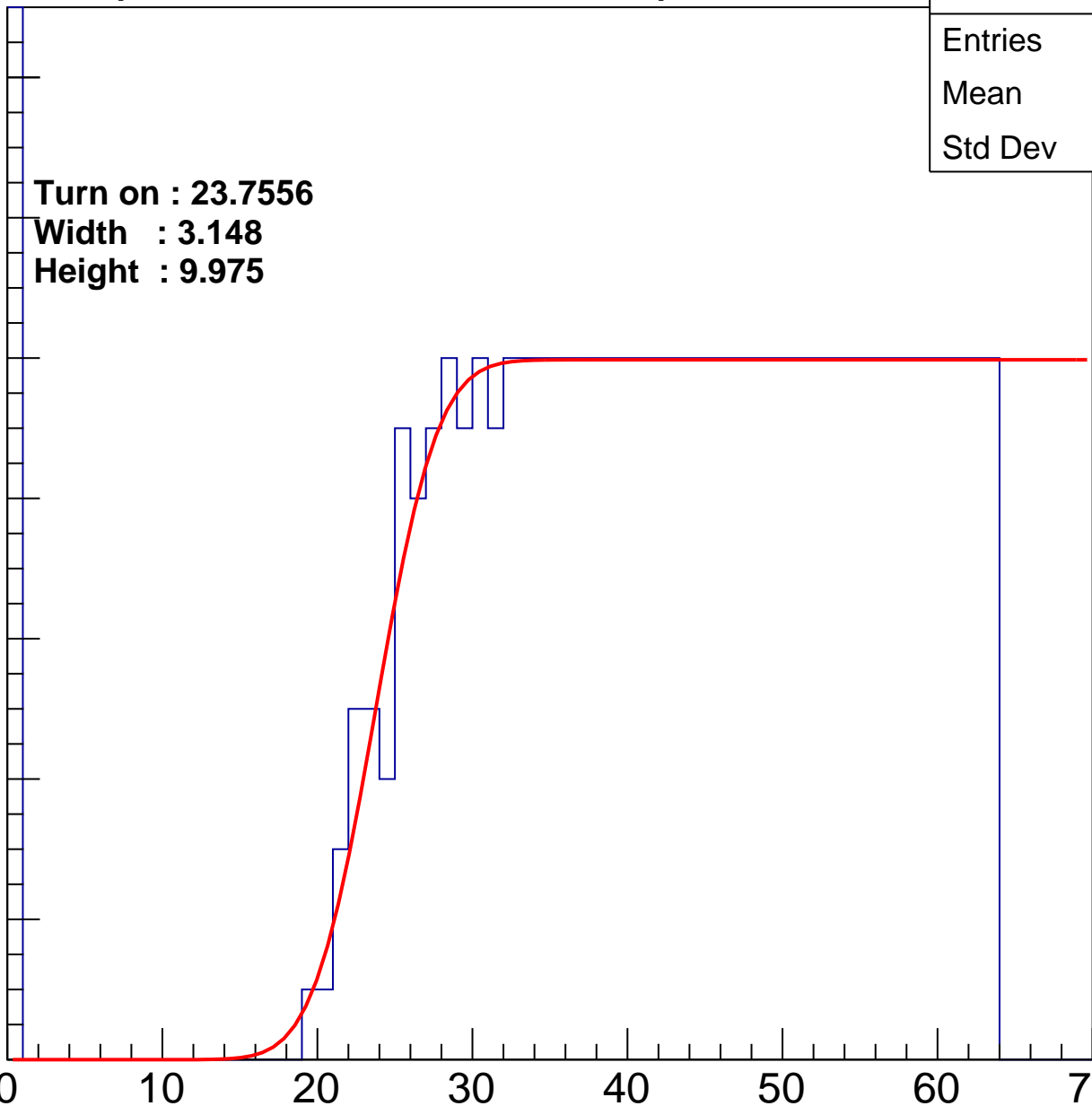
Entry

14
12
10
8
6
4
2
0

Turn on : 23.7556
Width : 3.148
Height : 9.975

Entries	461
Mean	37.79
Std Dev	18.11

ampl



B1L103S, U24-ch75

calib_packv5_041523_1651.root, FC#0, port C2

Entries	414
Mean	39.83
Std Dev	17.65

Turn on : 28.1042

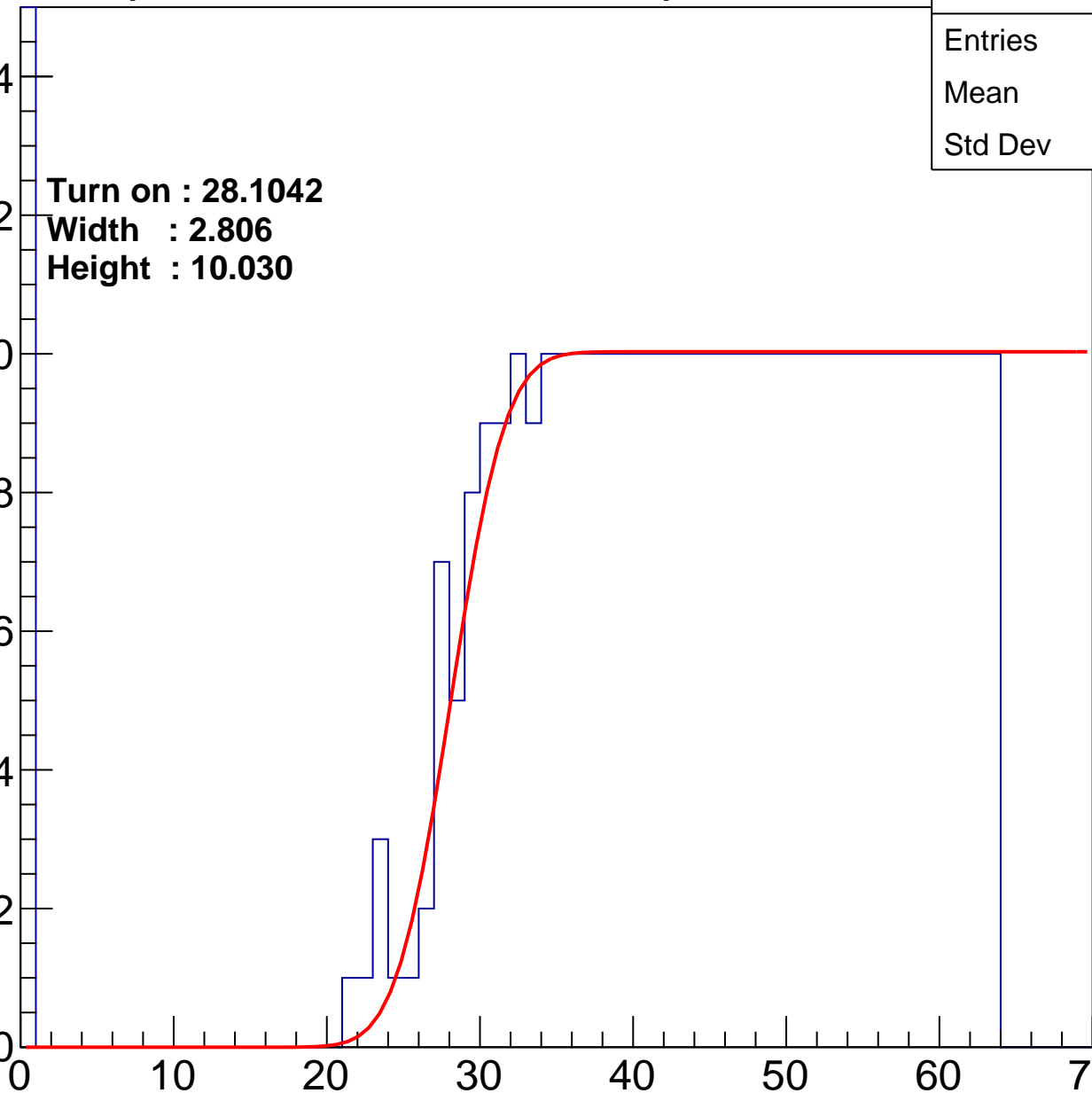
Width : 2.806

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch76

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	39.11
Std Dev	17.28

Turn on : 24.8152

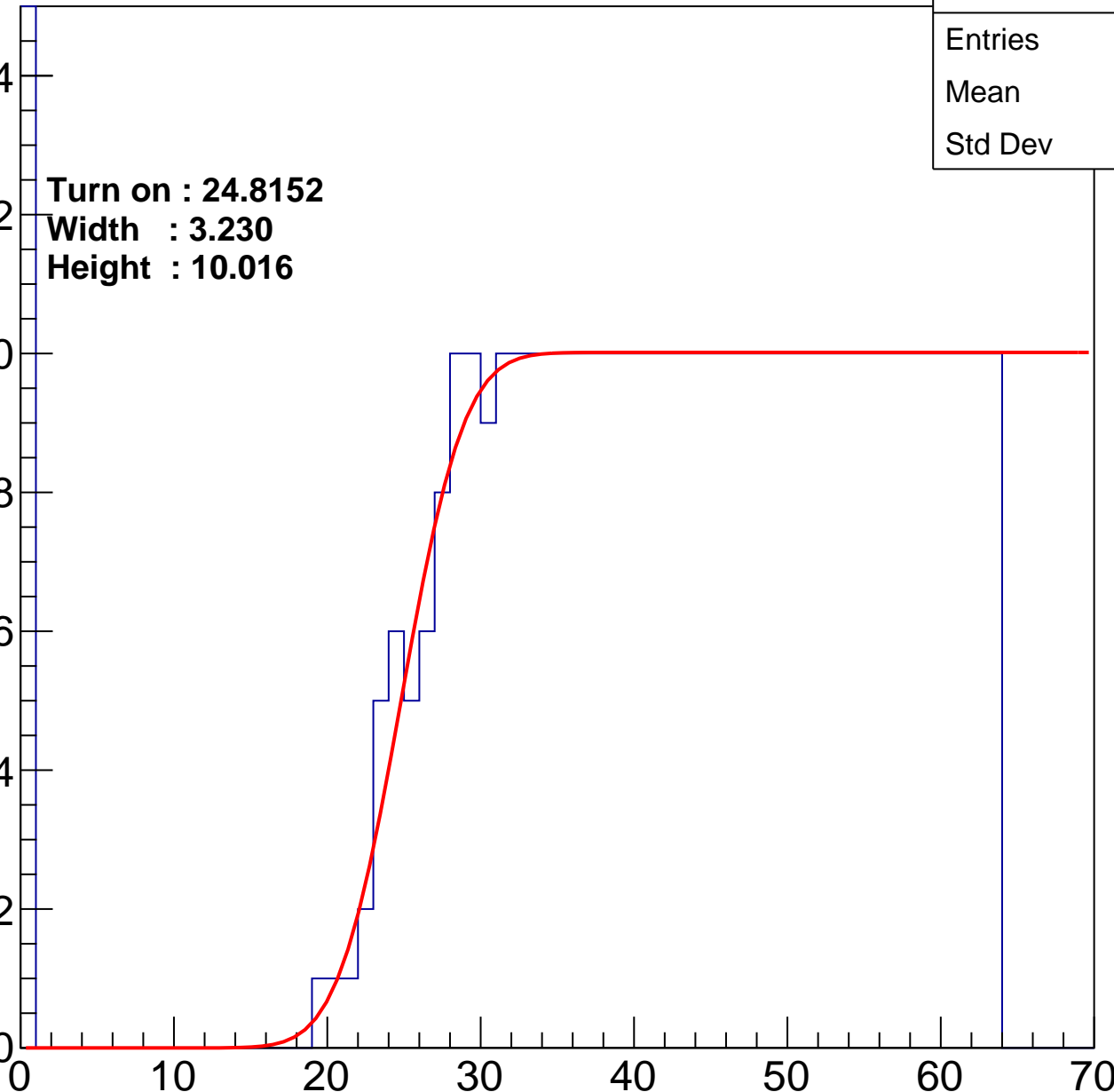
Width : 3.230

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch77

calib_packv5_041523_1651.root, FC#0, port C2

Entries	422
Mean	40.28
Std Dev	16.49

Turn on : 25.8018

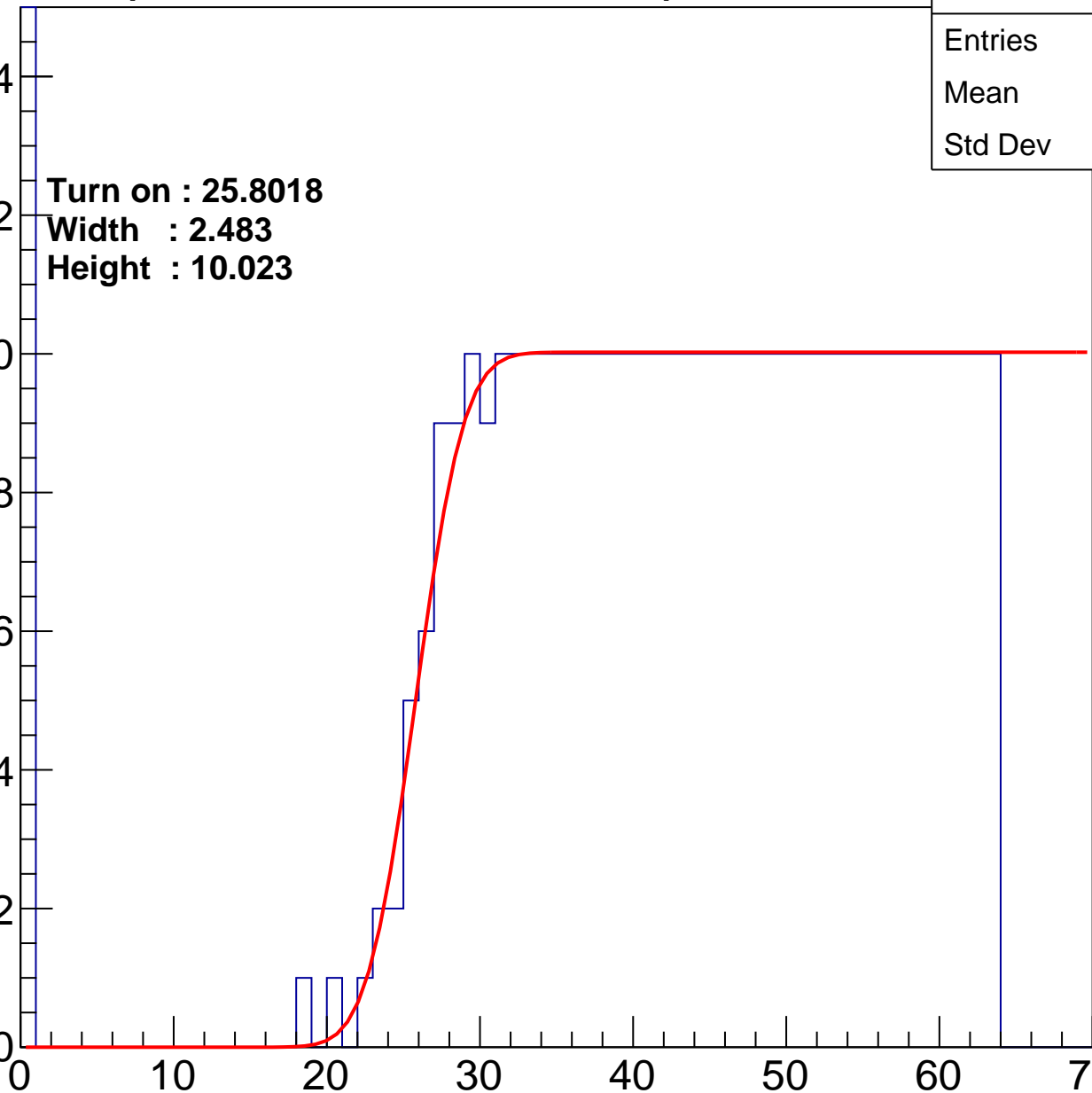
Width : 2.483

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch78

calib_packv5_041523_1651.root, FC#0, port C2

Entries	465
Mean	37.23
Std Dev	18.7

Turn on : 24.2765

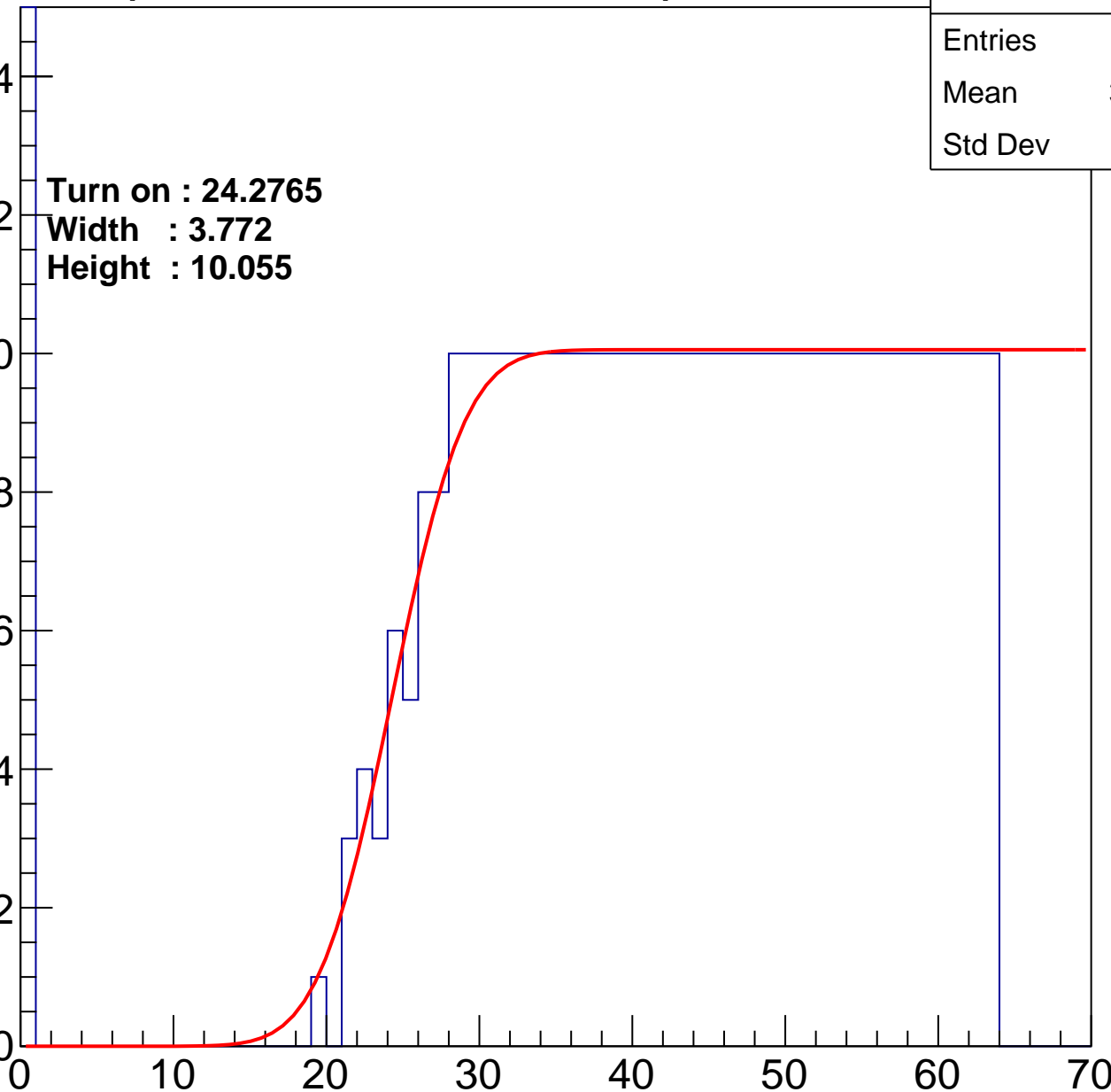
Width : 3.772

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch79

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	39.6
Std Dev	17.03

Turn on : 25.2620

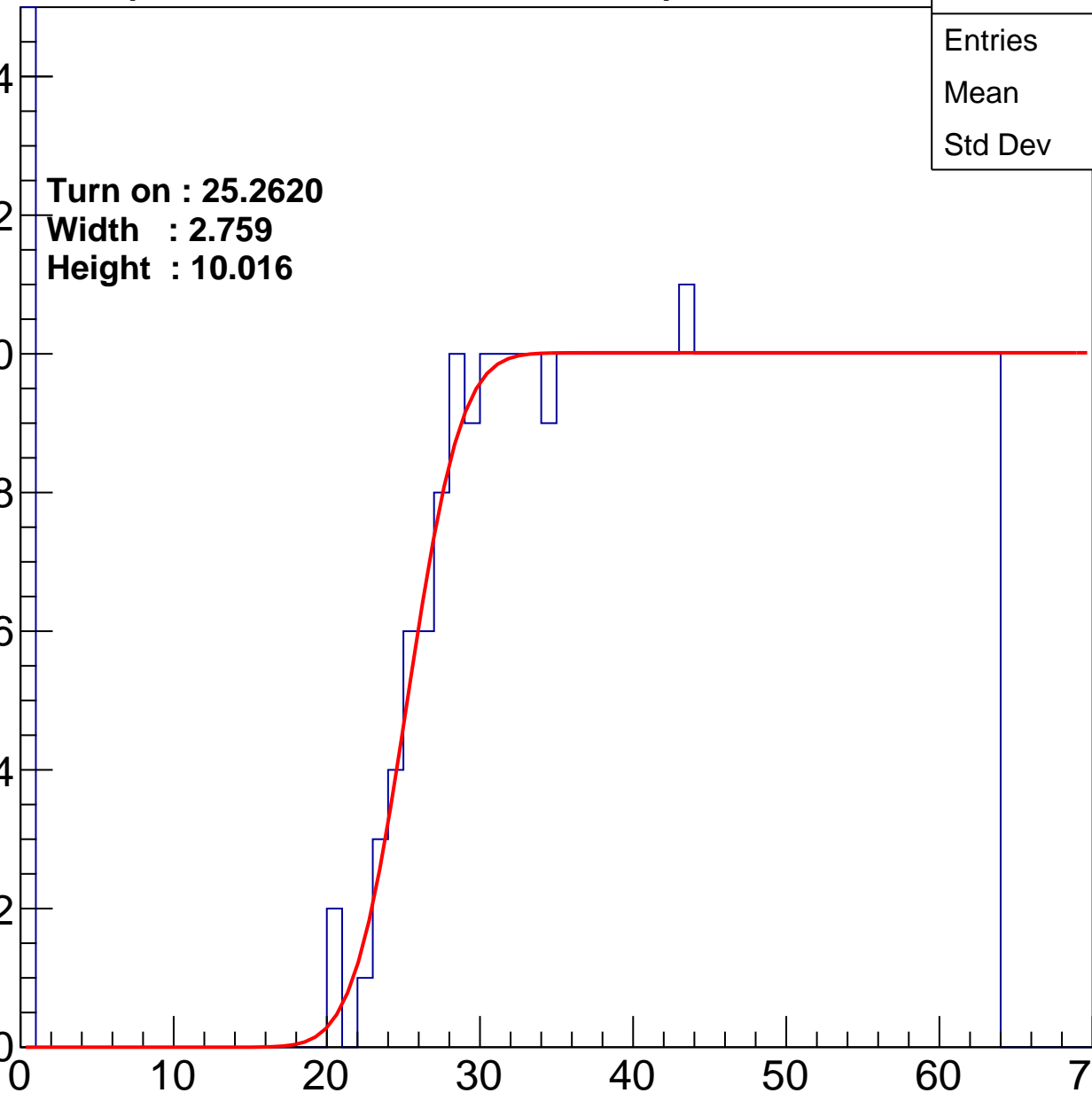
Width : 2.759

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch80

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	38.79
Std Dev	17.85

Turn on : 25.3819

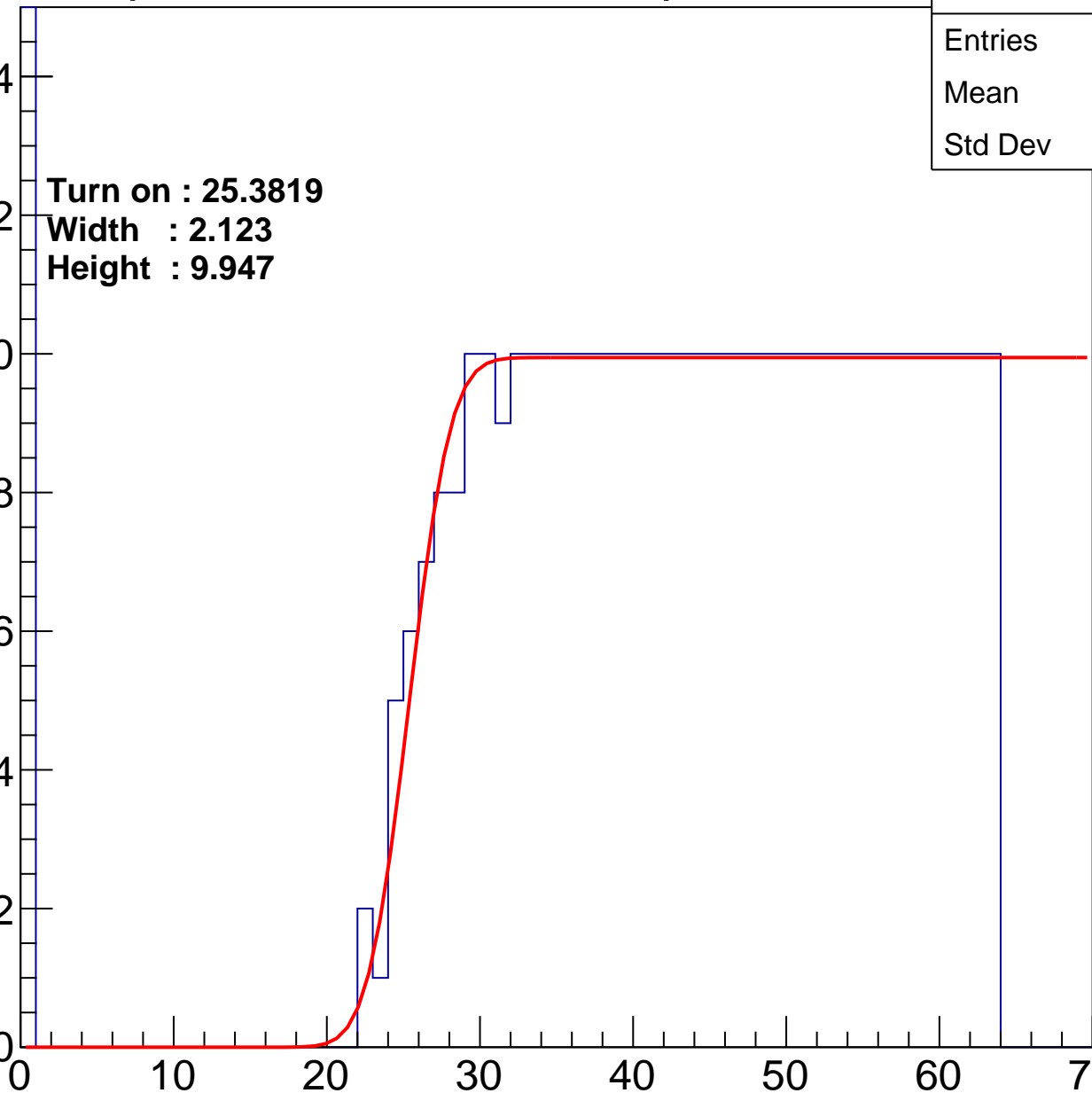
Width : 2.123

Height : 9.947

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch81

calib_packv5_041523_1651.root, FC#0, port C2

Entries	431
Mean	39.17
Std Dev	17.69

Turn on : 25.9102

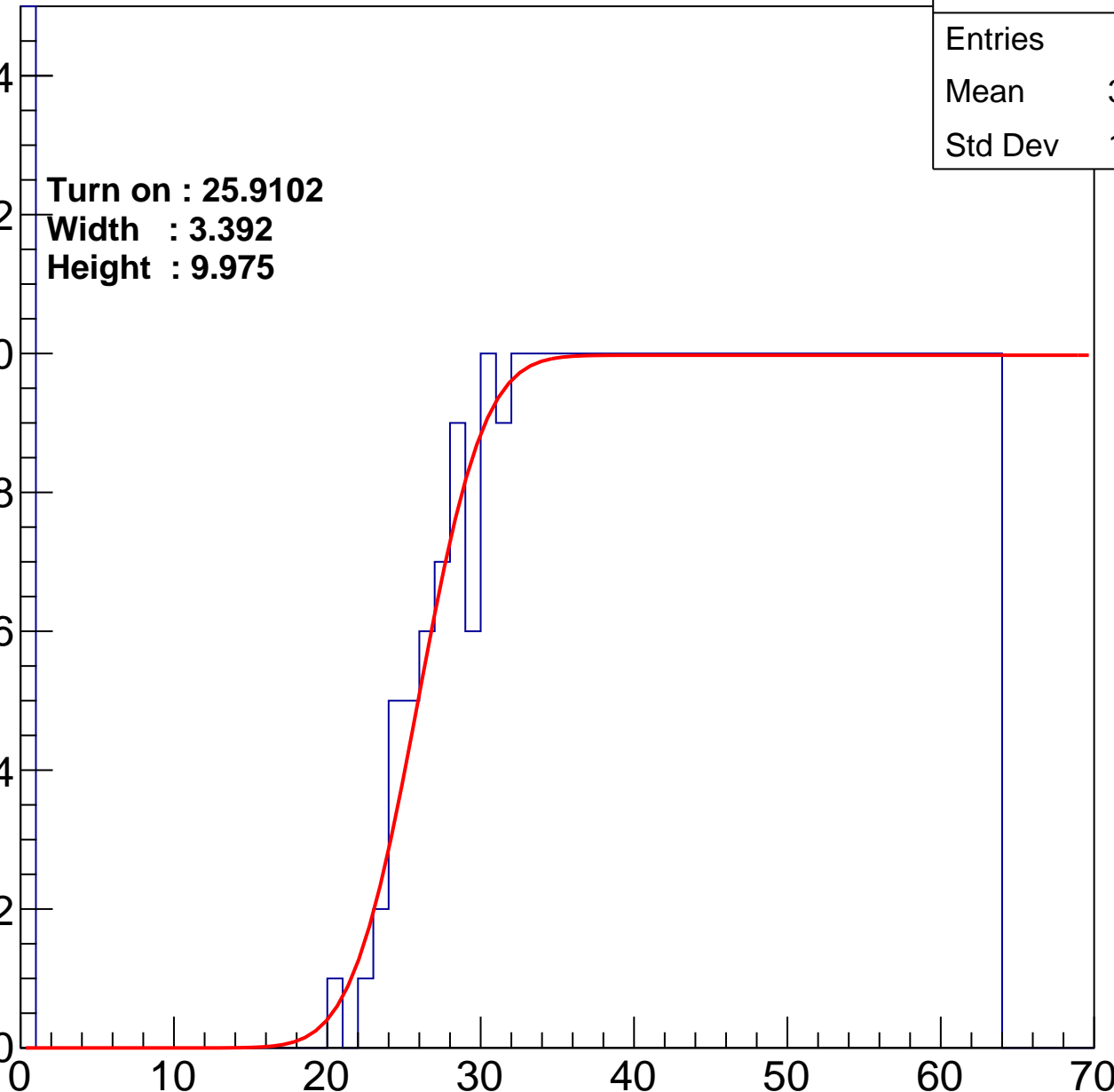
Width : 3.392

Height : 9.975

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch82

calib_packv5_041523_1651.root, FC#0, port C2

Entries	506
Mean	34.12
Std Dev	20.56

Turn on : 26.9195

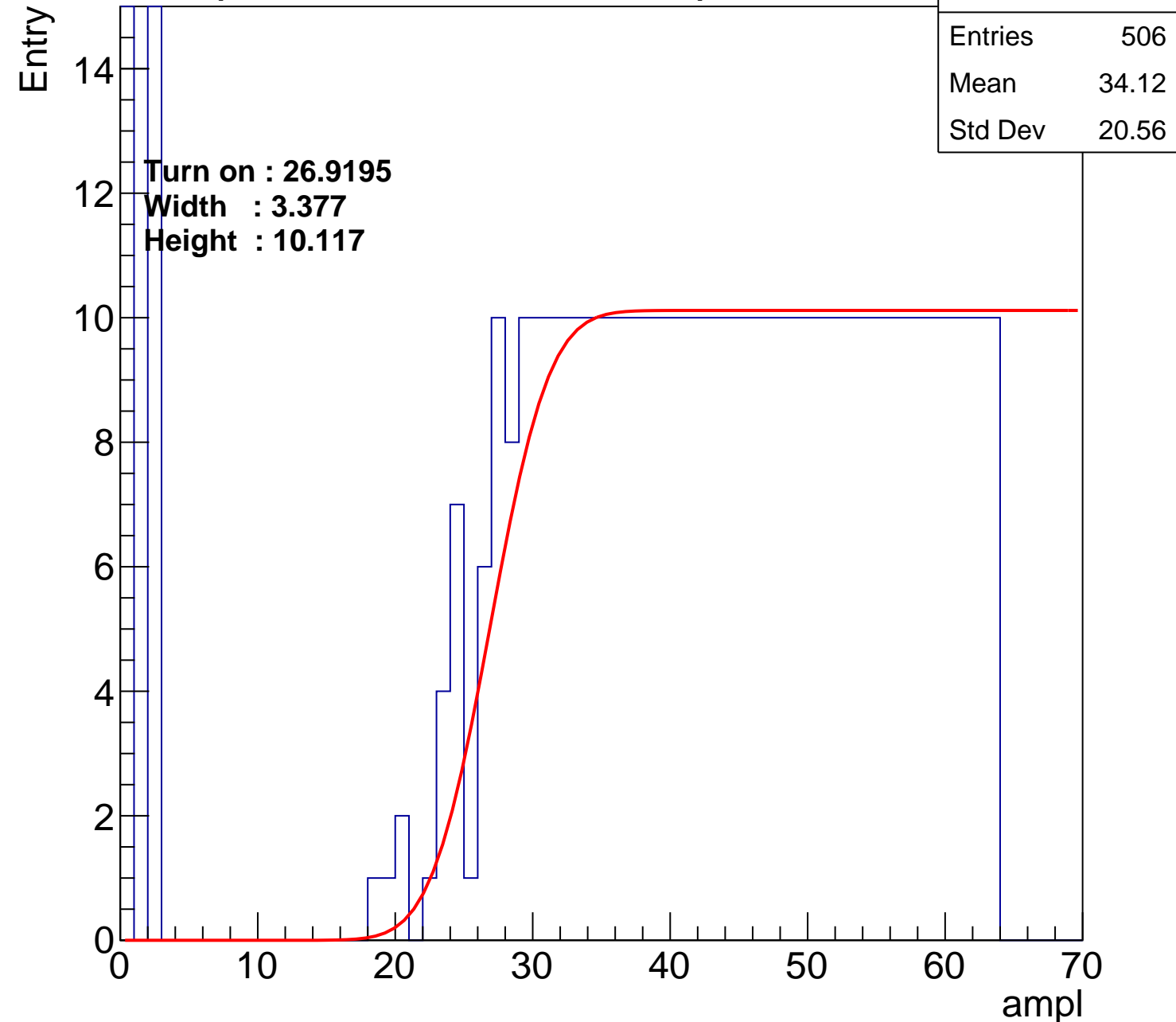
Width : 3.377

Height : 10.117

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch83

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	39.19
Std Dev	17.03

Turn on : 24.3934

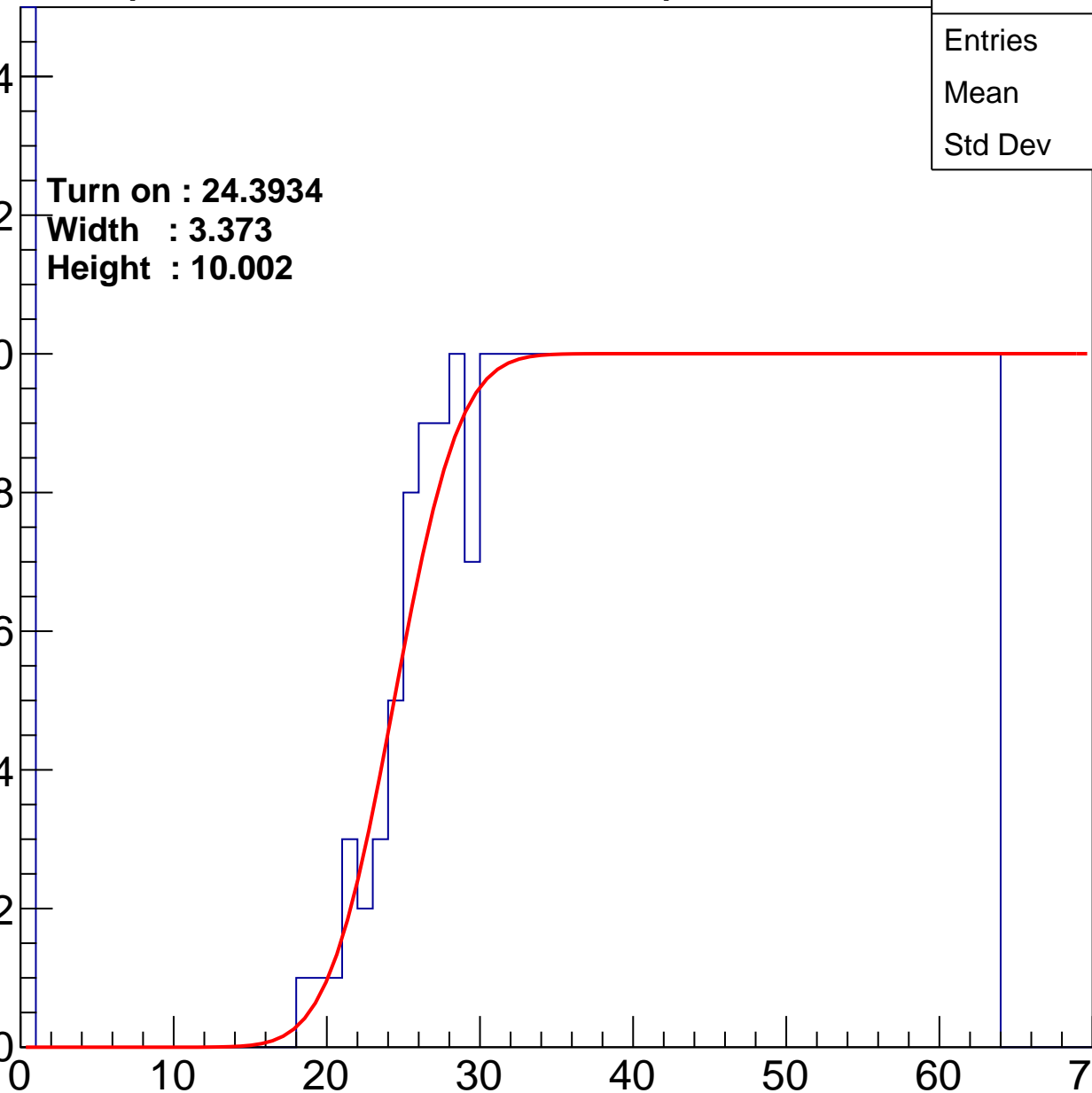
Width : 3.373

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch84

calib_packv5_041523_1651.root, FC#0, port C2

Entries	437
Mean	39.02
Std Dev	17.53

Turn on : 24.7892

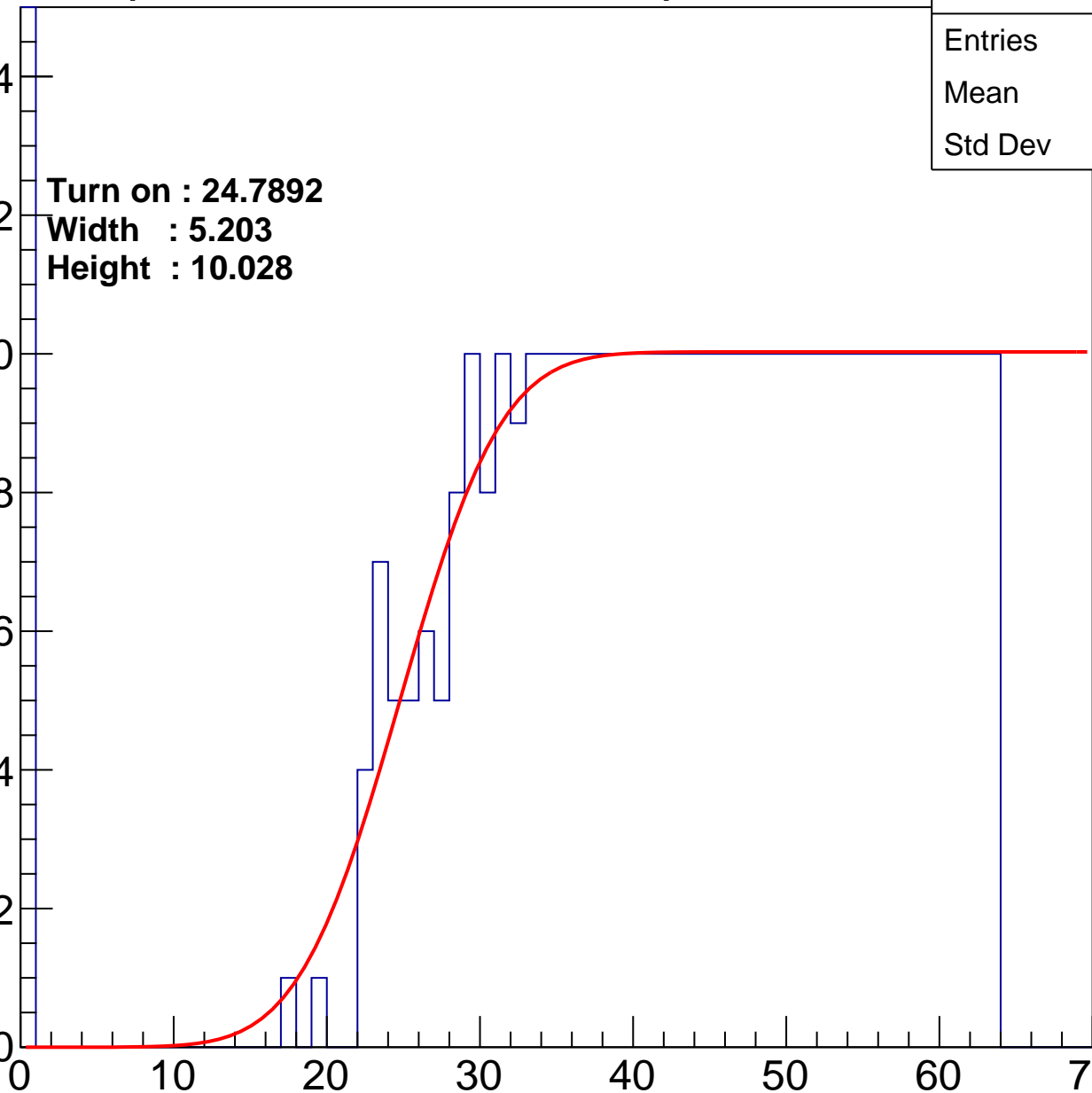
Width : 5.203

Height : 10.028

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch85

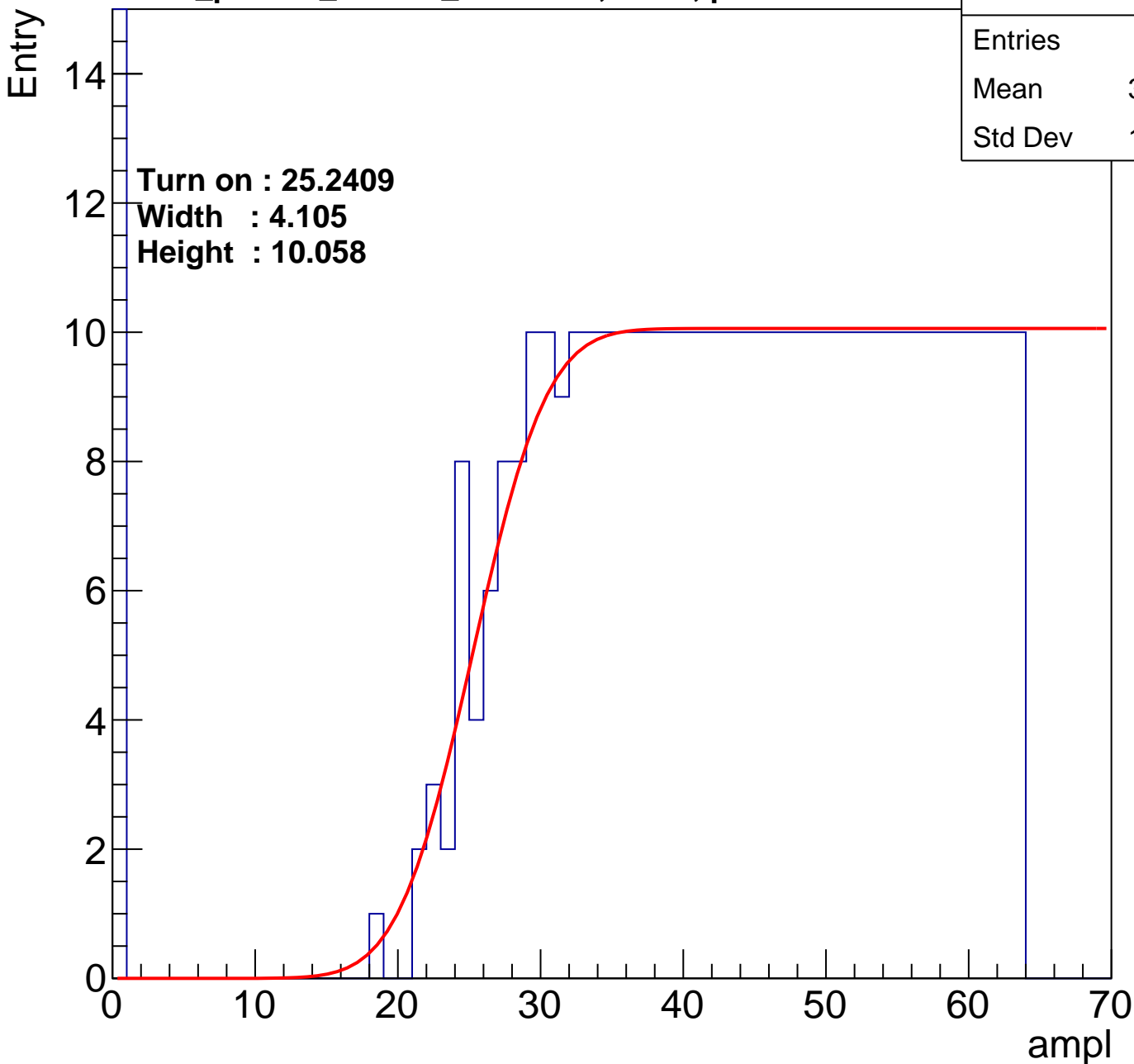
calib_packv5_041523_1651.root, FC#0, port C2

Entries	450
Mean	38.06
Std Dev	18.28

Turn on : 25.2409

Width : 4.105

Height : 10.058



B1L103S, U24-ch86

calib_packv5_041523_1651.root, FC#0, port C2

Entries	461
Mean	38.17
Std Dev	17.54

Turn on : 23.1738

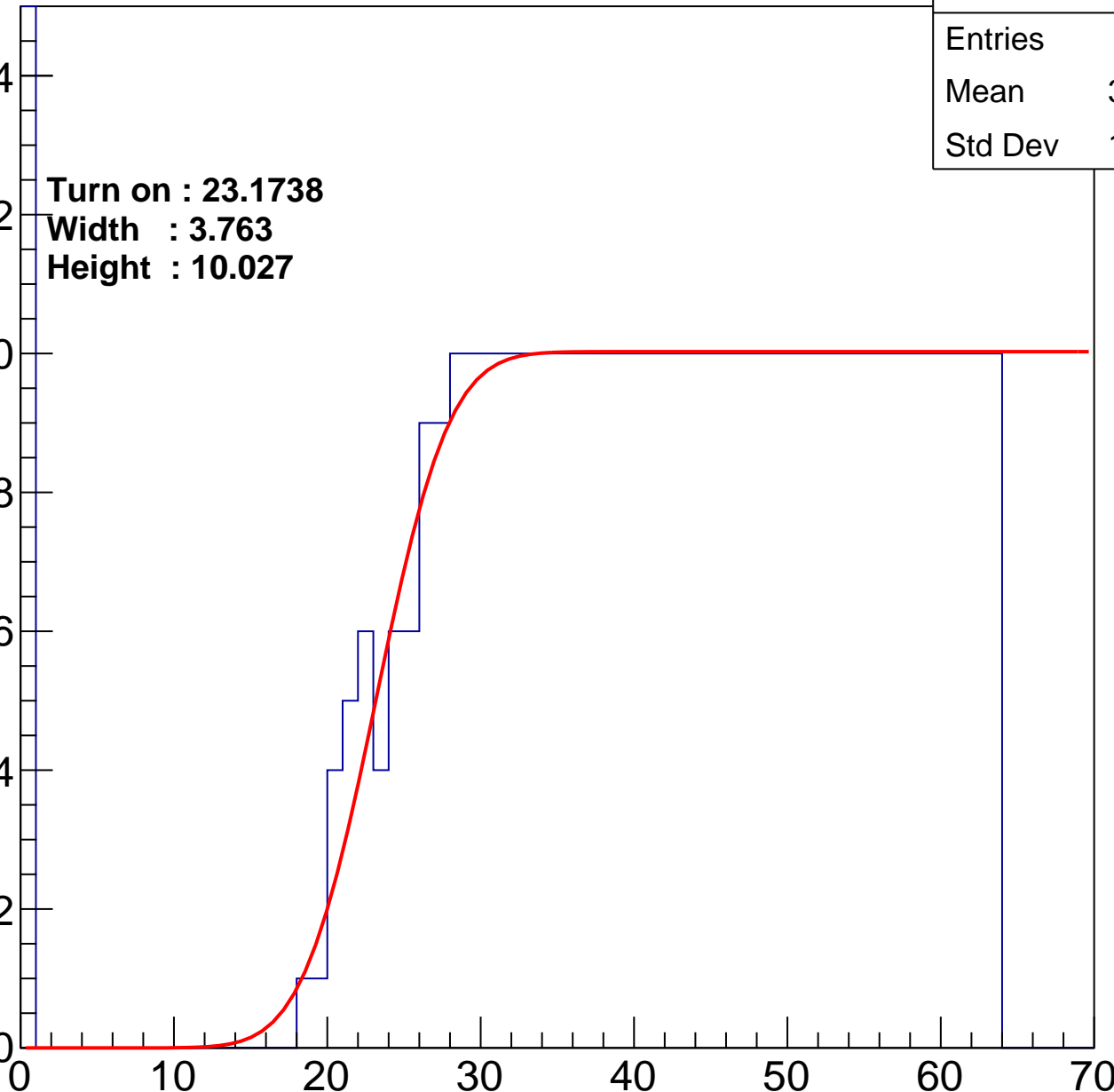
Width : 3.763

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch87

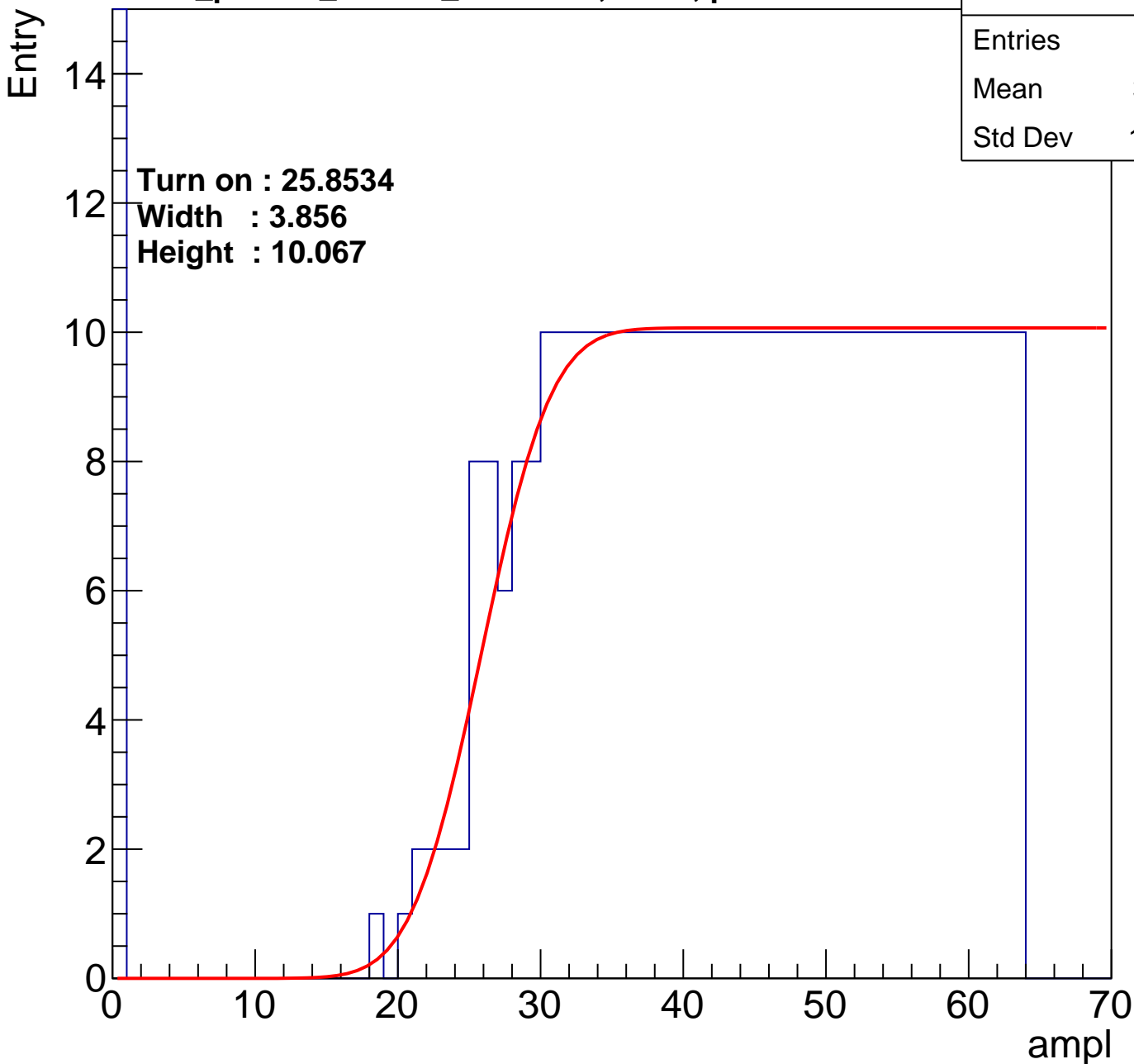
calib_packv5_041523_1651.root, FC#0, port C2

Entries	462
Mean	36.91
Std Dev	19.24

Turn on : 25.8534

Width : 3.856

Height : 10.067



B1L103S, U24-ch88

calib_packv5_041523_1651.root, FC#0, port C2

Entries	435
Mean	39.06
Std Dev	17.63

Turn on : 26.2049

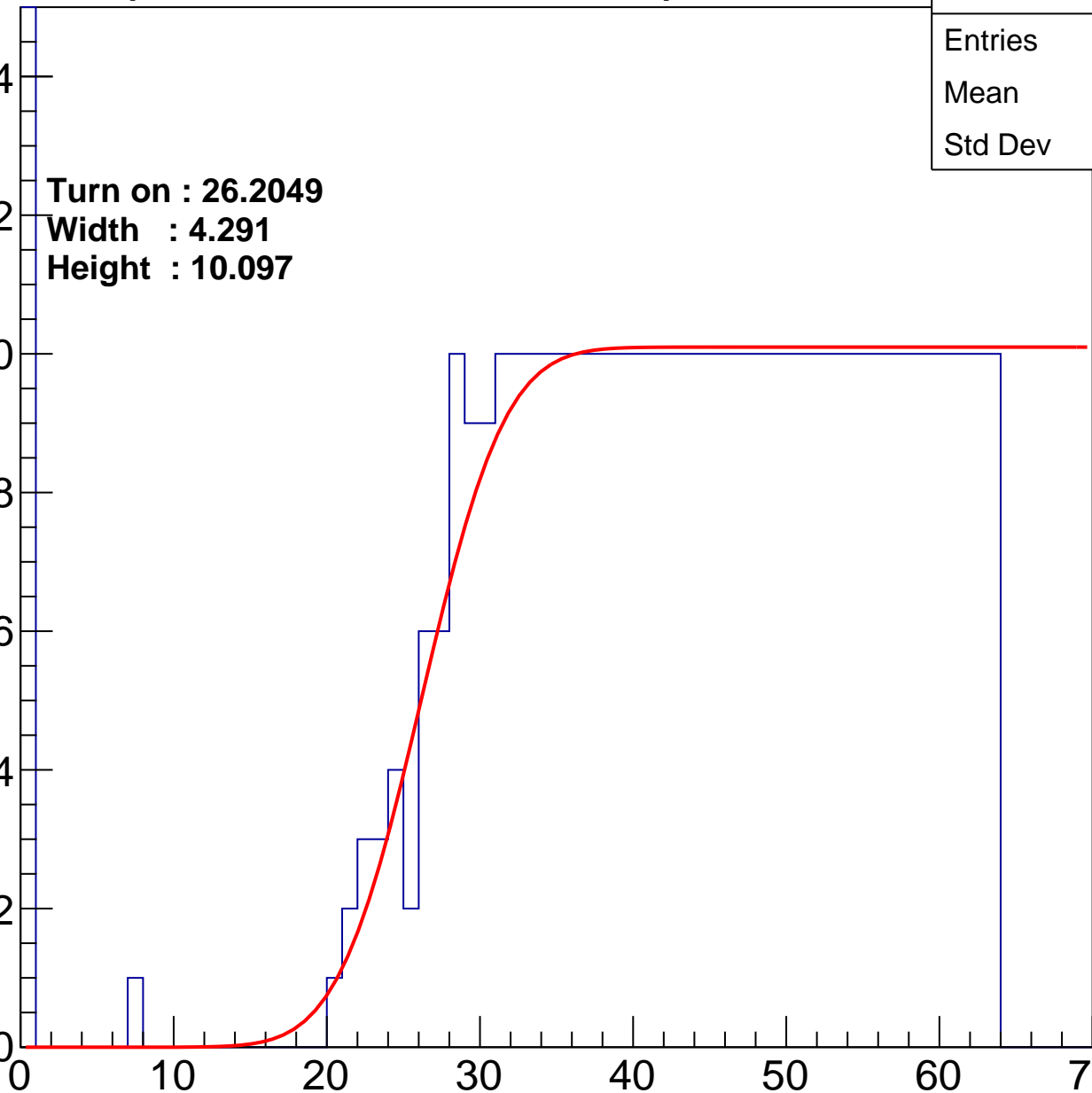
Width : 4.291

Height : 10.097

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch89

calib_packv5_041523_1651.root, FC#0, port C2

Entries	433
Mean	39.14
Std Dev	17.6

Turn on : 25.8696

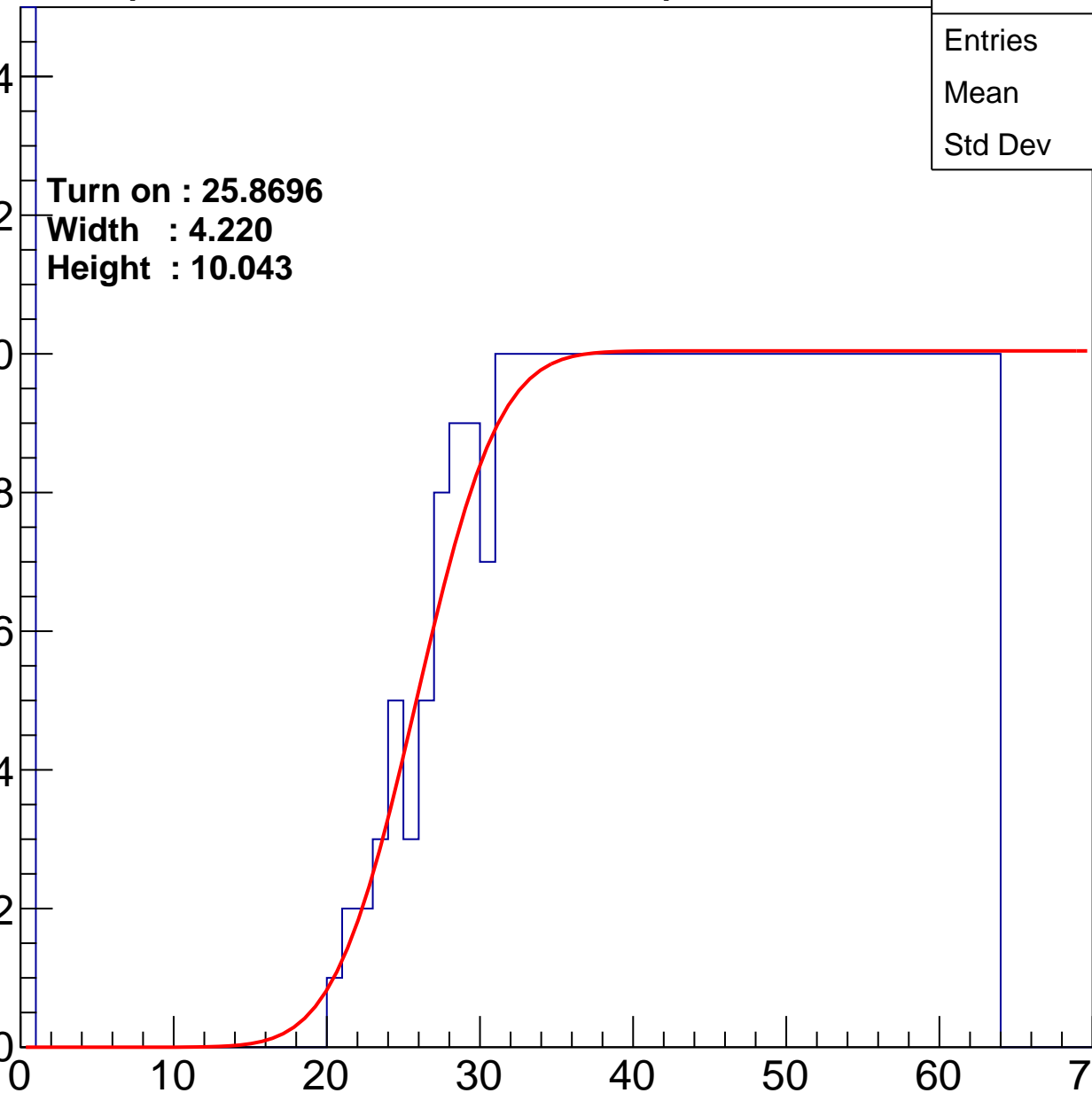
Width : 4.220

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch90

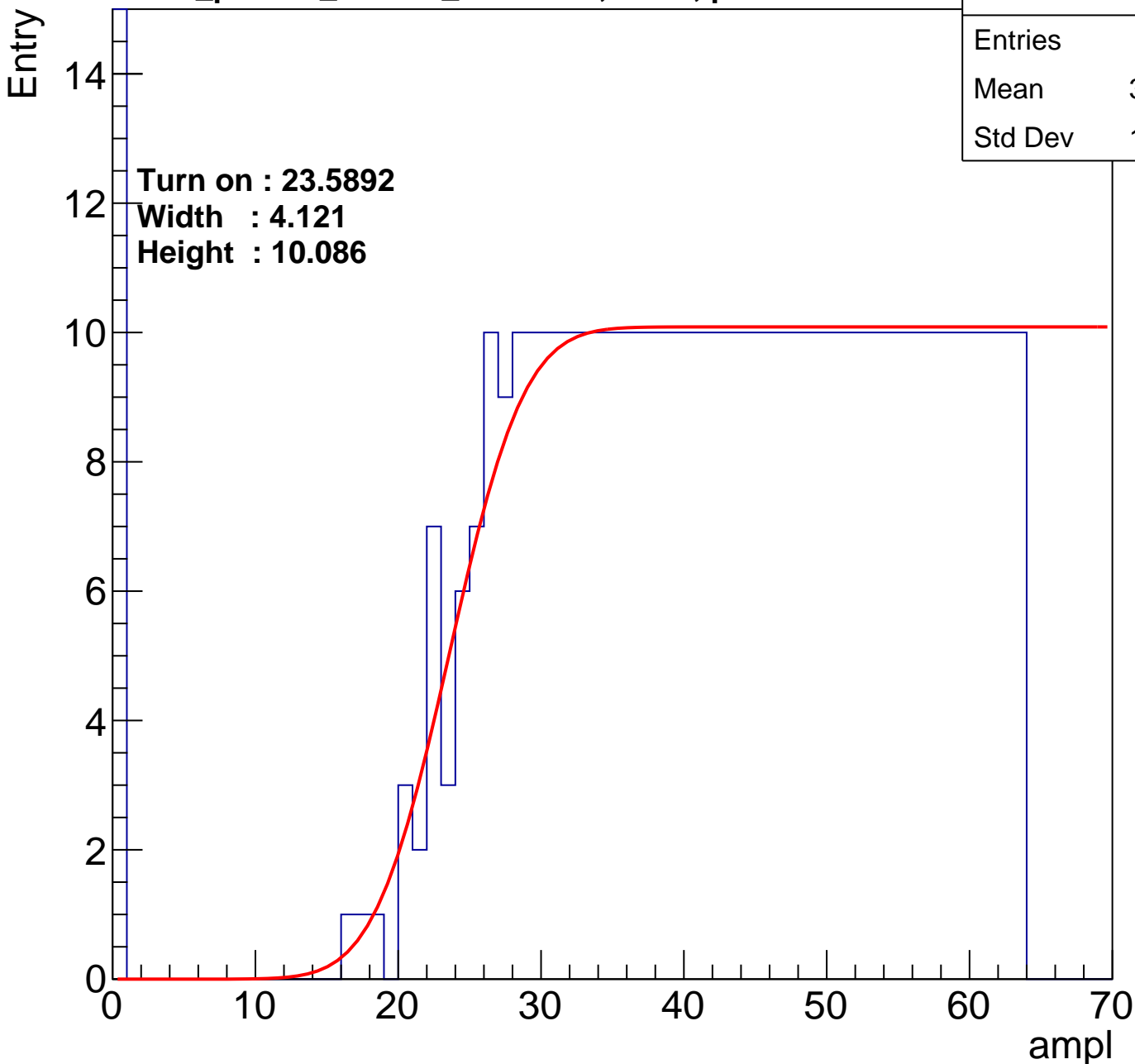
calib_packv5_041523_1651.root, FC#0, port C2

Entries	464
Mean	37.88
Std Dev	17.82

Turn on : 23.5892

Width : 4.121

Height : 10.086



B1L103S, U24-ch91

calib_packv5_041523_1651.root, FC#0, port C2

Entries	440
Mean	38.46
Std Dev	18.26

Turn on : 26.2313

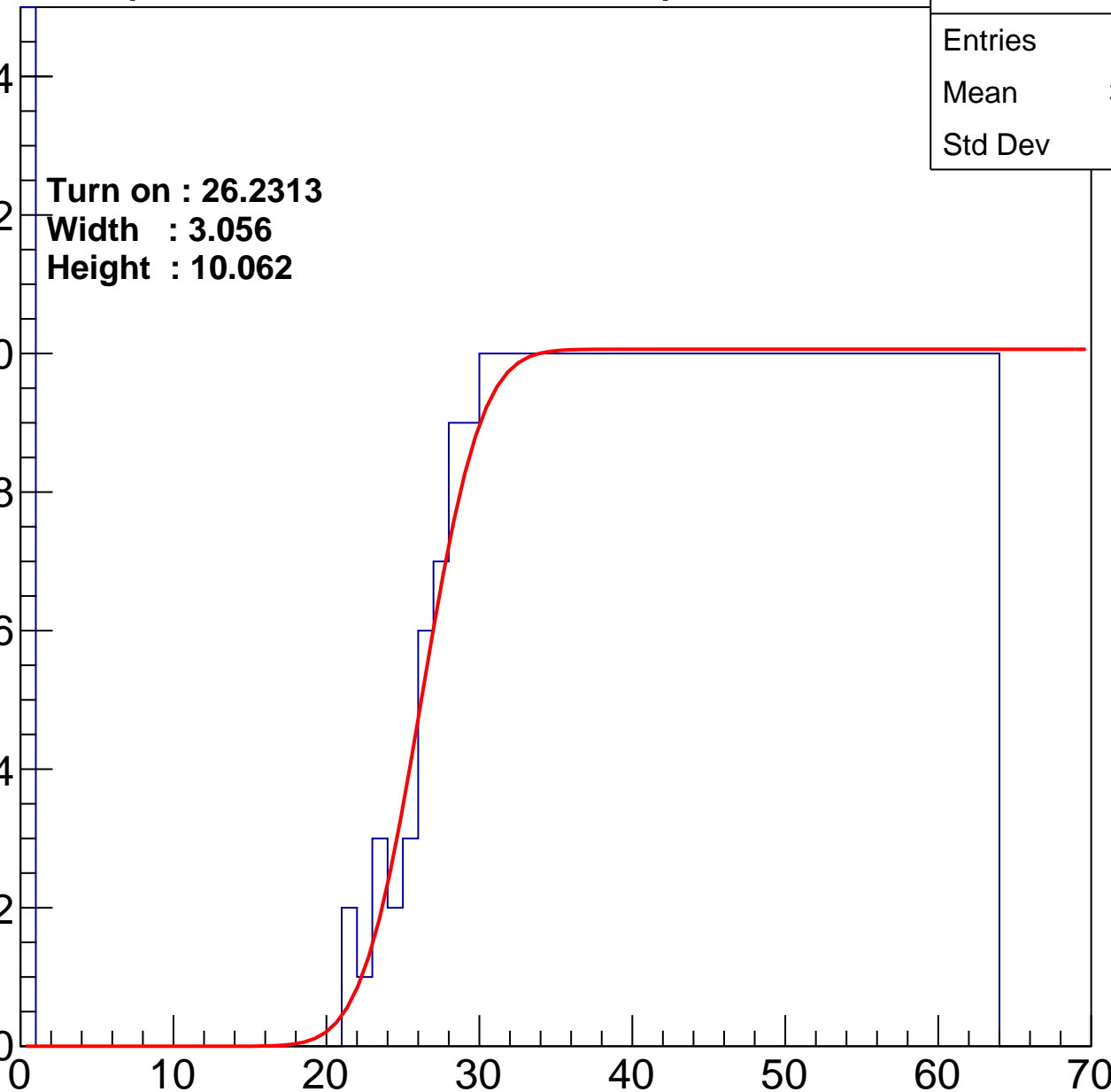
Width : 3.056

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch92

calib_packv5_041523_1651.root, FC#0, port C2

Entries	432
Mean	38.49
Std Dev	18.61

Turn on : 27.0024

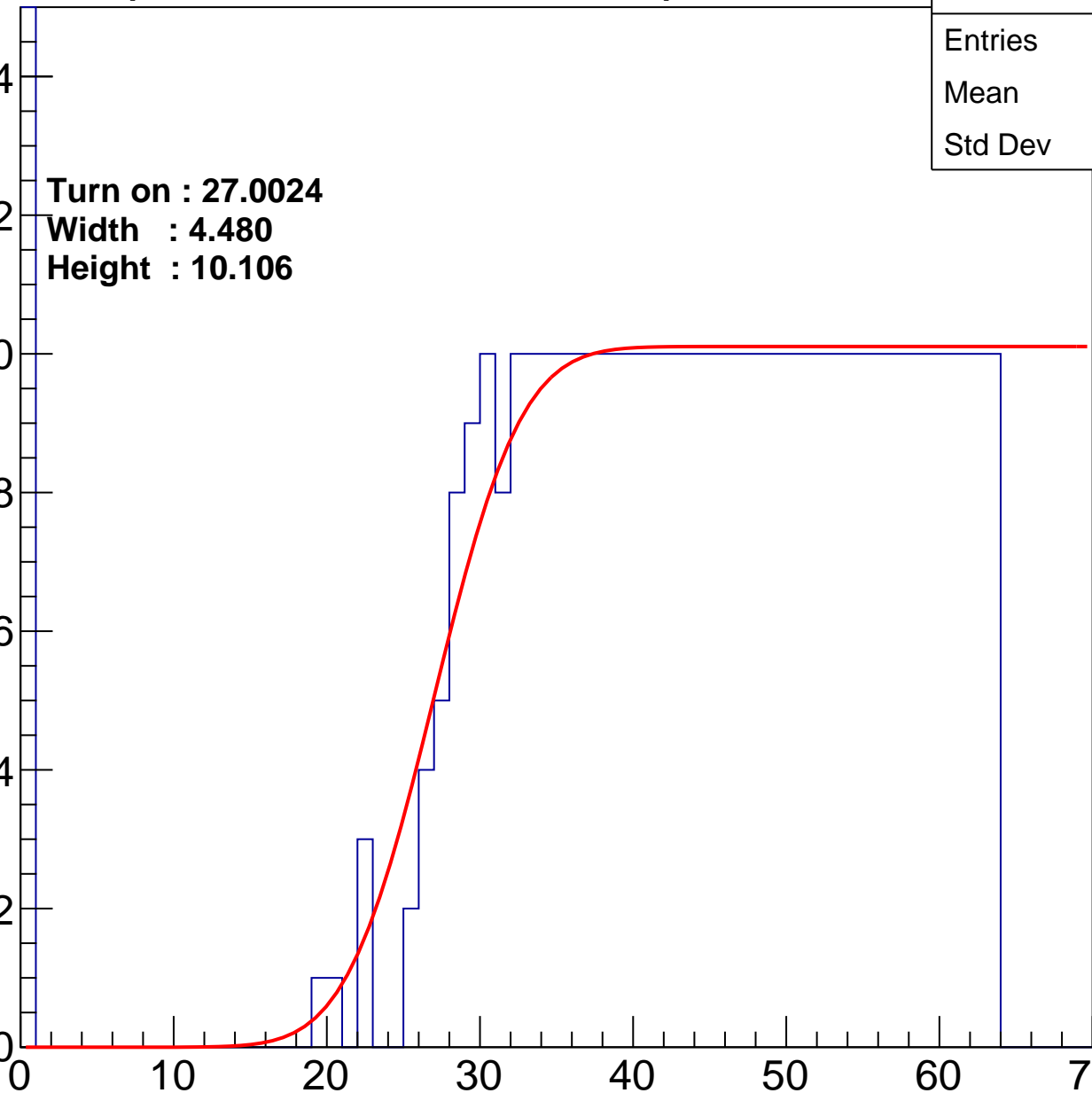
Width : 4.480

Height : 10.106

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch93

calib_packv5_041523_1651.root, FC#0, port C2

Entries	422
Mean	40.47
Std Dev	16.18

Turn on : 25.3757

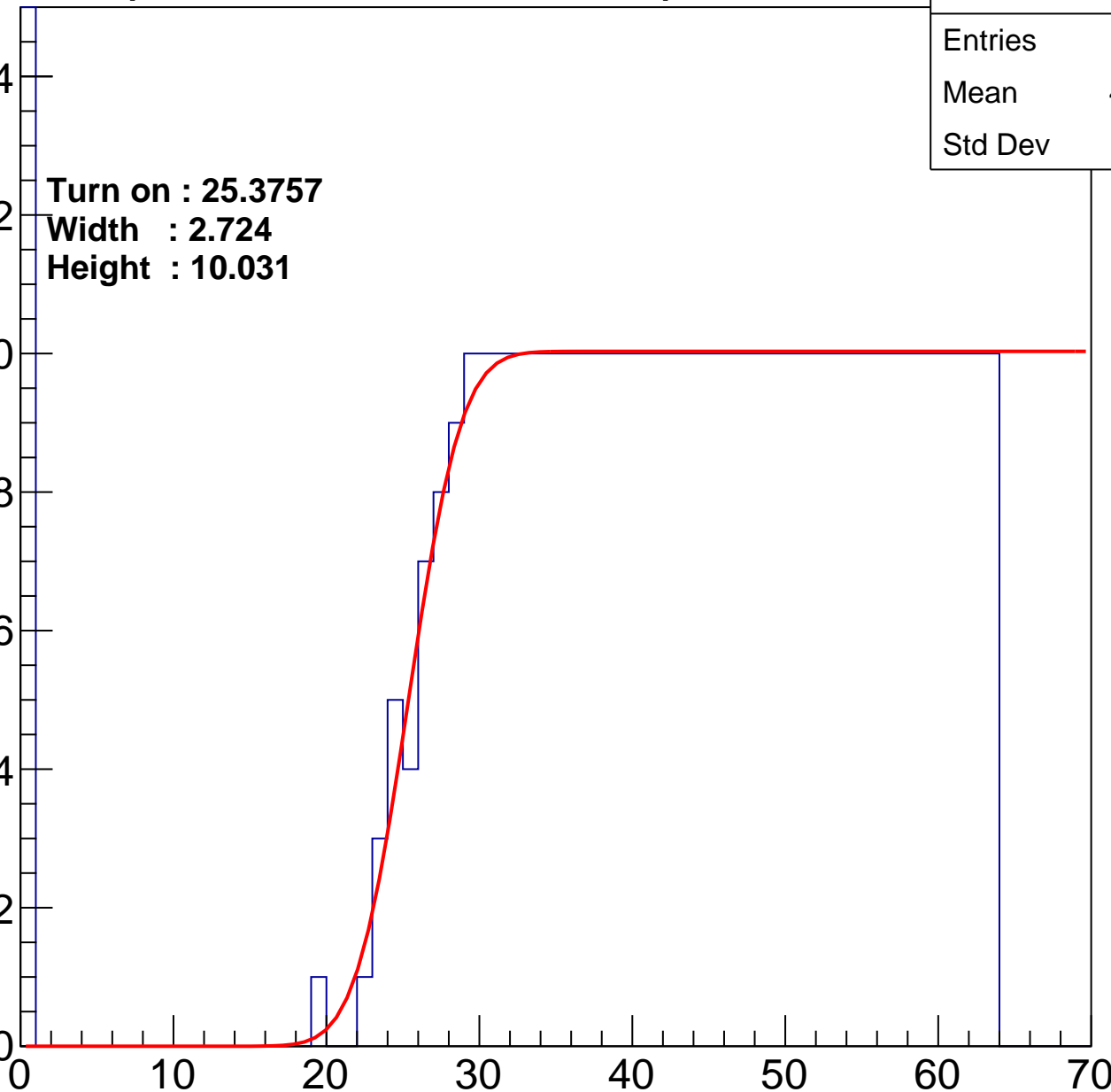
Width : 2.724

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch94

calib_packv5_041523_1651.root, FC#0, port C2

Entries	444
Mean	38.47
Std Dev	18.01

Turn on : 24.9781

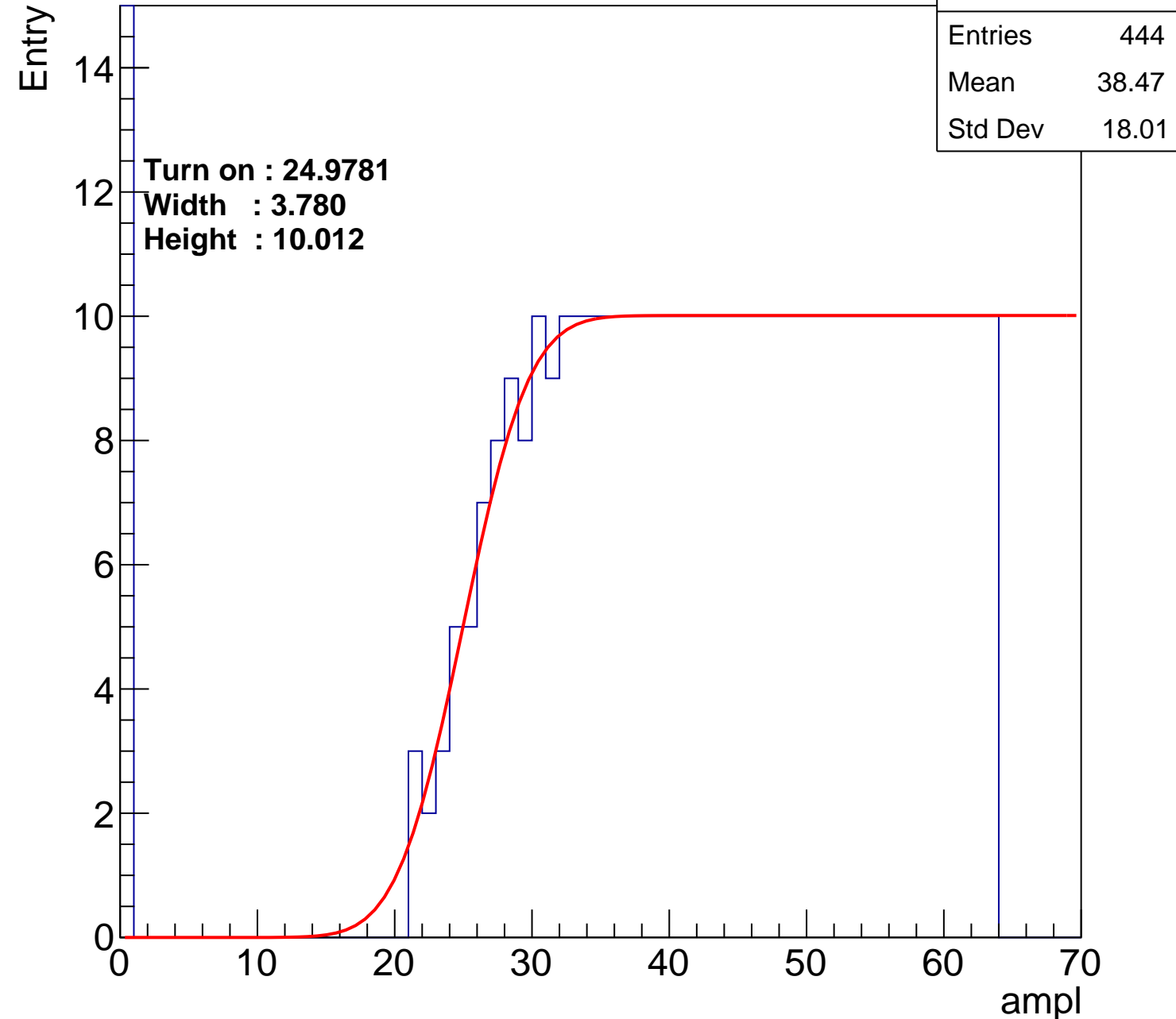
Width : 3.780

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch95

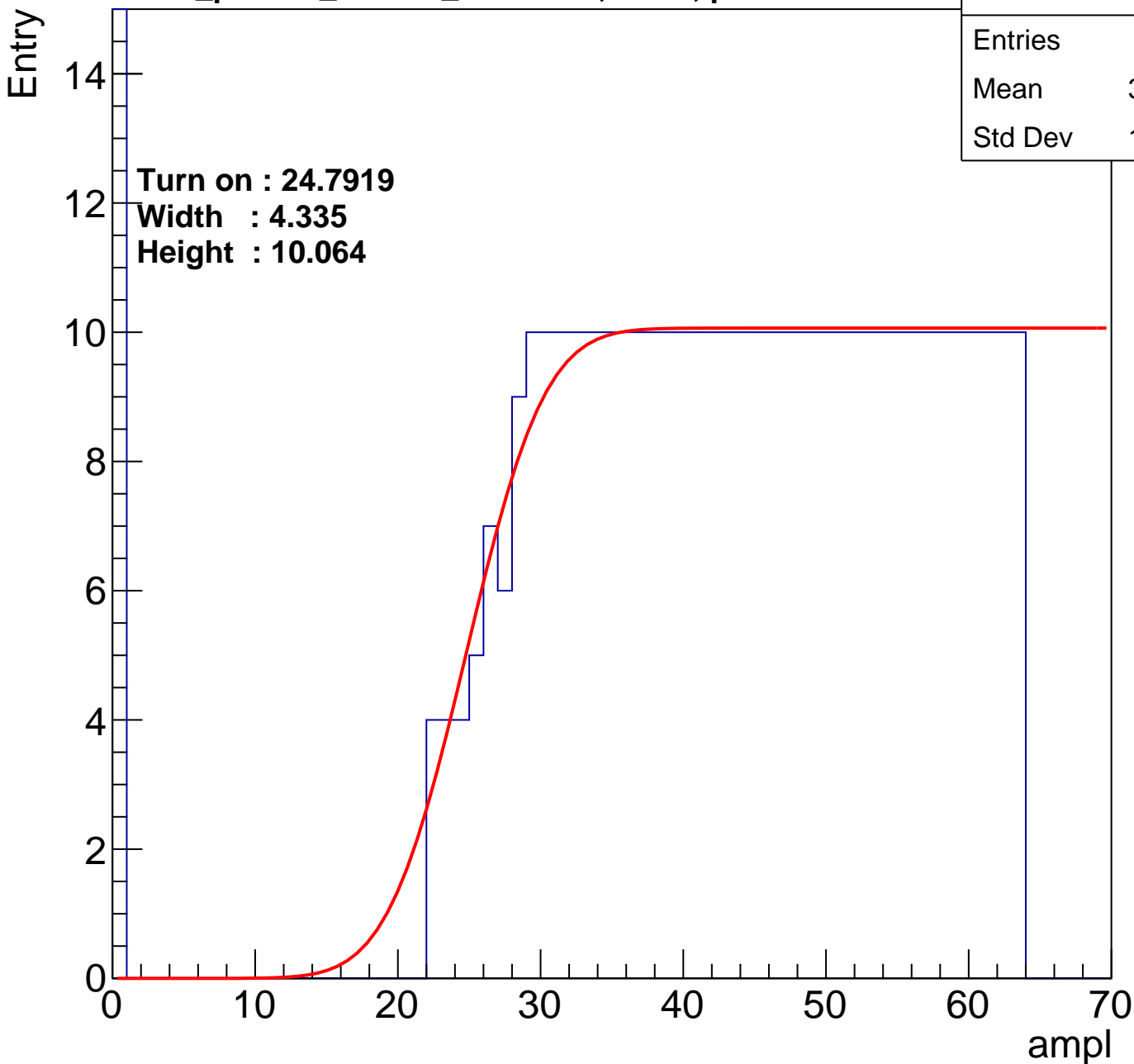
calib_packv5_041523_1651.root, FC#0, port C2

Entries	428
Mean	39.95
Std Dev	16.67

Turn on : 24.7919

Width : 4.335

Height : 10.064



B1L103S, U24-ch96

calib_packv5_041523_1651.root, FC#0, port C2

Entries	456
Mean	38.04
Std Dev	18.01

Turn on : 24.4412

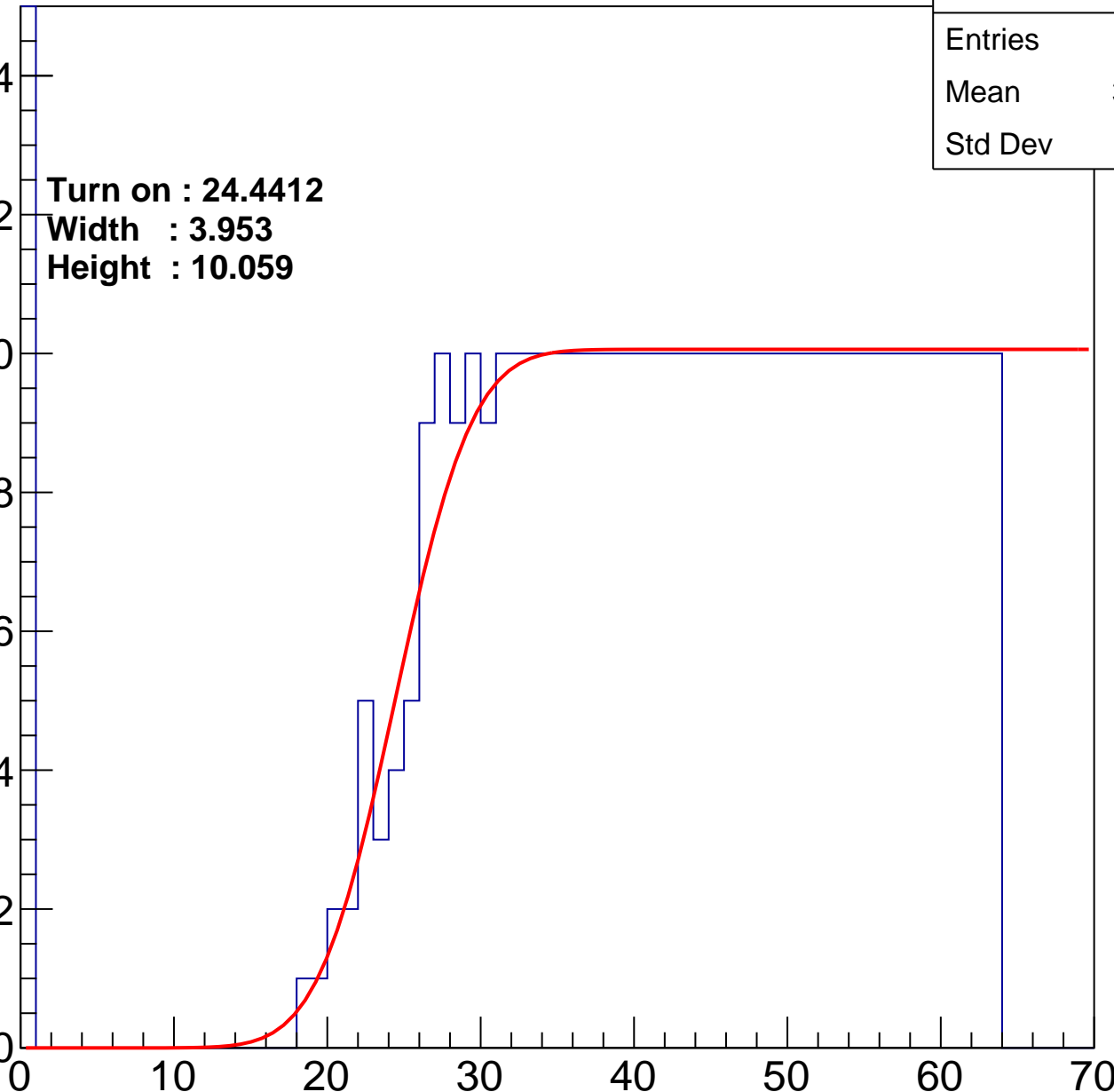
Width : 3.953

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch97

calib_packv5_041523_1651.root, FC#0, port C2

Entries	441
Mean	38.83
Std Dev	17.63

Turn on : 24.8886

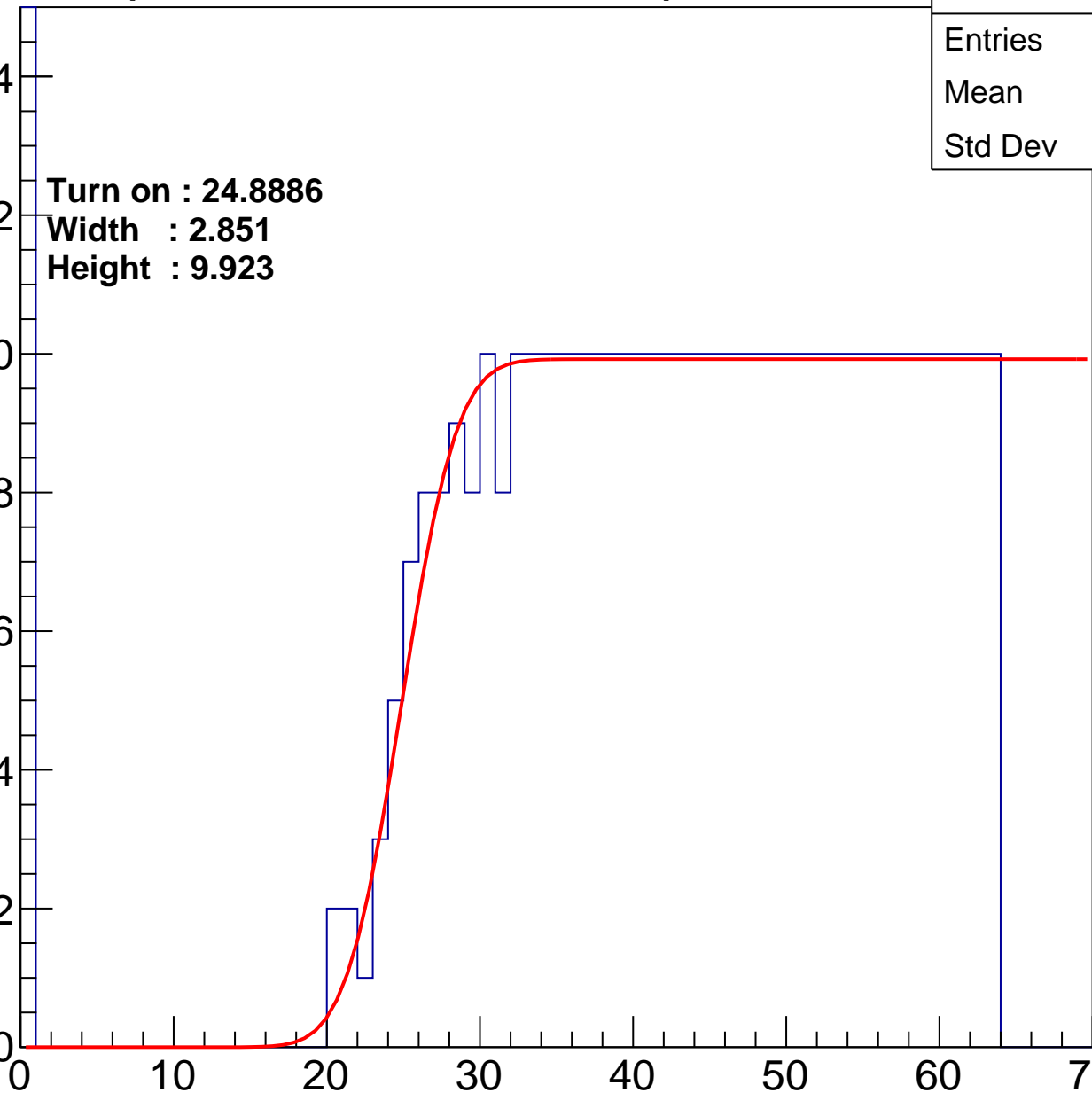
Width : 2.851

Height : 9.923

Entry

14
12
10
8
6
4
2
0

ampl

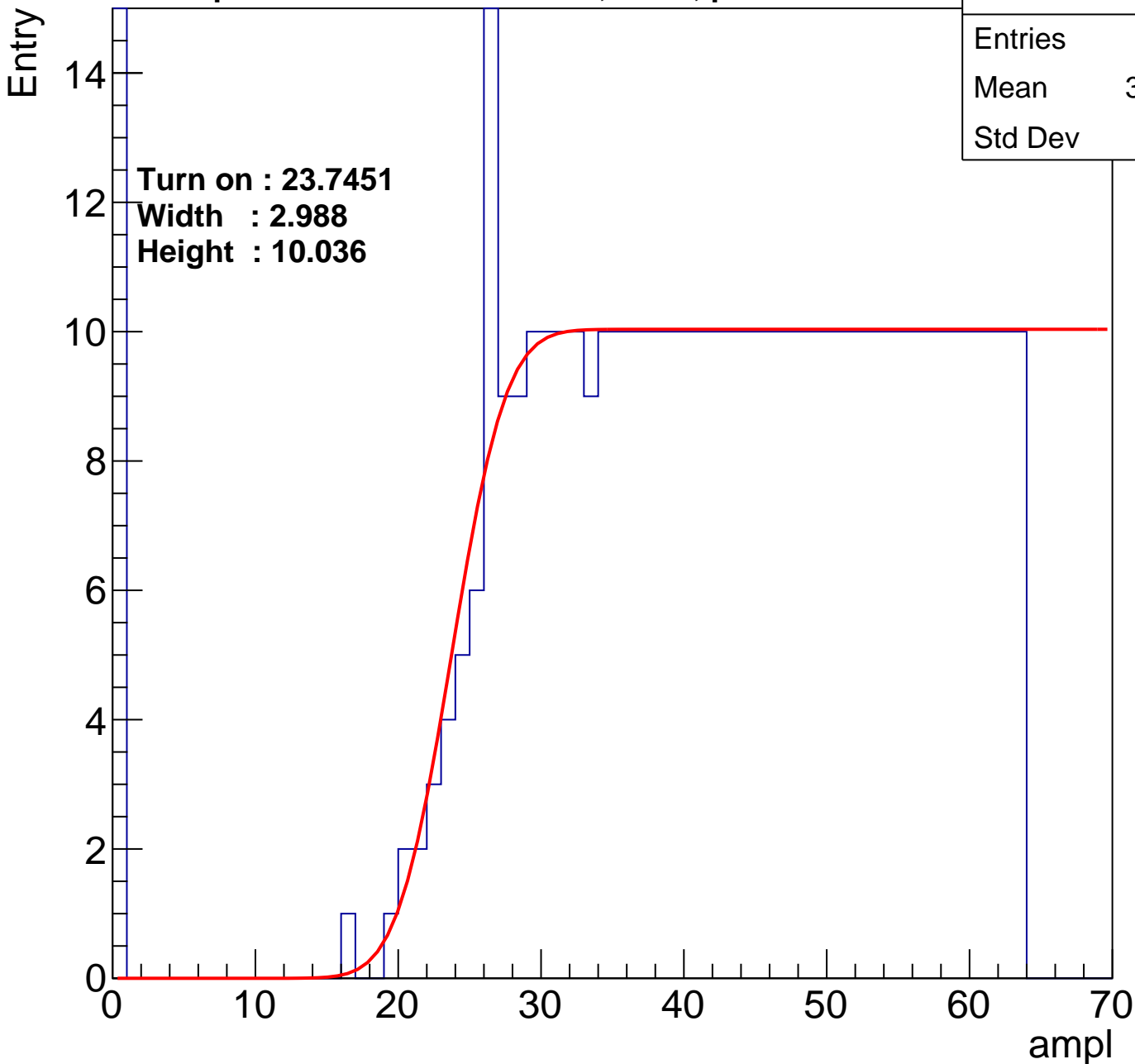


B1L103S, U24-ch98

calib_packv5_041523_1651.root, FC#0, port C2

Entries	471
Mean	38.03
Std Dev	17.3

Turn on : 23.7451
Width : 2.988
Height : 10.036



B1L103S, U24-ch99

calib_packv5_041523_1651.root, FC#0, port C2

Entries	444
Mean	38.5
Std Dev	18

Turn on : 25.6413

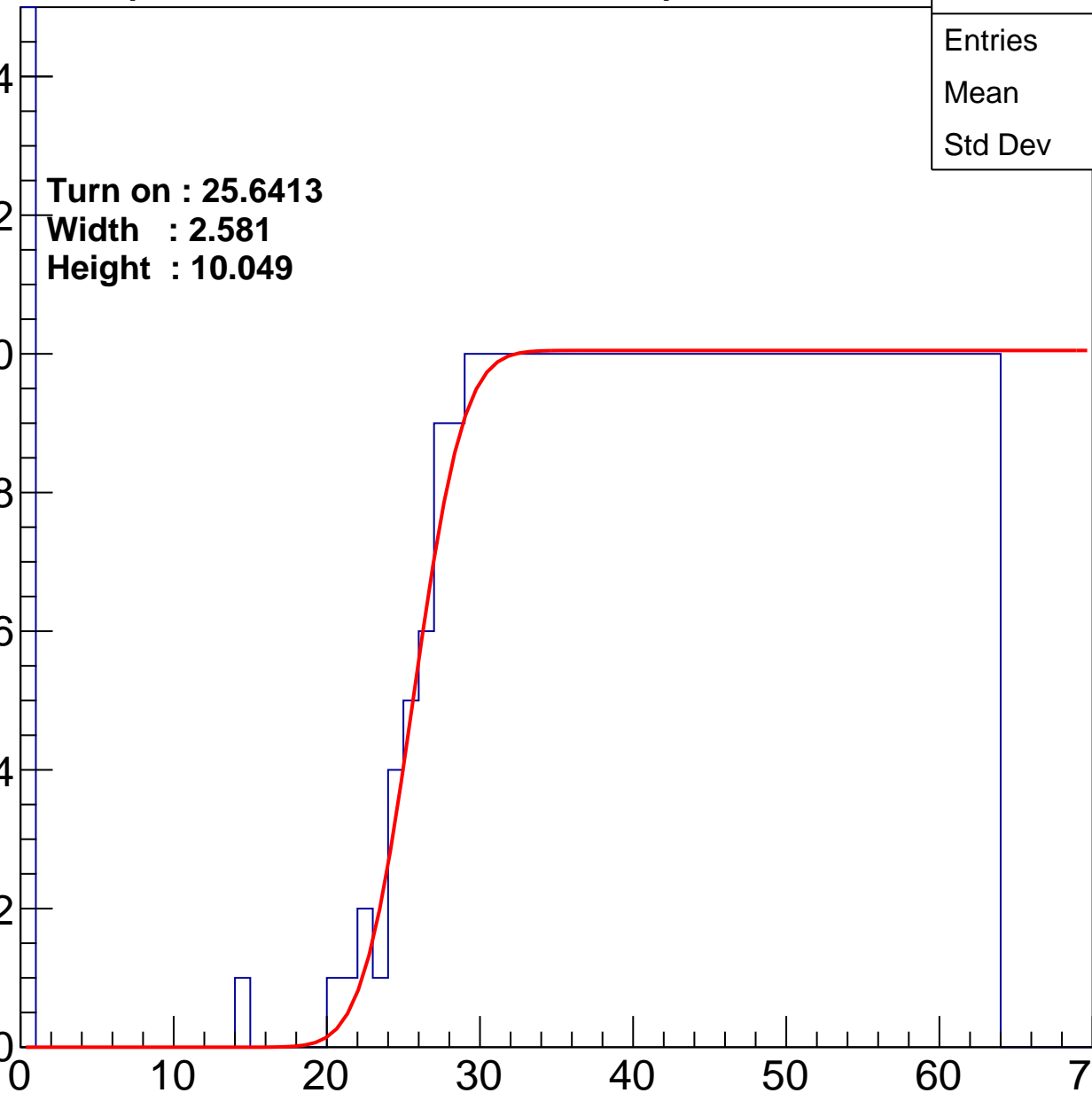
Width : 2.581

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch100

calib_packv5_041523_1651.root, FC#0, port C2

Entries	464
Mean	37.98
Std Dev	17.67

Turn on : 23.3858

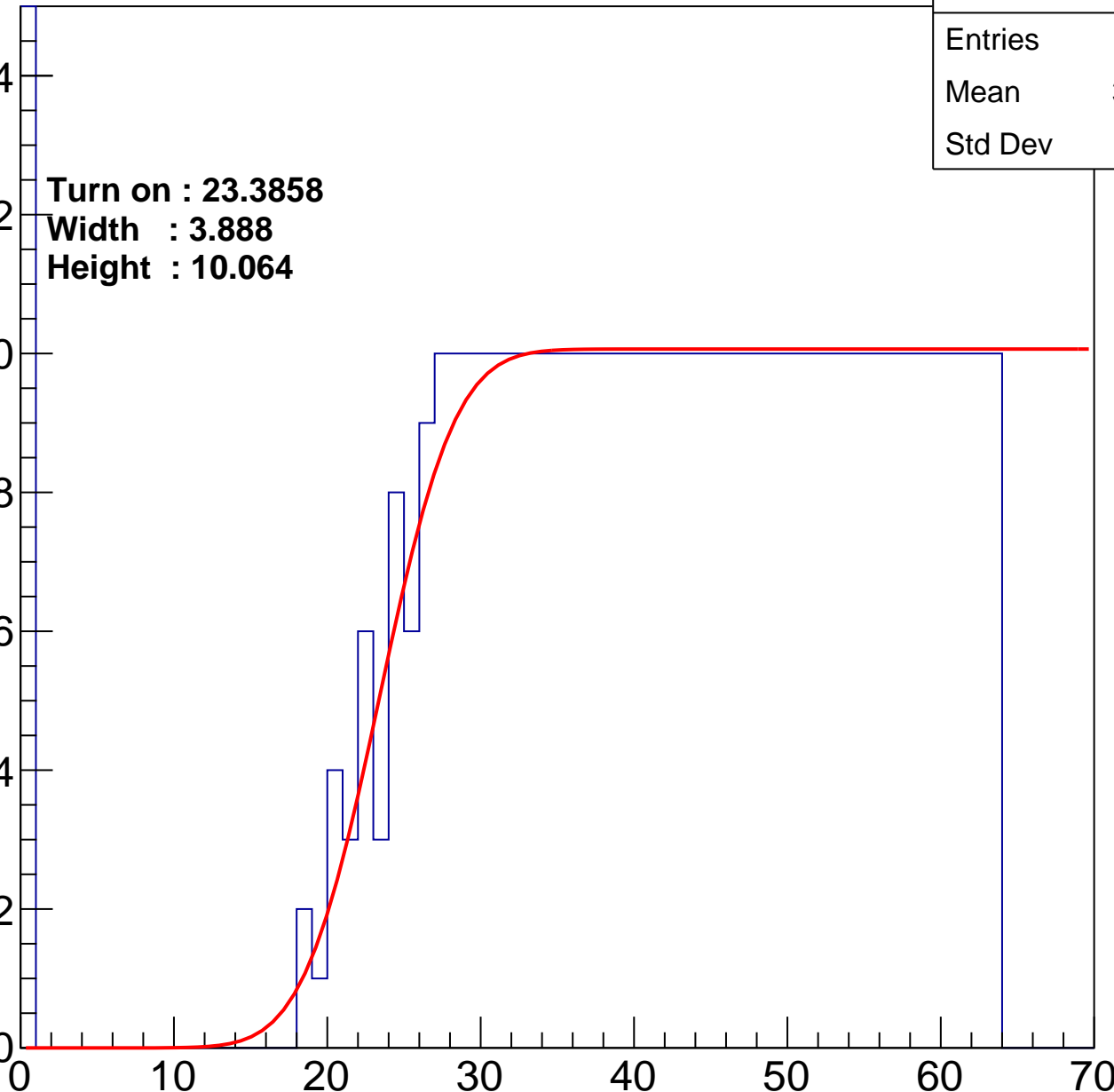
Width : 3.888

Height : 10.064

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch101

calib_packv5_041523_1651.root, FC#0, port C2

Entries	442
Mean	38.72
Std Dev	17.78

Turn on : 25.2019

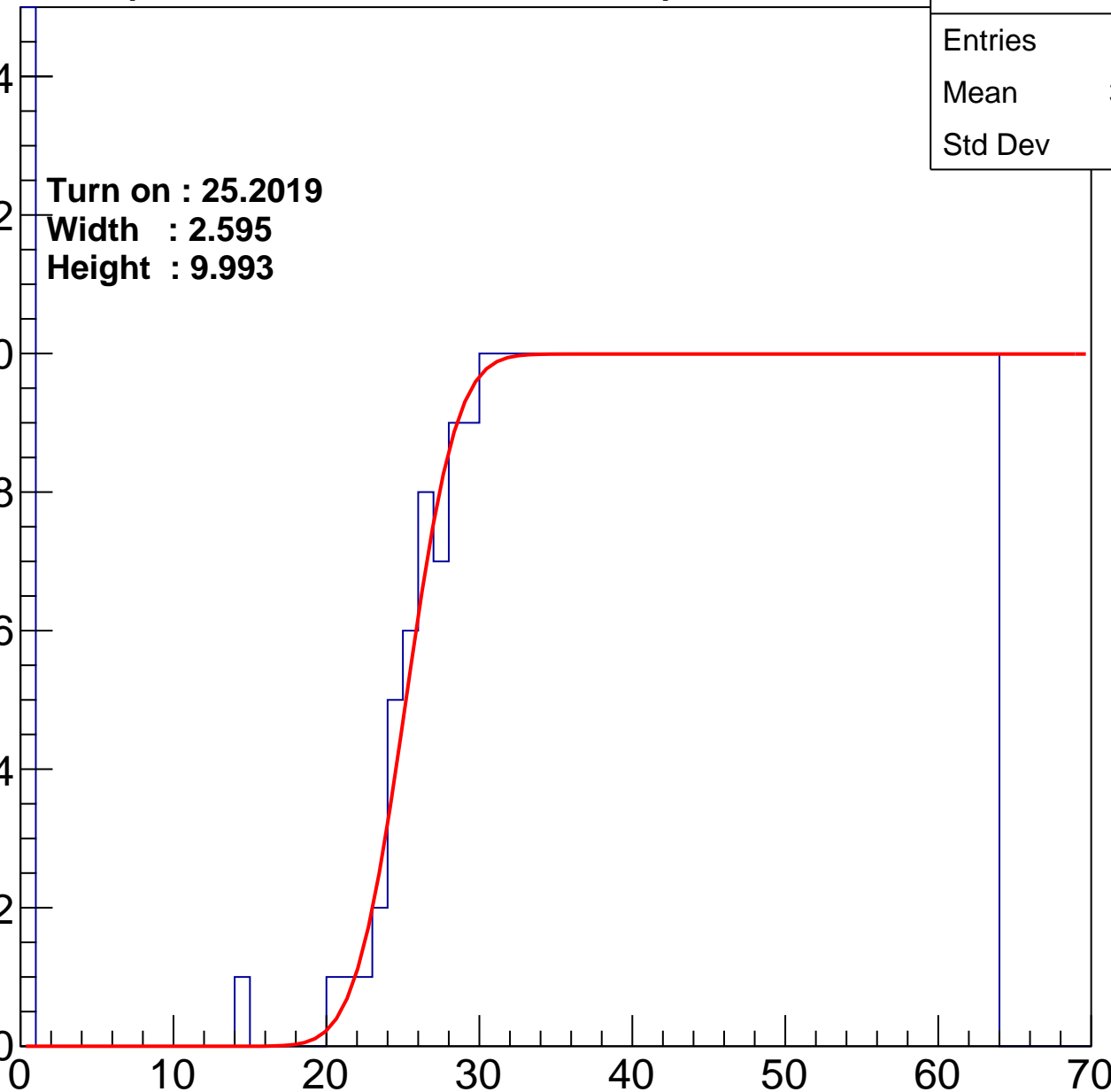
Width : 2.595

Height : 9.993

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch102

calib_packv5_041523_1651.root, FC#0, port C2

Entries	457
Mean	38.3
Std Dev	17.6

Turn on : 23.5148

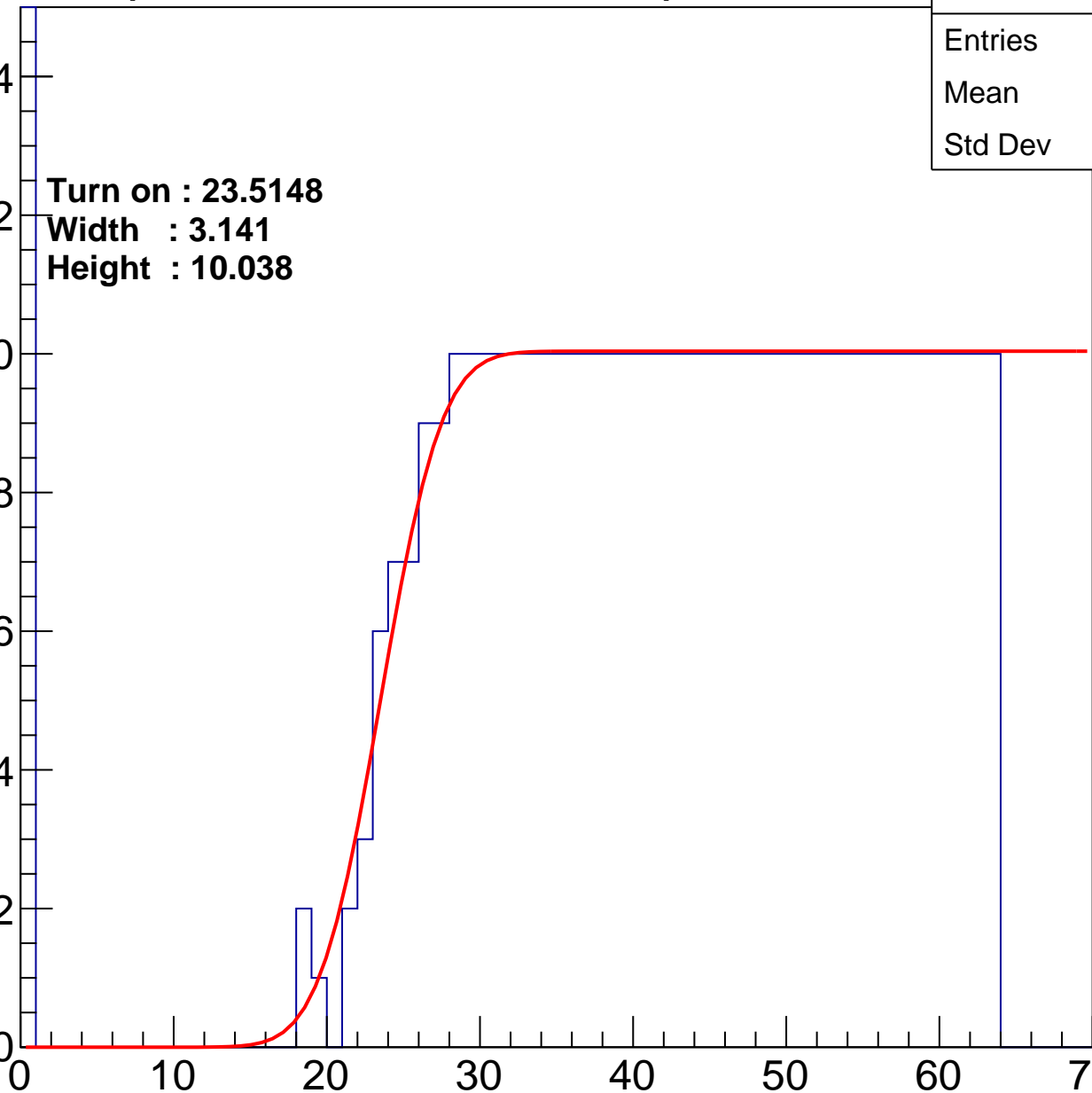
Width : 3.141

Height : 10.038

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch103

calib_packv5_041523_1651.root, FC#0, port C2

Entries	453
Mean	37.78
Std Dev	18.54

Turn on : 25.2512

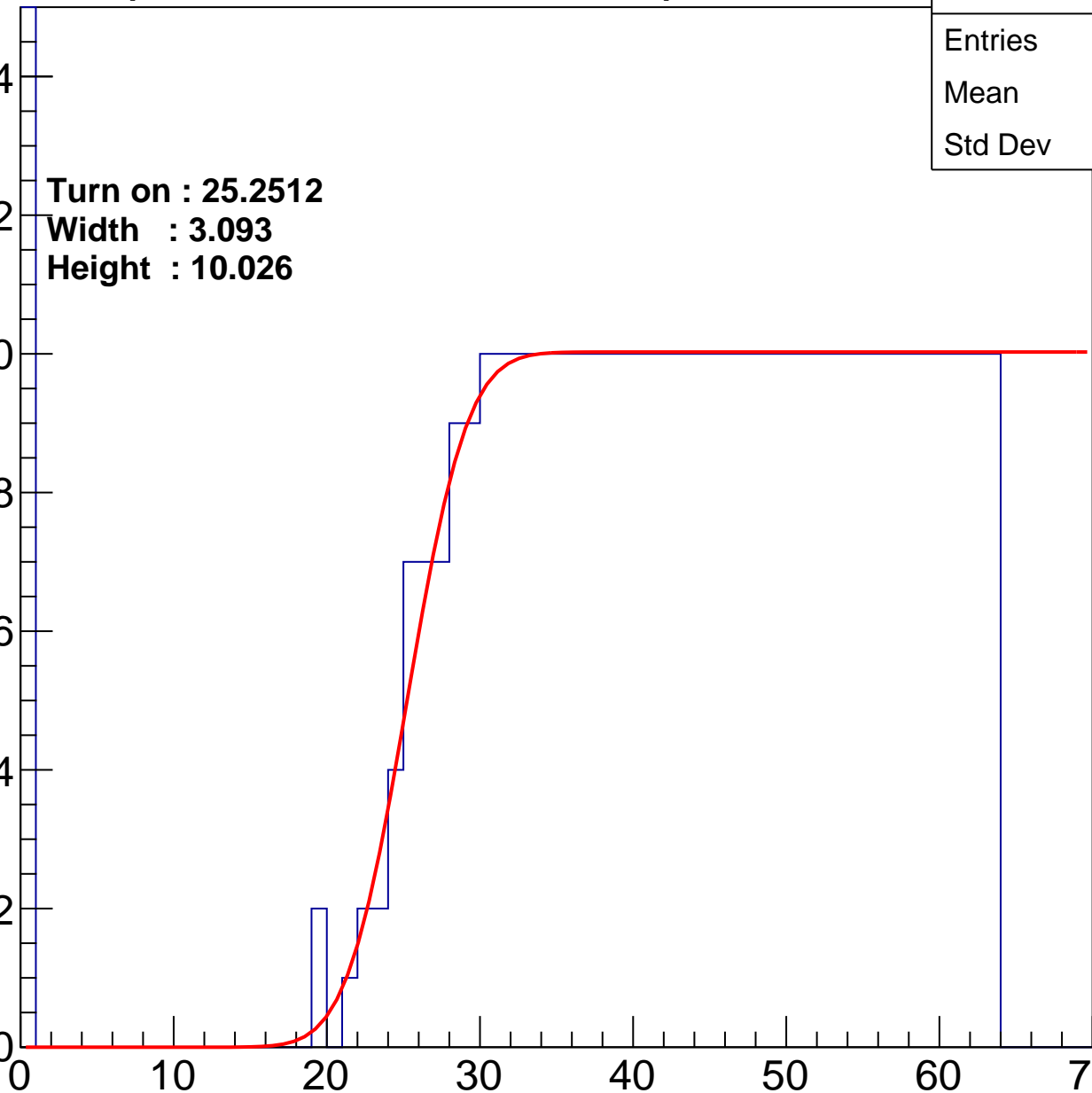
Width : 3.093

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch104

calib_packv5_041523_1651.root, FC#0, port C2

Entries	467
Mean	37.41
Std Dev	18.35

Turn on : 23.8442

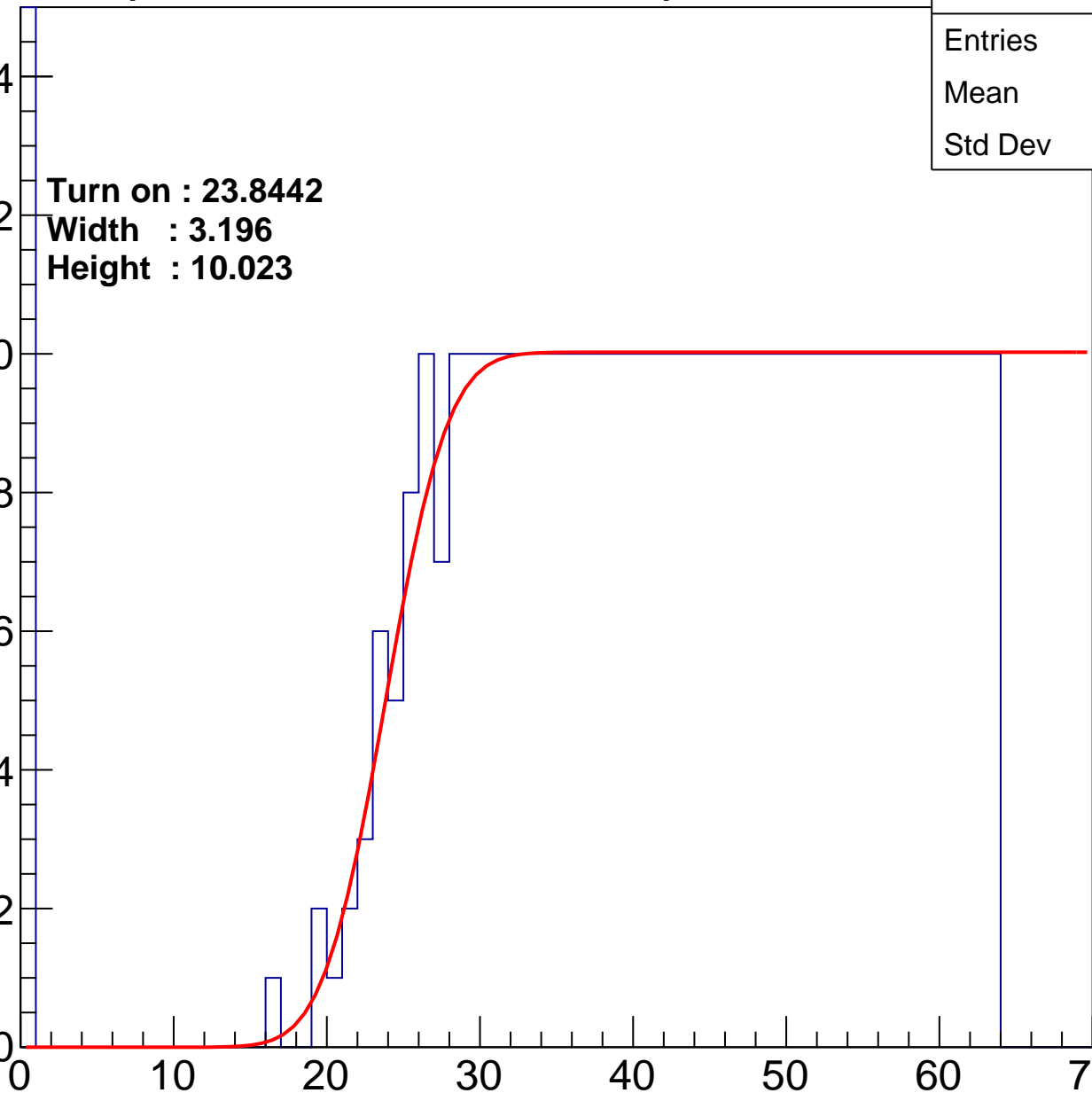
Width : 3.196

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch105

calib_packv5_041523_1651.root, FC#0, port C2

Entries	454
Mean	38.56
Std Dev	17.34

Turn on : 24.0837

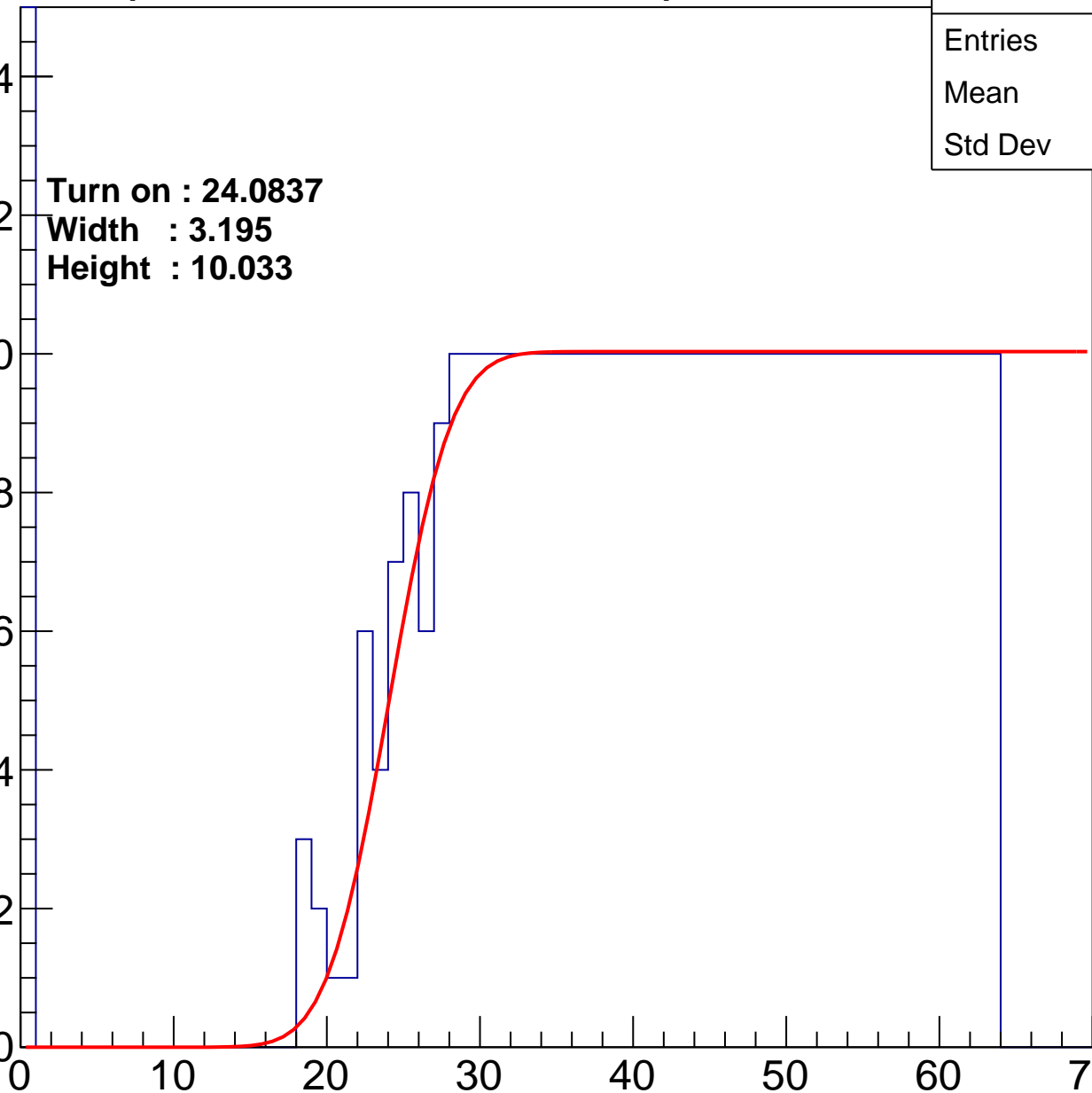
Width : 3.195

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch106

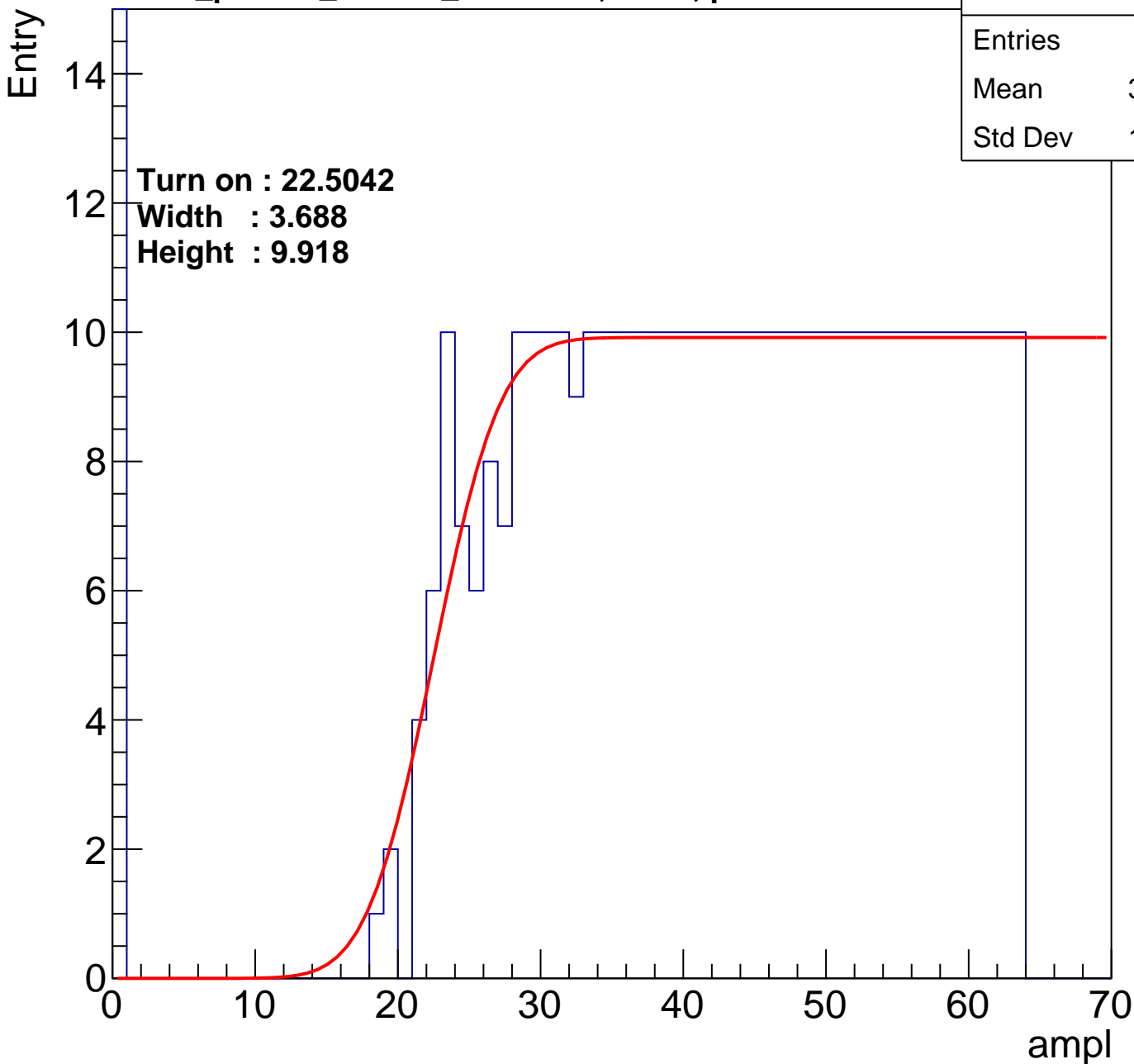
calib_packv5_041523_1651.root, FC#0, port C2

Entries	485
Mean	36.22
Std Dev	19.06

Turn on : 22.5042

Width : 3.688

Height : 9.918



B1L103S, U24-ch107

calib_packv5_041523_1651.root, FC#0, port C2

Entries	454
Mean	38.13
Std Dev	17.96

Turn on : 24.7335

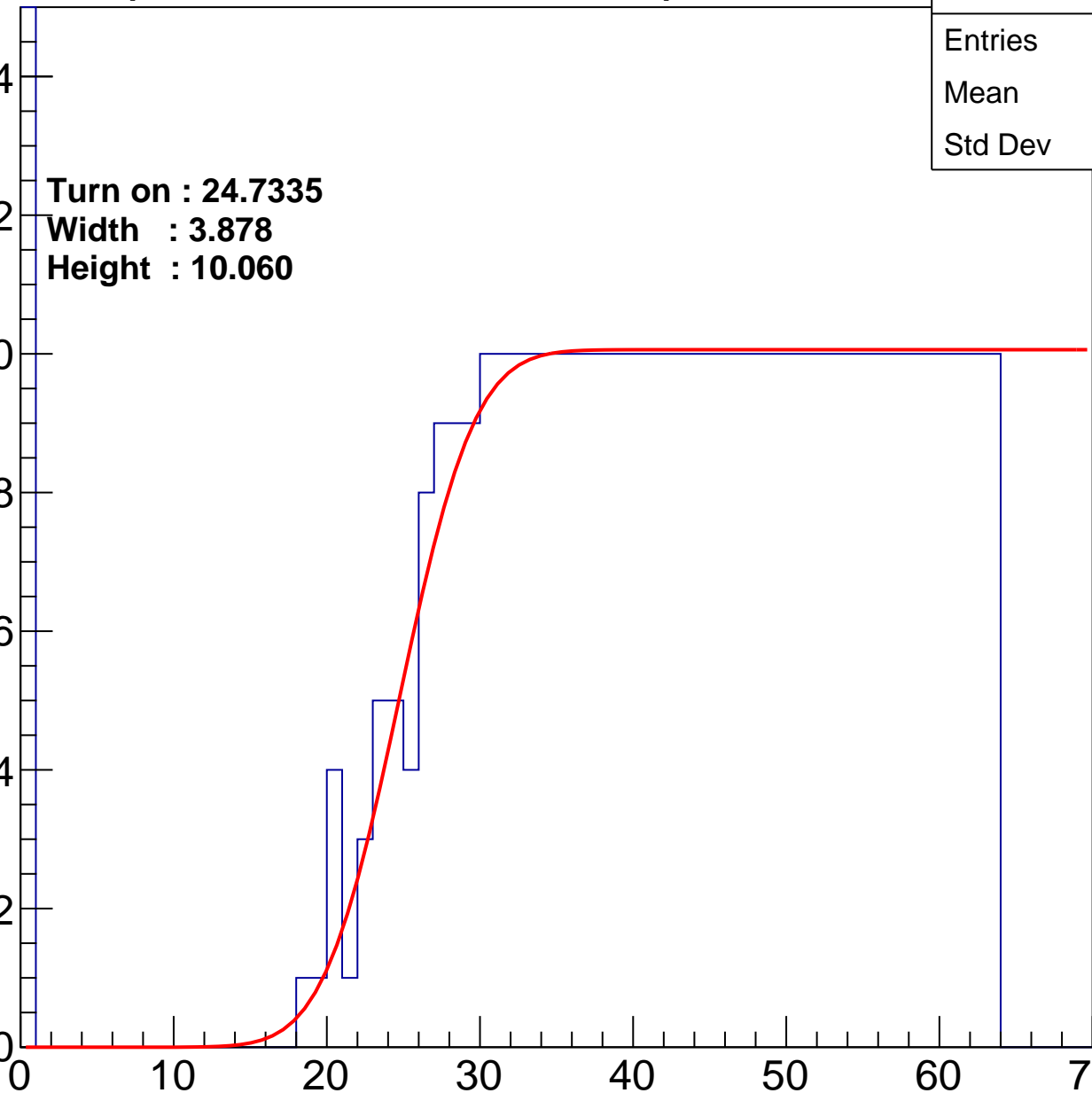
Width : 3.878

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch108

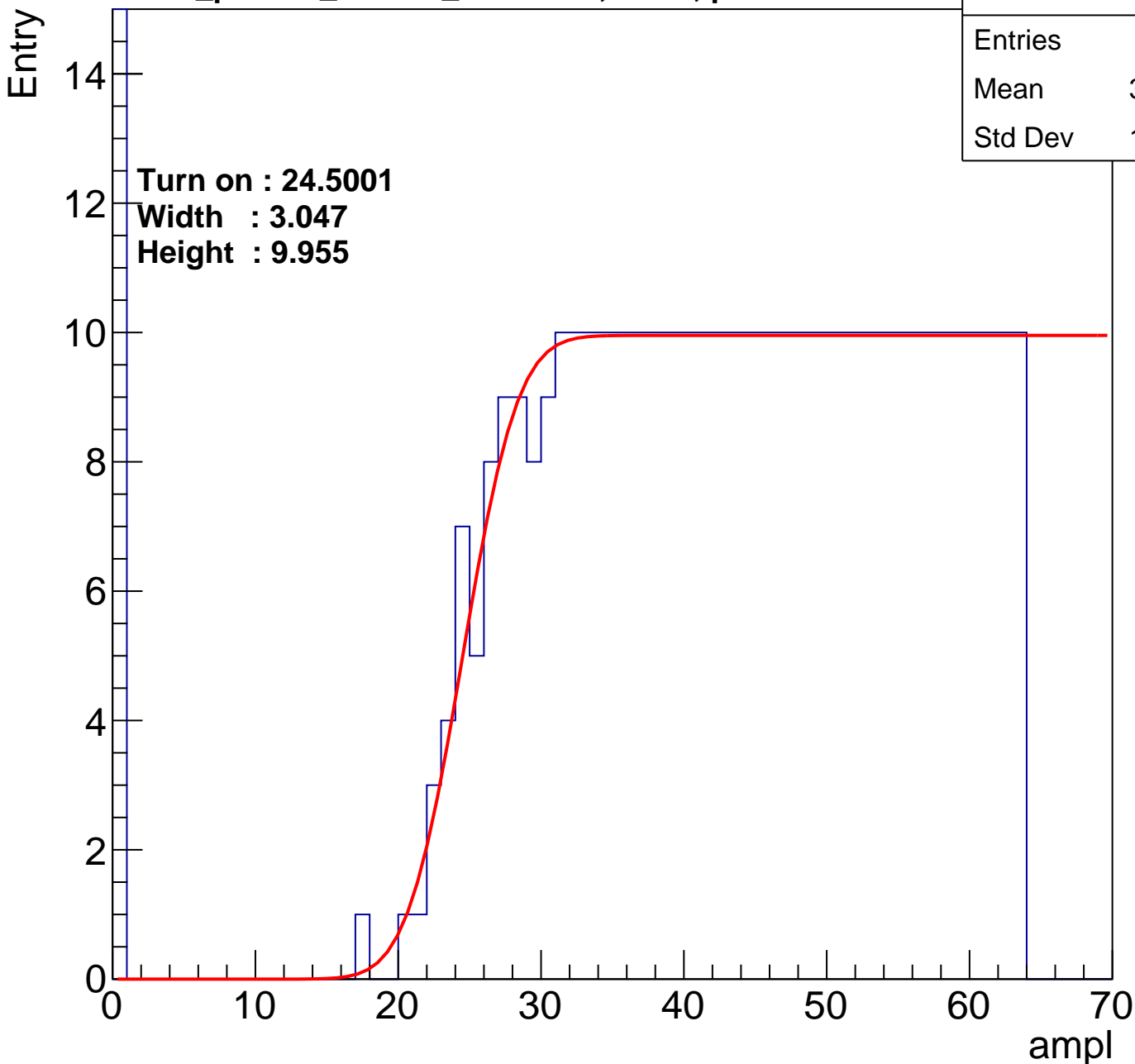
calib_packv5_041523_1651.root, FC#0, port C2

Entries	454
Mean	37.94
Std Dev	18.25

Turn on : 24.5001

Width : 3.047

Height : 9.955



B1L103S, U24-ch109

calib_packv5_041523_1651.root, FC#0, port C2

Entries	446
Mean	38.43
Std Dev	17.98

Turn on : 25.3665

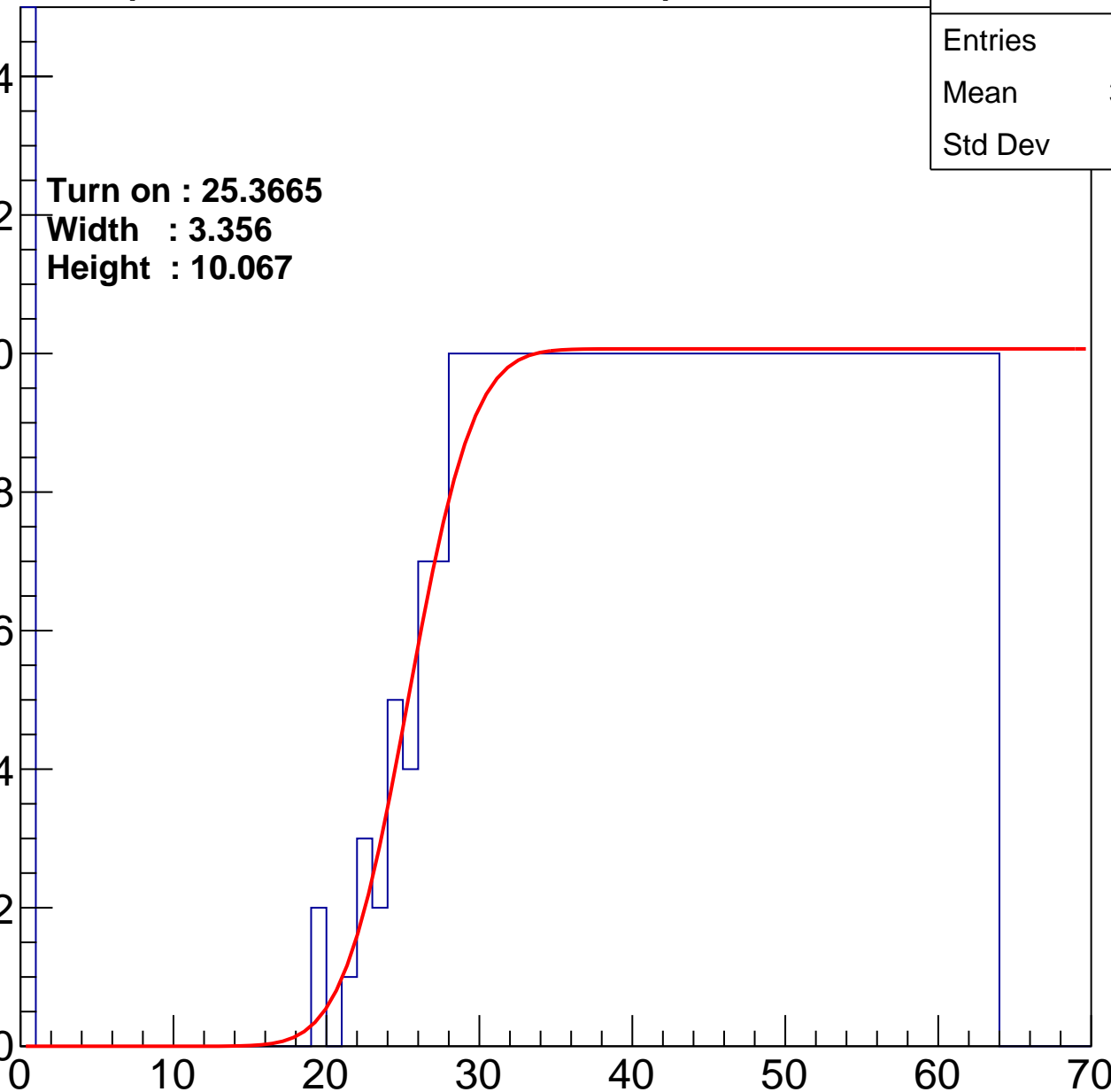
Width : 3.356

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch110

calib_packv5_041523_1651.root, FC#0, port C2

Entries	449
Mean	38.37
Std Dev	17.95

Turn on : 25.0459

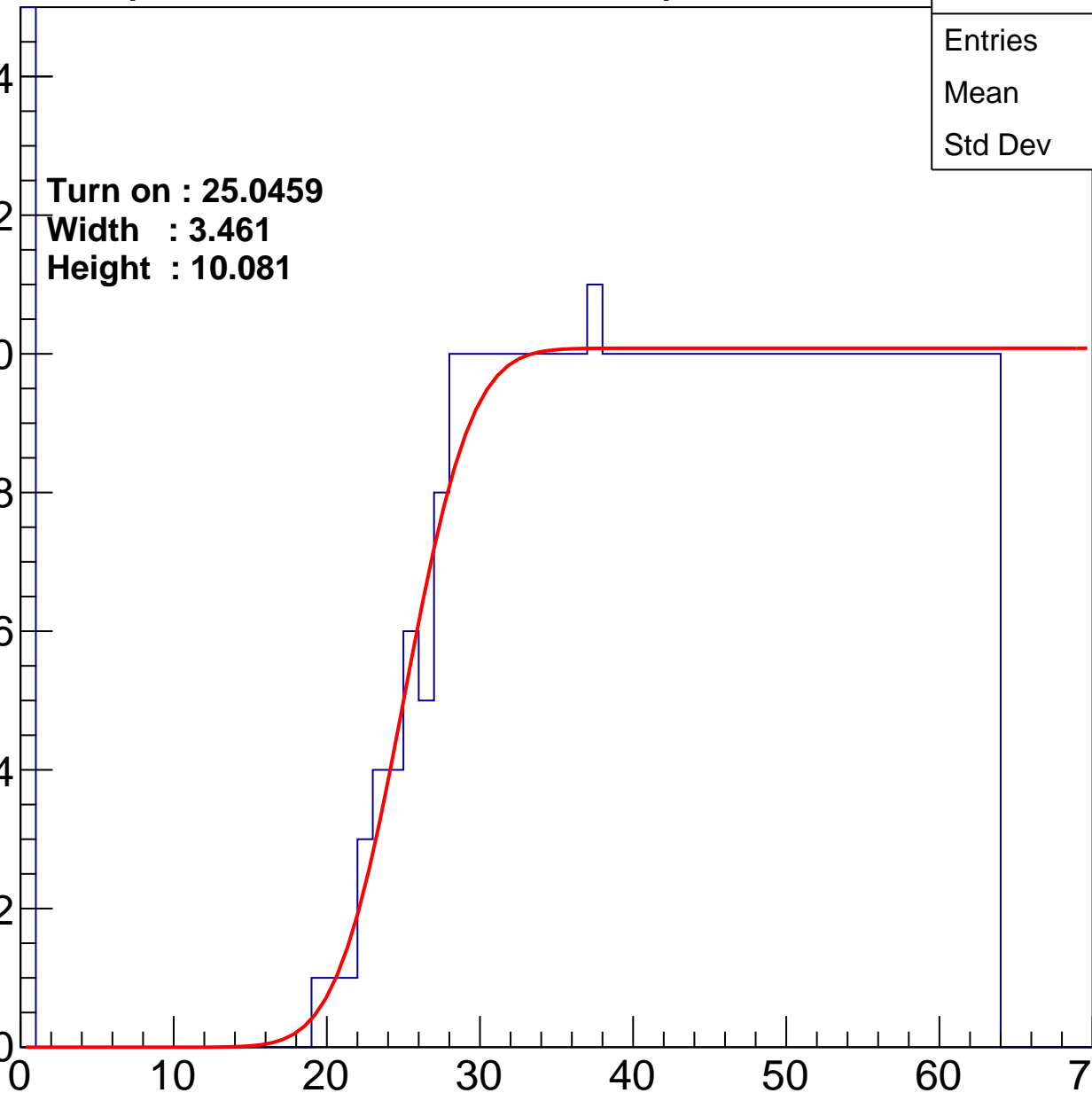
Width : 3.461

Height : 10.081

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch111

calib_packv5_041523_1651.root, FC#0, port C2

Entries	418
Mean	39.91
Std Dev	17.31

Turn on : 26.7173

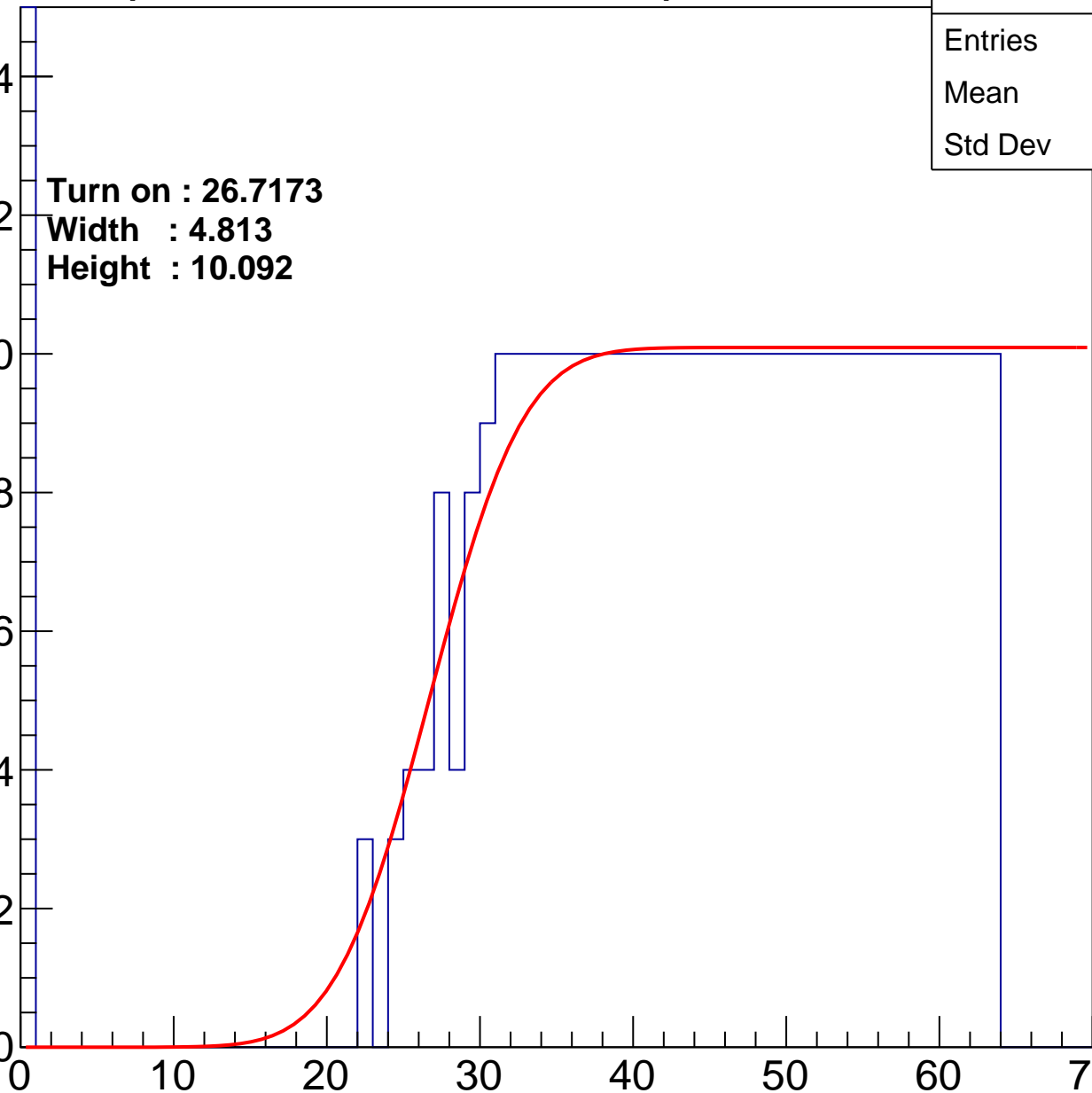
Width : 4.813

Height : 10.092

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch112

calib_packv5_041523_1651.root, FC#0, port C2

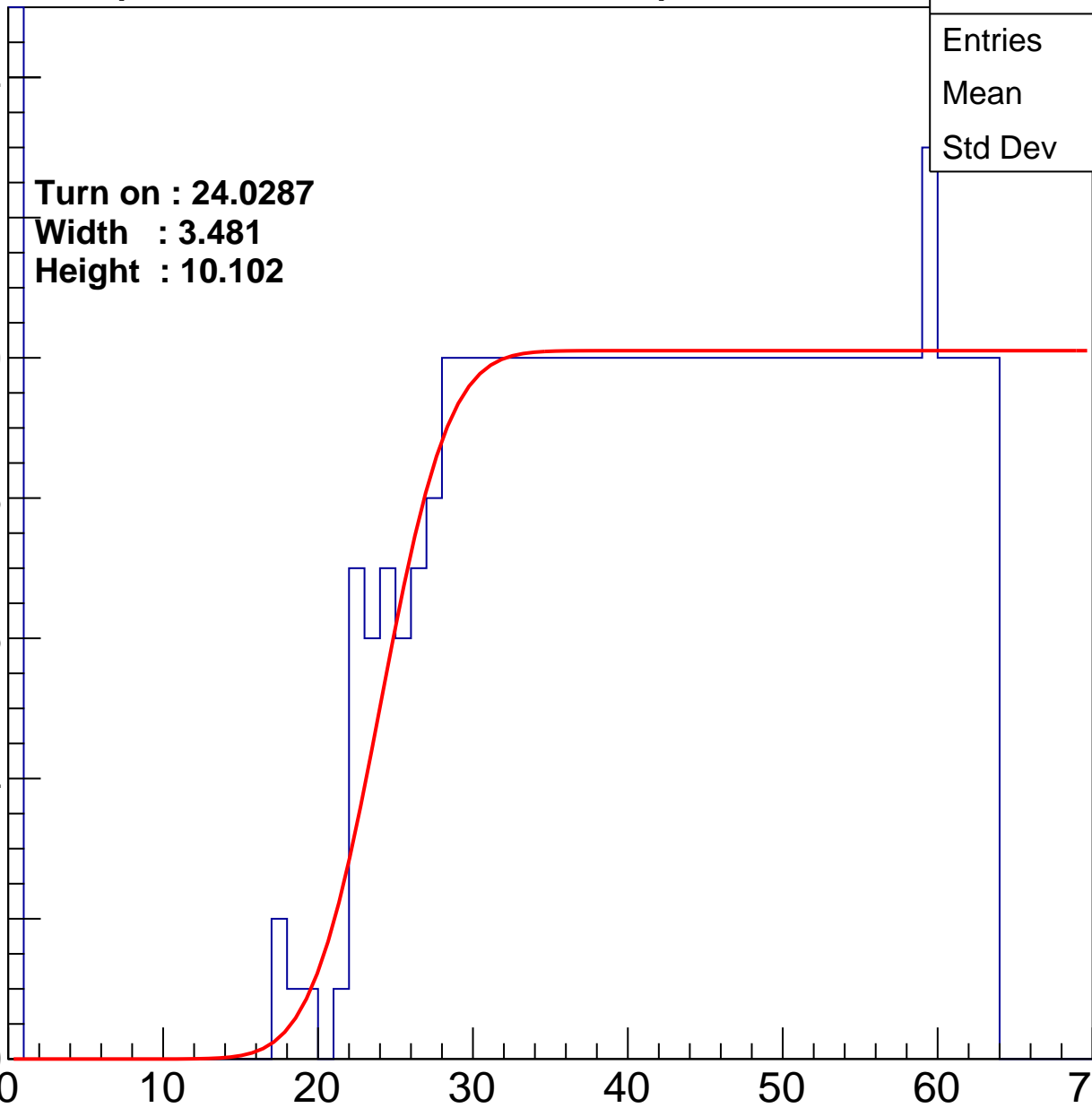
Entry

14
12
10
8
6
4
2
0

Turn on : 24.0287
Width : 3.481
Height : 10.102

Entries	471
Mean	37.49
Std Dev	18.39

ampl



B1L103S, U24-ch113

calib_packv5_041523_1651.root, FC#0, port C2

Entries	426
Mean	39.36
Std Dev	17.7

Turn on : 26.3079

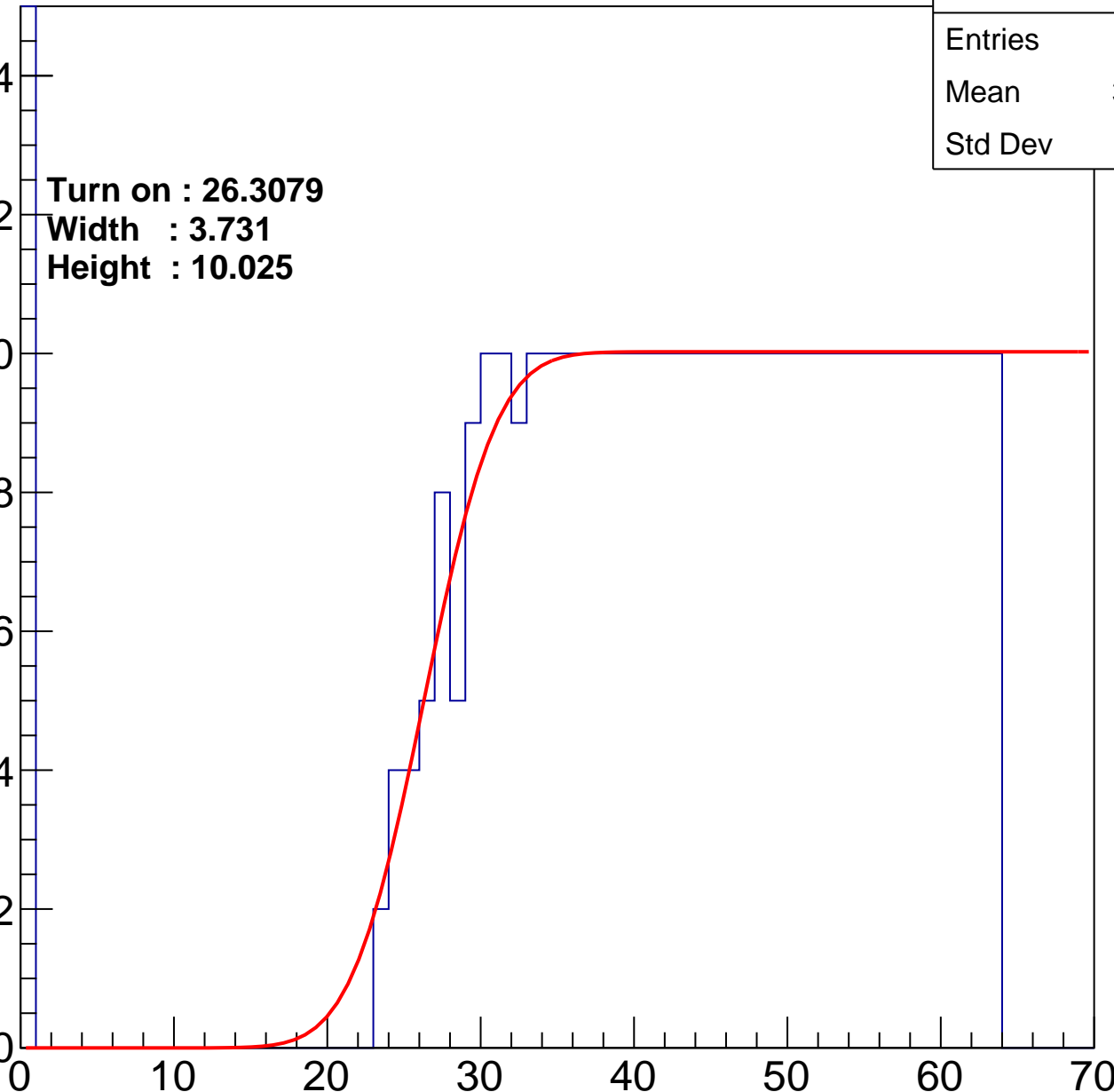
Width : 3.731

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch114

calib_packv5_041523_1651.root, FC#0, port C2

Entries	463
Mean	37.48
Std Dev	18.45

Turn on : 24.0345

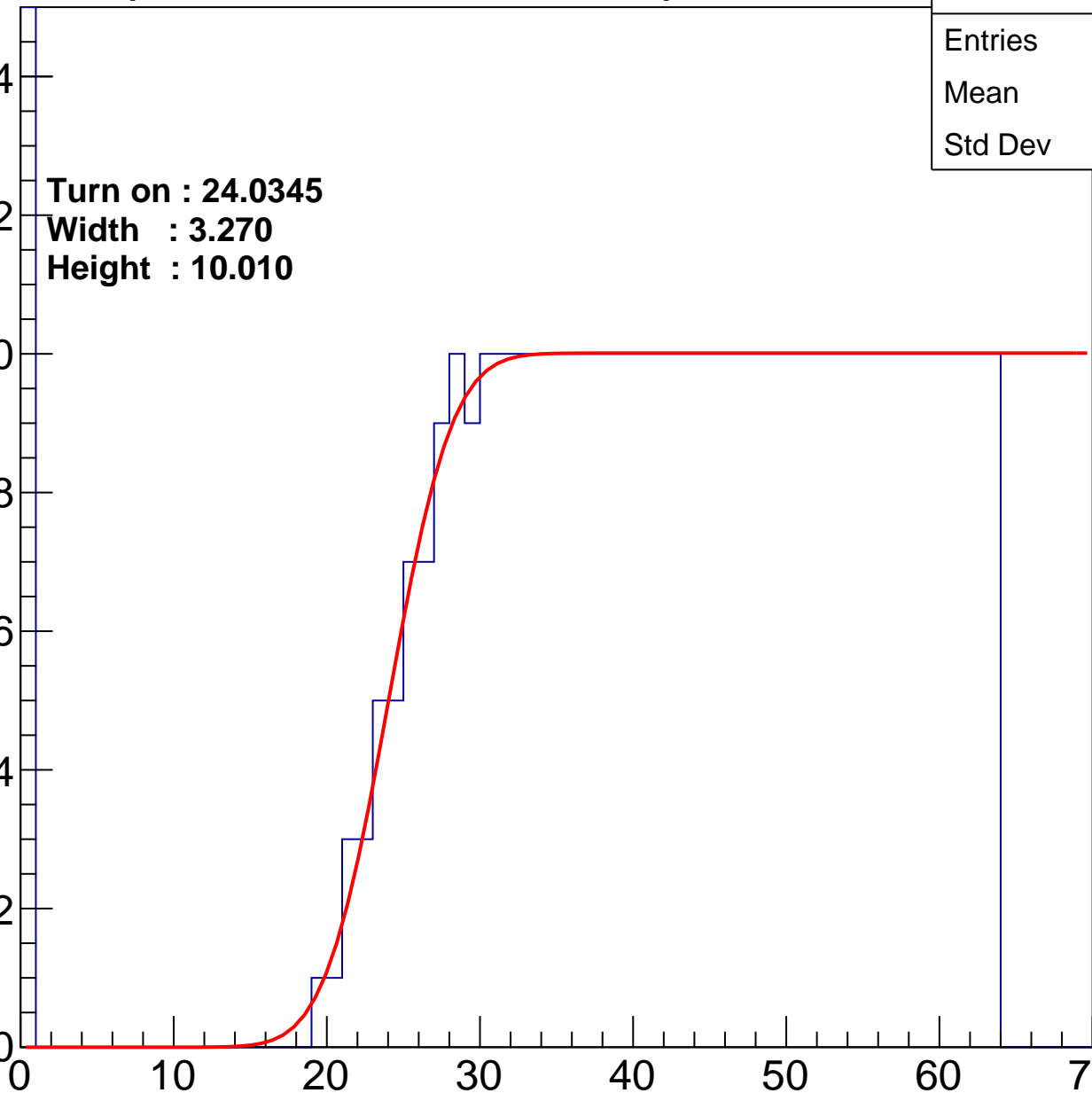
Width : 3.270

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch115

calib_packv5_041523_1651.root, FC#0, port C2

Entries	457
Mean	37.98
Std Dev	18.06

Turn on : 24.2776

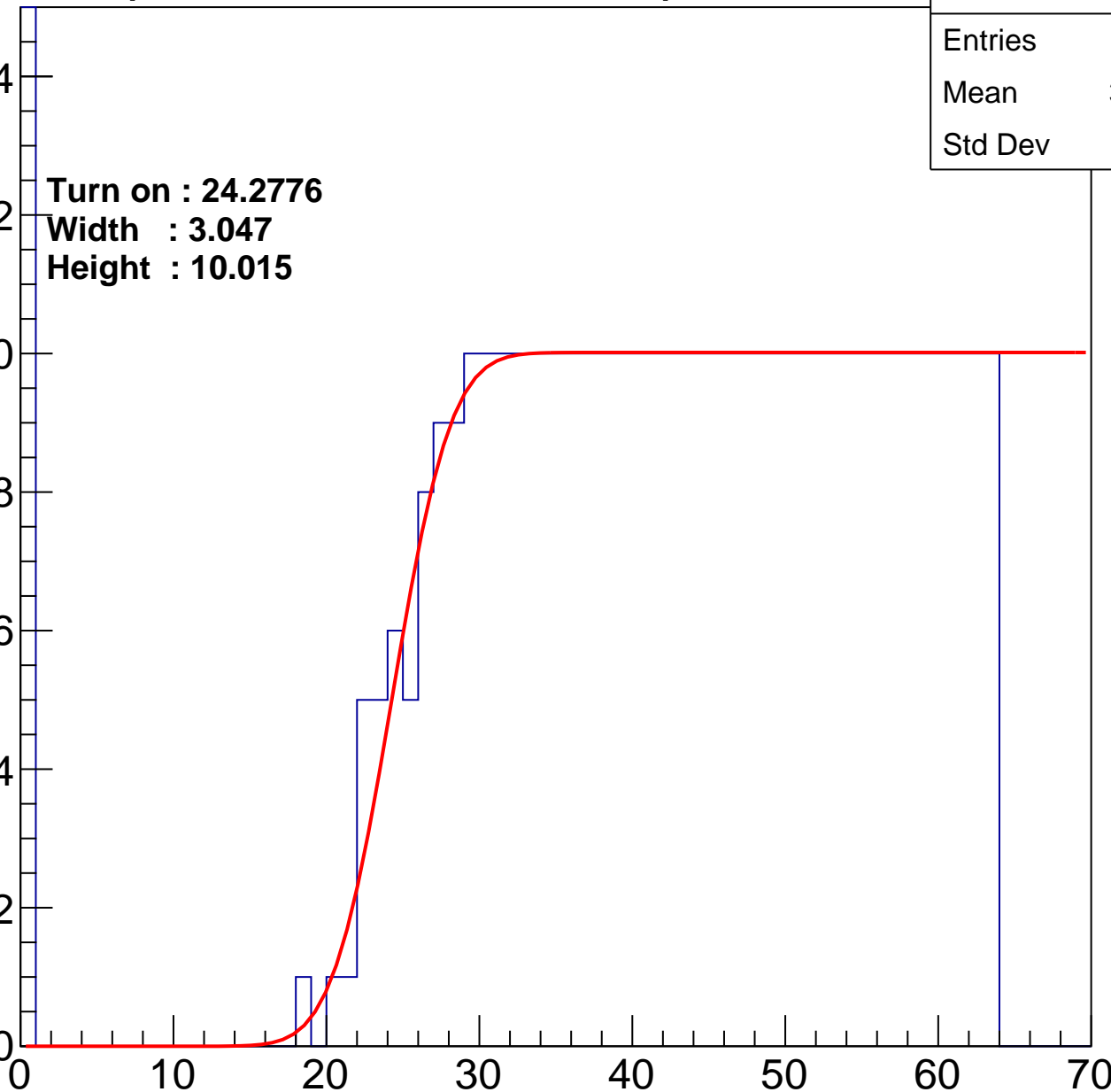
Width : 3.047

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch116

calib_packv5_041523_1651.root, FC#0, port C2

Entries	445
Mean	39.43
Std Dev	16.45

Turn on : 23.1736

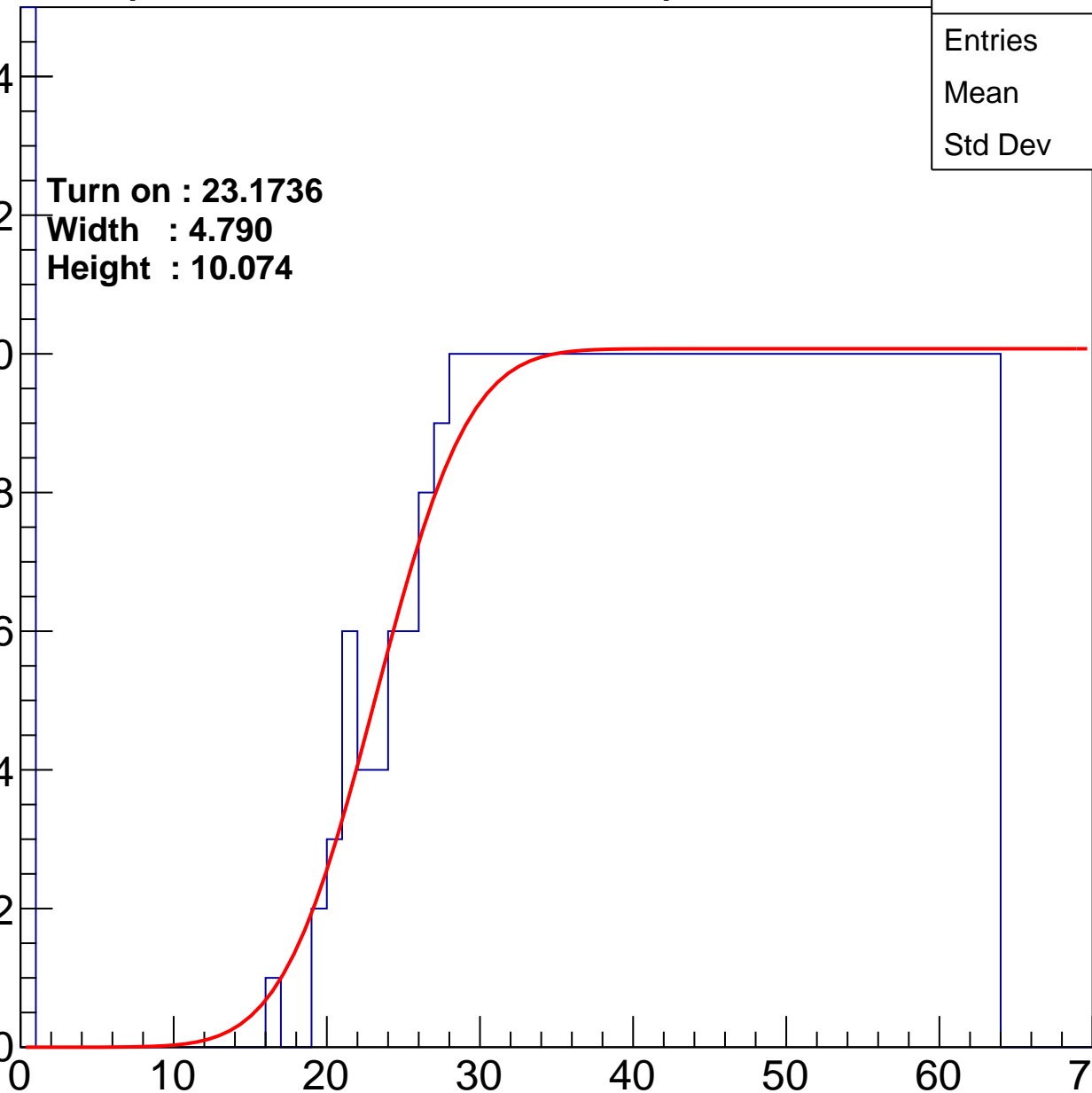
Width : 4.790

Height : 10.074

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch117

calib_packv5_041523_1651.root, FC#0, port C2

Entries	422
Mean	39.52
Std Dev	17.66

Turn on : 27.0838

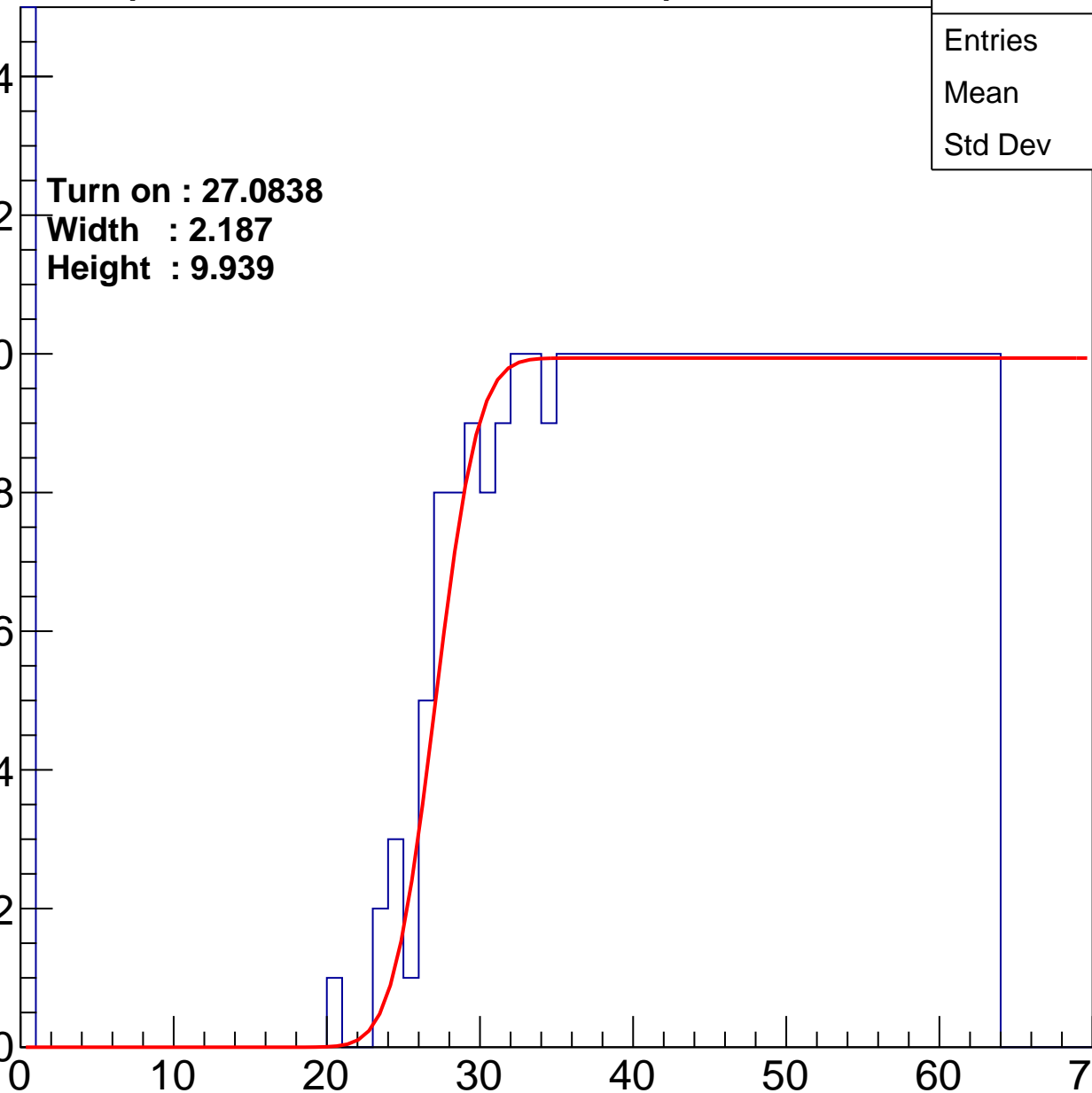
Width : 2.187

Height : 9.939

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch118

calib_packv5_041523_1651.root, FC#0, port C2

Entries	453
Mean	38.66
Std Dev	17.21

Turn on : 23.5230

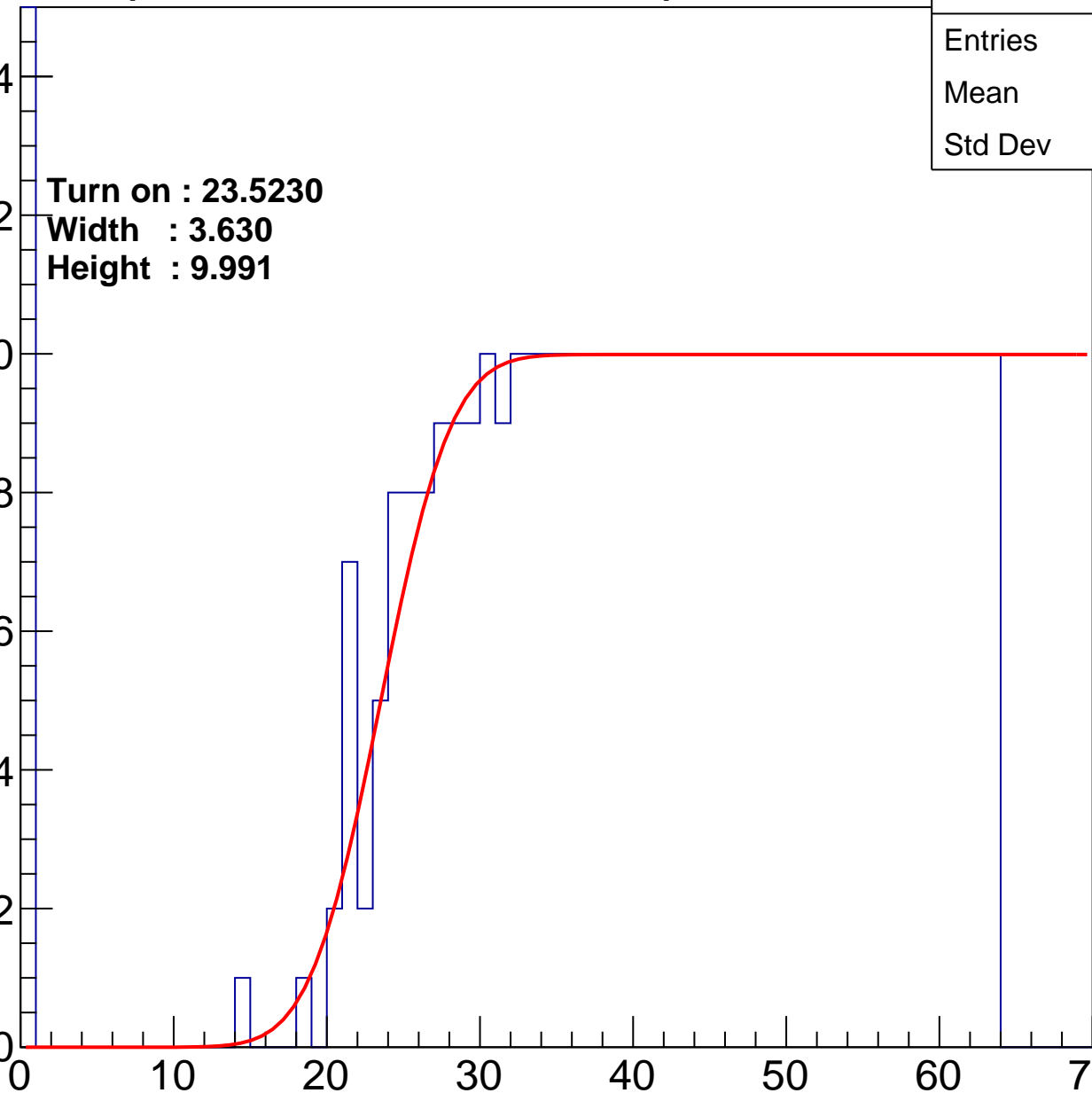
Width : 3.630

Height : 9.991

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch119

calib_packv5_041523_1651.root, FC#0, port C2

Entries	455
Mean	38.14
Std Dev	17.92

Turn on : 24.2680

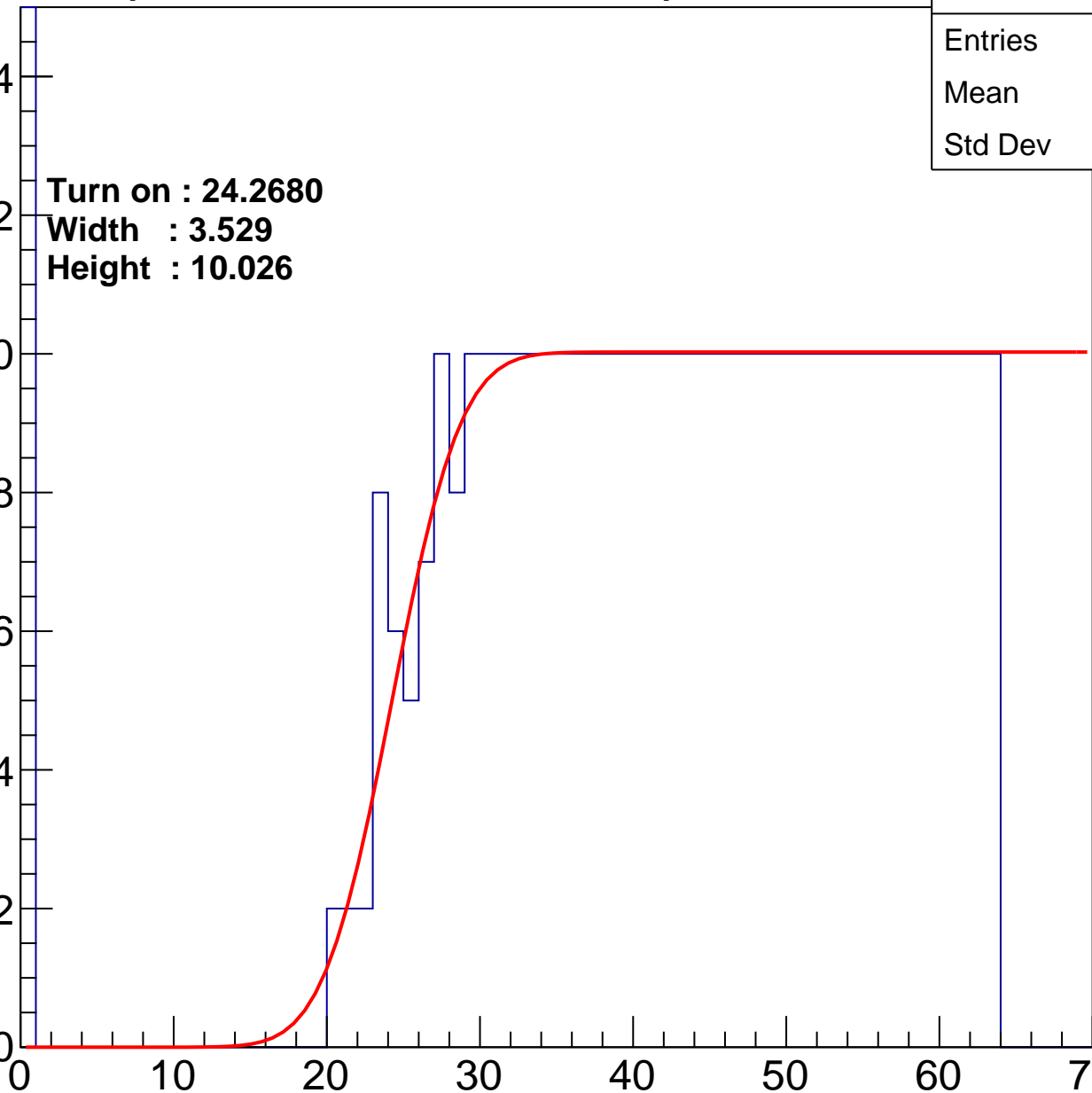
Width : 3.529

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch120

calib_packv5_041523_1651.root, FC#0, port C2

Entries	470
Mean	37.29
Std Dev	18.38

Turn on : 23.6774

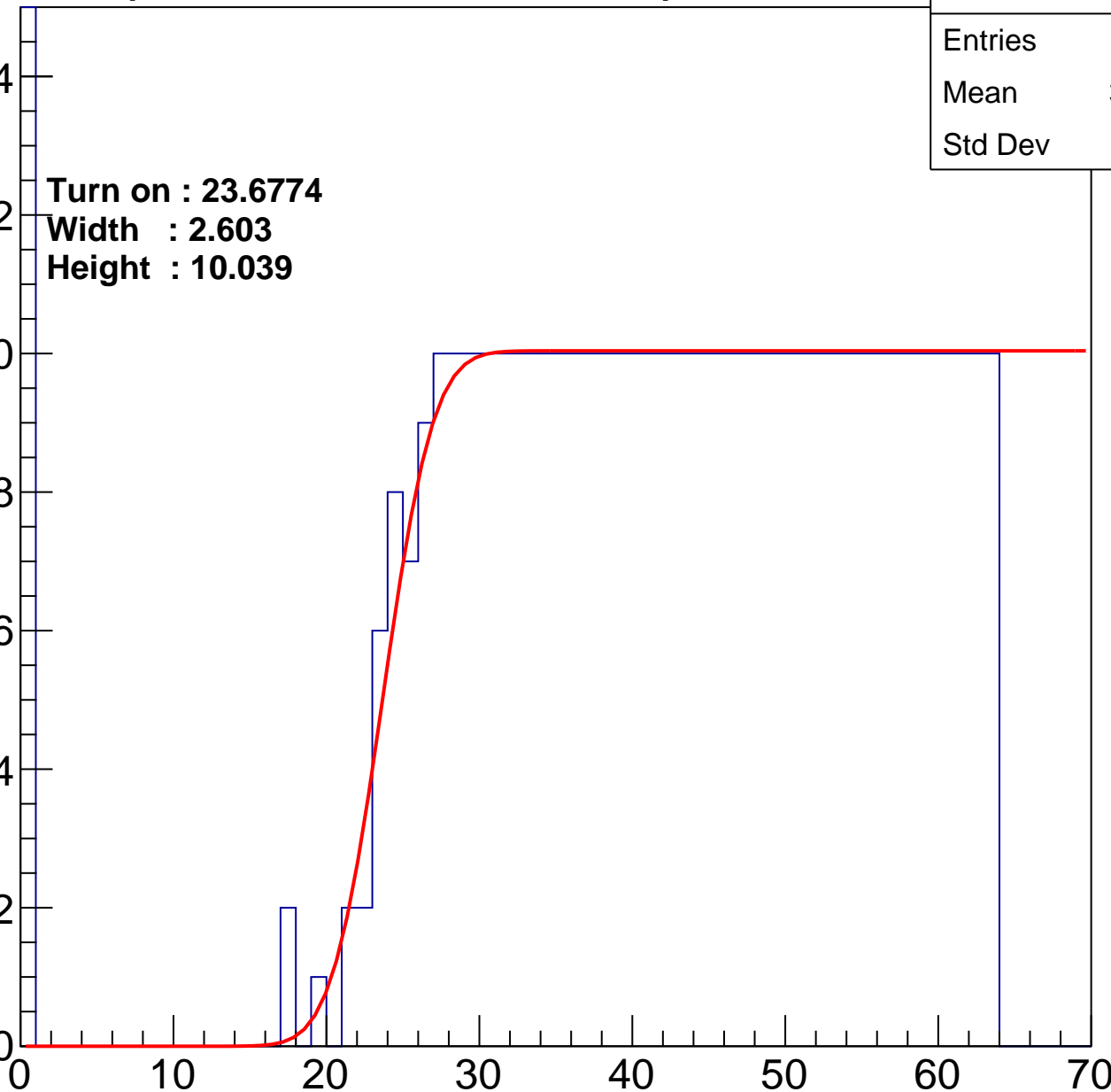
Width : 2.603

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch121

calib_packv5_041523_1651.root, FC#0, port C2

Entries	420
Mean	40.59
Std Dev	16.05

Turn on : 25.5150

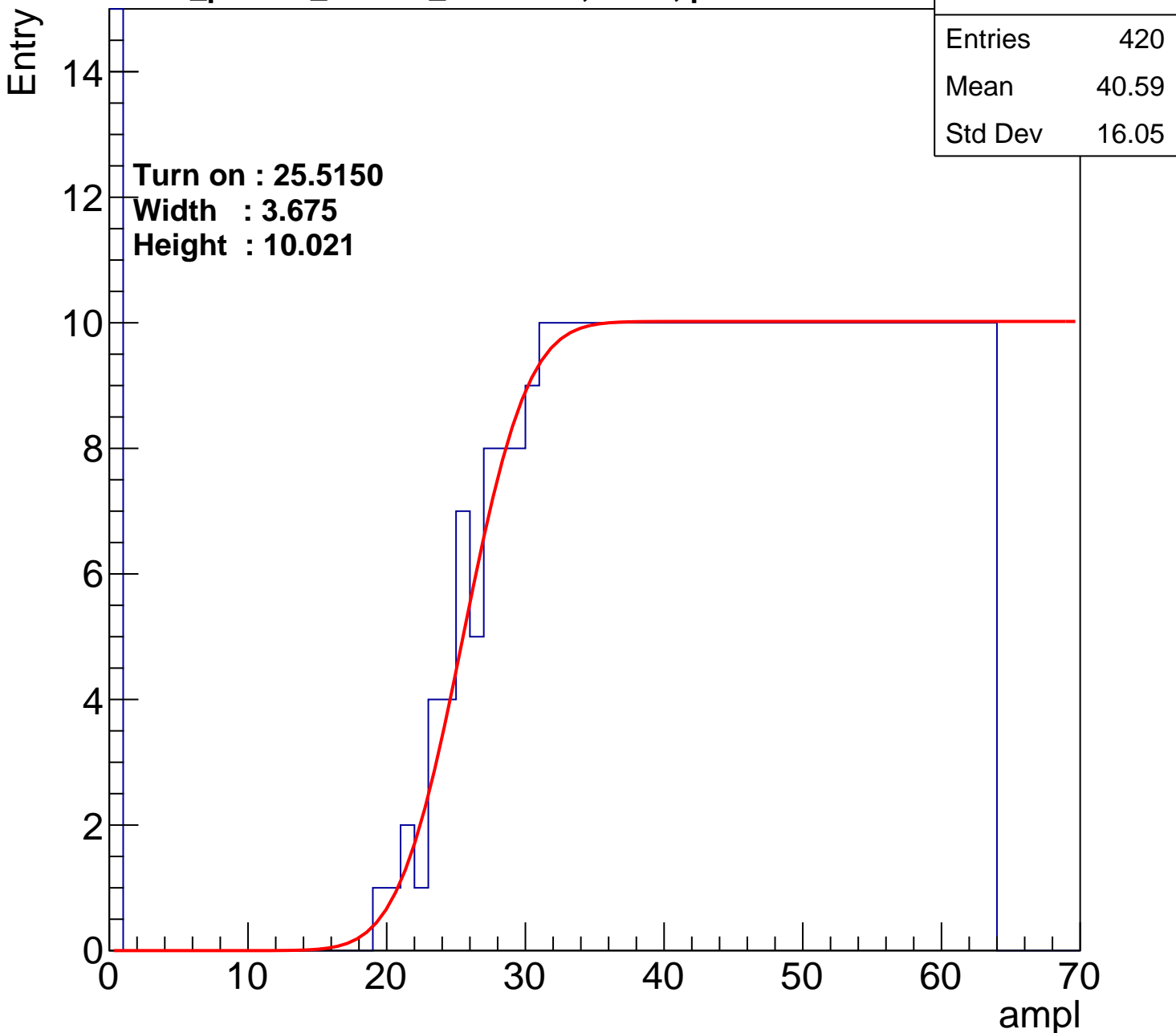
Width : 3.675

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch122

calib_packv5_041523_1651.root, FC#0, port C2

Entries	450
Mean	39.21
Std Dev	16.66

Turn on : 23.4294

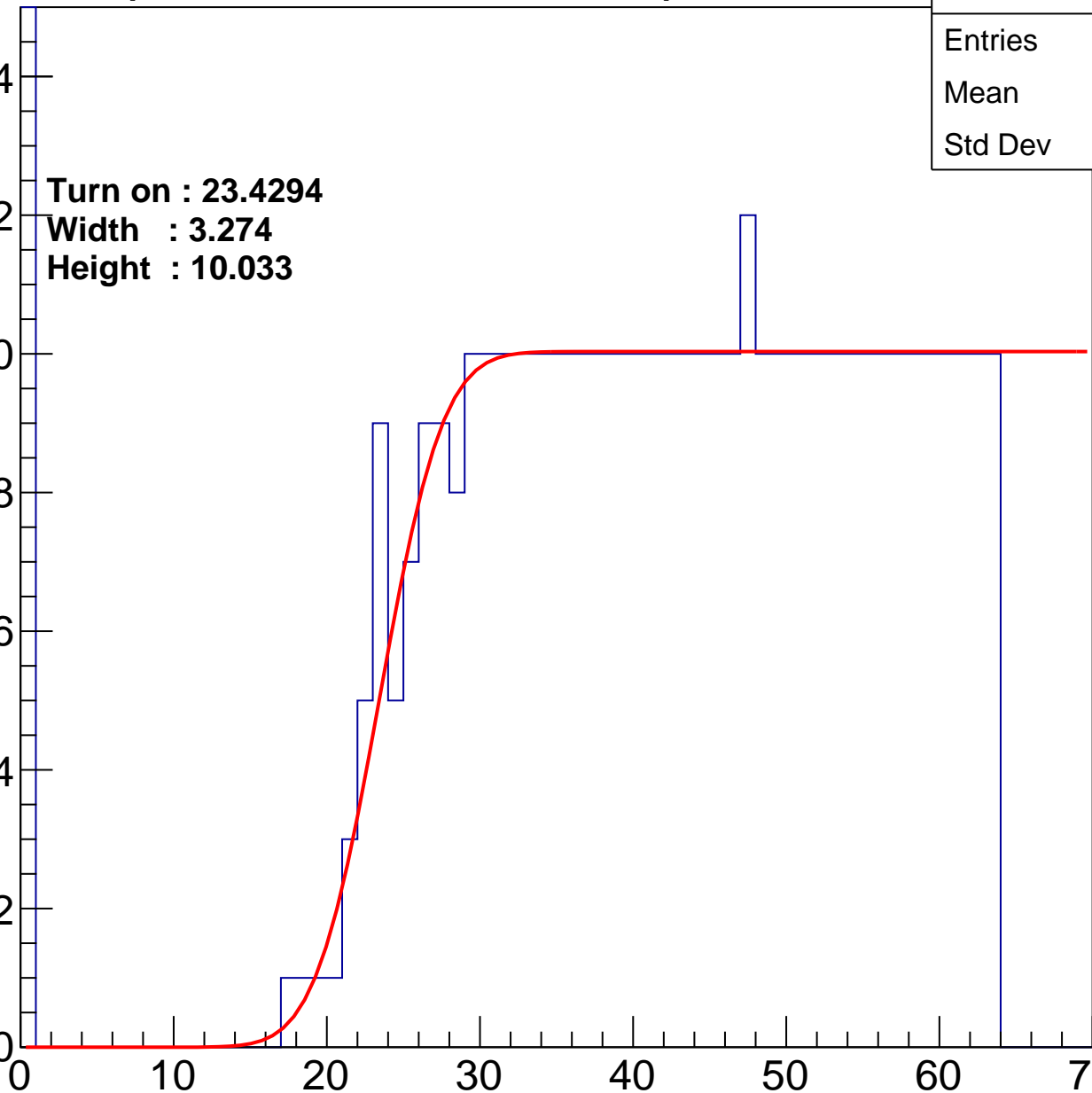
Width : 3.274

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch123

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	39.3
Std Dev	17.03

Turn on : 24.5939

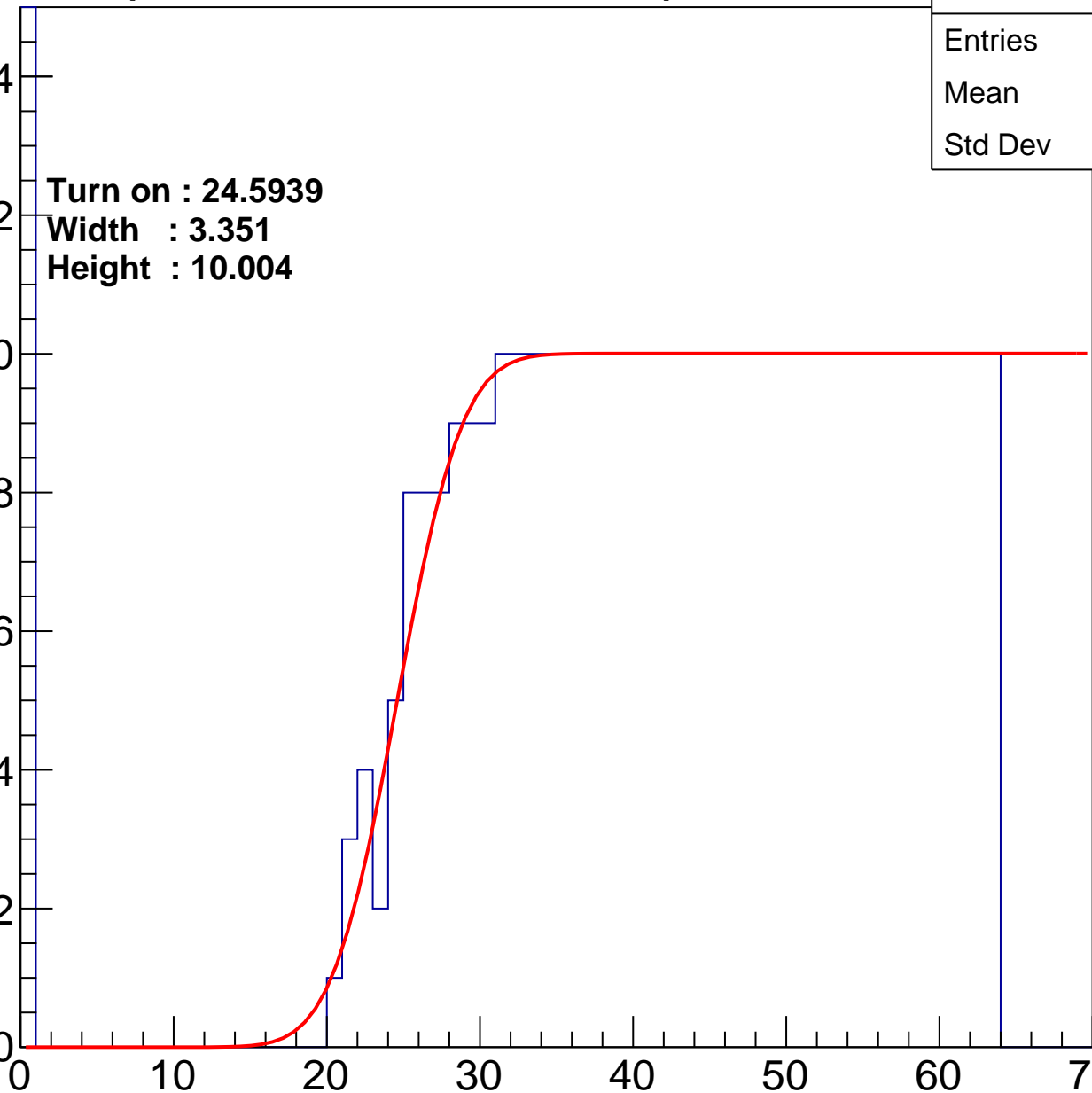
Width : 3.351

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch124

calib_packv5_041523_1651.root, FC#0, port C2

Entries	430
Mean	39.52
Std Dev	17.23

Turn on : 25.7190

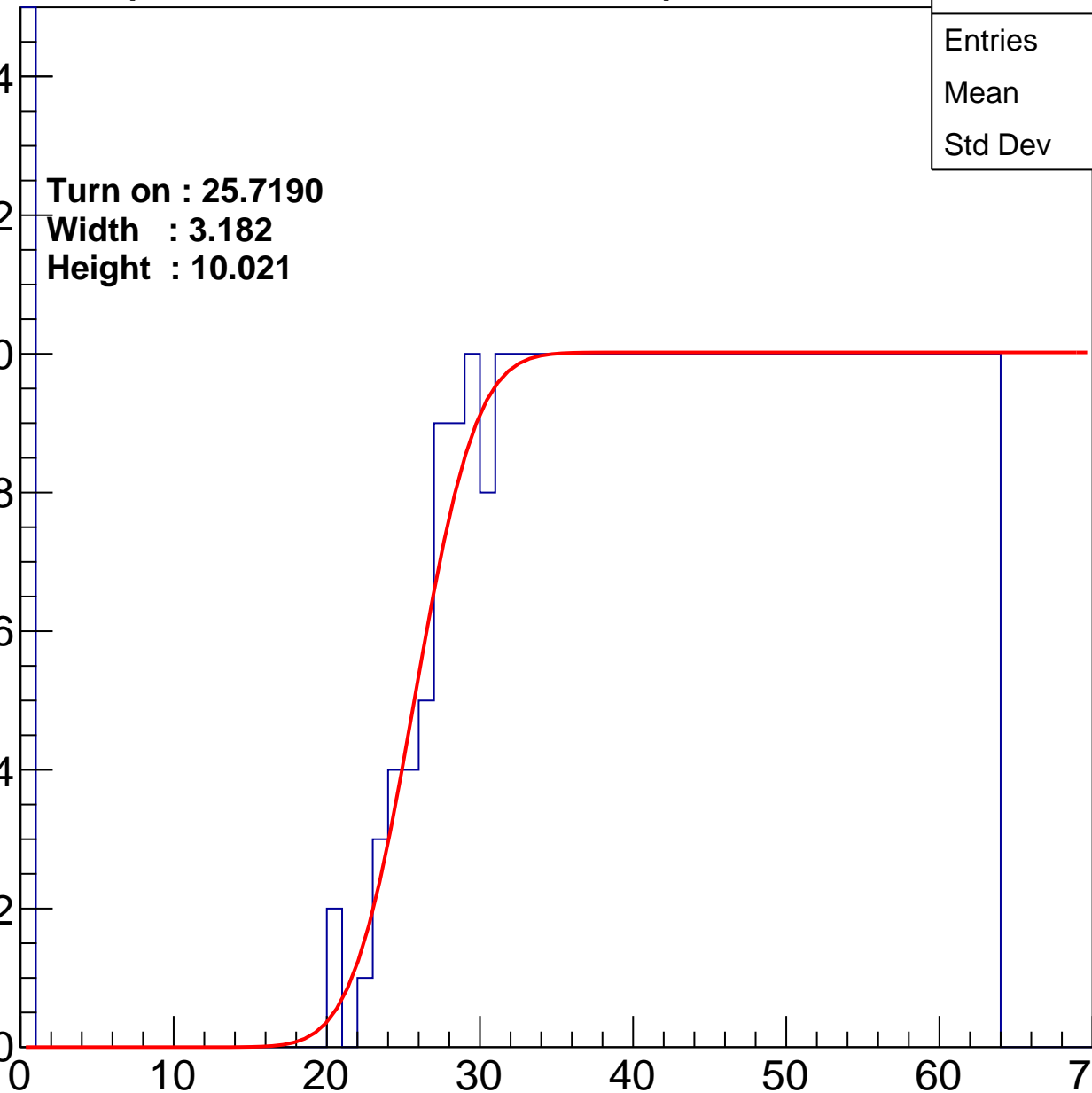
Width : 3.182

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch125

calib_packv5_041523_1651.root, FC#0, port C2

Entries	439
Mean	38.93
Std Dev	17.62

Turn on : 25.5309

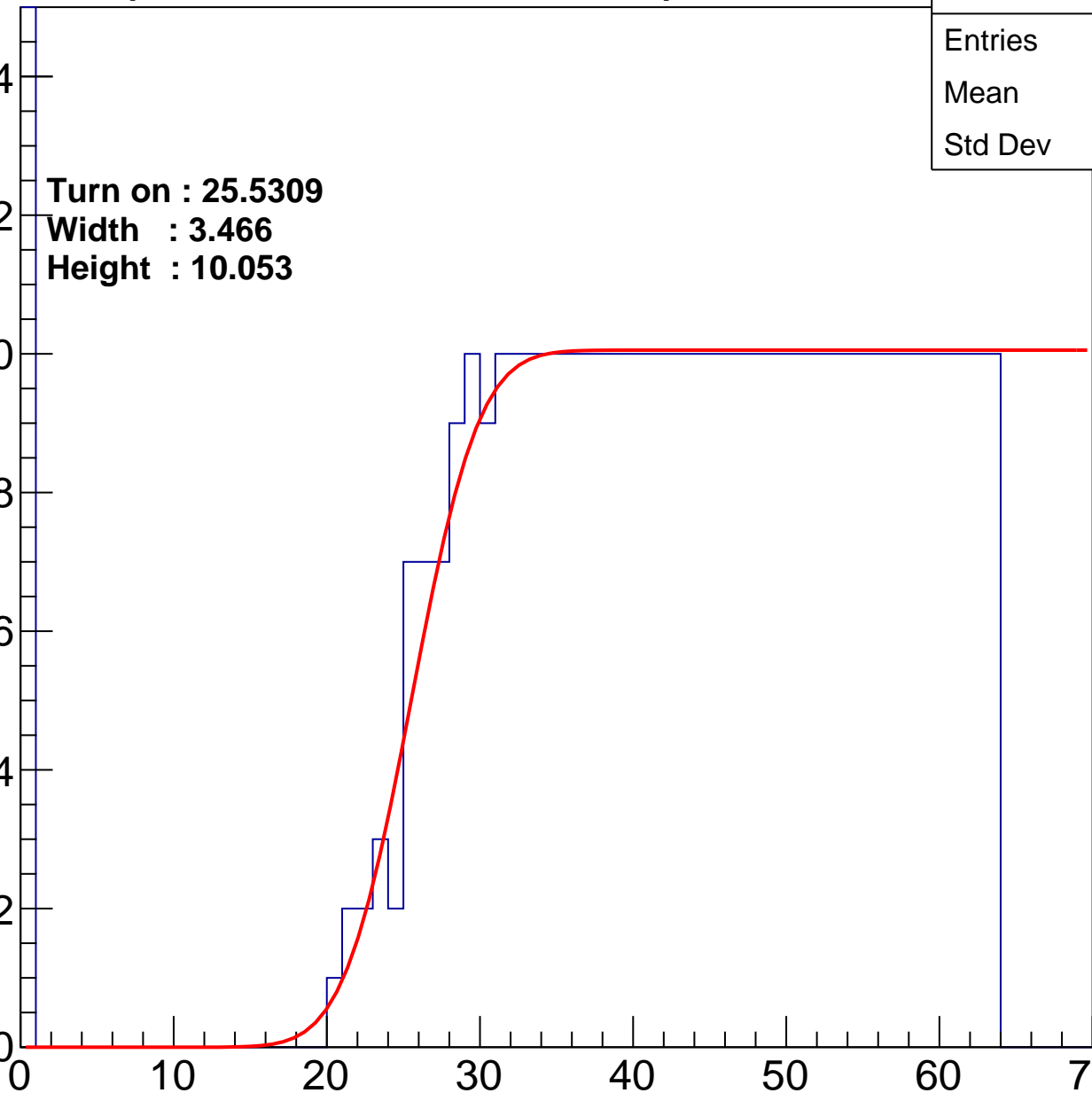
Width : 3.466

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch126

calib_packv5_041523_1651.root, FC#0, port C2

Entries	481
Mean	37.37
Std Dev	17.68

Turn on : 21.1904

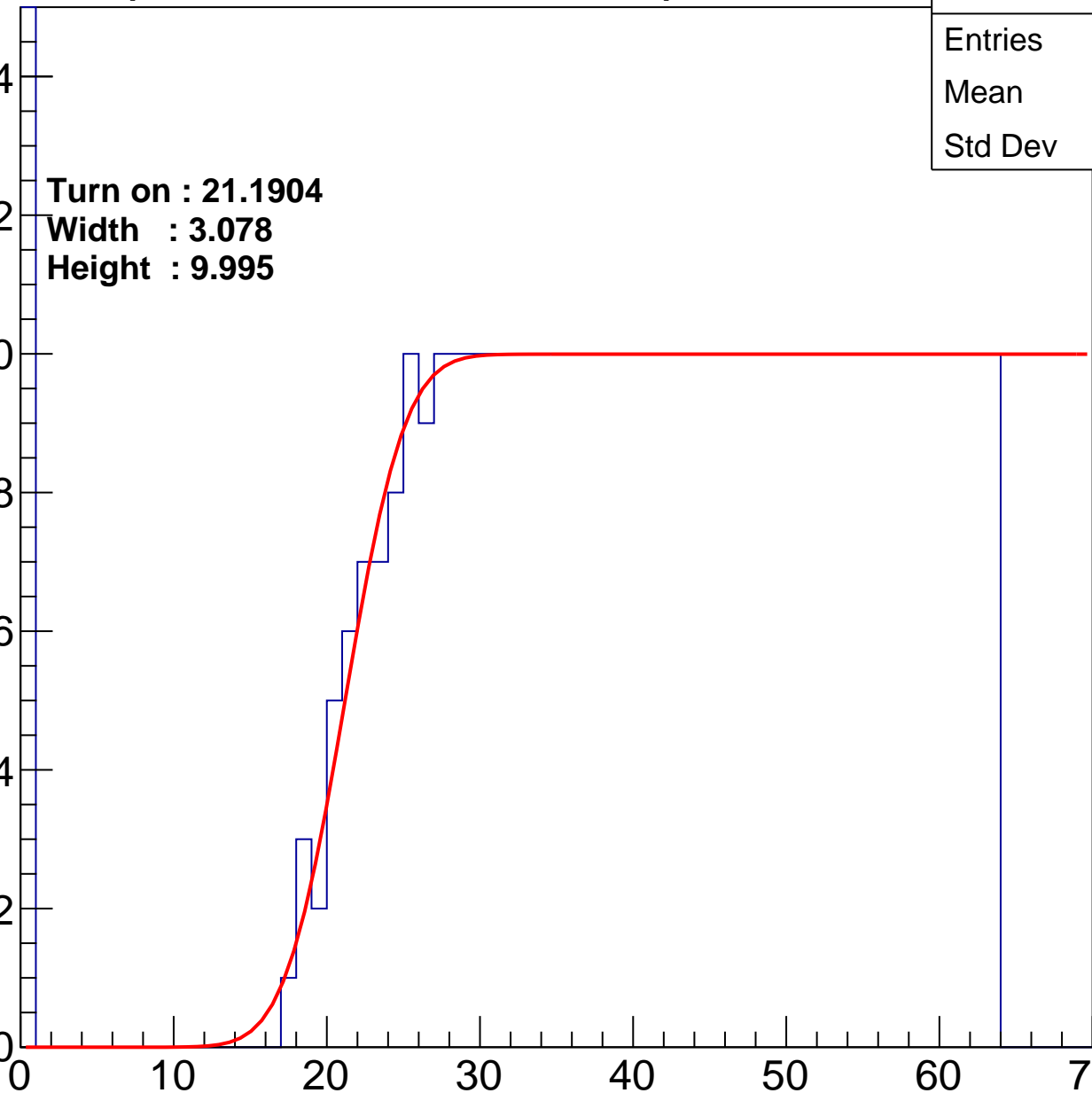
Width : 3.078

Height : 9.995

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U24-ch127

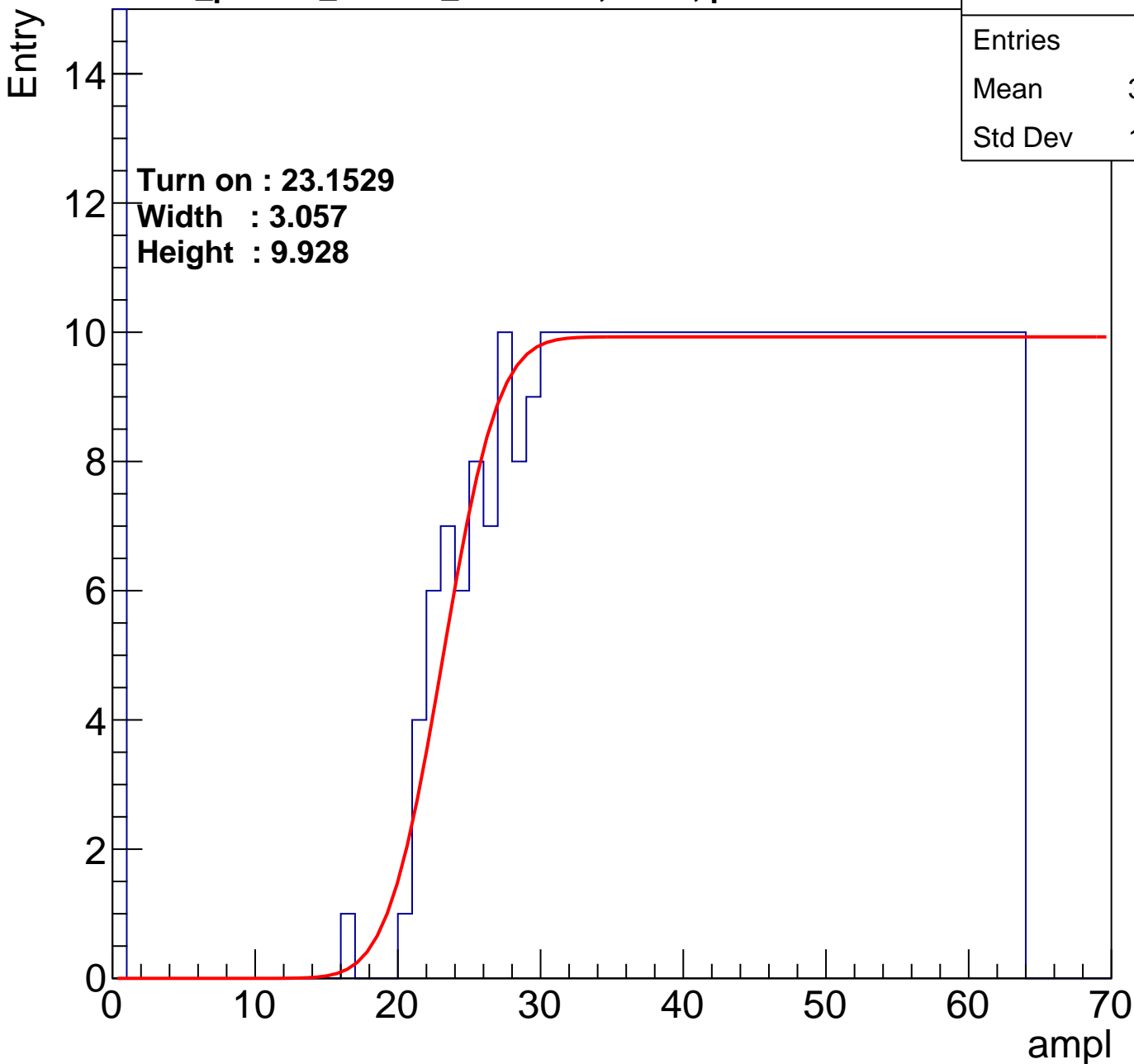
calib_packv5_041523_1651.root, FC#0, port C2

Entries	456
Mean	38.39
Std Dev	17.48

Turn on : 23.1529

Width : 3.057

Height : 9.928



B1L103S, U24-ch127

calib_packv5_041523_1651.root, FC#0, port C2

Entries	456
Mean	38.39
Std Dev	17.48

Turn on : 23.1529

Width : 3.057

Height : 9.928

Entry

14
12
10
8
6
4
2
0

ampl

