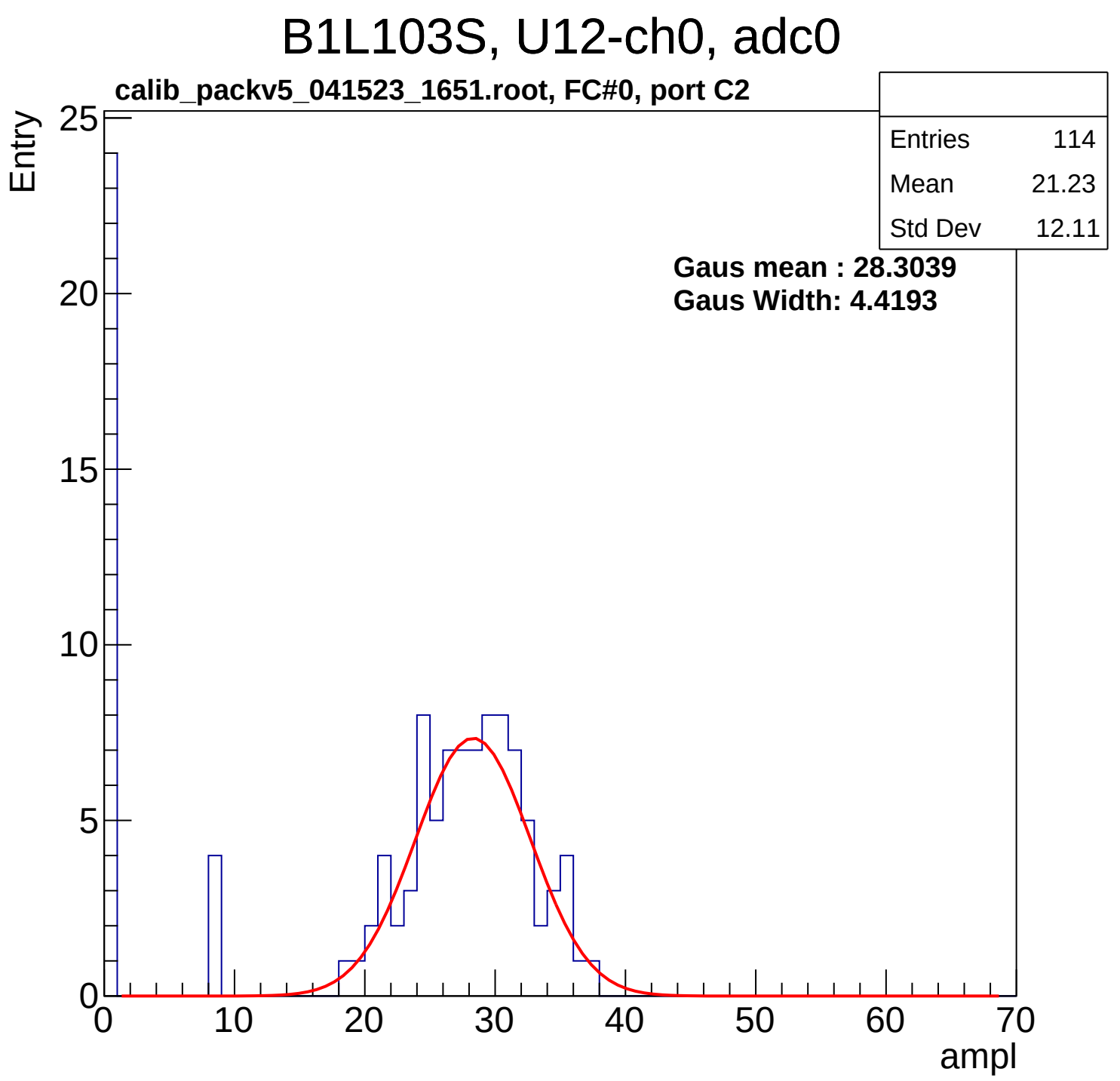
B1L103S, U12-ch0, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 114
Mean 21.23
Std Dev 12.11
Gaus mean : 28.3039
Gaus Width: 4.4193
Entry
ampl
0
5
10
15
20
25
0
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40
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60
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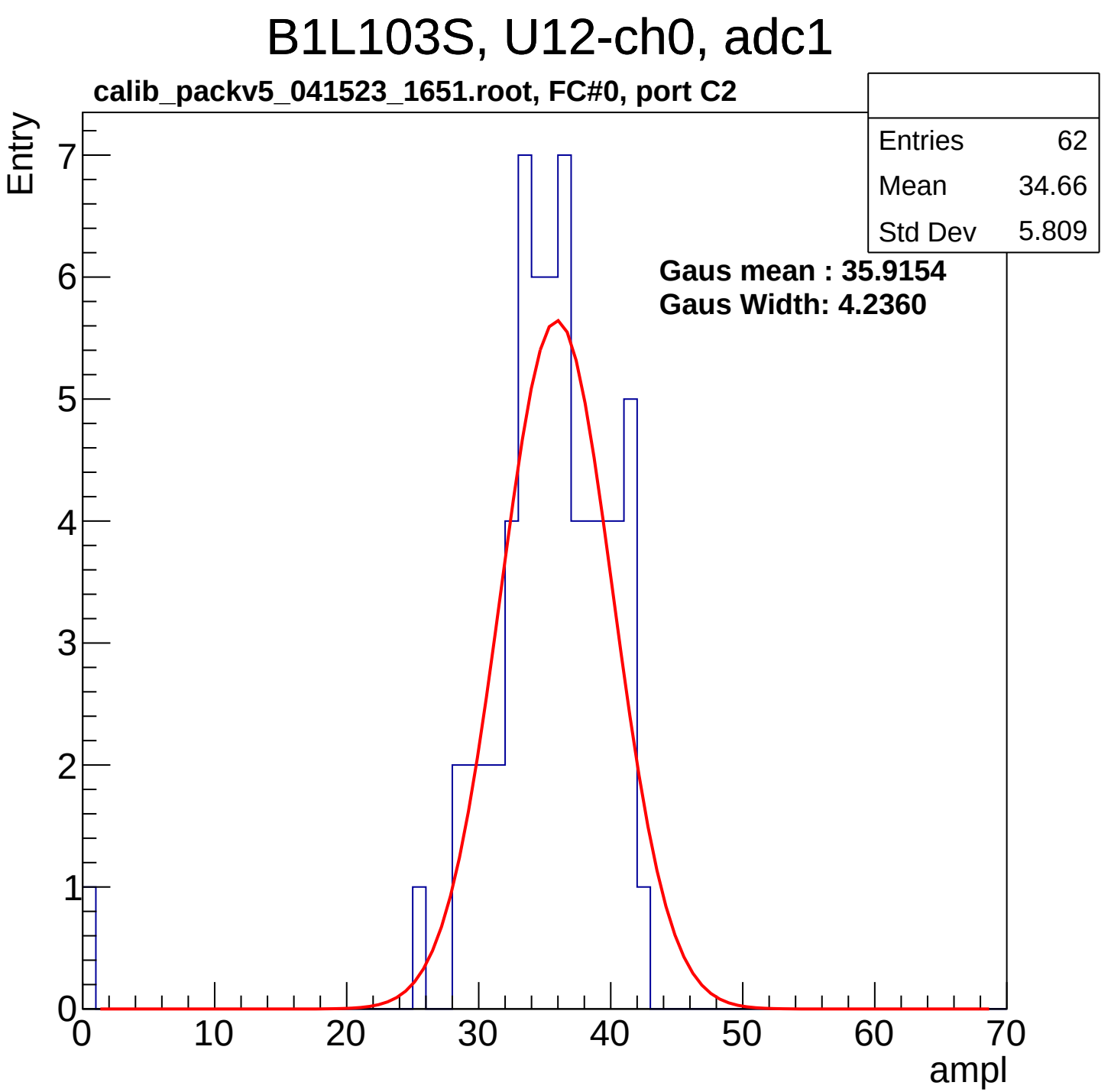
B1L103S, U12-ch0, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 34.66
Std Dev 5.809
Gaus mean : 35.9154
Gaus Width: 4.2360
Entry
ampl
0
1
2
3
4
5
6
7
0
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40
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60
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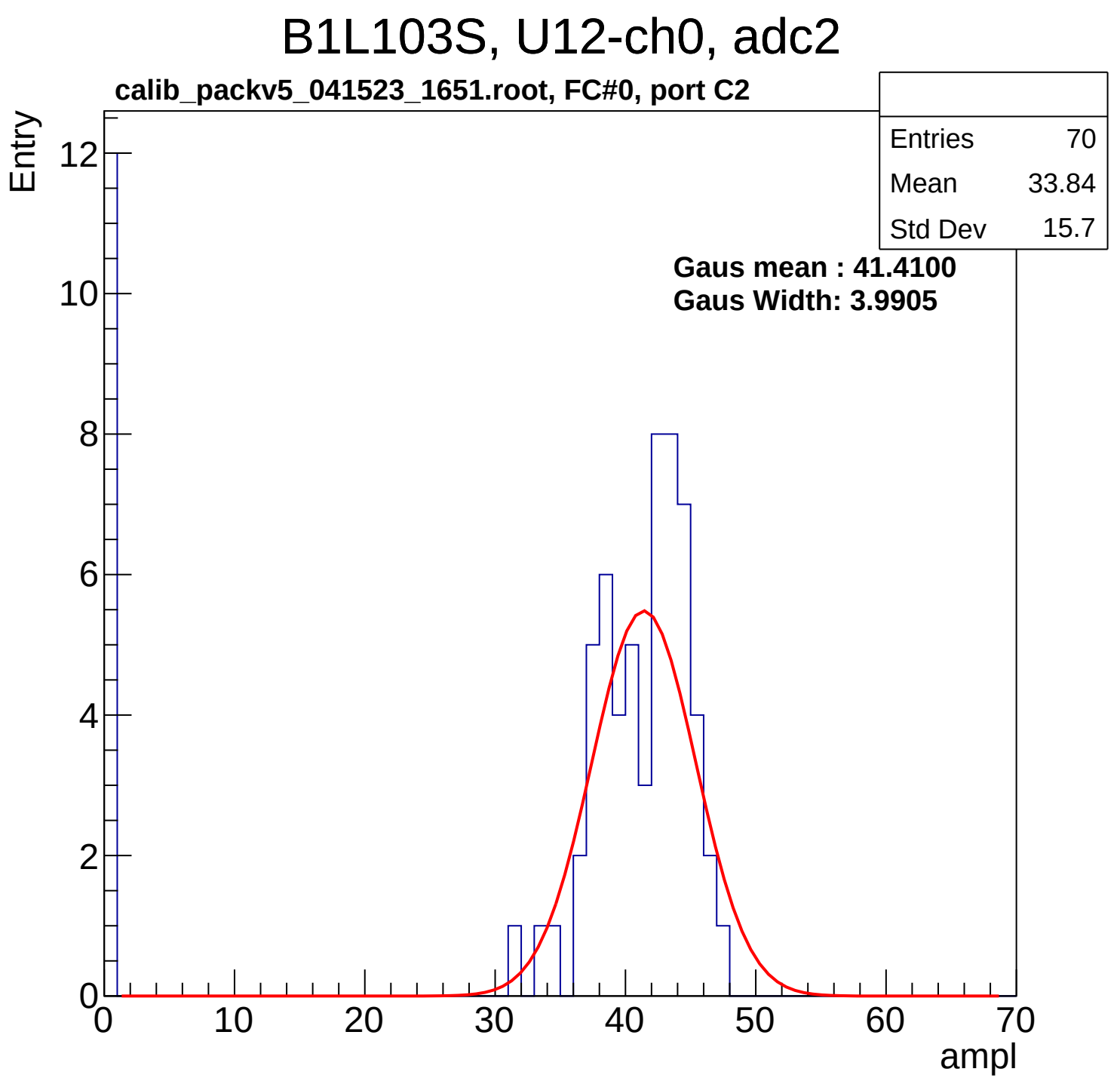
B1L103S, U12-ch0, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 33.84
Std Dev 15.7
Gaus mean : 41.4100
Gaus Width: 3.9905
Entry
ampl
0
2
4
6
8
10
12
0
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40
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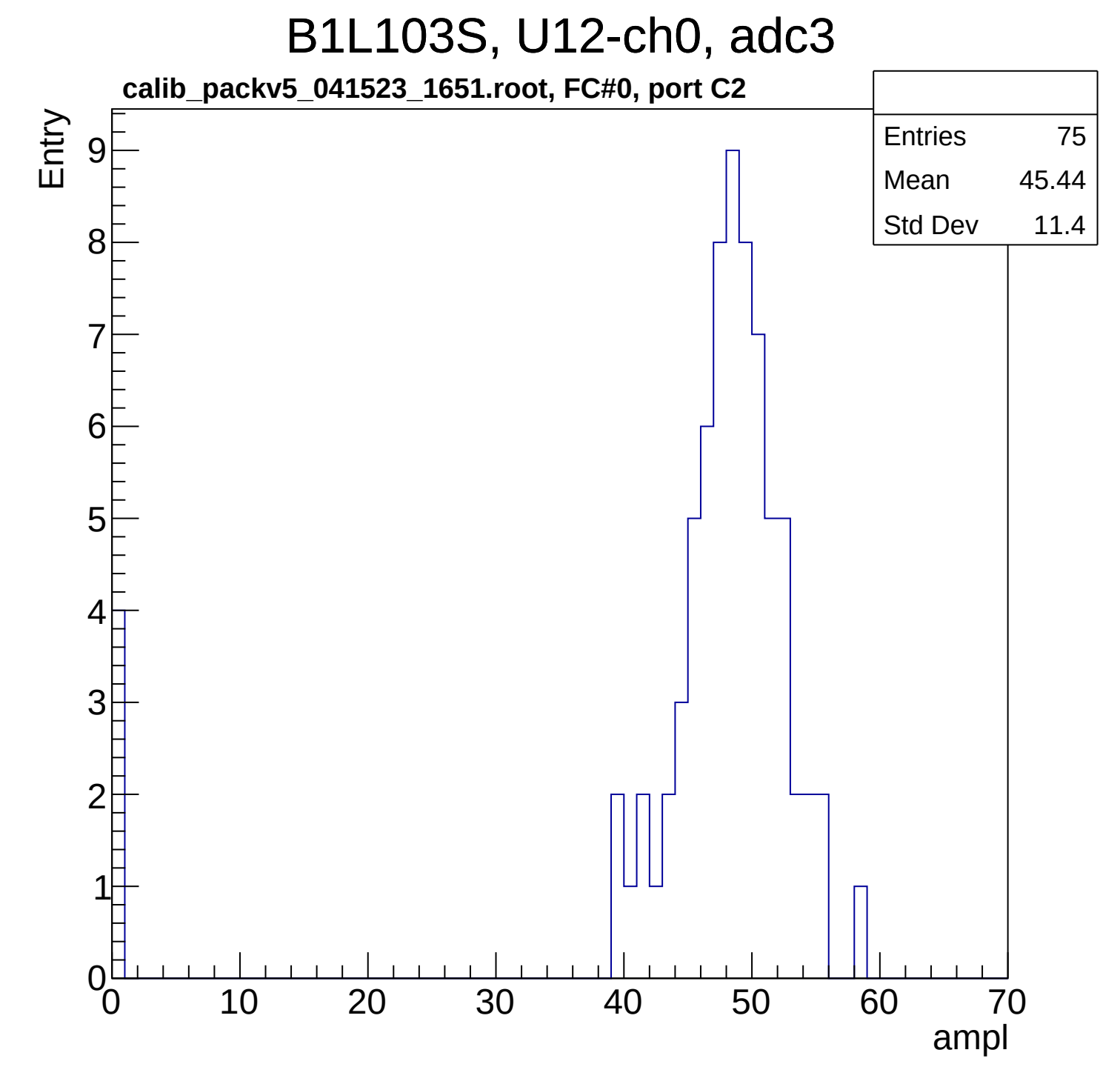
B1L103S, U12-ch0, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 45.44
Std Dev 11.4
Entry
ampl
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2
3
4
5
6
7
8
9
0
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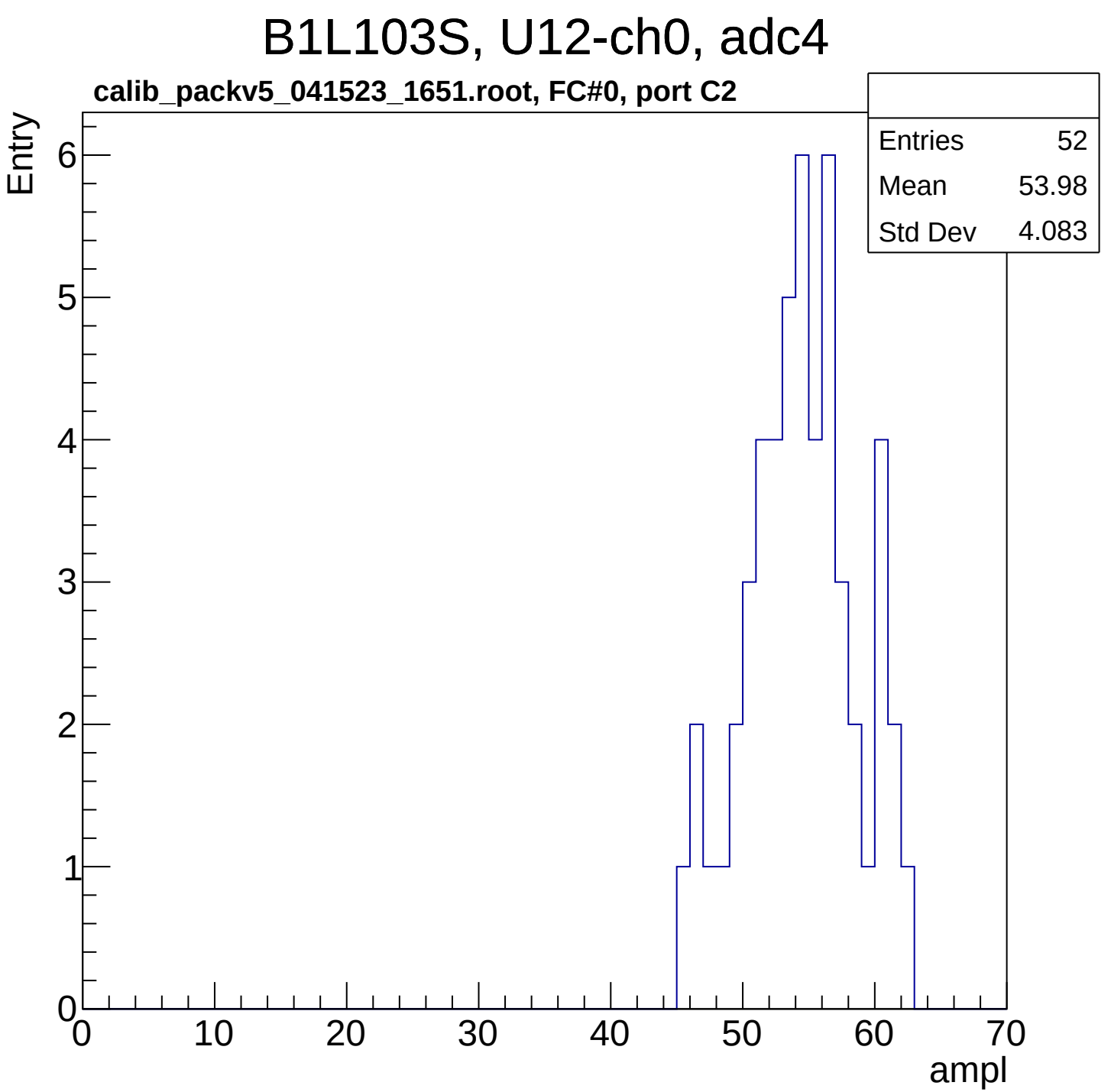
B1L103S, U12-ch0, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 53.98
Std Dev 4.083
Entry
ampl
0
1
2
3
4
5
6
0
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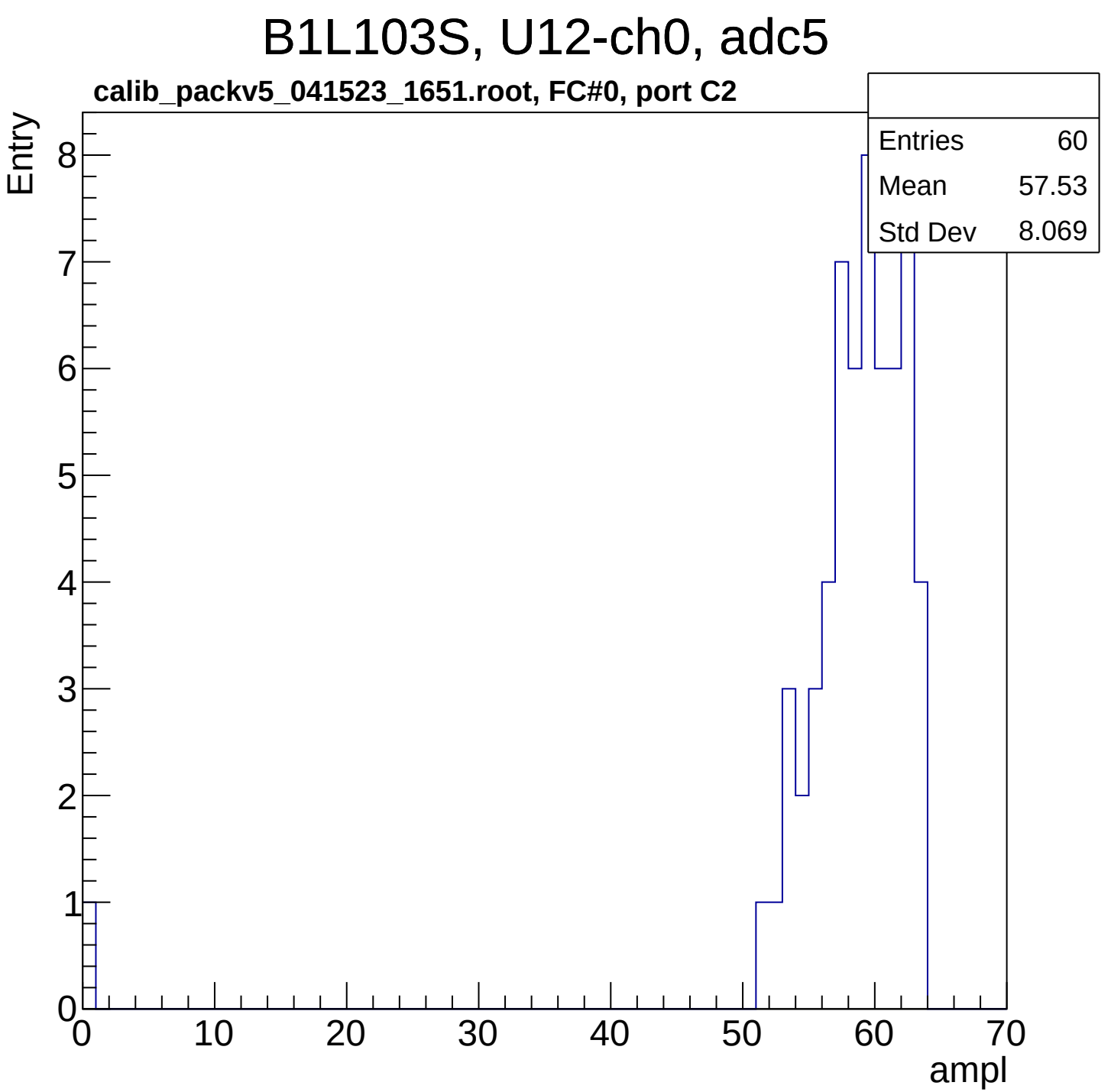
B1L103S, U12-ch0, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 57.53
Std Dev 8.069
Entry
ampl
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2
3
4
5
6
7
8
0
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60
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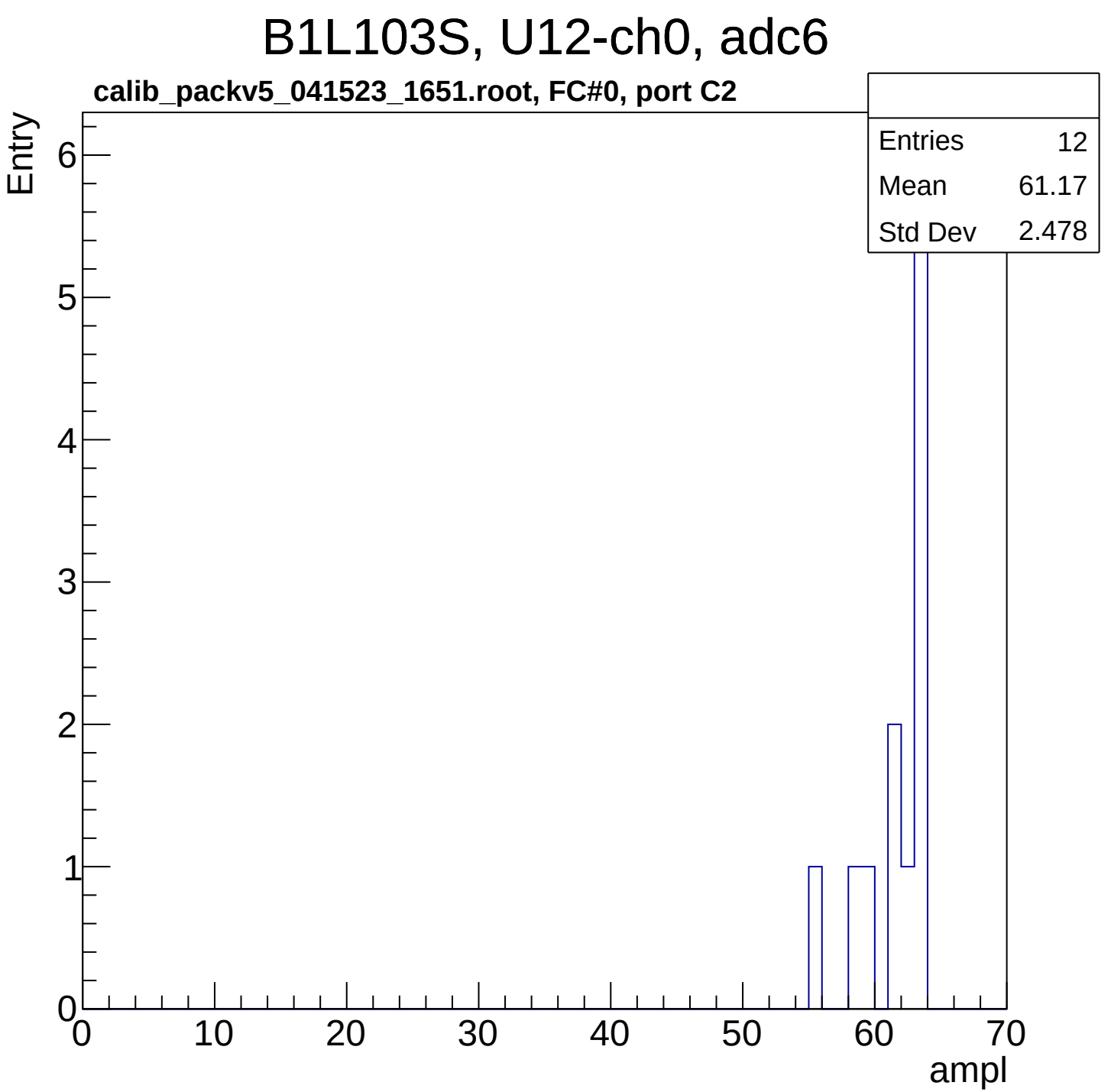
B1L103S, U12-ch0, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.17
Std Dev 2.478
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
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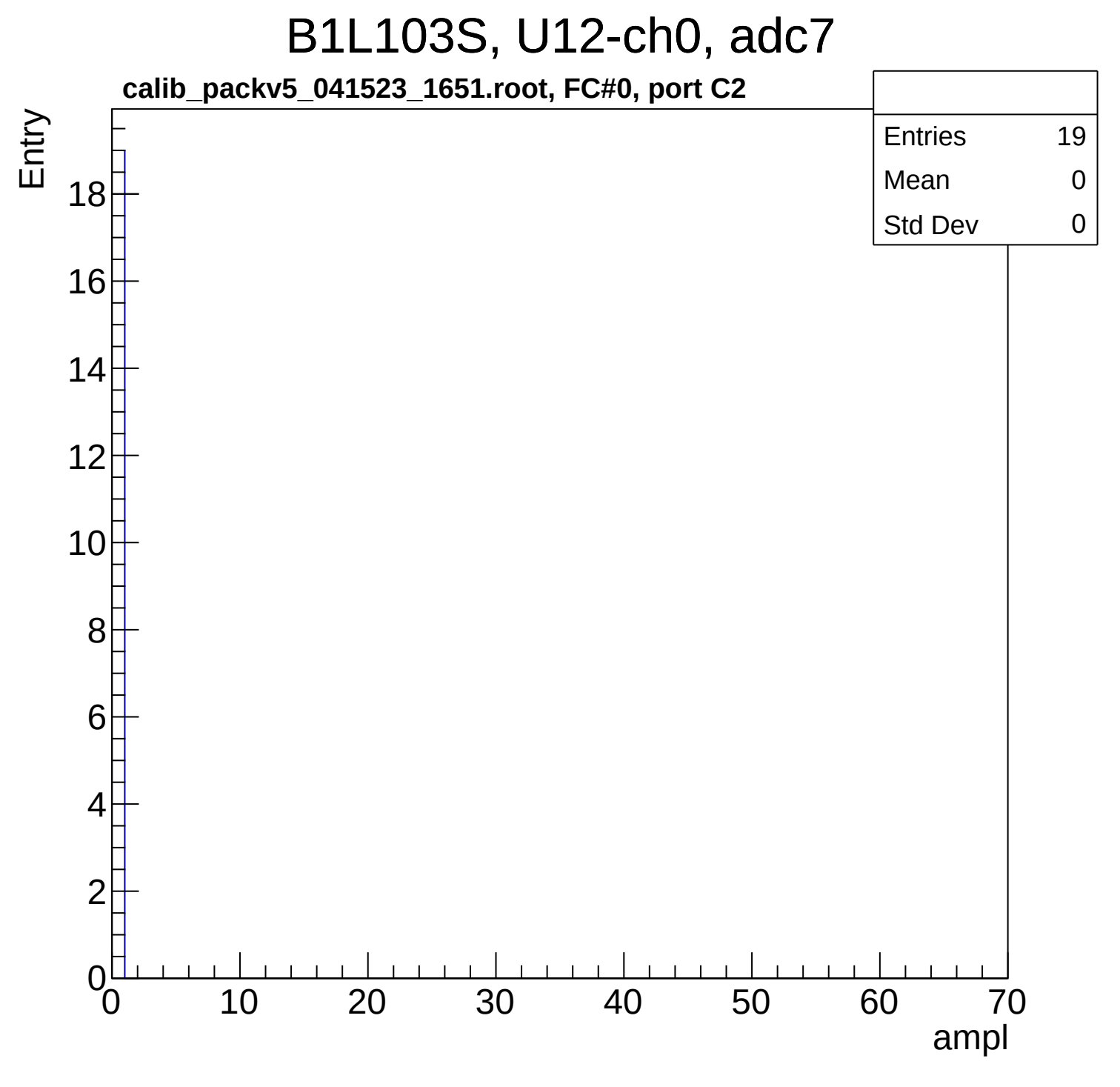
B1L103S, U12-ch0, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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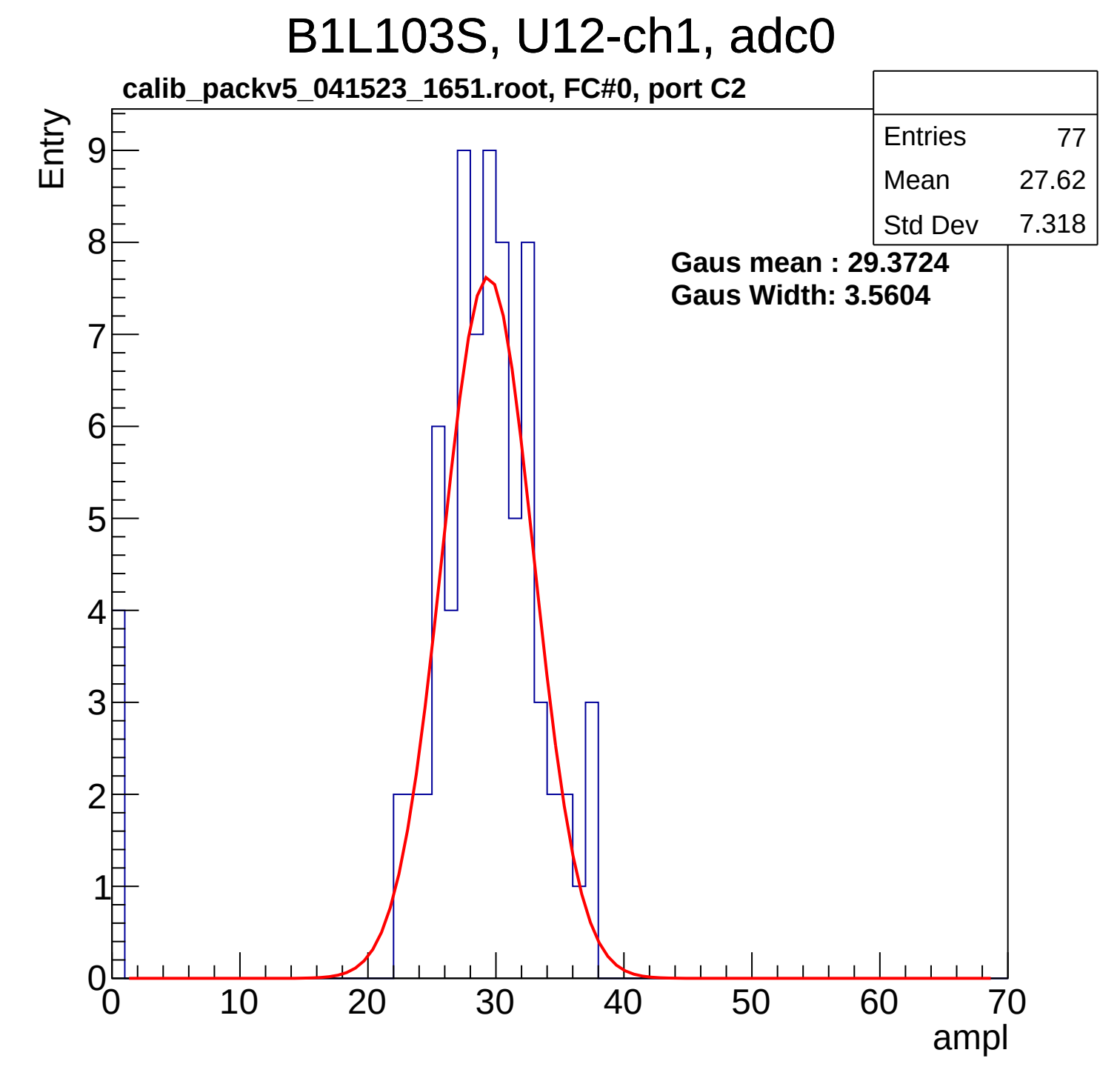
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch1, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 27.62
Std Dev 7.318
Gaus mean : 29.3724
Gaus Width: 3.5604
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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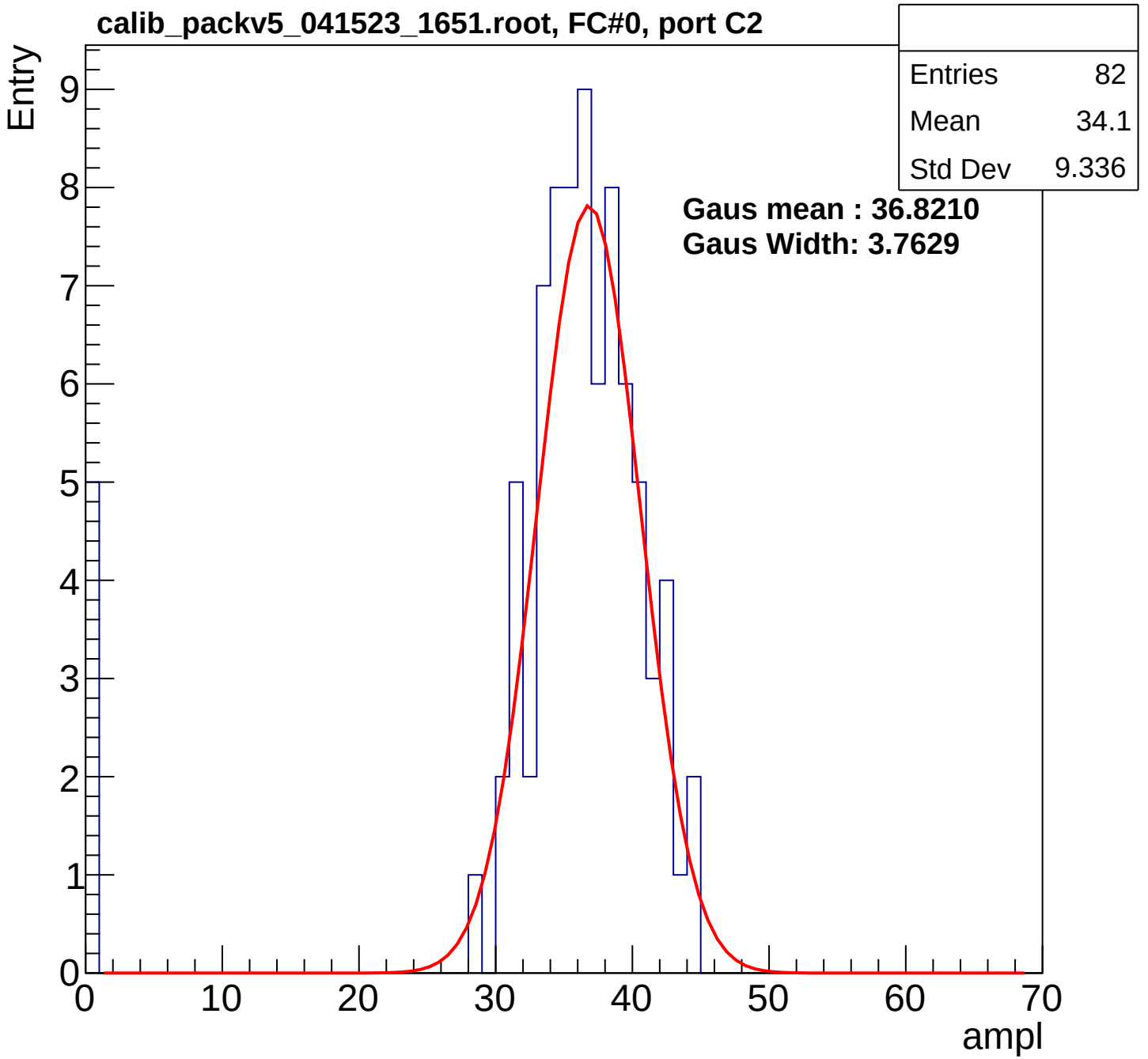
B1L103S, U12-ch1, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 34.1
Std Dev 9.336
Gaus mean : 36.8210
Gaus Width: 3.7629
Entry
ampl
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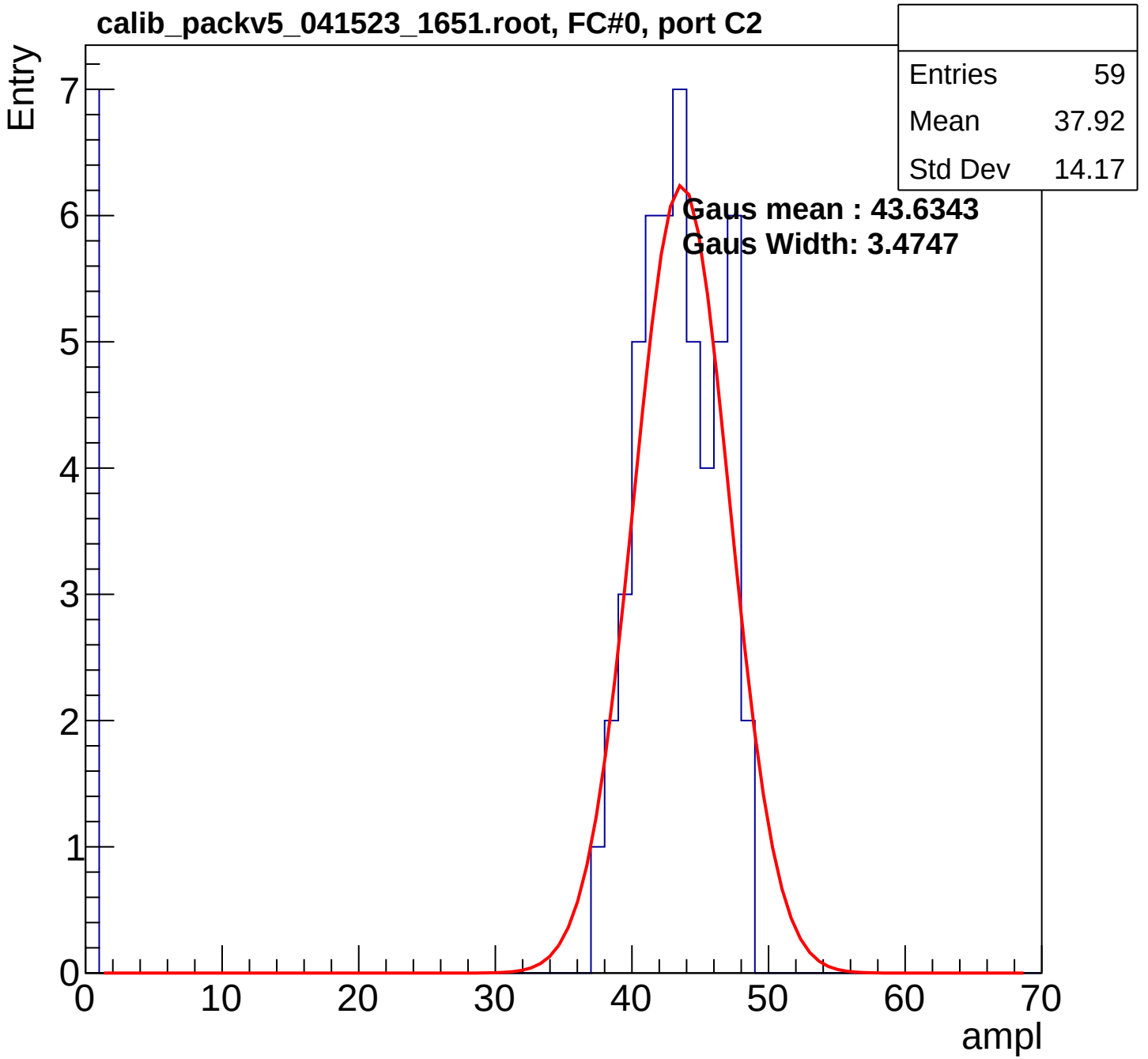
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U12-ch1, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 37.92
Std Dev 14.17
Gaus mean : 43.6343
Gaus Width: 3.4747
Entry
ampl
0
1
2
3
4
5
6
7
0
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60
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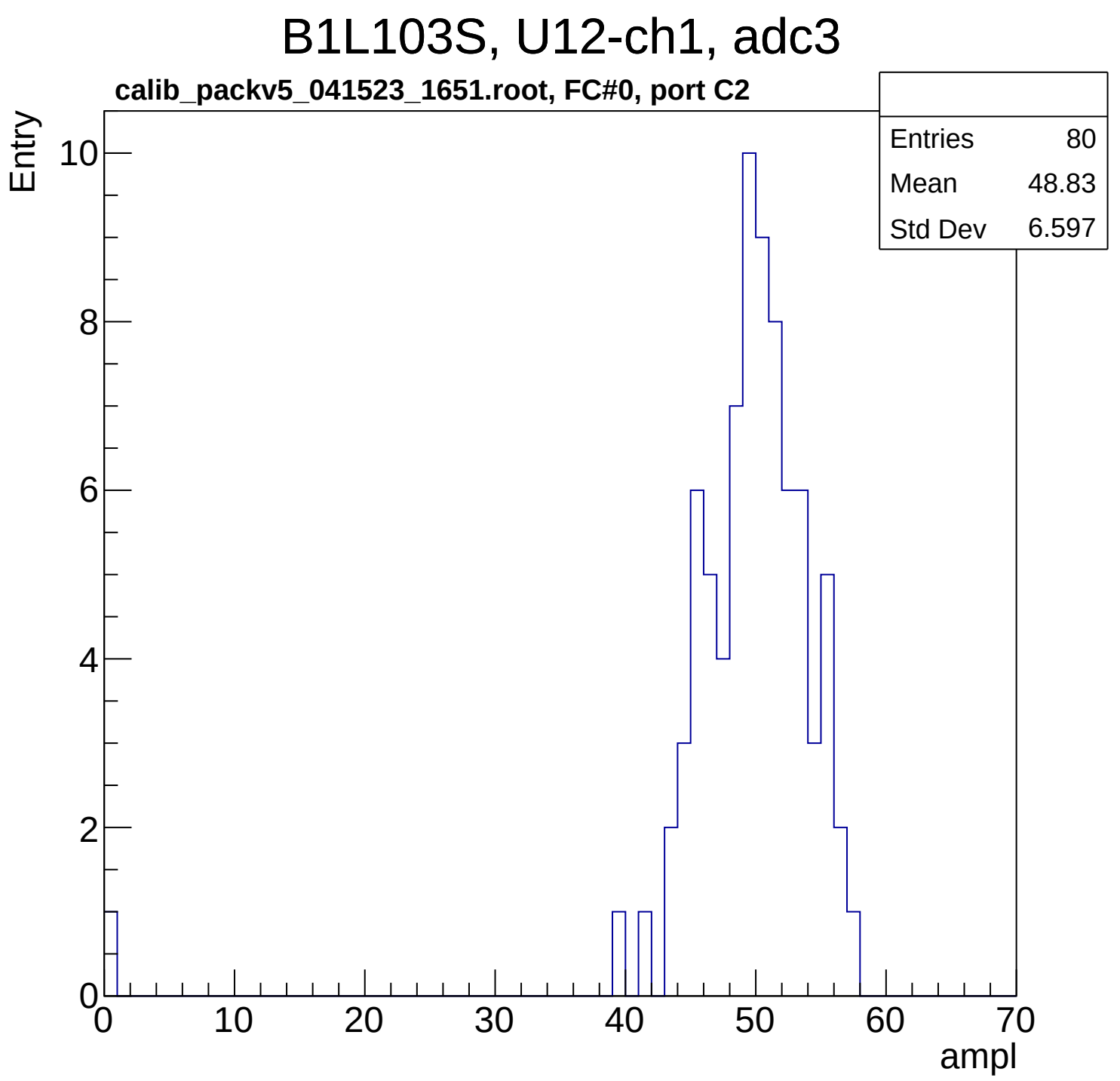
B1L103S, U12-ch1, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 48.83
Std Dev 6.597
Entry
ampl
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2
4
6
8
10
0
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20
30
40
50
60
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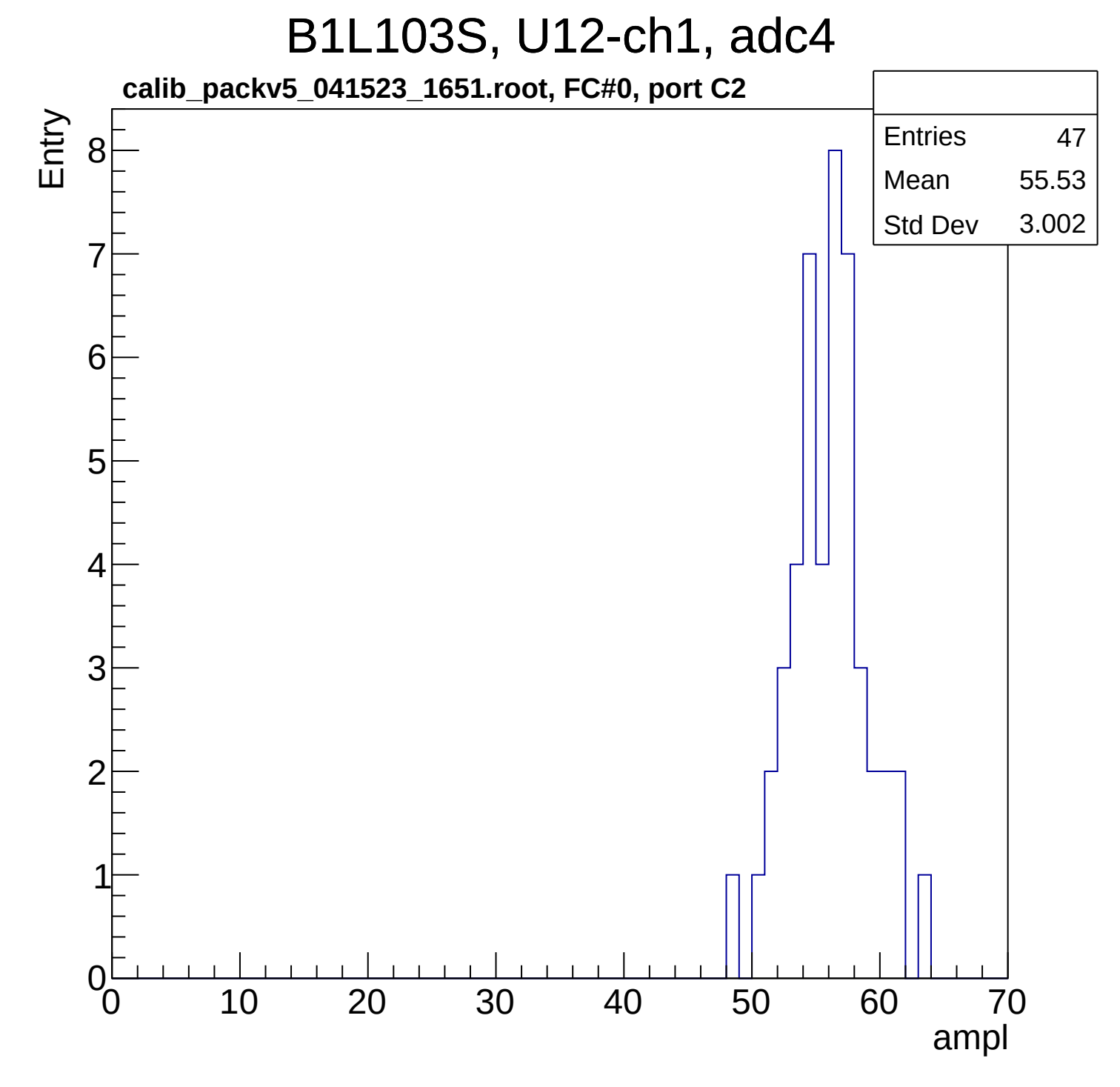
B1L103S, U12-ch1, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 55.53
Std Dev 3.002
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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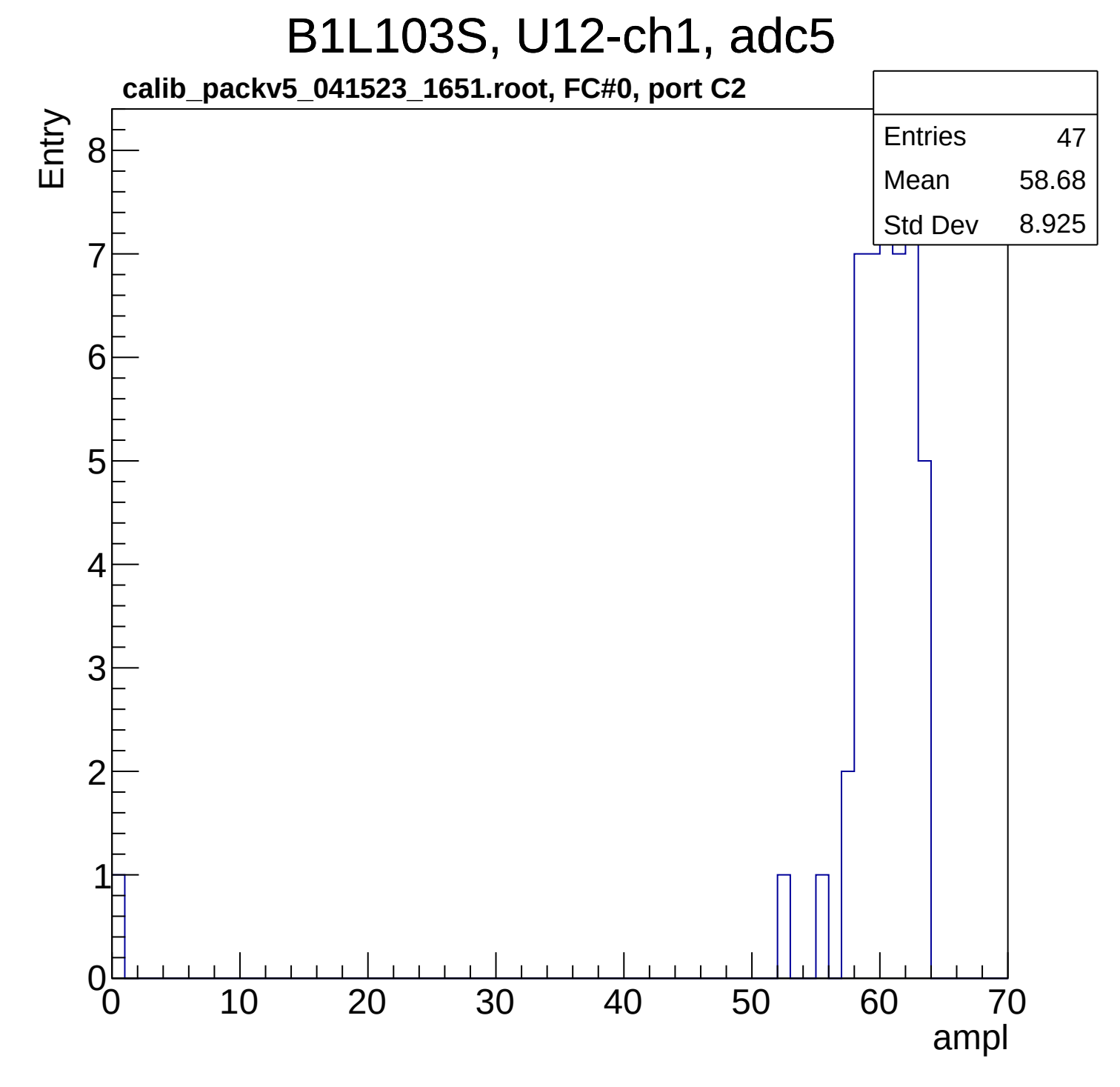
B1L103S, U12-ch1, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.68
Std Dev 8.925
Entry
ampl
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3
4
5
6
7
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0
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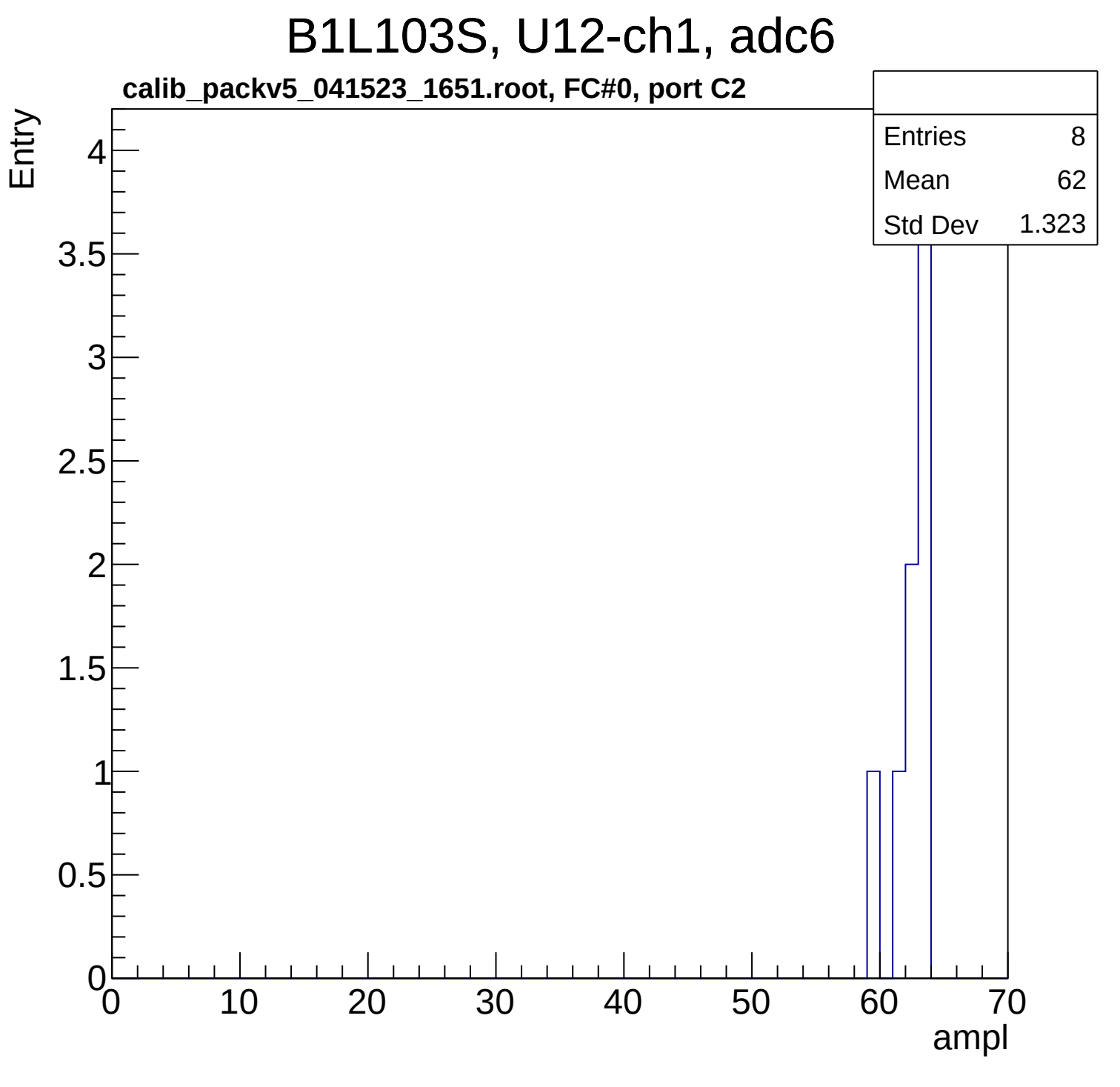
B1L103S, U12-ch1, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62
Std Dev 1.323
Entry
ampl
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1.5
2
2.5
3
3.5
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0
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40
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60
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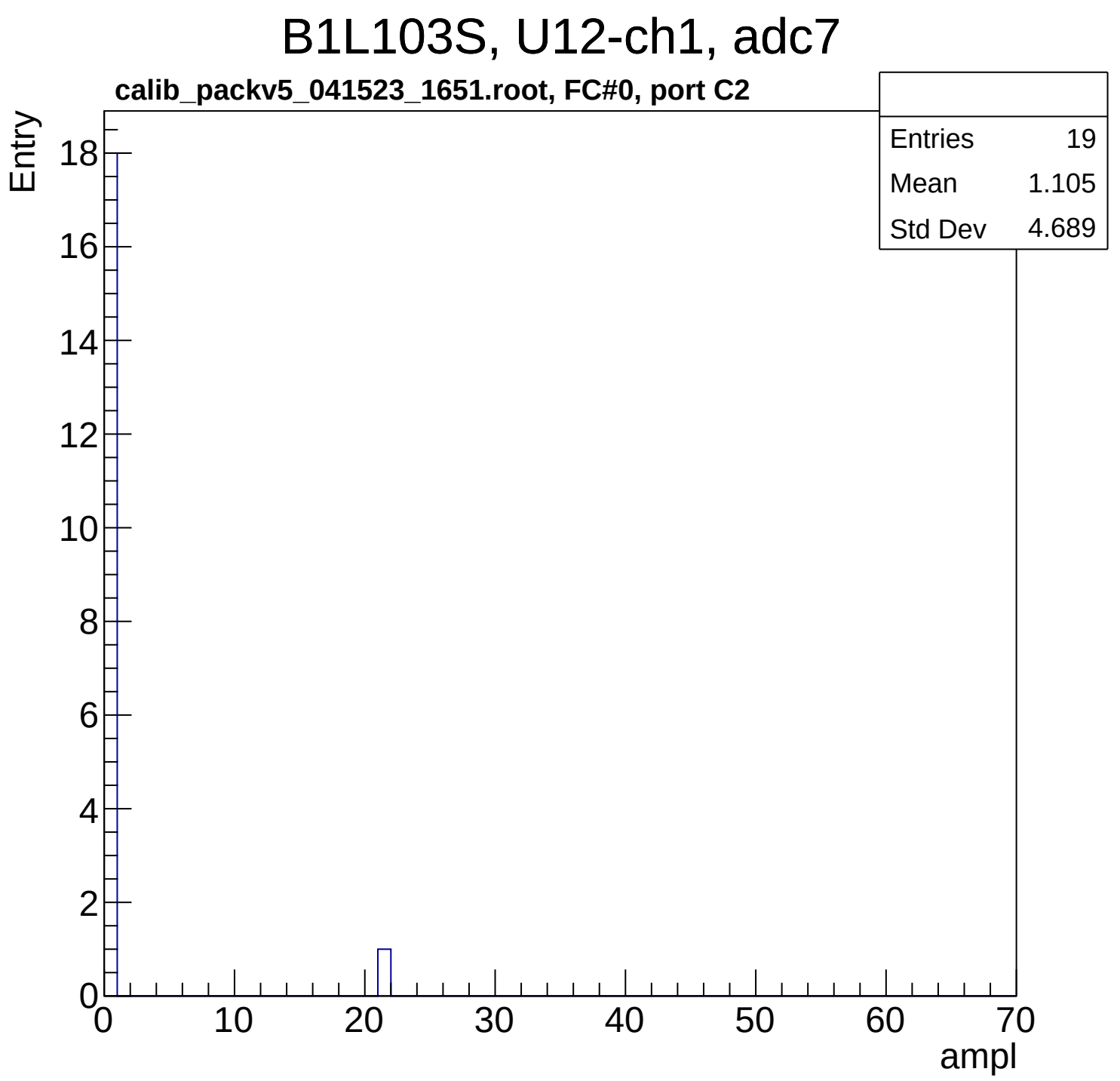
B1L103S, U12-ch1, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
ampl
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6
8
10
12
14
16
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0
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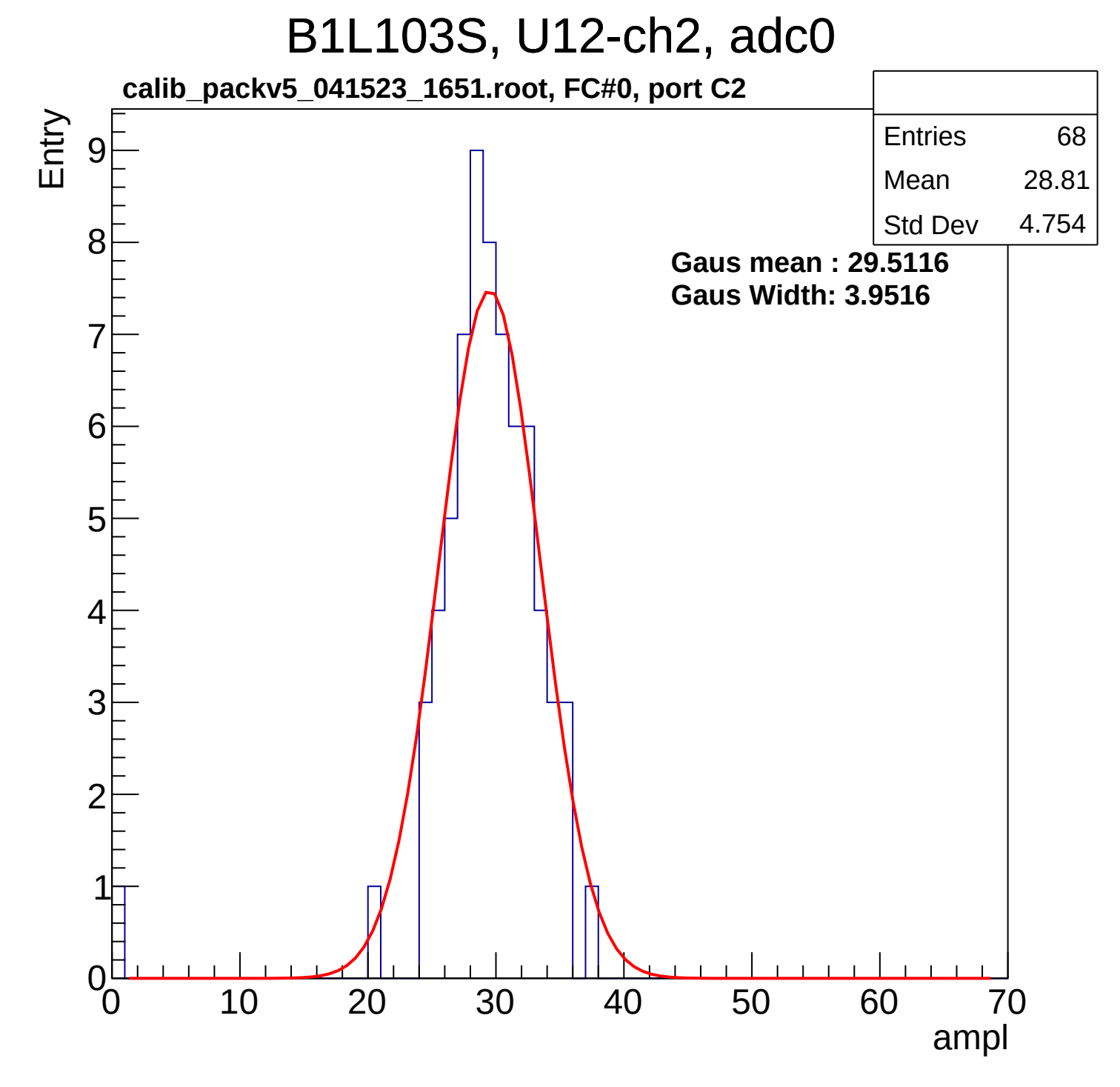
B1L103S, U12-ch2, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 28.81
Std Dev 4.754
Gaus mean : 29.5116
Gaus Width: 3.9516
Entry
ampl
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3
4
5
6
7
8
9
0
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20
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60
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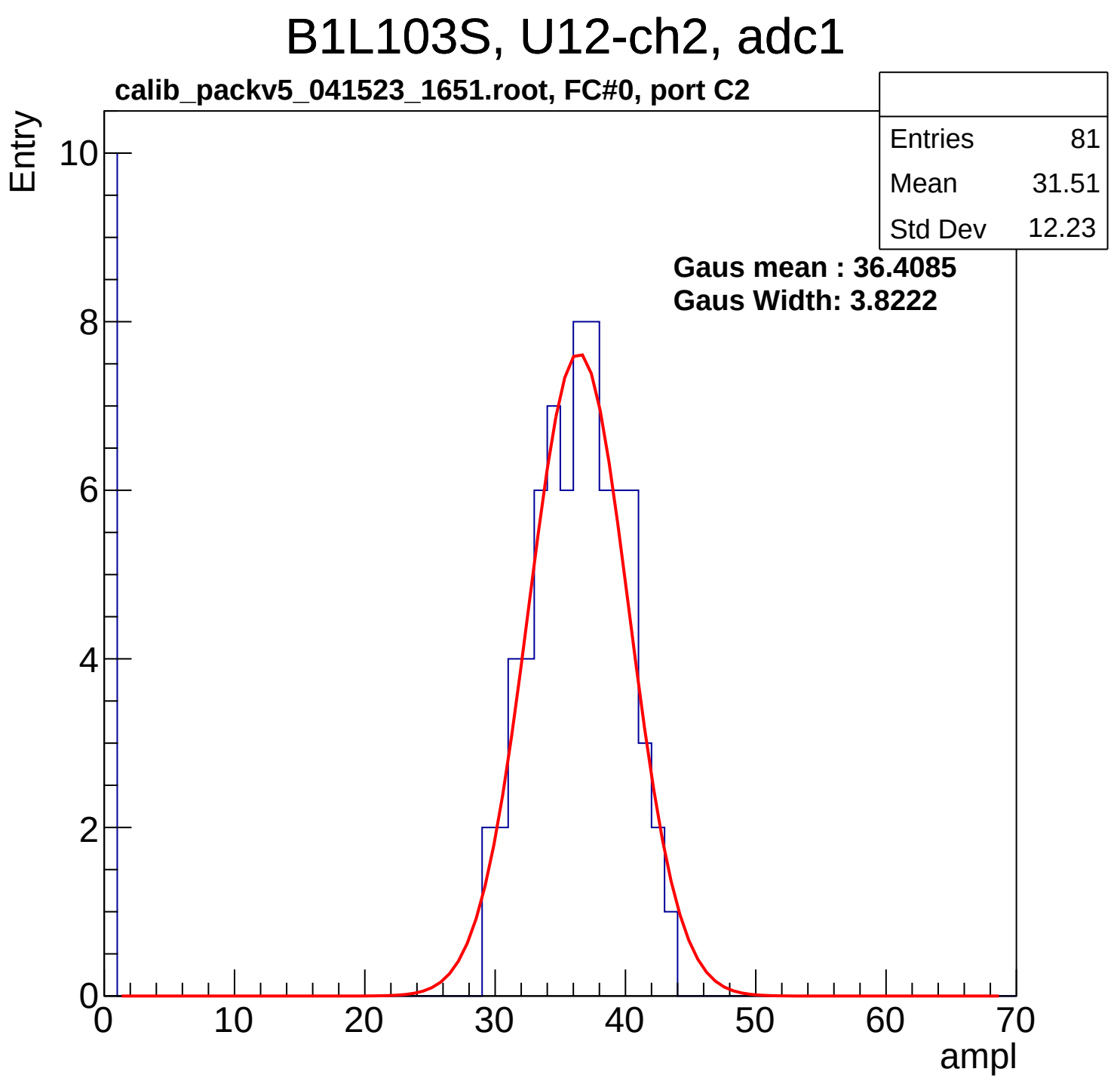
B1L103S, U12-ch2, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 31.51
Std Dev 12.23
Gaus mean : 36.4085
Gaus Width: 3.8222
Entry
ampl
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0
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60
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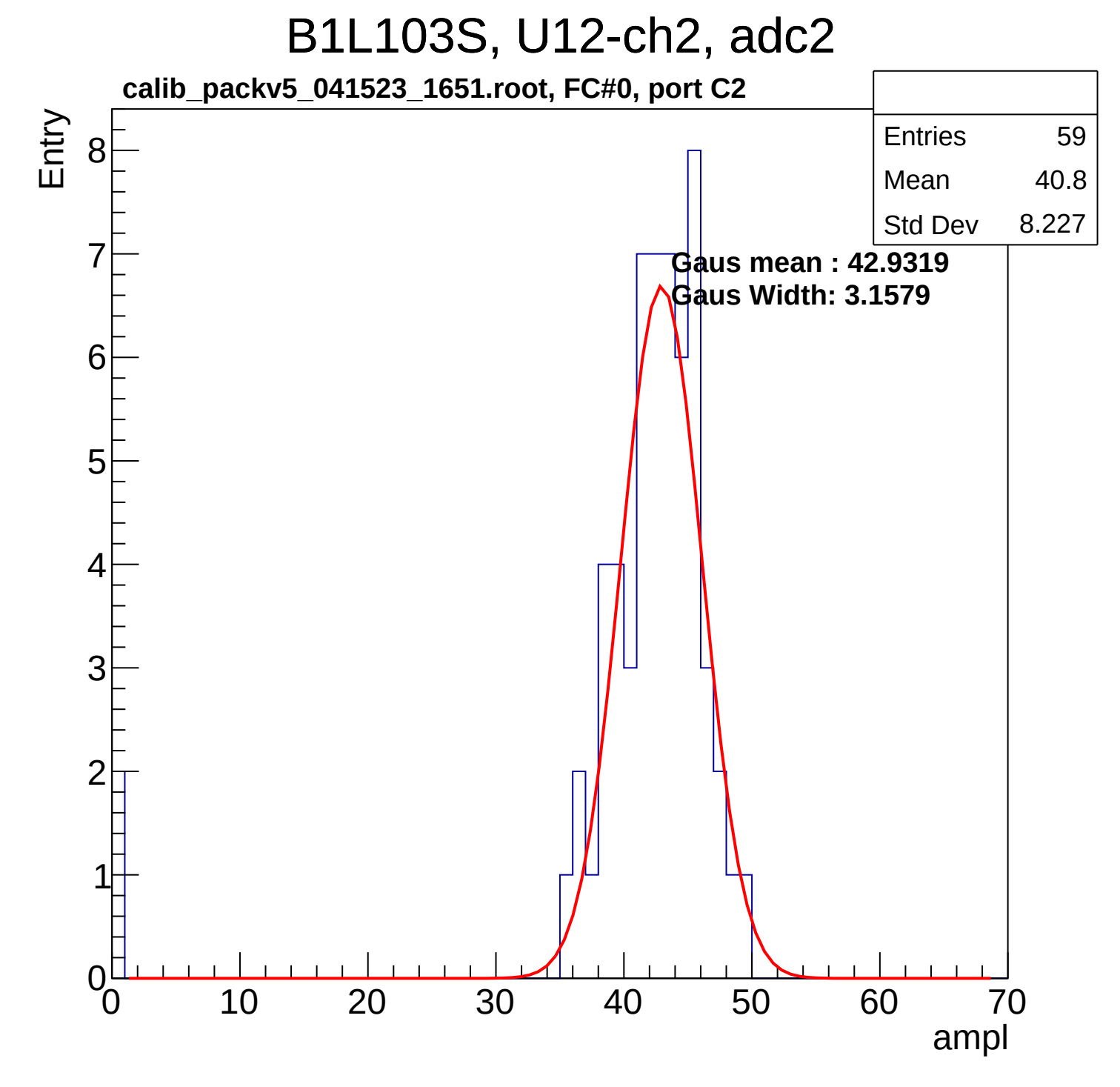
B1L103S, U12-ch2, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 40.8
Std Dev 8.227
Gaus mean : 42.9319
Gaus Width: 3.1579
Entry
ampl
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1
2
3
4
5
6
7
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0
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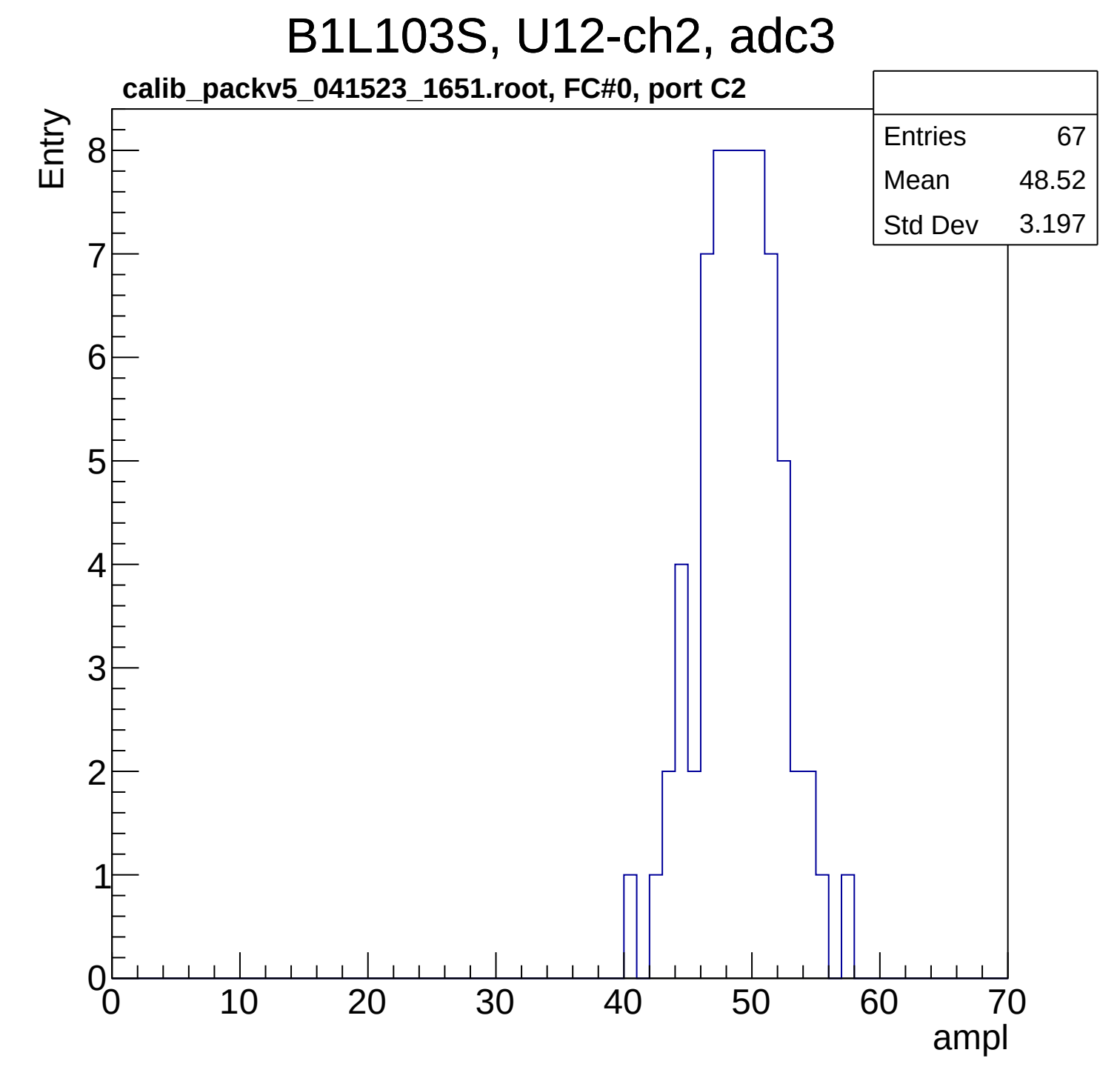
B1L103S, U12-ch2, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 48.52
Std Dev 3.197
Entry
ampl
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6
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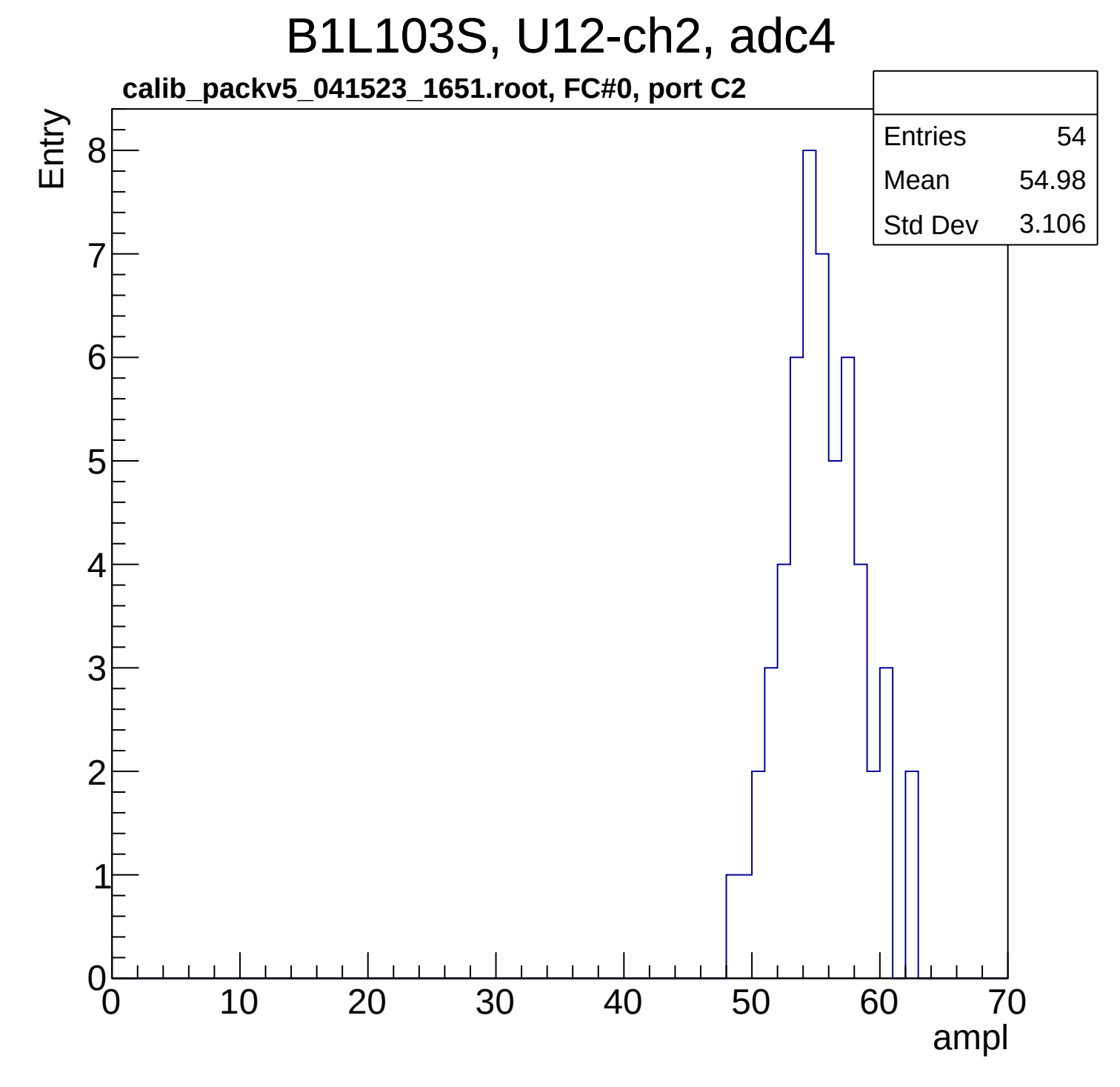
B1L103S, U12-ch2, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 54.98
Std Dev 3.106
Entry
ampl
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3
4
5
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7
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0
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60
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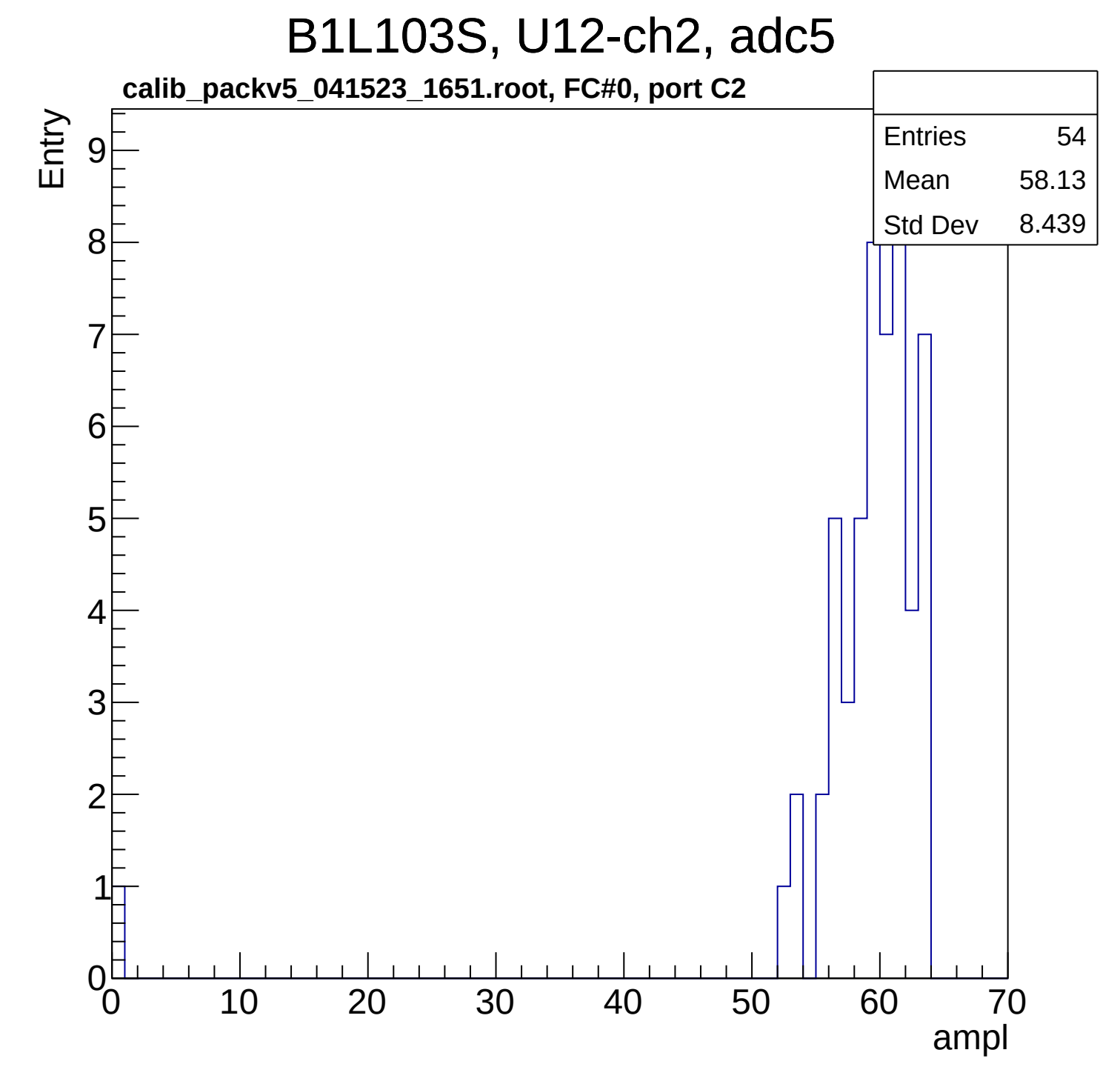
B1L103S, U12-ch2, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.13
Std Dev 8.439
Entry
ampl
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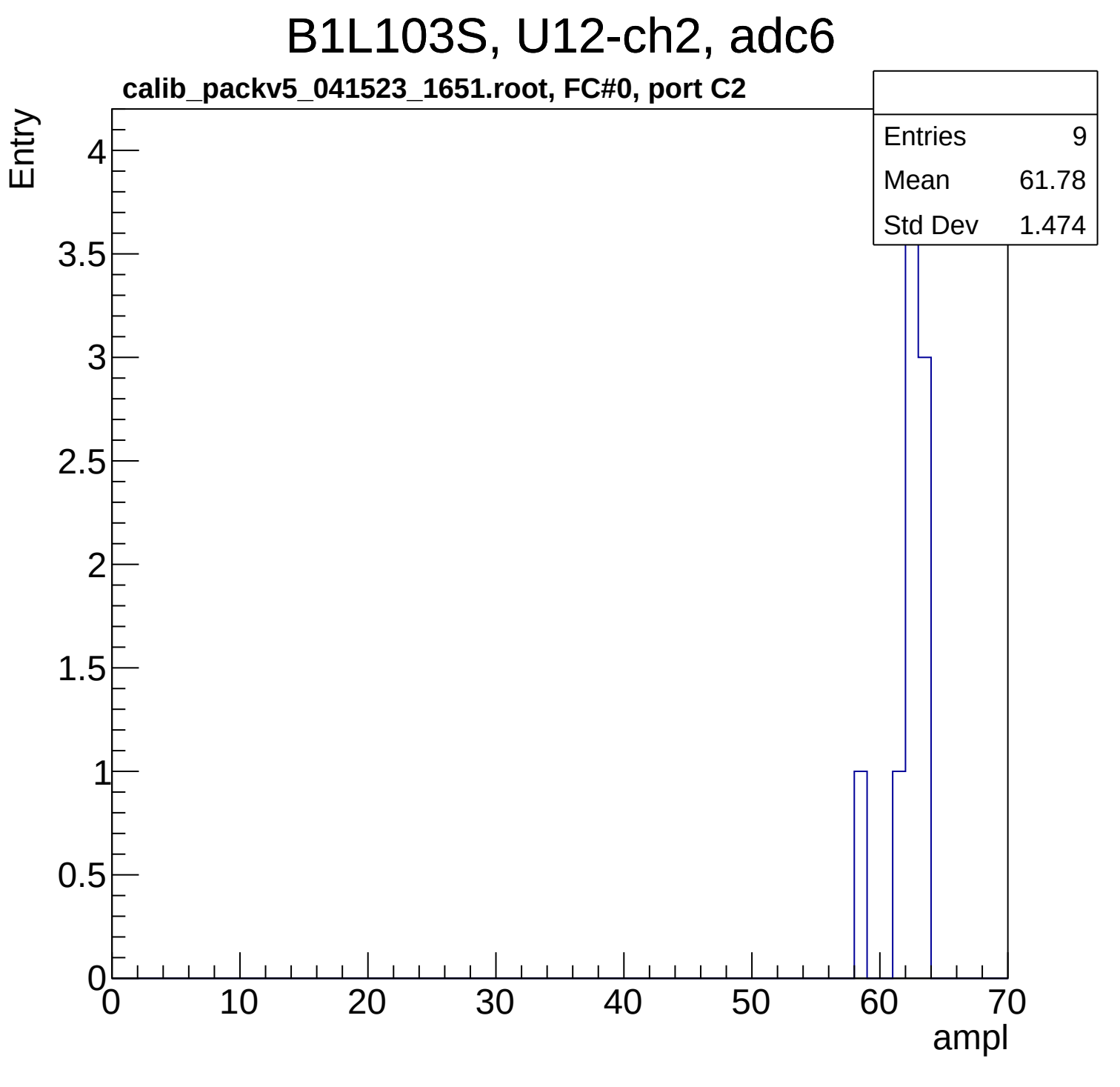
B1L103S, U12-ch2, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.78
Std Dev 1.474
Entry
ampl
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1.5
2
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3.5
4
0
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60
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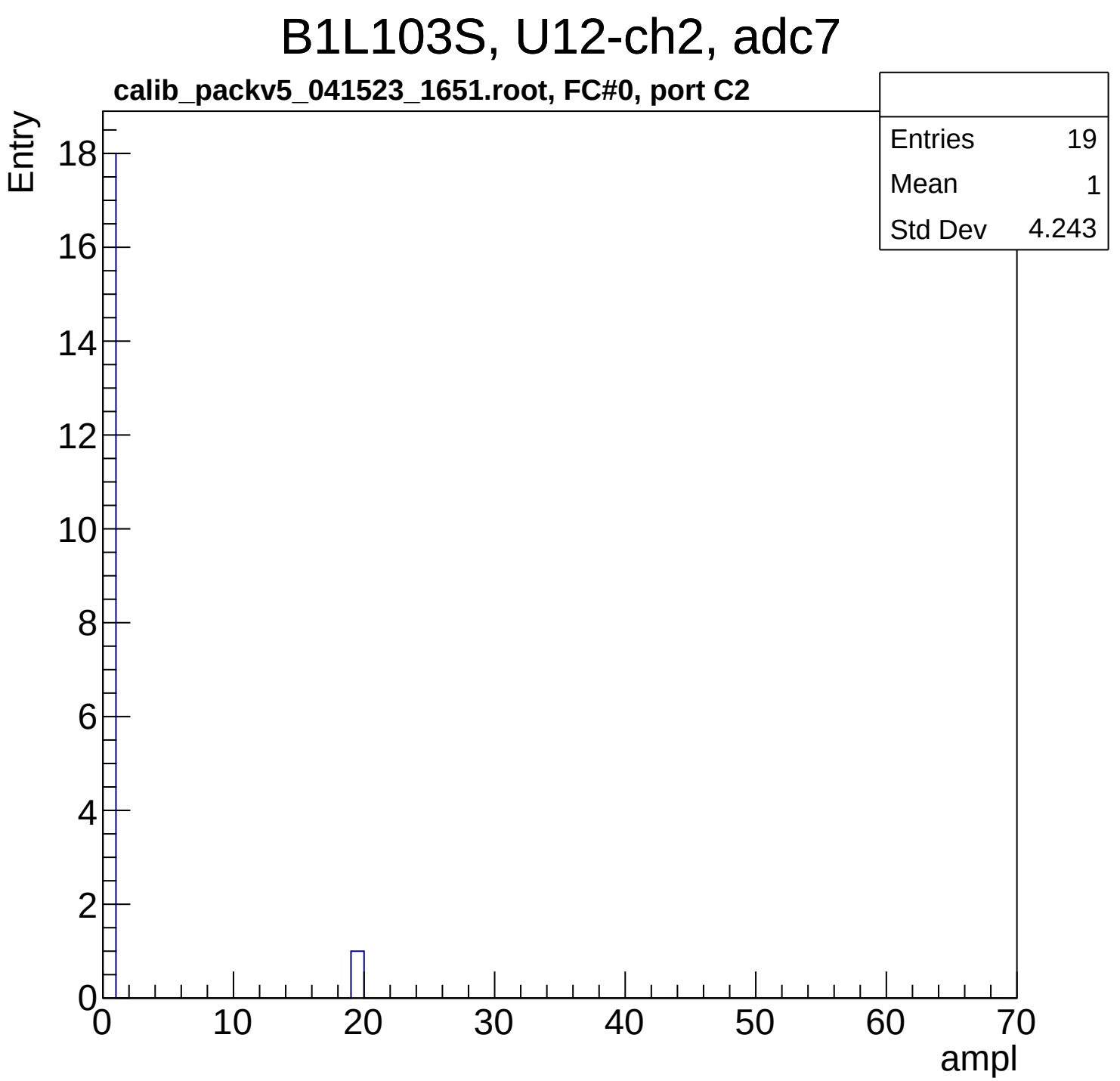
B1L103S, U12-ch2, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1
Std Dev 4.243
Entry
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10
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10
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30
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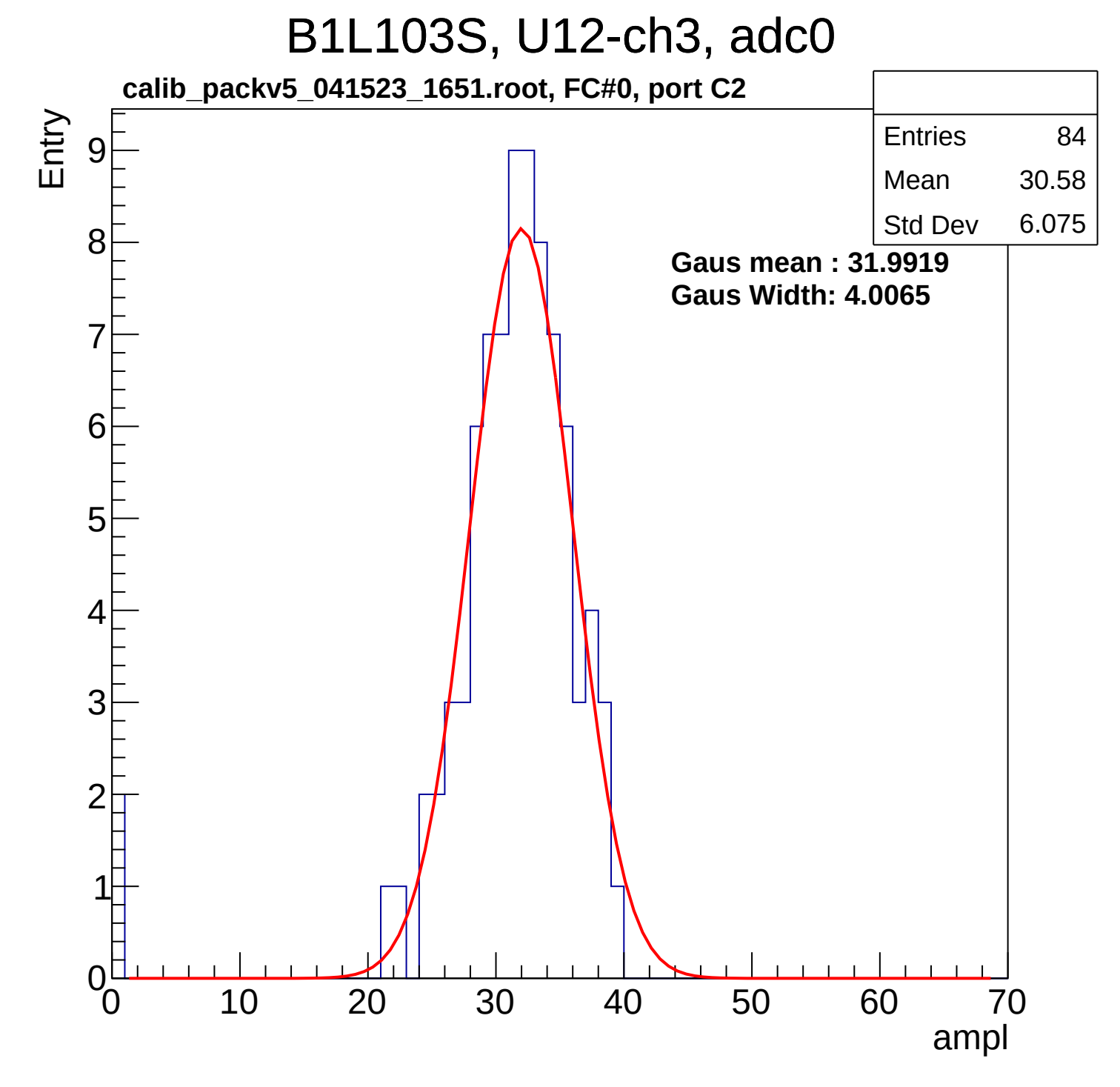
60
70
ampl


B1L103S, U12-ch3, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 30.58
Std Dev 6.075
Gaus mean : 31.9919
Gaus Width: 4.0065
Entry
ampl
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3
4
5
6
7
8
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0
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60
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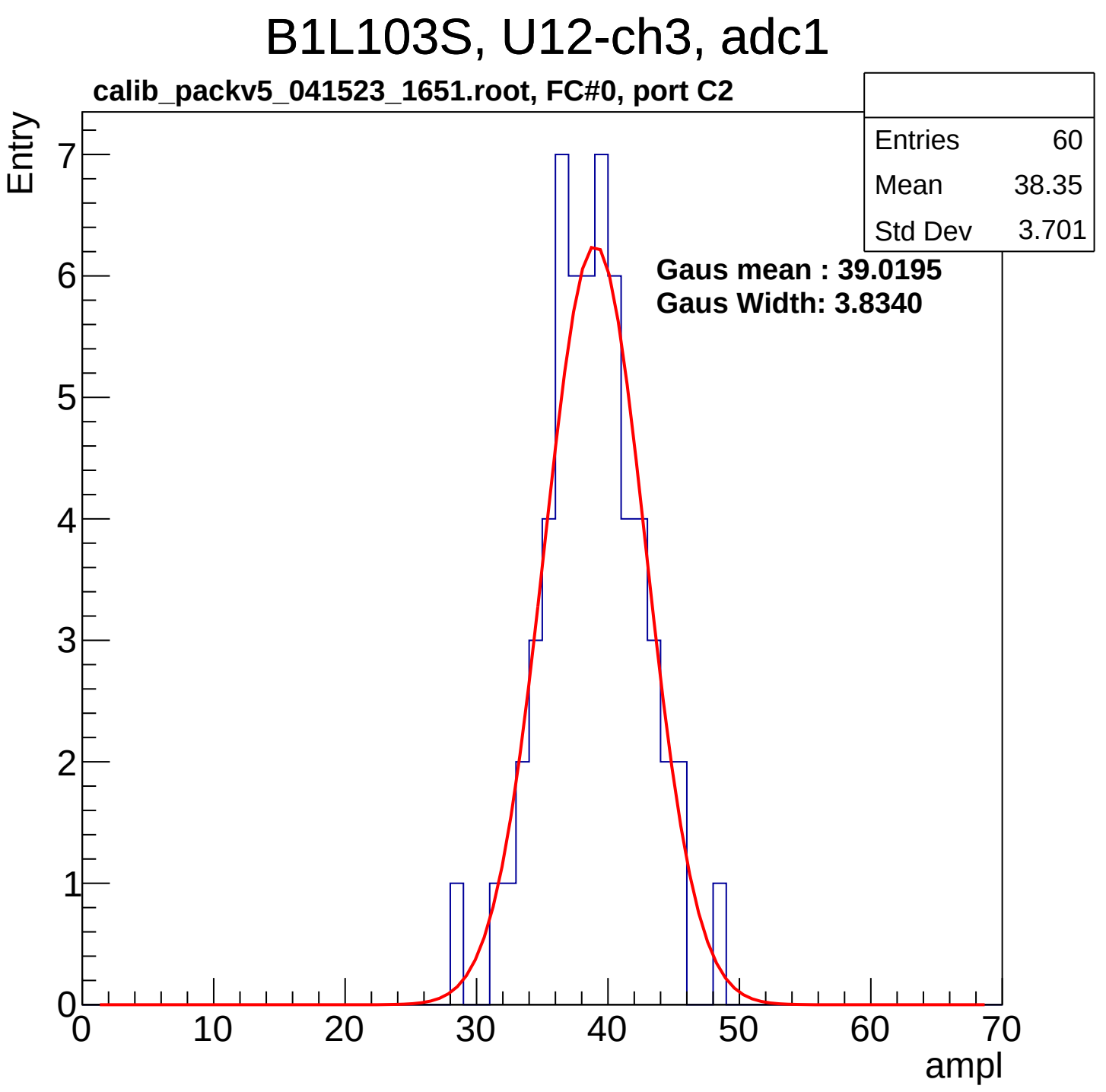
B1L103S, U12-ch3, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 38.35
Std Dev 3.701
Gaus mean : 39.0195
Gaus Width: 3.8340
Entry
ampl
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1
2
3
4
5
6
7
0
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20
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50
60
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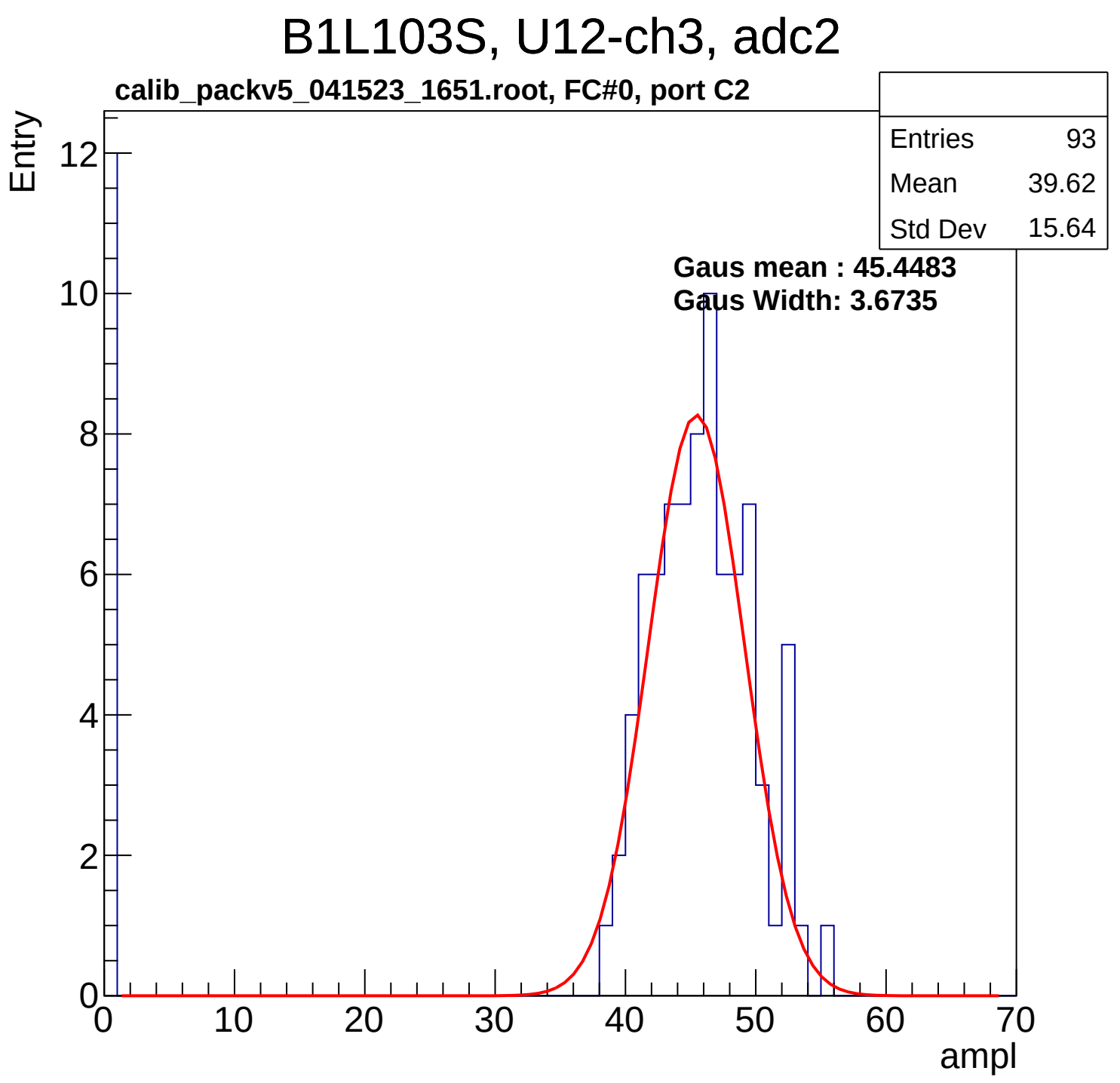
B1L103S, U12-ch3, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 39.62
Std Dev 15.64
Gaus mean : 45.4483
Gaus Width: 3.6735
Entry
ampl
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2
4
6
8
10
12
0
10
20
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40
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60
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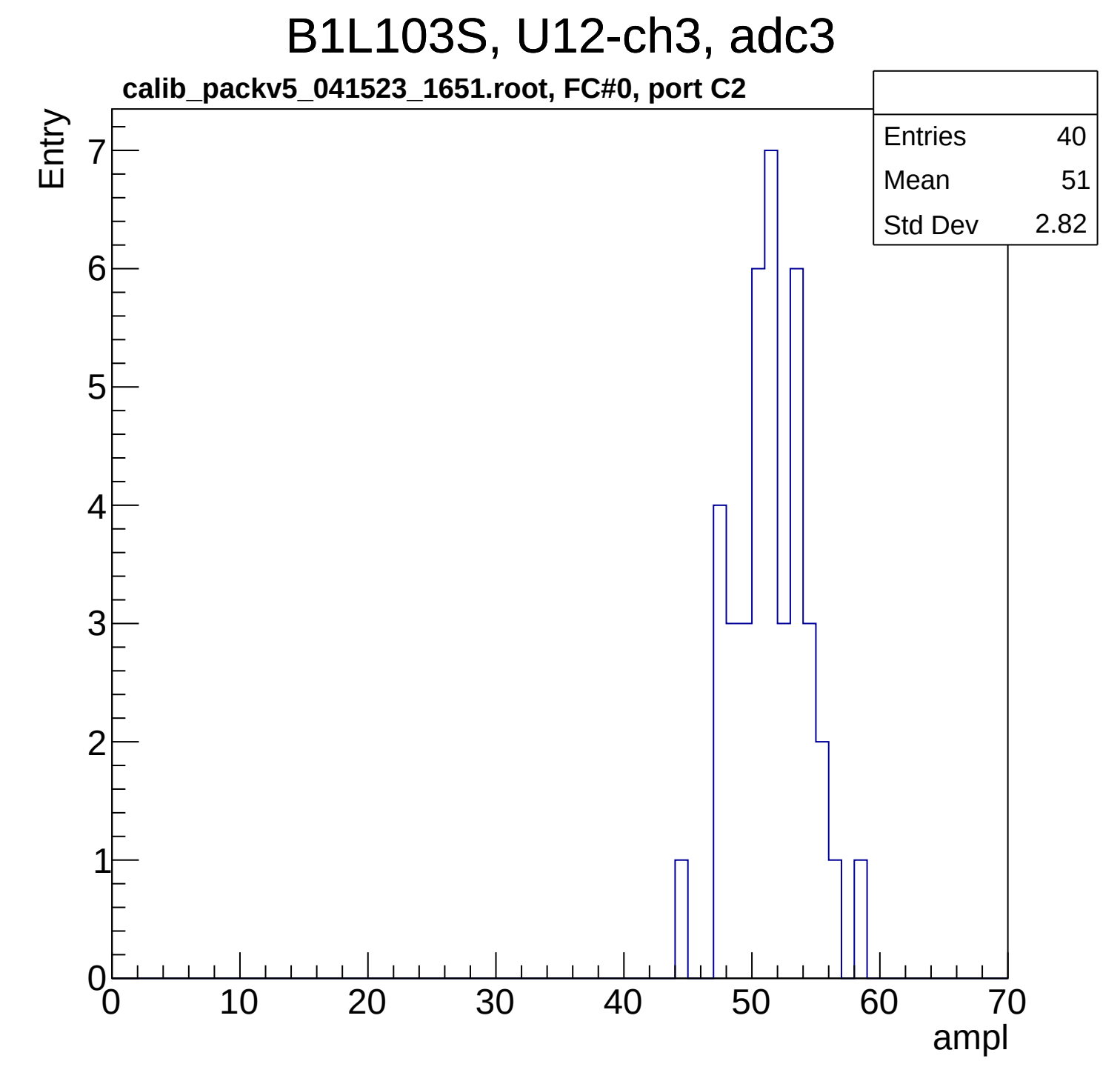
B1L103S, U12-ch3, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 51
Std Dev 2.82
Entry
ampl
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3
4
5
6
7
0
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20
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40
50
60
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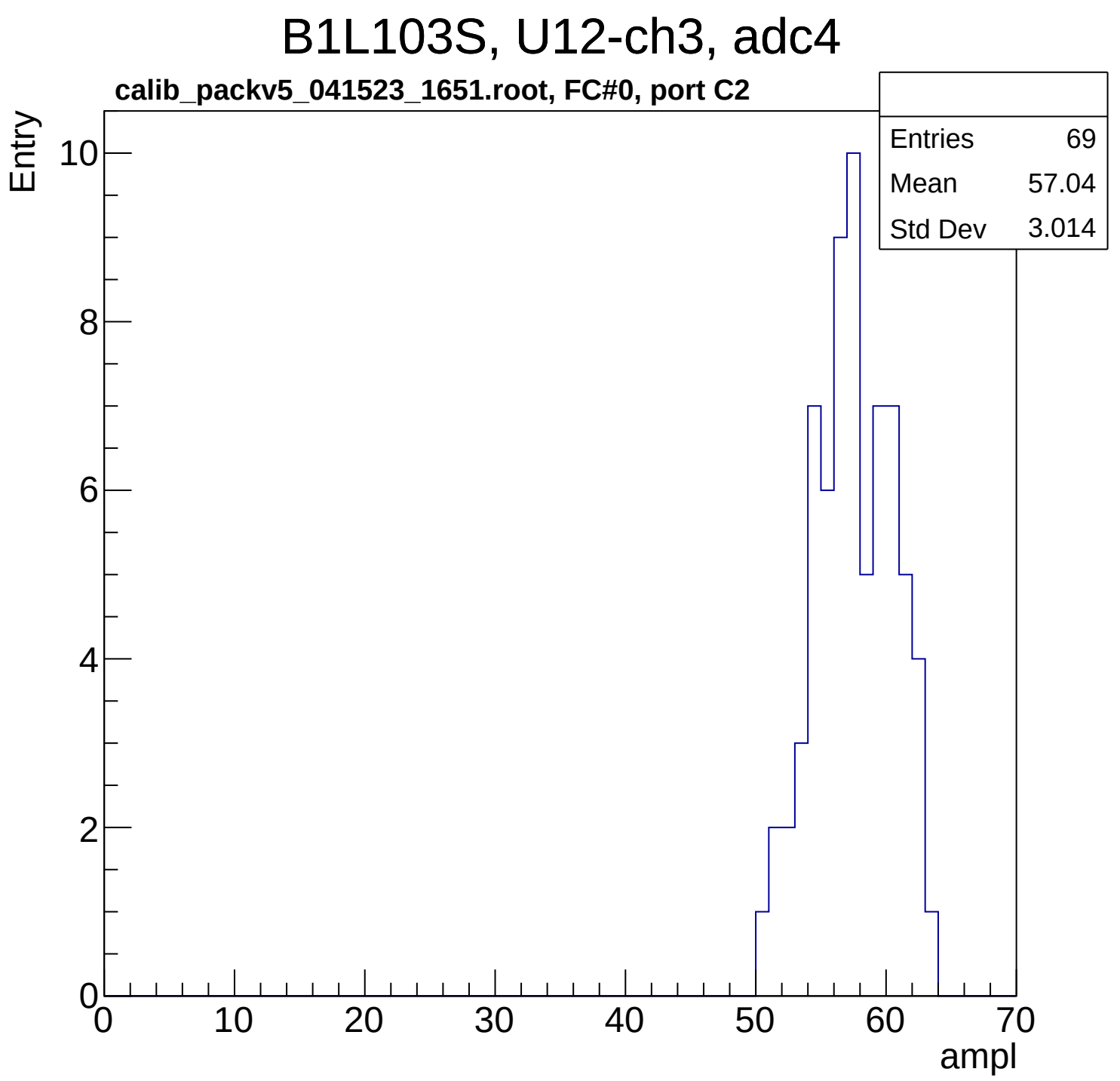
B1L103S, U12-ch3, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 57.04
Std Dev 3.014
Entry
ampl
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6
8
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40
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60
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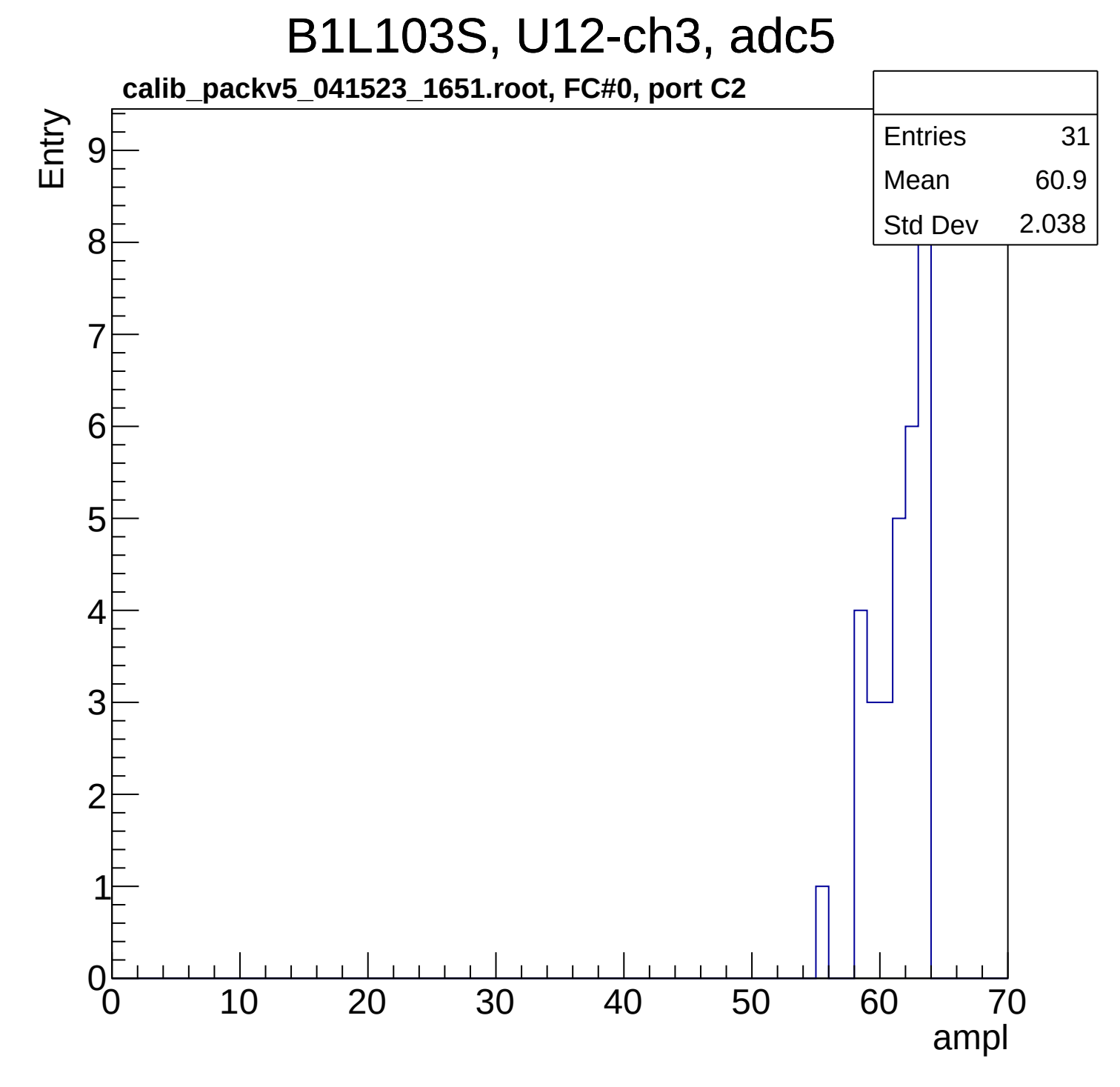
B1L103S, U12-ch3, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 60.9
Std Dev 2.038
Entry
ampl
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4
5
6
7
8
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0
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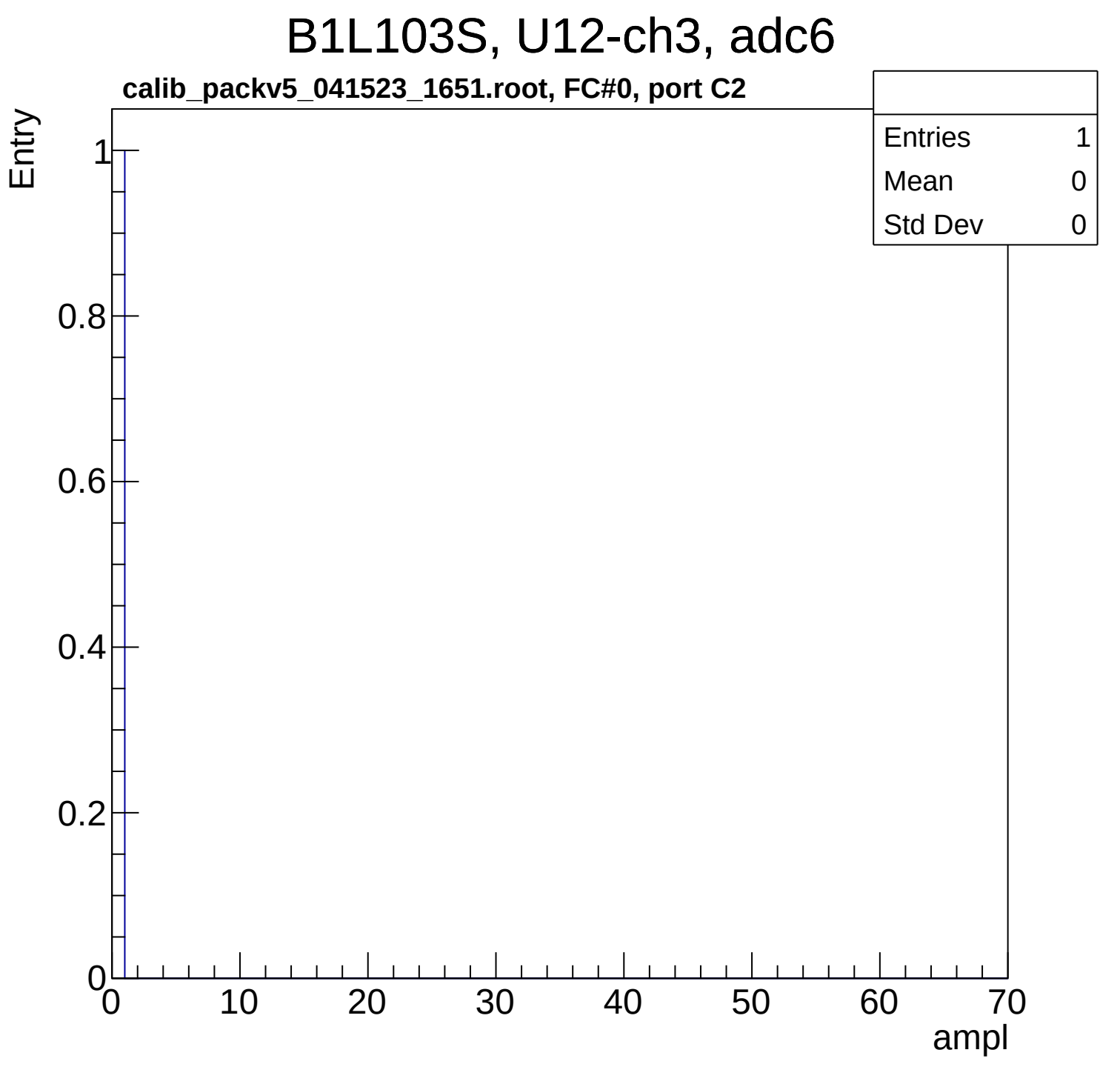
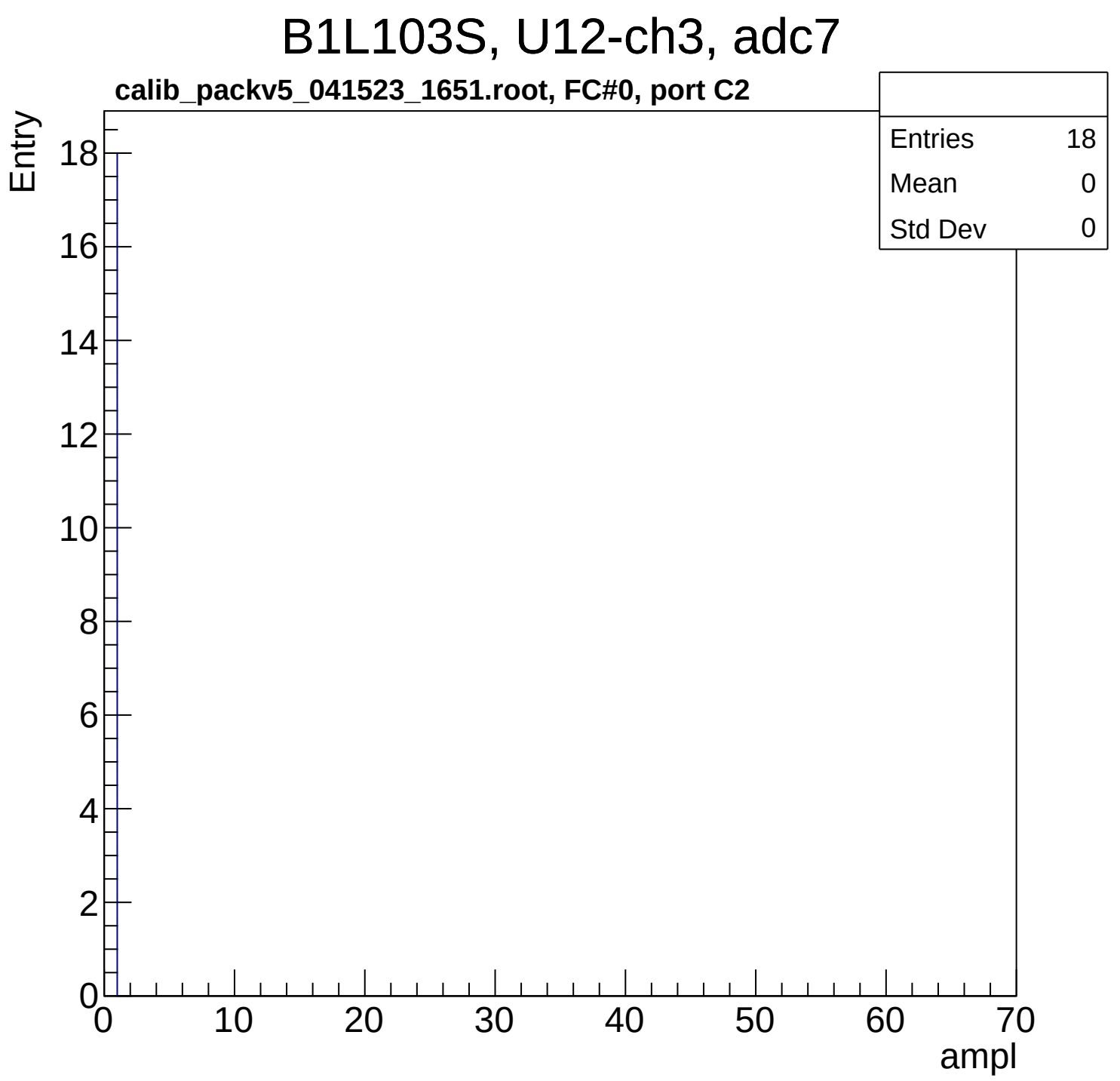
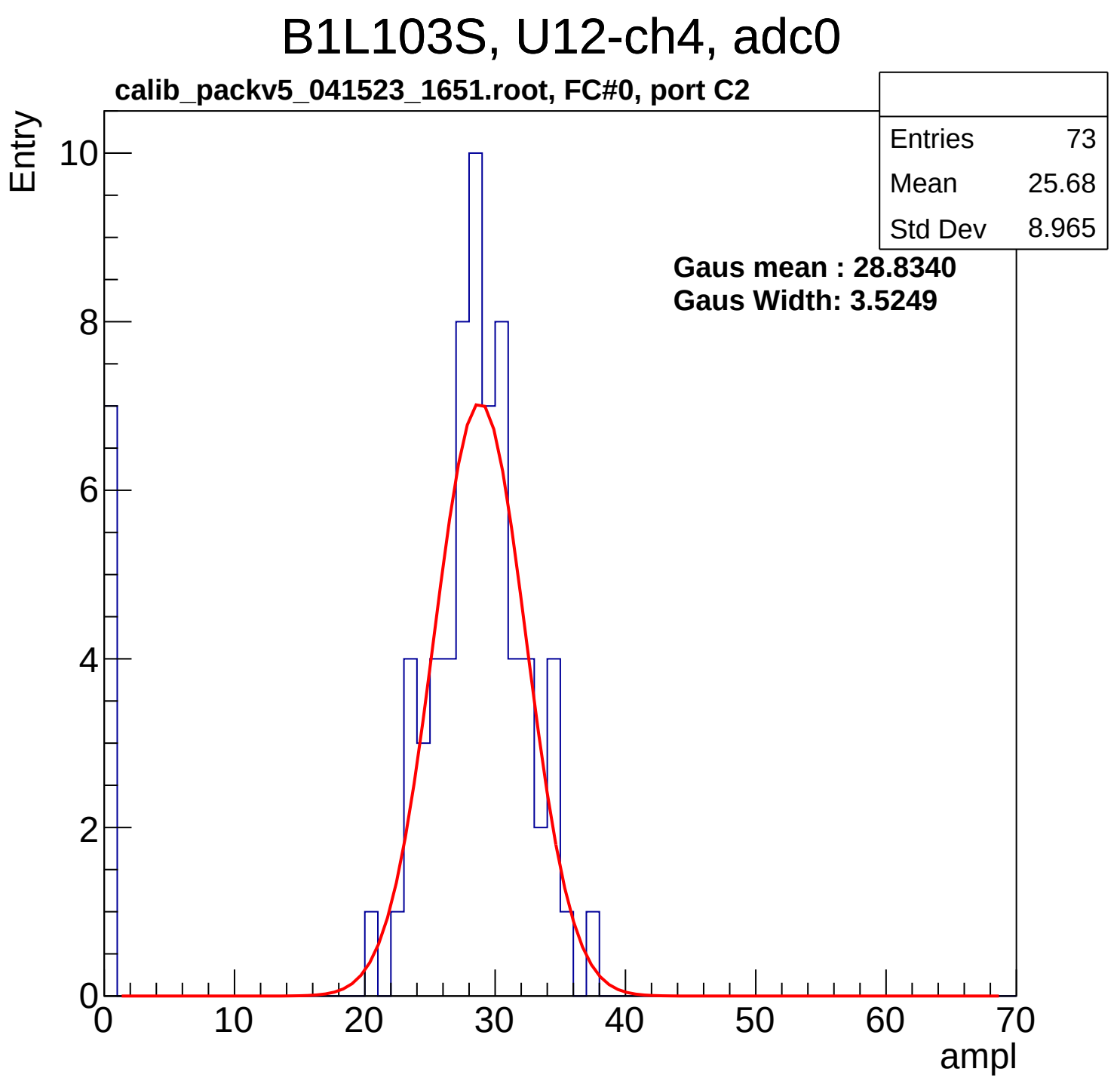
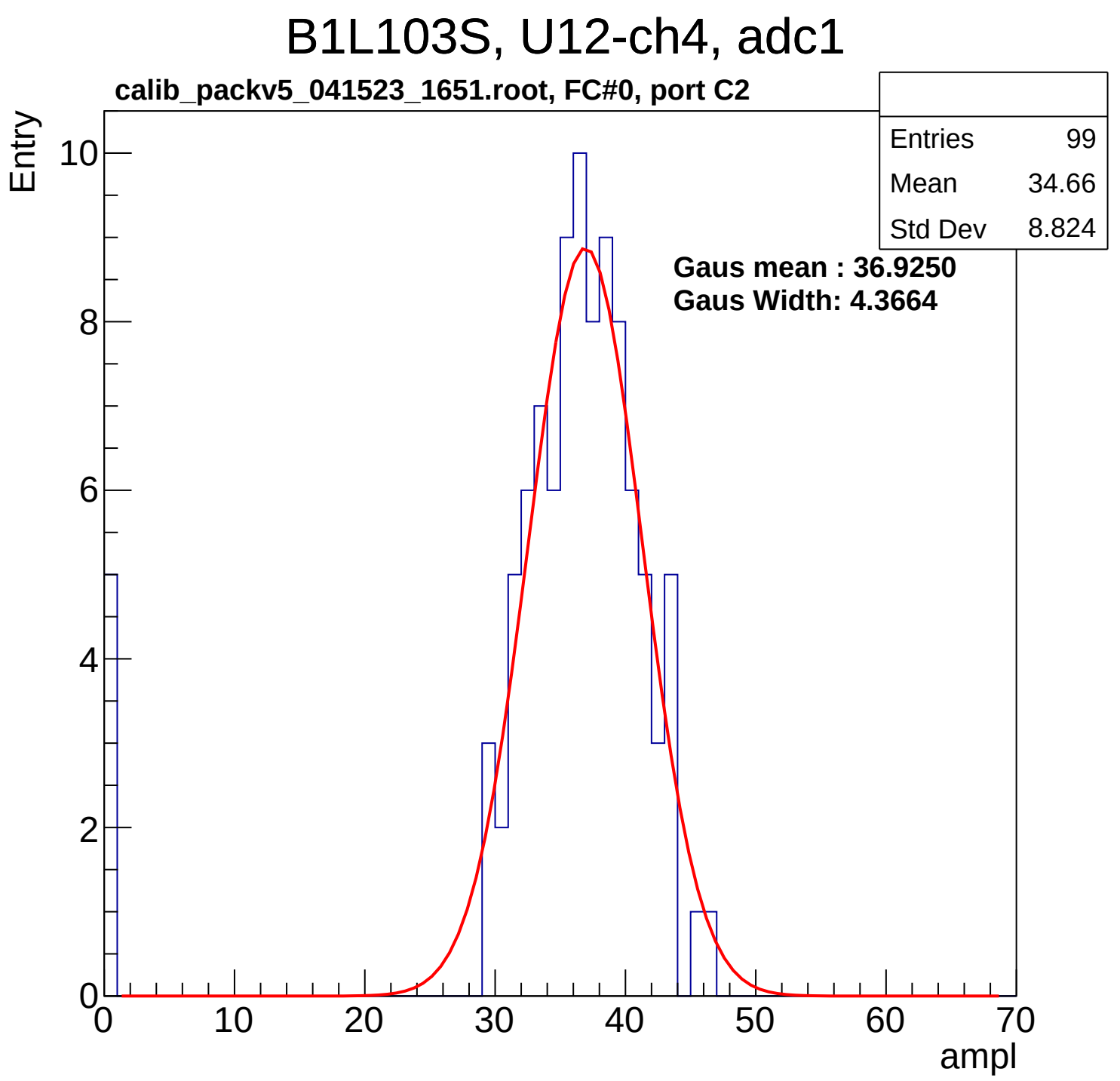

B1L103S, U12-ch3, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch3, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch4, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 25.68
Std Dev 8.965
Gaus mean : 28.8340
Gaus Width: 3.5249
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch4, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 34.66
Std Dev 8.824
Gaus mean : 36.9250
Gaus Width: 4.3664
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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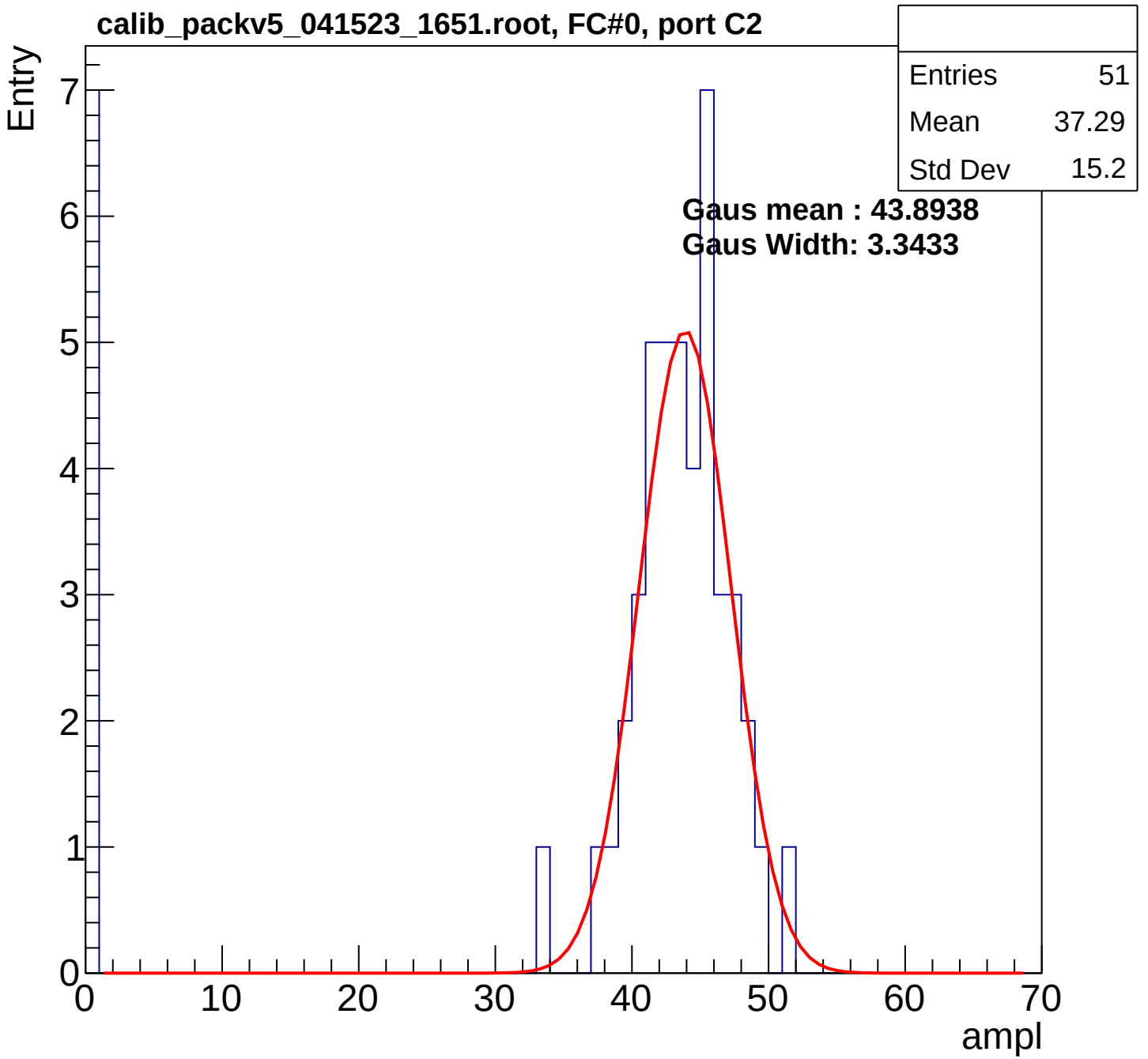
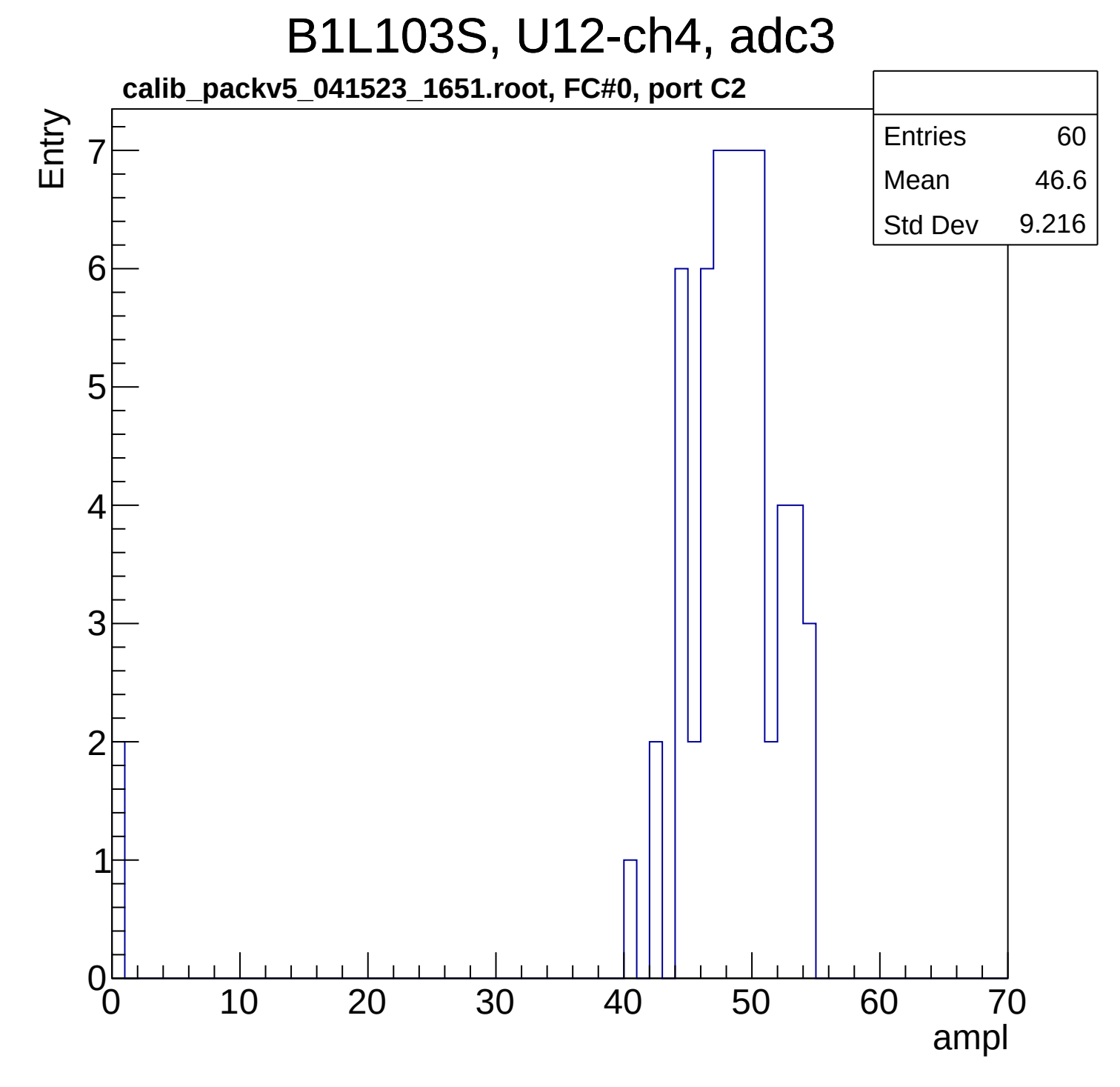

B1L103S, U12-ch4, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 37.29
Std Dev 15.2
Gaus mean : 43.8938
Gaus Width: 3.3433
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U12-ch4, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 46.6
Std Dev 9.216
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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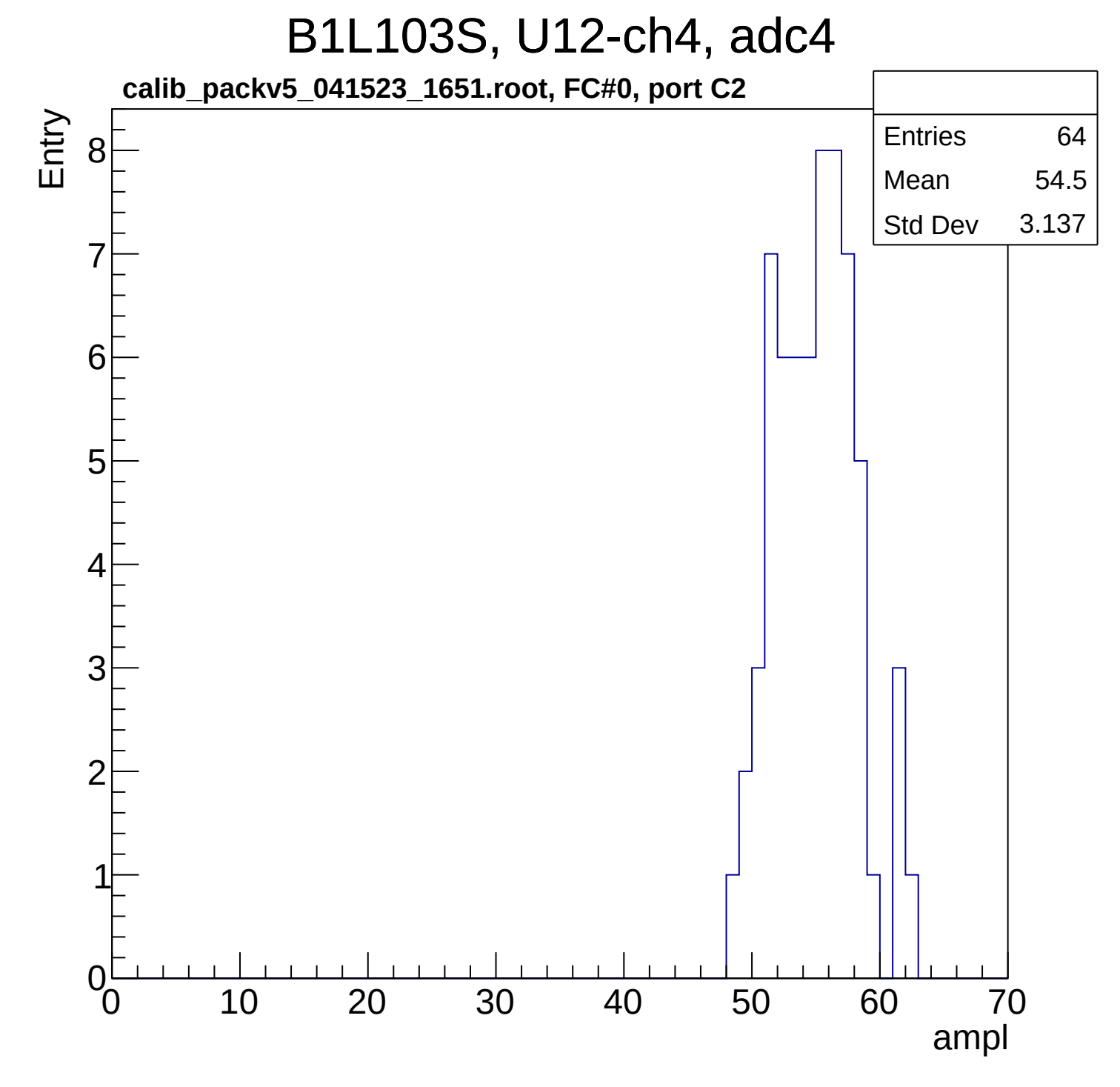
B1L103S, U12-ch4, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 54.5
Std Dev 3.137
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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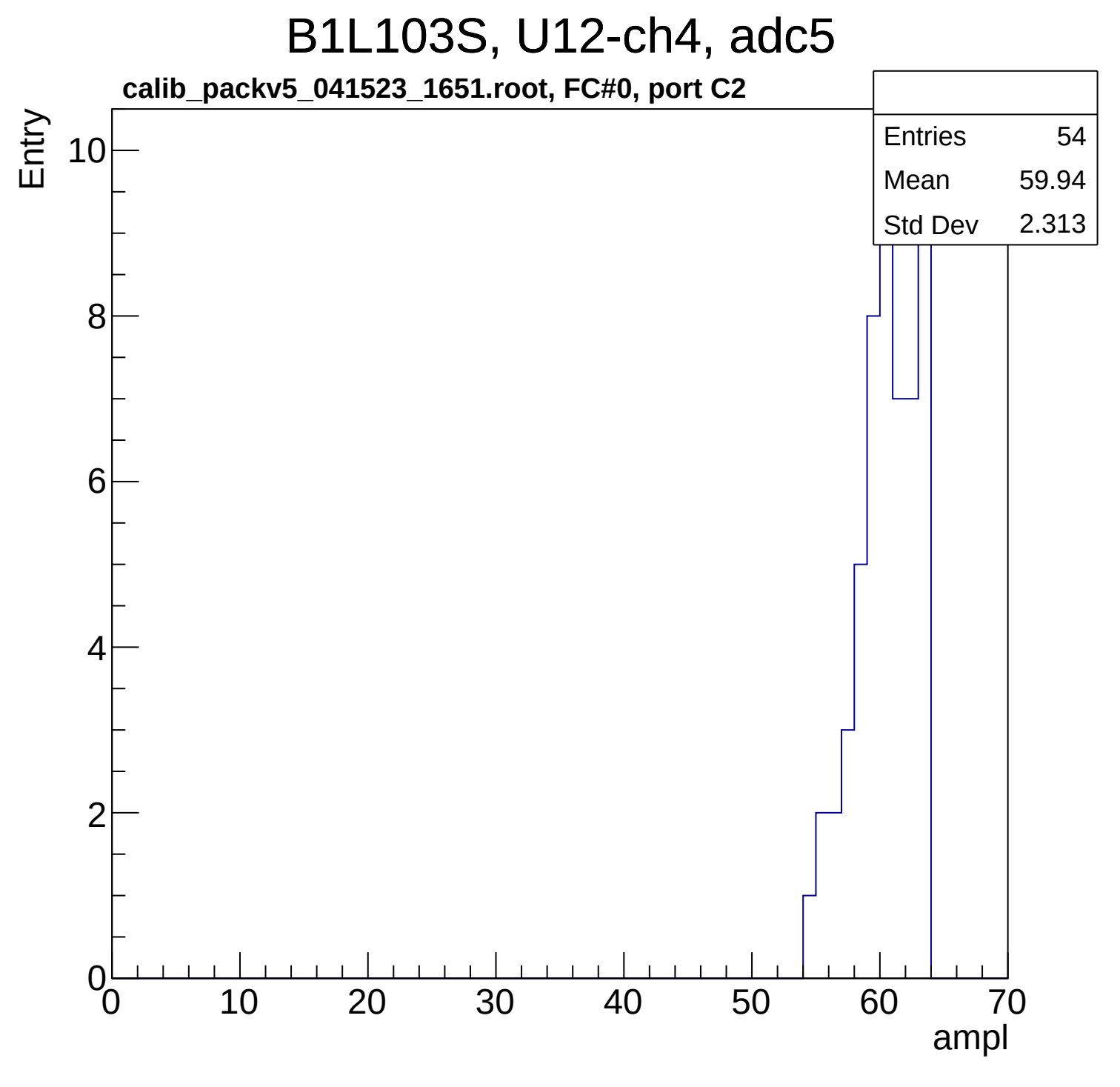
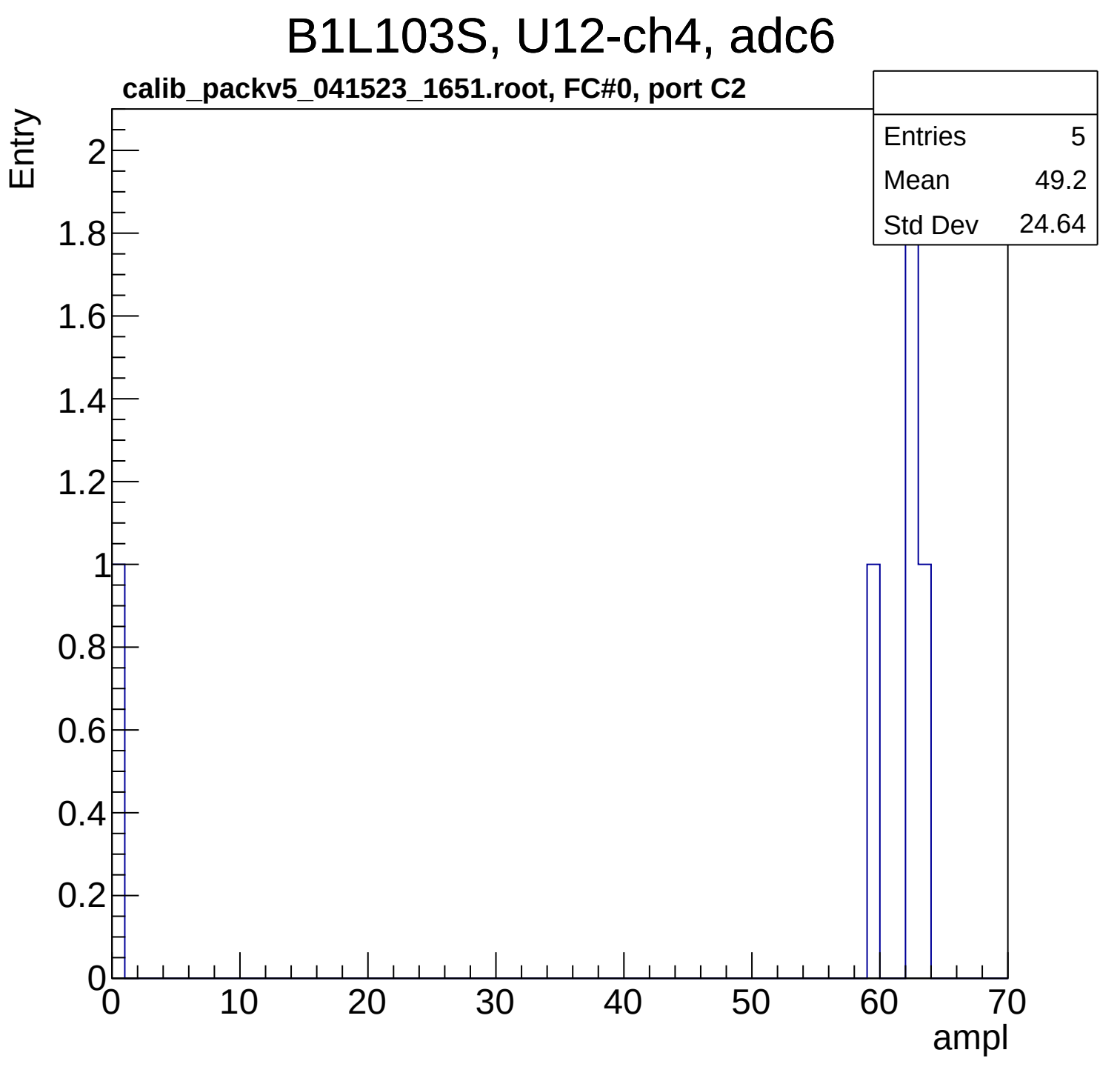

B1L103S, U12-ch4, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 59.94
Std Dev 2.313
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch4, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 49.2
Std Dev 24.64
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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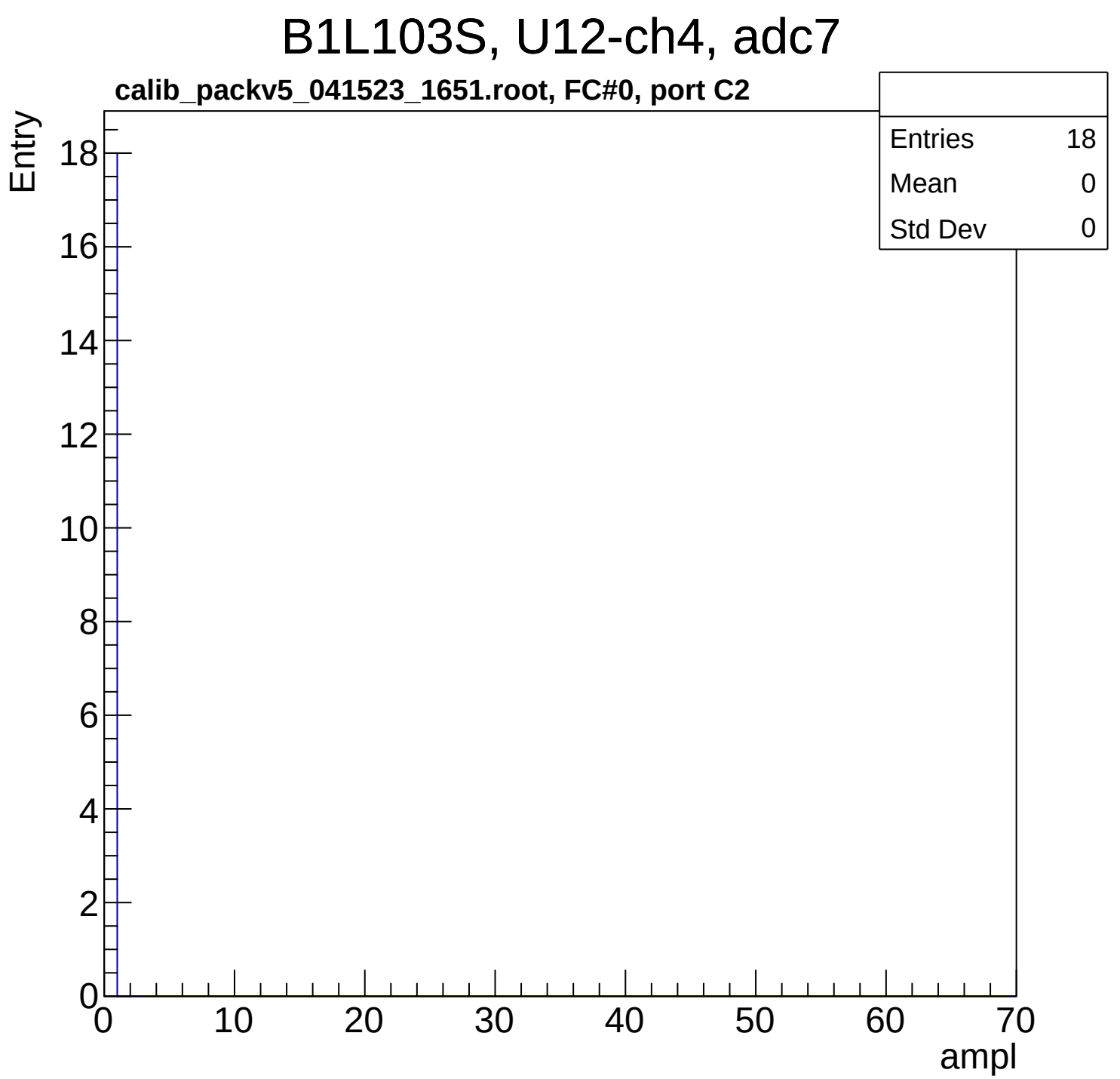
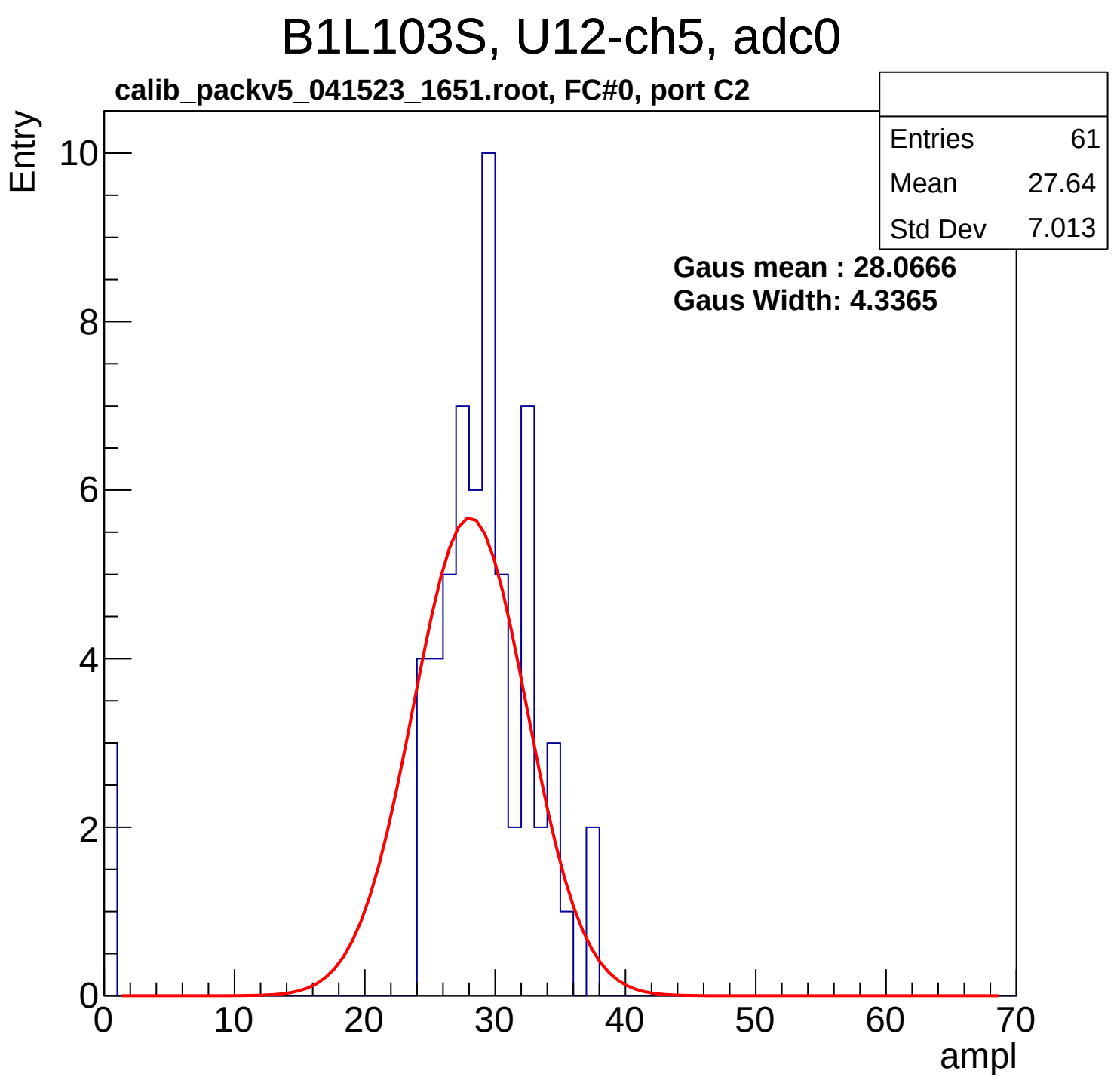
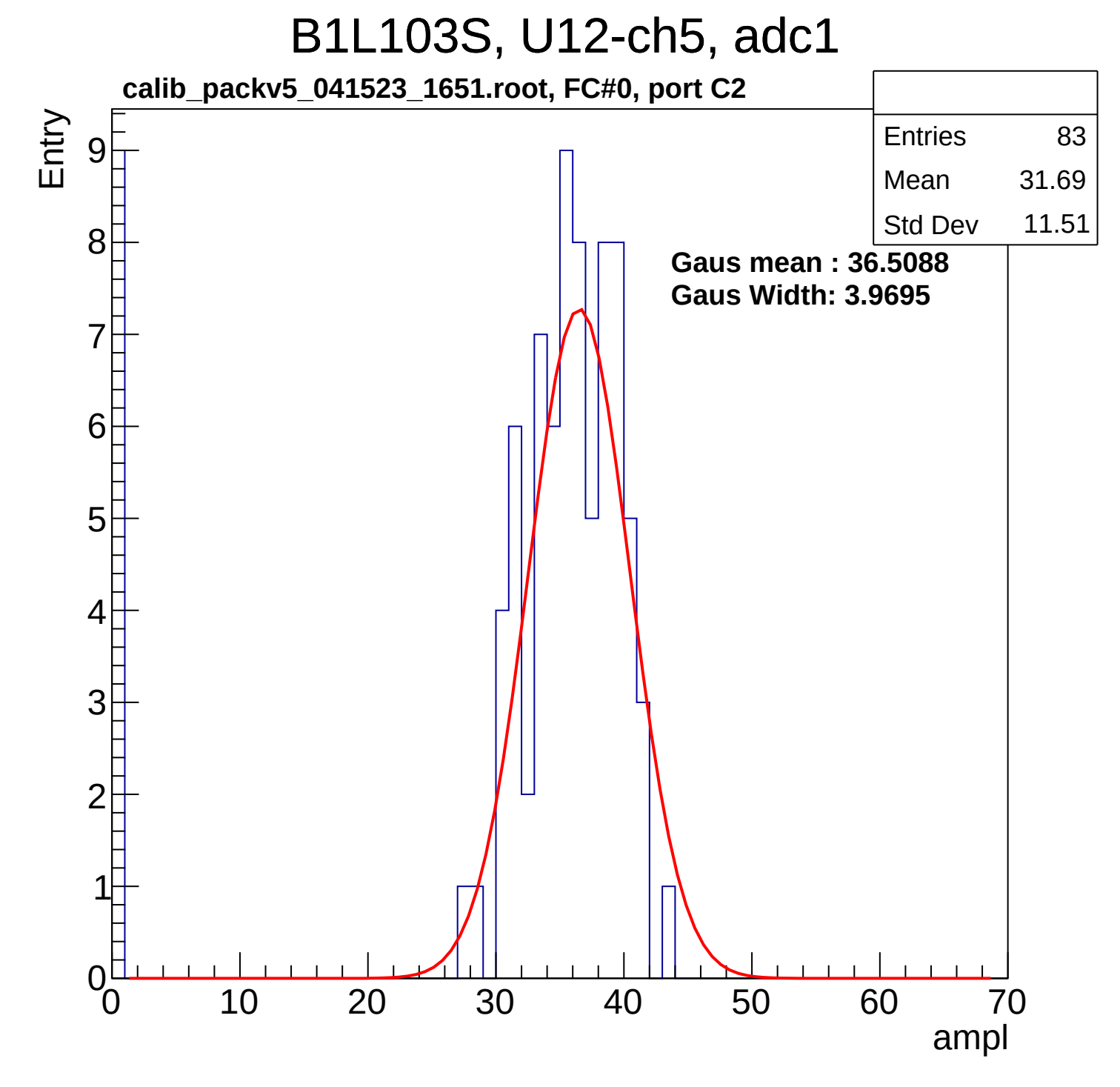
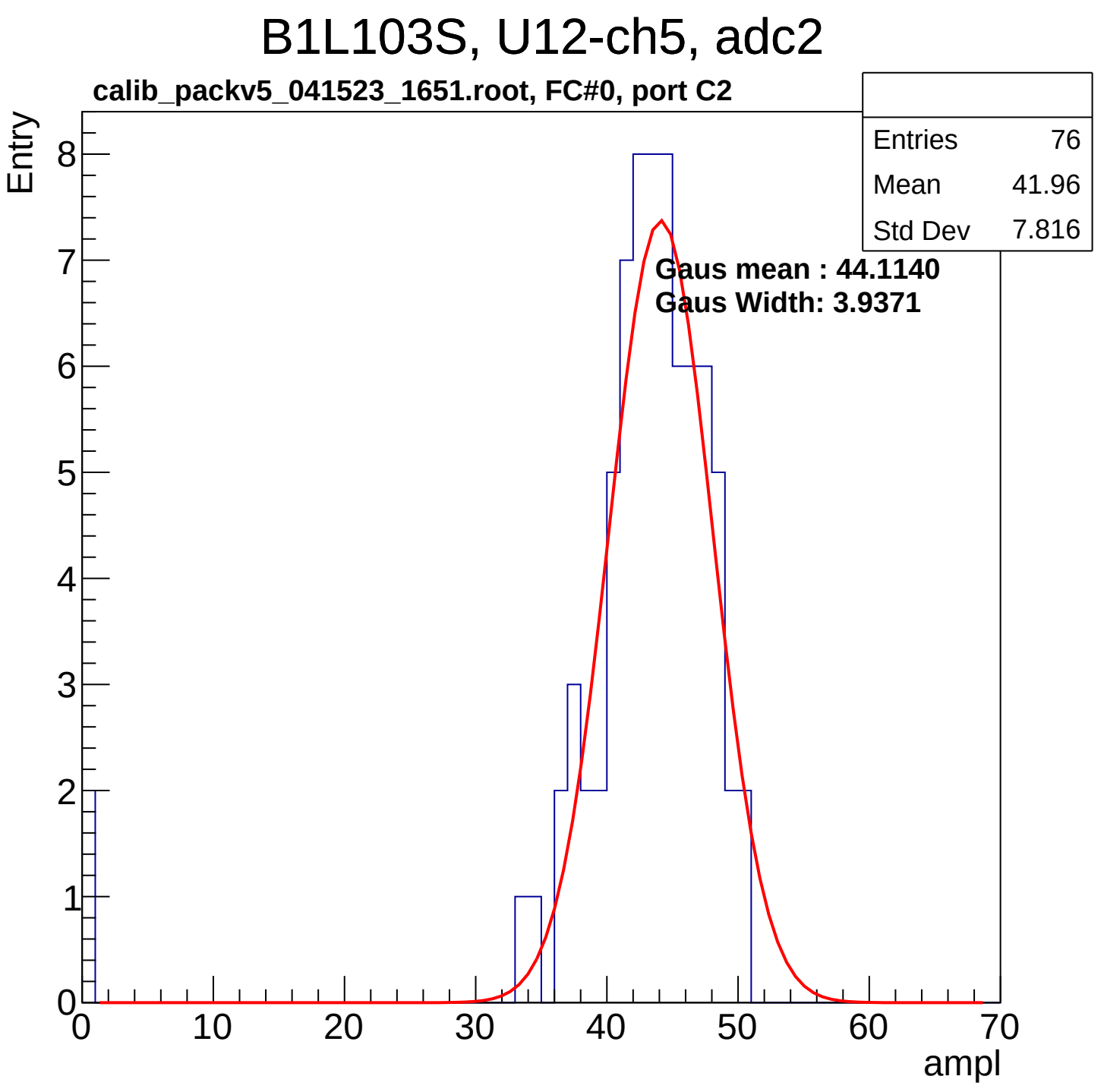
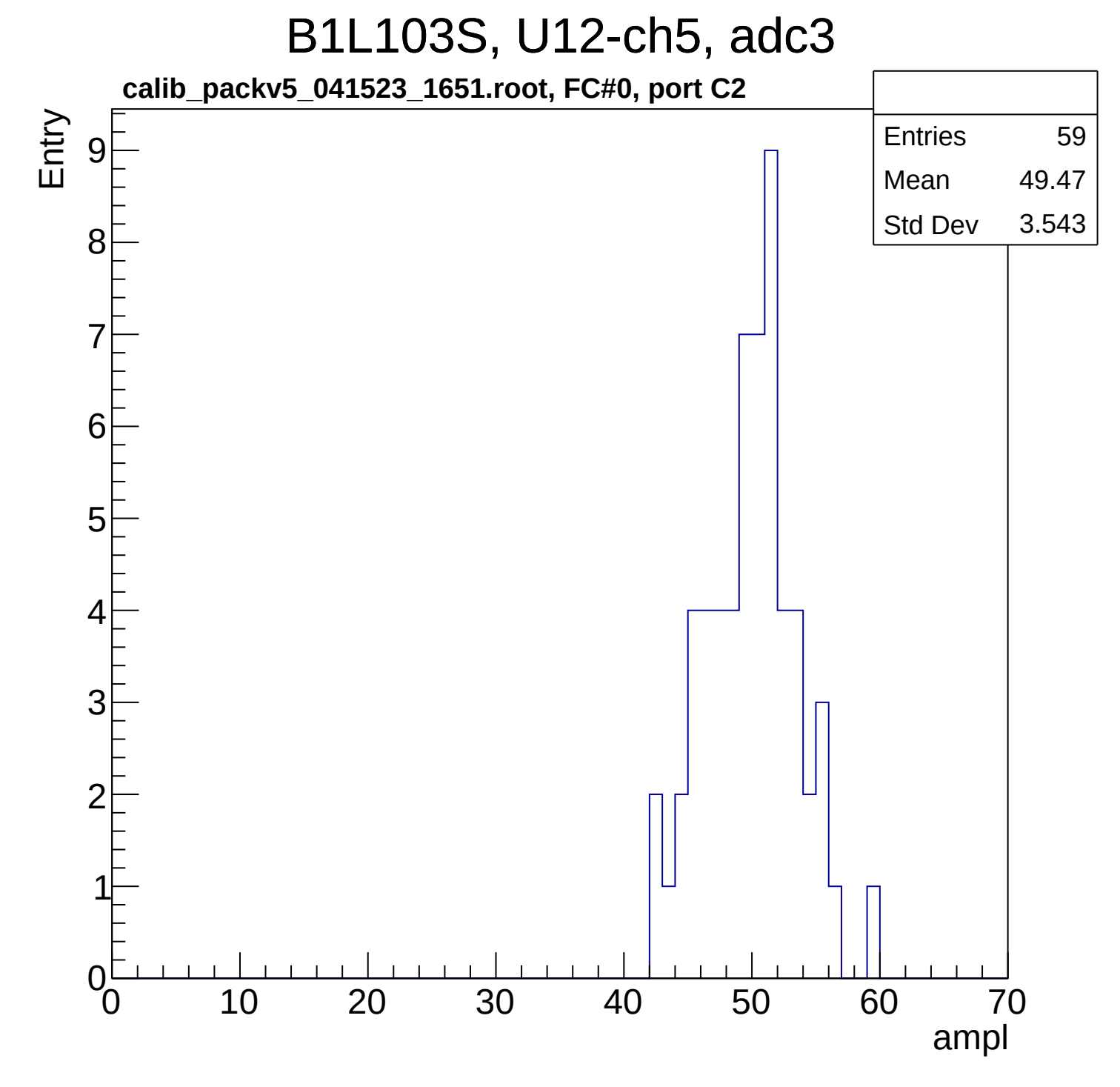
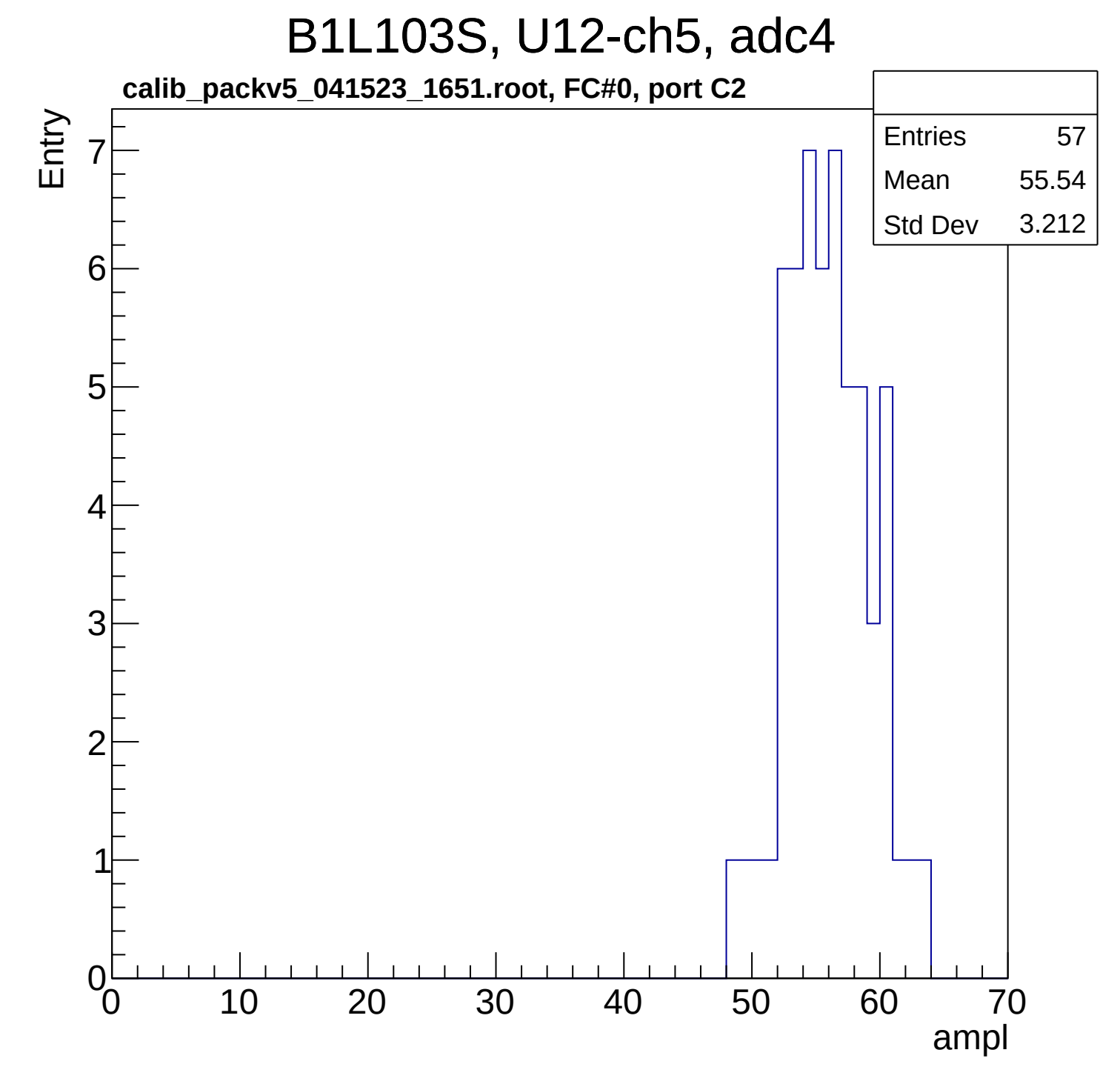

B1L103S, U12-ch4, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl

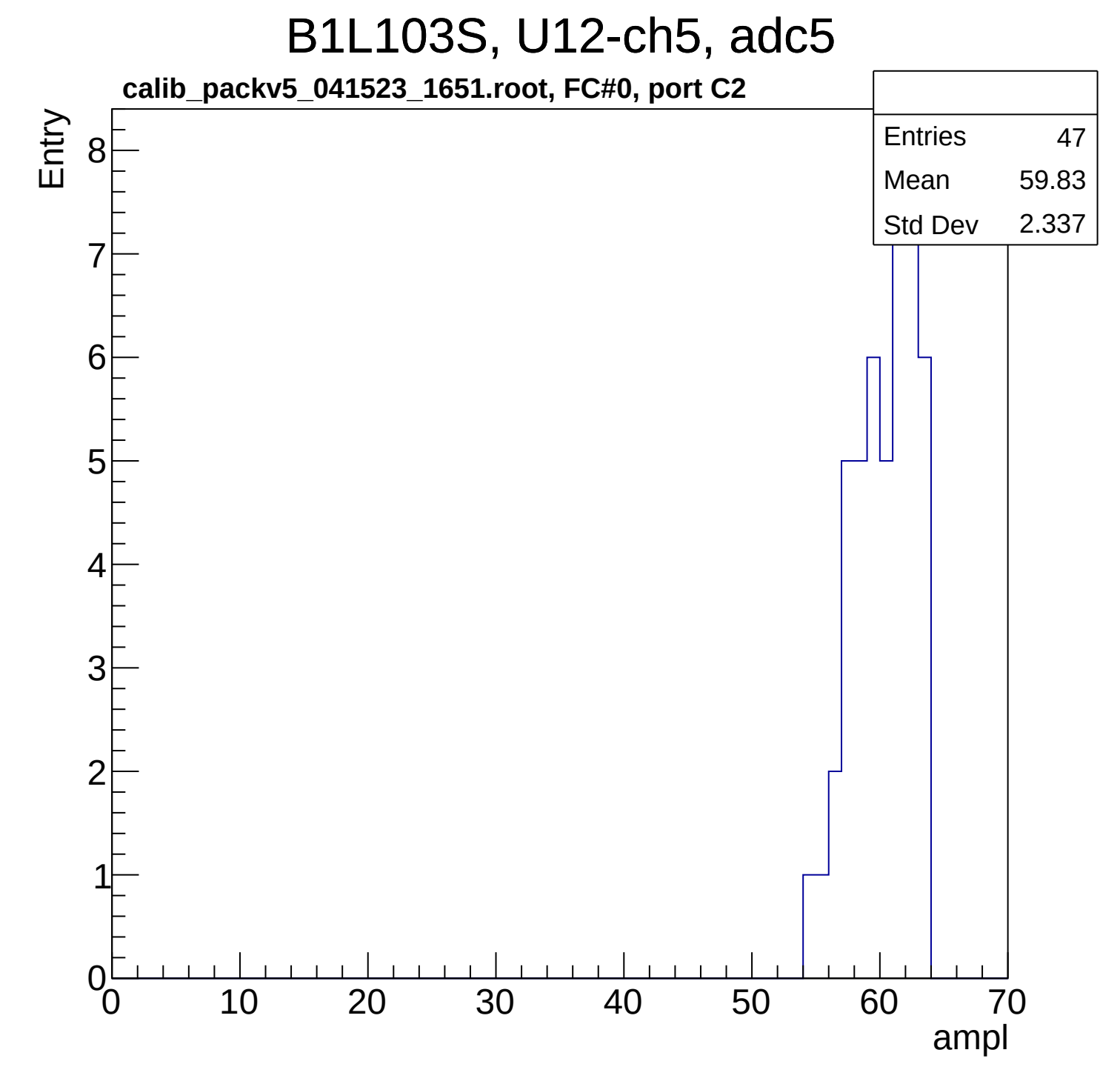

B1L103S, U12-ch5, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 27.64
Std Dev 7.013
Gaus mean : 28.0666
Gaus Width: 4.3365
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch5, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 31.69
Std Dev 11.51
Gaus mean : 36.5088
Gaus Width: 3.9695
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U12-ch5, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 41.96
Std Dev 7.816
Gaus mean : 44.1140
Gaus Width: 3.9371
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U12-ch5, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 49.47
Std Dev 3.543
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch5, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 55.54
Std Dev 3.212
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U12-ch5, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 59.83
Std Dev 2.337
Entry
ampl
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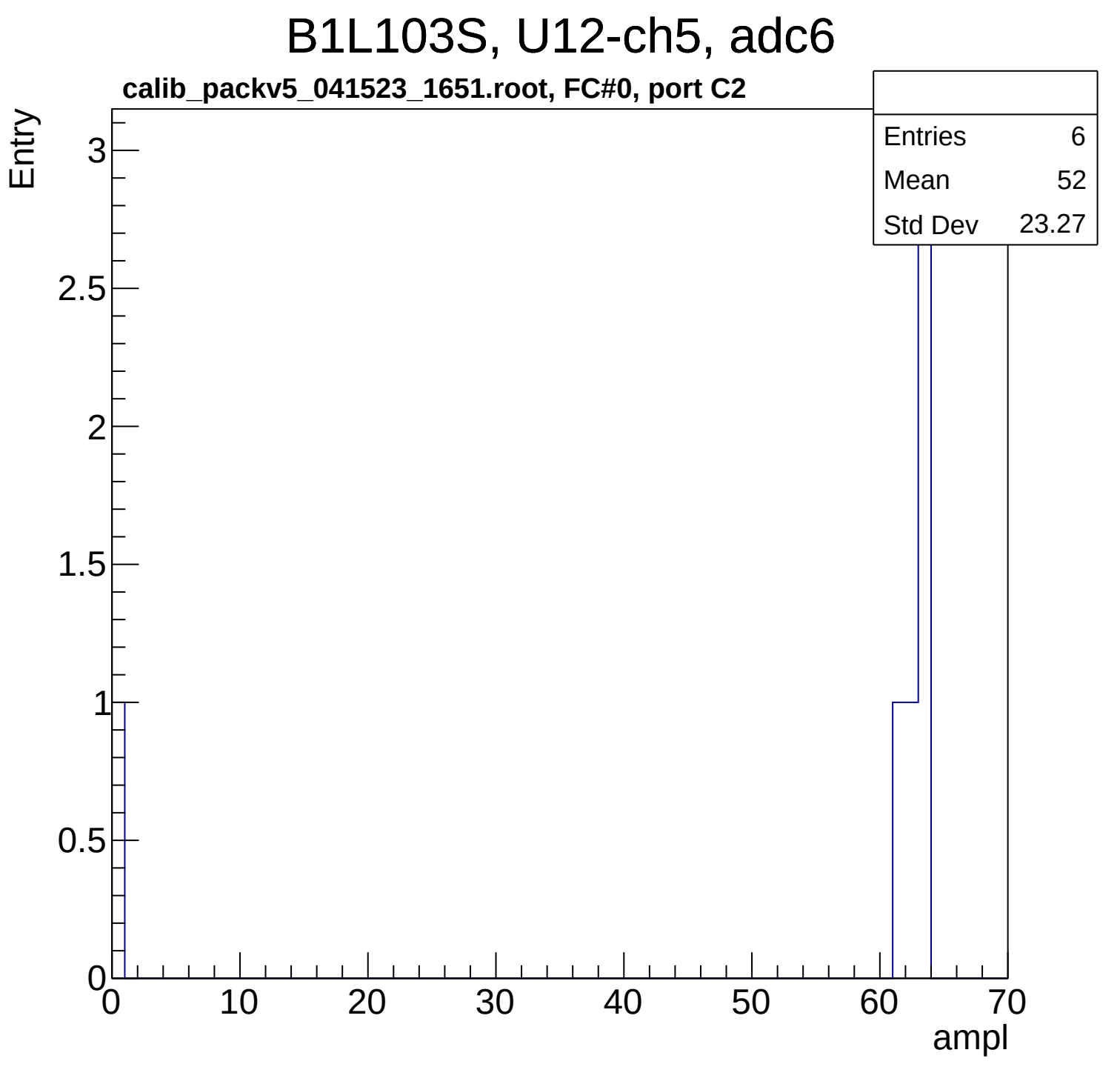
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U12-ch5, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 52
Std Dev 23.27
Entry
ampl
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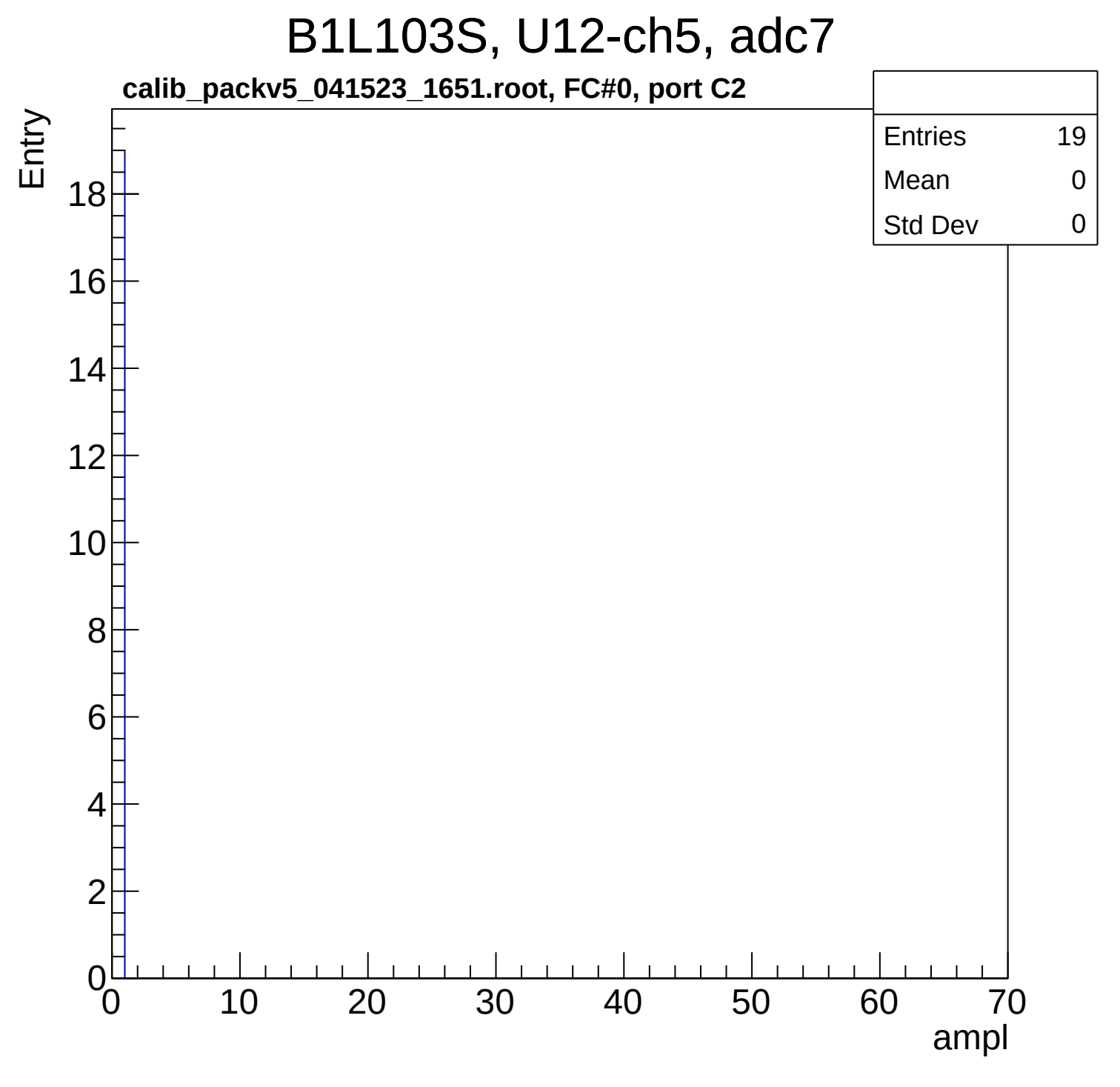
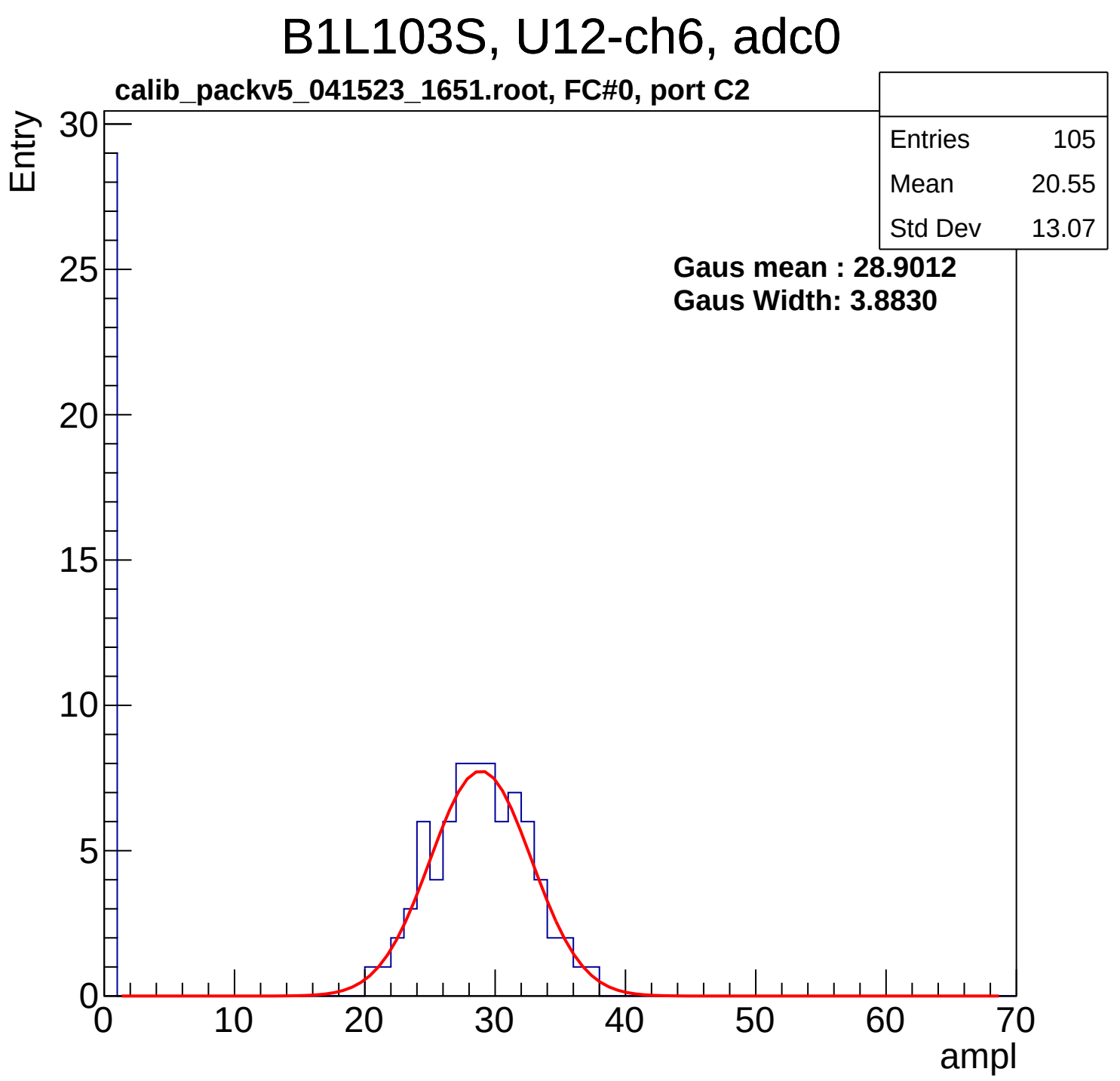
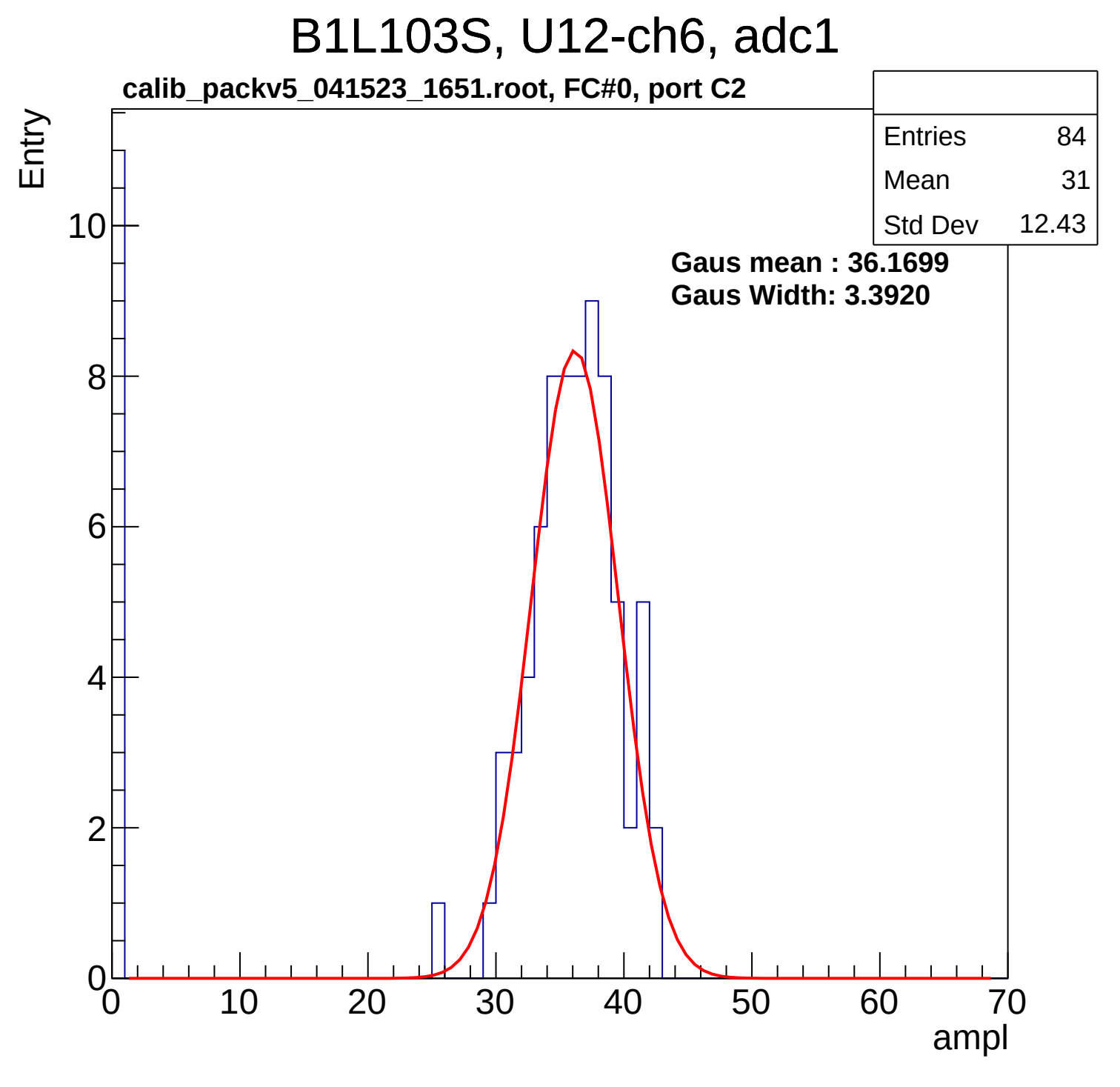
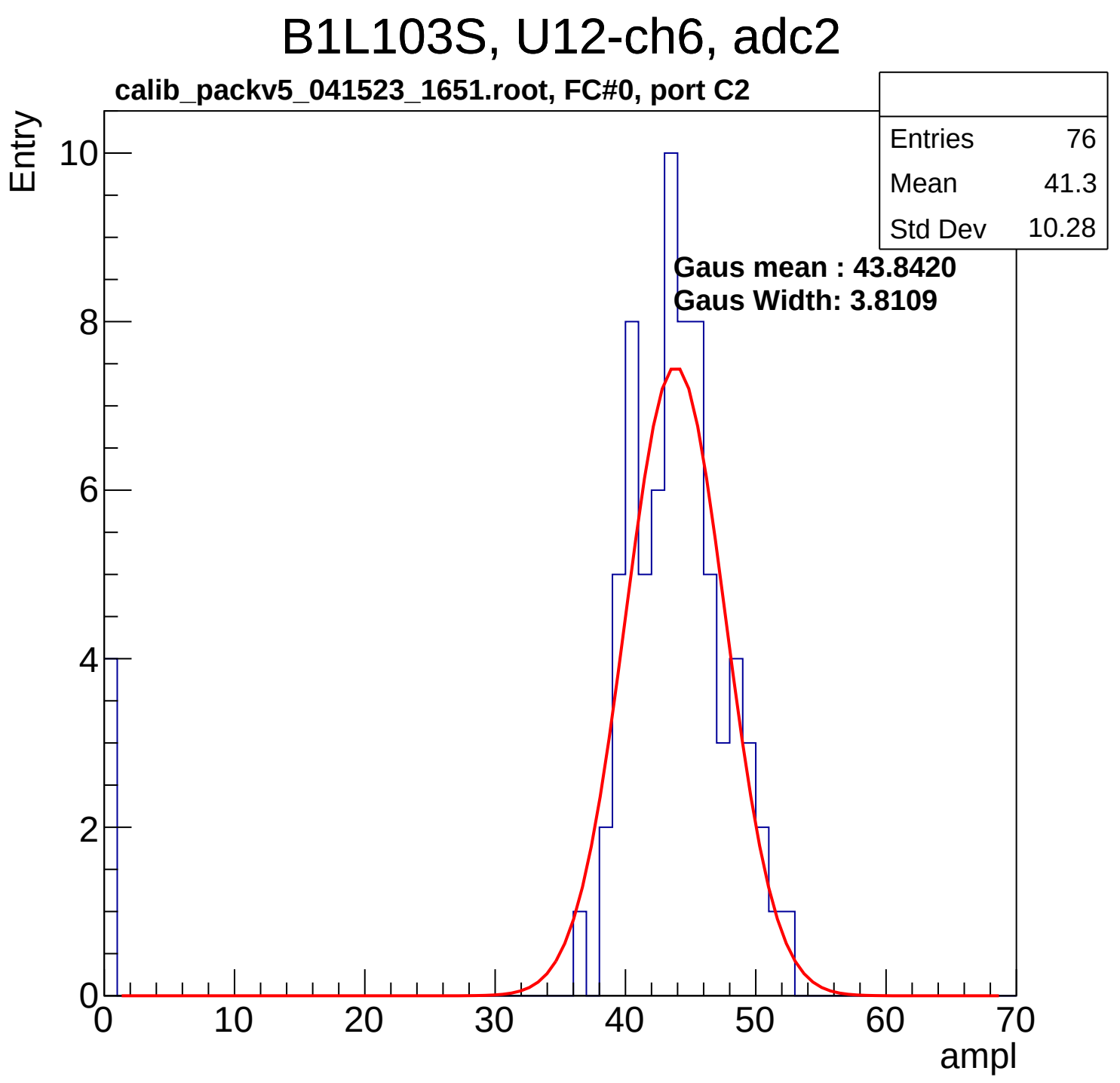
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U12-ch5, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch6, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 105
Mean 20.55
Std Dev 13.07
Gaus mean : 28.9012
Gaus Width: 3.8830
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
70


B1L103S, U12-ch6, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 31
Std Dev 12.43
Gaus mean : 36.1699
Gaus Width: 3.3920
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch6, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 41.3
Std Dev 10.28
Gaus mean : 43.8420
Gaus Width: 3.8109
Entry
ampl
0
2
4
6
8
10
0
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20
30
40
50
60
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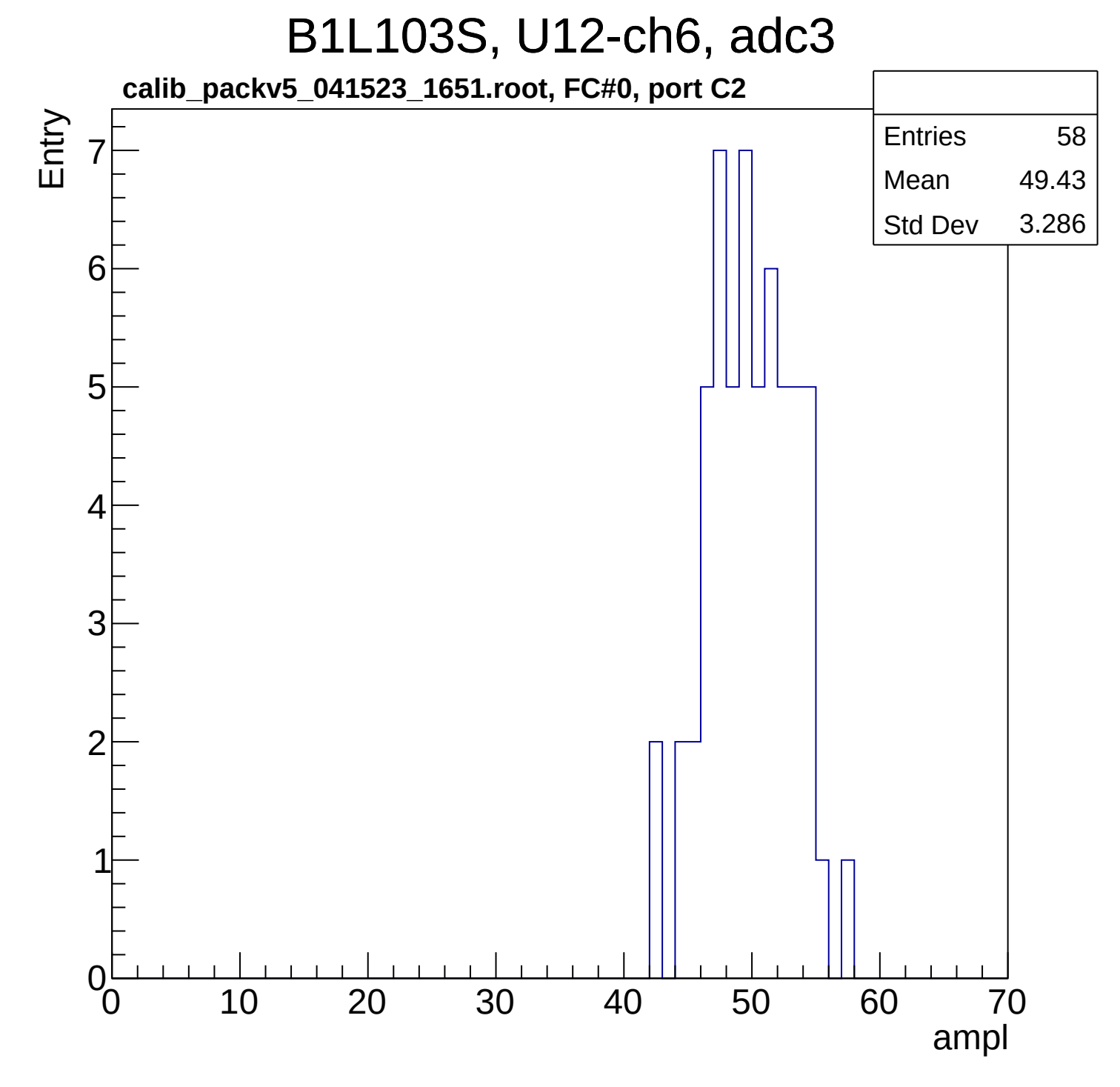
B1L103S, U12-ch6, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 49.43
Std Dev 3.286
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
30
40
50
60
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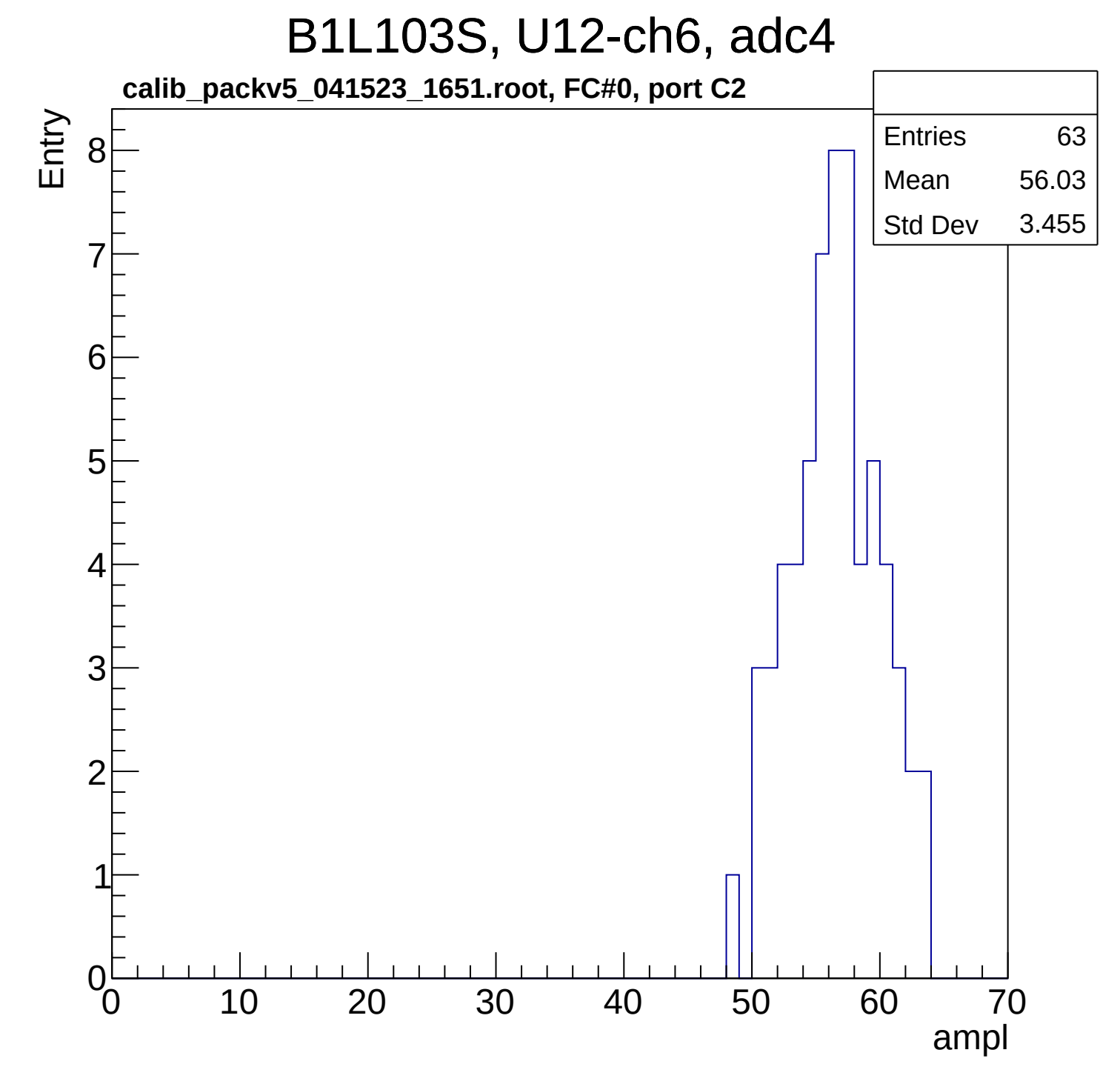
B1L103S, U12-ch6, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 56.03
Std Dev 3.455
Entry
ampl
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2
3
4
5
6
7
8
0
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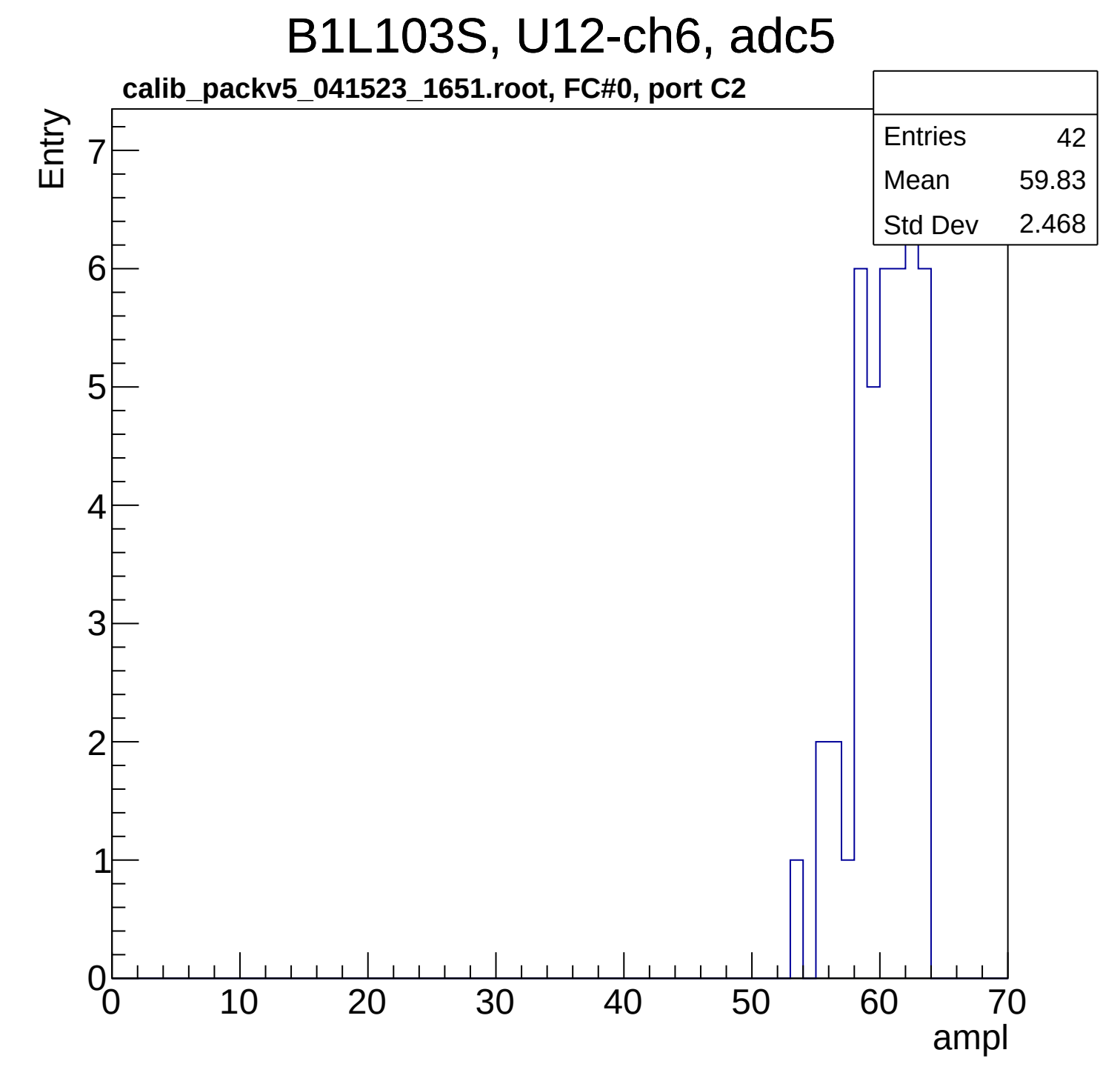
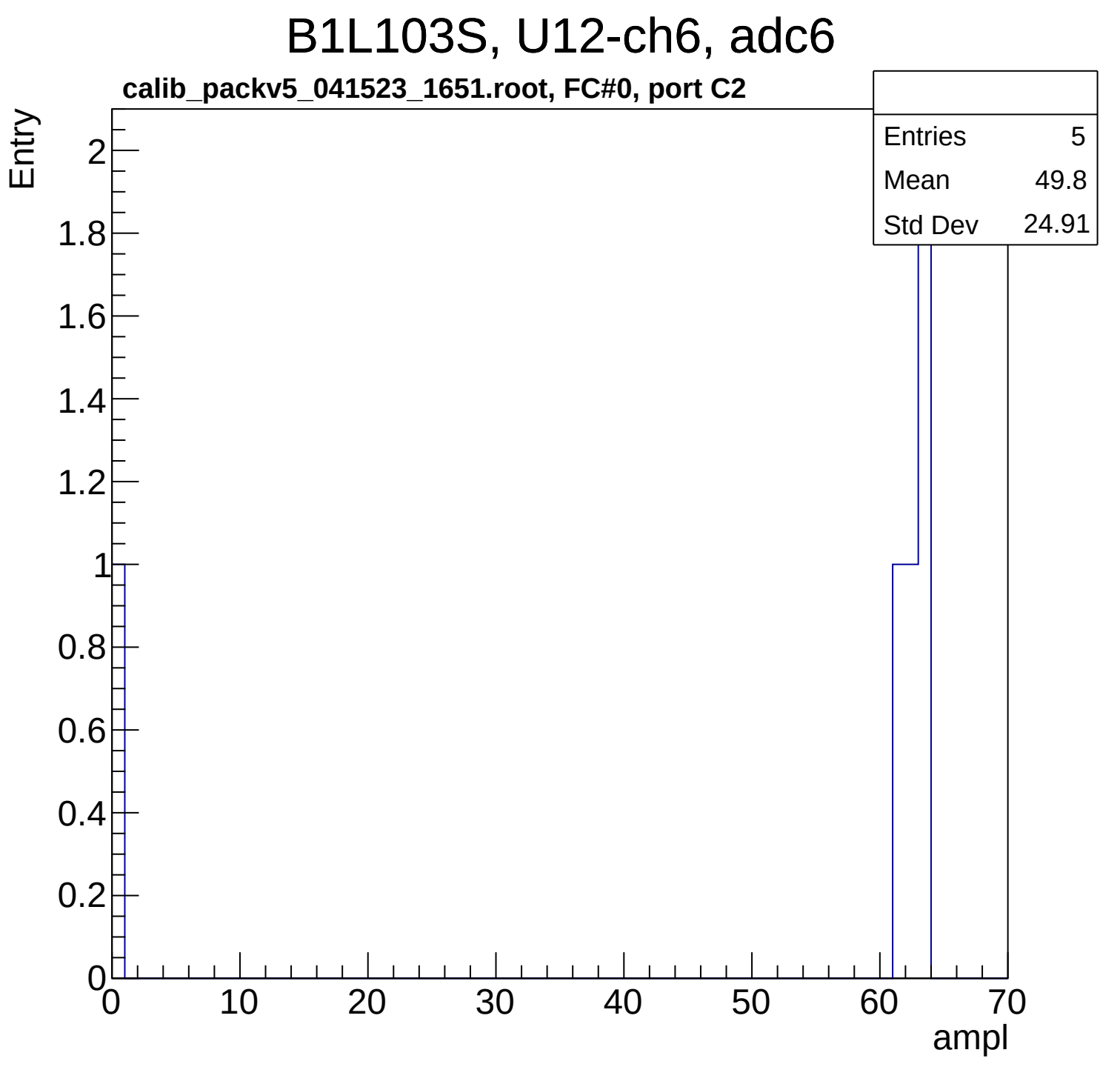
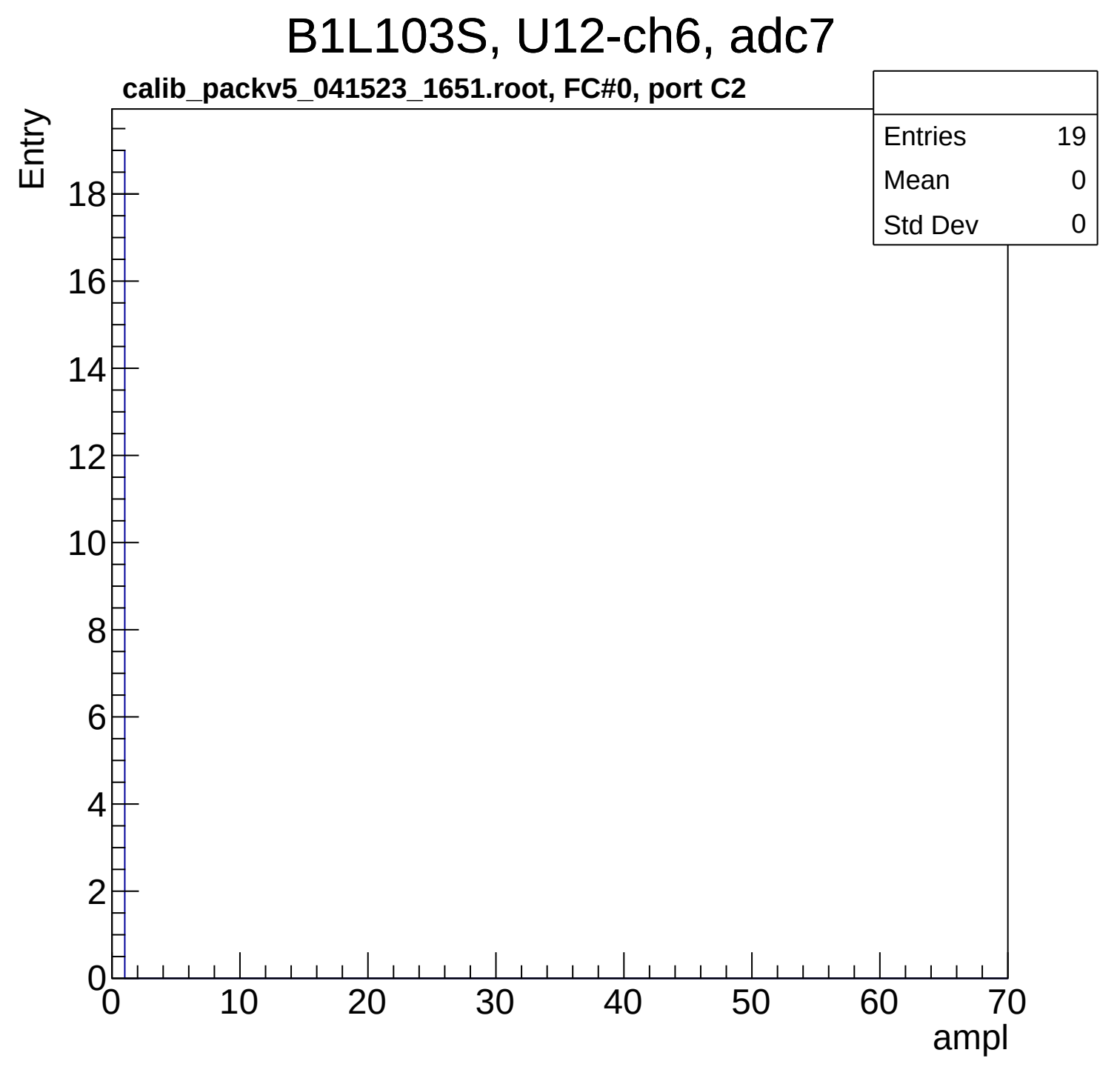
20
30
40
50
60
70


B1L103S, U12-ch6, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 59.83
Std Dev 2.468
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U12-ch6, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 49.8
Std Dev 24.91
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U12-ch6, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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10
20
30
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50
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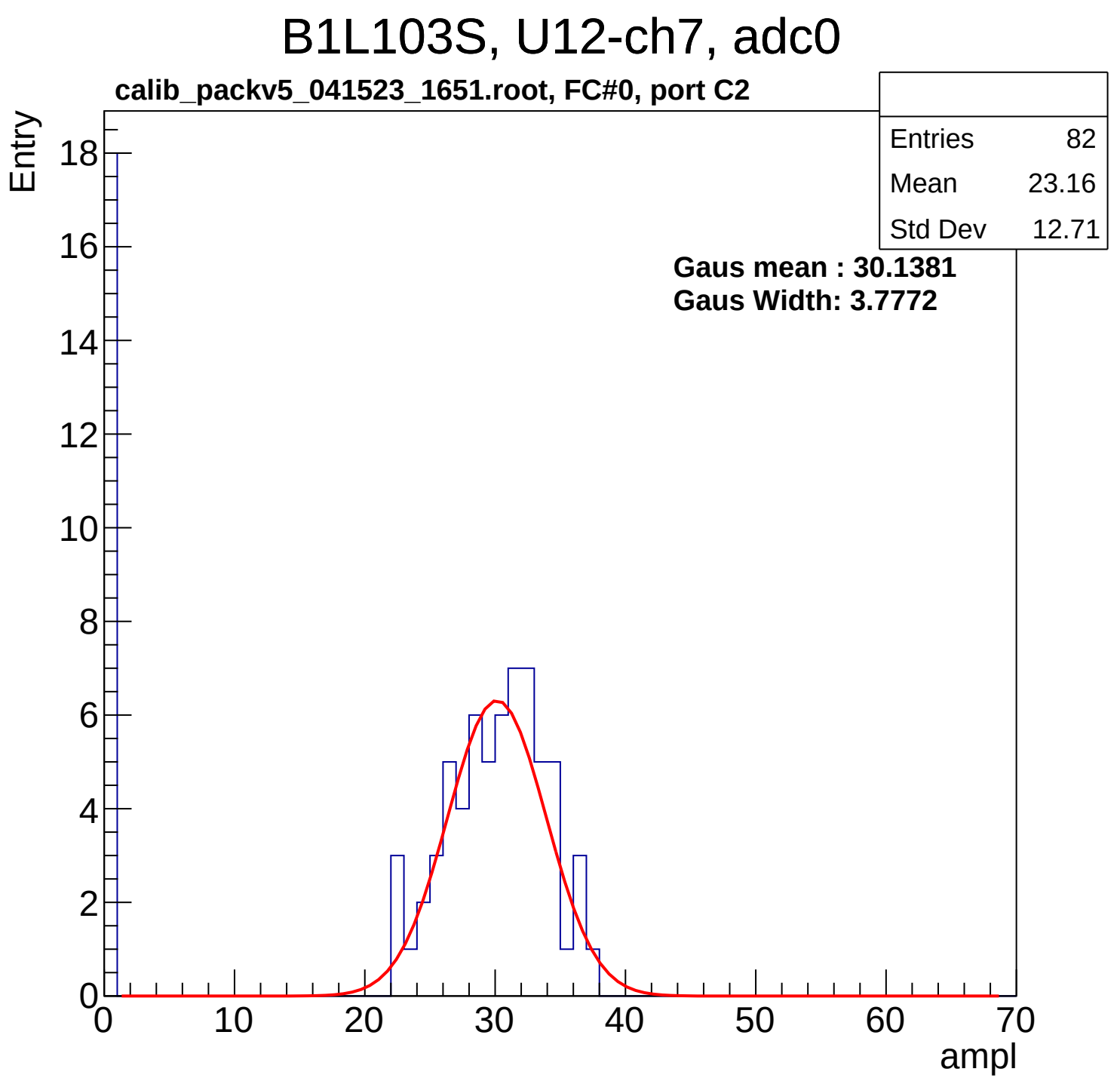
70
ampl


B1L103S, U12-ch7, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 23.16
Std Dev 12.71
Gaus mean : 30.1381
Gaus Width: 3.7772
Entry
ampl
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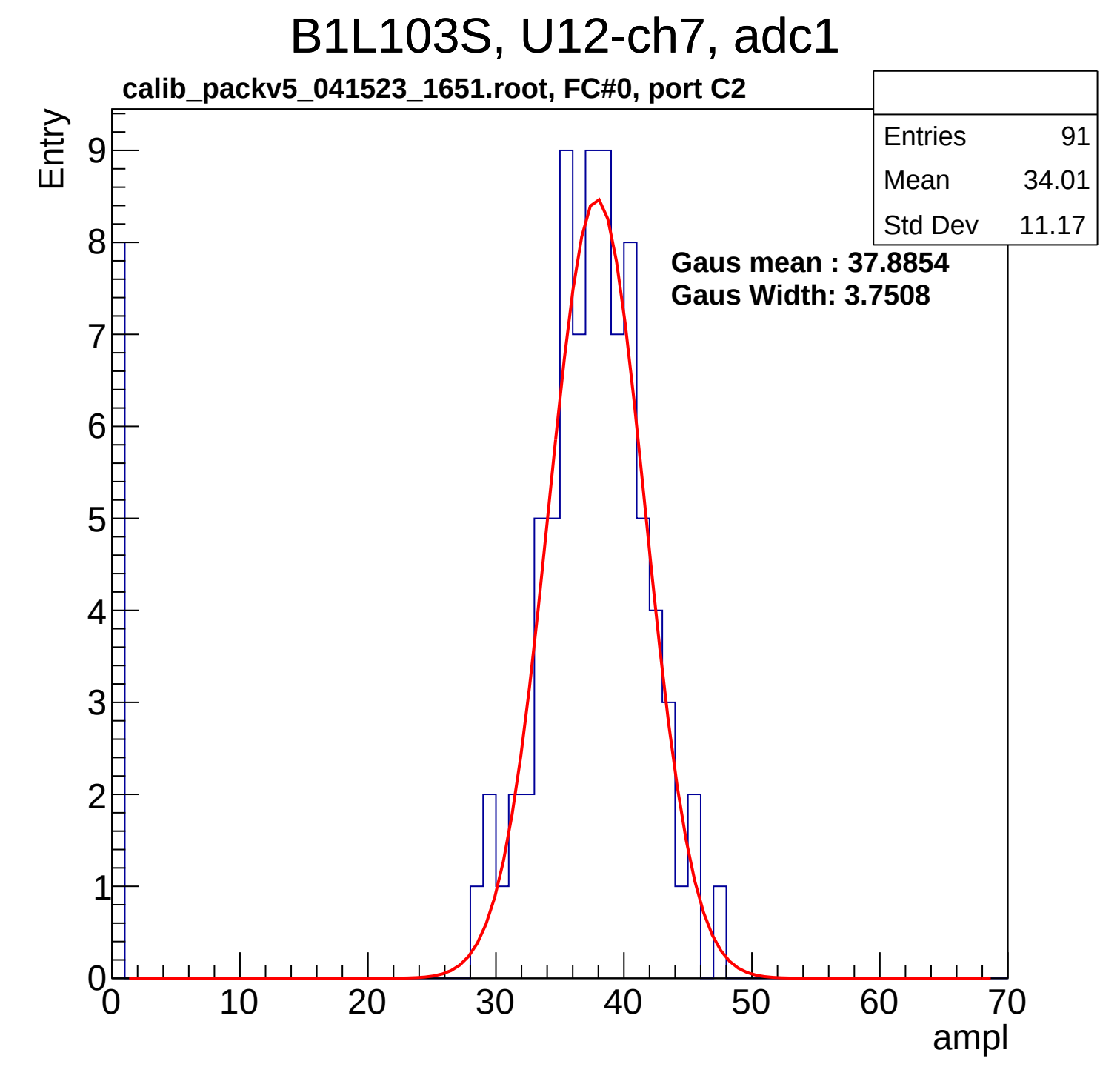
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L103S, U12-ch7, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 34.01
Std Dev 11.17
Gaus mean : 37.8854
Gaus Width: 3.7508
Entry
ampl
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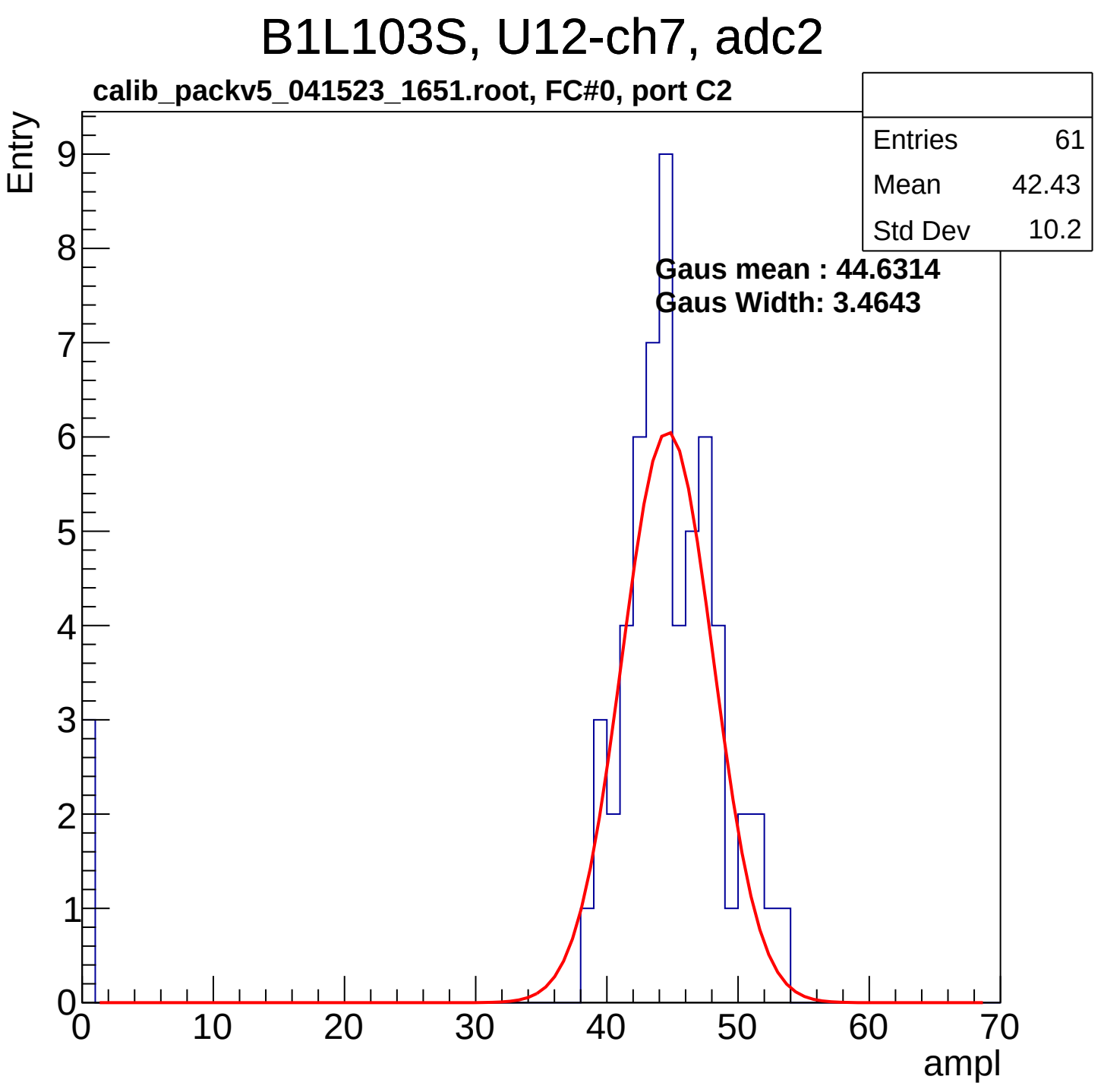
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch7, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 42.43
Std Dev 10.2
Gaus mean : 44.6314
Gaus Width: 3.4643
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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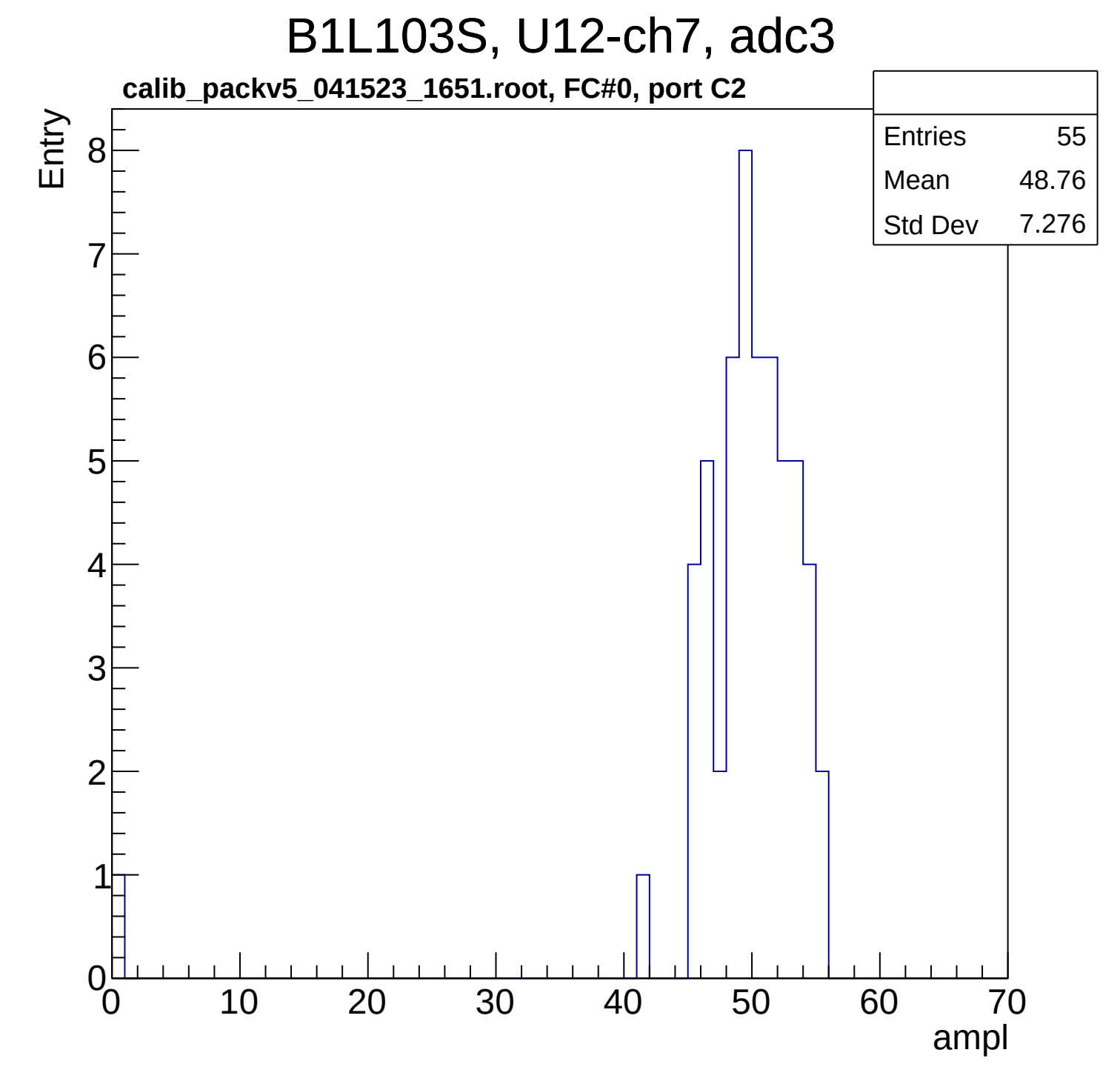
B1L103S, U12-ch7, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 48.76
Std Dev 7.276
Entry
ampl
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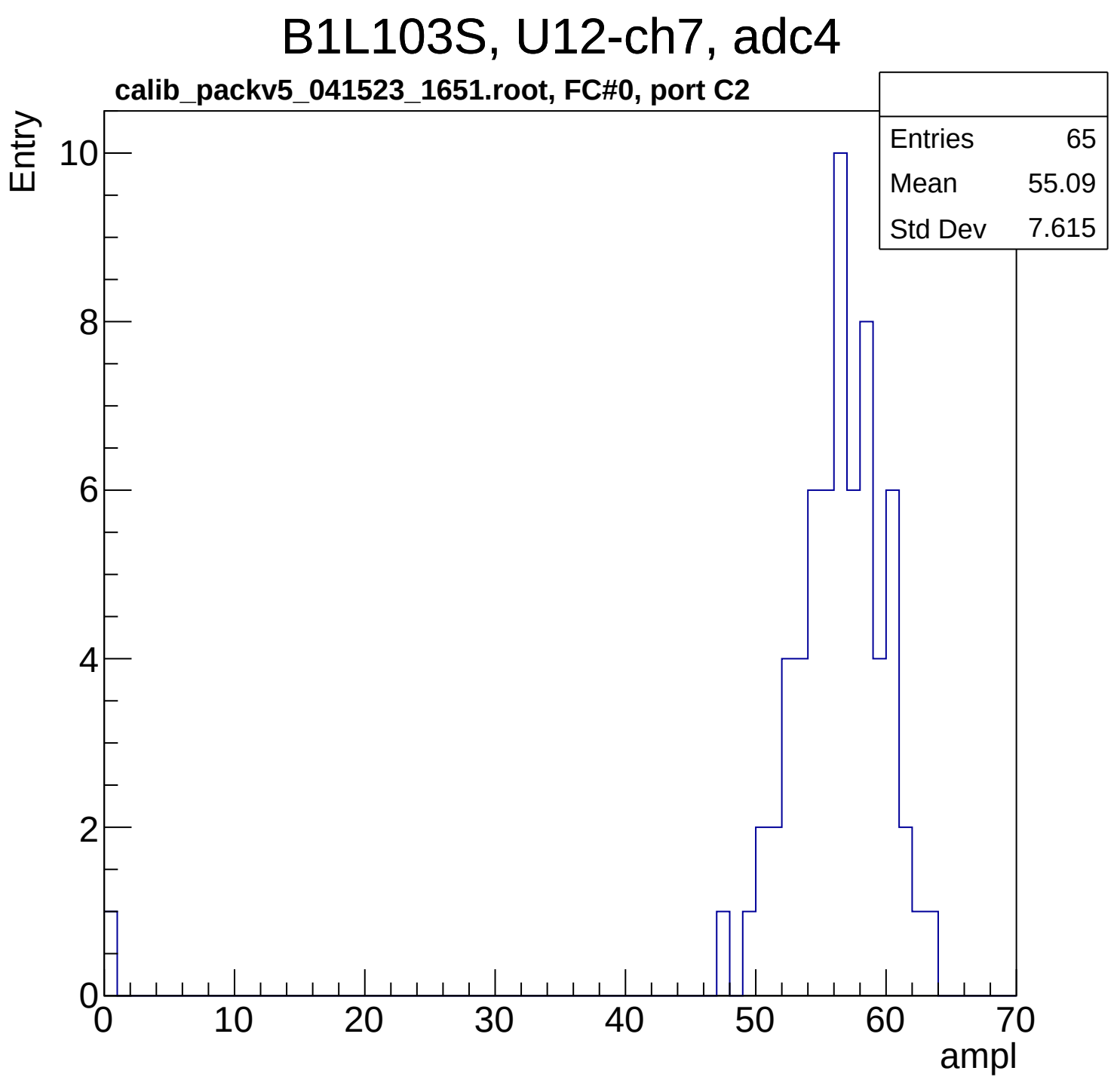
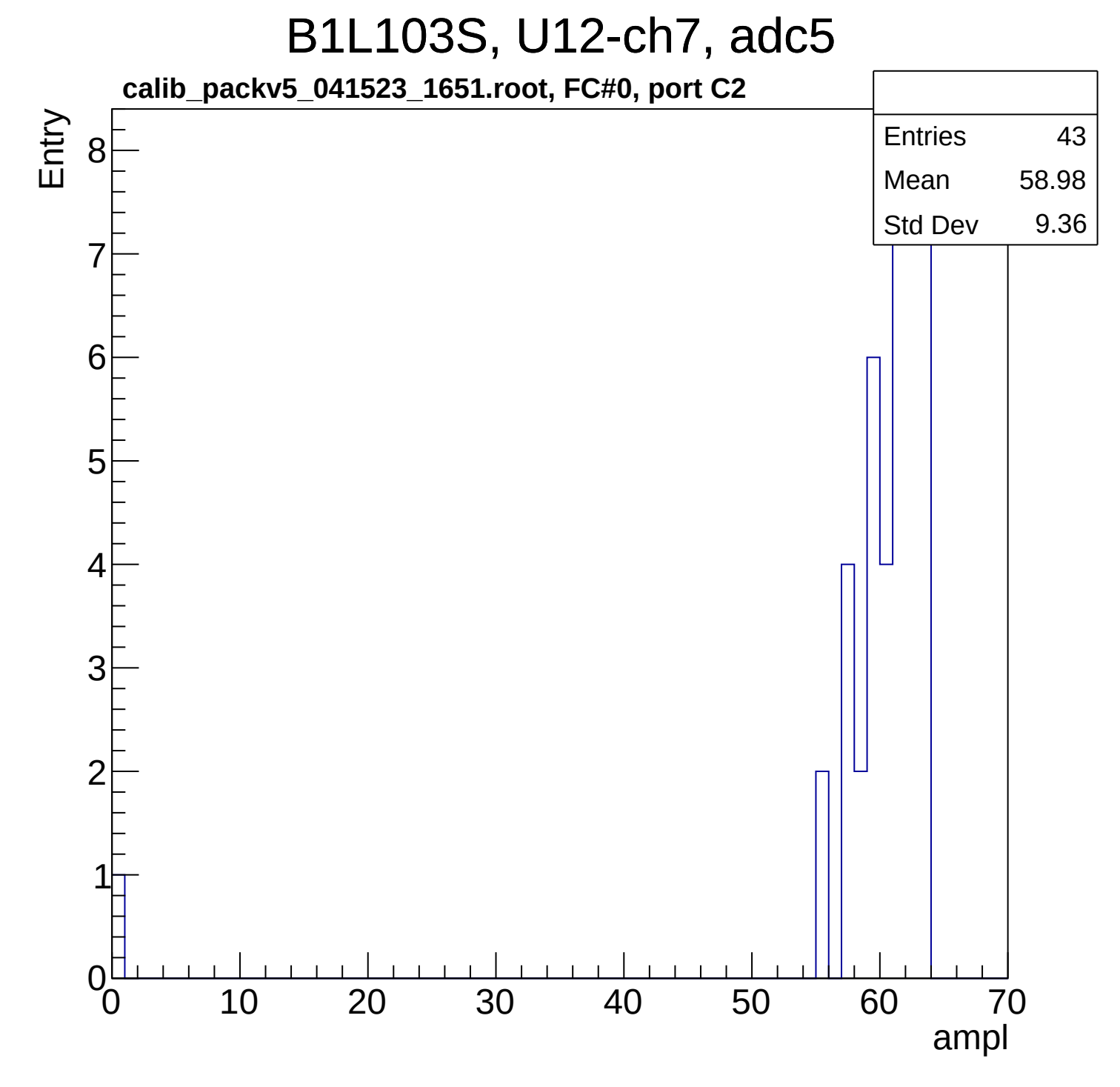
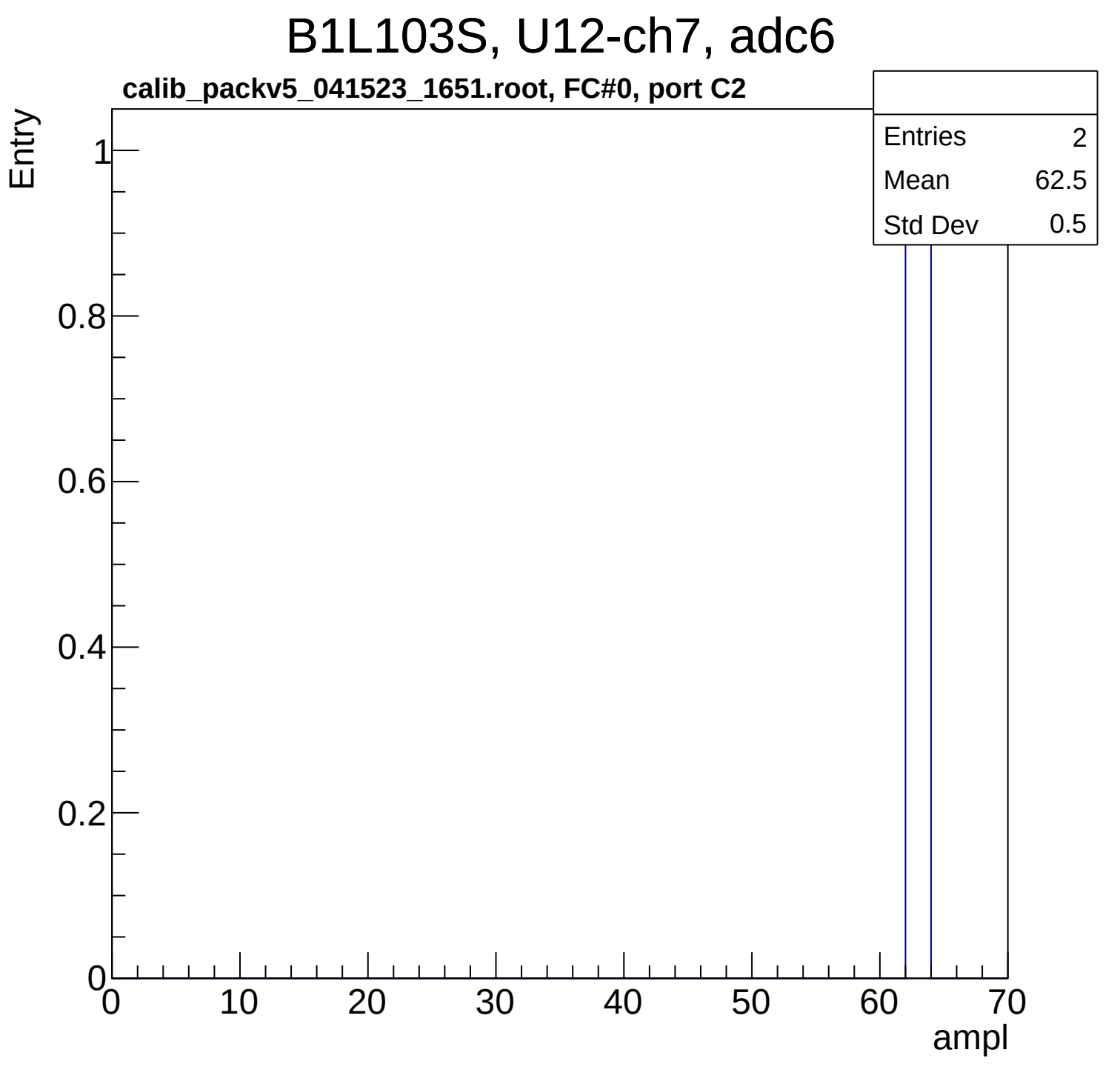
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U12-ch7, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 55.09
Std Dev 7.615
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch7, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 58.98
Std Dev 9.36
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U12-ch7, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
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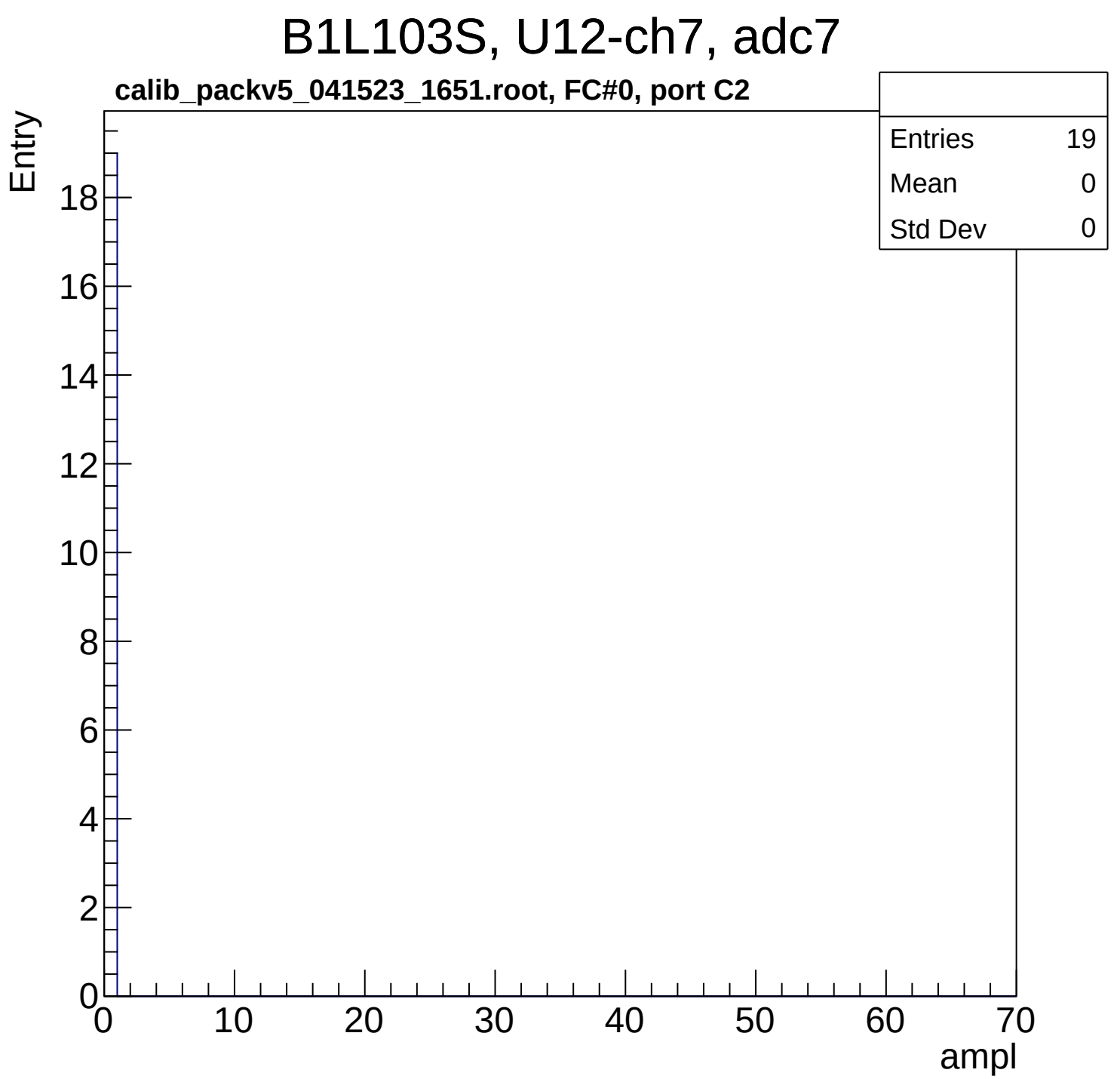
ampl


B1L103S, U12-ch7, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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6
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10
12
14
16
18
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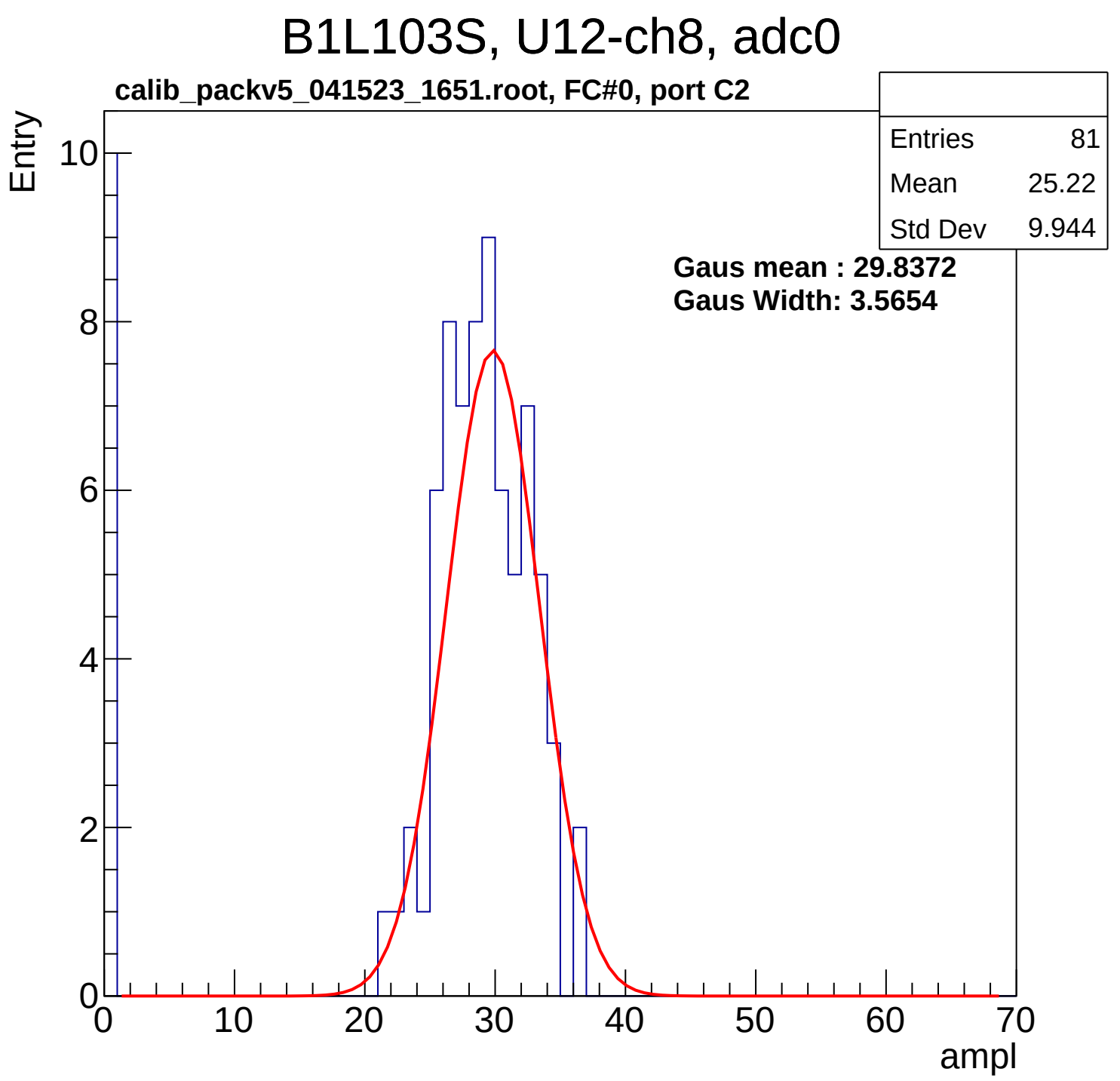
50
60
70
ampl


B1L103S, U12-ch8, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 25.22
Std Dev 9.944
Gaus mean : 29.8372
Gaus Width: 3.5654
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
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60
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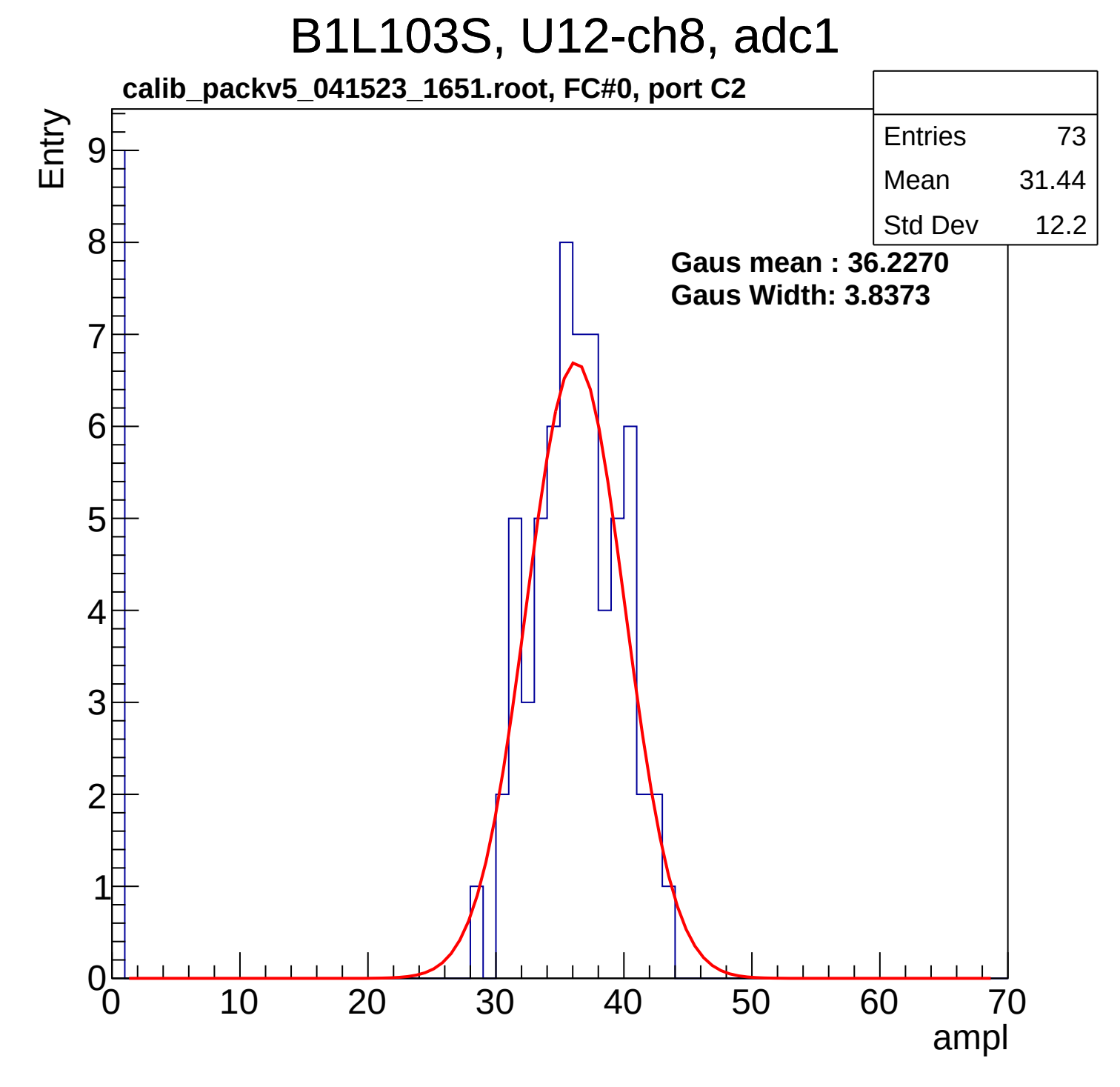
B1L103S, U12-ch8, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 31.44
Std Dev 12.2
Gaus mean : 36.2270
Gaus Width: 3.8373
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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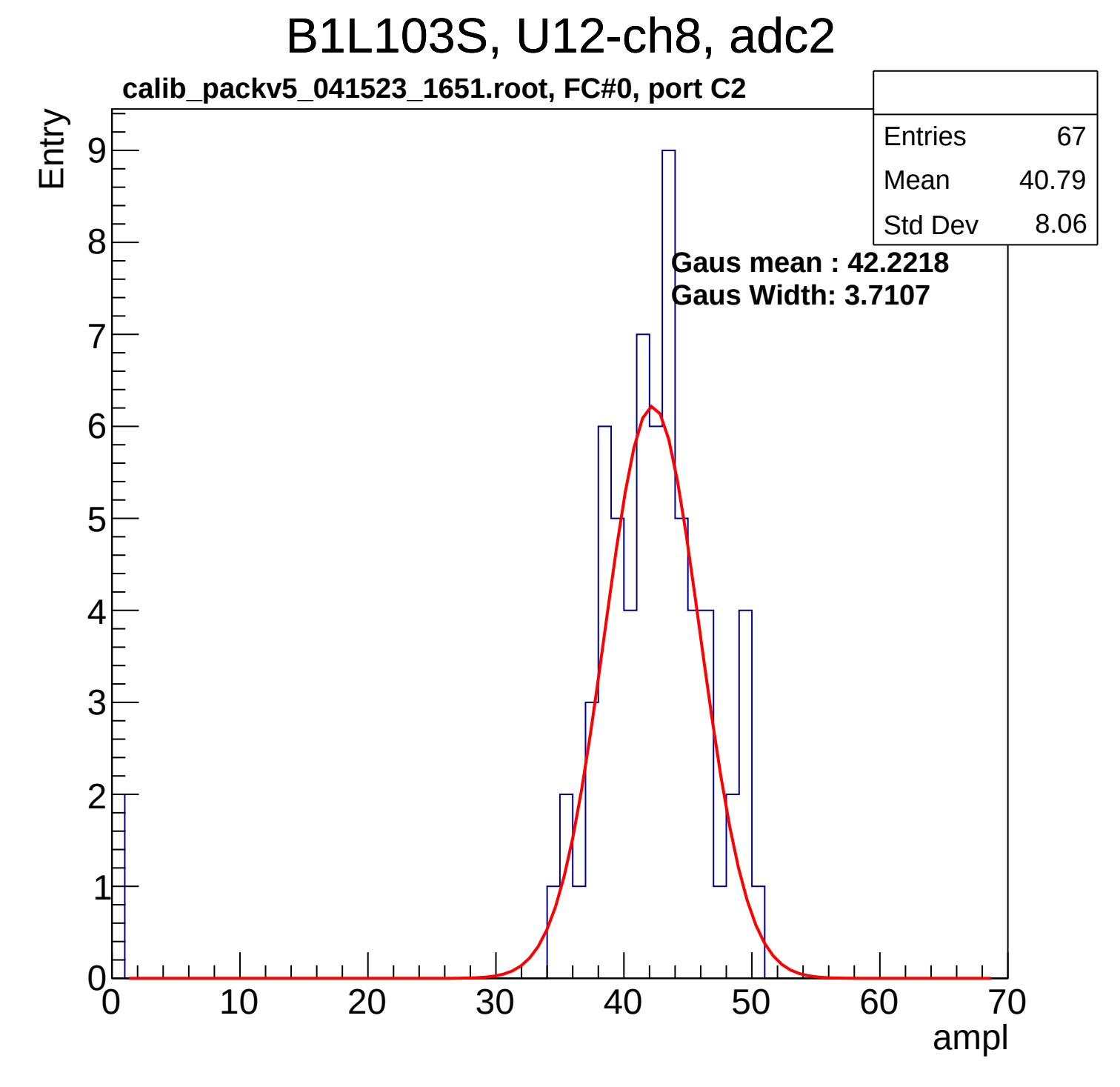
B1L103S, U12-ch8, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 40.79
Std Dev 8.06
Gaus mean : 42.2218
Gaus Width: 3.7107
Entry
ampl
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1
2
3
4
5
6
7
8
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0
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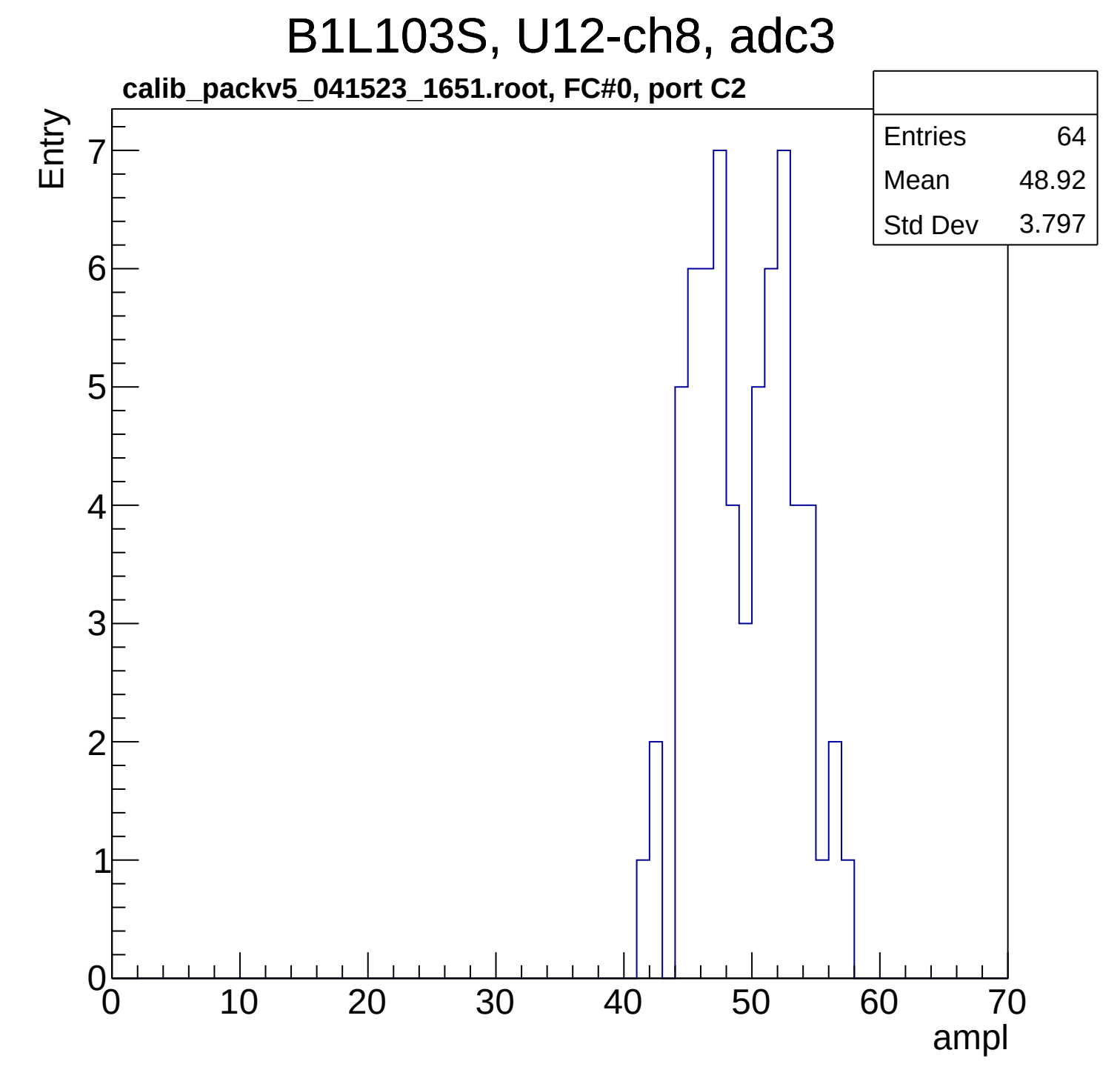
B1L103S, U12-ch8, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 48.92
Std Dev 3.797
Entry
ampl
0
1
2
3
4
5
6
7
0
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60
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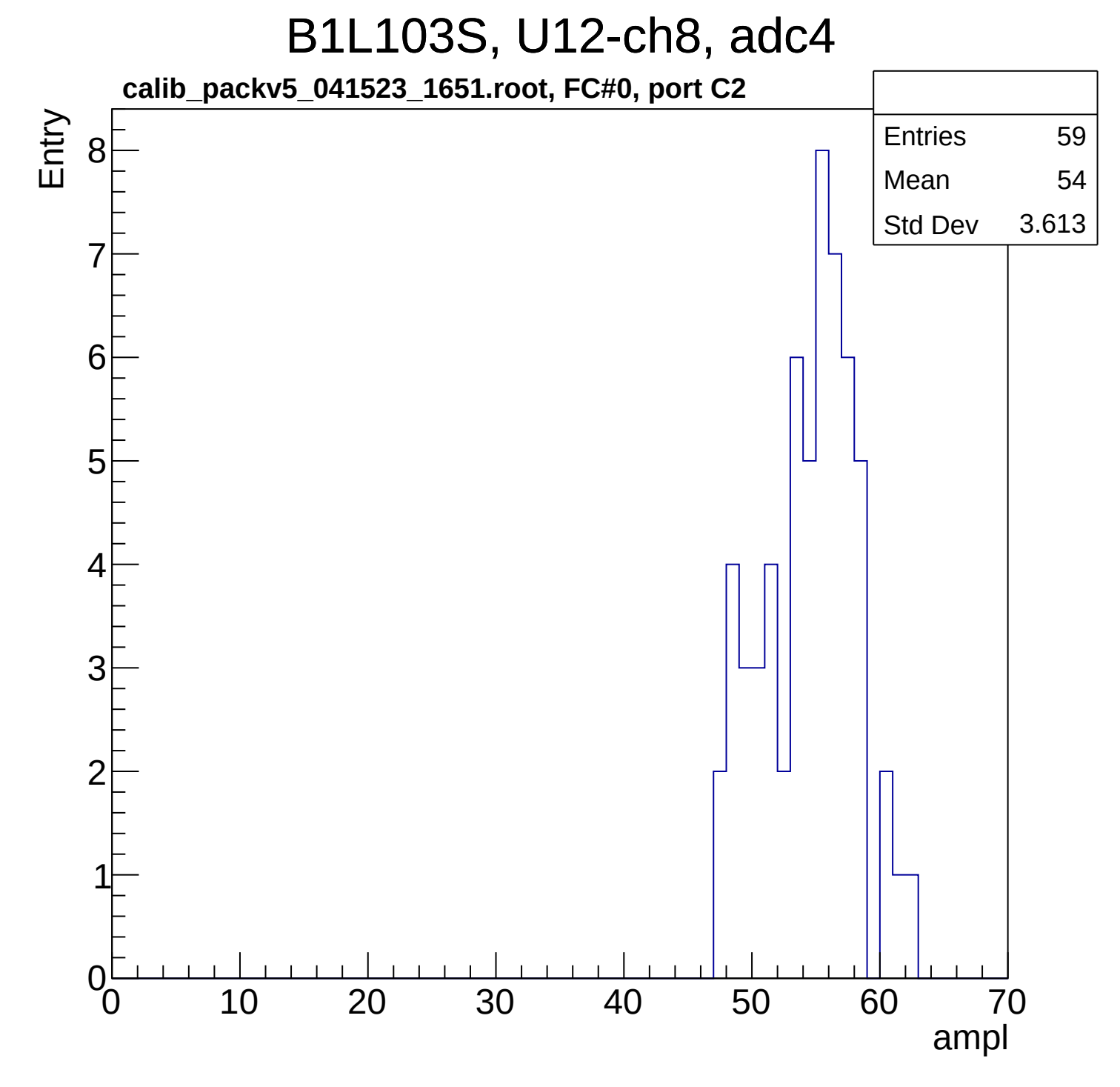
B1L103S, U12-ch8, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54
Std Dev 3.613
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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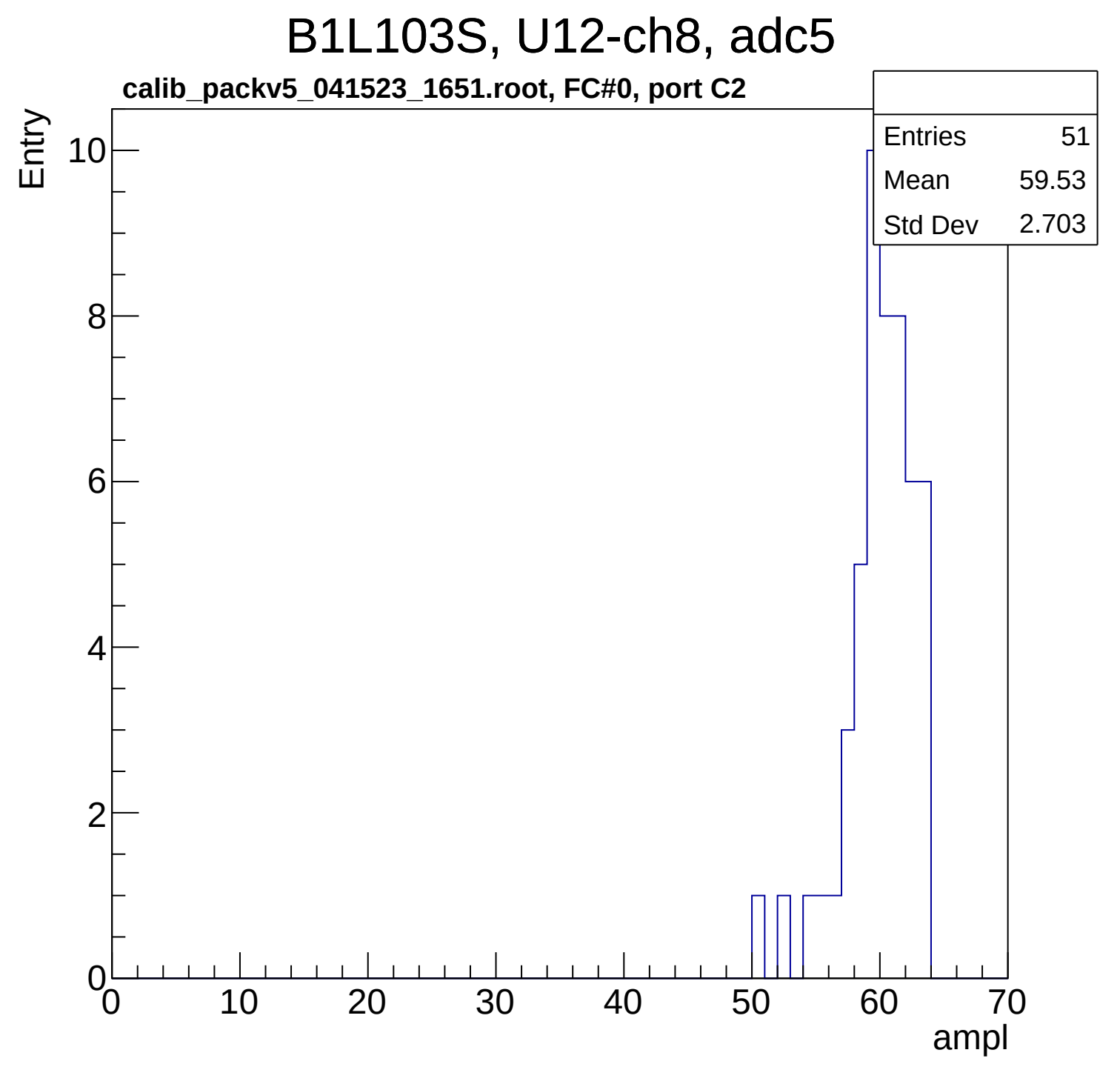
B1L103S, U12-ch8, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 59.53
Std Dev 2.703
Entry
ampl
0
2
4
6
8
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0
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20
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40
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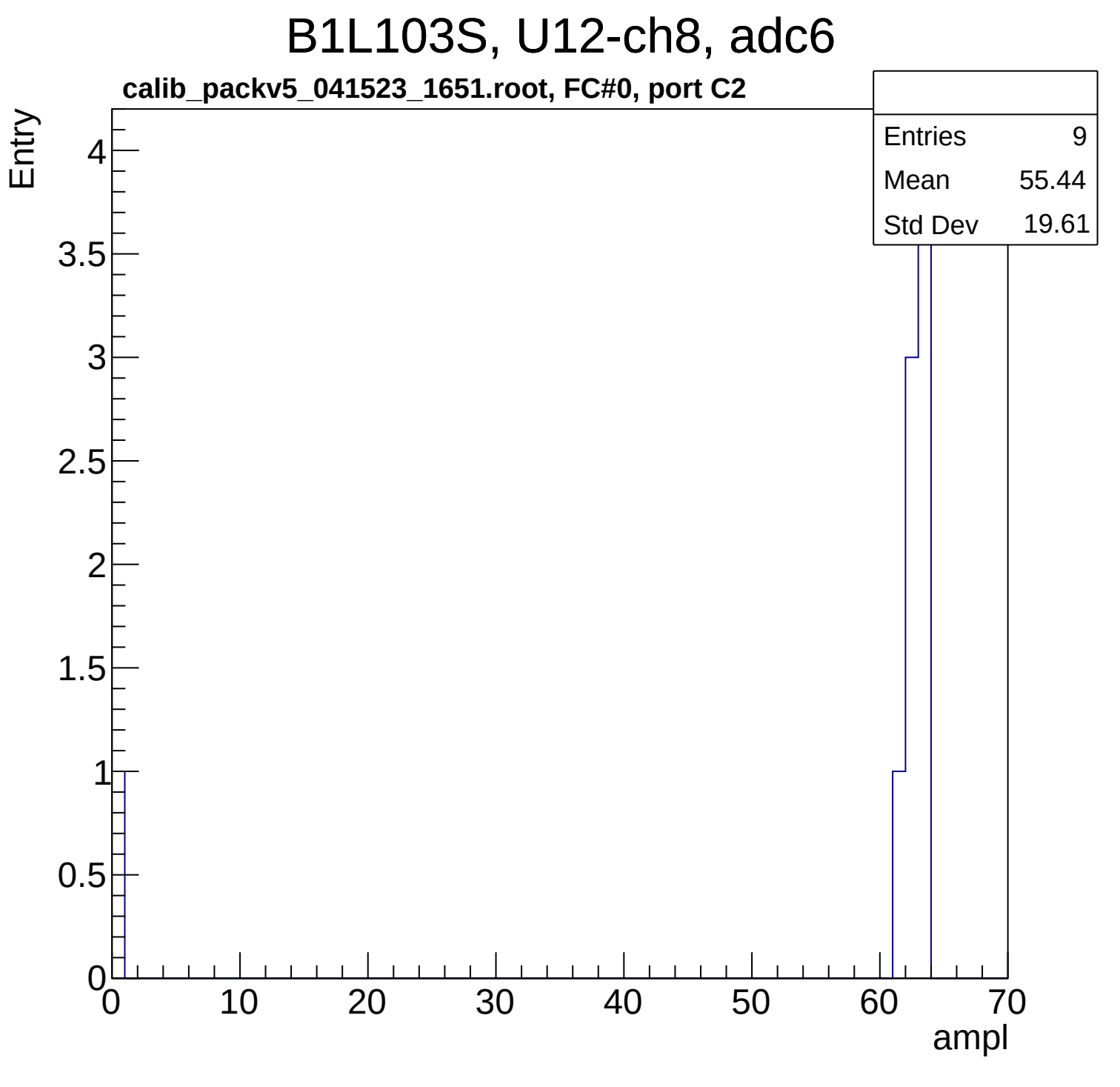
B1L103S, U12-ch8, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 55.44
Std Dev 19.61
Entry
ampl
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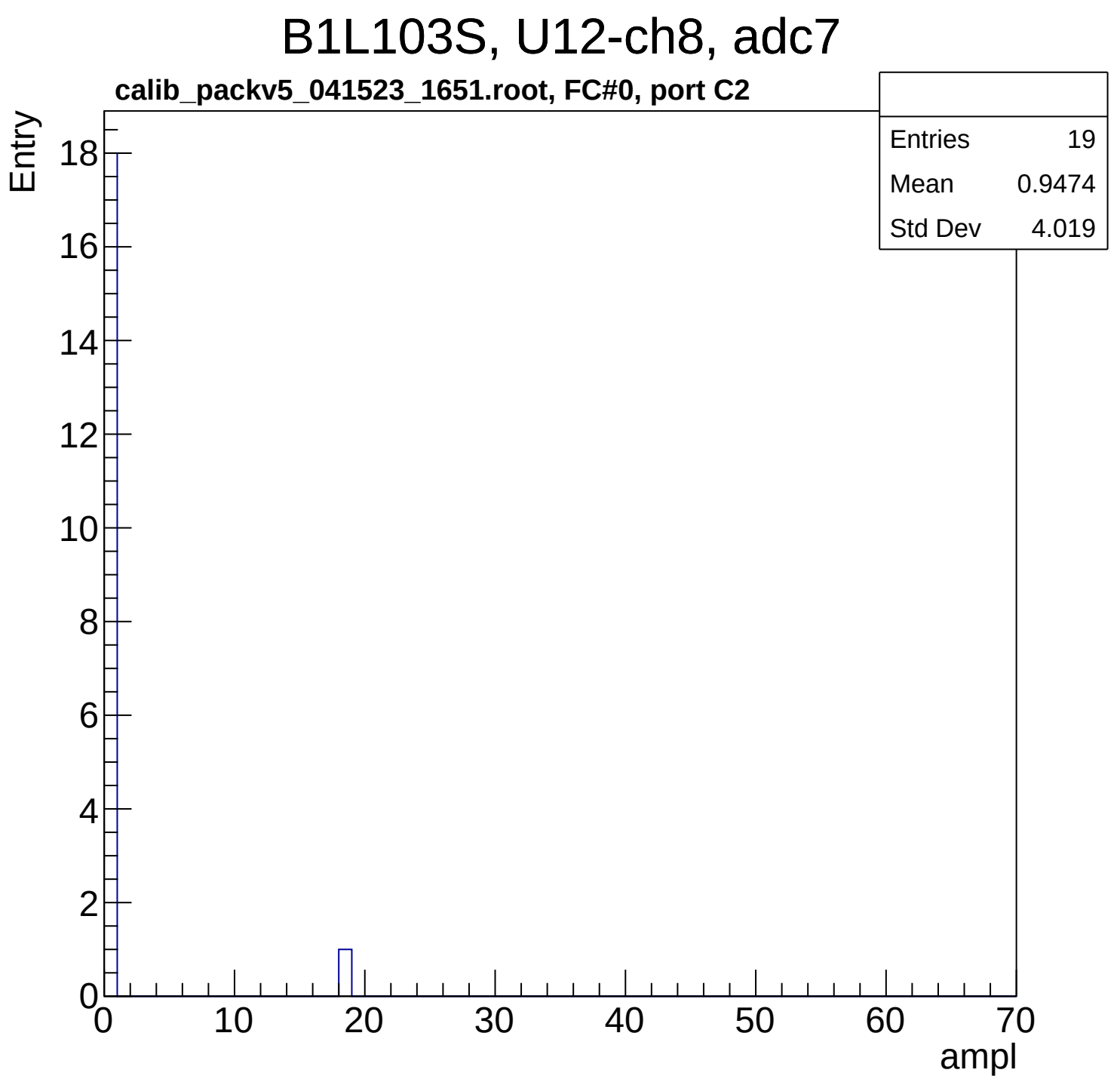
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U12-ch8, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0.9474
Std Dev 4.019
Entry
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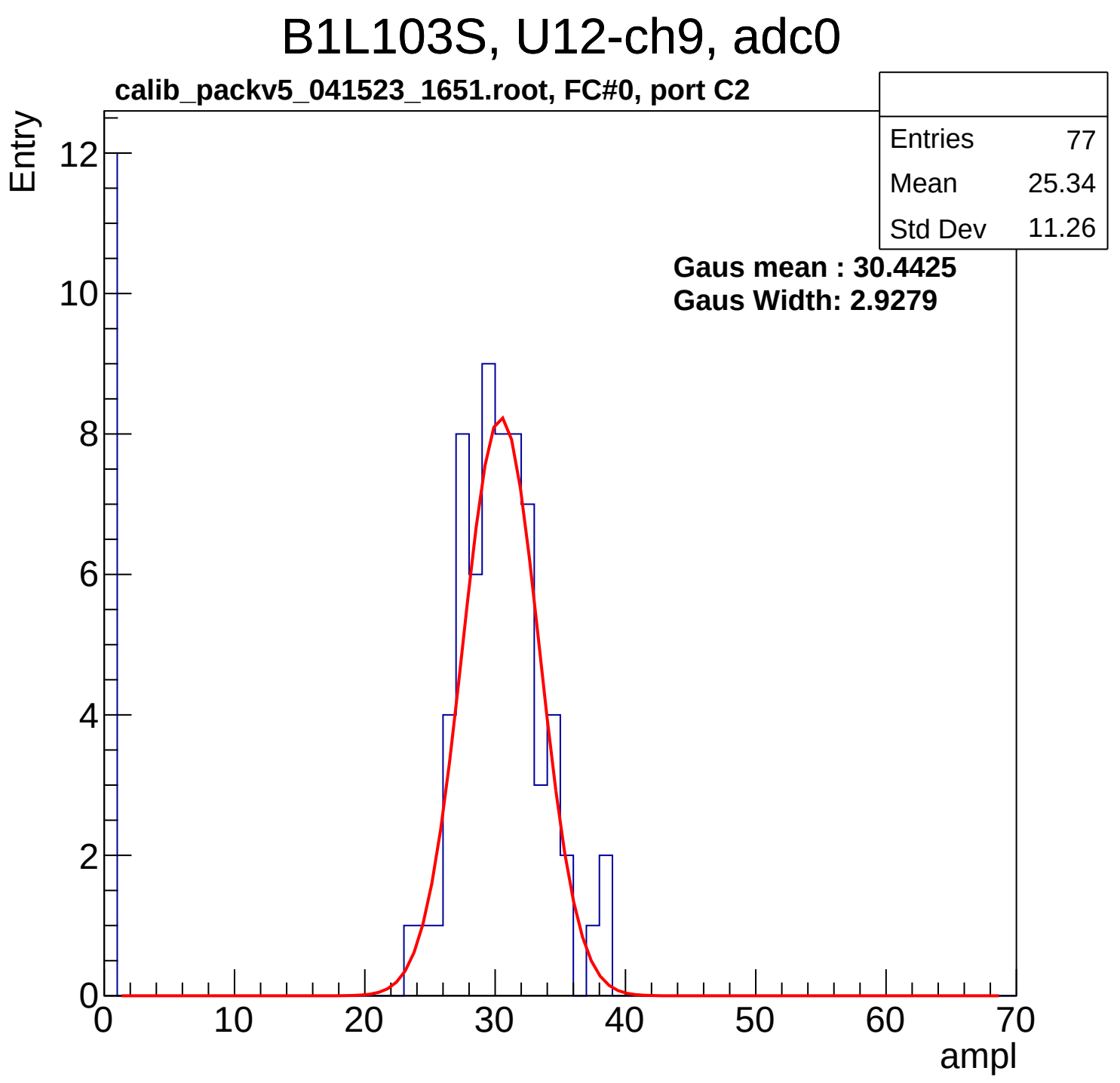
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch9, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 25.34
Std Dev 11.26
Gaus mean : 30.4425
Gaus Width: 2.9279
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
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60
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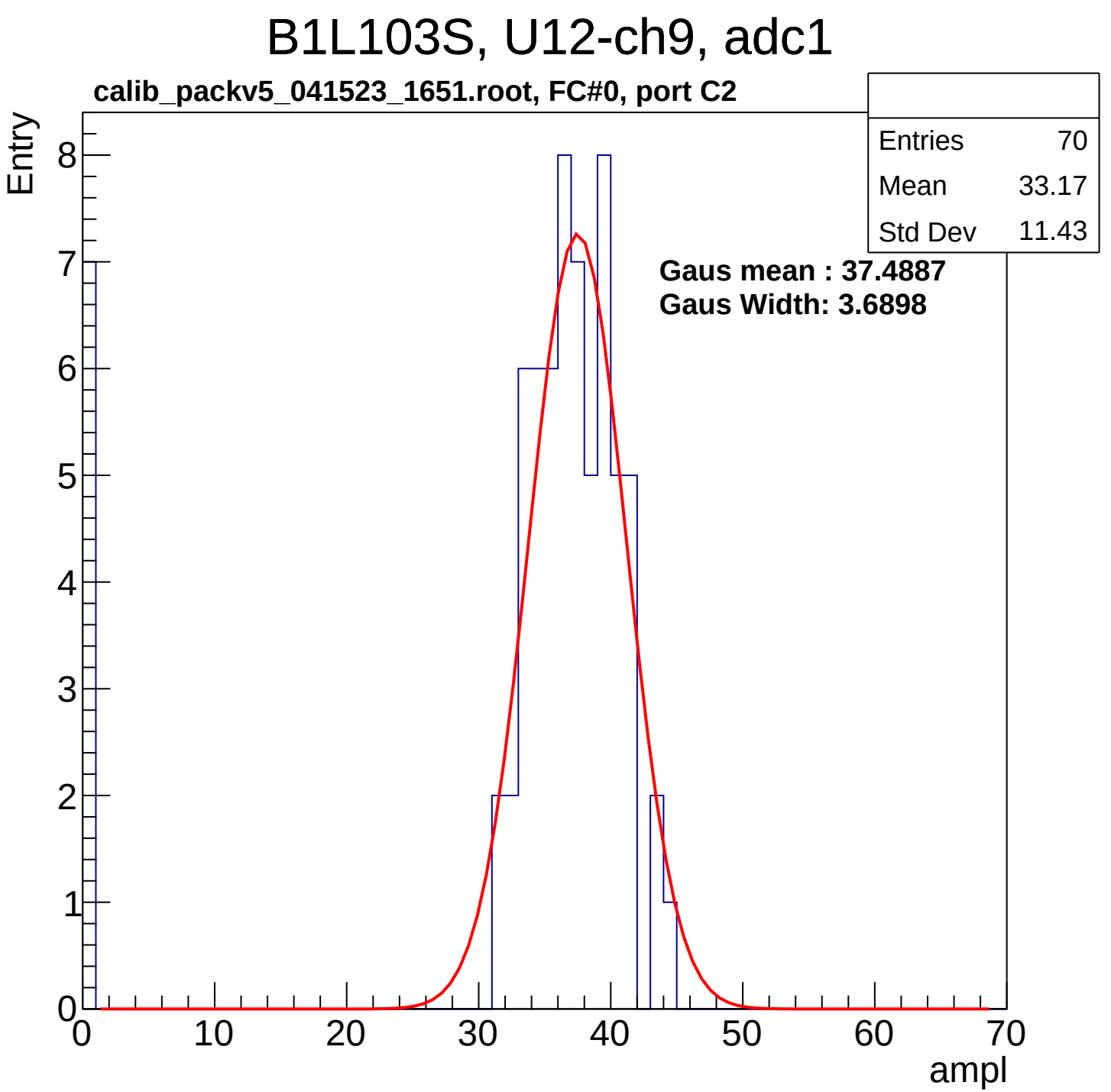
B1L103S, U12-ch9, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 33.17
Std Dev 11.43
Gaus mean : 37.4887
Gaus Width: 3.6898
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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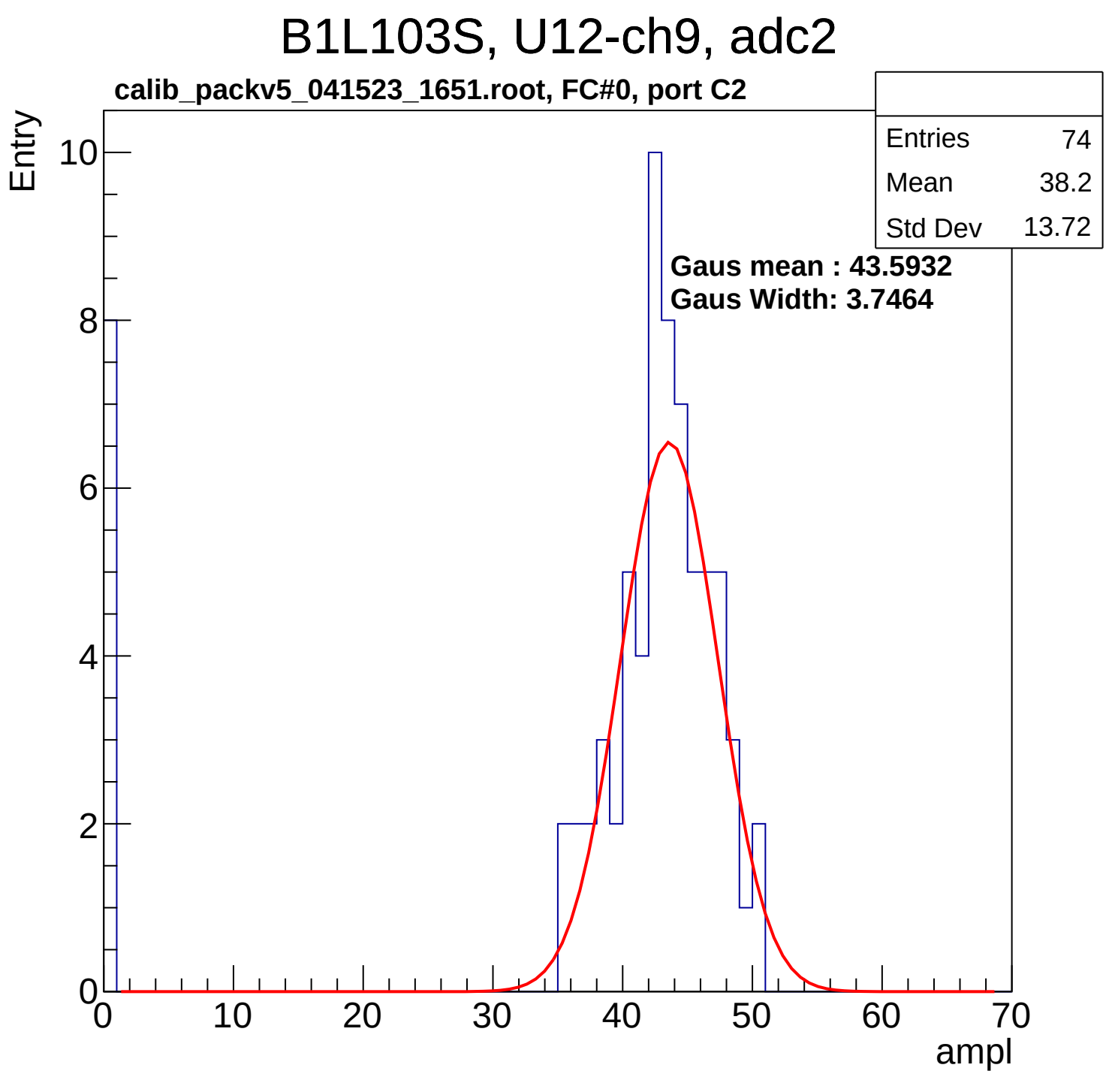
B1L103S, U12-ch9, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 38.2
Std Dev 13.72
Gaus mean : 43.5932
Gaus Width: 3.7464
Entry
ampl
0
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4
6
8
10
0
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20
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60
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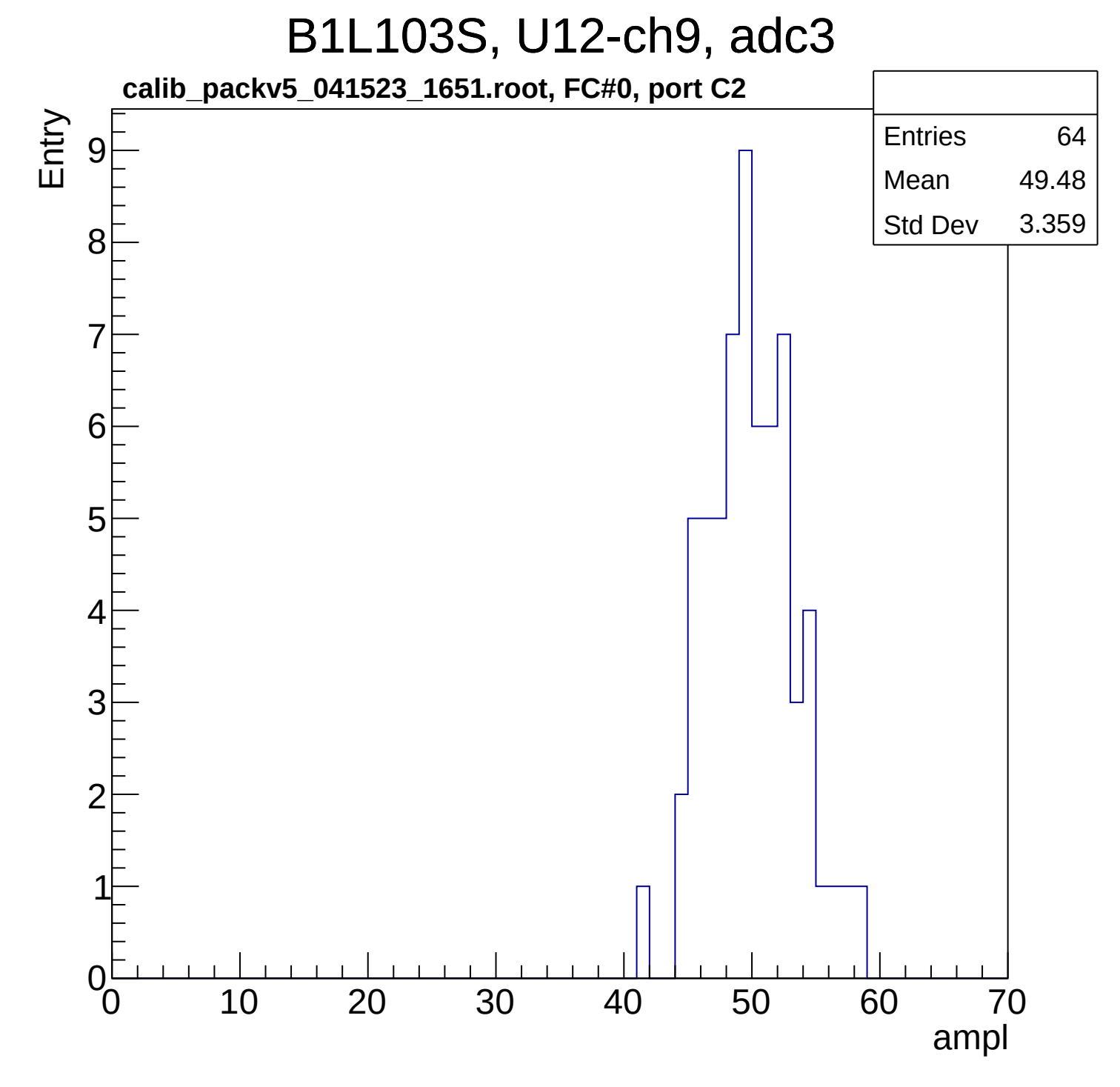
B1L103S, U12-ch9, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 49.48
Std Dev 3.359
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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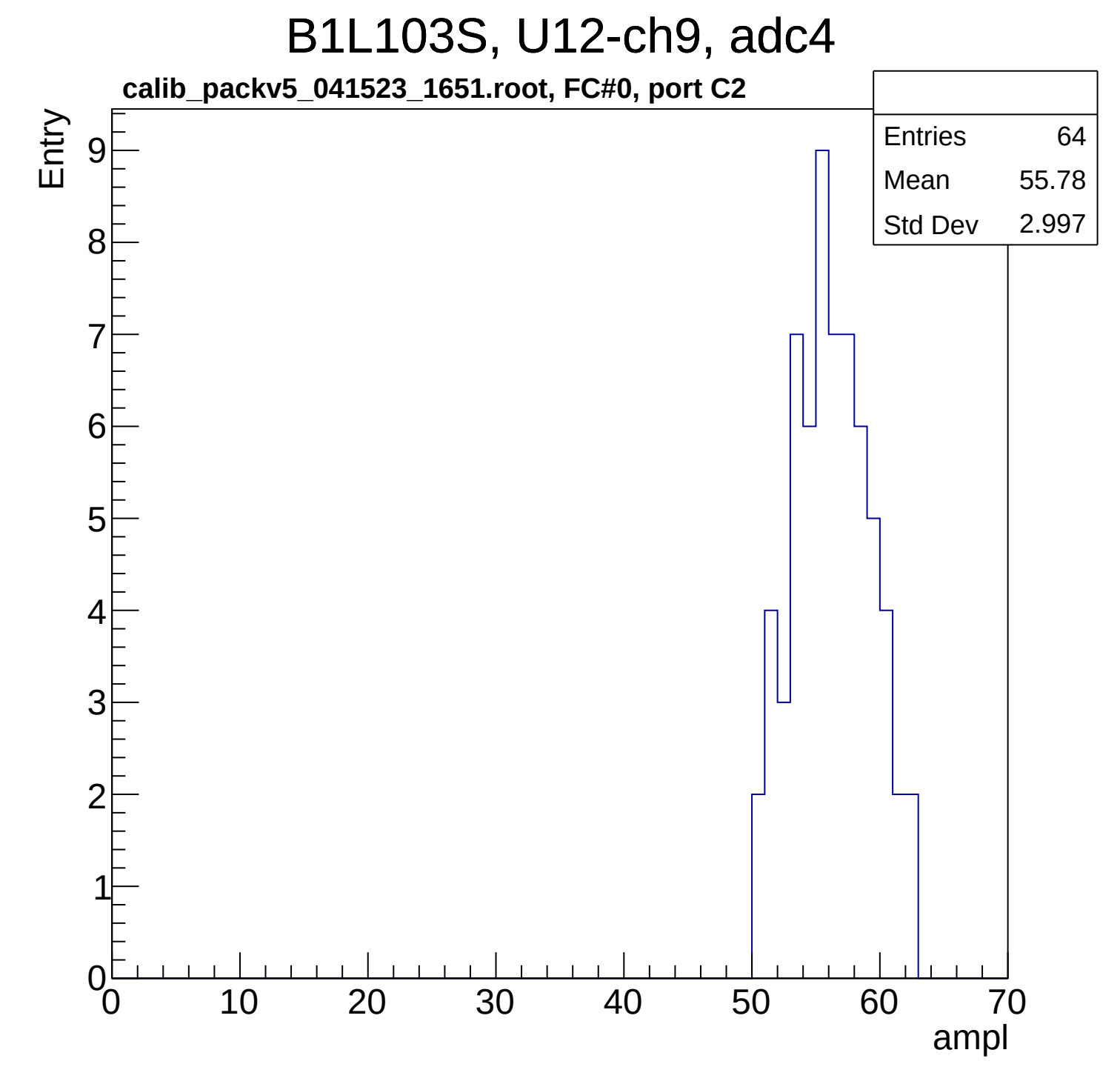
B1L103S, U12-ch9, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 55.78
Std Dev 2.997
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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60
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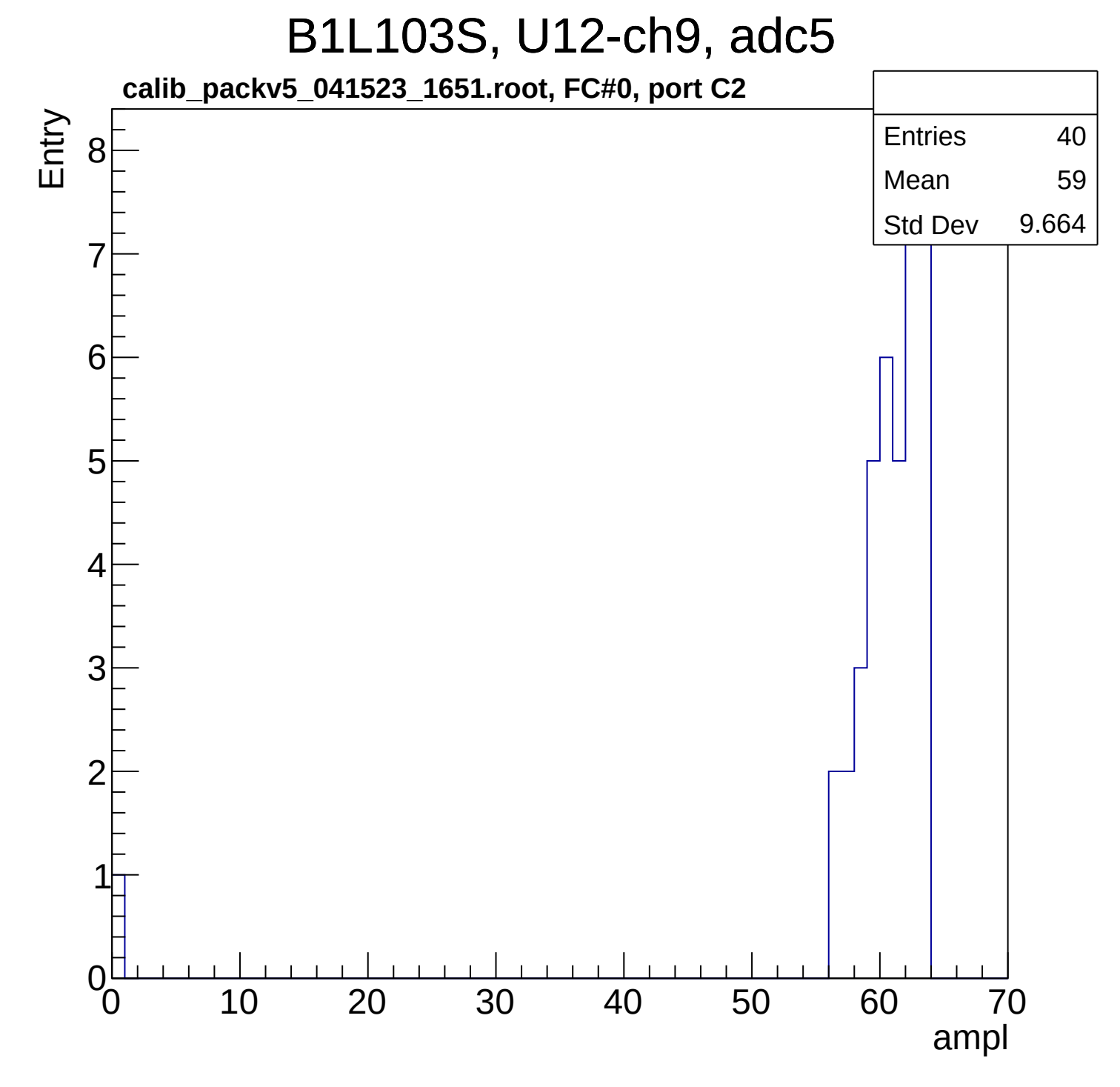
B1L103S, U12-ch9, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 59
Std Dev 9.664
Entry
ampl
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1
2
3
4
5
6
7
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0
10
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60
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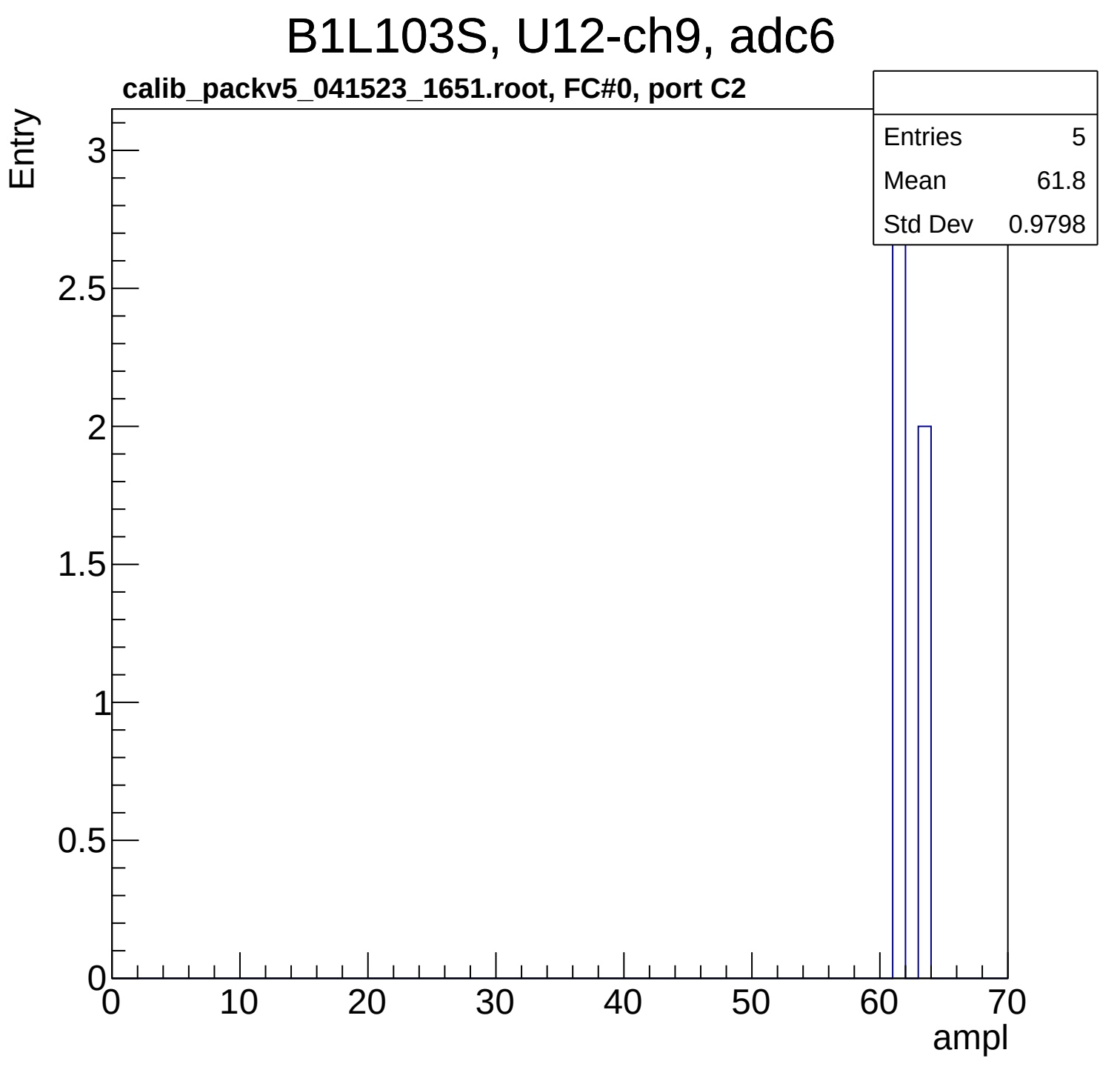
B1L103S, U12-ch9, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.8
Std Dev 0.9798
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
50
60
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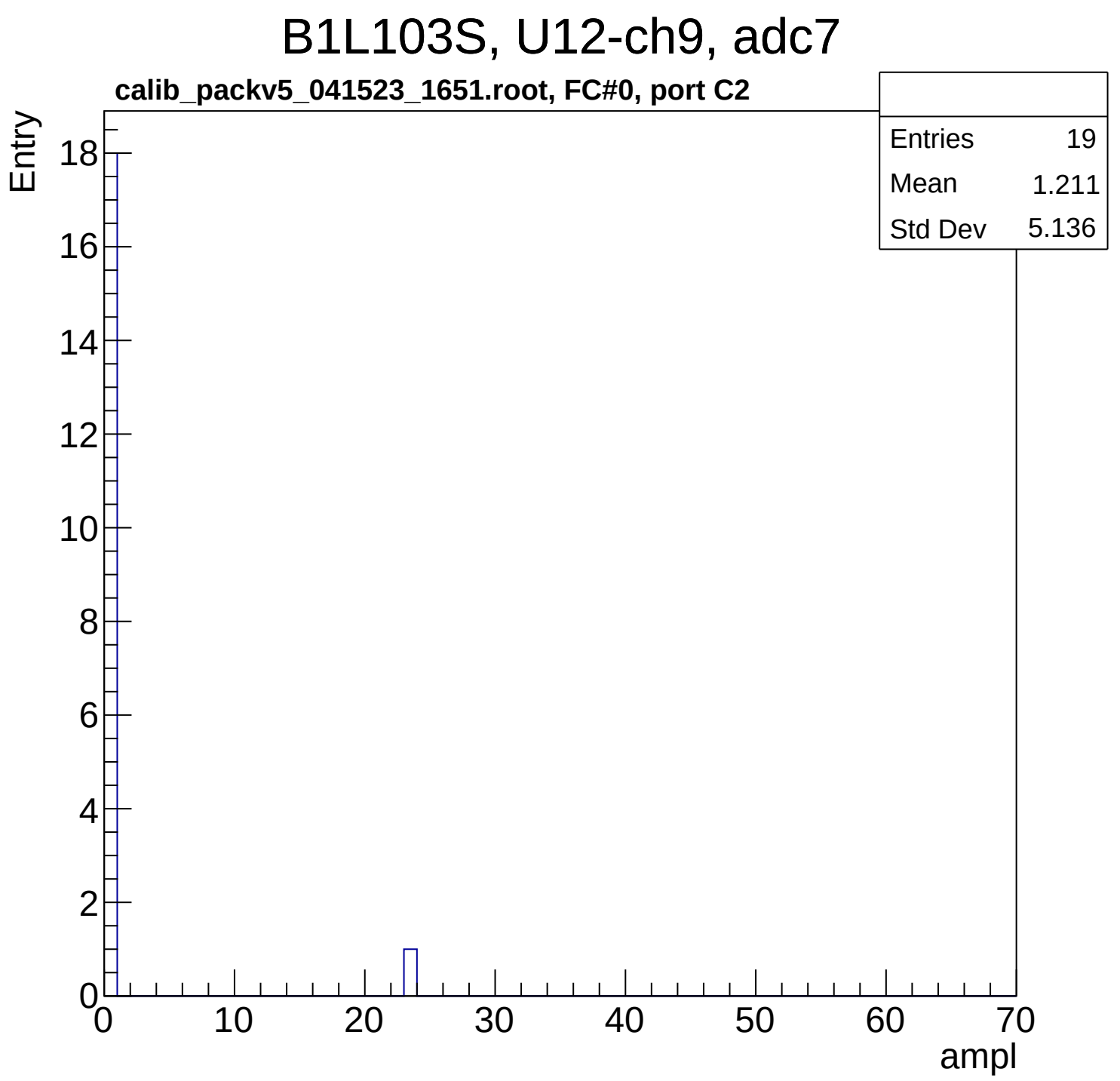
B1L103S, U12-ch9, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.211
Std Dev 5.136
Entry
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6
8
10
12
14
16
18
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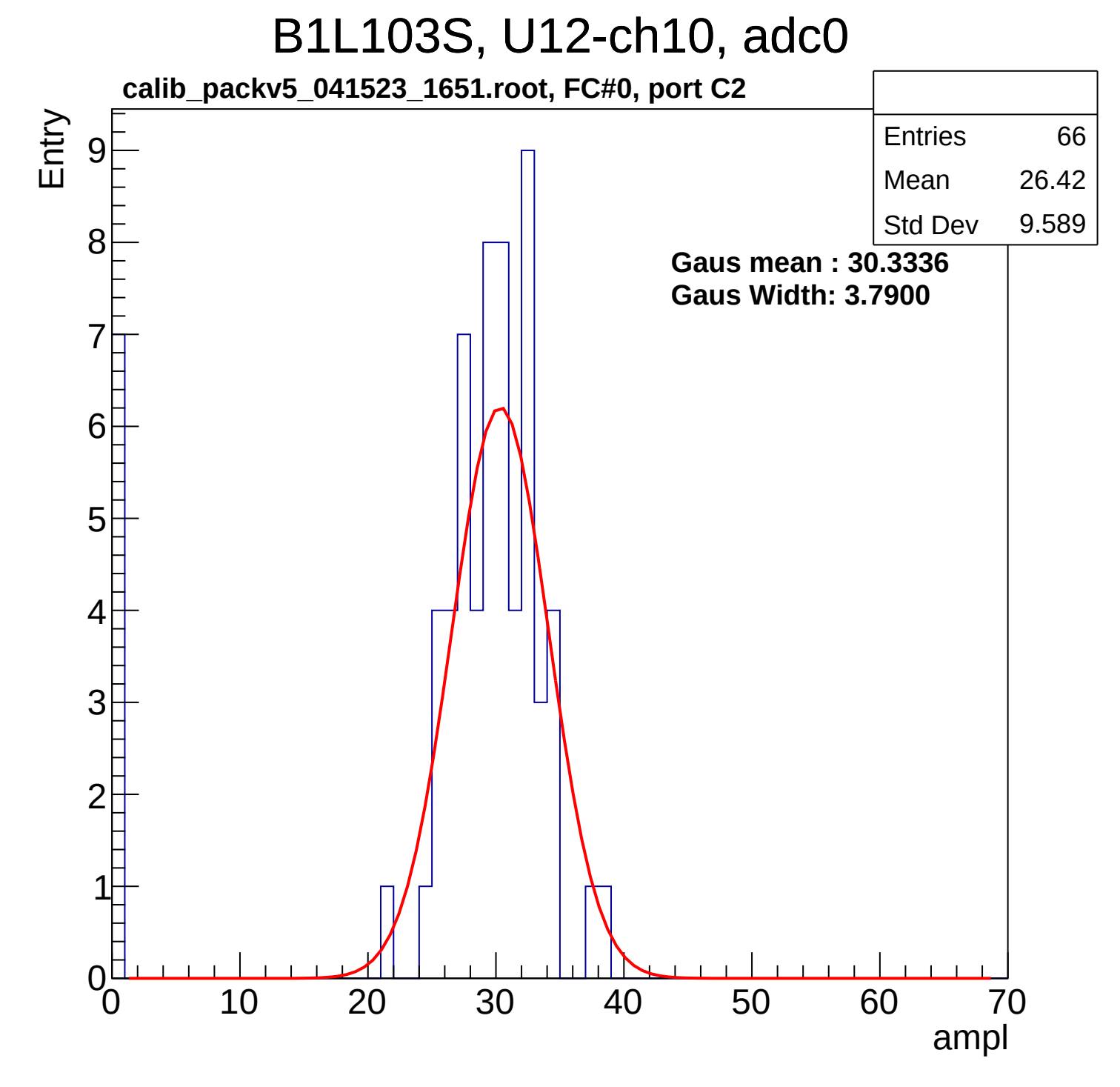
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch10, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 26.42
Std Dev 9.589
Gaus mean : 30.3336
Gaus Width: 3.7900
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
50
60
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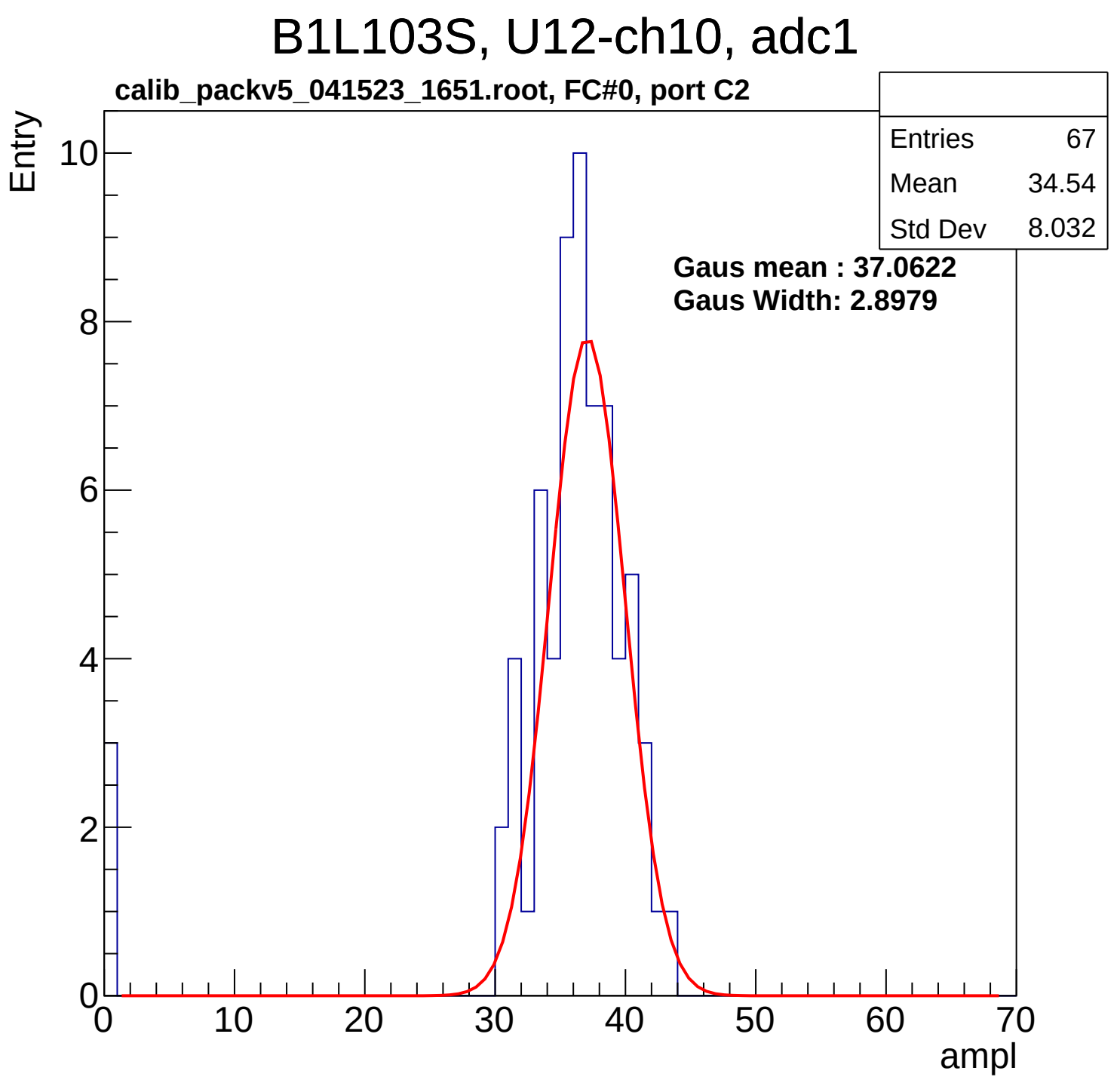
B1L103S, U12-ch10, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 34.54
Std Dev 8.032
Gaus mean : 37.0622
Gaus Width: 2.8979
Entry
ampl
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6
8
10
0
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60
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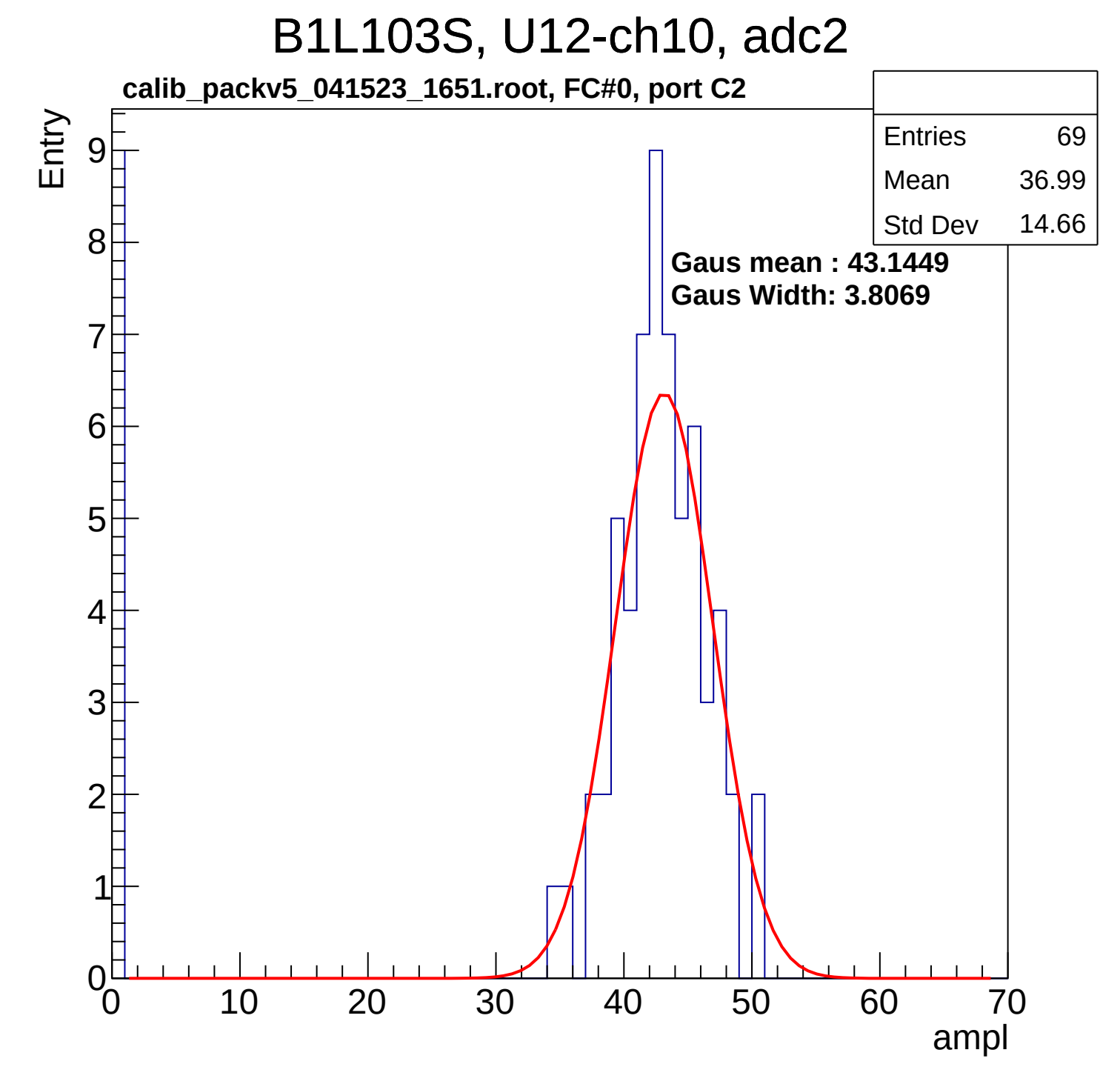
B1L103S, U12-ch10, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 36.99
Std Dev 14.66
Gaus mean : 43.1449
Gaus Width: 3.8069
Entry
ampl
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3
4
5
6
7
8
9
0
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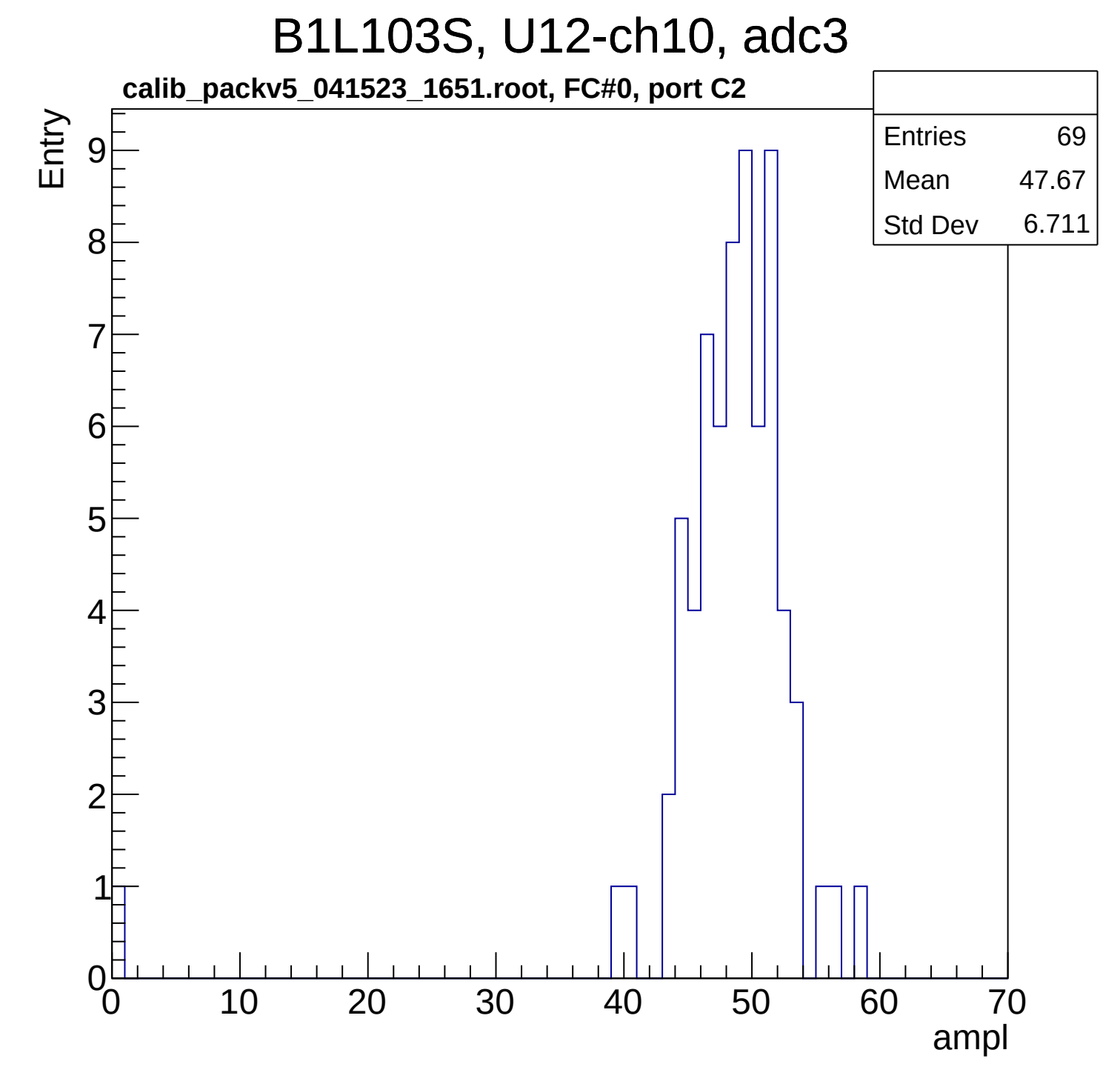
B1L103S, U12-ch10, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 47.67
Std Dev 6.711
Entry
ampl
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10
20
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2
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6
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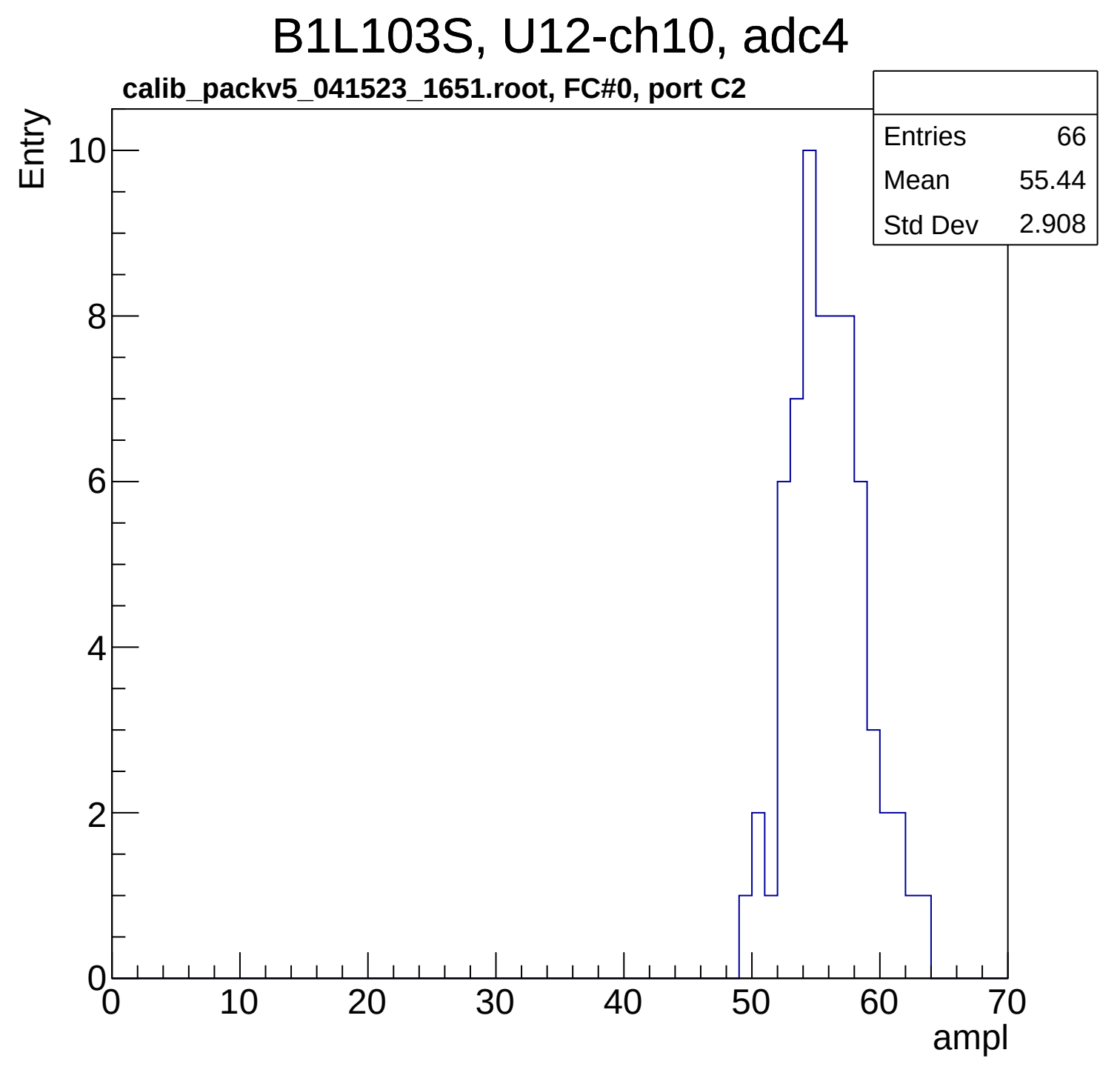
8
9


B1L103S, U12-ch10, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 55.44
Std Dev 2.908
Entry
ampl
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60
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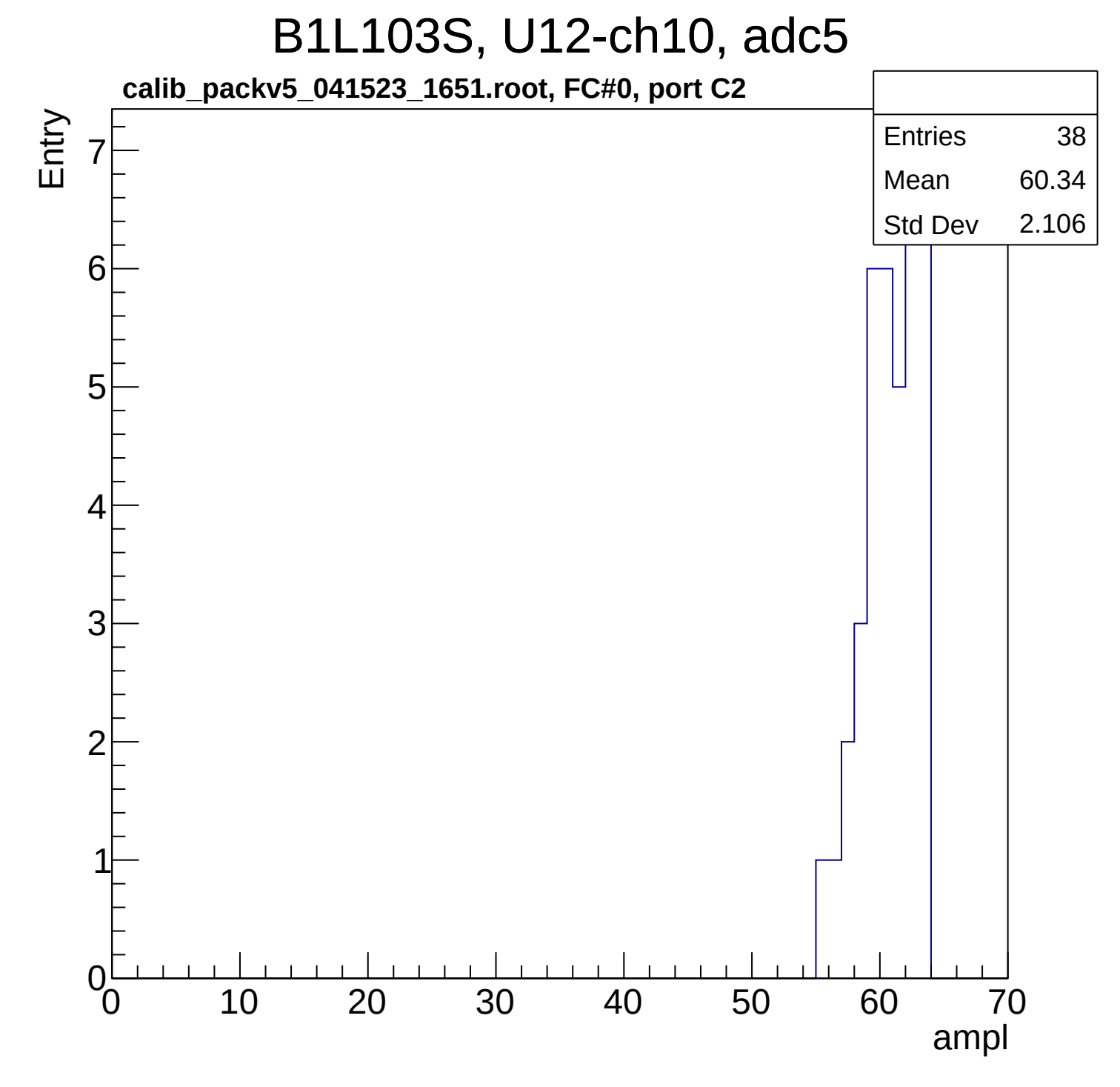
B1L103S, U12-ch10, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 60.34
Std Dev 2.106
Entry
ampl
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1
2
3
4
5
6
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0
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60
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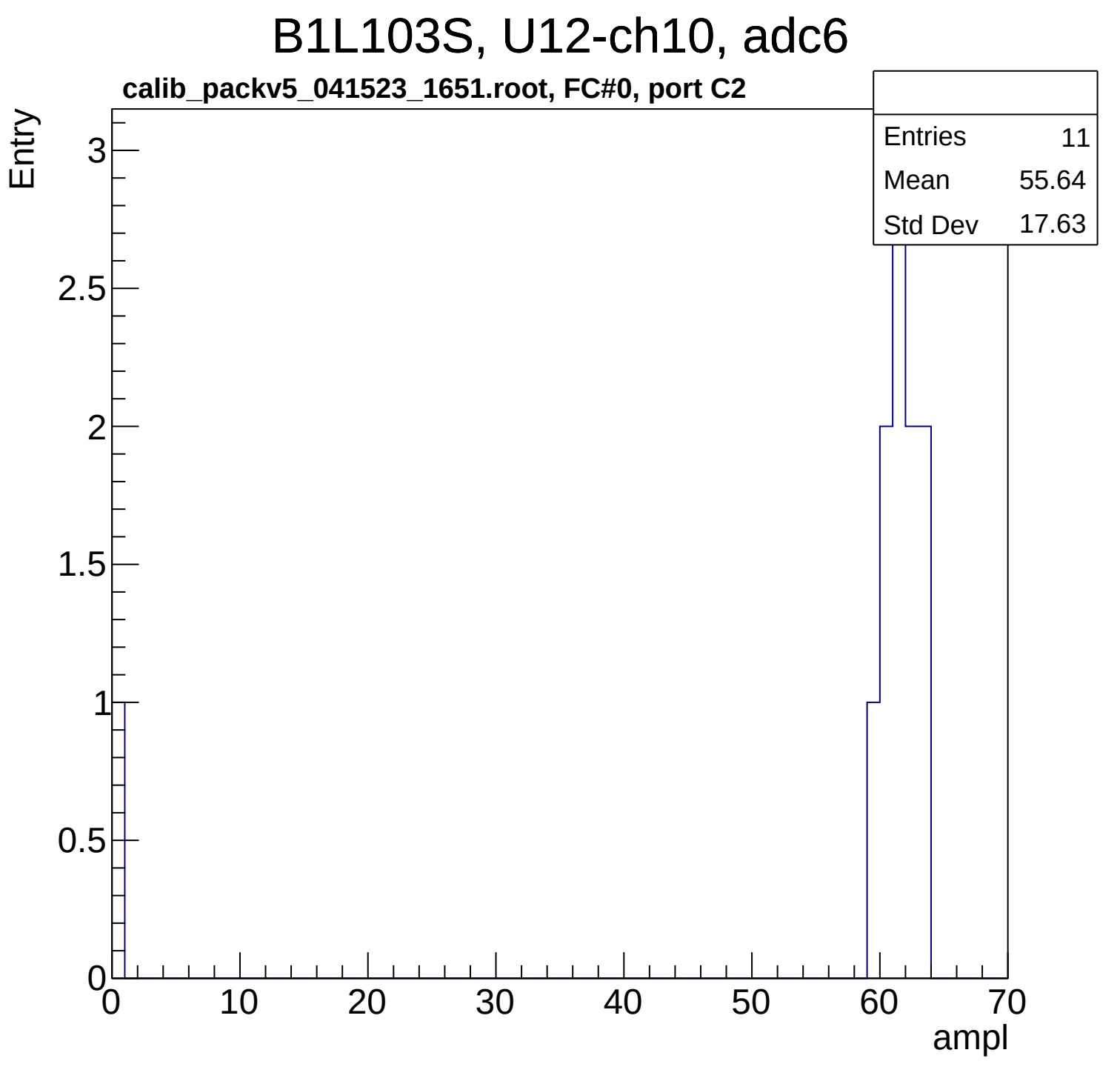
B1L103S, U12-ch10, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 55.64
Std Dev 17.63
Entry
ampl
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0.5
1
1.5
2
2.5
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0
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40
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60
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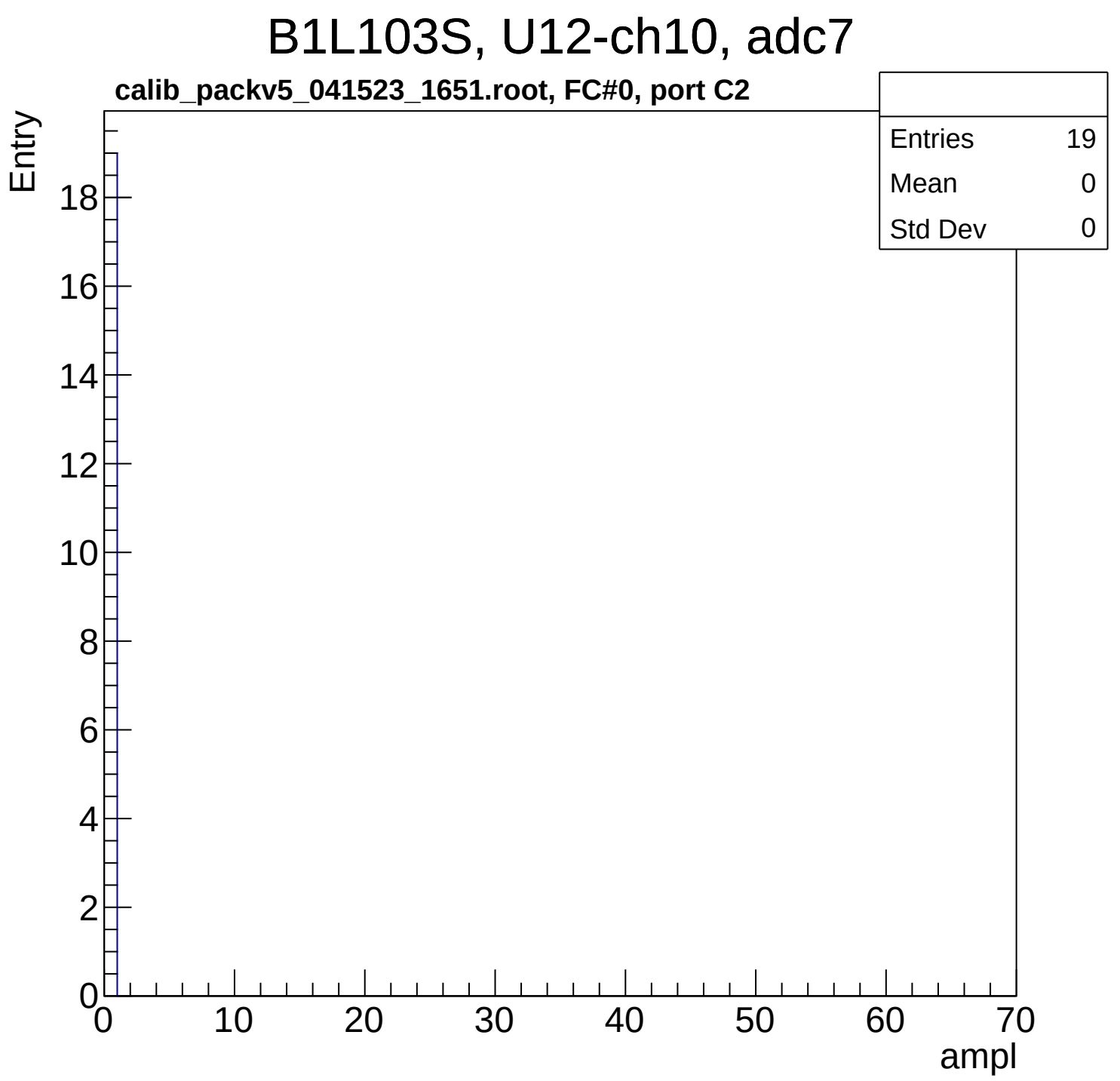
B1L103S, U12-ch10, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
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6
8
10
12
14
16
18
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10
20
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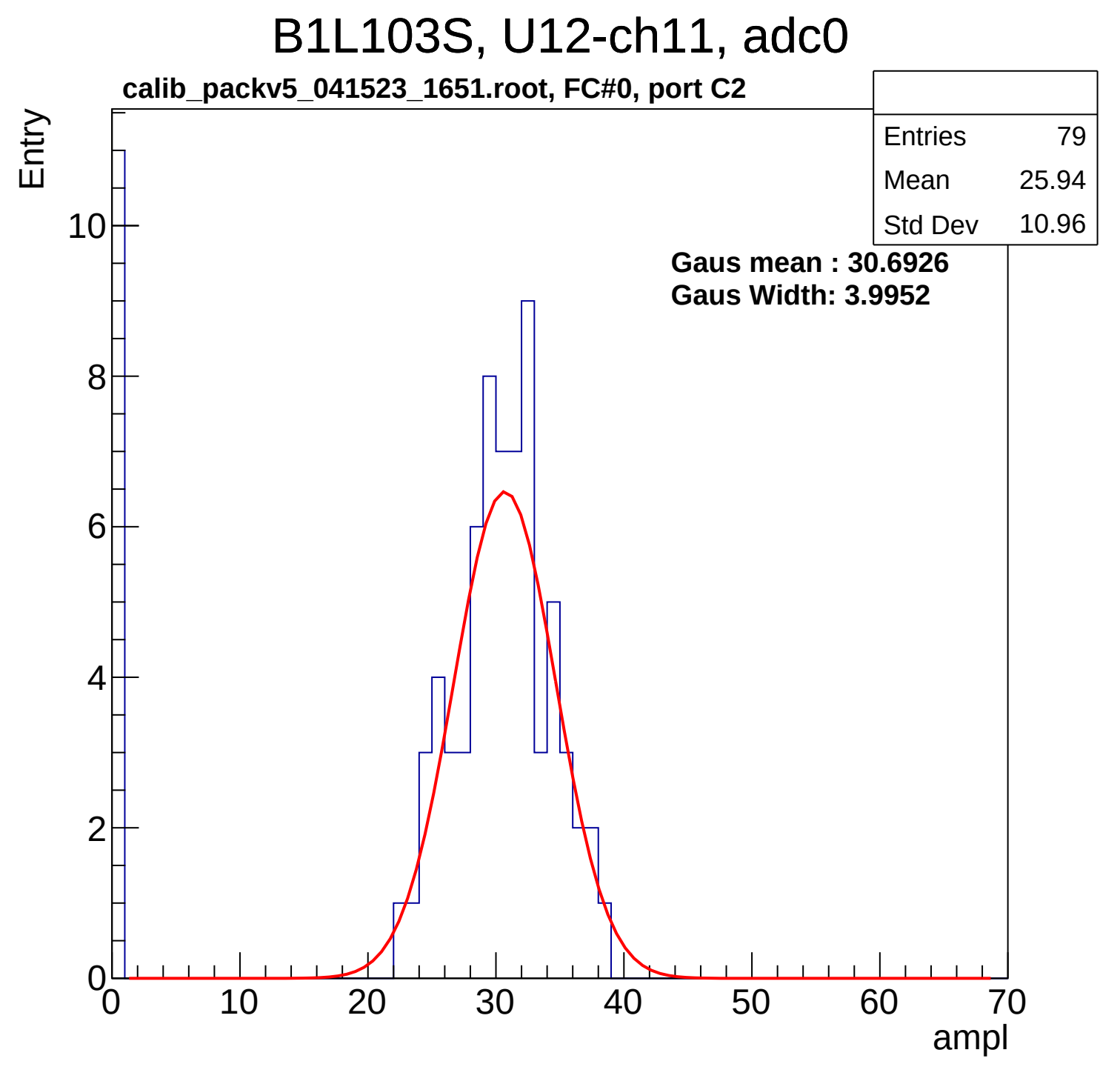
50
60
70
ampl


B1L103S, U12-ch11, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 25.94
Std Dev 10.96
Gaus mean : 30.6926
Gaus Width: 3.9952
Entry
ampl
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2
4
6
8
10
0
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40
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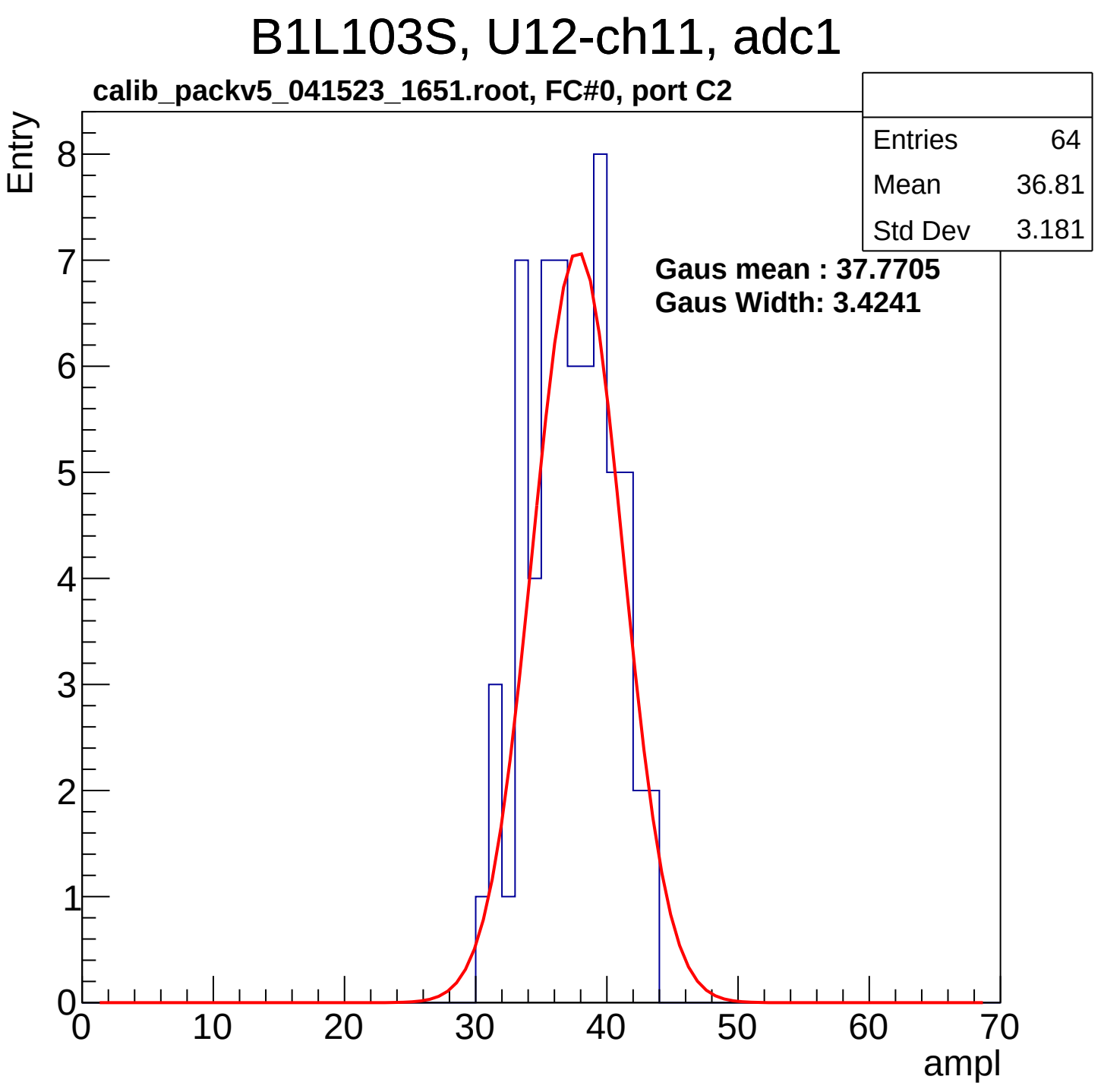
B1L103S, U12-ch11, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 36.81
Std Dev 3.181
Gaus mean : 37.7705
Gaus Width: 3.4241
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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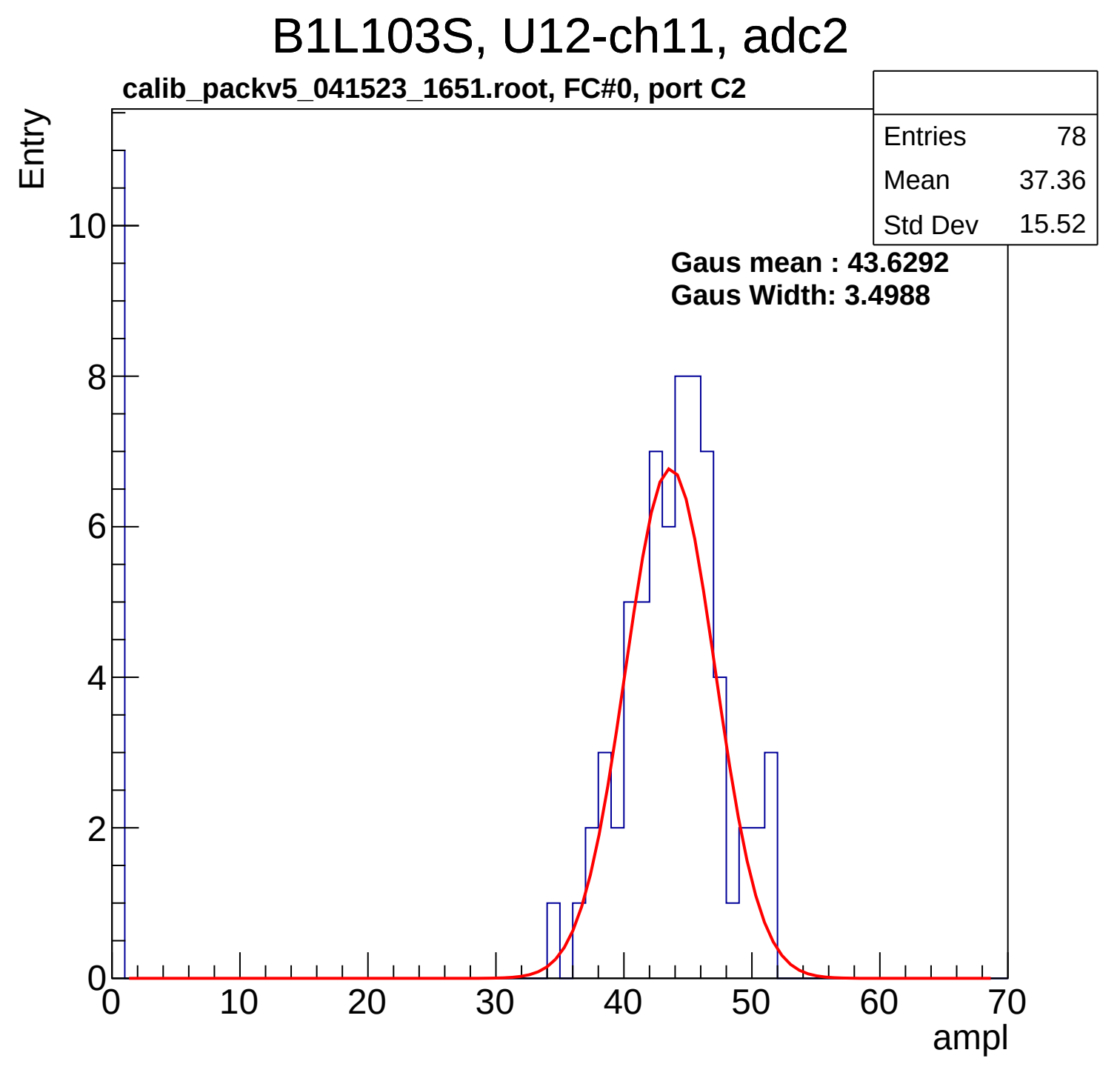
B1L103S, U12-ch11, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 37.36
Std Dev 15.52
Gaus mean : 43.6292
Gaus Width: 3.4988
Entry
ampl
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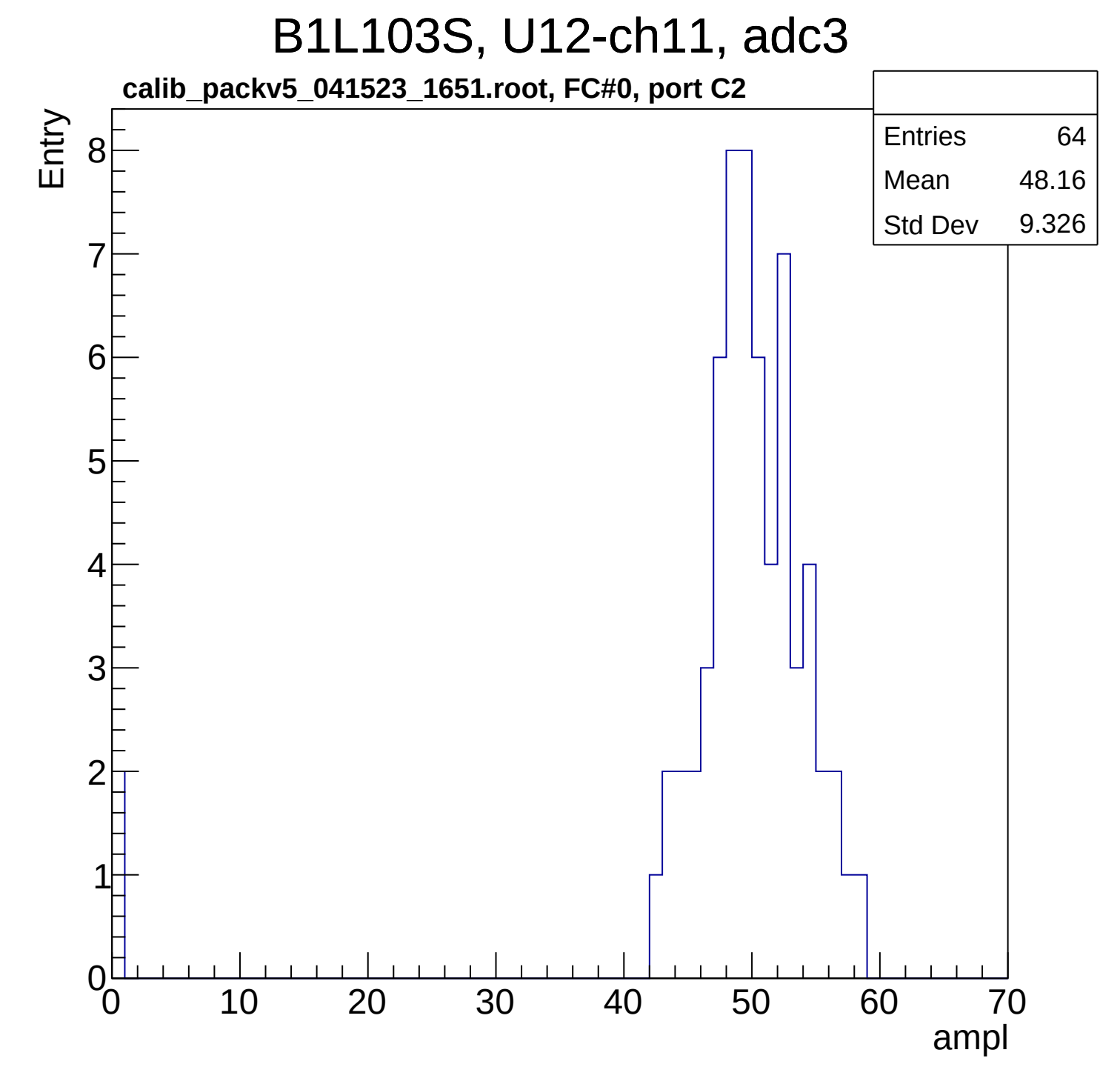
B1L103S, U12-ch11, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 48.16
Std Dev 9.326
Entry
ampl
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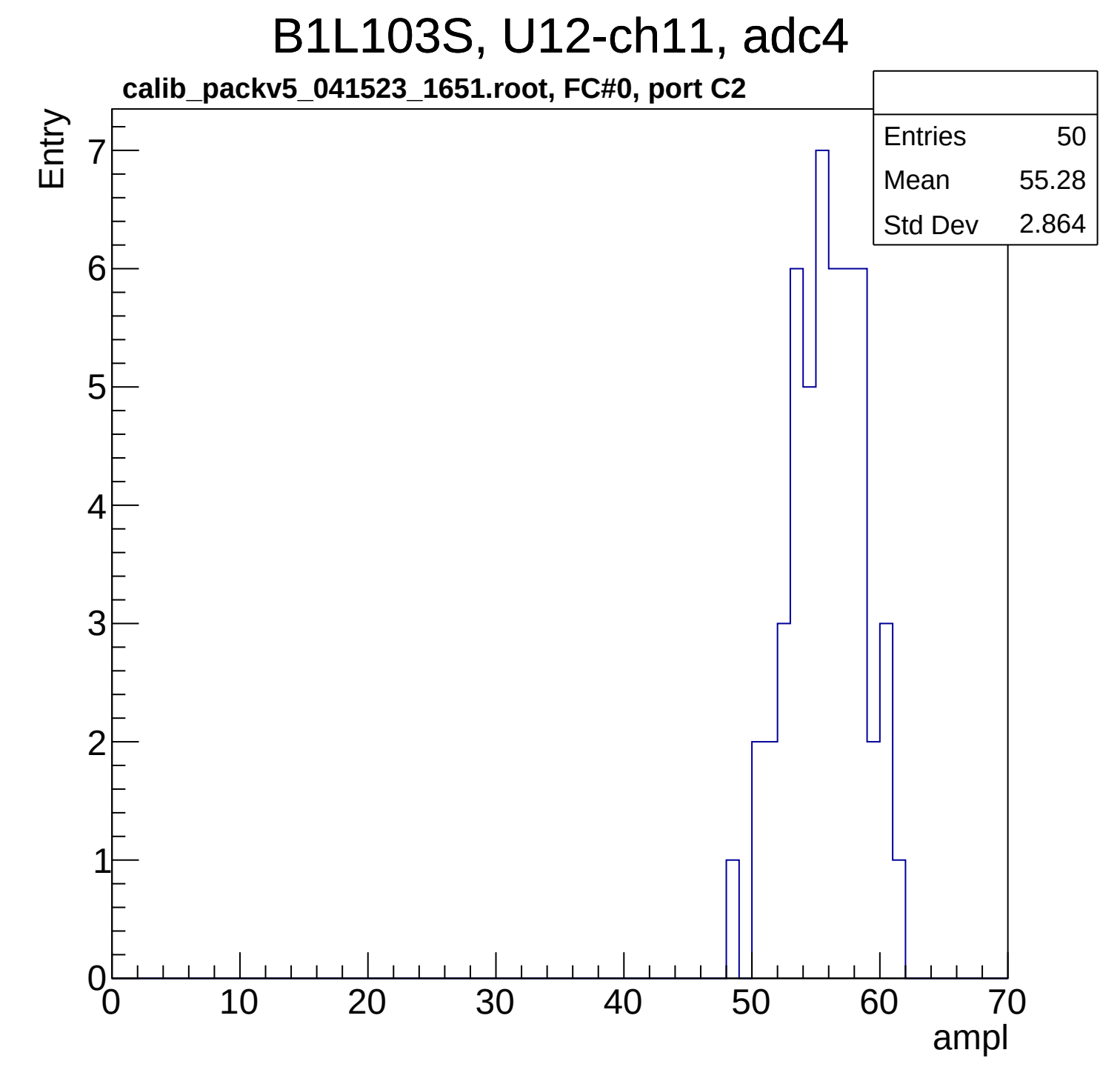
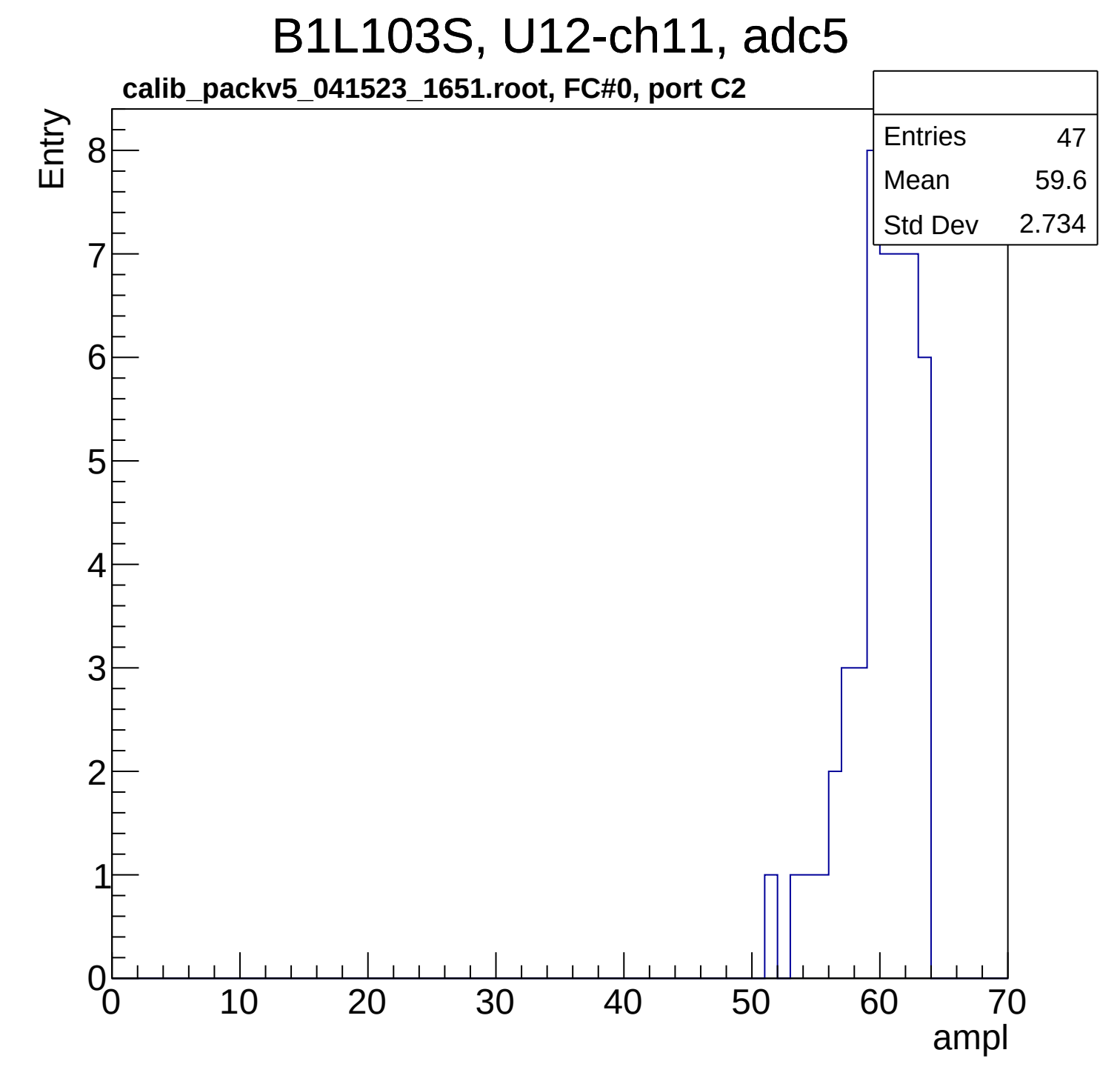

B1L103S, U12-ch11, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 55.28
Std Dev 2.864
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U12-ch11, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 59.6
Std Dev 2.734
Entry
ampl
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5
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0
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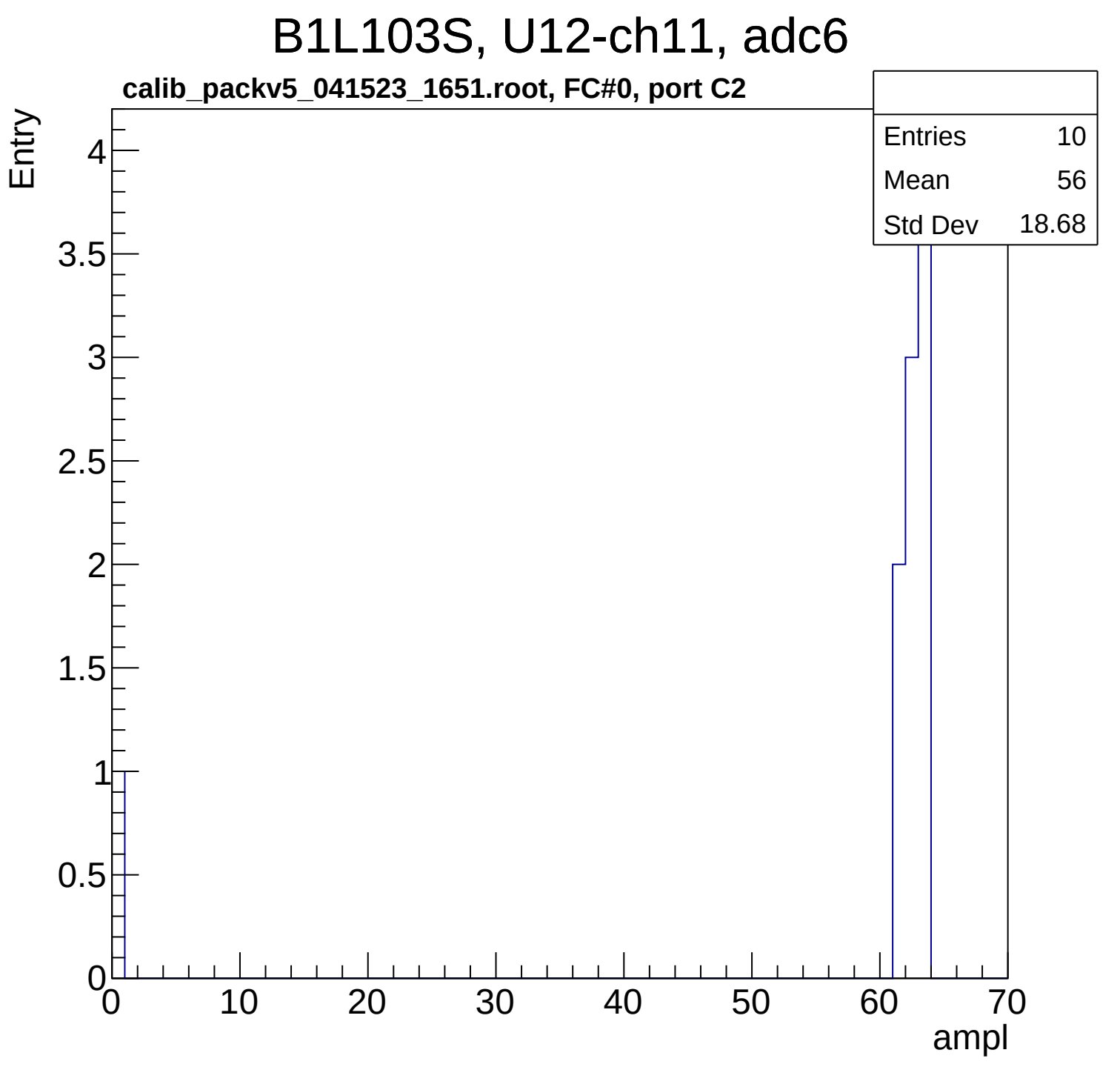
B1L103S, U12-ch11, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 56
Std Dev 18.68
Entry
ampl
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1.5
2
2.5
3
3.5
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0
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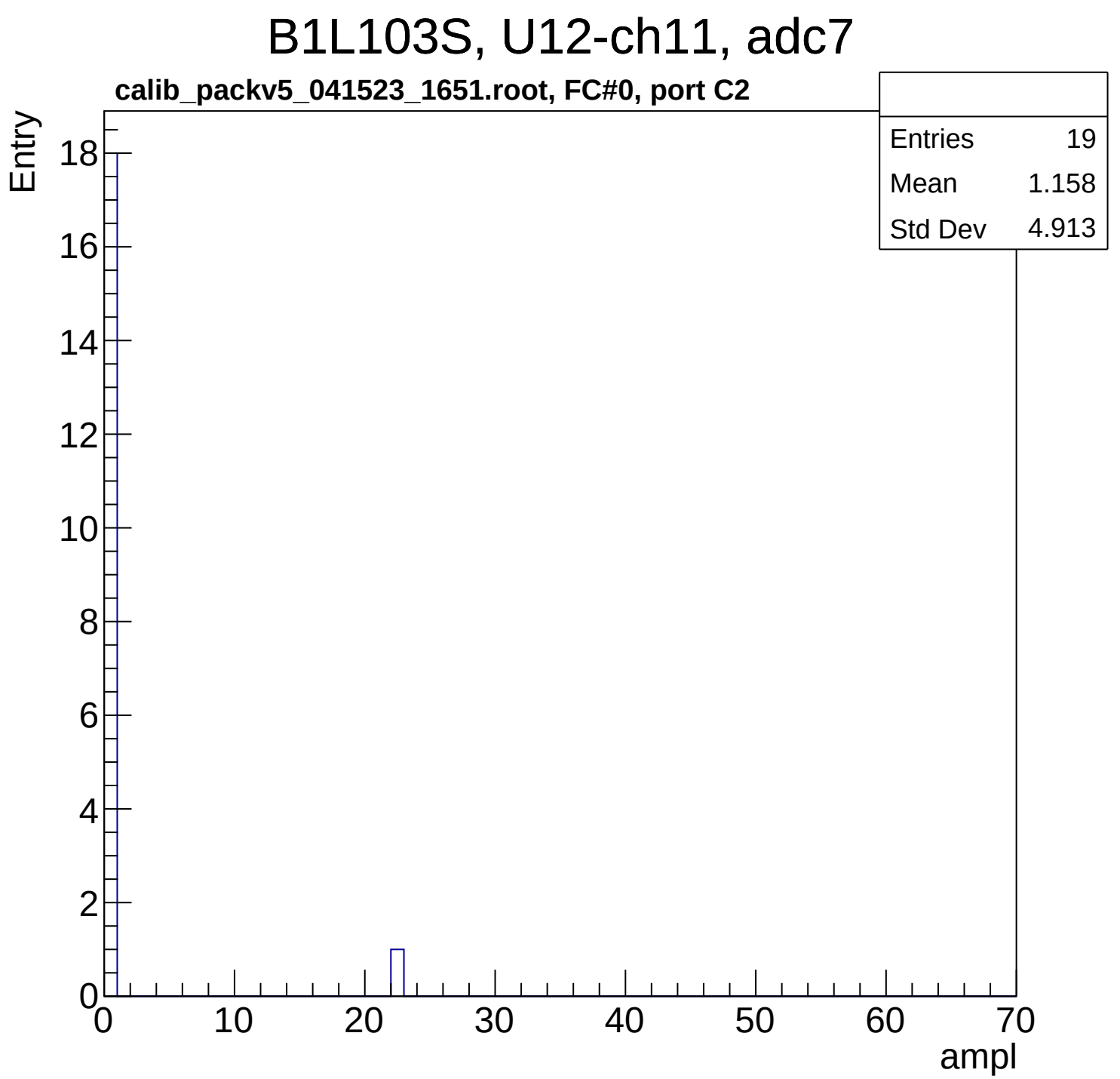
B1L103S, U12-ch11, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
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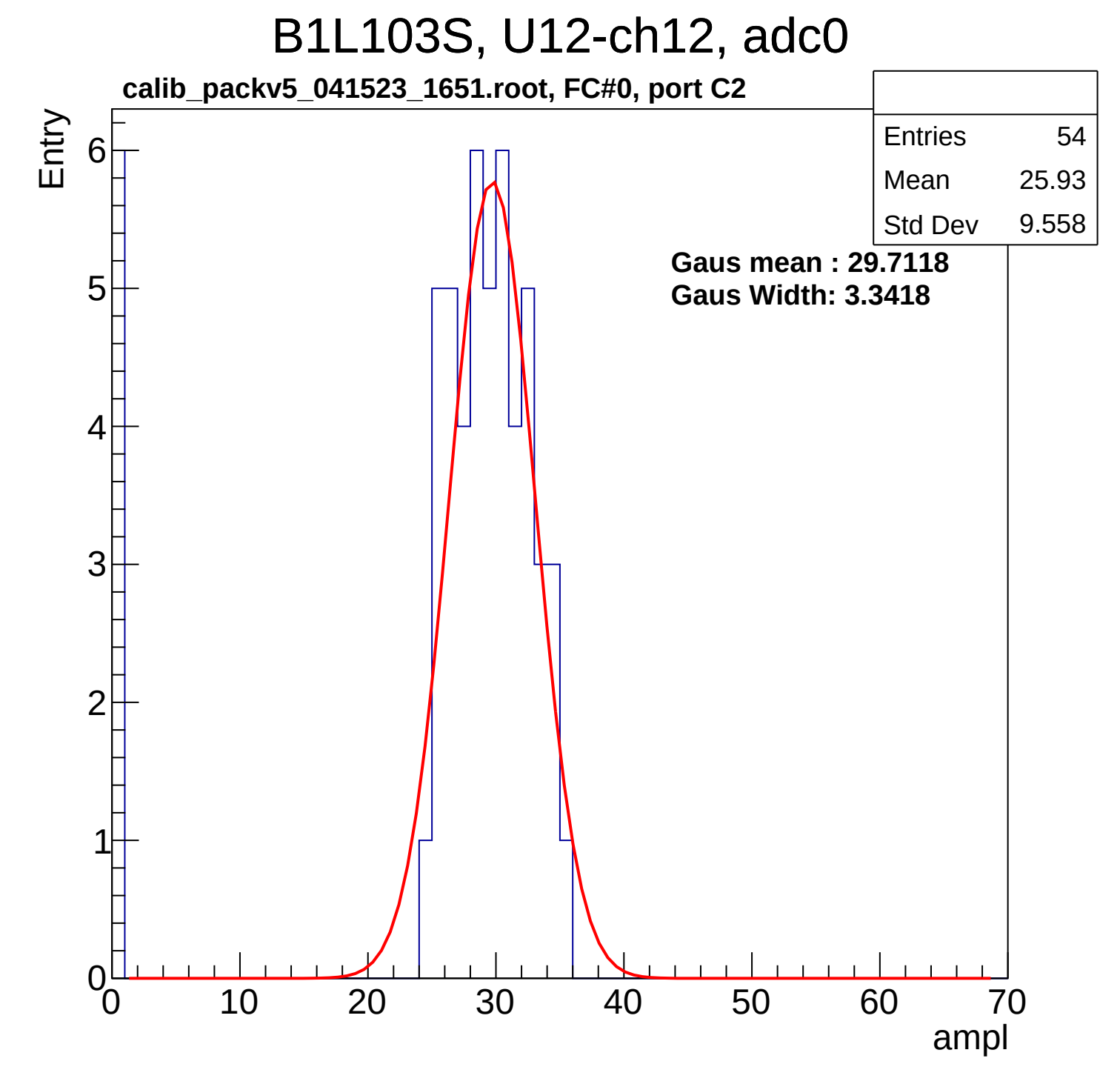
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch12, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 25.93
Std Dev 9.558
Gaus mean : 29.7118
Gaus Width: 3.3418
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
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60
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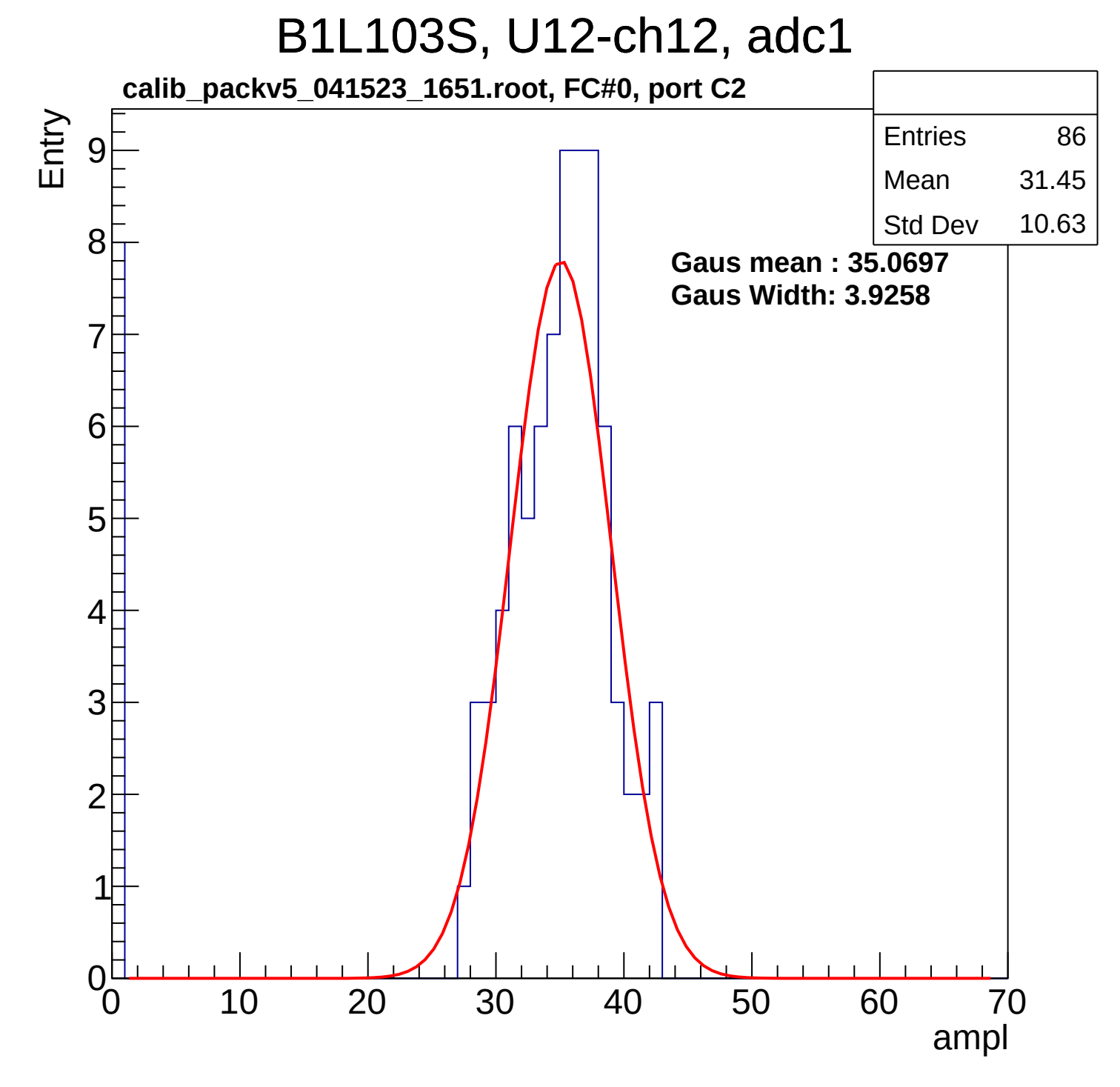
B1L103S, U12-ch12, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 31.45
Std Dev 10.63
Gaus mean : 35.0697
Gaus Width: 3.9258
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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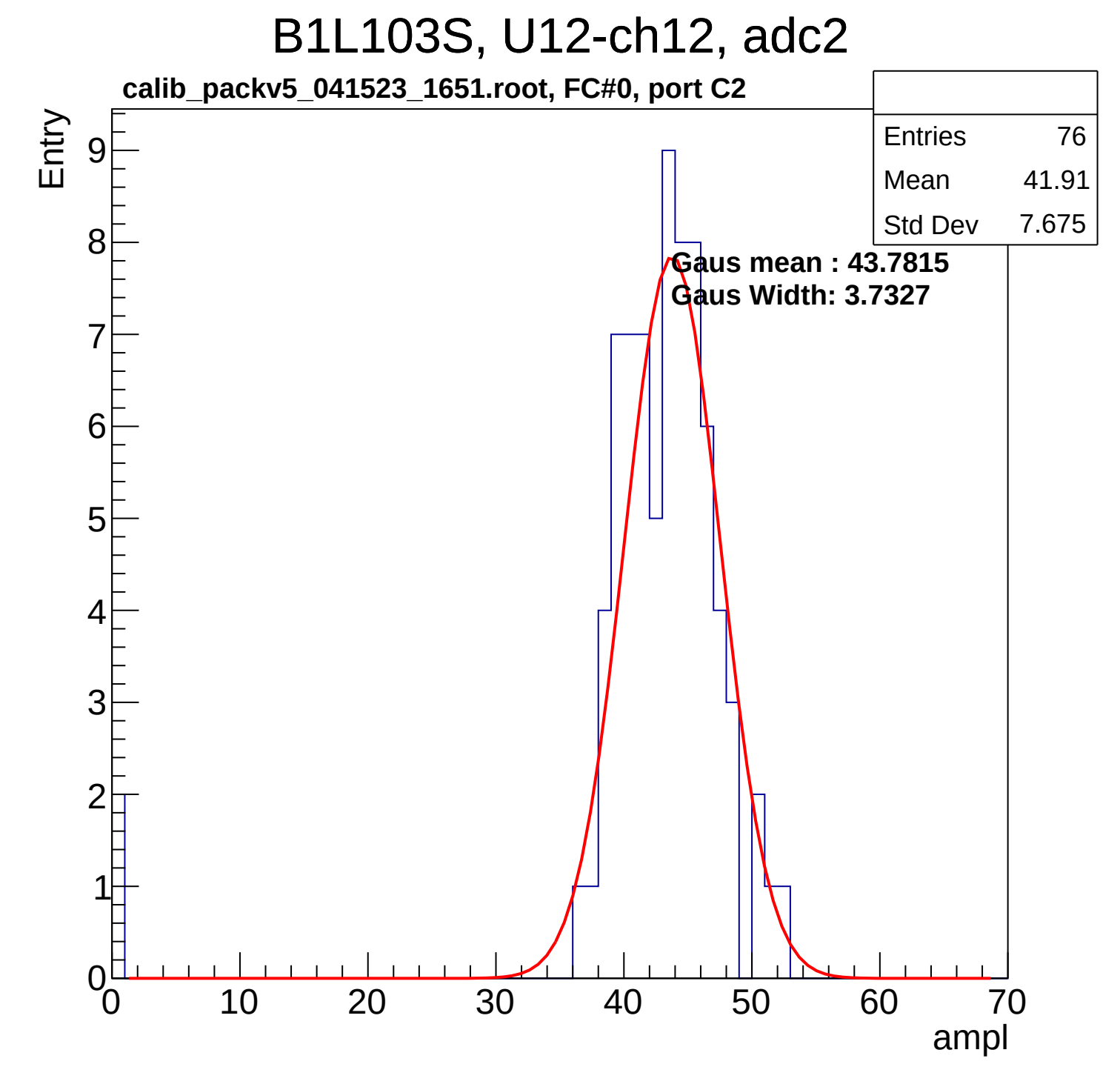
B1L103S, U12-ch12, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 41.91
Std Dev 7.675
Gaus mean : 43.7815
Gaus Width: 3.7327
Entry
ampl
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2
3
4
5
6
7
8
9
0
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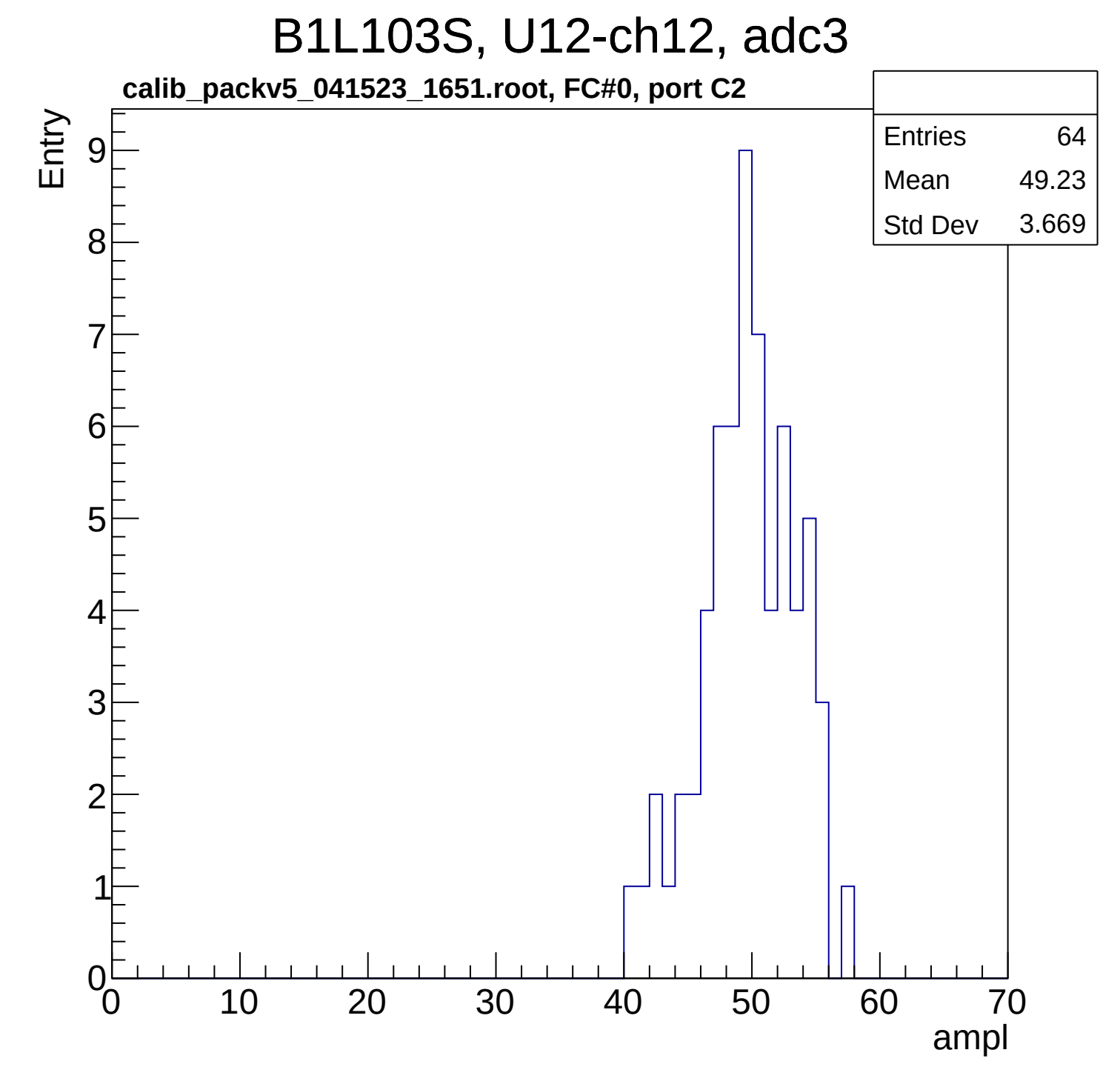
B1L103S, U12-ch12, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 49.23
Std Dev 3.669
Entry
ampl
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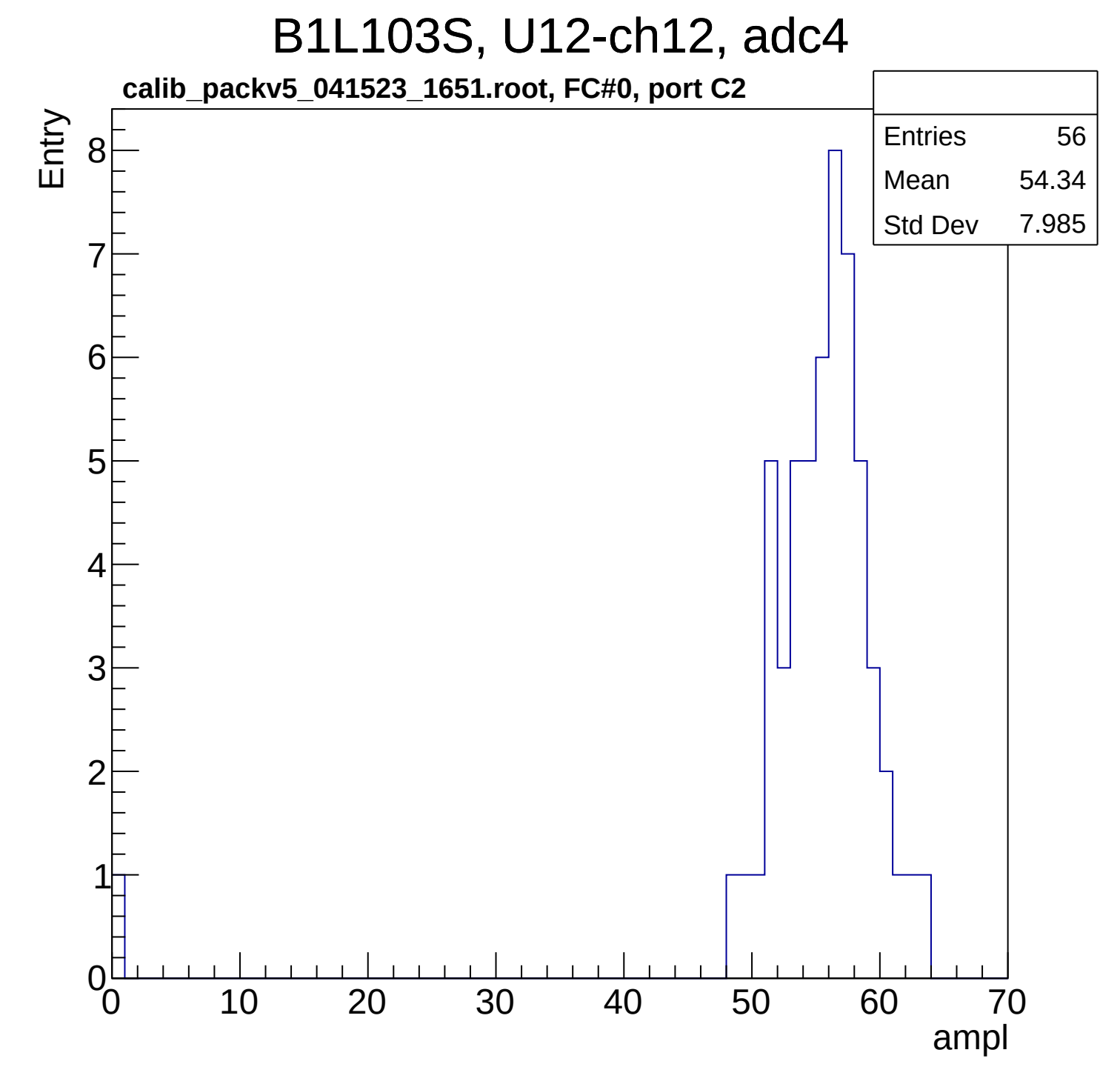
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U12-ch12, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 54.34
Std Dev 7.985
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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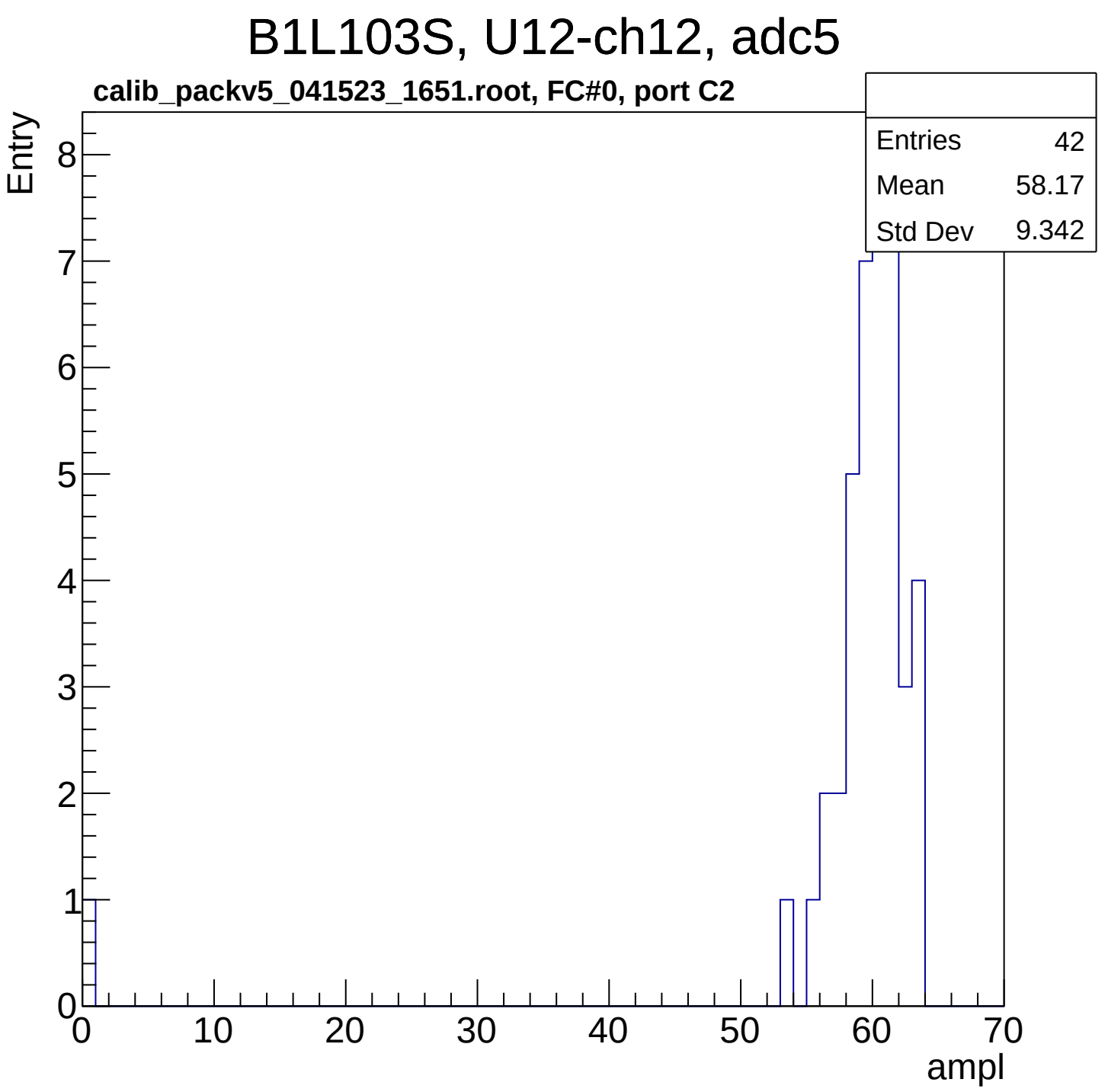
B1L103S, U12-ch12, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 58.17
Std Dev 9.342
Entry
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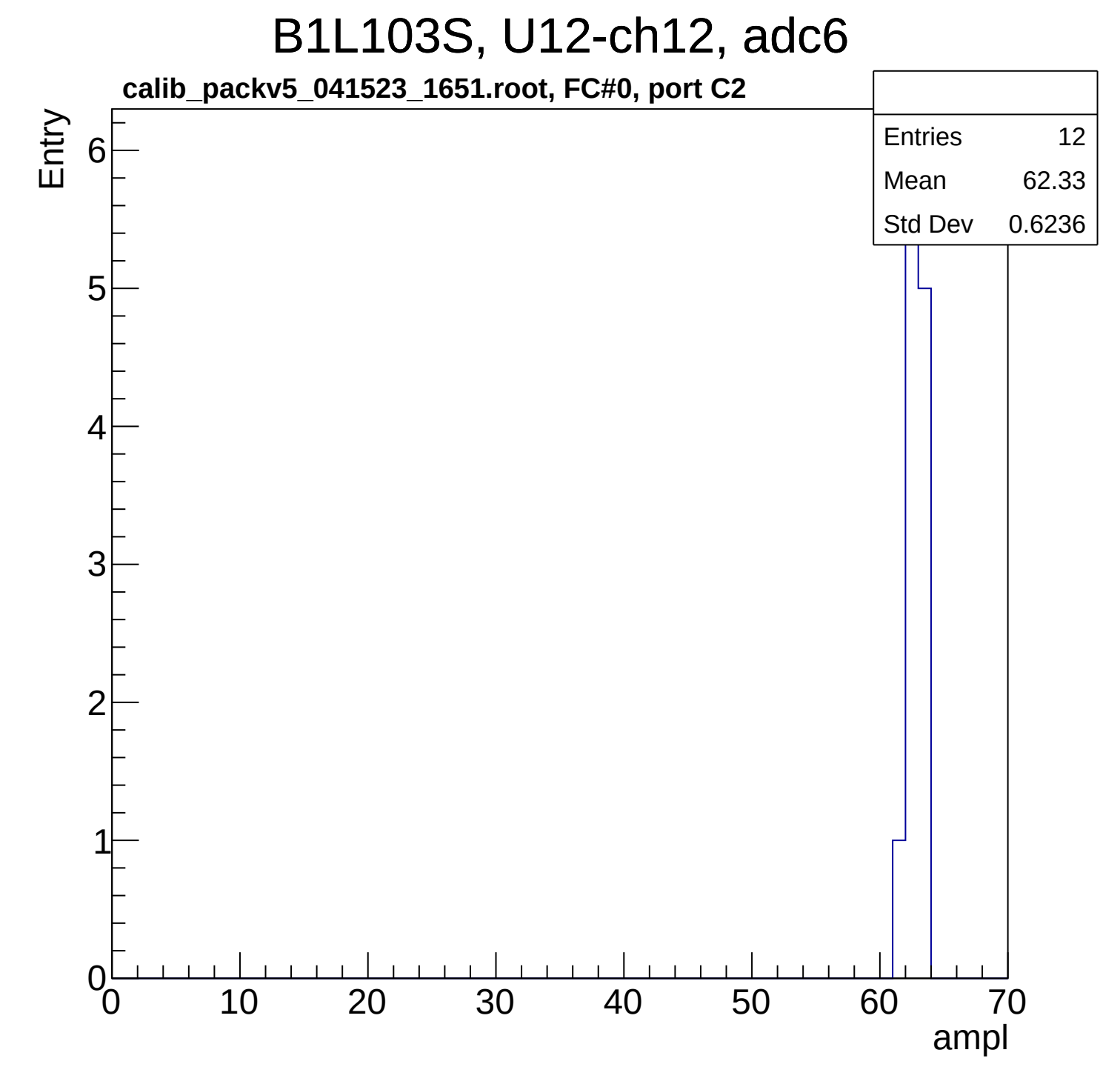
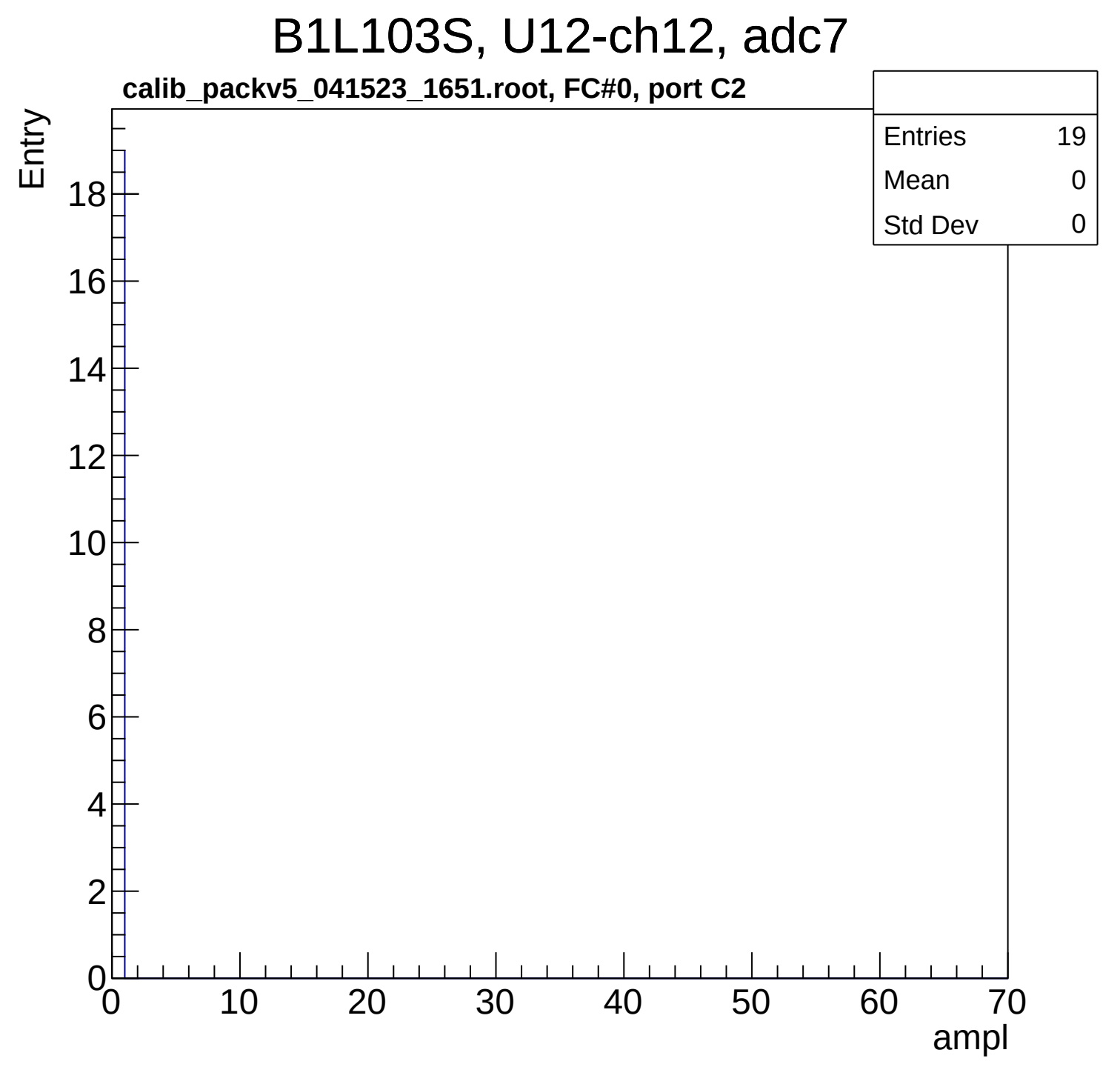
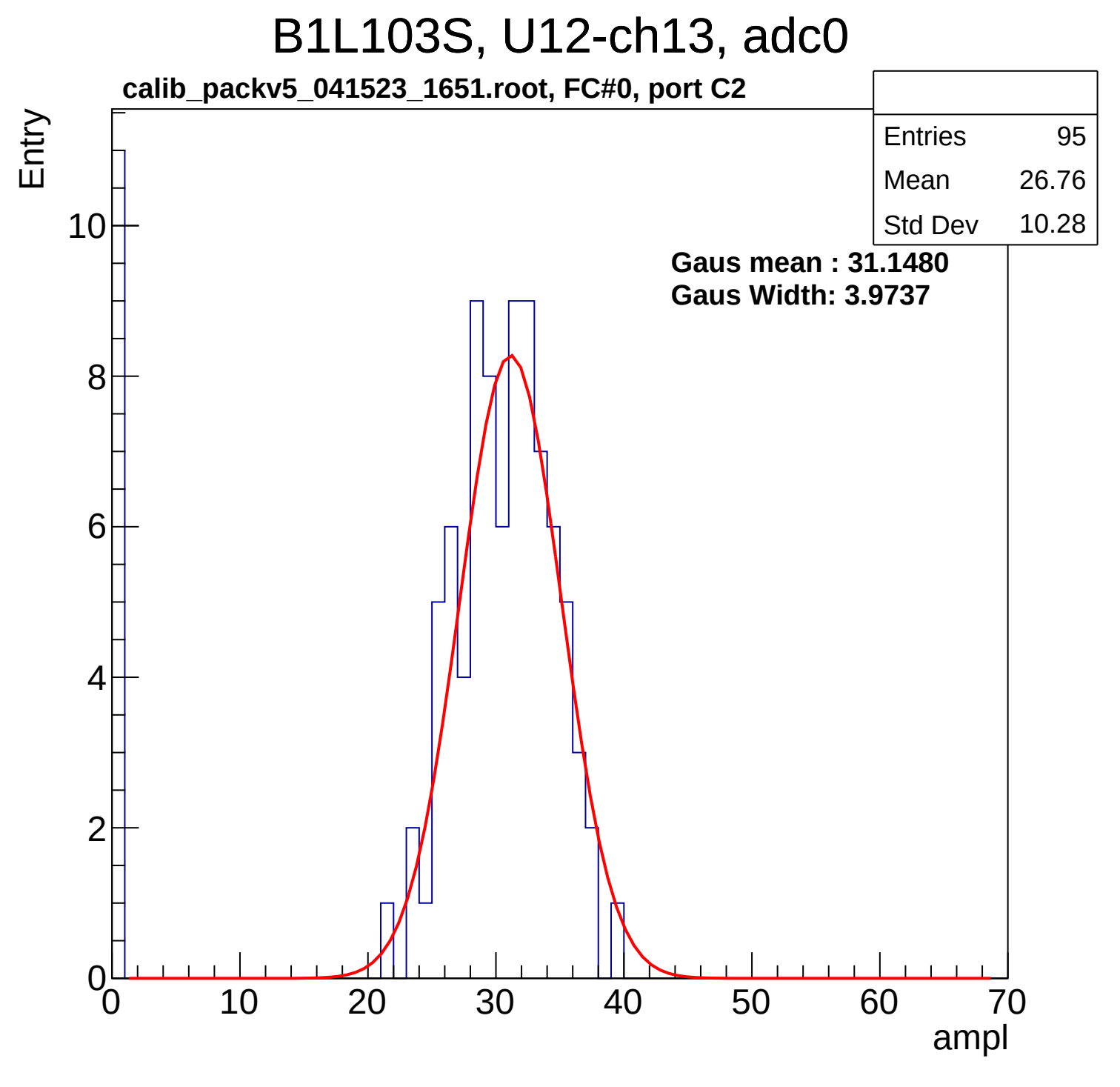
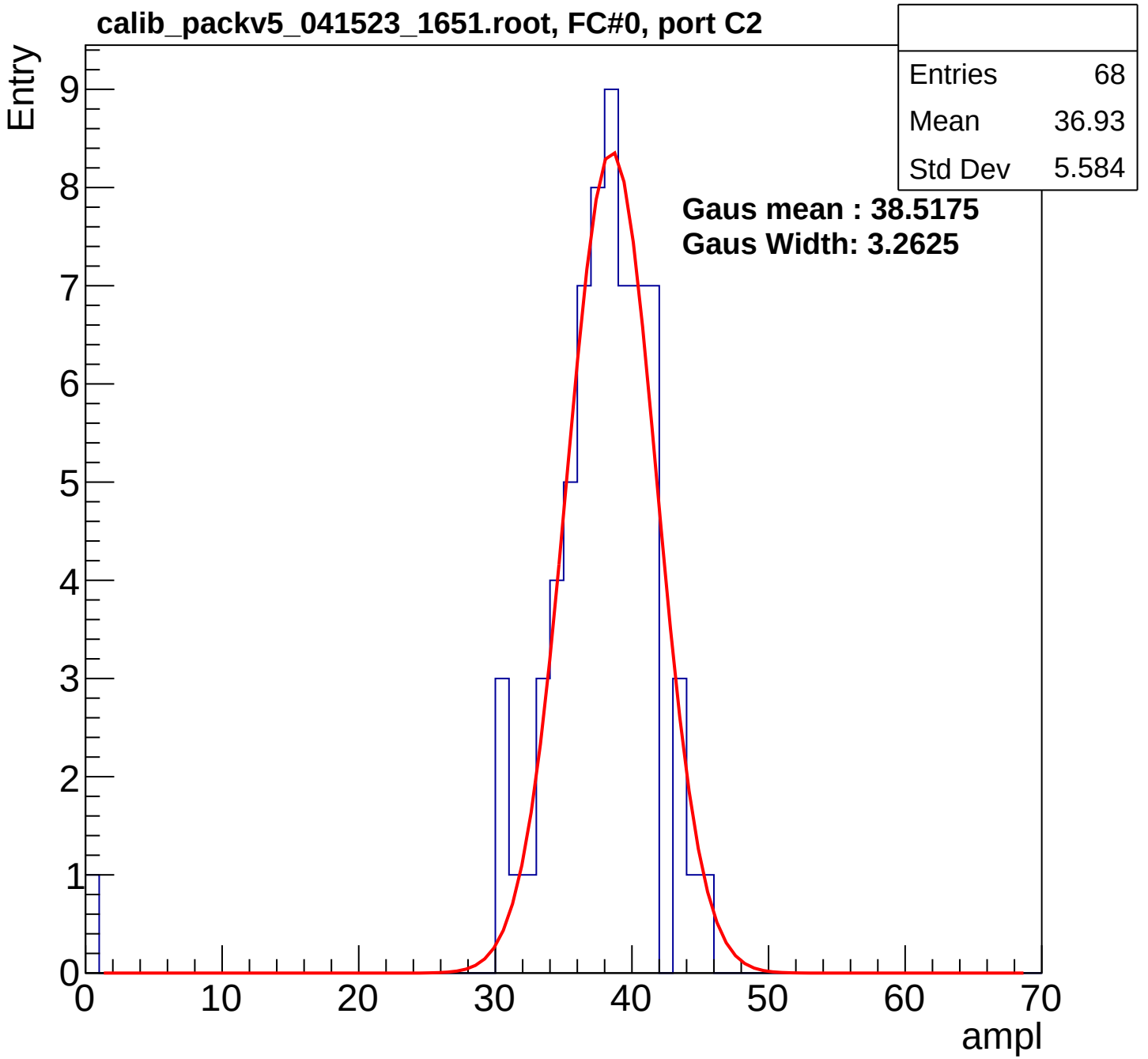
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch12, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 62.33
Std Dev 0.6236
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U12-ch12, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch13, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 26.76
Std Dev 10.28
Gaus mean : 31.1480
Gaus Width: 3.9737
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch13, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 36.93
Std Dev 5.584
Gaus mean : 38.5175
Gaus Width: 3.2625
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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60
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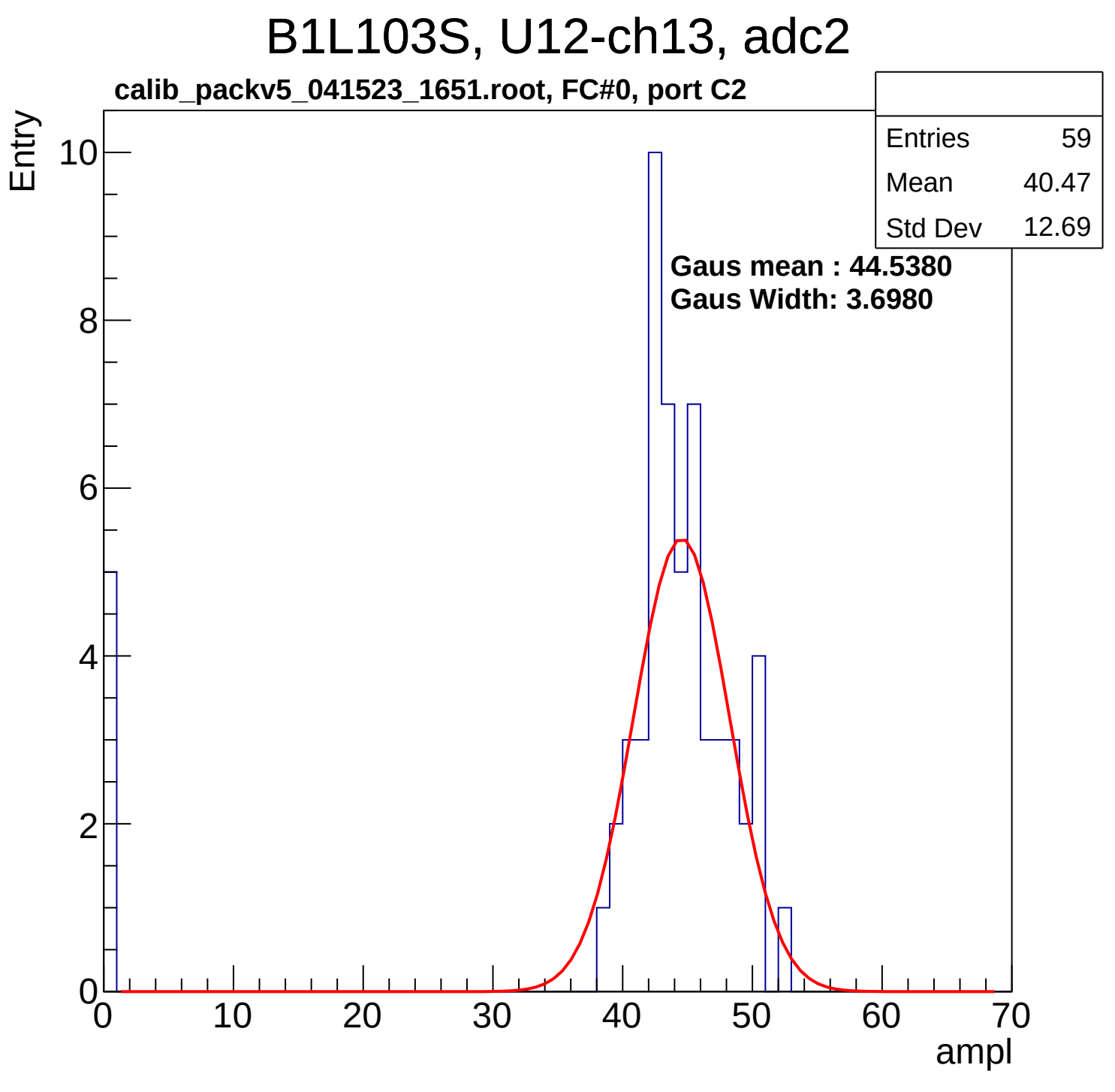
B1L103S, U12-ch13, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 40.47
Std Dev 12.69
Gaus mean : 44.5380
Gaus Width: 3.6980
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
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60
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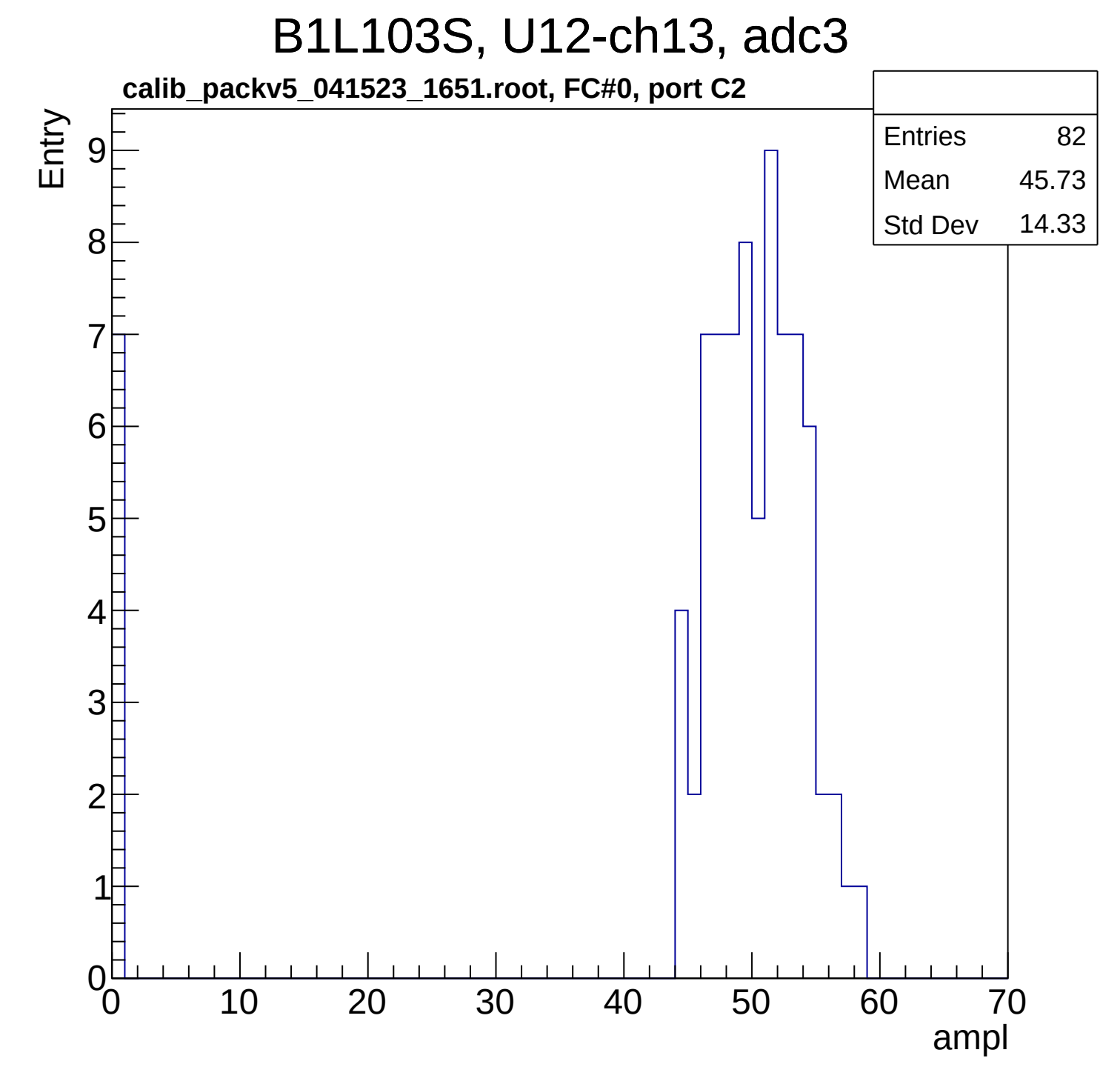
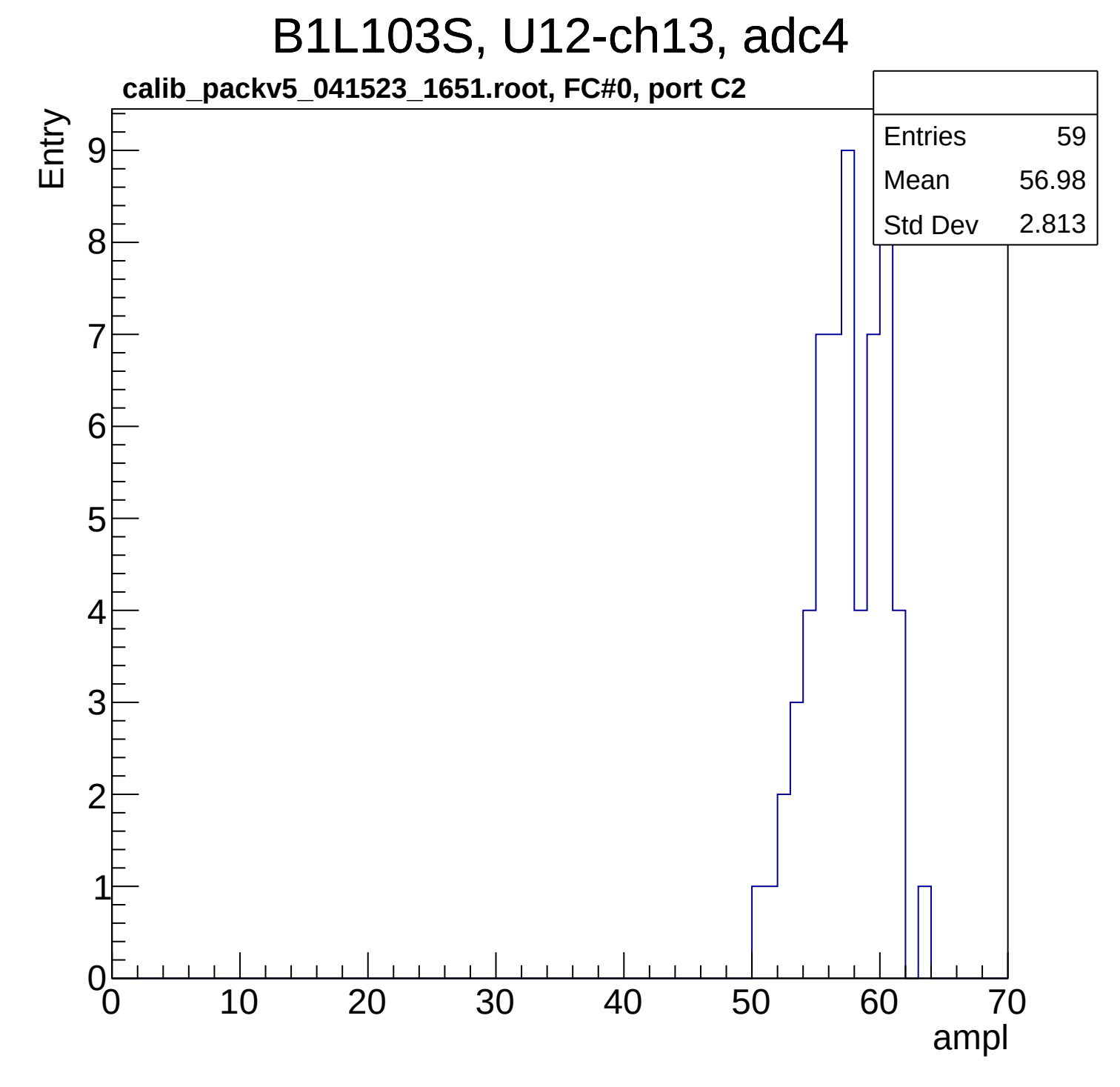

B1L103S, U12-ch13, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 45.73
Std Dev 14.33
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U12-ch13, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 56.98
Std Dev 2.813
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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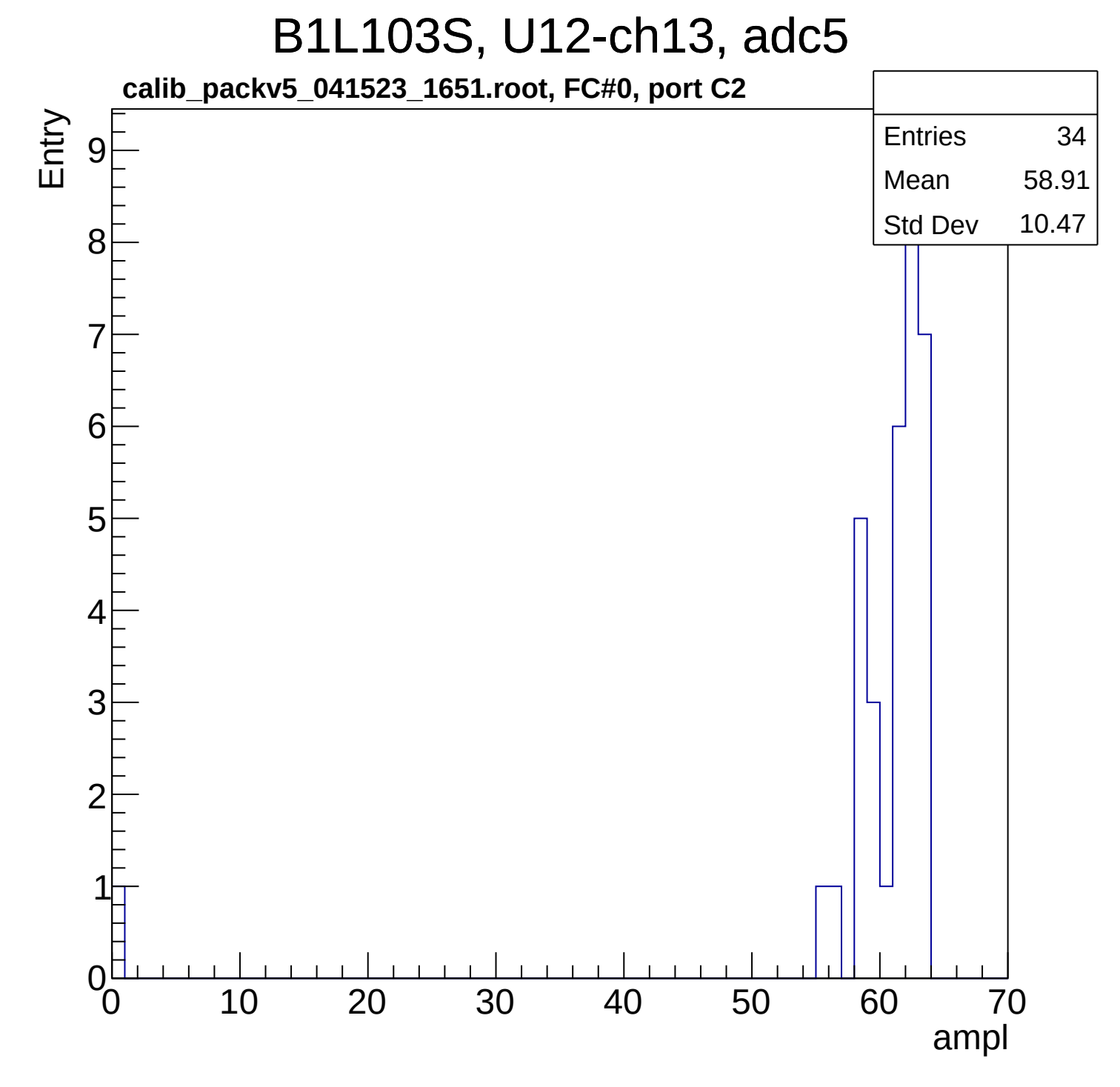
B1L103S, U12-ch13, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 58.91
Std Dev 10.47
Entry
ampl
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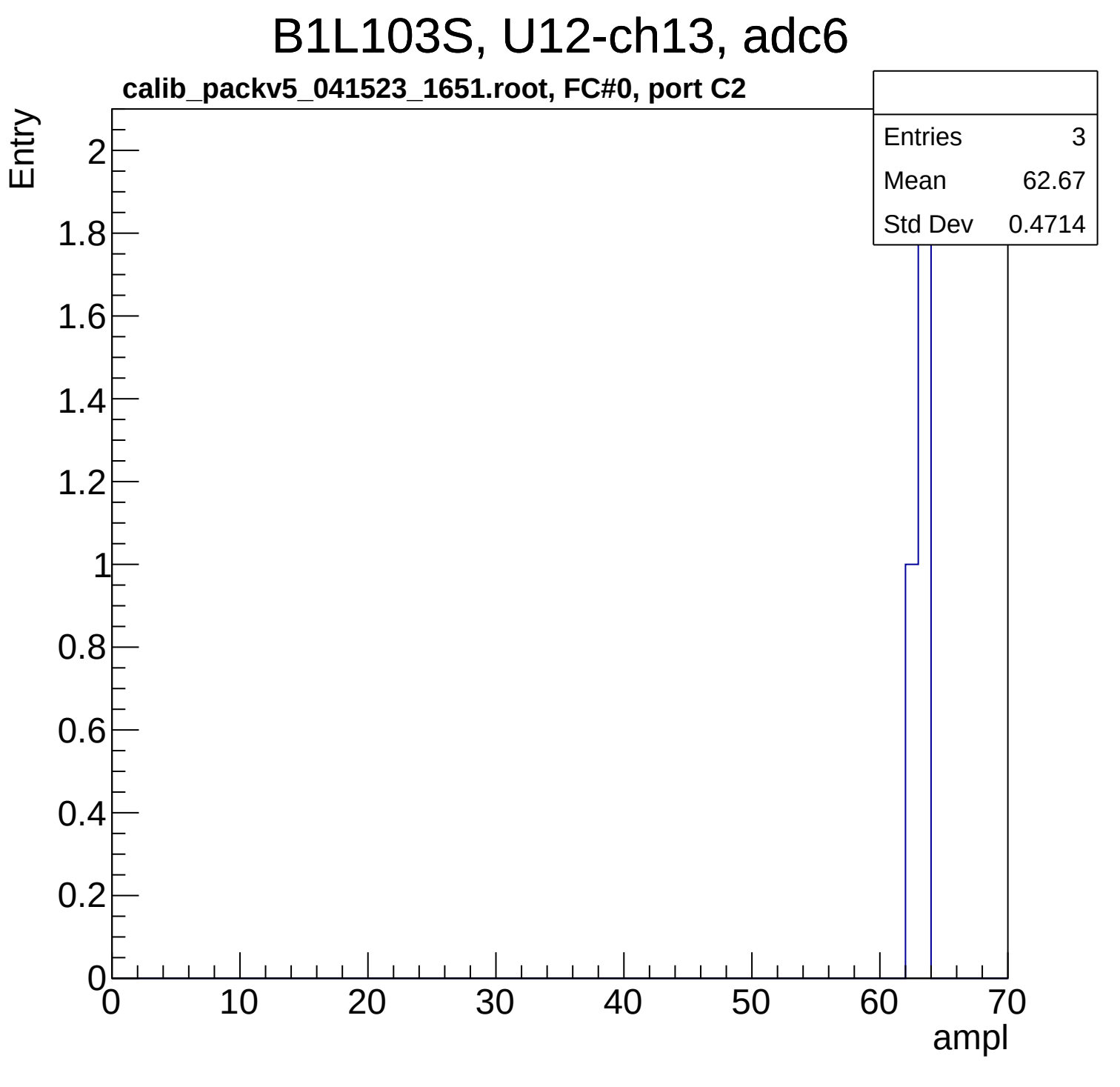
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U12-ch13, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
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1.2
1.4
1.6
1.8
2
0
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20
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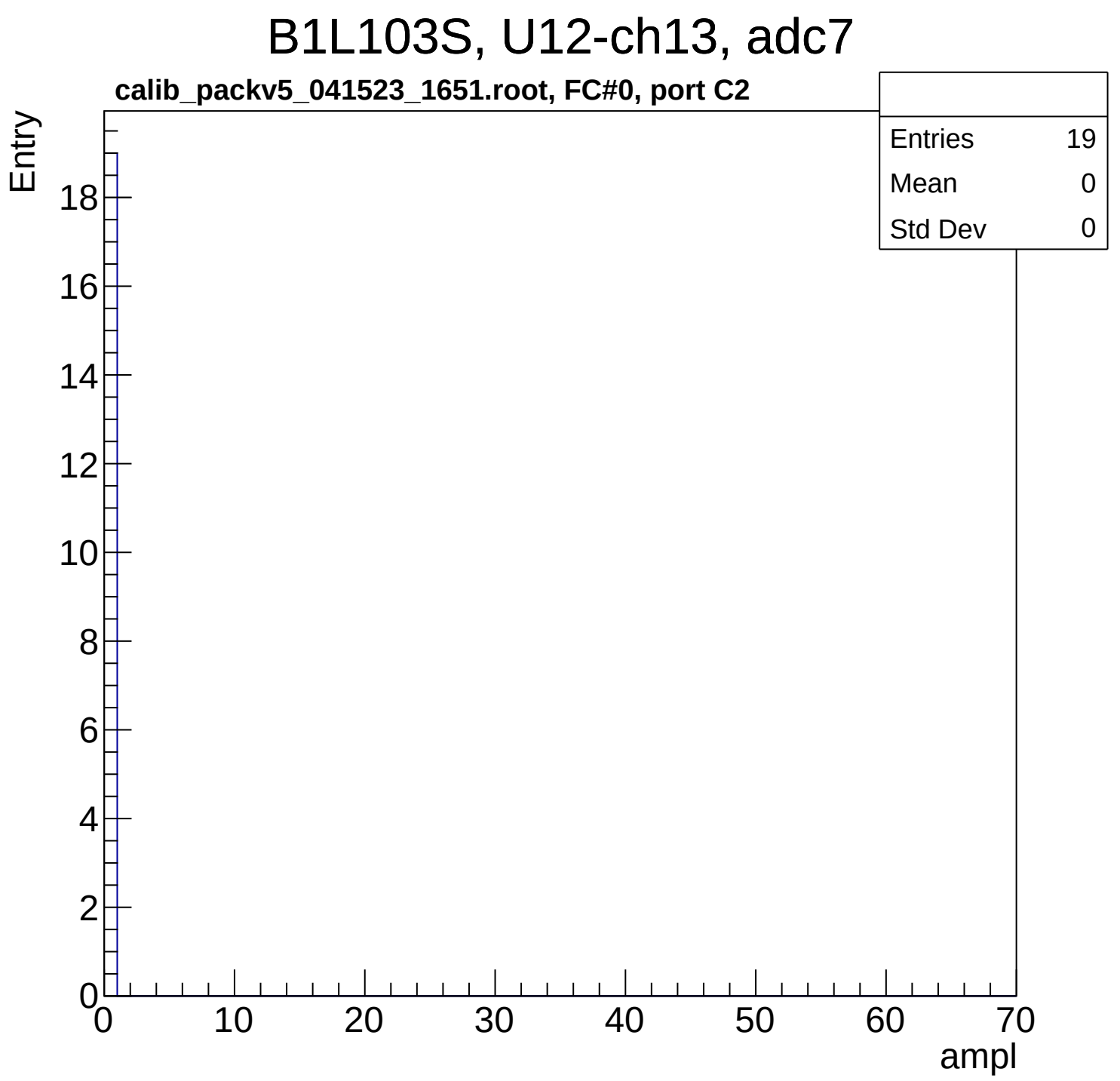
40
50
60
70


B1L103S, U12-ch13, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
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30
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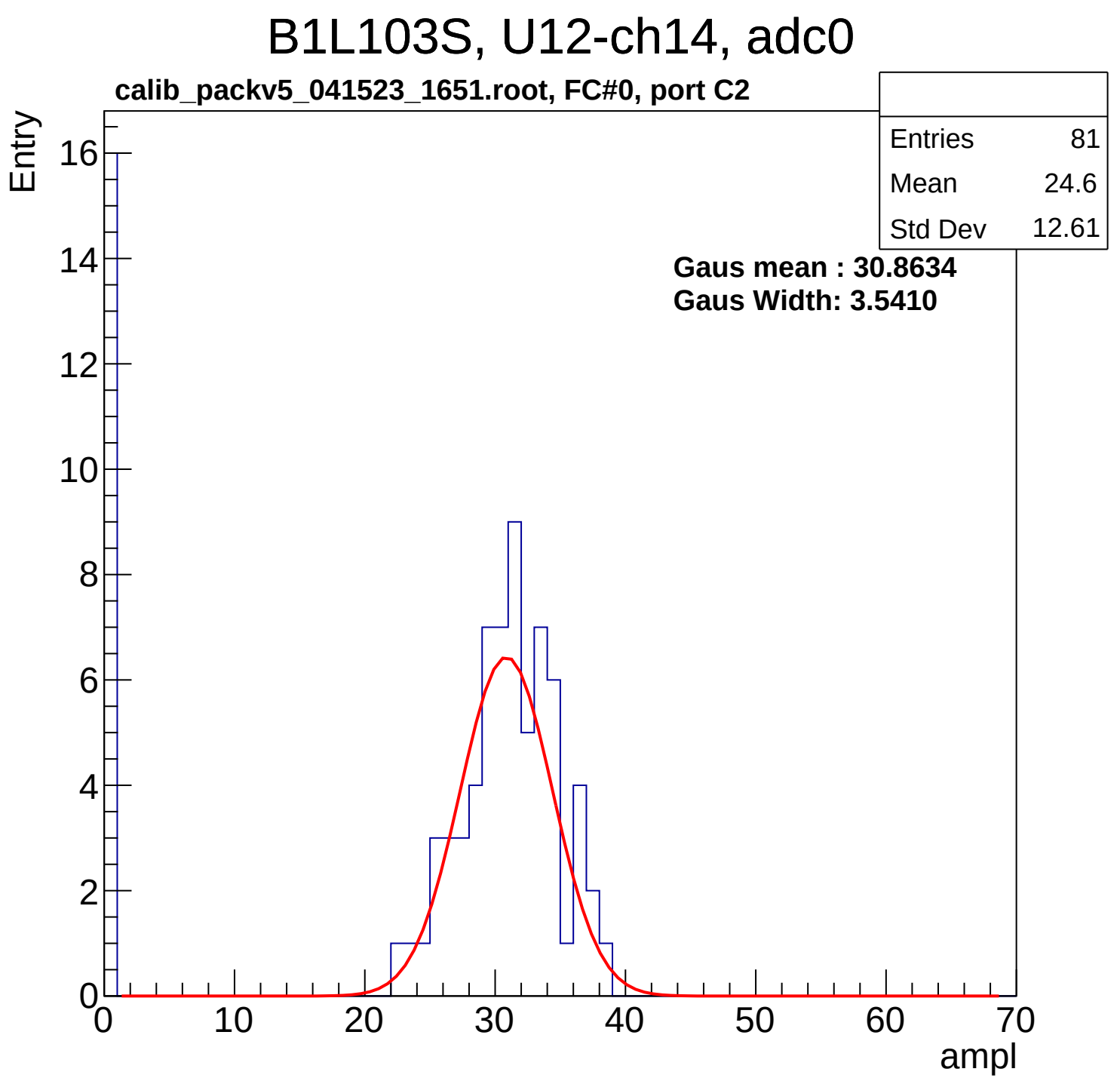
50
60
70
ampl


B1L103S, U12-ch14, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 24.6
Std Dev 12.61
Gaus mean : 30.8634
Gaus Width: 3.5410
Entry
ampl
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2
4
6
8
10
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0
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60
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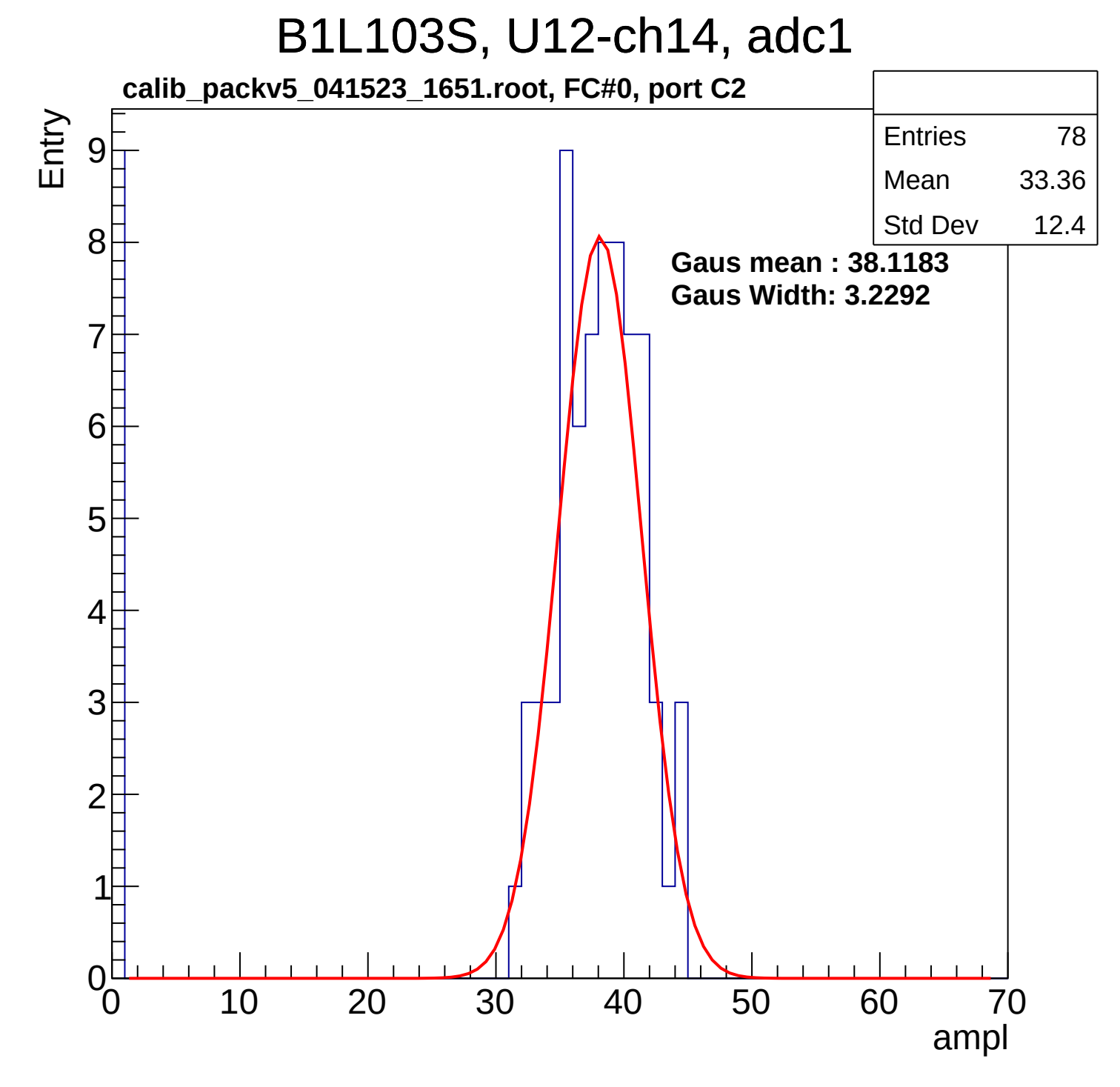
B1L103S, U12-ch14, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 33.36
Std Dev 12.4
Gaus mean : 38.1183
Gaus Width: 3.2292
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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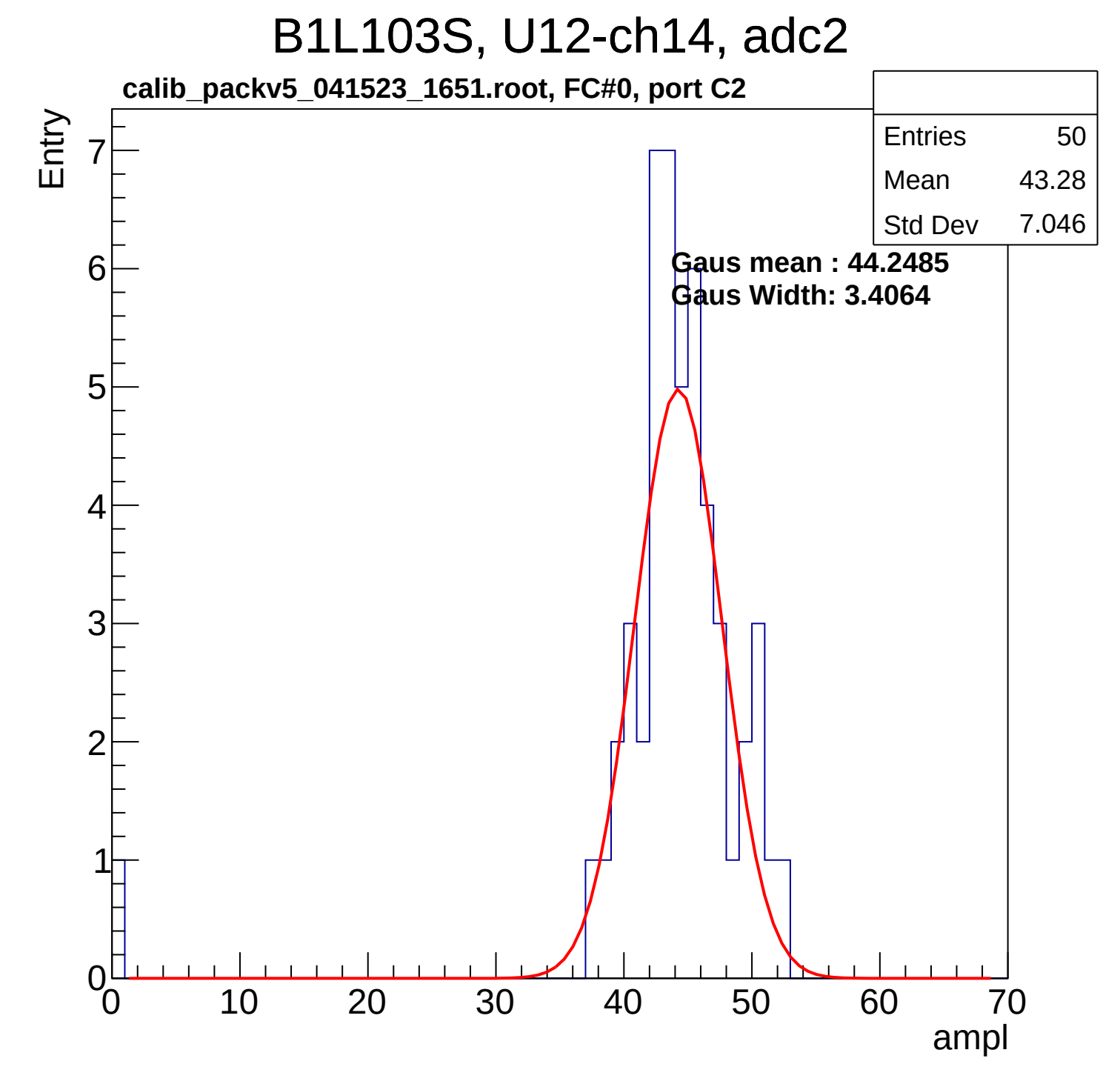
B1L103S, U12-ch14, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 43.28
Std Dev 7.046
Gaus mean : 44.2485
Gaus Width: 3.4064
Entry
ampl
0
1
2
3
4
5
6
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0
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20
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40
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60
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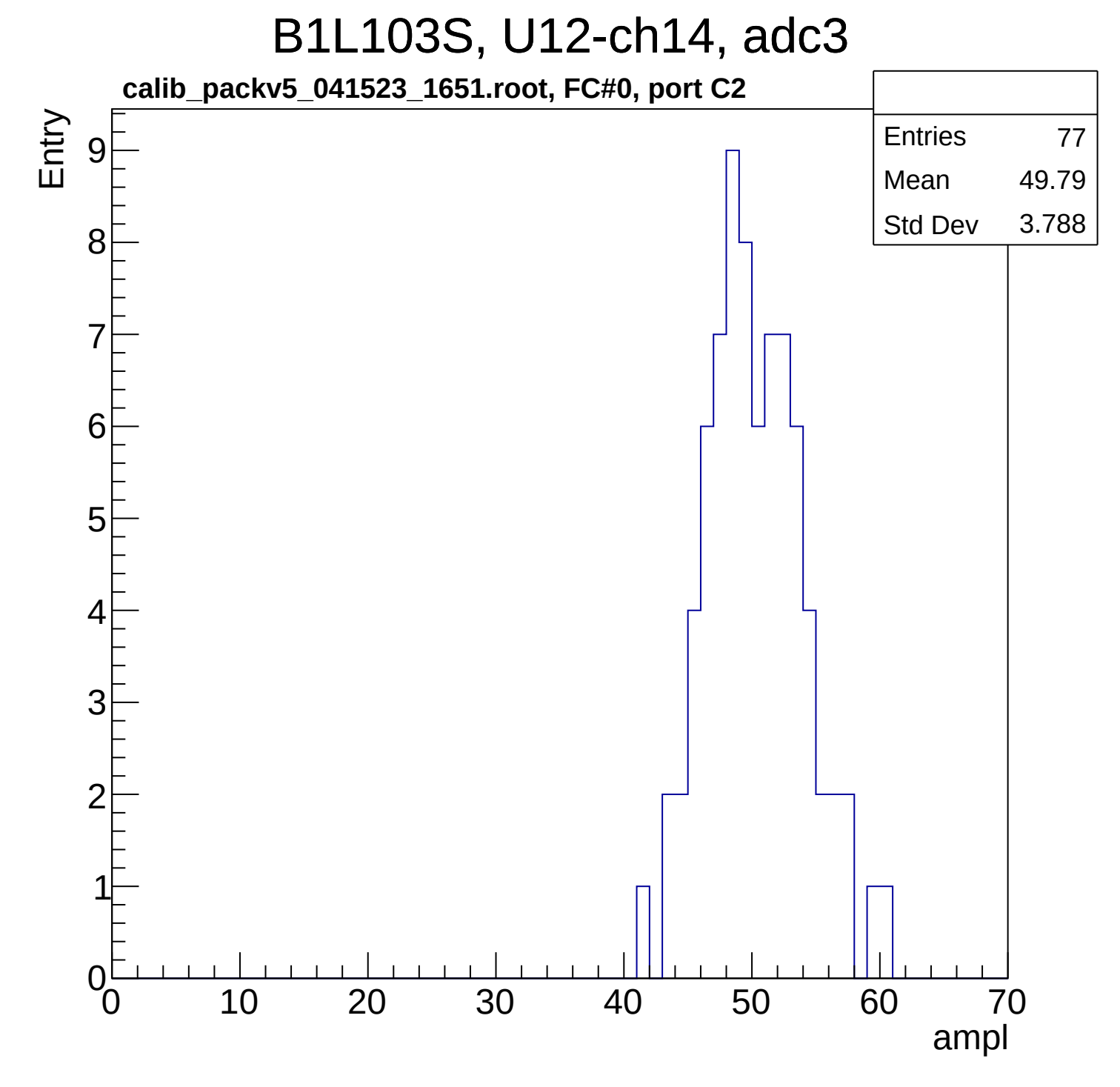
B1L103S, U12-ch14, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 49.79
Std Dev 3.788
Entry
ampl
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30
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50
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1
2
3
4
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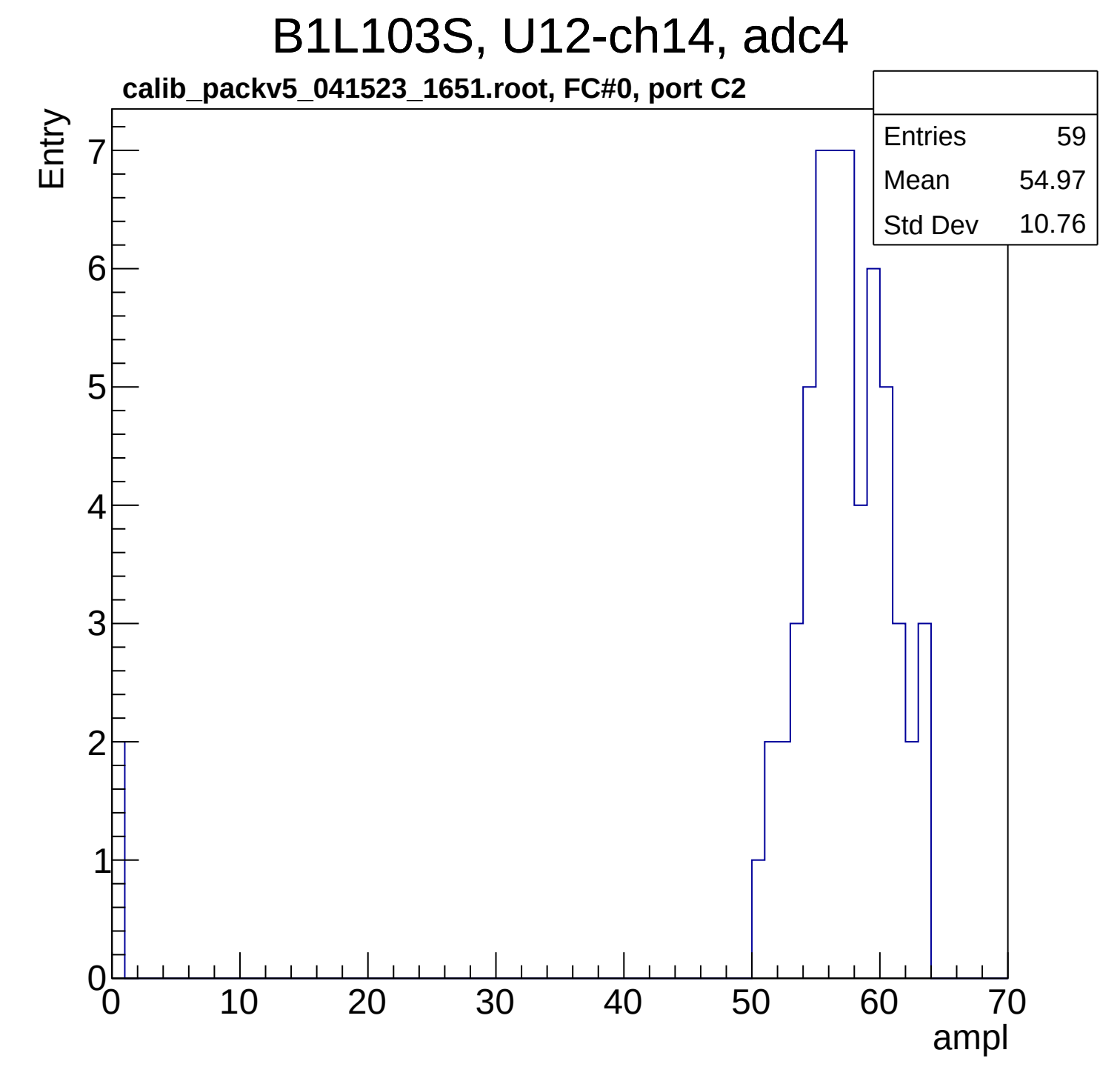
6
7
8
9


B1L103S, U12-ch14, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 54.97
Std Dev 10.76
Entry
ampl
0
1
2
3
4
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0
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40
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60
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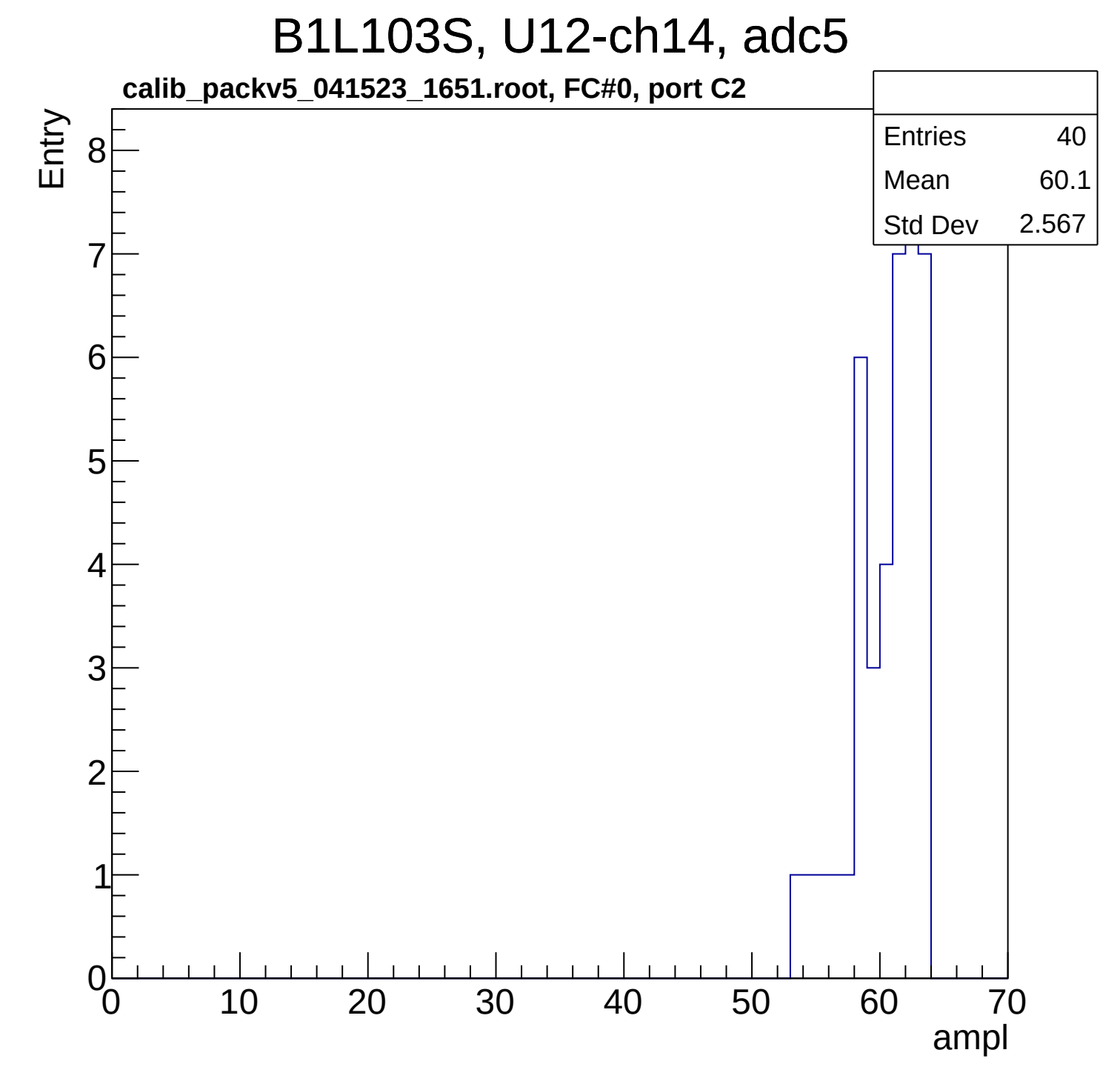
B1L103S, U12-ch14, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 60.1
Std Dev 2.567
Entry
ampl
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2
3
4
5
6
7
8
0
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20
30
40
50
60
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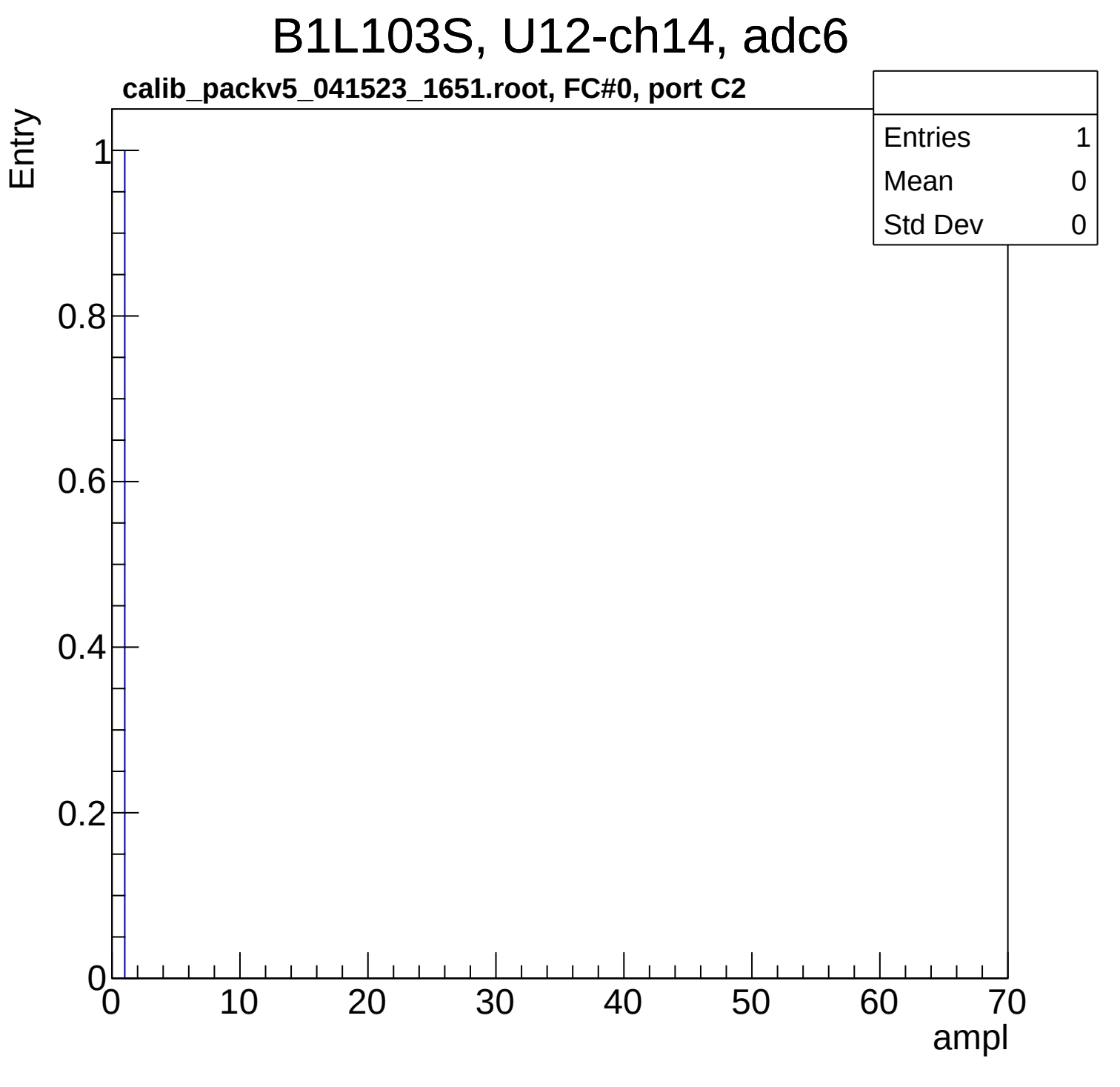
B1L103S, U12-ch14, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 0
Std Dev 0
Entry
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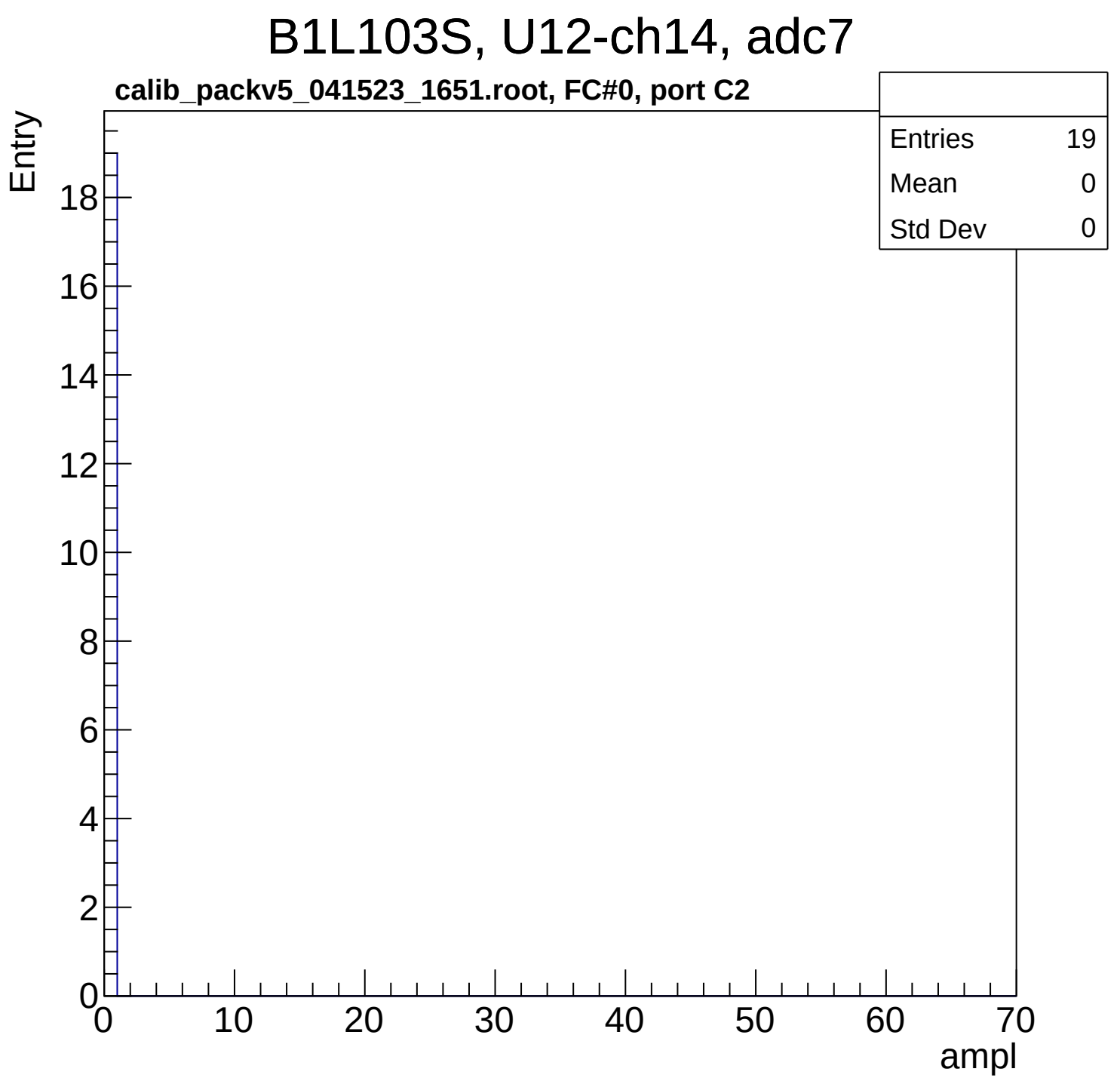
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch14, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
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10
20
30
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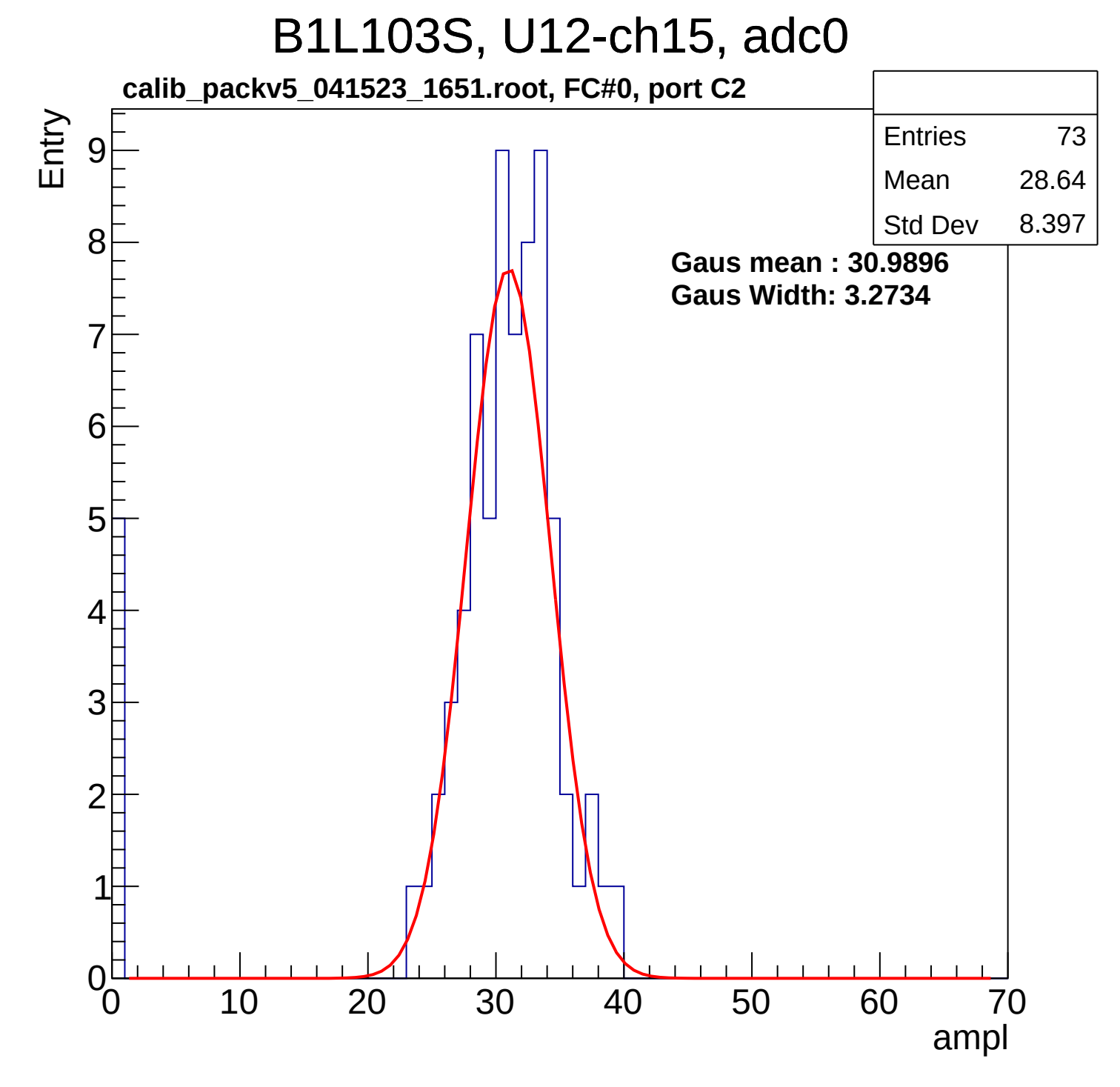
50
60
70
ampl


B1L103S, U12-ch15, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 28.64
Std Dev 8.397
Gaus mean : 30.9896
Gaus Width: 3.2734
Entry
ampl
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2
3
4
5
6
7
8
9
0
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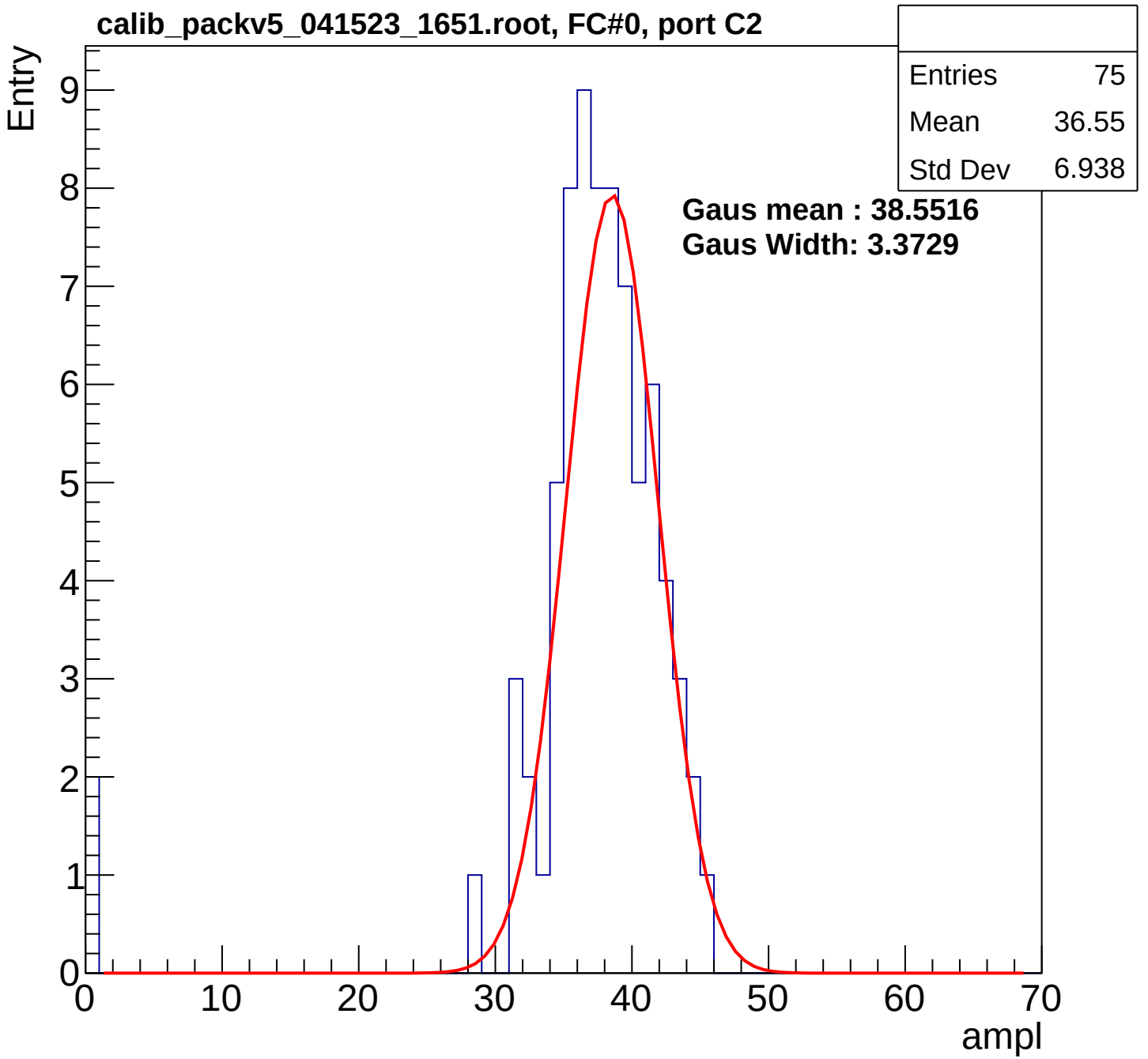
B1L103S, U12-ch15, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 36.55
Std Dev 6.938
Gaus mean : 38.5516
Gaus Width: 3.3729
Entry
ampl
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3
4
5
6
7
8
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0
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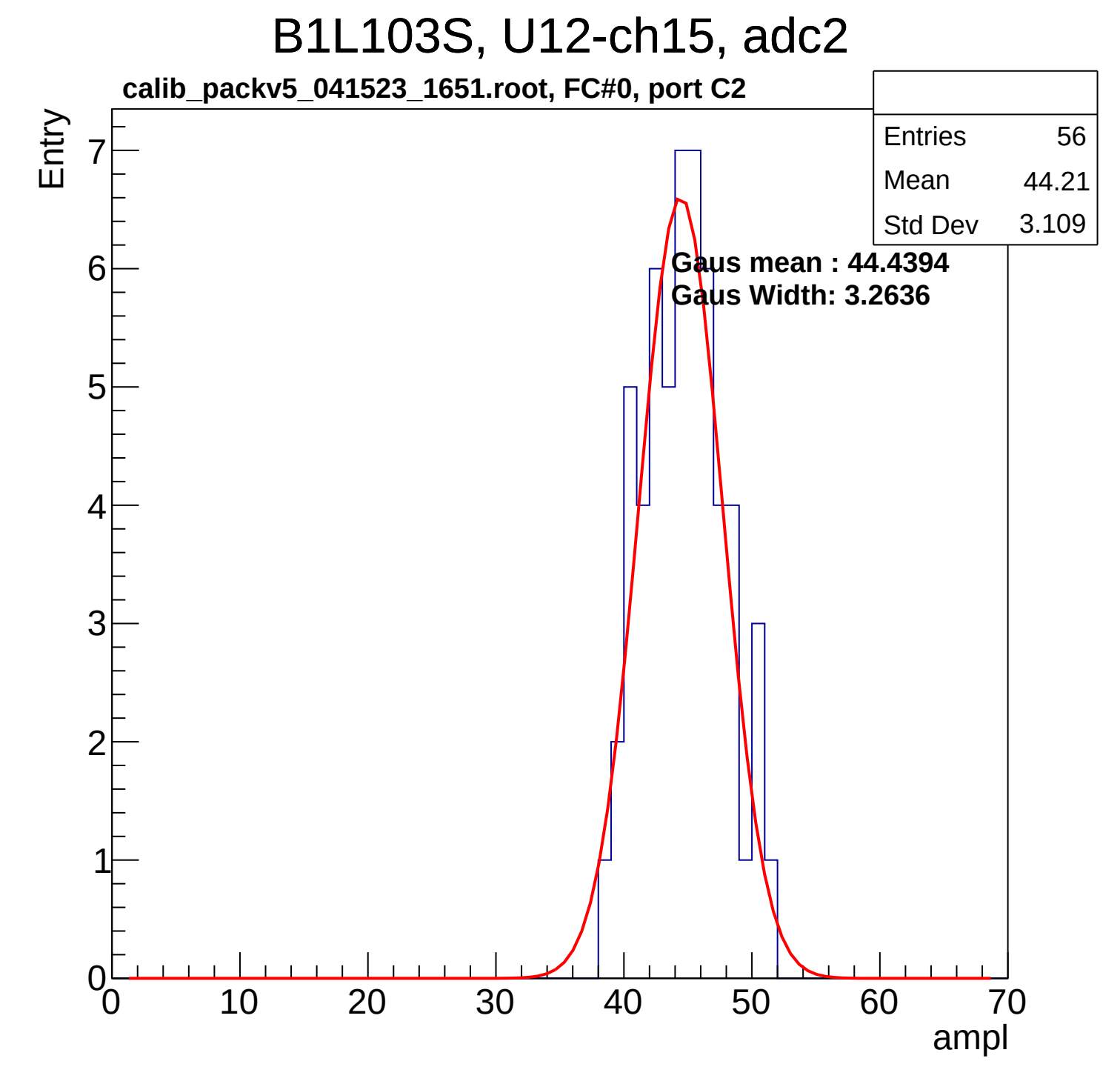
B1L103S, U12-ch15, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 44.21
Std Dev 3.109
Gaus mean : 44.4394
Gaus Width: 3.2636
Entry
ampl
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3
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0
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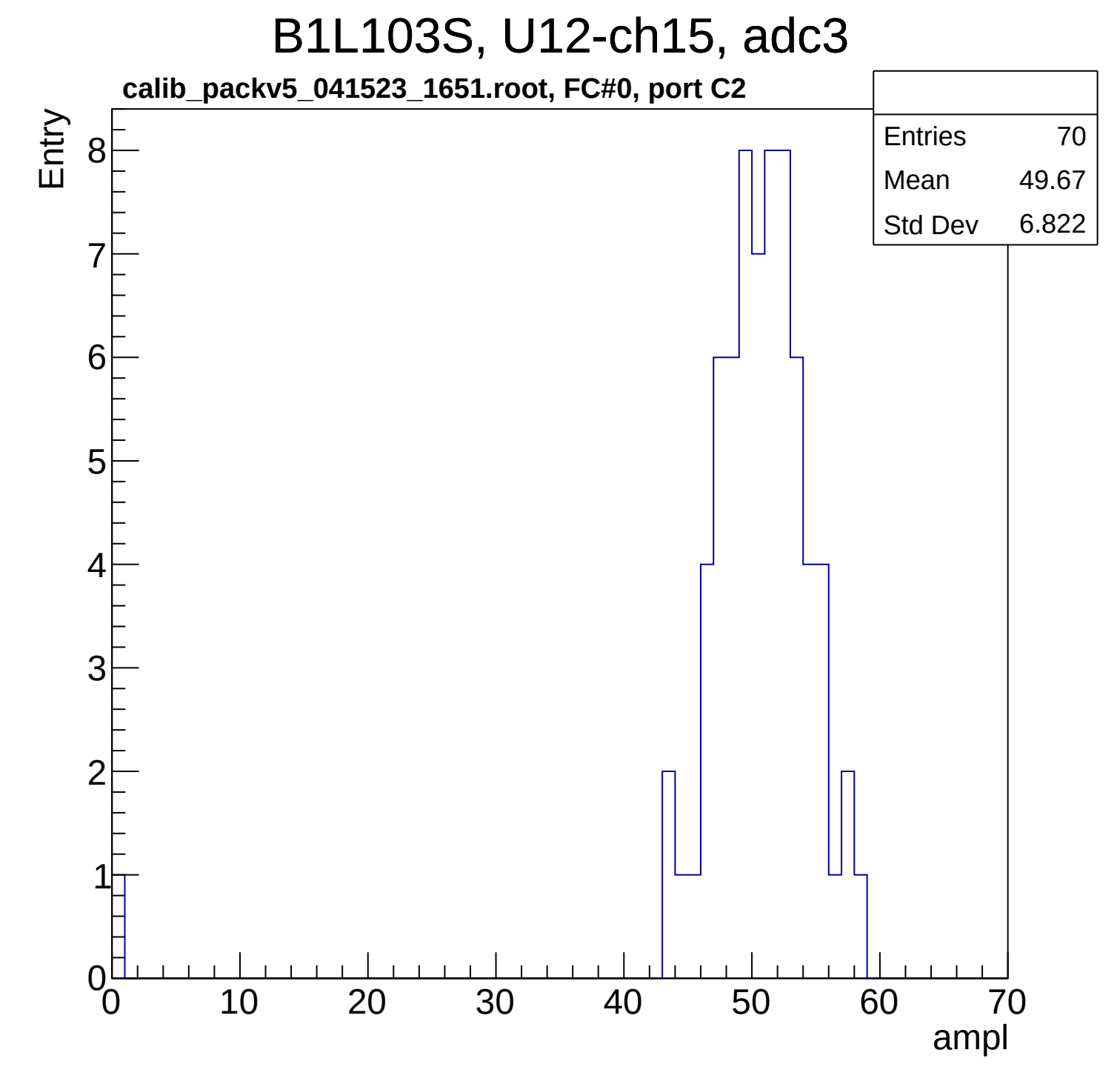
B1L103S, U12-ch15, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 49.67
Std Dev 6.822
Entry
ampl
0
1
2
3
4
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0
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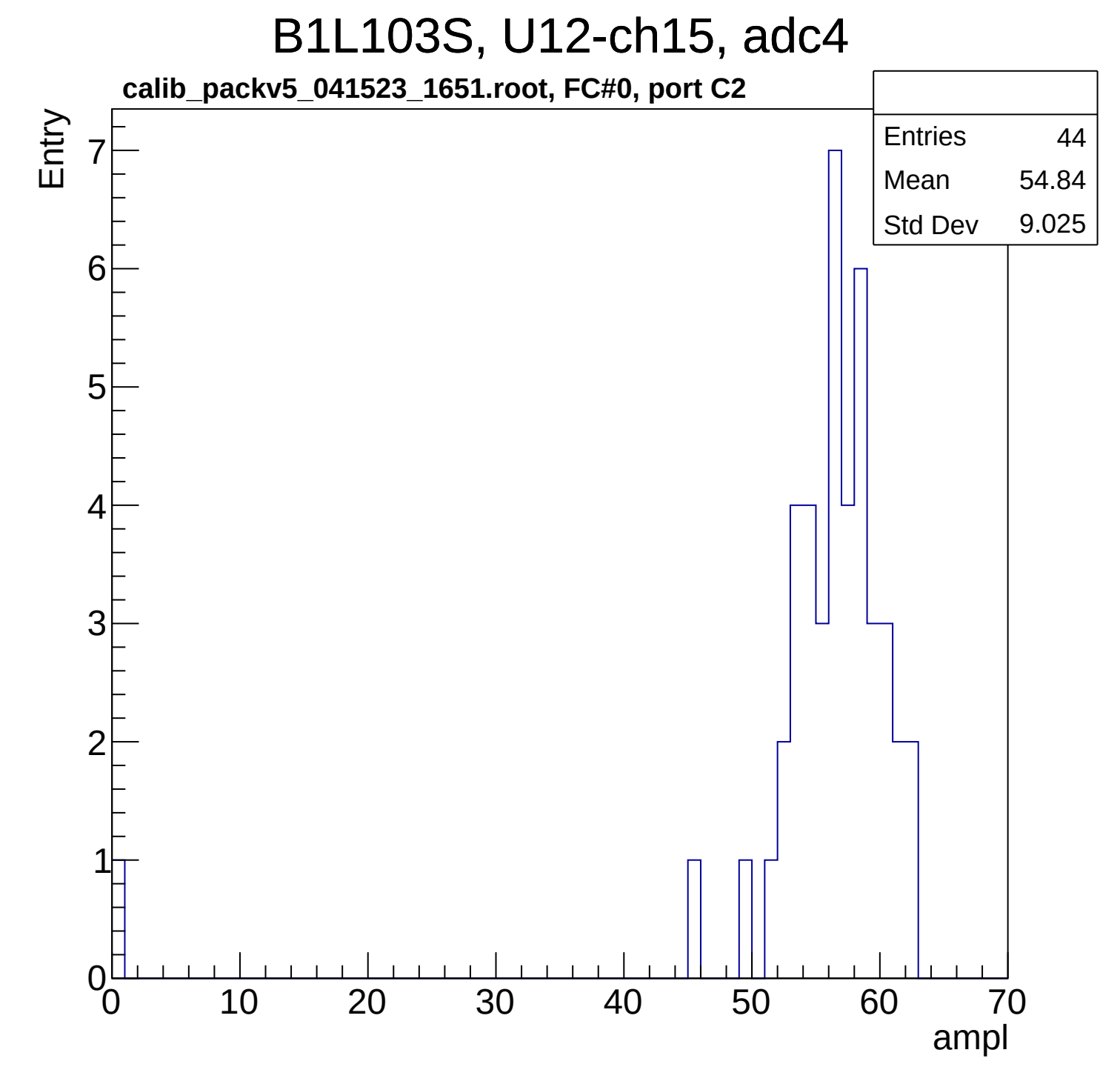
B1L103S, U12-ch15, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 54.84
Std Dev 9.025
Entry
ampl
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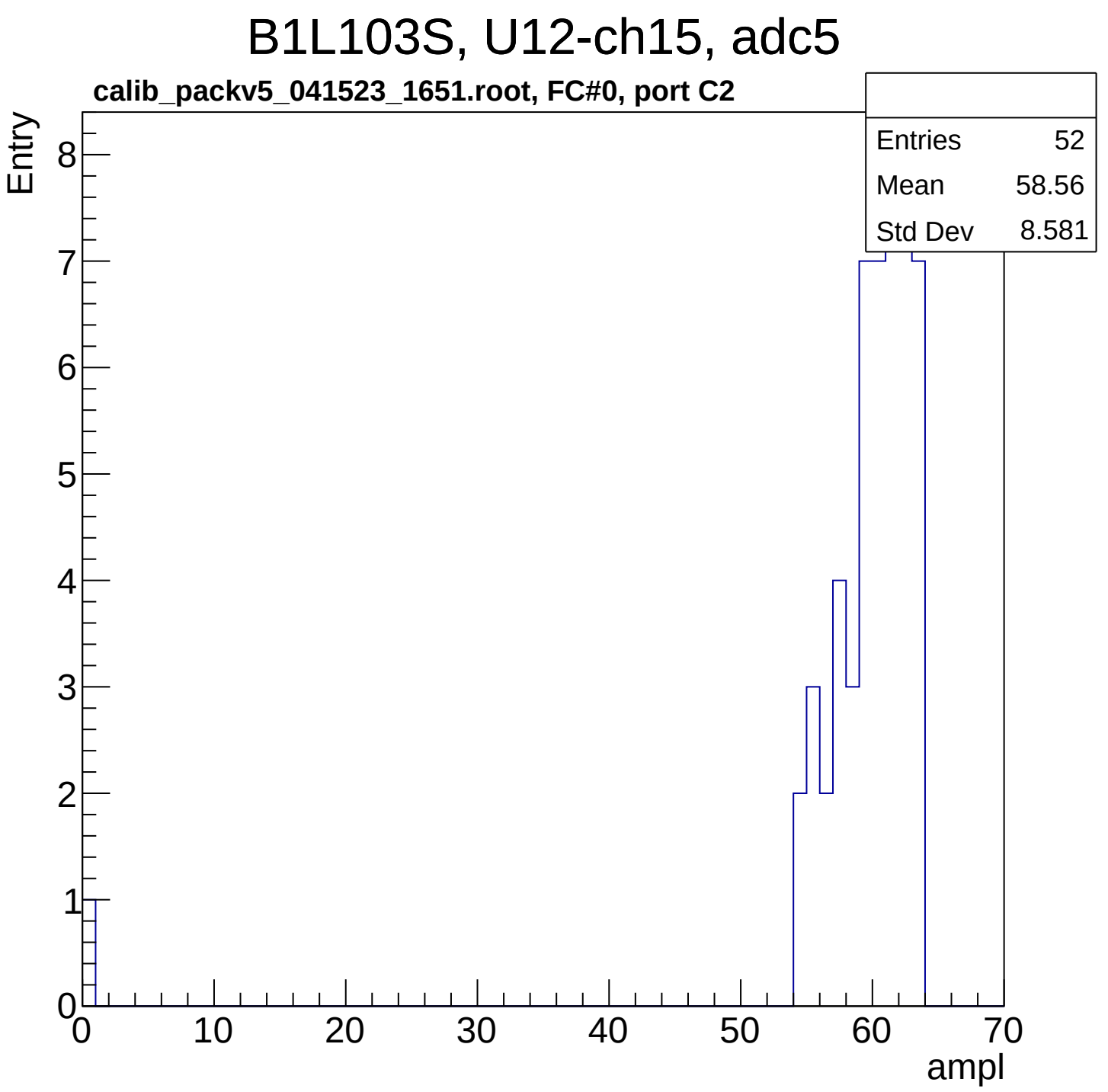
B1L103S, U12-ch15, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.56
Std Dev 8.581
Entry
ampl
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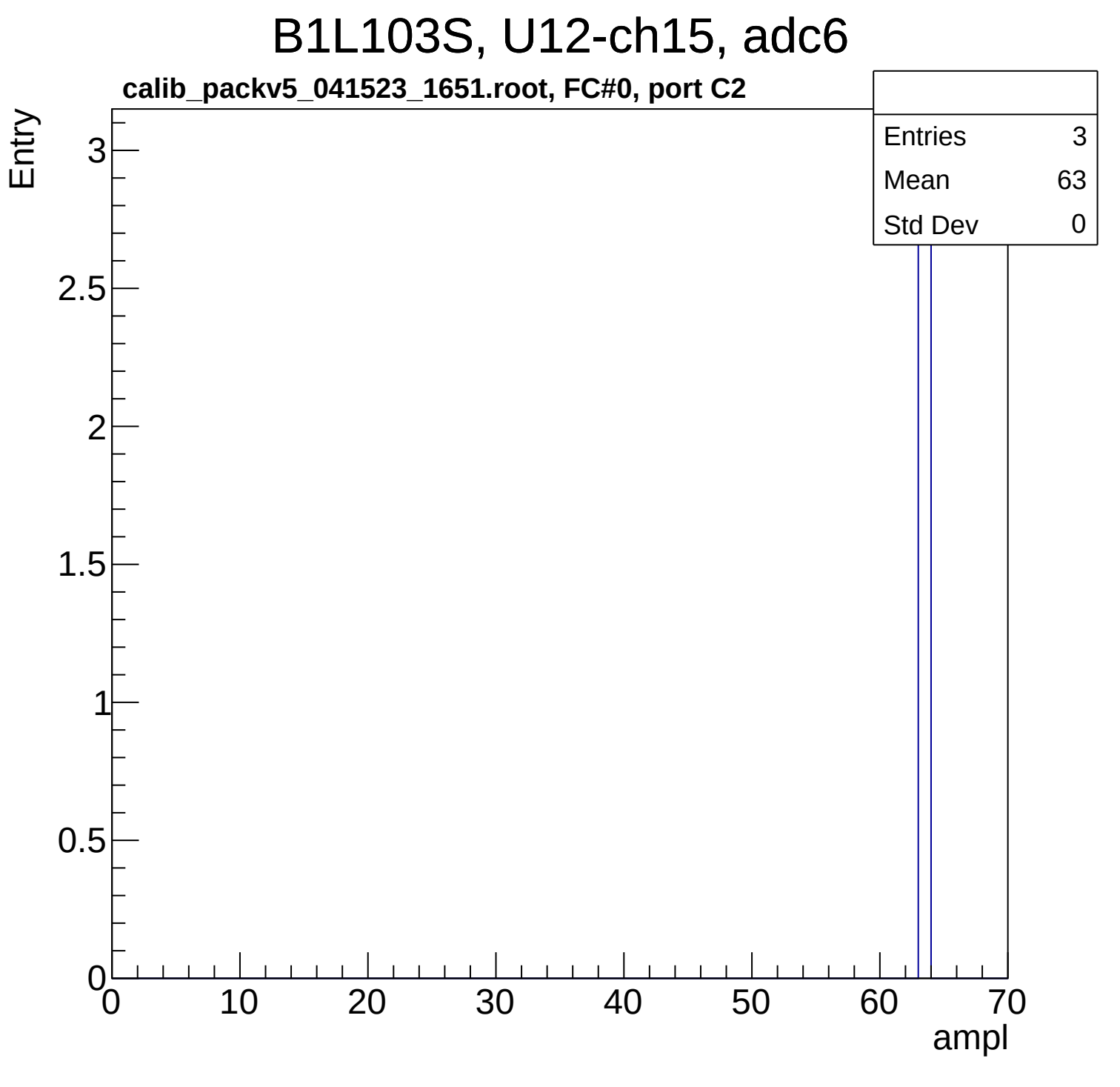
B1L103S, U12-ch15, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 63
Std Dev 0
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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40
50
60
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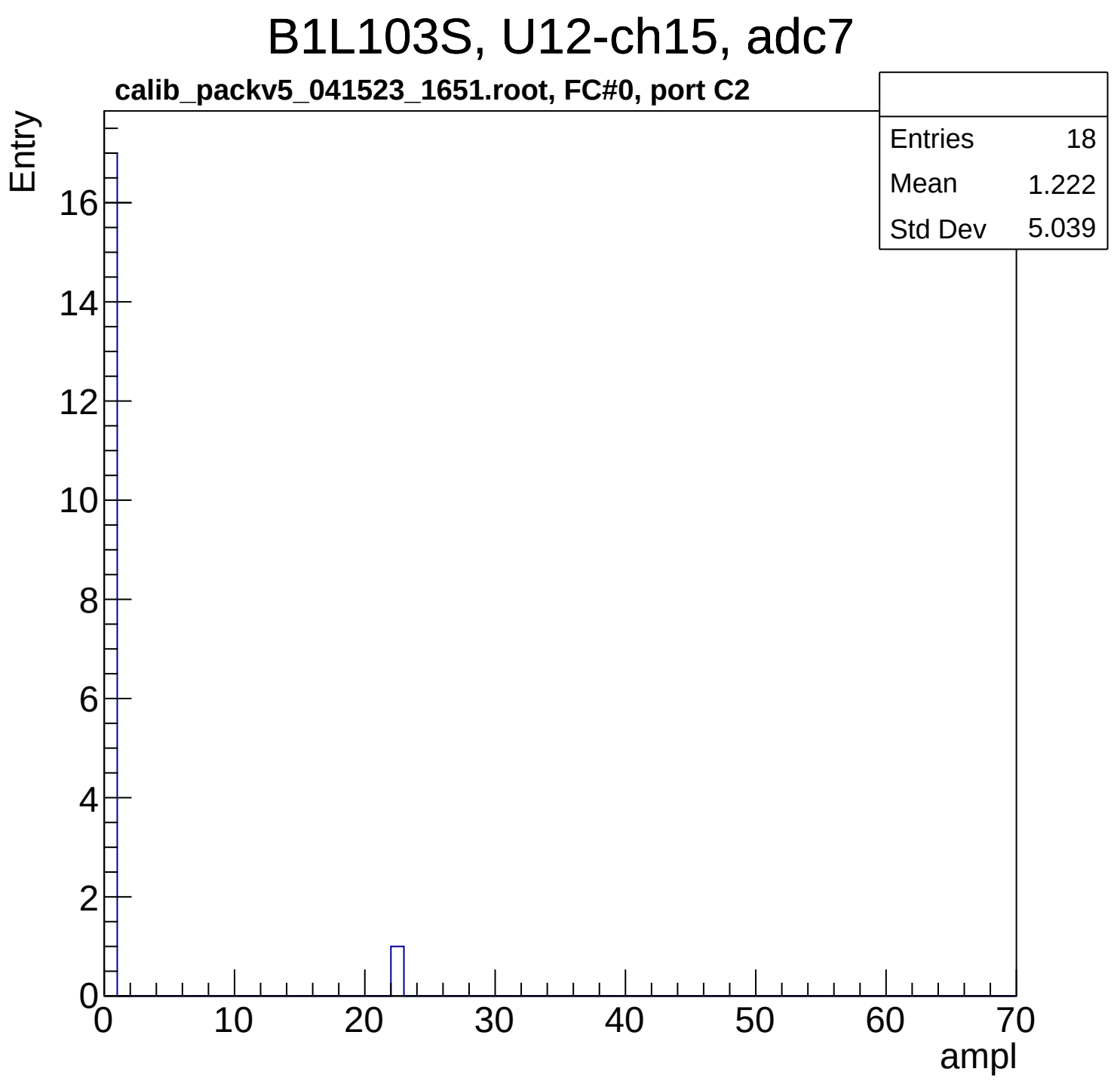
B1L103S, U12-ch15, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.222
Std Dev 5.039
Entry
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12
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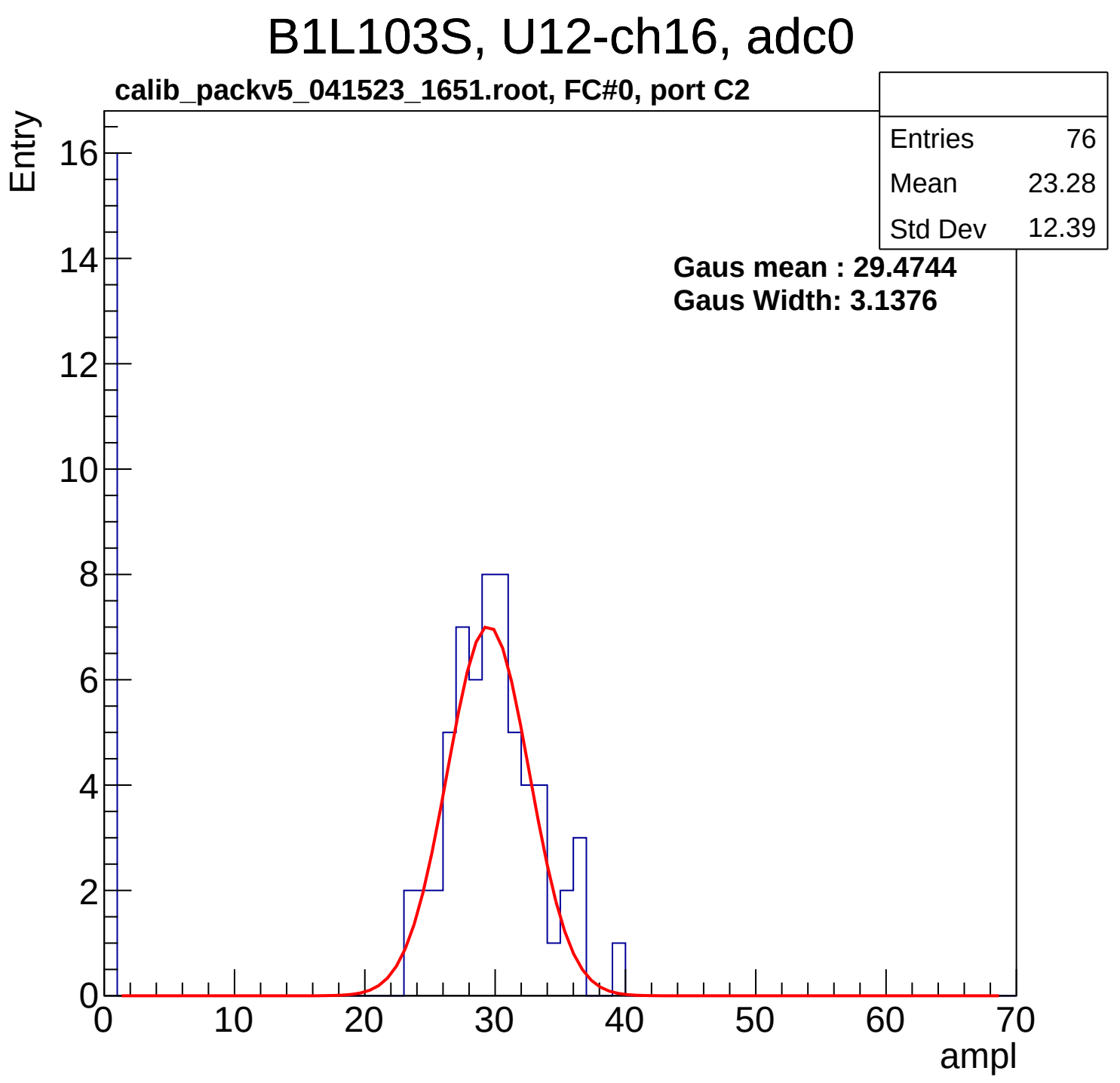
70
ampl


B1L103S, U12-ch16, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 23.28
Std Dev 12.39
Gaus mean : 29.4744
Gaus Width: 3.1376
Entry
ampl
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2
4
6
8
10
12
14
16
0
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40
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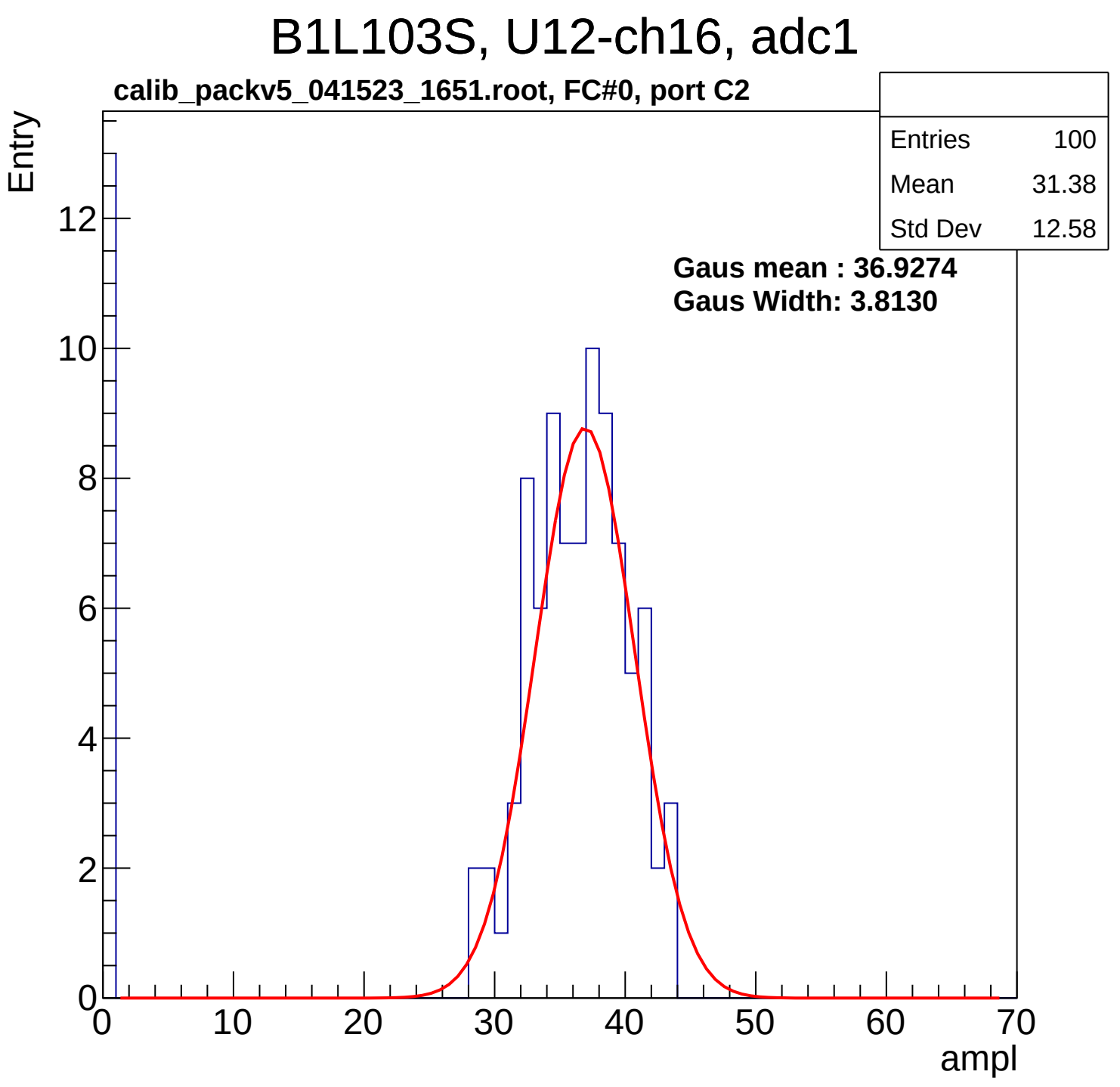
B1L103S, U12-ch16, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 31.38
Std Dev 12.58
Gaus mean : 36.9274
Gaus Width: 3.8130
Entry
ampl
0
2
4
6
8
10
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0
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60
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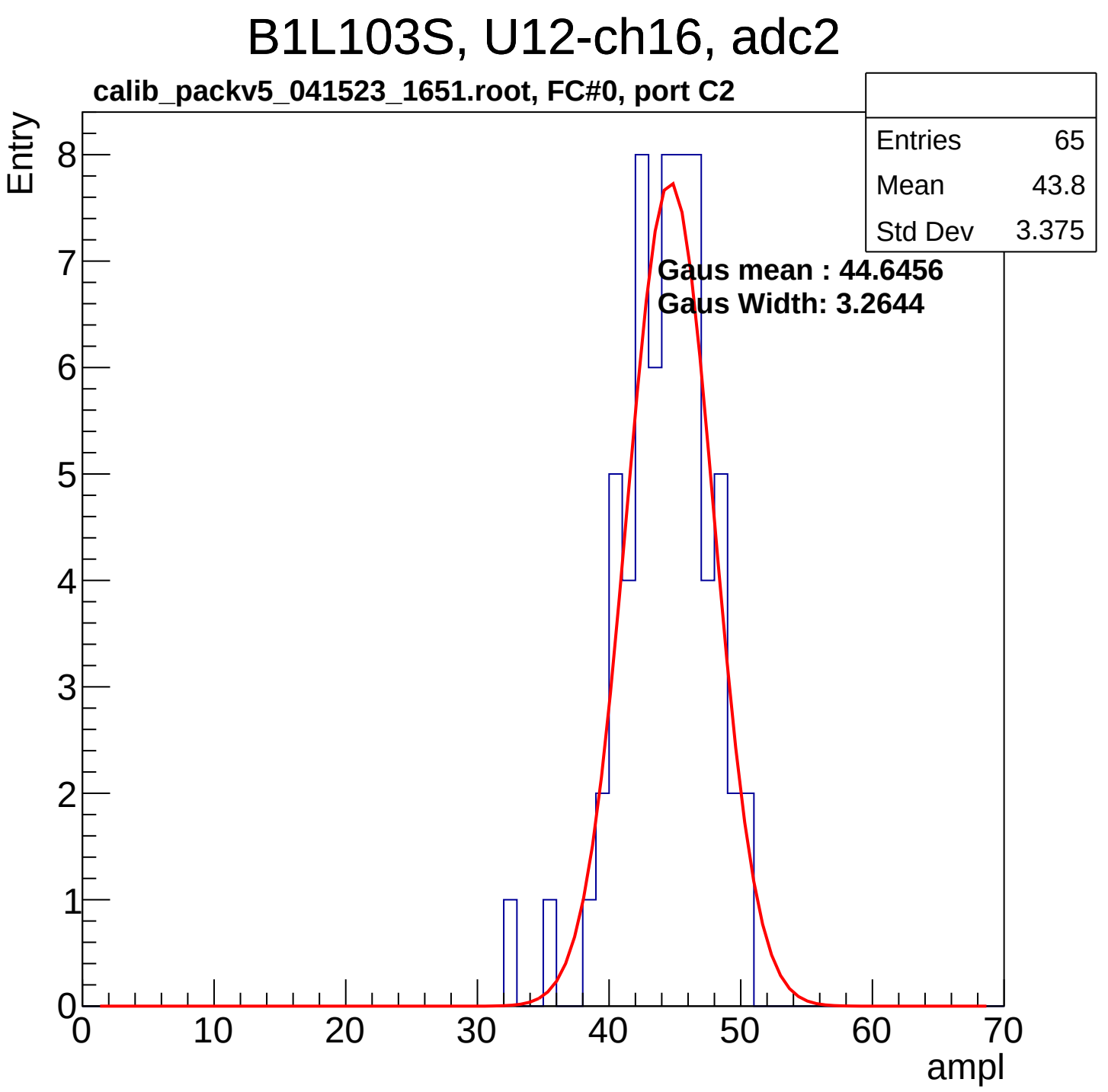
B1L103S, U12-ch16, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 43.8
Std Dev 3.375
Gaus mean : 44.6456
Gaus Width: 3.2644
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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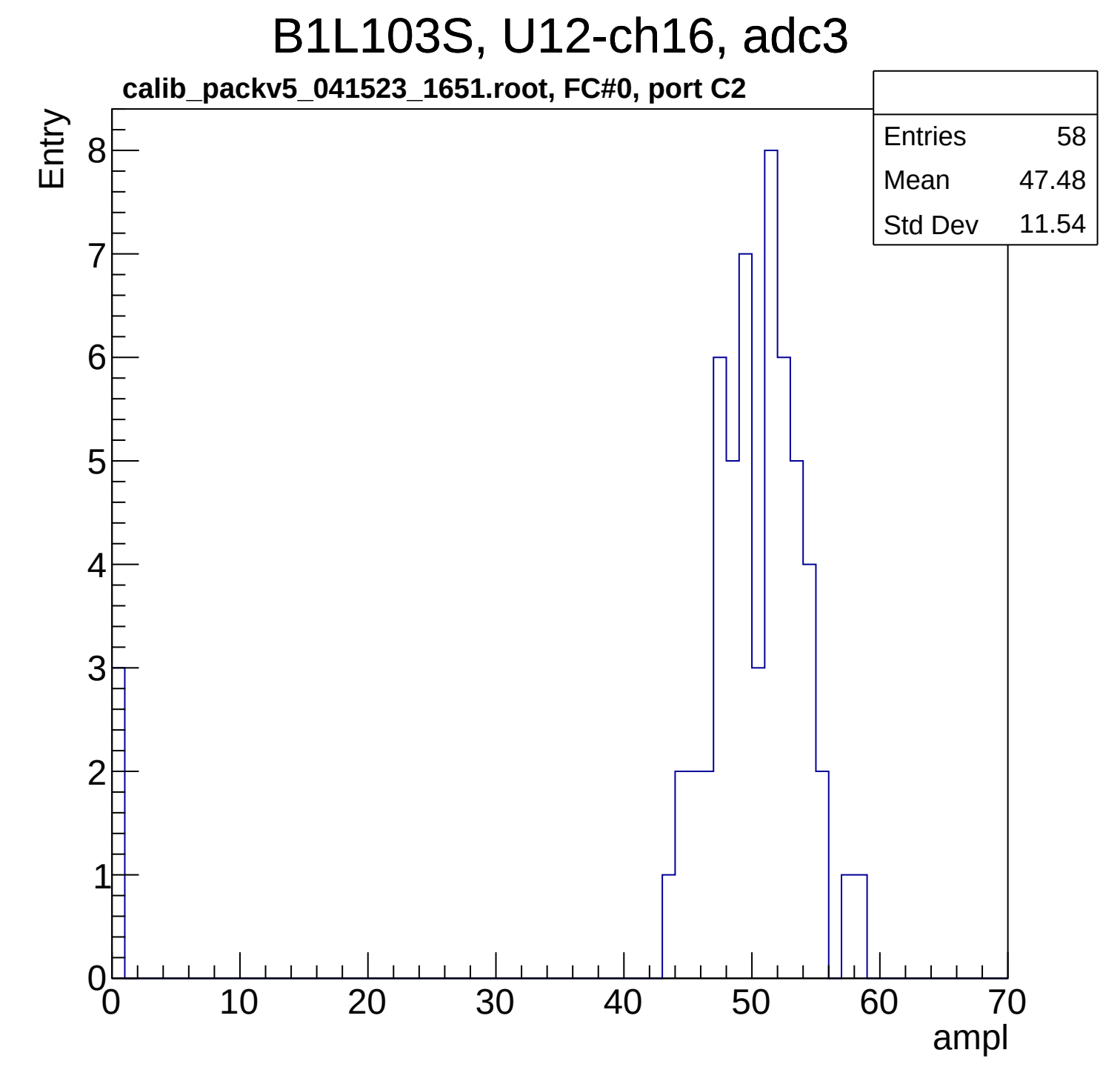
B1L103S, U12-ch16, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 47.48
Std Dev 11.54
Entry
ampl
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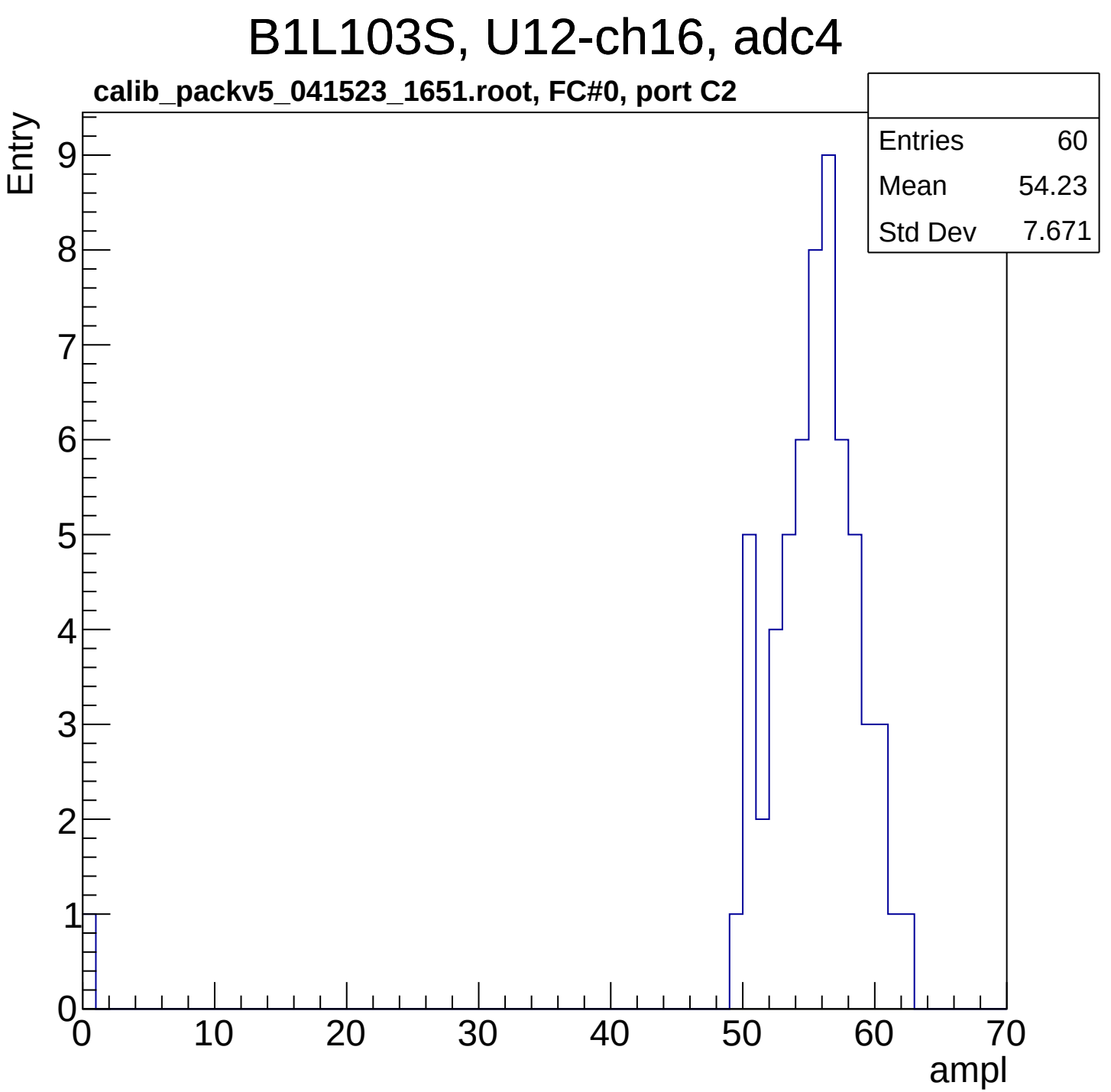
B1L103S, U12-ch16, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 54.23
Std Dev 7.671
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
50
60
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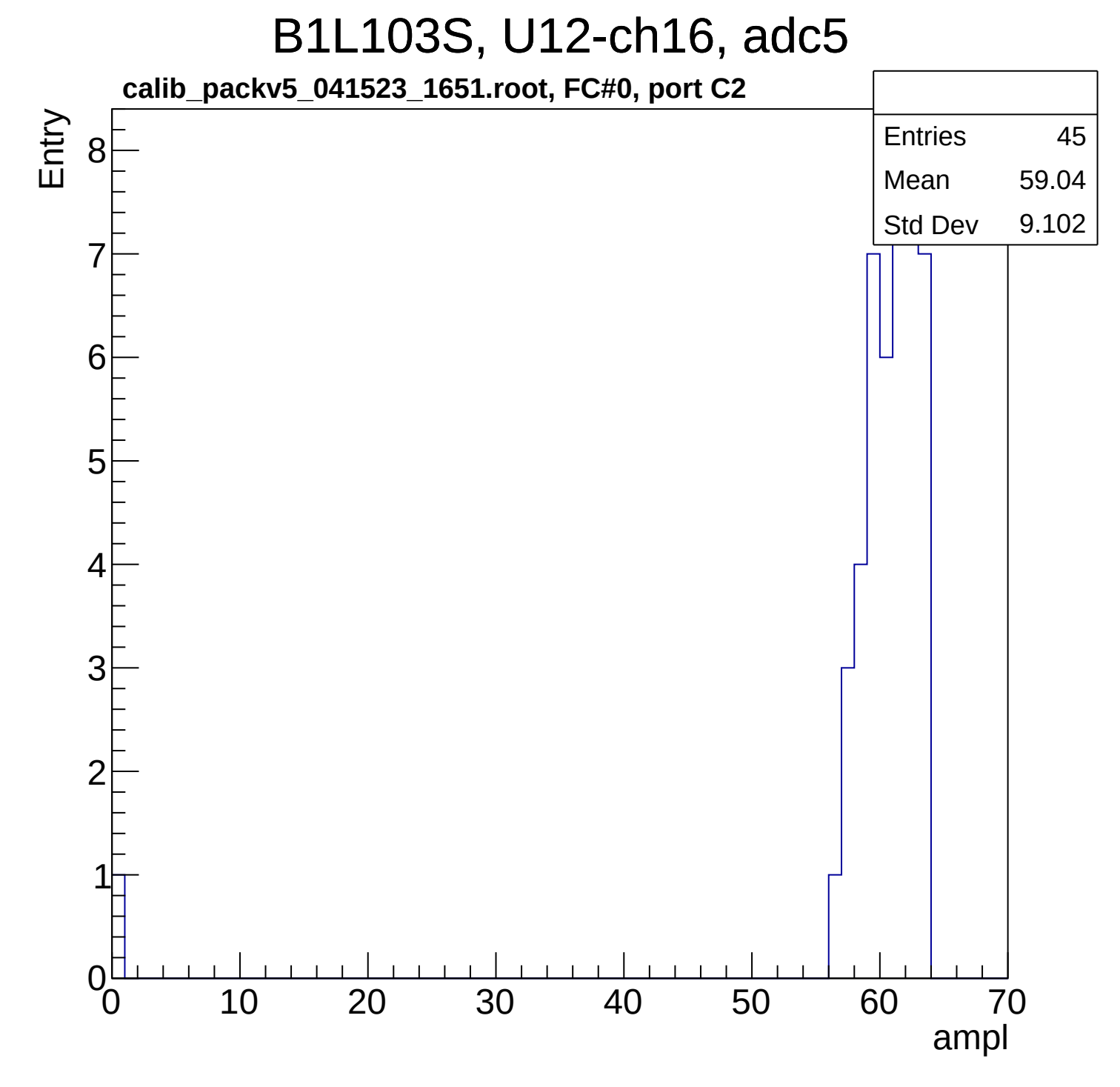
B1L103S, U12-ch16, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 59.04
Std Dev 9.102
Entry
ampl
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2
3
4
5
6
7
8
0
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60
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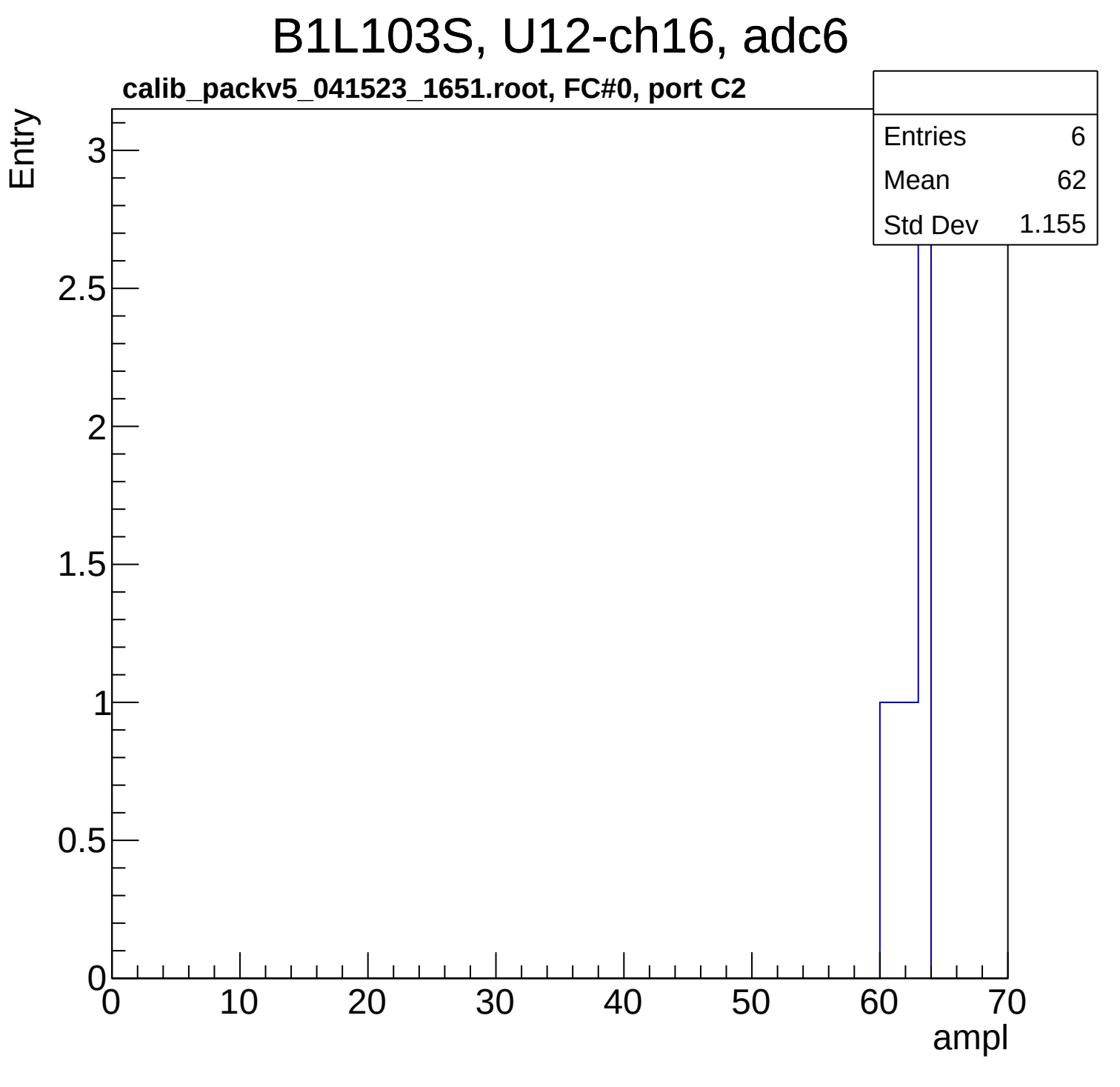
B1L103S, U12-ch16, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62
Std Dev 1.155
Entry
ampl
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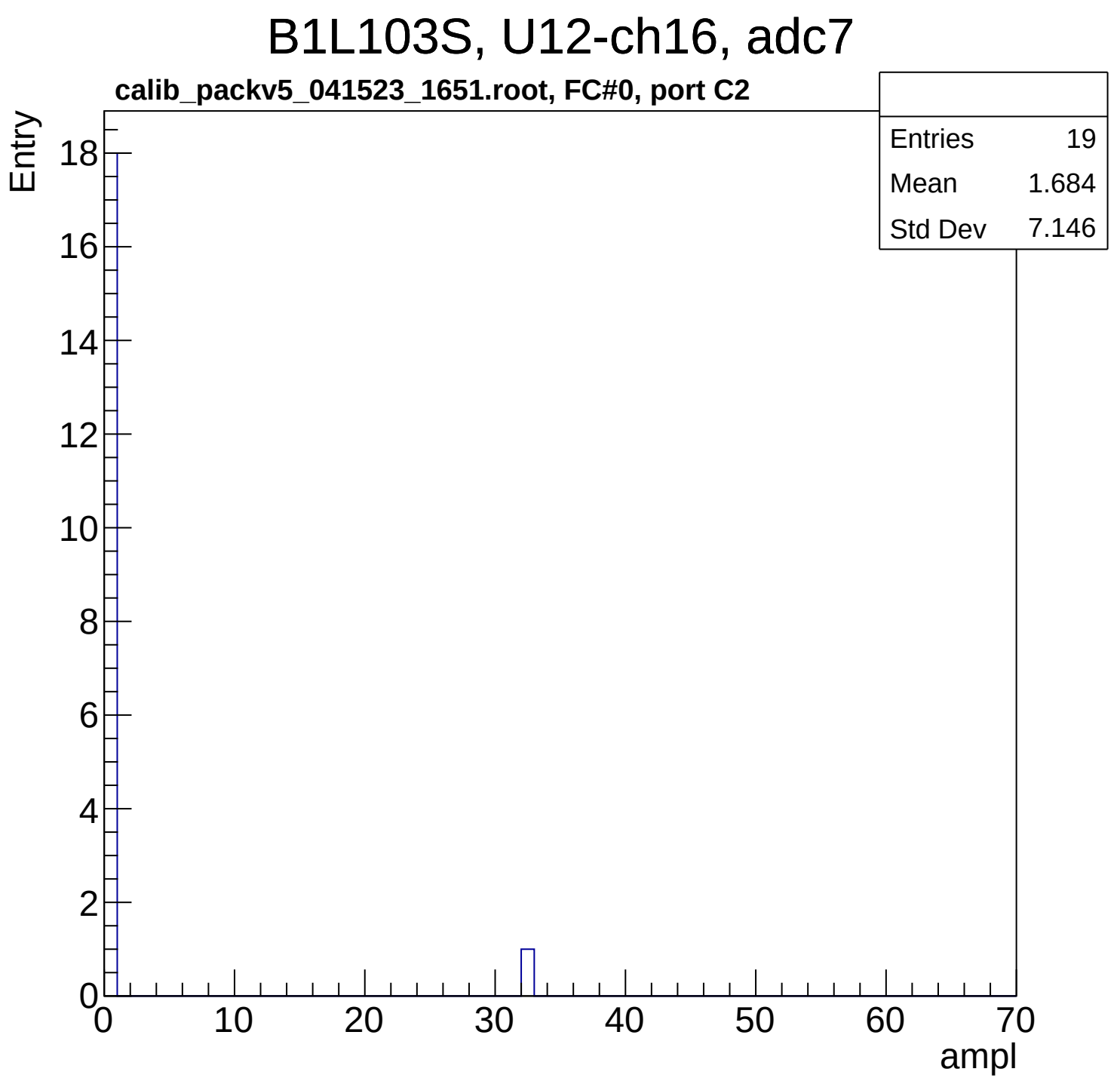
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U12-ch16, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.684
Std Dev 7.146
Entry
0
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6
8
10
12
14
16
18
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10
20
30
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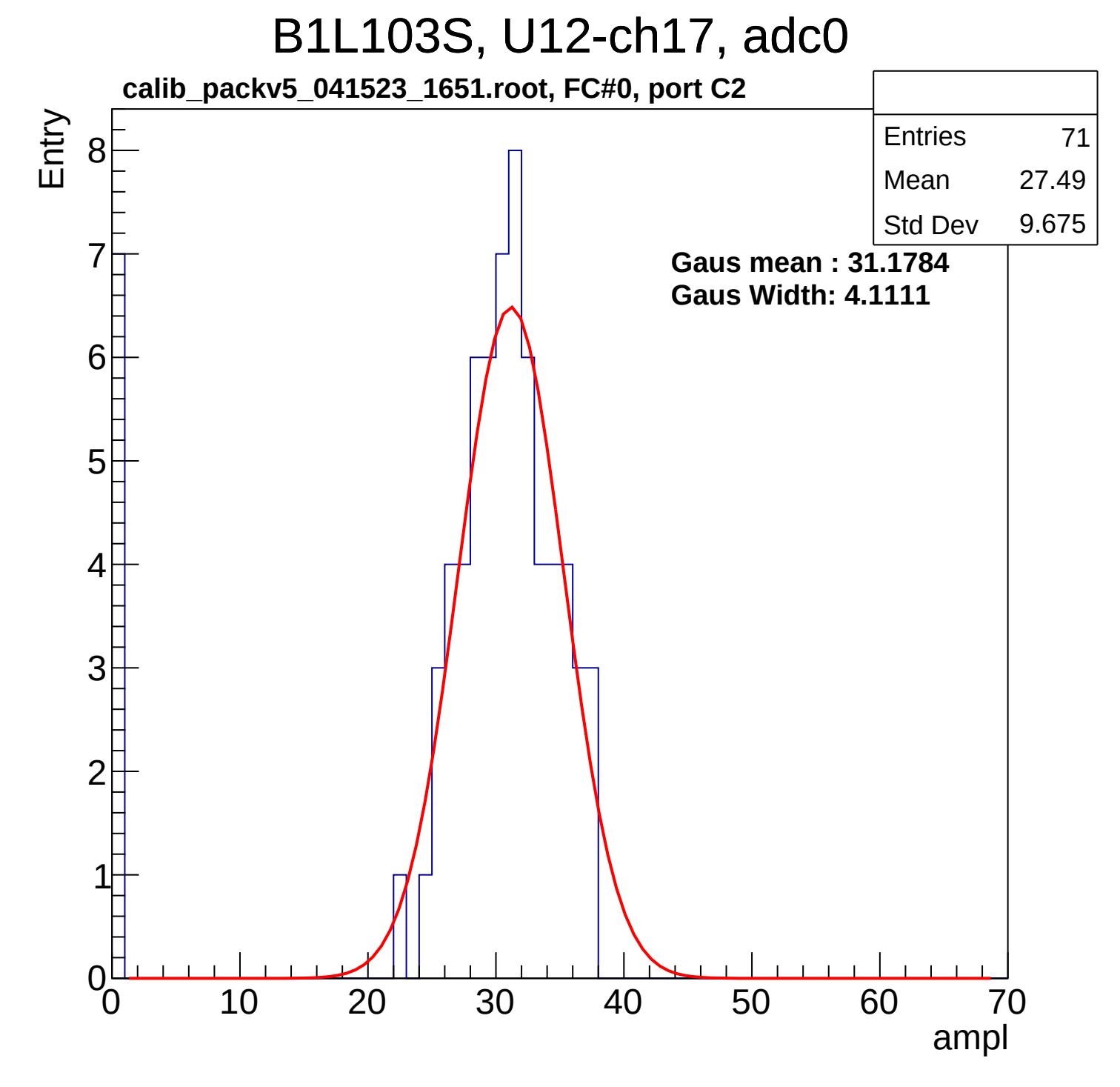
50
60
70
ampl


B1L103S, U12-ch17, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 27.49
Std Dev 9.675
Gaus mean : 31.1784
Gaus Width: 4.1111
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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20
30
40
50
60
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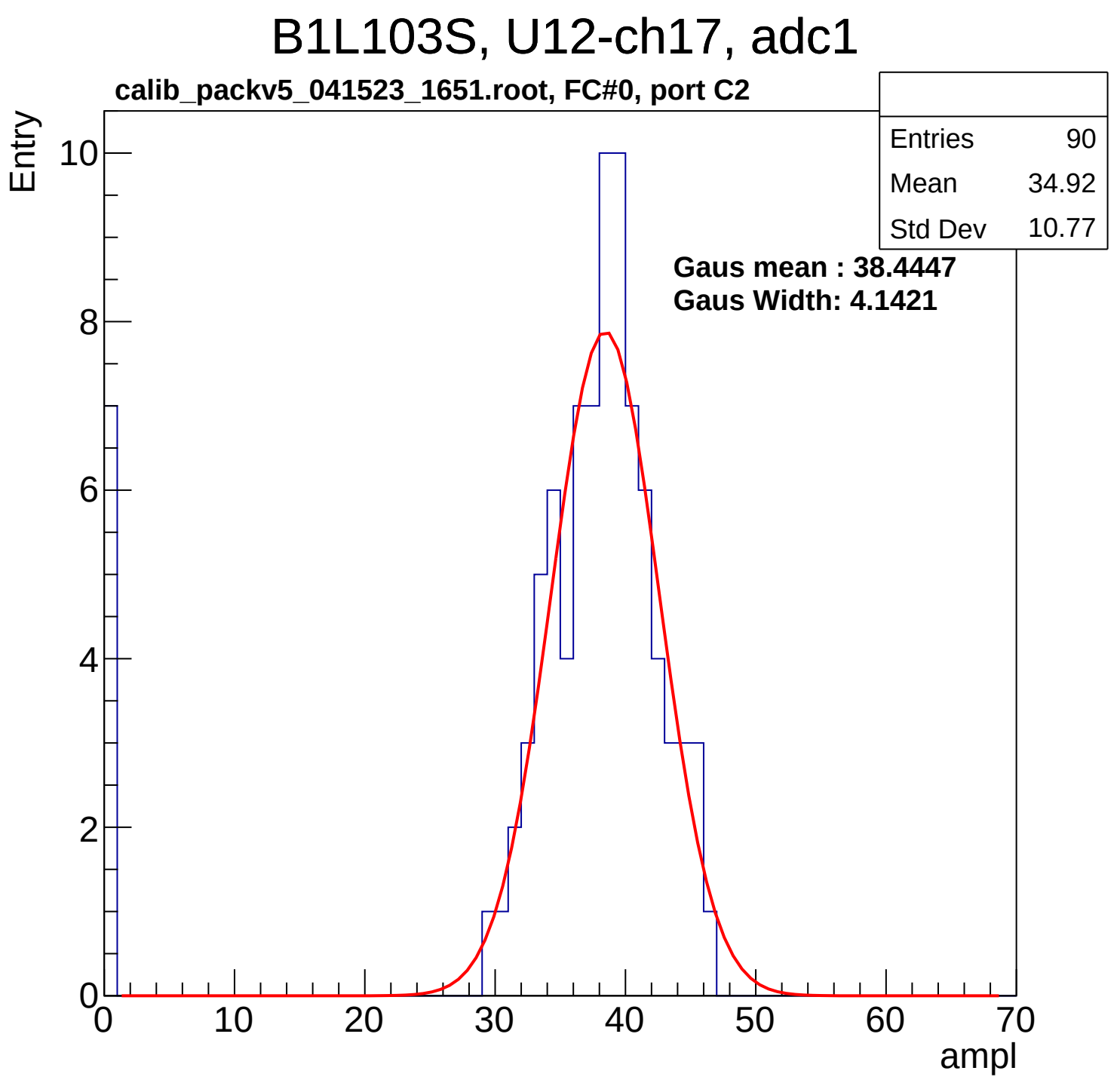
B1L103S, U12-ch17, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 34.92
Std Dev 10.77
Gaus mean : 38.4447
Gaus Width: 4.1421
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
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60
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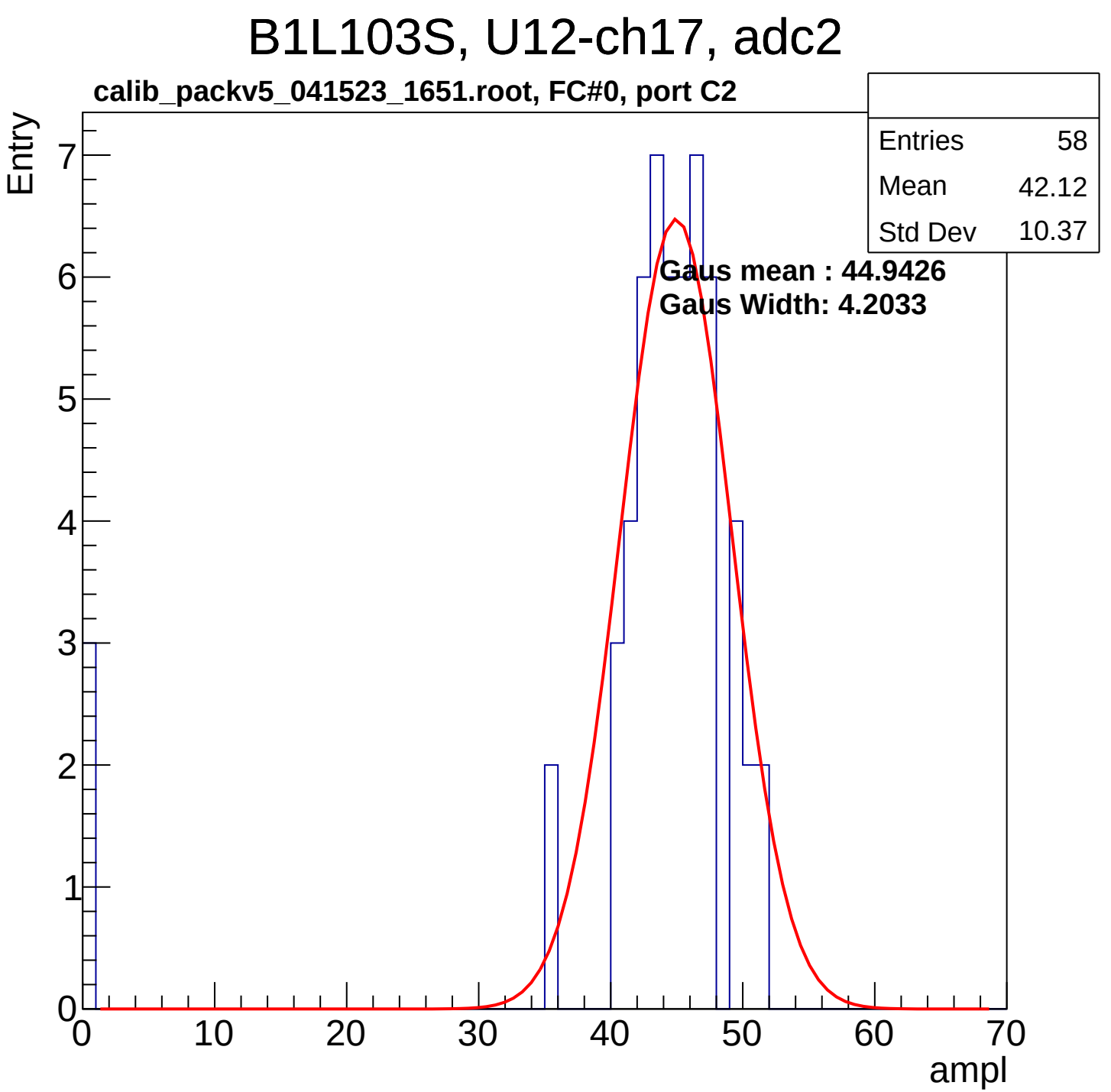
B1L103S, U12-ch17, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 42.12
Std Dev 10.37
Gaus mean : 44.9426
Gaus Width: 4.2033
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
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60
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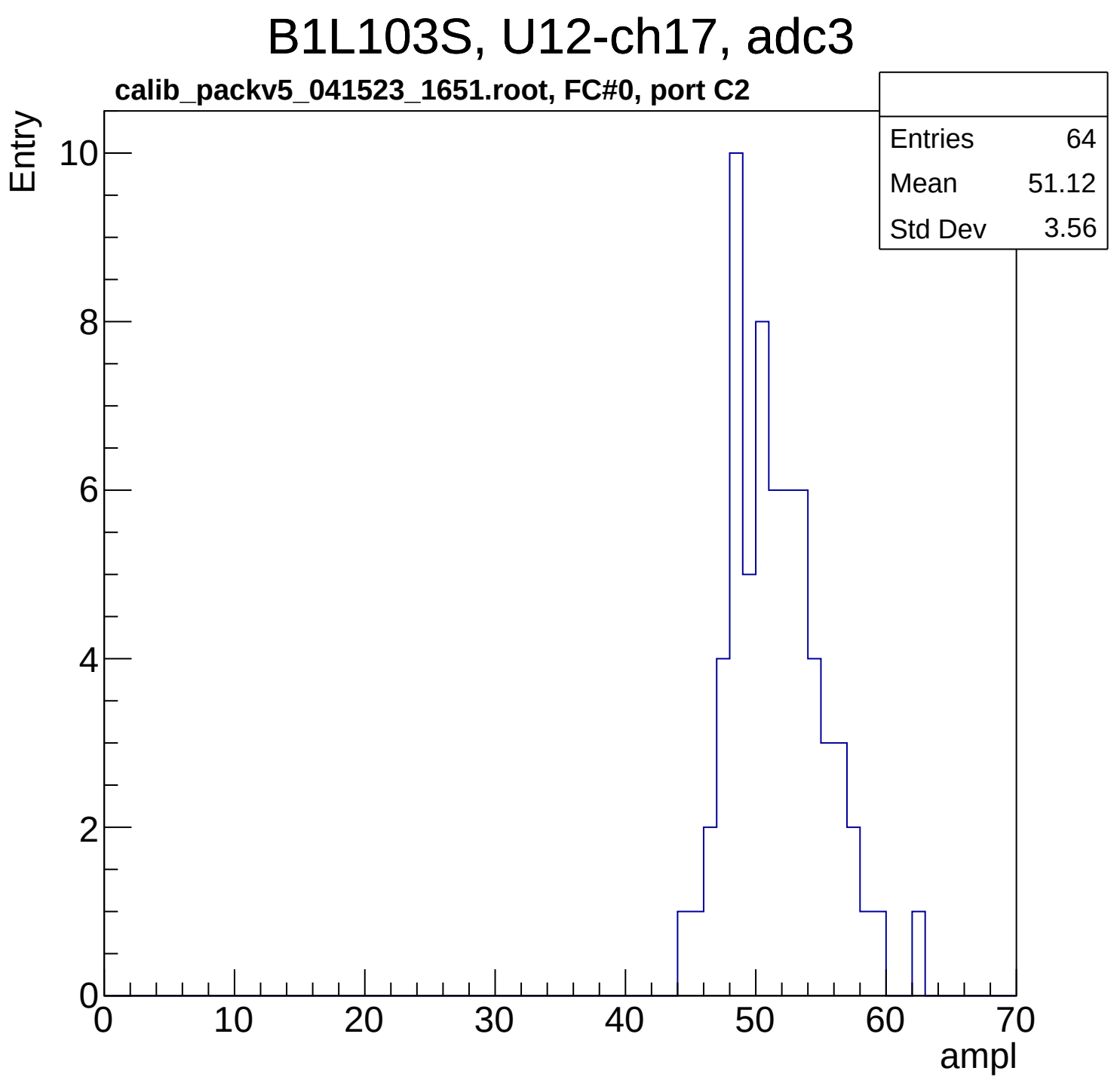
B1L103S, U12-ch17, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 51.12
Std Dev 3.56
Entry
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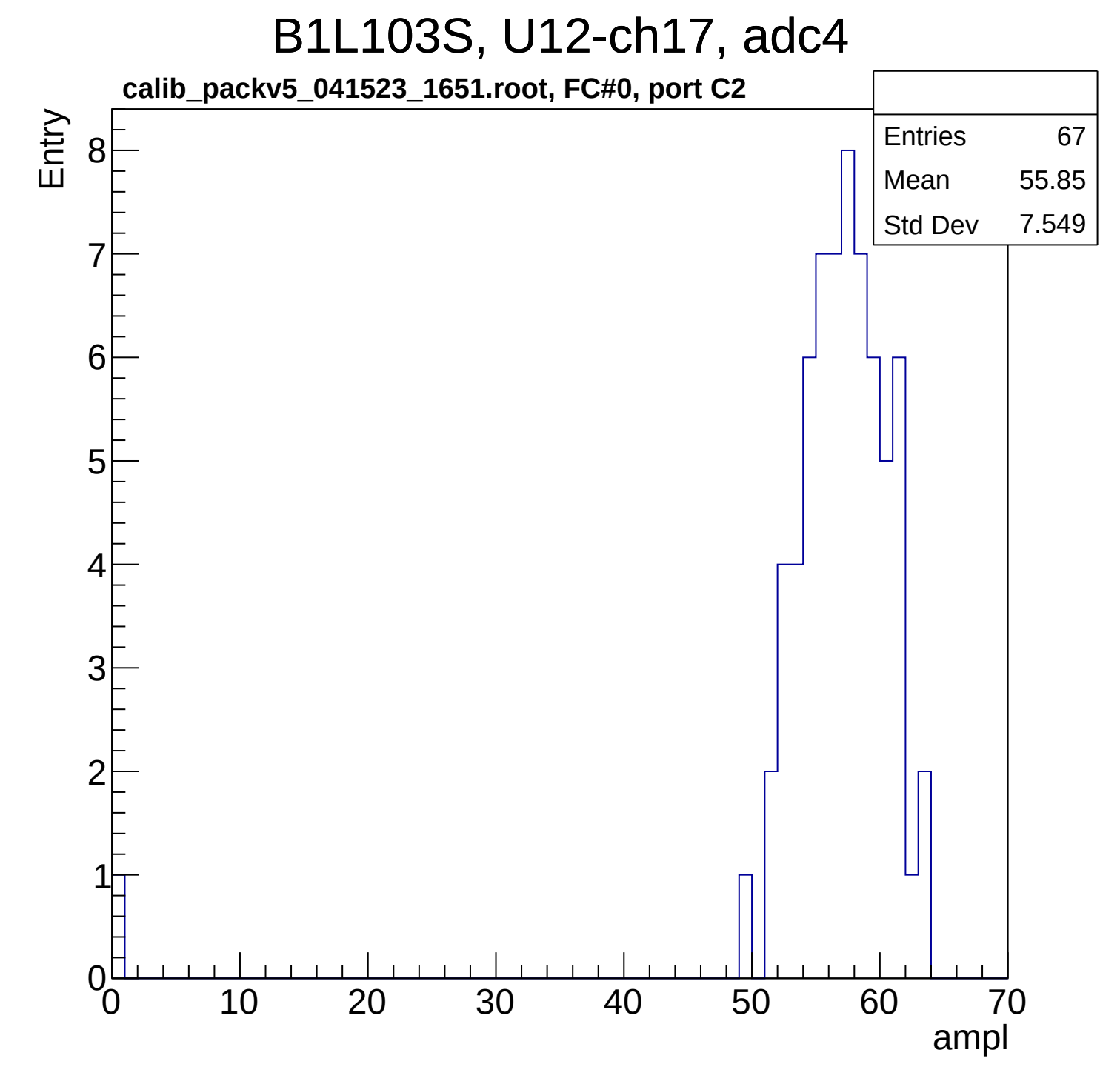
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch17, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 55.85
Std Dev 7.549
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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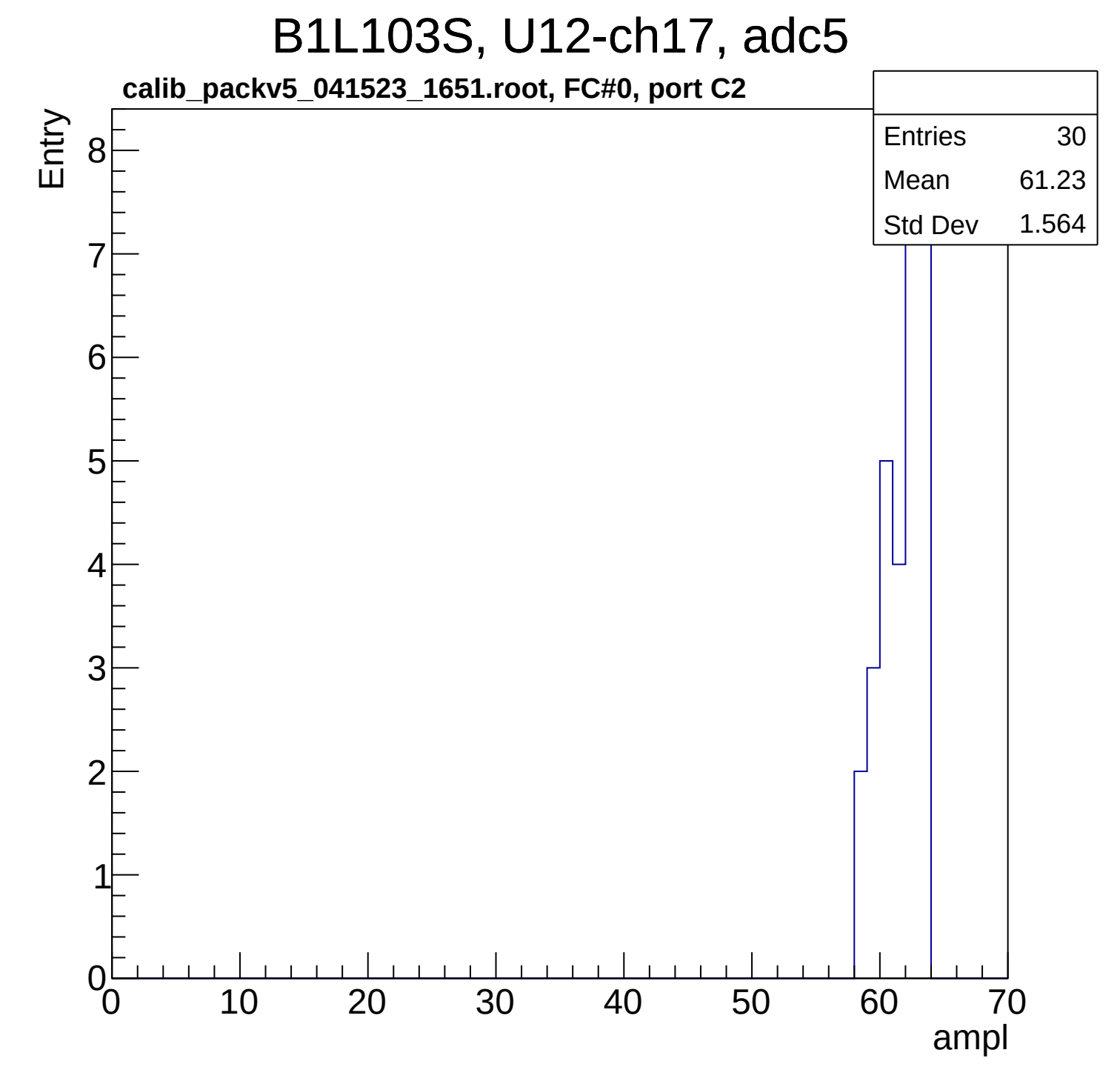
B1L103S, U12-ch17, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 61.23
Std Dev 1.564
Entry
ampl
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3
4
5
6
7
8
0
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20
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40
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60
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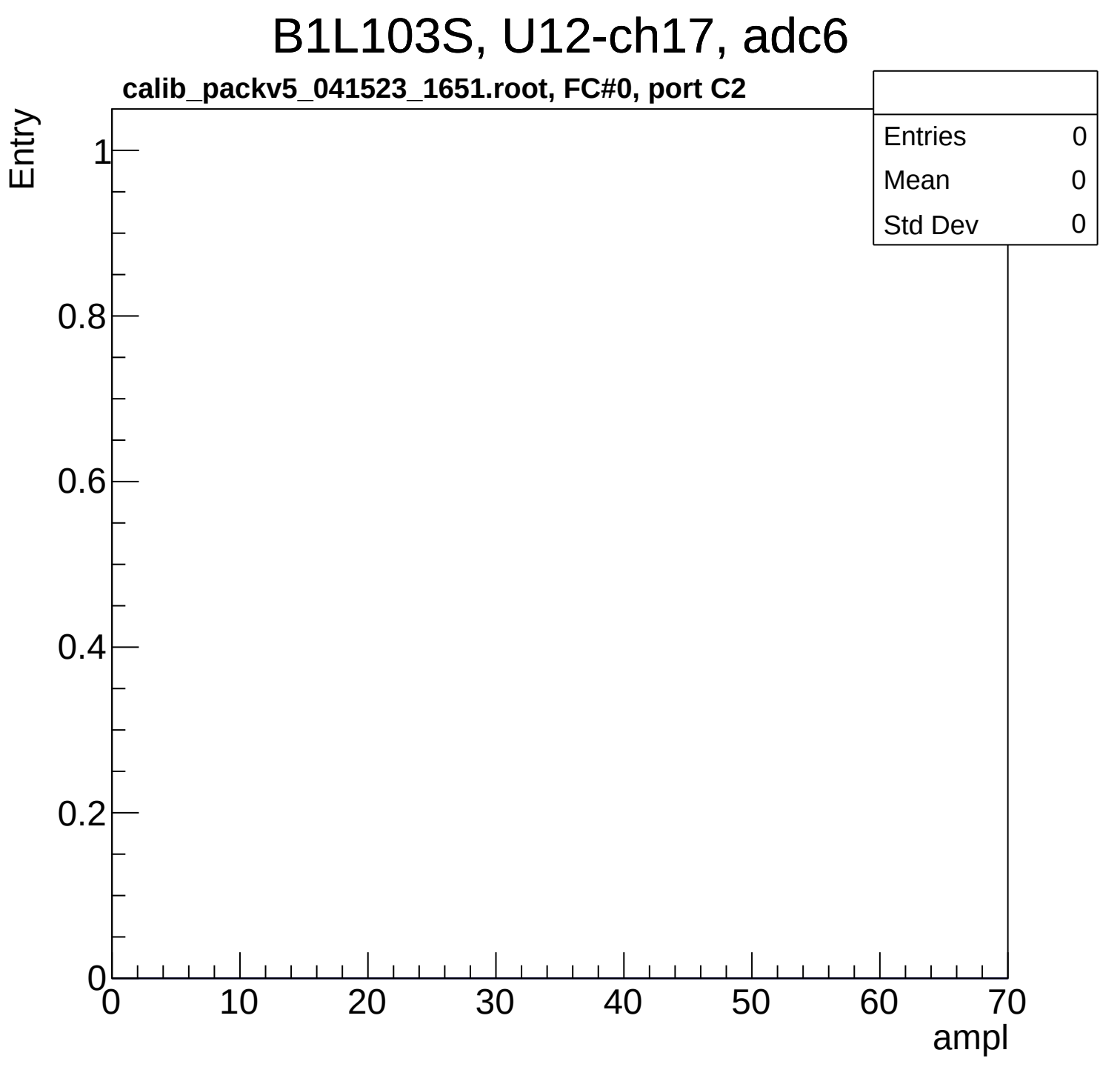
B1L103S, U12-ch17, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 0
Mean 0
Std Dev 0
Entry
1
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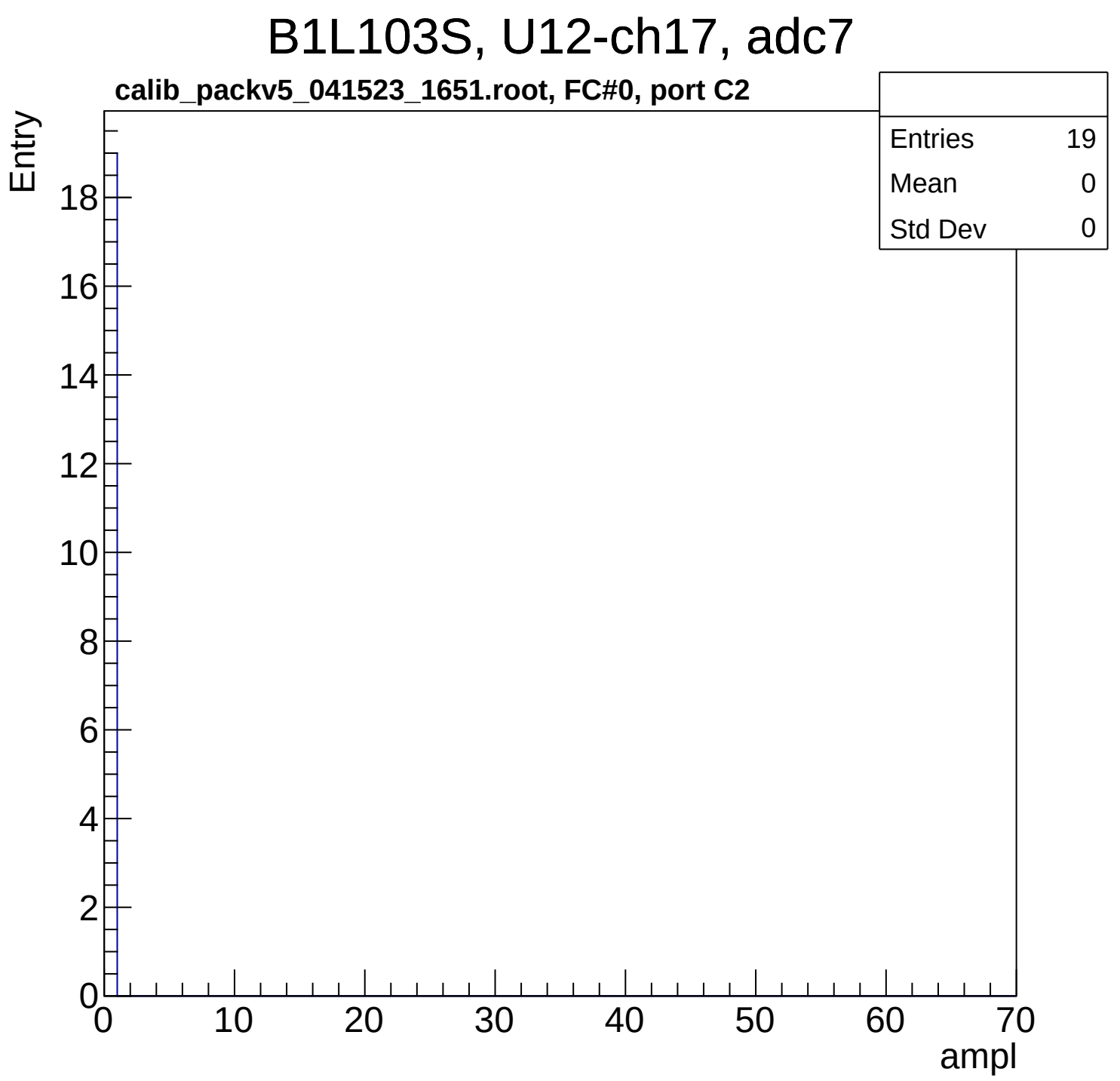
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch17, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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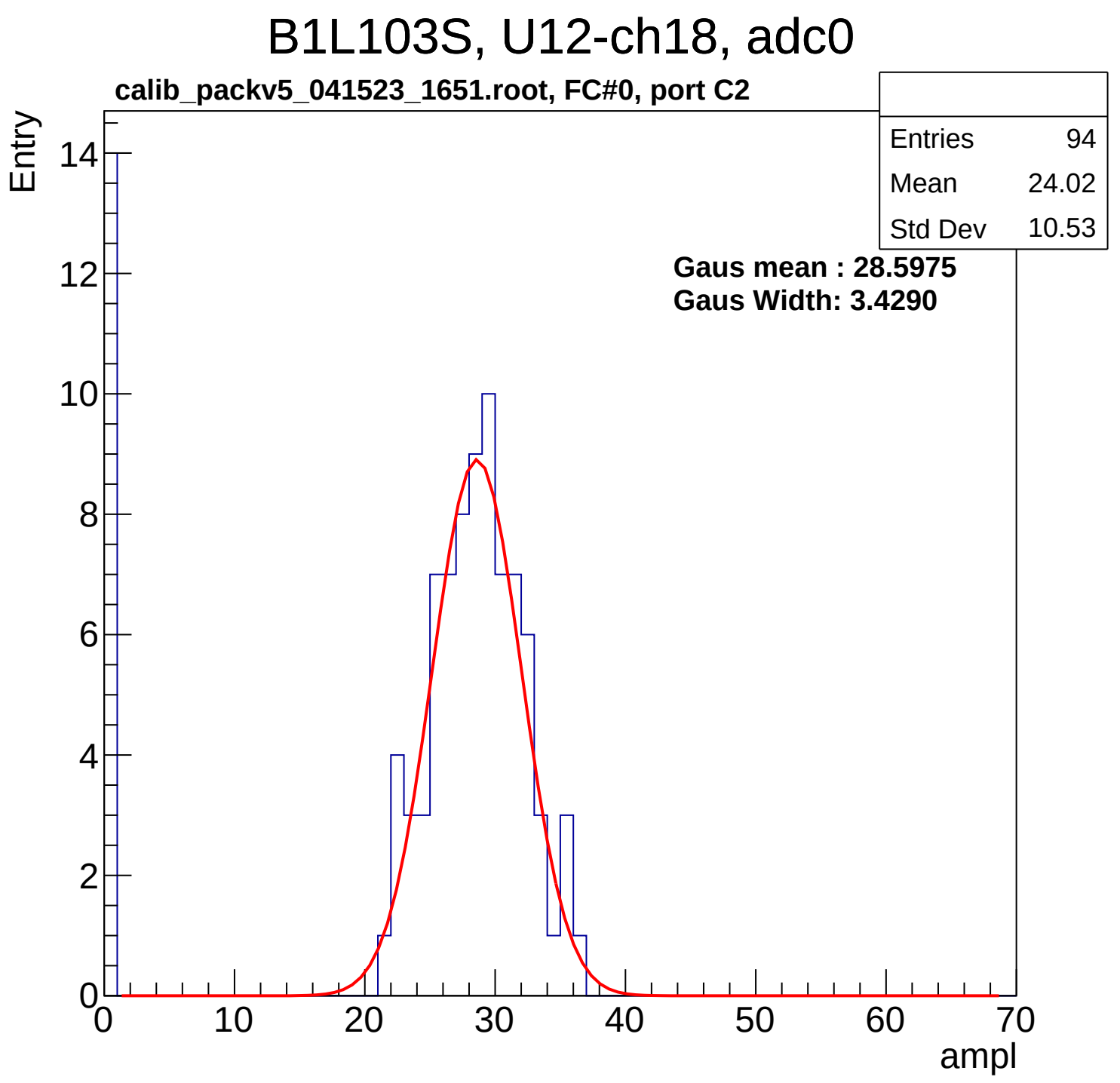
50
60
70
ampl


B1L103S, U12-ch18, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 24.02
Std Dev 10.53
Gaus mean : 28.5975
Gaus Width: 3.4290
Entry
ampl
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2
4
6
8
10
12
14
0
10
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30
40
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60
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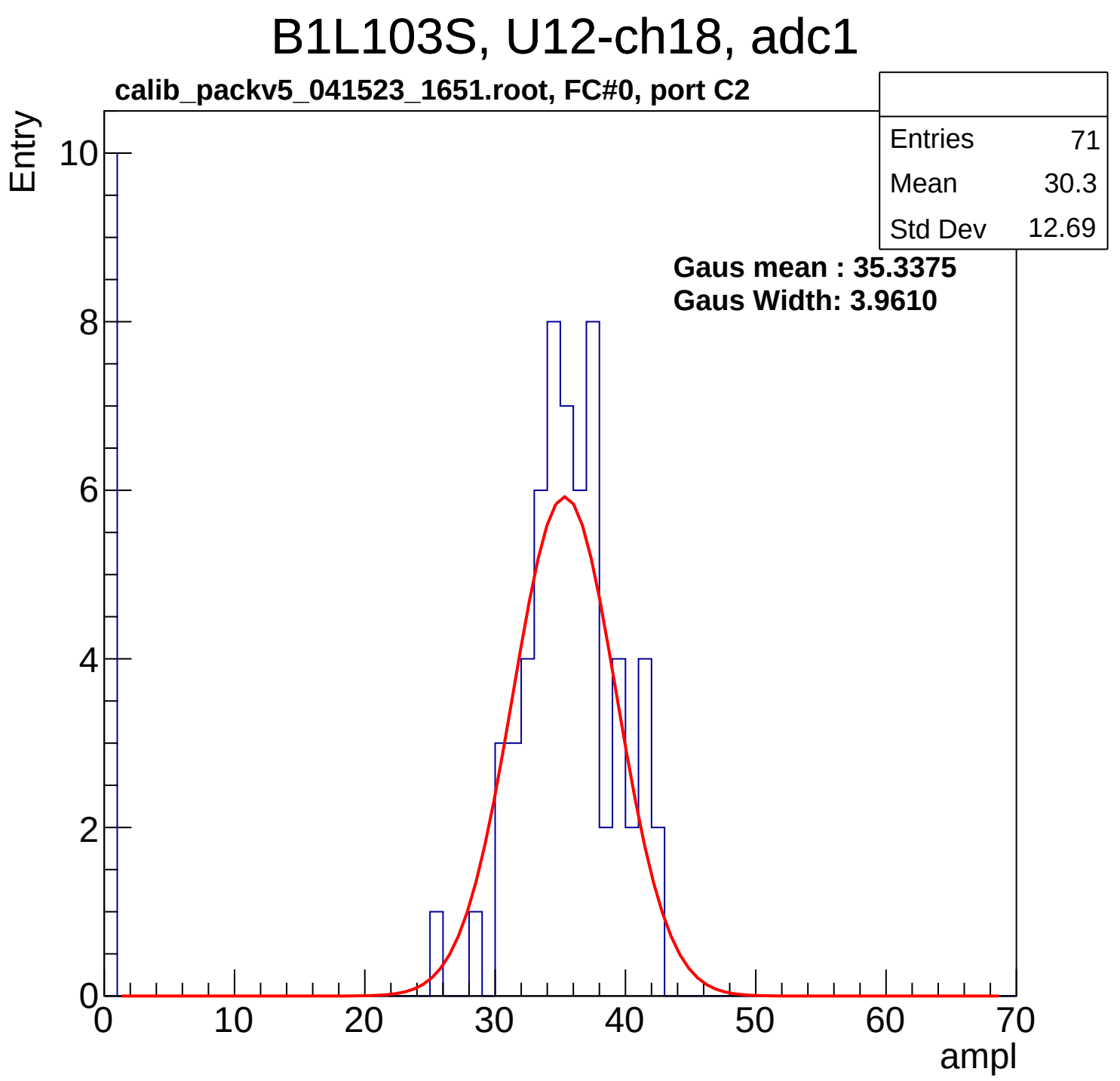
B1L103S, U12-ch18, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 30.3
Std Dev 12.69
Gaus mean : 35.3375
Gaus Width: 3.9610
Entry
ampl
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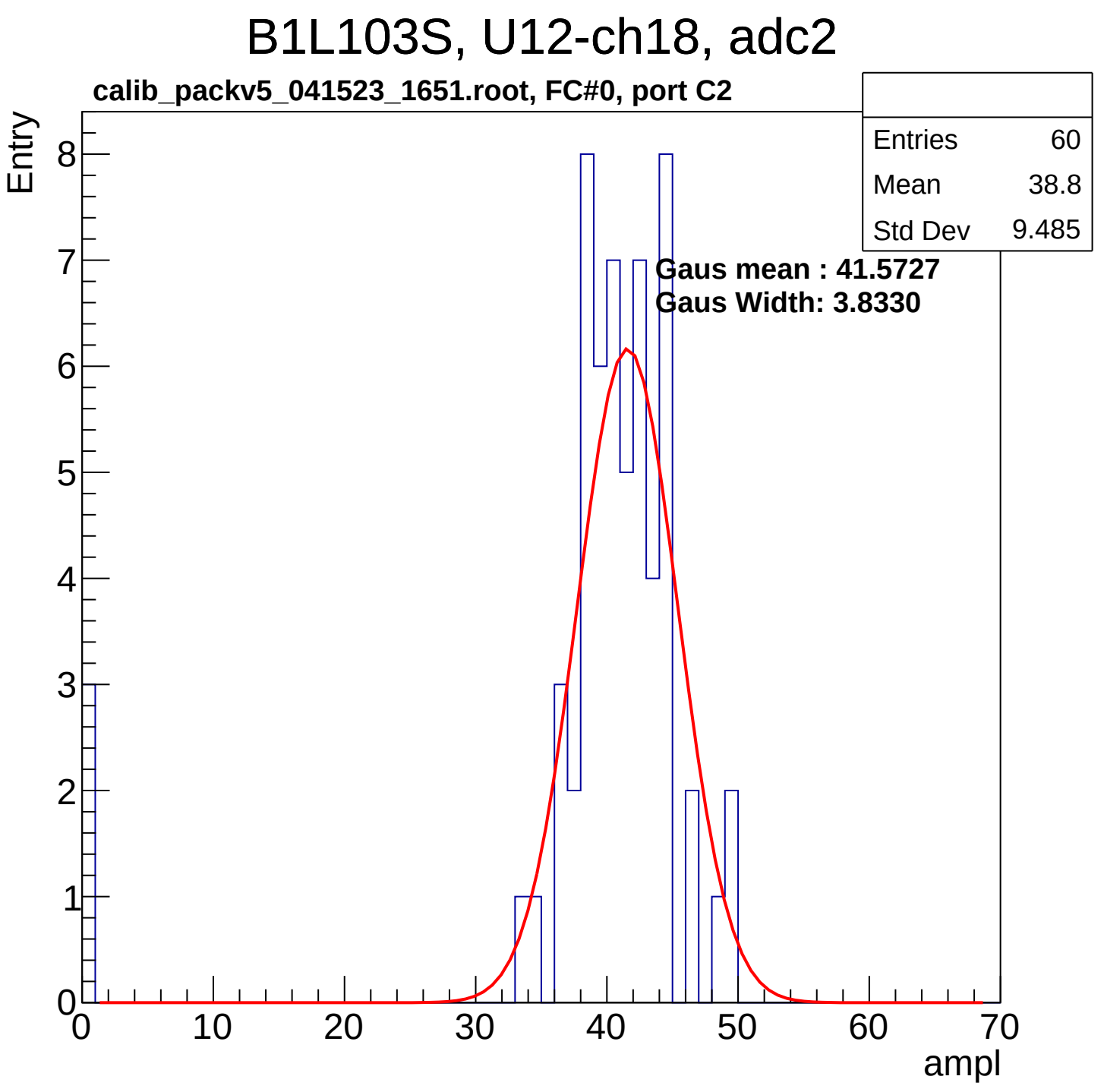
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch18, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 38.8
Std Dev 9.485
Gaus mean : 41.5727
Gaus Width: 3.8330
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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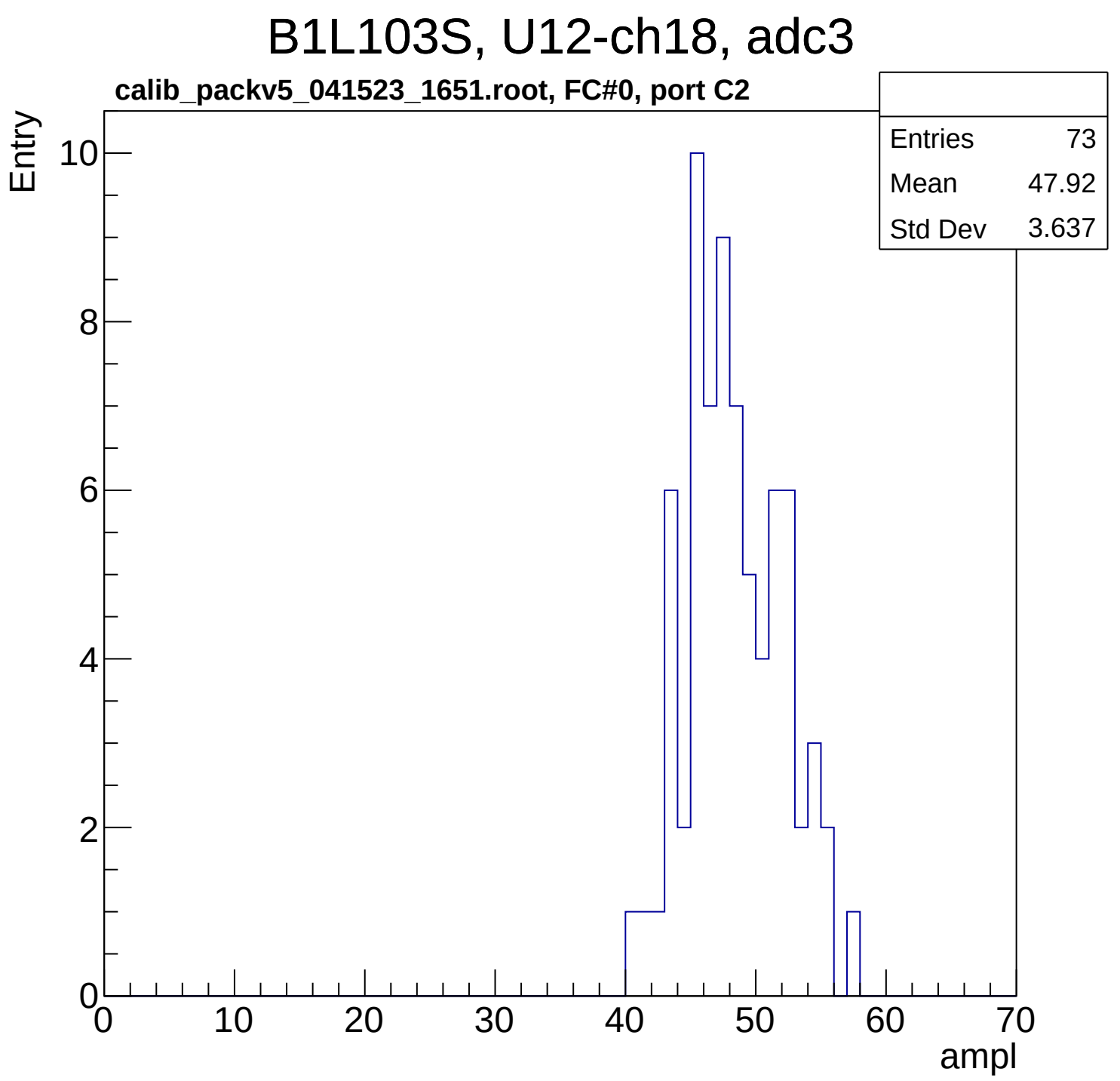
B1L103S, U12-ch18, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 47.92
Std Dev 3.637
Entry
ampl
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0
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20
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60
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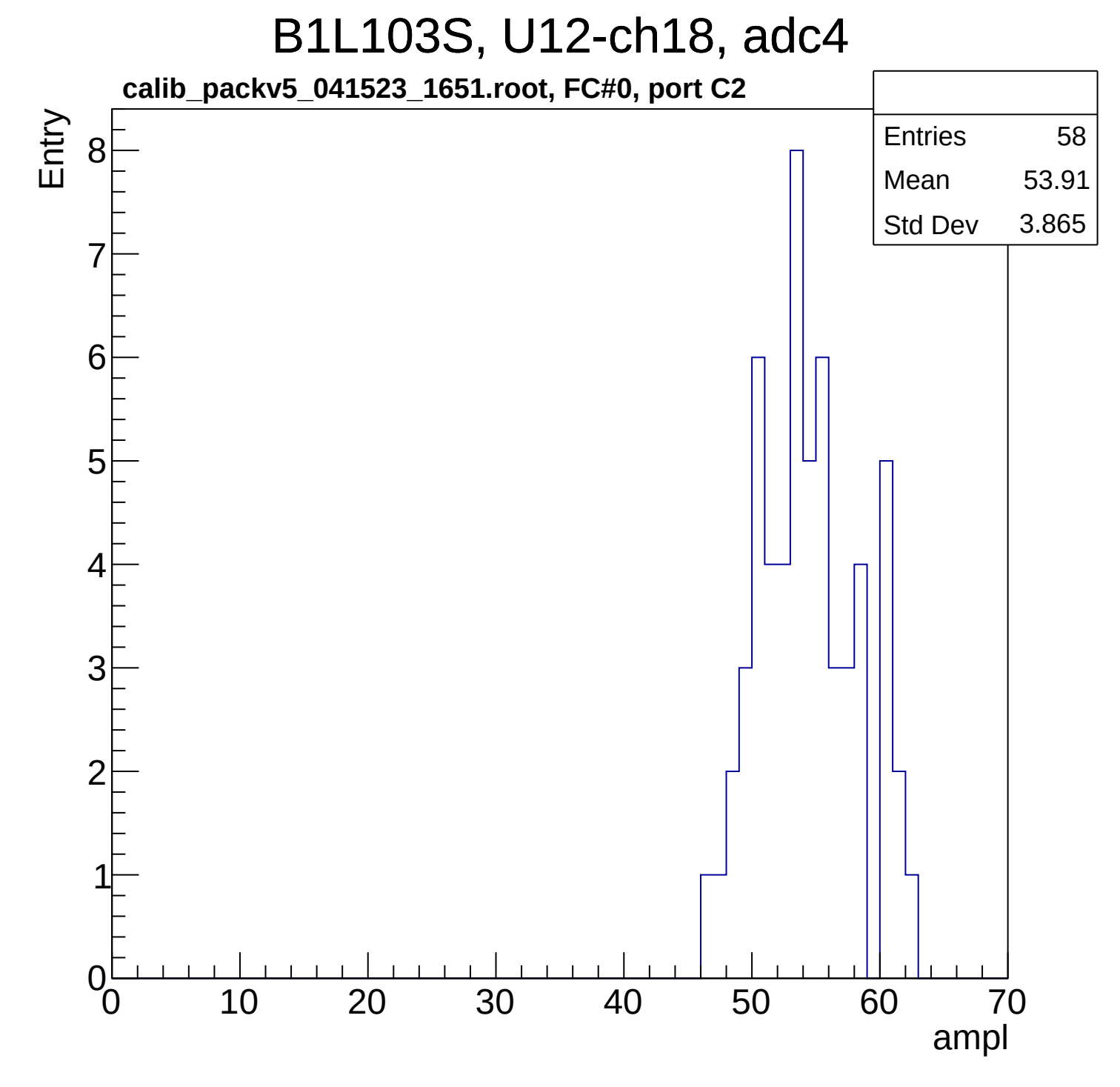
B1L103S, U12-ch18, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 53.91
Std Dev 3.865
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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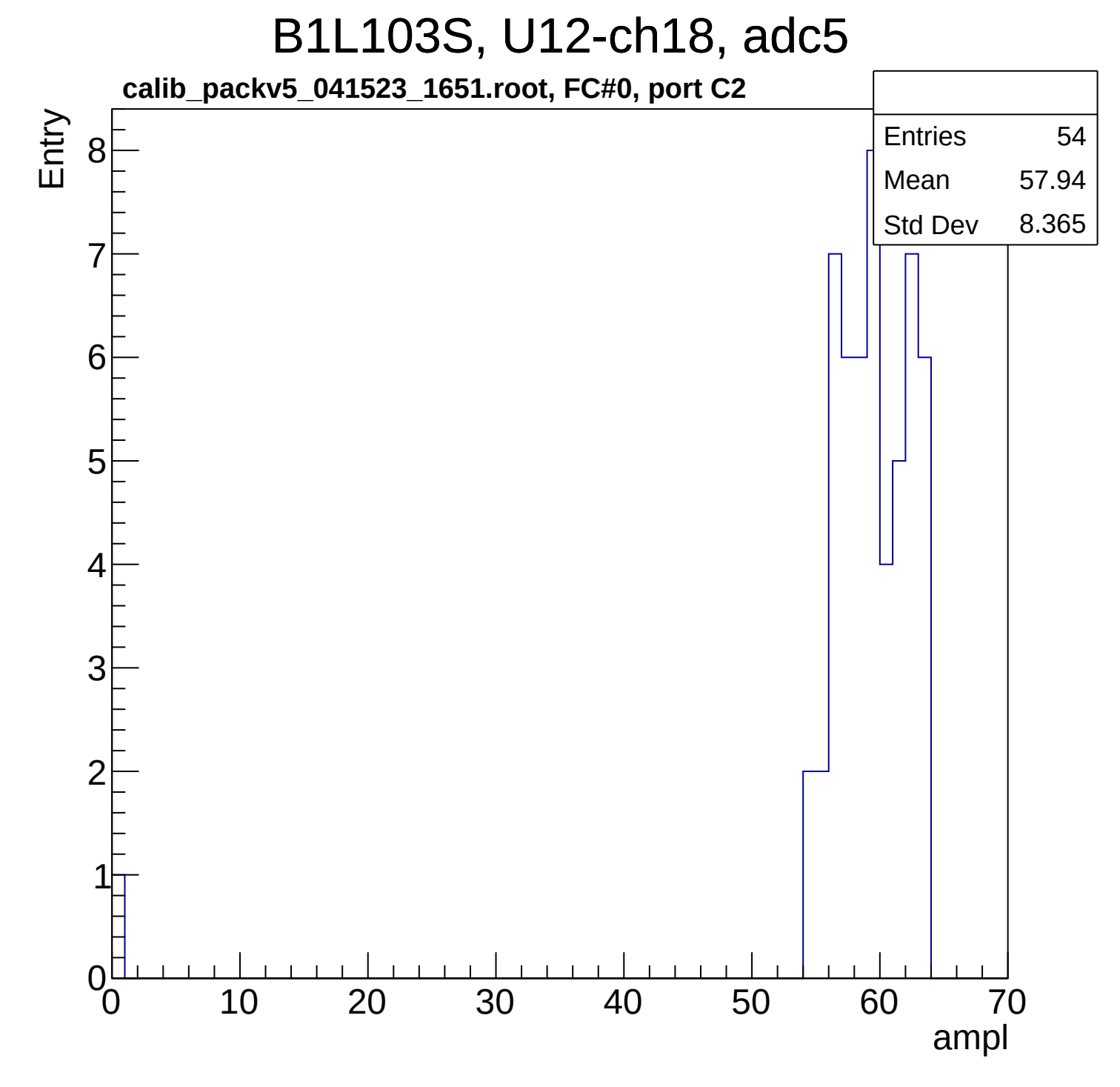
B1L103S, U12-ch18, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.94
Std Dev 8.365
Entry
ampl
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3
4
5
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7
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0
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40
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60
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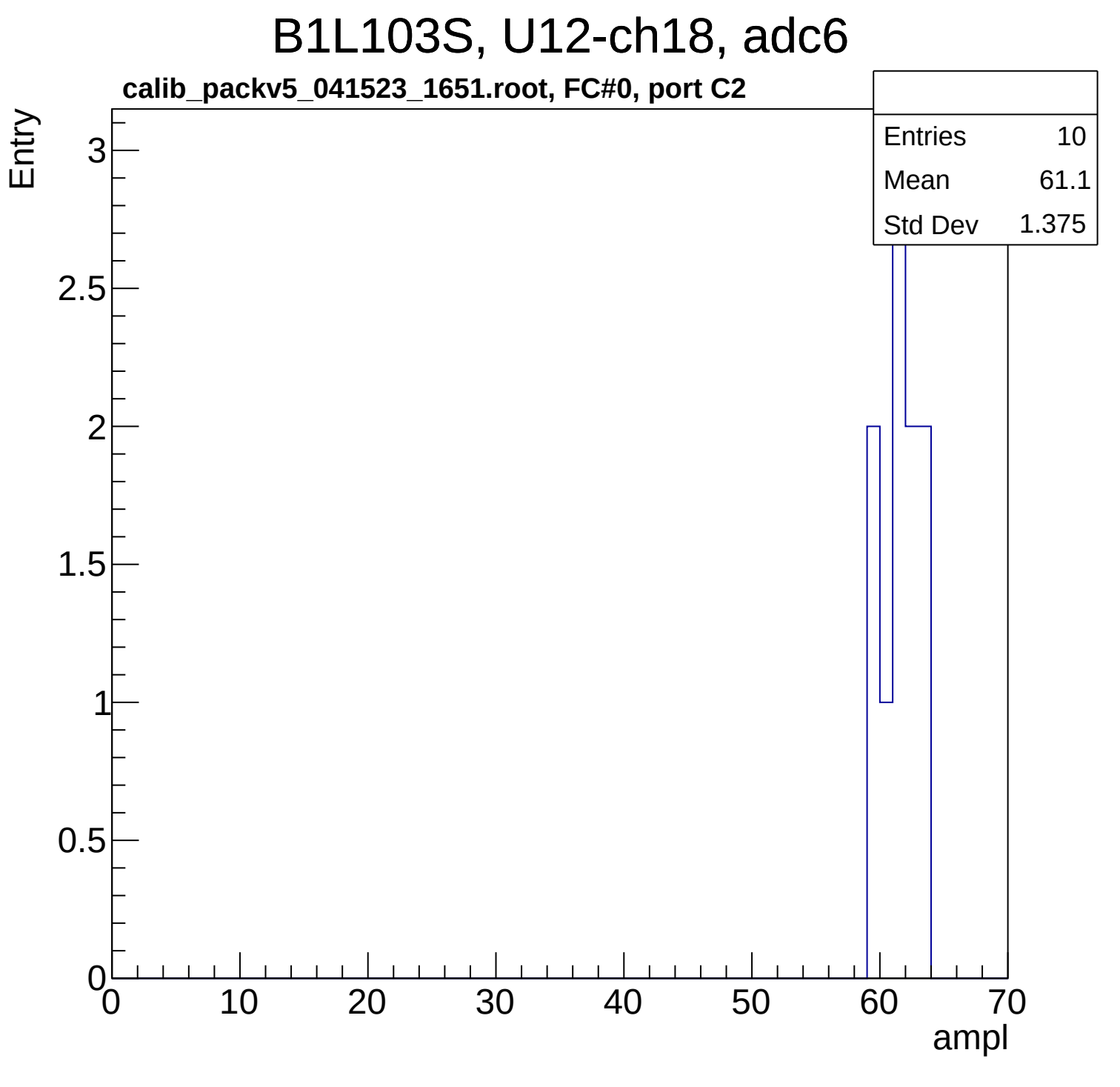
B1L103S, U12-ch18, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 61.1
Std Dev 1.375
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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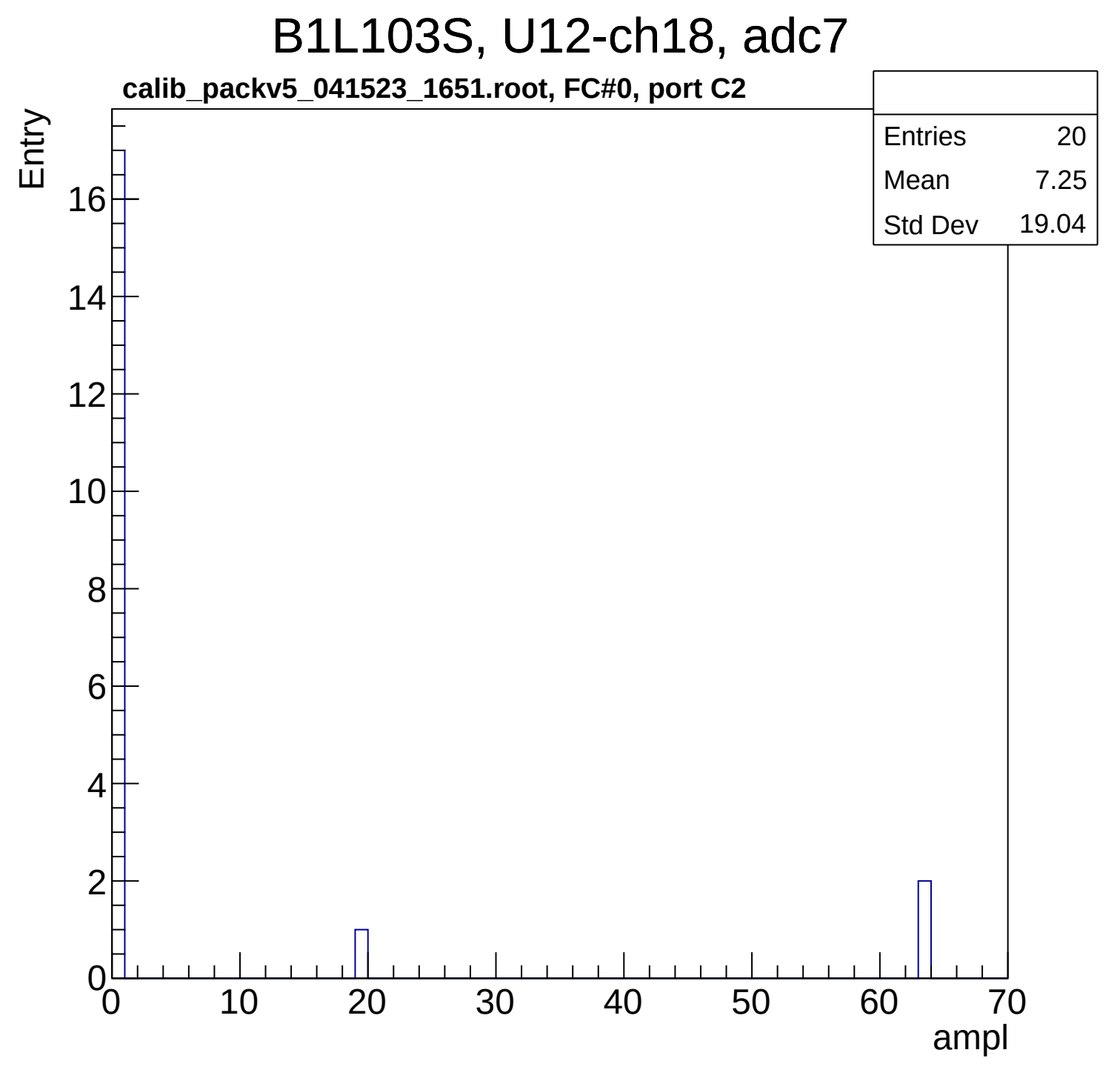
B1L103S, U12-ch18, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 7.25
Std Dev 19.04
Entry
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6
8
10
12
14
16
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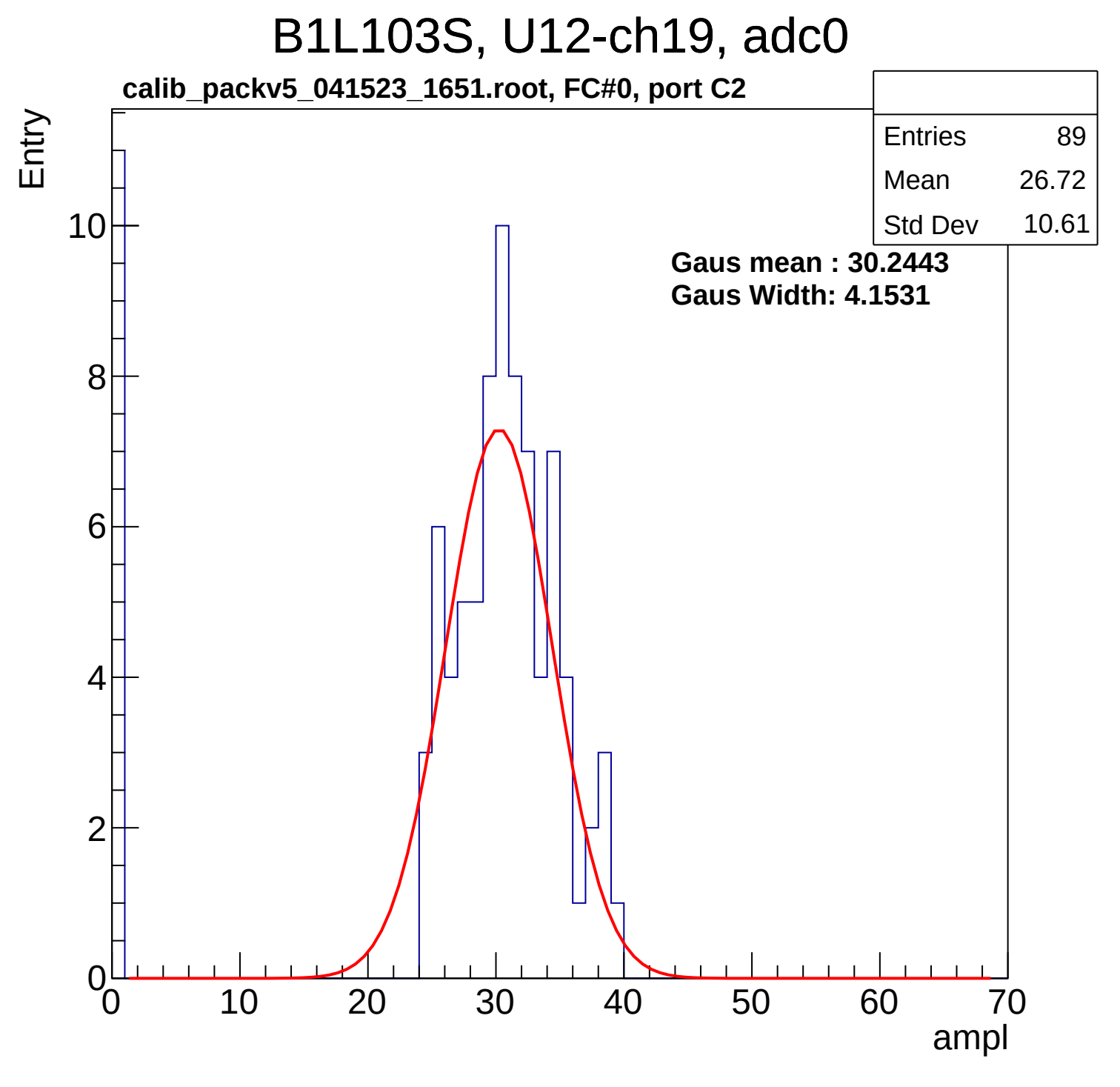
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch19, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 26.72
Std Dev 10.61
Gaus mean : 30.2443
Gaus Width: 4.1531
Entry
ampl
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6
8
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0
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20
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40
50
60
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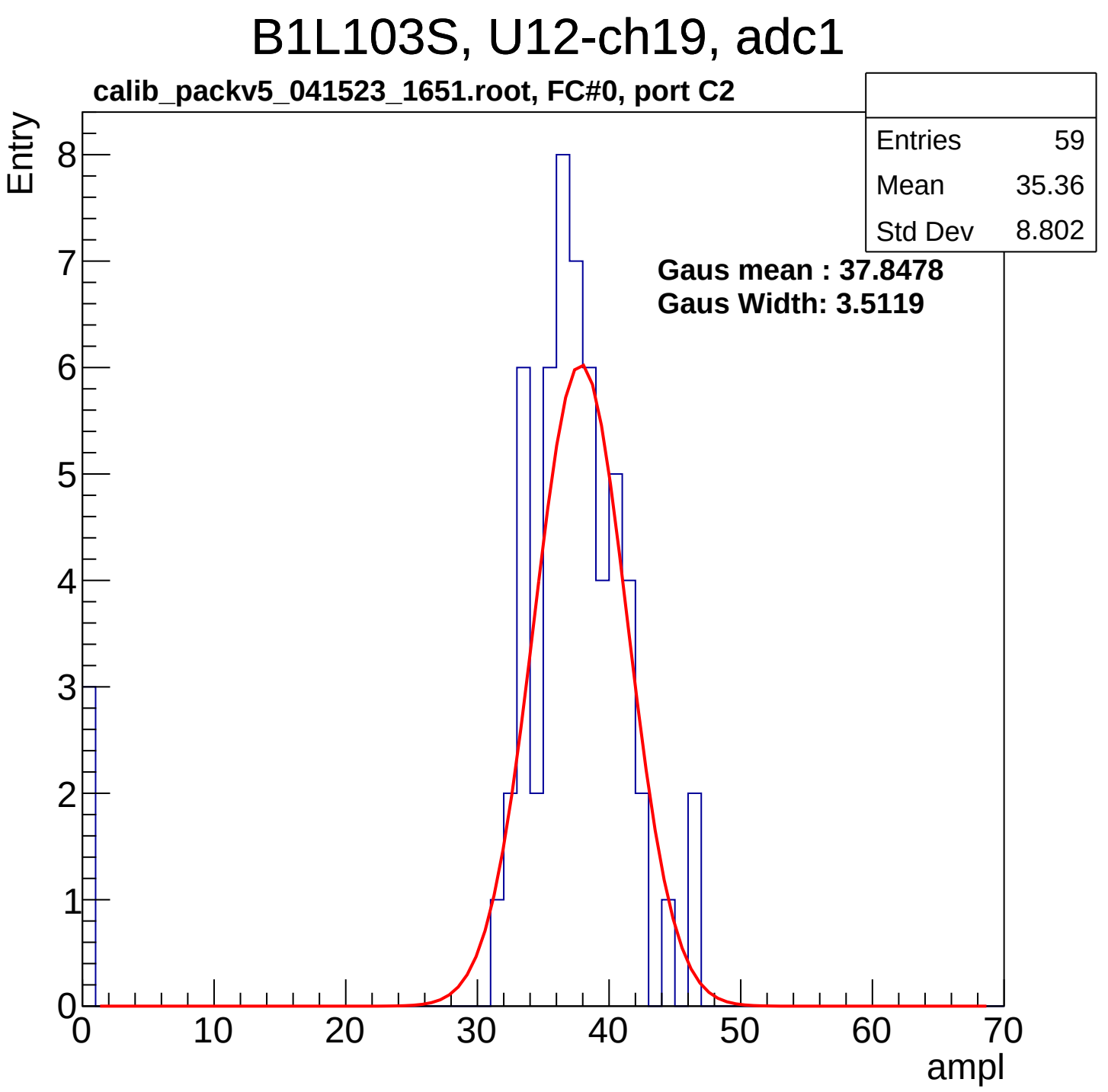
B1L103S, U12-ch19, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 35.36
Std Dev 8.802
Gaus mean : 37.8478
Gaus Width: 3.5119
Entry
ampl
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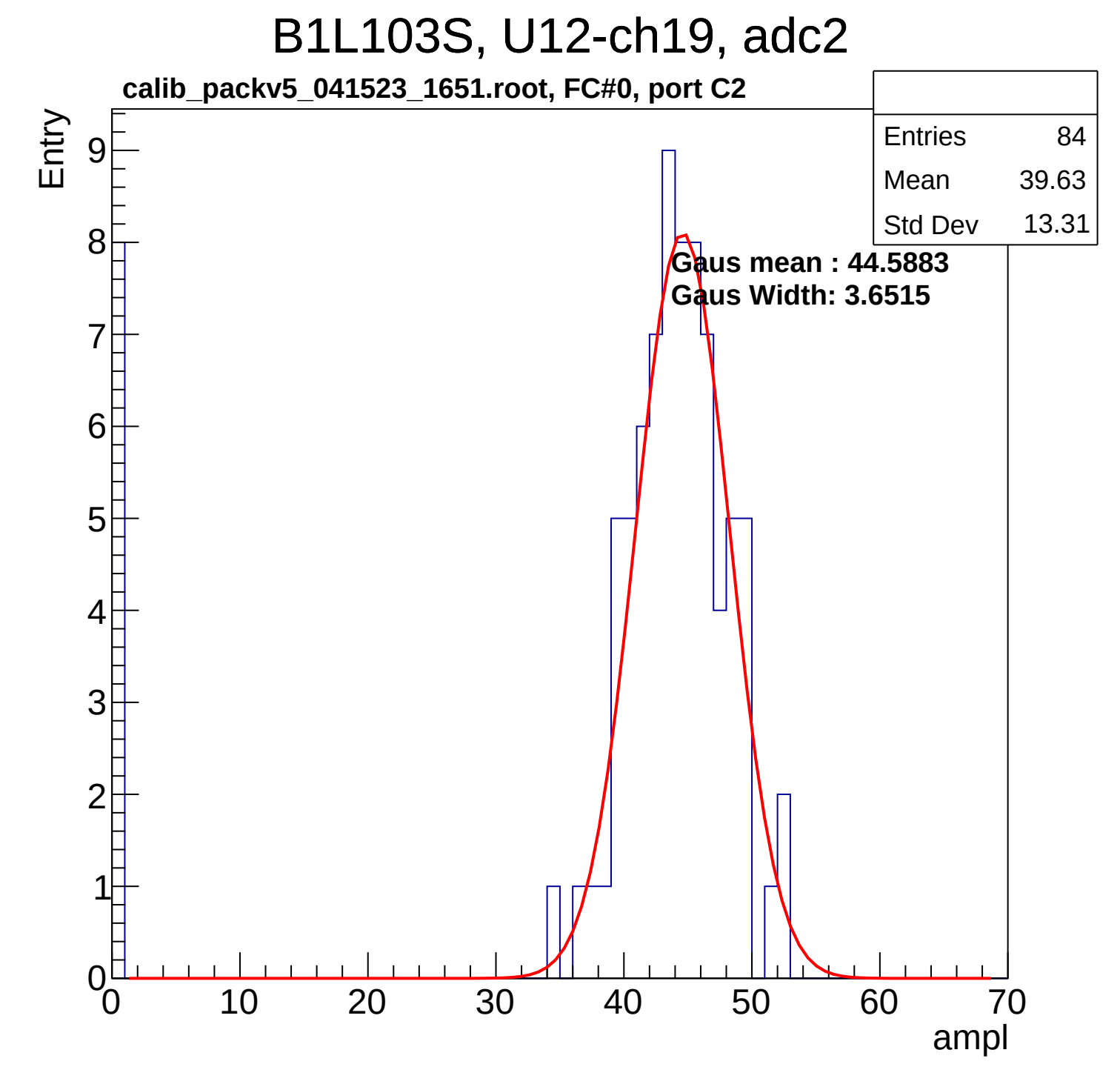
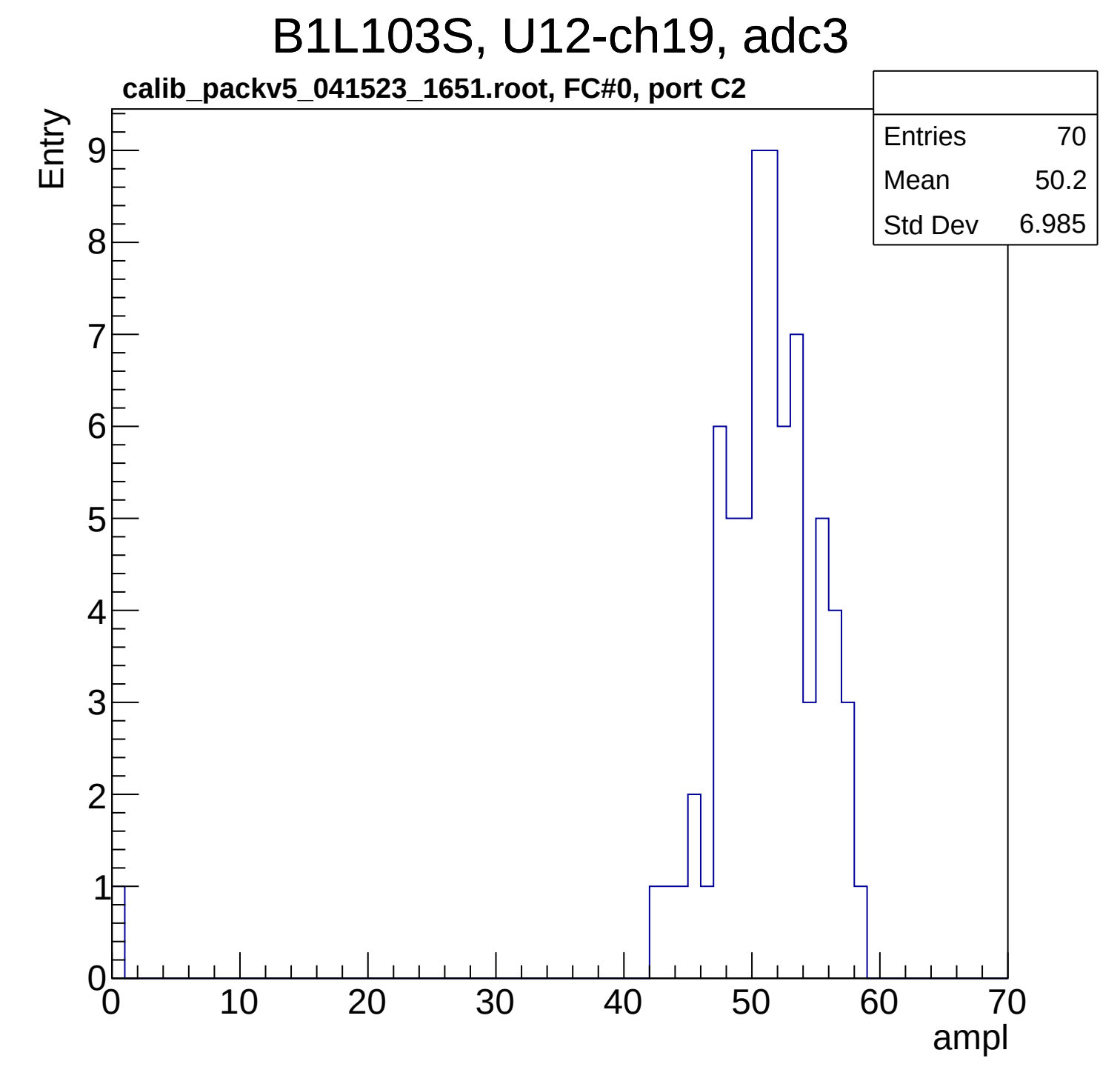
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U12-ch19, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 39.63
Std Dev 13.31
Gaus mean : 44.5883
Gaus Width: 3.6515
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch19, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 50.2
Std Dev 6.985
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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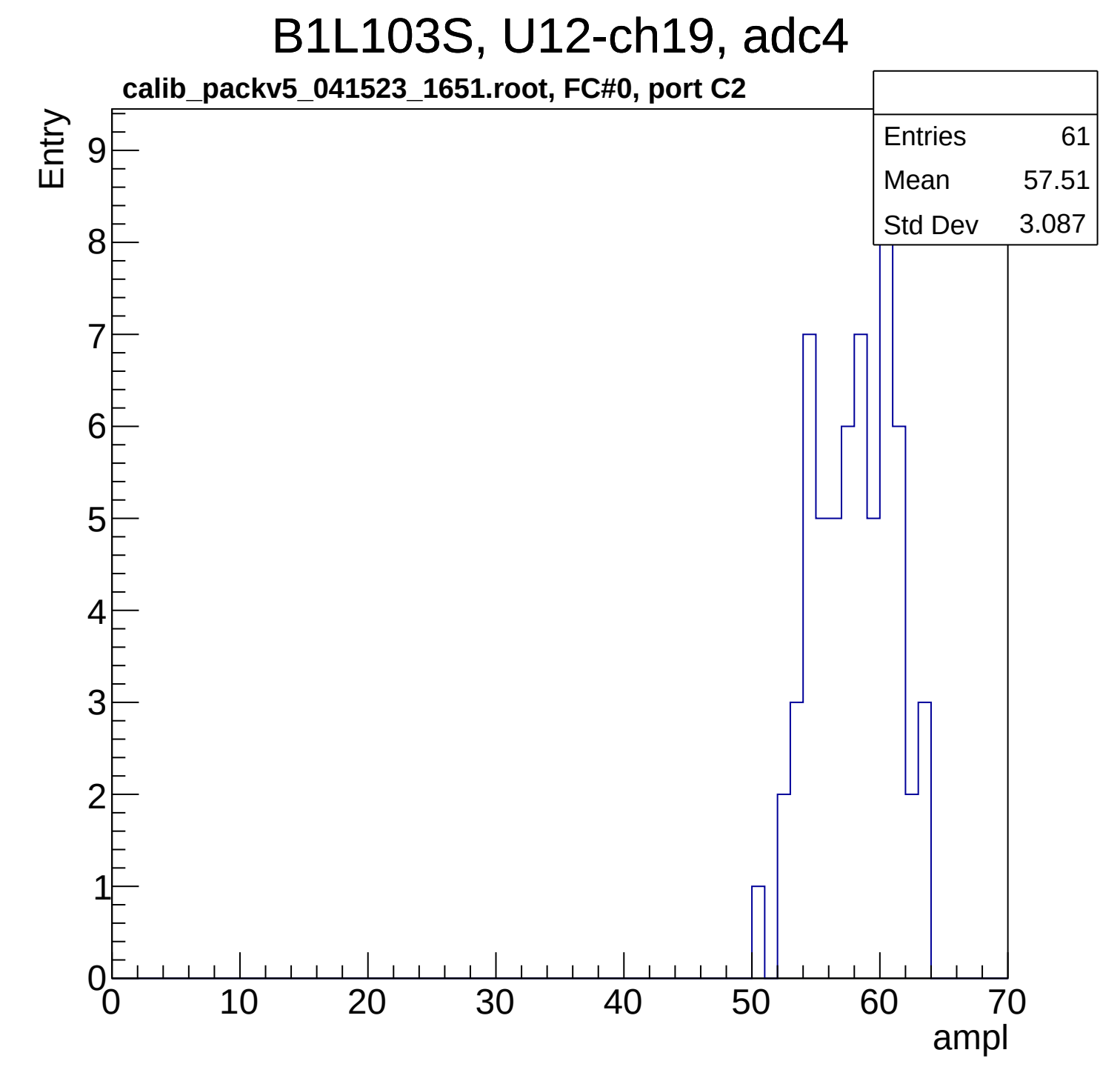
B1L103S, U12-ch19, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 57.51
Std Dev 3.087
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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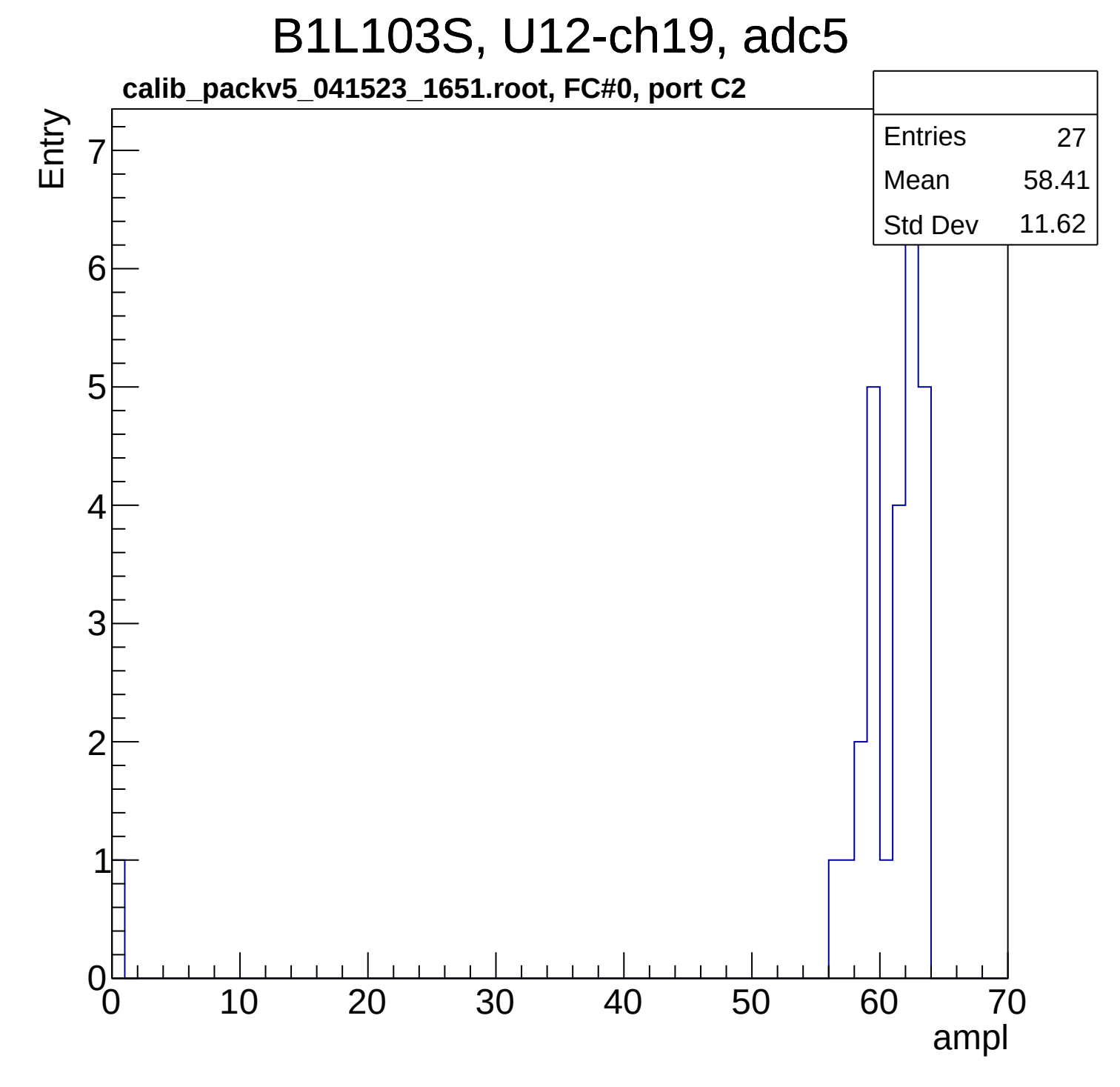
B1L103S, U12-ch19, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 27
Mean 58.41
Std Dev 11.62
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
30
40
50
60
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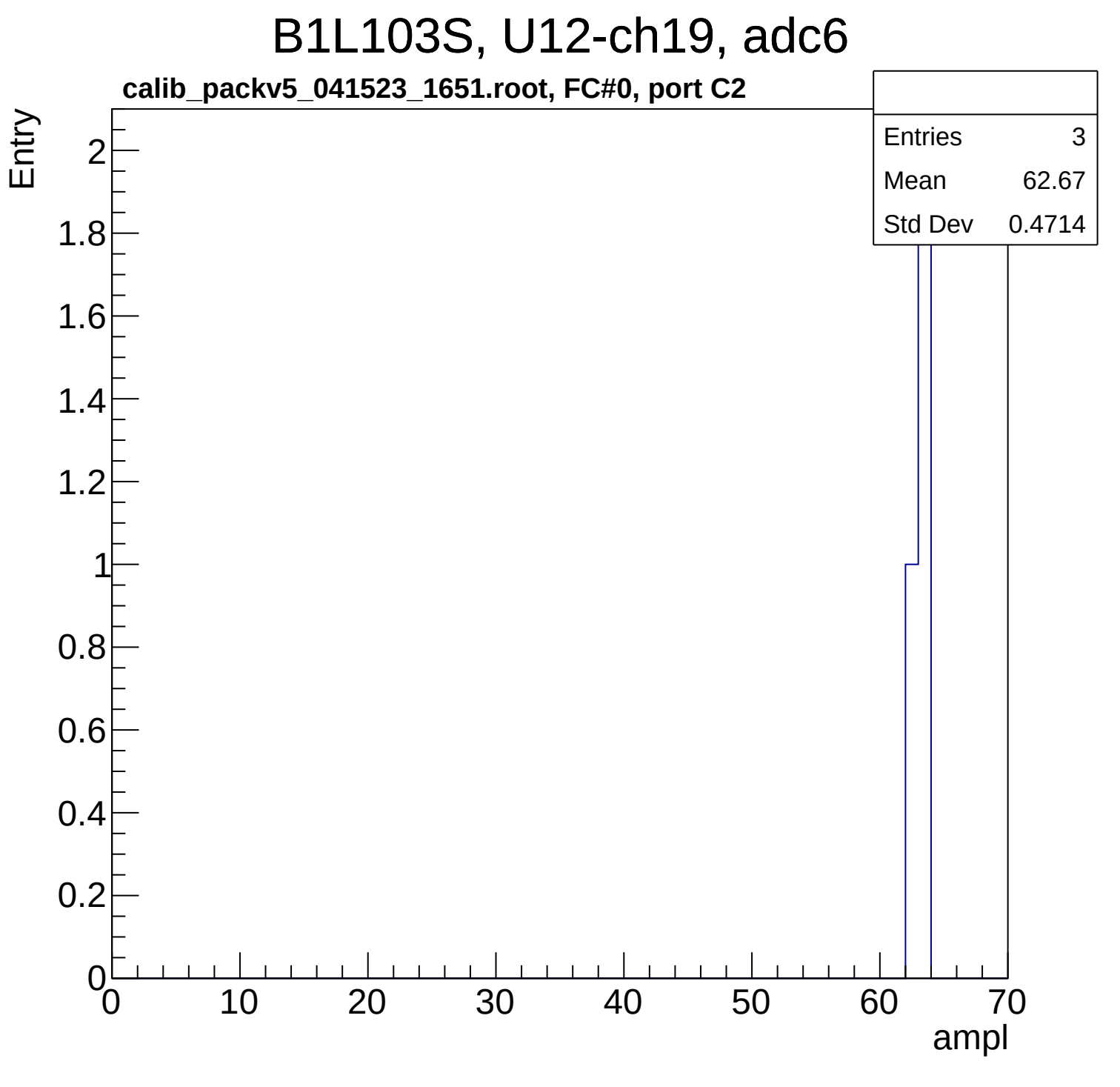
B1L103S, U12-ch19, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
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60
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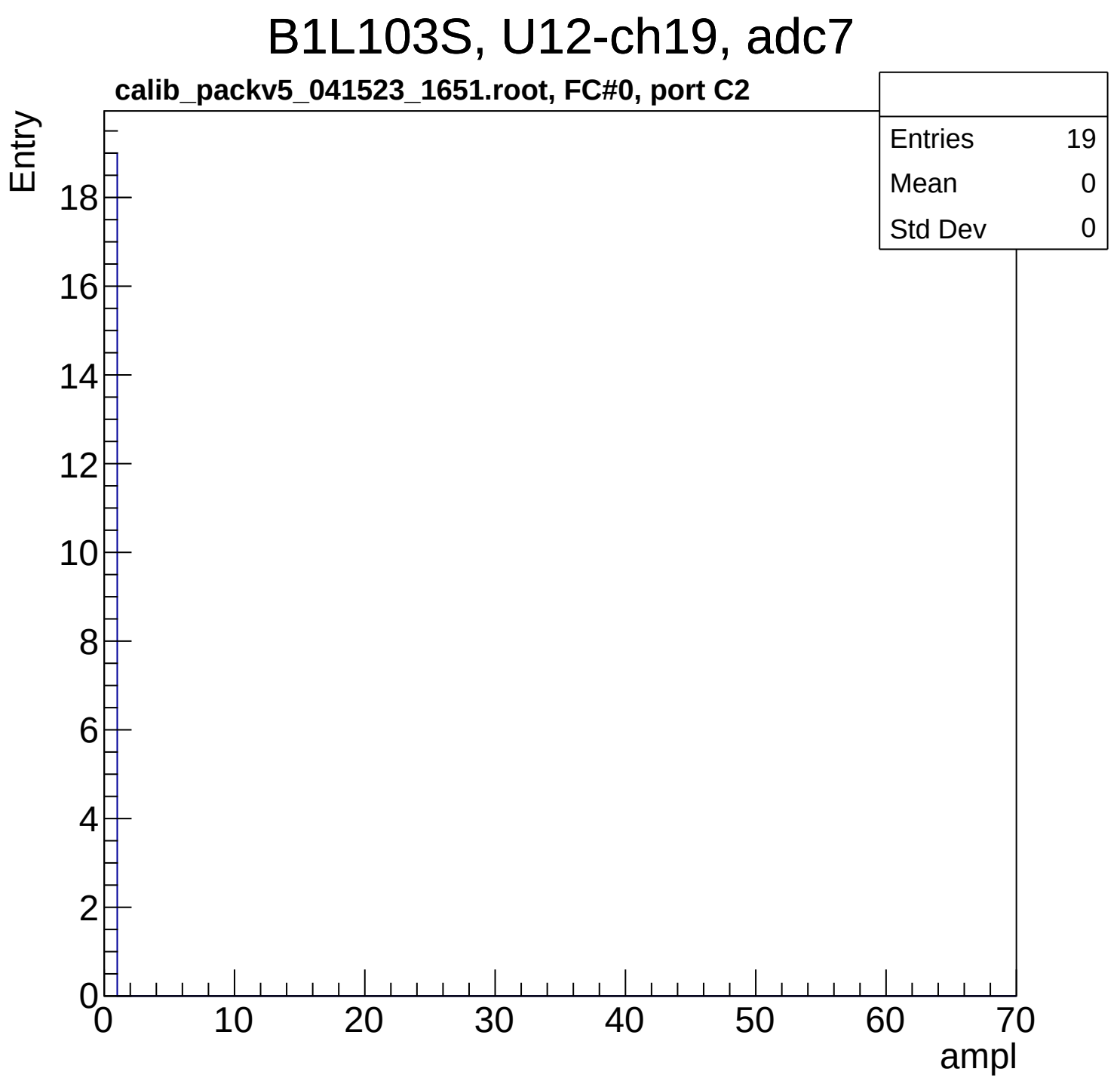
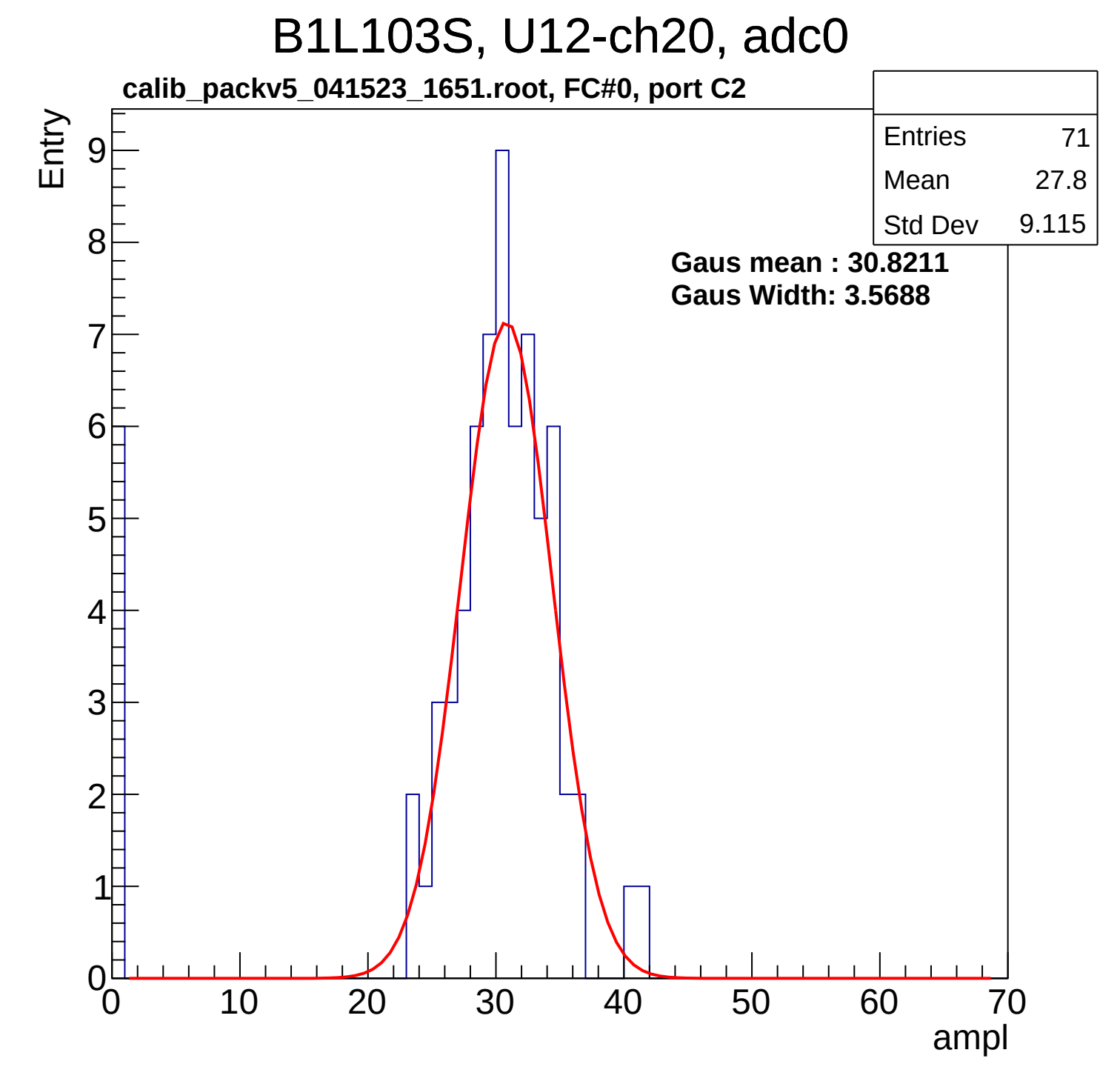
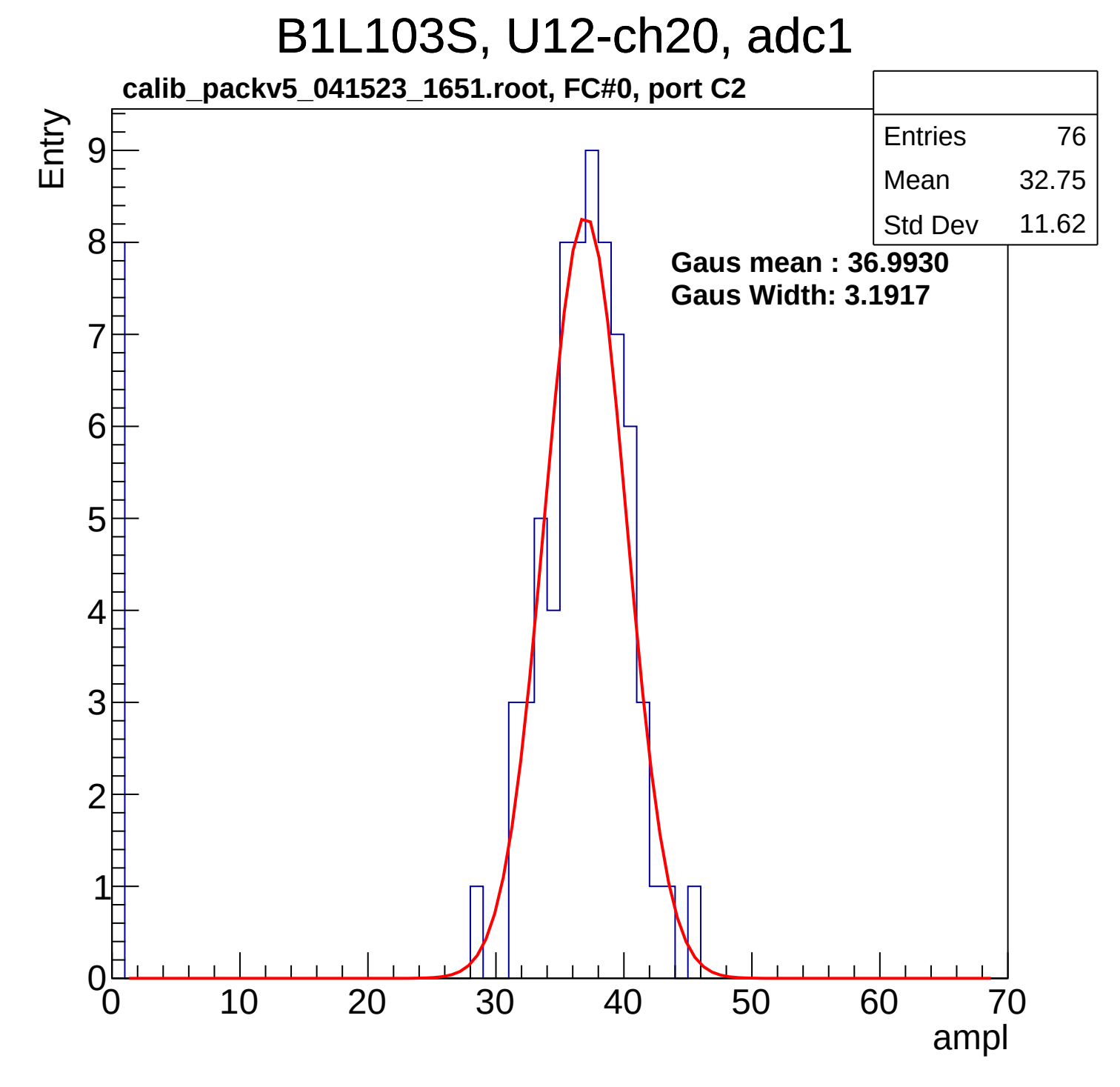

B1L103S, U12-ch19, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch20, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 27.8
Std Dev 9.115
Gaus mean : 30.8211
Gaus Width: 3.5688
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch20, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 32.75
Std Dev 11.62
Gaus mean : 36.9930
Gaus Width: 3.1917
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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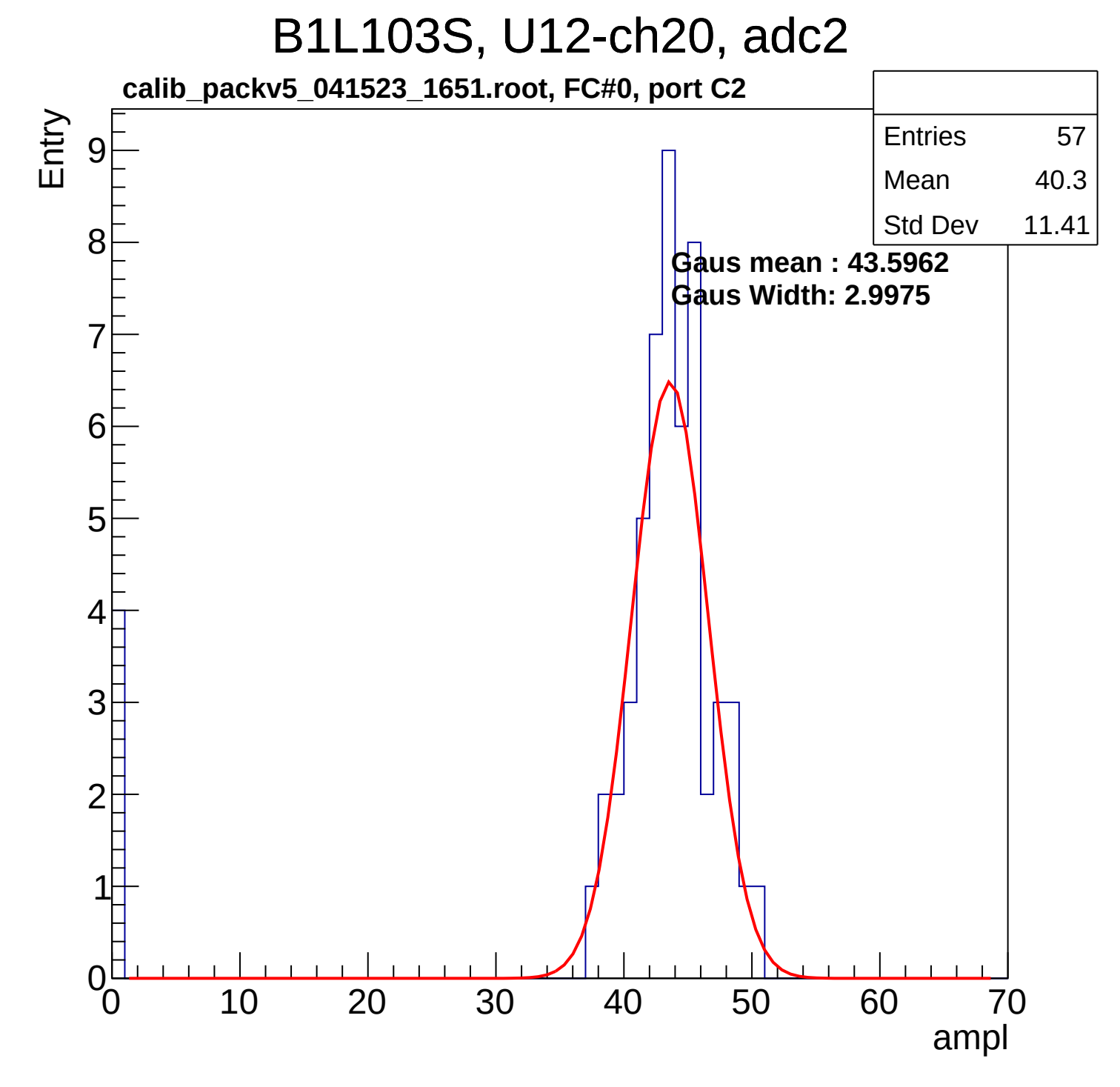
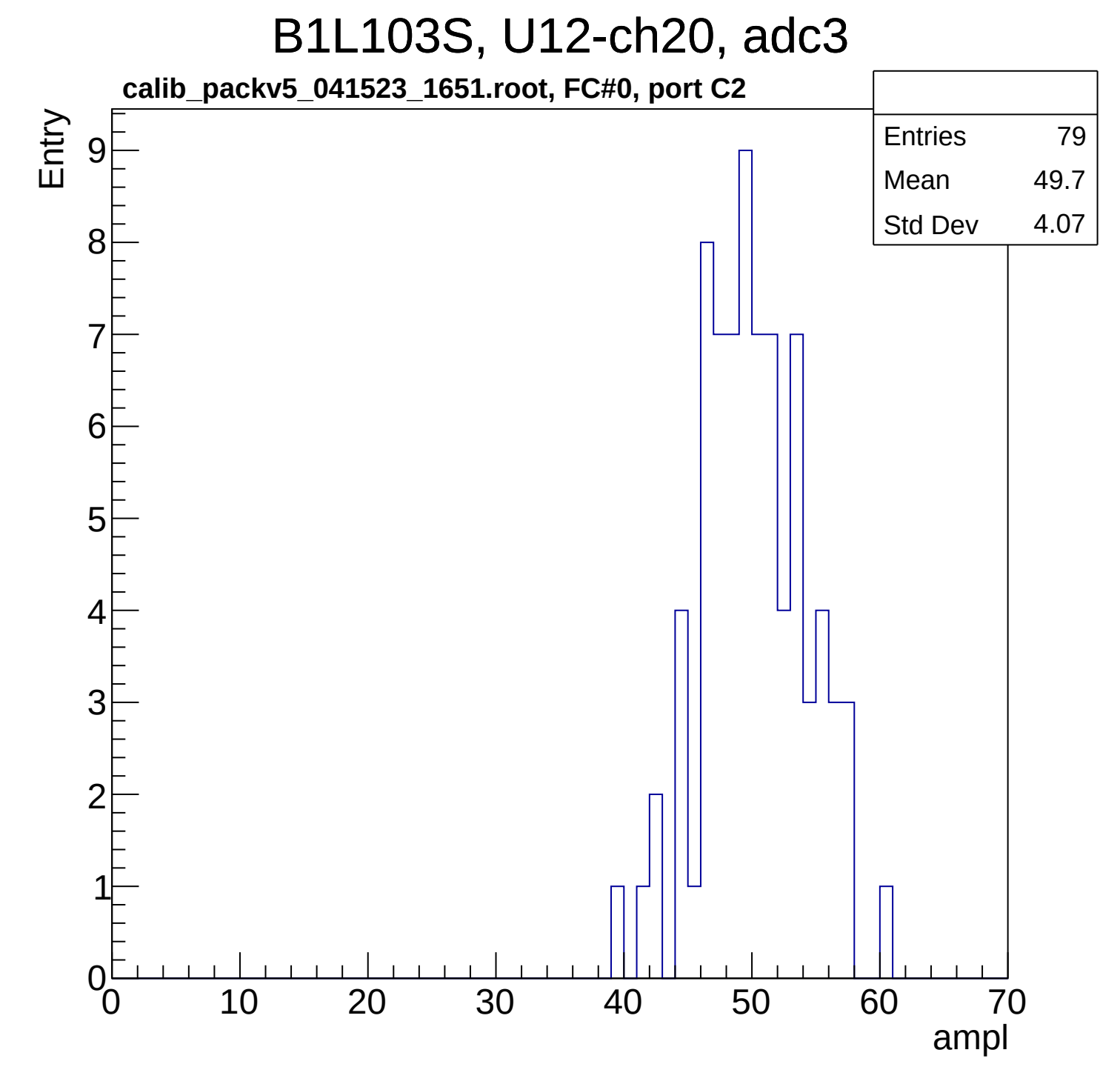
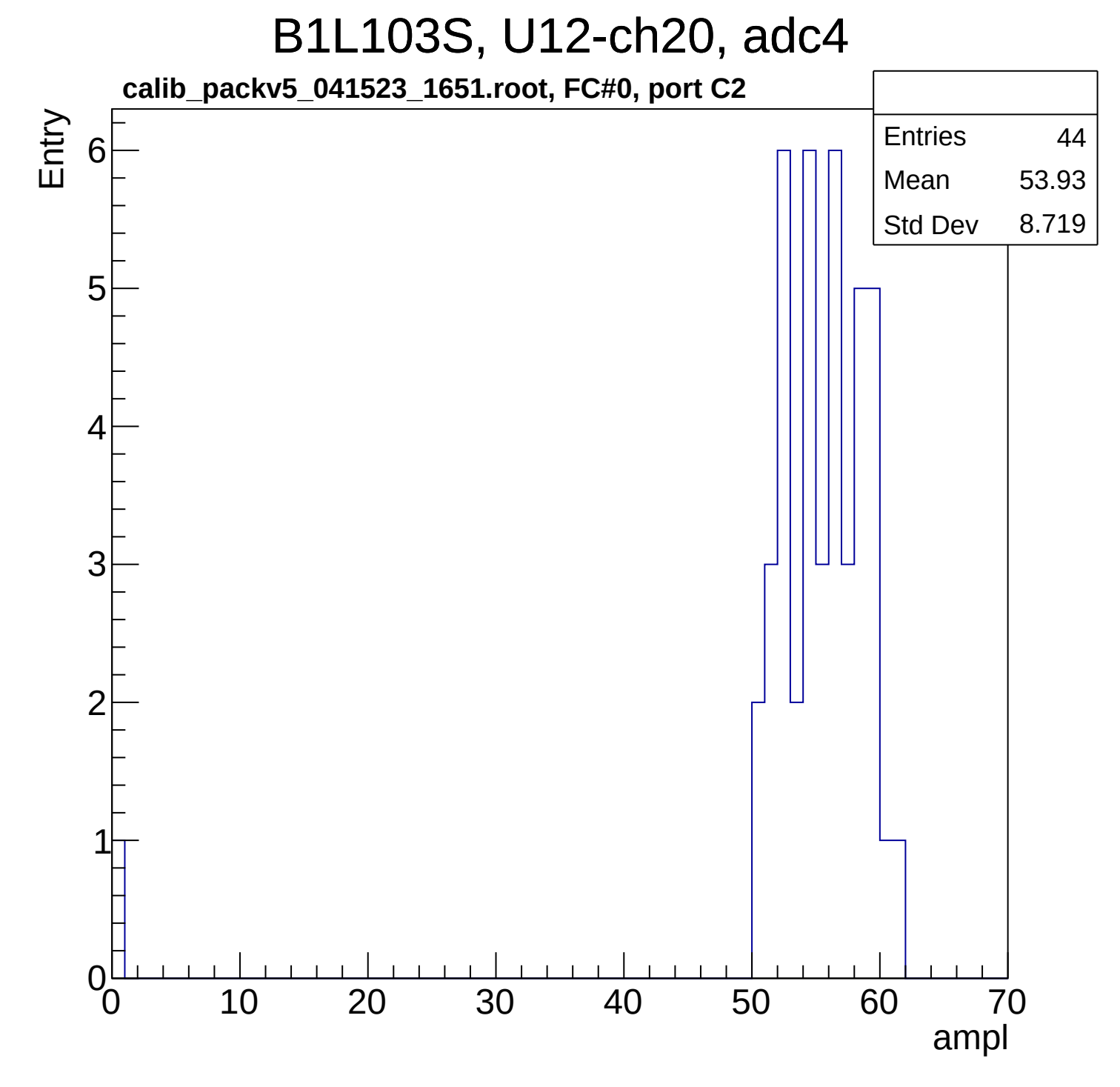
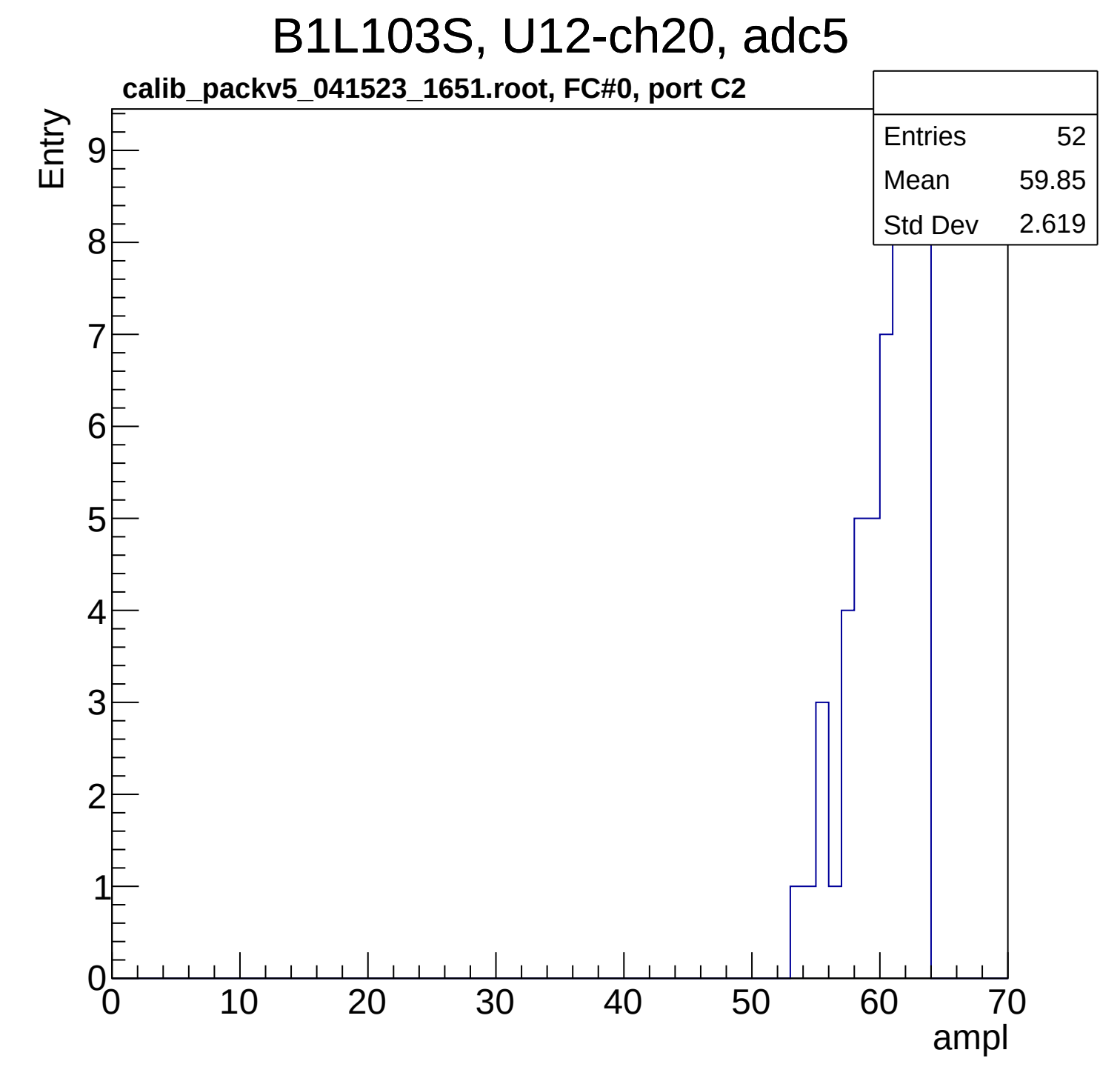

B1L103S, U12-ch20, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 40.3
Std Dev 11.41
Gaus mean : 43.5962
Gaus Width: 2.9975
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch20, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 49.7
Std Dev 4.07
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch20, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 53.93
Std Dev 8.719
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U12-ch20, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 59.85
Std Dev 2.619
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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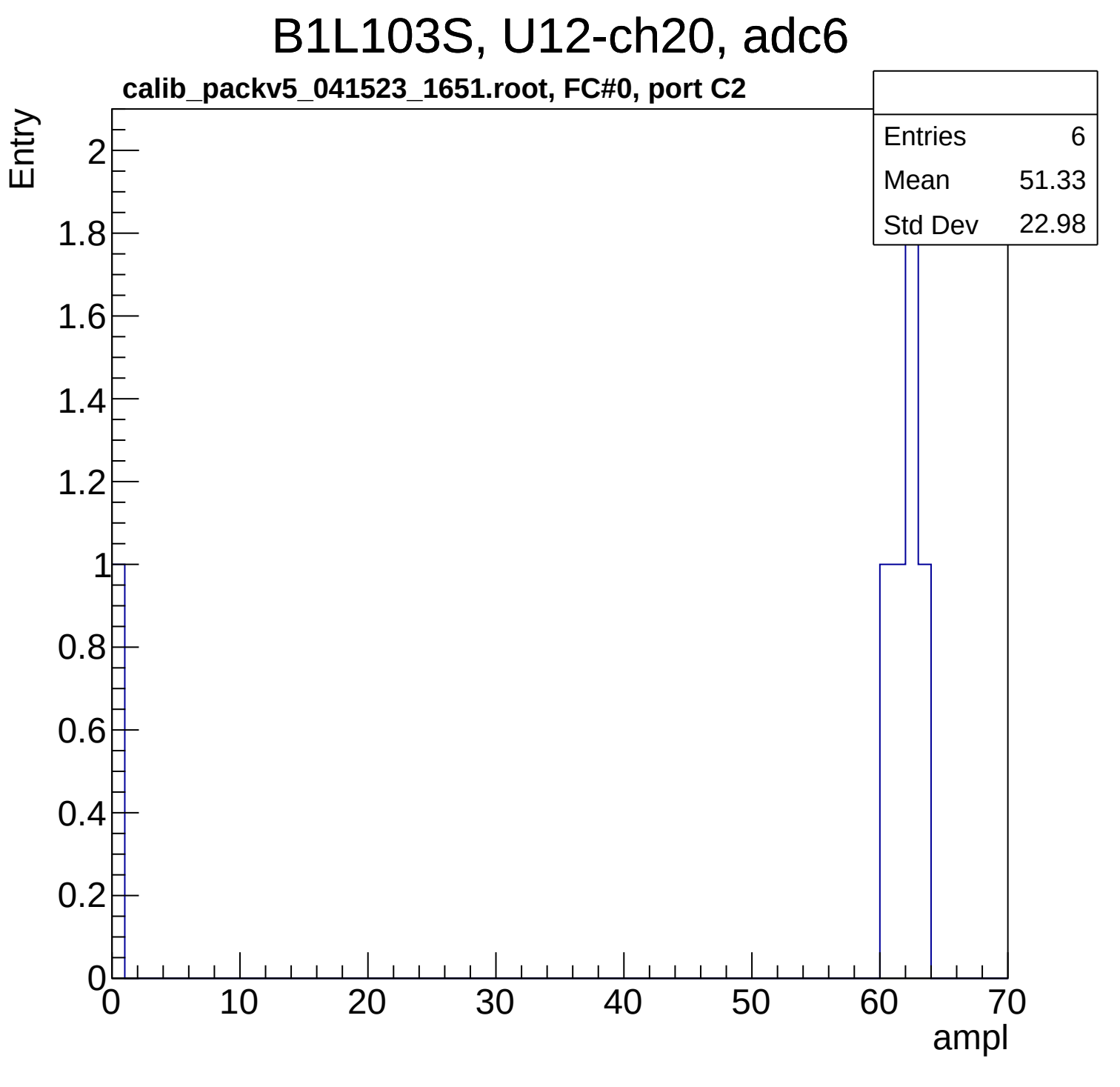
B1L103S, U12-ch20, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 51.33
Std Dev 22.98
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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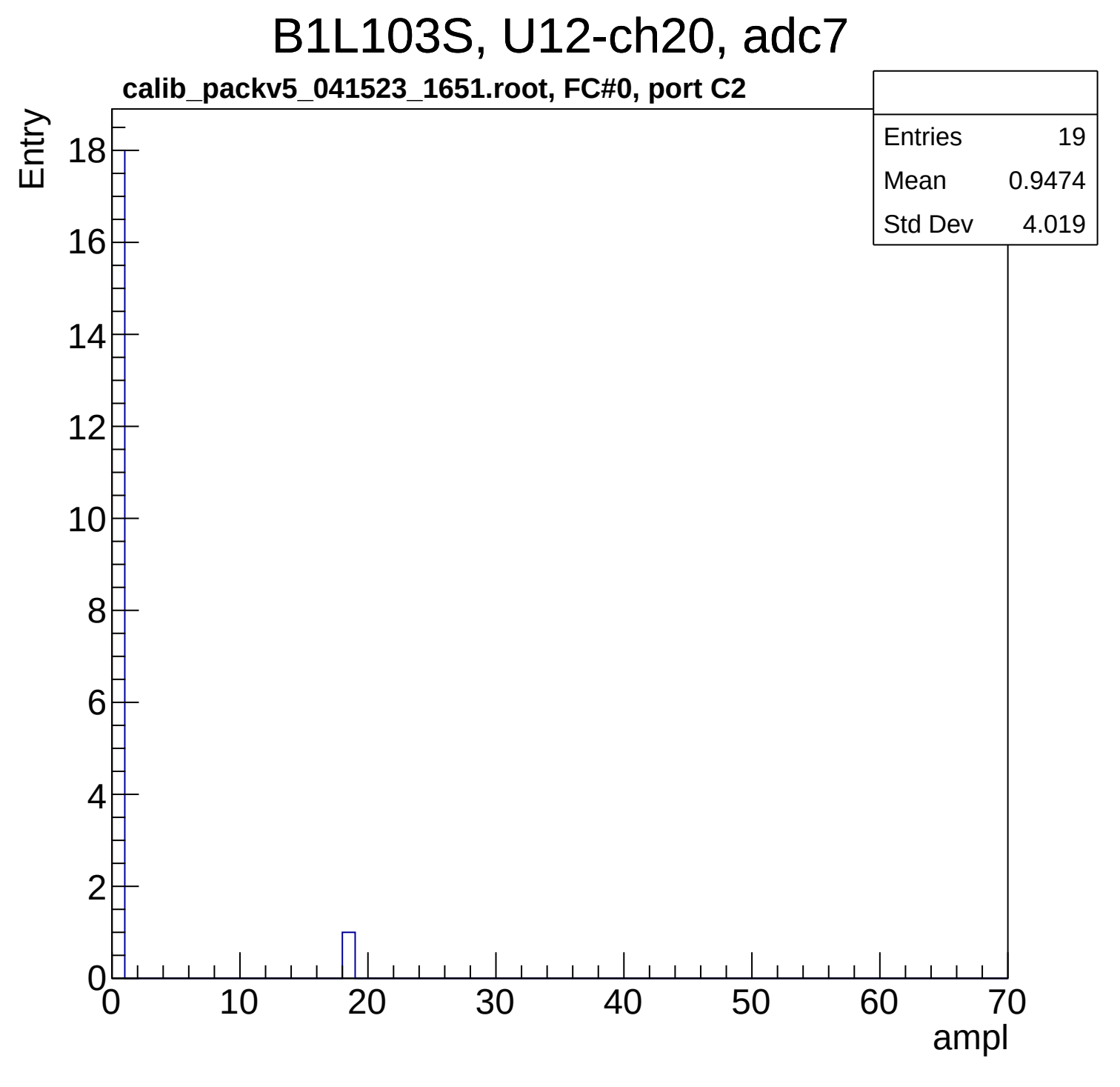
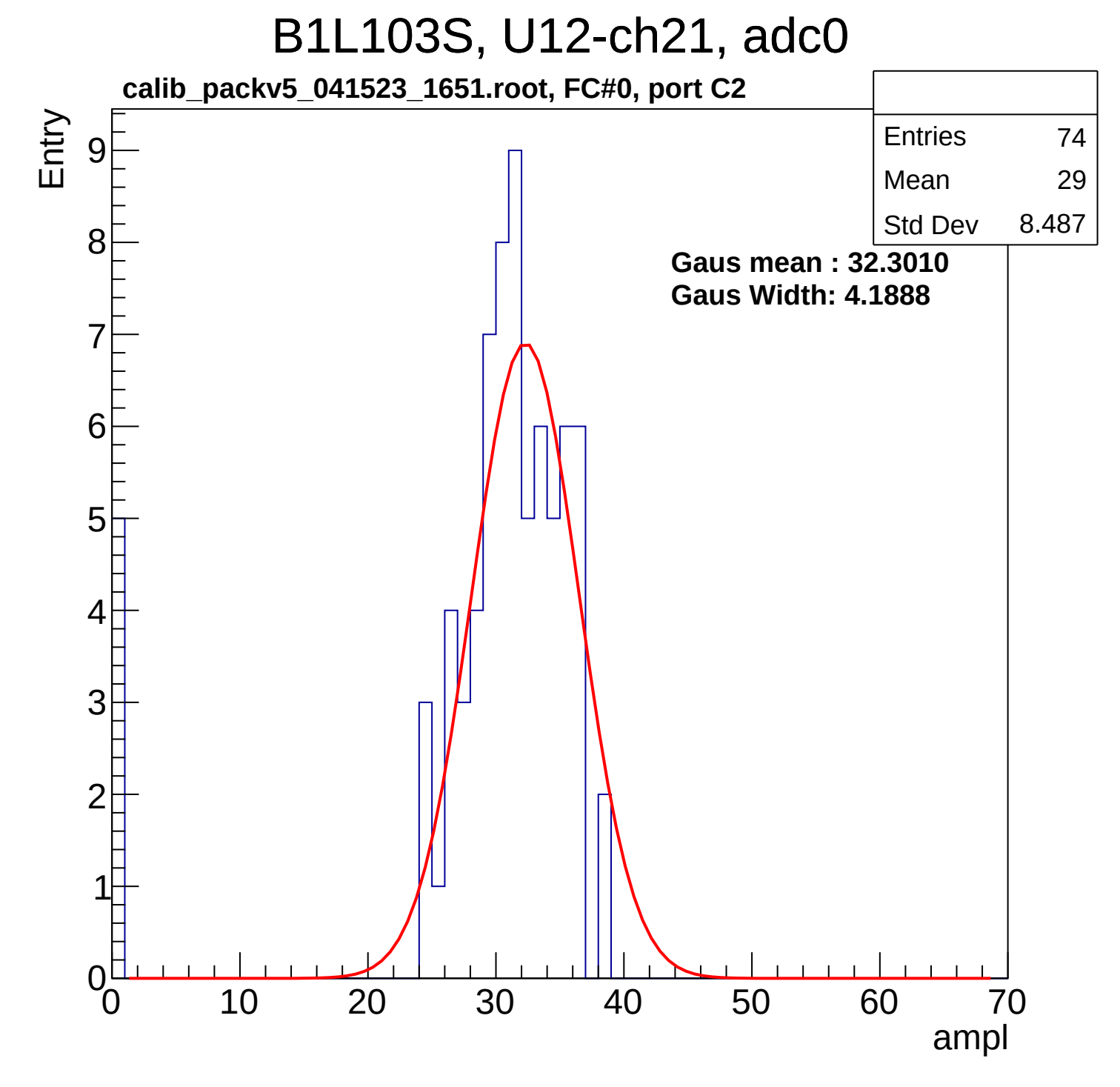
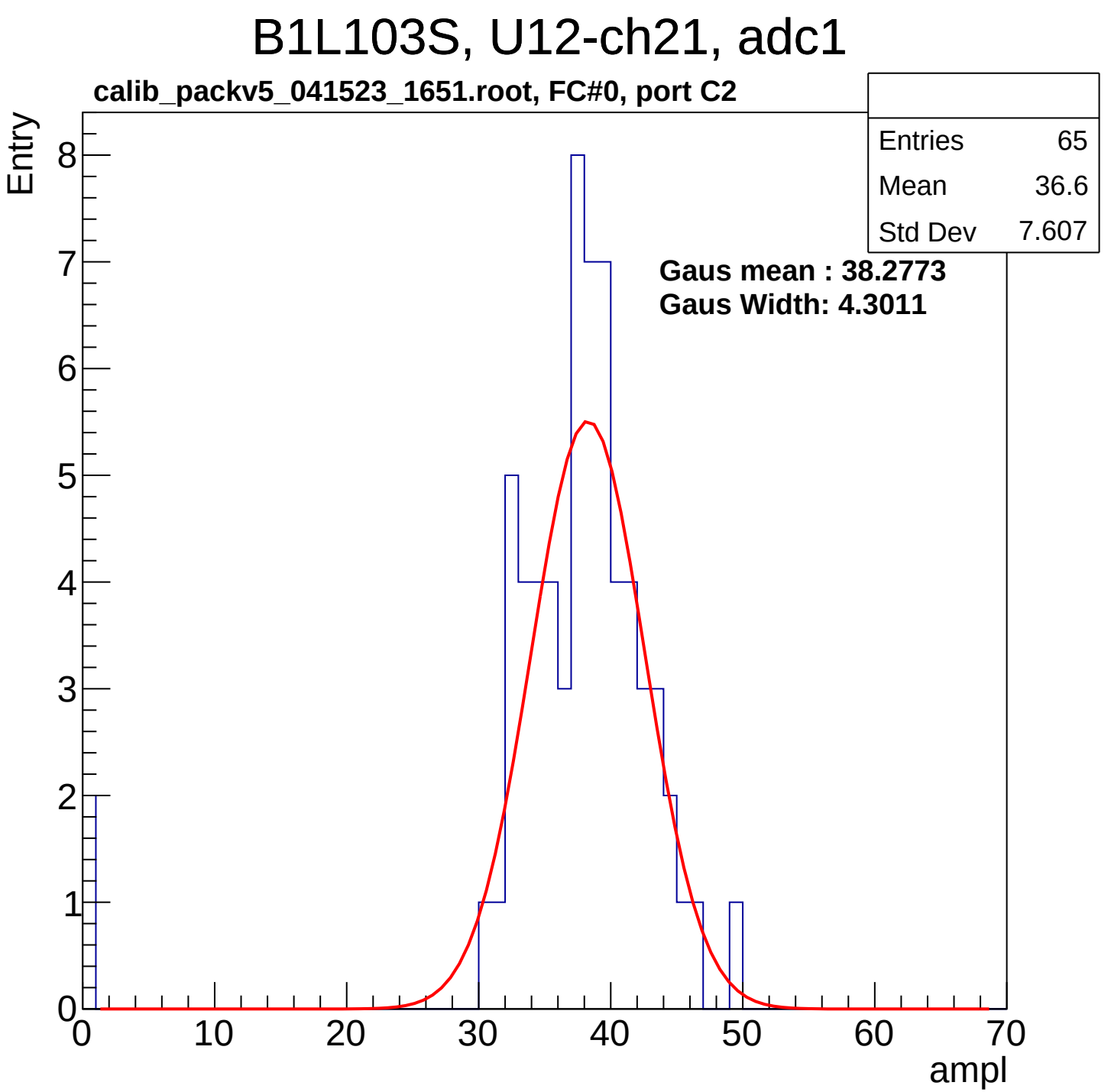

B1L103S, U12-ch20, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0.9474
Std Dev 4.019
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch21, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 29
Std Dev 8.487
Gaus mean : 32.3010
Gaus Width: 4.1888
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch21, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 36.6
Std Dev 7.607
Gaus mean : 38.2773
Gaus Width: 4.3011
Entry
ampl
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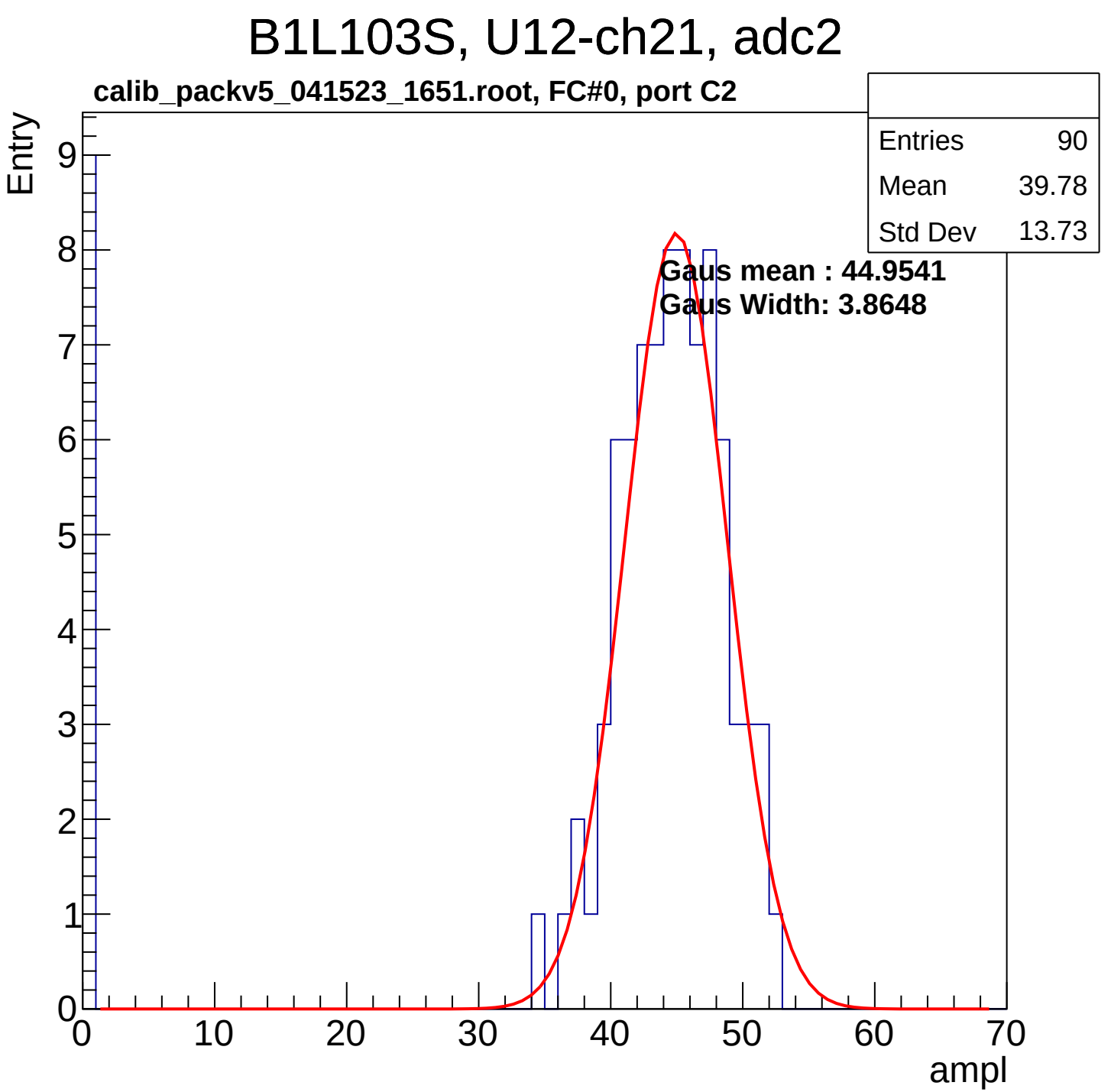
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U12-ch21, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 39.78
Std Dev 13.73
Gaus mean : 44.9541
Gaus Width: 3.8648
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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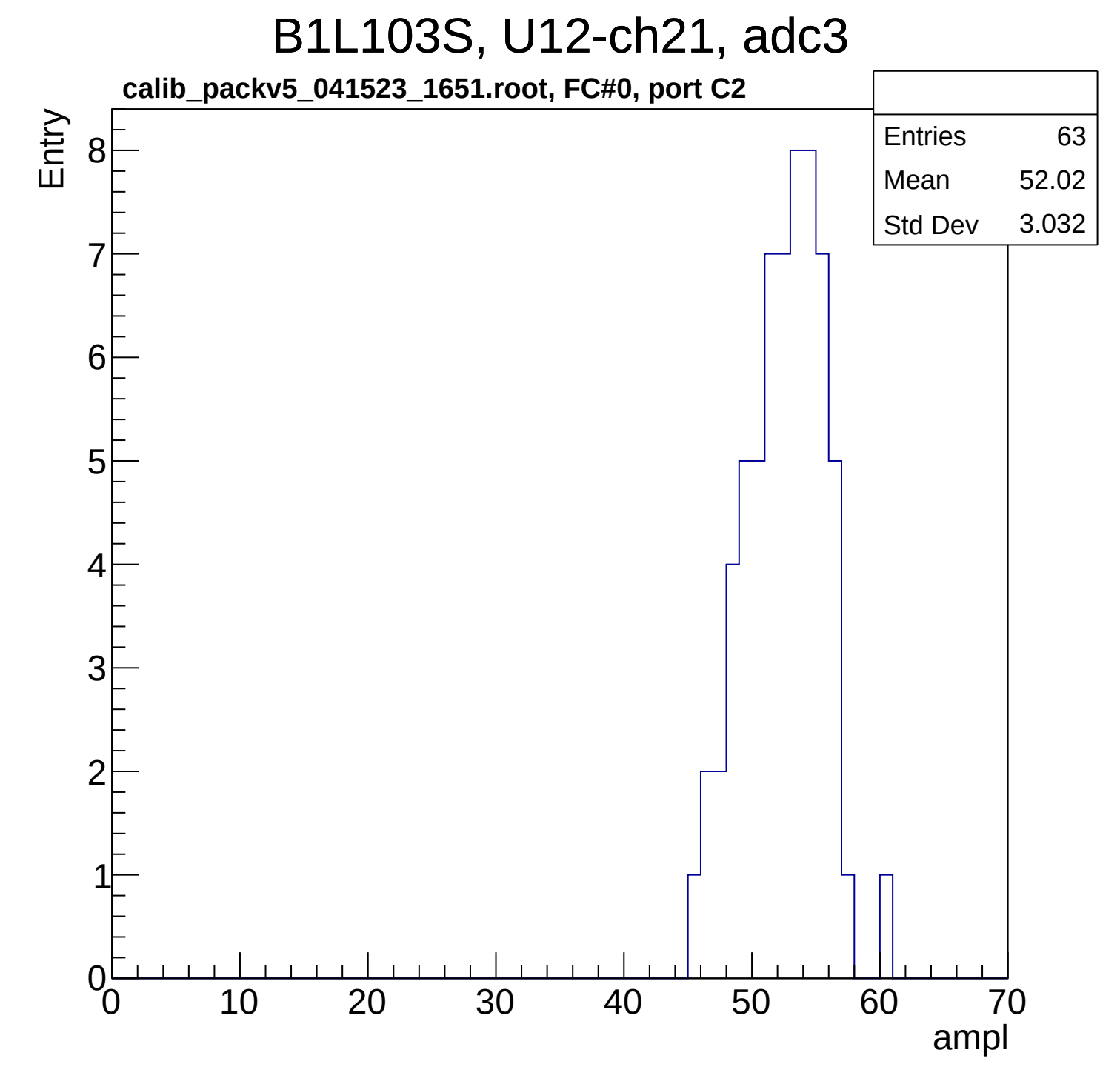
B1L103S, U12-ch21, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 52.02
Std Dev 3.032
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
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40
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60
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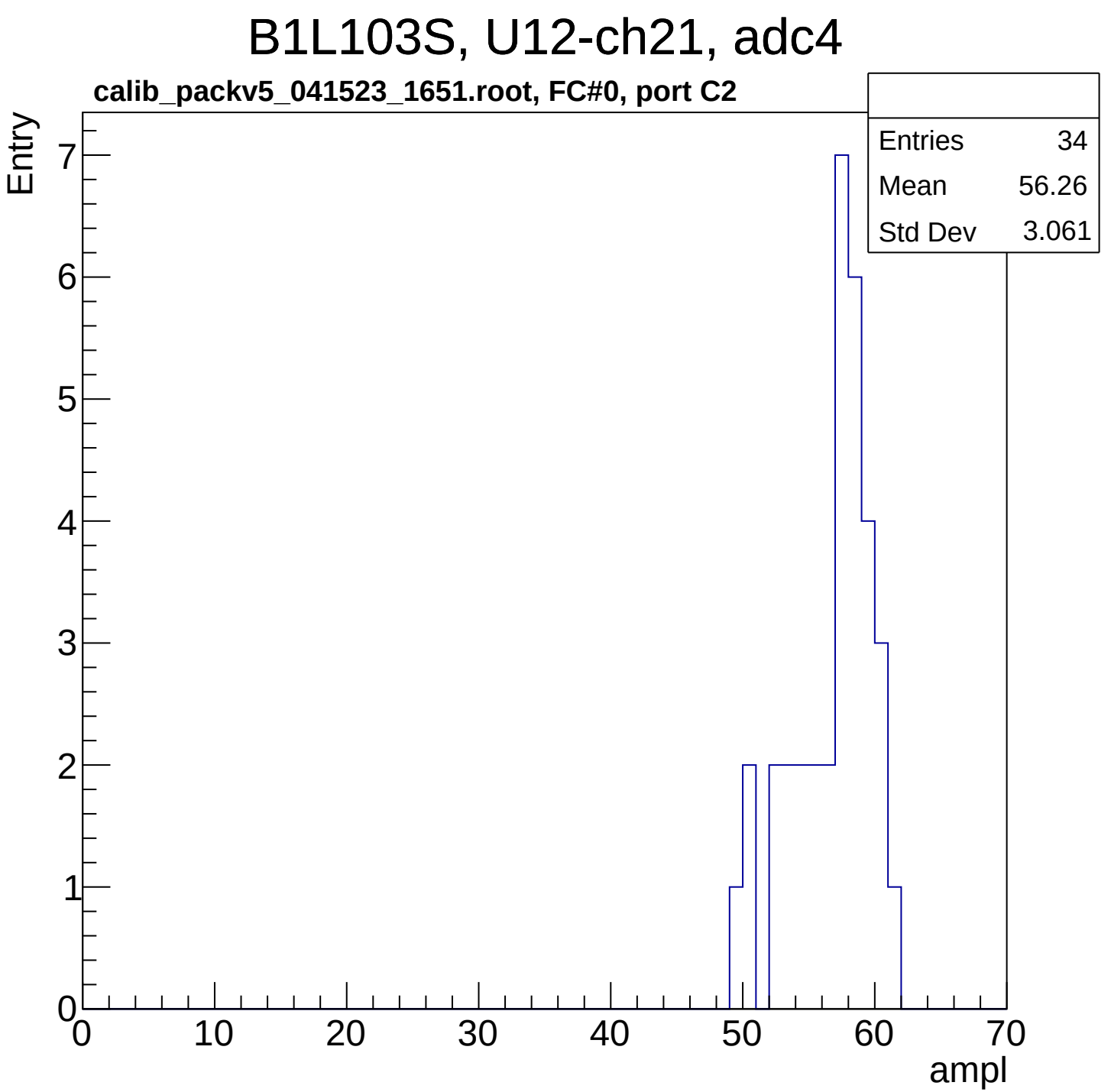
B1L103S, U12-ch21, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 56.26
Std Dev 3.061
Entry
ampl
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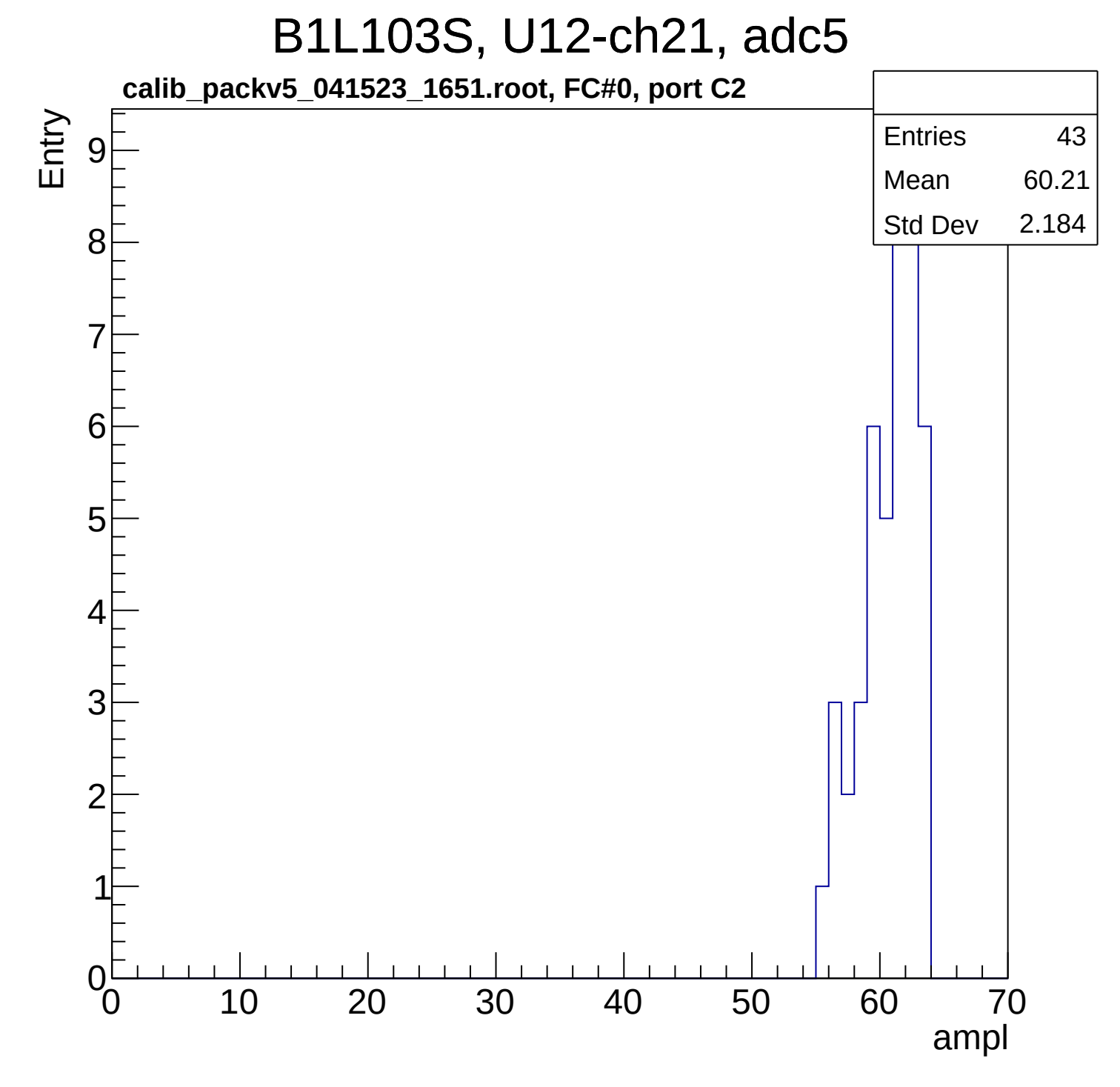
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U12-ch21, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 60.21
Std Dev 2.184
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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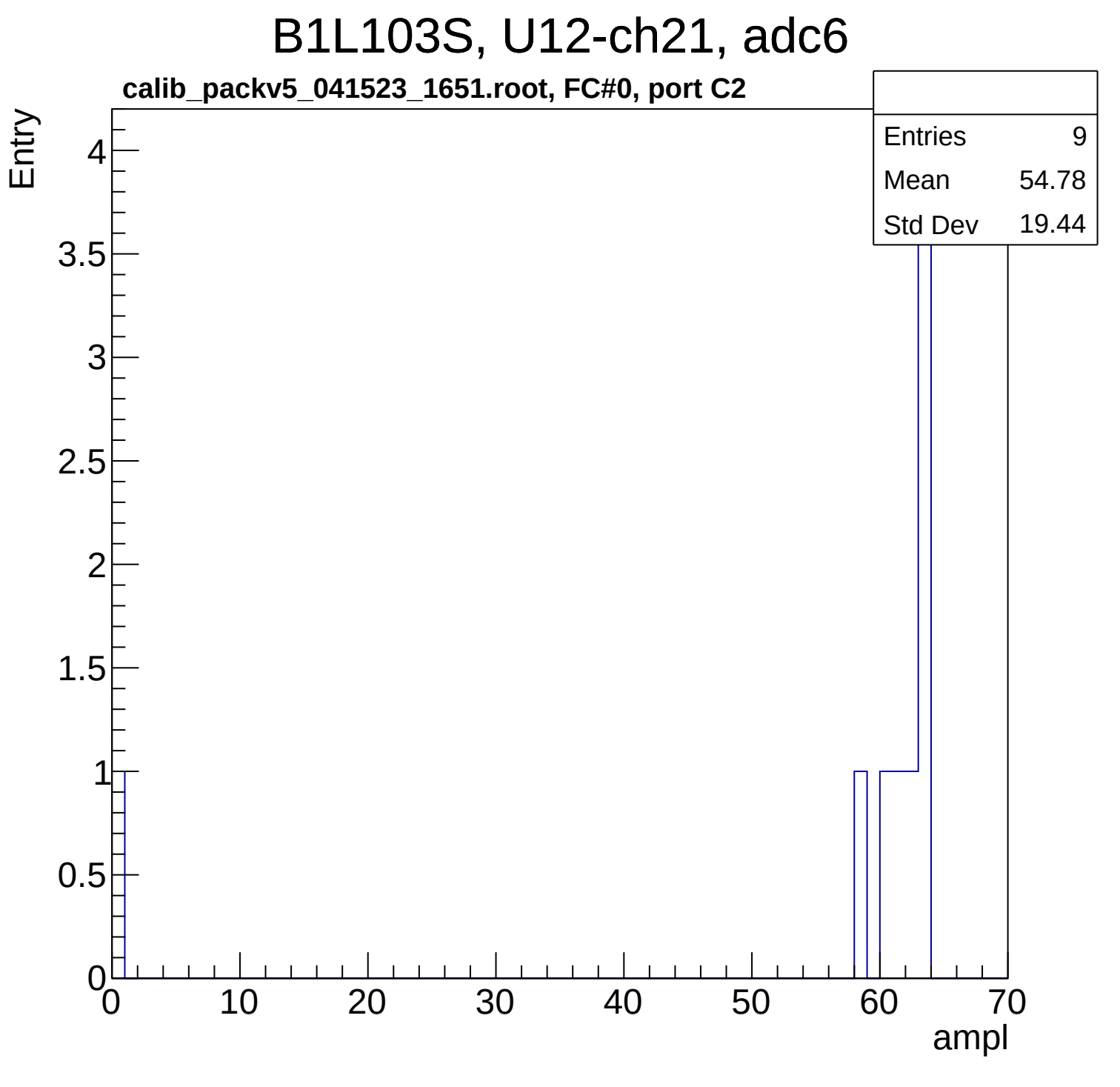
60
70


B1L103S, U12-ch21, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 54.78
Std Dev 19.44
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
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60
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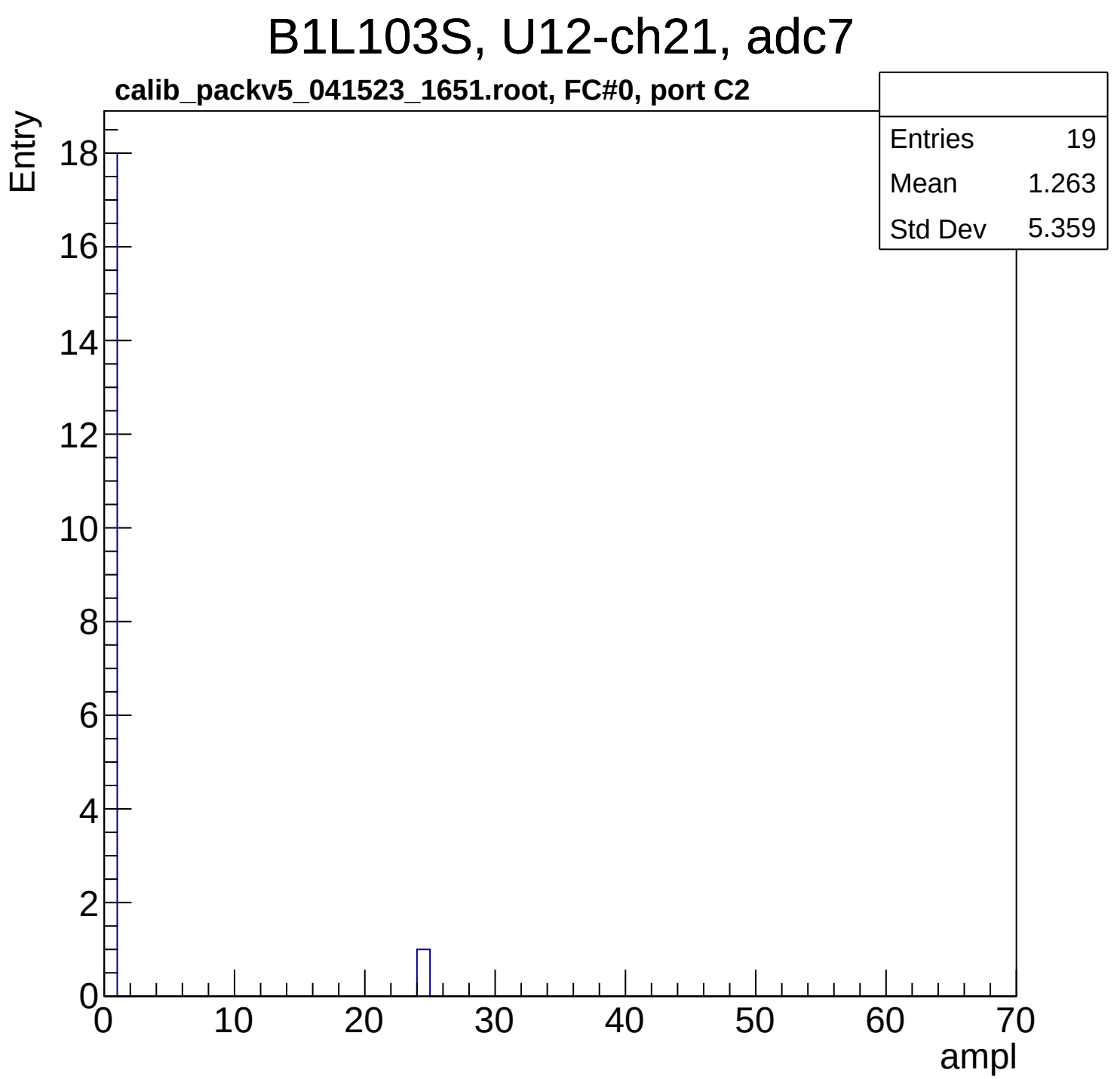
B1L103S, U12-ch21, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.263
Std Dev 5.359
Entry
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6
8
10
12
14
16
18
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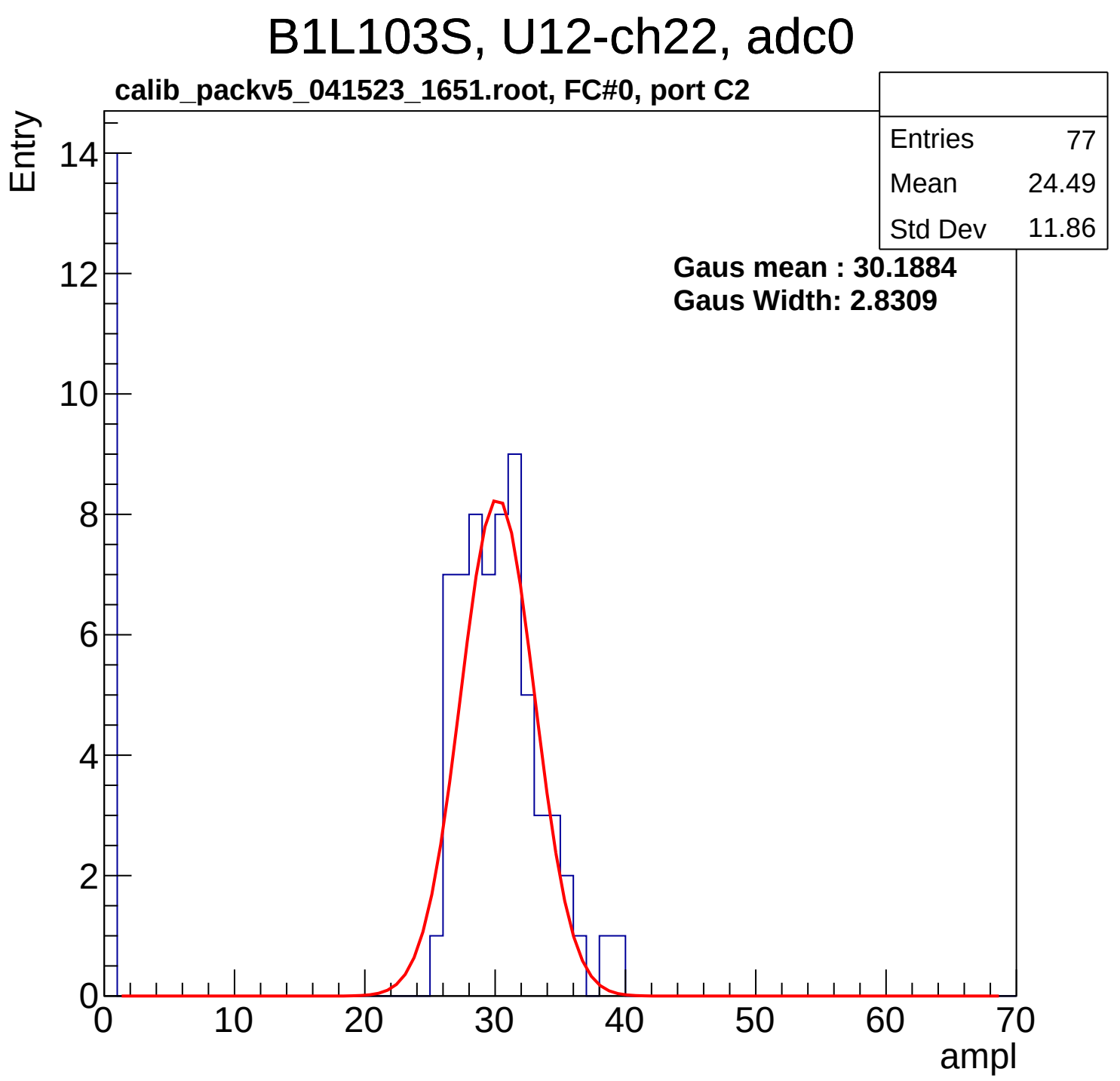
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch22, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 24.49
Std Dev 11.86
Gaus mean : 30.1884
Gaus Width: 2.8309
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
30
40
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60
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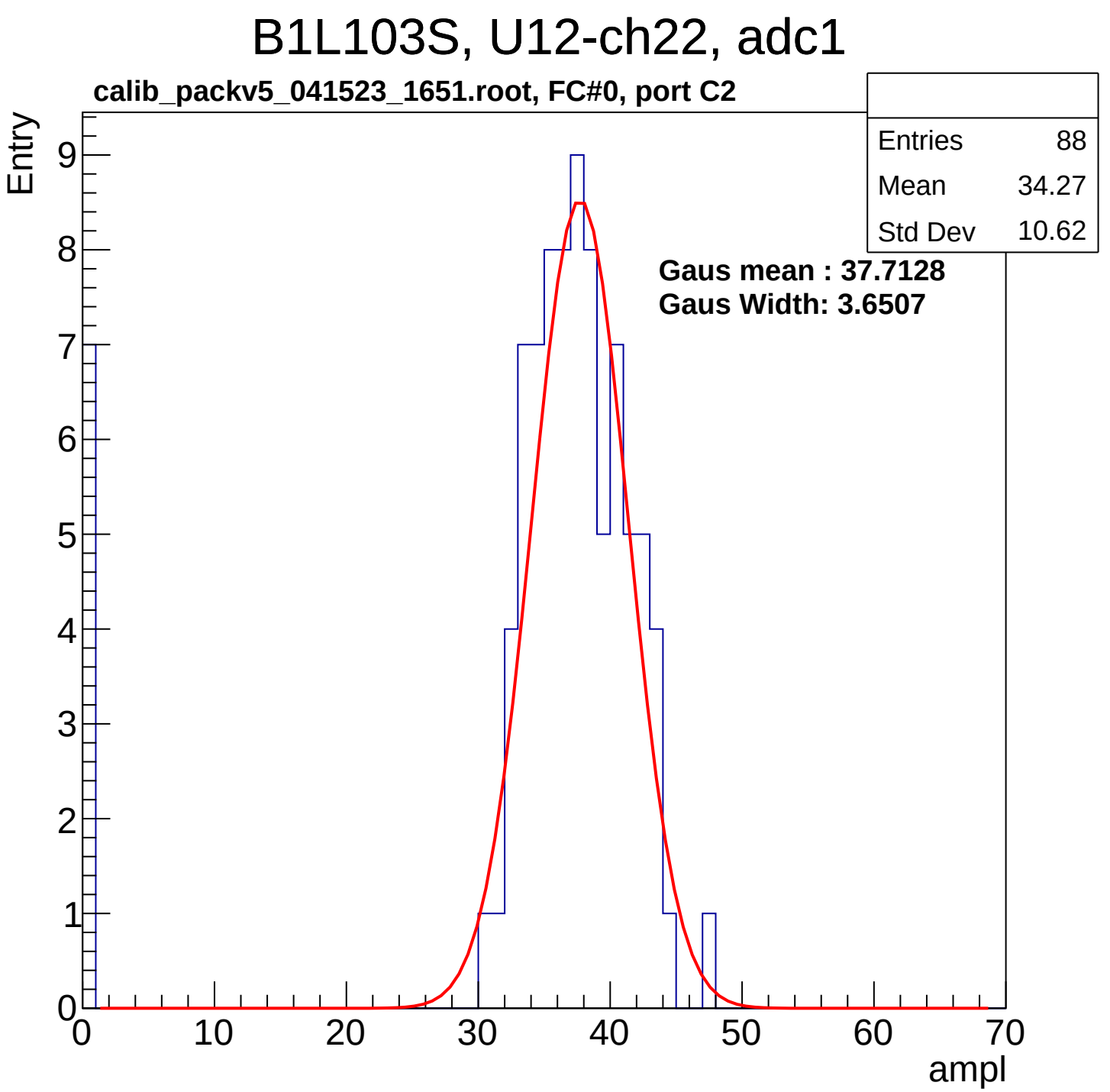
B1L103S, U12-ch22, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 34.27
Std Dev 10.62
Gaus mean : 37.7128
Gaus Width: 3.6507
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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60
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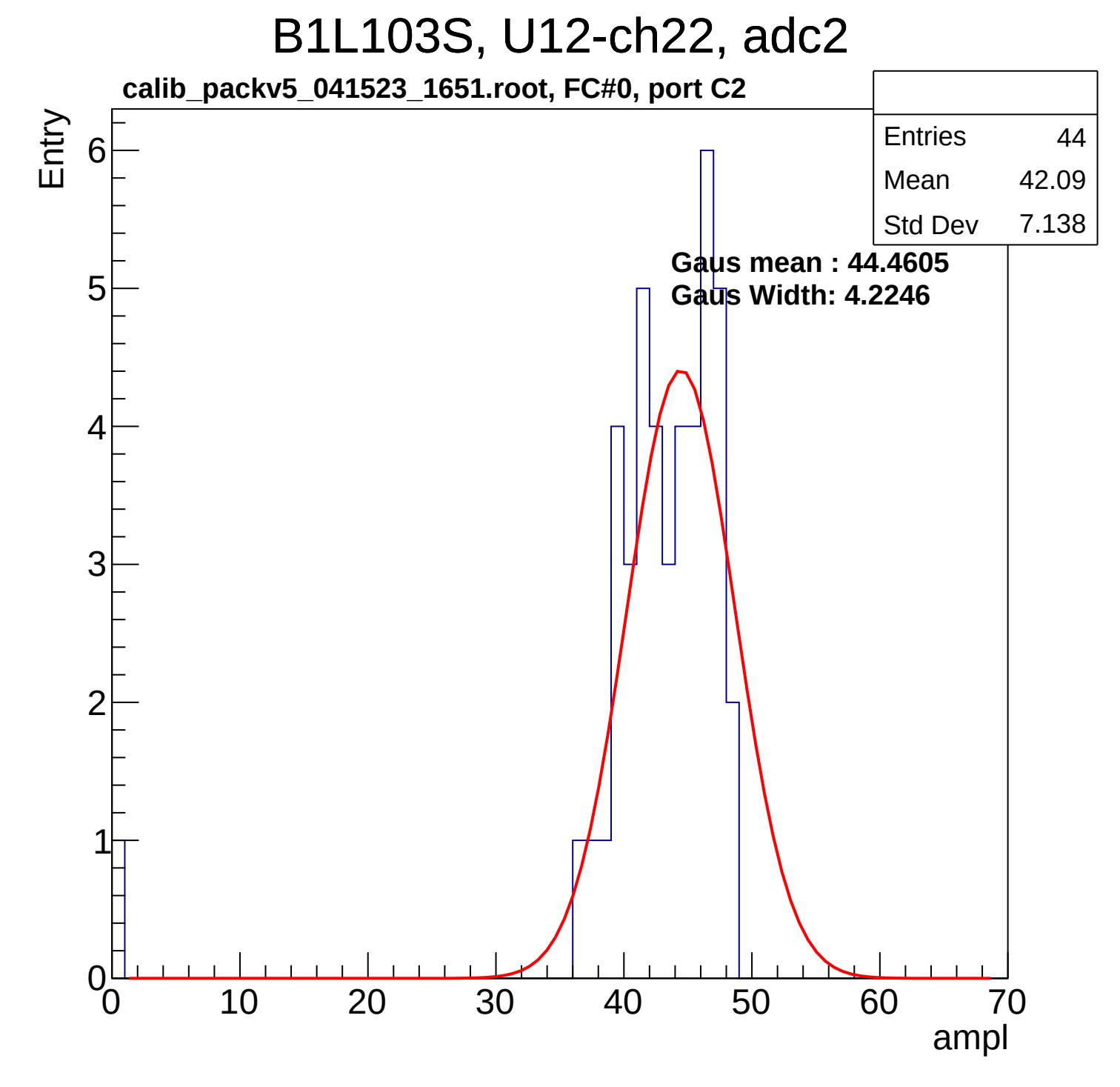
B1L103S, U12-ch22, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 42.09
Std Dev 7.138
Gaus mean : 44.4605
Gaus Width: 4.2246
Entry
ampl
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3
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0
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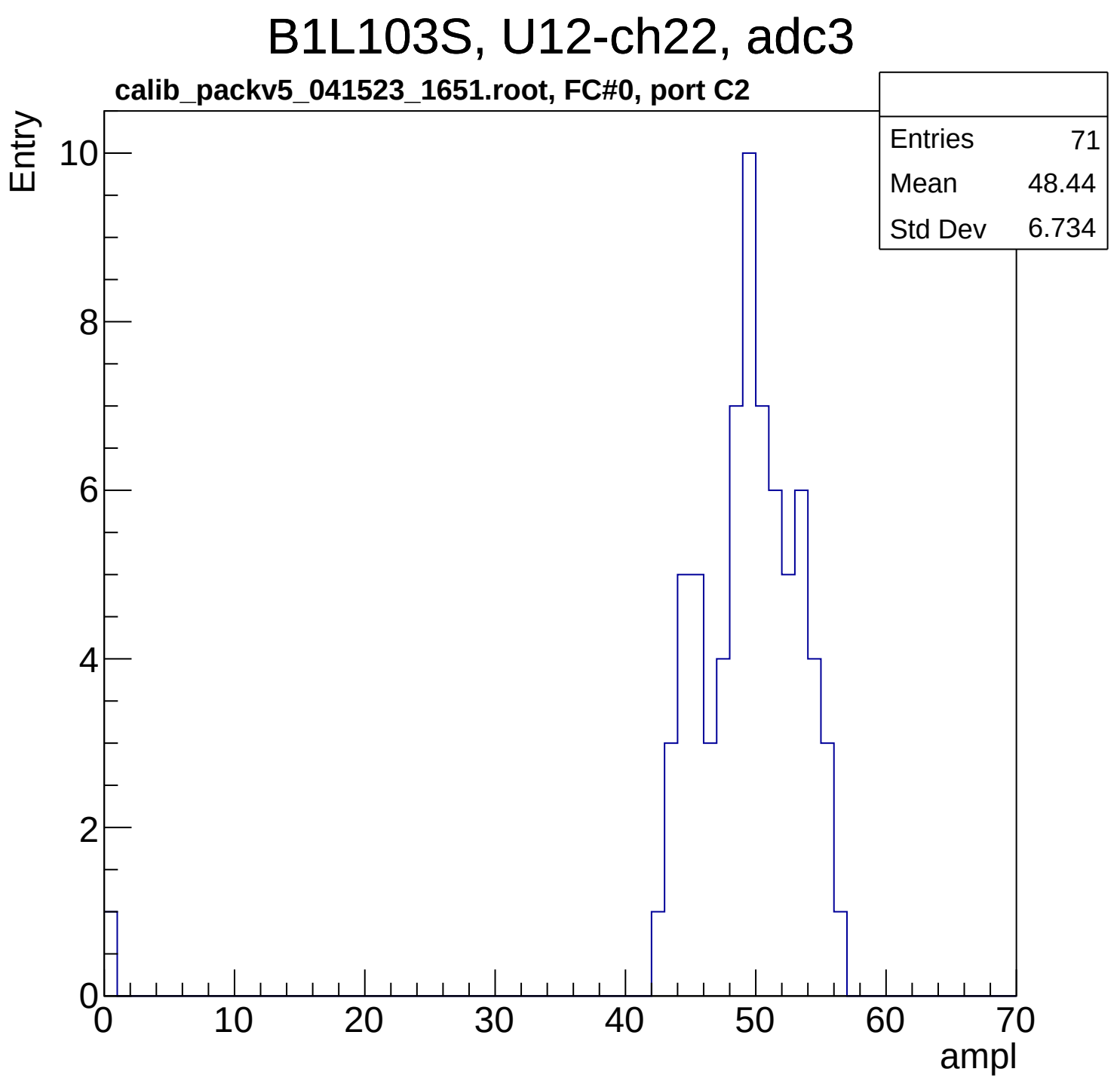
B1L103S, U12-ch22, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 48.44
Std Dev 6.734
Entry
ampl
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0
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20
30
40
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60
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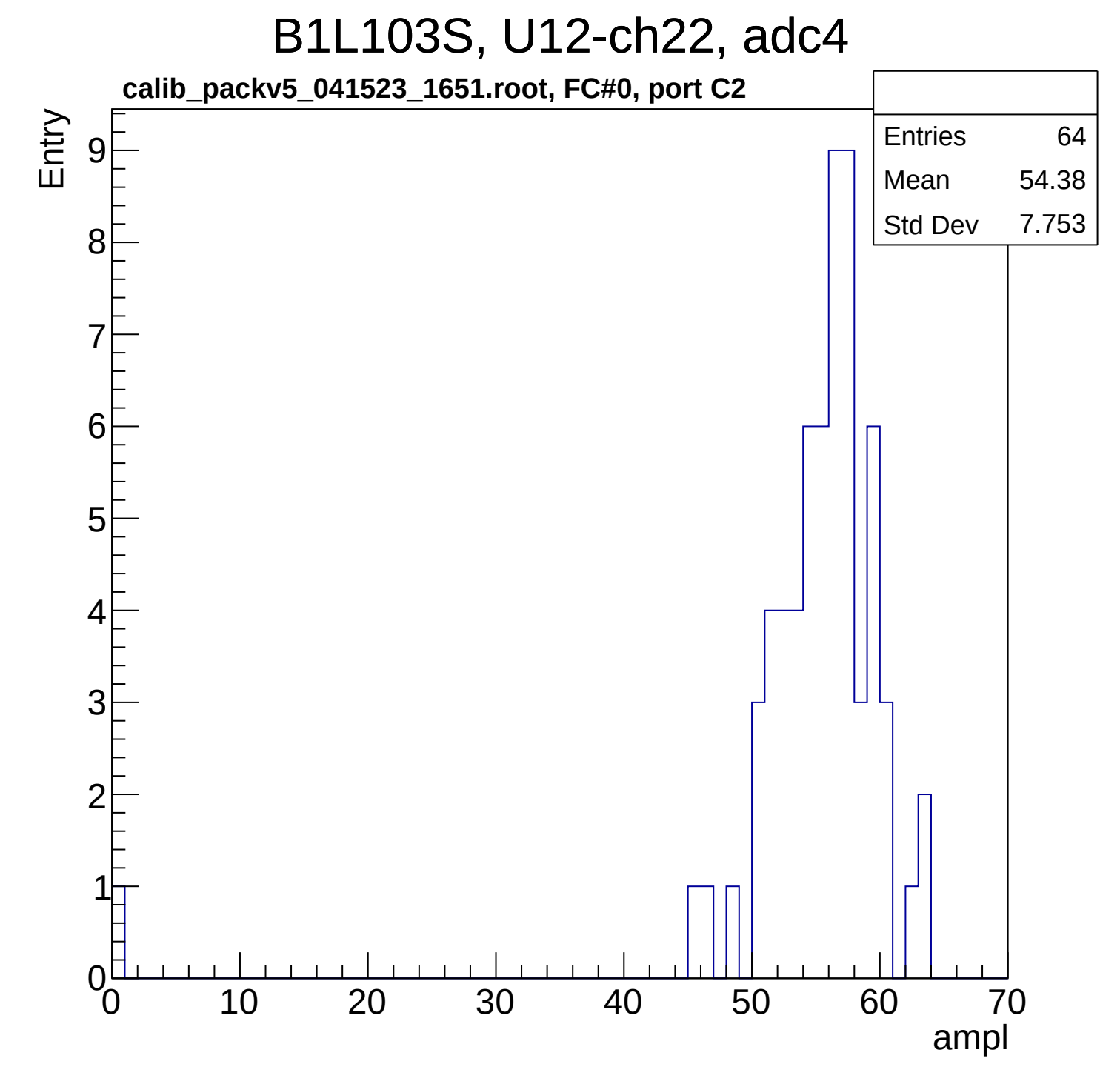
B1L103S, U12-ch22, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 54.38
Std Dev 7.753
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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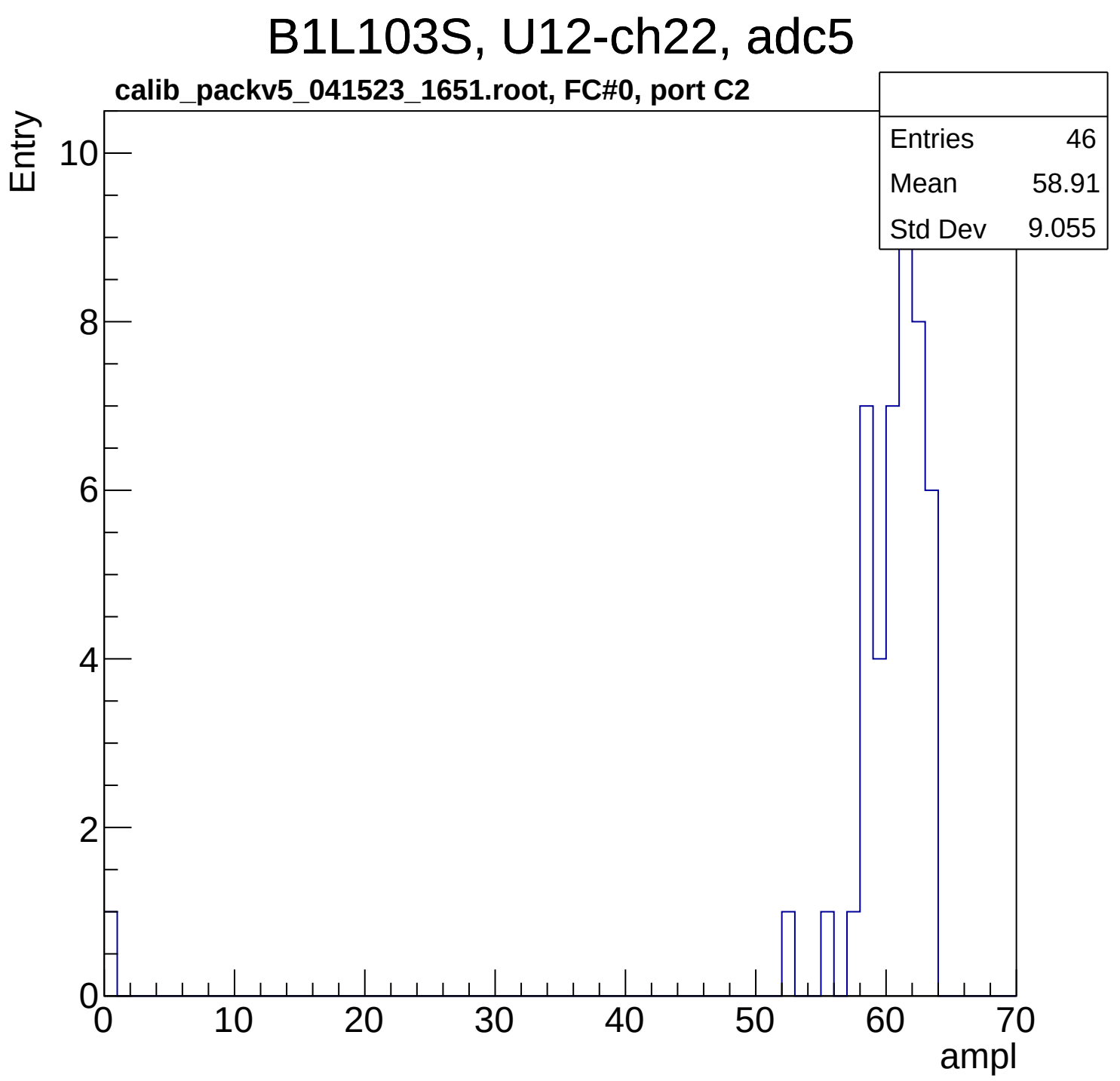
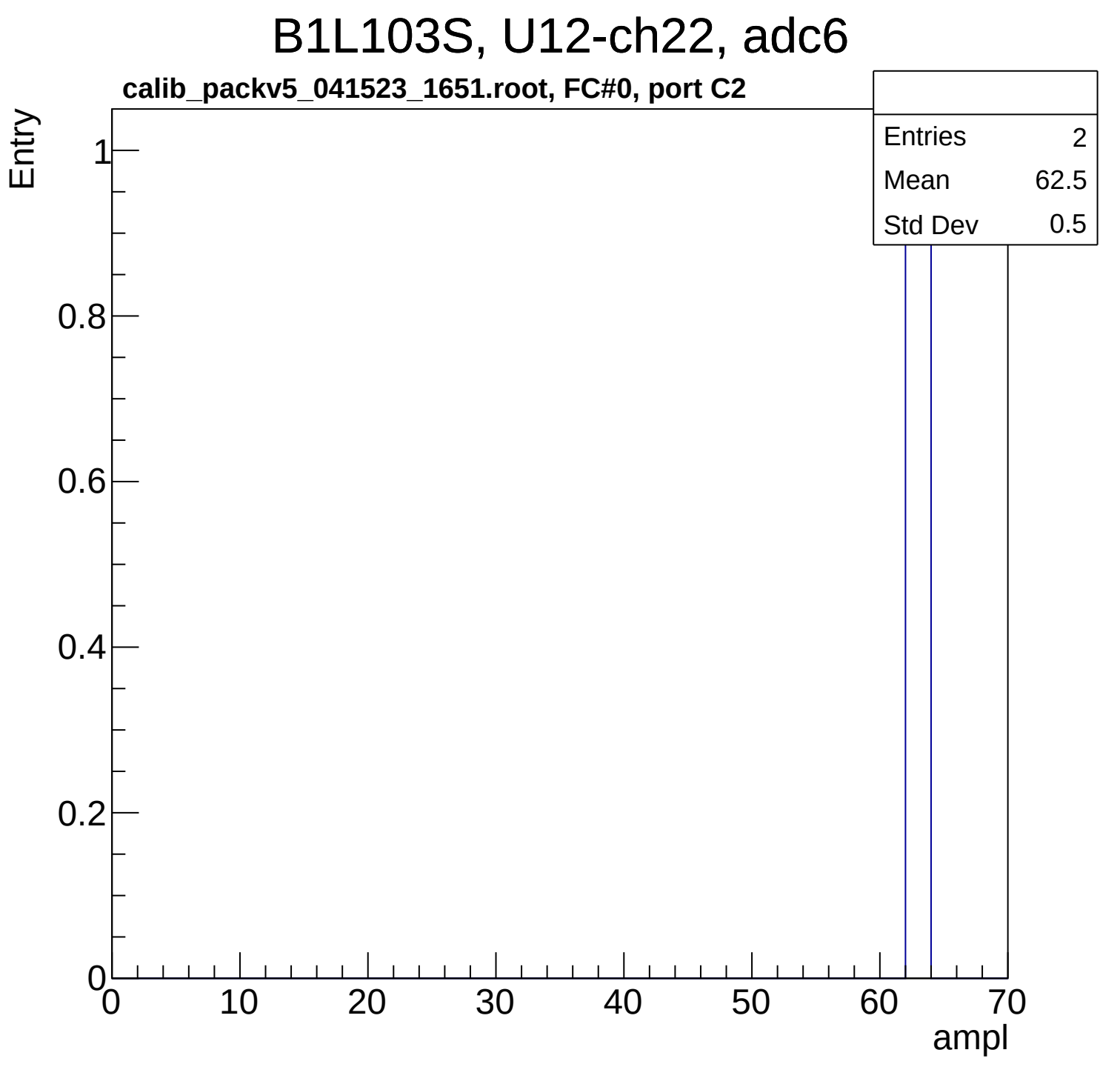
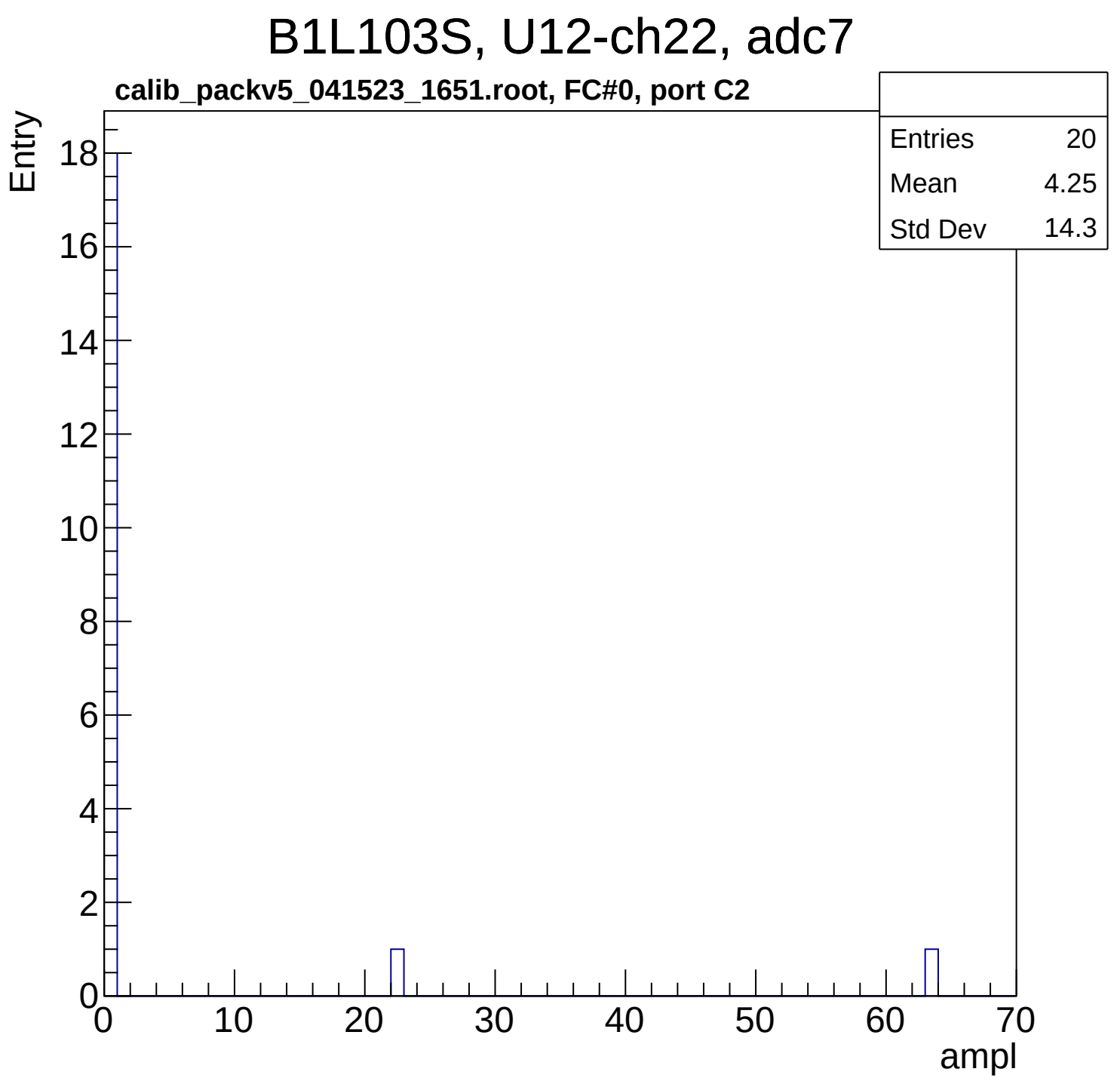

B1L103S, U12-ch22, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.91
Std Dev 9.055
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch22, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch22, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.25
Std Dev 14.3
Entry
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6
8
10
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14
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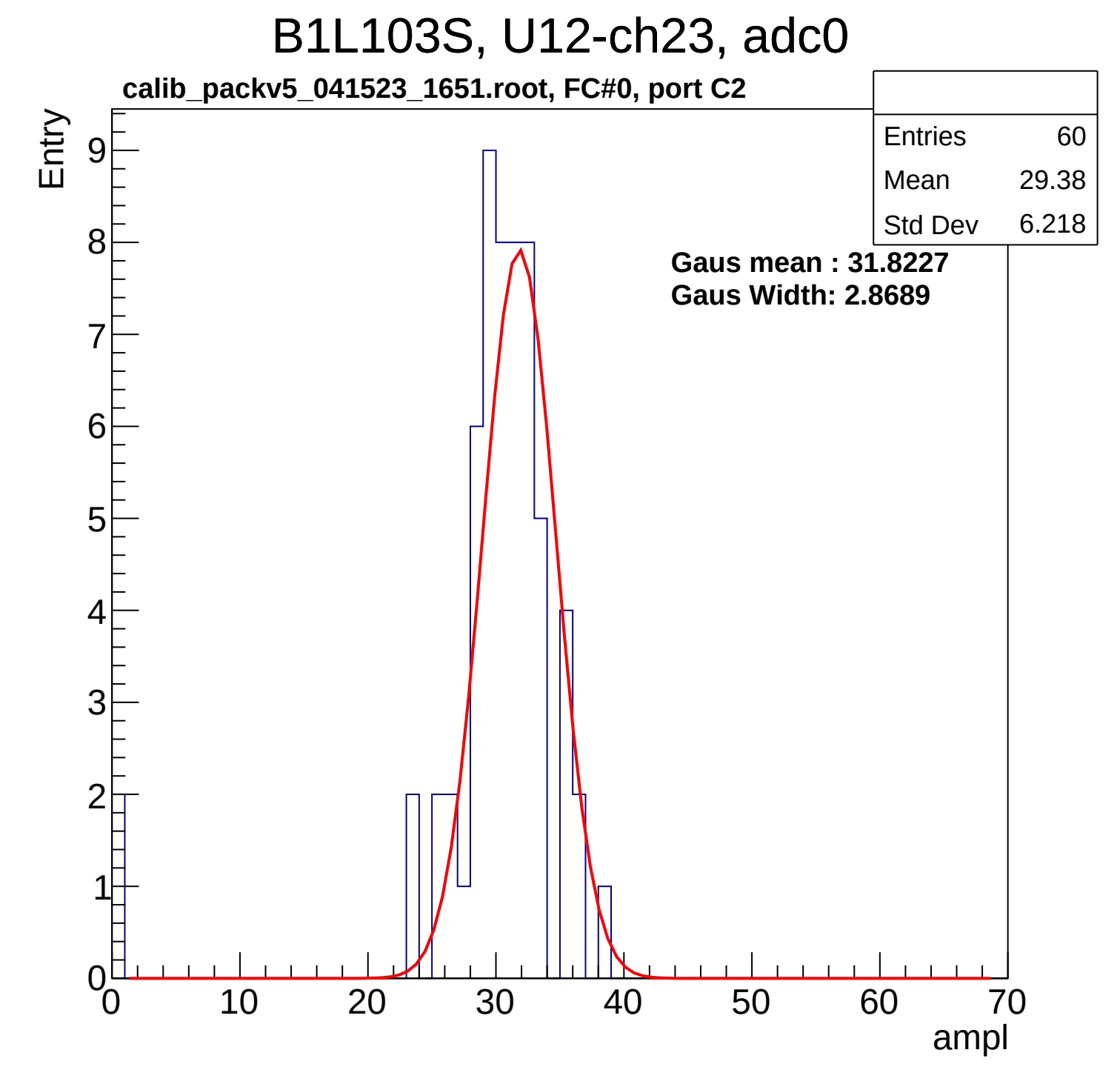
60
70
ampl


B1L103S, U12-ch23, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 29.38
Std Dev 6.218
Gaus mean : 31.8227
Gaus Width: 2.8689
Entry
ampl
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2
3
4
5
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7
8
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0
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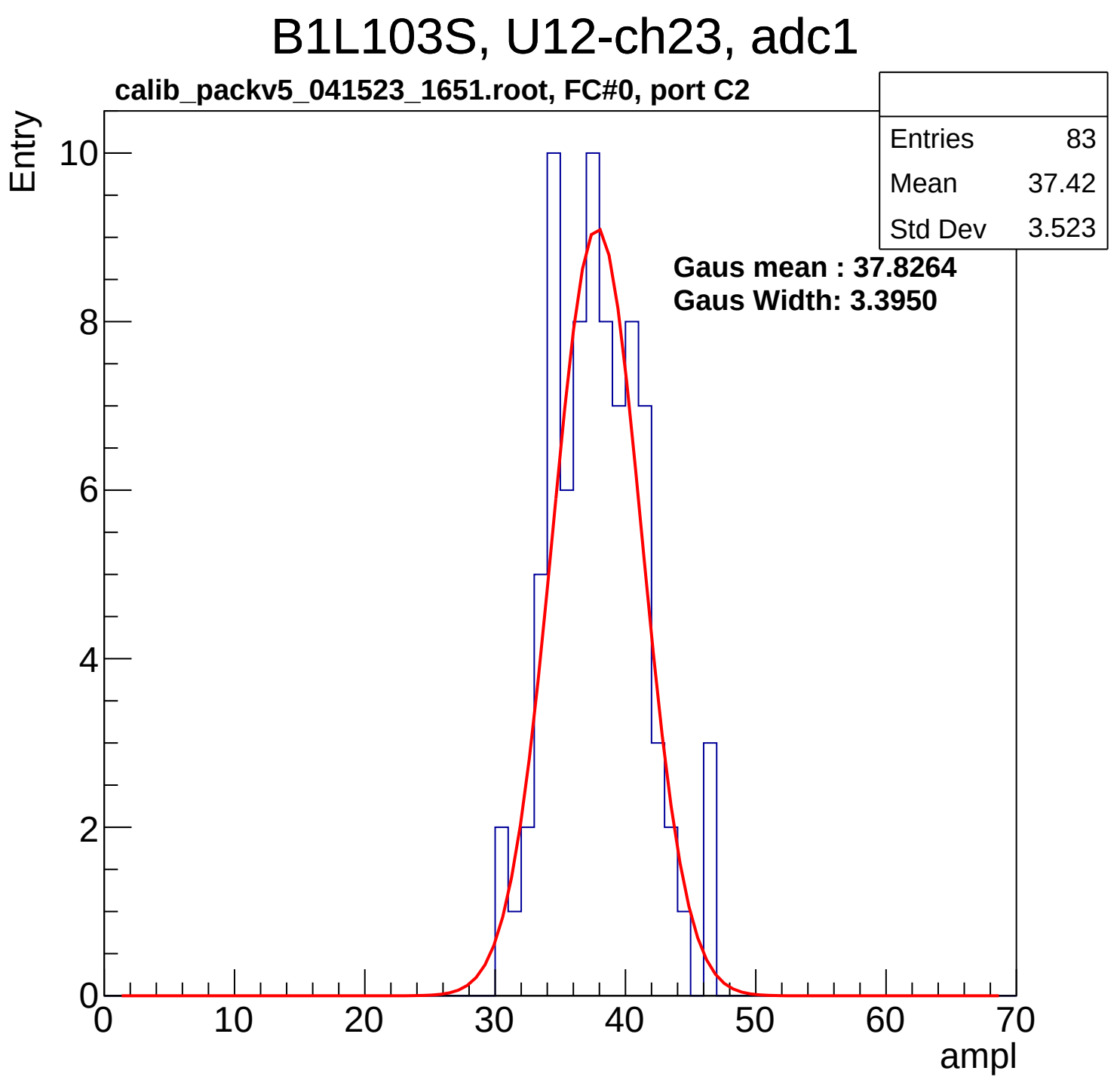
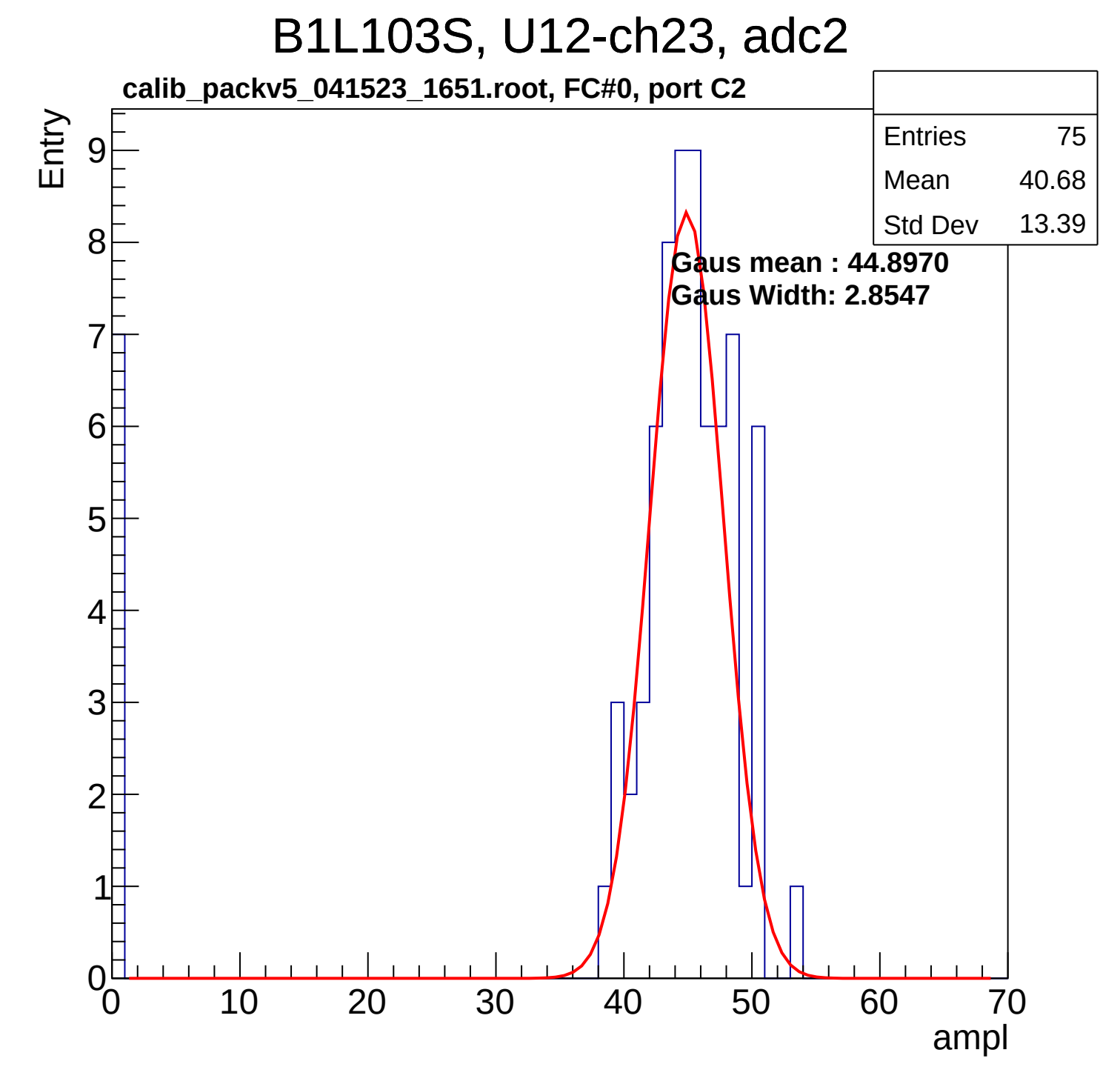
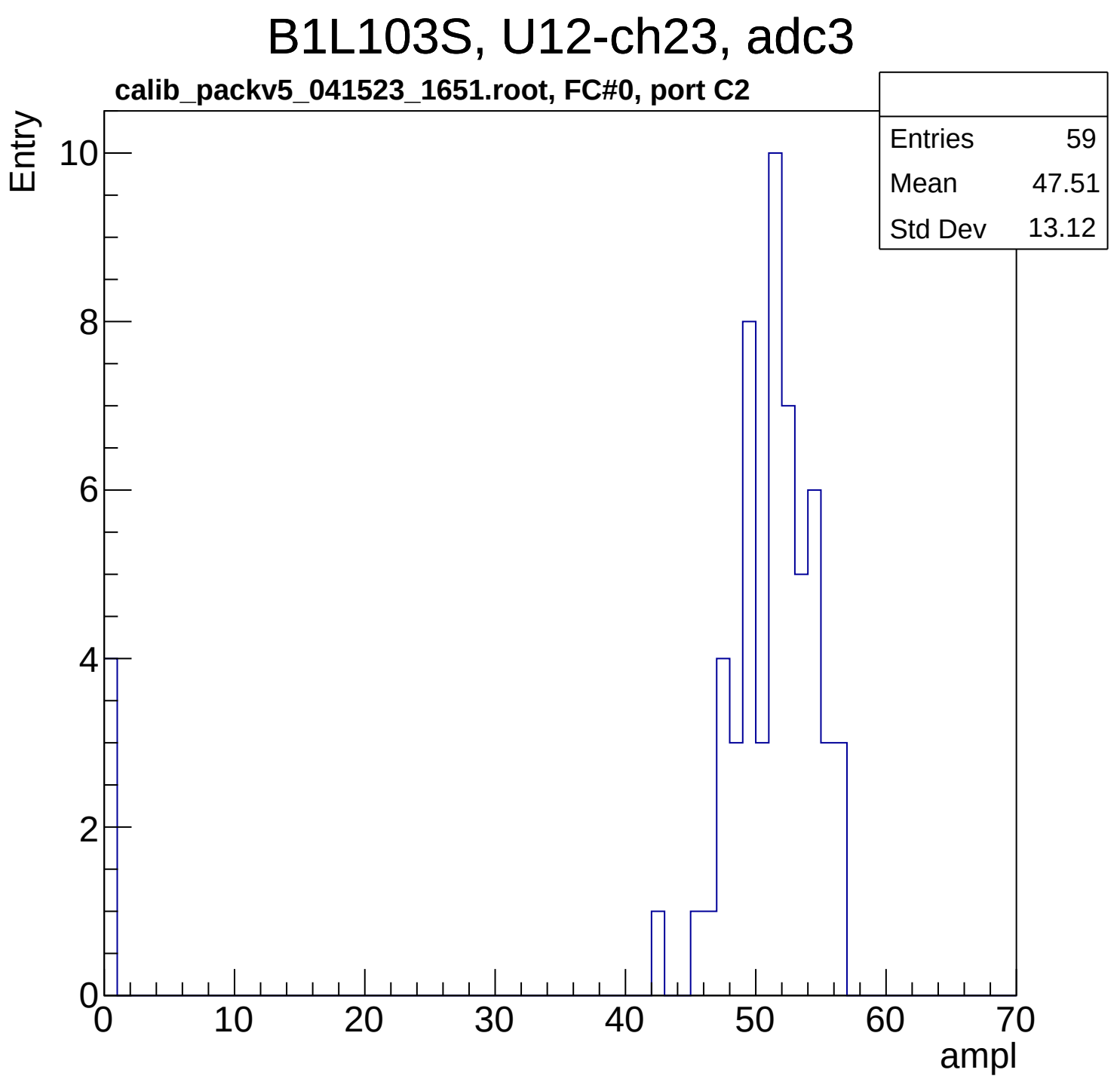
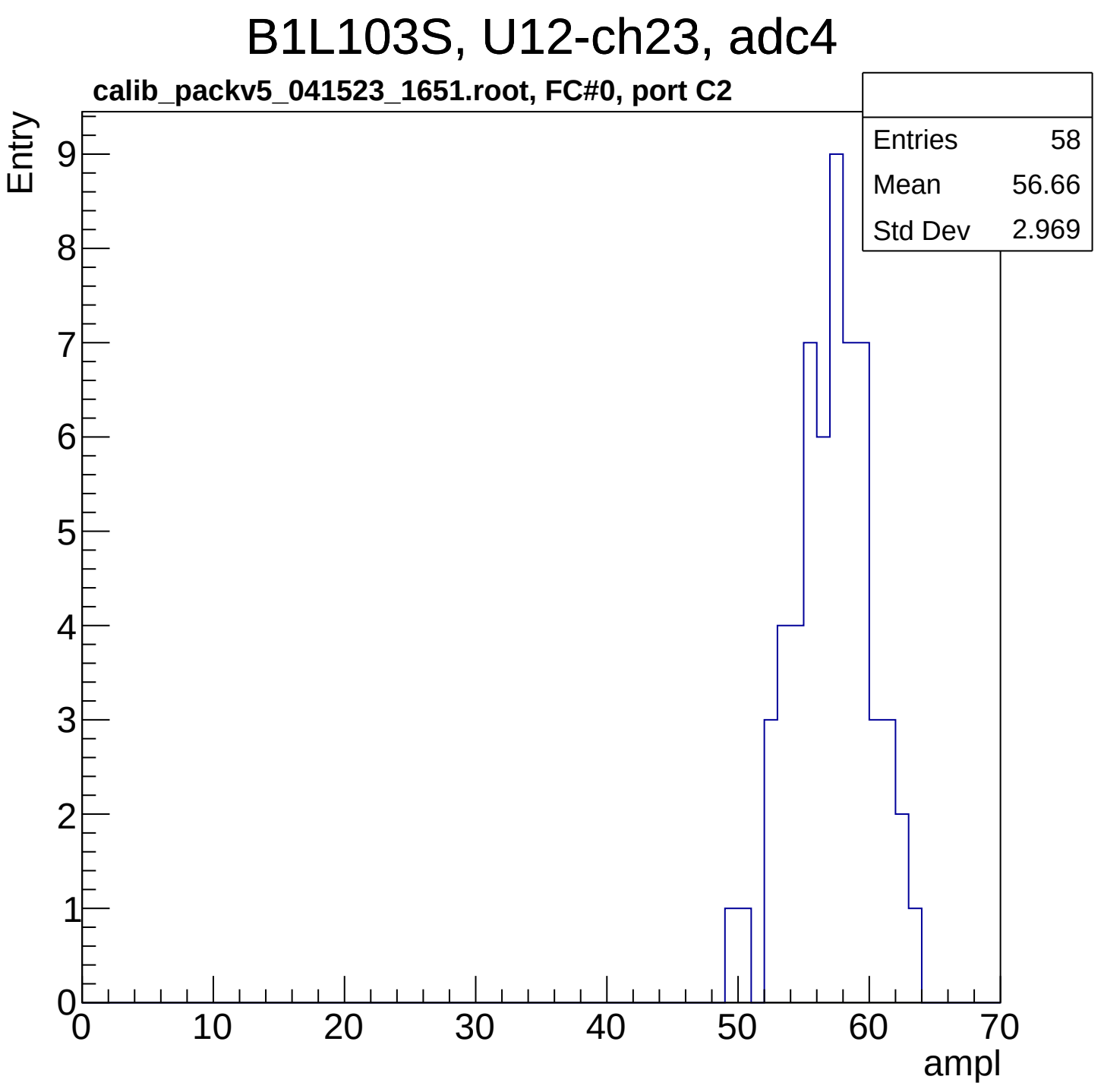
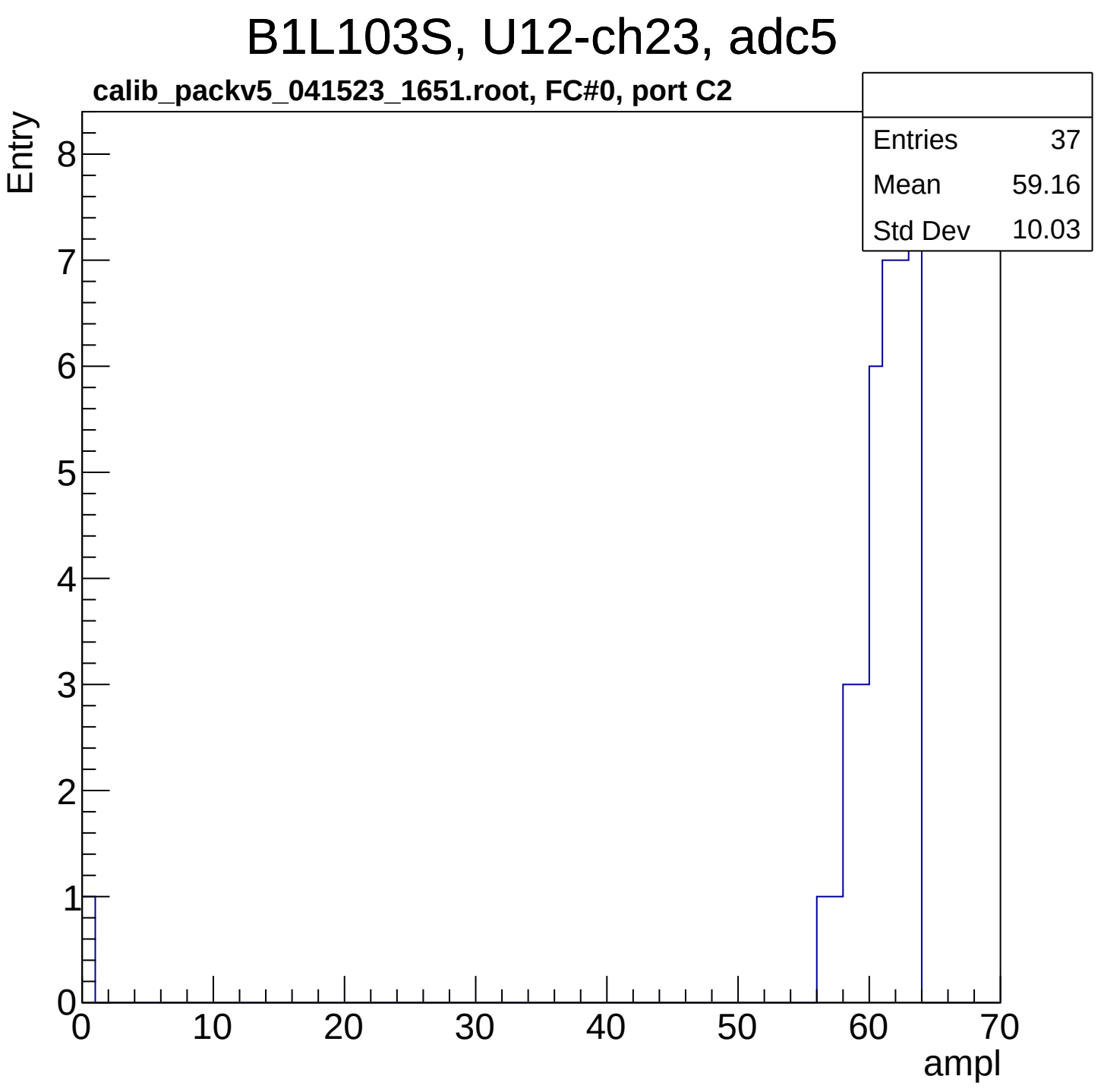
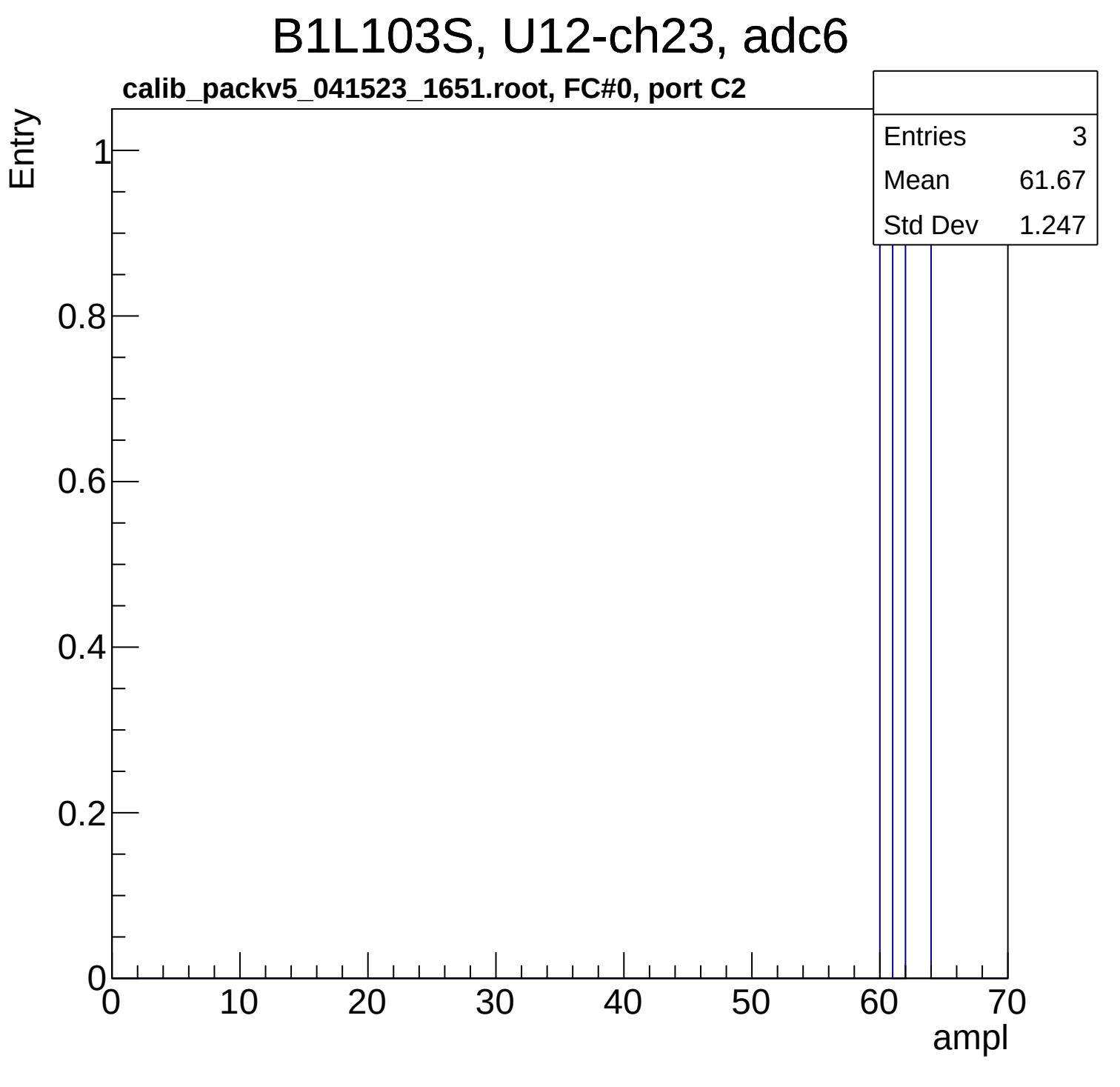

B1L103S, U12-ch23, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 37.42
Std Dev 3.523
Gaus mean : 37.8264
Gaus Width: 3.3950
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

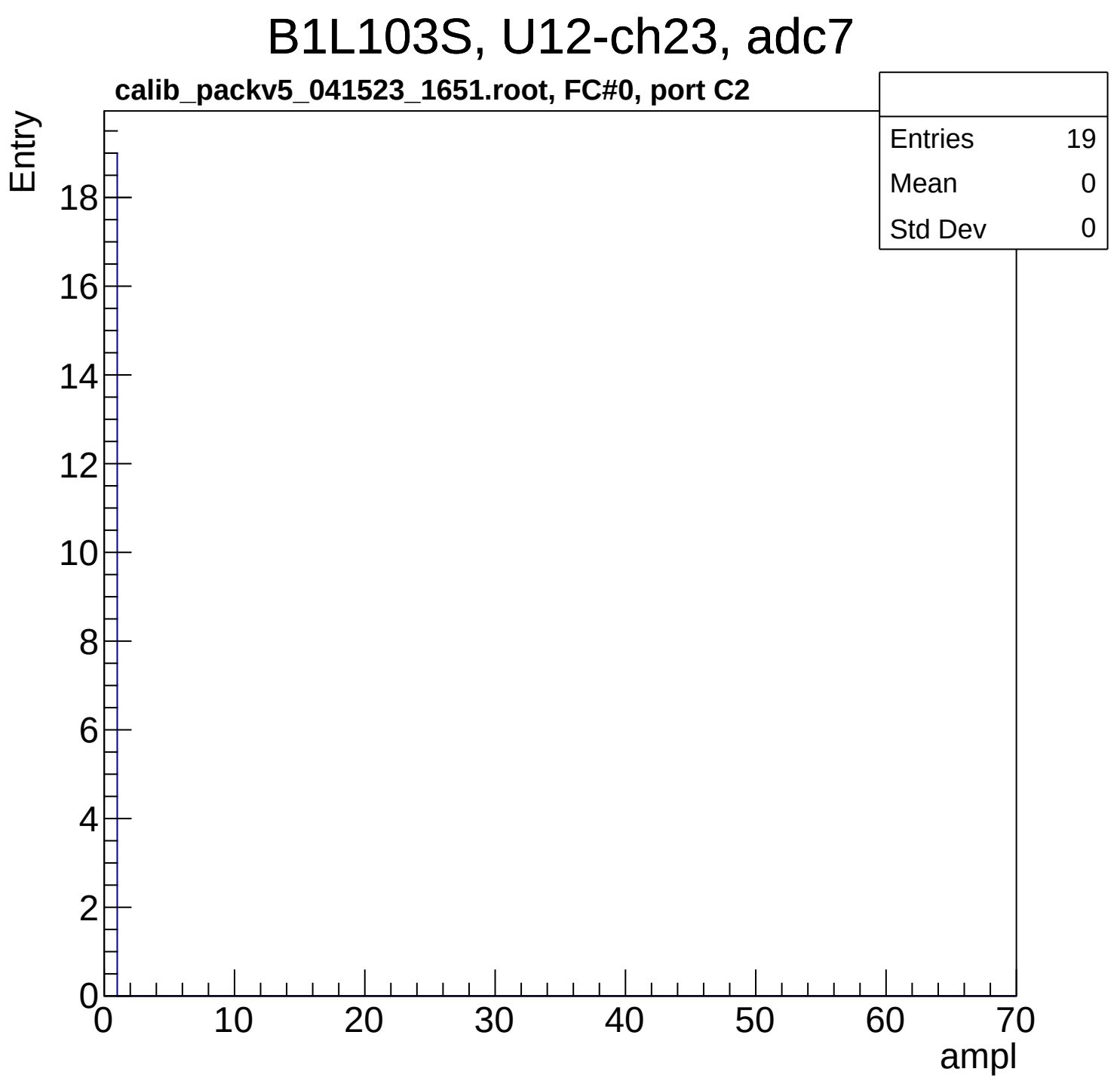

B1L103S, U12-ch23, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 40.68
Std Dev 13.39
Gaus mean : 44.8970
Gaus Width: 2.8547
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

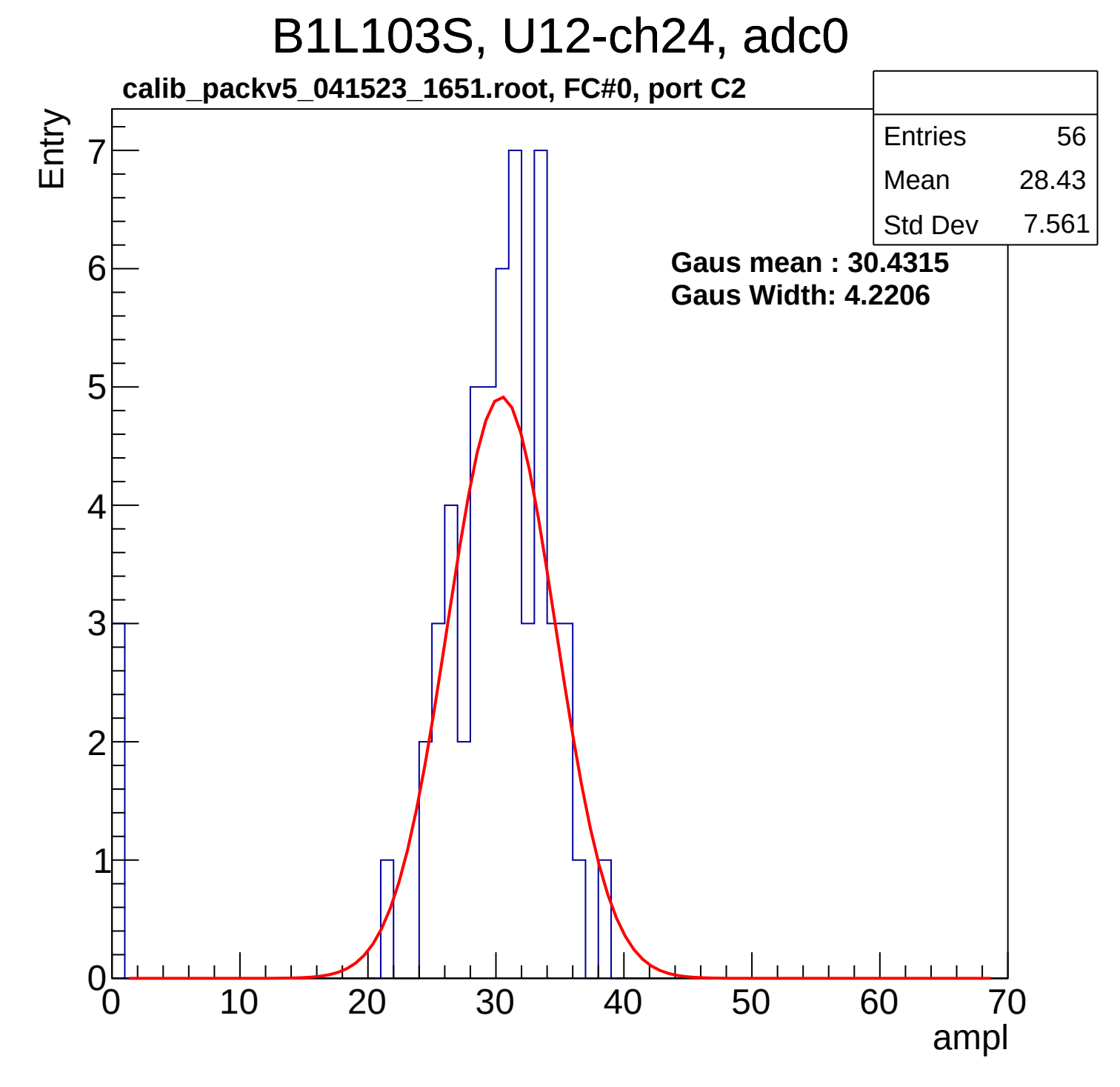

B1L103S, U12-ch23, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 47.51
Std Dev 13.12
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

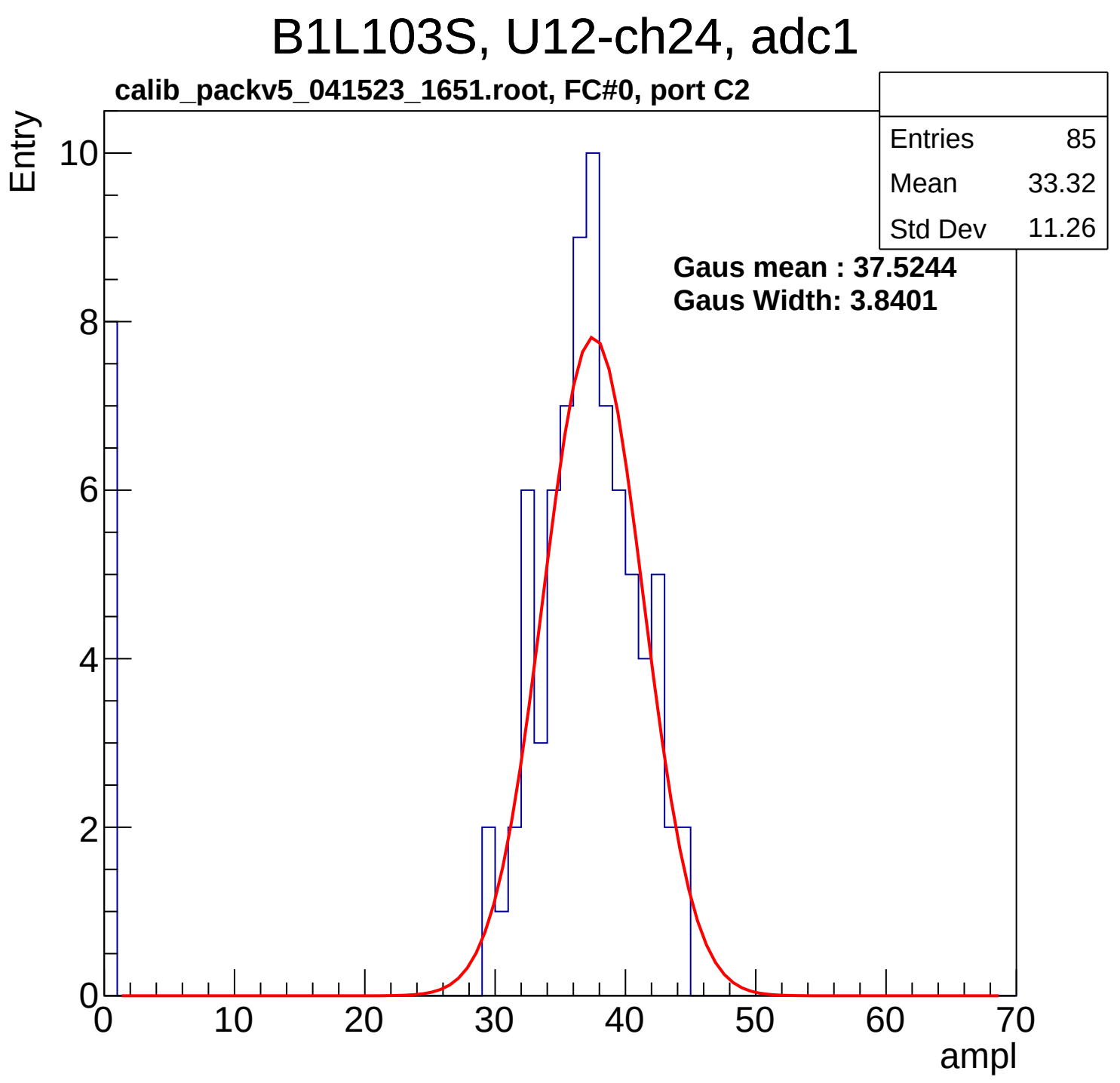

B1L103S, U12-ch23, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 56.66
Std Dev 2.969
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

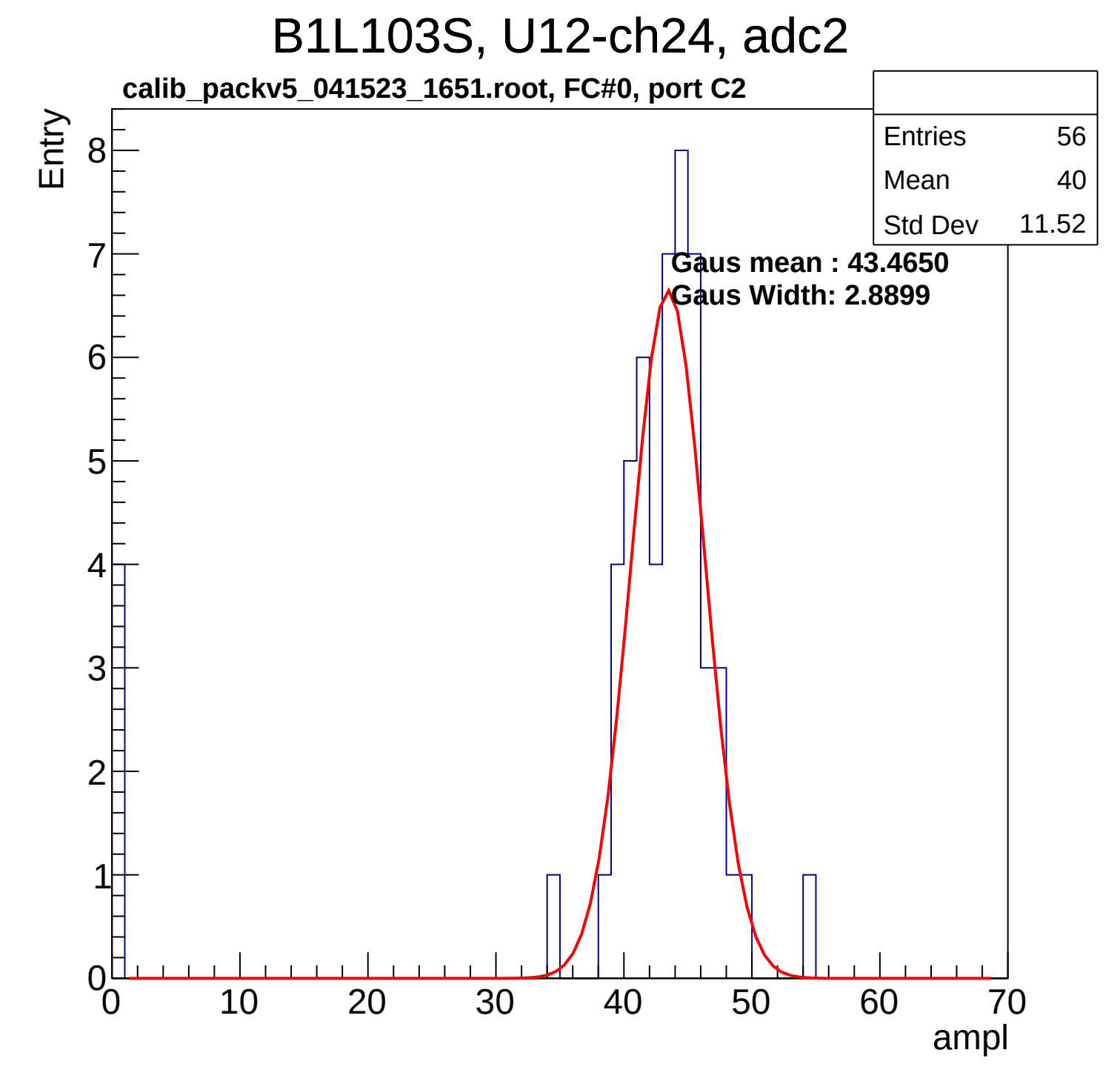

B1L103S, U12-ch23, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 37
Mean 59.16
Std Dev 10.03
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

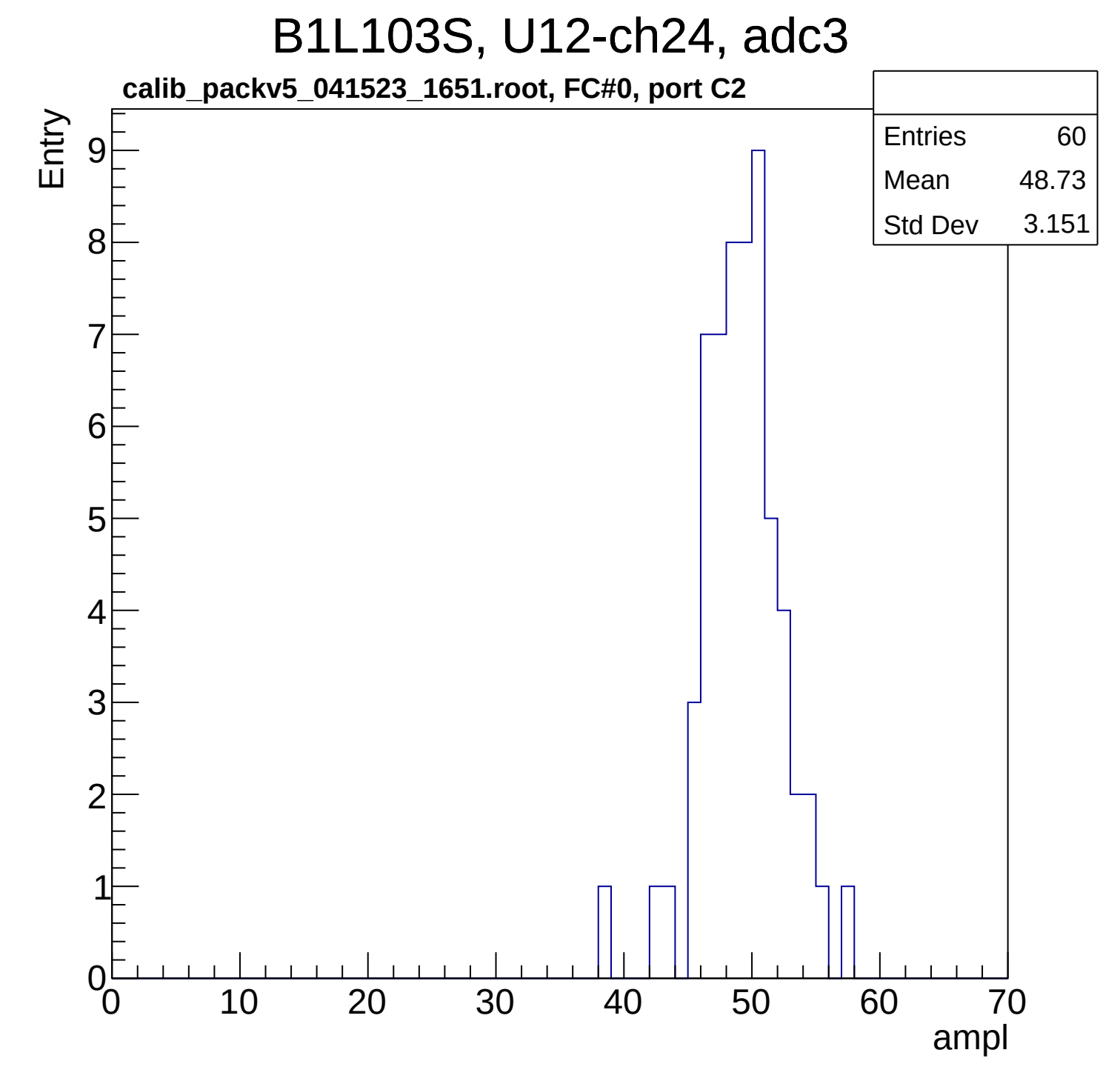

B1L103S, U12-ch23, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 61.67
Std Dev 1.247
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

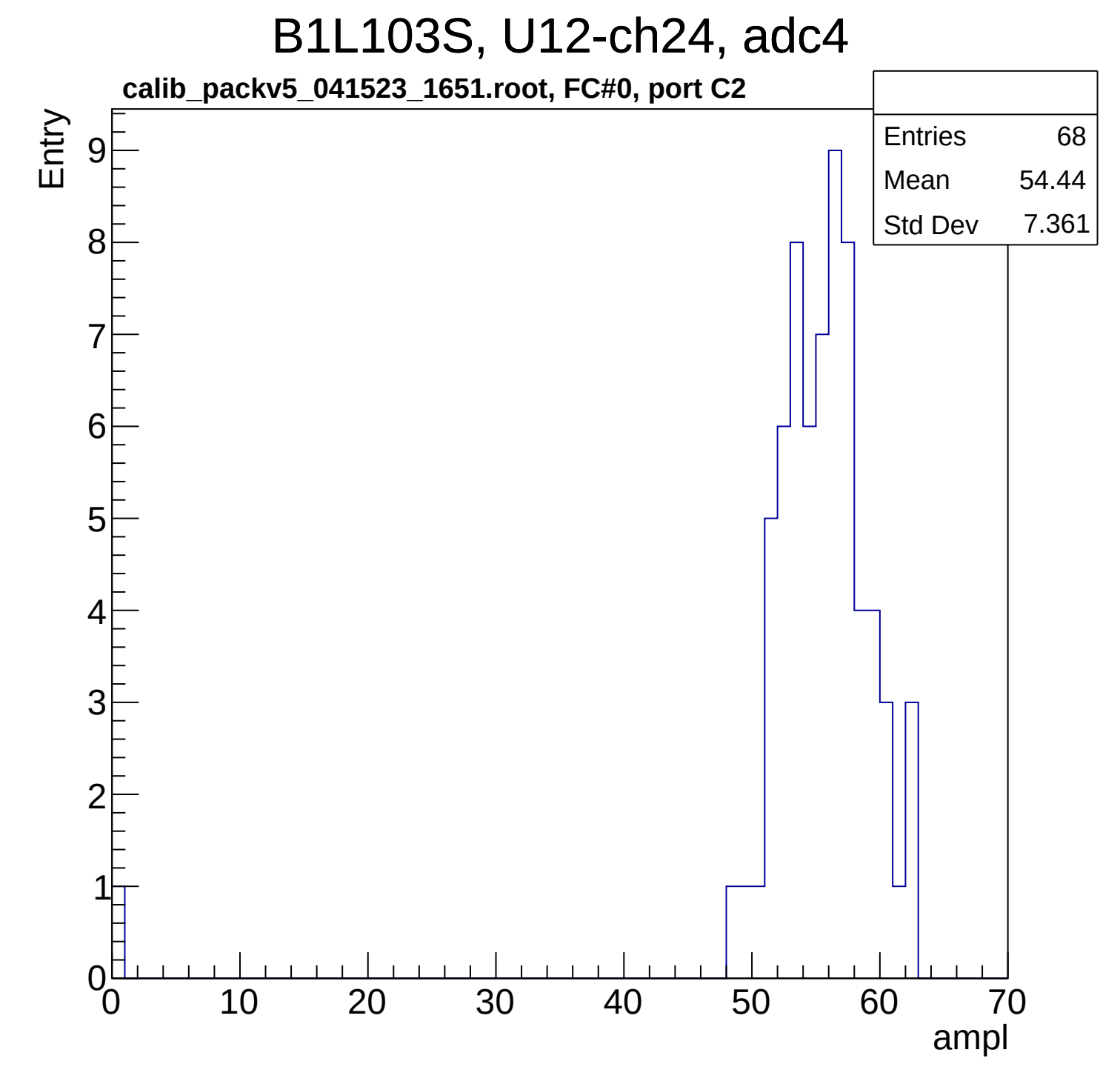

B1L103S, U12-ch23, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch24, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 28.43
Std Dev 7.561
Gaus mean : 30.4315
Gaus Width: 4.2206
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U12-ch24, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 33.32
Std Dev 11.26
Gaus mean : 37.5244
Gaus Width: 3.8401
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch24, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 40
Std Dev 11.52
Gaus mean : 43.4650
Gaus Width: 2.8899
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U12-ch24, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 48.73
Std Dev 3.151
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch24, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 54.44
Std Dev 7.361
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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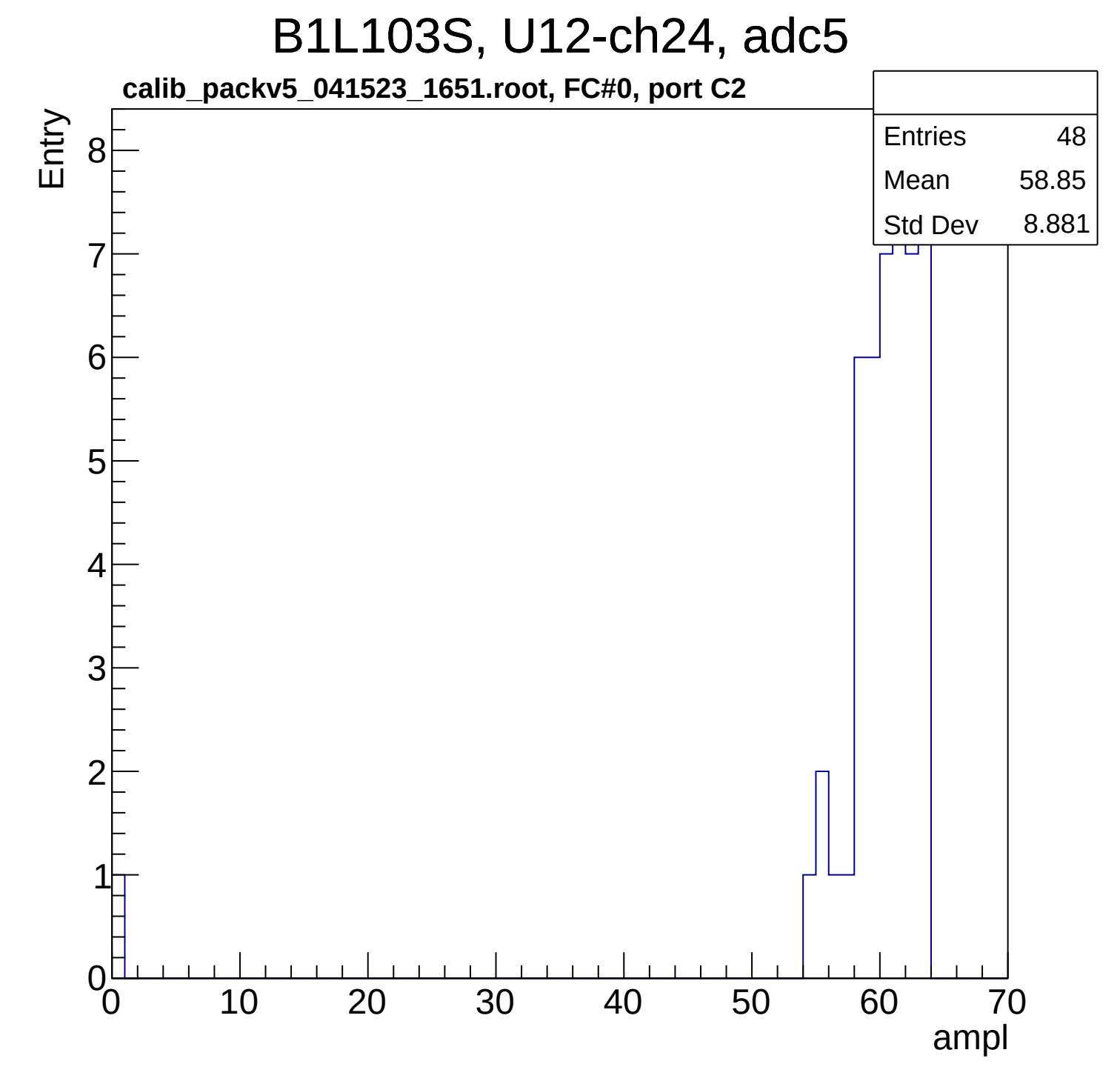
B1L103S, U12-ch24, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.85
Std Dev 8.881
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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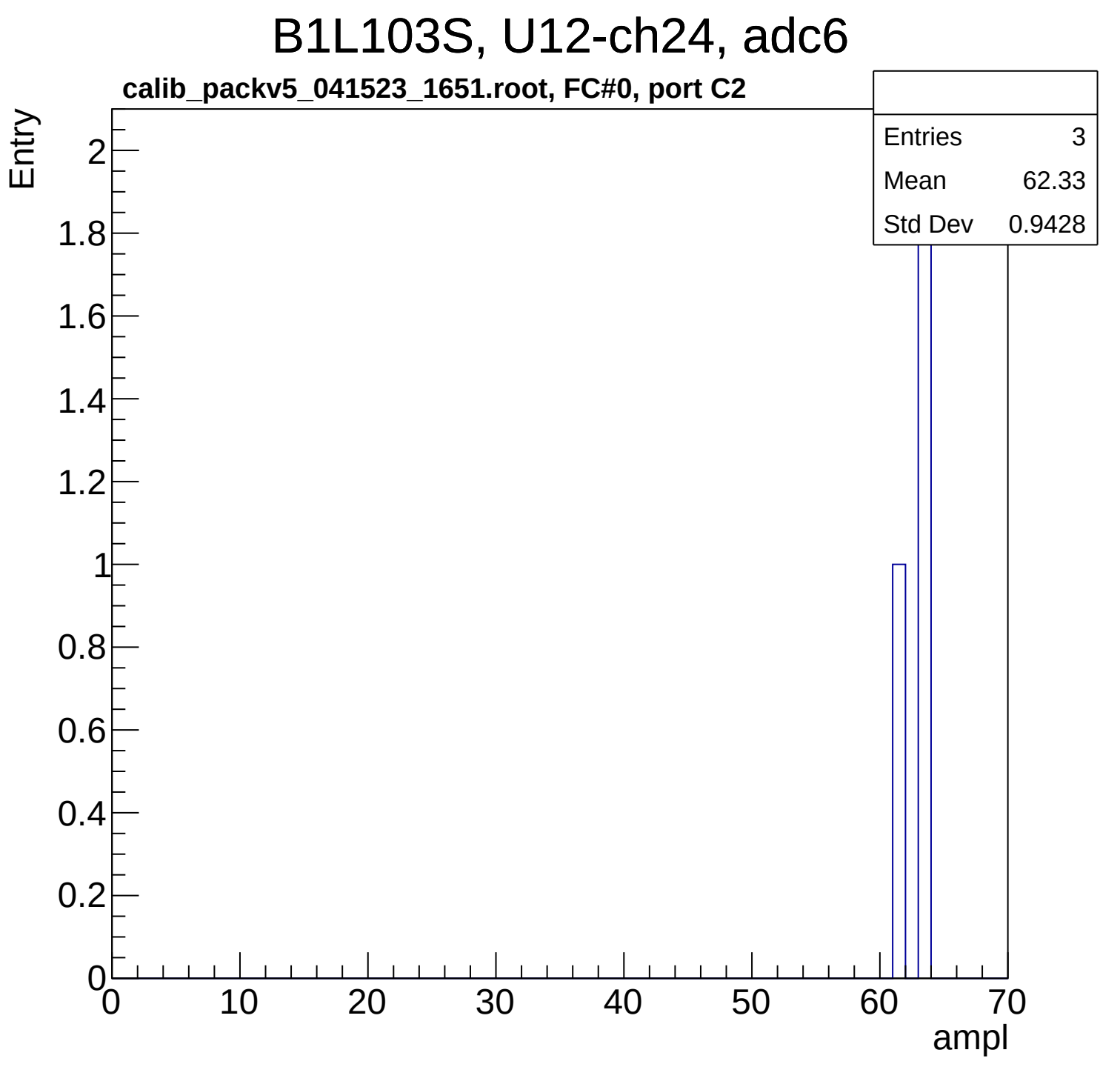
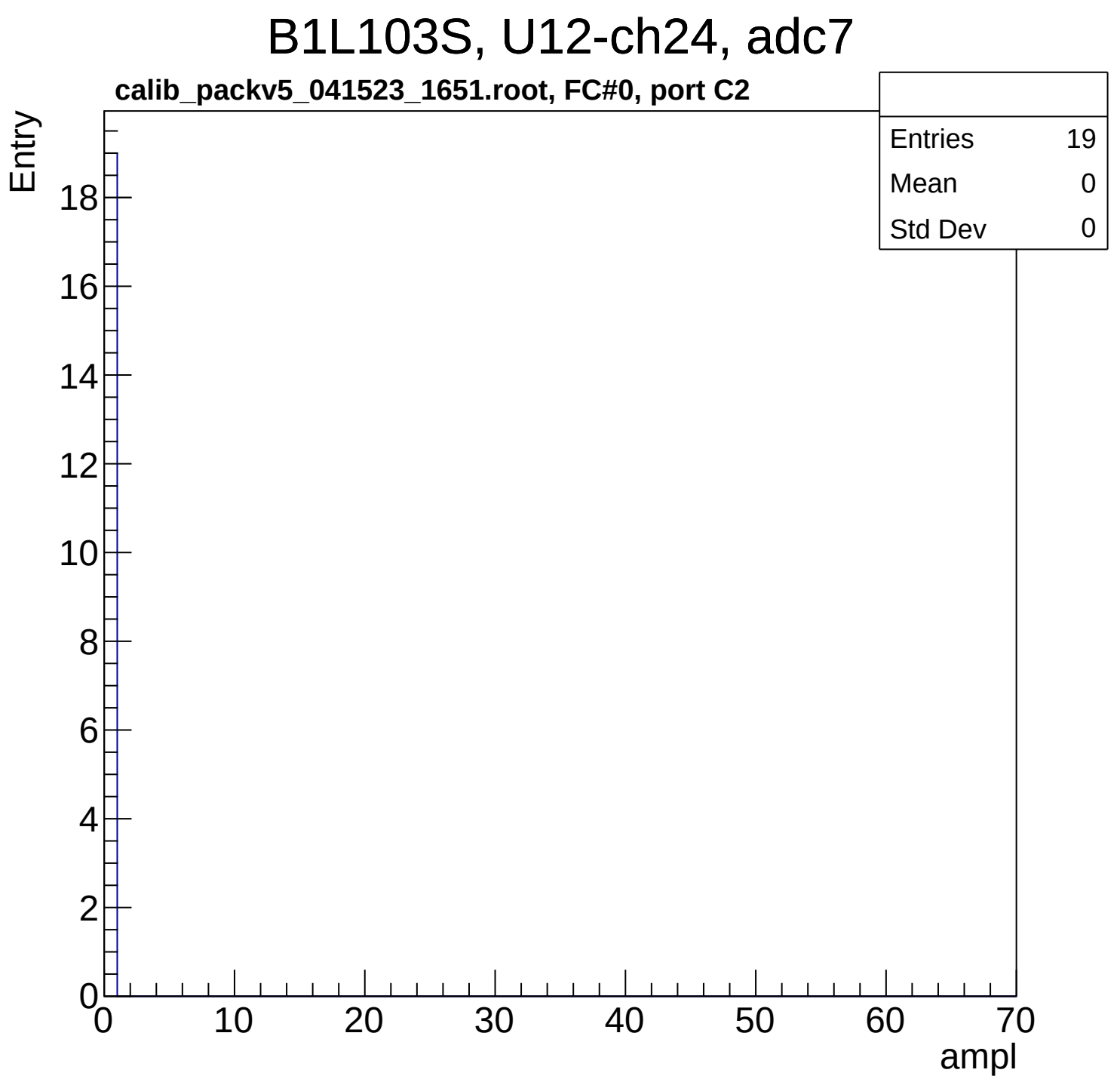
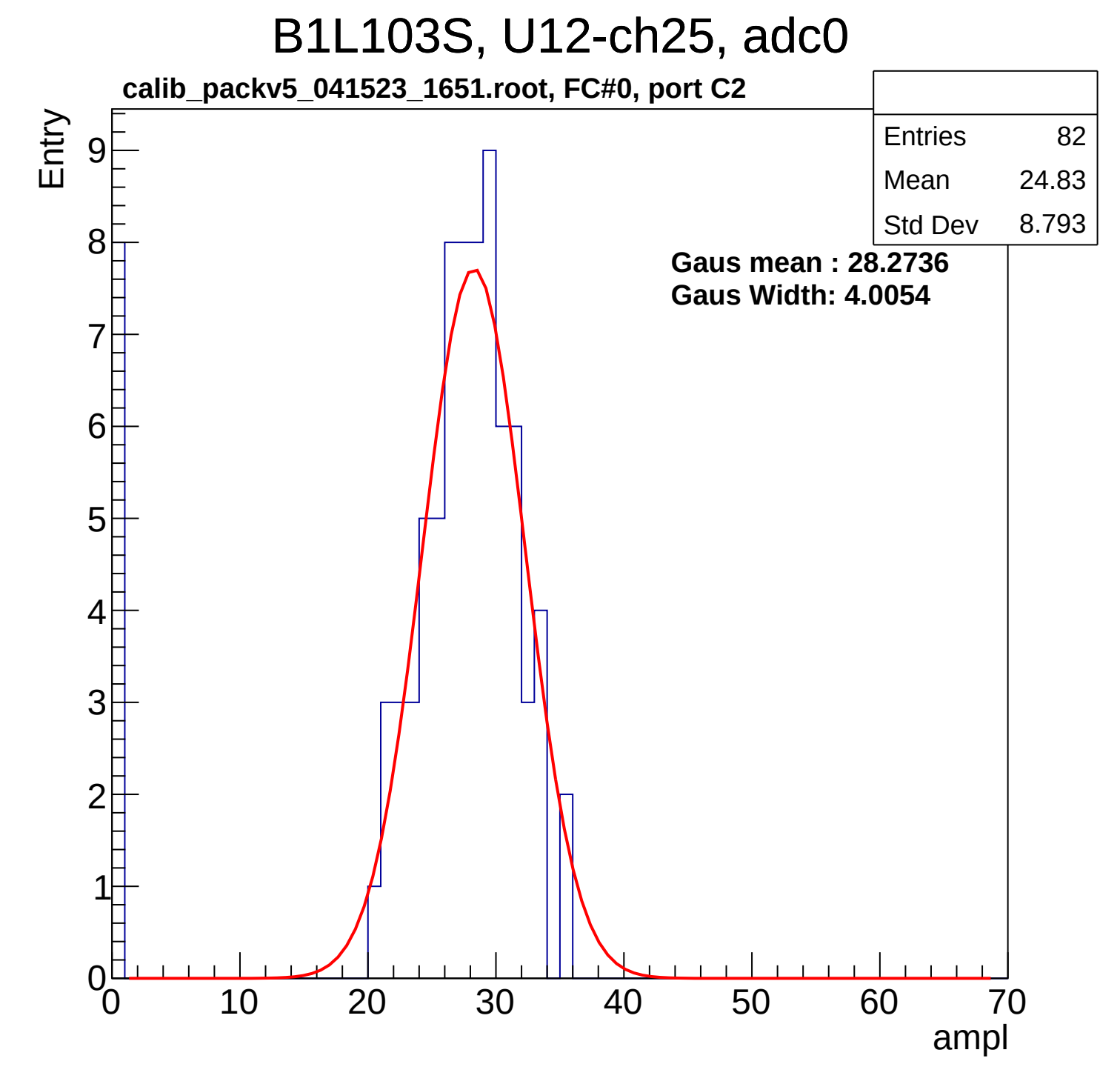

B1L103S, U12-ch24, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.33
Std Dev 0.9428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U12-ch24, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch25, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 24.83
Std Dev 8.793
Gaus mean : 28.2736
Gaus Width: 4.0054
Entry
ampl
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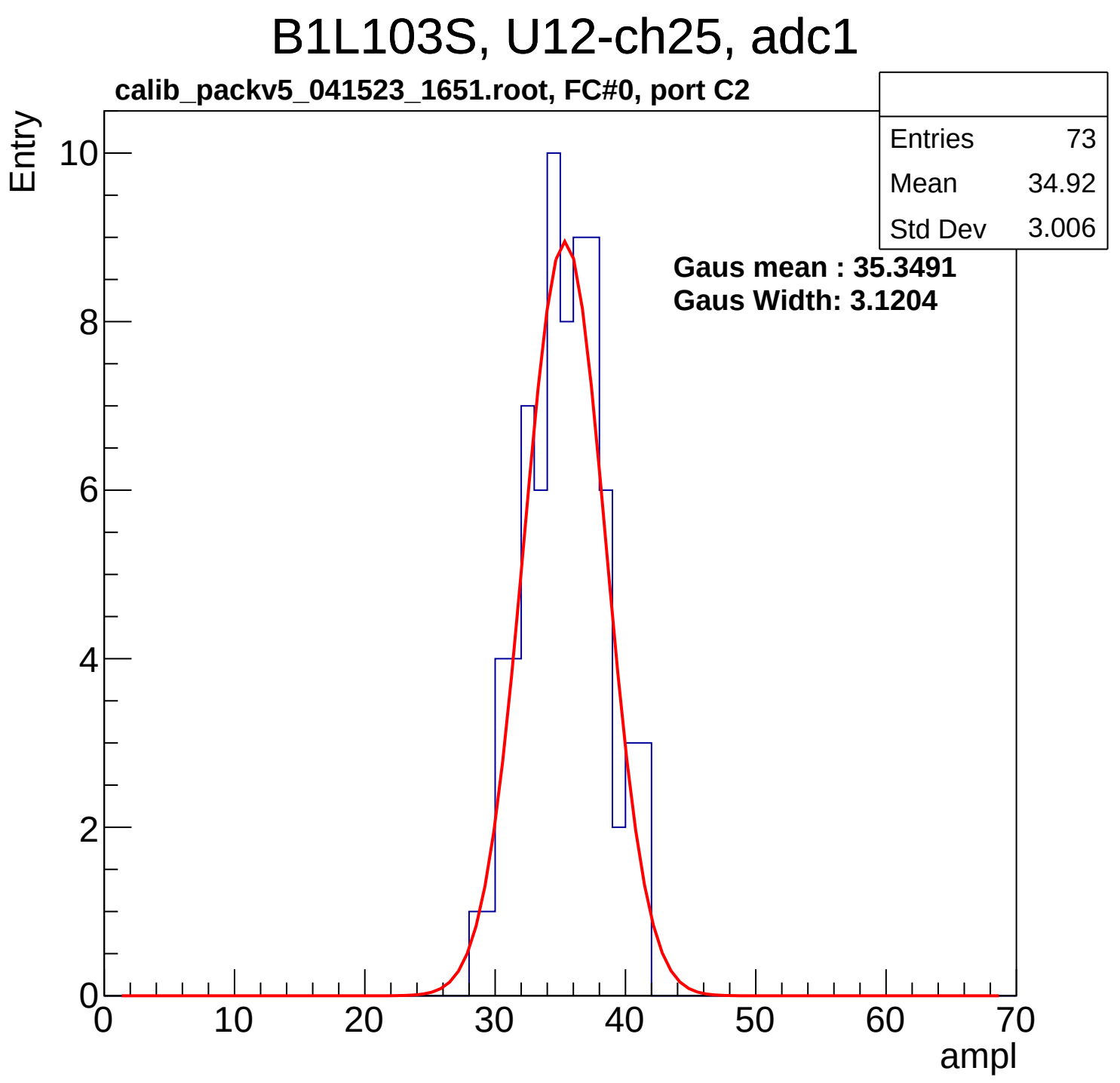
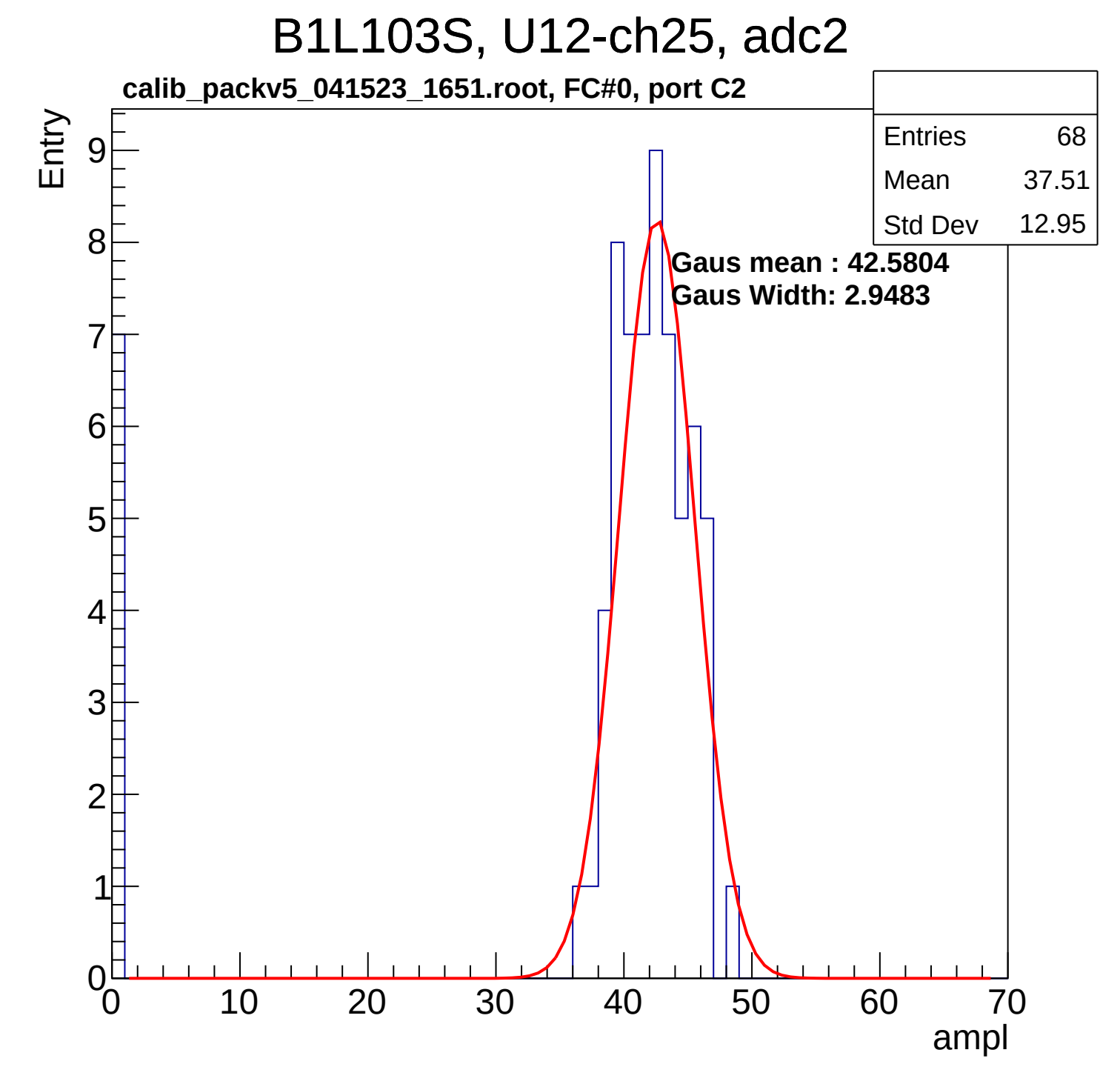
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch25, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 34.92
Std Dev 3.006
Gaus mean : 35.3491
Gaus Width: 3.1204
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch25, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 37.51
Std Dev 12.95
Gaus mean : 42.5804
Gaus Width: 2.9483
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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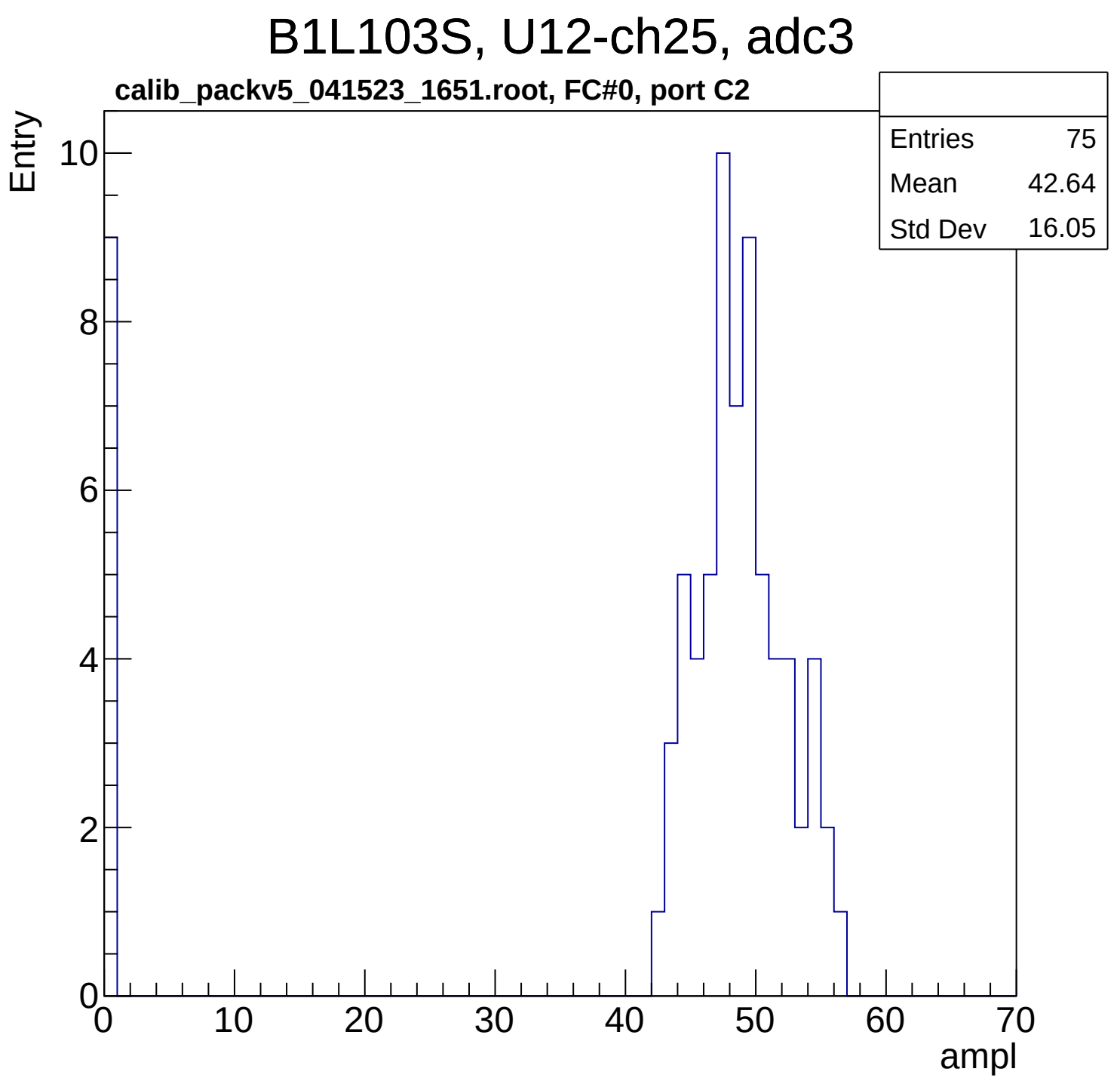
B1L103S, U12-ch25, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 42.64
Std Dev 16.05
Entry
ampl
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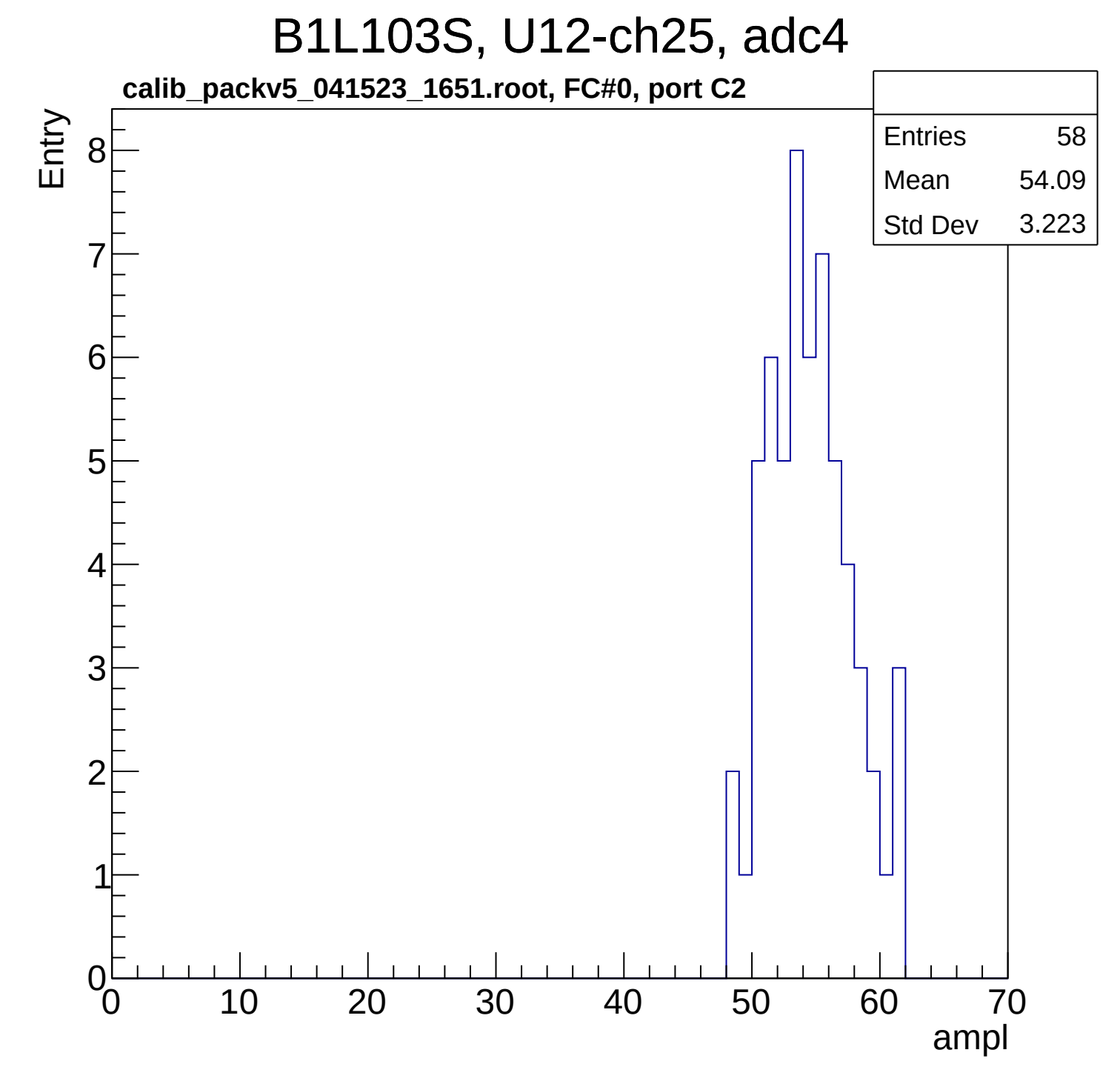
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch25, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 54.09
Std Dev 3.223
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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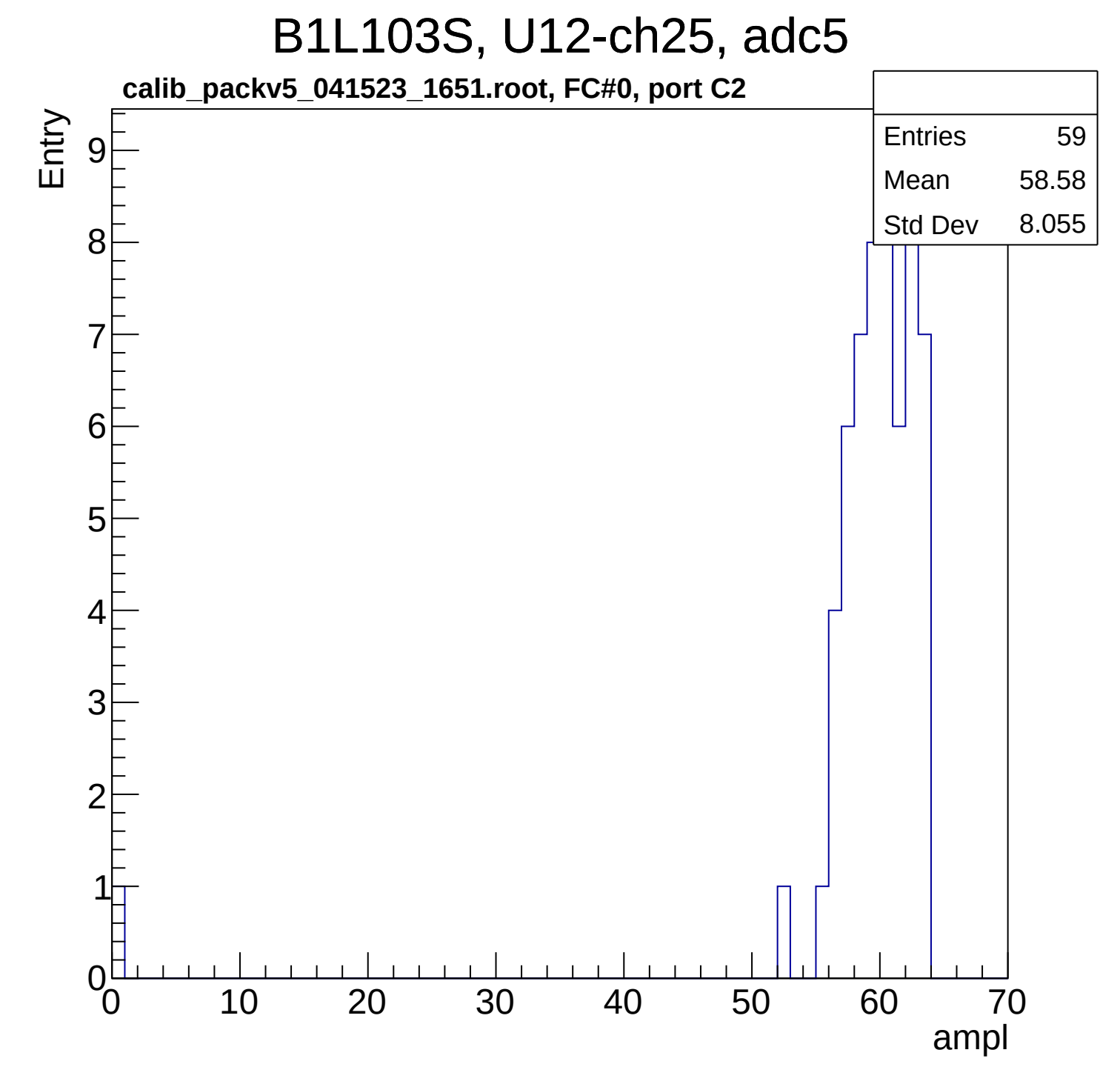
B1L103S, U12-ch25, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 58.58
Std Dev 8.055
Entry
ampl
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1
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5
6
7
8
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0
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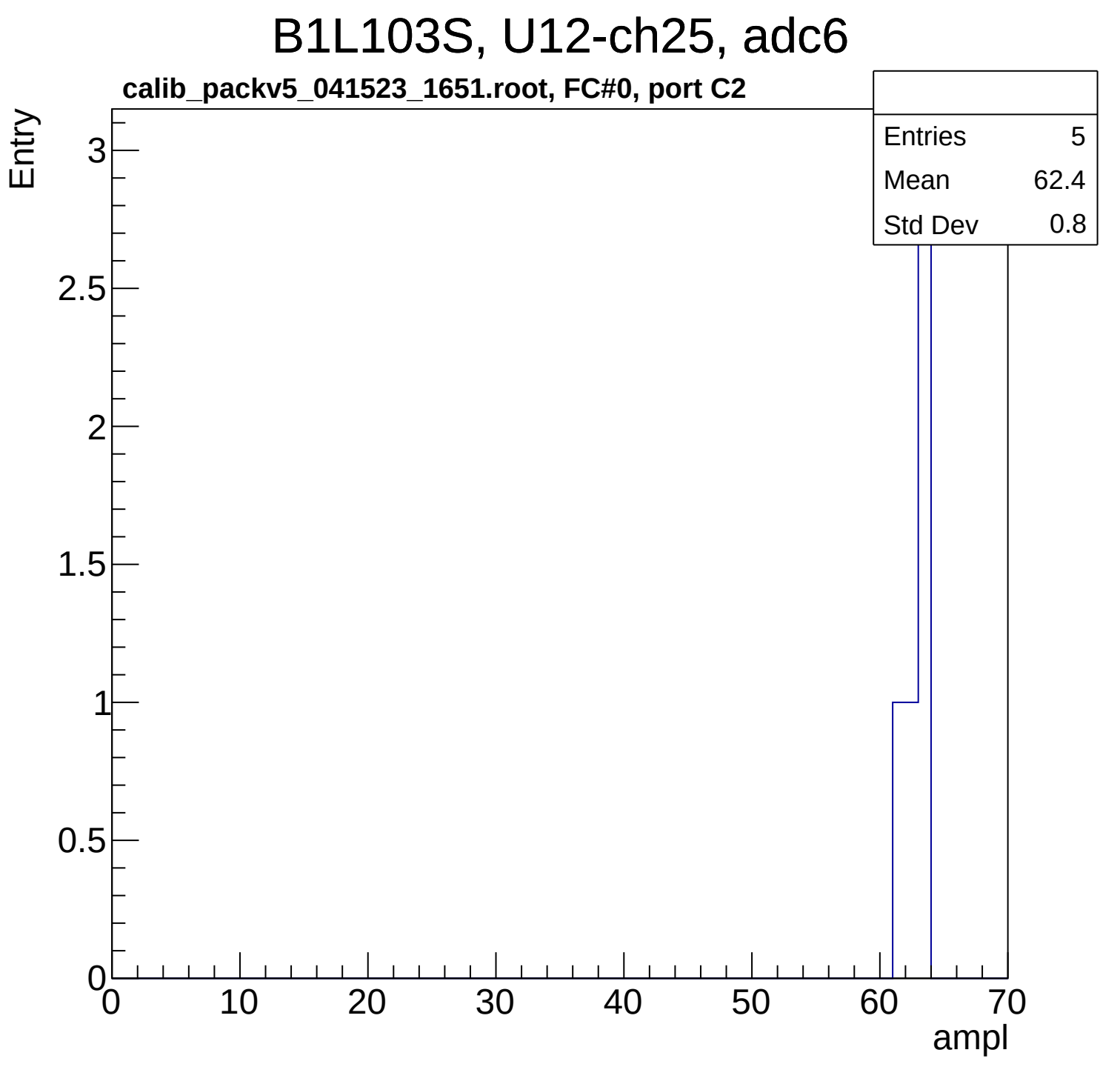
B1L103S, U12-ch25, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.4
Std Dev 0.8
Entry
ampl
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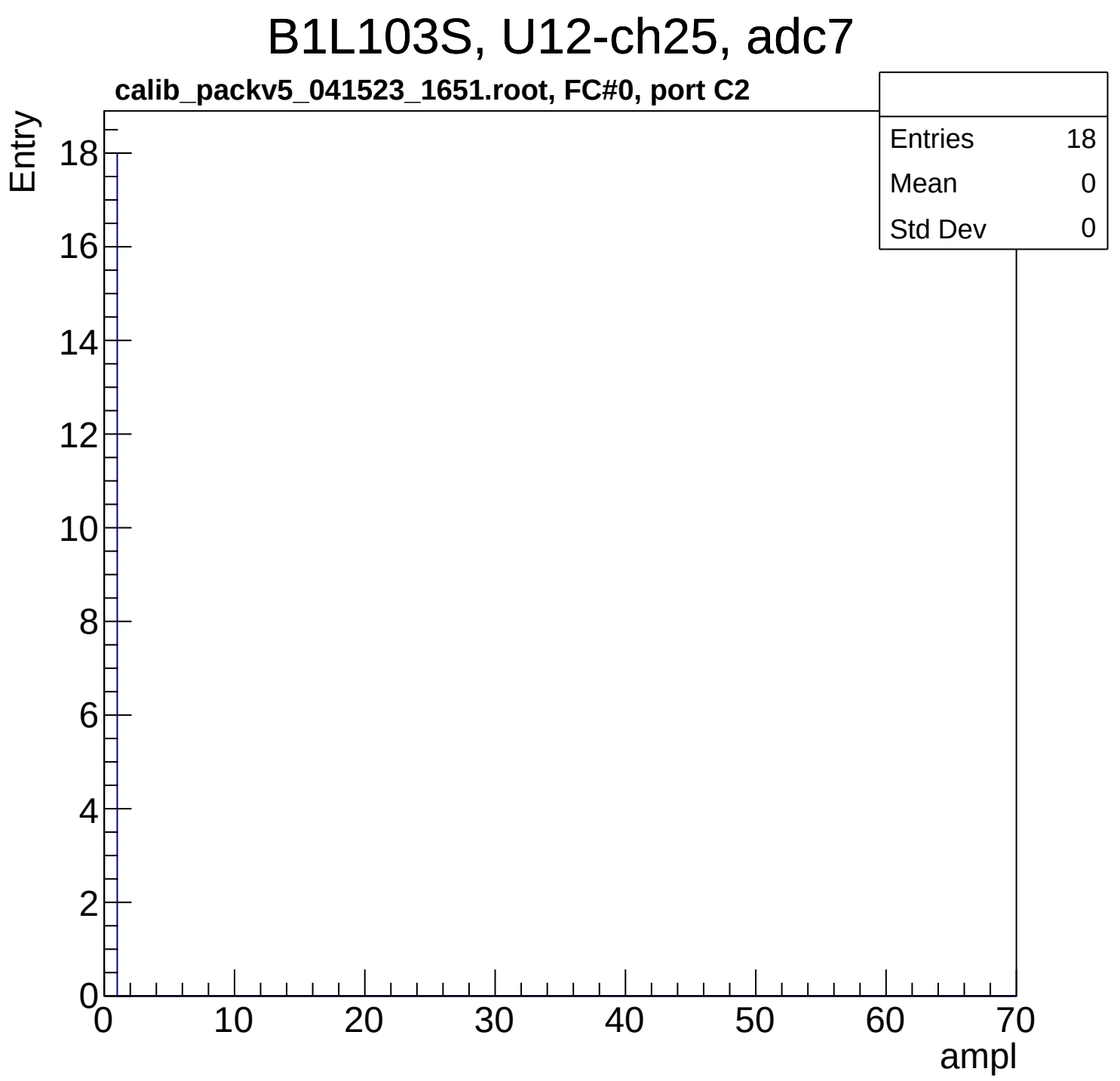
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U12-ch25, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
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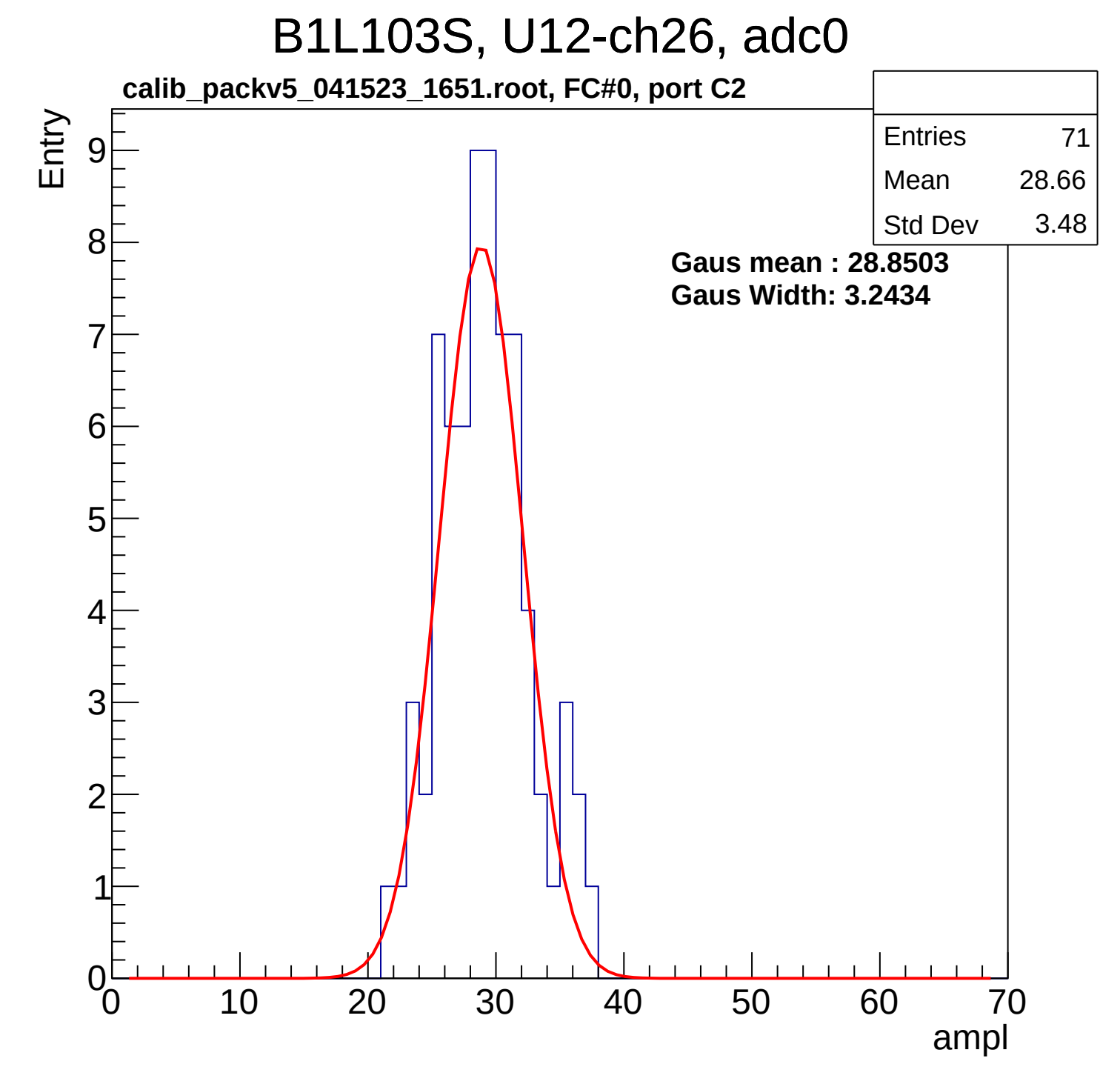
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch26, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 28.66
Std Dev 3.48
Gaus mean : 28.8503
Gaus Width: 3.2434
Entry
ampl
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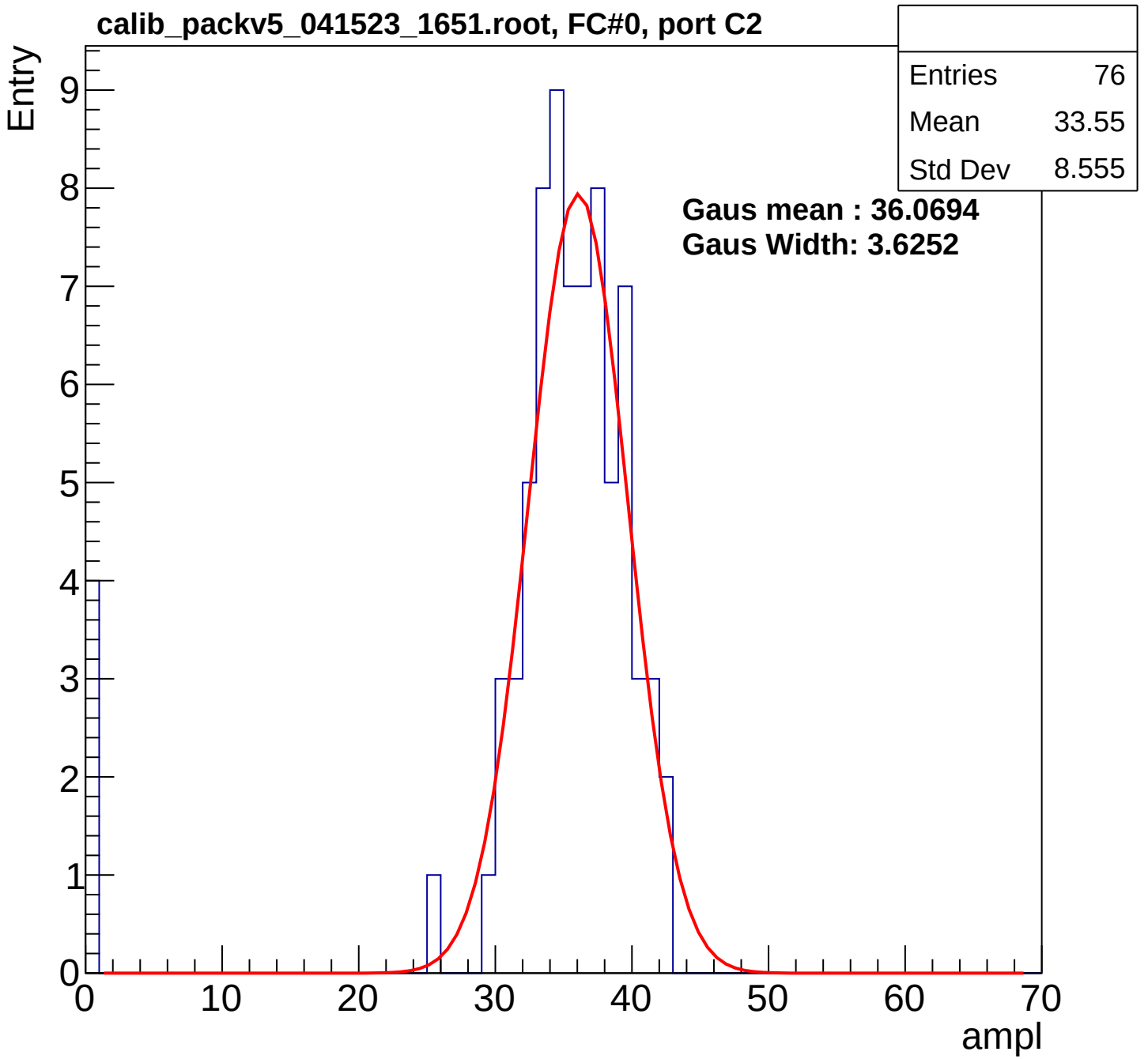
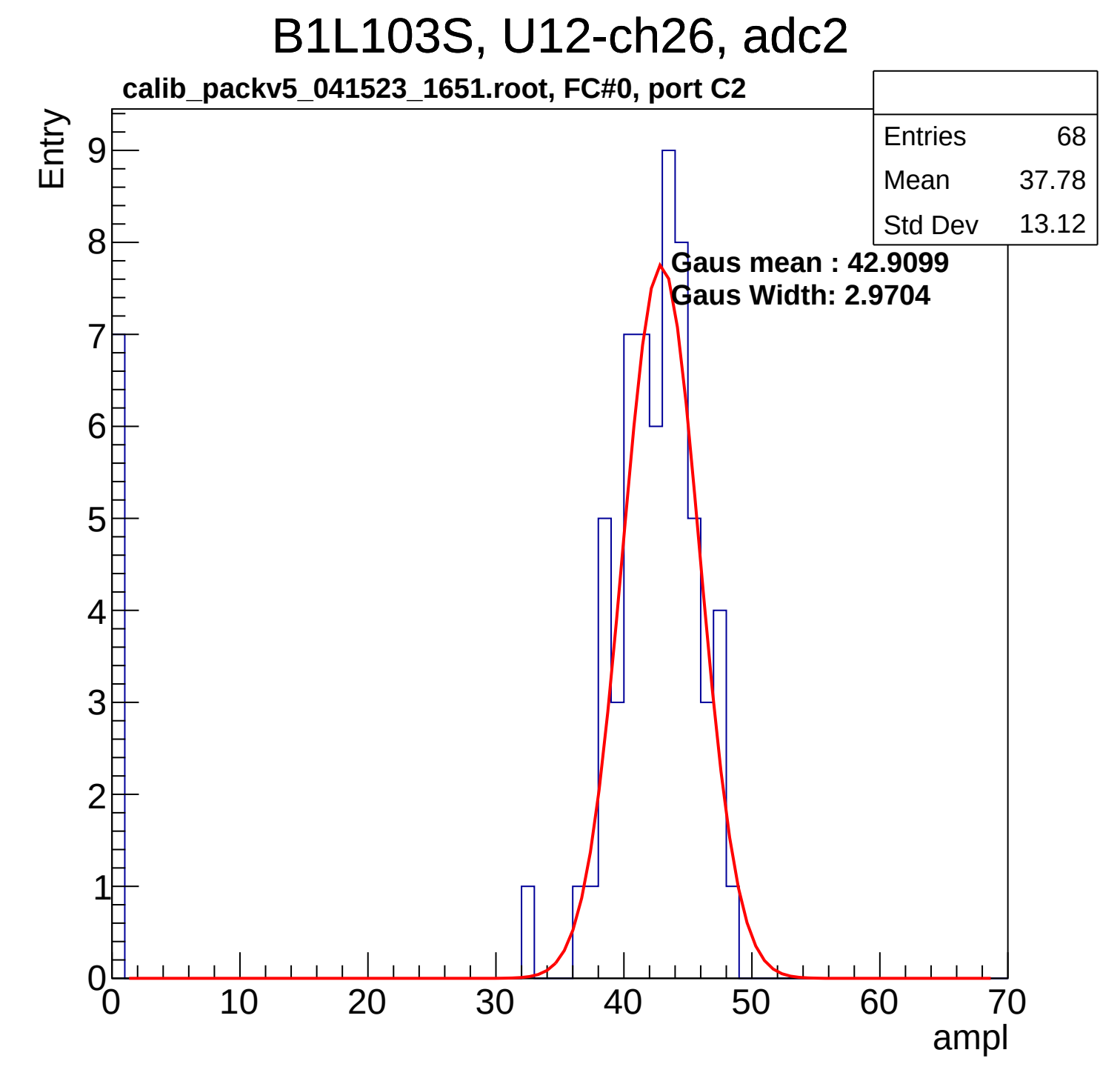
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch26, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 33.55
Std Dev 8.555
Gaus mean : 36.0694
Gaus Width: 3.6252
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch26, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 37.78
Std Dev 13.12
Gaus mean : 42.9099
Gaus Width: 2.9704
Entry
ampl
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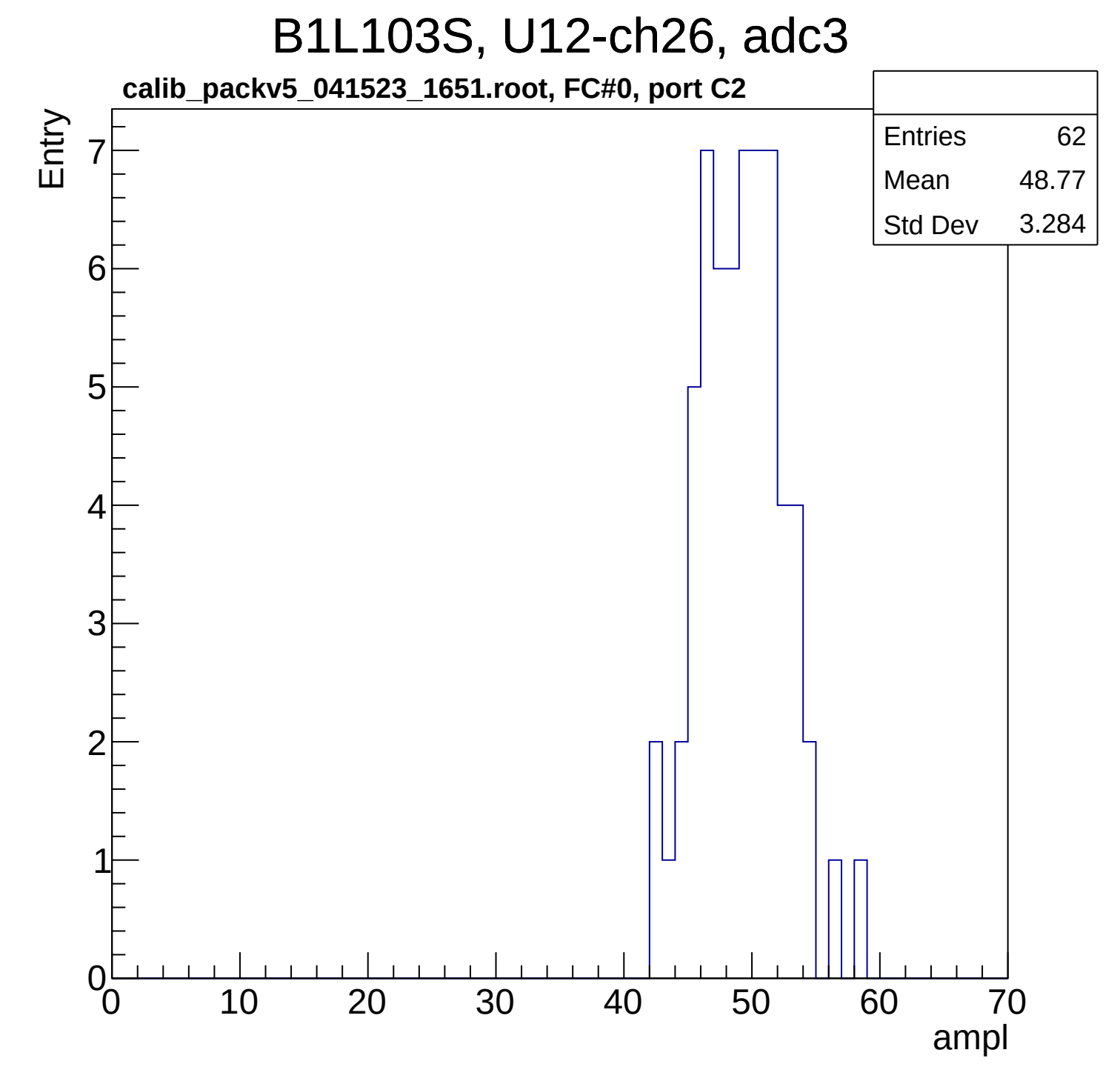
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U12-ch26, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 48.77
Std Dev 3.284
Entry
ampl
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1
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6
7
0
10
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60
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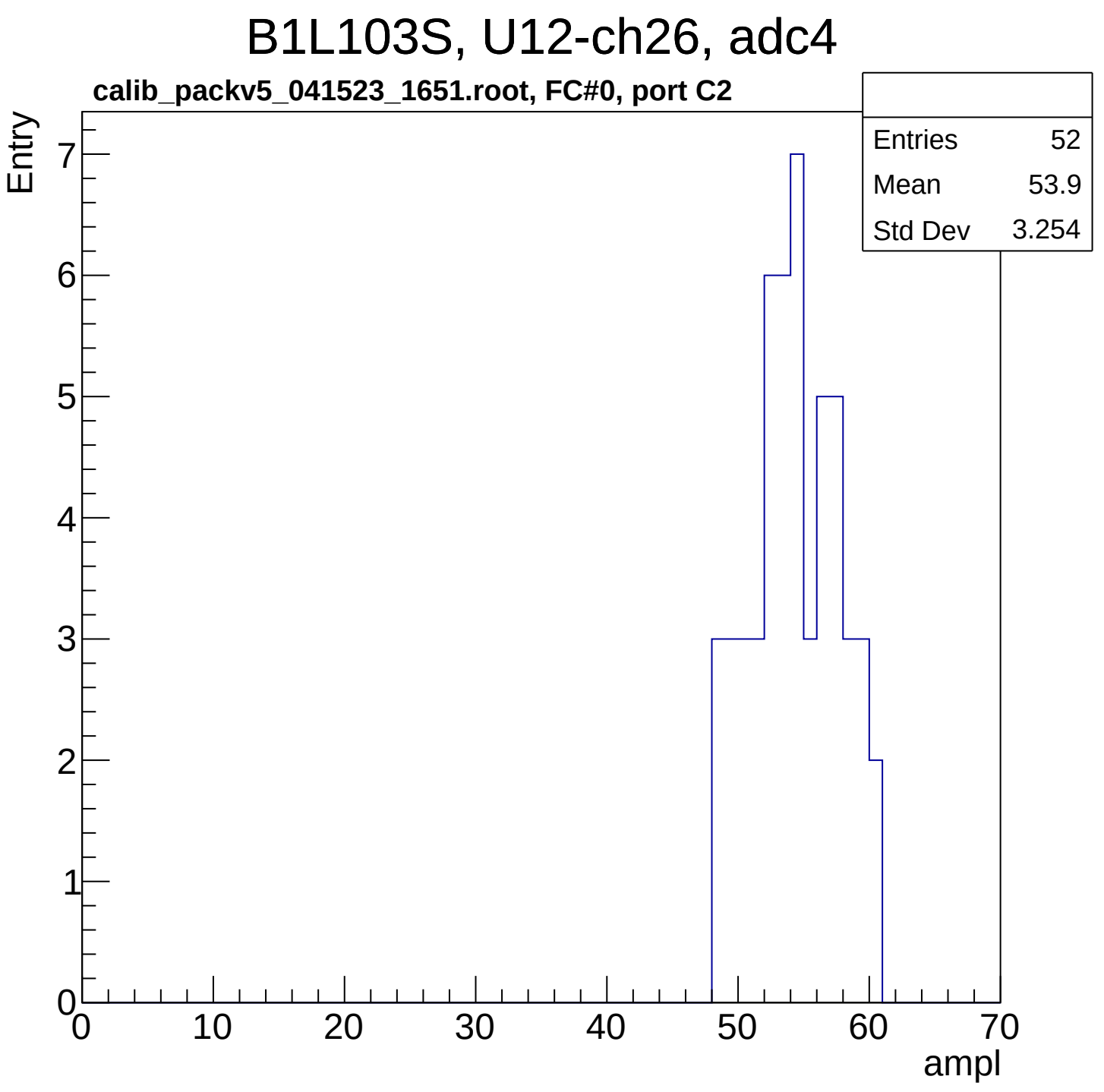
B1L103S, U12-ch26, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 53.9
Std Dev 3.254
Entry
ampl
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1
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3
4
5
6
7
0
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20
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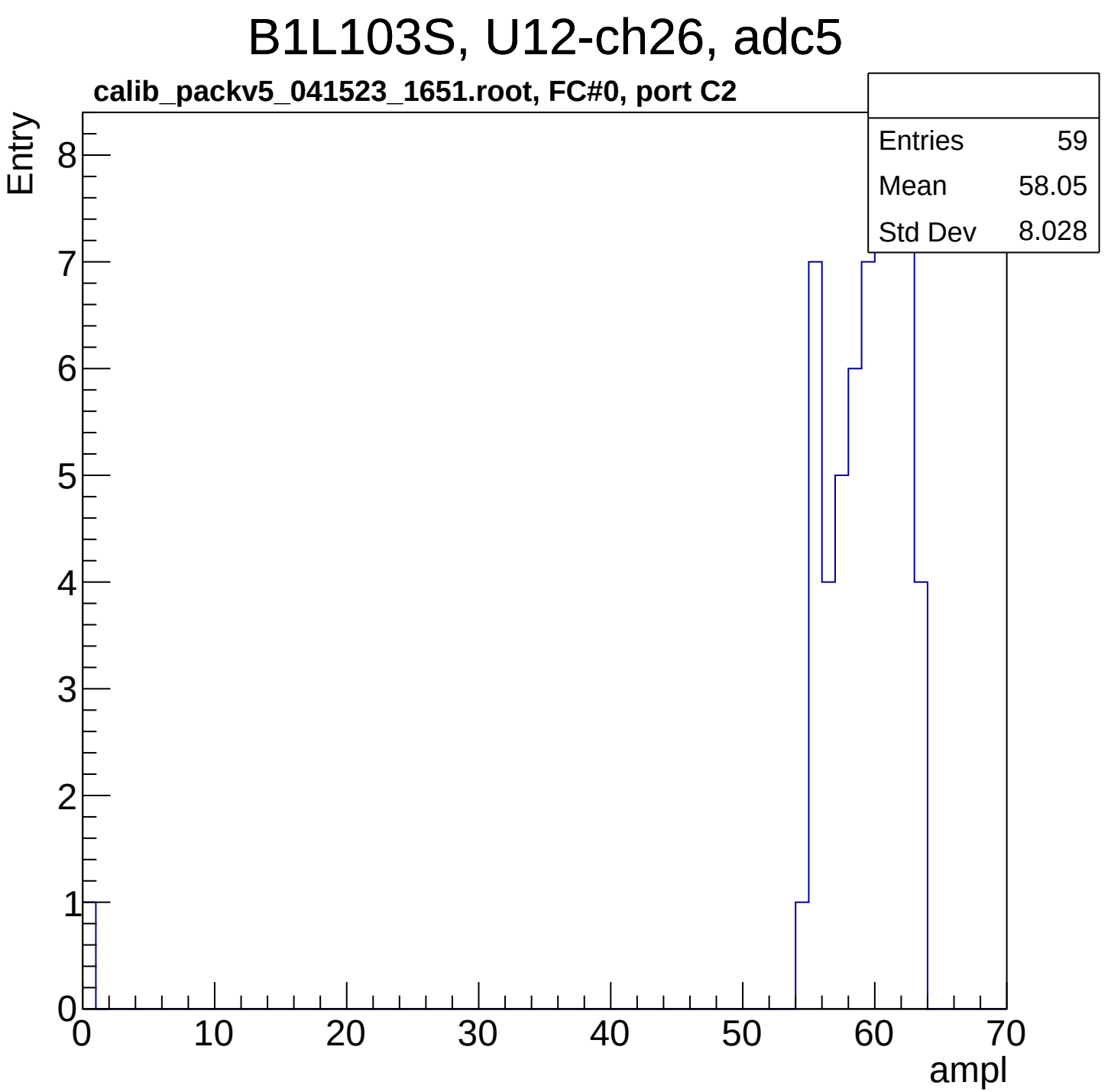
40
50
60
70


B1L103S, U12-ch26, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 58.05
Std Dev 8.028
Entry
ampl
0
1
2
3
4
5
6
7
8
0
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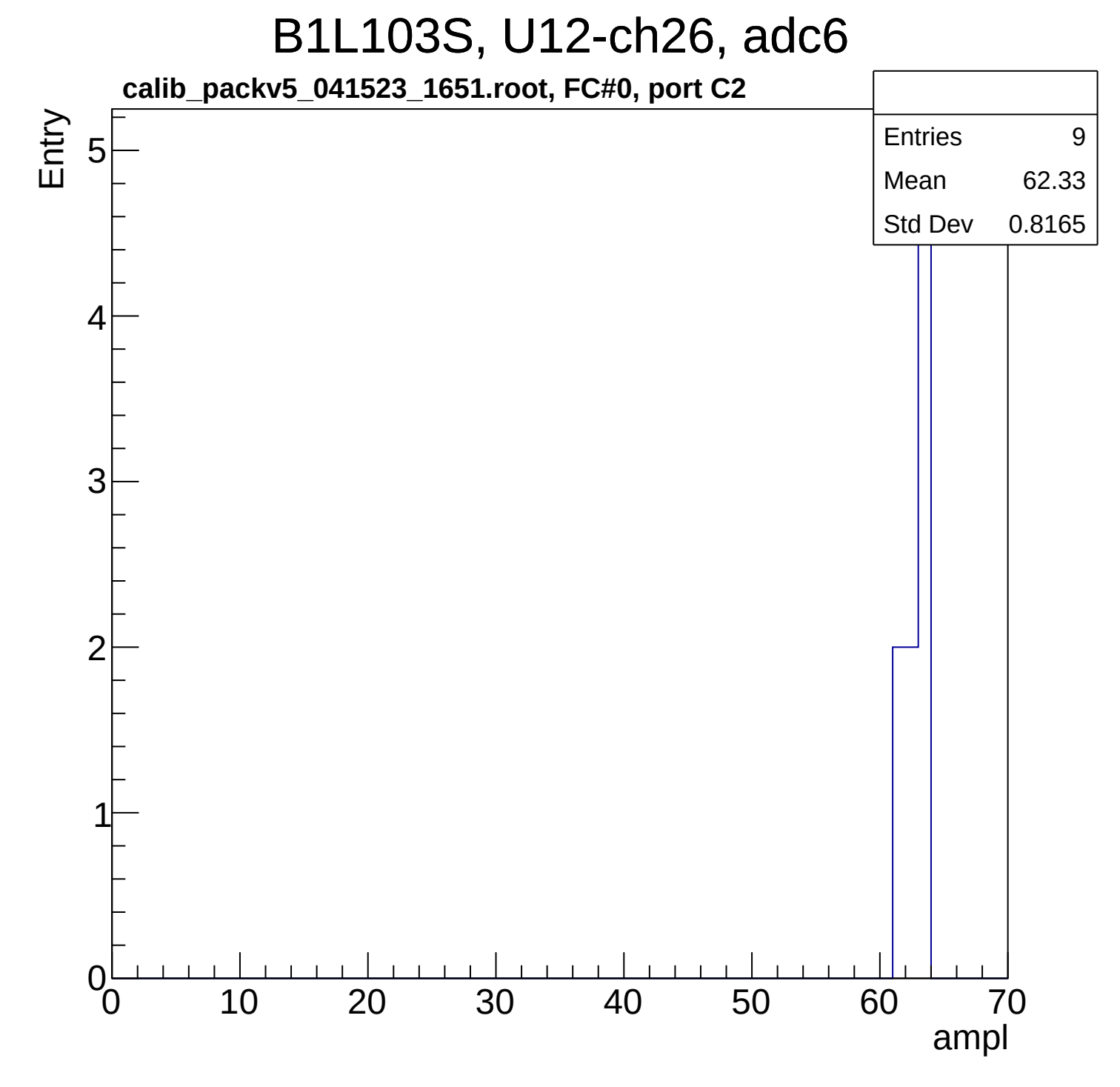
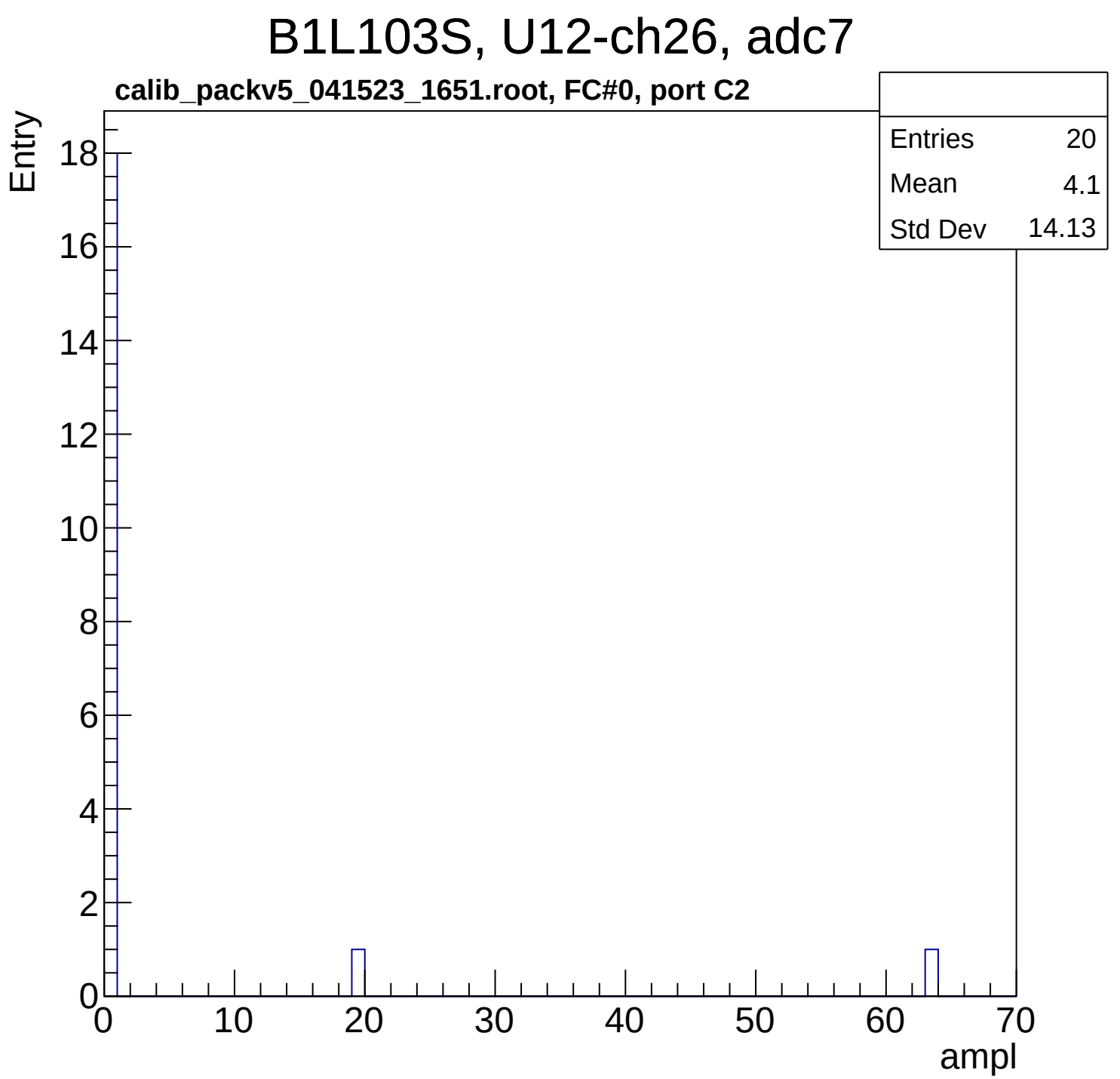

B1L103S, U12-ch26, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 62.33
Std Dev 0.8165
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U12-ch26, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.1
Std Dev 14.13
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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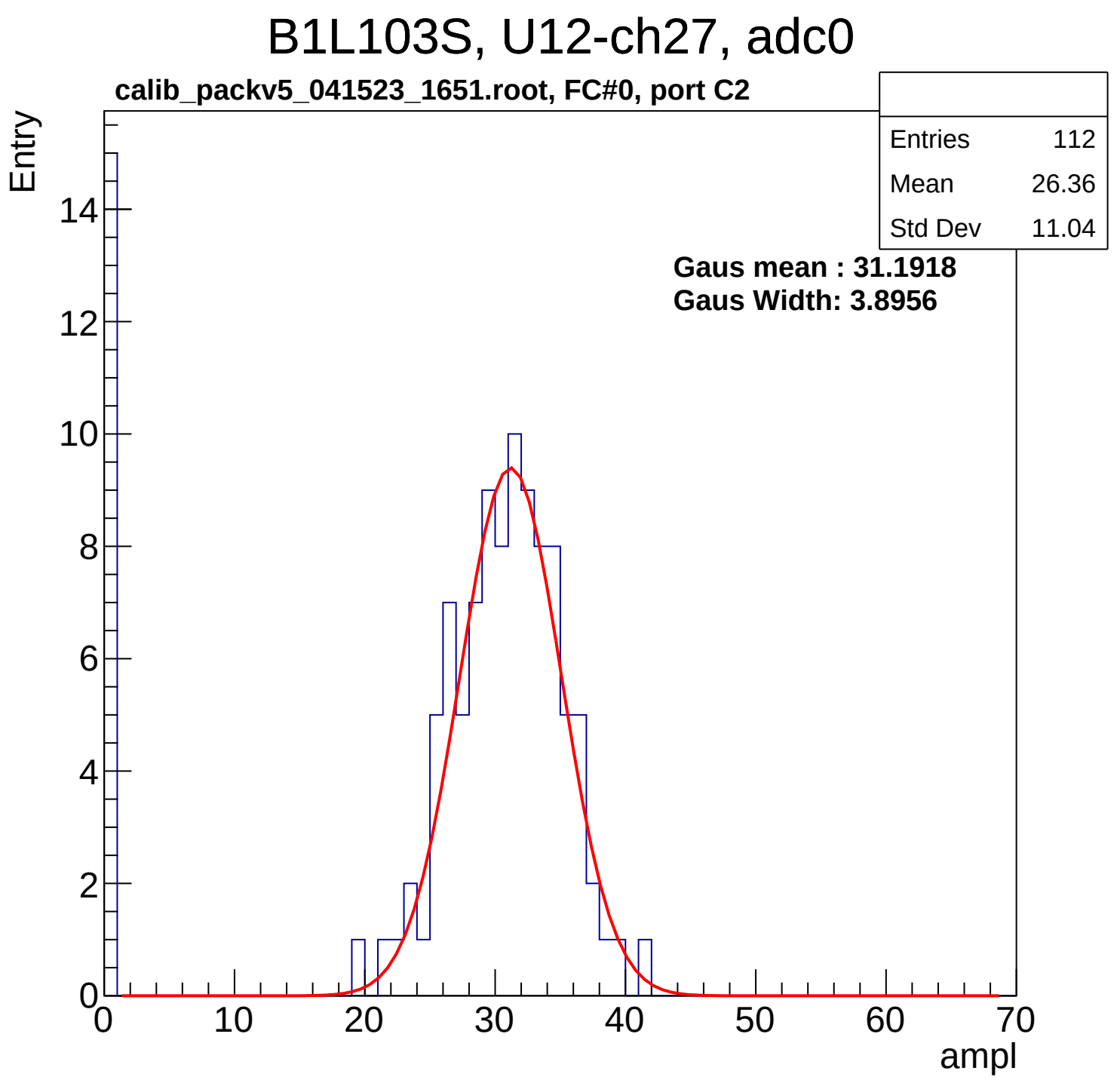
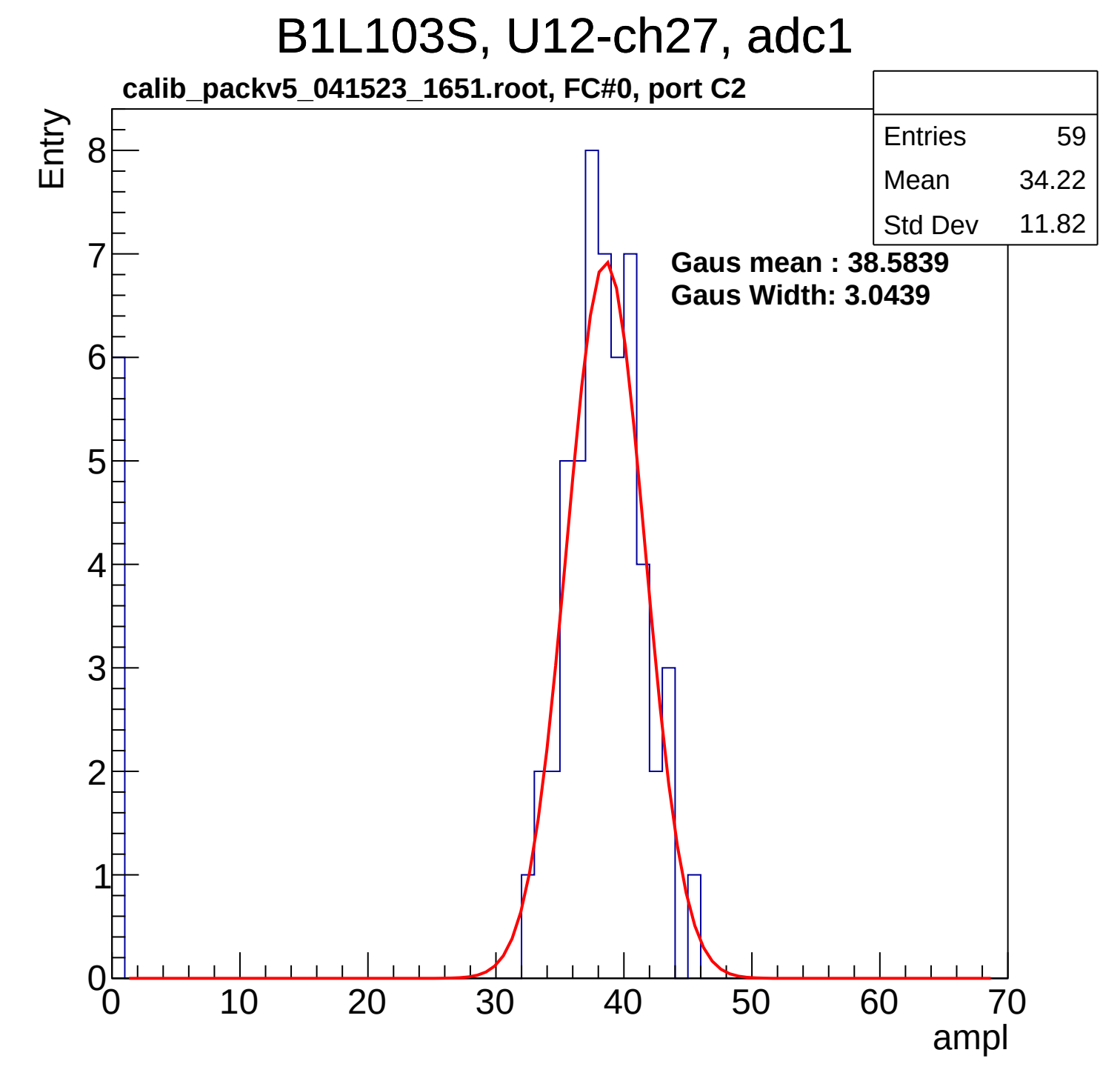
50
60
70
ampl


B1L103S, U12-ch27, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 112
Mean 26.36
Std Dev 11.04
Gaus mean : 31.1918
Gaus Width: 3.8956
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U12-ch27, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 34.22
Std Dev 11.82
Gaus mean : 38.5839
Gaus Width: 3.0439
Entry
ampl
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1
2
3
4
5
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7
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0
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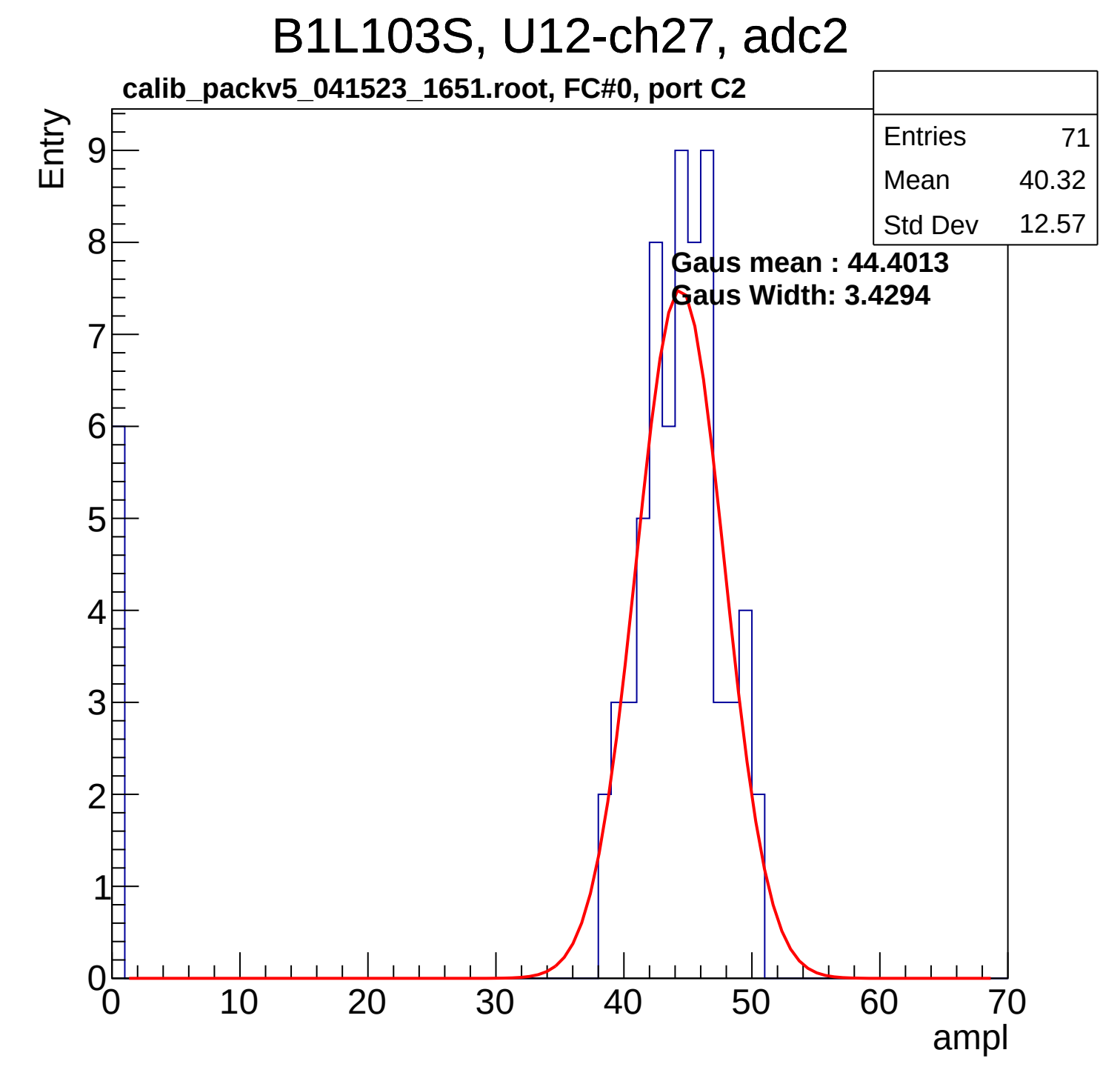
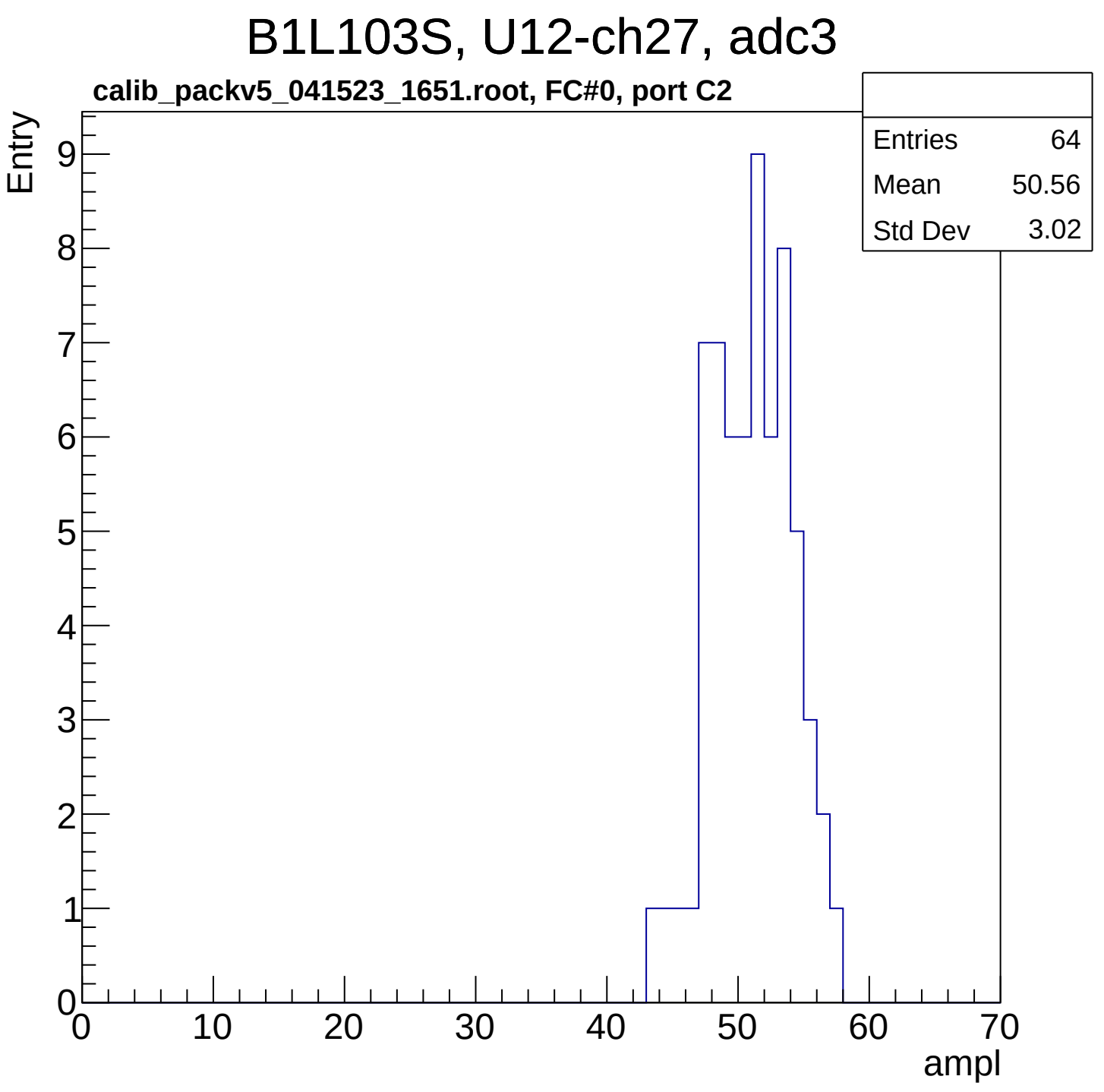

B1L103S, U12-ch27, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 40.32
Std Dev 12.57
Gaus mean : 44.4013
Gaus Width: 3.4294
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U12-ch27, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 50.56
Std Dev 3.02
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
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60
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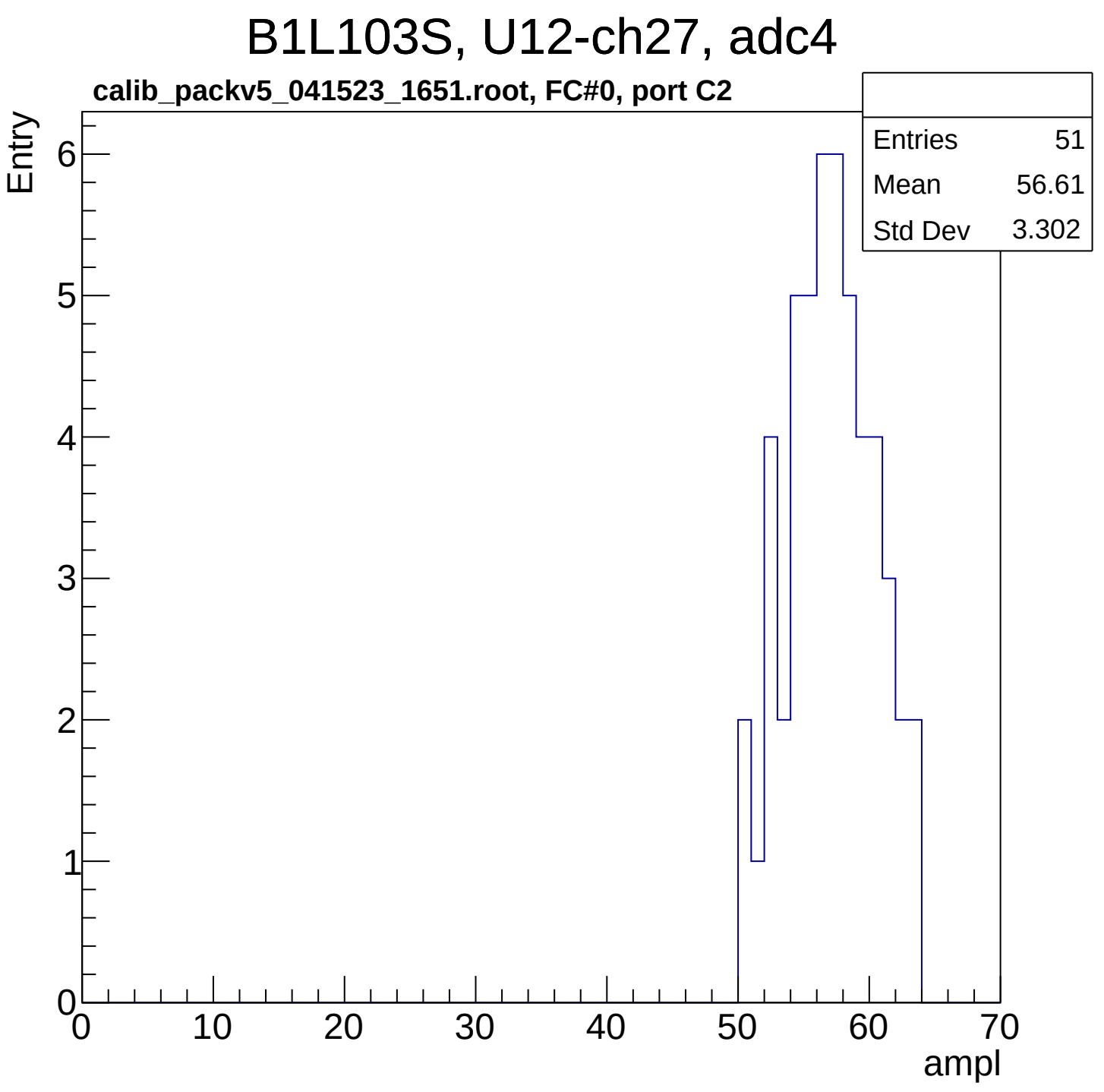
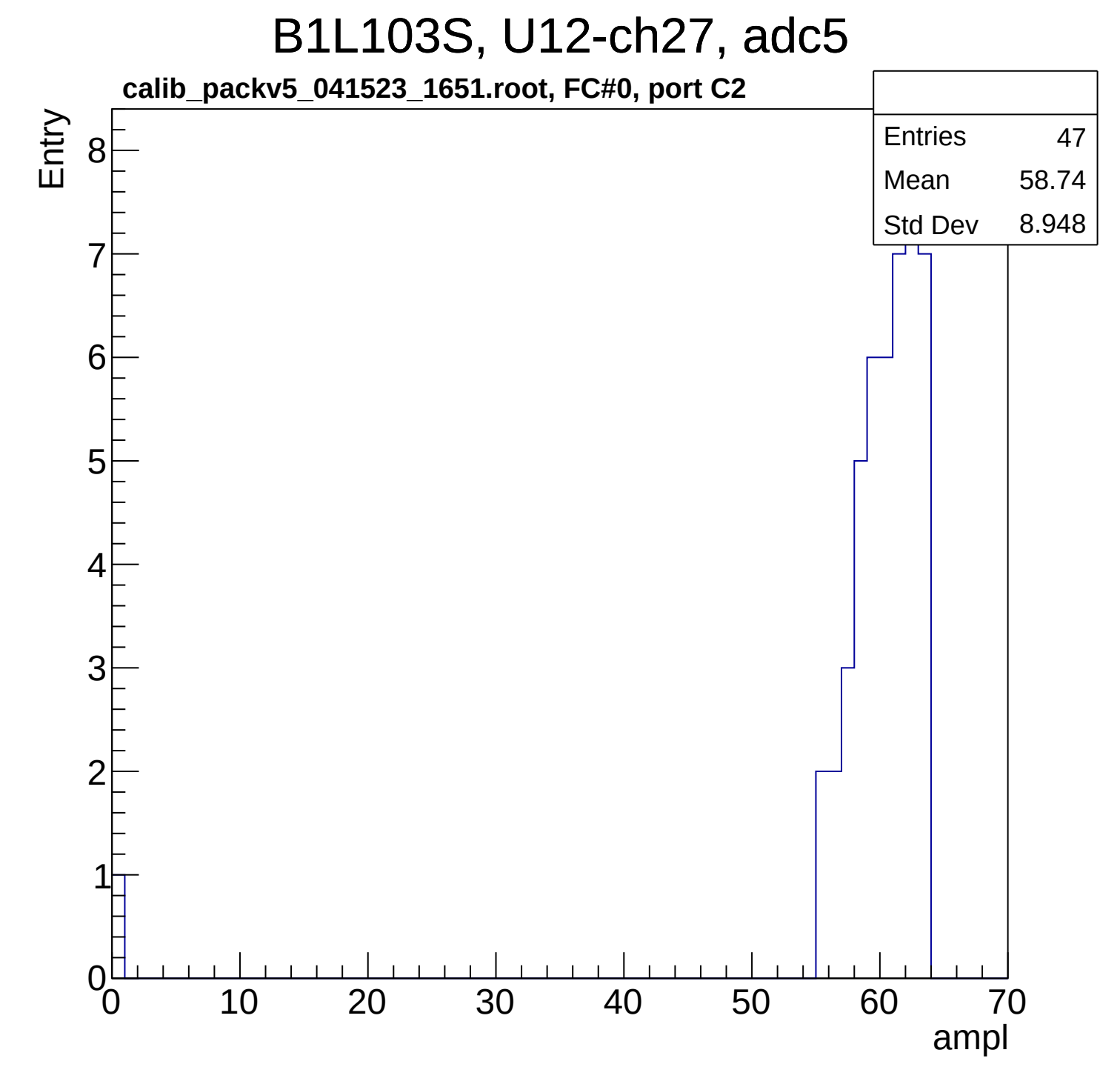

B1L103S, U12-ch27, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 56.61
Std Dev 3.302
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U12-ch27, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.74
Std Dev 8.948
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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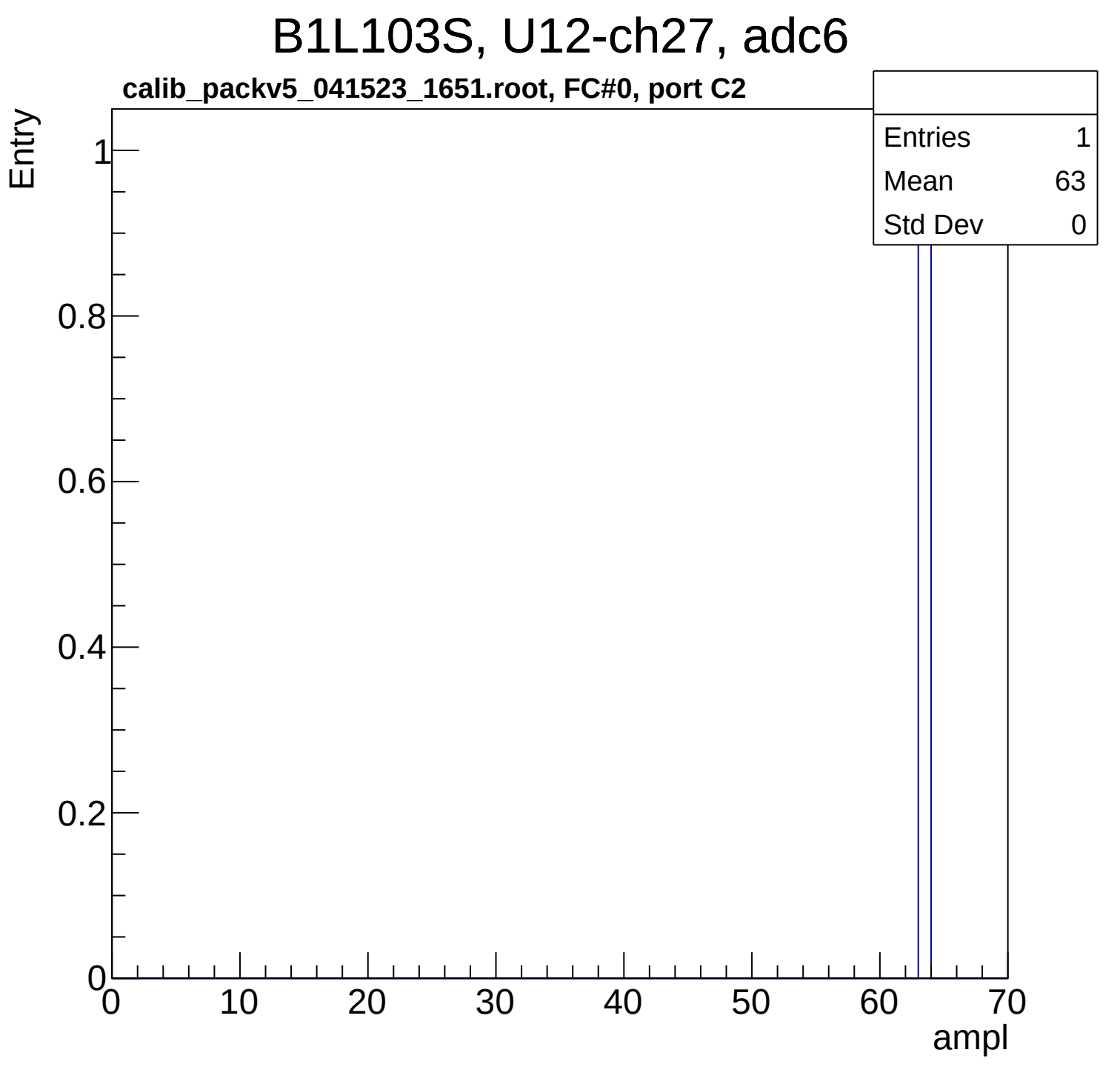
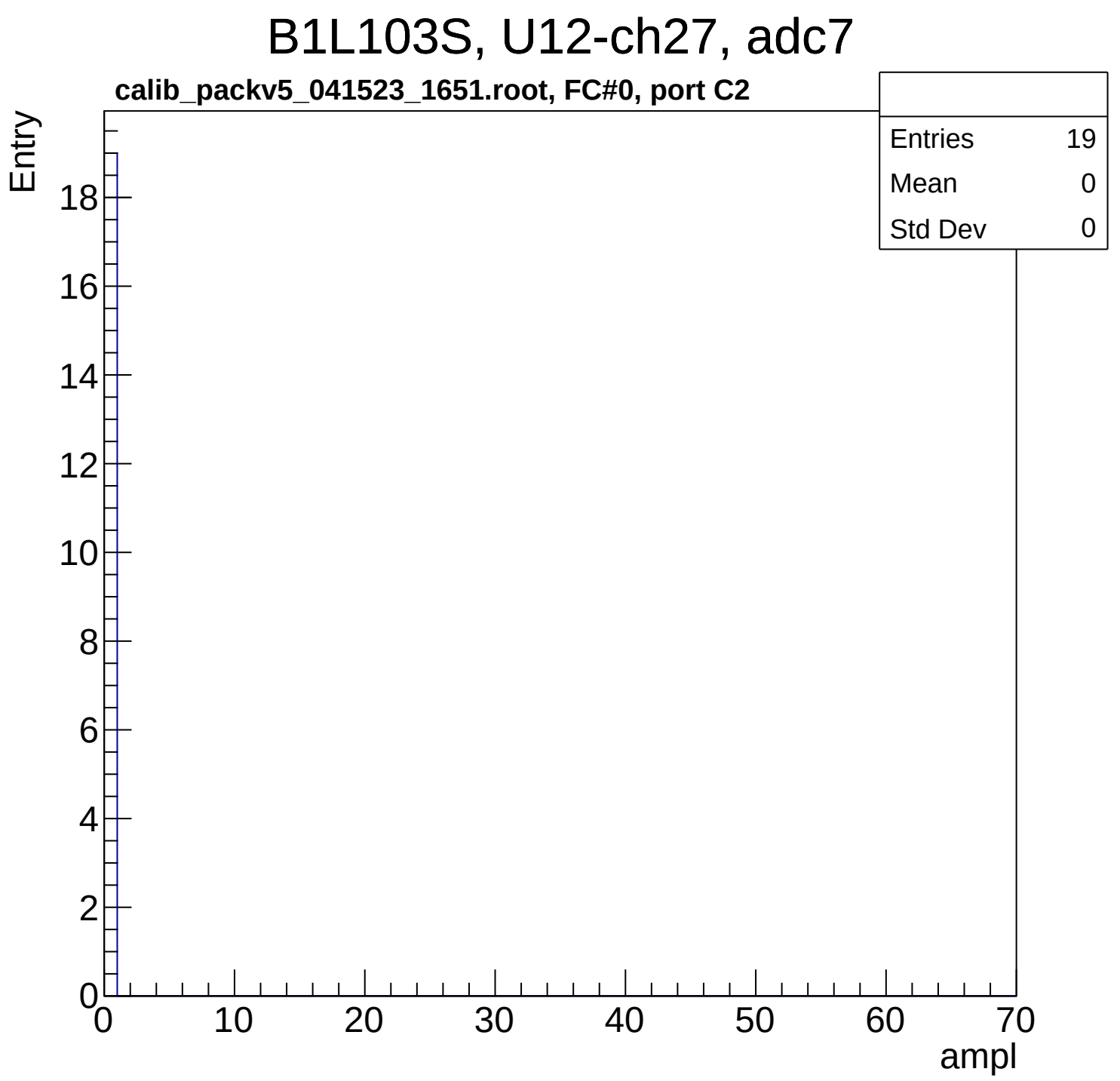
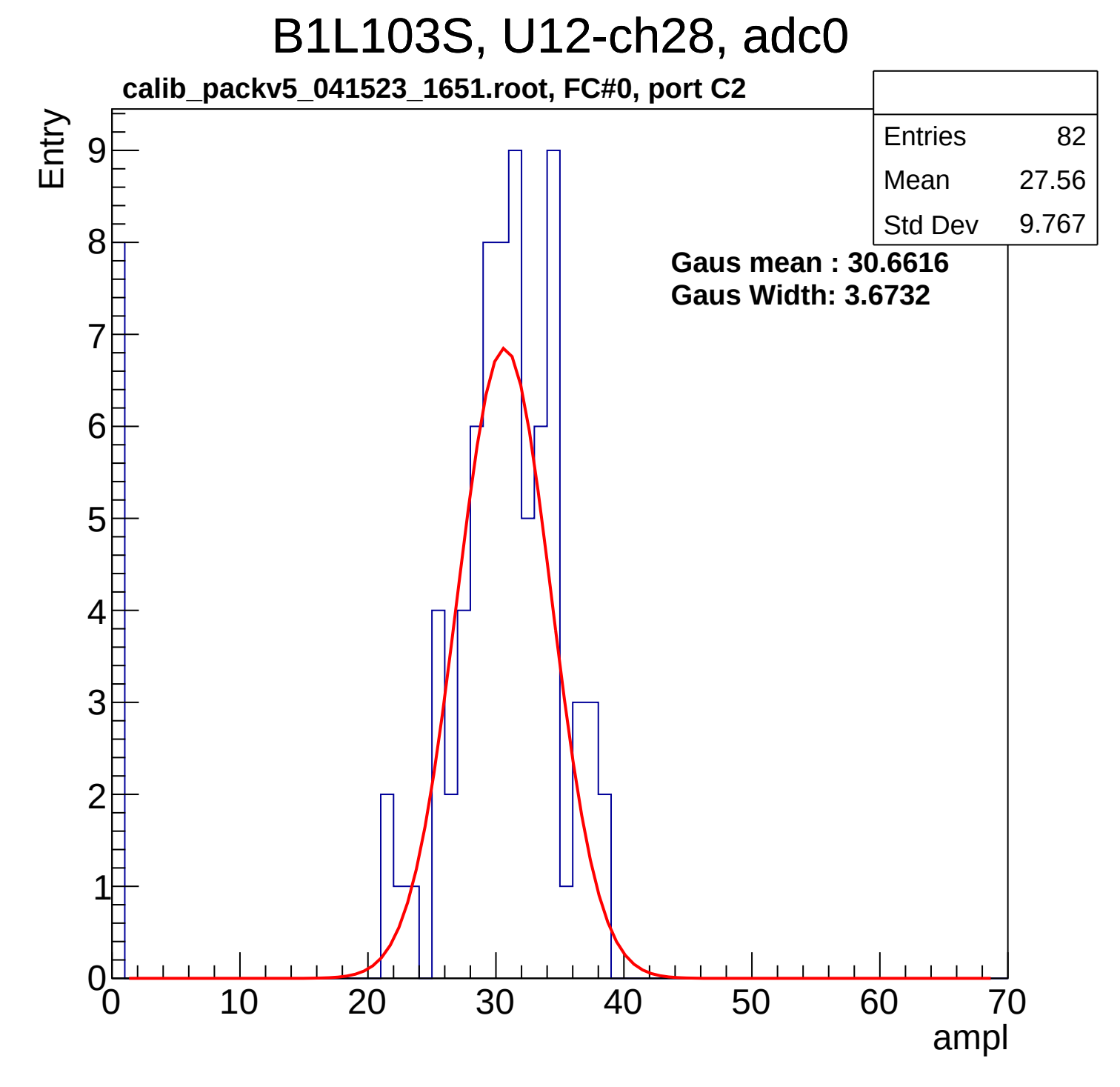

B1L103S, U12-ch27, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch27, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch28, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 27.56
Std Dev 9.767
Gaus mean : 30.6616
Gaus Width: 3.6732
Entry
ampl
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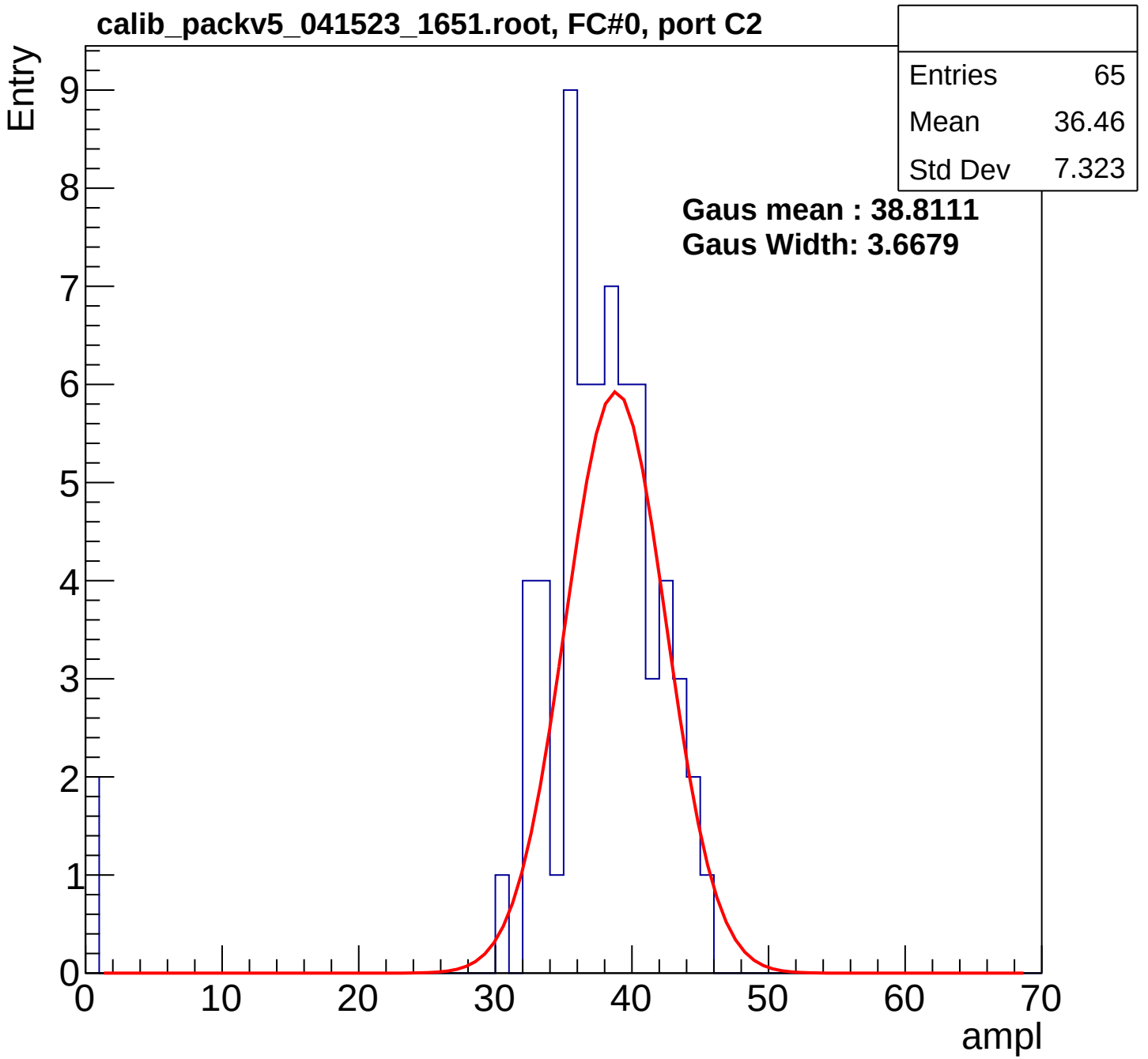
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch28, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 36.46
Std Dev 7.323
Gaus mean : 38.8111
Gaus Width: 3.6679
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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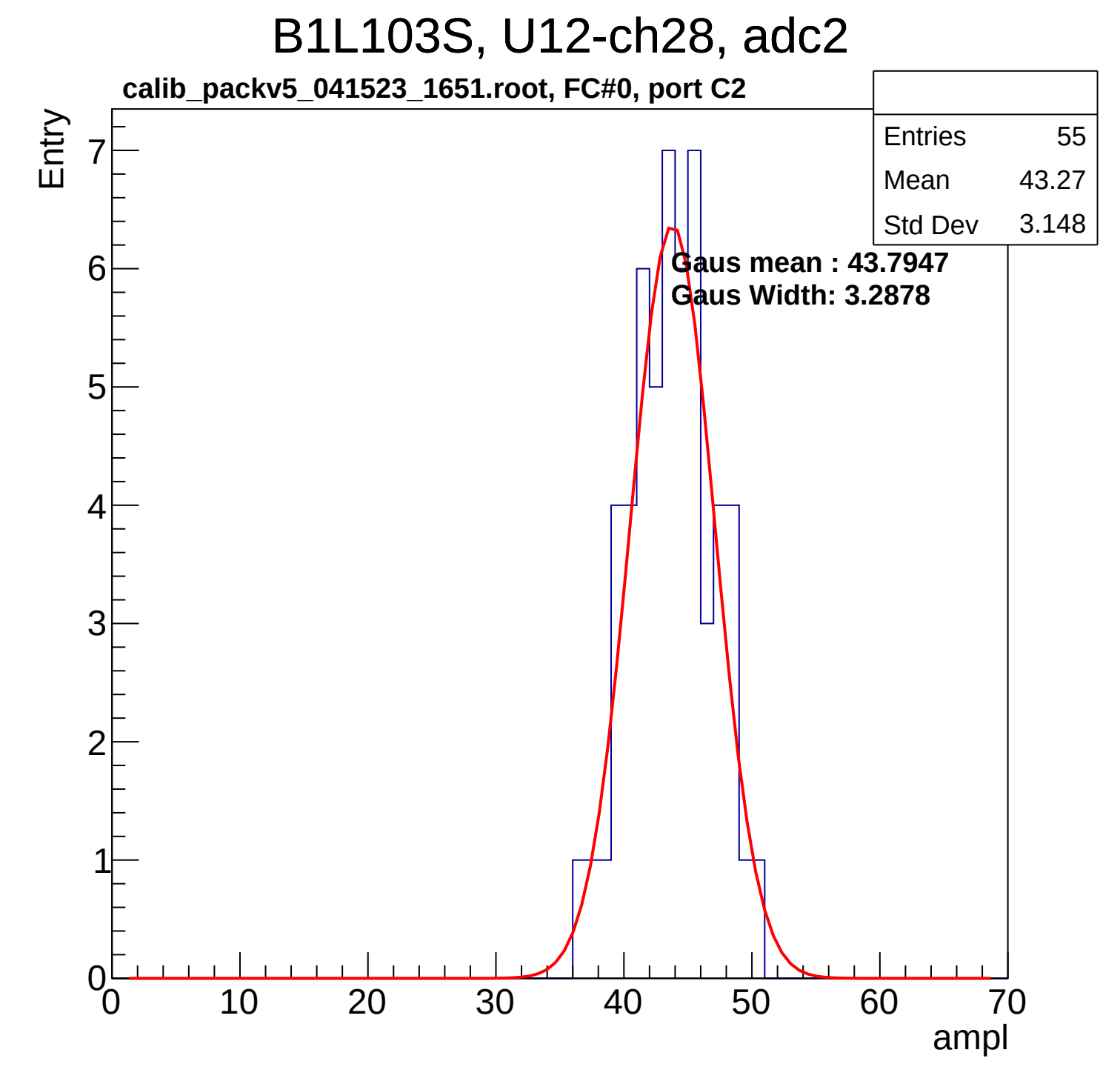
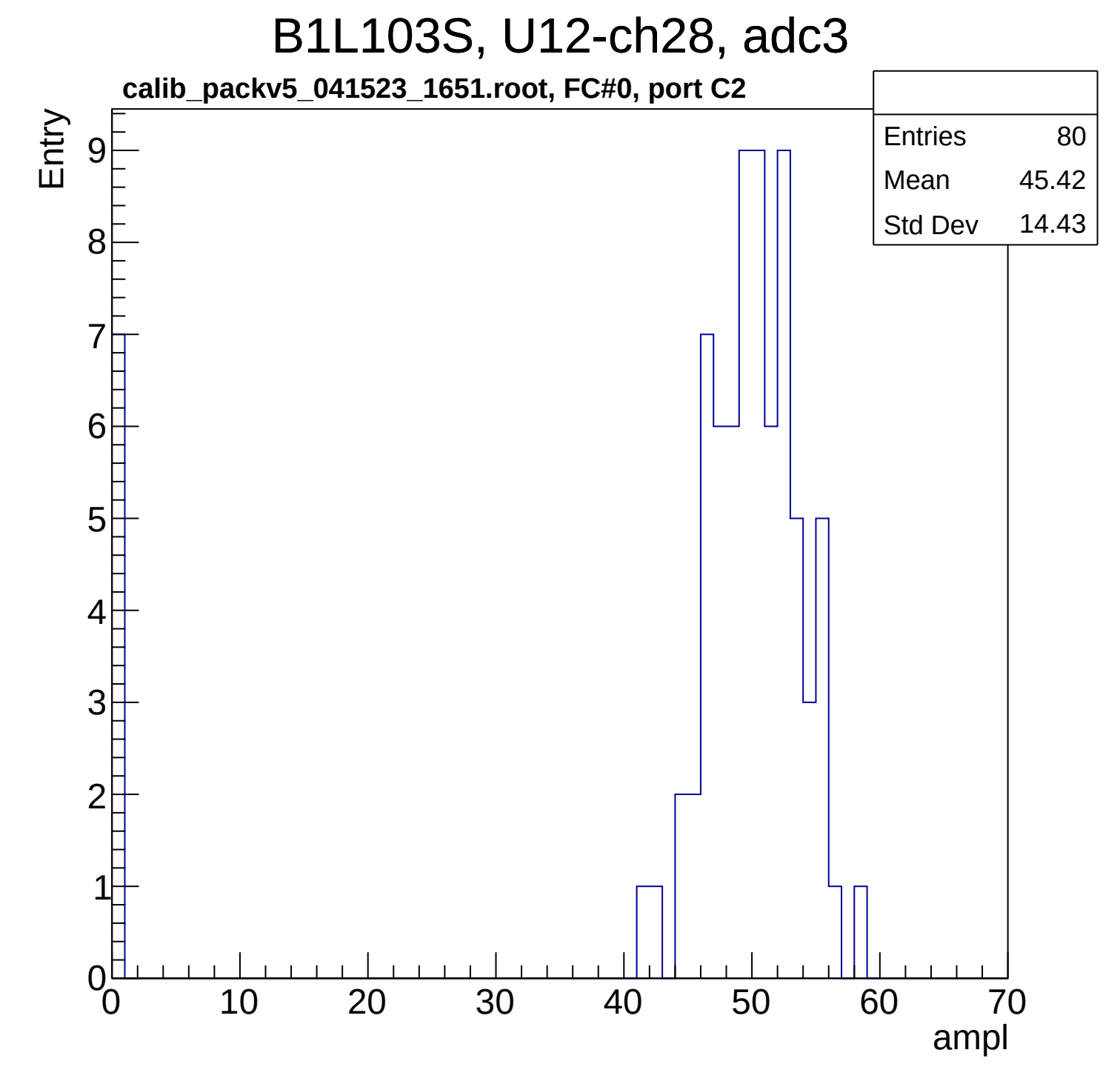

B1L103S, U12-ch28, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 43.27
Std Dev 3.148
Gaus mean : 43.7947
Gaus Width: 3.2878
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U12-ch28, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 45.42
Std Dev 14.43
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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40
50
60
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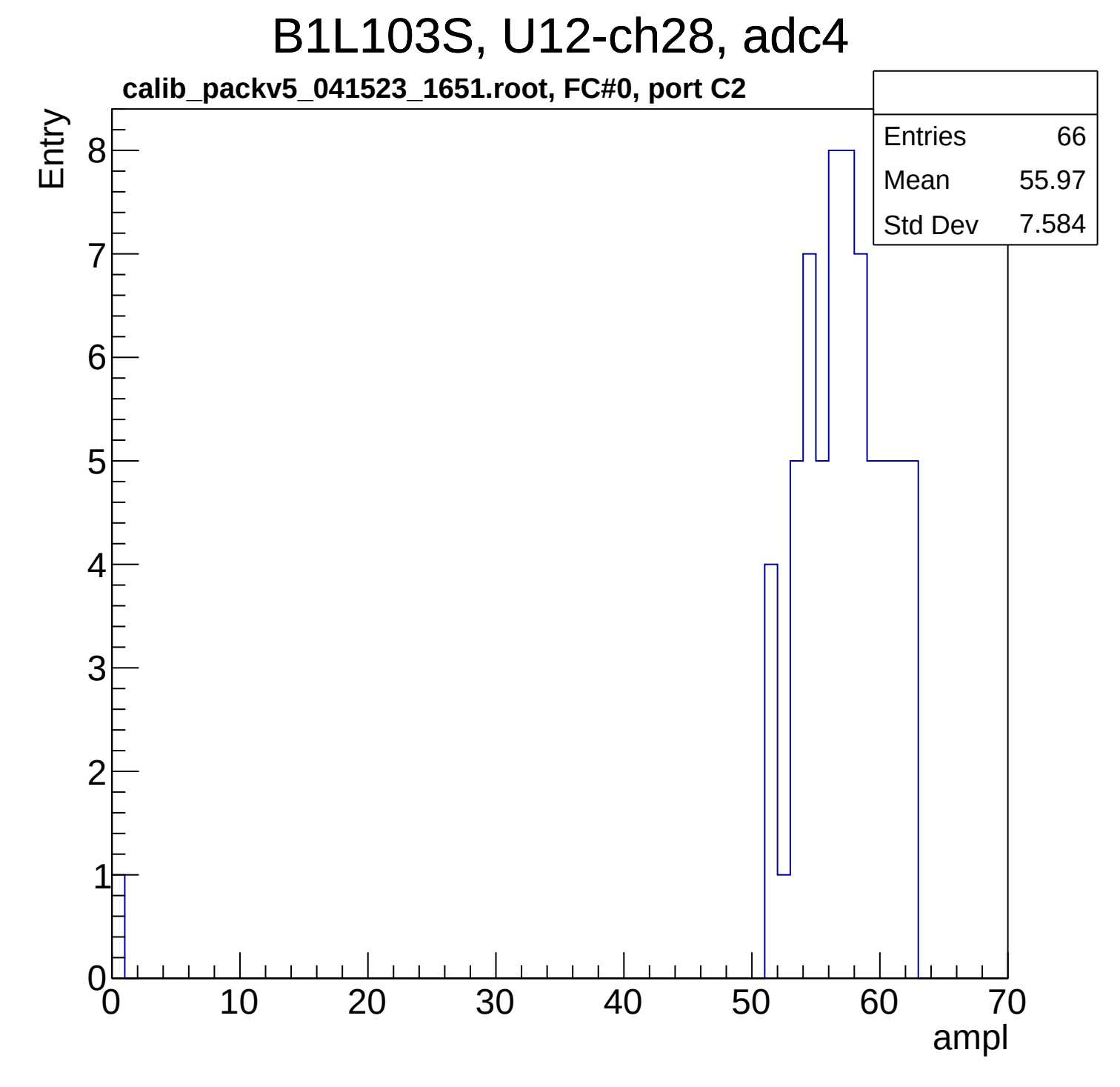
B1L103S, U12-ch28, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 55.97
Std Dev 7.584
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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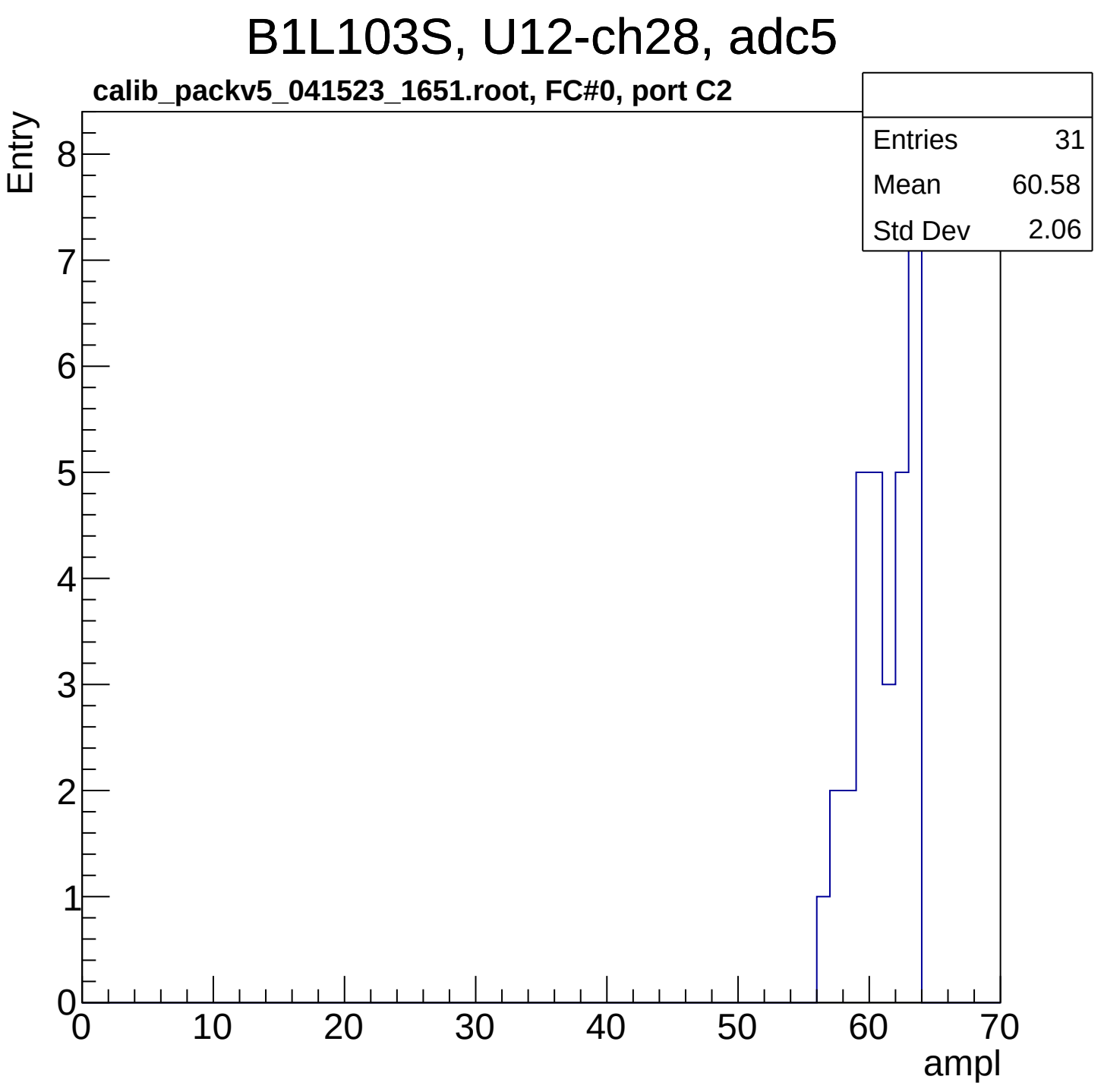
B1L103S, U12-ch28, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 31
Mean 60.58
Std Dev 2.06
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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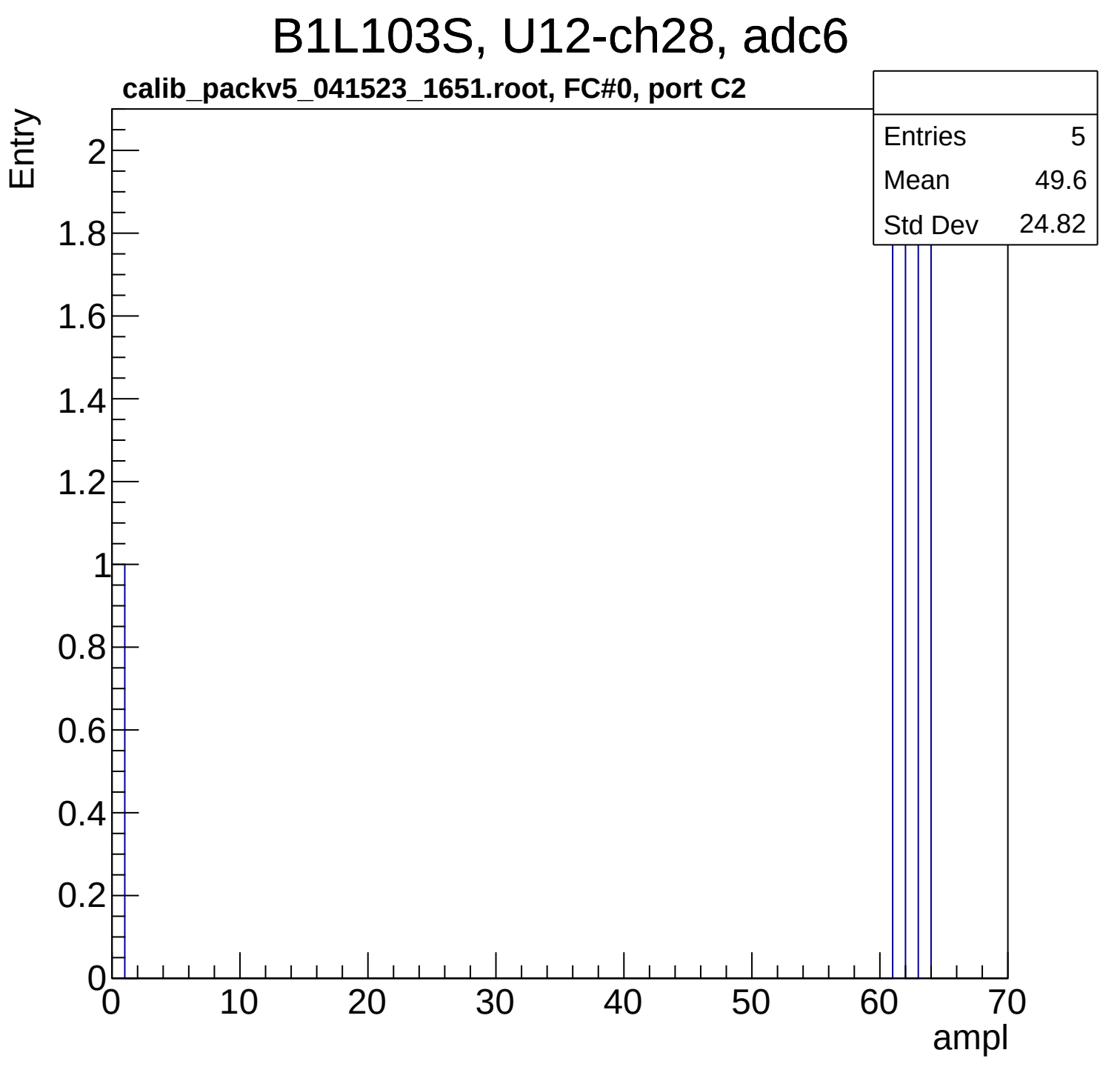
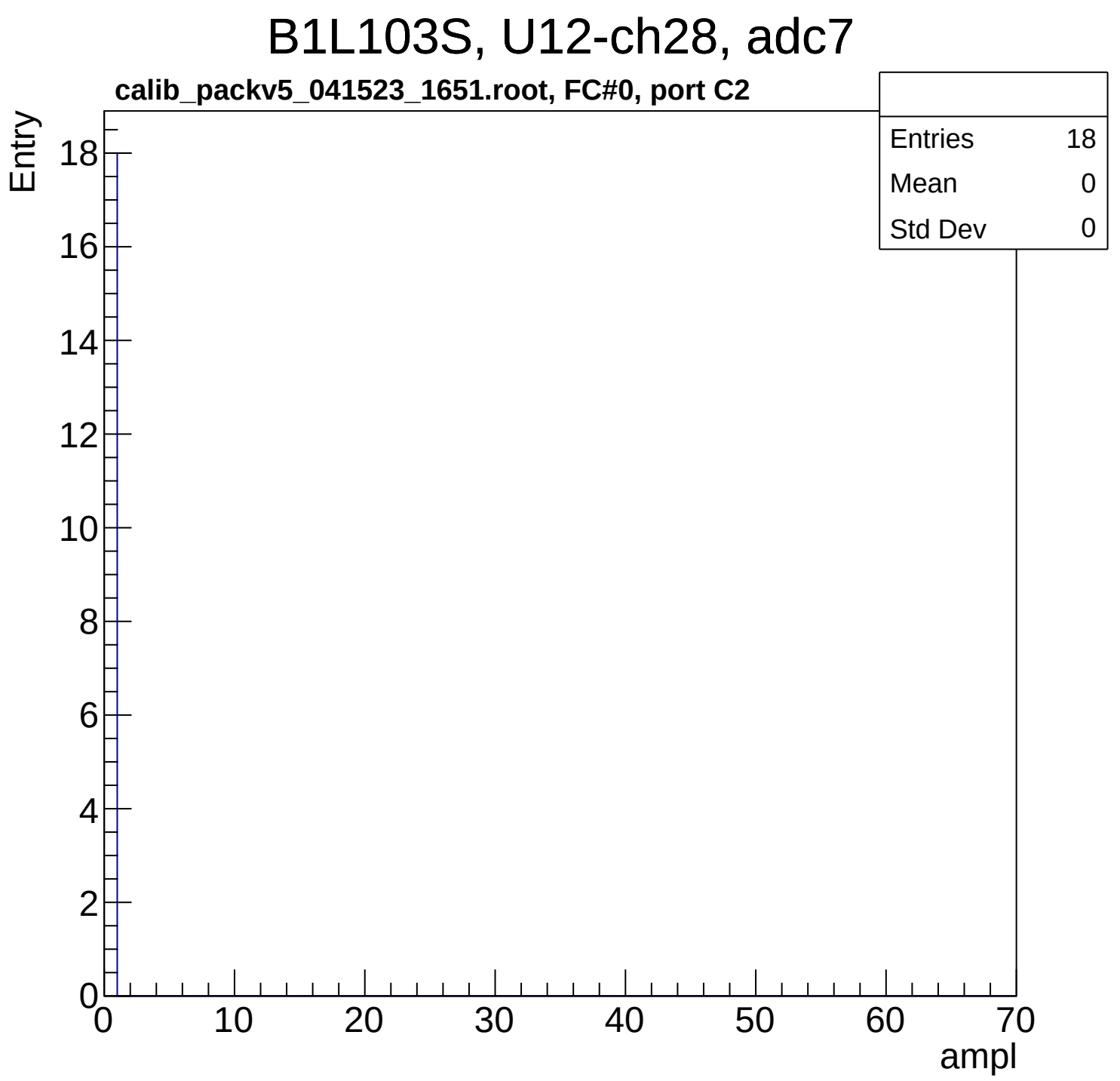

B1L103S, U12-ch28, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 49.6
Std Dev 24.82
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U12-ch28, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
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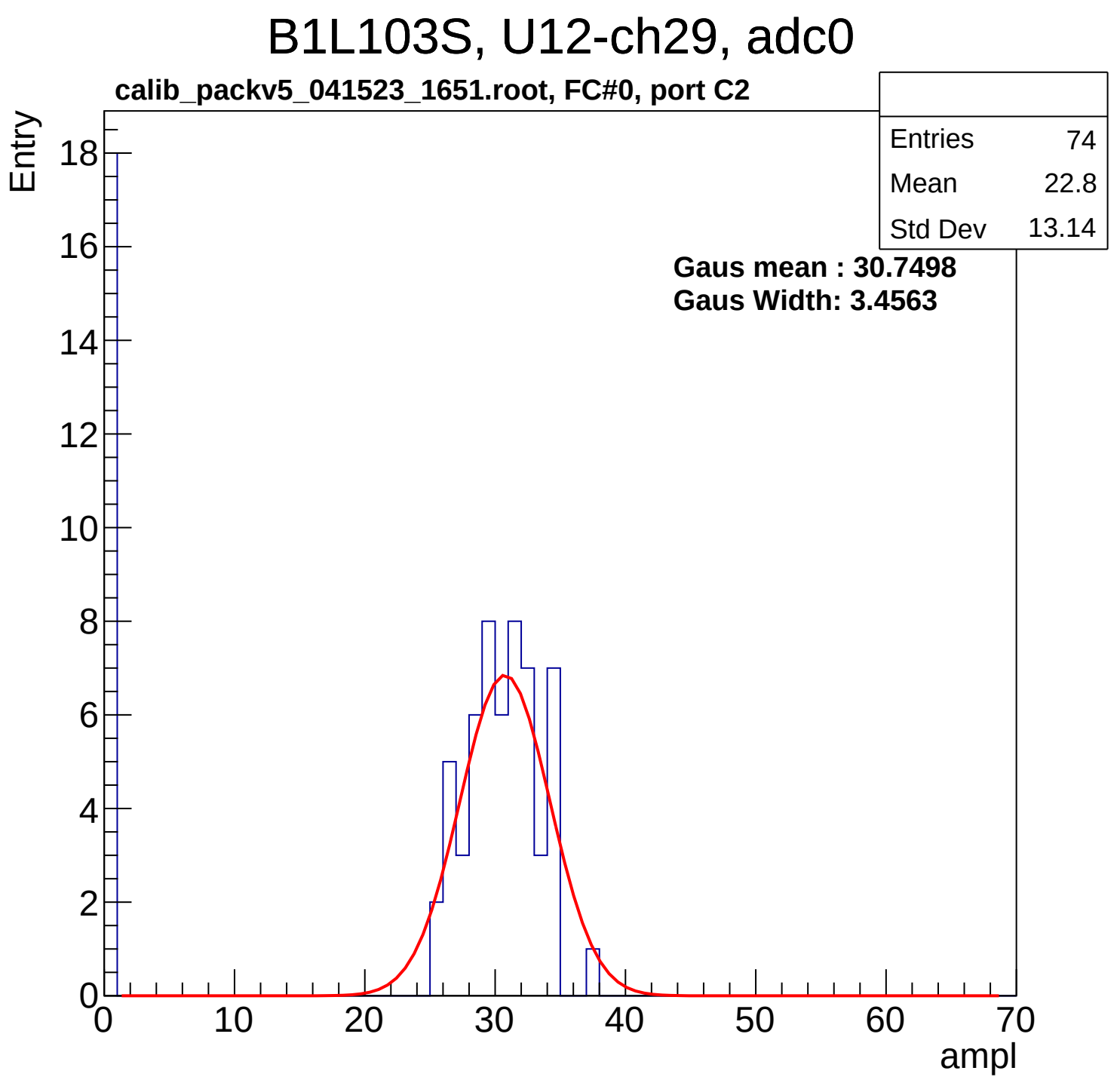
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch29, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 22.8
Std Dev 13.14
Gaus mean : 30.7498
Gaus Width: 3.4563
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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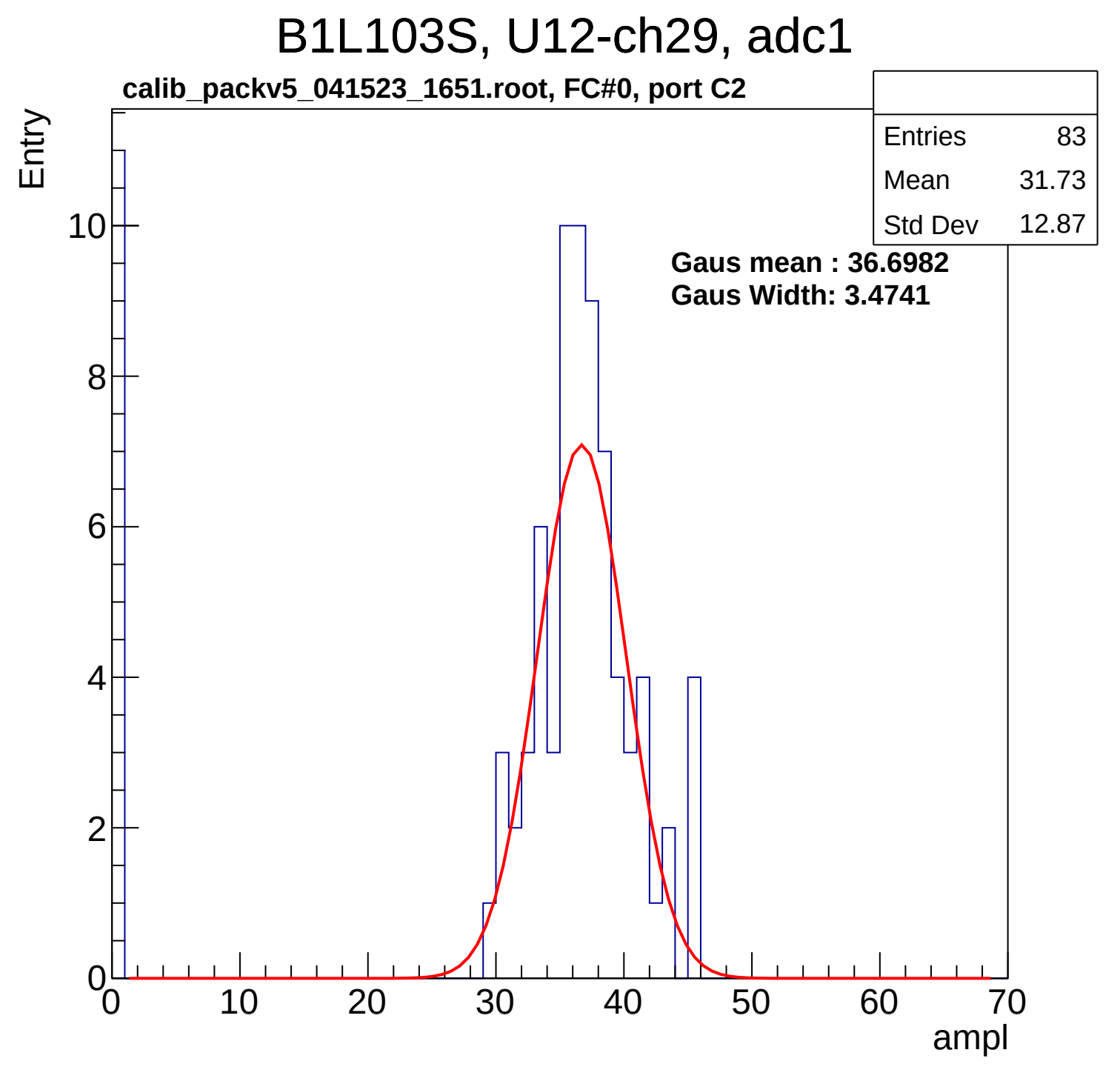
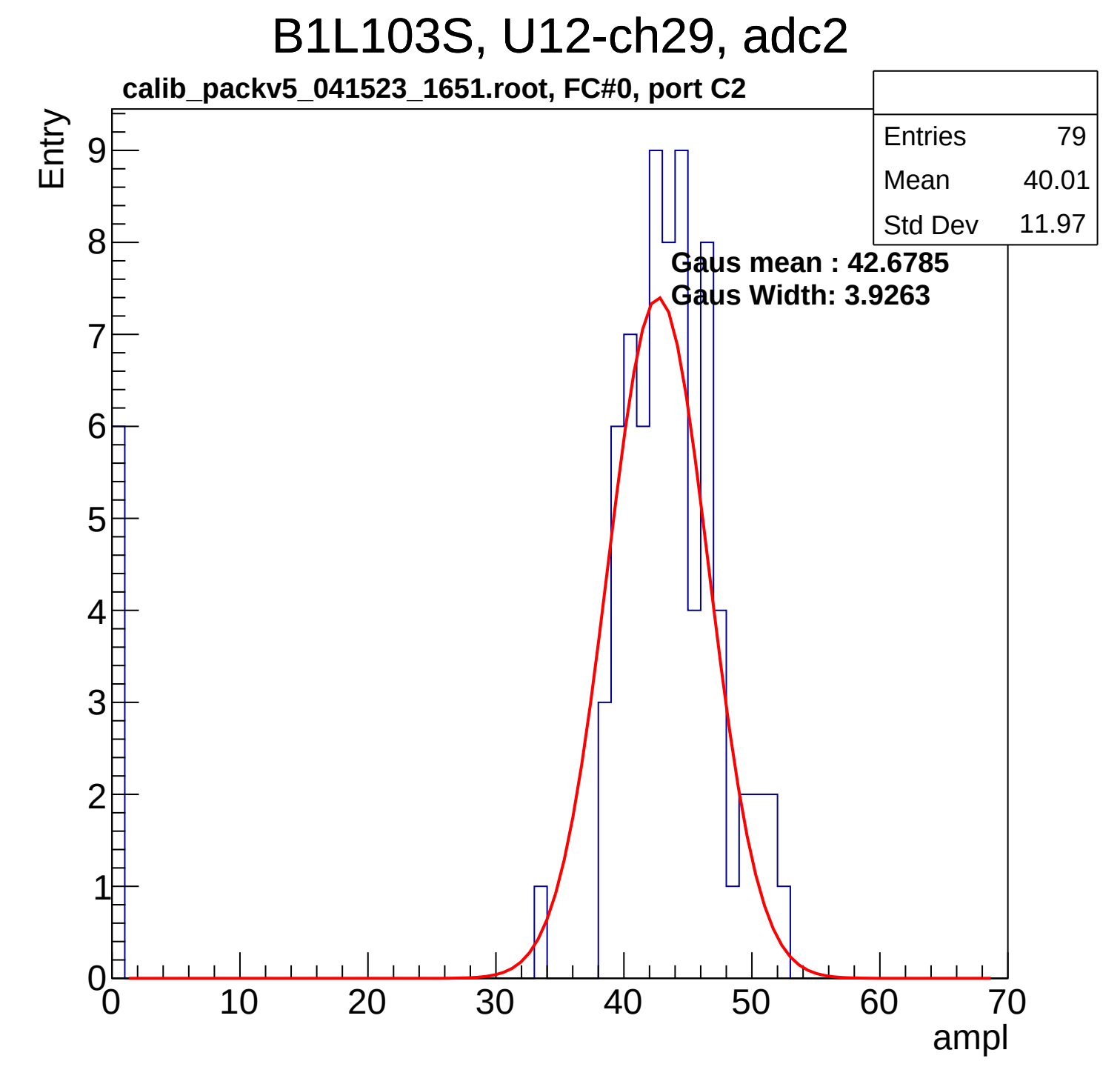

B1L103S, U12-ch29, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 31.73
Std Dev 12.87
Gaus mean : 36.6982
Gaus Width: 3.4741
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch29, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 40.01
Std Dev 11.97
Gaus mean : 42.6785
Gaus Width: 3.9263
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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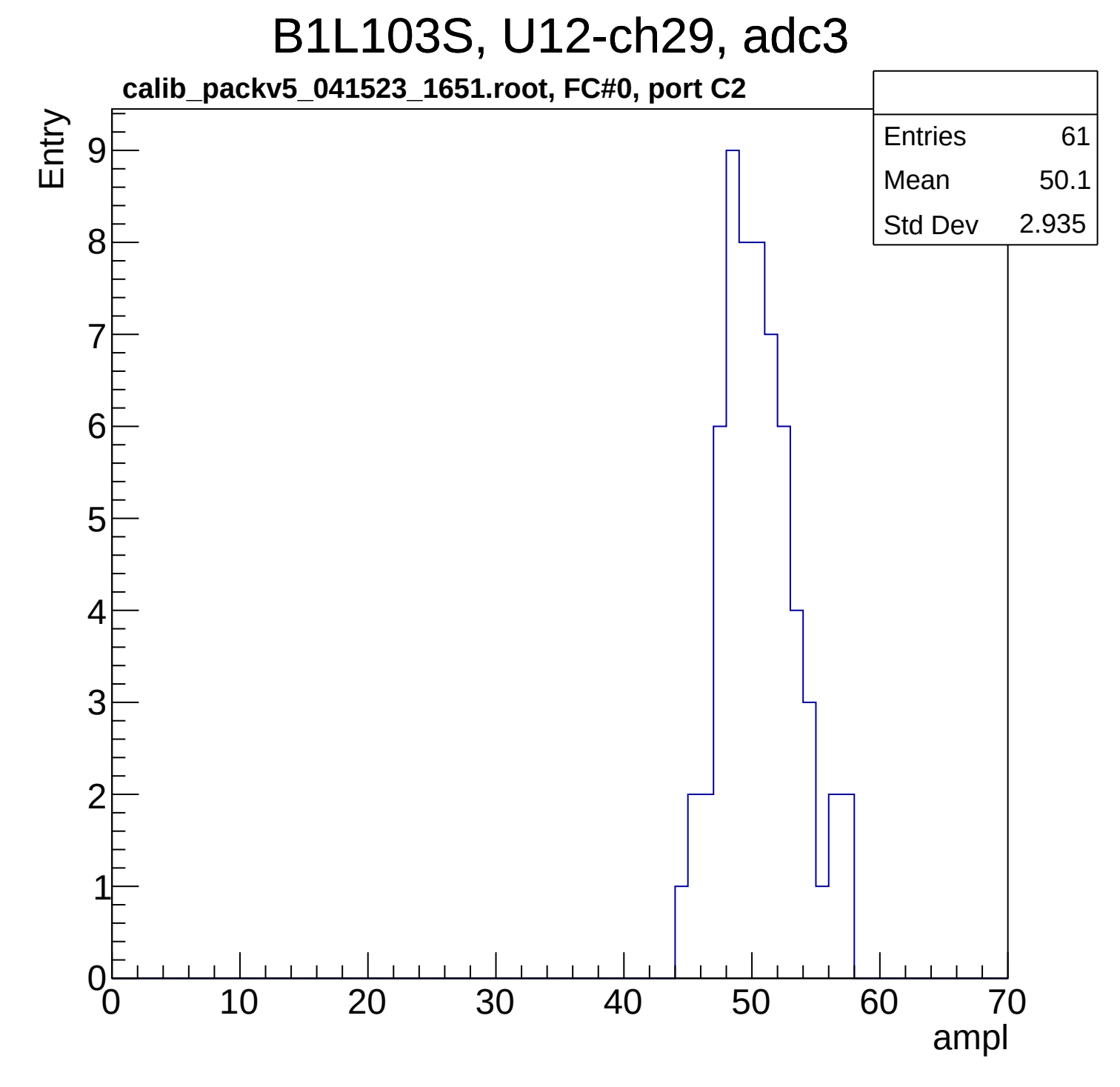
B1L103S, U12-ch29, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 50.1
Std Dev 2.935
Entry
ampl
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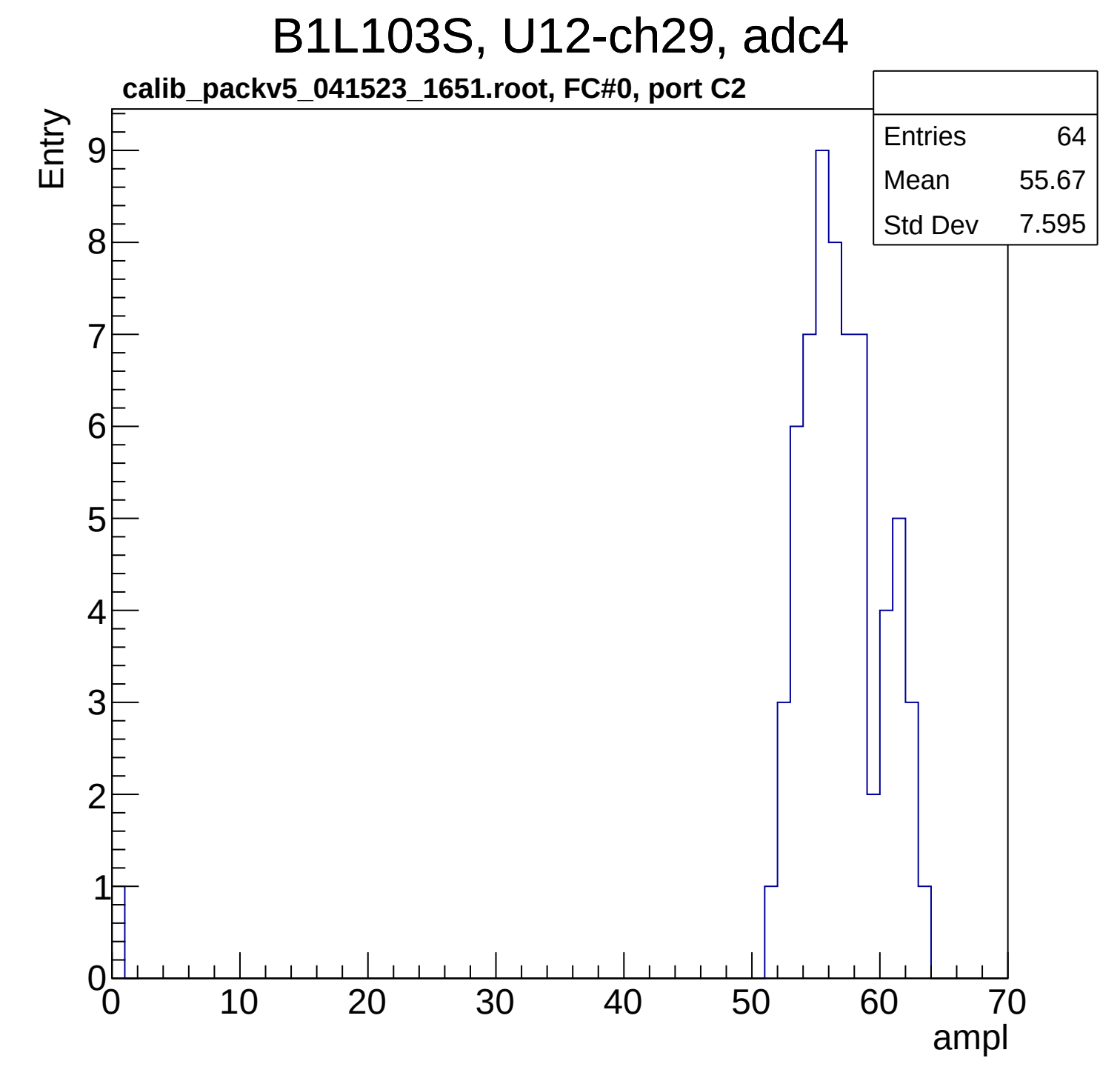
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U12-ch29, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 55.67
Std Dev 7.595
Entry
ampl
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3
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5
6
7
8
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0
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60
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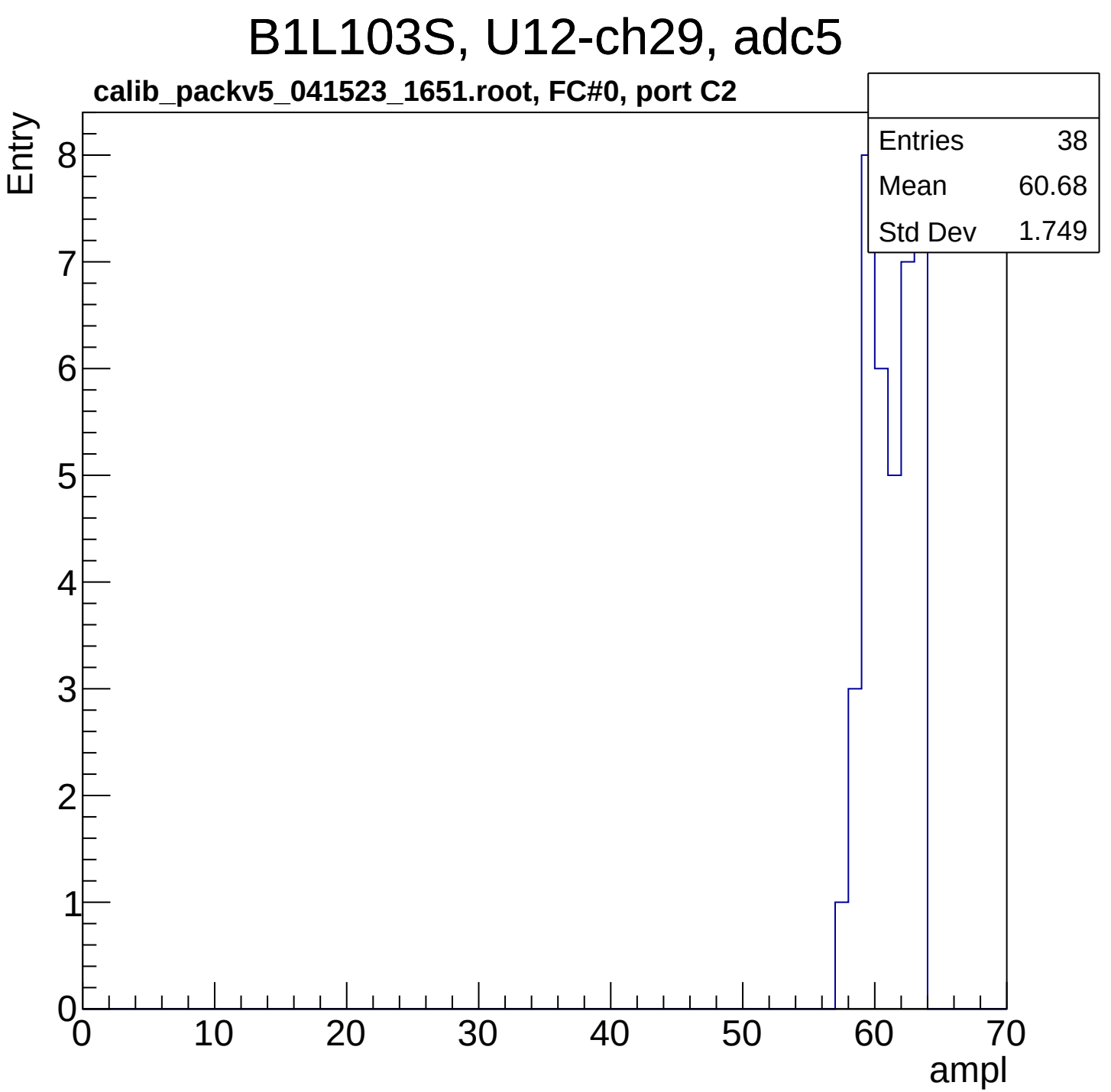
B1L103S, U12-ch29, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 60.68
Std Dev 1.749
Entry
ampl
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1
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3
4
5
6
7
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0
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60
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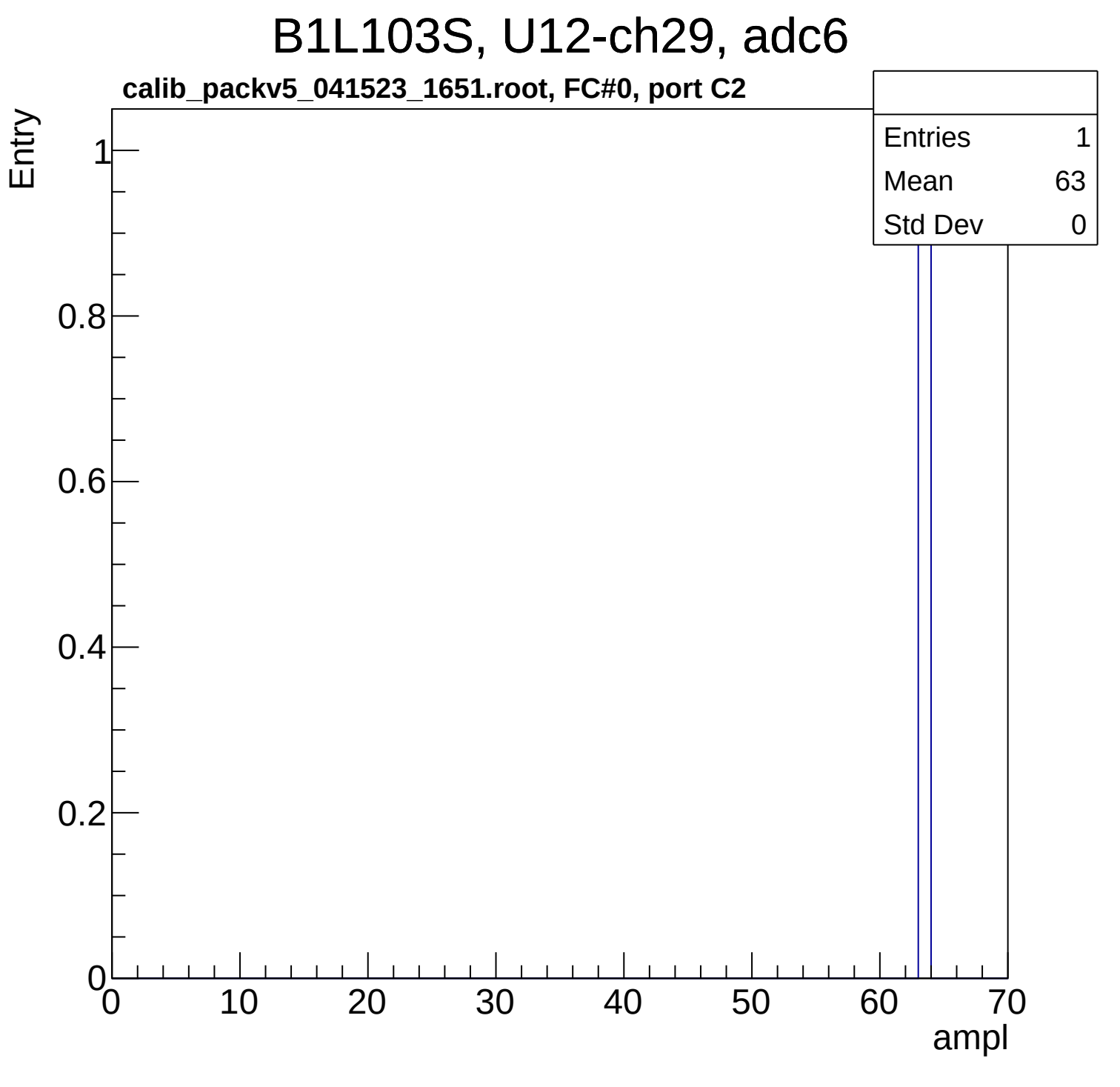
B1L103S, U12-ch29, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 63
Std Dev 0
Entry
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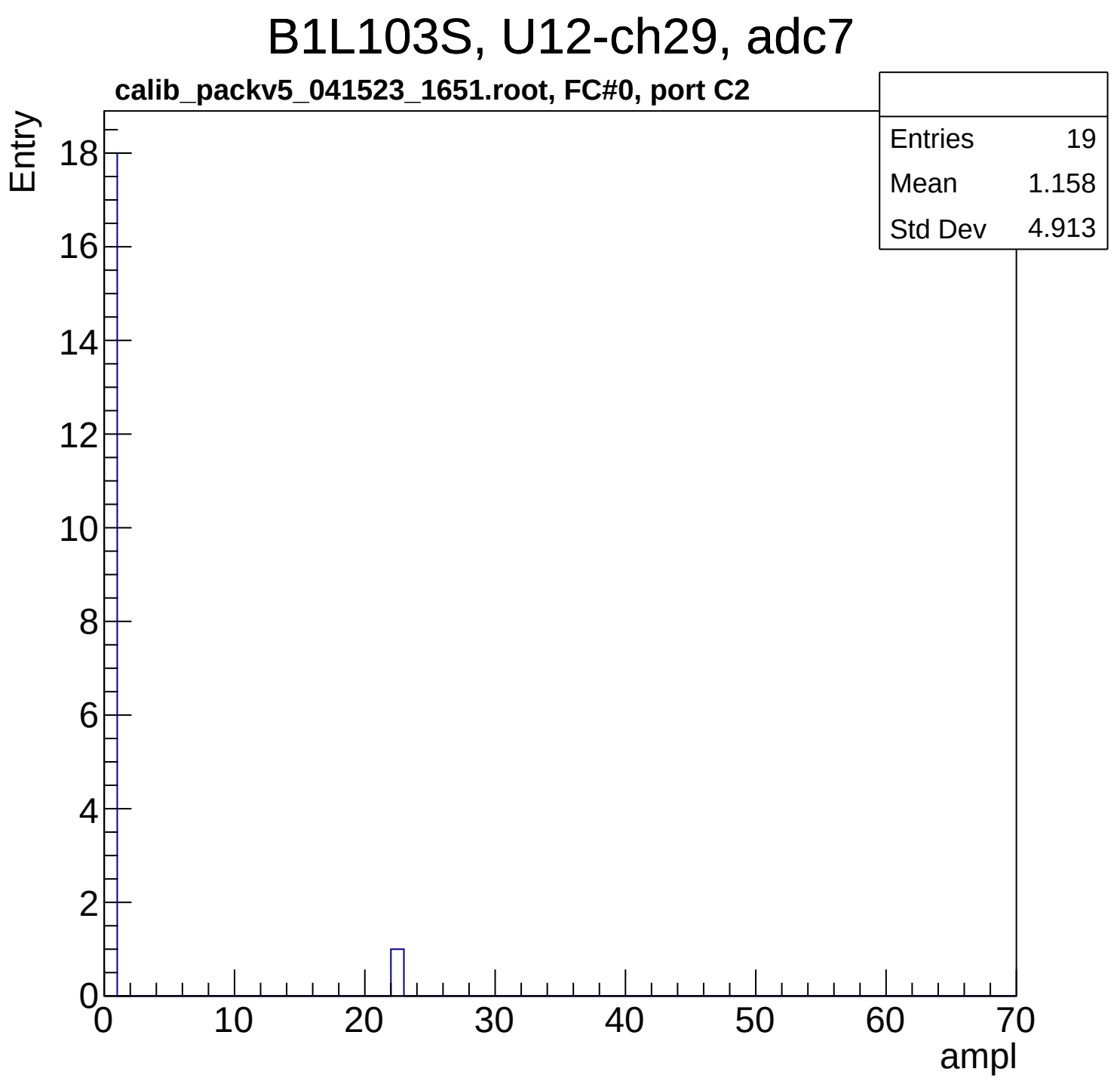
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch29, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
0
2
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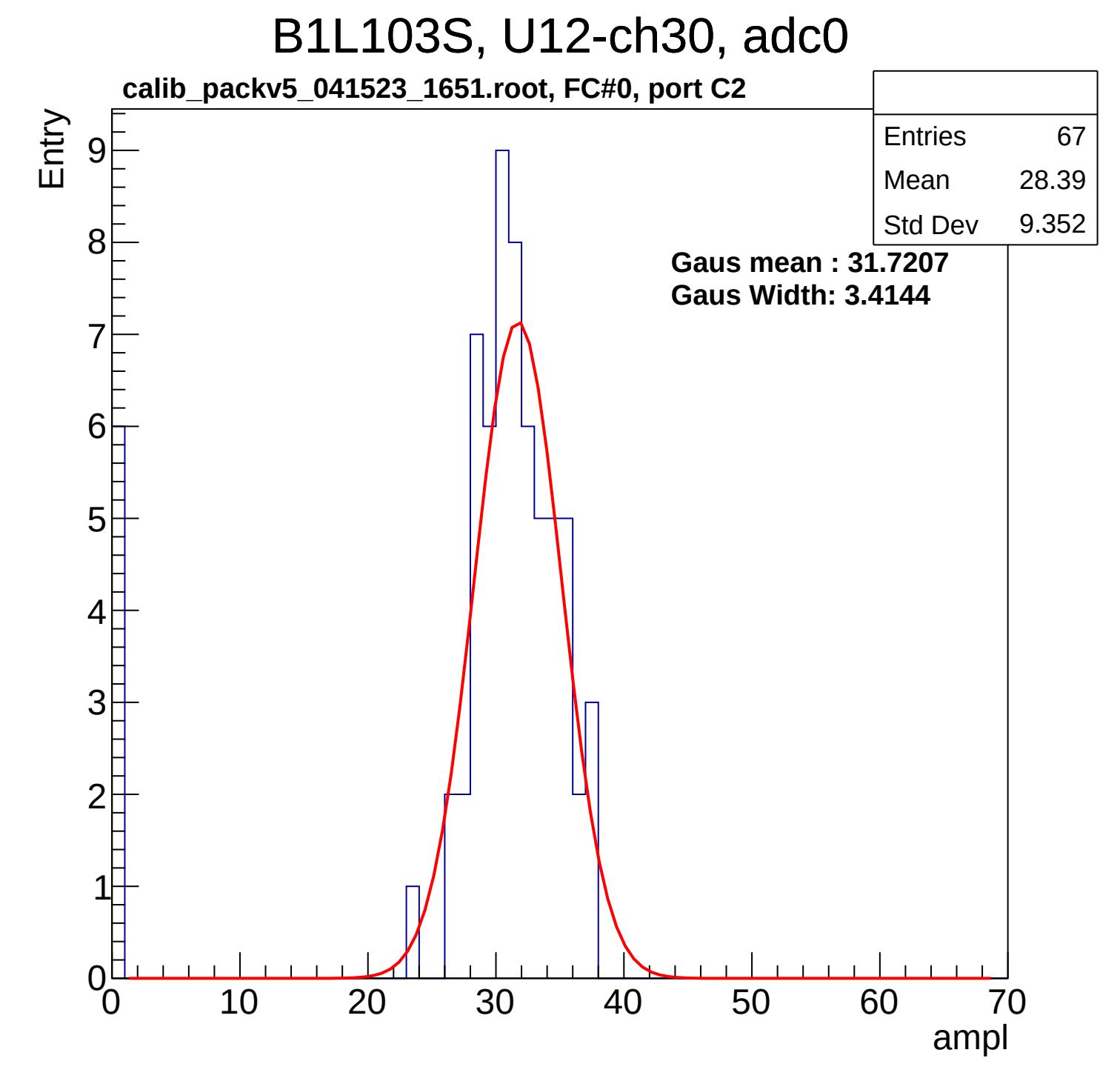
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch30, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 28.39
Std Dev 9.352
Gaus mean : 31.7207
Gaus Width: 3.4144
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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60
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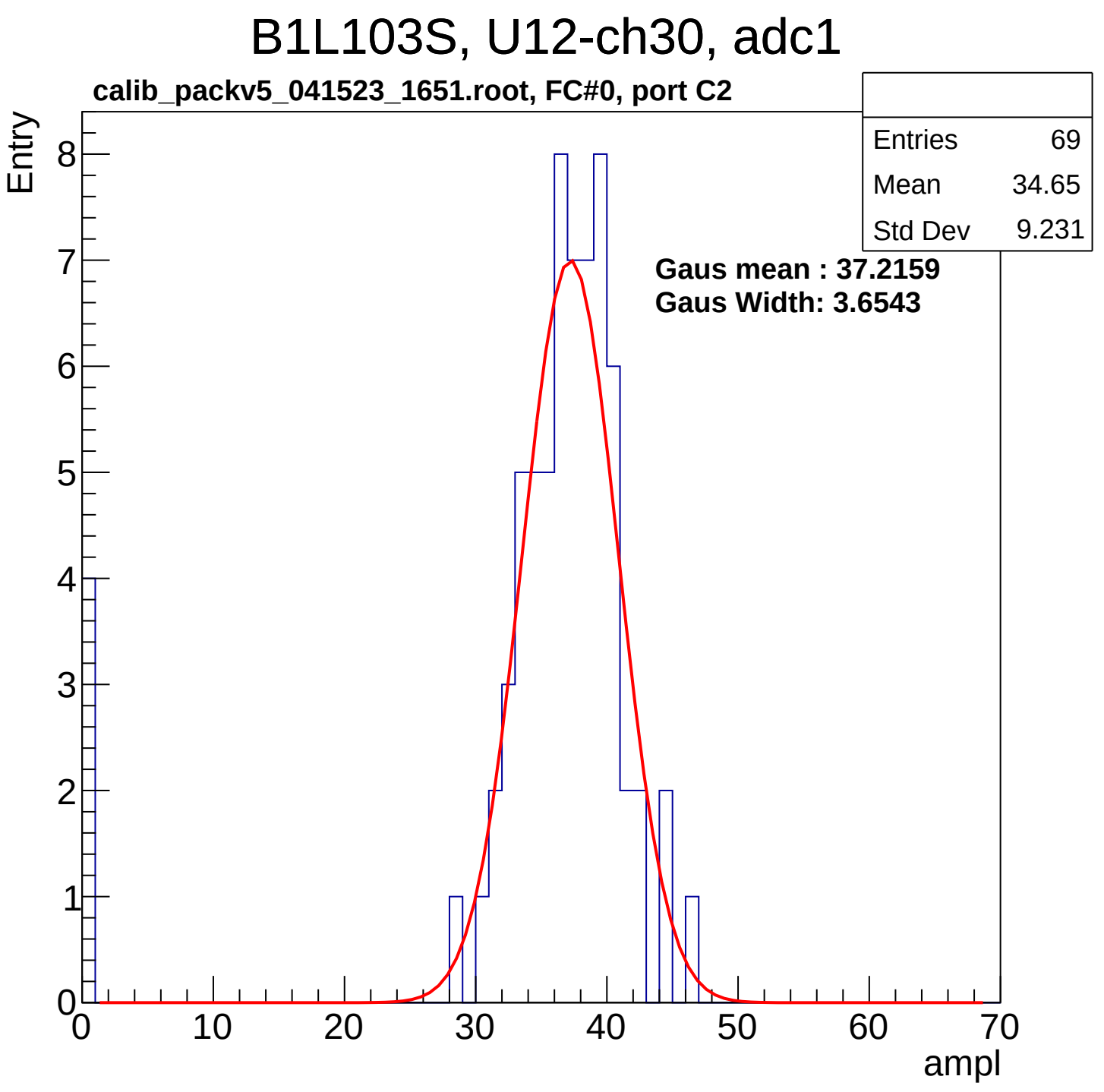
B1L103S, U12-ch30, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 34.65
Std Dev 9.231
Gaus mean : 37.2159
Gaus Width: 3.6543
Entry
ampl
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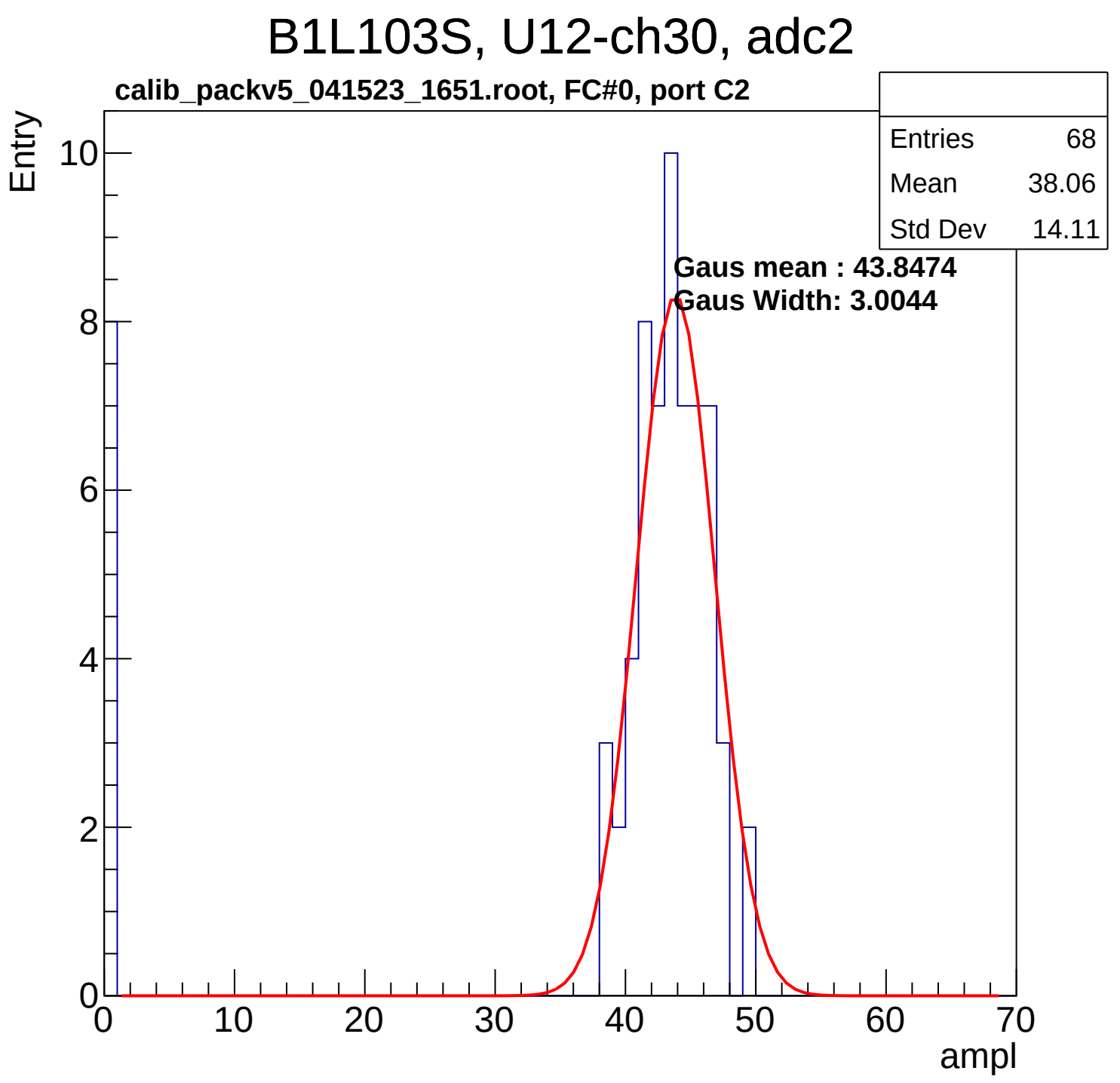
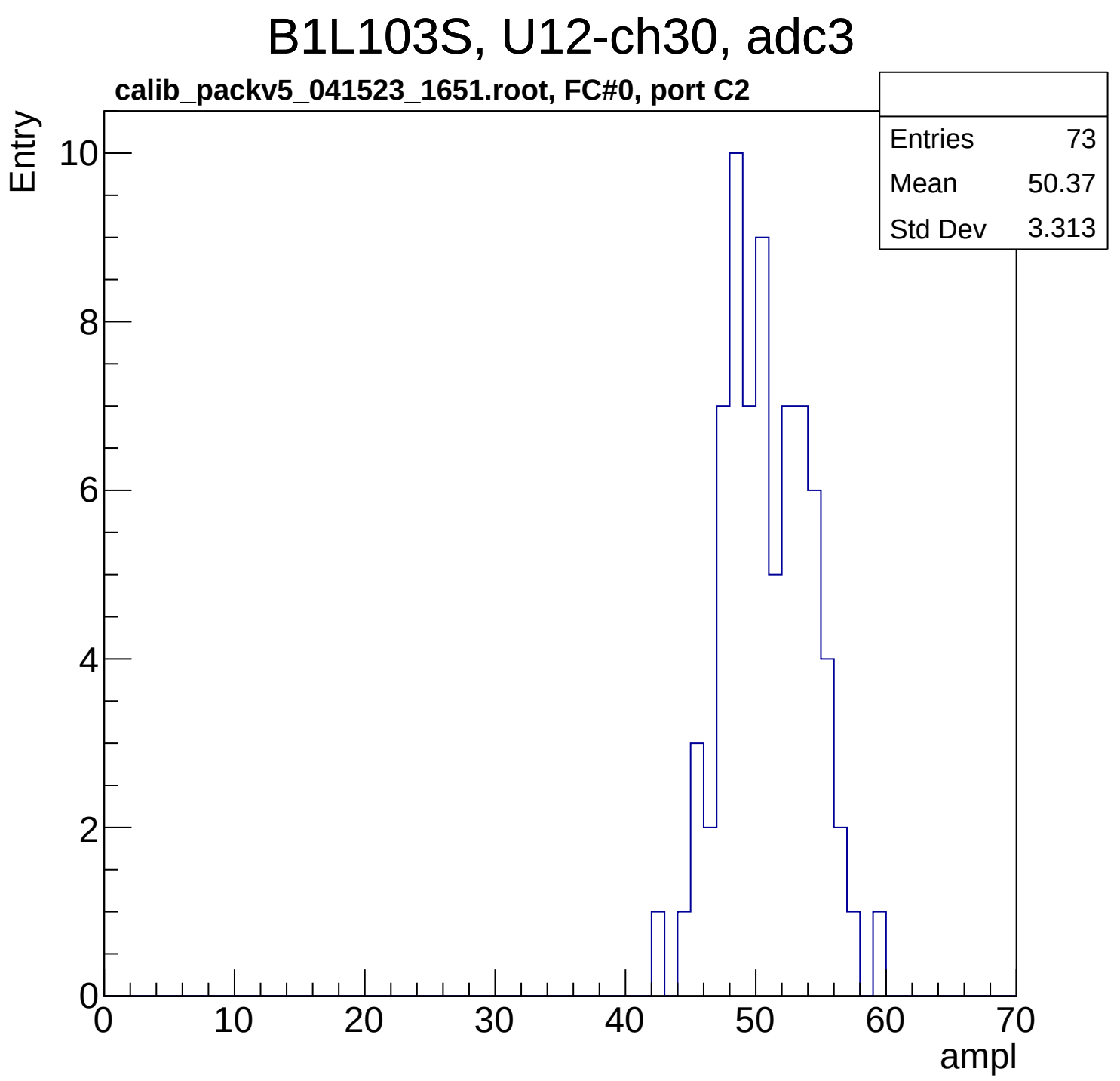
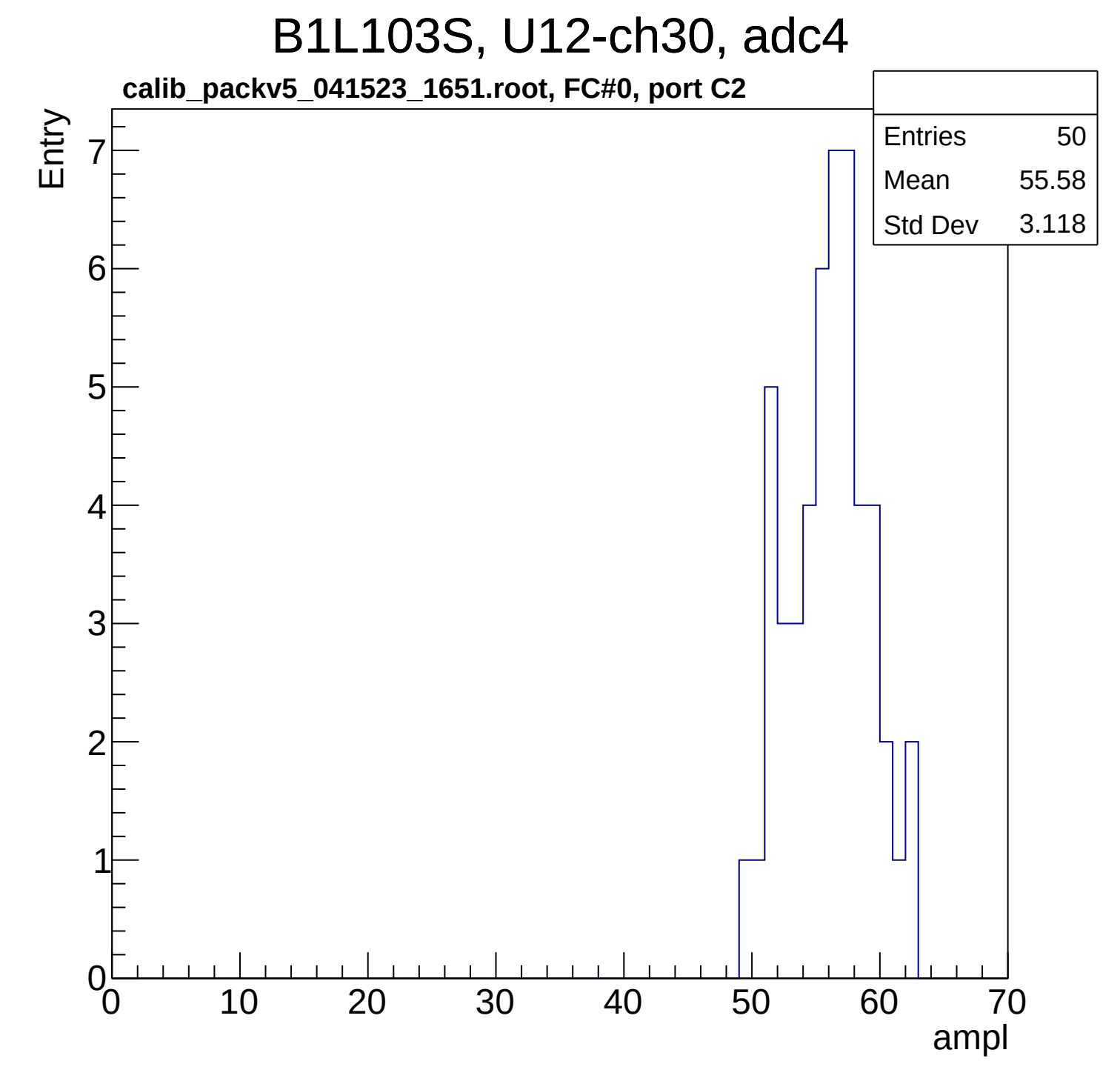
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U12-ch30, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 38.06
Std Dev 14.11
Gaus mean : 43.8474
Gaus Width: 3.0044
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch30, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 50.37
Std Dev 3.313
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch30, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 55.58
Std Dev 3.118
Entry
ampl
0
1
2
3
4
5
6
7
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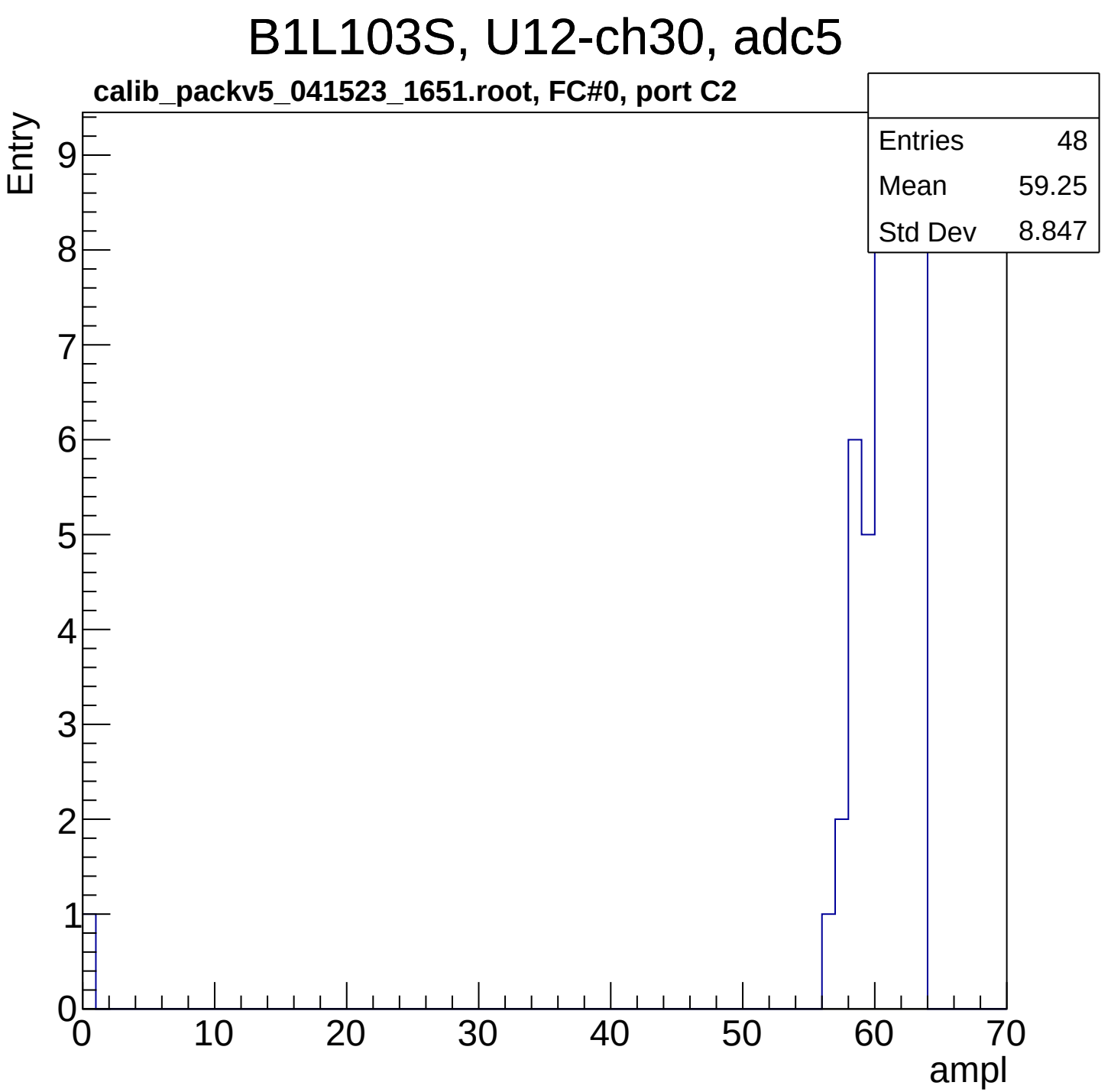
B1L103S, U12-ch30, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 59.25
Std Dev 8.847
Entry
ampl
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10
20
30
40
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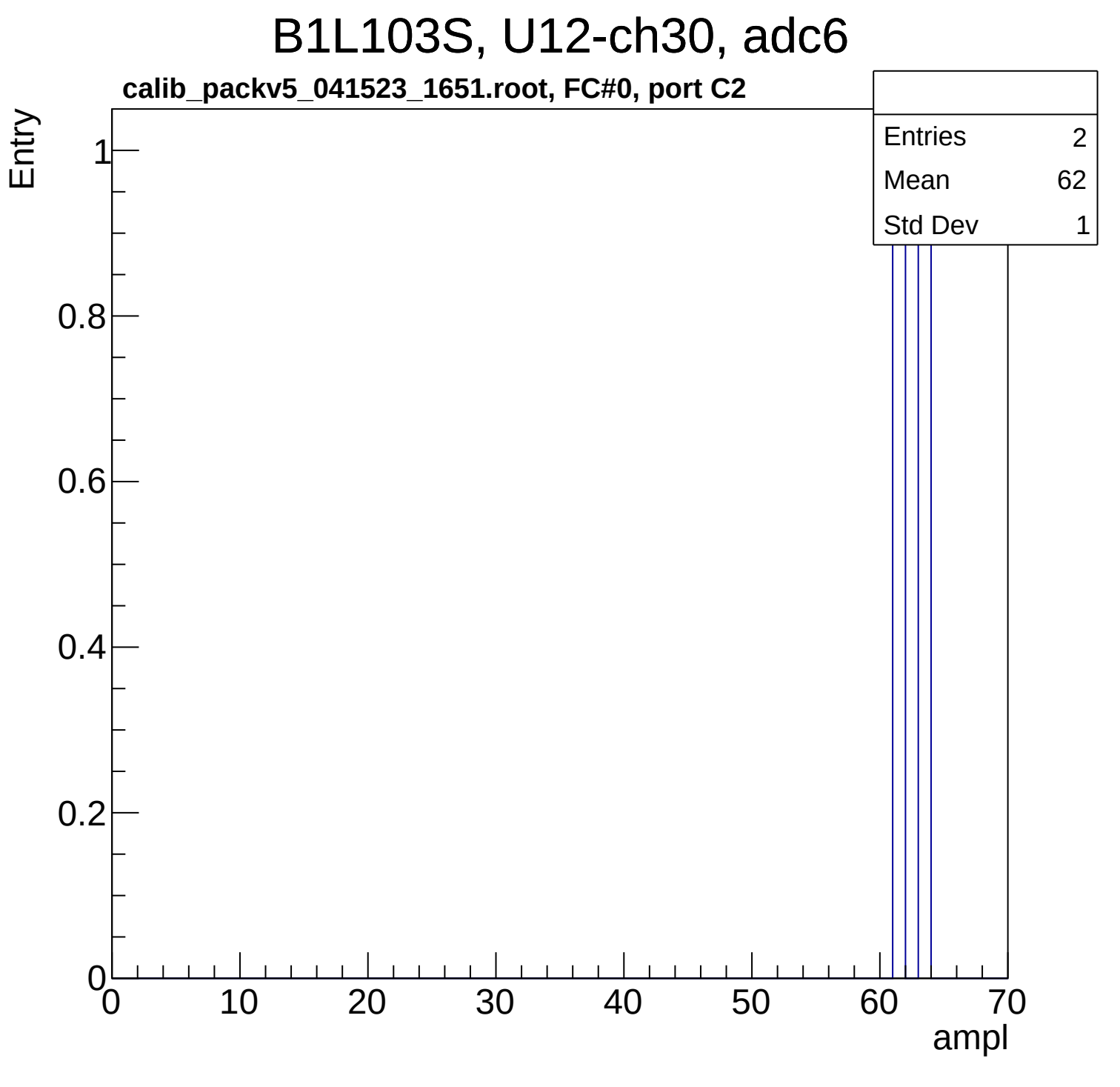
1
2
3
4
5
6
7
8
9


B1L103S, U12-ch30, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62
Std Dev 1
Entry
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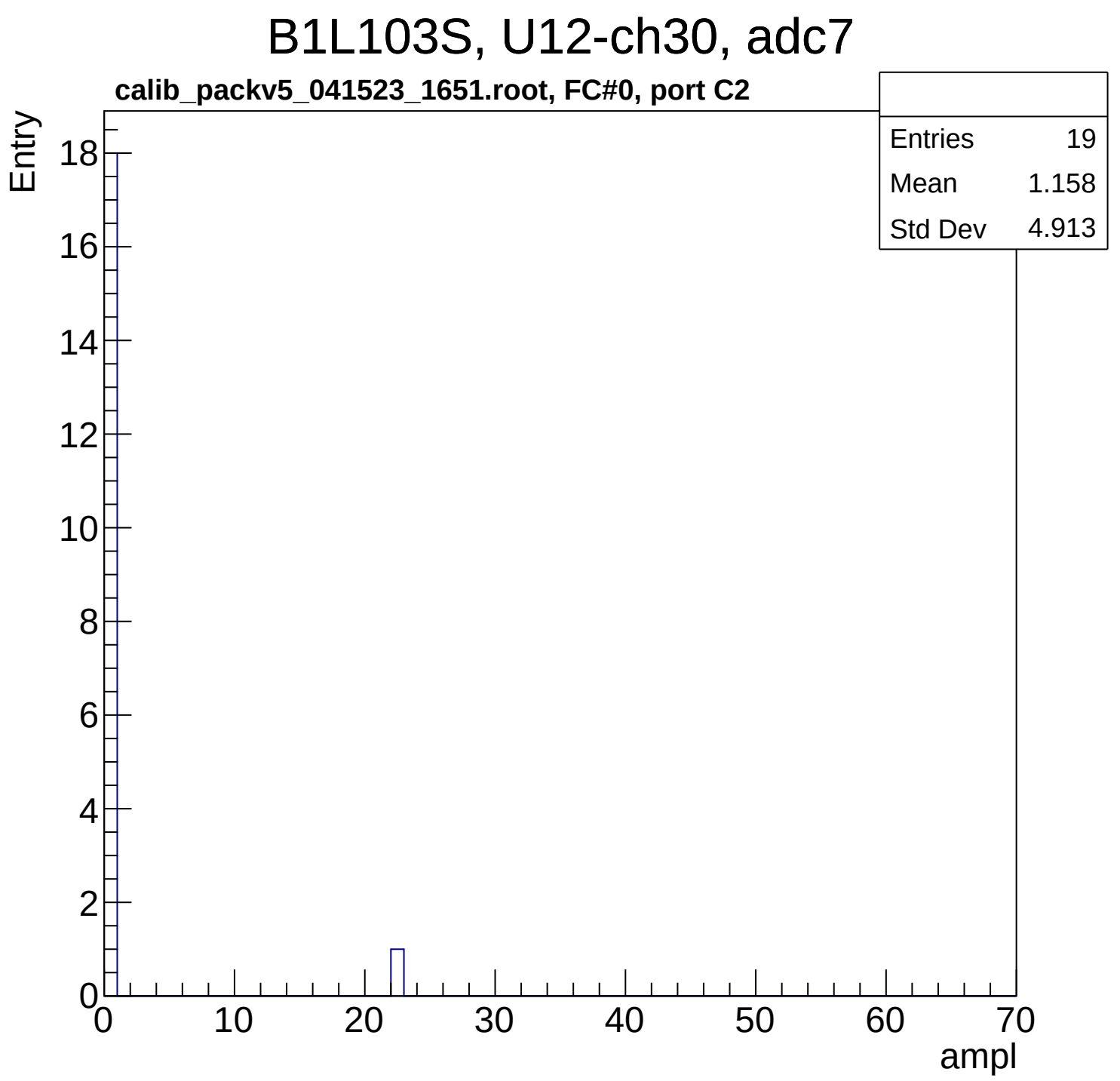
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch30, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.158
Std Dev 4.913
Entry
0
2
4
6
8
10
12
14
16
18
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10
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30
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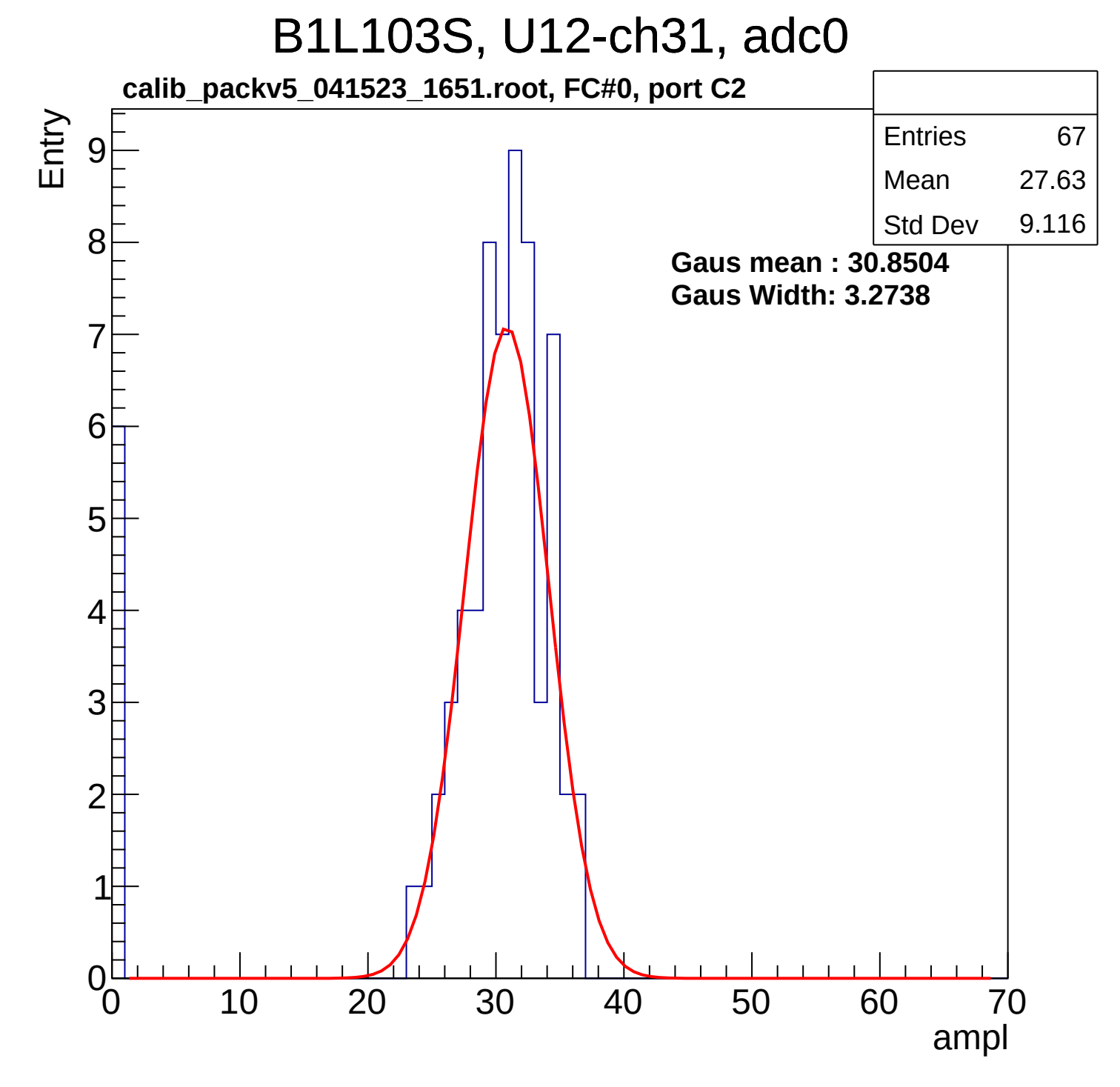
50
60
70
ampl


B1L103S, U12-ch31, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 27.63
Std Dev 9.116
Gaus mean : 30.8504
Gaus Width: 3.2738
Entry
ampl
0
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2
3
4
5
6
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0
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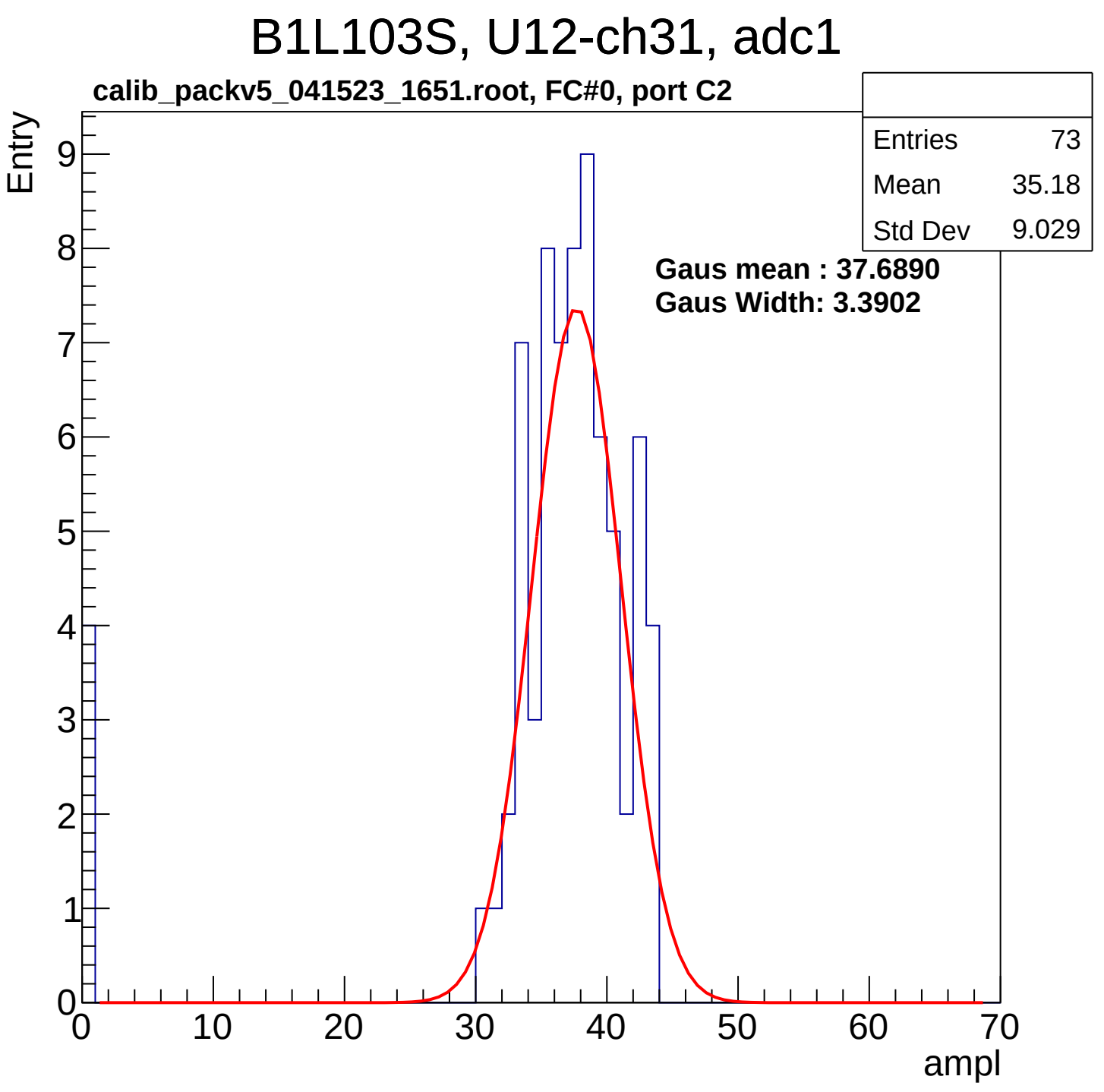
B1L103S, U12-ch31, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 35.18
Std Dev 9.029
Gaus mean : 37.6890
Gaus Width: 3.3902
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
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40
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60
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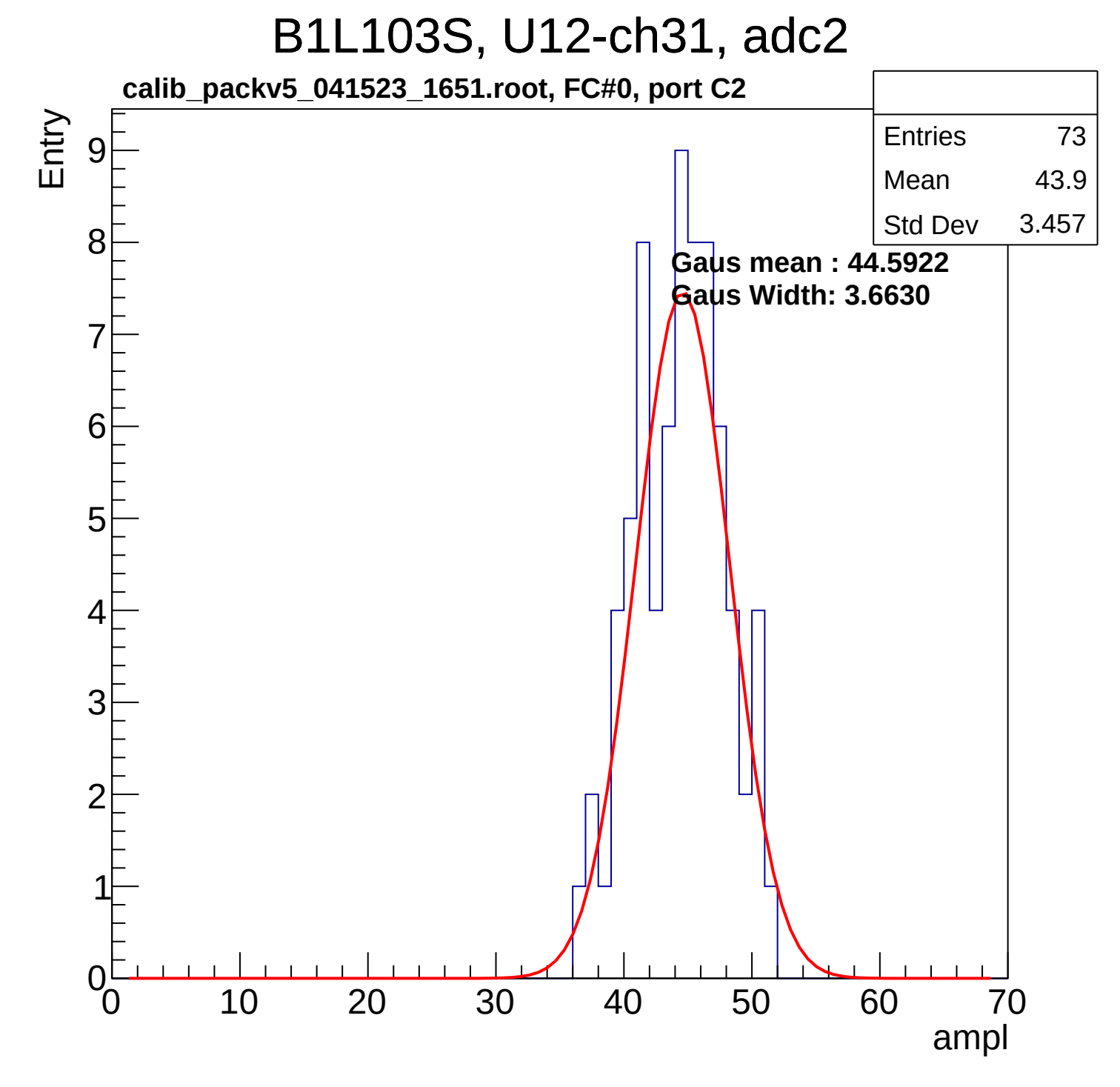
B1L103S, U12-ch31, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 43.9
Std Dev 3.457
Gaus mean : 44.5922
Gaus Width: 3.6630
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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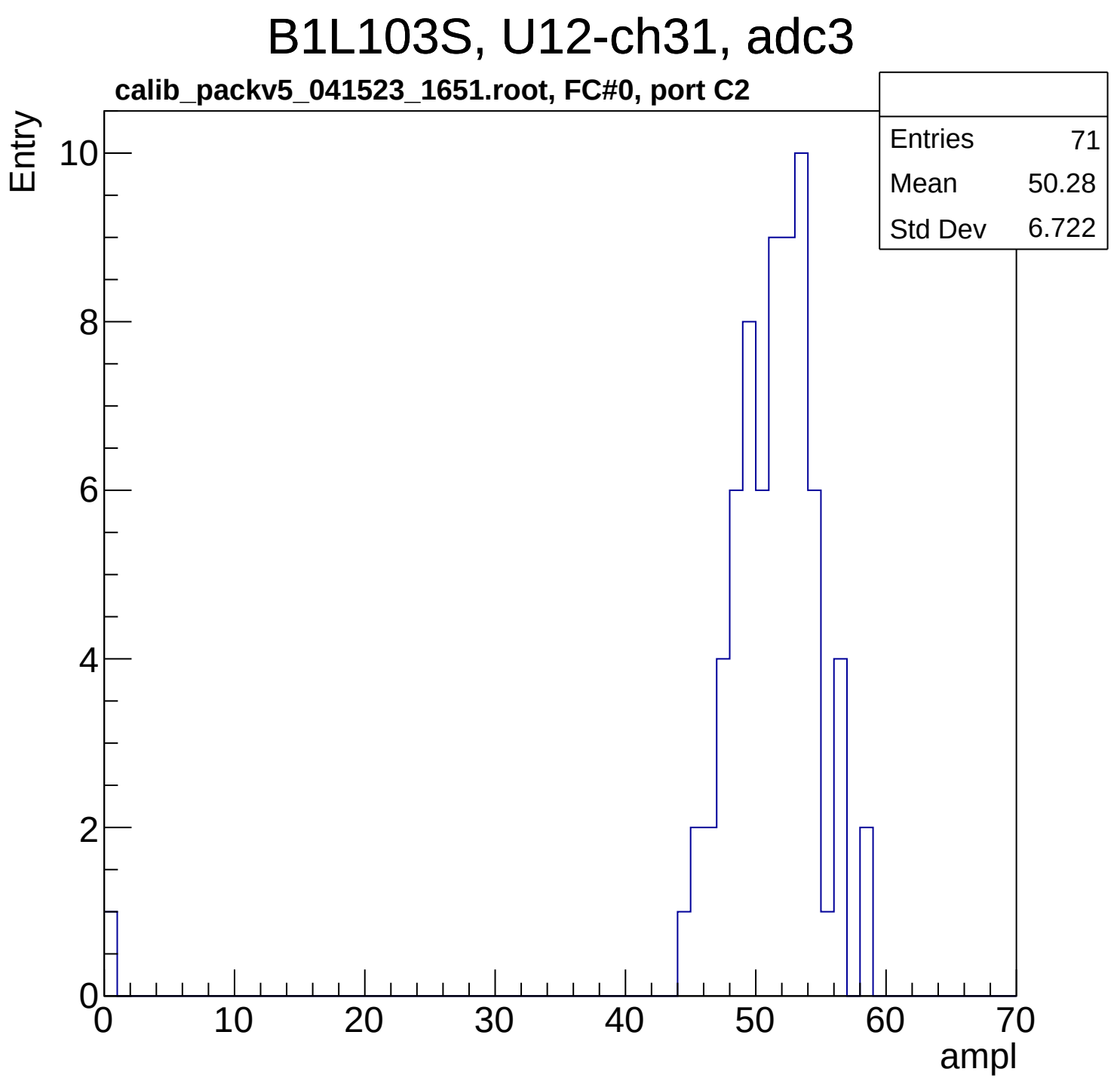
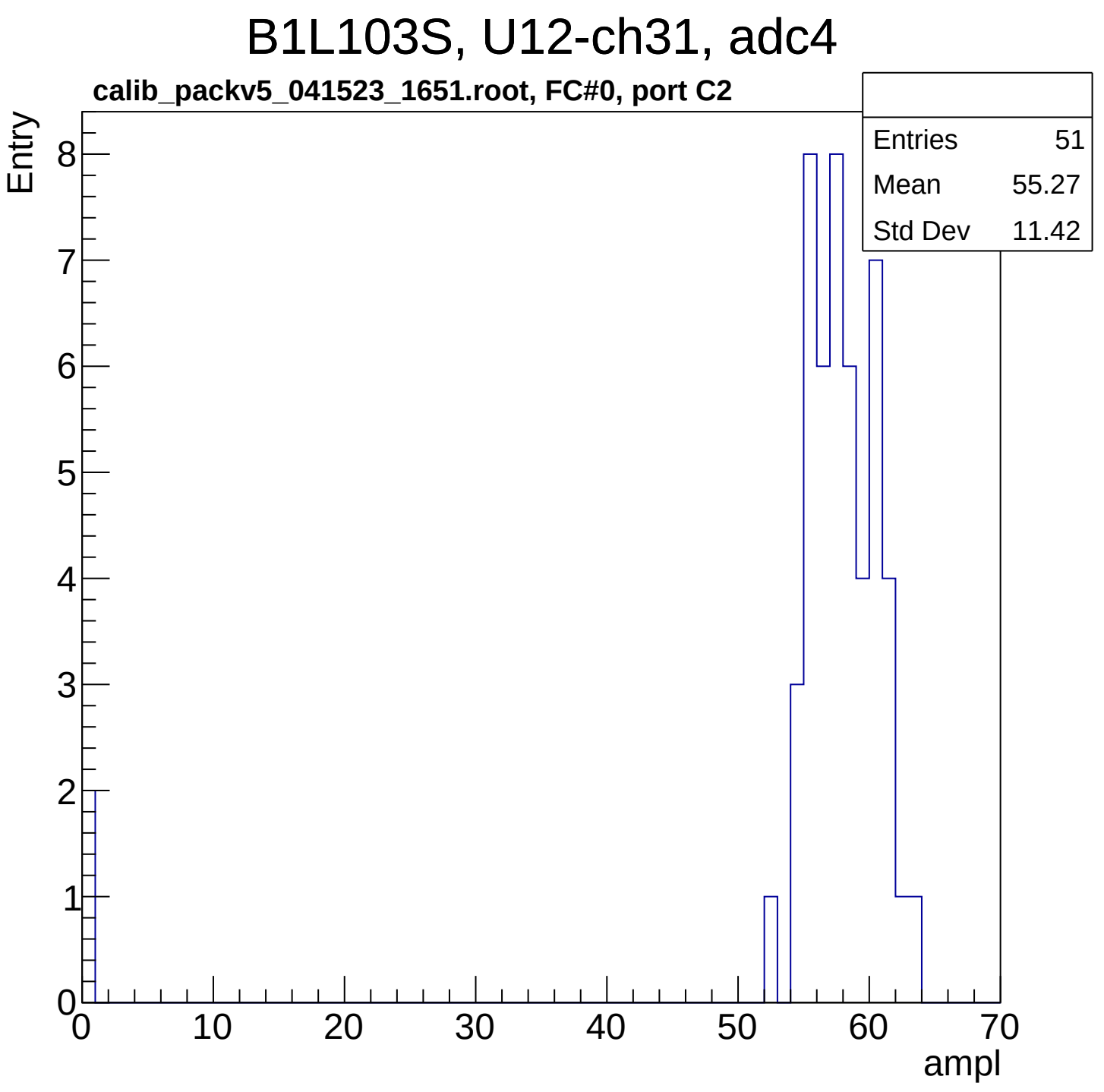

B1L103S, U12-ch31, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 50.28
Std Dev 6.722
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch31, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 55.27
Std Dev 11.42
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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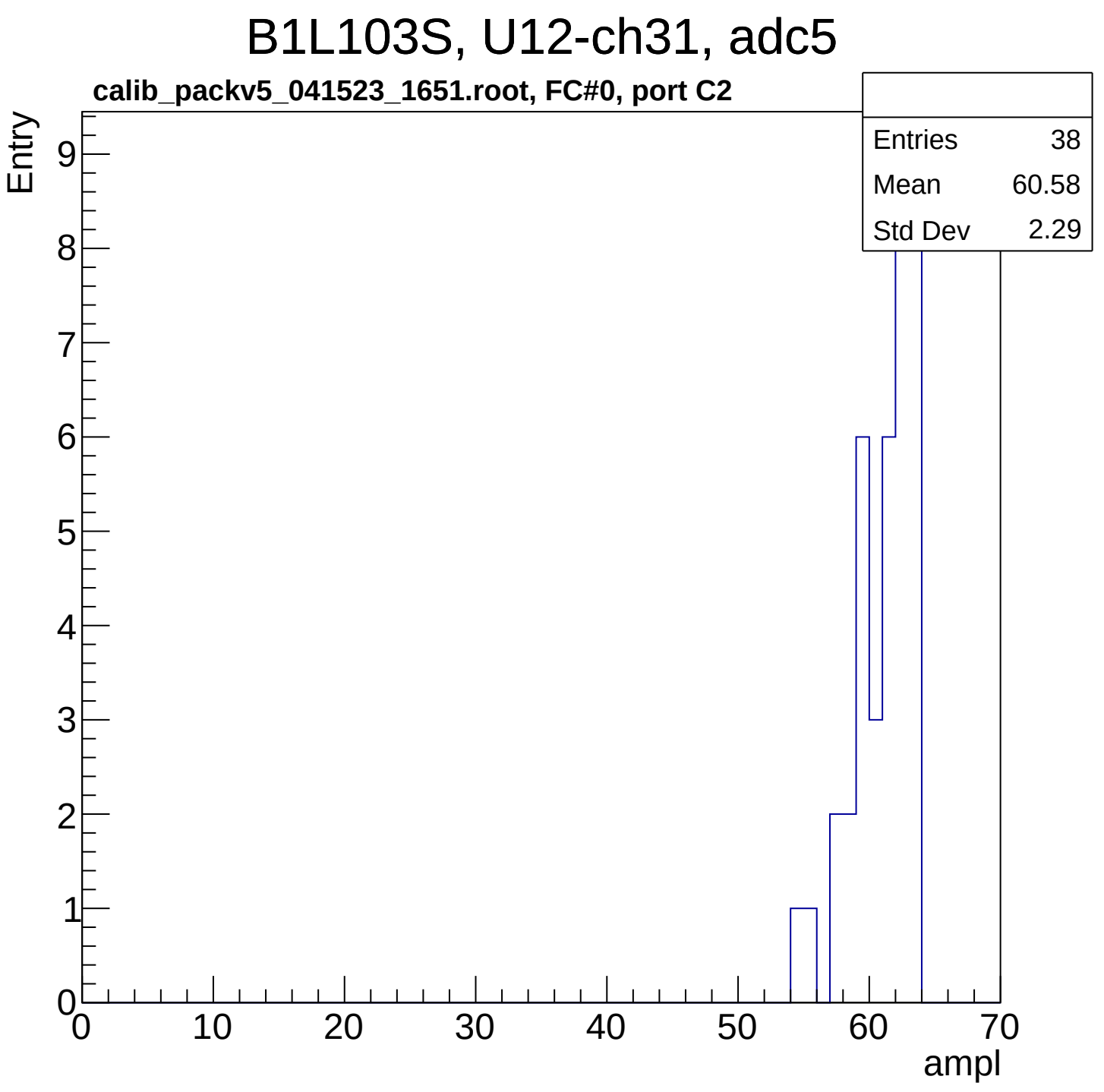
B1L103S, U12-ch31, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 60.58
Std Dev 2.29
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
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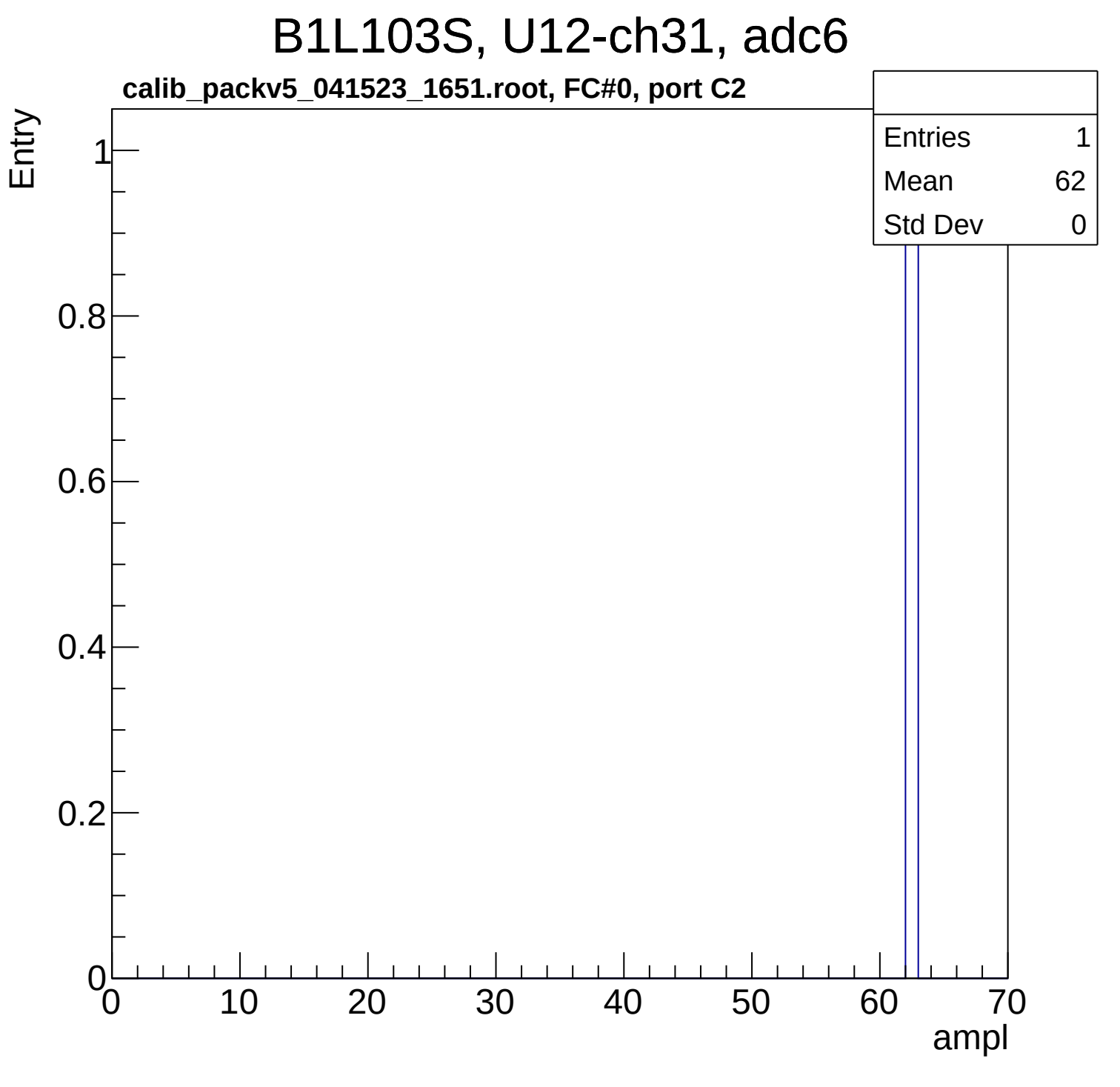
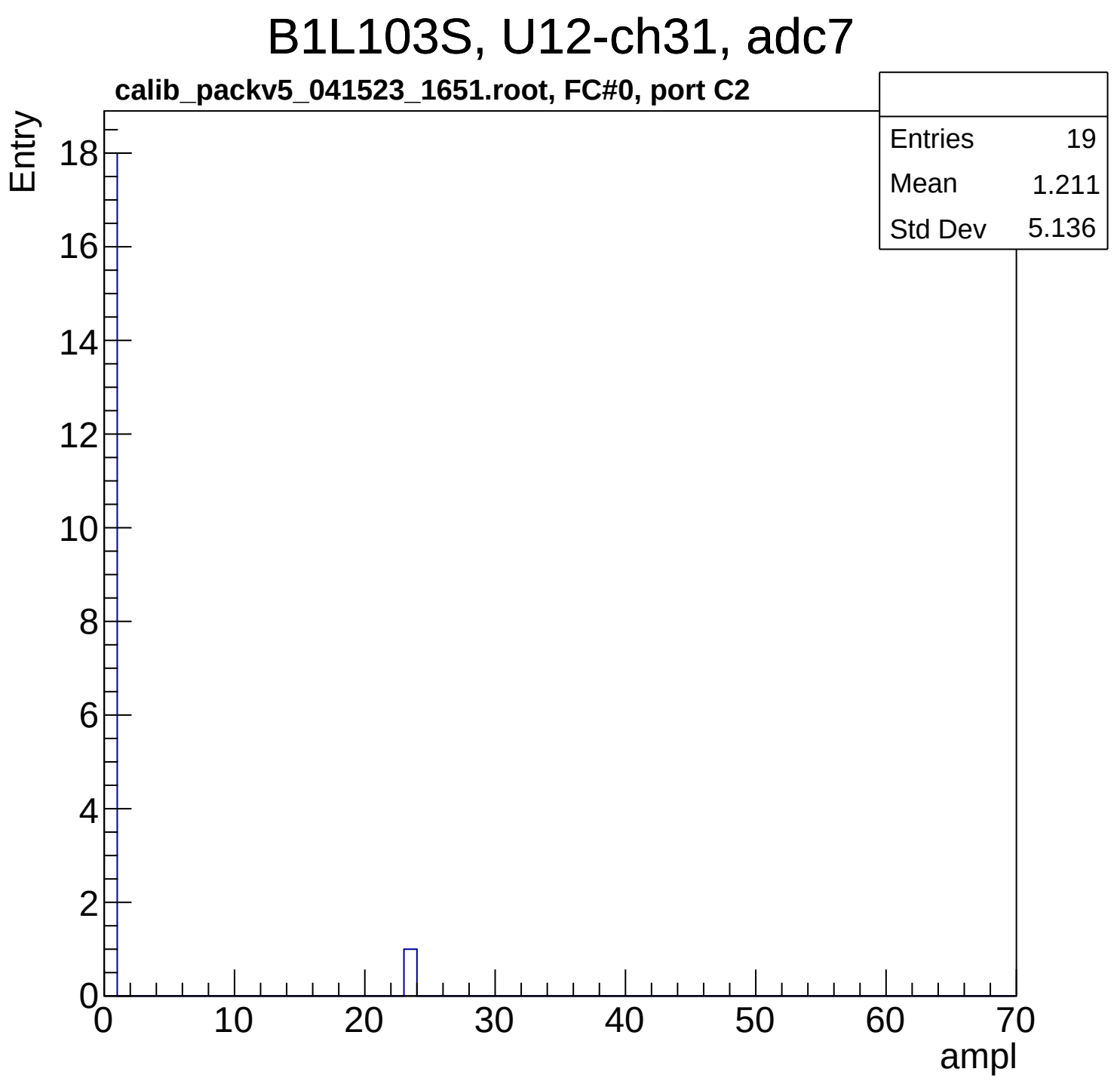

B1L103S, U12-ch31, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch31, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.211
Std Dev 5.136
Entry
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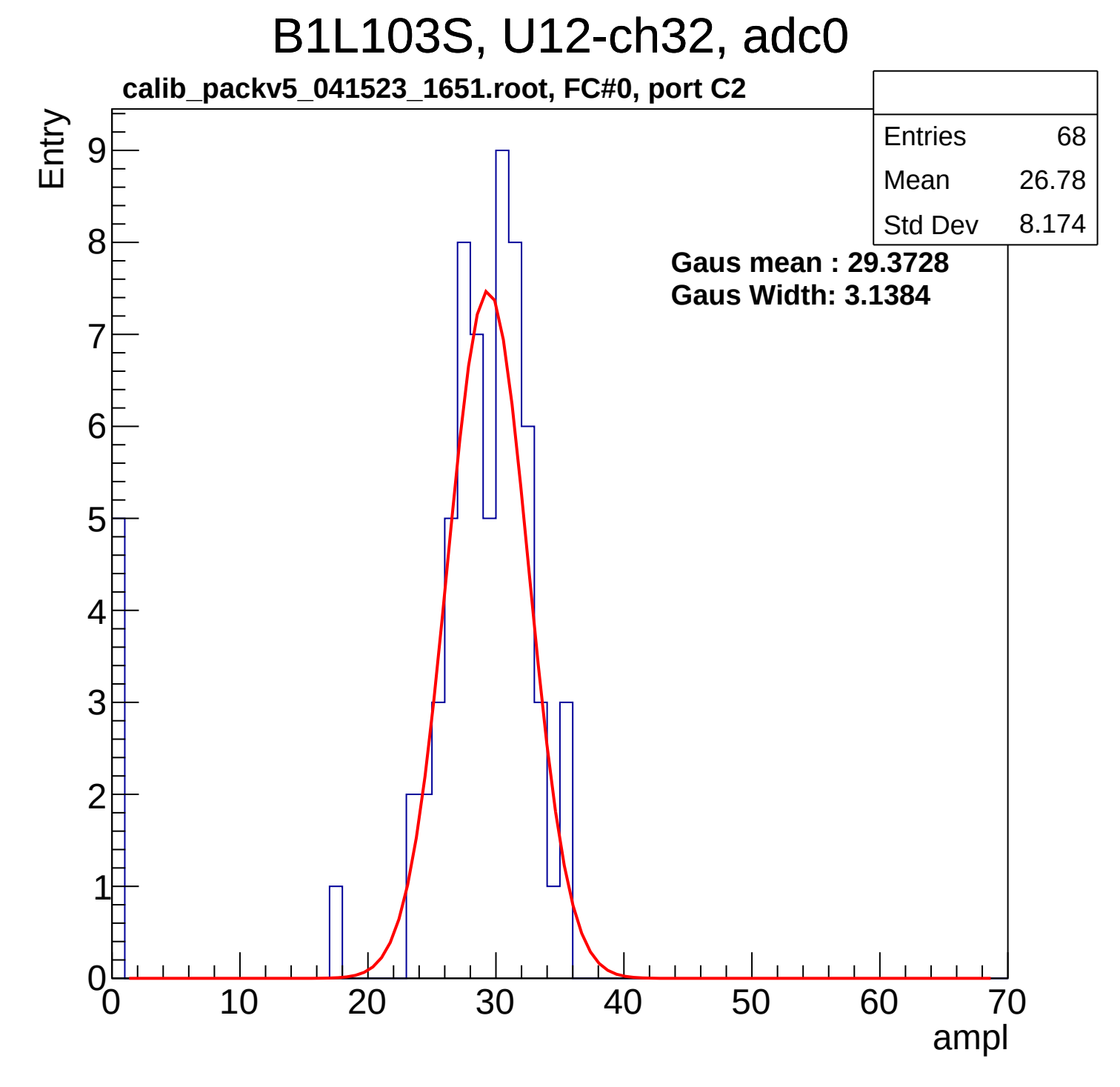
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch32, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 26.78
Std Dev 8.174
Gaus mean : 29.3728
Gaus Width: 3.1384
Entry
ampl
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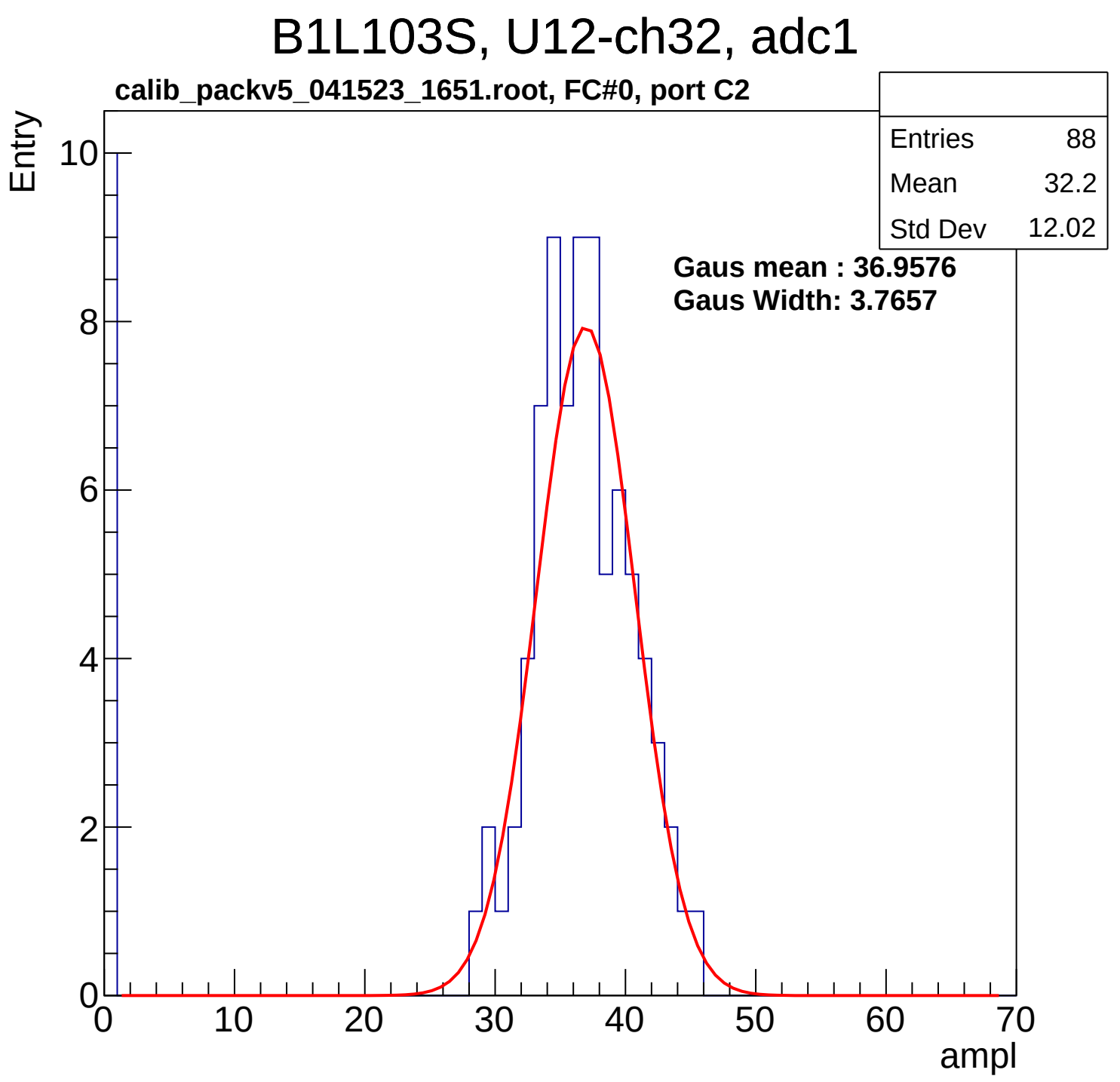
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch32, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 32.2
Std Dev 12.02
Gaus mean : 36.9576
Gaus Width: 3.7657
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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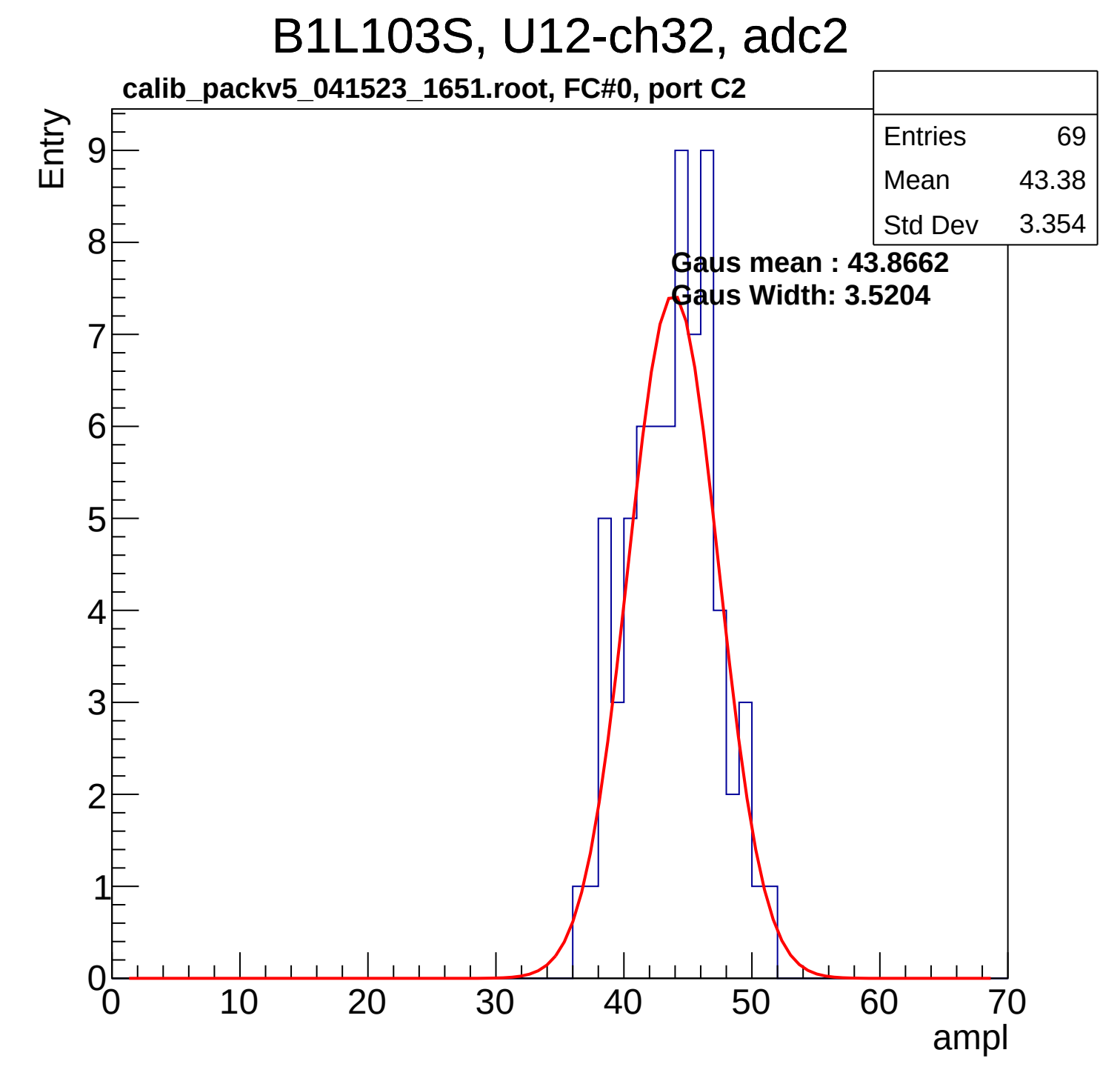
B1L103S, U12-ch32, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 43.38
Std Dev 3.354
Gaus mean : 43.8662
Gaus Width: 3.5204
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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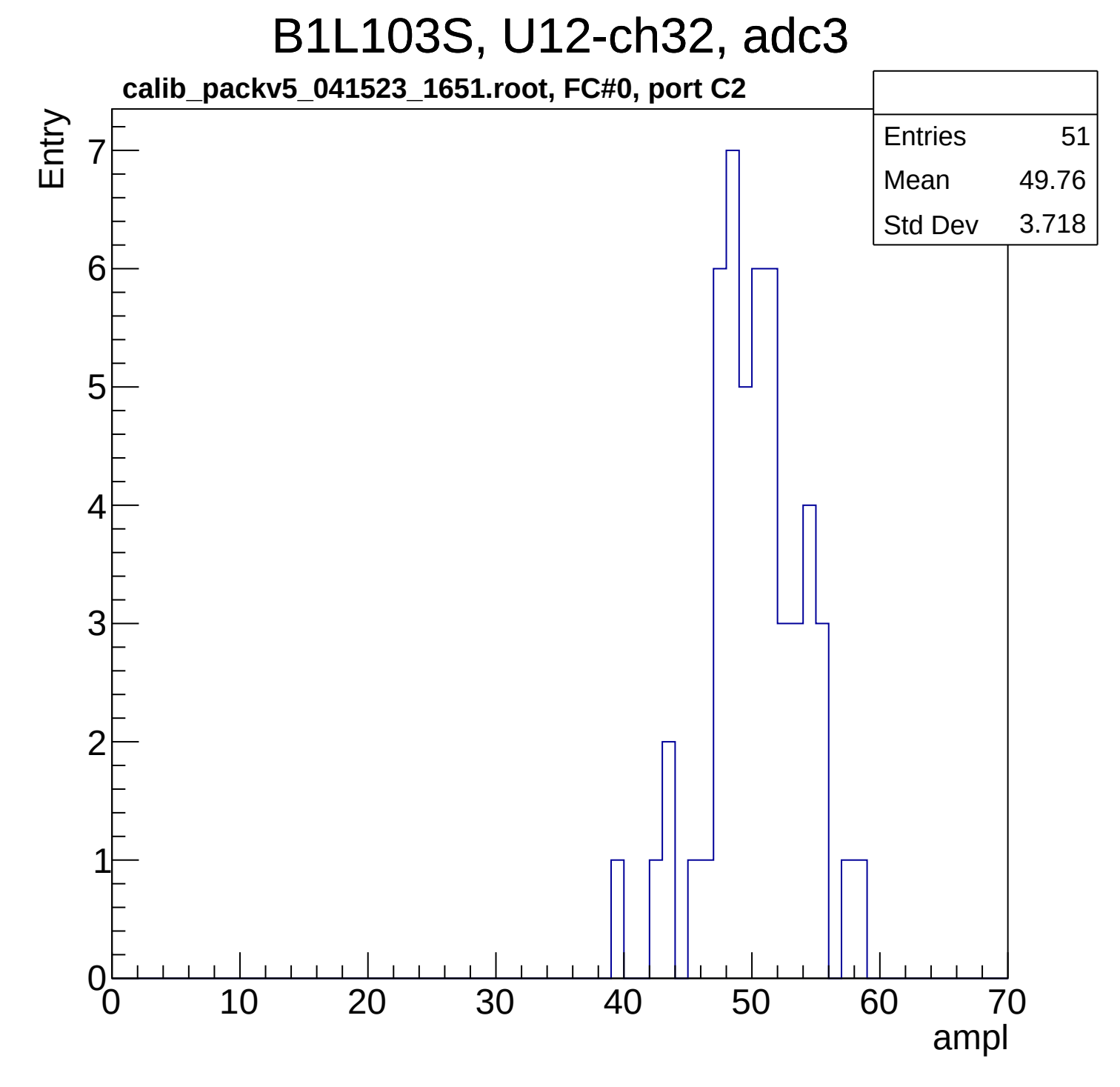
B1L103S, U12-ch32, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 49.76
Std Dev 3.718
Entry
ampl
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1
2
3
4
5
6
7
0
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60
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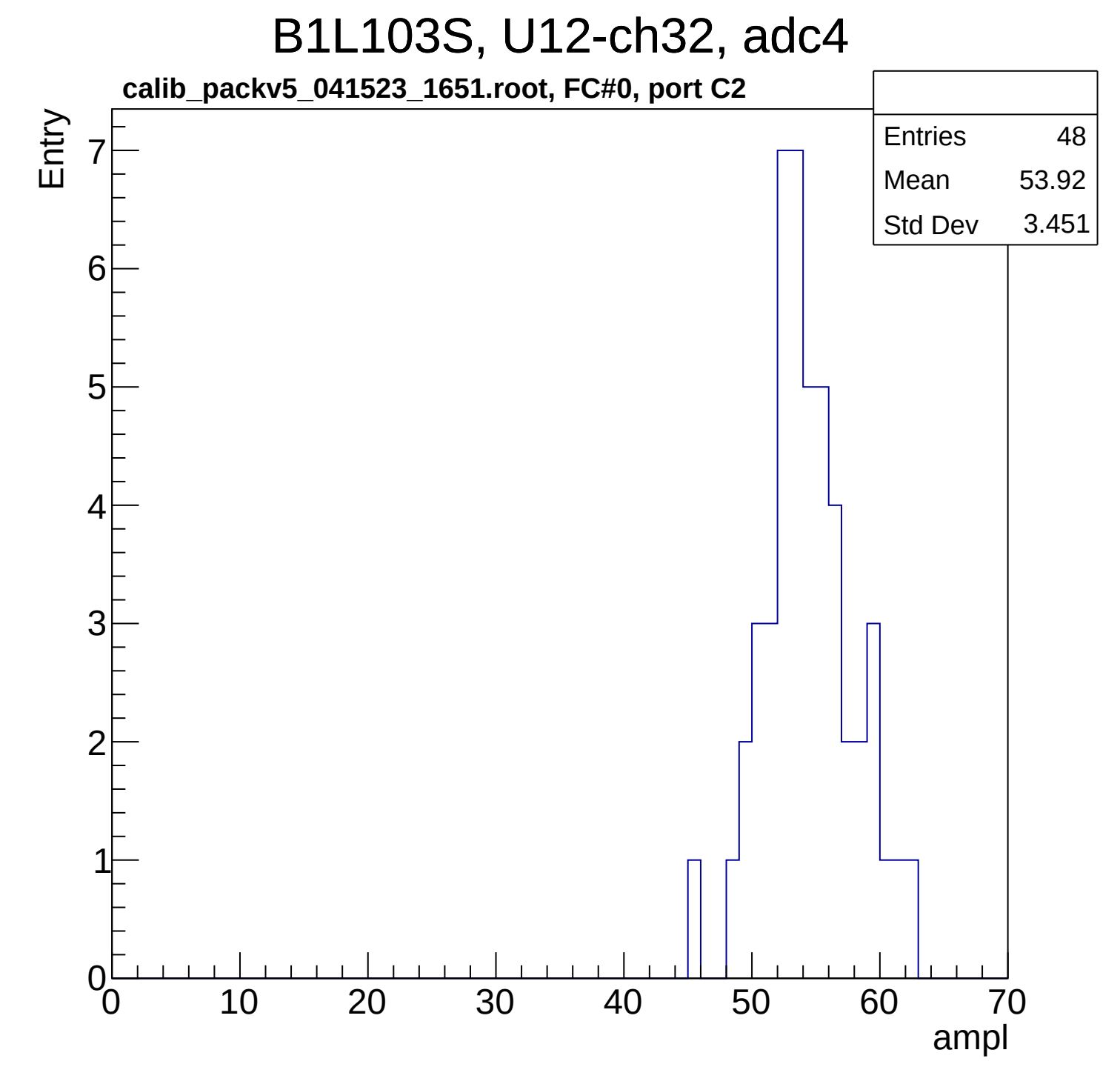
B1L103S, U12-ch32, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 53.92
Std Dev 3.451
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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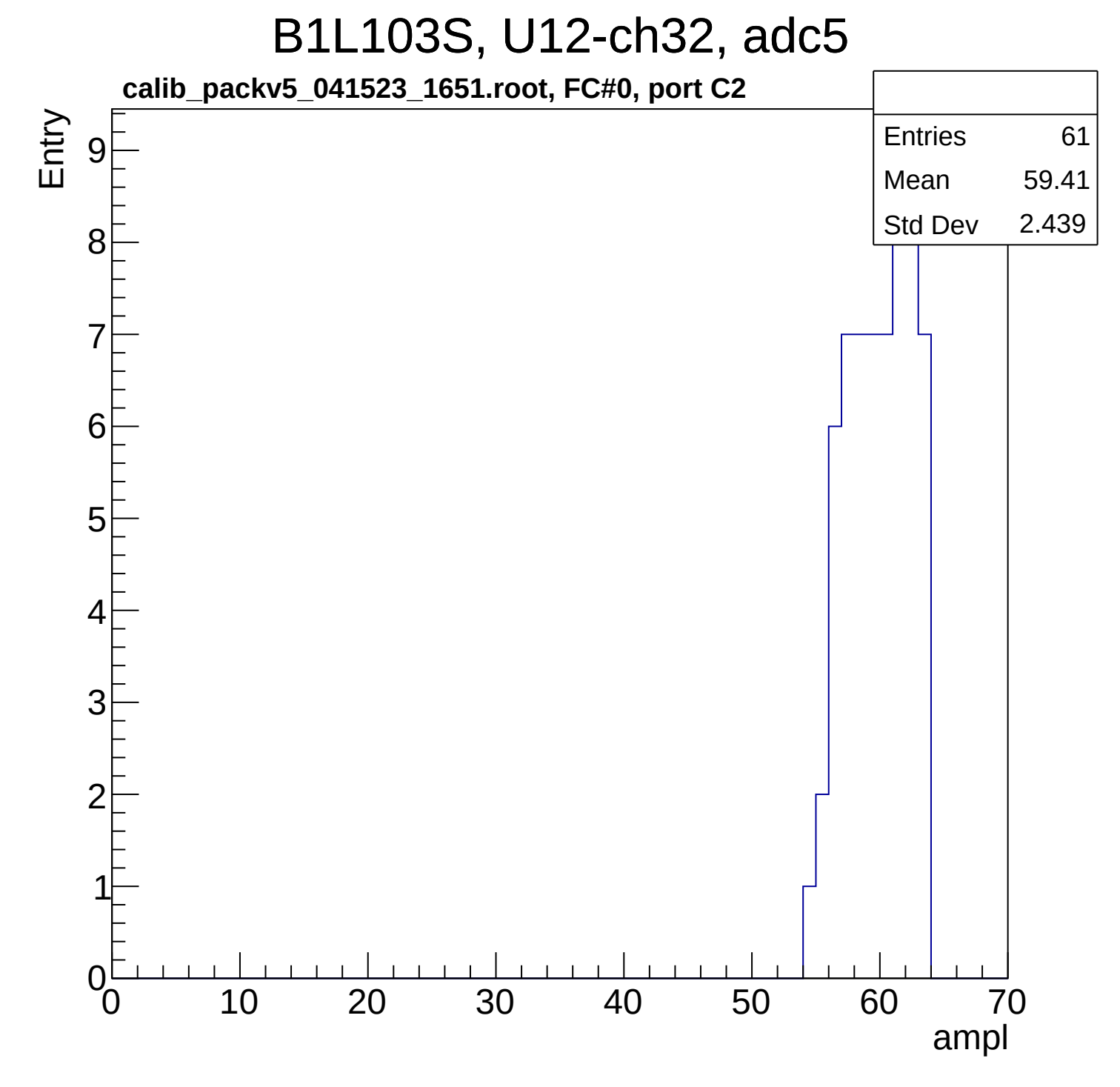
B1L103S, U12-ch32, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 59.41
Std Dev 2.439
Entry
ampl
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3
4
5
6
7
8
9
0
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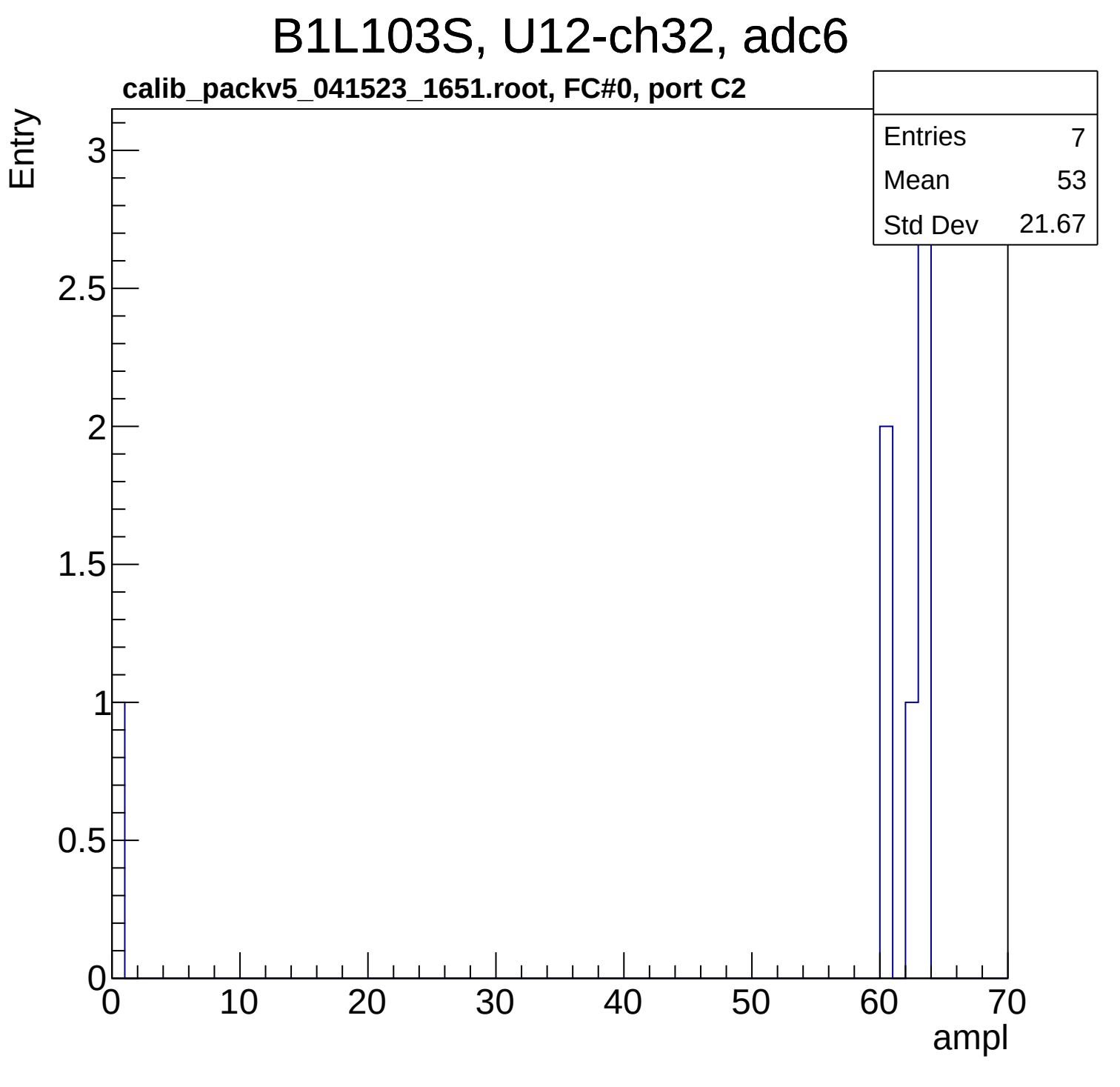
B1L103S, U12-ch32, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 53
Std Dev 21.67
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
50
60
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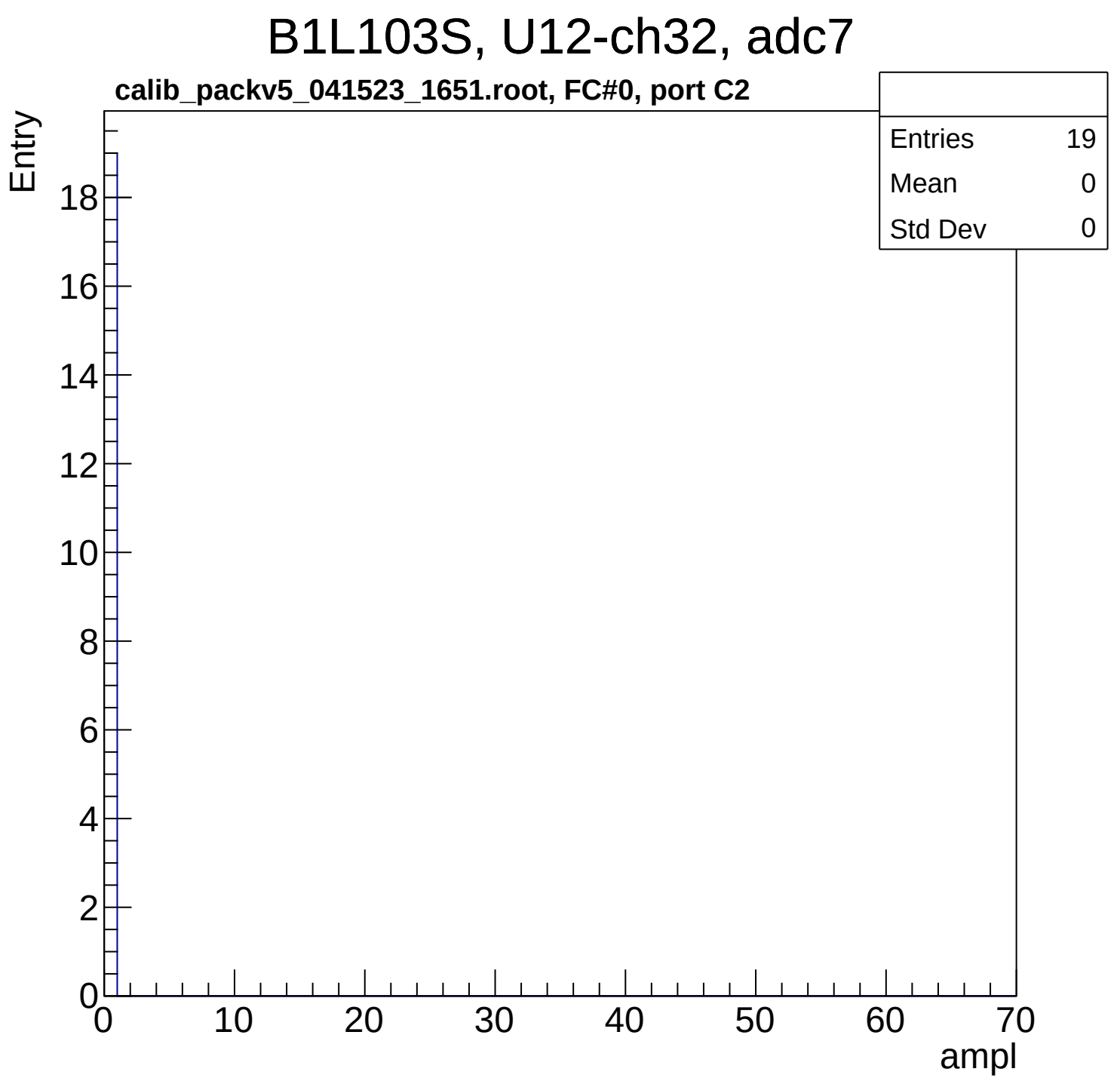
B1L103S, U12-ch32, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
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6
8
10
12
14
16
18
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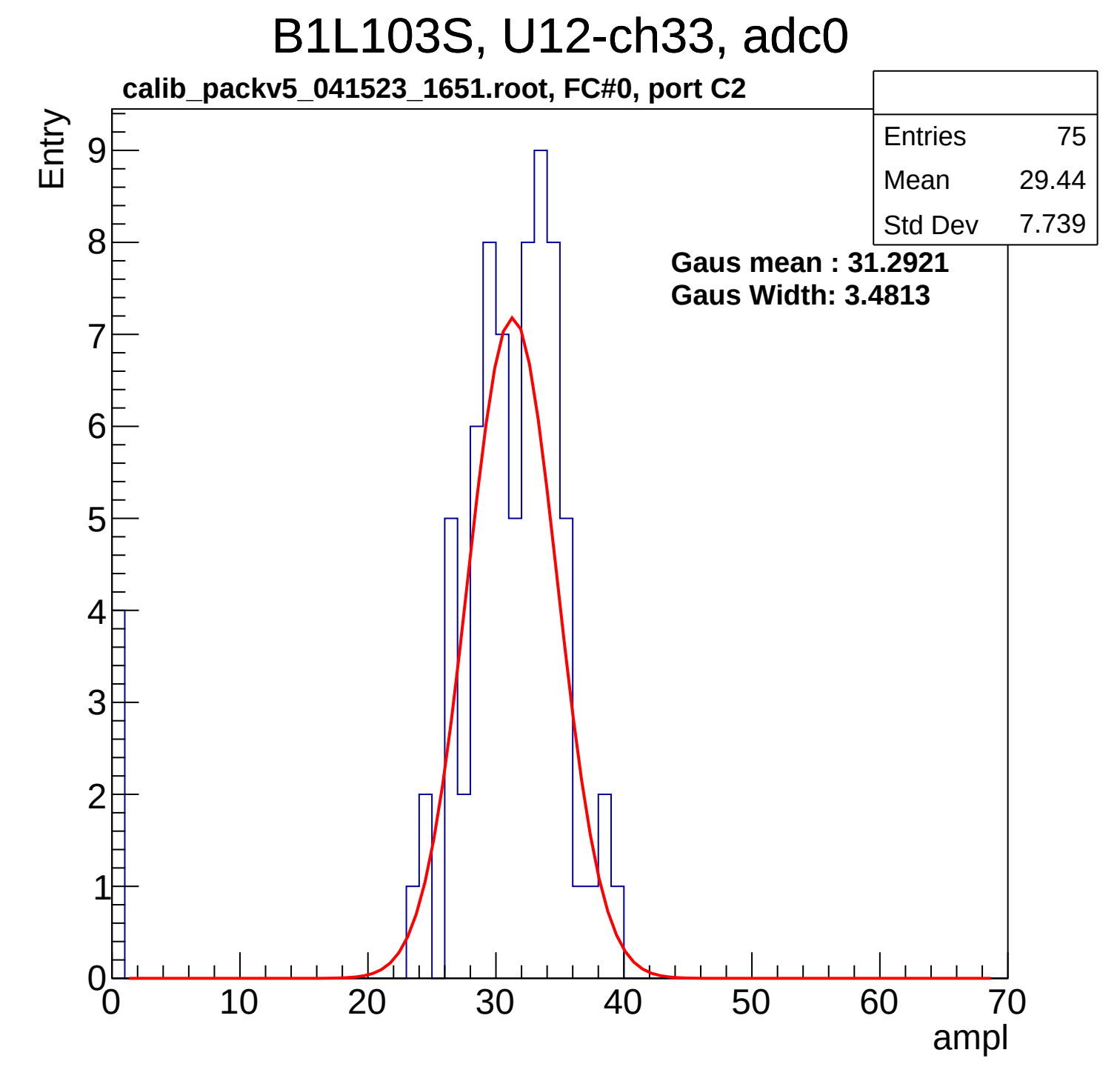
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch33, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 29.44
Std Dev 7.739
Gaus mean : 31.2921
Gaus Width: 3.4813
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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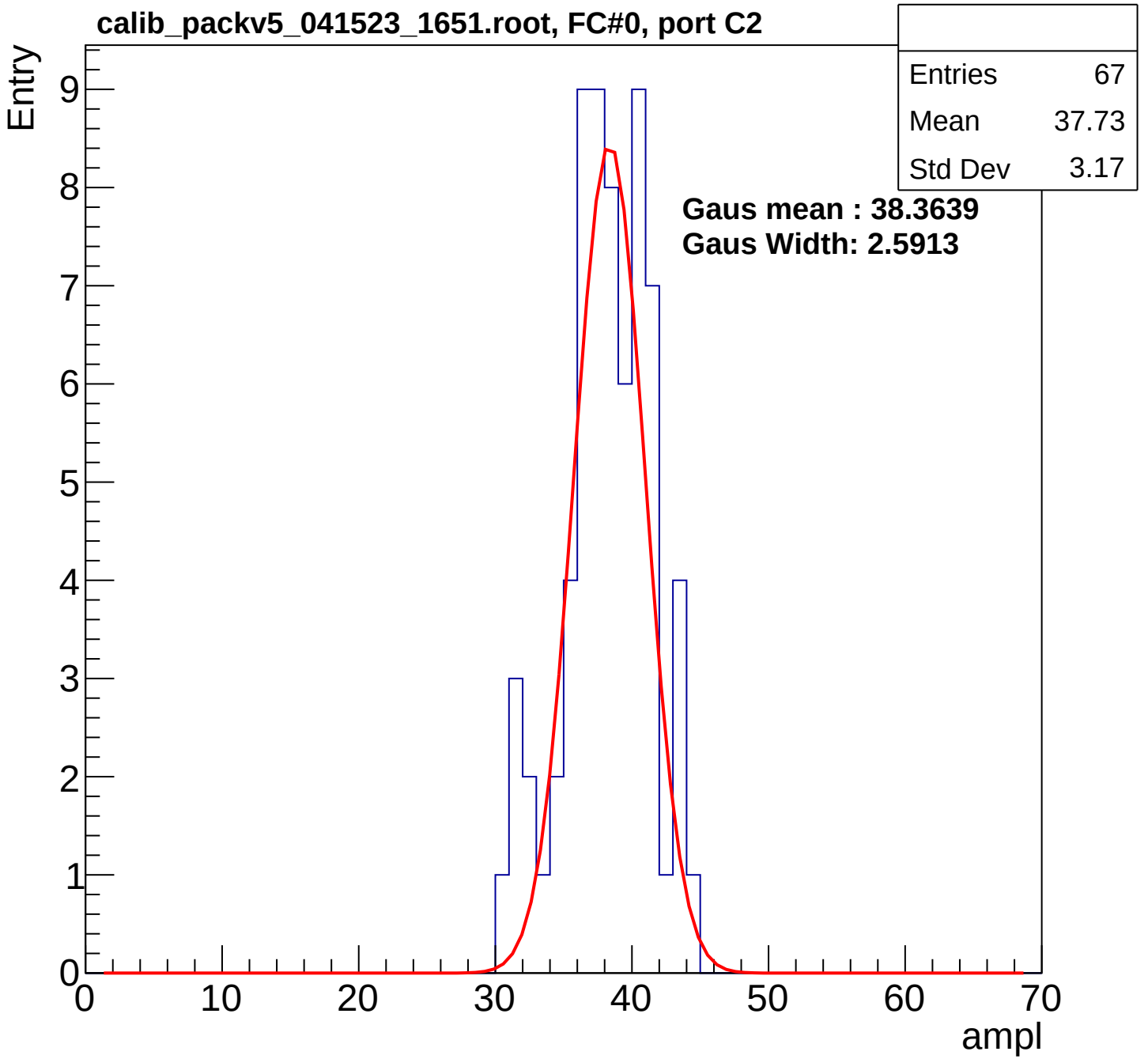
B1L103S, U12-ch33, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 37.73
Std Dev 3.17
Gaus mean : 38.3639
Gaus Width: 2.5913
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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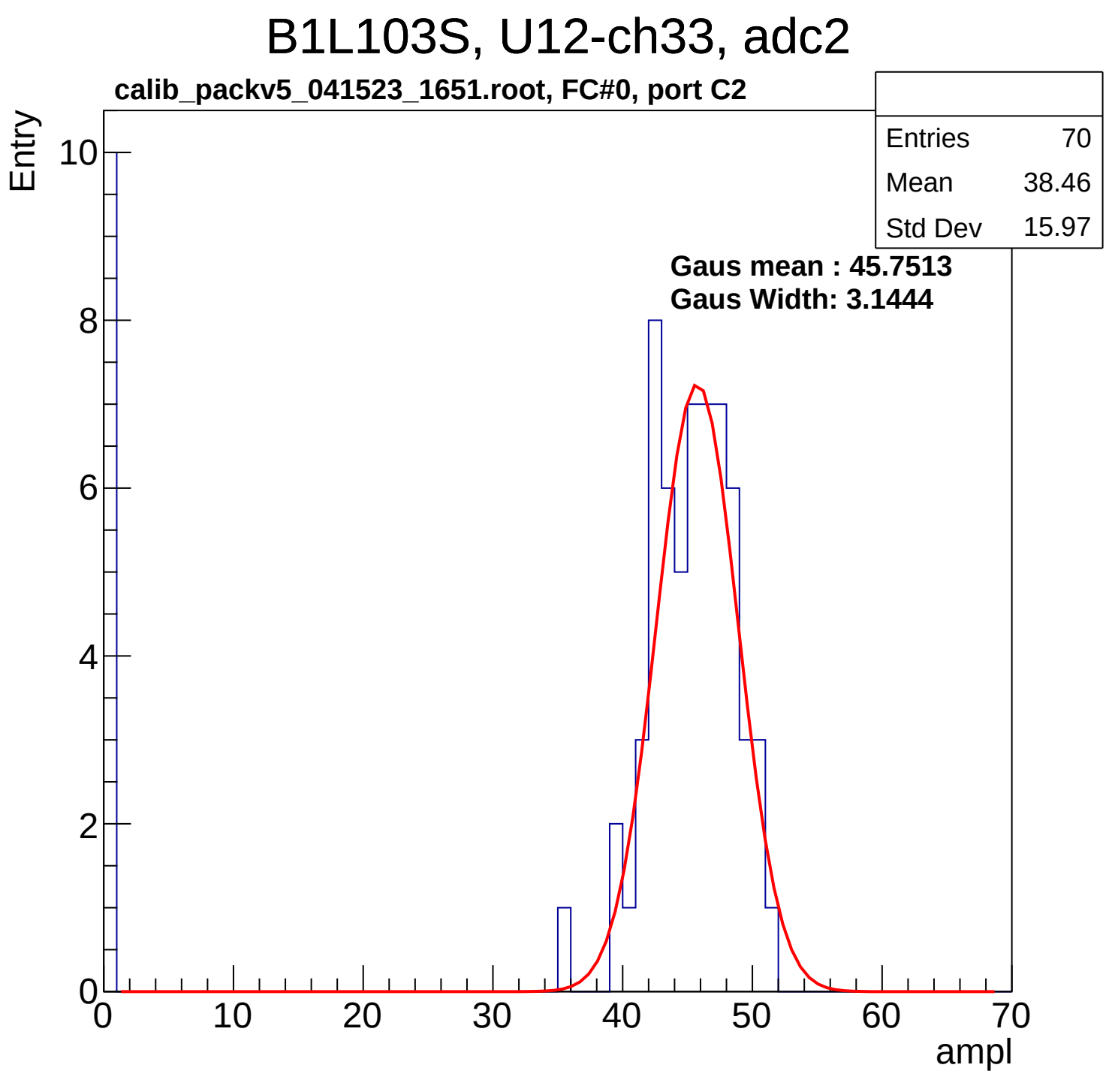
B1L103S, U12-ch33, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 38.46
Std Dev 15.97
Gaus mean : 45.7513
Gaus Width: 3.1444
Entry
ampl
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2
4
6
8
10
0
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40
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60
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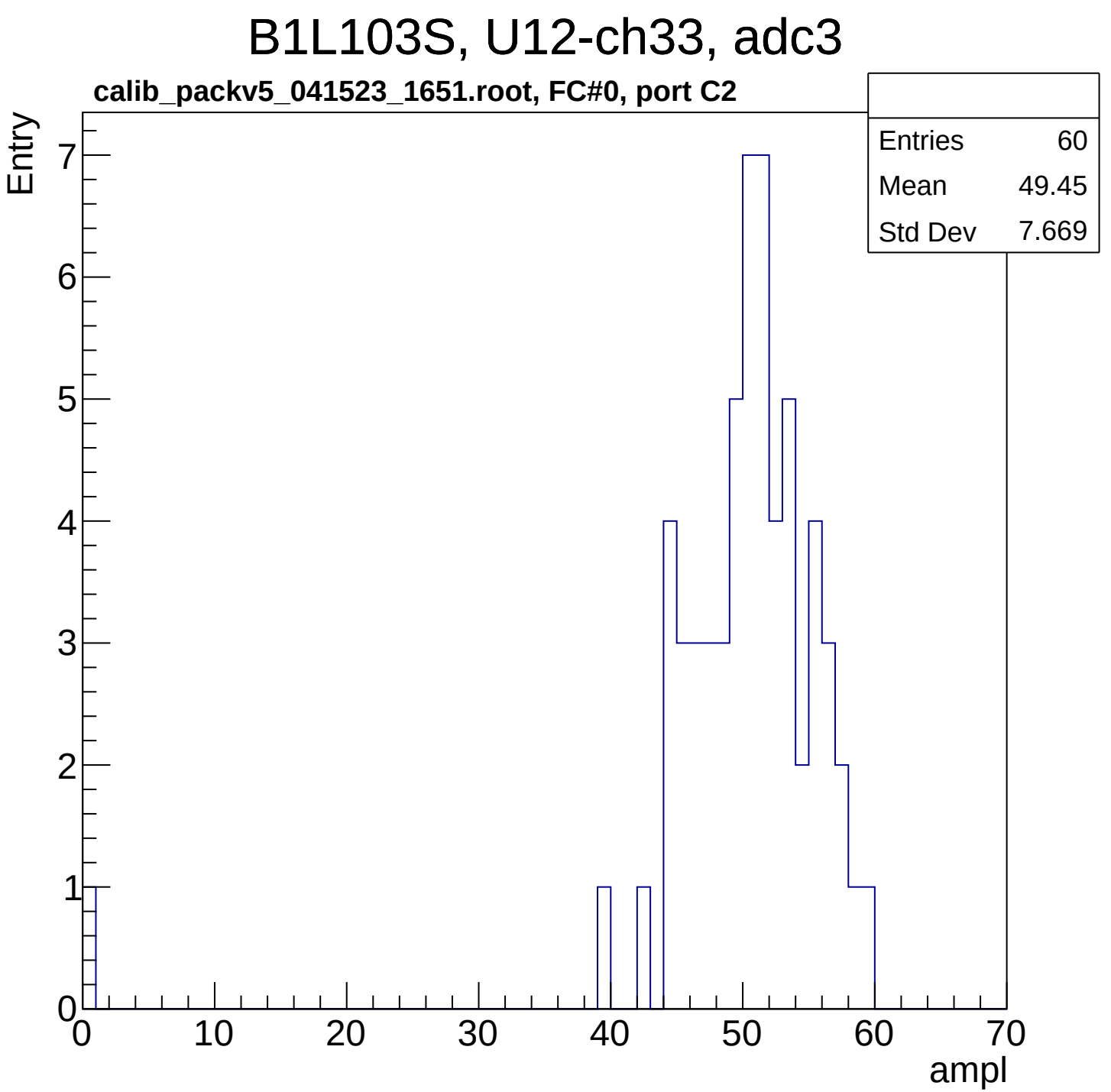
B1L103S, U12-ch33, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 49.45
Std Dev 7.669
Entry
ampl
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60
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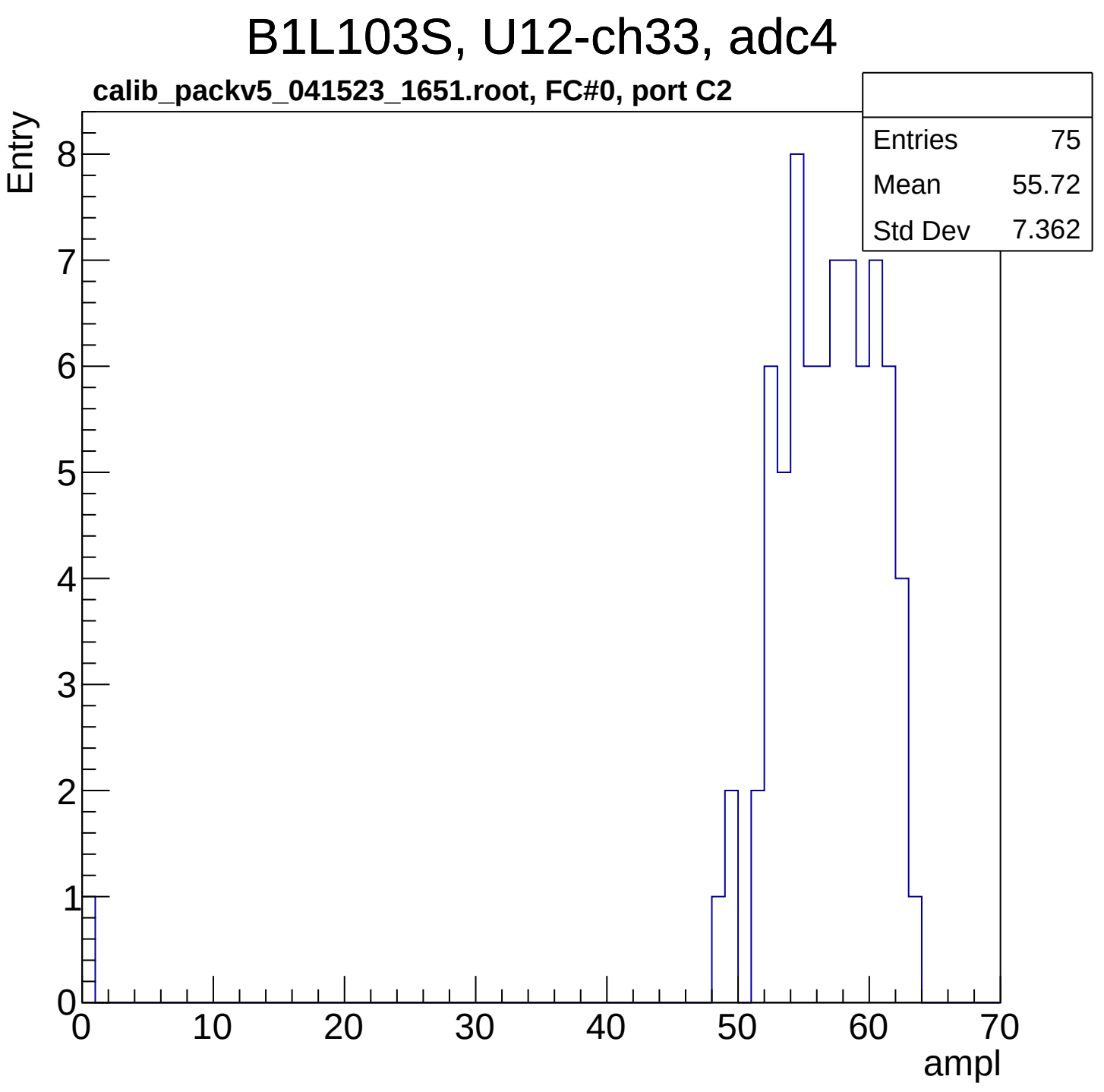
B1L103S, U12-ch33, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 55.72
Std Dev 7.362
Entry
ampl
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4
5
6
7
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0
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60
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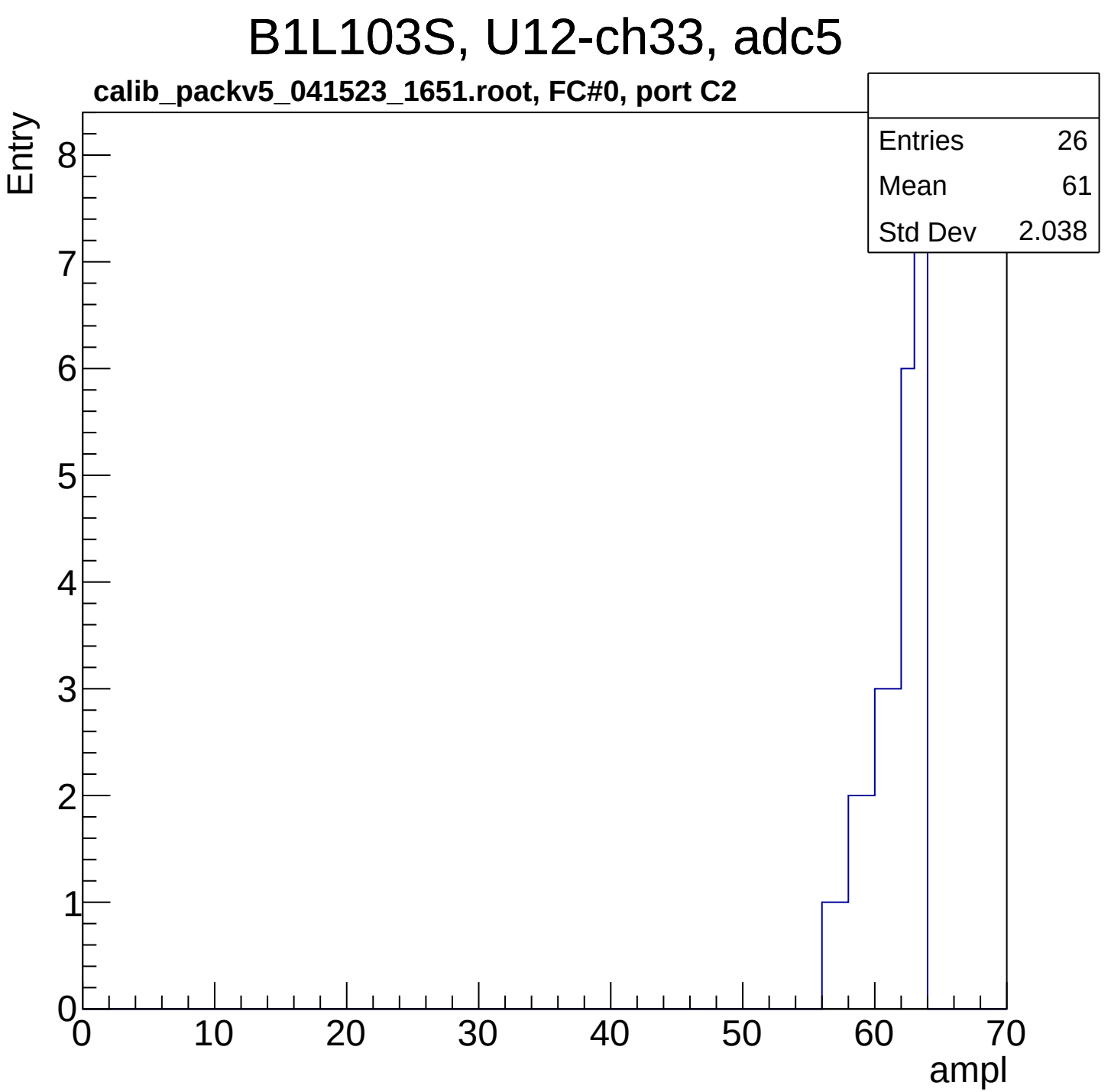
B1L103S, U12-ch33, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 61
Std Dev 2.038
Entry
ampl
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4
5
6
7
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0
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60
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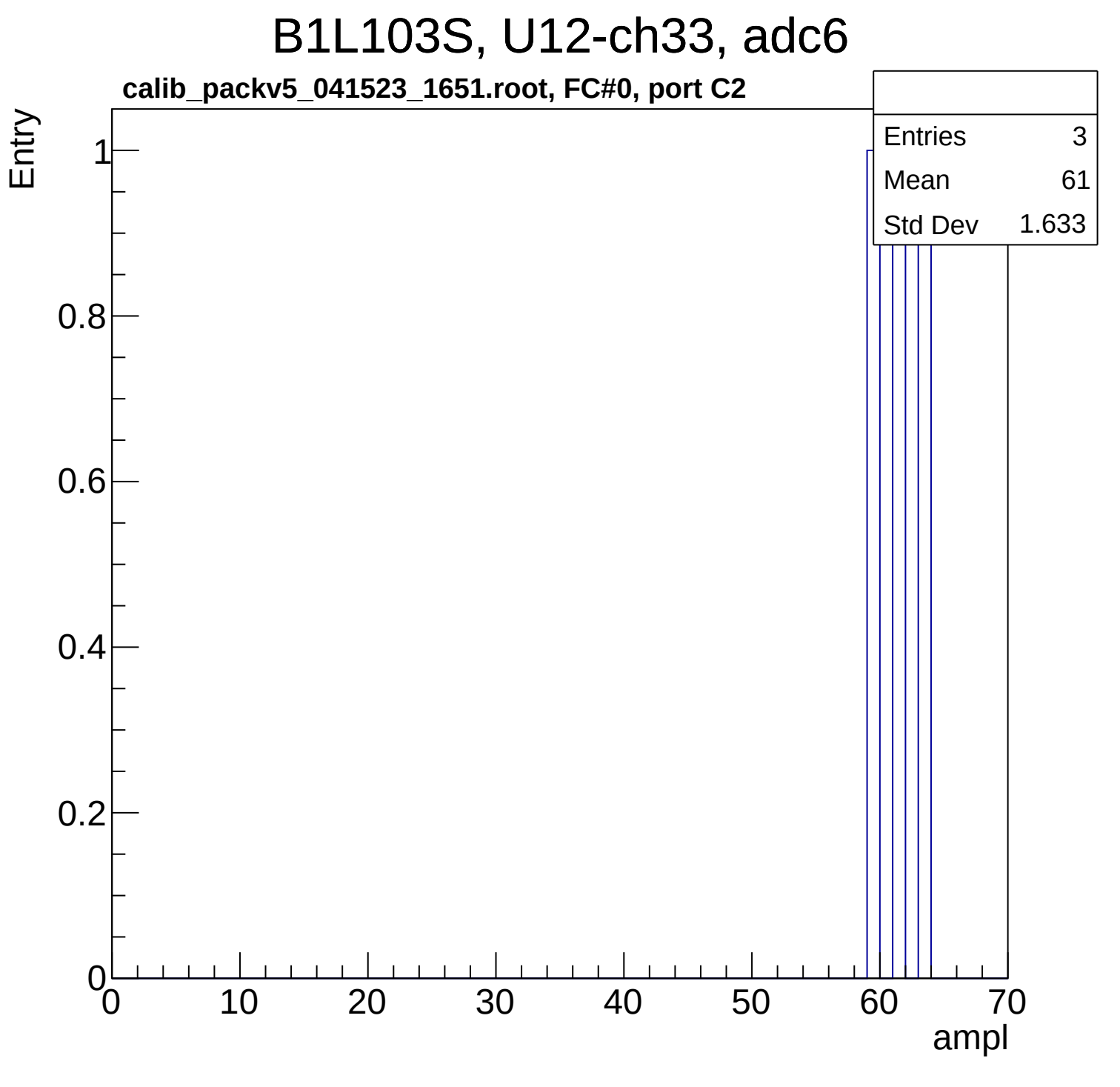
B1L103S, U12-ch33, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 61
Std Dev 1.633
Entry
ampl
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0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
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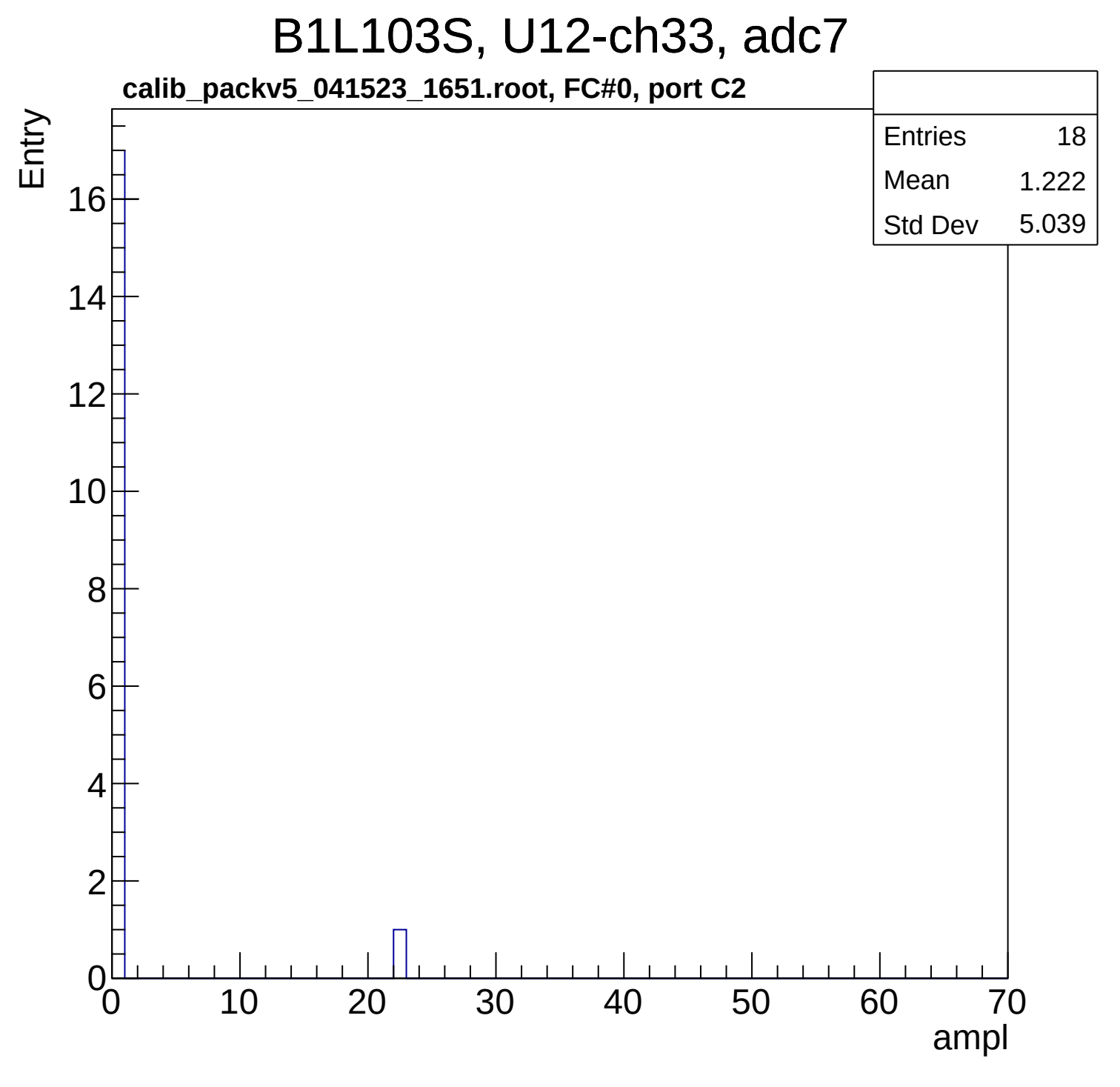
B1L103S, U12-ch33, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.222
Std Dev 5.039
Entry
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8
10
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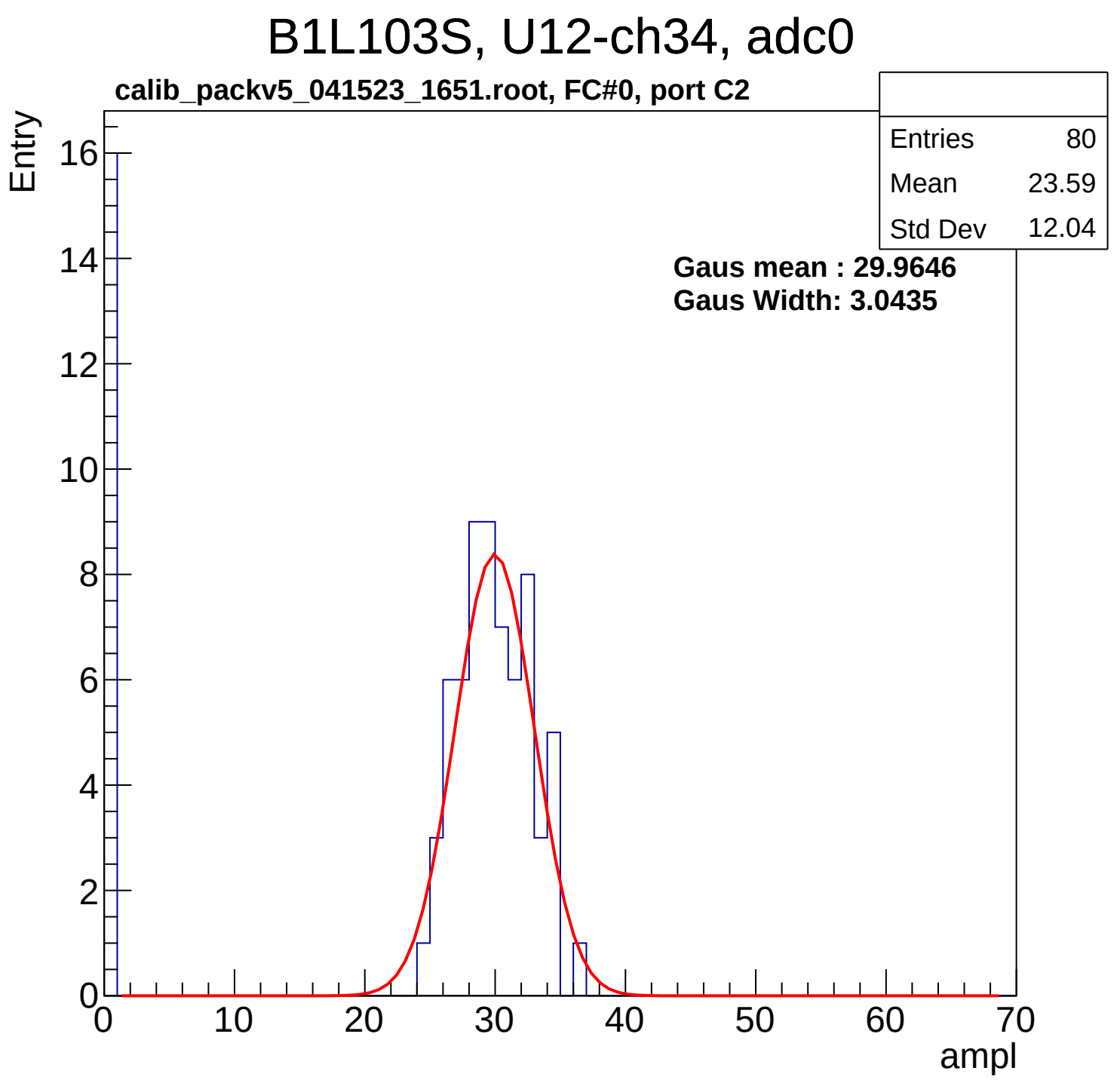
70
ampl


B1L103S, U12-ch34, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 23.59
Std Dev 12.04
Gaus mean : 29.9646
Gaus Width: 3.0435
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
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40
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60
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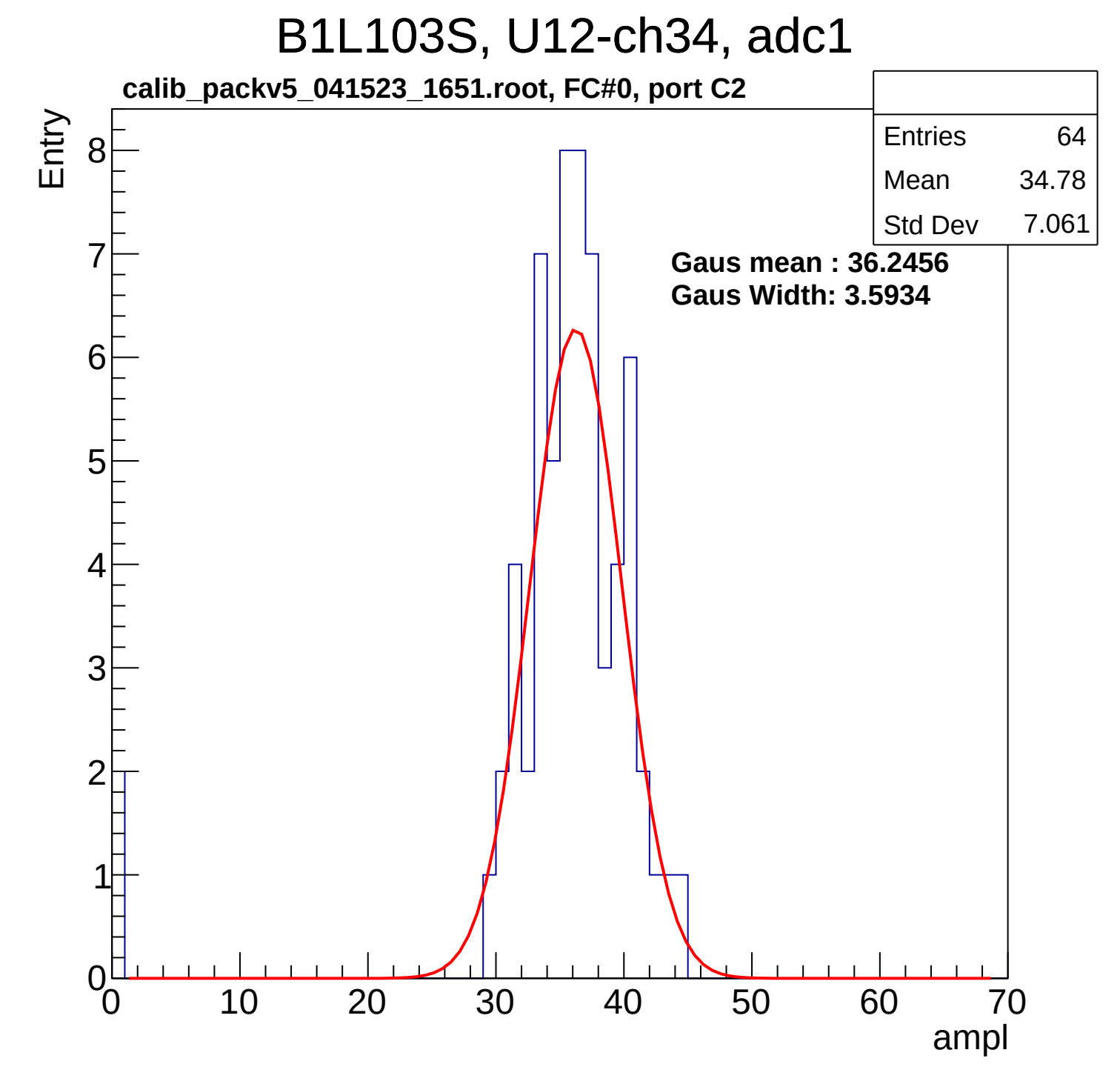
B1L103S, U12-ch34, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 34.78
Std Dev 7.061
Gaus mean : 36.2456
Gaus Width: 3.5934
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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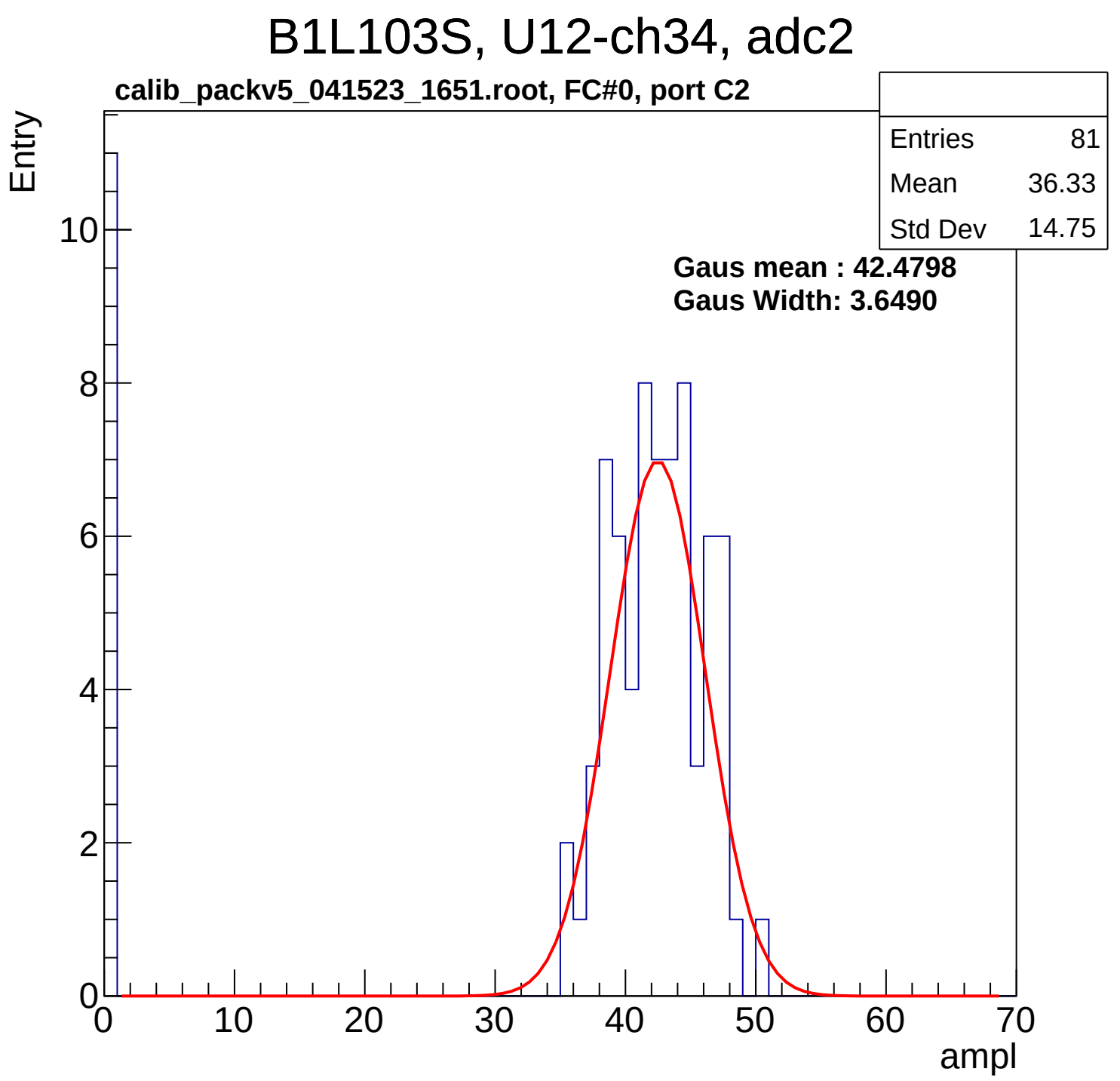
B1L103S, U12-ch34, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 36.33
Std Dev 14.75
Gaus mean : 42.4798
Gaus Width: 3.6490
Entry
ampl
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0
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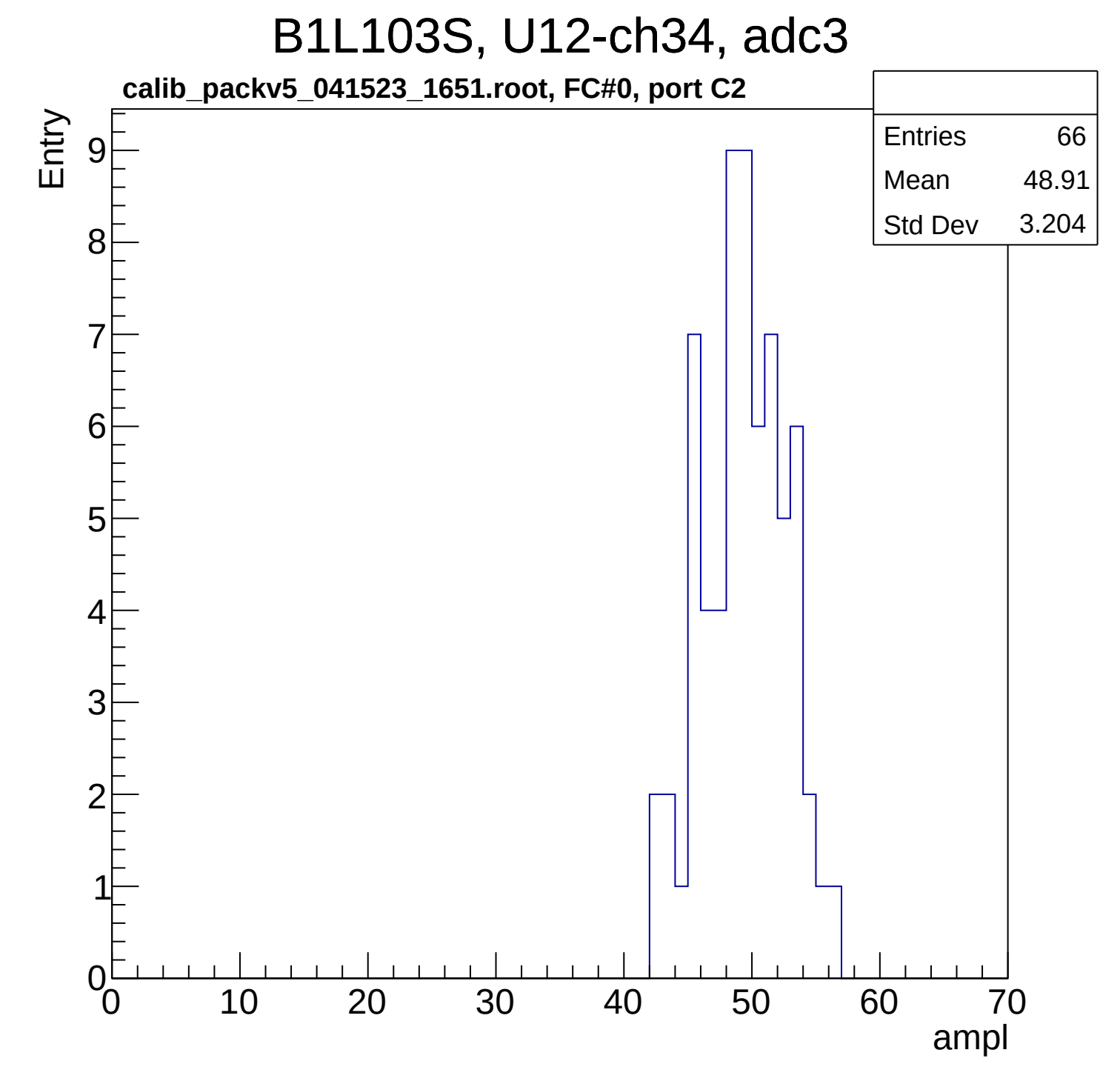
B1L103S, U12-ch34, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 48.91
Std Dev 3.204
Entry
ampl
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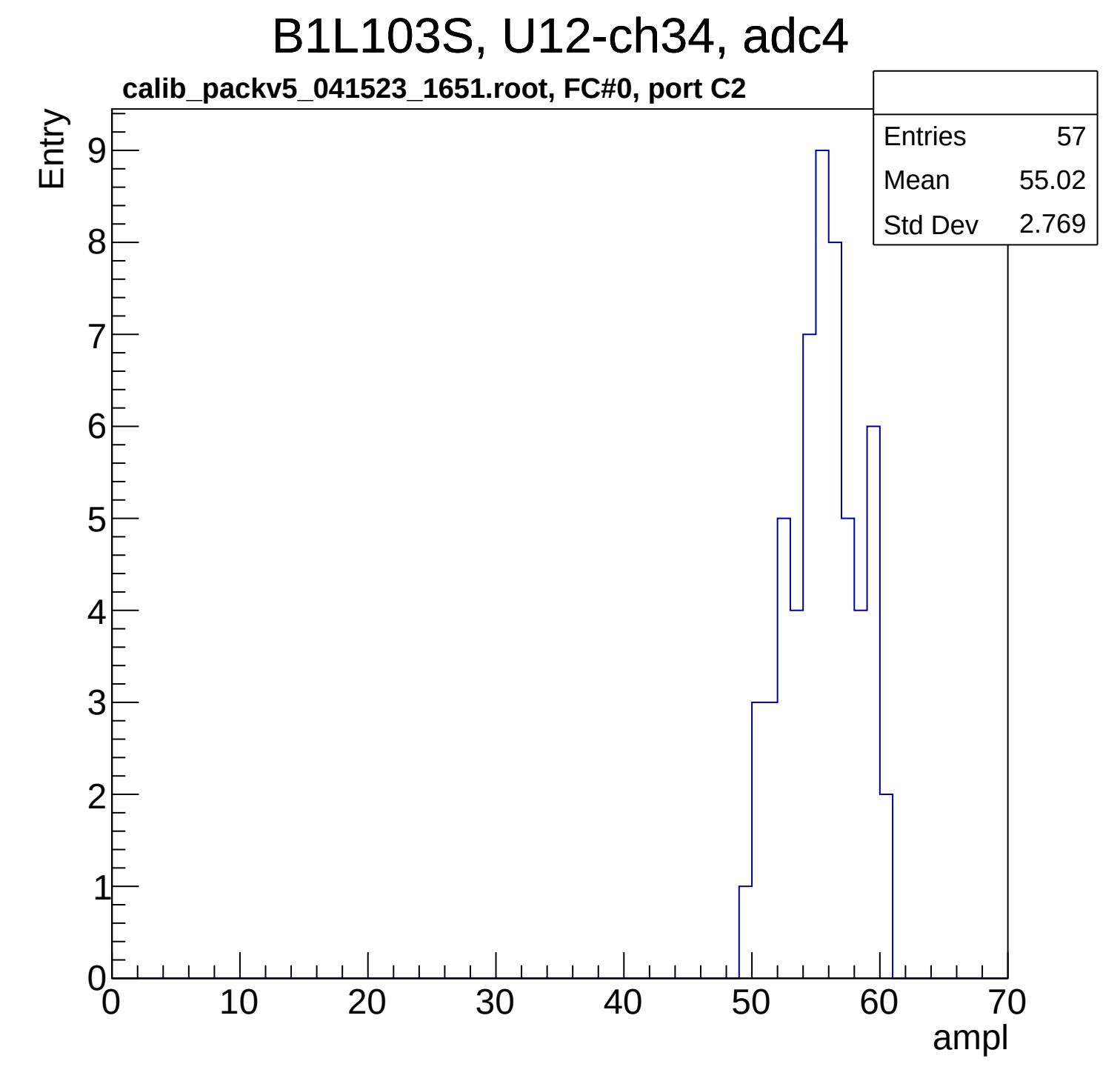
B1L103S, U12-ch34, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 55.02
Std Dev 2.769
Entry
ampl
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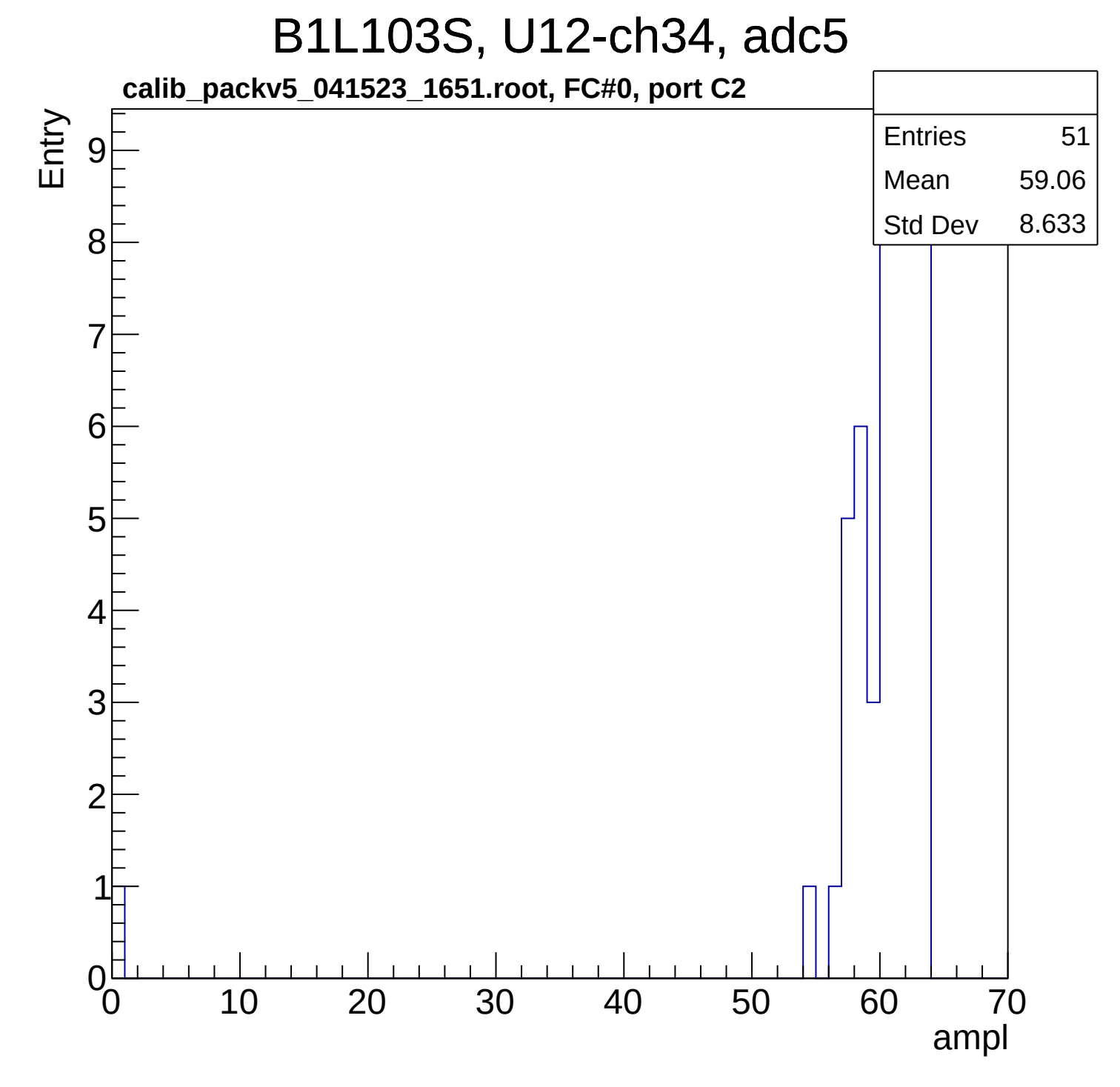
B1L103S, U12-ch34, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 59.06
Std Dev 8.633
Entry
ampl
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3
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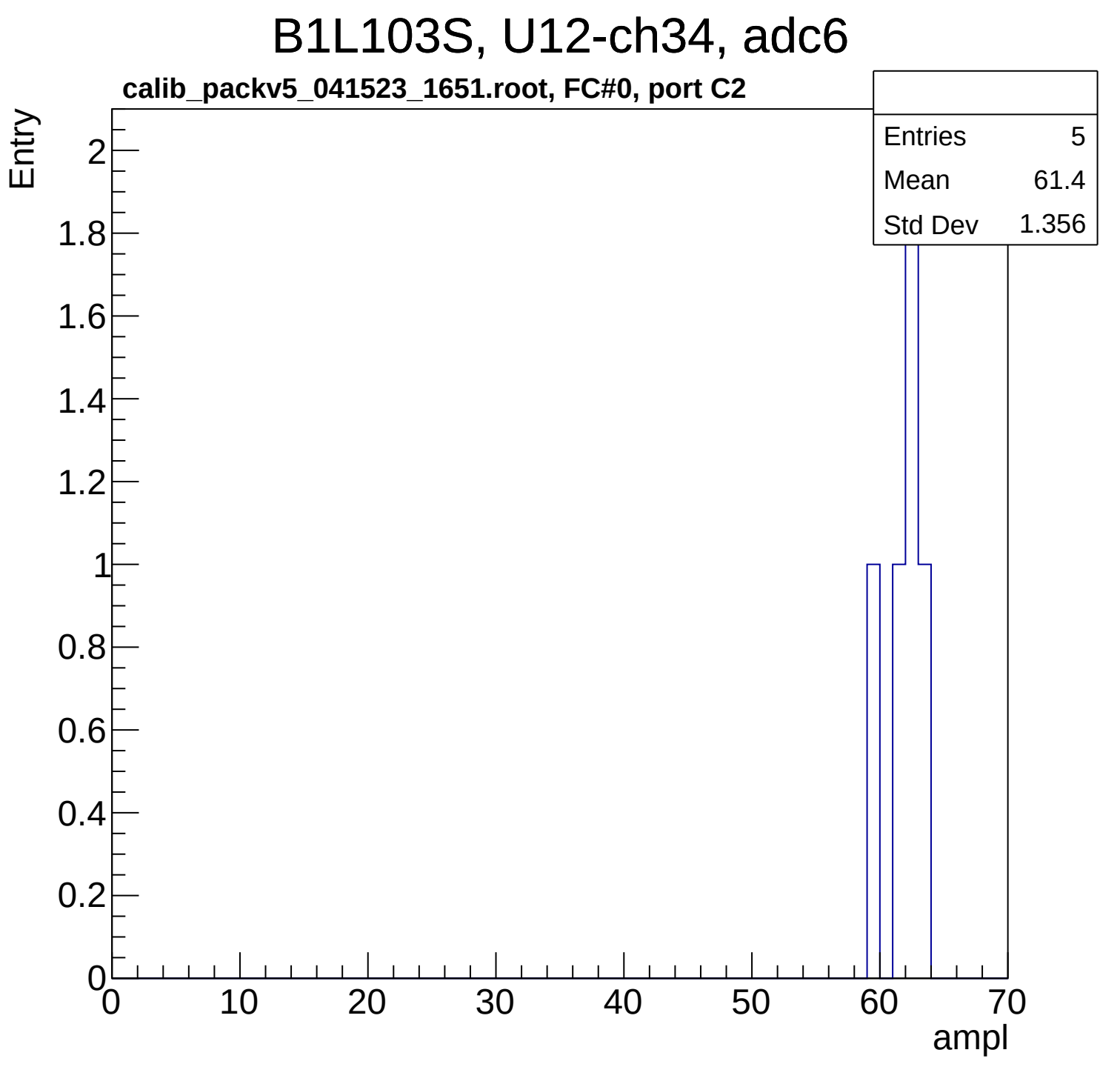
B1L103S, U12-ch34, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.4
Std Dev 1.356
Entry
ampl
0
0.2
0.4
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1.4
1.6
1.8
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0
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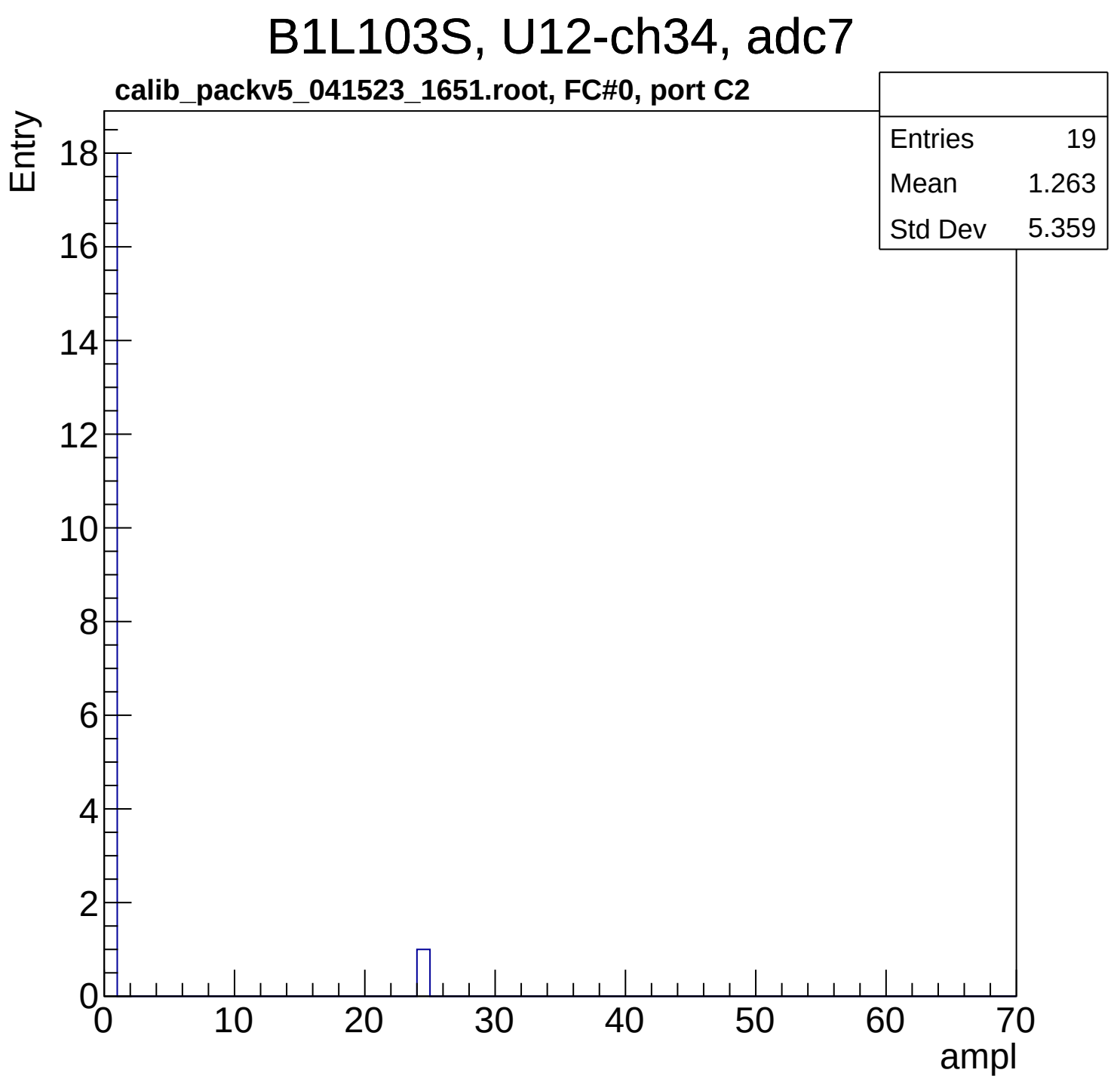
B1L103S, U12-ch34, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.263
Std Dev 5.359
Entry
ampl
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6
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10
12
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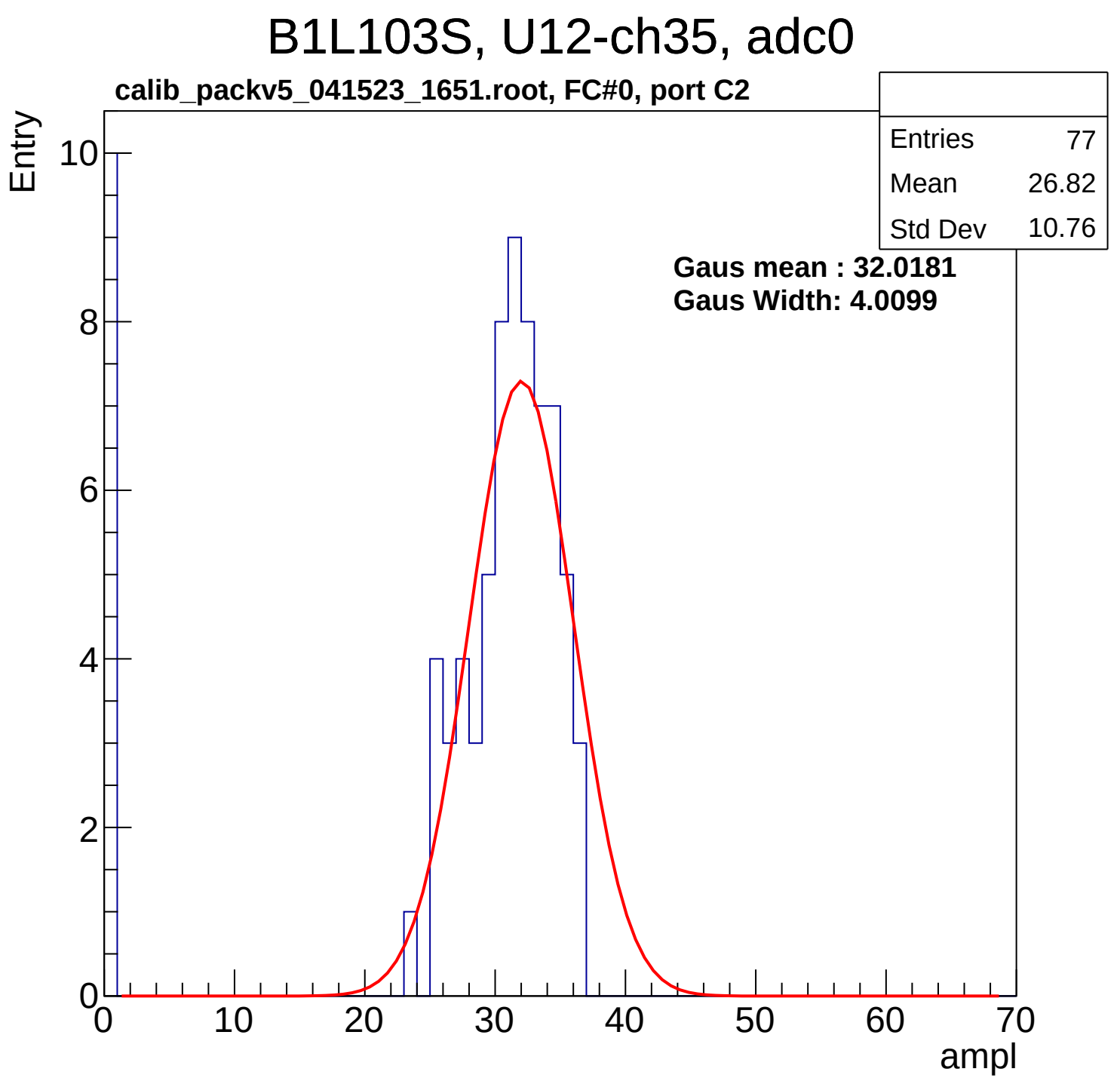
B1L103S, U12-ch35, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 26.82
Std Dev 10.76
Gaus mean : 32.0181
Gaus Width: 4.0099
Entry
ampl
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2
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0
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40
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60
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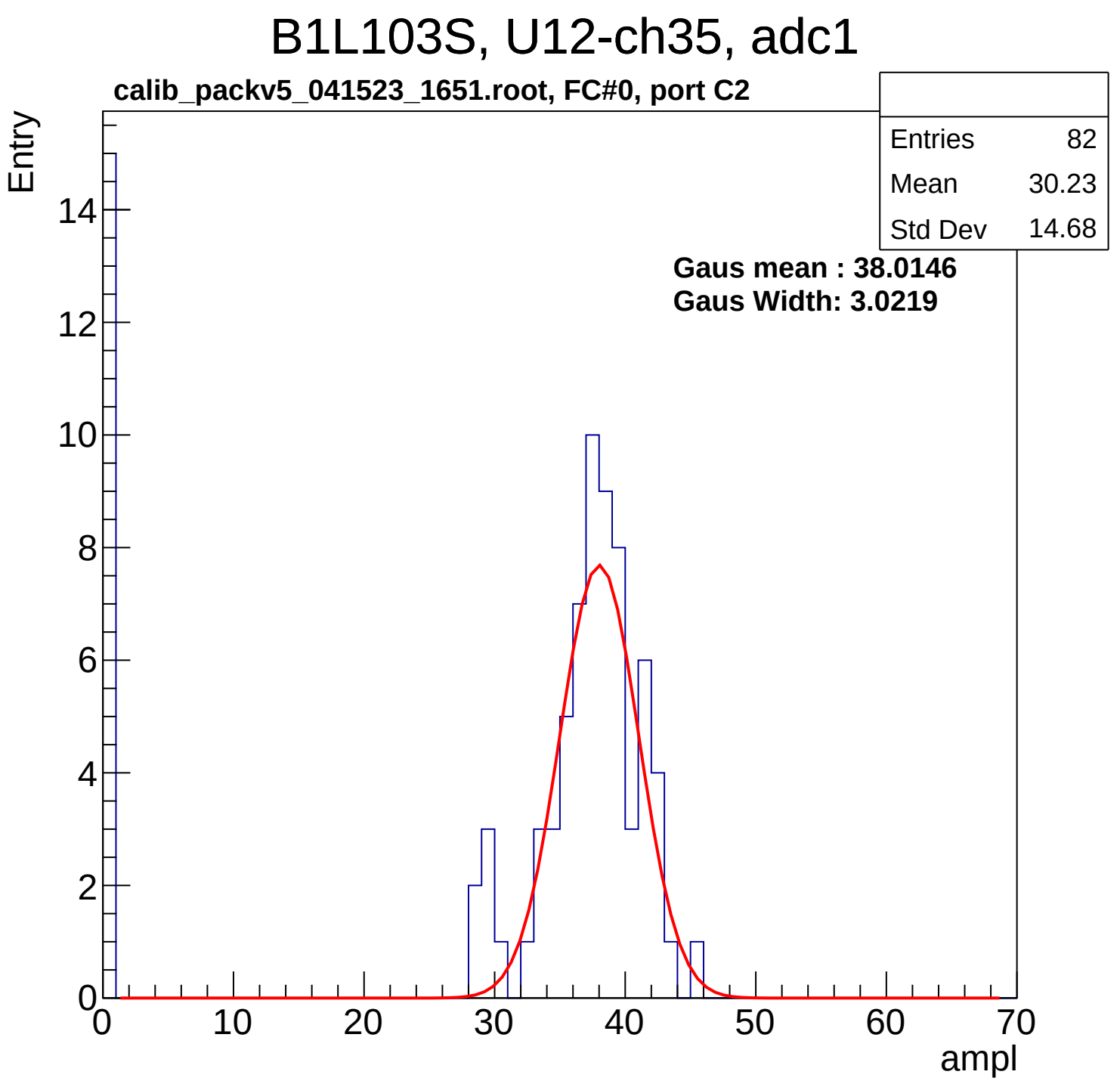
B1L103S, U12-ch35, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 30.23
Std Dev 14.68
Gaus mean : 38.0146
Gaus Width: 3.0219
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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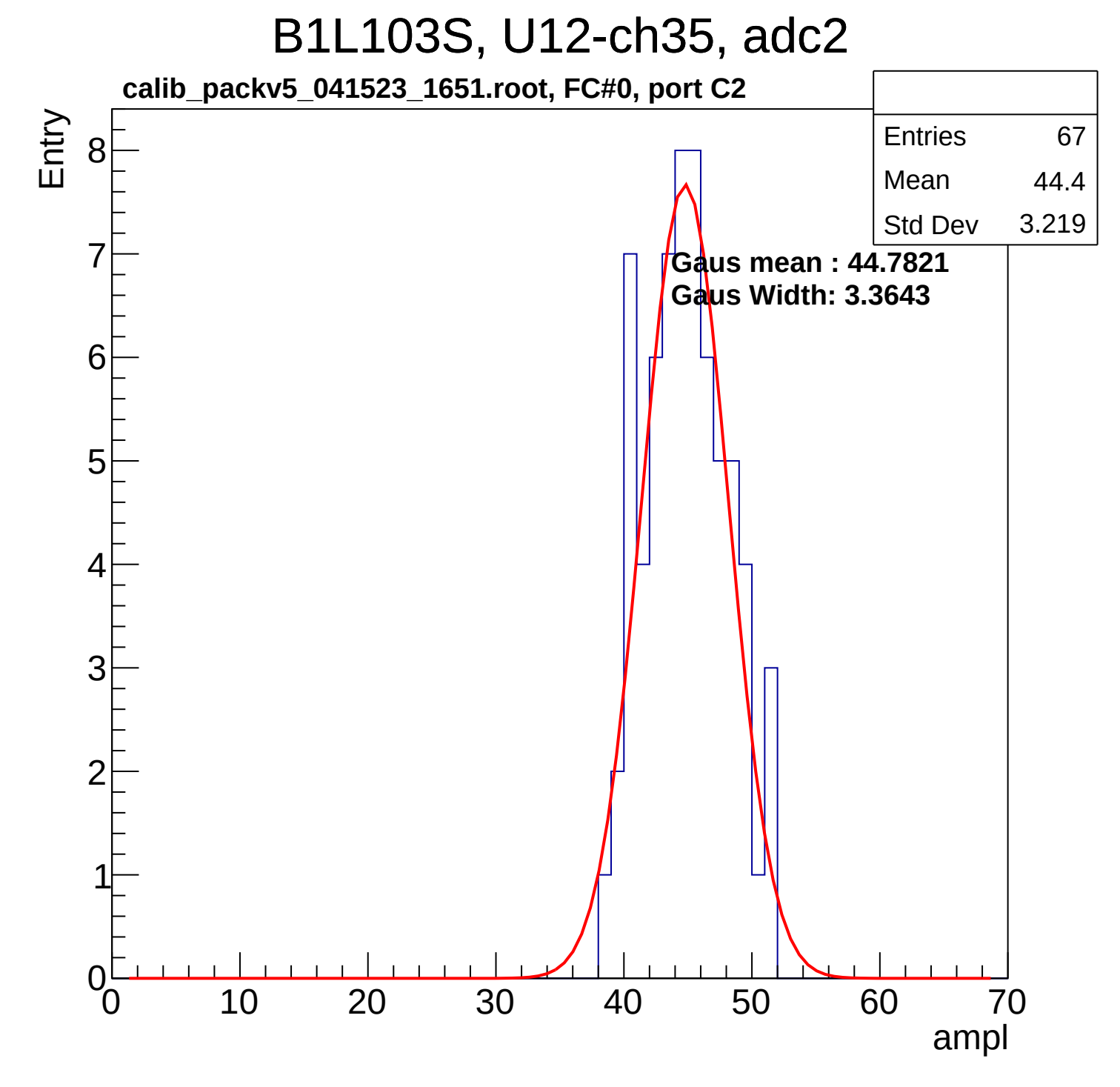
B1L103S, U12-ch35, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 44.4
Std Dev 3.219
Gaus mean : 44.7821
Gaus Width: 3.3643
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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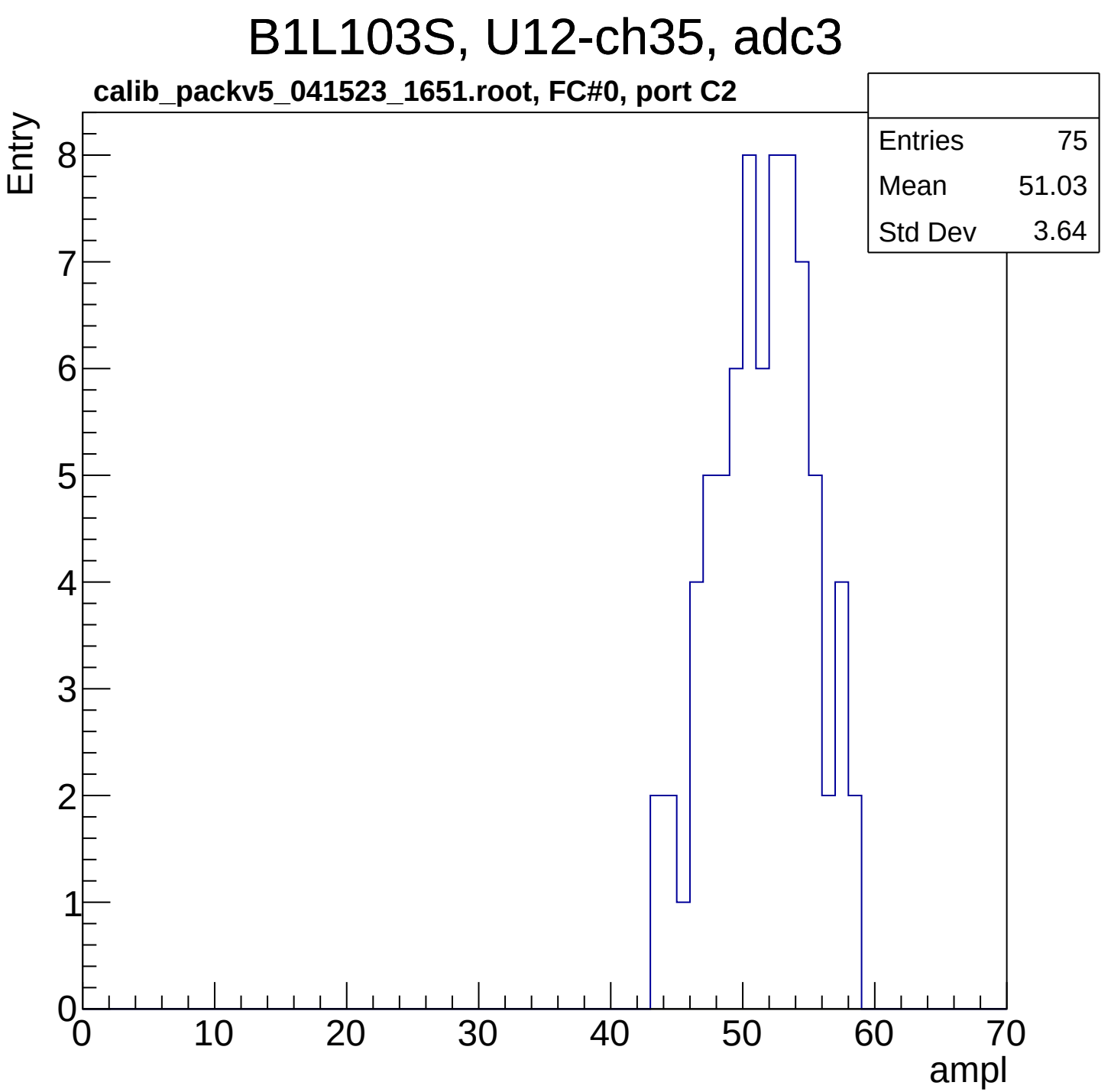
B1L103S, U12-ch35, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 51.03
Std Dev 3.64
Entry
ampl
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1
2
3
4
5
6
7
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0
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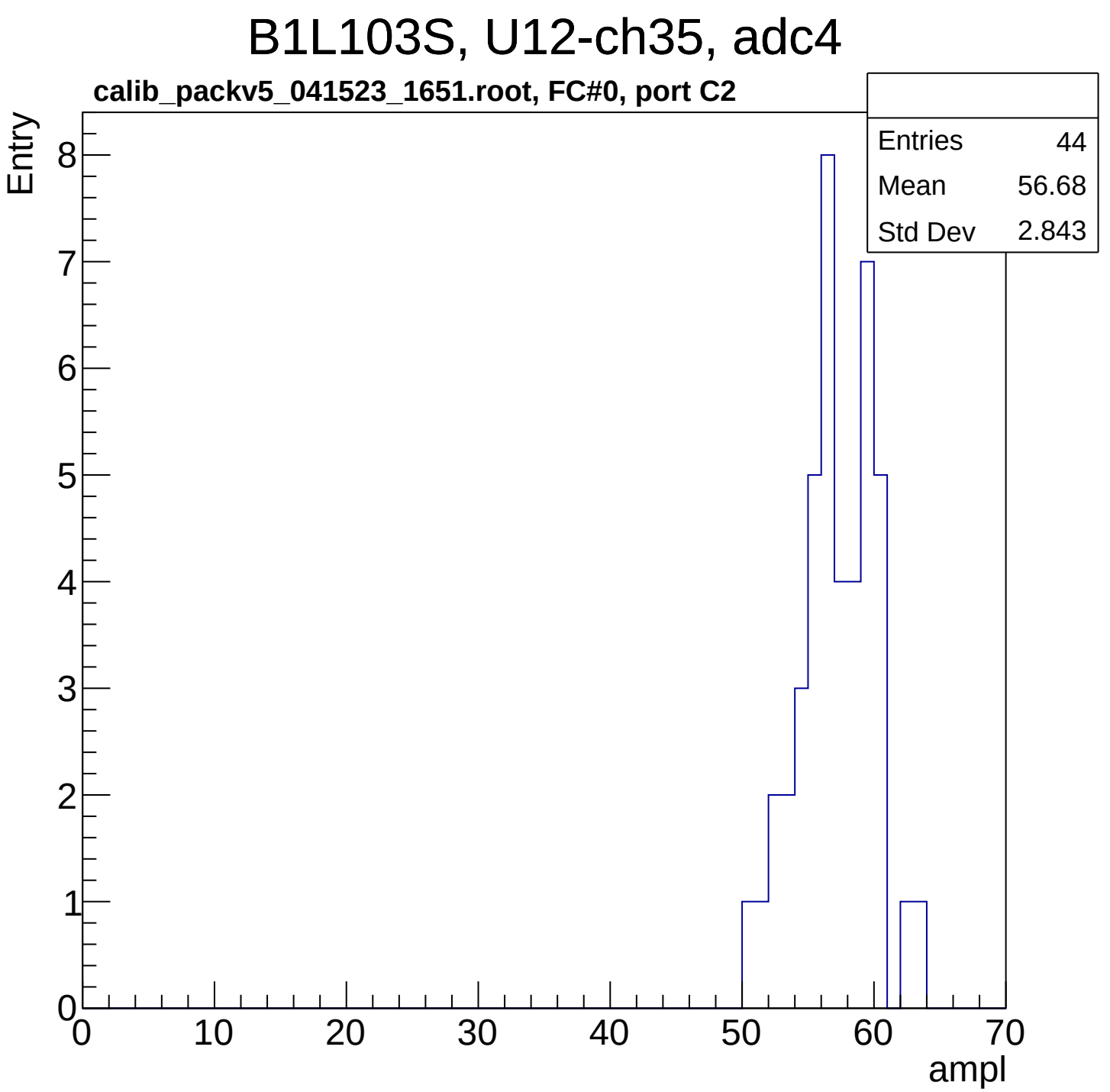
B1L103S, U12-ch35, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 56.68
Std Dev 2.843
Entry
ampl
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1
2
3
4
5
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0
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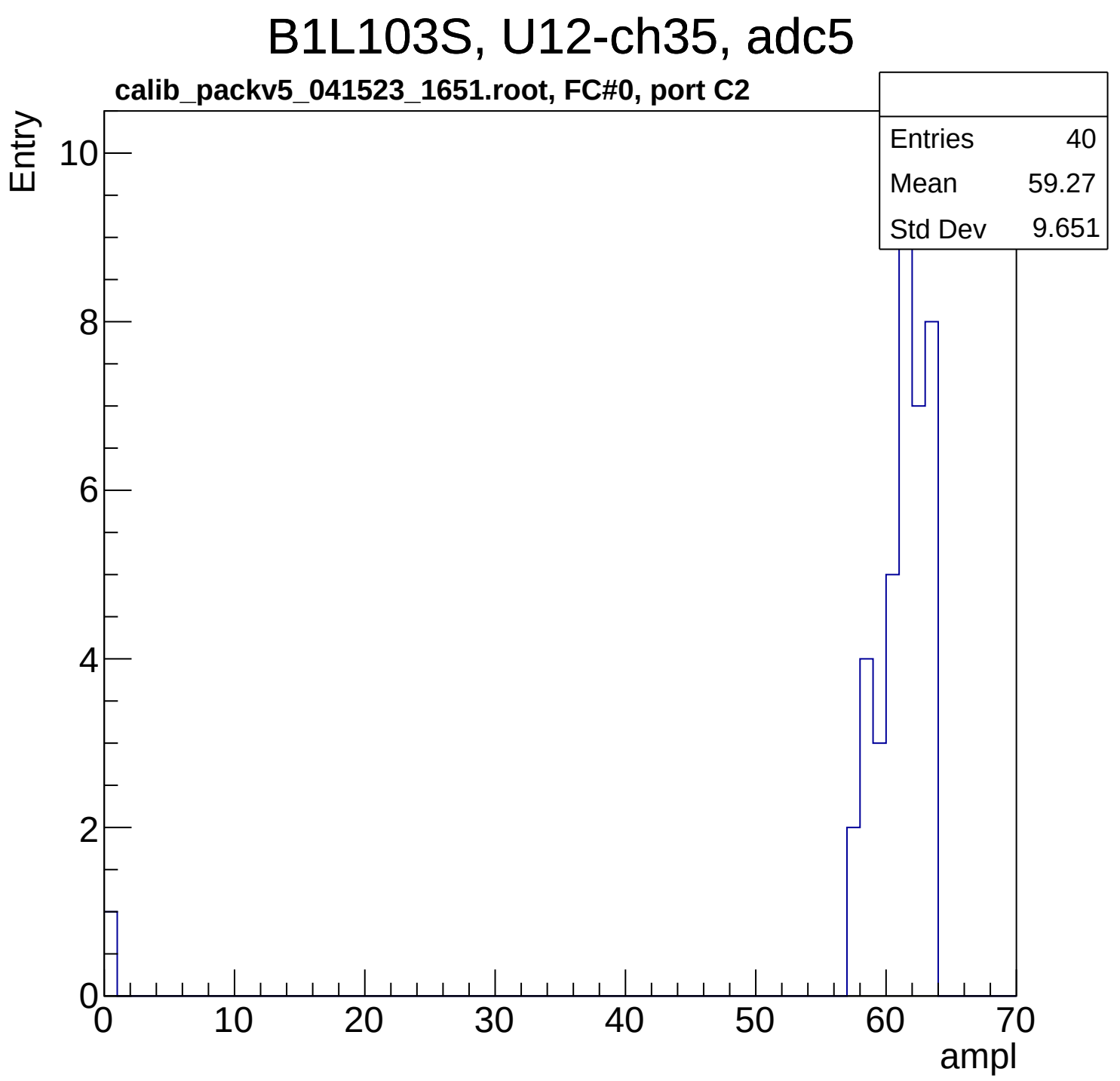
B1L103S, U12-ch35, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 59.27
Std Dev 9.651
Entry
0
2
4
6
8
10
0
10
20
30
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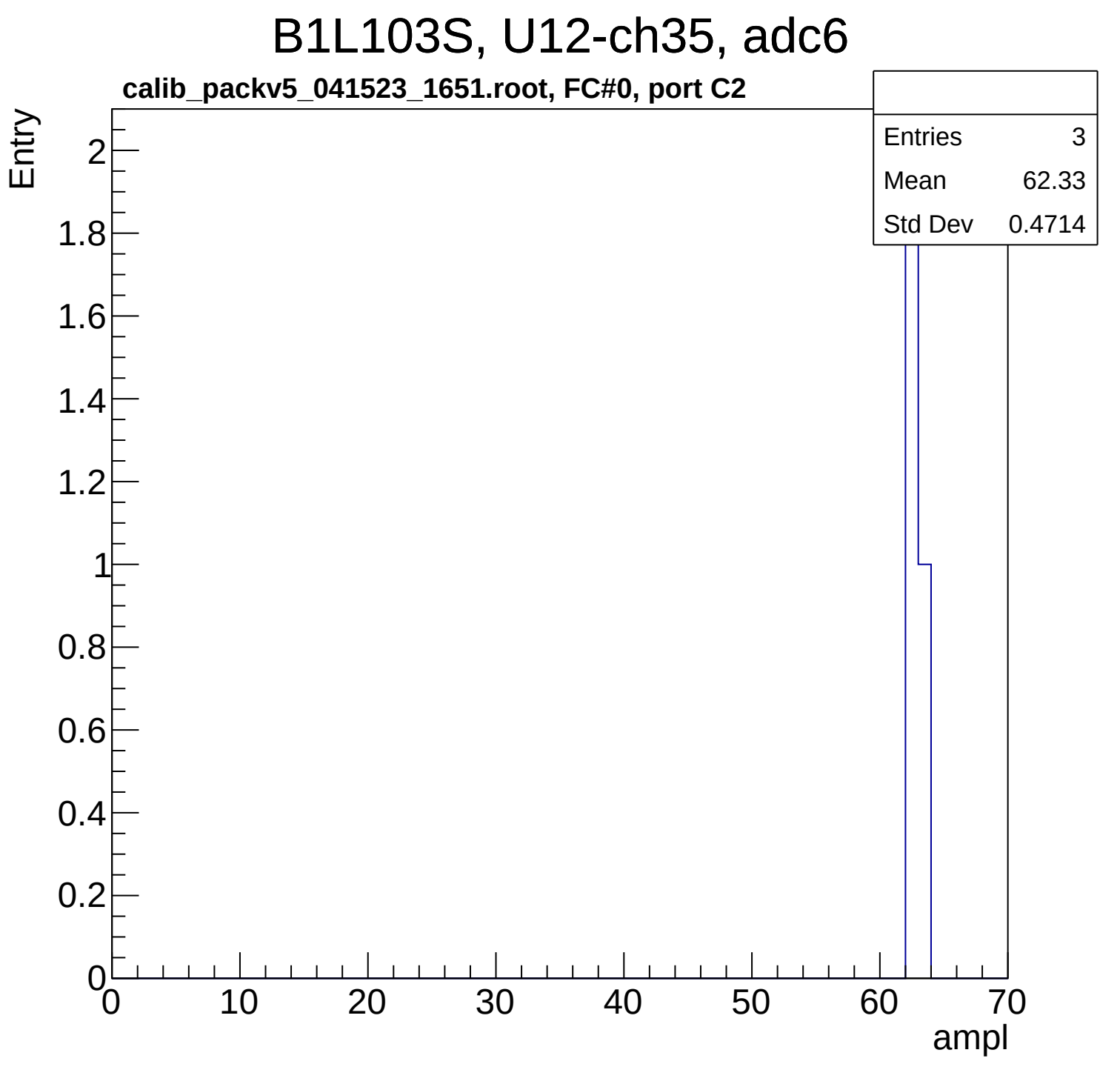
50
60
70
ampl


B1L103S, U12-ch35, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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40
50
60
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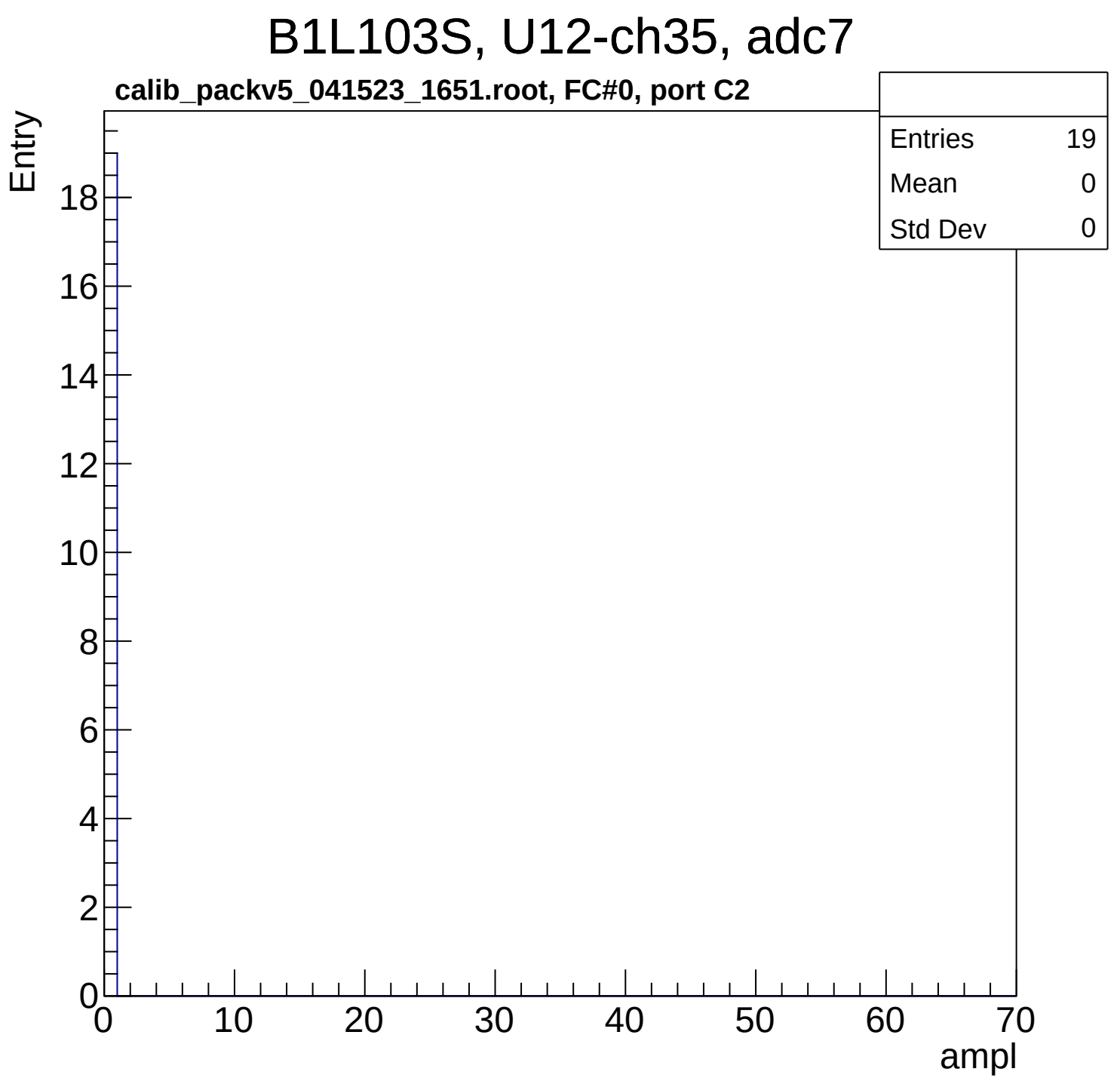
B1L103S, U12-ch35, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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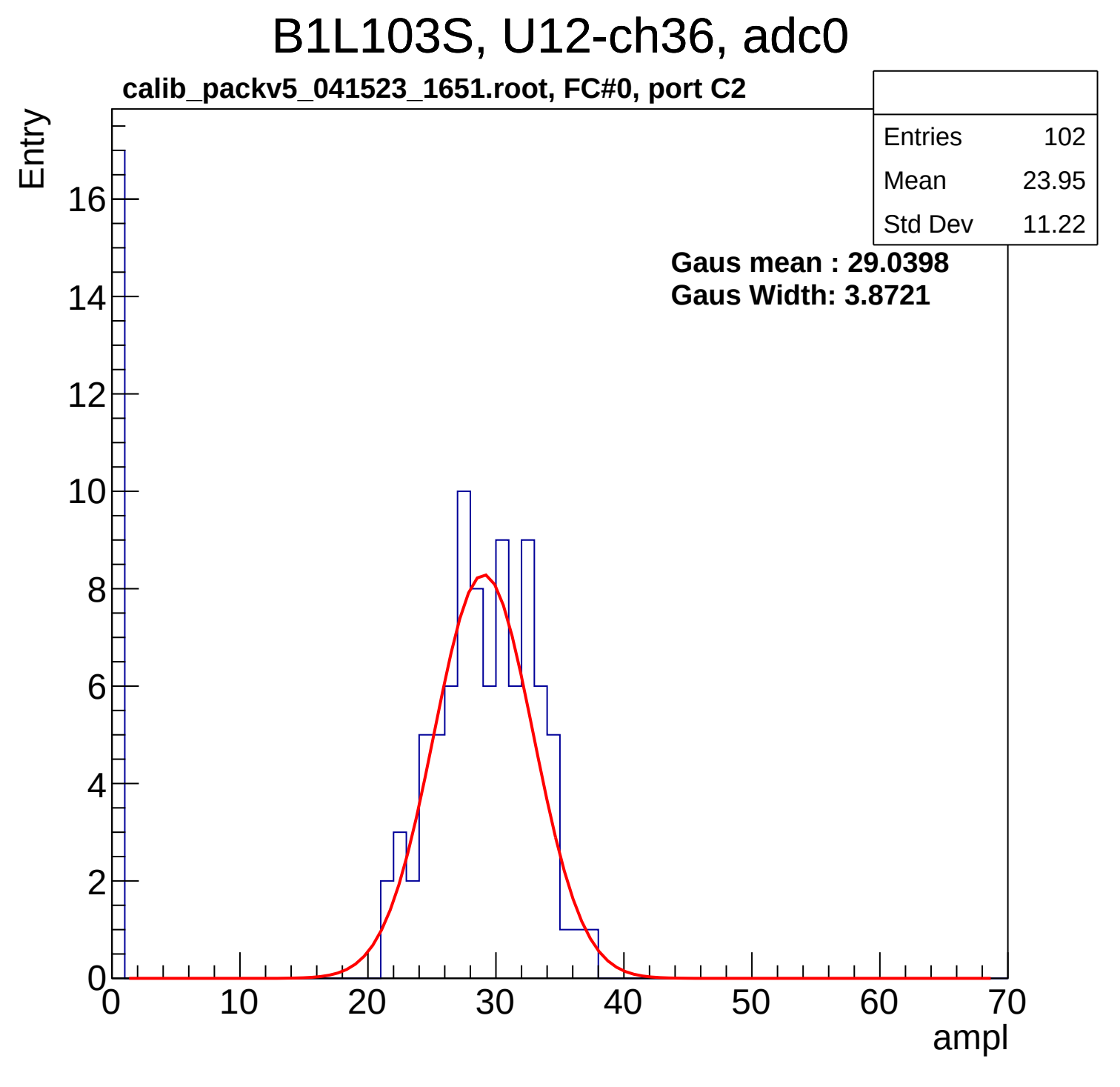
50
60
70
ampl


B1L103S, U12-ch36, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 102
Mean 23.95
Std Dev 11.22
Gaus mean : 29.0398
Gaus Width: 3.8721
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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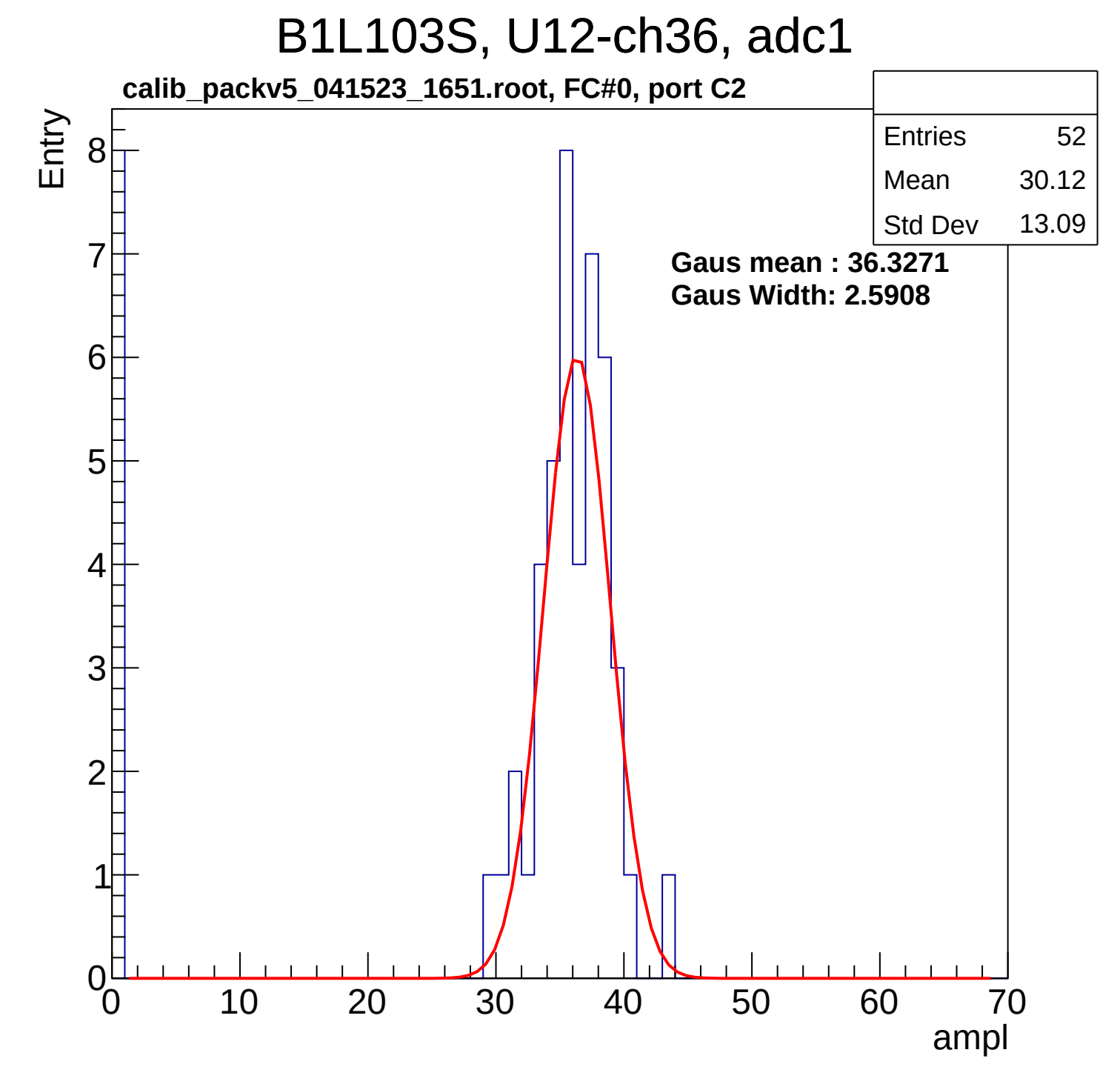
B1L103S, U12-ch36, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 30.12
Std Dev 13.09
Gaus mean : 36.3271
Gaus Width: 2.5908
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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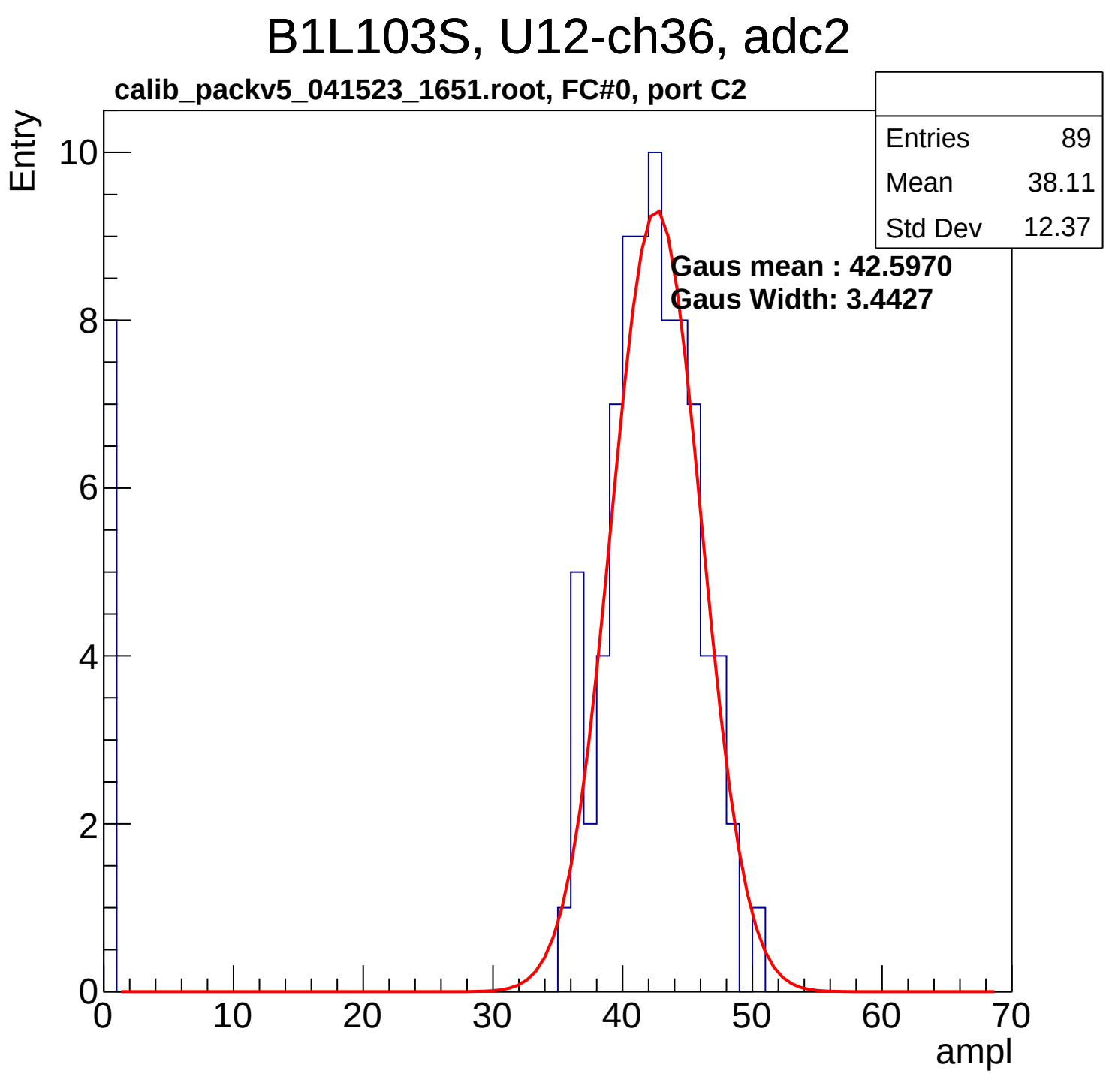
B1L103S, U12-ch36, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 38.11
Std Dev 12.37
Gaus mean : 42.5970
Gaus Width: 3.4427
Entry
ampl
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2
4
6
8
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0
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20
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40
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60
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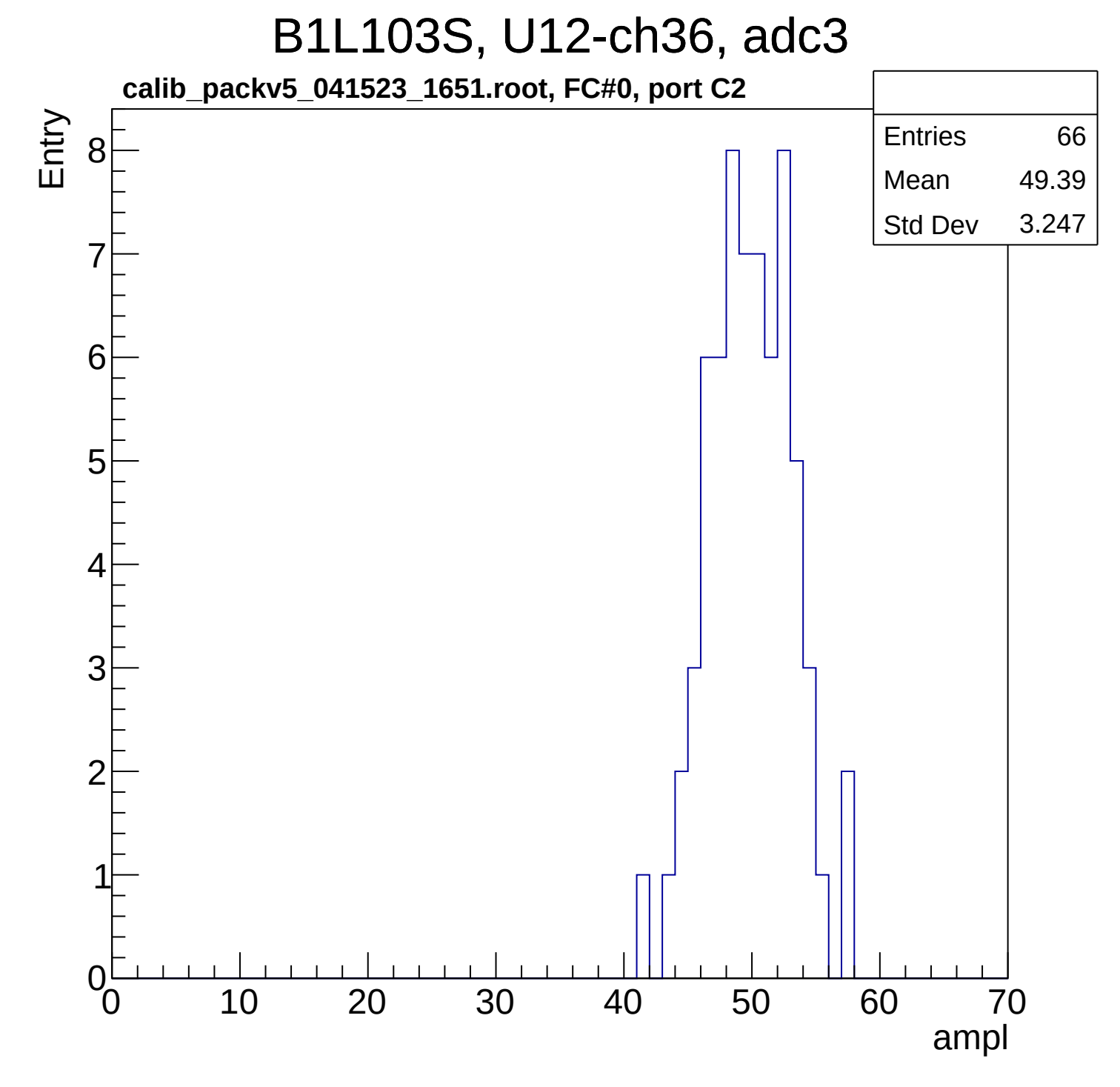
B1L103S, U12-ch36, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 49.39
Std Dev 3.247
Entry
ampl
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2
3
4
5
6
7
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0
10
20
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50
60
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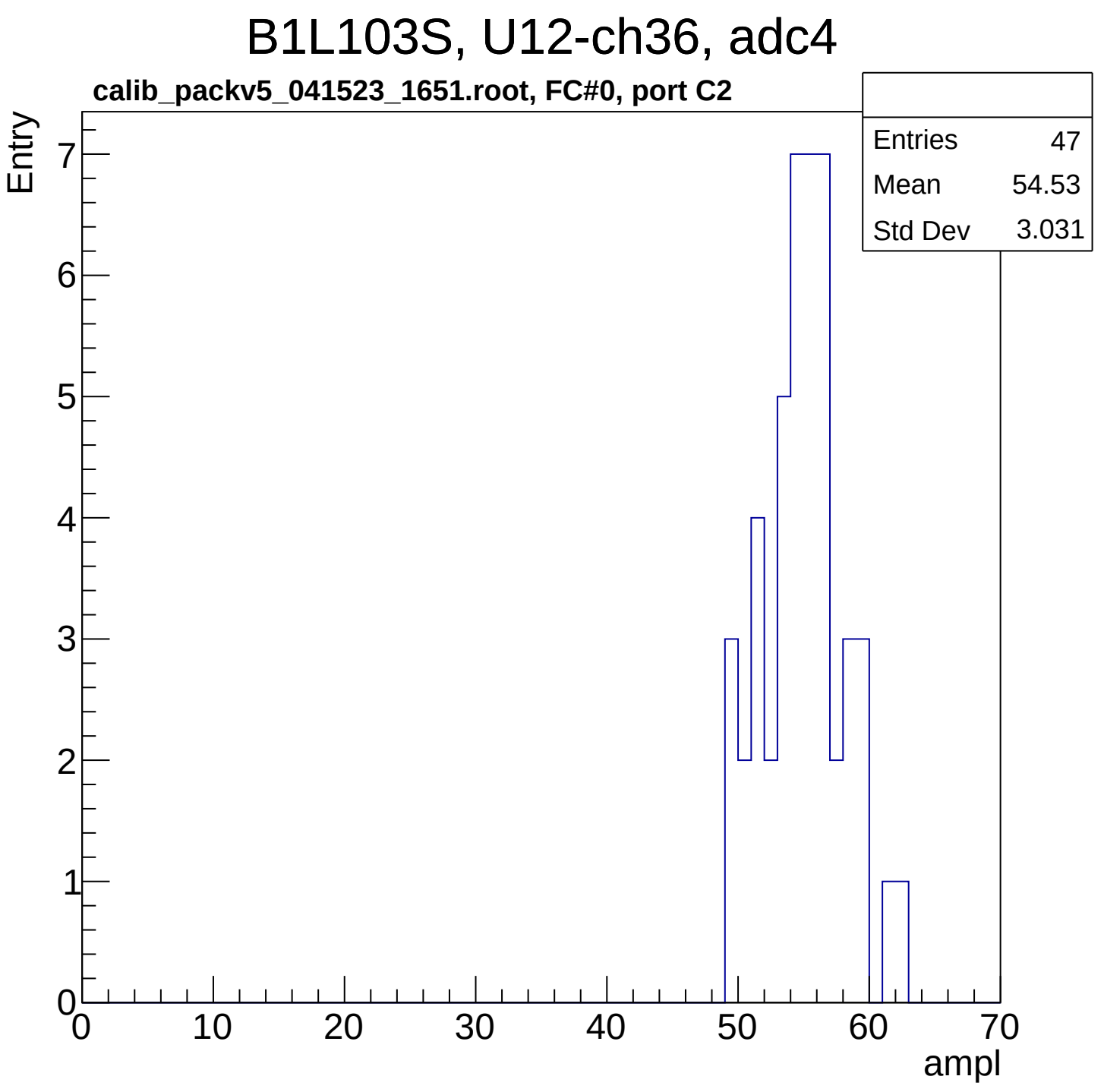
B1L103S, U12-ch36, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 54.53
Std Dev 3.031
Entry
ampl
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1
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3
4
5
6
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0
10
20
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40
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60
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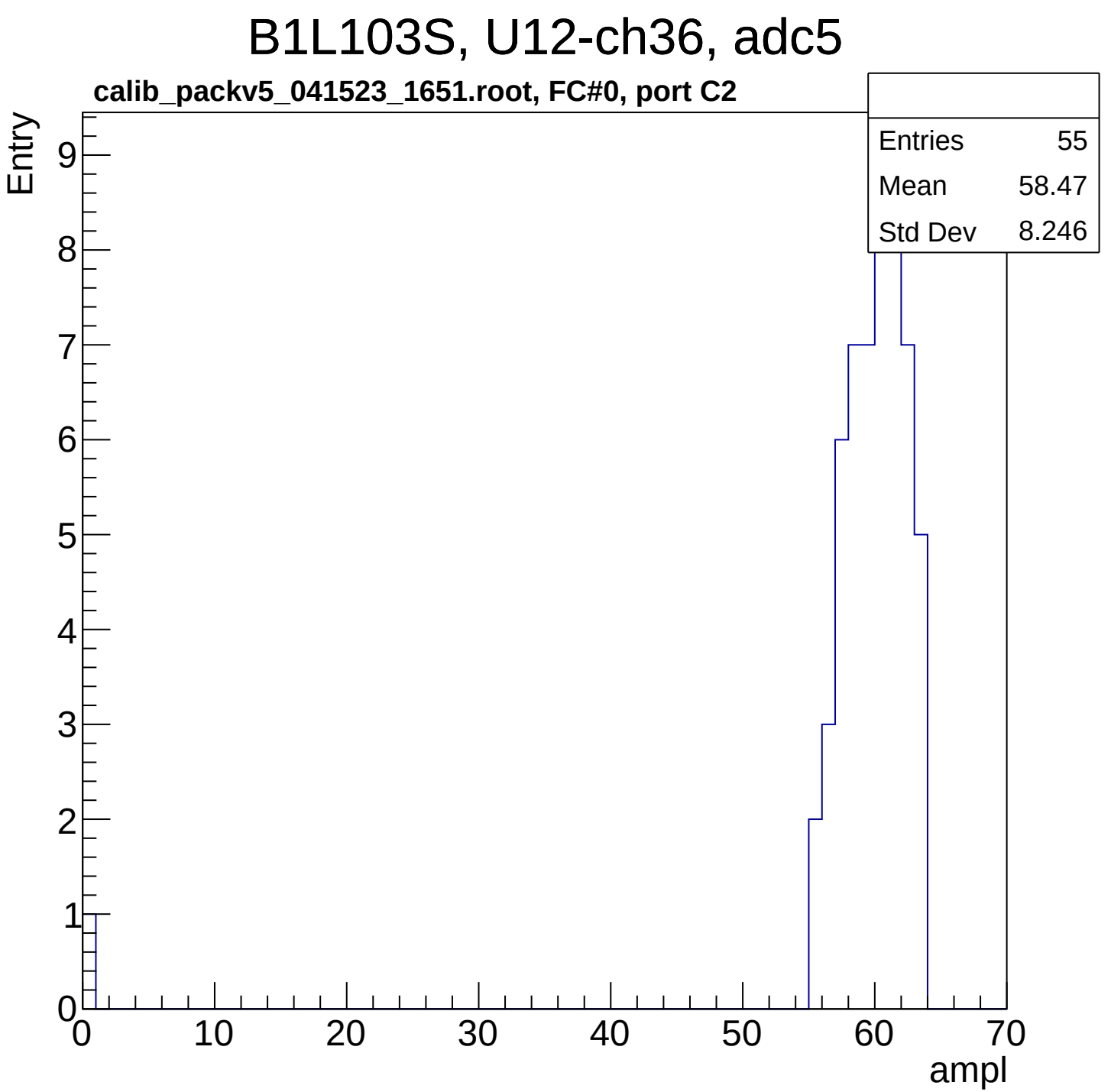
B1L103S, U12-ch36, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.47
Std Dev 8.246
Entry
ampl
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6
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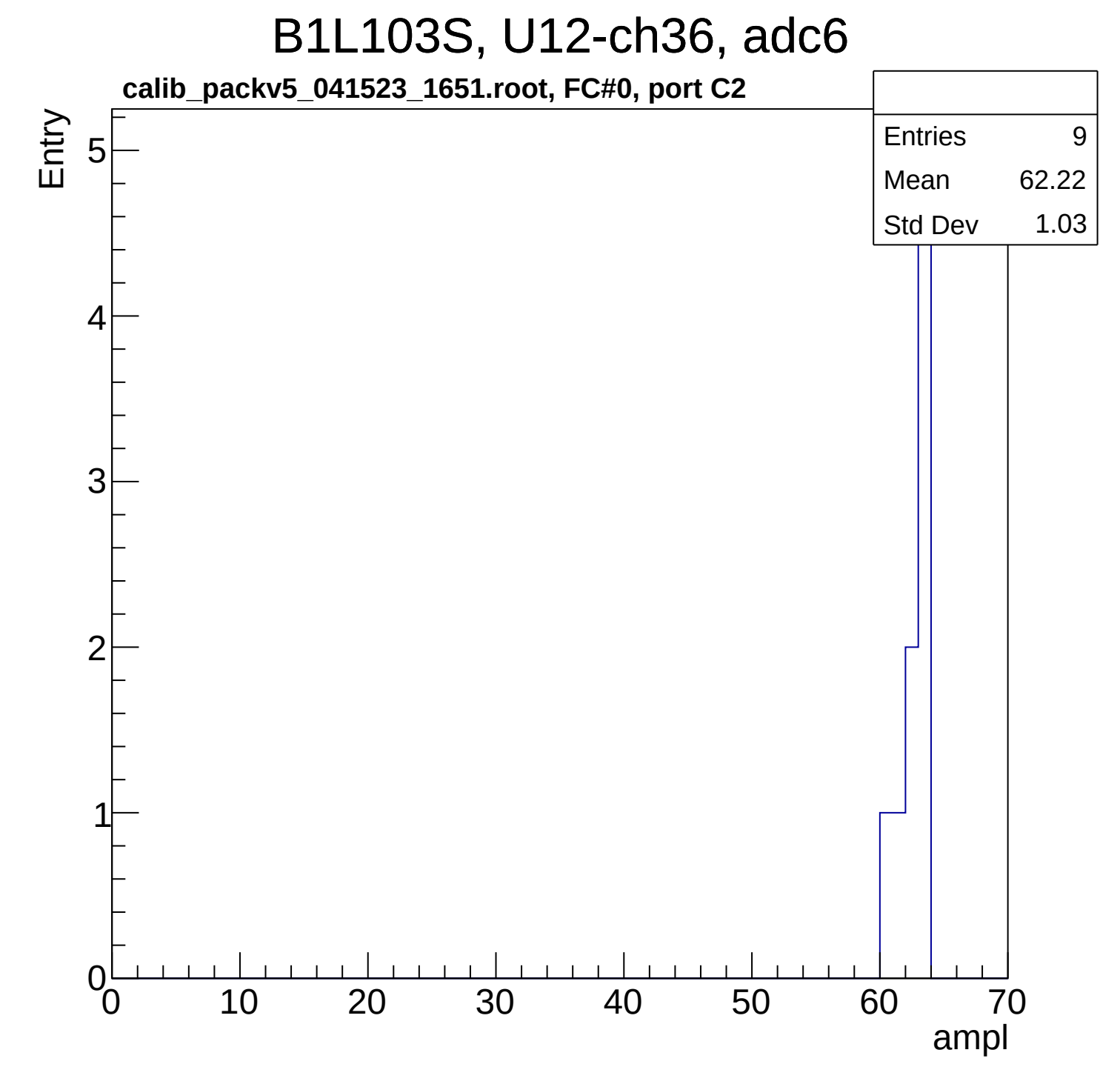
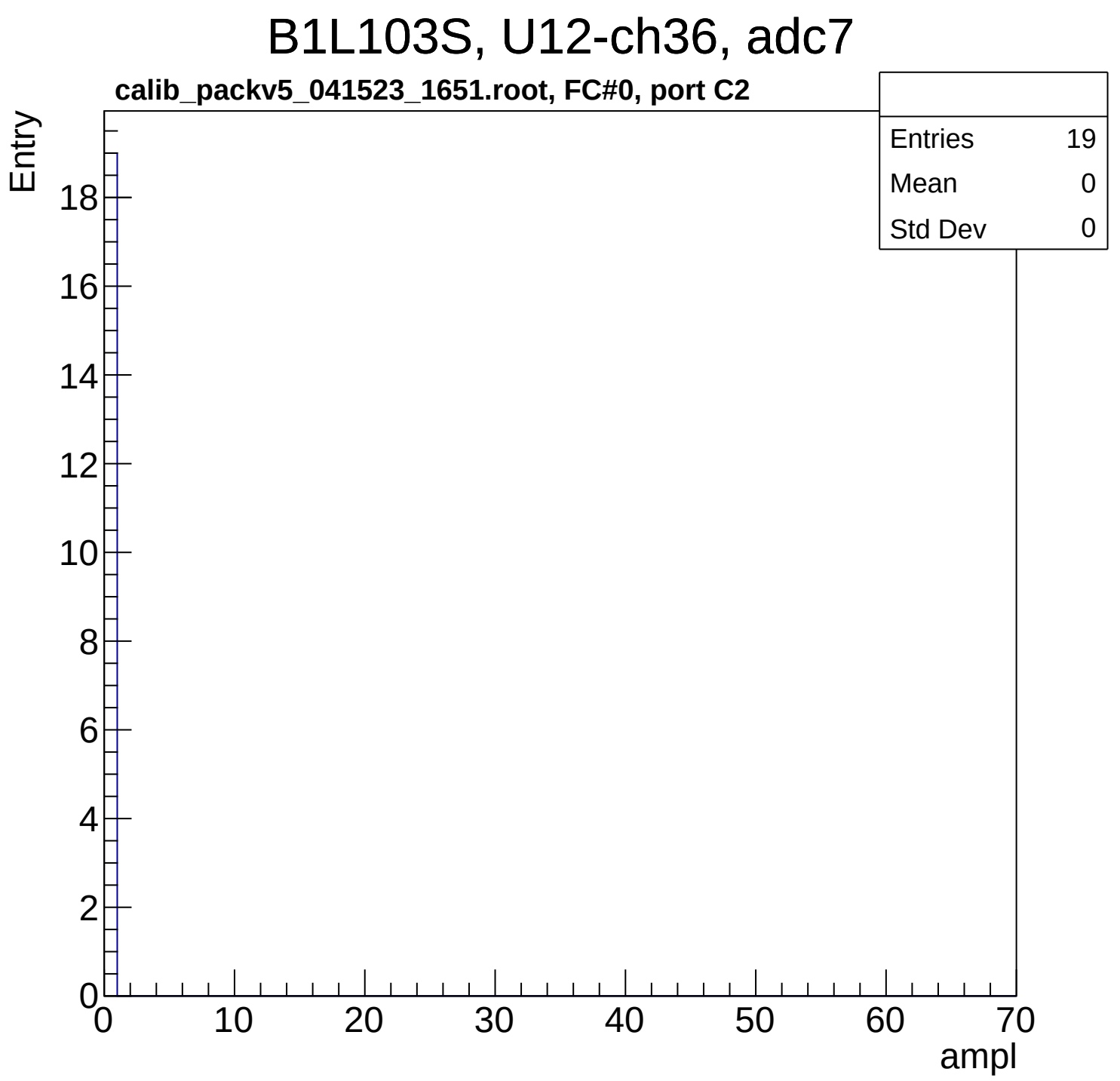

B1L103S, U12-ch36, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 62.22
Std Dev 1.03
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U12-ch36, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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6
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10
12
14
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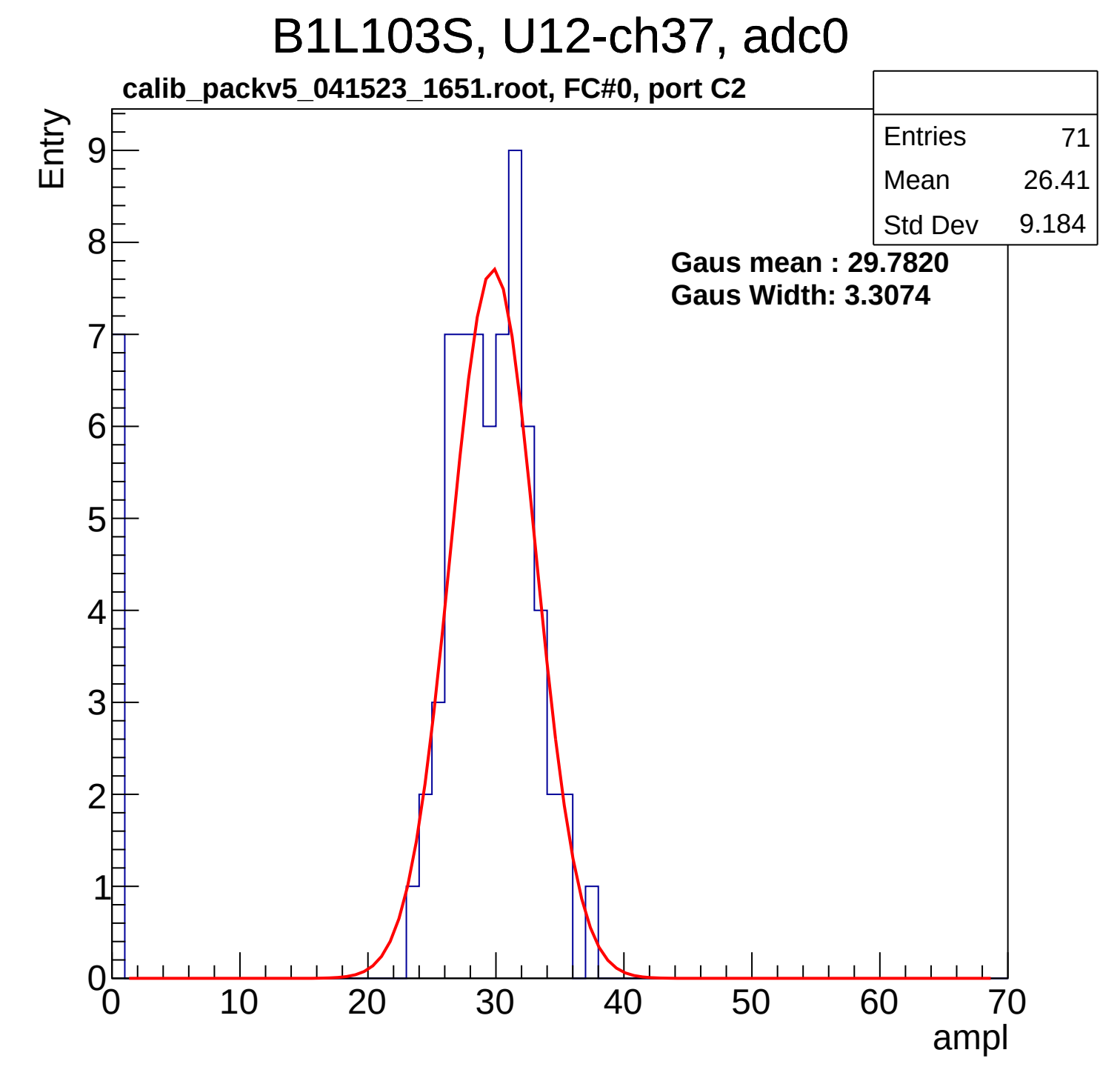
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch37, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 26.41
Std Dev 9.184
Gaus mean : 29.7820
Gaus Width: 3.3074
Entry
ampl
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3
4
5
6
7
8
9
0
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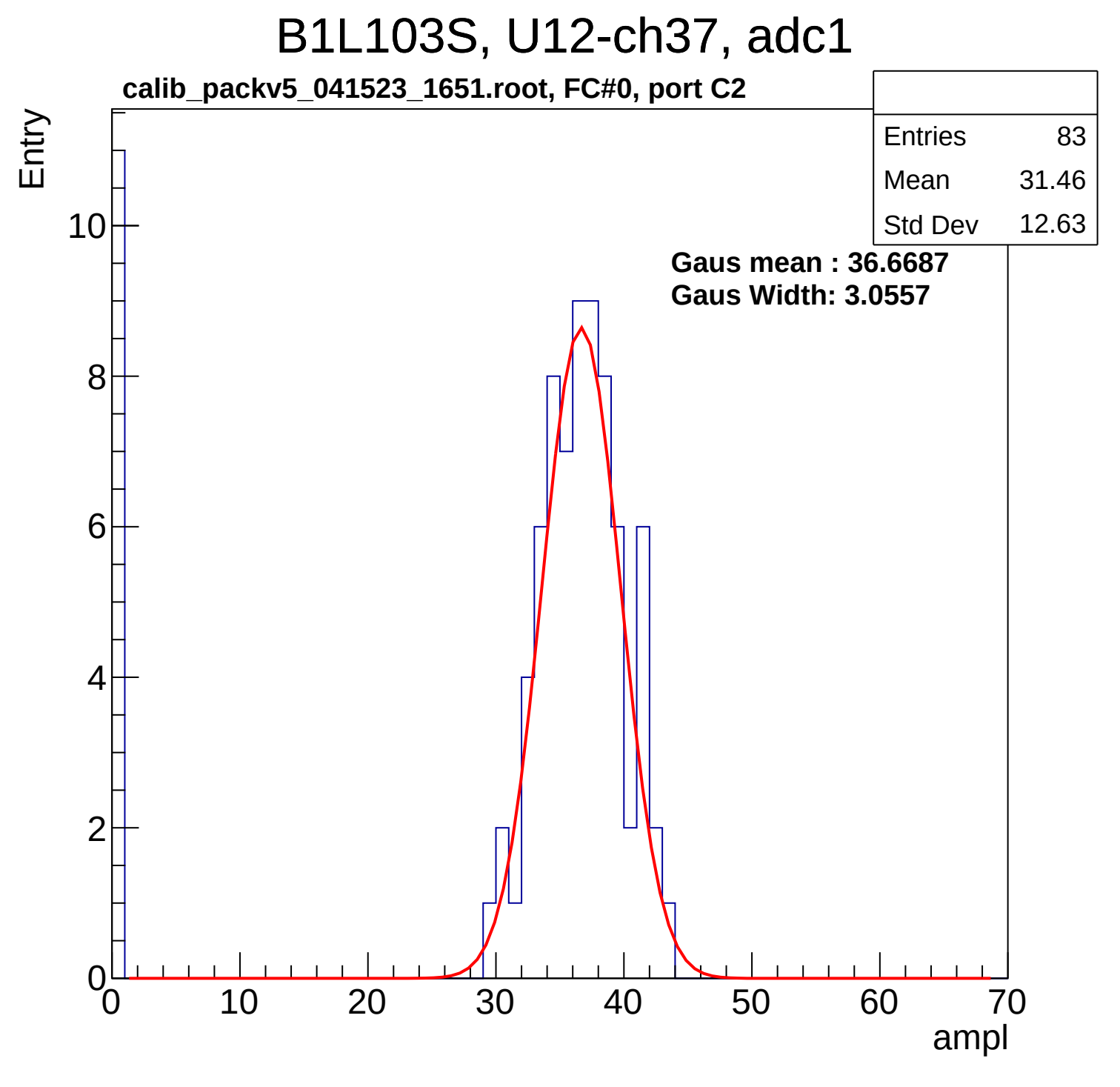
B1L103S, U12-ch37, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 31.46
Std Dev 12.63
Gaus mean : 36.6687
Gaus Width: 3.0557
Entry
ampl
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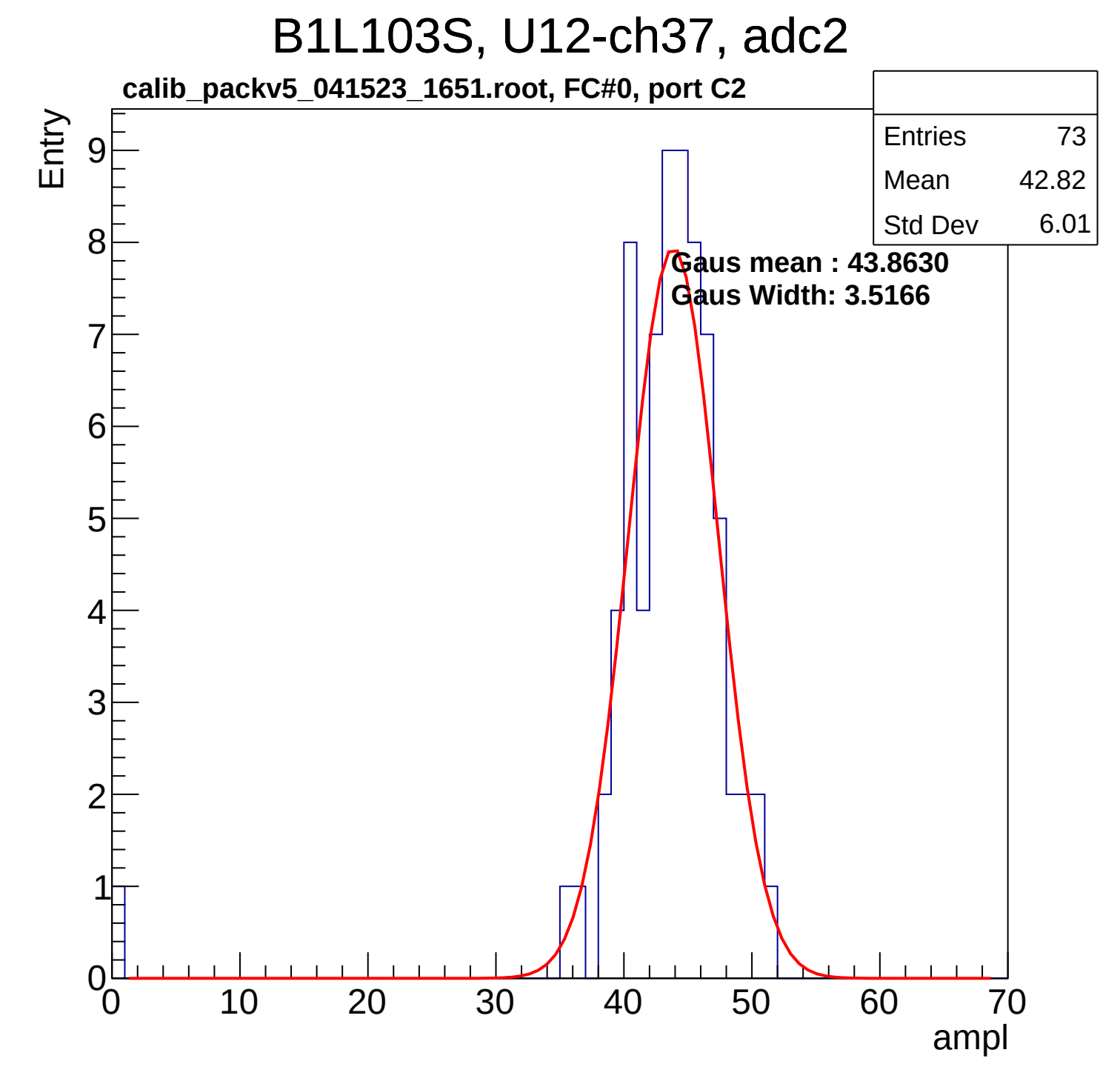
B1L103S, U12-ch37, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 42.82
Std Dev 6.01
Gaus mean : 43.8630
Gaus Width: 3.5166
Entry
ampl
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2
3
4
5
6
7
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9
0
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60
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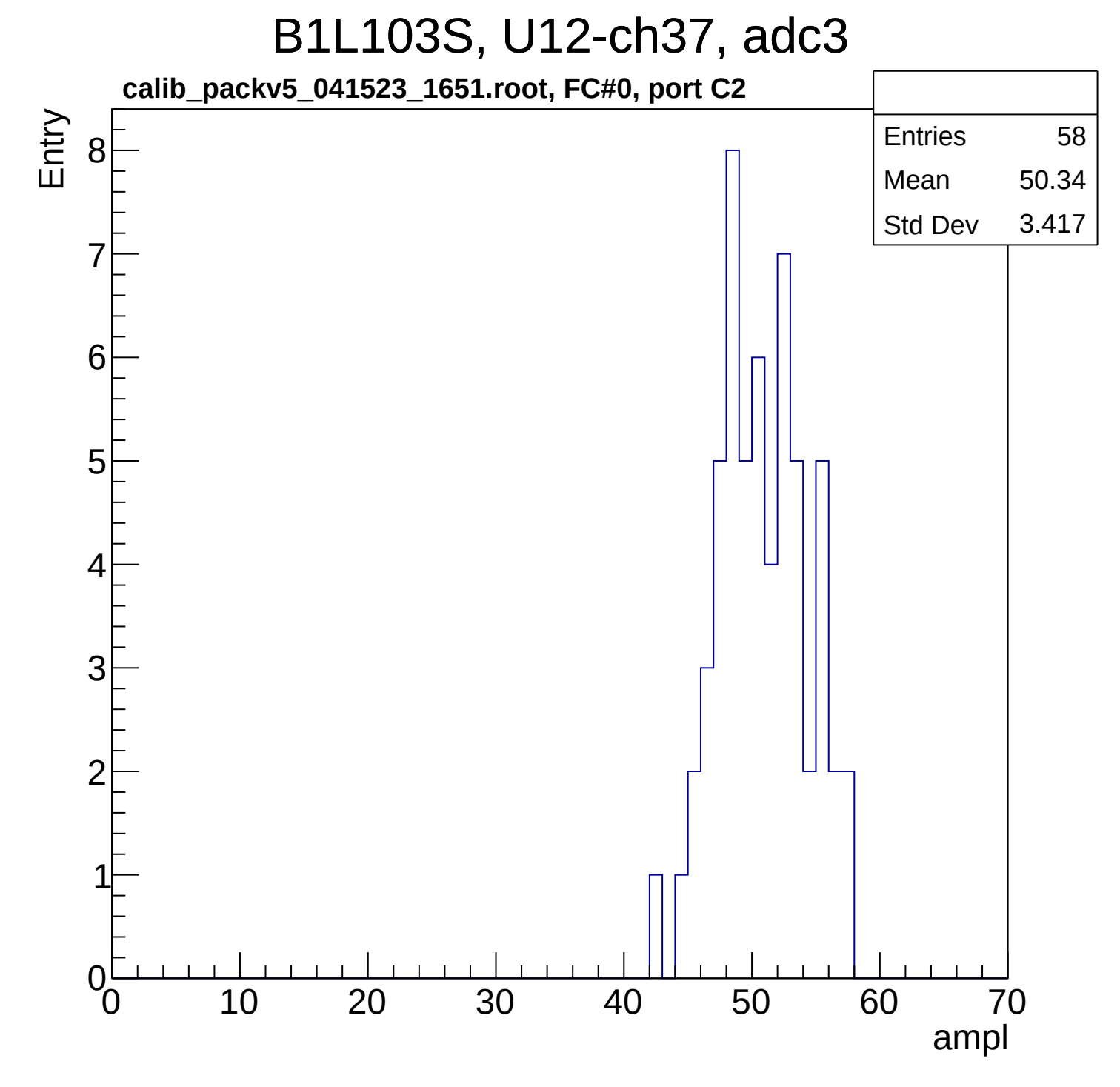
B1L103S, U12-ch37, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 50.34
Std Dev 3.417
Entry
ampl
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60
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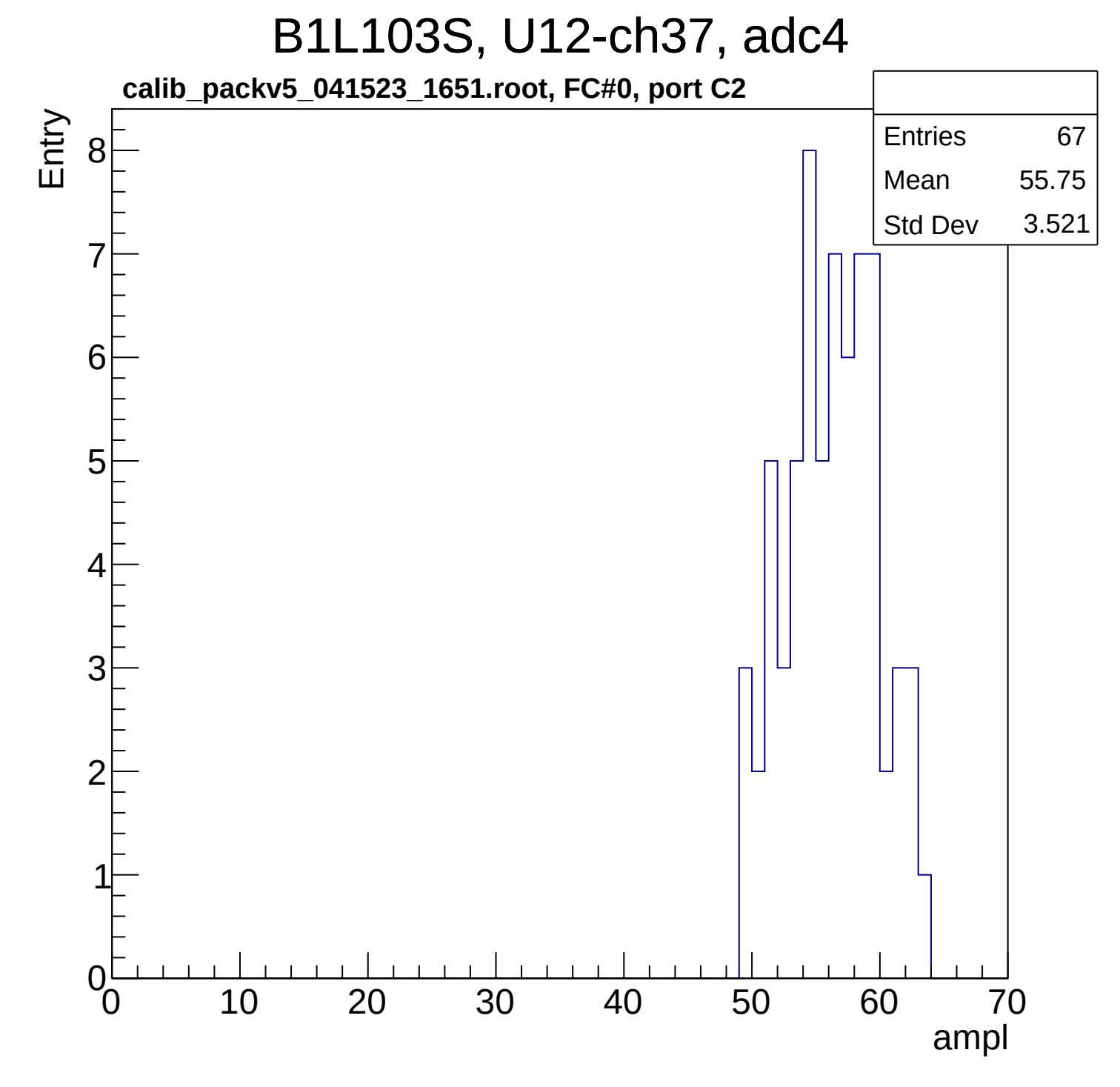
B1L103S, U12-ch37, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 55.75
Std Dev 3.521
Entry
ampl
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4
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0
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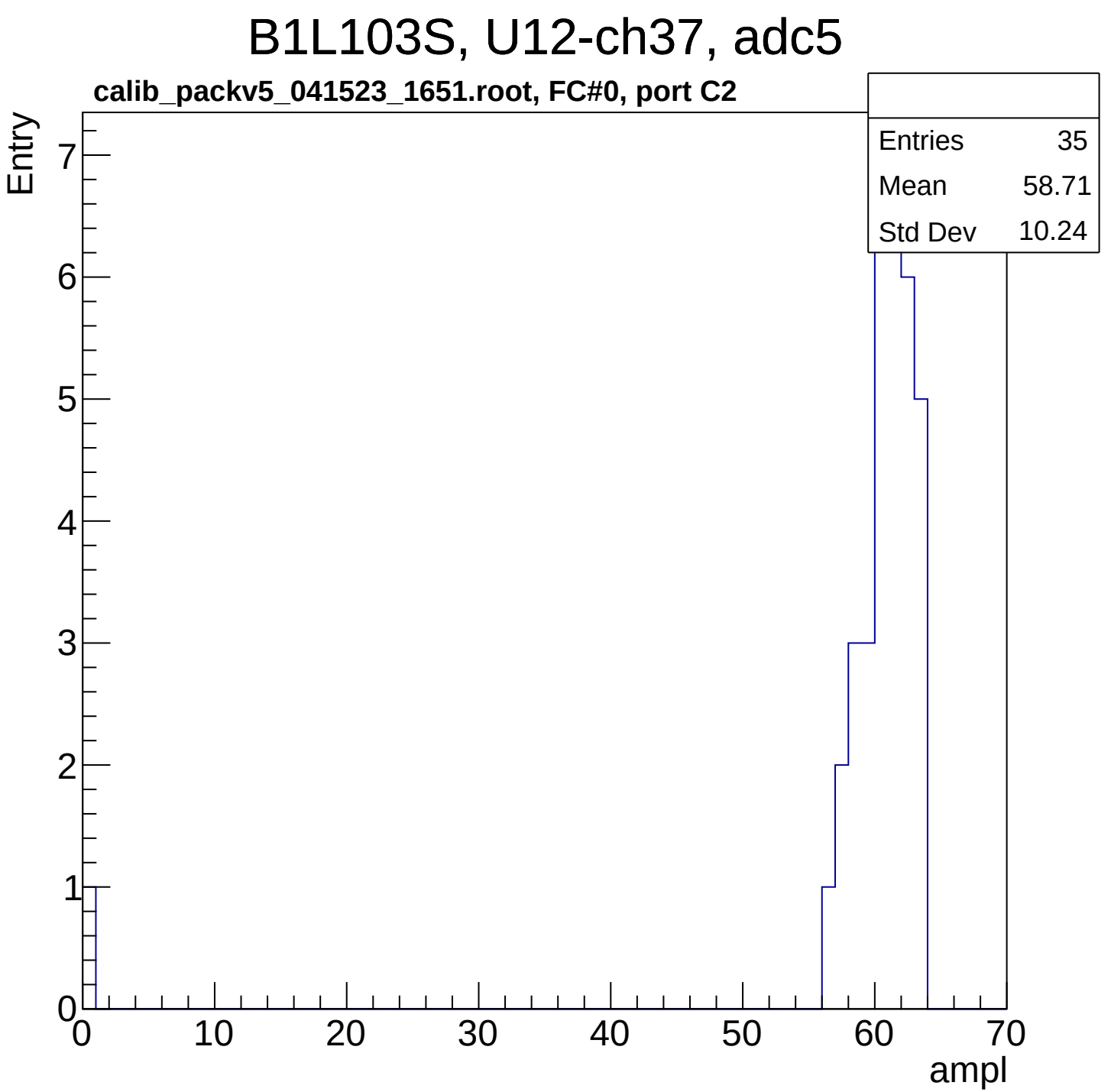
B1L103S, U12-ch37, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 58.71
Std Dev 10.24
Entry
ampl
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4
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0
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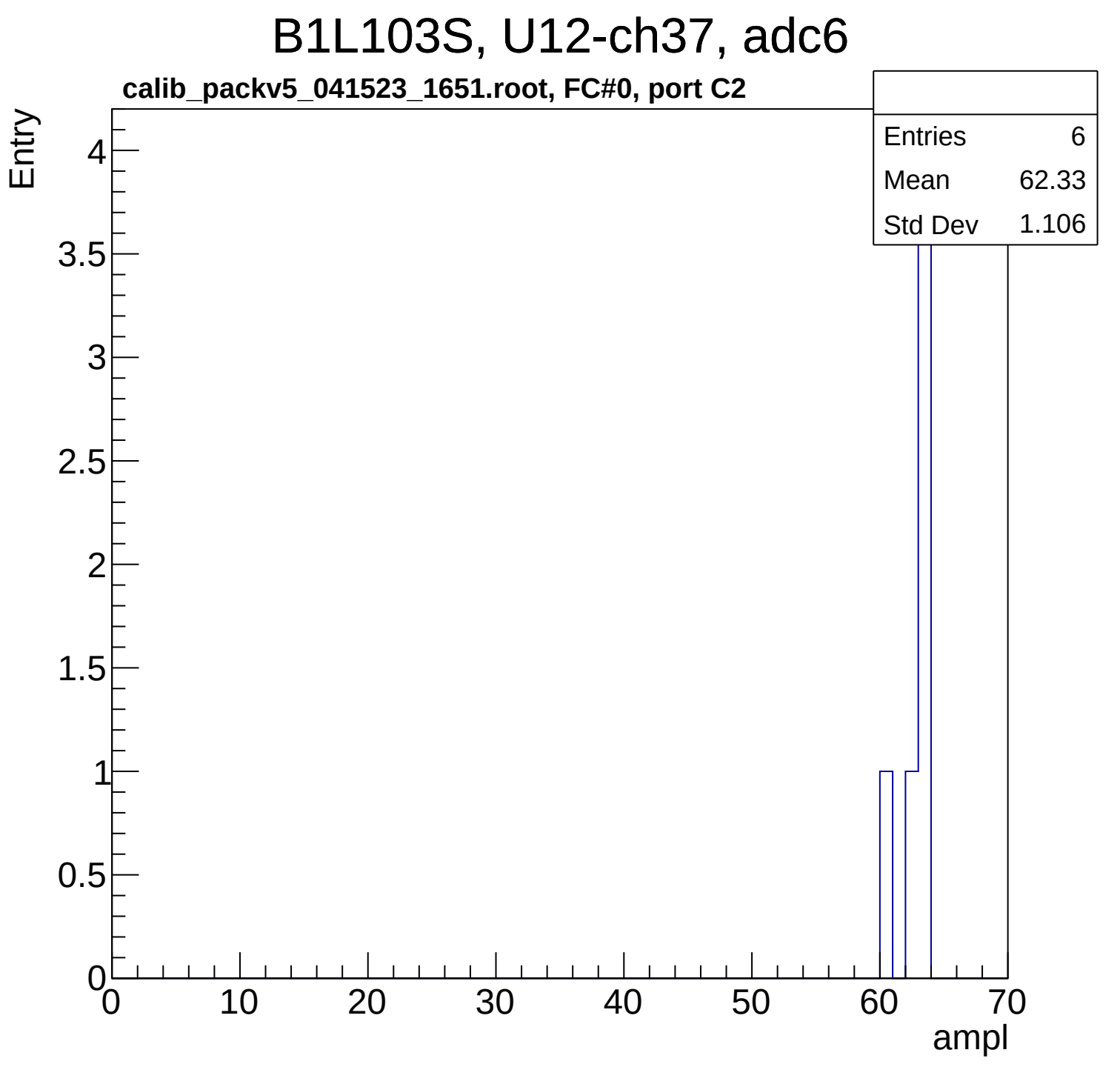
B1L103S, U12-ch37, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.33
Std Dev 1.106
Entry
ampl
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1.5
2
2.5
3
3.5
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0
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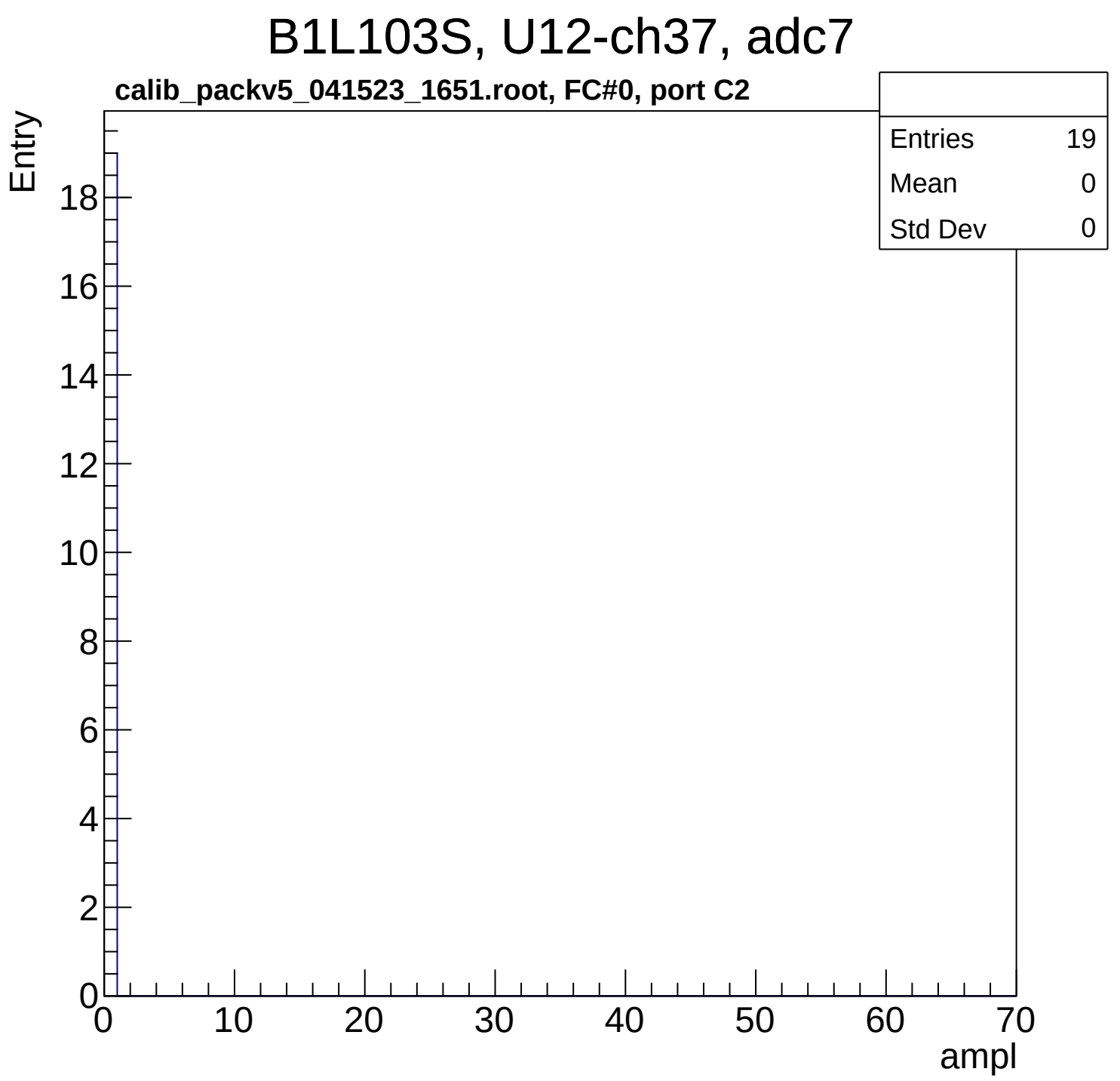
B1L103S, U12-ch37, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
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20
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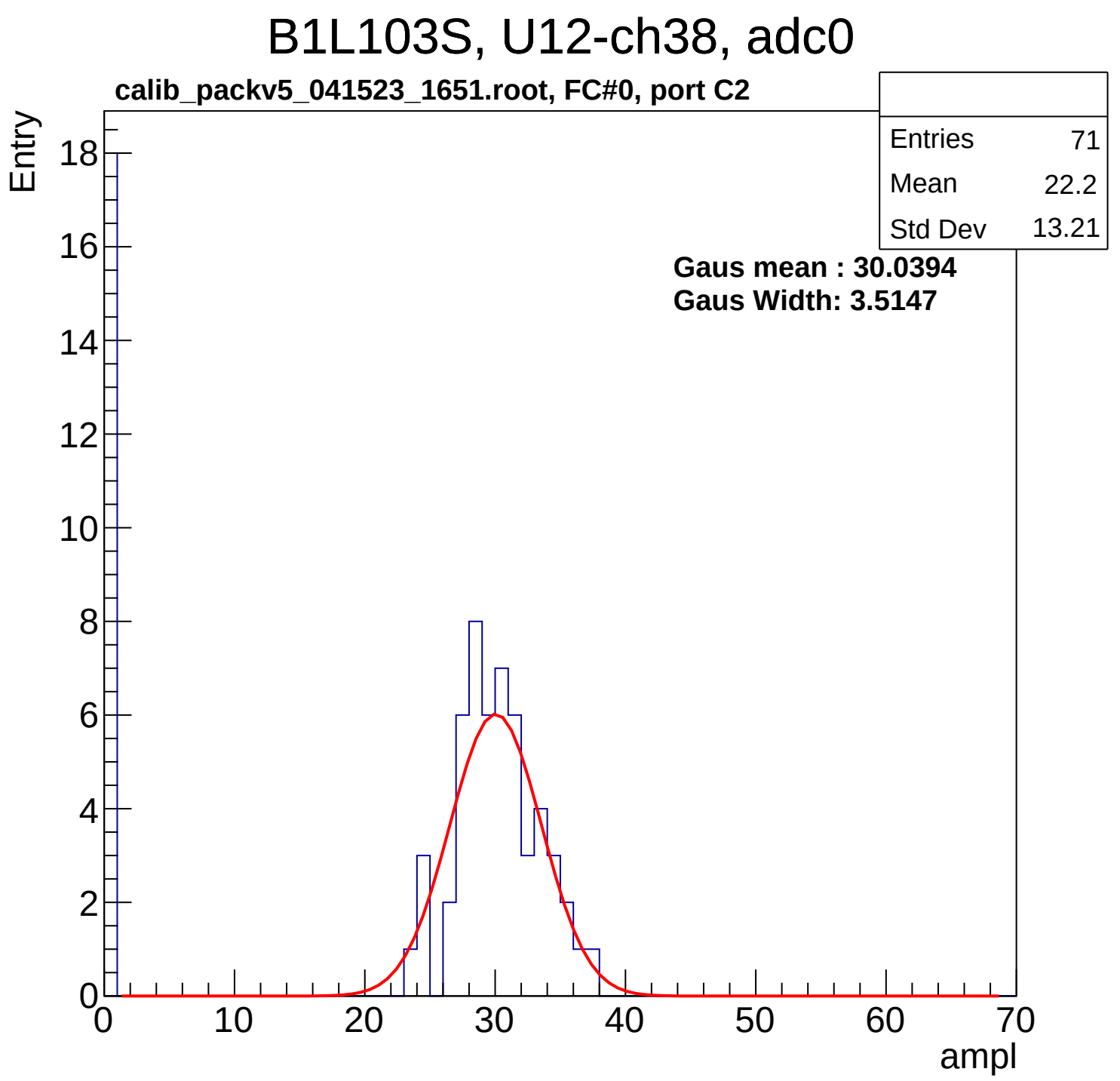
50
60
70
ampl


B1L103S, U12-ch38, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 22.2
Std Dev 13.21
Gaus mean : 30.0394
Gaus Width: 3.5147
Entry
ampl
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6
8
10
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0
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60
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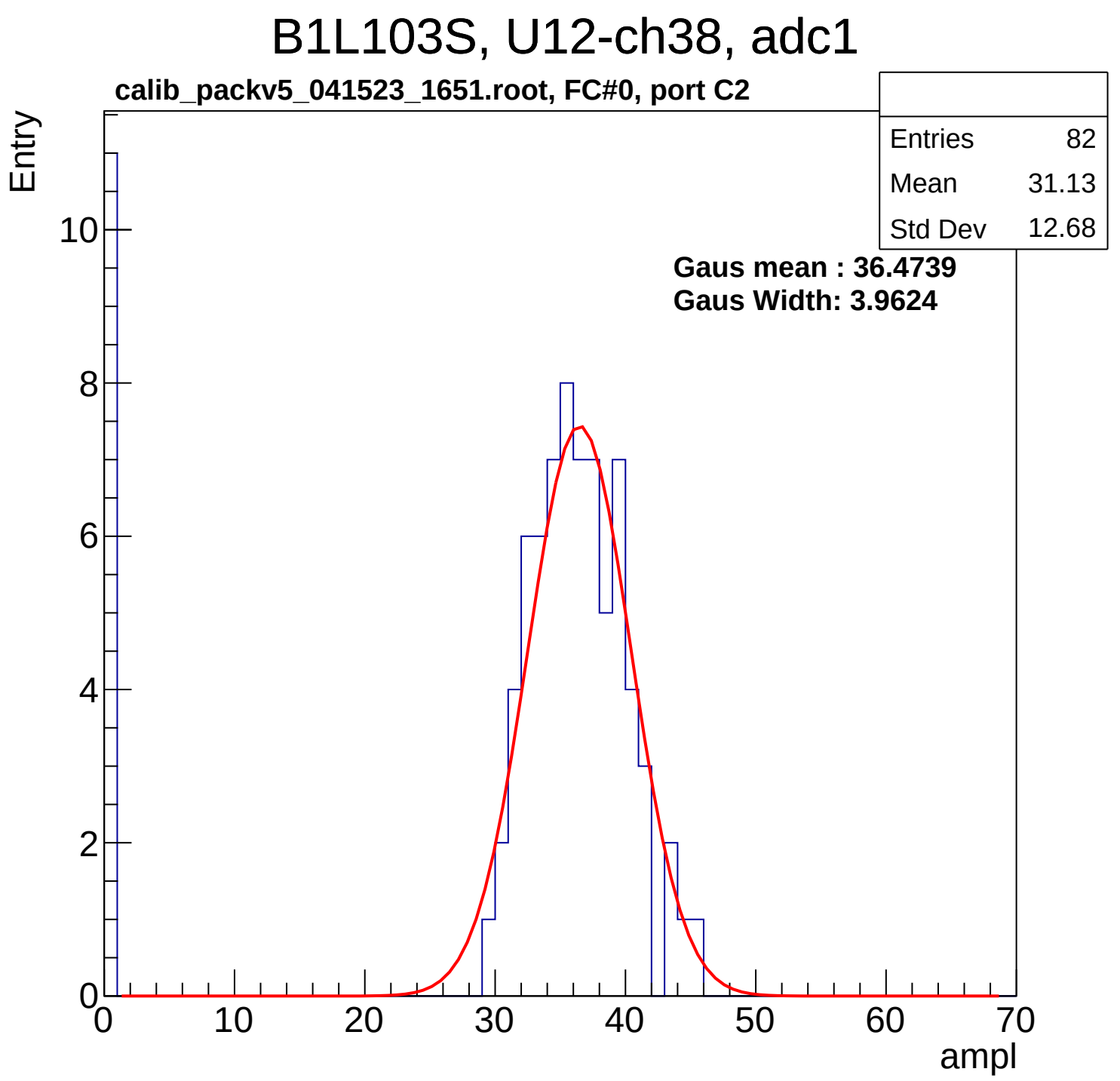
B1L103S, U12-ch38, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 31.13
Std Dev 12.68
Gaus mean : 36.4739
Gaus Width: 3.9624
Entry
ampl
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2
4
6
8
10
0
10
20
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40
50
60
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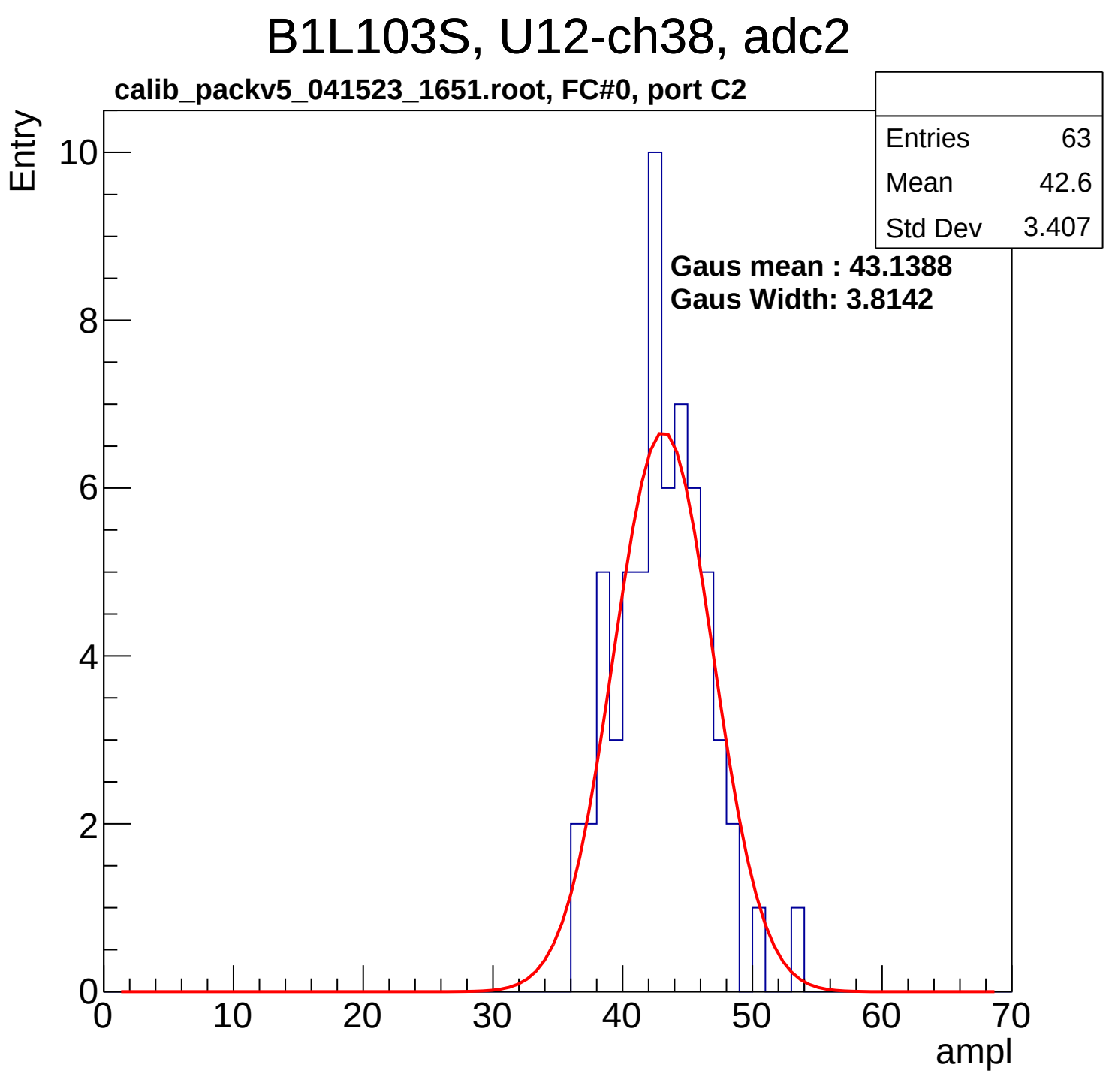
B1L103S, U12-ch38, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 42.6
Std Dev 3.407
Gaus mean : 43.1388
Gaus Width: 3.8142
Entry
ampl
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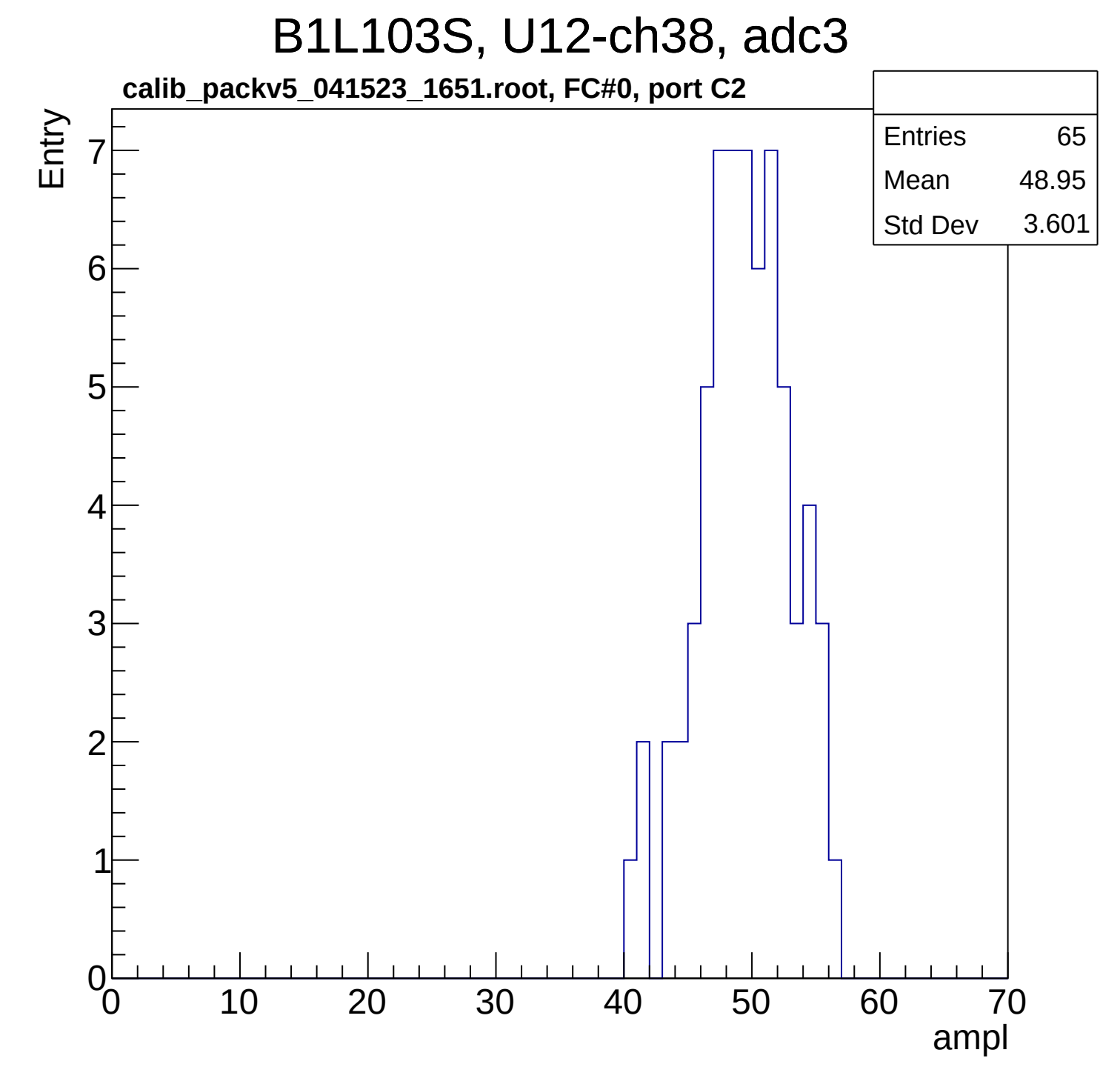
B1L103S, U12-ch38, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 48.95
Std Dev 3.601
Entry
ampl
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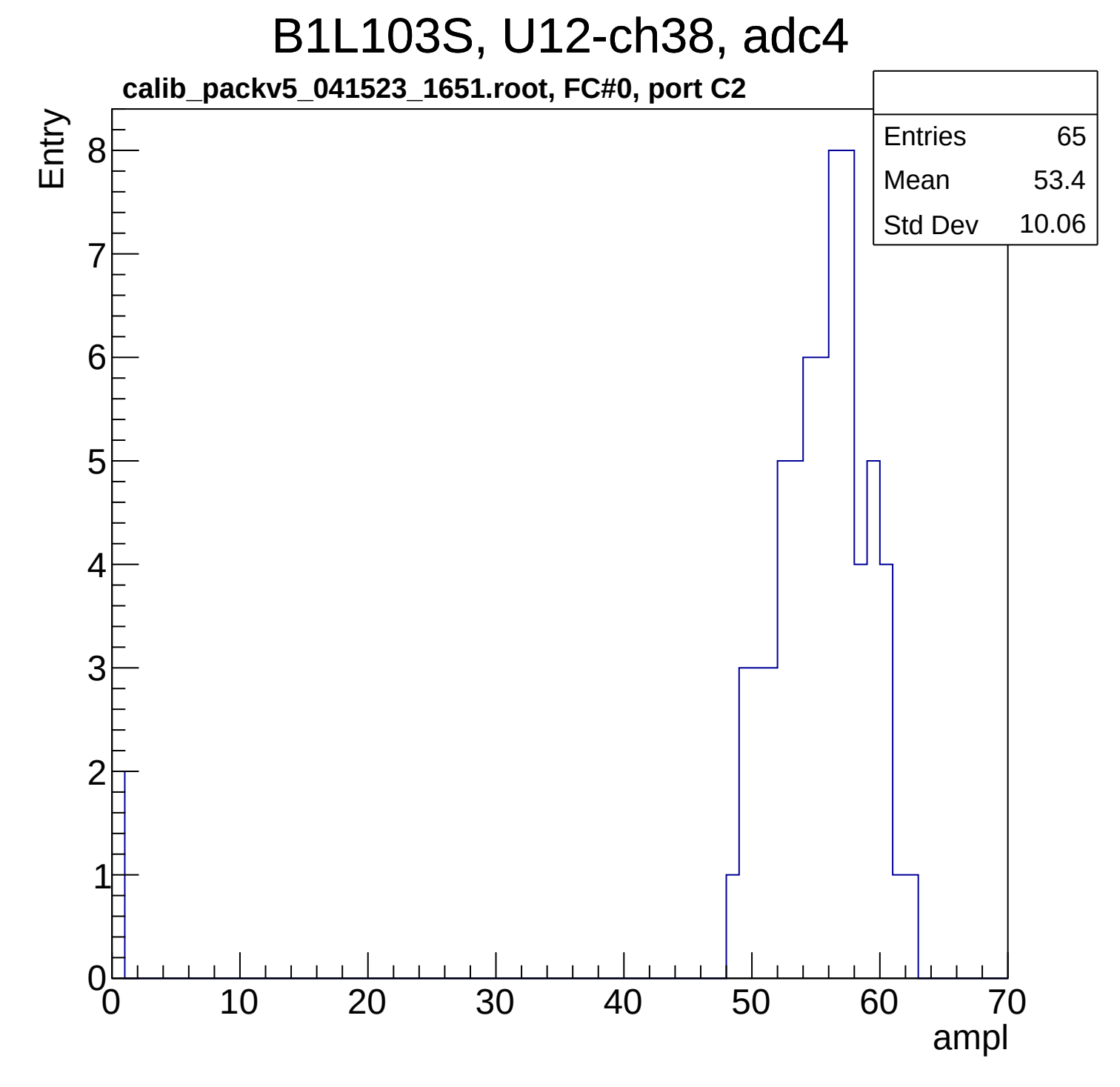
B1L103S, U12-ch38, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 53.4
Std Dev 10.06
Entry
ampl
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40
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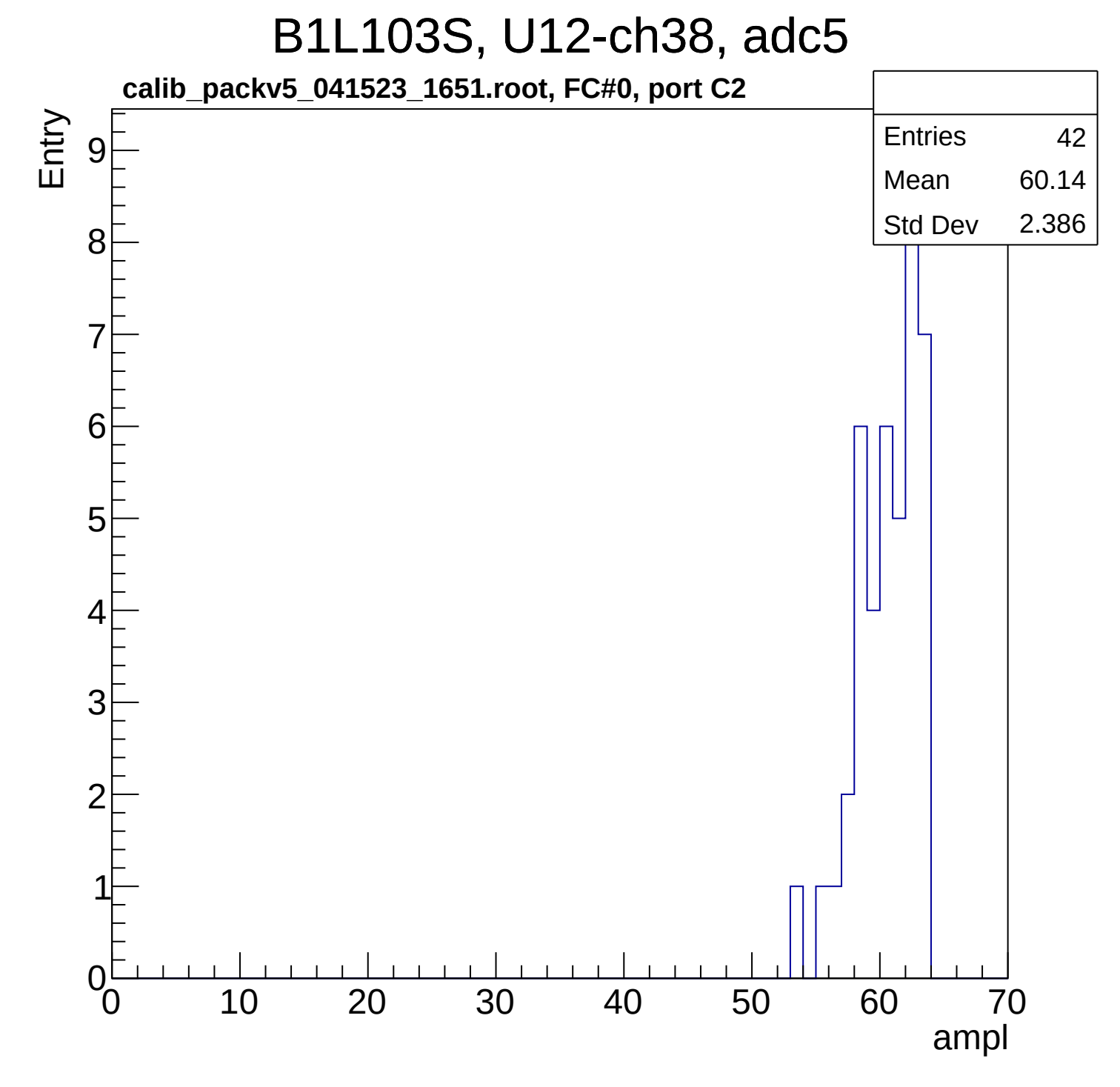
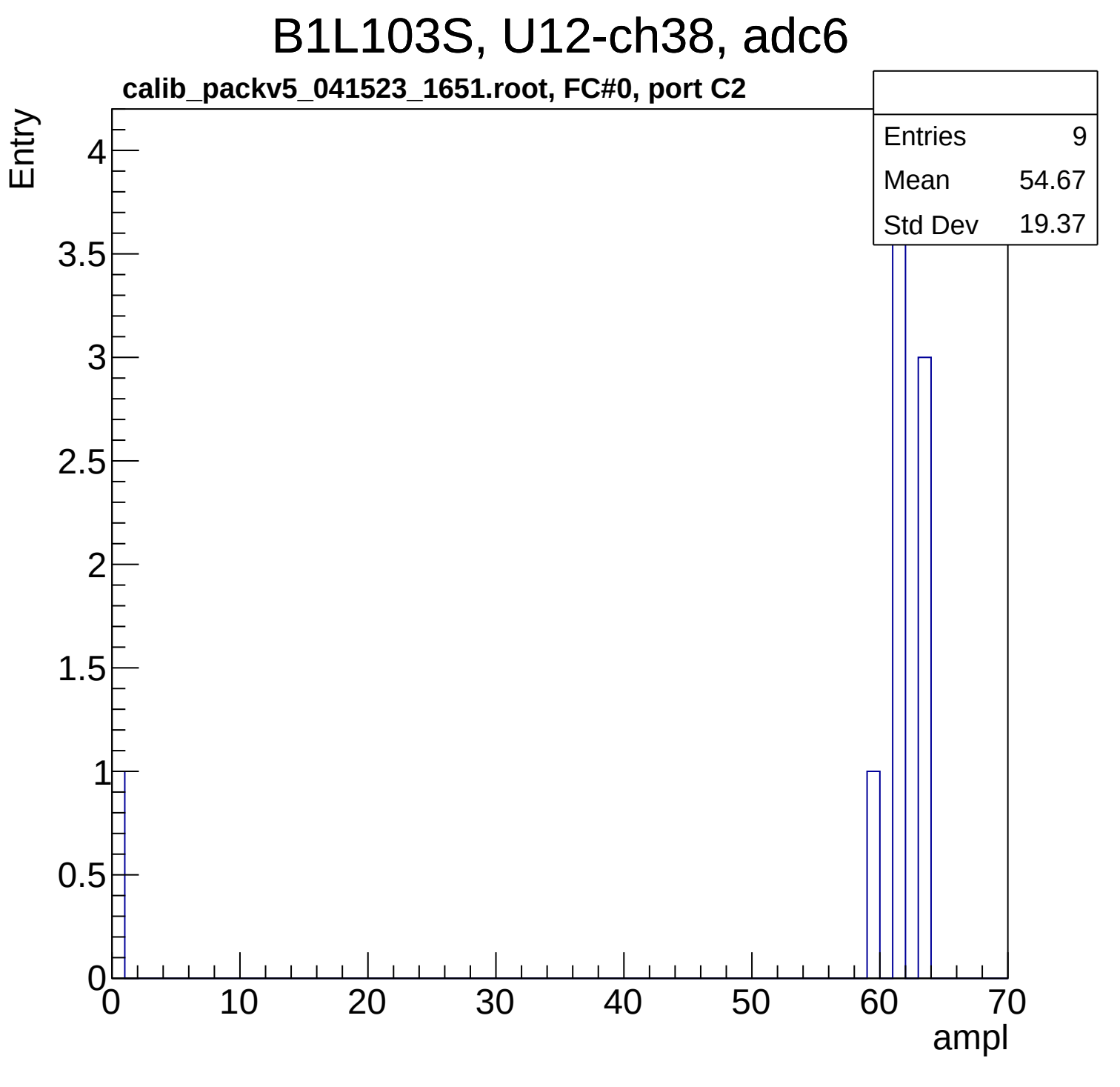

B1L103S, U12-ch38, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 60.14
Std Dev 2.386
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U12-ch38, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 54.67
Std Dev 19.37
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
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40
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60
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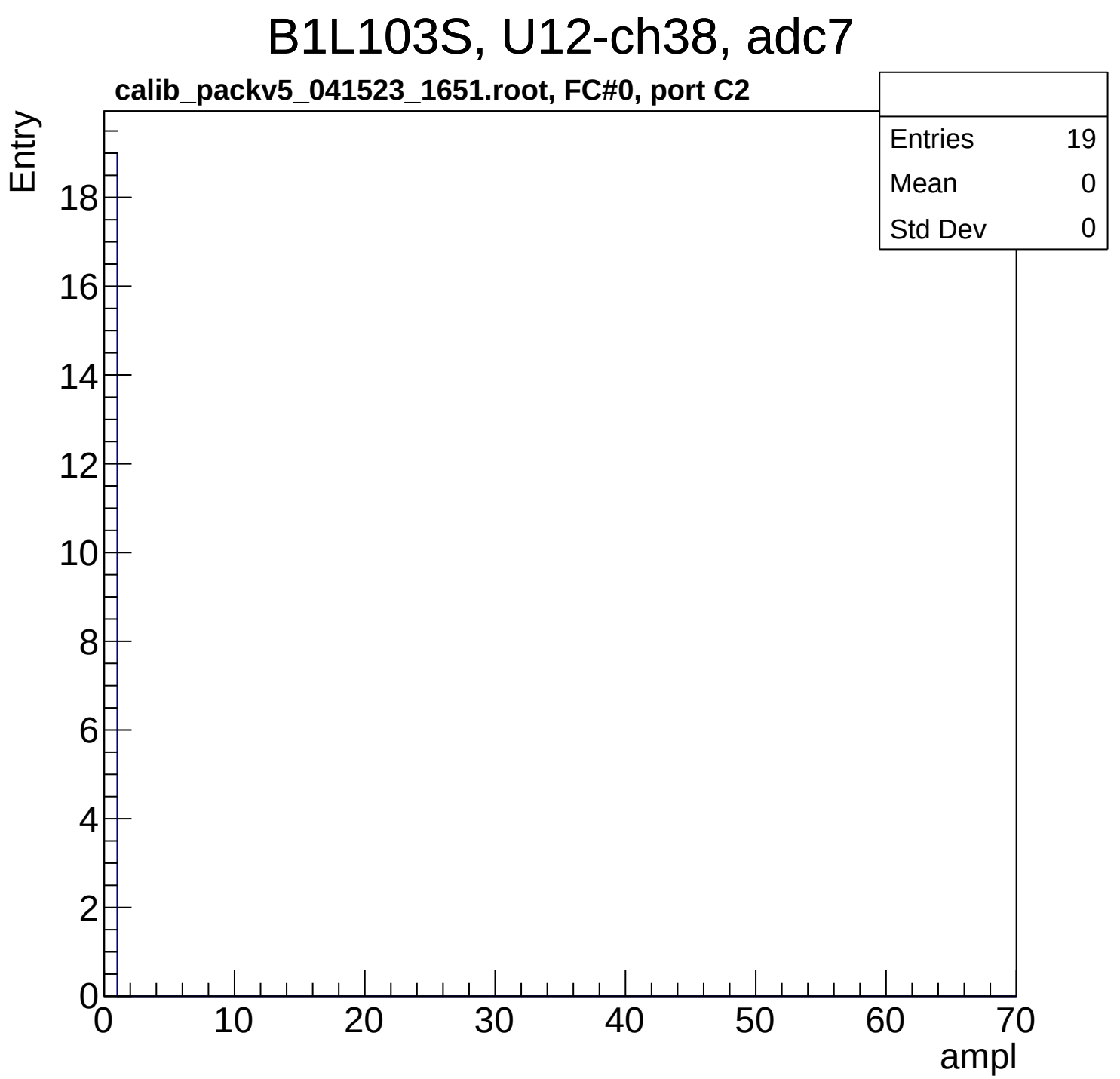
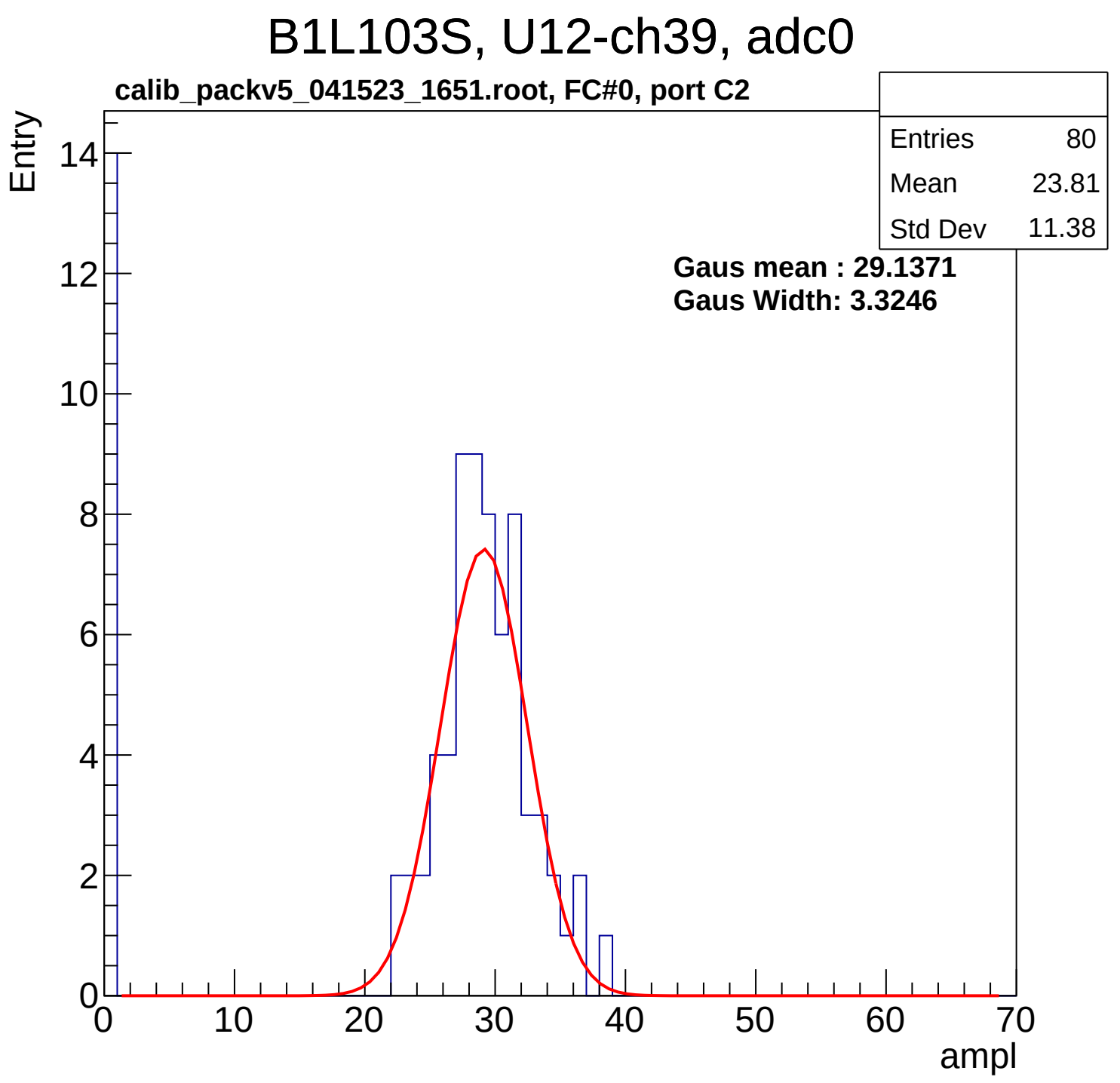

B1L103S, U12-ch38, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch39, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 23.81
Std Dev 11.38
Gaus mean : 29.1371
Gaus Width: 3.3246
Entry
ampl
0
2
4
6
8
10
12
14
0
10
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40
50
60
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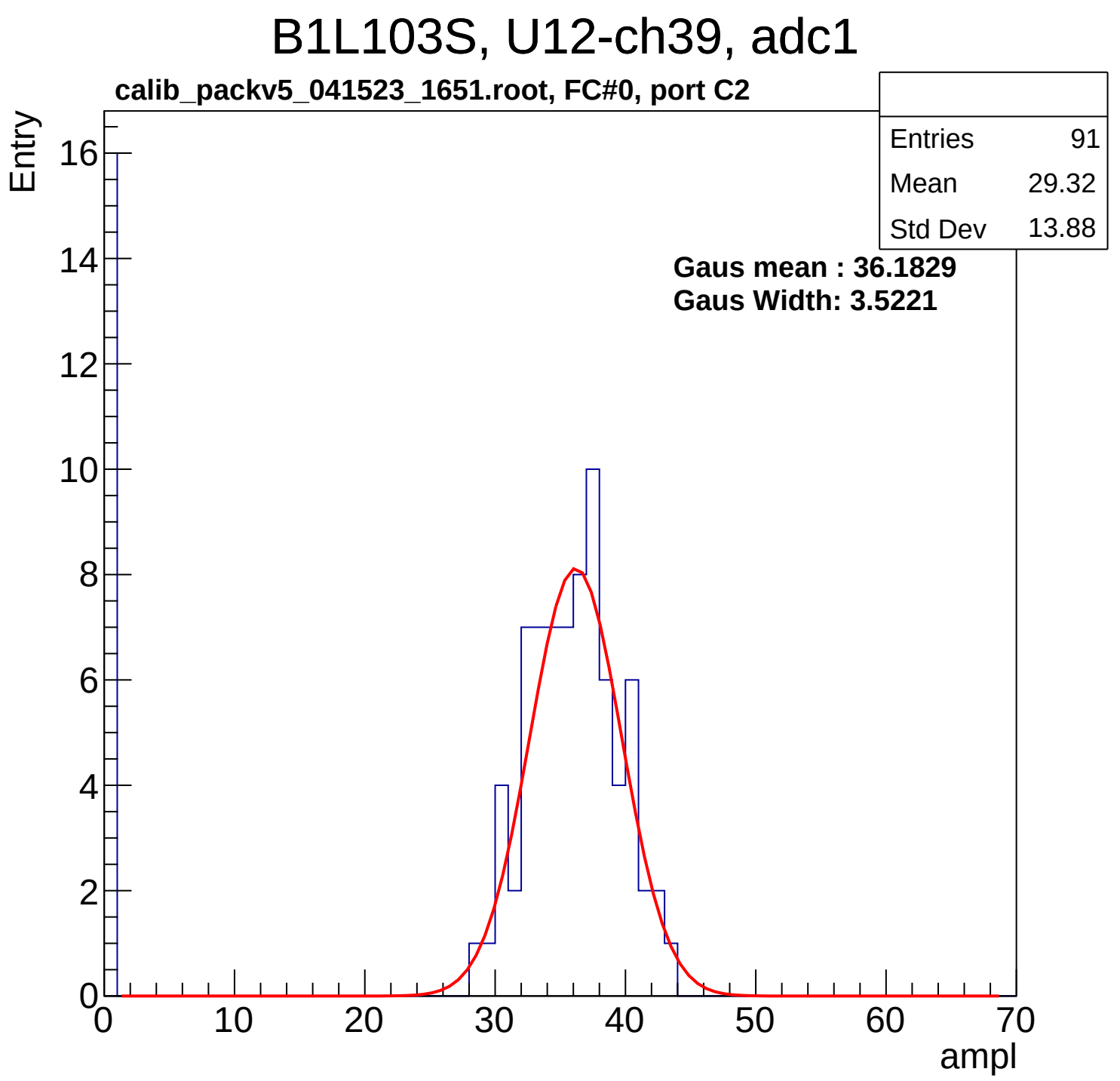
B1L103S, U12-ch39, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 29.32
Std Dev 13.88
Gaus mean : 36.1829
Gaus Width: 3.5221
Entry
ampl
0
2
4
6
8
10
12
14
16
0
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40
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60
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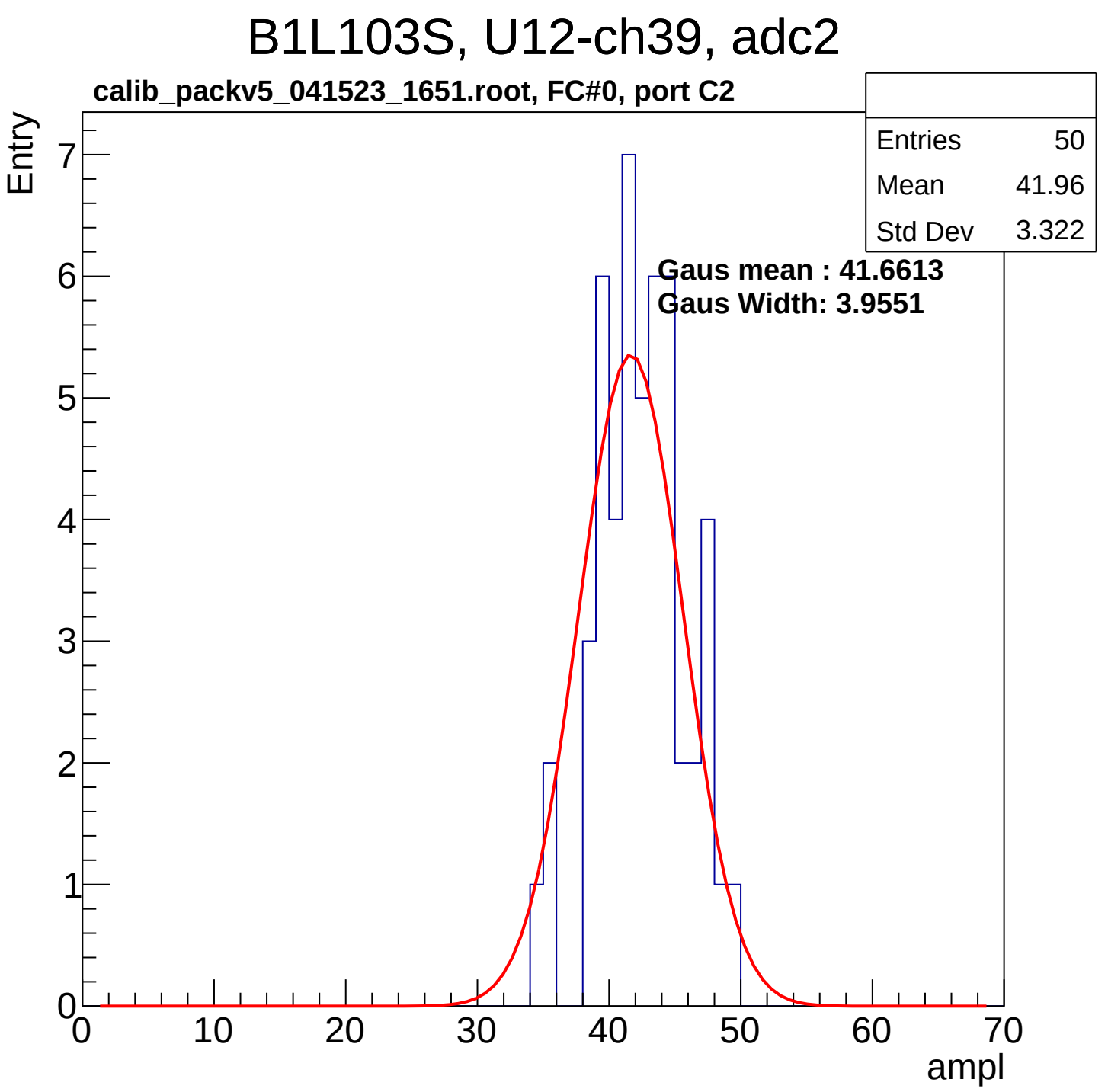
B1L103S, U12-ch39, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 41.96
Std Dev 3.322
Gaus mean : 41.6613
Gaus Width: 3.9551
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
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60
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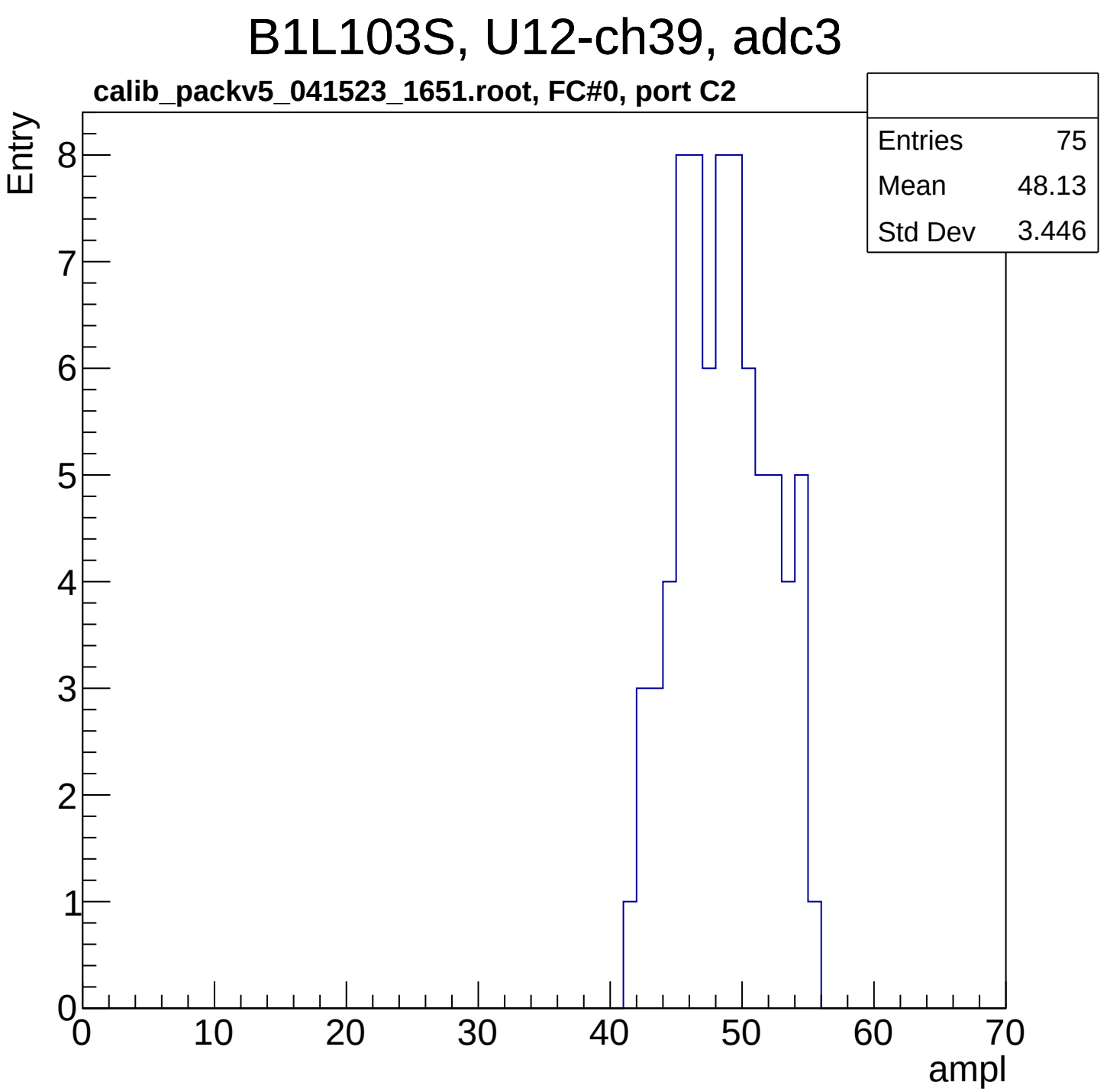
B1L103S, U12-ch39, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 48.13
Std Dev 3.446
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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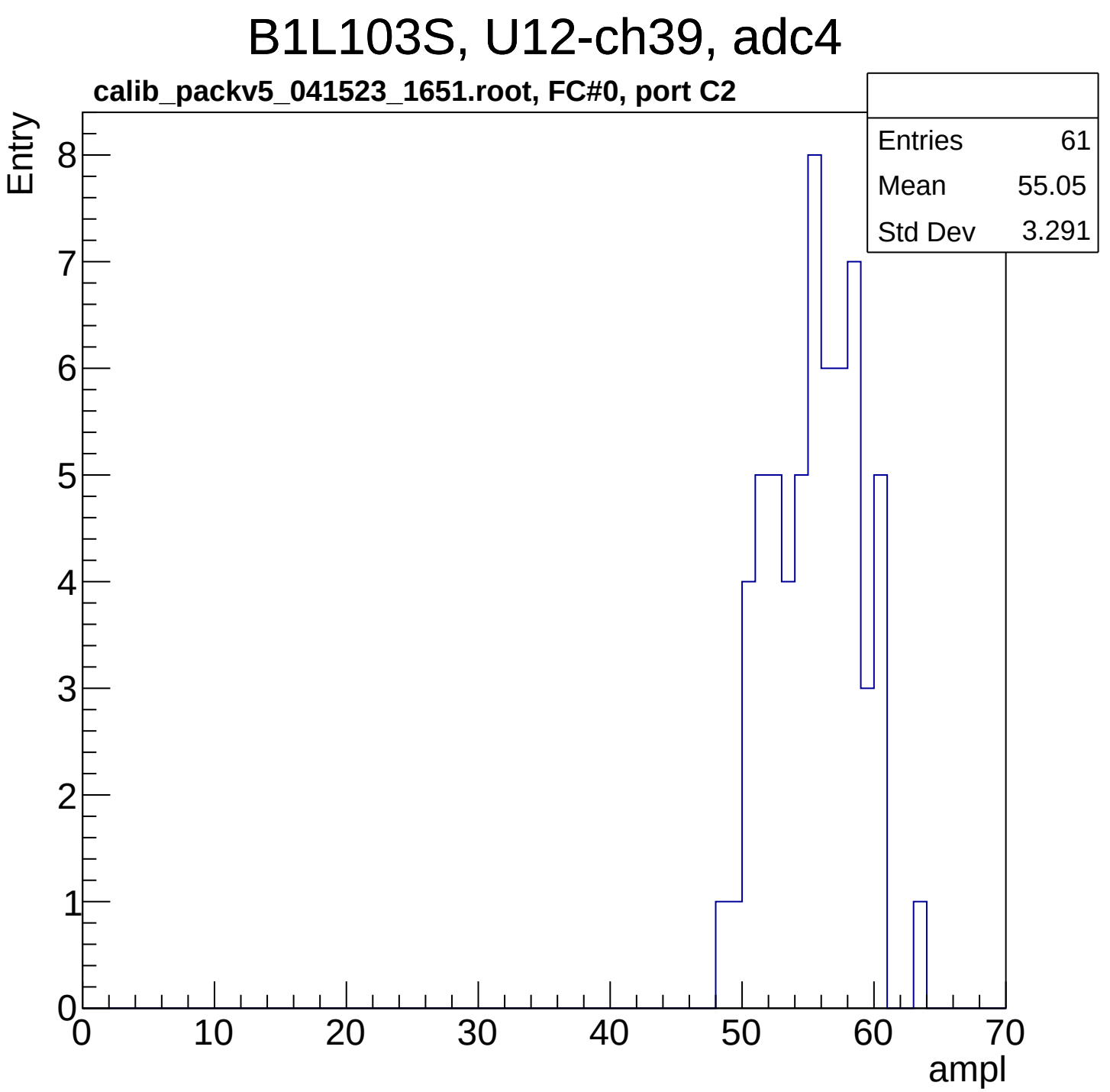
B1L103S, U12-ch39, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 55.05
Std Dev 3.291
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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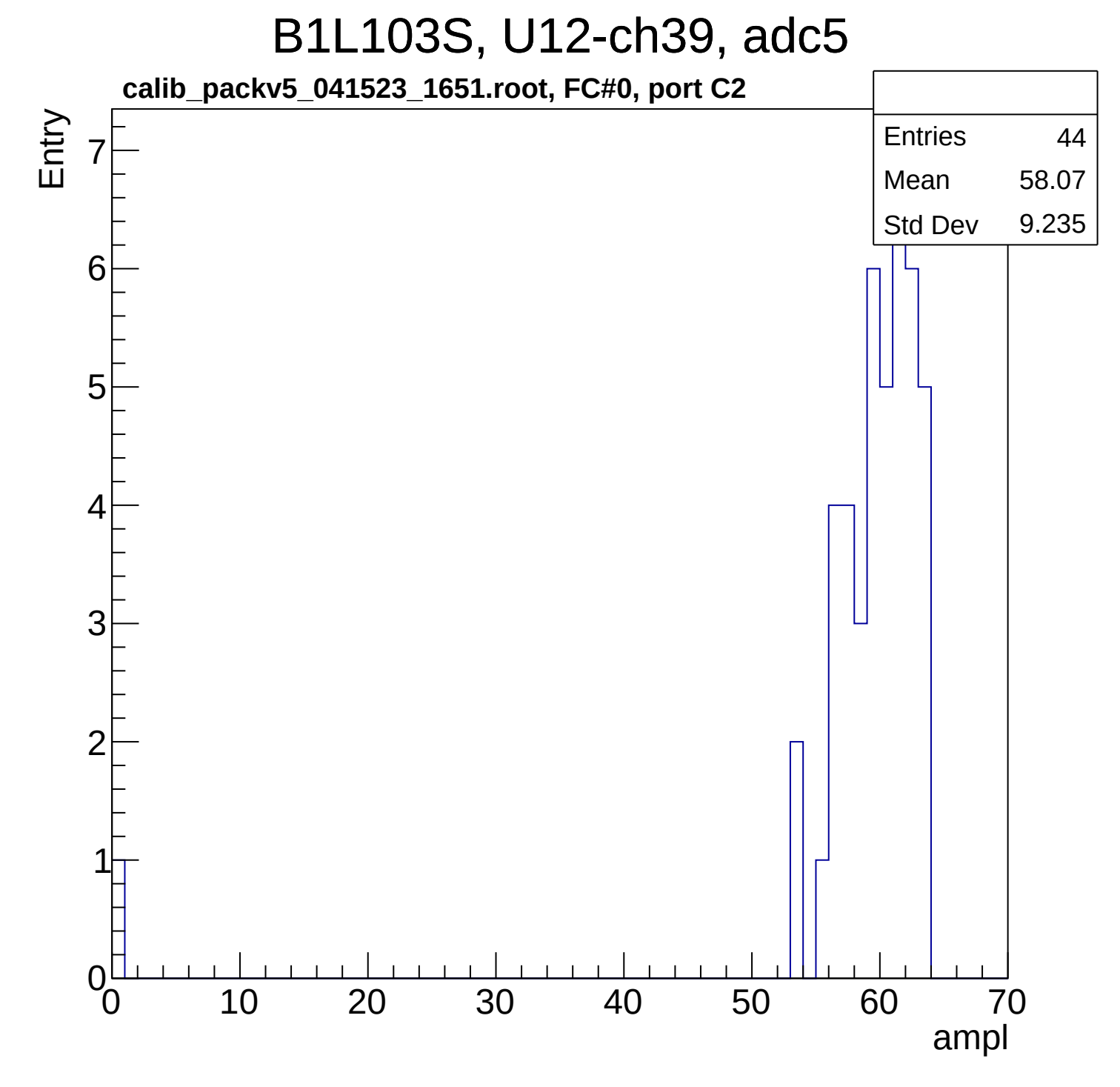
B1L103S, U12-ch39, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 58.07
Std Dev 9.235
Entry
ampl
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1
2
3
4
5
6
7
0
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40
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60
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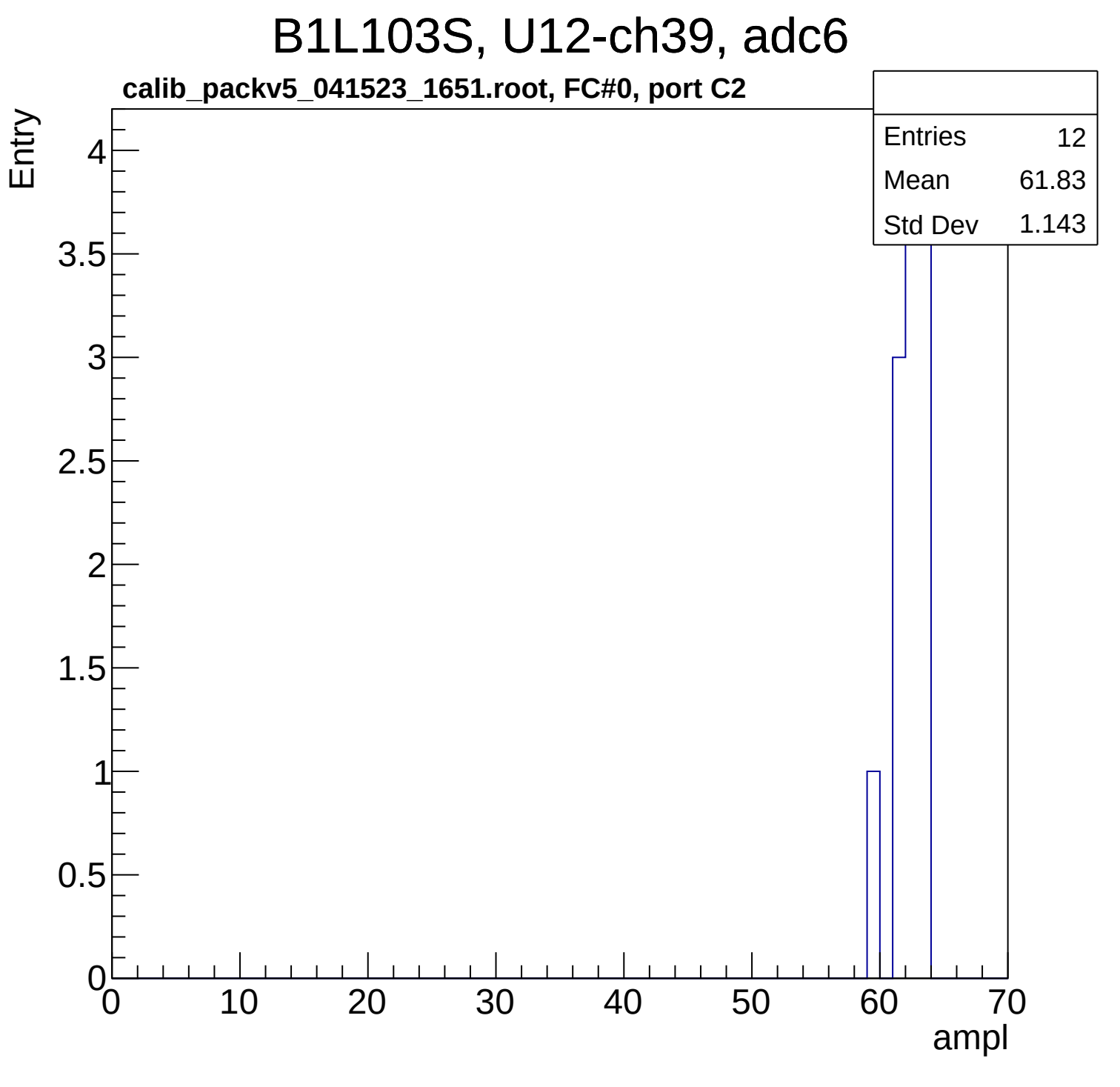
B1L103S, U12-ch39, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.83
Std Dev 1.143
Entry
ampl
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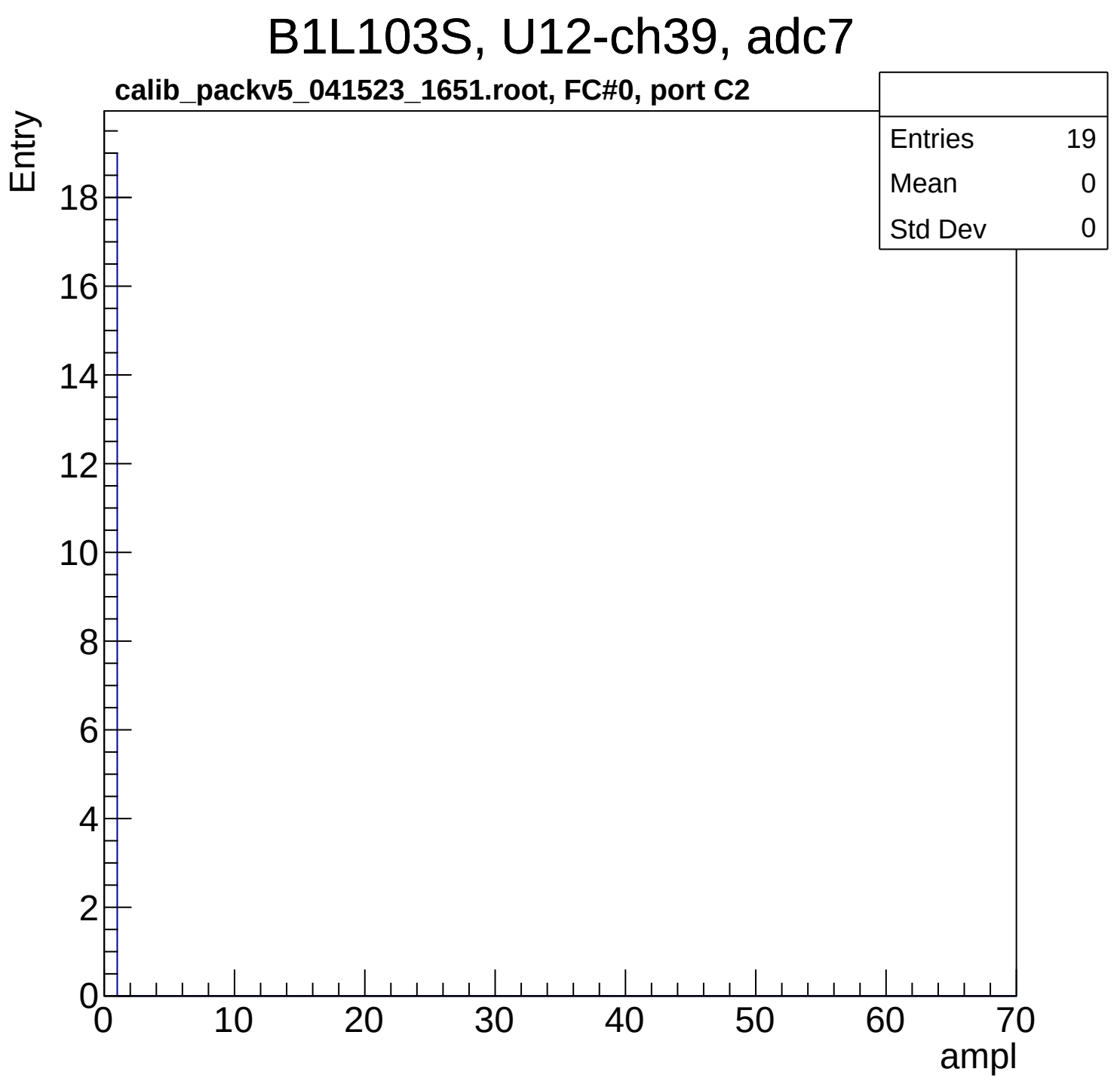
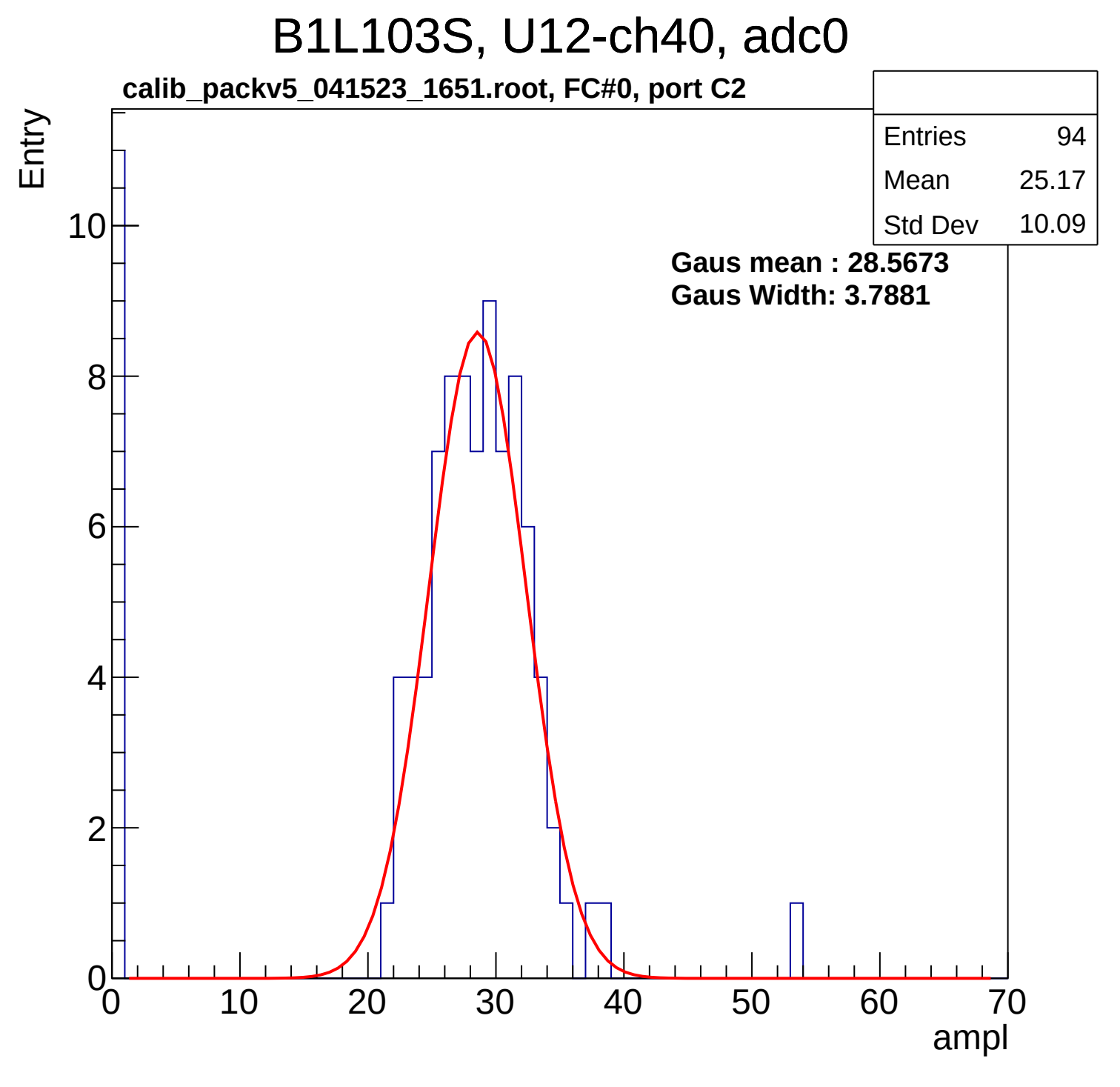
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U12-ch39, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch40, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 25.17
Std Dev 10.09
Gaus mean : 28.5673
Gaus Width: 3.7881
Entry
ampl
0
2
4
6
8
10
0
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20
30
40
50
60
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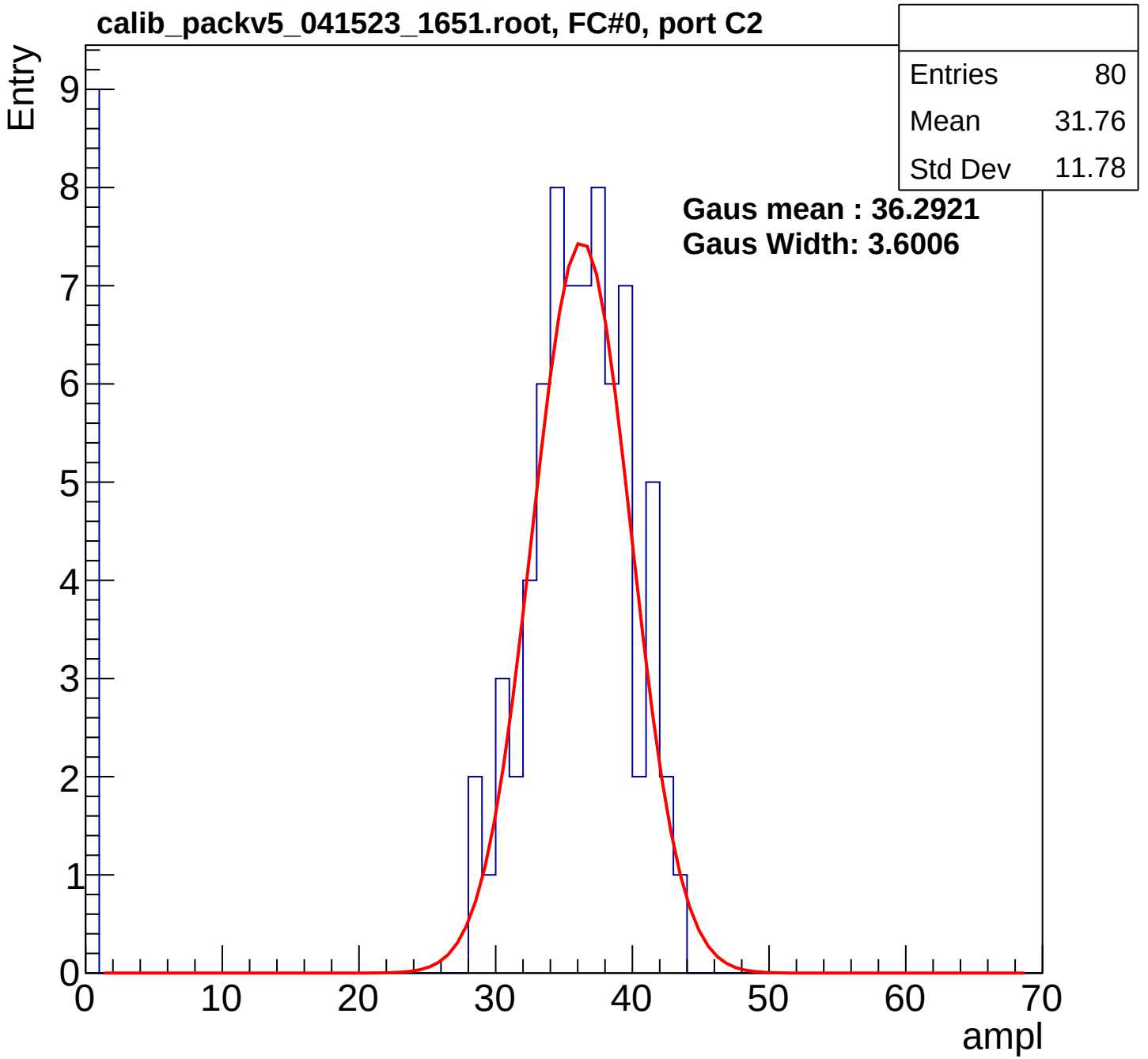
B1L103S, U12-ch40, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 31.76
Std Dev 11.78
Gaus mean : 36.2921
Gaus Width: 3.6006
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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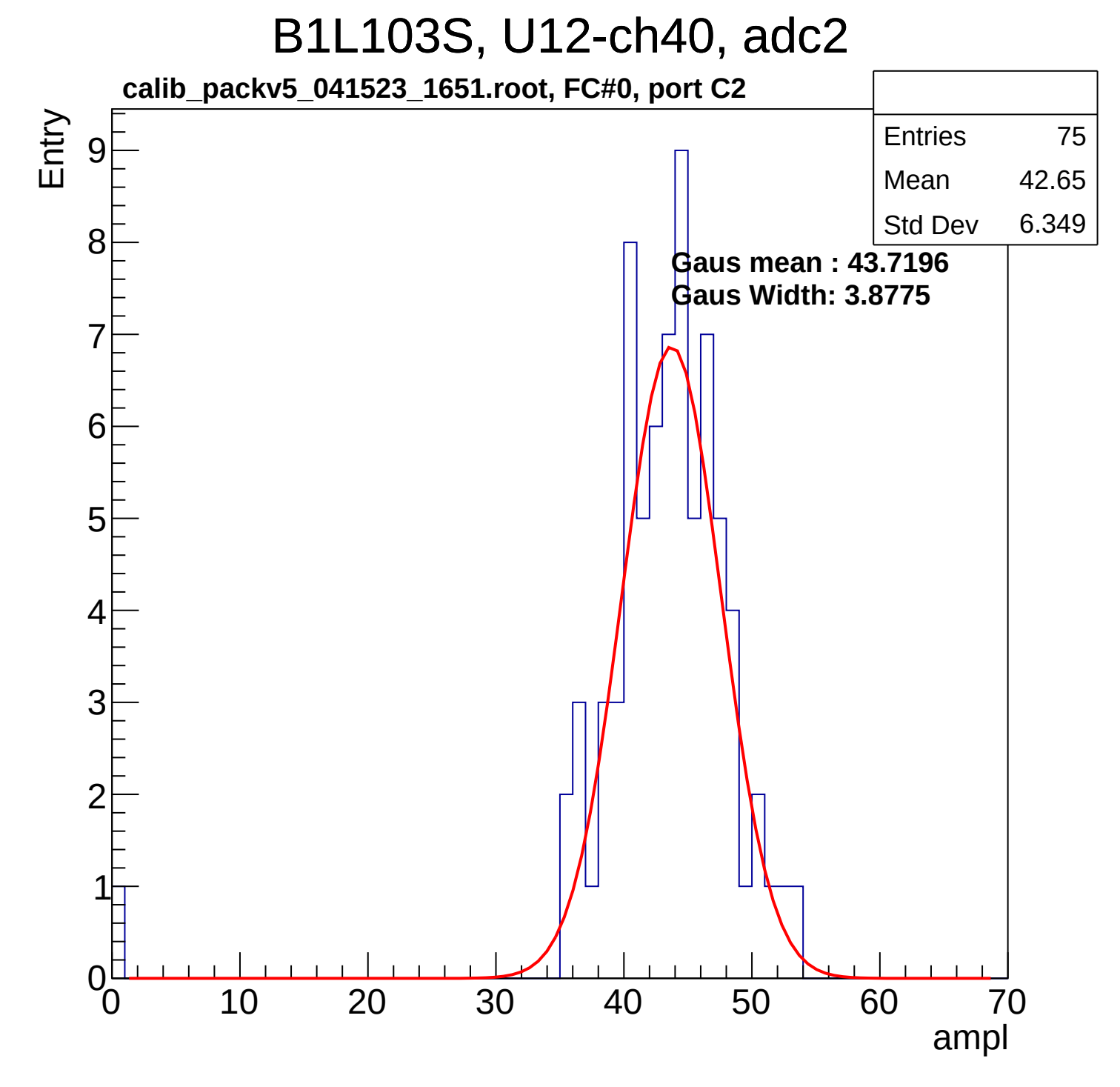
B1L103S, U12-ch40, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 42.65
Std Dev 6.349
Gaus mean : 43.7196
Gaus Width: 3.8775
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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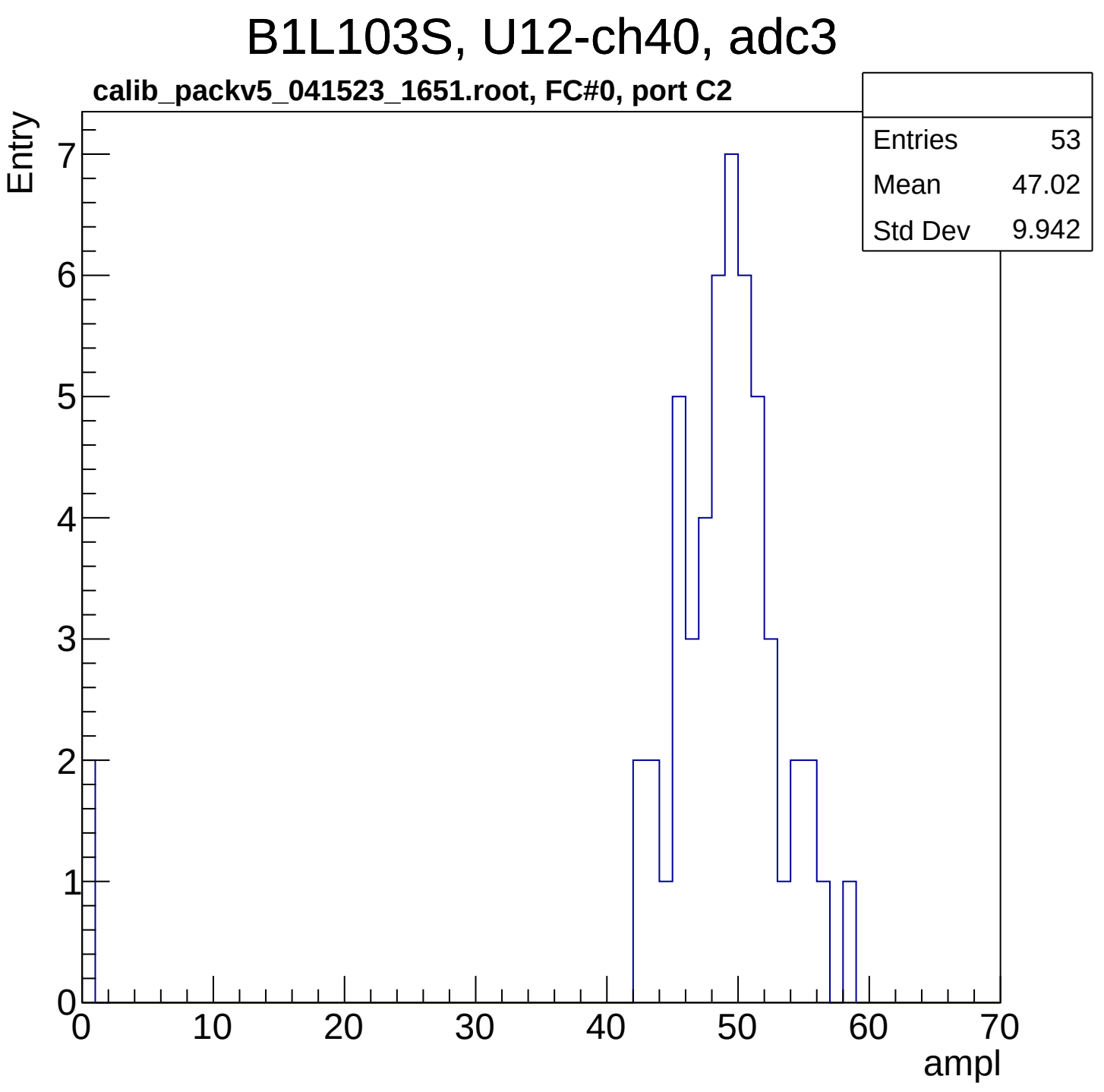
B1L103S, U12-ch40, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 47.02
Std Dev 9.942
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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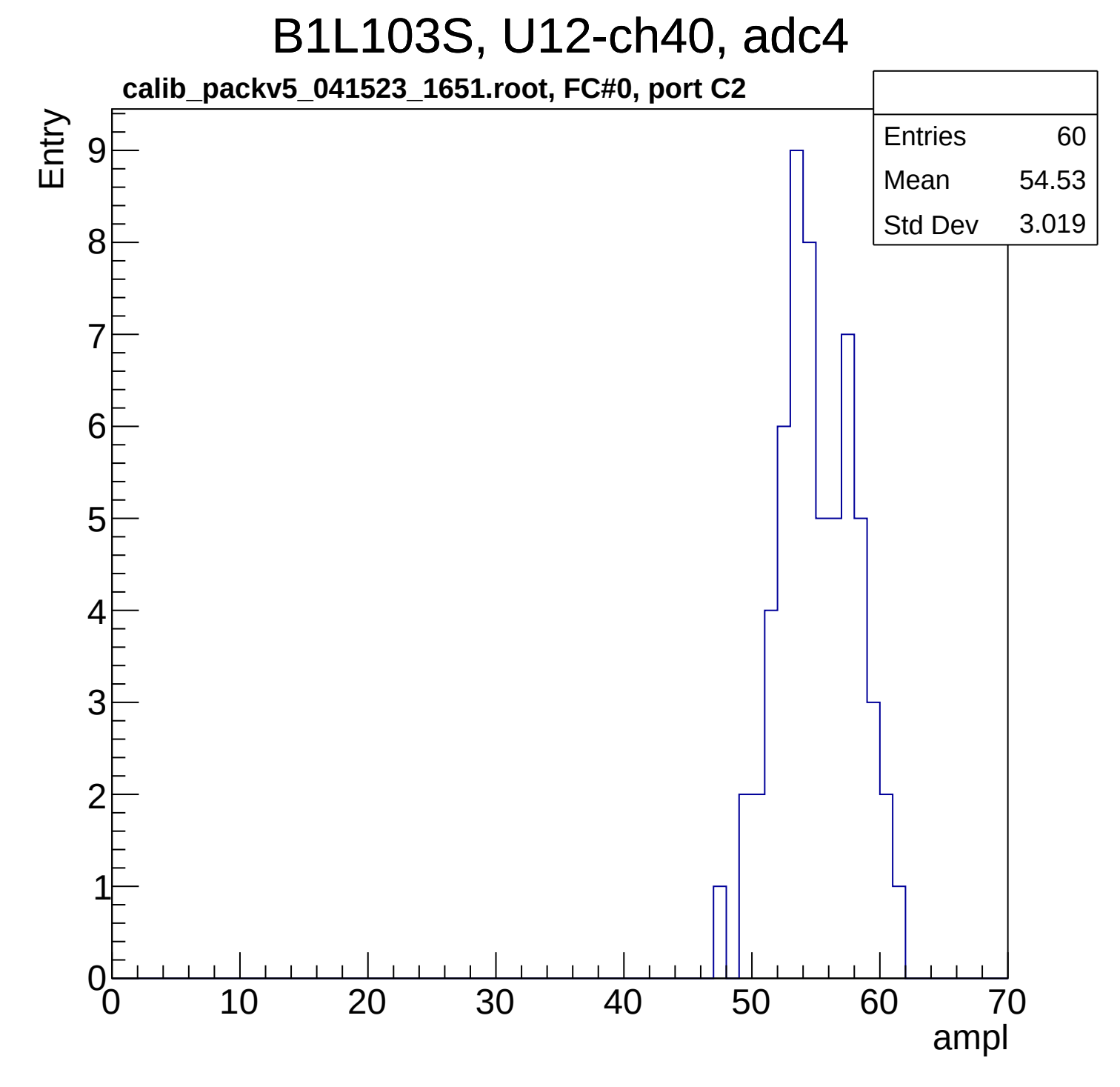
B1L103S, U12-ch40, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 54.53
Std Dev 3.019
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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40
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60
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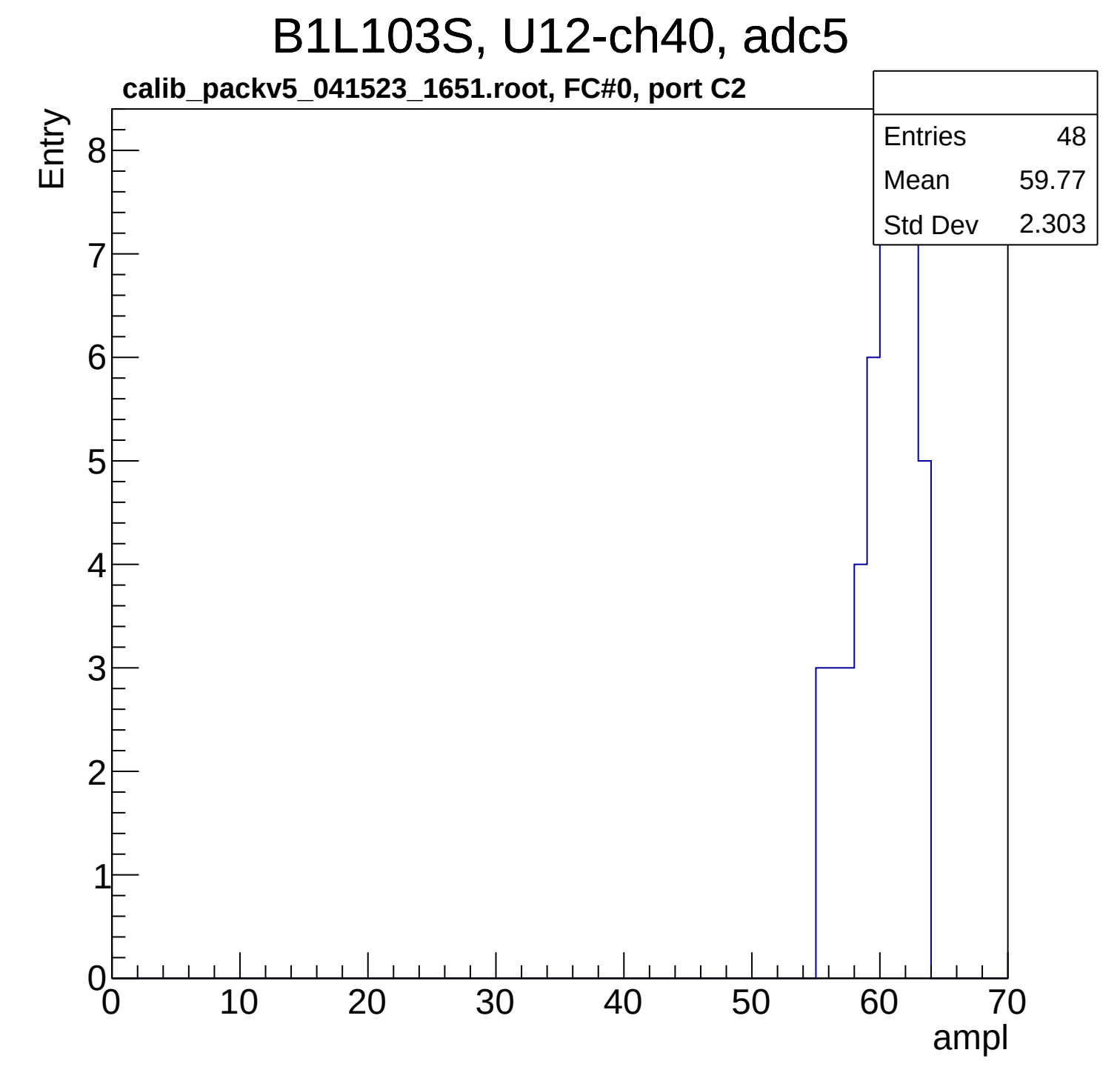
B1L103S, U12-ch40, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 59.77
Std Dev 2.303
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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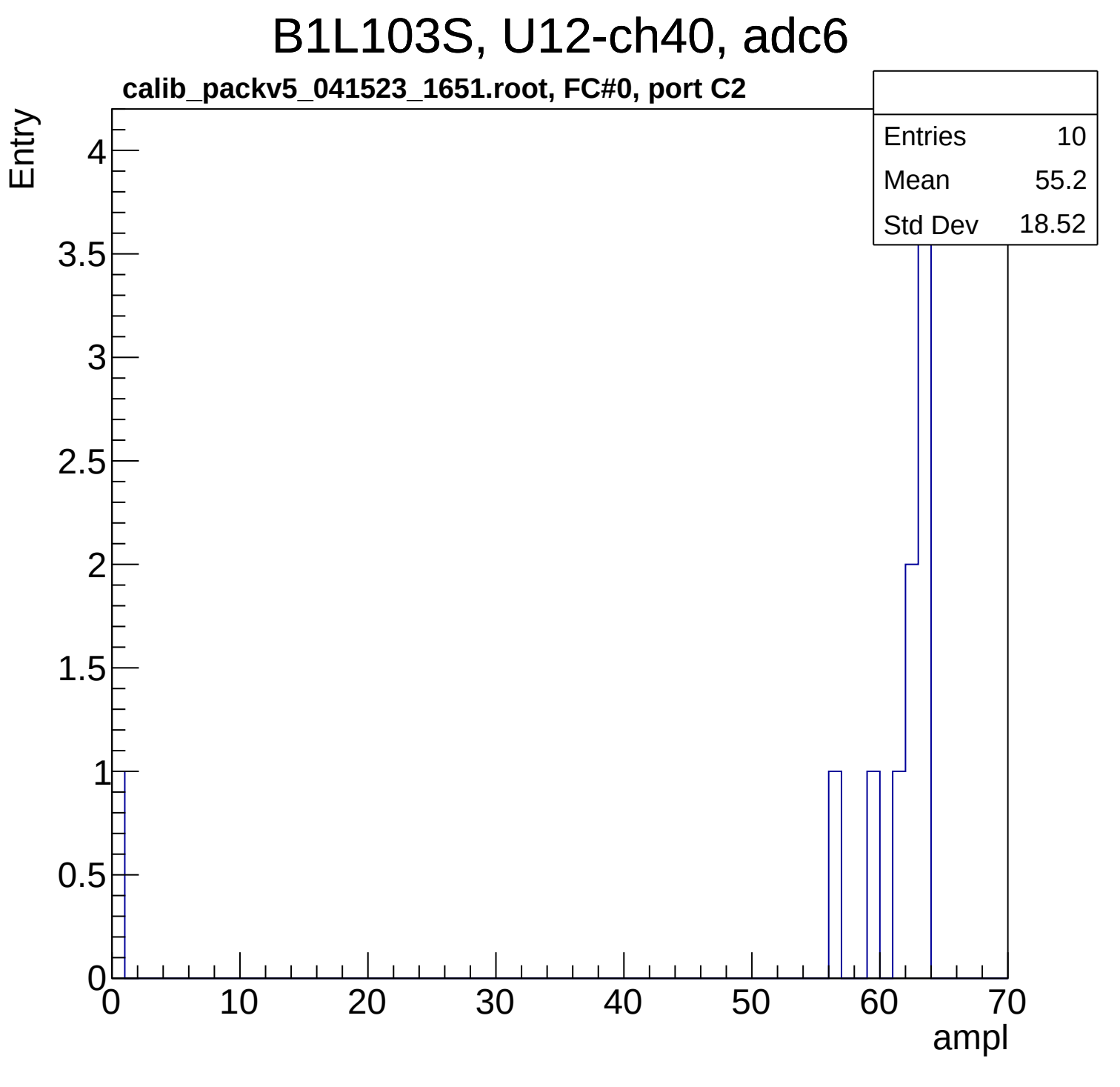
B1L103S, U12-ch40, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.2
Std Dev 18.52
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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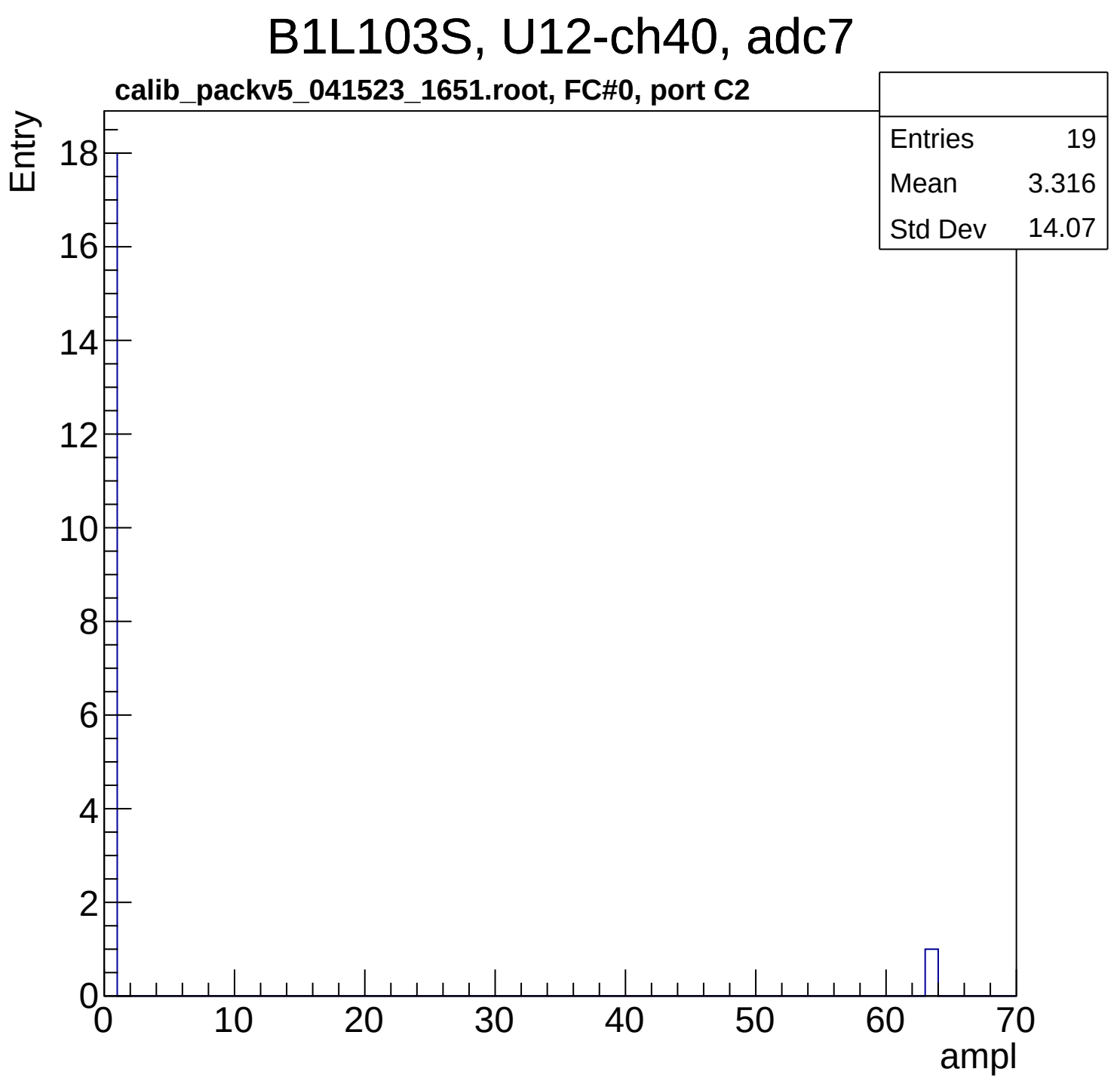
B1L103S, U12-ch40, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
0
2
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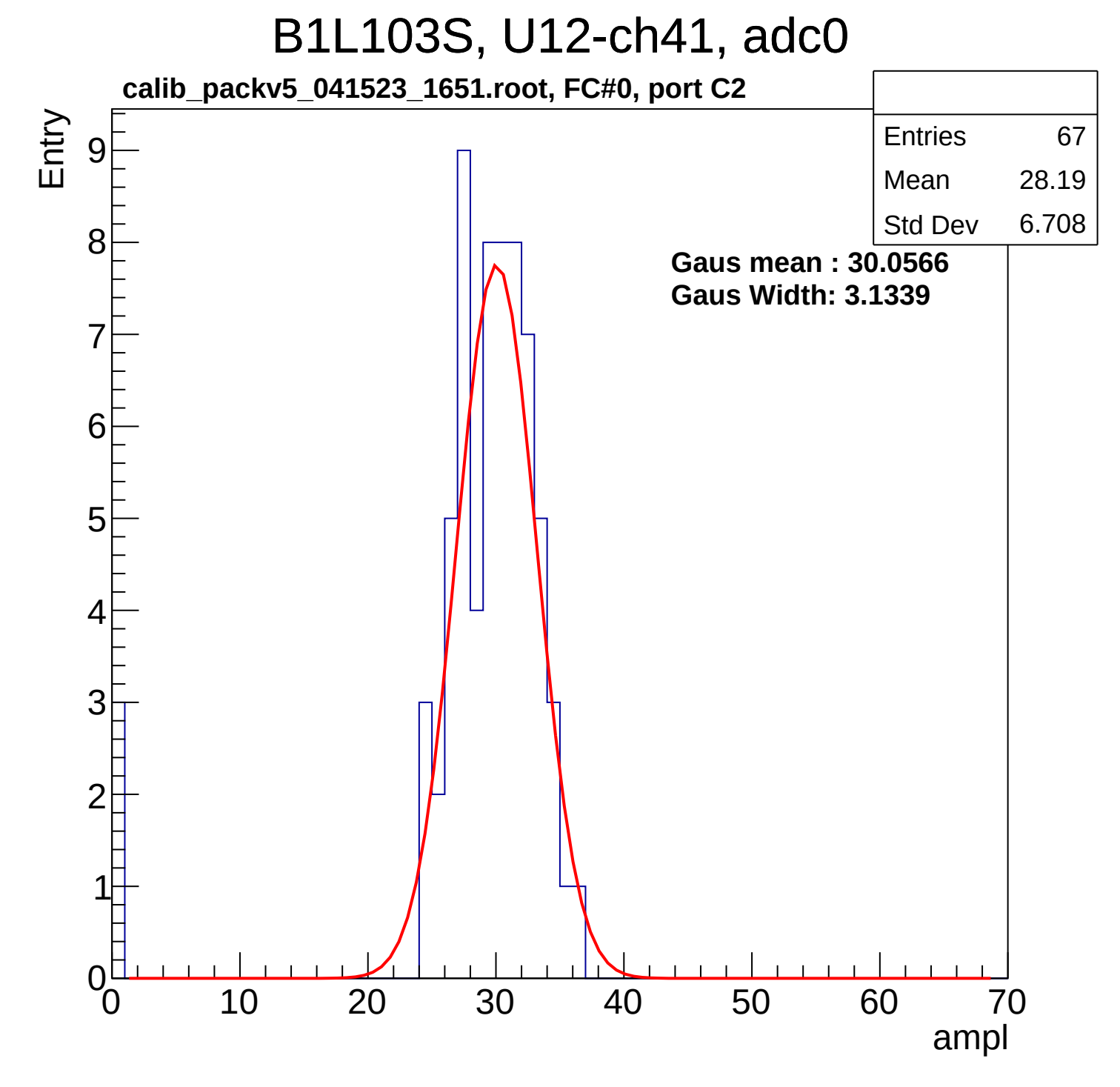
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch41, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 28.19
Std Dev 6.708
Gaus mean : 30.0566
Gaus Width: 3.1339
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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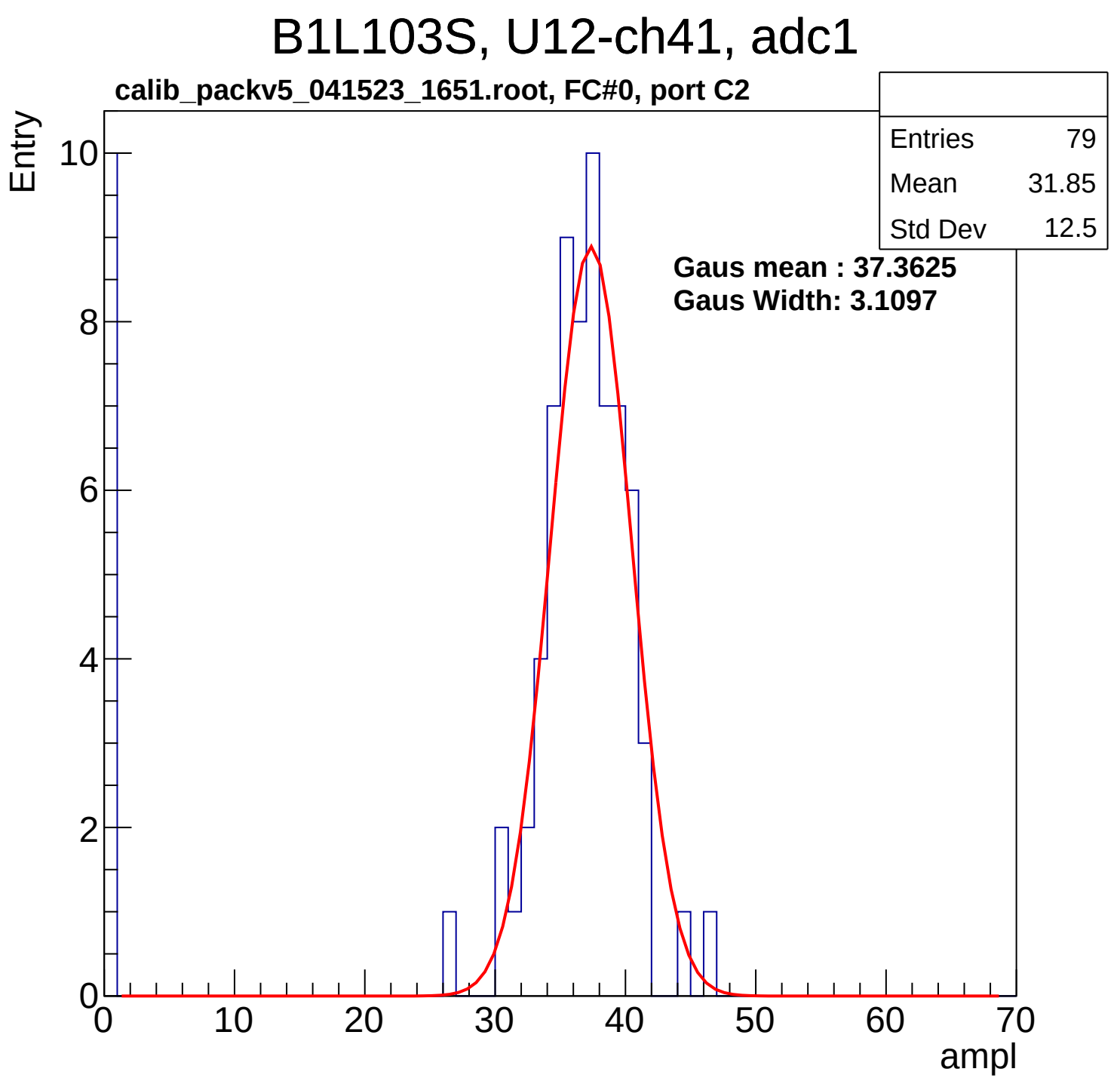
B1L103S, U12-ch41, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 31.85
Std Dev 12.5
Gaus mean : 37.3625
Gaus Width: 3.1097
Entry
ampl
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0
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20
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40
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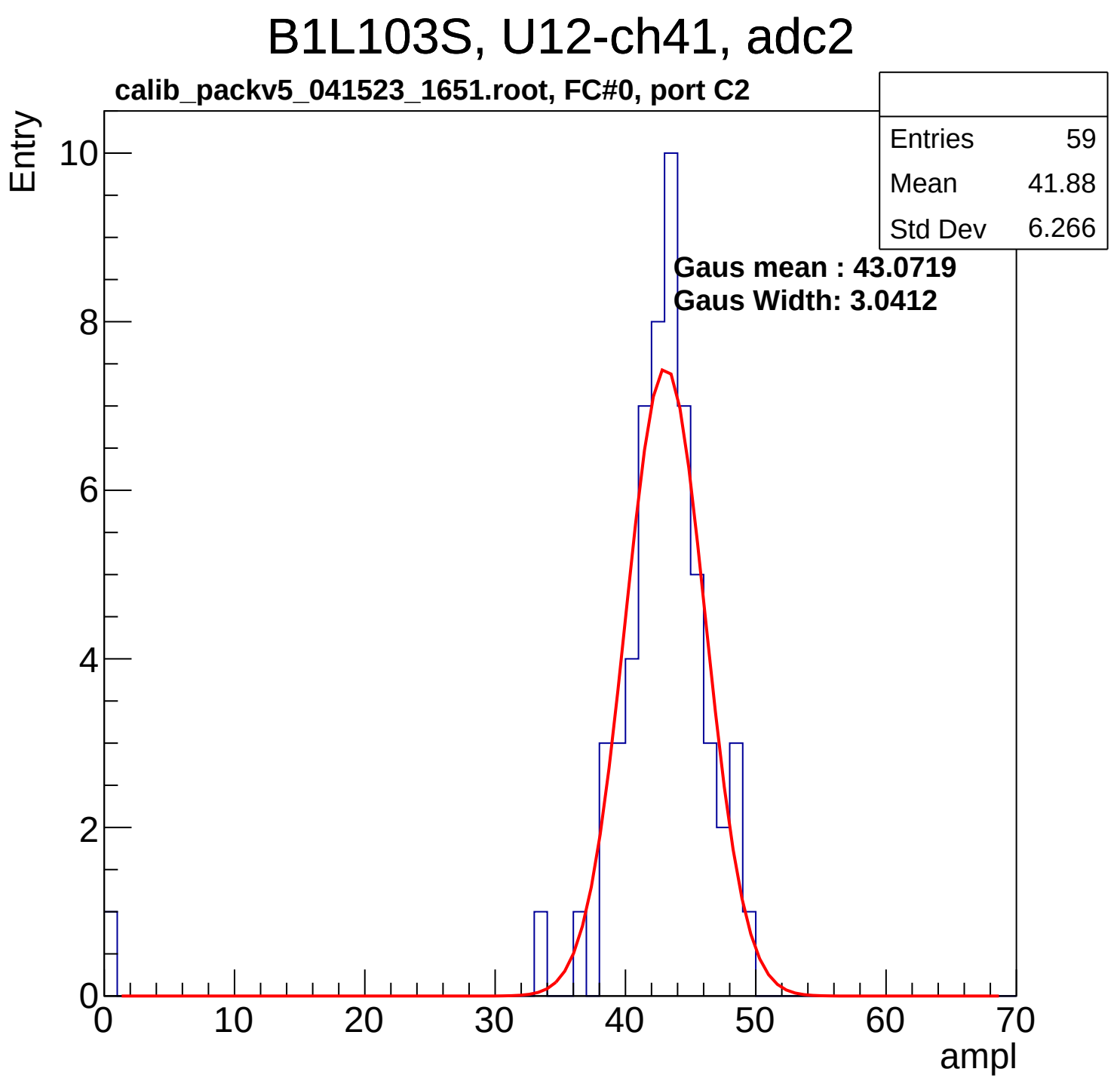
60
70


B1L103S, U12-ch41, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 41.88
Std Dev 6.266
Gaus mean : 43.0719
Gaus Width: 3.0412
Entry
ampl
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2
4
6
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10
0
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20
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40
50
60
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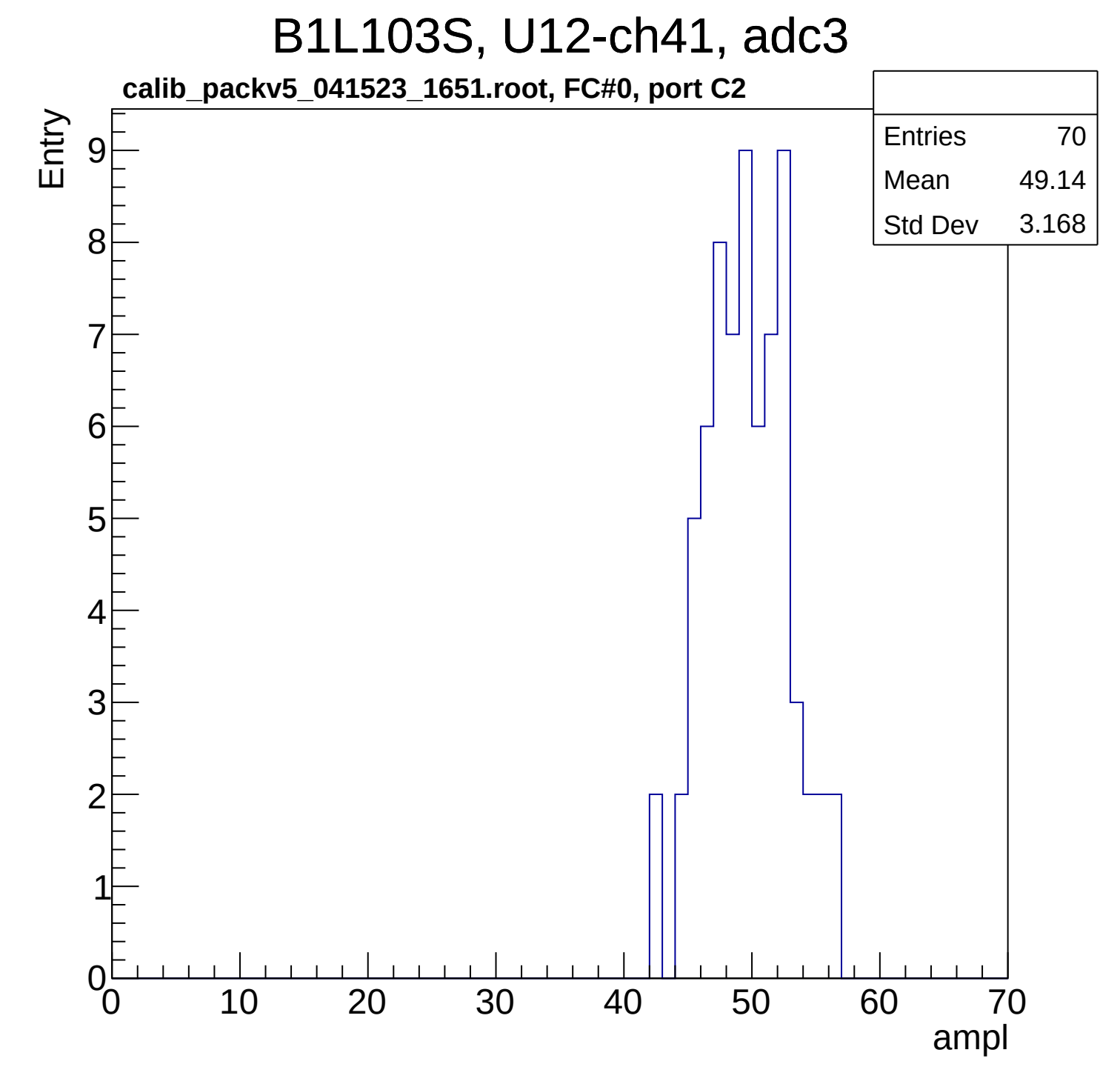
B1L103S, U12-ch41, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 49.14
Std Dev 3.168
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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60
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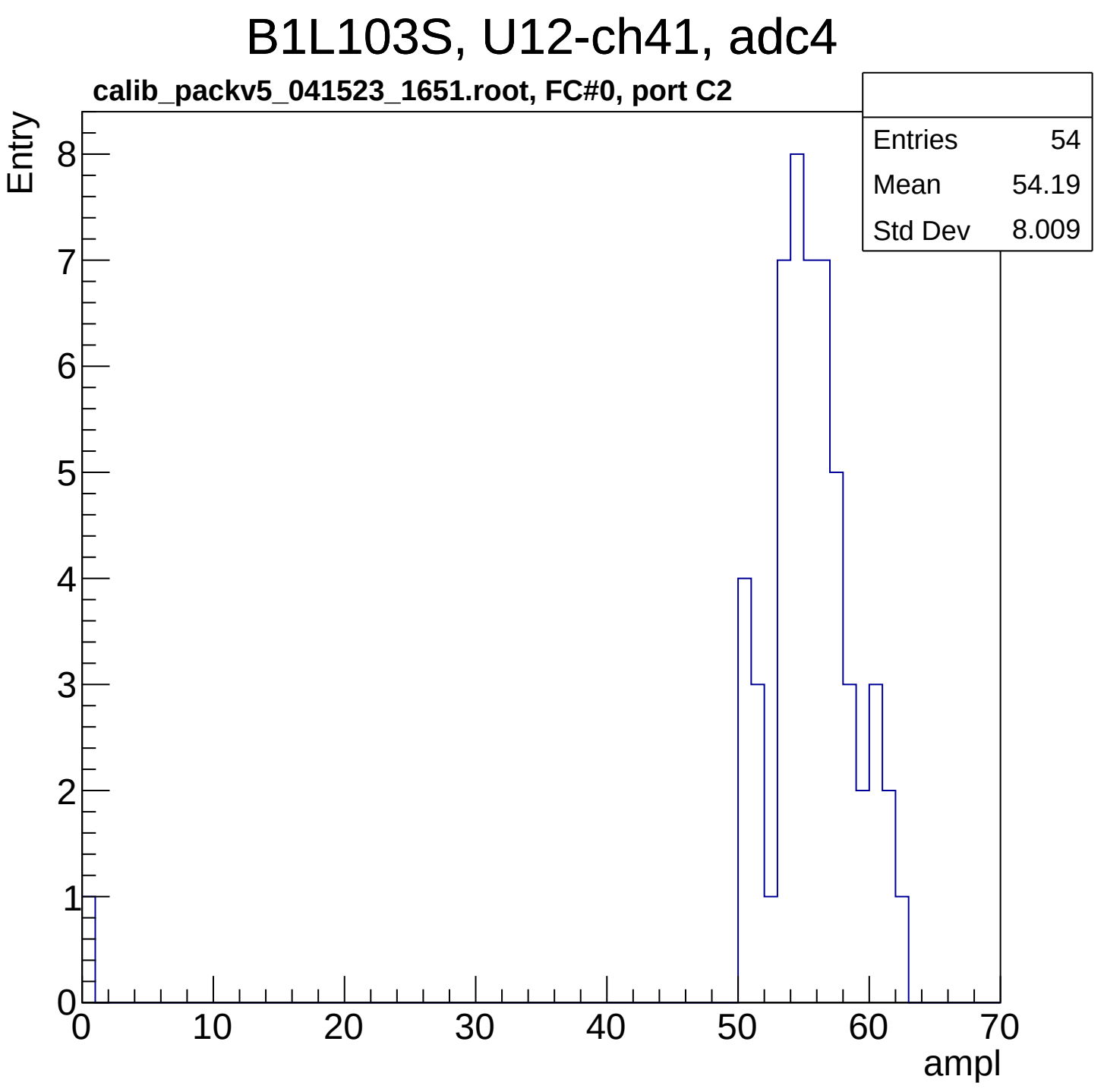
B1L103S, U12-ch41, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 54.19
Std Dev 8.009
Entry
ampl
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1
2
3
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5
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7
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0
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20
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40
50
60
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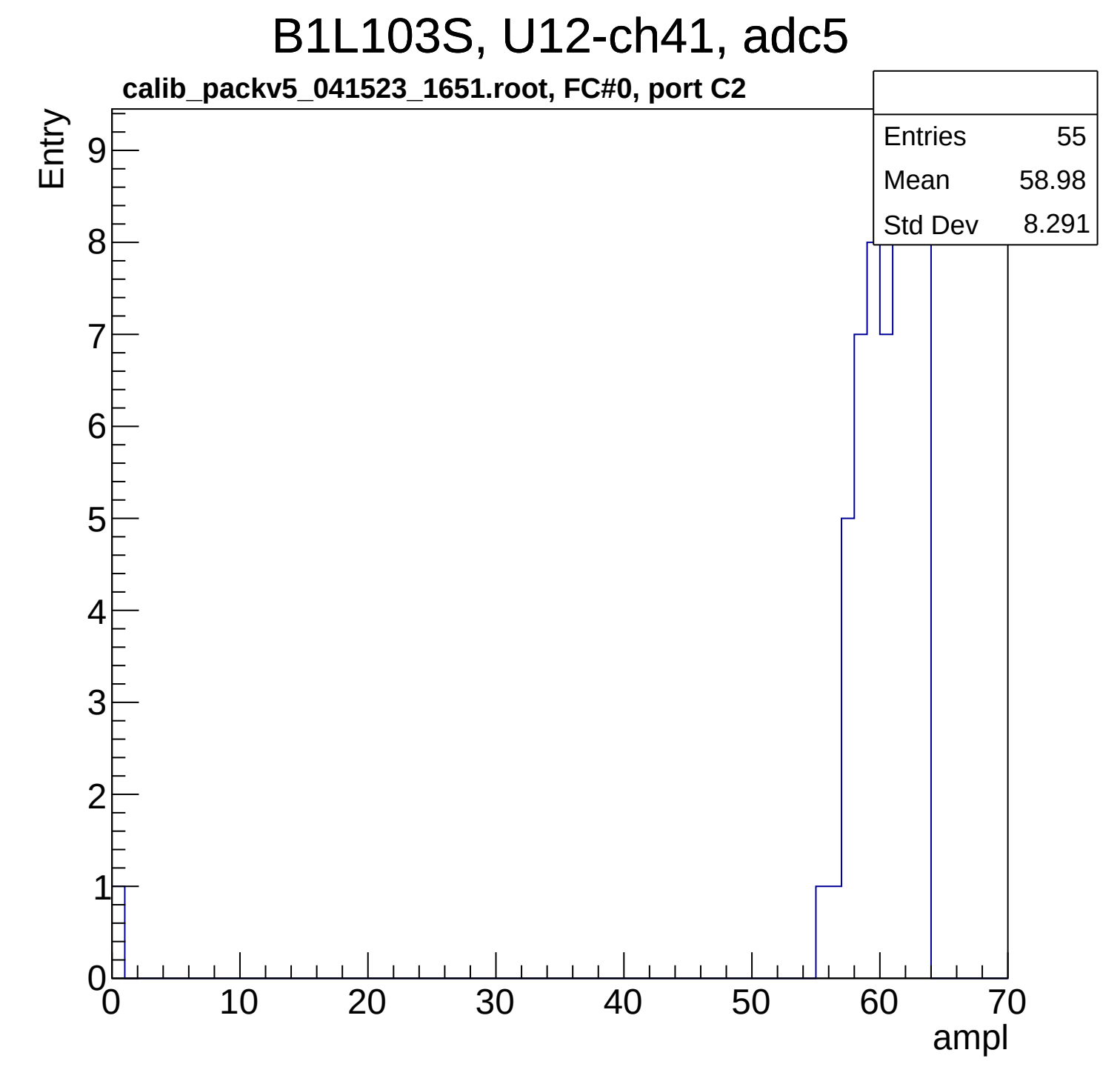
B1L103S, U12-ch41, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.98
Std Dev 8.291
Entry
ampl
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2
3
4
5
6
7
8
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0
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40
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60
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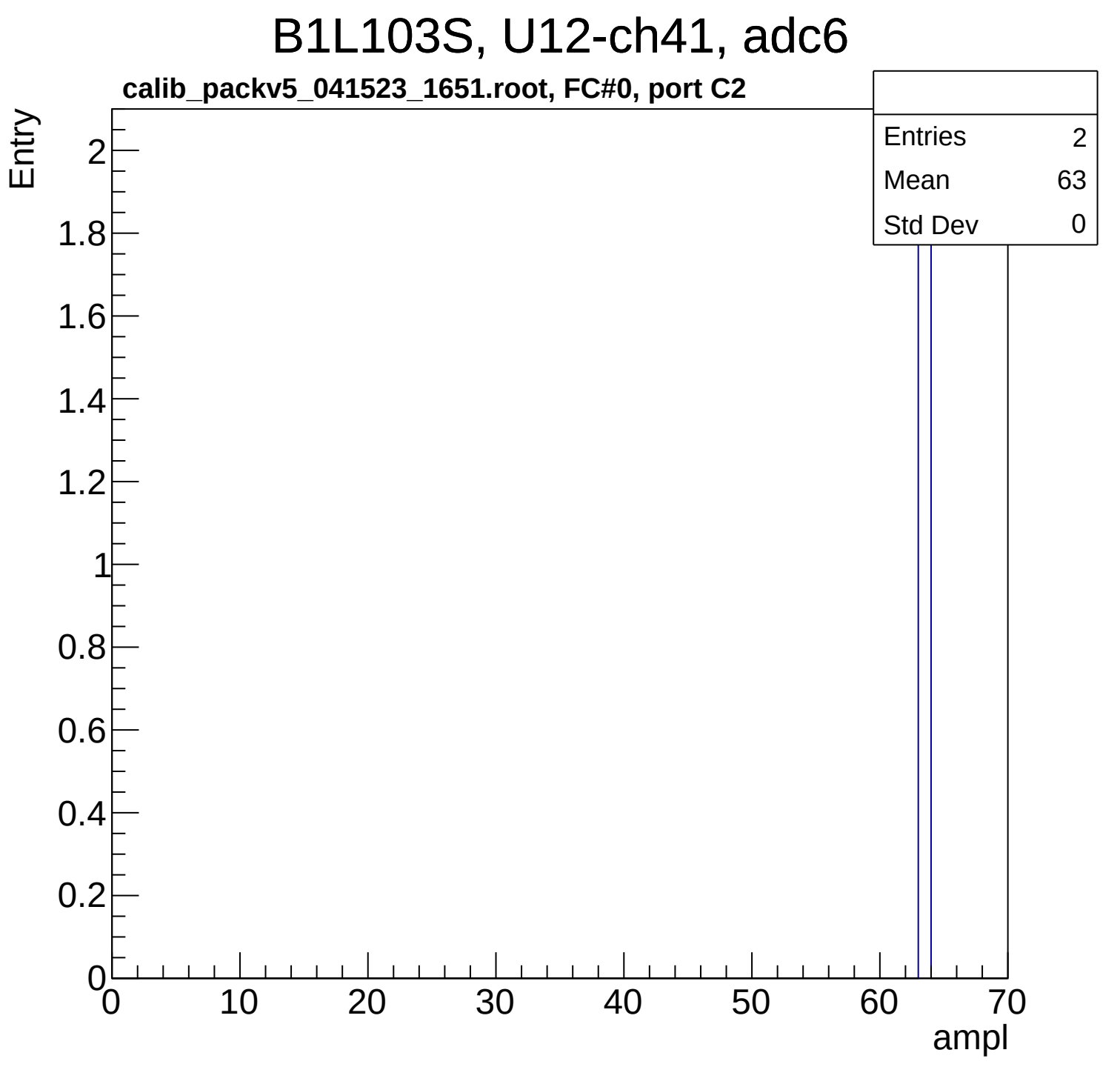
B1L103S, U12-ch41, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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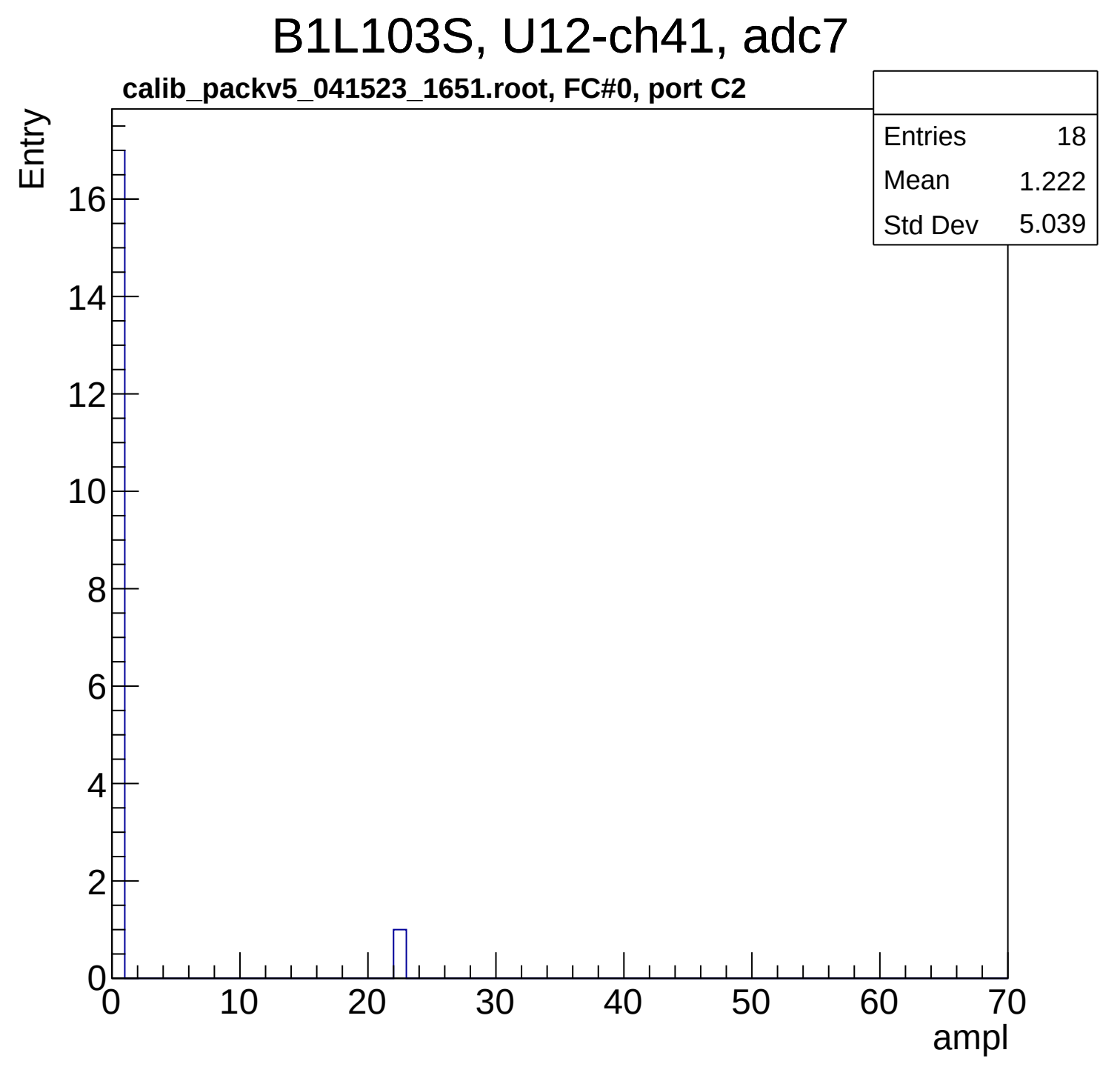
B1L103S, U12-ch41, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.222
Std Dev 5.039
Entry
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4
6
8
10
12
14
16
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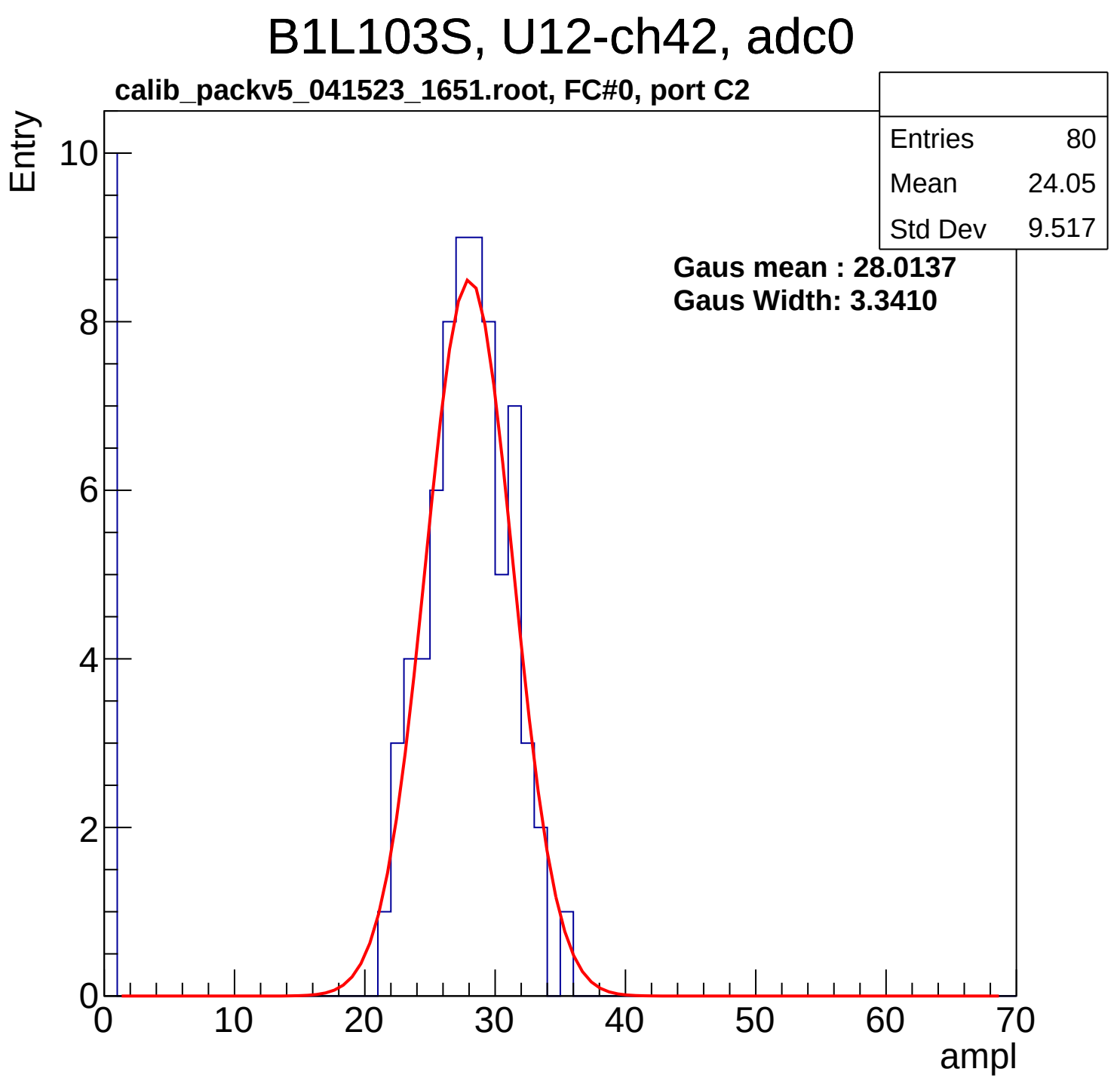
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch42, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 24.05
Std Dev 9.517
Gaus mean : 28.0137
Gaus Width: 3.3410
Entry
ampl
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2
4
6
8
10
0
10
20
30
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50
60
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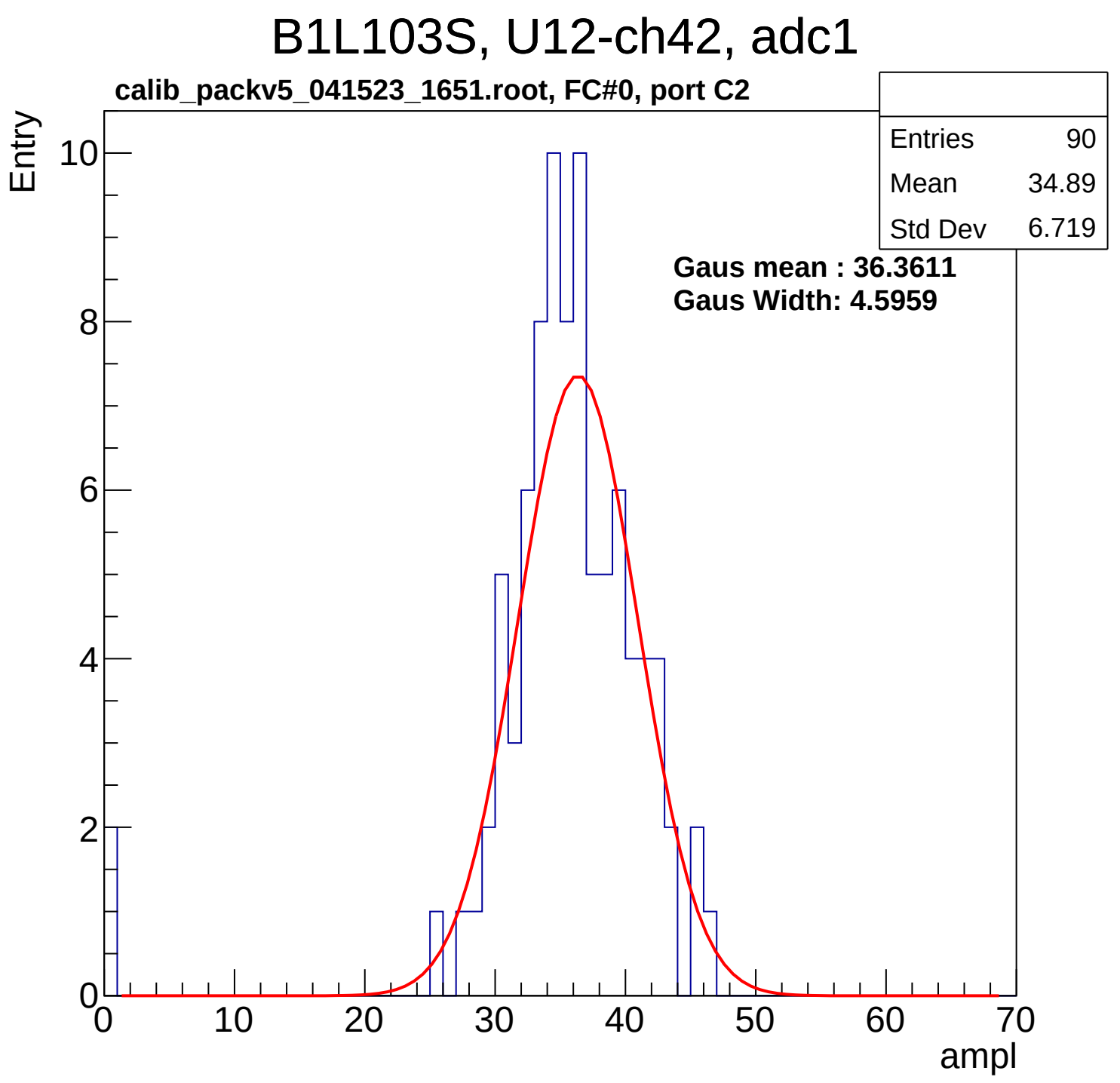
B1L103S, U12-ch42, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 34.89
Std Dev 6.719
Gaus mean : 36.3611
Gaus Width: 4.5959
Entry
ampl
0
2
4
6
8
10
0
10
20
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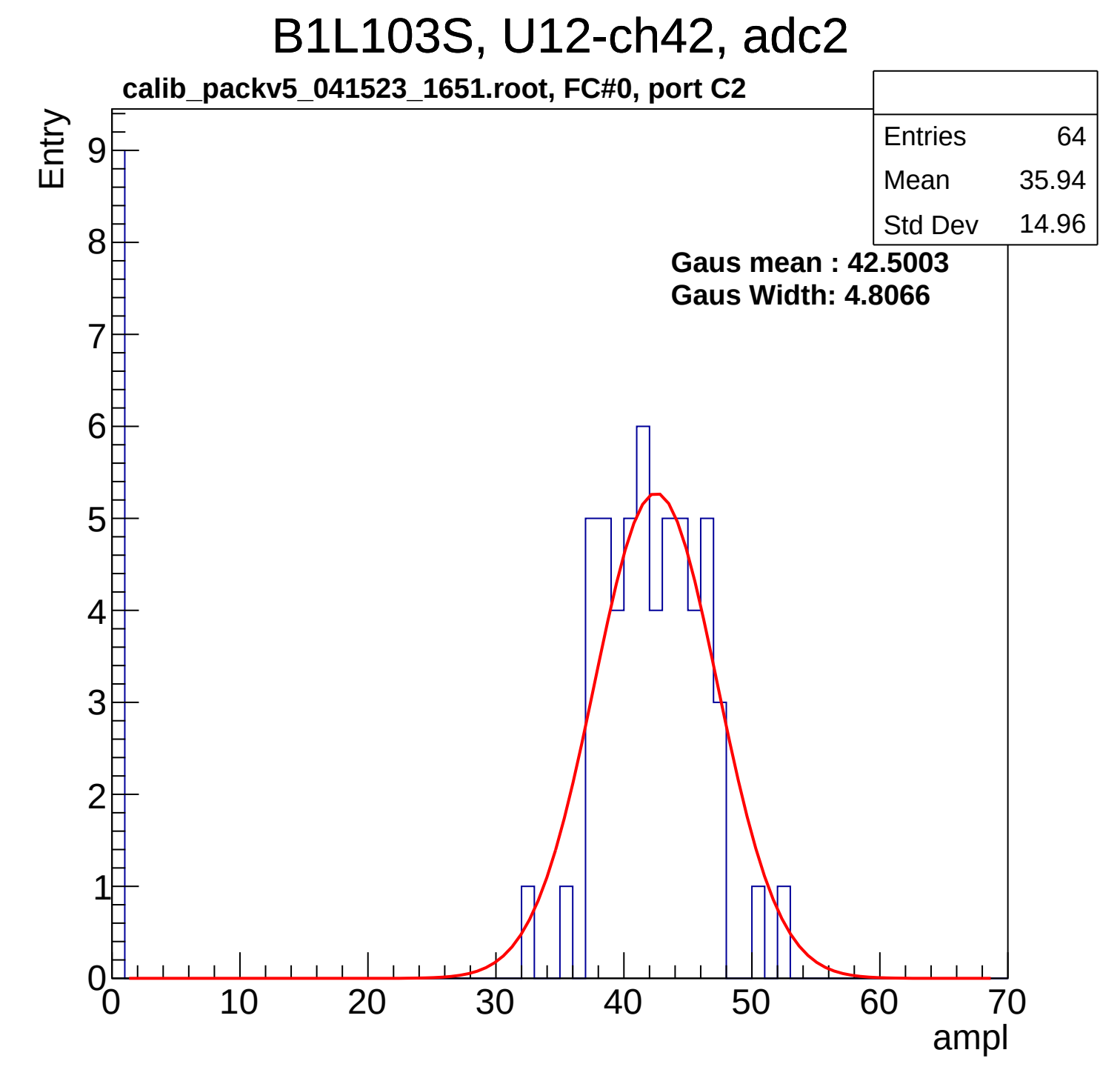
B1L103S, U12-ch42, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 35.94
Std Dev 14.96
Gaus mean : 42.5003
Gaus Width: 4.8066
Entry
ampl
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2
3
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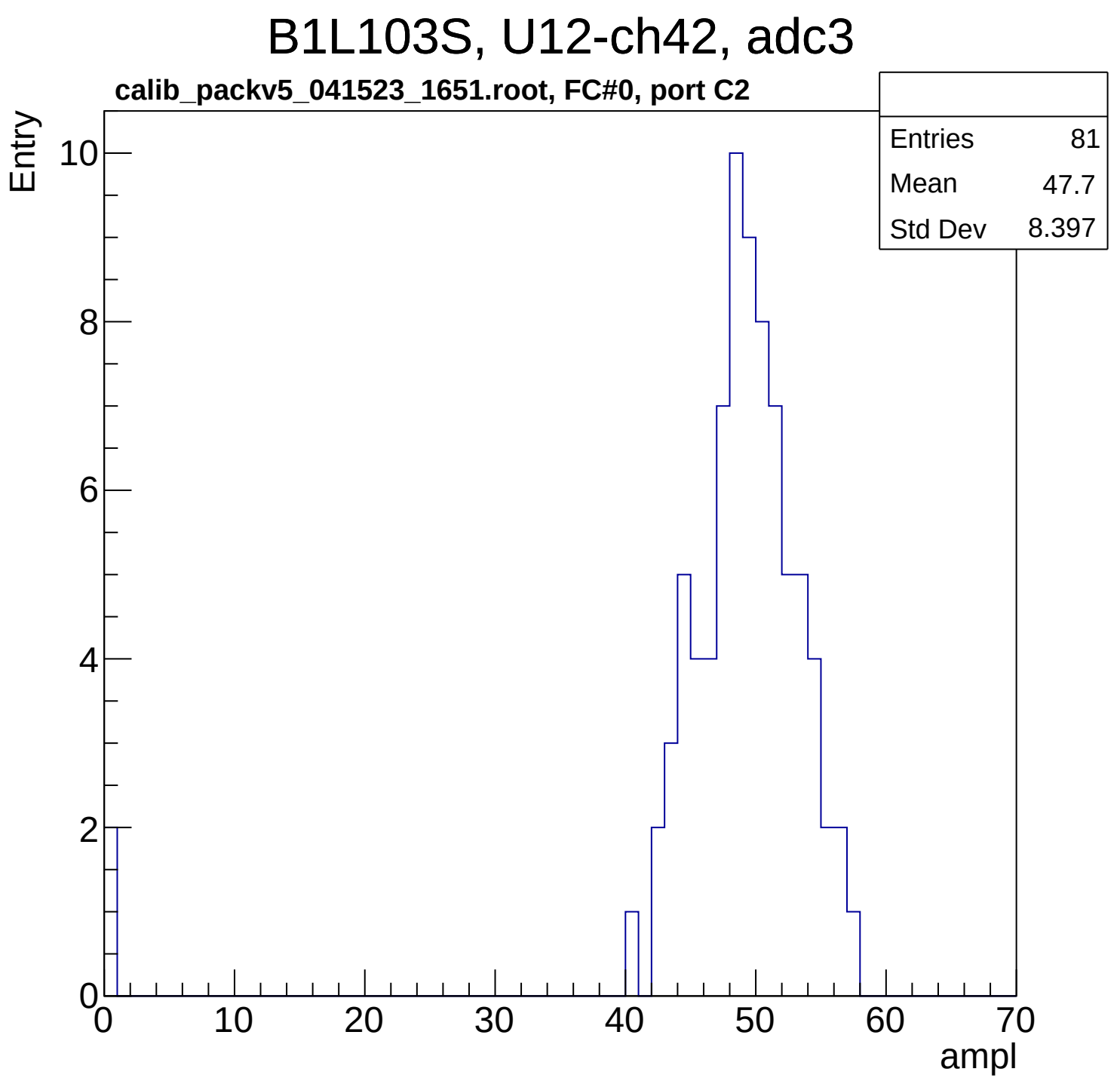
B1L103S, U12-ch42, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 47.7
Std Dev 8.397
Entry
ampl
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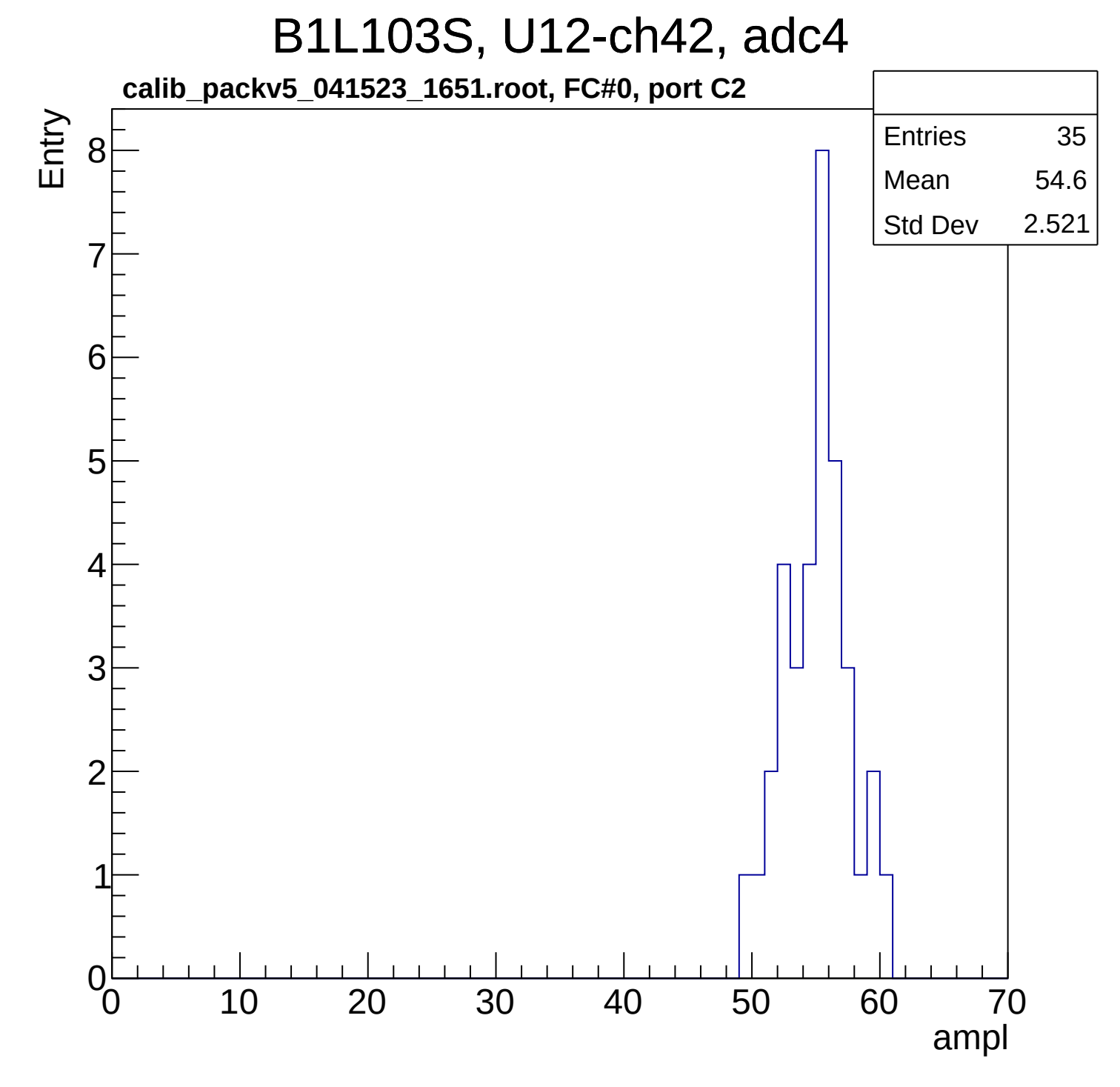
B1L103S, U12-ch42, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 54.6
Std Dev 2.521
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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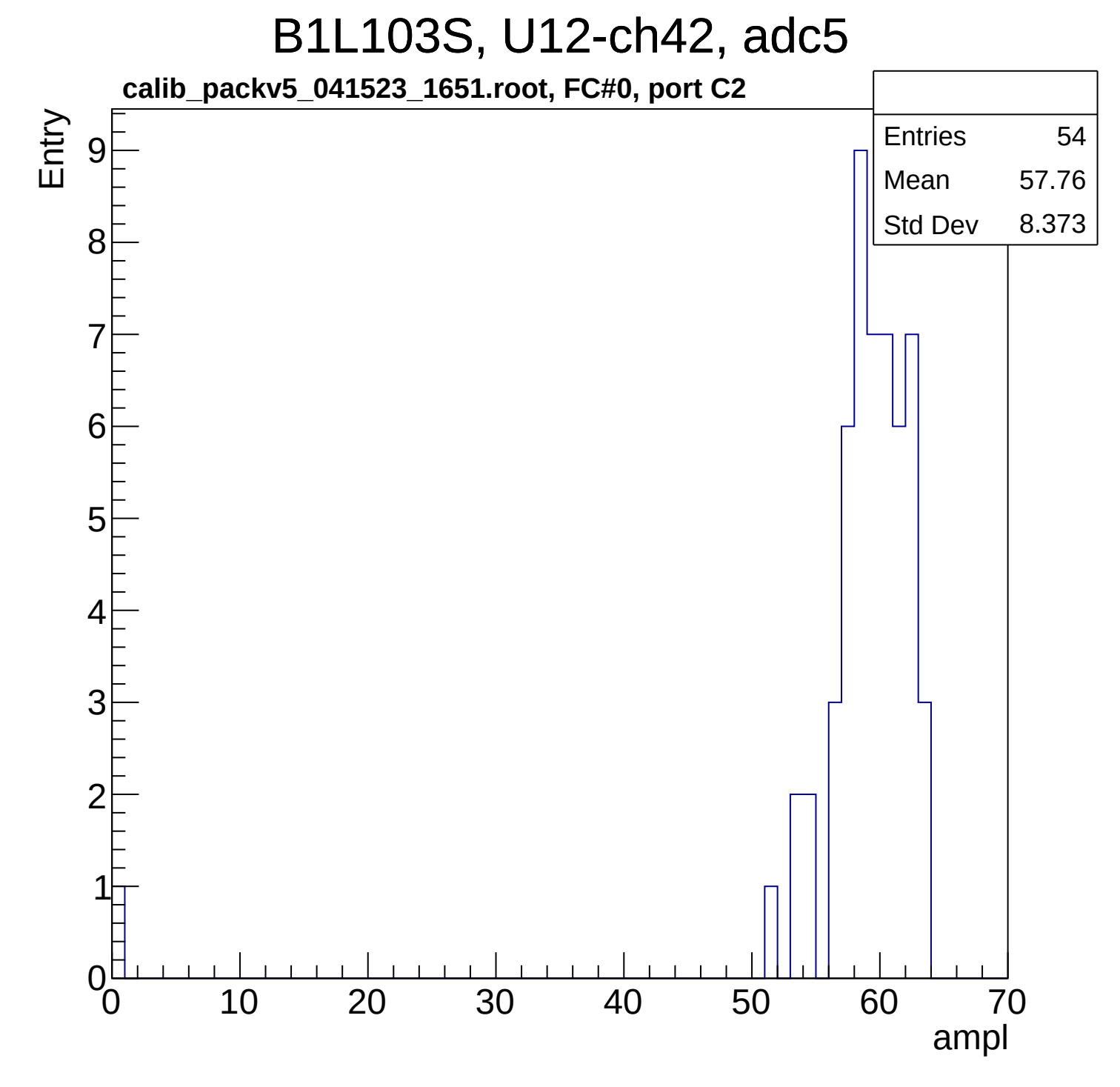
40
50
60
70


B1L103S, U12-ch42, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.76
Std Dev 8.373
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
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60
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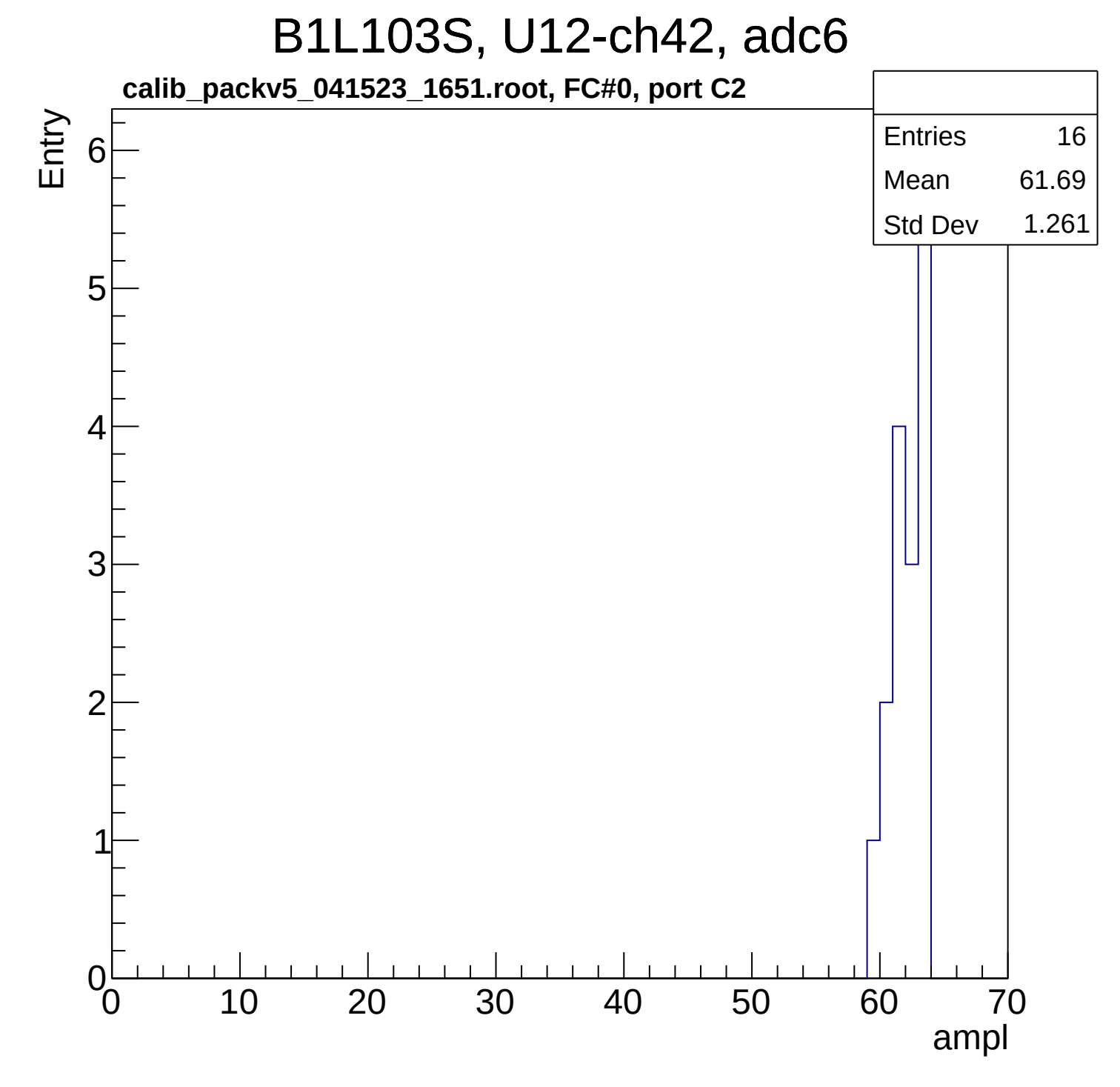
B1L103S, U12-ch42, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 61.69
Std Dev 1.261
Entry
ampl
0
1
2
3
4
5
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0
10
20
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40
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60
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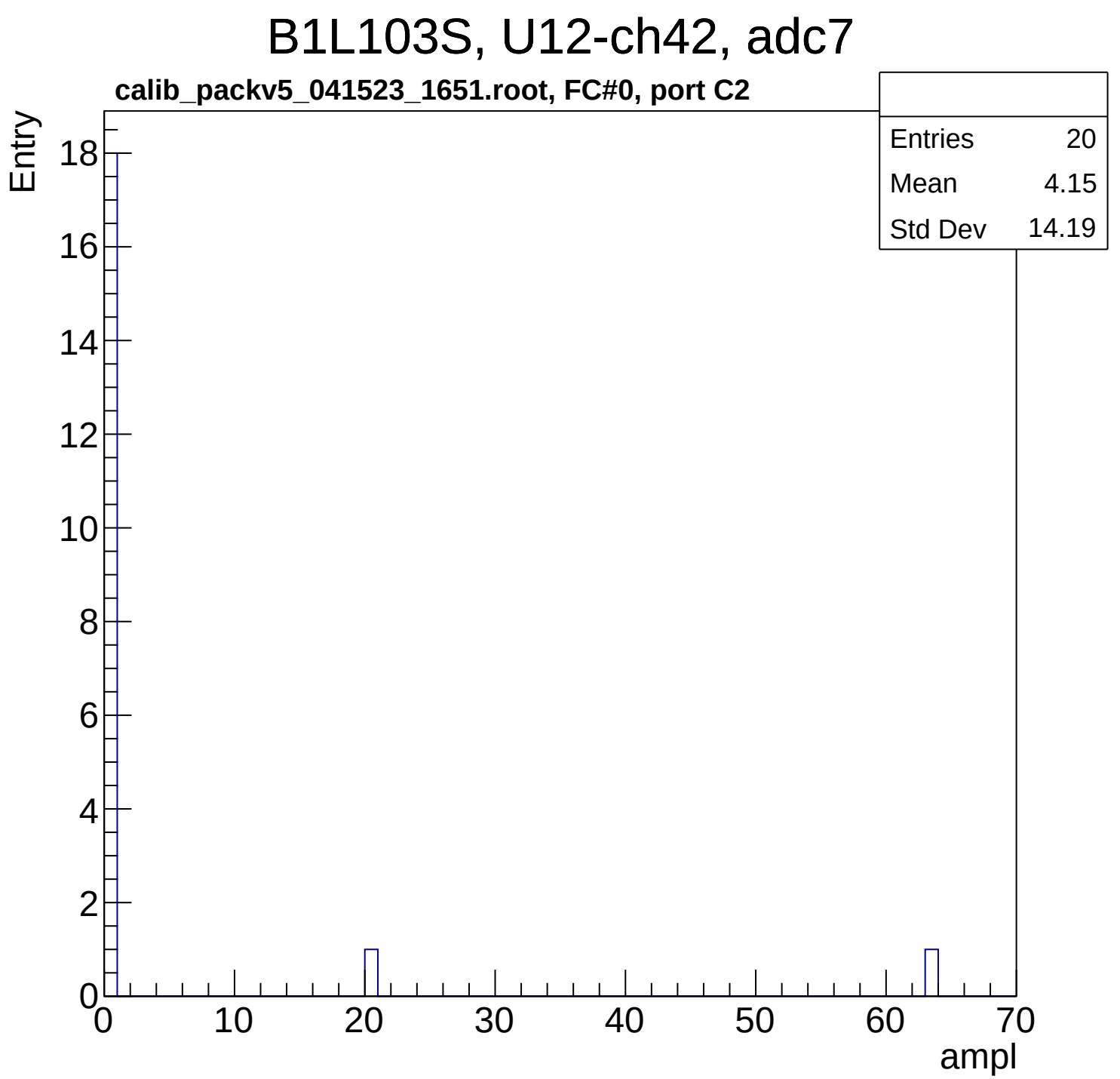
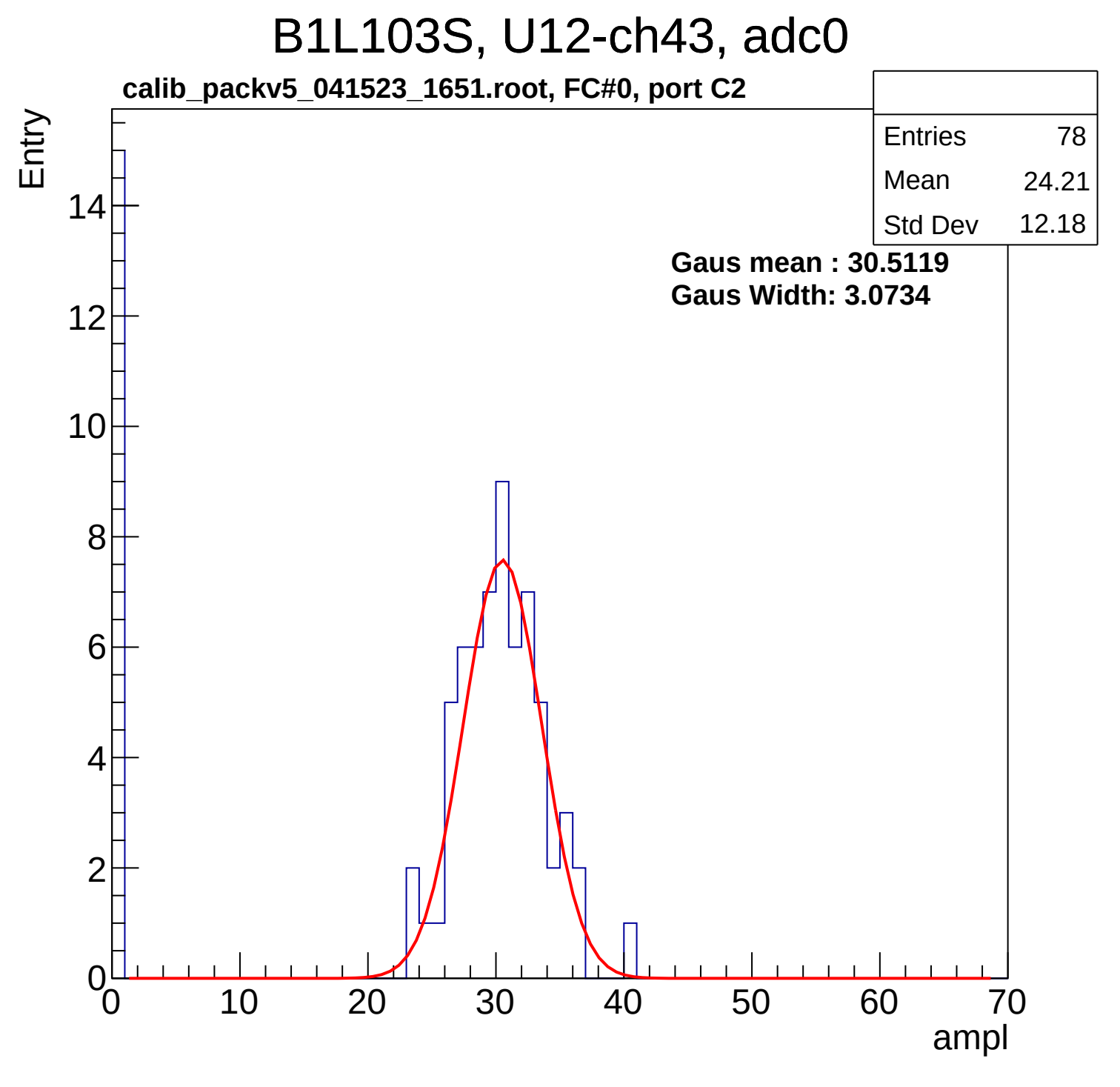

B1L103S, U12-ch42, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.15
Std Dev 14.19
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch43, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 24.21
Std Dev 12.18
Gaus mean : 30.5119
Gaus Width: 3.0734
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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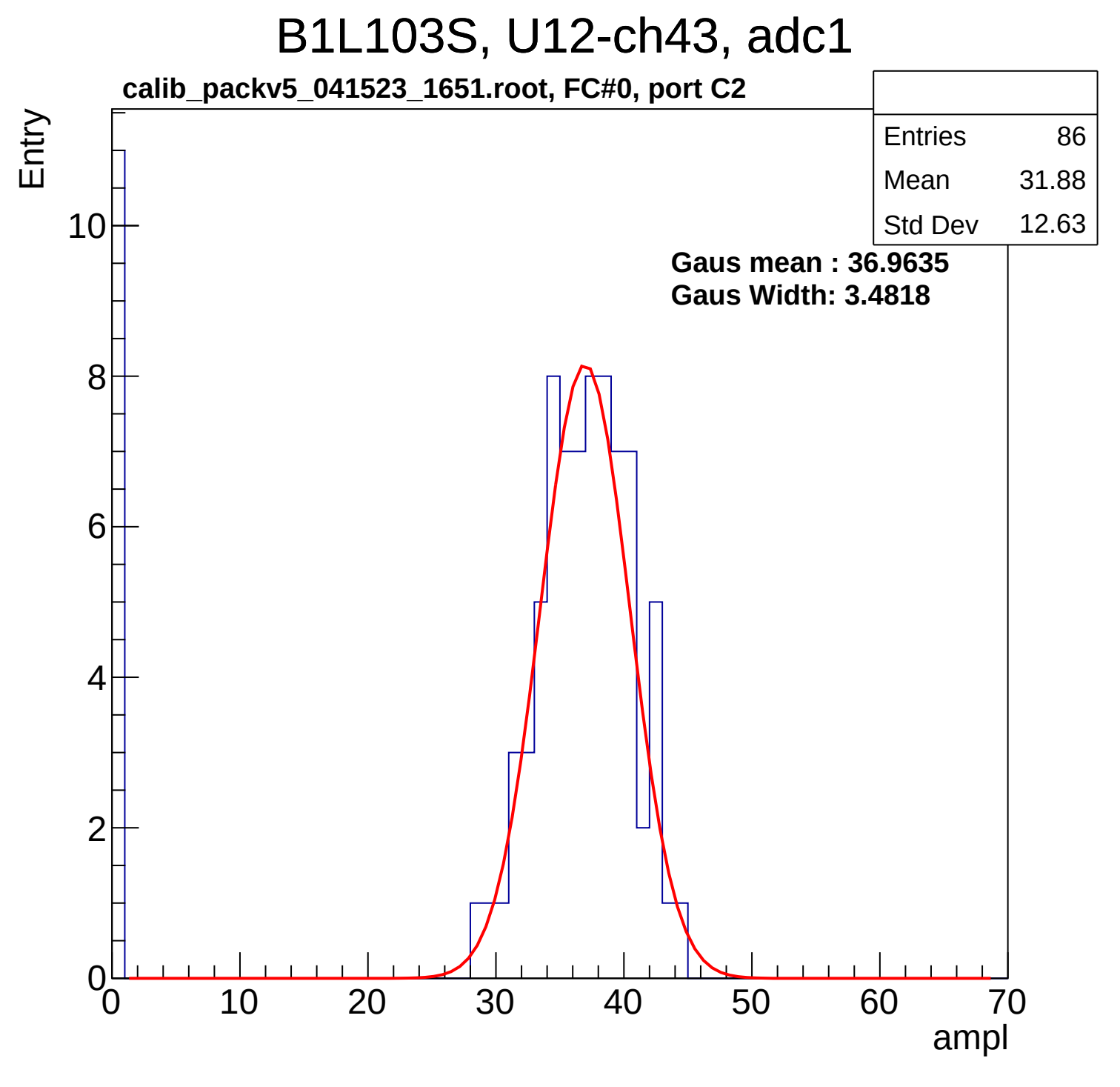
B1L103S, U12-ch43, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 31.88
Std Dev 12.63
Gaus mean : 36.9635
Gaus Width: 3.4818
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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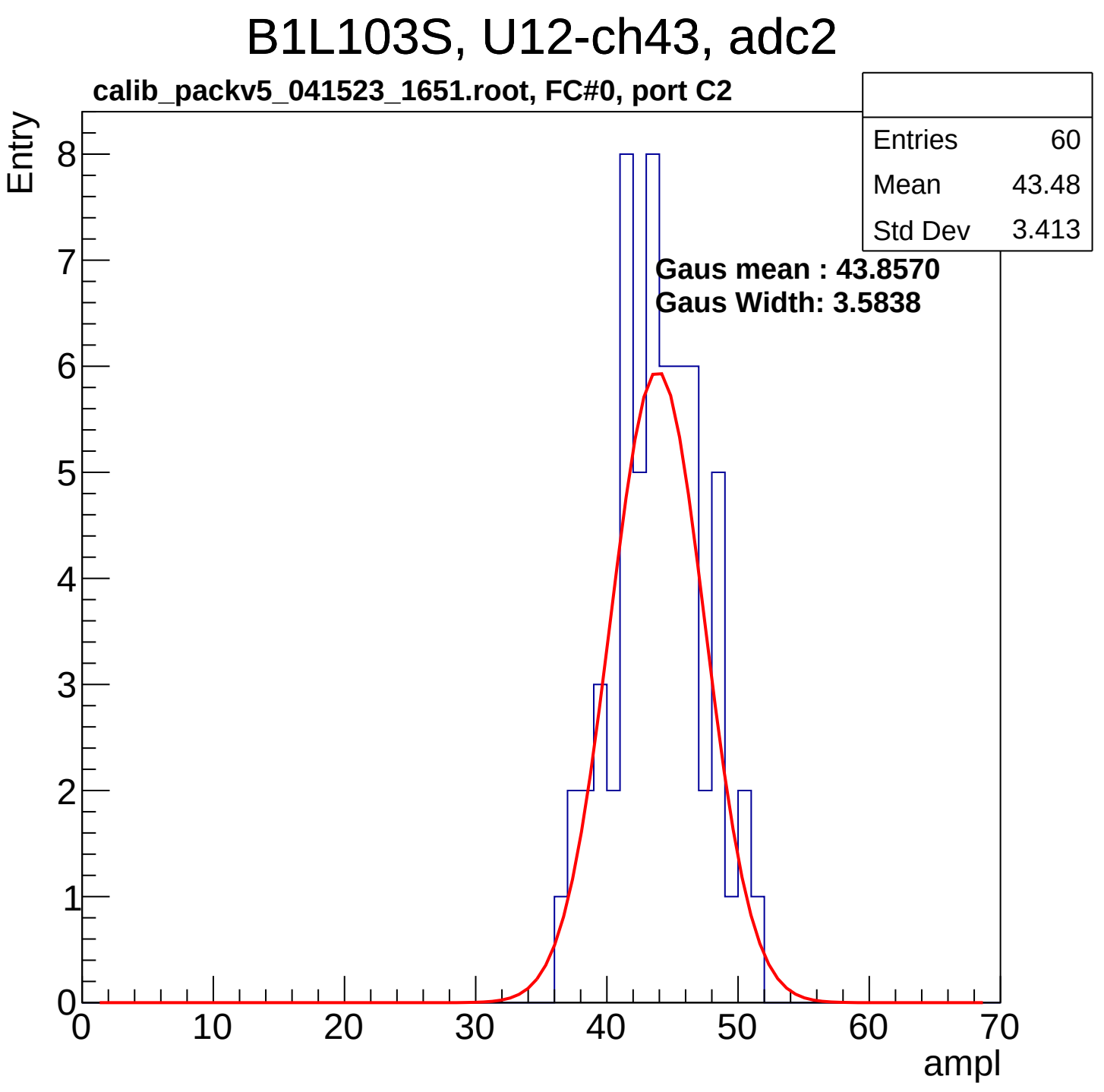
B1L103S, U12-ch43, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 43.48
Std Dev 3.413
Gaus mean : 43.8570
Gaus Width: 3.5838
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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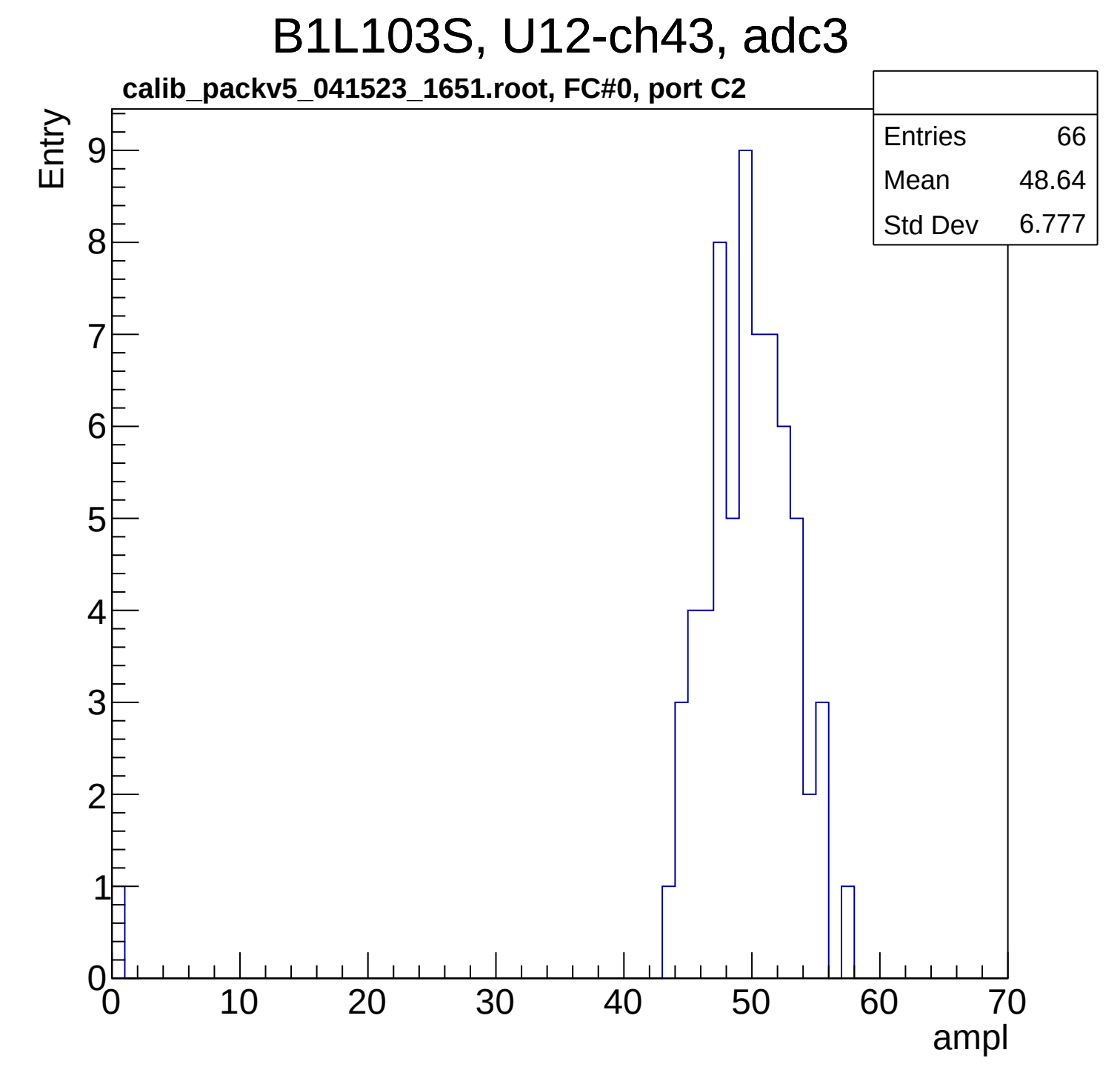
B1L103S, U12-ch43, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 48.64
Std Dev 6.777
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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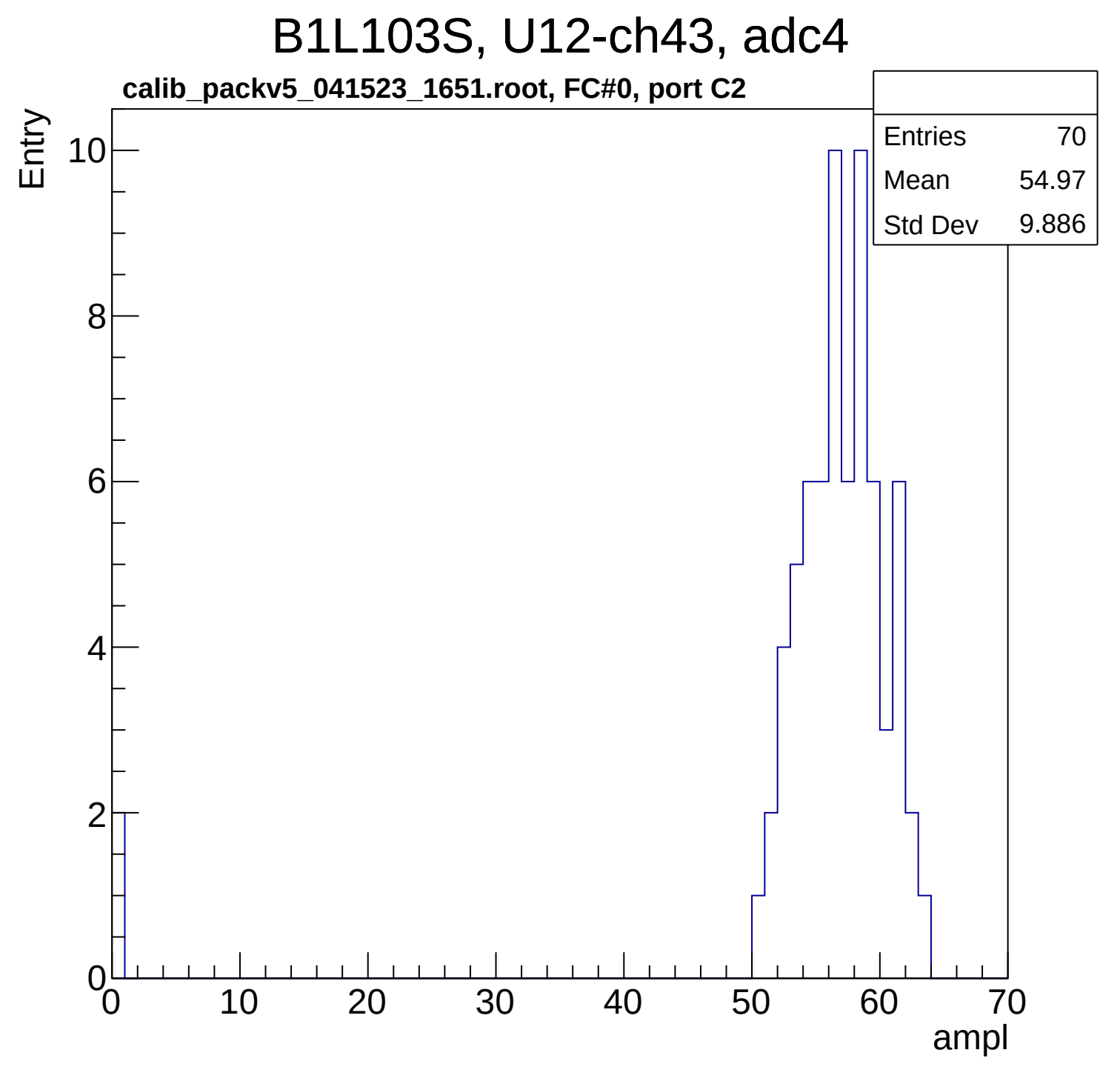
B1L103S, U12-ch43, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 54.97
Std Dev 9.886
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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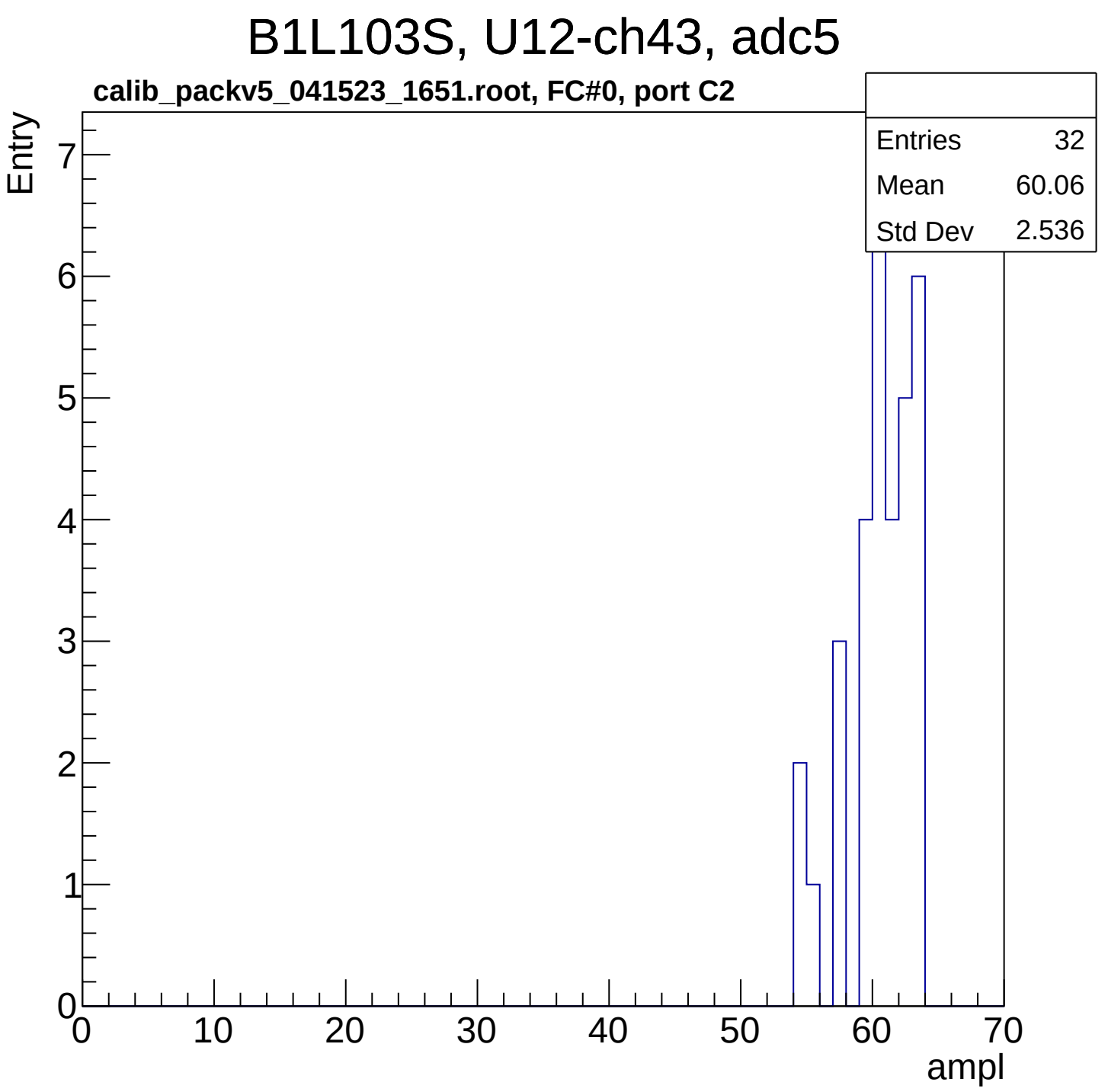
B1L103S, U12-ch43, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 60.06
Std Dev 2.536
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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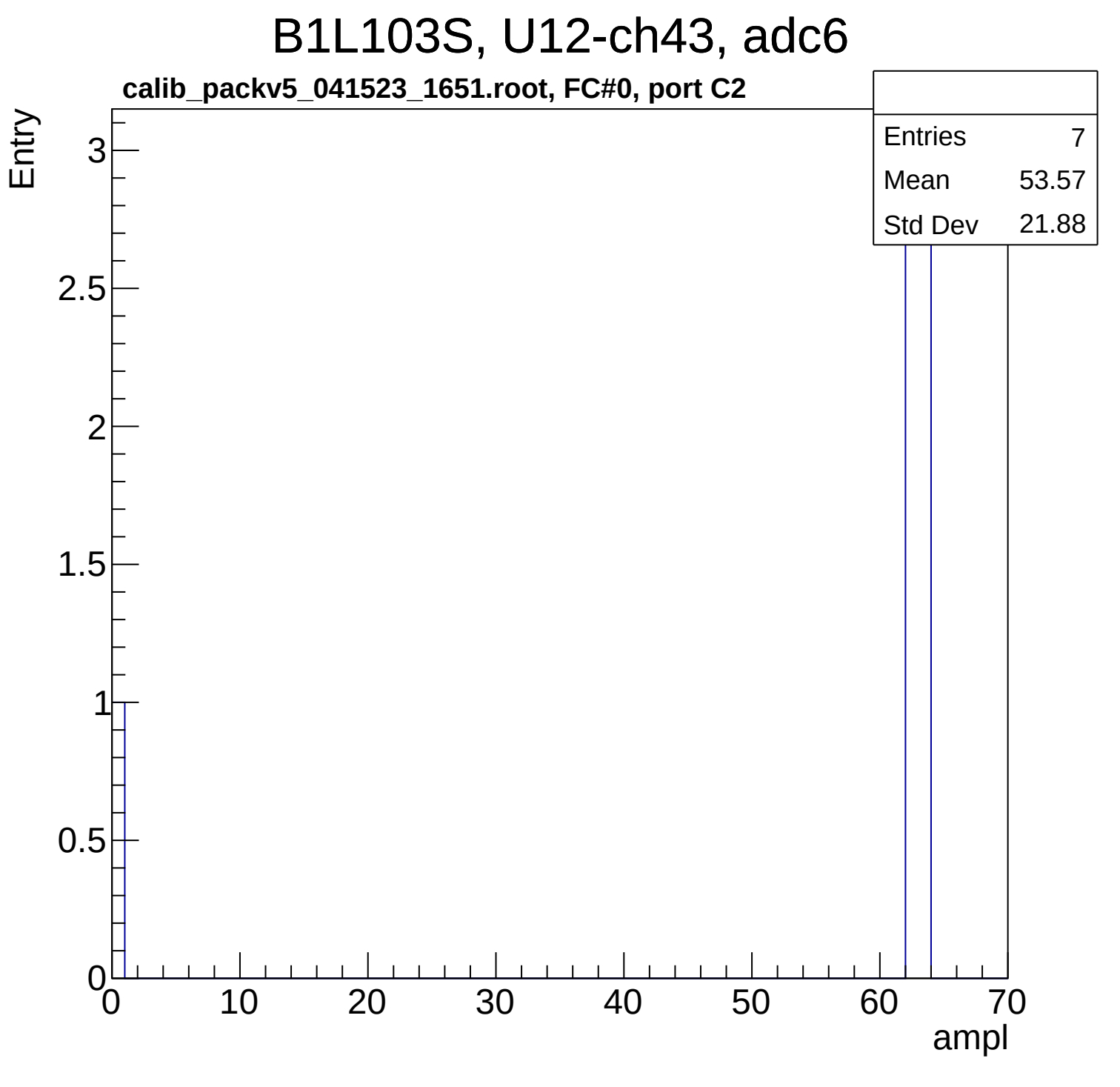
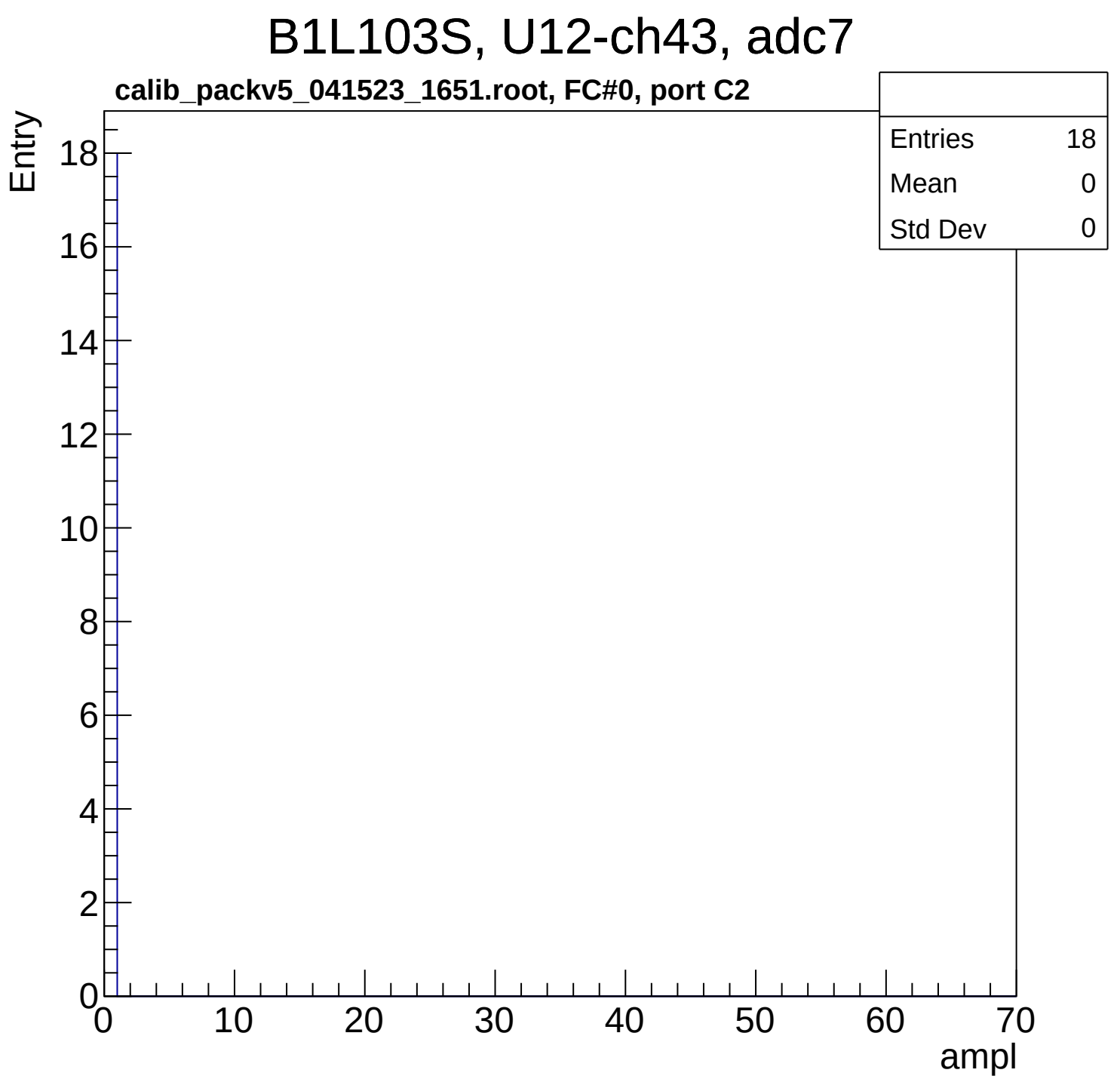
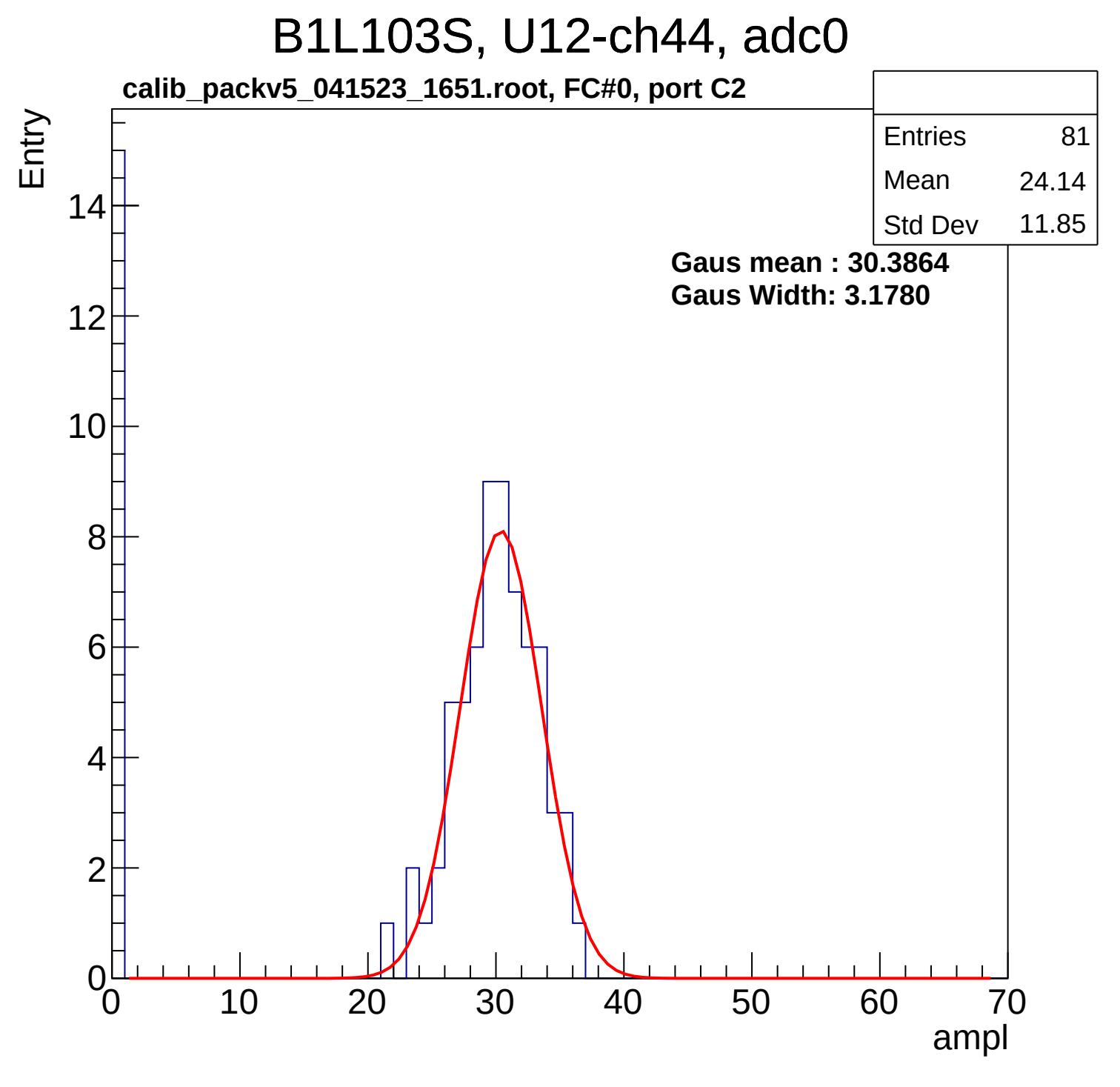
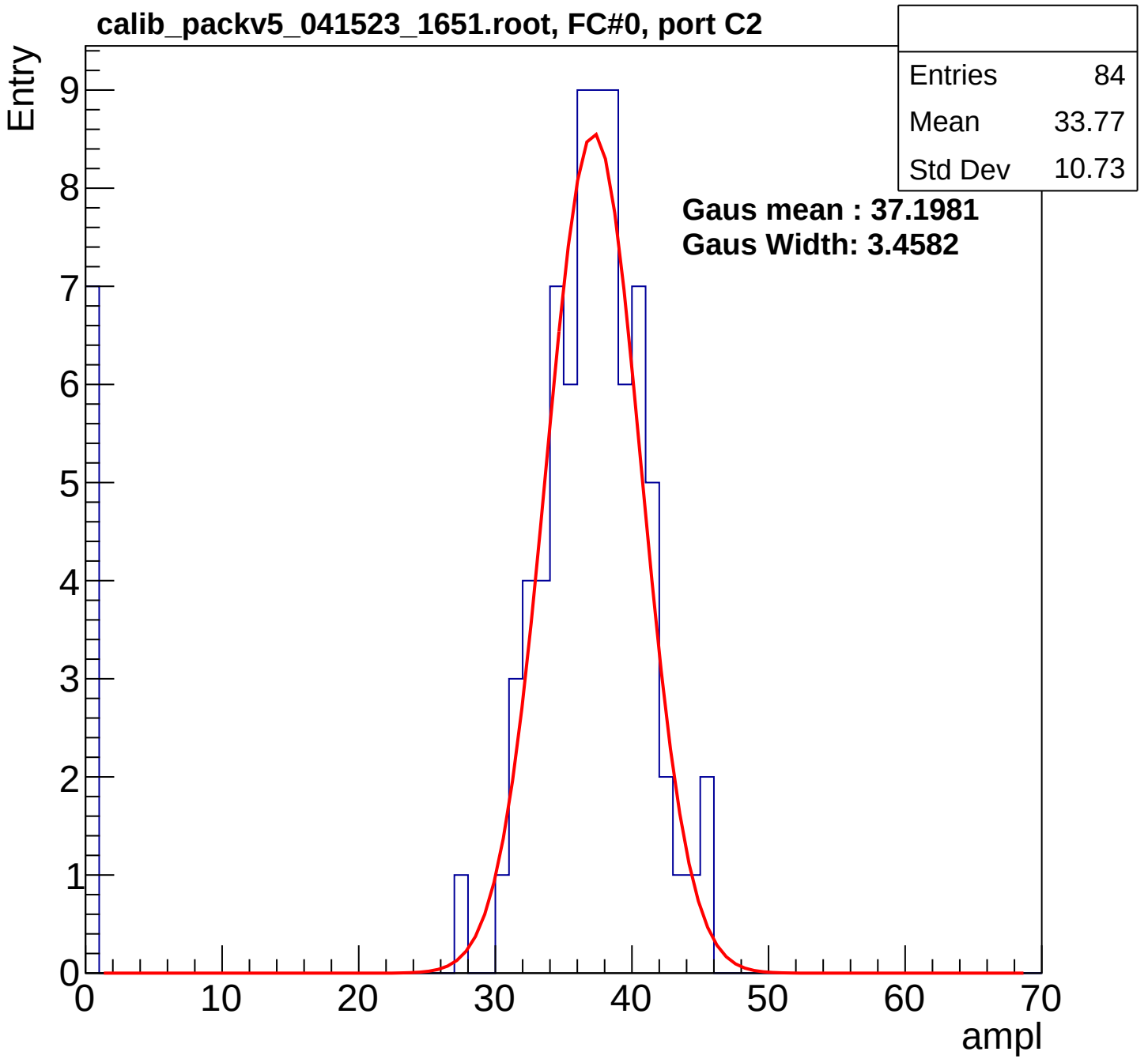

B1L103S, U12-ch43, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 53.57
Std Dev 21.88
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U12-ch43, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch44, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 24.14
Std Dev 11.85
Gaus mean : 30.3864
Gaus Width: 3.1780
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U12-ch44, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 33.77
Std Dev 10.73
Gaus mean : 37.1981
Gaus Width: 3.4582
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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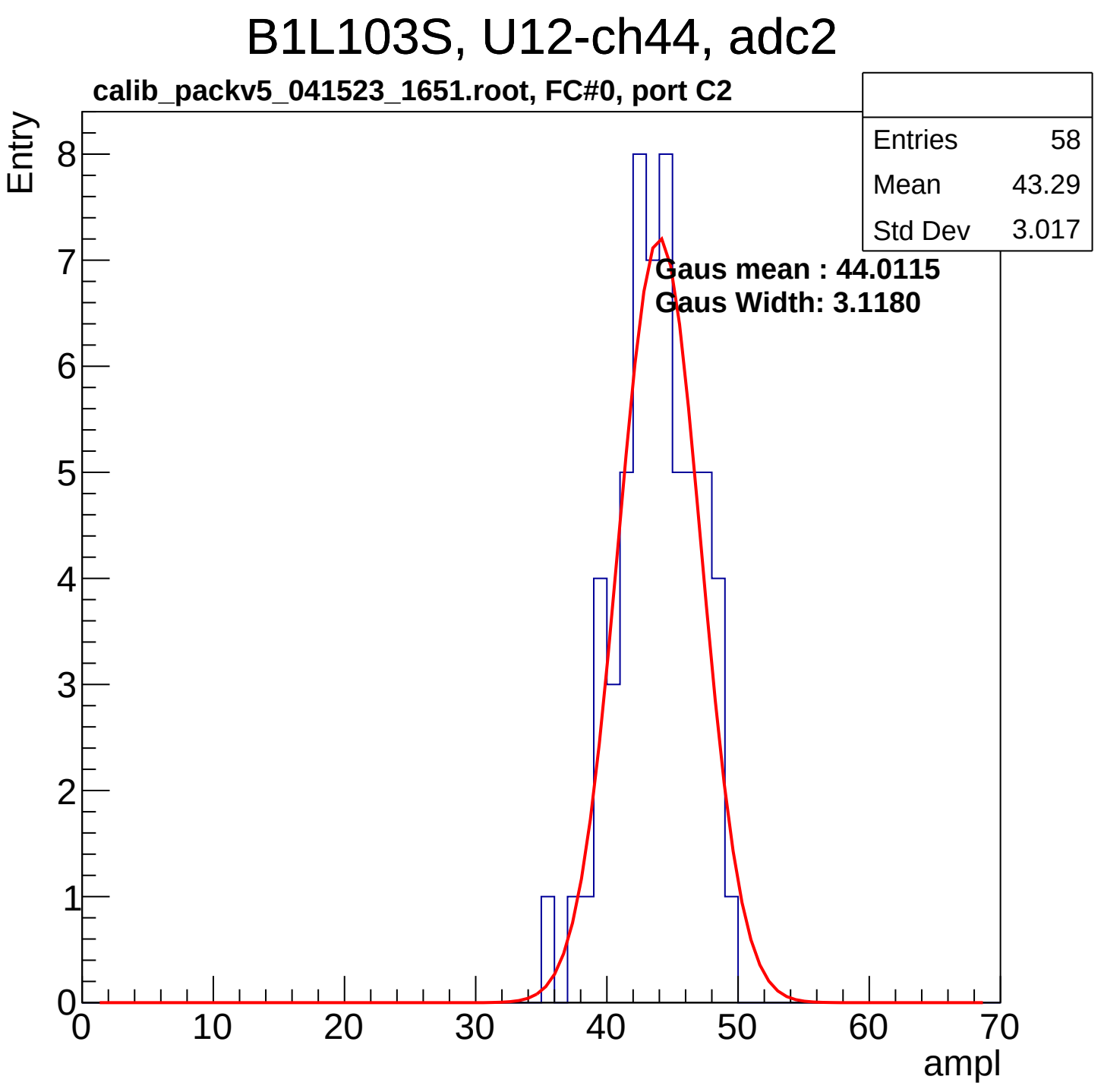
60
70


B1L103S, U12-ch44, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 43.29
Std Dev 3.017
Gaus mean : 44.0115
Gaus Width: 3.1180
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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40
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60
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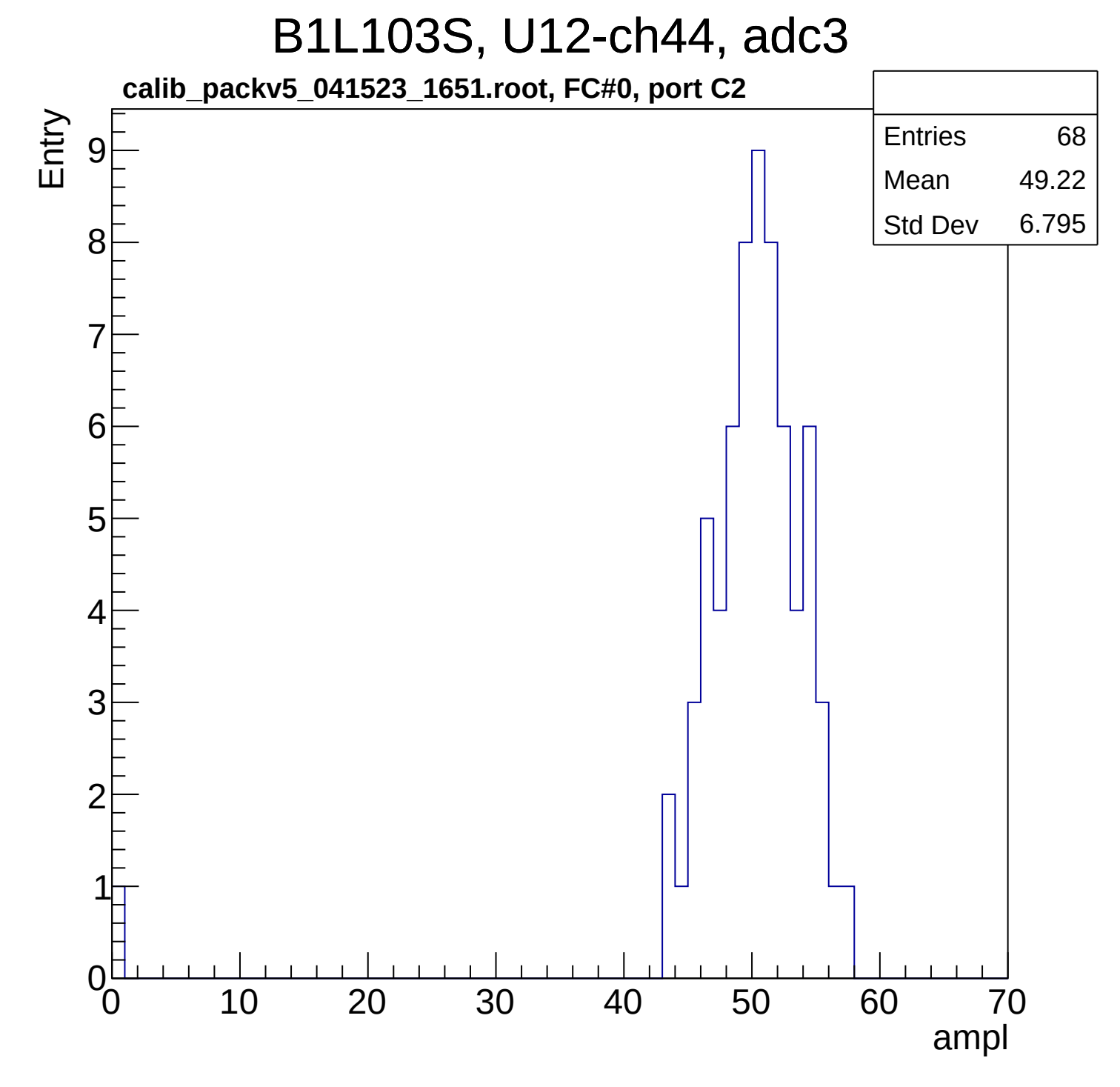
B1L103S, U12-ch44, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 49.22
Std Dev 6.795
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
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60
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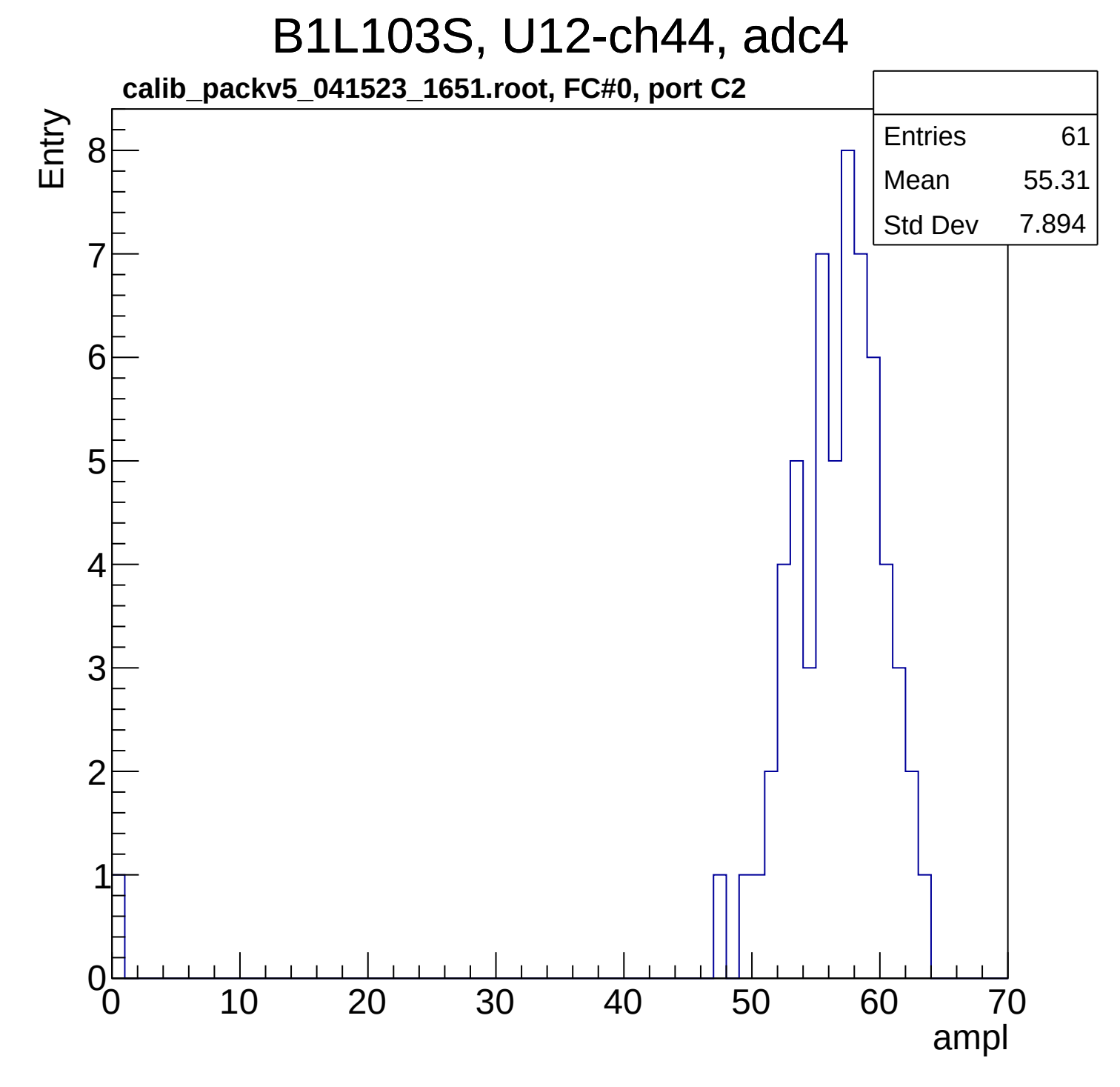
B1L103S, U12-ch44, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 55.31
Std Dev 7.894
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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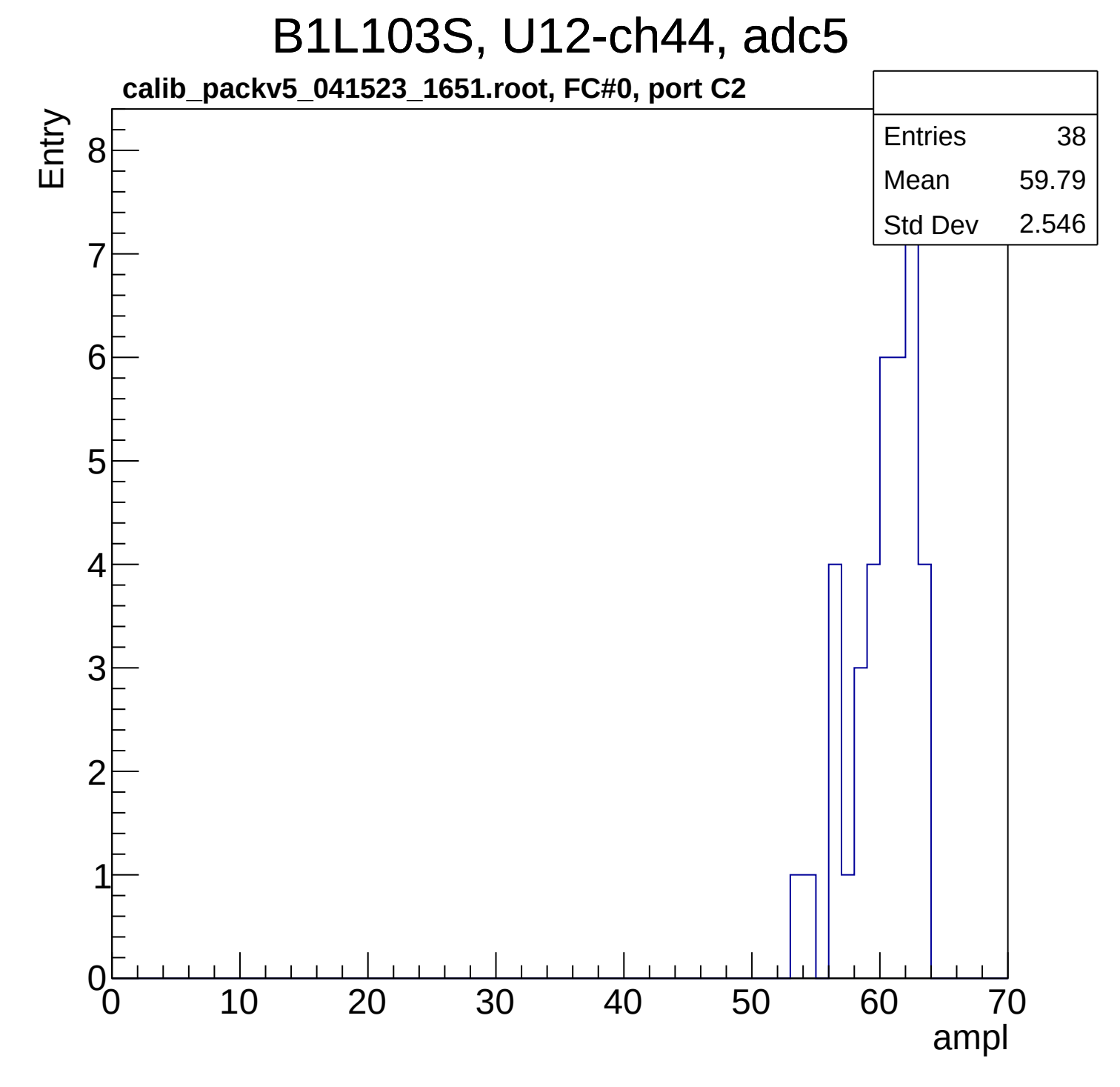
B1L103S, U12-ch44, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 59.79
Std Dev 2.546
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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60
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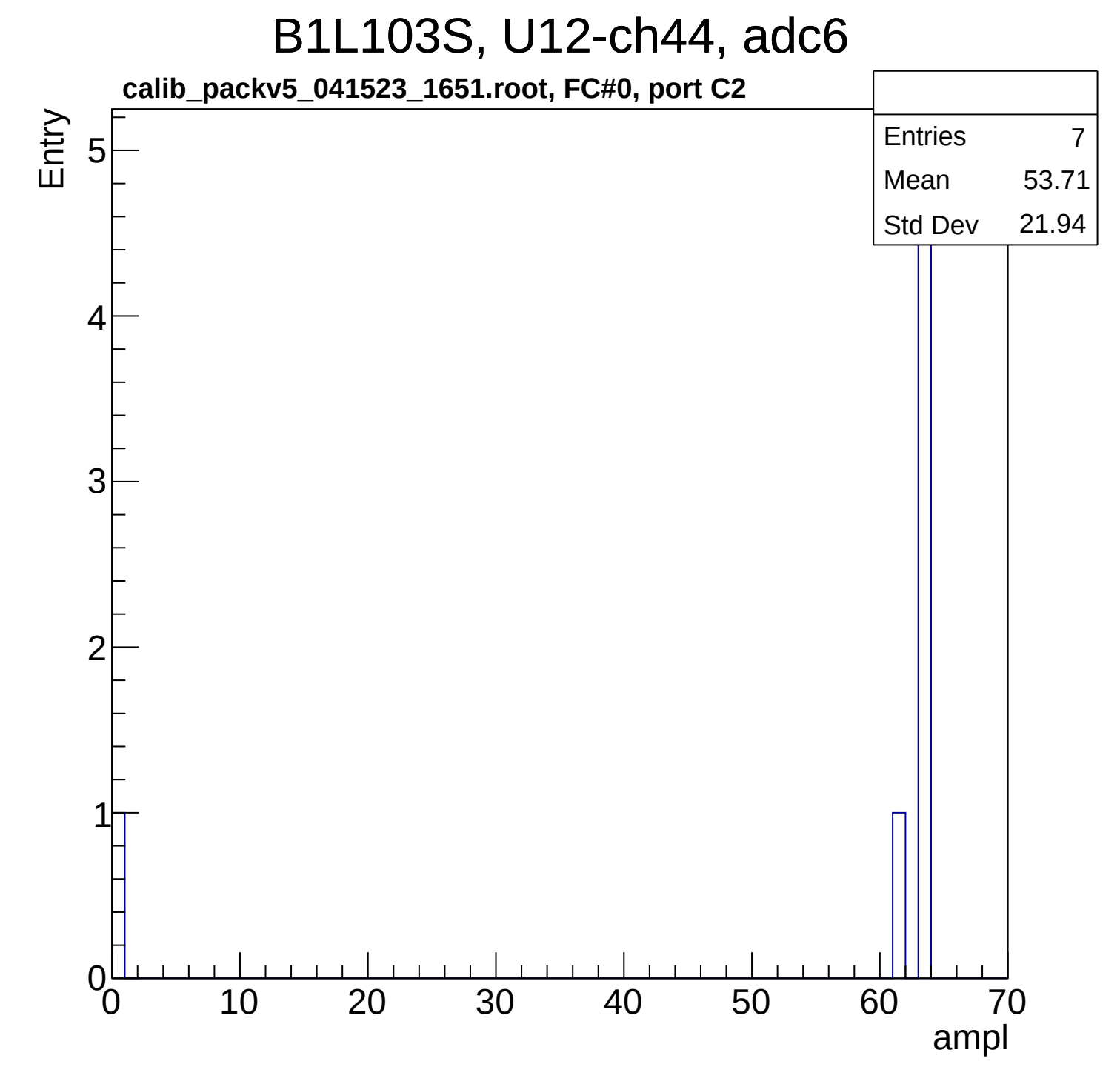
B1L103S, U12-ch44, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 53.71
Std Dev 21.94
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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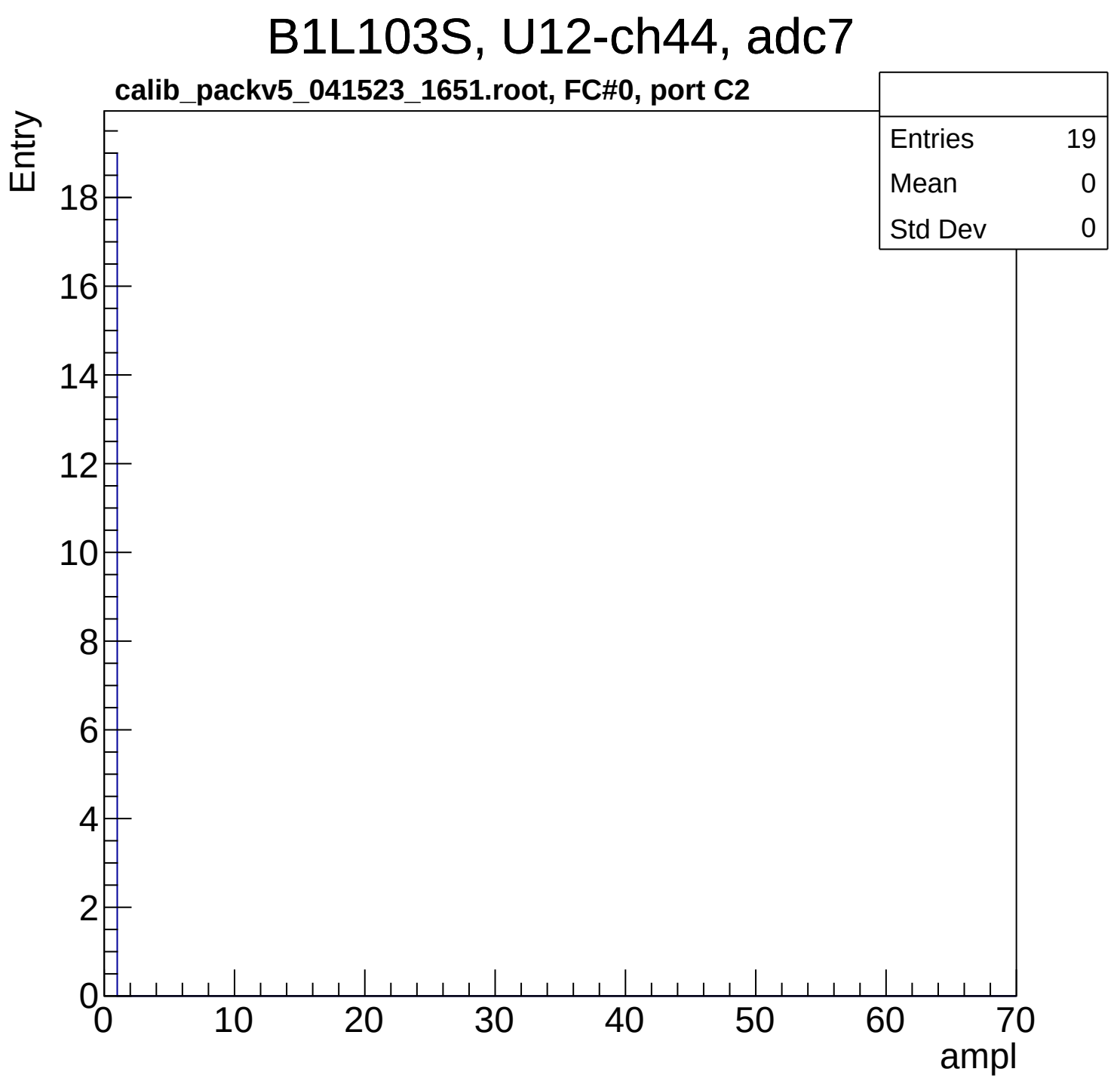
B1L103S, U12-ch44, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
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6
8
10
12
14
16
18
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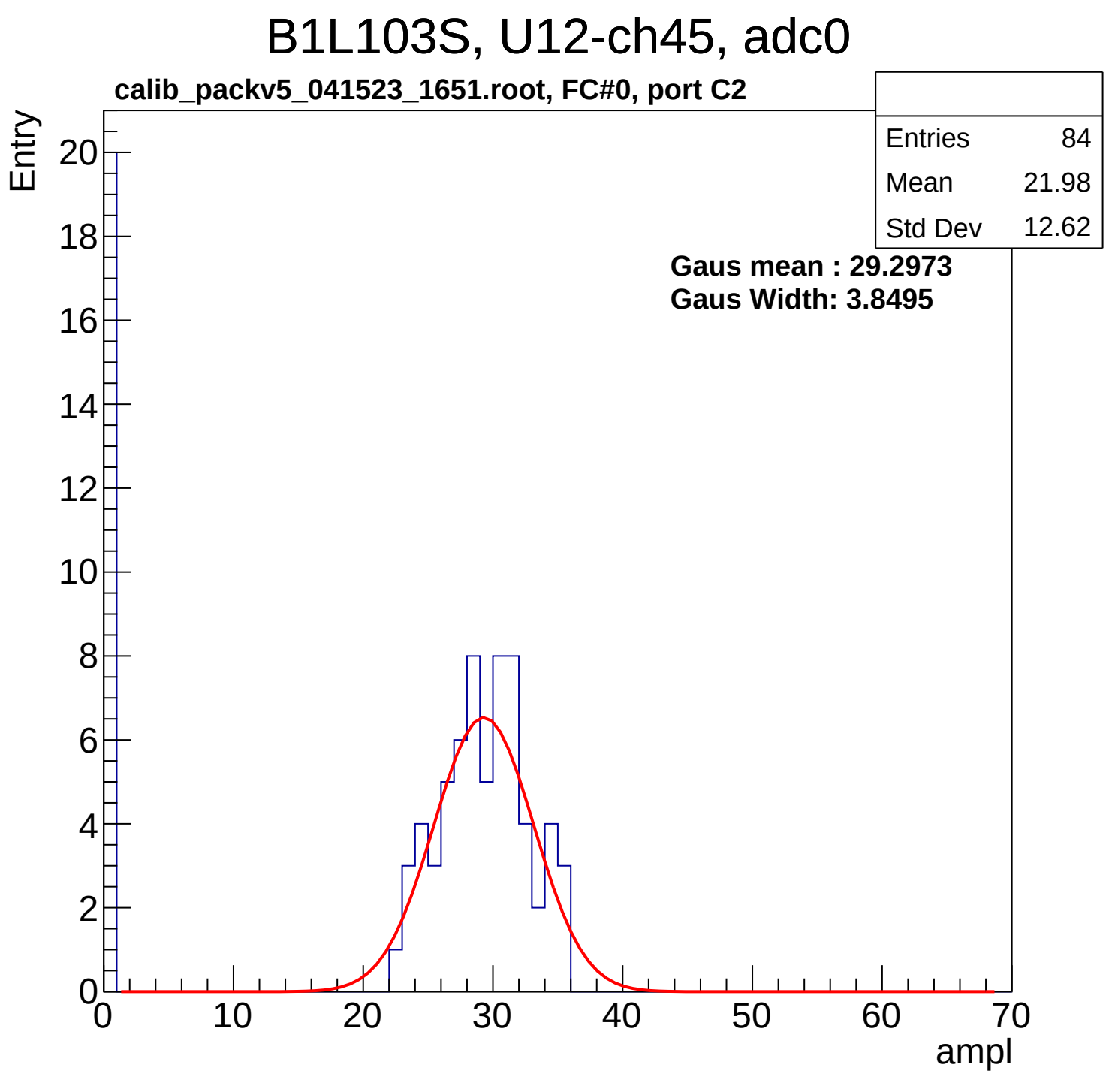
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch45, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 21.98
Std Dev 12.62
Gaus mean : 29.2973
Gaus Width: 3.8495
Entry
ampl
0
2
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6
8
10
12
14
16
18
20
0
10
20
30
40
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60
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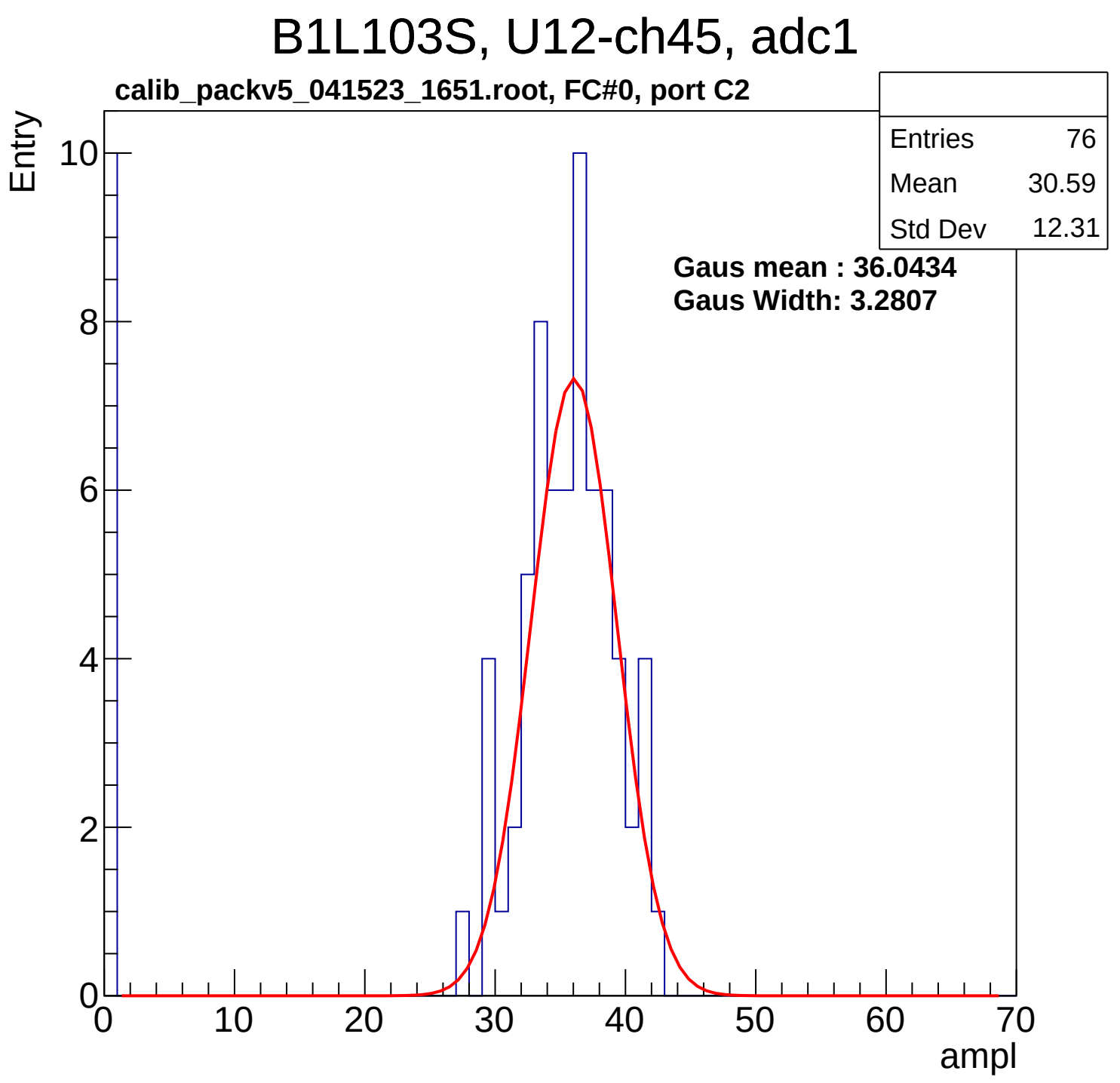
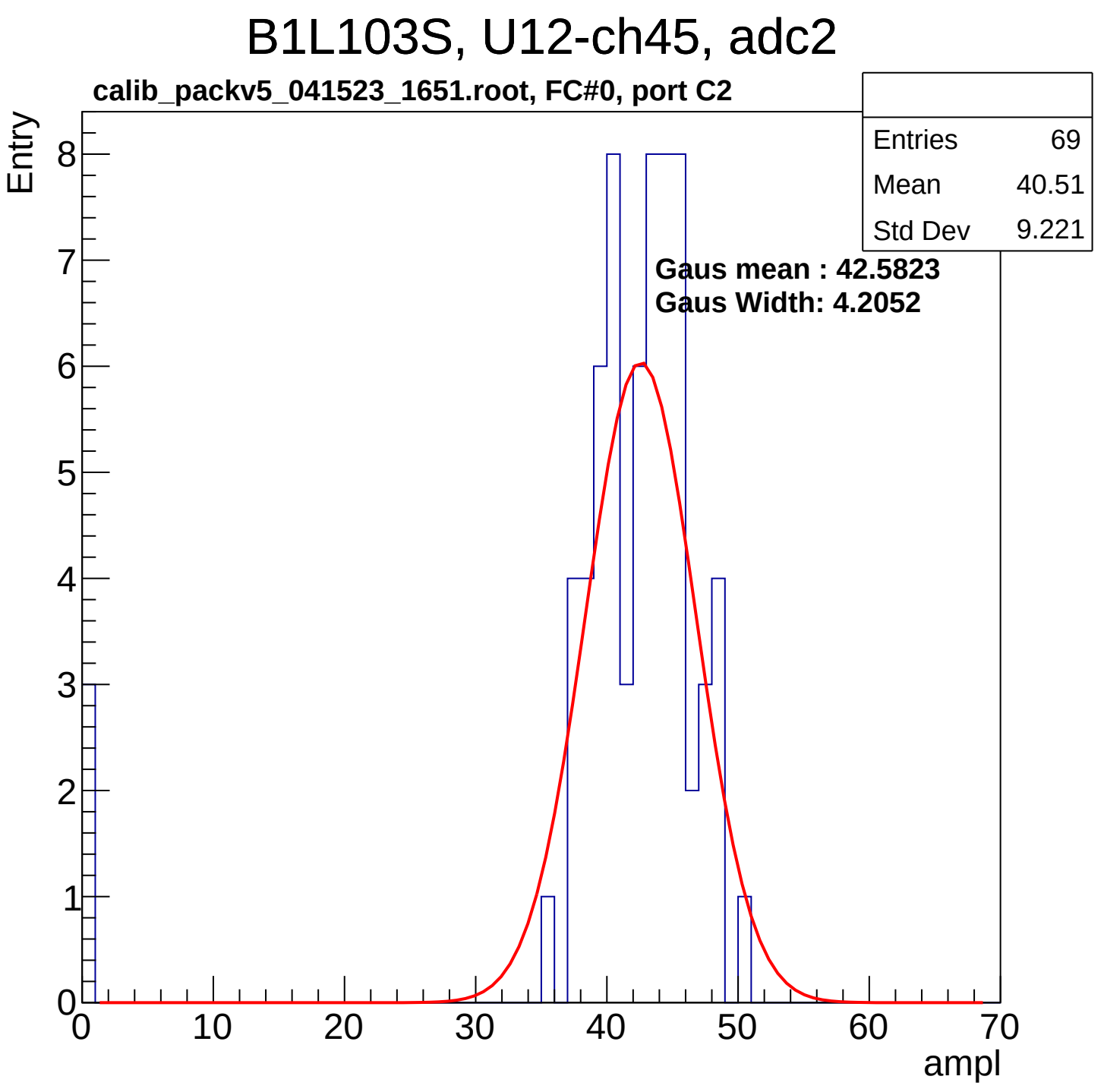

B1L103S, U12-ch45, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 30.59
Std Dev 12.31
Gaus mean : 36.0434
Gaus Width: 3.2807
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch45, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 40.51
Std Dev 9.221
Gaus mean : 42.5823
Gaus Width: 4.2052
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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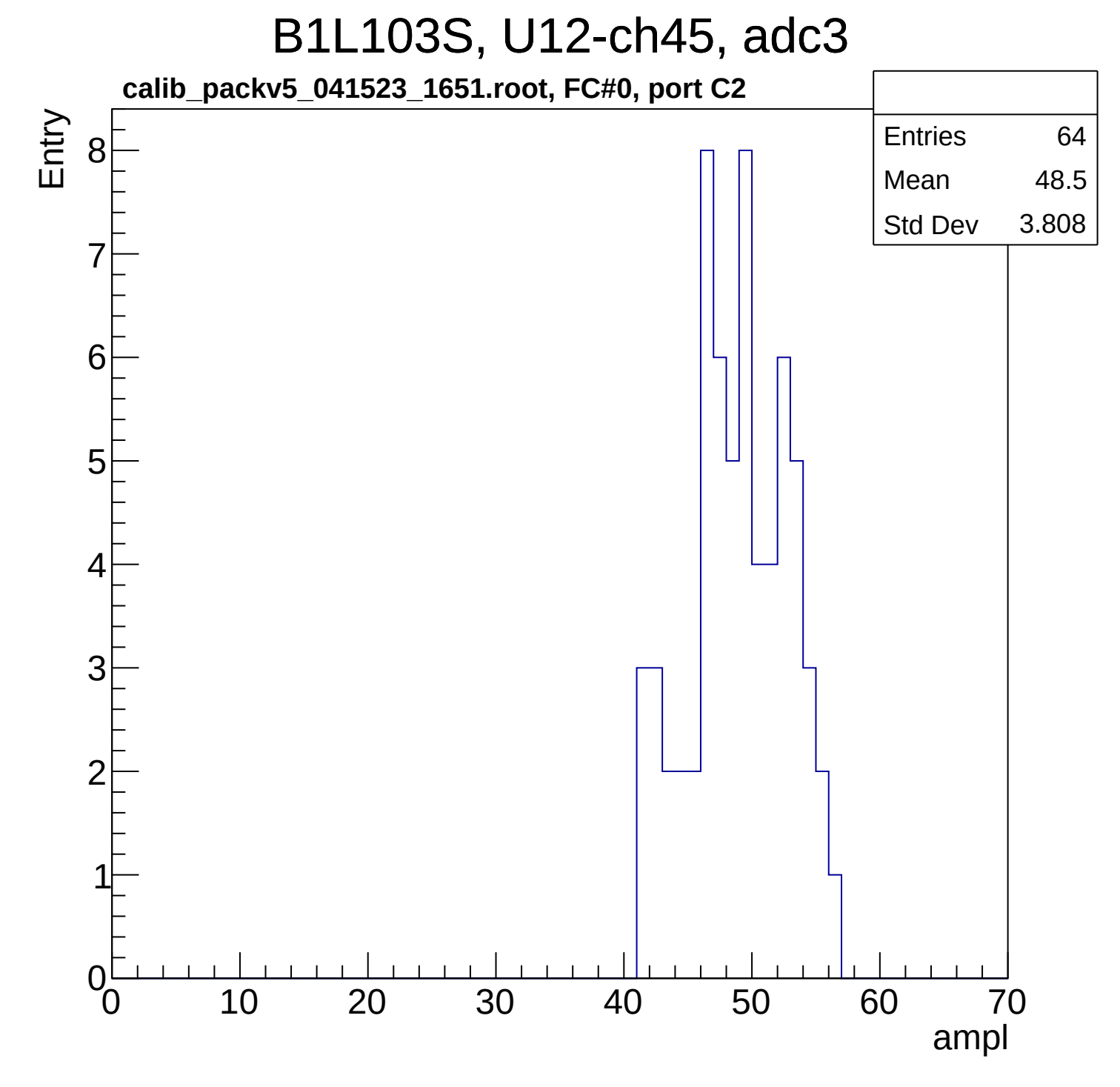
B1L103S, U12-ch45, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 48.5
Std Dev 3.808
Entry
ampl
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2
3
4
5
6
7
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0
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20
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40
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60
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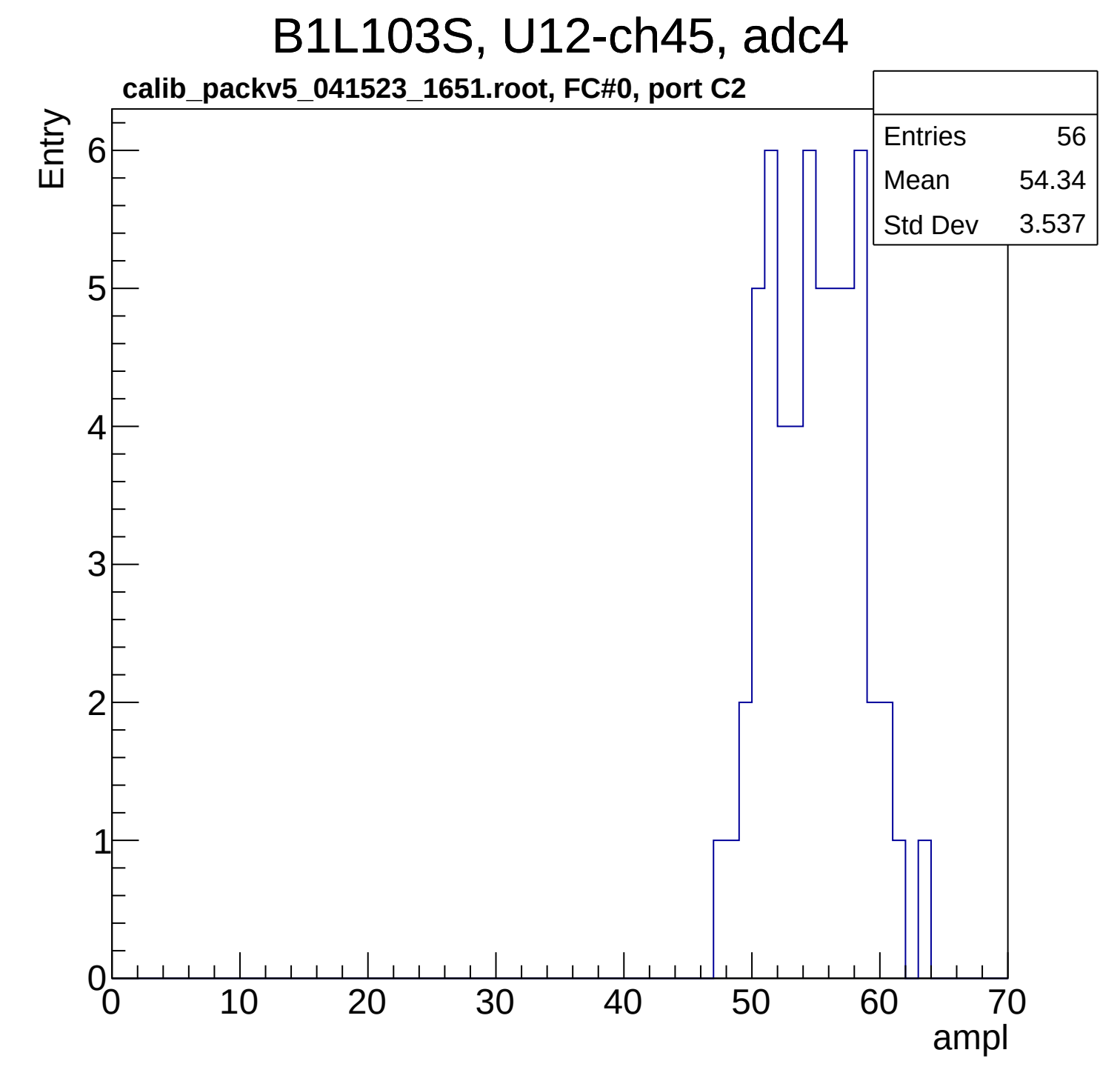
B1L103S, U12-ch45, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 54.34
Std Dev 3.537
Entry
ampl
0
1
2
3
4
5
6
0
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20
30
40
50
60
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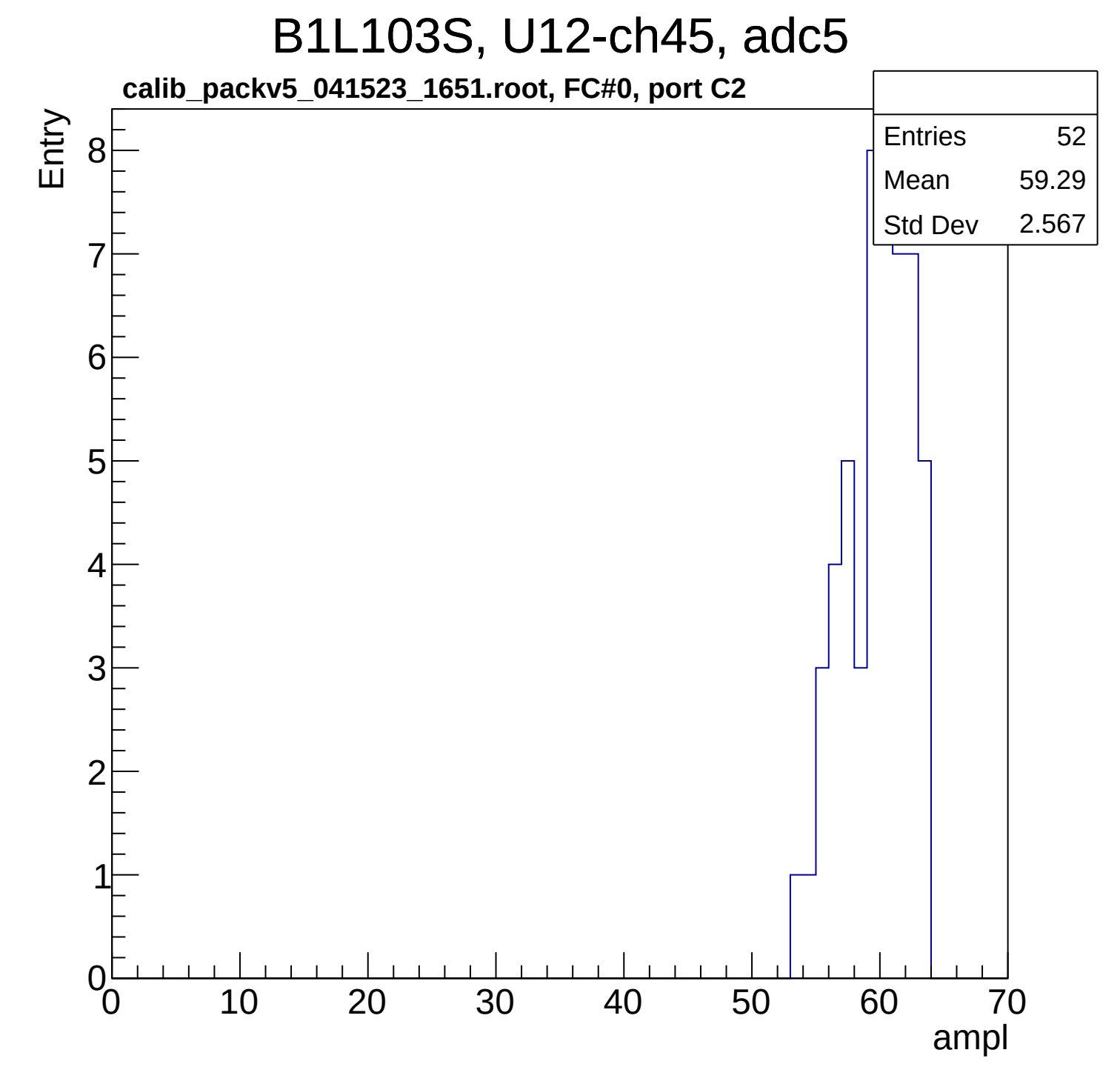
B1L103S, U12-ch45, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 59.29
Std Dev 2.567
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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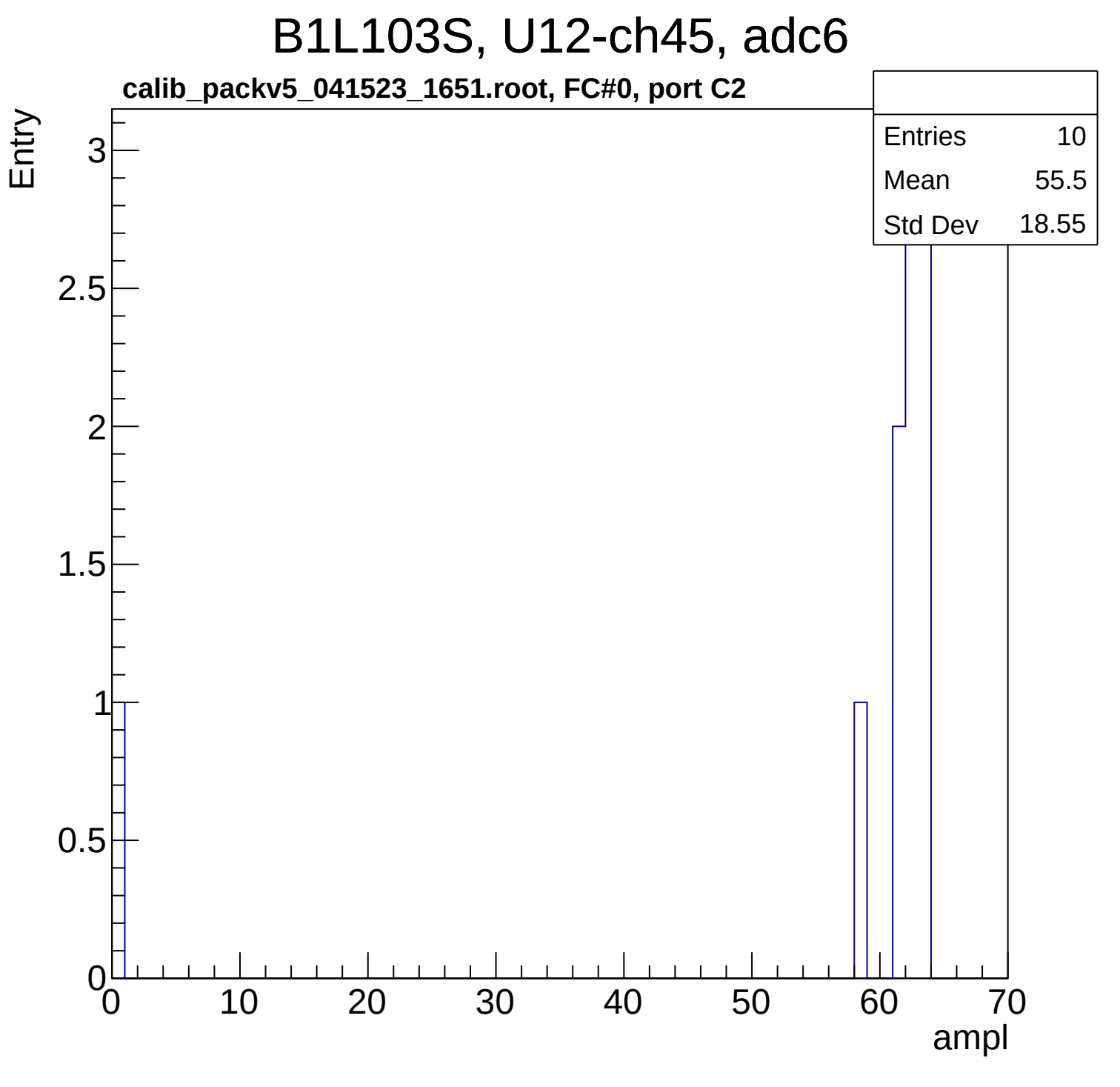
B1L103S, U12-ch45, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.5
Std Dev 18.55
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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60
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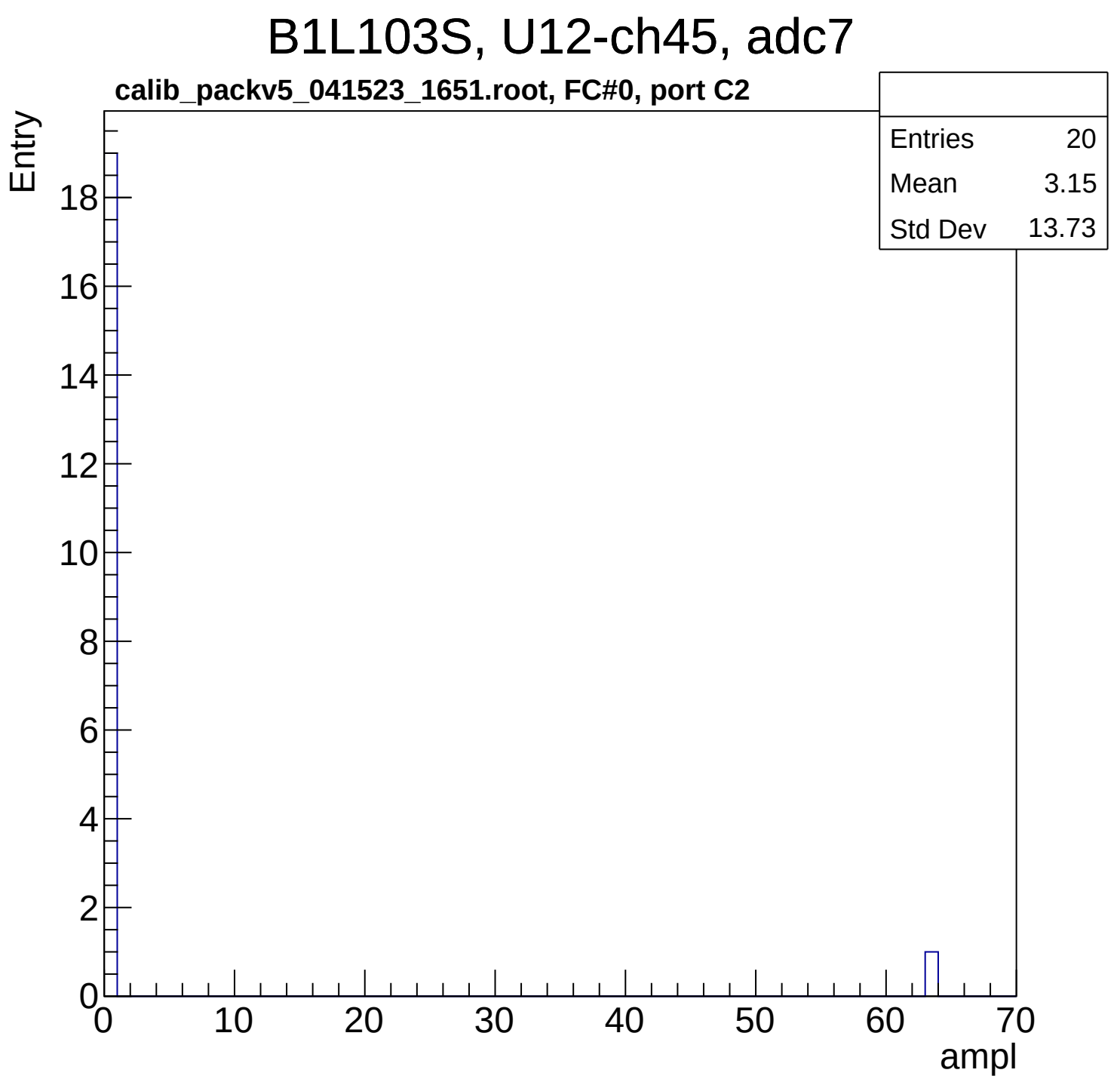
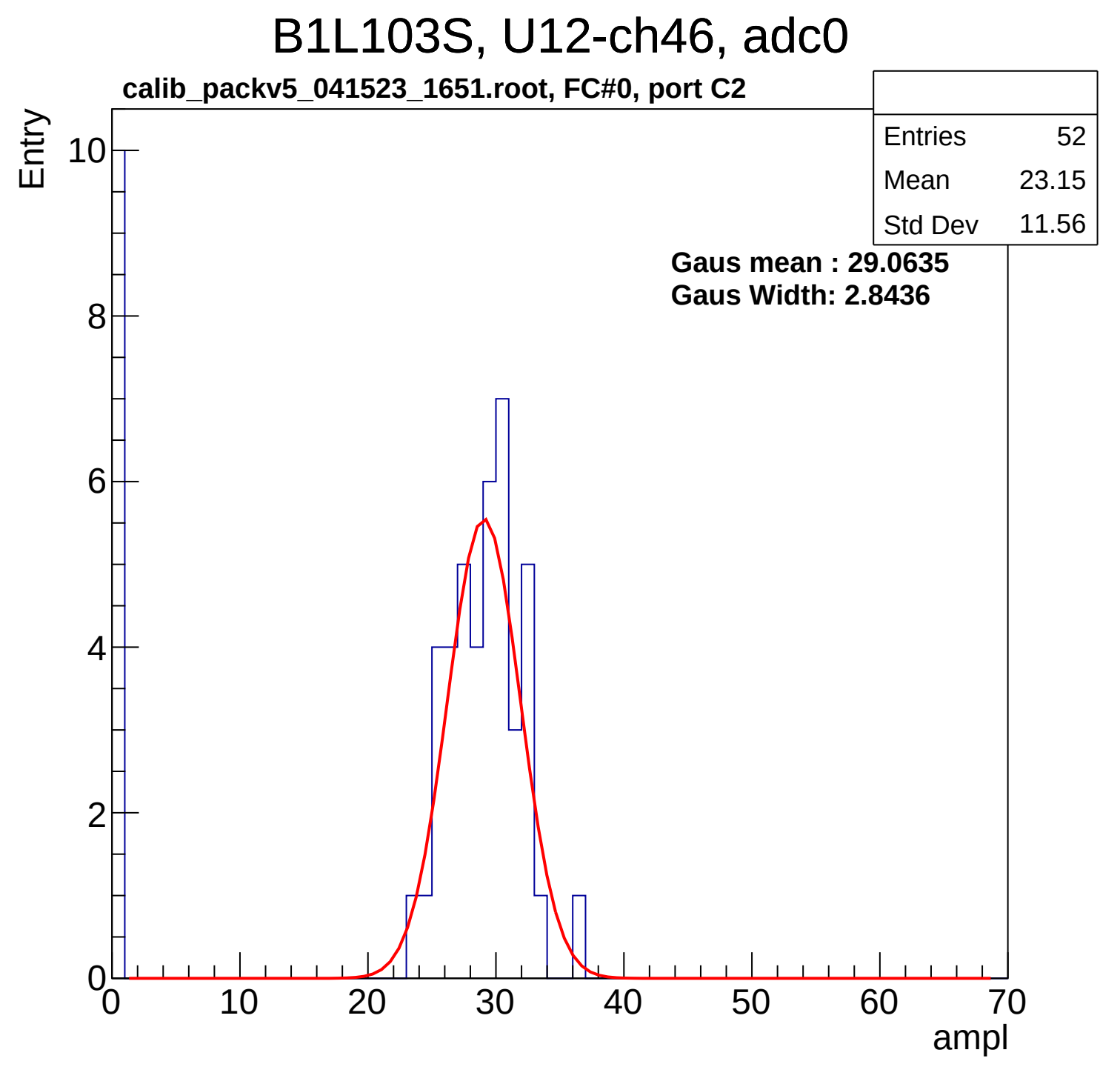
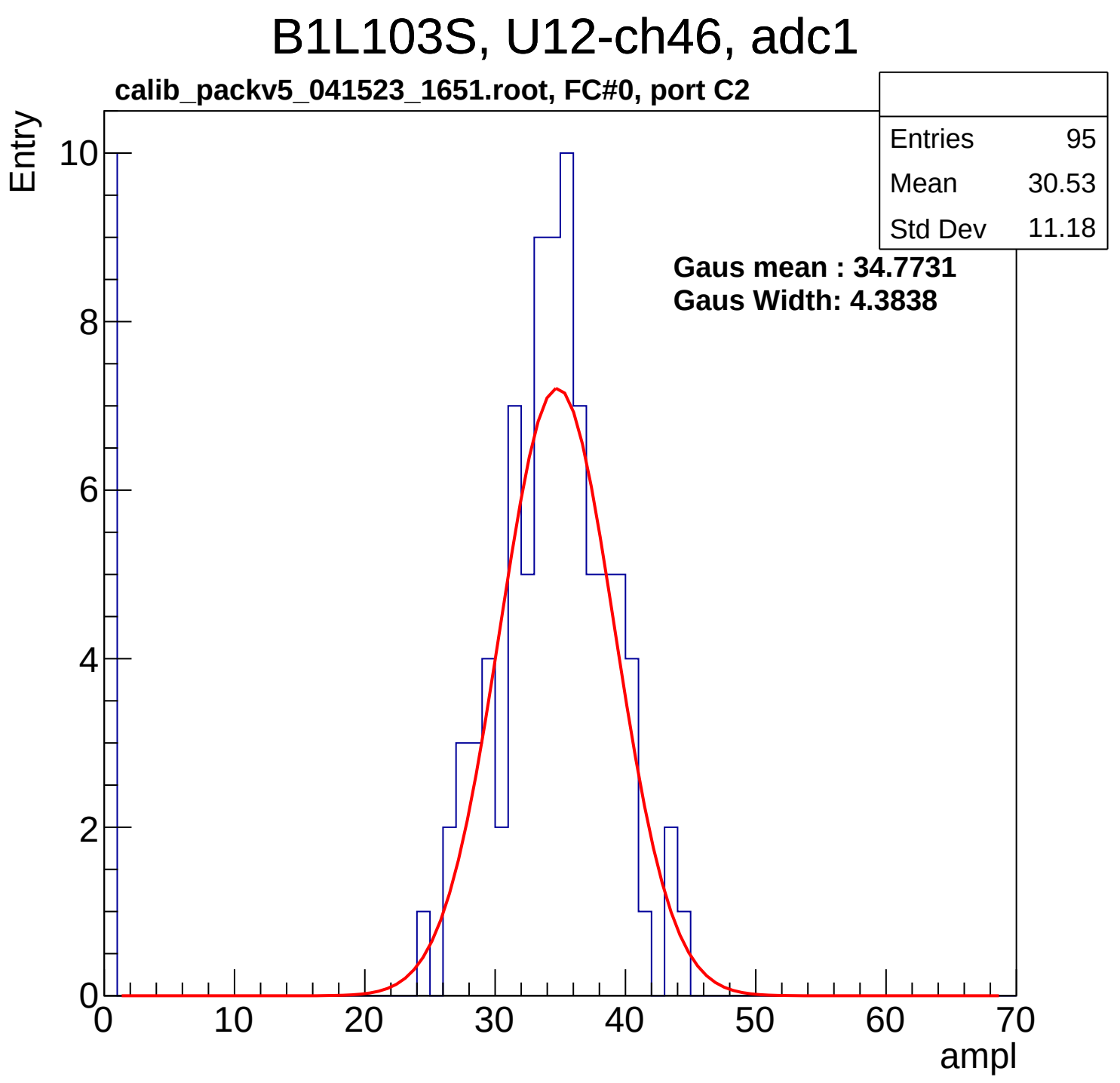

B1L103S, U12-ch45, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch46, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 23.15
Std Dev 11.56
Gaus mean : 29.0635
Gaus Width: 2.8436
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch46, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 30.53
Std Dev 11.18
Gaus mean : 34.7731
Gaus Width: 4.3838
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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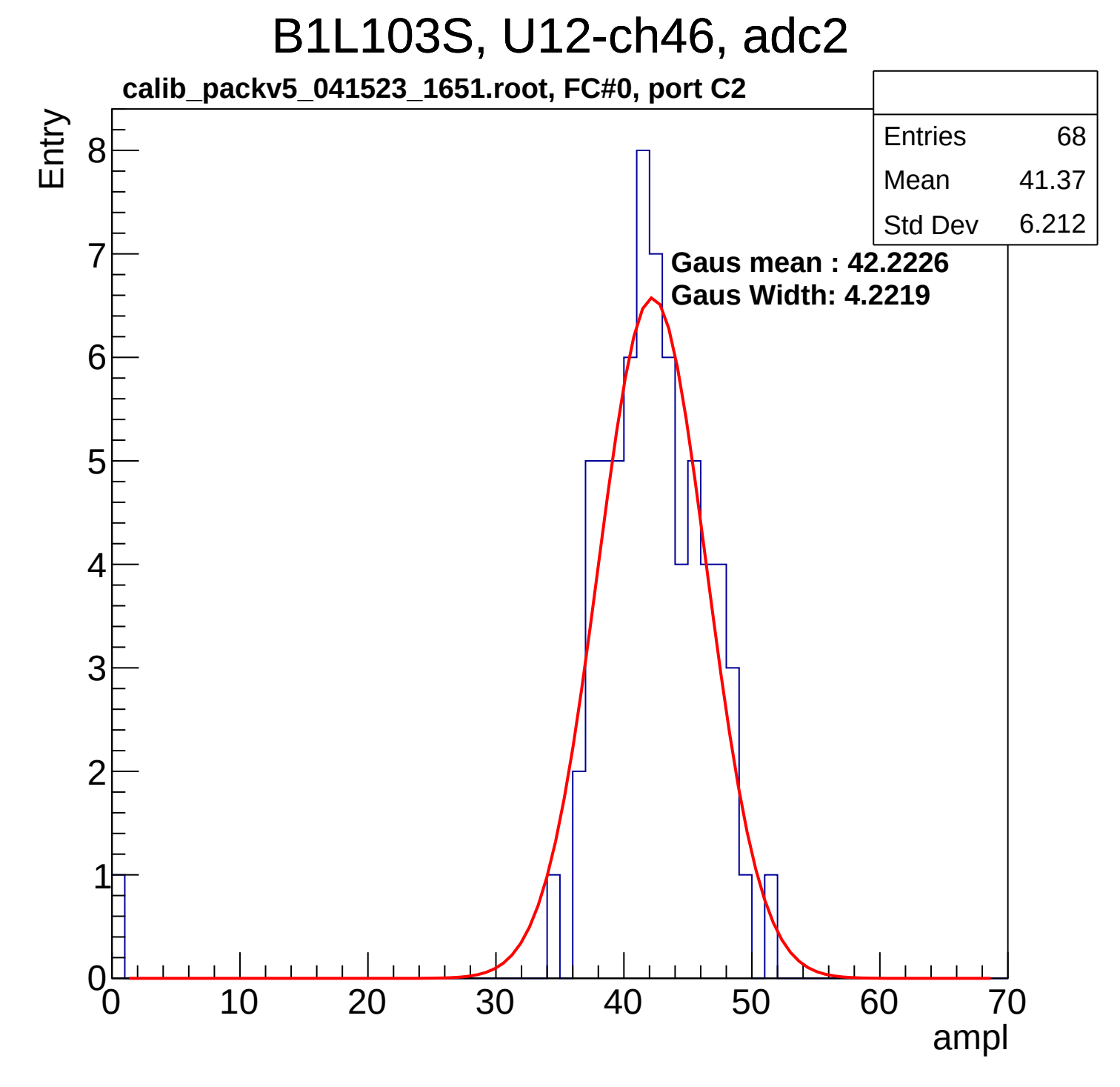
B1L103S, U12-ch46, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 41.37
Std Dev 6.212
Gaus mean : 42.2226
Gaus Width: 4.2219
Entry
ampl
0
1
2
3
4
5
6
7
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0
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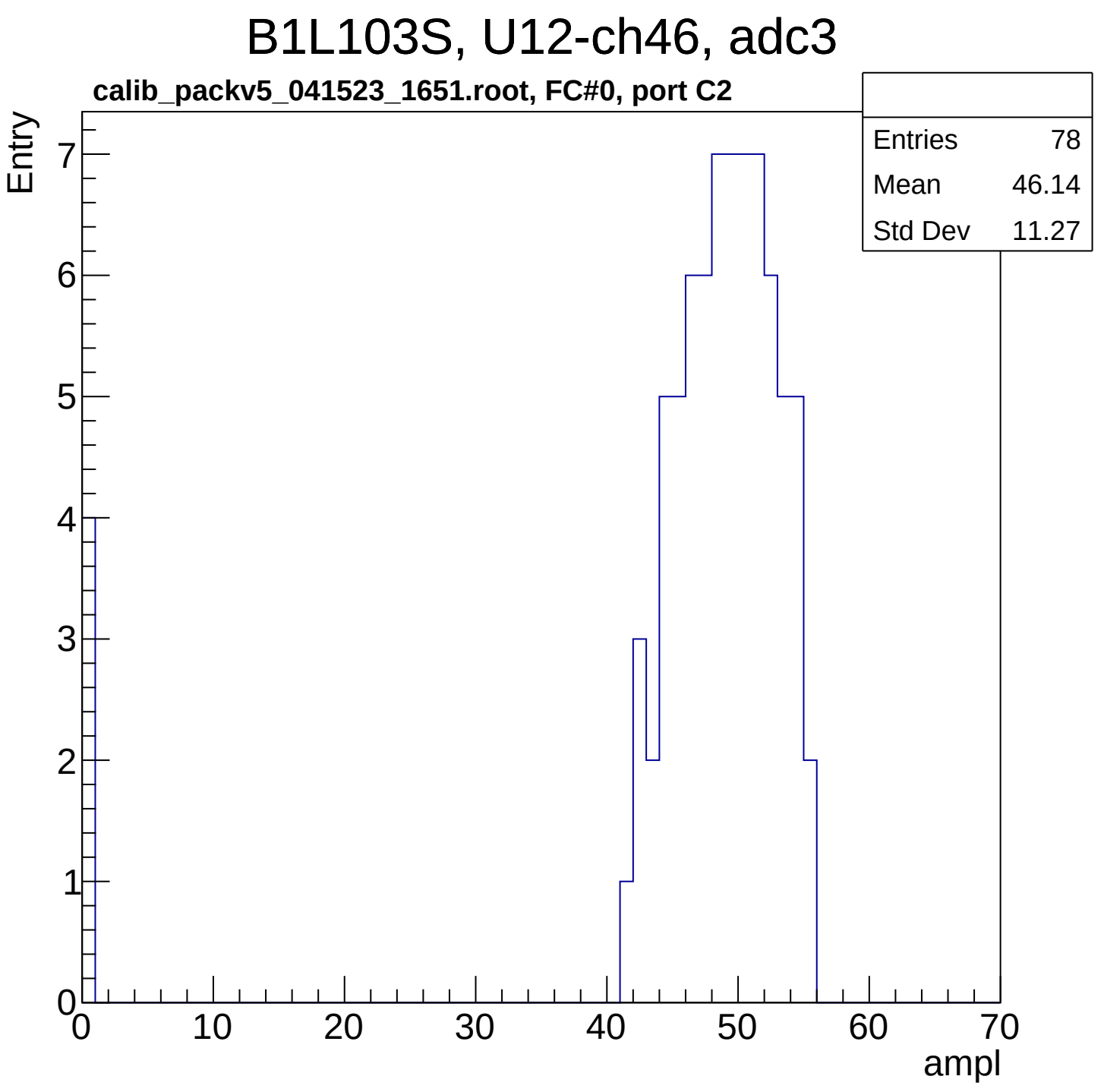
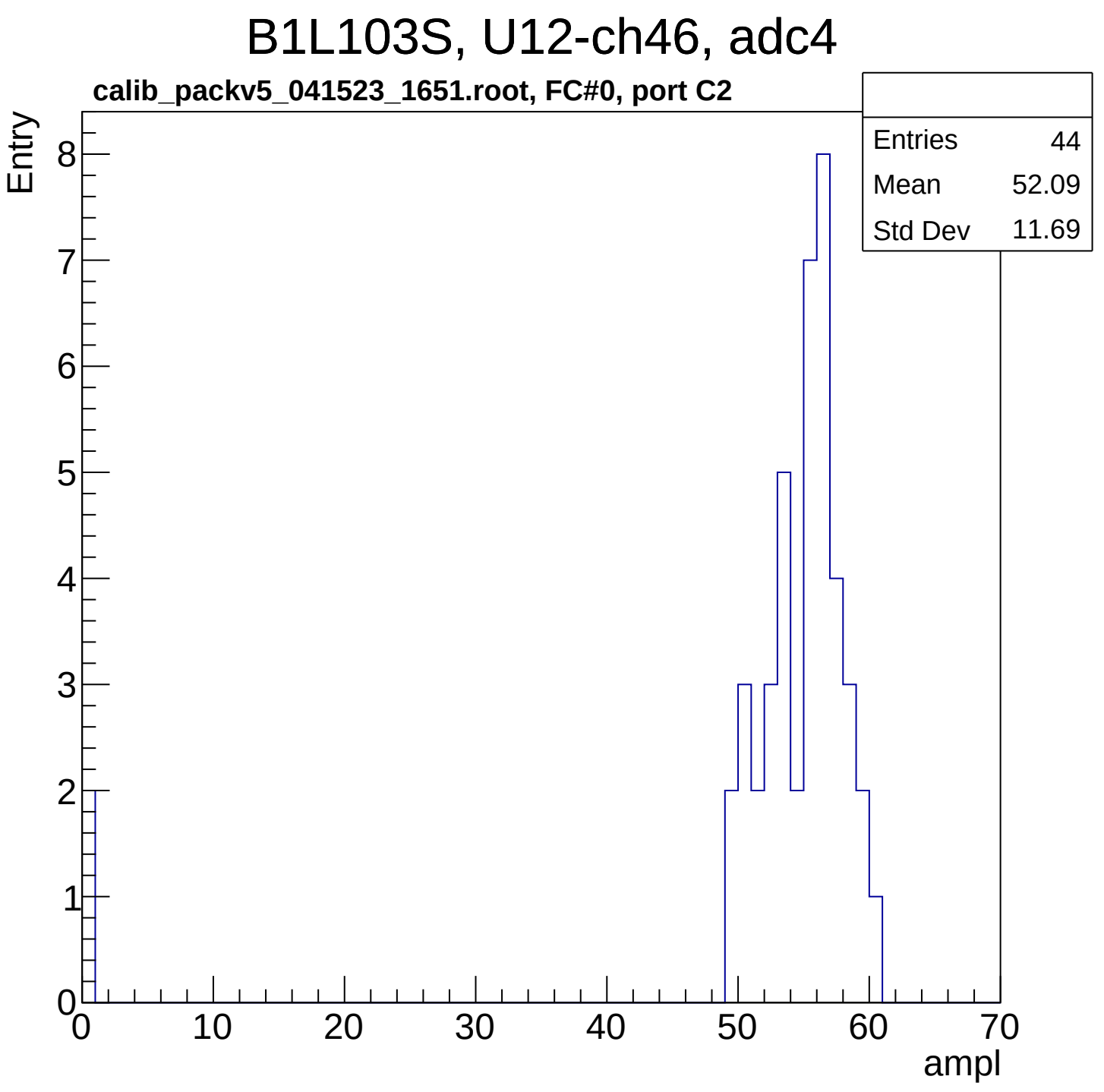

B1L103S, U12-ch46, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 46.14
Std Dev 11.27
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U12-ch46, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 52.09
Std Dev 11.69
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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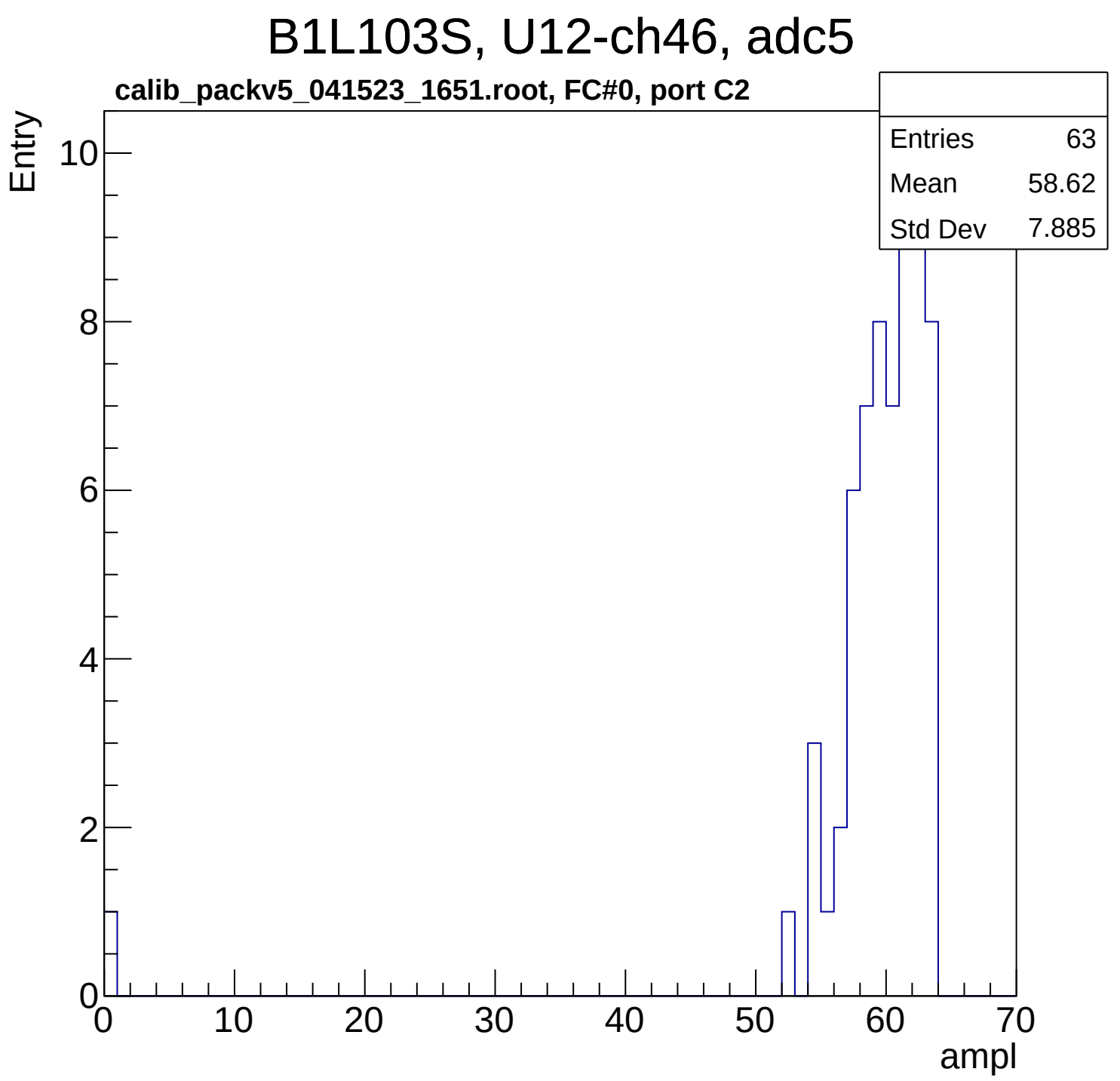
B1L103S, U12-ch46, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 58.62
Std Dev 7.885
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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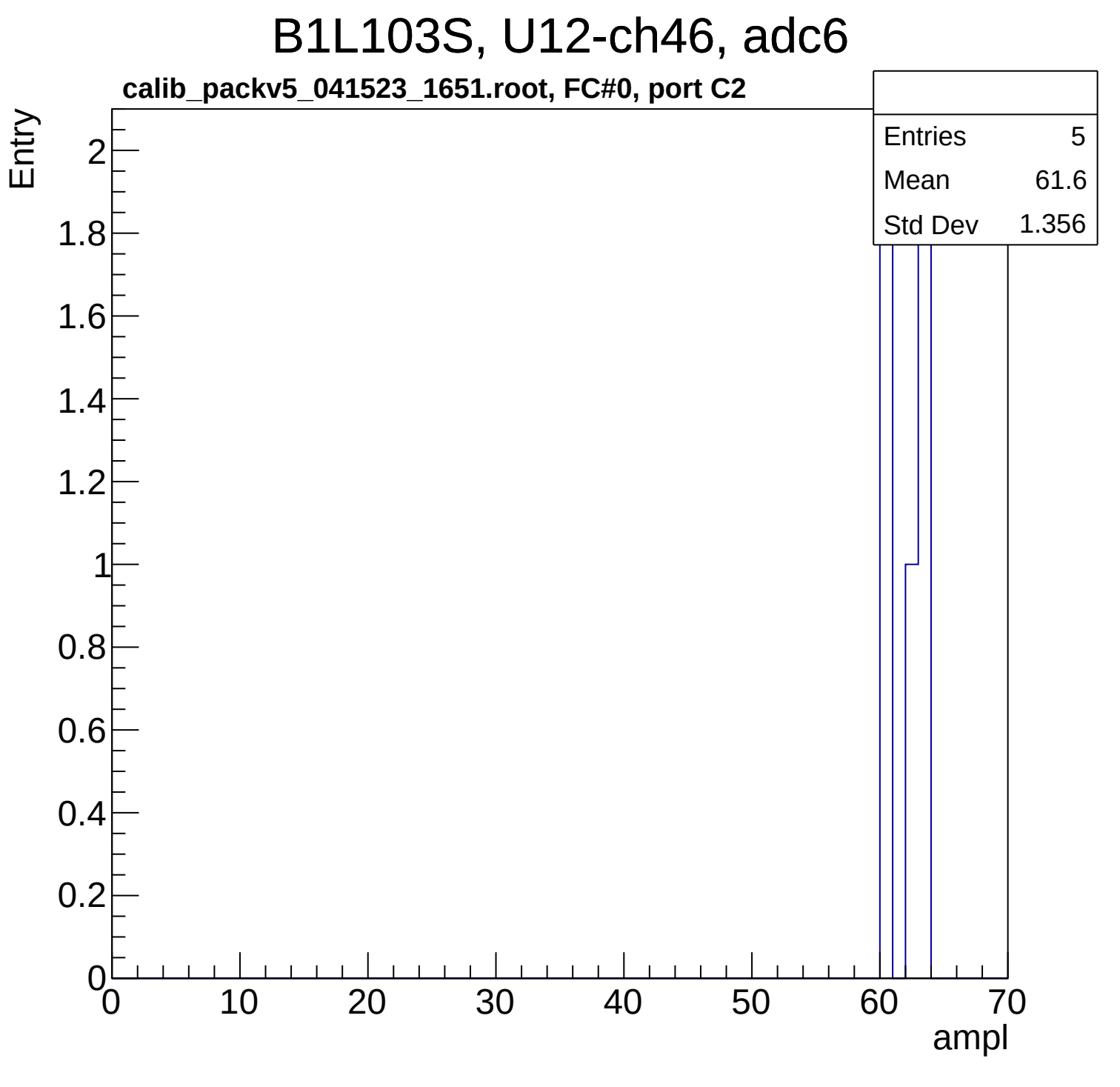
B1L103S, U12-ch46, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.6
Std Dev 1.356
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
50
60
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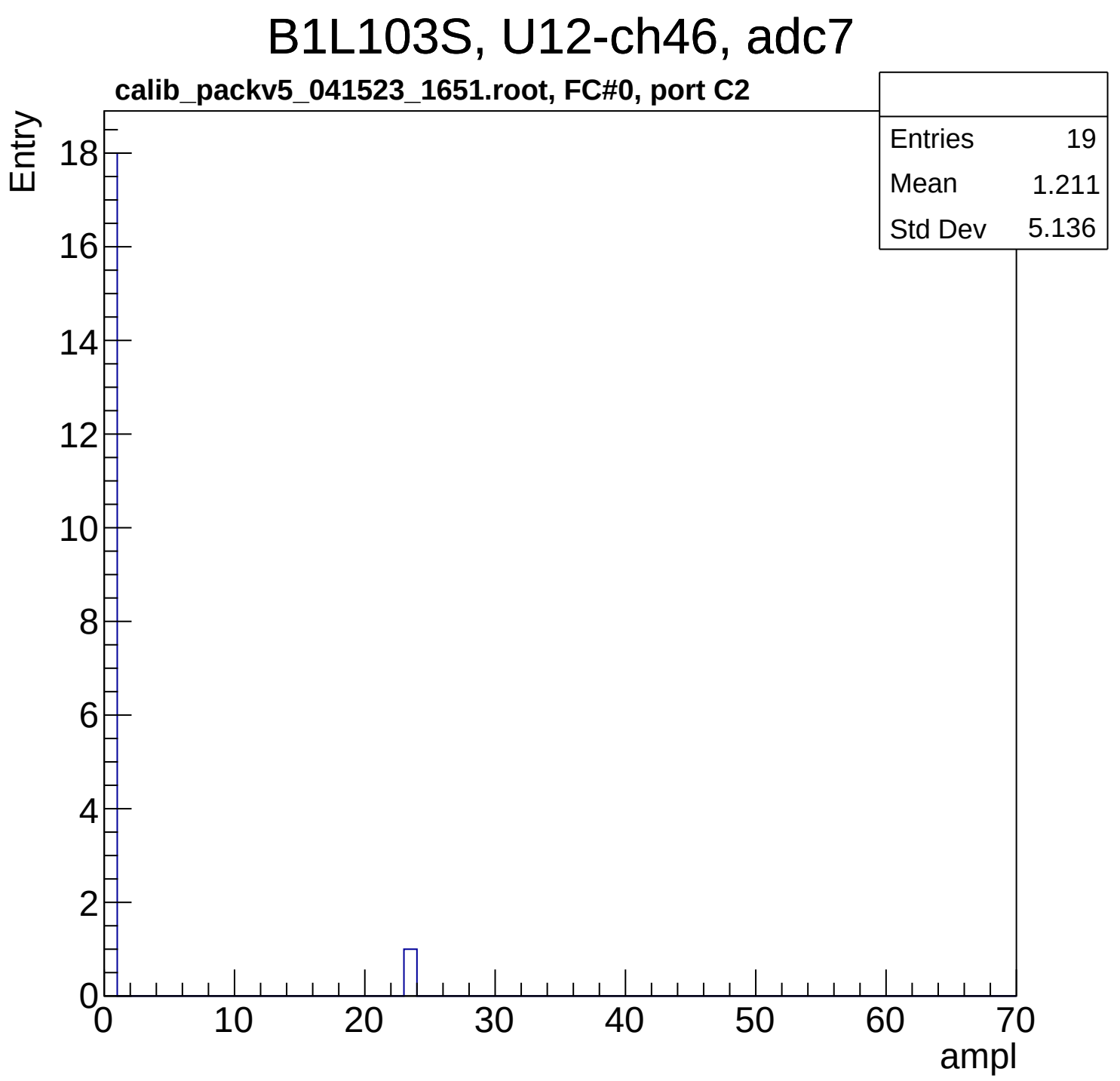
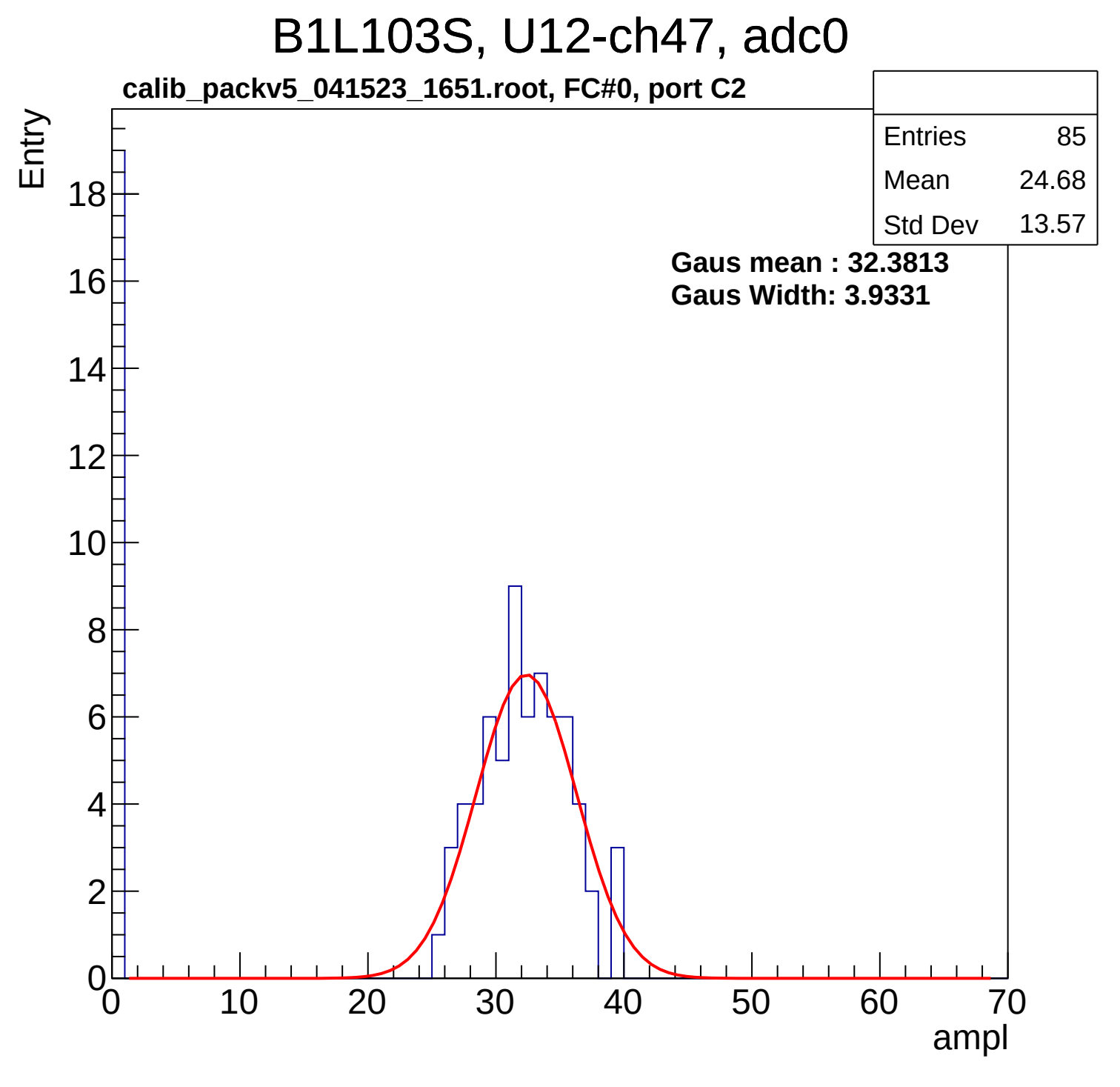

B1L103S, U12-ch46, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.211
Std Dev 5.136
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch47, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 24.68
Std Dev 13.57
Gaus mean : 32.3813
Gaus Width: 3.9331
Entry
ampl
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2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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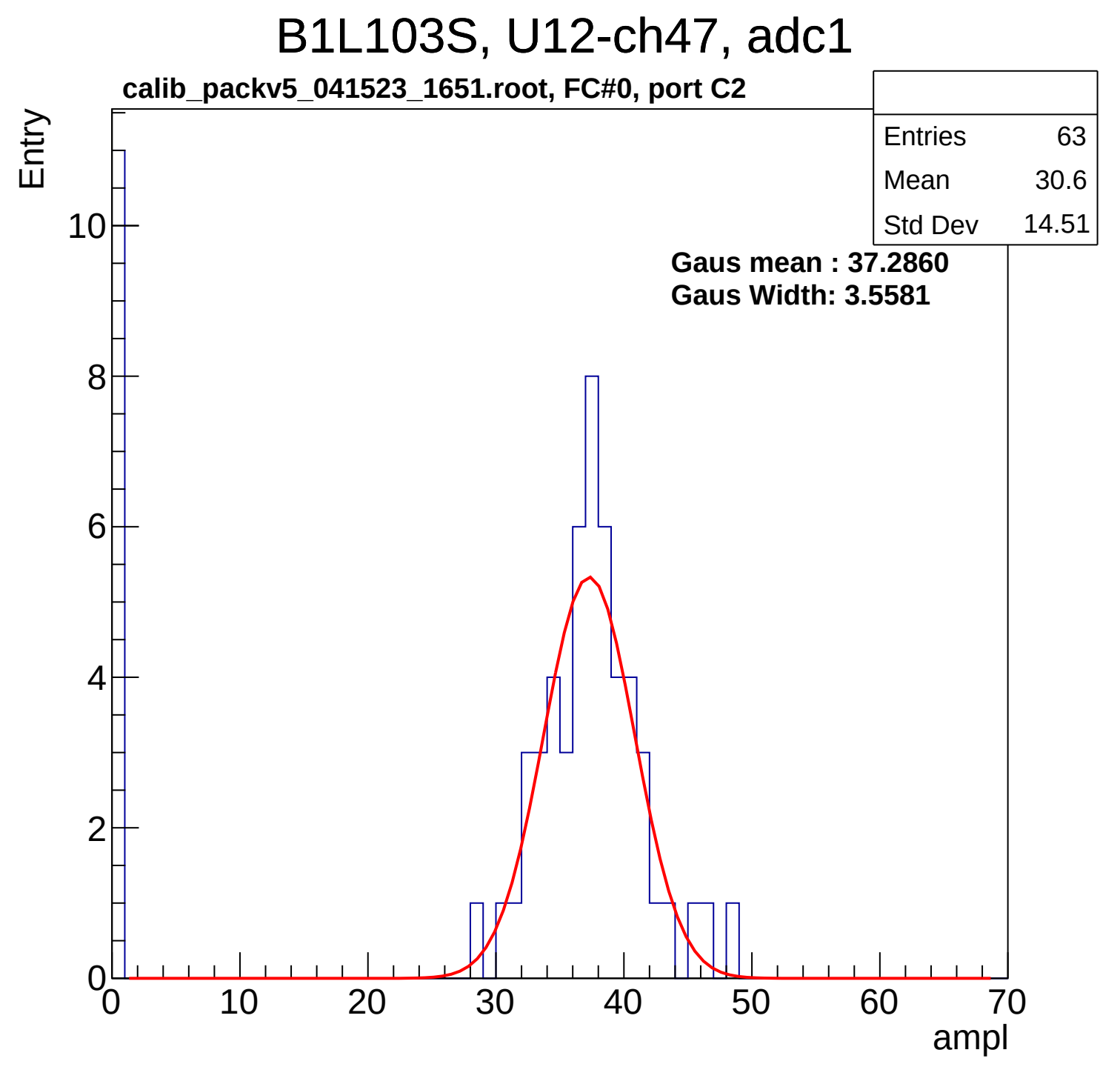
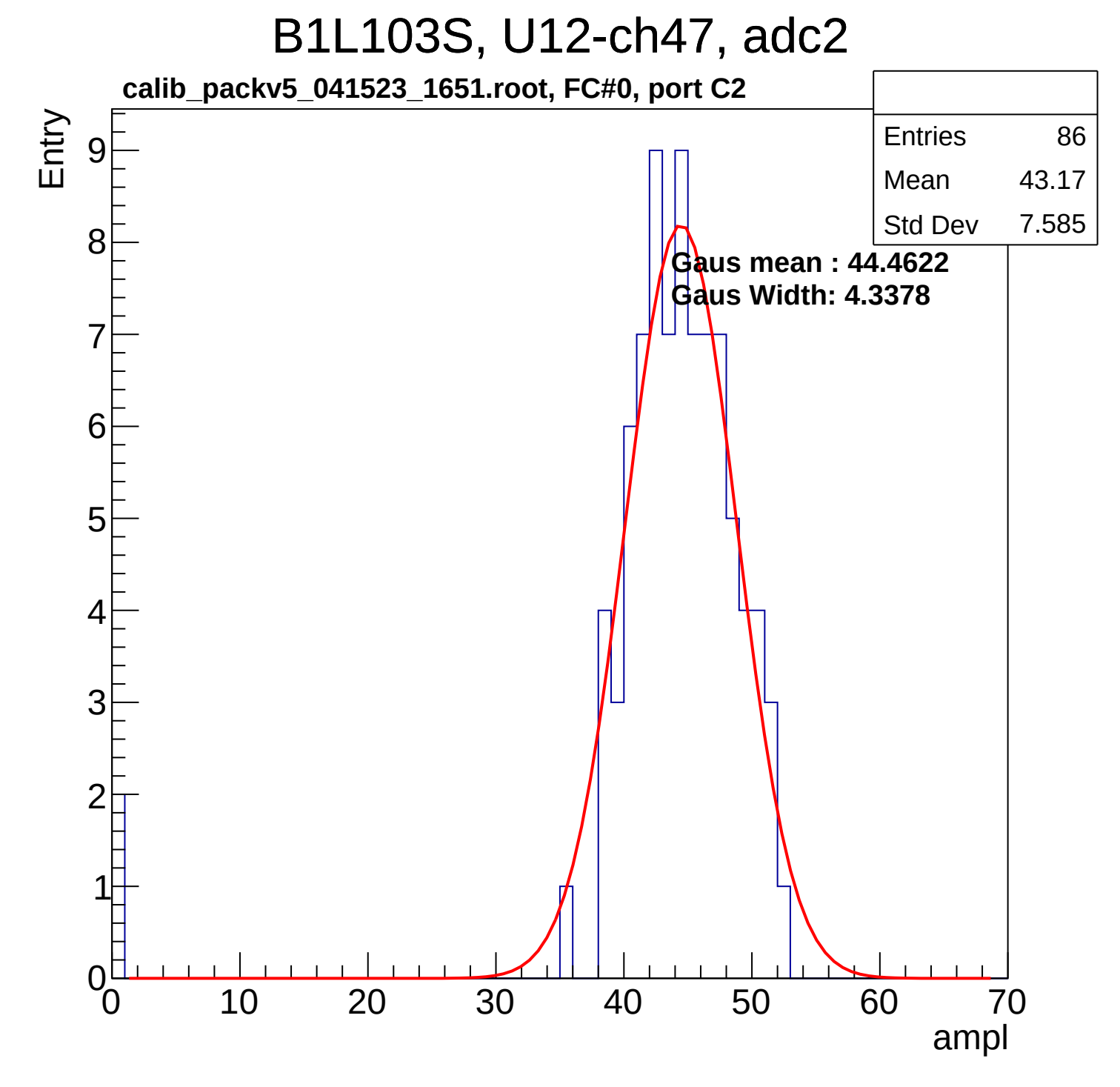

B1L103S, U12-ch47, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 30.6
Std Dev 14.51
Gaus mean : 37.2860
Gaus Width: 3.5581
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch47, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 43.17
Std Dev 7.585
Gaus mean : 44.4622
Gaus Width: 4.3378
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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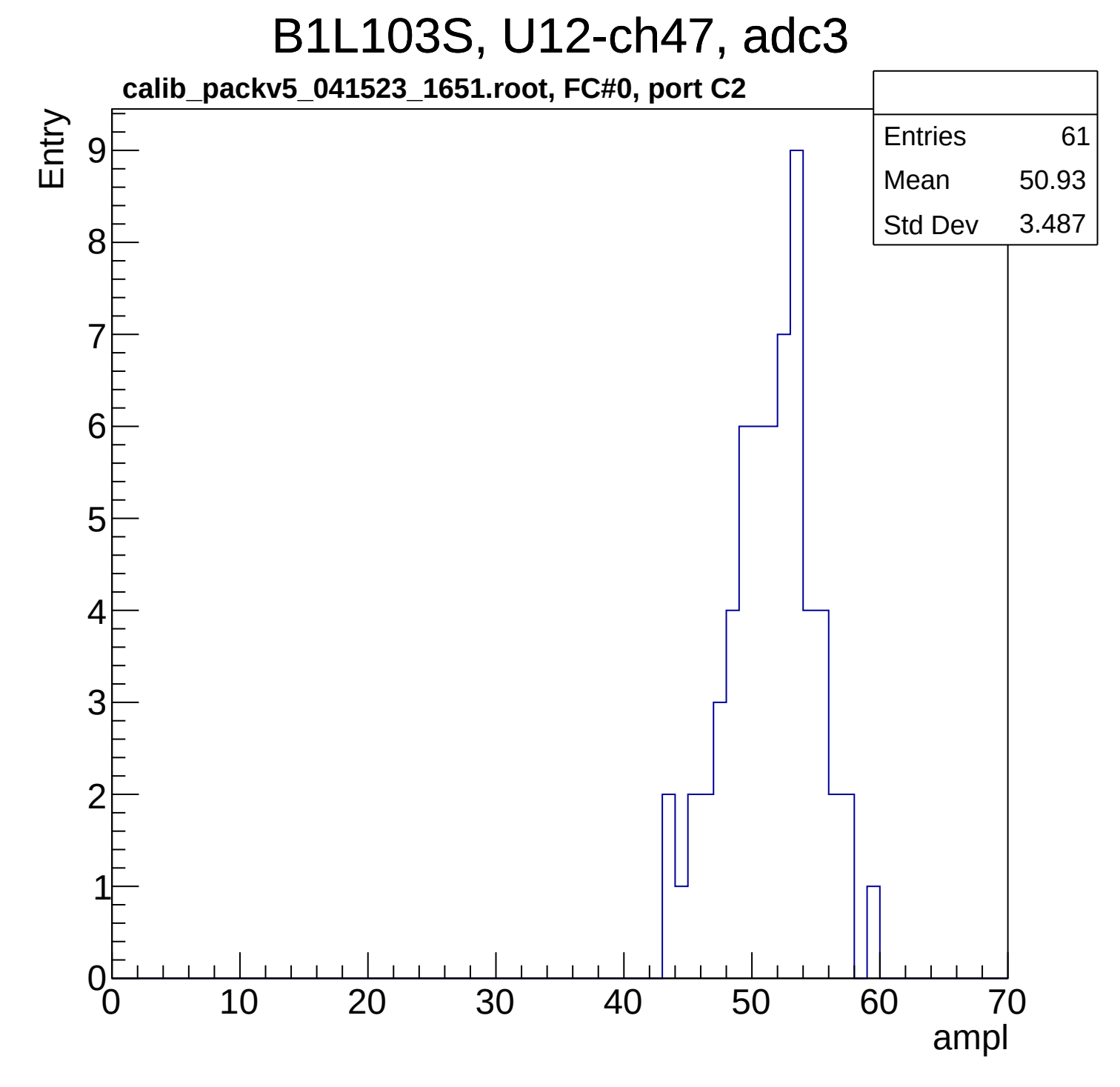
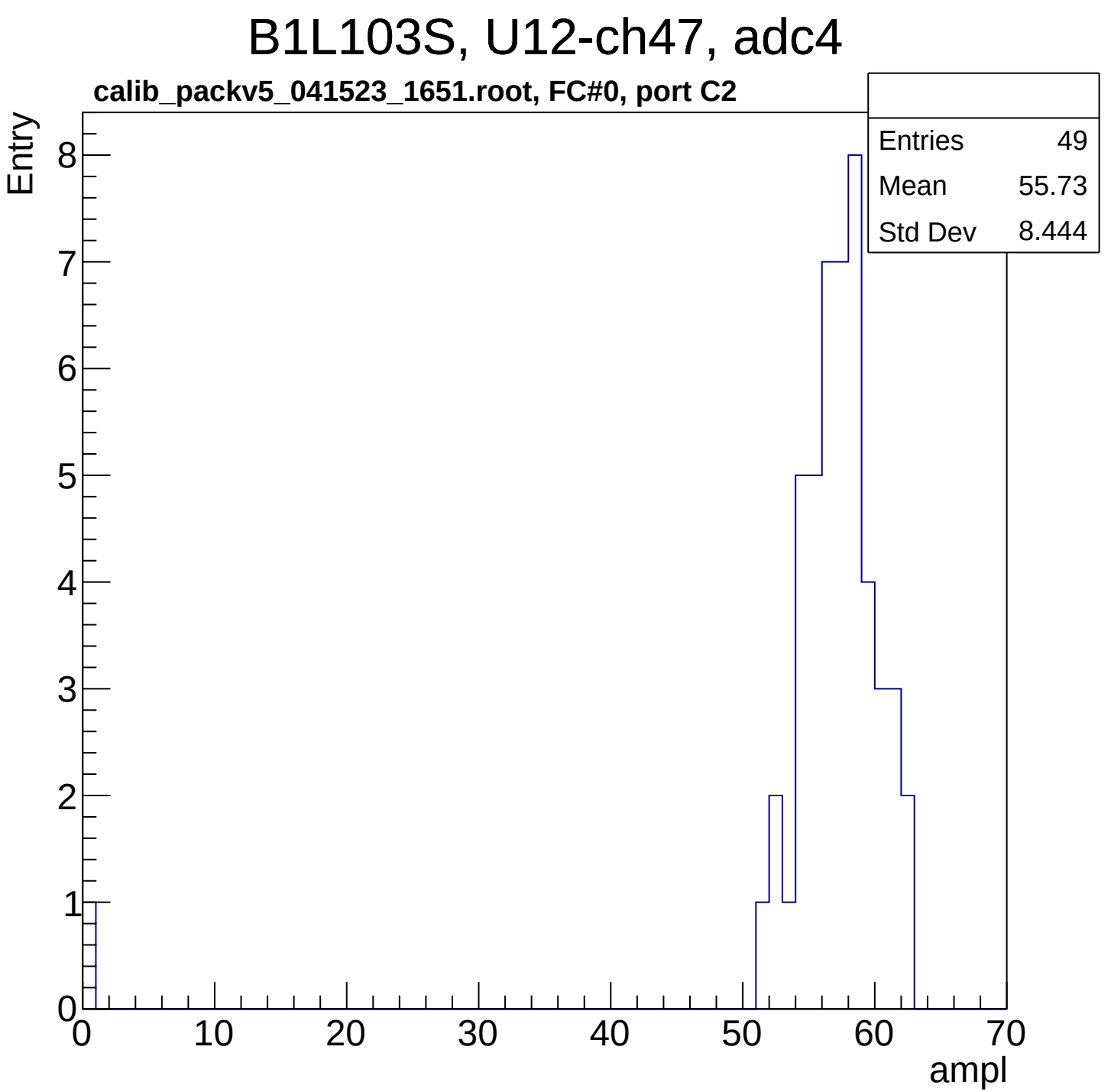

B1L103S, U12-ch47, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 50.93
Std Dev 3.487
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch47, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 55.73
Std Dev 8.444
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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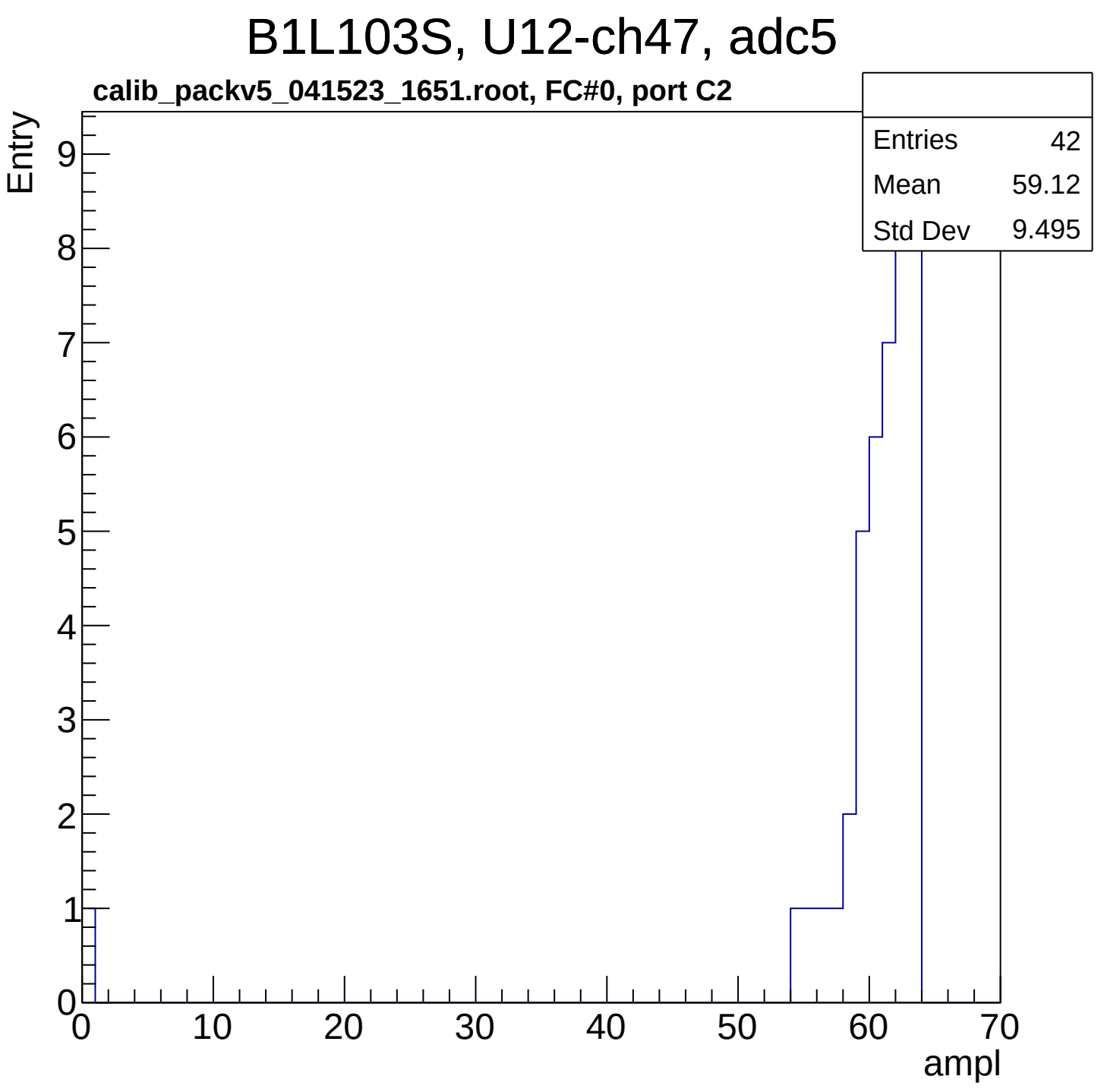
B1L103S, U12-ch47, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 59.12
Std Dev 9.495
Entry
ampl
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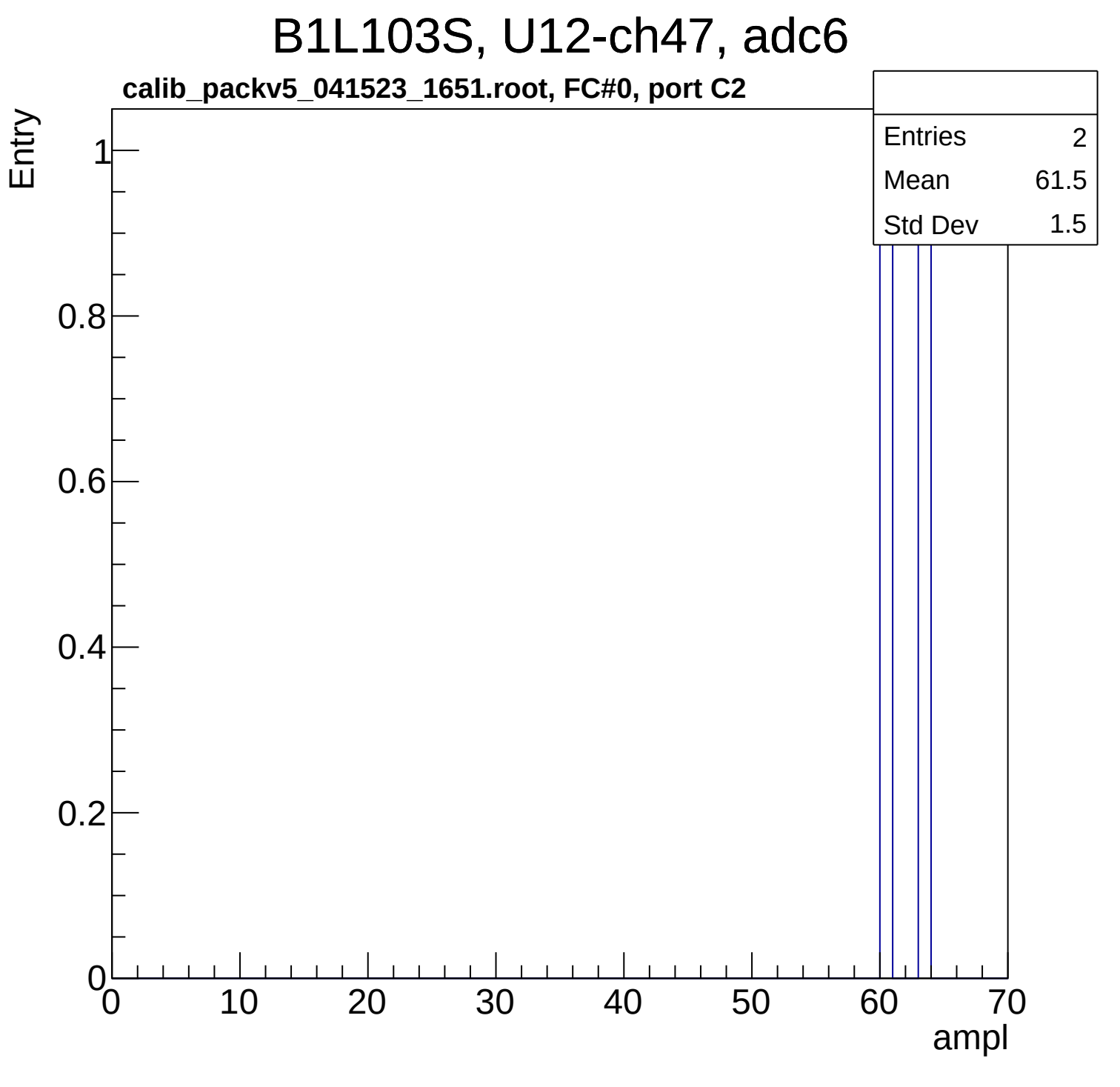
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U12-ch47, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 61.5
Std Dev 1.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
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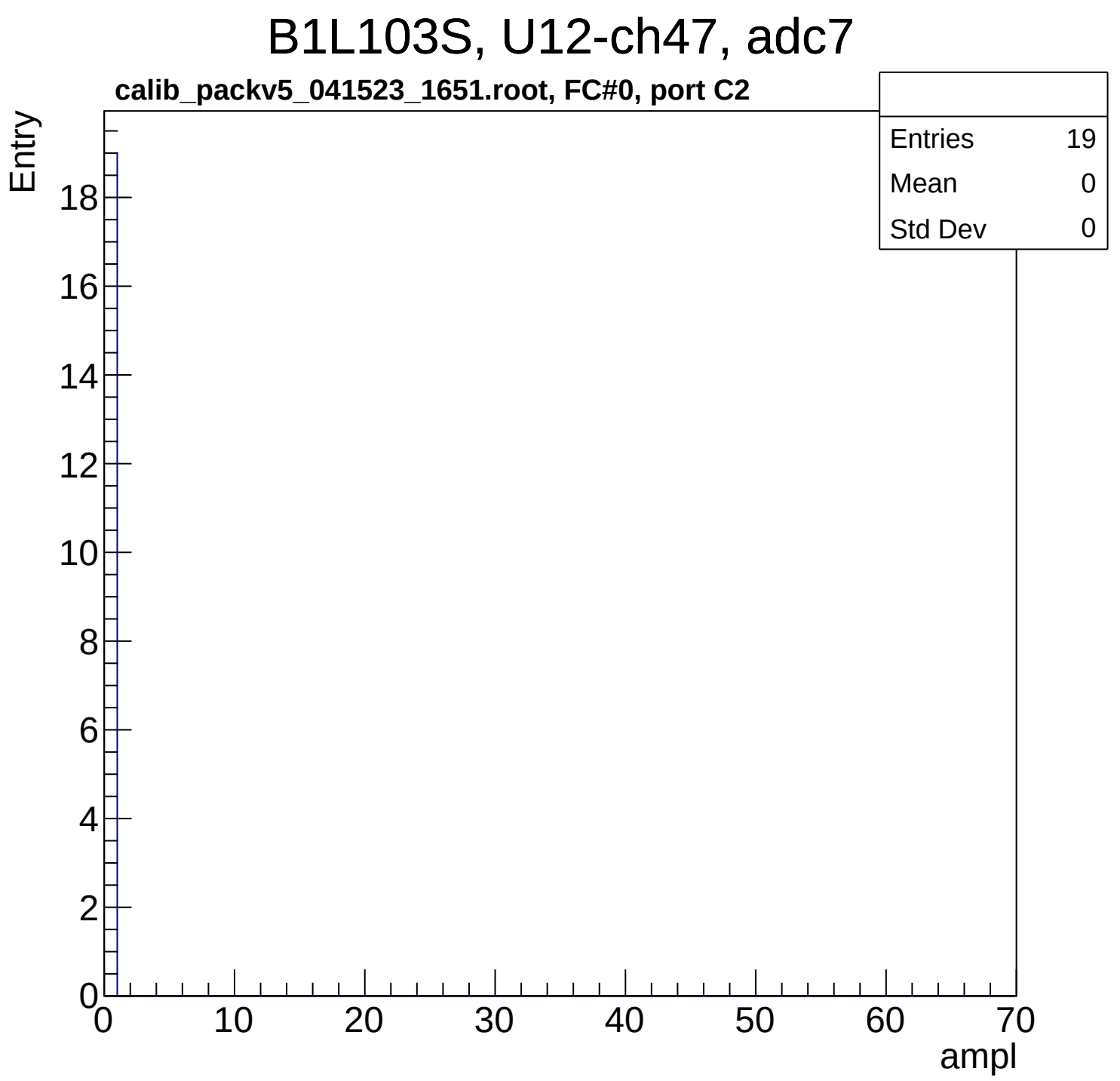
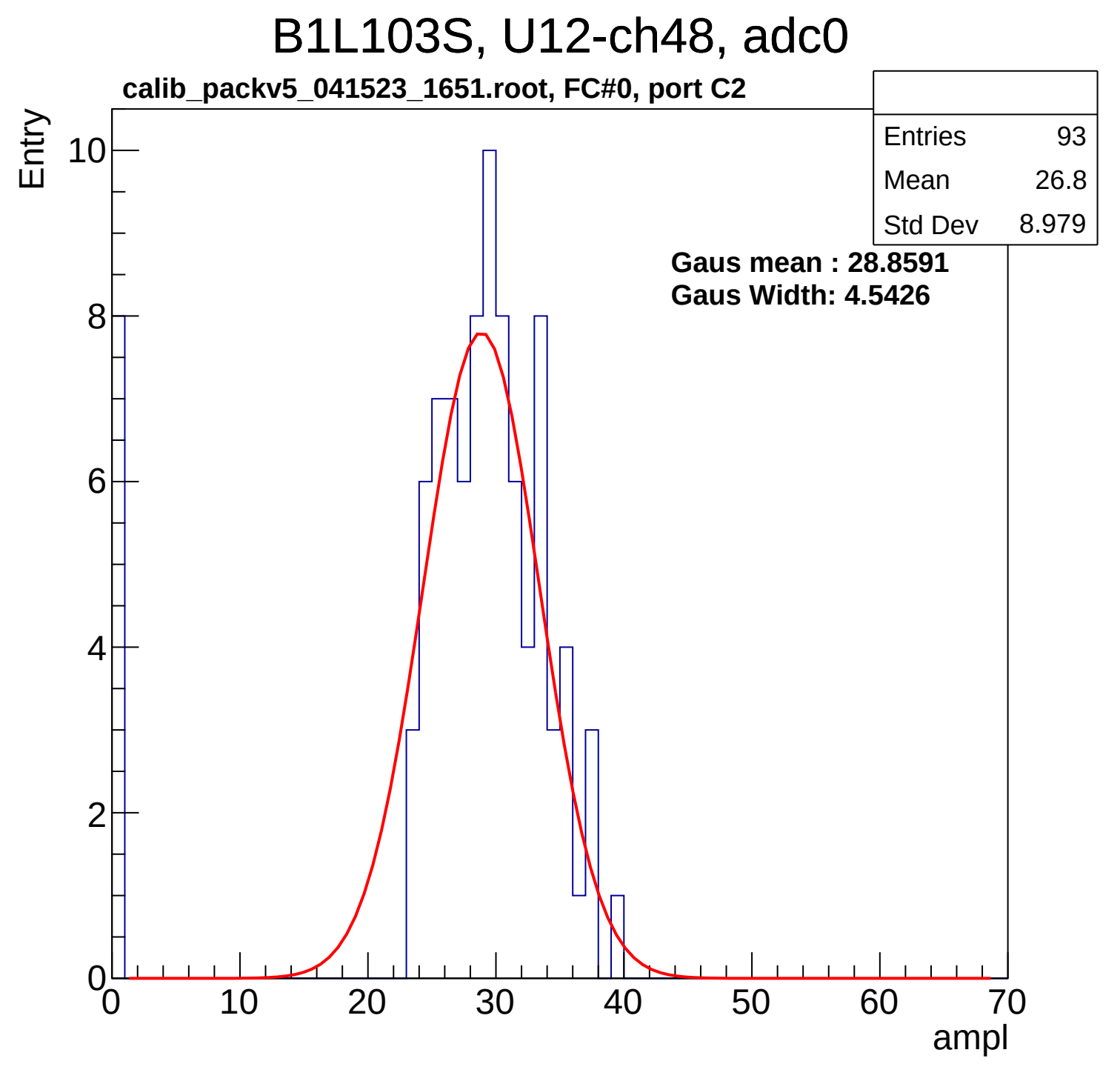
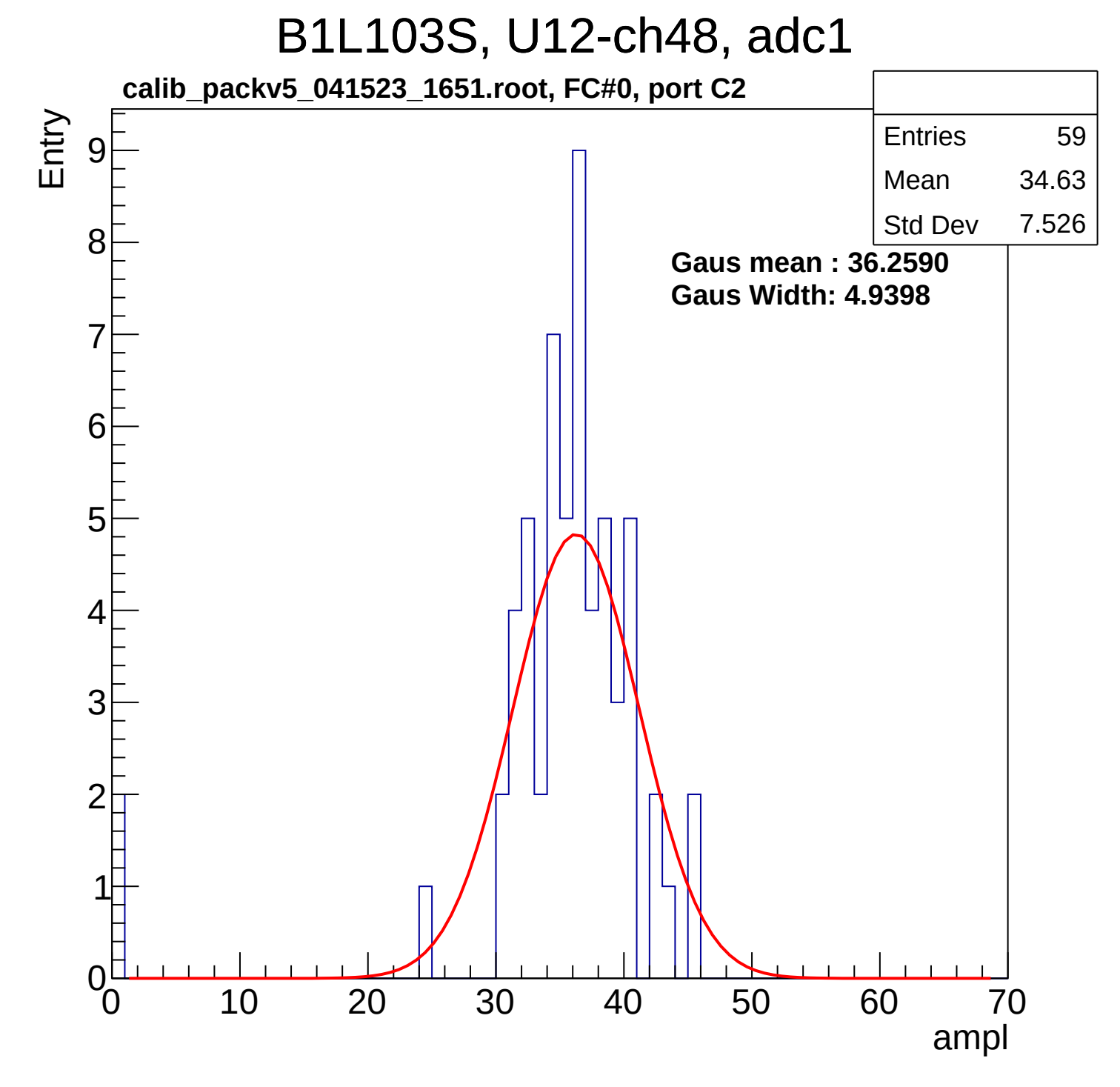

B1L103S, U12-ch47, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch48, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 26.8
Std Dev 8.979
Gaus mean : 28.8591
Gaus Width: 4.5426
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch48, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 34.63
Std Dev 7.526
Gaus mean : 36.2590
Gaus Width: 4.9398
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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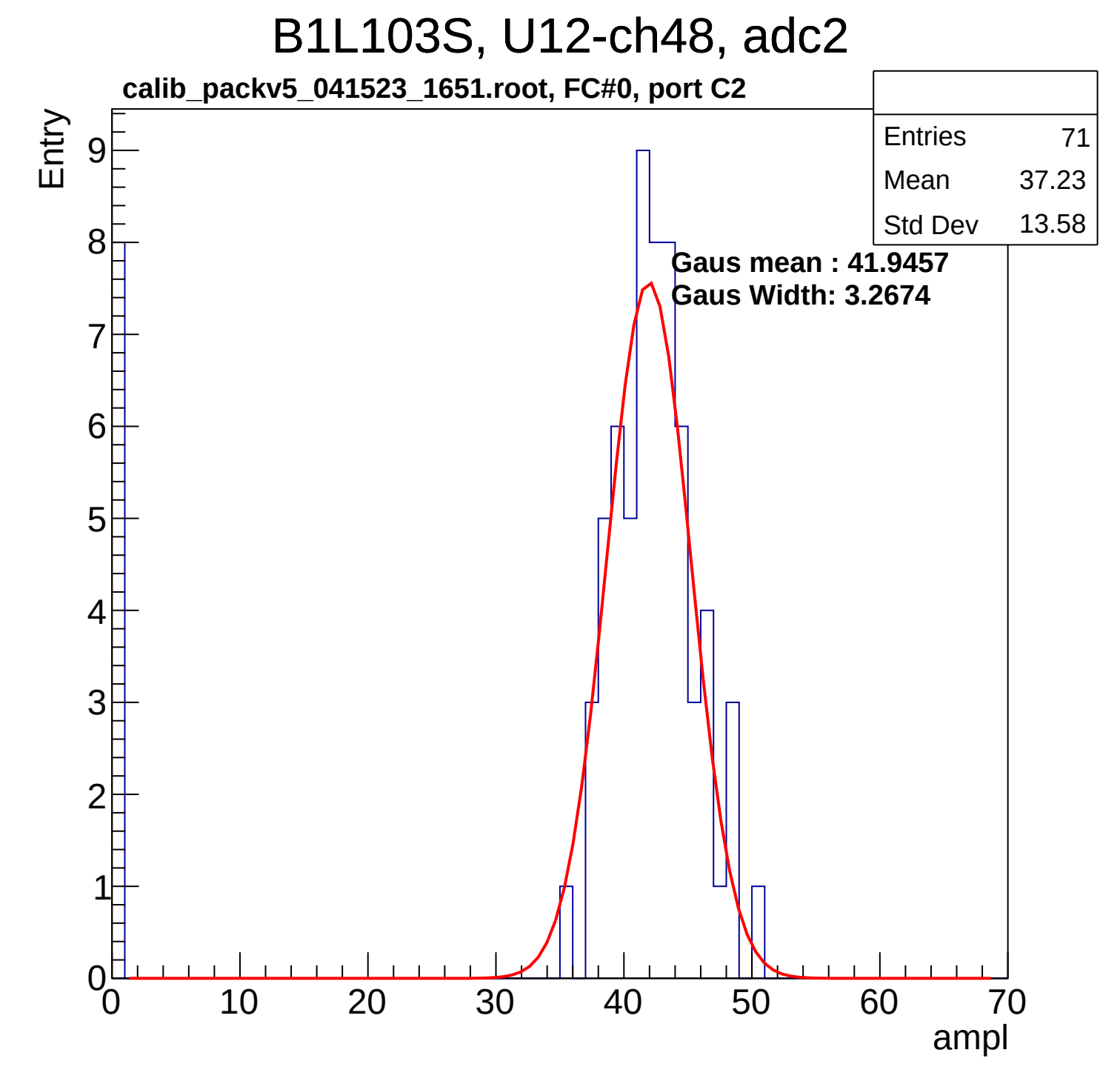
60
70


B1L103S, U12-ch48, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 37.23
Std Dev 13.58
Gaus mean : 41.9457
Gaus Width: 3.2674
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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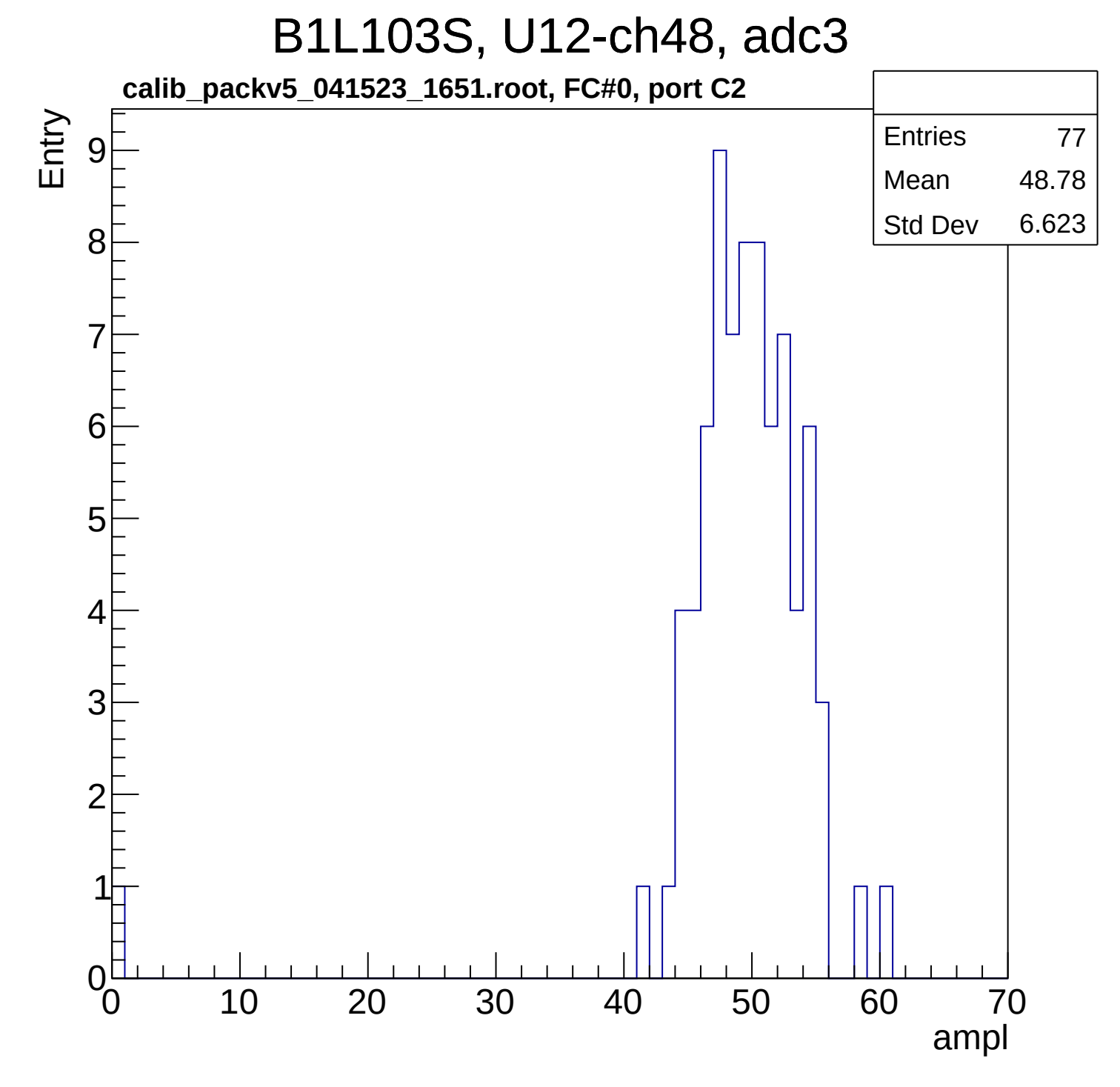
B1L103S, U12-ch48, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 48.78
Std Dev 6.623
Entry
ampl
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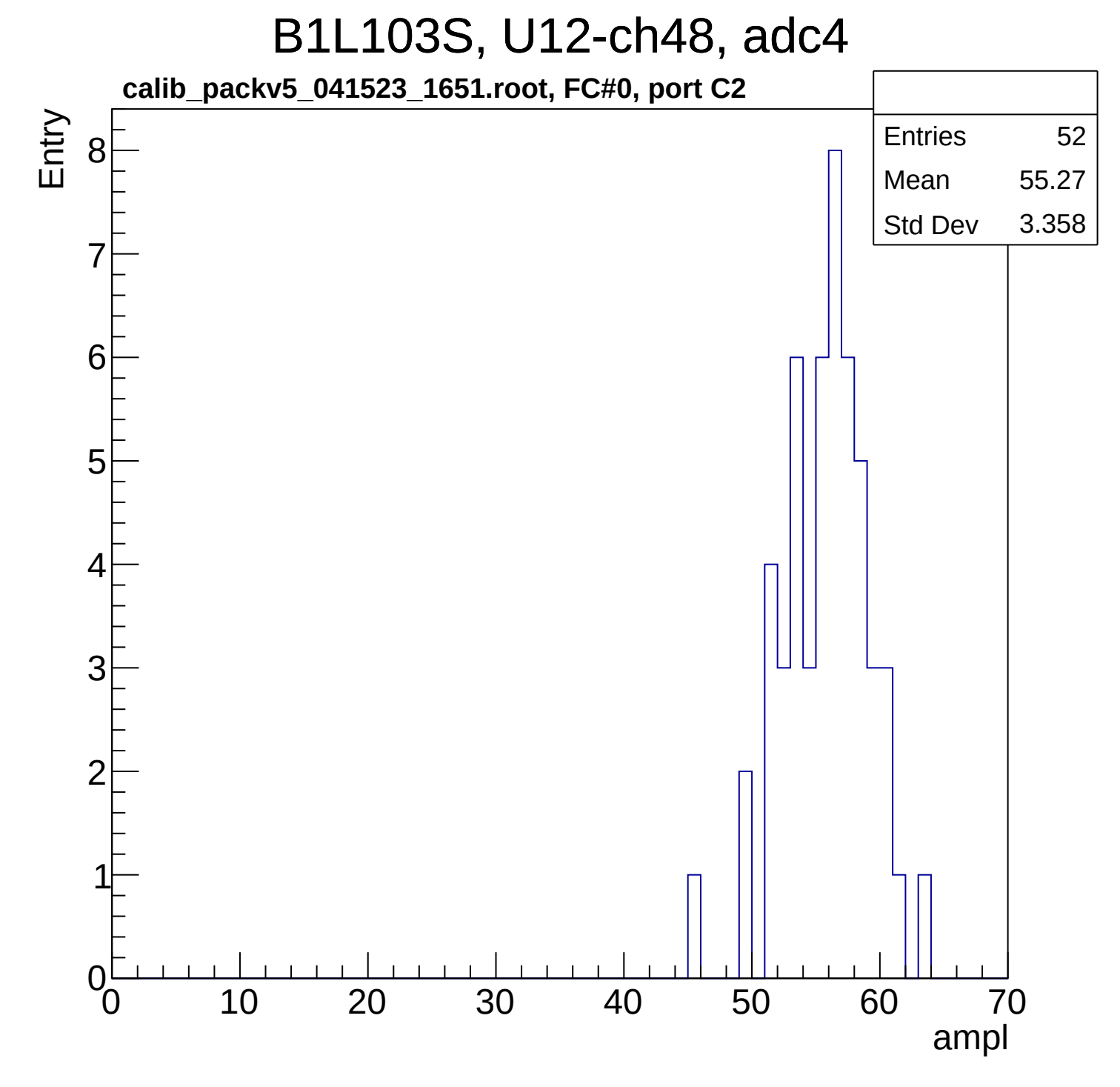
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U12-ch48, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 55.27
Std Dev 3.358
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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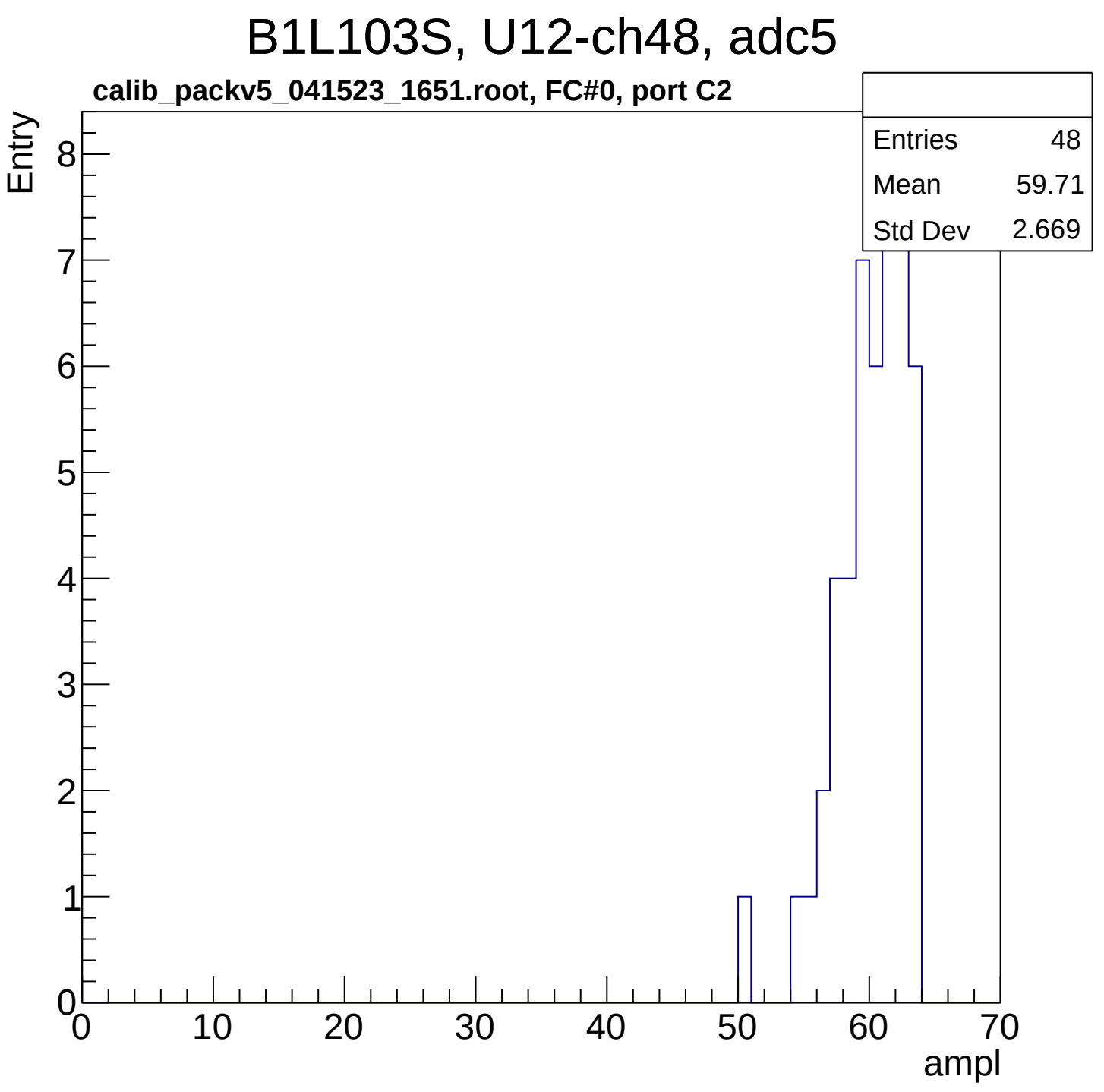
40
50
60
70


B1L103S, U12-ch48, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 59.71
Std Dev 2.669
Entry
ampl
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2
3
4
5
6
7
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0
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20
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40
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60
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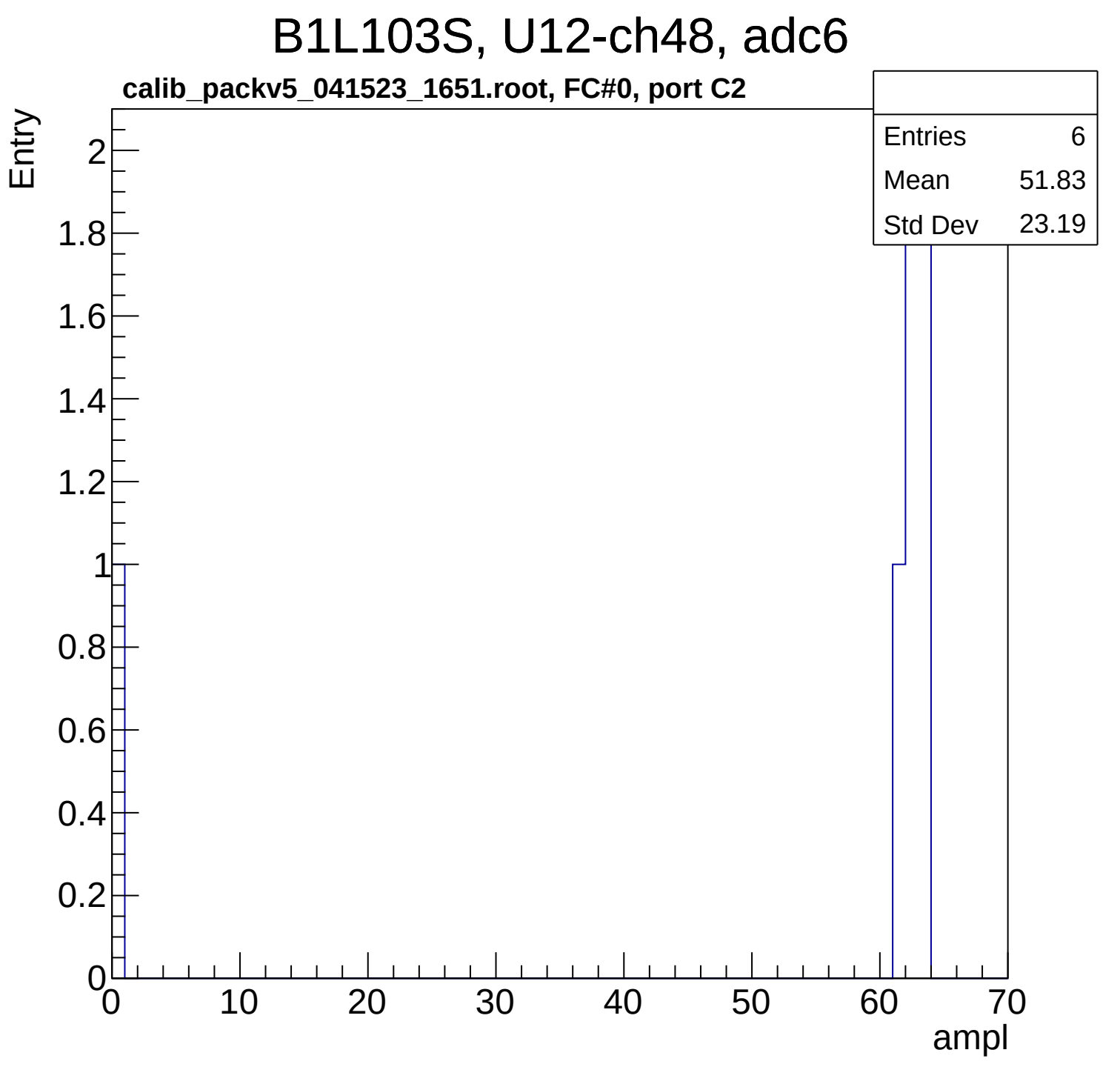
B1L103S, U12-ch48, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 51.83
Std Dev 23.19
Entry
ampl
0
0.2
0.4
0.6
0.8
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1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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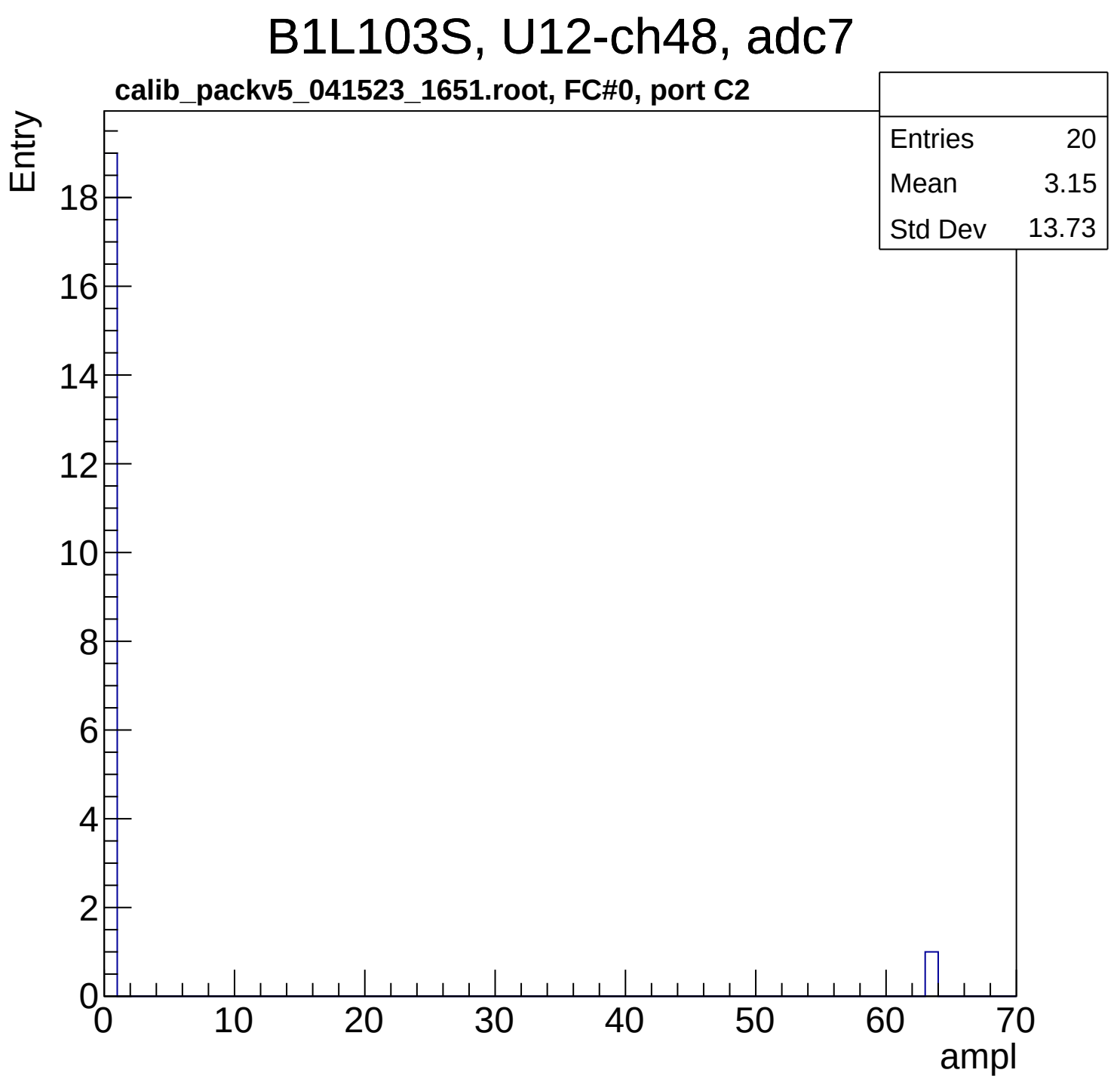
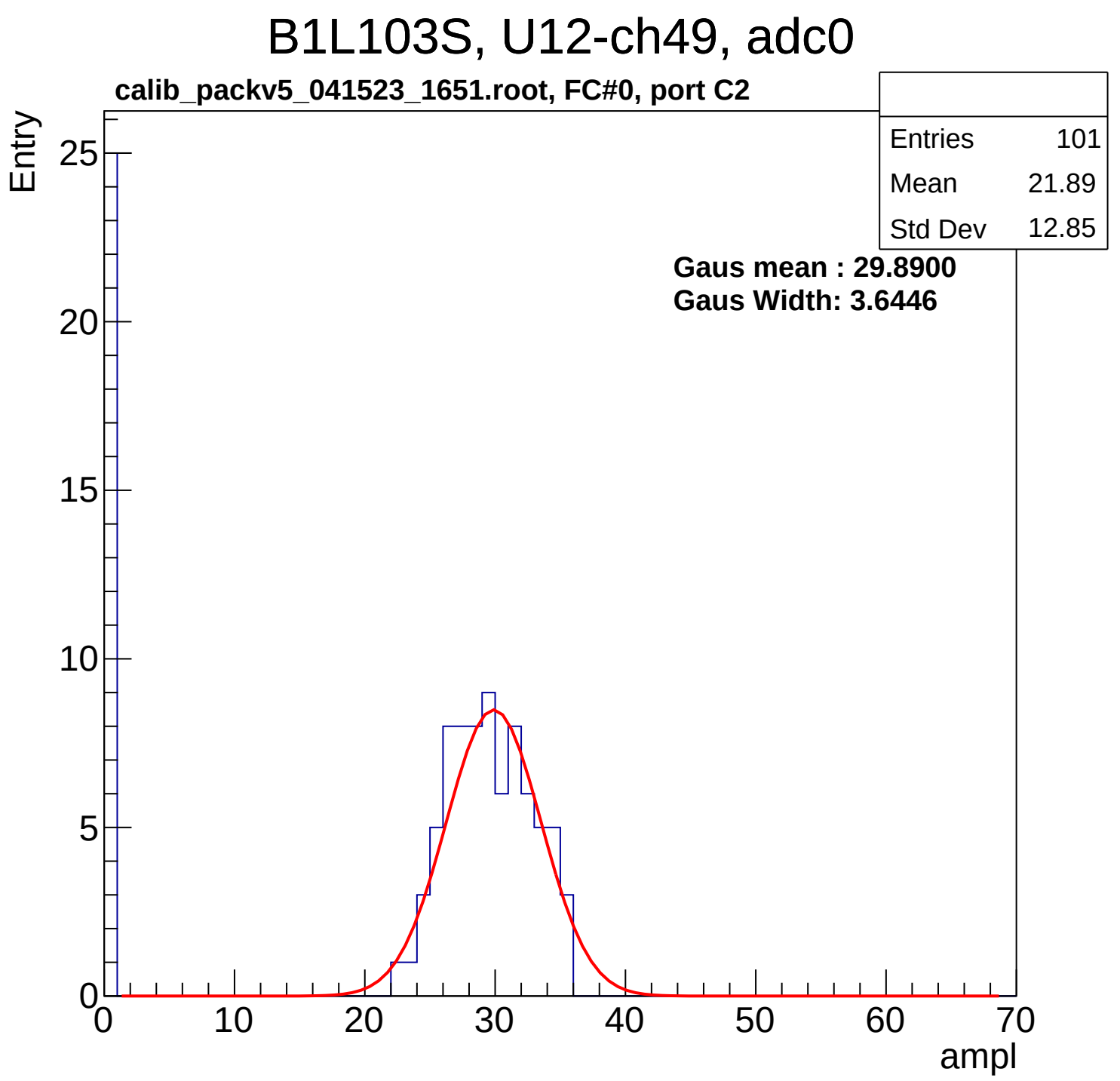
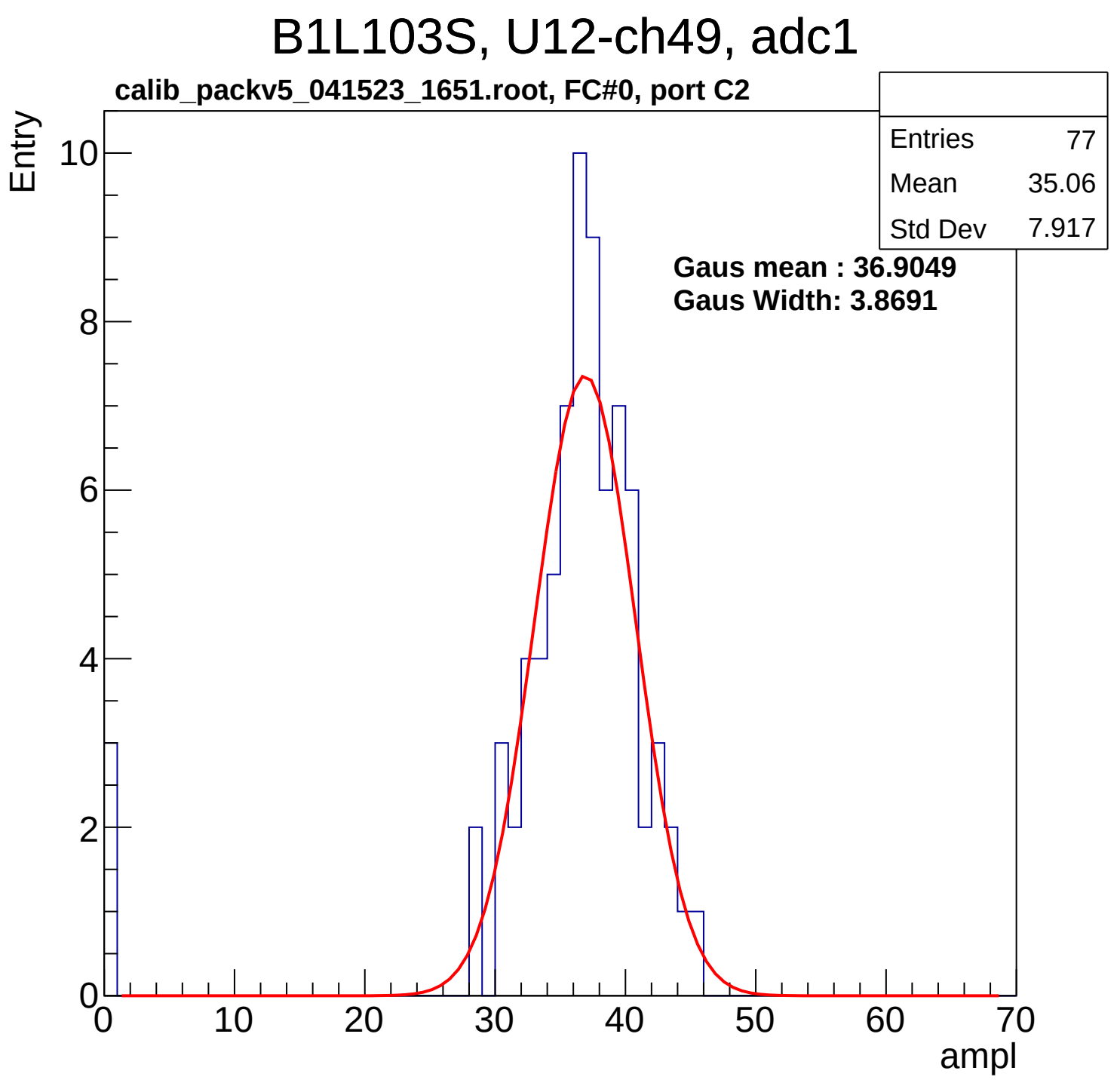

B1L103S, U12-ch48, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch49, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 21.89
Std Dev 12.85
Gaus mean : 29.8900
Gaus Width: 3.6446
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U12-ch49, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 35.06
Std Dev 7.917
Gaus mean : 36.9049
Gaus Width: 3.8691
Entry
ampl
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2
4
6
8
10
0
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20
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40
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60
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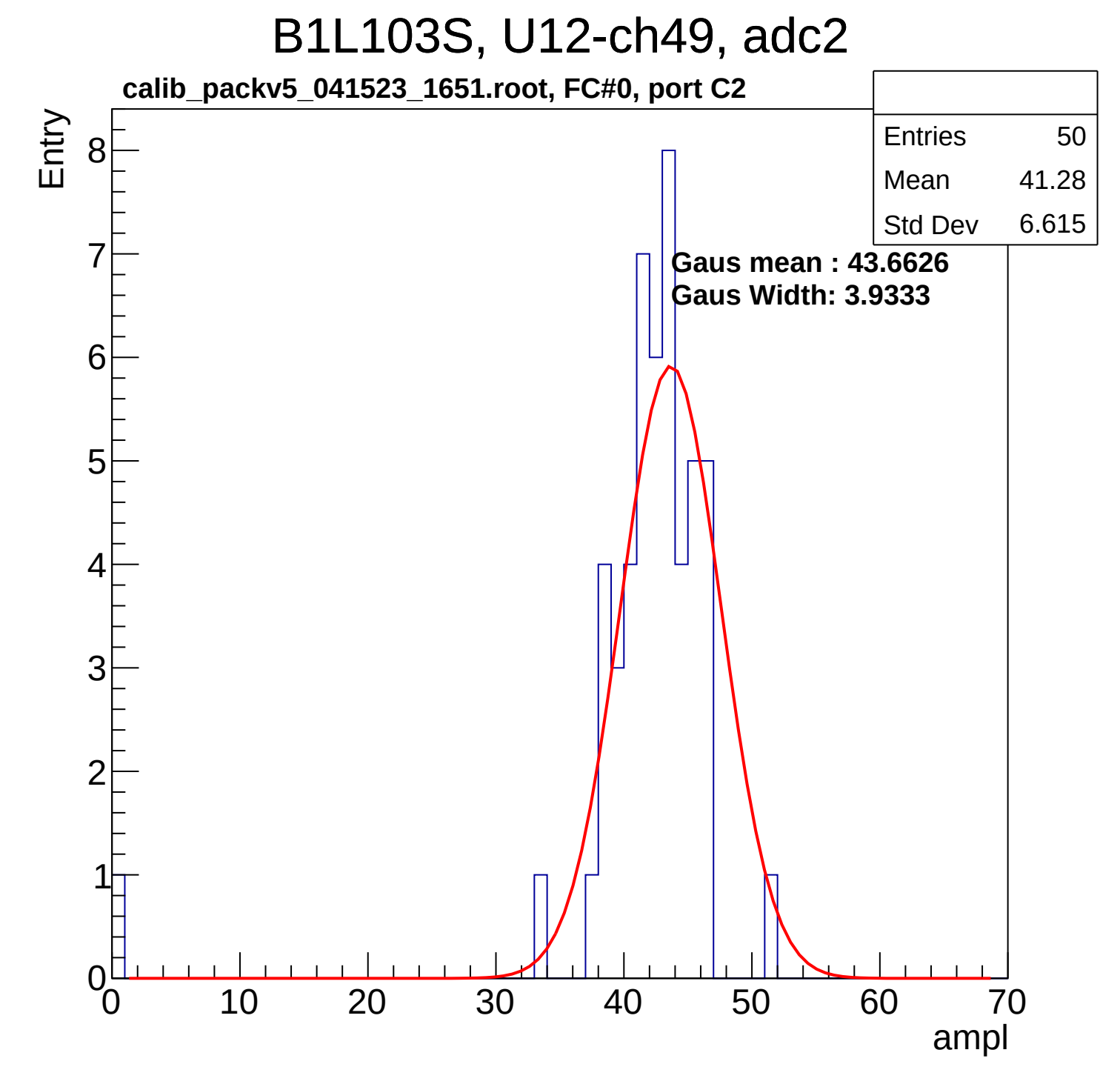
B1L103S, U12-ch49, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 41.28
Std Dev 6.615
Gaus mean : 43.6626
Gaus Width: 3.9333
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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40
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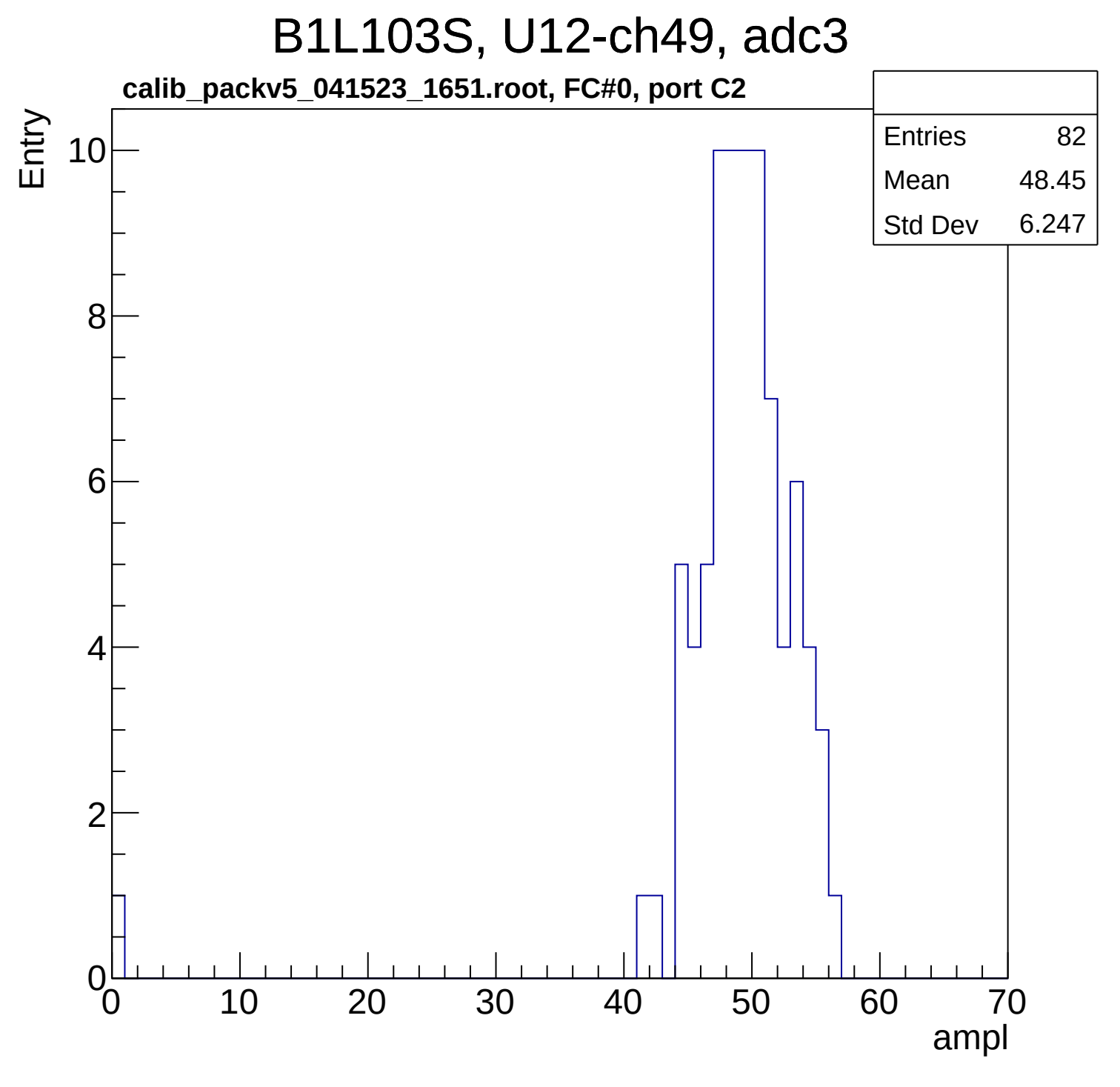
B1L103S, U12-ch49, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 48.45
Std Dev 6.247
Entry
ampl
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4
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0
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60
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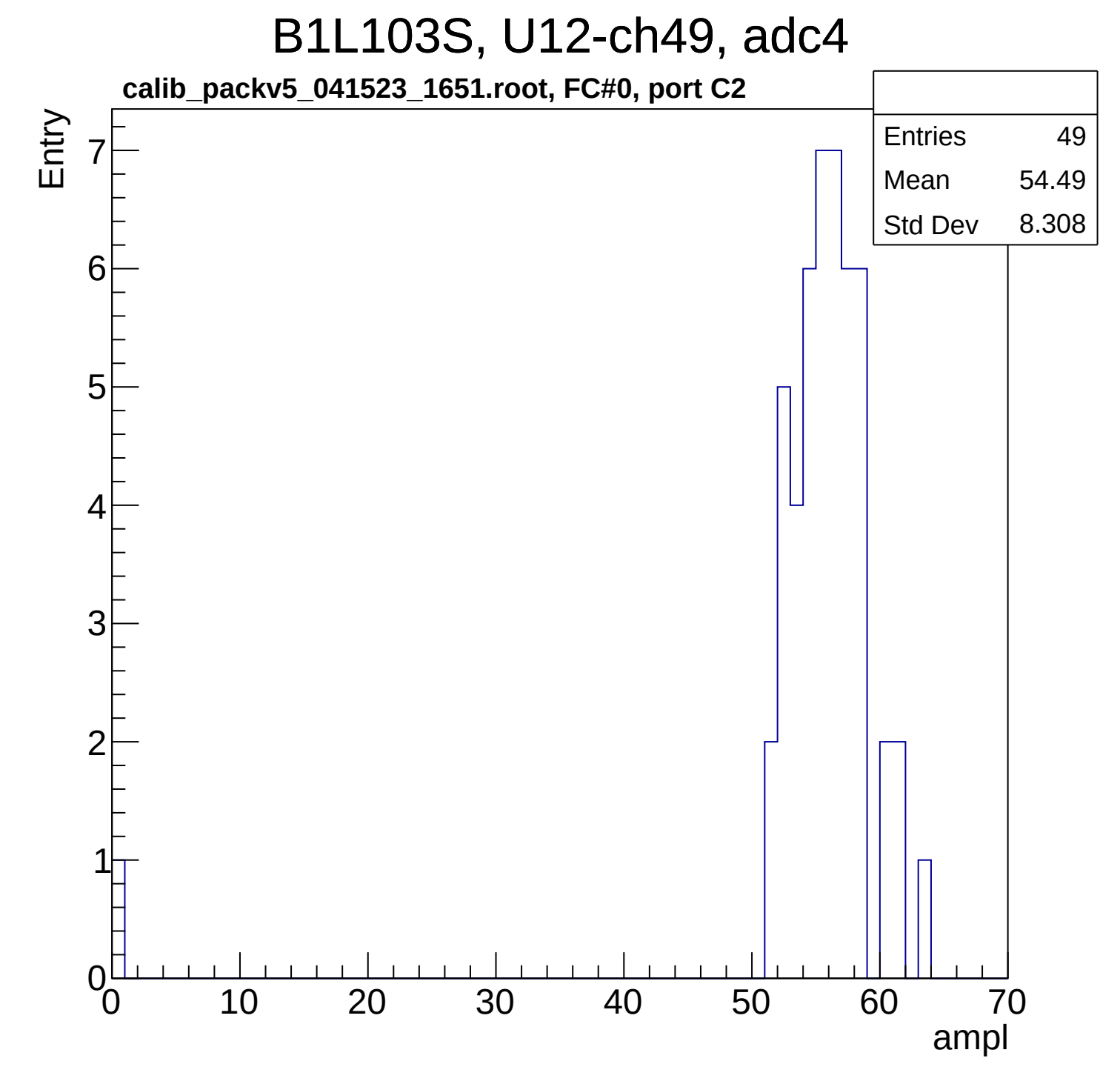
B1L103S, U12-ch49, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 54.49
Std Dev 8.308
Entry
ampl
0
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2
3
4
5
6
7
0
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20
30
40
50
60
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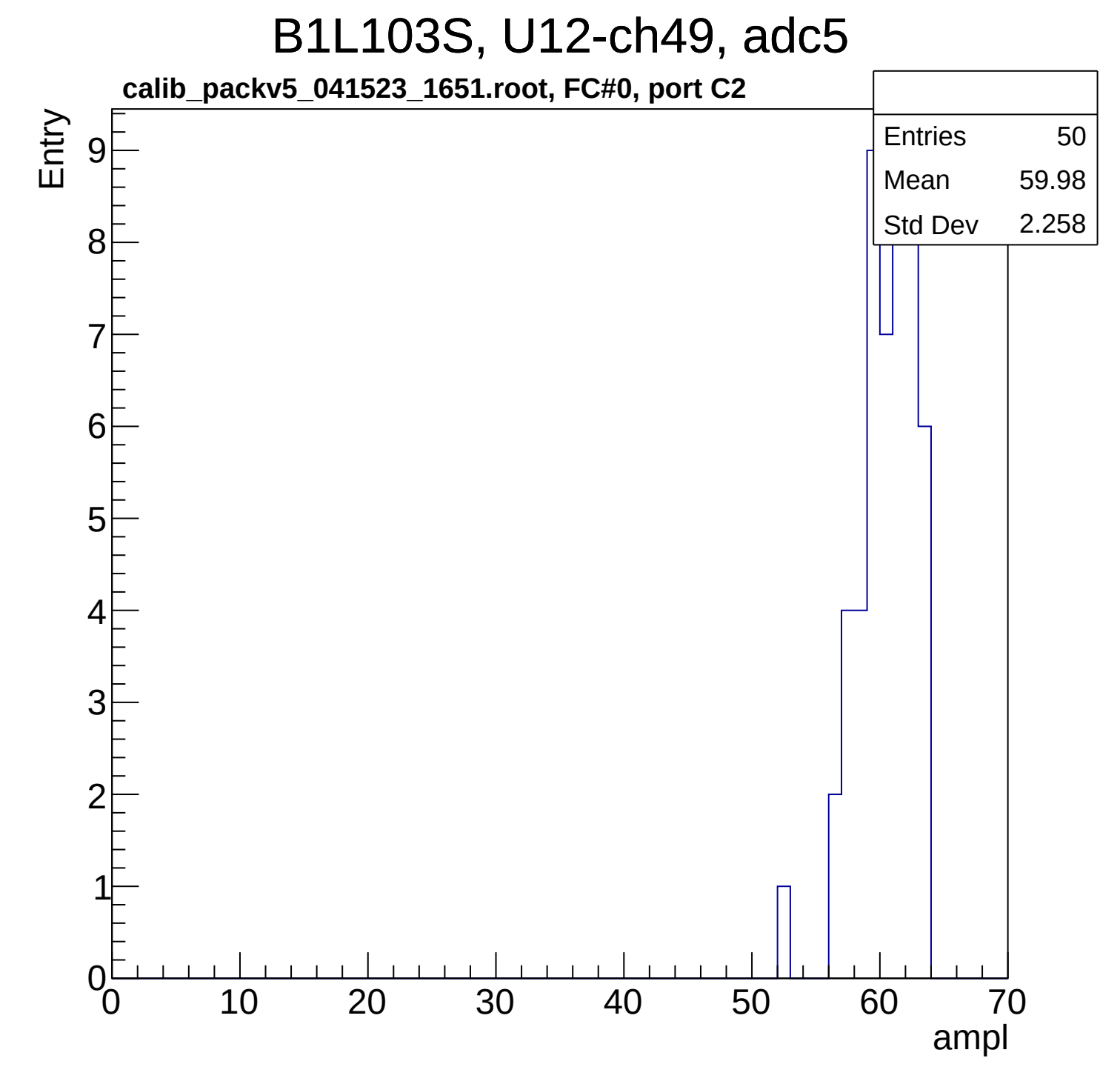
B1L103S, U12-ch49, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 59.98
Std Dev 2.258
Entry
ampl
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2
3
4
5
6
7
8
9
0
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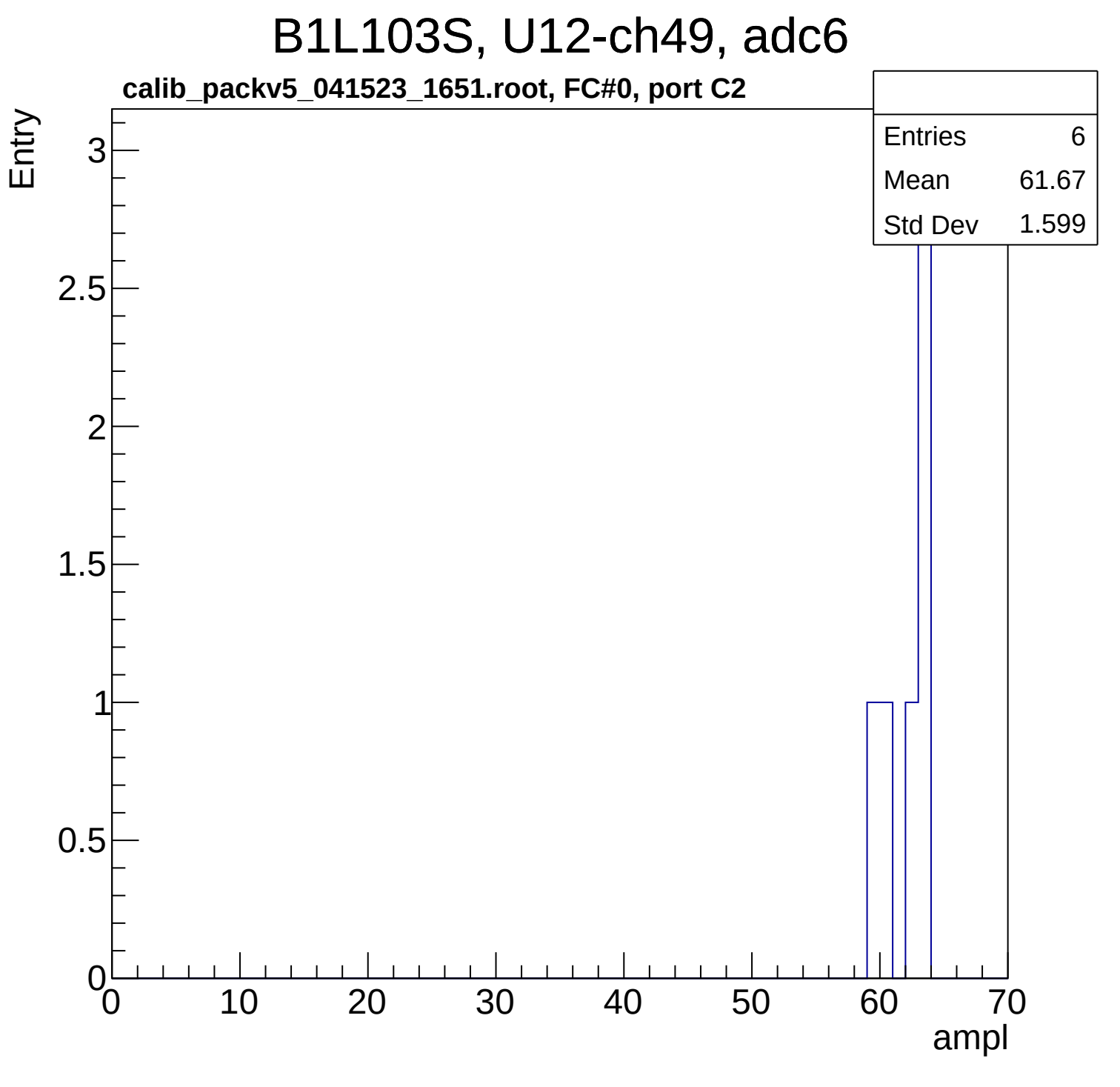
B1L103S, U12-ch49, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.67
Std Dev 1.599
Entry
ampl
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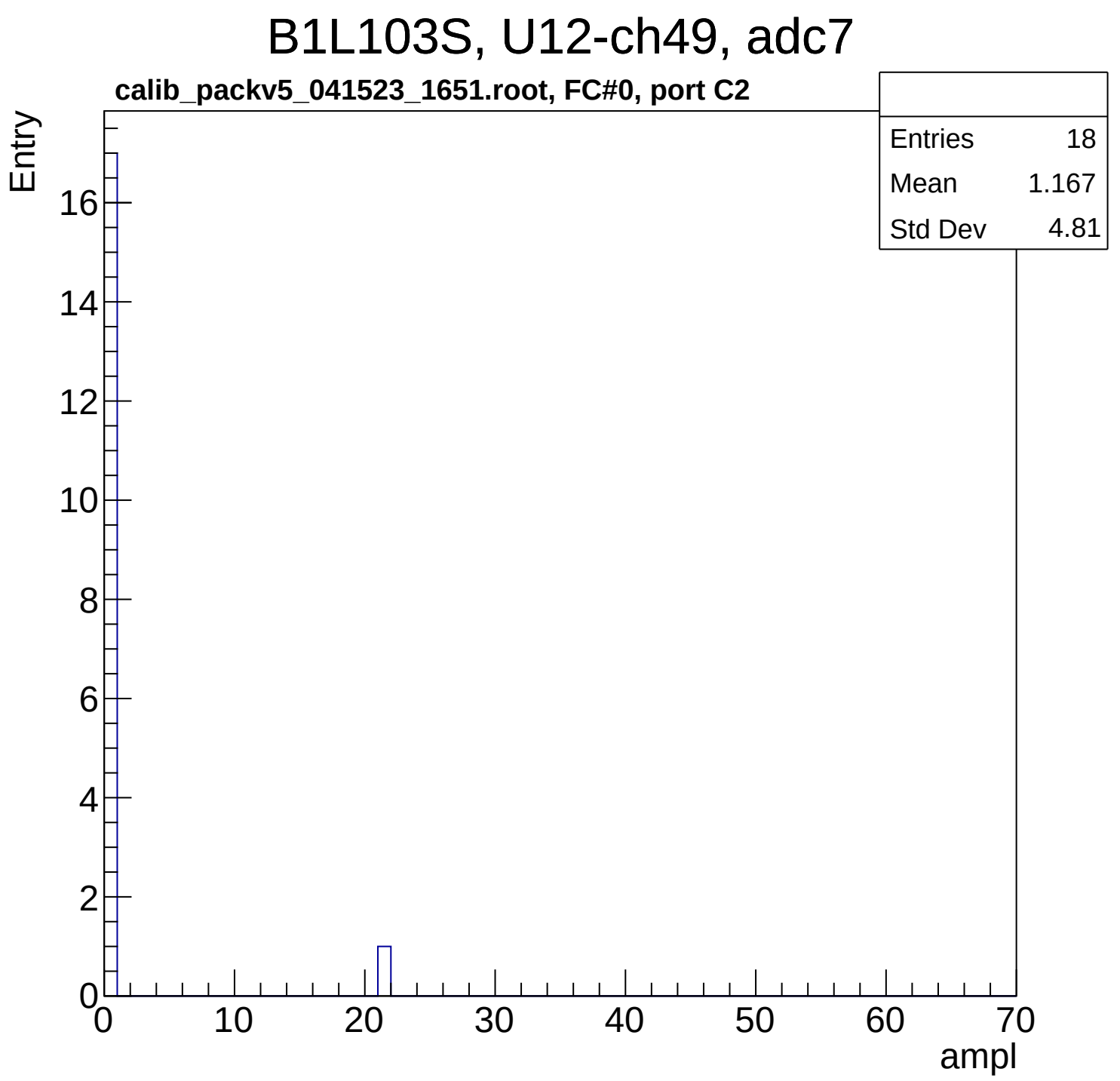
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U12-ch49, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.167
Std Dev 4.81
Entry
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4
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8
10
12
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16
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10
20
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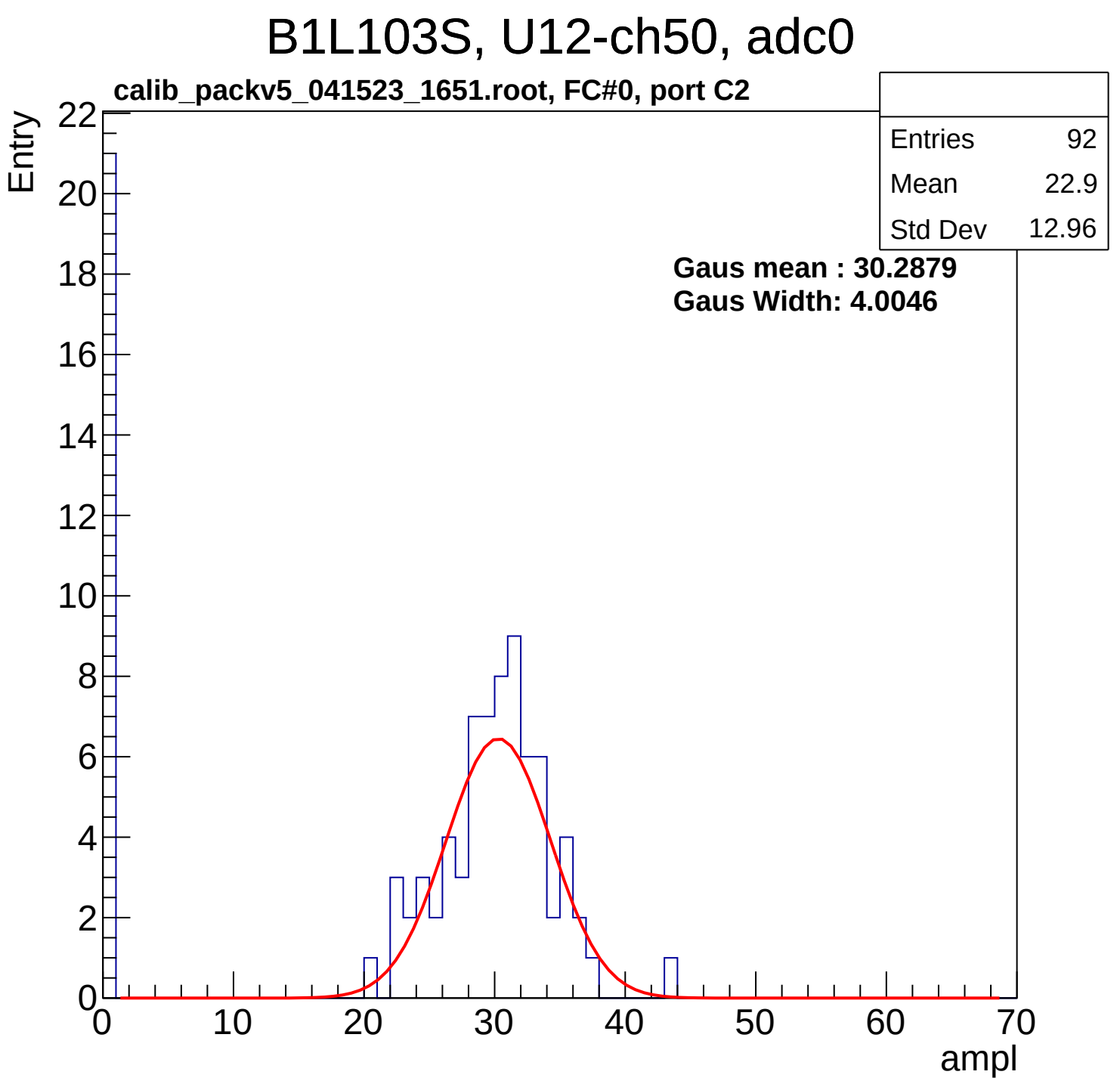
50
60
70
ampl


B1L103S, U12-ch50, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 22.9
Std Dev 12.96
Gaus mean : 30.2879
Gaus Width: 4.0046
Entry
ampl
0
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8
10
12
14
16
18
20
22
0
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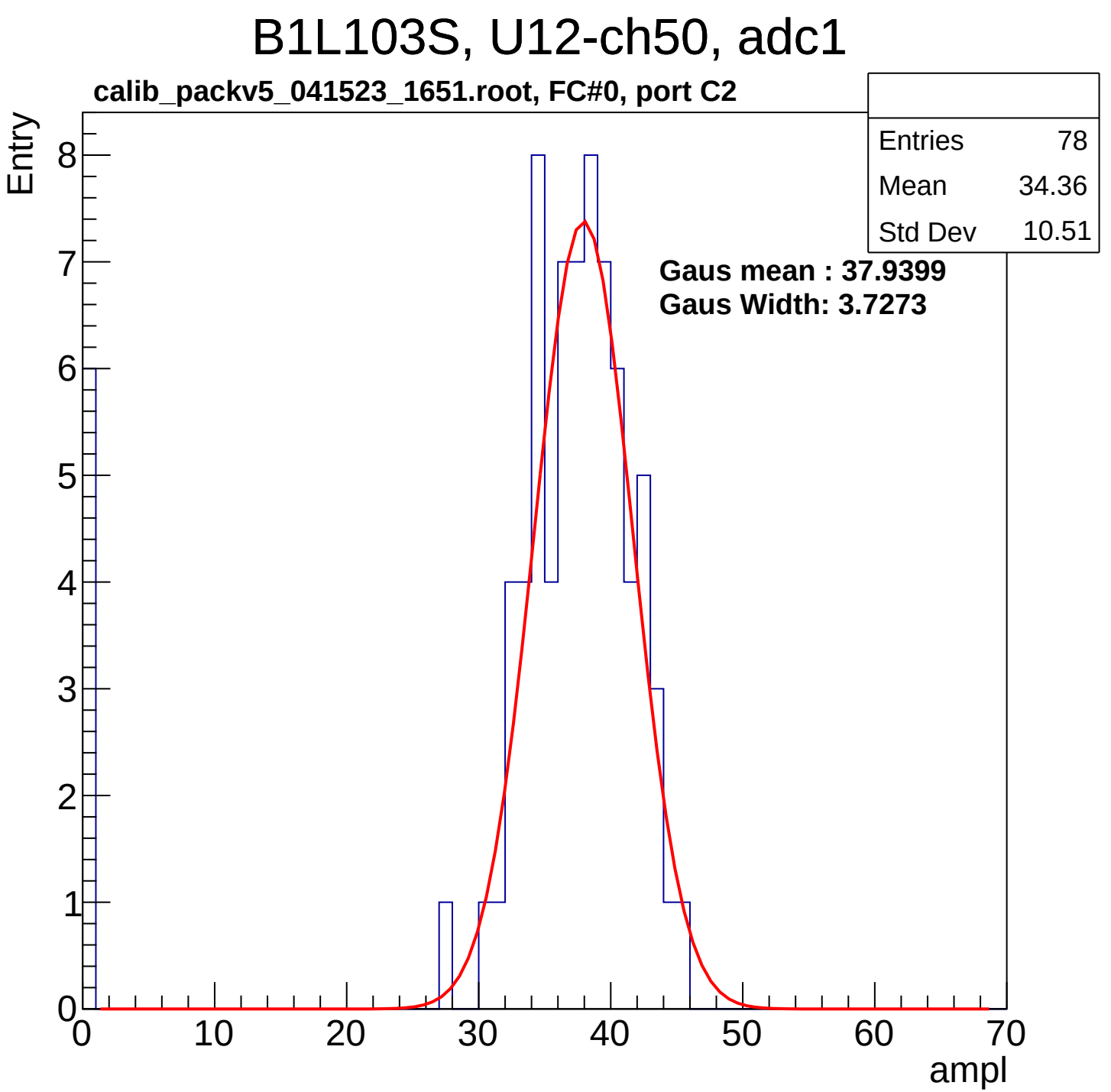
B1L103S, U12-ch50, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 34.36
Std Dev 10.51
Gaus mean : 37.9399
Gaus Width: 3.7273
Entry
ampl
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1
2
3
4
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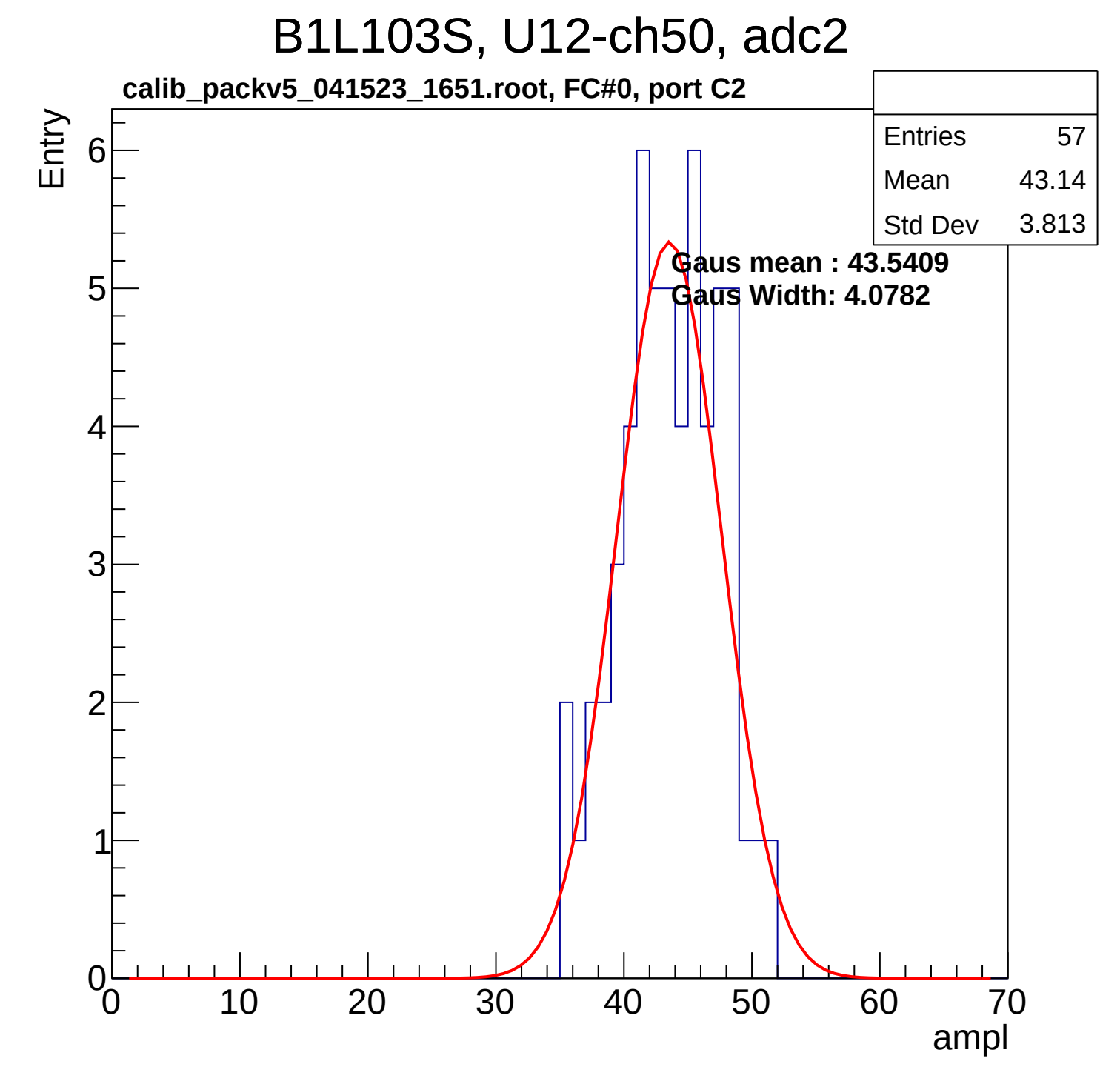
B1L103S, U12-ch50, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 43.14
Std Dev 3.813
Gaus mean : 43.5409
Gaus Width: 4.0782
Entry
ampl
0
1
2
3
4
5
6
0
10
20
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40
50
60
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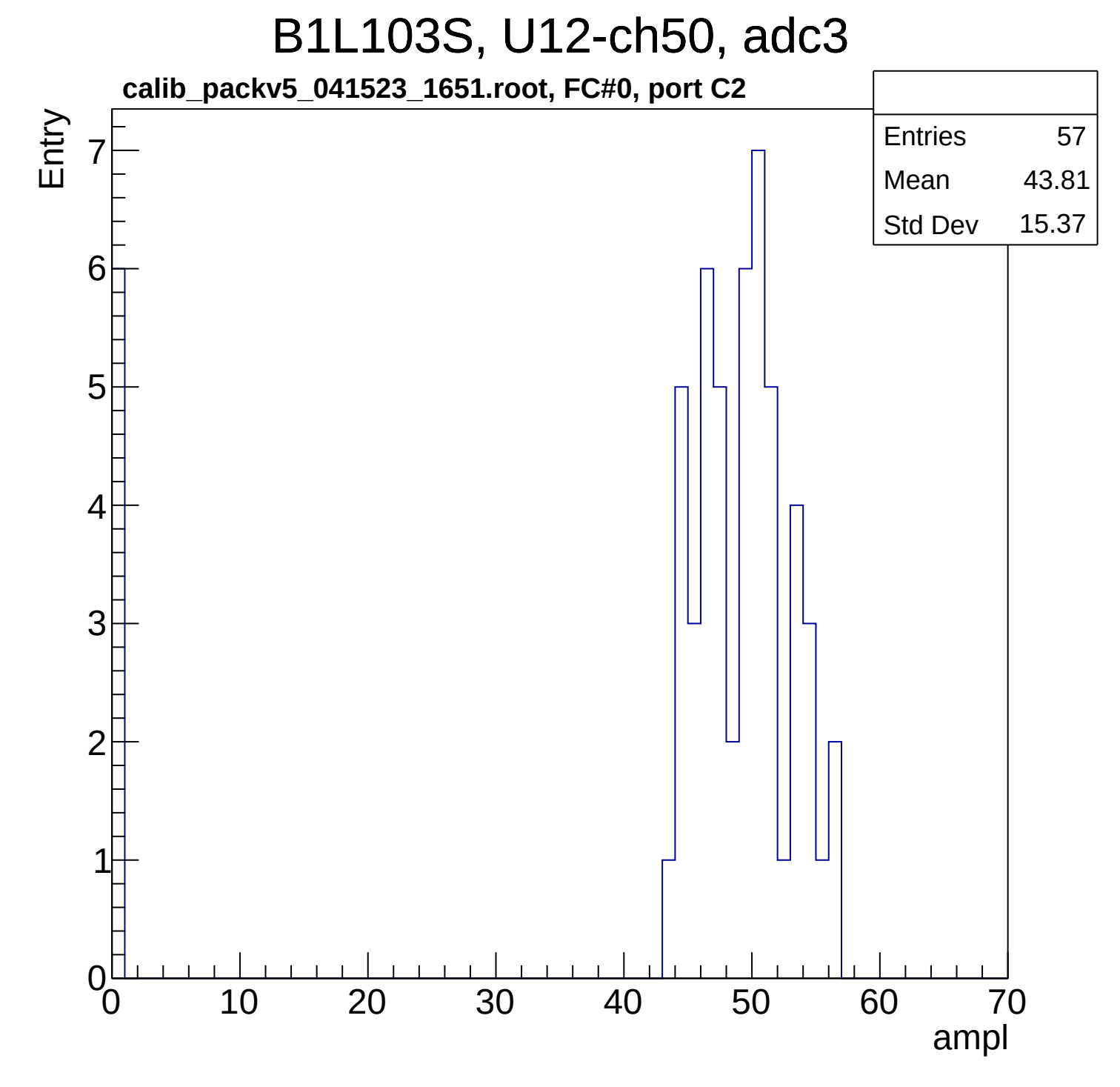
B1L103S, U12-ch50, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 43.81
Std Dev 15.37
Entry
ampl
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4
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0
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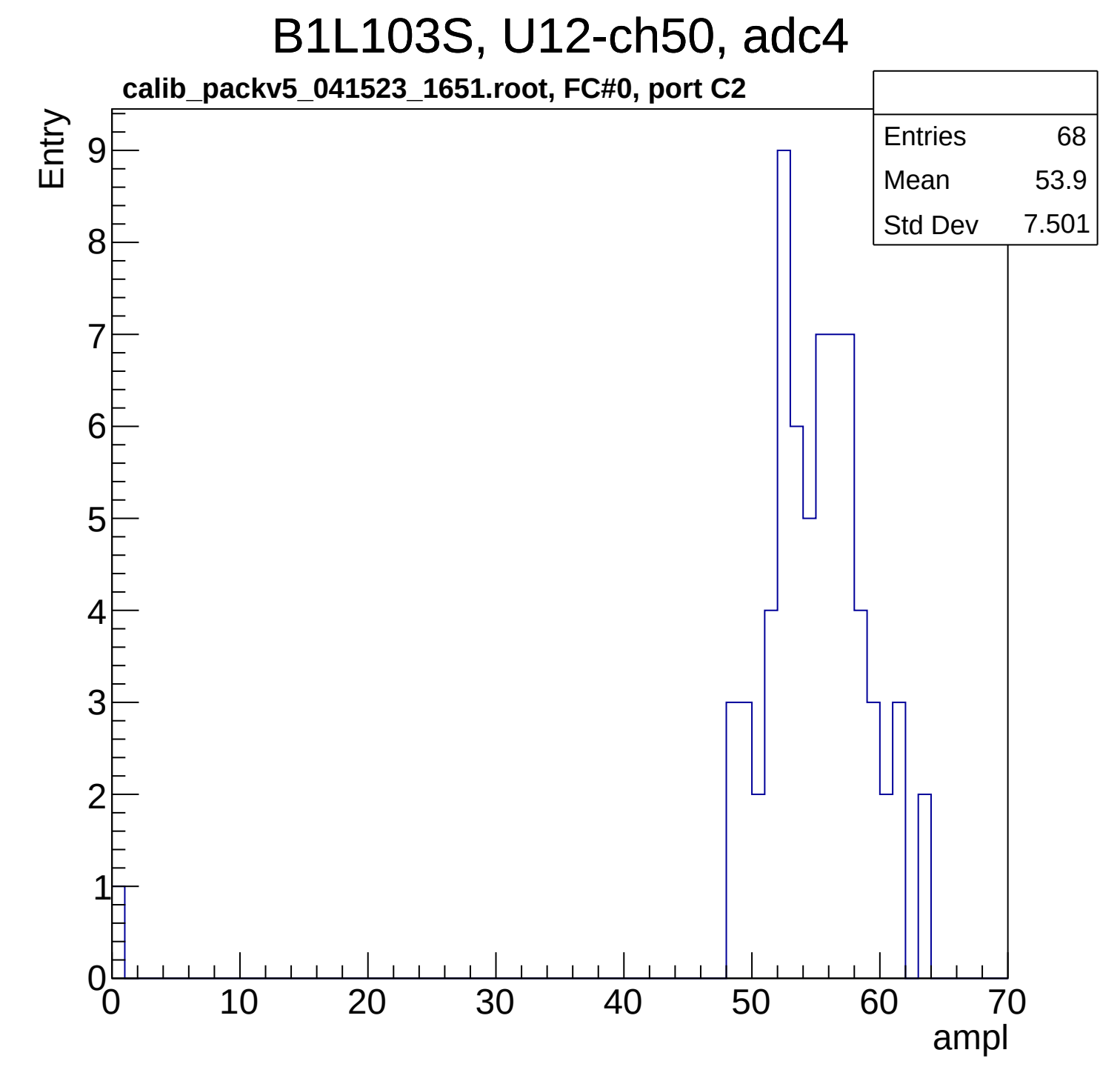
B1L103S, U12-ch50, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 53.9
Std Dev 7.501
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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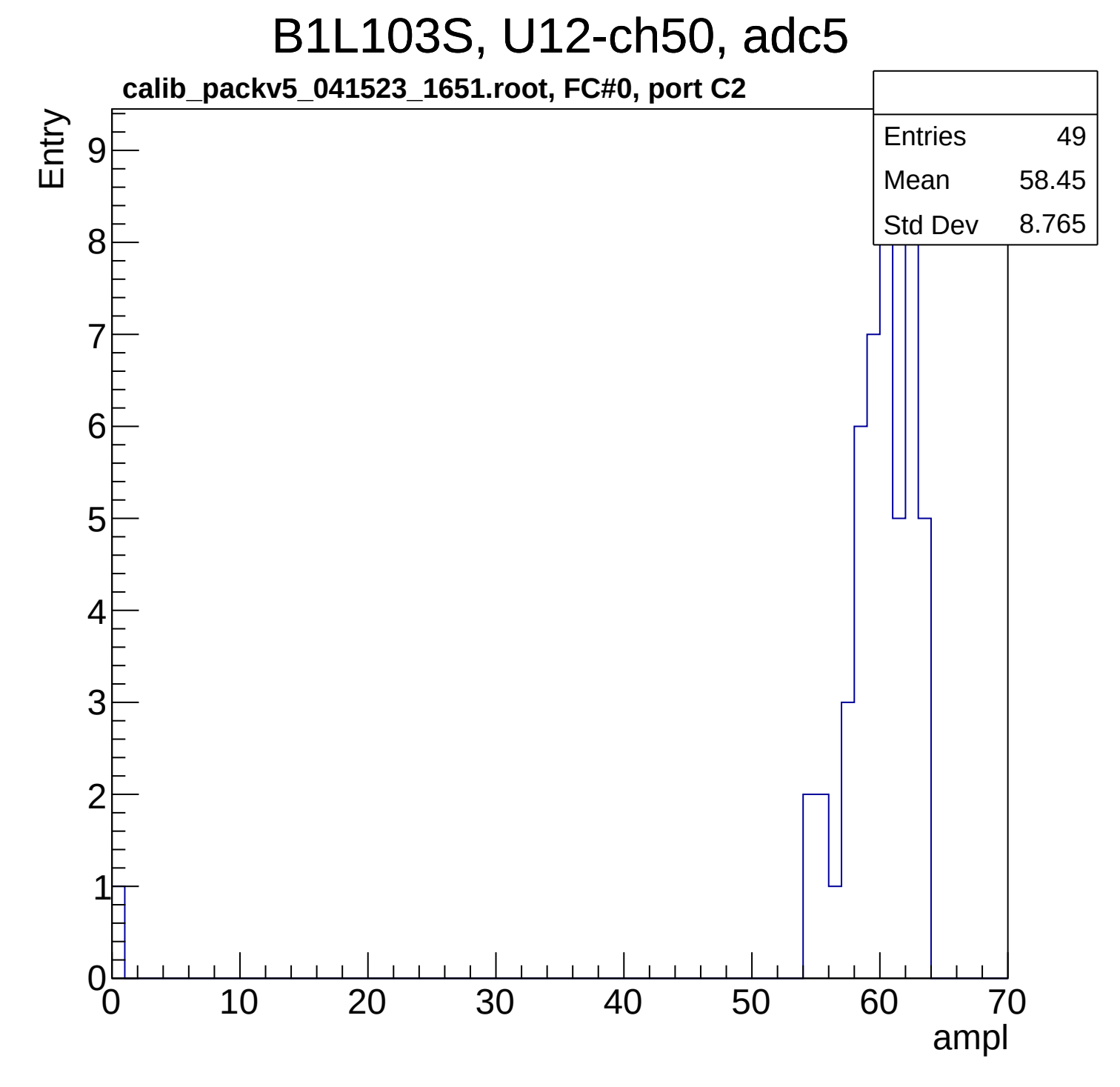
B1L103S, U12-ch50, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 58.45
Std Dev 8.765
Entry
ampl
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3
4
5
6
7
8
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0
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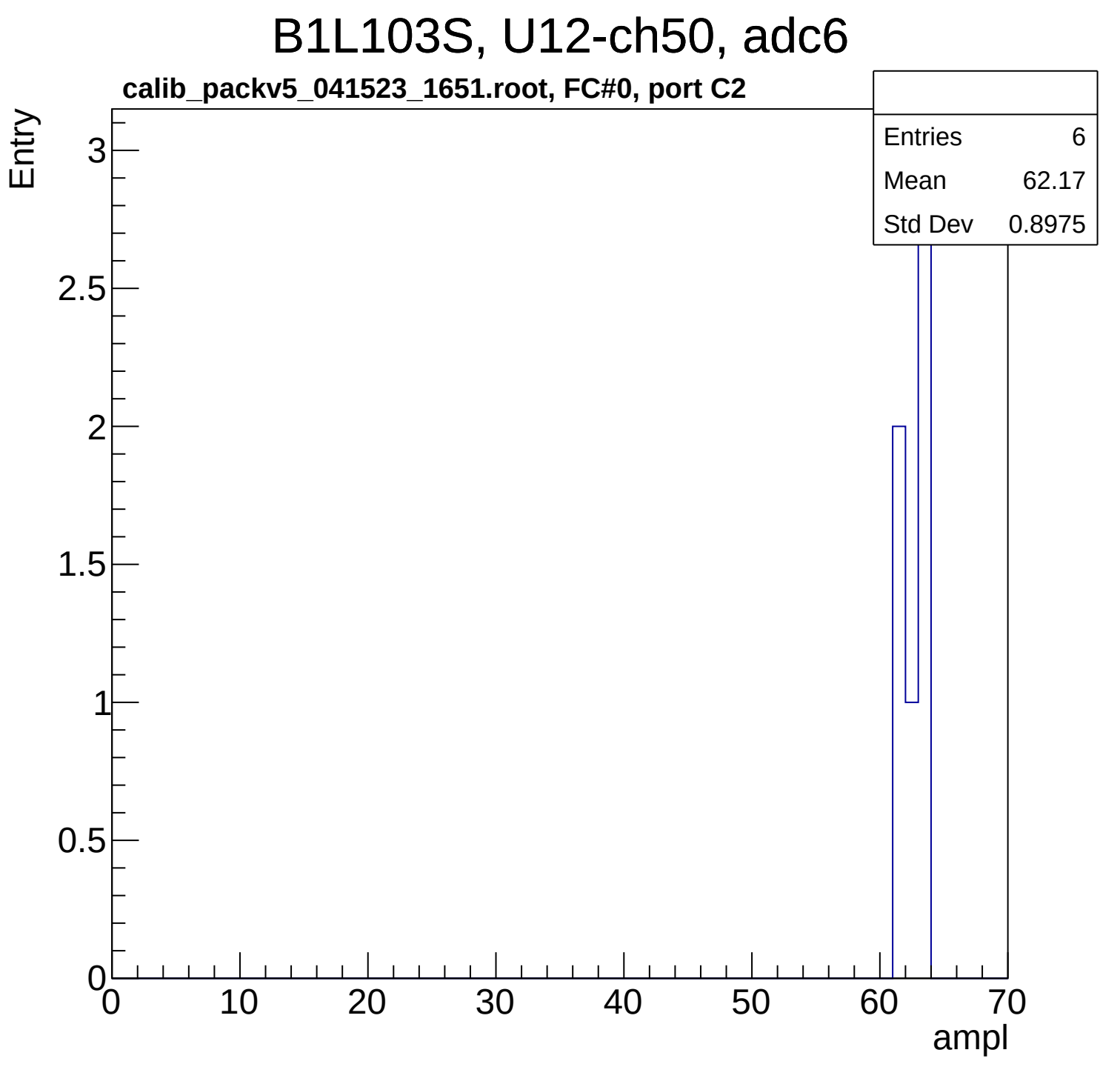
B1L103S, U12-ch50, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.17
Std Dev 0.8975
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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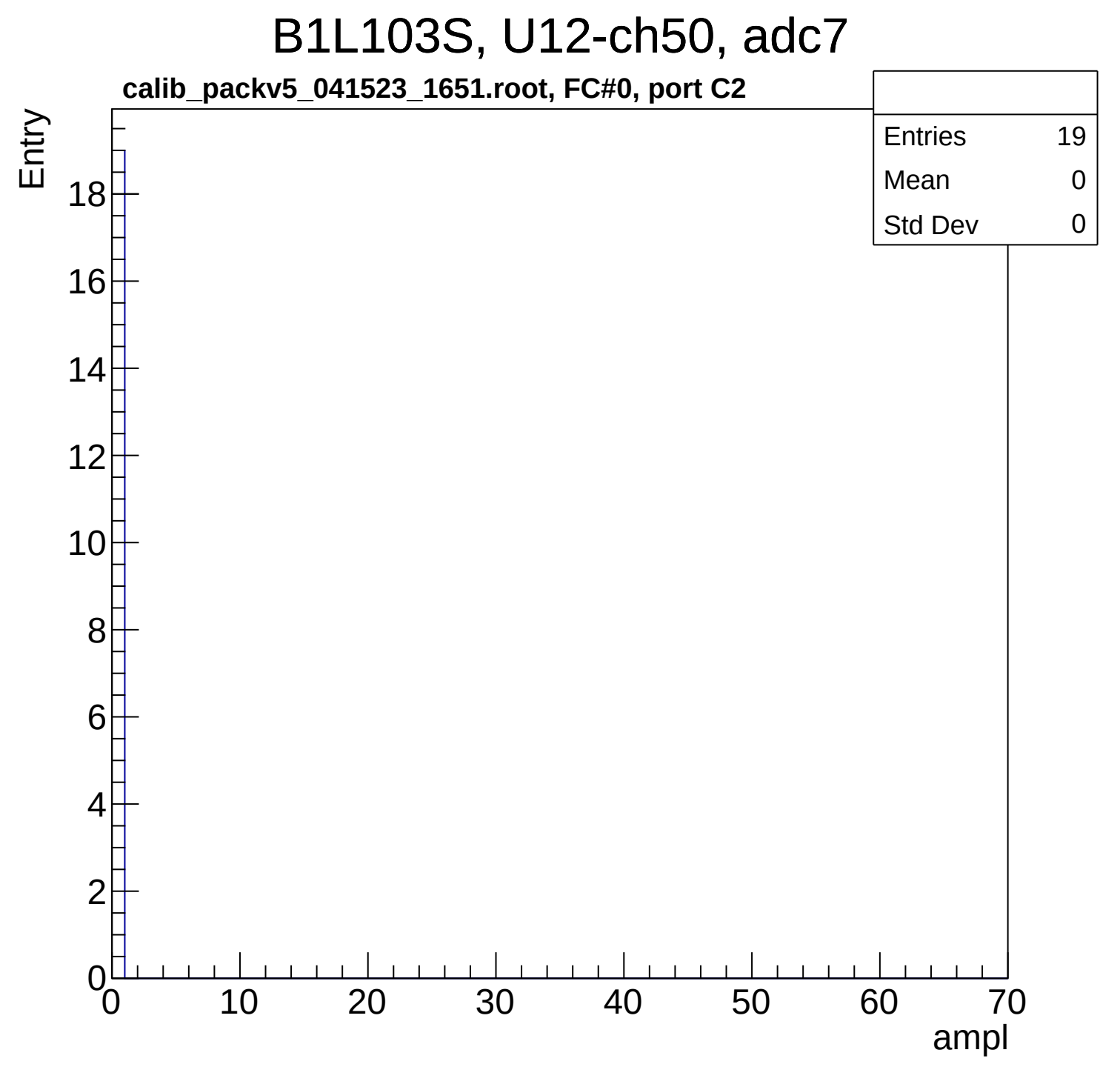
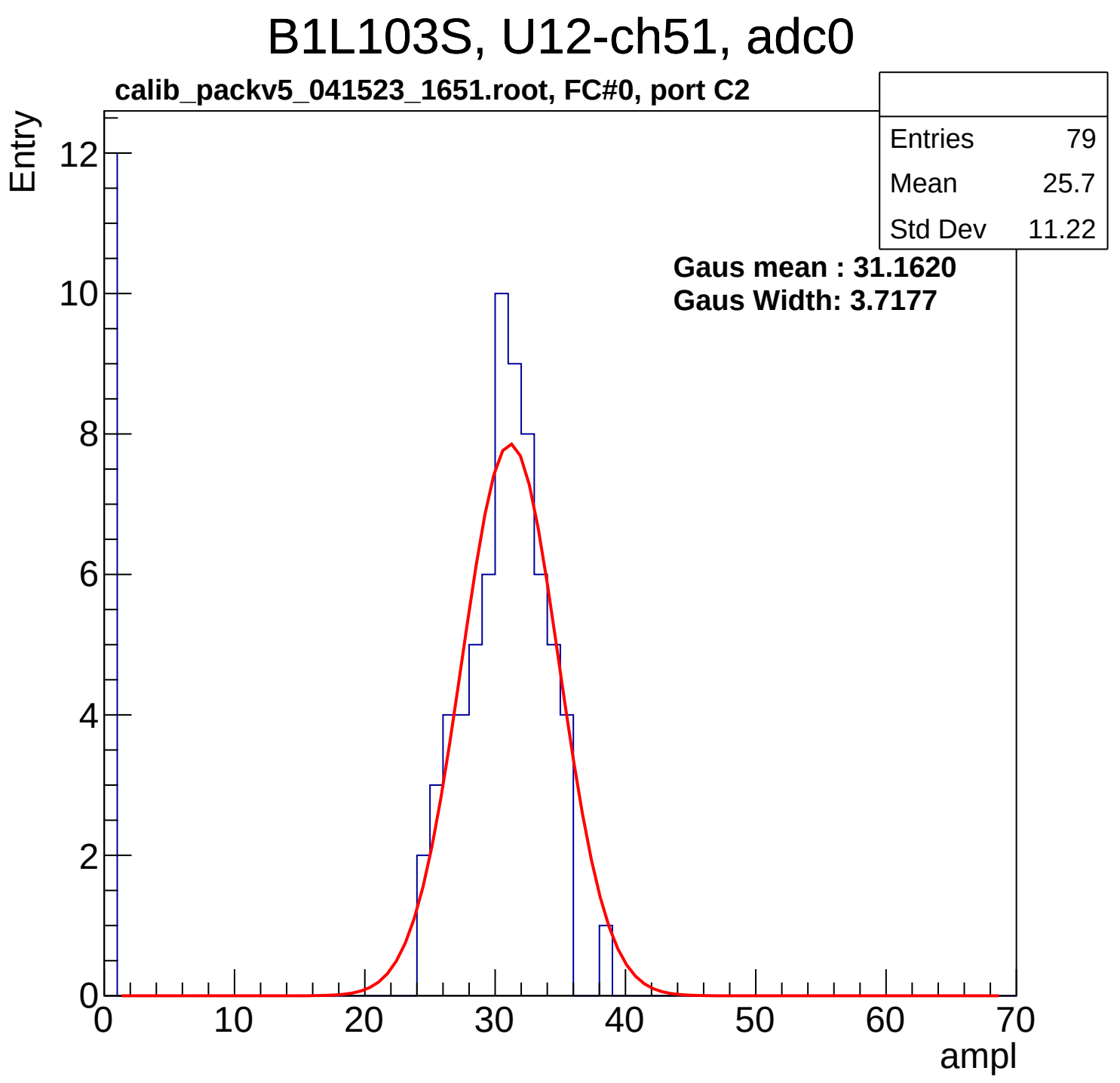
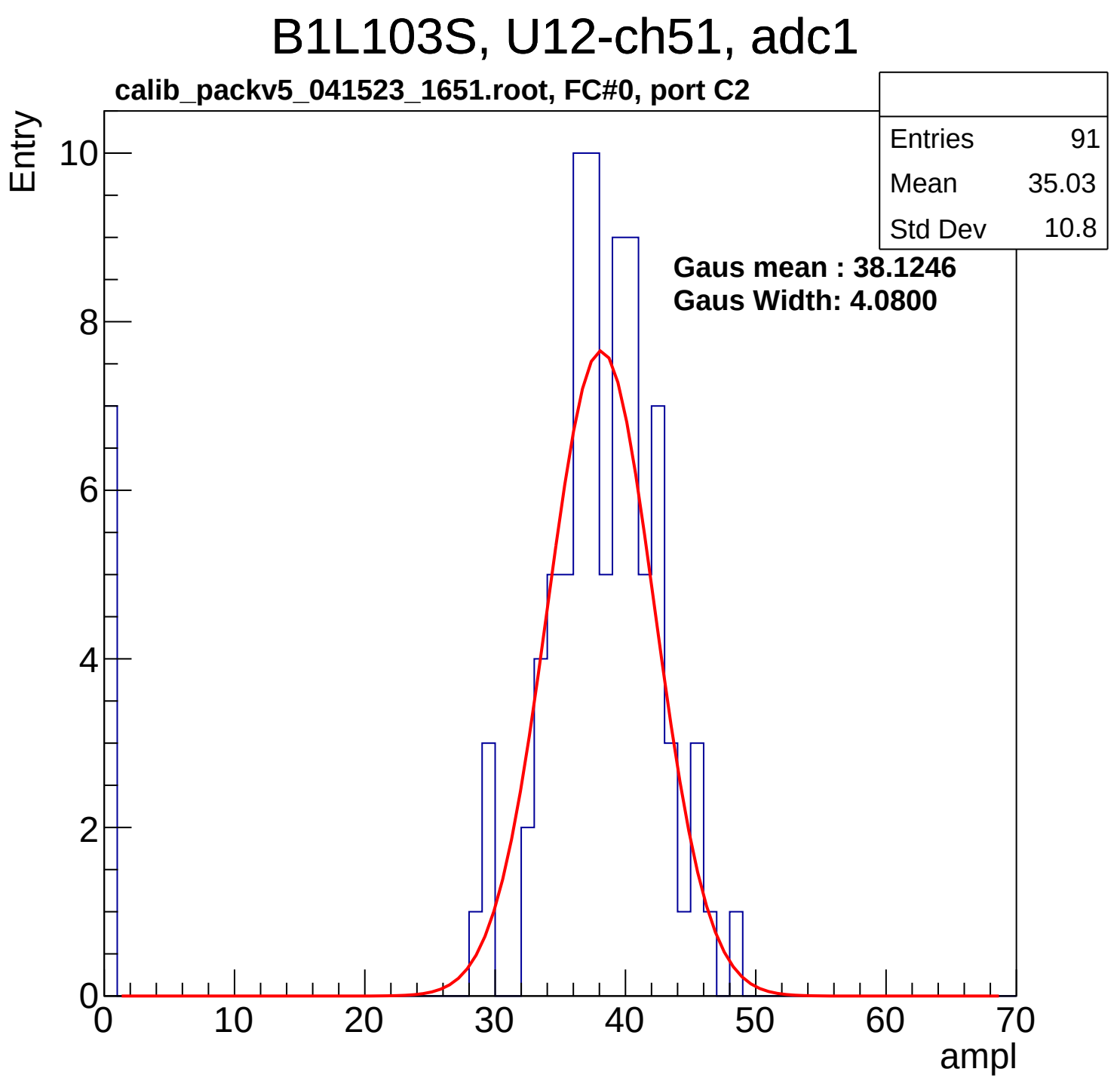

B1L103S, U12-ch50, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch51, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 25.7
Std Dev 11.22
Gaus mean : 31.1620
Gaus Width: 3.7177
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U12-ch51, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 35.03
Std Dev 10.8
Gaus mean : 38.1246
Gaus Width: 4.0800
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
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60
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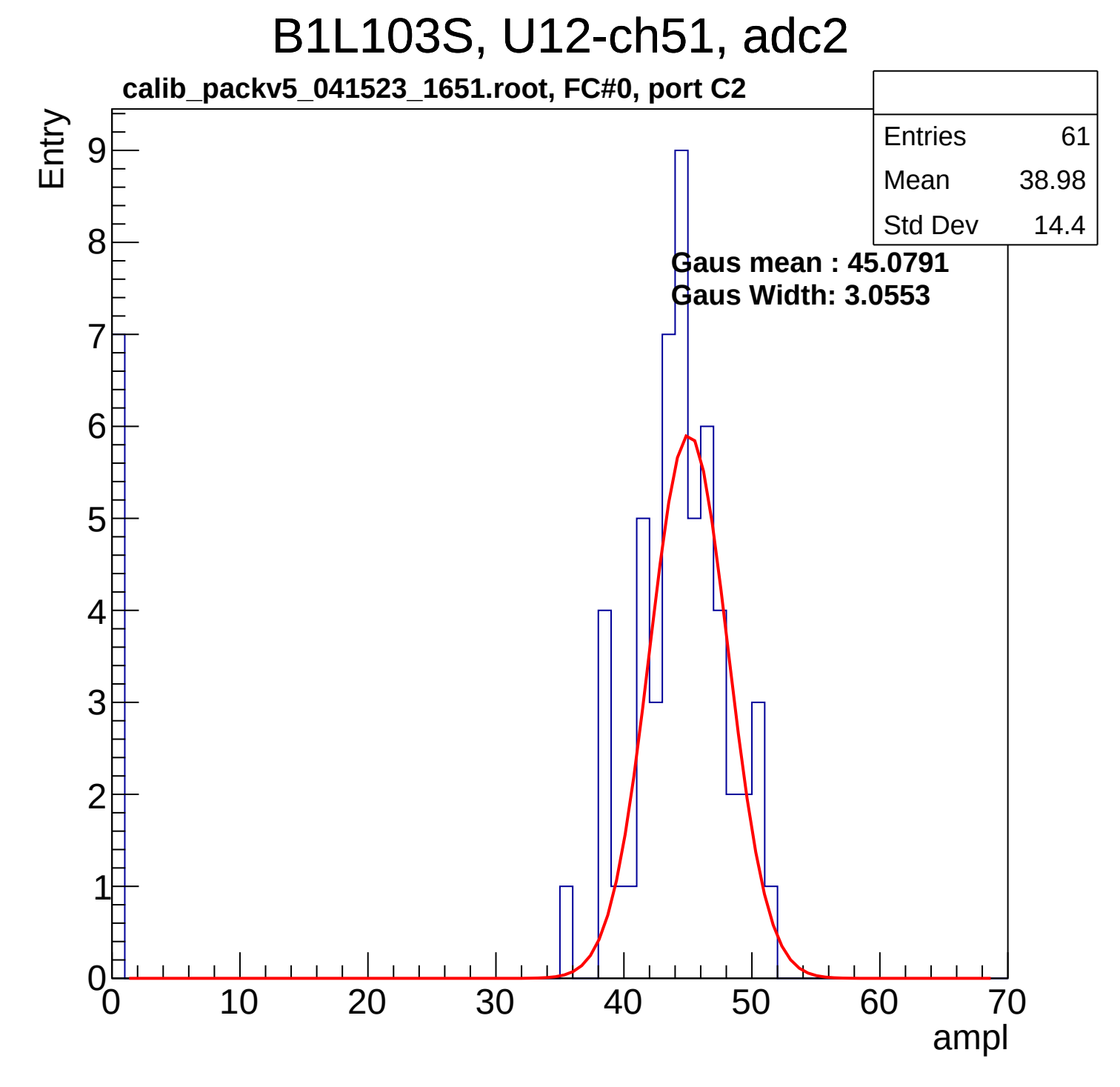
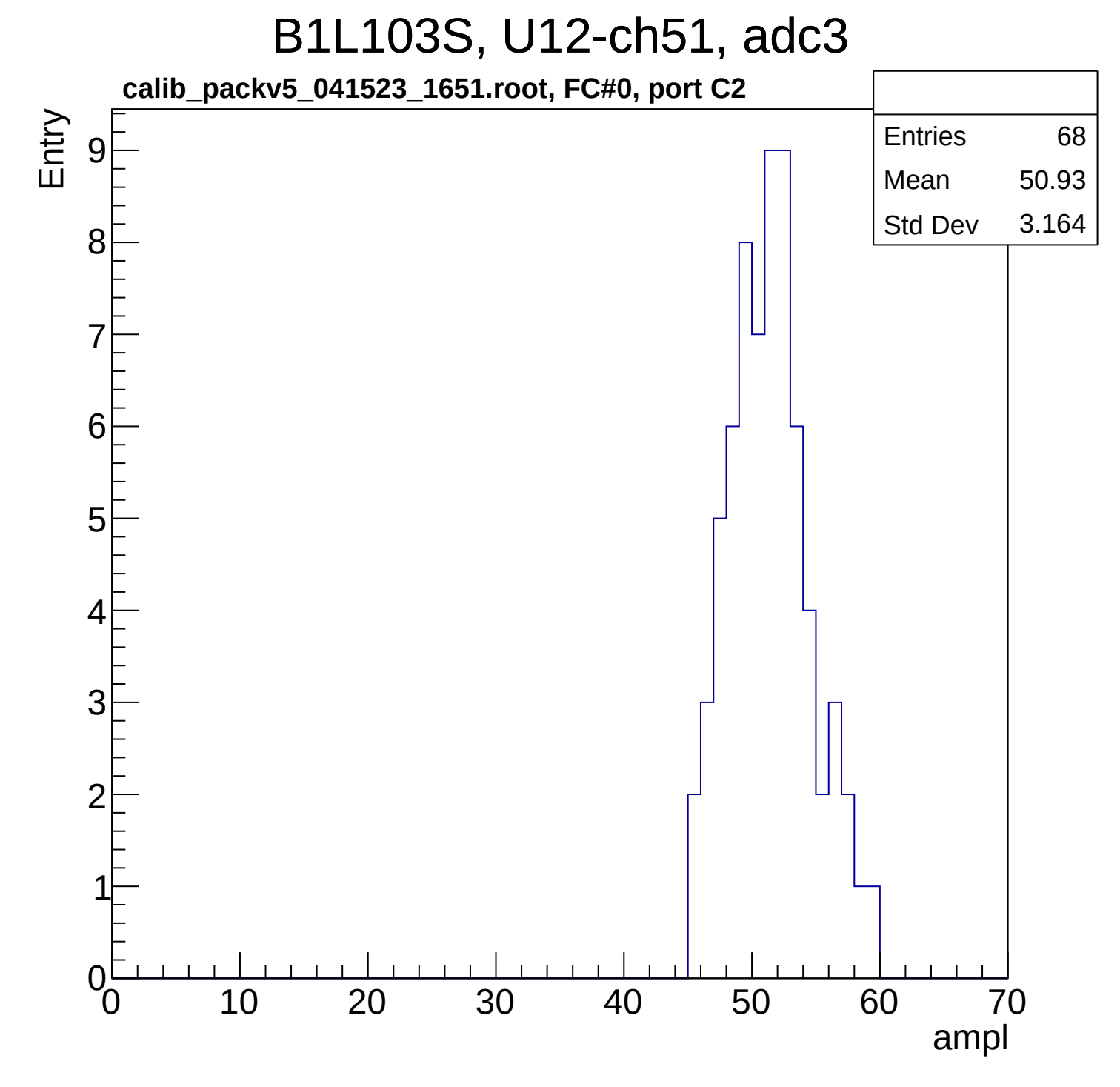

B1L103S, U12-ch51, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 38.98
Std Dev 14.4
Gaus mean : 45.0791
Gaus Width: 3.0553
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch51, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 50.93
Std Dev 3.164
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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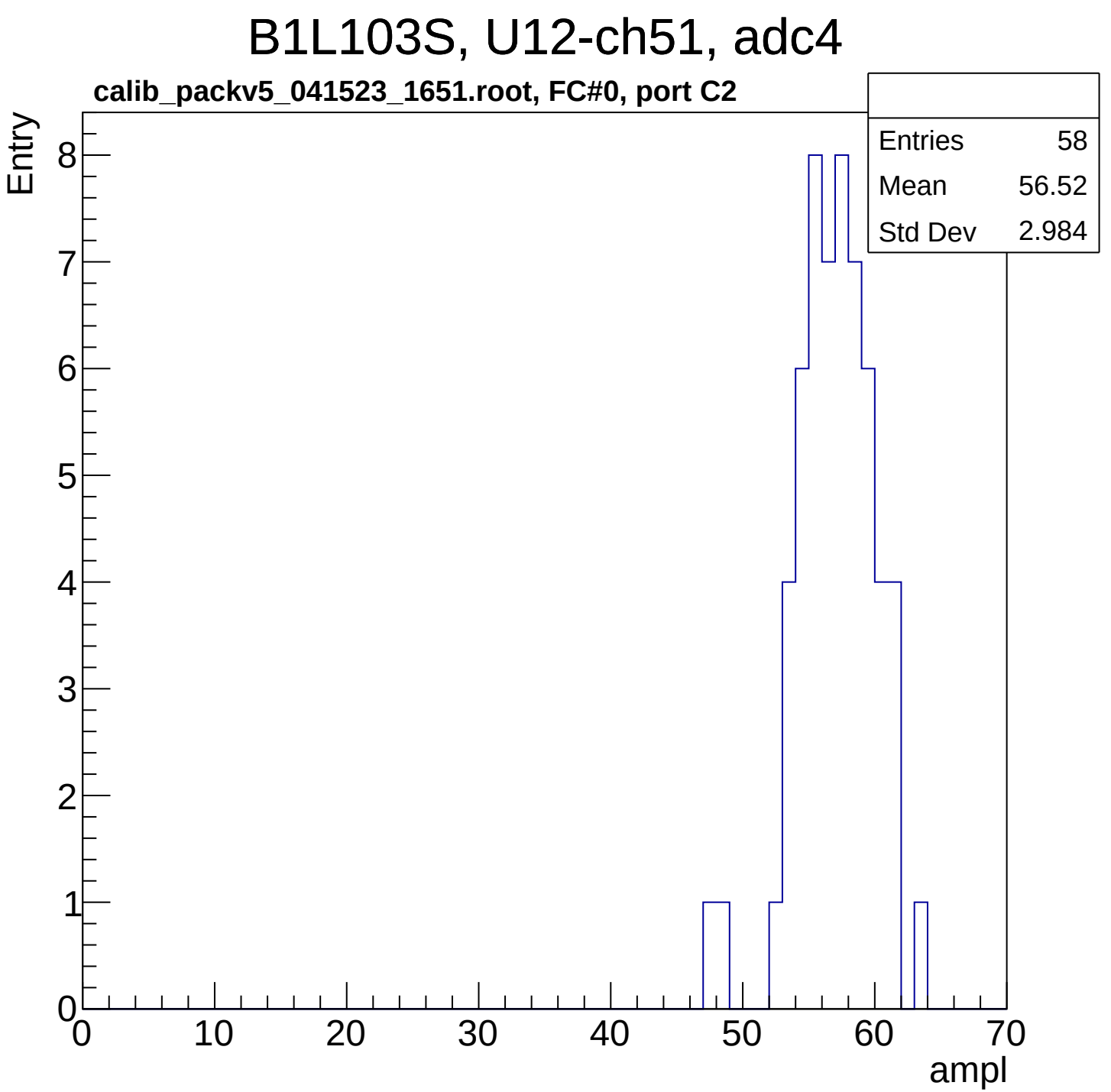
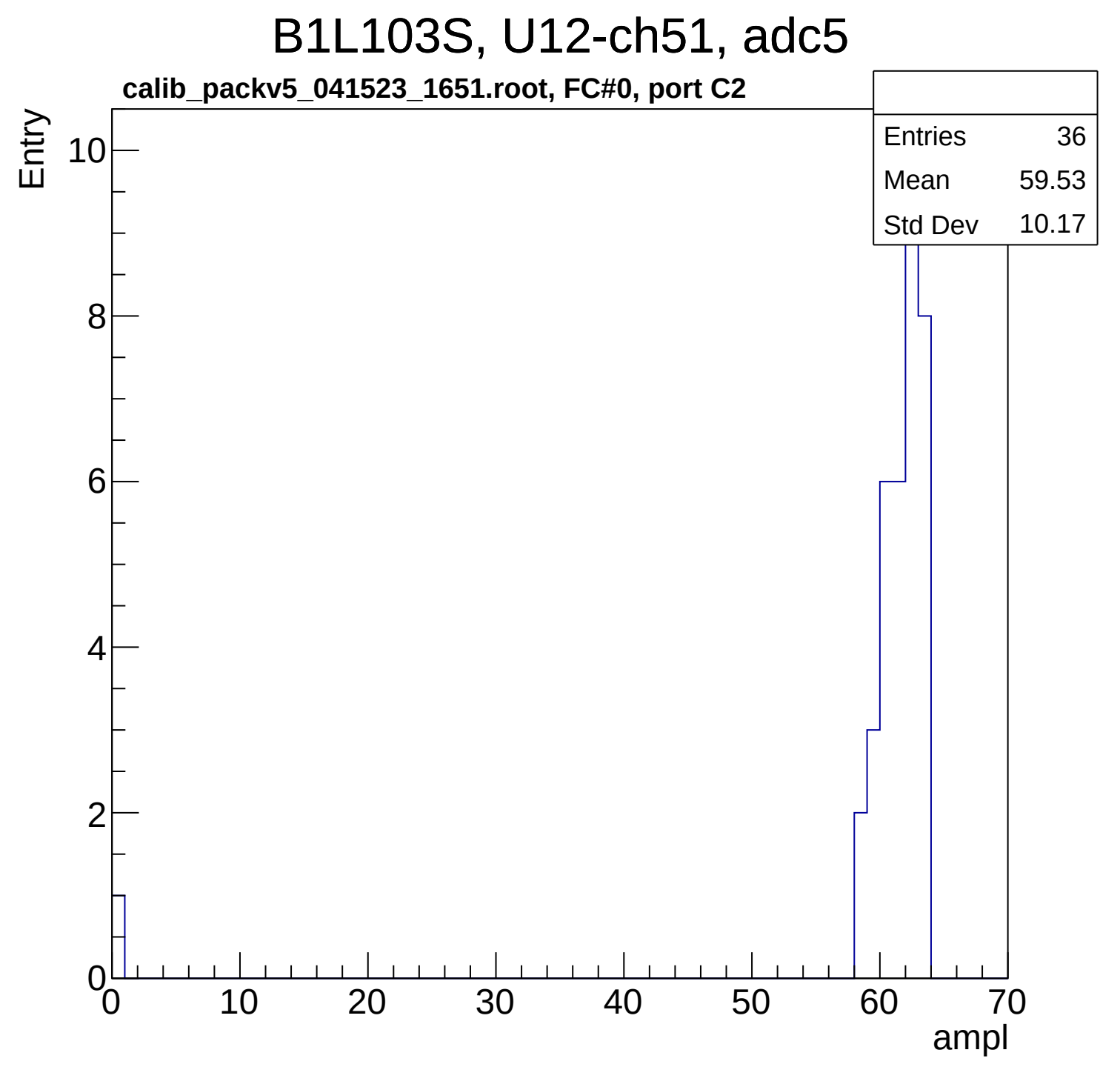
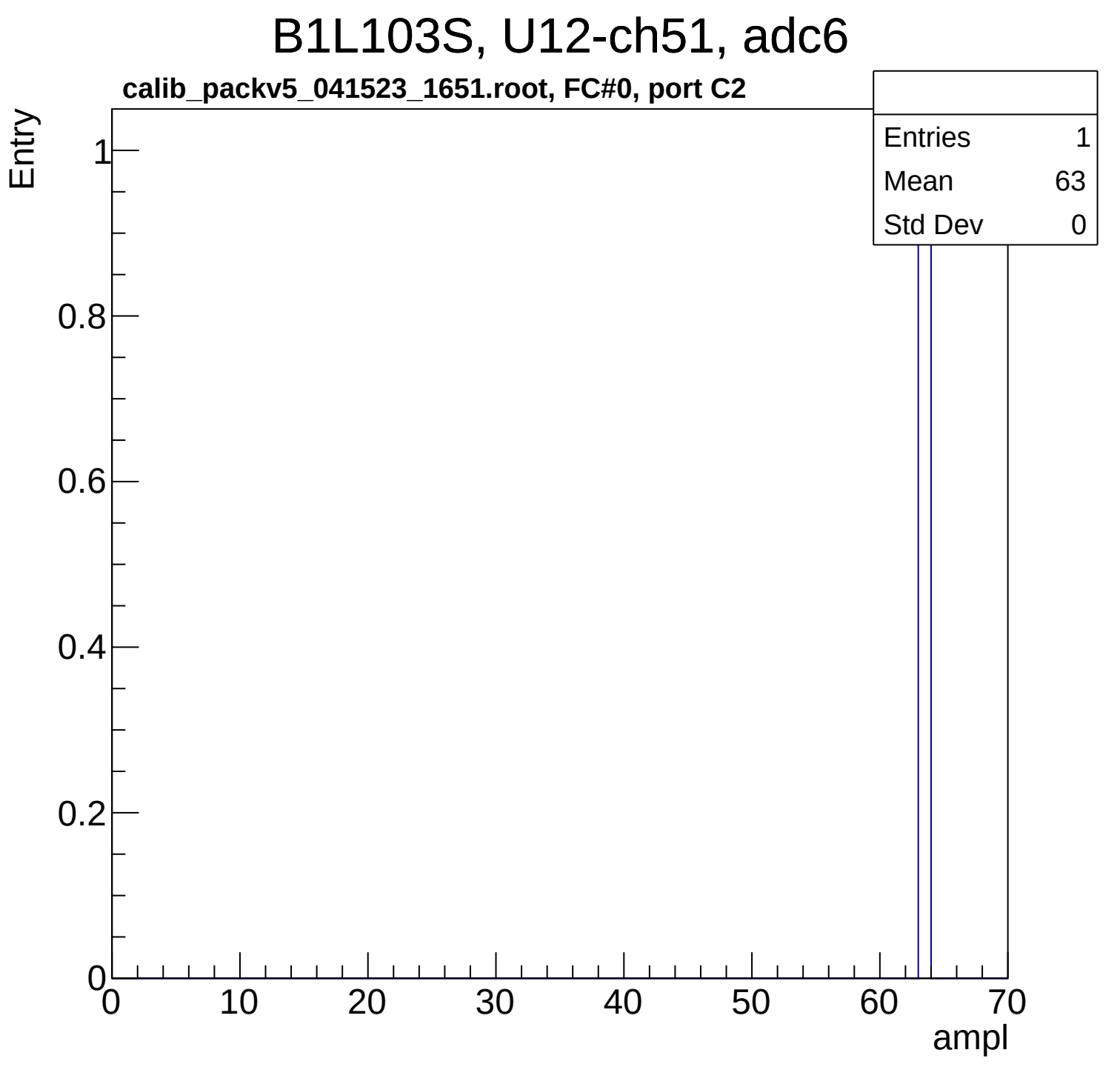
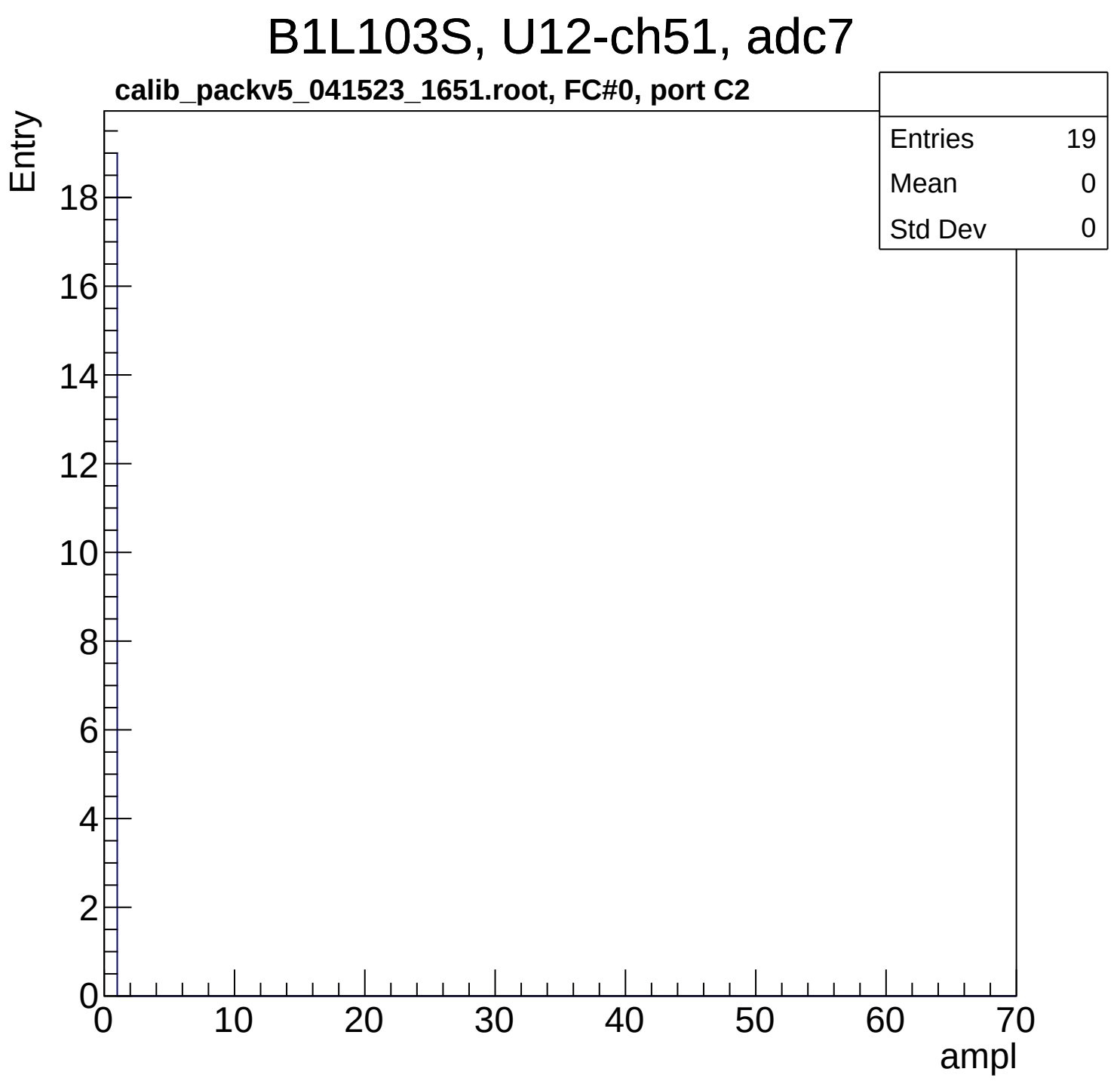
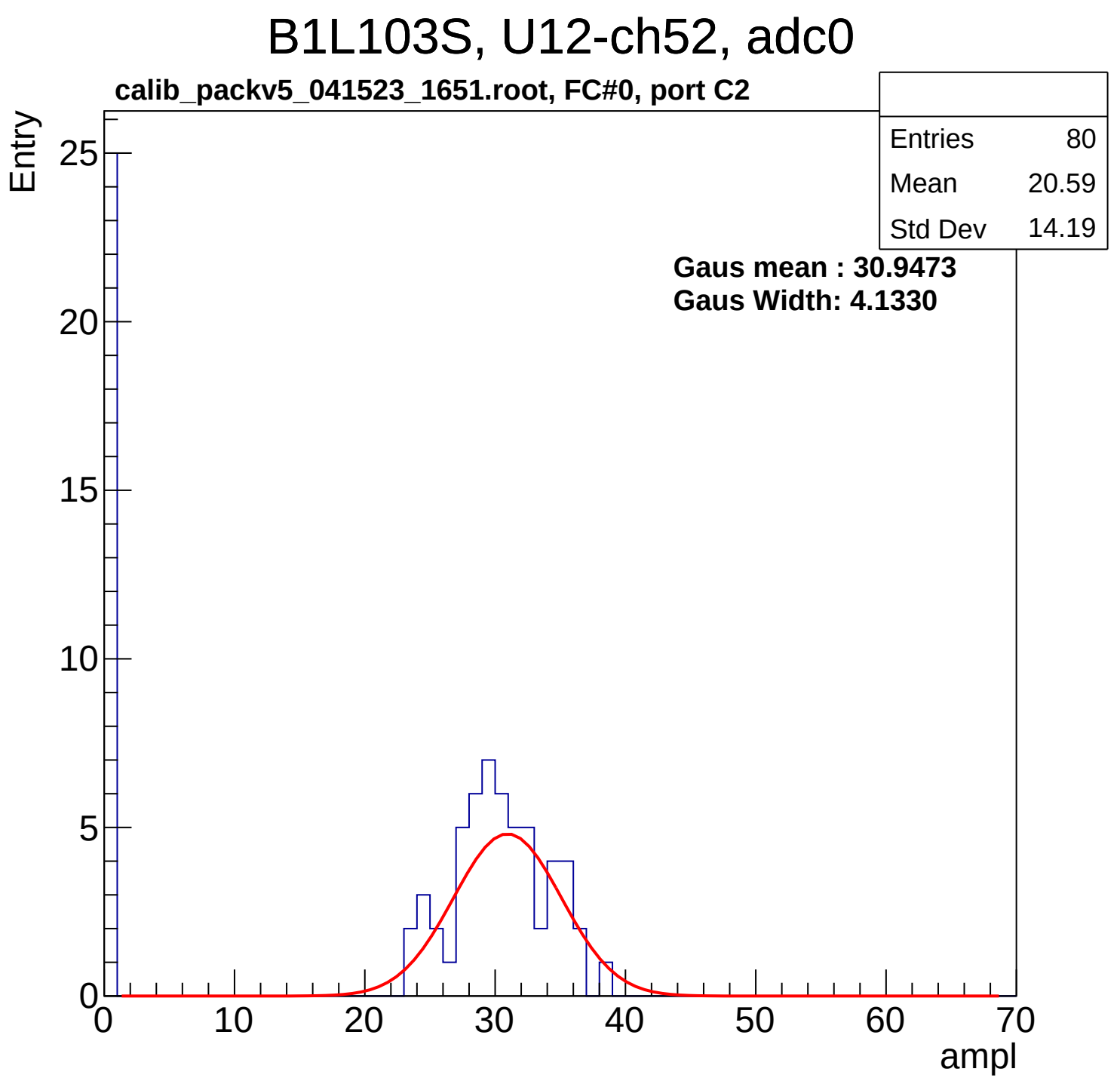
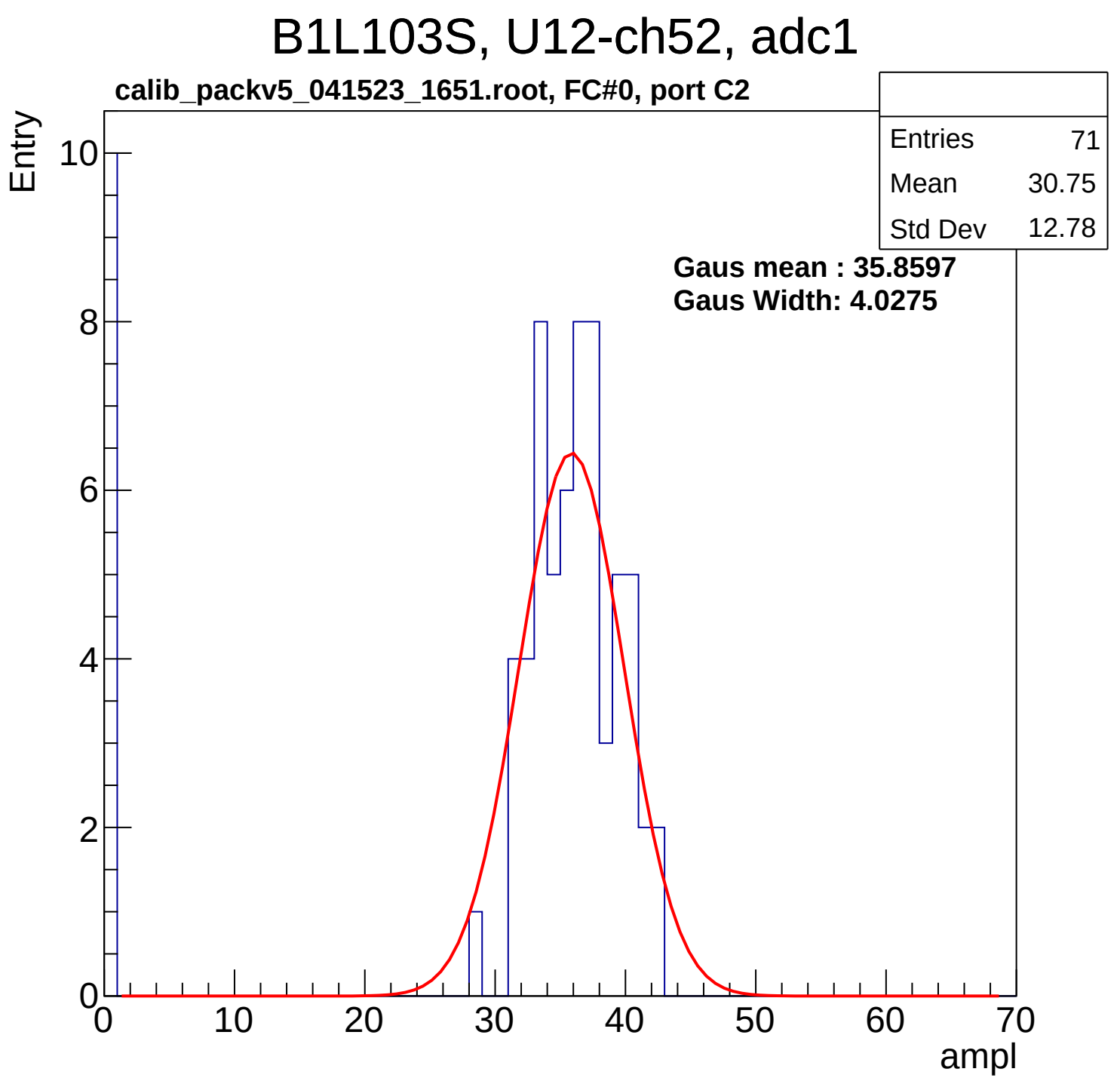

B1L103S, U12-ch51, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 56.52
Std Dev 2.984
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

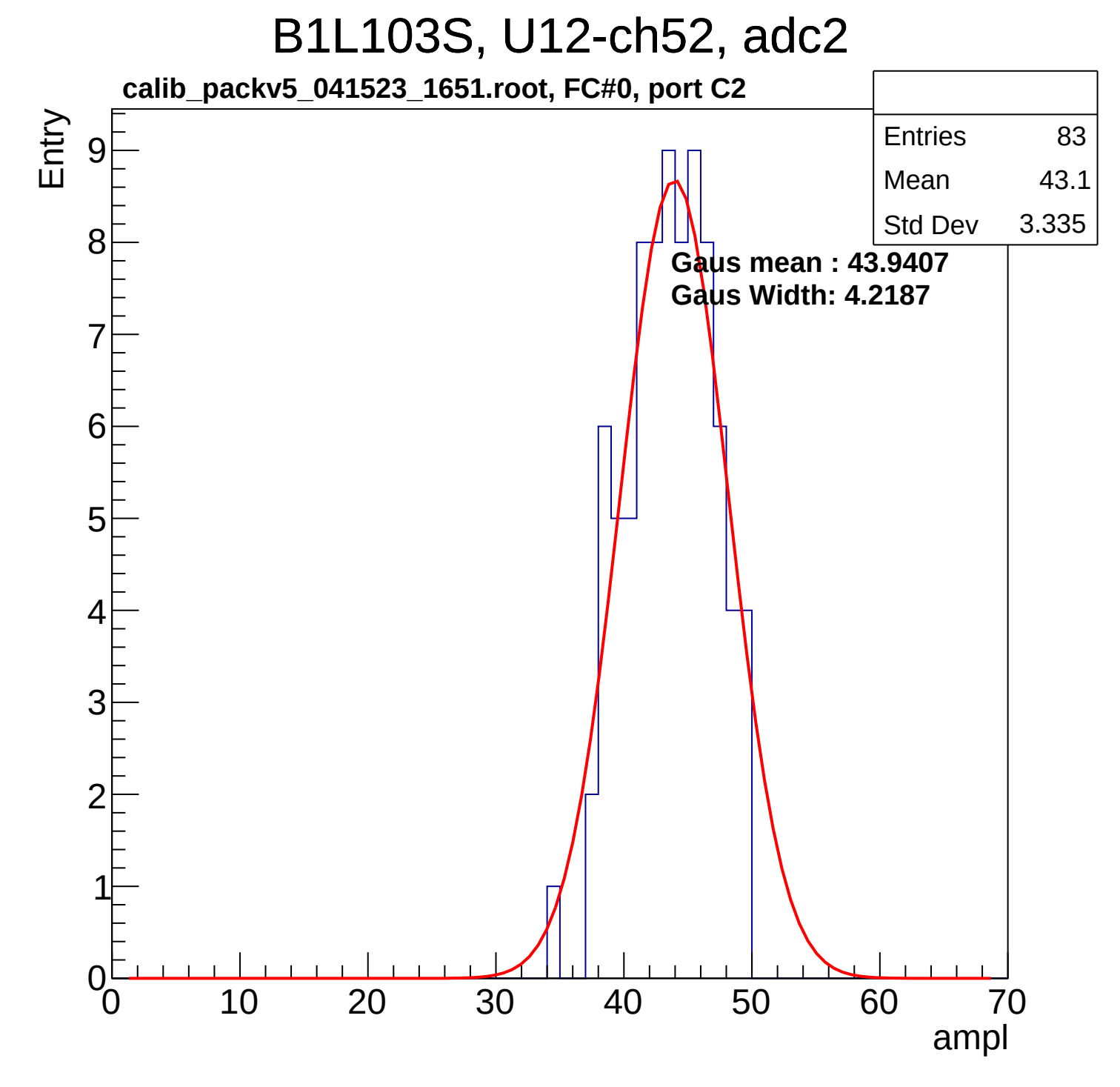

B1L103S, U12-ch51, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 59.53
Std Dev 10.17
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

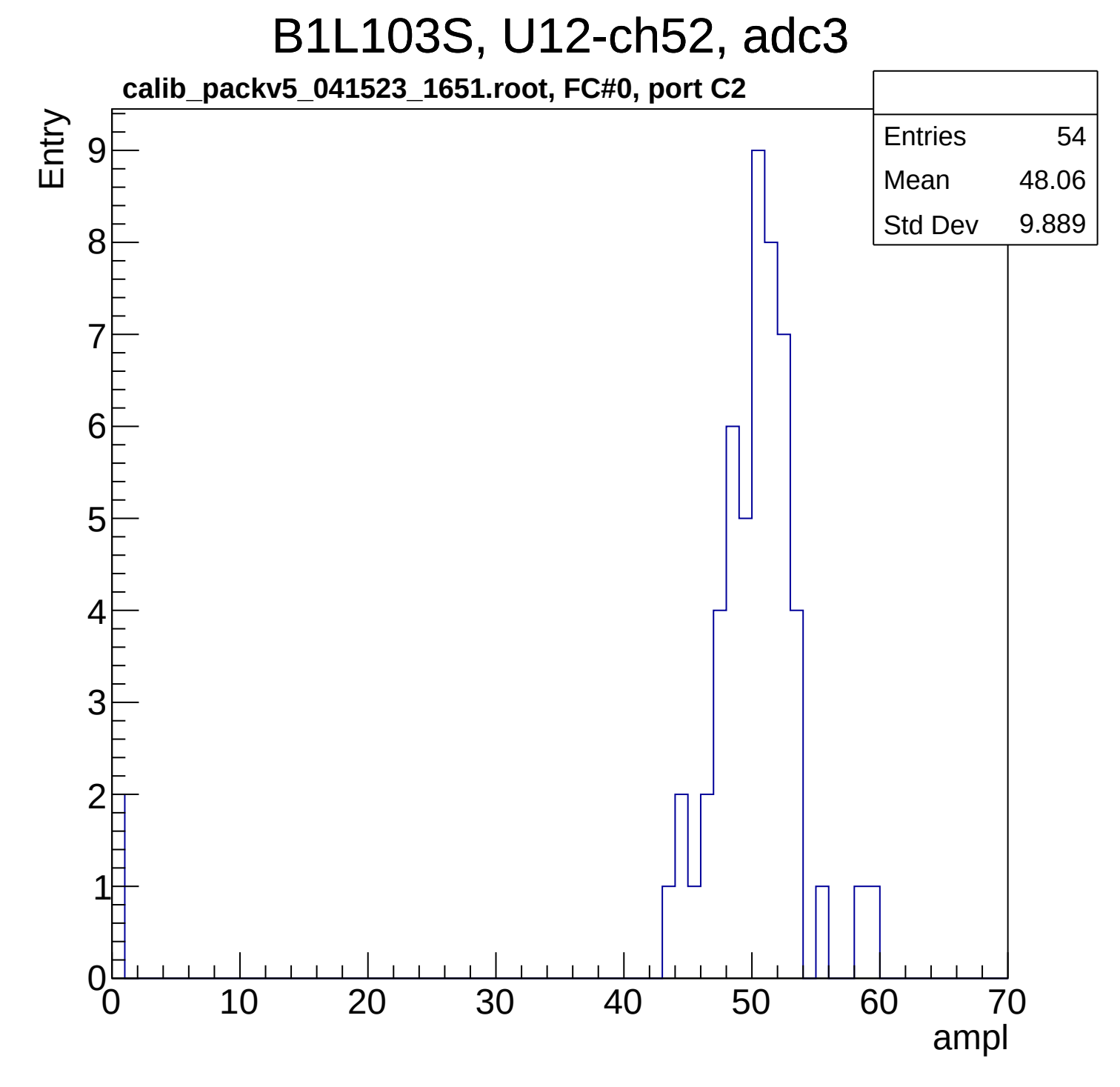

B1L103S, U12-ch51, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch51, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch52, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 20.59
Std Dev 14.19
Gaus mean : 30.9473
Gaus Width: 4.1330
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U12-ch52, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 30.75
Std Dev 12.78
Gaus mean : 35.8597
Gaus Width: 4.0275
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch52, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 43.1
Std Dev 3.335
Gaus mean : 43.9407
Gaus Width: 4.2187
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch52, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 48.06
Std Dev 9.889
Entry
ampl
0
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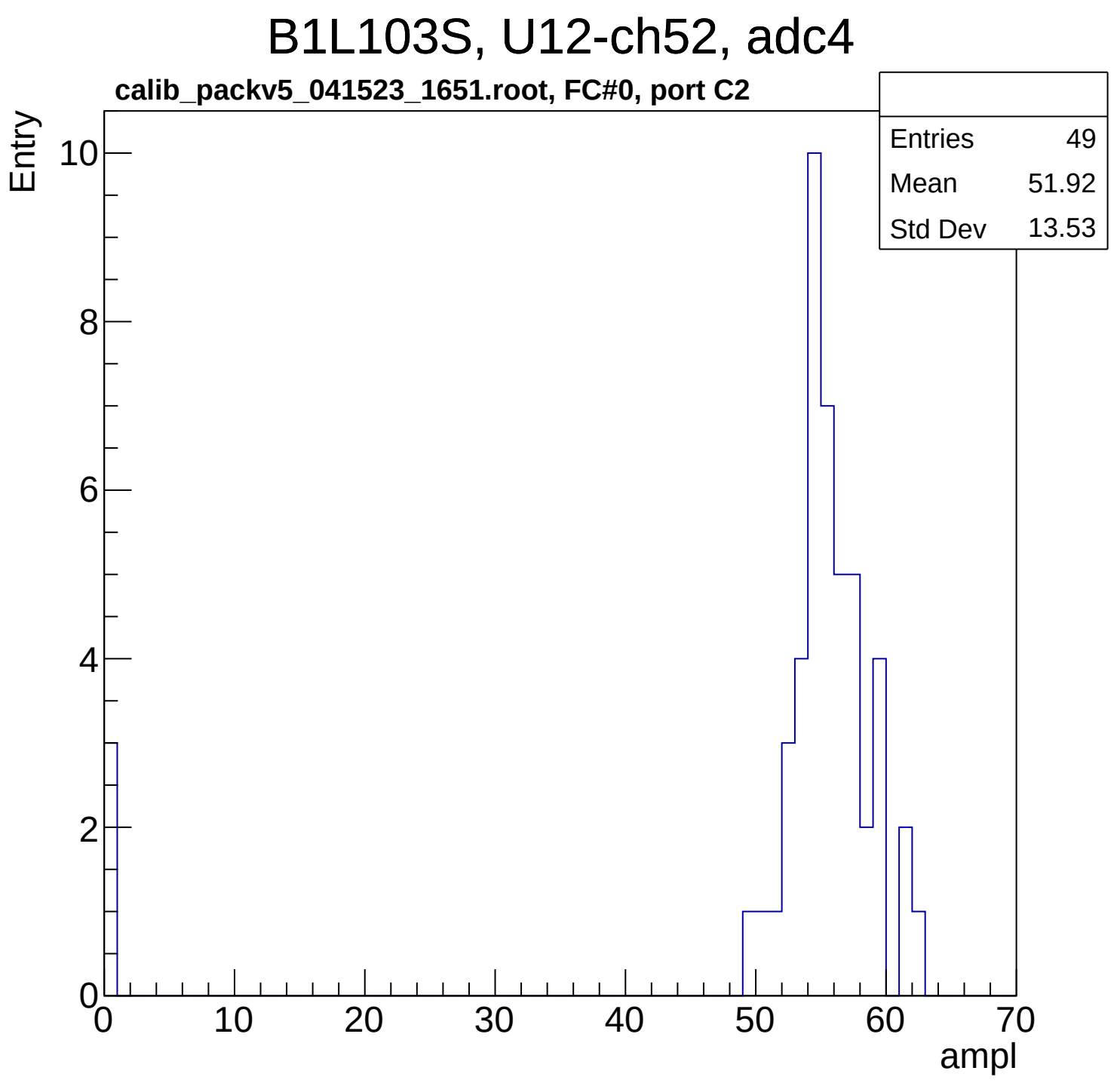
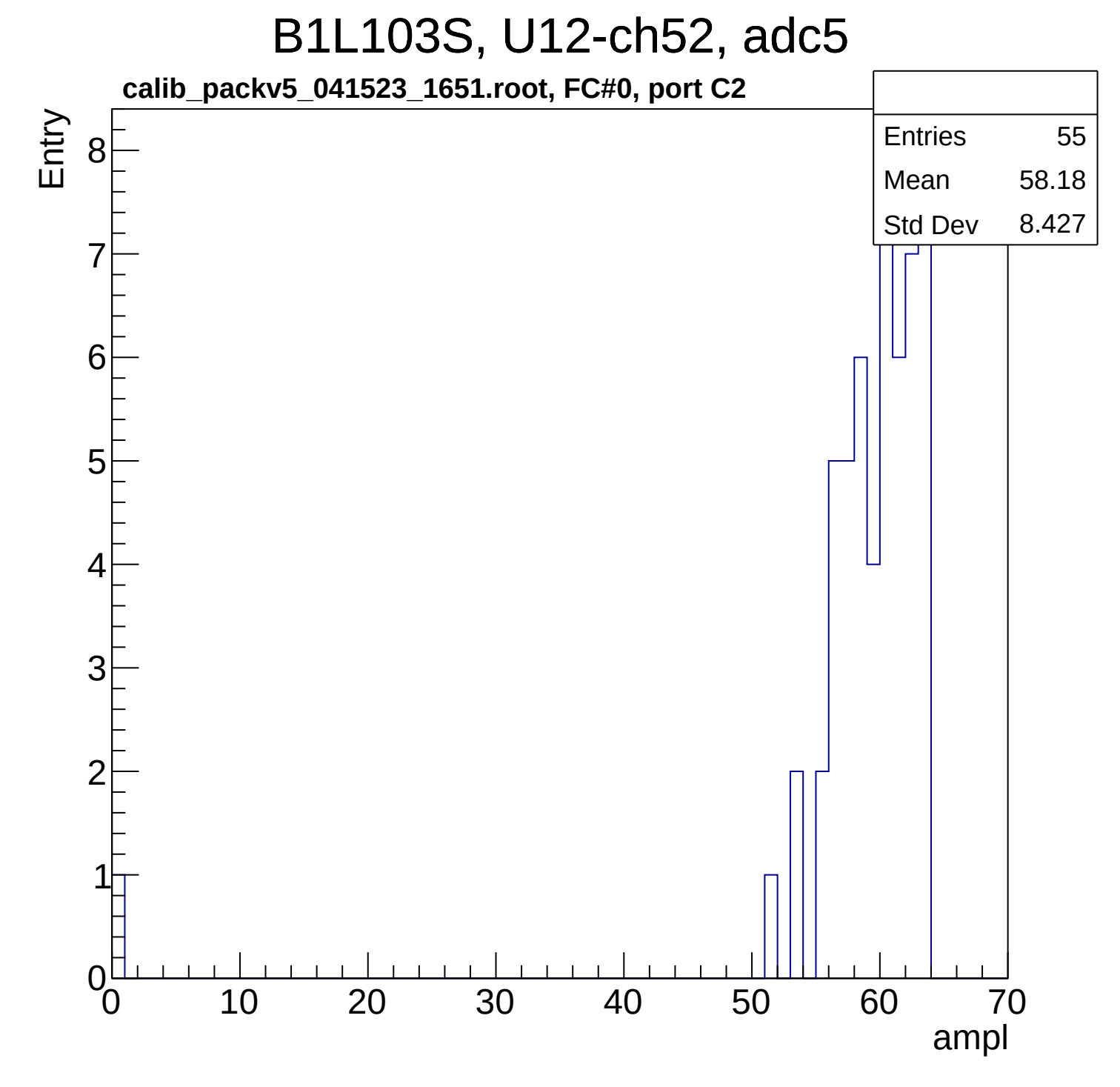
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch52, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 51.92
Std Dev 13.53
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch52, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.18
Std Dev 8.427
Entry
ampl
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4
5
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8
0
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60
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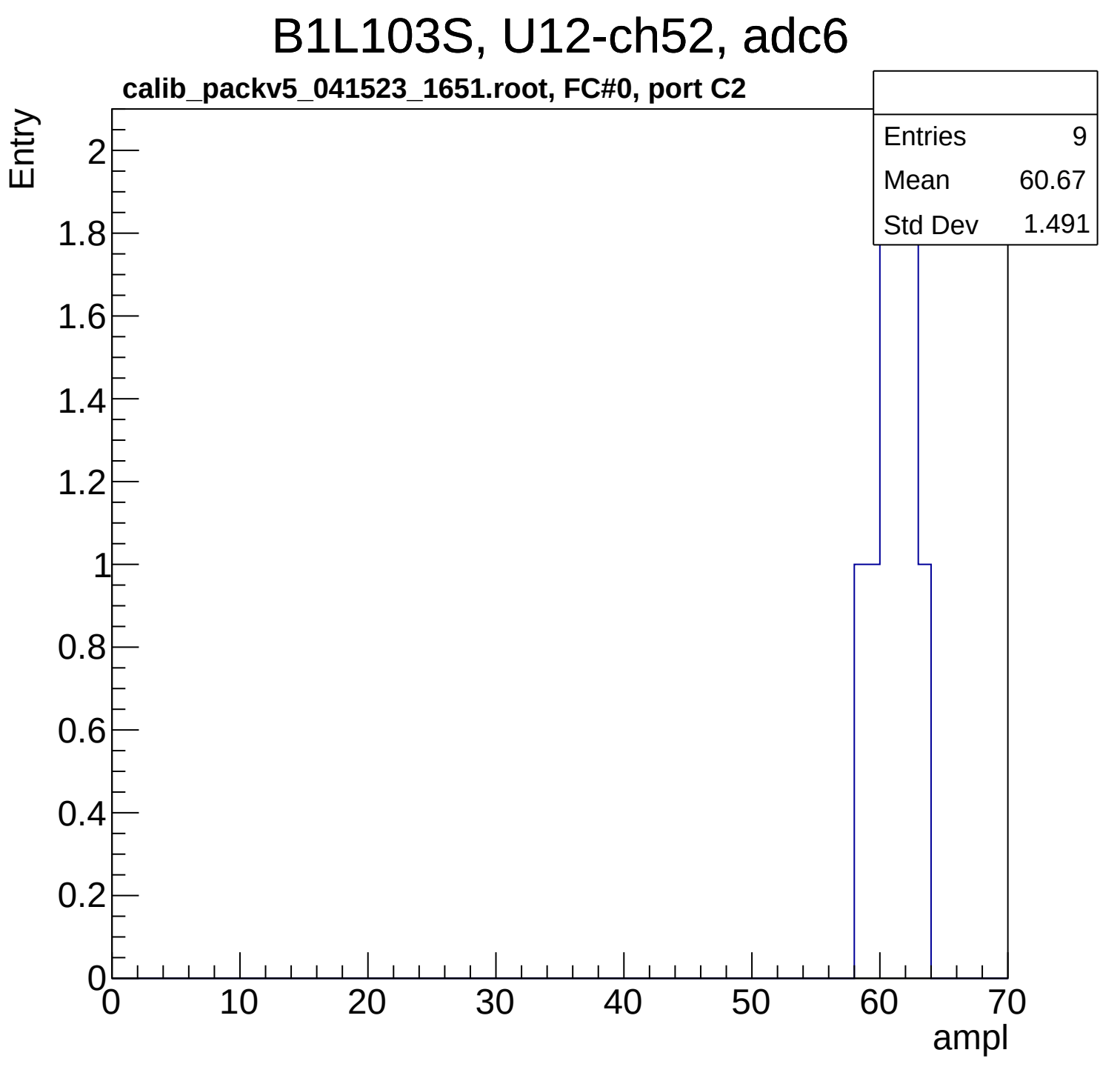
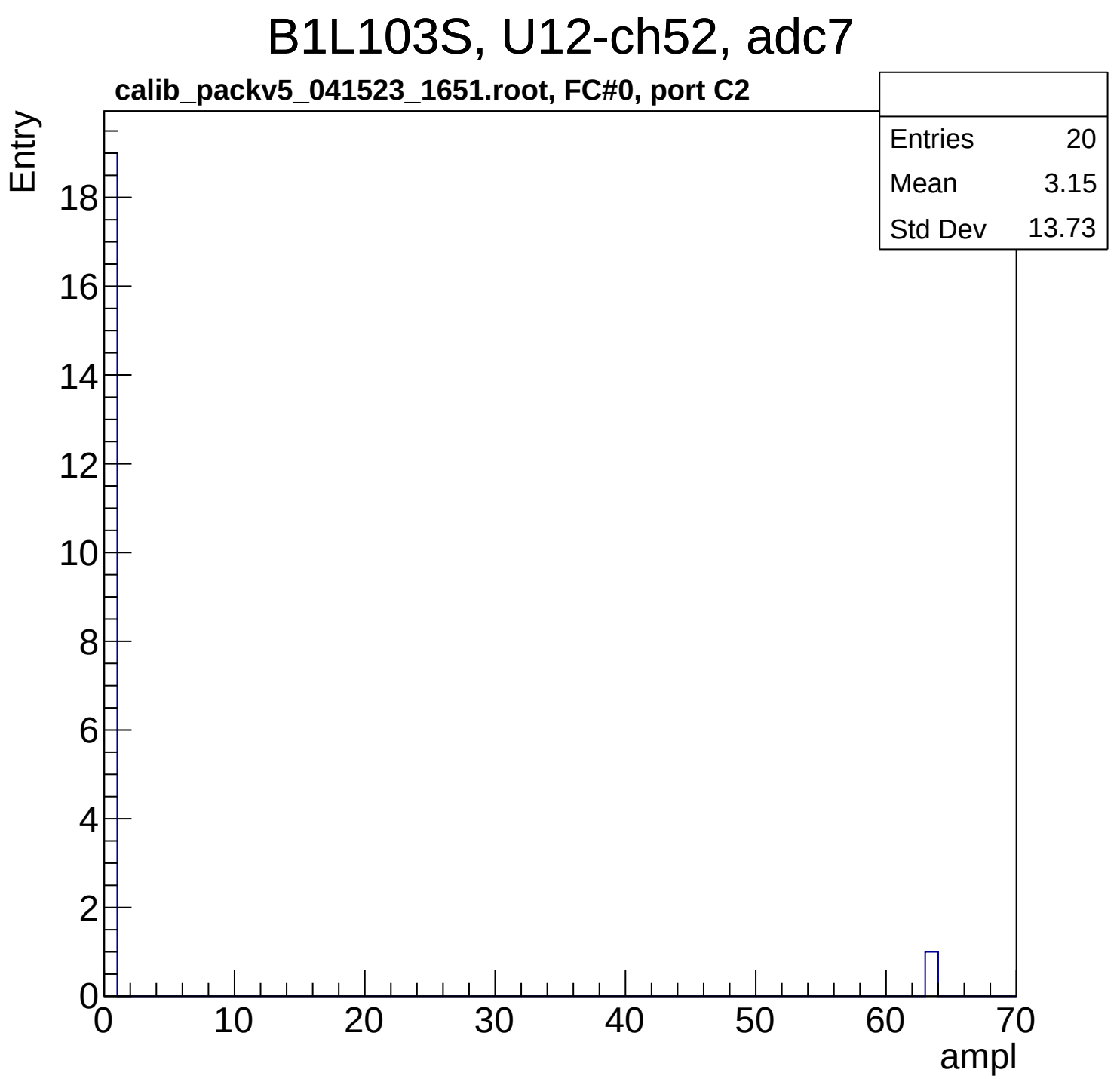
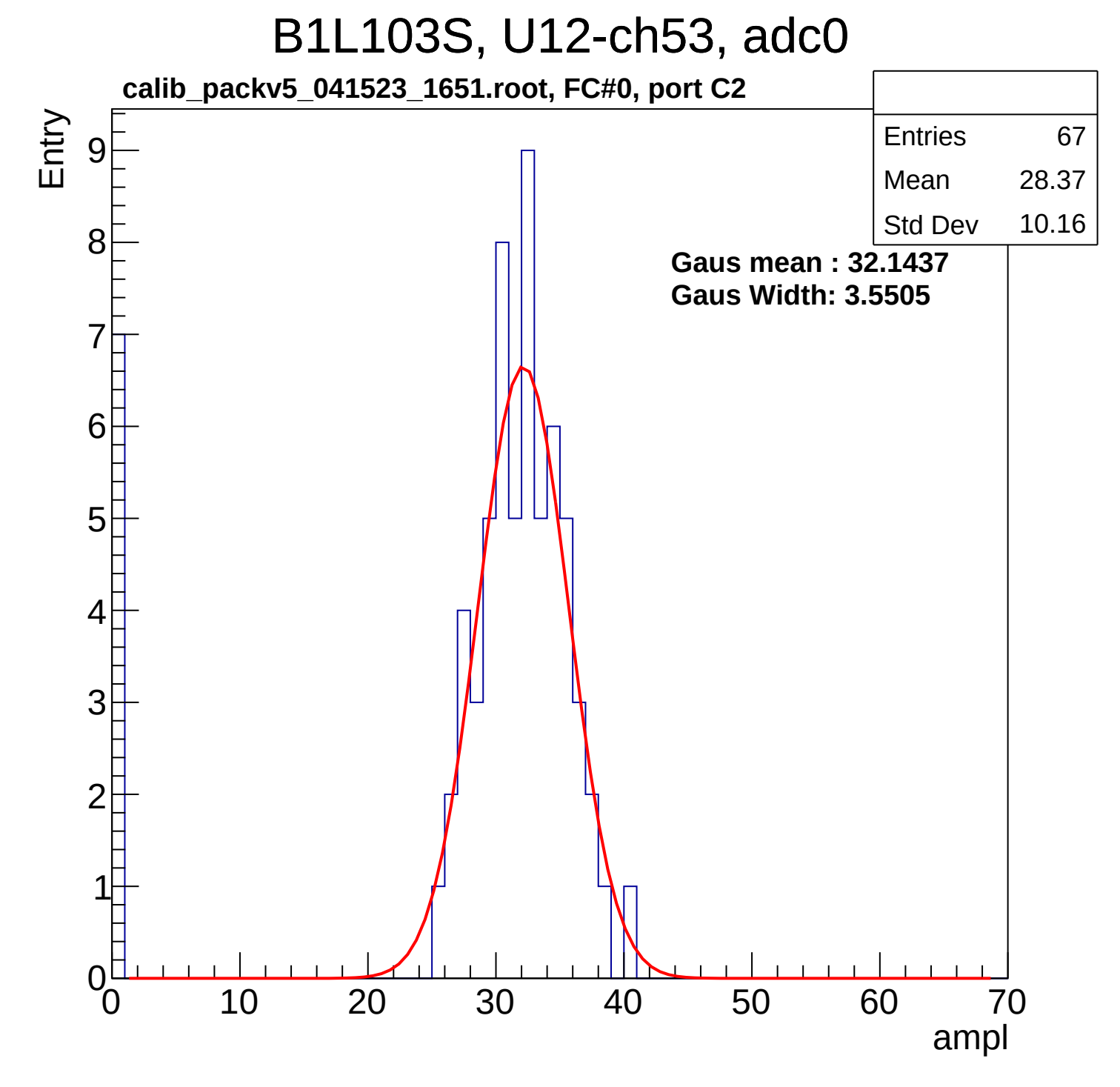
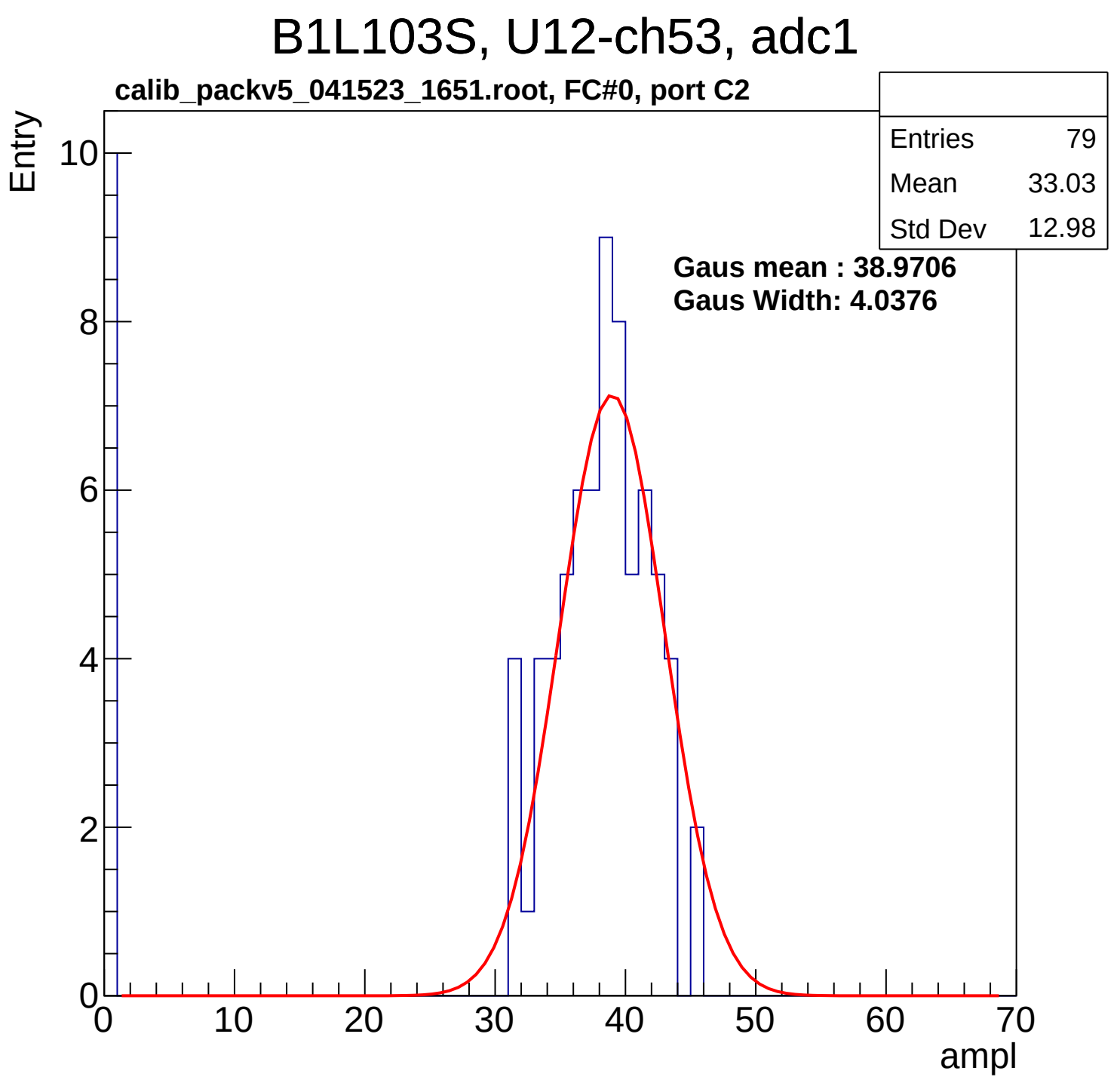
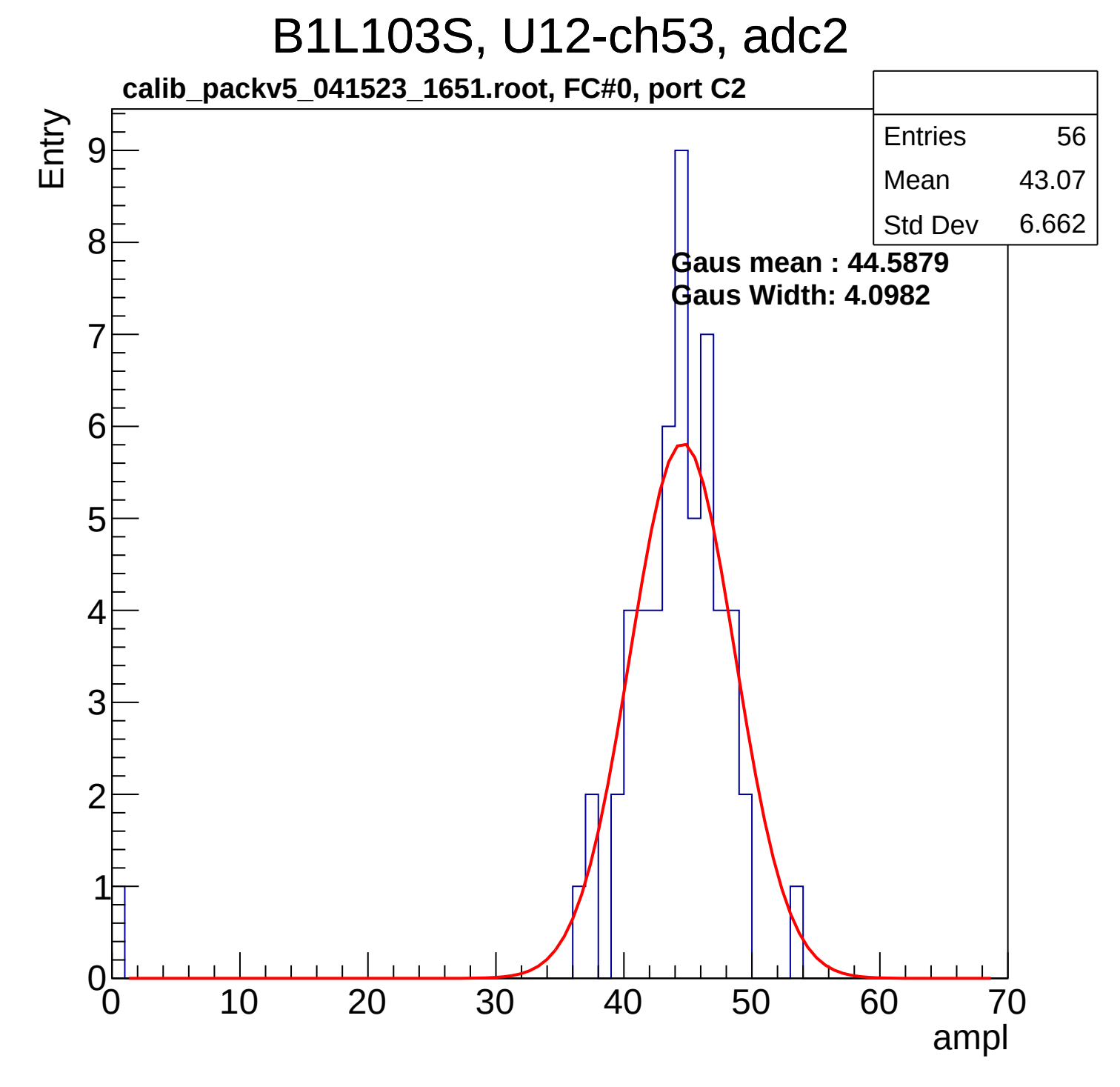

B1L103S, U12-ch52, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 60.67
Std Dev 1.491
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U12-ch52, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch53, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 28.37
Std Dev 10.16
Gaus mean : 32.1437
Gaus Width: 3.5505
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch53, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 33.03
Std Dev 12.98
Gaus mean : 38.9706
Gaus Width: 4.0376
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch53, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 43.07
Std Dev 6.662
Gaus mean : 44.5879
Gaus Width: 4.0982
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
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60
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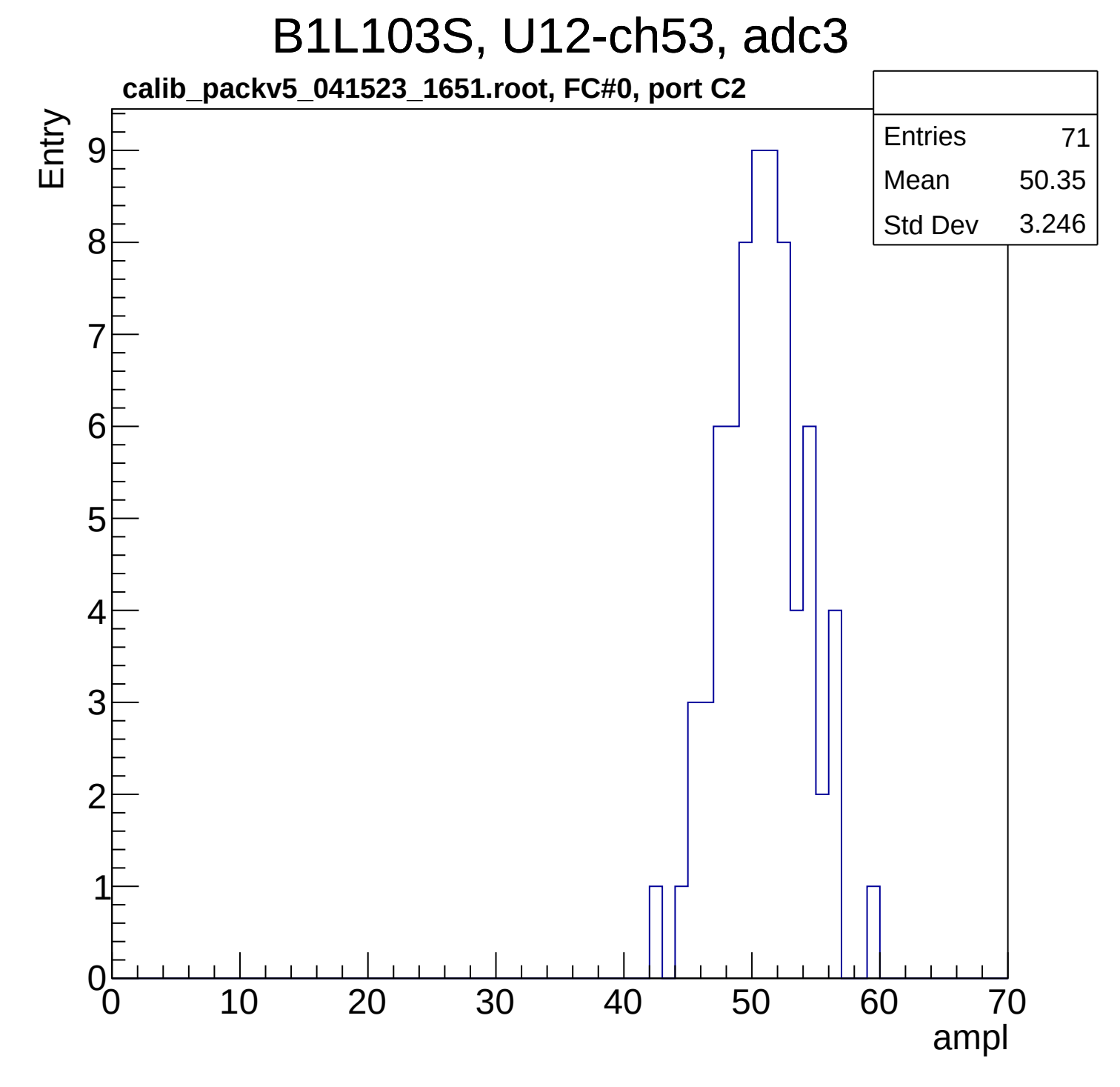
B1L103S, U12-ch53, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 50.35
Std Dev 3.246
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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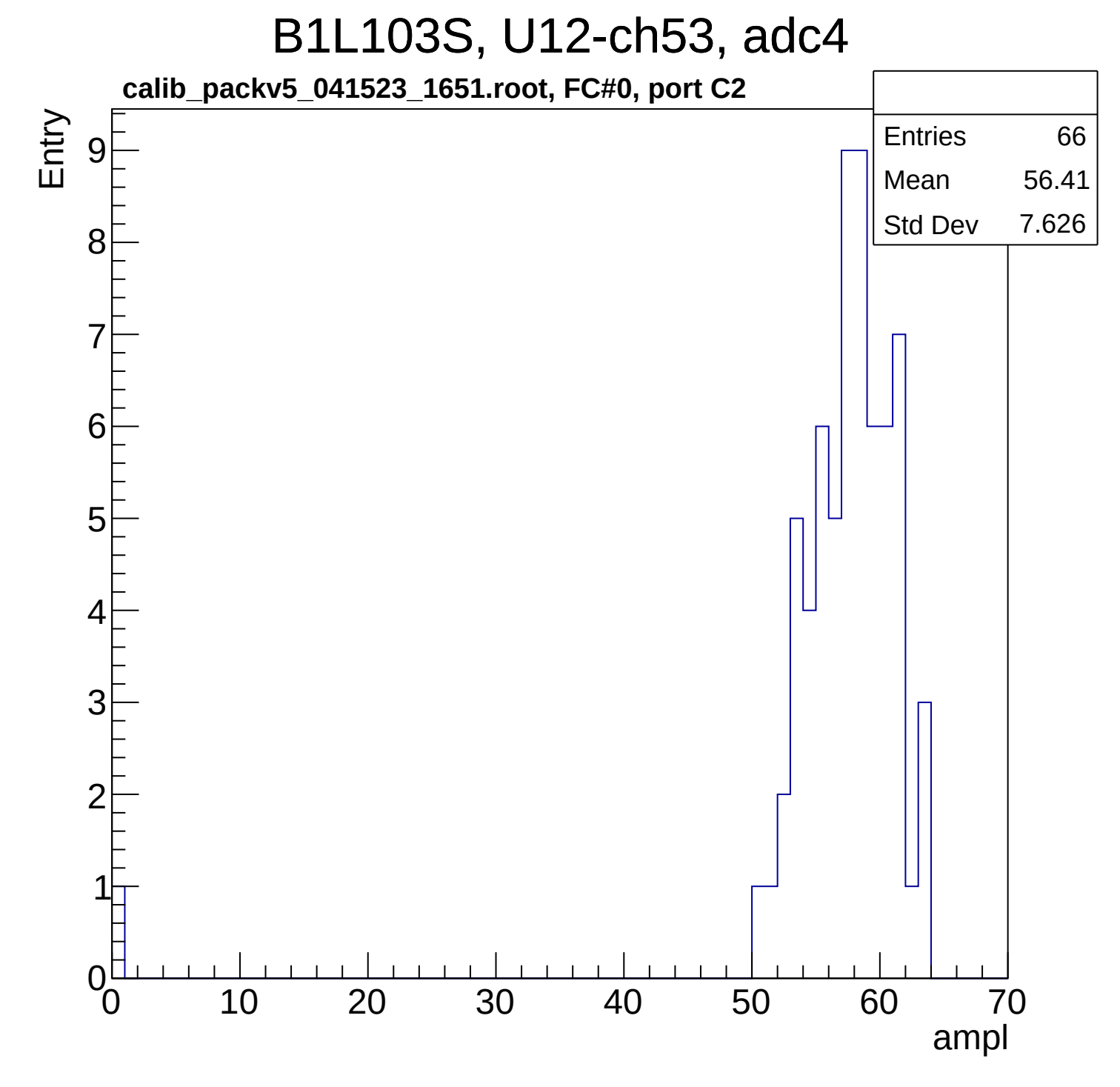
B1L103S, U12-ch53, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 56.41
Std Dev 7.626
Entry
ampl
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2
3
4
5
6
7
8
9
0
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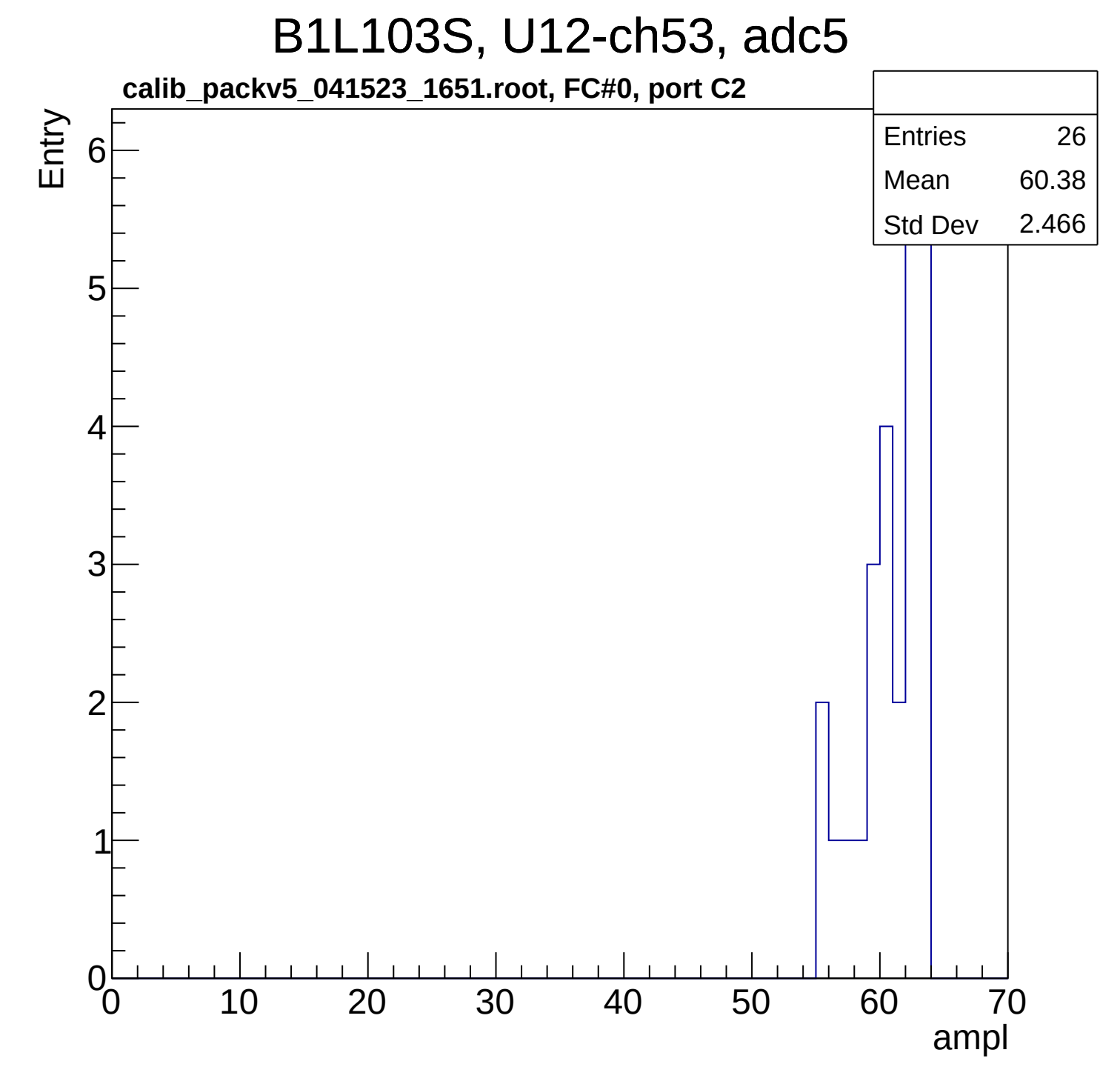
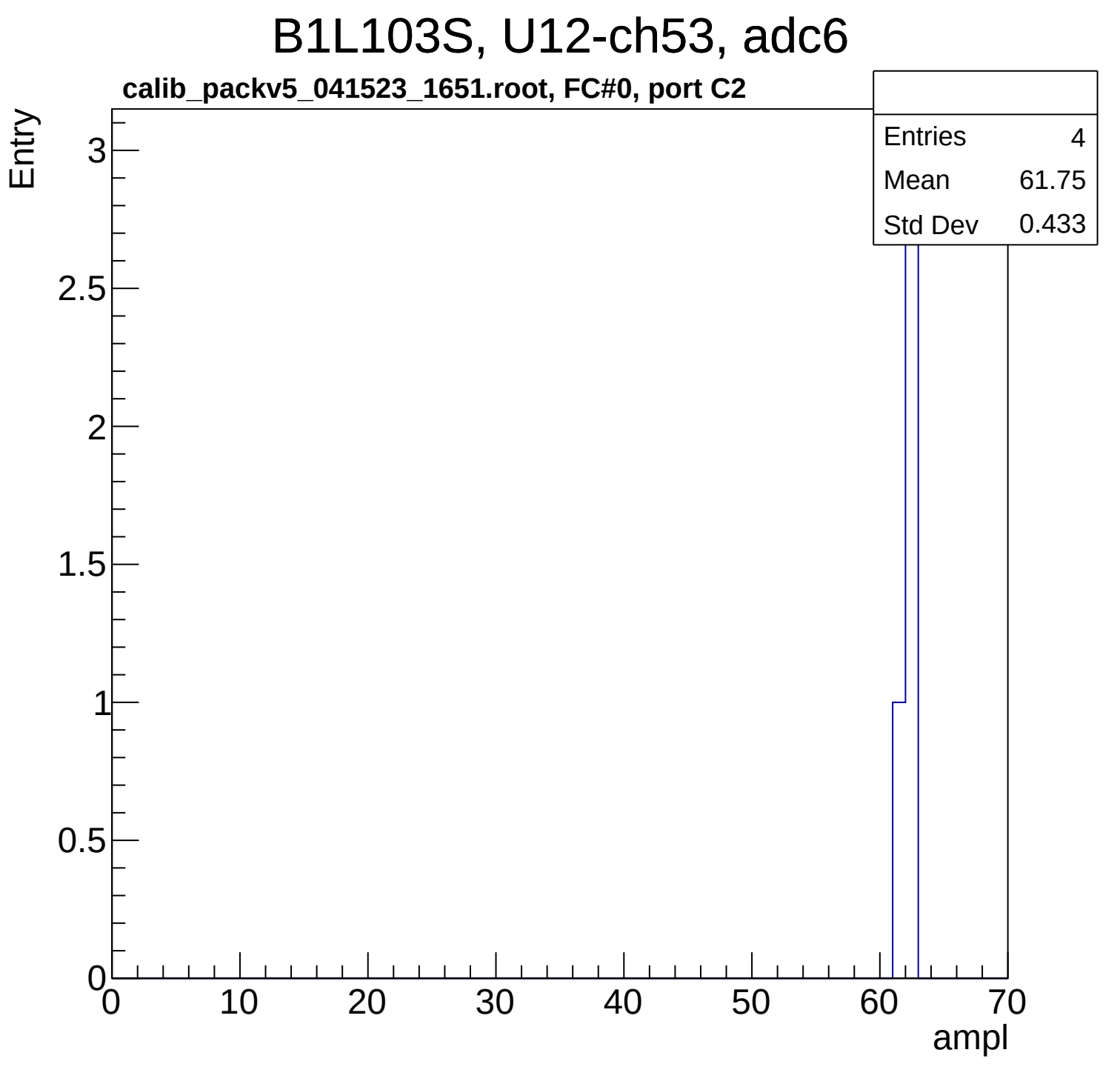
40
50
60
70


B1L103S, U12-ch53, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 60.38
Std Dev 2.466
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch53, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61.75
Std Dev 0.433
Entry
ampl
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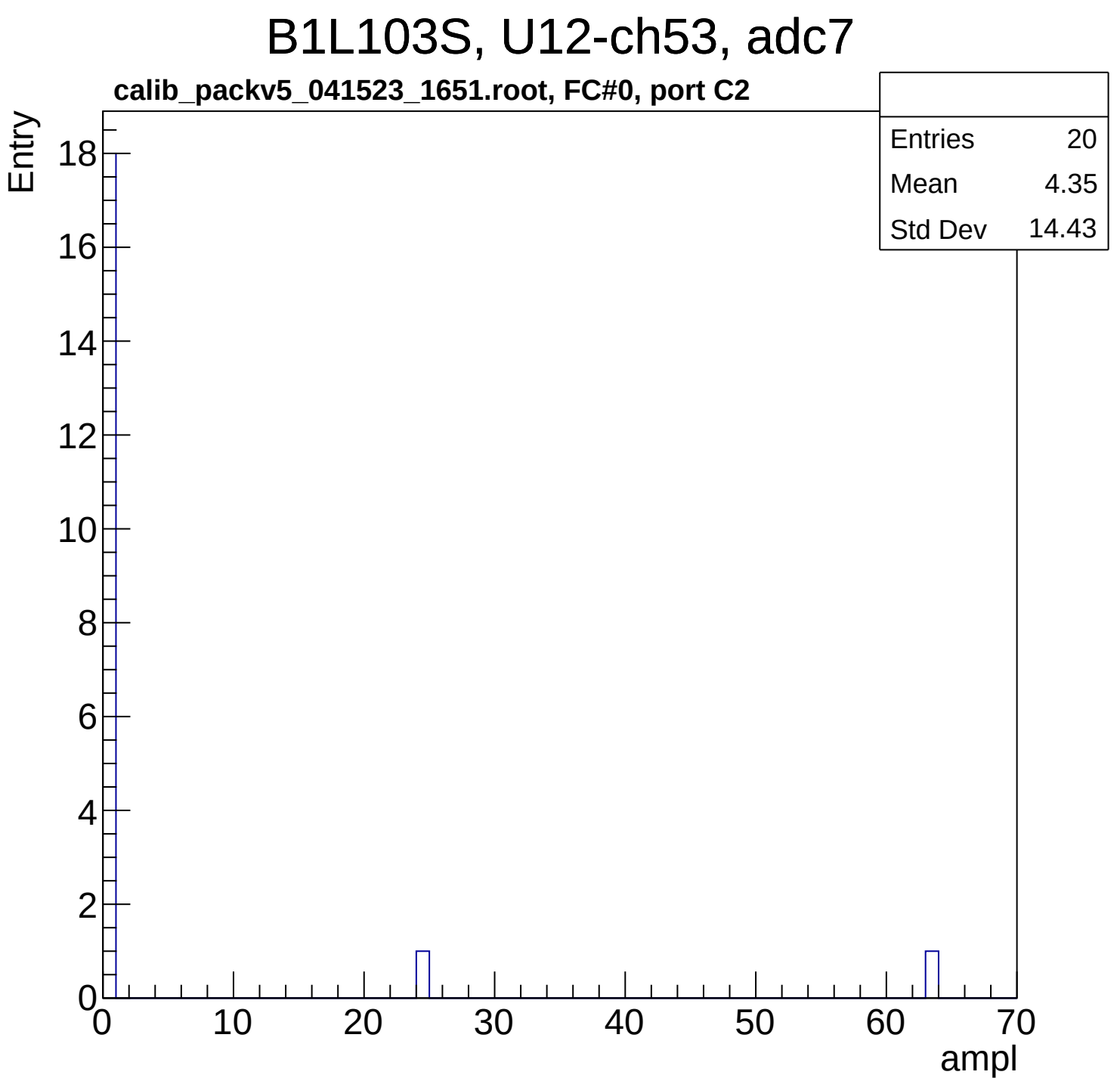
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U12-ch53, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.35
Std Dev 14.43
Entry
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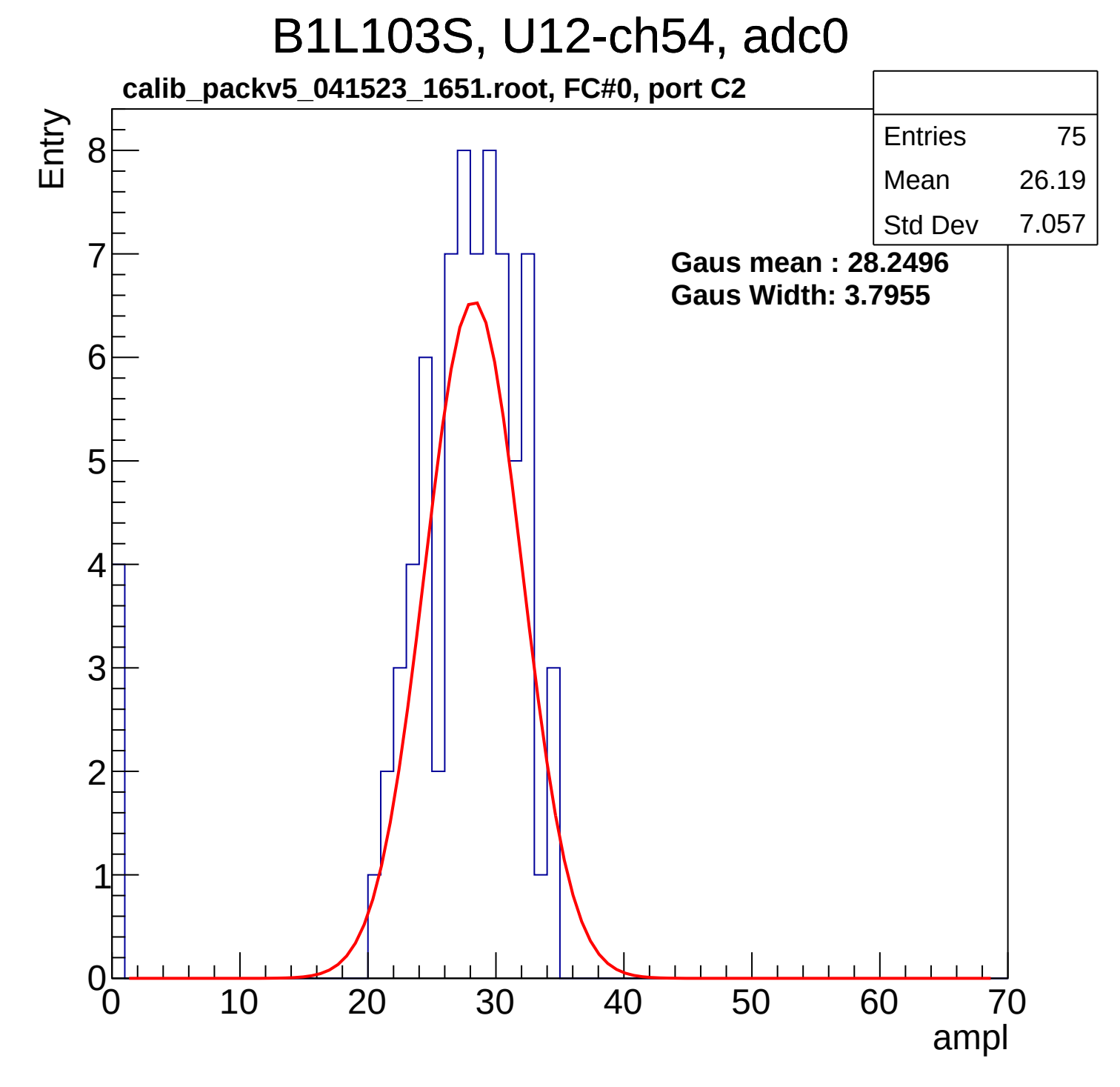
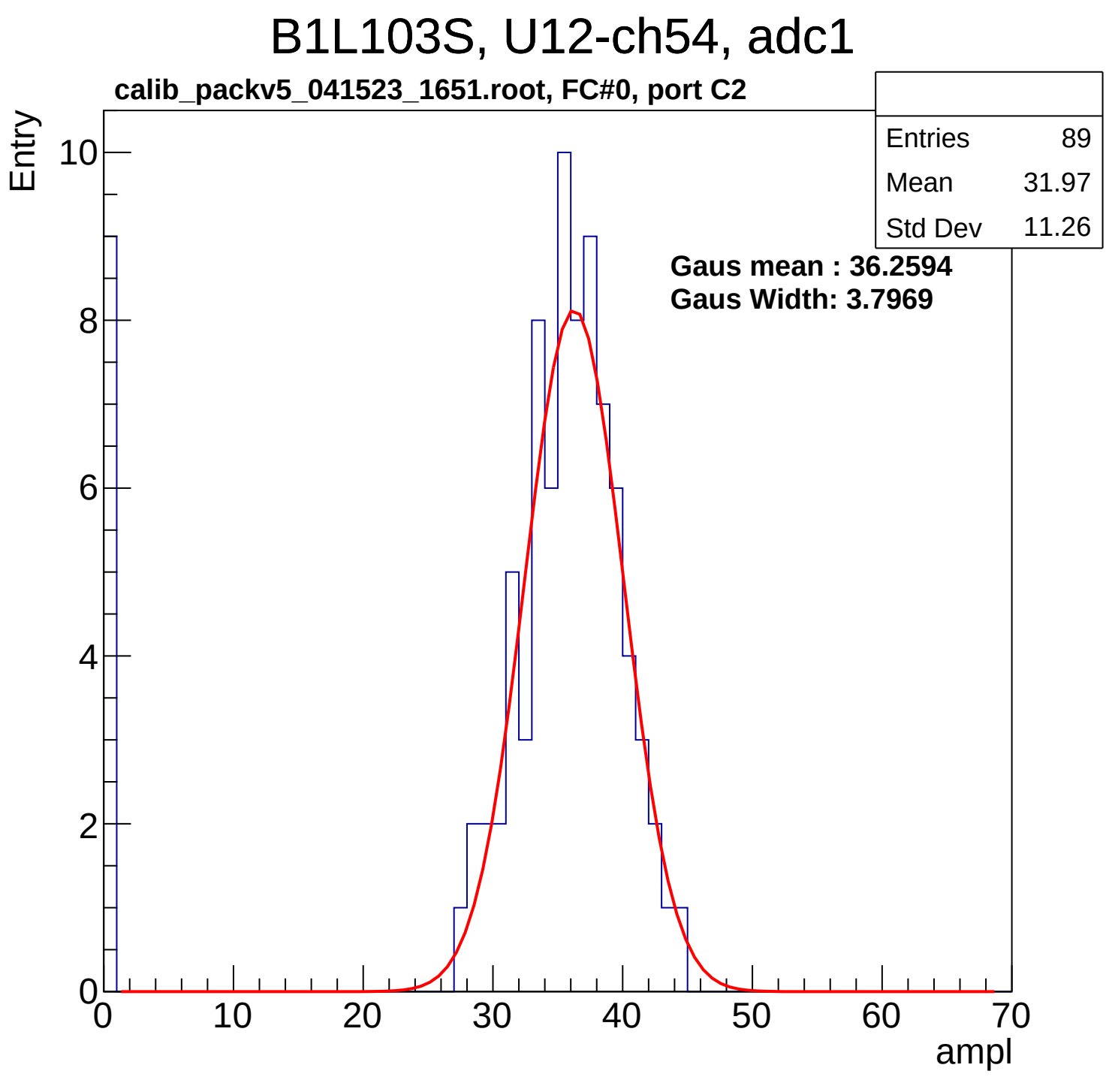
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch54, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 26.19
Std Dev 7.057
Gaus mean : 28.2496
Gaus Width: 3.7955
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U12-ch54, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 31.97
Std Dev 11.26
Gaus mean : 36.2594
Gaus Width: 3.7969
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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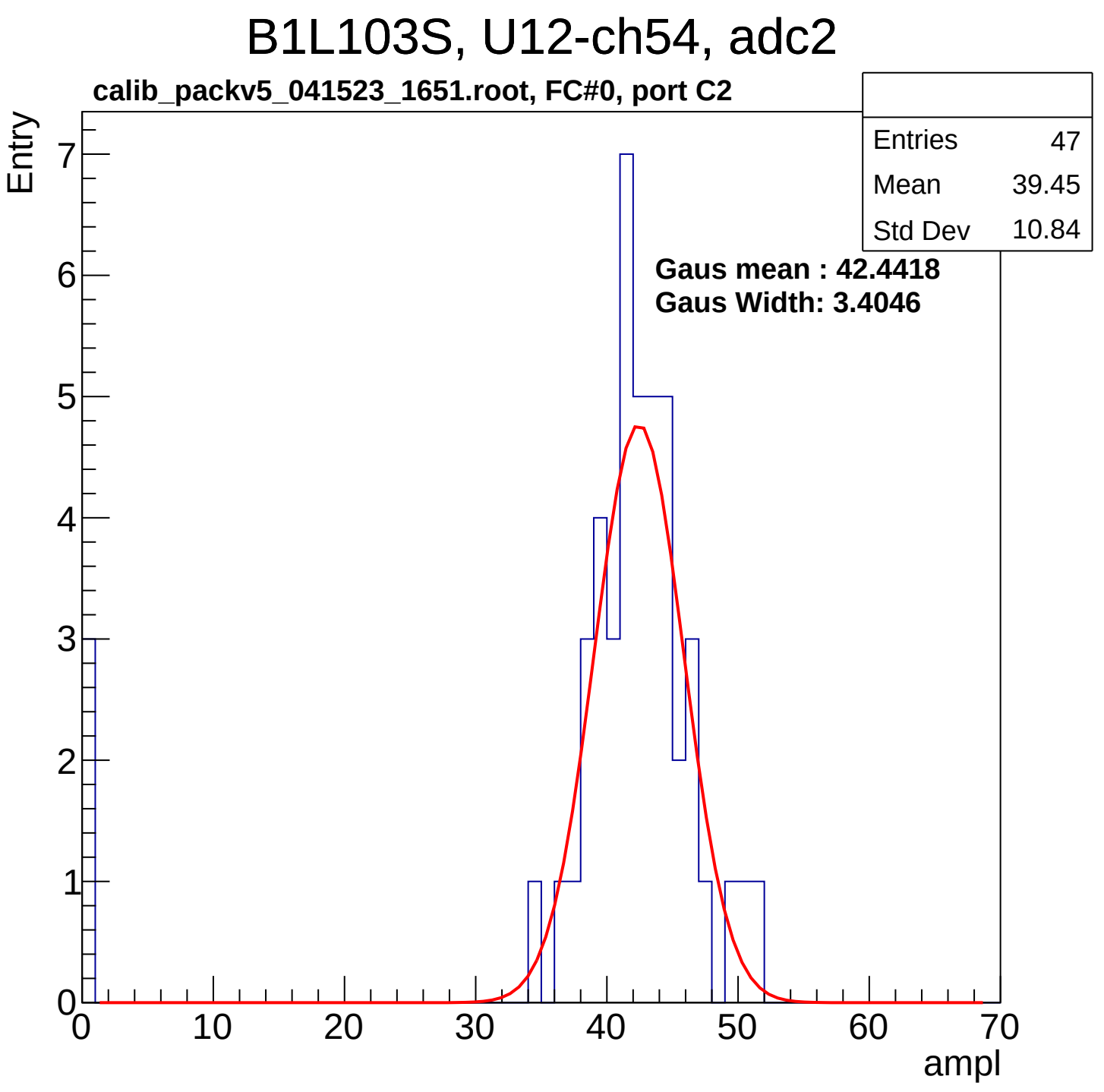
B1L103S, U12-ch54, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 39.45
Std Dev 10.84
Gaus mean : 42.4418
Gaus Width: 3.4046
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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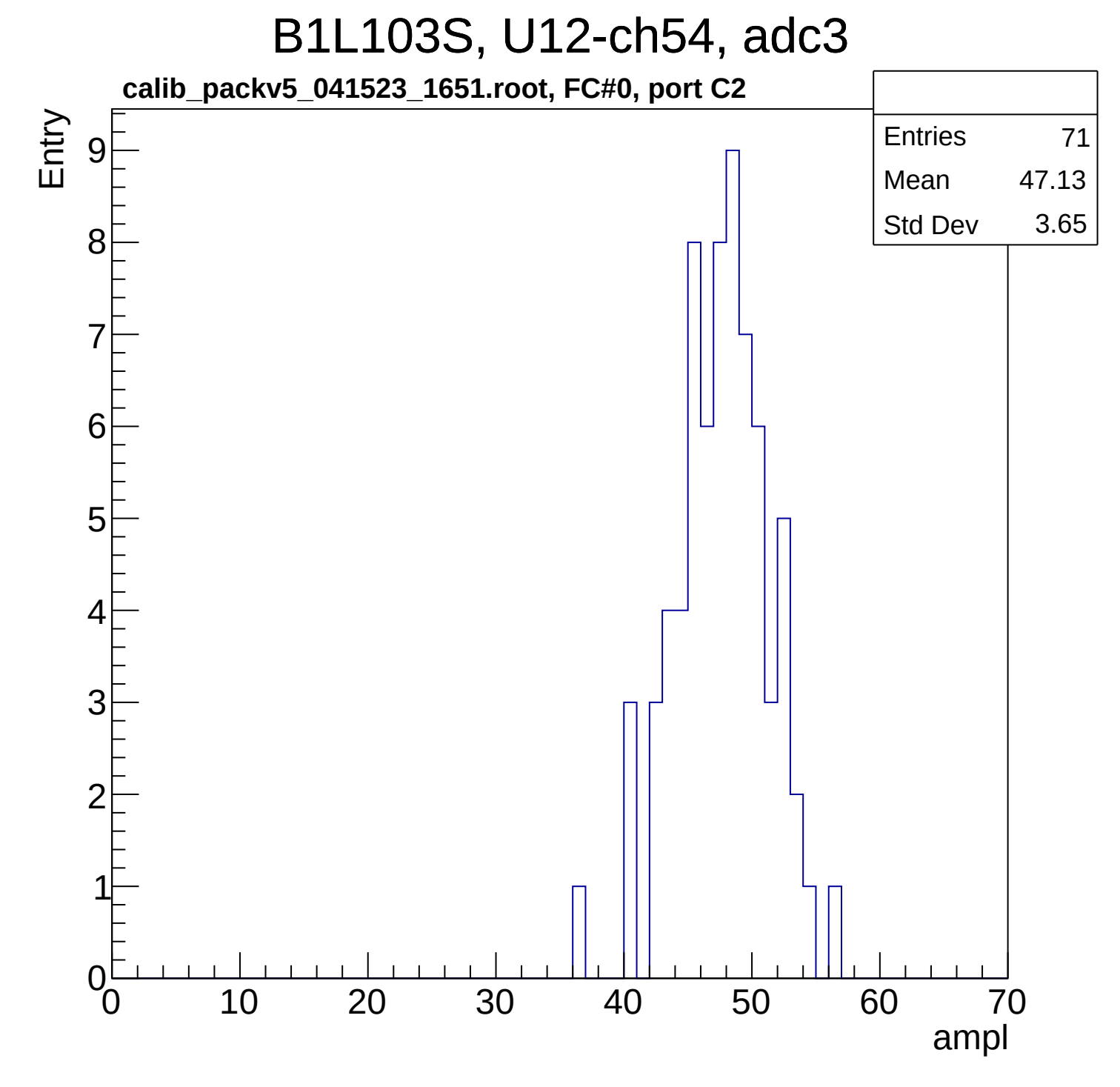
B1L103S, U12-ch54, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 47.13
Std Dev 3.65
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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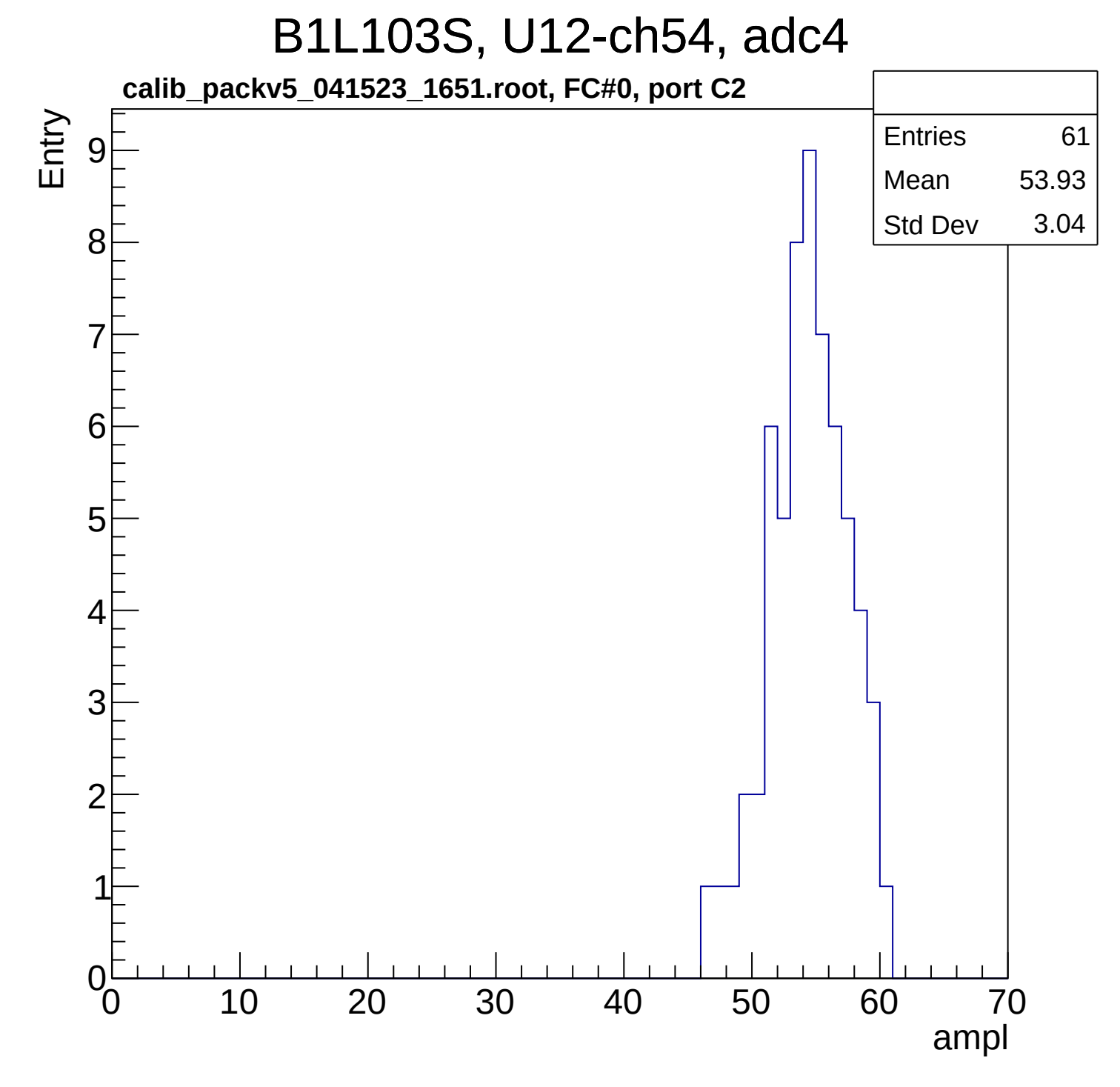
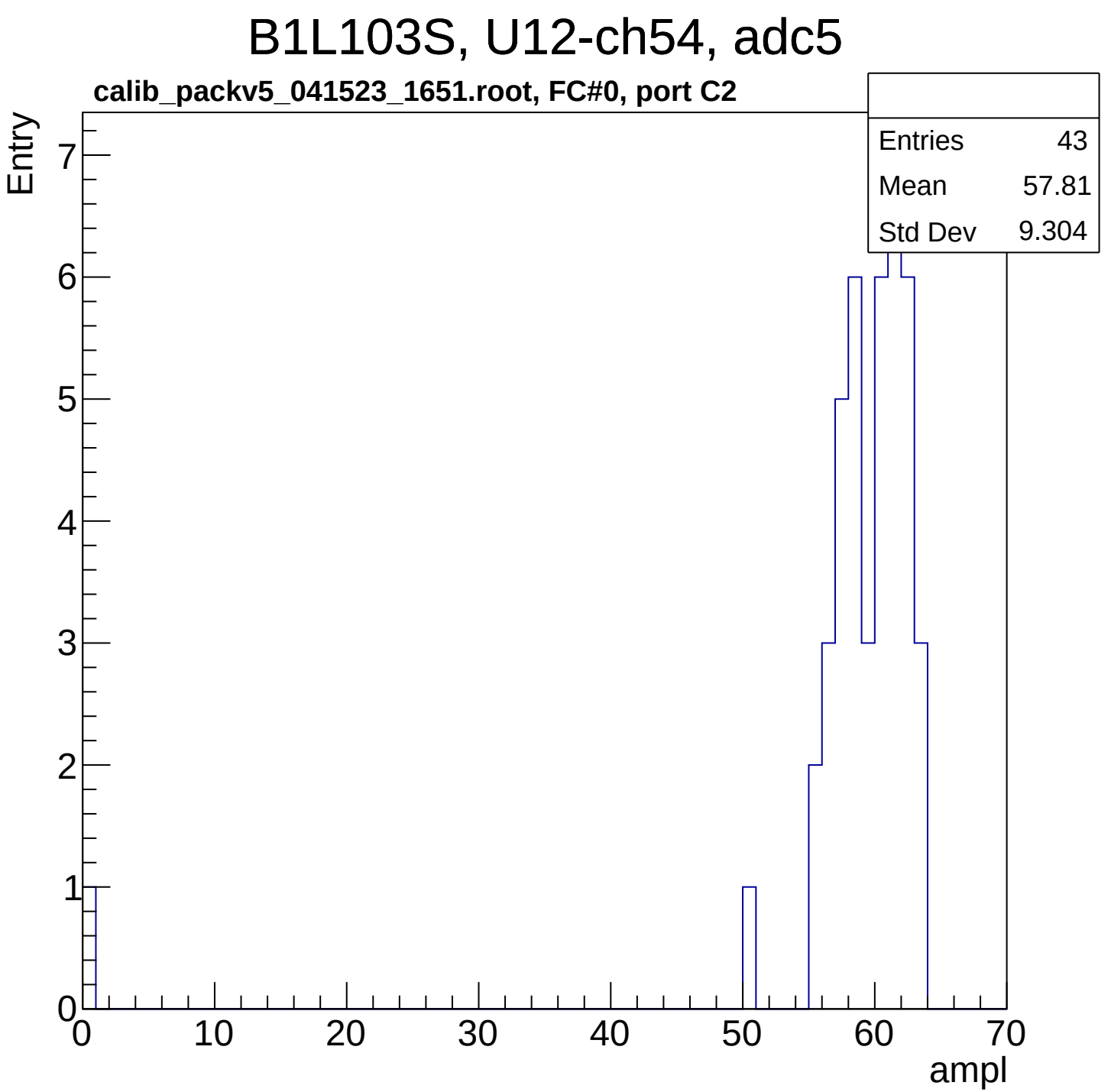
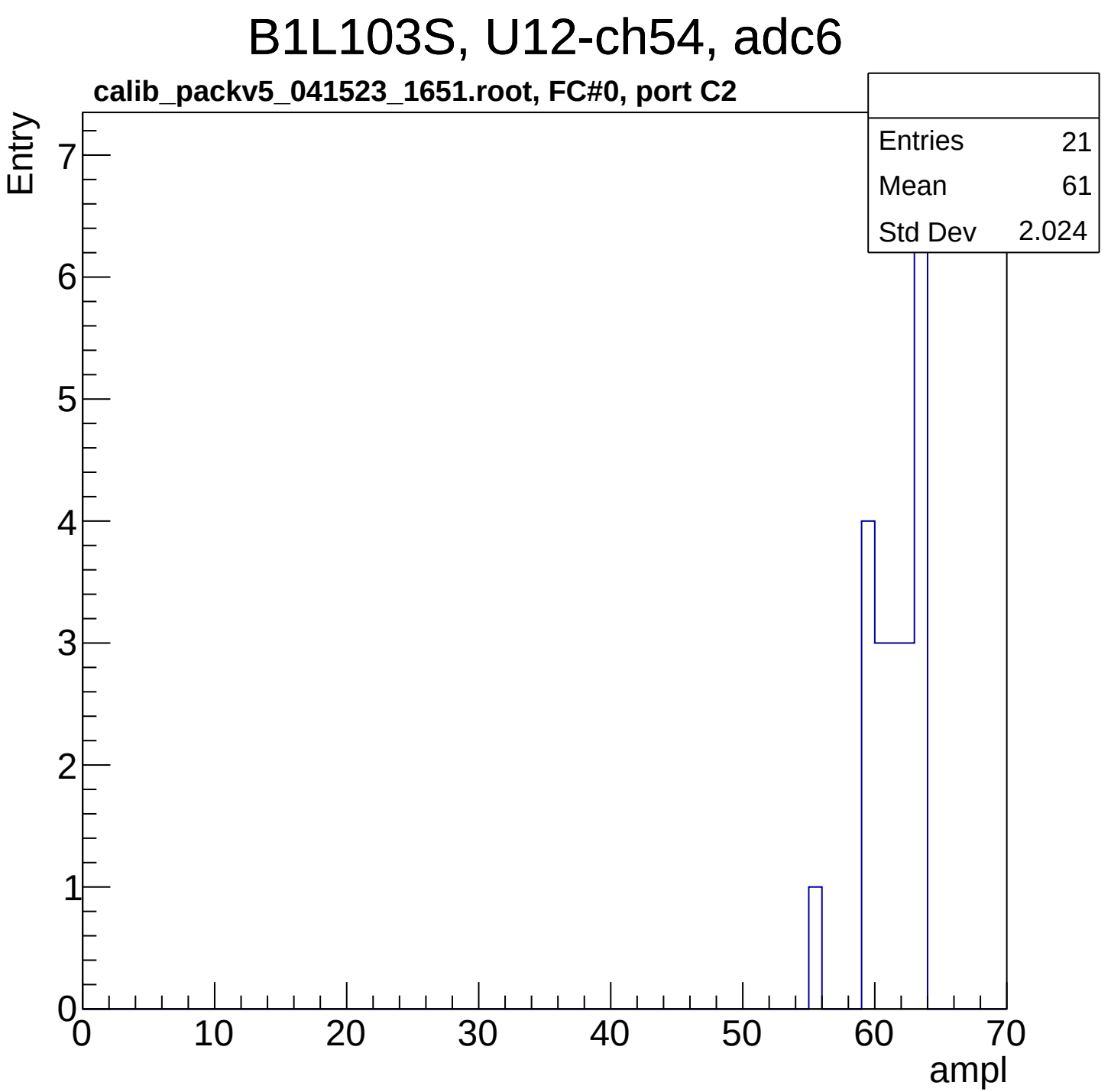
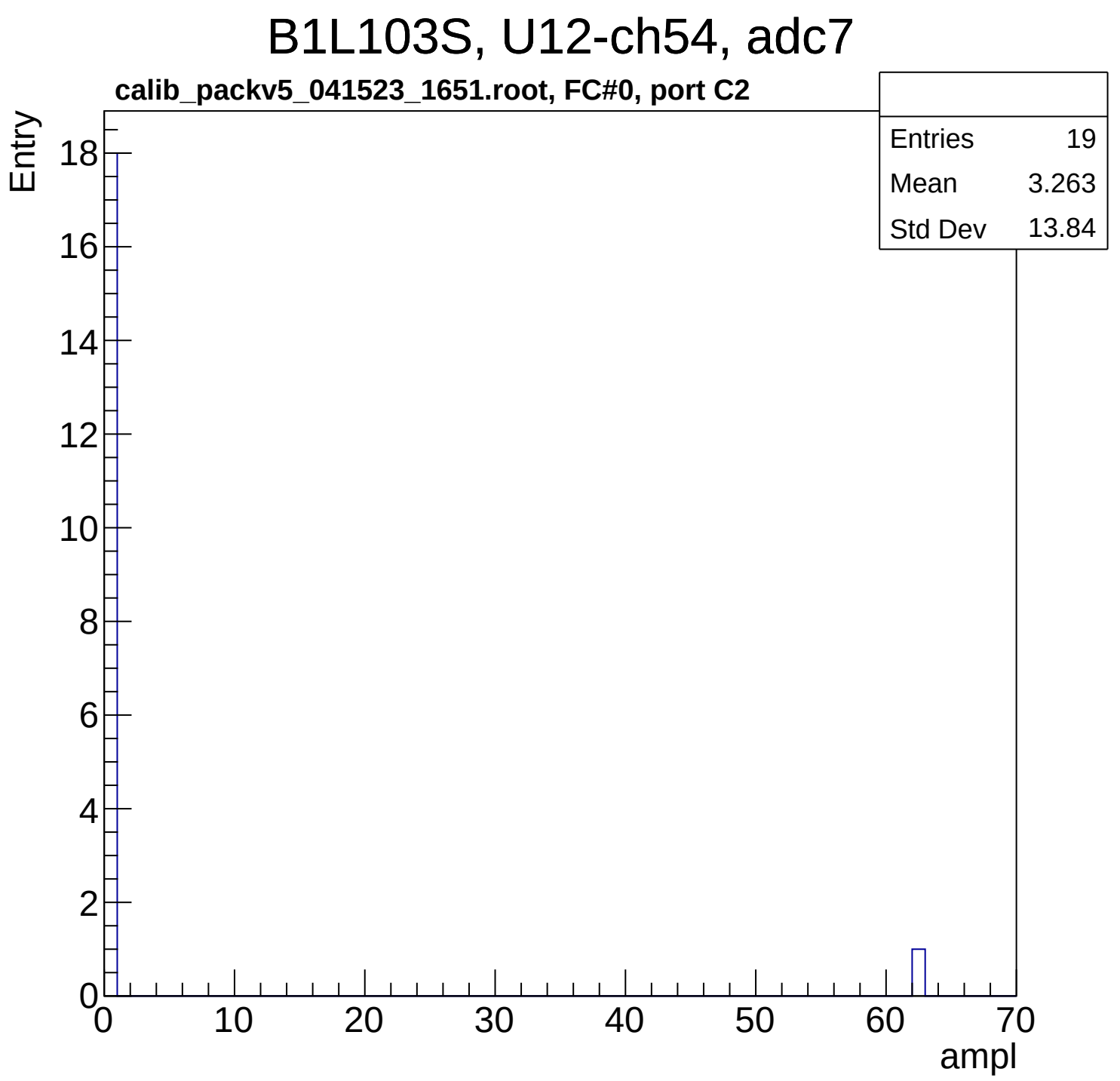

B1L103S, U12-ch54, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 53.93
Std Dev 3.04
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch54, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 57.81
Std Dev 9.304
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U12-ch54, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 61
Std Dev 2.024
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch54, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.263
Std Dev 13.84
Entry
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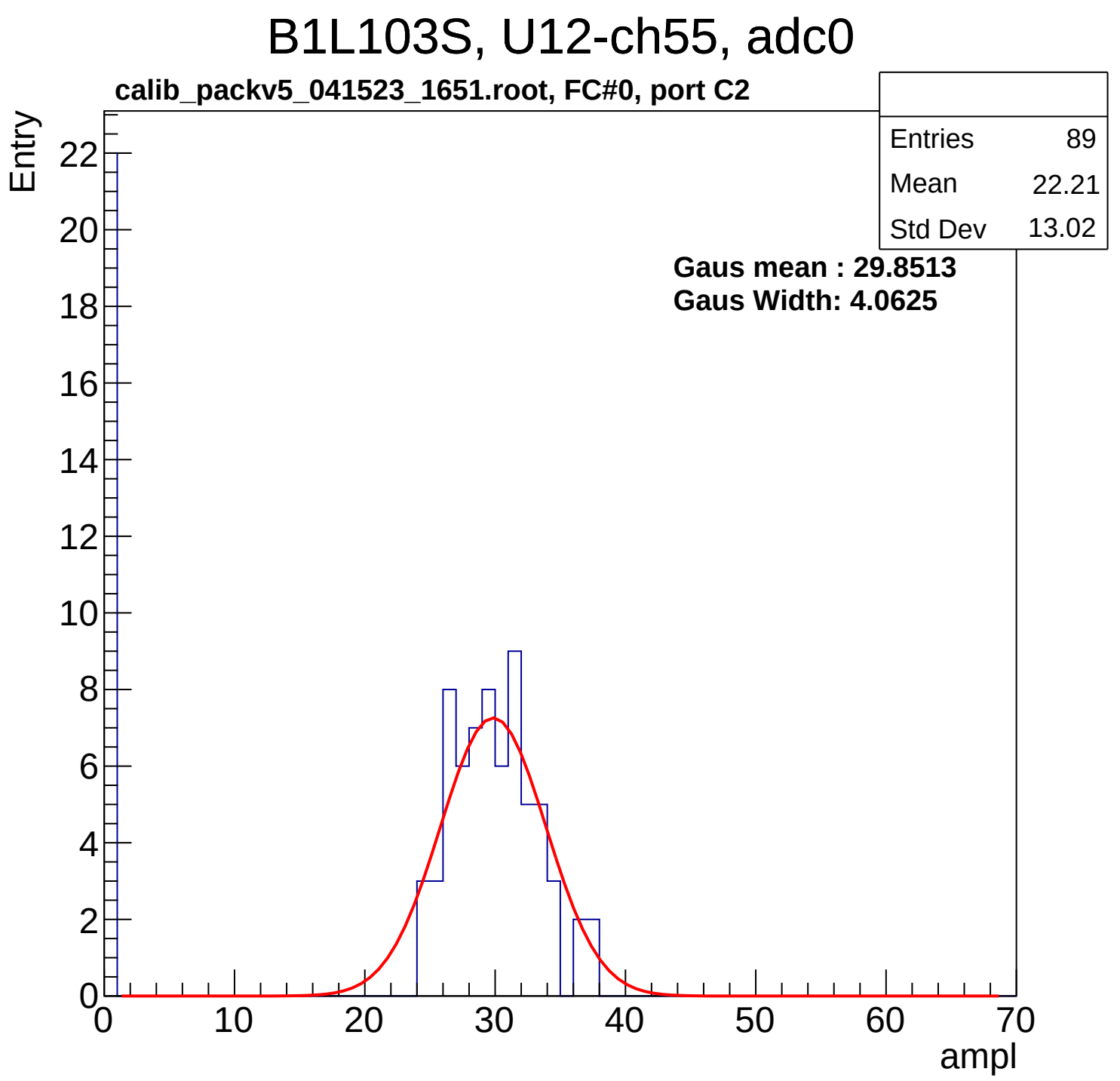
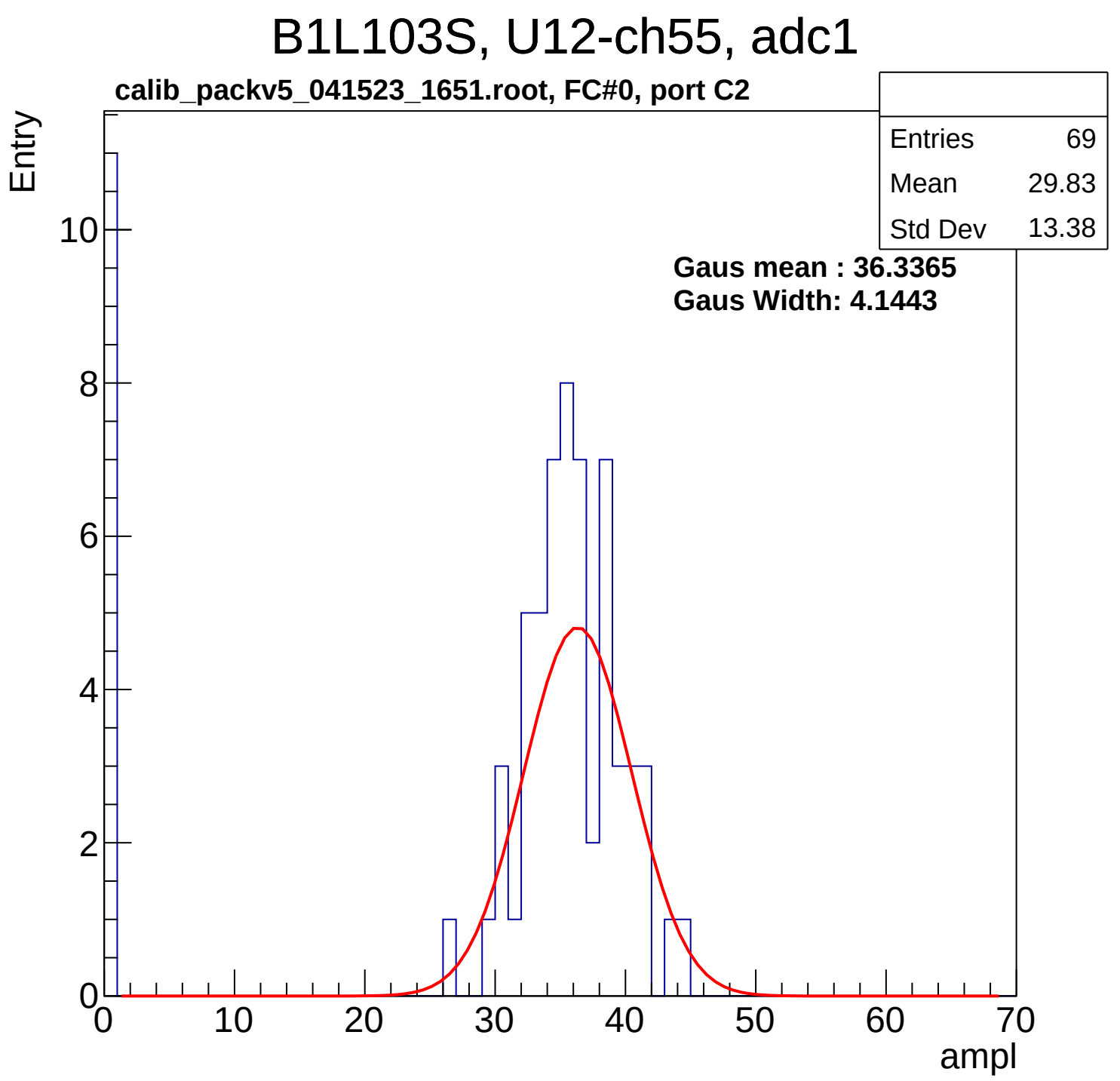
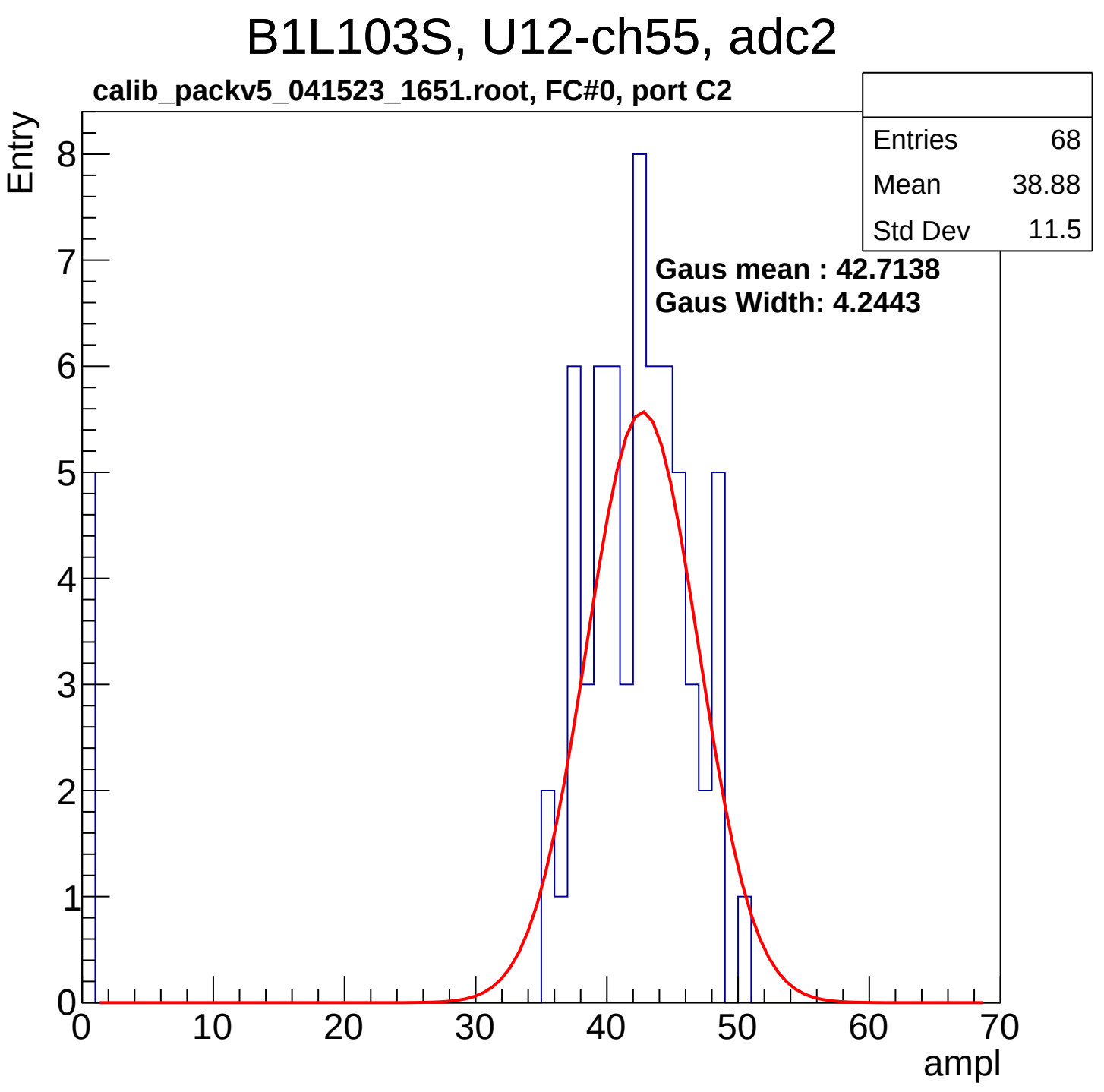
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch55, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 22.21
Std Dev 13.02
Gaus mean : 29.8513
Gaus Width: 4.0625
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U12-ch55, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 29.83
Std Dev 13.38
Gaus mean : 36.3365
Gaus Width: 4.1443
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch55, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 38.88
Std Dev 11.5
Gaus mean : 42.7138
Gaus Width: 4.2443
Entry
ampl
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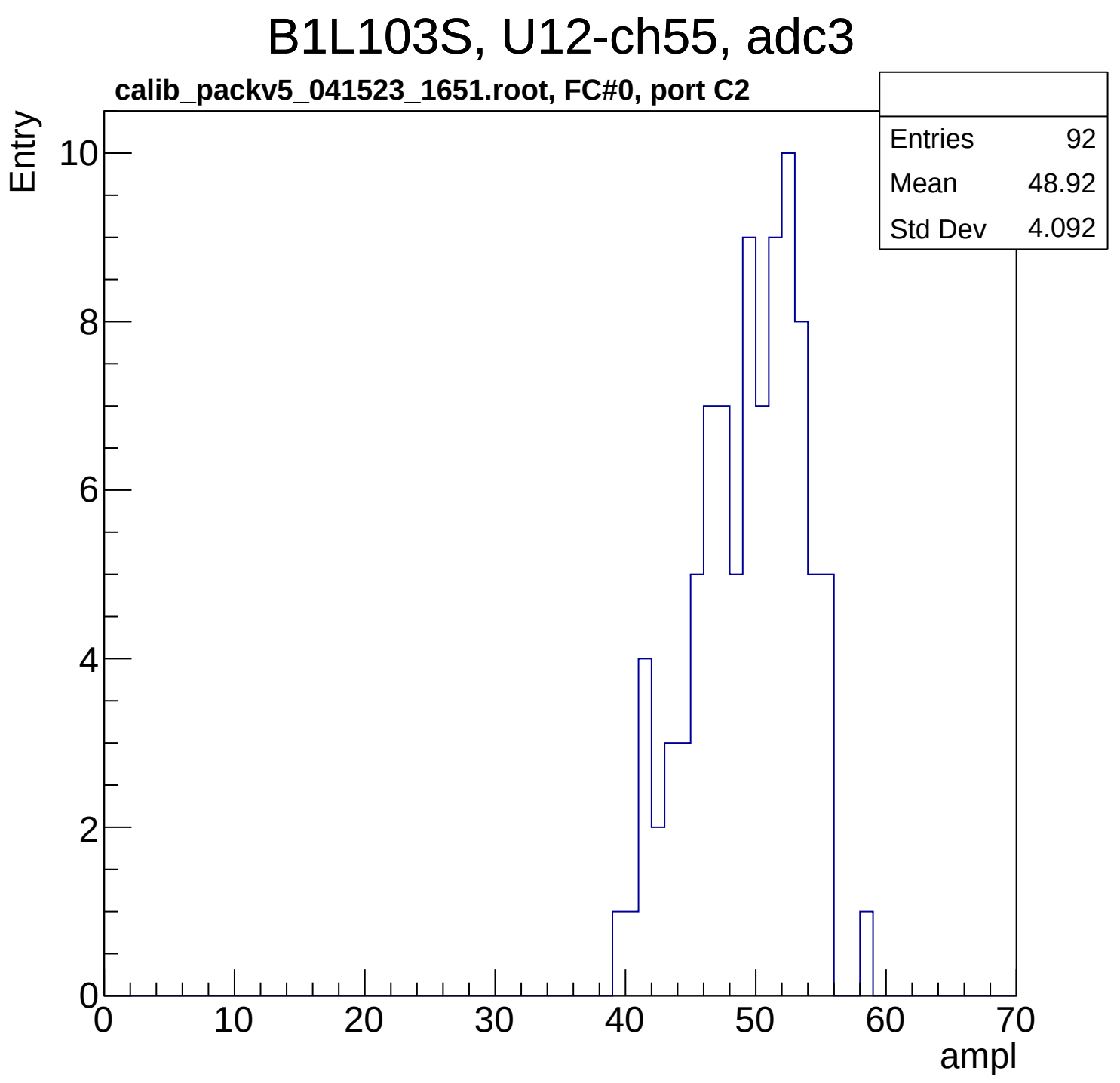
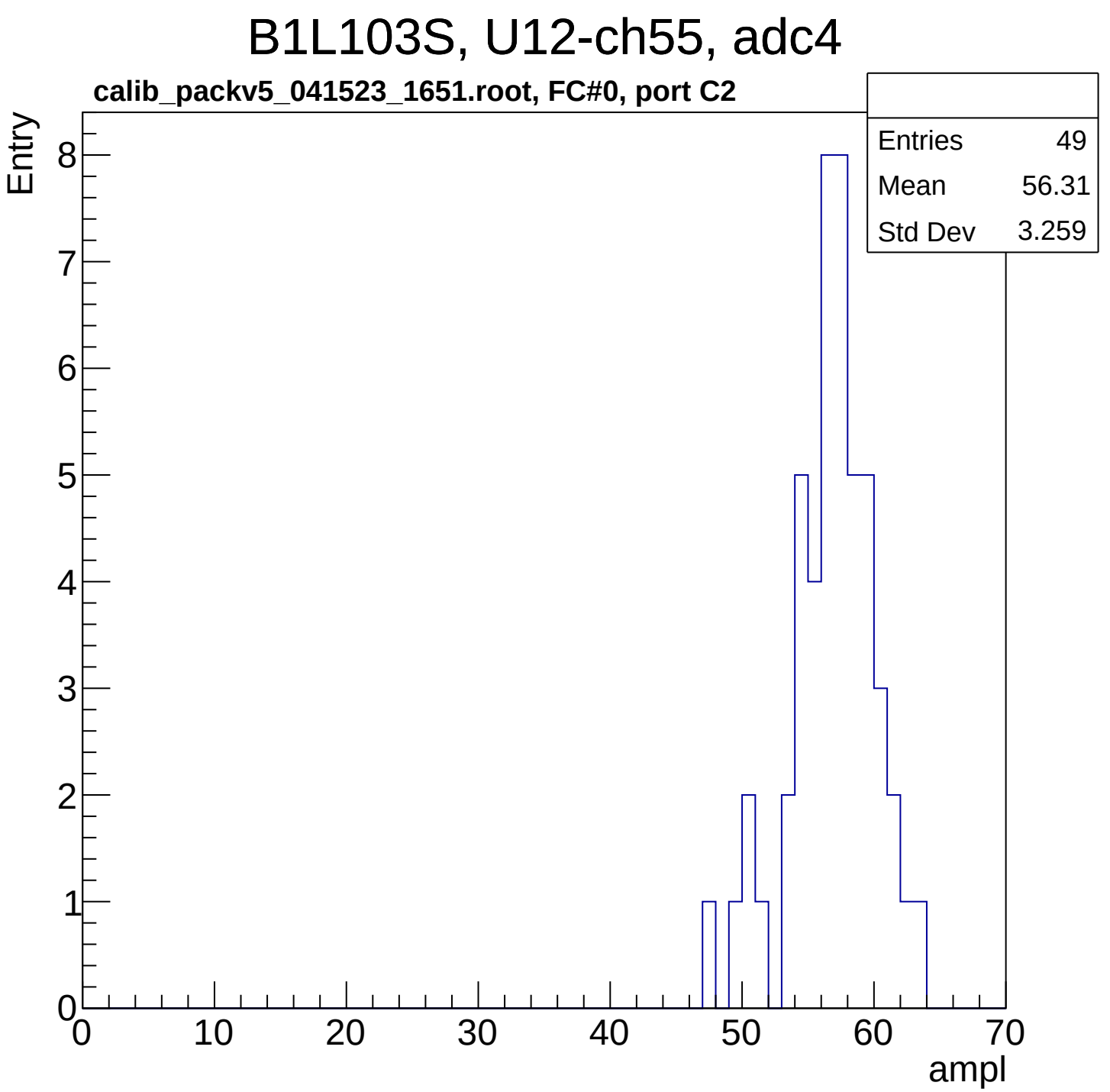
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U12-ch55, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 48.92
Std Dev 4.092
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch55, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 56.31
Std Dev 3.259
Entry
ampl
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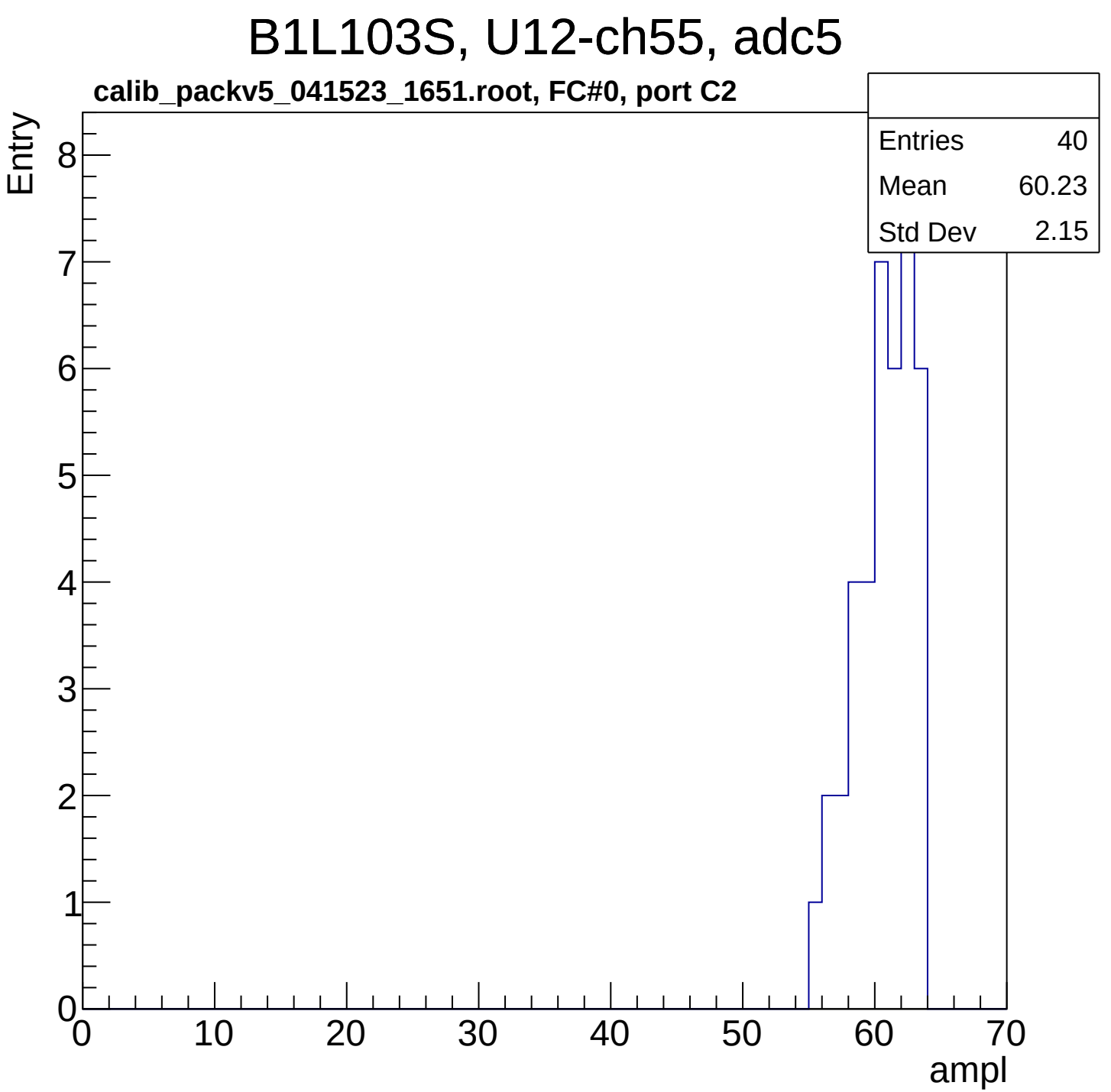
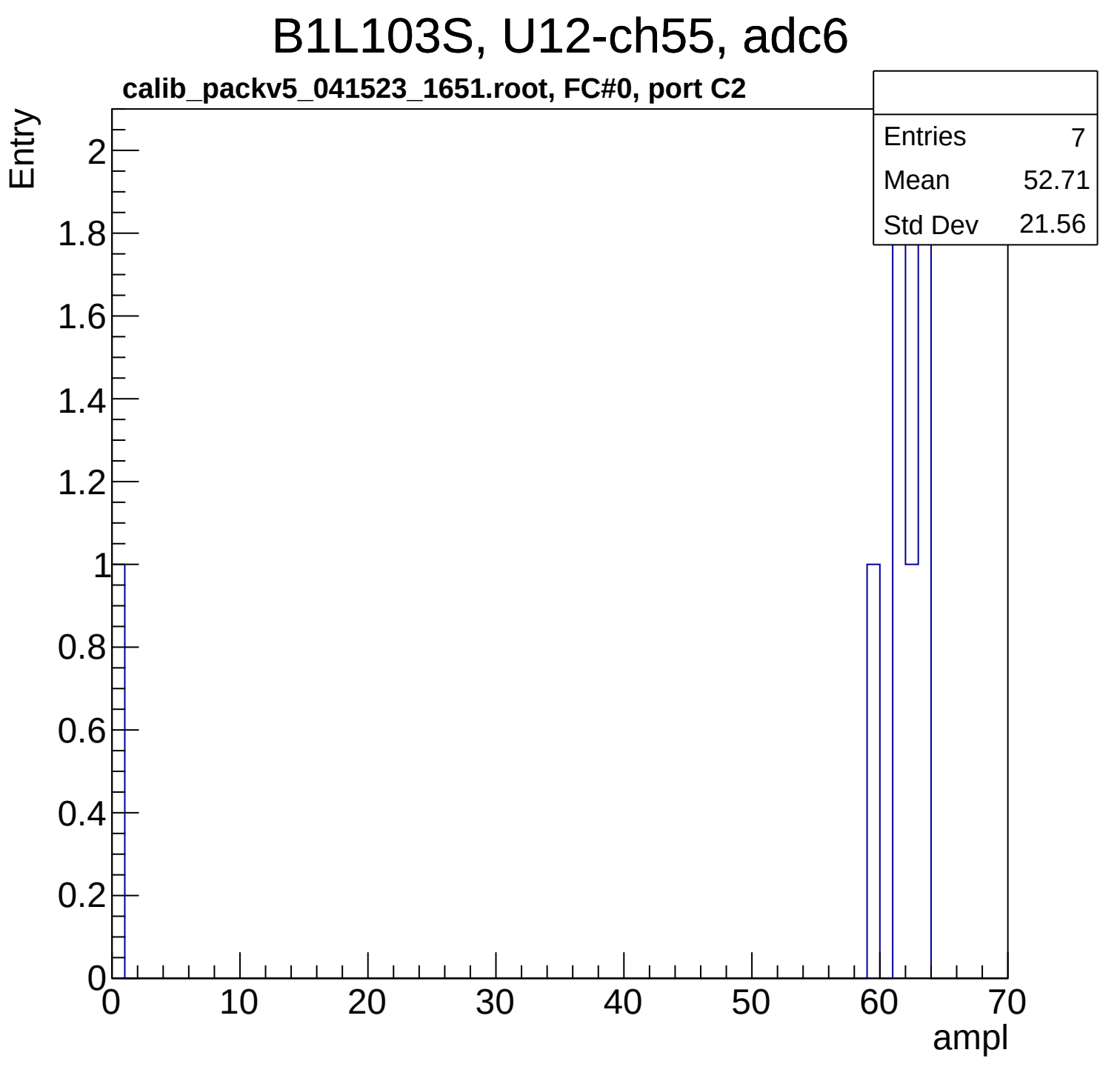
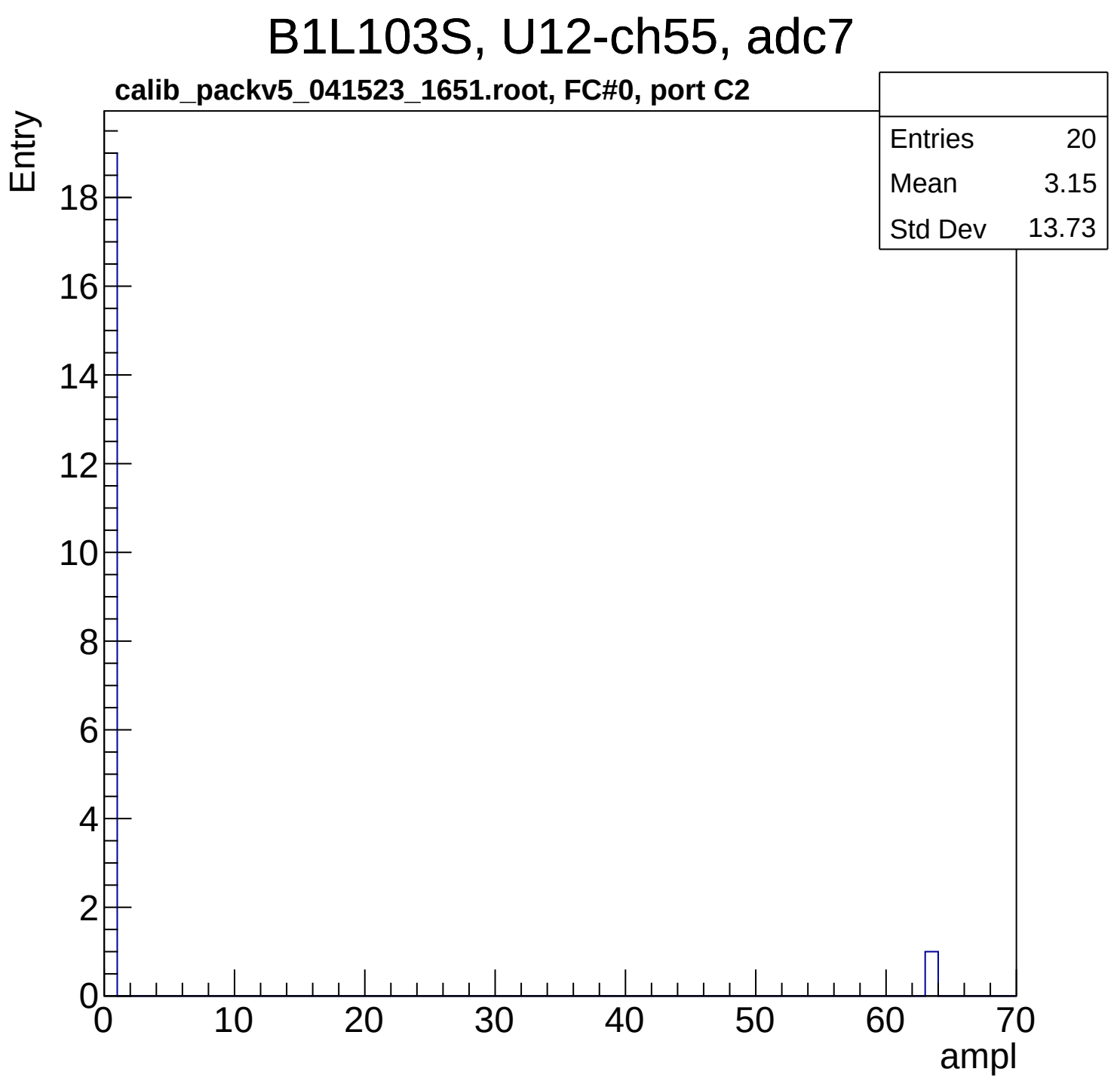
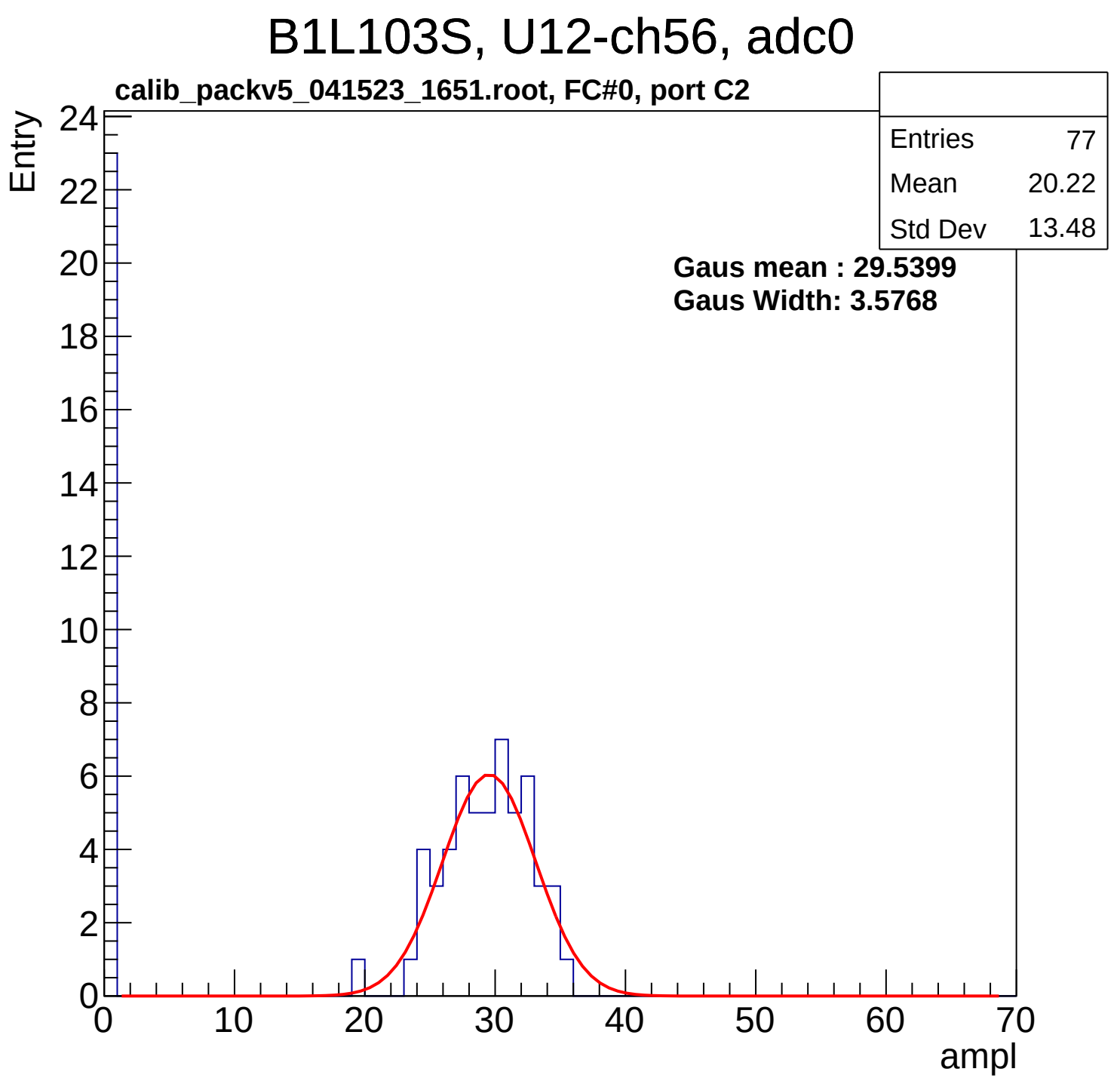
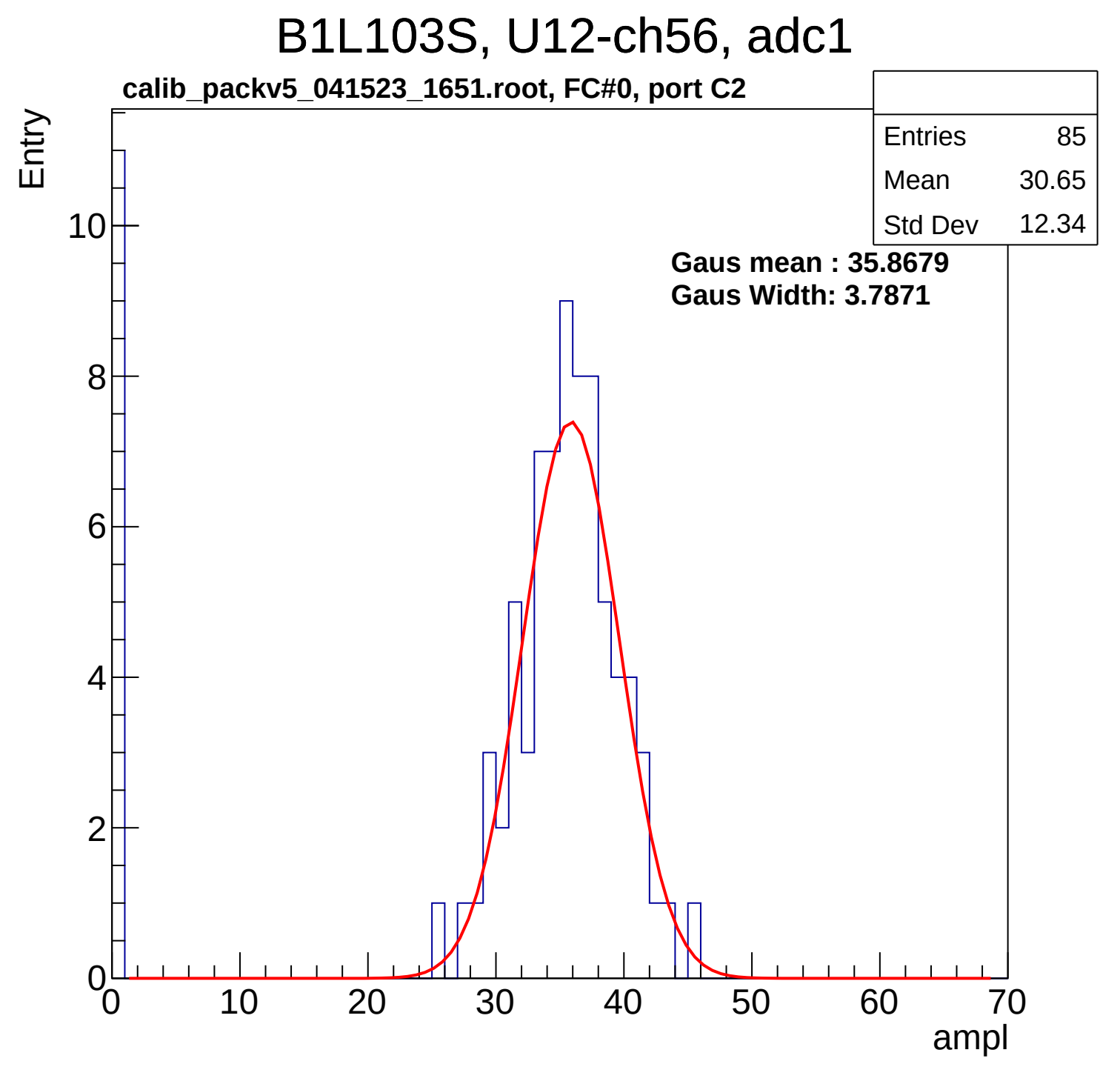
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

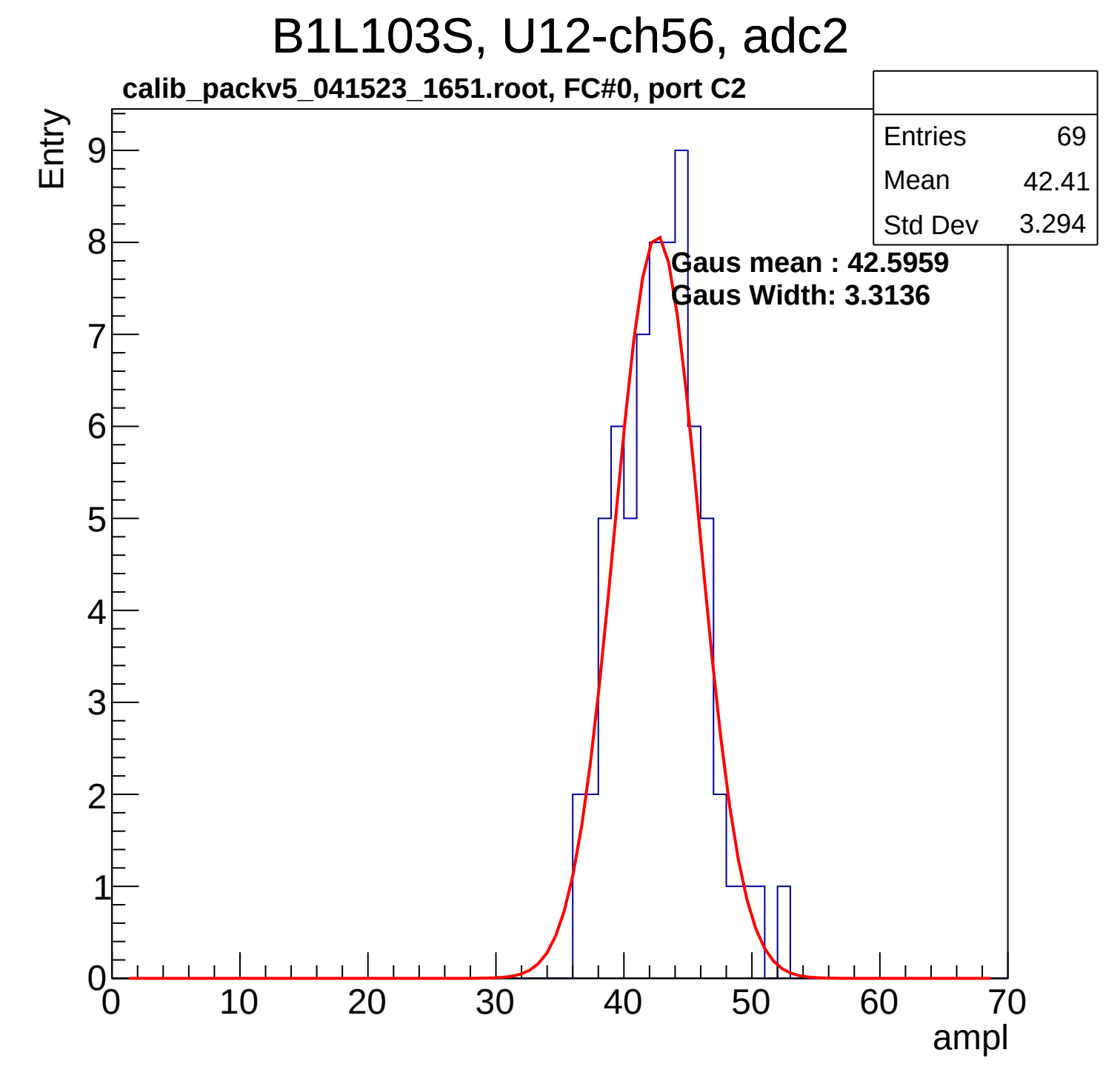

B1L103S, U12-ch55, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 60.23
Std Dev 2.15
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U12-ch55, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 52.71
Std Dev 21.56
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U12-ch55, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch56, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 20.22
Std Dev 13.48
Gaus mean : 29.5399
Gaus Width: 3.5768
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
24
0
10
20
30
40
50
60
70


B1L103S, U12-ch56, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 30.65
Std Dev 12.34
Gaus mean : 35.8679
Gaus Width: 3.7871
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch56, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 42.41
Std Dev 3.294
Gaus mean : 42.5959
Gaus Width: 3.3136
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
50
60
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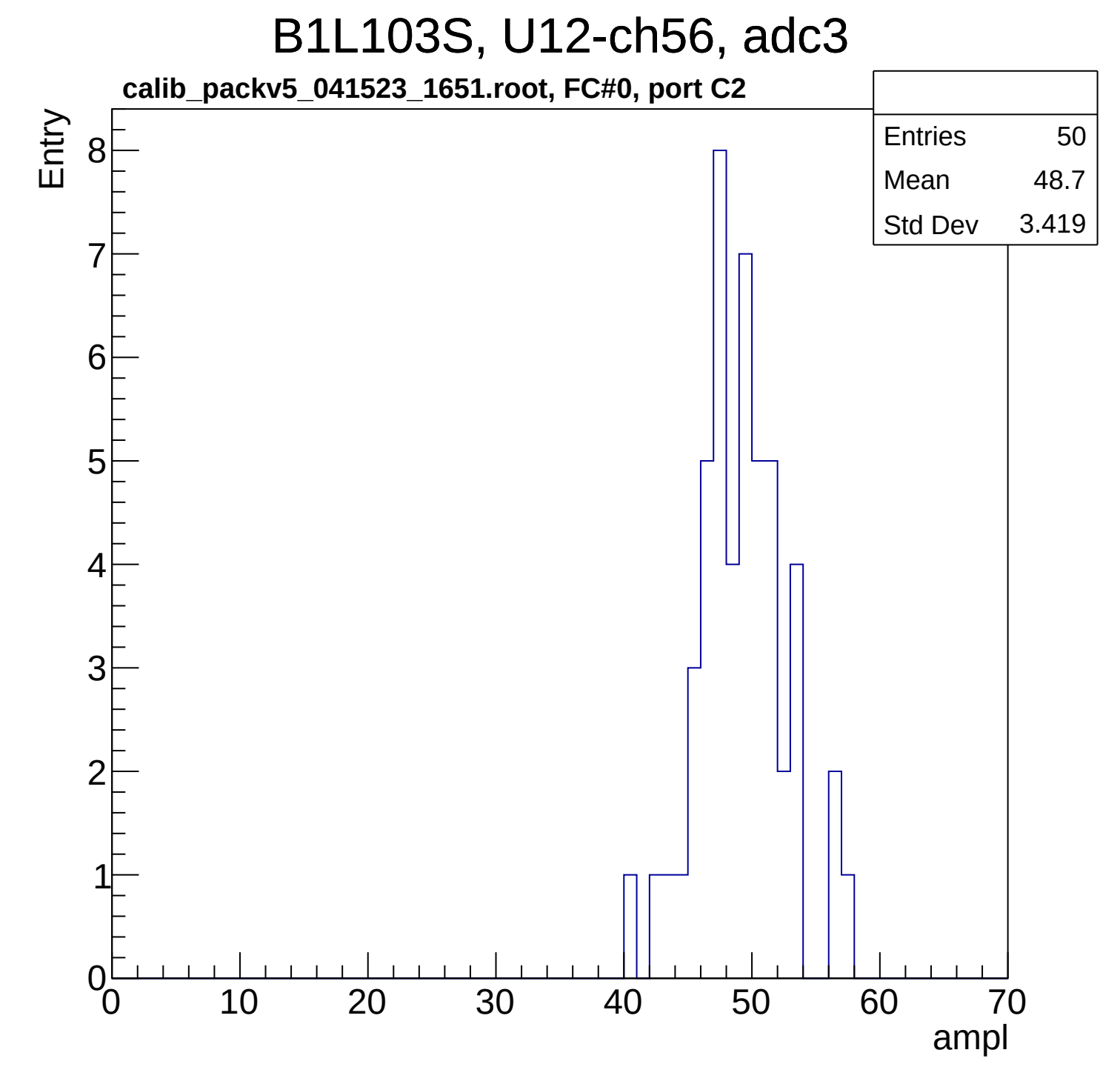
B1L103S, U12-ch56, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 48.7
Std Dev 3.419
Entry
ampl
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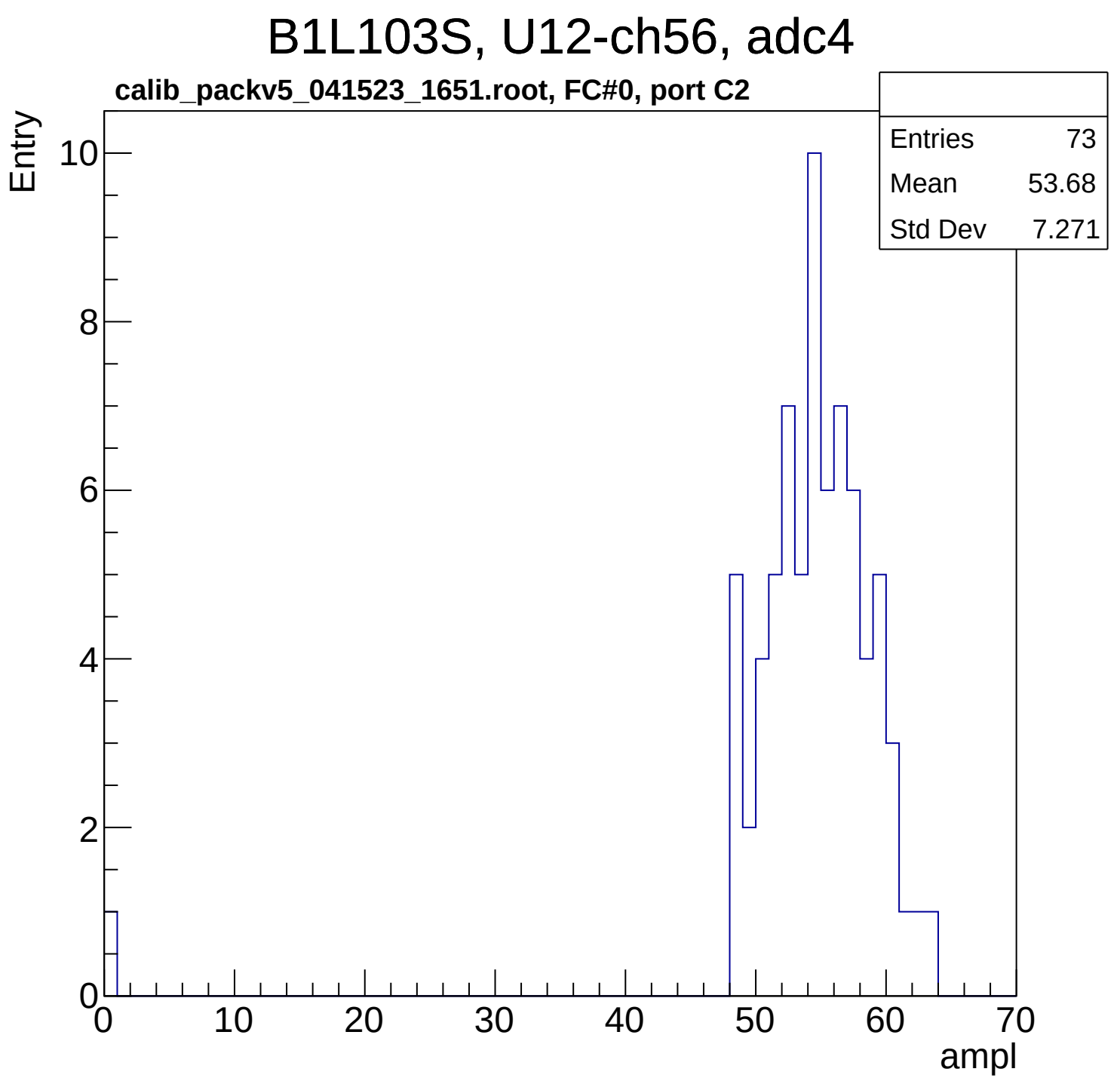
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U12-ch56, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 53.68
Std Dev 7.271
Entry
ampl
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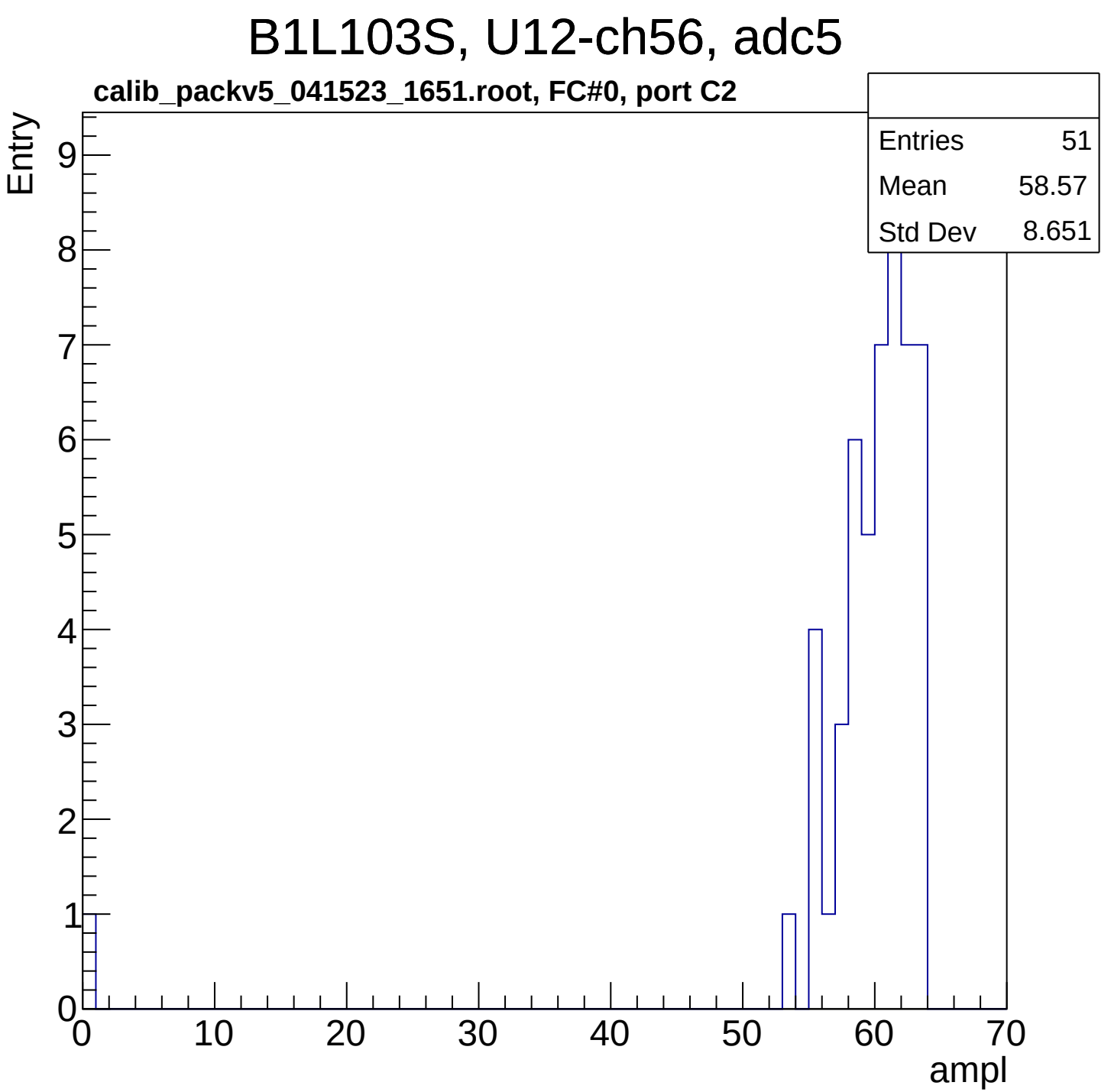
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch56, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.57
Std Dev 8.651
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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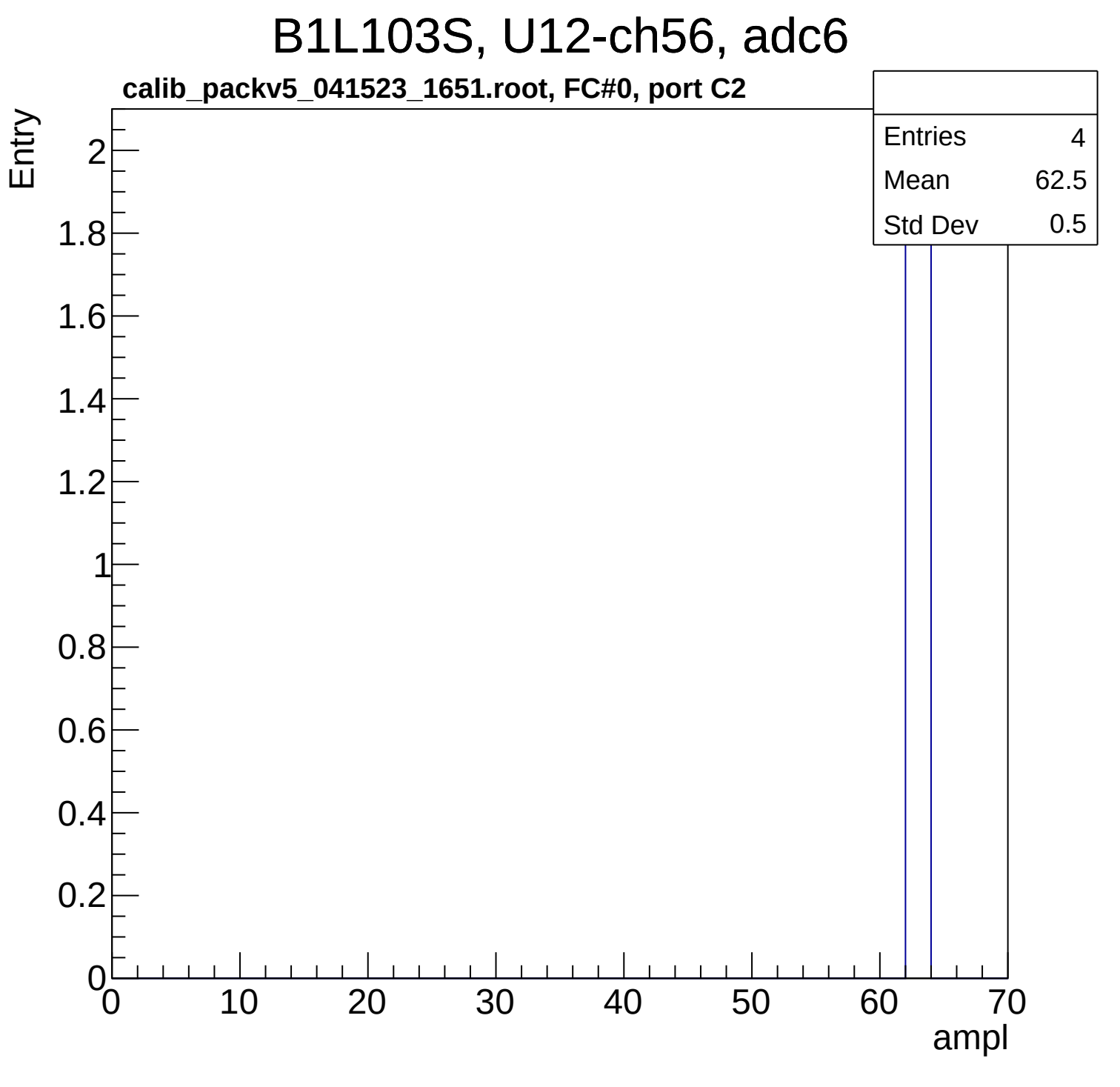
60
70


B1L103S, U12-ch56, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.5
Std Dev 0.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
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40
50
60
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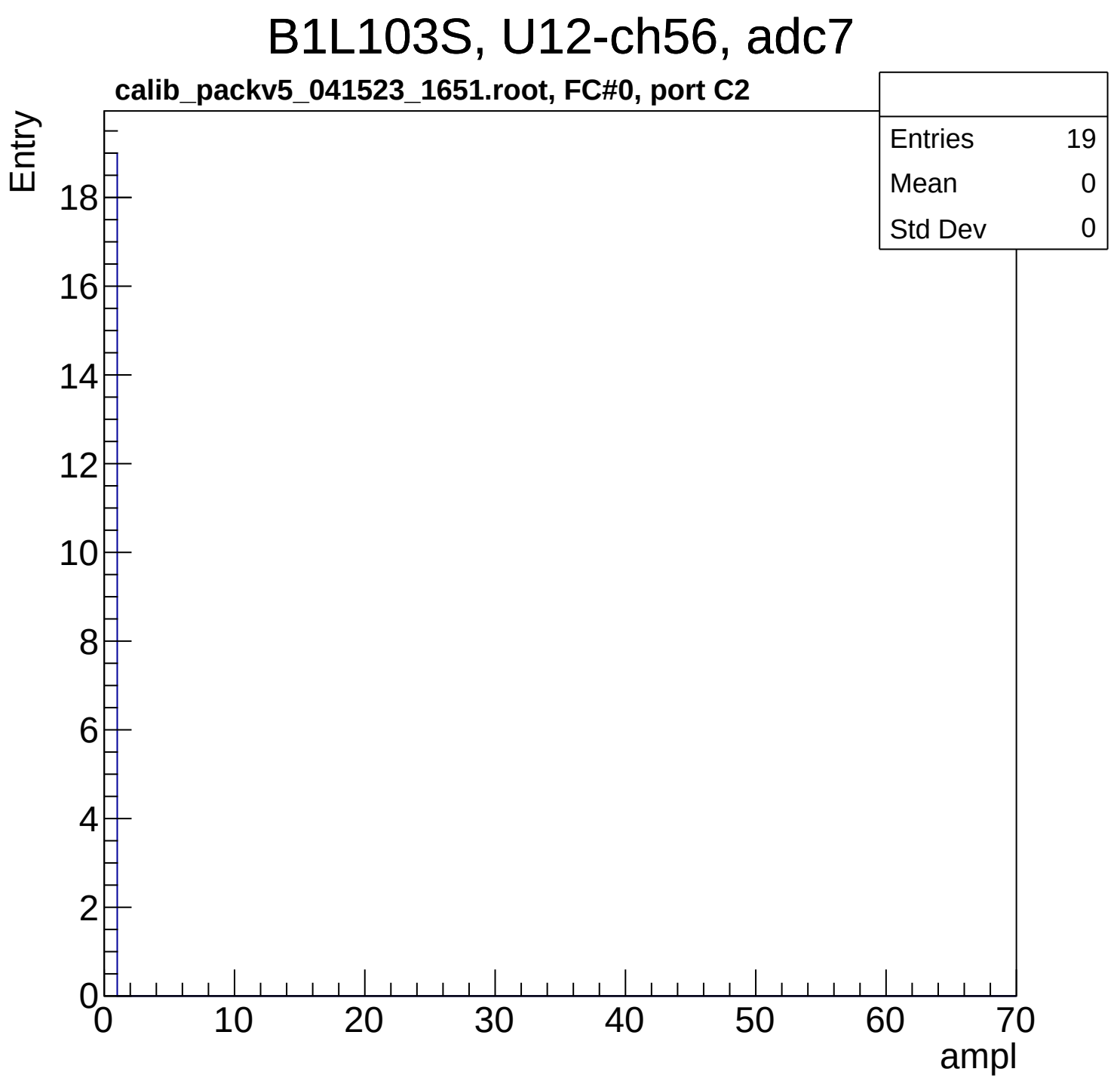
B1L103S, U12-ch56, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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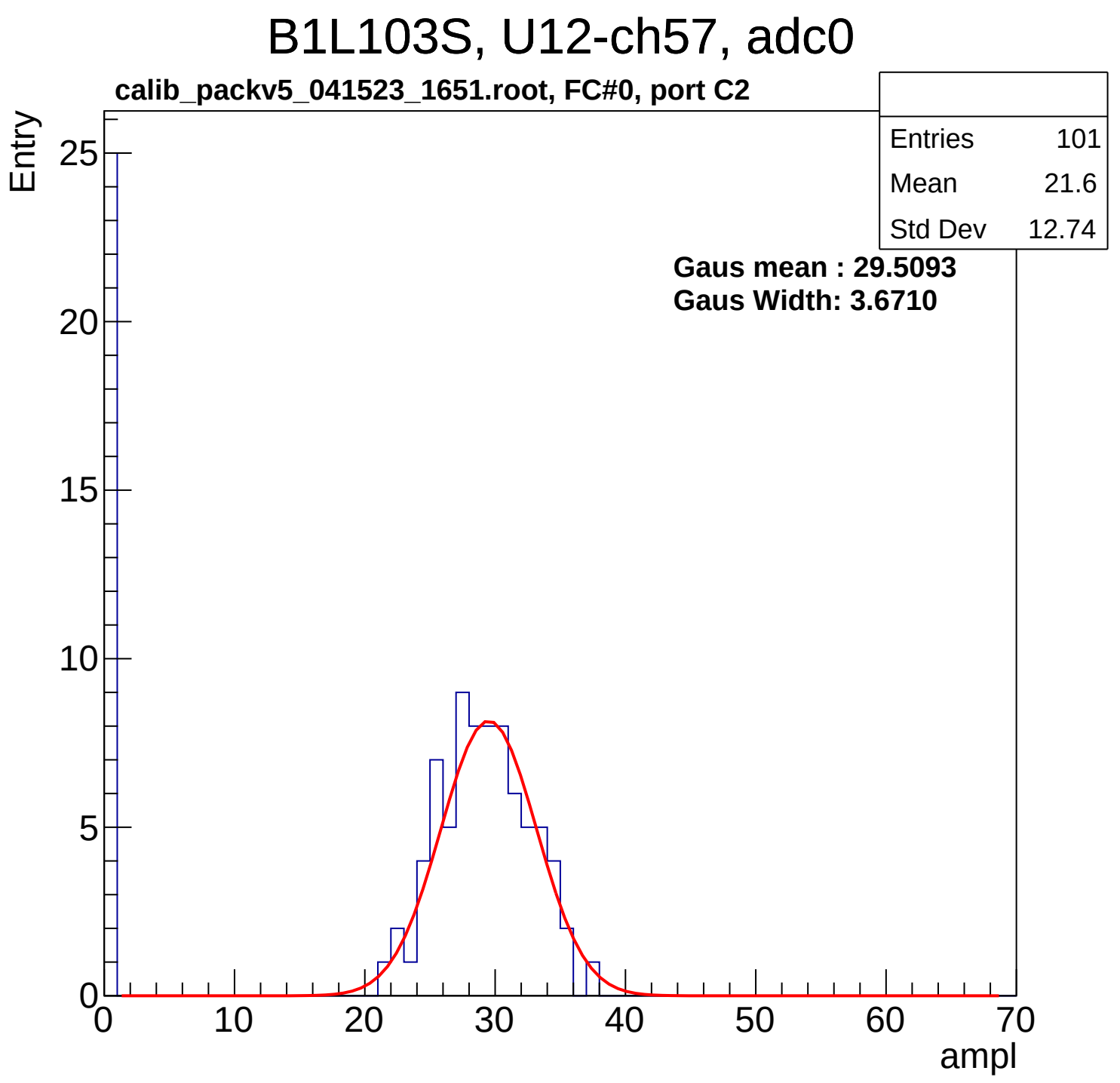
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch57, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 21.6
Std Dev 12.74
Gaus mean : 29.5093
Gaus Width: 3.6710
Entry
ampl
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5
10
15
20
25
0
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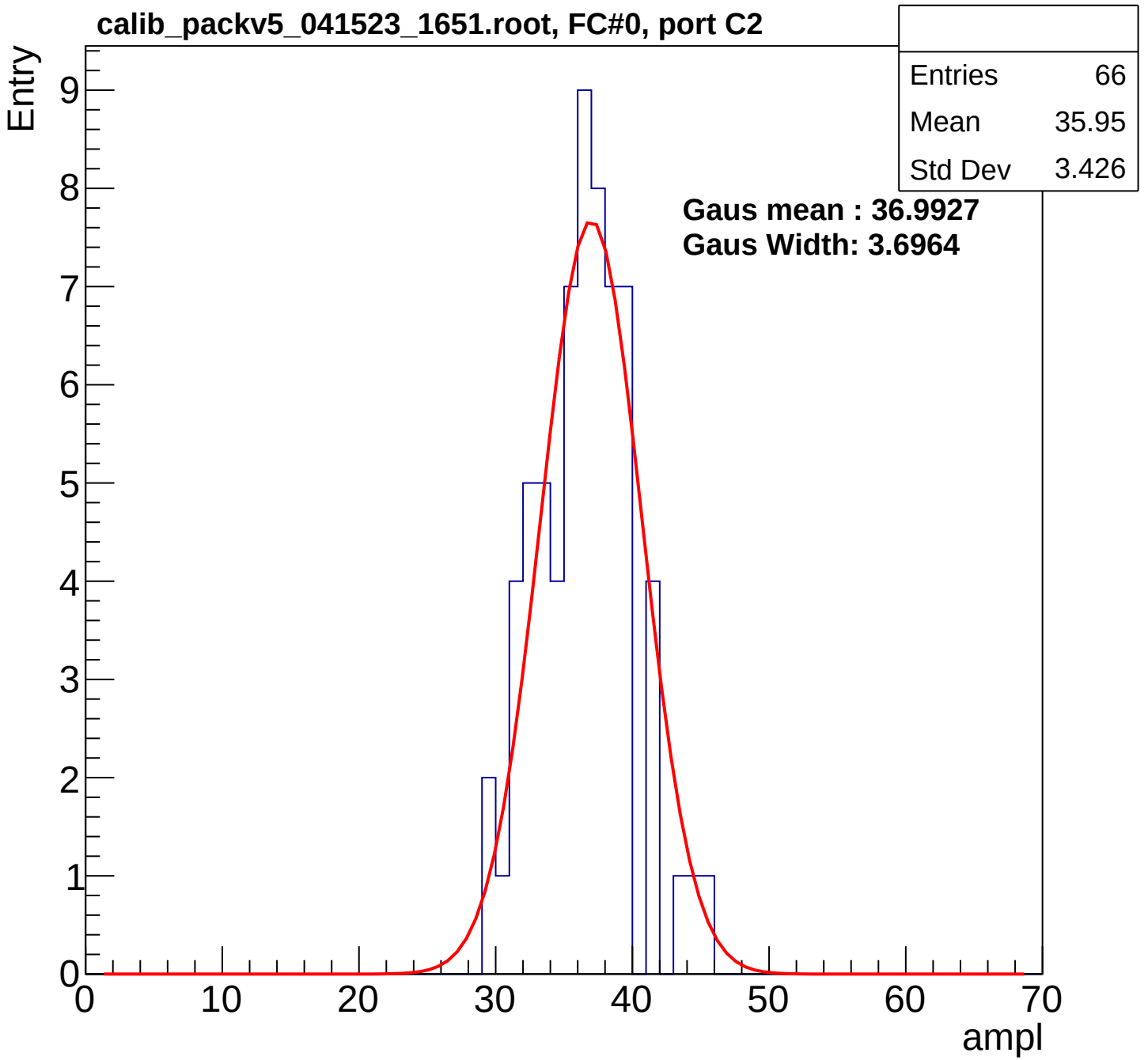
40
50
60
70


B1L103S, U12-ch57, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 35.95
Std Dev 3.426
Gaus mean : 36.9927
Gaus Width: 3.6964
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
50
60
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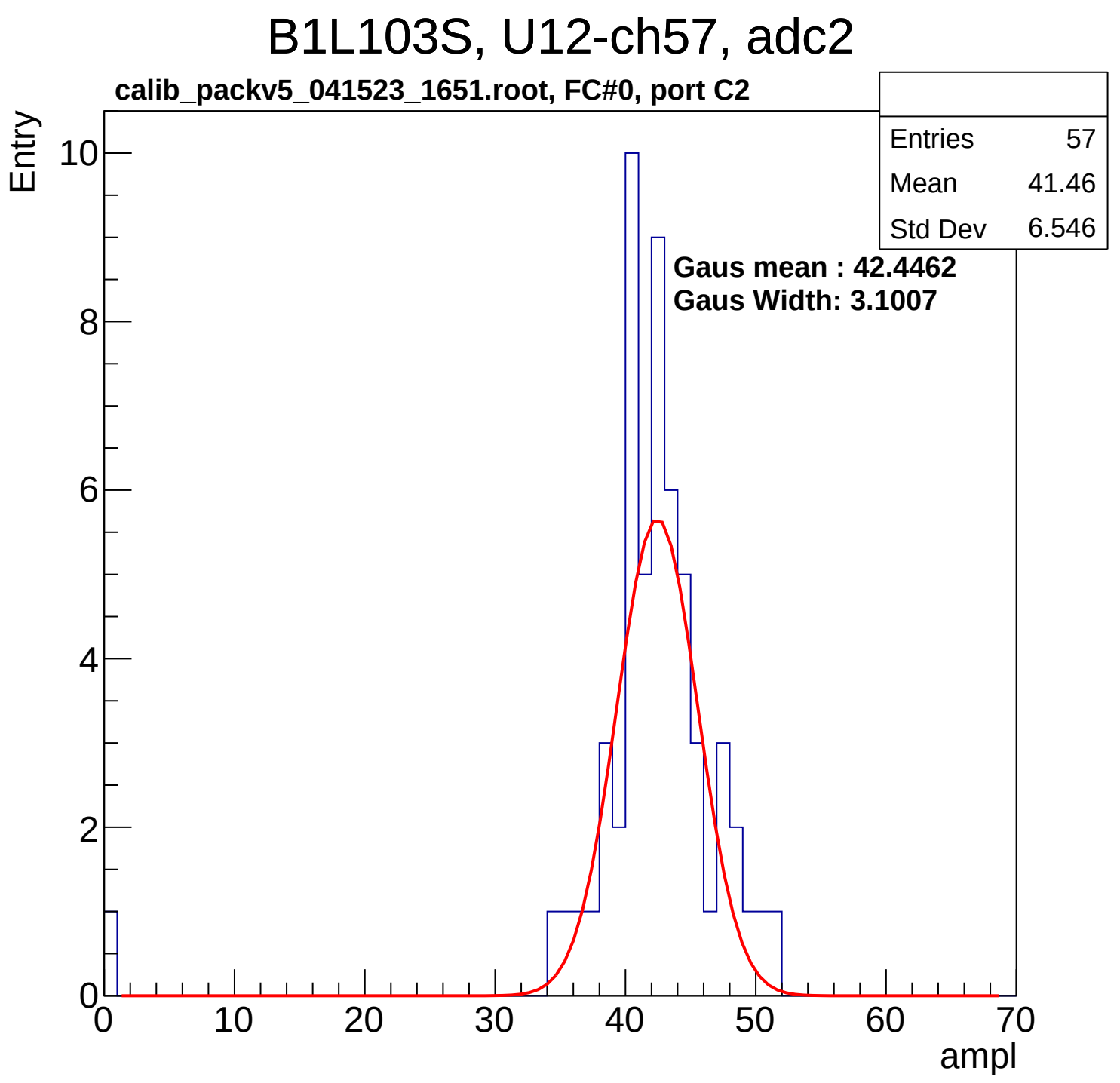
B1L103S, U12-ch57, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 41.46
Std Dev 6.546
Gaus mean : 42.4462
Gaus Width: 3.1007
Entry
ampl
0
2
4
6
8
10
0
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30
40
50
60
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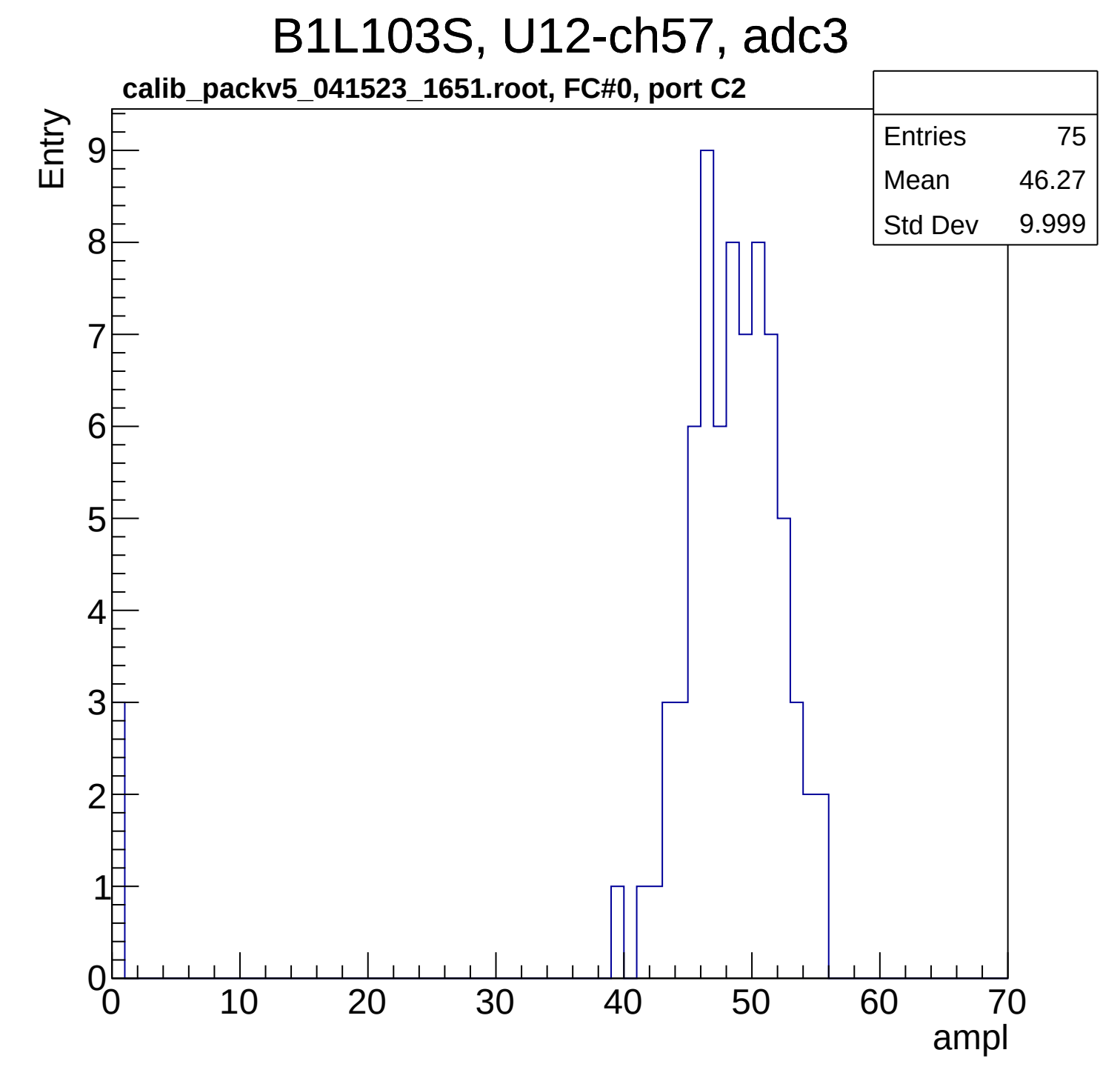
B1L103S, U12-ch57, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 46.27
Std Dev 9.999
Entry
ampl
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2
3
4
5
6
7
8
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0
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50
60
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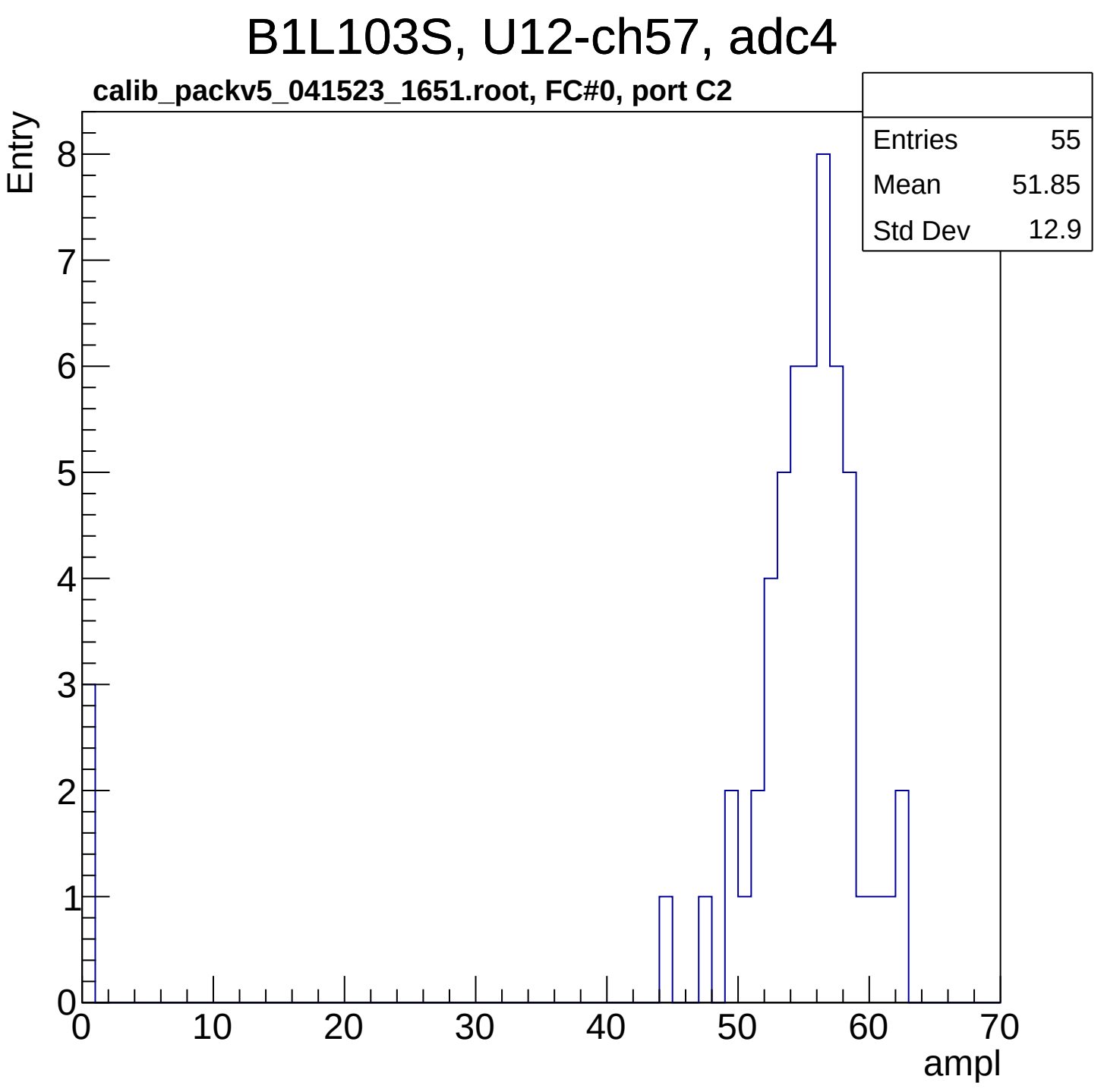
B1L103S, U12-ch57, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 51.85
Std Dev 12.9
Entry
ampl
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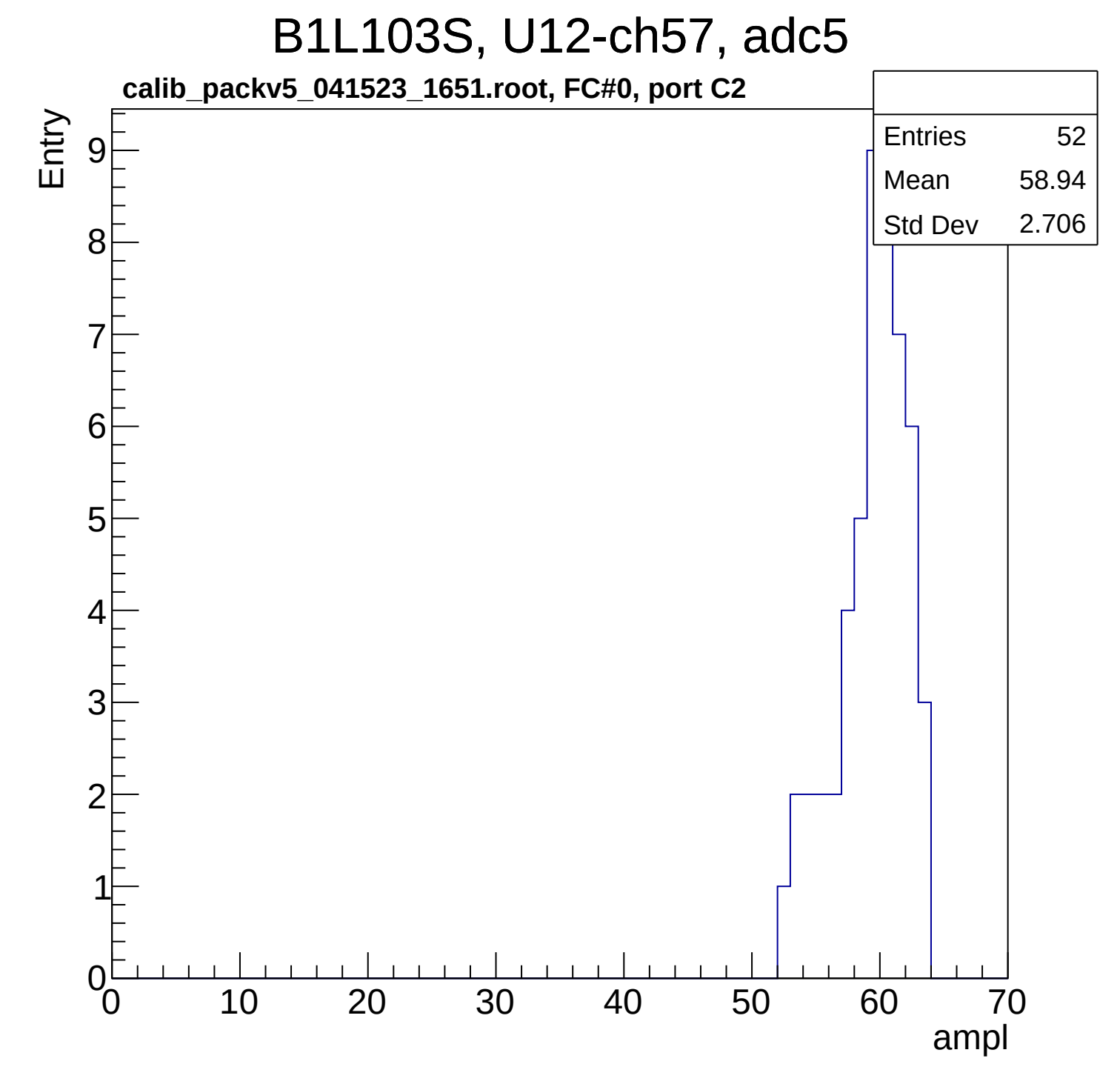
B1L103S, U12-ch57, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 58.94
Std Dev 2.706
Entry
ampl
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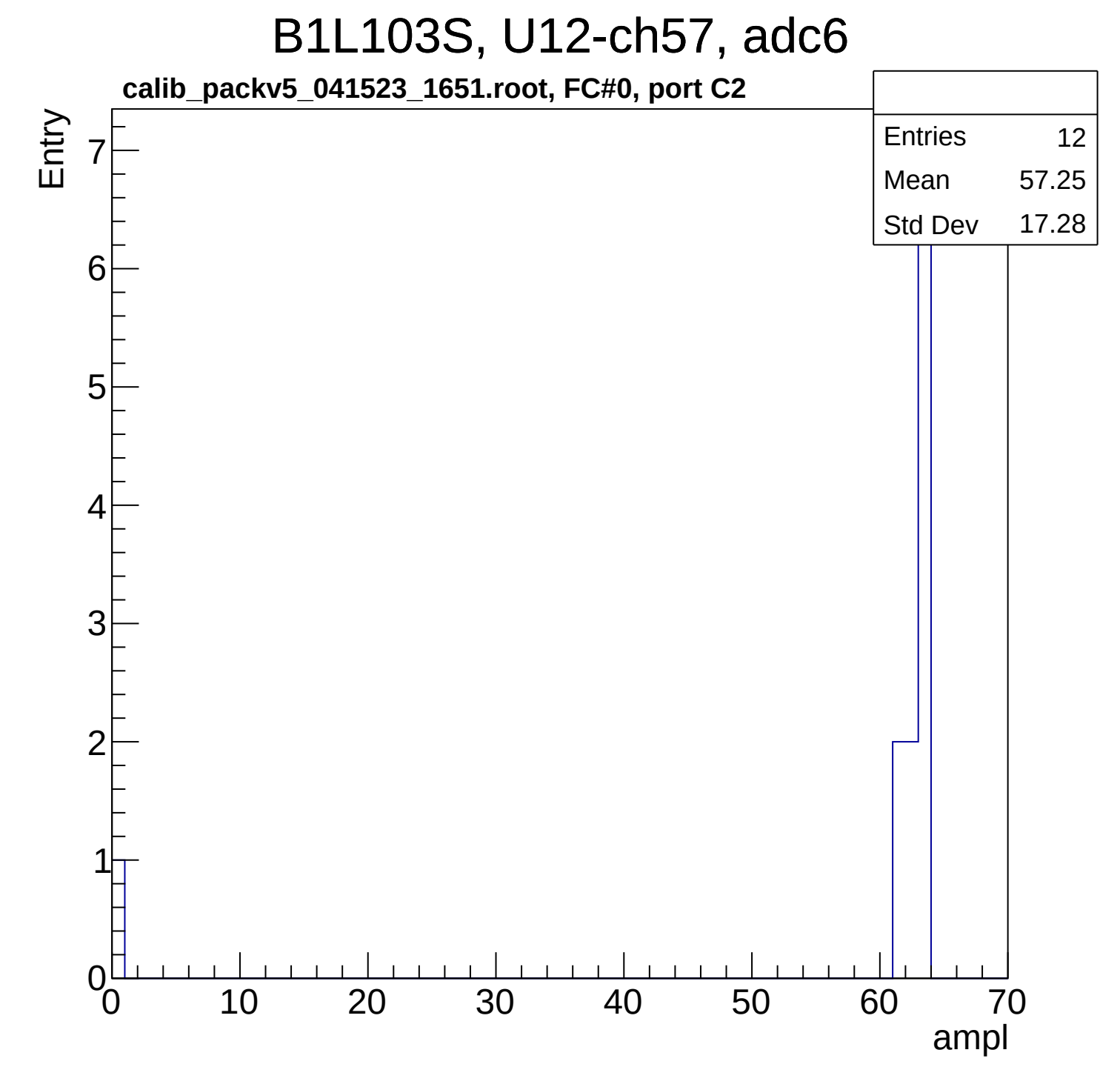
B1L103S, U12-ch57, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 57.25
Std Dev 17.28
Entry
ampl
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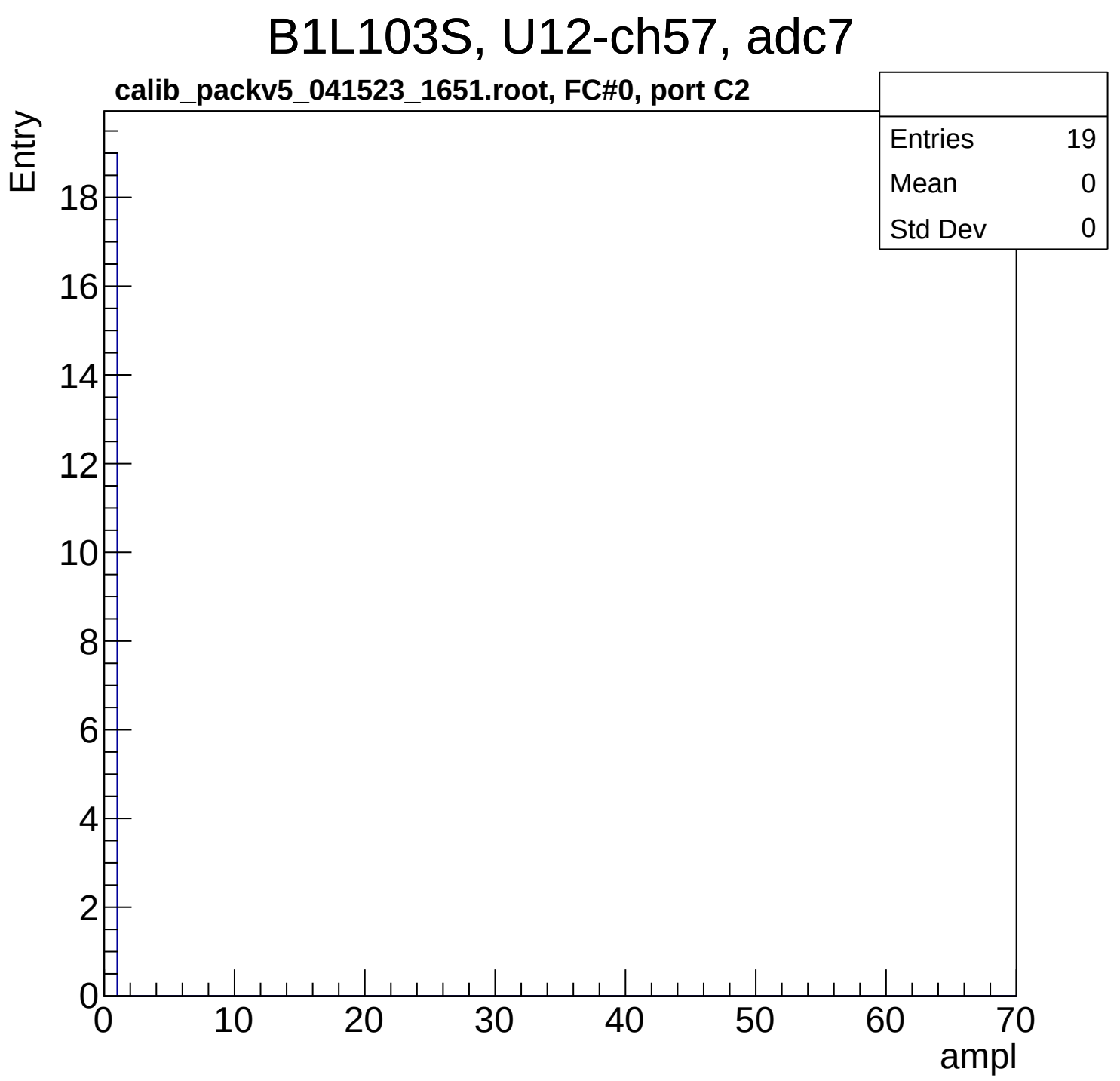
B1L103S, U12-ch57, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
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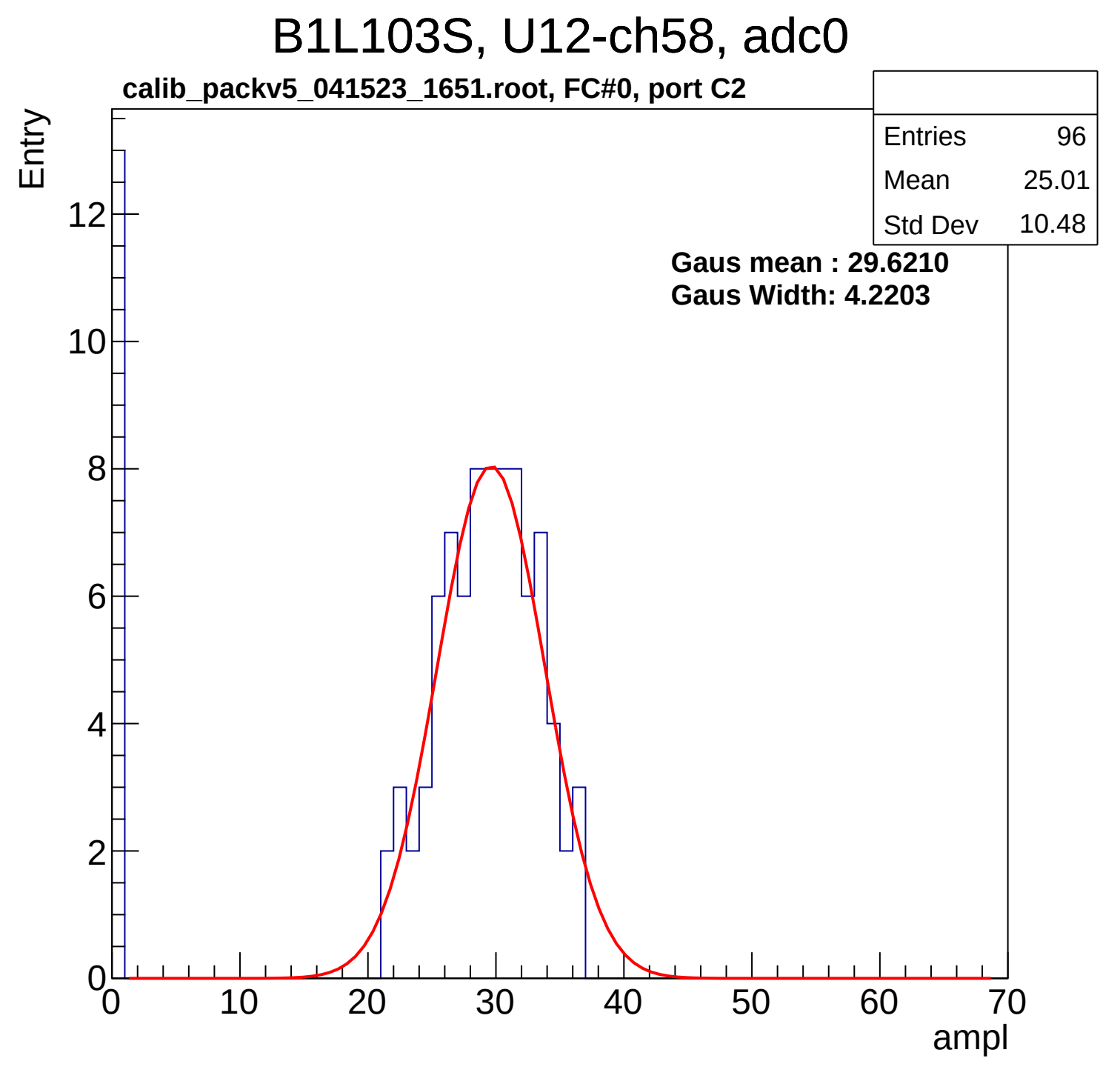
40
50
60
70
ampl


B1L103S, U12-ch58, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 96
Mean 25.01
Std Dev 10.48
Gaus mean : 29.6210
Gaus Width: 4.2203
Entry
ampl
0
2
4
6
8
10
12
0
10
20
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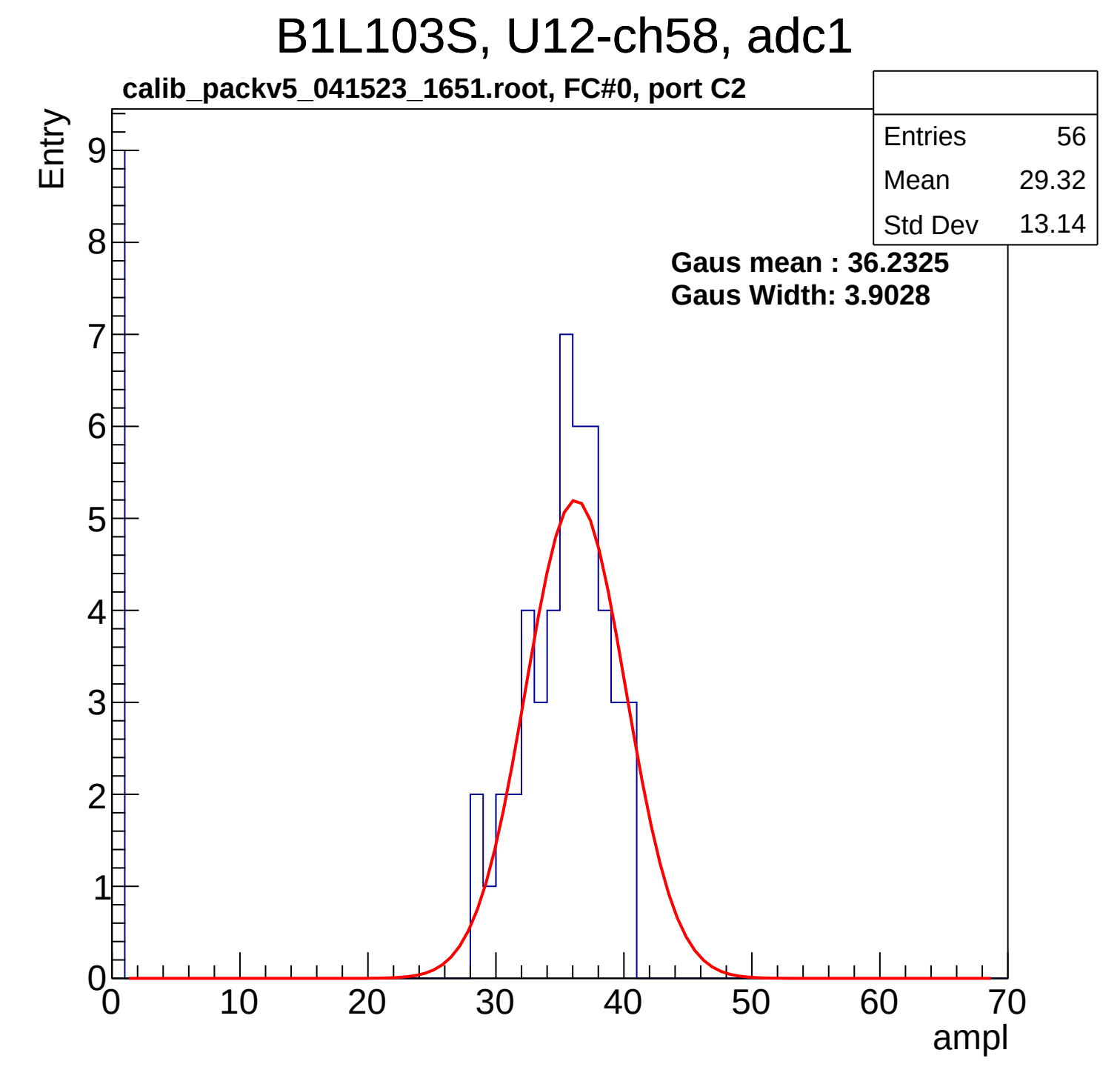
40
50
60
70


B1L103S, U12-ch58, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 29.32
Std Dev 13.14
Gaus mean : 36.2325
Gaus Width: 3.9028
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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40
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60
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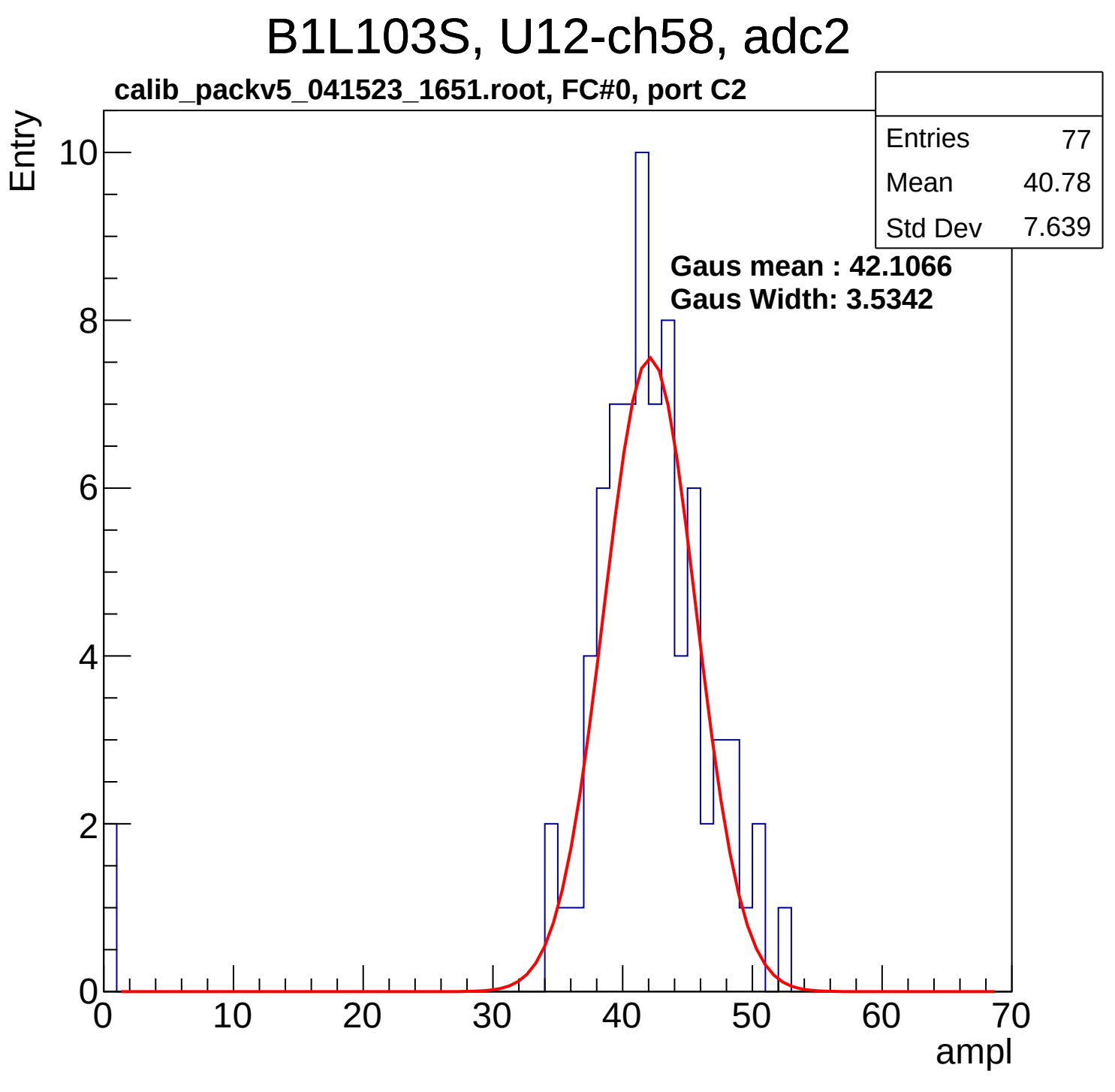
B1L103S, U12-ch58, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 40.78
Std Dev 7.639
Gaus mean : 42.1066
Gaus Width: 3.5342
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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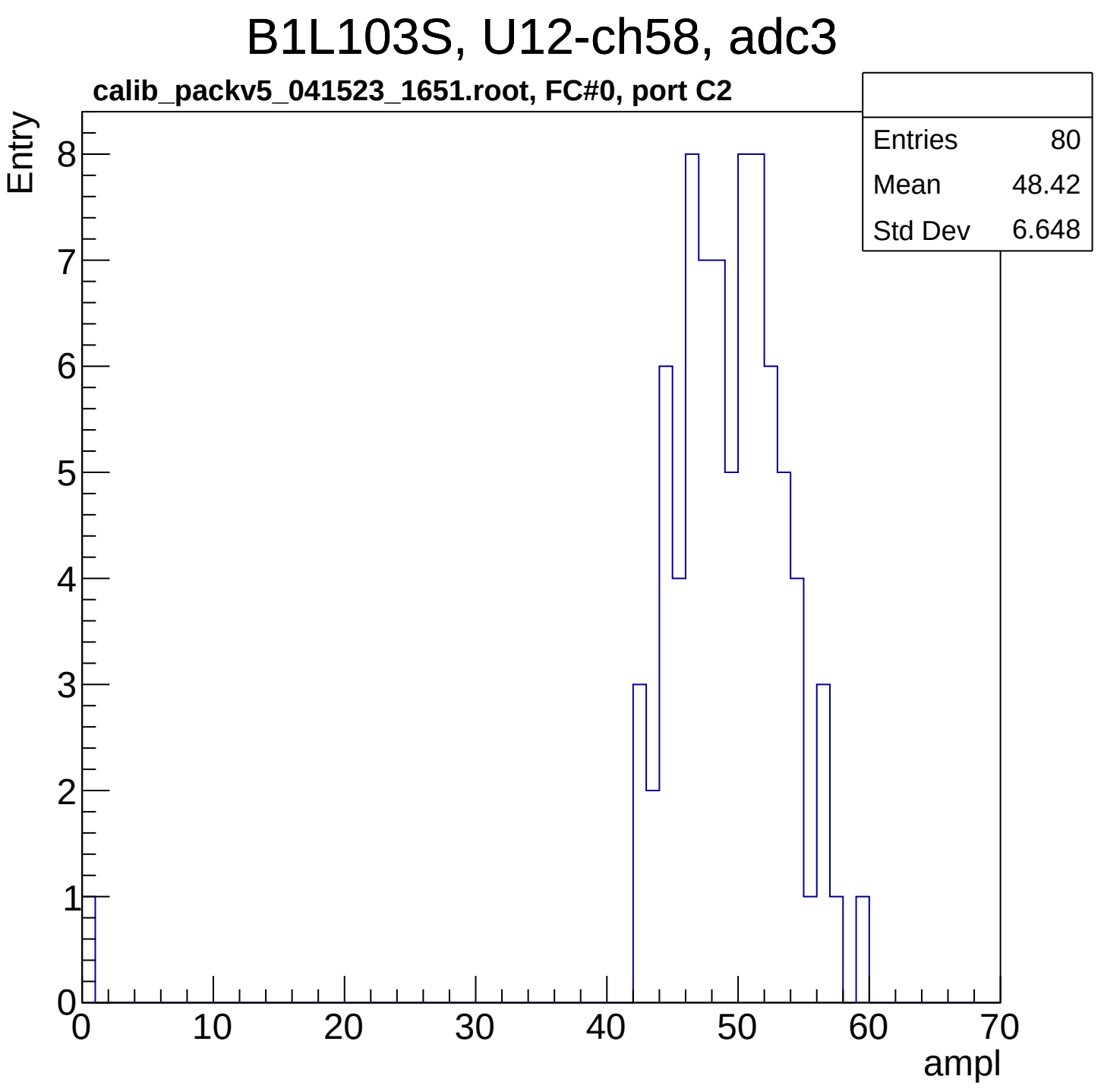
B1L103S, U12-ch58, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 48.42
Std Dev 6.648
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
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40
50
60
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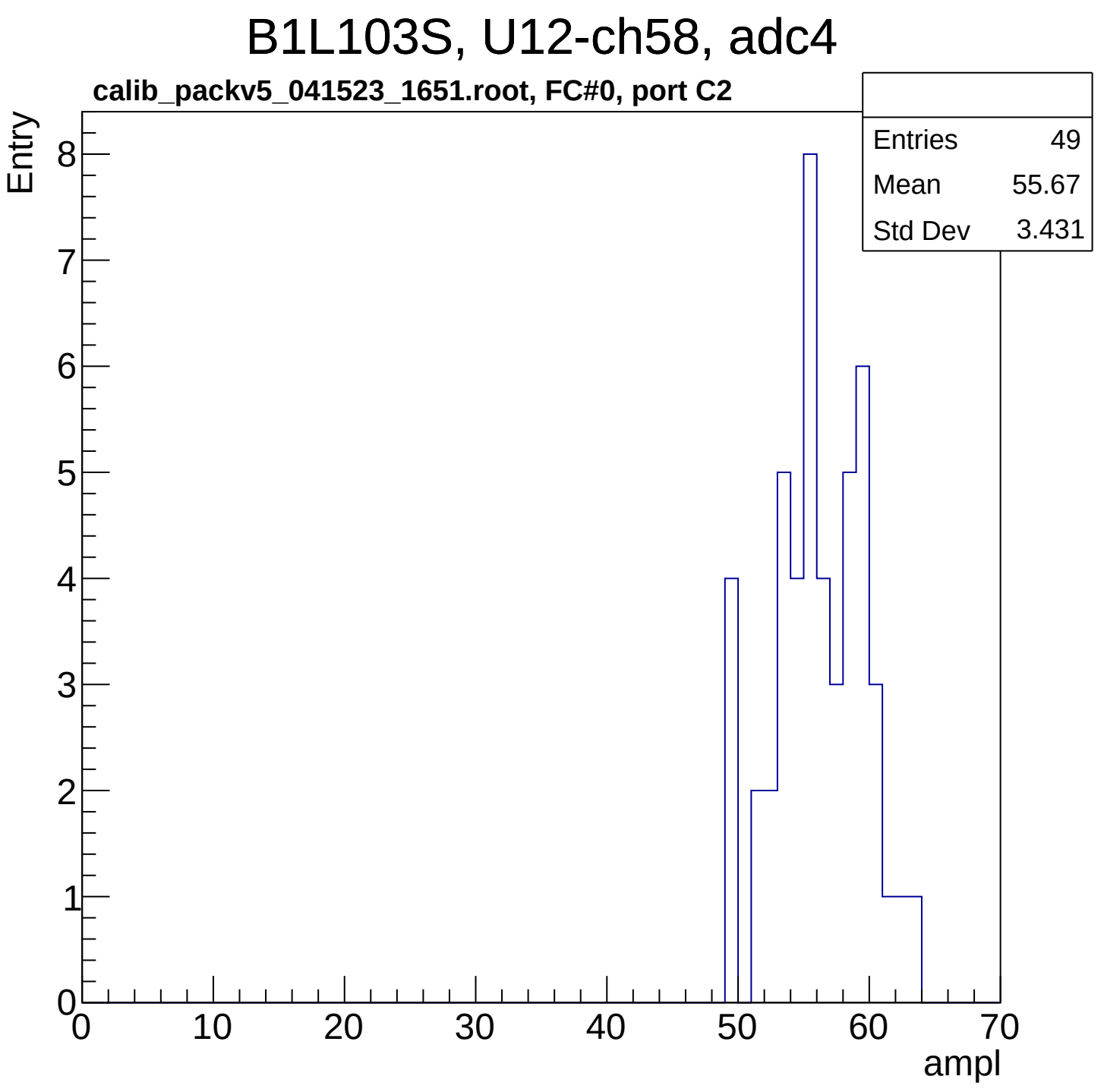
B1L103S, U12-ch58, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 55.67
Std Dev 3.431
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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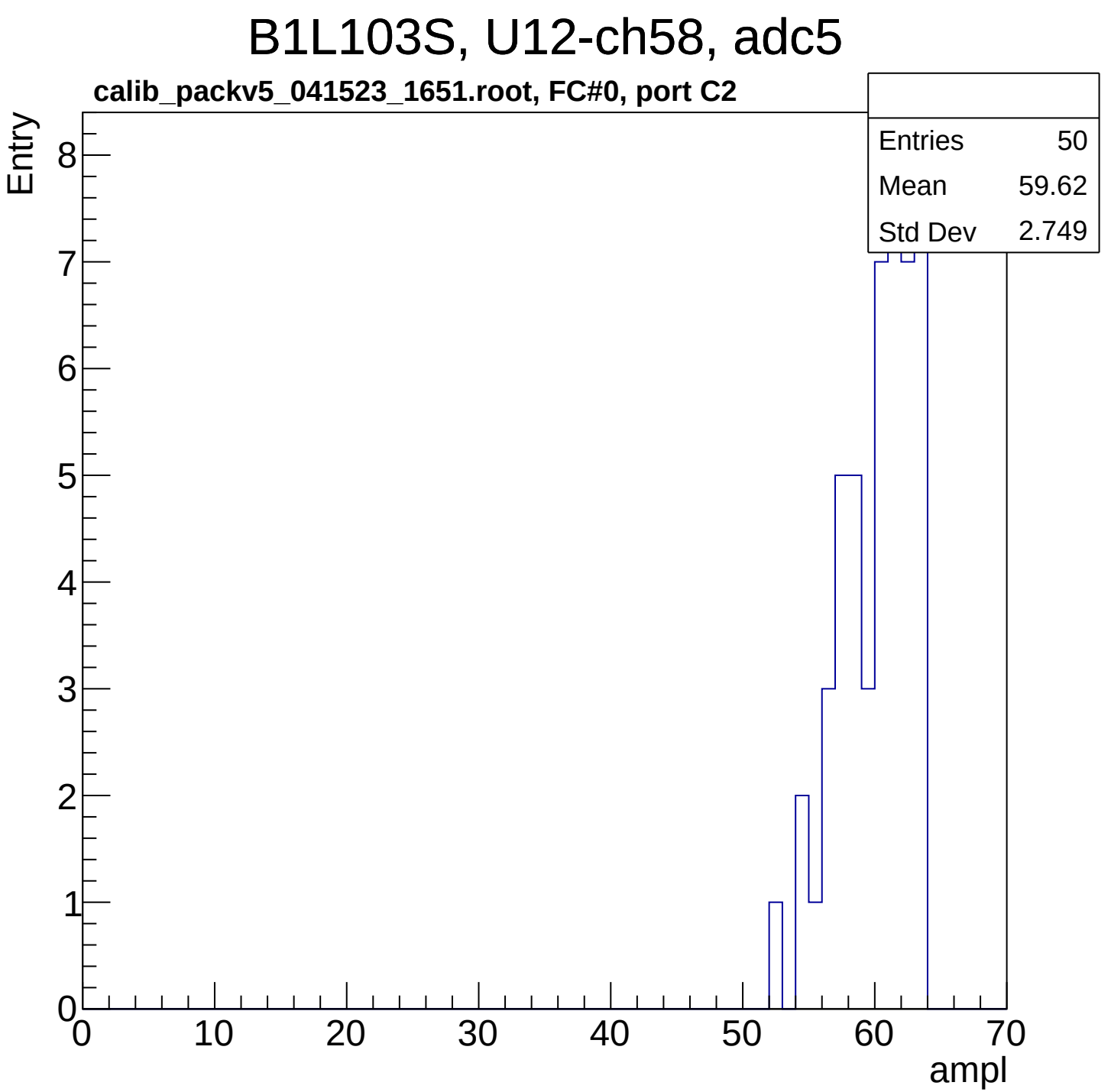
B1L103S, U12-ch58, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 59.62
Std Dev 2.749
Entry
ampl
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2
3
4
5
6
7
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60
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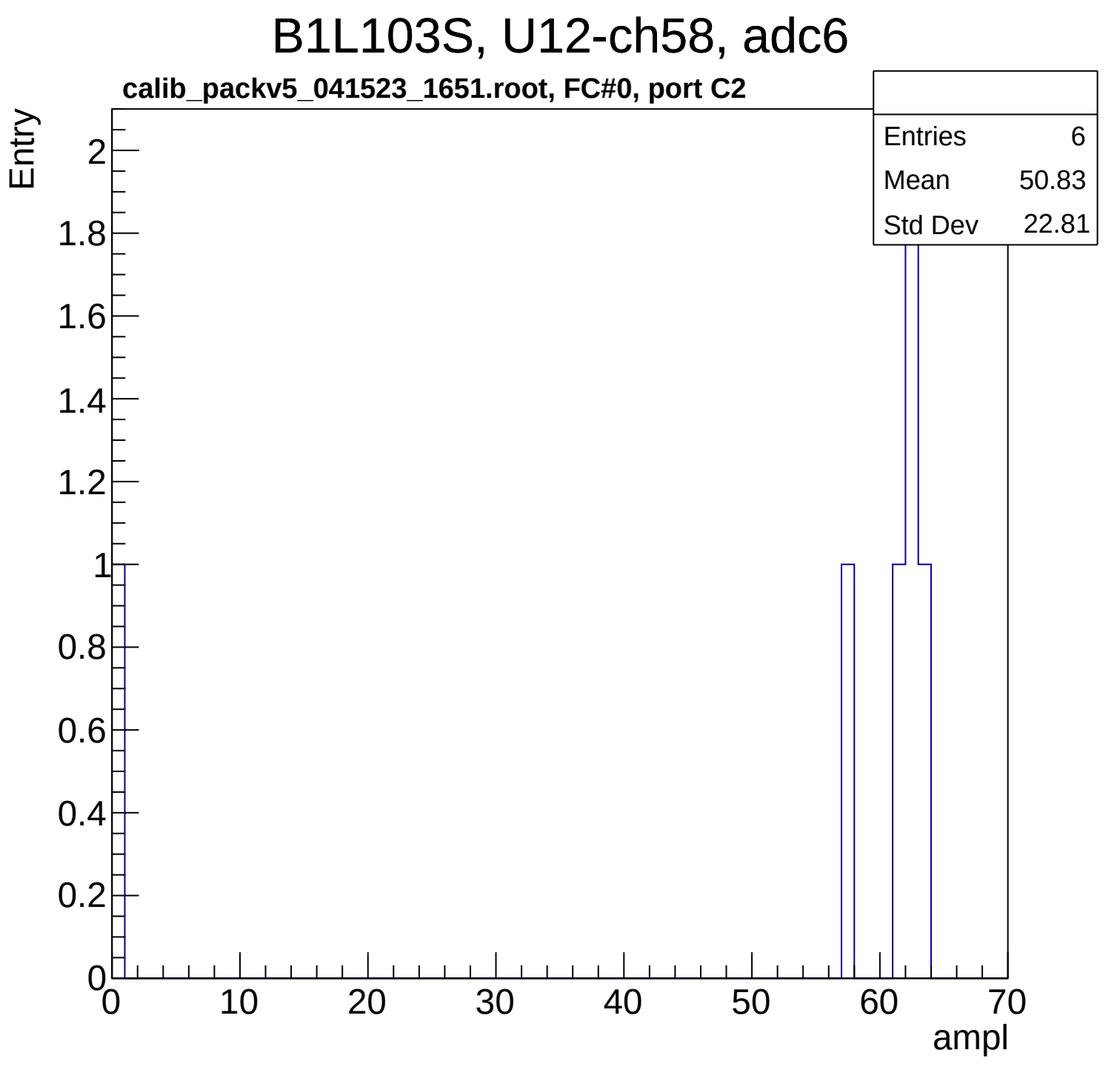
B1L103S, U12-ch58, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 50.83
Std Dev 22.81
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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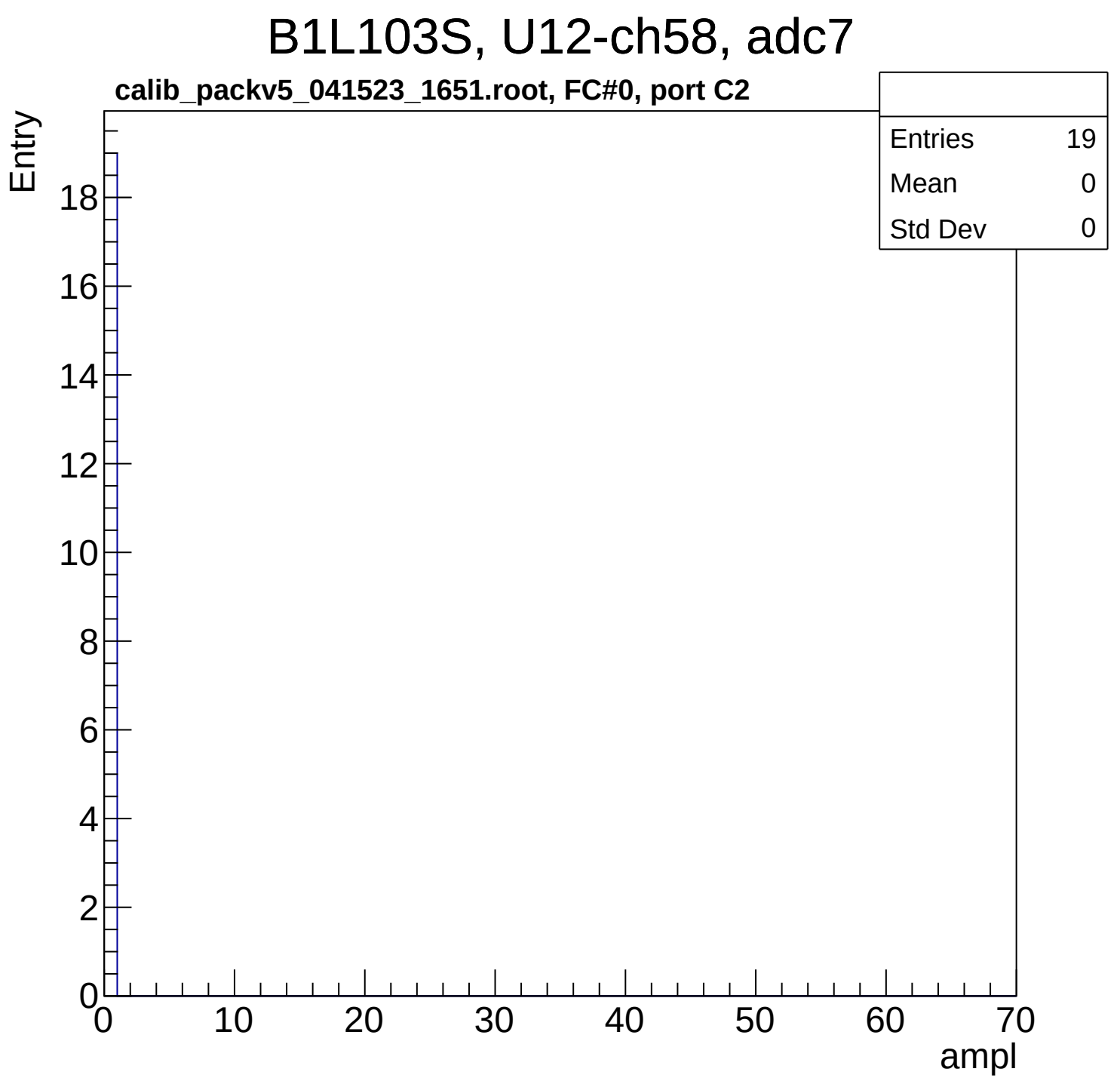
B1L103S, U12-ch58, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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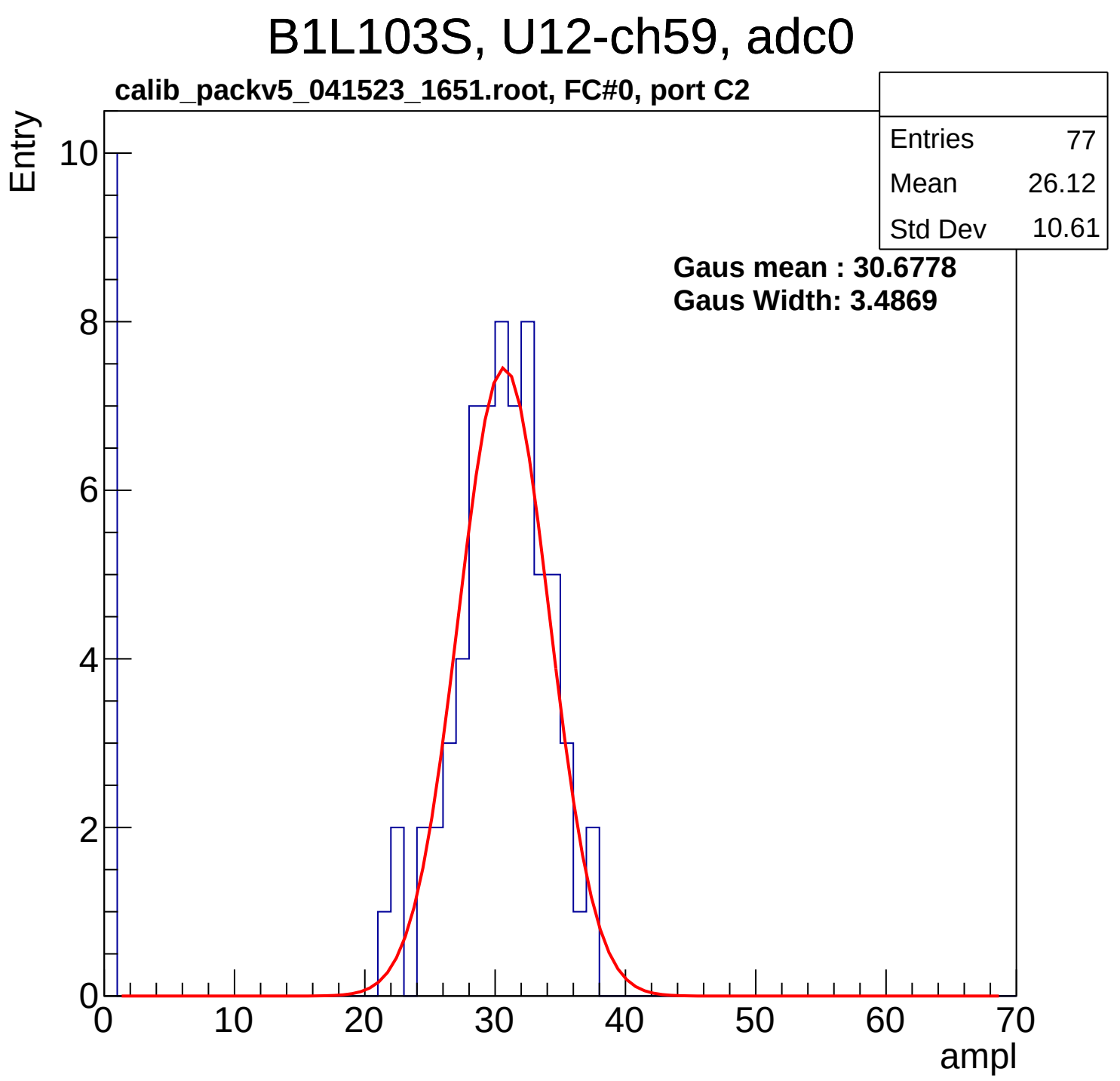
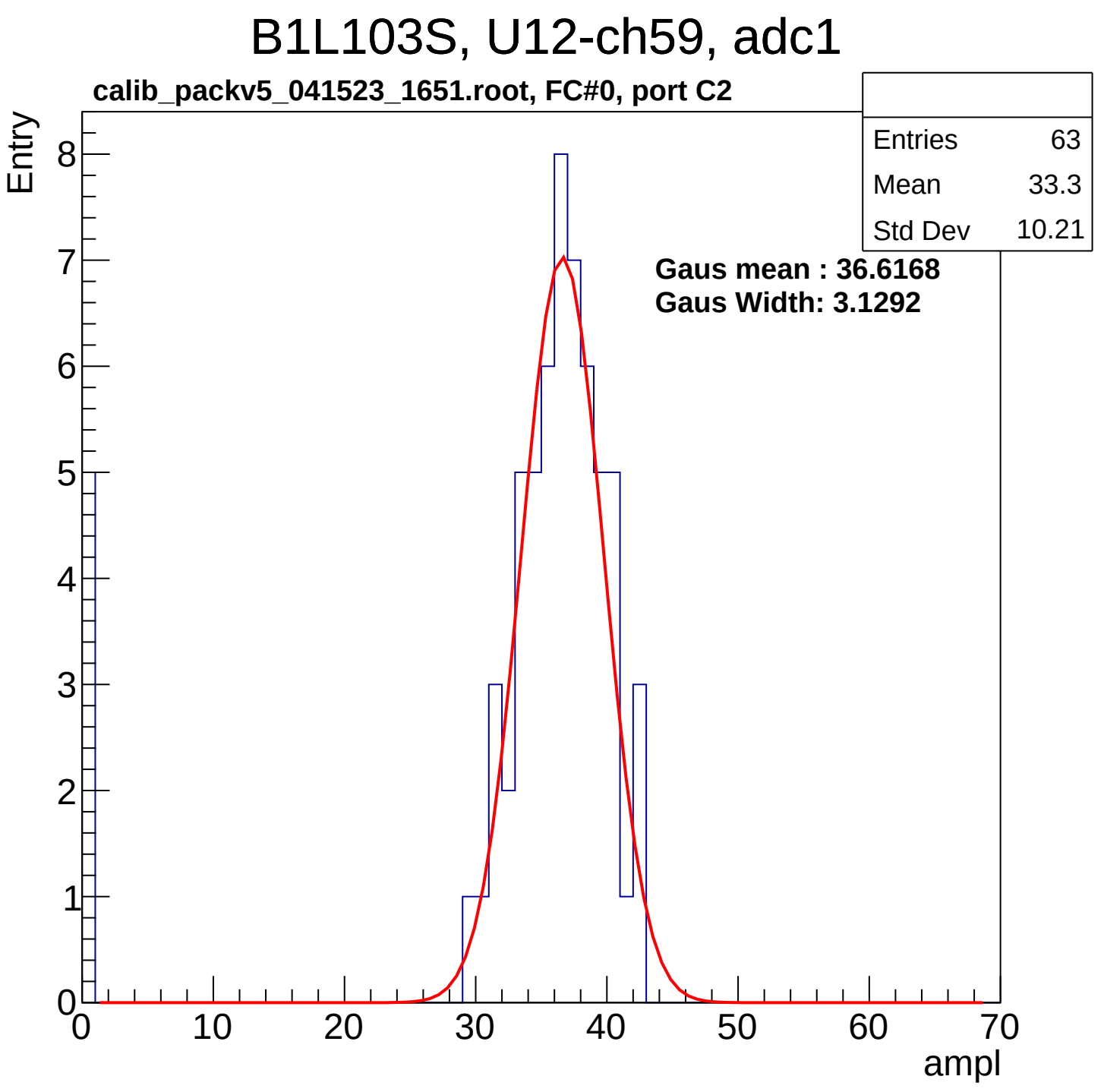
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch59, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 26.12
Std Dev 10.61
Gaus mean : 30.6778
Gaus Width: 3.4869
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch59, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 33.3
Std Dev 10.21
Gaus mean : 36.6168
Gaus Width: 3.1292
Entry
ampl
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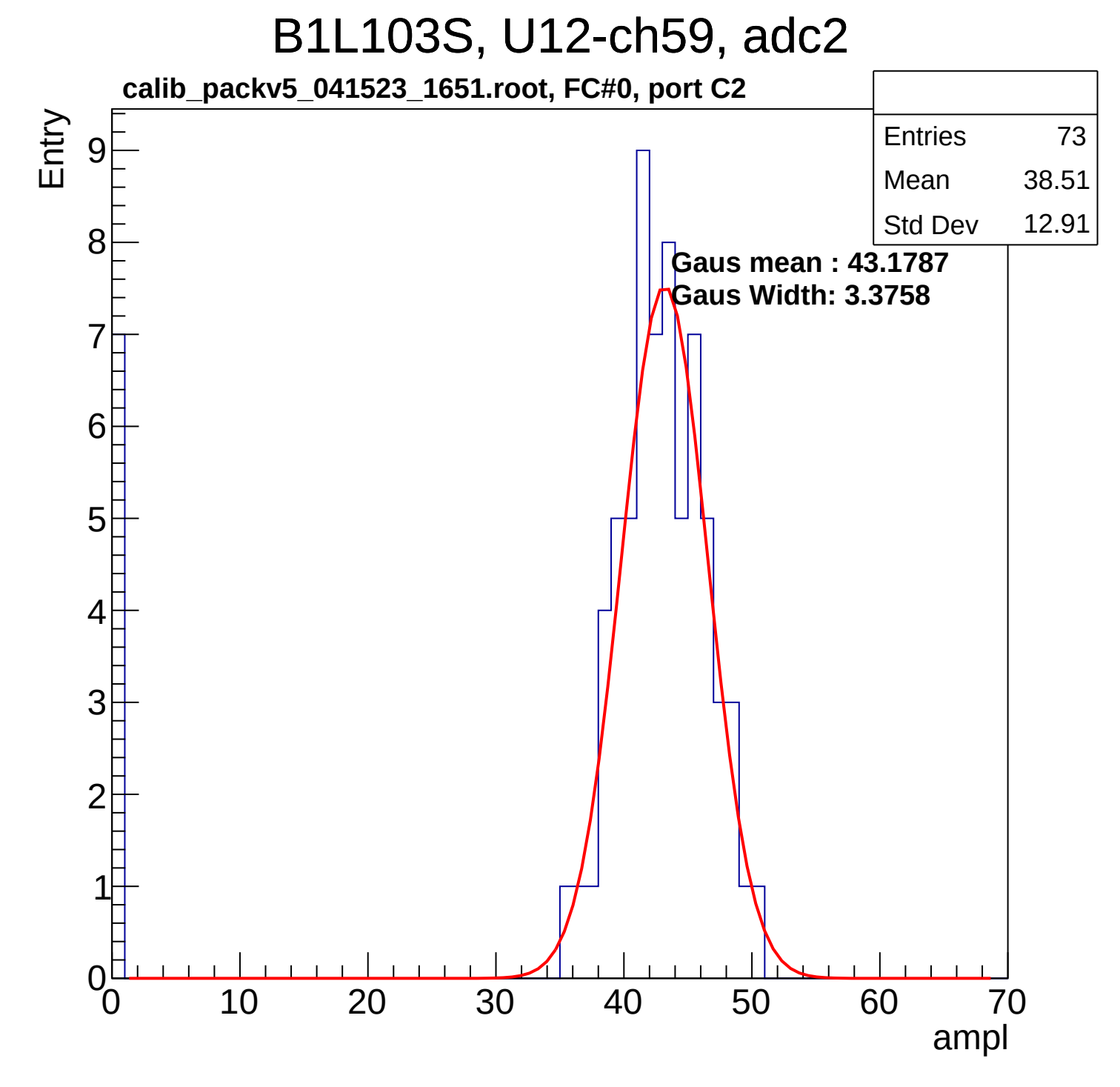
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U12-ch59, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 38.51
Std Dev 12.91
Gaus mean : 43.1787
Gaus Width: 3.3758
Entry
ampl
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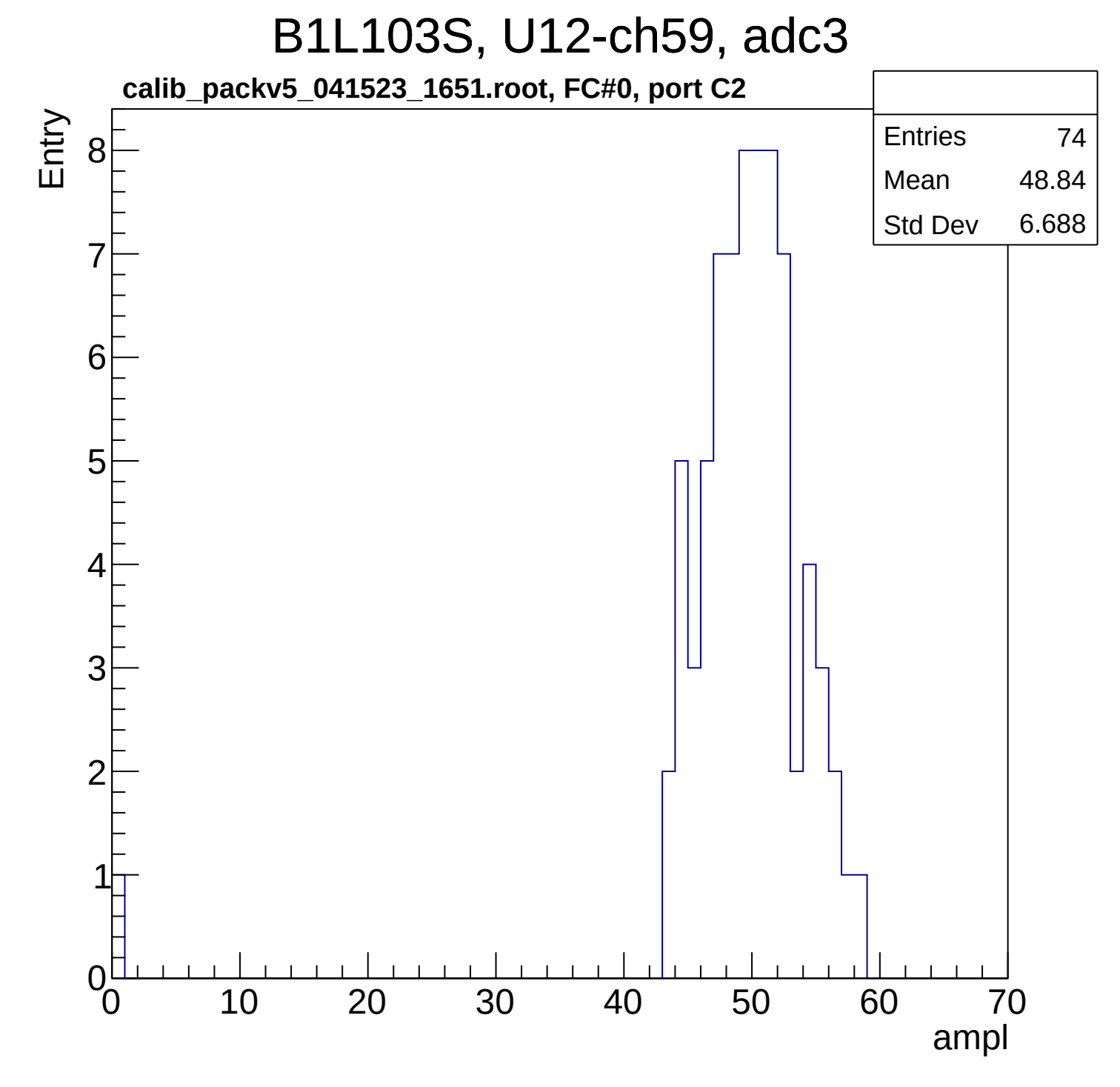
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U12-ch59, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 48.84
Std Dev 6.688
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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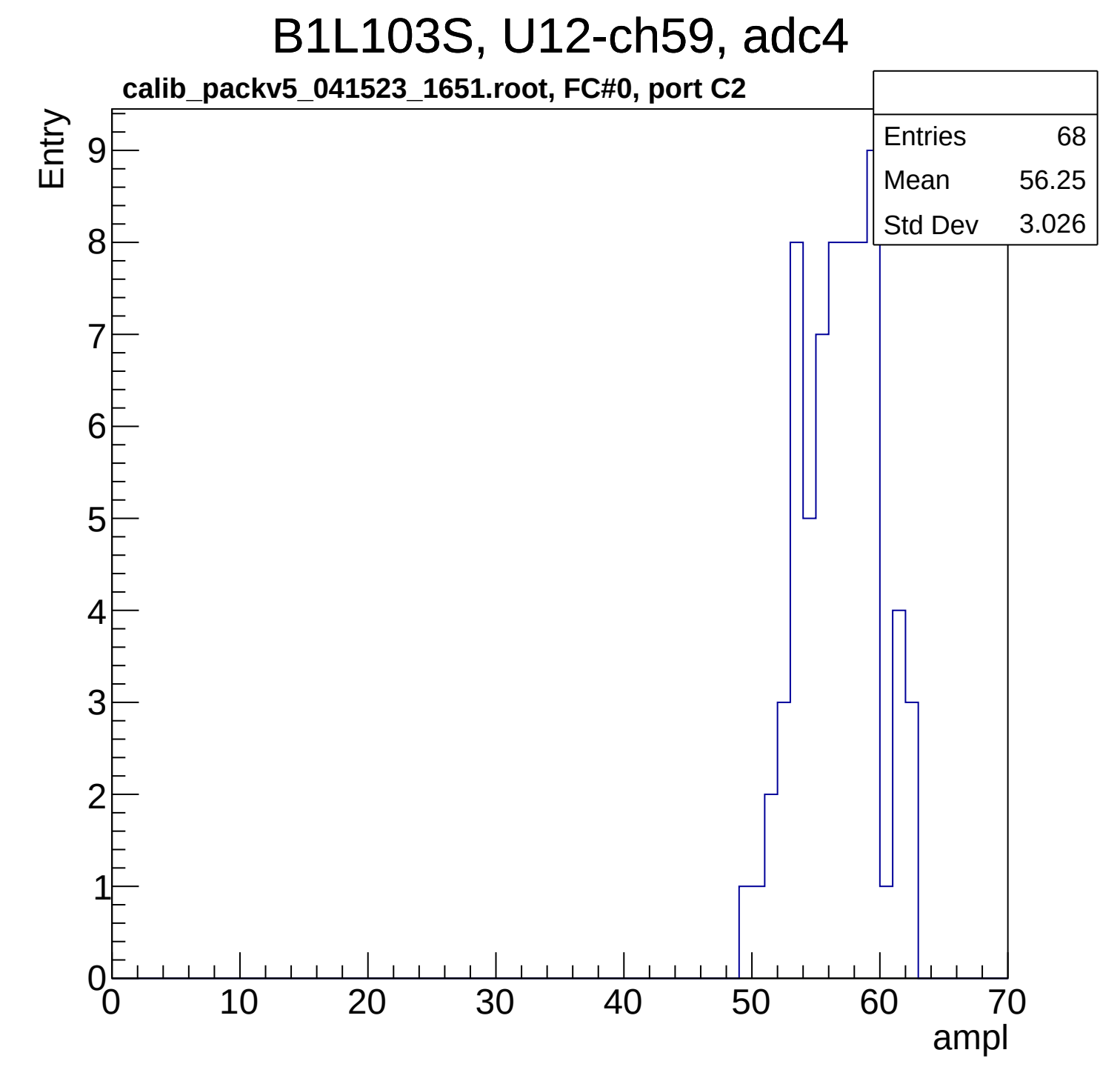
B1L103S, U12-ch59, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 56.25
Std Dev 3.026
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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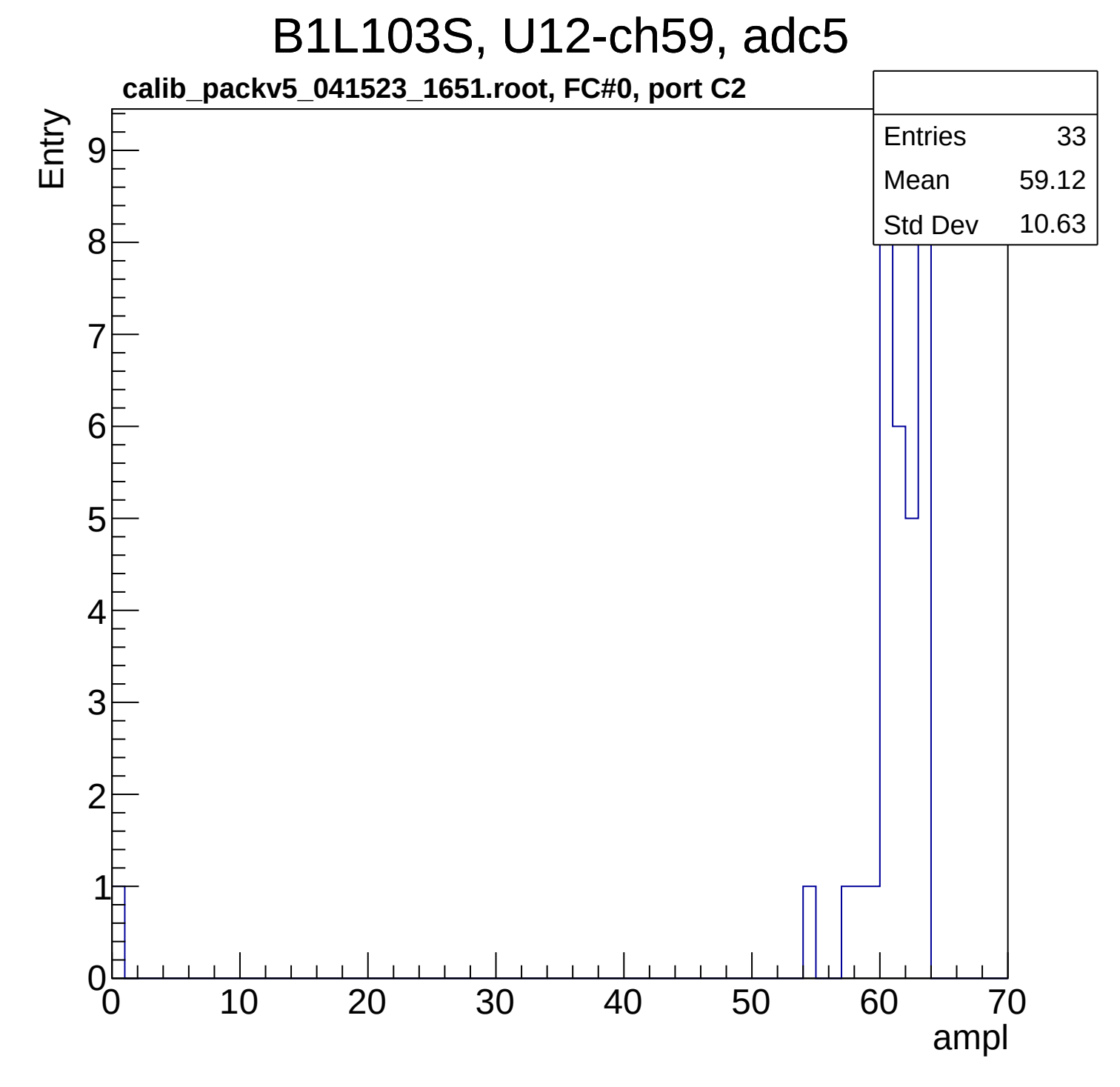
B1L103S, U12-ch59, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 59.12
Std Dev 10.63
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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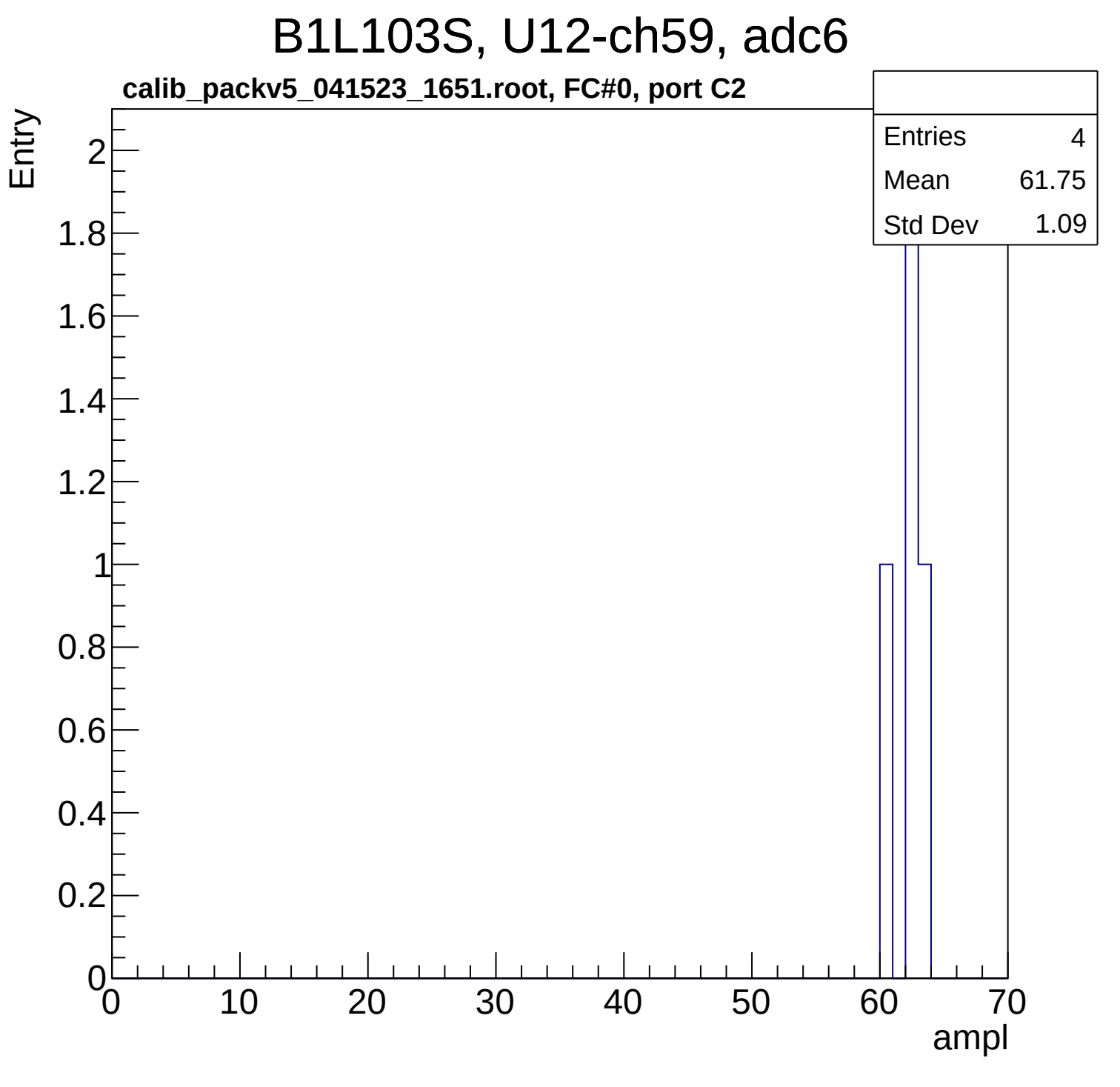
B1L103S, U12-ch59, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 61.75
Std Dev 1.09
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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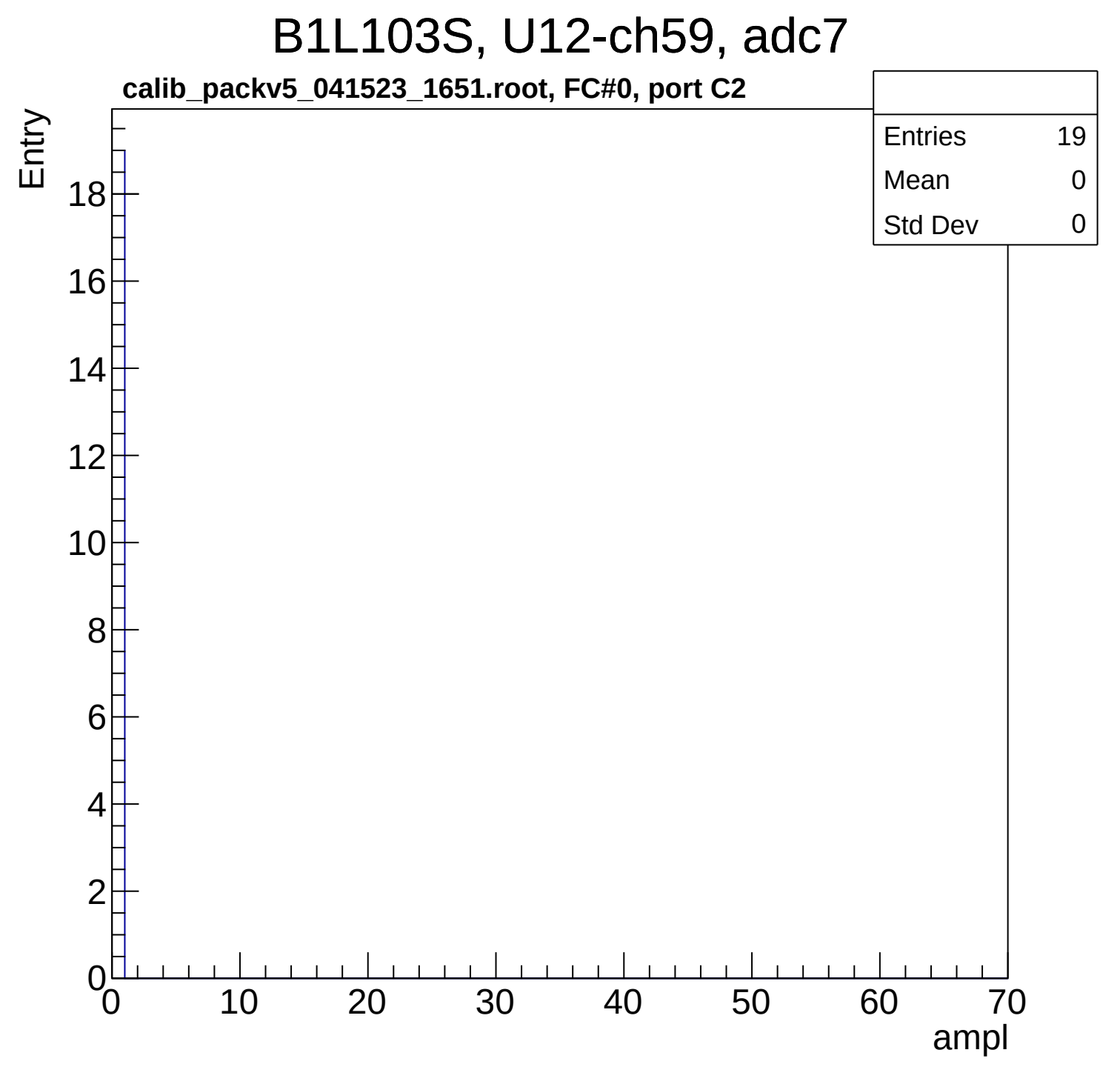
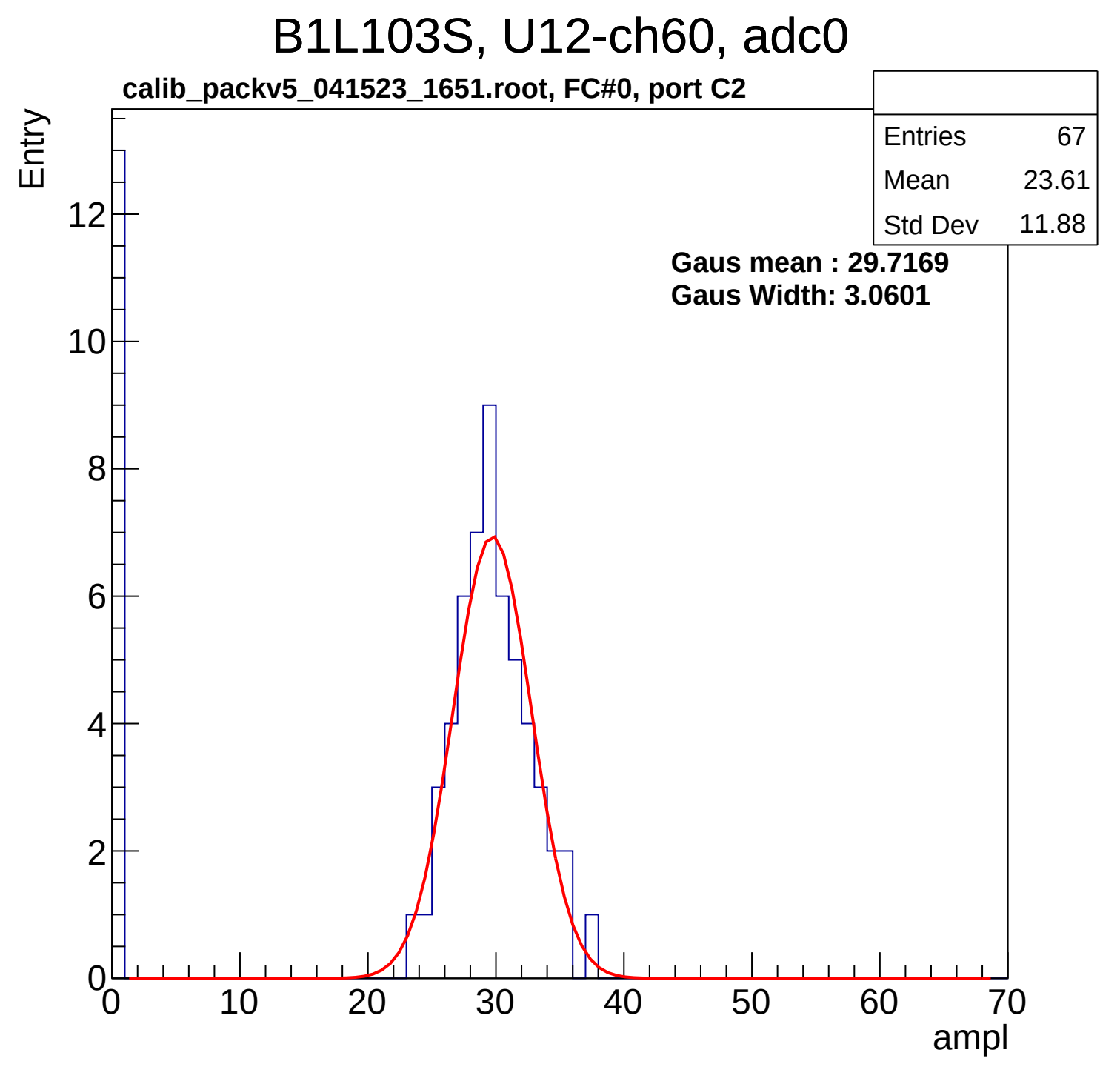
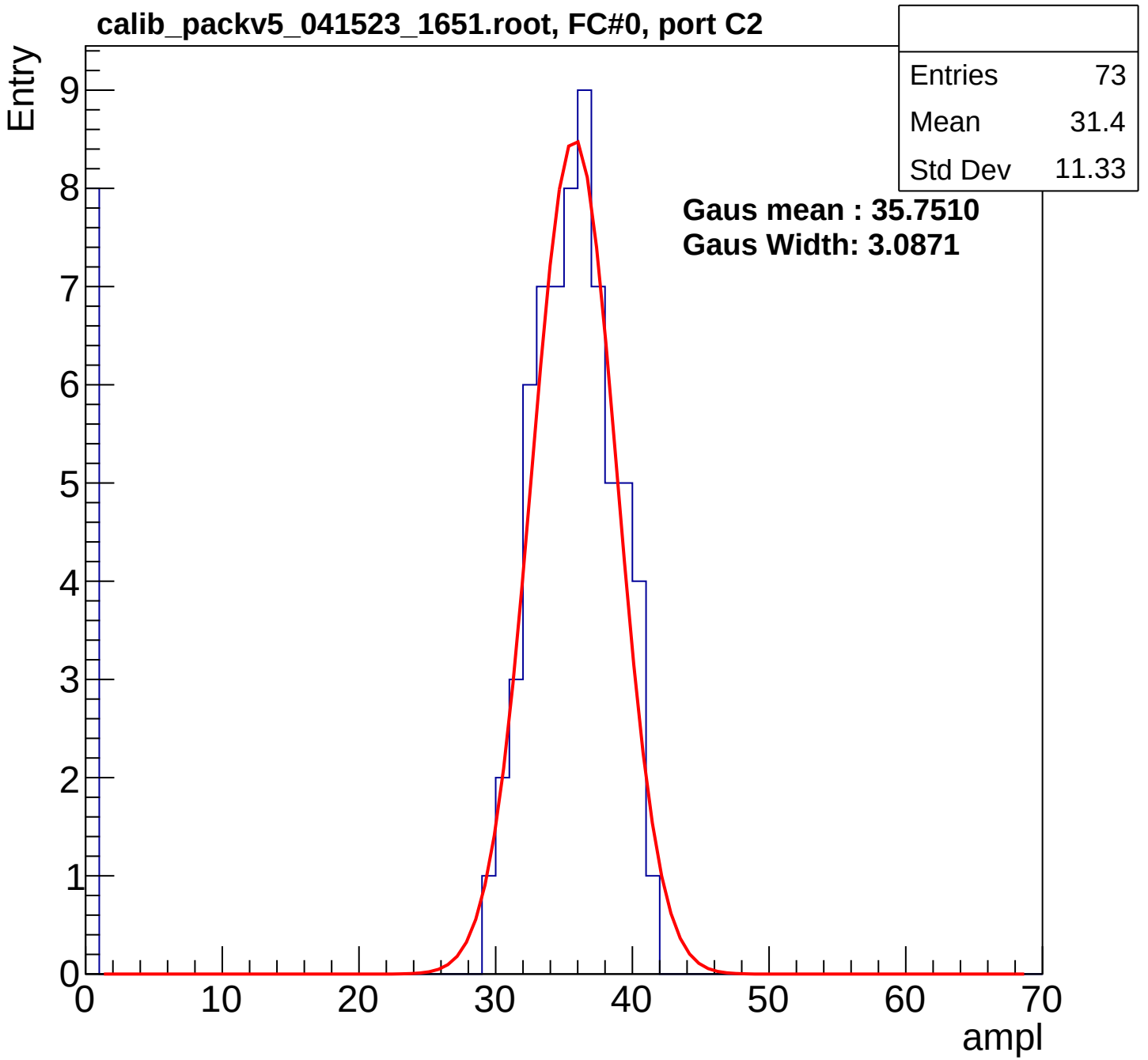

B1L103S, U12-ch59, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch60, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 23.61
Std Dev 11.88
Gaus mean : 29.7169
Gaus Width: 3.0601
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U12-ch60, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 31.4
Std Dev 11.33
Gaus mean : 35.7510
Gaus Width: 3.0871
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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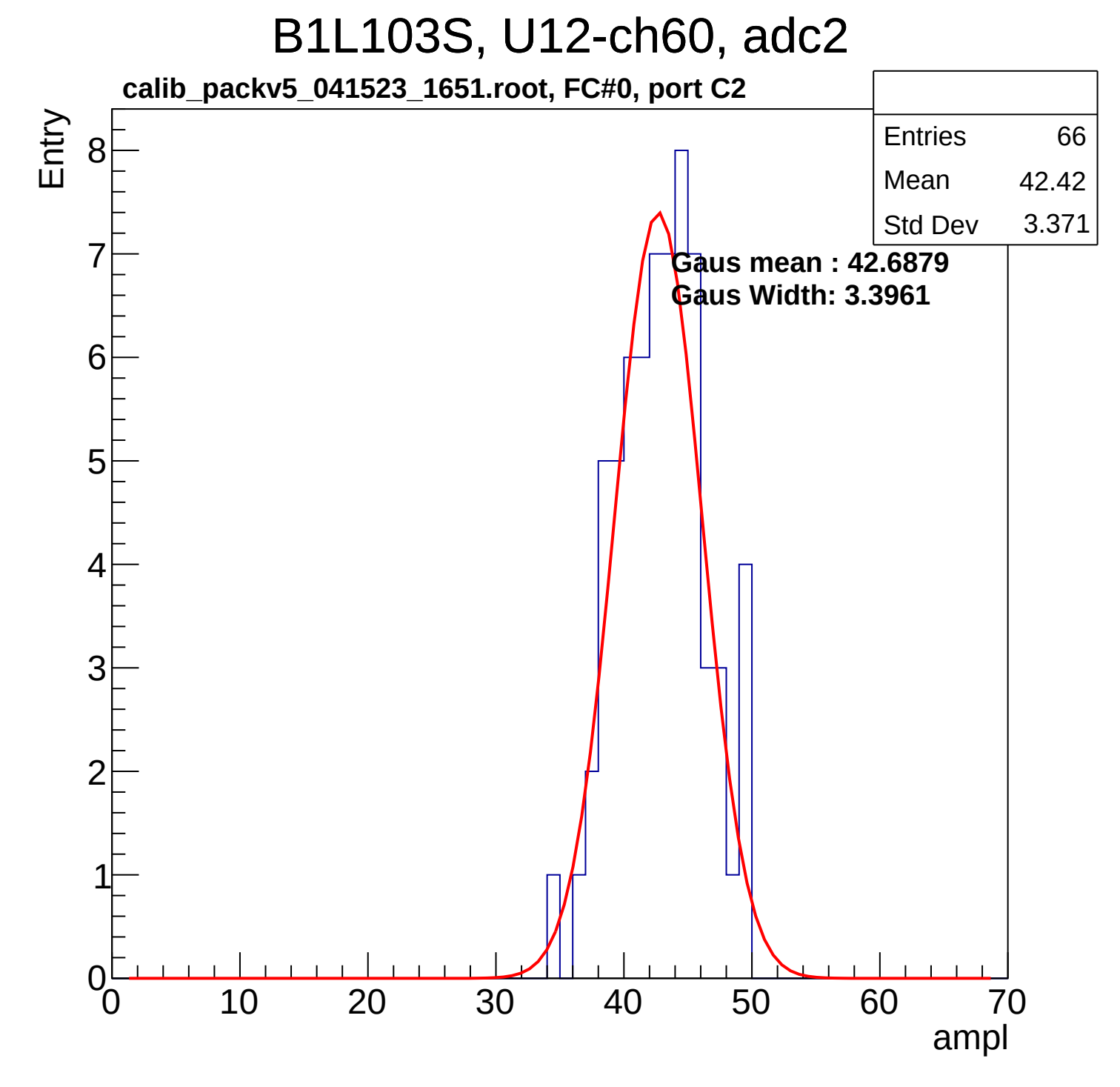
B1L103S, U12-ch60, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 42.42
Std Dev 3.371
Gaus mean : 42.6879
Gaus Width: 3.3961
Entry
ampl
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2
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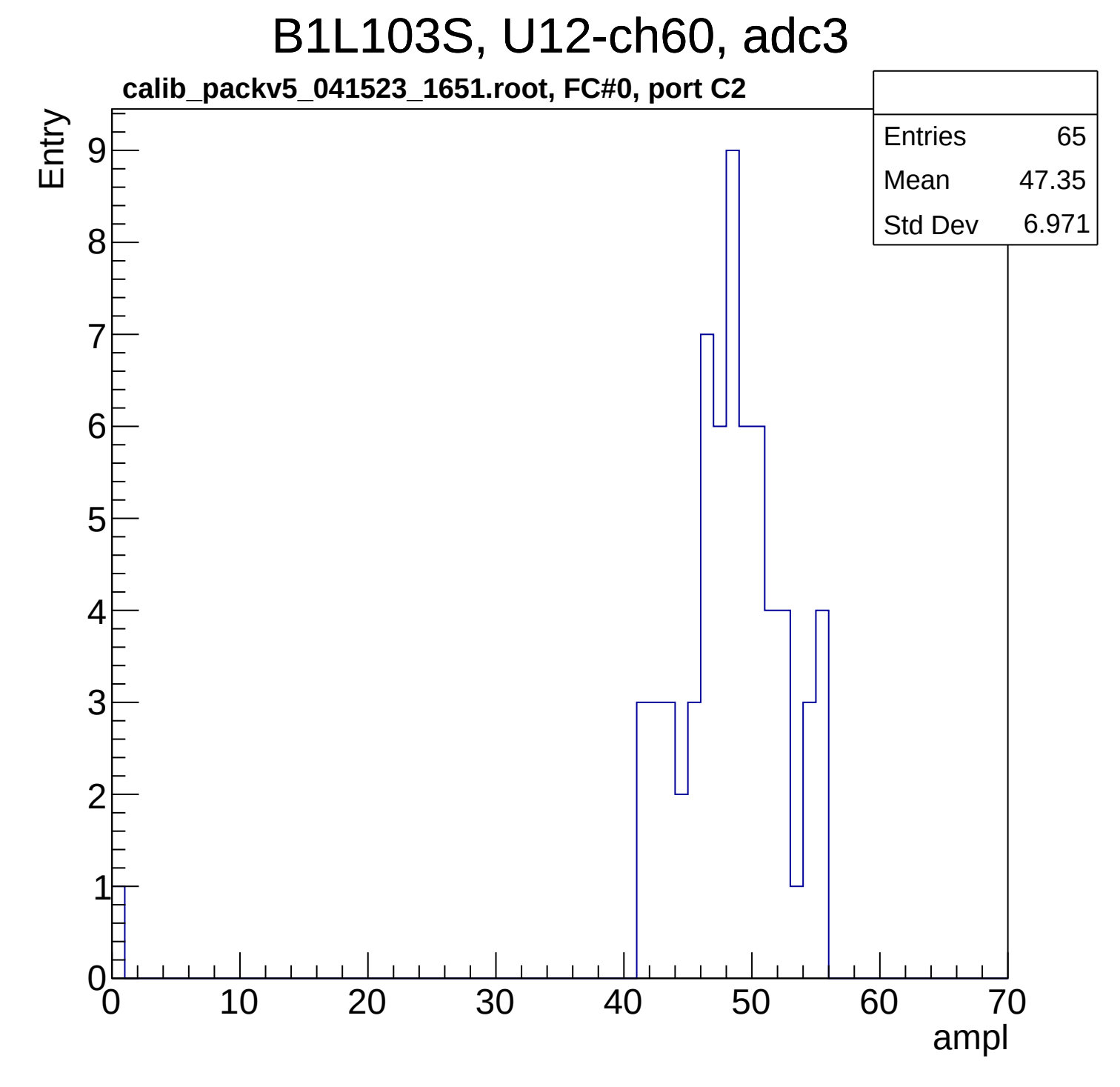
B1L103S, U12-ch60, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 47.35
Std Dev 6.971
Entry
ampl
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7
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0
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60
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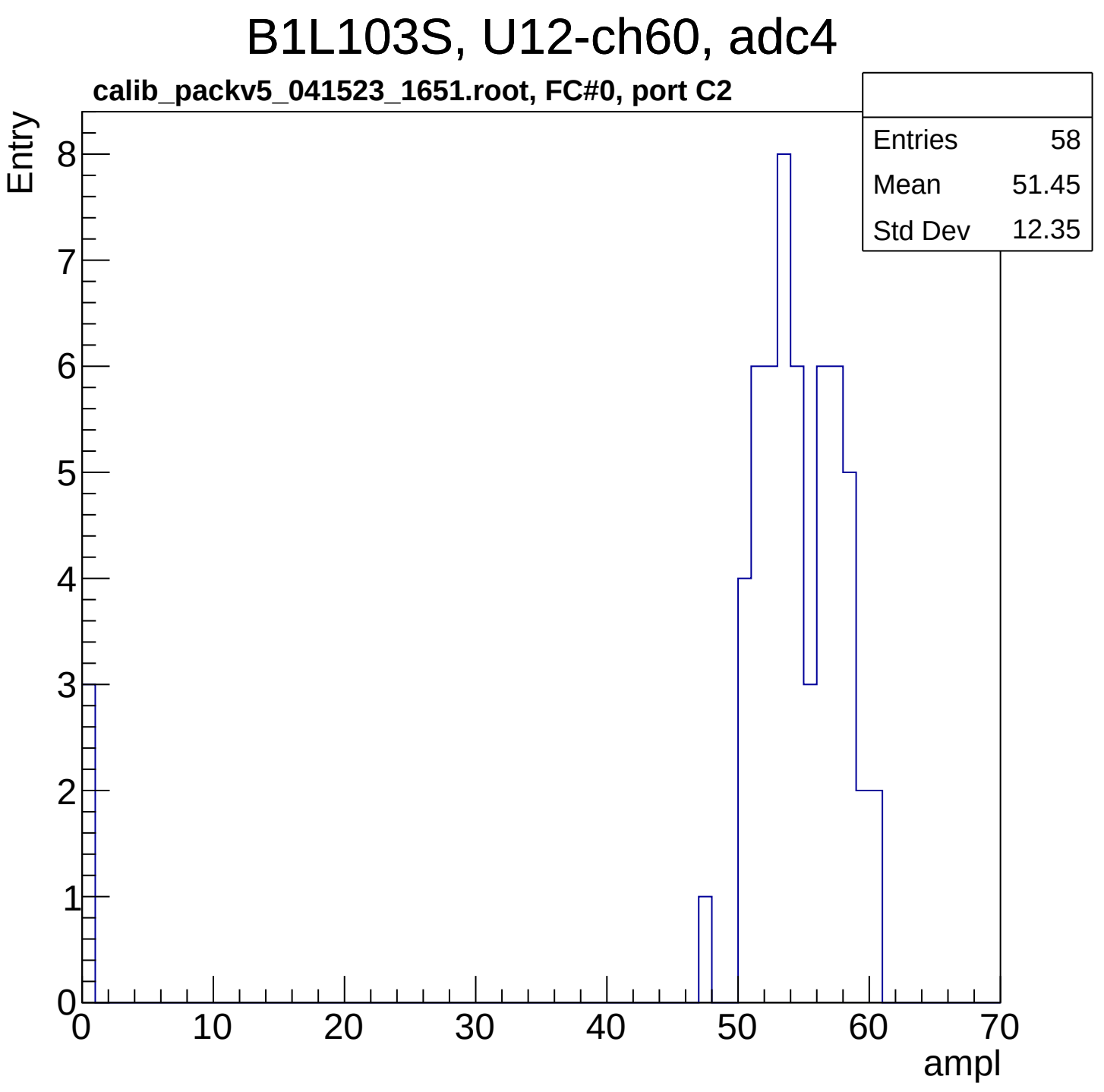
B1L103S, U12-ch60, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 51.45
Std Dev 12.35
Entry
ampl
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2
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4
5
6
7
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0
10
20
30
40
50
60
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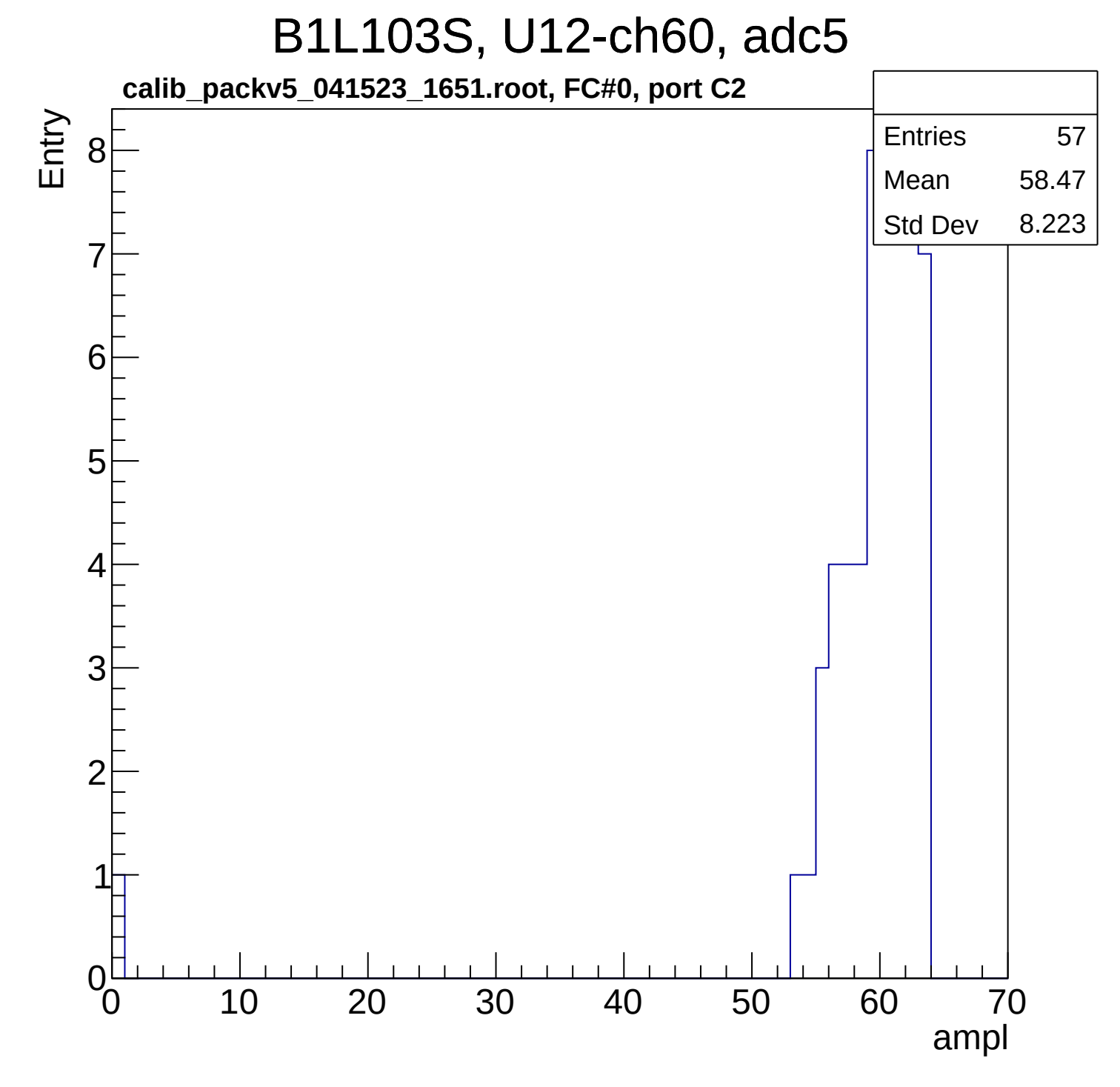
B1L103S, U12-ch60, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.47
Std Dev 8.223
Entry
ampl
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6
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0
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60
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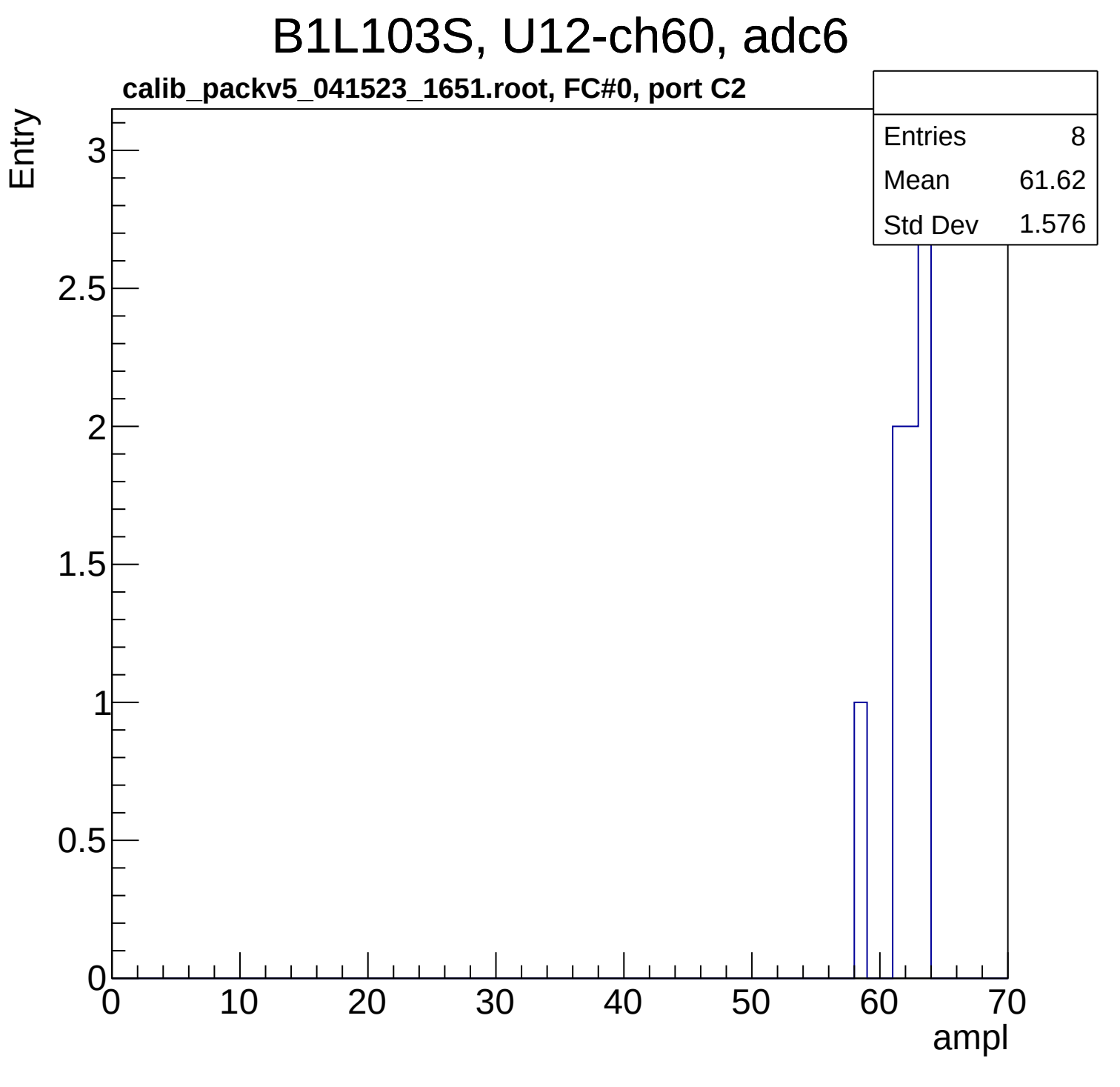
B1L103S, U12-ch60, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.62
Std Dev 1.576
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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40
50
60
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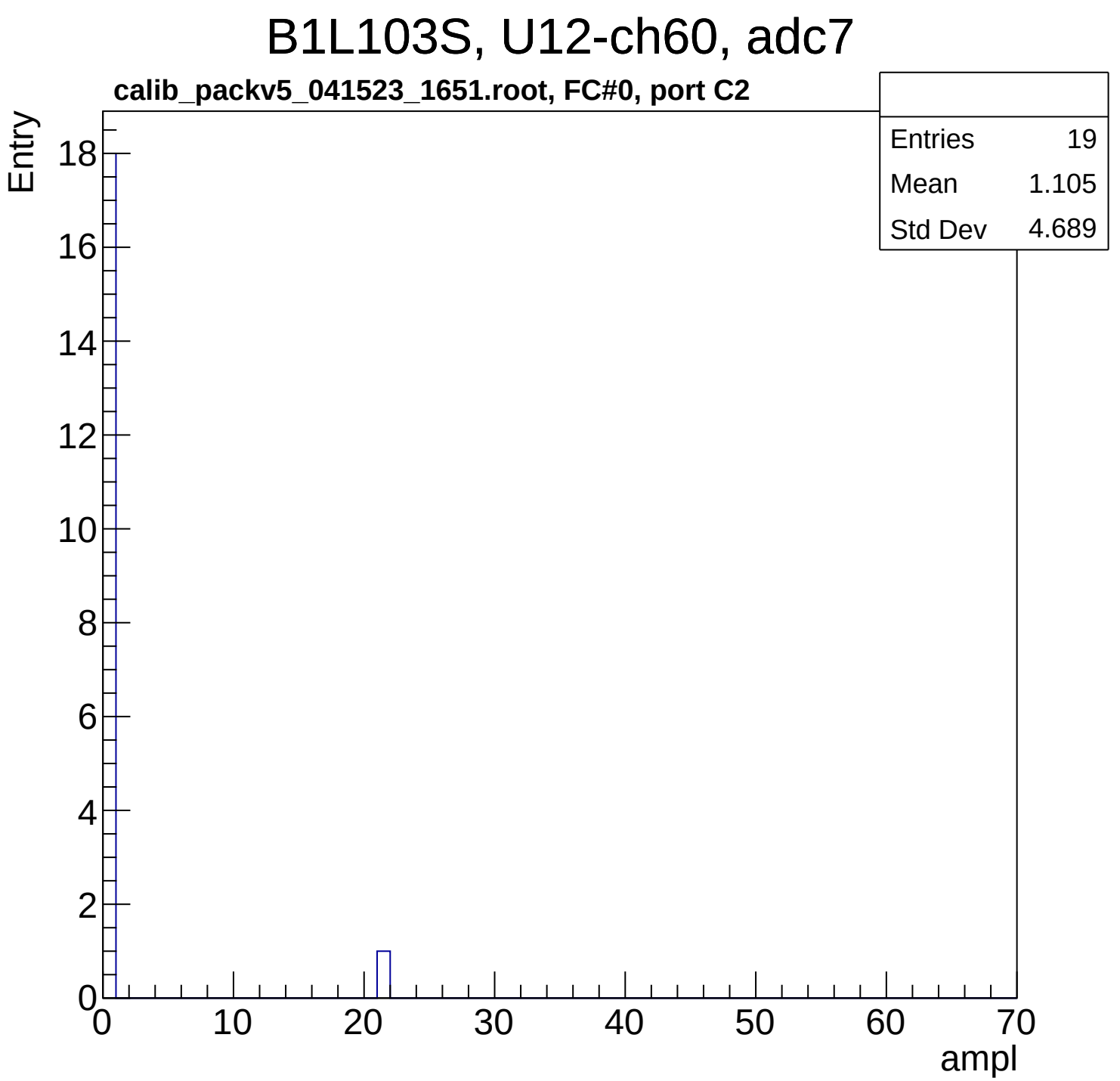
B1L103S, U12-ch60, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
ampl
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10
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14
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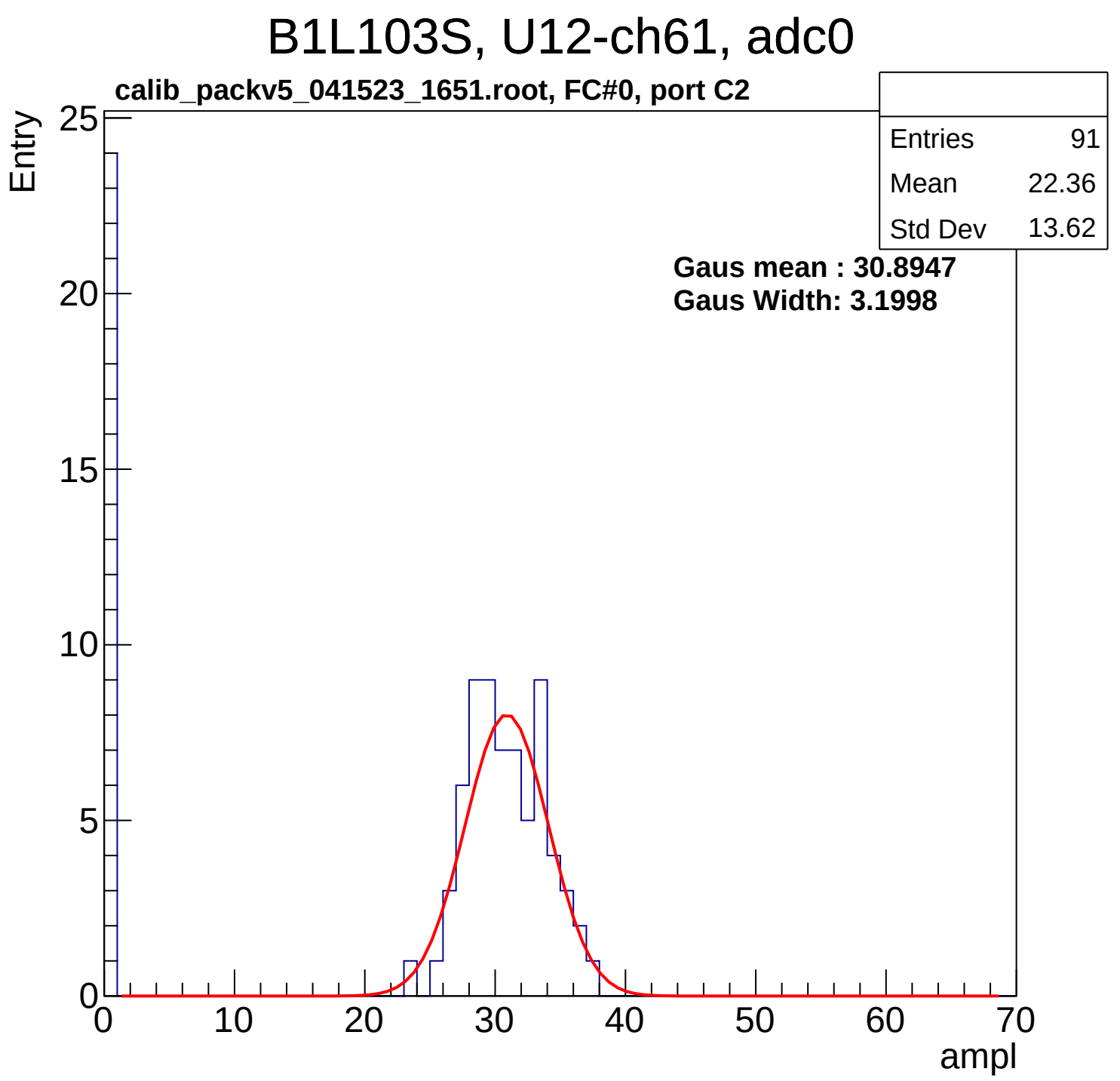
B1L103S, U12-ch61, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 22.36
Std Dev 13.62
Gaus mean : 30.8947
Gaus Width: 3.1998
Entry
ampl
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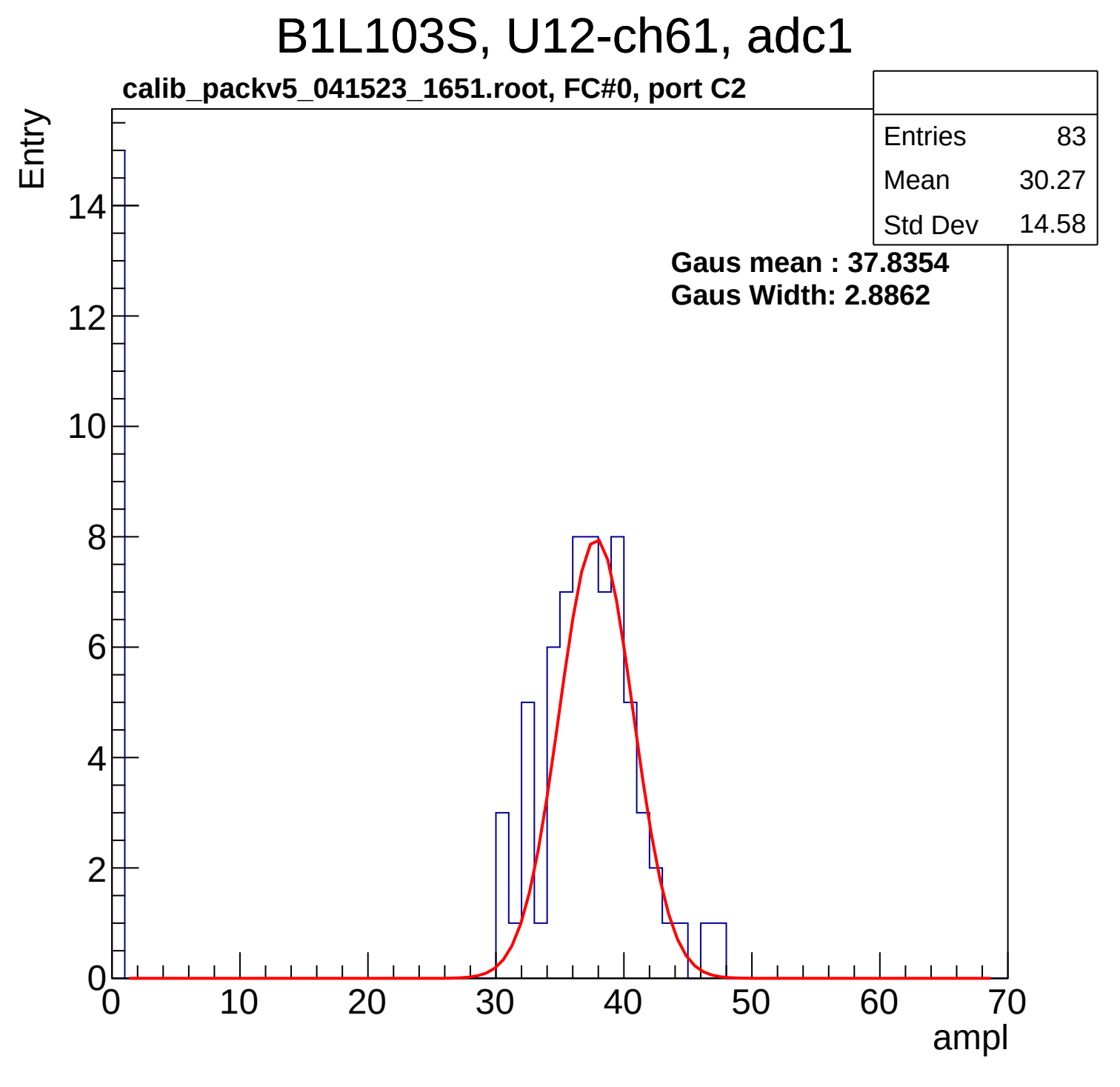
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U12-ch61, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 30.27
Std Dev 14.58
Gaus mean : 37.8354
Gaus Width: 2.8862
Entry
ampl
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4
6
8
10
12
14
0
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20
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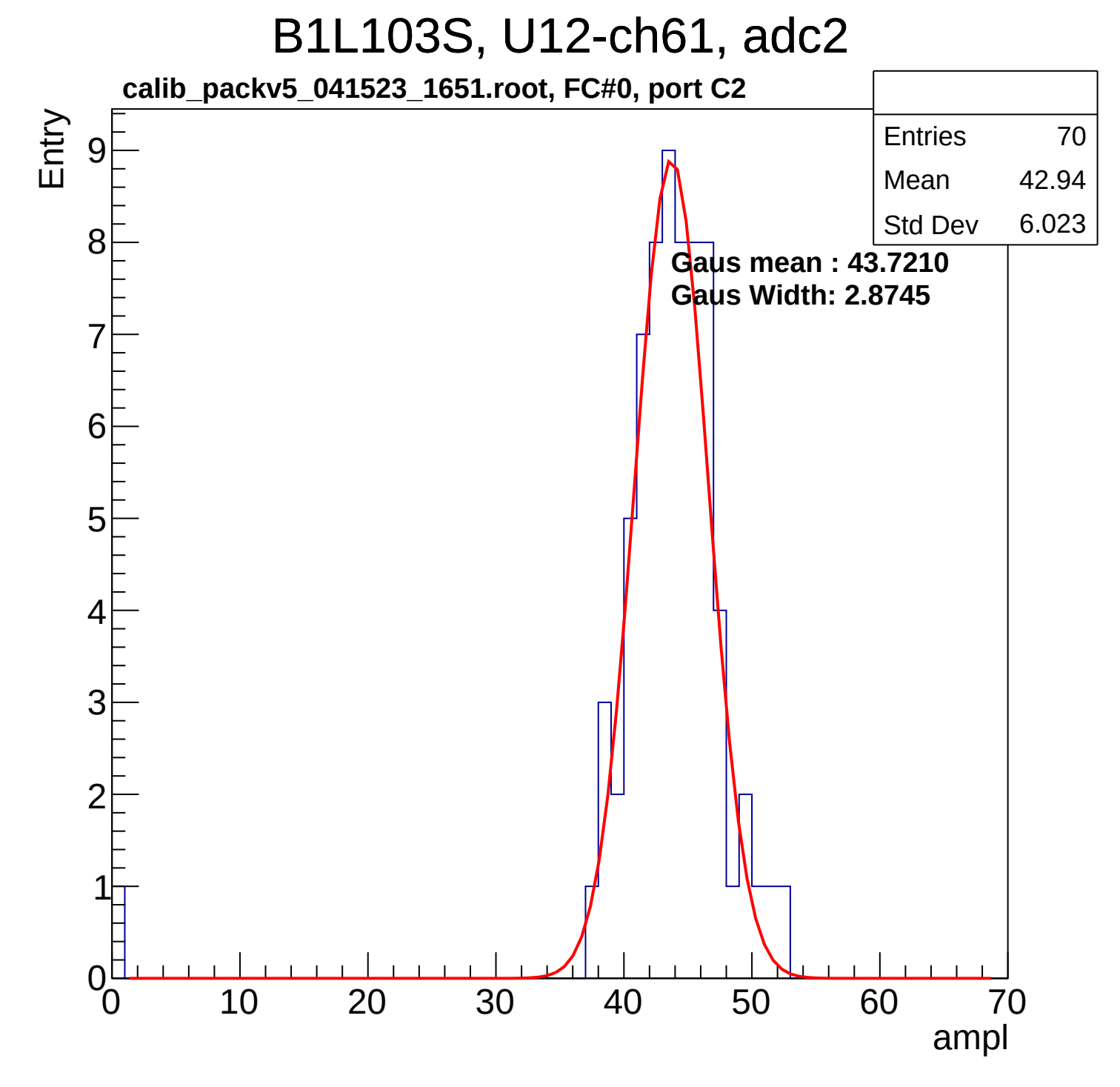
B1L103S, U12-ch61, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 42.94
Std Dev 6.023
Gaus mean : 43.7210
Gaus Width: 2.8745
Entry
ampl
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2
3
4
5
6
7
8
9
0
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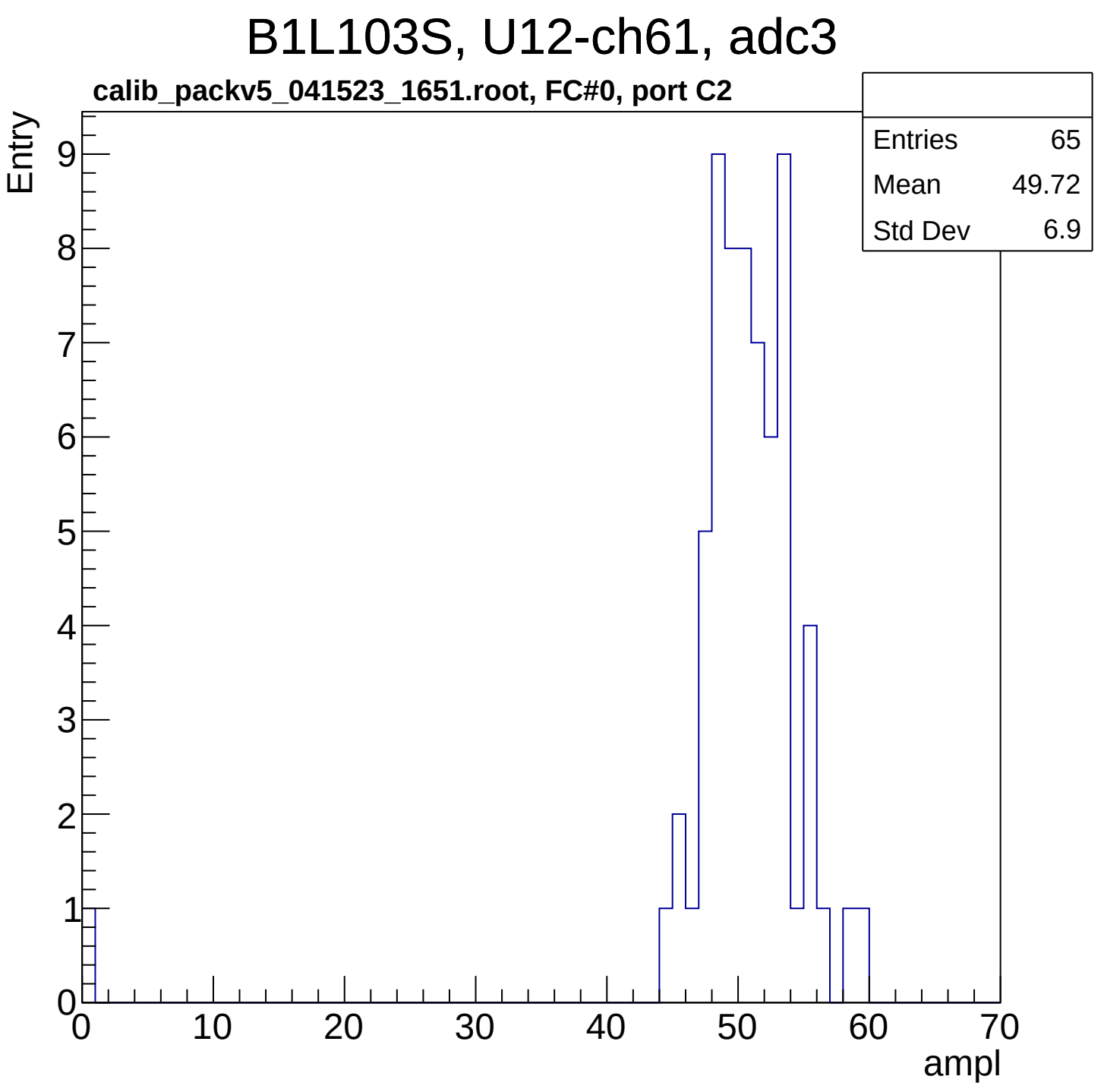
B1L103S, U12-ch61, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 49.72
Std Dev 6.9
Entry
ampl
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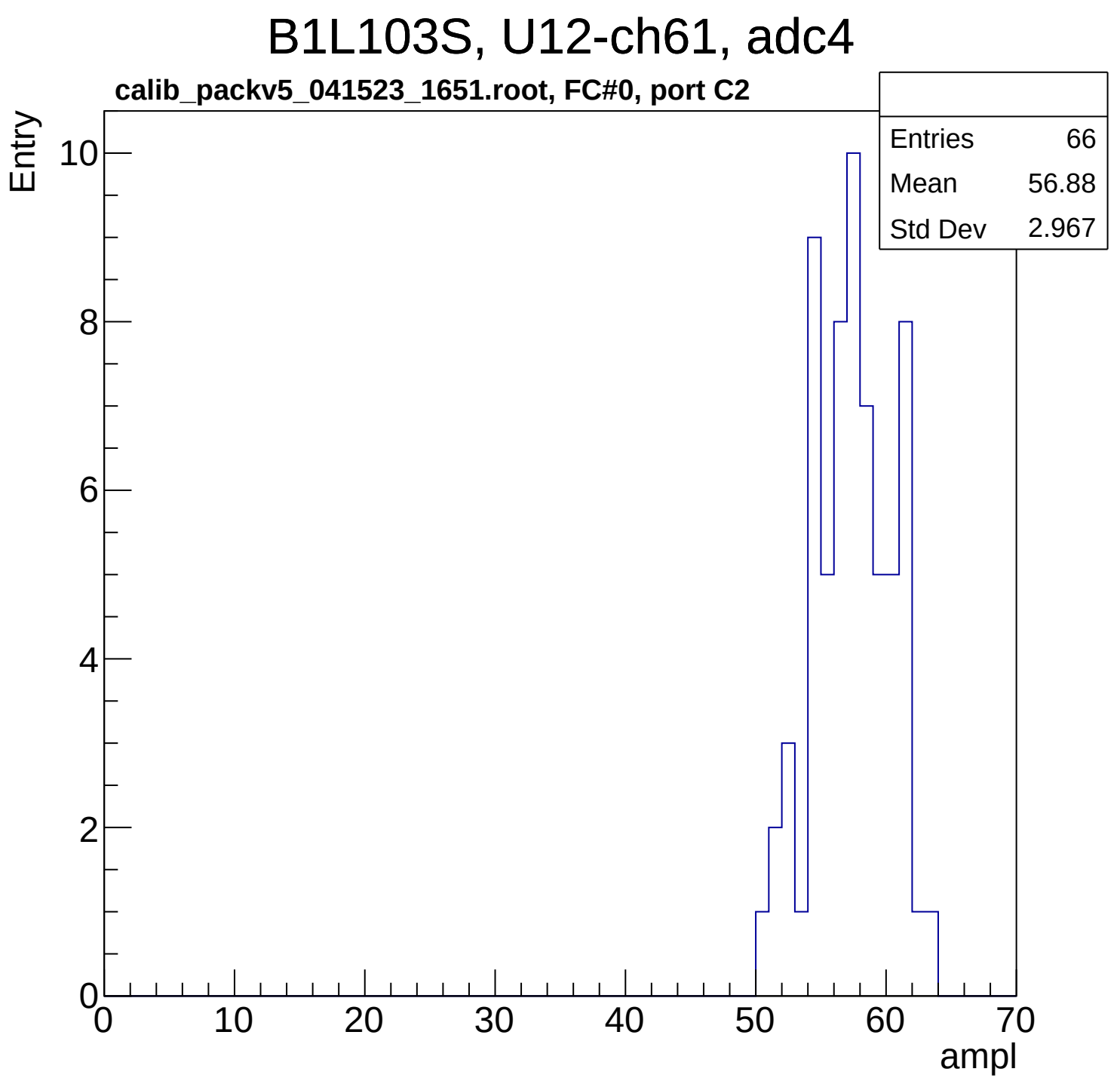
B1L103S, U12-ch61, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 56.88
Std Dev 2.967
Entry
ampl
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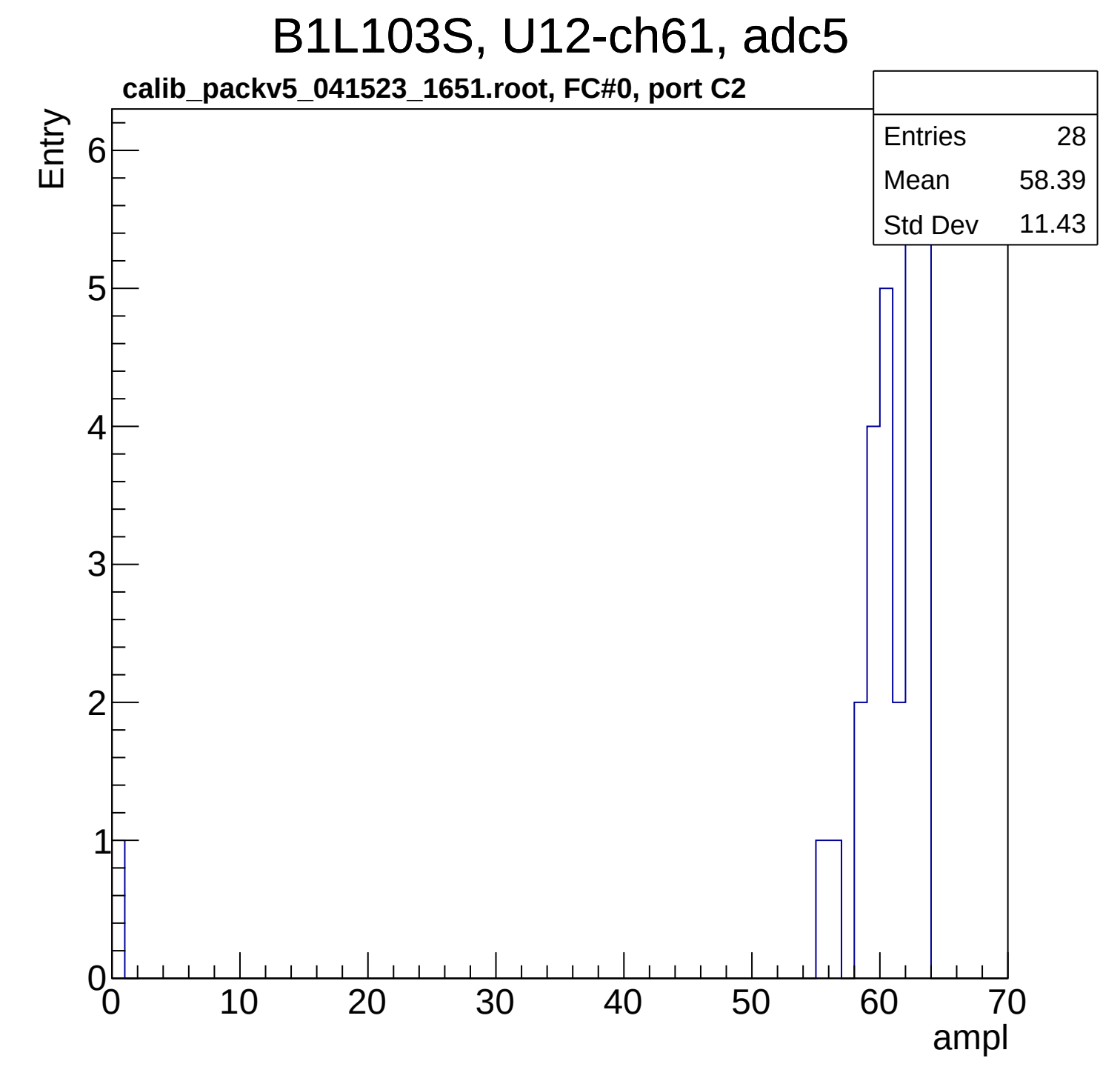
B1L103S, U12-ch61, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 28
Mean 58.39
Std Dev 11.43
Entry
ampl
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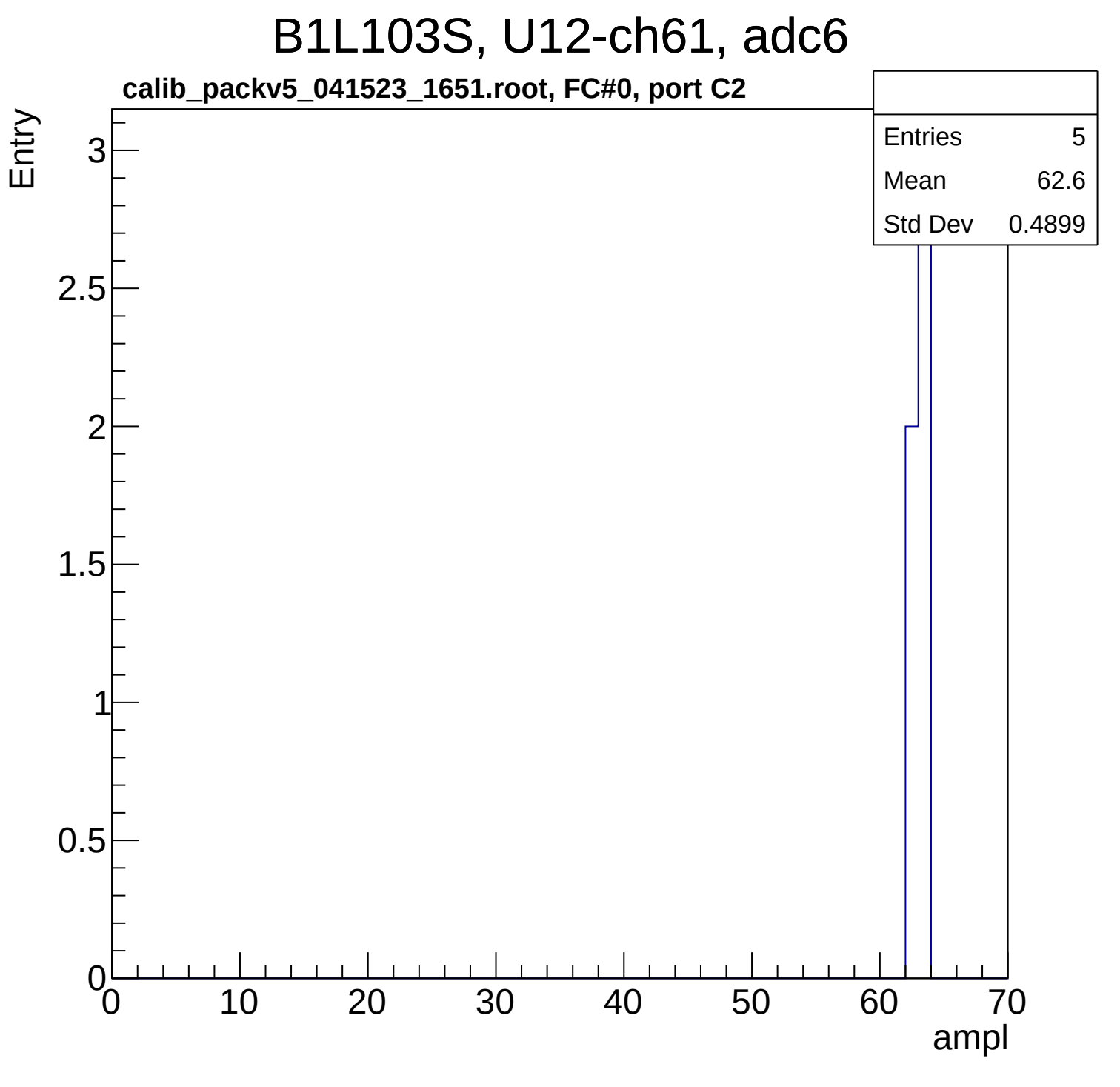
B1L103S, U12-ch61, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.6
Std Dev 0.4899
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
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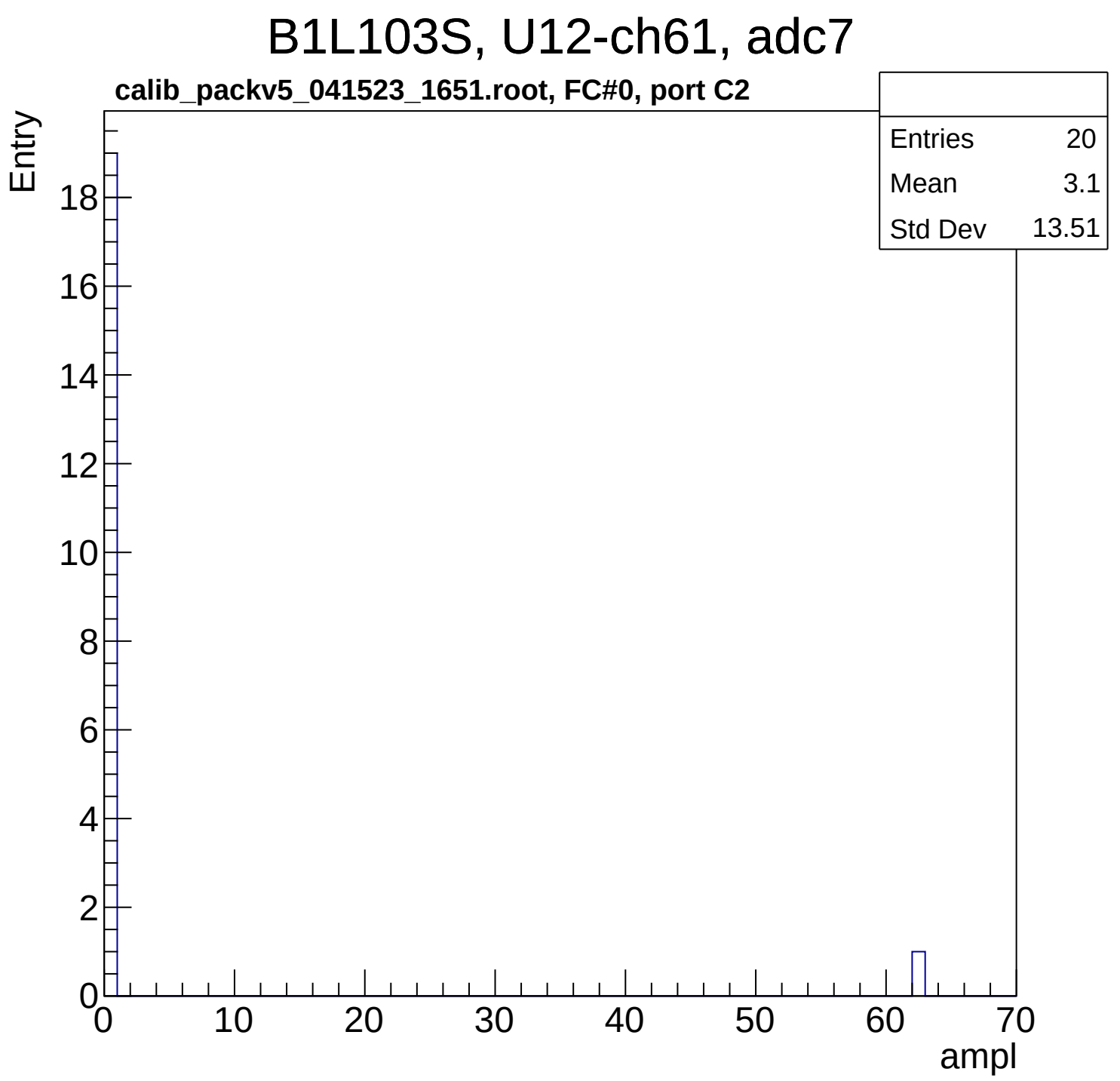
40
50
60
70


B1L103S, U12-ch61, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
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4
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16
18
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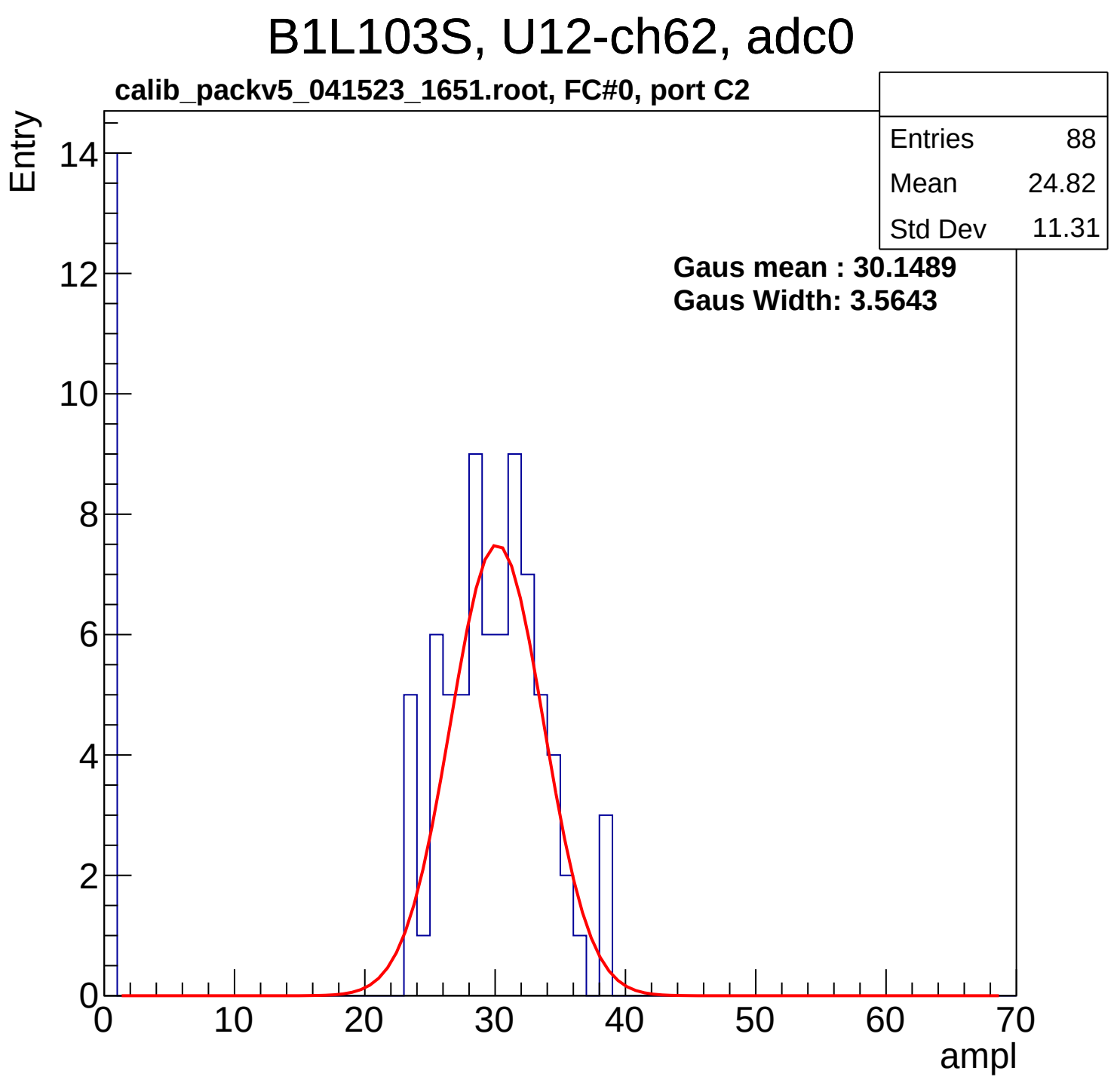
60
70
ampl


B1L103S, U12-ch62, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 24.82
Std Dev 11.31
Gaus mean : 30.1489
Gaus Width: 3.5643
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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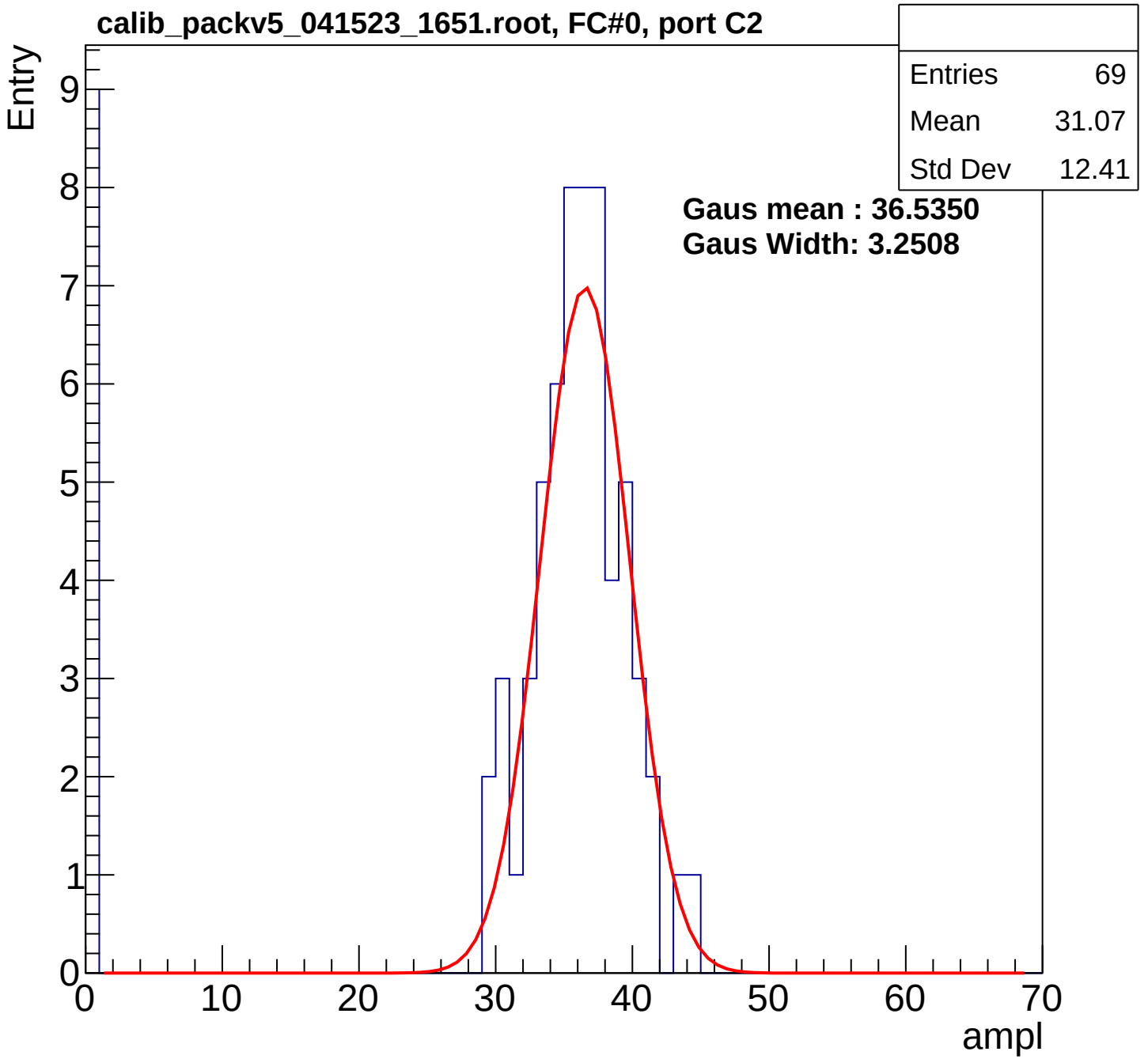
B1L103S, U12-ch62, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 31.07
Std Dev 12.41
Gaus mean : 36.5350
Gaus Width: 3.2508
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
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30
40
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60
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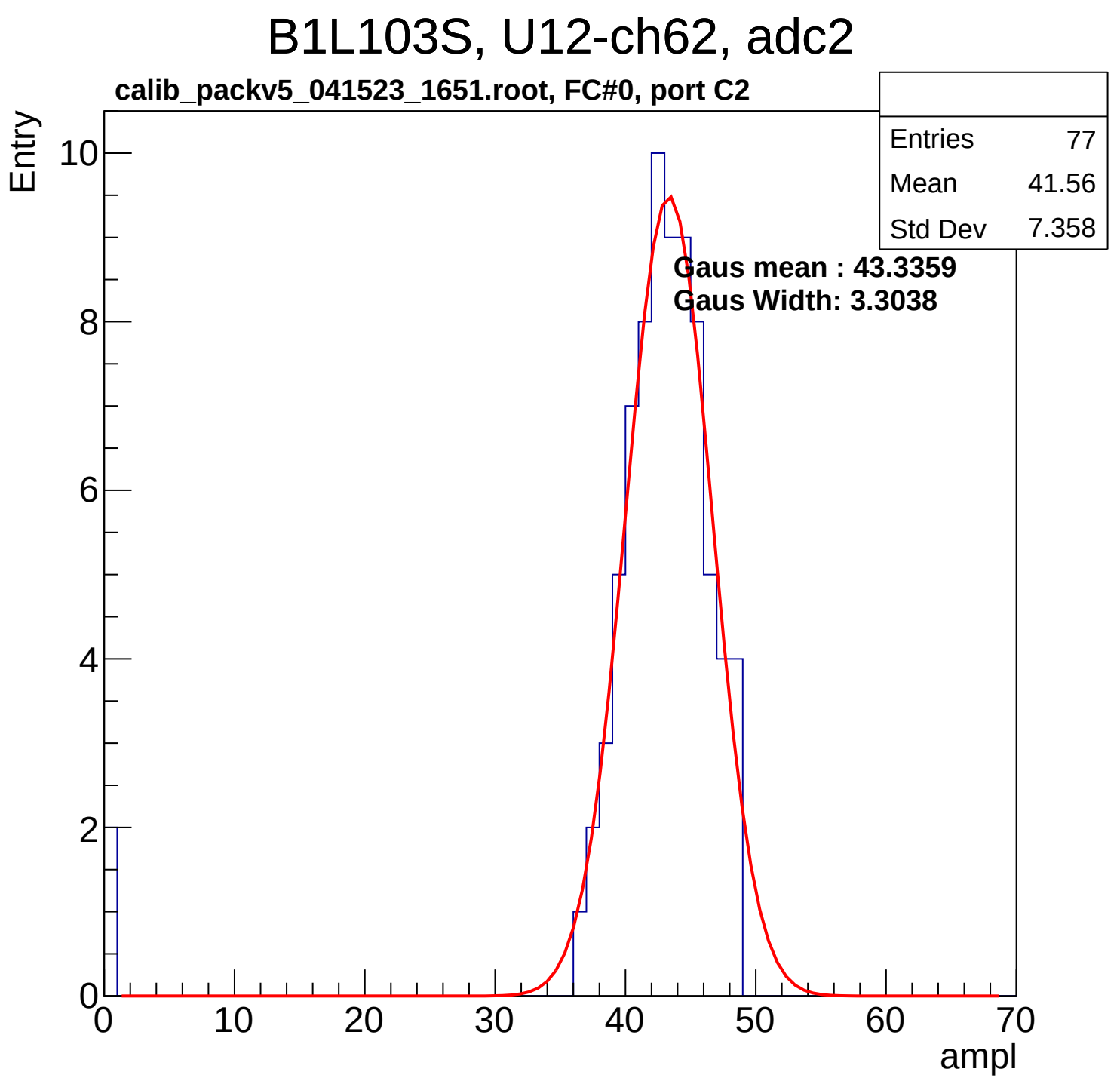
B1L103S, U12-ch62, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 41.56
Std Dev 7.358
Gaus mean : 43.3359
Gaus Width: 3.3038
Entry
ampl
0
2
4
6
8
10
0
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20
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40
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60
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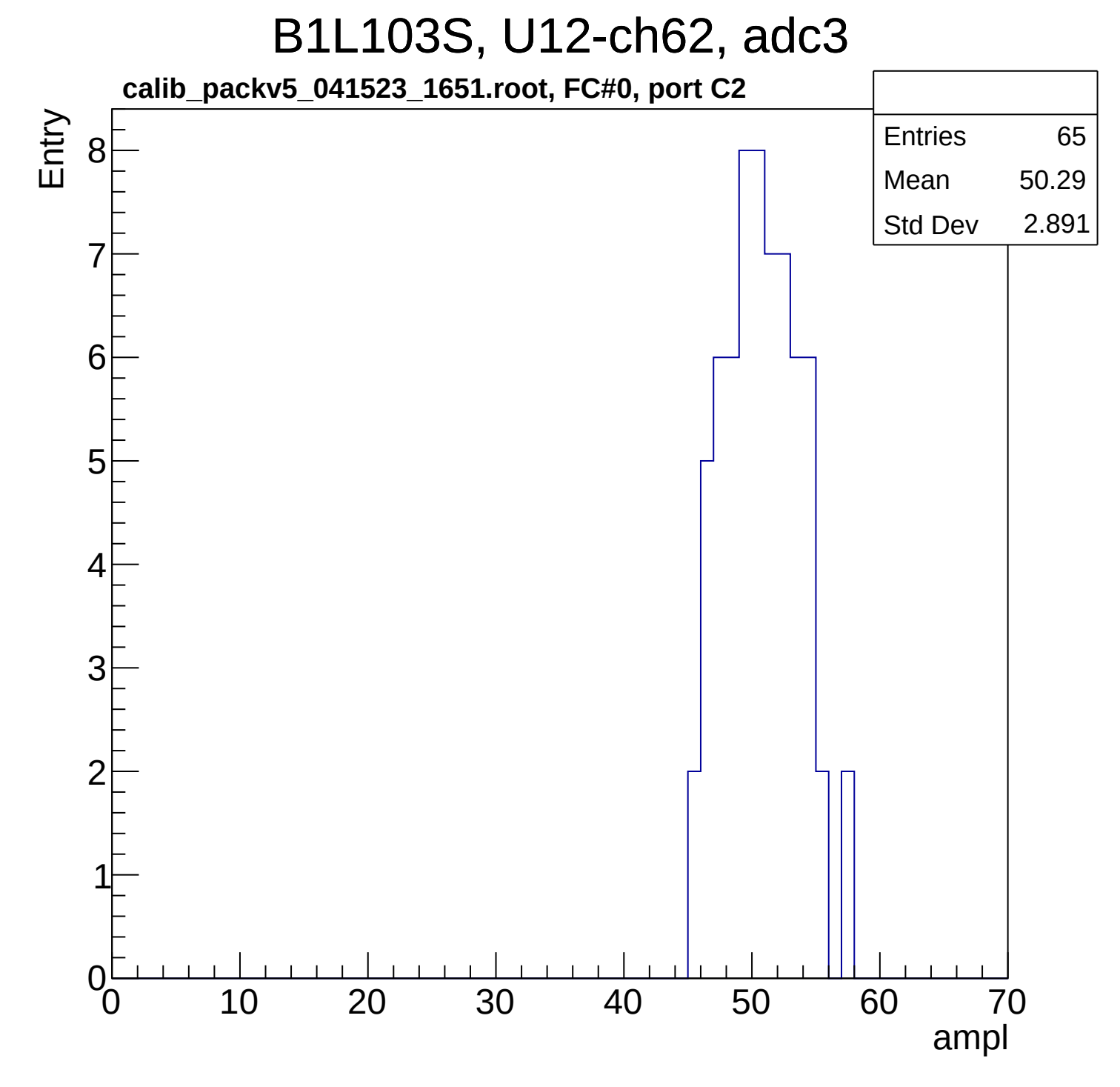
B1L103S, U12-ch62, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 50.29
Std Dev 2.891
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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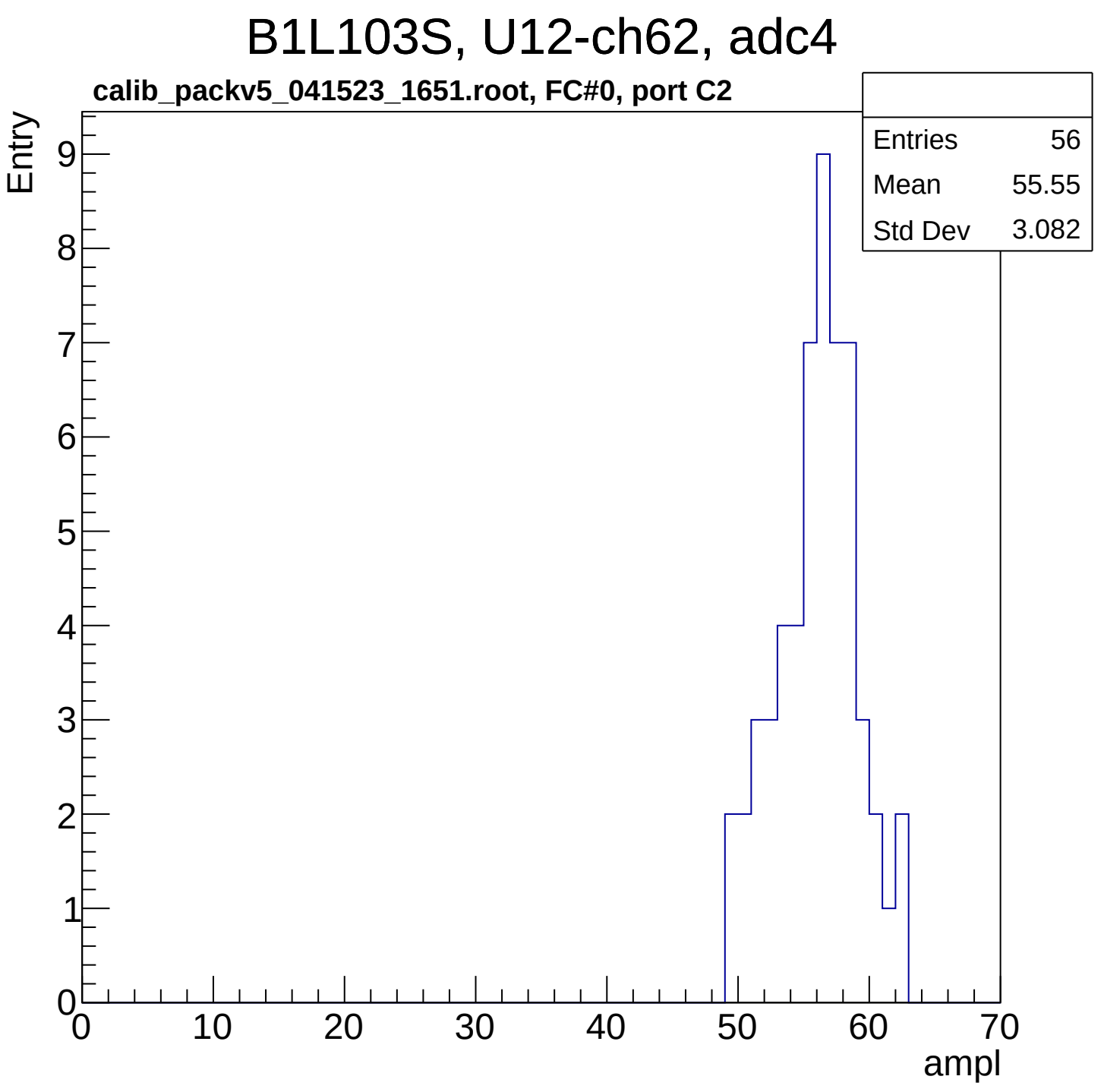
B1L103S, U12-ch62, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 55.55
Std Dev 3.082
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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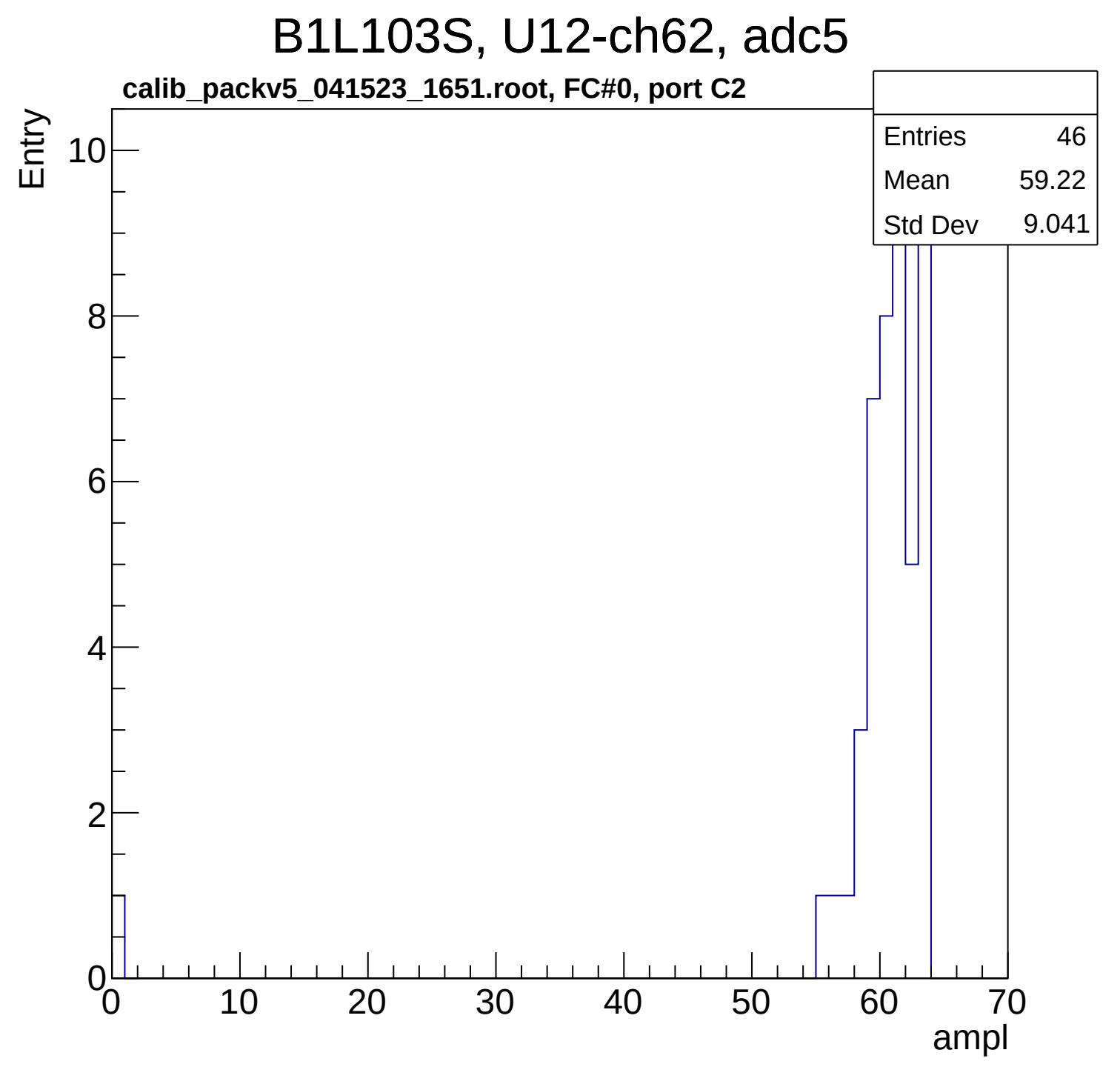
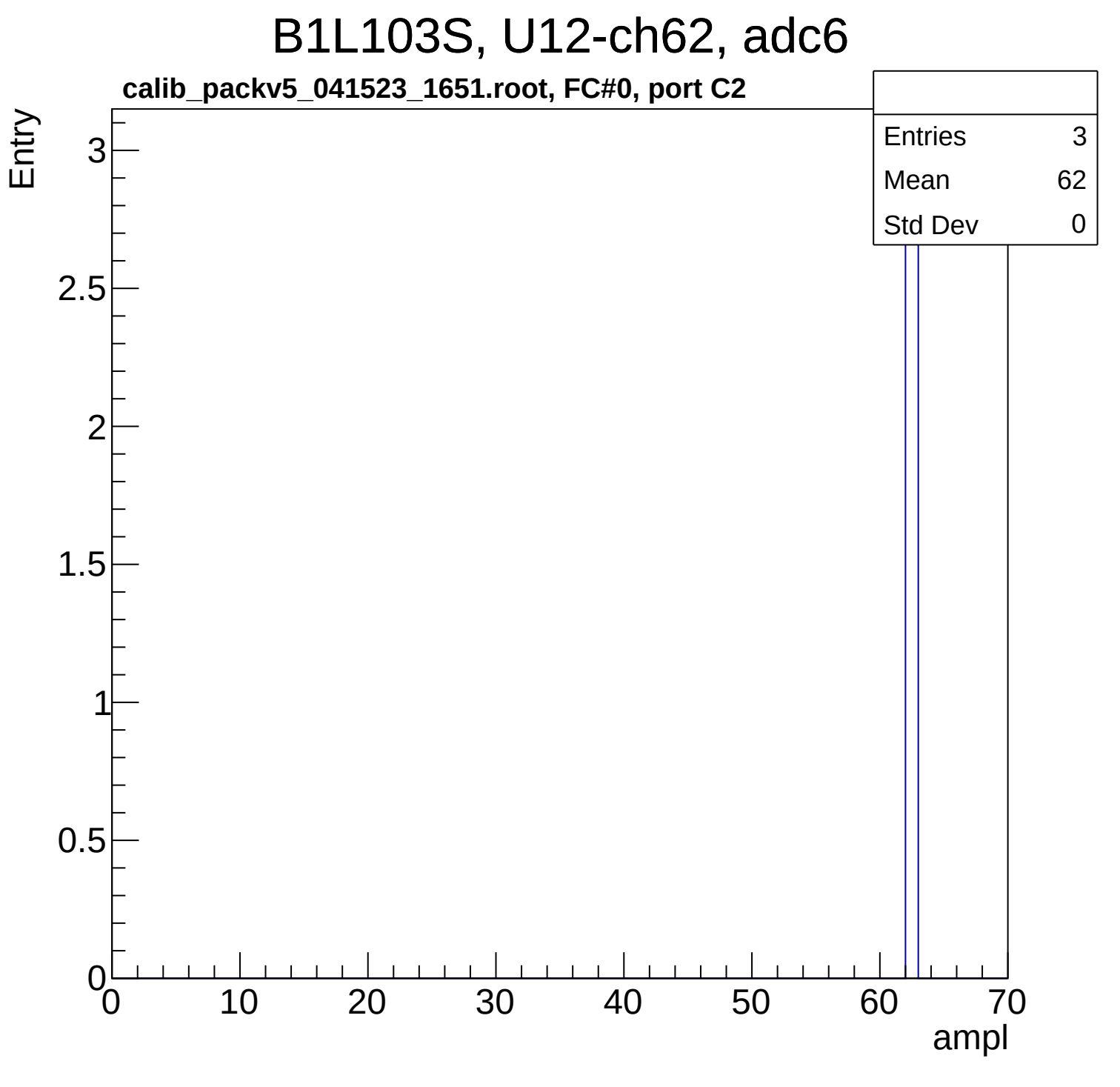
40
50
60
70


B1L103S, U12-ch62, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 59.22
Std Dev 9.041
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch62, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62
Std Dev 0
Entry
ampl
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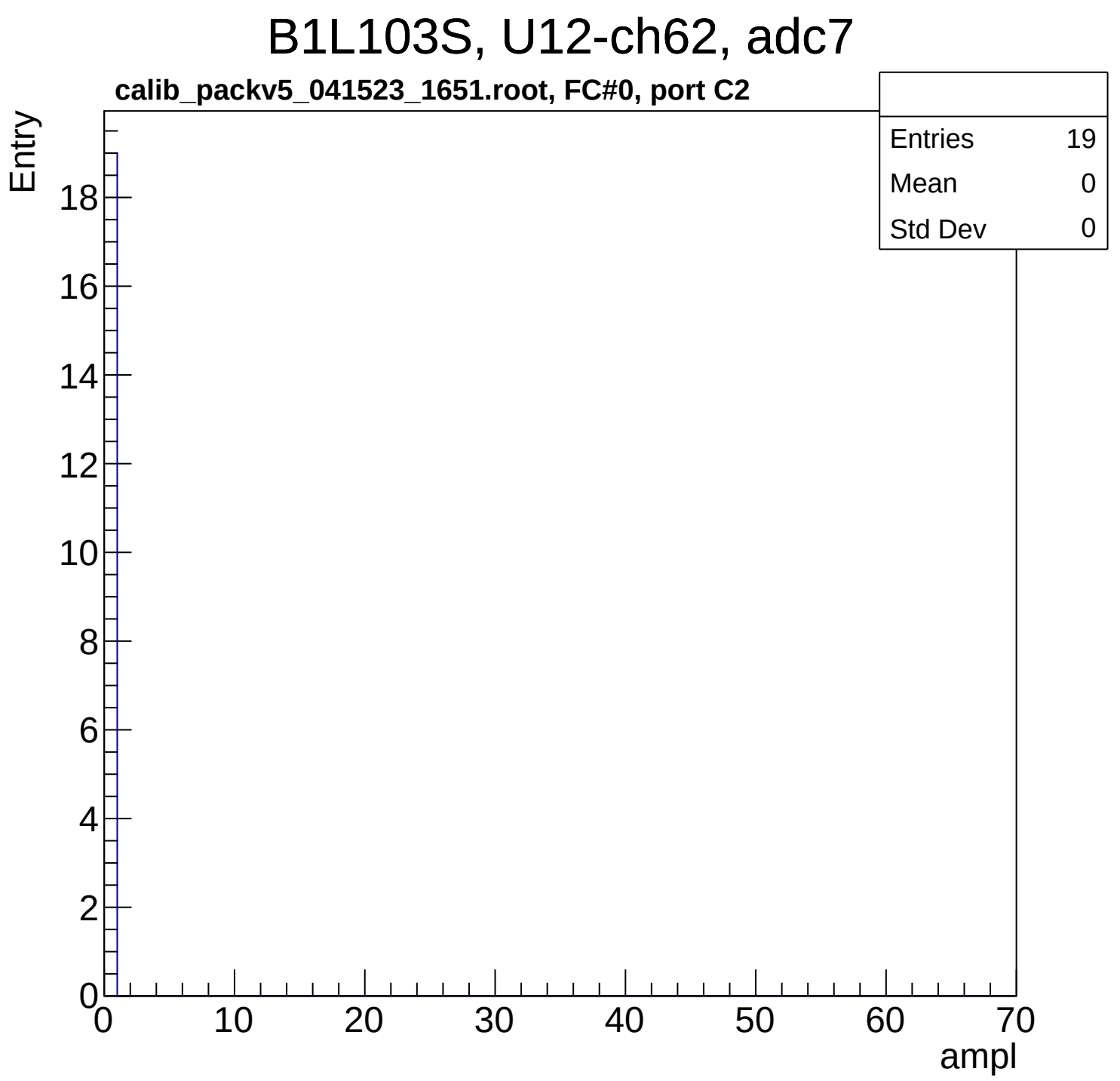
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U12-ch62, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
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18
0
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20
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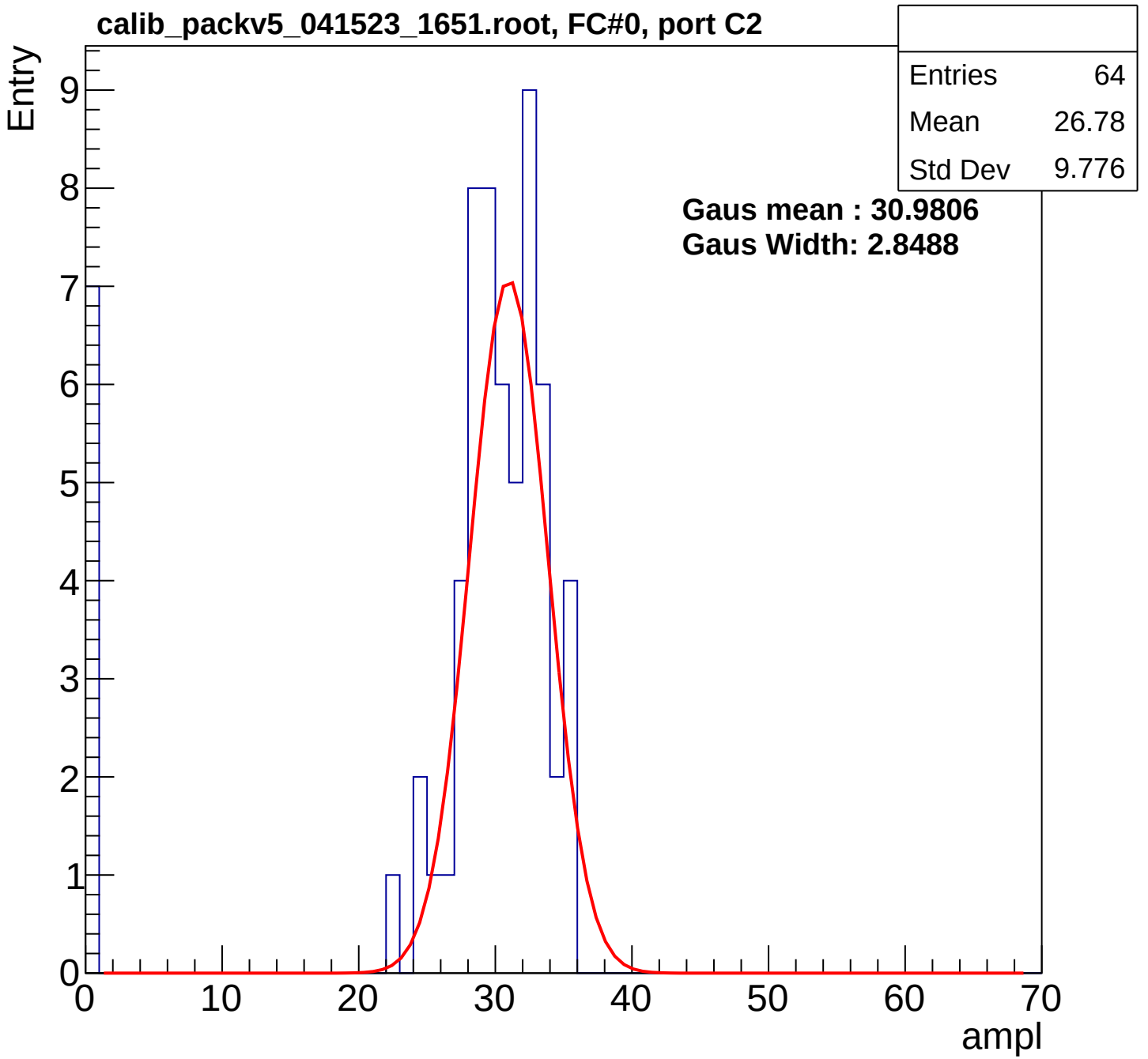
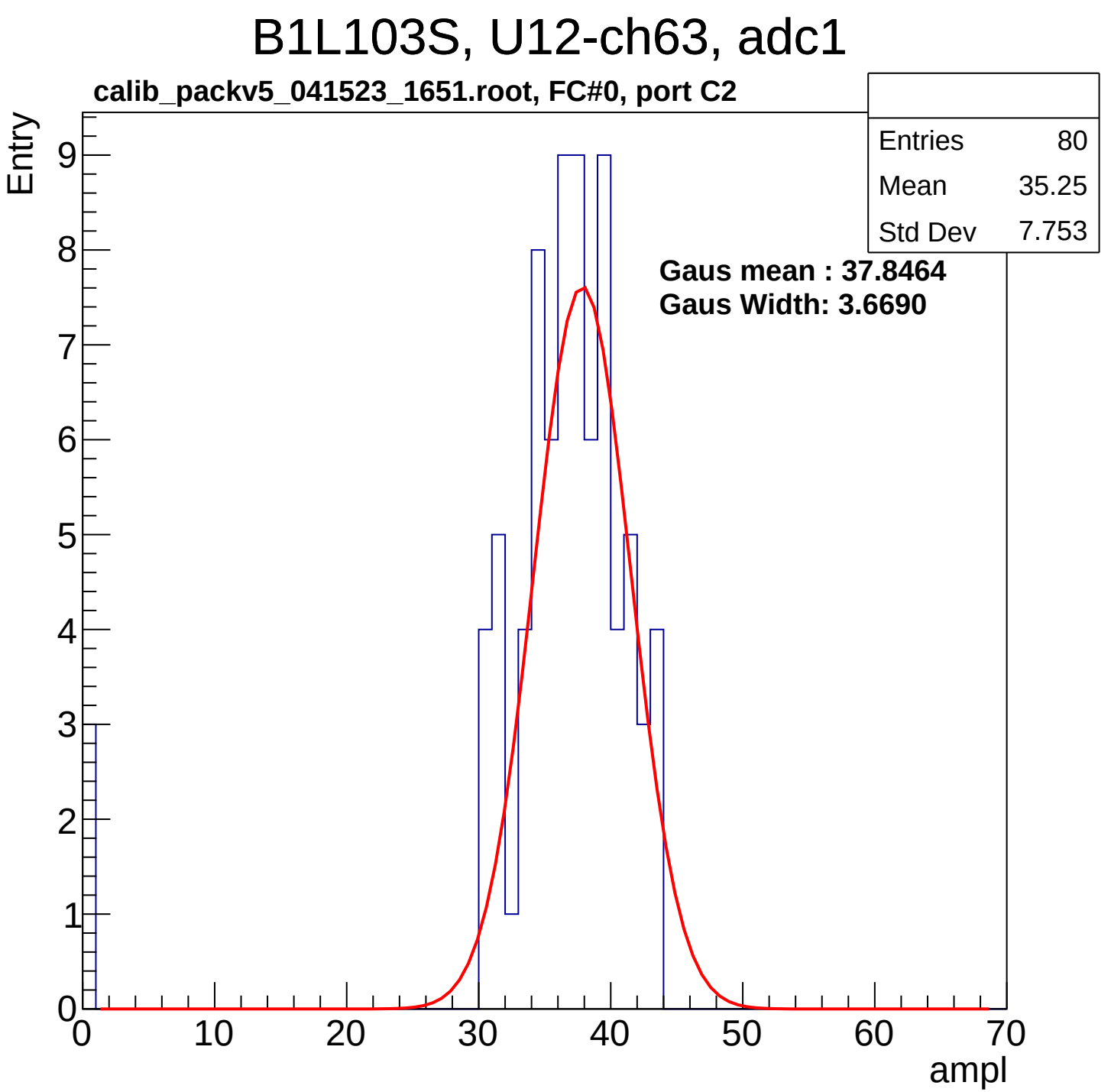
50
60
70
ampl


B1L103S, U12-ch63, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 26.78
Std Dev 9.776
Gaus mean : 30.9806
Gaus Width: 2.8488
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch63, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 35.25
Std Dev 7.753
Gaus mean : 37.8464
Gaus Width: 3.6690
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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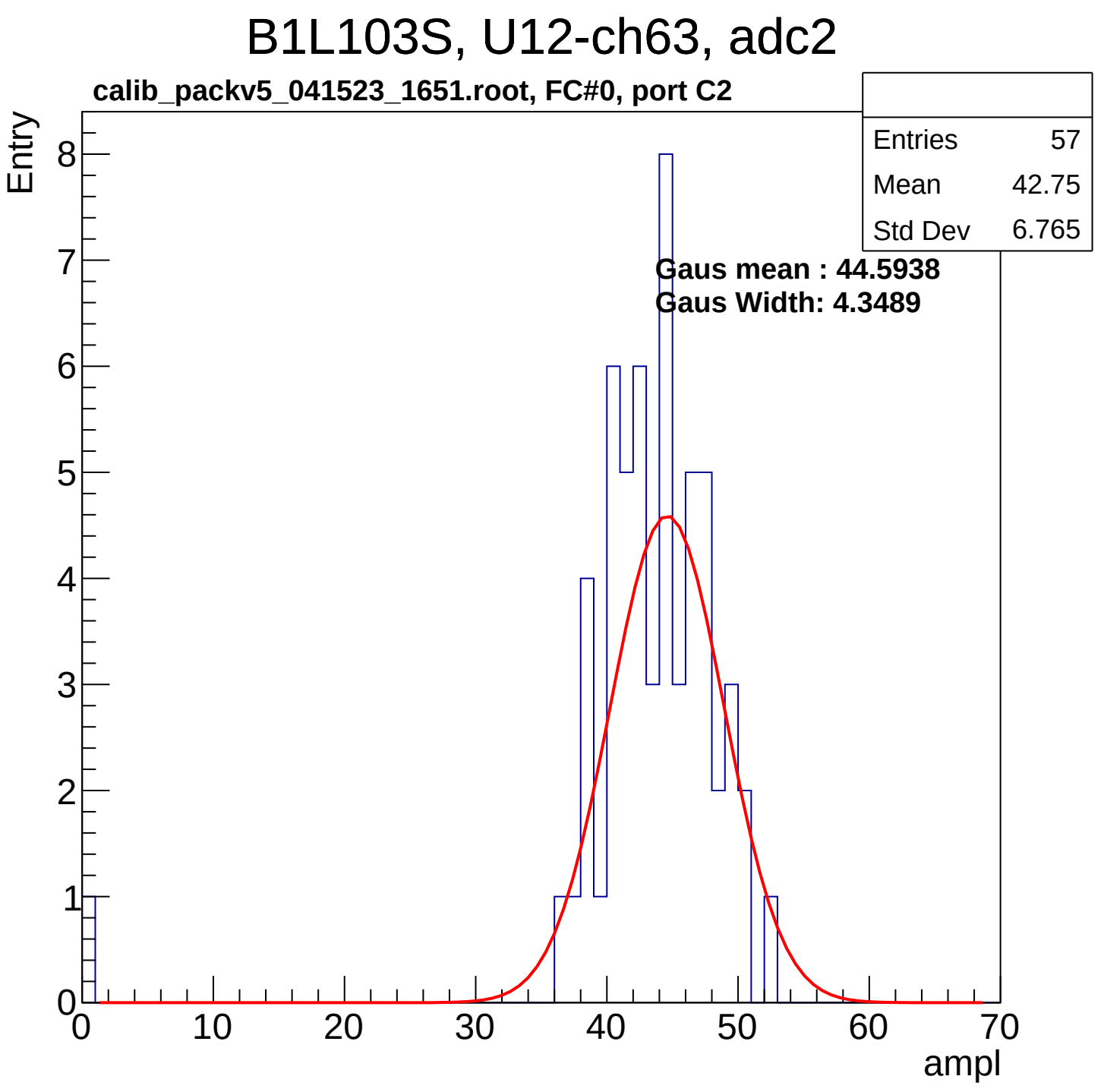
B1L103S, U12-ch63, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 42.75
Std Dev 6.765
Gaus mean : 44.5938
Gaus Width: 4.3489
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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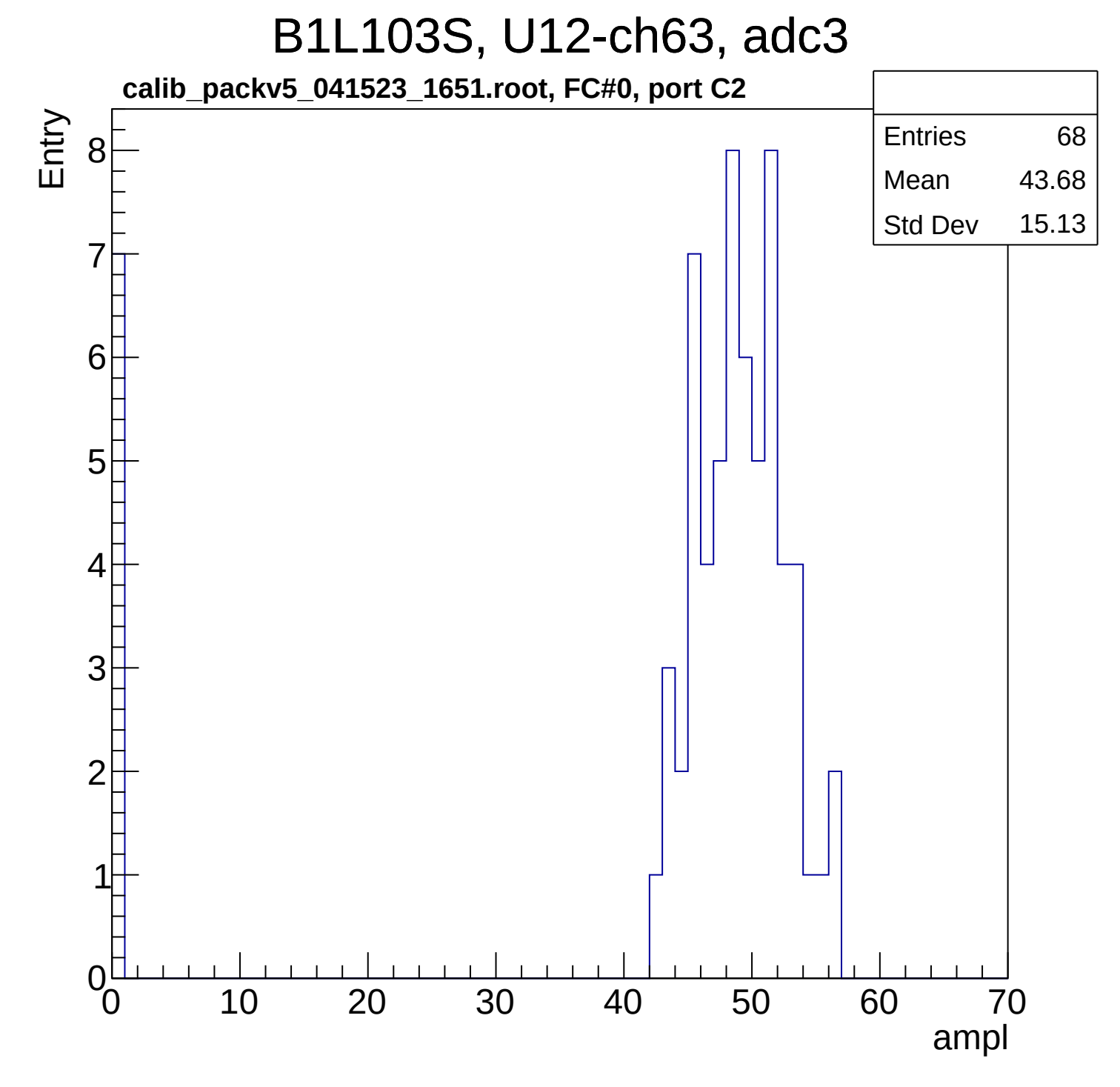
B1L103S, U12-ch63, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 43.68
Std Dev 15.13
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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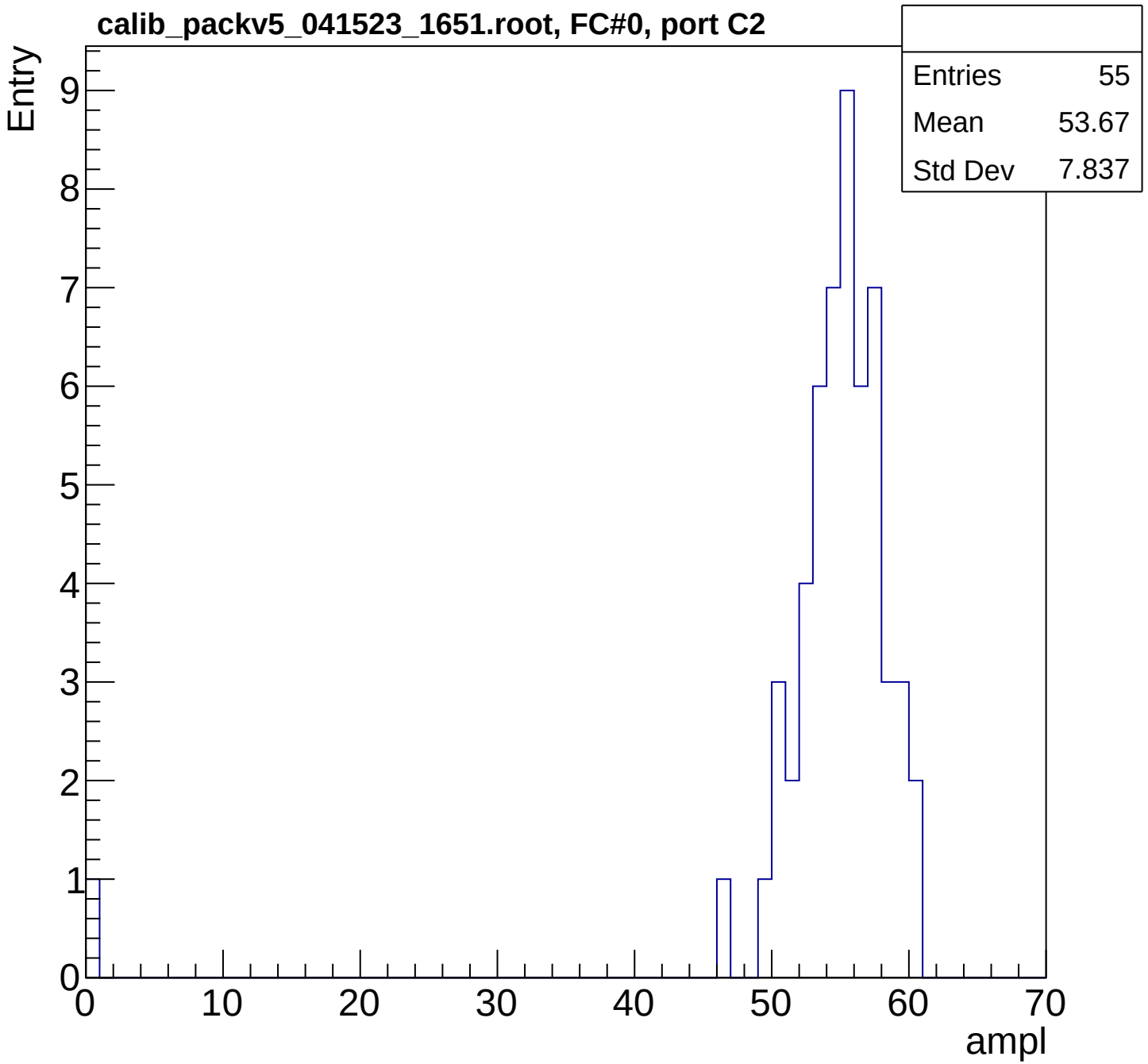
B1L103S, U12-ch63, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 53.67
Std Dev 7.837
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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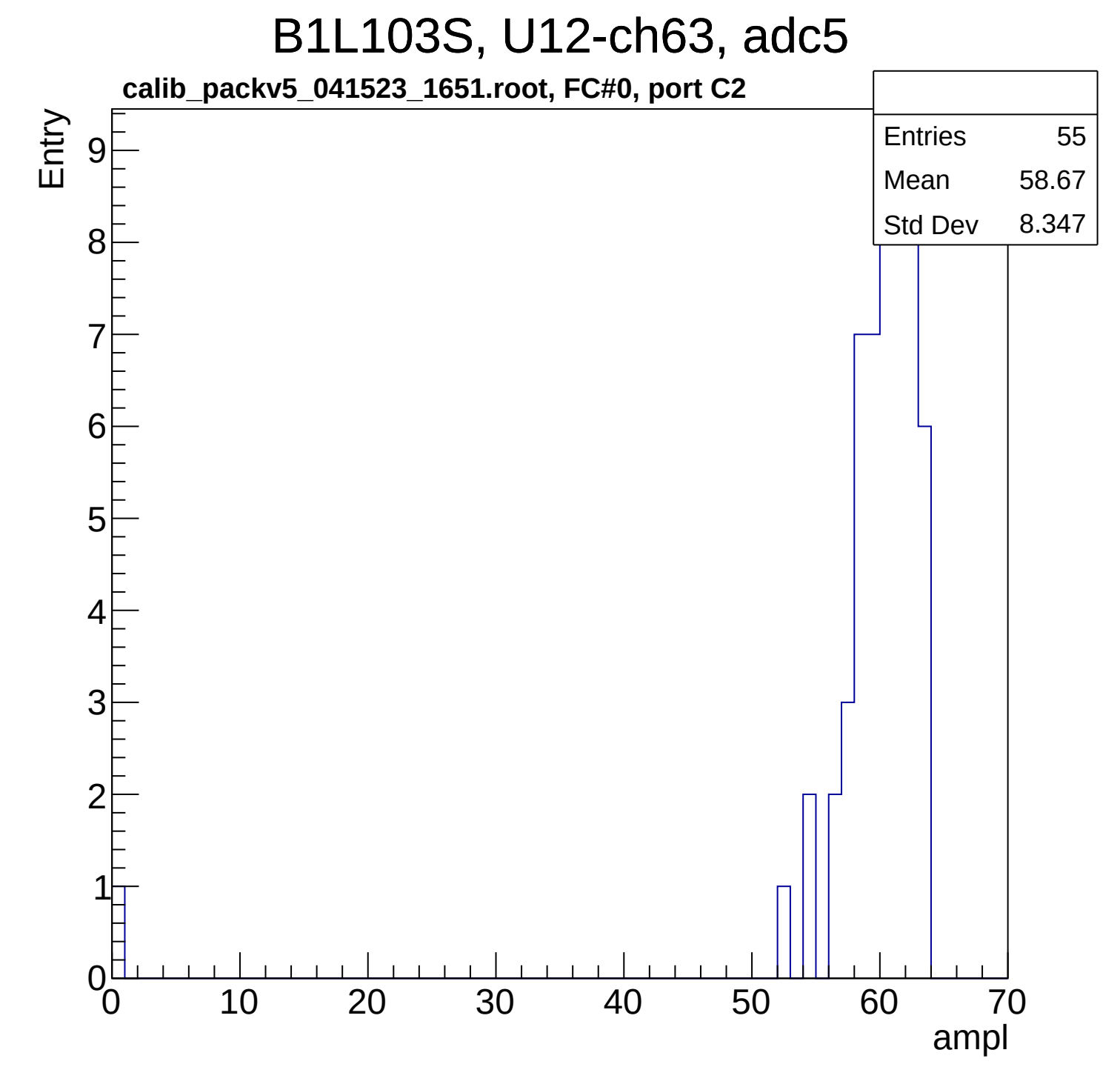
B1L103S, U12-ch63, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.67
Std Dev 8.347
Entry
ampl
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3
4
5
6
7
8
9
0
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60
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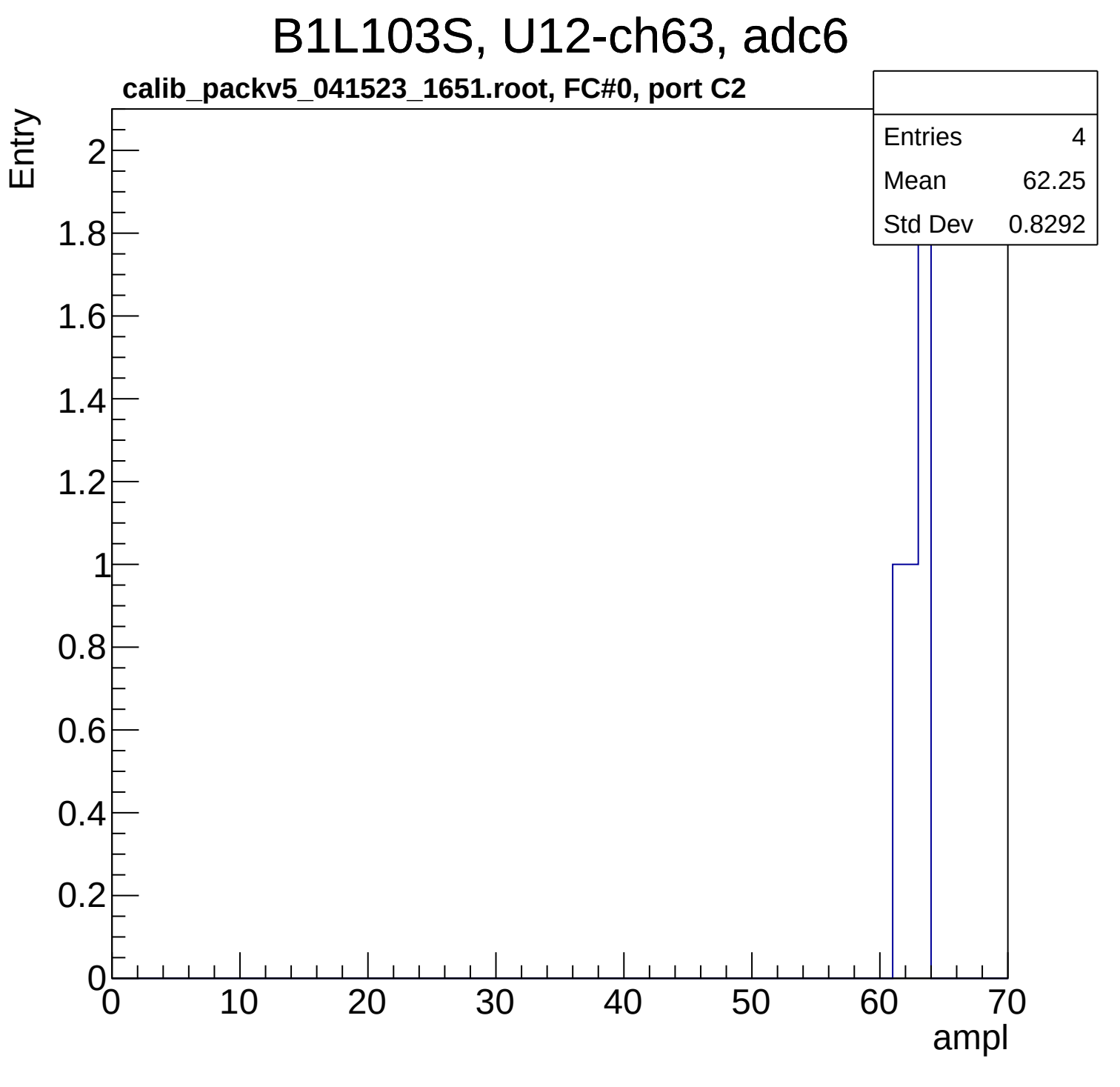
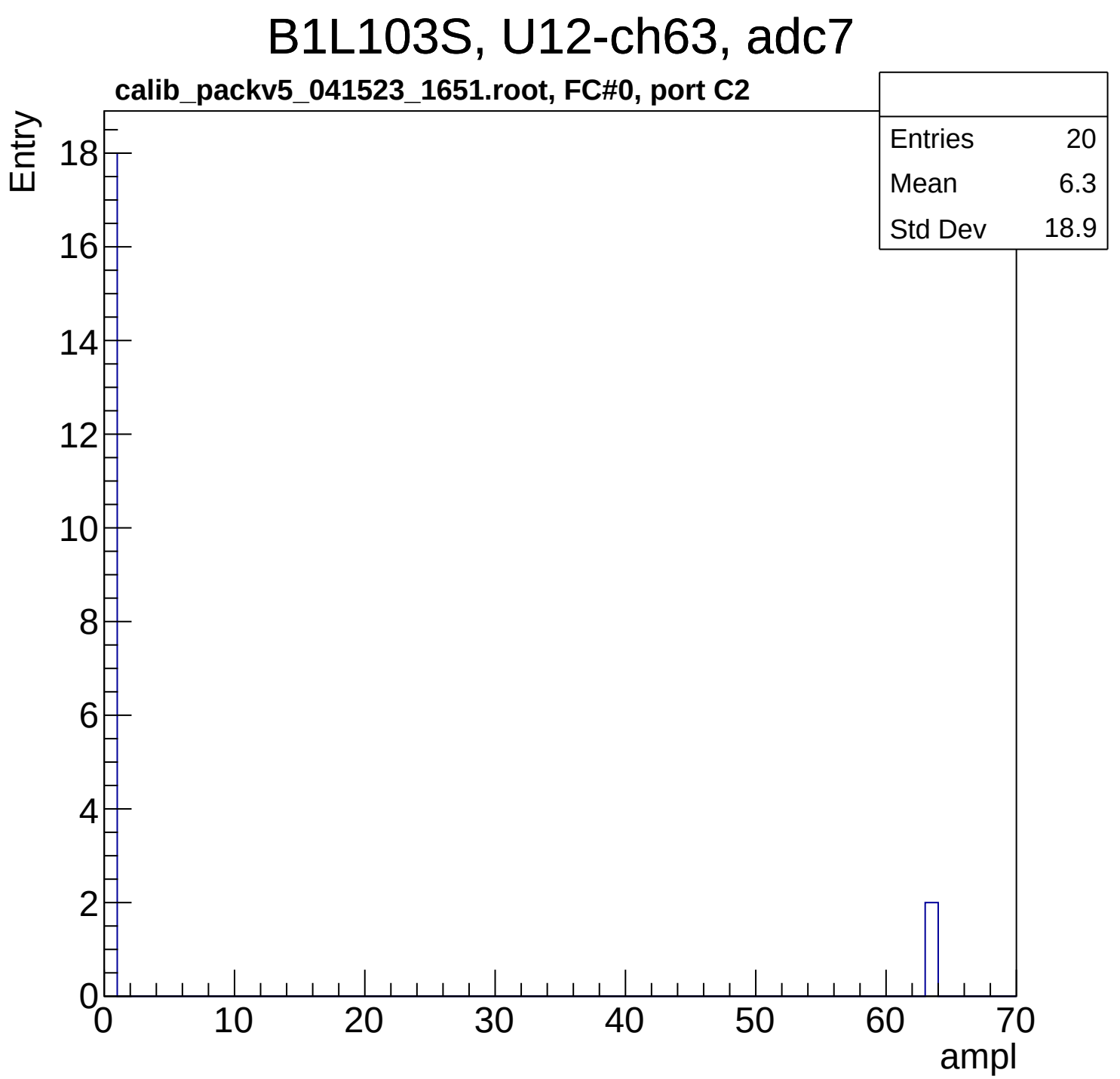

B1L103S, U12-ch63, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U12-ch63, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.3
Std Dev 18.9
Entry
0
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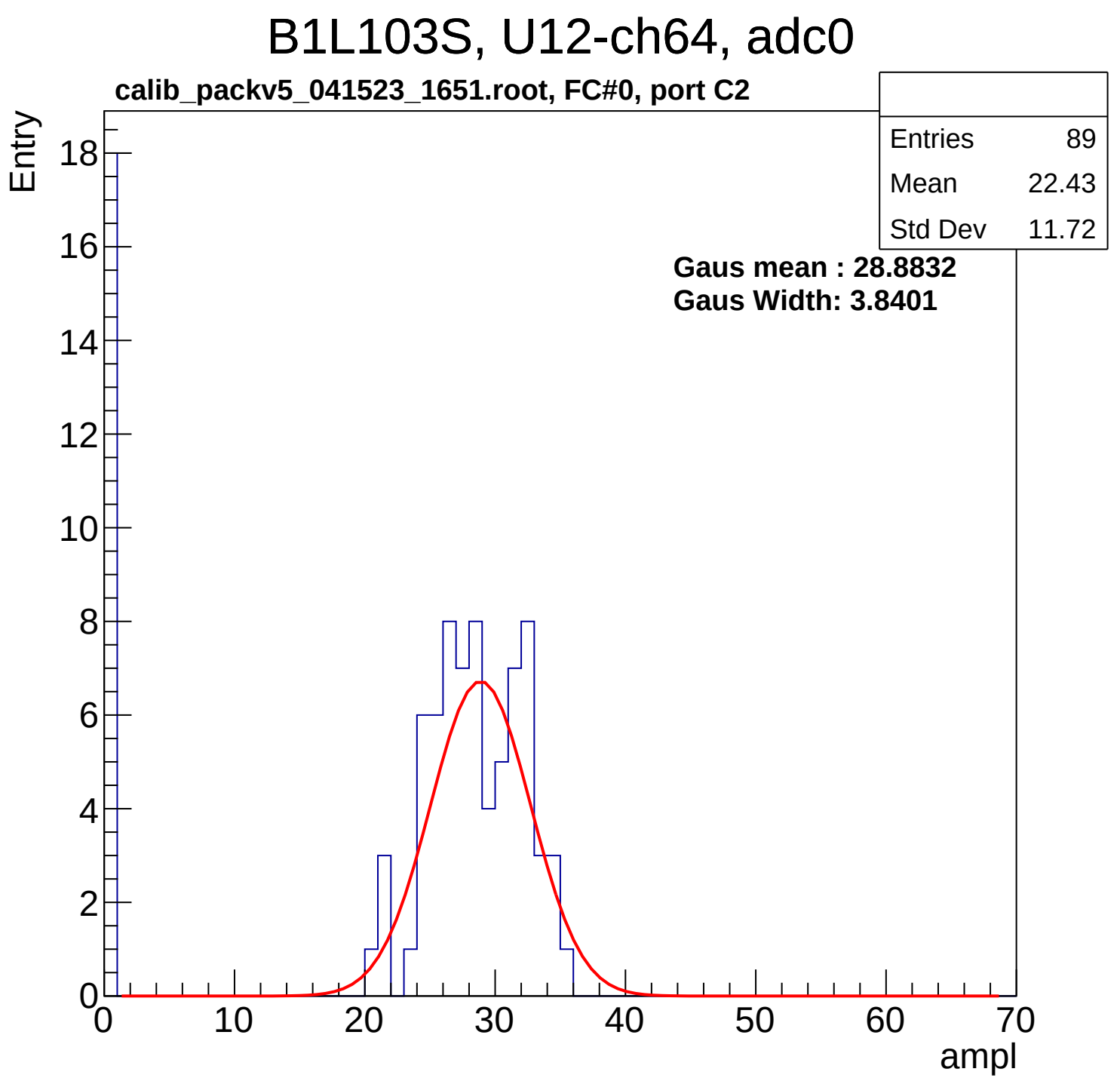
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch64, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 89
Mean 22.43
Std Dev 11.72
Gaus mean : 28.8832
Gaus Width: 3.8401
Entry
ampl
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4
6
8
10
12
14
16
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0
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20
30
40
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60
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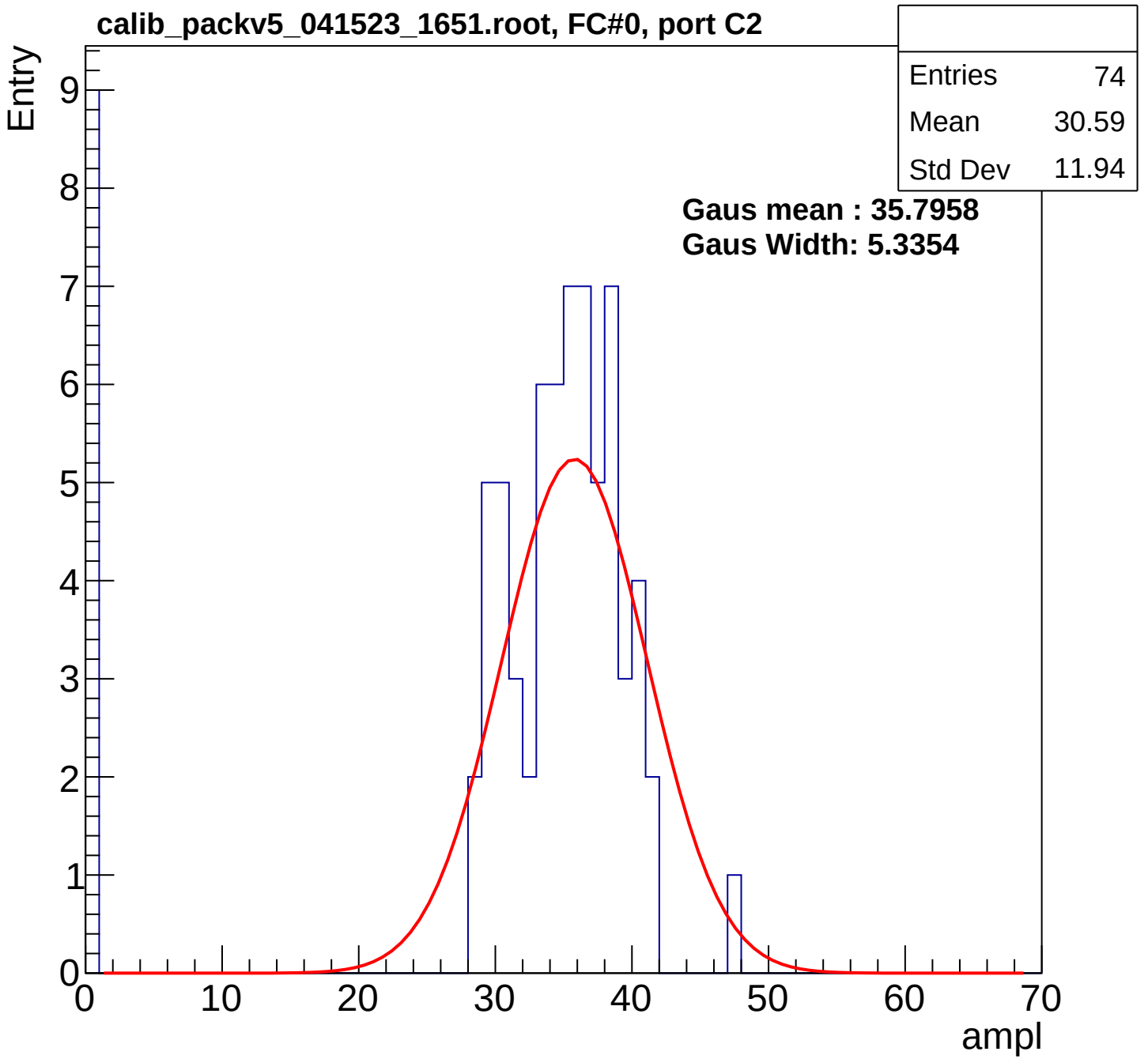
B1L103S, U12-ch64, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 30.59
Std Dev 11.94
Gaus mean : 35.7958
Gaus Width: 5.3354
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
30
40
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60
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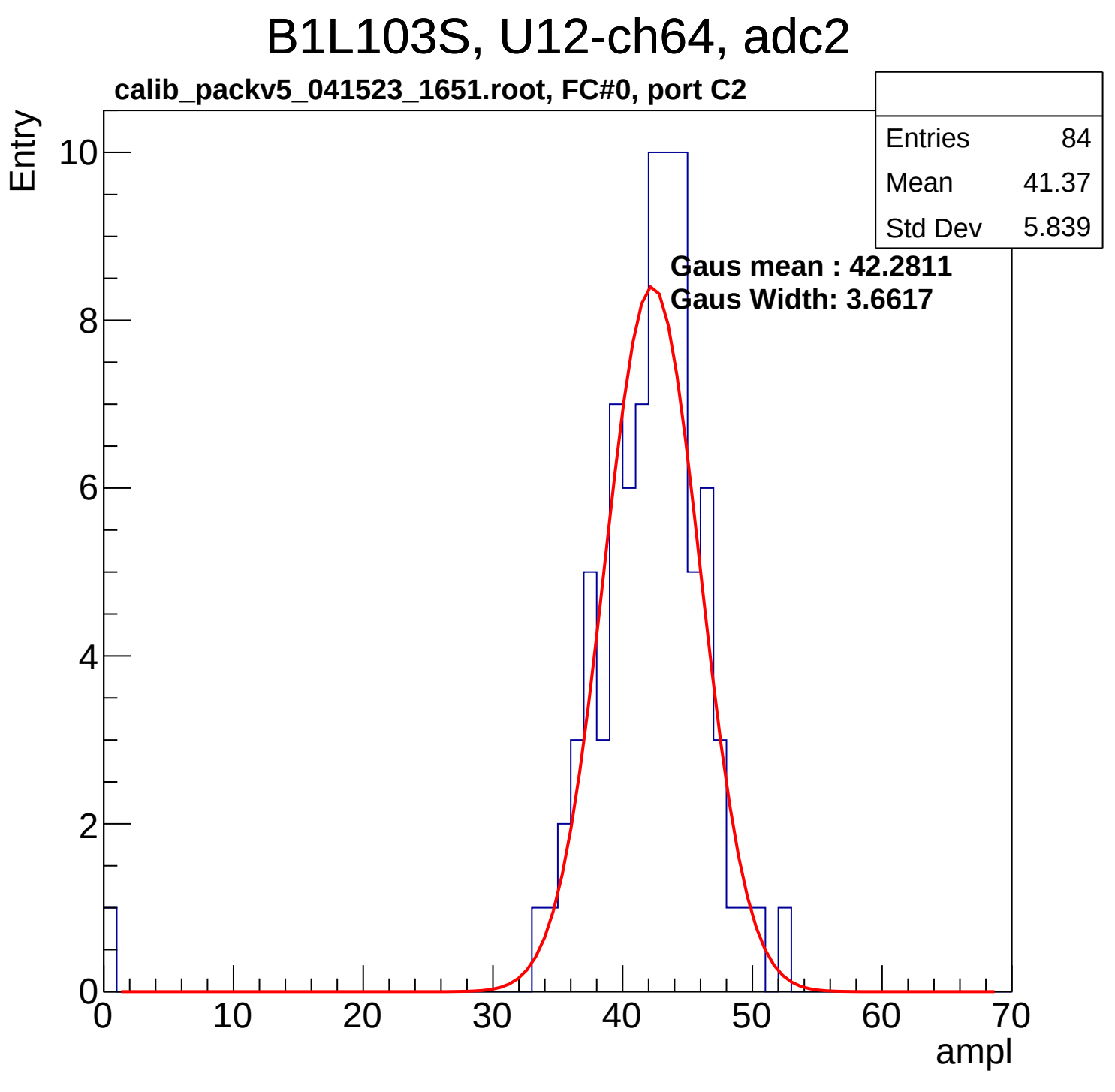
B1L103S, U12-ch64, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 41.37
Std Dev 5.839
Gaus mean : 42.2811
Gaus Width: 3.6617
Entry
ampl
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0
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60
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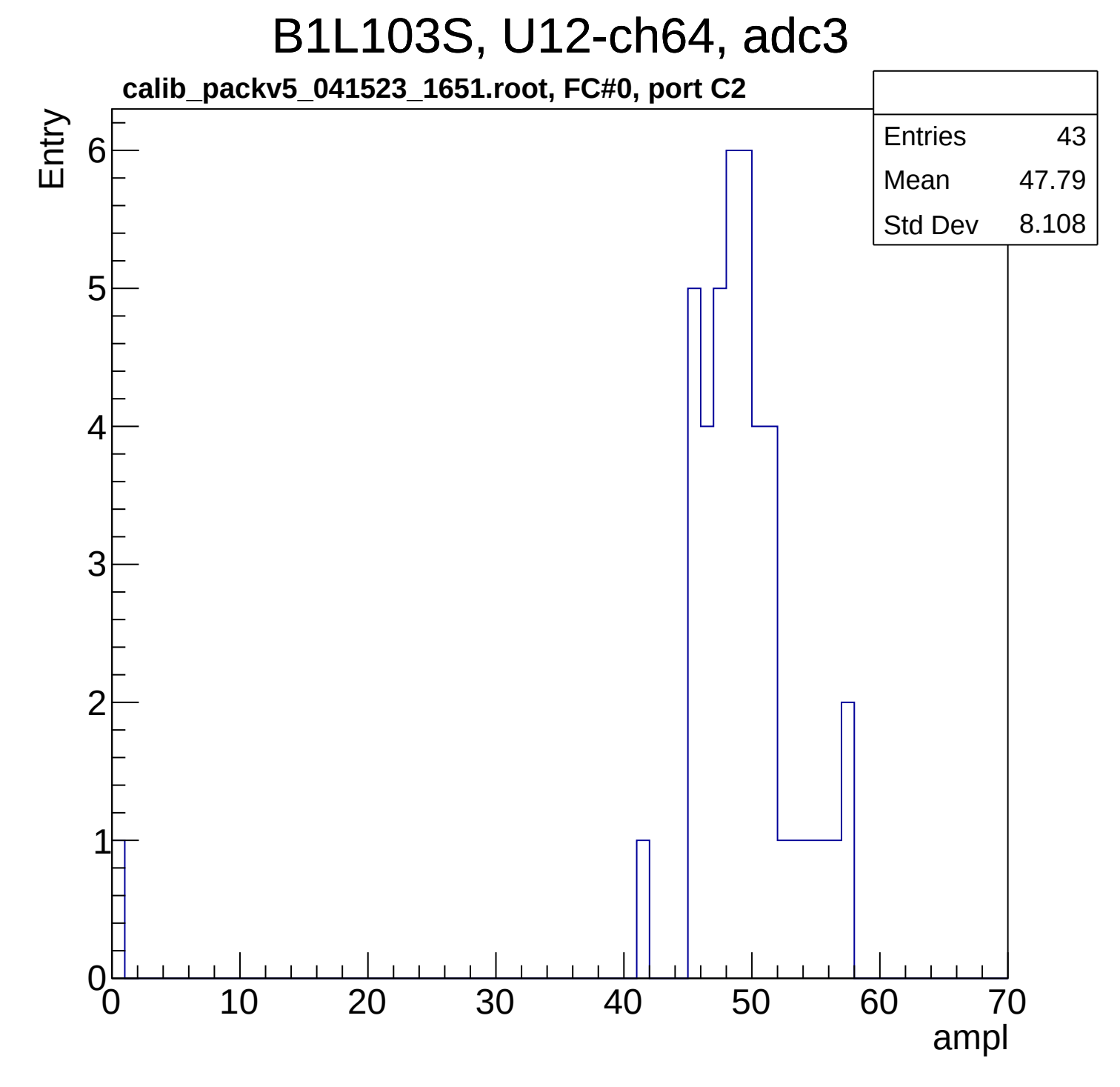
B1L103S, U12-ch64, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 47.79
Std Dev 8.108
Entry
ampl
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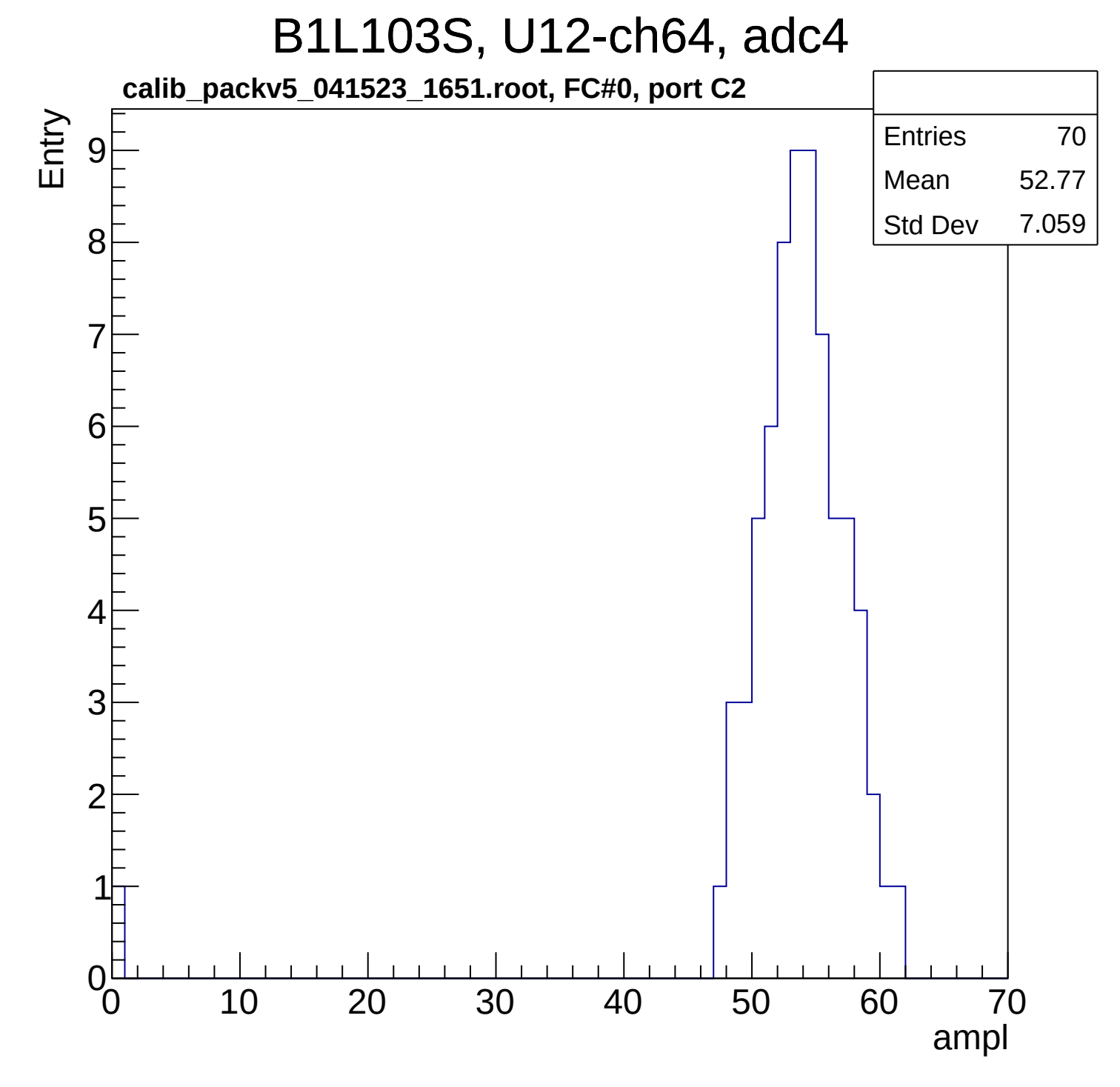
B1L103S, U12-ch64, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 52.77
Std Dev 7.059
Entry
ampl
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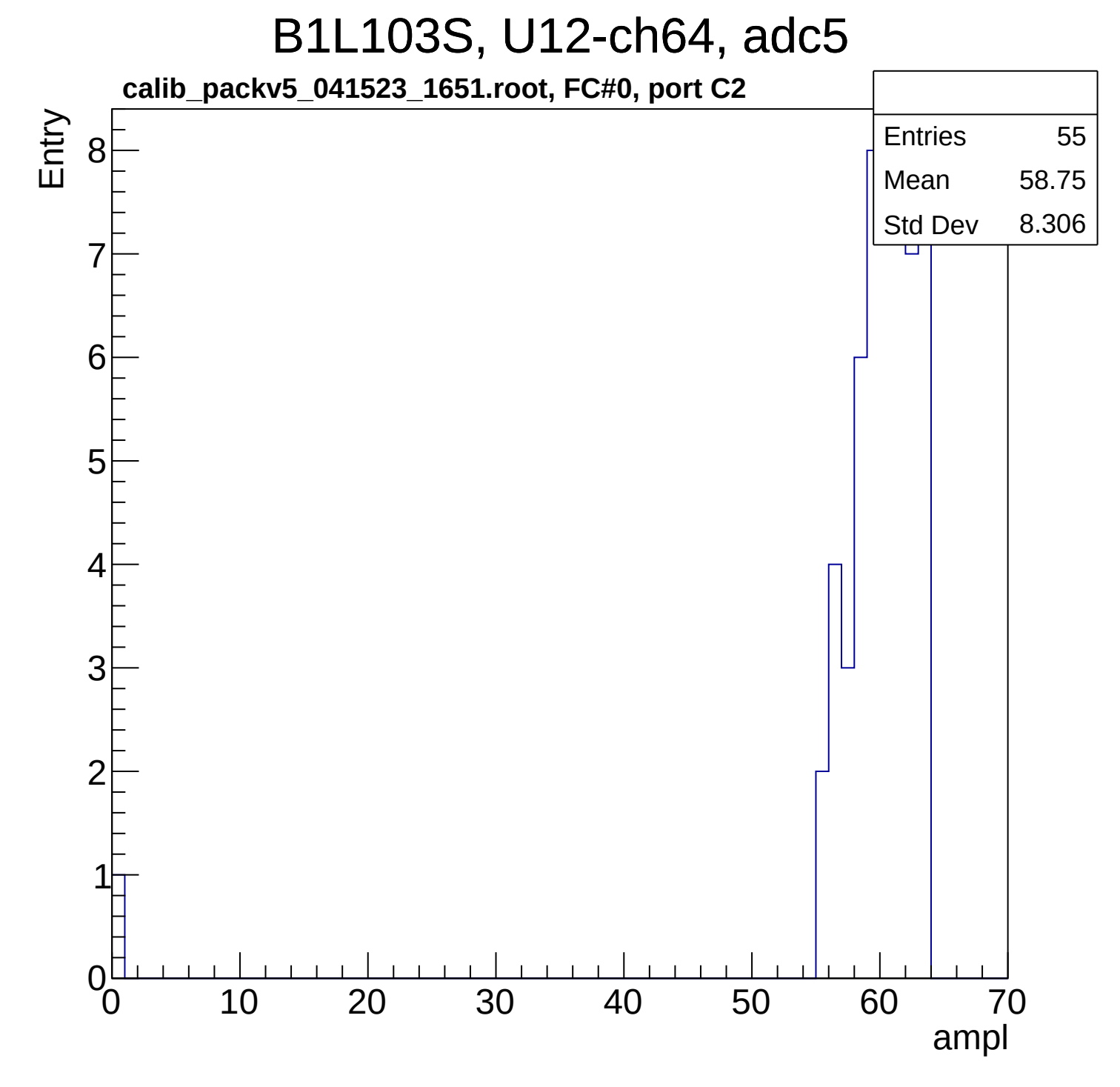
B1L103S, U12-ch64, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.75
Std Dev 8.306
Entry
ampl
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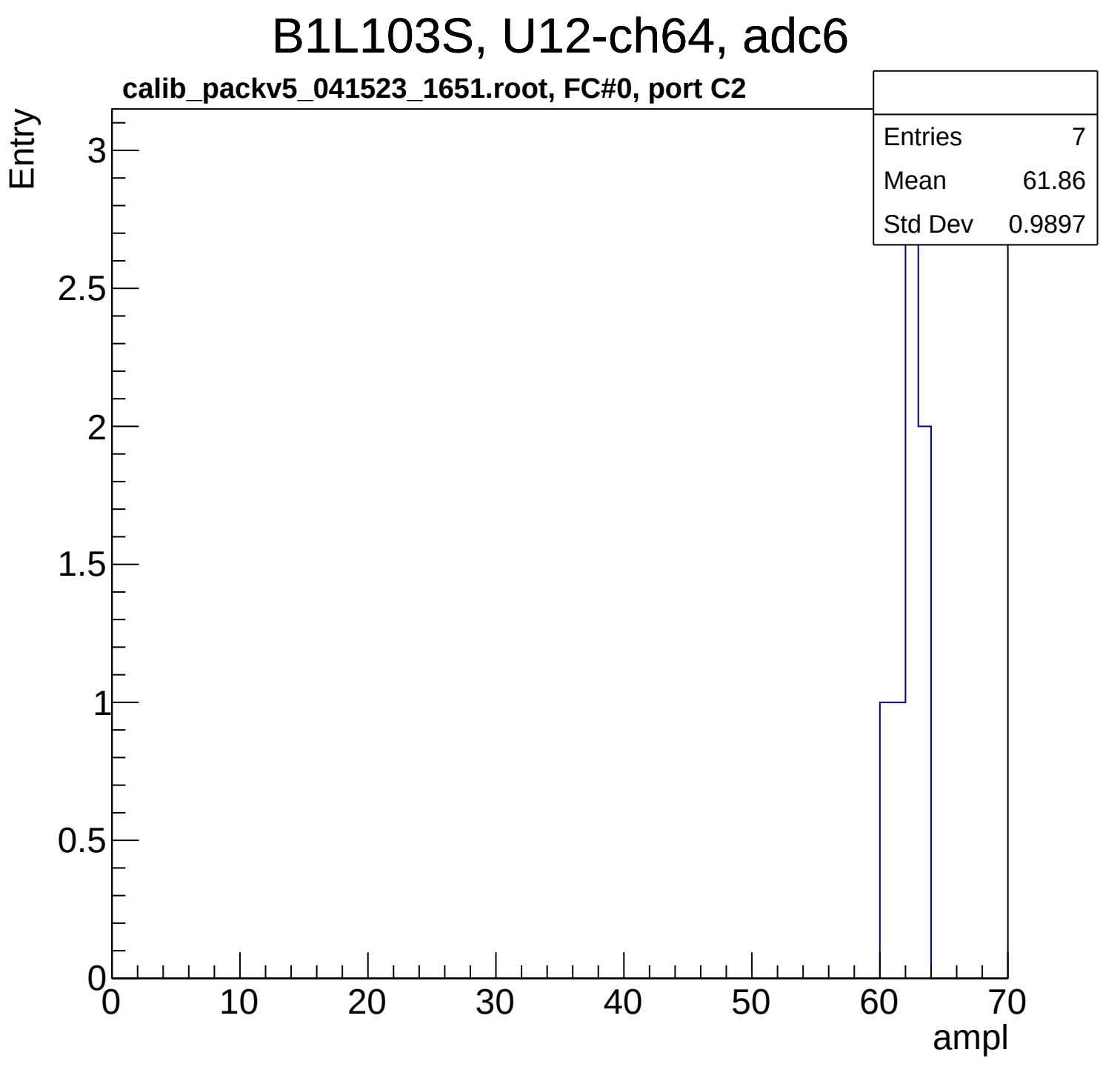
B1L103S, U12-ch64, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.86
Std Dev 0.9897
Entry
ampl
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1
1.5
2
2.5
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0
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20
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40
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60
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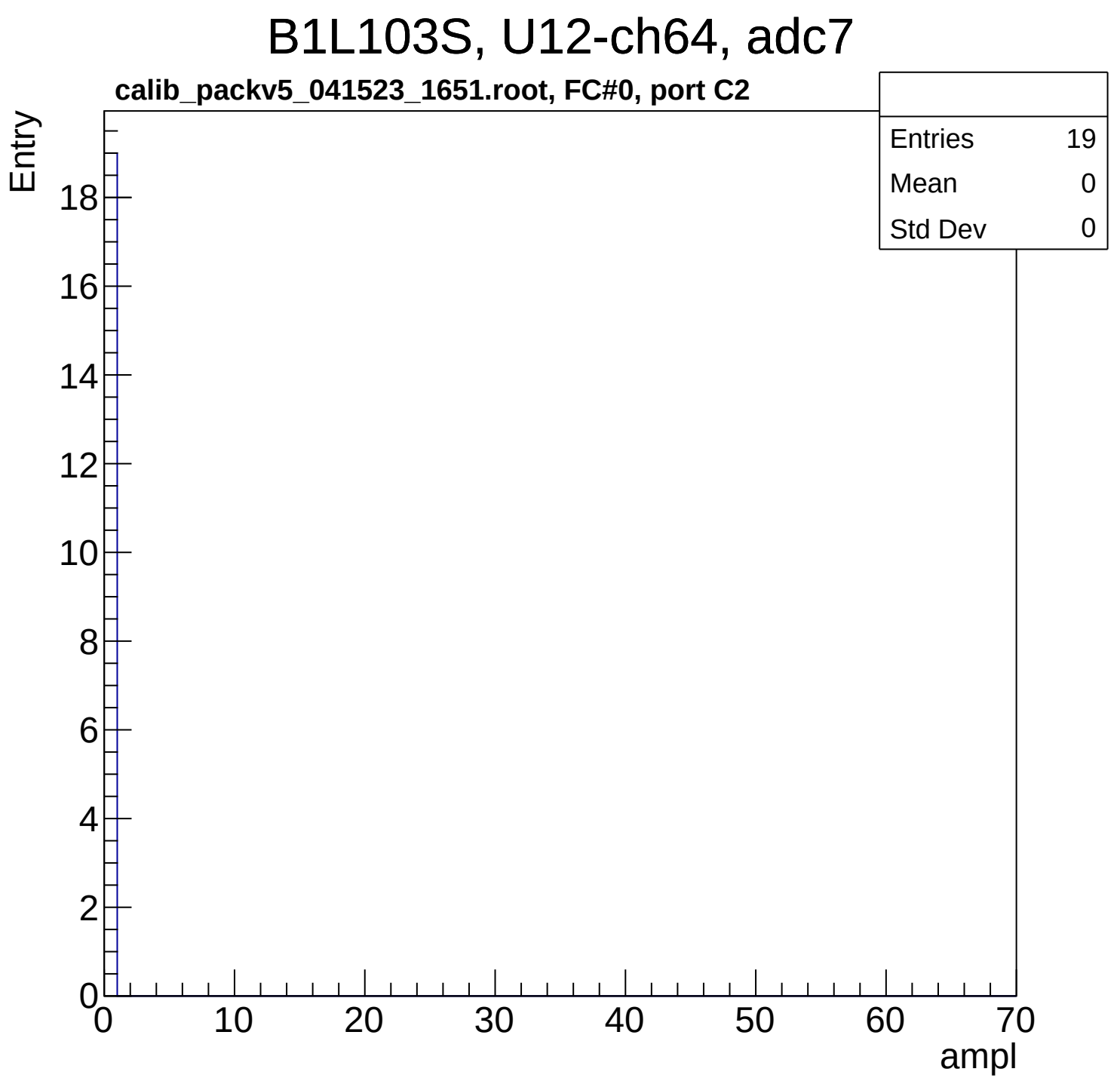
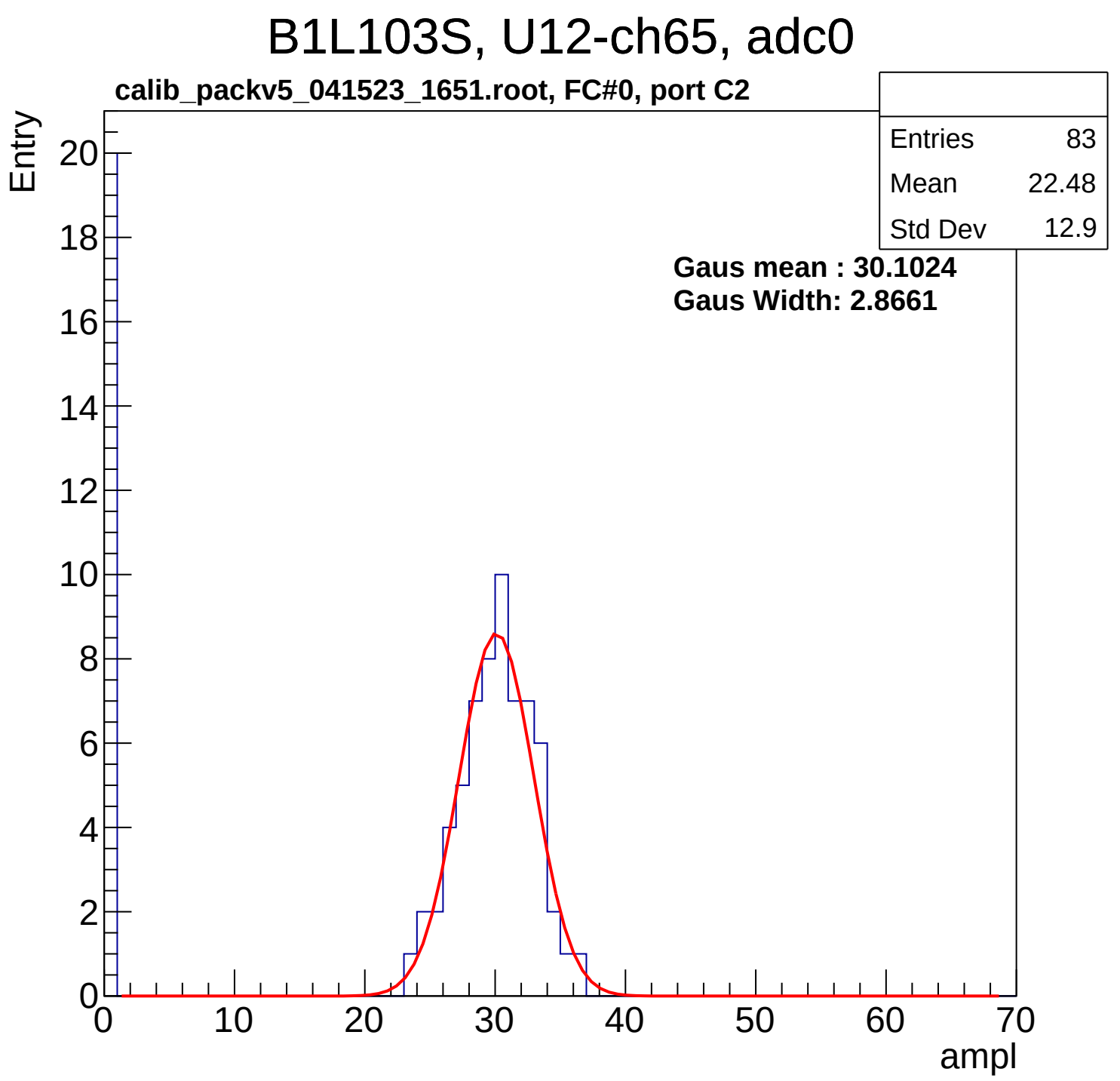

B1L103S, U12-ch64, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch65, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 22.48
Std Dev 12.9
Gaus mean : 30.1024
Gaus Width: 2.8661
Entry
ampl
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6
8
10
12
14
16
18
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0
10
20
30
40
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60
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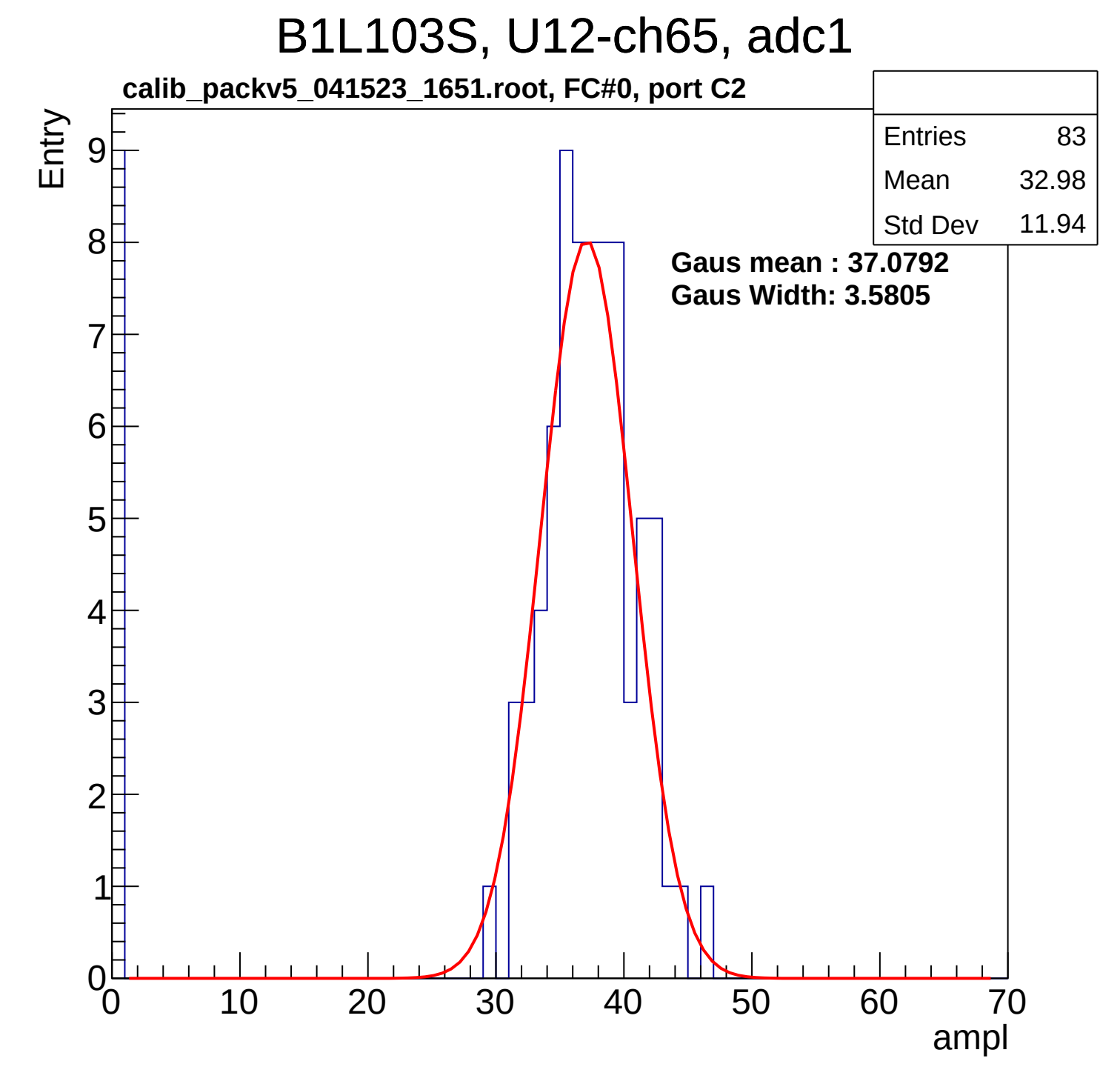
B1L103S, U12-ch65, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 32.98
Std Dev 11.94
Gaus mean : 37.0792
Gaus Width: 3.5805
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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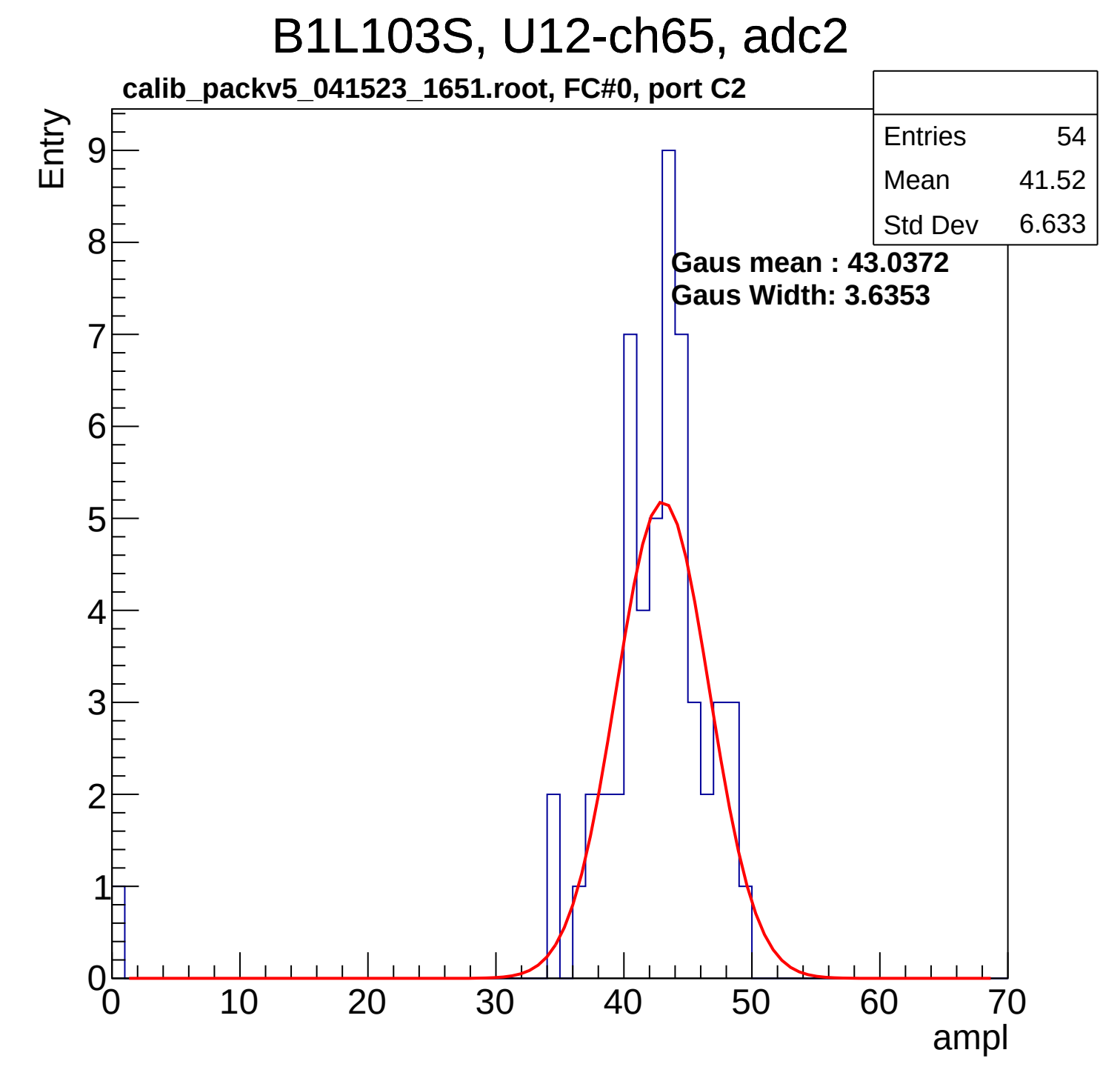
B1L103S, U12-ch65, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 41.52
Std Dev 6.633
Gaus mean : 43.0372
Gaus Width: 3.6353
Entry
ampl
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2
3
4
5
6
7
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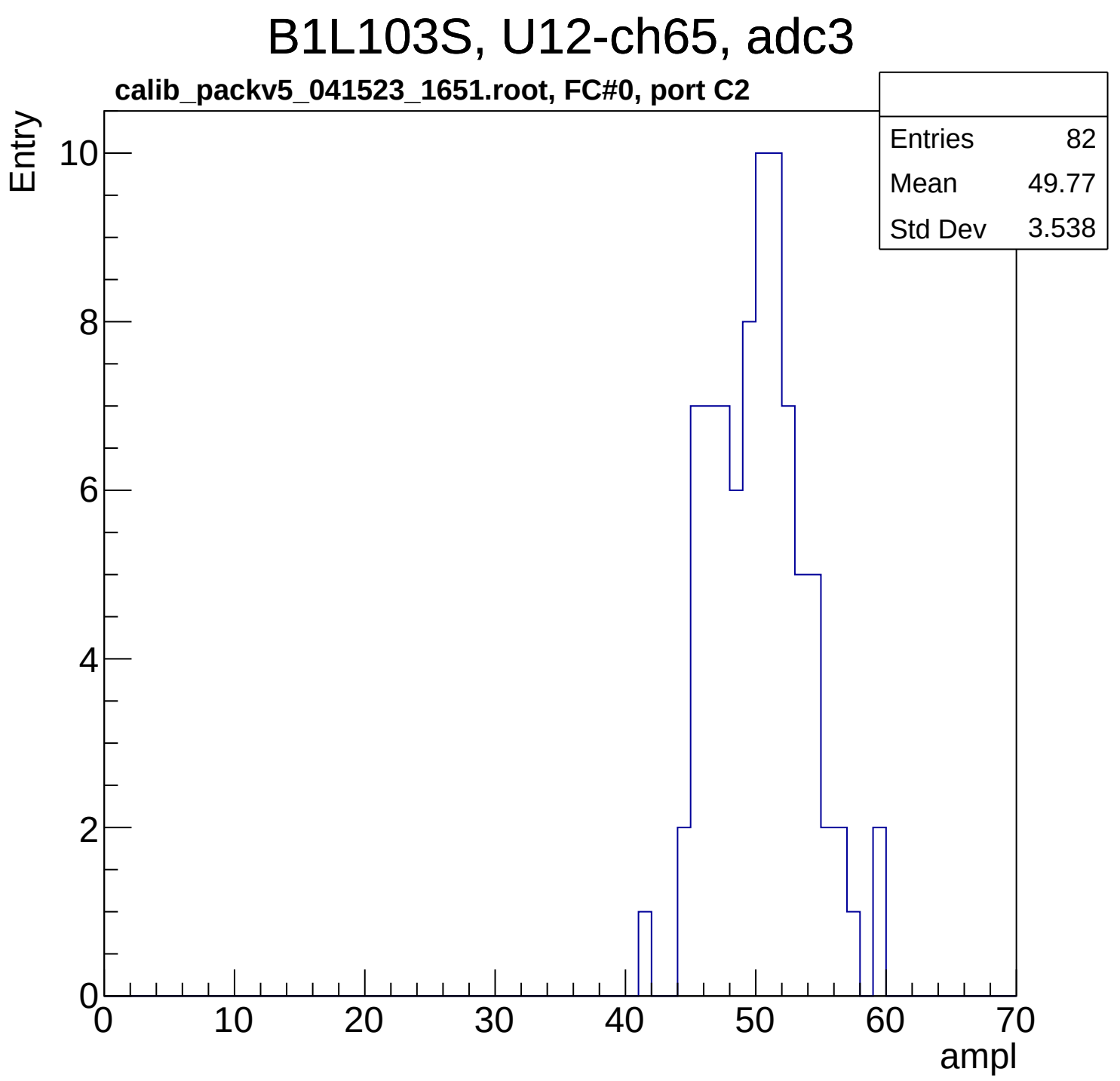
B1L103S, U12-ch65, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 49.77
Std Dev 3.538
Entry
ampl
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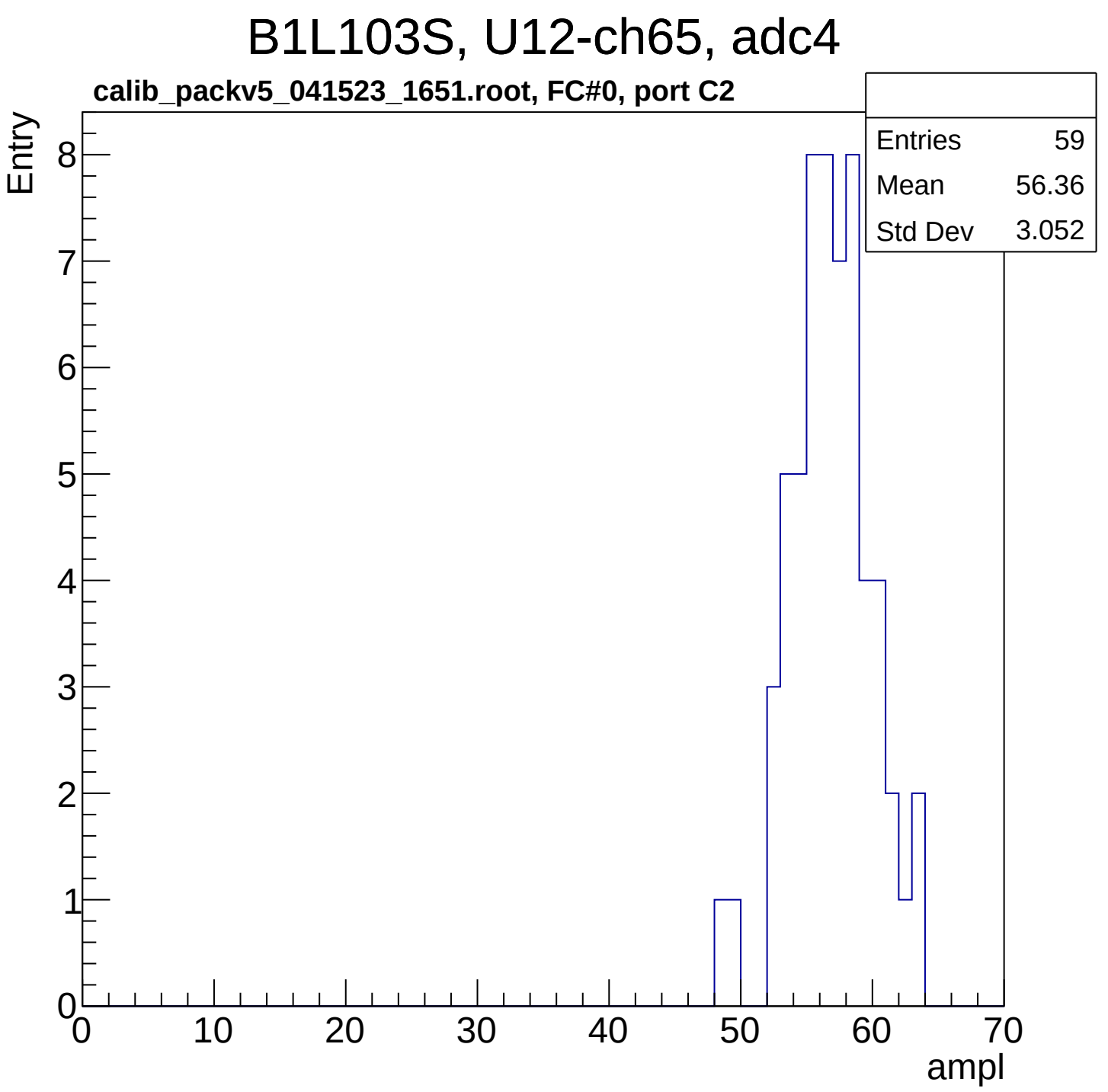
B1L103S, U12-ch65, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 56.36
Std Dev 3.052
Entry
ampl
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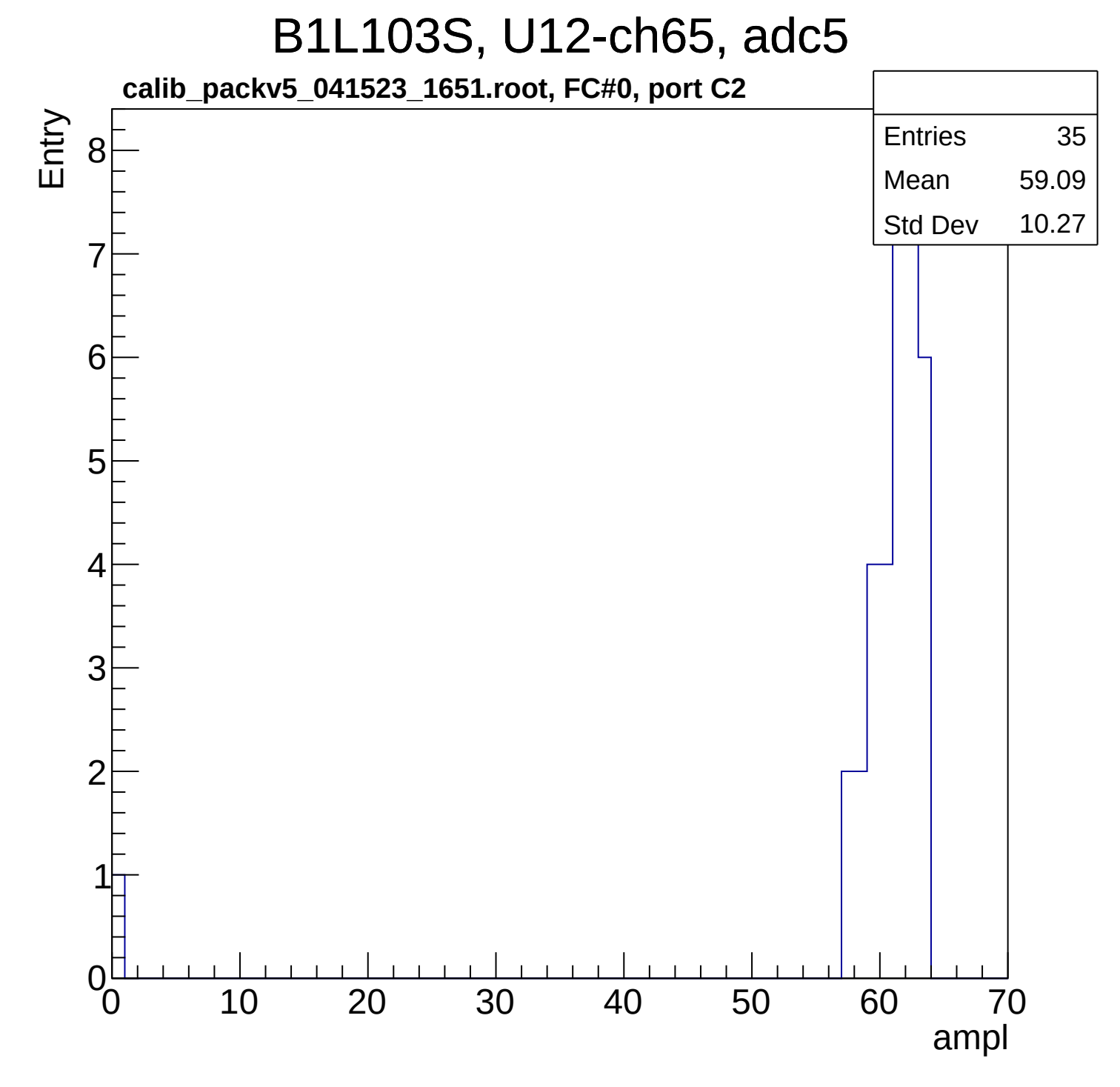
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U12-ch65, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 35
Mean 59.09
Std Dev 10.27
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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60
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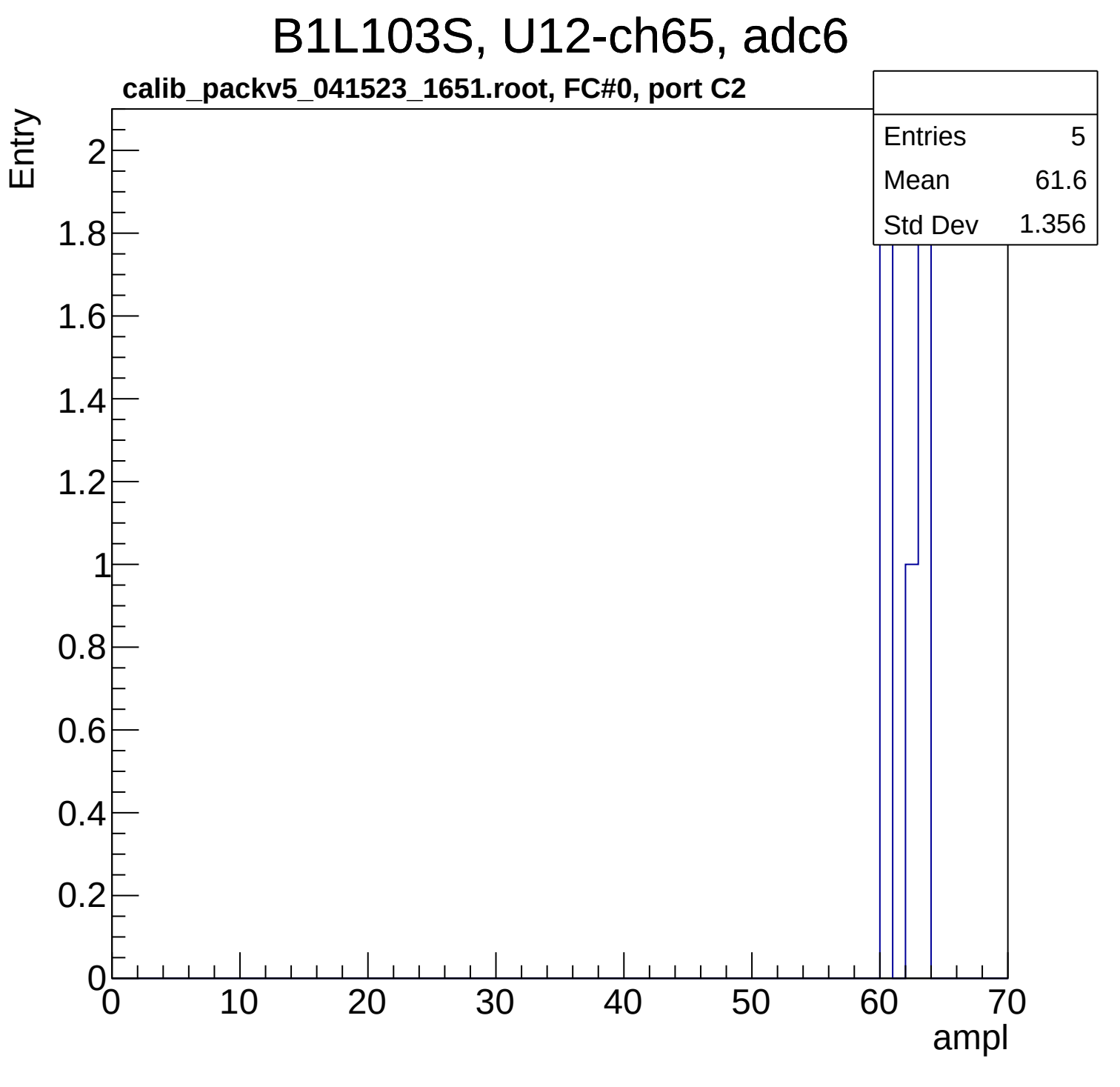
B1L103S, U12-ch65, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.6
Std Dev 1.356
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
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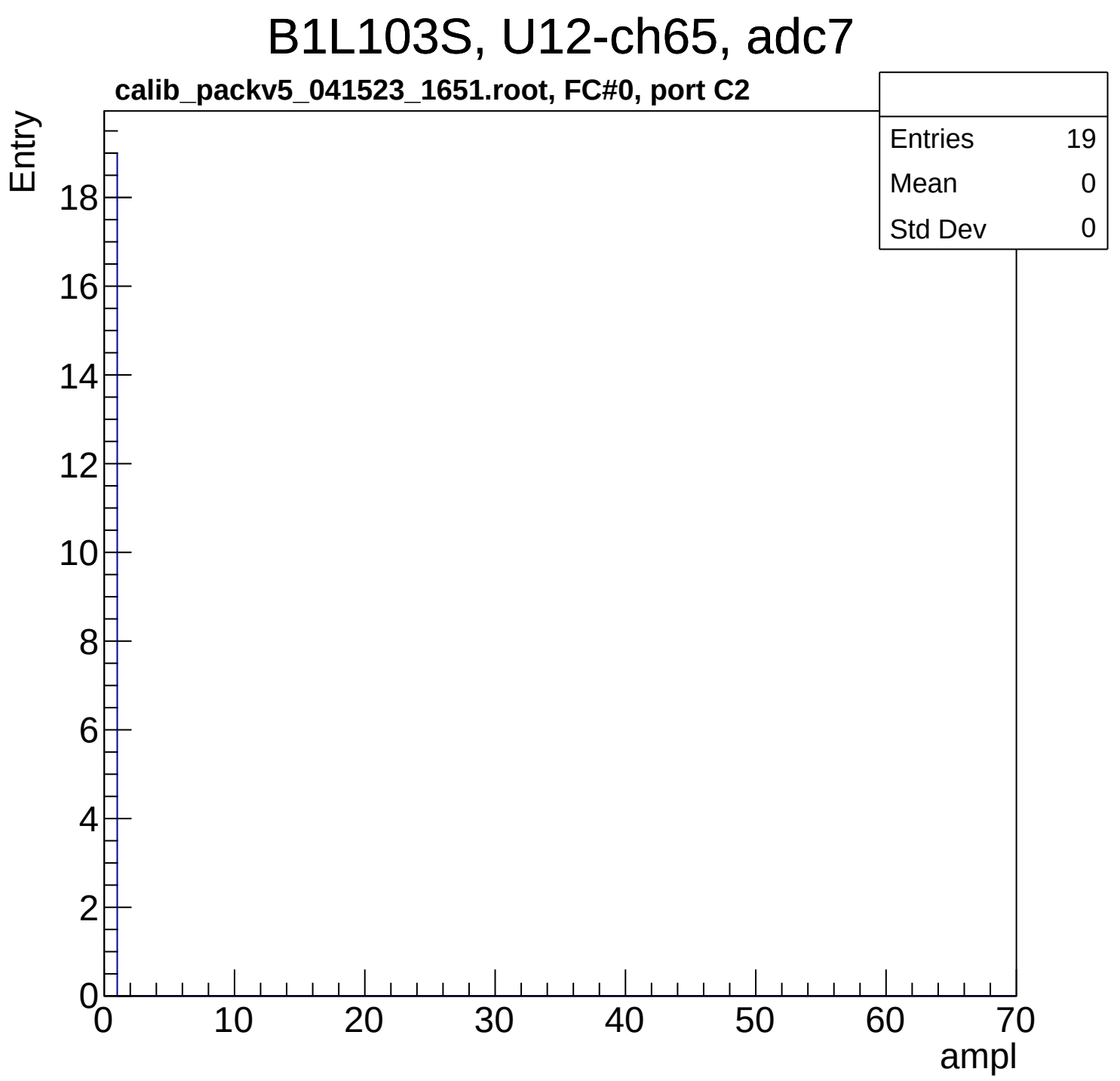
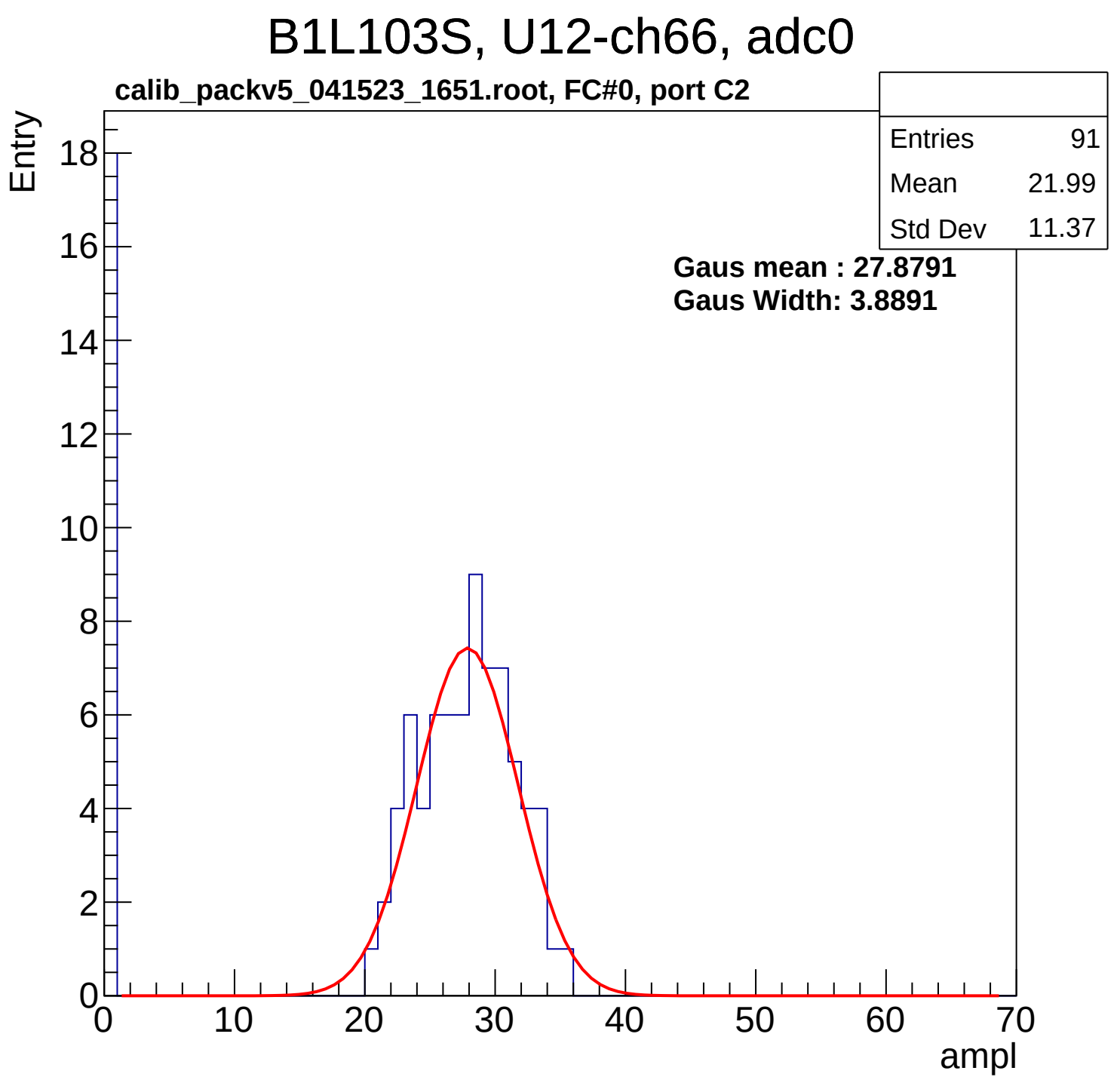

B1L103S, U12-ch65, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch66, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 21.99
Std Dev 11.37
Gaus mean : 27.8791
Gaus Width: 3.8891
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
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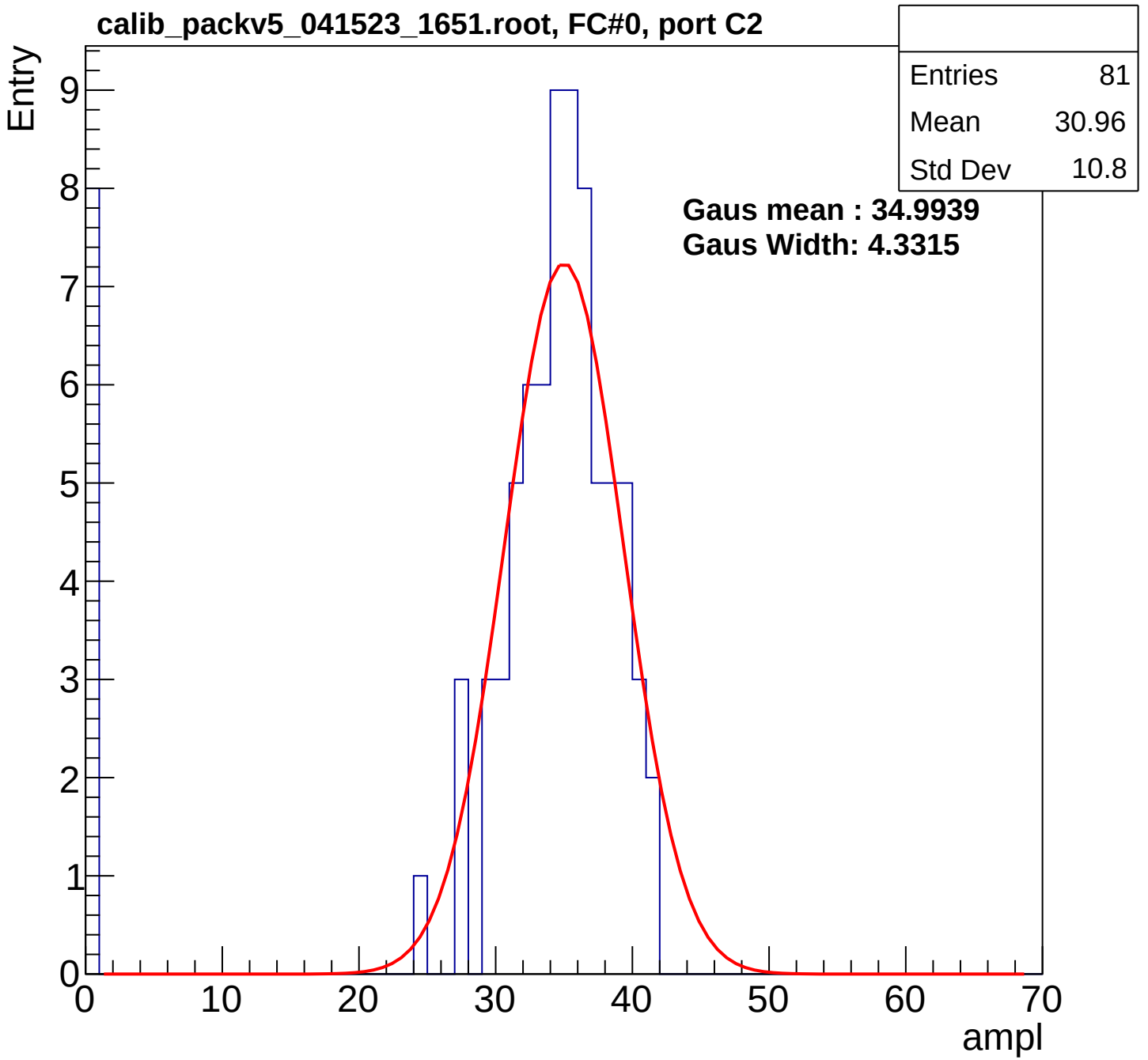
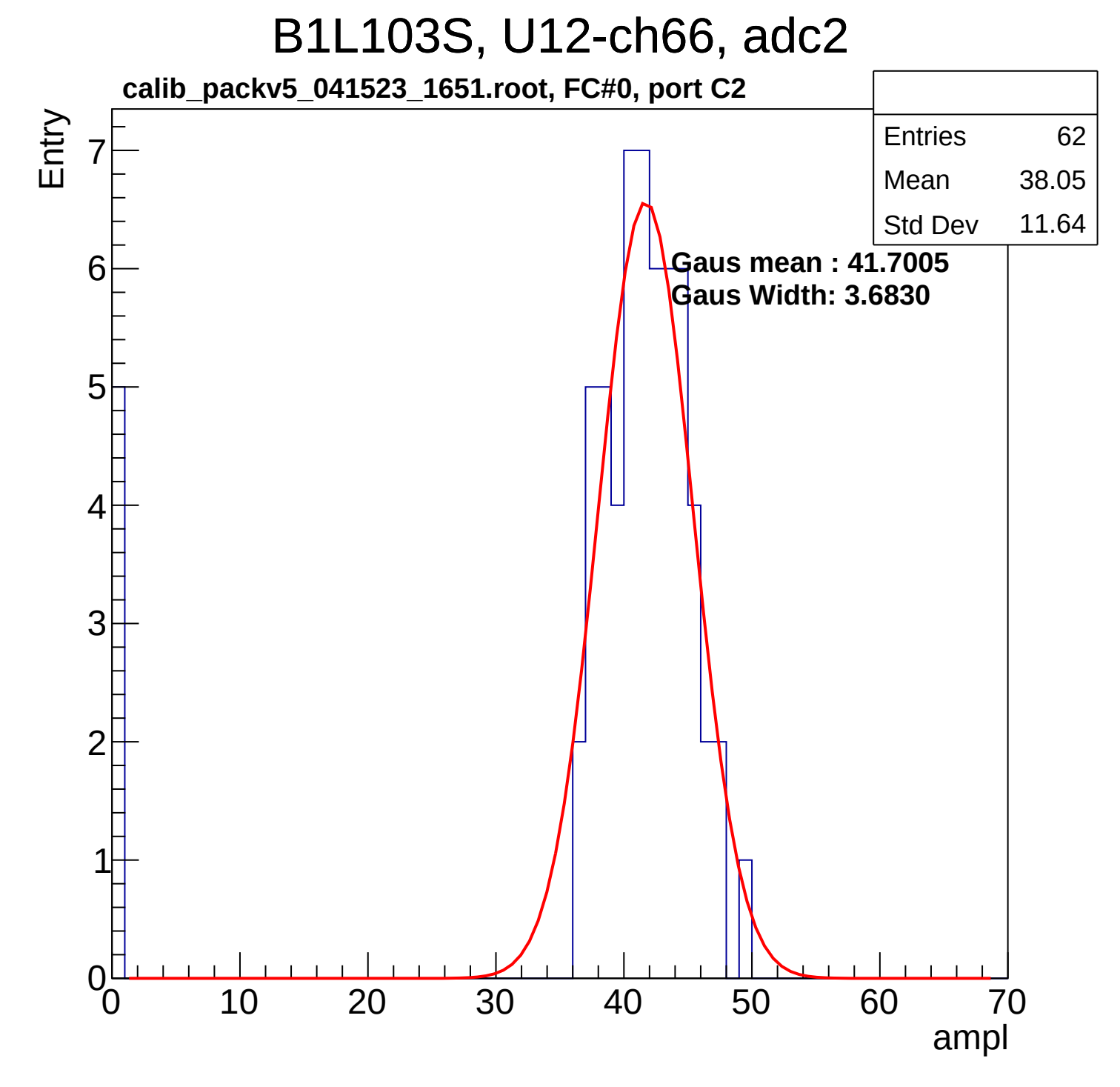
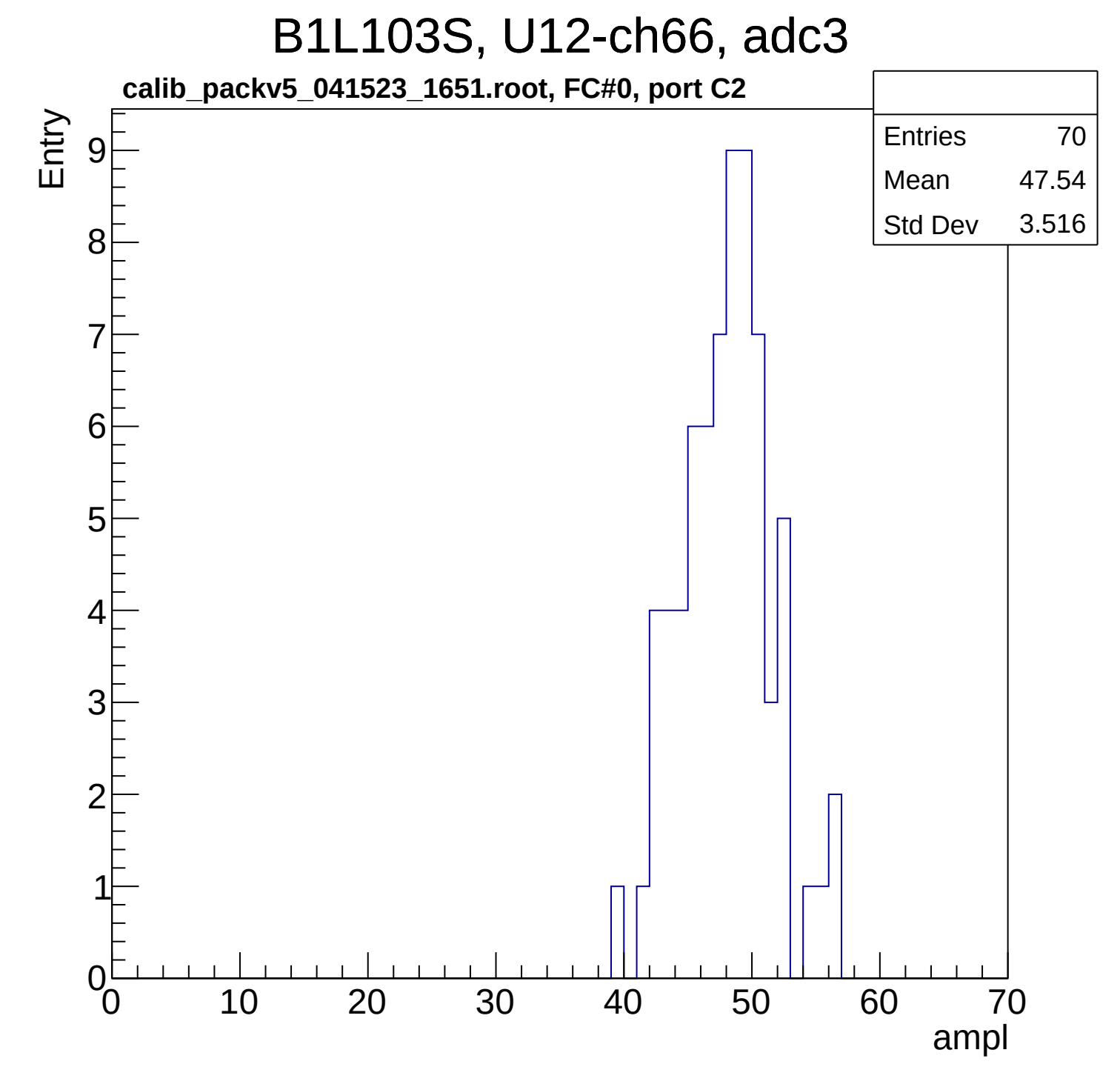
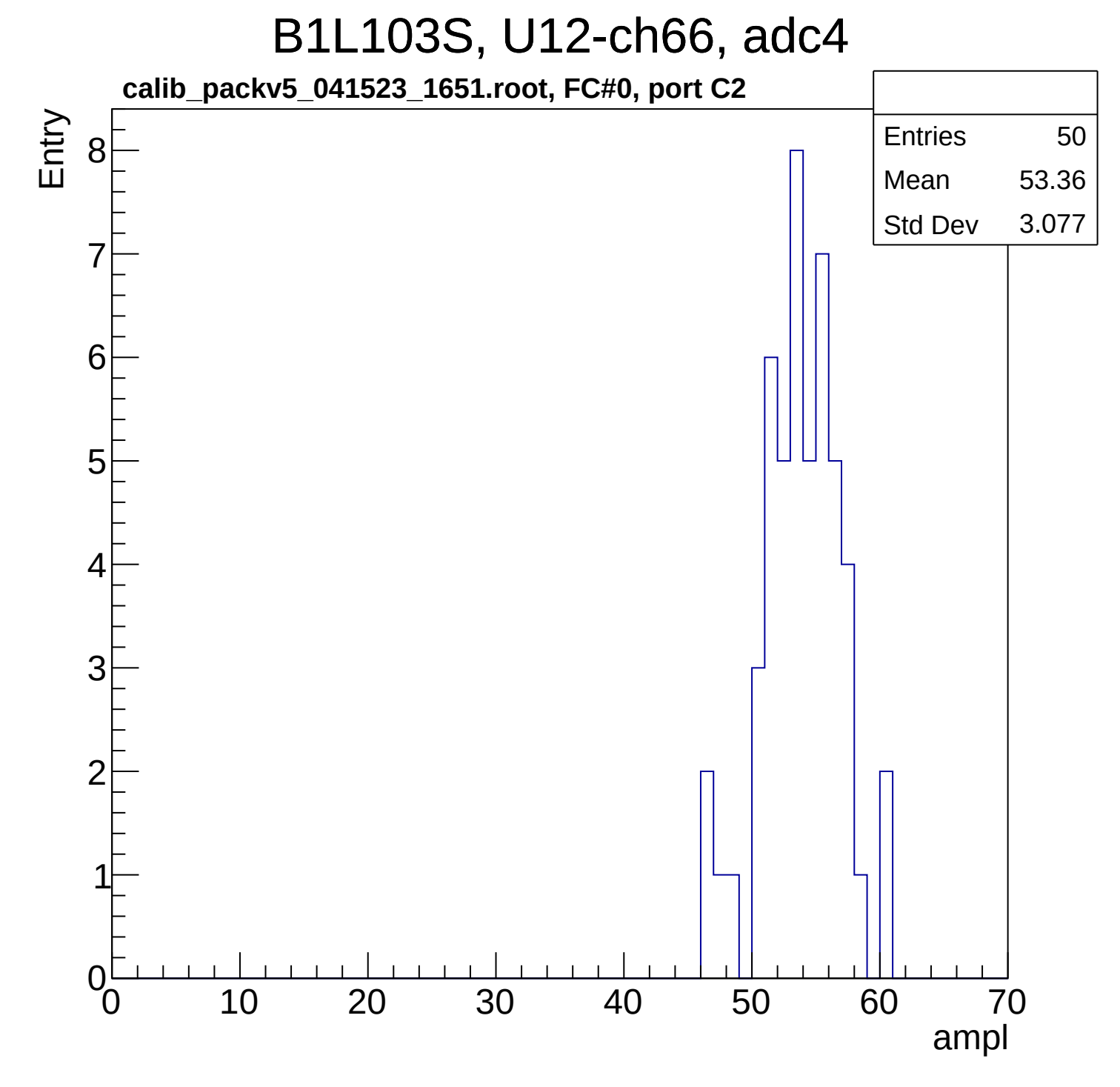

B1L103S, U12-ch66, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 30.96
Std Dev 10.8
Gaus mean : 34.9939
Gaus Width: 4.3315
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch66, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 38.05
Std Dev 11.64
Gaus mean : 41.7005
Gaus Width: 3.6830
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U12-ch66, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 47.54
Std Dev 3.516
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch66, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 53.36
Std Dev 3.077
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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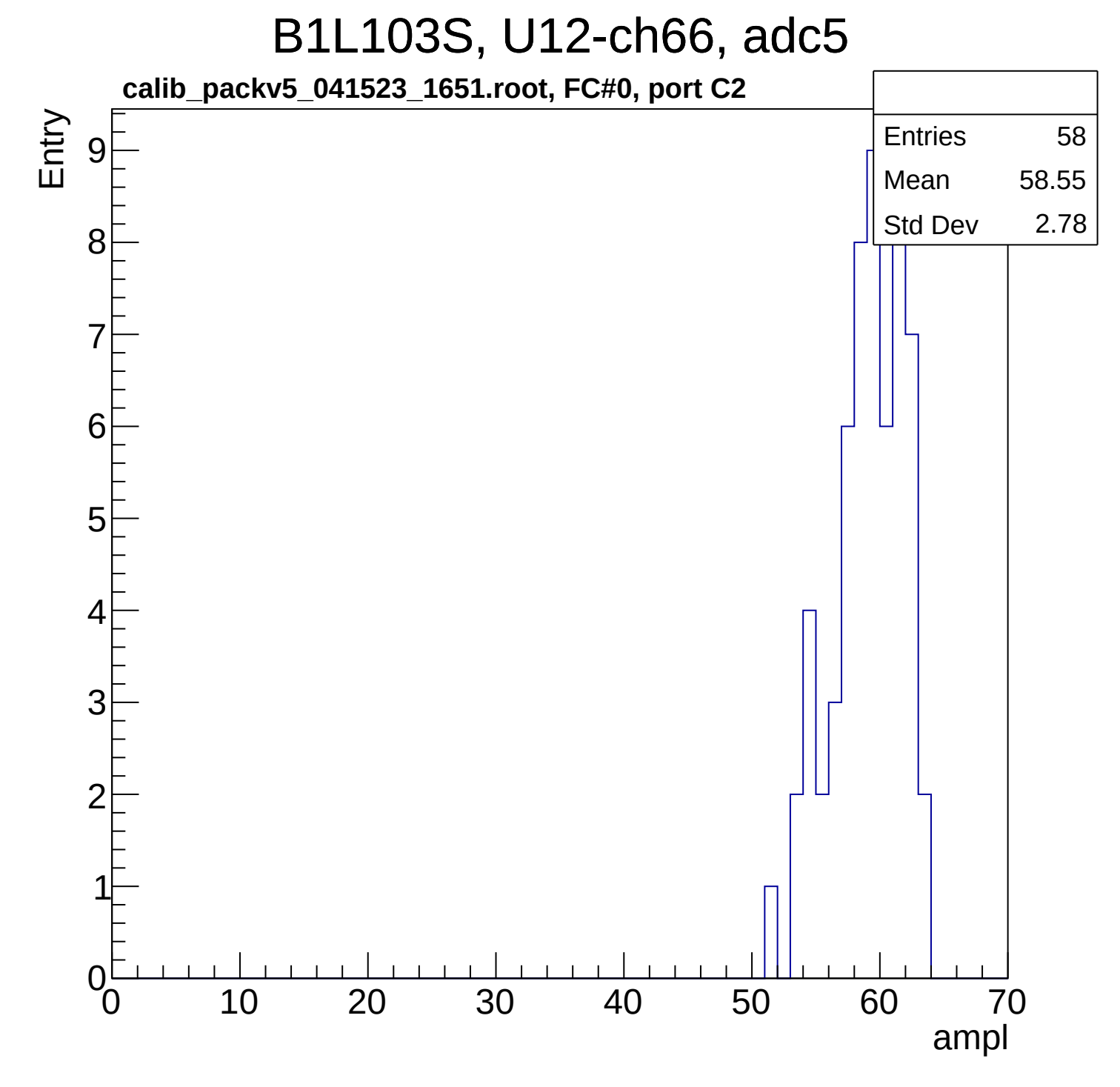
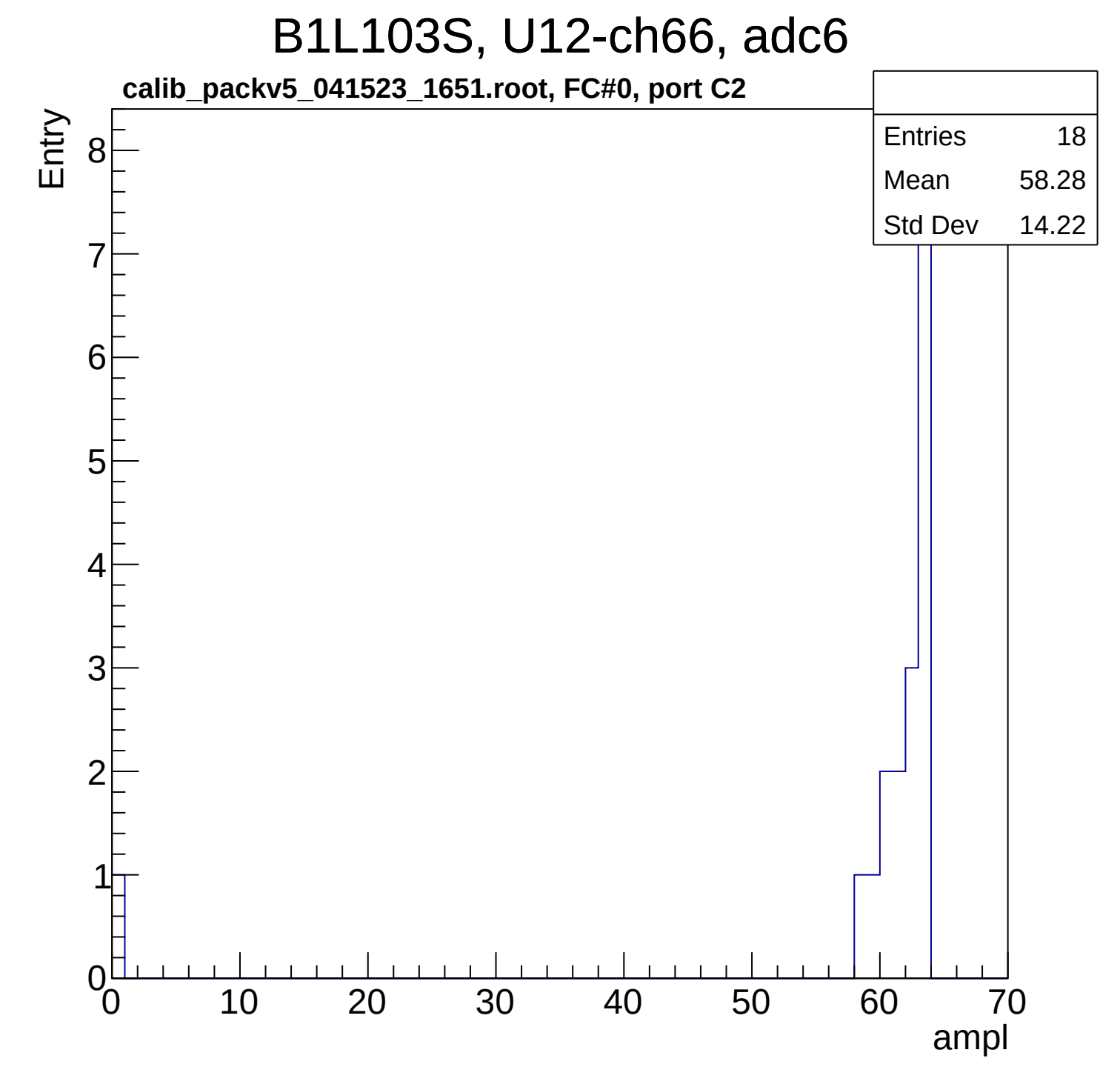

B1L103S, U12-ch66, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 58.55
Std Dev 2.78
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch66, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 58.28
Std Dev 14.22
Entry
ampl
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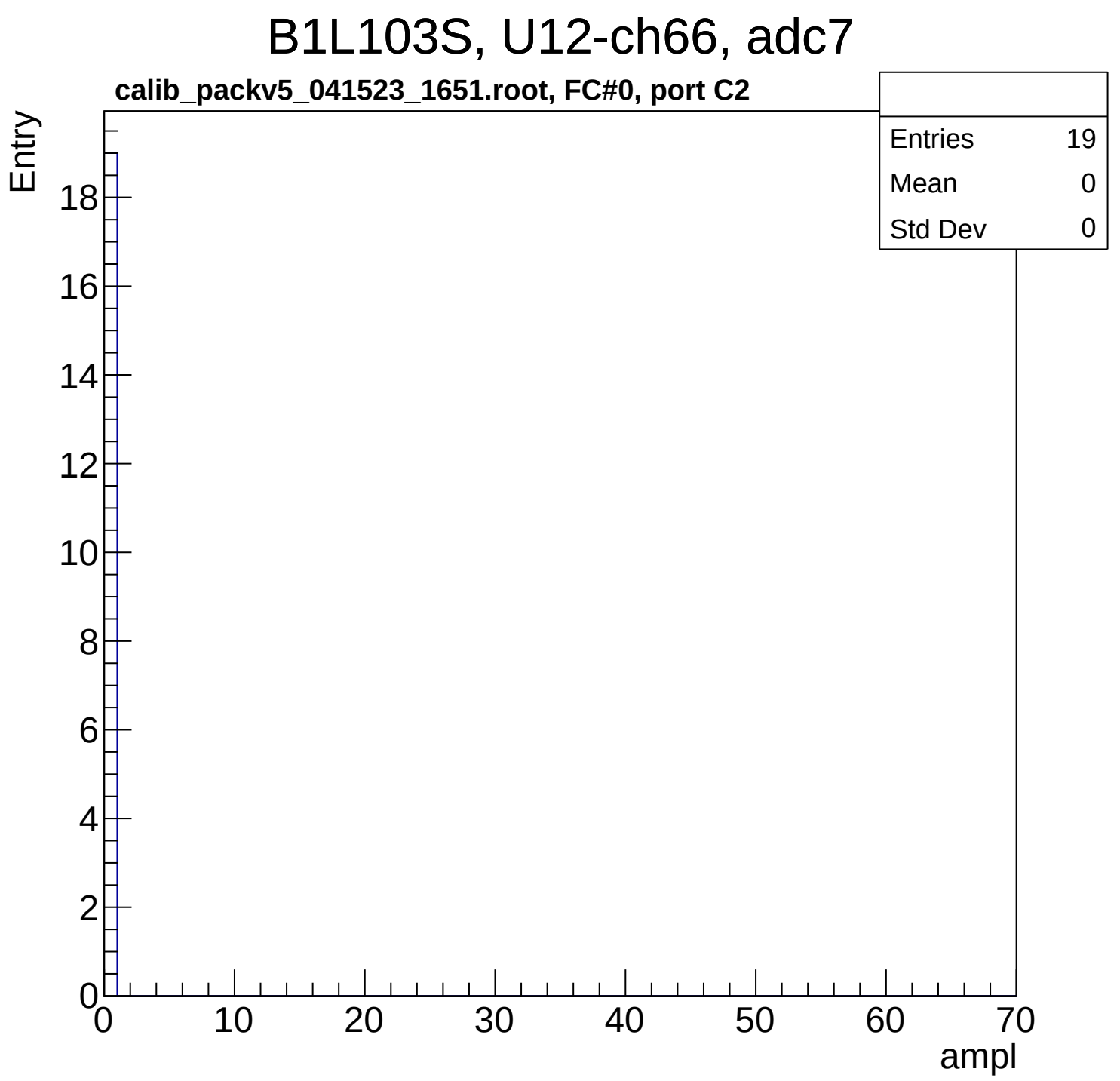
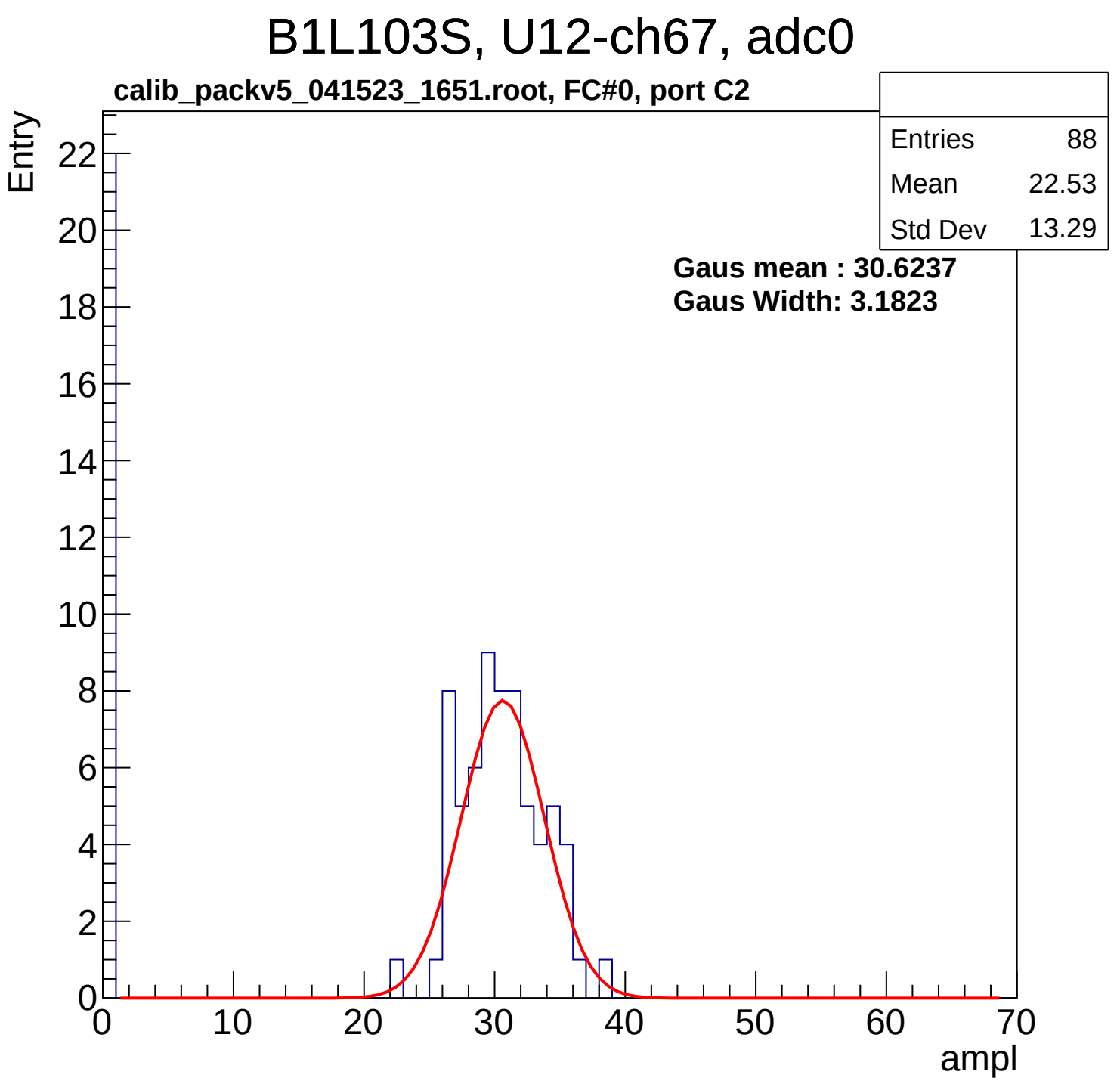
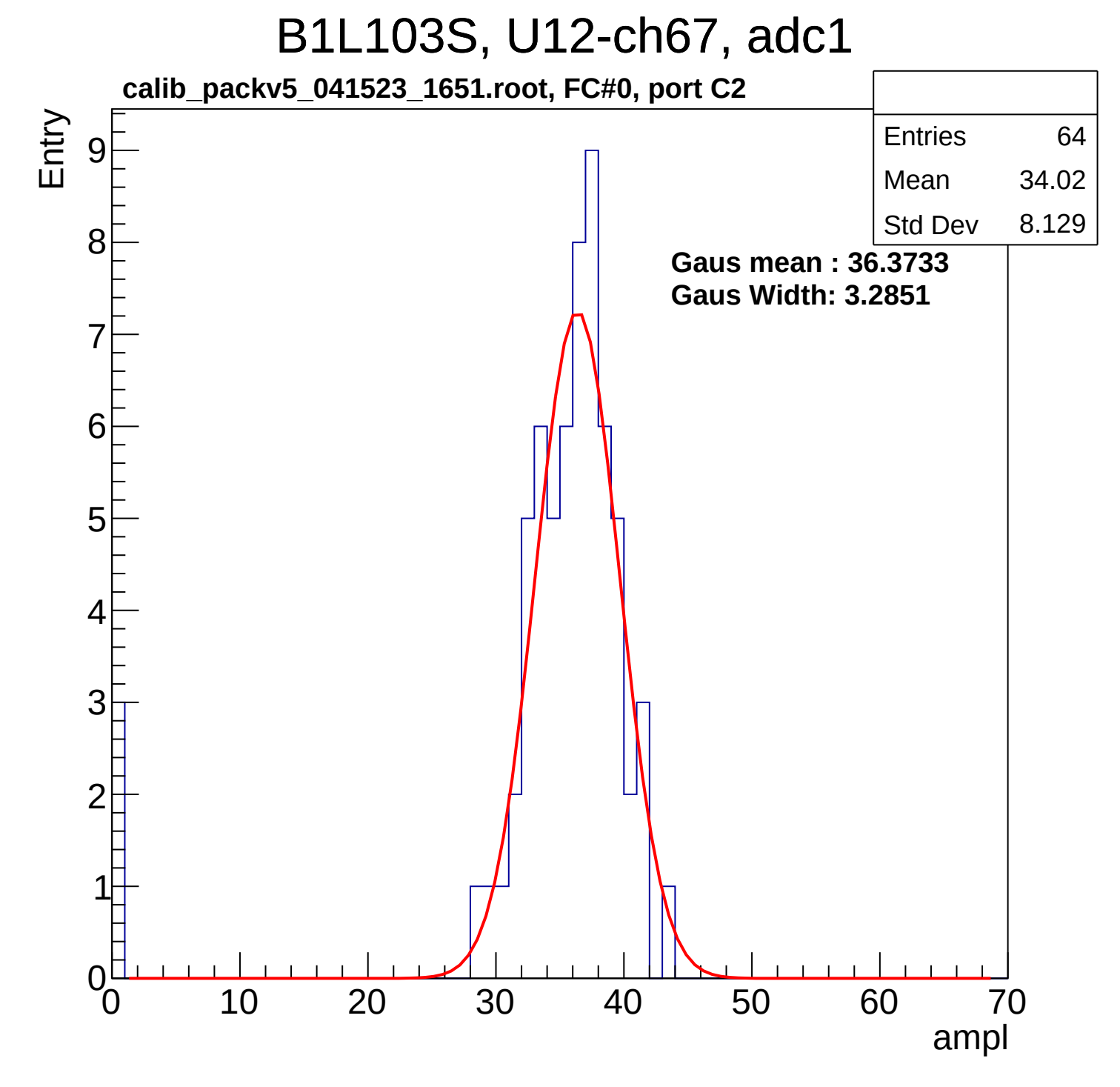
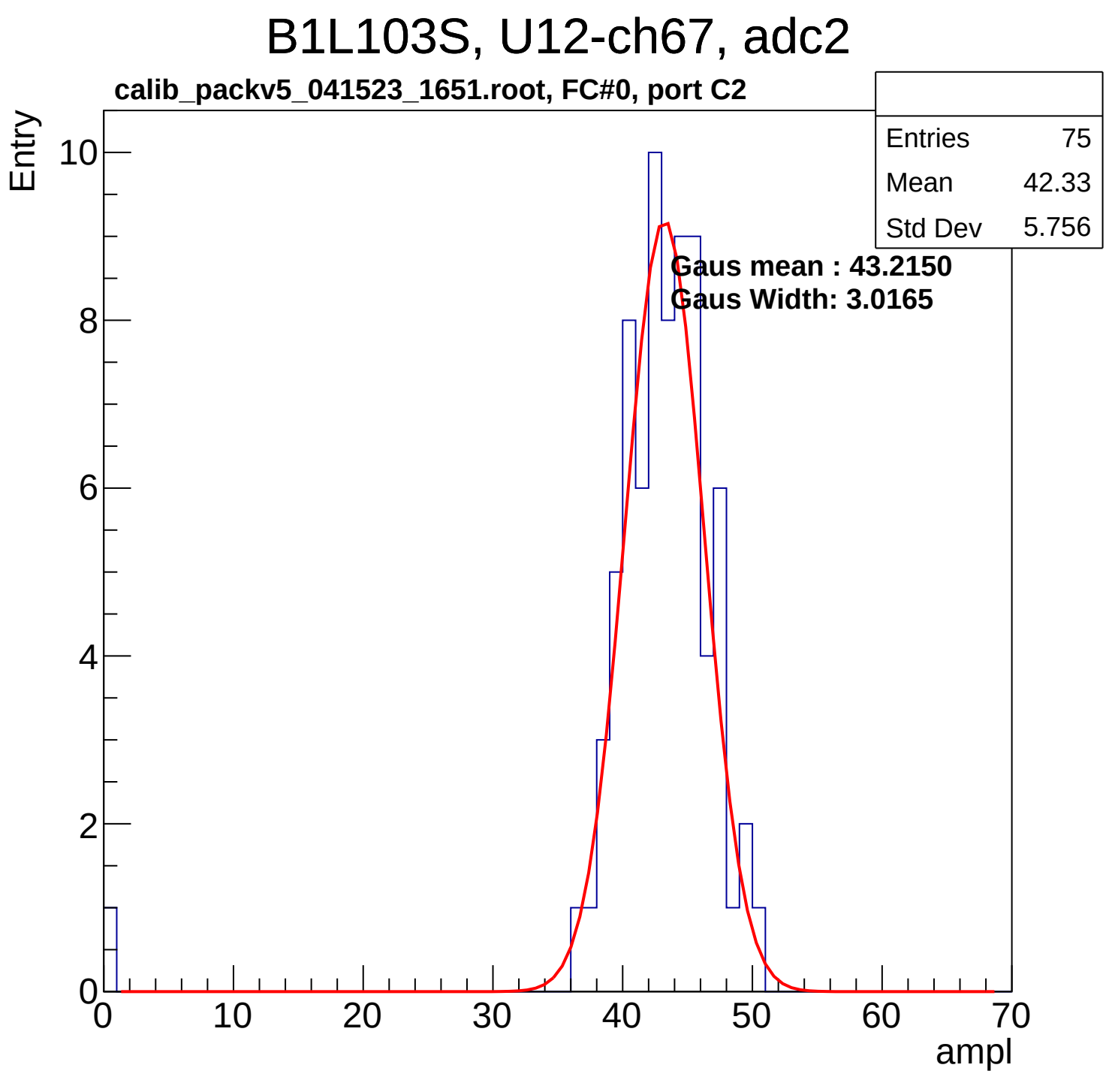
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U12-ch66, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch67, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 22.53
Std Dev 13.29
Gaus mean : 30.6237
Gaus Width: 3.1823
Entry
ampl
0
2
4
6
8
10
12
14
16
18
20
22
0
10
20
30
40
50
60
70


B1L103S, U12-ch67, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 34.02
Std Dev 8.129
Gaus mean : 36.3733
Gaus Width: 3.2851
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch67, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 42.33
Std Dev 5.756
Gaus mean : 43.2150
Gaus Width: 3.0165
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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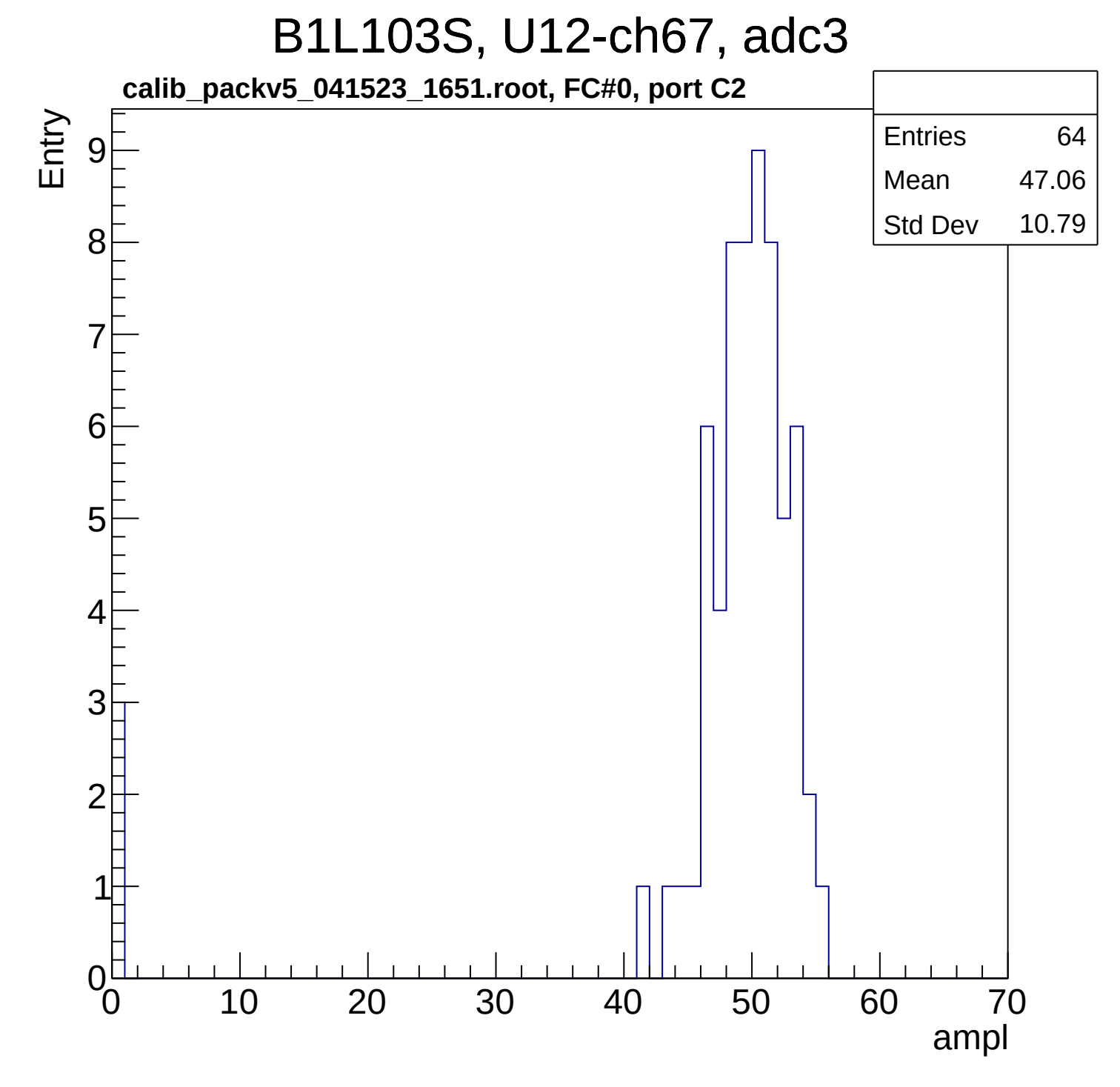
B1L103S, U12-ch67, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 47.06
Std Dev 10.79
Entry
ampl
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2
3
4
5
6
7
8
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0
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60
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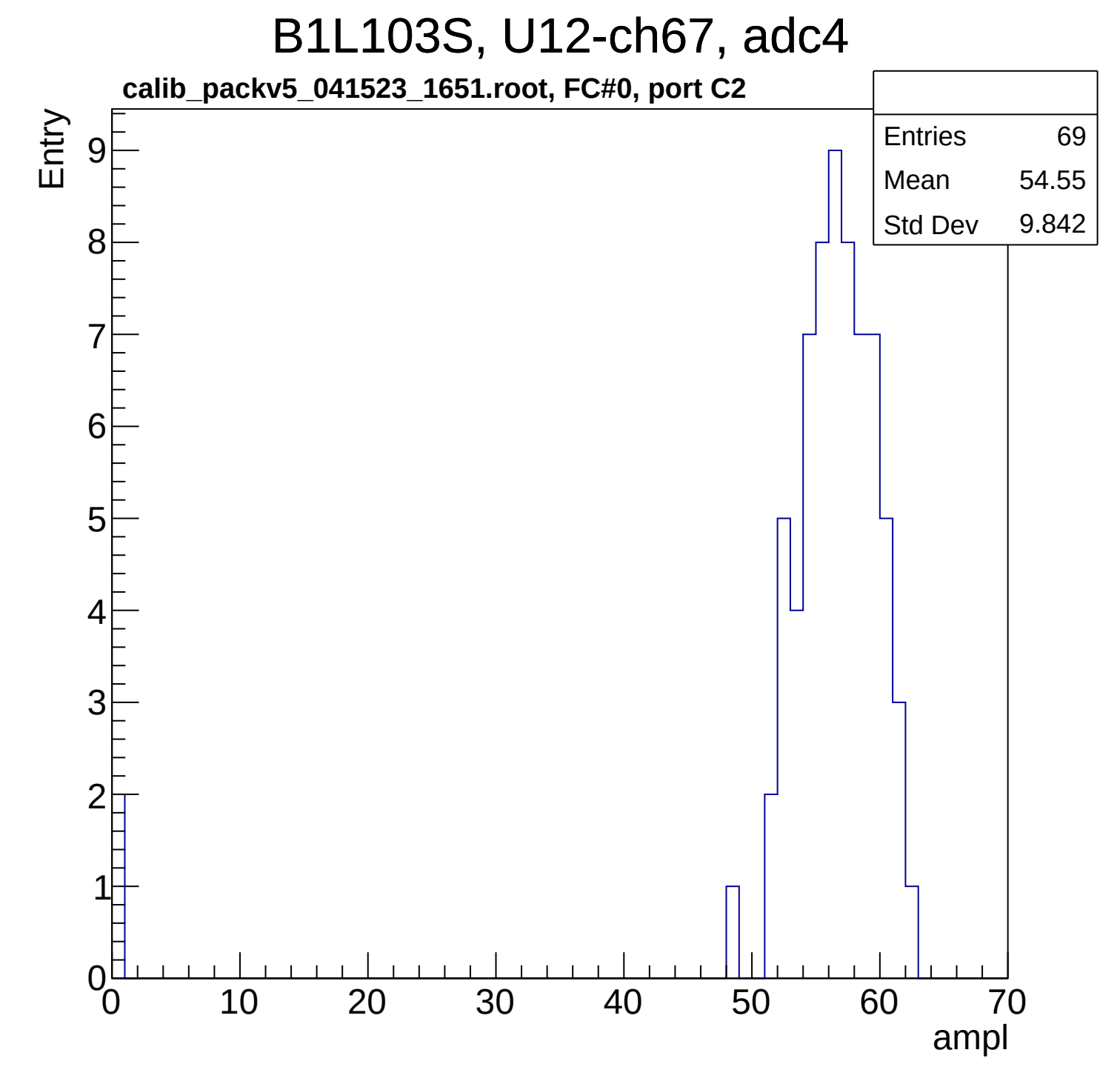
B1L103S, U12-ch67, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 54.55
Std Dev 9.842
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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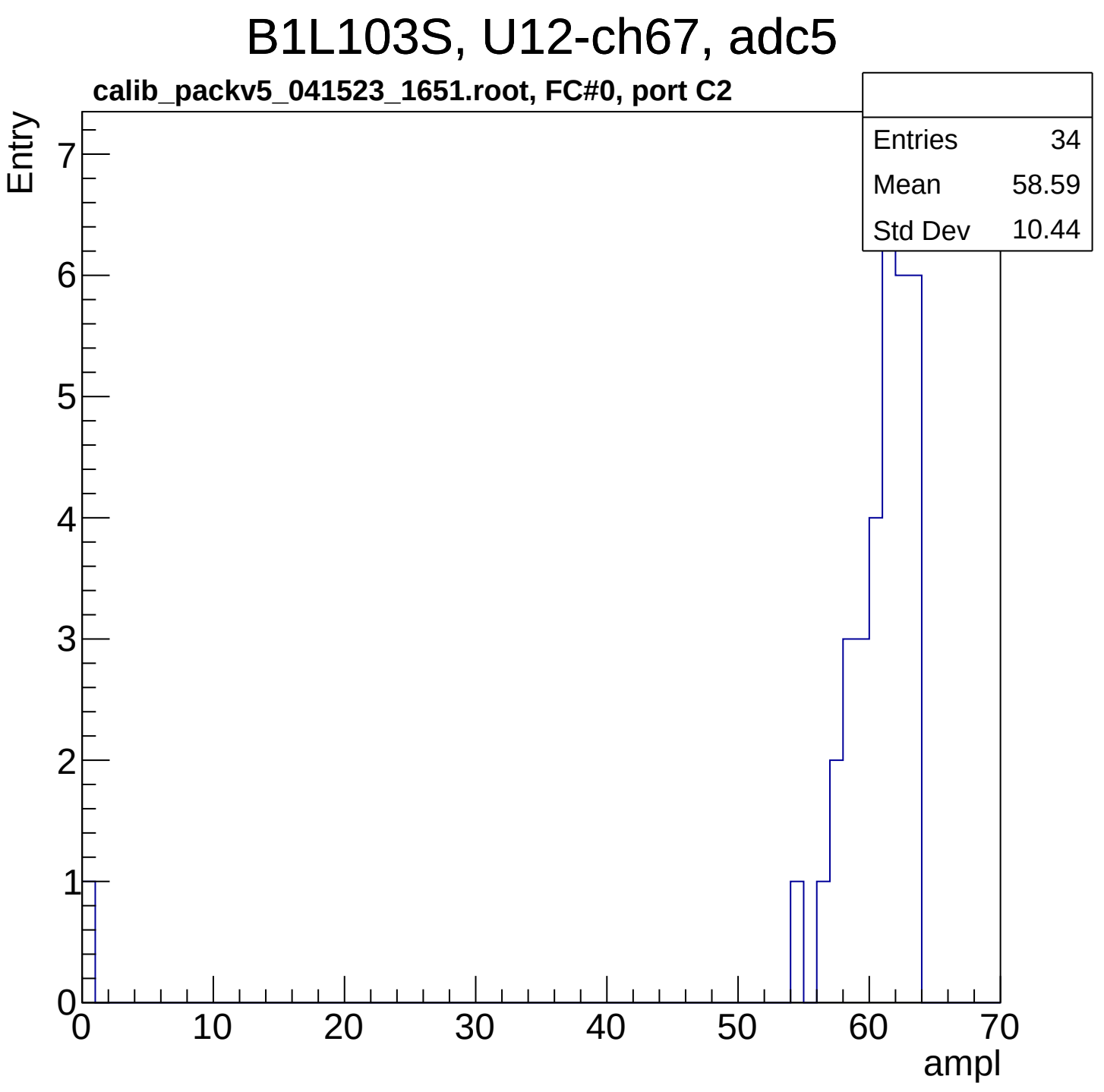
B1L103S, U12-ch67, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 34
Mean 58.59
Std Dev 10.44
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
50
60
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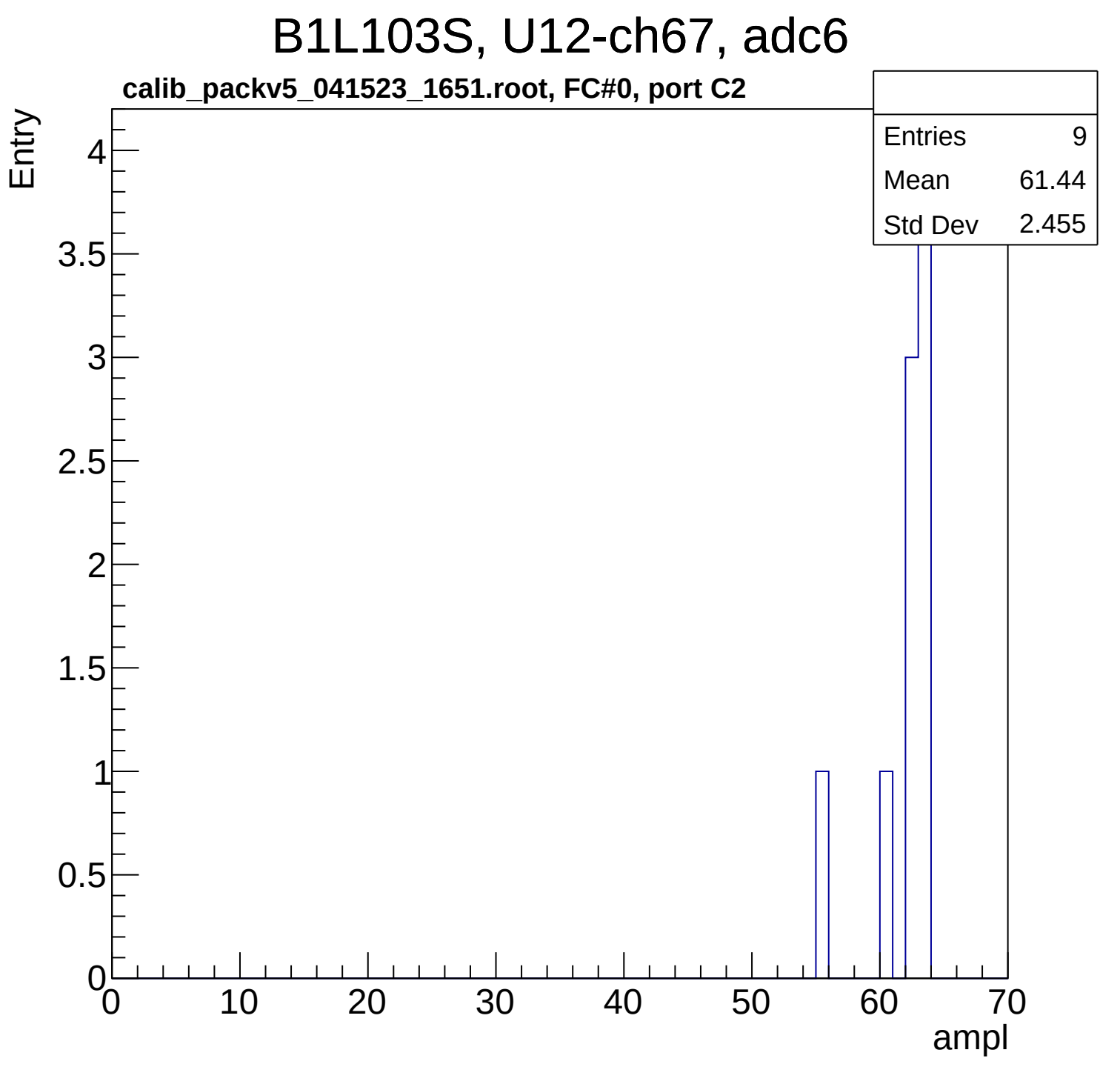
B1L103S, U12-ch67, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.44
Std Dev 2.455
Entry
ampl
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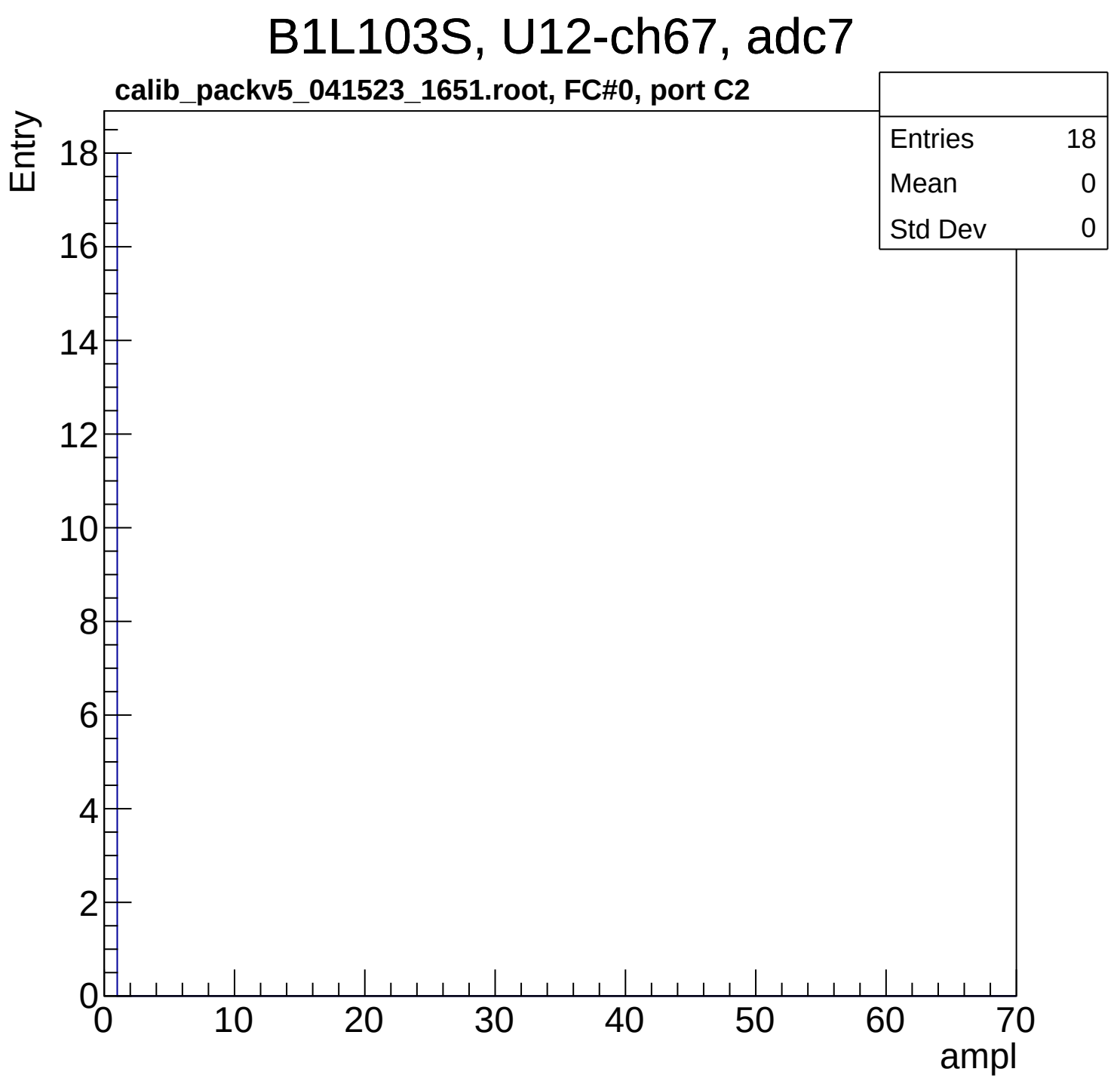
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U12-ch67, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
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6
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14
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18
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10
20
30
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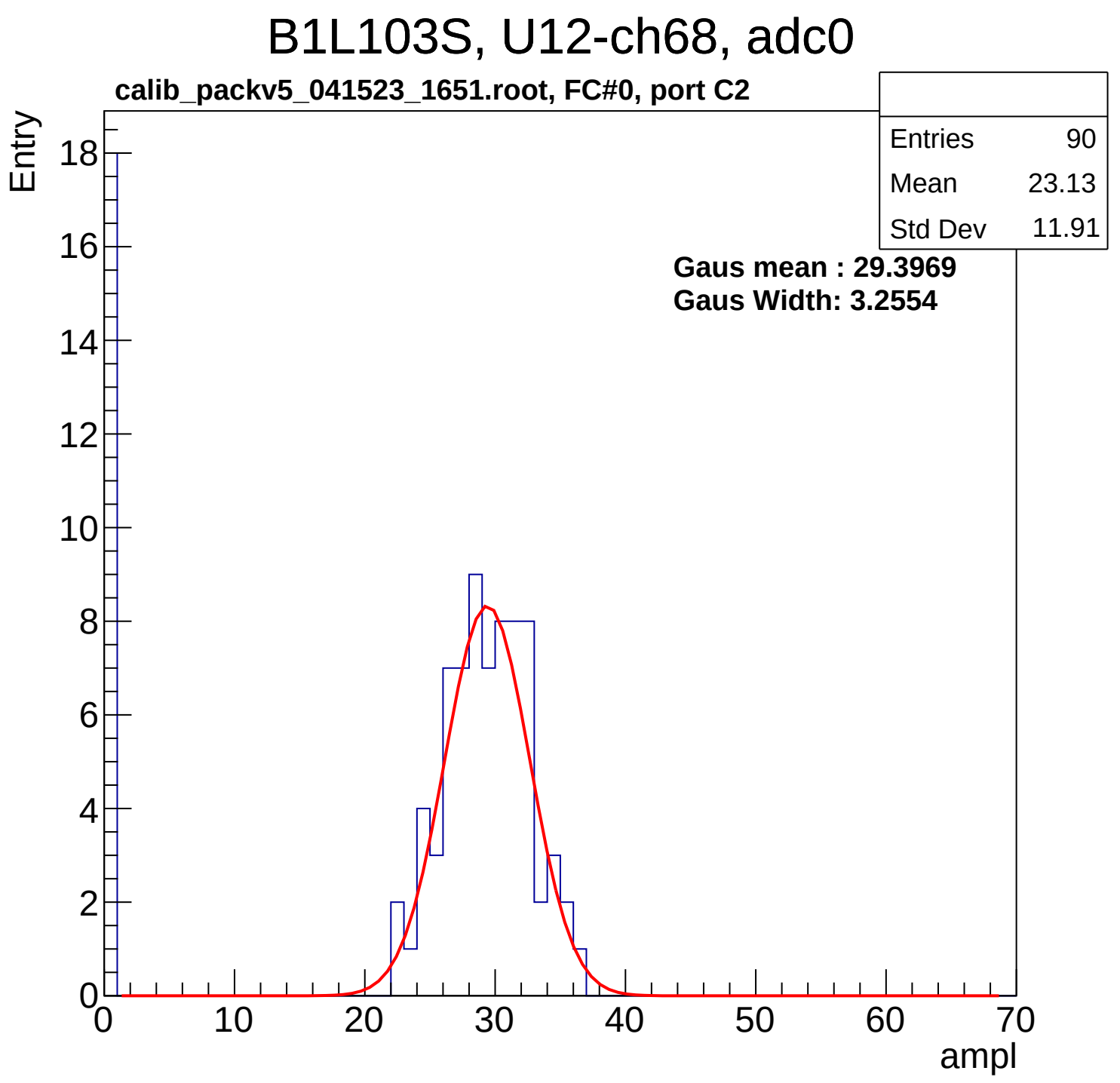
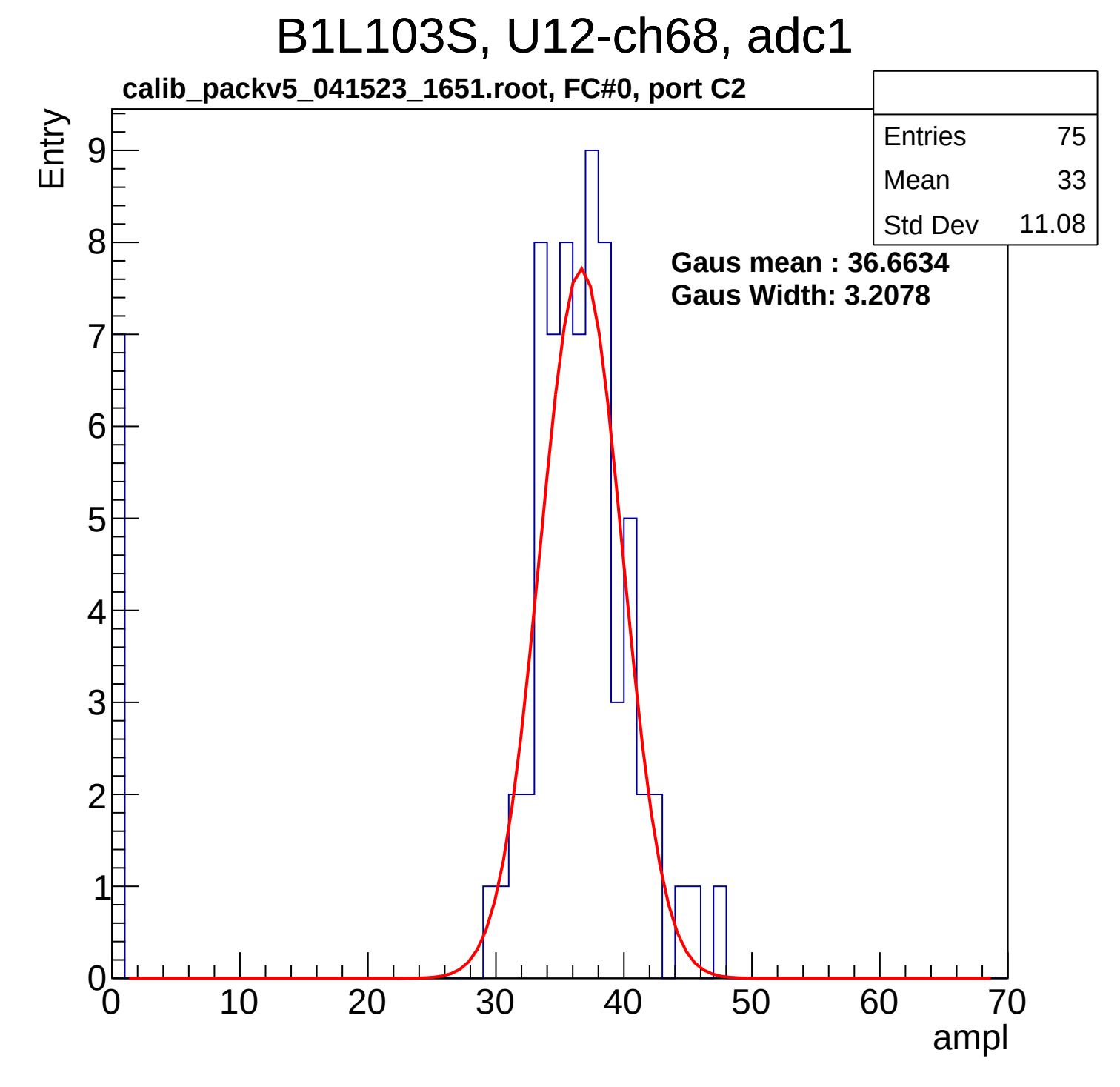
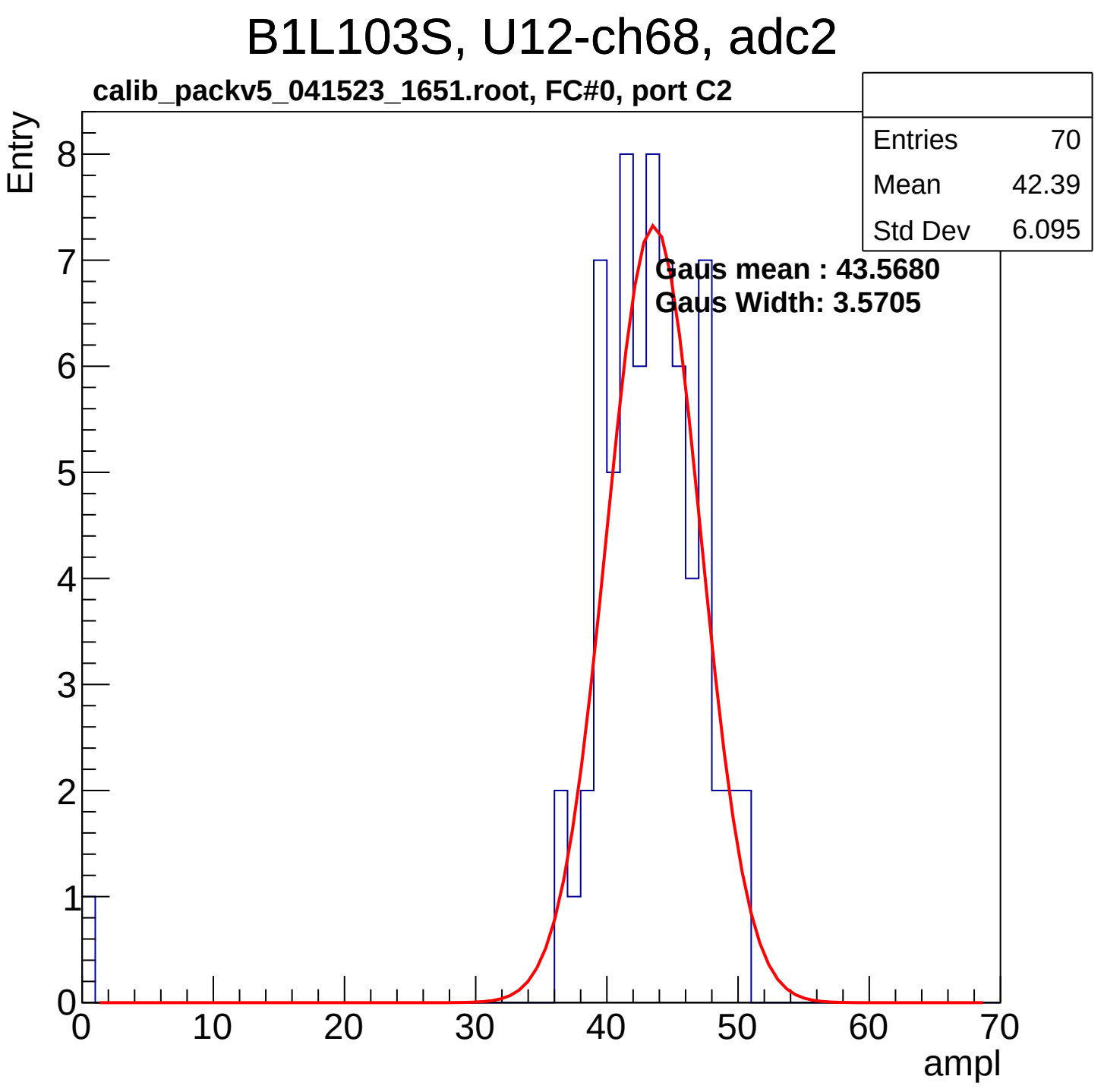
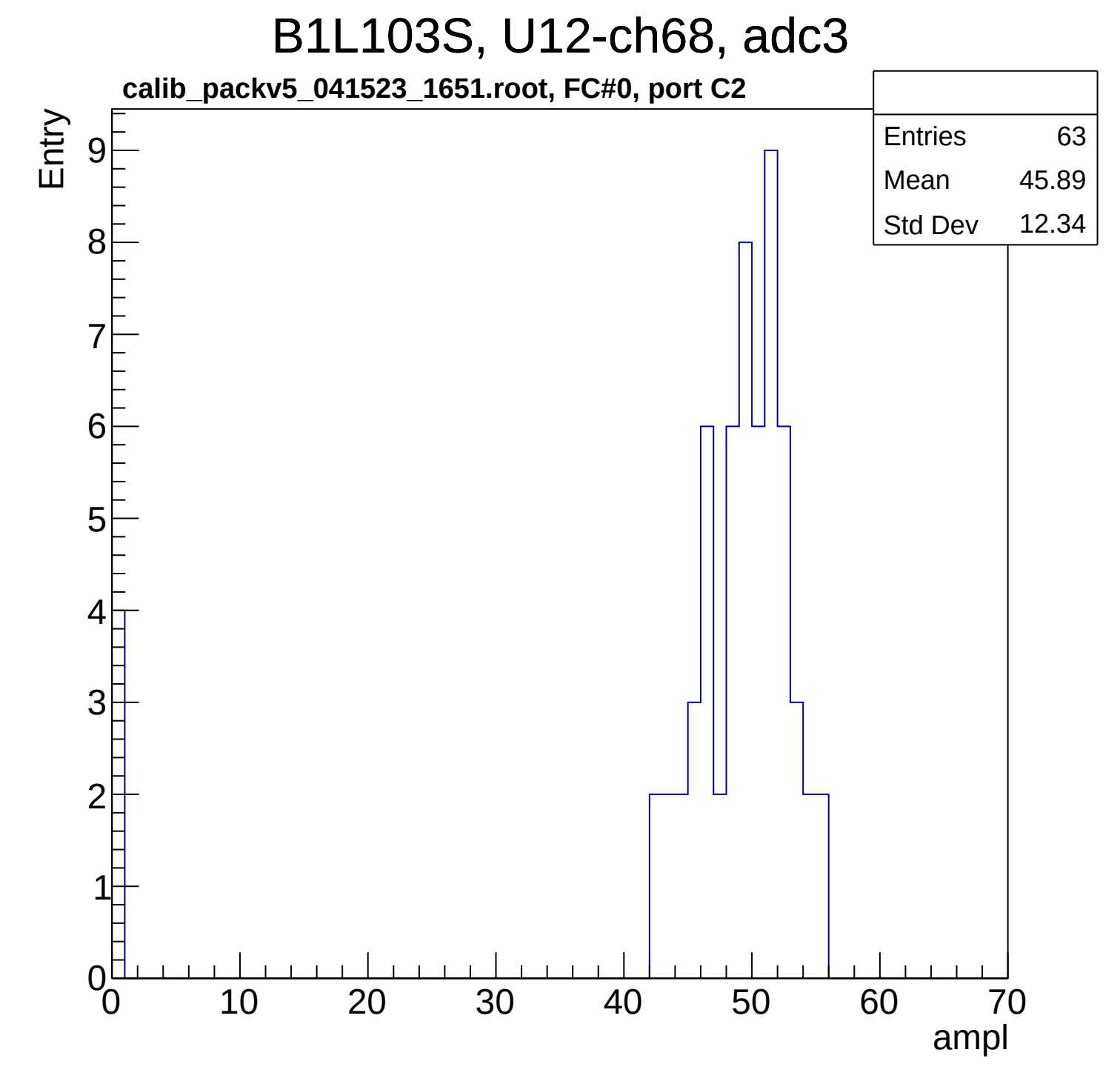
50
60
70
ampl


B1L103S, U12-ch68, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 23.13
Std Dev 11.91
Gaus mean : 29.3969
Gaus Width: 3.2554
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L103S, U12-ch68, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 33
Std Dev 11.08
Gaus mean : 36.6634
Gaus Width: 3.2078
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch68, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 42.39
Std Dev 6.095
Gaus mean : 43.5680
Gaus Width: 3.5705
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U12-ch68, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 45.89
Std Dev 12.34
Entry
ampl
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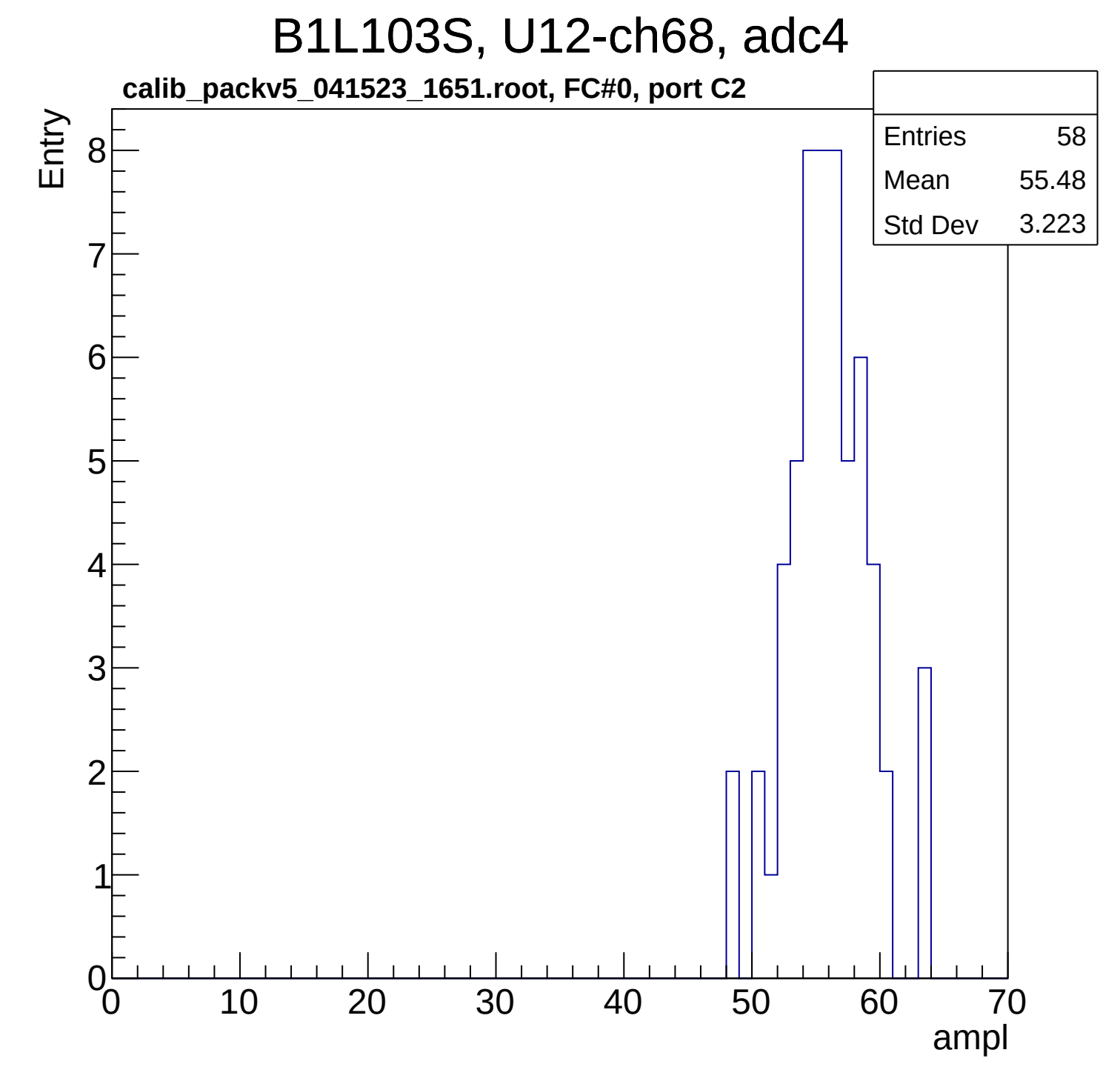
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch68, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 55.48
Std Dev 3.223
Entry
ampl
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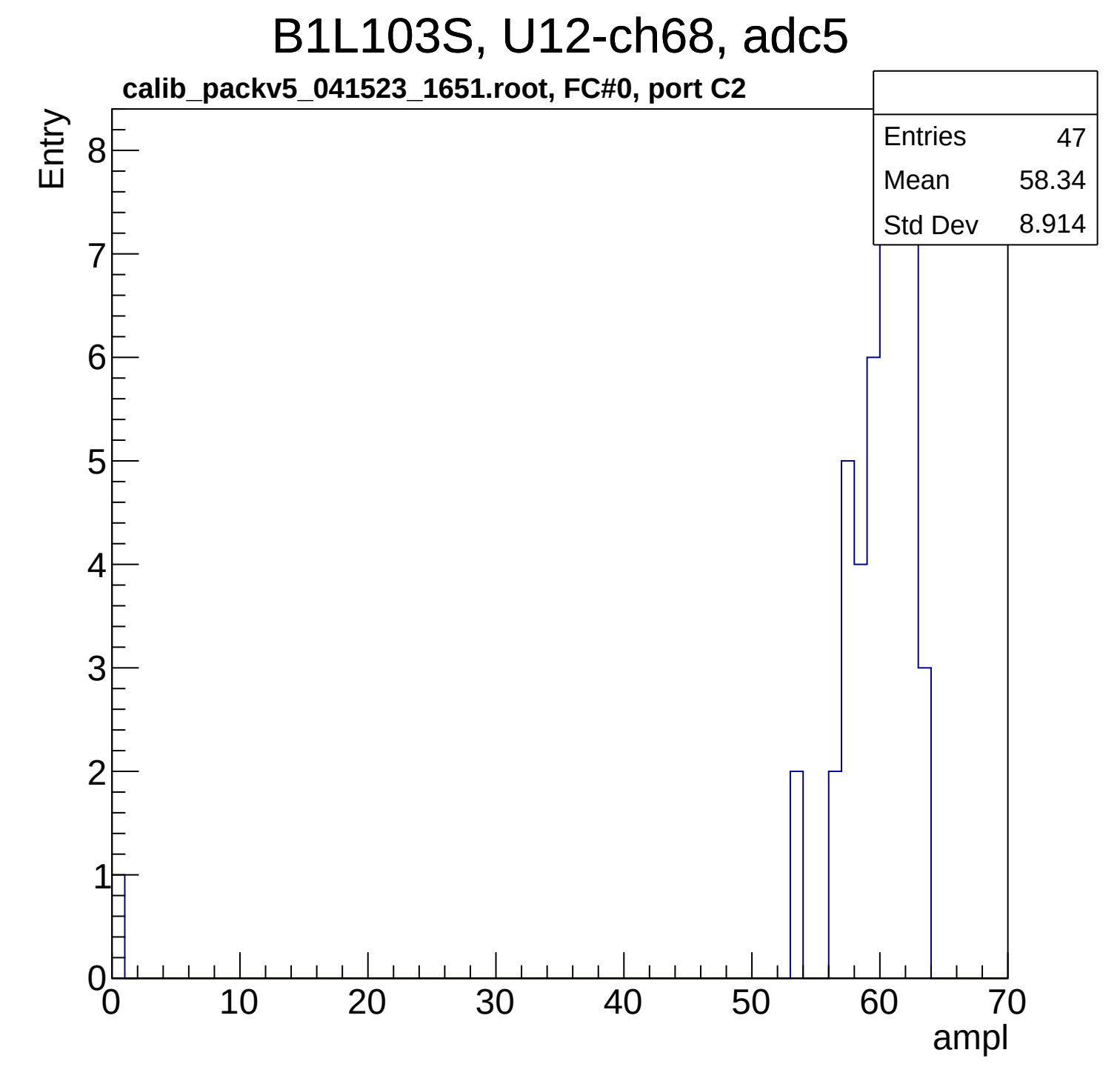
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U12-ch68, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 58.34
Std Dev 8.914
Entry
ampl
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2
3
4
5
6
7
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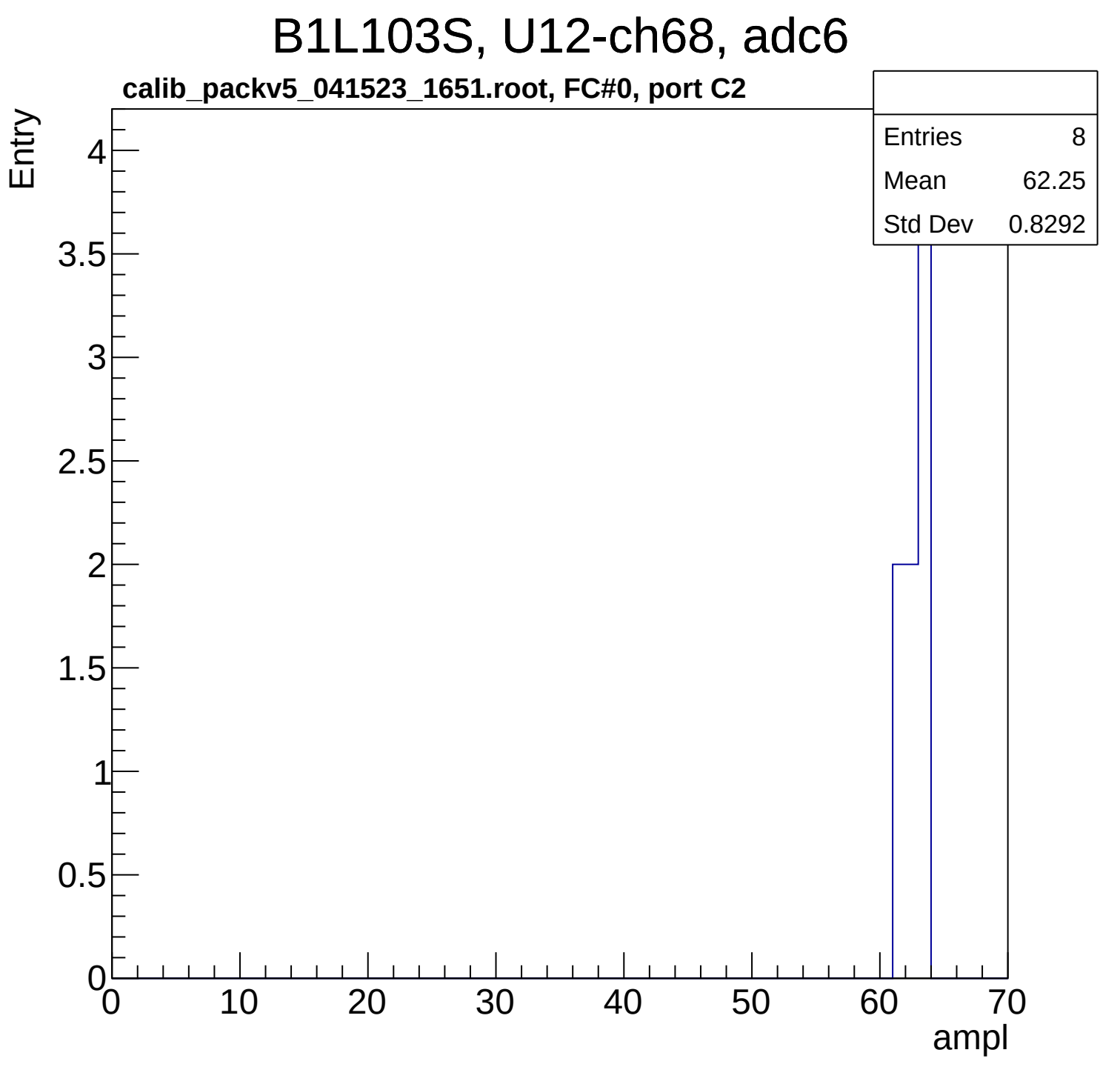
60
70


B1L103S, U12-ch68, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62.25
Std Dev 0.8292
Entry
ampl
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0.5
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1.5
2
2.5
3
3.5
4
0
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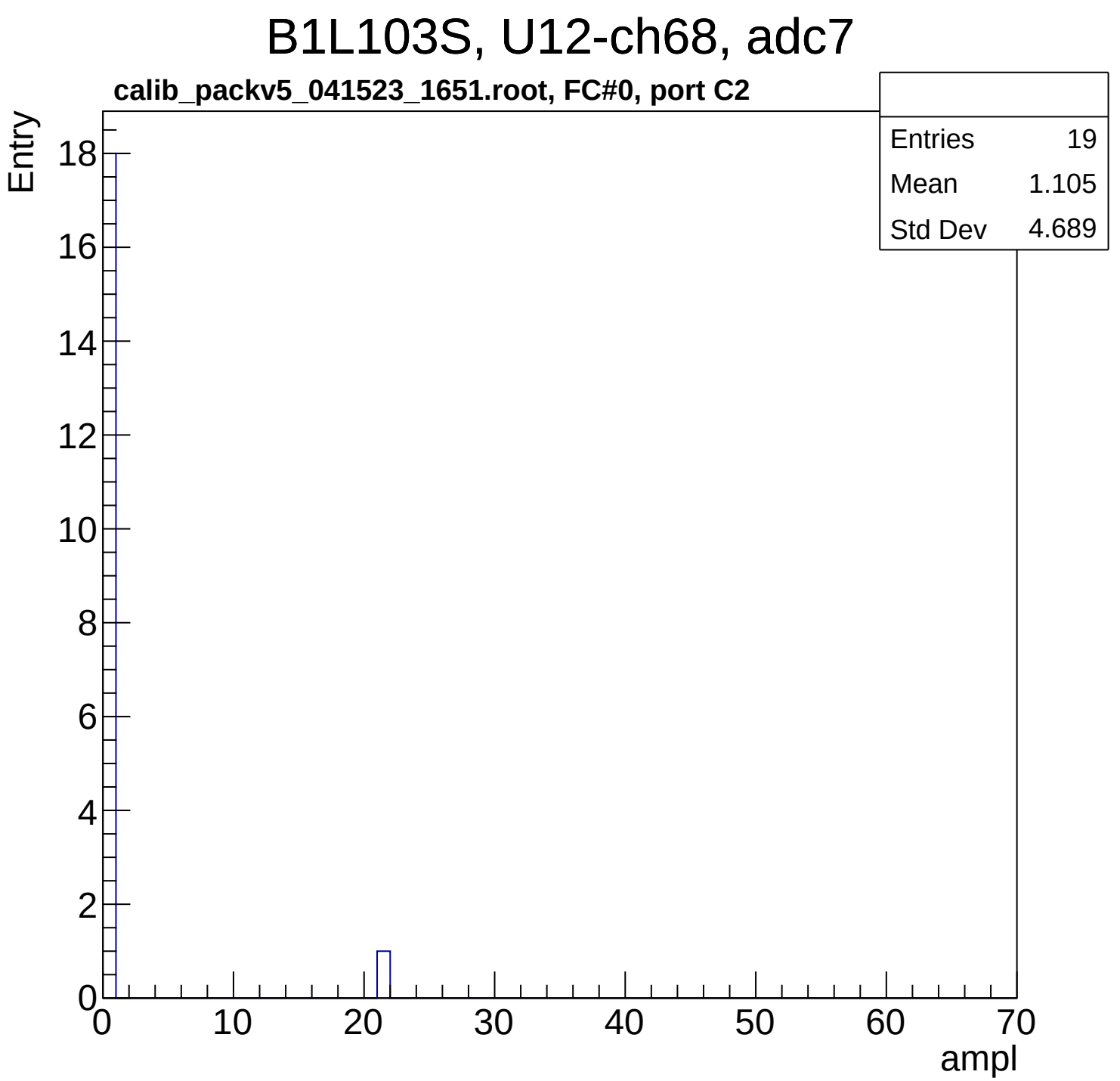
20
30
40
50
60
70


B1L103S, U12-ch68, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
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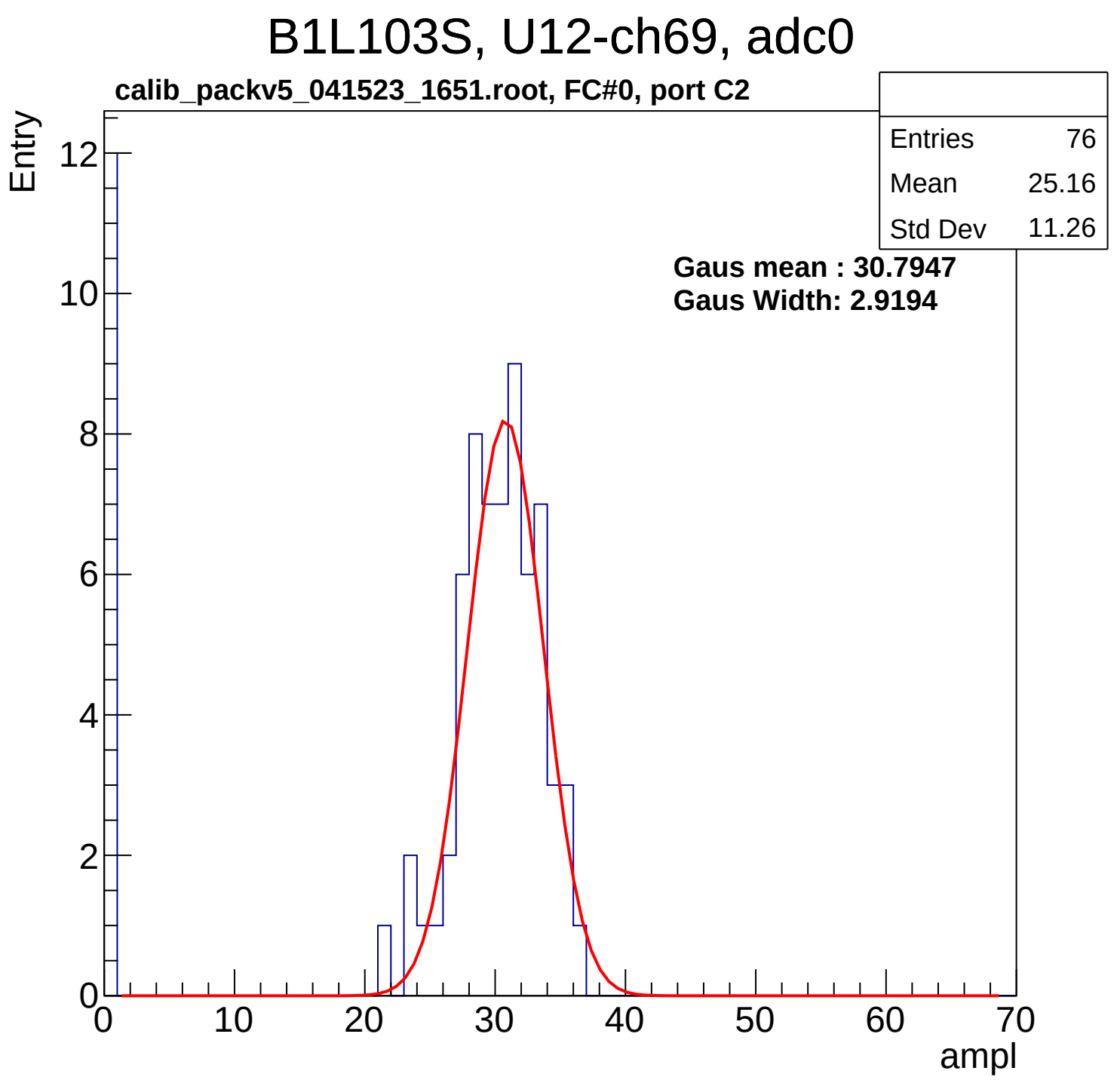
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch69, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 25.16
Std Dev 11.26
Gaus mean : 30.7947
Gaus Width: 2.9194
Entry
ampl
0
2
4
6
8
10
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0
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20
30
40
50
60
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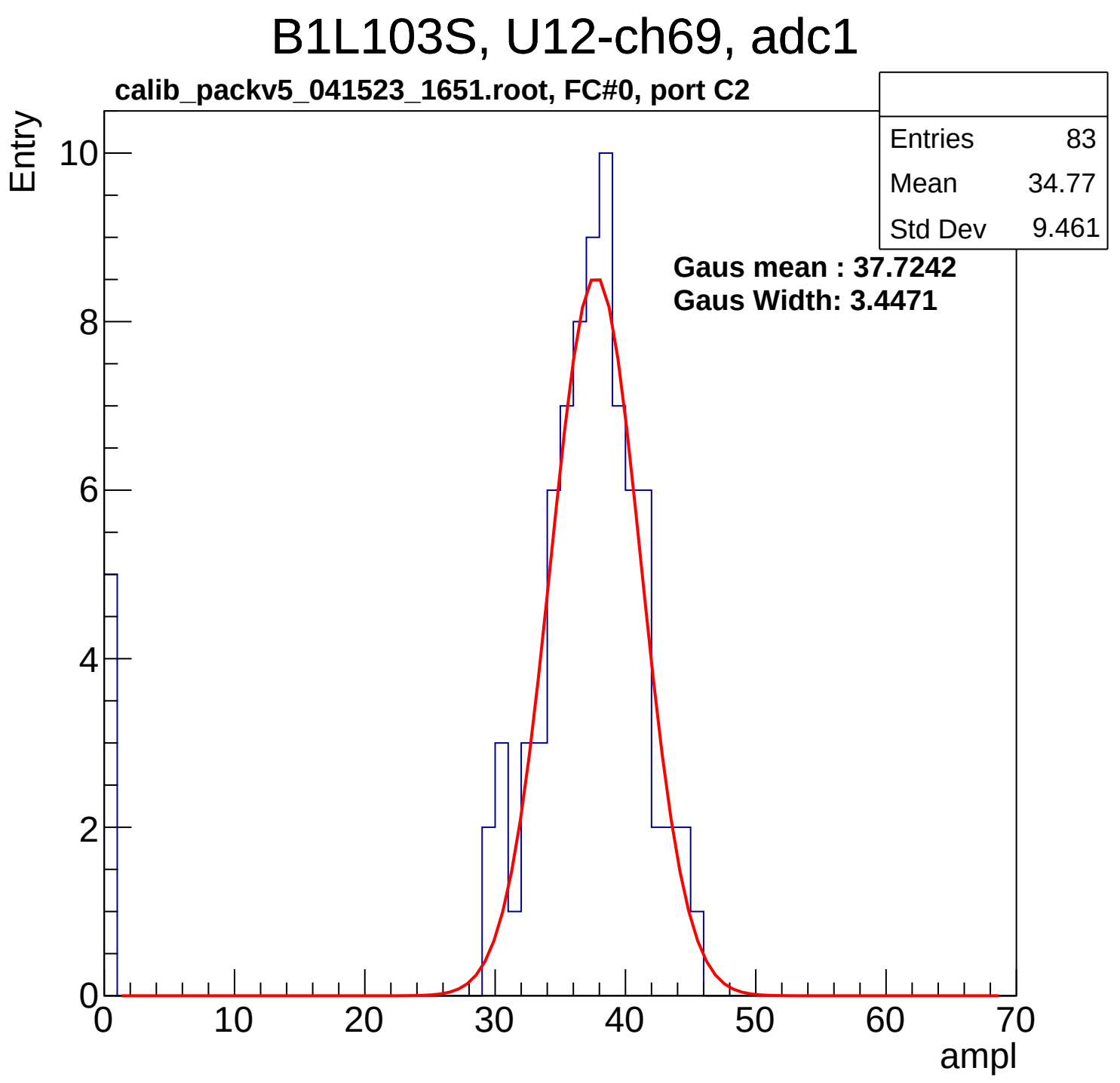
B1L103S, U12-ch69, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 34.77
Std Dev 9.461
Gaus mean : 37.7242
Gaus Width: 3.4471
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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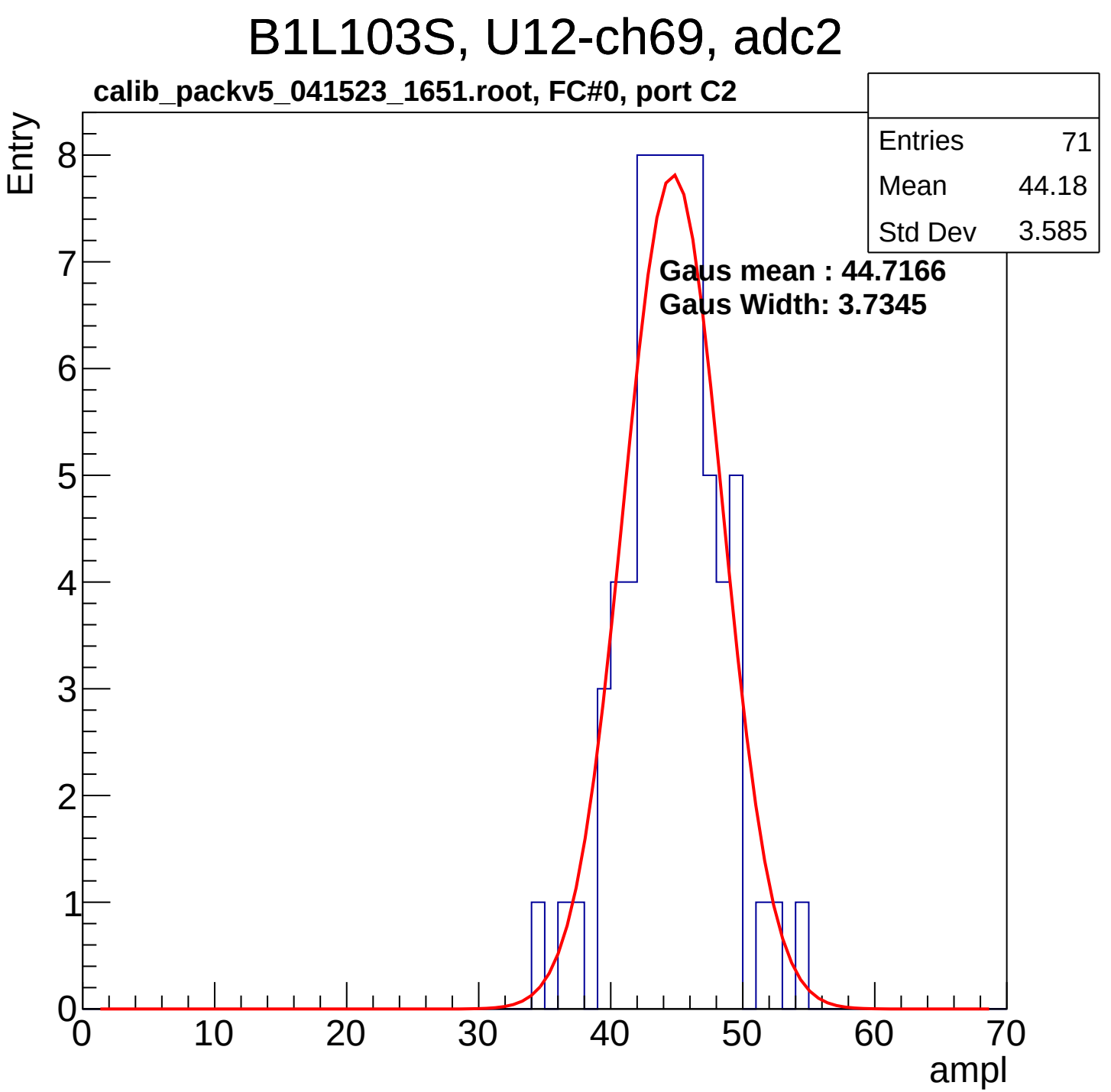
B1L103S, U12-ch69, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 44.18
Std Dev 3.585
Gaus mean : 44.7166
Gaus Width: 3.7345
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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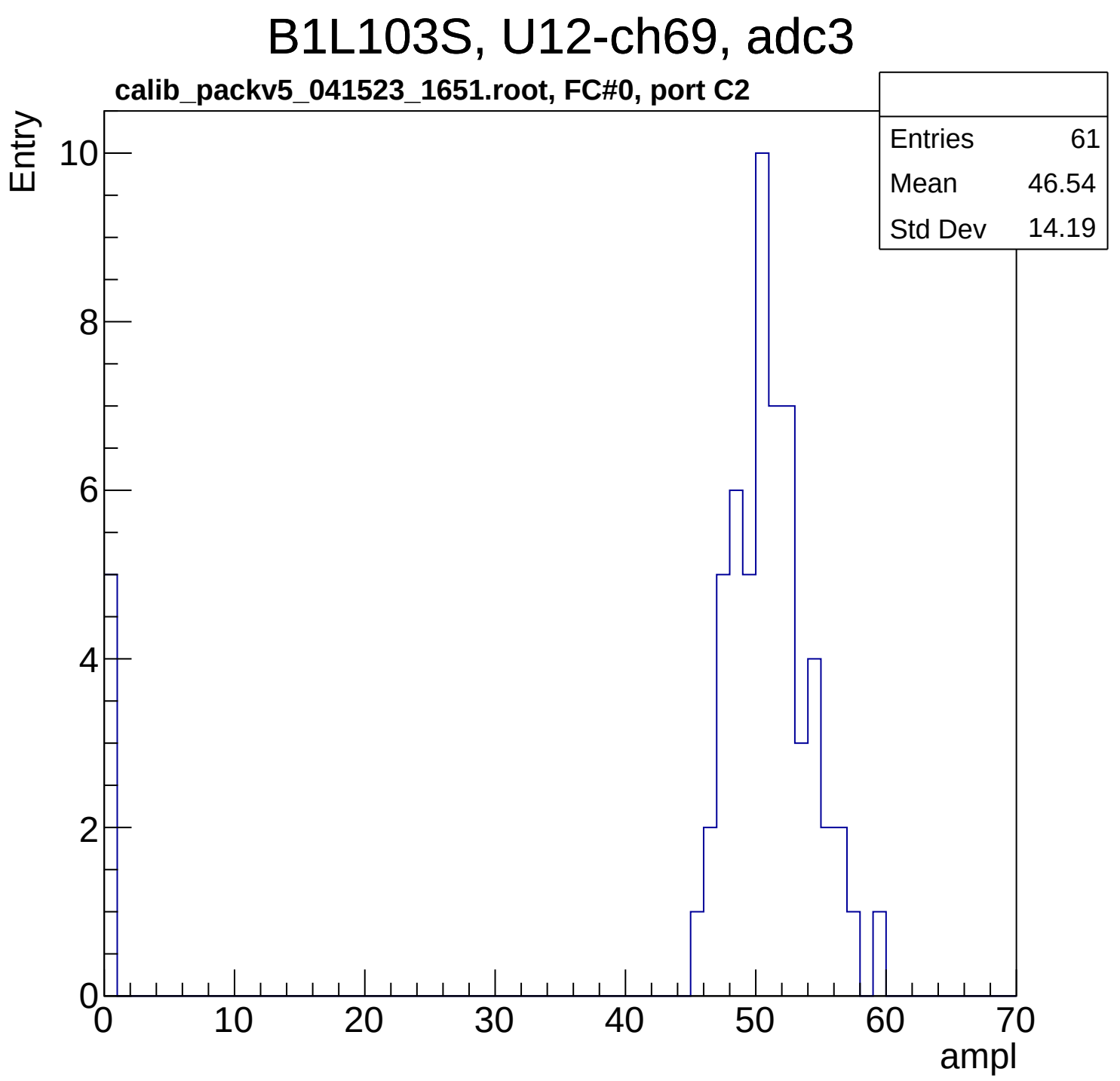
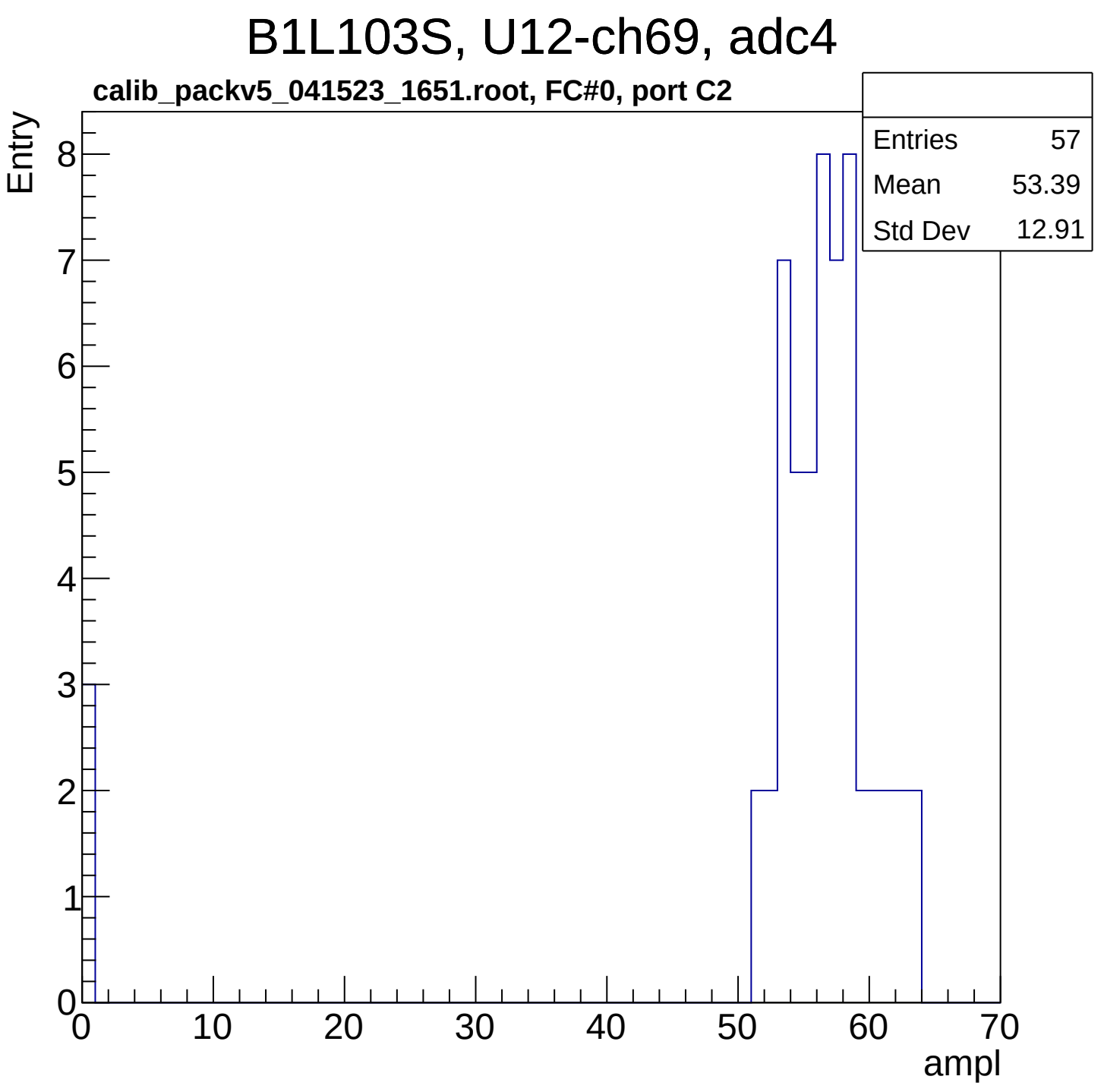

B1L103S, U12-ch69, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 46.54
Std Dev 14.19
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch69, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 53.39
Std Dev 12.91
Entry
ampl
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1
2
3
4
5
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7
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0
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60
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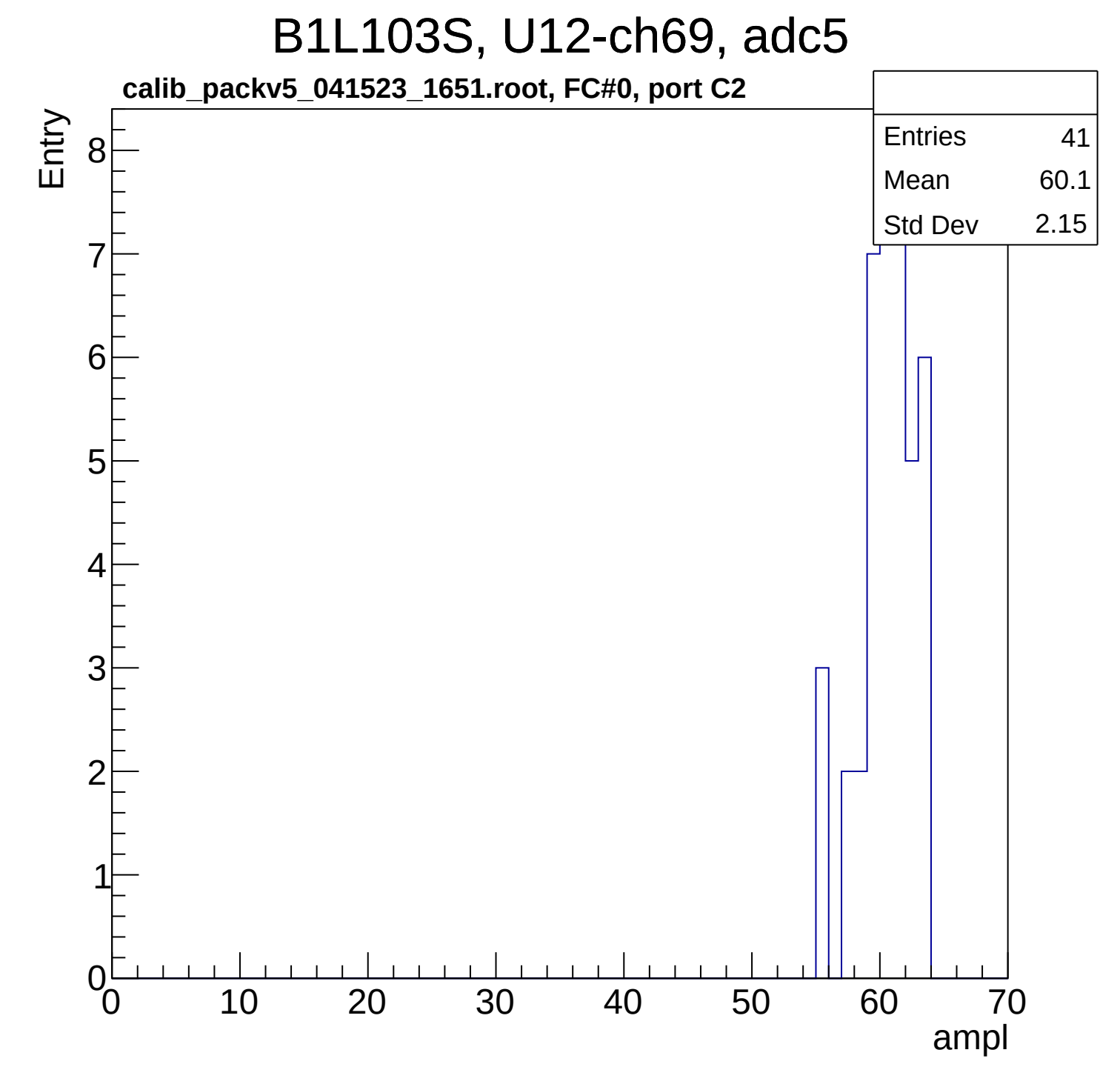
B1L103S, U12-ch69, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 60.1
Std Dev 2.15
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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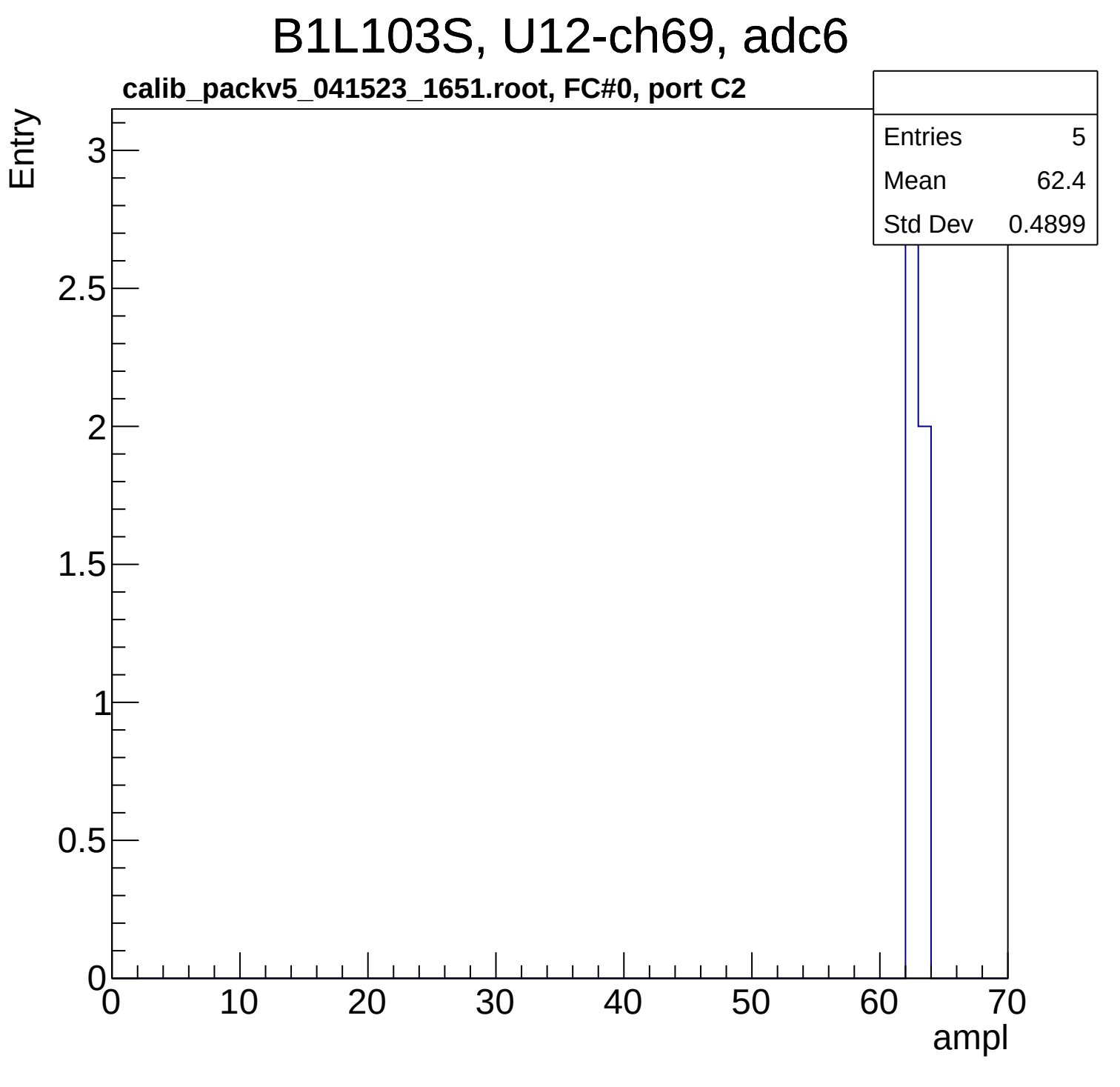
B1L103S, U12-ch69, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 62.4
Std Dev 0.4899
Entry
ampl
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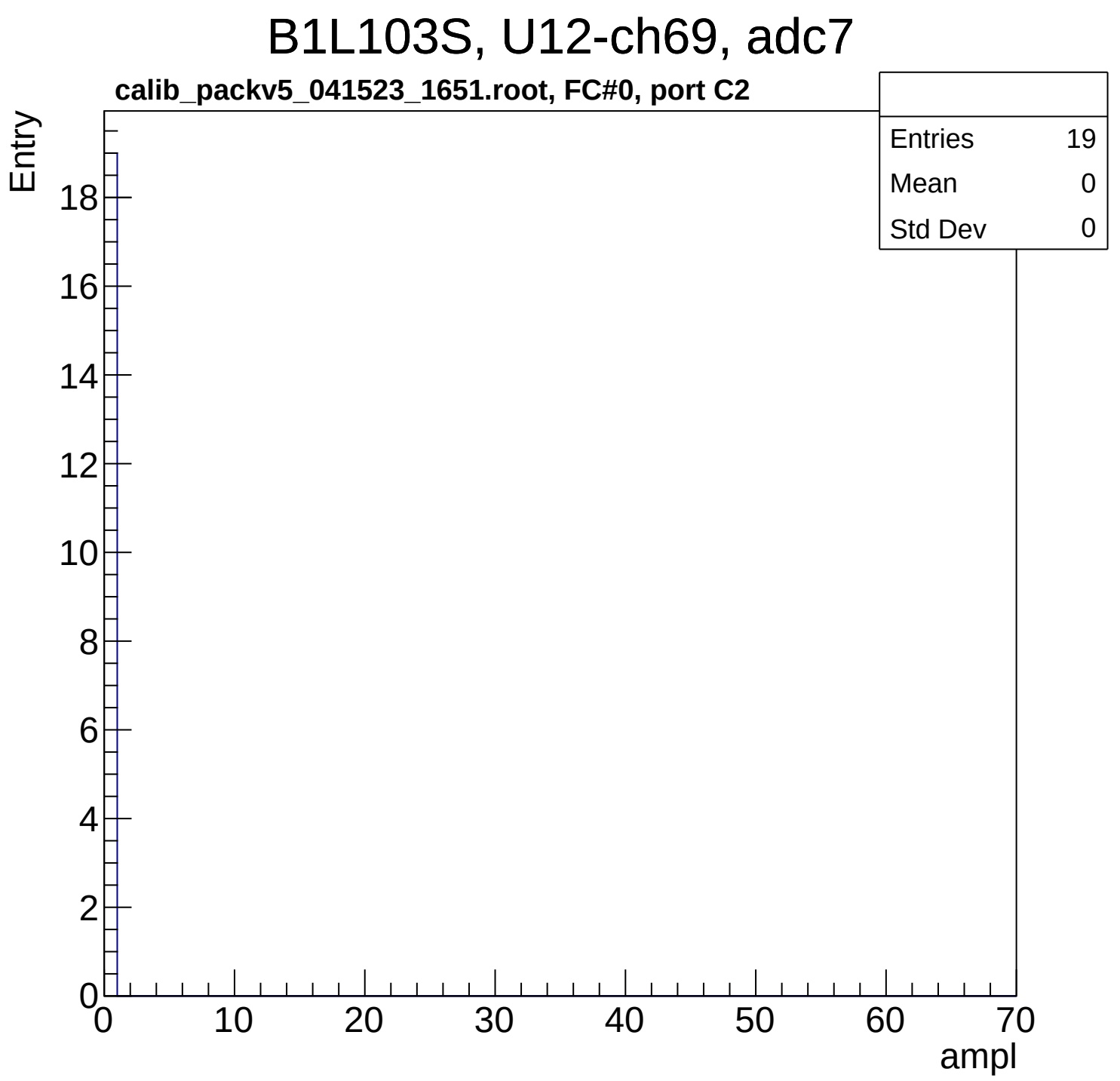
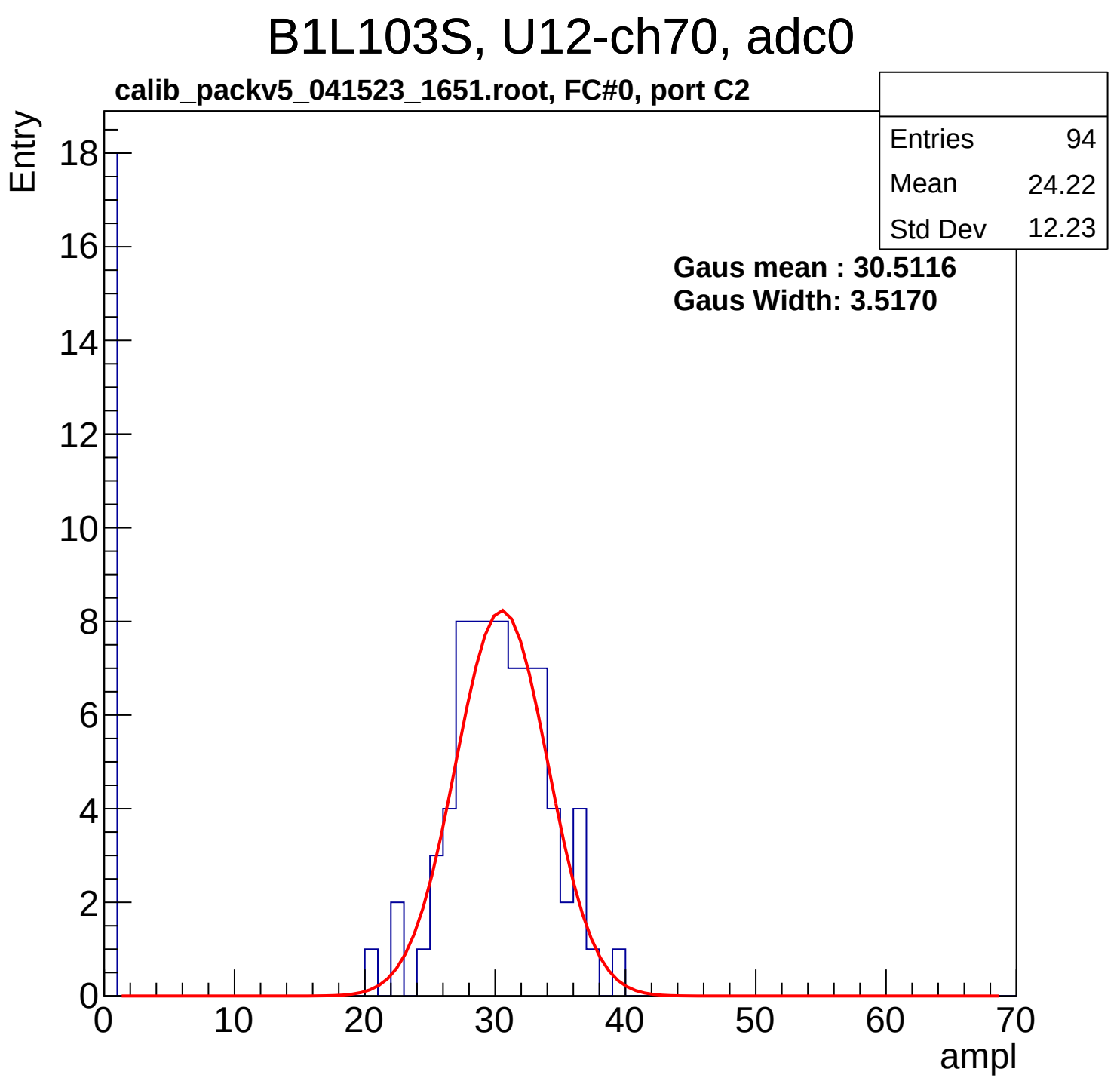
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U12-ch69, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch70, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 24.22
Std Dev 12.23
Gaus mean : 30.5116
Gaus Width: 3.5170
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
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60
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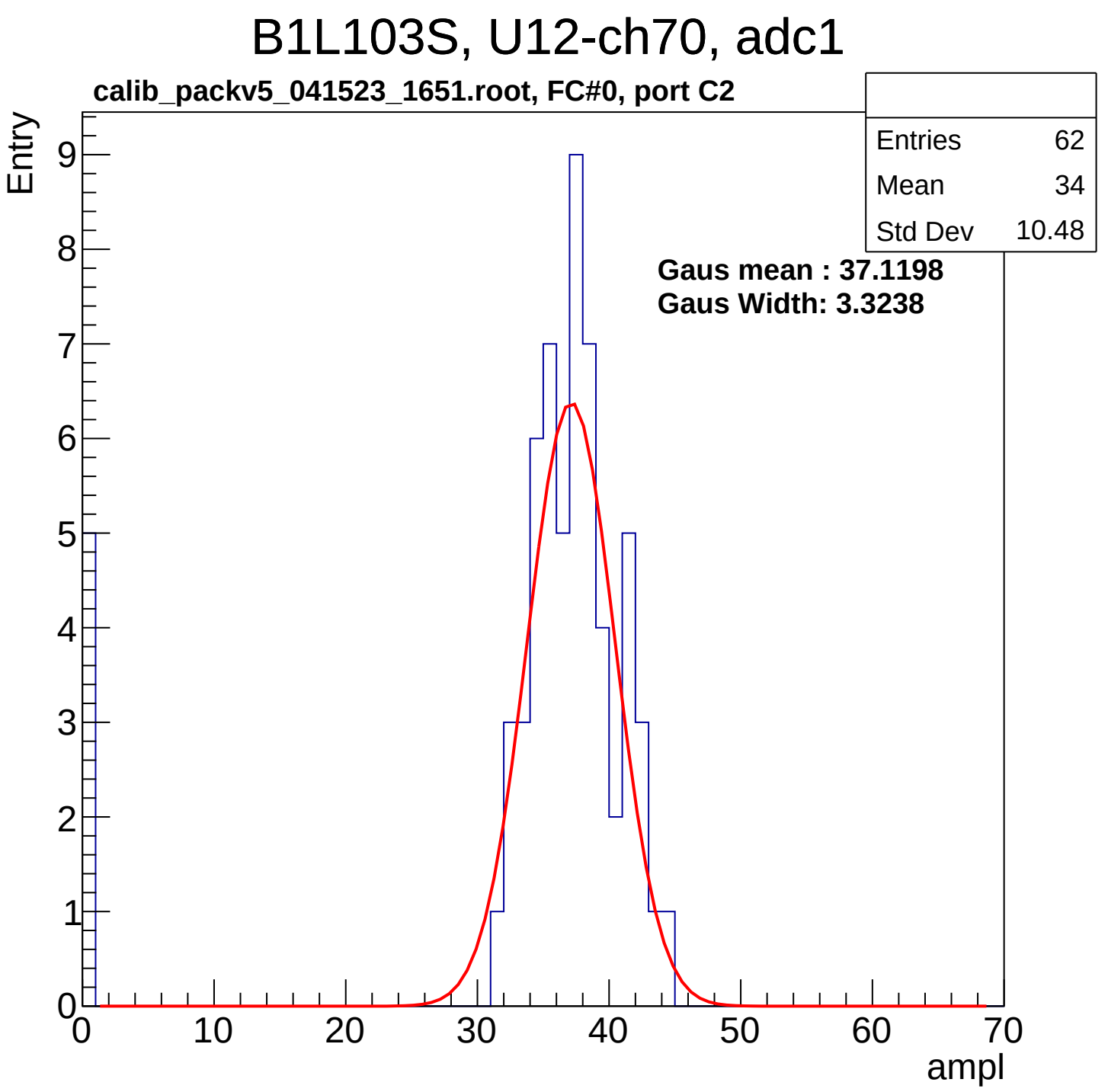
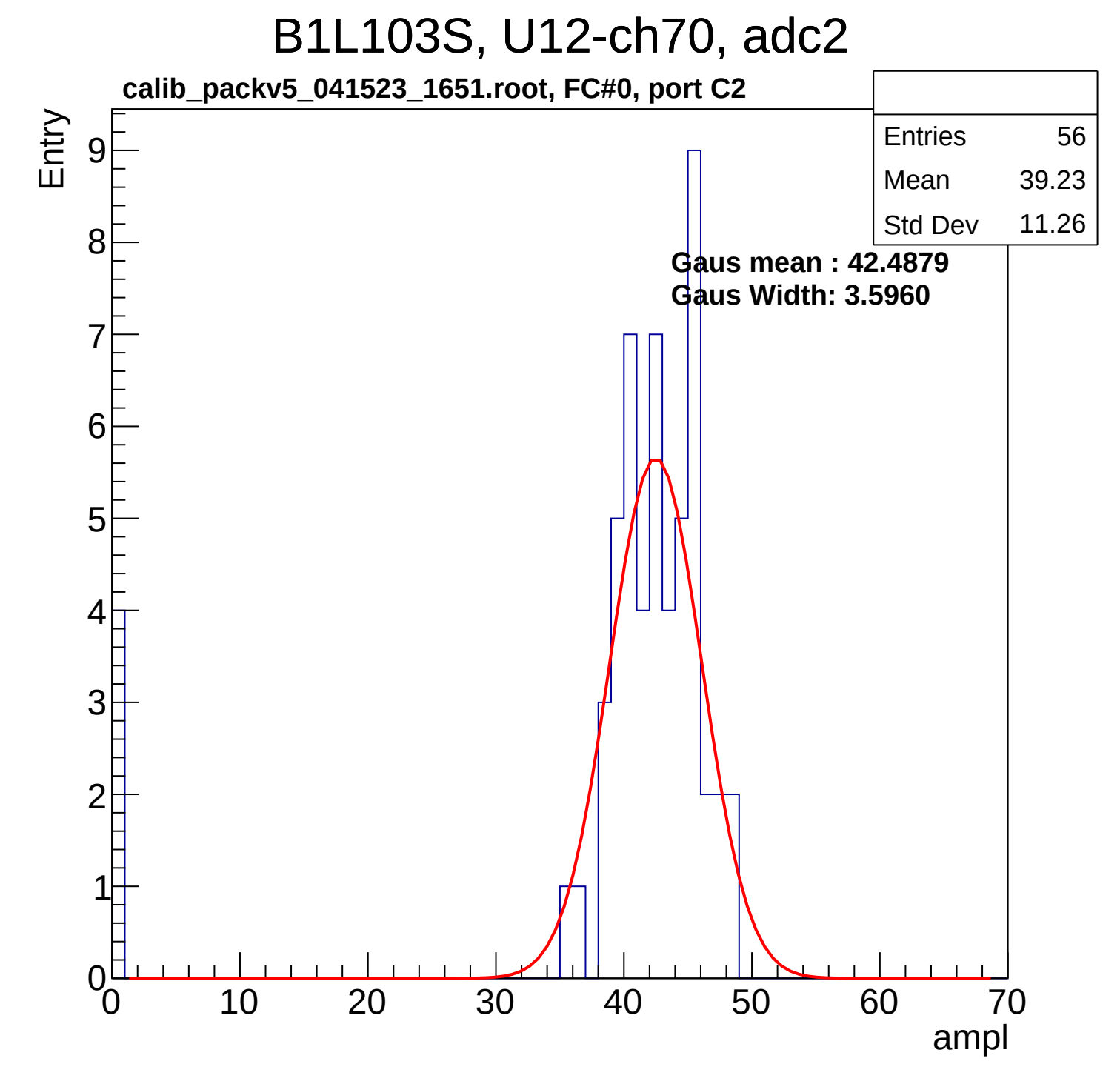

B1L103S, U12-ch70, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 34
Std Dev 10.48
Gaus mean : 37.1198
Gaus Width: 3.3238
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch70, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 39.23
Std Dev 11.26
Gaus mean : 42.4879
Gaus Width: 3.5960
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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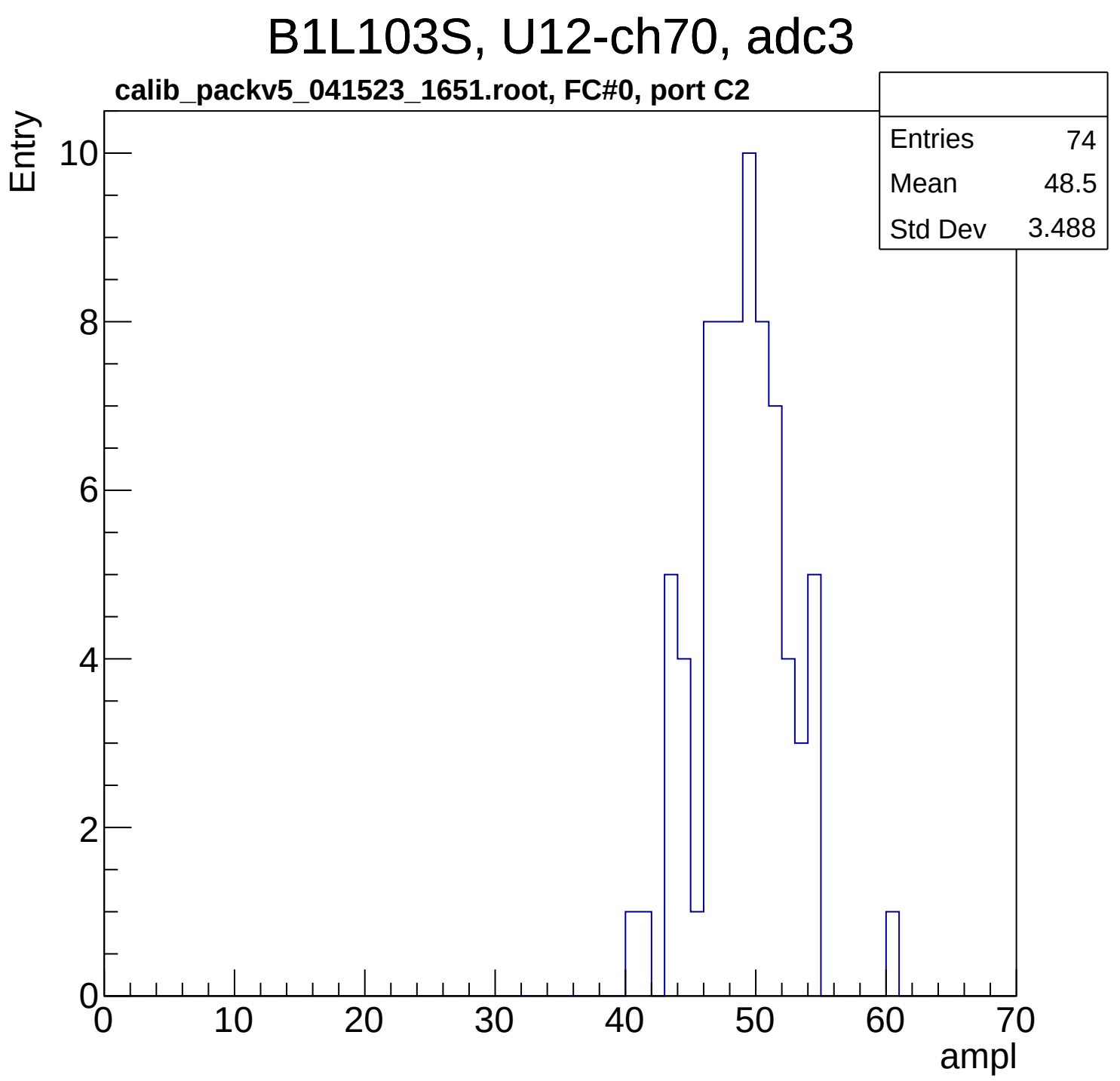
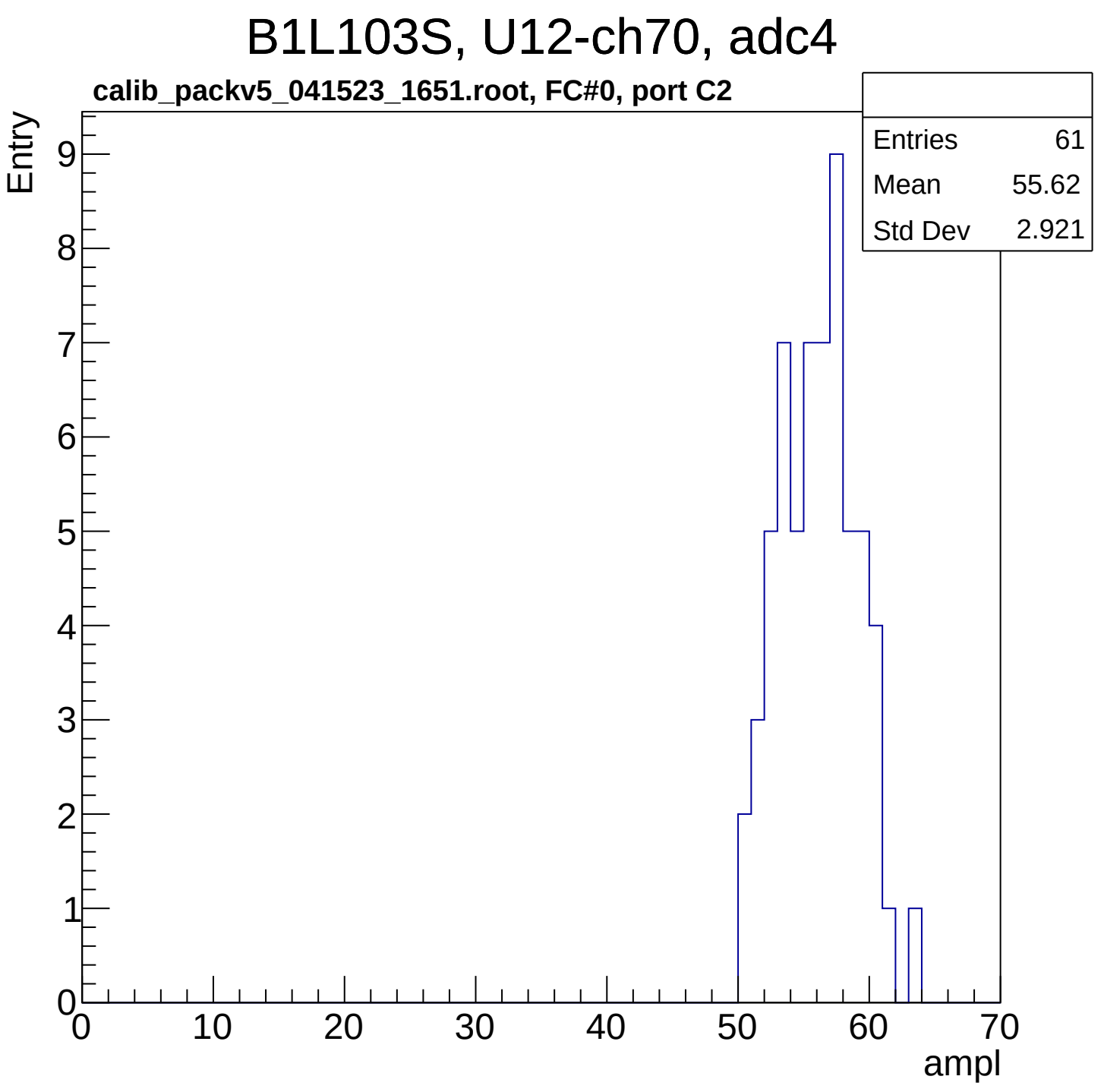
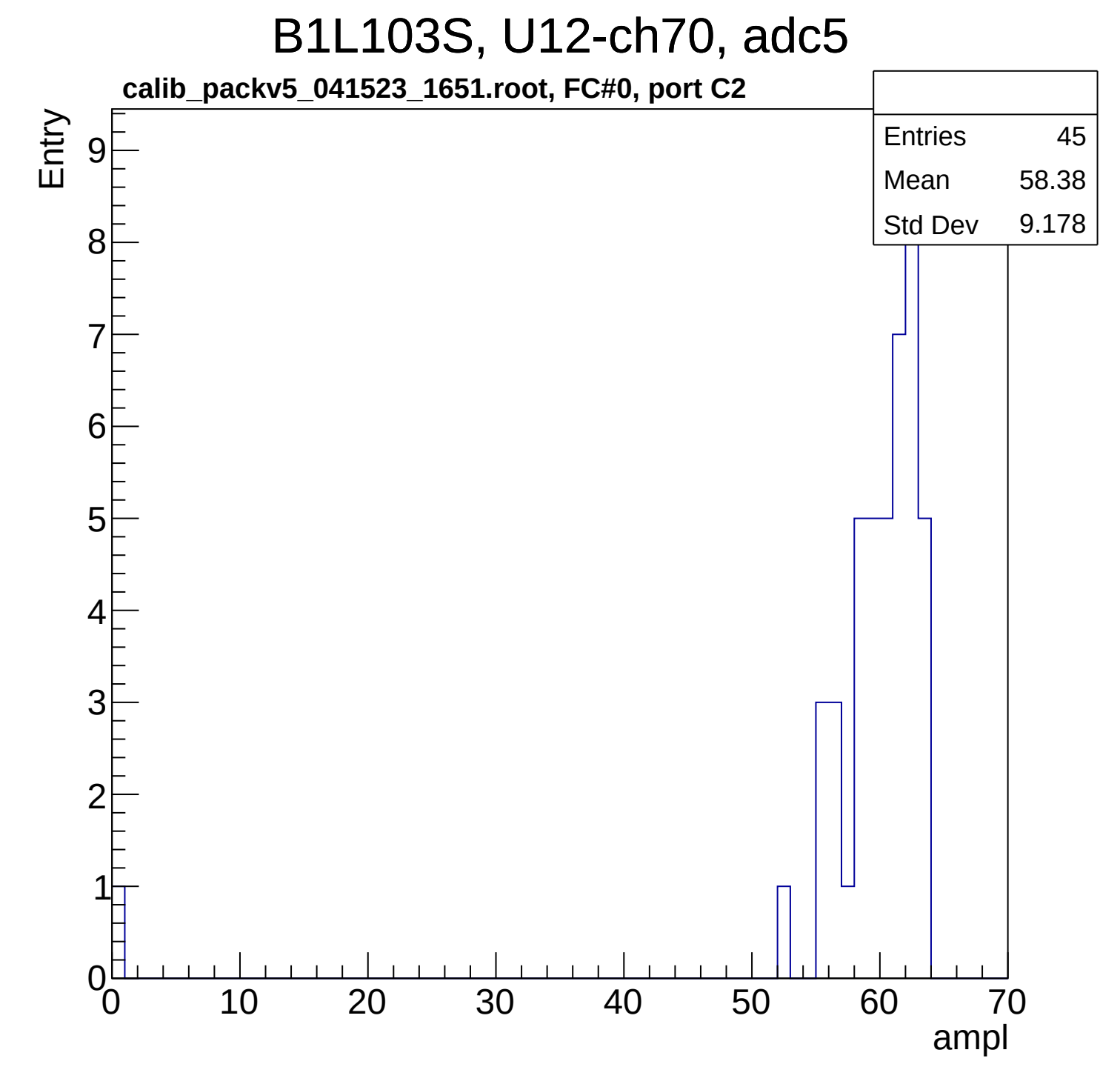

B1L103S, U12-ch70, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 48.5
Std Dev 3.488
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch70, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 55.62
Std Dev 2.921
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch70, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.38
Std Dev 9.178
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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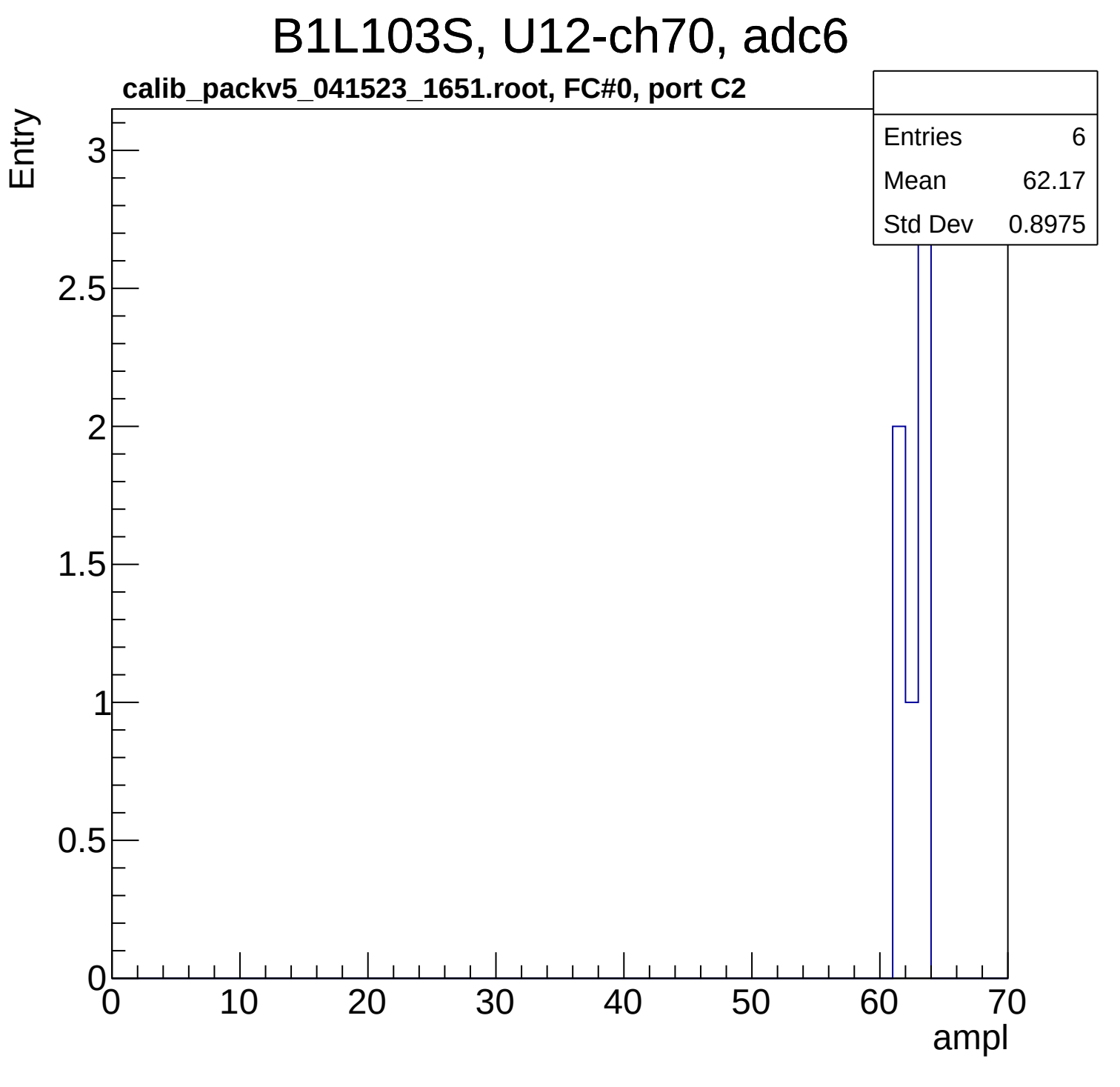
B1L103S, U12-ch70, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.17
Std Dev 0.8975
Entry
ampl
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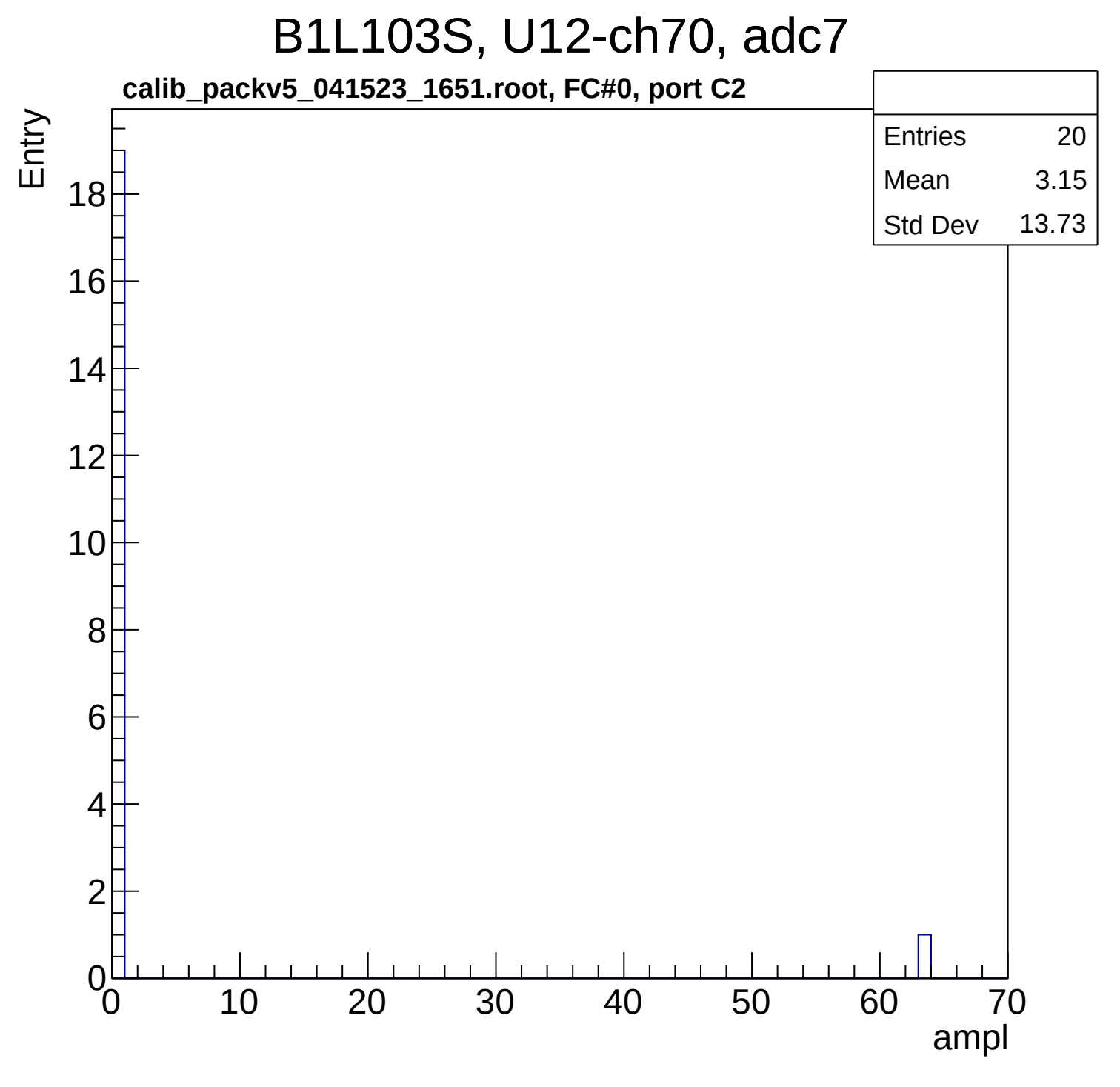
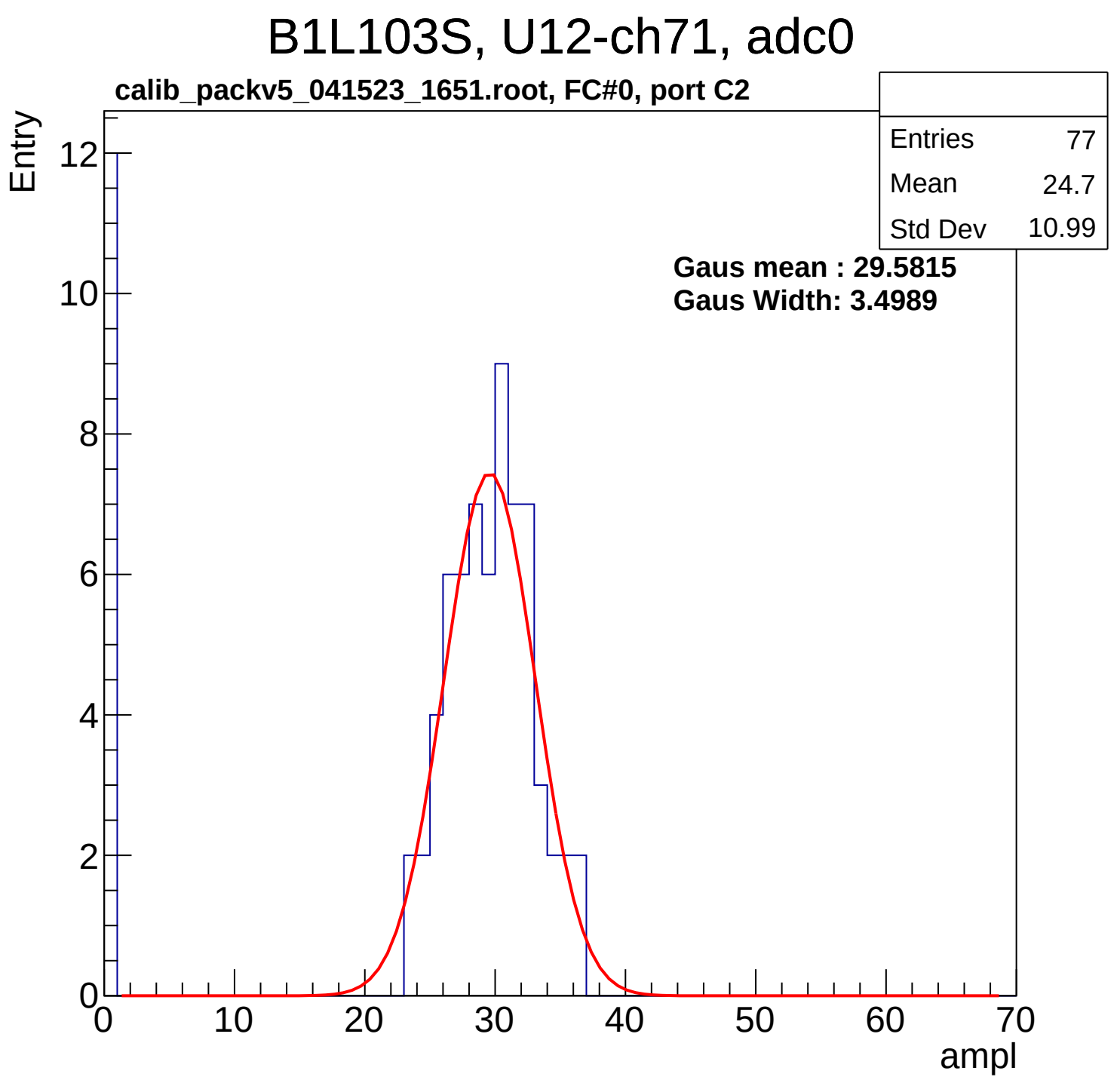
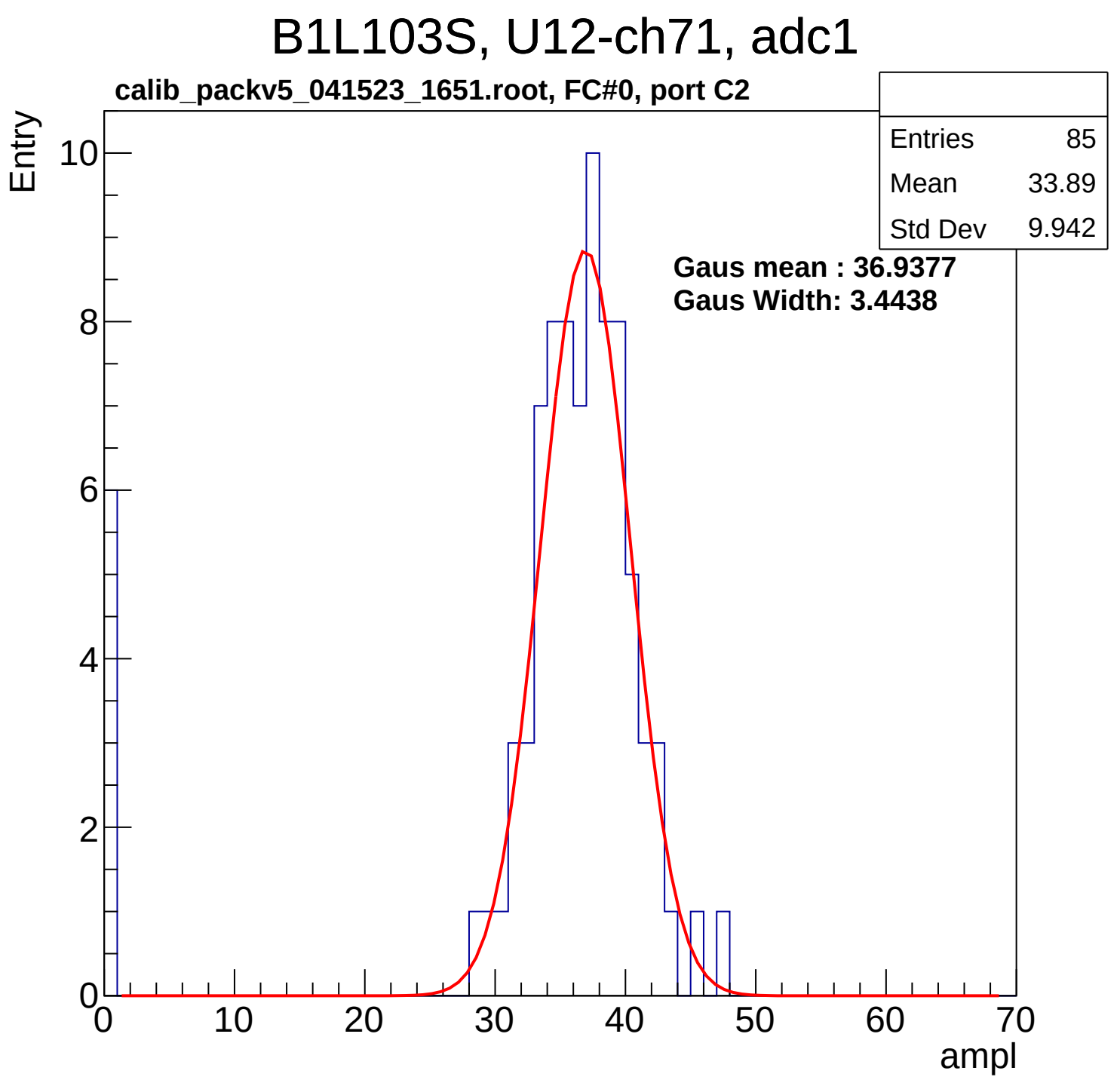
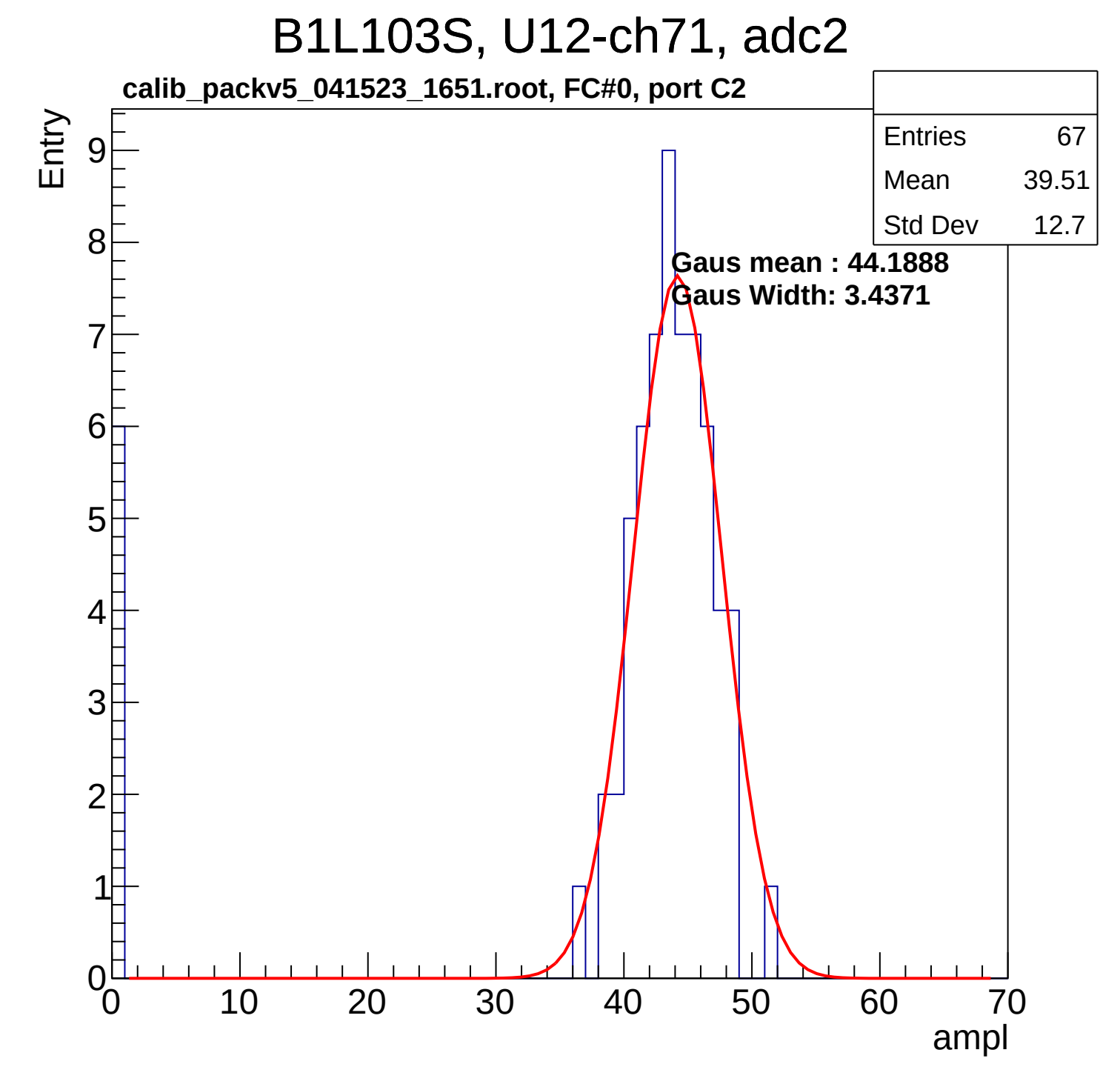
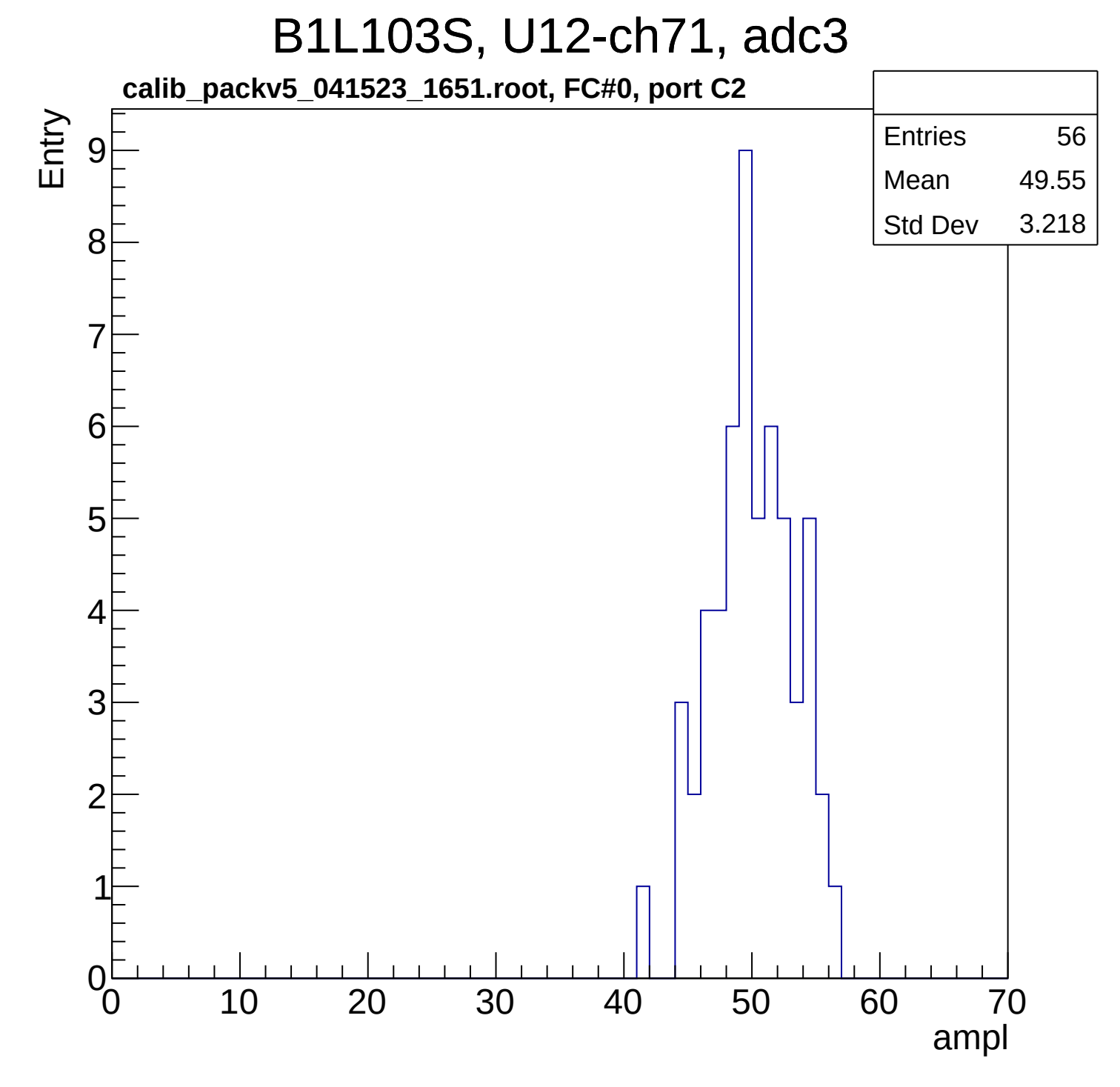
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U12-ch70, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch71, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 24.7
Std Dev 10.99
Gaus mean : 29.5815
Gaus Width: 3.4989
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U12-ch71, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 33.89
Std Dev 9.942
Gaus mean : 36.9377
Gaus Width: 3.4438
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch71, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 39.51
Std Dev 12.7
Gaus mean : 44.1888
Gaus Width: 3.4371
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch71, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 49.55
Std Dev 3.218
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
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60
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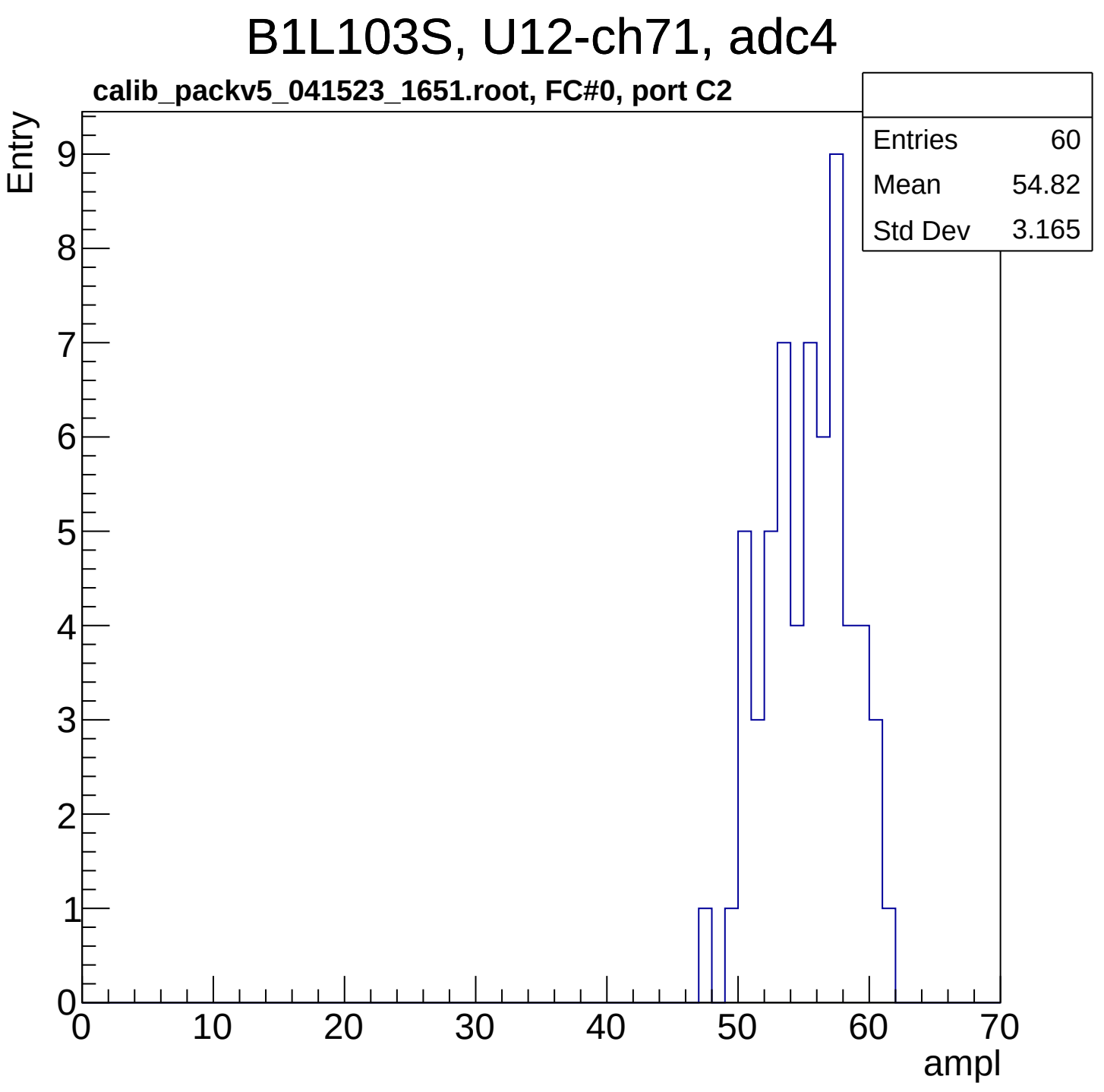
B1L103S, U12-ch71, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 54.82
Std Dev 3.165
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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40
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60
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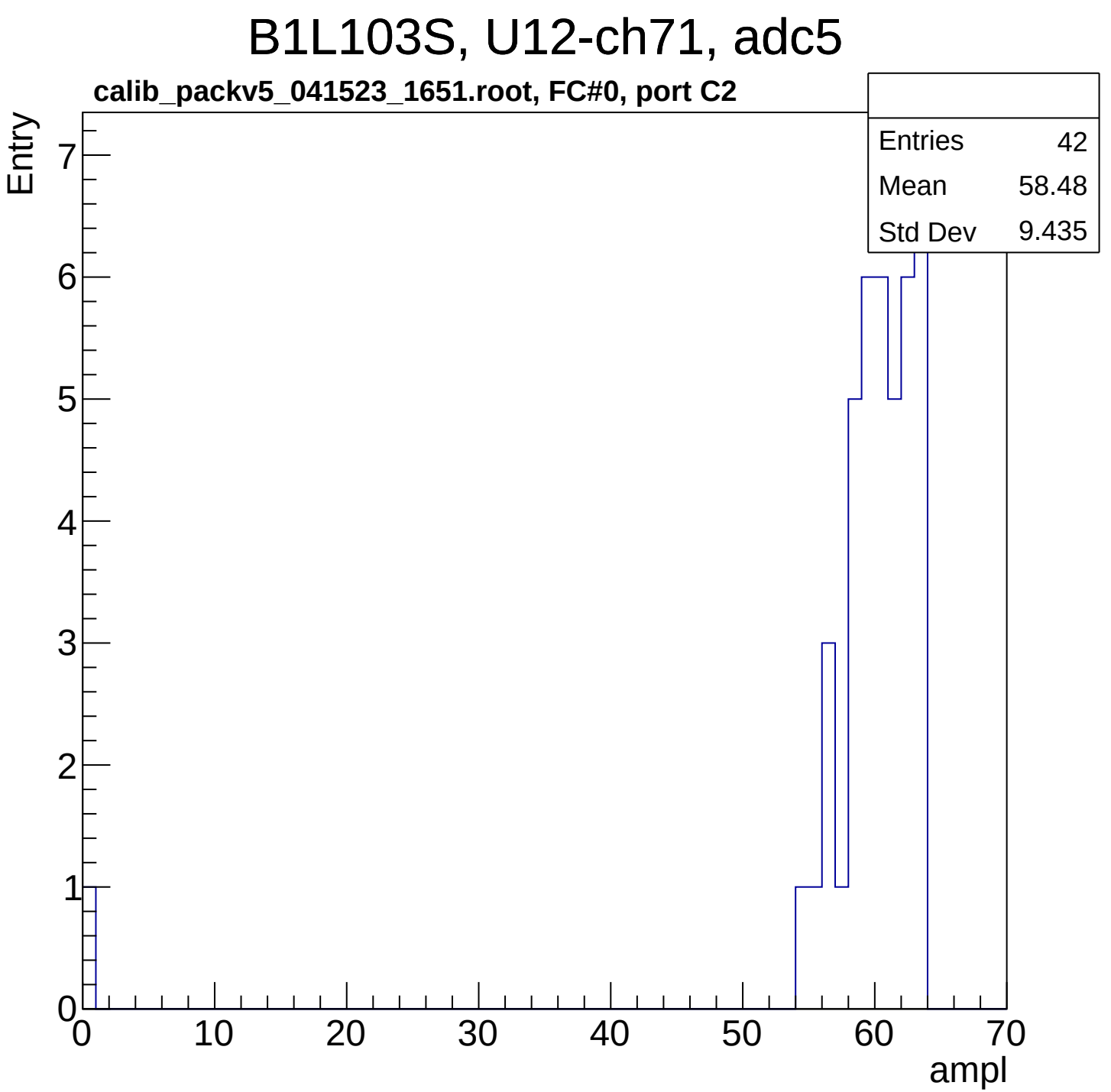
B1L103S, U12-ch71, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 58.48
Std Dev 9.435
Entry
ampl
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1
2
3
4
5
6
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0
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60
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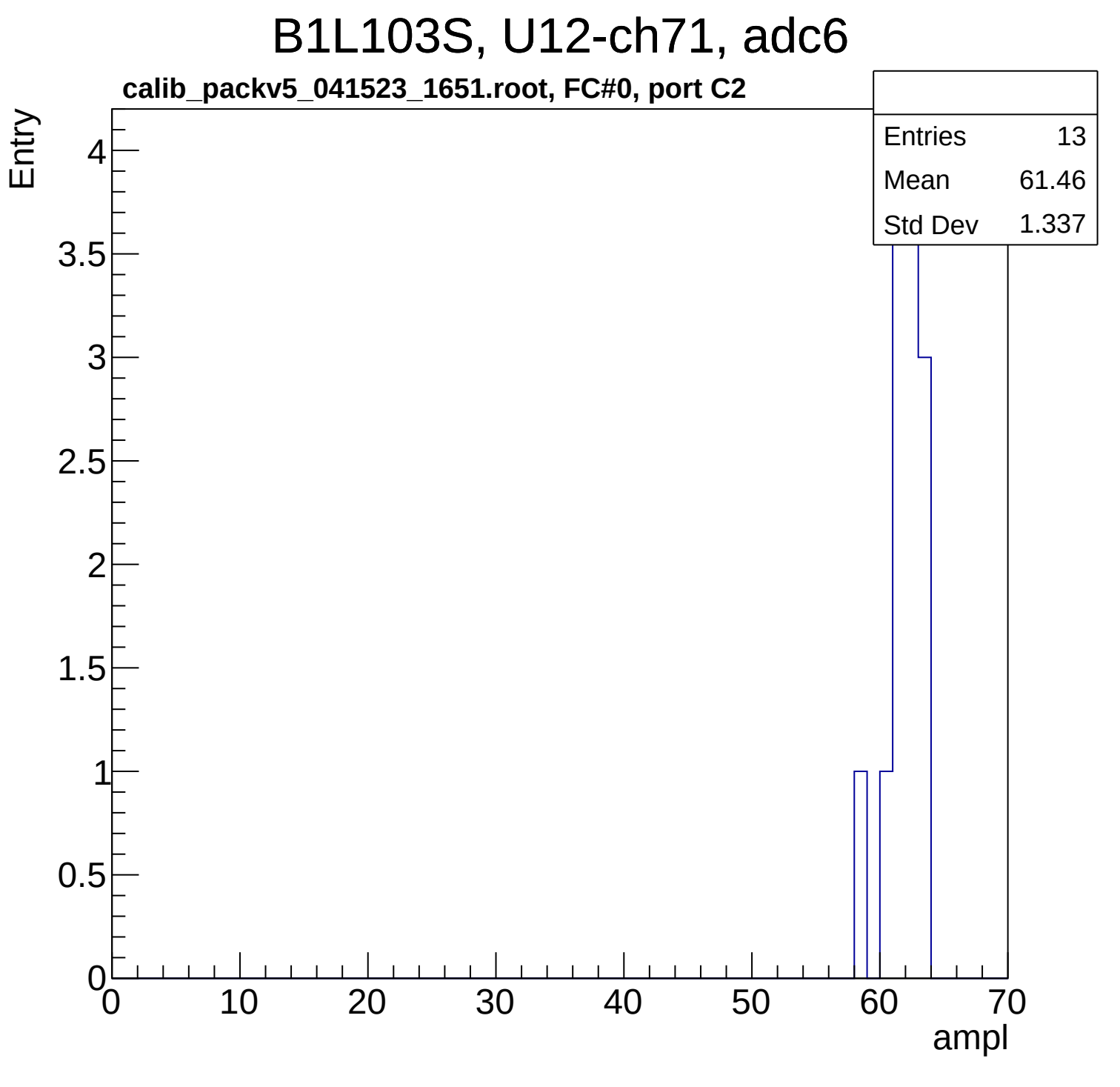
B1L103S, U12-ch71, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.46
Std Dev 1.337
Entry
ampl
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1
1.5
2
2.5
3
3.5
4
0
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60
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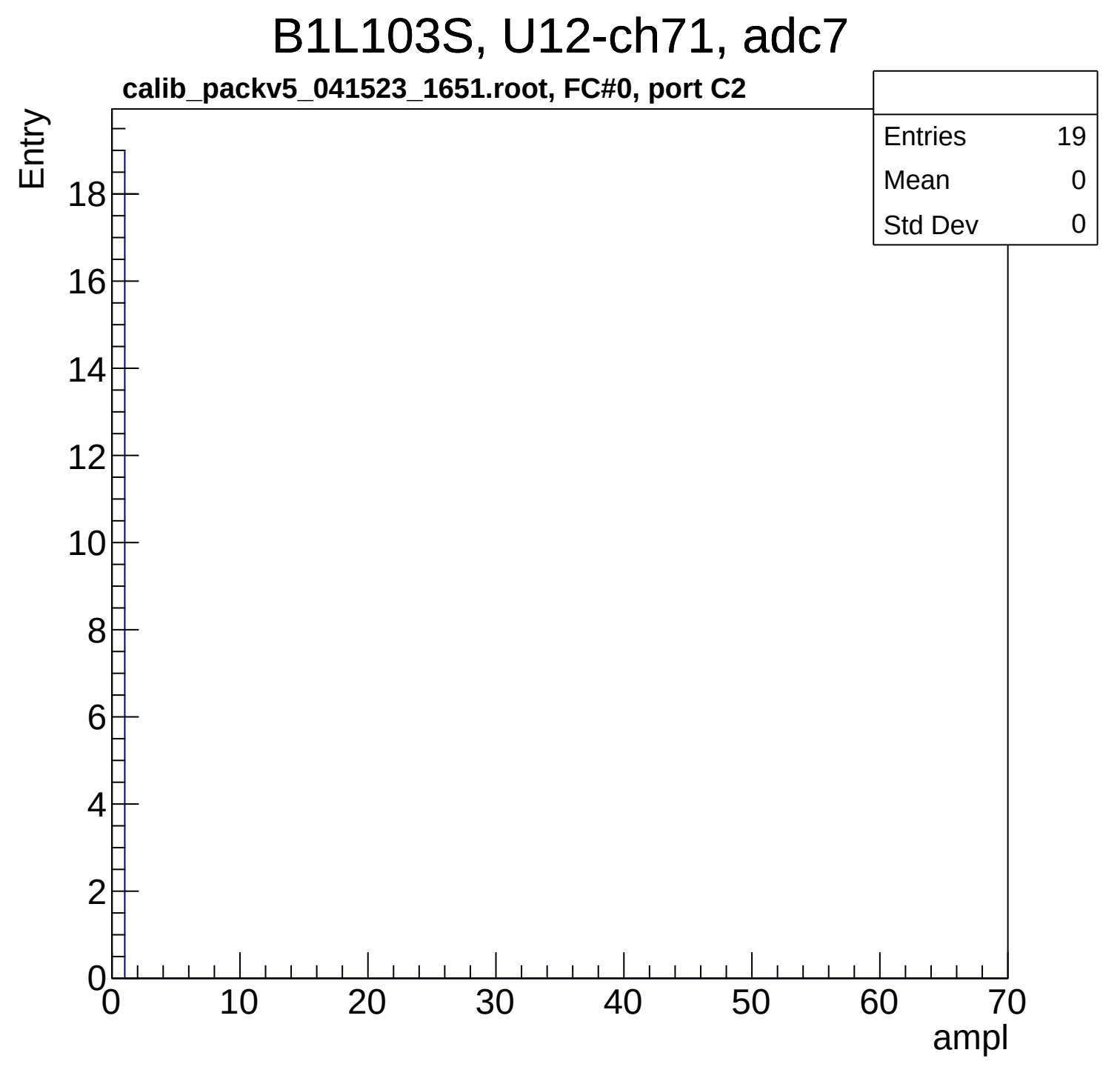
B1L103S, U12-ch71, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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10
20
30
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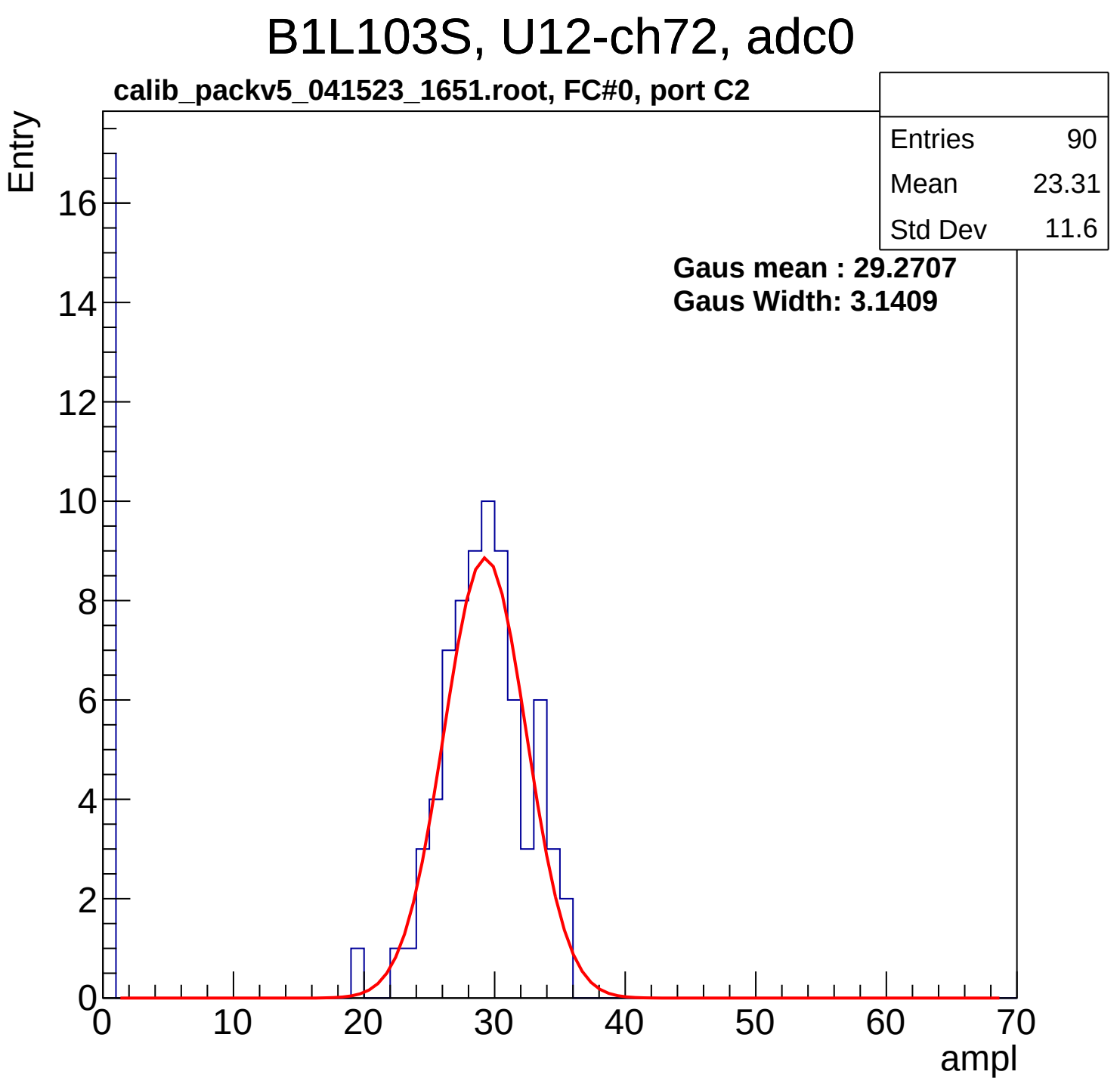
50
60
70
ampl


B1L103S, U12-ch72, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 23.31
Std Dev 11.6
Gaus mean : 29.2707
Gaus Width: 3.1409
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
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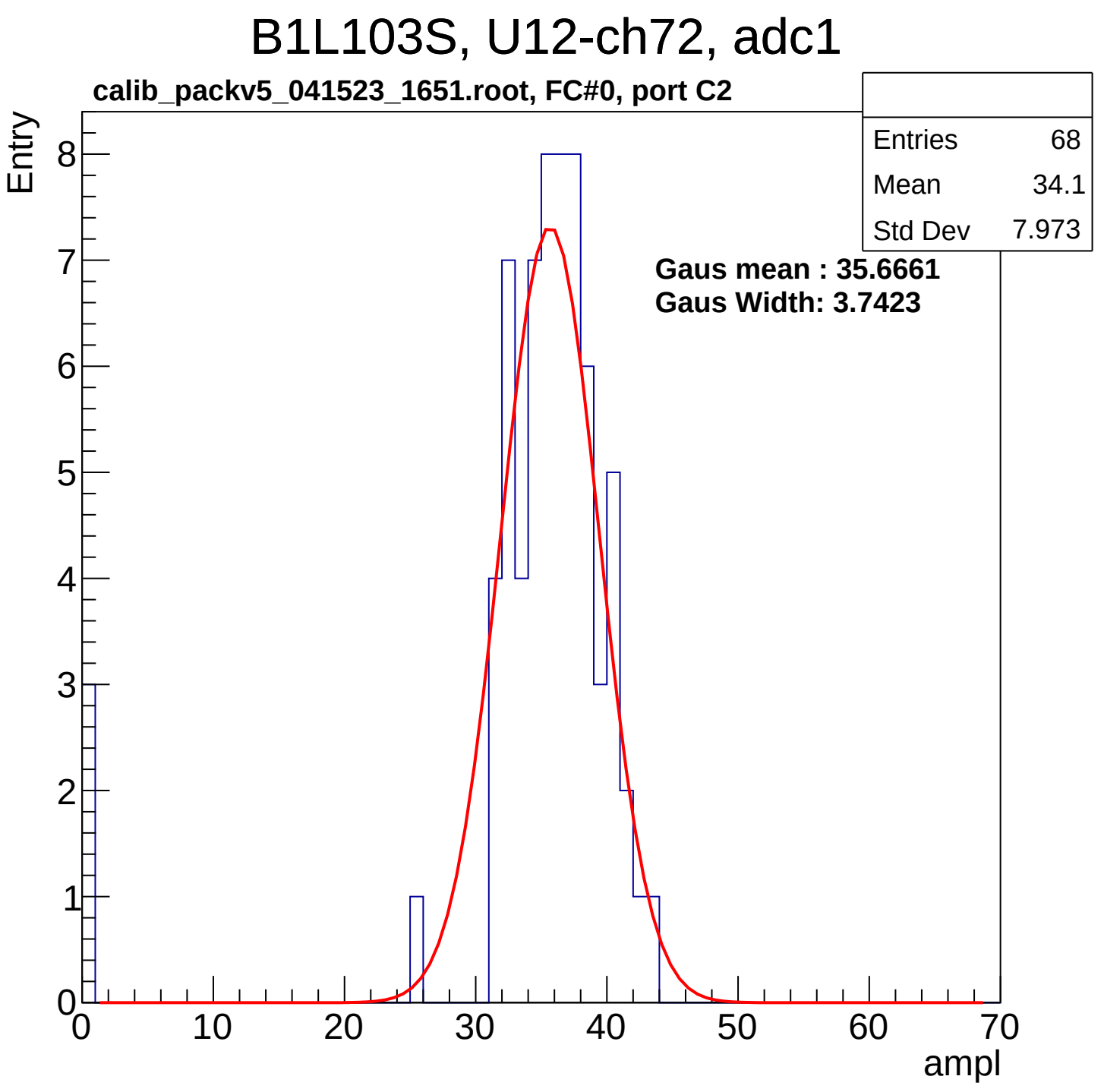
B1L103S, U12-ch72, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 34.1
Std Dev 7.973
Gaus mean : 35.6661
Gaus Width: 3.7423
Entry
ampl
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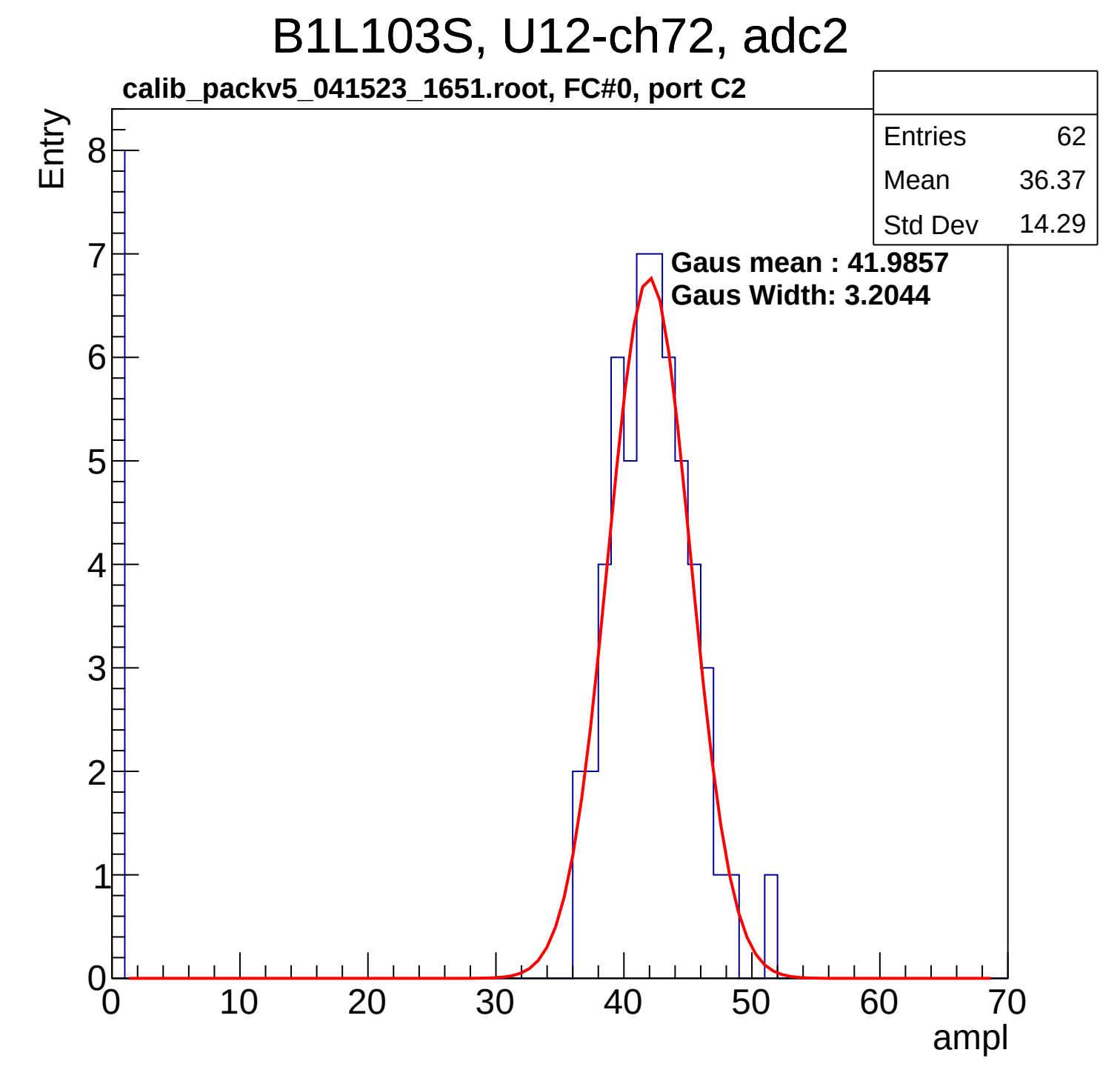
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U12-ch72, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 36.37
Std Dev 14.29
Gaus mean : 41.9857
Gaus Width: 3.2044
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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60
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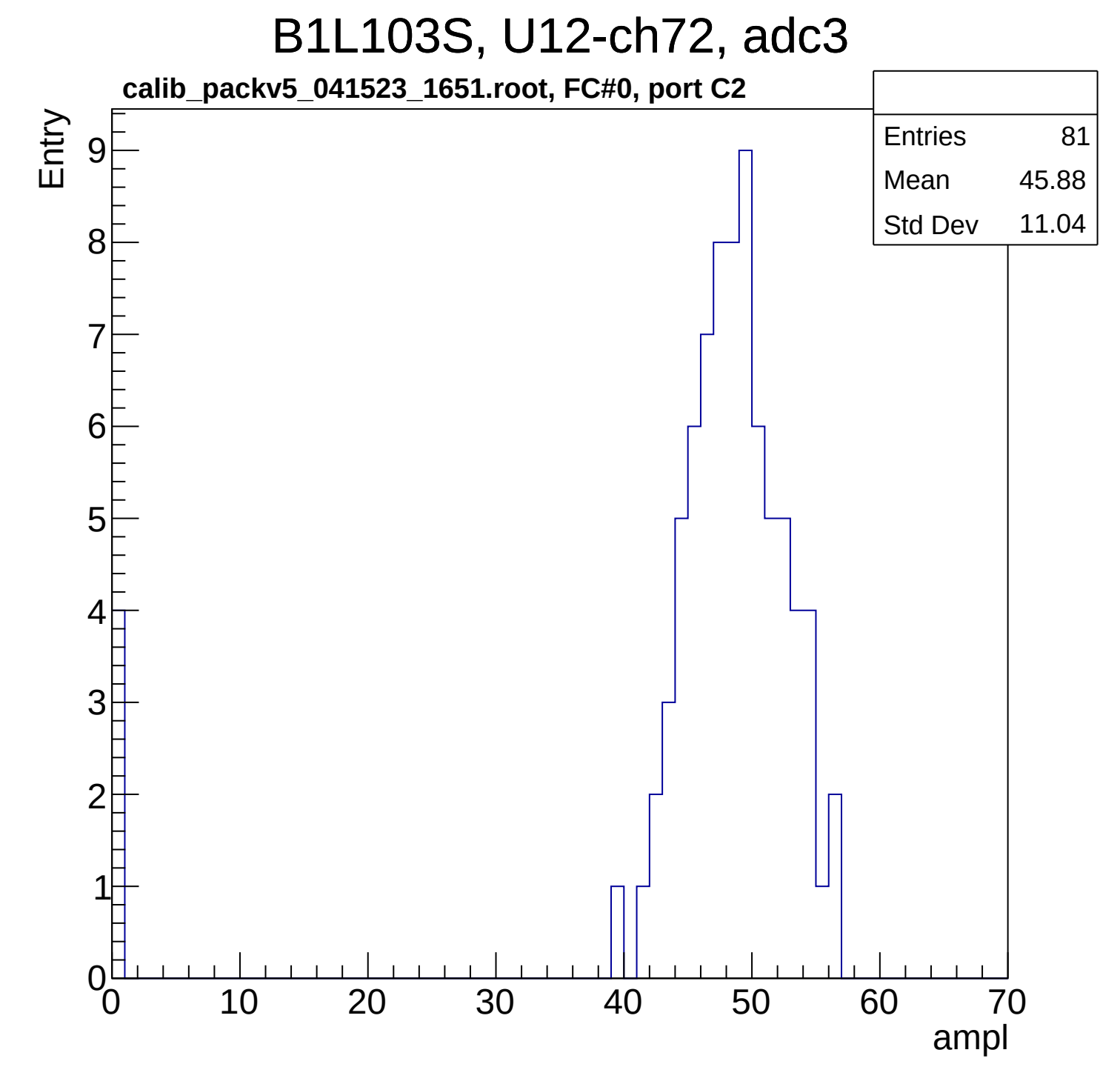
B1L103S, U12-ch72, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 45.88
Std Dev 11.04
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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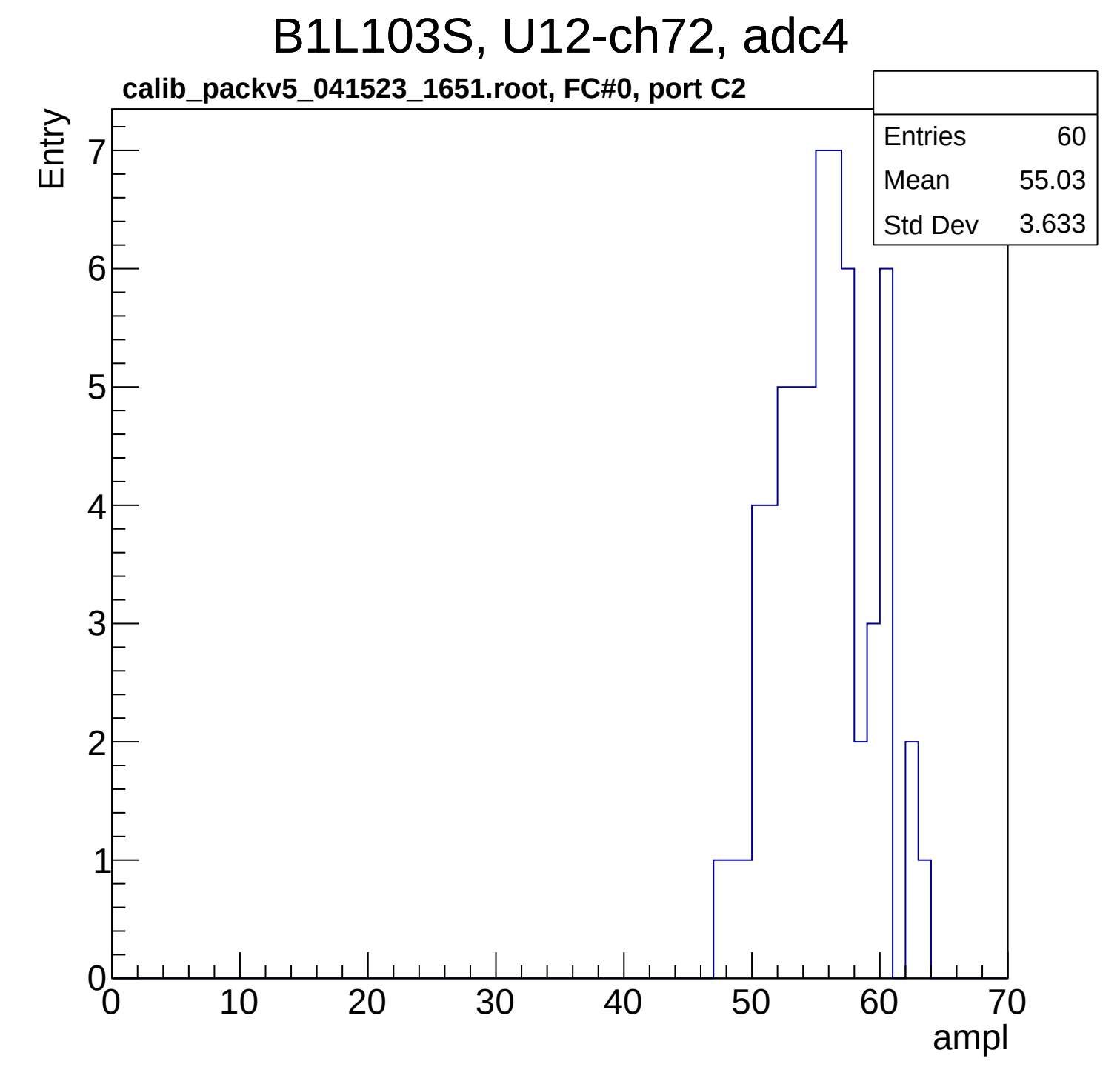
40
50
60
70


B1L103S, U12-ch72, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 55.03
Std Dev 3.633
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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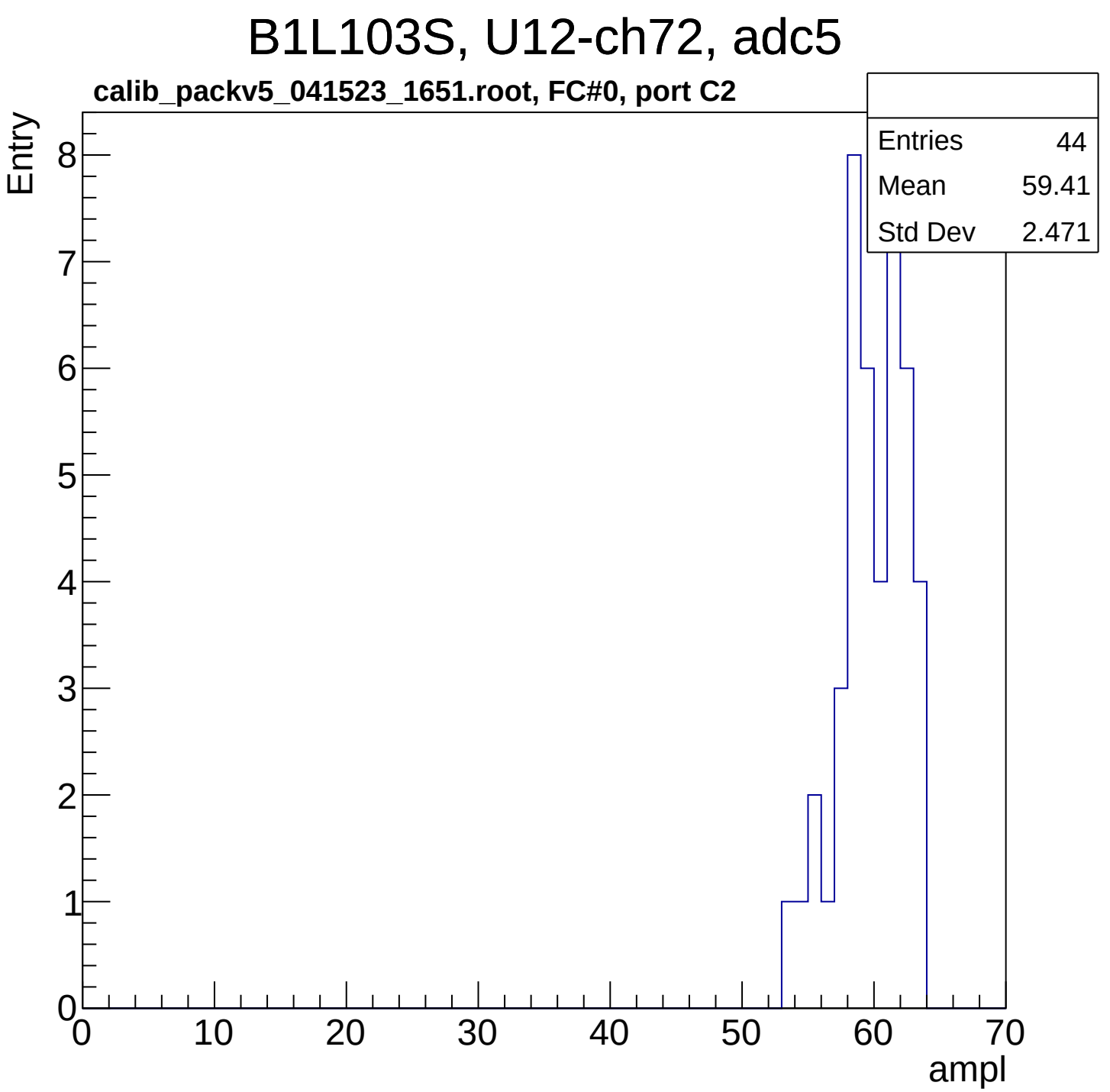
B1L103S, U12-ch72, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 59.41
Std Dev 2.471
Entry
ampl
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2
3
4
5
6
7
8
0
10
20
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40
50
60
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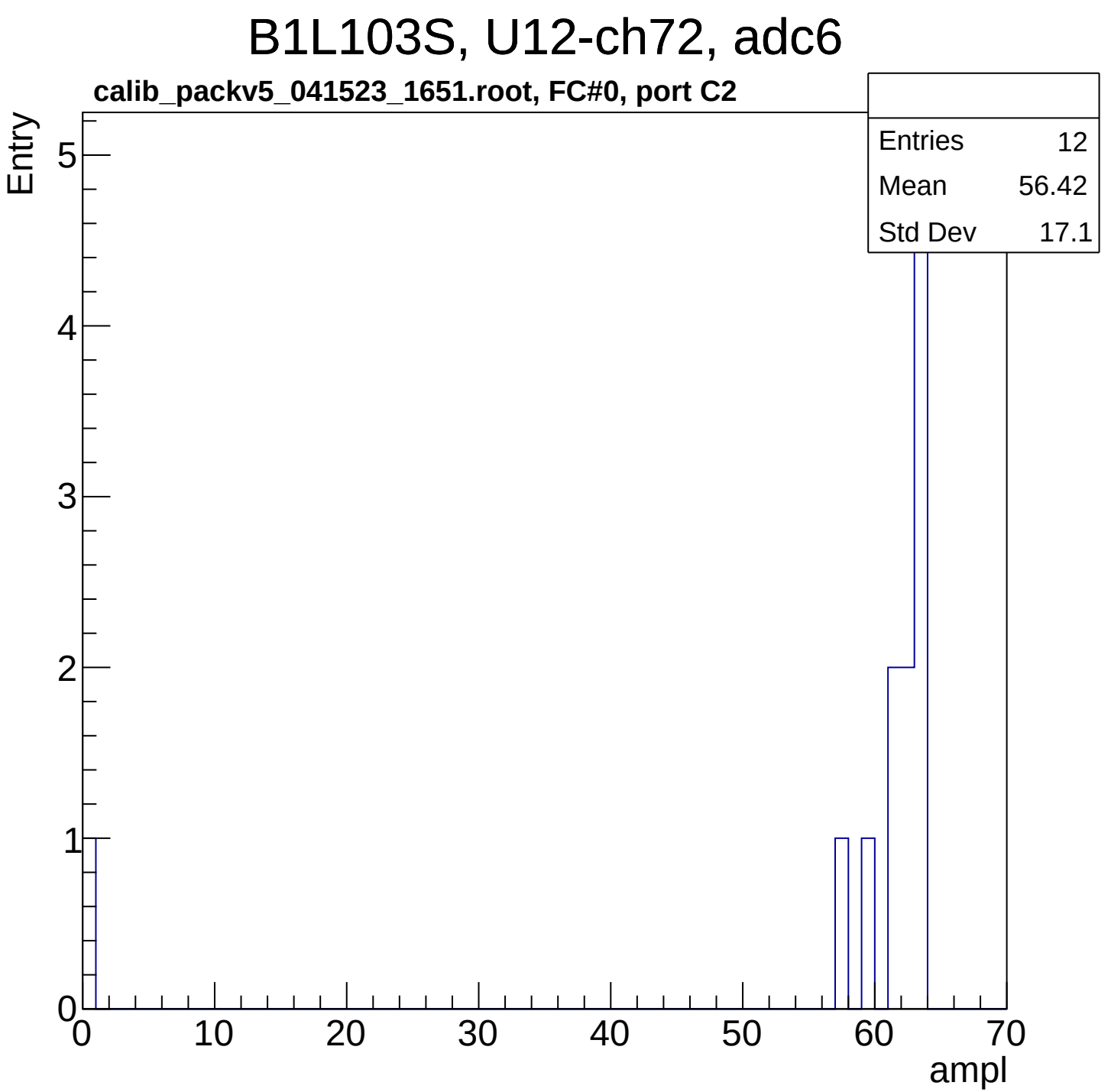
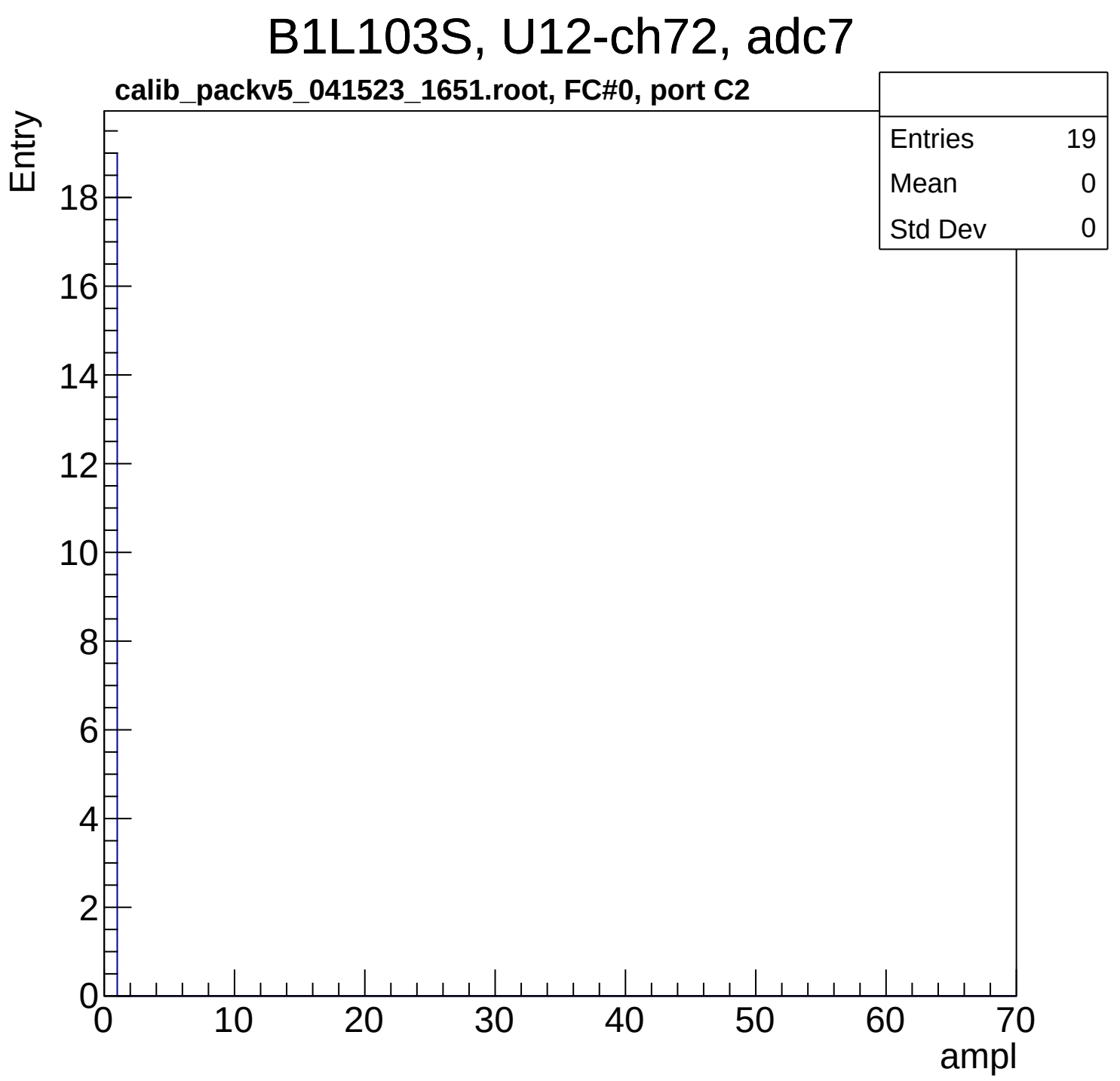

B1L103S, U12-ch72, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 56.42
Std Dev 17.1
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch72, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
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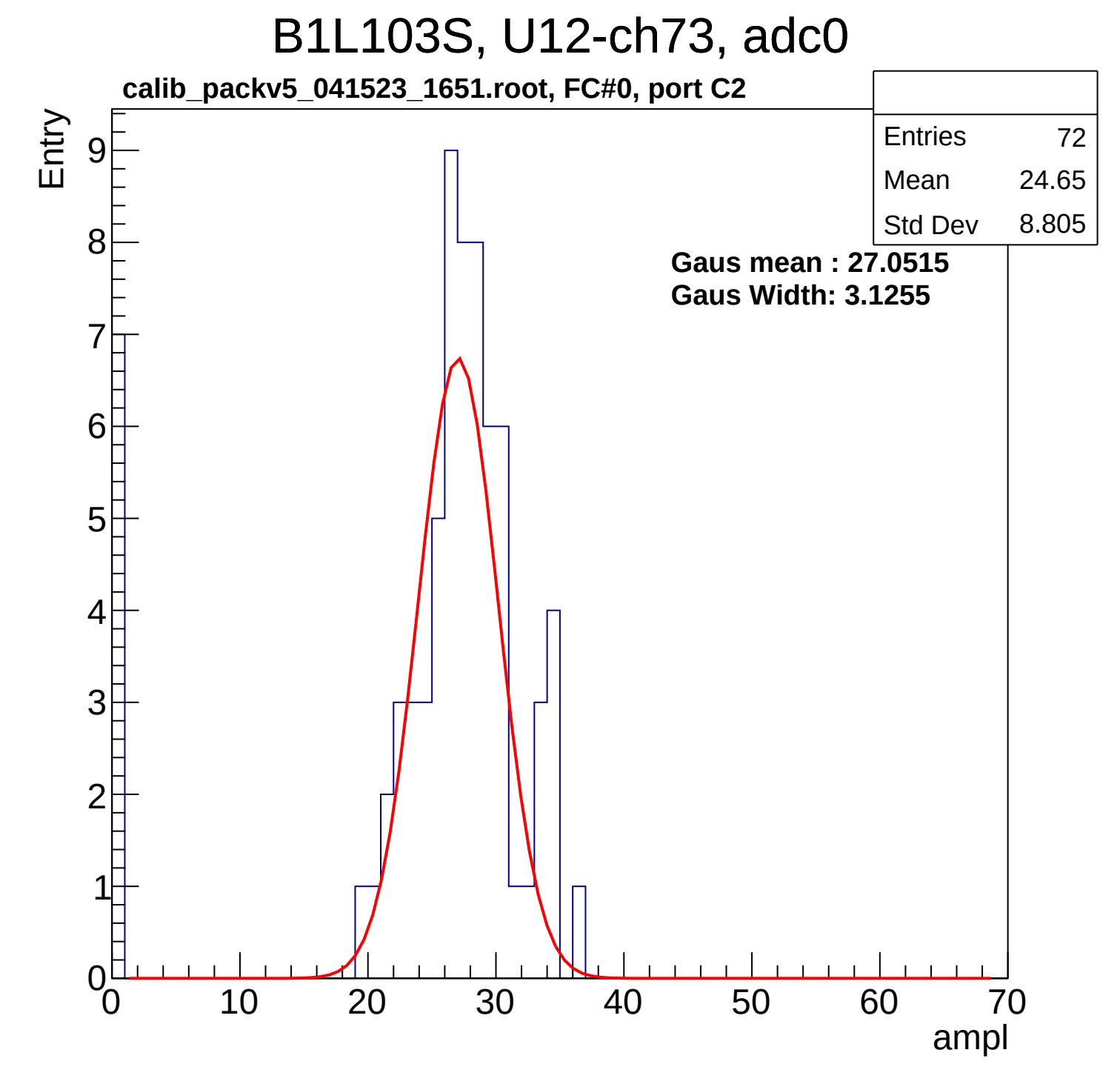
50
60
70
ampl


B1L103S, U12-ch73, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 24.65
Std Dev 8.805
Gaus mean : 27.0515
Gaus Width: 3.1255
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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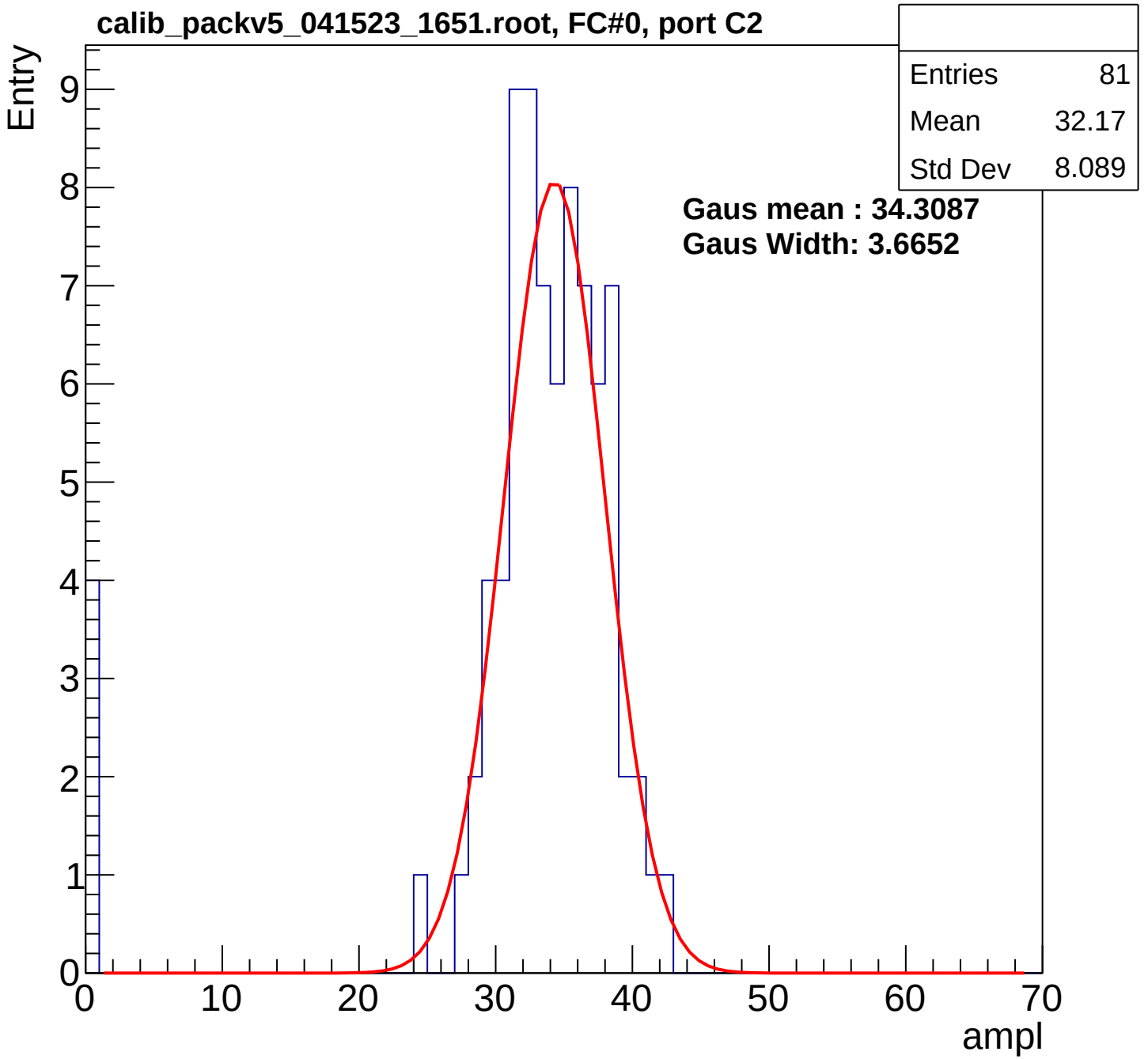
B1L103S, U12-ch73, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 32.17
Std Dev 8.089
Gaus mean : 34.3087
Gaus Width: 3.6652
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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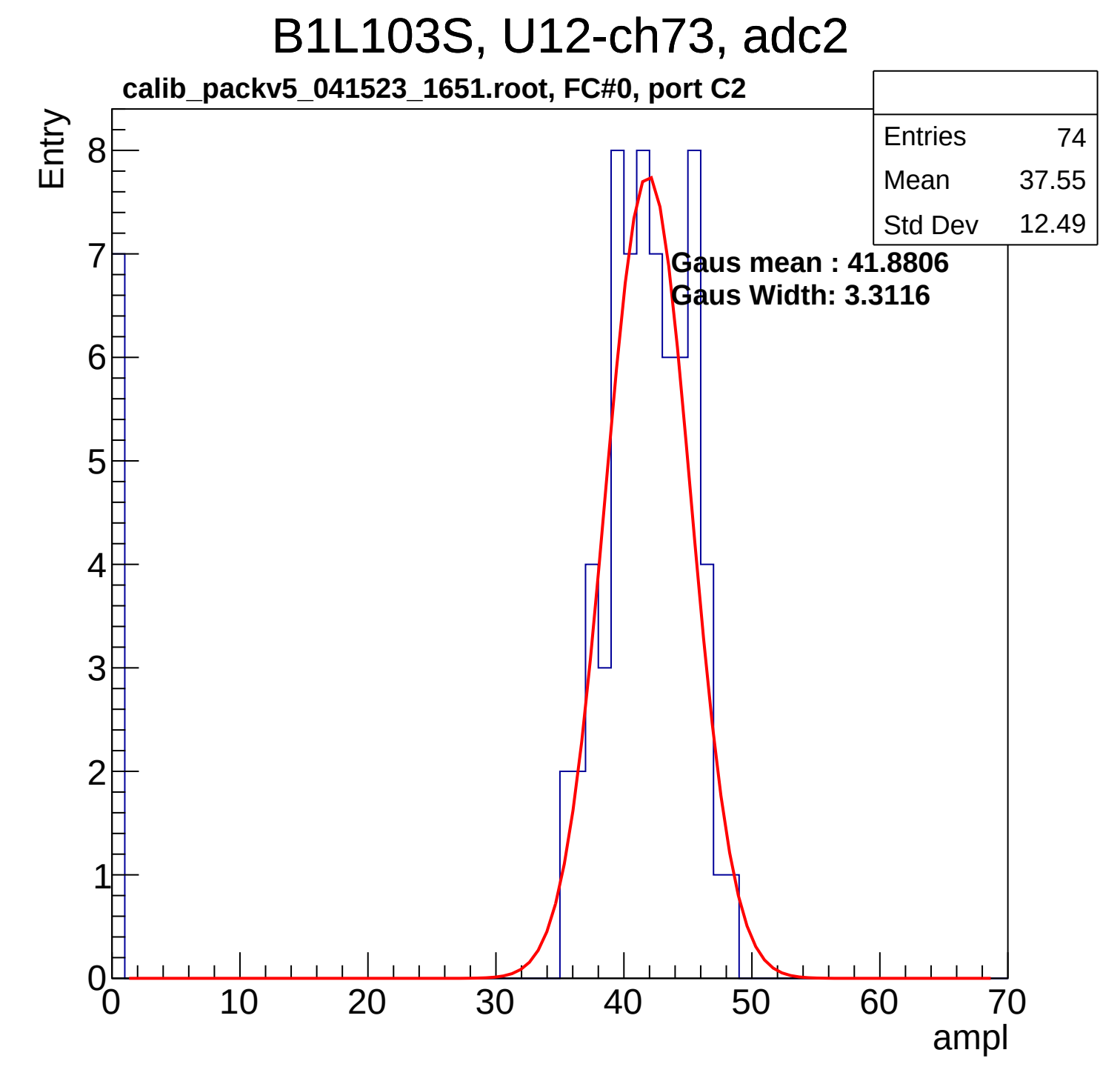
B1L103S, U12-ch73, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 37.55
Std Dev 12.49
Gaus mean : 41.8806
Gaus Width: 3.3116
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
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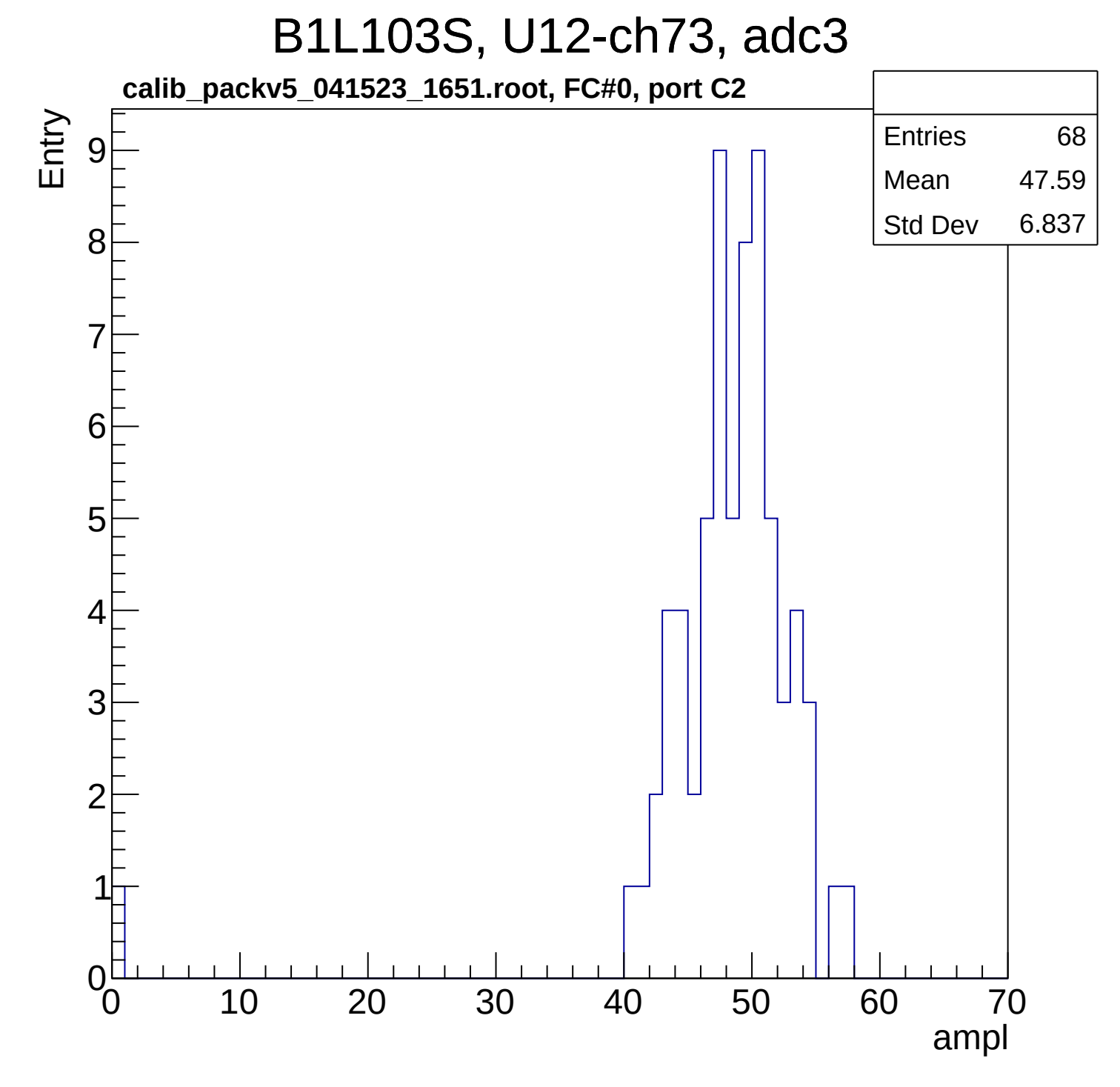
40
50
60
70


B1L103S, U12-ch73, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 47.59
Std Dev 6.837
Entry
ampl
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2
3
4
5
6
7
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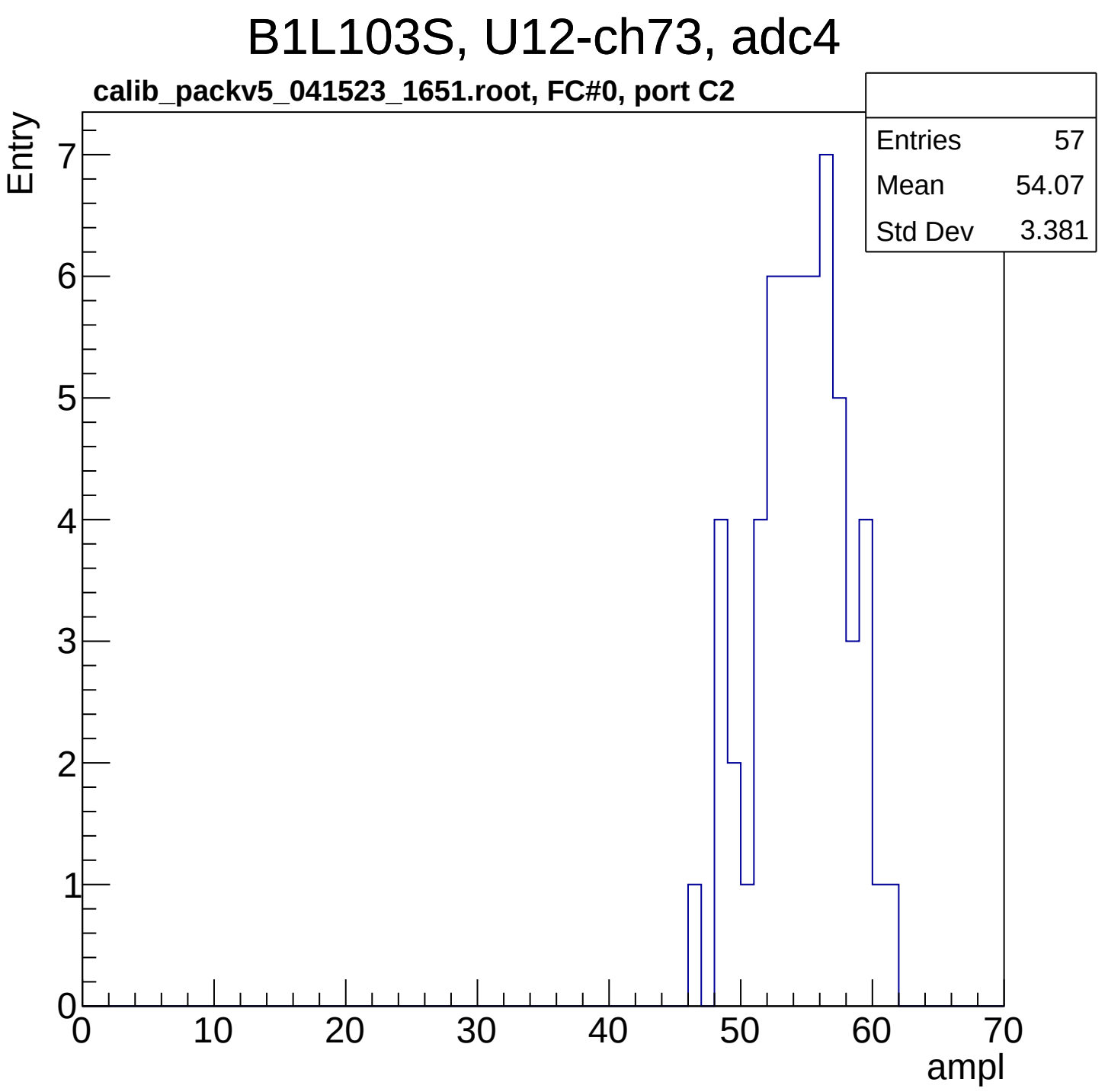
B1L103S, U12-ch73, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 54.07
Std Dev 3.381
Entry
ampl
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1
2
3
4
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6
7
0
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20
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40
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60
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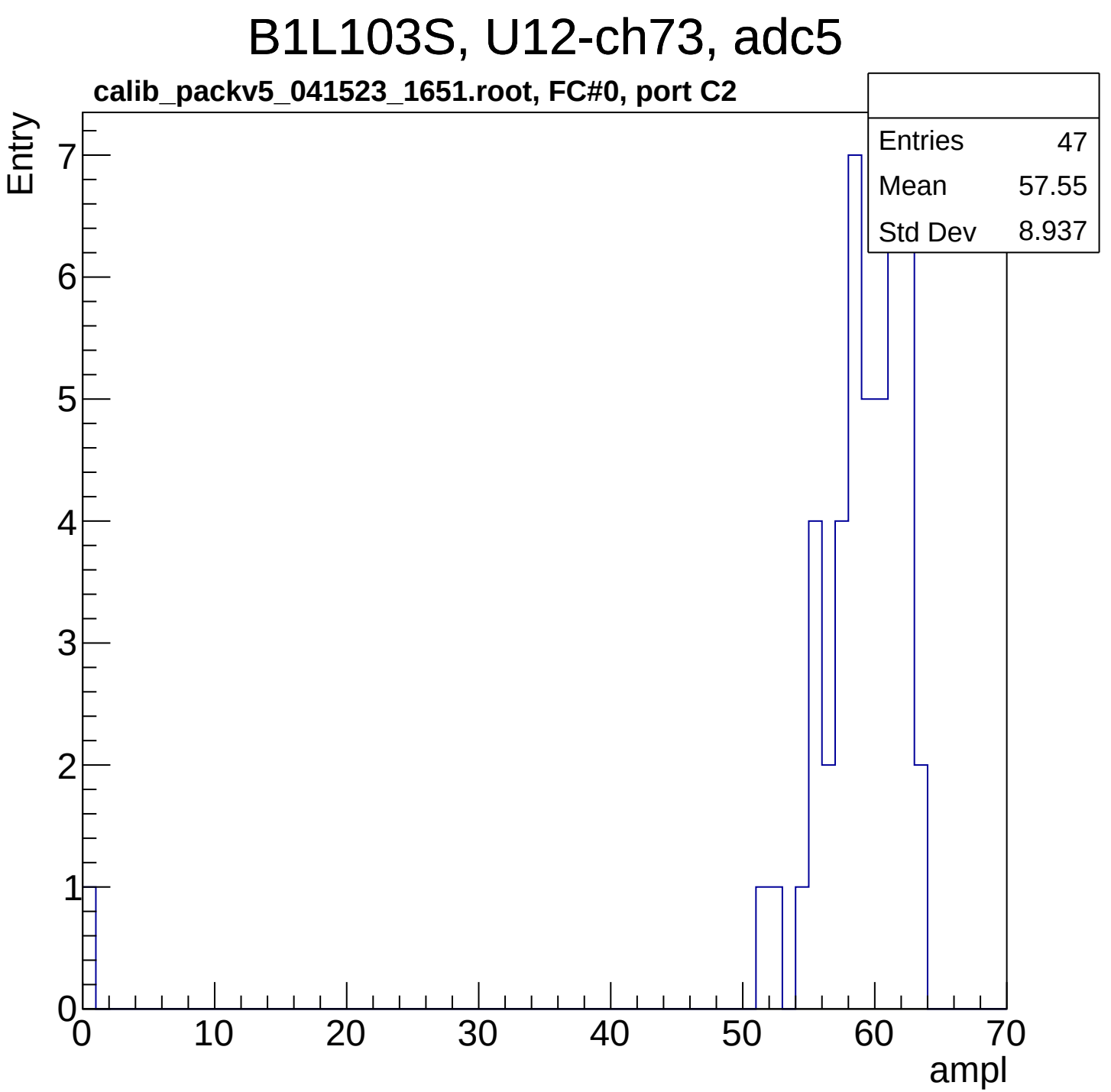
B1L103S, U12-ch73, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 57.55
Std Dev 8.937
Entry
ampl
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1
2
3
4
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6
7
0
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20
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40
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60
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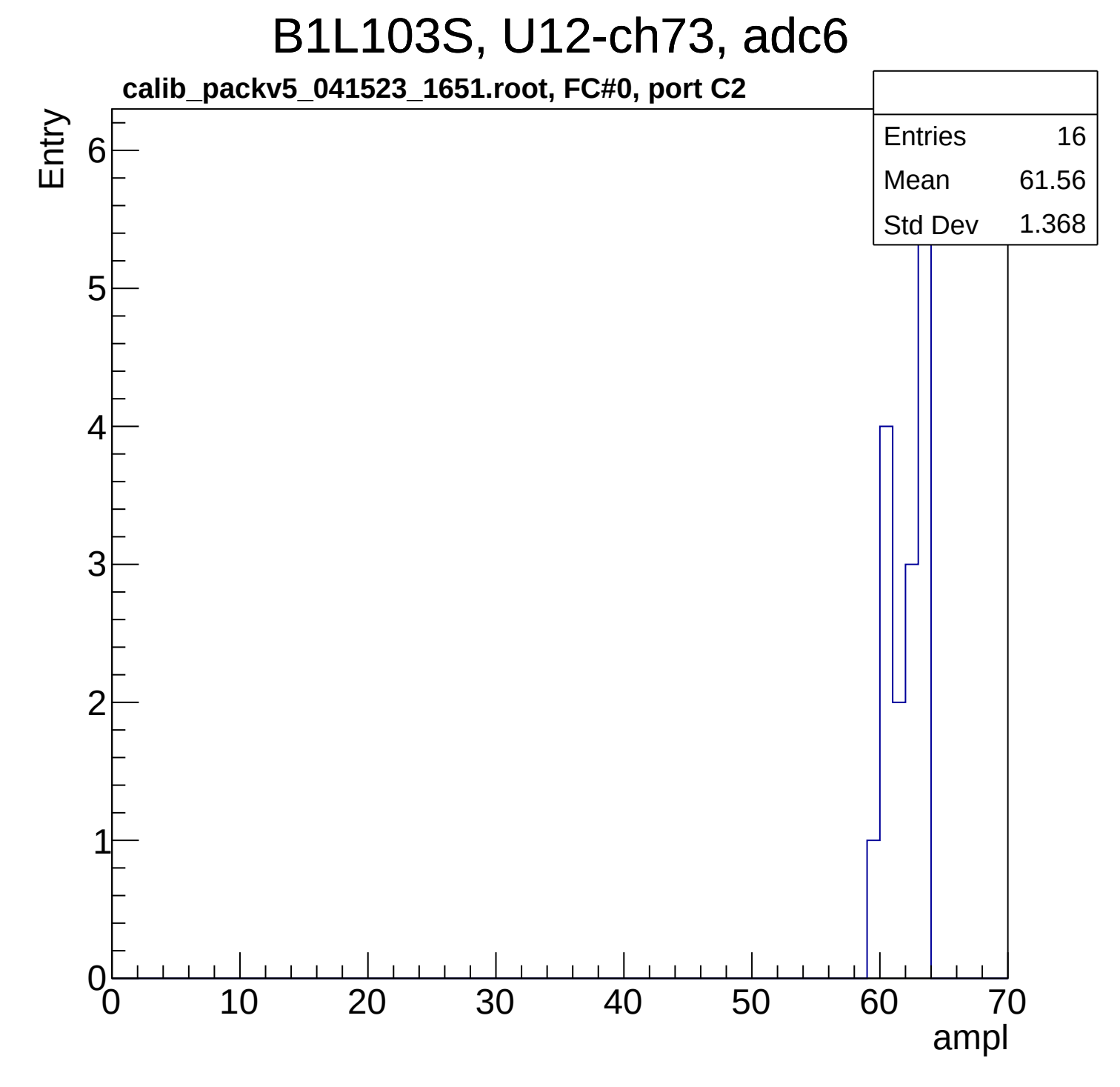
B1L103S, U12-ch73, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 61.56
Std Dev 1.368
Entry
ampl
0
1
2
3
4
5
6
0
10
20
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40
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60
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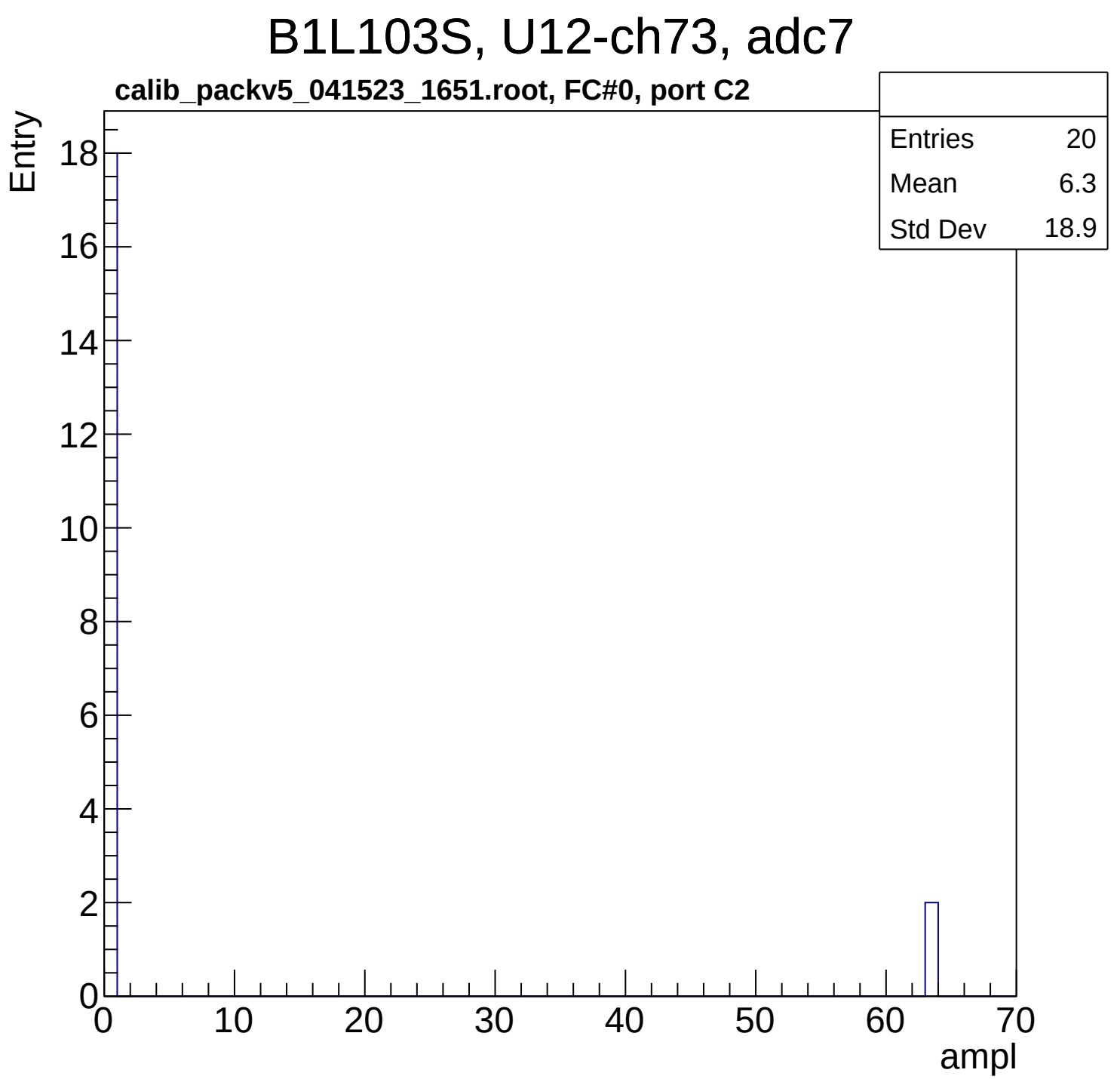
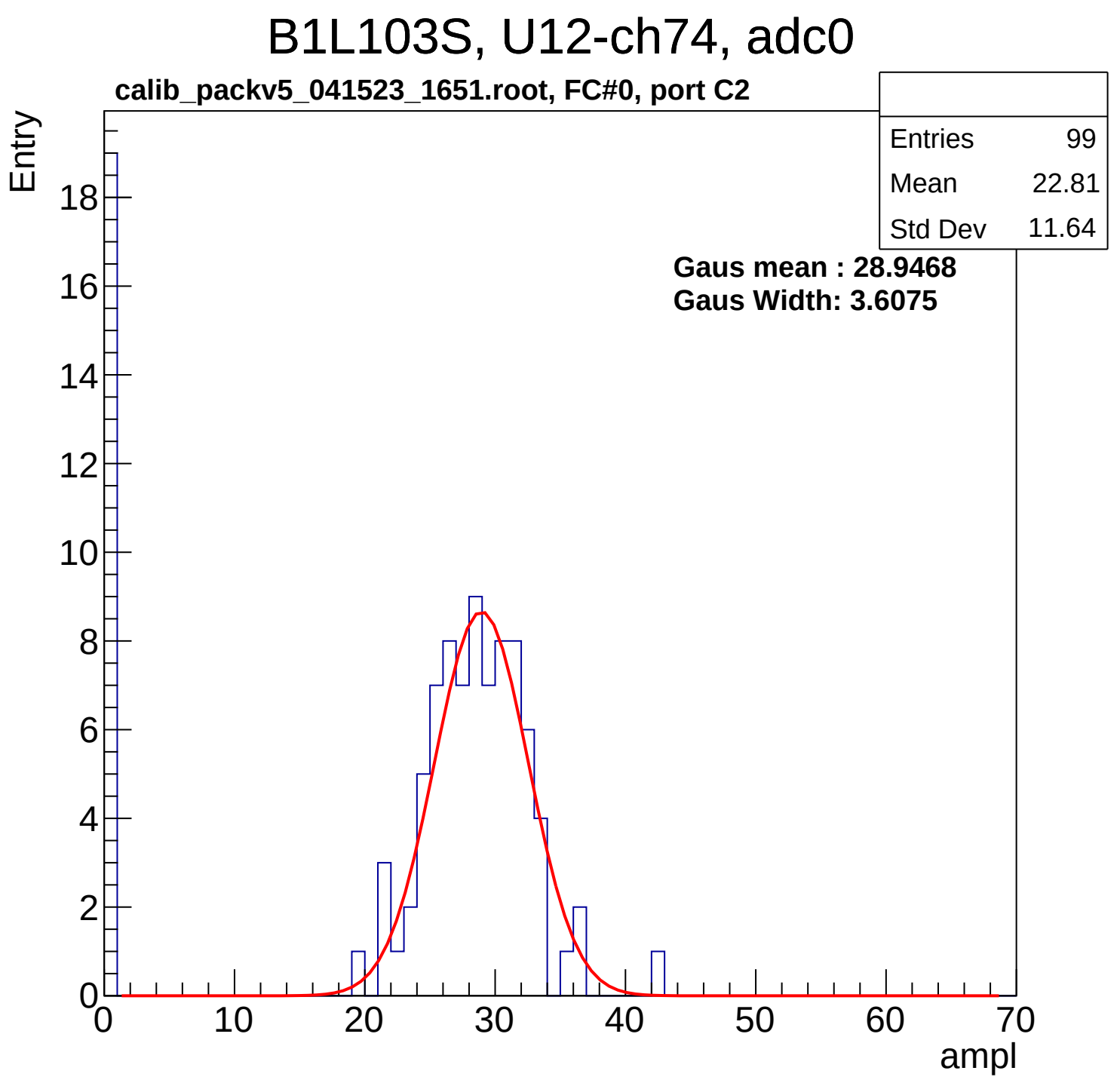

B1L103S, U12-ch73, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.3
Std Dev 18.9
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch74, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 22.81
Std Dev 11.64
Gaus mean : 28.9468
Gaus Width: 3.6075
Entry
ampl
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2
4
6
8
10
12
14
16
18
0
10
20
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40
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60
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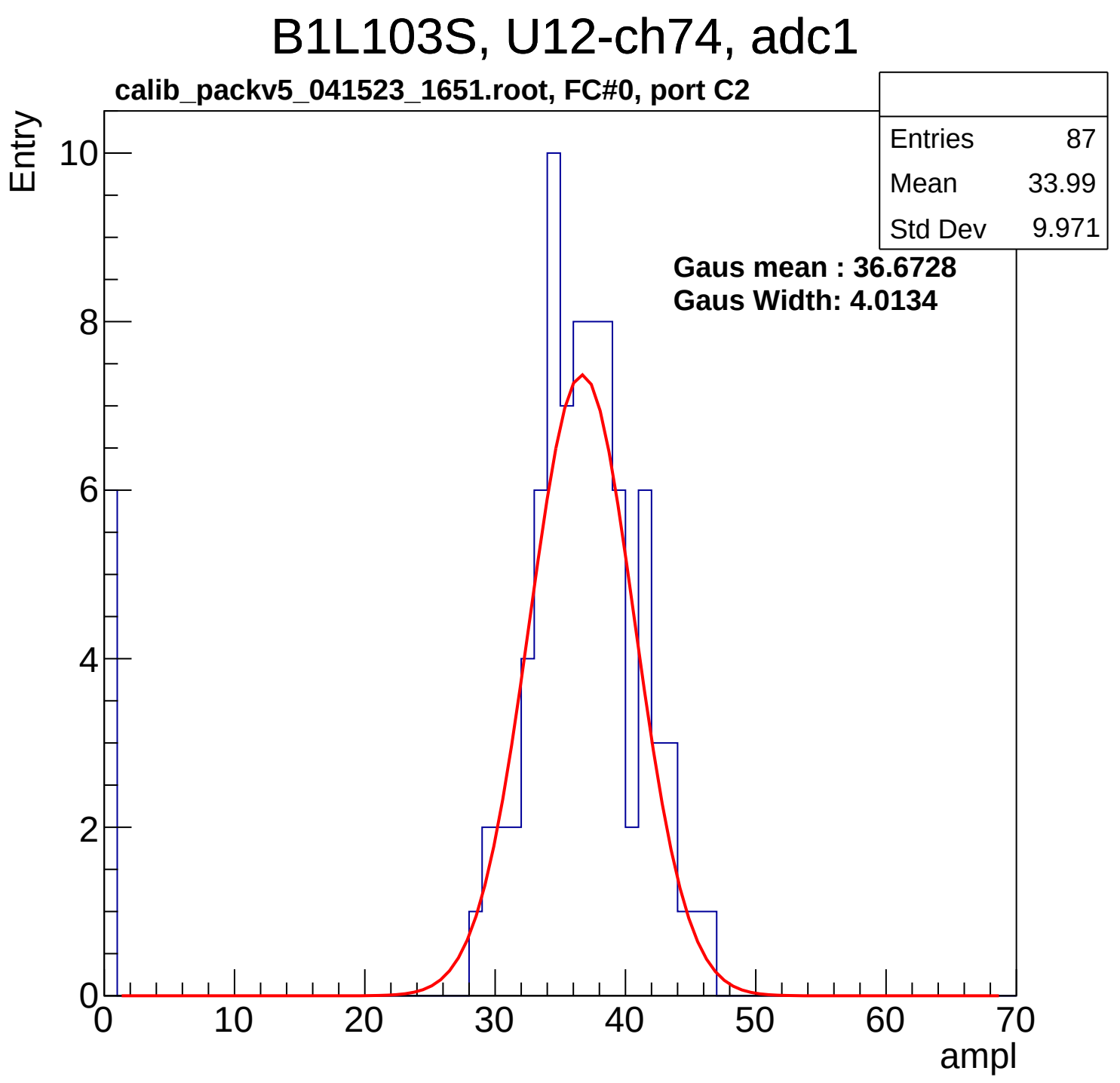
B1L103S, U12-ch74, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 33.99
Std Dev 9.971
Gaus mean : 36.6728
Gaus Width: 4.0134
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
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60
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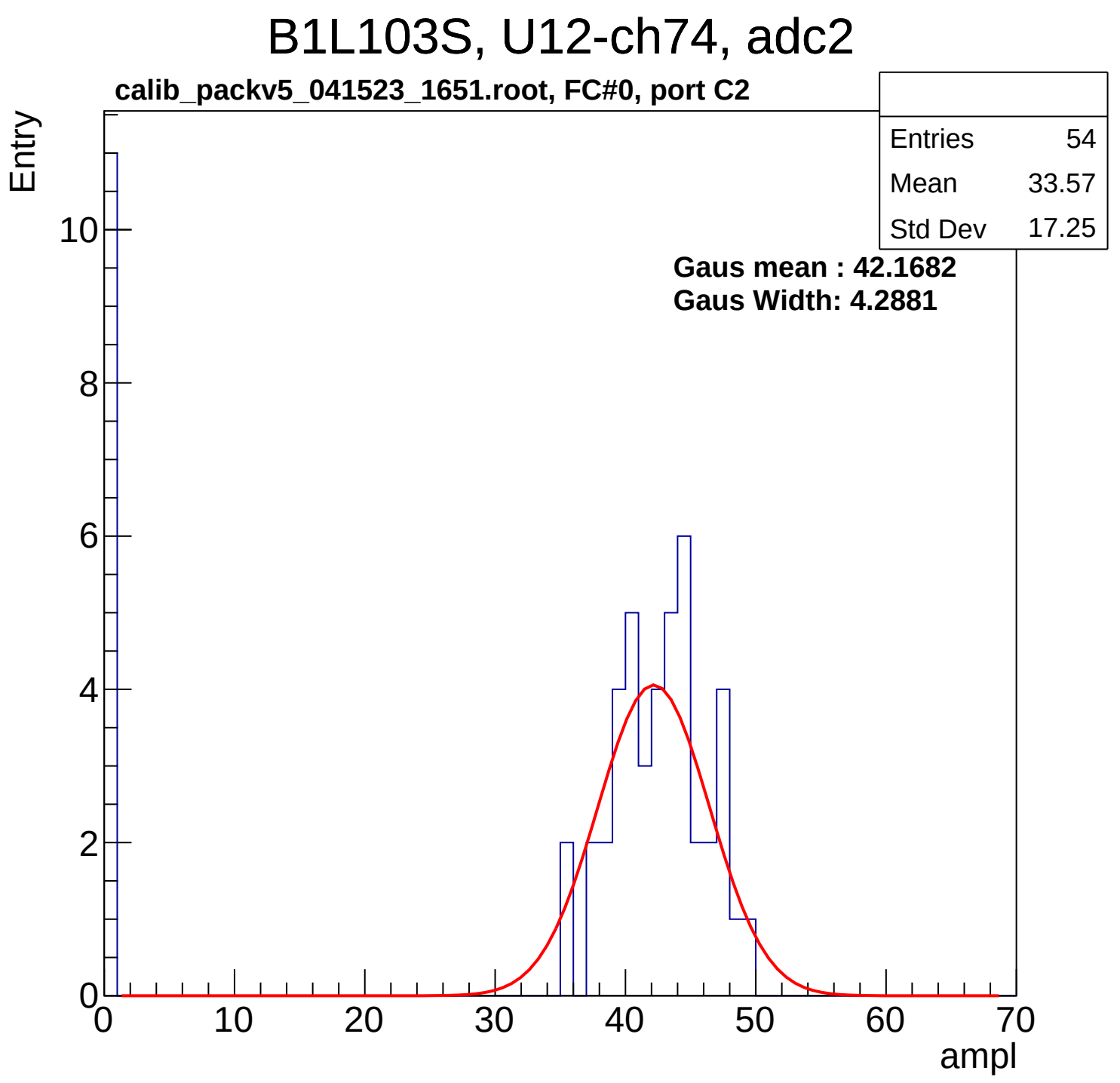
B1L103S, U12-ch74, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 33.57
Std Dev 17.25
Gaus mean : 42.1682
Gaus Width: 4.2881
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
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60
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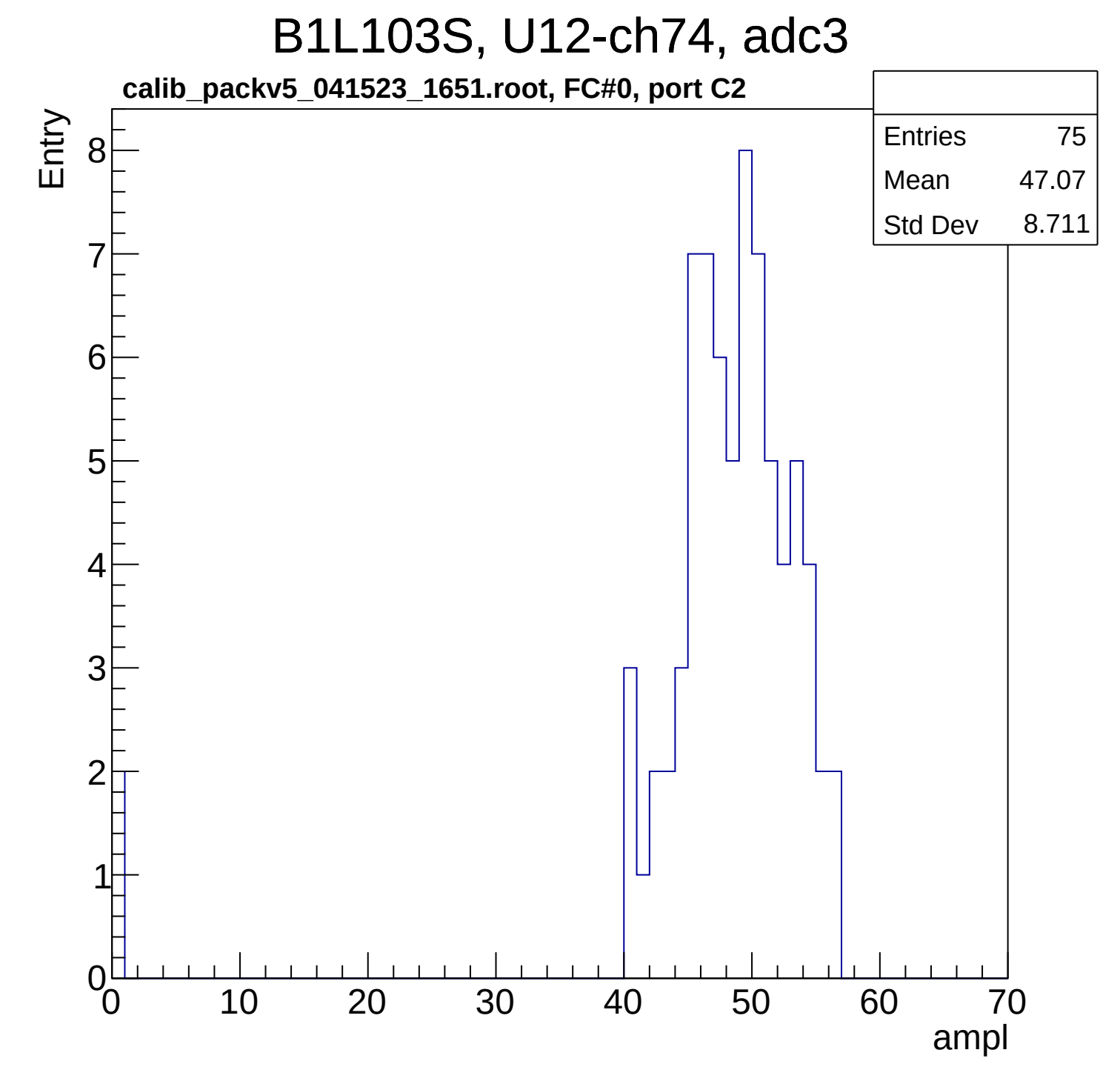
B1L103S, U12-ch74, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 47.07
Std Dev 8.711
Entry
ampl
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1
2
3
4
5
6
7
8
0
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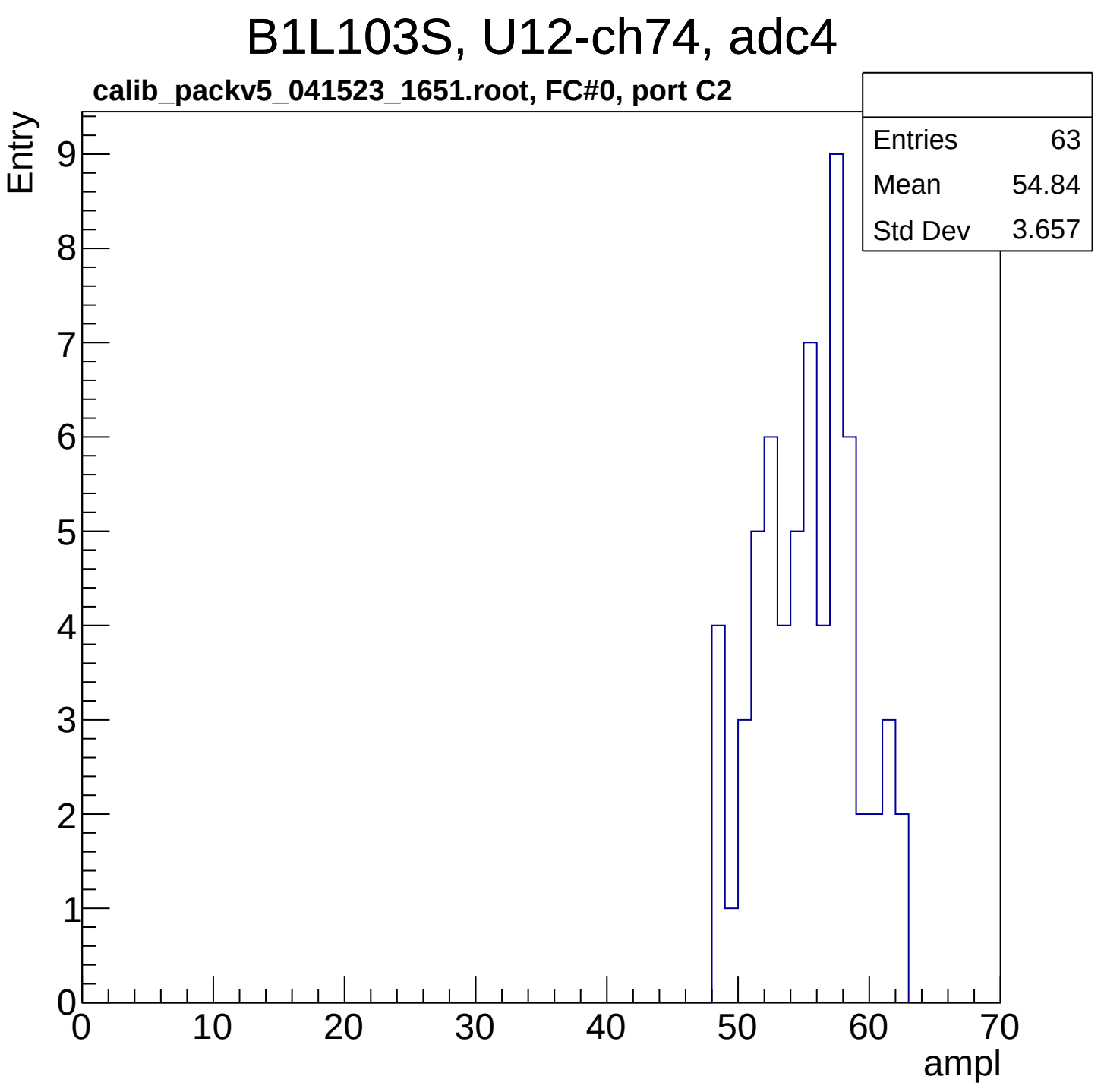
B1L103S, U12-ch74, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 54.84
Std Dev 3.657
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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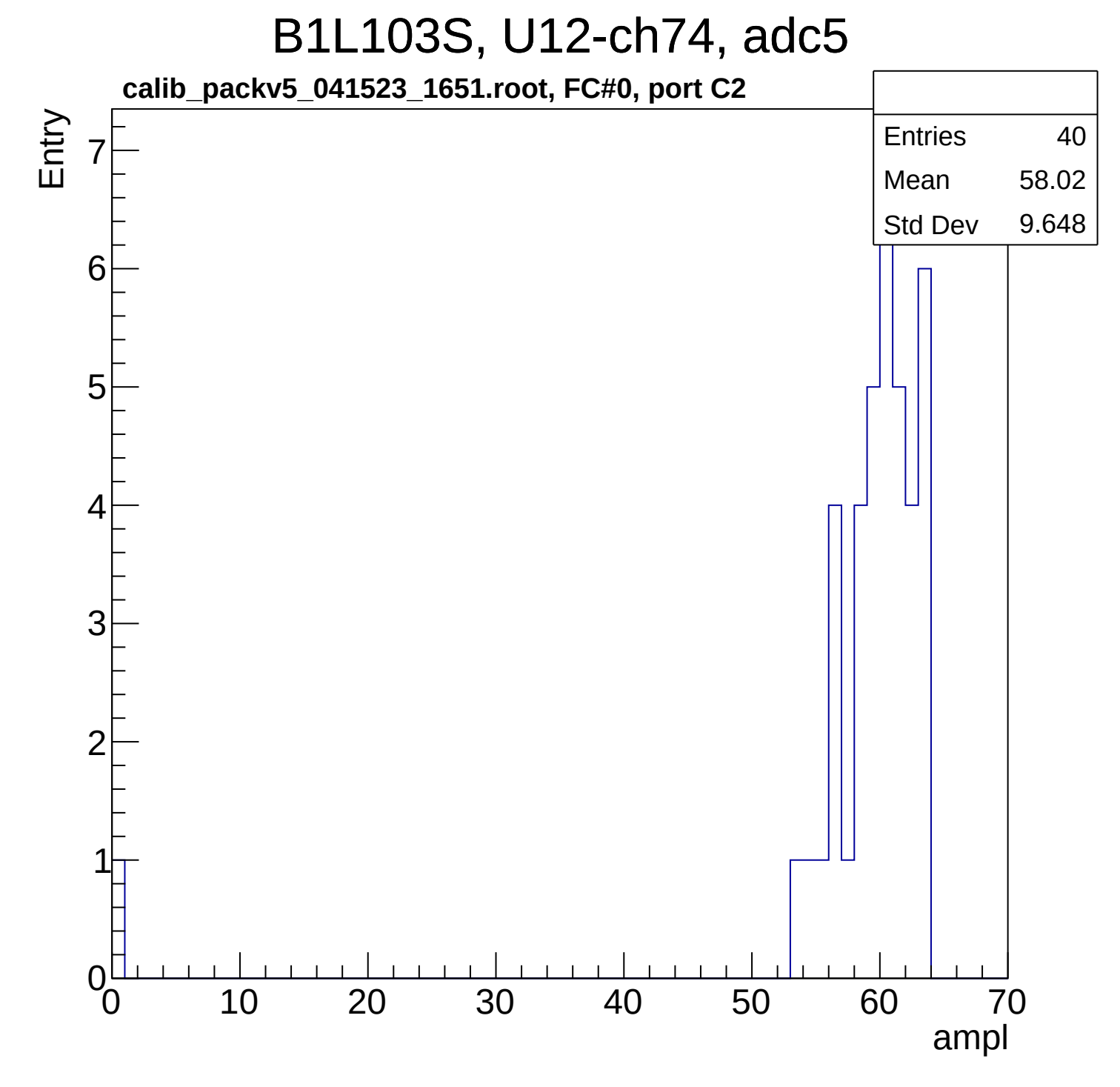
B1L103S, U12-ch74, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 58.02
Std Dev 9.648
Entry
ampl
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1
2
3
4
5
6
7
0
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60
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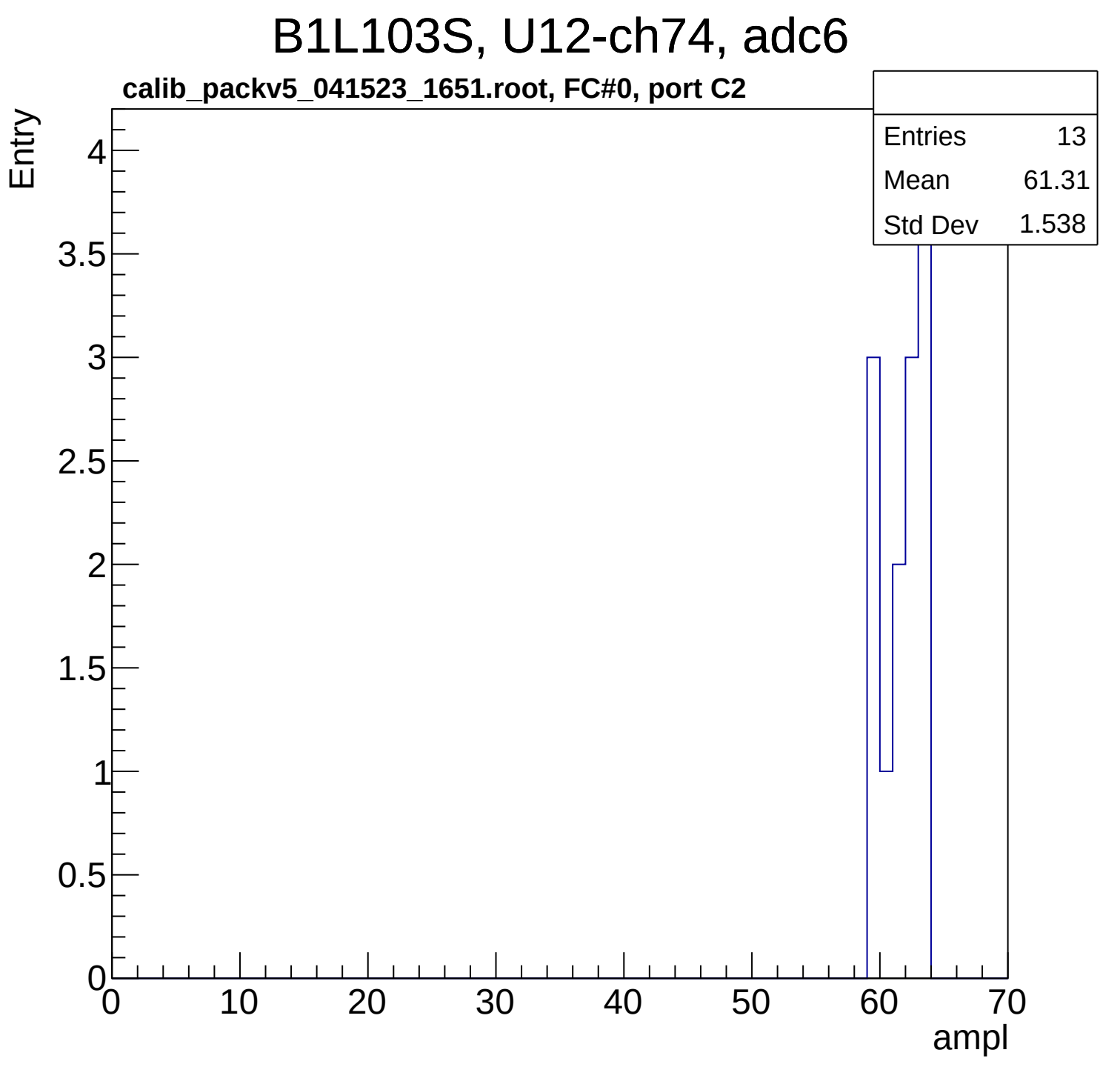
B1L103S, U12-ch74, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.31
Std Dev 1.538
Entry
ampl
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1
1.5
2
2.5
3
3.5
4
0
10
20
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40
50
60
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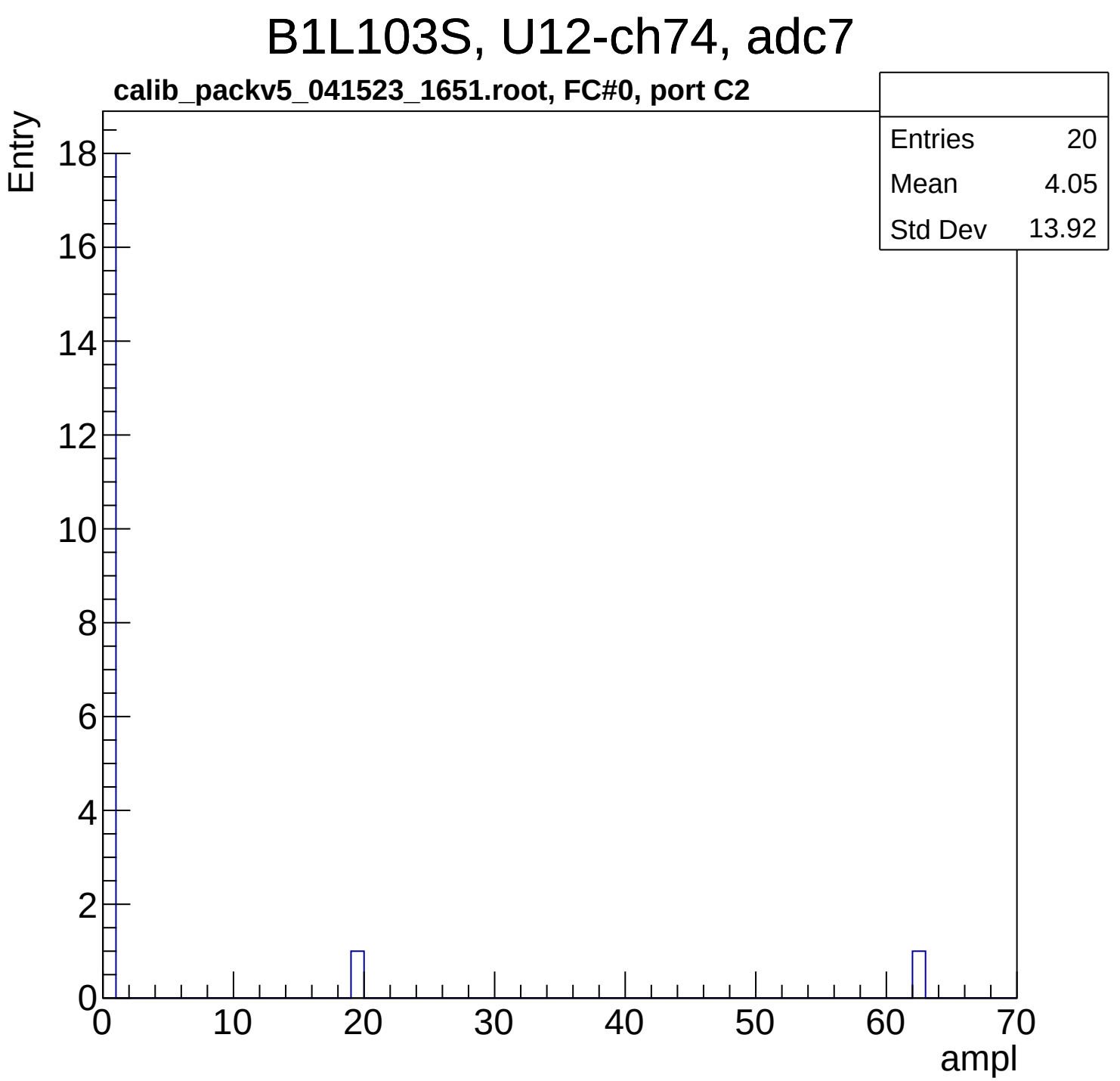
B1L103S, U12-ch74, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.05
Std Dev 13.92
Entry
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6
8
10
12
14
16
18
0
10
20
30
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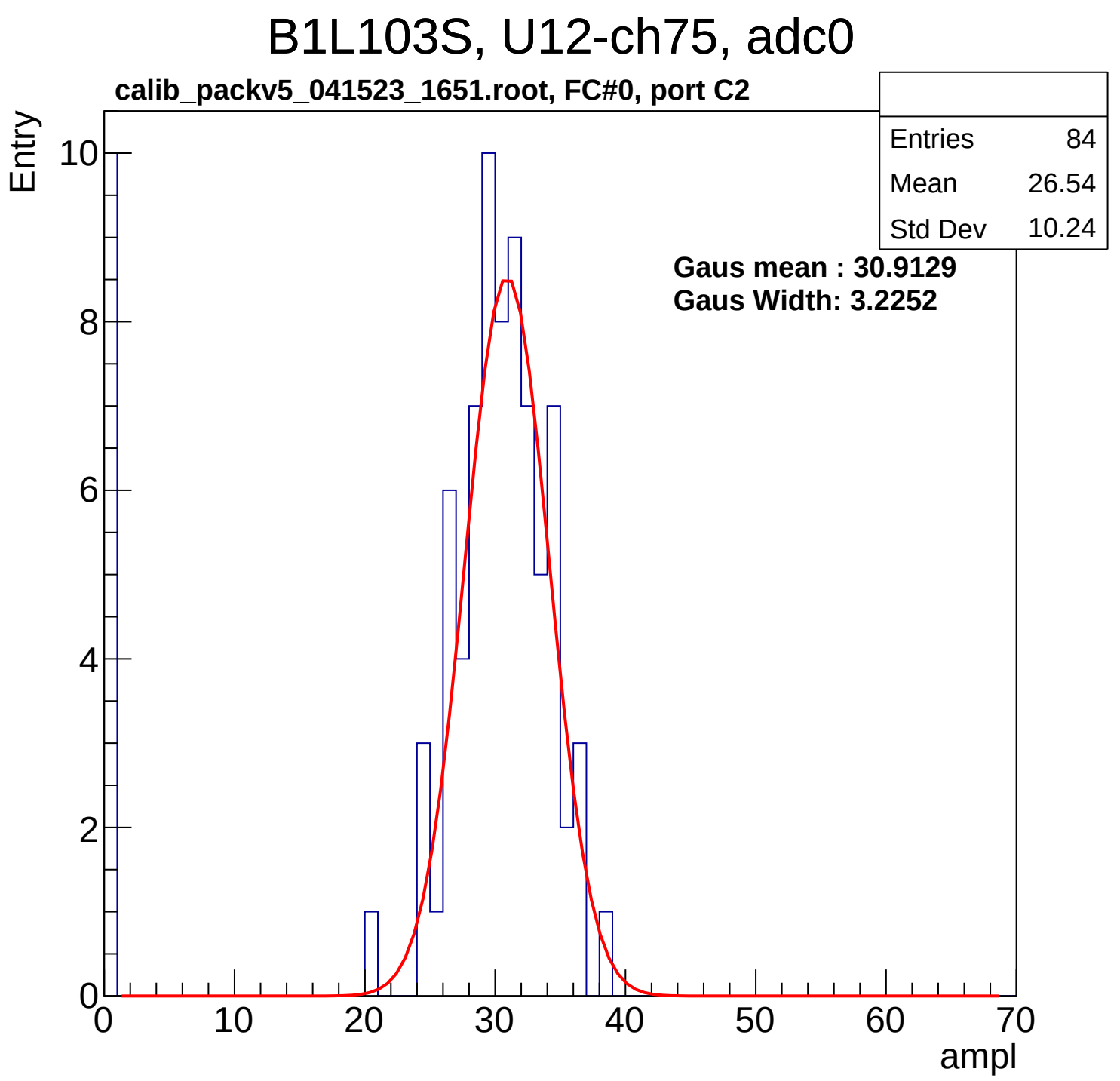
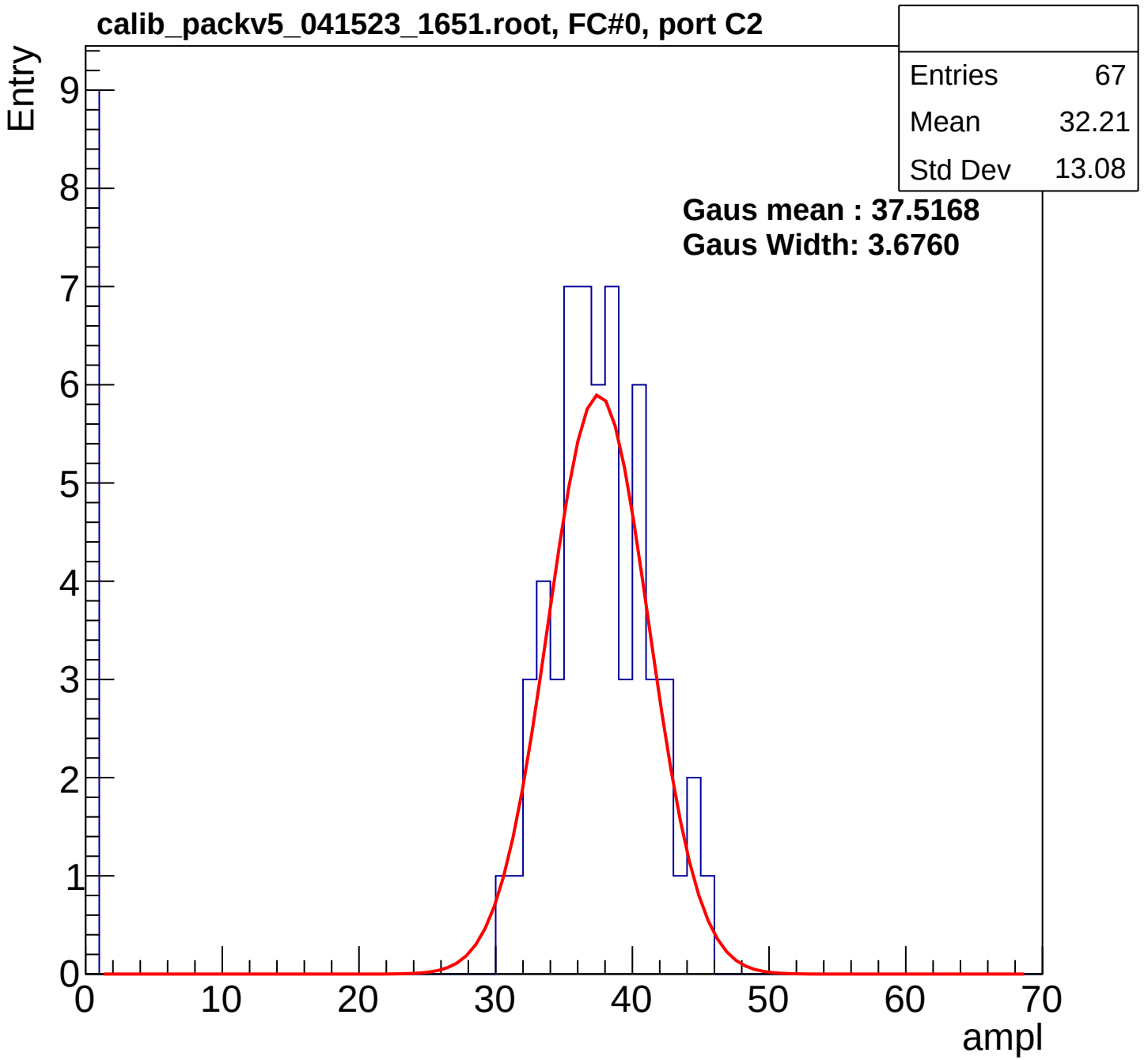
50
60
70
ampl


B1L103S, U12-ch75, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 26.54
Std Dev 10.24
Gaus mean : 30.9129
Gaus Width: 3.2252
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch75, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 32.21
Std Dev 13.08
Gaus mean : 37.5168
Gaus Width: 3.6760
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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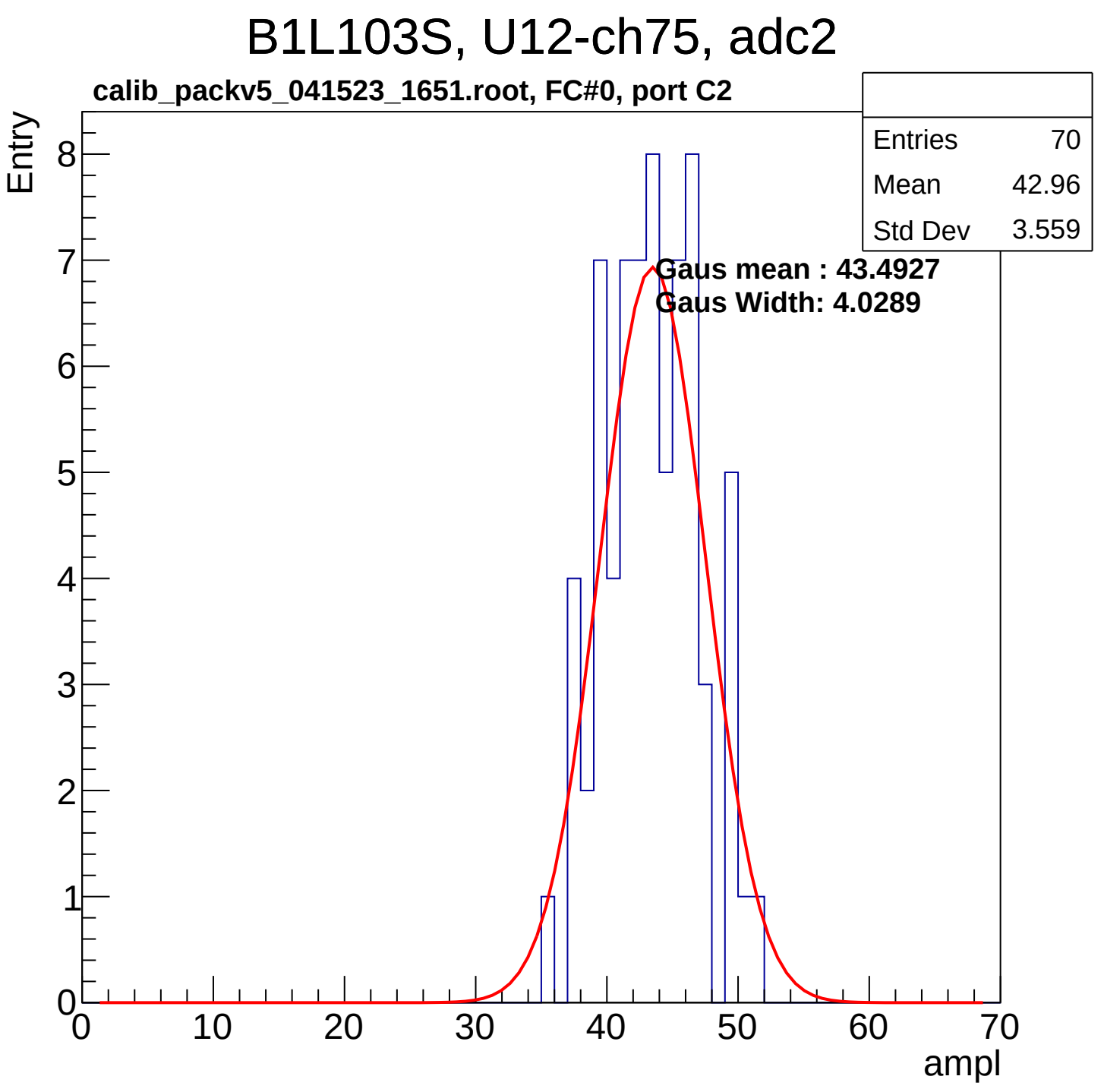
B1L103S, U12-ch75, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 42.96
Std Dev 3.559
Gaus mean : 43.4927
Gaus Width: 4.0289
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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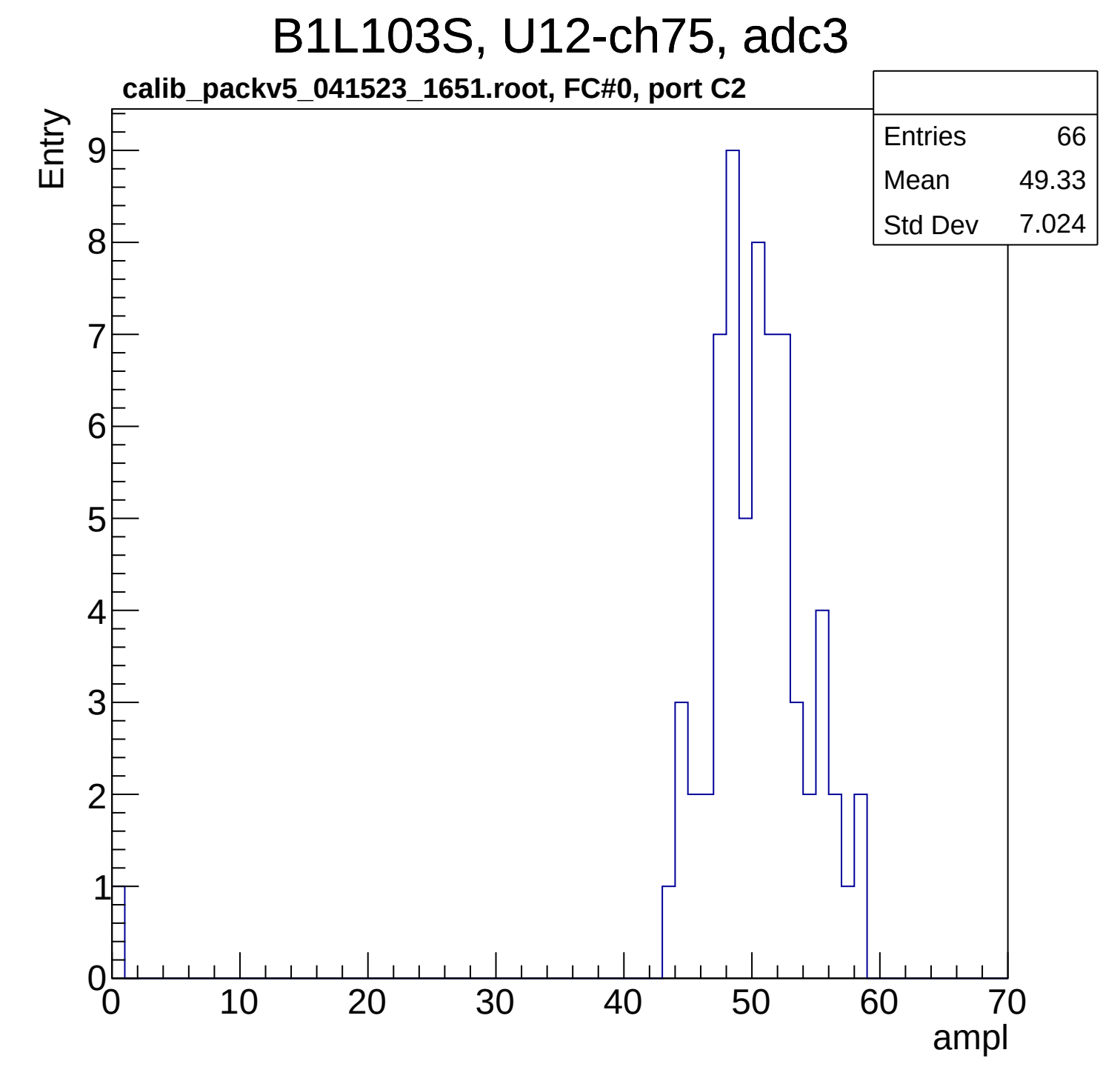
B1L103S, U12-ch75, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 49.33
Std Dev 7.024
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
50
60
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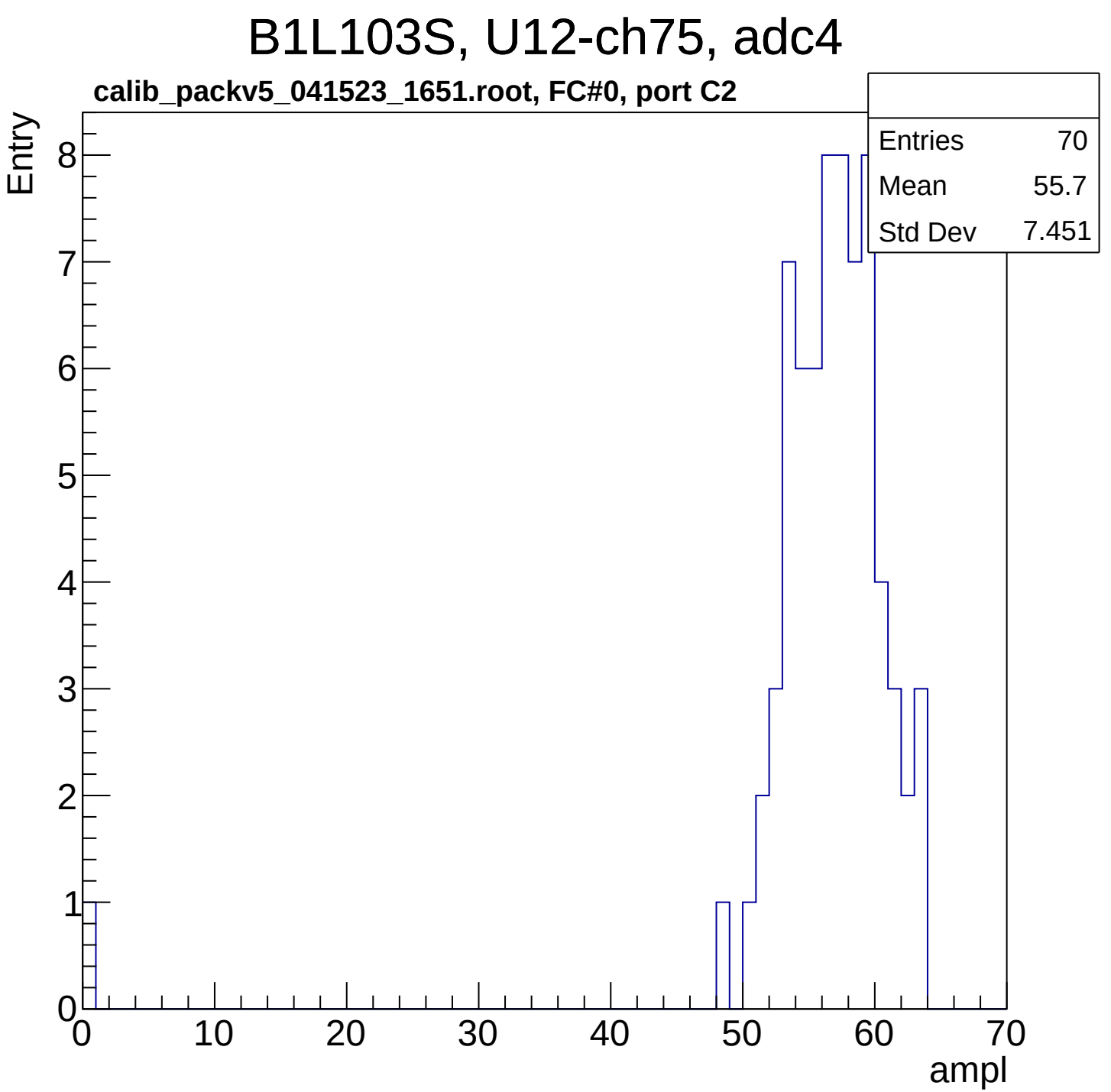
B1L103S, U12-ch75, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 55.7
Std Dev 7.451
Entry
ampl
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2
3
4
5
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7
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0
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20
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40
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60
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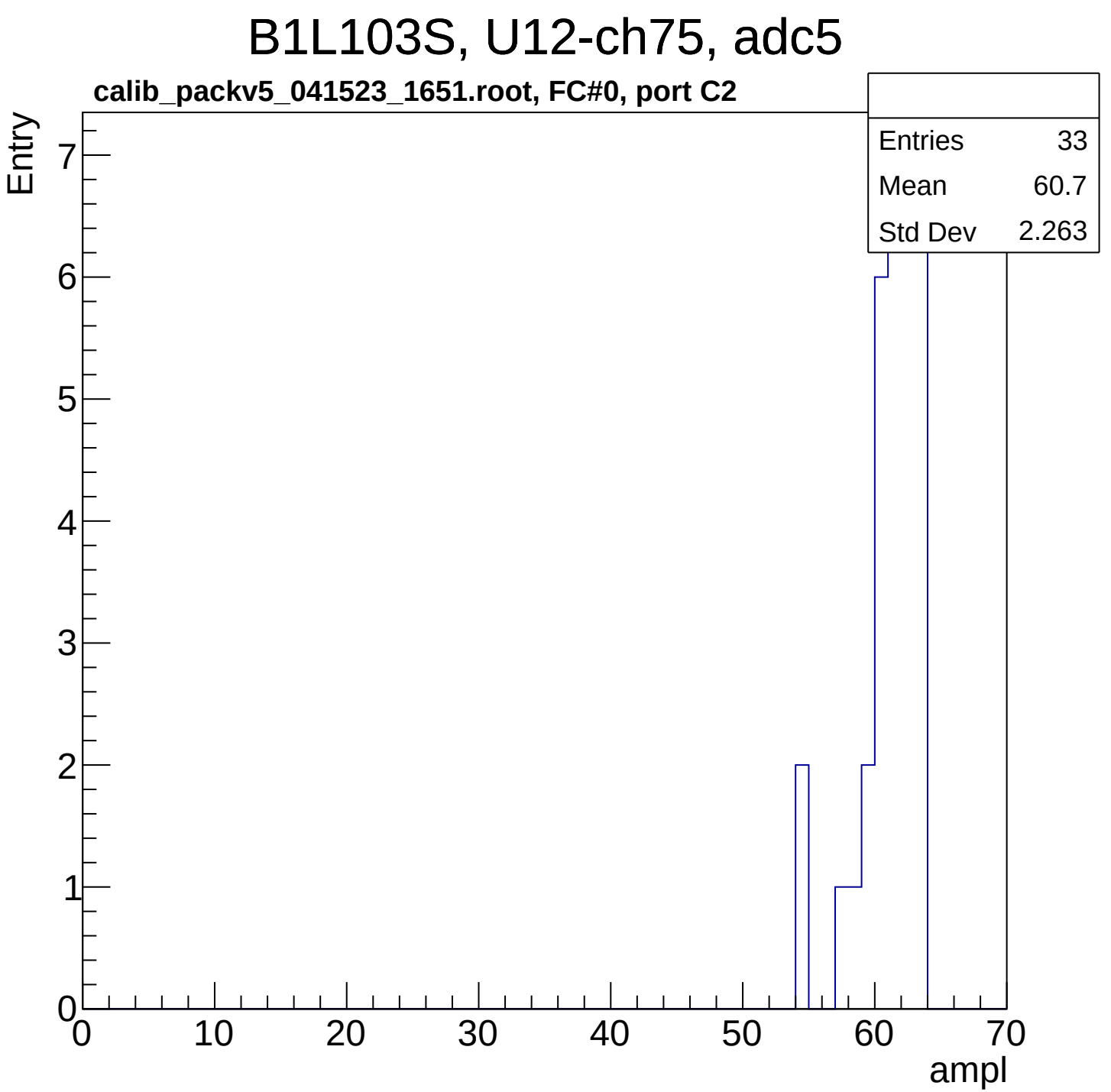
B1L103S, U12-ch75, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 60.7
Std Dev 2.263
Entry
ampl
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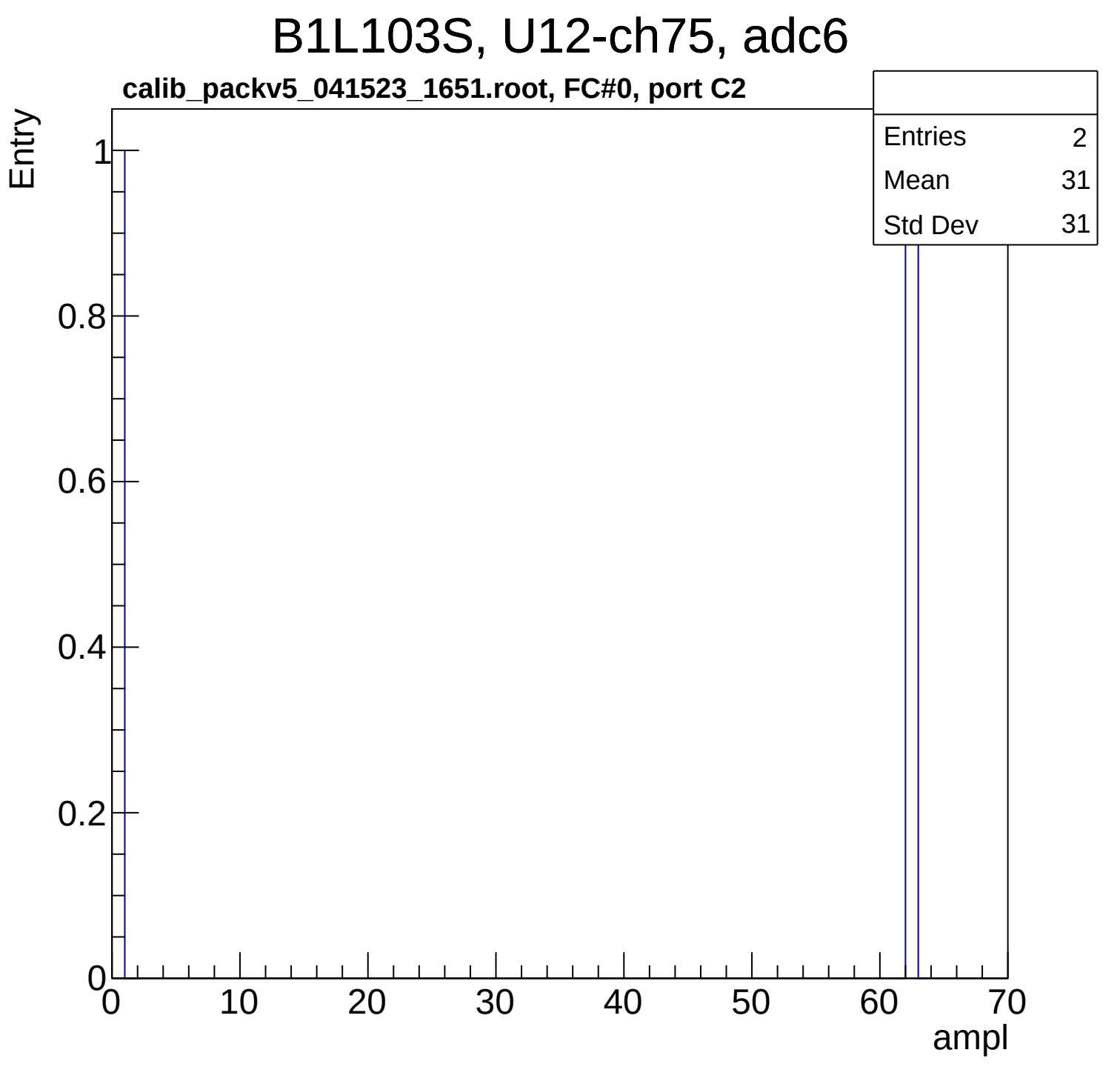
B1L103S, U12-ch75, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 31
Std Dev 31
Entry
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0.6
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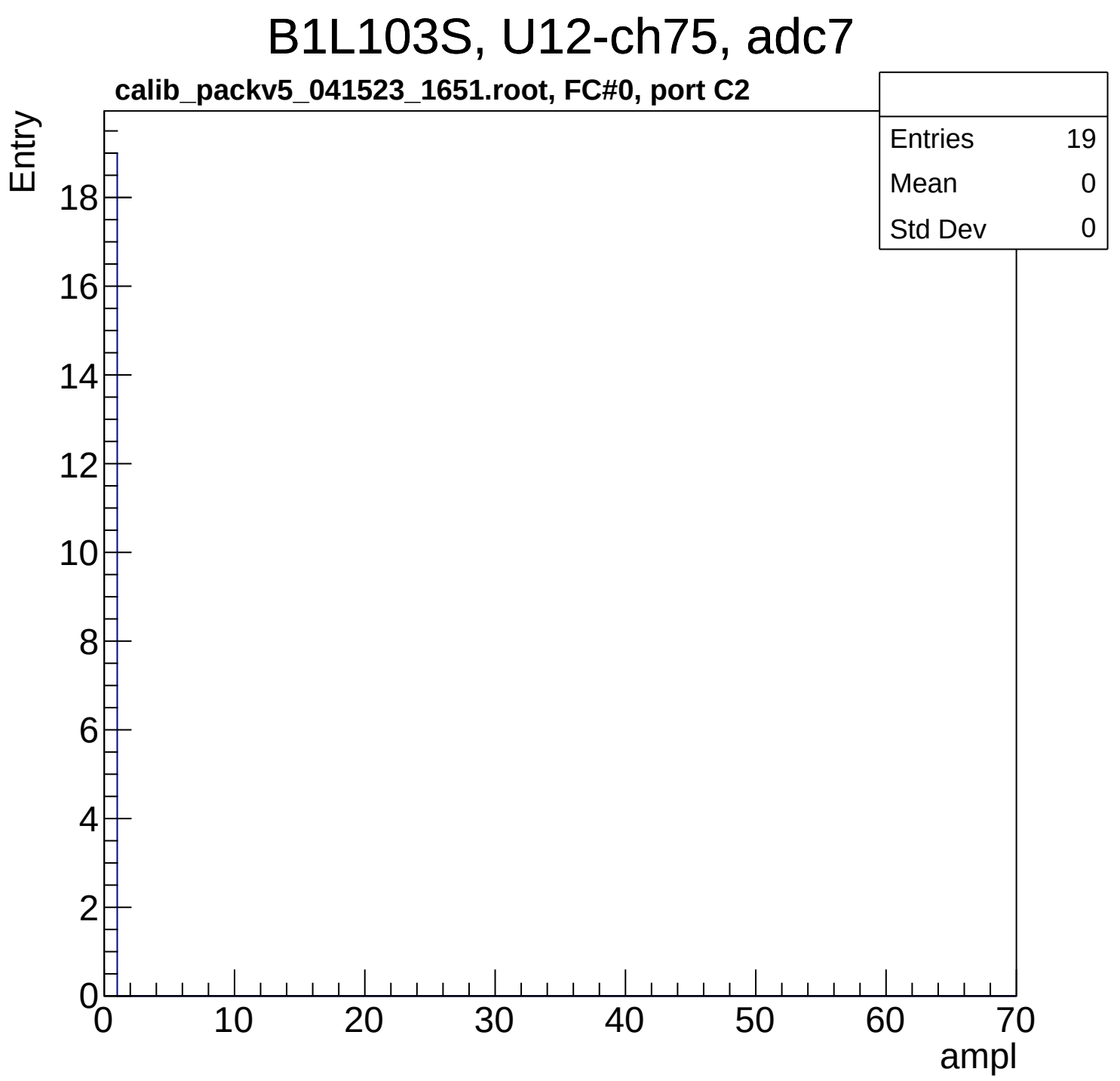
60
70
ampl


B1L103S, U12-ch75, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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6
8
10
12
14
16
18
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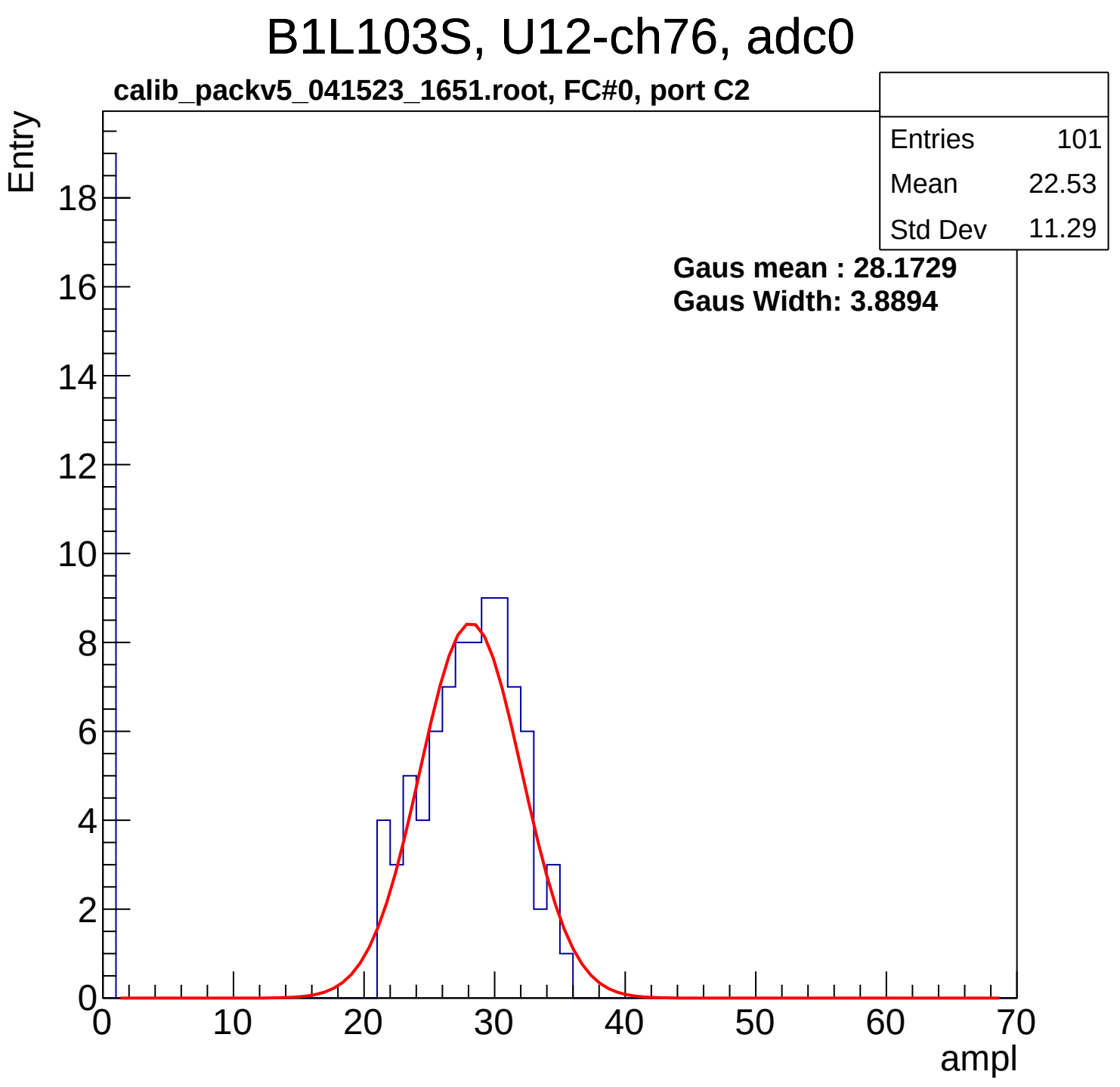
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch76, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 22.53
Std Dev 11.29
Gaus mean : 28.1729
Gaus Width: 3.8894
Entry
ampl
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4
6
8
10
12
14
16
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0
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60
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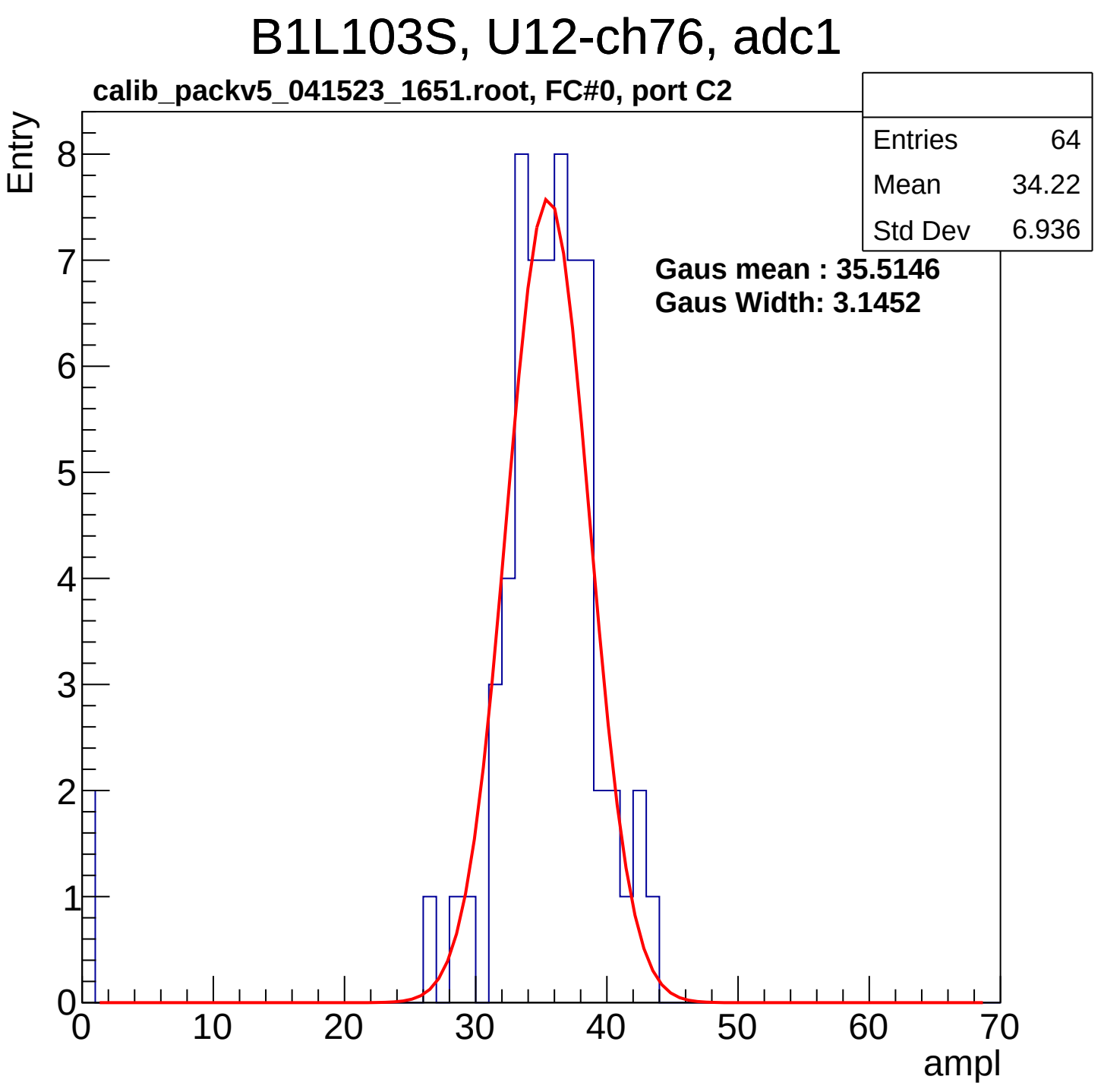
B1L103S, U12-ch76, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 34.22
Std Dev 6.936
Gaus mean : 35.5146
Gaus Width: 3.1452
Entry
ampl
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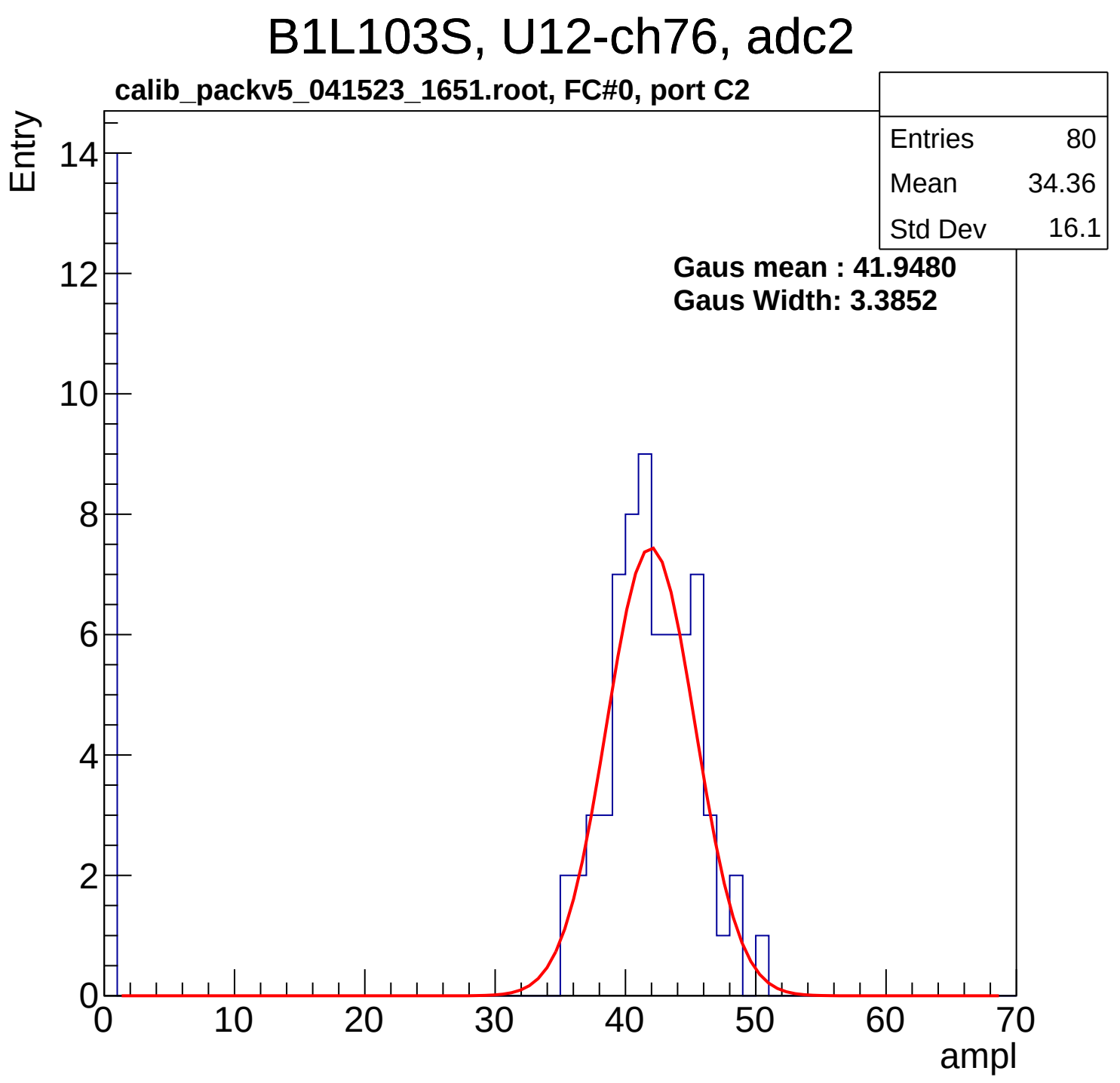
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U12-ch76, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 34.36
Std Dev 16.1
Gaus mean : 41.9480
Gaus Width: 3.3852
Entry
ampl
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10
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0
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40
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60
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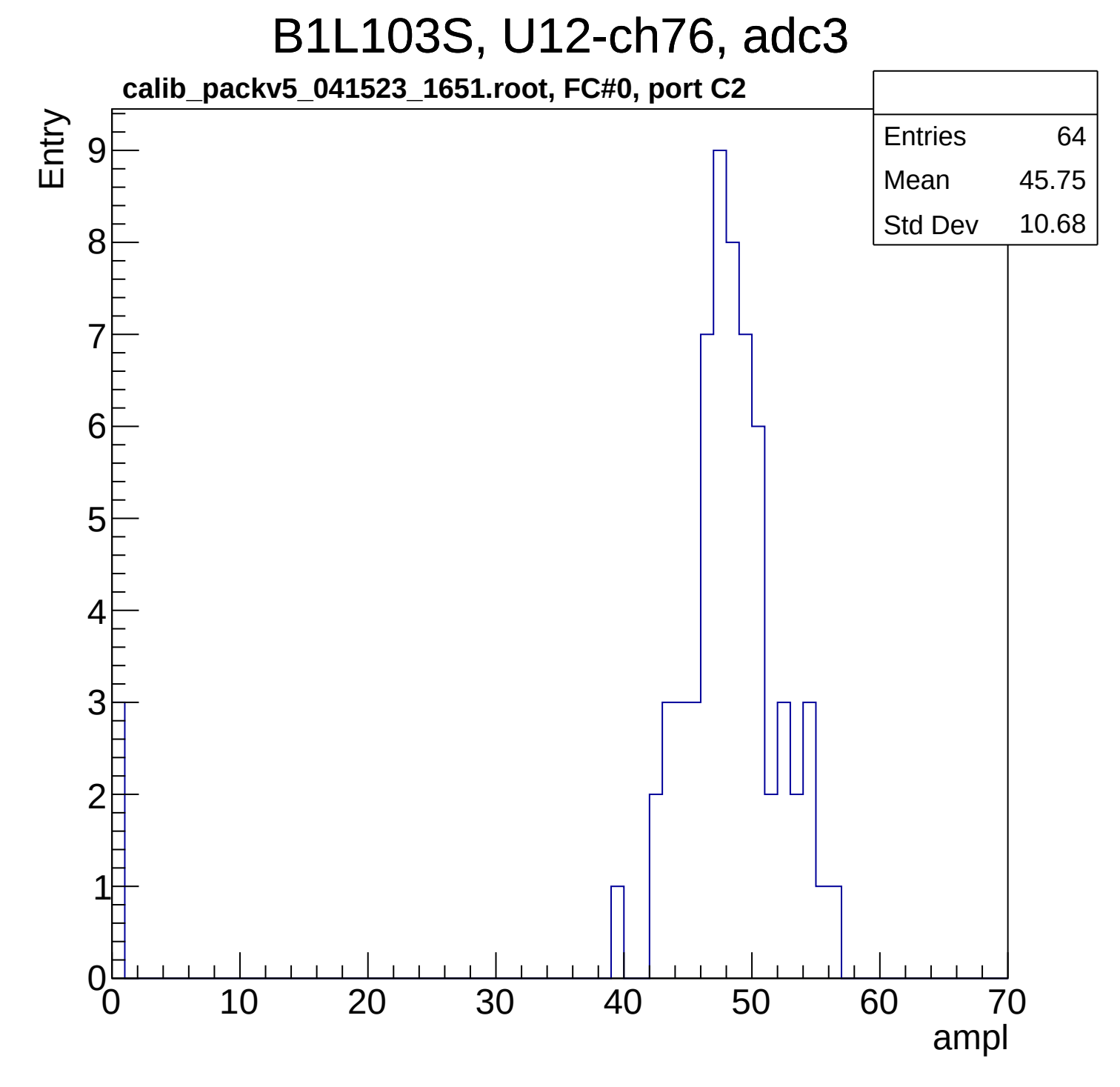
B1L103S, U12-ch76, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 45.75
Std Dev 10.68
Entry
ampl
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10
20
30
40
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1
2
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6
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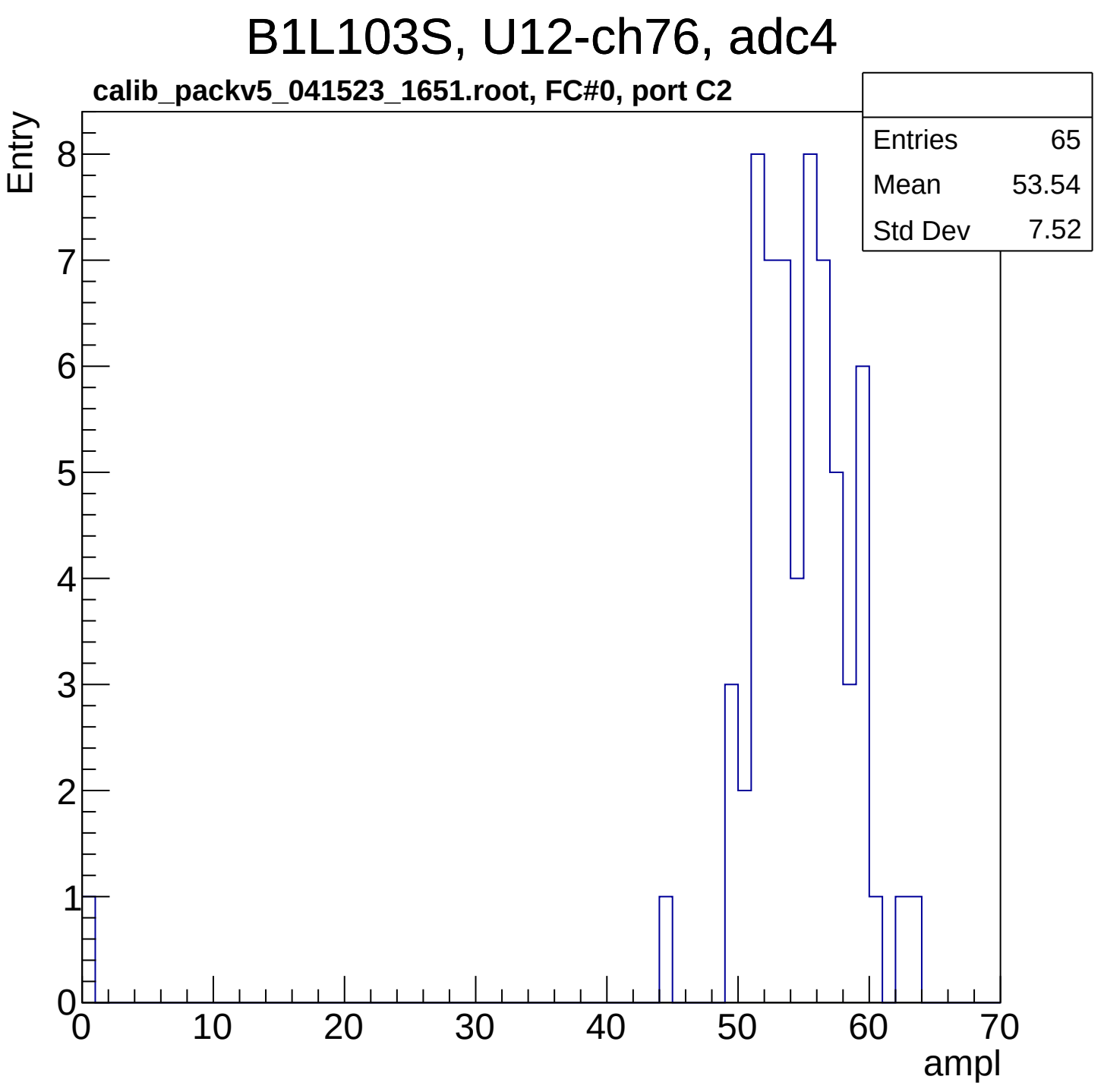
8
9


B1L103S, U12-ch76, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 53.54
Std Dev 7.52
Entry
ampl
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2
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4
5
6
7
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0
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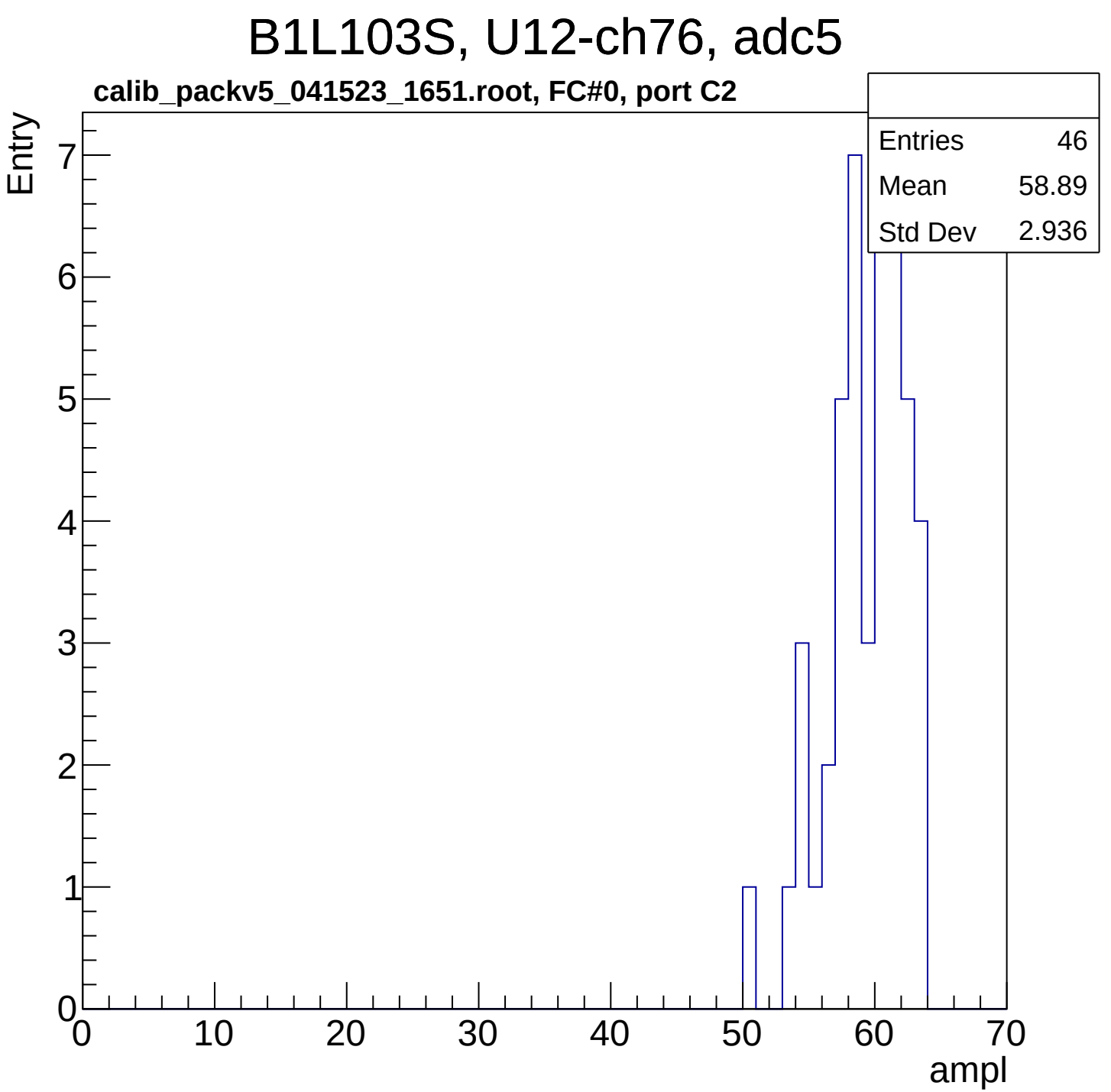
B1L103S, U12-ch76, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 58.89
Std Dev 2.936
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
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40
50
60
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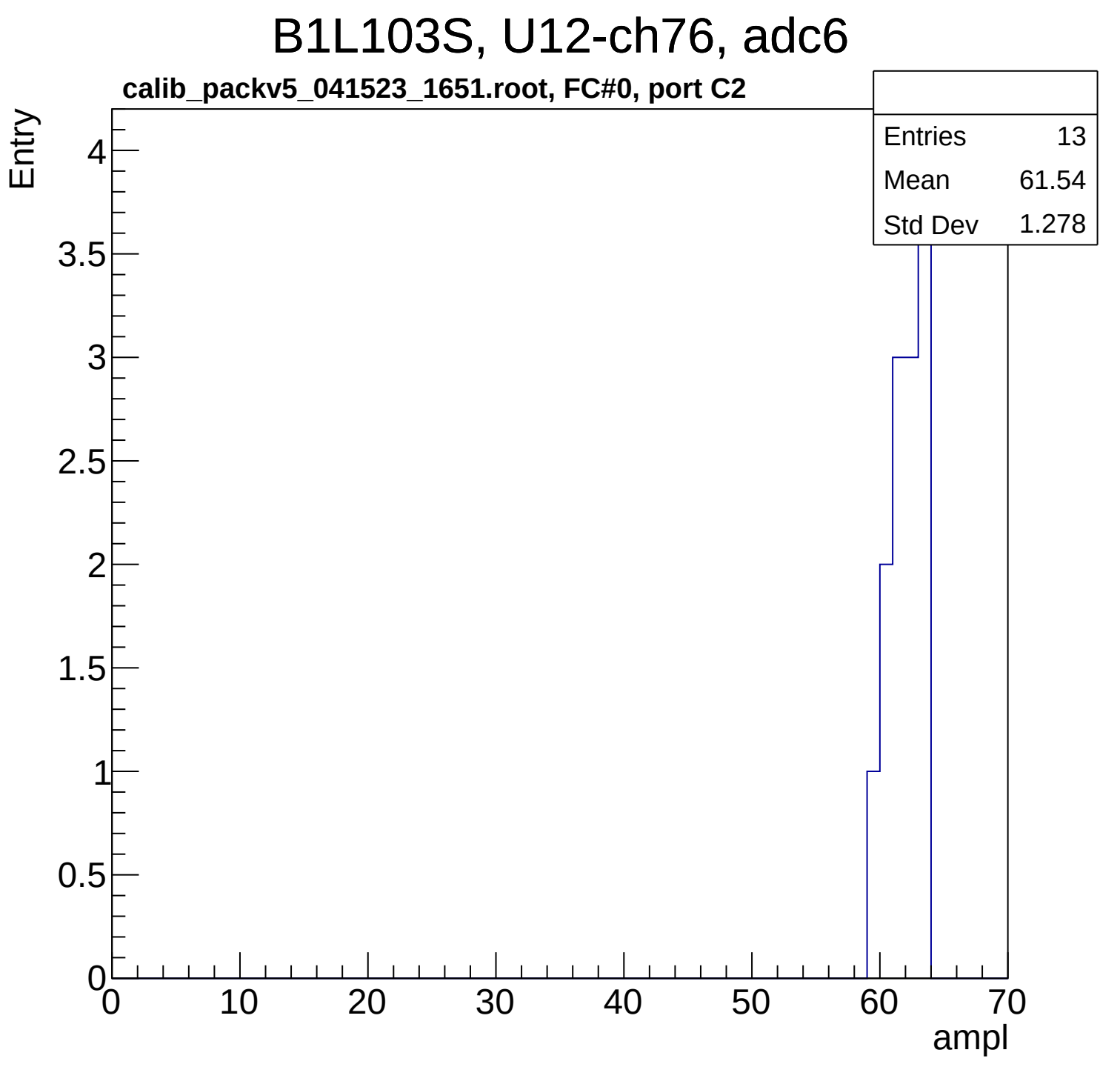
B1L103S, U12-ch76, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 61.54
Std Dev 1.278
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
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20
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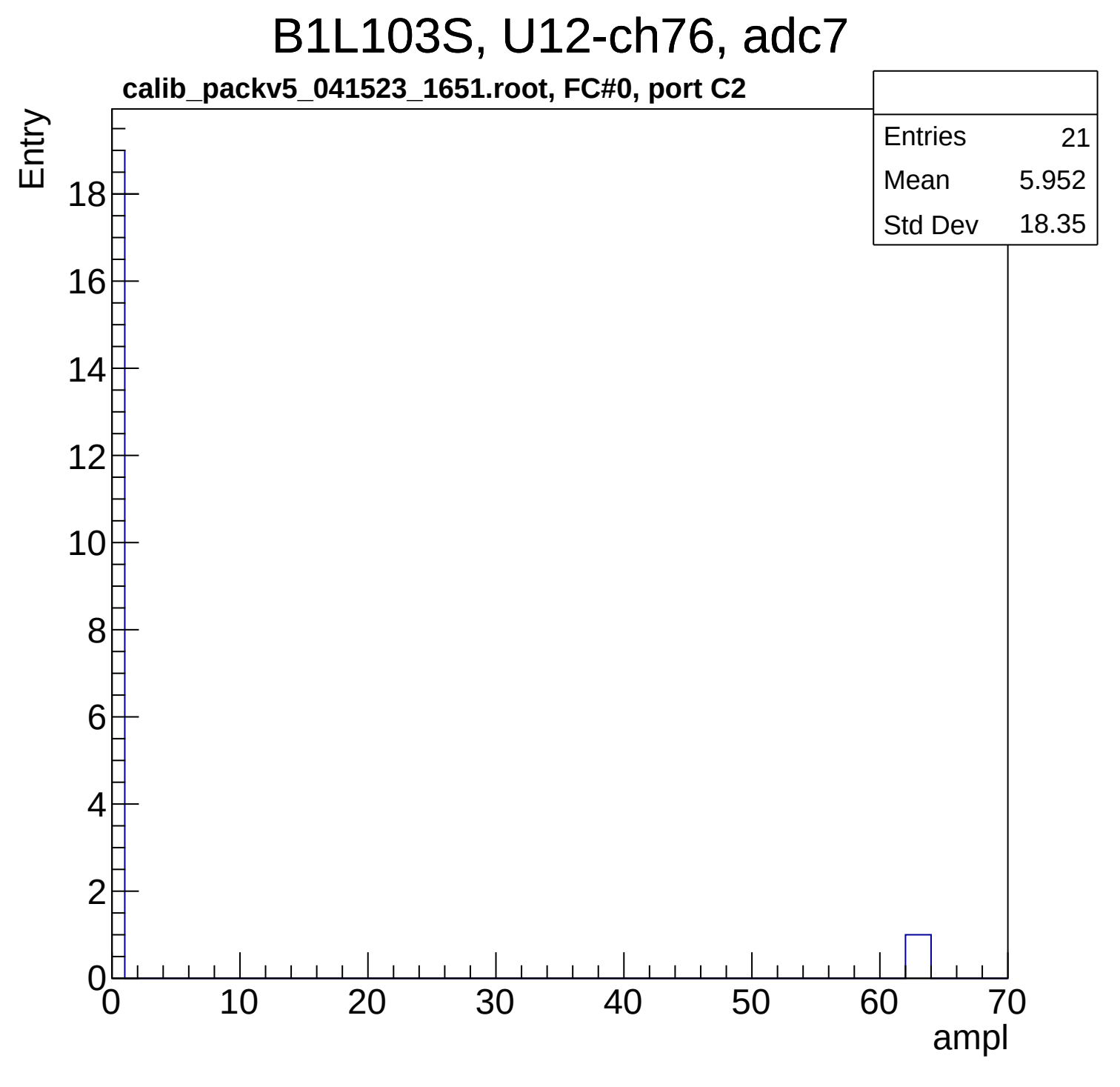
B1L103S, U12-ch76, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
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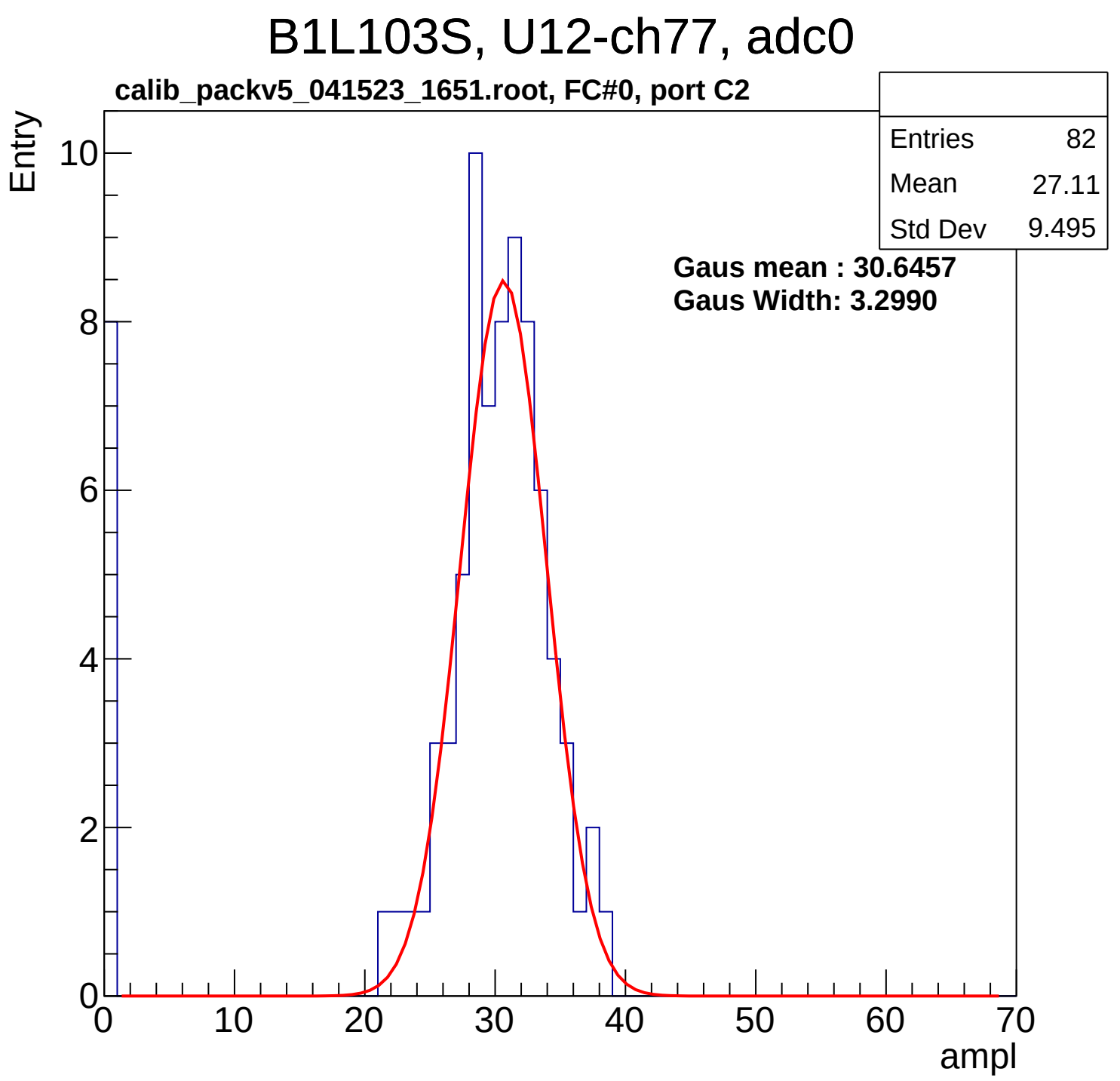
70
ampl


B1L103S, U12-ch77, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 27.11
Std Dev 9.495
Gaus mean : 30.6457
Gaus Width: 3.2990
Entry
ampl
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6
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10
0
10
20
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40
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60
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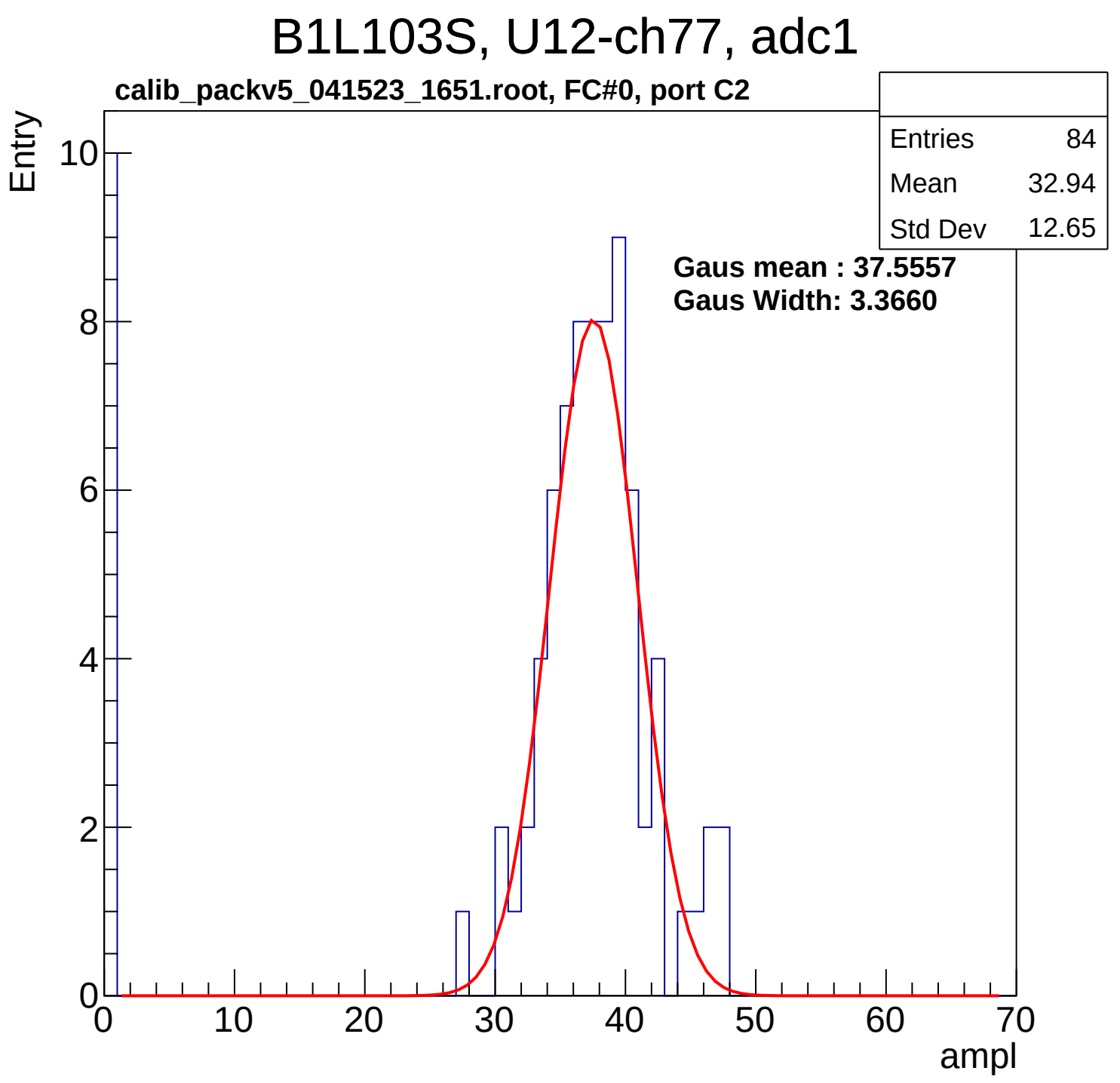
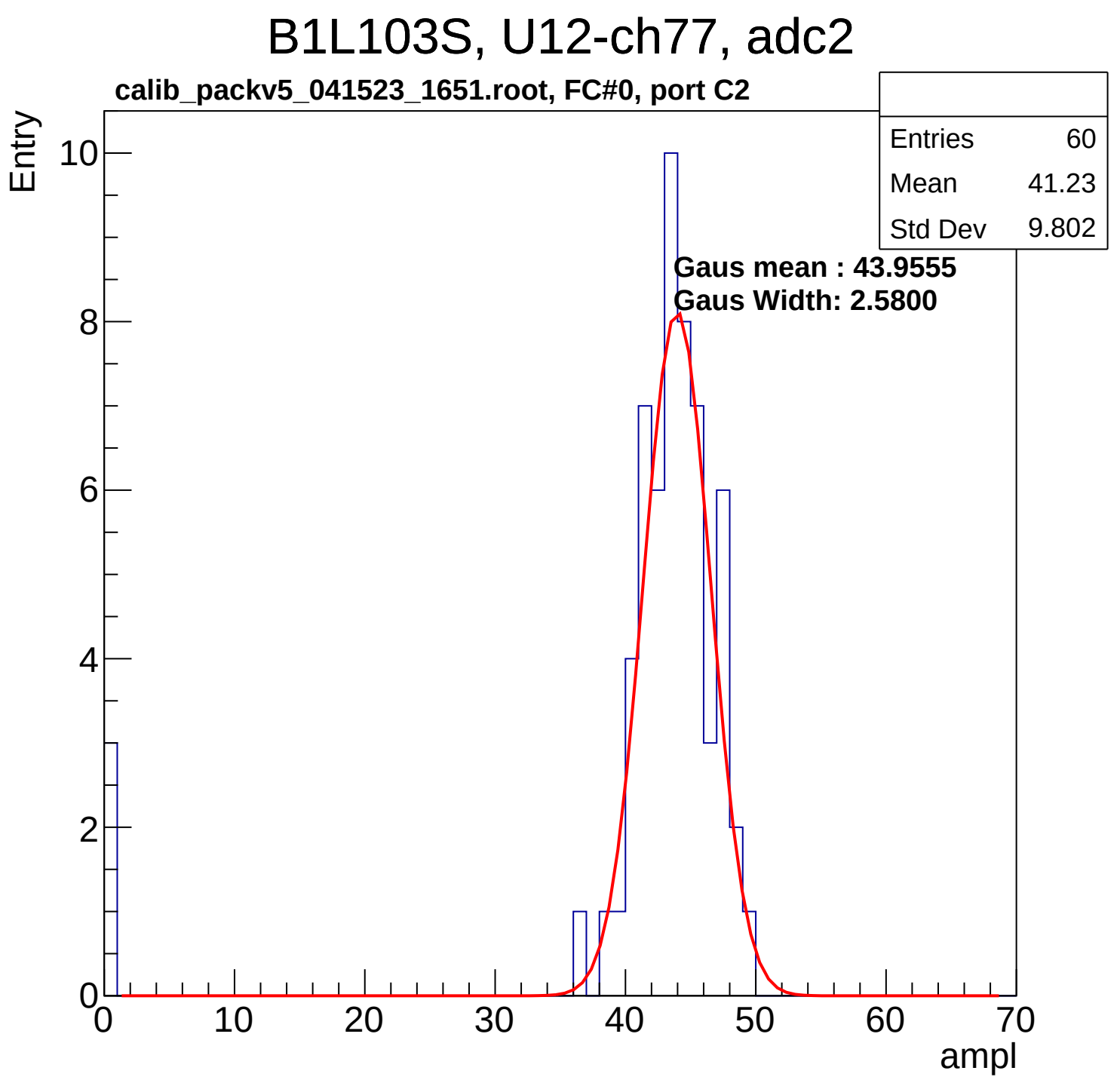
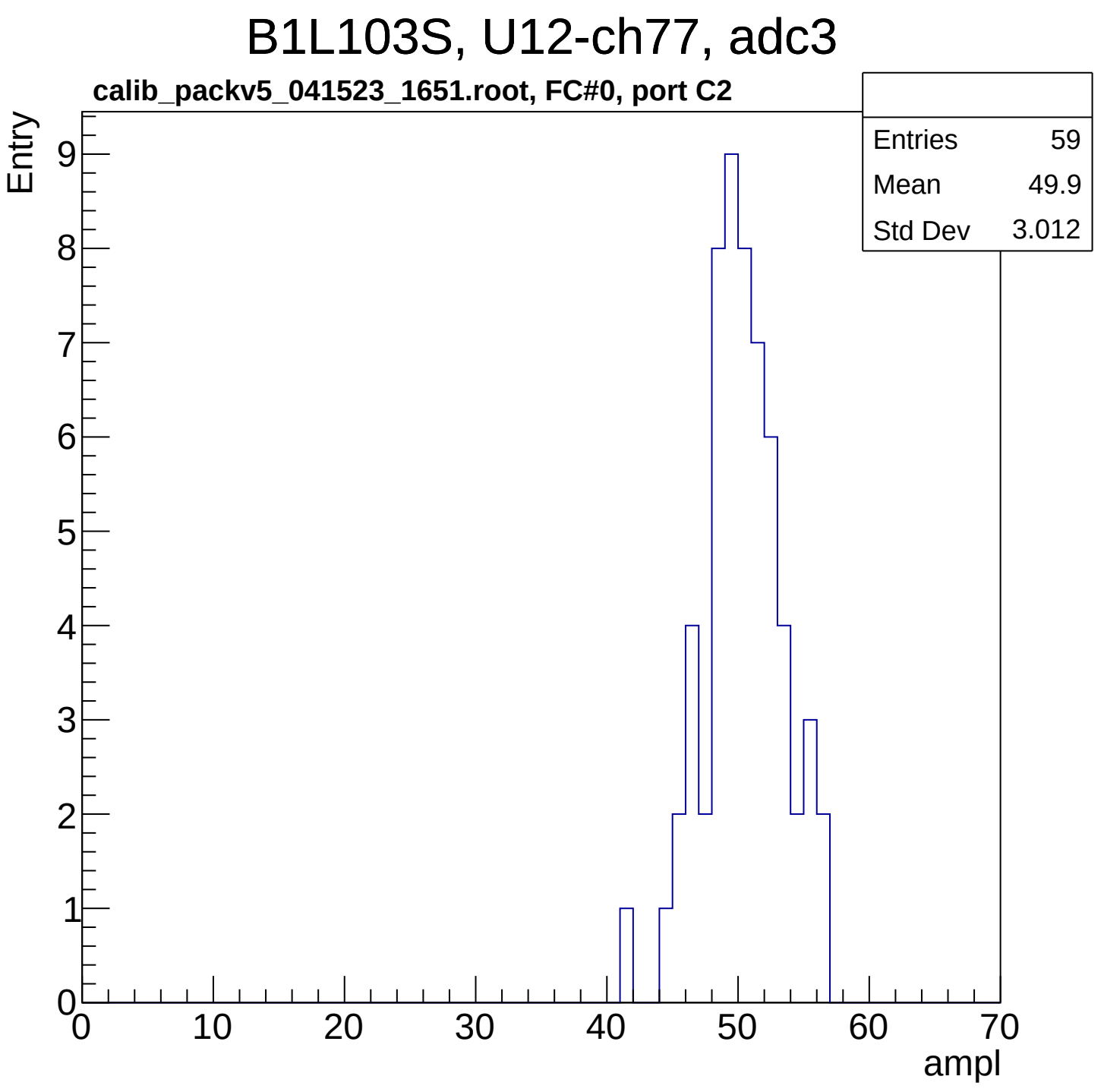
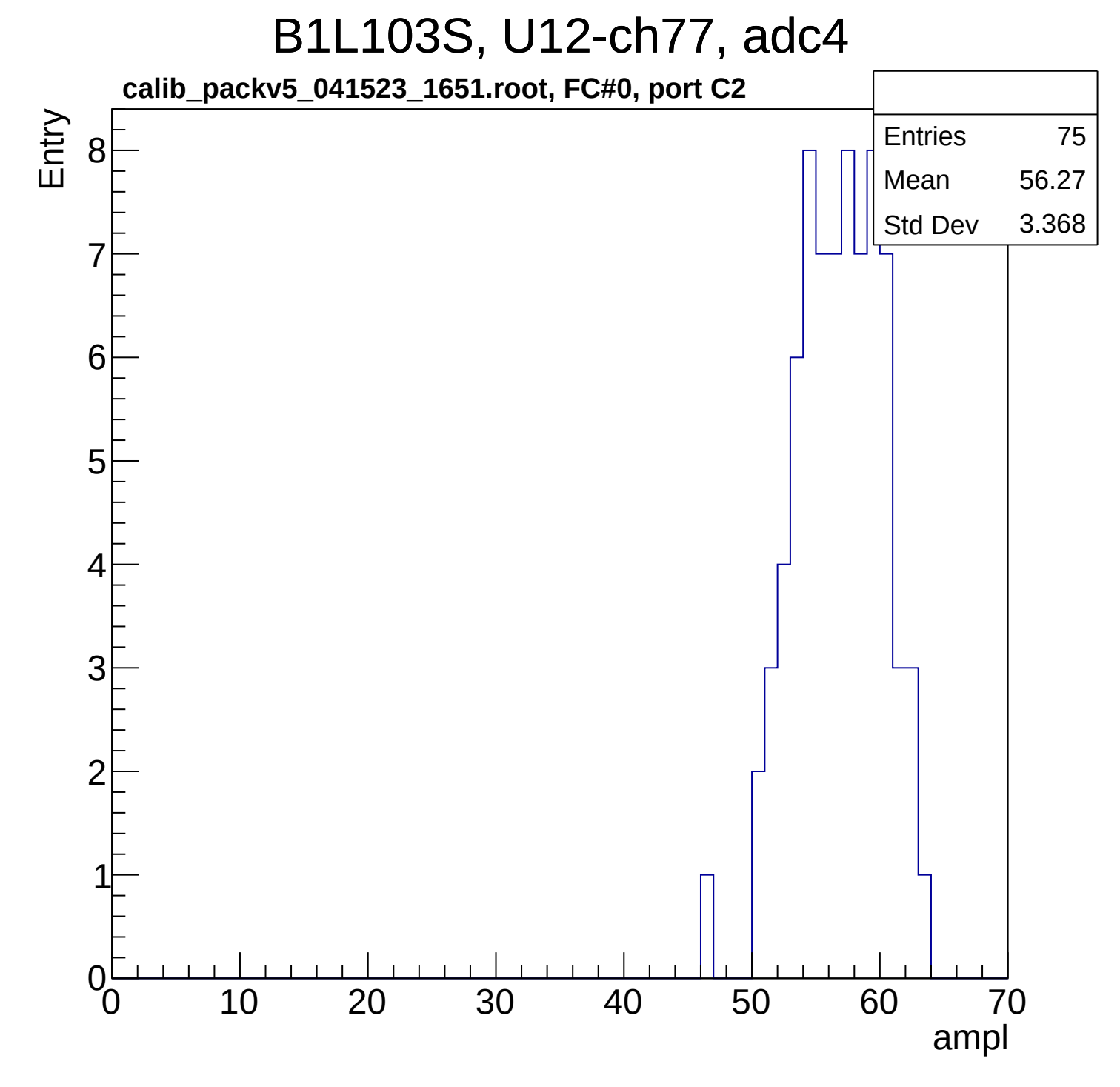
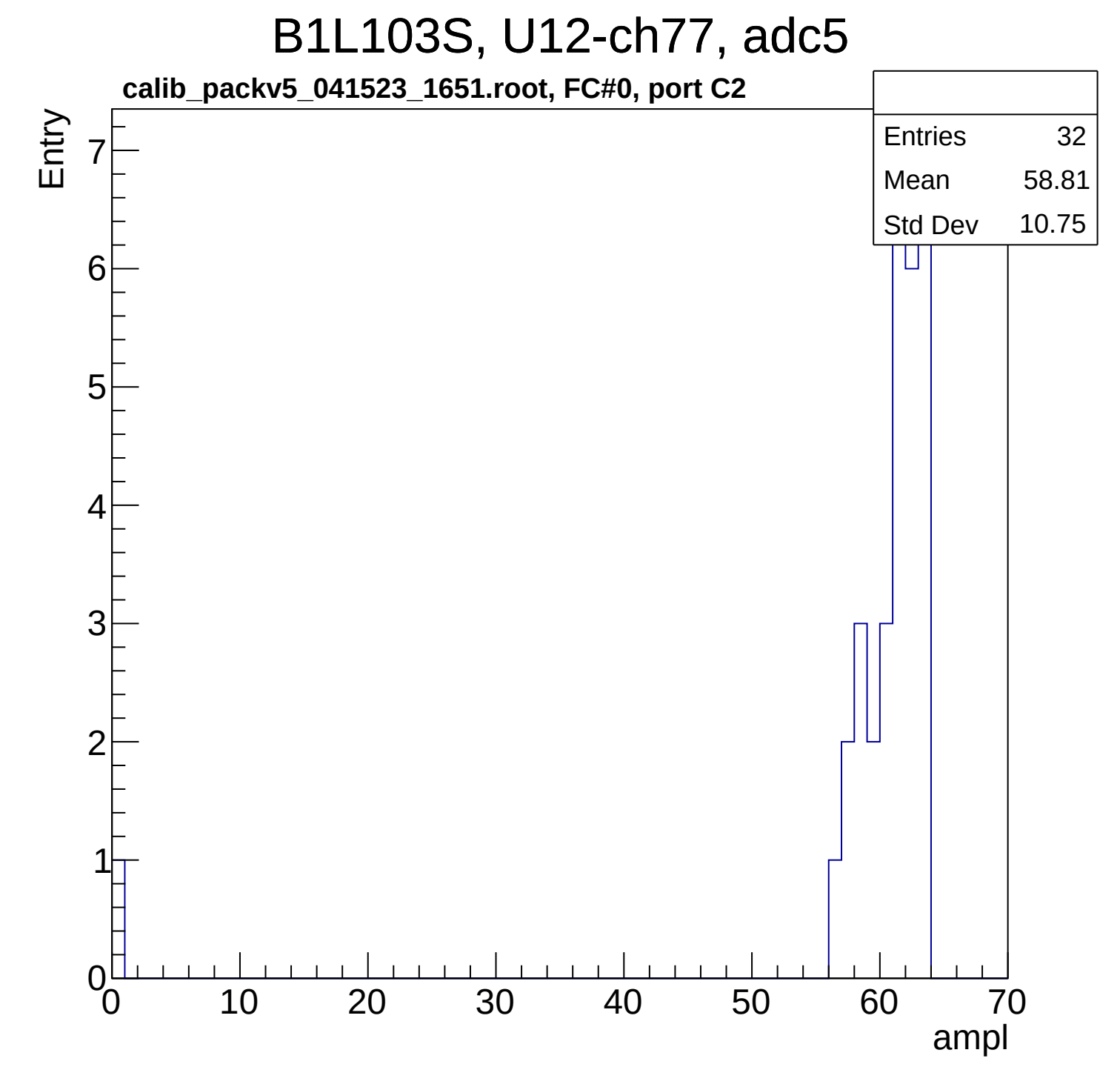
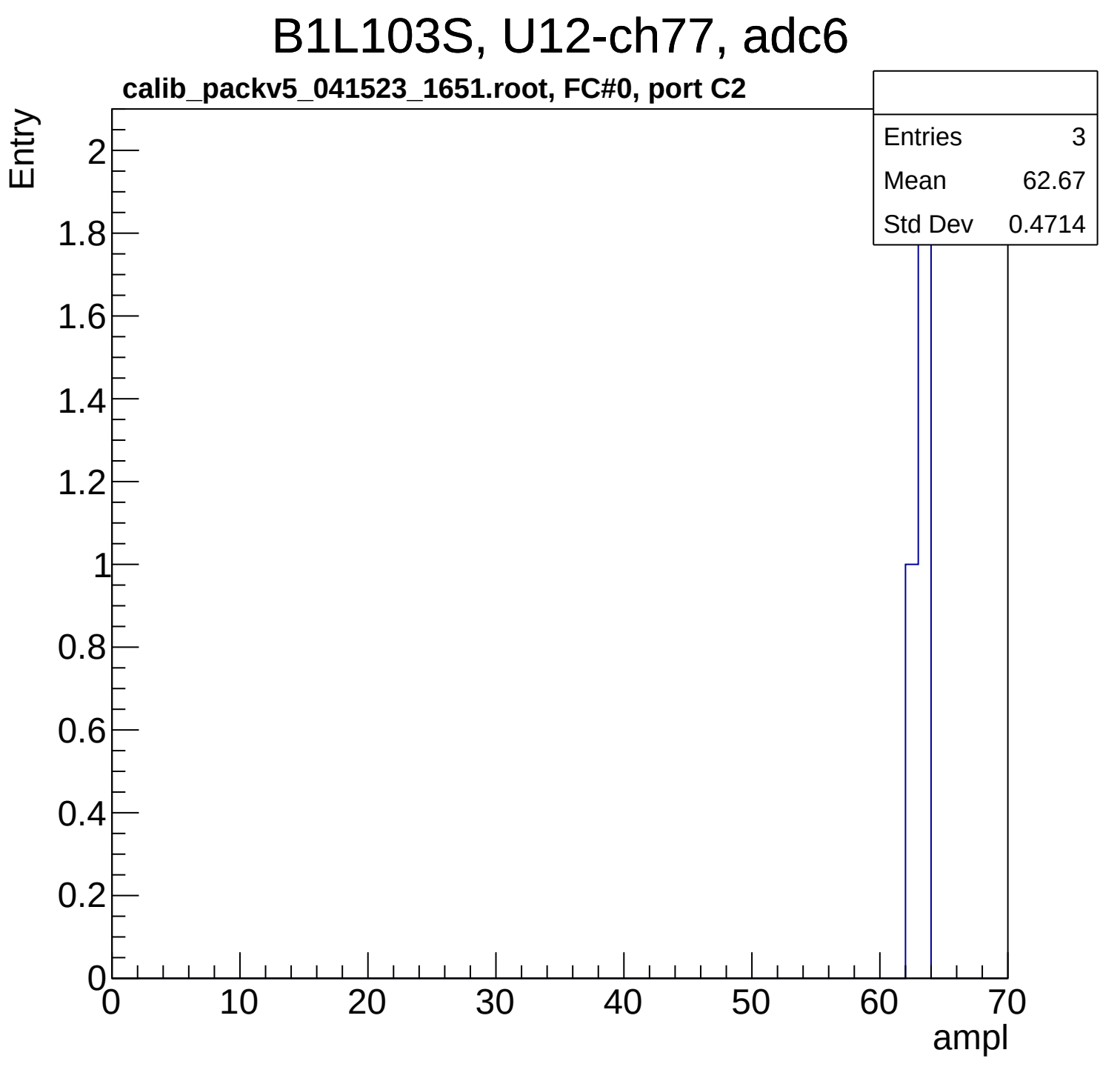

B1L103S, U12-ch77, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 32.94
Std Dev 12.65
Gaus mean : 37.5557
Gaus Width: 3.3660
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

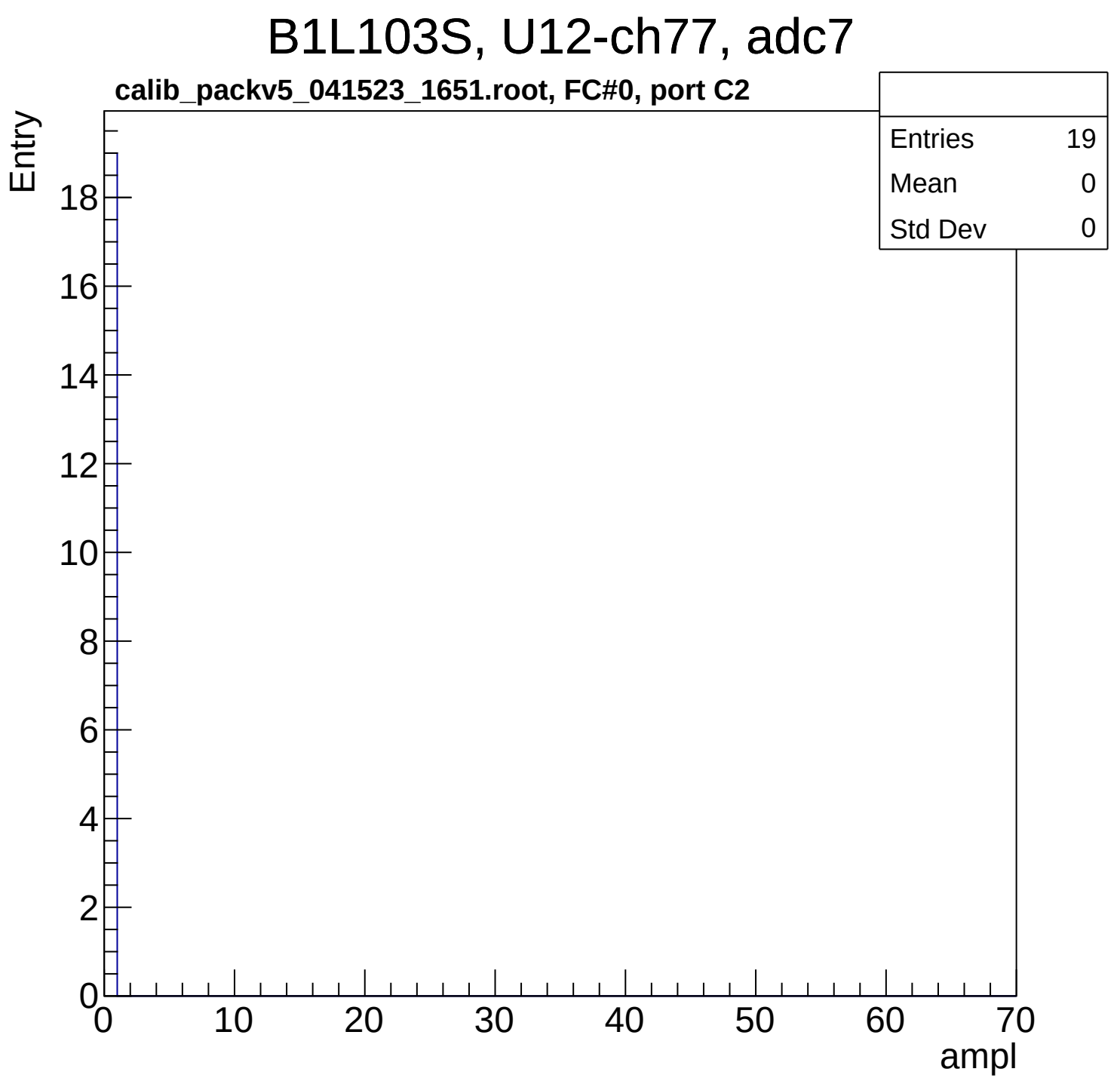

B1L103S, U12-ch77, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 41.23
Std Dev 9.802
Gaus mean : 43.9555
Gaus Width: 2.5800
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

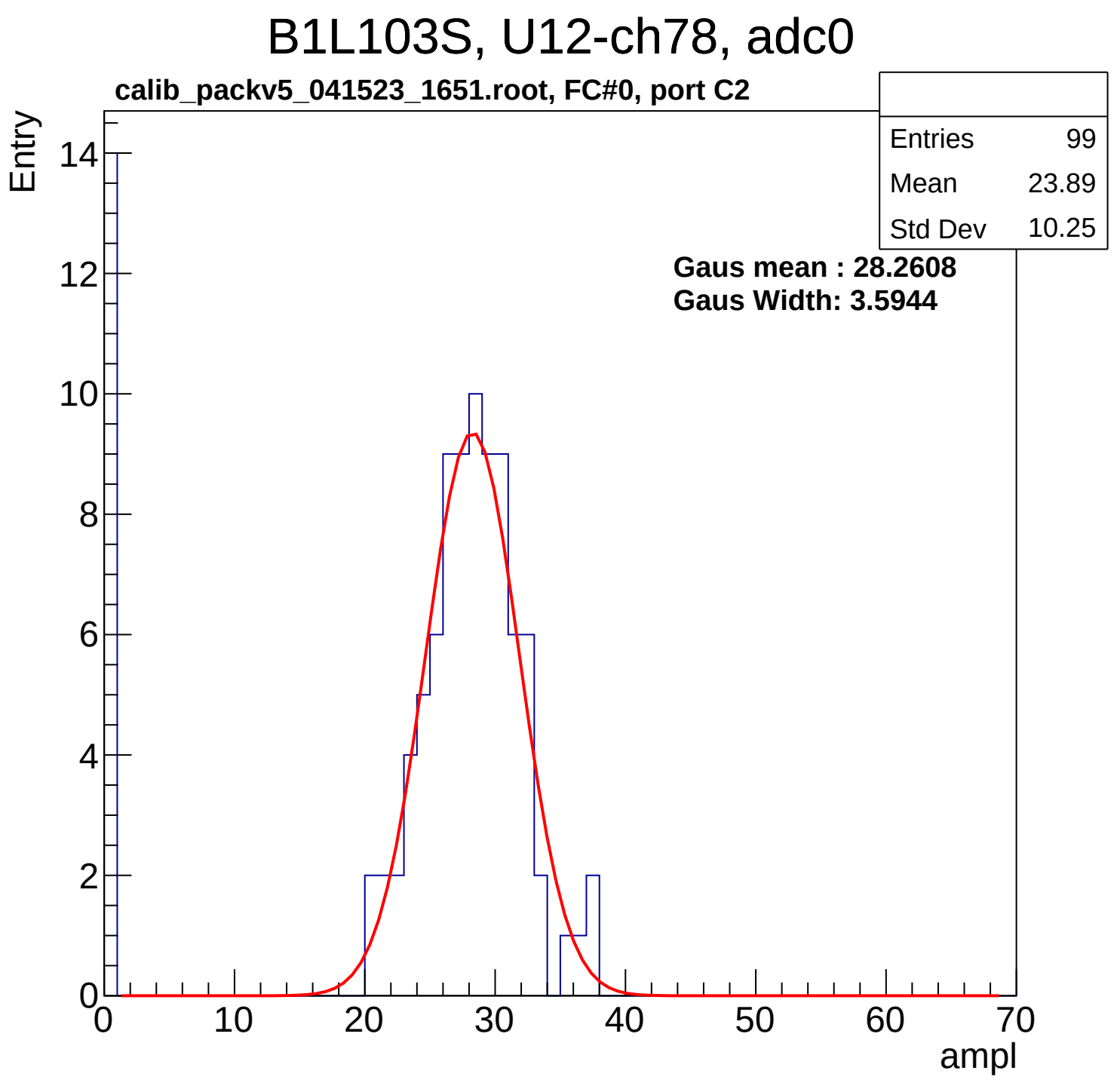

B1L103S, U12-ch77, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 49.9
Std Dev 3.012
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

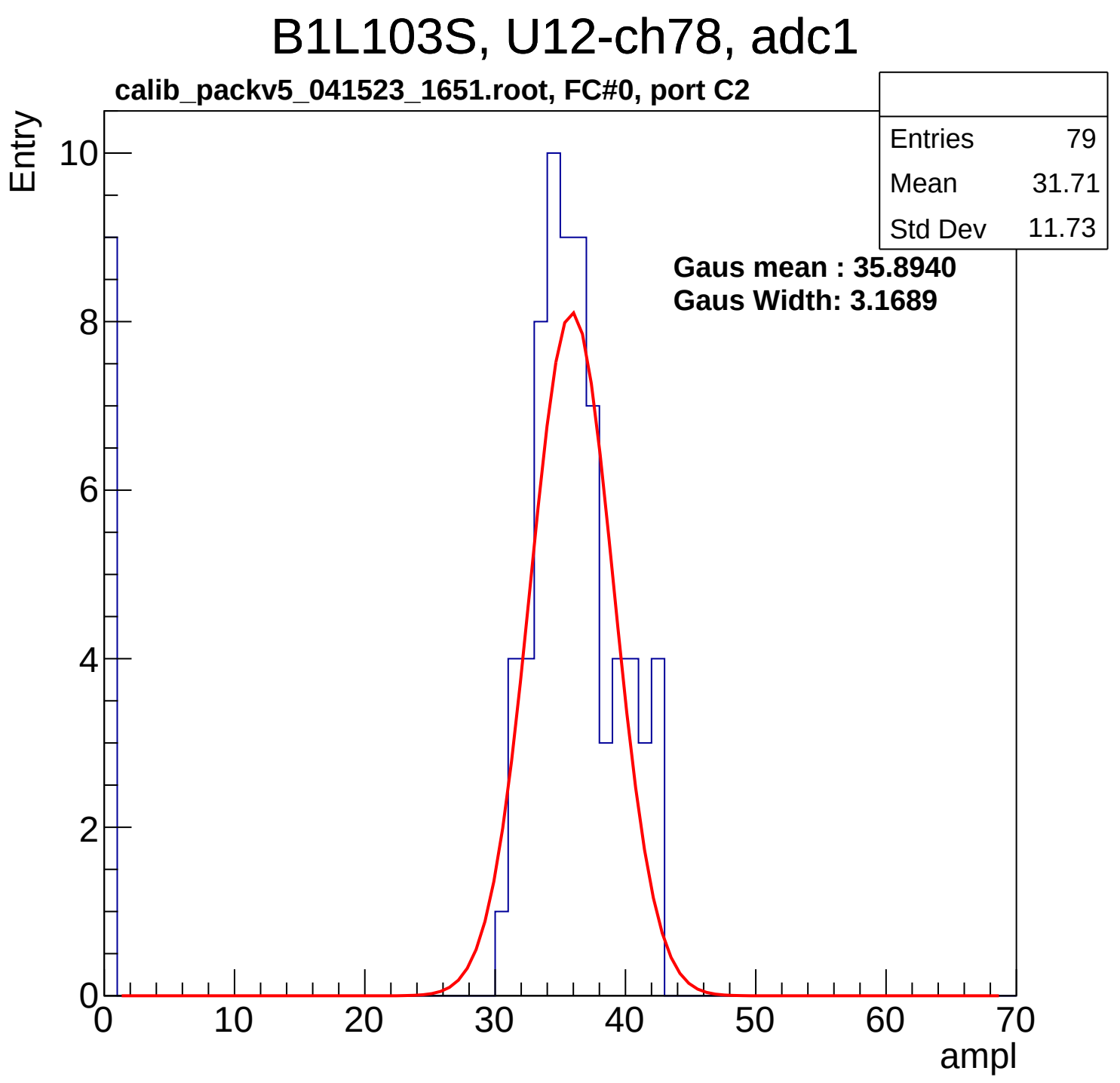

B1L103S, U12-ch77, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 56.27
Std Dev 3.368
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

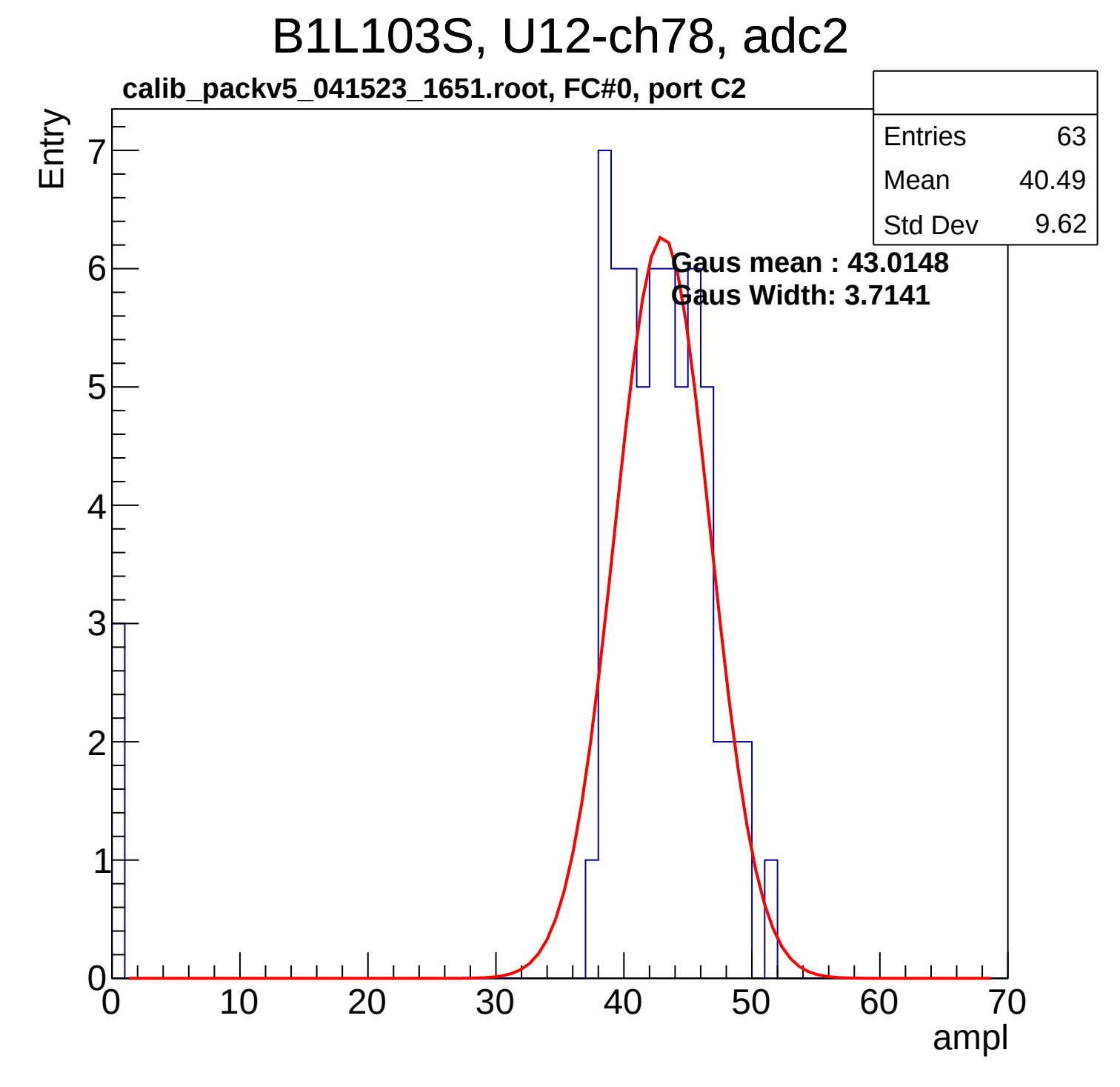

B1L103S, U12-ch77, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 32
Mean 58.81
Std Dev 10.75
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

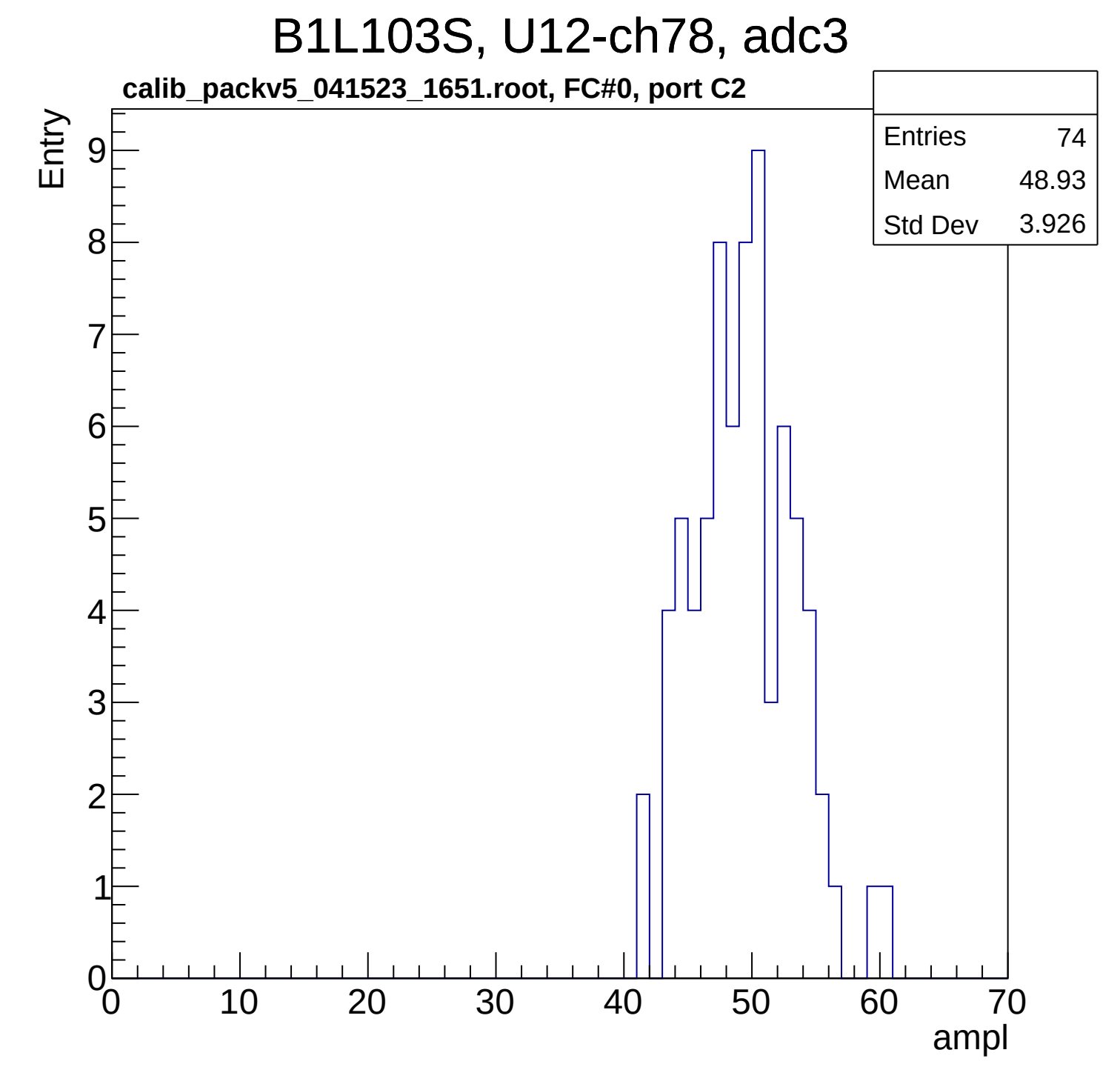

B1L103S, U12-ch77, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

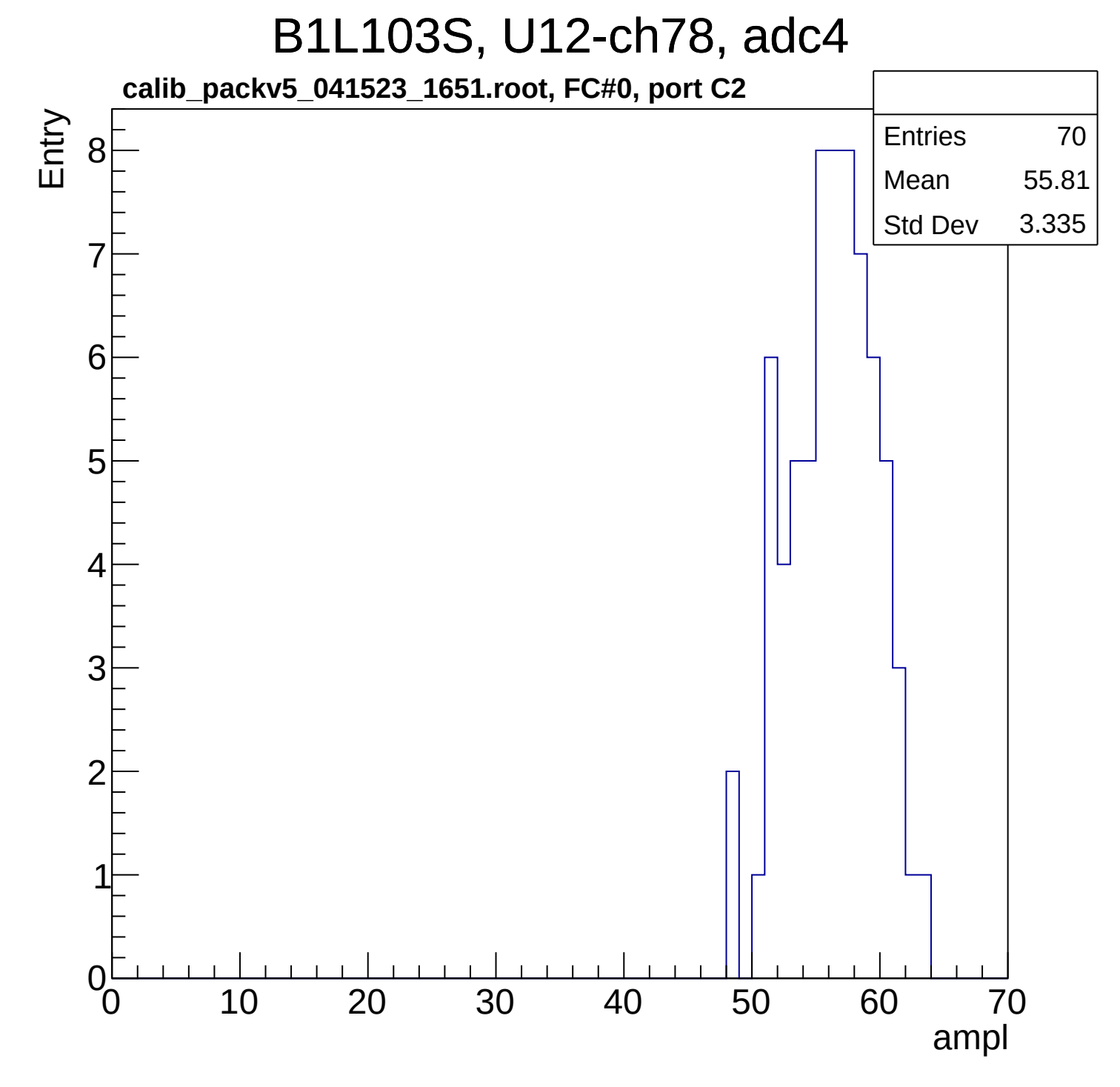

B1L103S, U12-ch77, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch78, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 23.89
Std Dev 10.25
Gaus mean : 28.2608
Gaus Width: 3.5944
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U12-ch78, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 31.71
Std Dev 11.73
Gaus mean : 35.8940
Gaus Width: 3.1689
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch78, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 40.49
Std Dev 9.62
Gaus mean : 43.0148
Gaus Width: 3.7141
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U12-ch78, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 48.93
Std Dev 3.926
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch78, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 55.81
Std Dev 3.335
Entry
ampl
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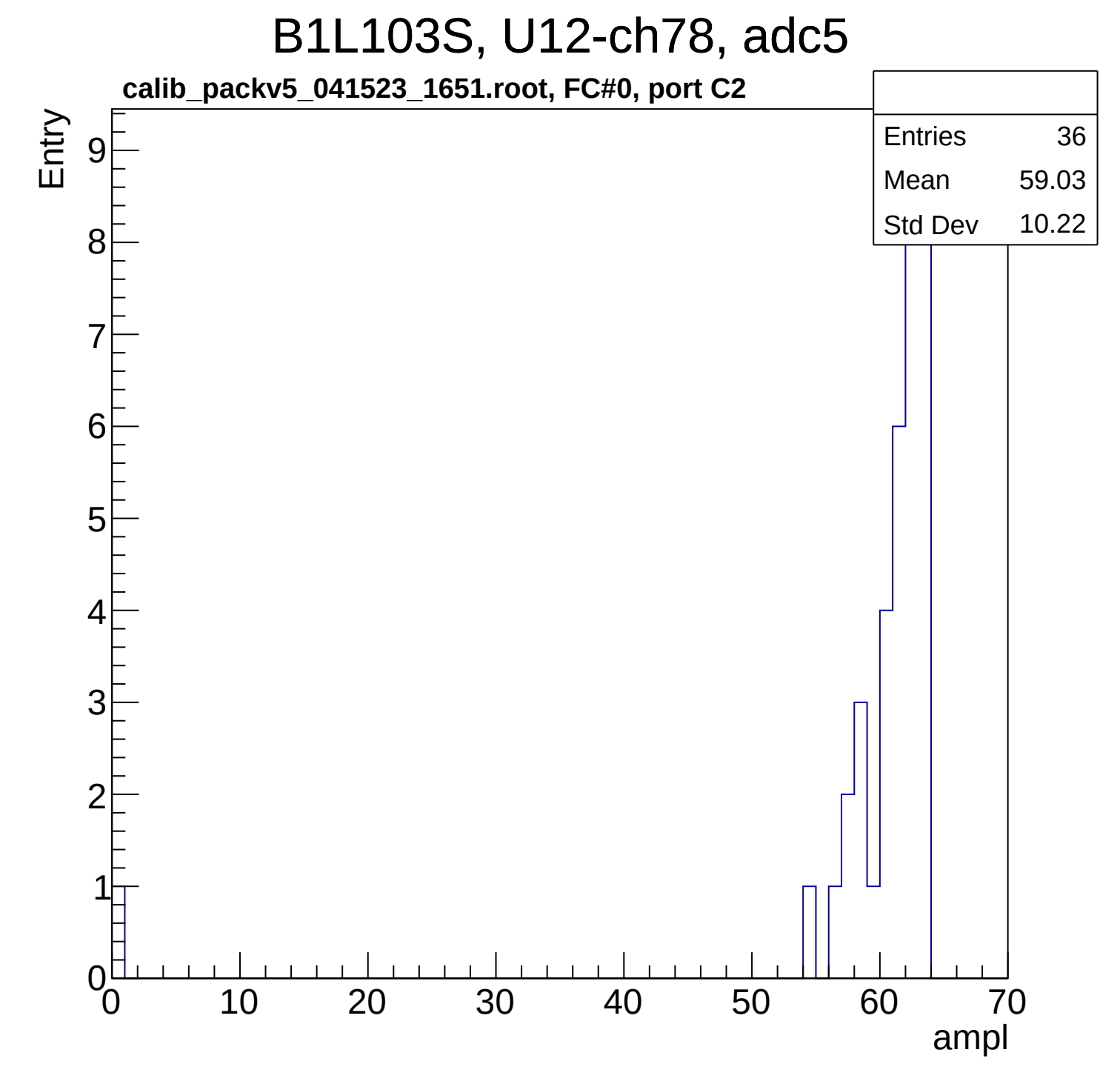
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U12-ch78, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 36
Mean 59.03
Std Dev 10.22
Entry
ampl
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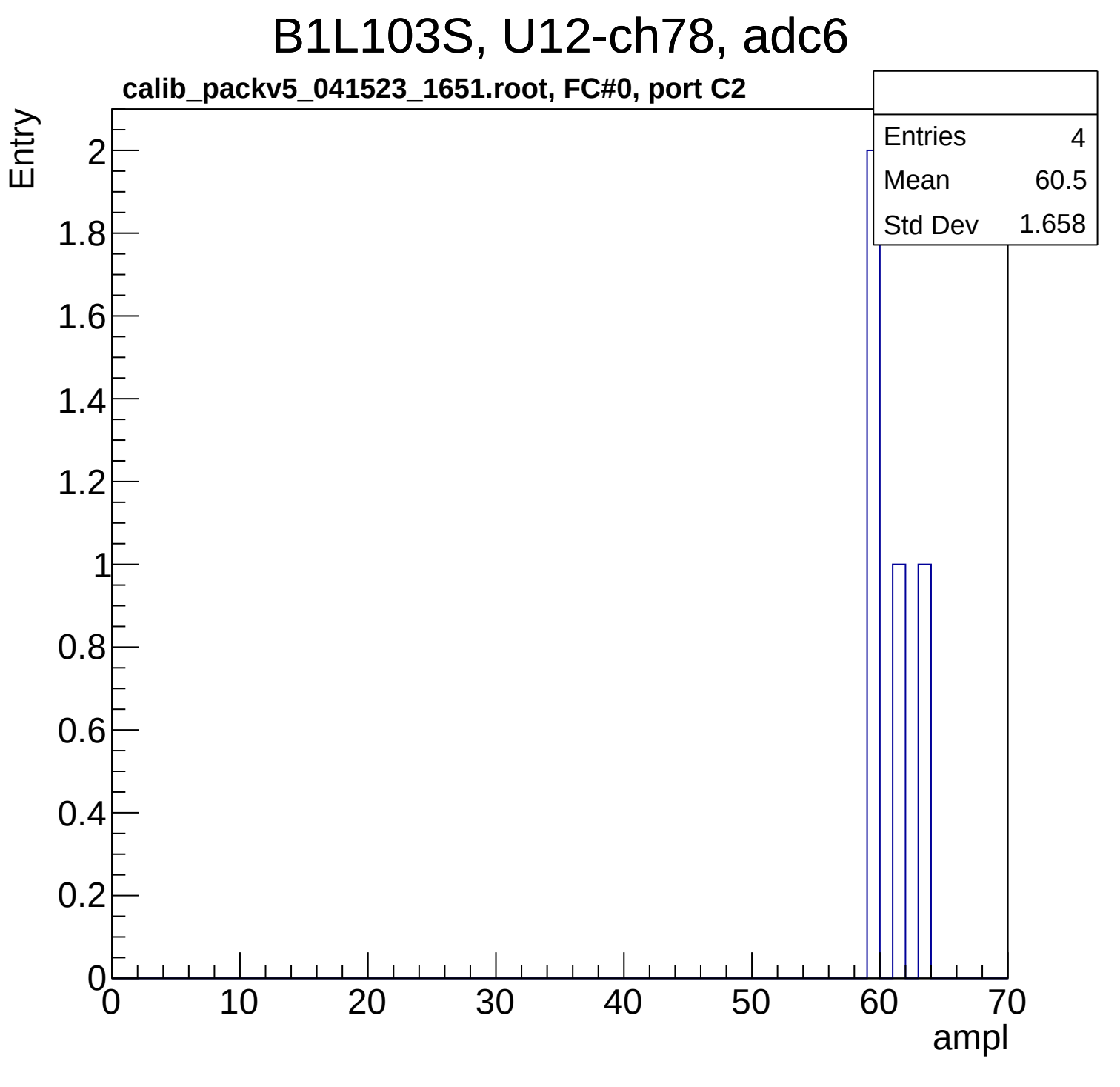
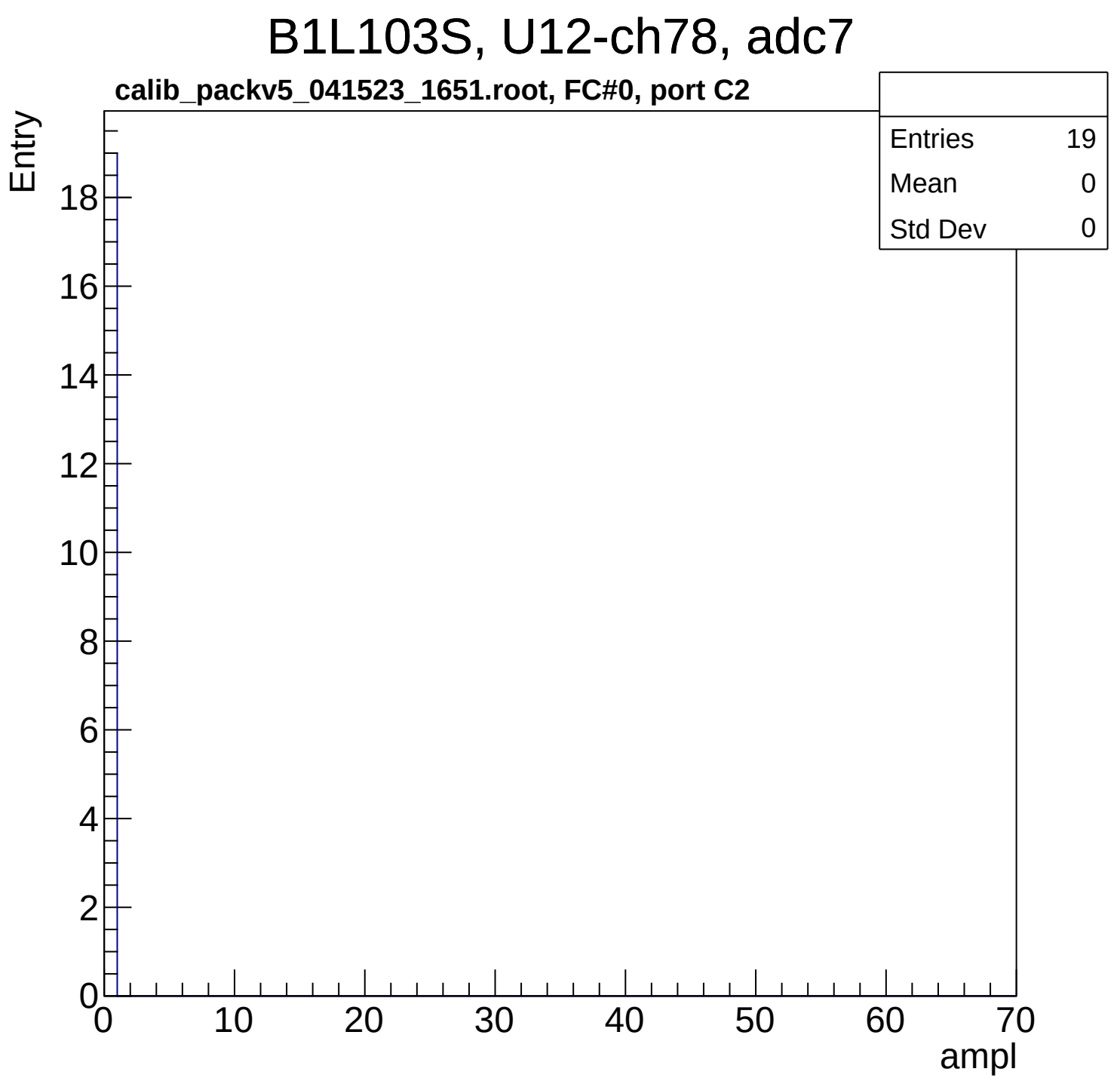
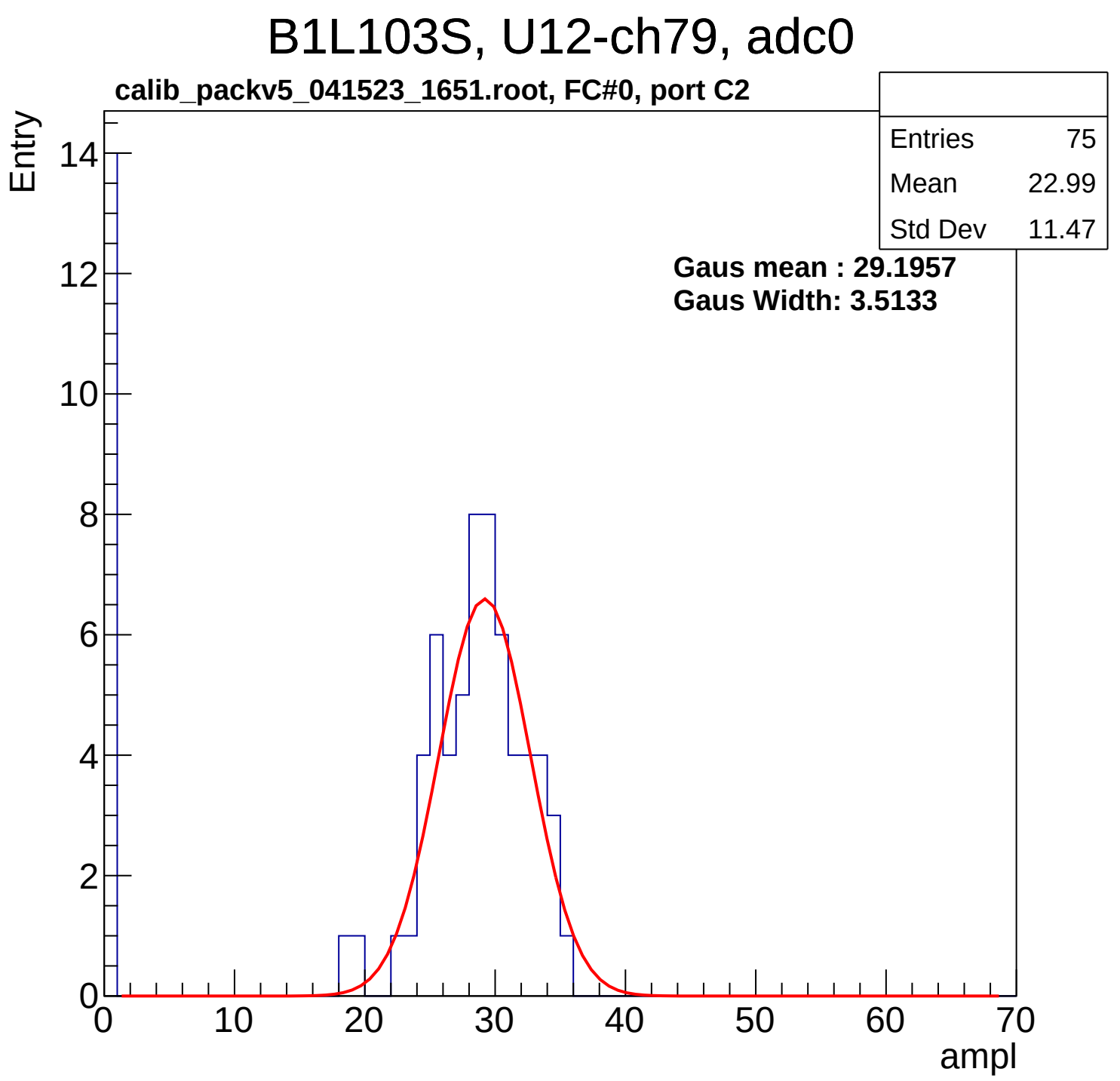
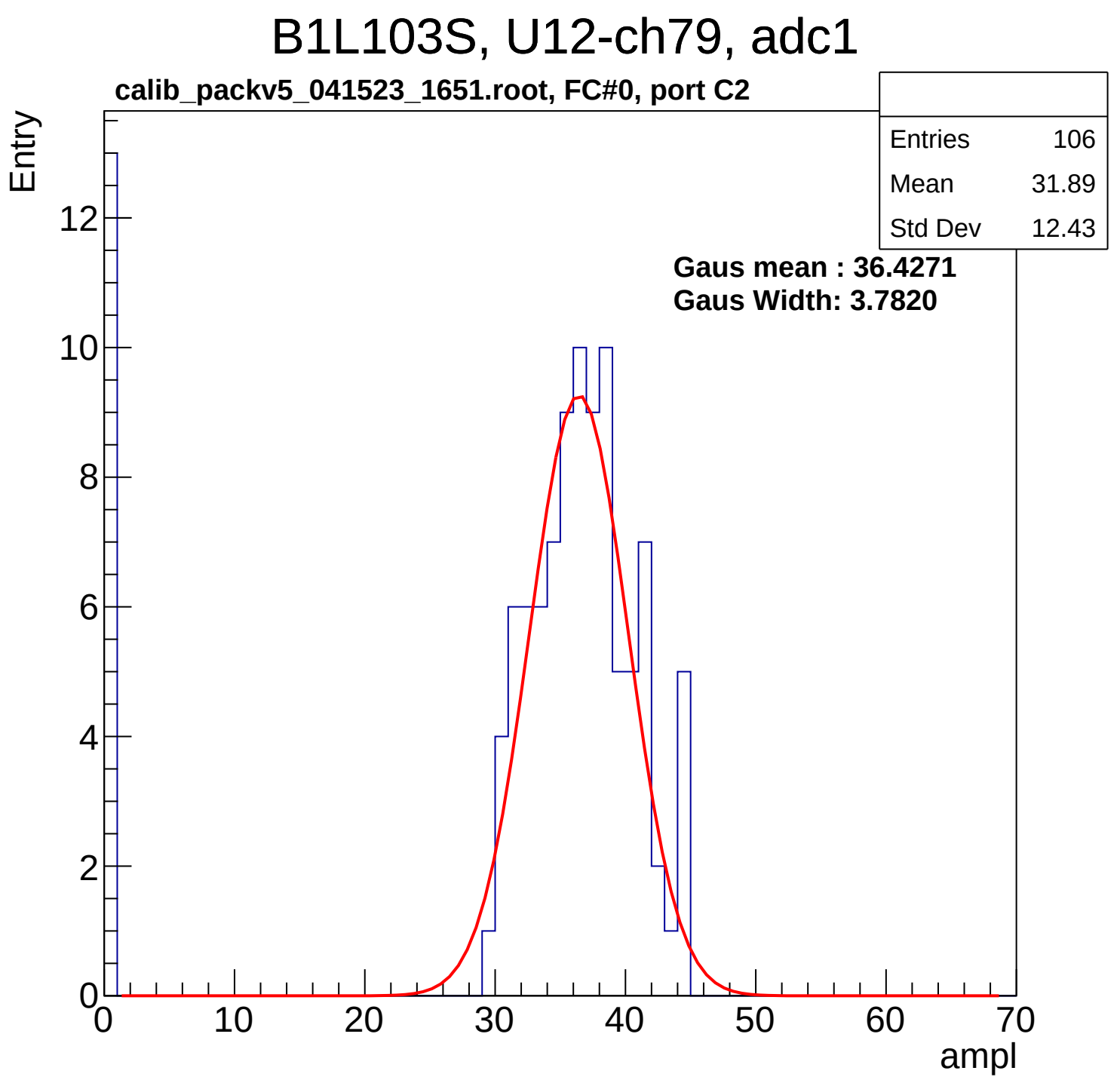
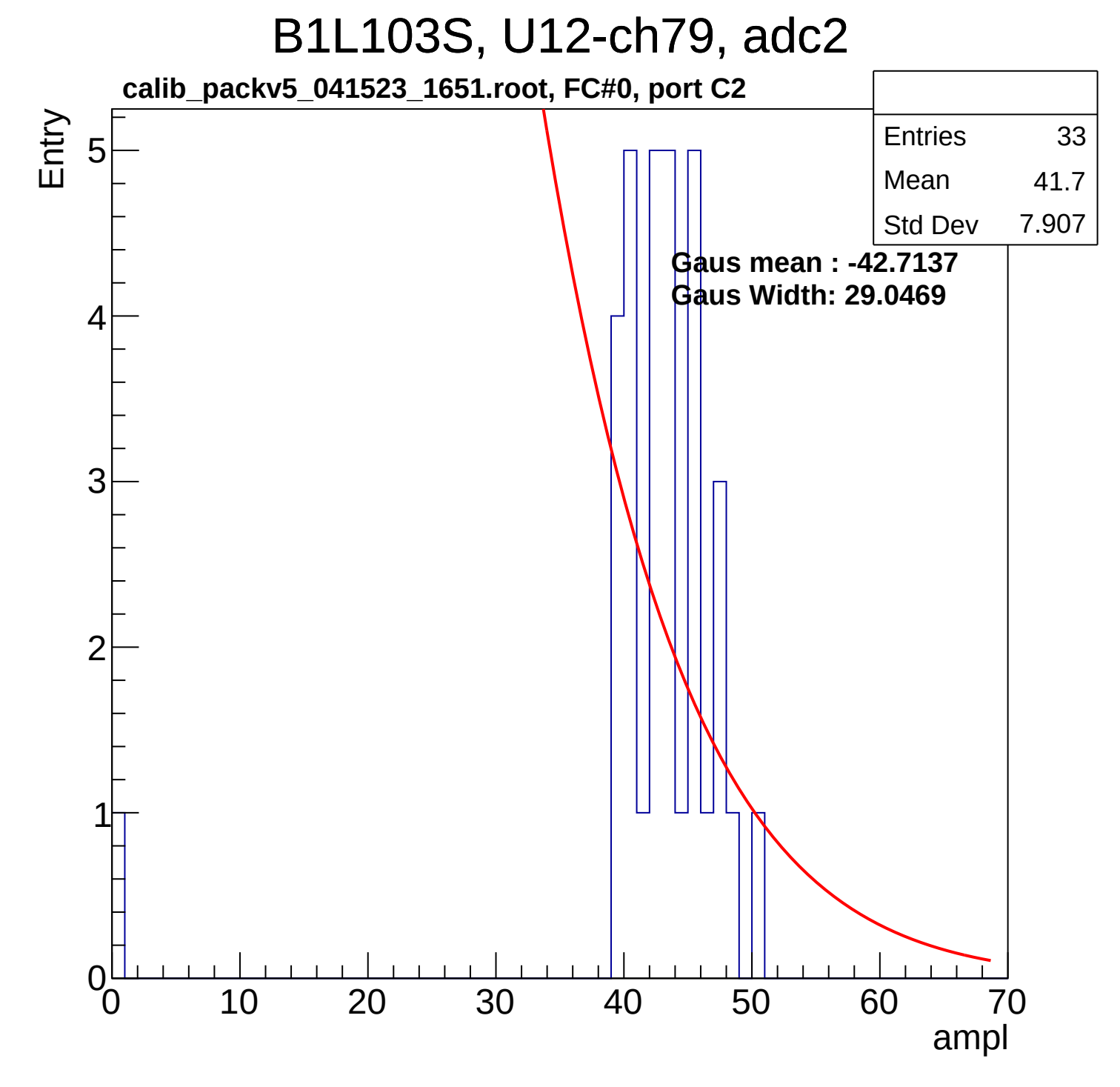
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

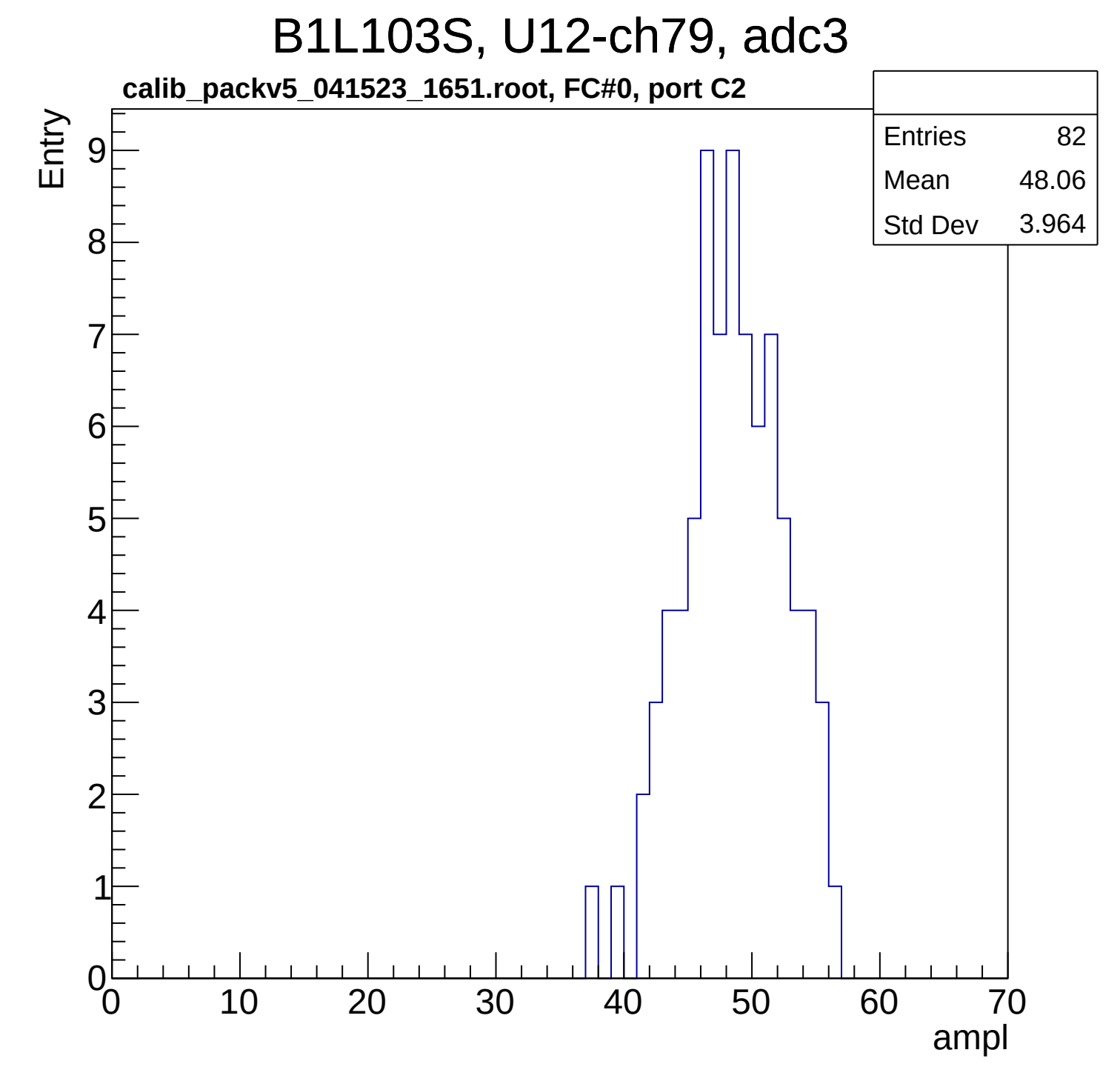

B1L103S, U12-ch78, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 60.5
Std Dev 1.658
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U12-ch78, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch79, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 22.99
Std Dev 11.47
Gaus mean : 29.1957
Gaus Width: 3.5133
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U12-ch79, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 106
Mean 31.89
Std Dev 12.43
Gaus mean : 36.4271
Gaus Width: 3.7820
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U12-ch79, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 33
Mean 41.7
Std Dev 7.907
Gaus mean : -42.7137
Gaus Width: 29.0469
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70


B1L103S, U12-ch79, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 48.06
Std Dev 3.964
Entry
ampl
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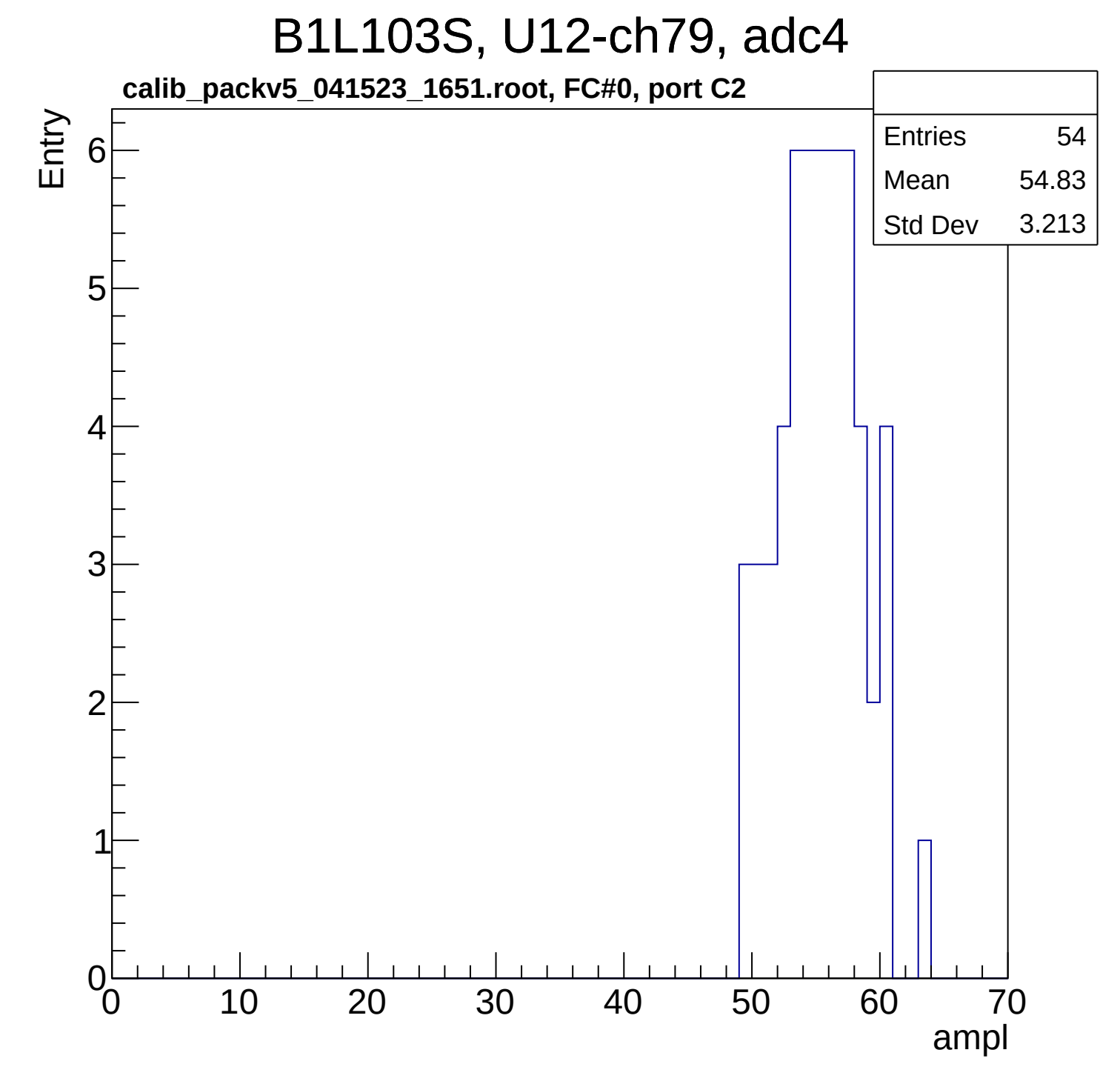
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch79, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 54.83
Std Dev 3.213
Entry
ampl
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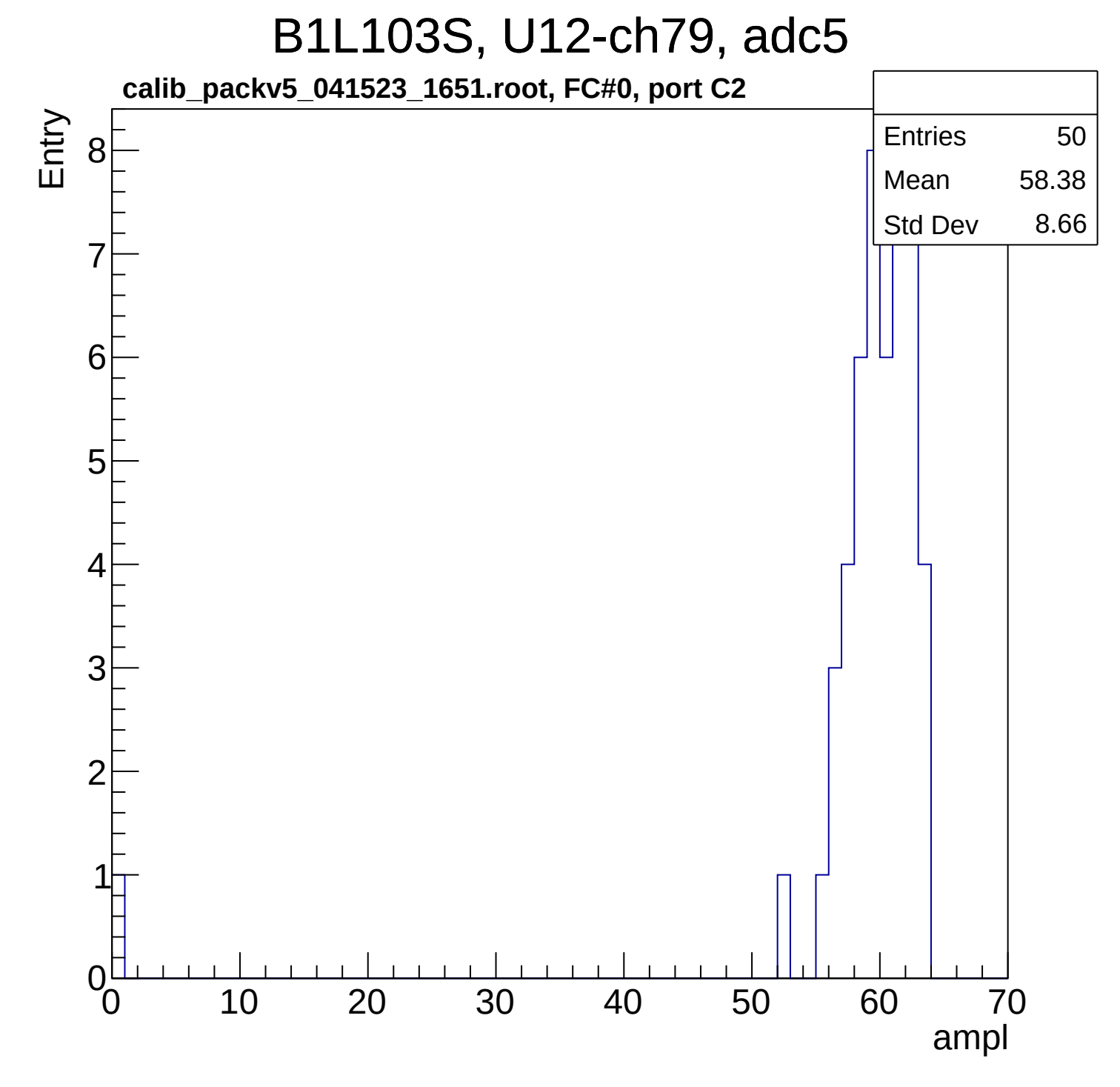
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U12-ch79, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.38
Std Dev 8.66
Entry
ampl
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1
2
3
4
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6
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0
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20
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40
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60
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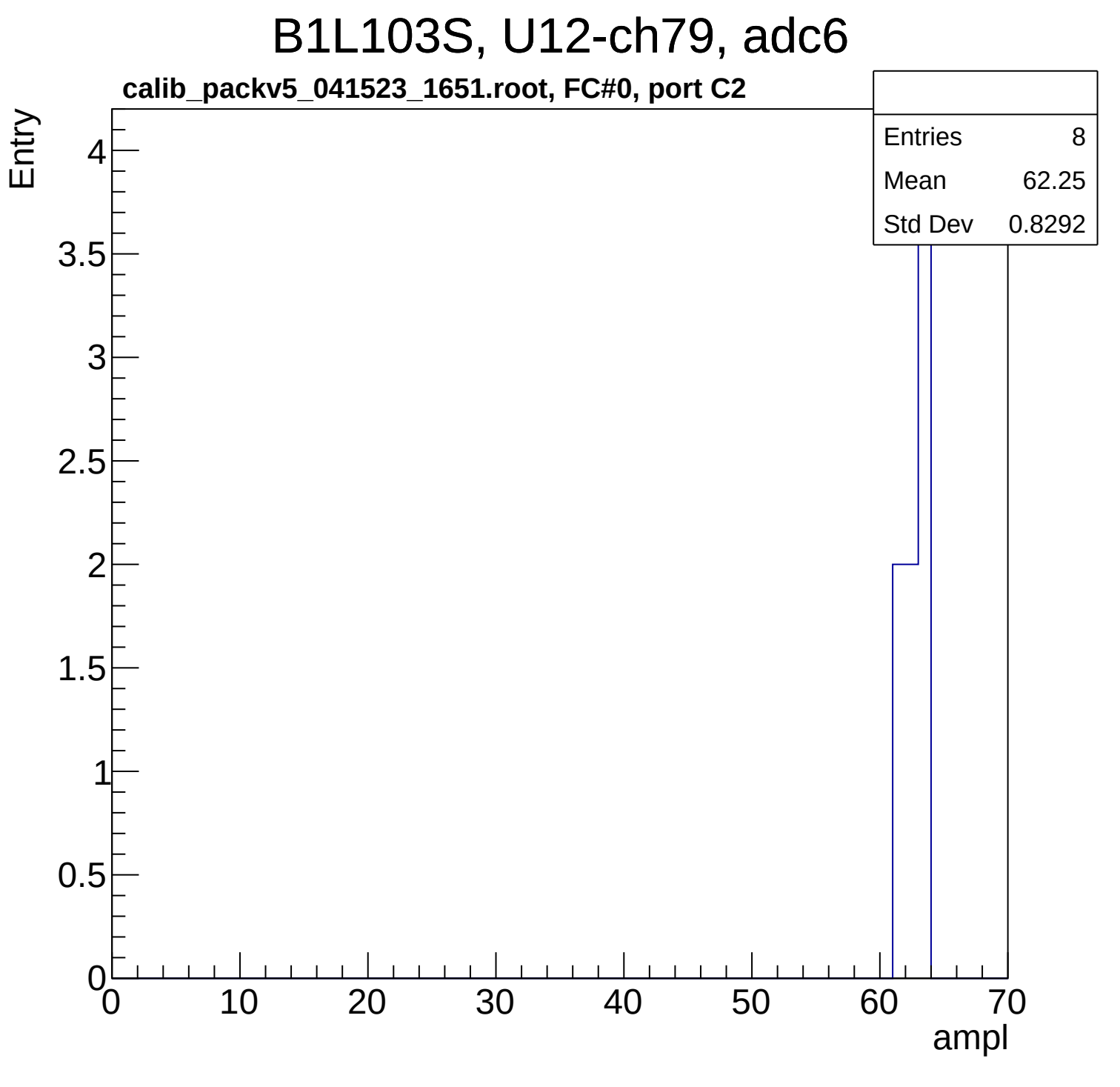
B1L103S, U12-ch79, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62.25
Std Dev 0.8292
Entry
ampl
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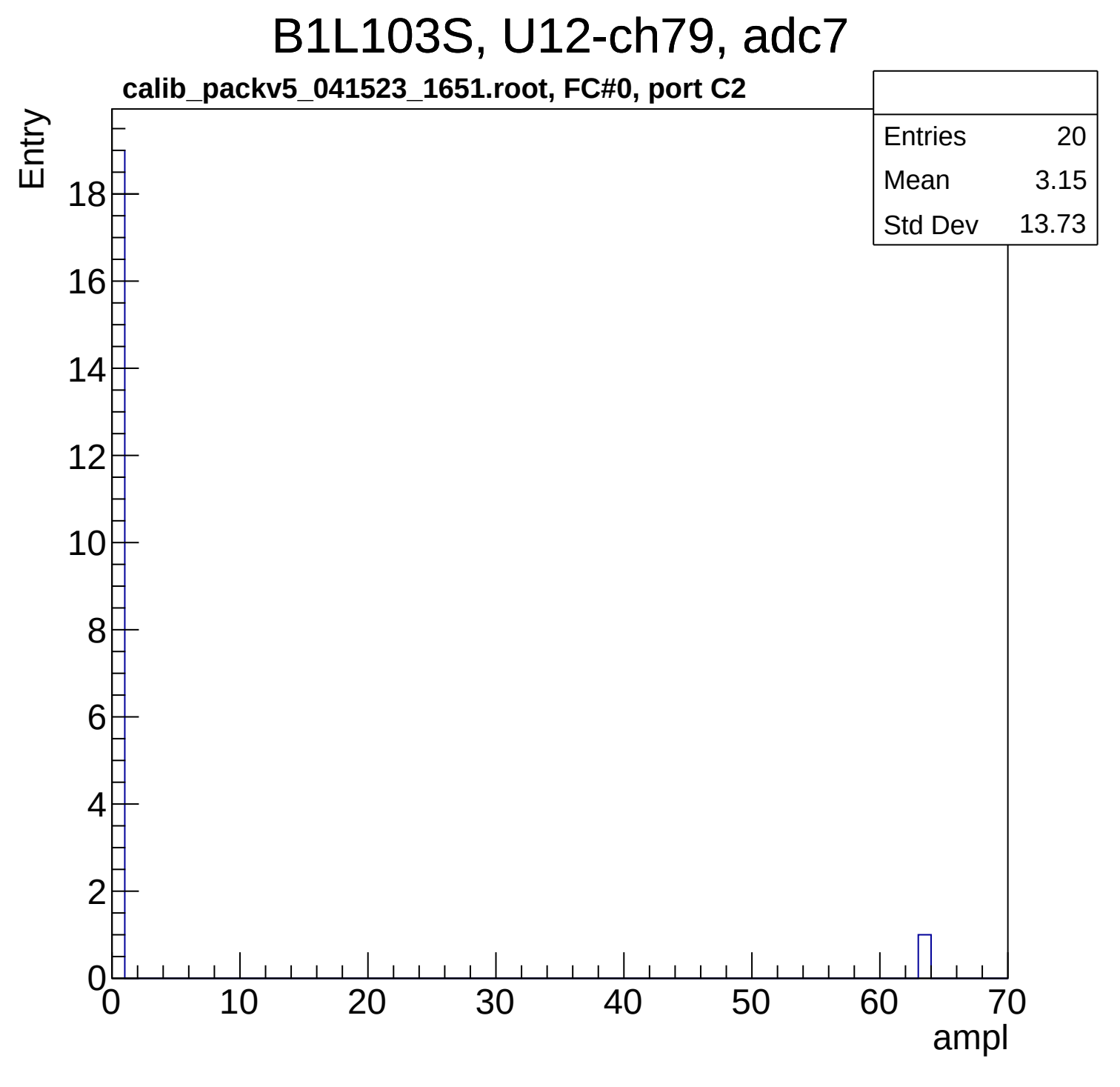
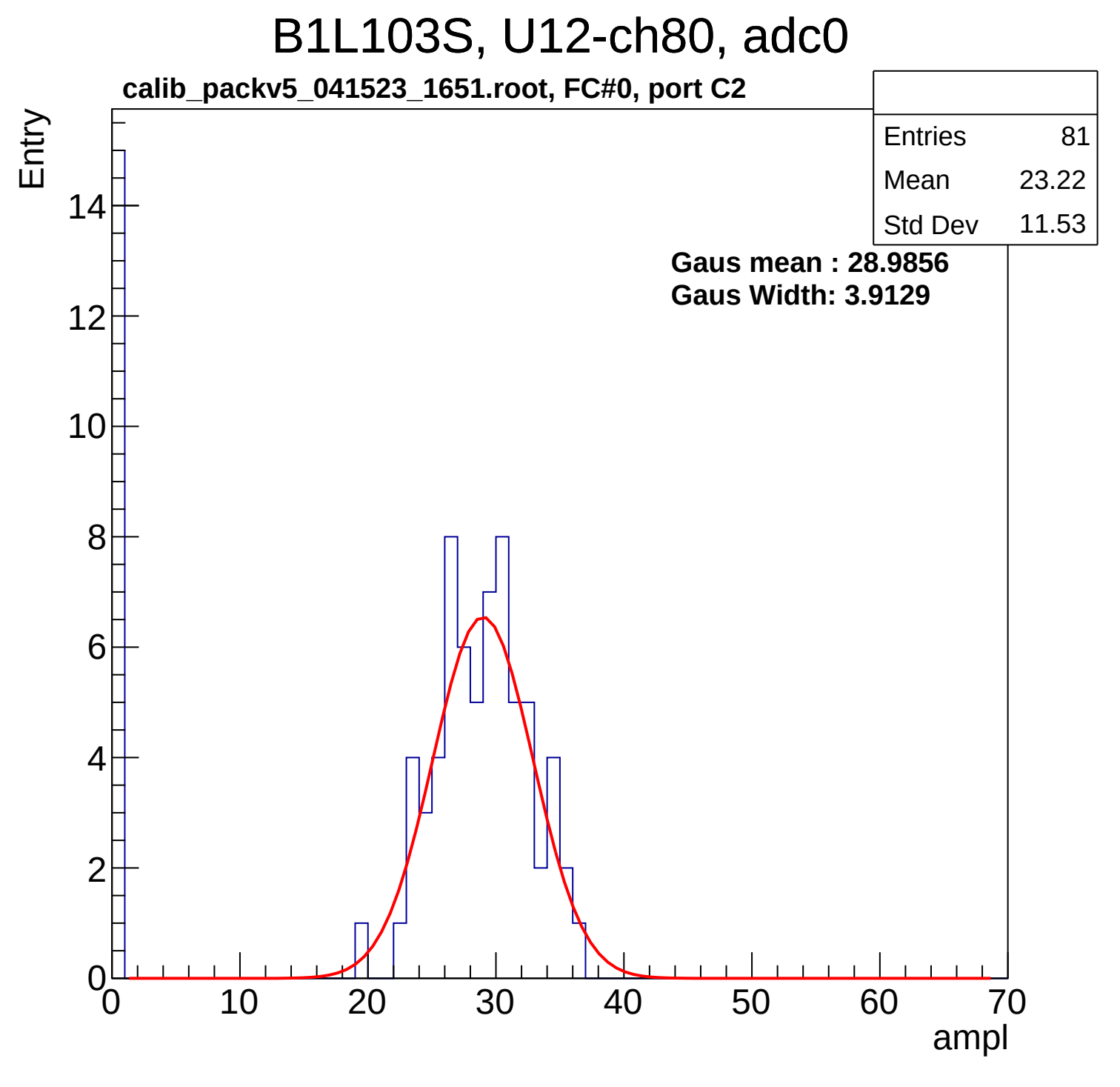
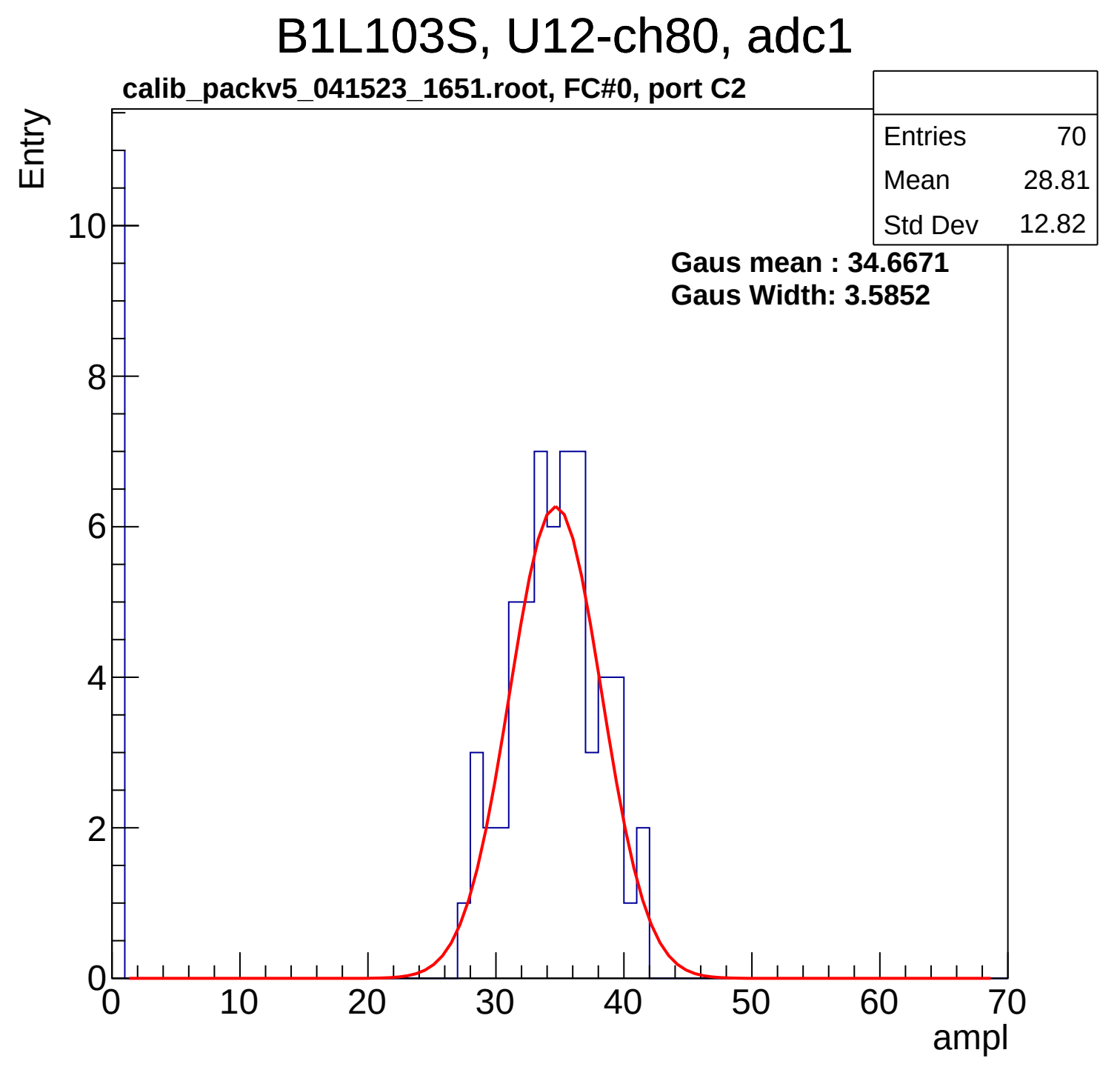
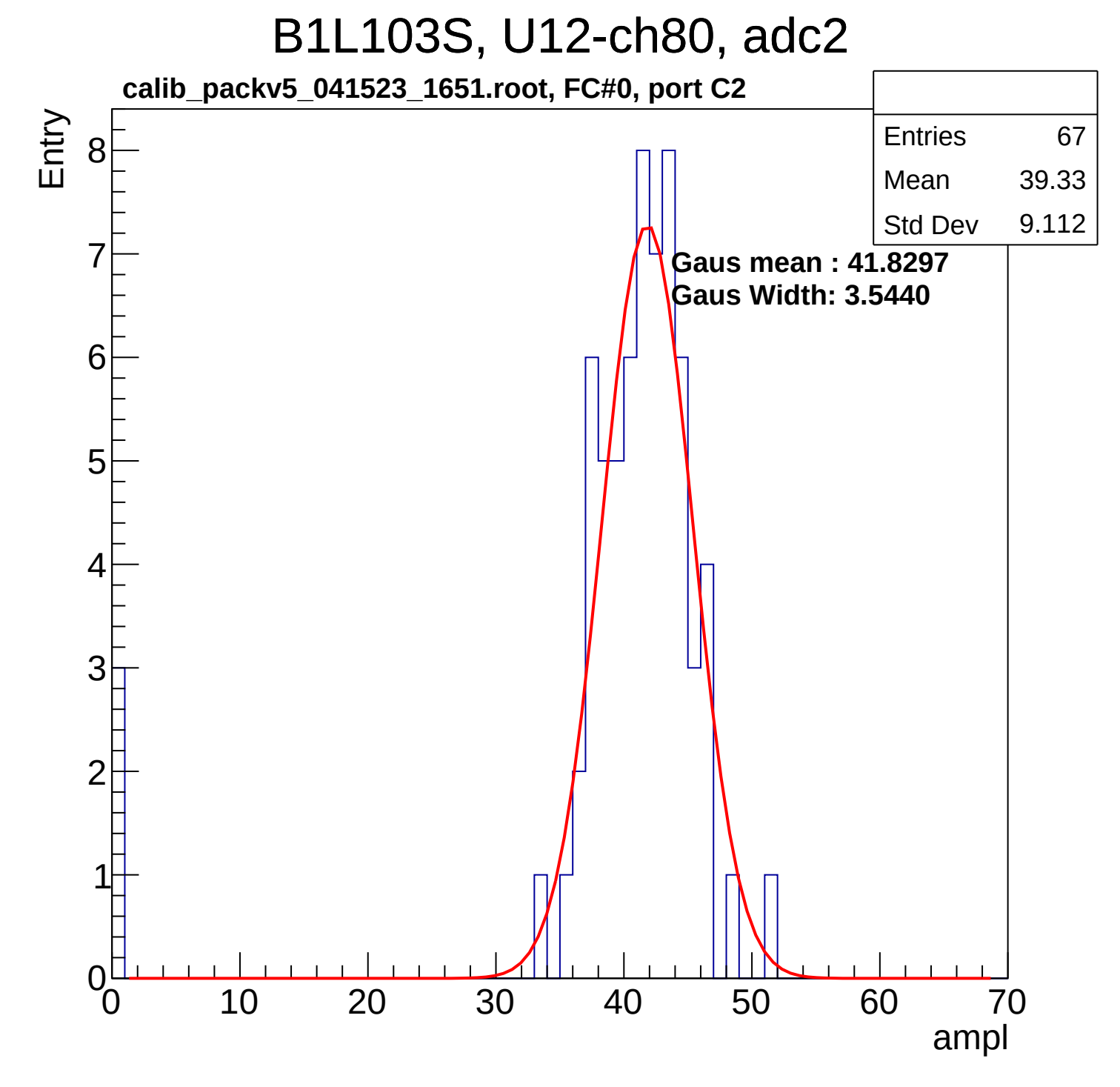
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U12-ch79, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch80, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 23.22
Std Dev 11.53
Gaus mean : 28.9856
Gaus Width: 3.9129
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U12-ch80, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 28.81
Std Dev 12.82
Gaus mean : 34.6671
Gaus Width: 3.5852
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch80, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 39.33
Std Dev 9.112
Gaus mean : 41.8297
Gaus Width: 3.5440
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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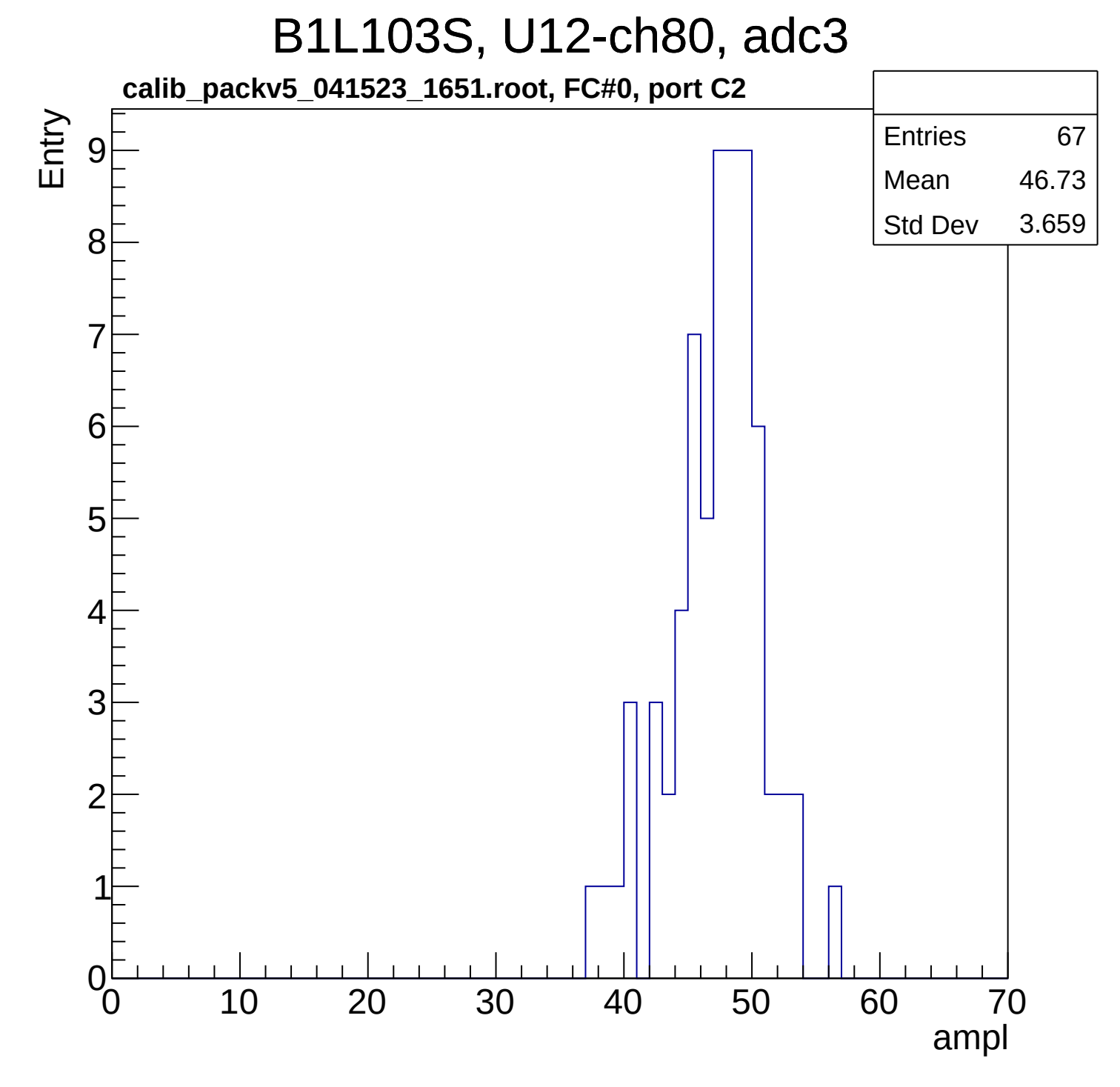
B1L103S, U12-ch80, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 46.73
Std Dev 3.659
Entry
ampl
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3
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5
6
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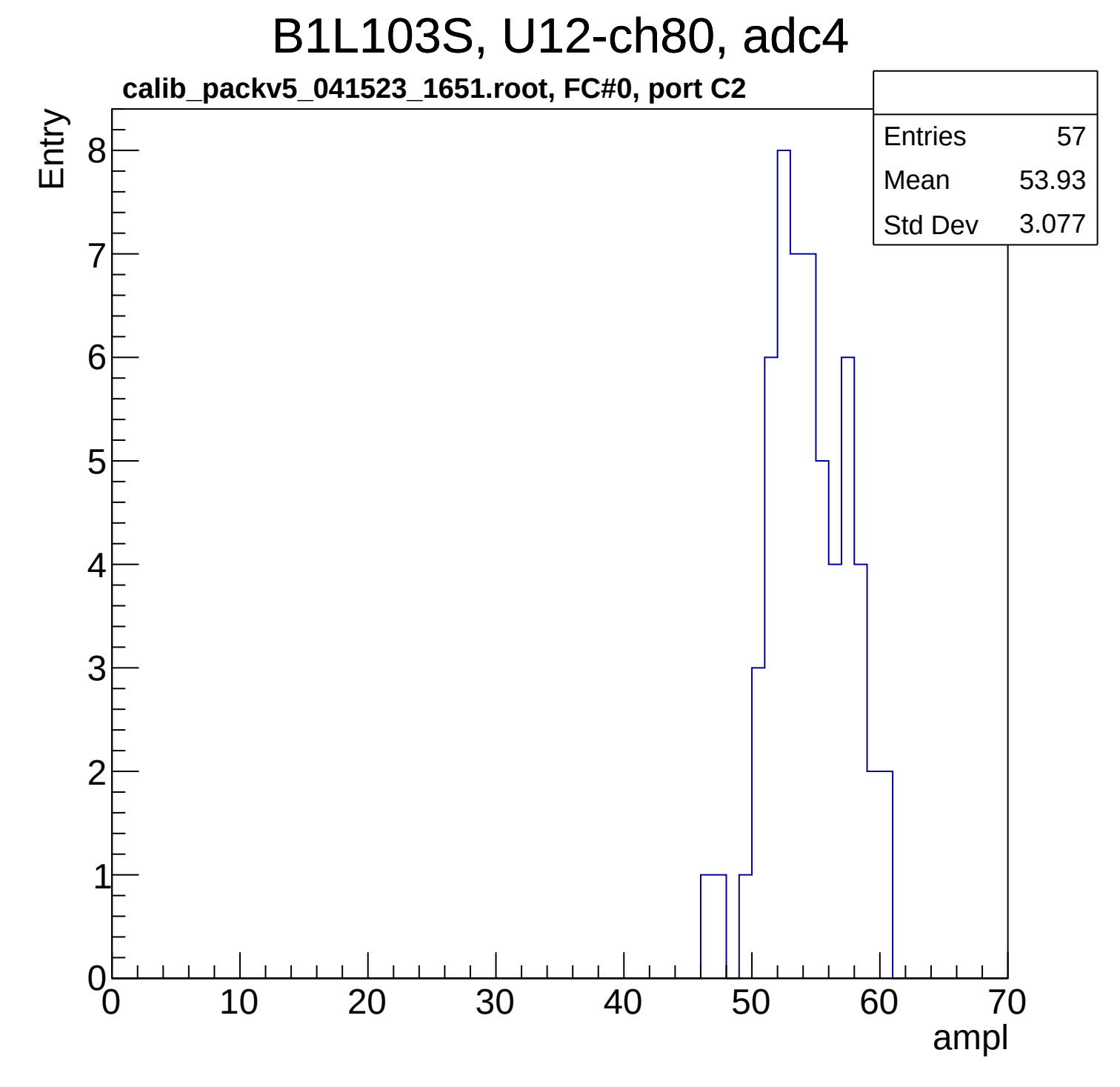
B1L103S, U12-ch80, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 53.93
Std Dev 3.077
Entry
ampl
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2
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4
5
6
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0
10
20
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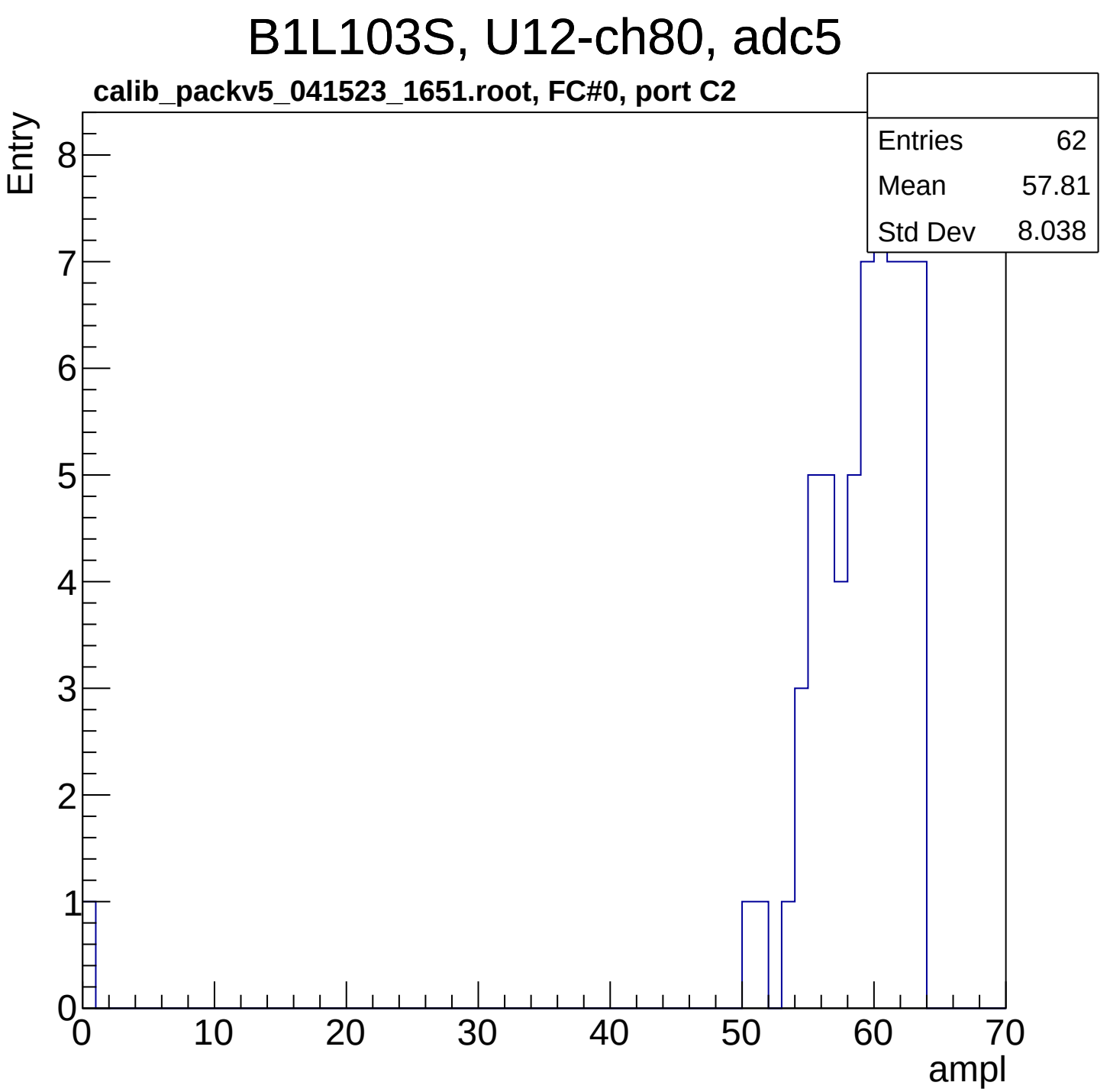
40
50
60
70


B1L103S, U12-ch80, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 57.81
Std Dev 8.038
Entry
ampl
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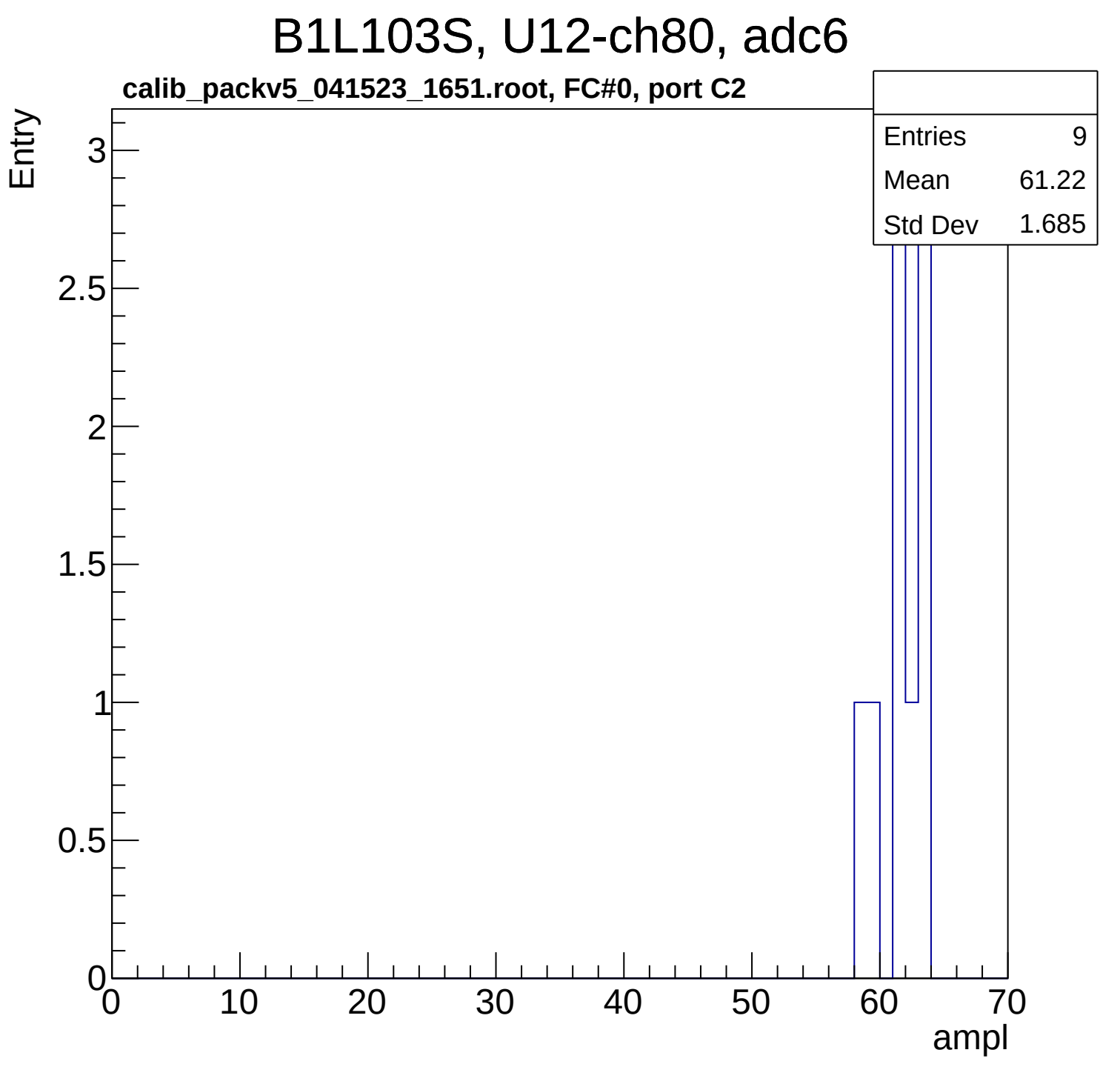
B1L103S, U12-ch80, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.22
Std Dev 1.685
Entry
ampl
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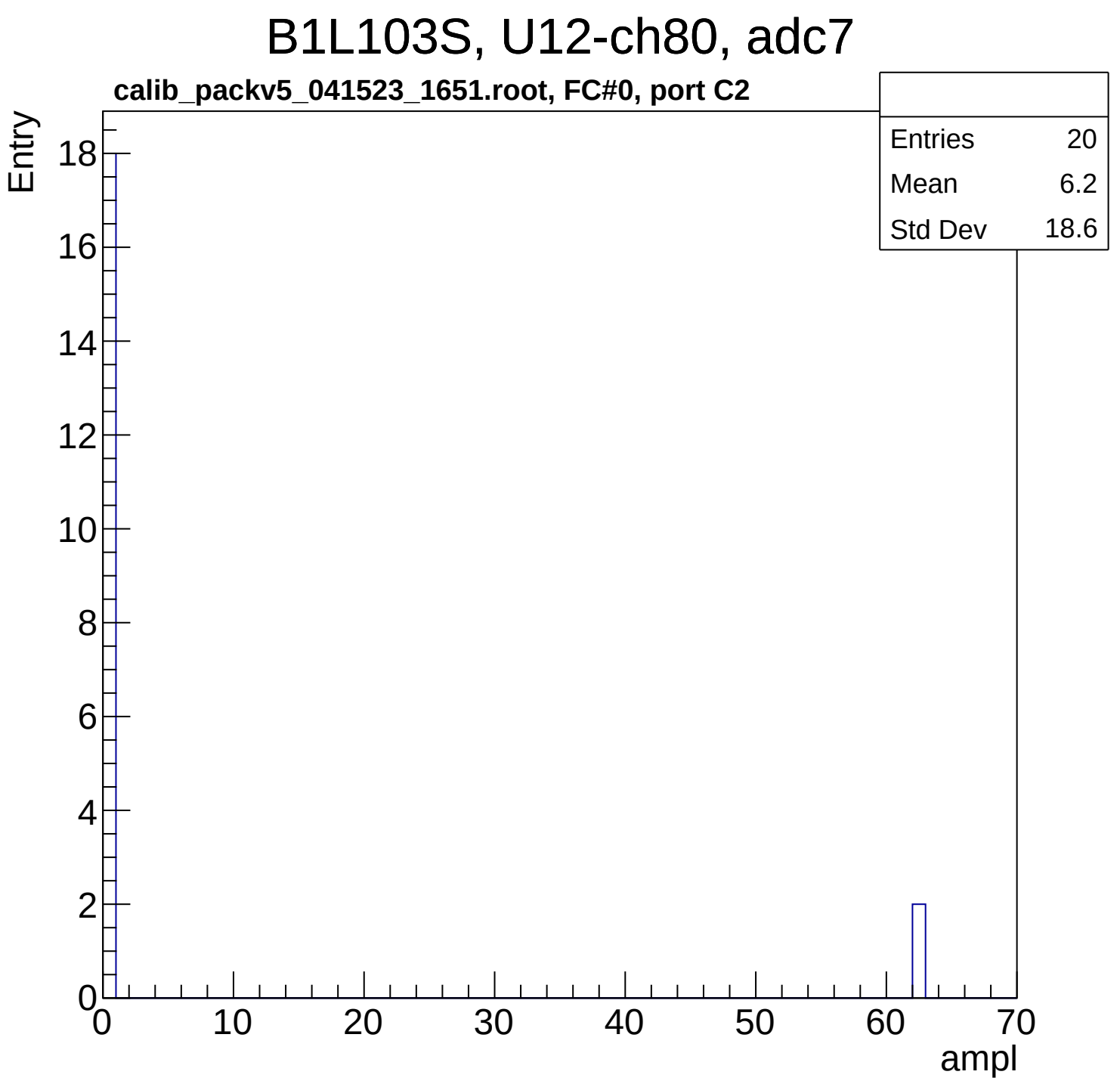
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U12-ch80, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.2
Std Dev 18.6
Entry
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6
8
10
12
14
16
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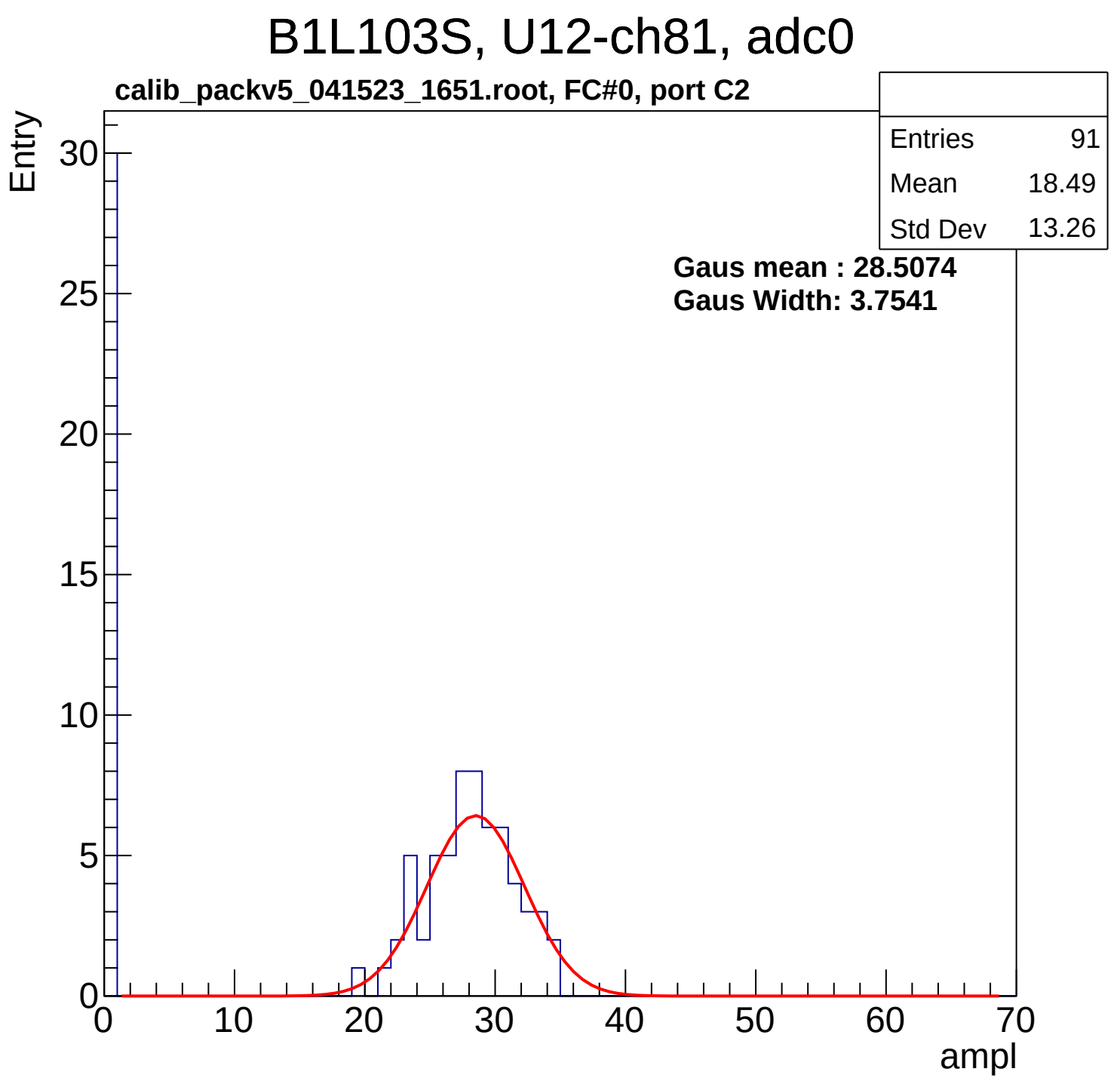
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch81, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 18.49
Std Dev 13.26
Gaus mean : 28.5074
Gaus Width: 3.7541
Entry
ampl
0
5
10
15
20
25
30
0
10
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40
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60
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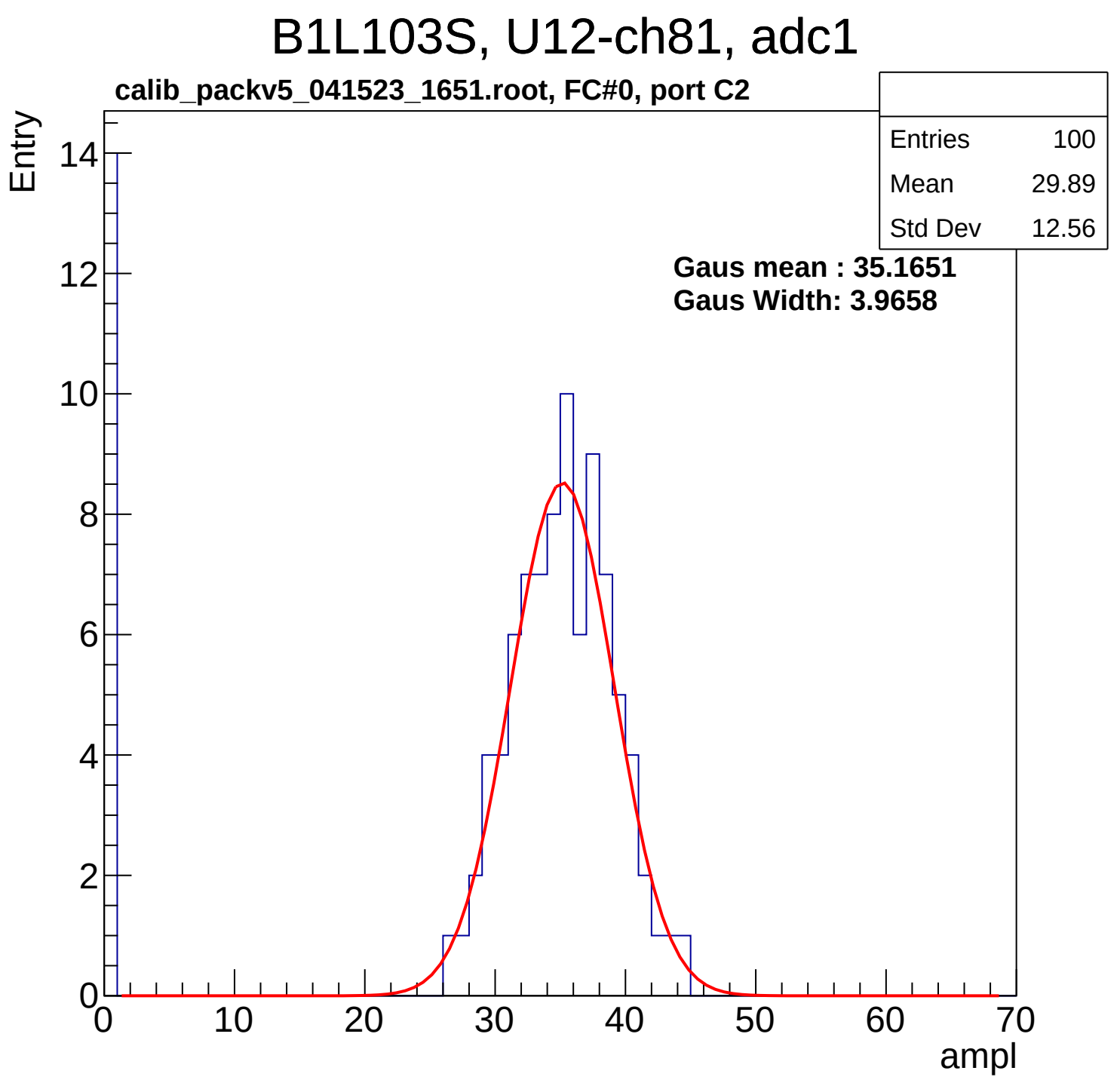
B1L103S, U12-ch81, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 29.89
Std Dev 12.56
Gaus mean : 35.1651
Gaus Width: 3.9658
Entry
ampl
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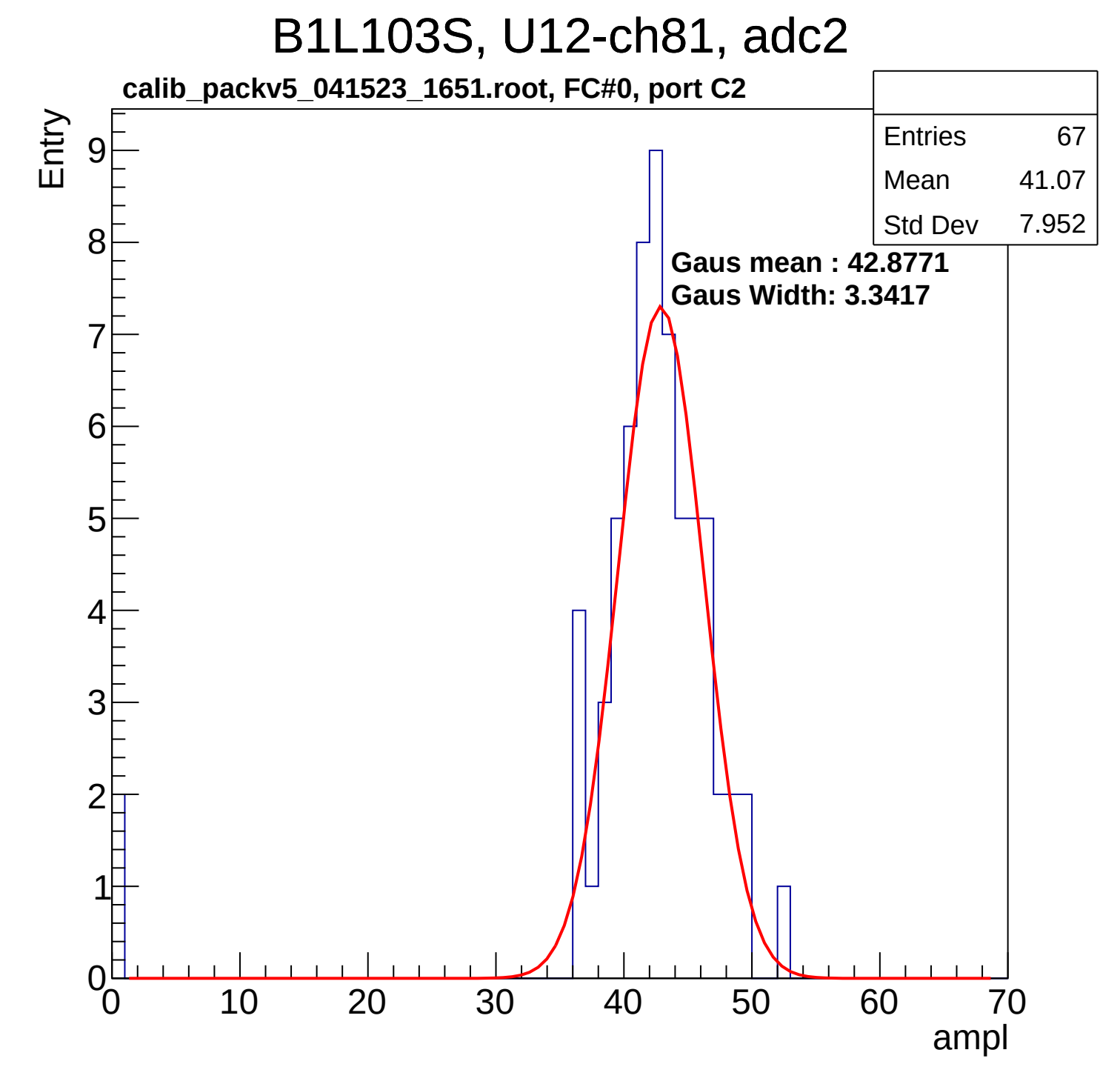
B1L103S, U12-ch81, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 41.07
Std Dev 7.952
Gaus mean : 42.8771
Gaus Width: 3.3417
Entry
ampl
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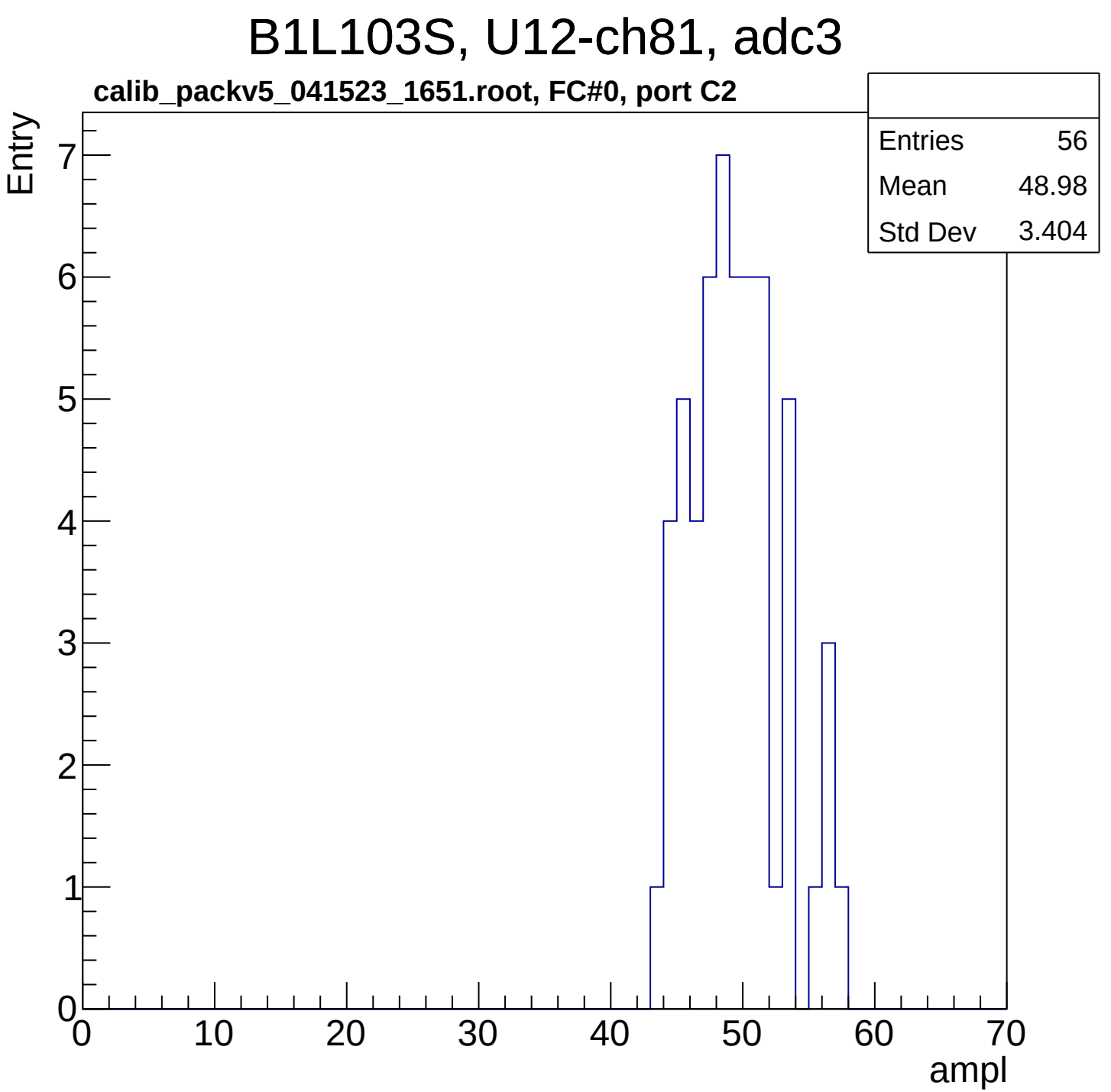
B1L103S, U12-ch81, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 48.98
Std Dev 3.404
Entry
ampl
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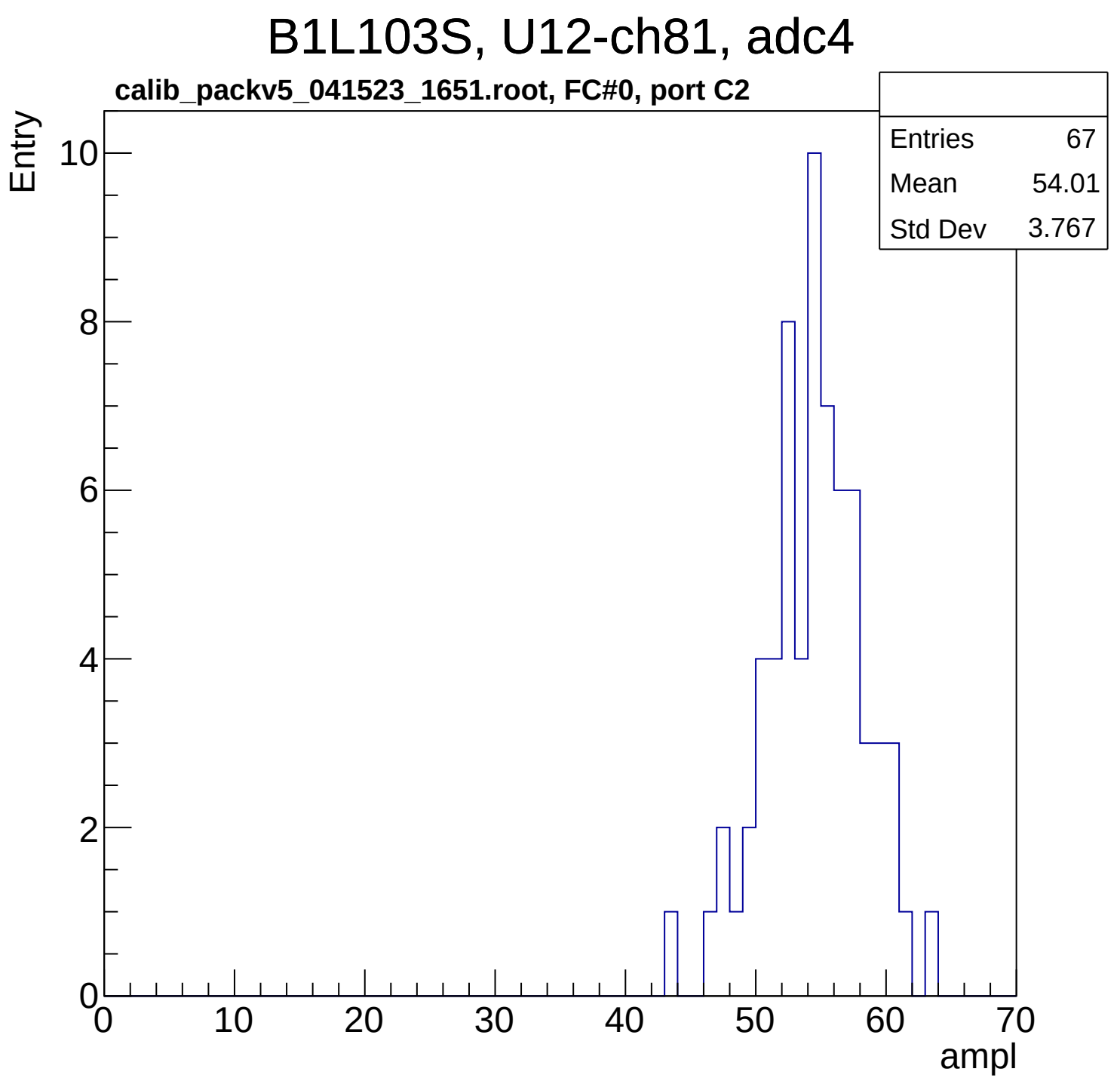
B1L103S, U12-ch81, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 54.01
Std Dev 3.767
Entry
ampl
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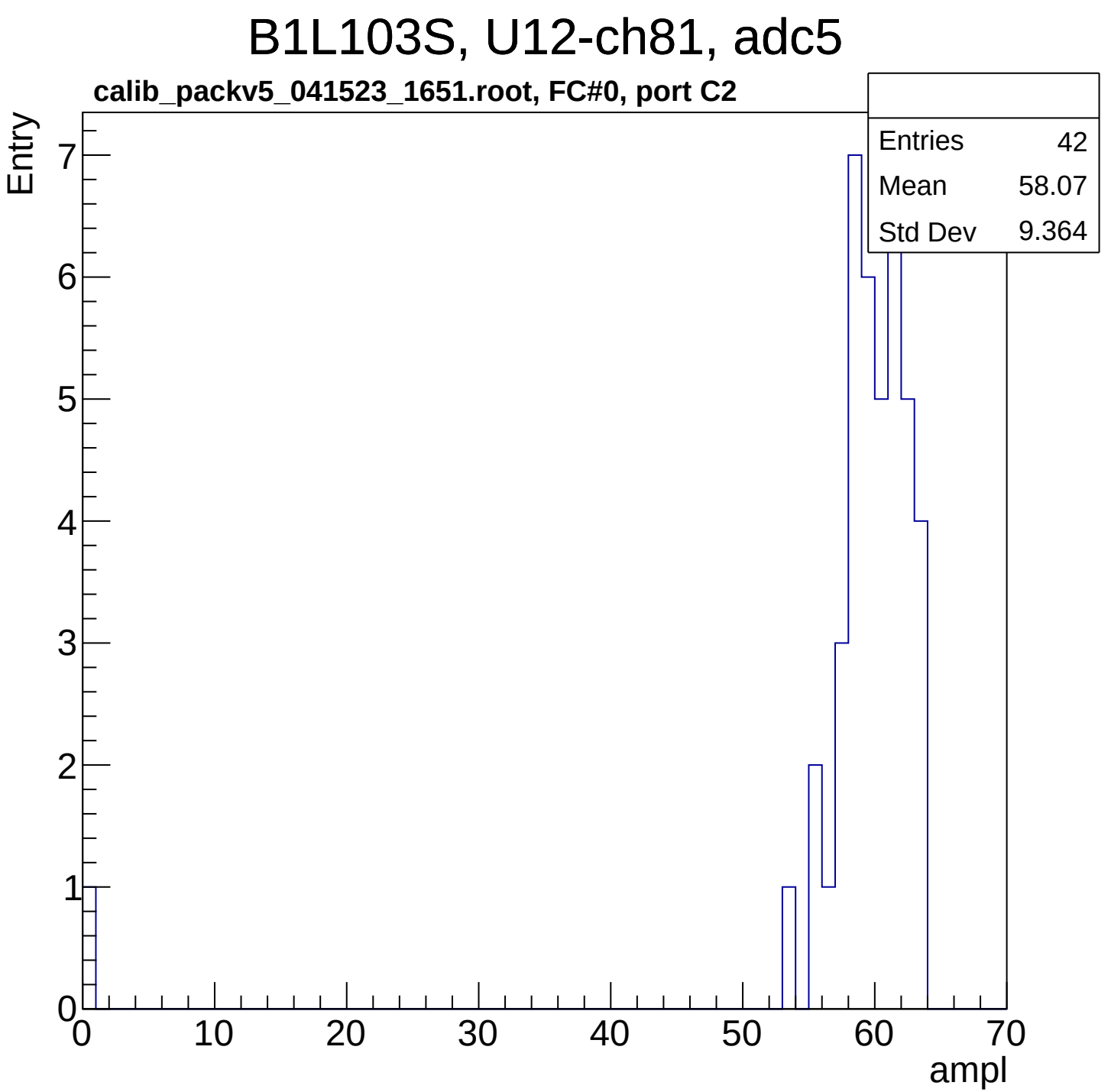
B1L103S, U12-ch81, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 58.07
Std Dev 9.364
Entry
ampl
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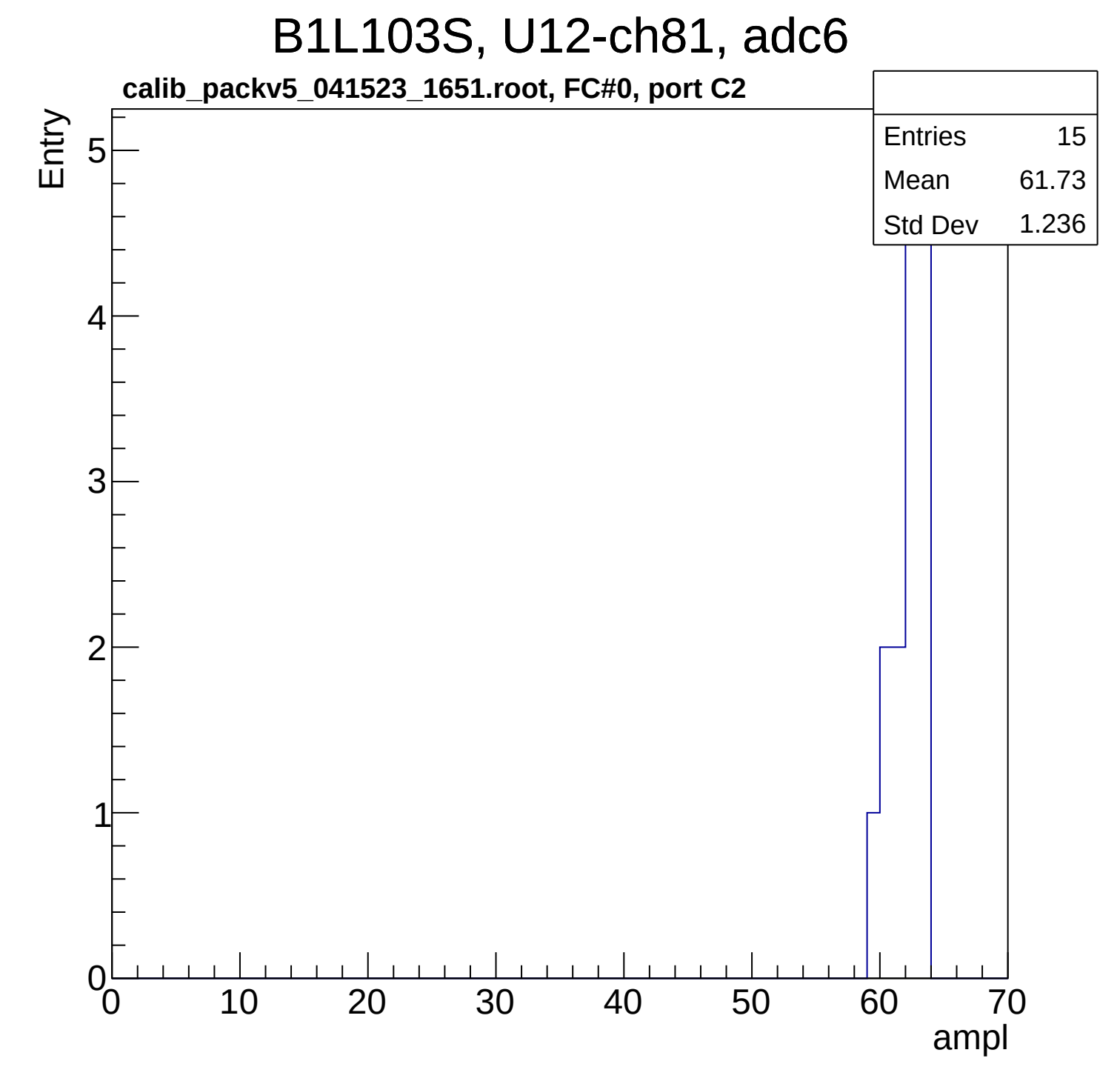
B1L103S, U12-ch81, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.73
Std Dev 1.236
Entry
ampl
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0
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60
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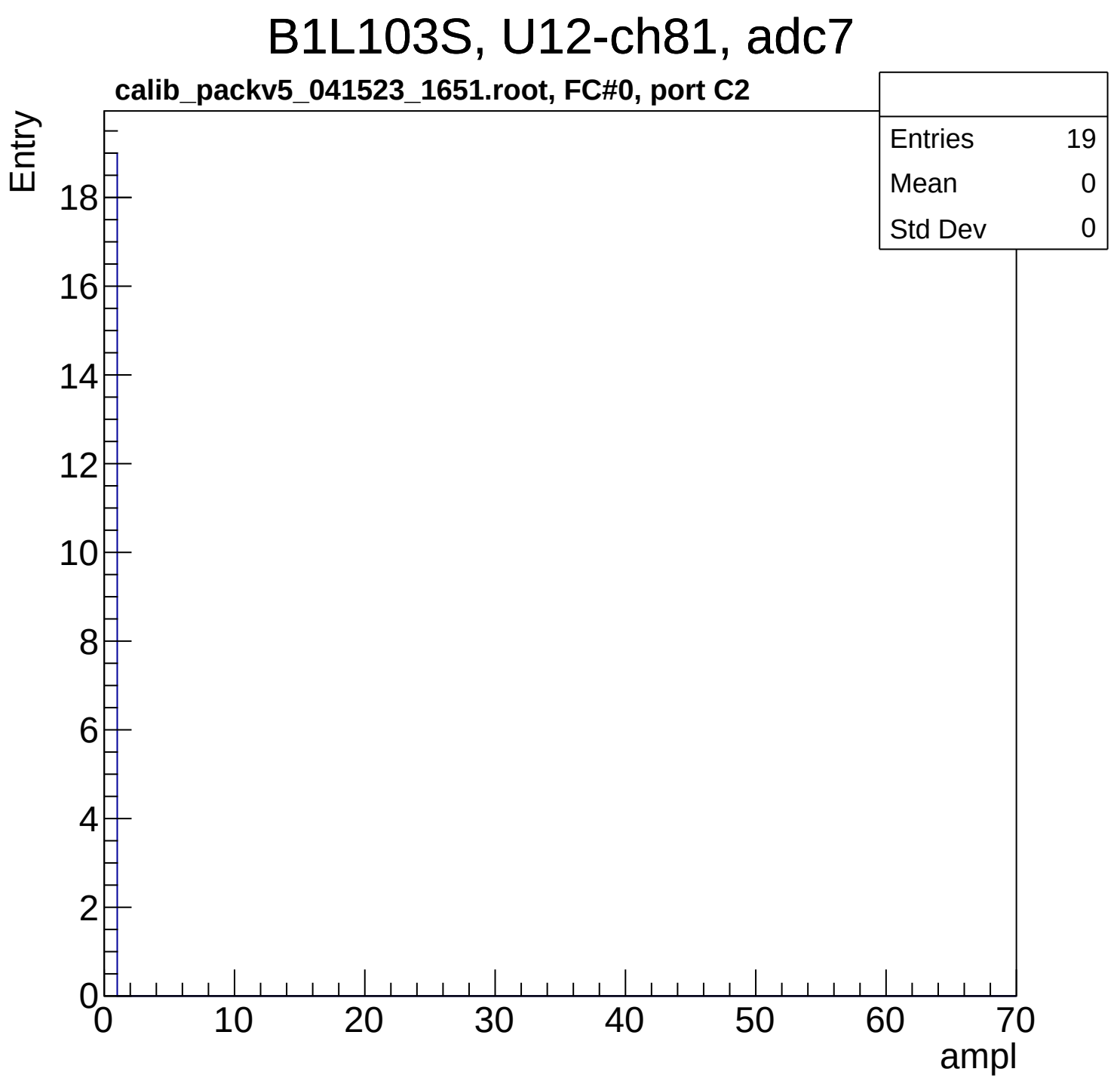
B1L103S, U12-ch81, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
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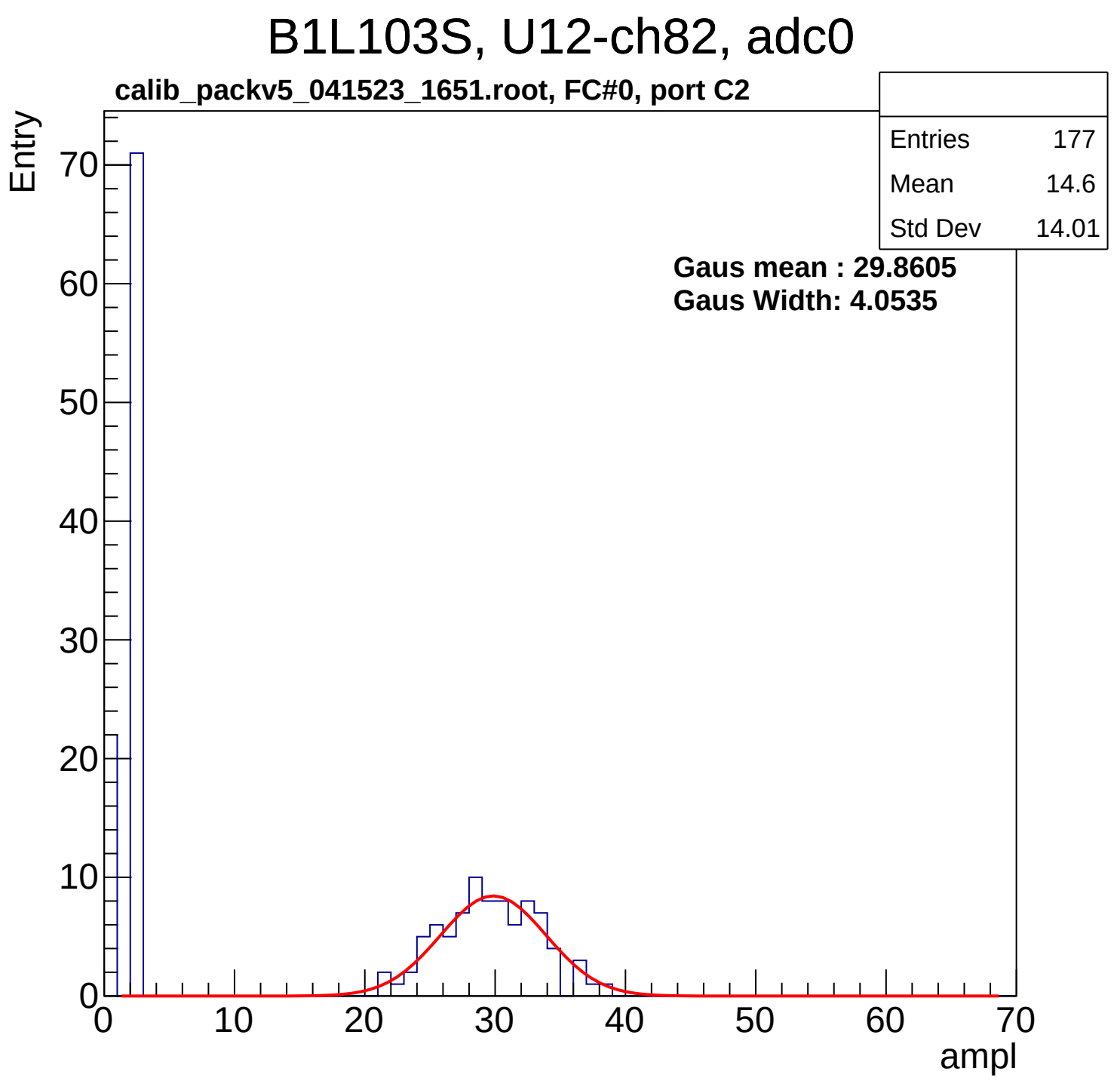
50
60
70
ampl


B1L103S, U12-ch82, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 177
Mean 14.6
Std Dev 14.01
Gaus mean : 29.8605
Gaus Width: 4.0535
Entry
ampl
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10
20
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40
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60
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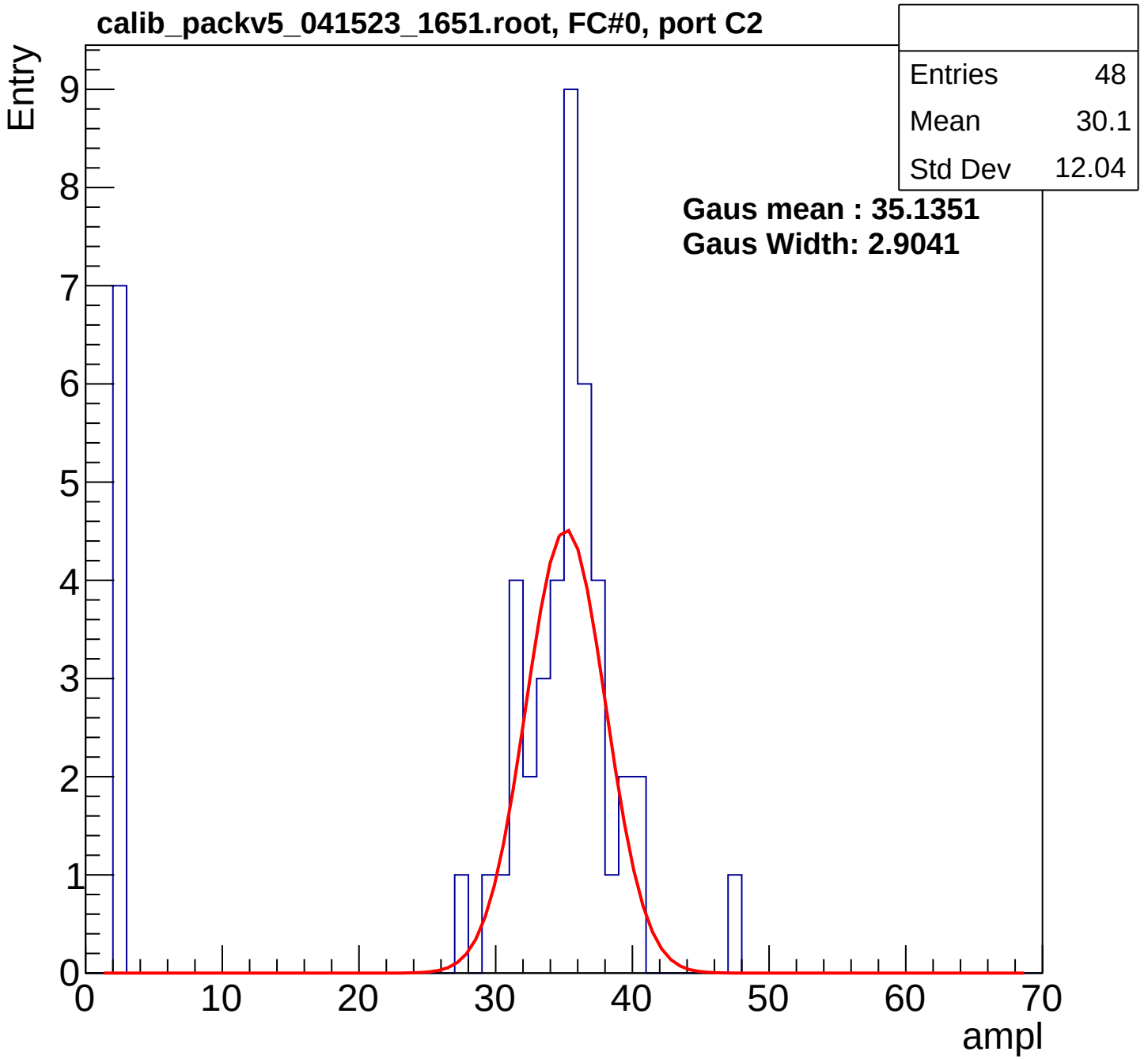
B1L103S, U12-ch82, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 30.1
Std Dev 12.04
Gaus mean : 35.1351
Gaus Width: 2.9041
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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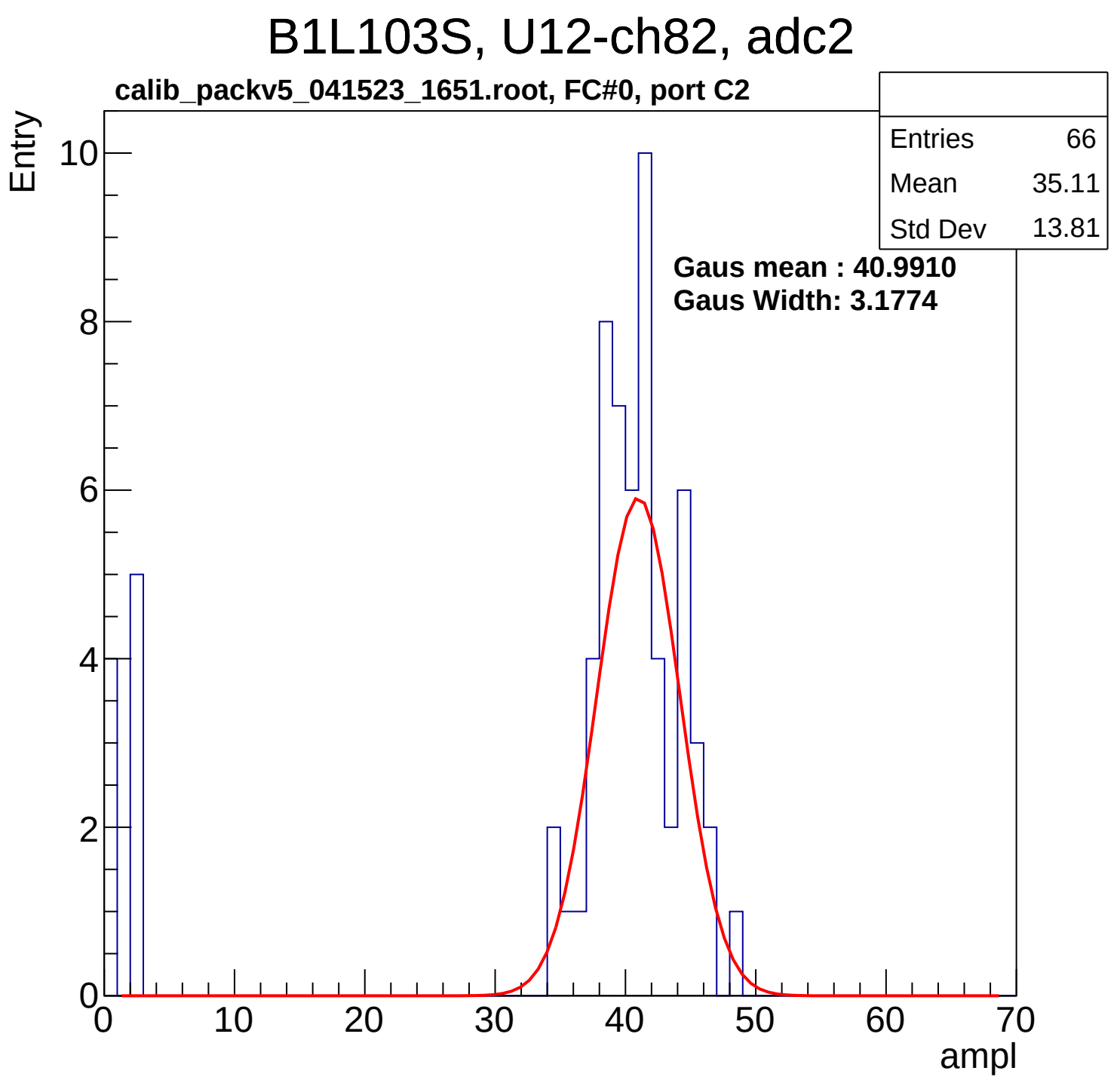
B1L103S, U12-ch82, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 35.11
Std Dev 13.81
Gaus mean : 40.9910
Gaus Width: 3.1774
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
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60
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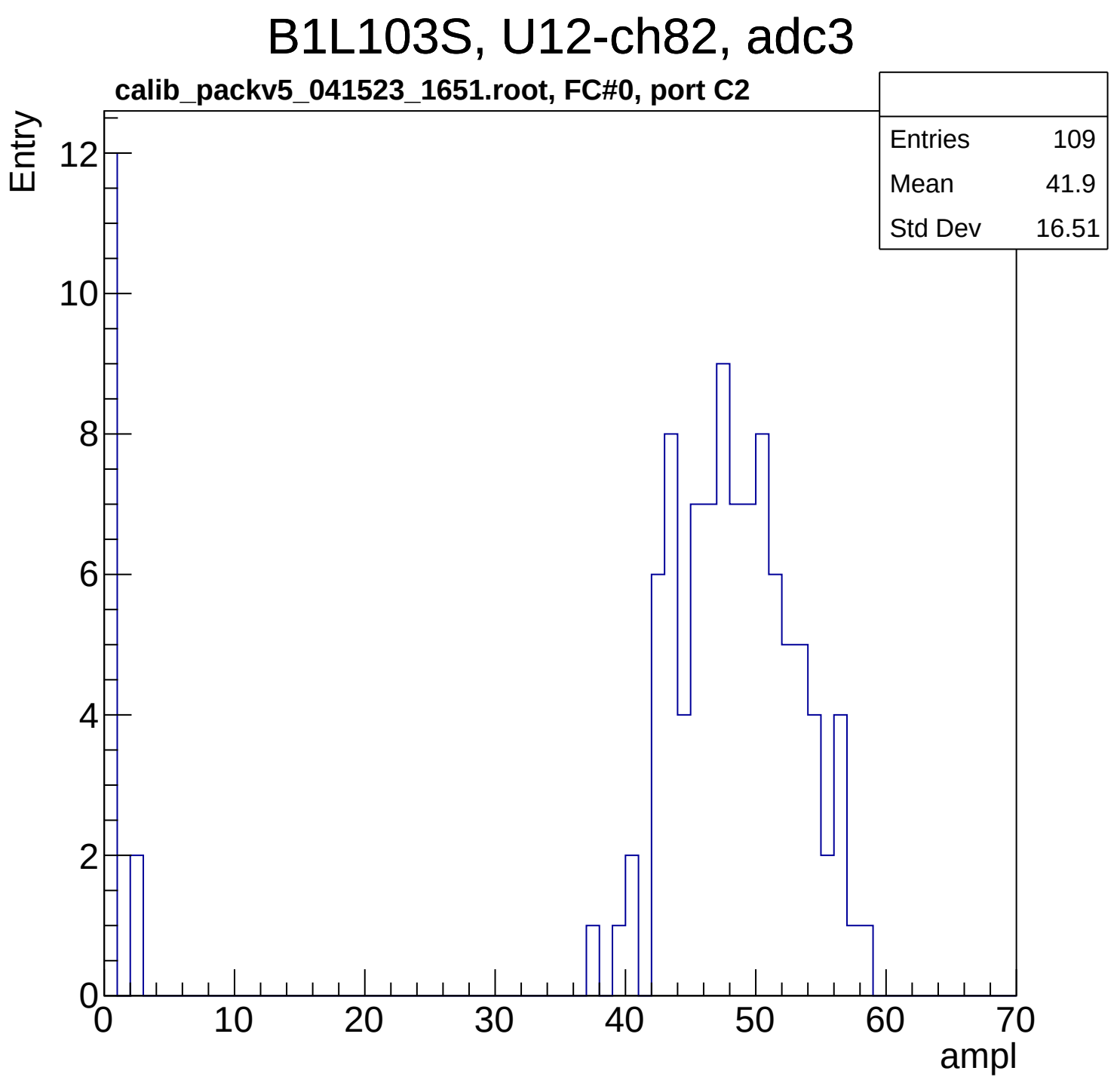
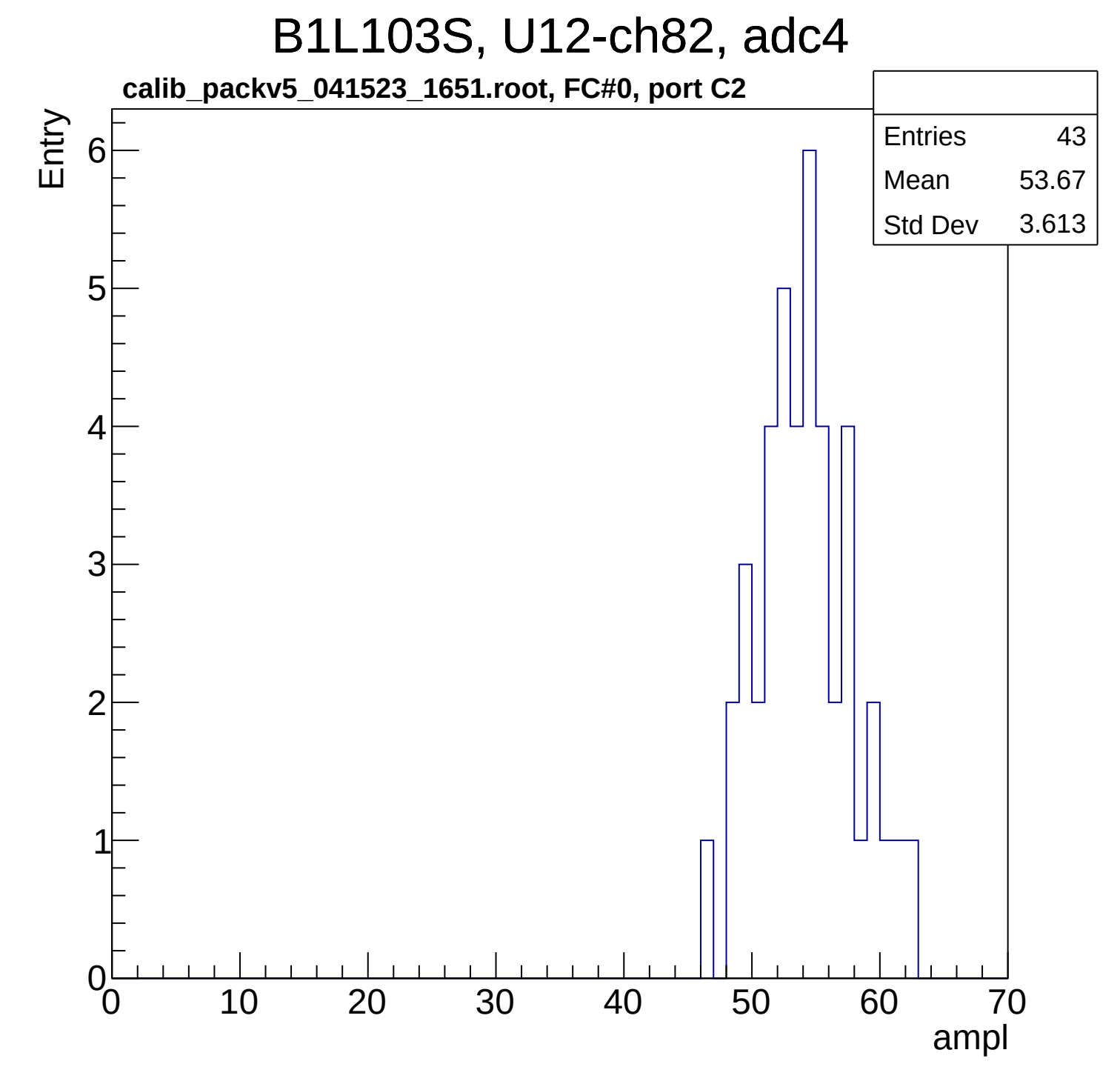

B1L103S, U12-ch82, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 109
Mean 41.9
Std Dev 16.51
Entry
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch82, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 53.67
Std Dev 3.613
Entry
ampl
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1
2
3
4
5
6
0
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20
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40
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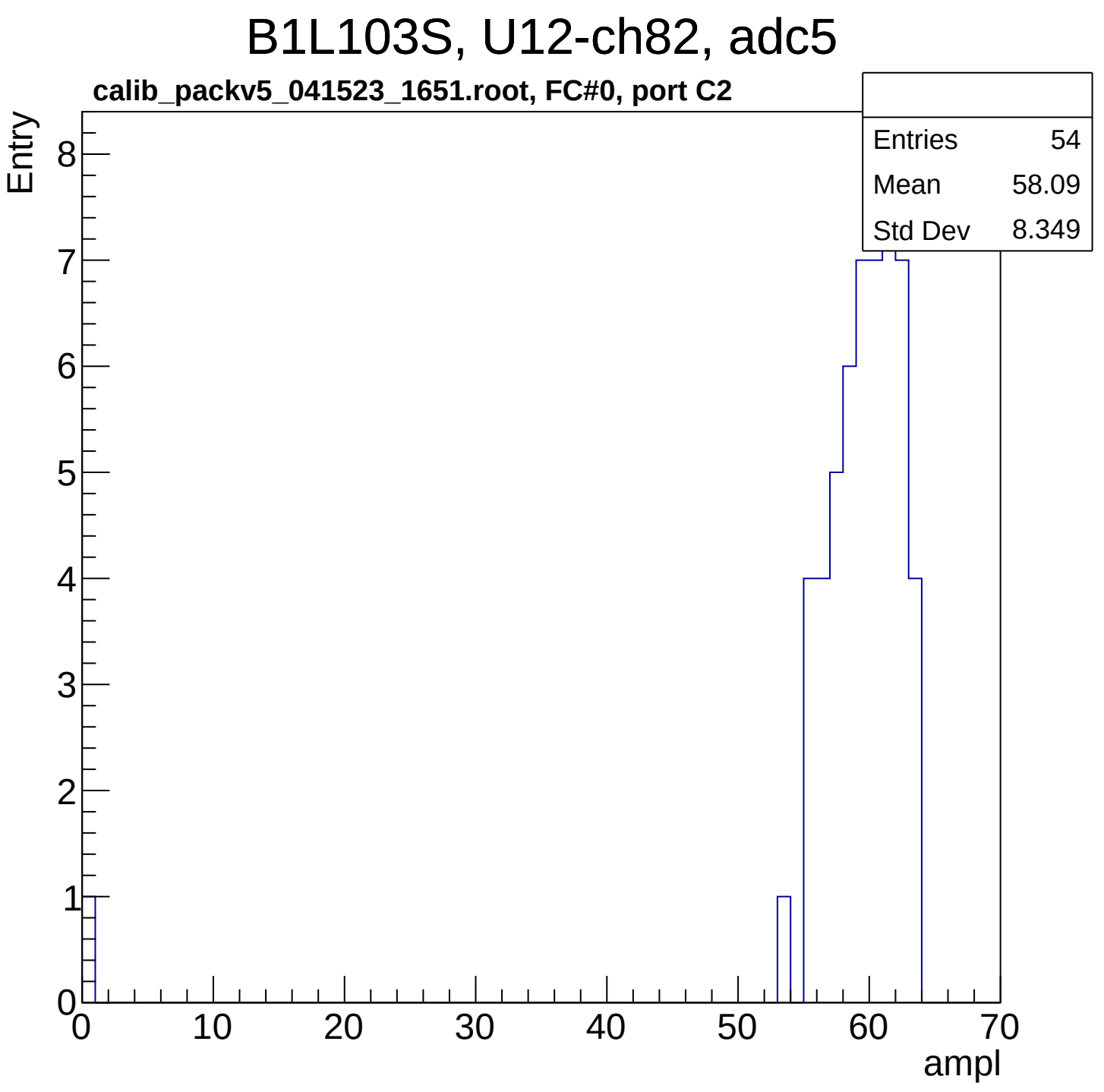
B1L103S, U12-ch82, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.09
Std Dev 8.349
Entry
ampl
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4
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0
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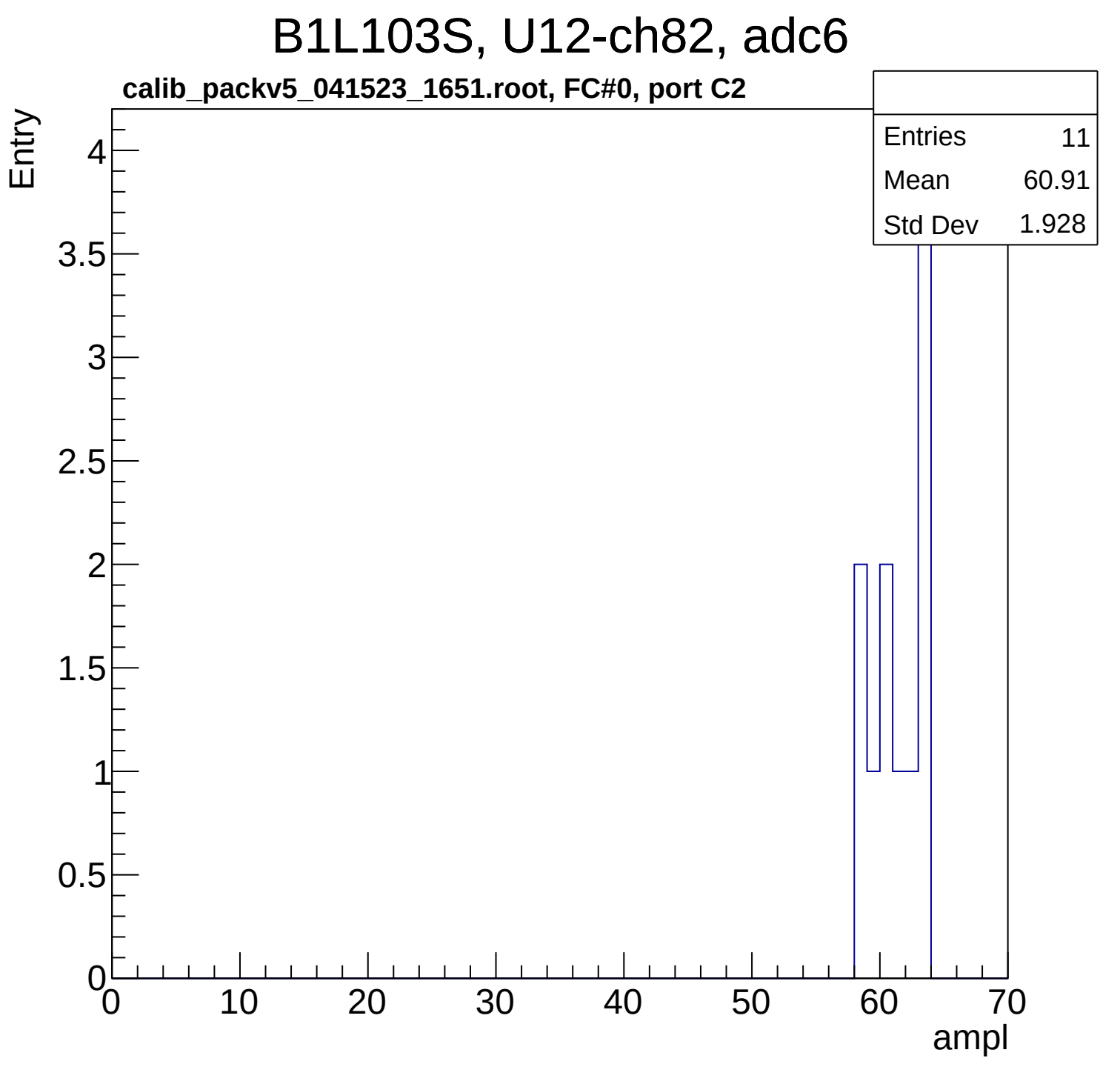
B1L103S, U12-ch82, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 60.91
Std Dev 1.928
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
50
60
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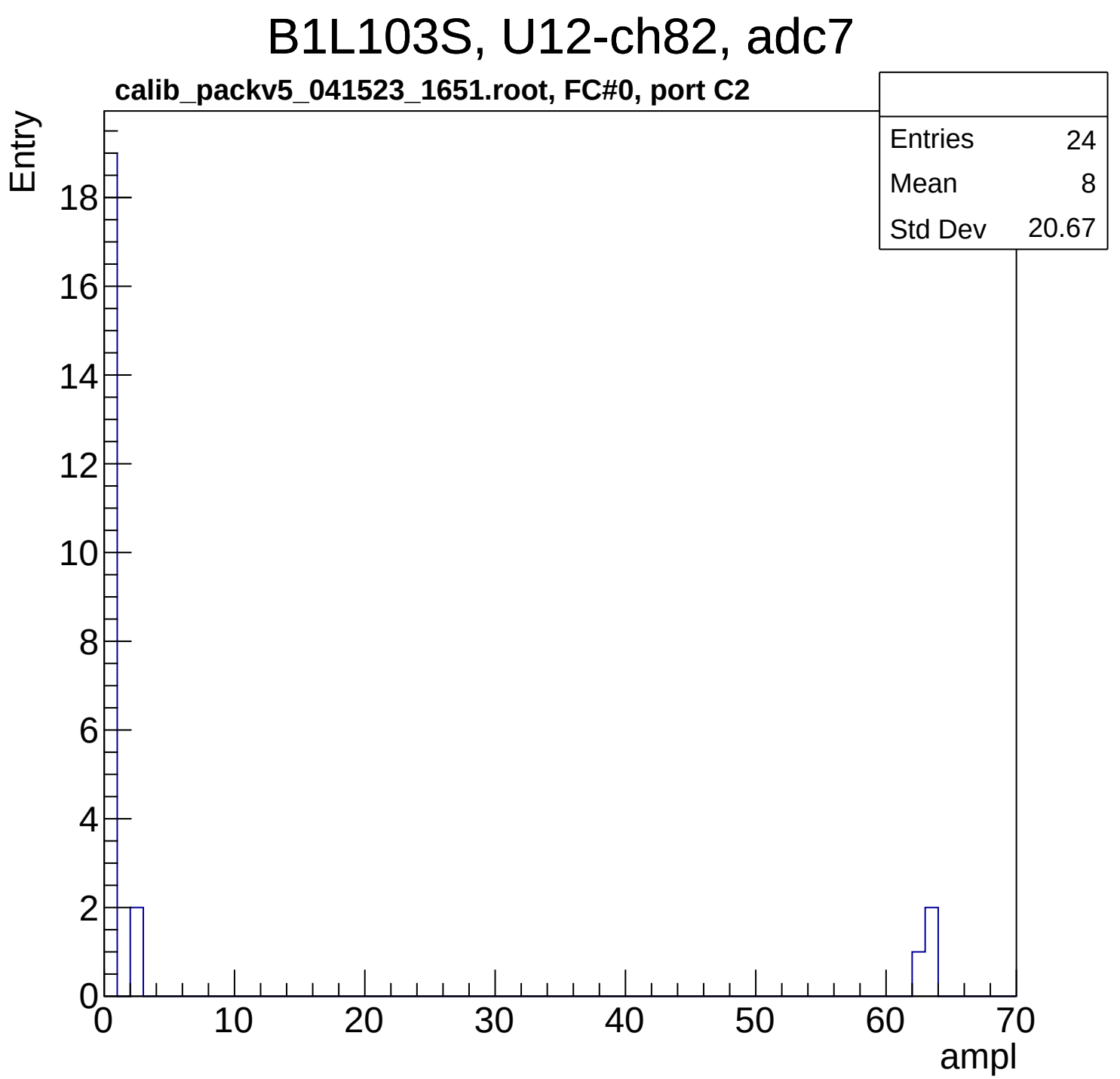
B1L103S, U12-ch82, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 8
Std Dev 20.67
Entry
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6
8
10
12
14
16
18
0
10
20
30
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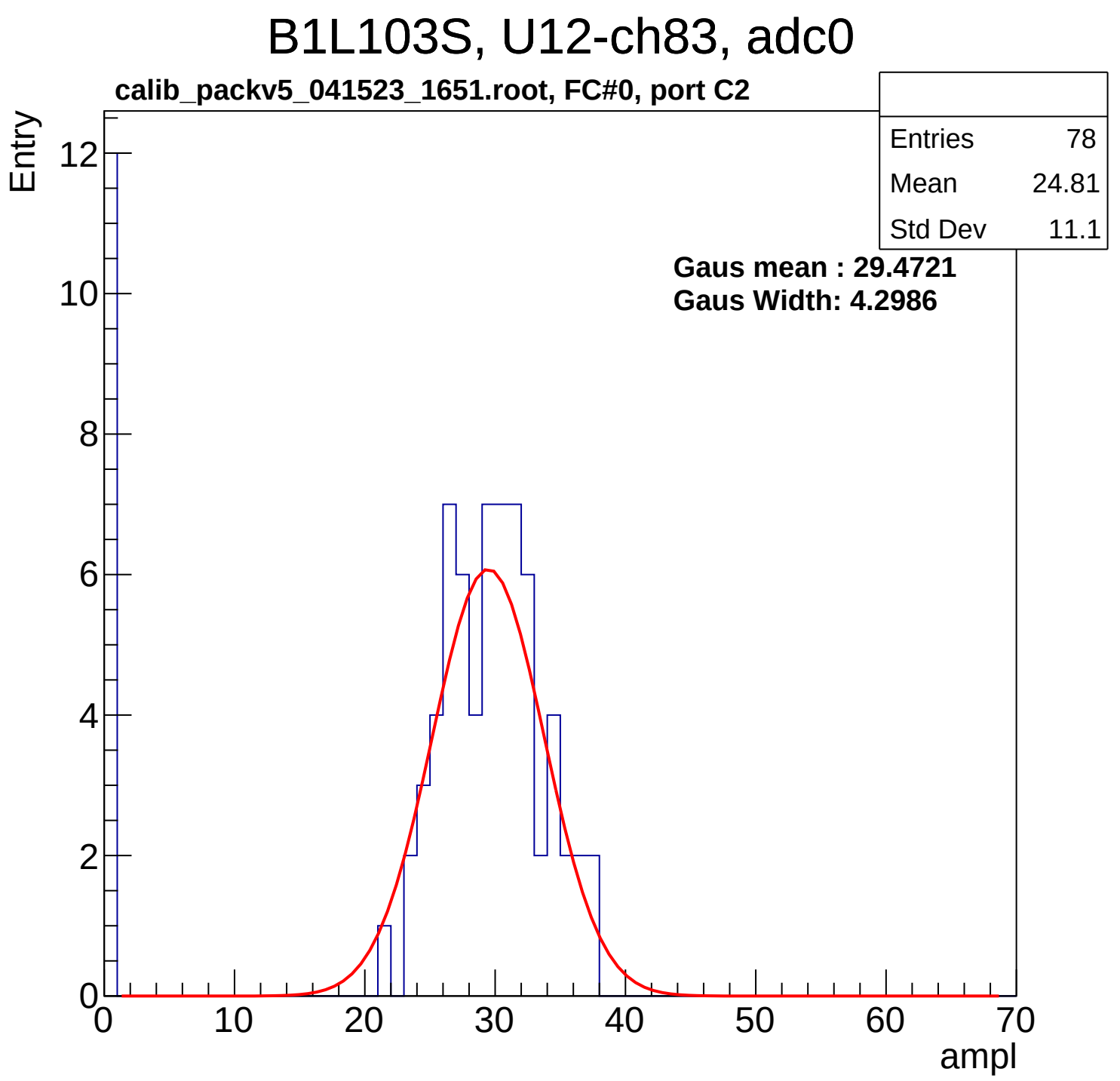
50
60
70
ampl


B1L103S, U12-ch83, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 24.81
Std Dev 11.1
Gaus mean : 29.4721
Gaus Width: 4.2986
Entry
ampl
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4
6
8
10
12
0
10
20
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60
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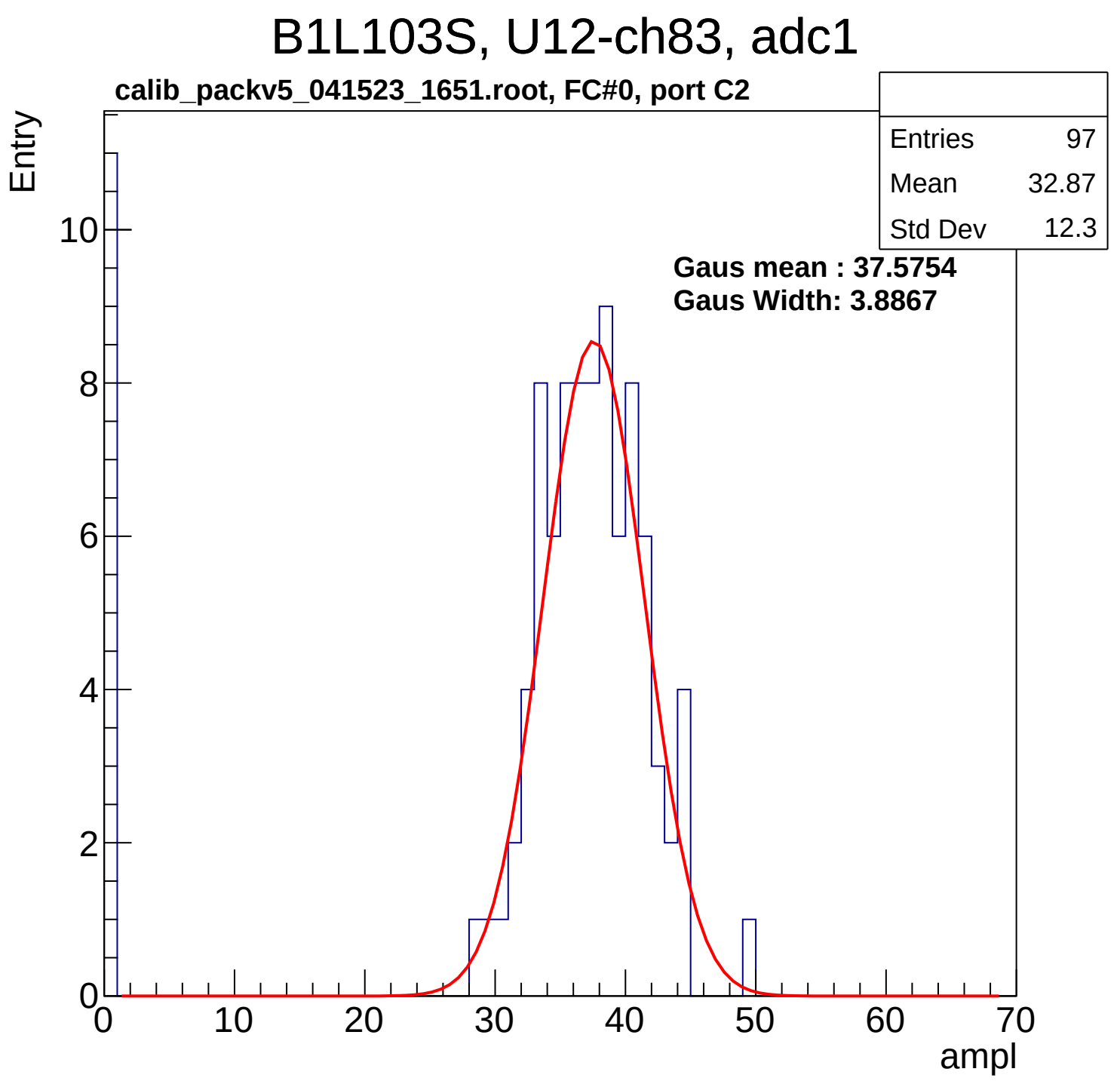
B1L103S, U12-ch83, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 32.87
Std Dev 12.3
Gaus mean : 37.5754
Gaus Width: 3.8867
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
50
60
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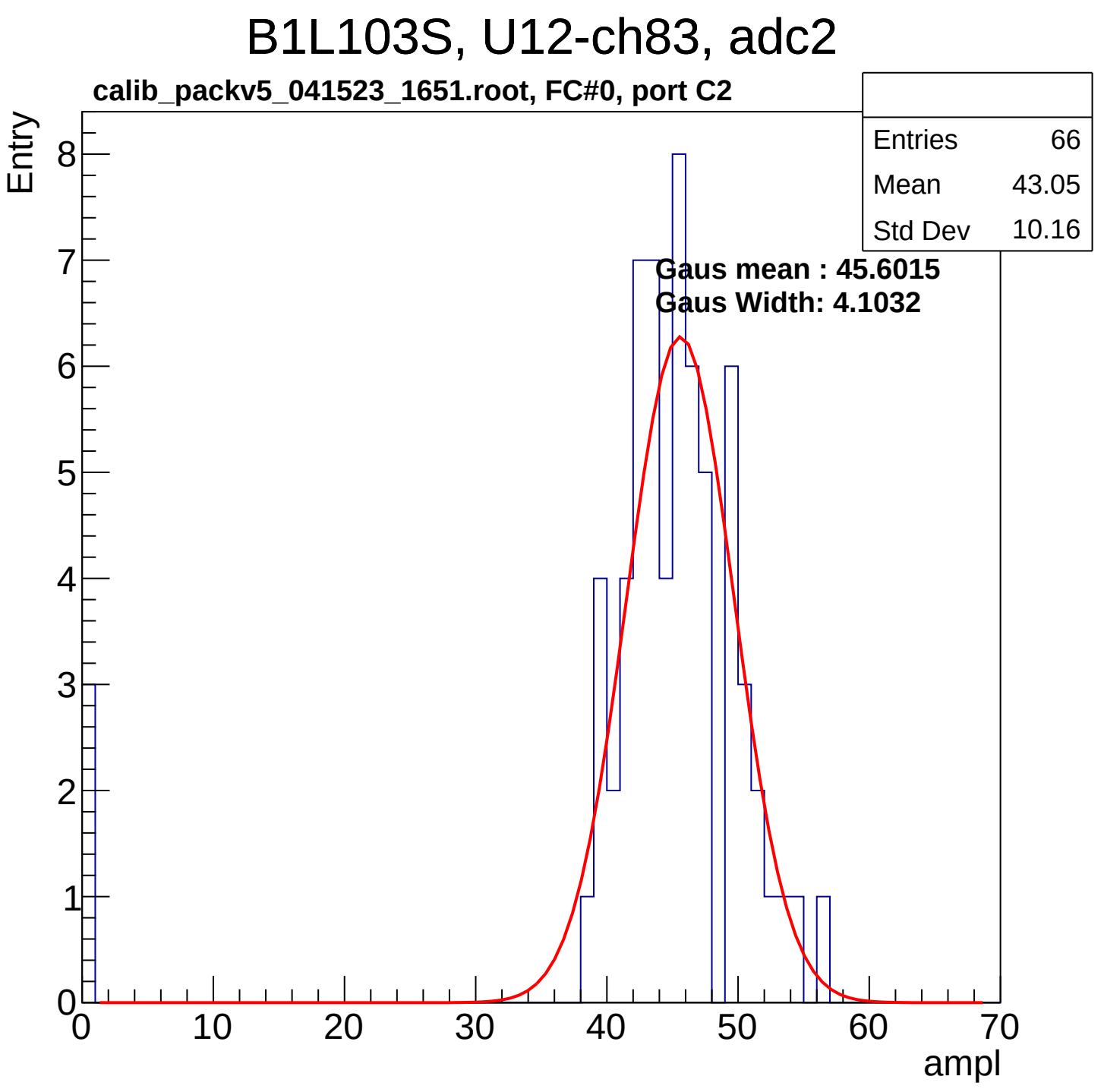
B1L103S, U12-ch83, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 43.05
Std Dev 10.16
Gaus mean : 45.6015
Gaus Width: 4.1032
Entry
ampl
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2
3
4
5
6
7
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0
10
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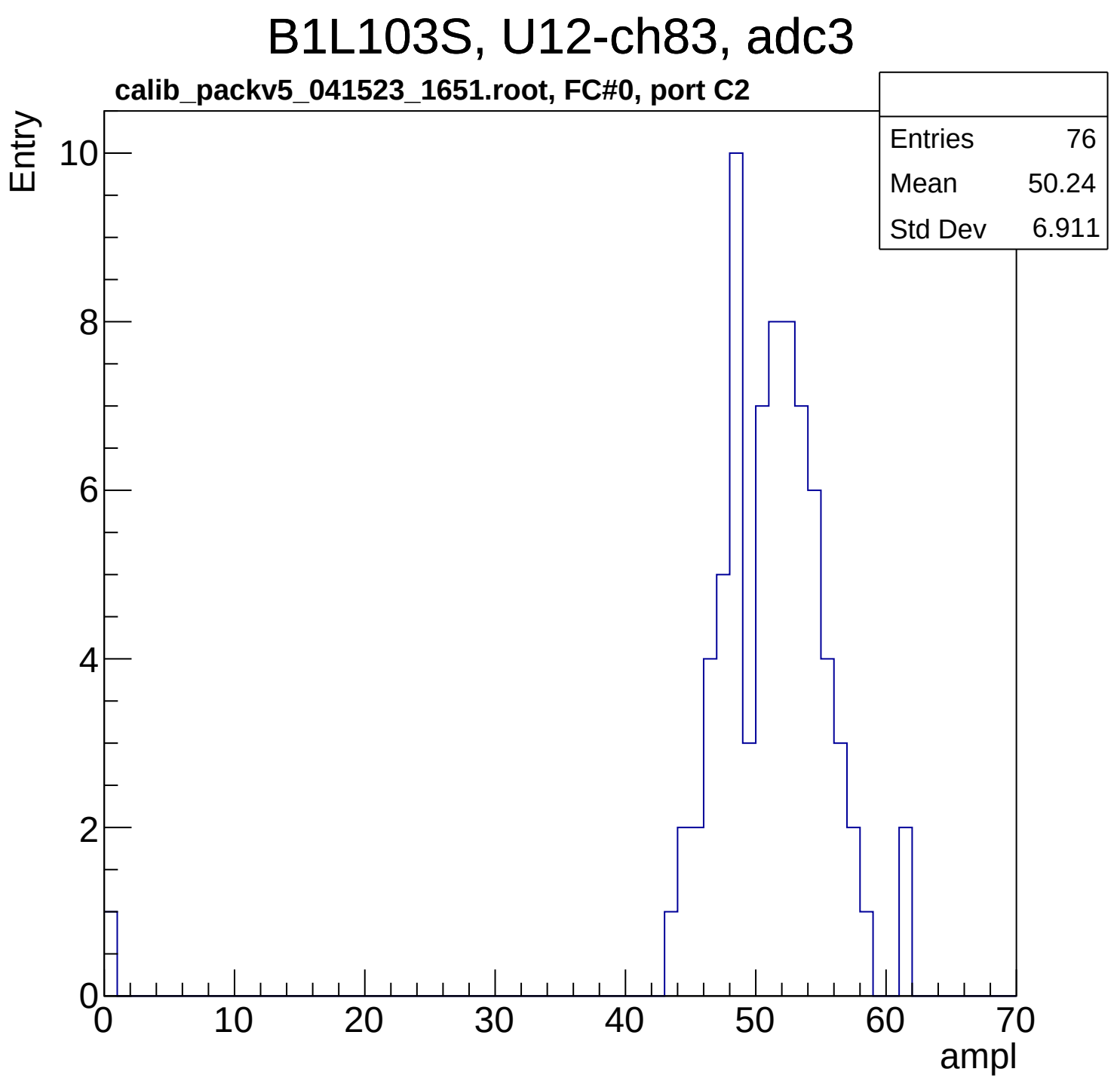
B1L103S, U12-ch83, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 50.24
Std Dev 6.911
Entry
ampl
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0
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40
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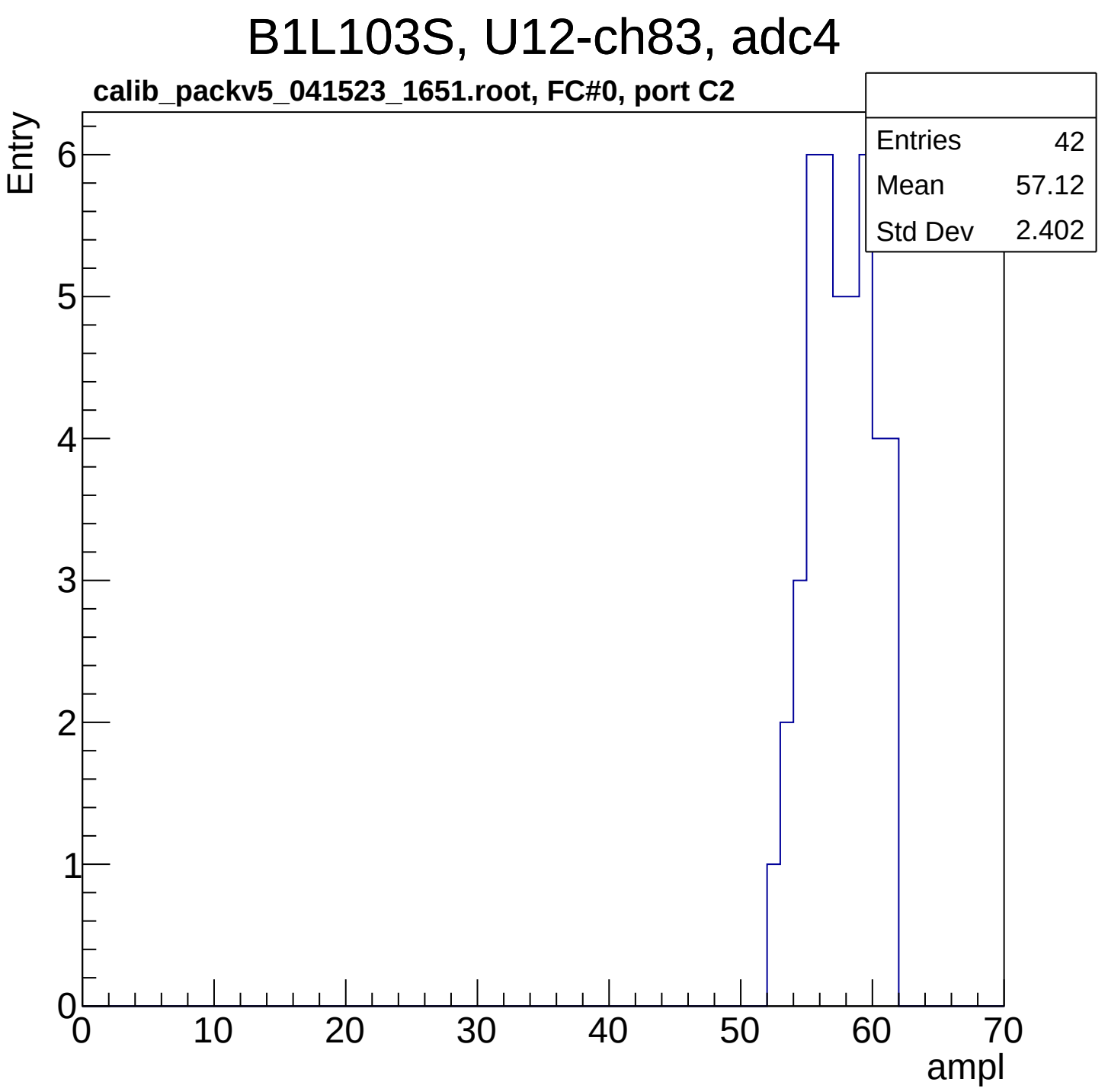
B1L103S, U12-ch83, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 57.12
Std Dev 2.402
Entry
ampl
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3
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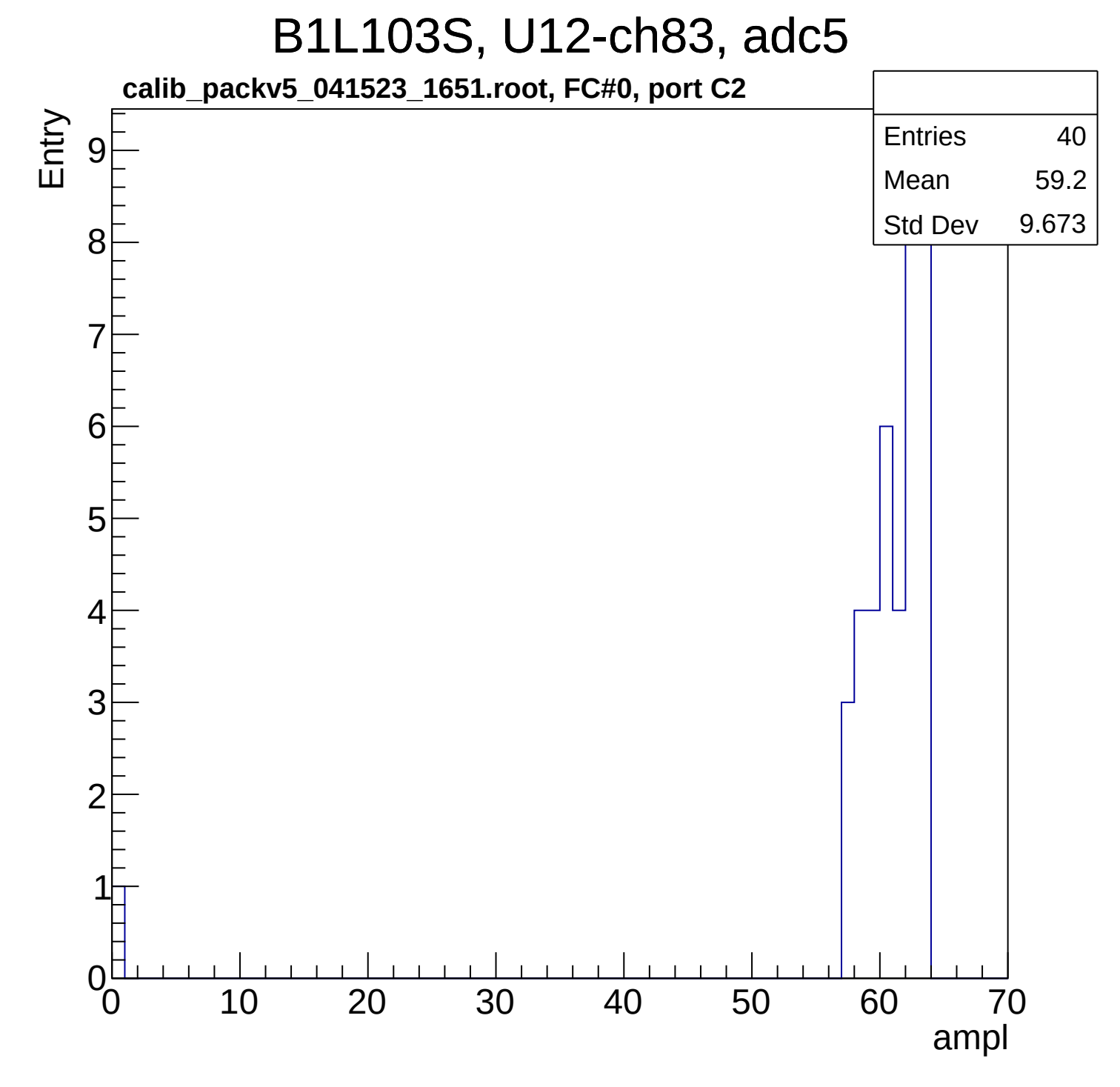
B1L103S, U12-ch83, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 40
Mean 59.2
Std Dev 9.673
Entry
ampl
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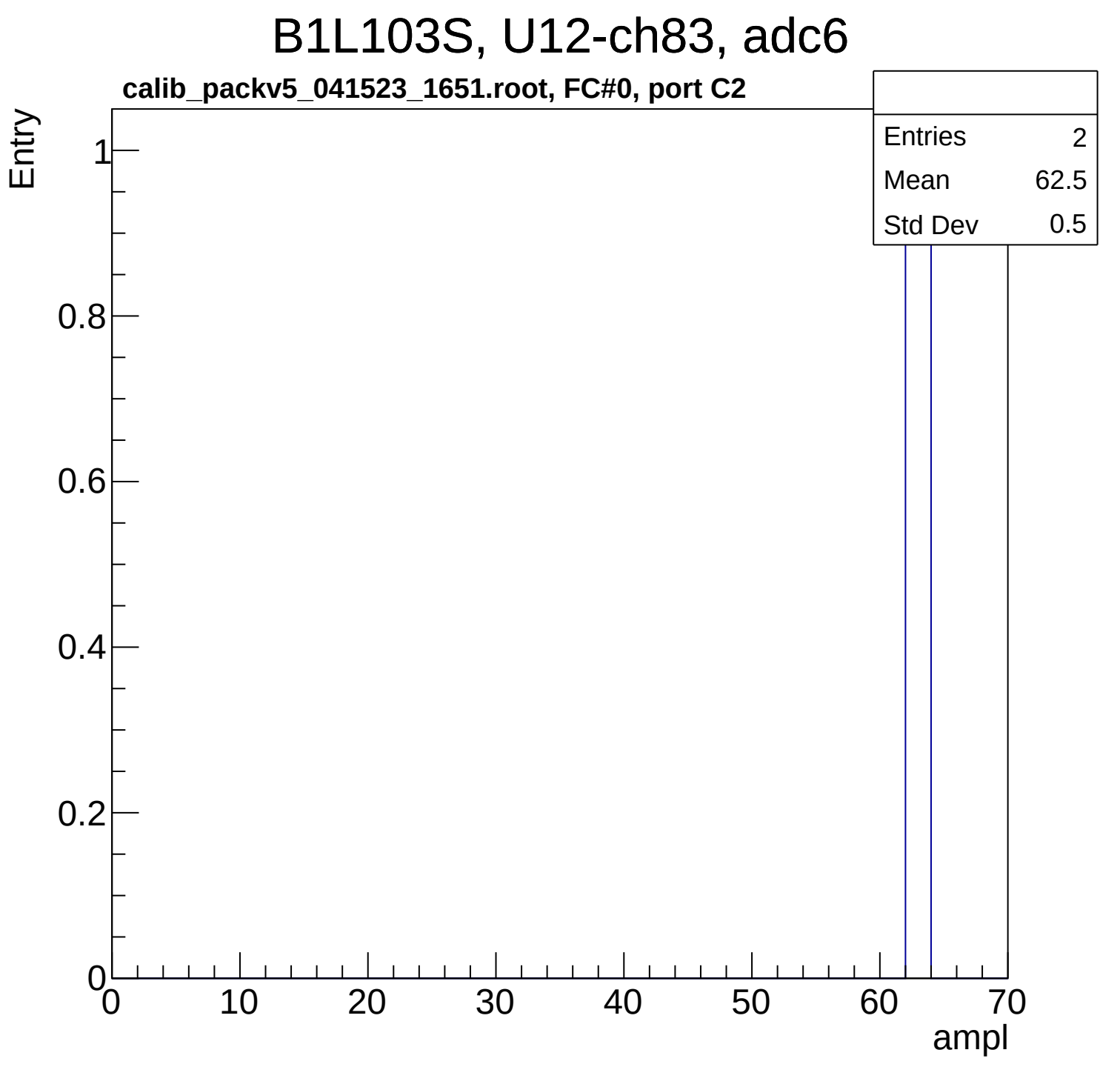
B1L103S, U12-ch83, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
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0.6
0.4
0.2
0
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10
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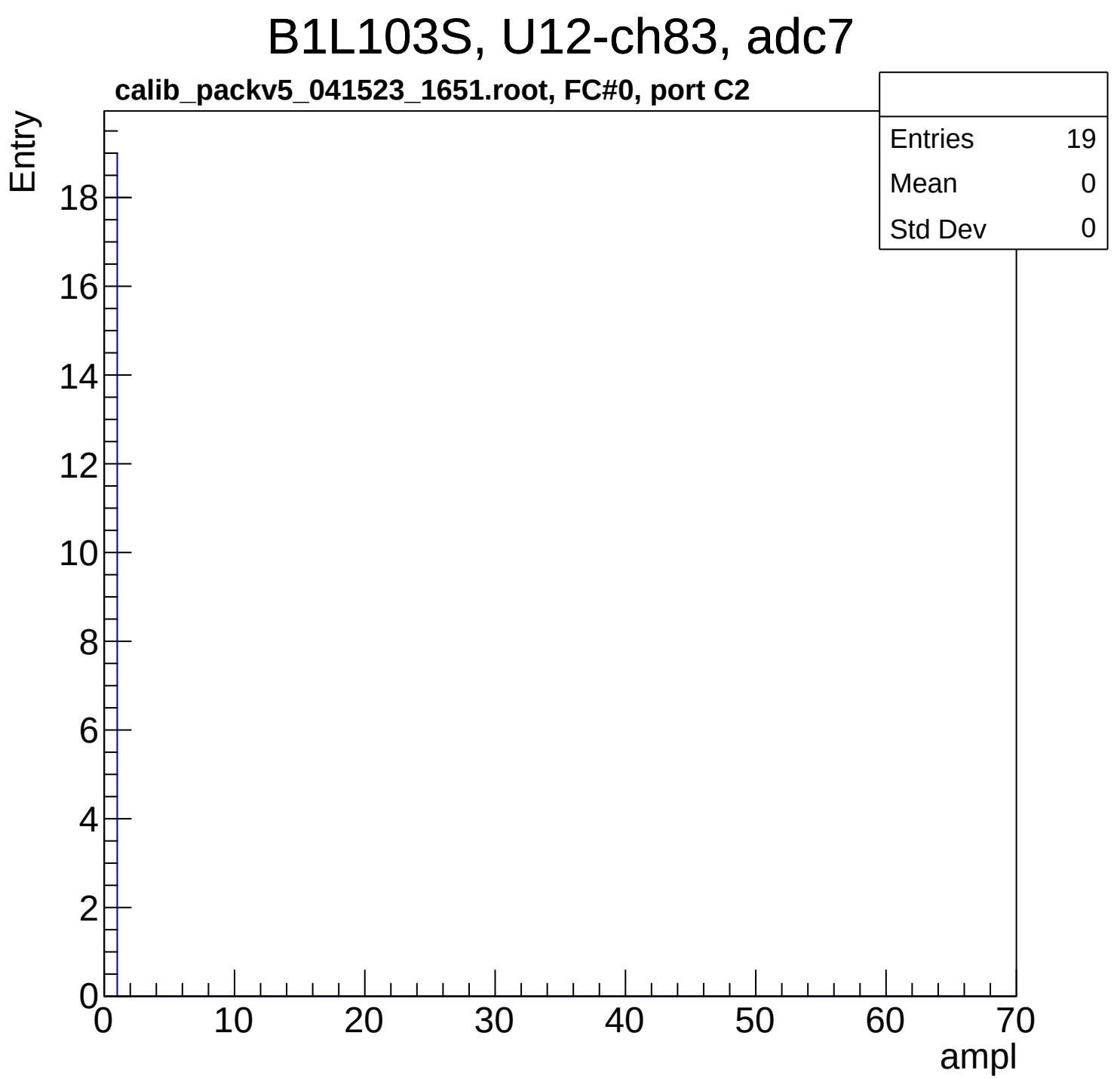
70
ampl


B1L103S, U12-ch83, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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8
10
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14
16
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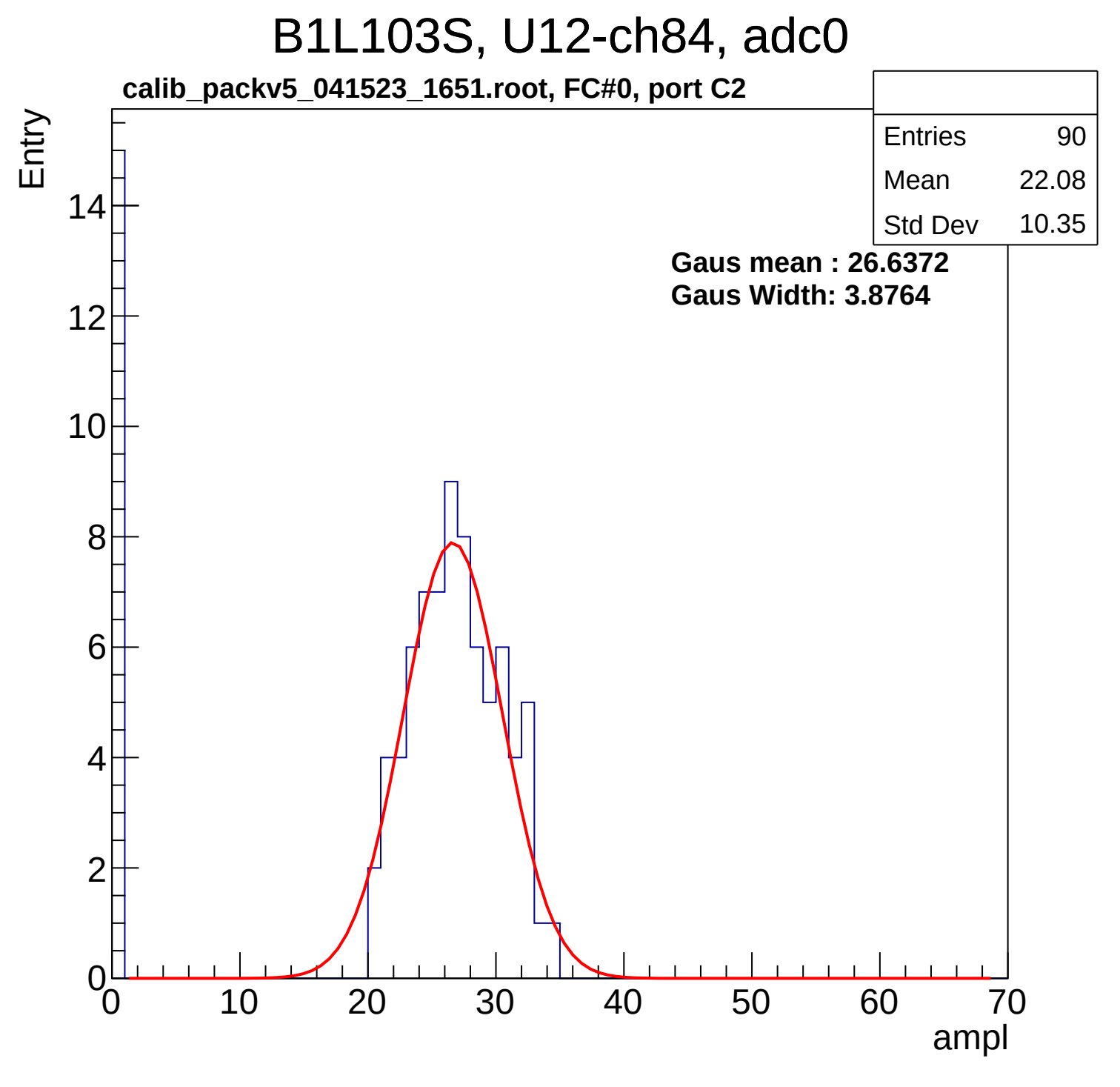
ampl


B1L103S, U12-ch84, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 22.08
Std Dev 10.35
Gaus mean : 26.6372
Gaus Width: 3.8764
Entry
ampl
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8
10
12
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0
10
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60
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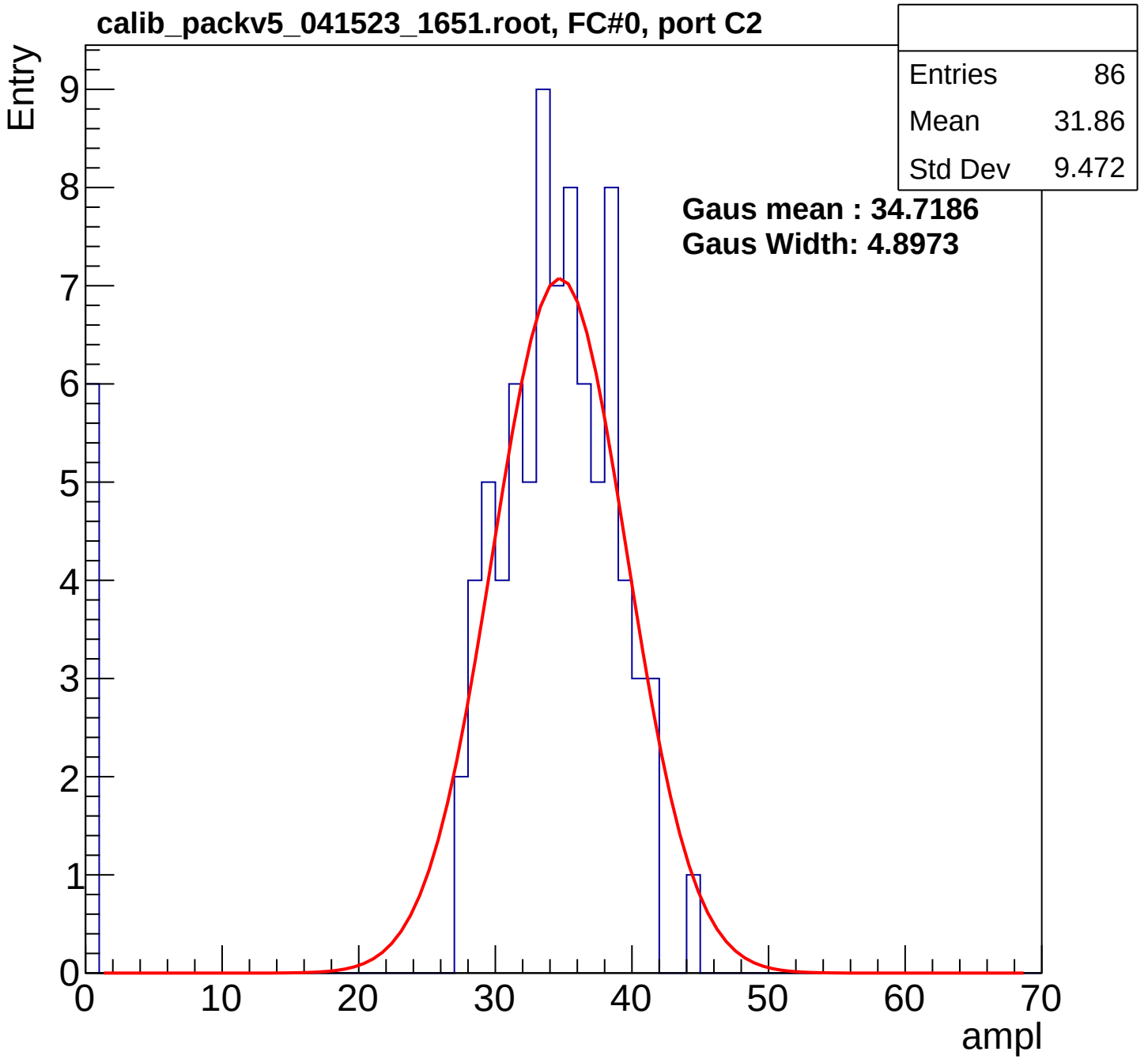
B1L103S, U12-ch84, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 31.86
Std Dev 9.472
Gaus mean : 34.7186
Gaus Width: 4.8973
Entry
ampl
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3
4
5
6
7
8
9
0
10
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40
50
60
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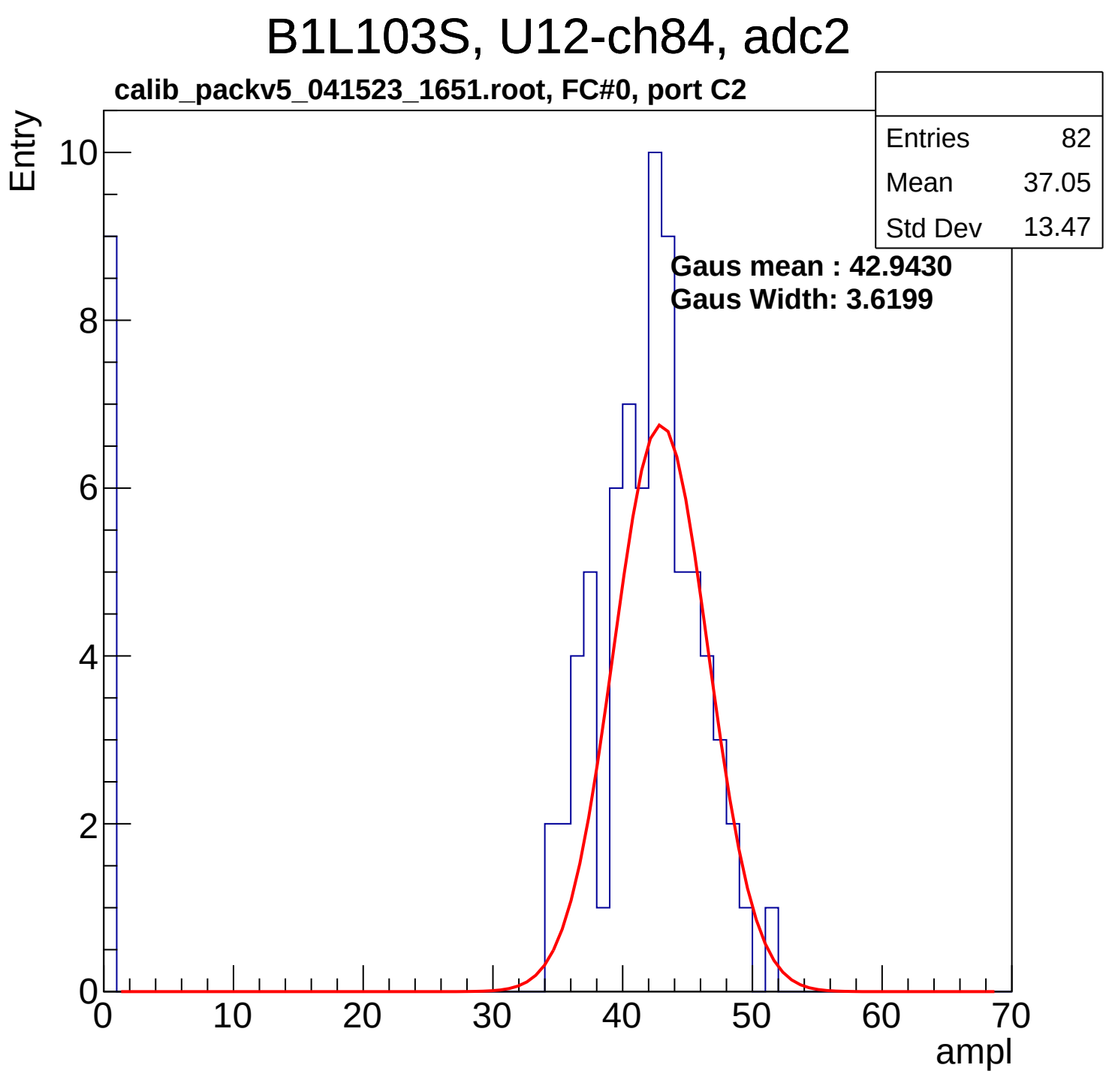
B1L103S, U12-ch84, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 37.05
Std Dev 13.47
Gaus mean : 42.9430
Gaus Width: 3.6199
Entry
ampl
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2
4
6
8
10
0
10
20
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40
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60
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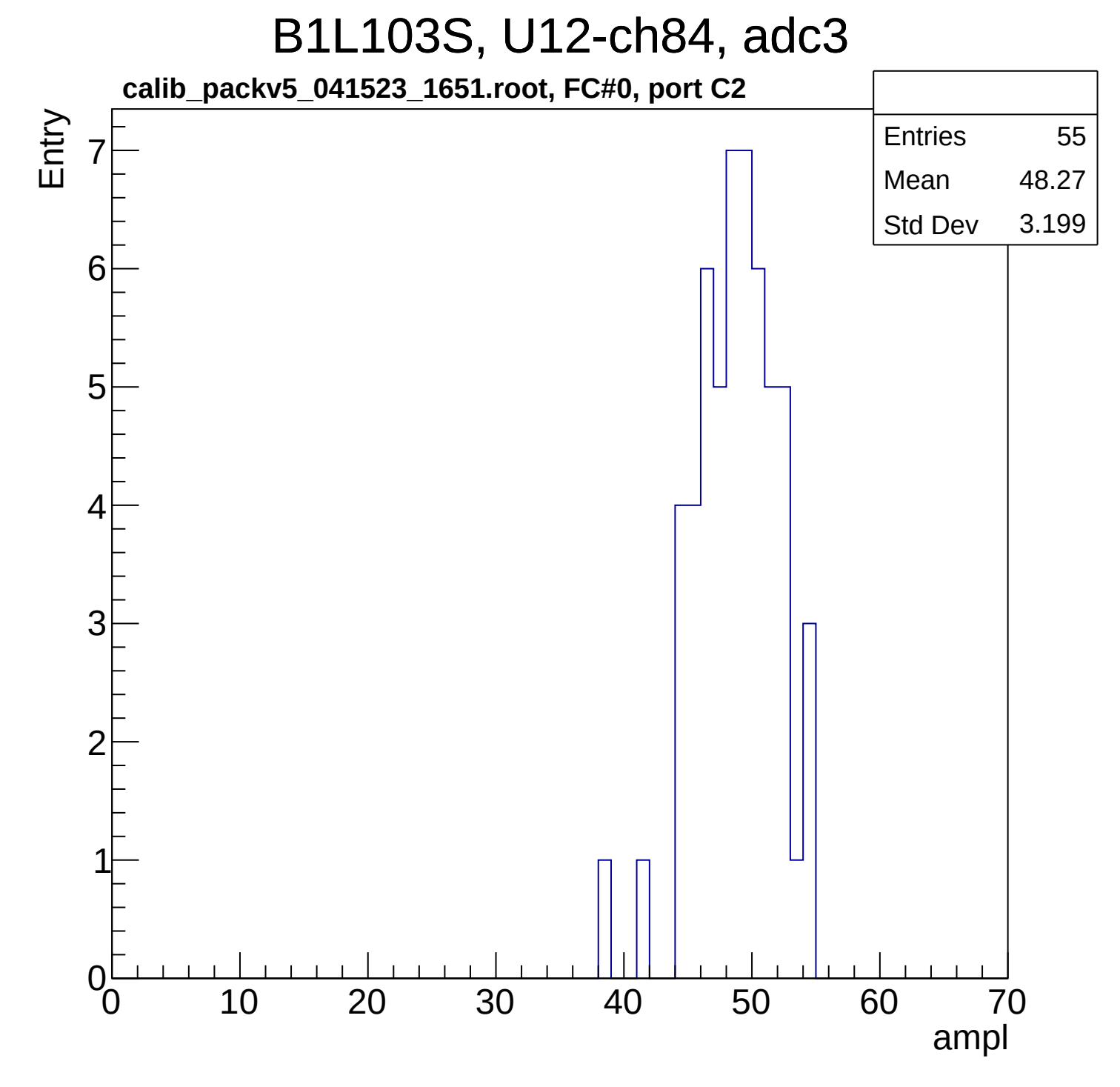
B1L103S, U12-ch84, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 48.27
Std Dev 3.199
Entry
ampl
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4
5
6
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0
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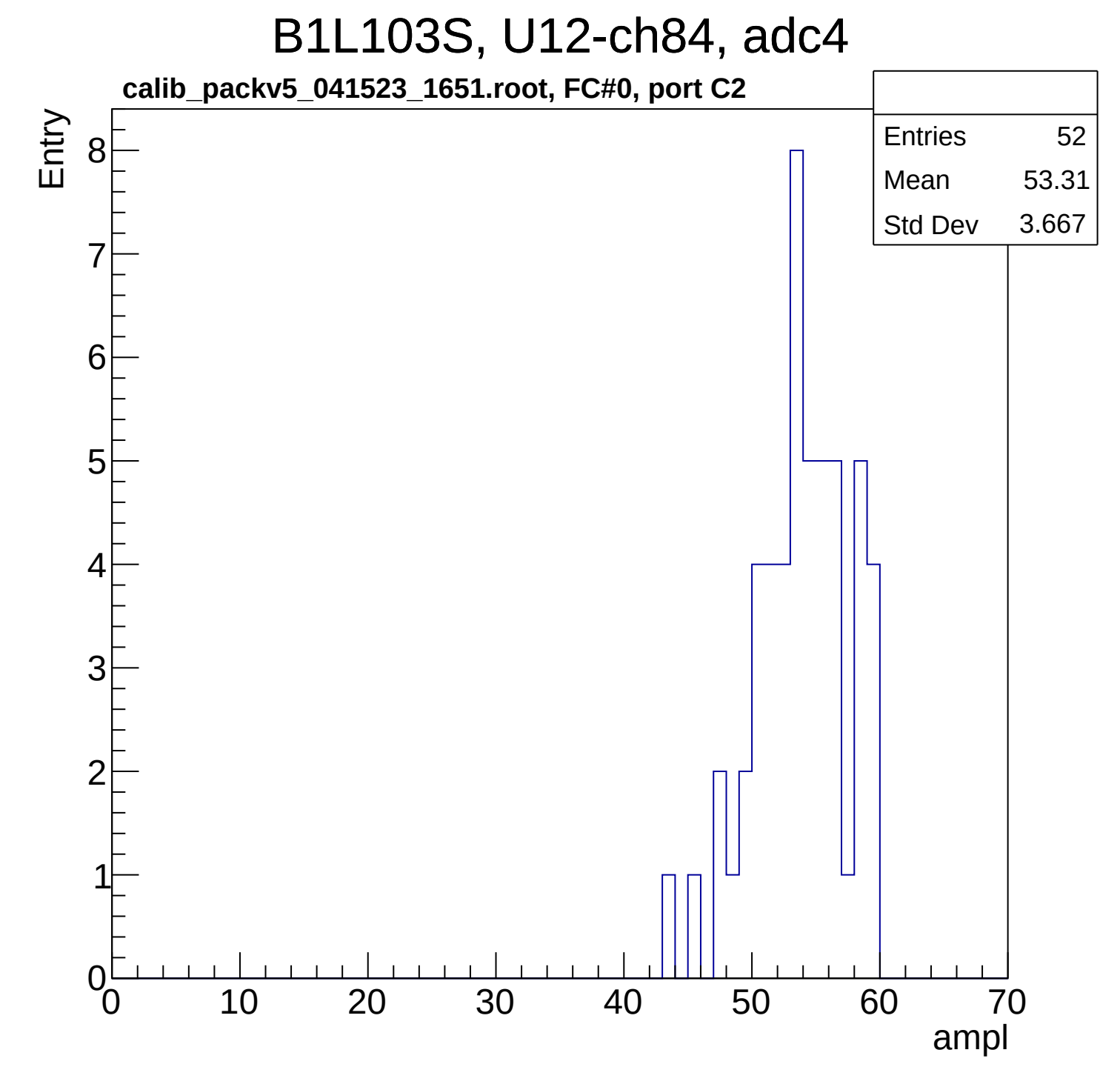
B1L103S, U12-ch84, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 53.31
Std Dev 3.667
Entry
ampl
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3
4
5
6
7
8
0
10
20
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40
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60
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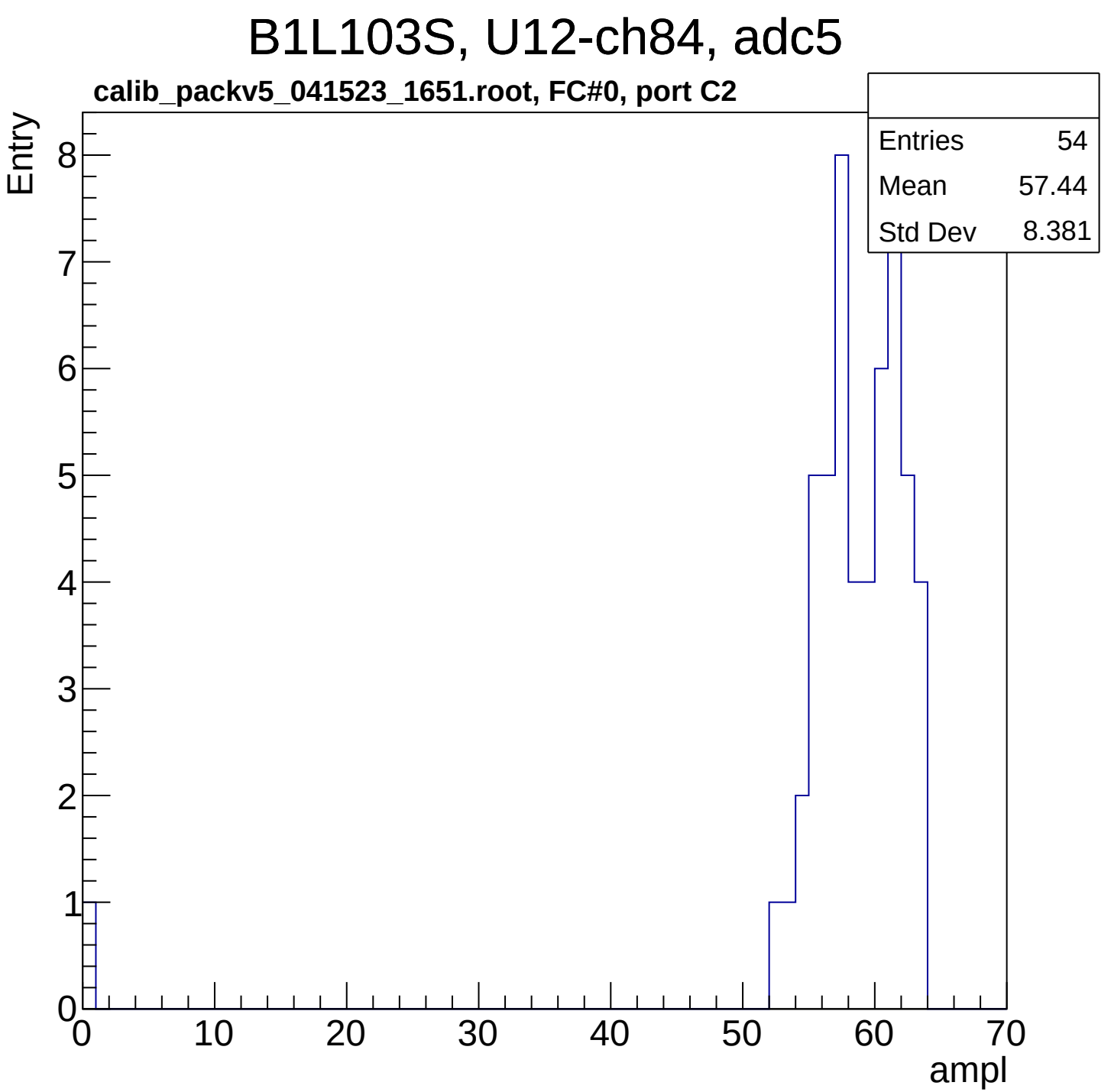
B1L103S, U12-ch84, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.44
Std Dev 8.381
Entry
ampl
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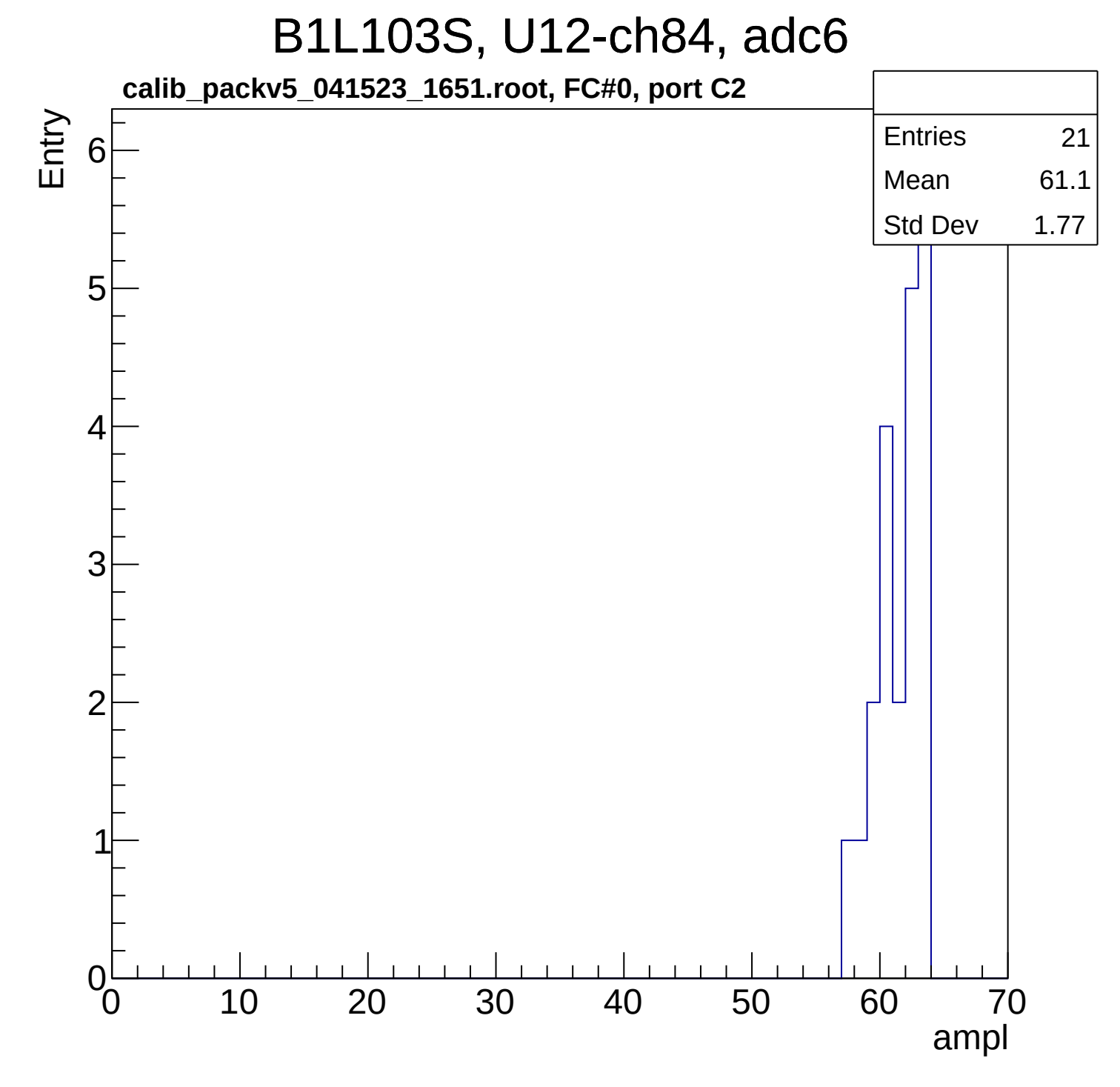
B1L103S, U12-ch84, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 61.1
Std Dev 1.77
Entry
ampl
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4
5
6
0
10
20
30
40
50
60
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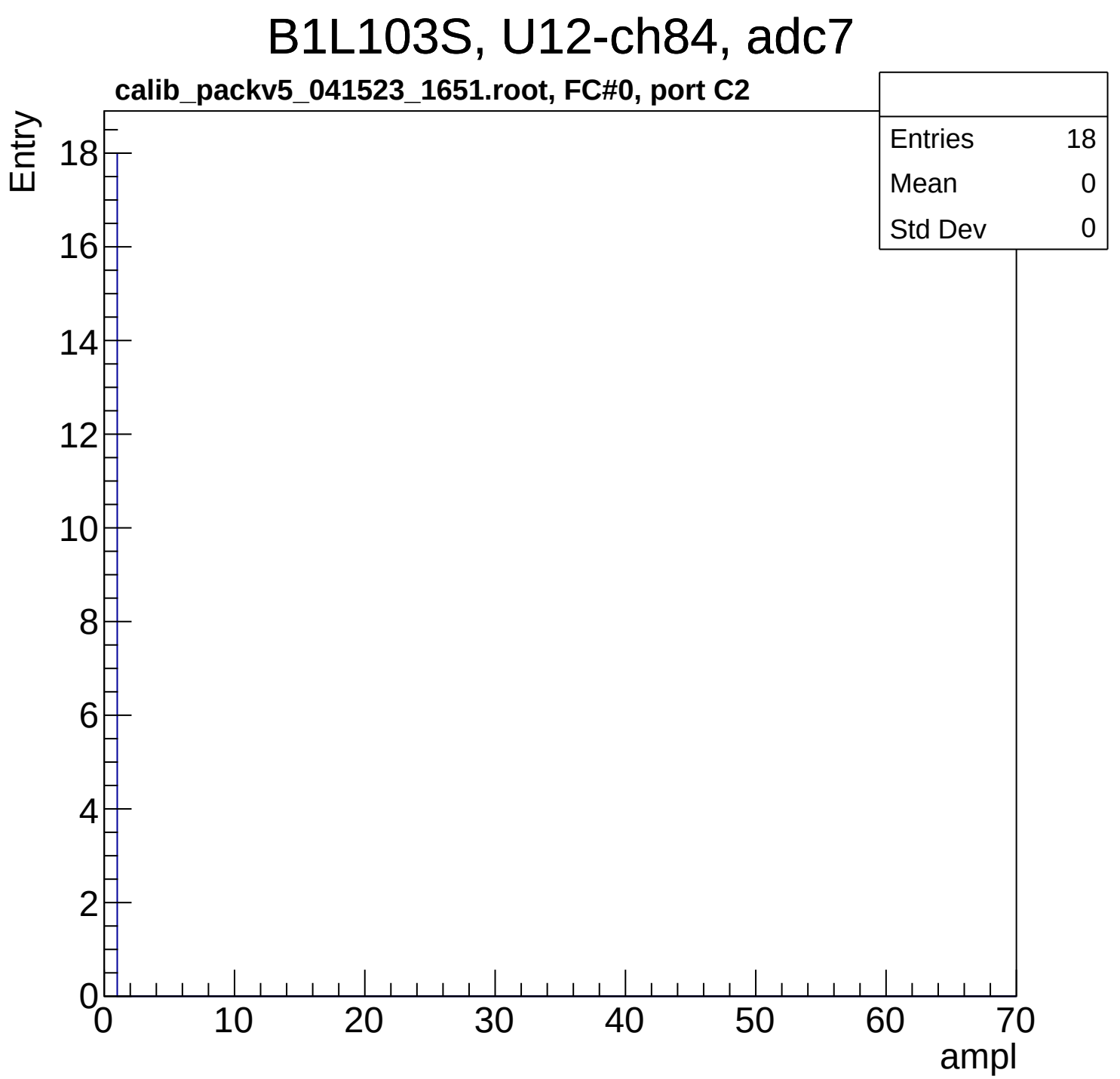
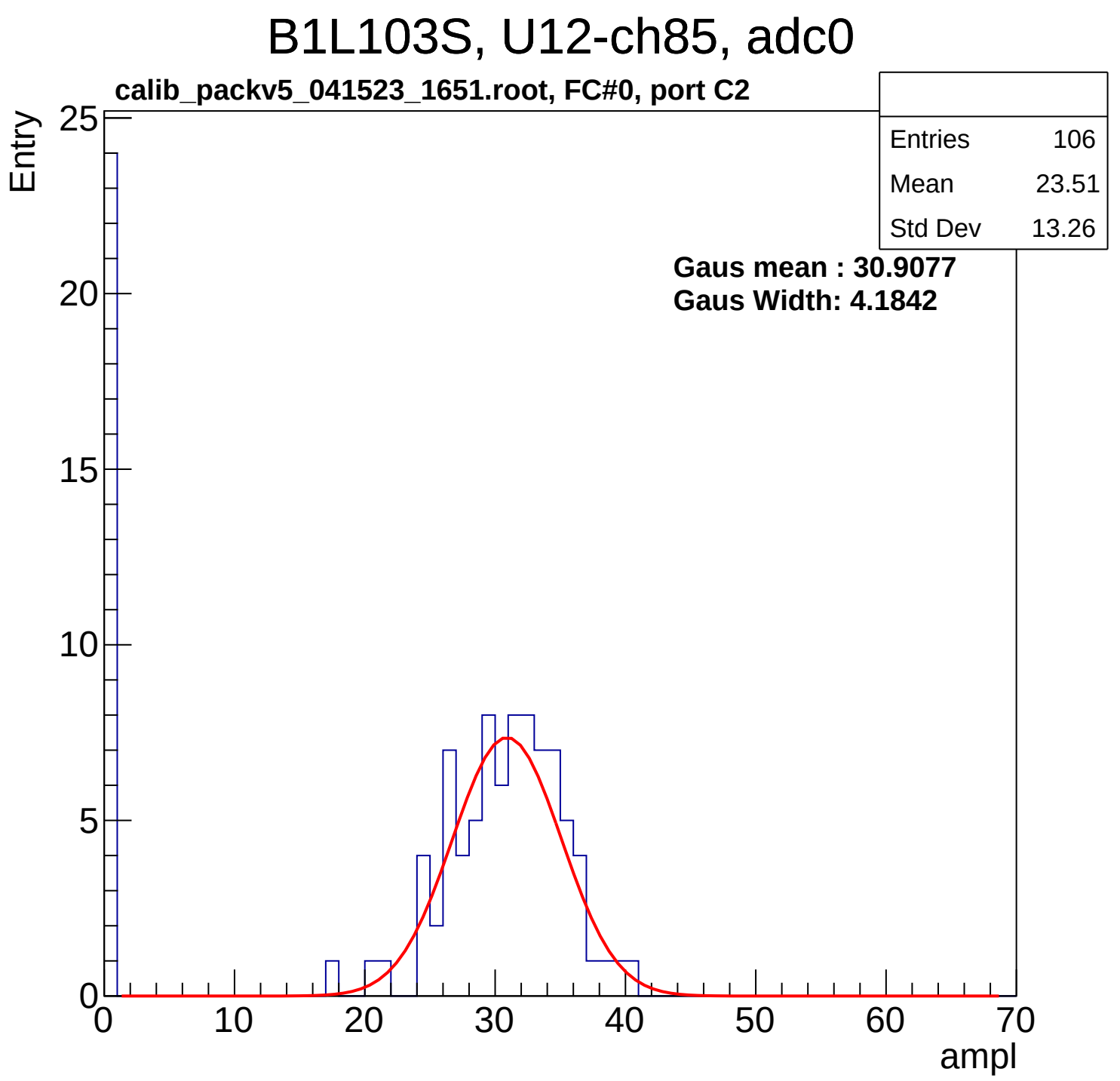

B1L103S, U12-ch84, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch85, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 106
Mean 23.51
Std Dev 13.26
Gaus mean : 30.9077
Gaus Width: 4.1842
Entry
ampl
0
5
10
15
20
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0
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40
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60
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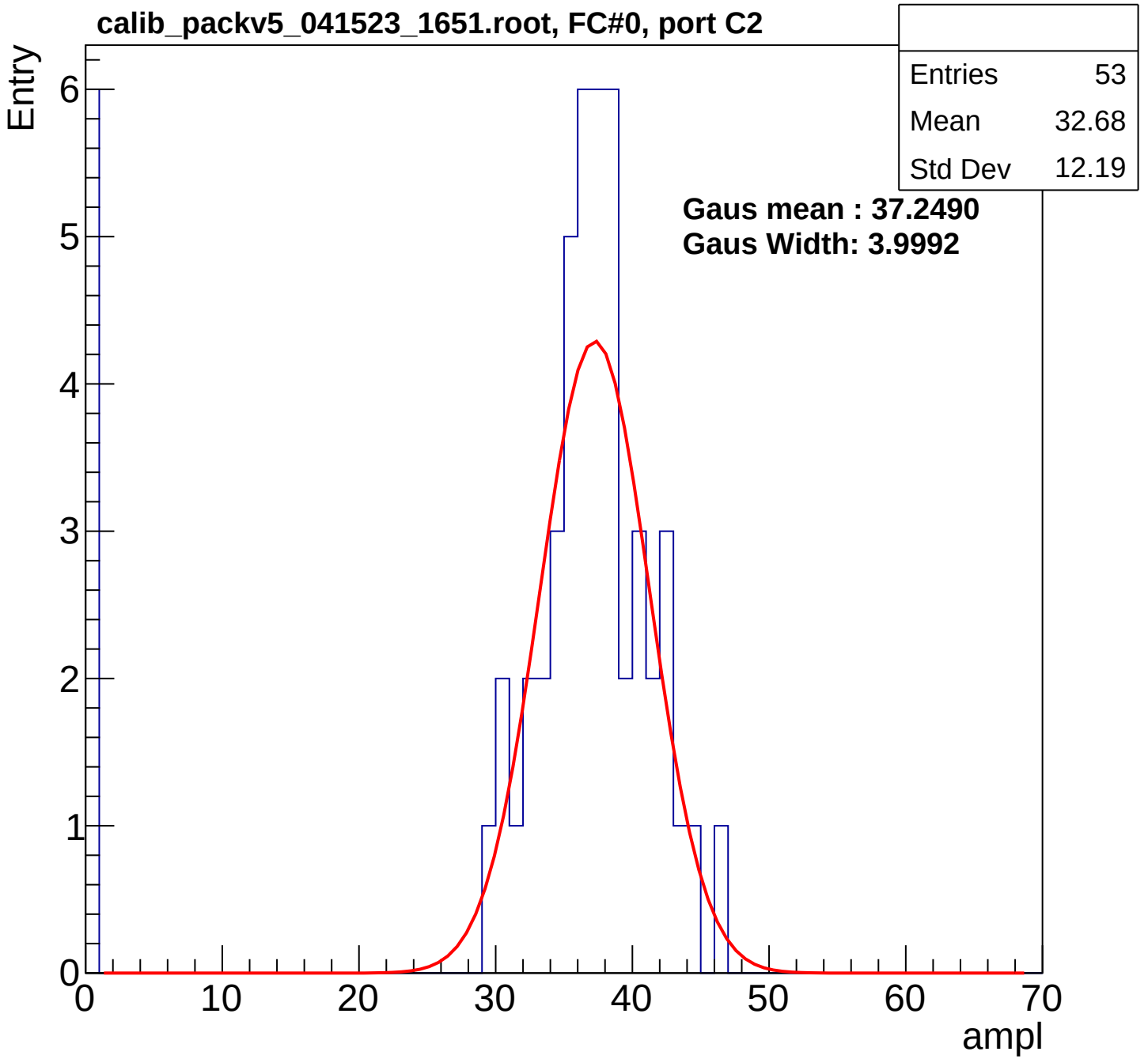
B1L103S, U12-ch85, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 32.68
Std Dev 12.19
Gaus mean : 37.2490
Gaus Width: 3.9992
Entry
ampl
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1
2
3
4
5
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0
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40
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60
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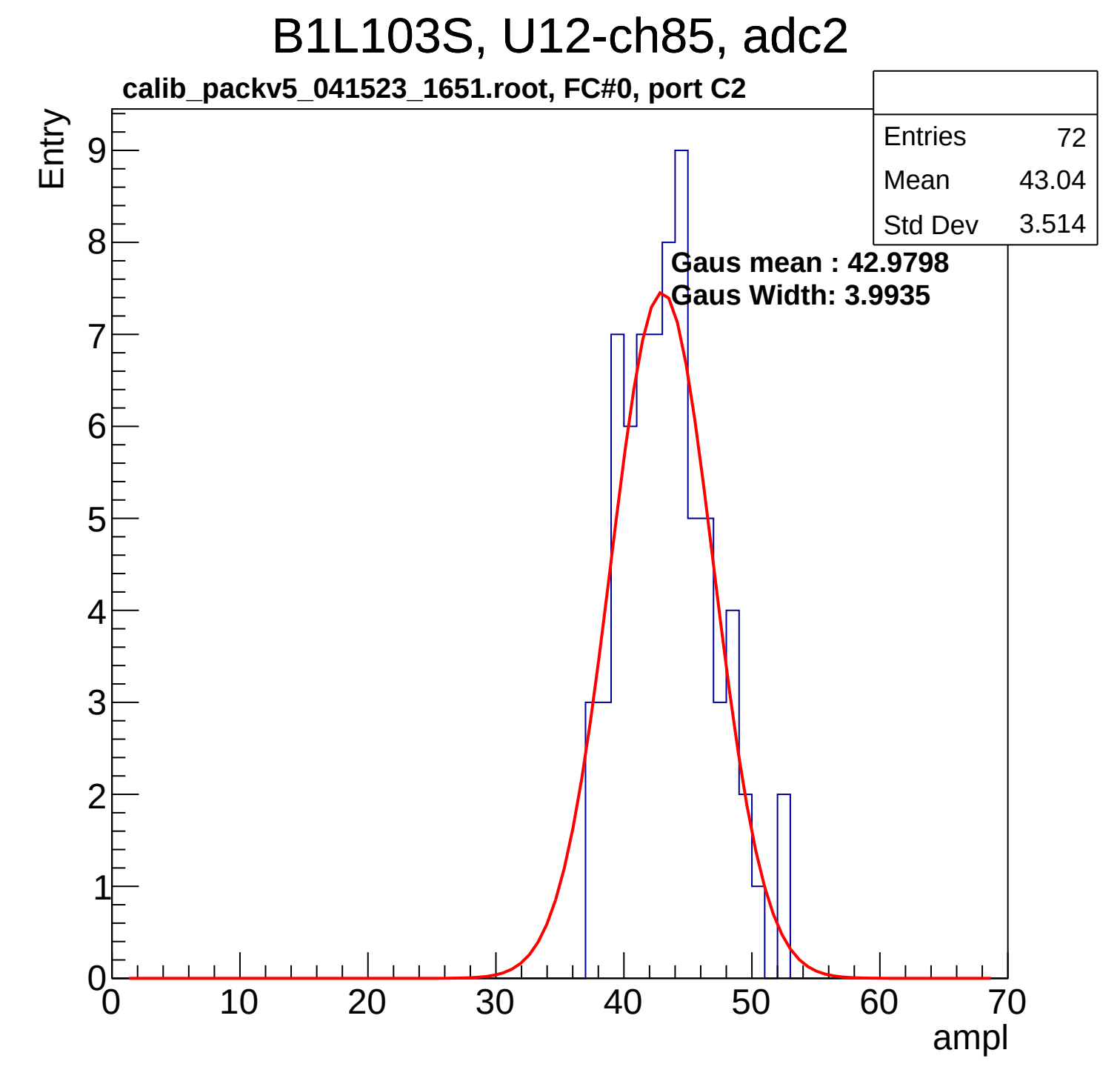
B1L103S, U12-ch85, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 43.04
Std Dev 3.514
Gaus mean : 42.9798
Gaus Width: 3.9935
Entry
ampl
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1
2
3
4
5
6
7
8
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0
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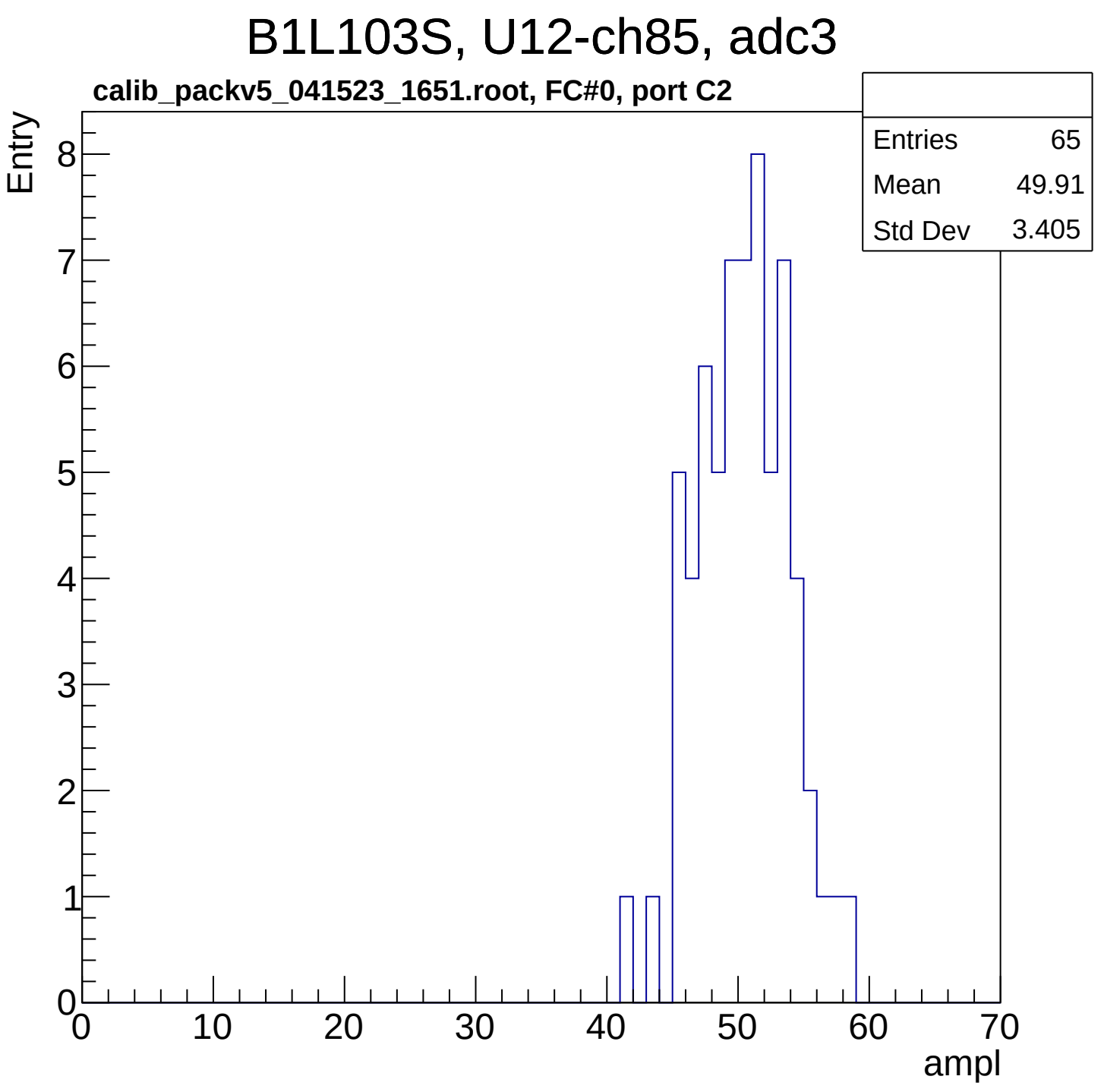
B1L103S, U12-ch85, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 49.91
Std Dev 3.405
Entry
ampl
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1
2
3
4
5
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7
8
0
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40
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60
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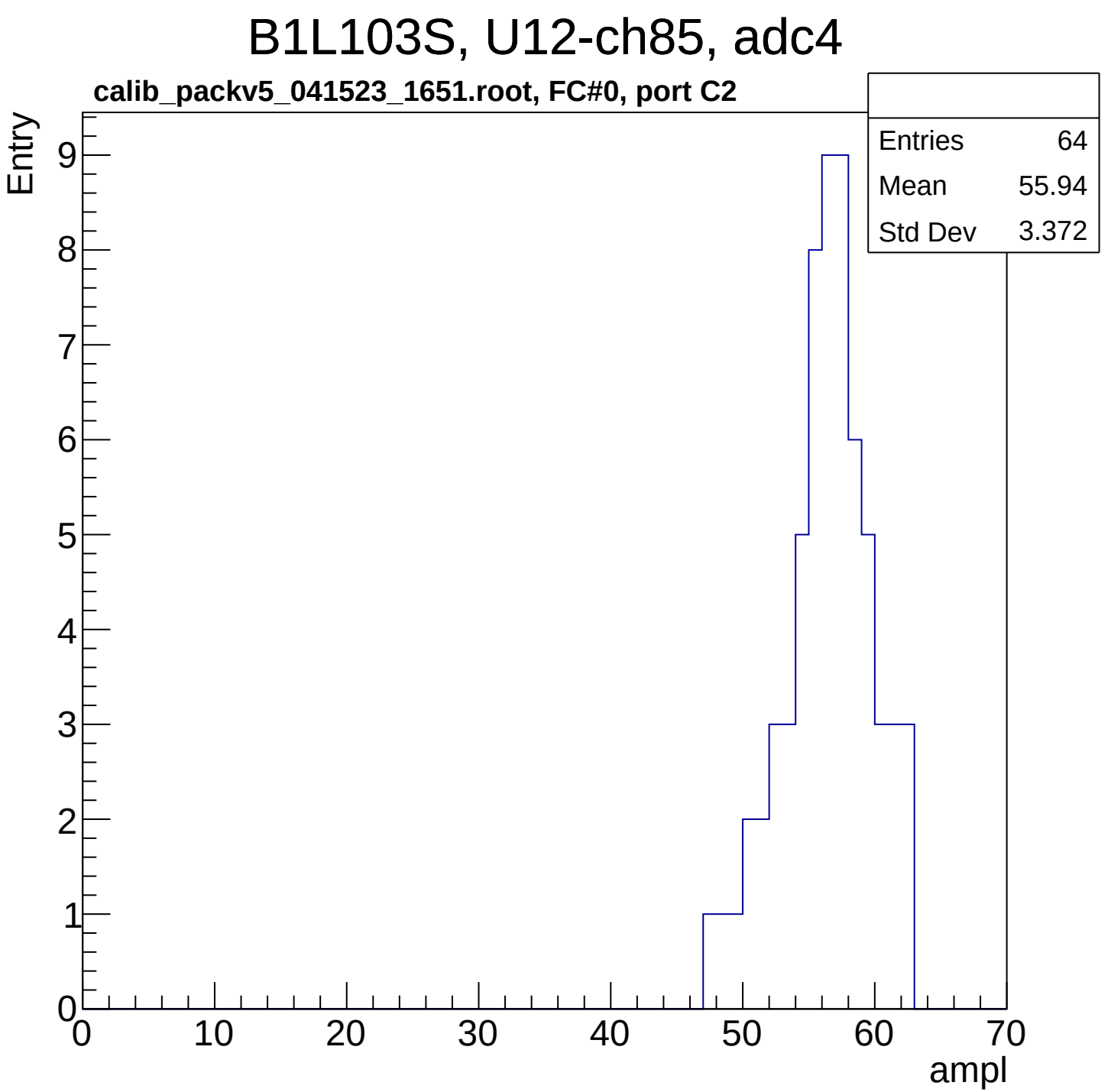
B1L103S, U12-ch85, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 55.94
Std Dev 3.372
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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40
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60
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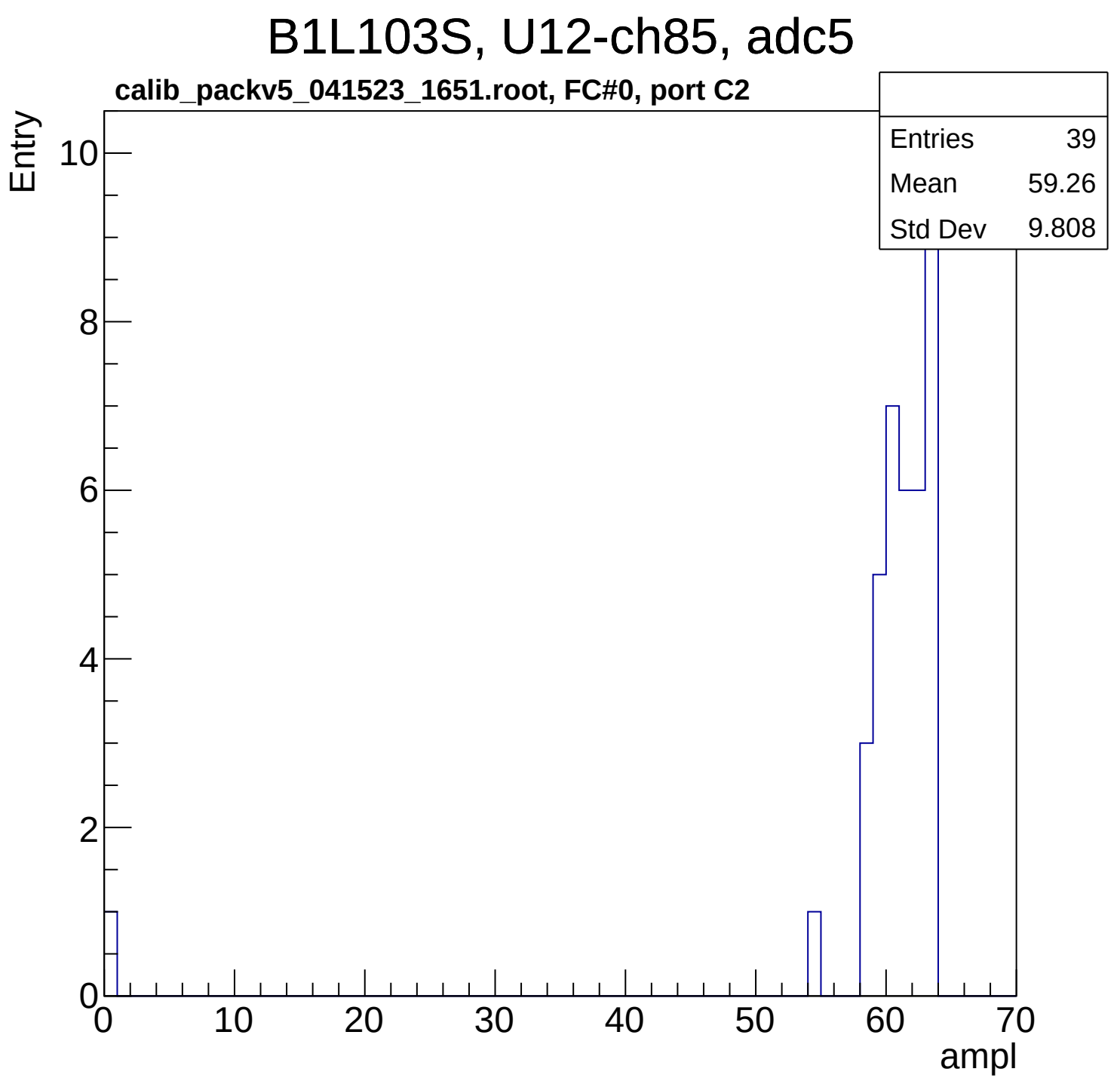
B1L103S, U12-ch85, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 59.26
Std Dev 9.808
Entry
ampl
0
2
4
6
8
10
0
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20
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40
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60
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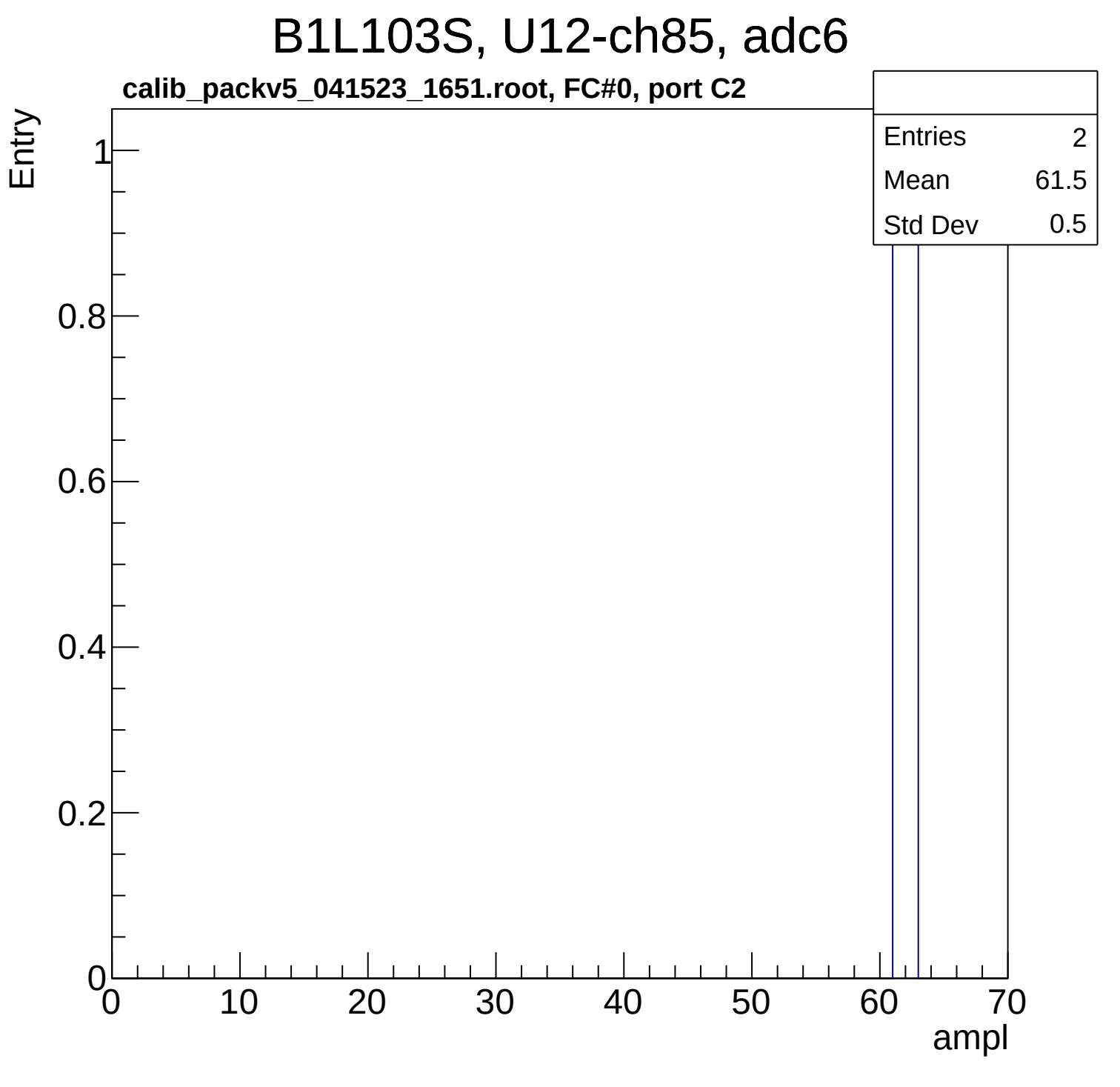
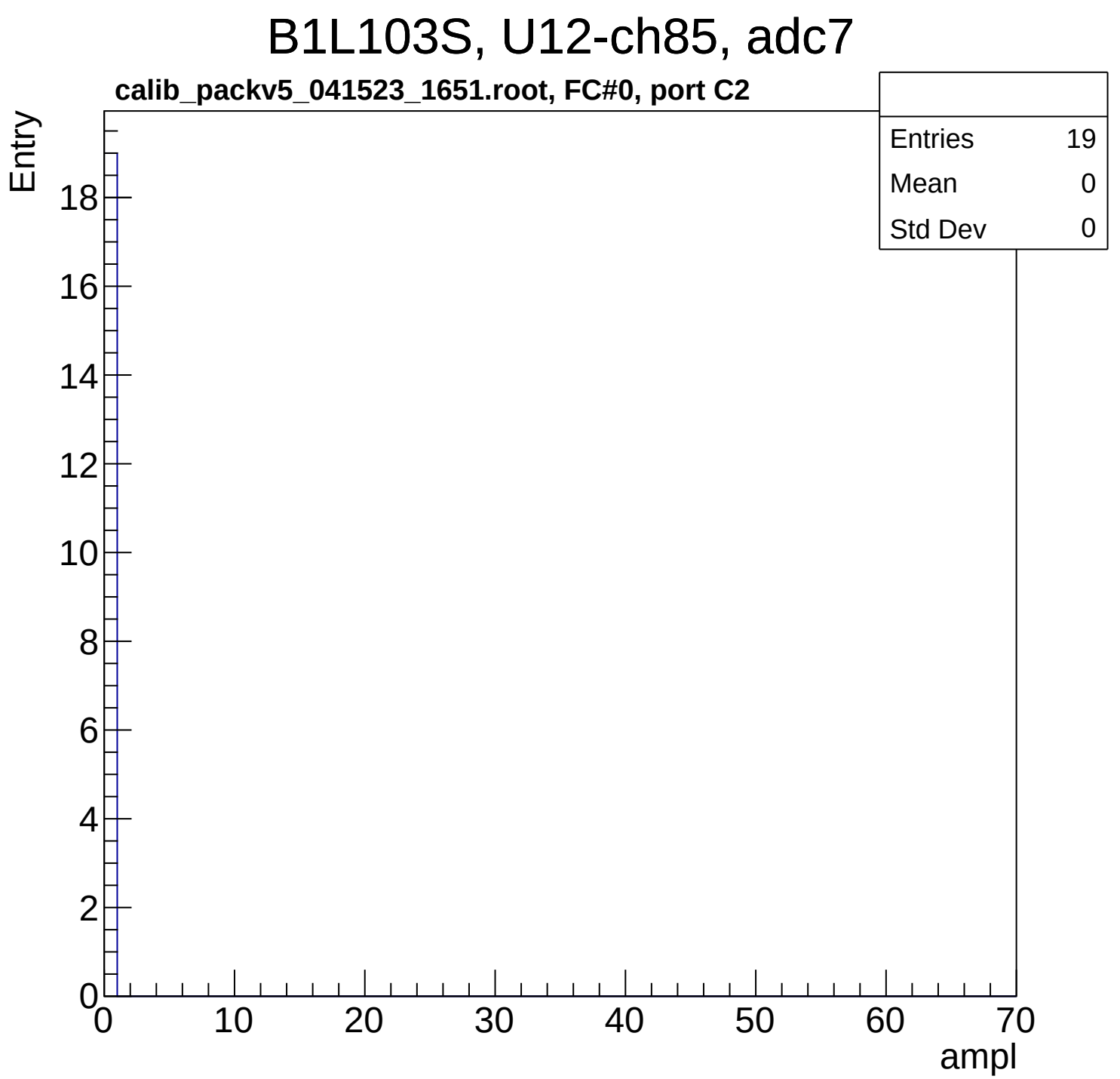
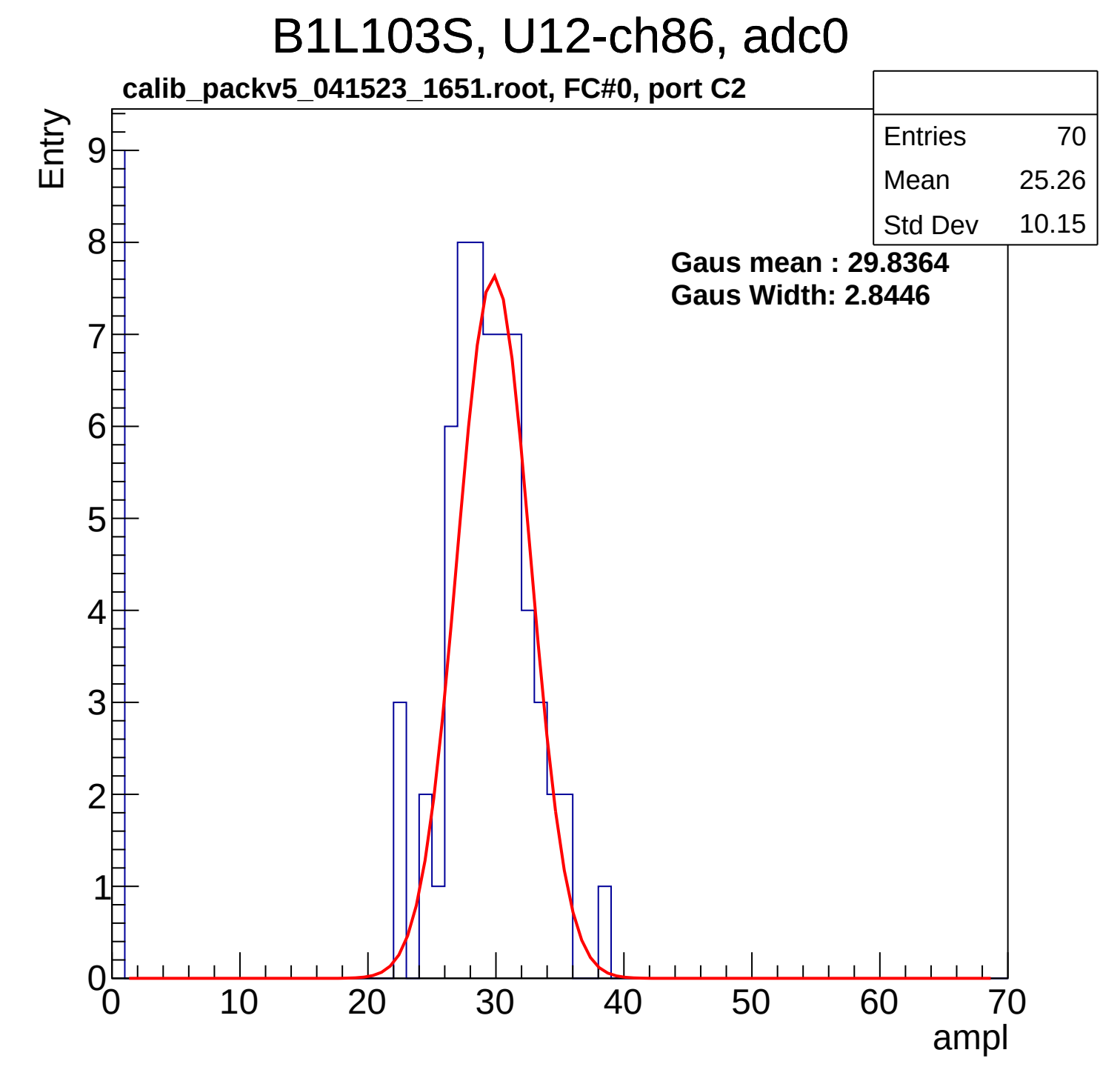
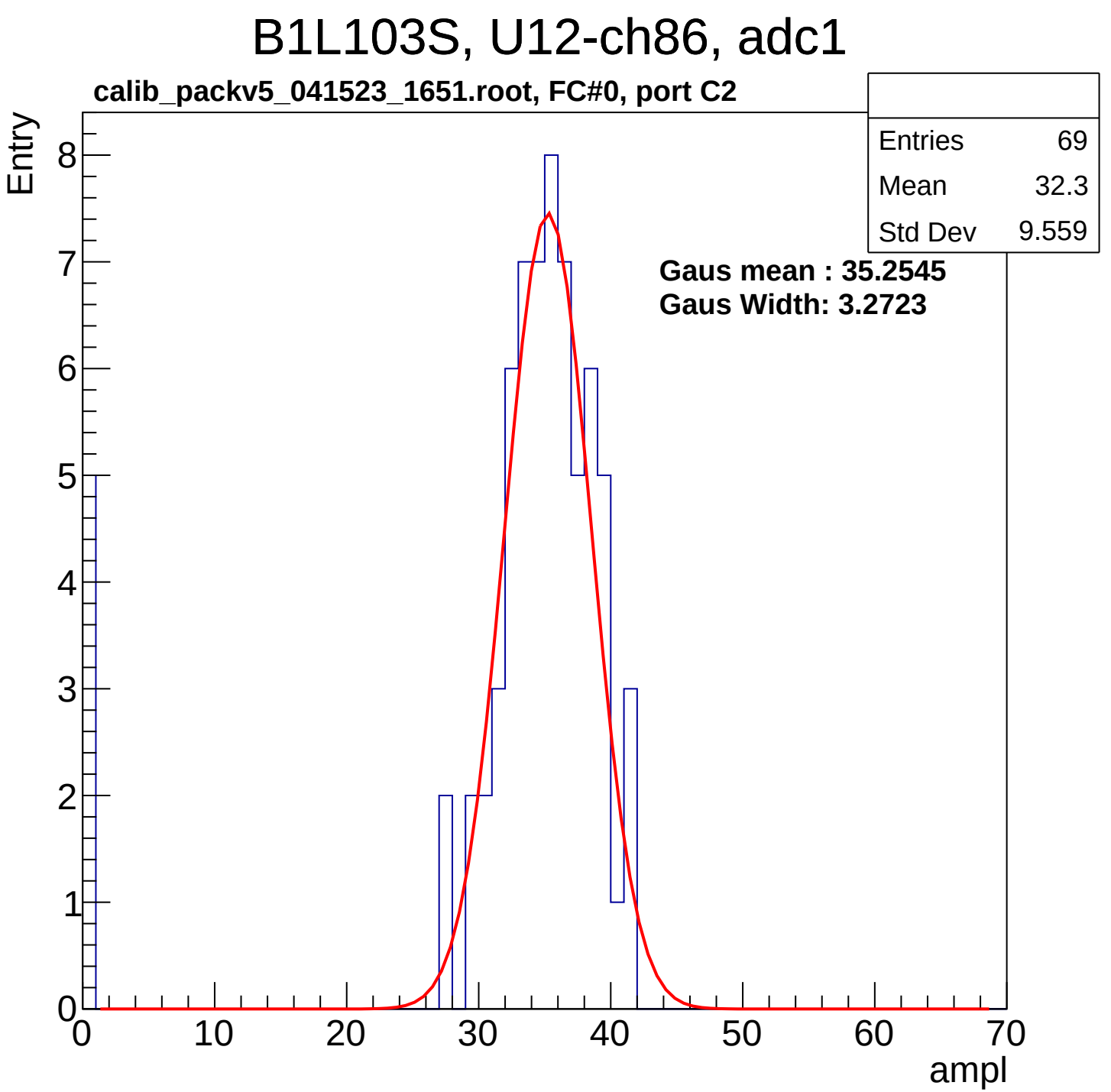

B1L103S, U12-ch85, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 2
Mean 61.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch85, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch86, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 25.26
Std Dev 10.15
Gaus mean : 29.8364
Gaus Width: 2.8446
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch86, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 32.3
Std Dev 9.559
Gaus mean : 35.2545
Gaus Width: 3.2723
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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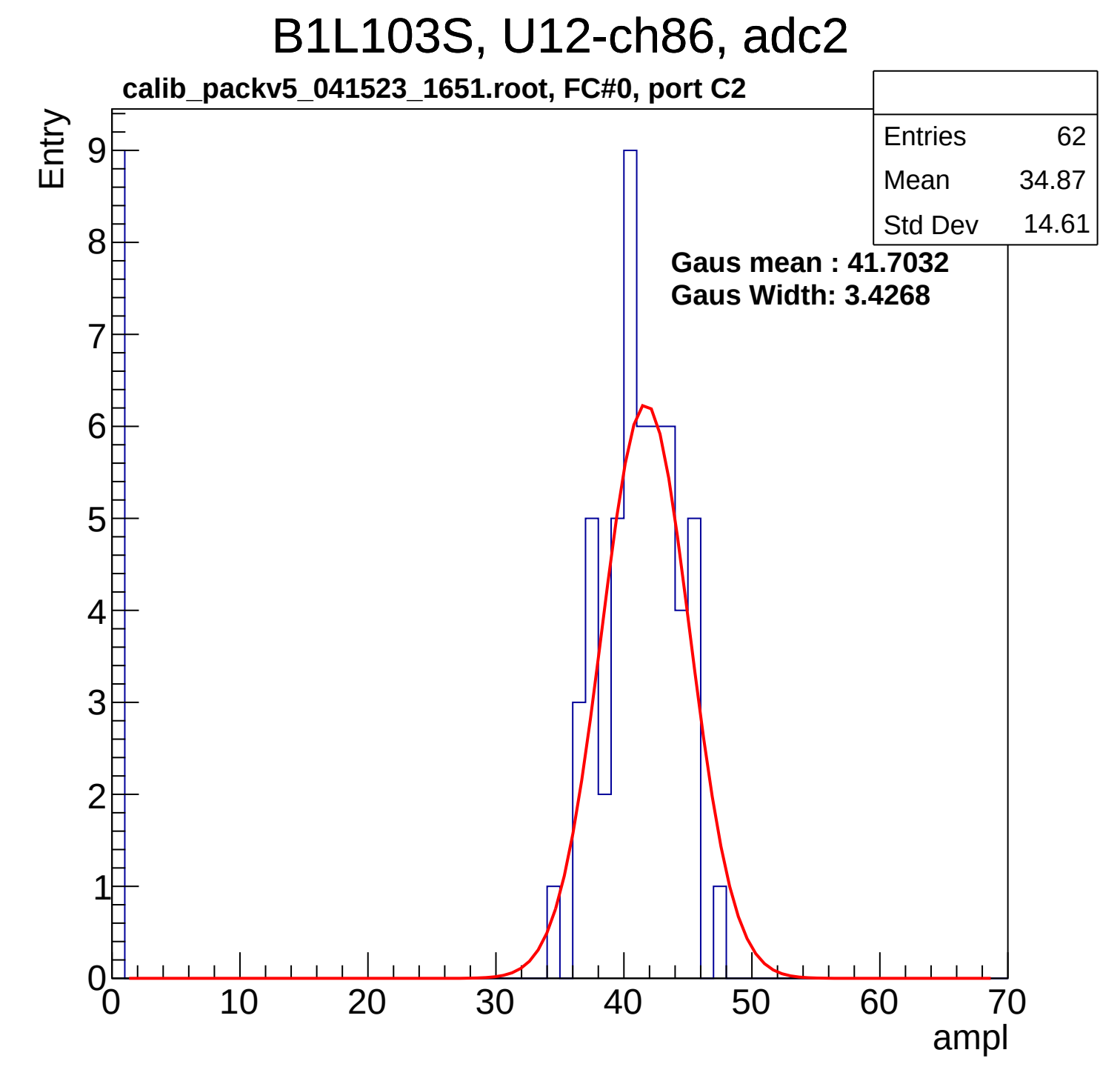
B1L103S, U12-ch86, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 34.87
Std Dev 14.61
Gaus mean : 41.7032
Gaus Width: 3.4268
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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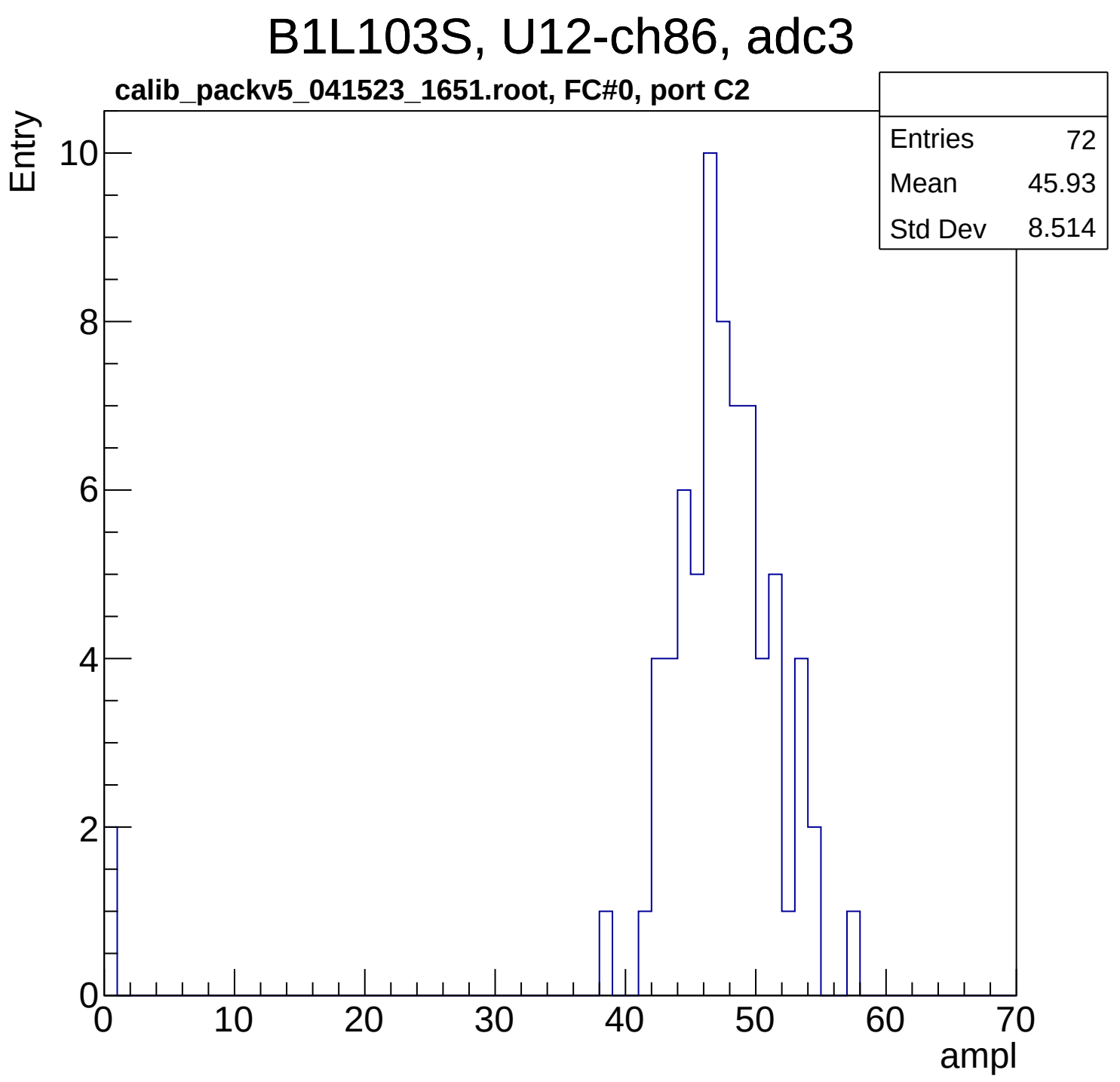
B1L103S, U12-ch86, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 45.93
Std Dev 8.514
Entry
ampl
0
2
4
6
8
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0
10
20
30
40
50
60
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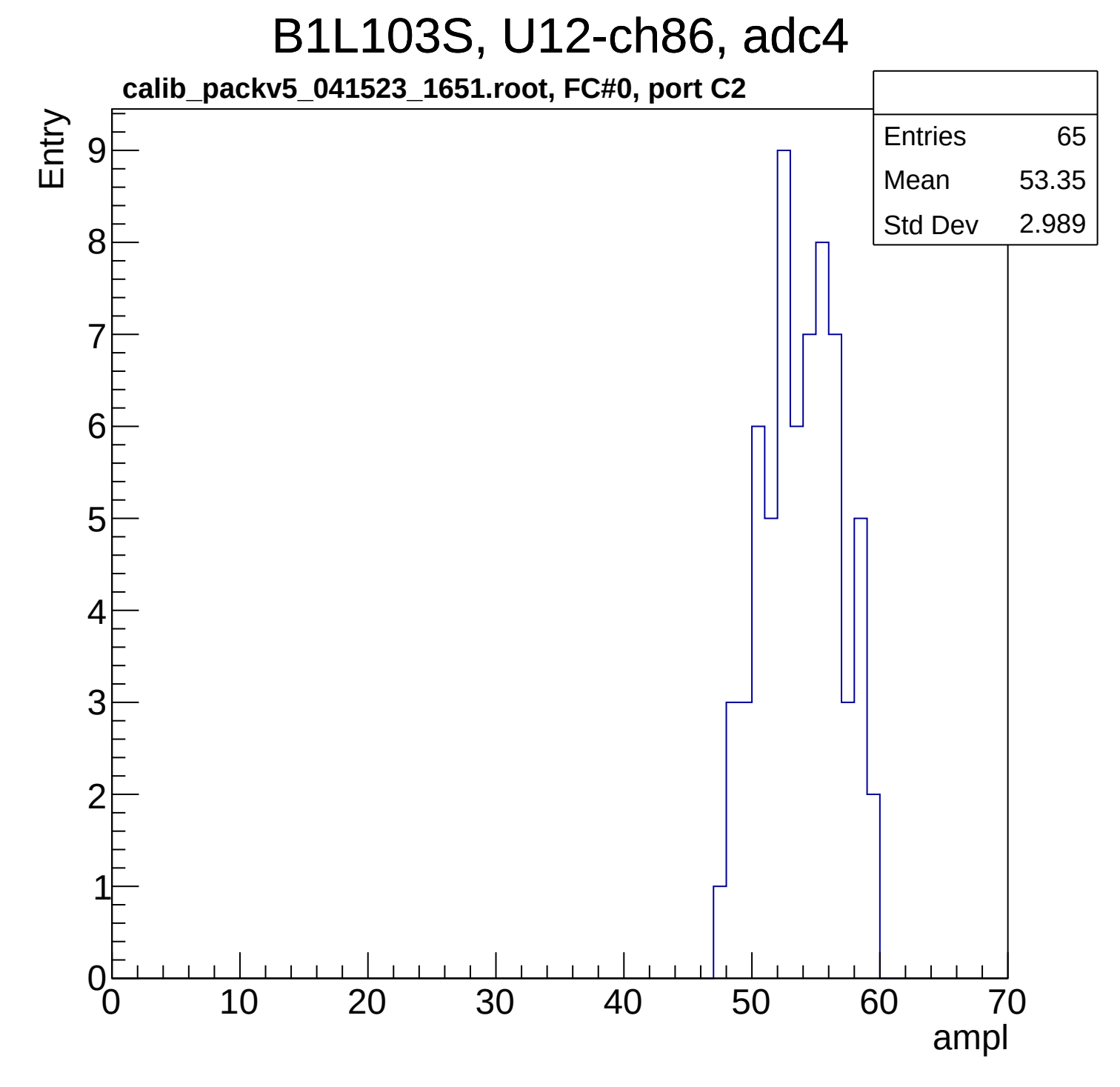
B1L103S, U12-ch86, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 53.35
Std Dev 2.989
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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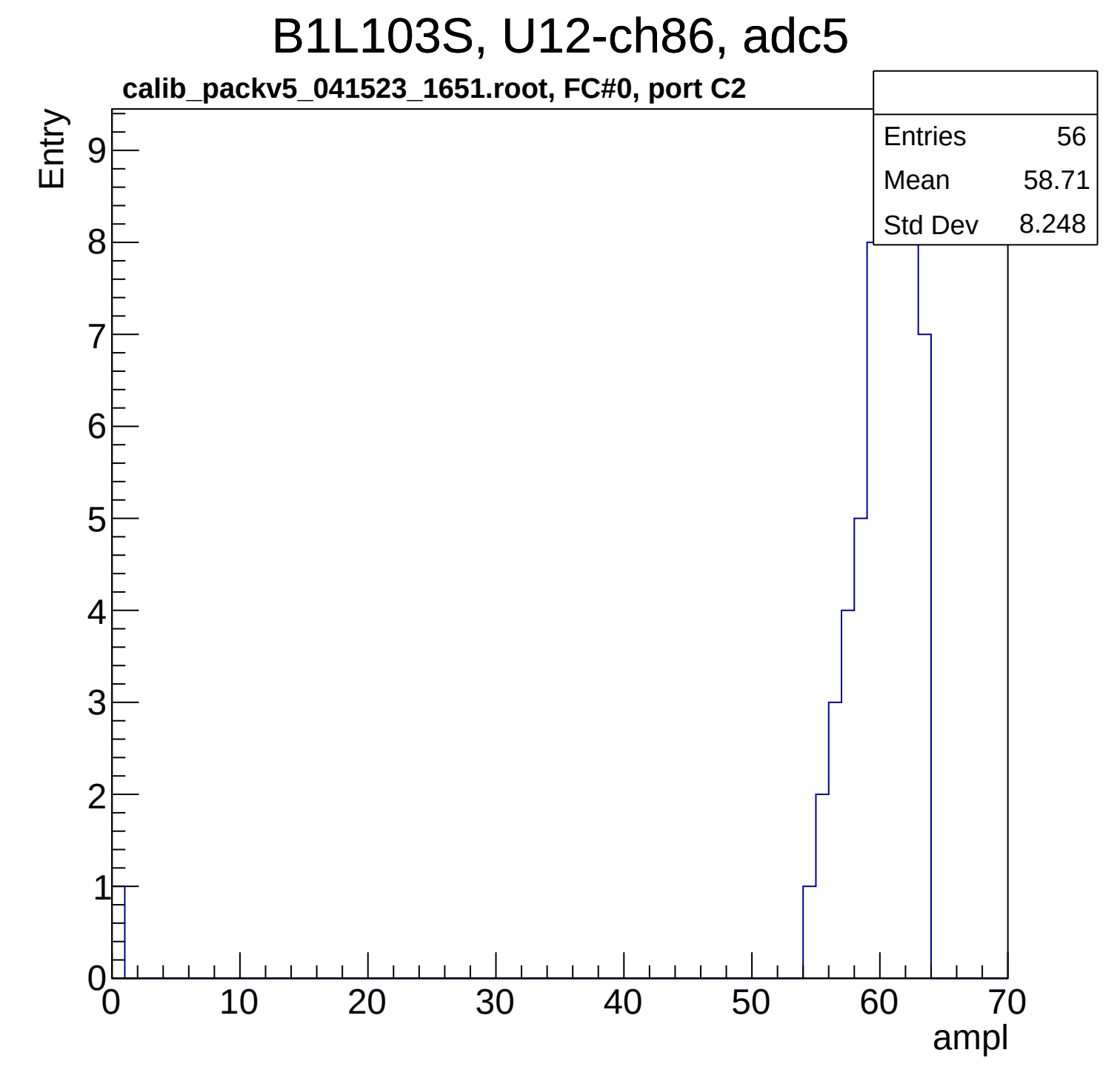
B1L103S, U12-ch86, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 58.71
Std Dev 8.248
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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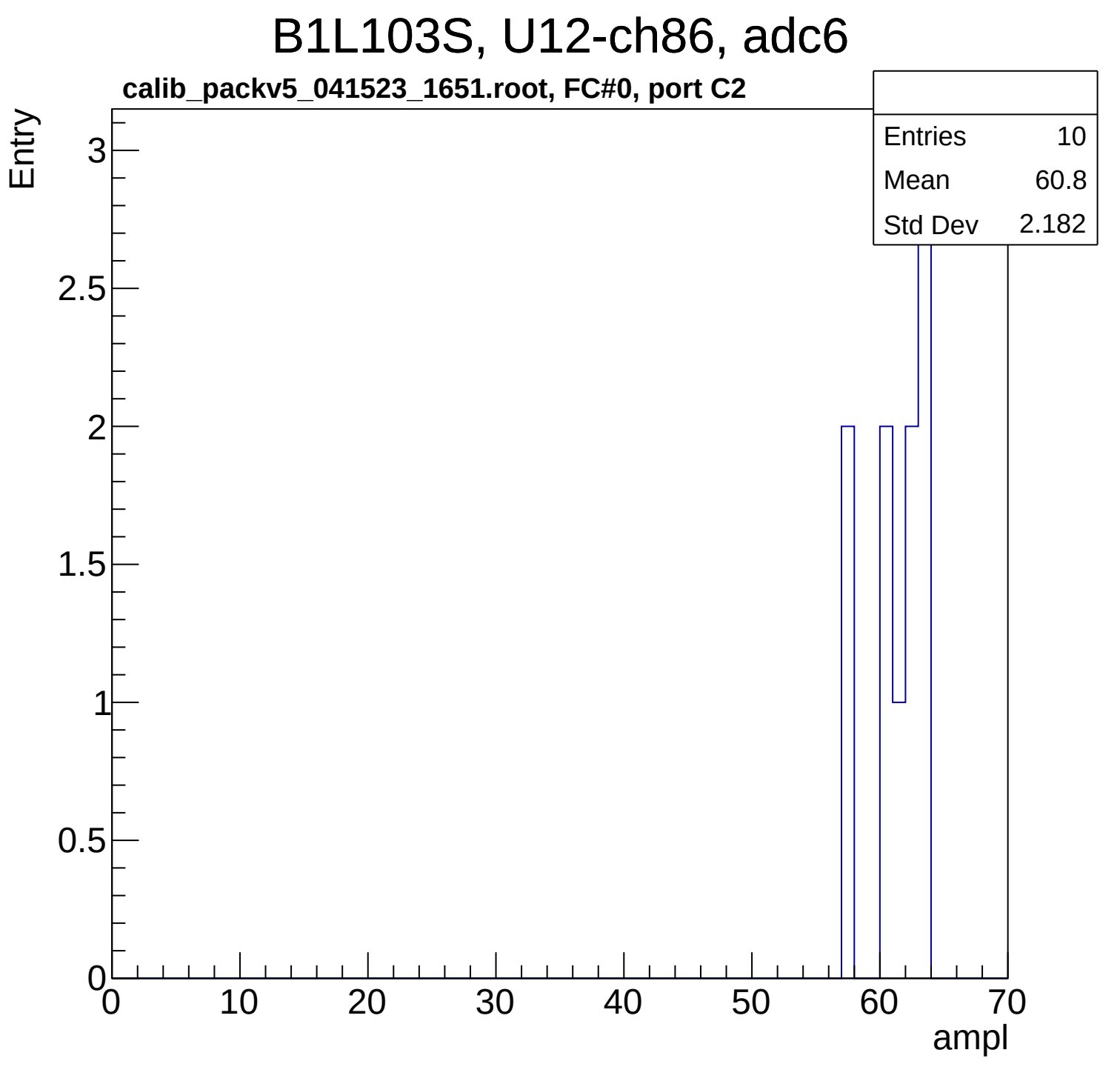
B1L103S, U12-ch86, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 60.8
Std Dev 2.182
Entry
ampl
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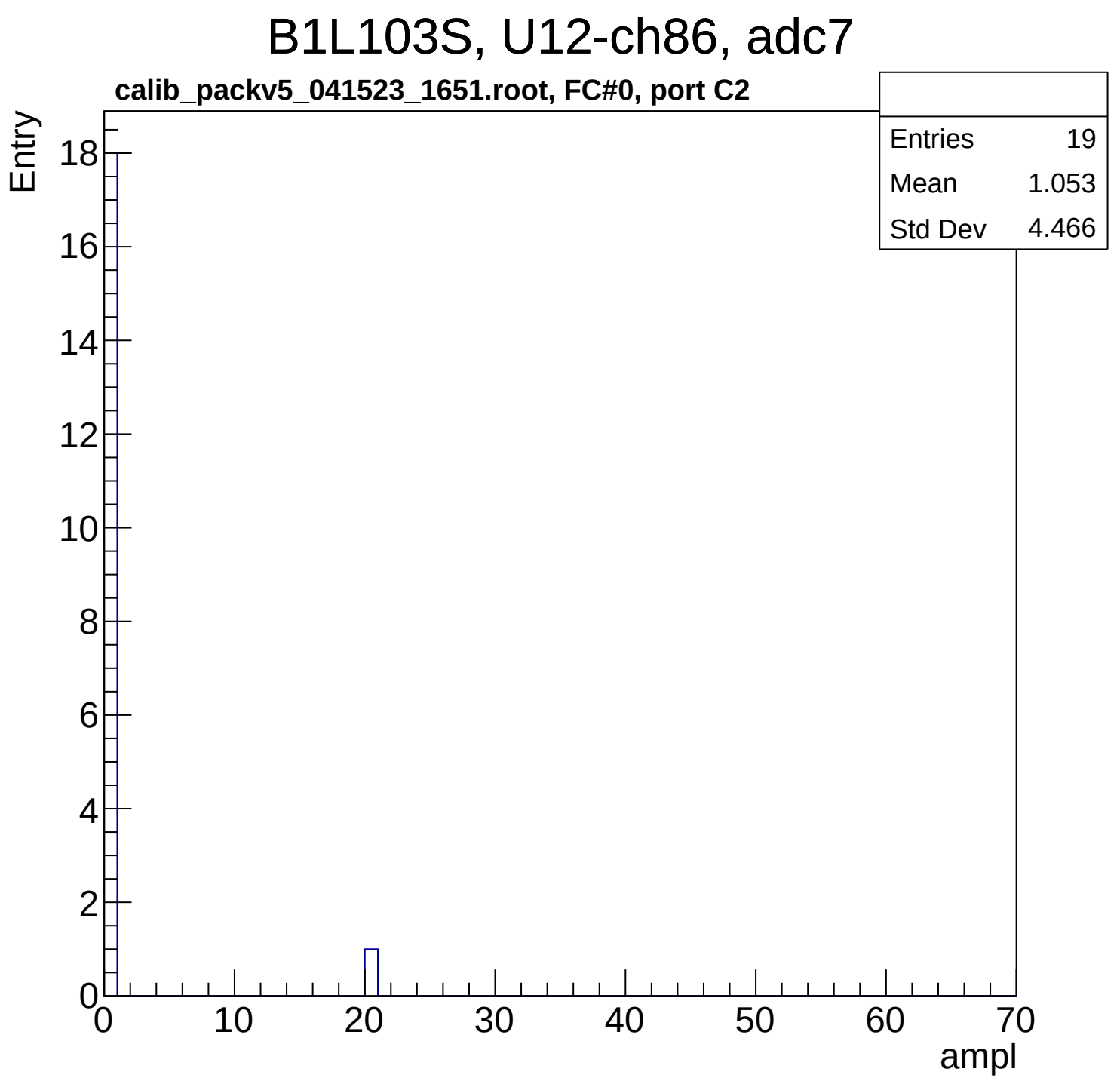
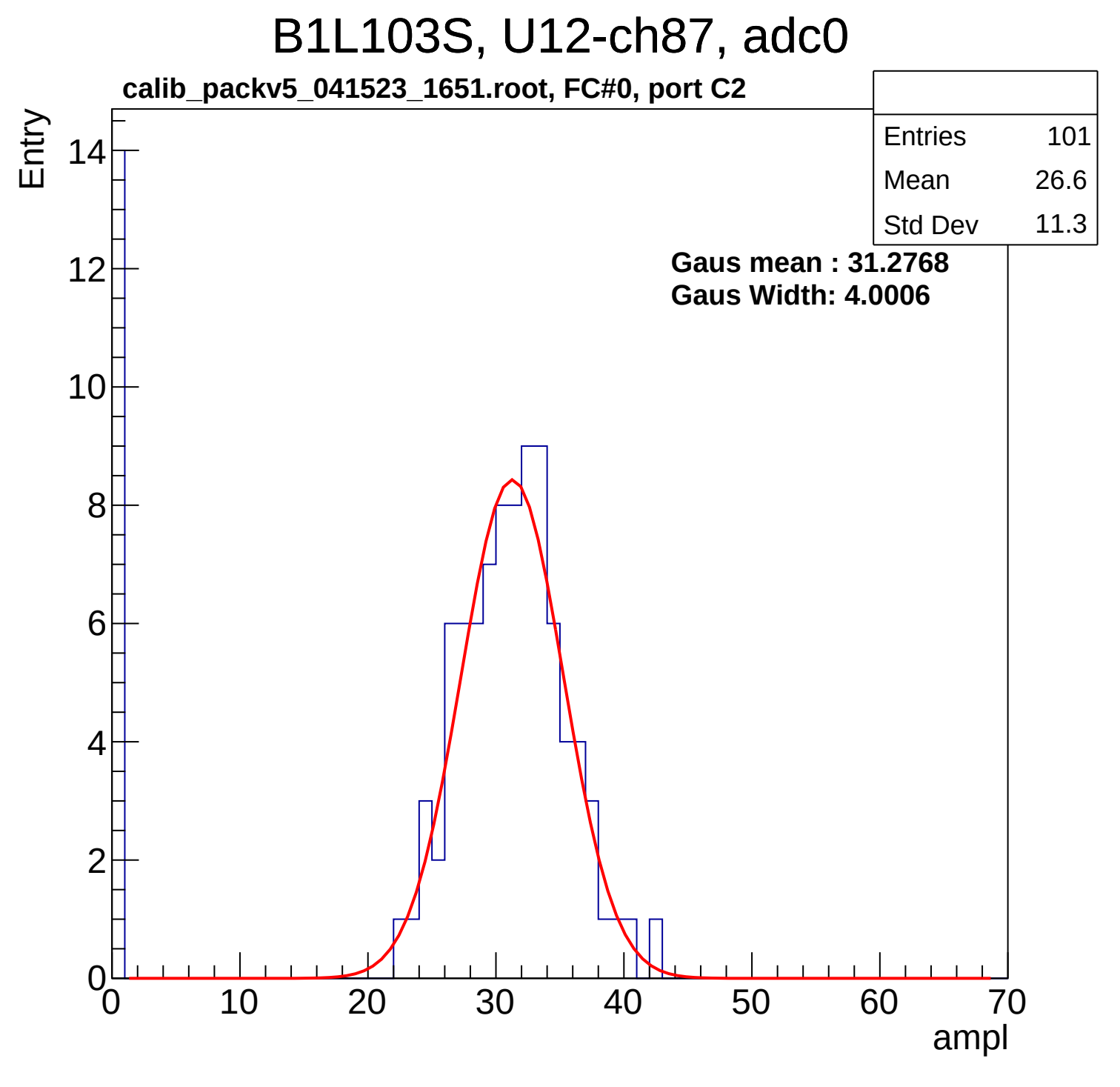
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U12-ch86, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.053
Std Dev 4.466
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch87, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 101
Mean 26.6
Std Dev 11.3
Gaus mean : 31.2768
Gaus Width: 4.0006
Entry
ampl
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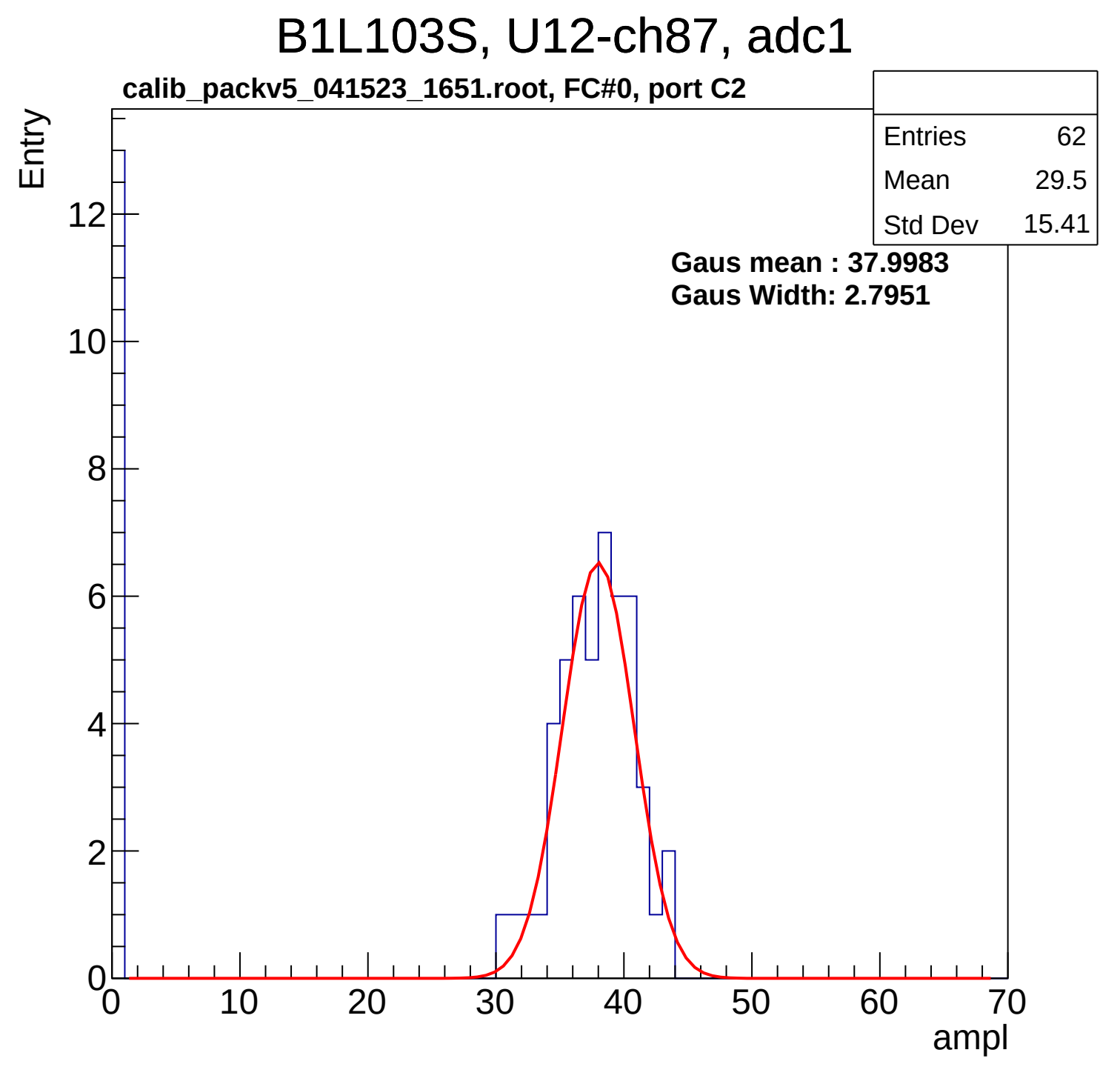
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L103S, U12-ch87, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 29.5
Std Dev 15.41
Gaus mean : 37.9983
Gaus Width: 2.7951
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
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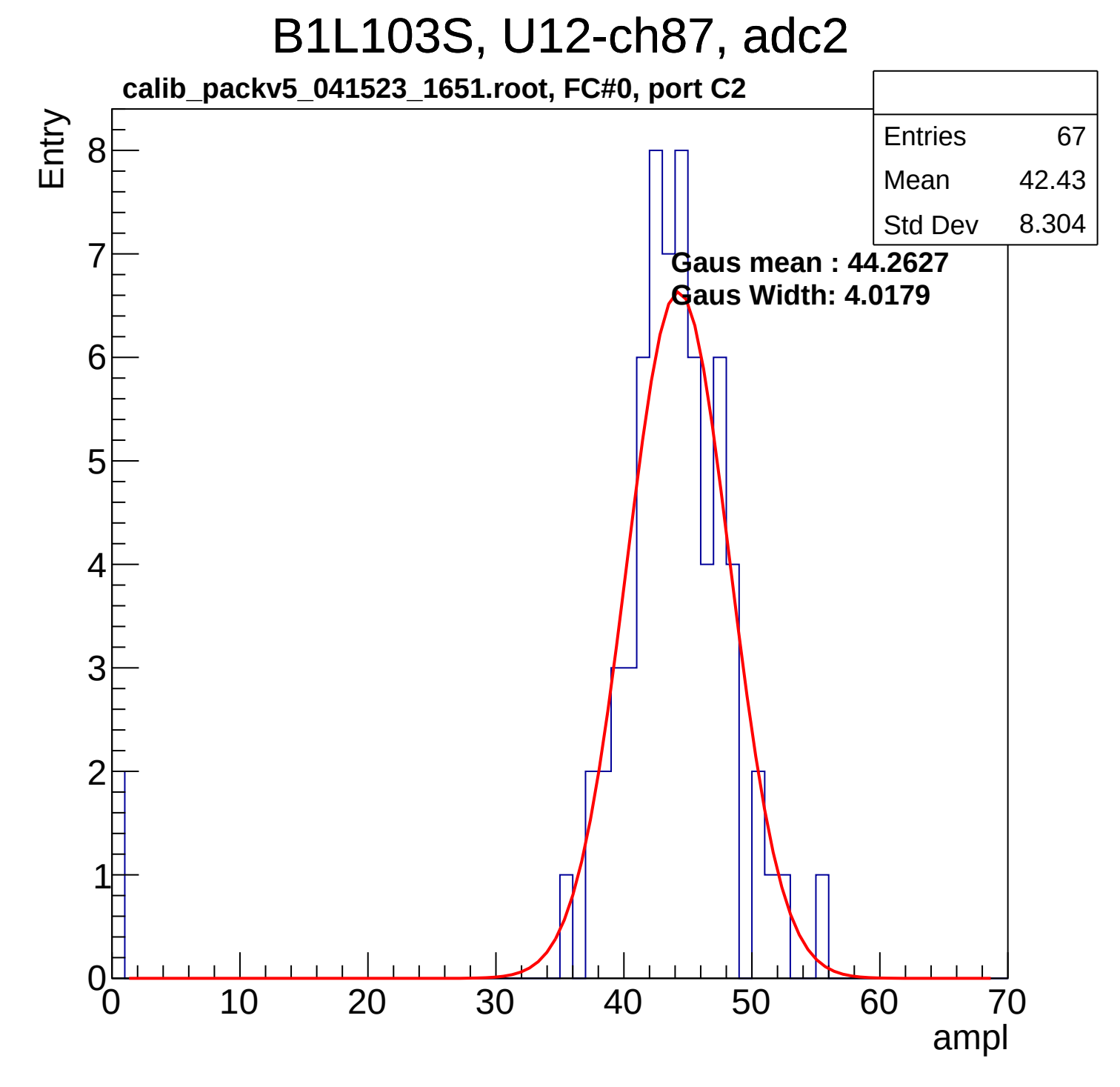
B1L103S, U12-ch87, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 42.43
Std Dev 8.304
Gaus mean : 44.2627
Gaus Width: 4.0179
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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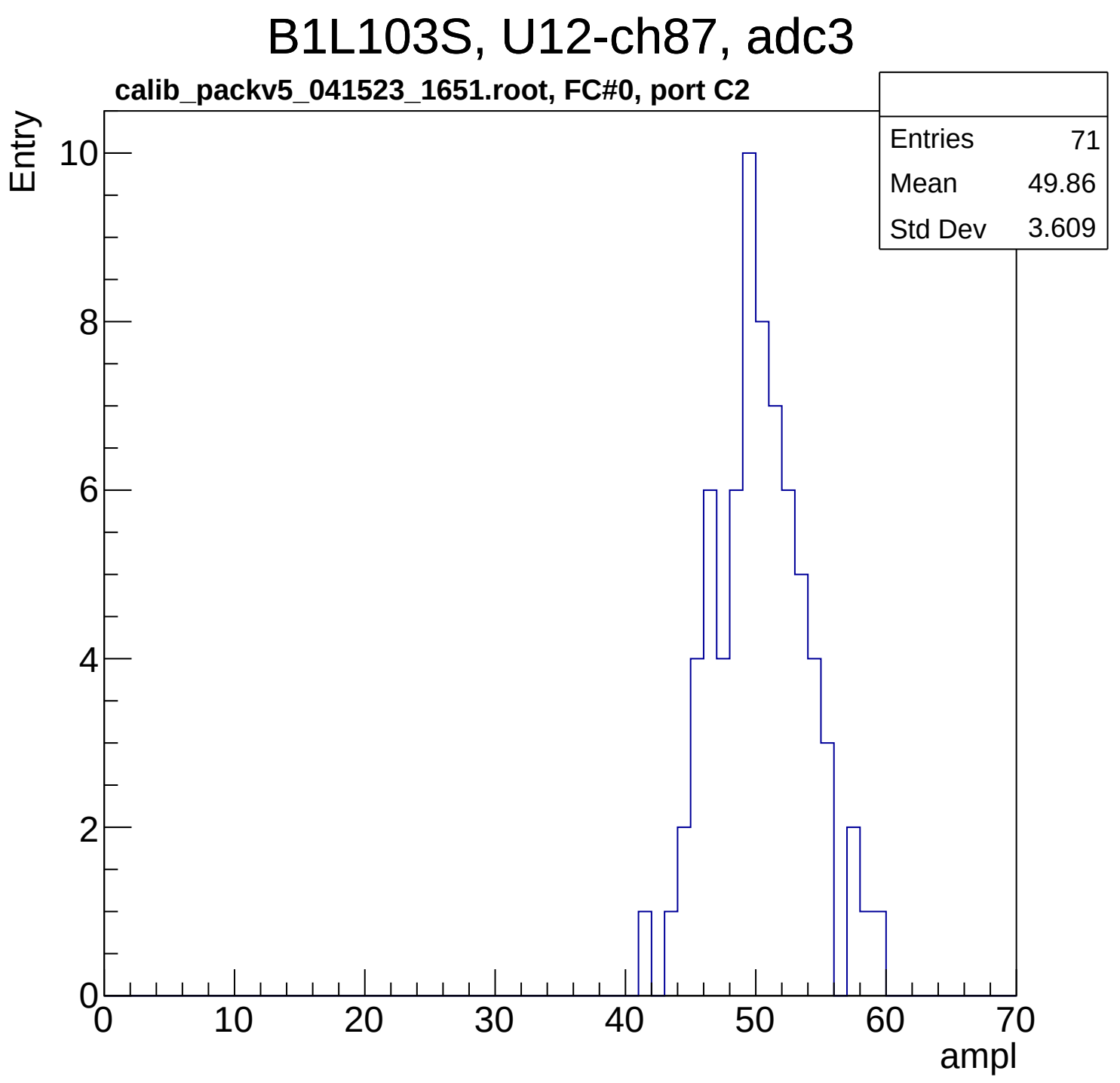
B1L103S, U12-ch87, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 49.86
Std Dev 3.609
Entry
ampl
0
2
4
6
8
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0
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40
50
60
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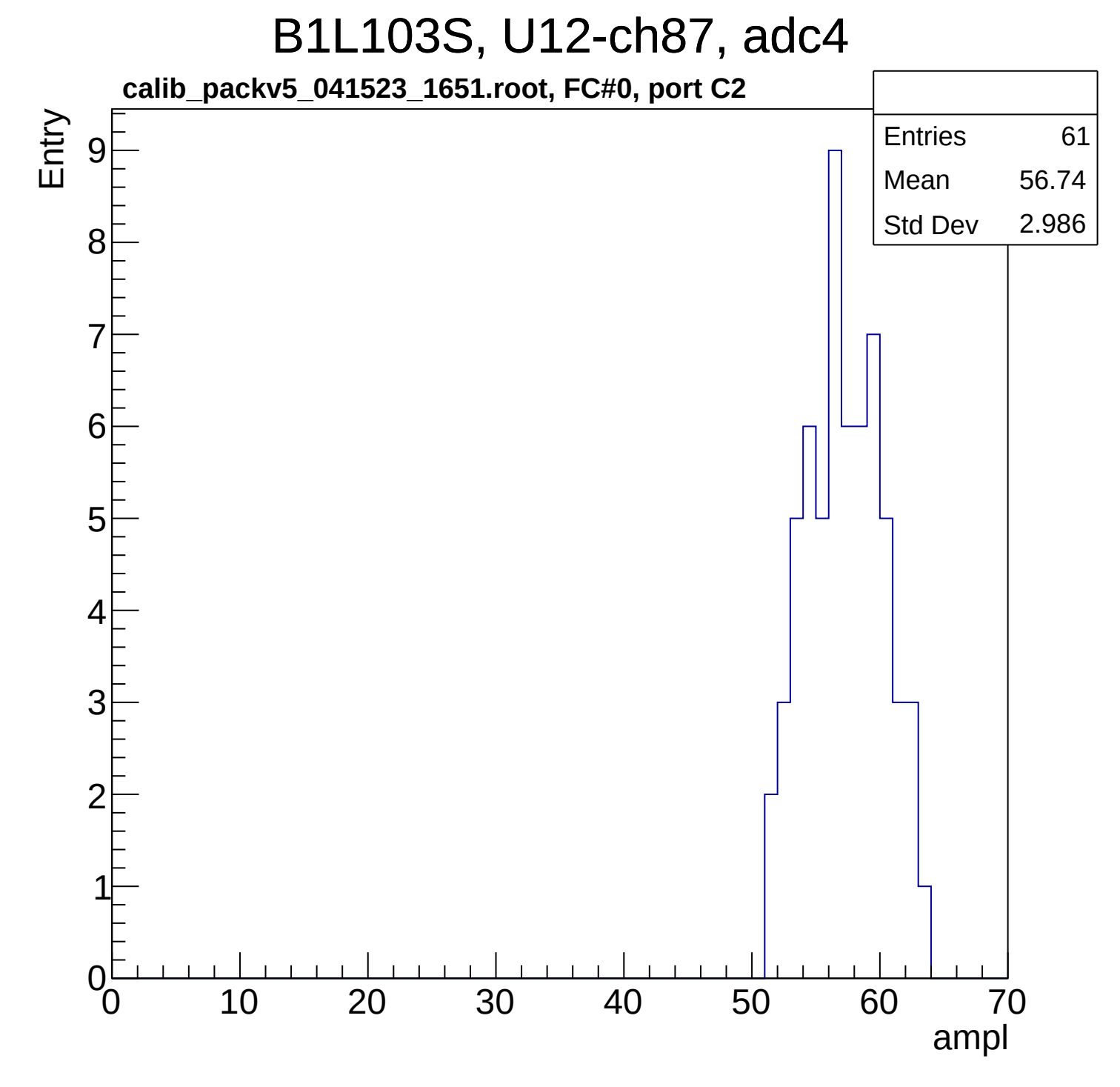
B1L103S, U12-ch87, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 56.74
Std Dev 2.986
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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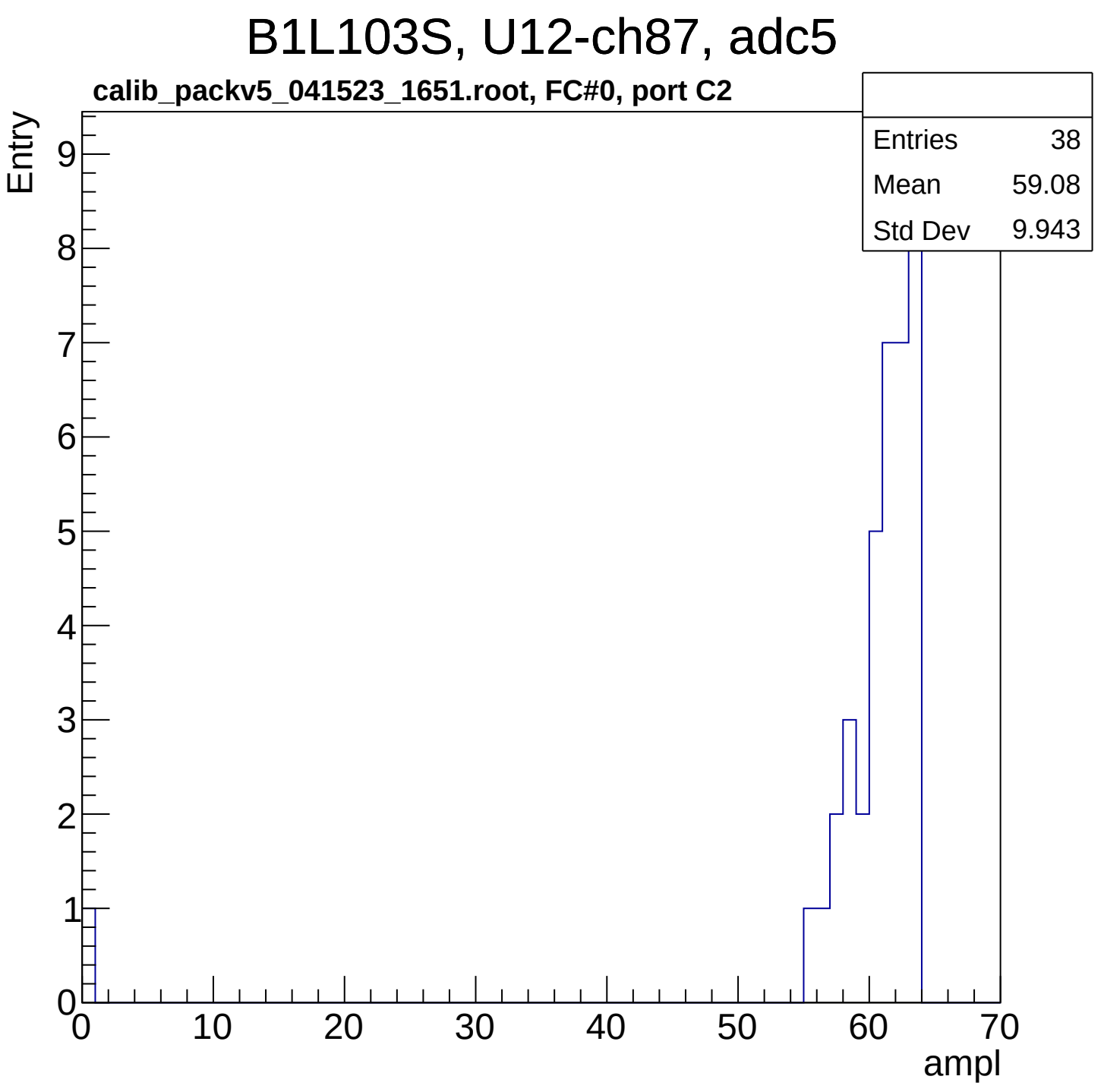
B1L103S, U12-ch87, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 38
Mean 59.08
Std Dev 9.943
Entry
ampl
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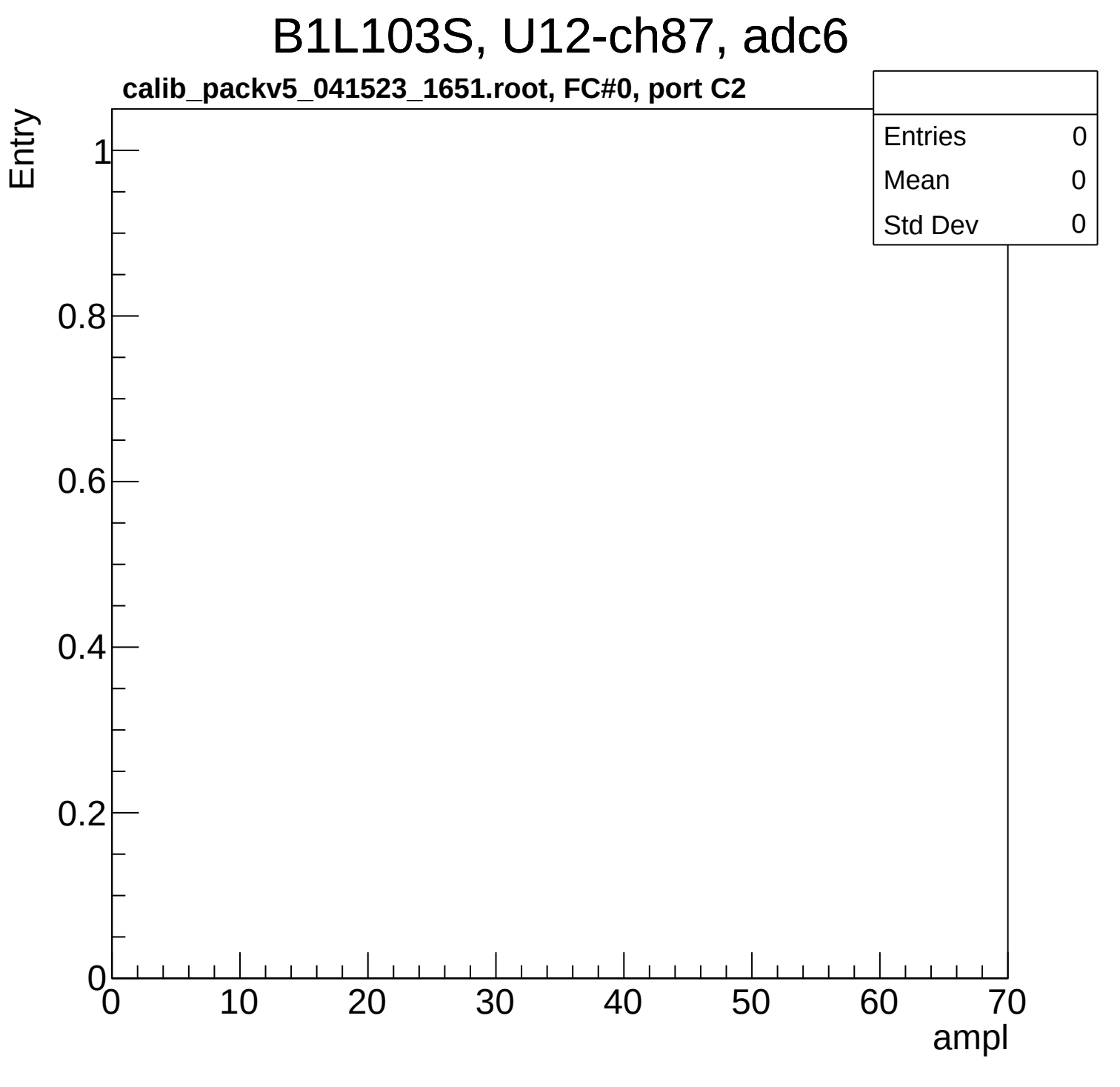
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9


B1L103S, U12-ch87, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 0
Mean 0
Std Dev 0
Entry
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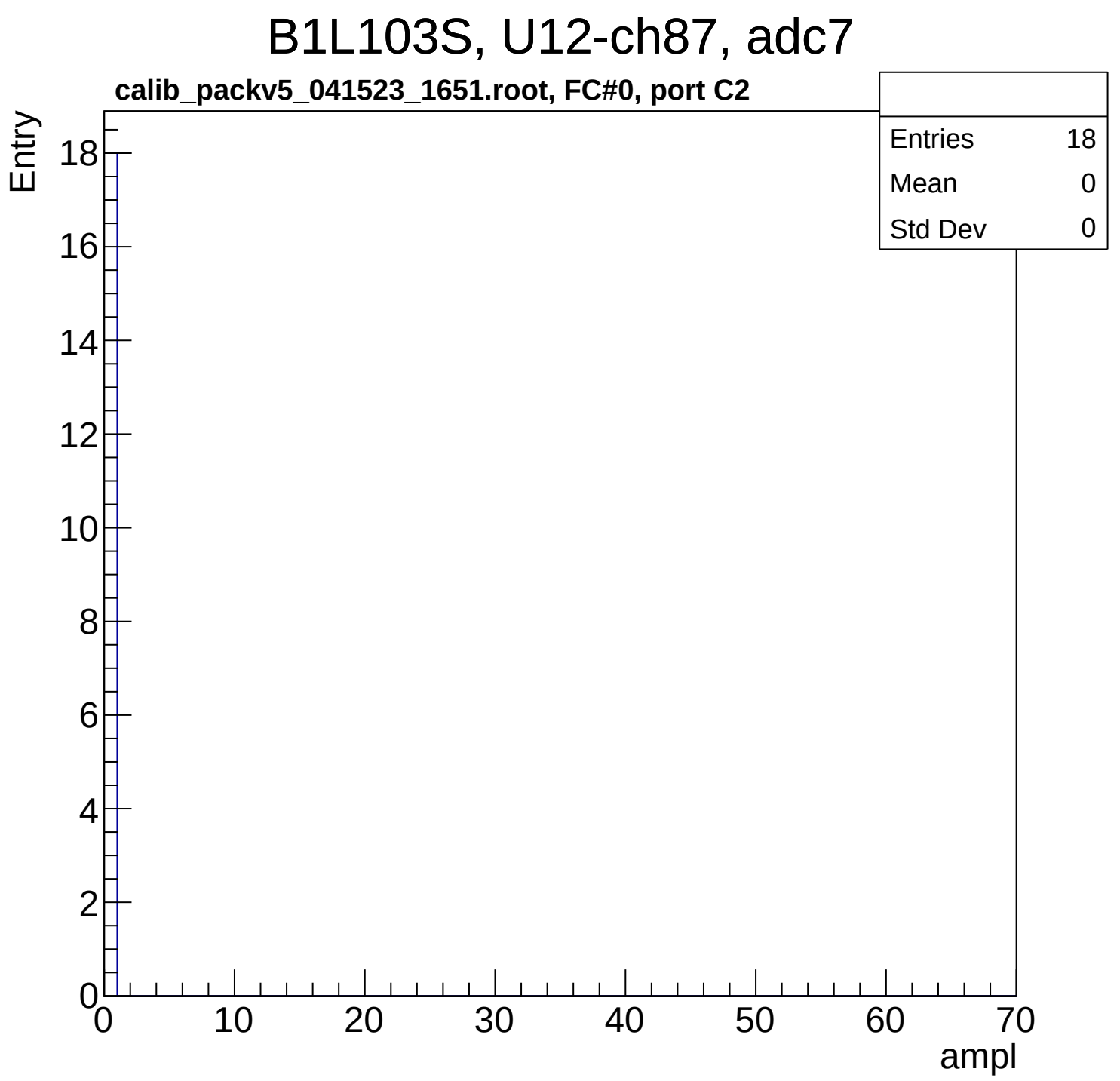
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch87, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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8
10
12
14
16
18
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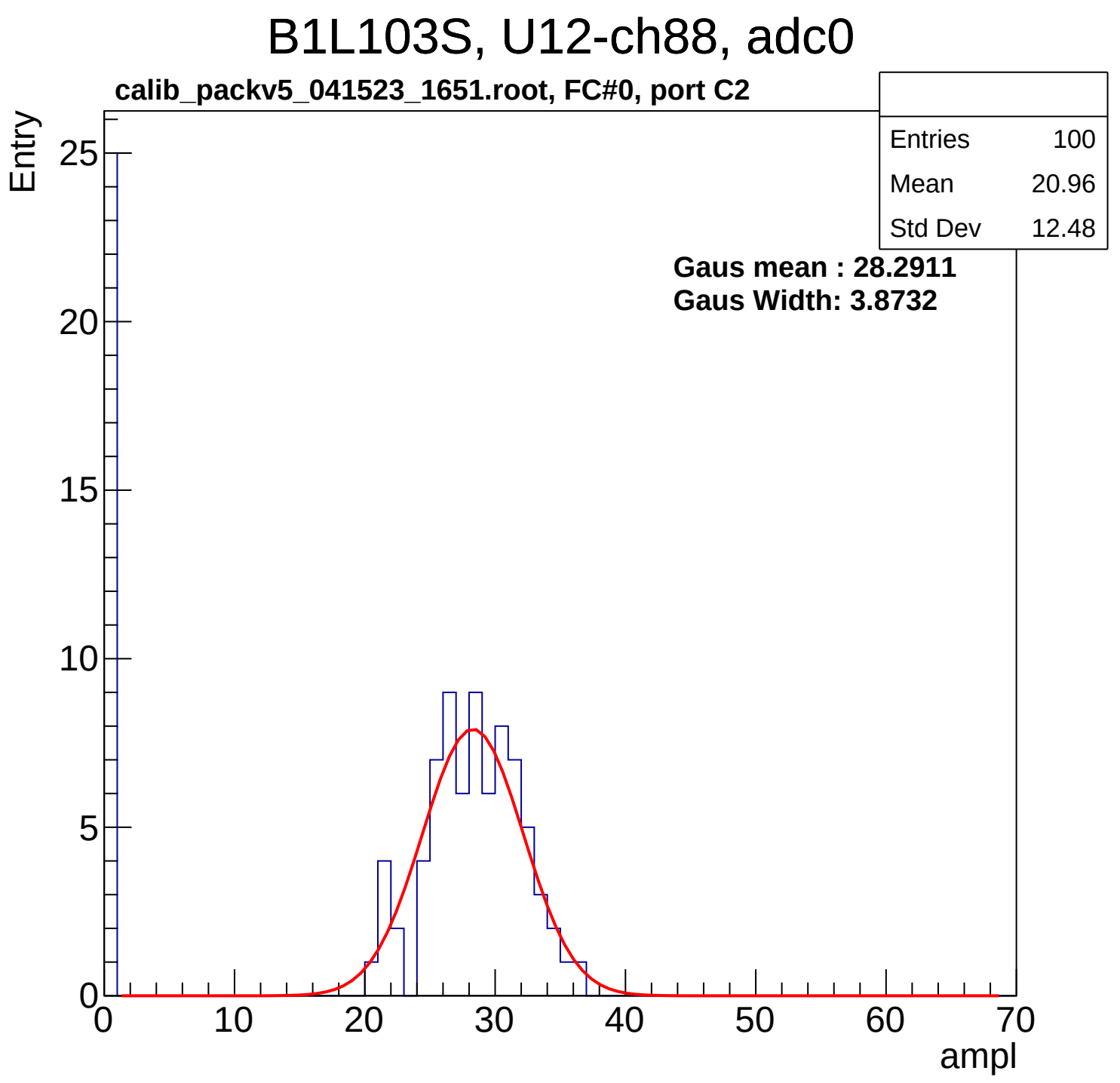
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch88, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 100
Mean 20.96
Std Dev 12.48
Gaus mean : 28.2911
Gaus Width: 3.8732
Entry
ampl
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5
10
15
20
25
0
10
20
30
40
50
60
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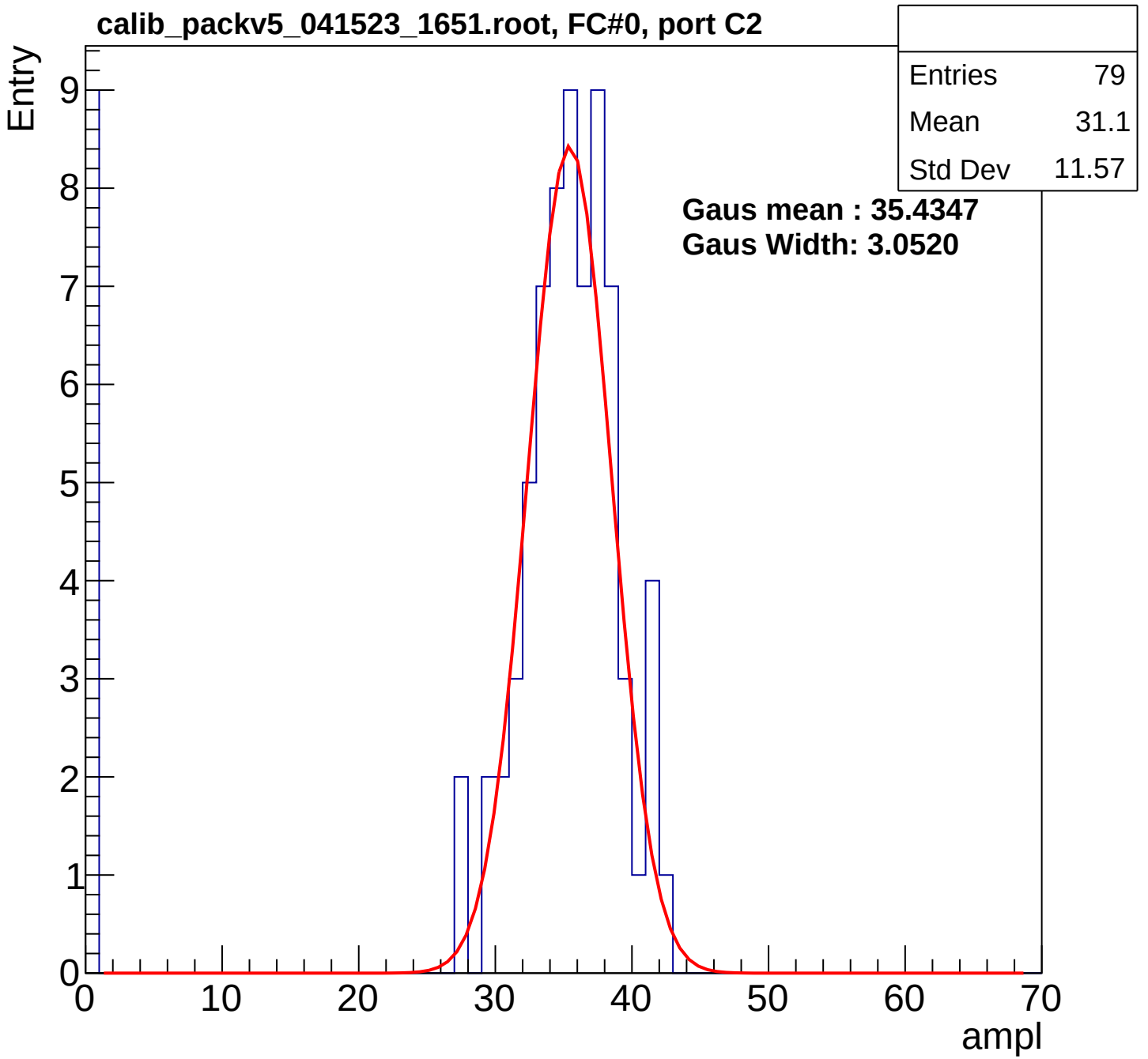
B1L103S, U12-ch88, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 31.1
Std Dev 11.57
Gaus mean : 35.4347
Gaus Width: 3.0520
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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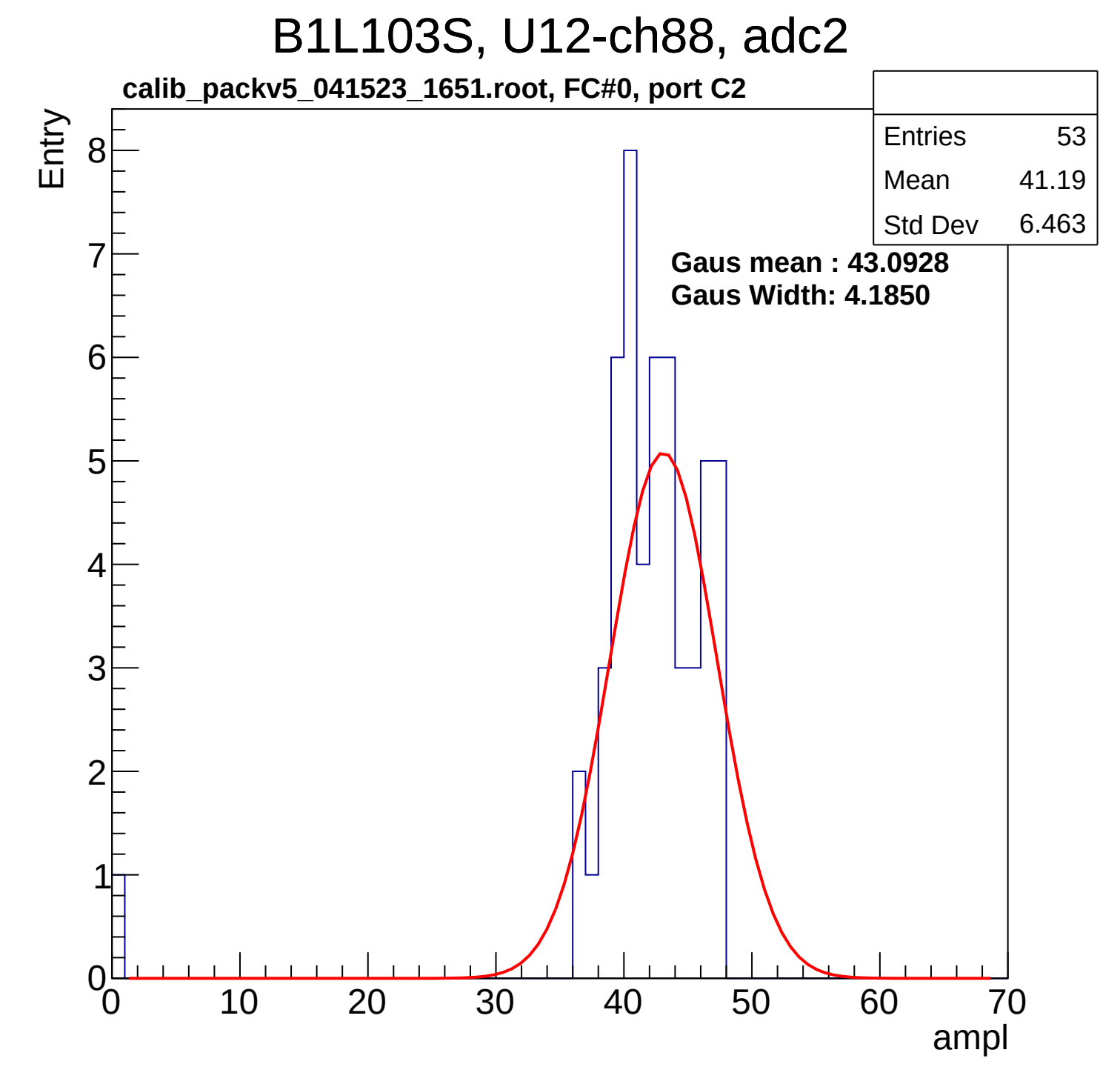
B1L103S, U12-ch88, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 41.19
Std Dev 6.463
Gaus mean : 43.0928
Gaus Width: 4.1850
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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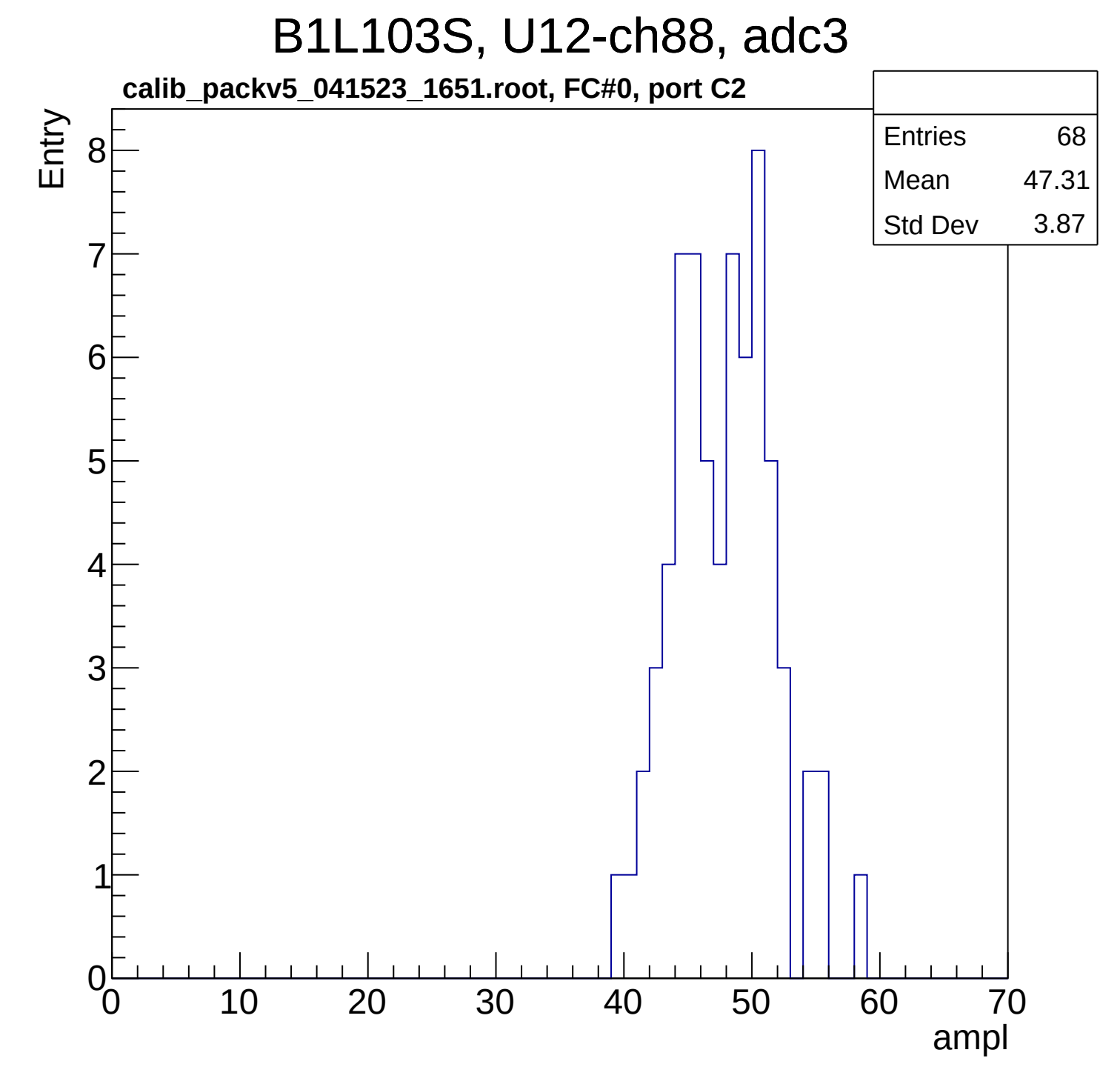
B1L103S, U12-ch88, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 47.31
Std Dev 3.87
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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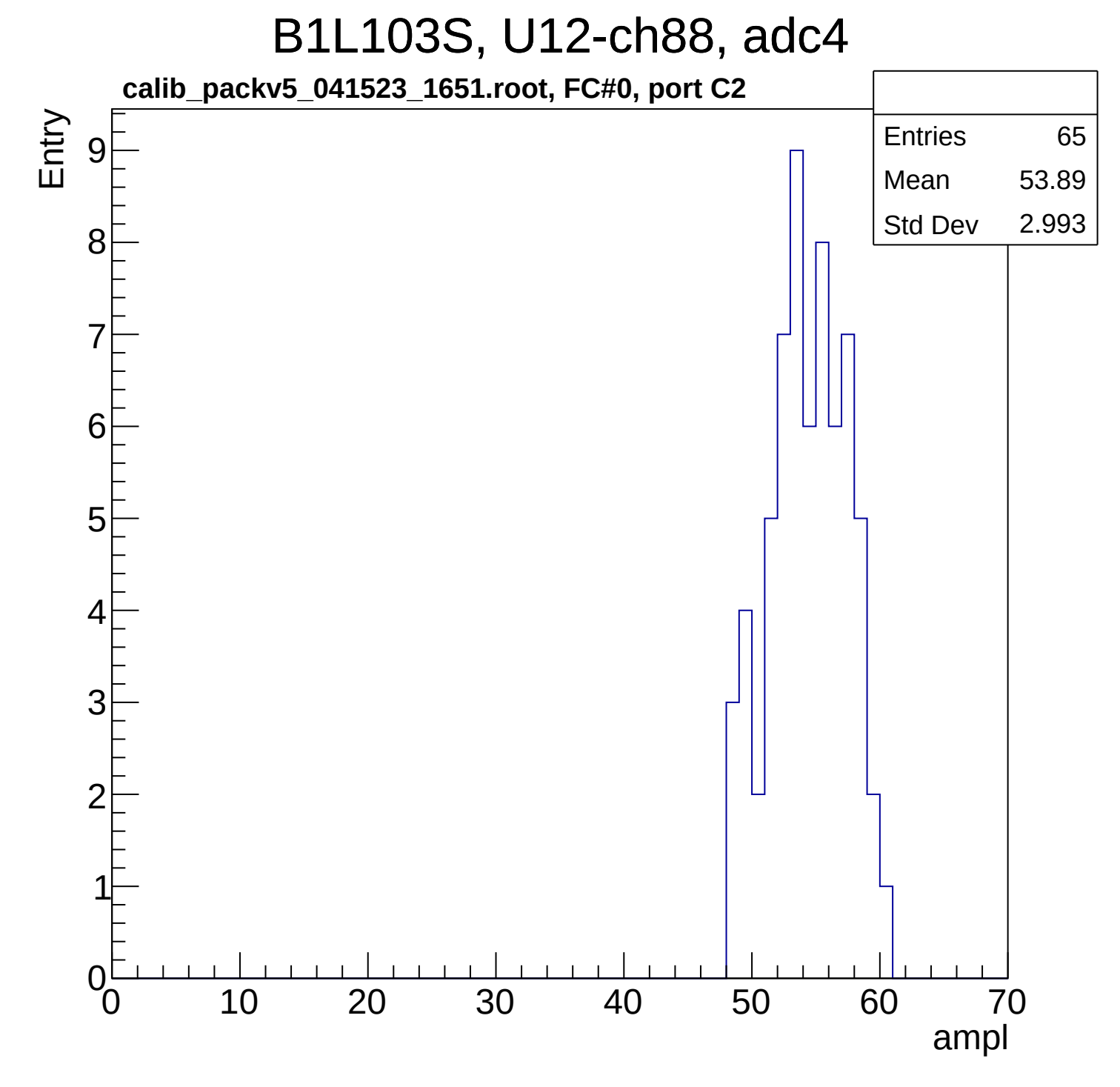
B1L103S, U12-ch88, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 53.89
Std Dev 2.993
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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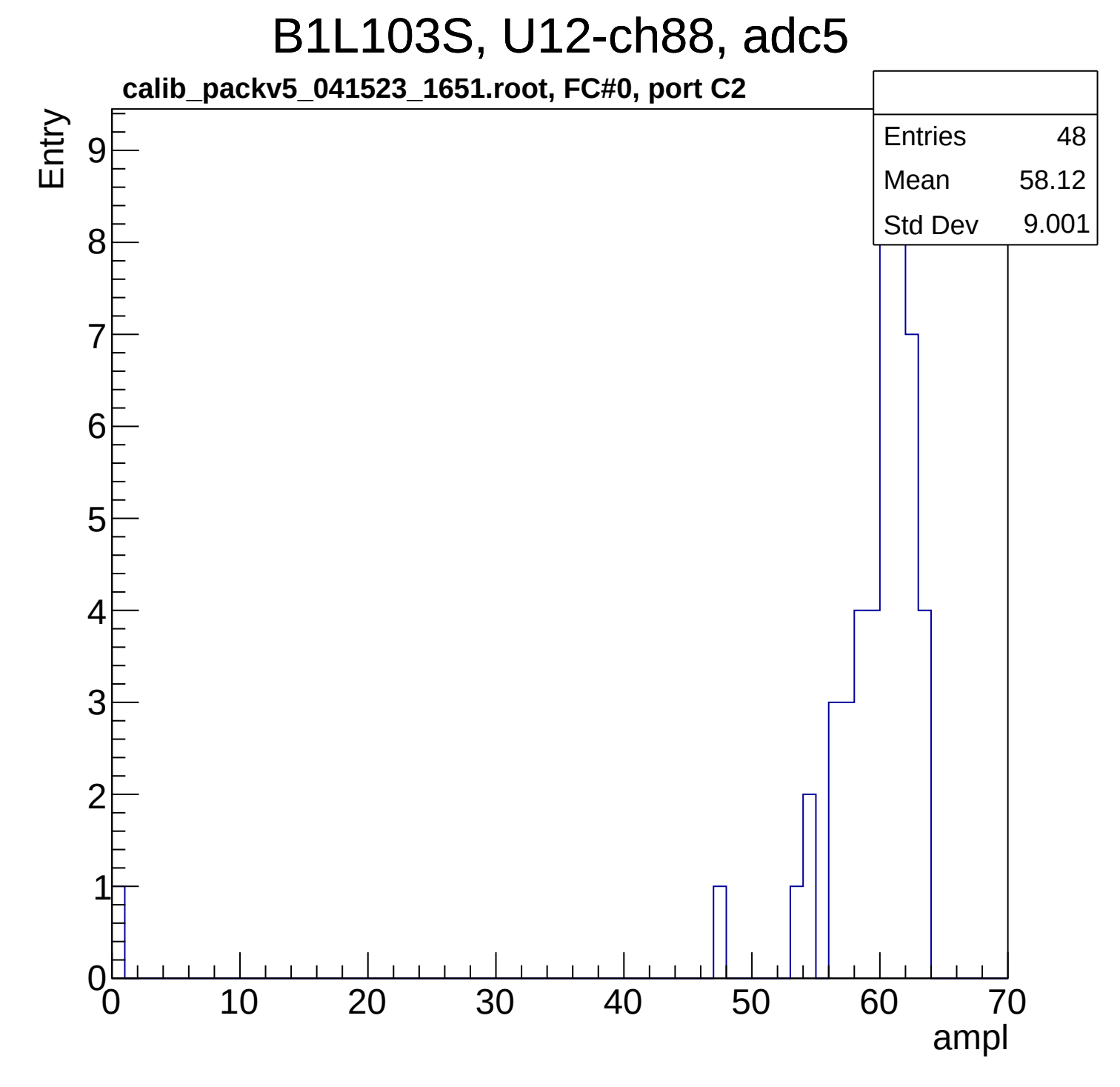
B1L103S, U12-ch88, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.12
Std Dev 9.001
Entry
ampl
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3
4
5
6
7
8
9
0
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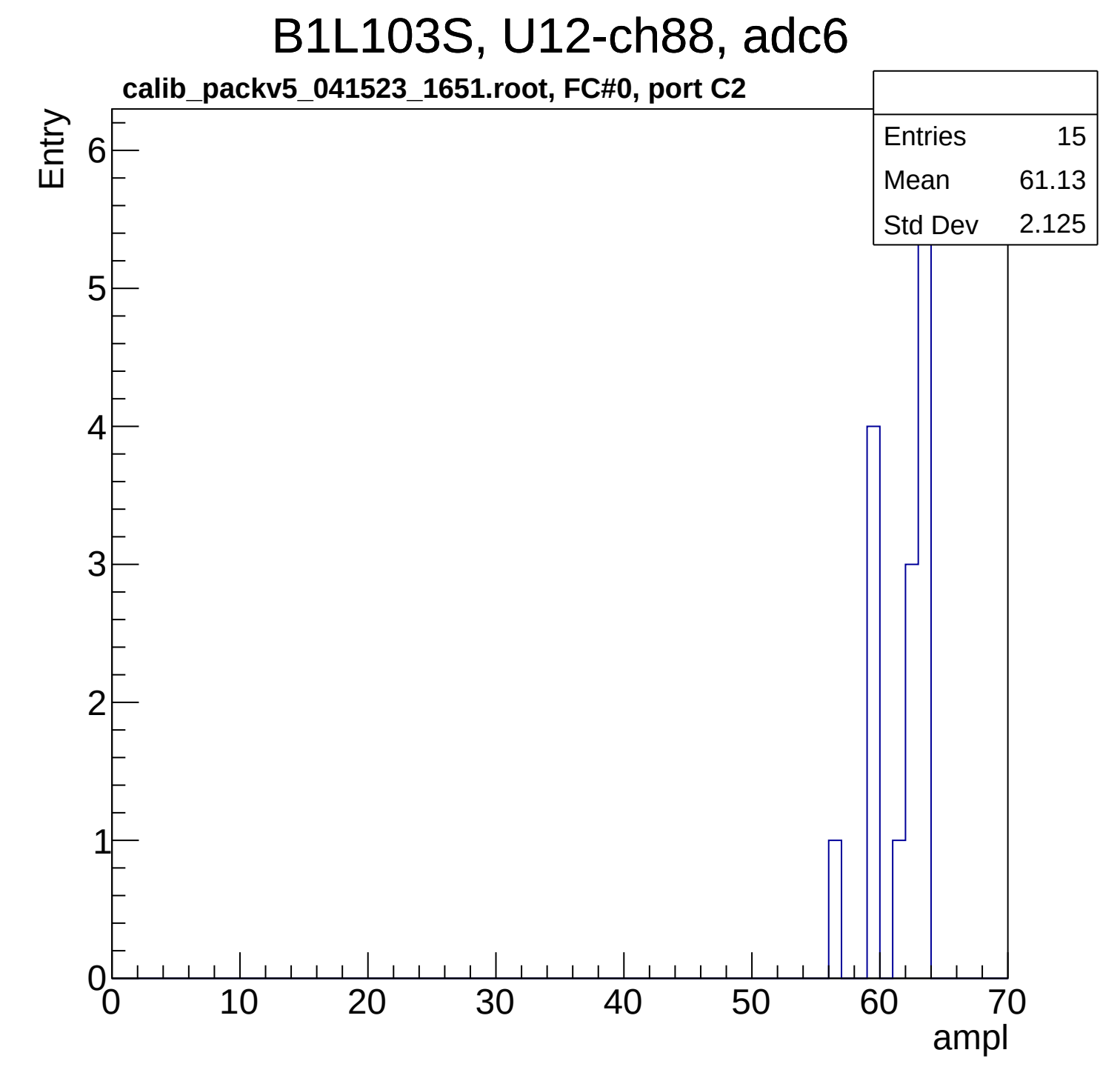
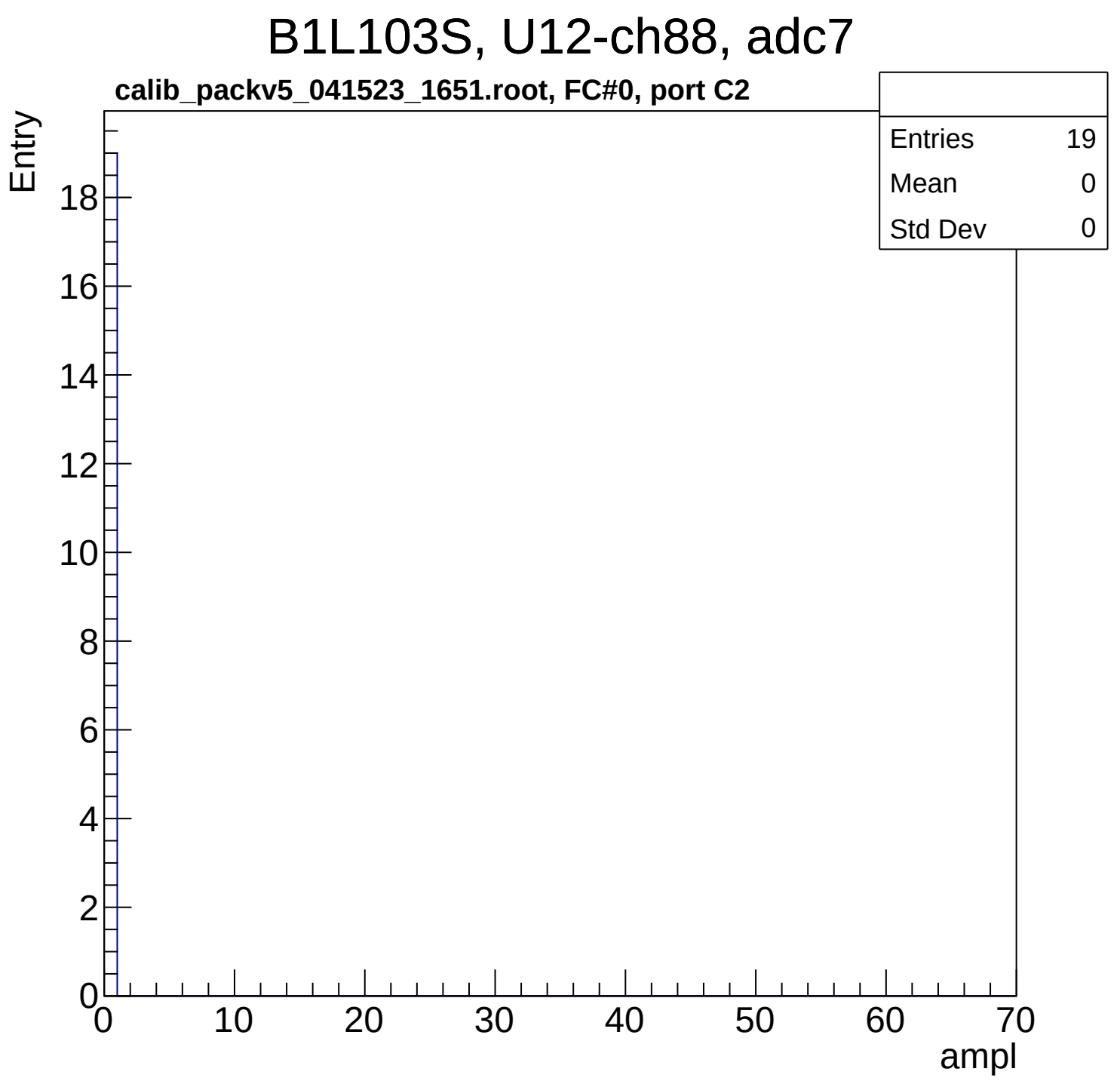

B1L103S, U12-ch88, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 15
Mean 61.13
Std Dev 2.125
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U12-ch88, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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6
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14
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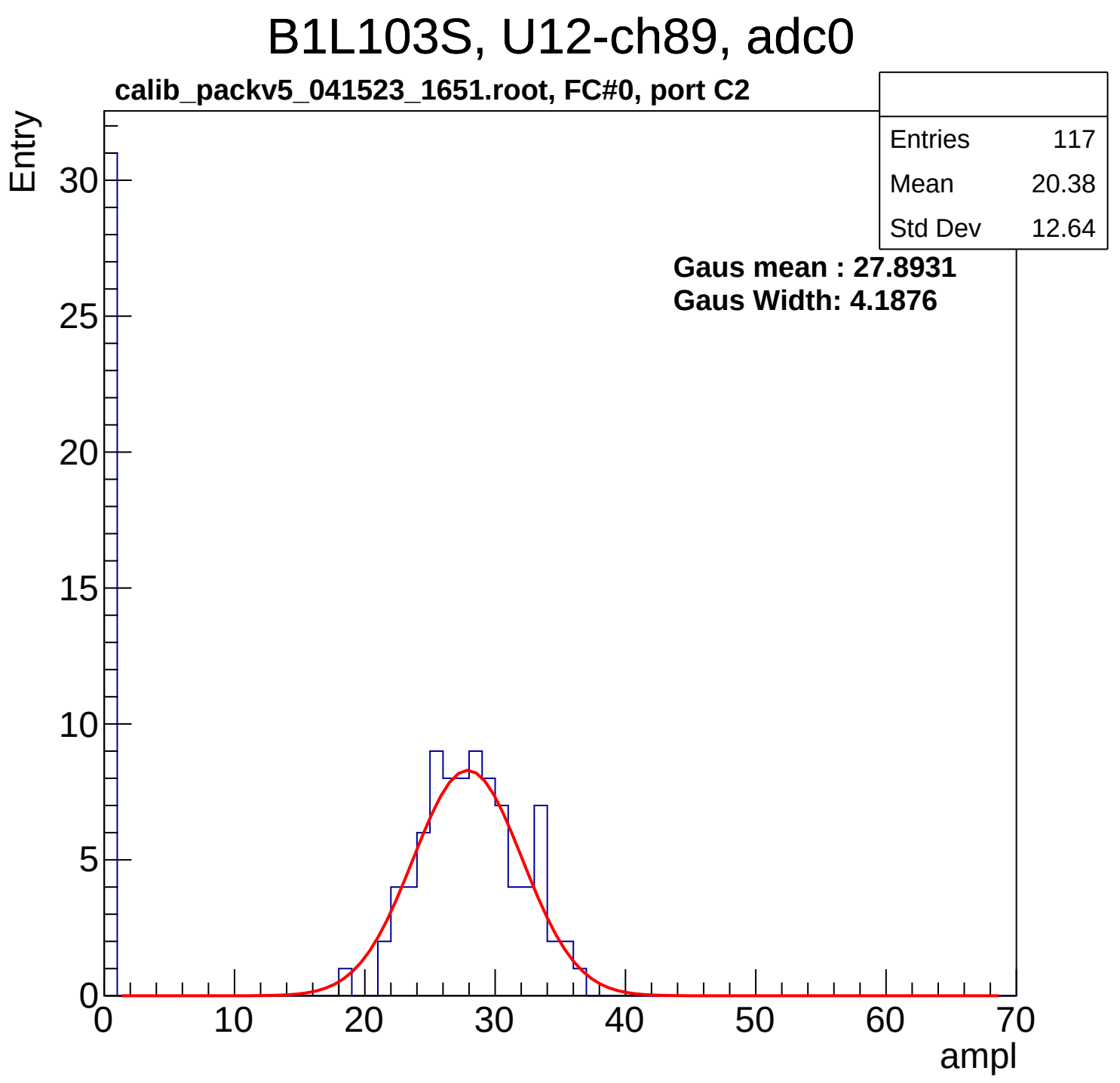
ampl


B1L103S, U12-ch89, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 117
Mean 20.38
Std Dev 12.64
Gaus mean : 27.8931
Gaus Width: 4.1876
Entry
ampl
0
5
10
15
20
25
30
0
10
20
30
40
50
60
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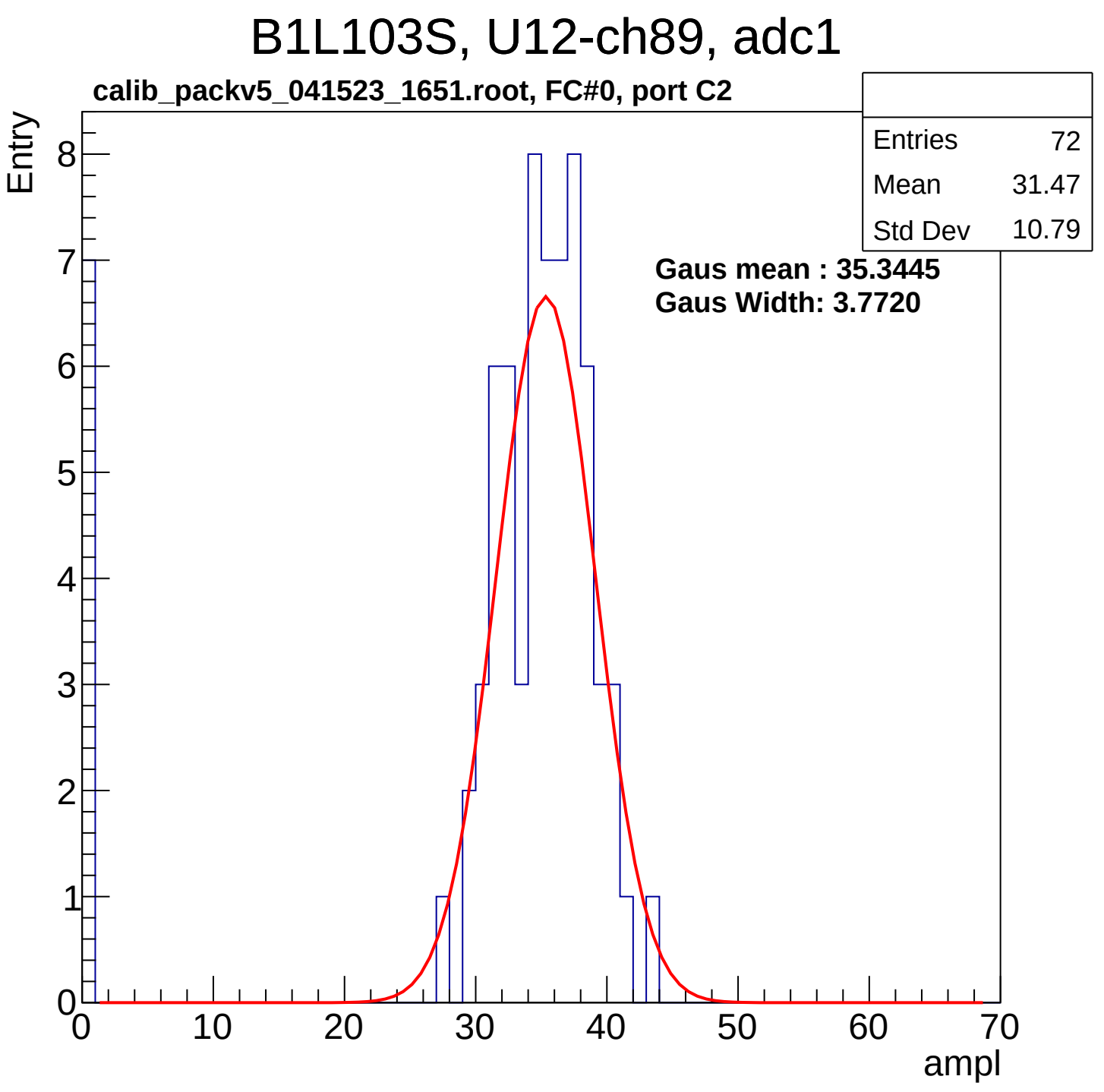
B1L103S, U12-ch89, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 31.47
Std Dev 10.79
Gaus mean : 35.3445
Gaus Width: 3.7720
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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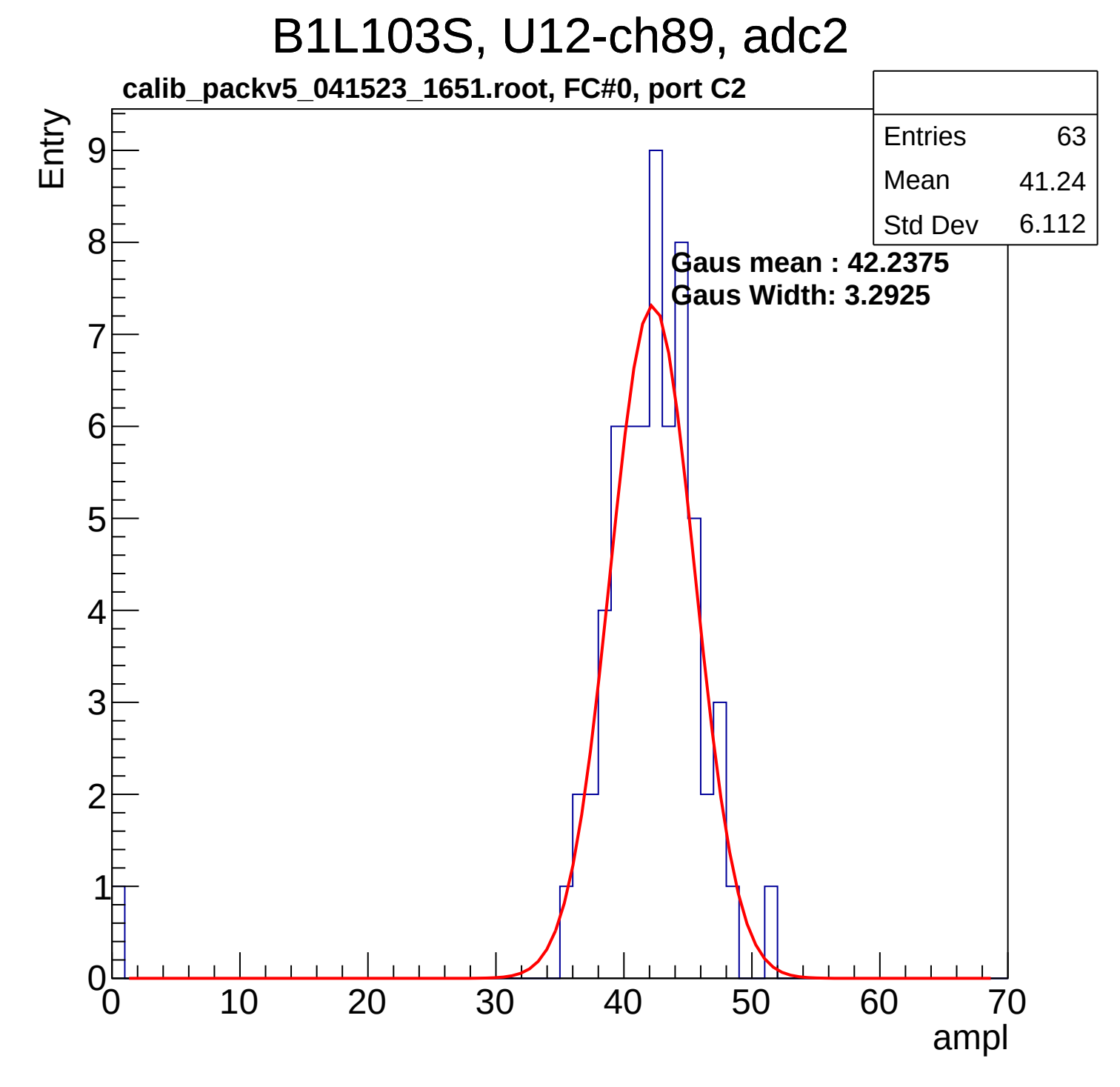
B1L103S, U12-ch89, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 41.24
Std Dev 6.112
Gaus mean : 42.2375
Gaus Width: 3.2925
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
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20
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40
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60
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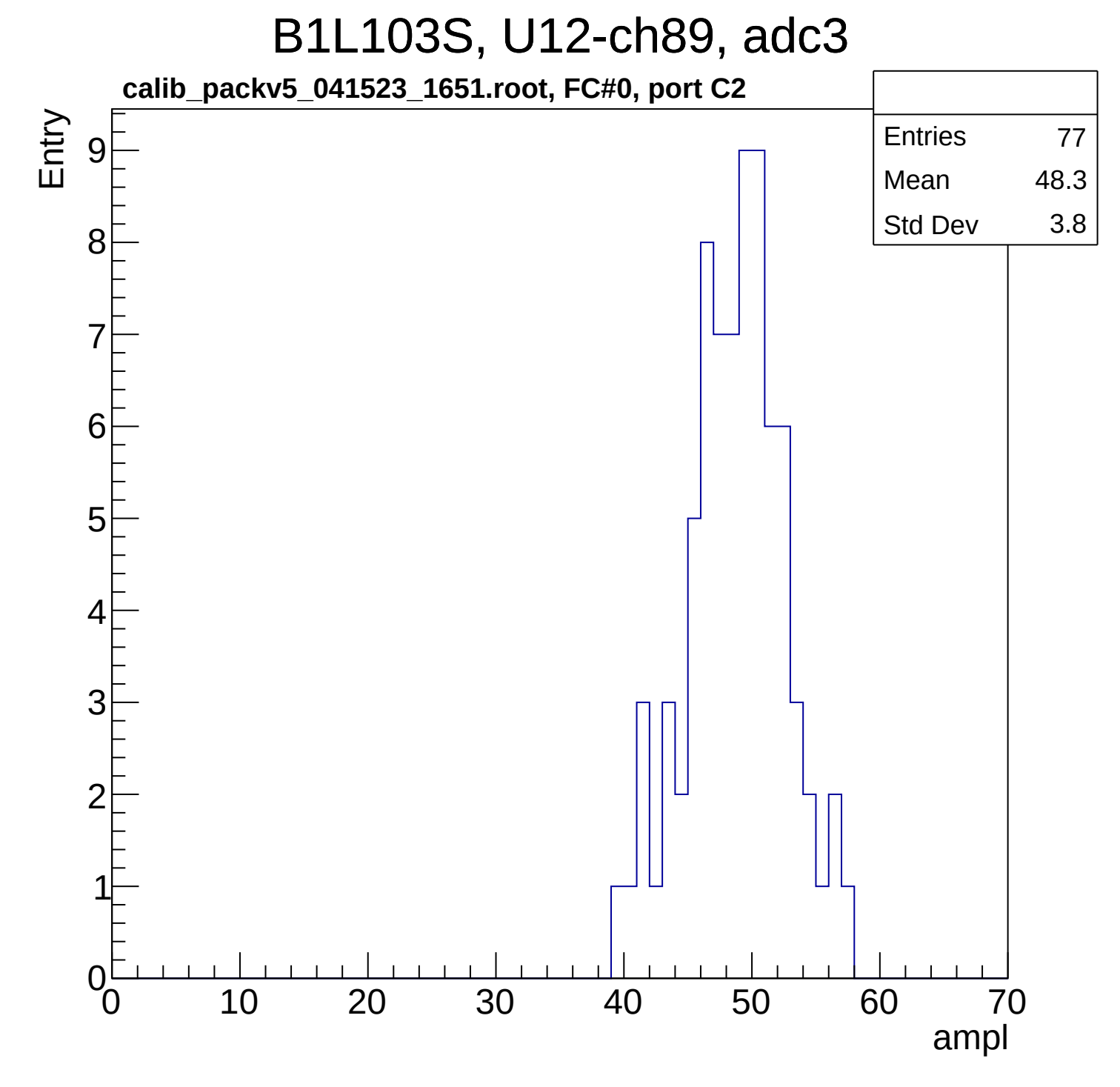
B1L103S, U12-ch89, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 48.3
Std Dev 3.8
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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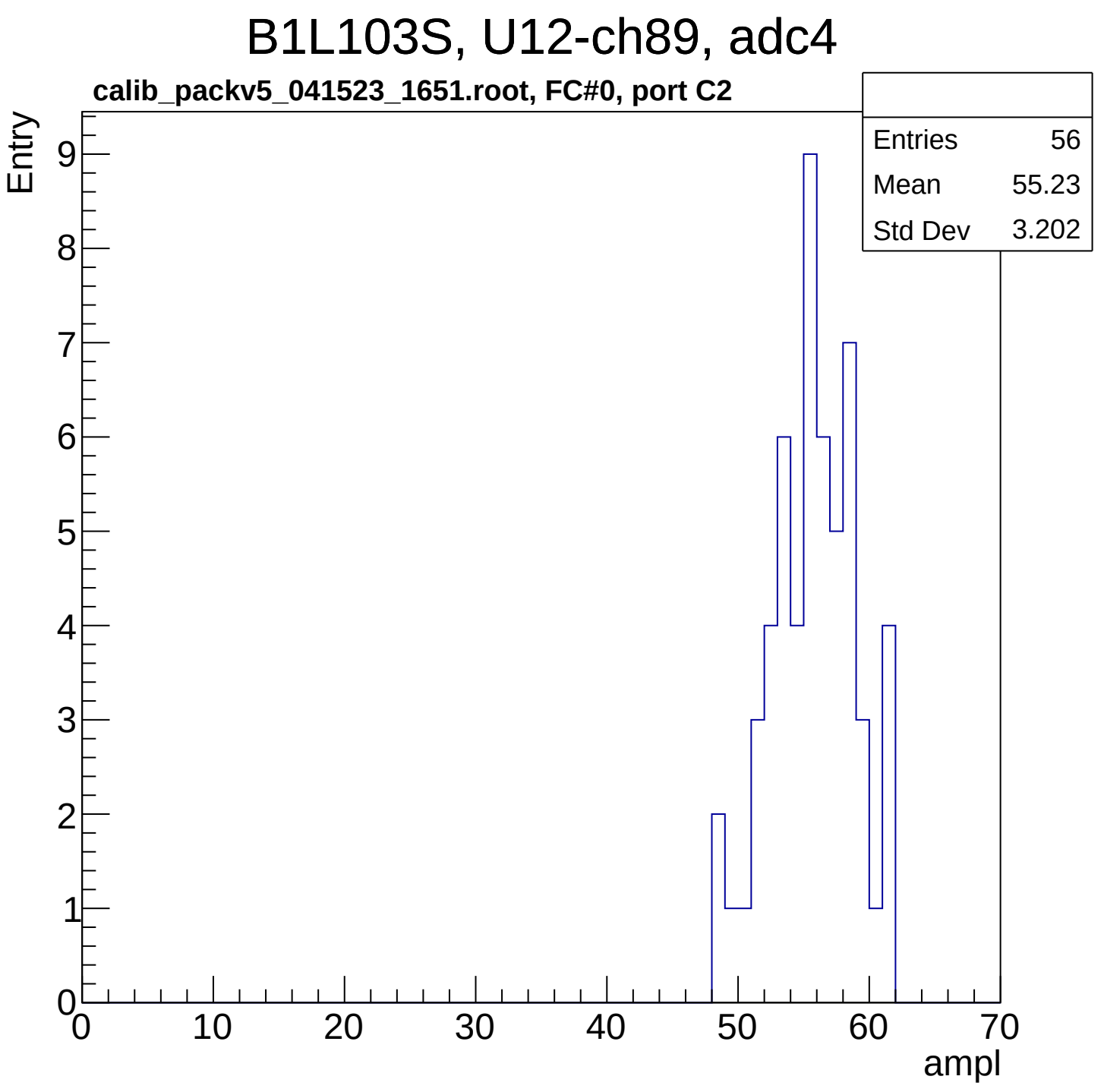
B1L103S, U12-ch89, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 55.23
Std Dev 3.202
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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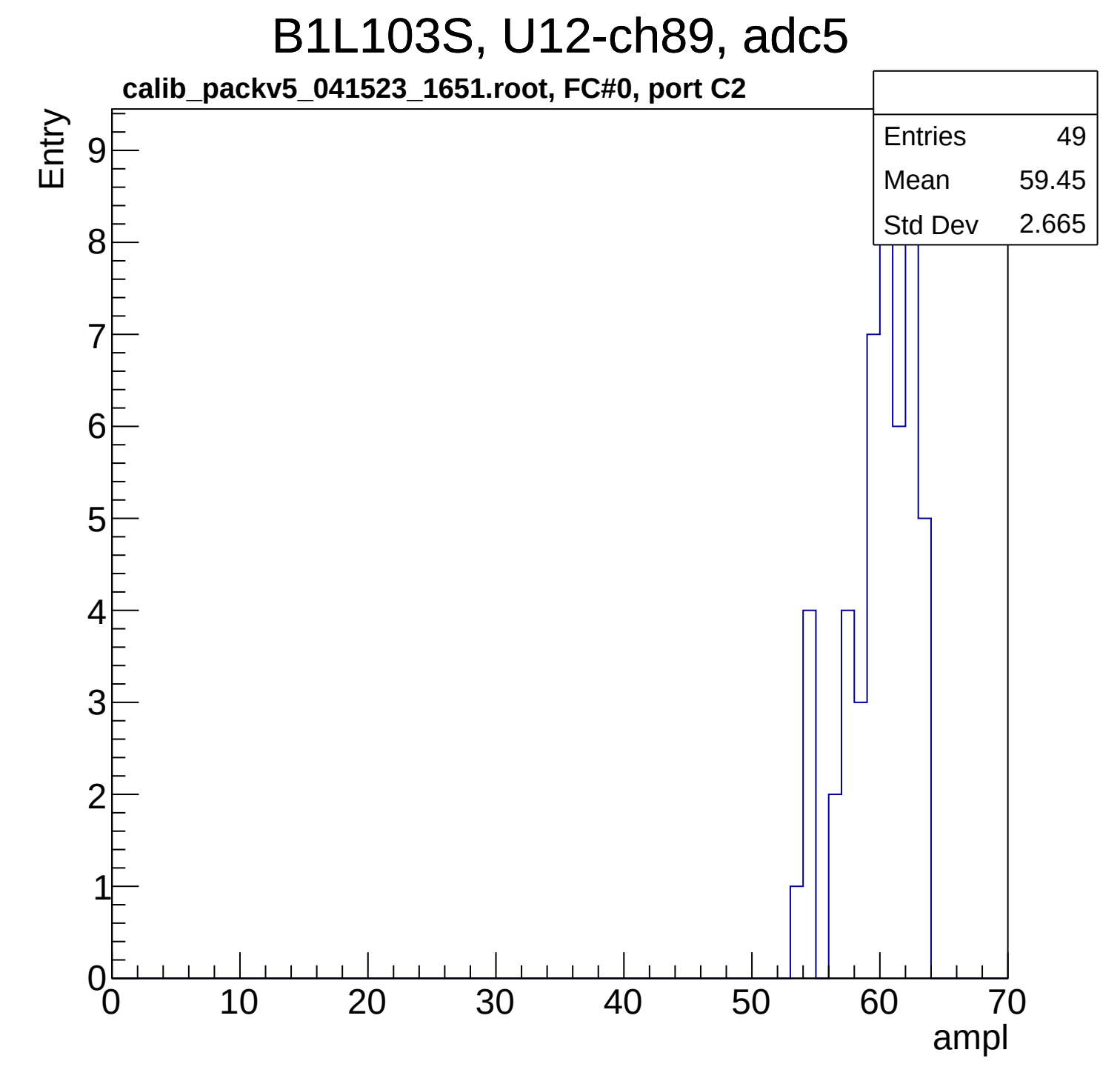
B1L103S, U12-ch89, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 59.45
Std Dev 2.665
Entry
ampl
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3
4
5
6
7
8
9
0
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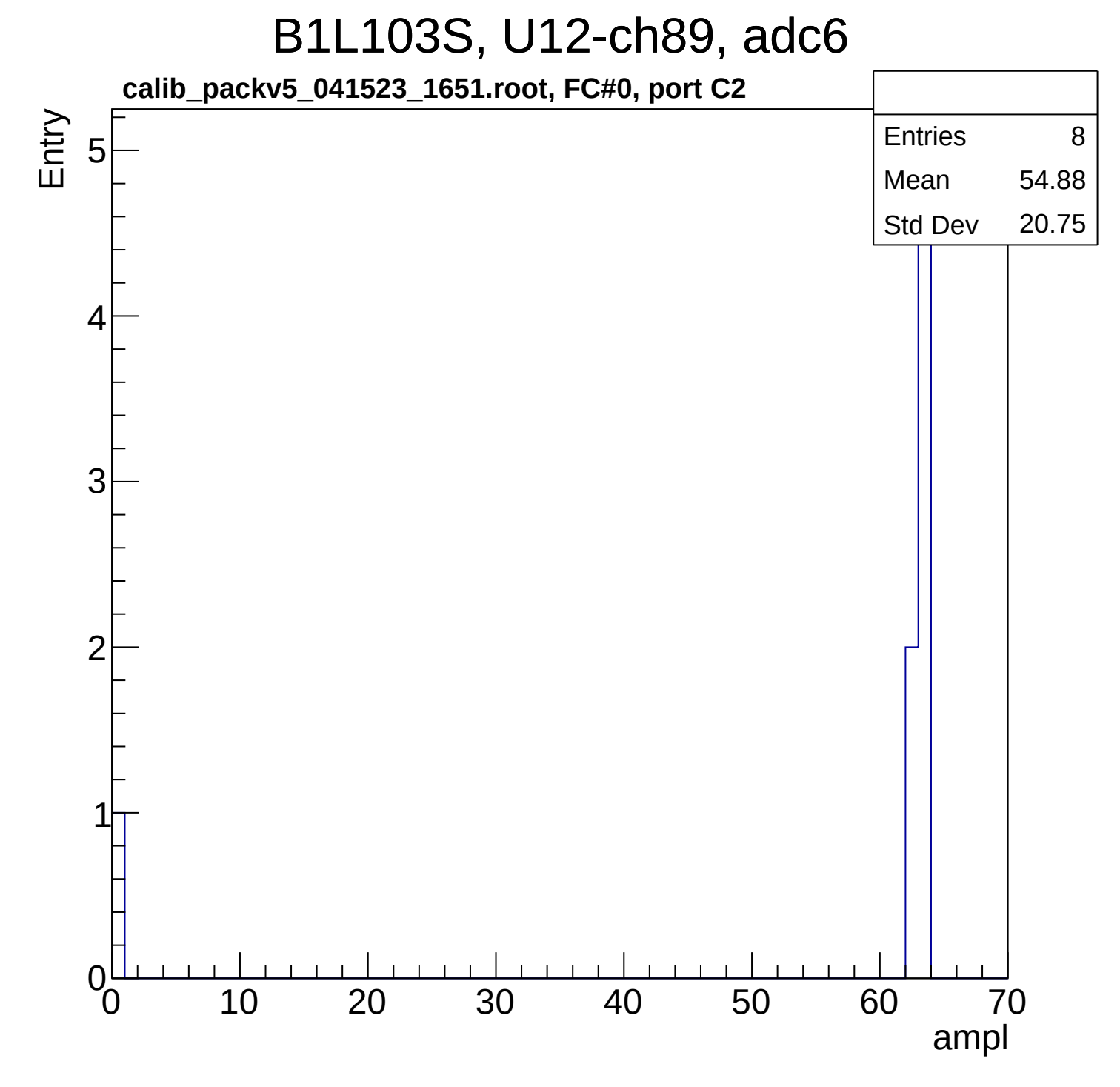
B1L103S, U12-ch89, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 54.88
Std Dev 20.75
Entry
ampl
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1
2
3
4
5
0
10
20
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40
50
60
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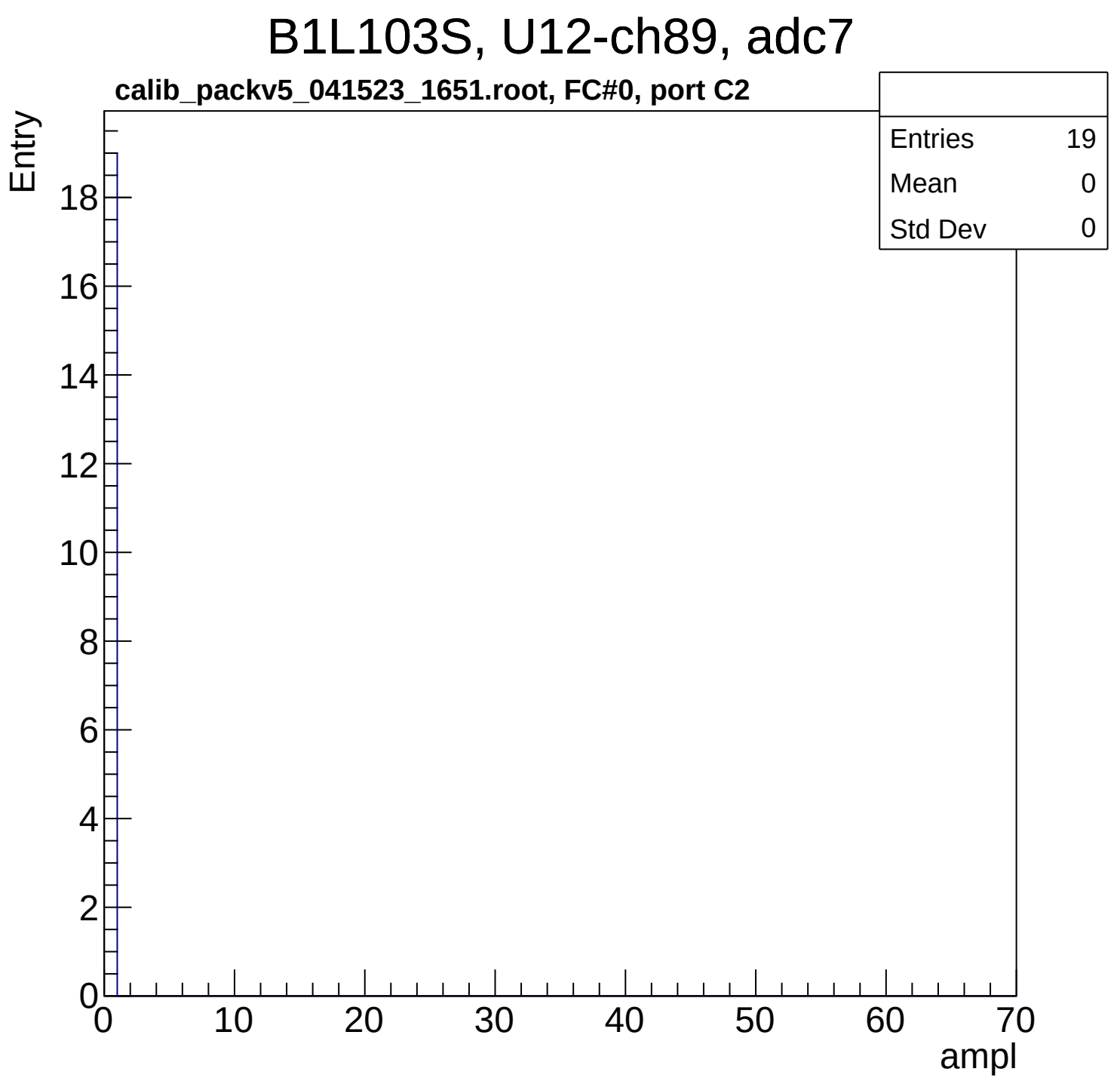
B1L103S, U12-ch89, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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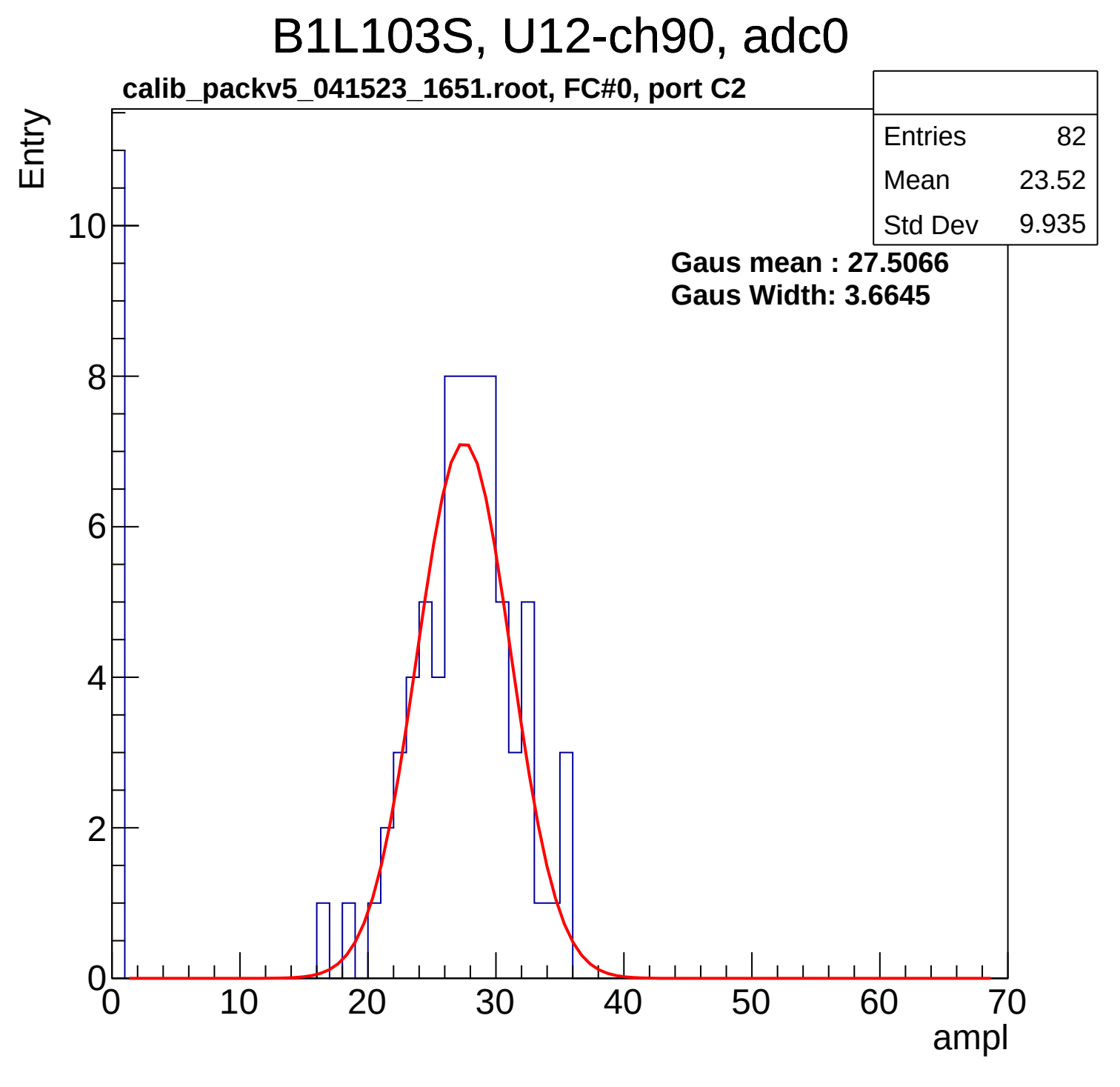
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch90, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 23.52
Std Dev 9.935
Gaus mean : 27.5066
Gaus Width: 3.6645
Entry
ampl
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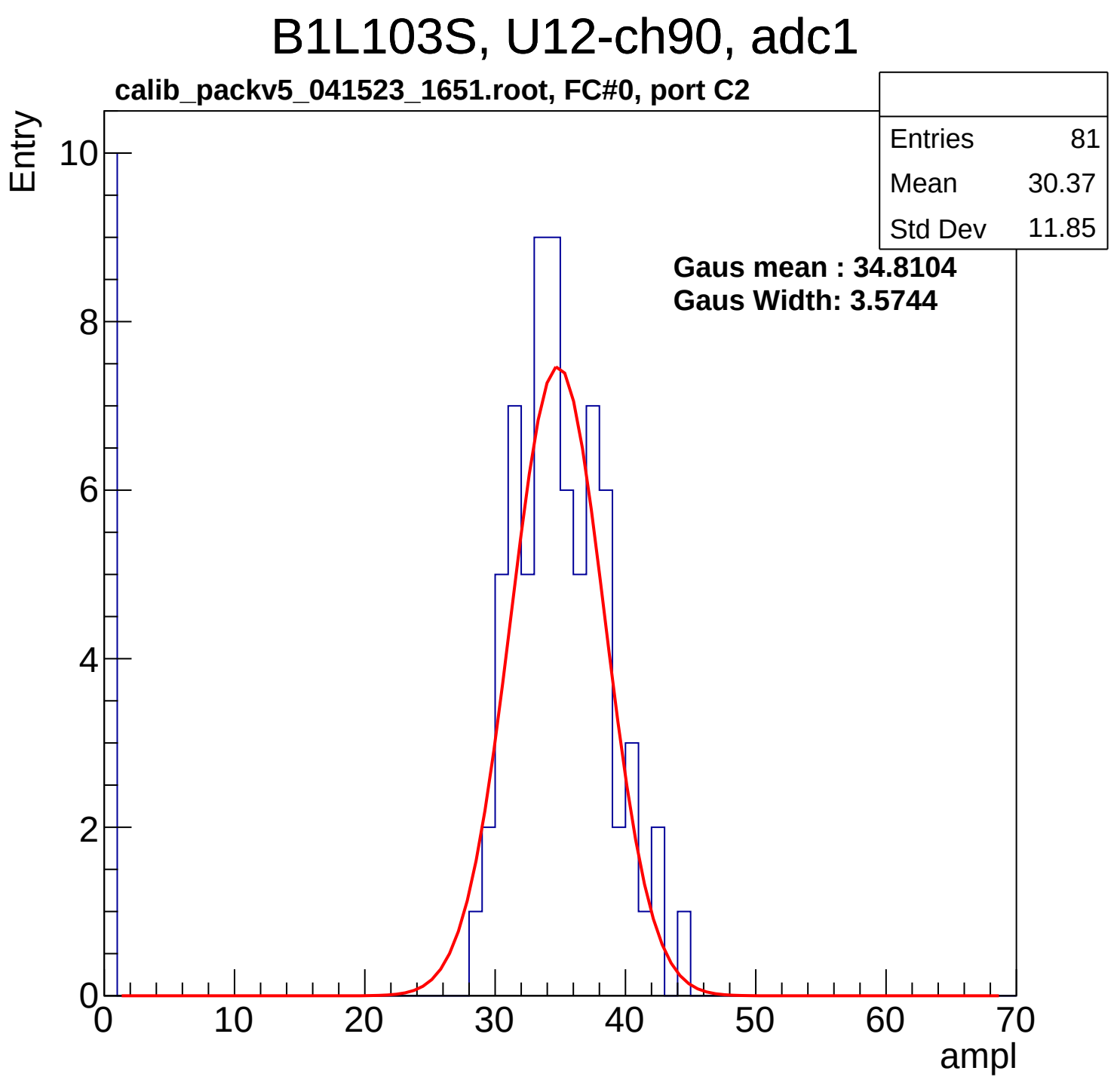
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch90, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 30.37
Std Dev 11.85
Gaus mean : 34.8104
Gaus Width: 3.5744
Entry
ampl
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2
4
6
8
10
0
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40
50
60
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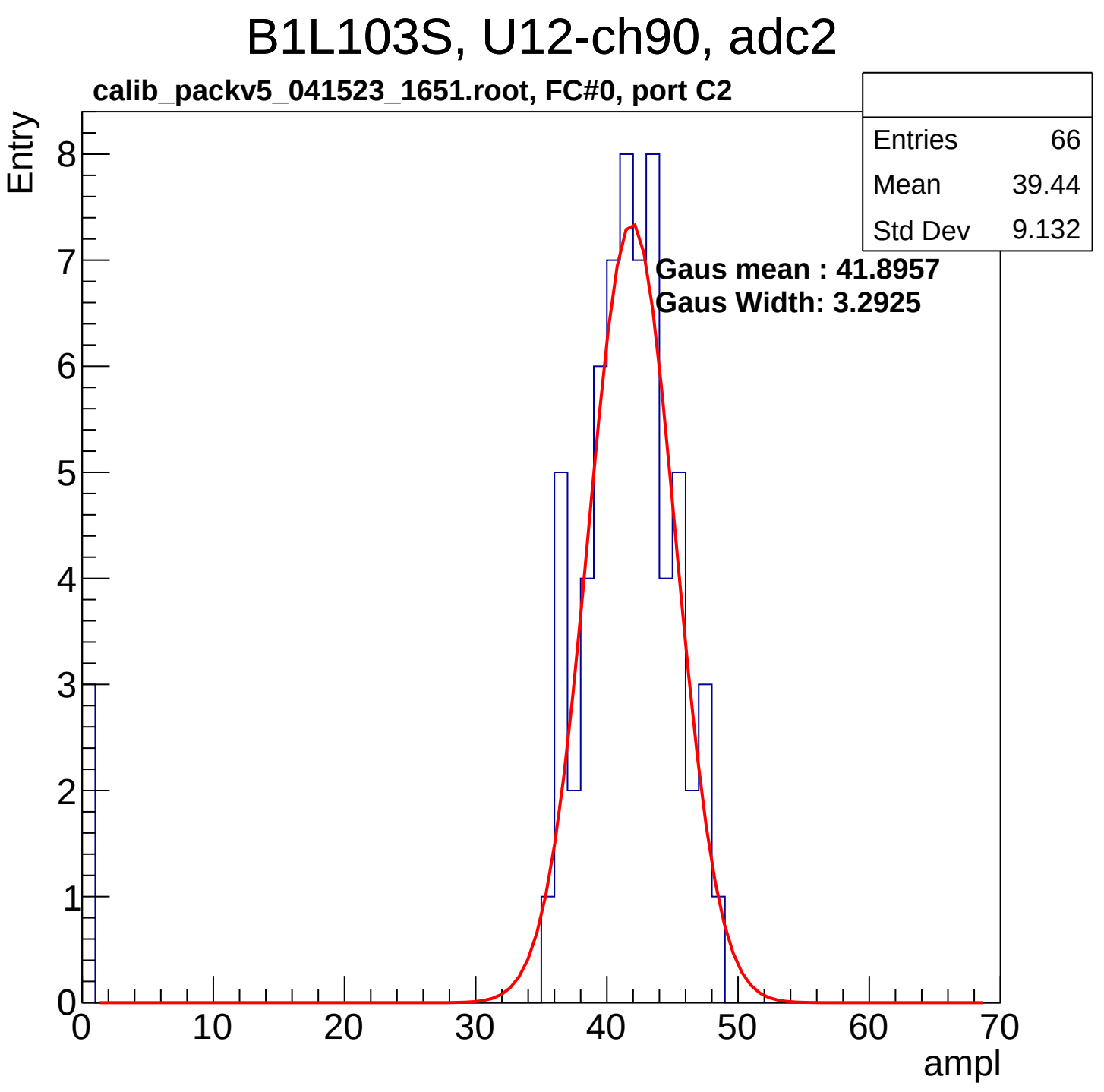
B1L103S, U12-ch90, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 39.44
Std Dev 9.132
Gaus mean : 41.8957
Gaus Width: 3.2925
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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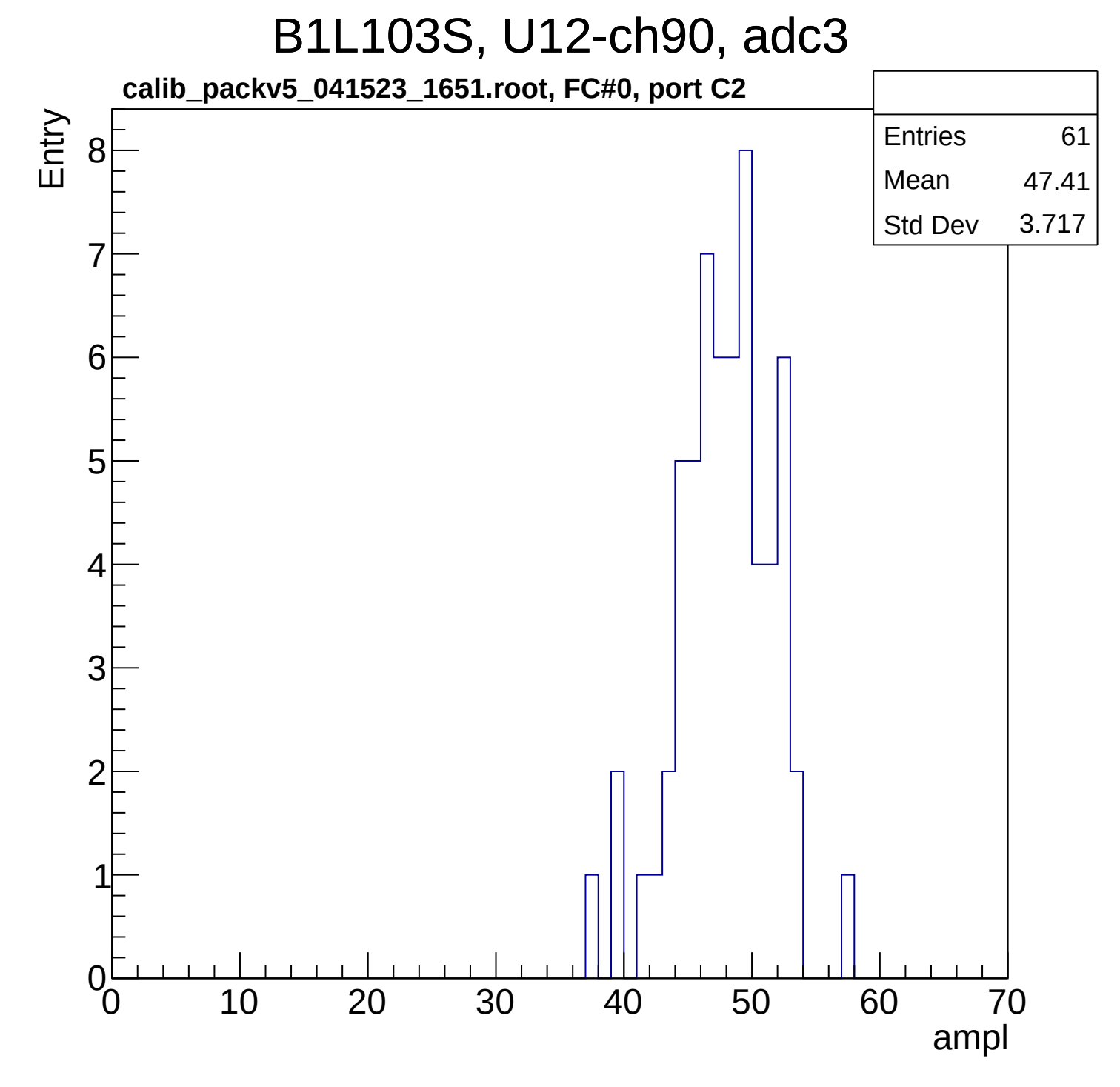
B1L103S, U12-ch90, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 47.41
Std Dev 3.717
Entry
ampl
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1
2
3
4
5
6
7
8
0
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60
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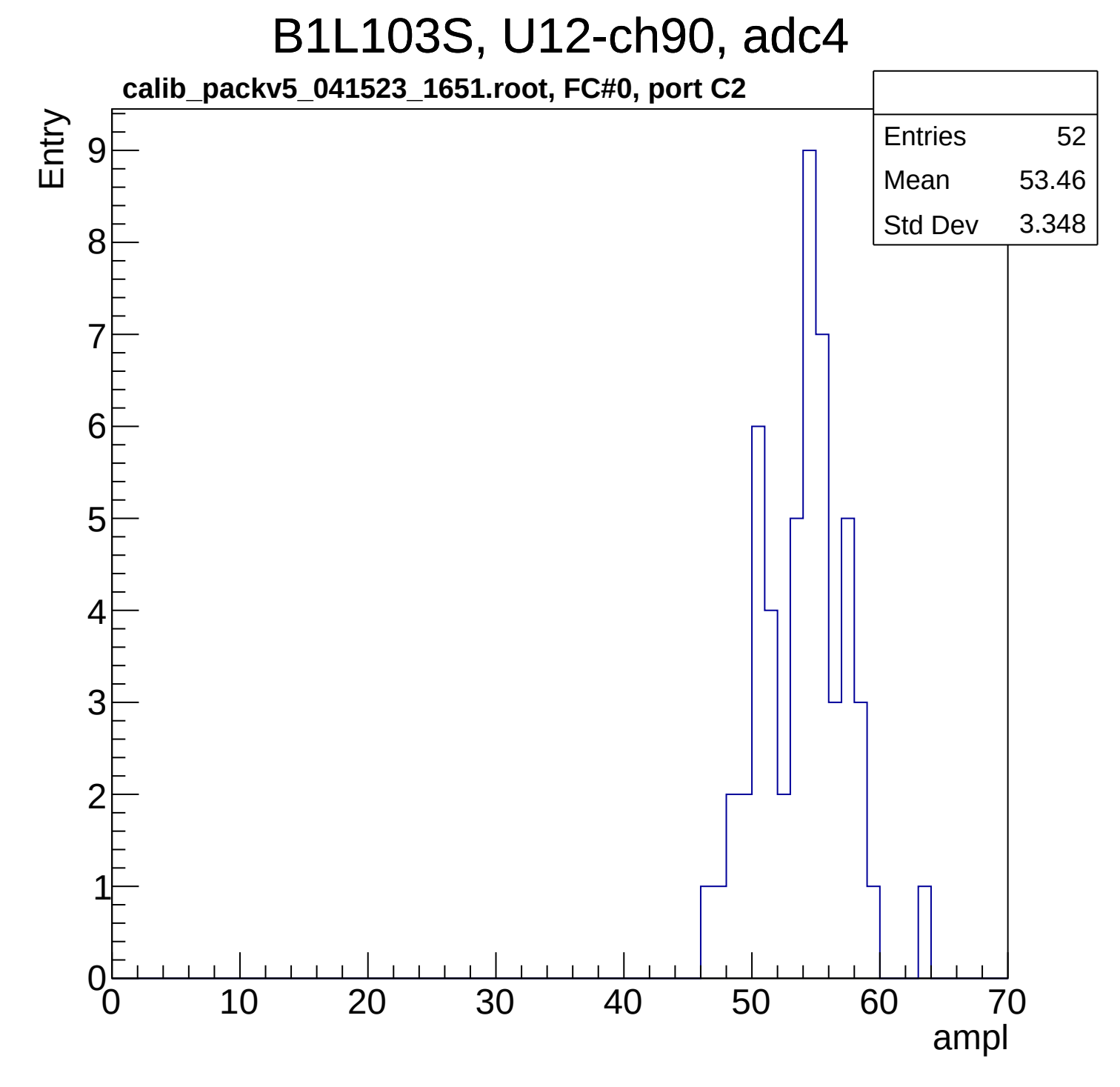
B1L103S, U12-ch90, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 53.46
Std Dev 3.348
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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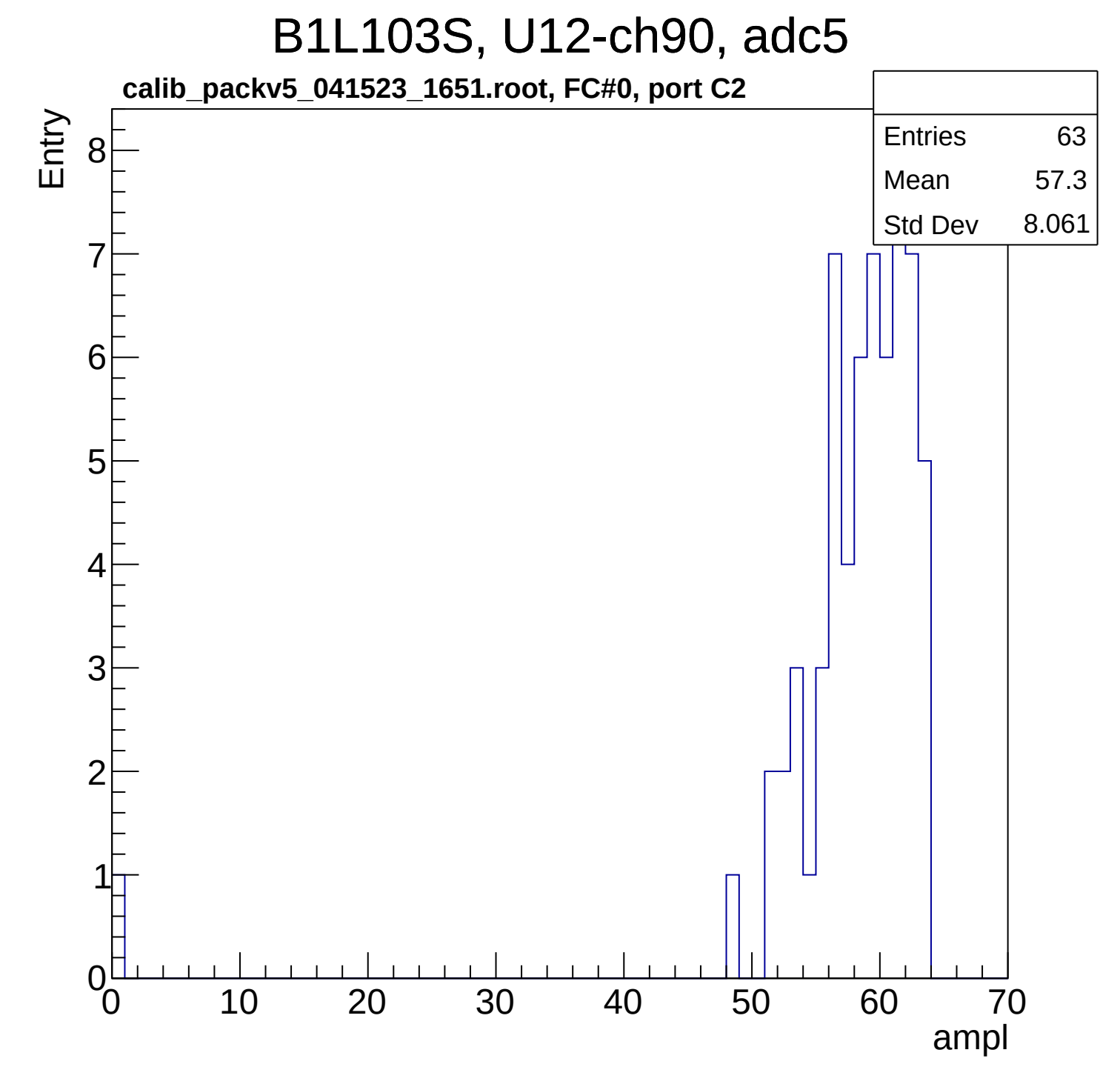
B1L103S, U12-ch90, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 57.3
Std Dev 8.061
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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60
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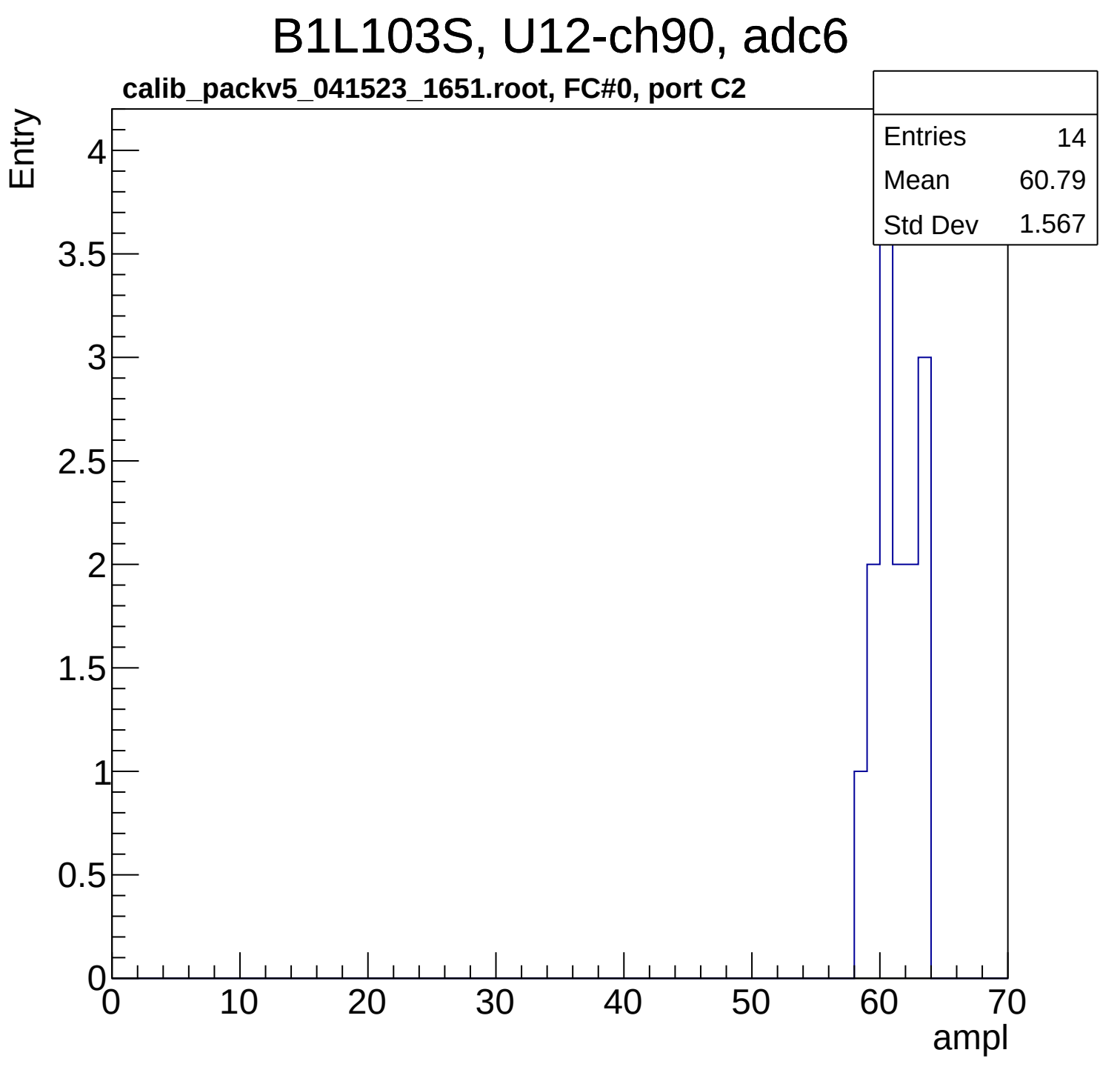
B1L103S, U12-ch90, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 14
Mean 60.79
Std Dev 1.567
Entry
ampl
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1
1.5
2
2.5
3
3.5
4
0
10
20
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40
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60
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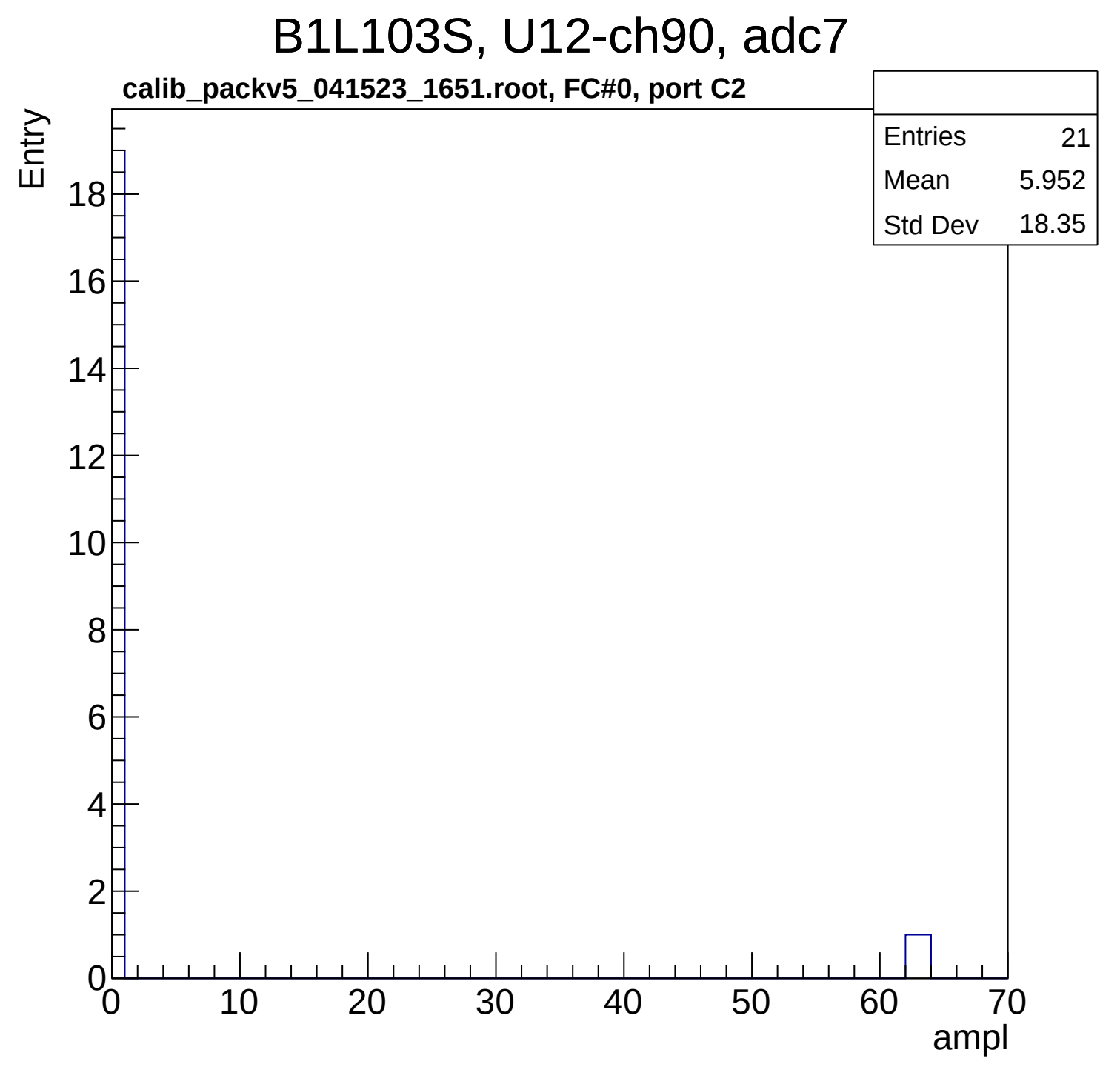
B1L103S, U12-ch90, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 21
Mean 5.952
Std Dev 18.35
Entry
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6
8
10
12
14
16
18
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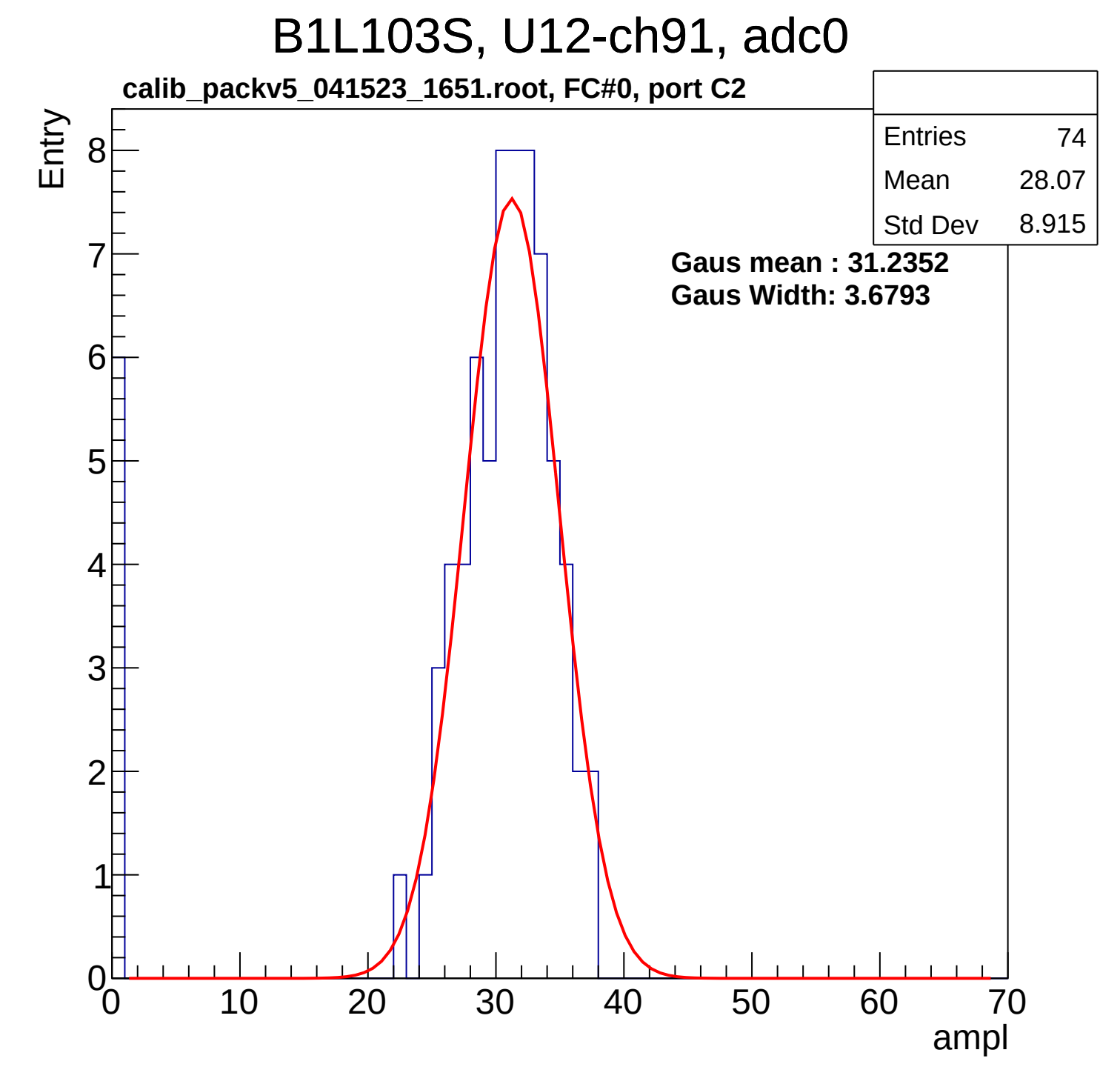
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch91, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 28.07
Std Dev 8.915
Gaus mean : 31.2352
Gaus Width: 3.6793
Entry
ampl
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3
4
5
6
7
8
0
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20
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60
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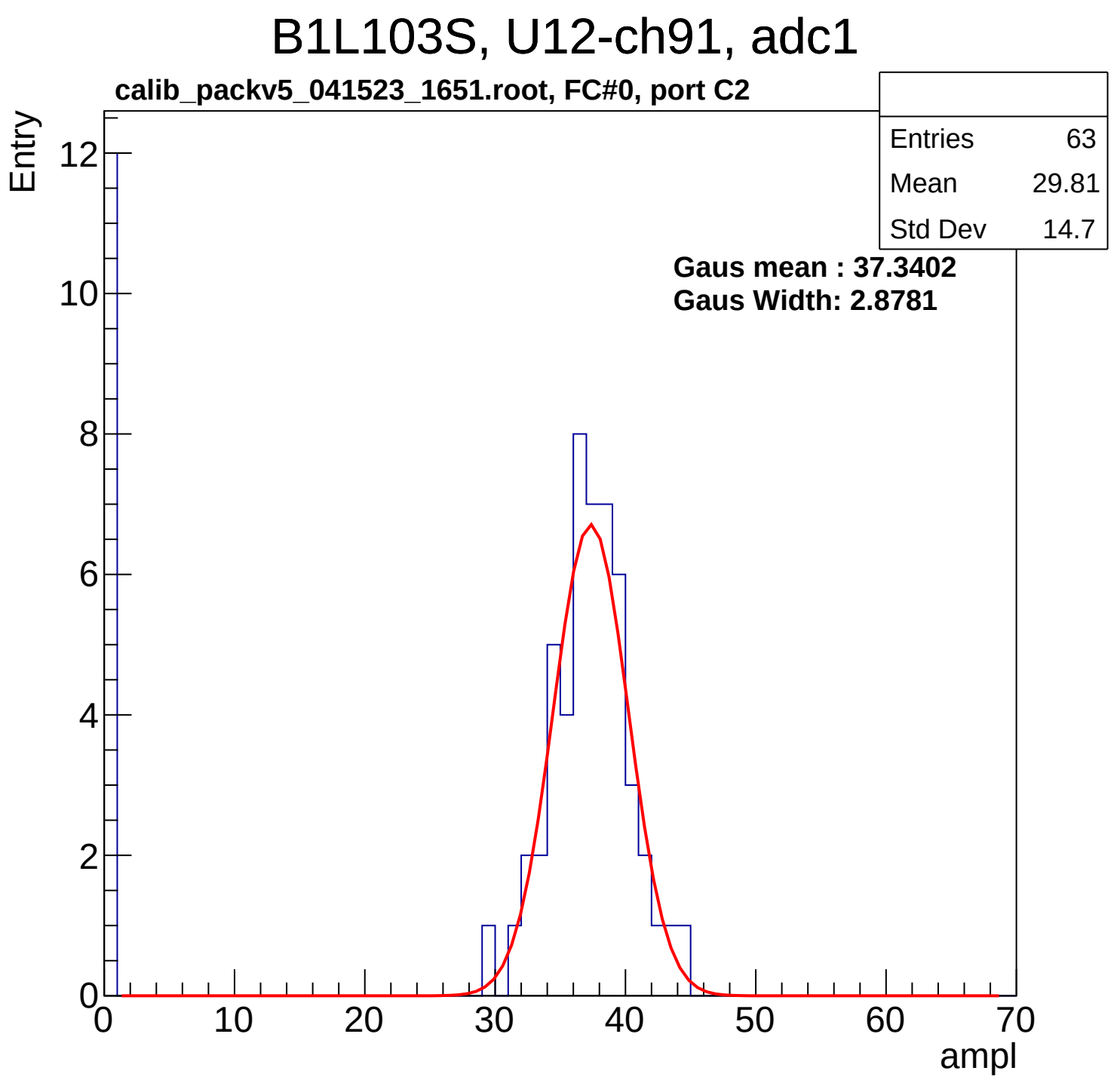
B1L103S, U12-ch91, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 29.81
Std Dev 14.7
Gaus mean : 37.3402
Gaus Width: 2.8781
Entry
ampl
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2
4
6
8
10
12
0
10
20
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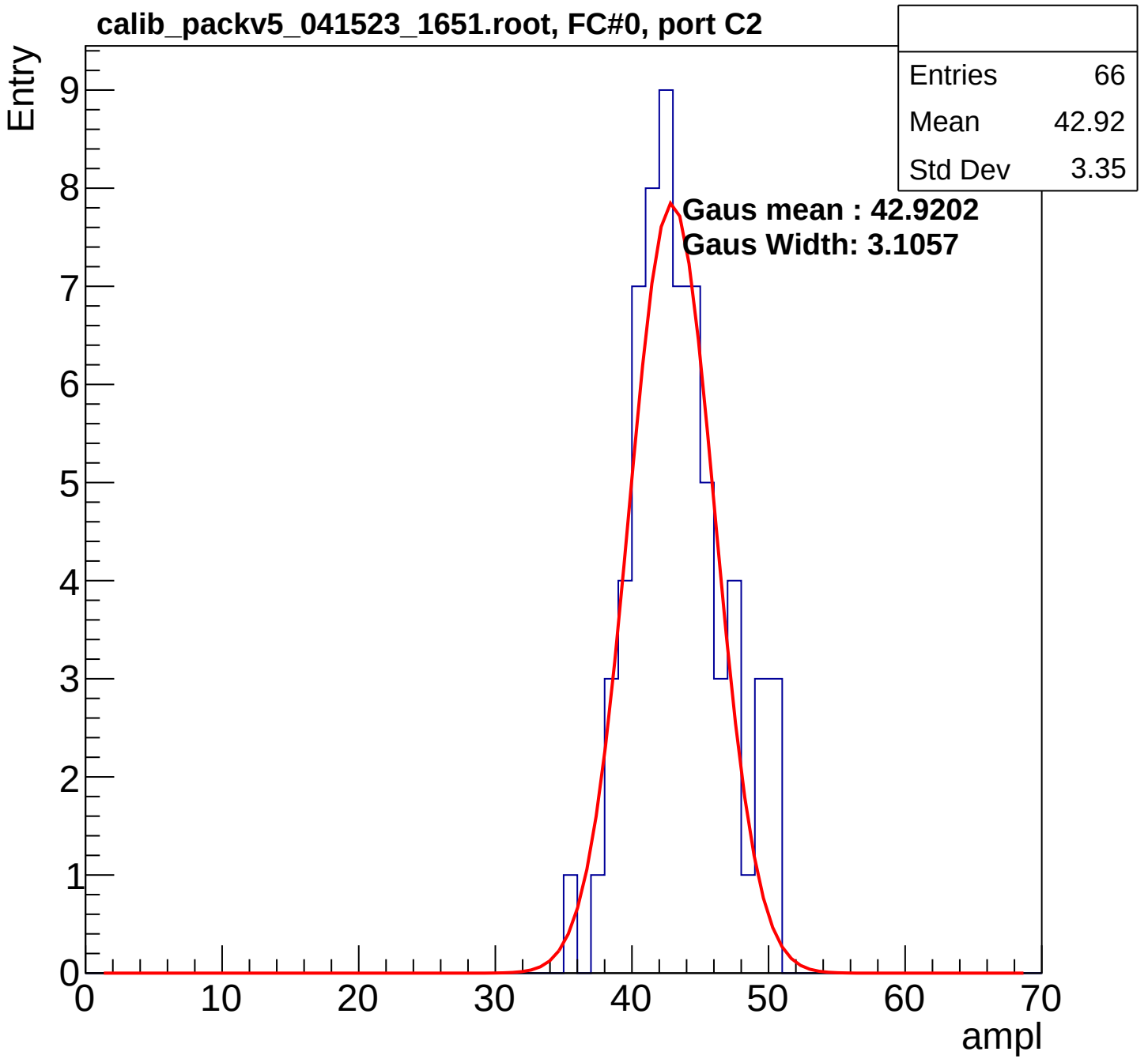
40
50
60
70


B1L103S, U12-ch91, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 42.92
Std Dev 3.35
Gaus mean : 42.9202
Gaus Width: 3.1057
Entry
ampl
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3
4
5
6
7
8
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0
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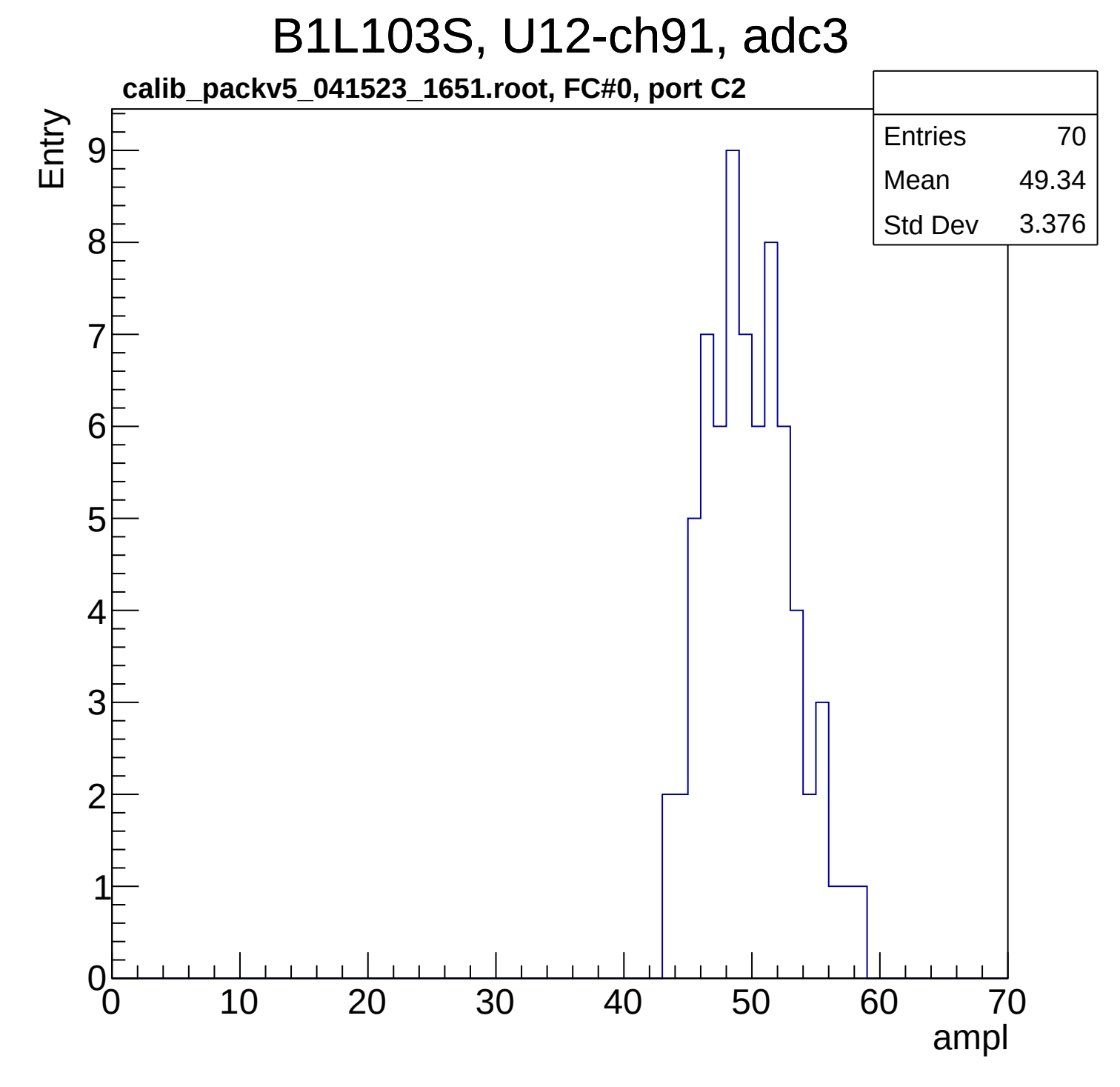
B1L103S, U12-ch91, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 49.34
Std Dev 3.376
Entry
ampl
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3
4
5
6
7
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0
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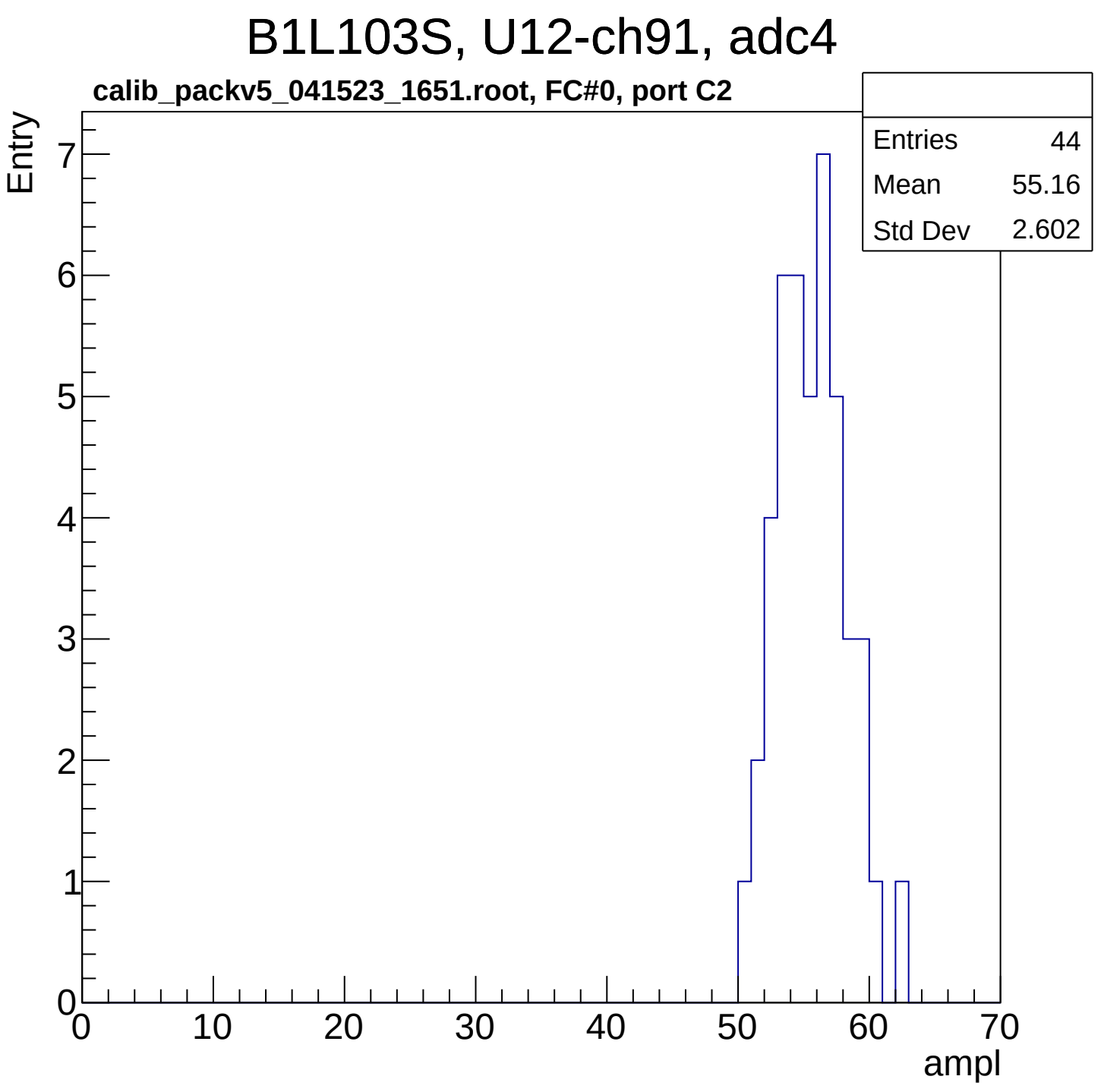
B1L103S, U12-ch91, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 44
Mean 55.16
Std Dev 2.602
Entry
ampl
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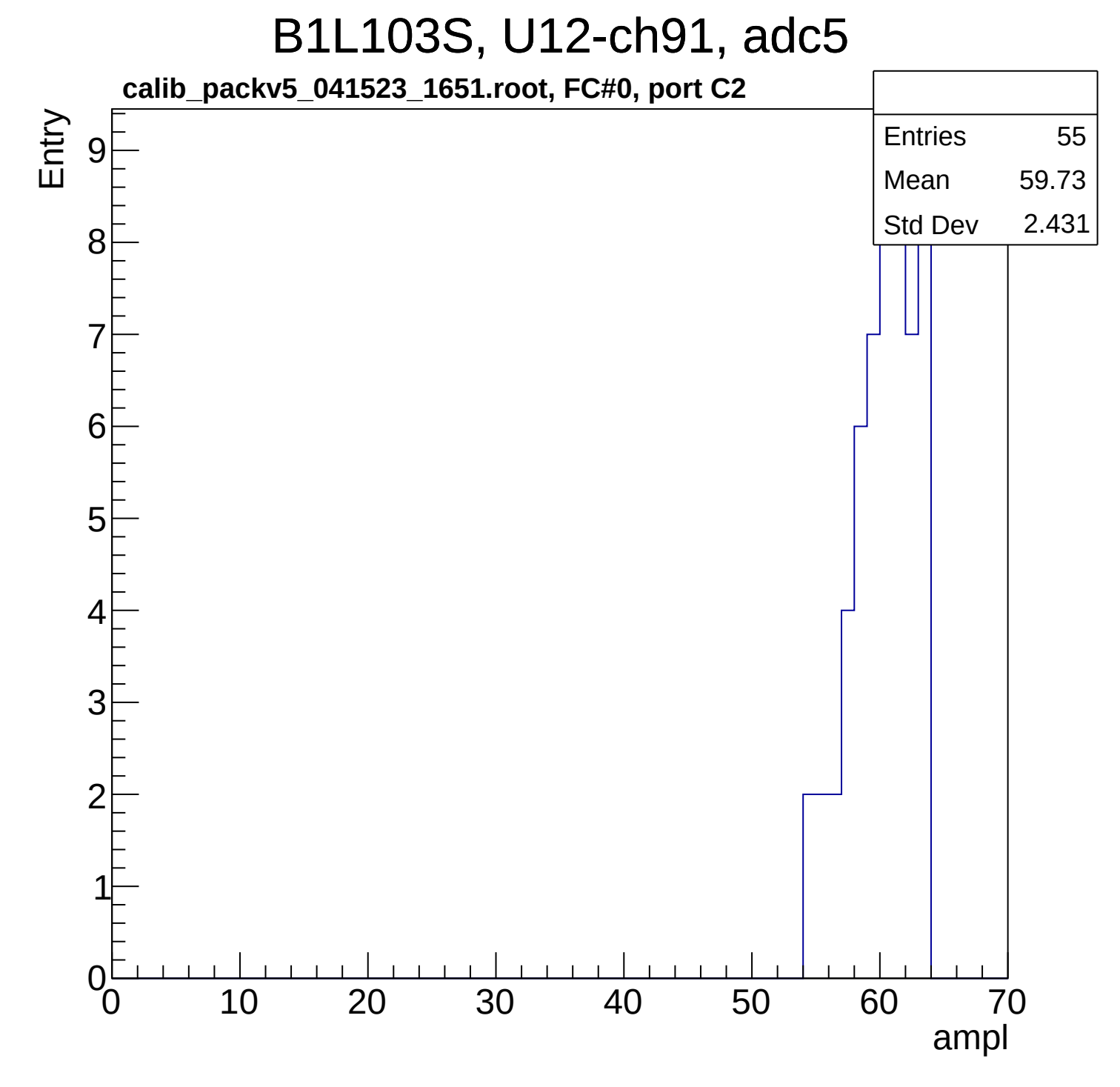
B1L103S, U12-ch91, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 59.73
Std Dev 2.431
Entry
ampl
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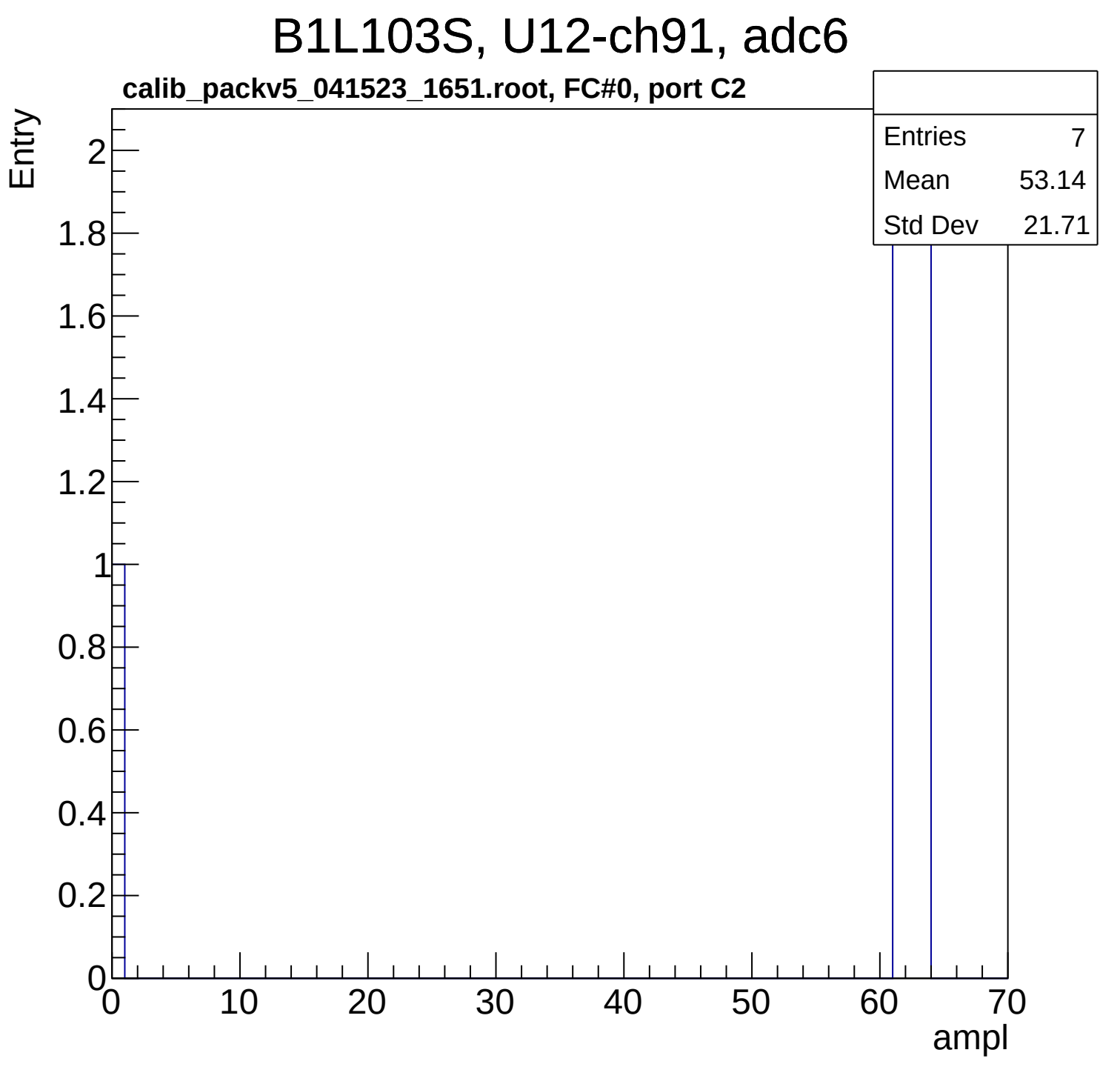
6
7
8
9


B1L103S, U12-ch91, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 53.14
Std Dev 21.71
Entry
ampl
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0.2
0.4
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1.2
1.4
1.6
1.8
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60
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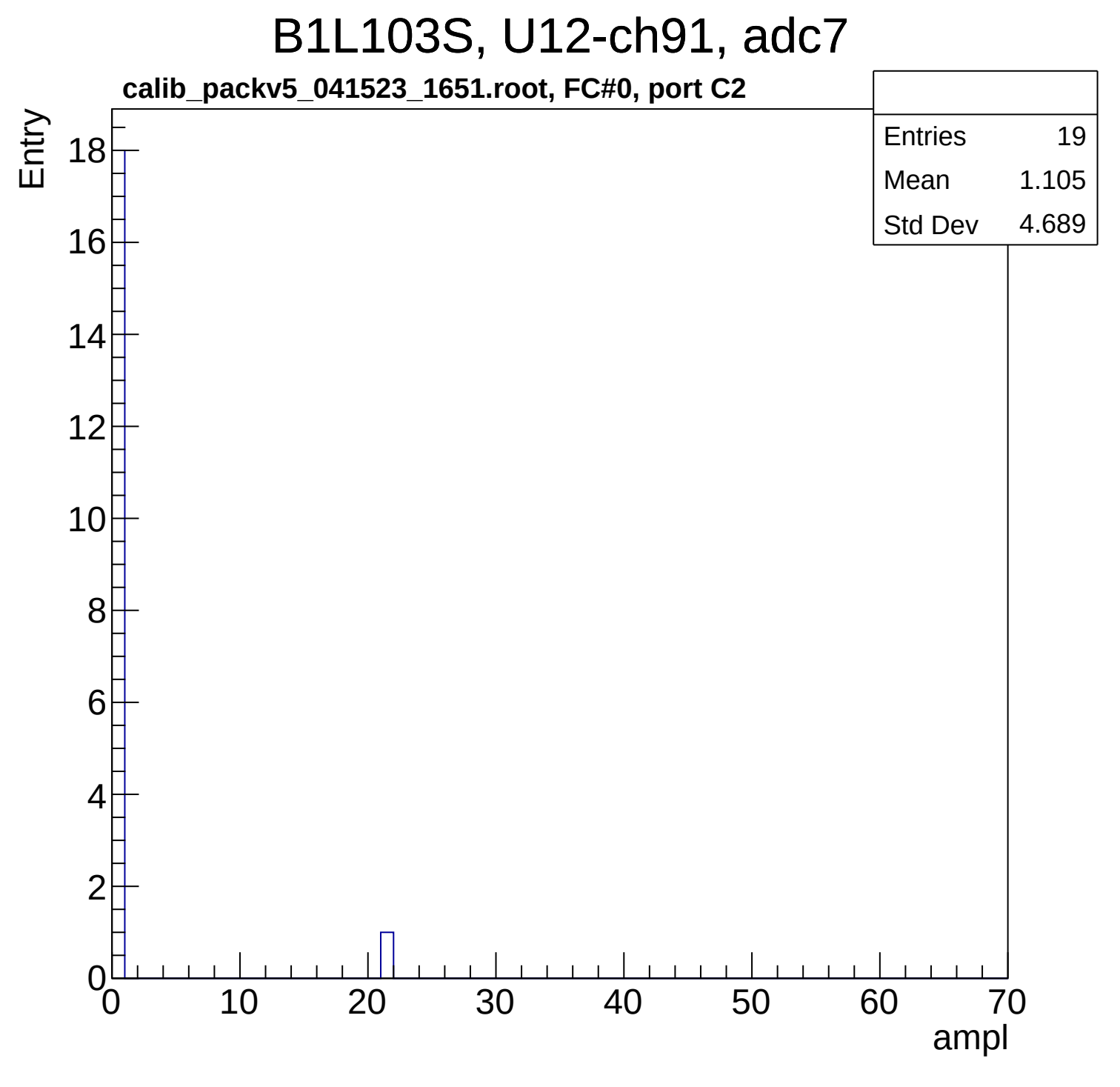
B1L103S, U12-ch91, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
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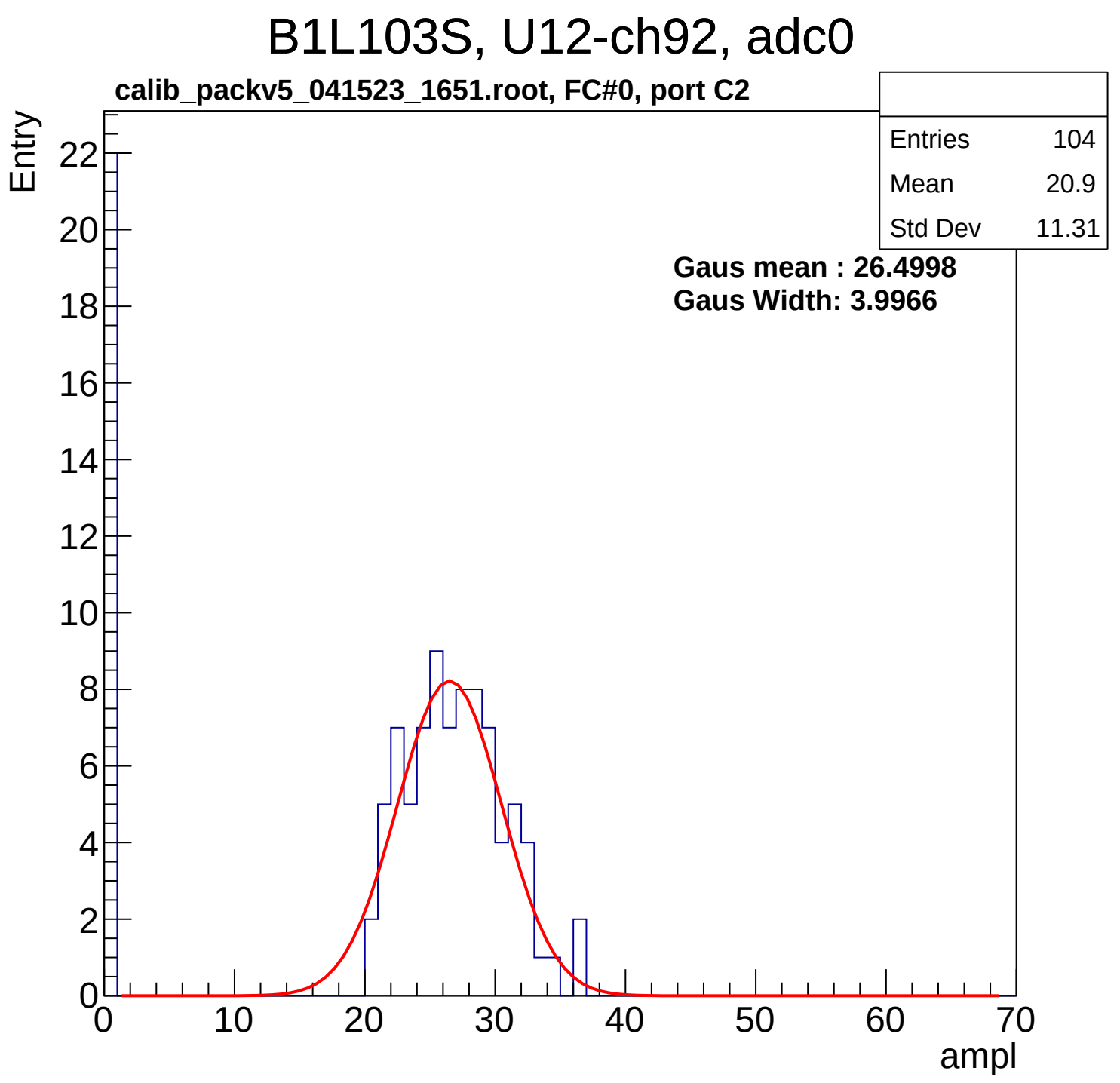
ampl


B1L103S, U12-ch92, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 104
Mean 20.9
Std Dev 11.31
Gaus mean : 26.4998
Gaus Width: 3.9966
Entry
ampl
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10
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14
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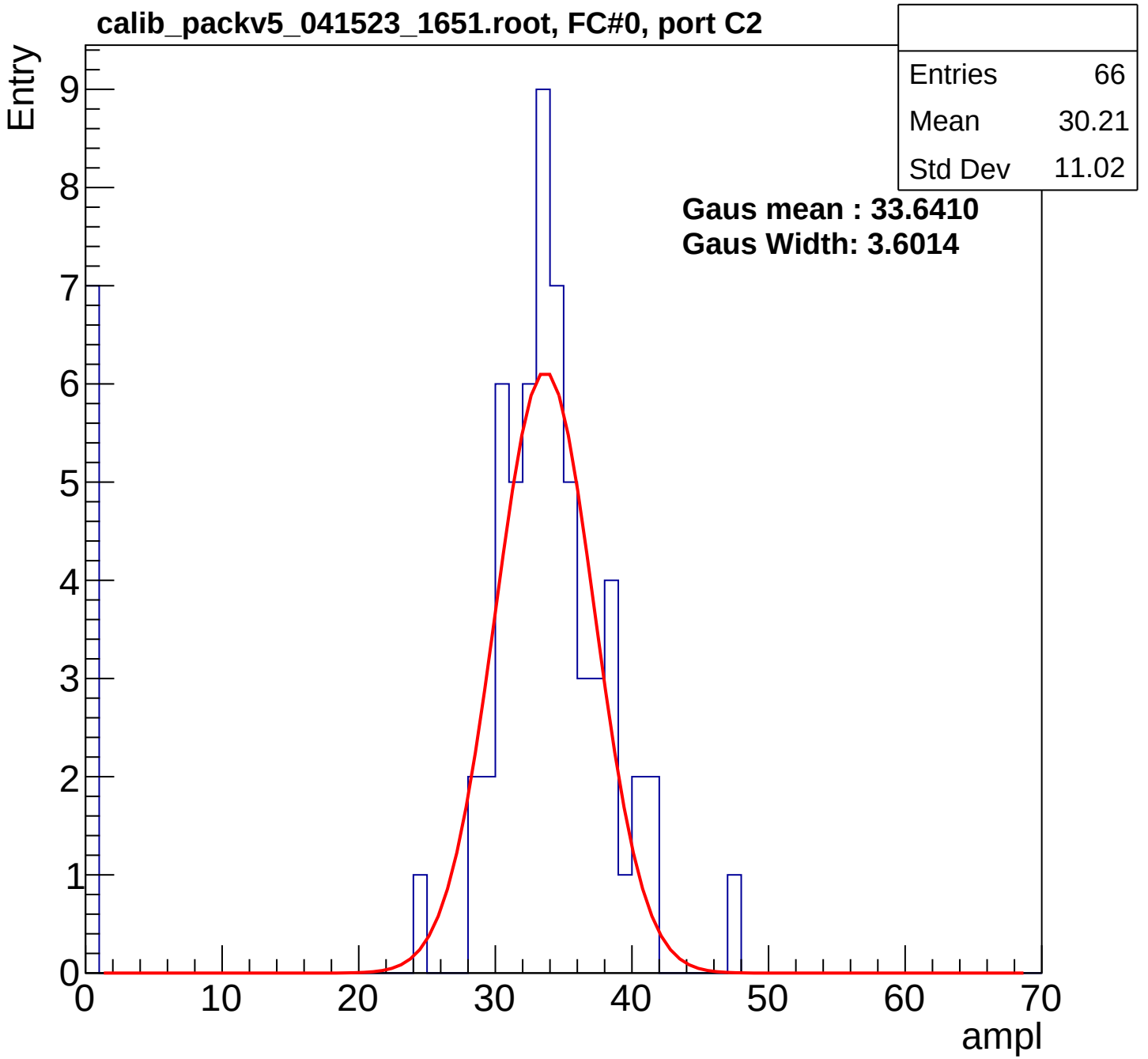
B1L103S, U12-ch92, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 30.21
Std Dev 11.02
Gaus mean : 33.6410
Gaus Width: 3.6014
Entry
ampl
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2
3
4
5
6
7
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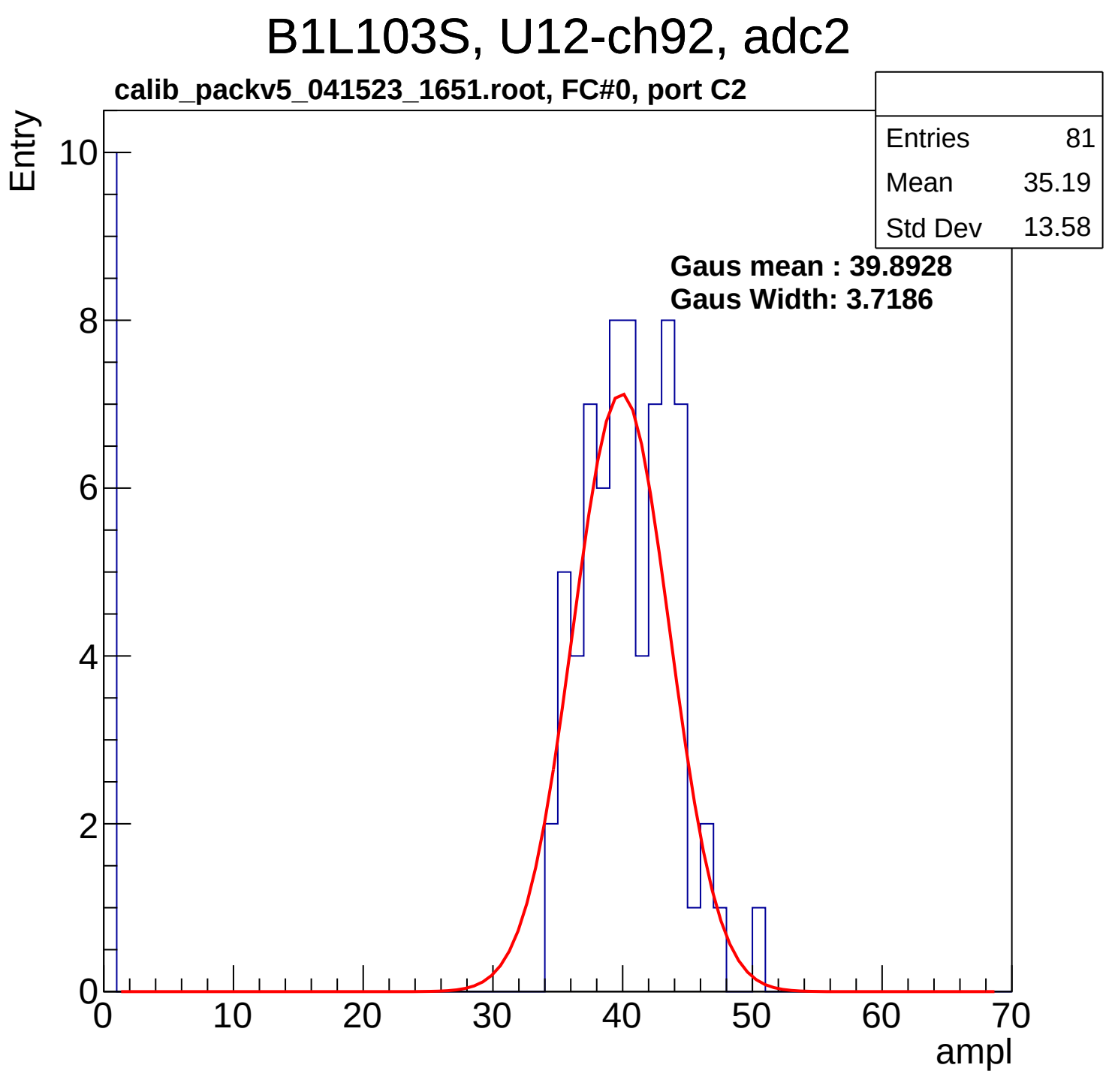
B1L103S, U12-ch92, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 35.19
Std Dev 13.58
Gaus mean : 39.8928
Gaus Width: 3.7186
Entry
ampl
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4
6
8
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0
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60
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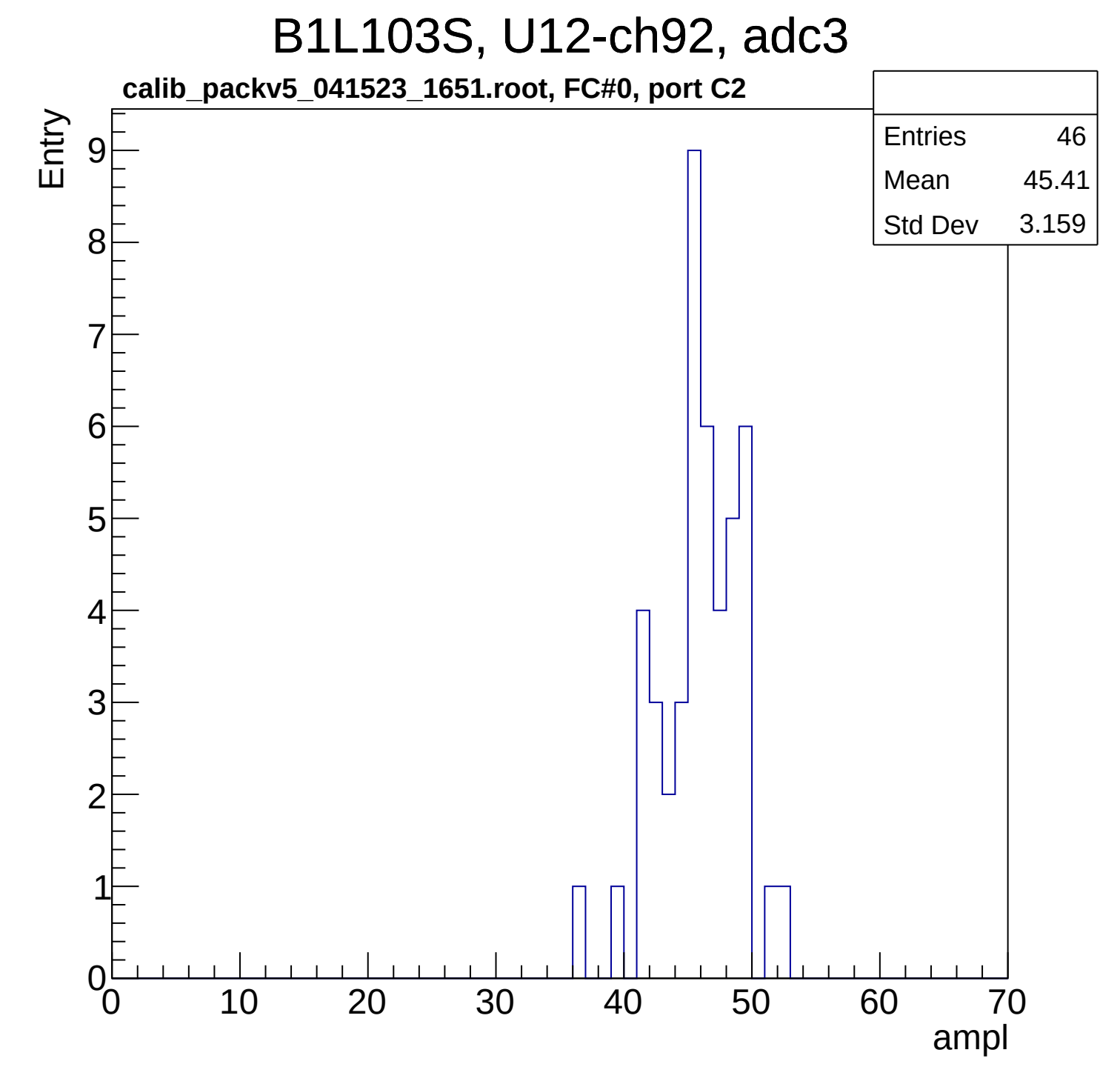
B1L103S, U12-ch92, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 46
Mean 45.41
Std Dev 3.159
Entry
ampl
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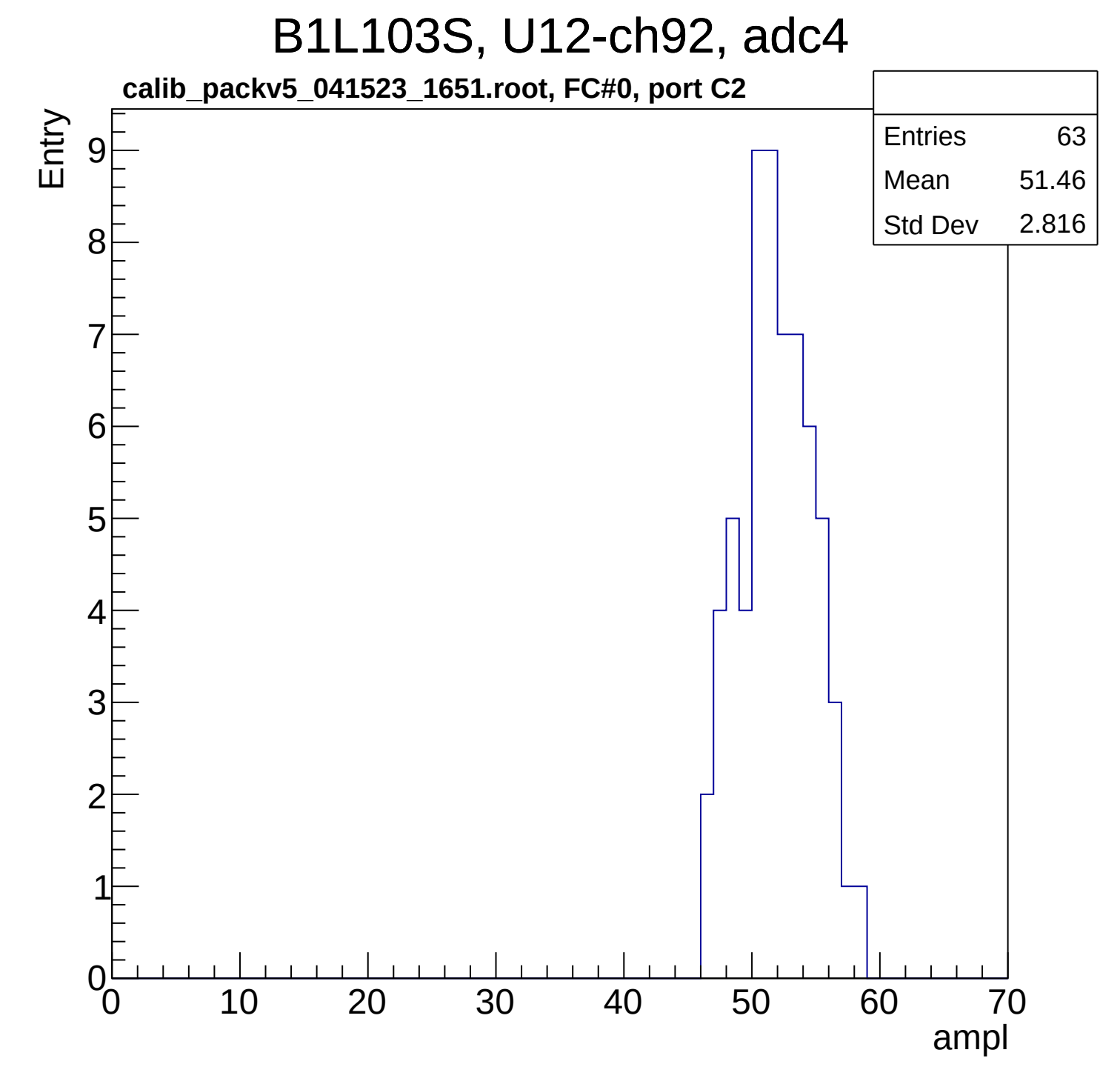
B1L103S, U12-ch92, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 51.46
Std Dev 2.816
Entry
ampl
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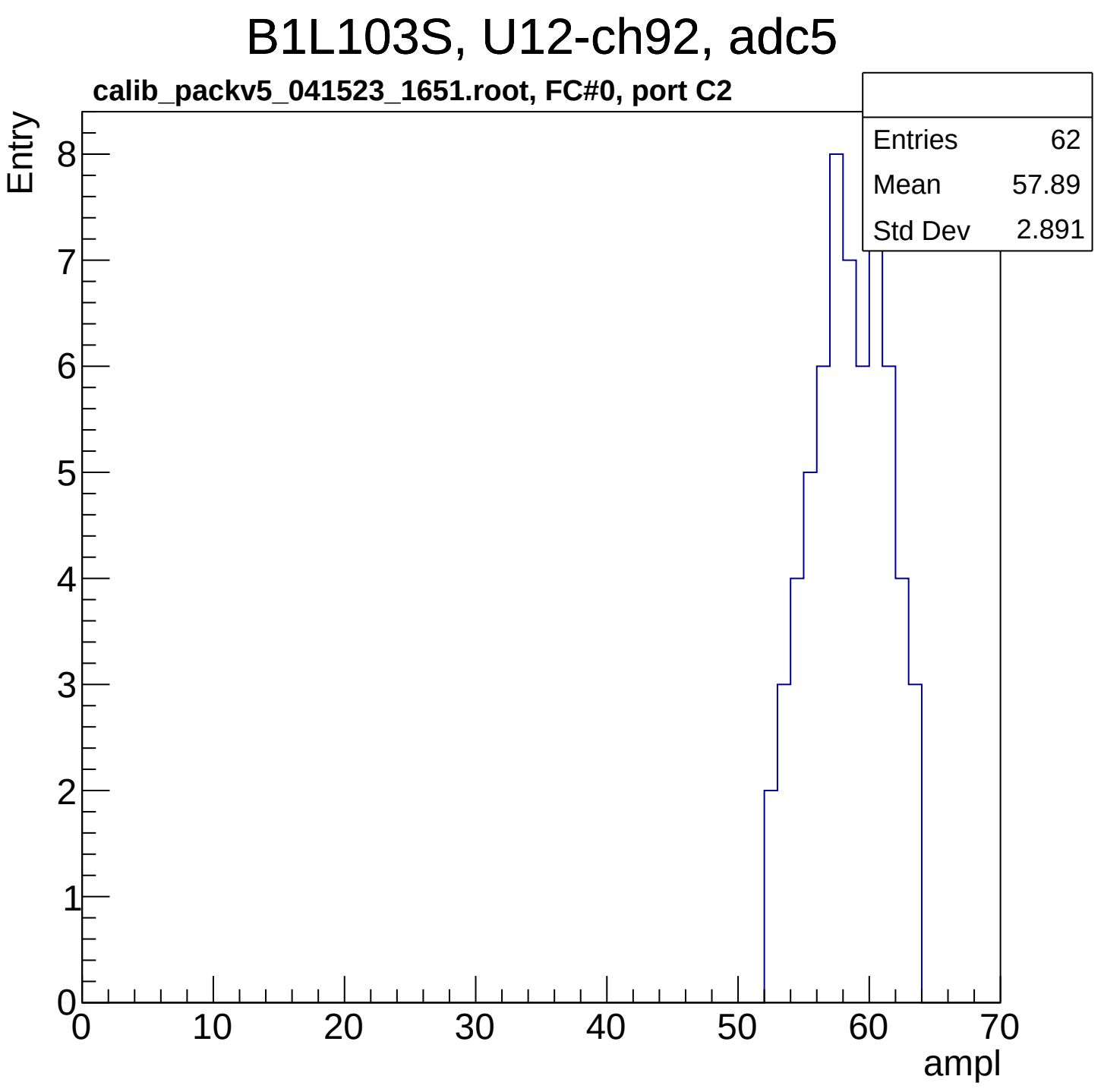
B1L103S, U12-ch92, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 57.89
Std Dev 2.891
Entry
ampl
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1
2
3
4
5
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7
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0
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60
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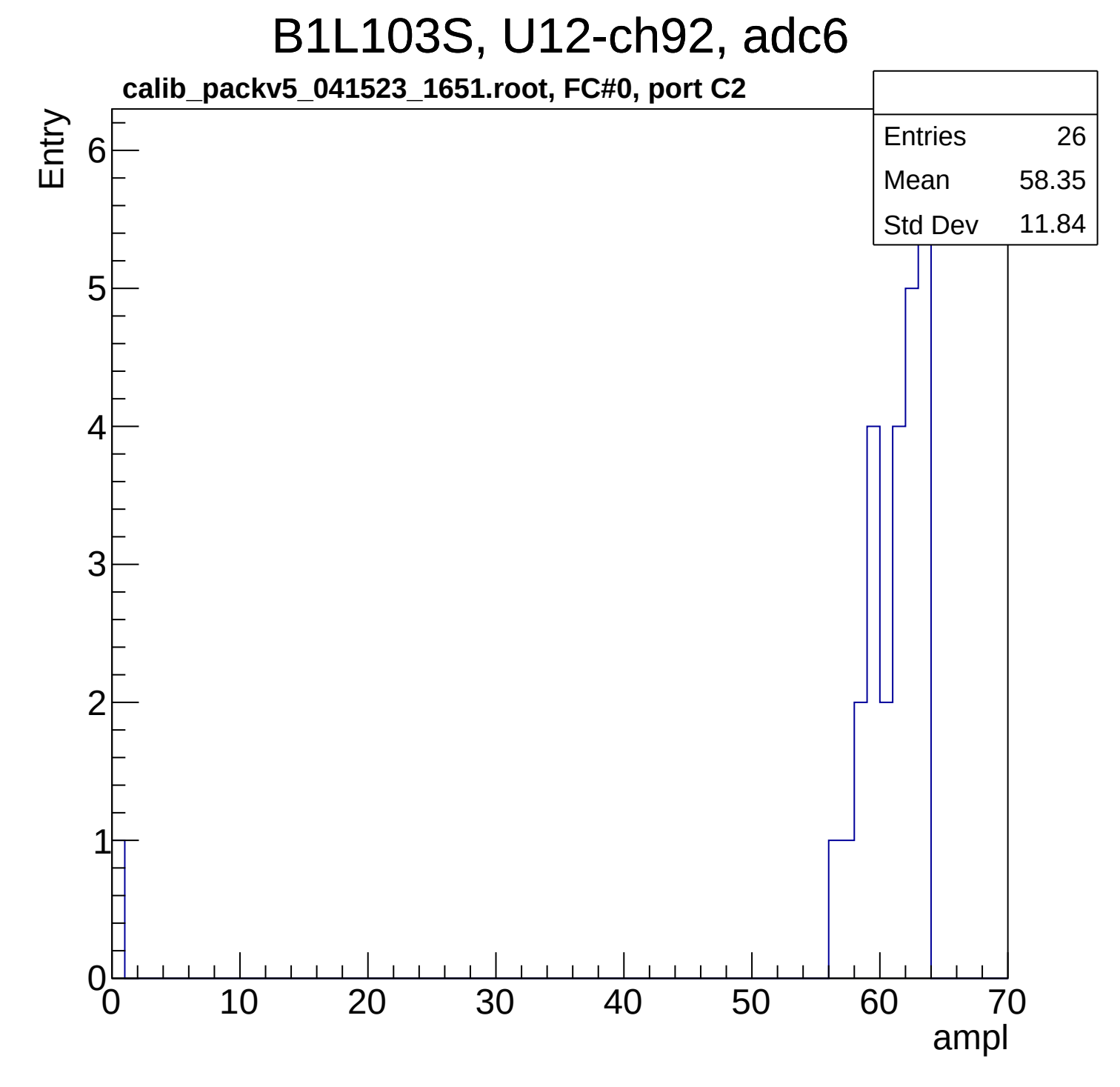
B1L103S, U12-ch92, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 26
Mean 58.35
Std Dev 11.84
Entry
0
1
2
3
4
5
6
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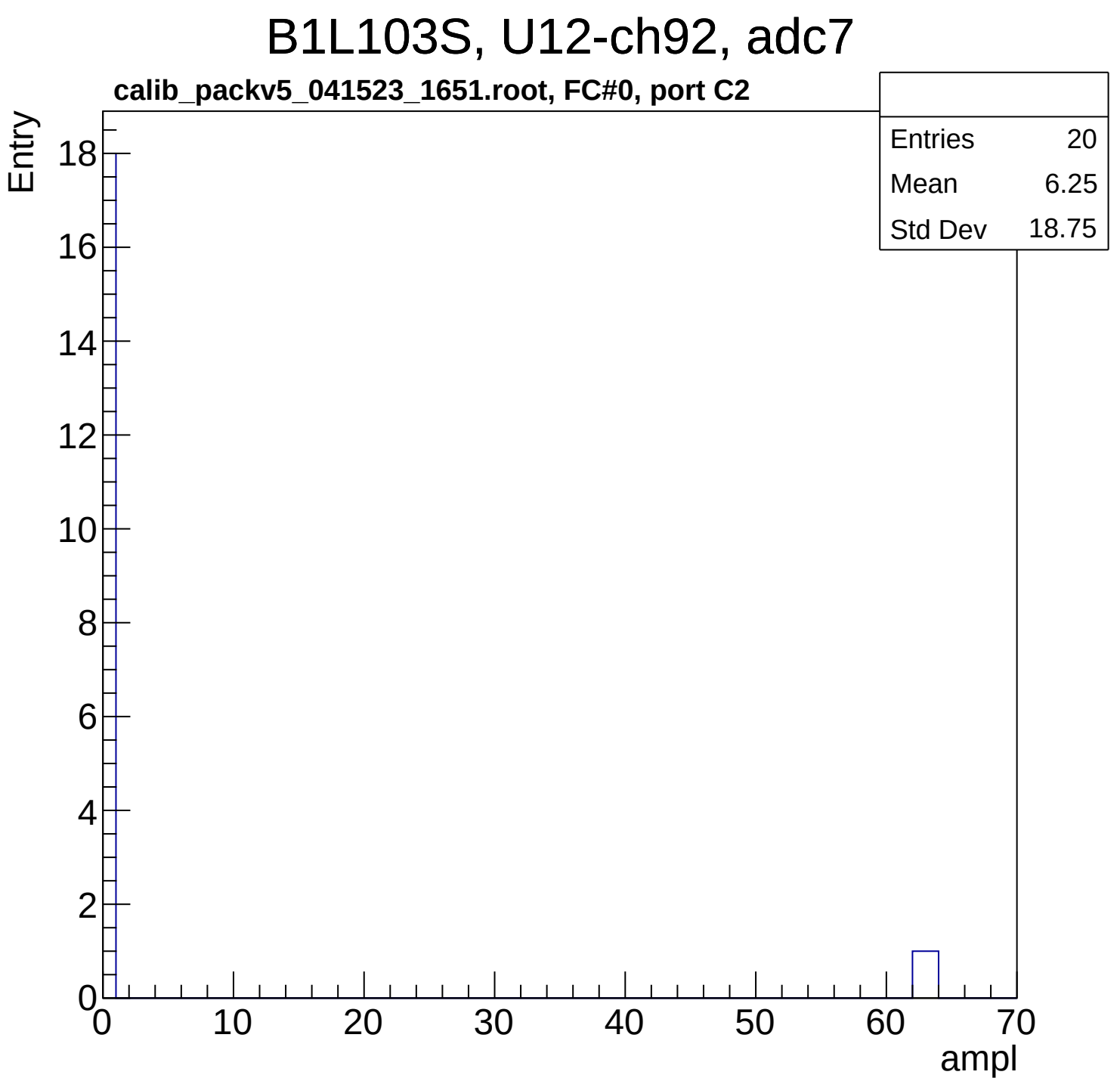
70
ampl


B1L103S, U12-ch92, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 6.25
Std Dev 18.75
Entry
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8
10
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16
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10
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50
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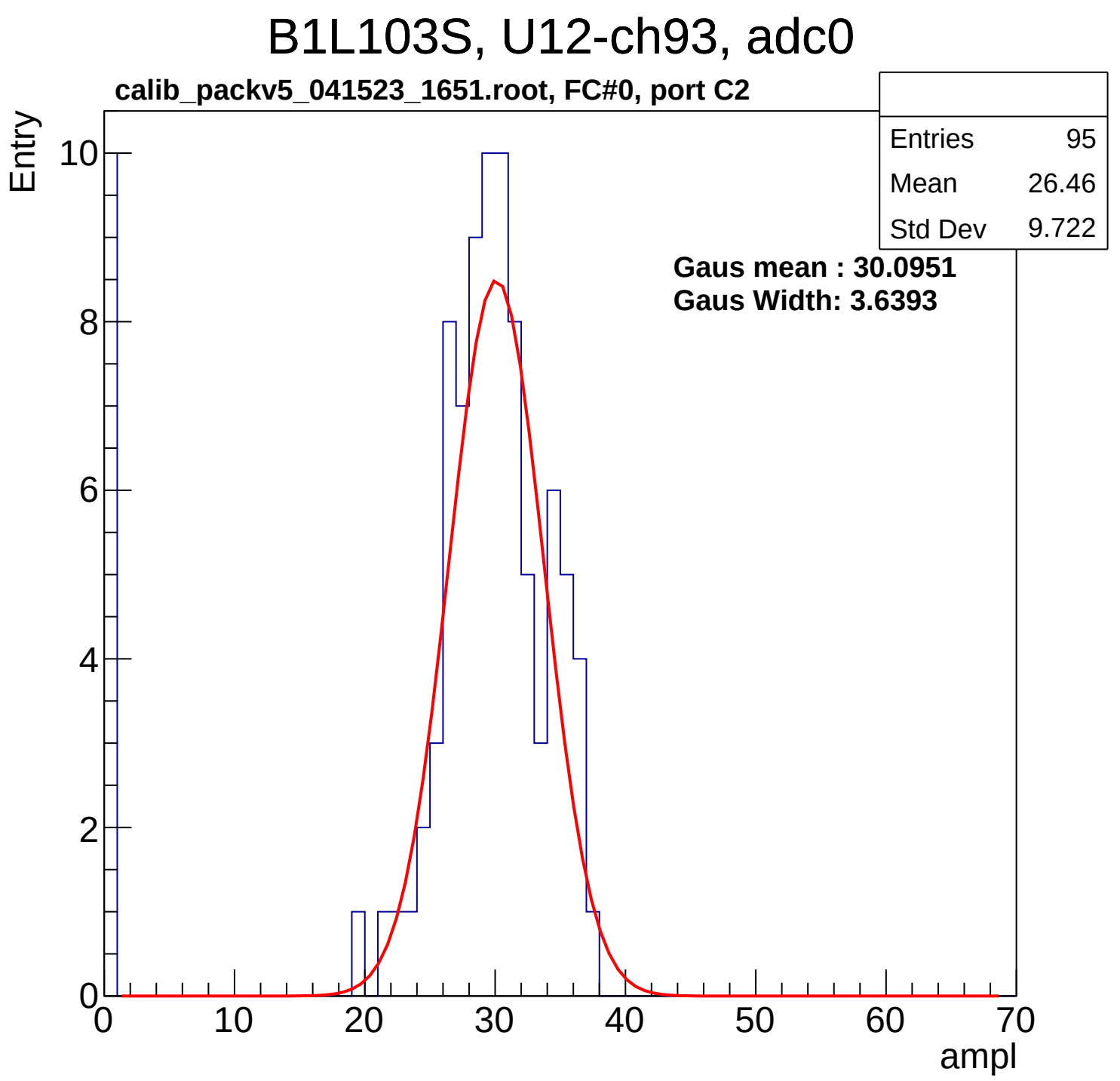
70
ampl


B1L103S, U12-ch93, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 26.46
Std Dev 9.722
Gaus mean : 30.0951
Gaus Width: 3.6393
Entry
ampl
0
2
4
6
8
10
0
10
20
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40
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60
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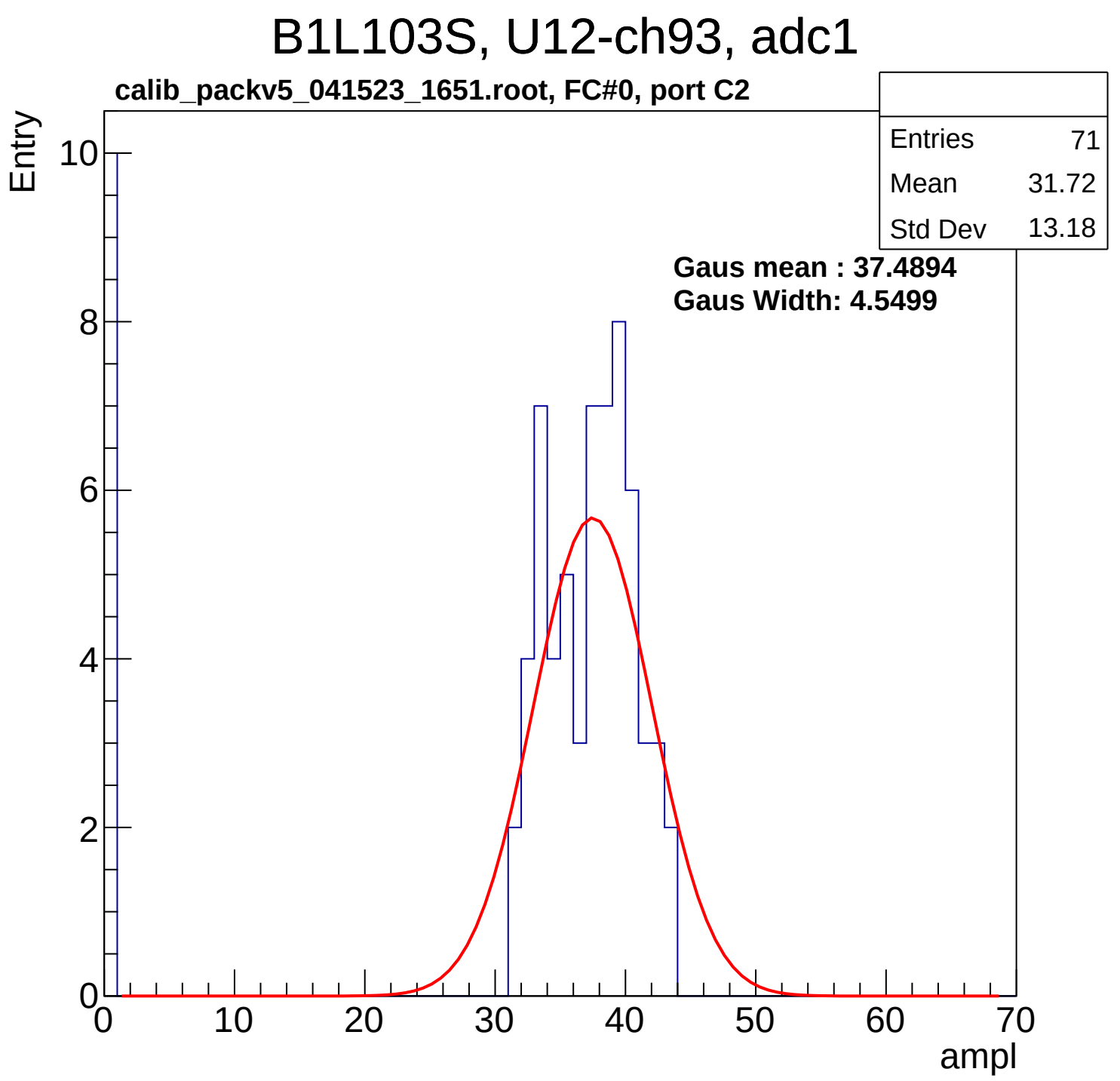
B1L103S, U12-ch93, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 31.72
Std Dev 13.18
Gaus mean : 37.4894
Gaus Width: 4.5499
Entry
ampl
0
2
4
6
8
10
0
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40
50
60
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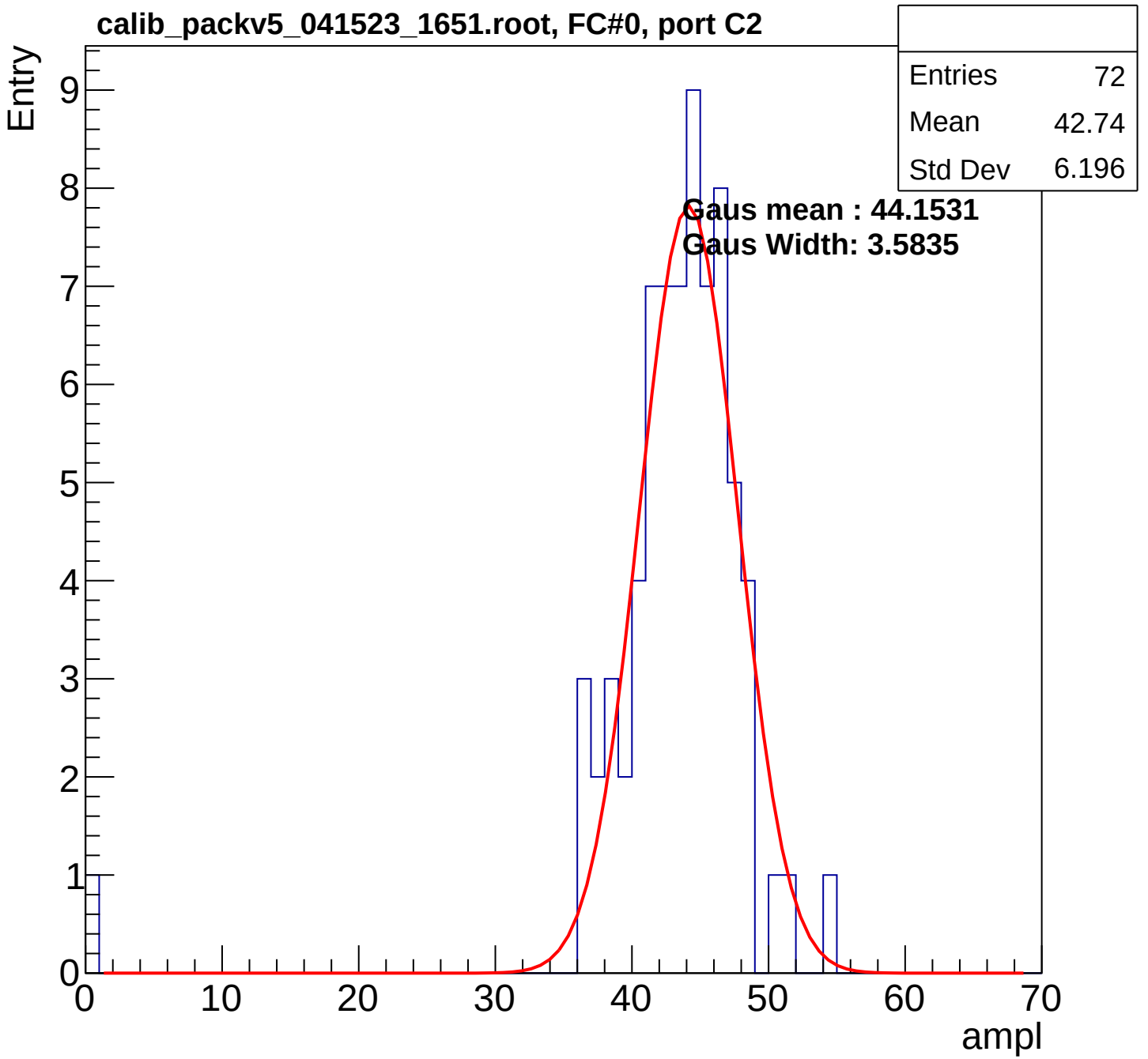
B1L103S, U12-ch93, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 42.74
Std Dev 6.196
Gaus mean : 44.1531
Gaus Width: 3.5835
Entry
ampl
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2
3
4
5
6
7
8
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0
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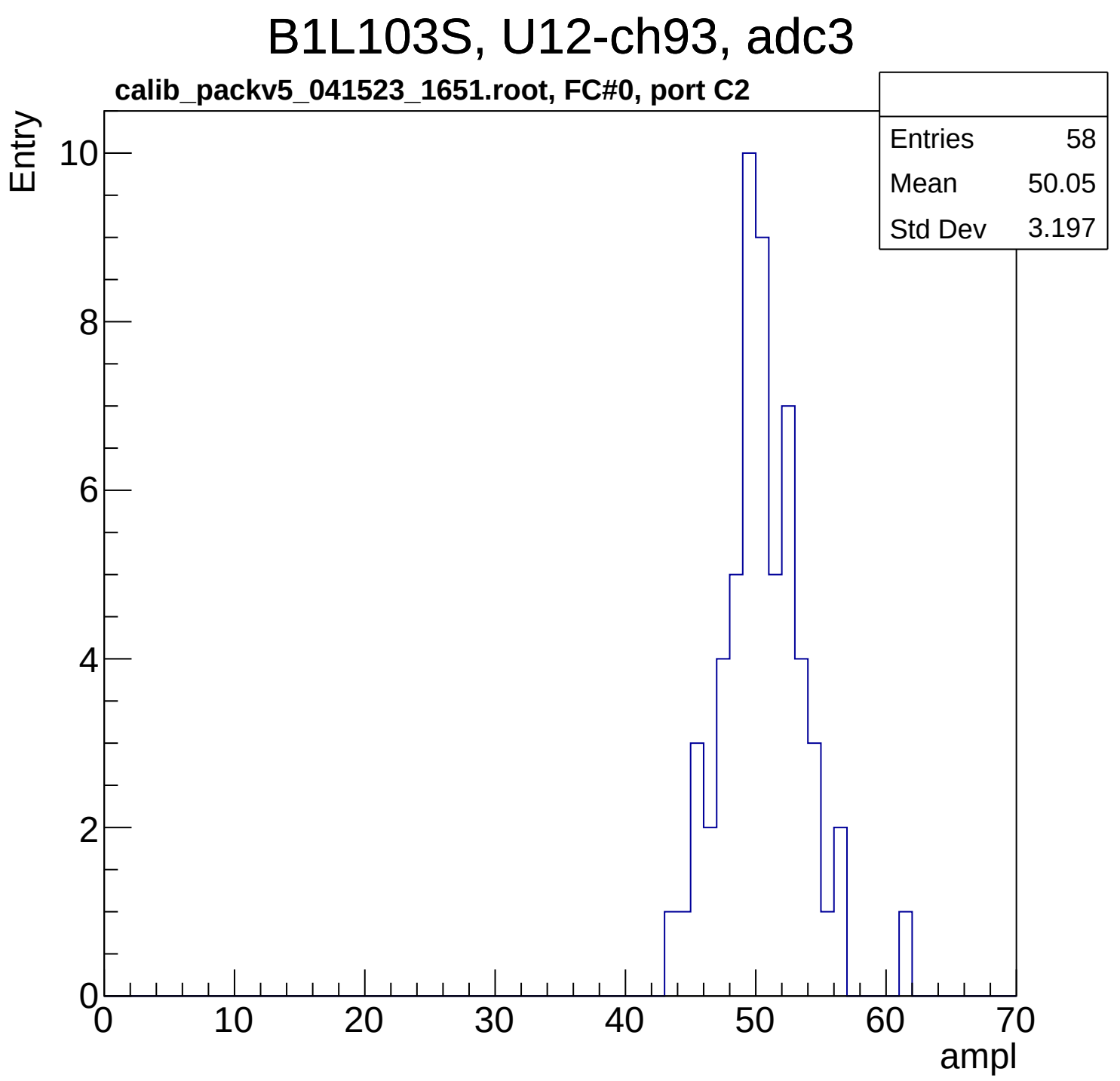
B1L103S, U12-ch93, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 50.05
Std Dev 3.197
Entry
ampl
0
2
4
6
8
10
0
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40
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60
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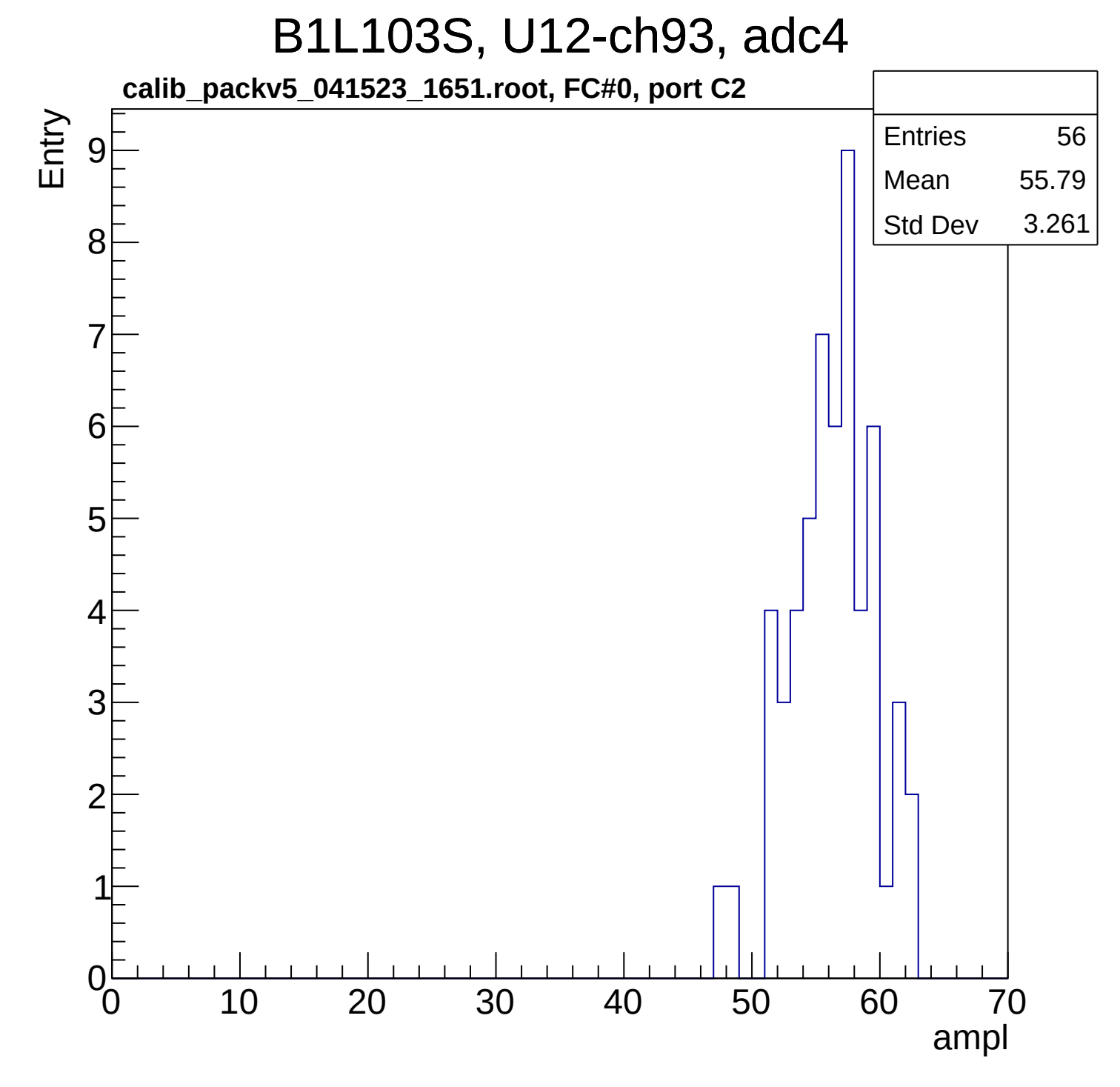
B1L103S, U12-ch93, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 55.79
Std Dev 3.261
Entry
ampl
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2
3
4
5
6
7
8
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0
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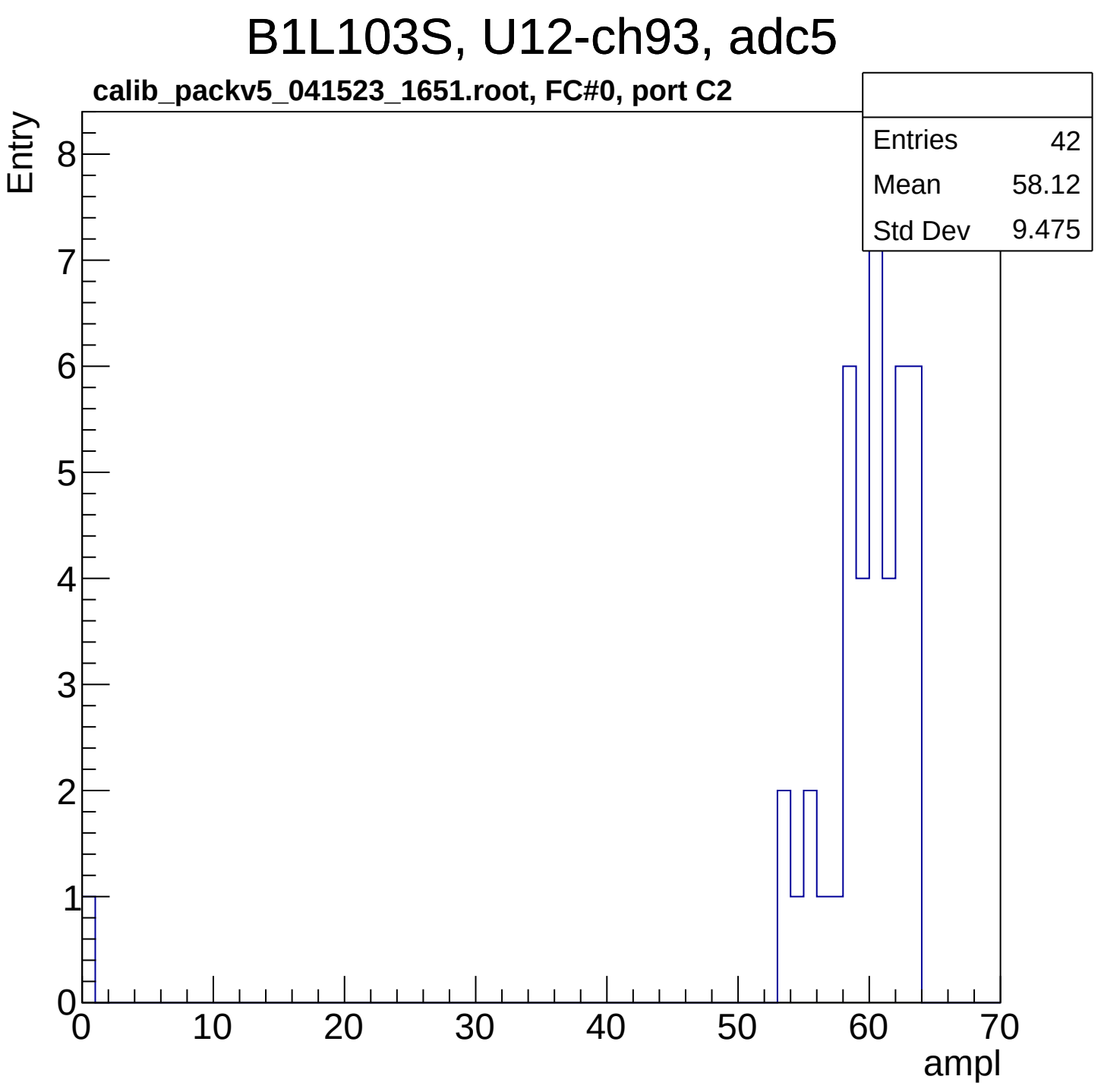
B1L103S, U12-ch93, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 42
Mean 58.12
Std Dev 9.475
Entry
ampl
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1
2
3
4
5
6
7
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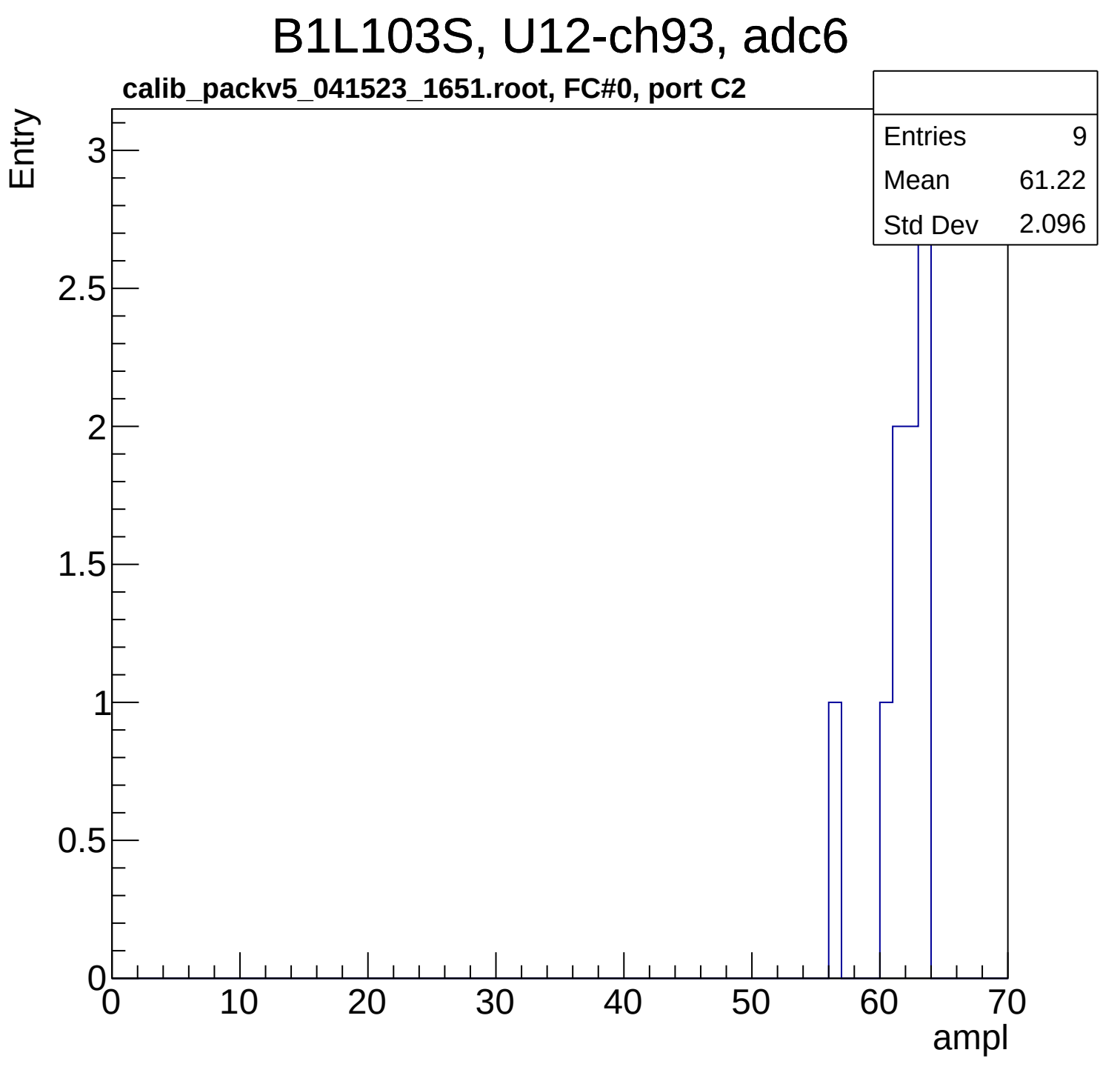
B1L103S, U12-ch93, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 61.22
Std Dev 2.096
Entry
ampl
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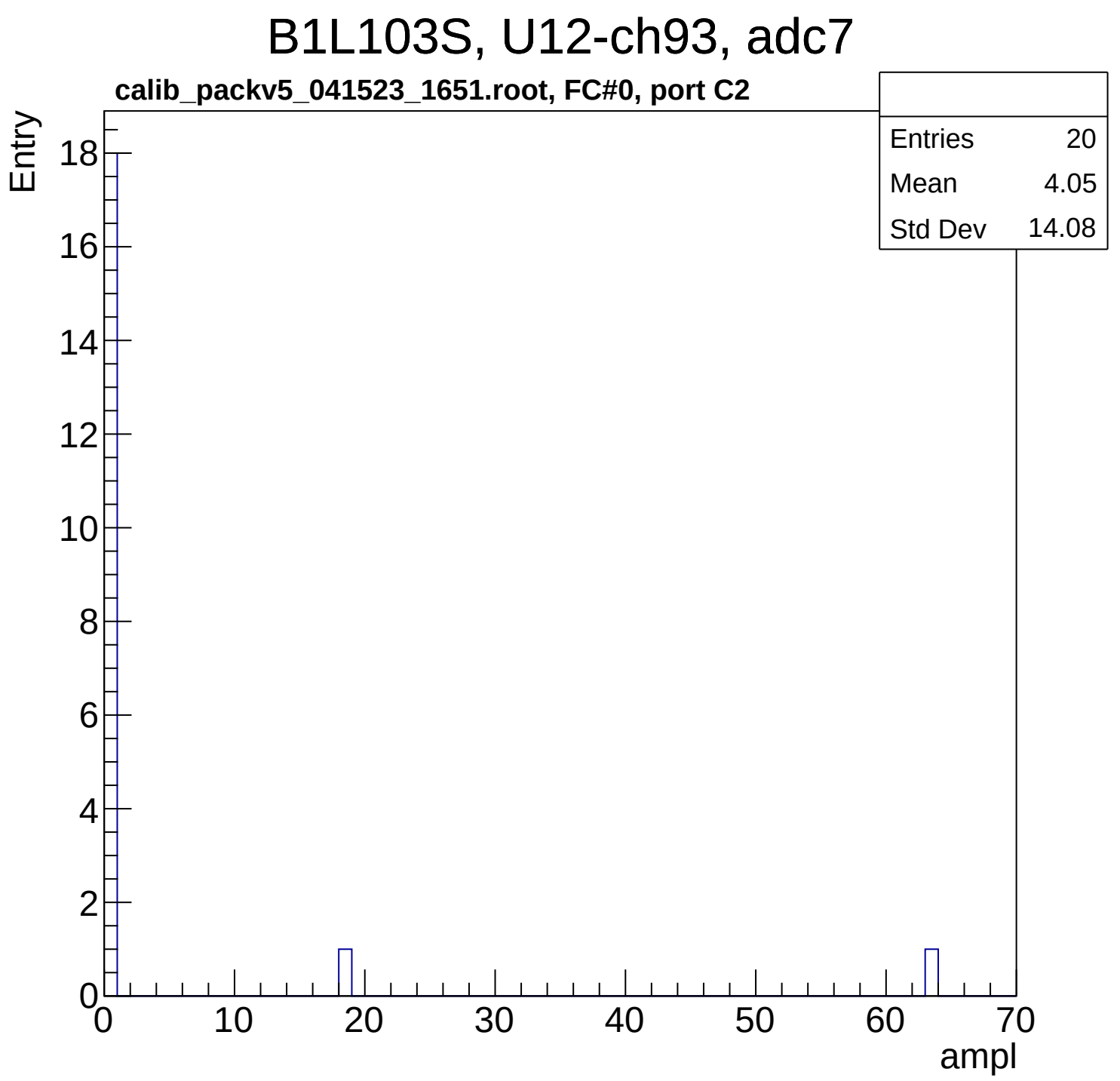
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U12-ch93, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.05
Std Dev 14.08
Entry
0
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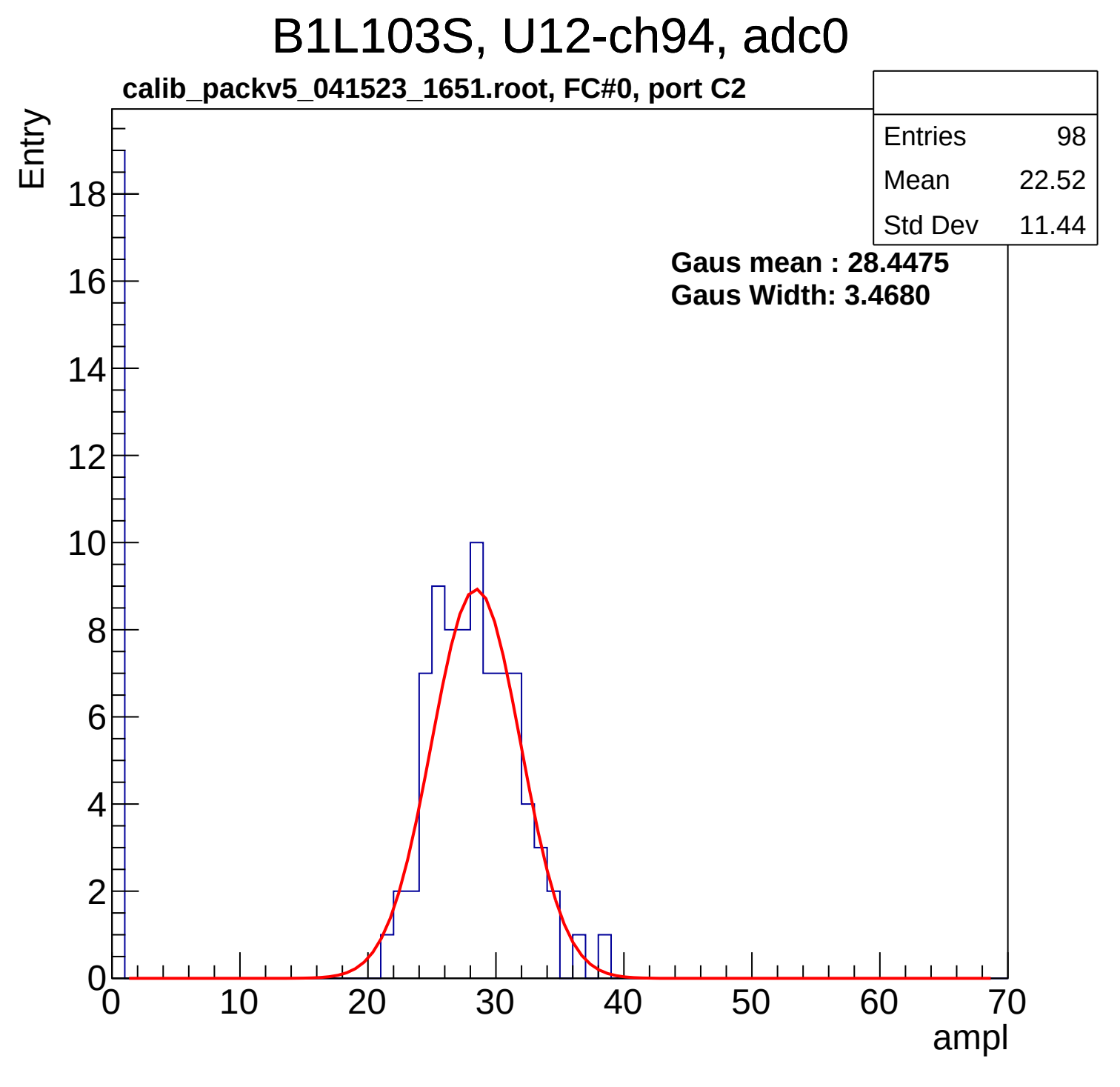
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch94, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 22.52
Std Dev 11.44
Gaus mean : 28.4475
Gaus Width: 3.4680
Entry
ampl
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2
4
6
8
10
12
14
16
18
0
10
20
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40
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60
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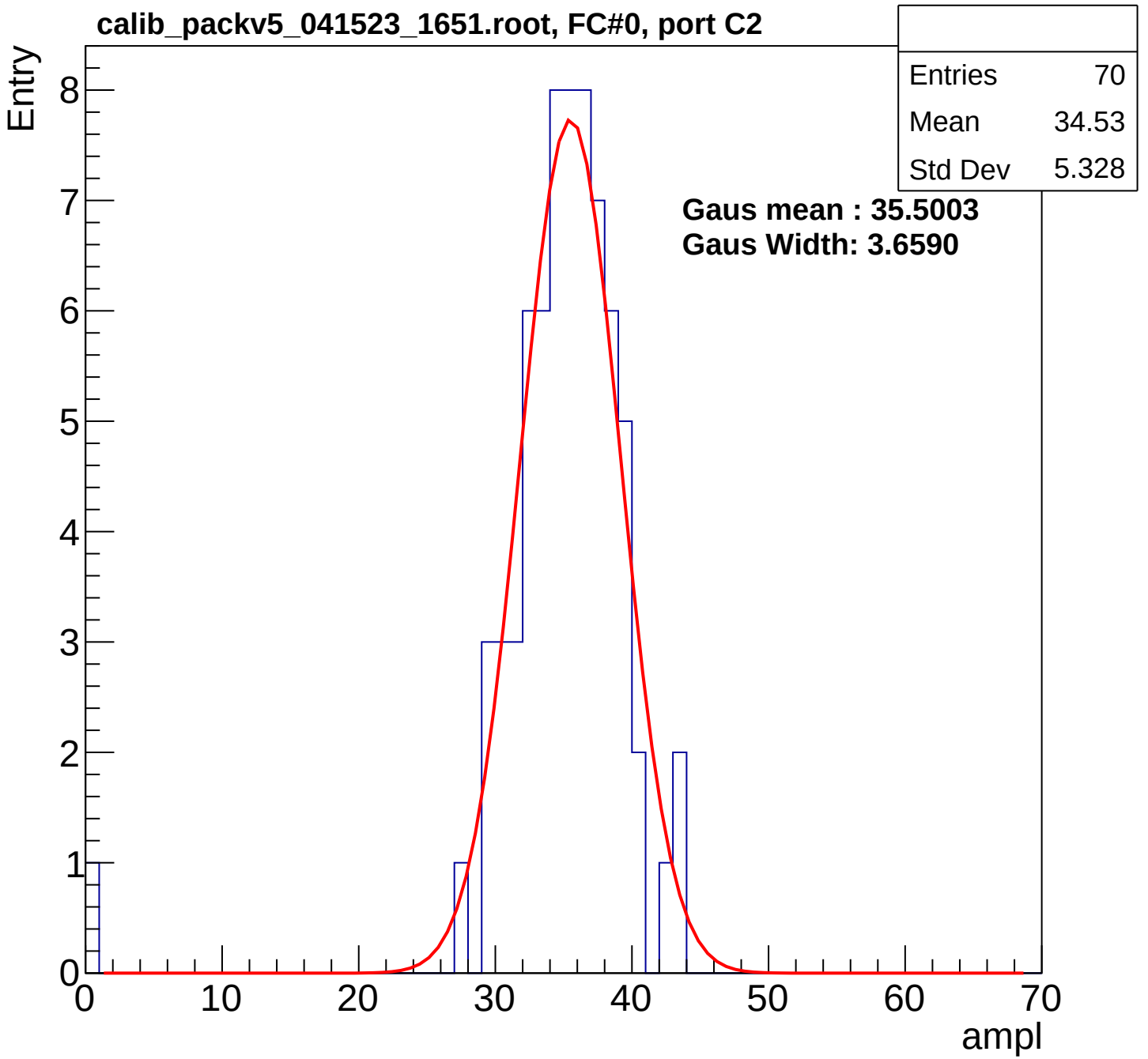
B1L103S, U12-ch94, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 34.53
Std Dev 5.328
Gaus mean : 35.5003
Gaus Width: 3.6590
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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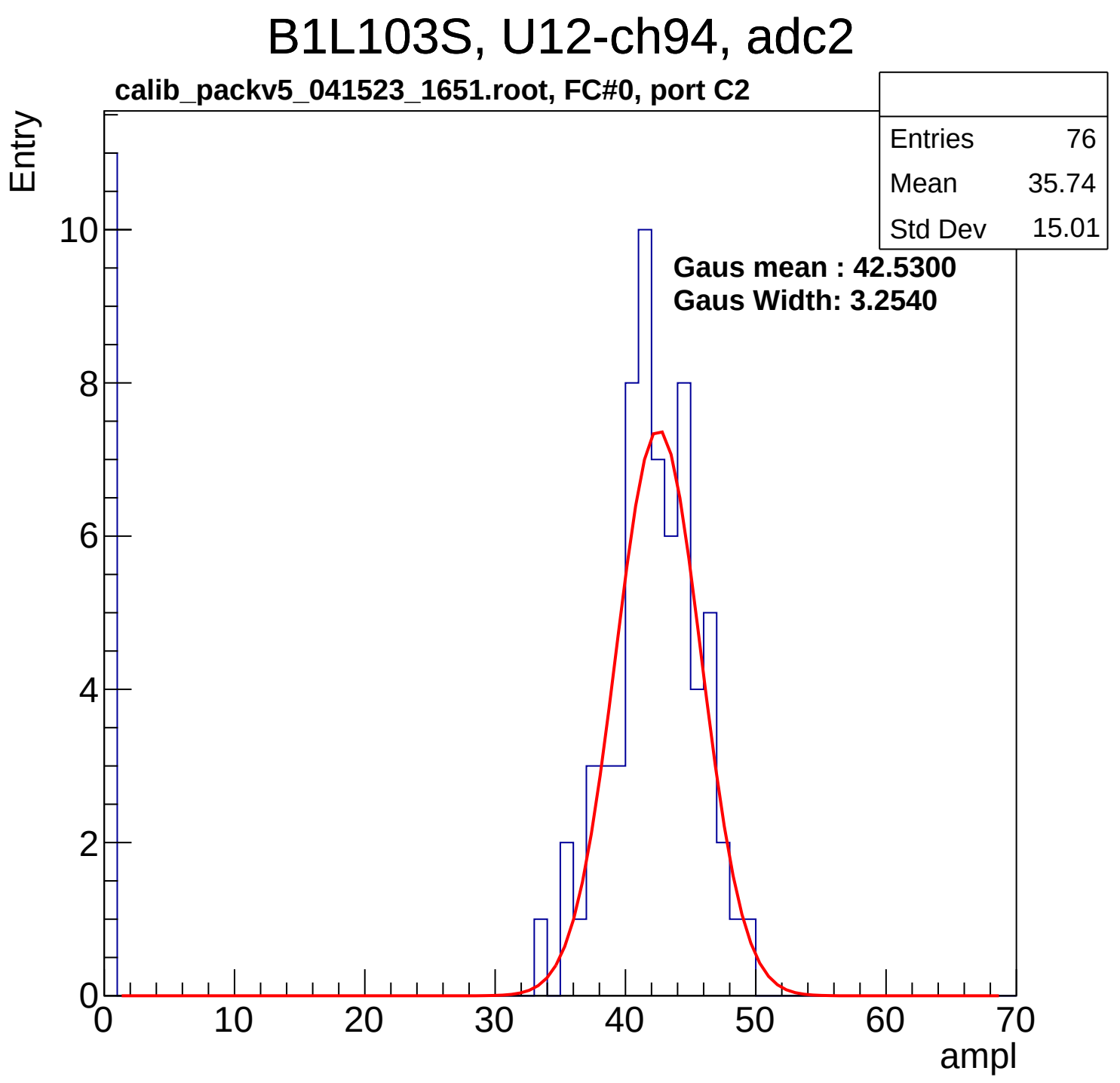
B1L103S, U12-ch94, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 35.74
Std Dev 15.01
Gaus mean : 42.5300
Gaus Width: 3.2540
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
50
60
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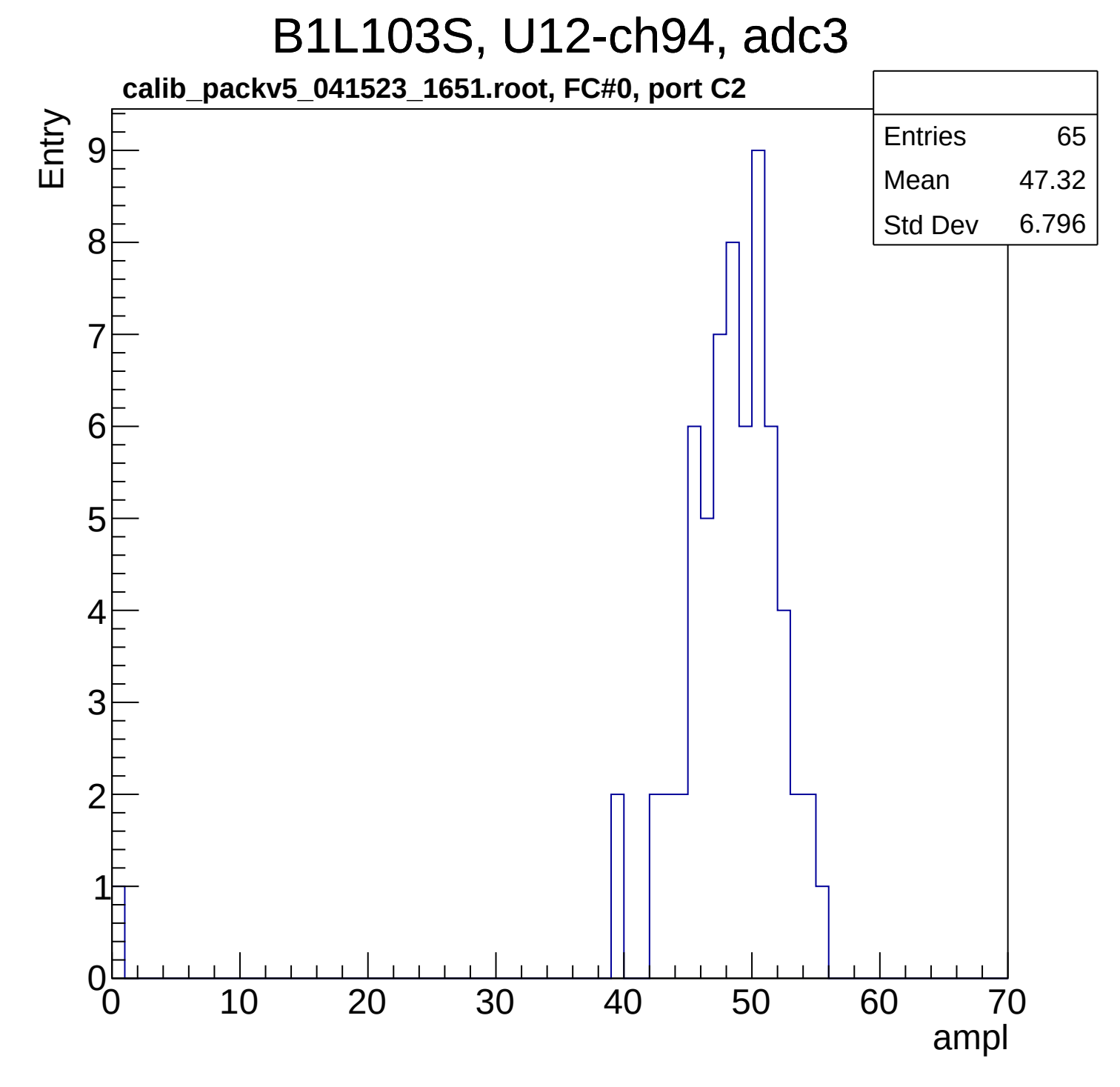
B1L103S, U12-ch94, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 47.32
Std Dev 6.796
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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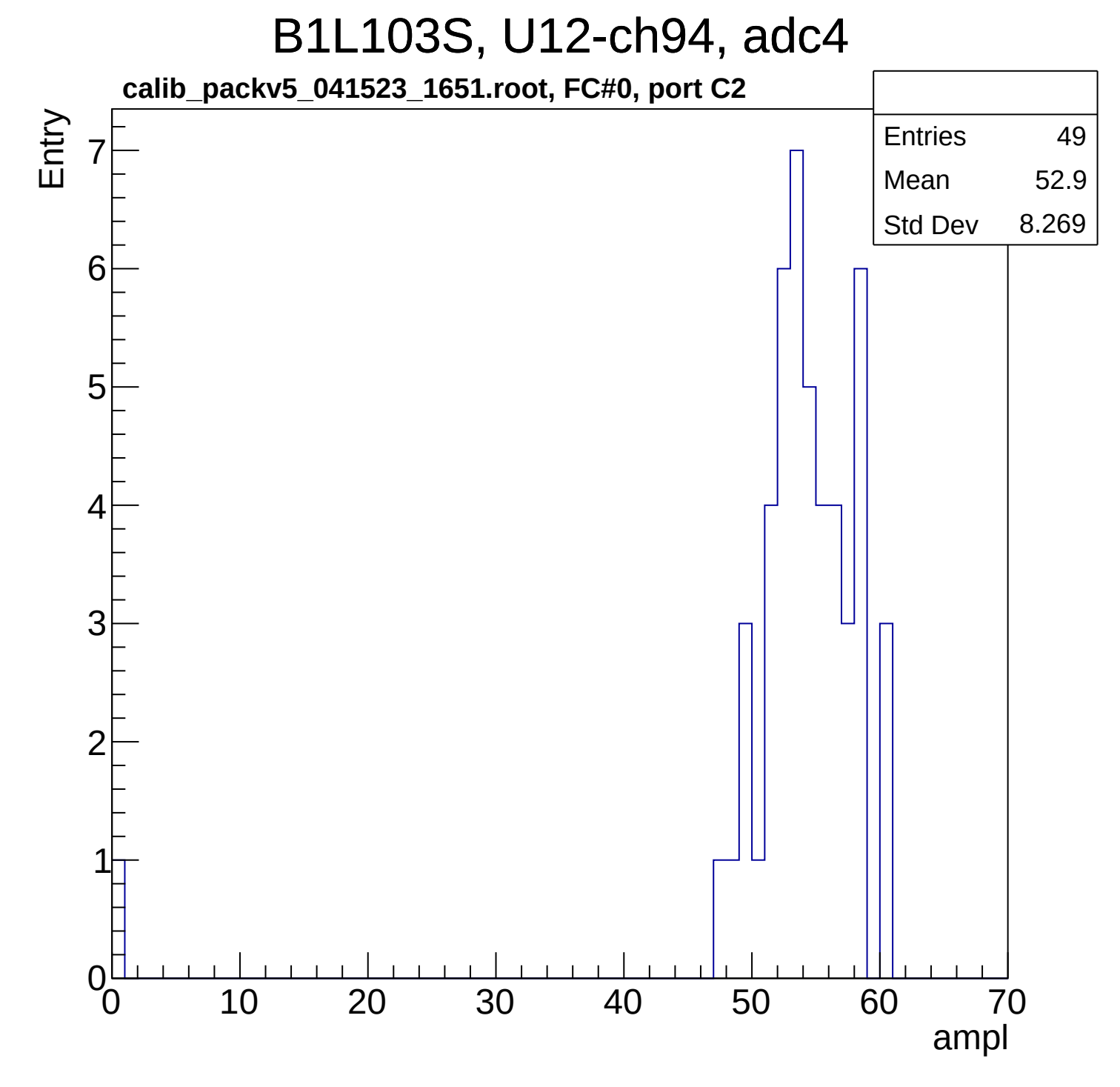
B1L103S, U12-ch94, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 52.9
Std Dev 8.269
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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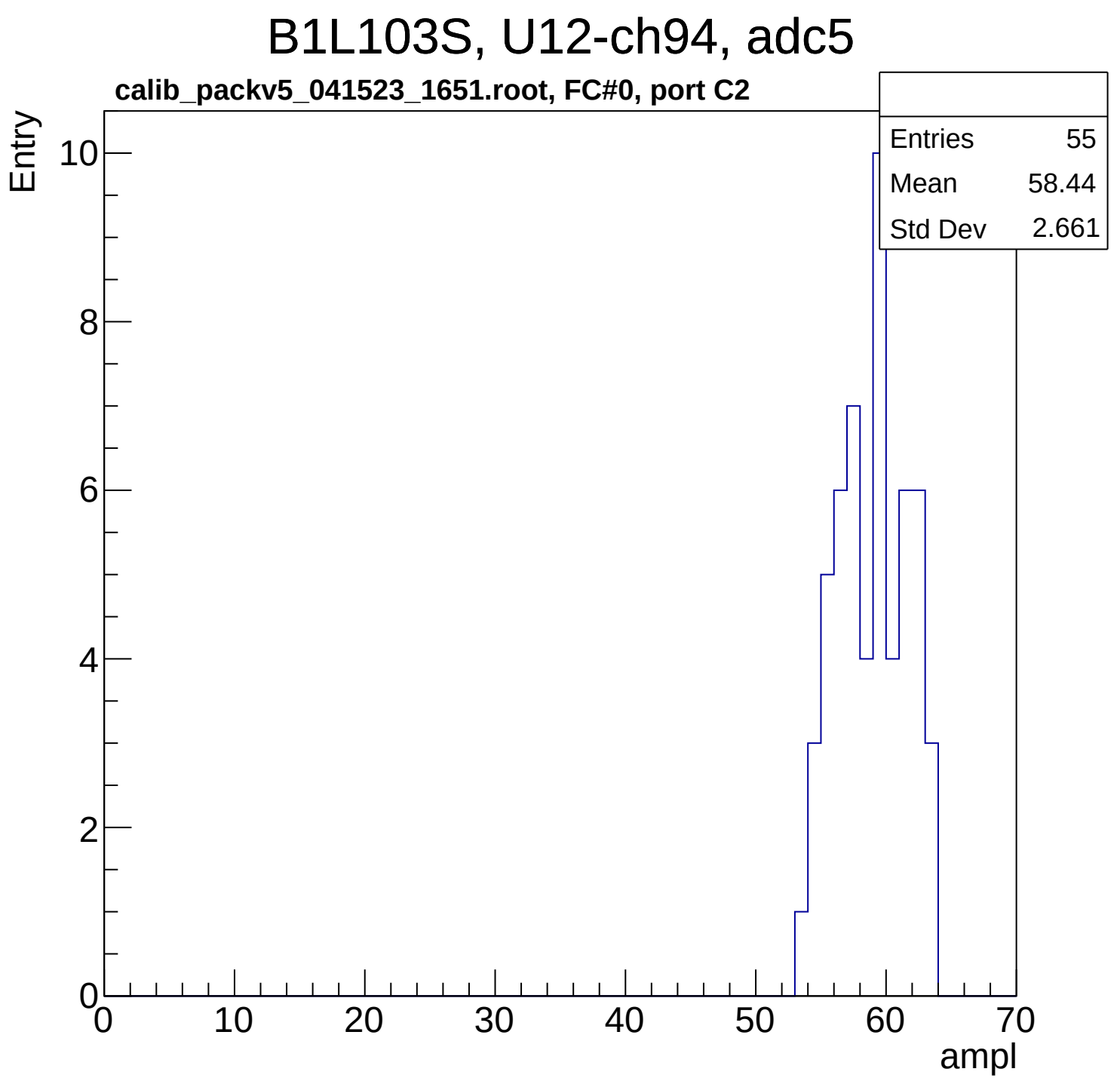
B1L103S, U12-ch94, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.44
Std Dev 2.661
Entry
0
2
4
6
8
10
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10
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30
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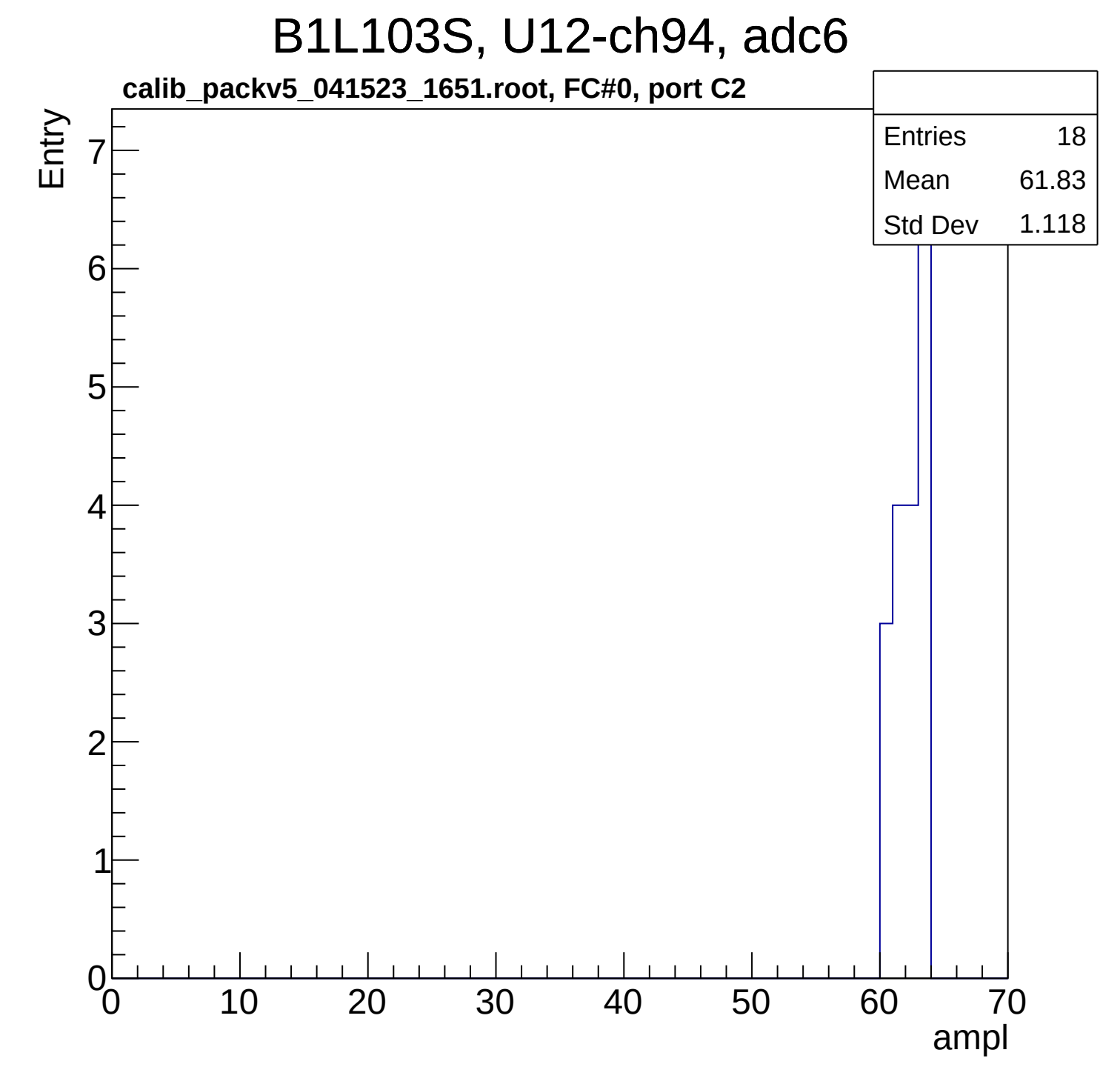
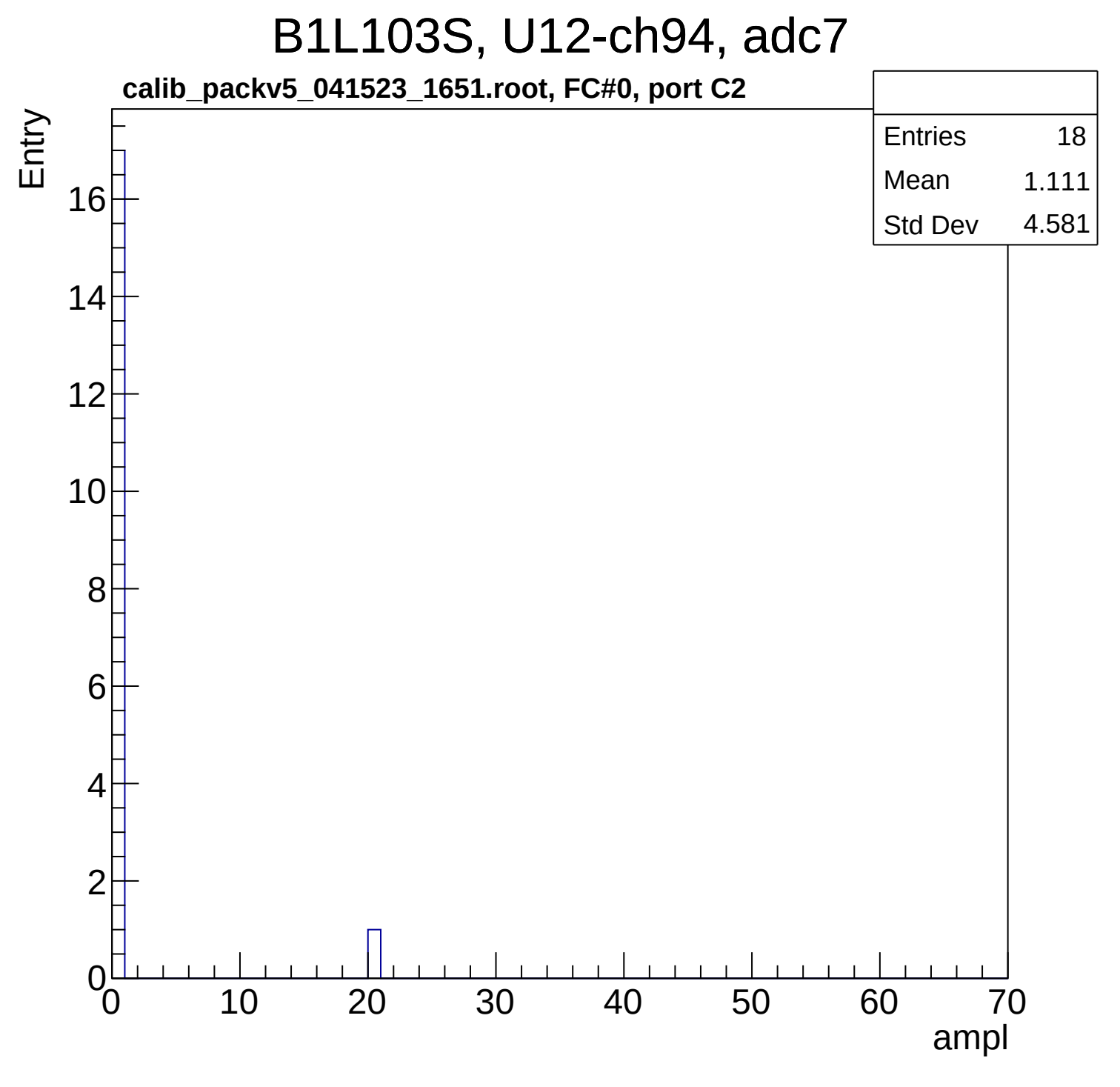
50
60
70
ampl


B1L103S, U12-ch94, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 61.83
Std Dev 1.118
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U12-ch94, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 1.111
Std Dev 4.581
Entry
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6
8
10
12
14
16
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10
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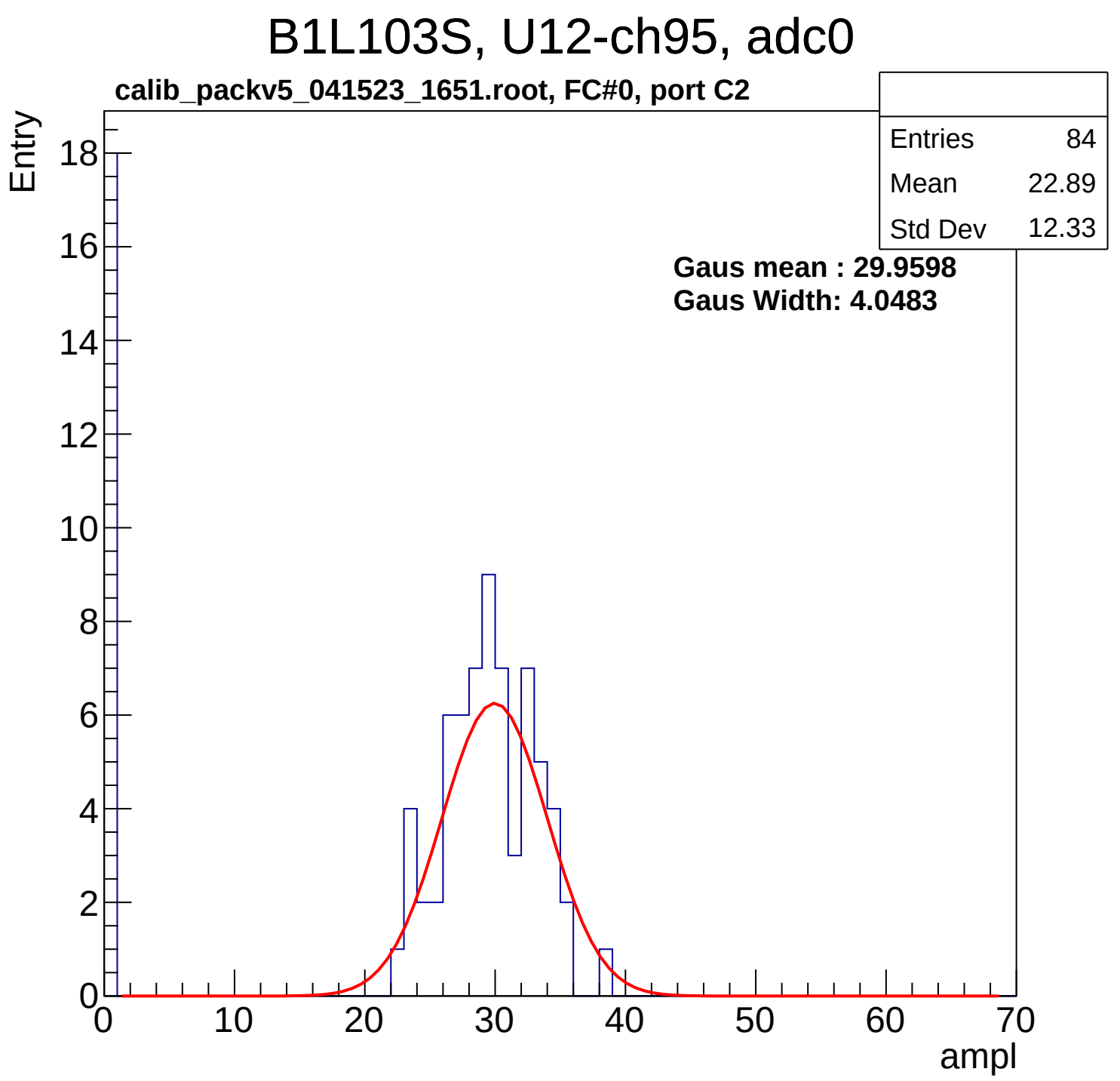
50
60
70
ampl


B1L103S, U12-ch95, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 22.89
Std Dev 12.33
Gaus mean : 29.9598
Gaus Width: 4.0483
Entry
ampl
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6
8
10
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0
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60
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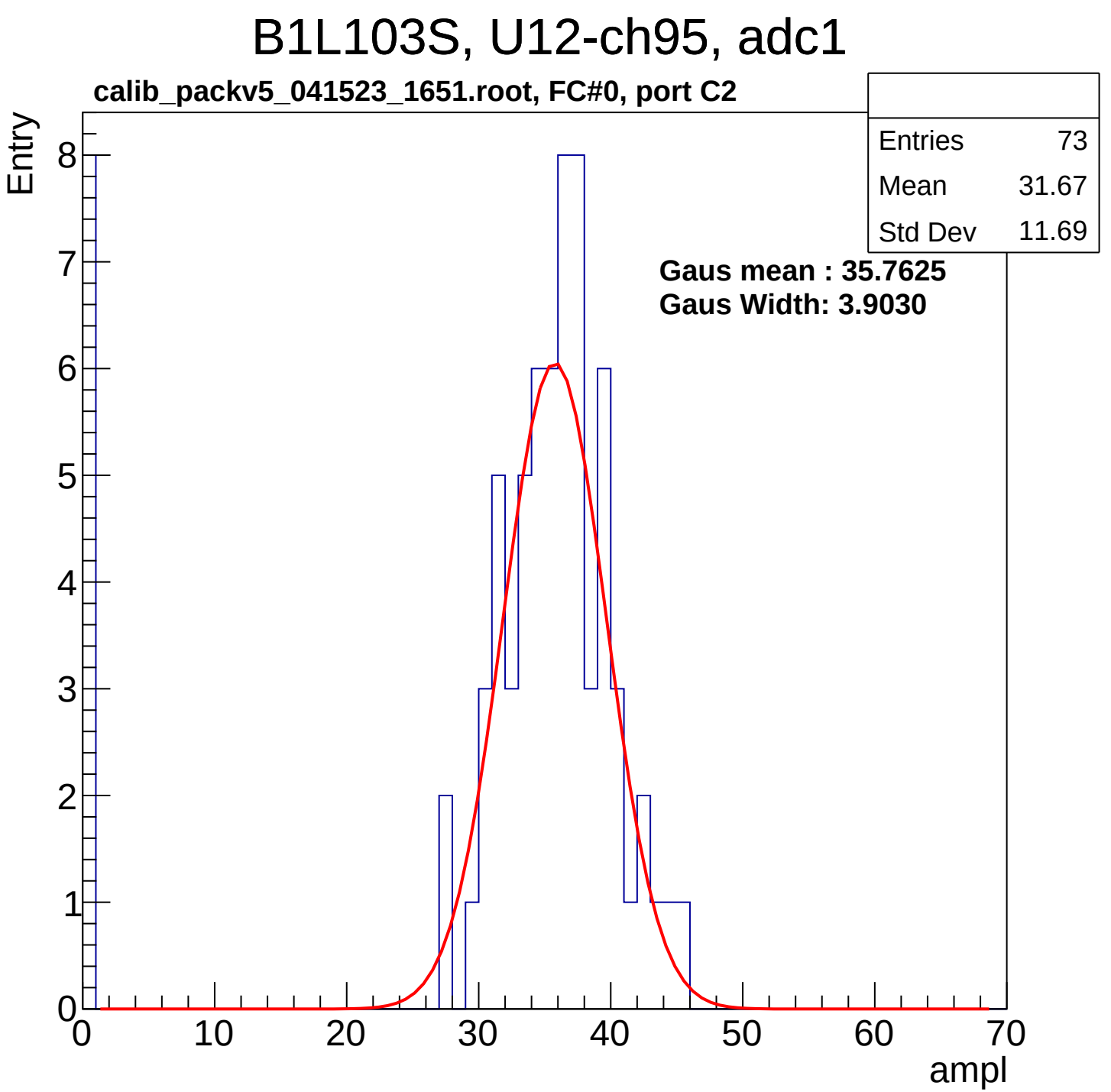
B1L103S, U12-ch95, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 31.67
Std Dev 11.69
Gaus mean : 35.7625
Gaus Width: 3.9030
Entry
ampl
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1
2
3
4
5
6
7
8
0
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40
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60
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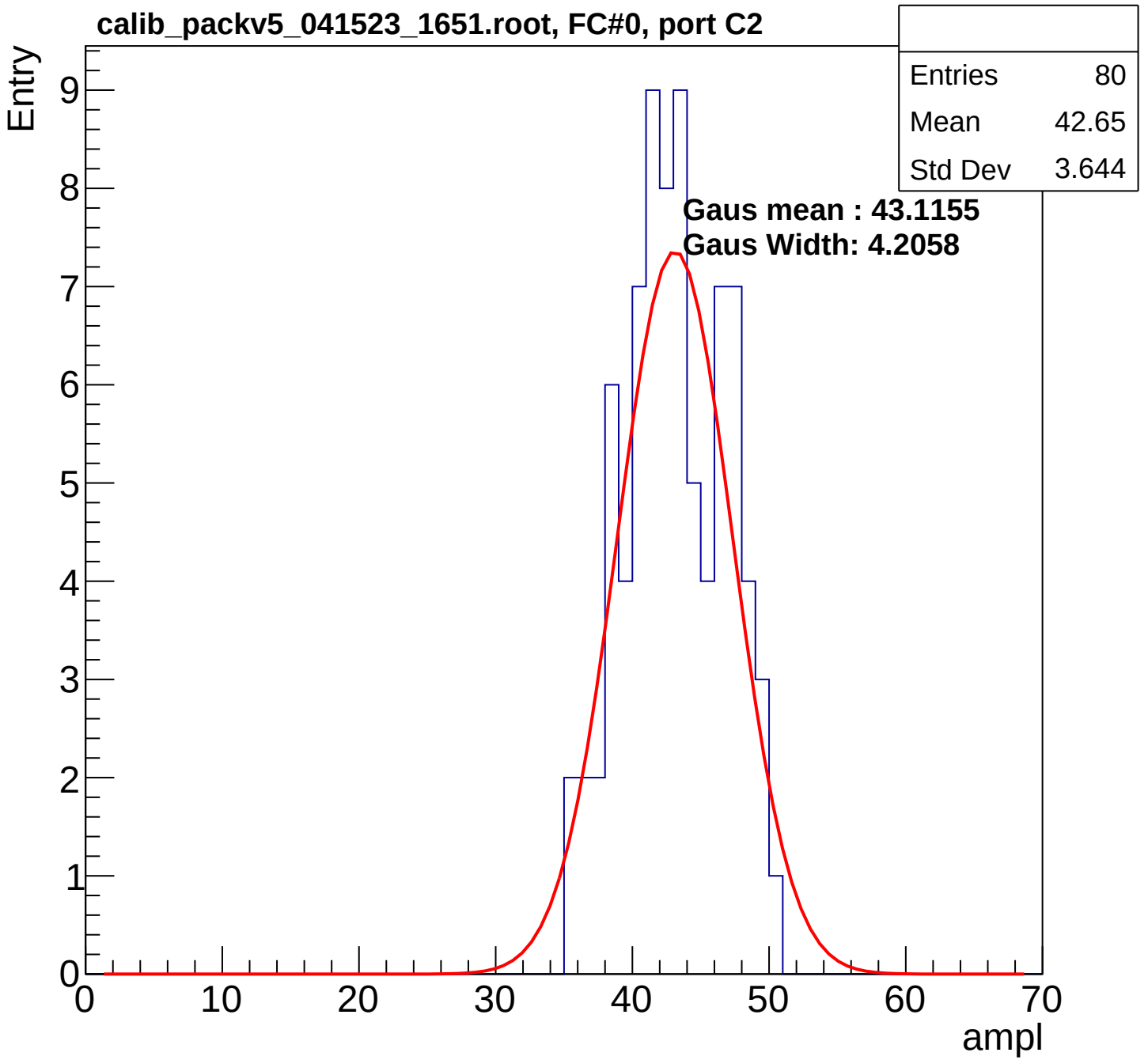
B1L103S, U12-ch95, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 42.65
Std Dev 3.644
Gaus mean : 43.1155
Gaus Width: 4.2058
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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60
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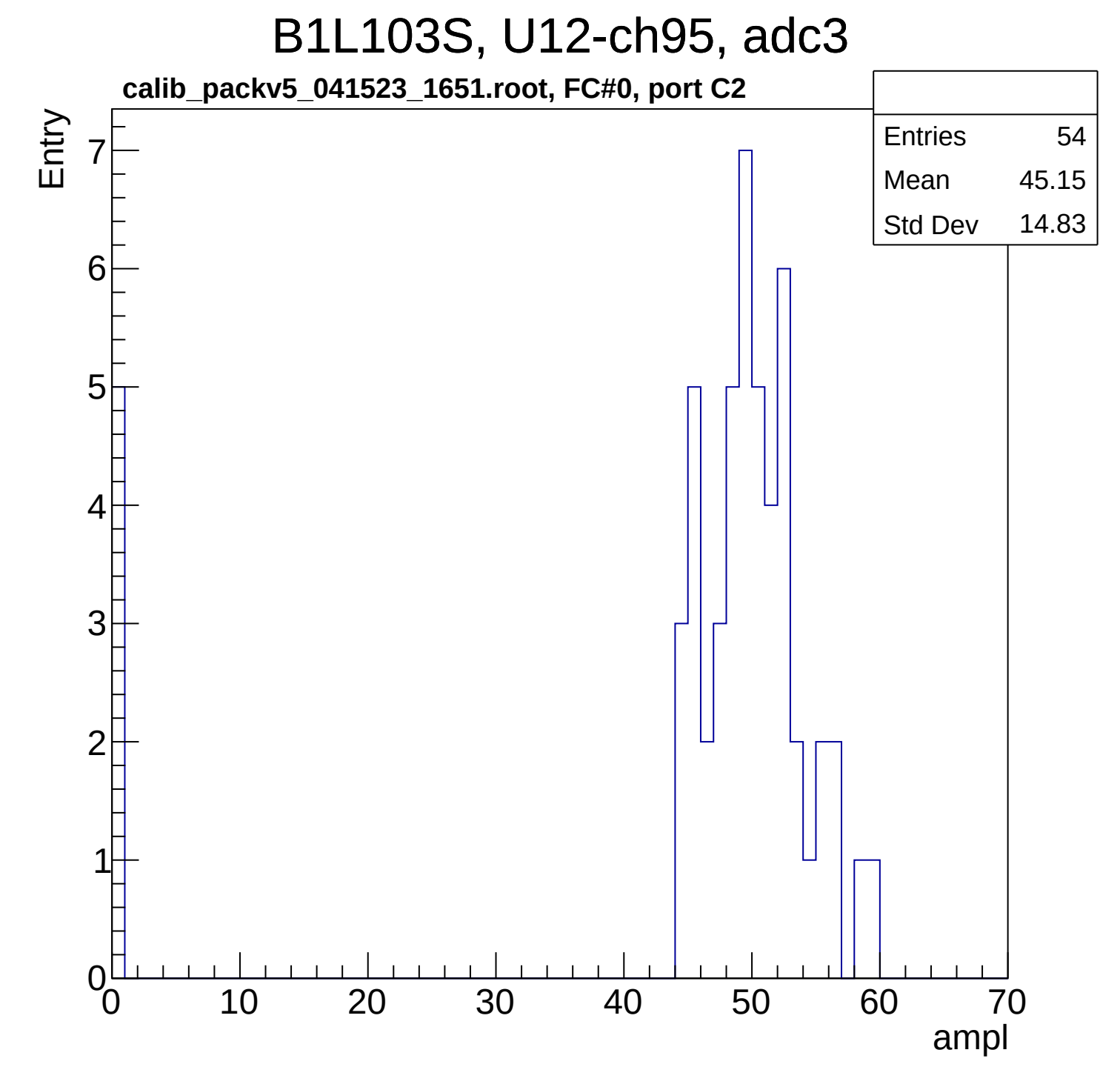
B1L103S, U12-ch95, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 45.15
Std Dev 14.83
Entry
ampl
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1
2
3
4
5
6
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0
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60
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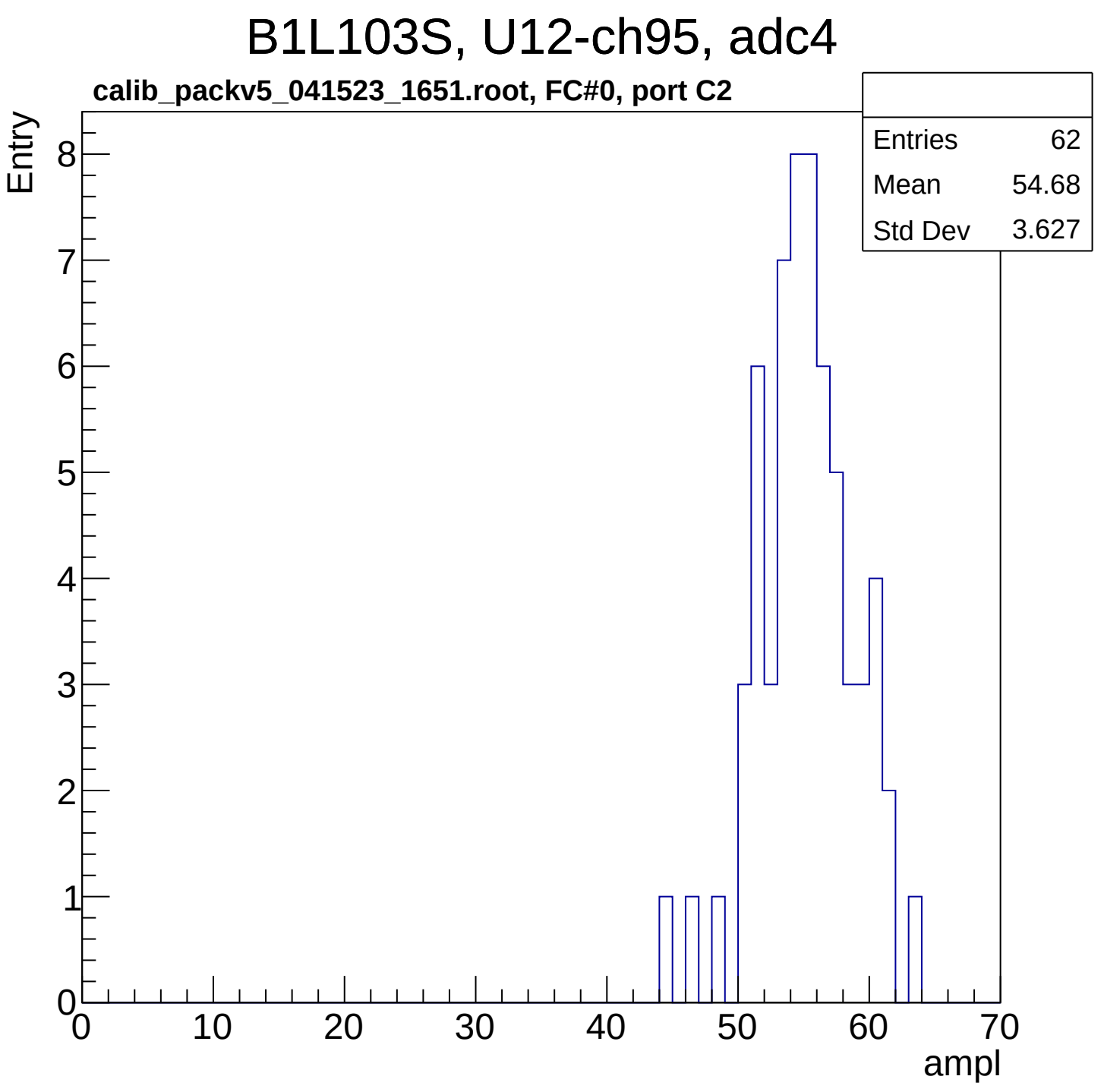
B1L103S, U12-ch95, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 54.68
Std Dev 3.627
Entry
ampl
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3
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5
6
7
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0
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60
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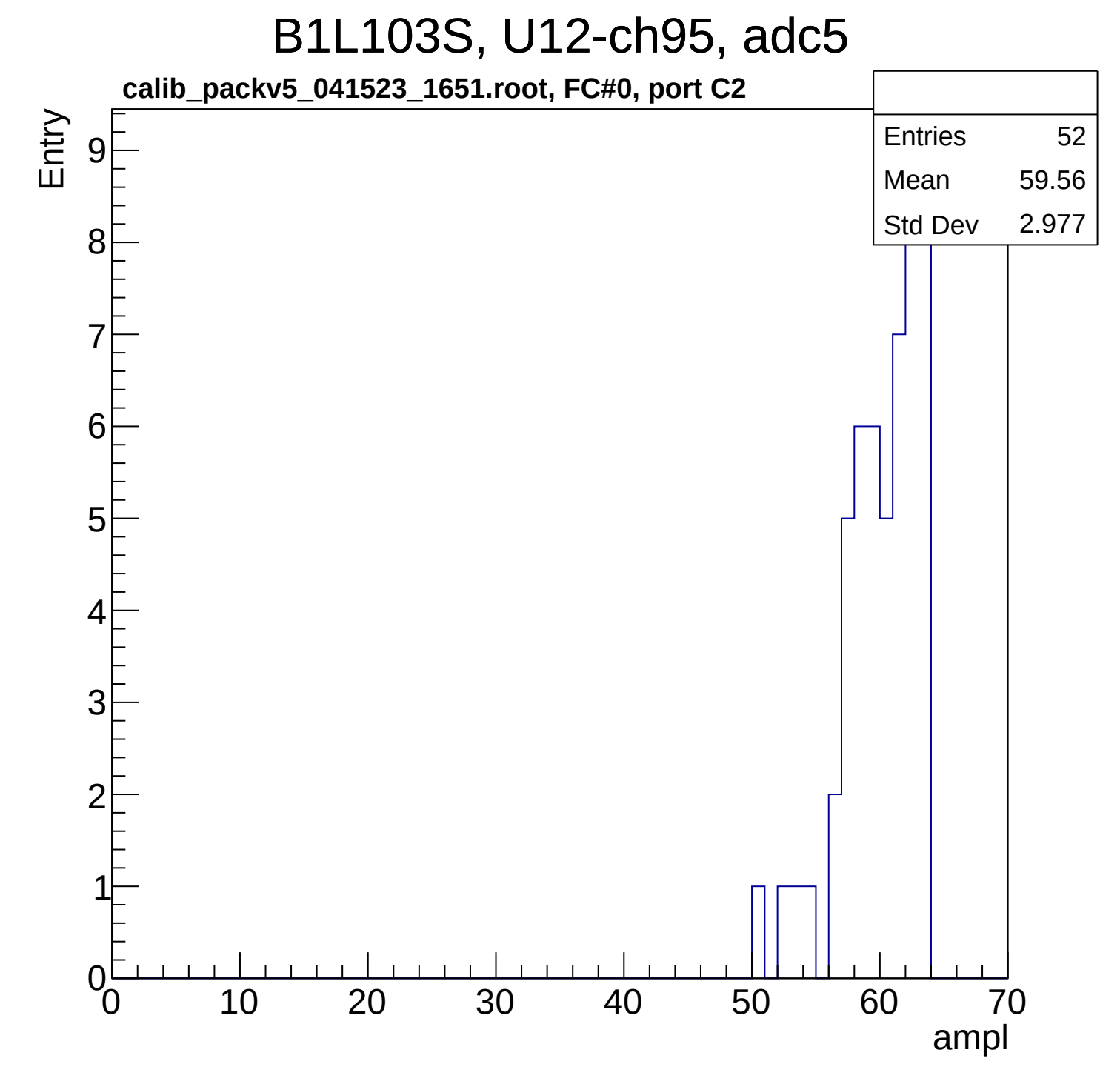
B1L103S, U12-ch95, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 59.56
Std Dev 2.977
Entry
ampl
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4
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6
7
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0
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60
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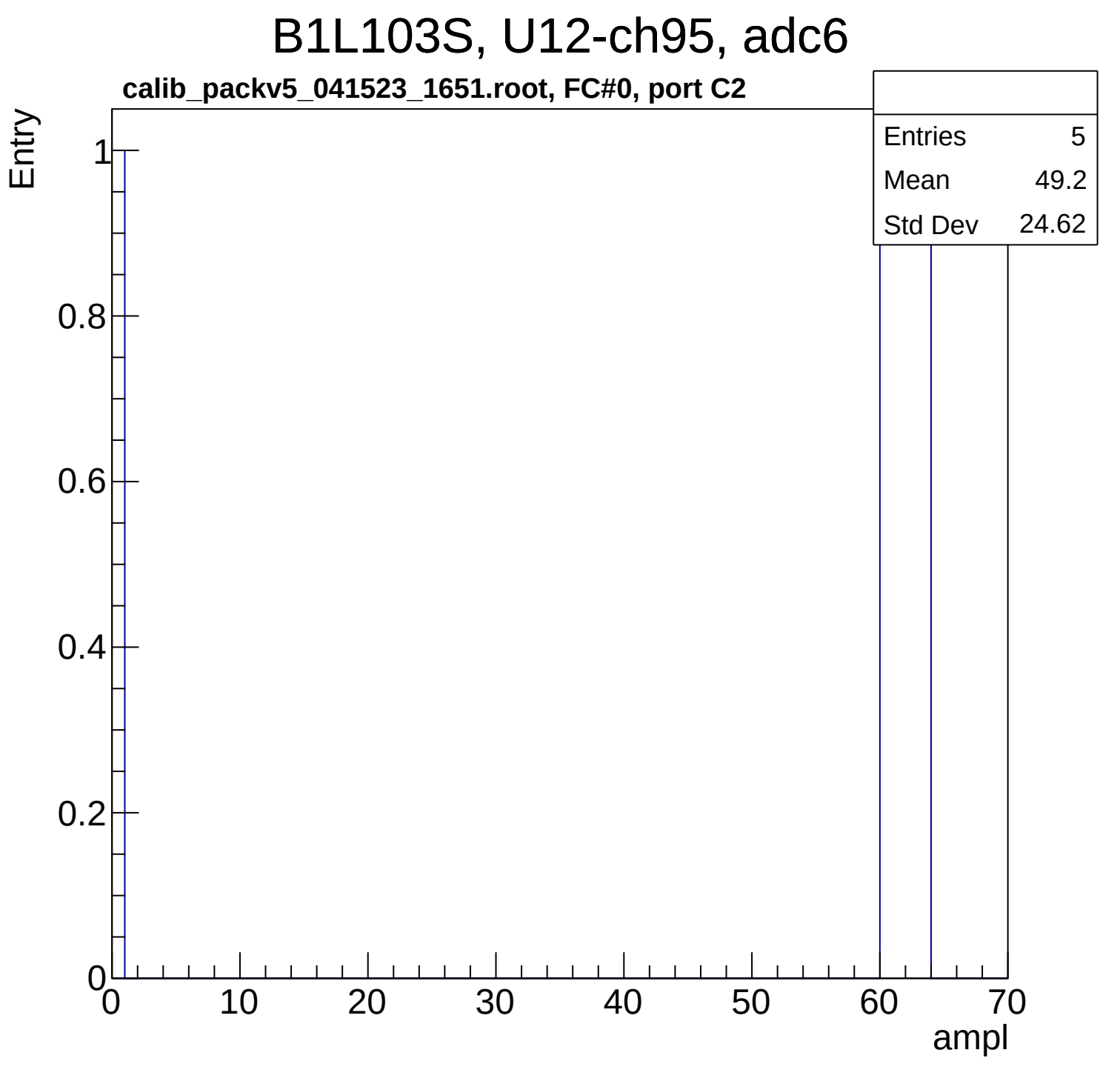
B1L103S, U12-ch95, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 49.2
Std Dev 24.62
Entry
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0.6
0.4
0.2
0
0
10
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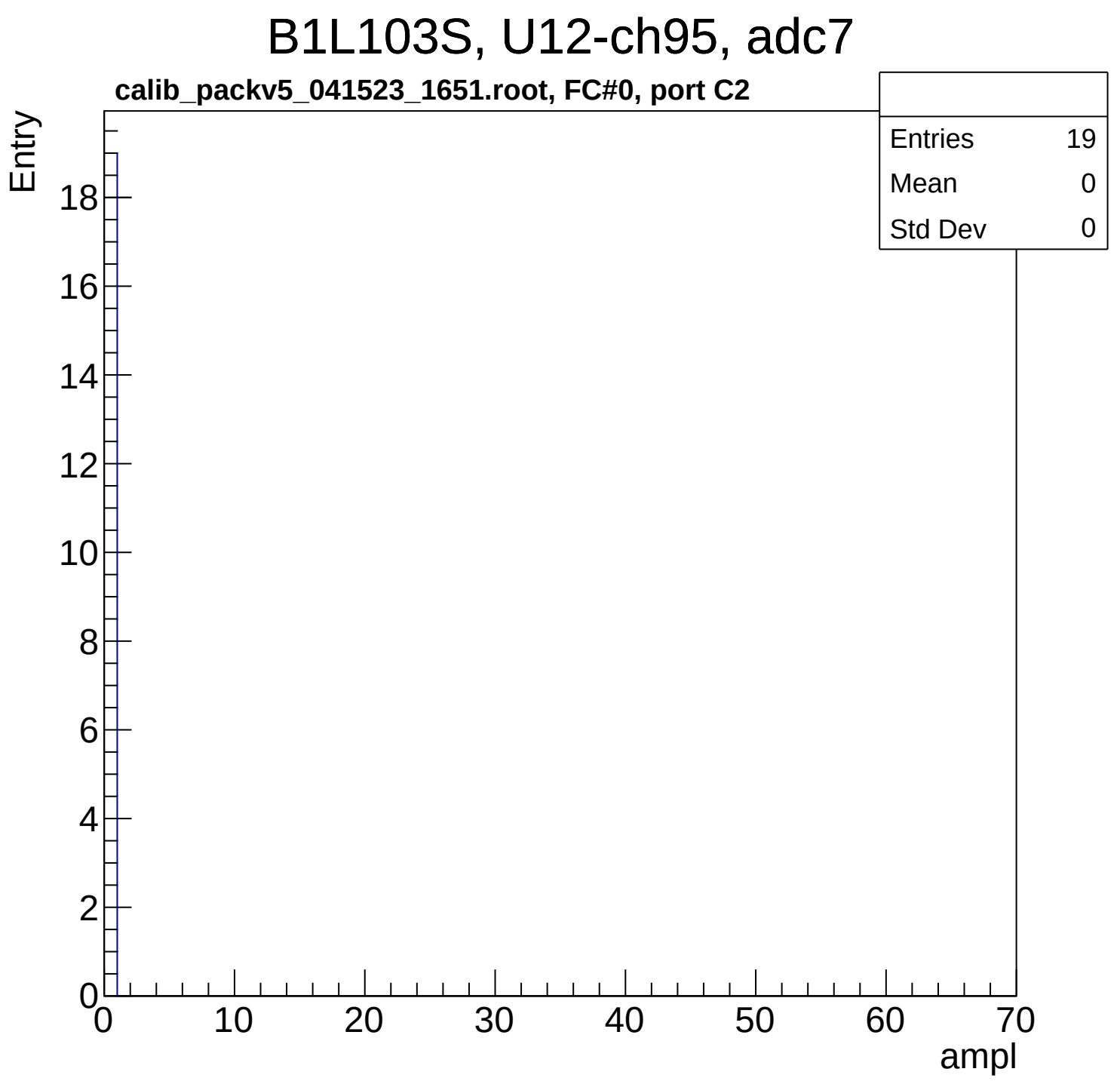
50
60
70
ampl


B1L103S, U12-ch95, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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8
10
12
14
16
18
0
10
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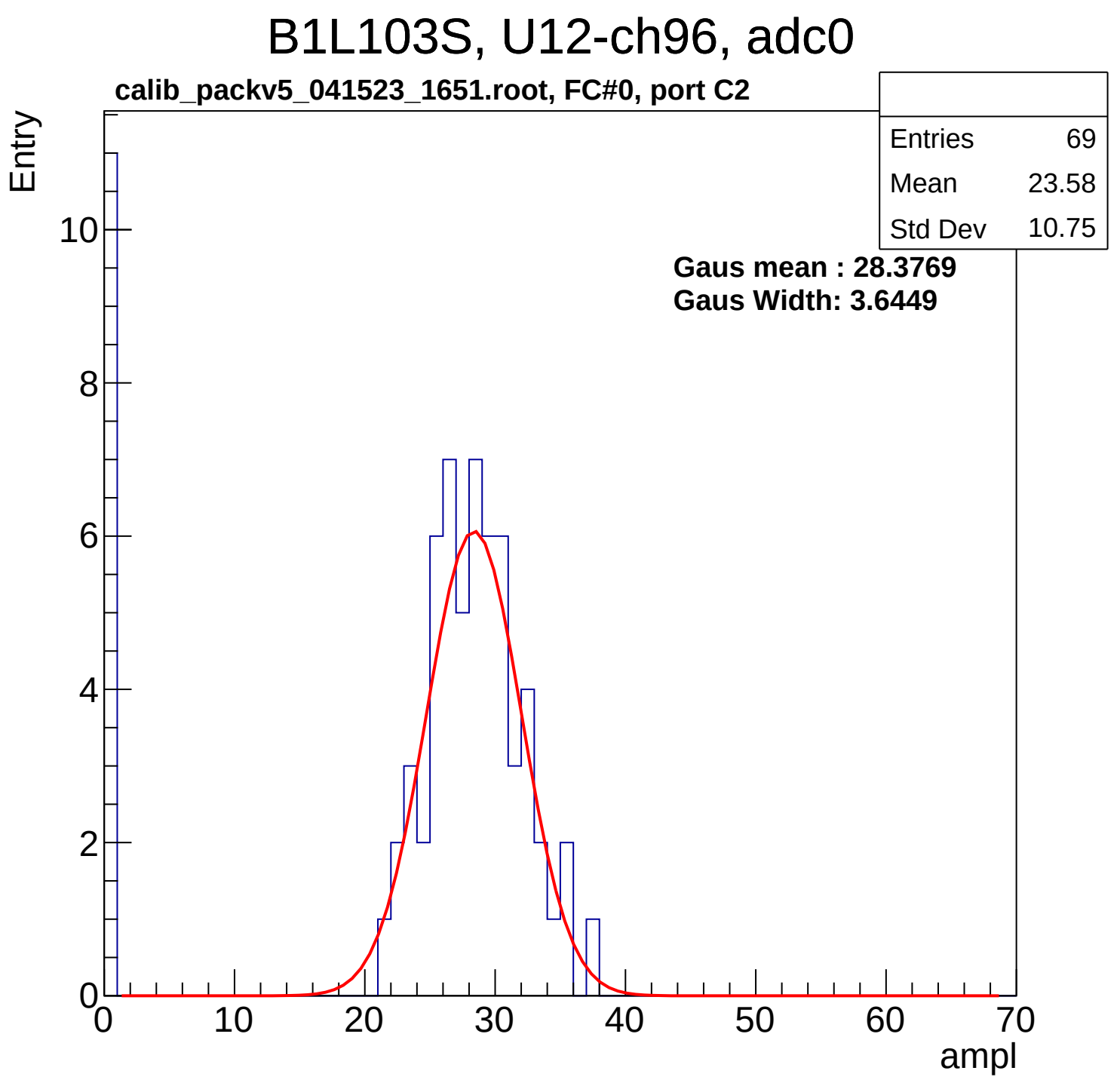
50
60
70
ampl


B1L103S, U12-ch96, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 23.58
Std Dev 10.75
Gaus mean : 28.3769
Gaus Width: 3.6449
Entry
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4
6
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10
0
10
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30
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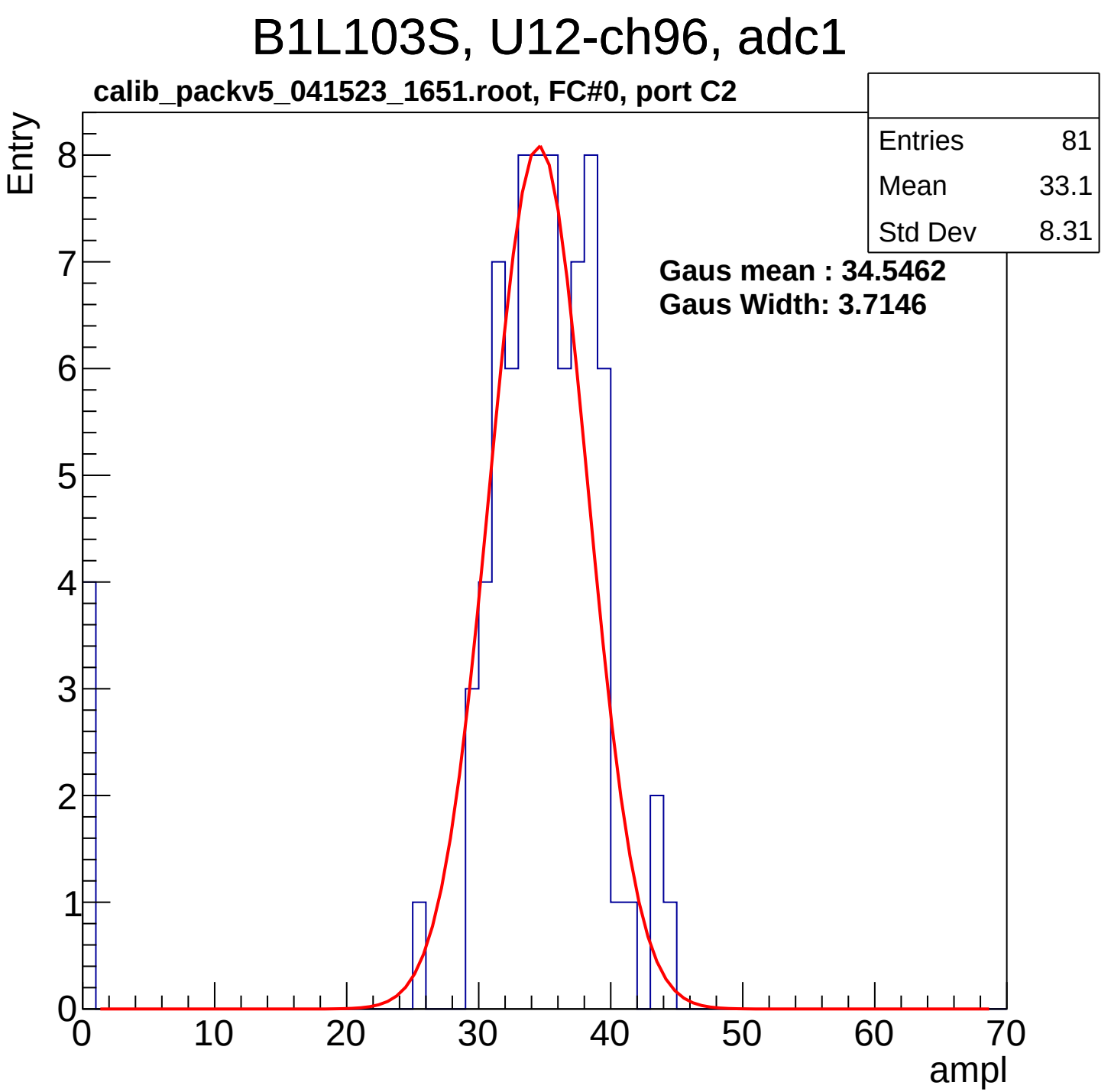
50
60
70
ampl


B1L103S, U12-ch96, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 33.1
Std Dev 8.31
Gaus mean : 34.5462
Gaus Width: 3.7146
Entry
ampl
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2
3
4
5
6
7
8
0
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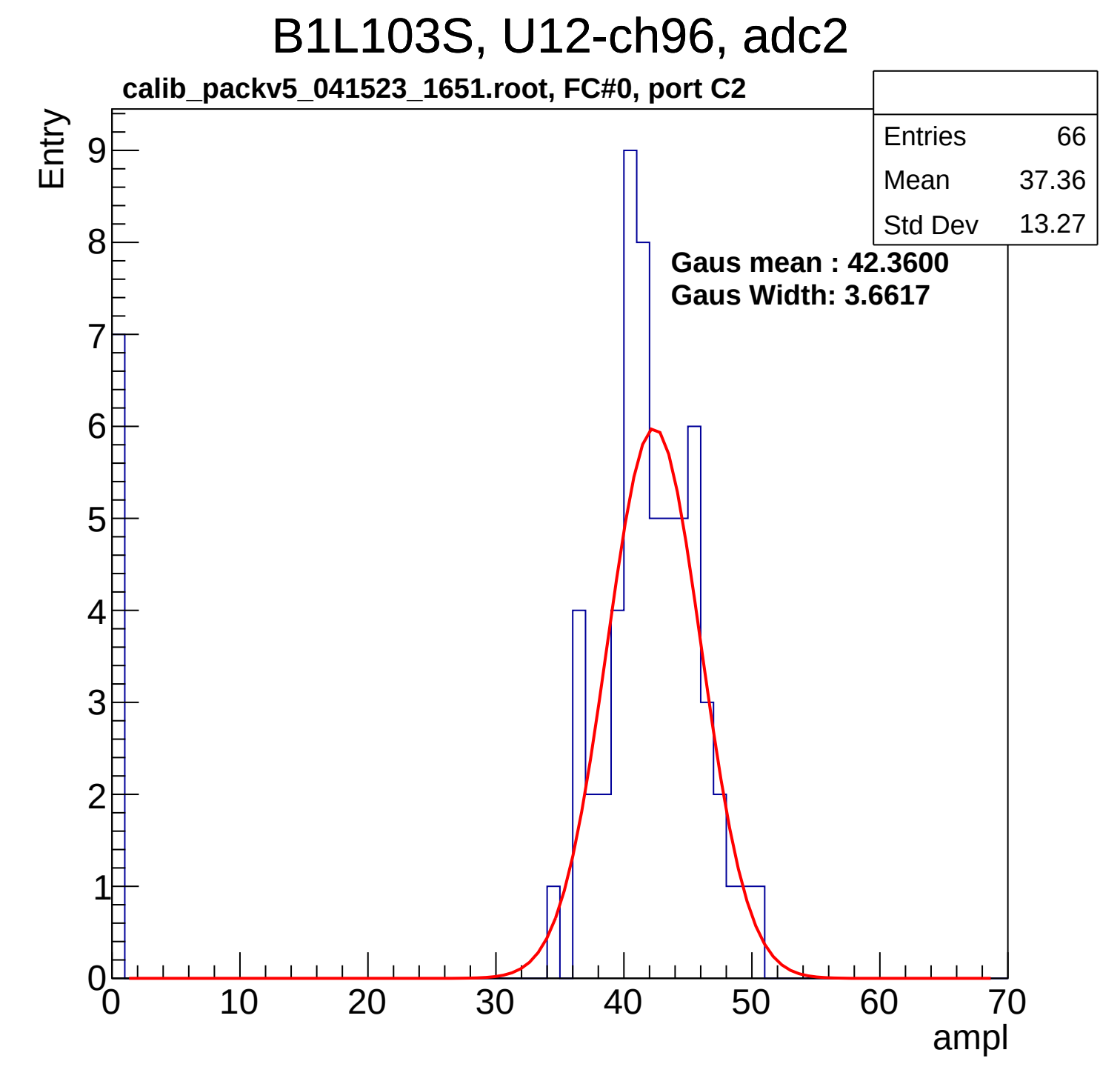
B1L103S, U12-ch96, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 37.36
Std Dev 13.27
Gaus mean : 42.3600
Gaus Width: 3.6617
Entry
ampl
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3
4
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6
7
8
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0
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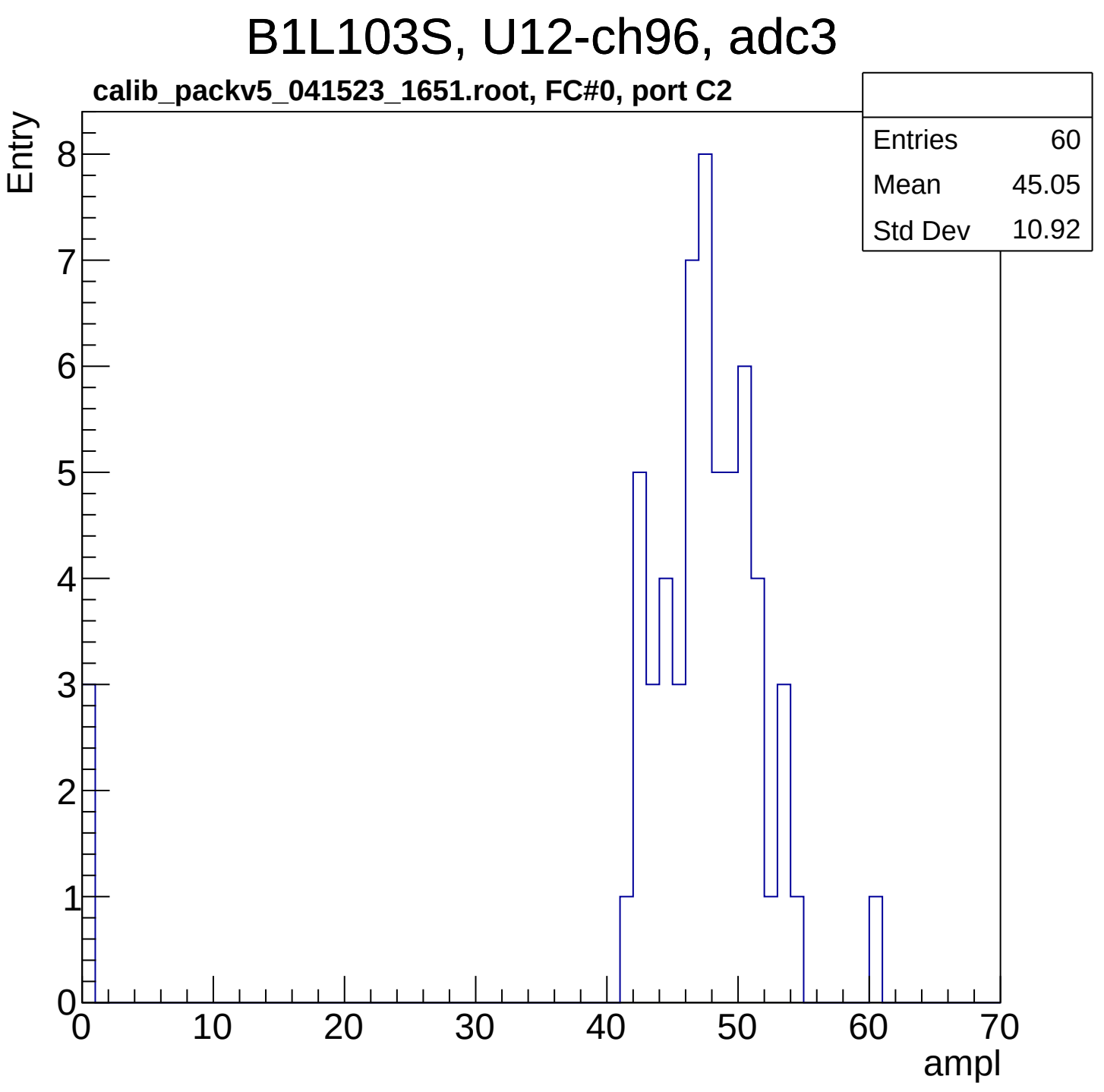
B1L103S, U12-ch96, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 45.05
Std Dev 10.92
Entry
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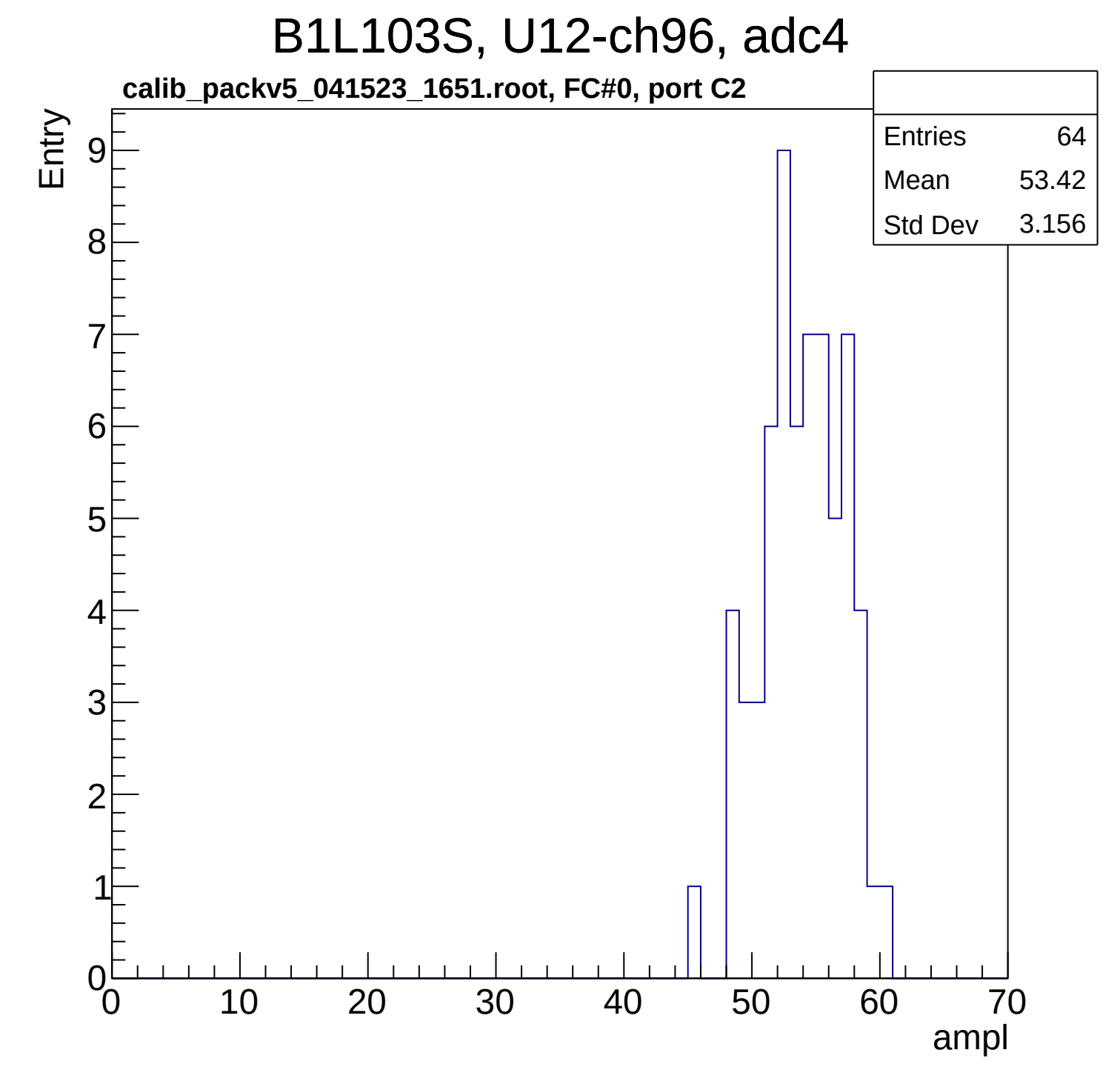
50
60
70
ampl


B1L103S, U12-ch96, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 53.42
Std Dev 3.156
Entry
ampl
0
1
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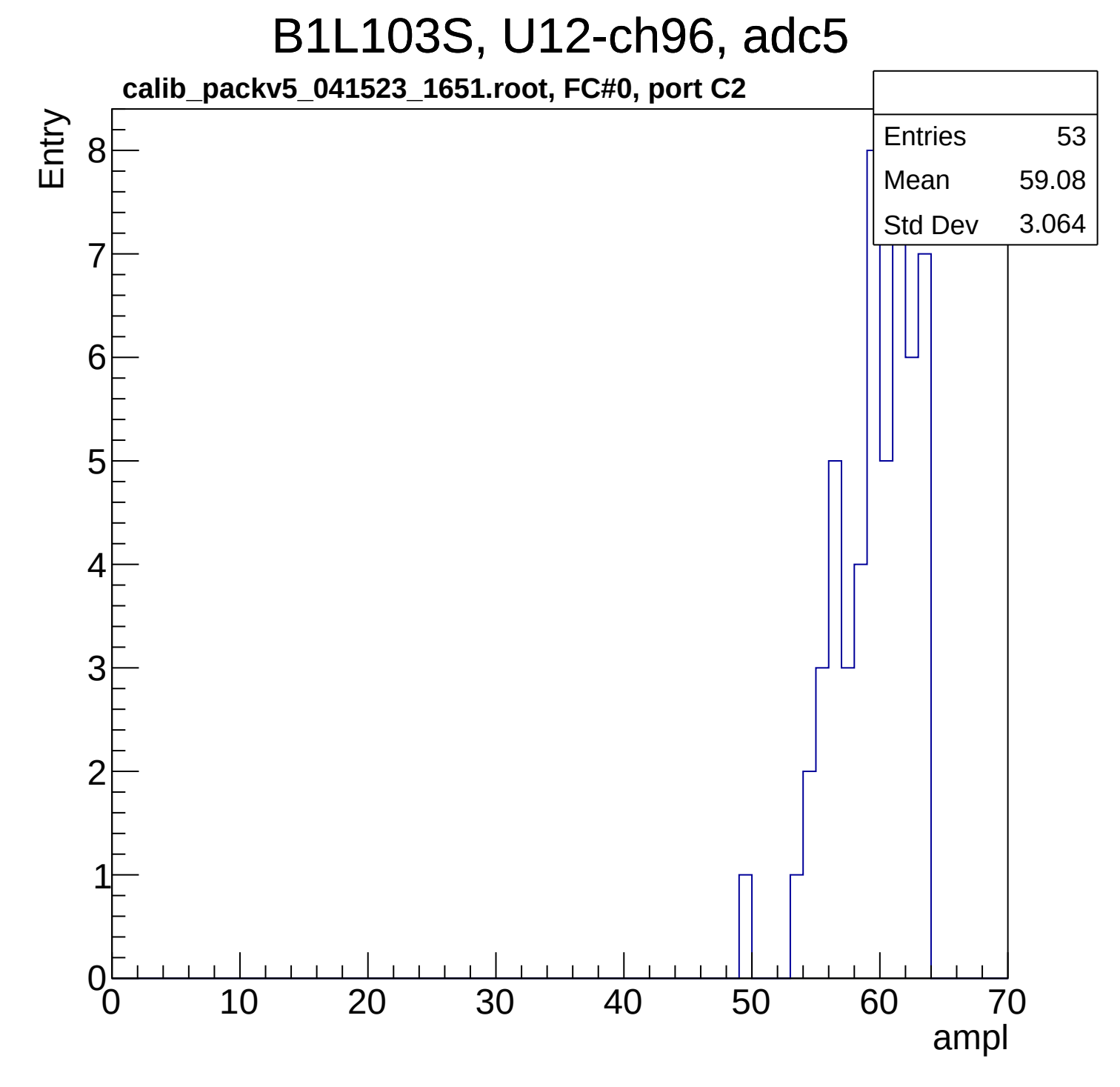
B1L103S, U12-ch96, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 59.08
Std Dev 3.064
Entry
ampl
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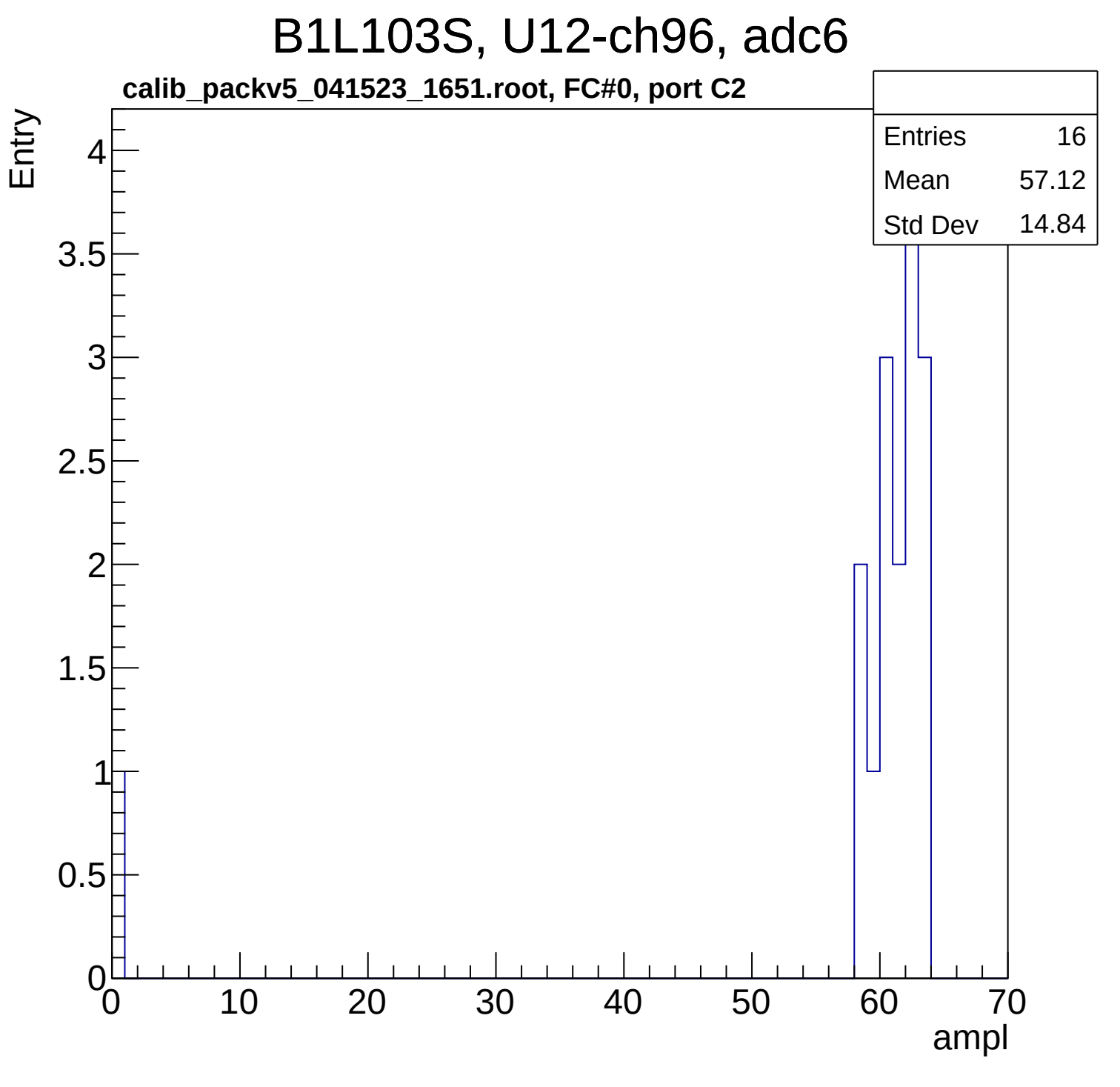
B1L103S, U12-ch96, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 16
Mean 57.12
Std Dev 14.84
Entry
ampl
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0.5
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1.5
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2.5
3
3.5
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0
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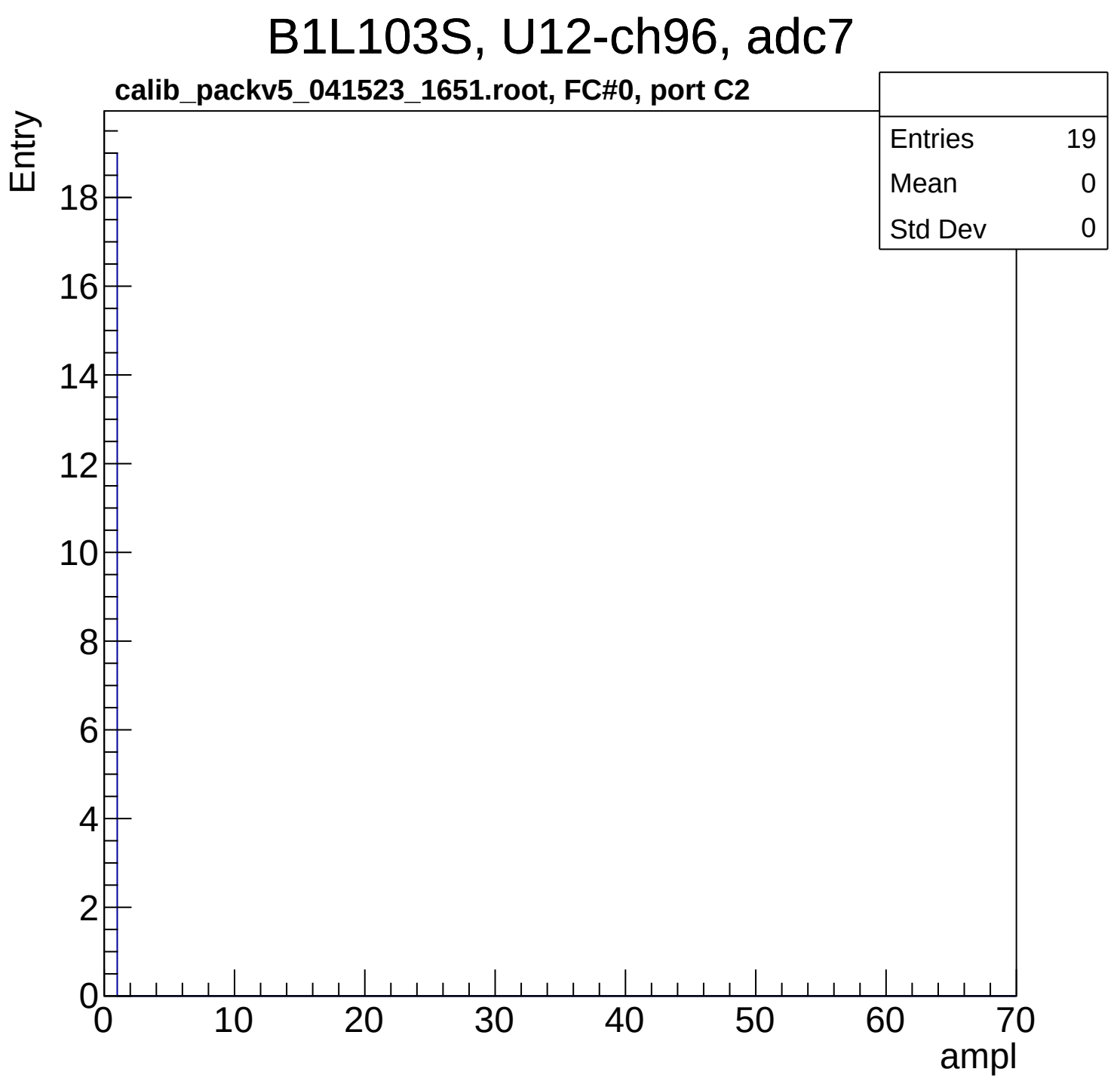
B1L103S, U12-ch96, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
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6
8
10
12
14
16
18
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10
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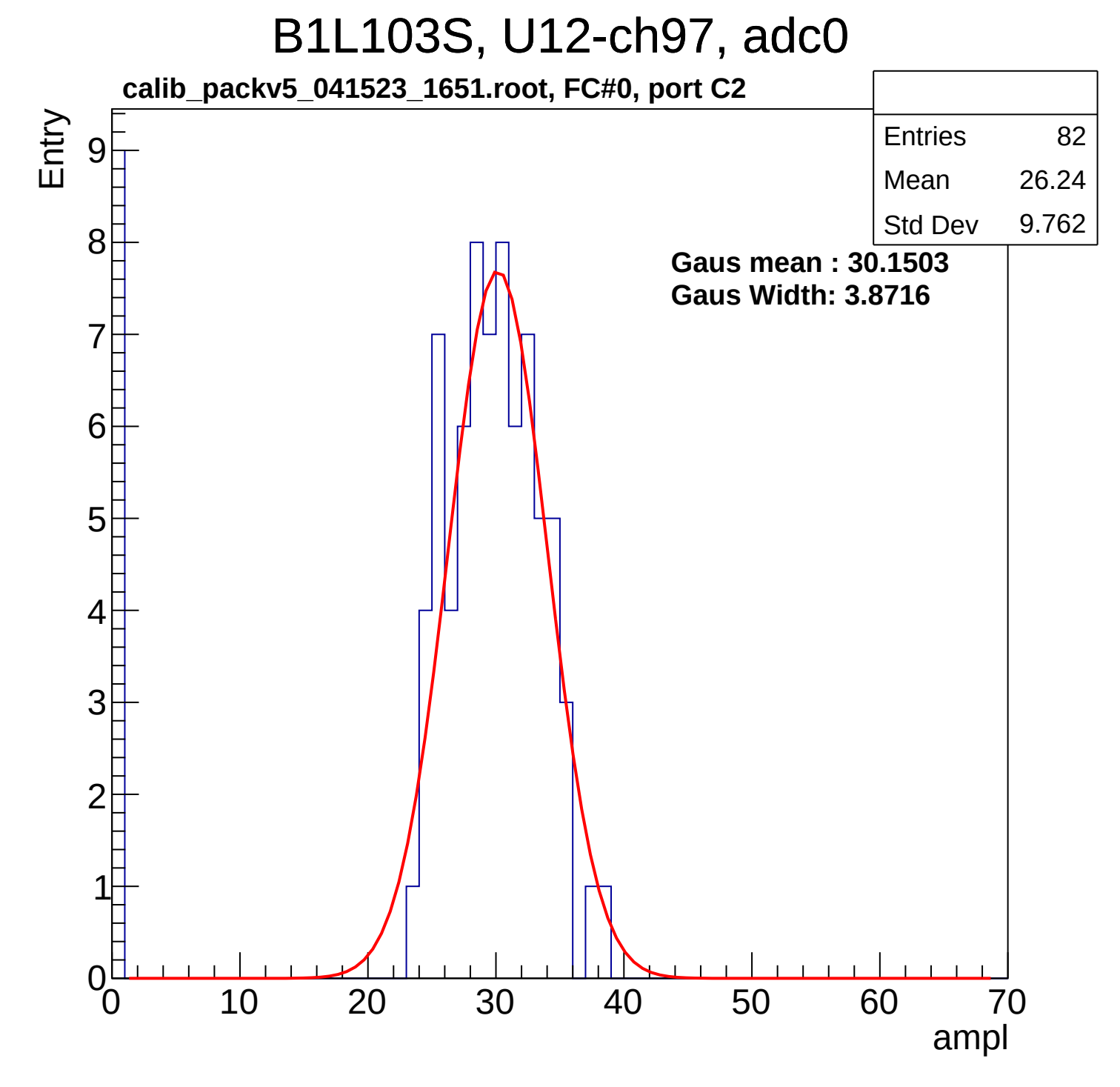
50
60
70
ampl


B1L103S, U12-ch97, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 26.24
Std Dev 9.762
Gaus mean : 30.1503
Gaus Width: 3.8716
Entry
ampl
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1
2
3
4
5
6
7
8
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0
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40
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60
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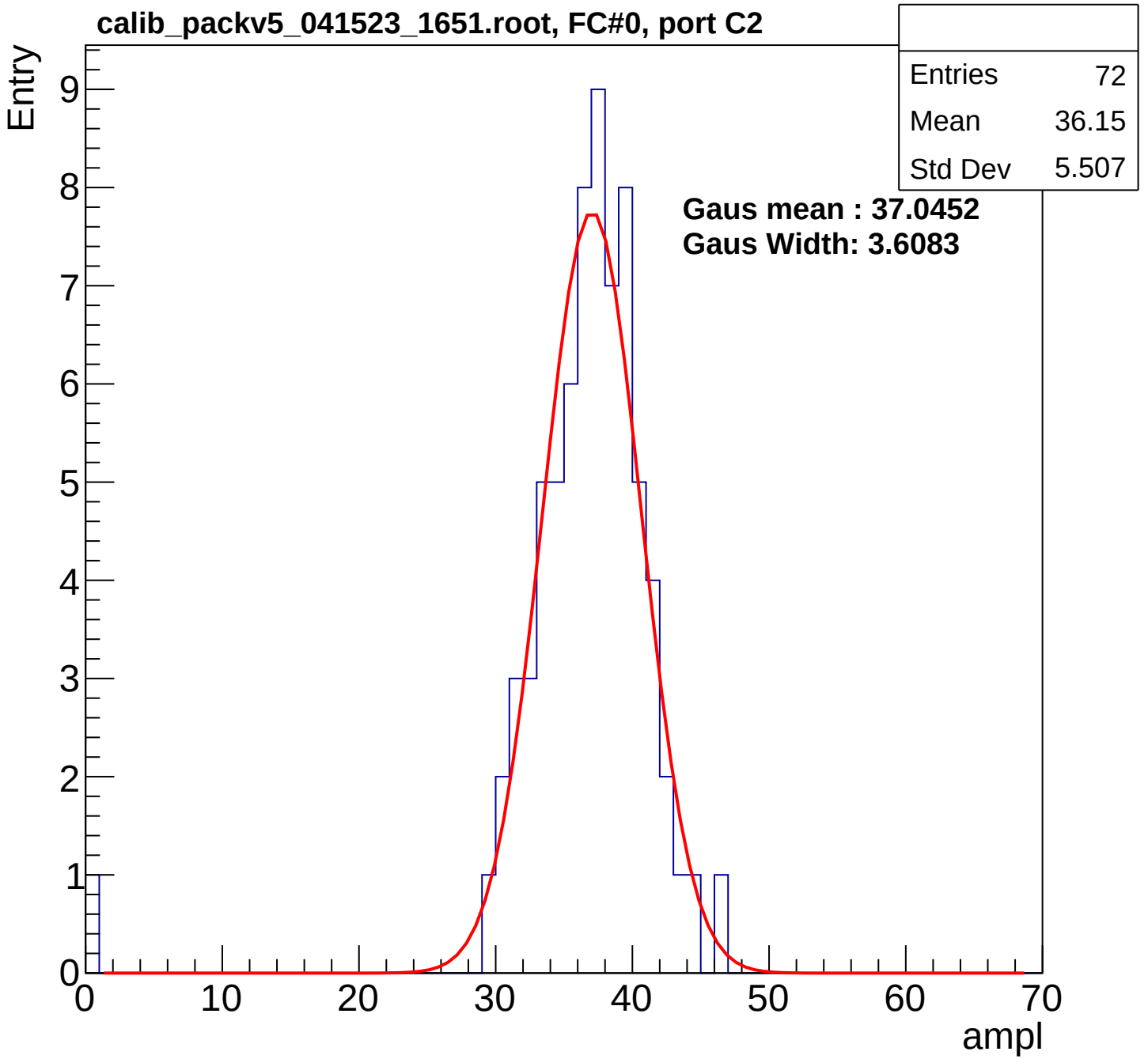
B1L103S, U12-ch97, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 36.15
Std Dev 5.507
Gaus mean : 37.0452
Gaus Width: 3.6083
Entry
ampl
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2
3
4
5
6
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8
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0
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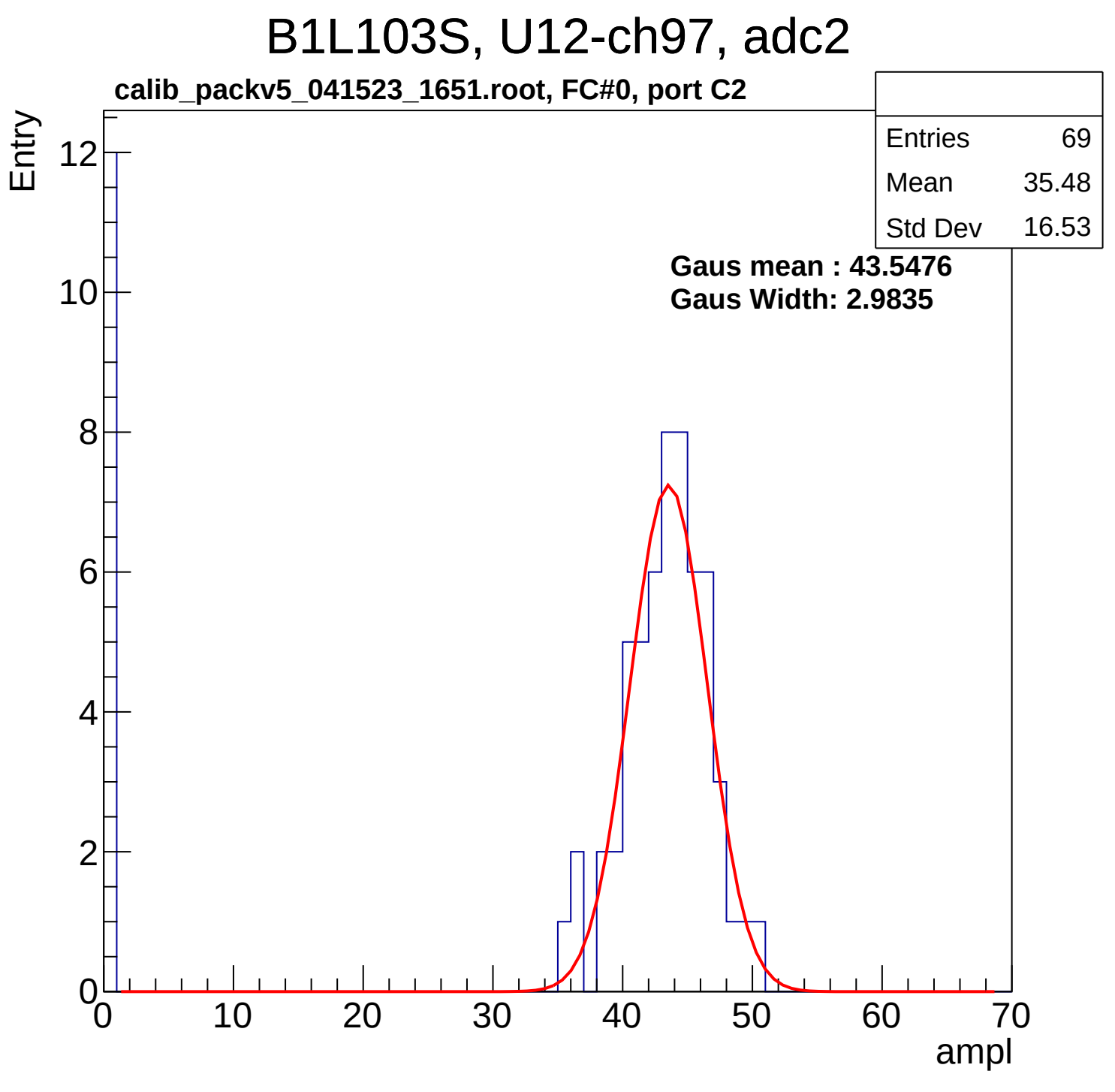
B1L103S, U12-ch97, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 35.48
Std Dev 16.53
Gaus mean : 43.5476
Gaus Width: 2.9835
Entry
ampl
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2
4
6
8
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0
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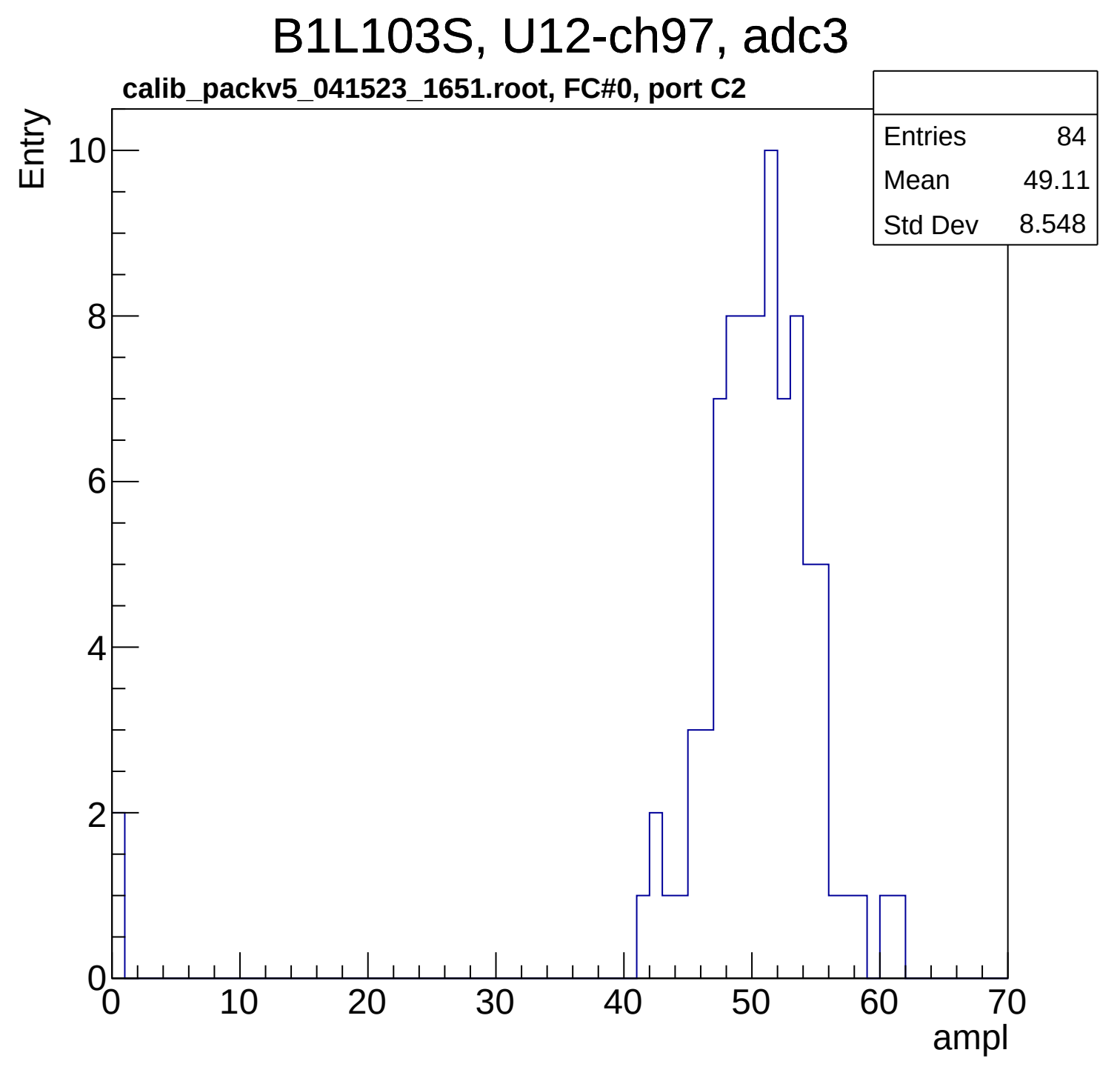
B1L103S, U12-ch97, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 49.11
Std Dev 8.548
Entry
ampl
0
2
4
6
8
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0
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40
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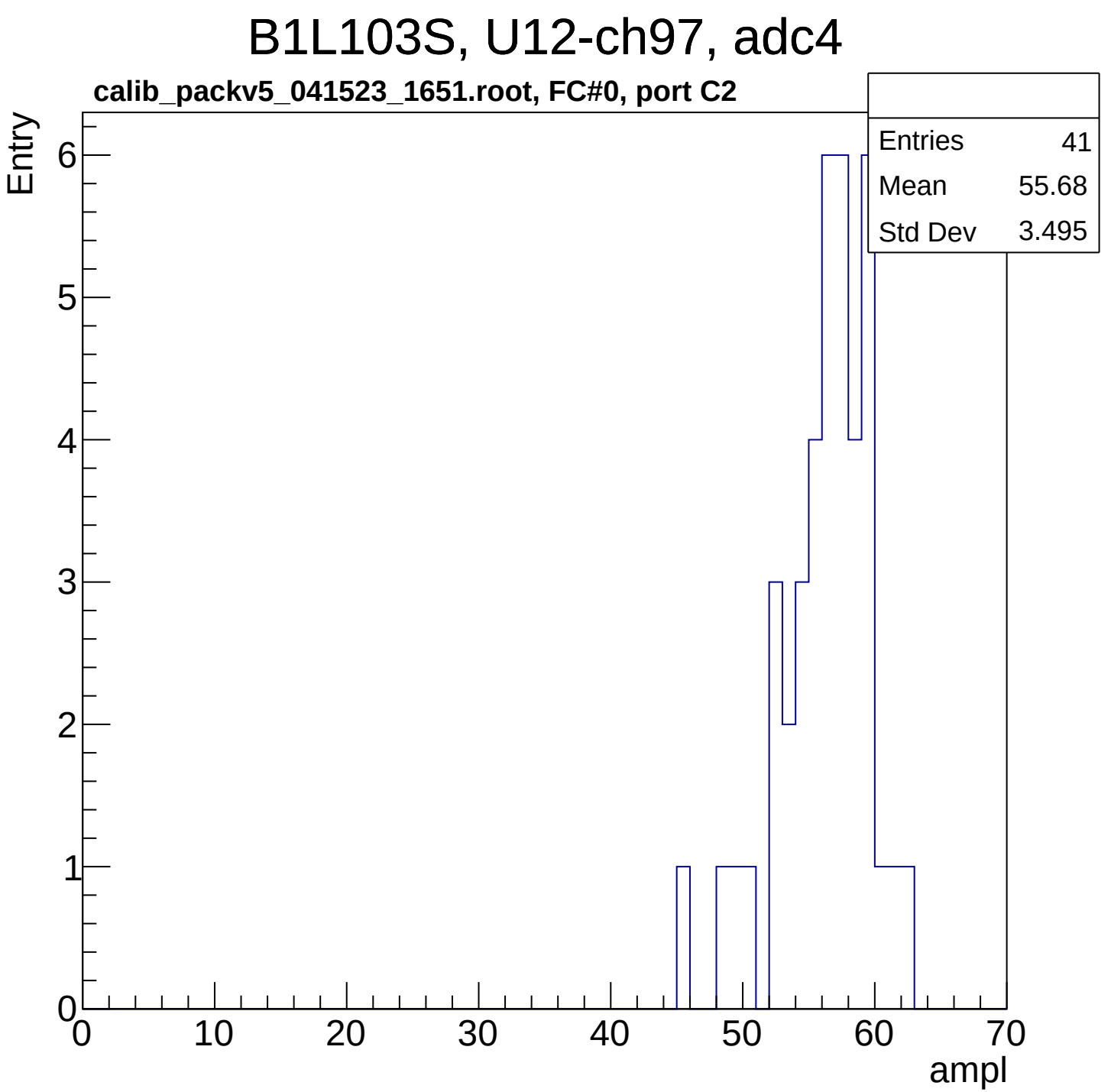
B1L103S, U12-ch97, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 55.68
Std Dev 3.495
Entry
0
1
2
3
4
5
6
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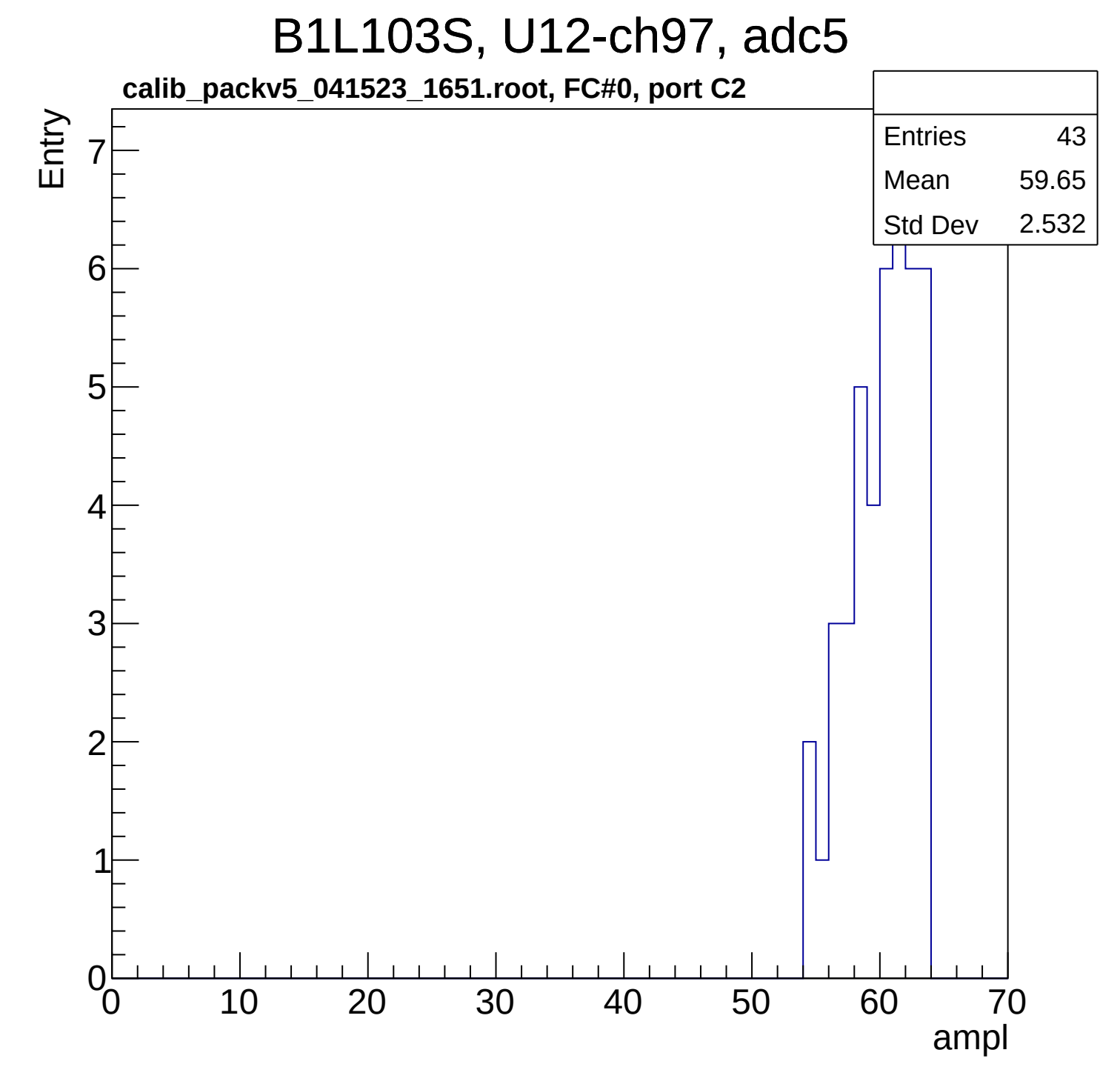
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch97, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 59.65
Std Dev 2.532
Entry
ampl
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1
2
3
4
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6
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0
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60
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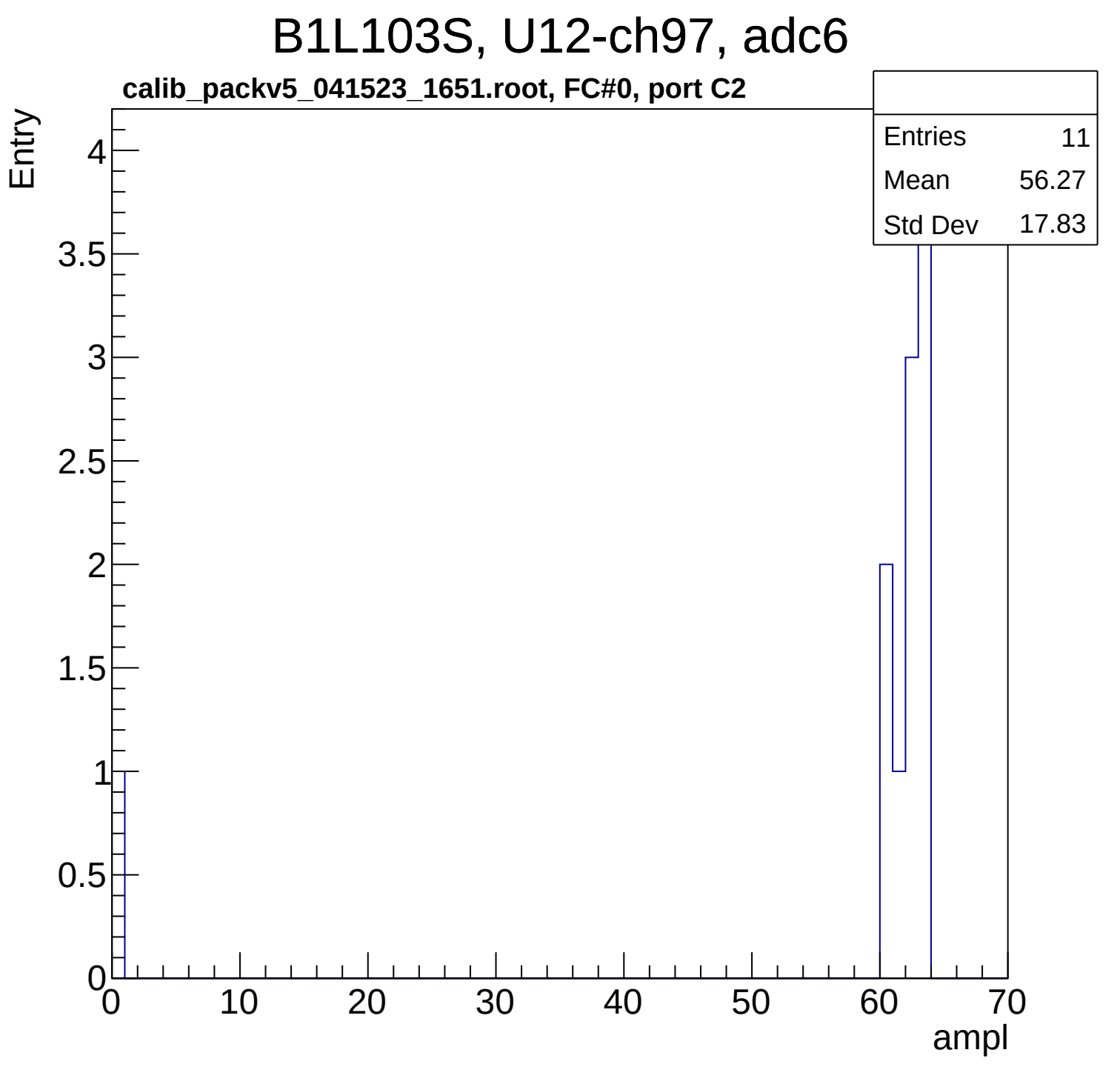
B1L103S, U12-ch97, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 56.27
Std Dev 17.83
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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40
50
60
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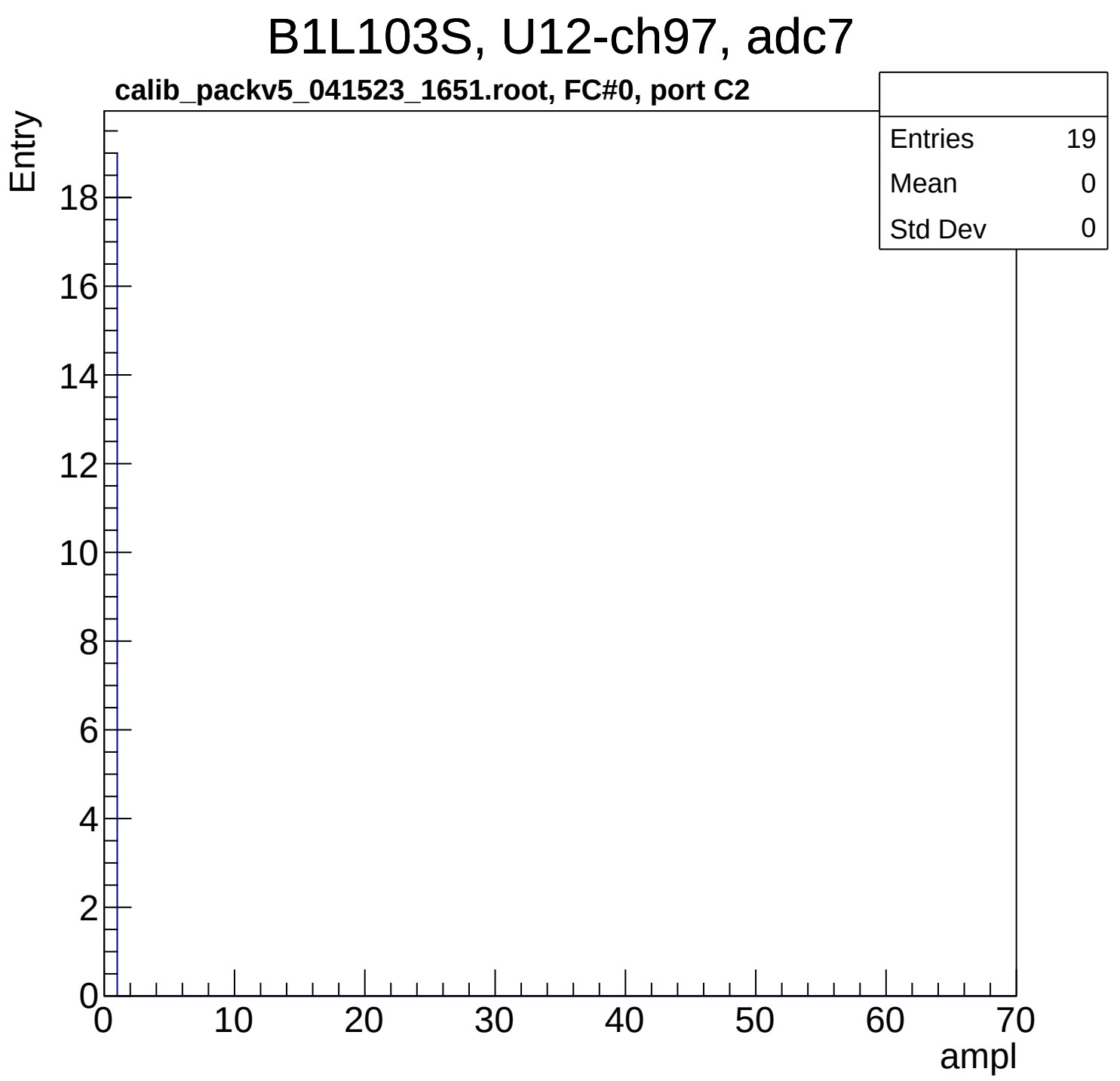
B1L103S, U12-ch97, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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2
4
6
8
10
12
14
16
18
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10
20
30
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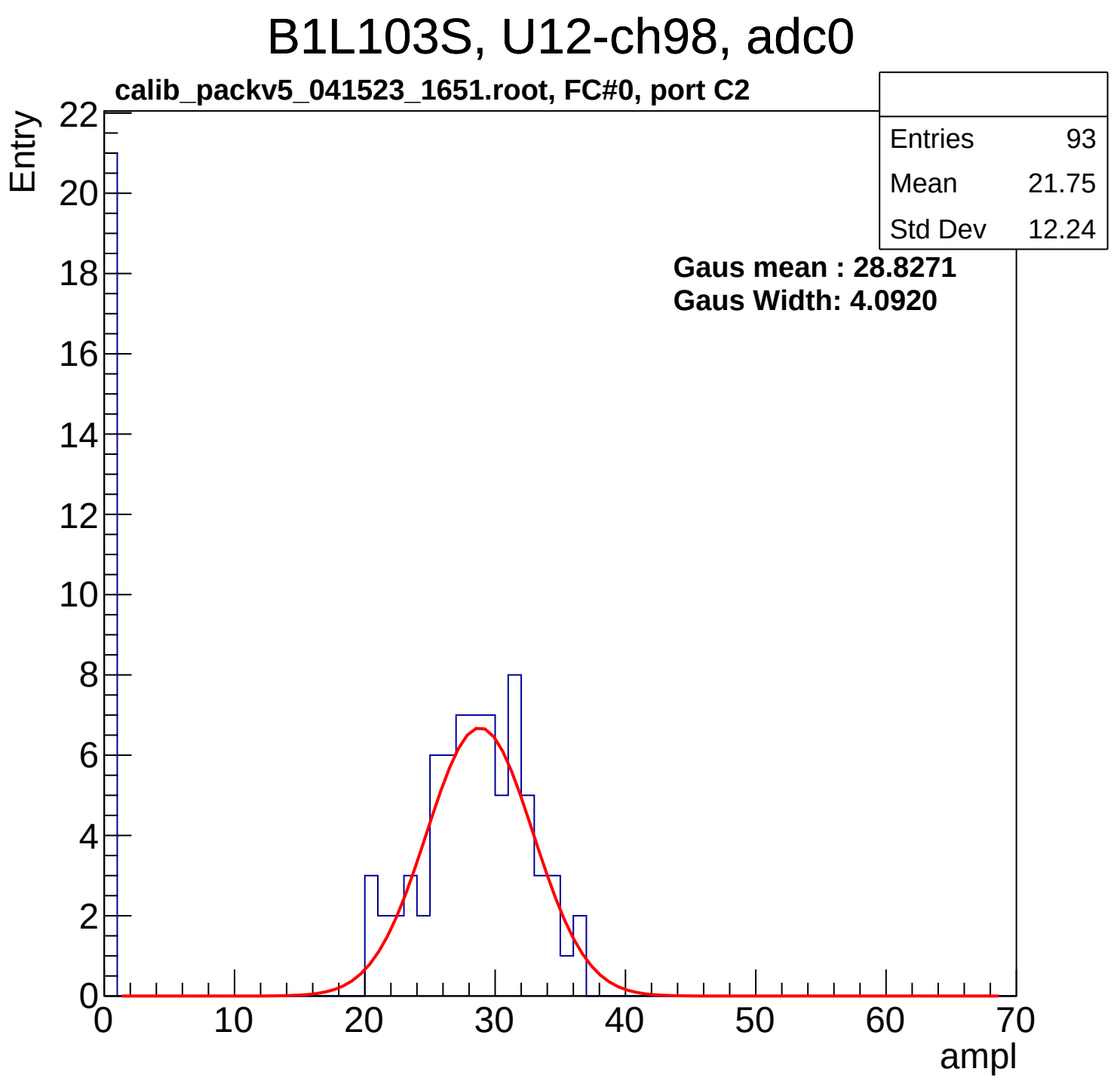
50
60
70
ampl


B1L103S, U12-ch98, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 93
Mean 21.75
Std Dev 12.24
Gaus mean : 28.8271
Gaus Width: 4.0920
Entry
ampl
0
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4
6
8
10
12
14
16
18
20
22
0
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40
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60
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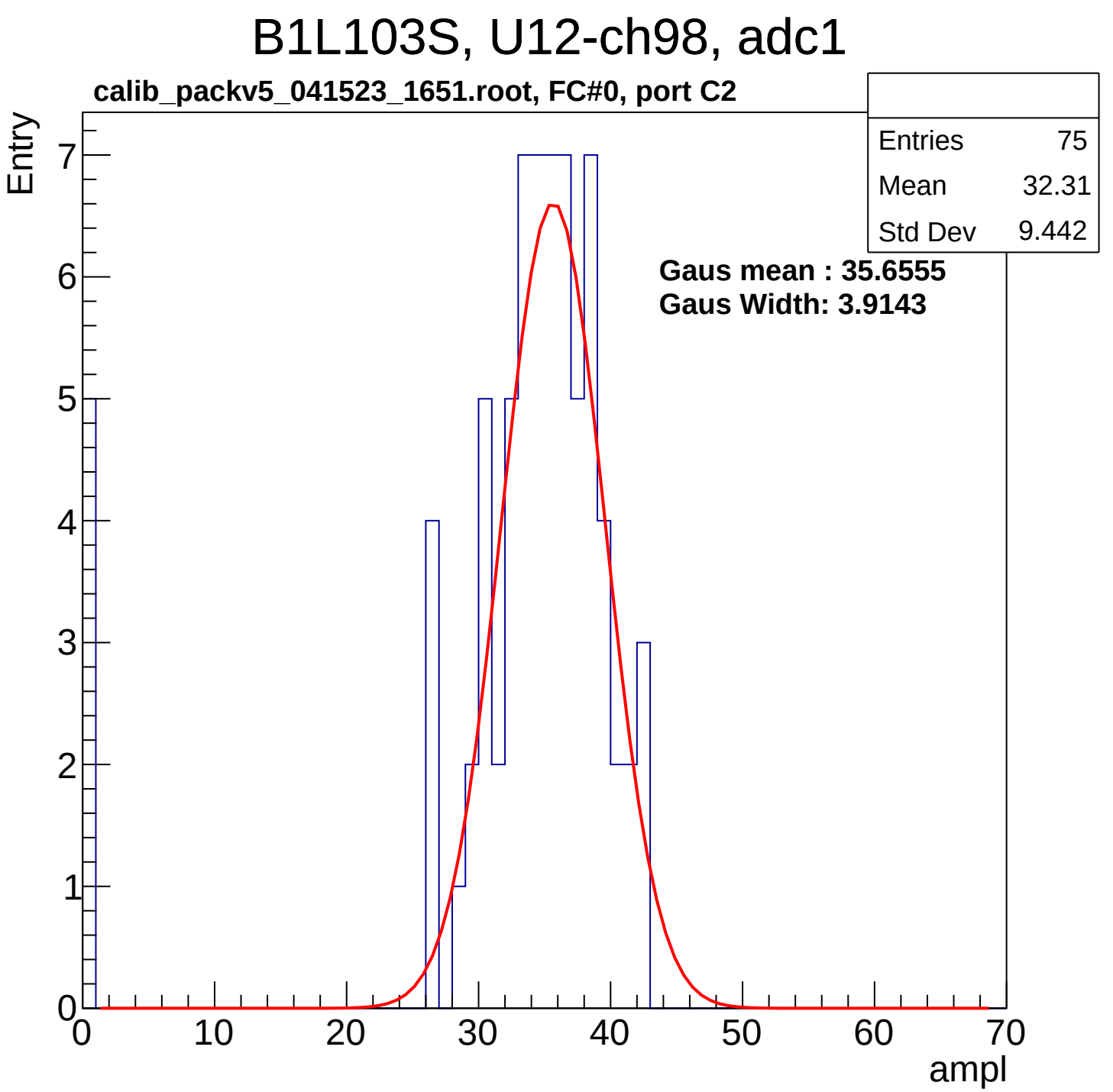
B1L103S, U12-ch98, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 32.31
Std Dev 9.442
Gaus mean : 35.6555
Gaus Width: 3.9143
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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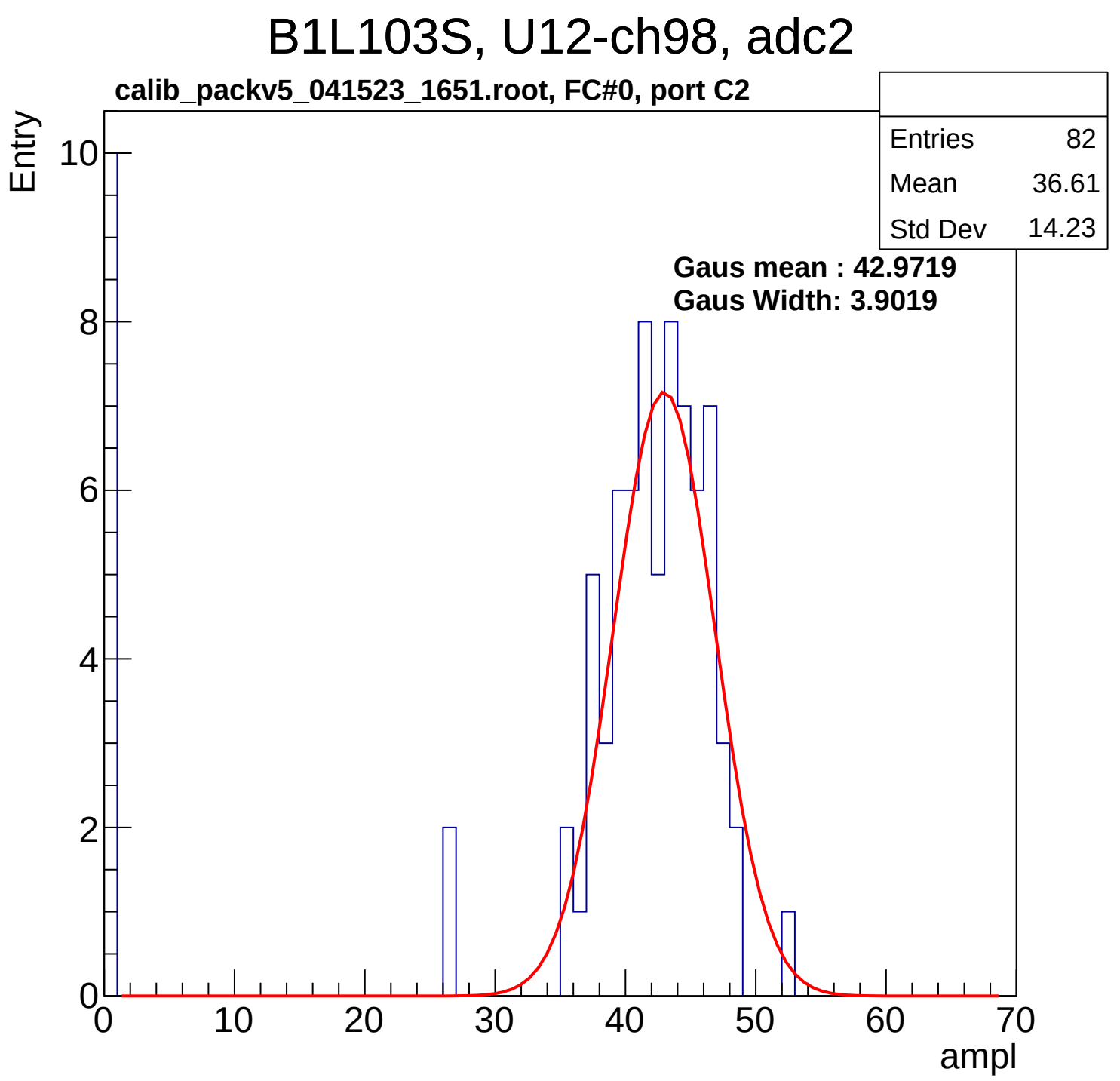
B1L103S, U12-ch98, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 36.61
Std Dev 14.23
Gaus mean : 42.9719
Gaus Width: 3.9019
Entry
ampl
0
2
4
6
8
10
0
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60
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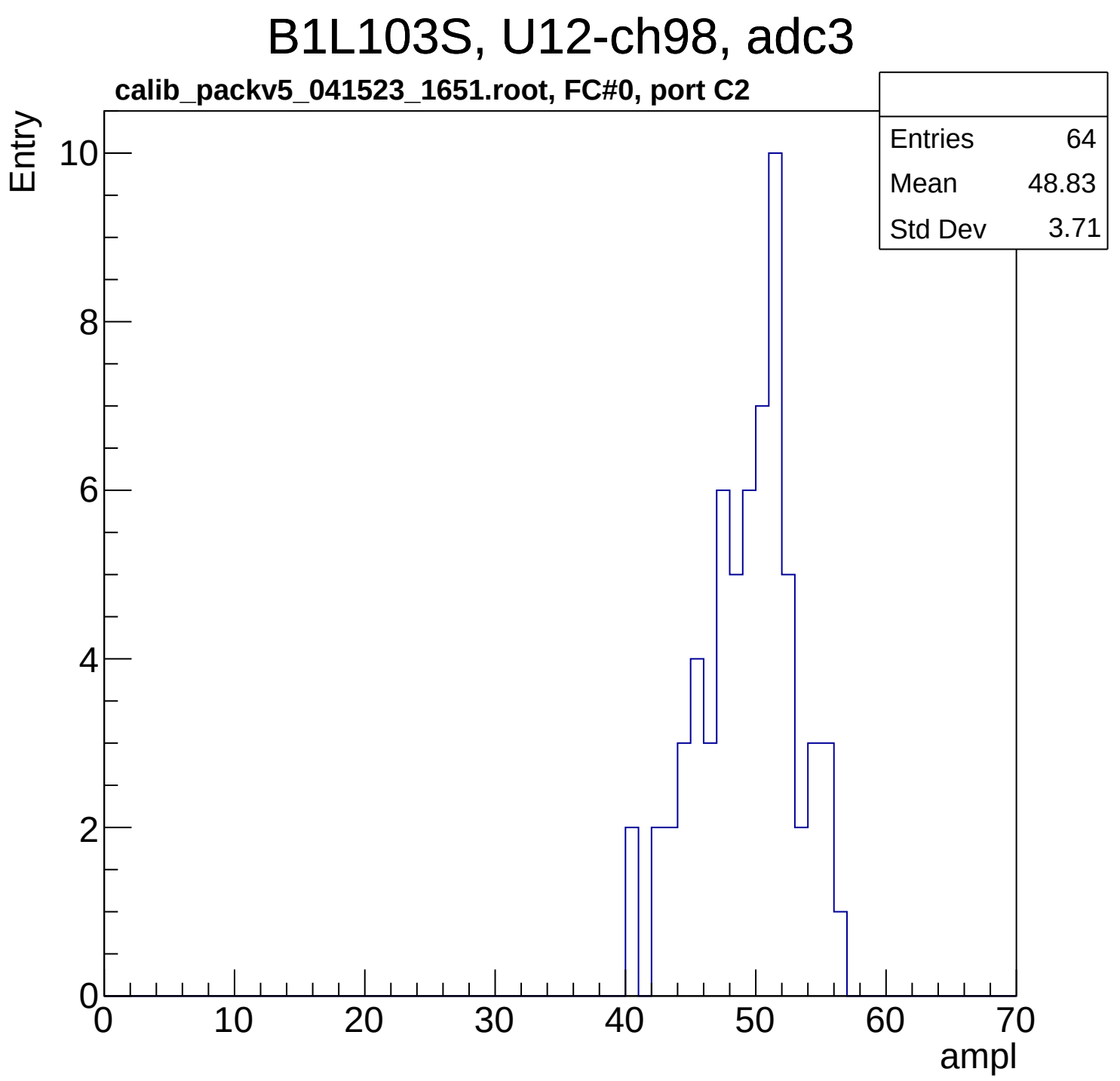
B1L103S, U12-ch98, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 48.83
Std Dev 3.71
Entry
ampl
0
2
4
6
8
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0
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20
30
40
50
60
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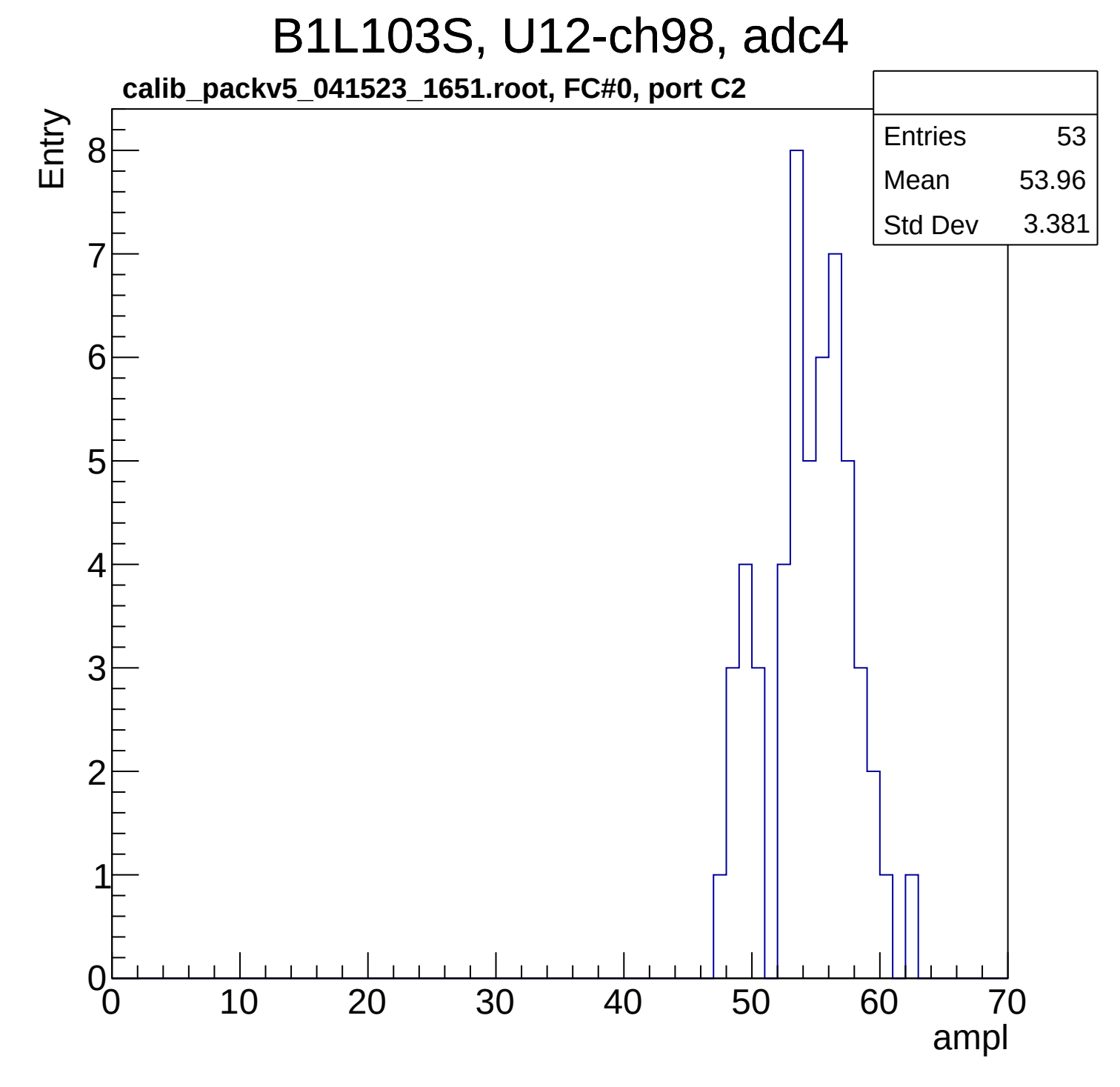
B1L103S, U12-ch98, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 53
Mean 53.96
Std Dev 3.381
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
30
40
50
60
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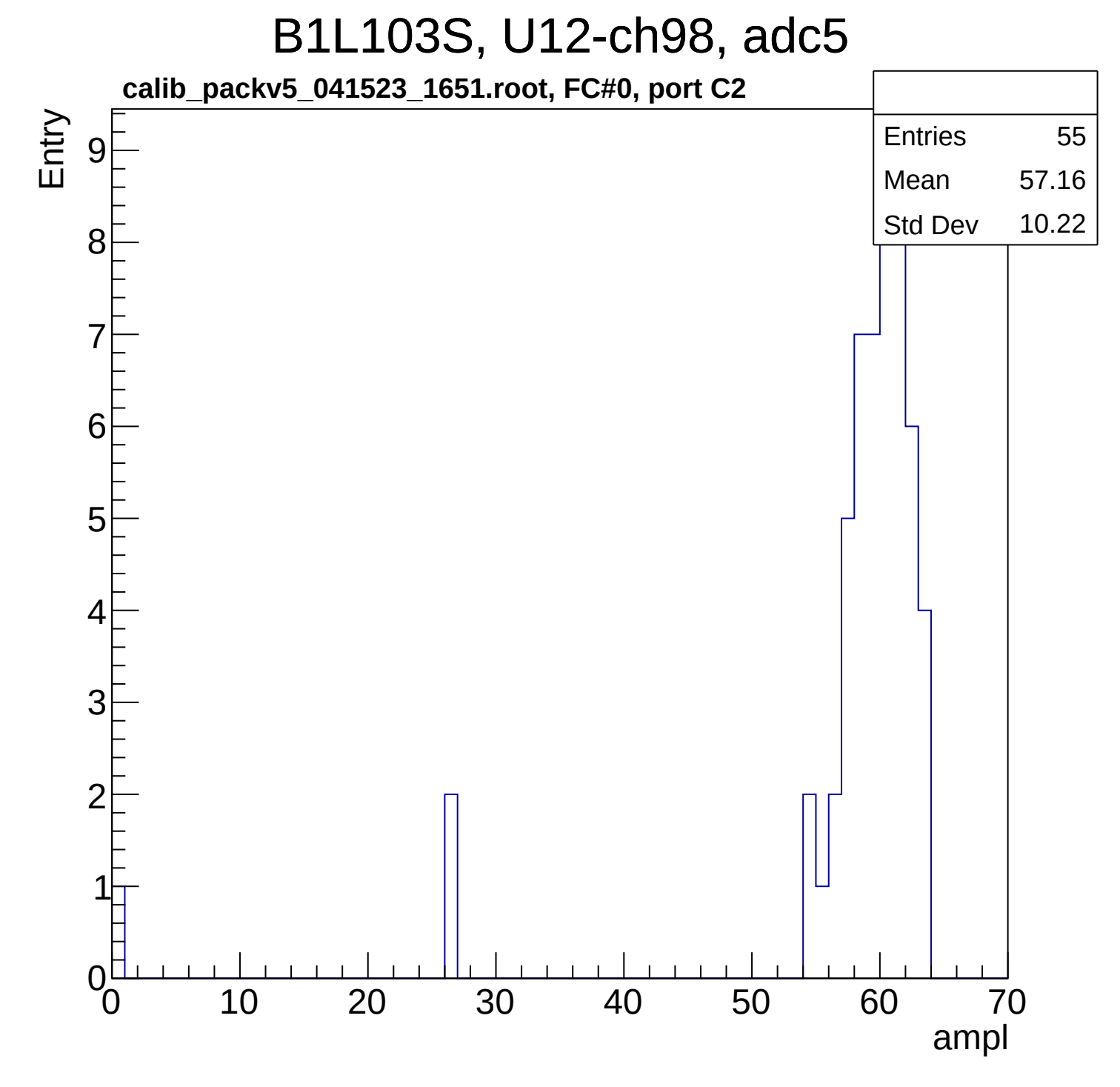
B1L103S, U12-ch98, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.16
Std Dev 10.22
Entry
ampl
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3
4
5
6
7
8
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0
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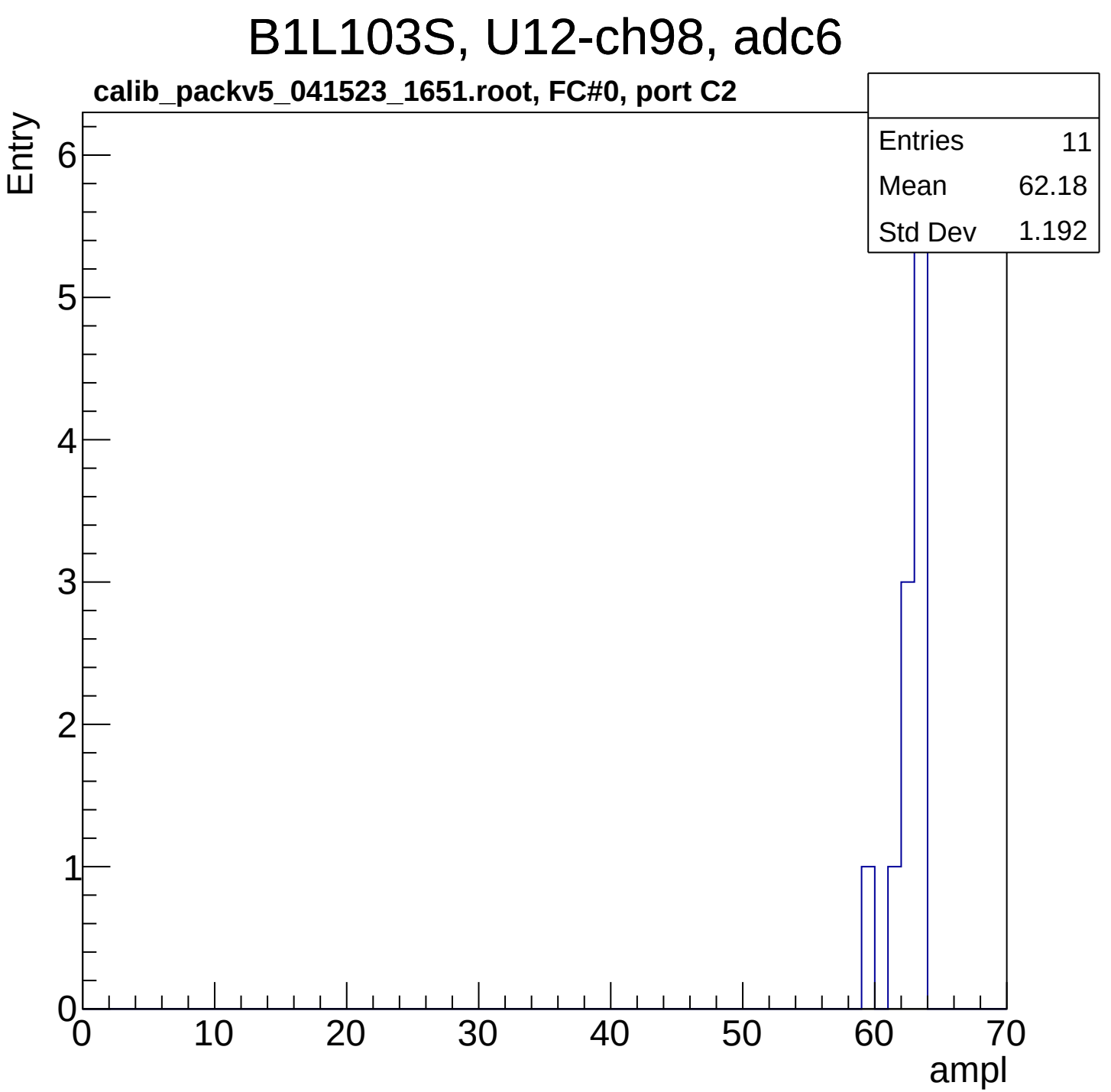
B1L103S, U12-ch98, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 11
Mean 62.18
Std Dev 1.192
Entry
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3
4
5
6
0
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20
30
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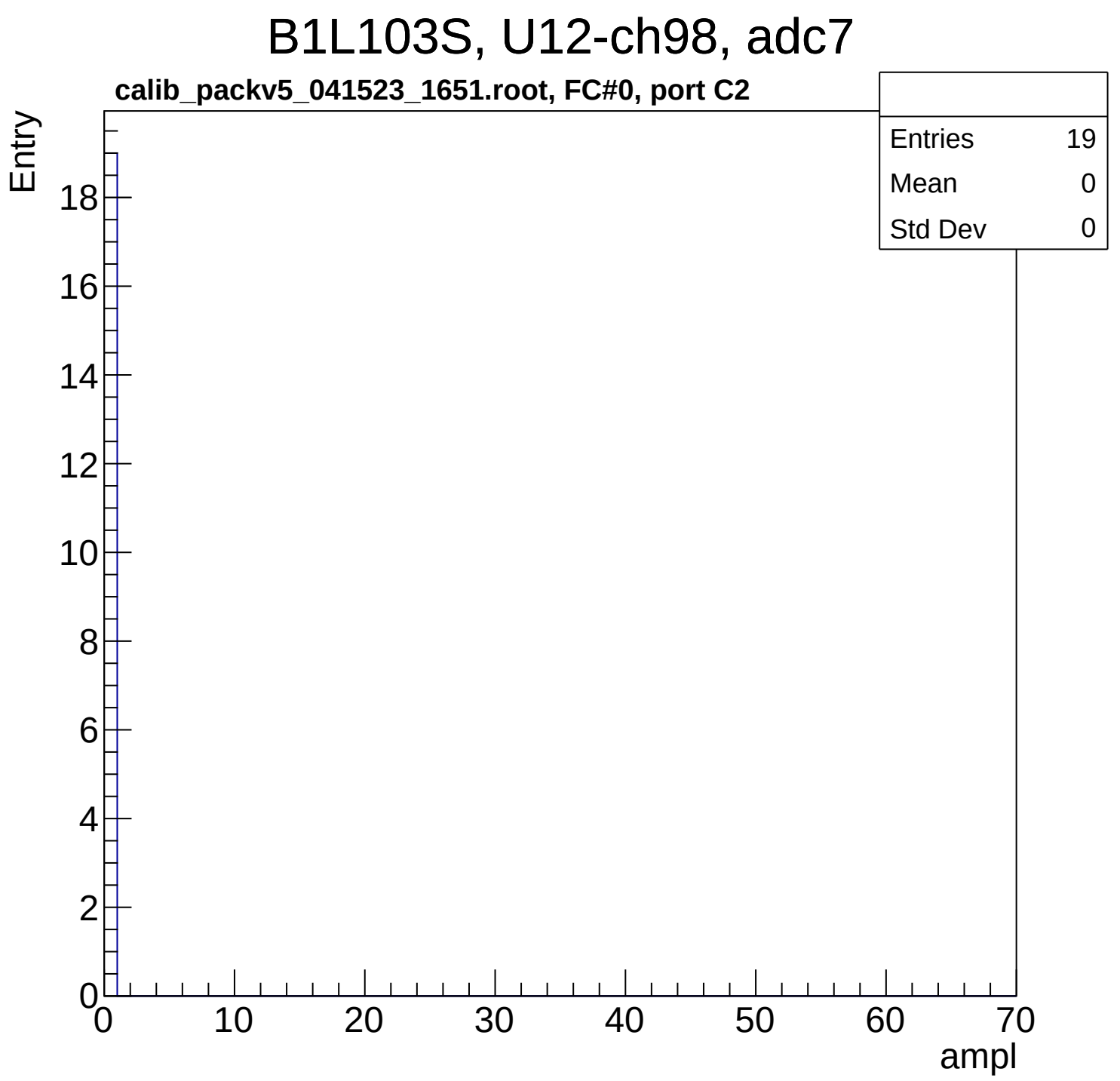
50
60
70
ampl


B1L103S, U12-ch98, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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6
8
10
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14
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18
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20
30
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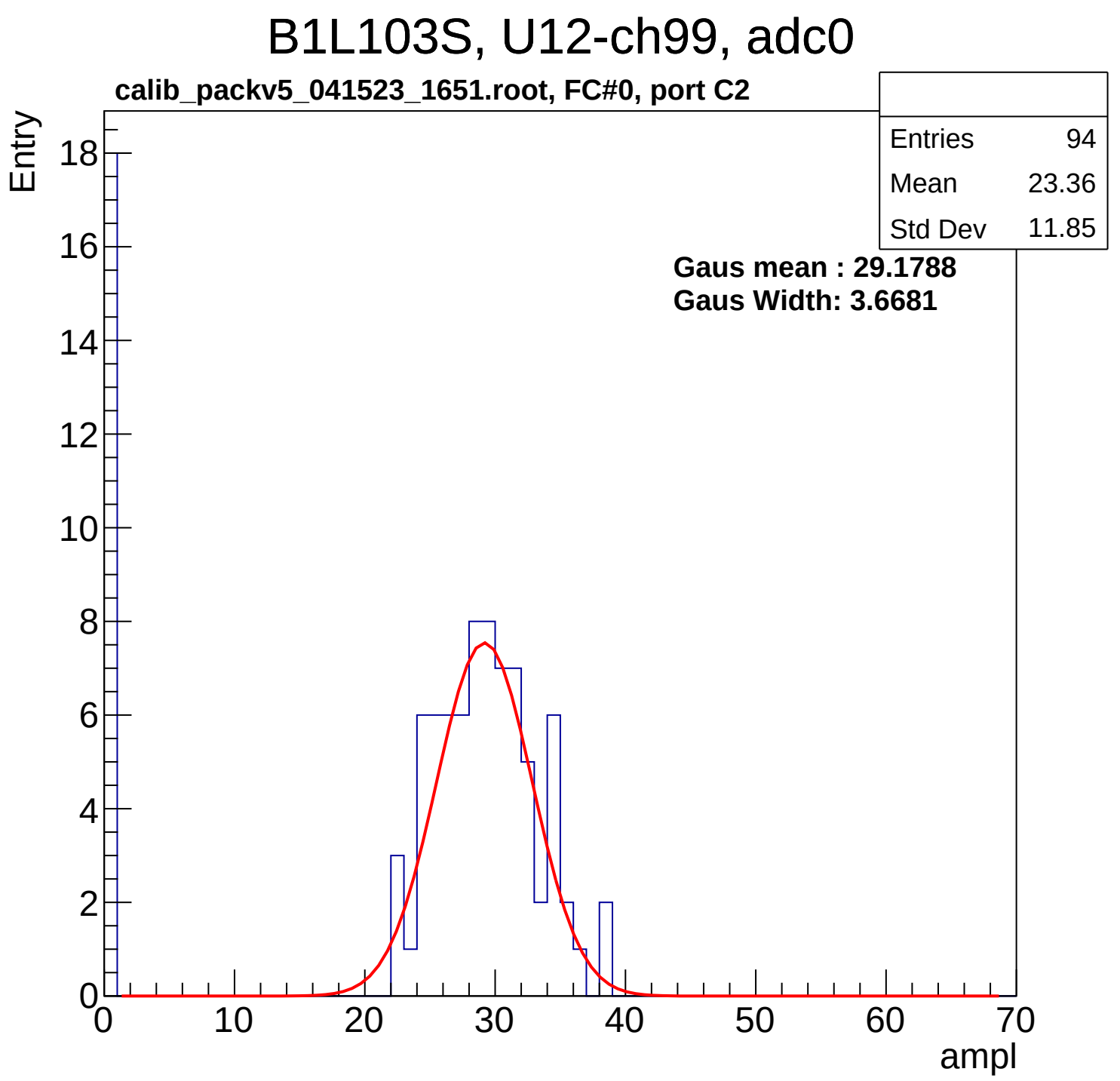
50
60
70
ampl


B1L103S, U12-ch99, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 23.36
Std Dev 11.85
Gaus mean : 29.1788
Gaus Width: 3.6681
Entry
ampl
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4
6
8
10
12
14
16
18
0
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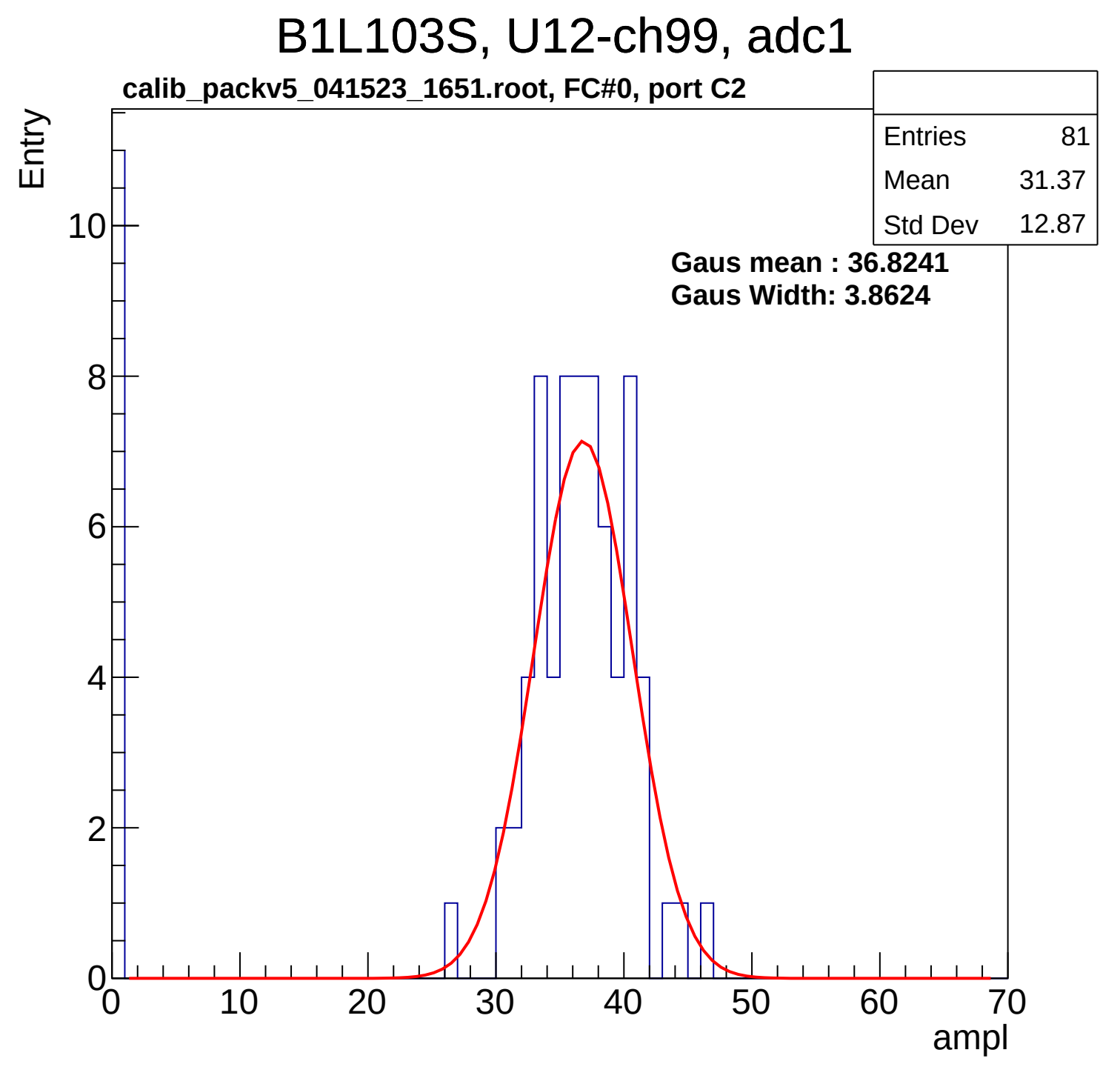
B1L103S, U12-ch99, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 31.37
Std Dev 12.87
Gaus mean : 36.8241
Gaus Width: 3.8624
Entry
ampl
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2
4
6
8
10
0
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20
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40
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60
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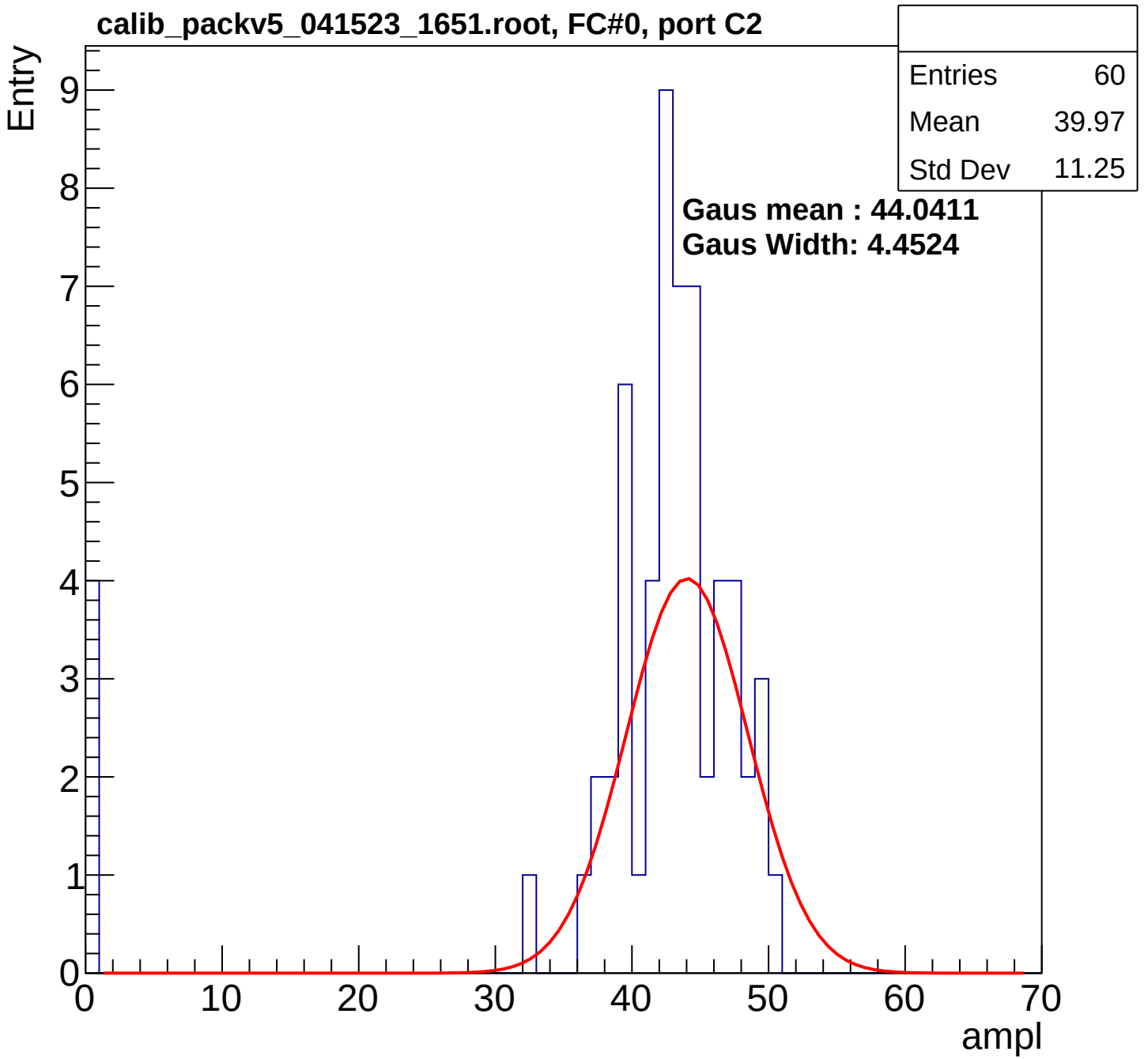
B1L103S, U12-ch99, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 39.97
Std Dev 11.25
Gaus mean : 44.0411
Gaus Width: 4.4524
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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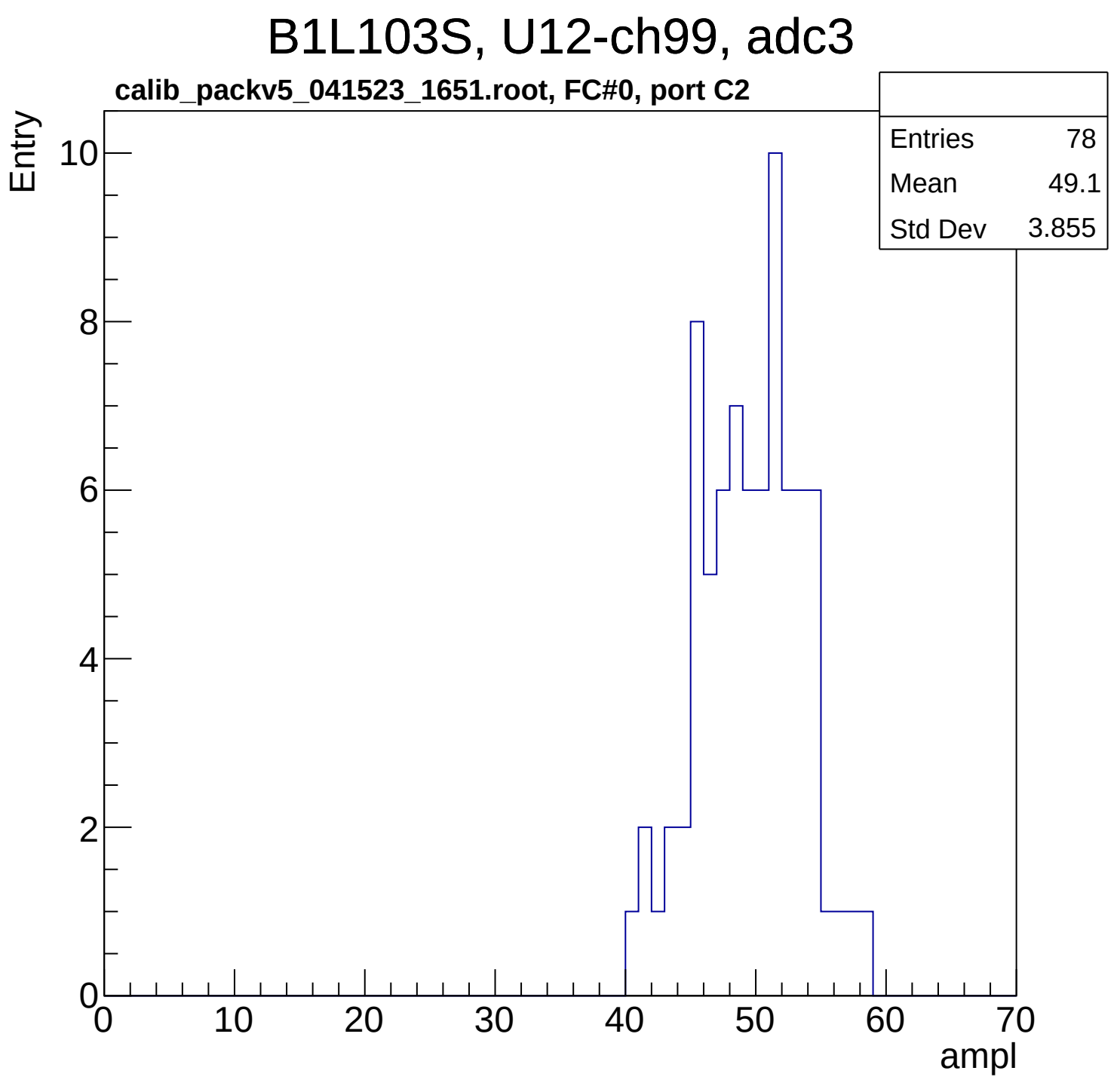
B1L103S, U12-ch99, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 49.1
Std Dev 3.855
Entry
ampl
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60
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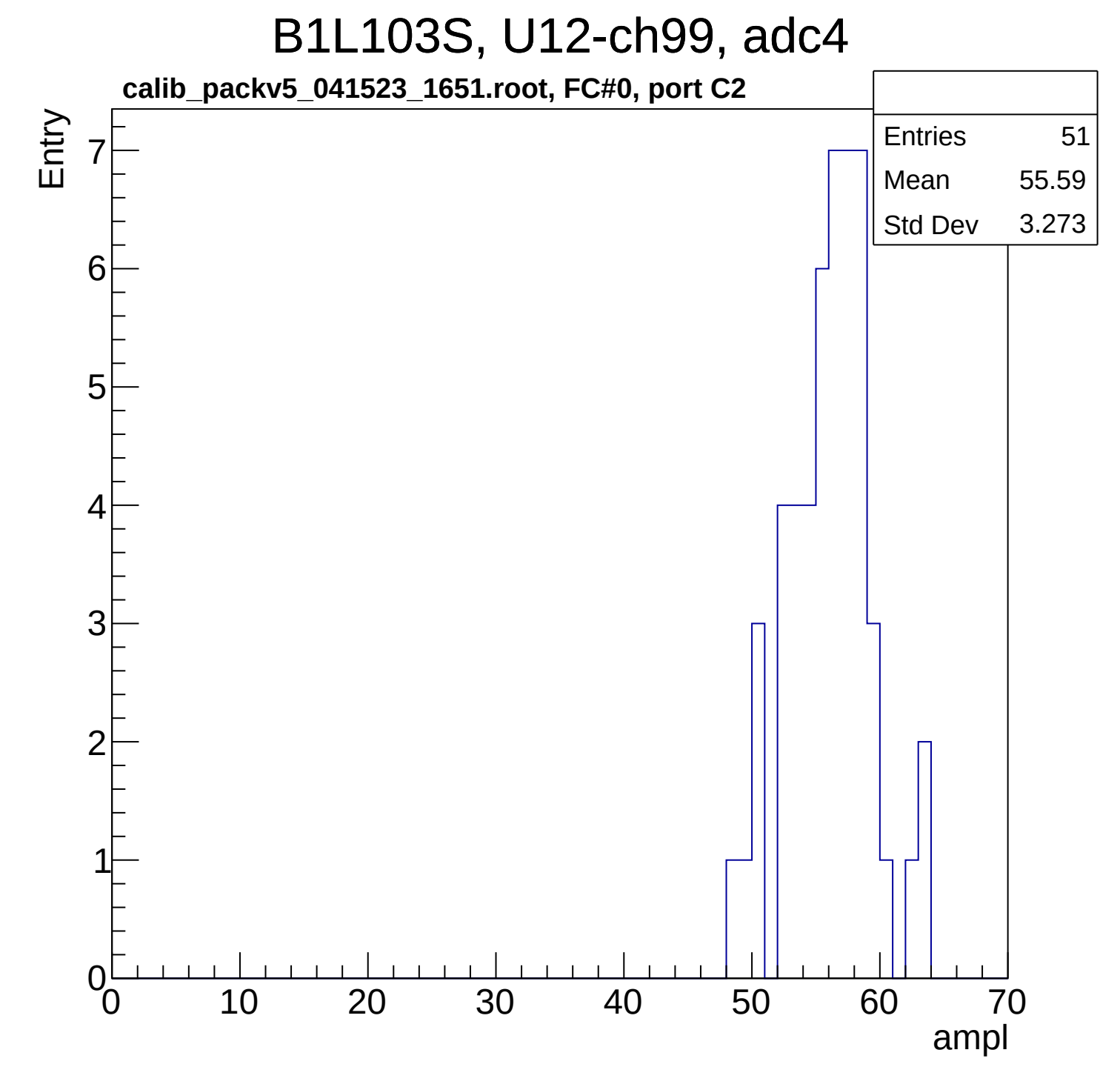
B1L103S, U12-ch99, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 55.59
Std Dev 3.273
Entry
ampl
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3
4
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0
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60
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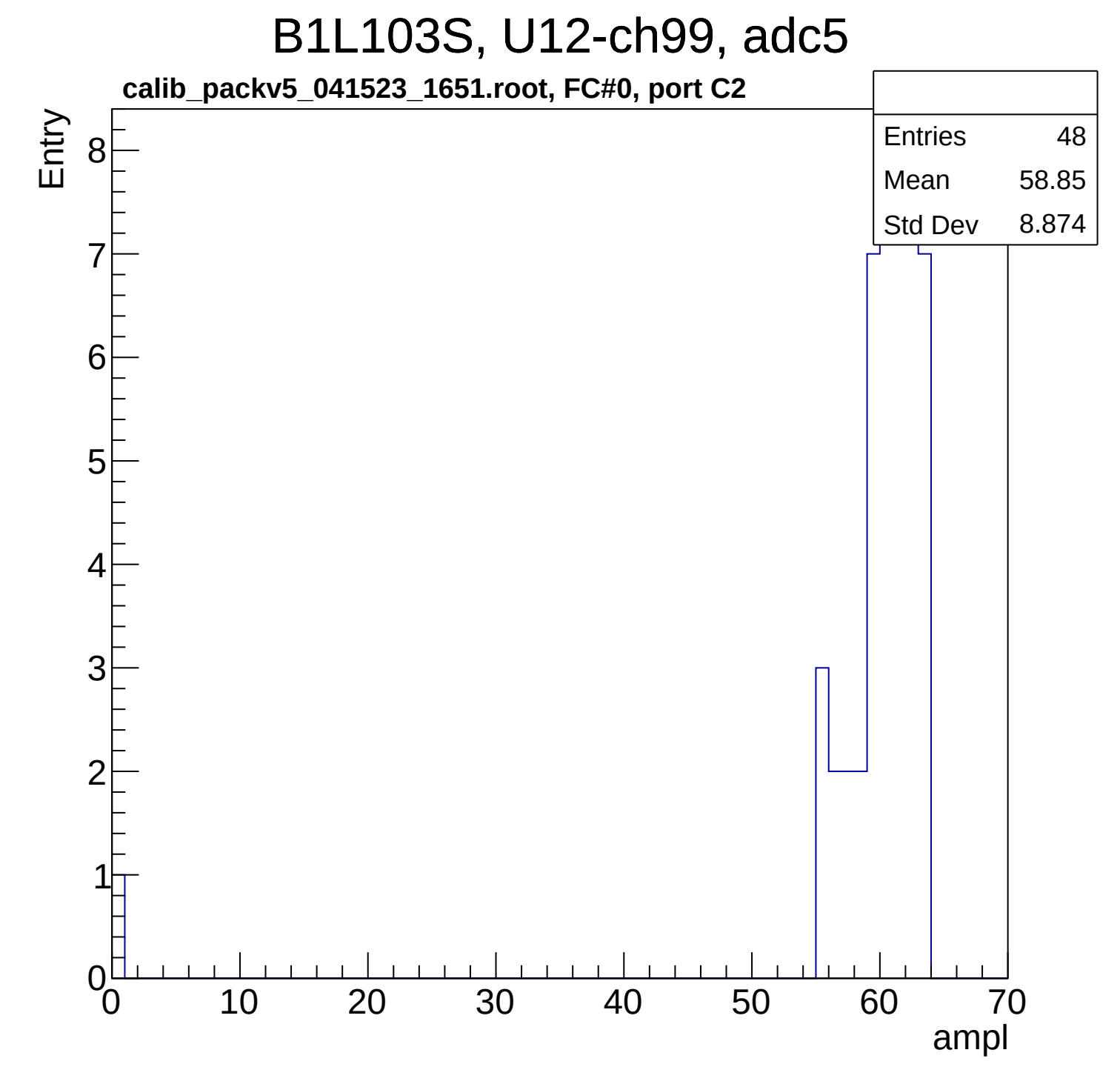
B1L103S, U12-ch99, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.85
Std Dev 8.874
Entry
ampl
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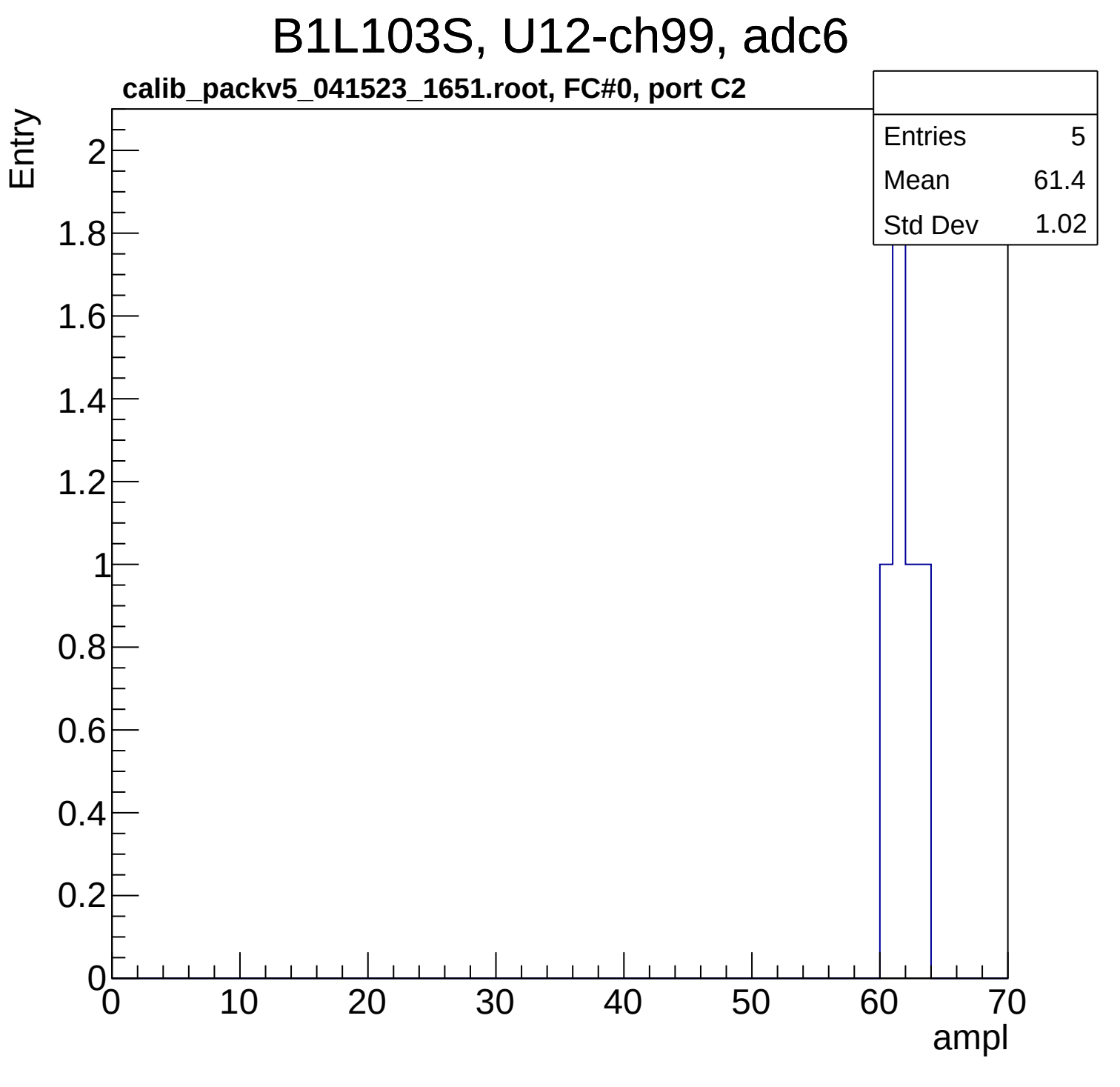
B1L103S, U12-ch99, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.4
Std Dev 1.02
Entry
ampl
0
0.2
0.4
0.6
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1
1.2
1.4
1.6
1.8
2
0
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60
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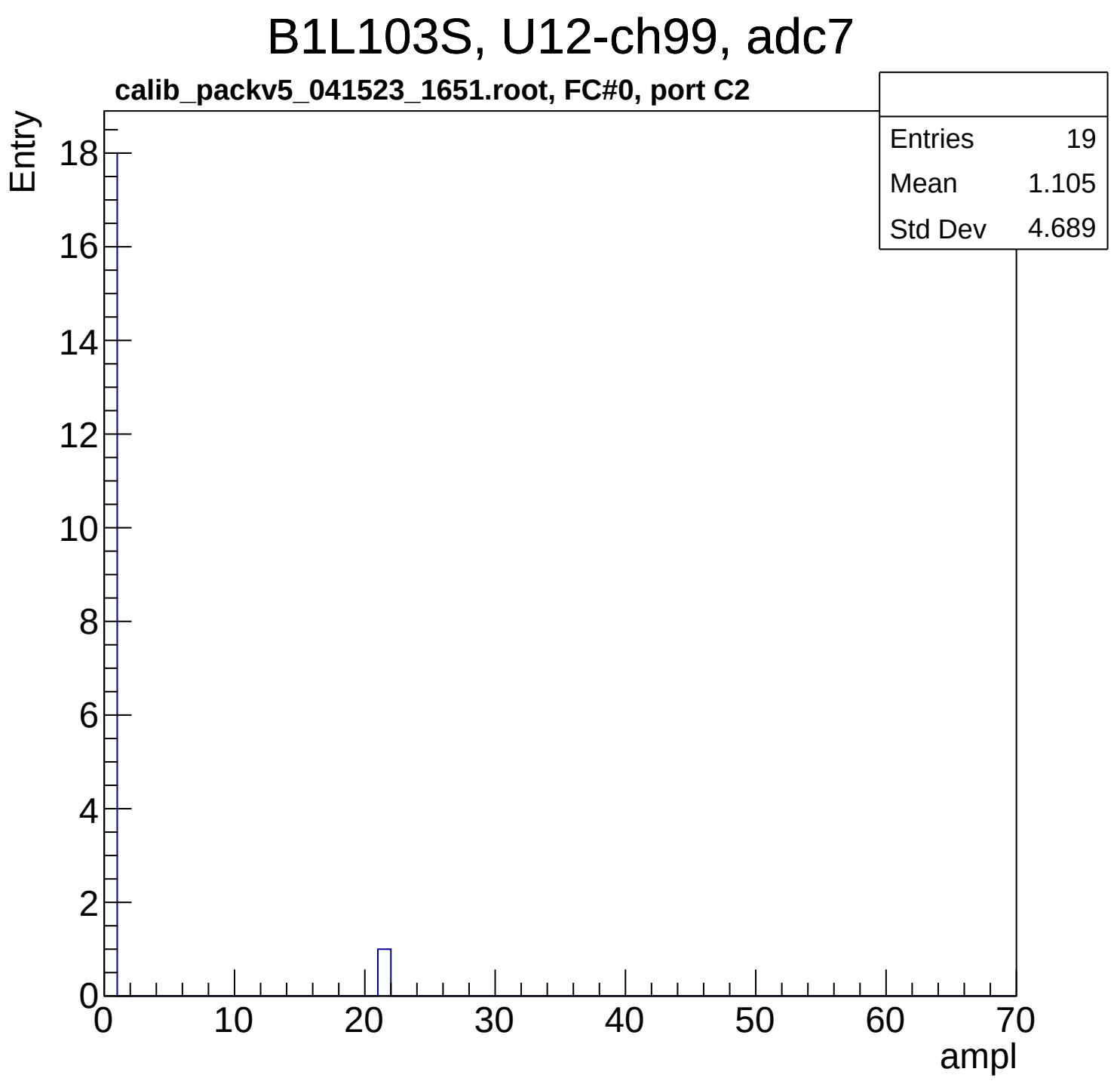
B1L103S, U12-ch99, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 1.105
Std Dev 4.689
Entry
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6
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10
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14
16
18
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10
20
30
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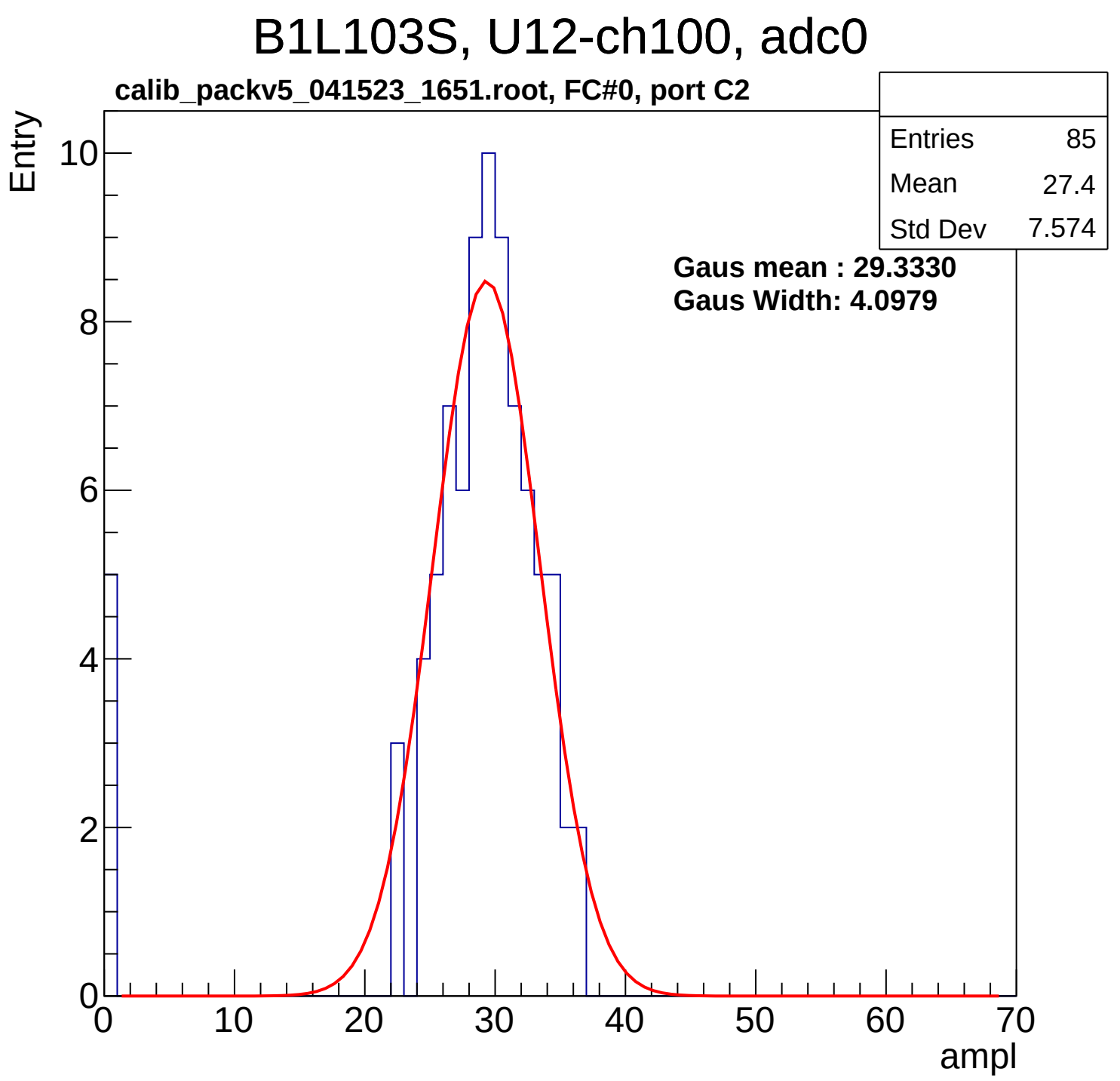
50
60
70
ampl


B1L103S, U12-ch100, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 27.4
Std Dev 7.574
Gaus mean : 29.3330
Gaus Width: 4.0979
Entry
ampl
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2
4
6
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10
0
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20
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40
50
60
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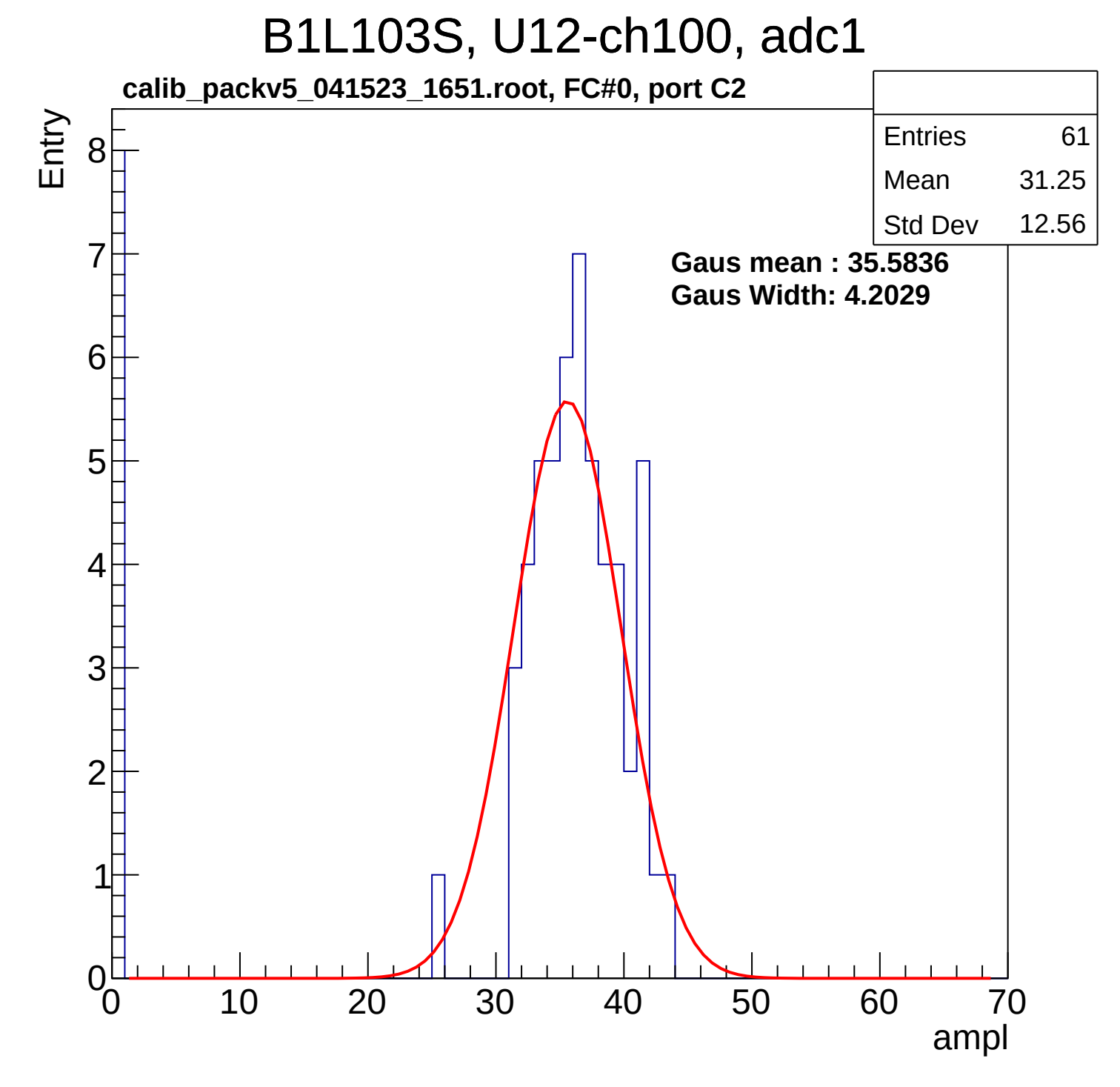
B1L103S, U12-ch100, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 31.25
Std Dev 12.56
Gaus mean : 35.5836
Gaus Width: 4.2029
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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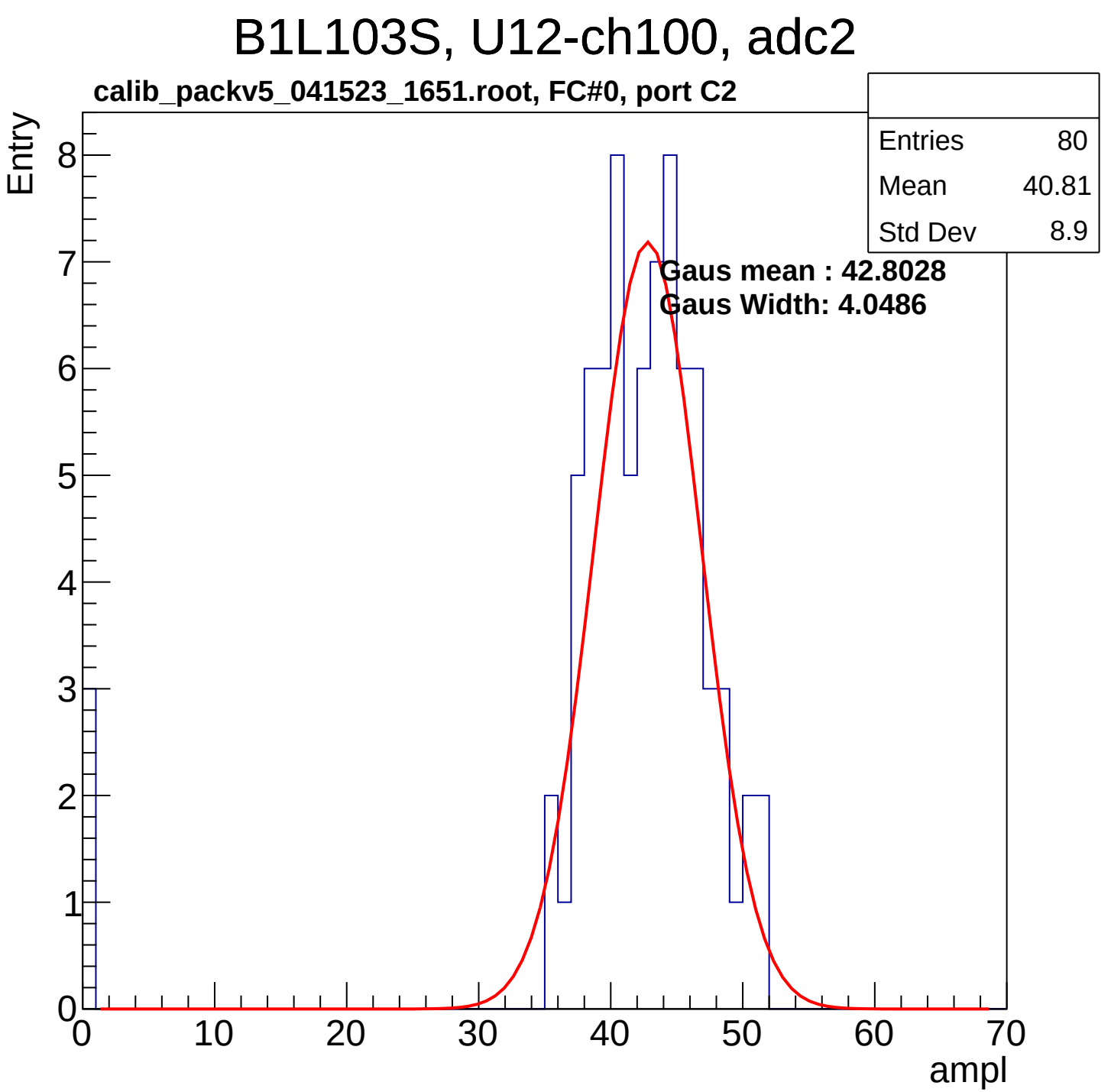
B1L103S, U12-ch100, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 40.81
Std Dev 8.9
Gaus mean : 42.8028
Gaus Width: 4.0486
Entry
ampl
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1
2
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4
5
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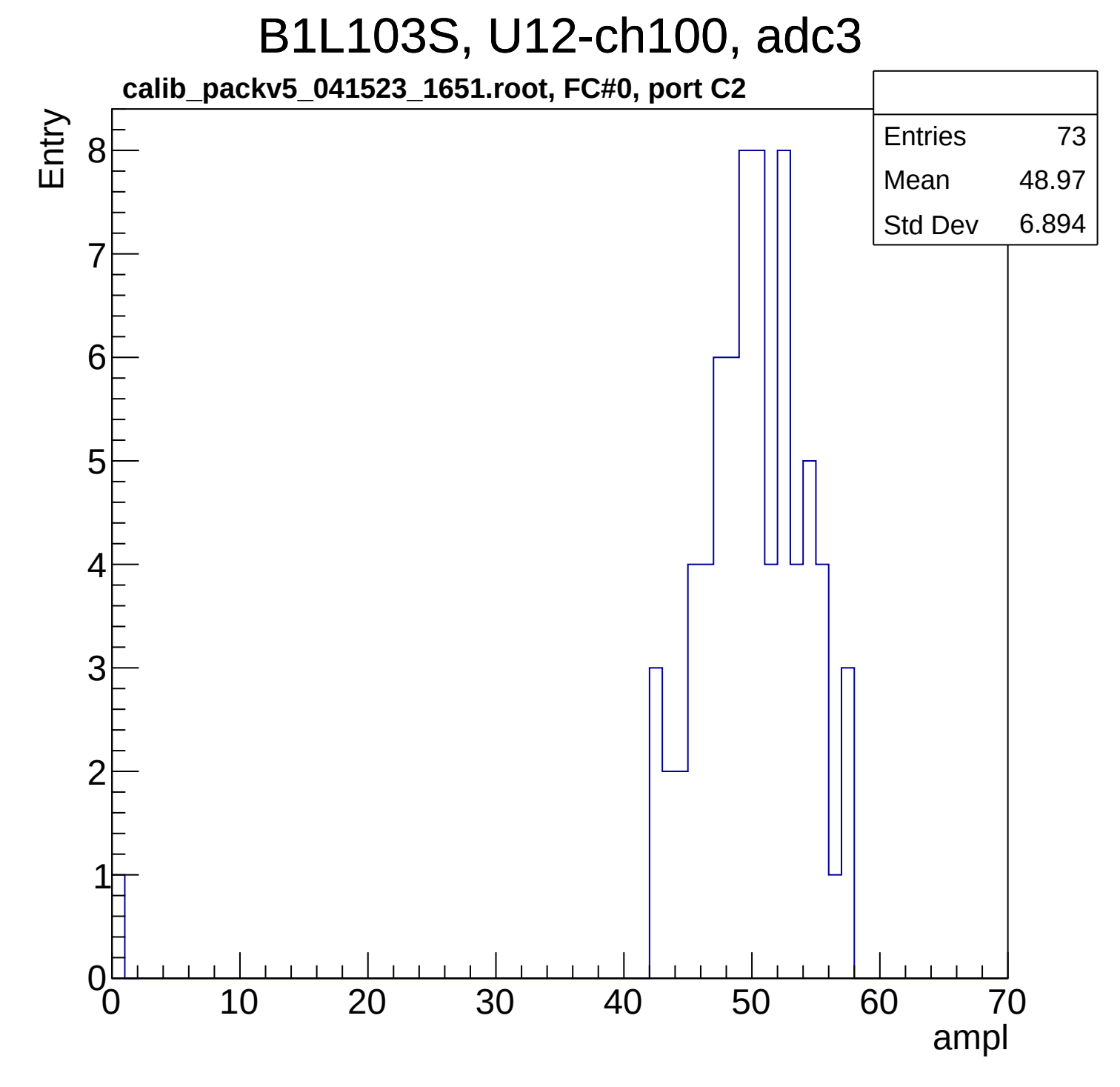
B1L103S, U12-ch100, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 48.97
Std Dev 6.894
Entry
ampl
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1
2
3
4
5
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7
8
0
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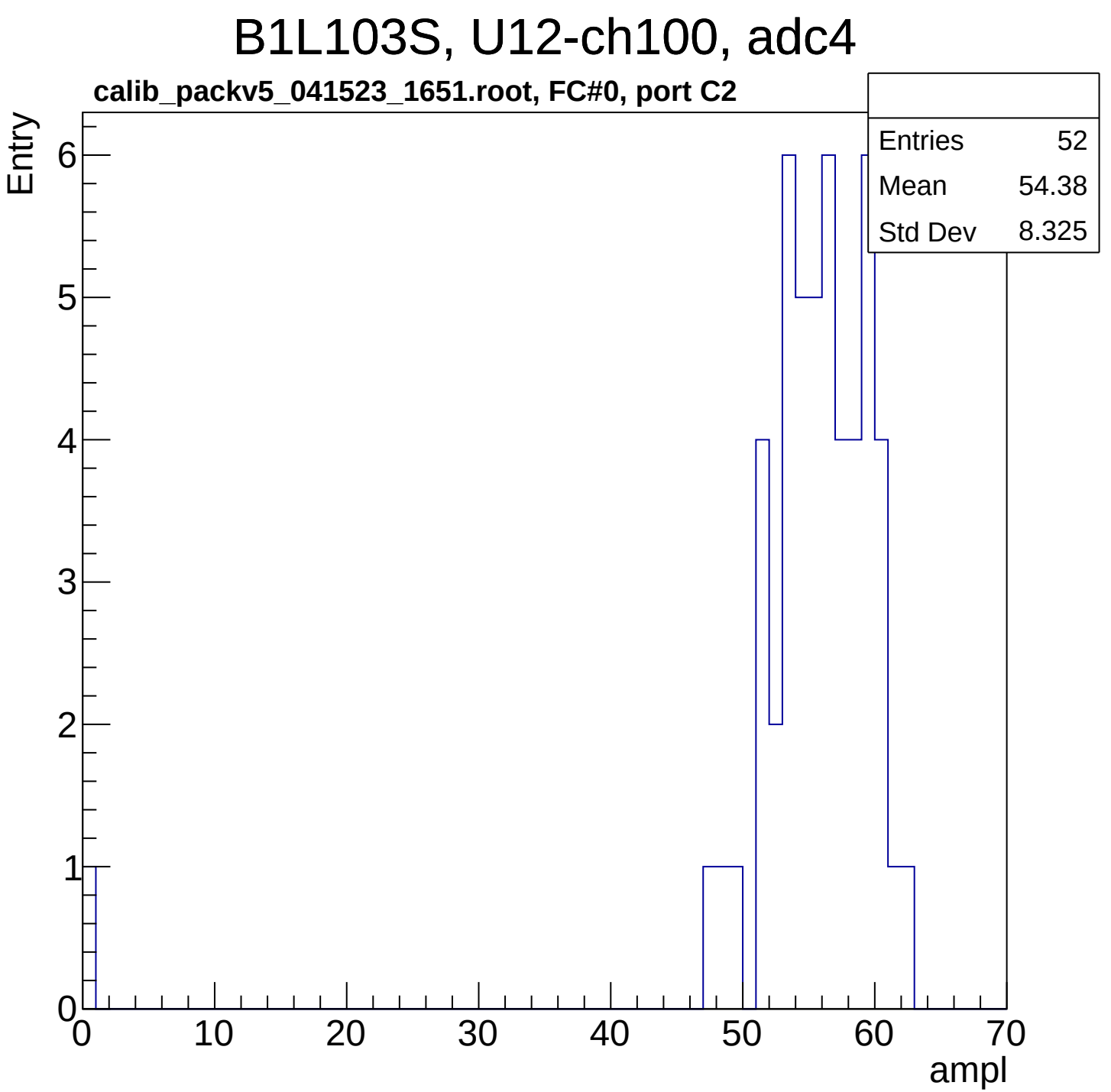
40
50
60
70


B1L103S, U12-ch100, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 54.38
Std Dev 8.325
Entry
ampl
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2
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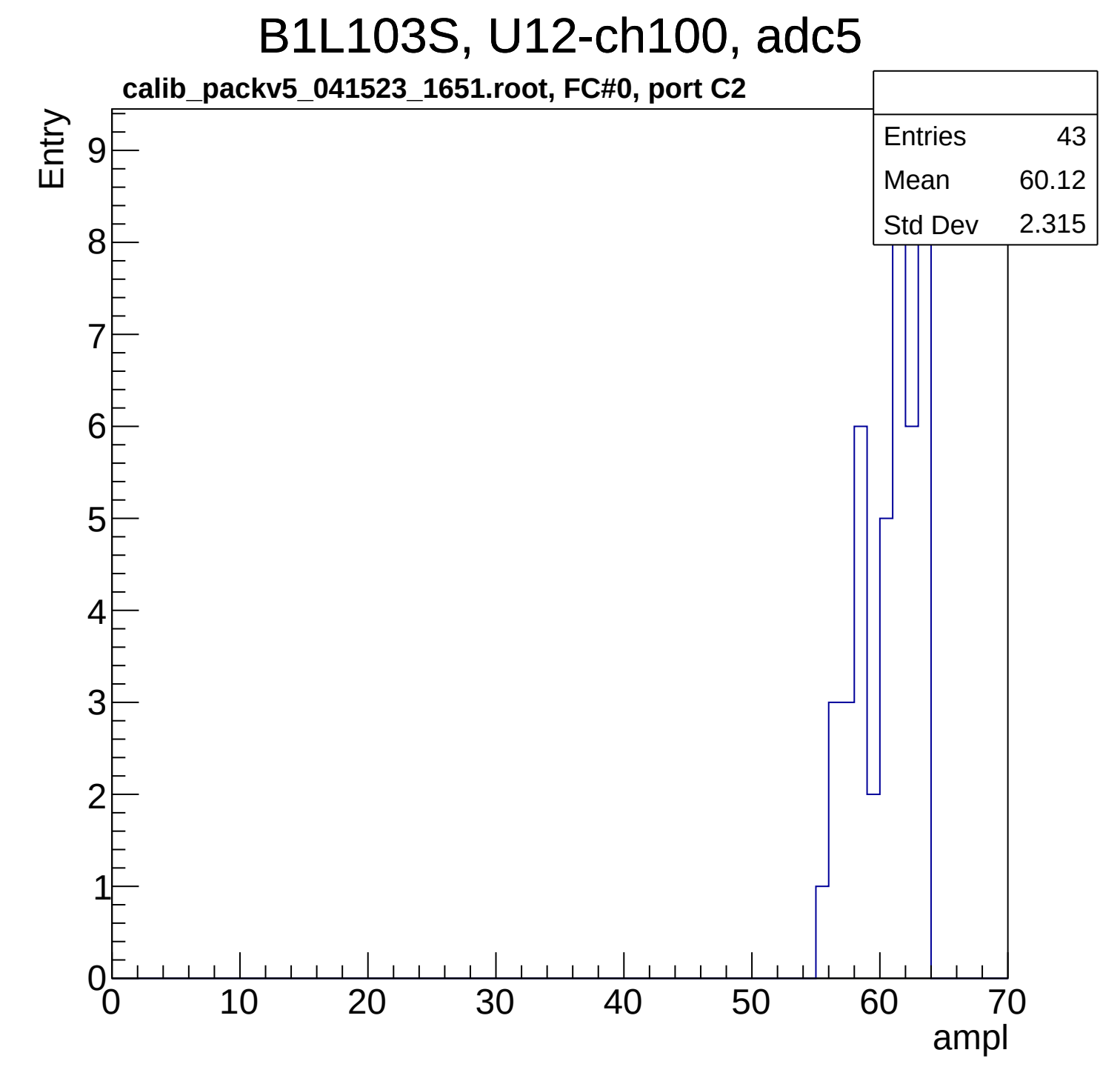
B1L103S, U12-ch100, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 60.12
Std Dev 2.315
Entry
ampl
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3
4
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6
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0
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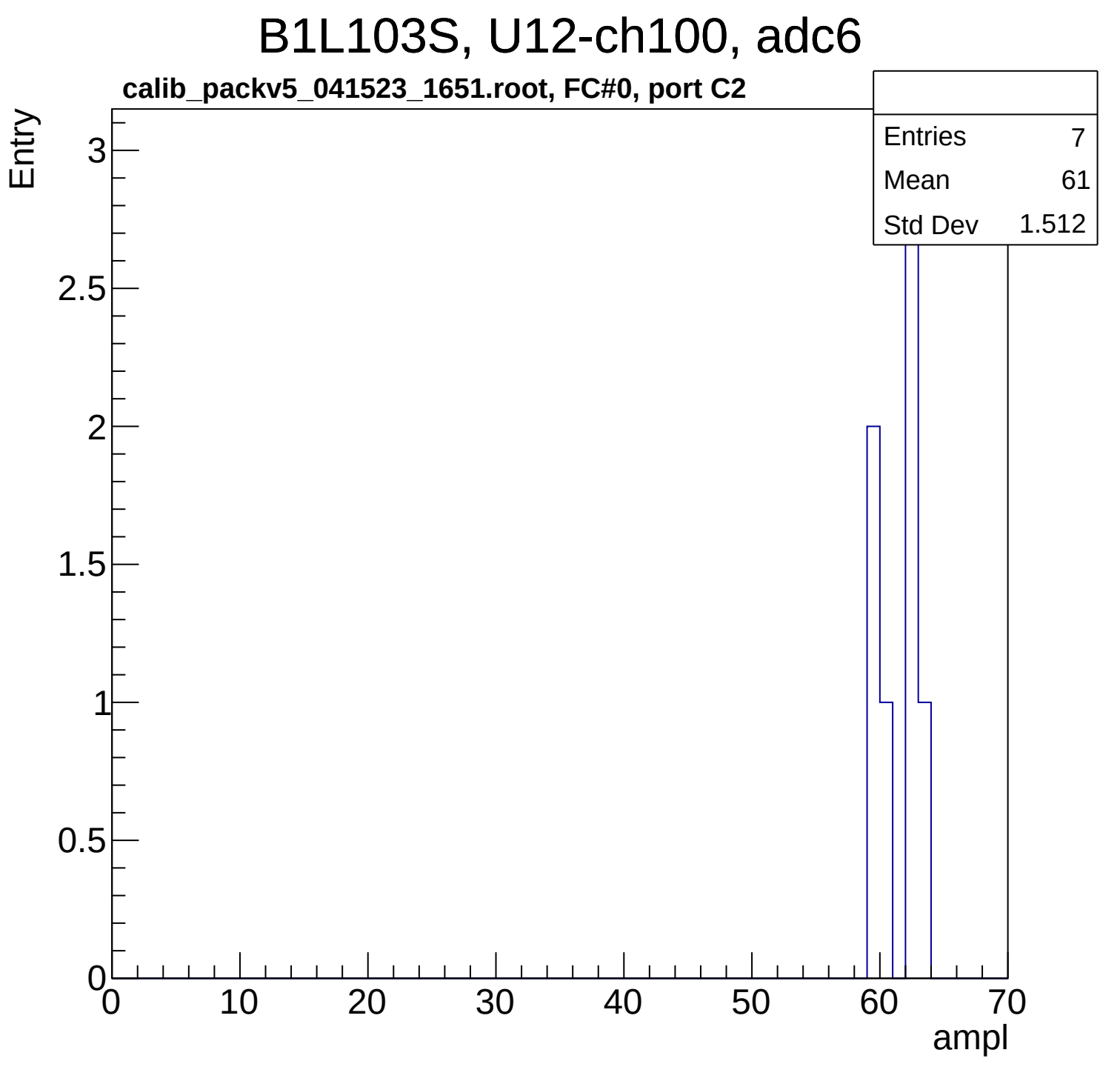
B1L103S, U12-ch100, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61
Std Dev 1.512
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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40
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60
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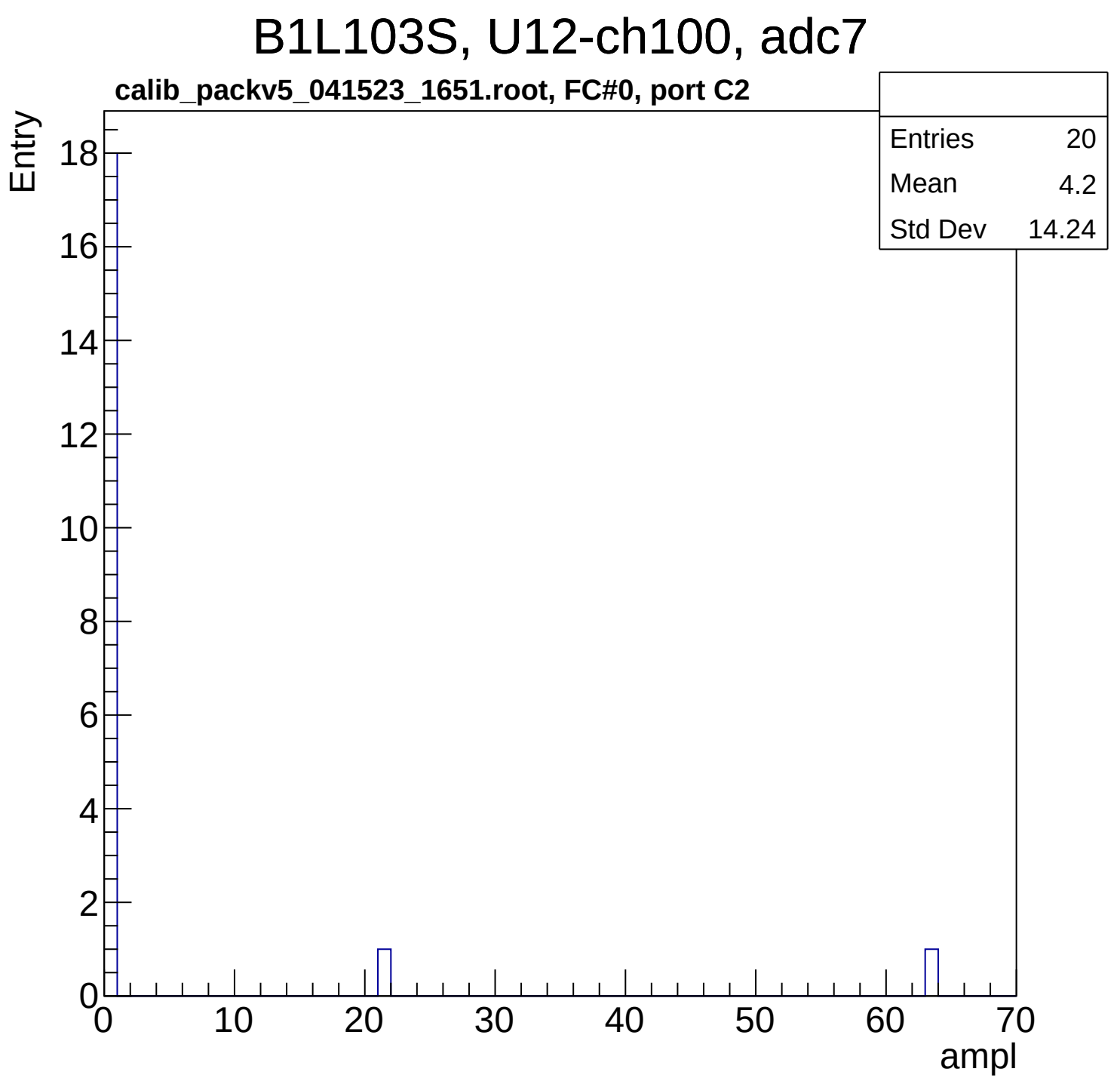
B1L103S, U12-ch100, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 4.2
Std Dev 14.24
Entry
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4
6
8
10
12
14
16
18
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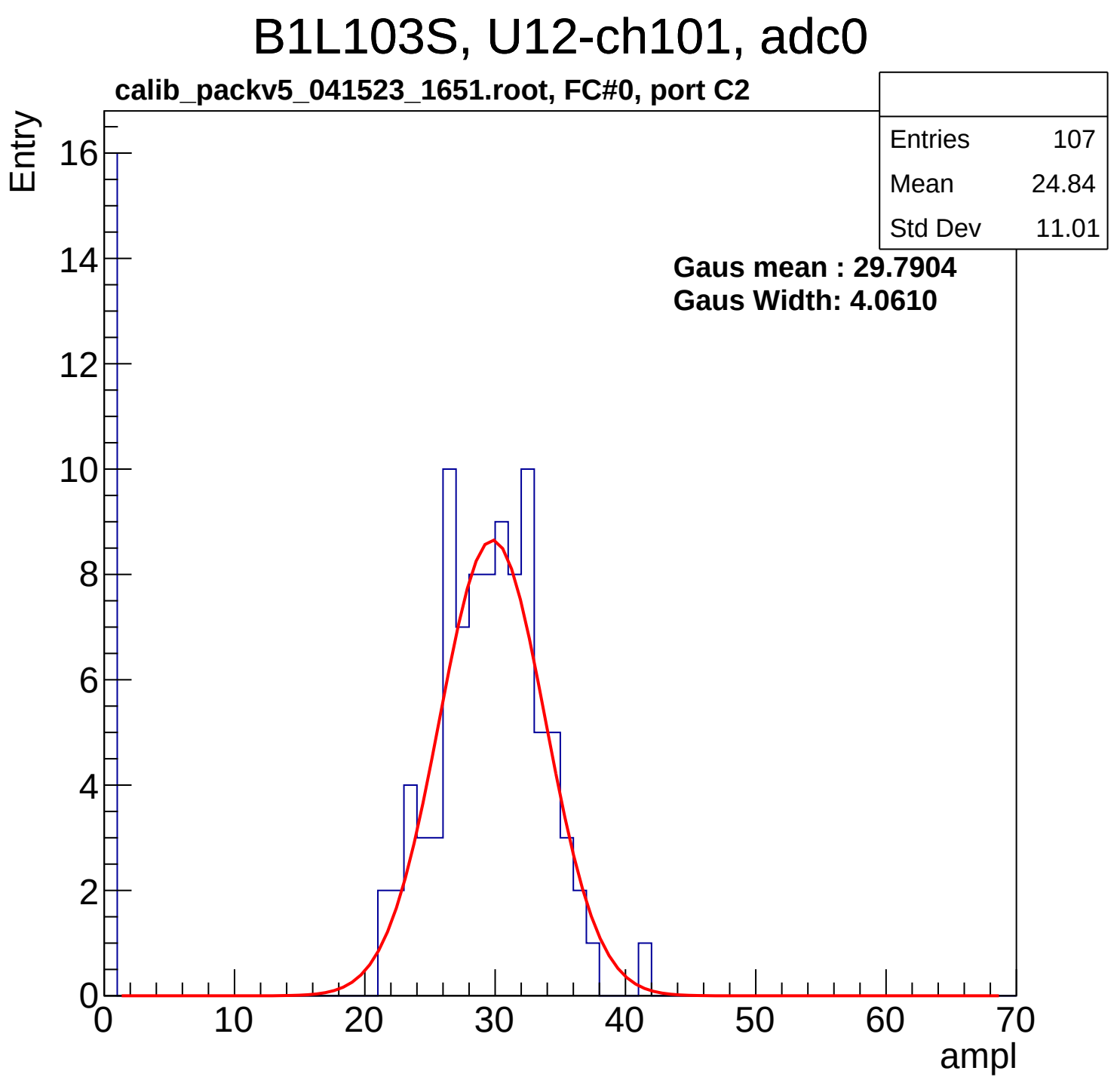
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch101, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 107
Mean 24.84
Std Dev 11.01
Gaus mean : 29.7904
Gaus Width: 4.0610
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
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40
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60
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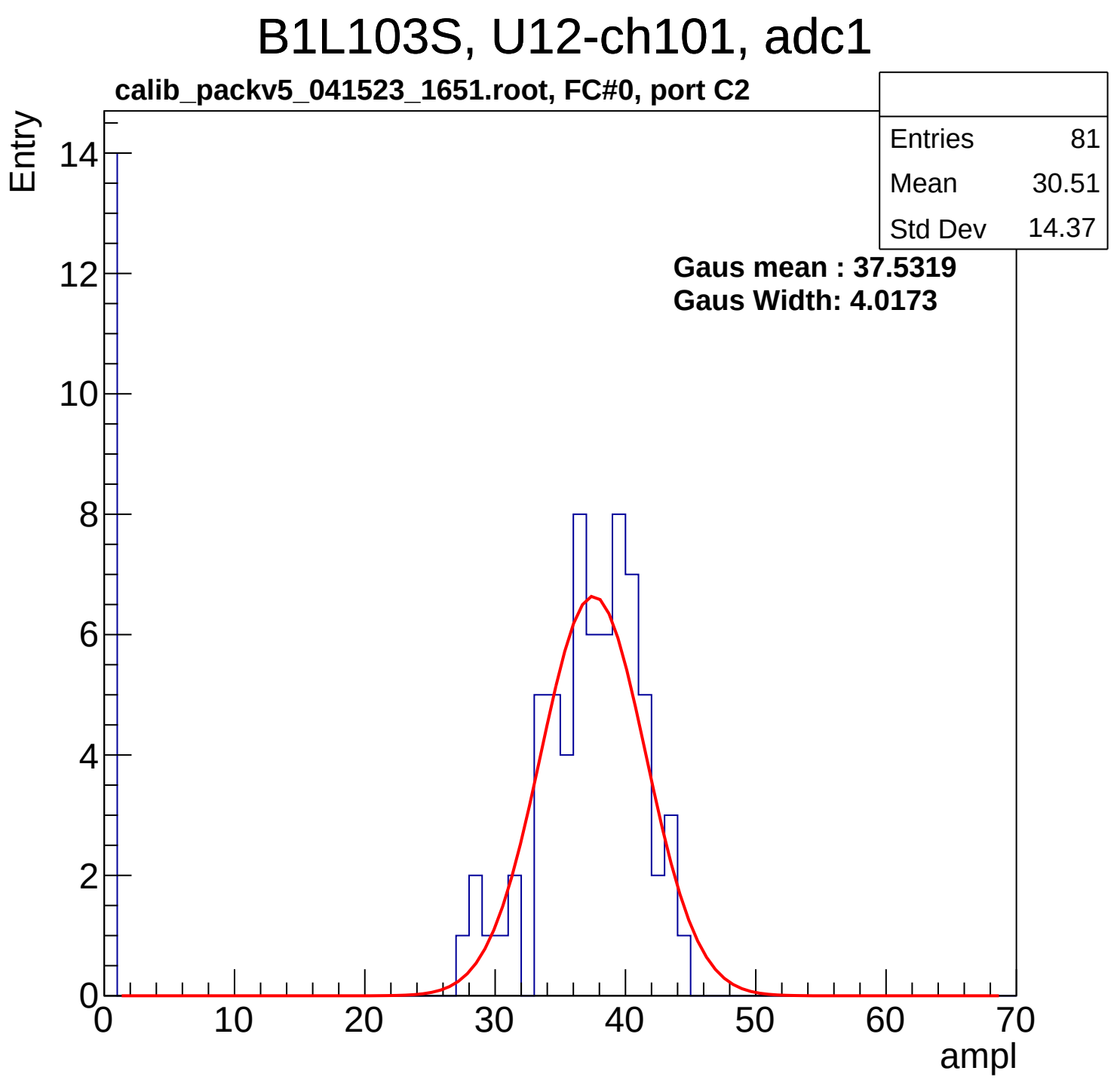
B1L103S, U12-ch101, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 30.51
Std Dev 14.37
Gaus mean : 37.5319
Gaus Width: 4.0173
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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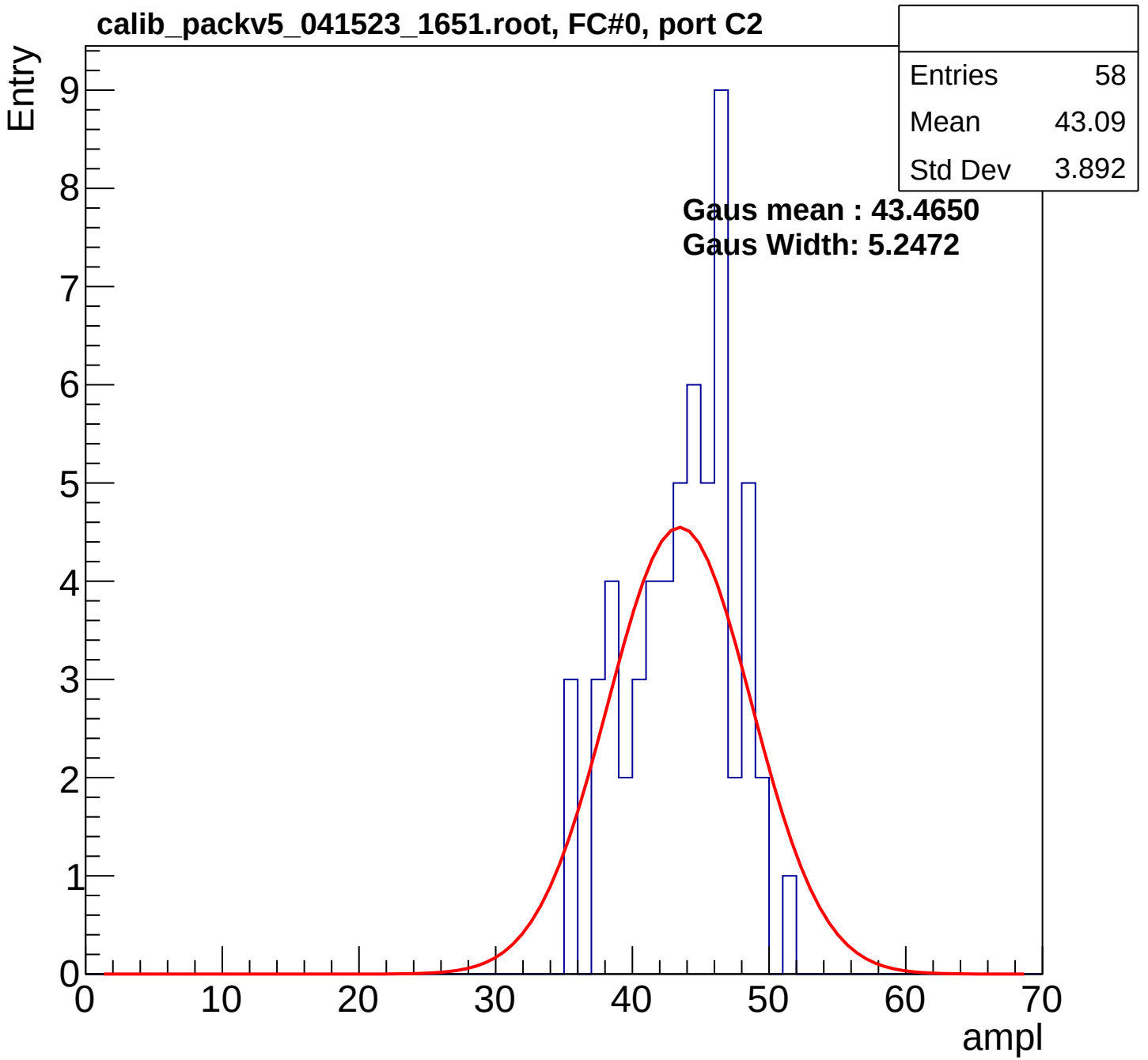
B1L103S, U12-ch101, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 43.09
Std Dev 3.892
Gaus mean : 43.4650
Gaus Width: 5.2472
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
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40
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60
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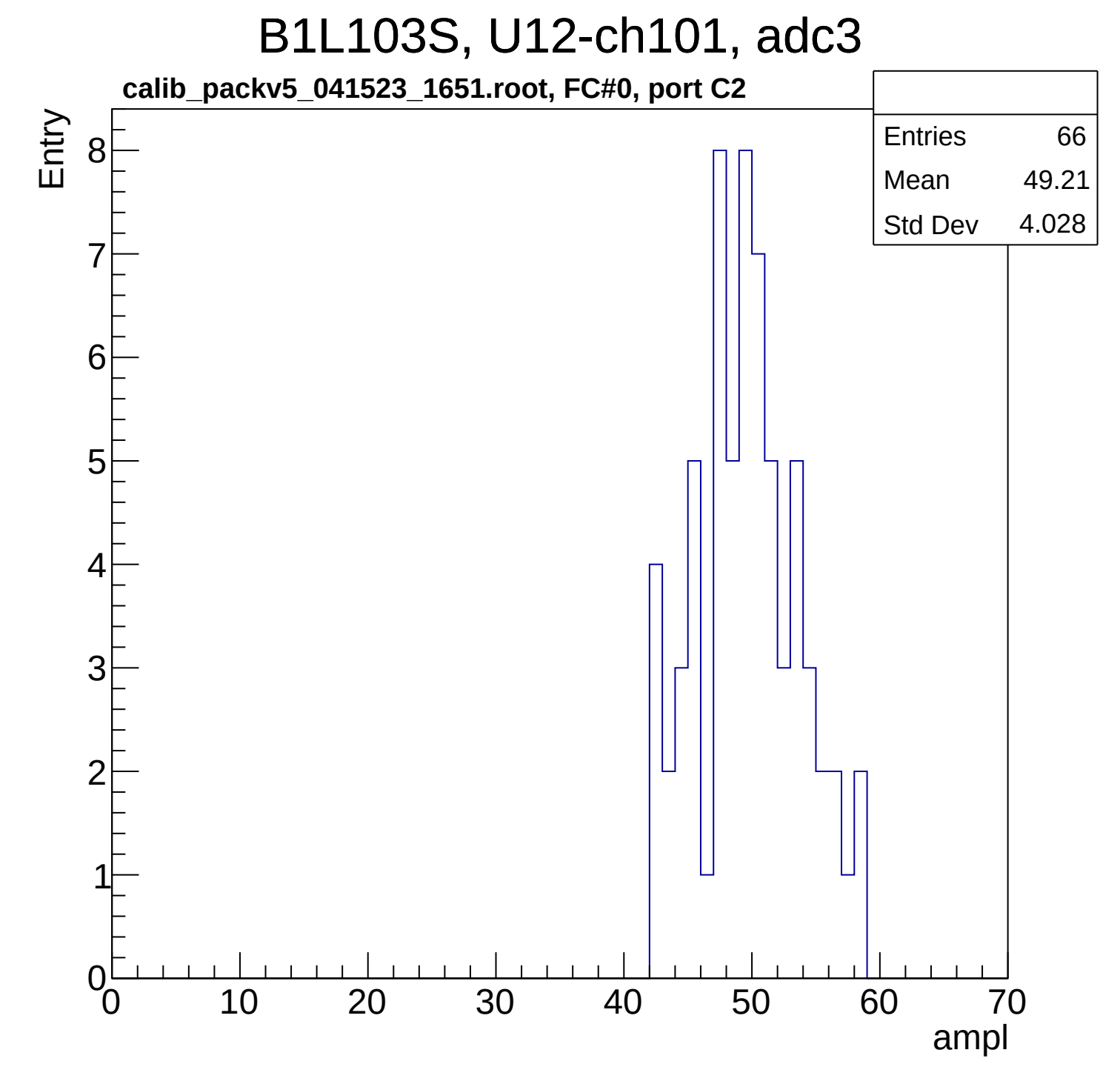
B1L103S, U12-ch101, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 49.21
Std Dev 4.028
Entry
ampl
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1
2
3
4
5
6
7
8
0
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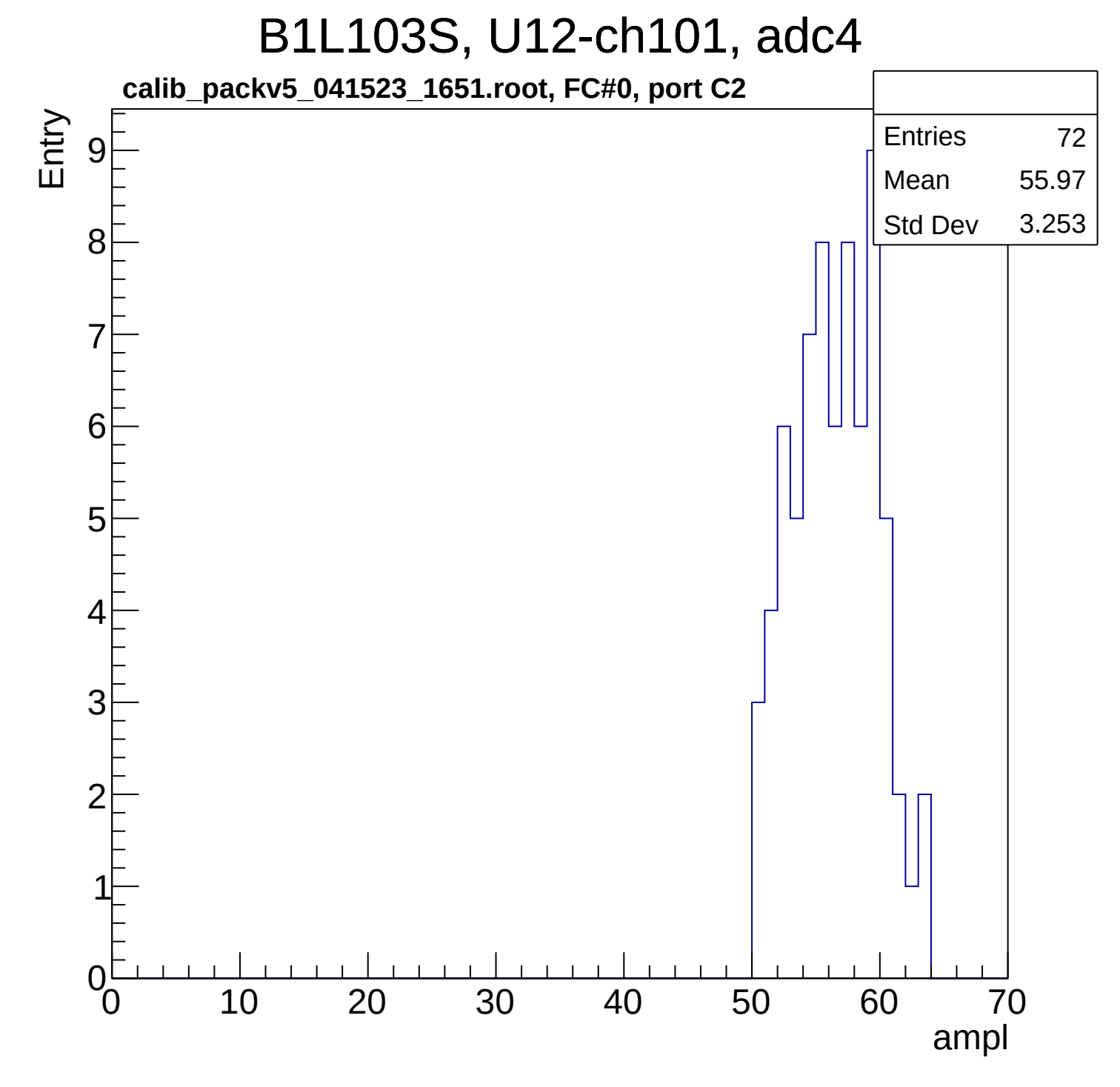
B1L103S, U12-ch101, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 55.97
Std Dev 3.253
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
30
40
50
60
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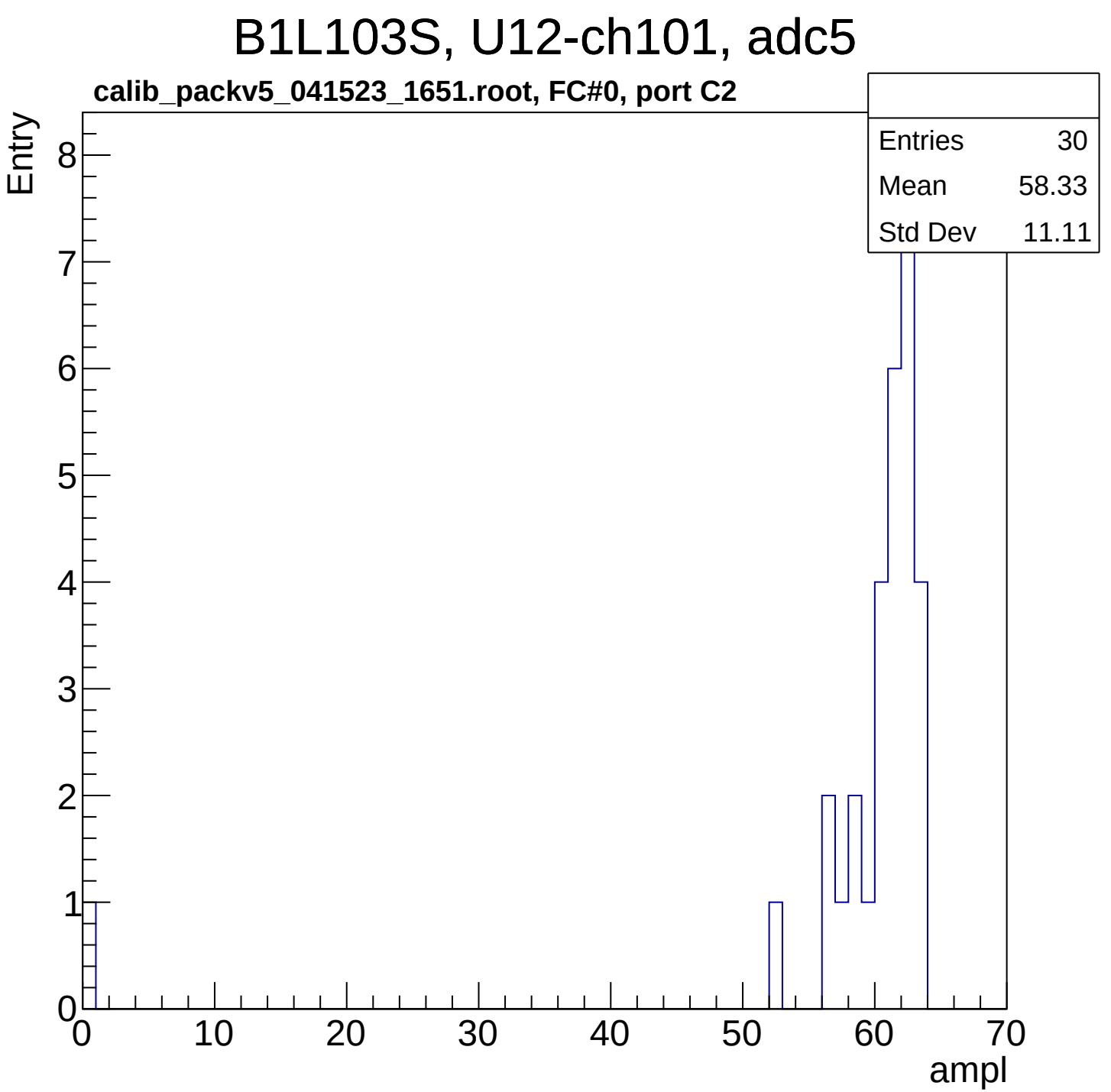
B1L103S, U12-ch101, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 58.33
Std Dev 11.11
Entry
ampl
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2
3
4
5
6
7
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0
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60
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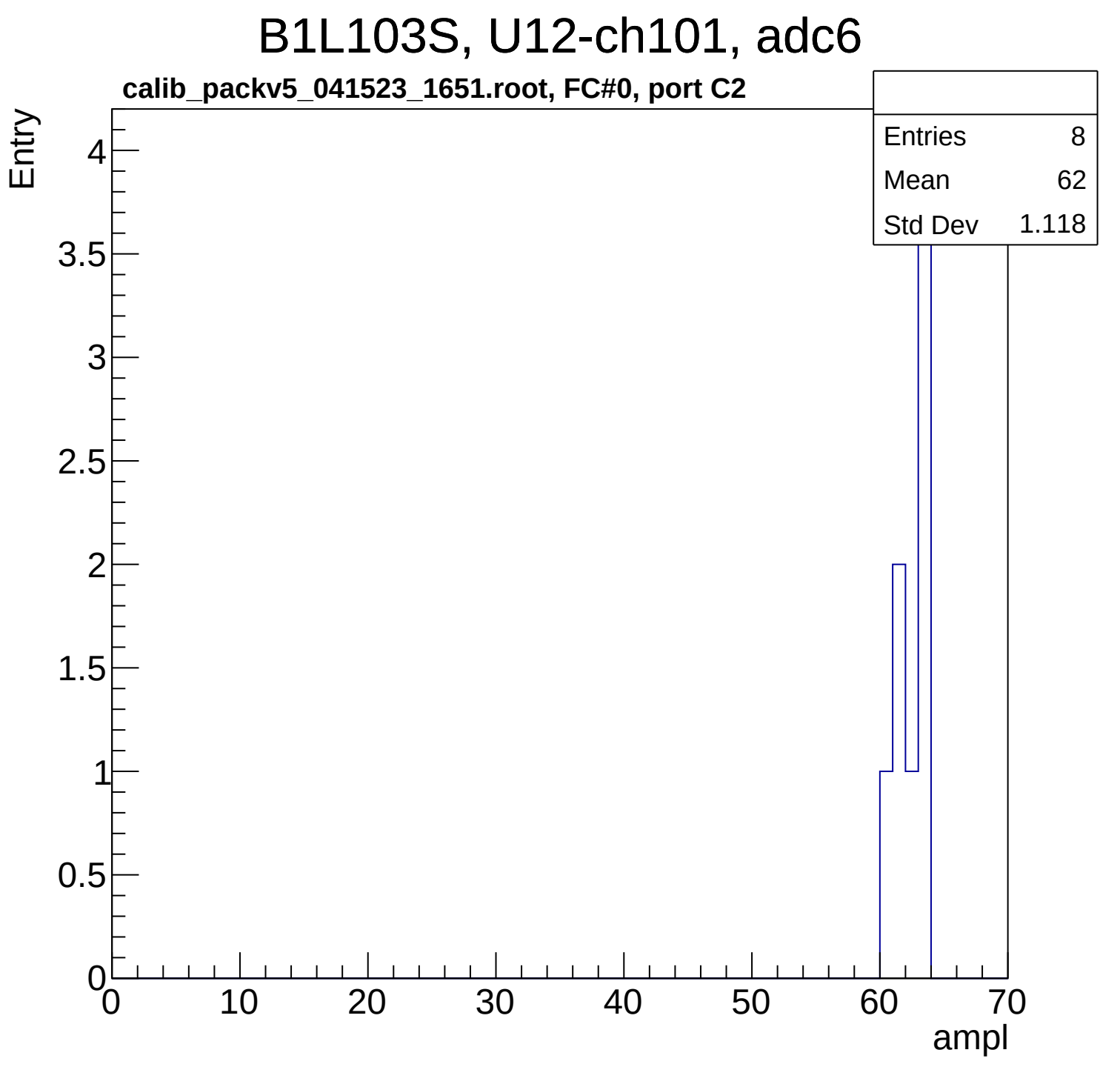
B1L103S, U12-ch101, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62
Std Dev 1.118
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
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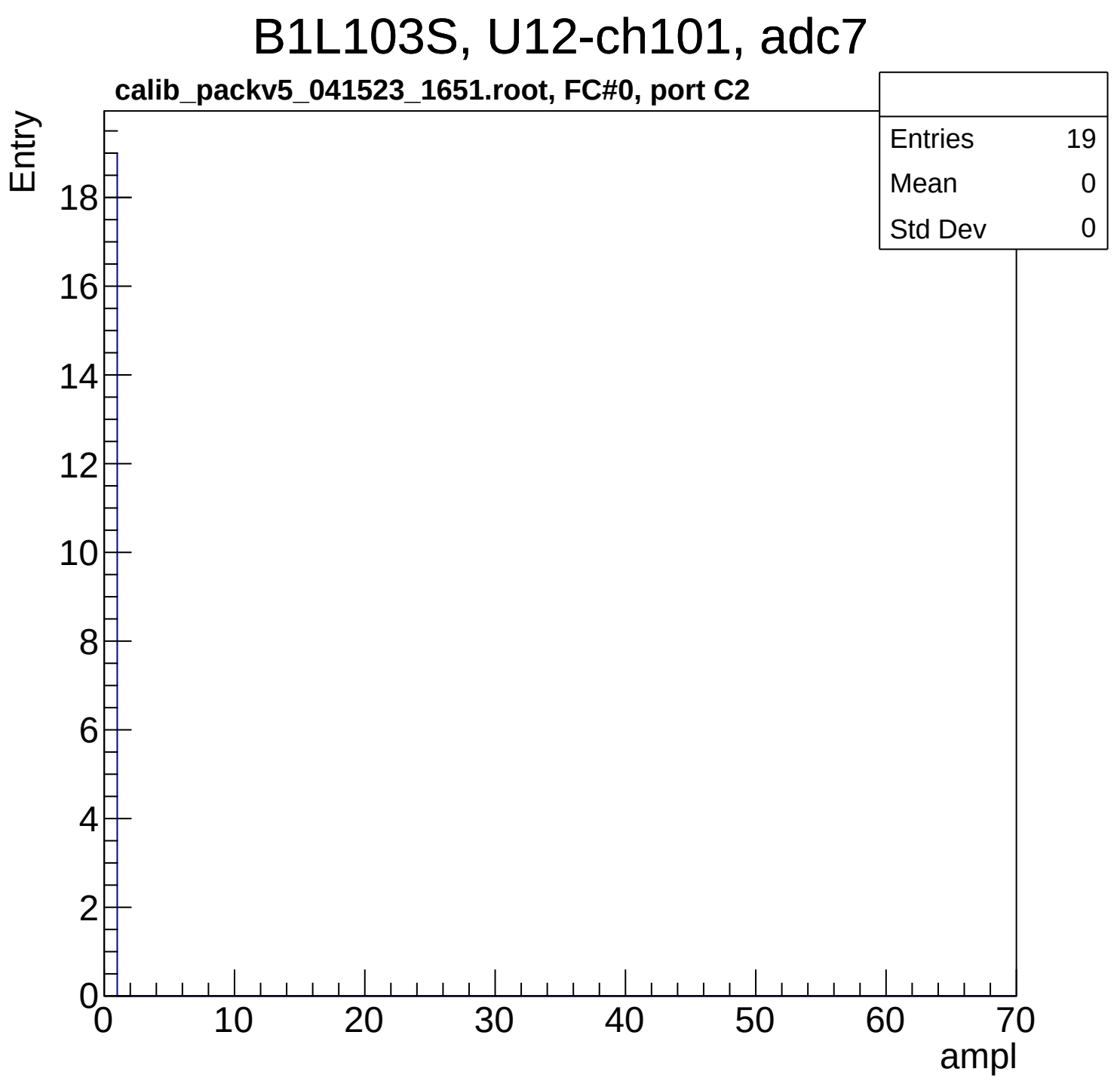
40
50
60
70


B1L103S, U12-ch101, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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4
6
8
10
12
14
16
18
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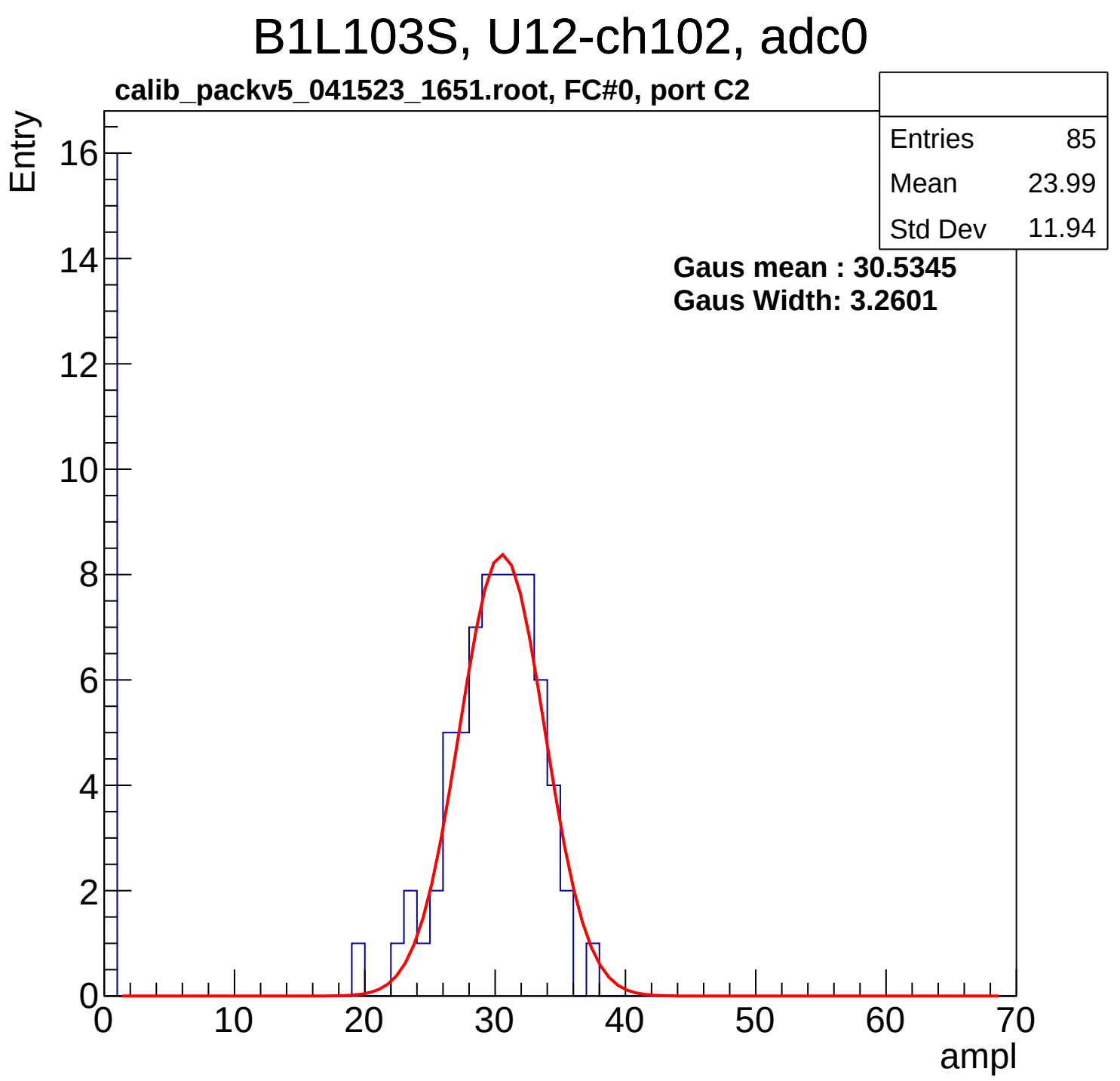
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch102, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 23.99
Std Dev 11.94
Gaus mean : 30.5345
Gaus Width: 3.2601
Entry
ampl
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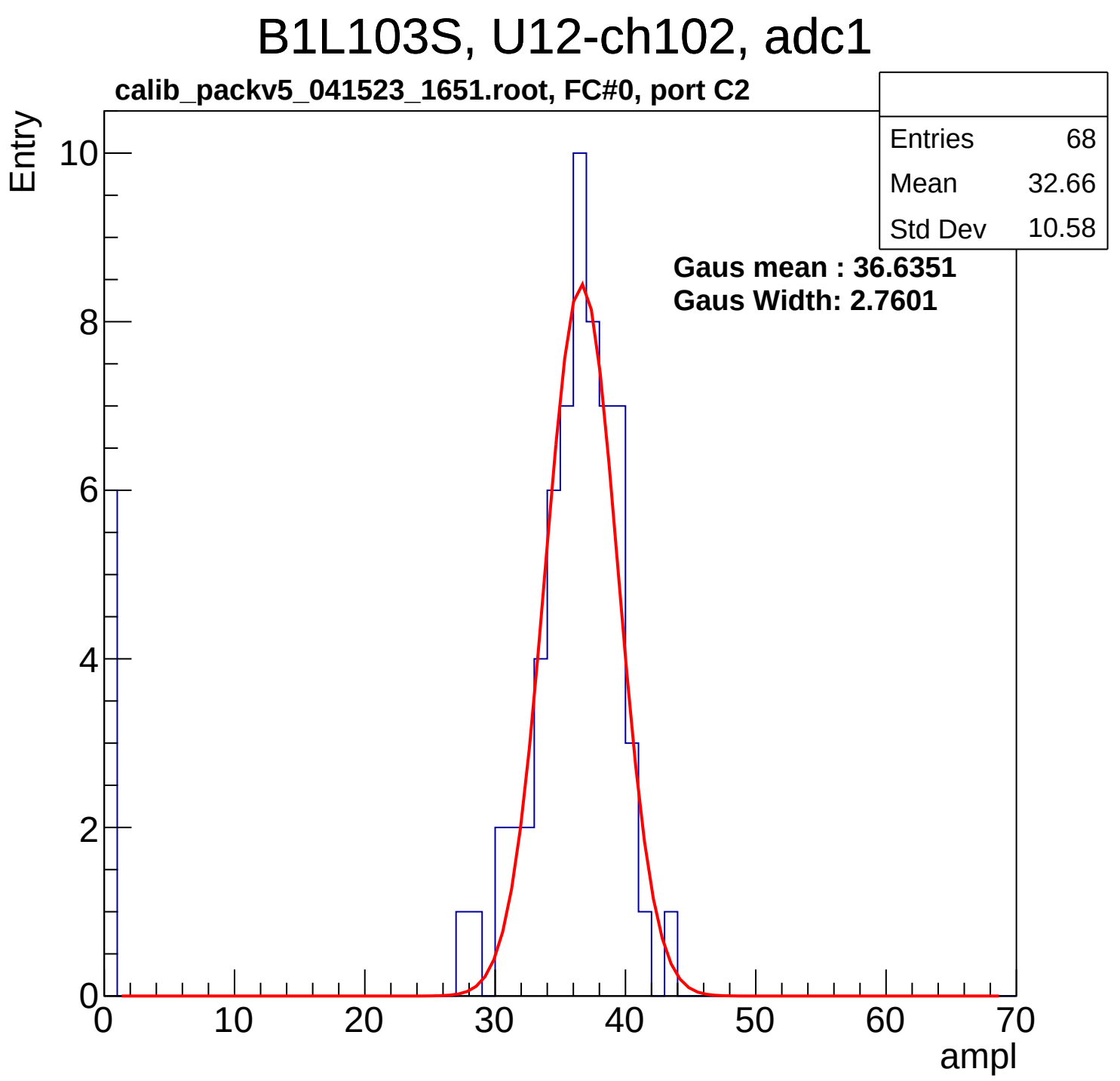
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U12-ch102, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 32.66
Std Dev 10.58
Gaus mean : 36.6351
Gaus Width: 2.7601
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
50
60
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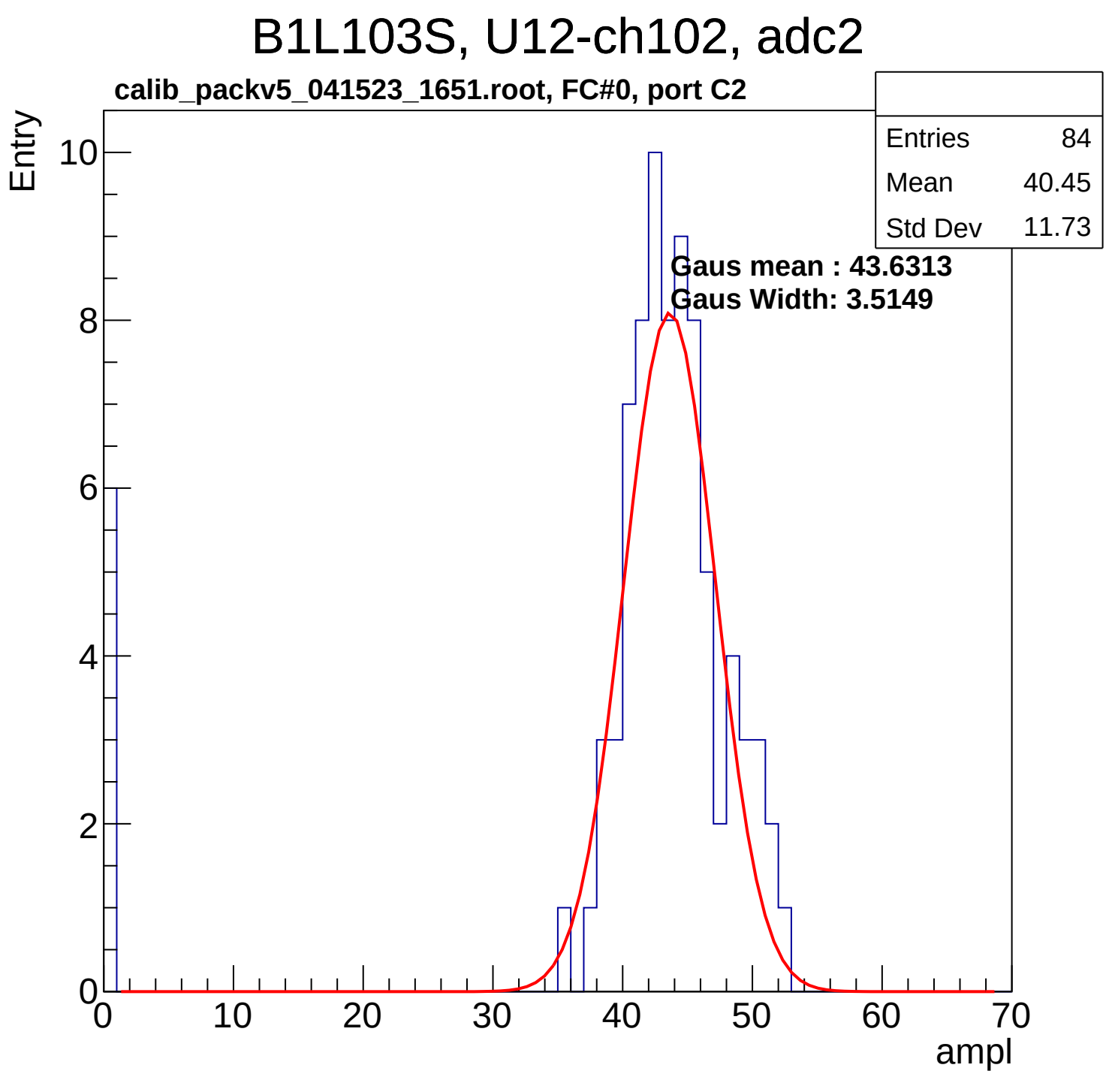
B1L103S, U12-ch102, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 40.45
Std Dev 11.73
Gaus mean : 43.6313
Gaus Width: 3.5149
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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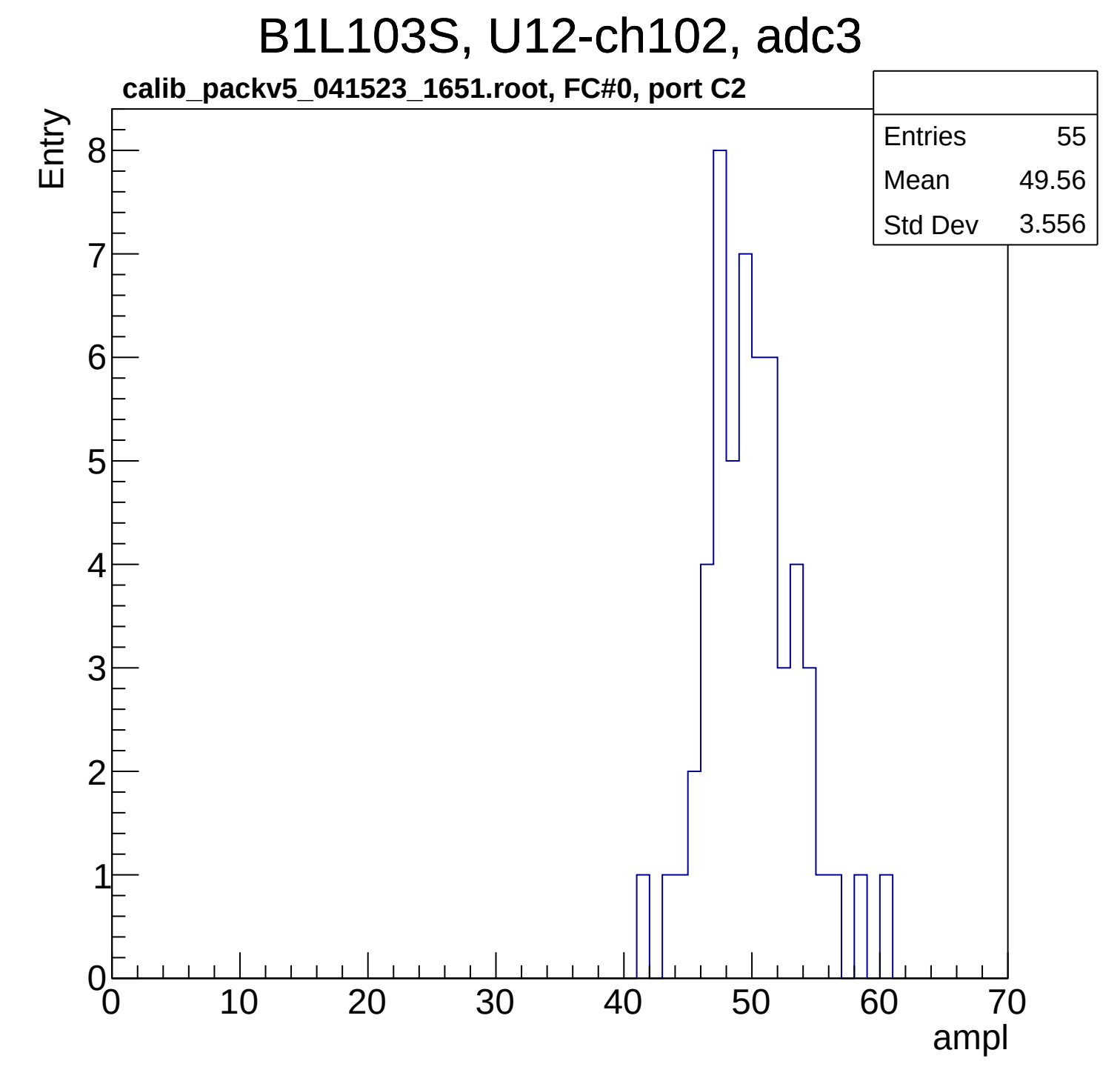
B1L103S, U12-ch102, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 49.56
Std Dev 3.556
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
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60
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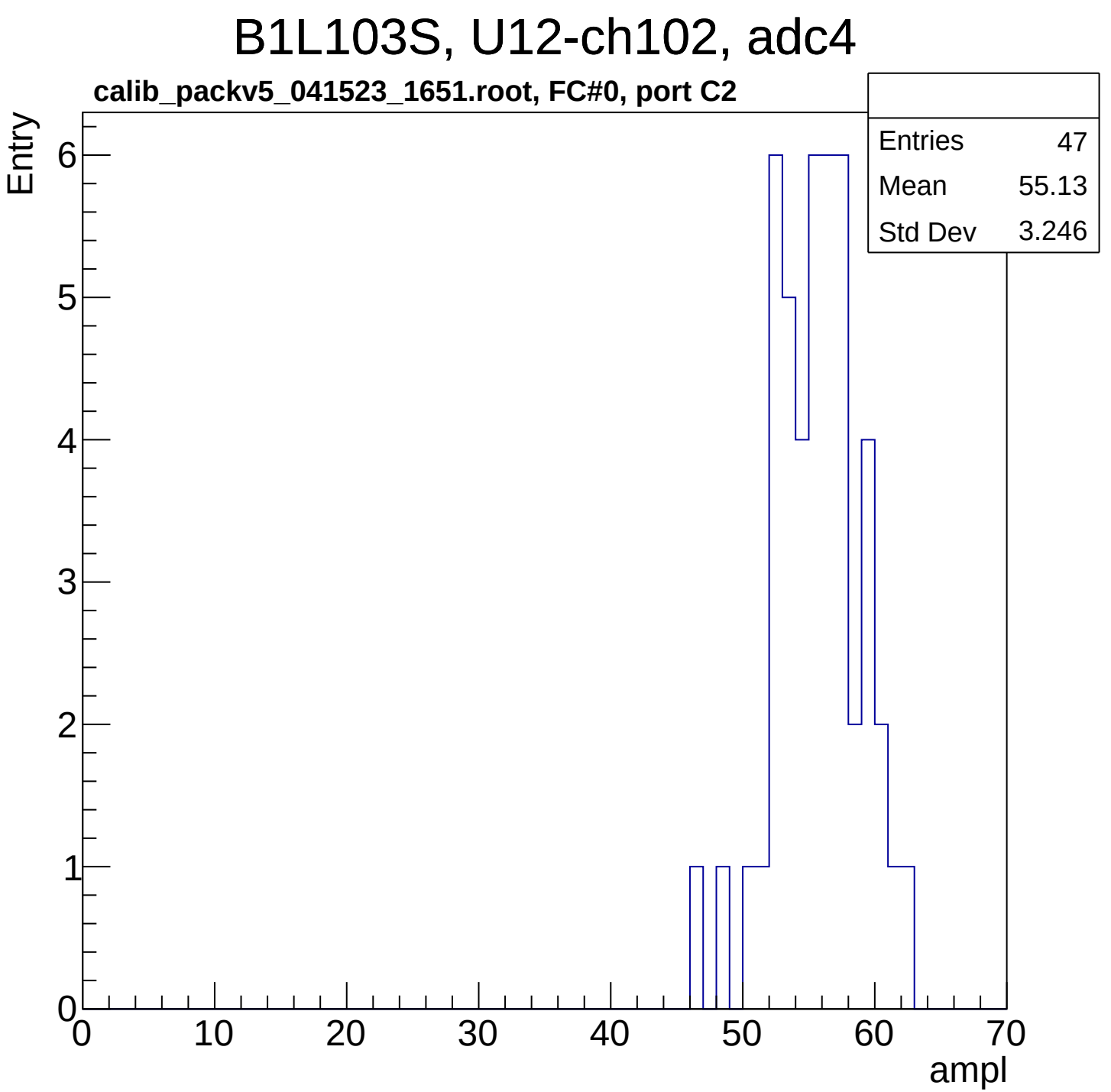
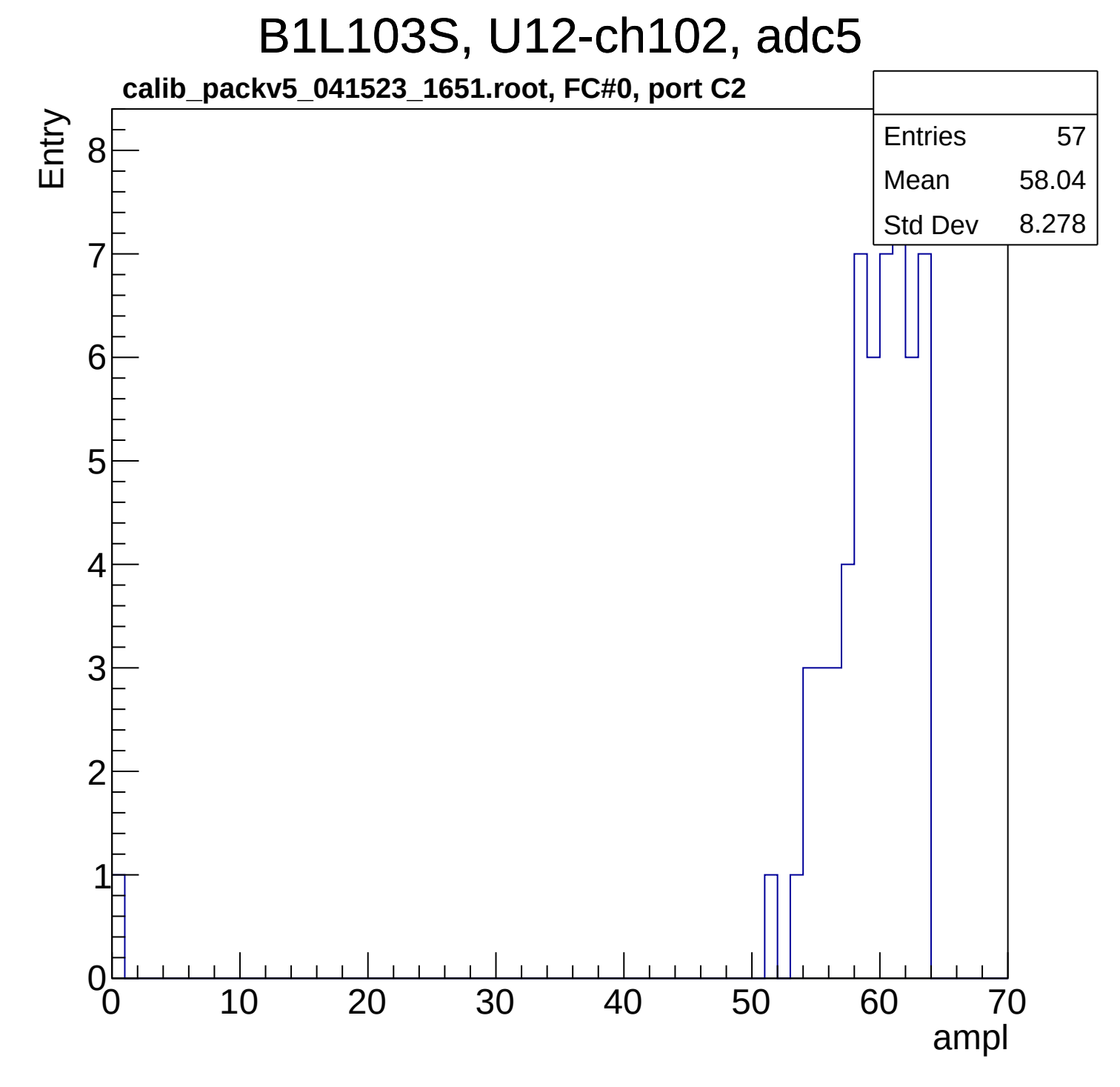

B1L103S, U12-ch102, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 55.13
Std Dev 3.246
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U12-ch102, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 58.04
Std Dev 8.278
Entry
ampl
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2
3
4
5
6
7
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0
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40
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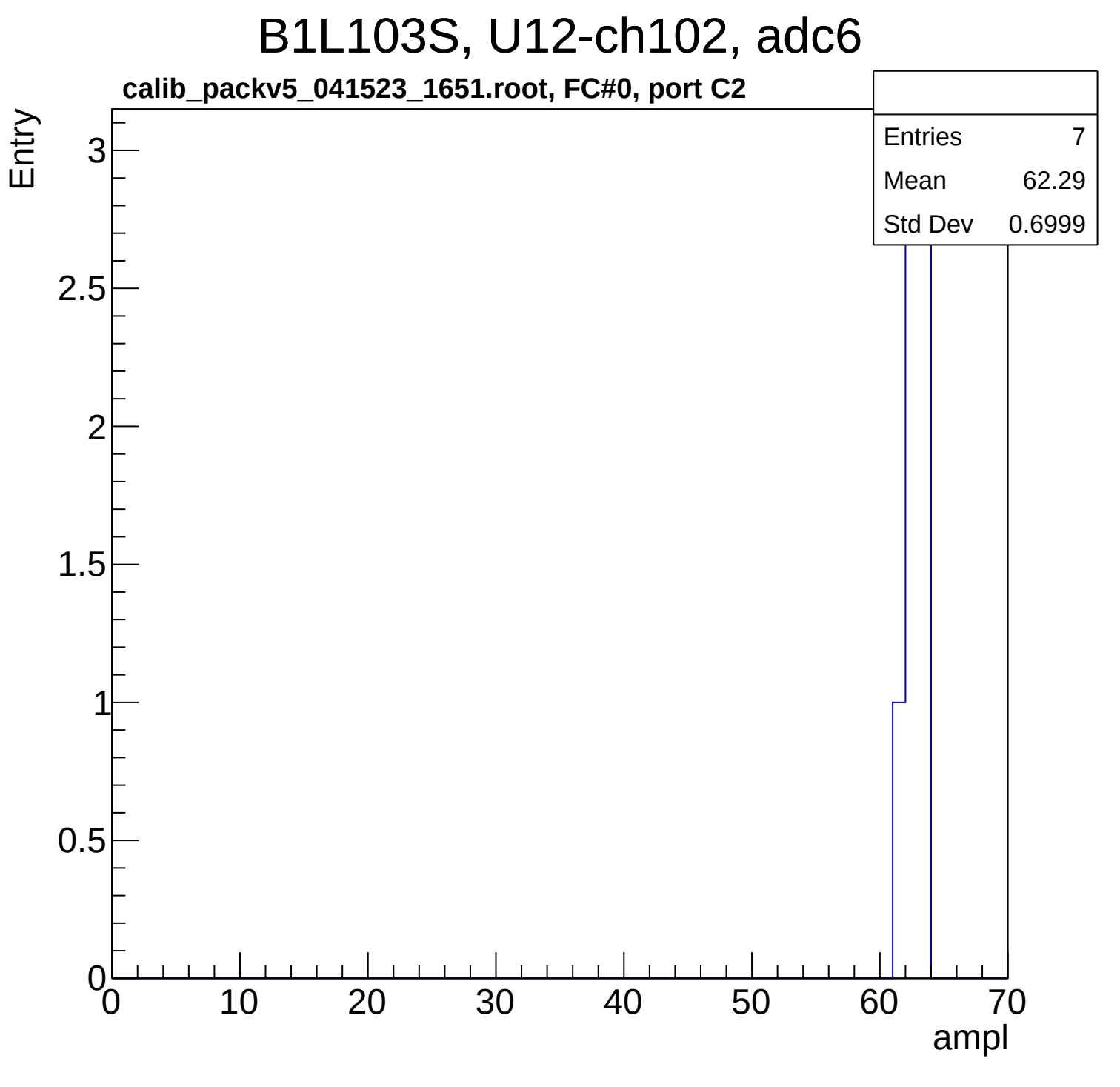
B1L103S, U12-ch102, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62.29
Std Dev 0.6999
Entry
ampl
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1
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0
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60
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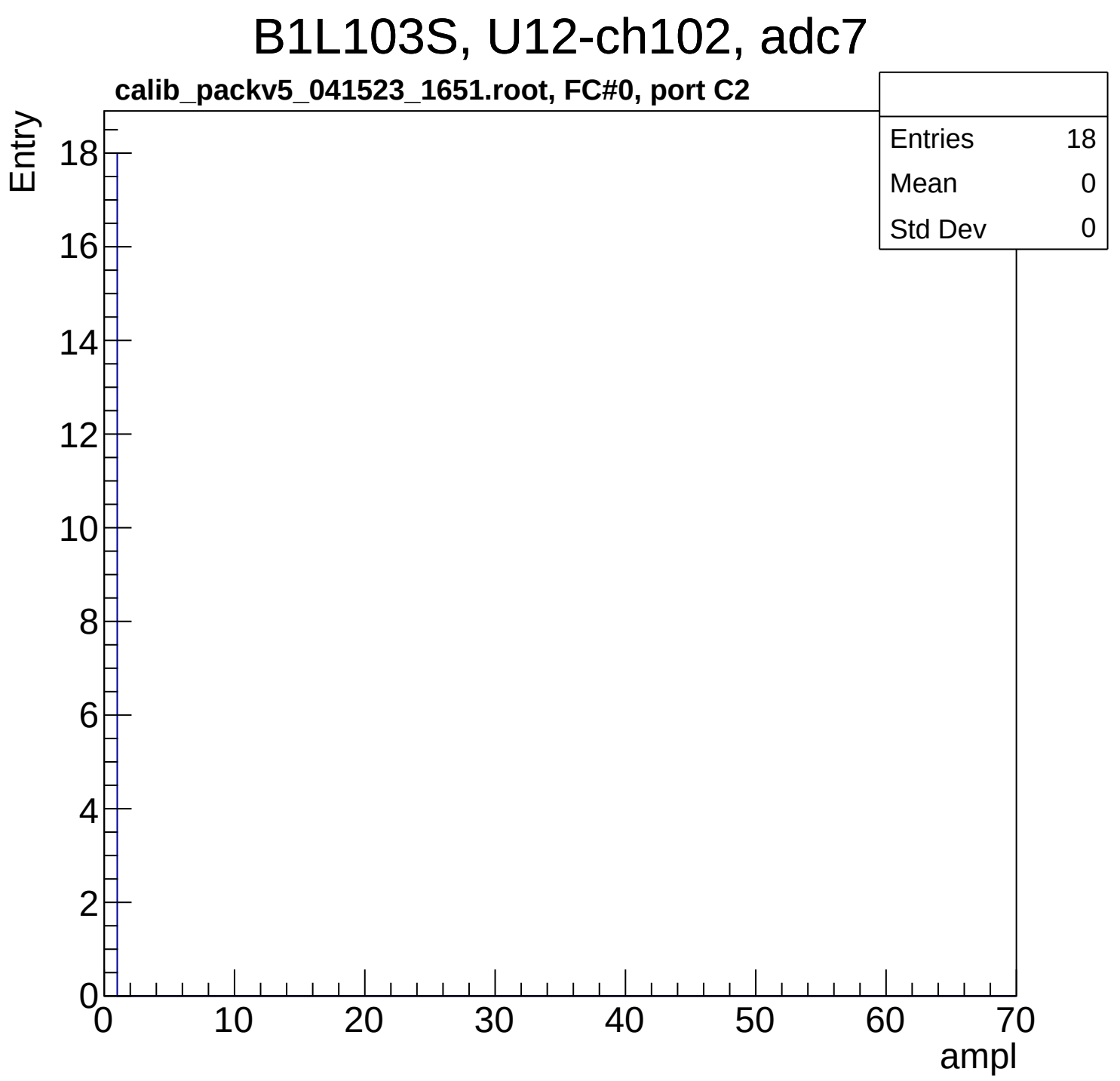
B1L103S, U12-ch102, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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14
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18
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10
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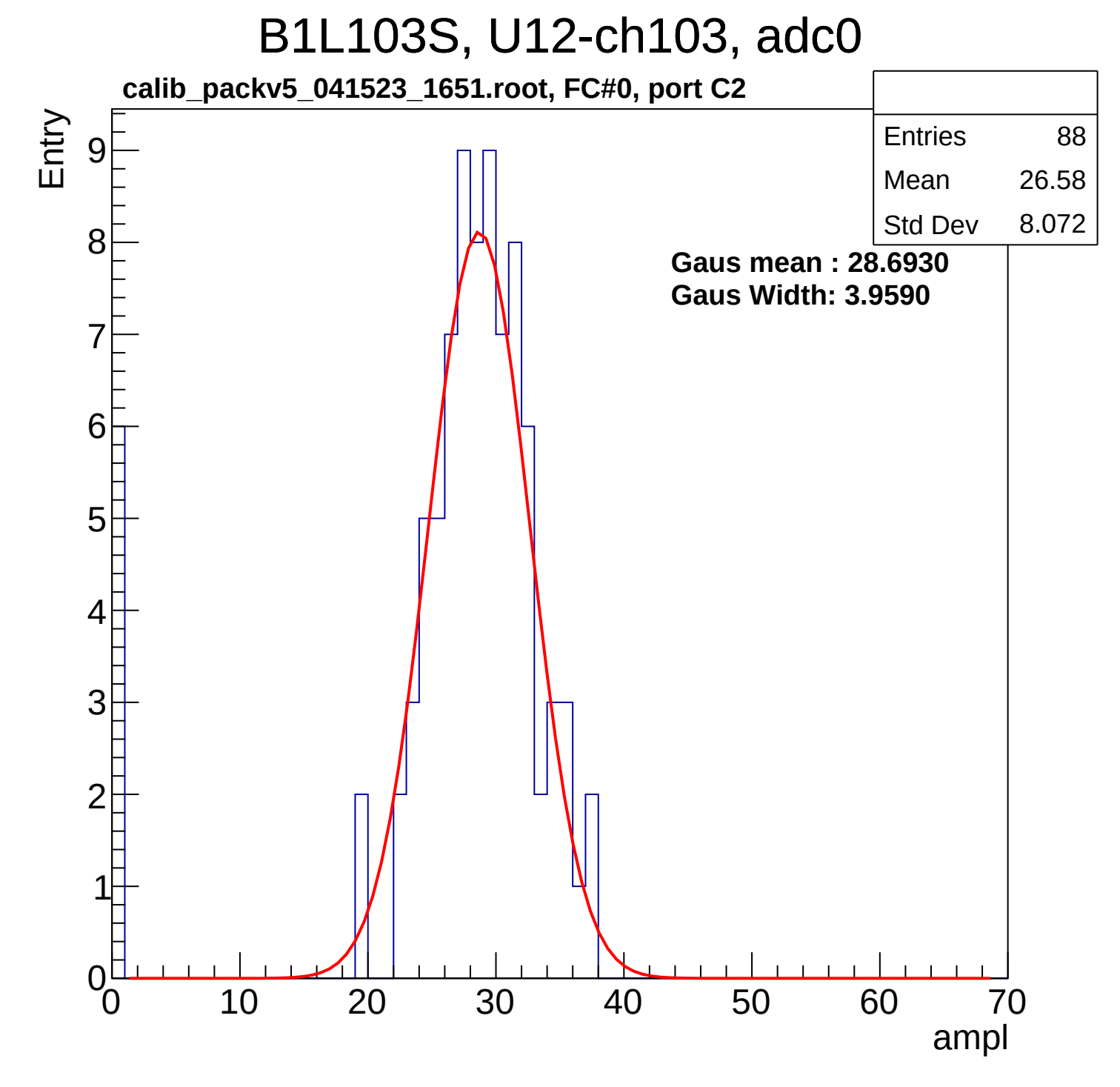
70
ampl


B1L103S, U12-ch103, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 88
Mean 26.58
Std Dev 8.072
Gaus mean : 28.6930
Gaus Width: 3.9590
Entry
ampl
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10
20
30
40
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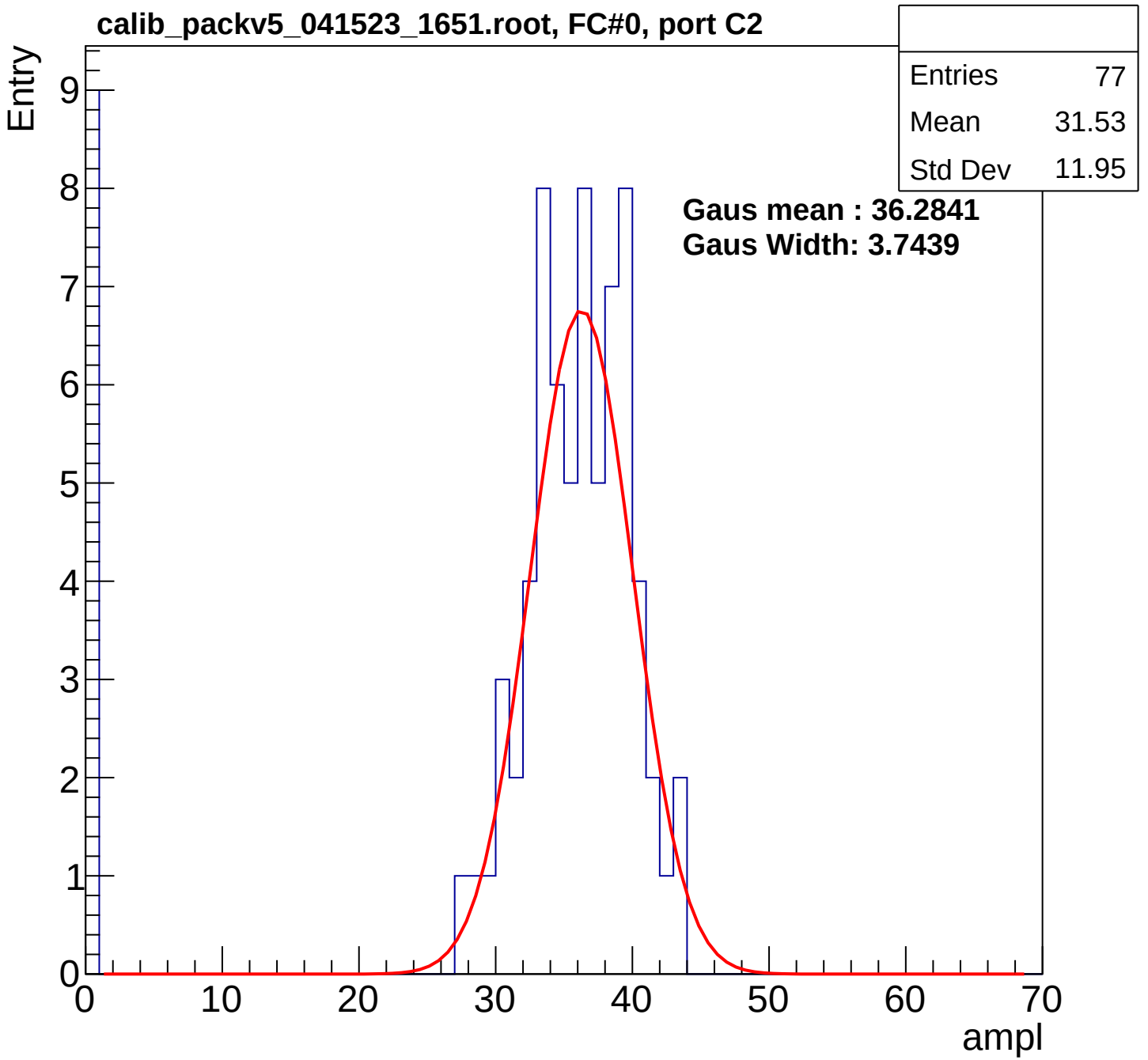
1
2
3
4
5
6
7
8
9


B1L103S, U12-ch103, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 31.53
Std Dev 11.95
Gaus mean : 36.2841
Gaus Width: 3.7439
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
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60
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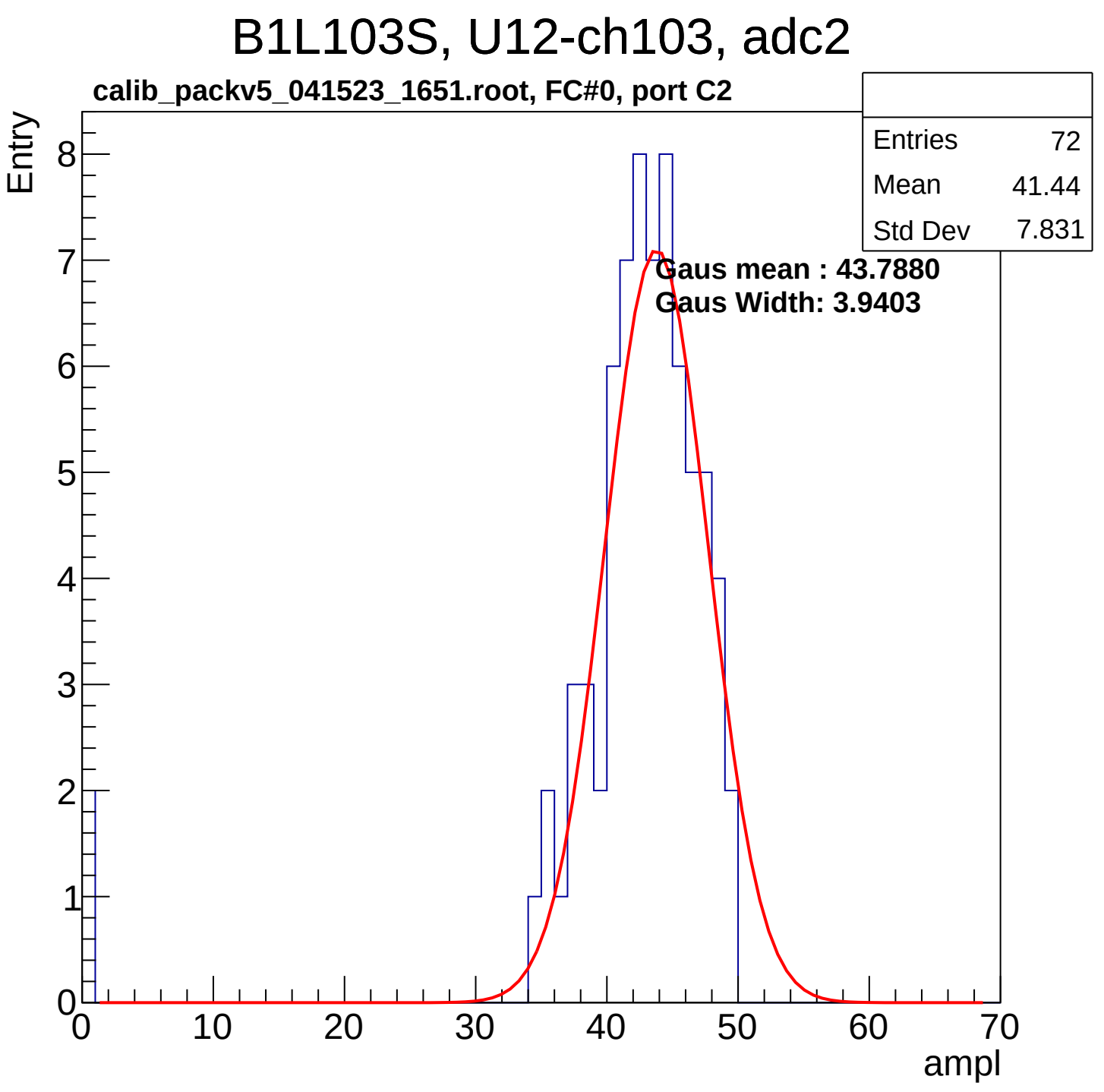
B1L103S, U12-ch103, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 41.44
Std Dev 7.831
Gaus mean : 43.7880
Gaus Width: 3.9403
Entry
ampl
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1
2
3
4
5
6
7
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0
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20
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40
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60
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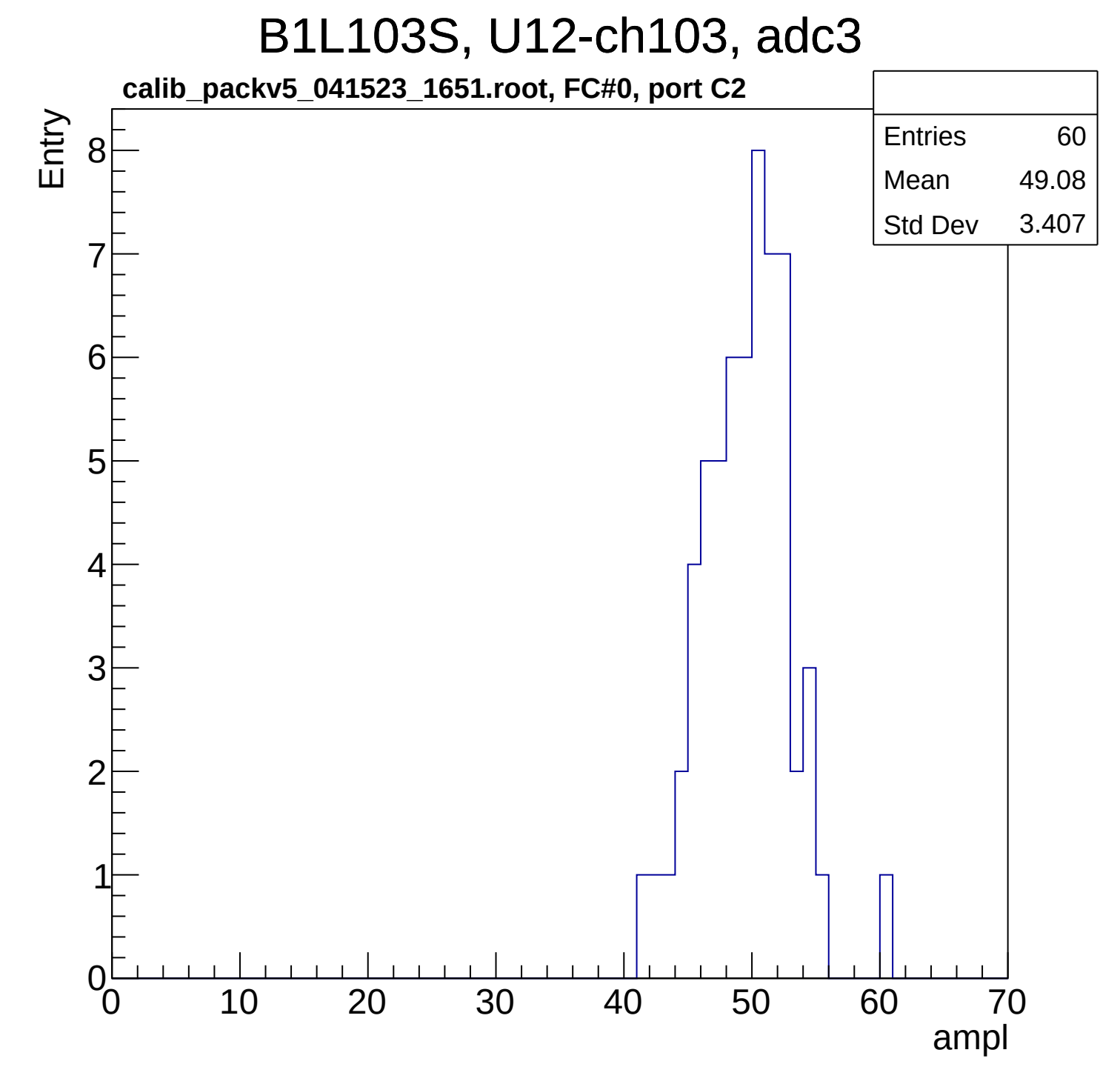
B1L103S, U12-ch103, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 49.08
Std Dev 3.407
Entry
ampl
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3
4
5
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0
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60
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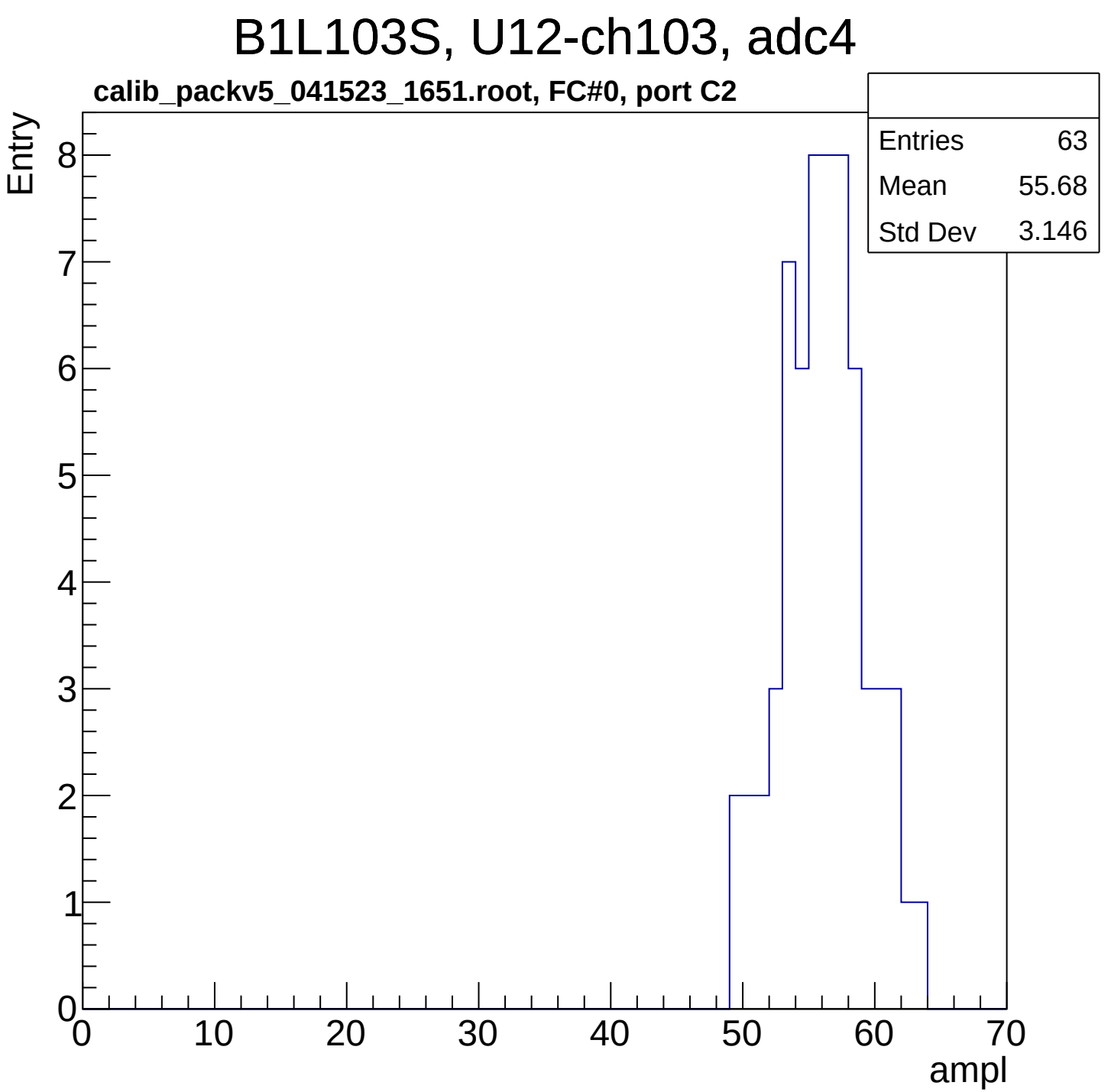
B1L103S, U12-ch103, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 55.68
Std Dev 3.146
Entry
ampl
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6
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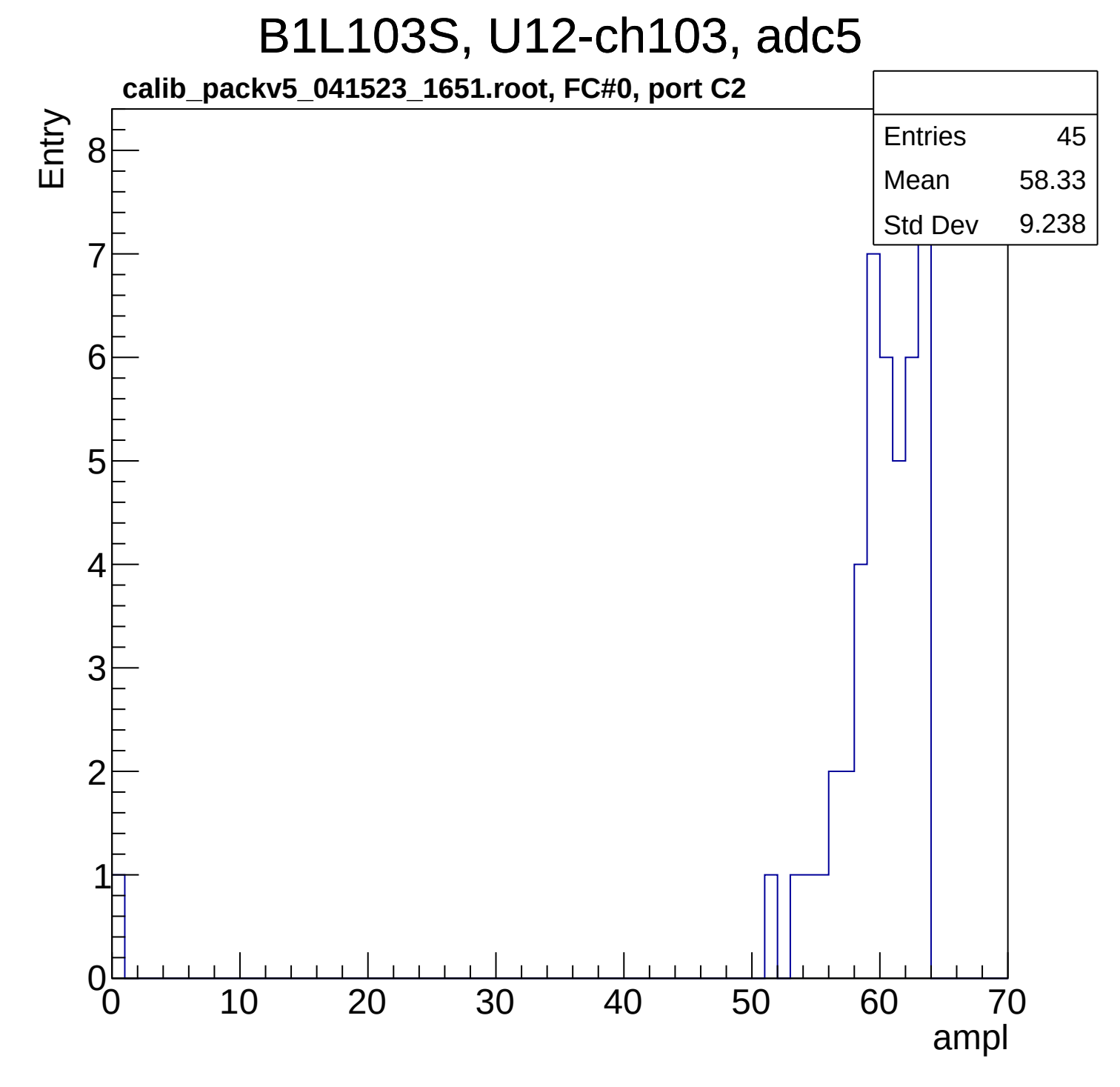
B1L103S, U12-ch103, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 58.33
Std Dev 9.238
Entry
ampl
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1
2
3
4
5
6
7
8
0
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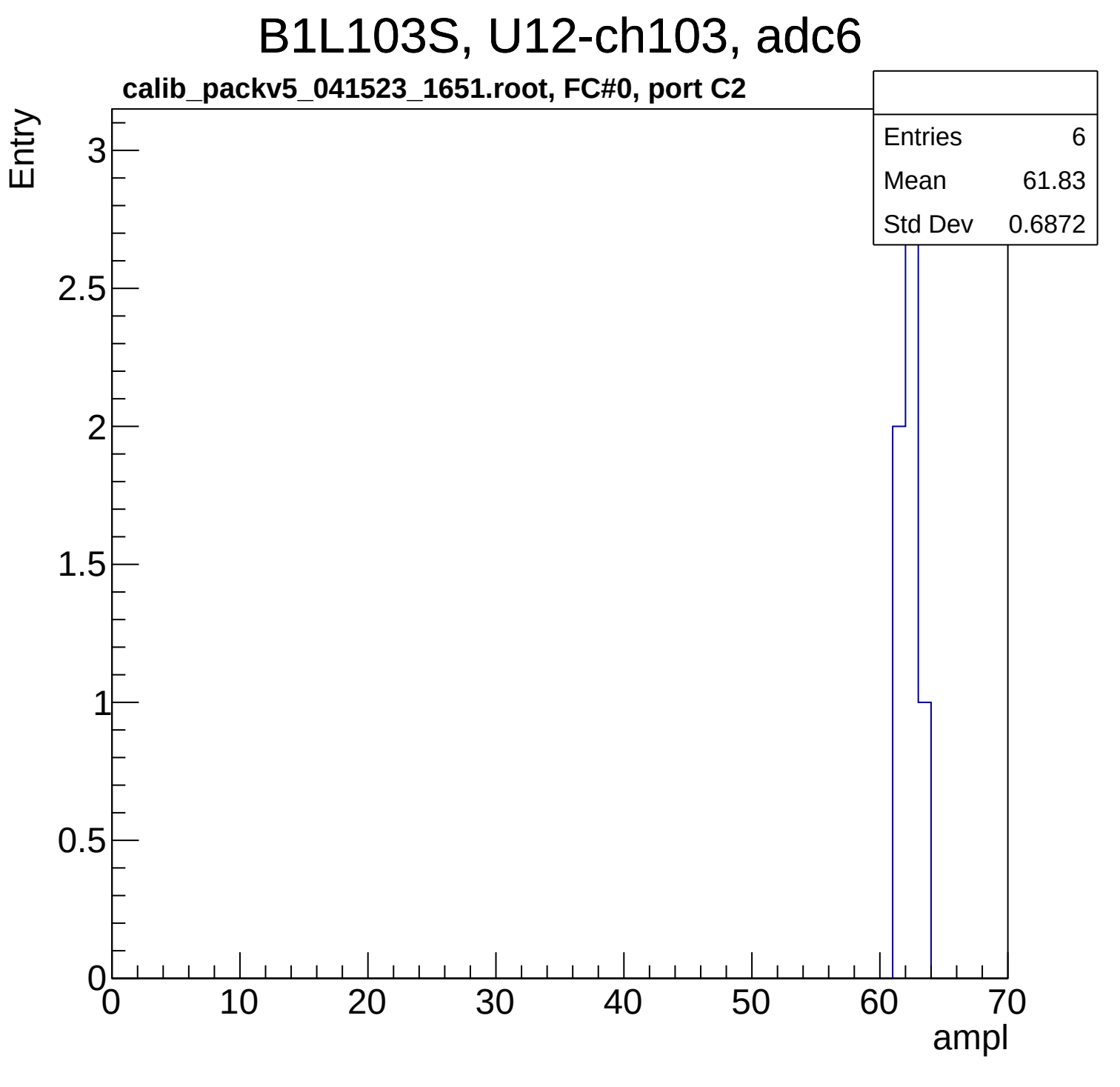
B1L103S, U12-ch103, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.83
Std Dev 0.6872
Entry
ampl
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0.5
1
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2.5
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0
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20
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60
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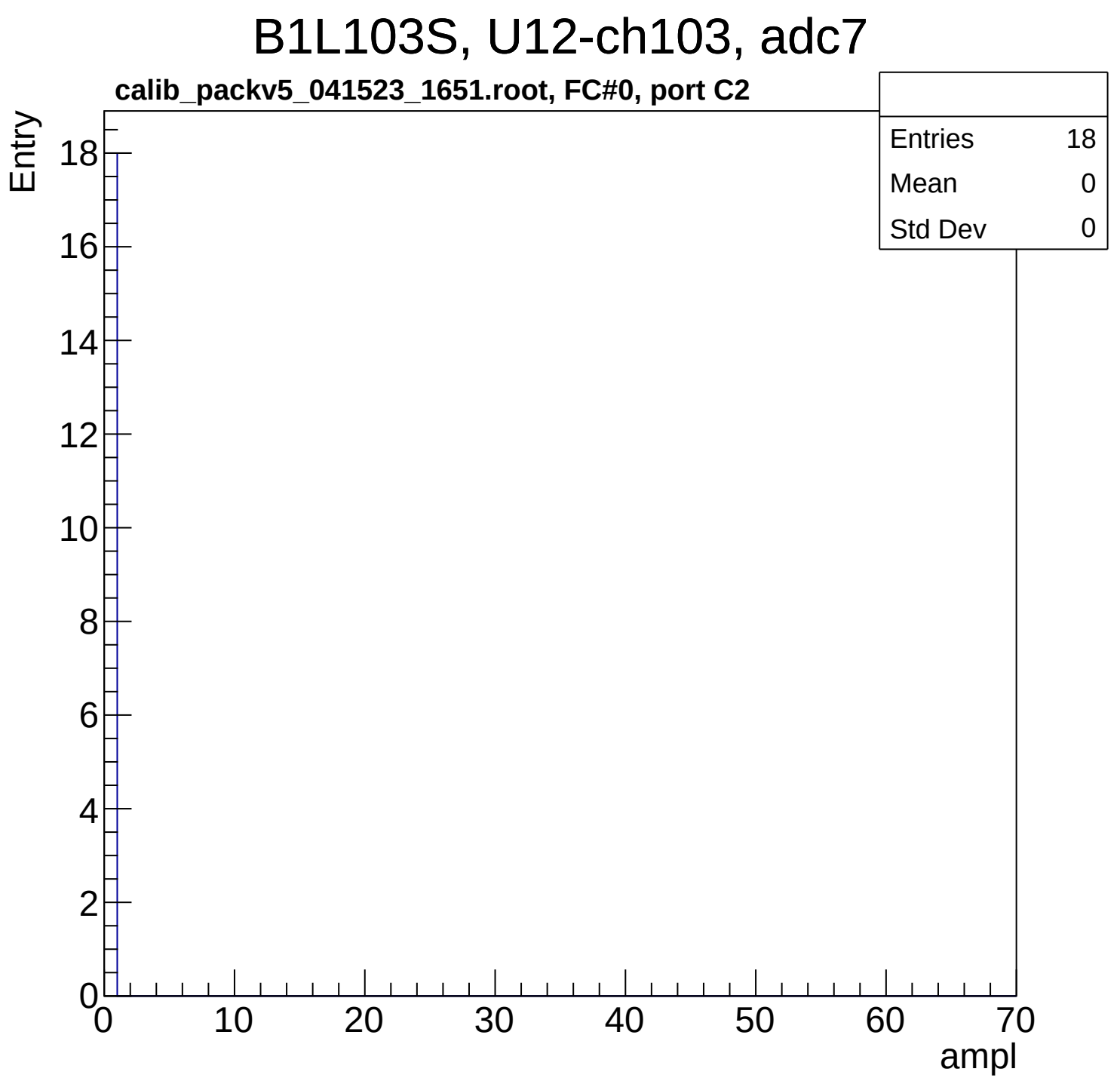
B1L103S, U12-ch103, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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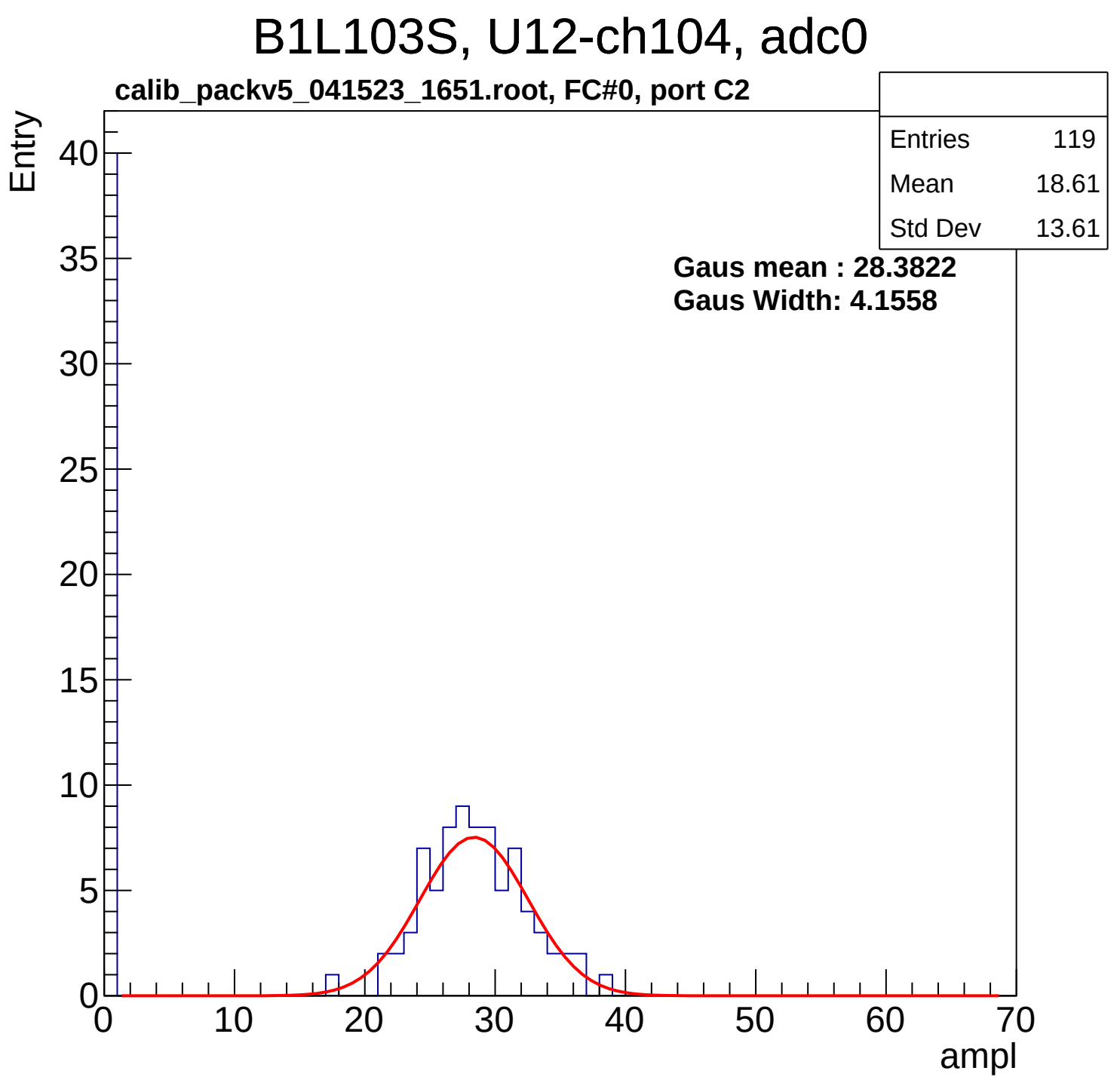
50
60
70
ampl


B1L103S, U12-ch104, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 119
Mean 18.61
Std Dev 13.61
Gaus mean : 28.3822
Gaus Width: 4.1558
Entry
ampl
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5
10
15
20
25
30
35
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0
10
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40
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60
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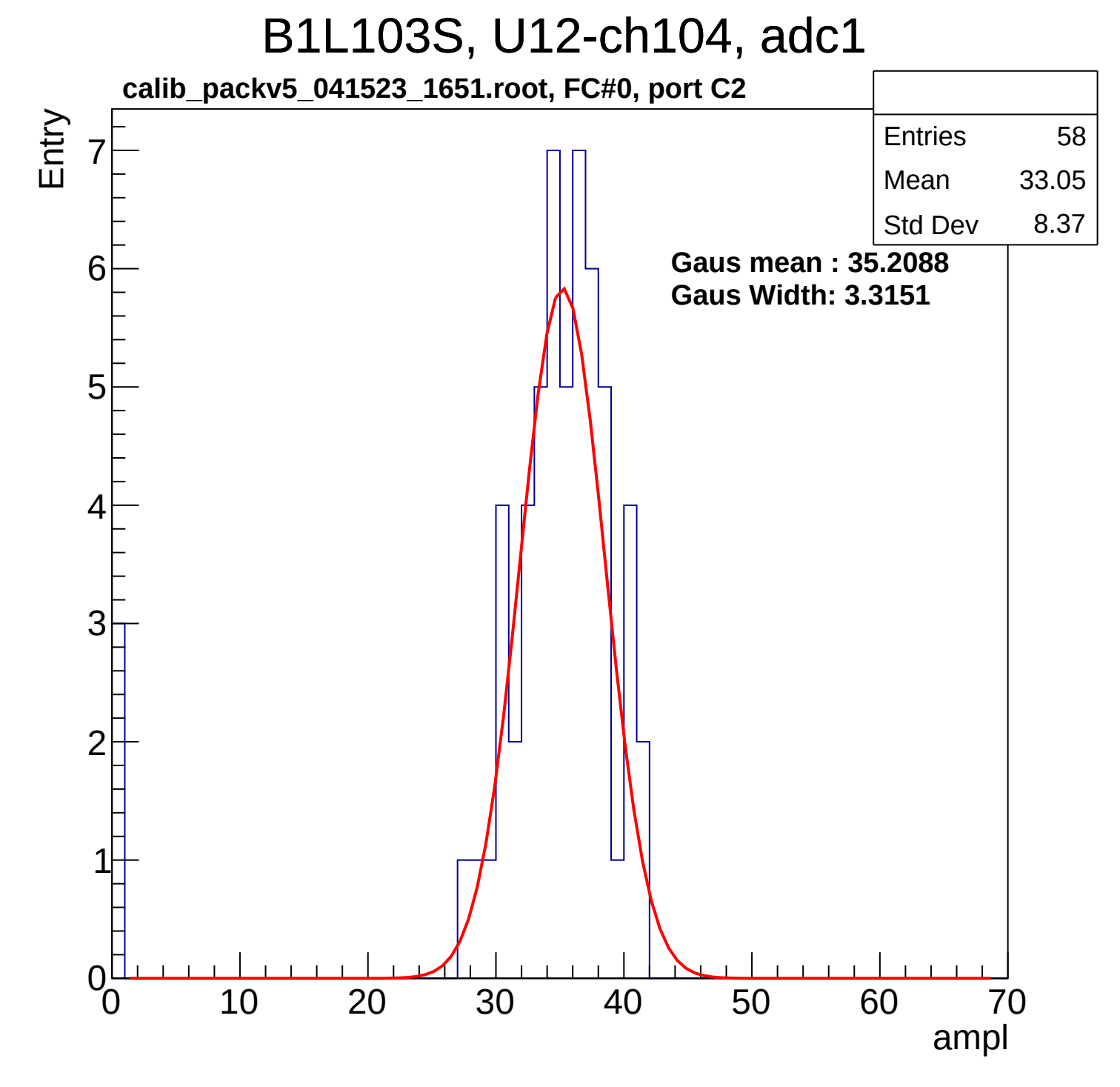
B1L103S, U12-ch104, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 33.05
Std Dev 8.37
Gaus mean : 35.2088
Gaus Width: 3.3151
Entry
ampl
0
1
2
3
4
5
6
7
0
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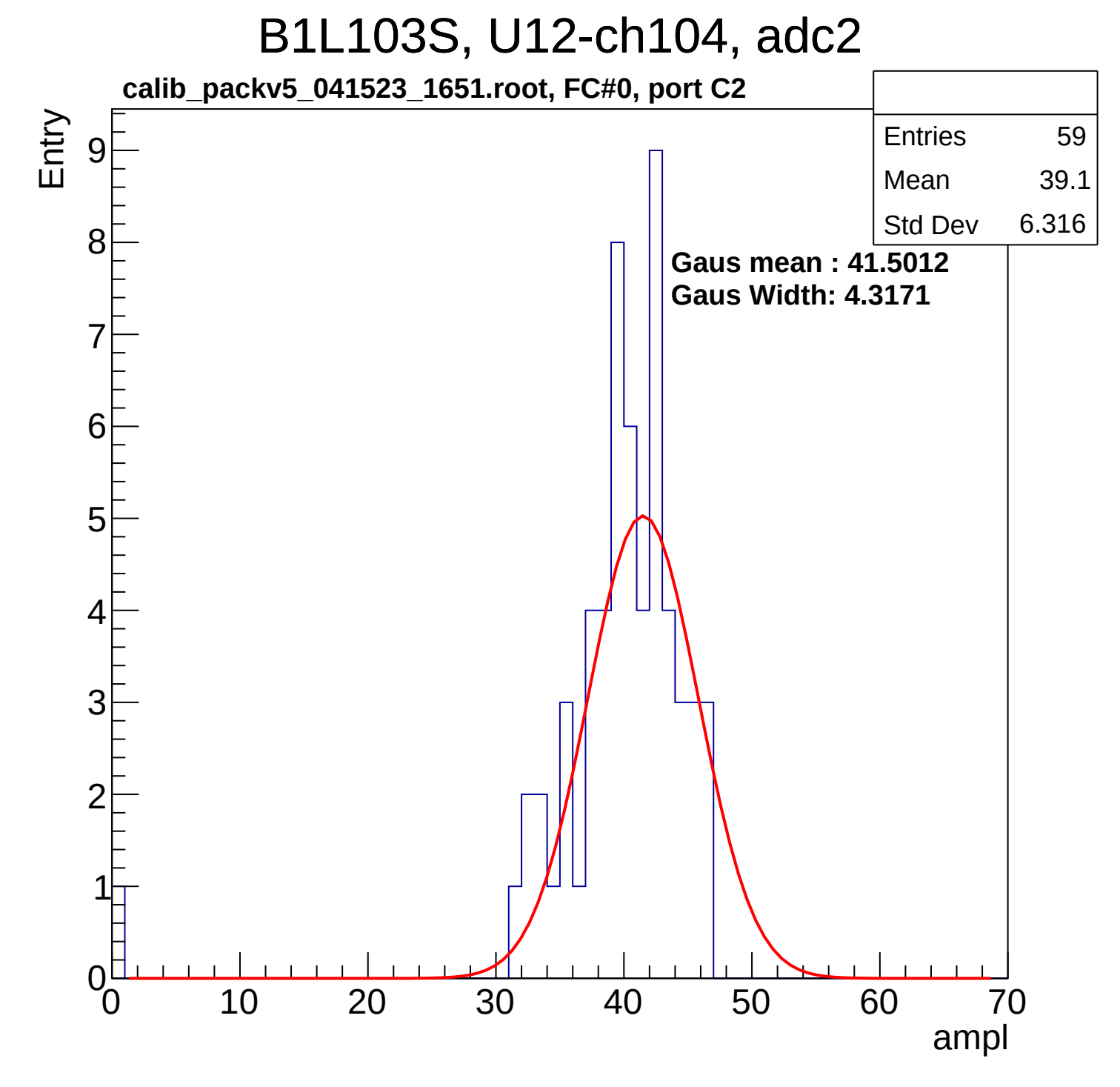
B1L103S, U12-ch104, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 39.1
Std Dev 6.316
Gaus mean : 41.5012
Gaus Width: 4.3171
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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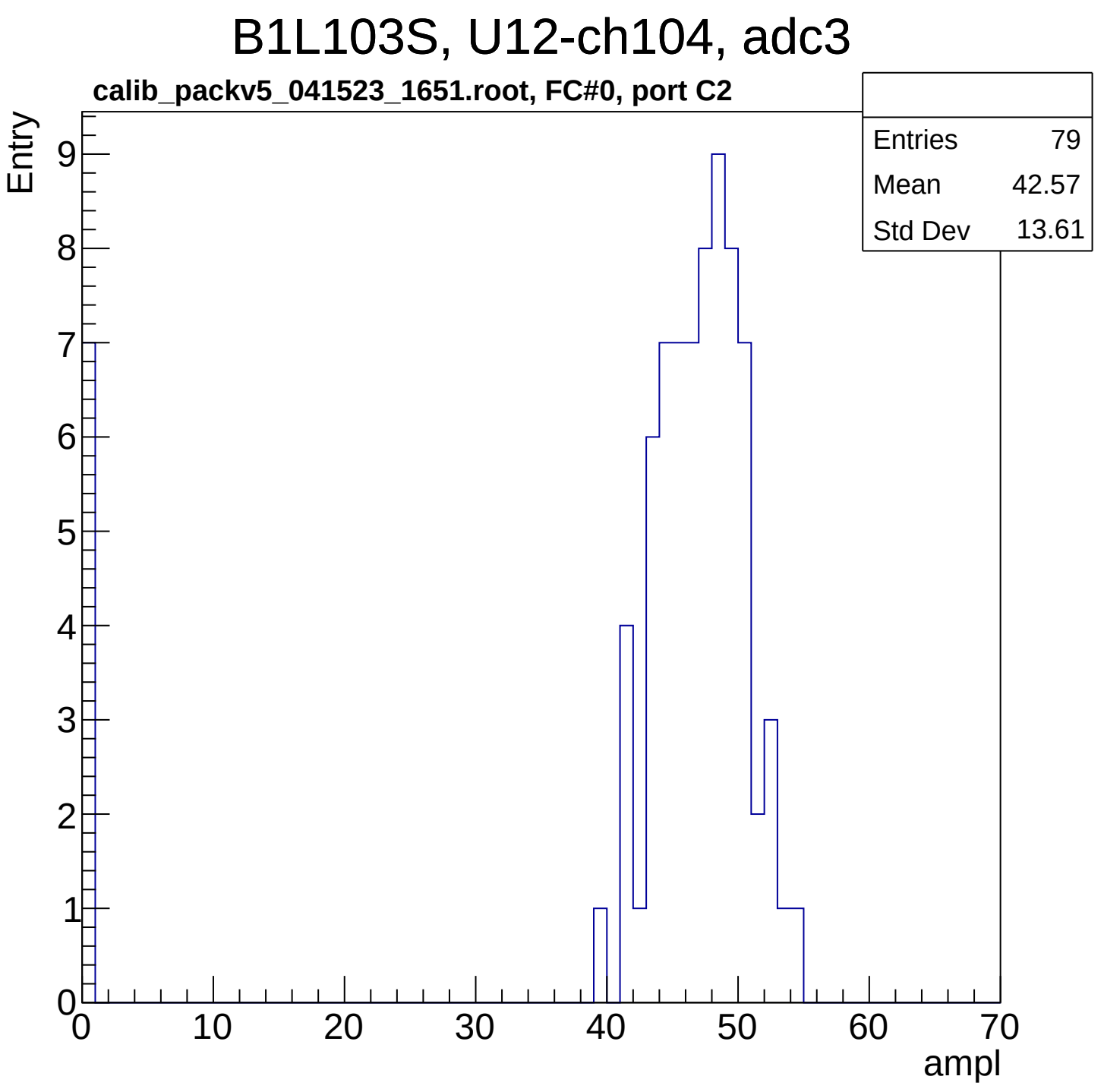
B1L103S, U12-ch104, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 42.57
Std Dev 13.61
Entry
ampl
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3
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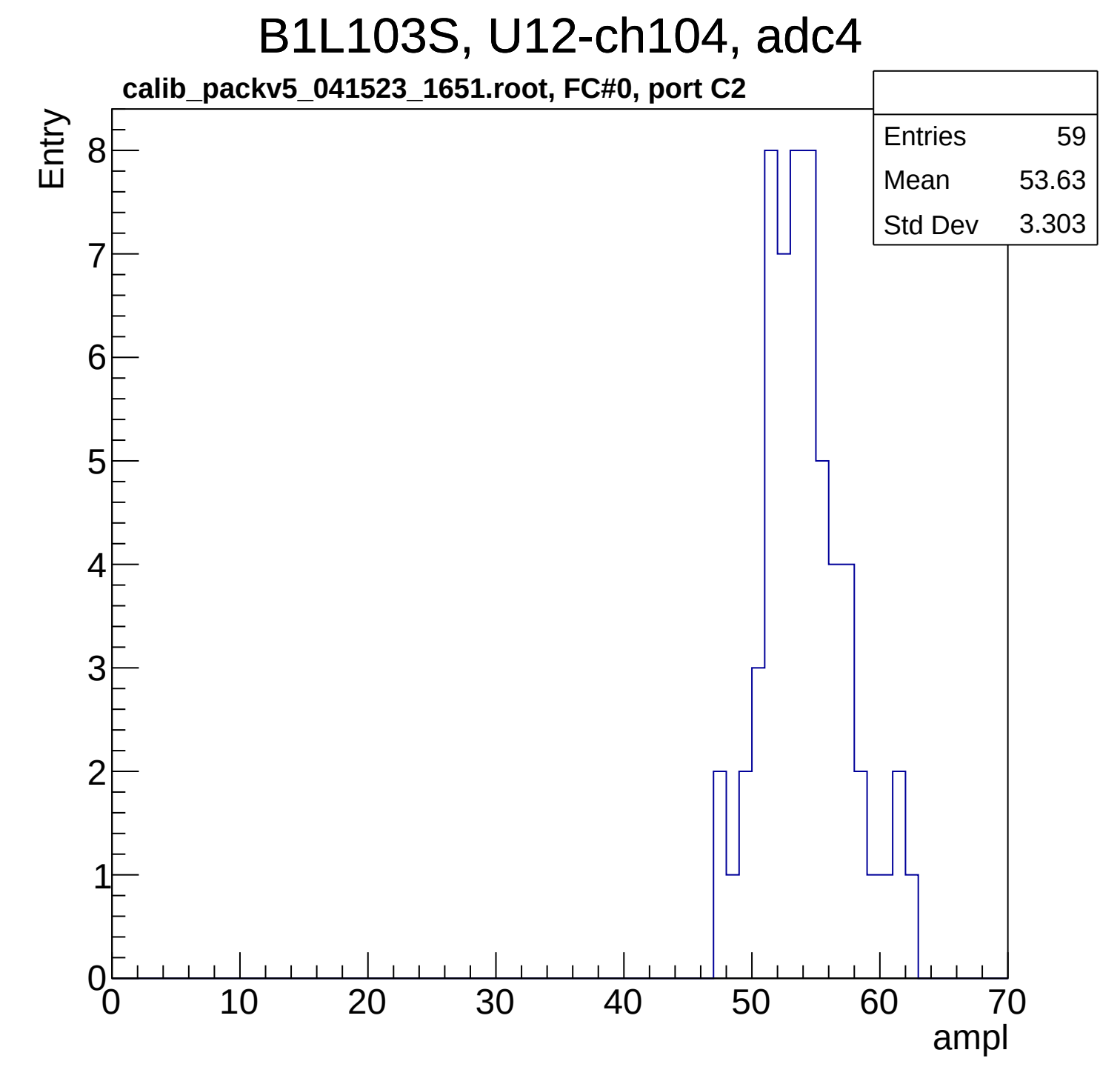
B1L103S, U12-ch104, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 53.63
Std Dev 3.303
Entry
ampl
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5
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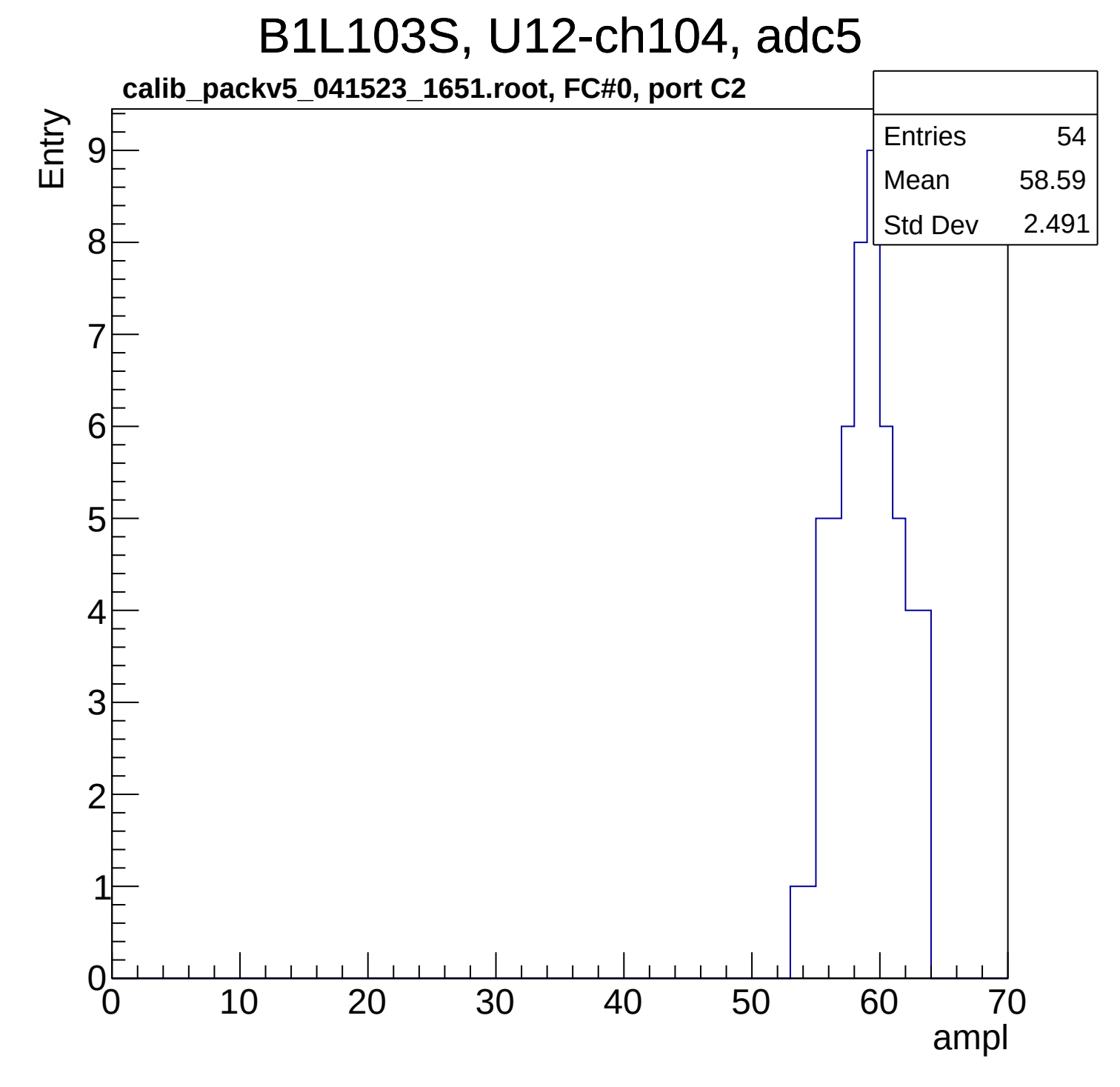
B1L103S, U12-ch104, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.59
Std Dev 2.491
Entry
ampl
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6
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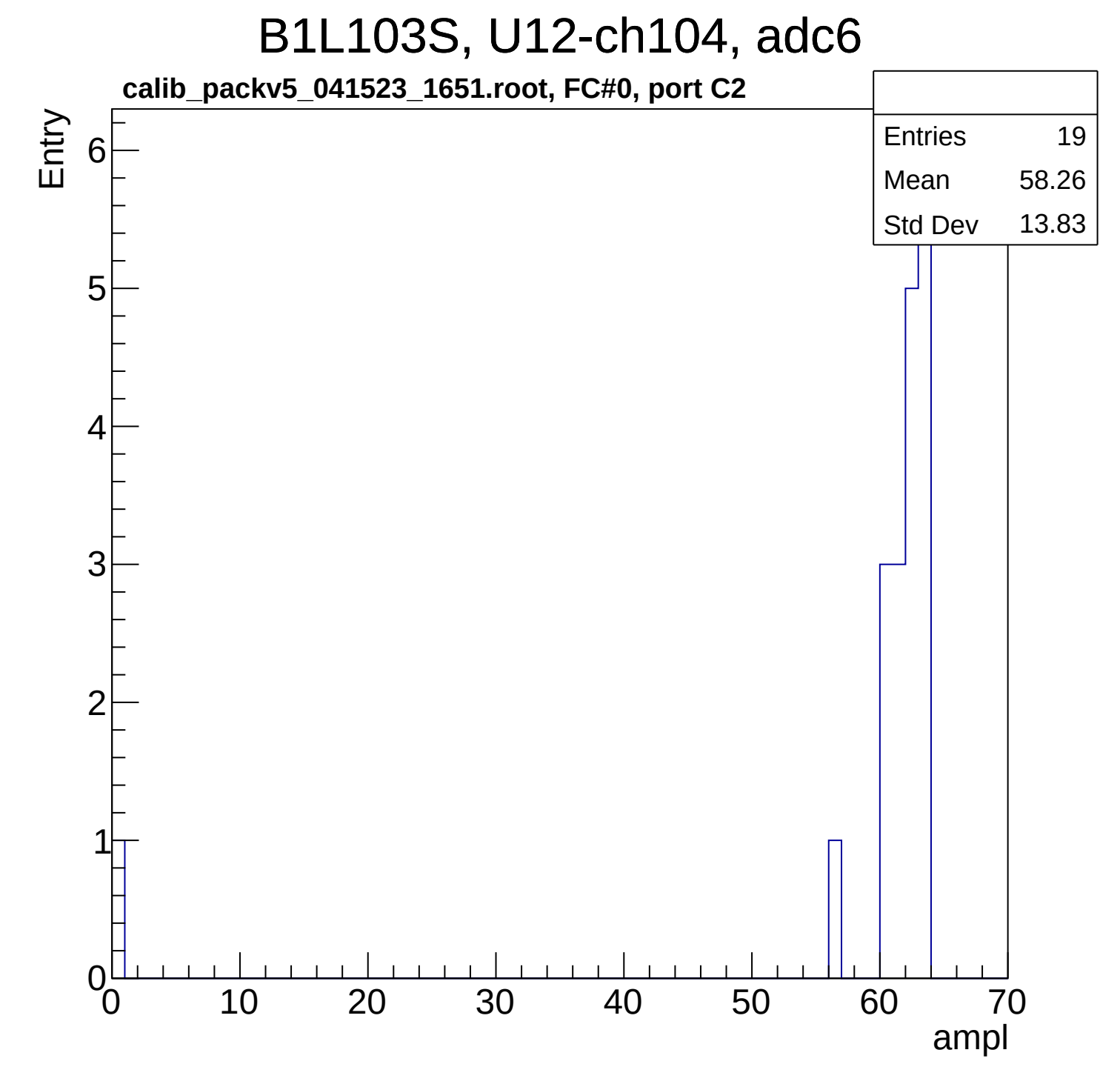
B1L103S, U12-ch104, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 58.26
Std Dev 13.83
Entry
ampl
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2
3
4
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0
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60
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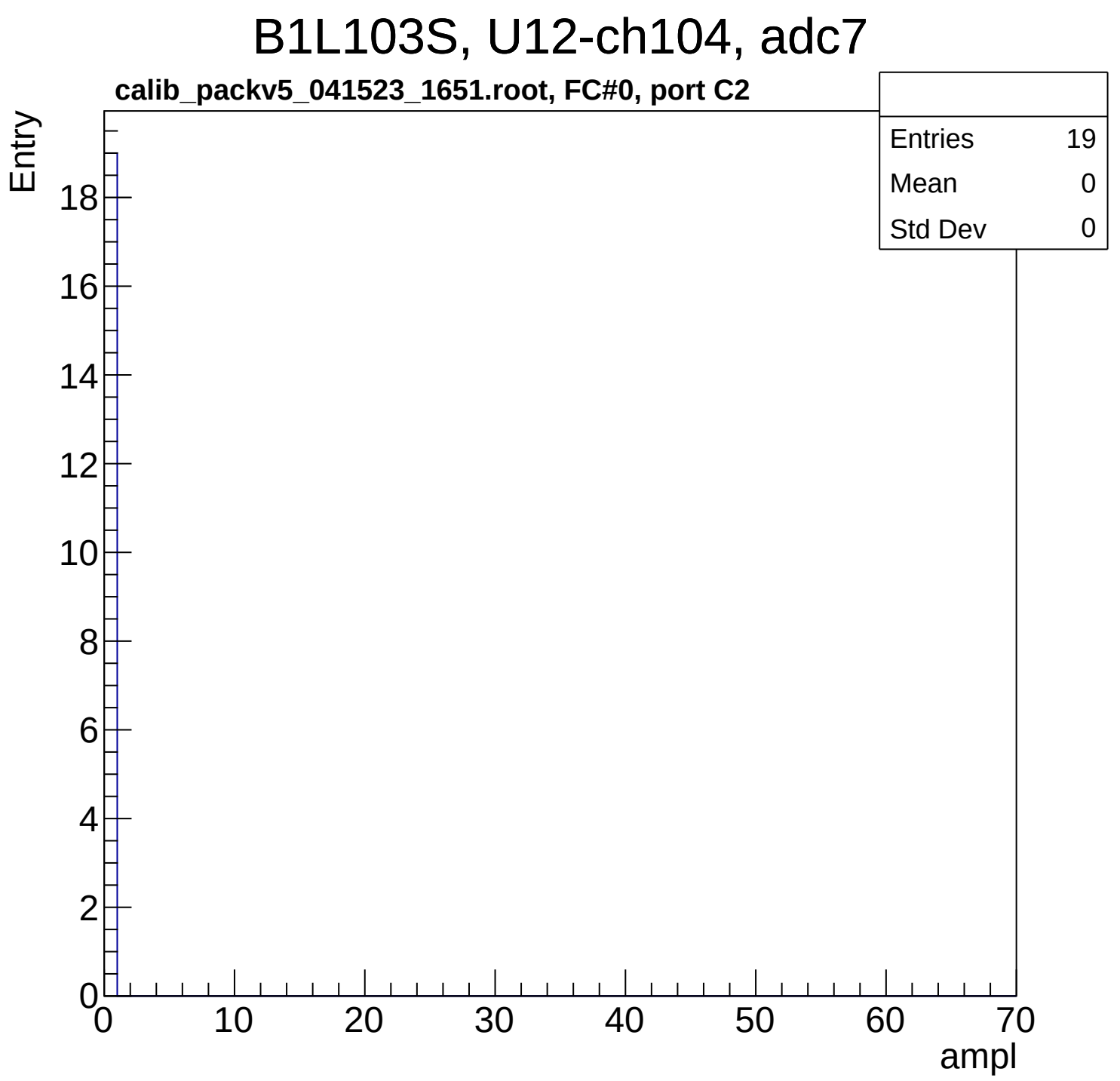
B1L103S, U12-ch104, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
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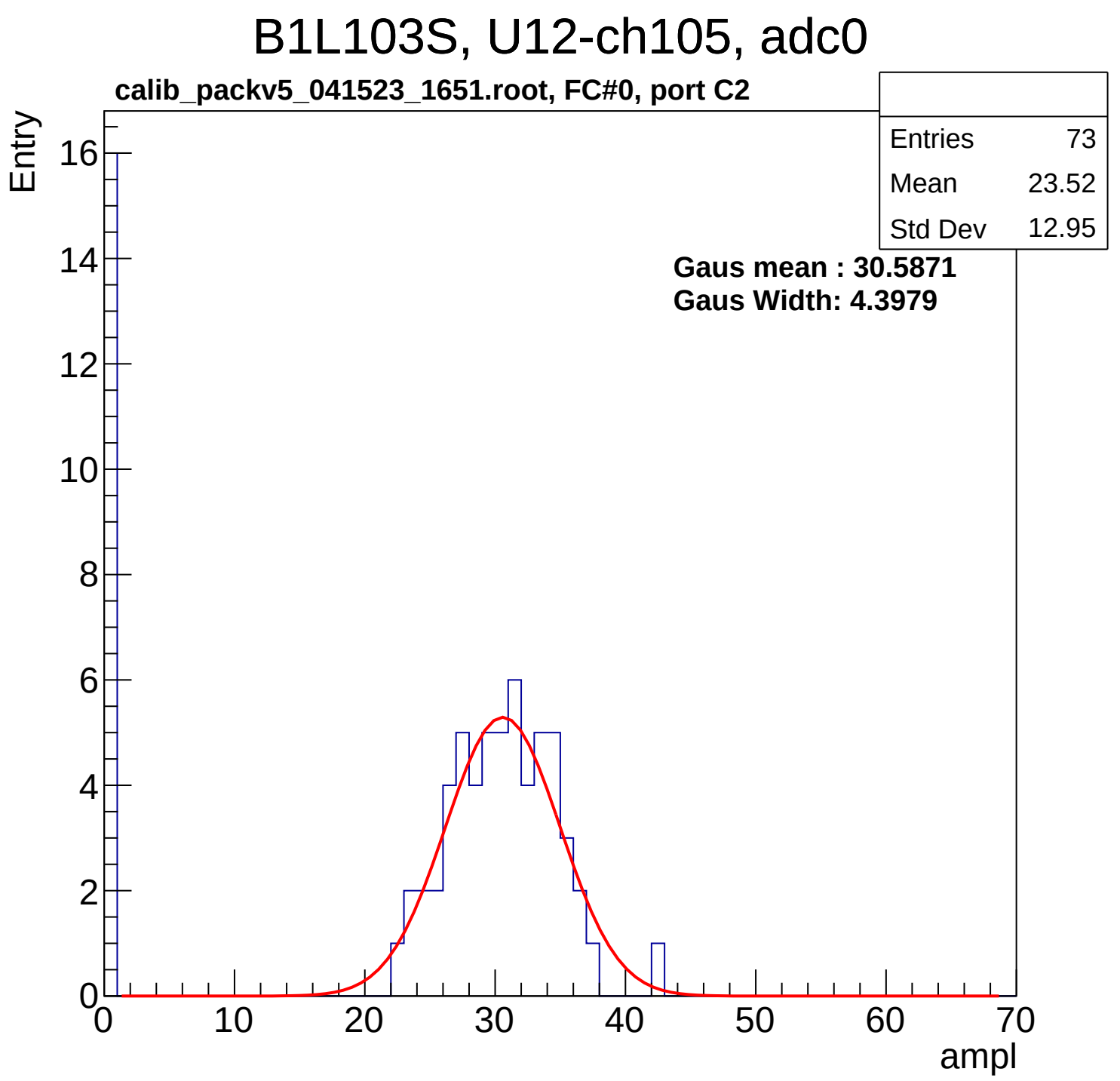
50
60
70
ampl


B1L103S, U12-ch105, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 23.52
Std Dev 12.95
Gaus mean : 30.5871
Gaus Width: 4.3979
Entry
ampl
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2
4
6
8
10
12
14
16
0
10
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40
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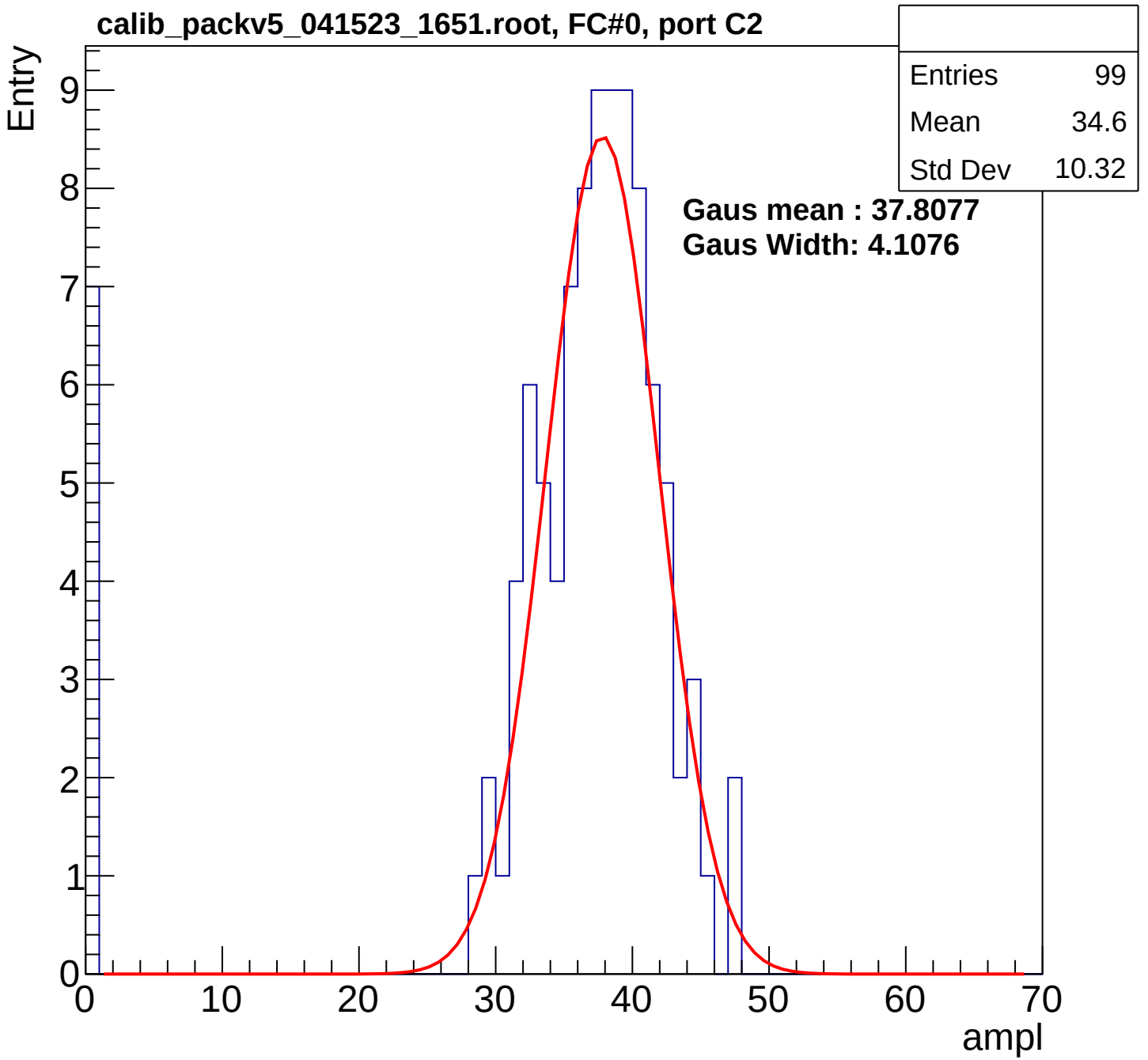
B1L103S, U12-ch105, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 34.6
Std Dev 10.32
Gaus mean : 37.8077
Gaus Width: 4.1076
Entry
ampl
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2
3
4
5
6
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0
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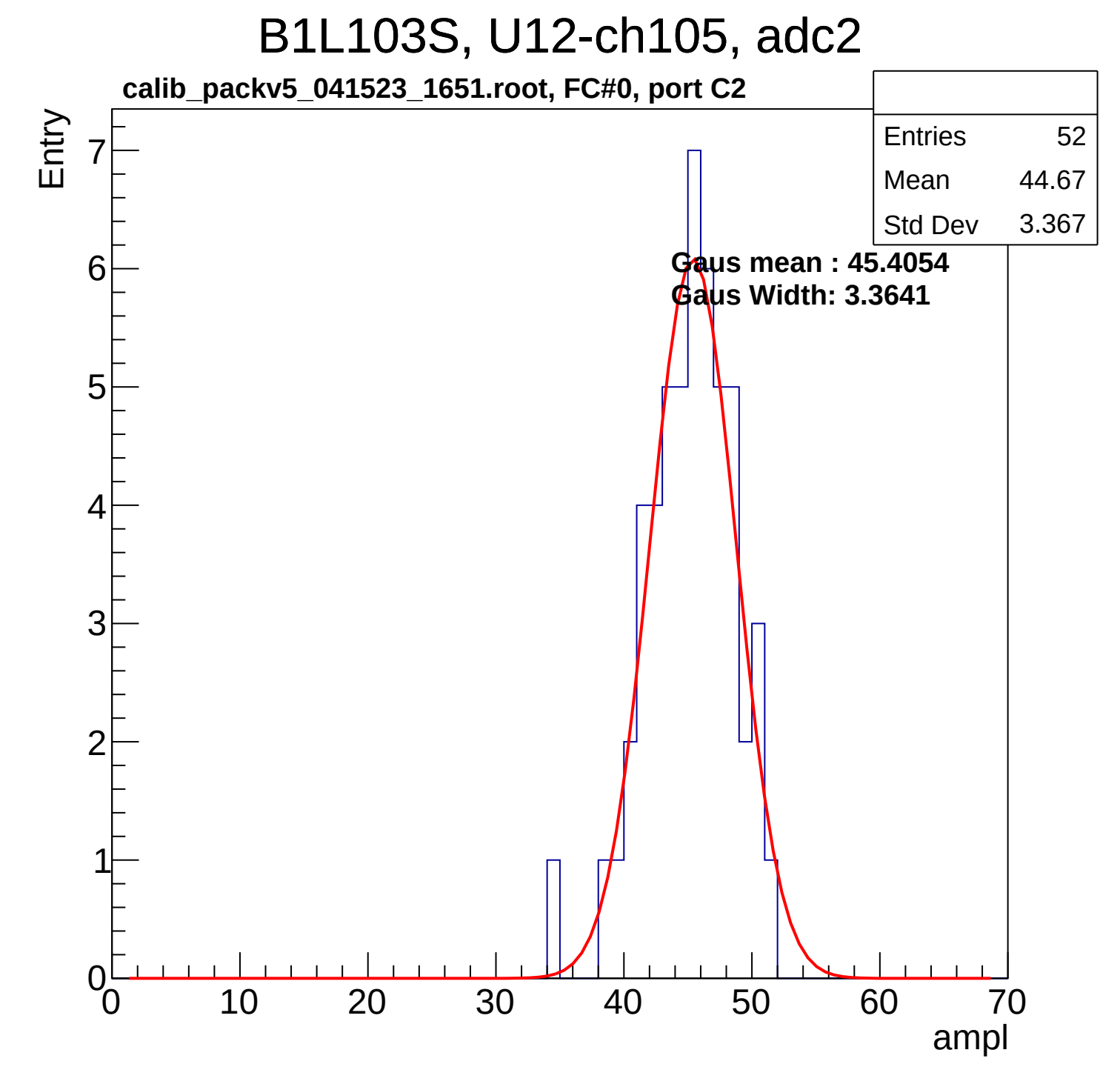
B1L103S, U12-ch105, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 44.67
Std Dev 3.367
Gaus mean : 45.4054
Gaus Width: 3.3641
Entry
ampl
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1
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3
4
5
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0
10
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60
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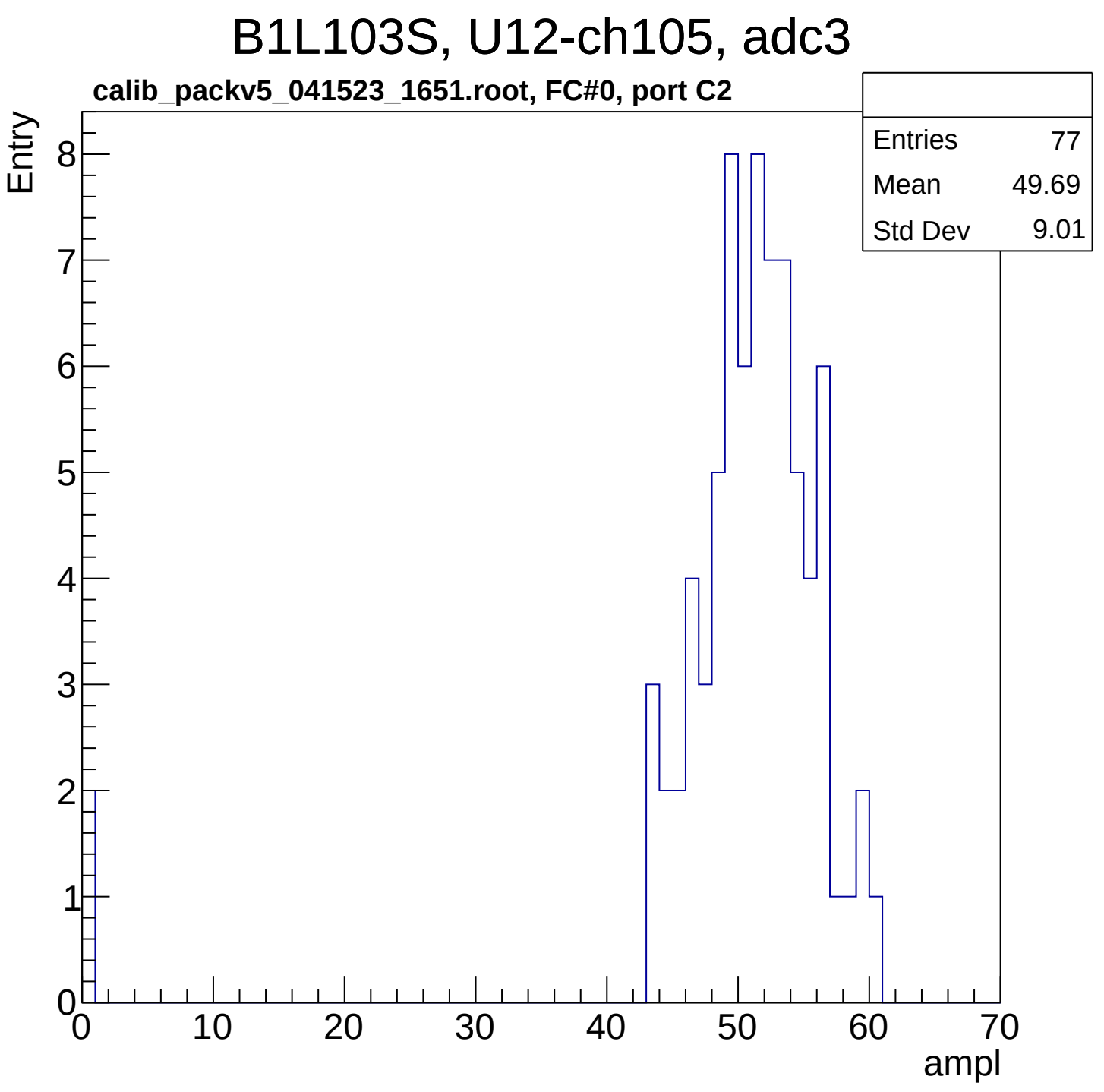
B1L103S, U12-ch105, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 49.69
Std Dev 9.01
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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60
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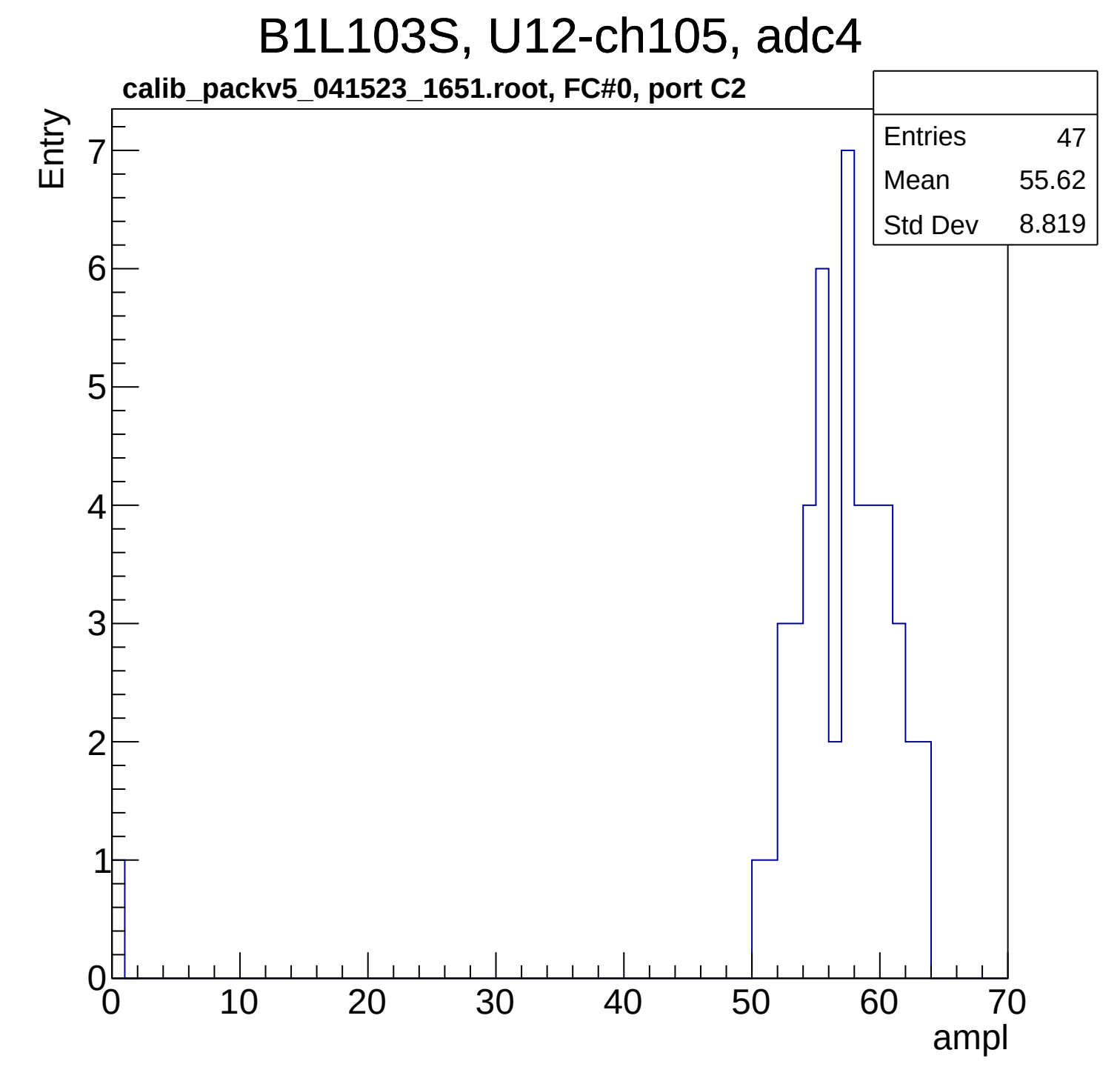
B1L103S, U12-ch105, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 55.62
Std Dev 8.819
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
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60
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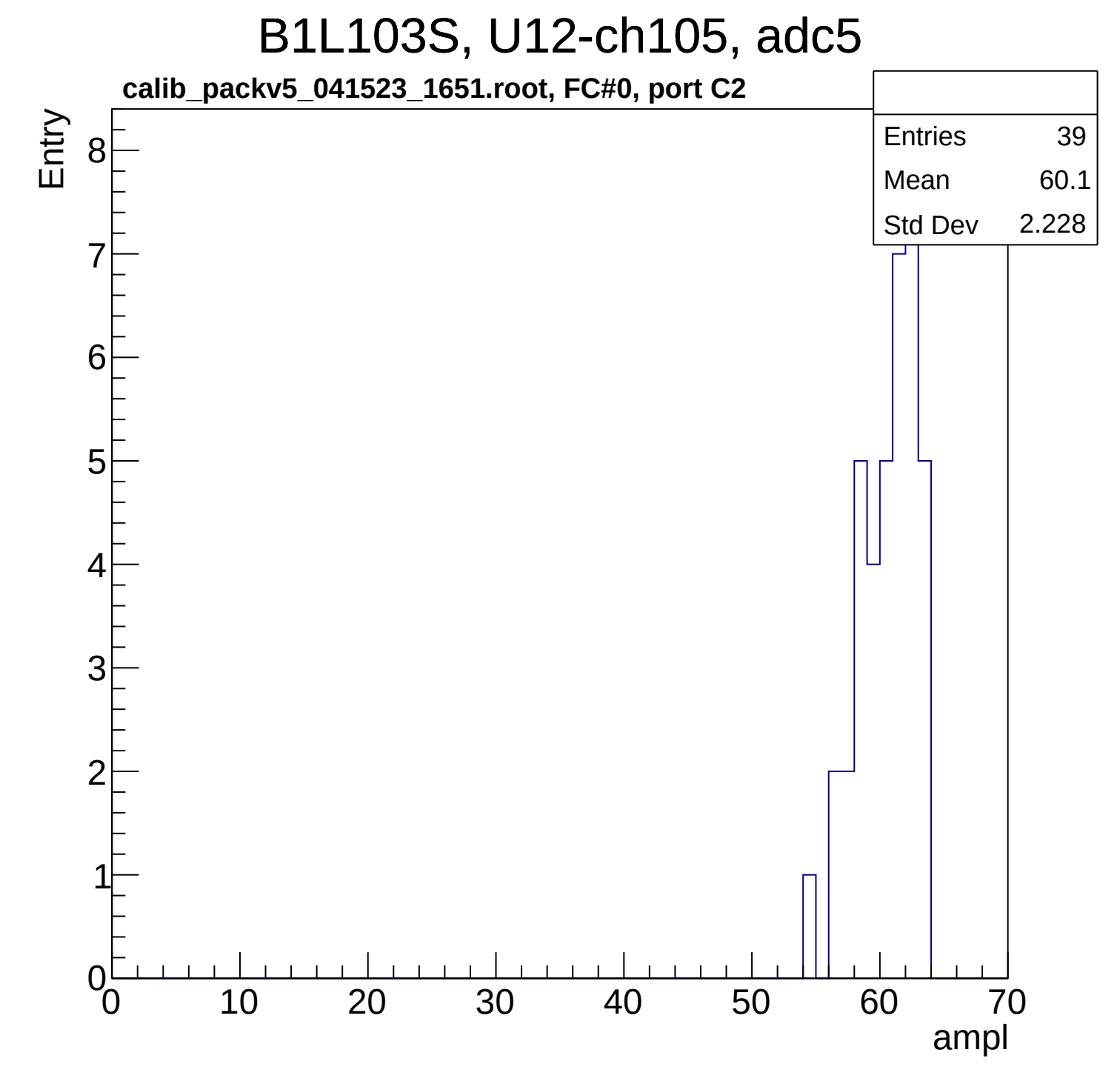
B1L103S, U12-ch105, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 60.1
Std Dev 2.228
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
50
60
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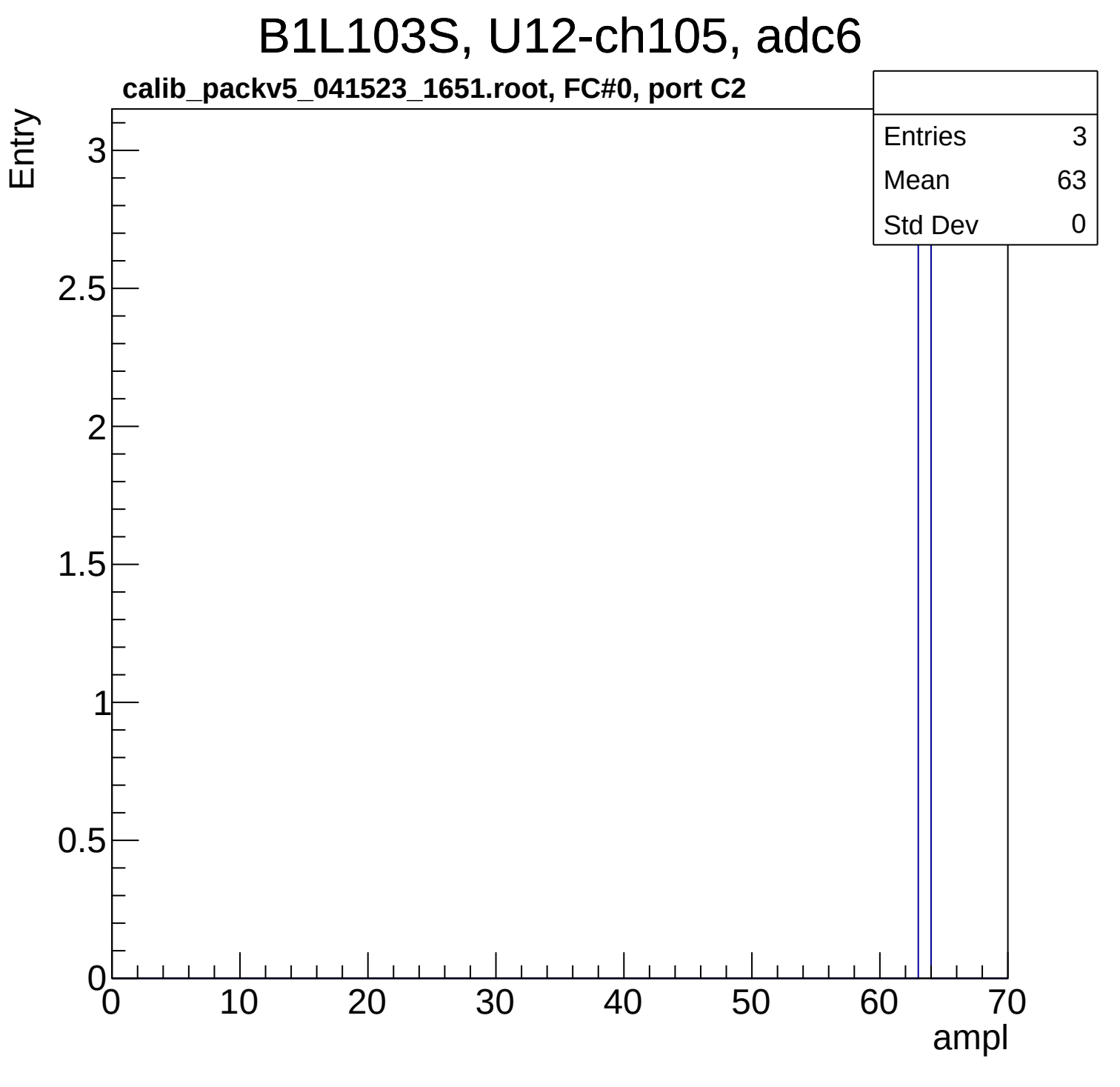
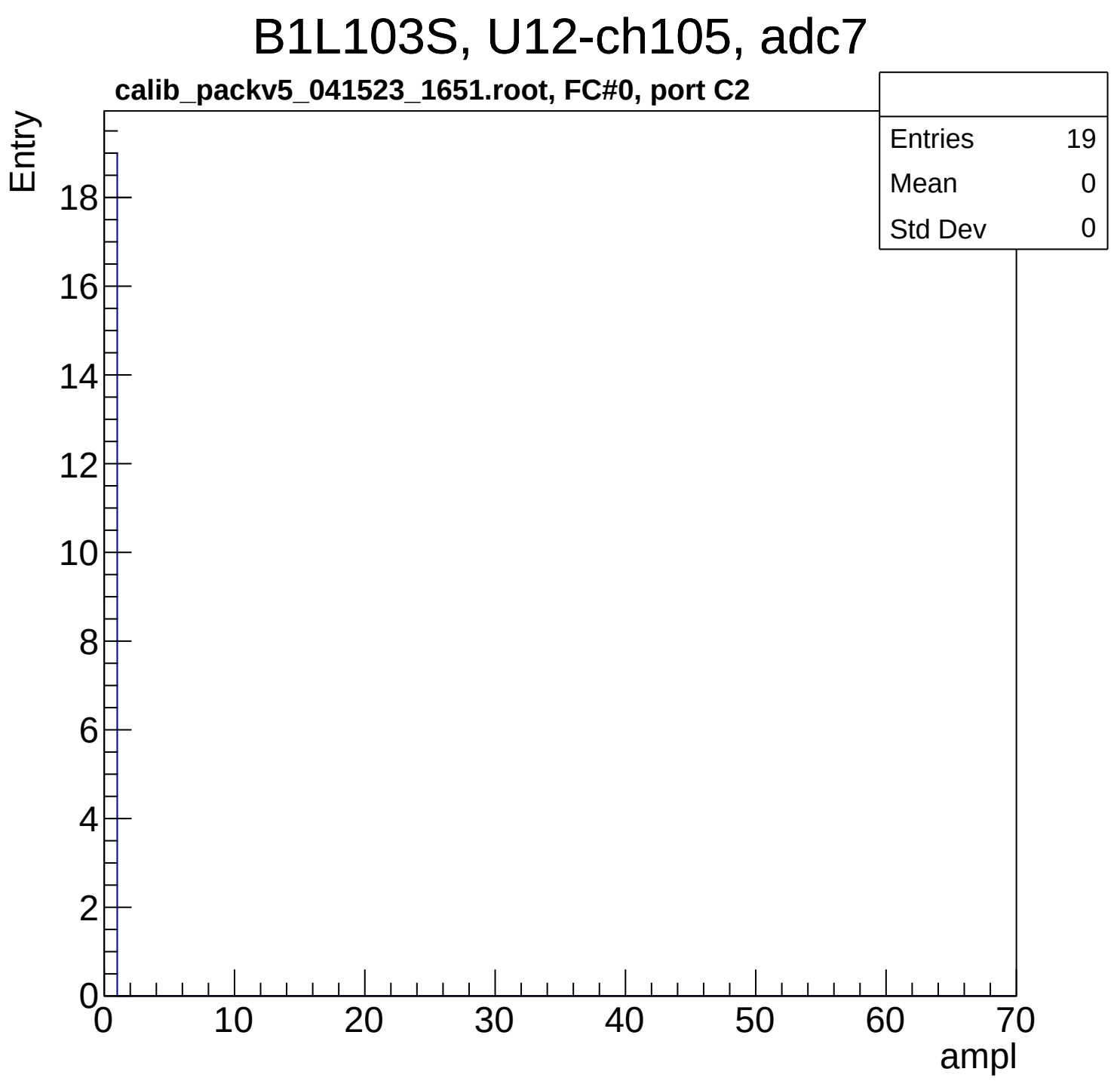
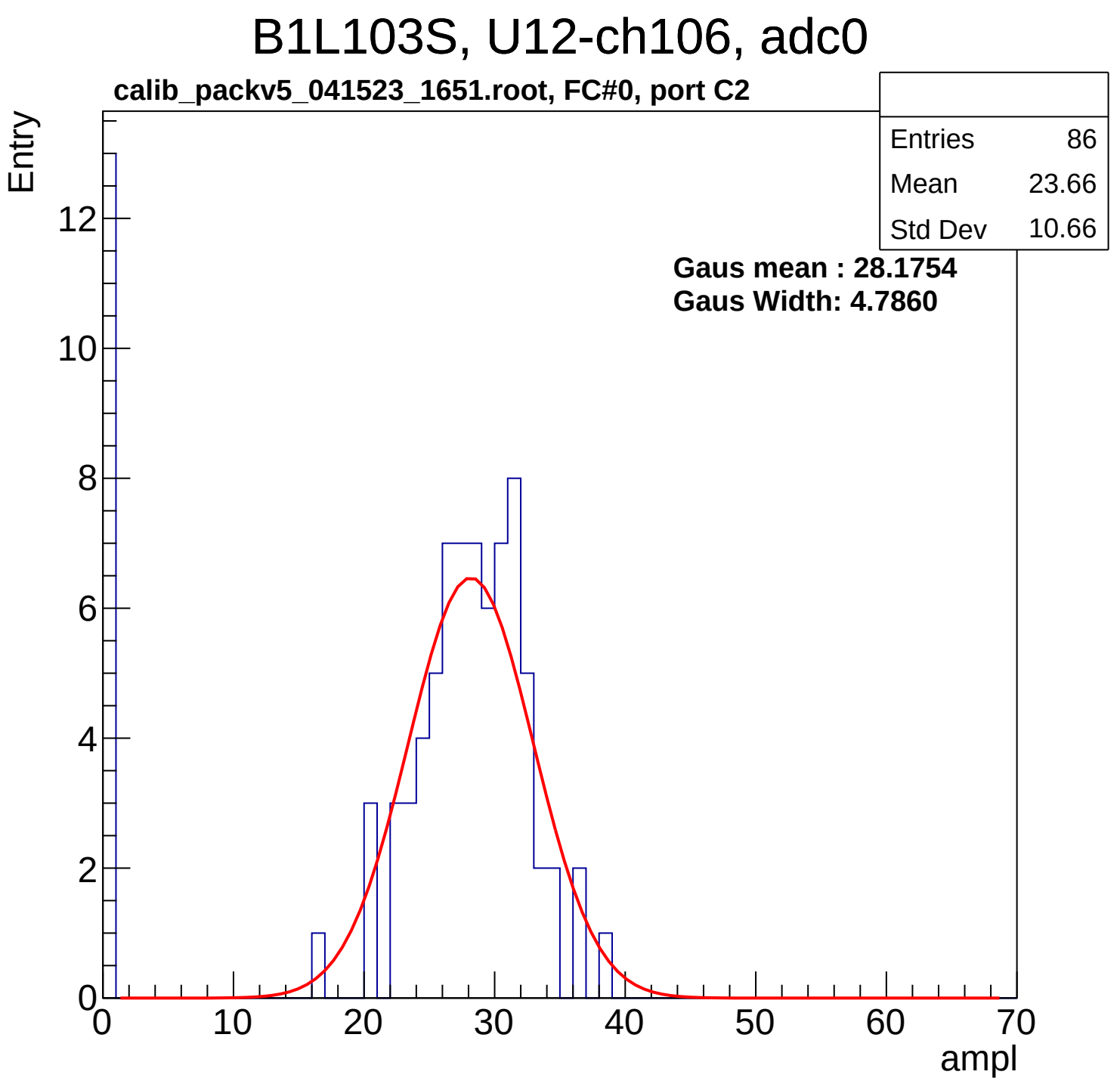
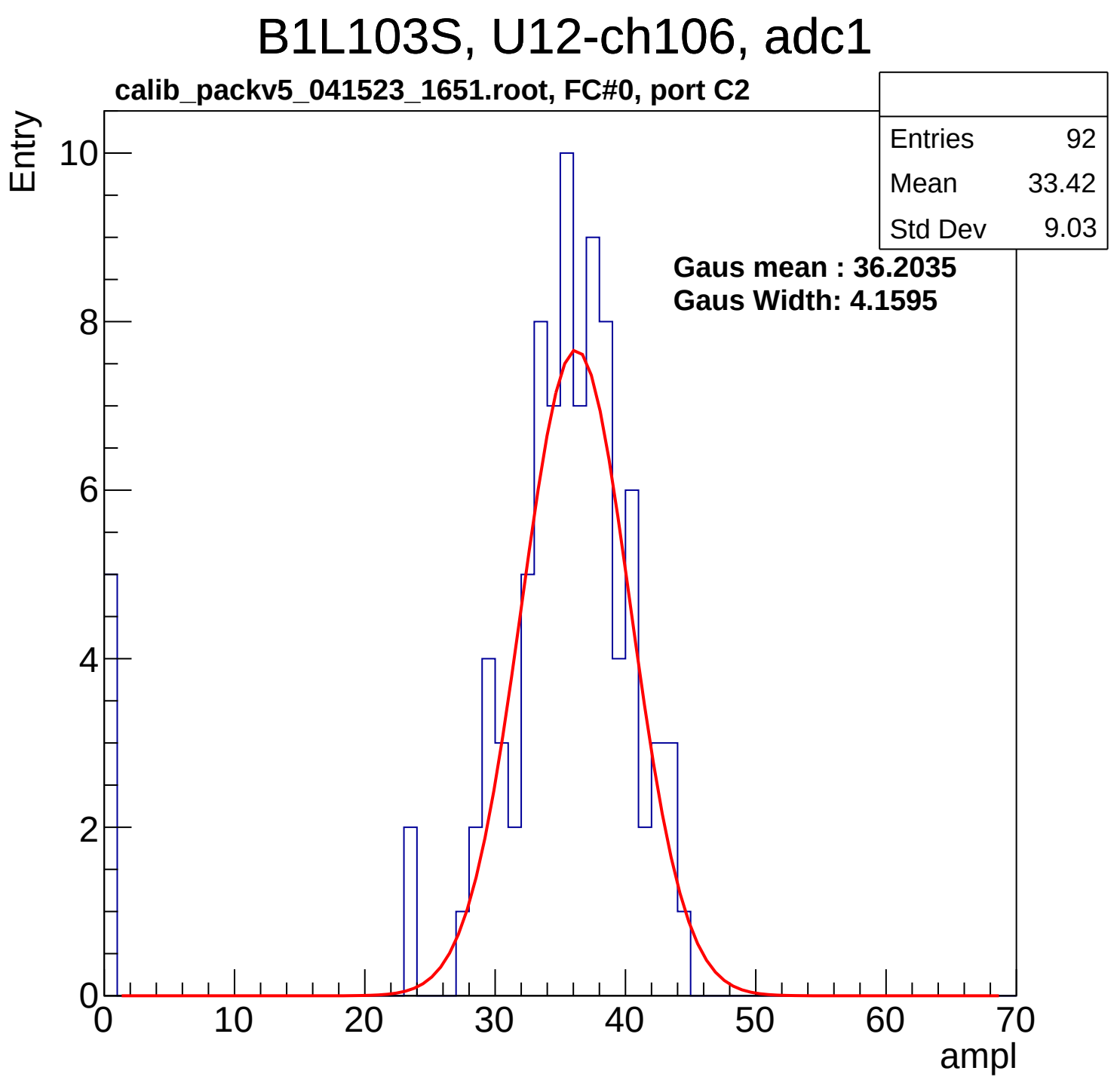

B1L103S, U12-ch105, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 3
Mean 63
Std Dev 0
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U12-ch105, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch106, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 86
Mean 23.66
Std Dev 10.66
Gaus mean : 28.1754
Gaus Width: 4.7860
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U12-ch106, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 33.42
Std Dev 9.03
Gaus mean : 36.2035
Gaus Width: 4.1595
Entry
ampl
0
2
4
6
8
10
0
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20
30
40
50
60
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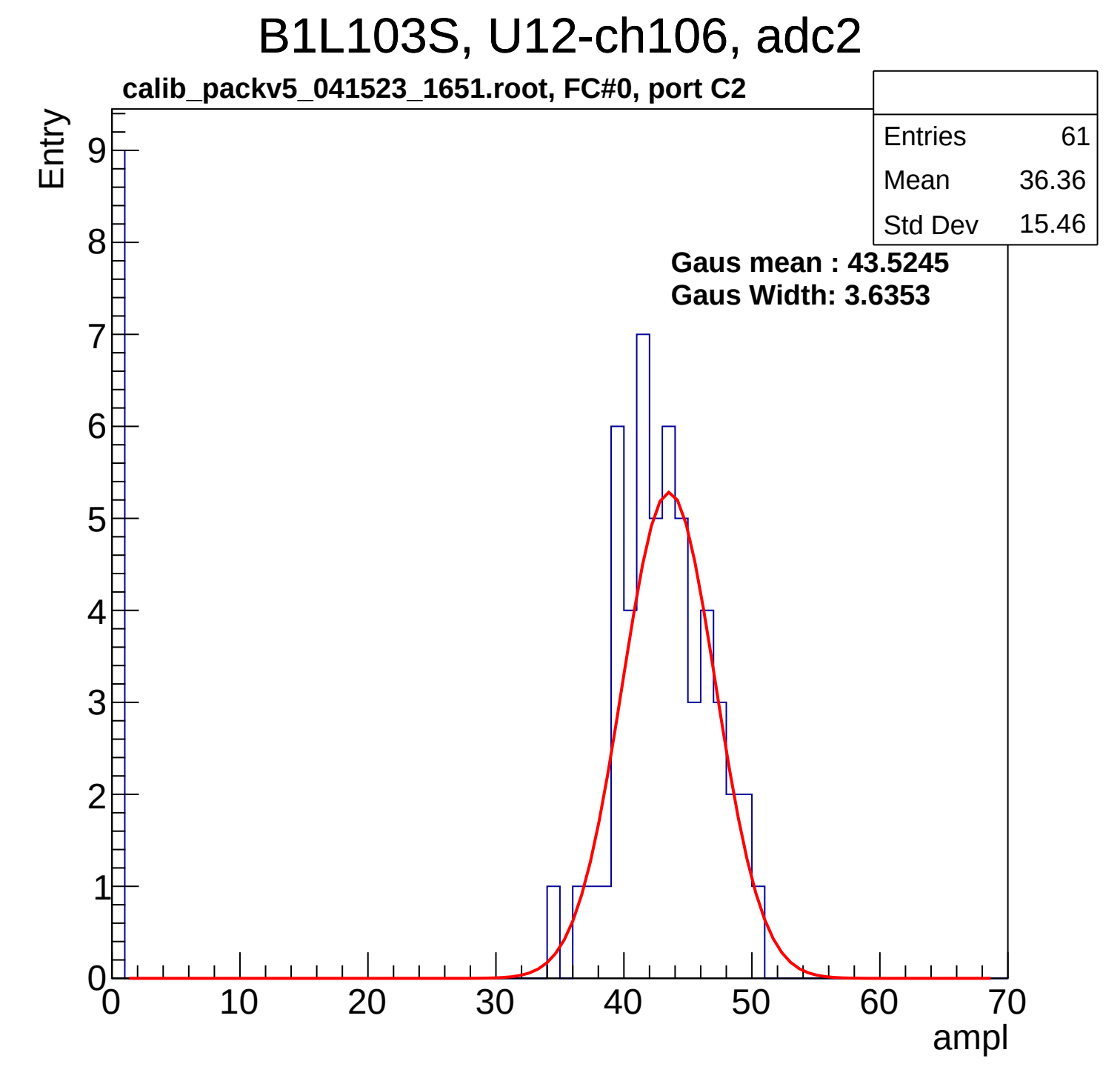
B1L103S, U12-ch106, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 36.36
Std Dev 15.46
Gaus mean : 43.5245
Gaus Width: 3.6353
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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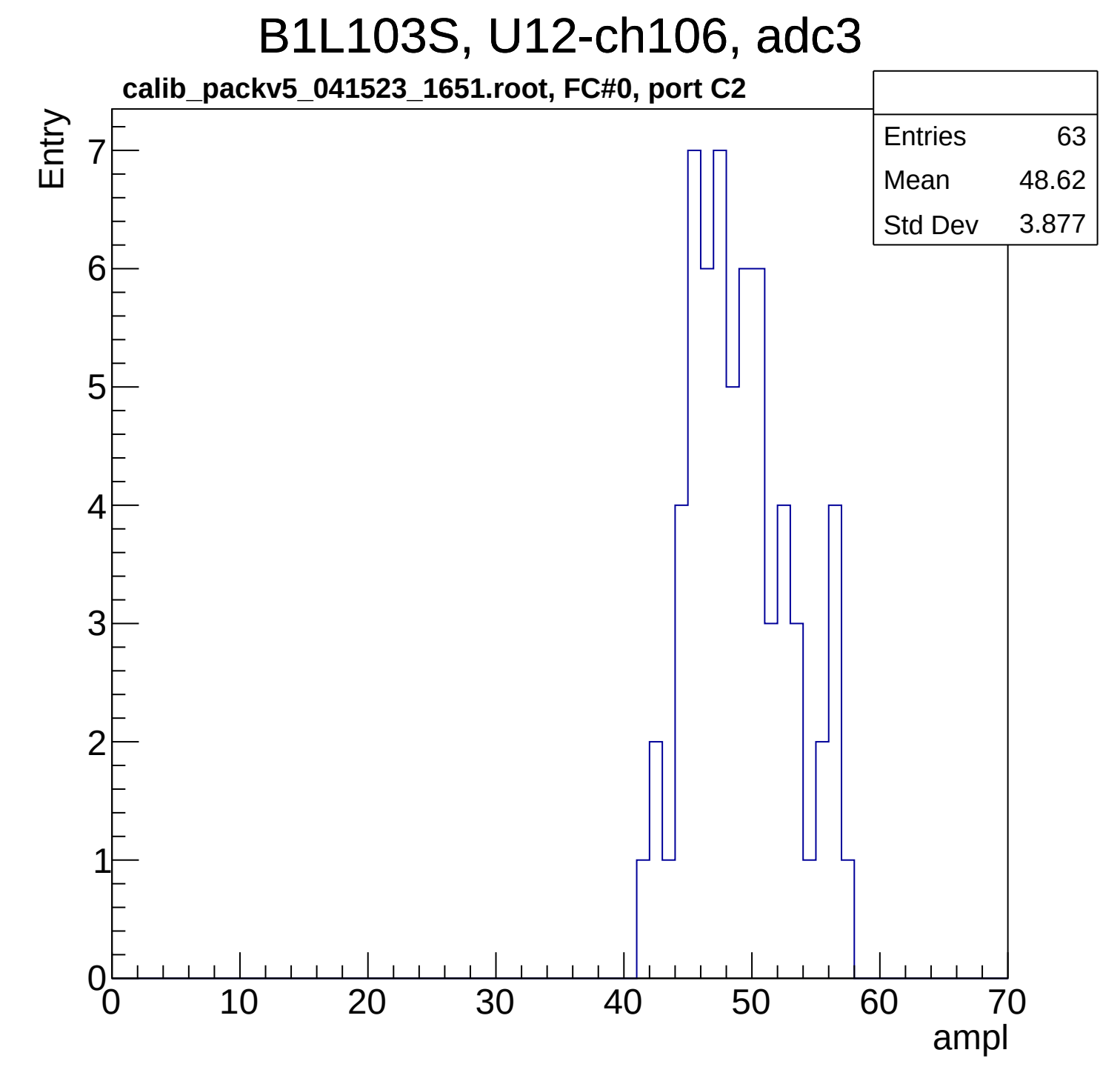
B1L103S, U12-ch106, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 48.62
Std Dev 3.877
Entry
ampl
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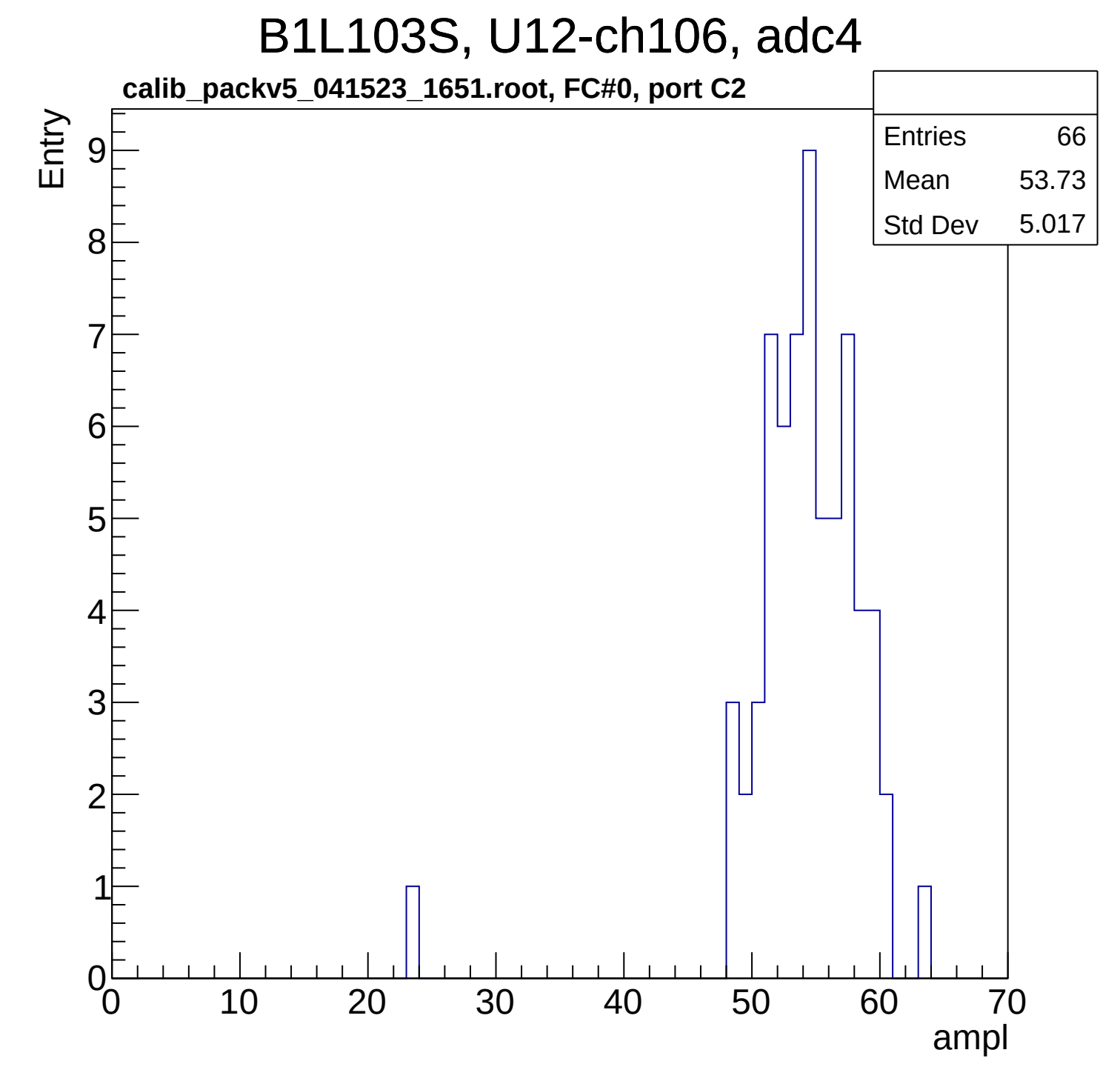
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U12-ch106, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 53.73
Std Dev 5.017
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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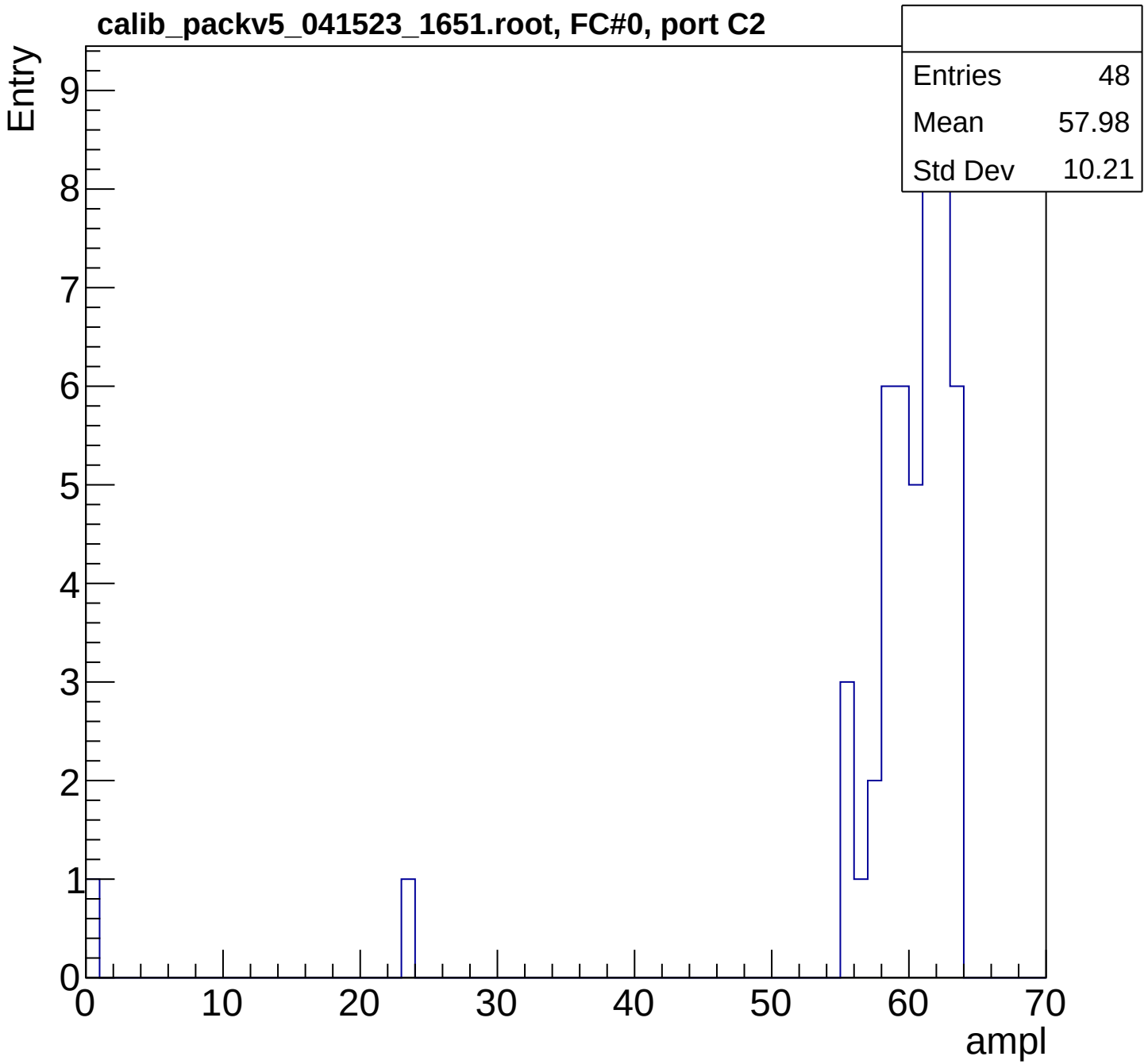
B1L103S, U12-ch106, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 57.98
Std Dev 10.21
Entry
ampl
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6
7
8
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0
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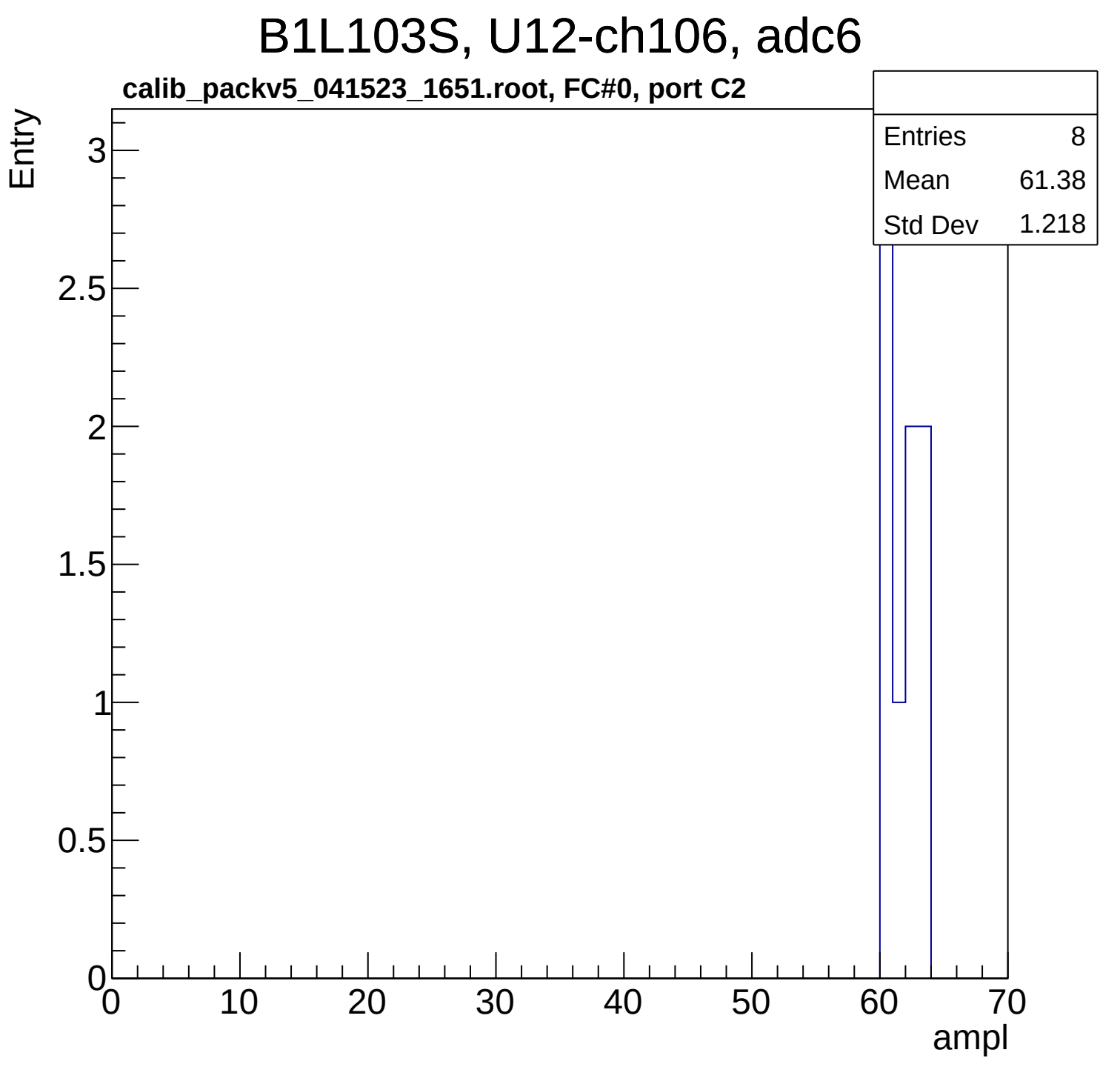
B1L103S, U12-ch106, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.38
Std Dev 1.218
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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20
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40
50
60
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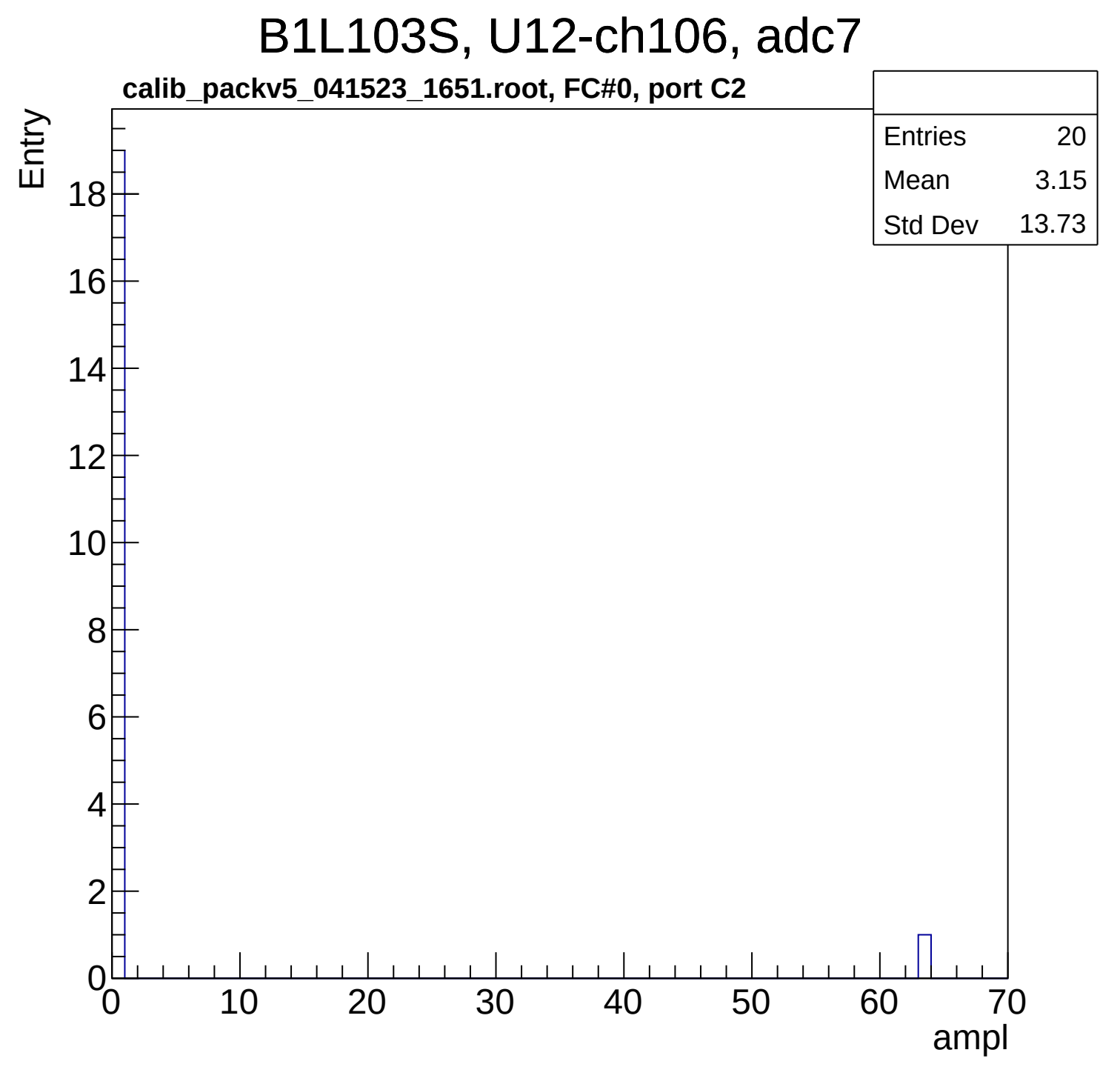
B1L103S, U12-ch106, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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2
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6
8
10
12
14
16
18
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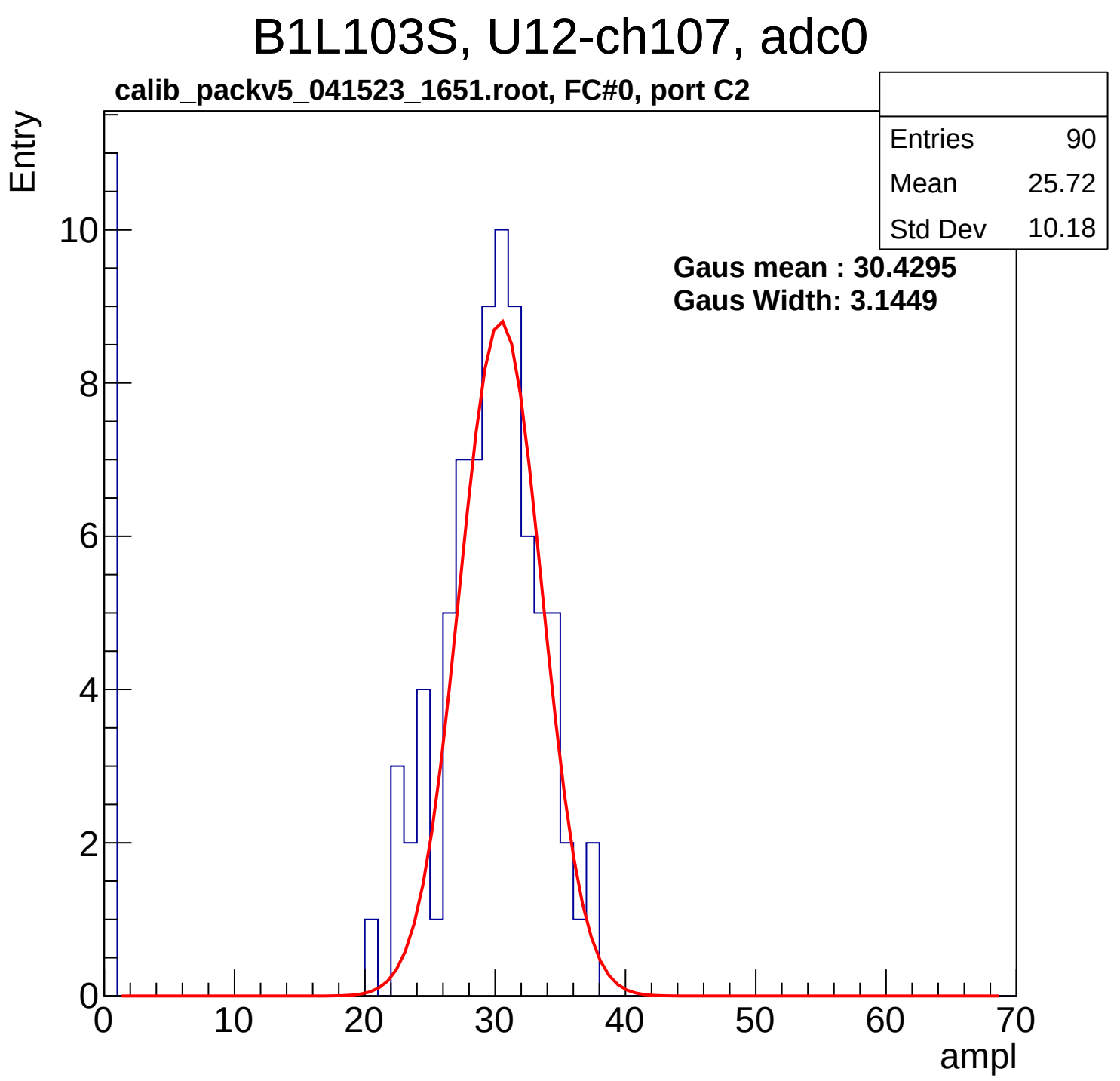
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch107, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 25.72
Std Dev 10.18
Gaus mean : 30.4295
Gaus Width: 3.1449
Entry
ampl
0
2
4
6
8
10
0
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20
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40
50
60
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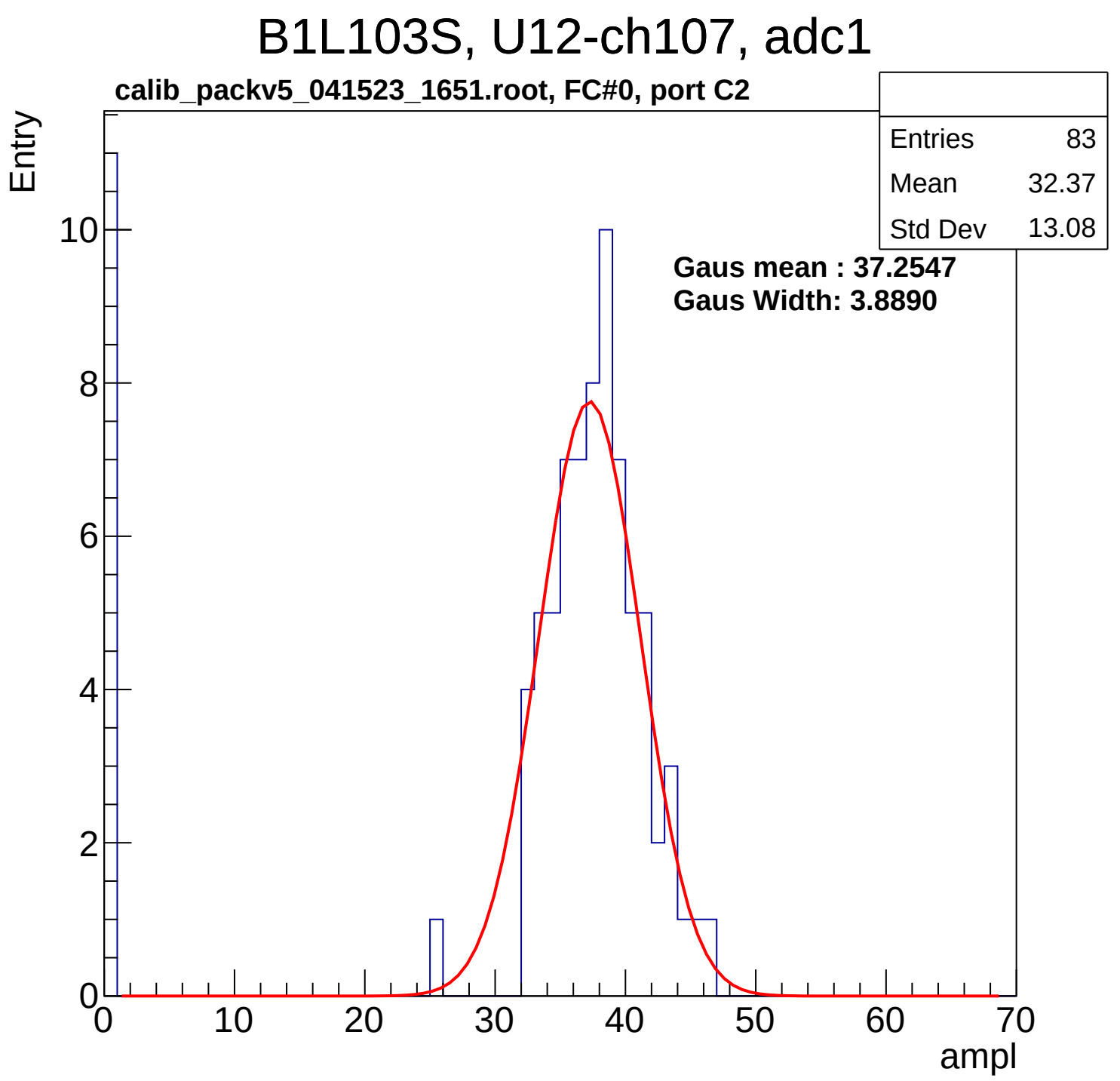
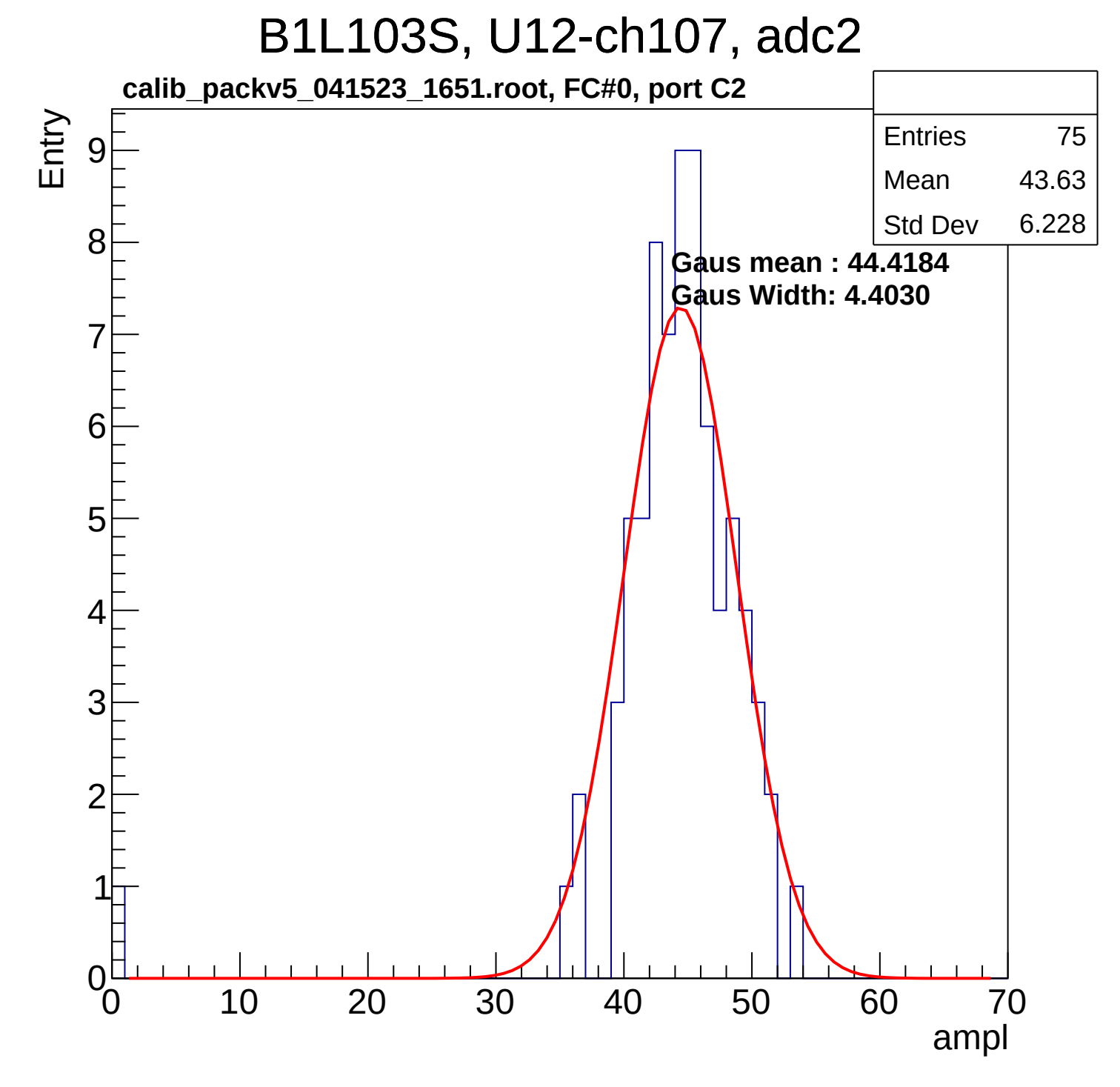

B1L103S, U12-ch107, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 32.37
Std Dev 13.08
Gaus mean : 37.2547
Gaus Width: 3.8890
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch107, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 75
Mean 43.63
Std Dev 6.228
Gaus mean : 44.4184
Gaus Width: 4.4030
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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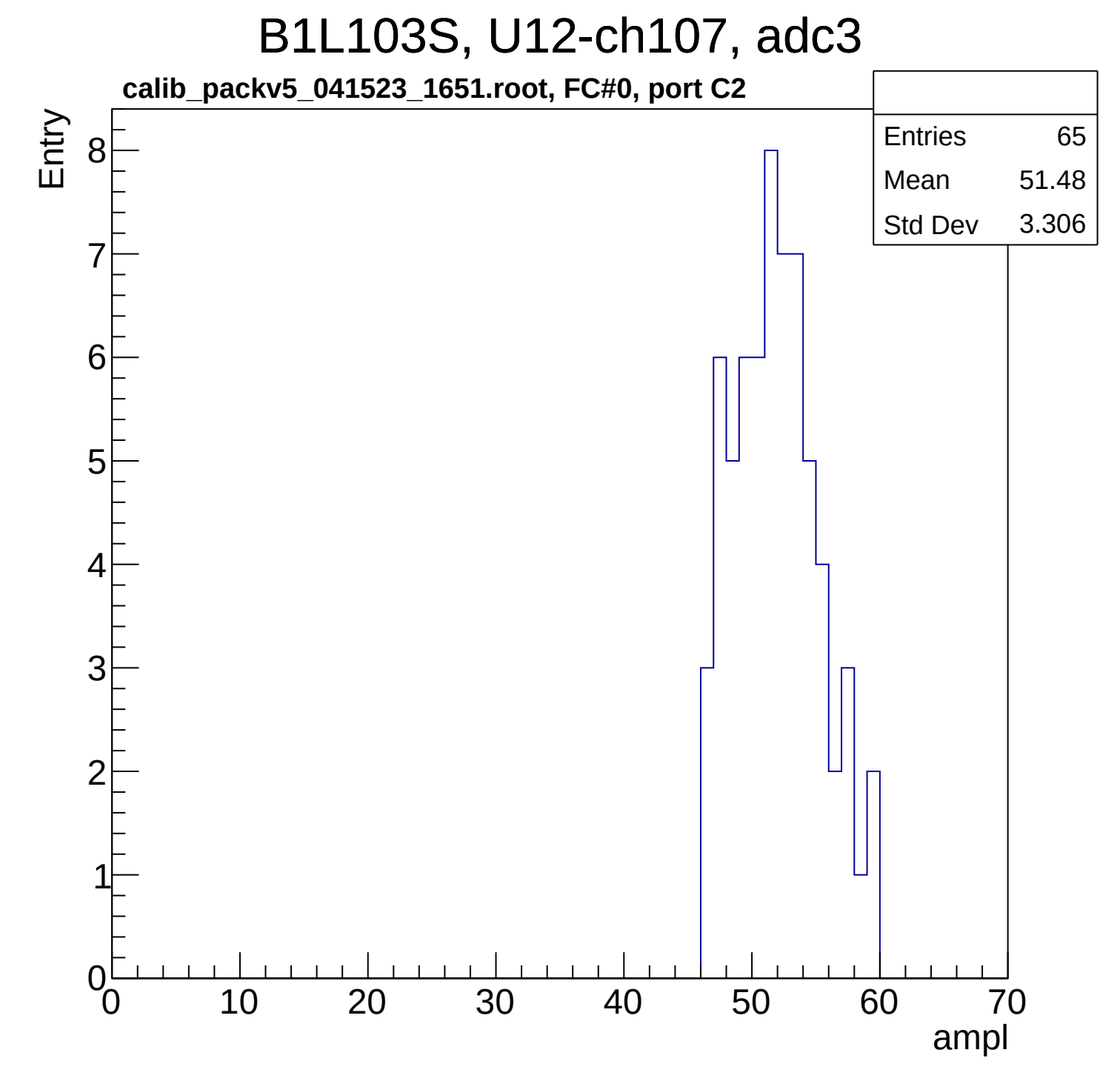
B1L103S, U12-ch107, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 51.48
Std Dev 3.306
Entry
ampl
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4
5
6
7
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0
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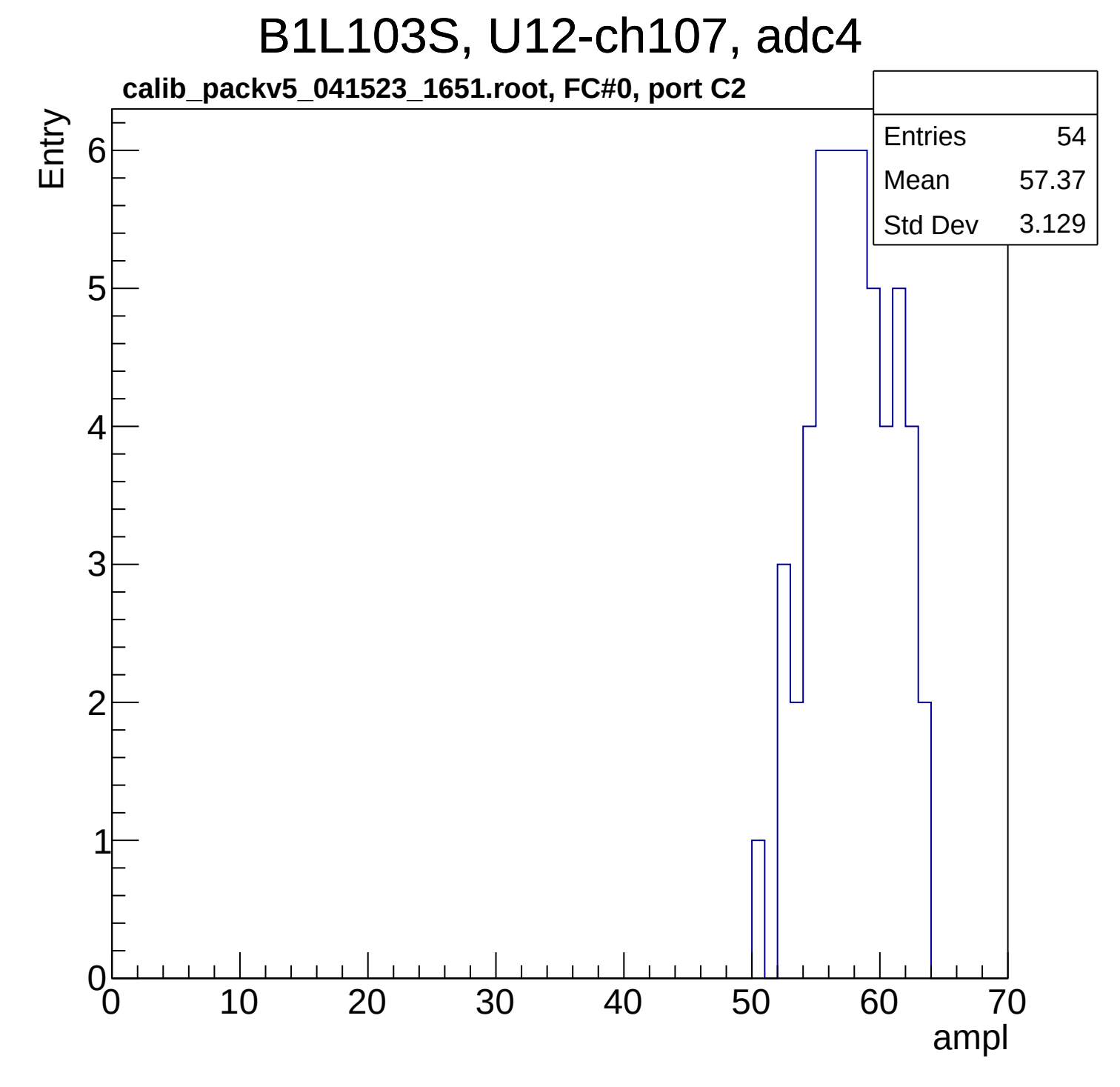
B1L103S, U12-ch107, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 57.37
Std Dev 3.129
Entry
ampl
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1
2
3
4
5
6
0
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20
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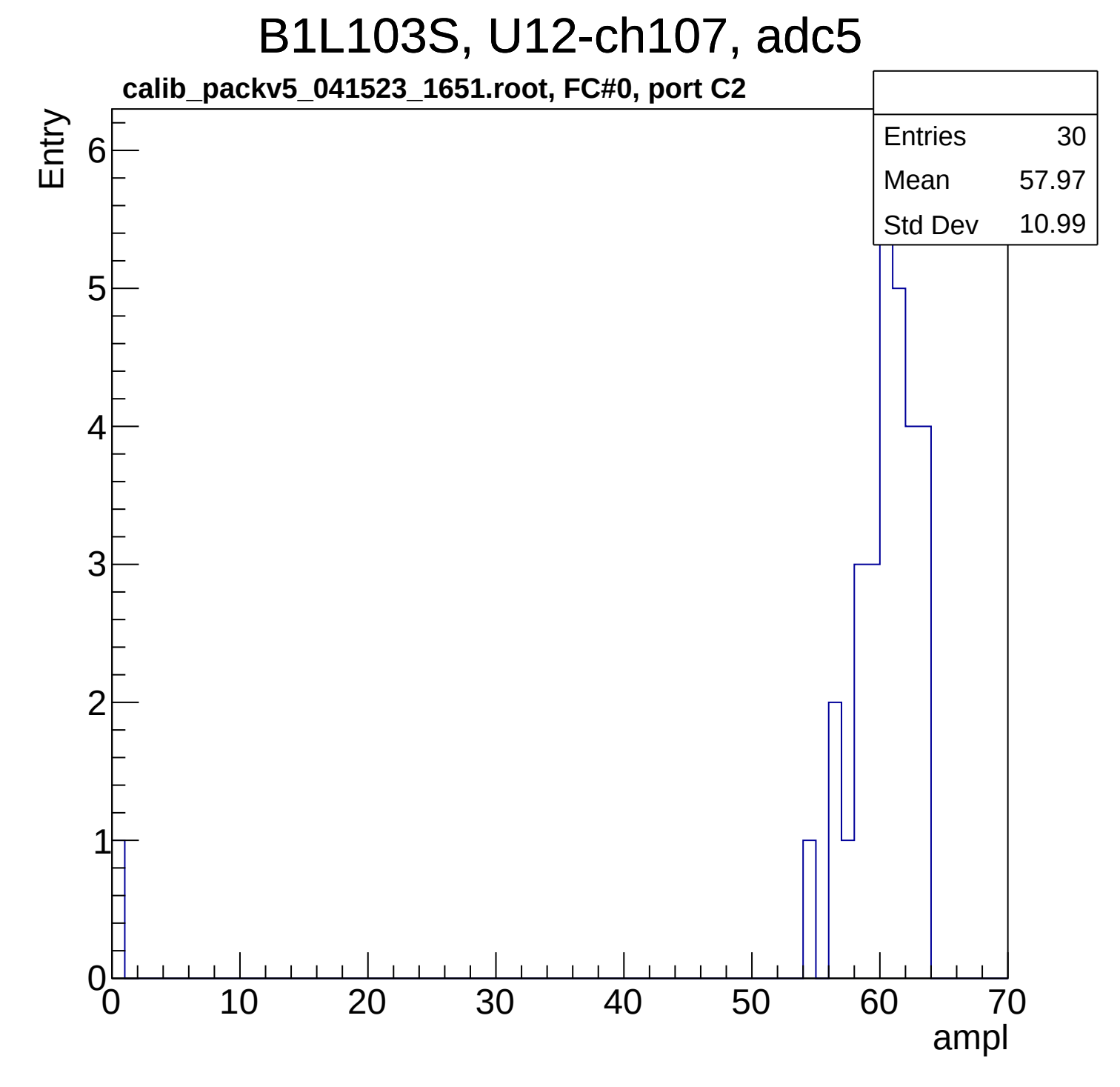
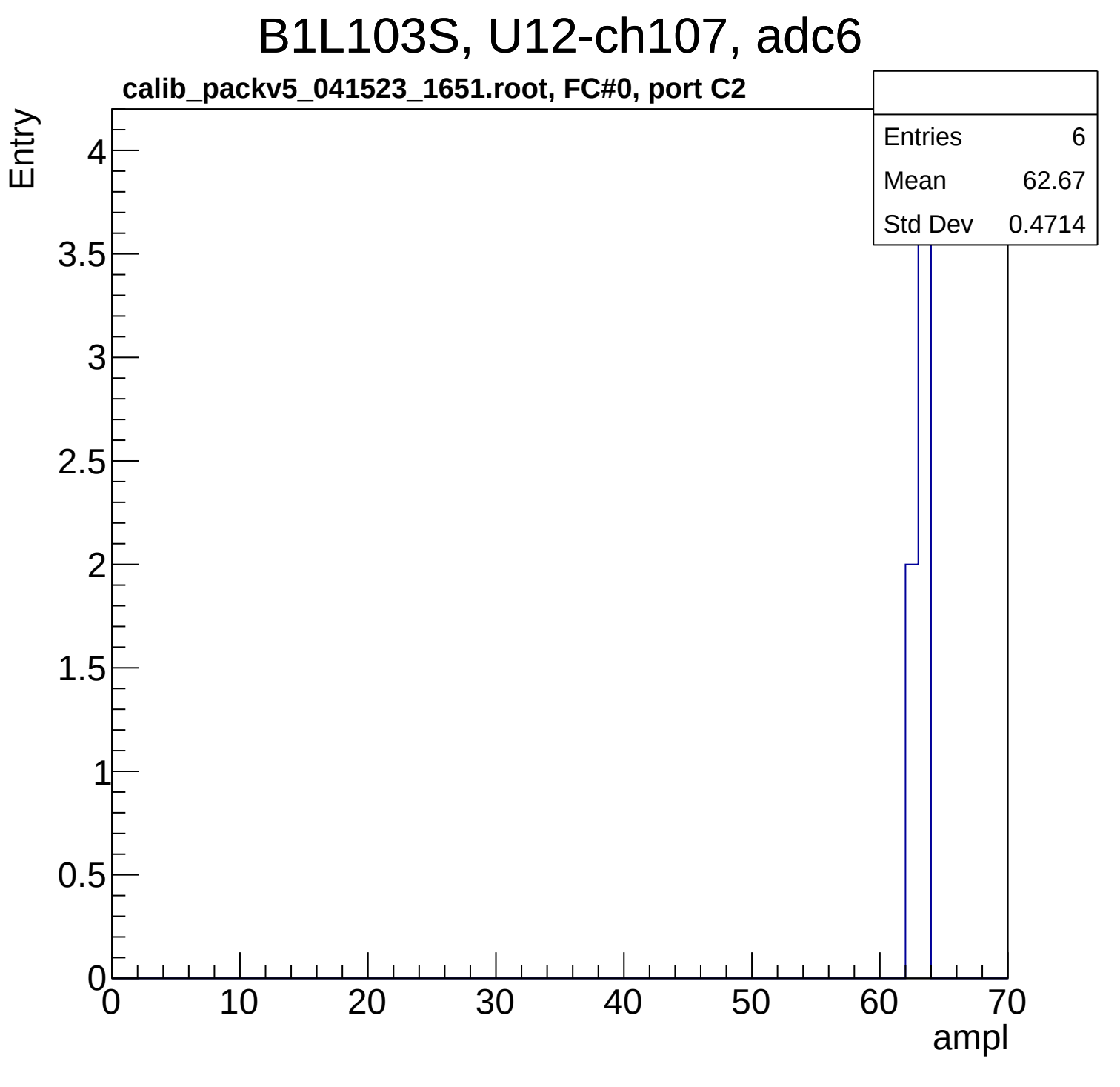

B1L103S, U12-ch107, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 57.97
Std Dev 10.99
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U12-ch107, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62.67
Std Dev 0.4714
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
10
20
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40
50
60
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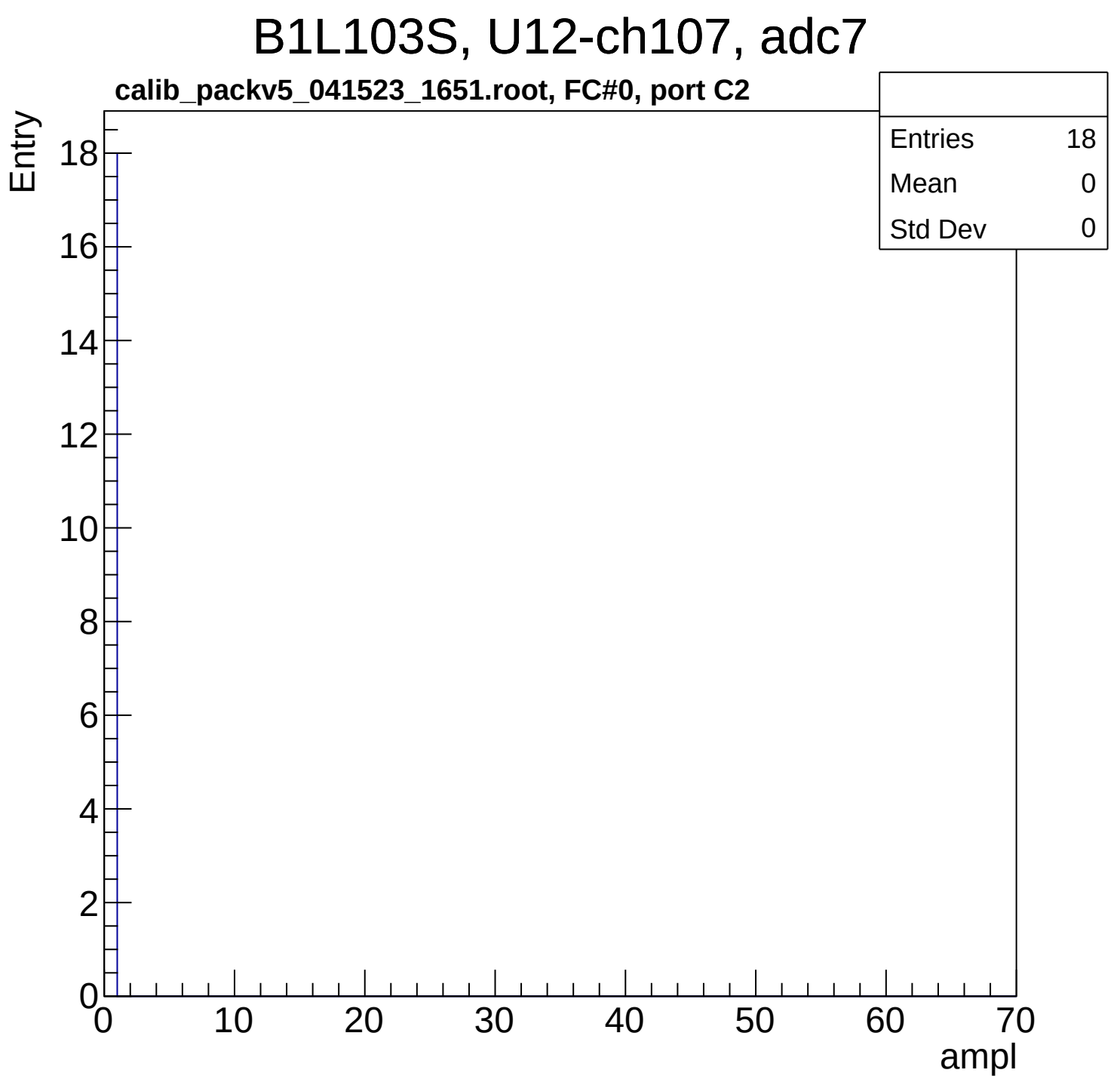
B1L103S, U12-ch107, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
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8
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16
18
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10
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30
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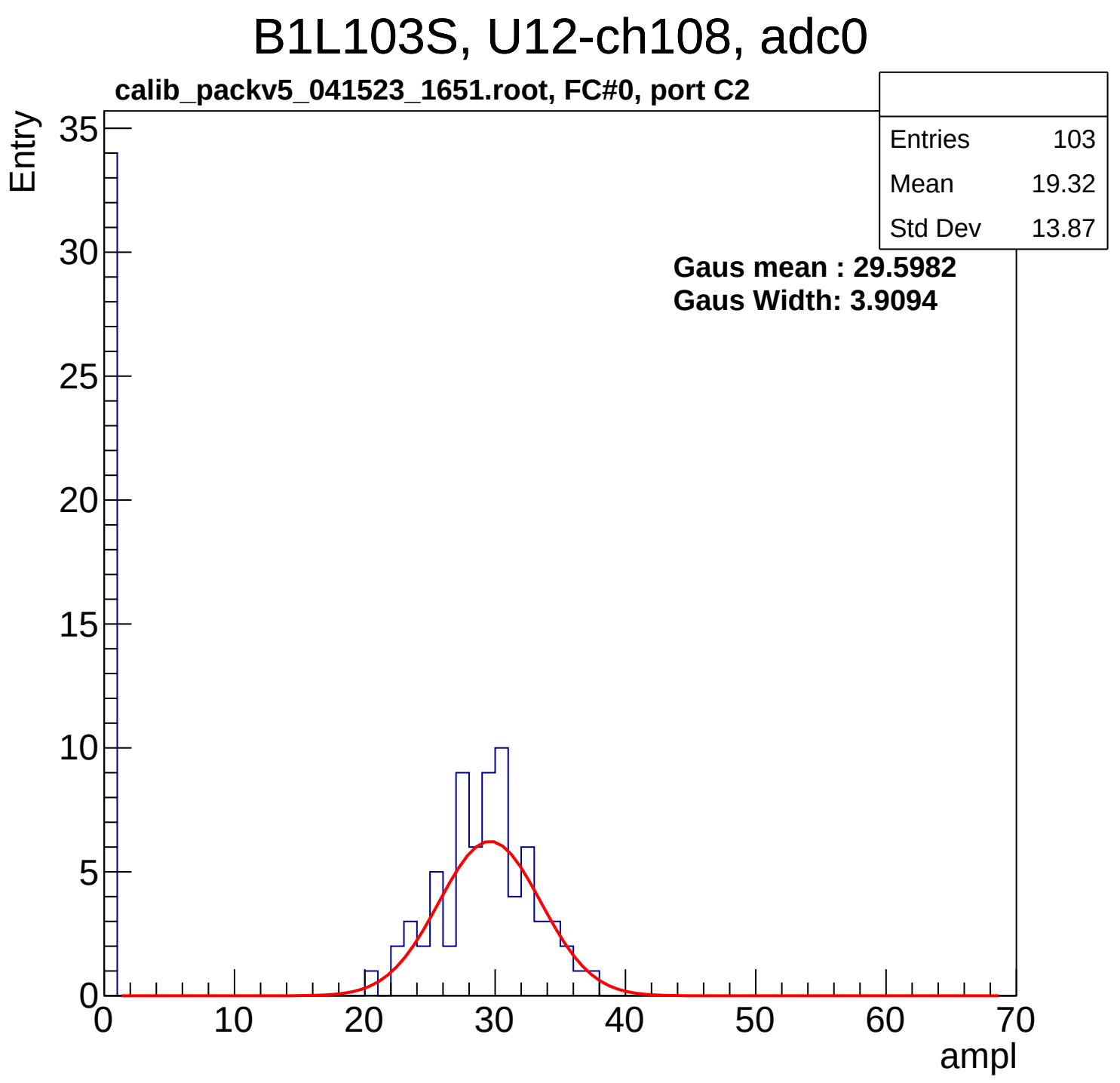
70
ampl


B1L103S, U12-ch108, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 103
Mean 19.32
Std Dev 13.87
Gaus mean : 29.5982
Gaus Width: 3.9094
Entry
ampl
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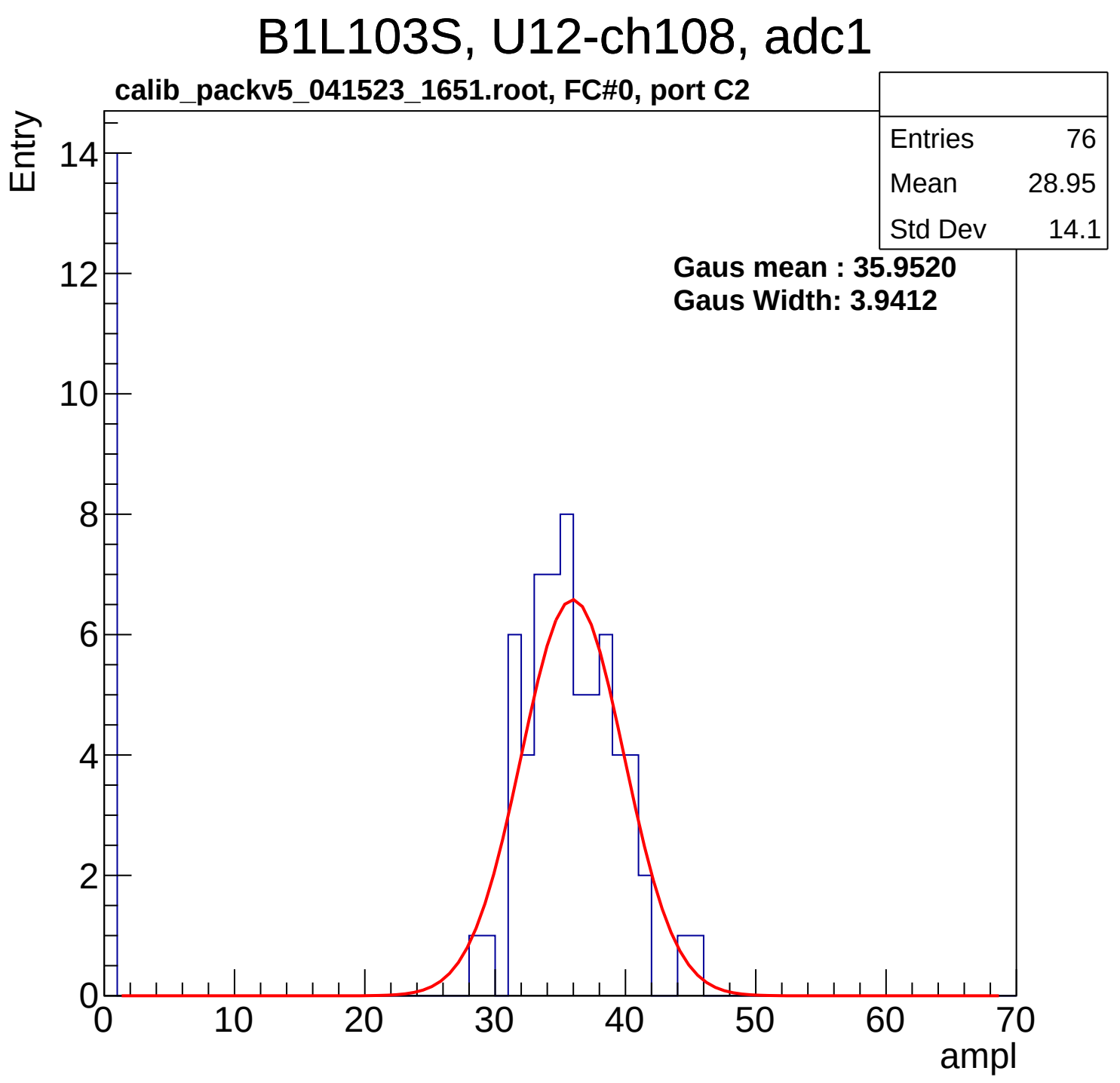
5
10
15
20
25
30
35
0
10
20
30
40
50
60
70


B1L103S, U12-ch108, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 28.95
Std Dev 14.1
Gaus mean : 35.9520
Gaus Width: 3.9412
Entry
ampl
0
2
4
6
8
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0
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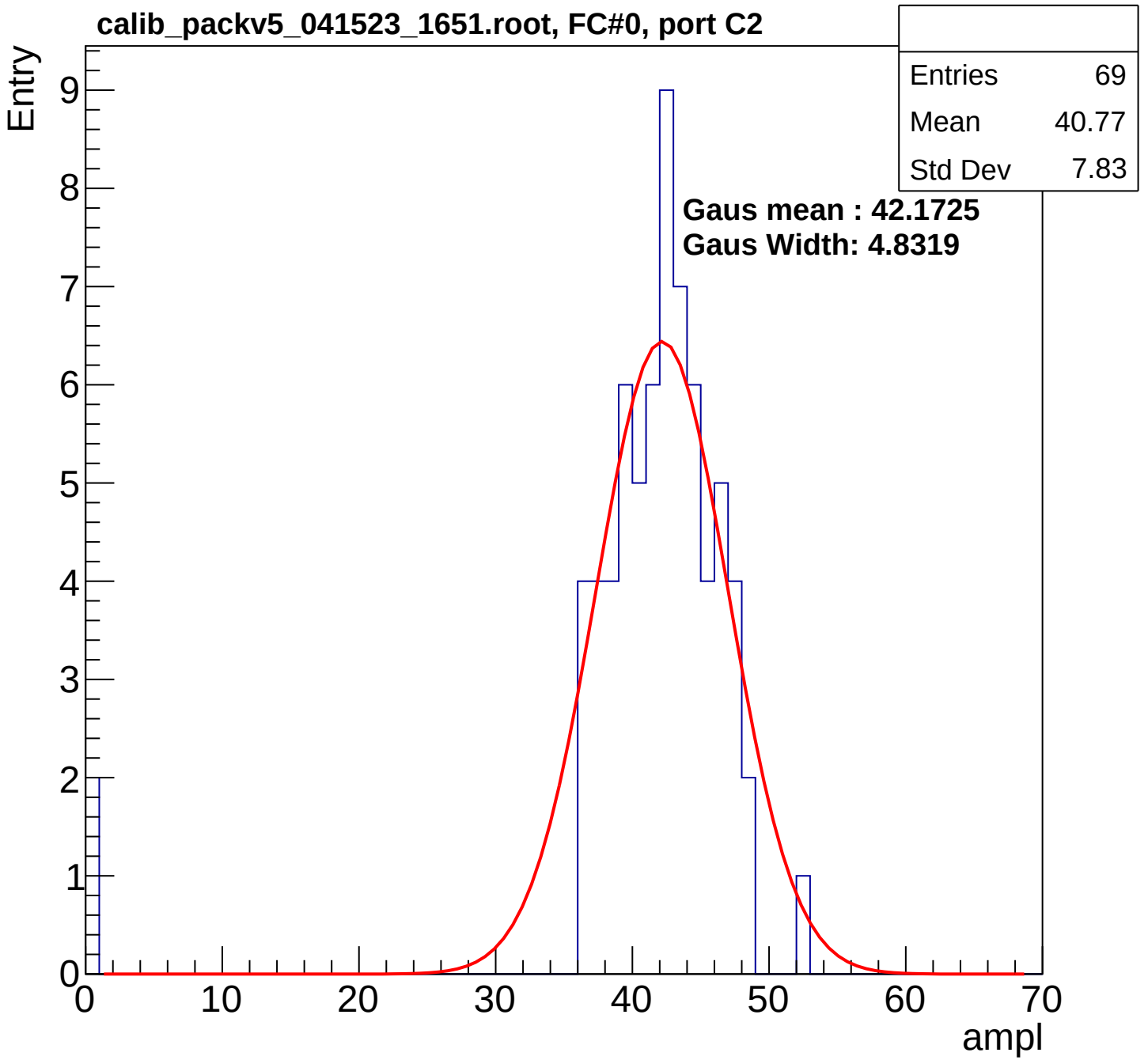
40
50
60
70


B1L103S, U12-ch108, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 69
Mean 40.77
Std Dev 7.83
Gaus mean : 42.1725
Gaus Width: 4.8319
Entry
ampl
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10
20
30
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1
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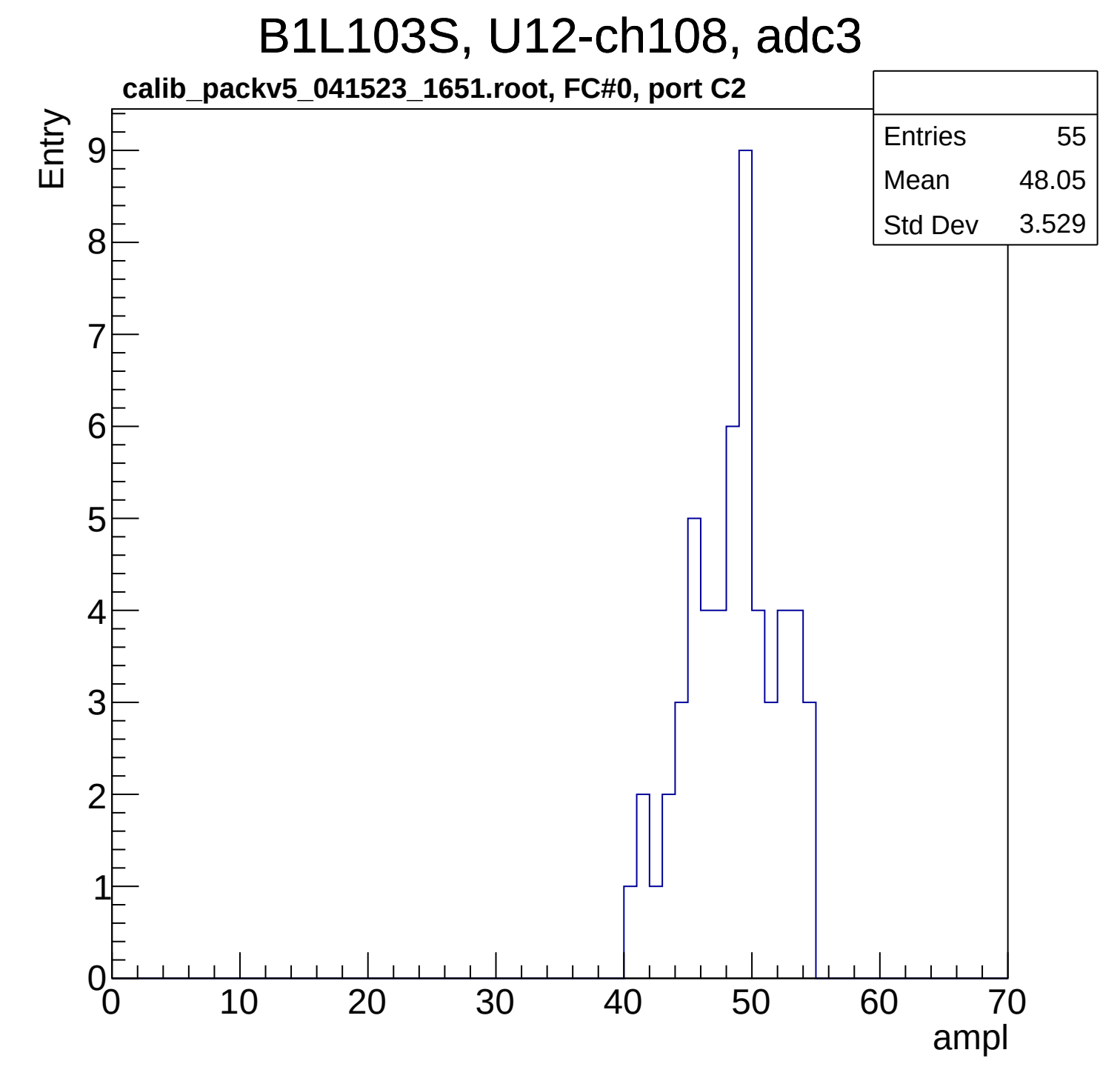
8
9


B1L103S, U12-ch108, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 48.05
Std Dev 3.529
Entry
ampl
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3
4
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6
7
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0
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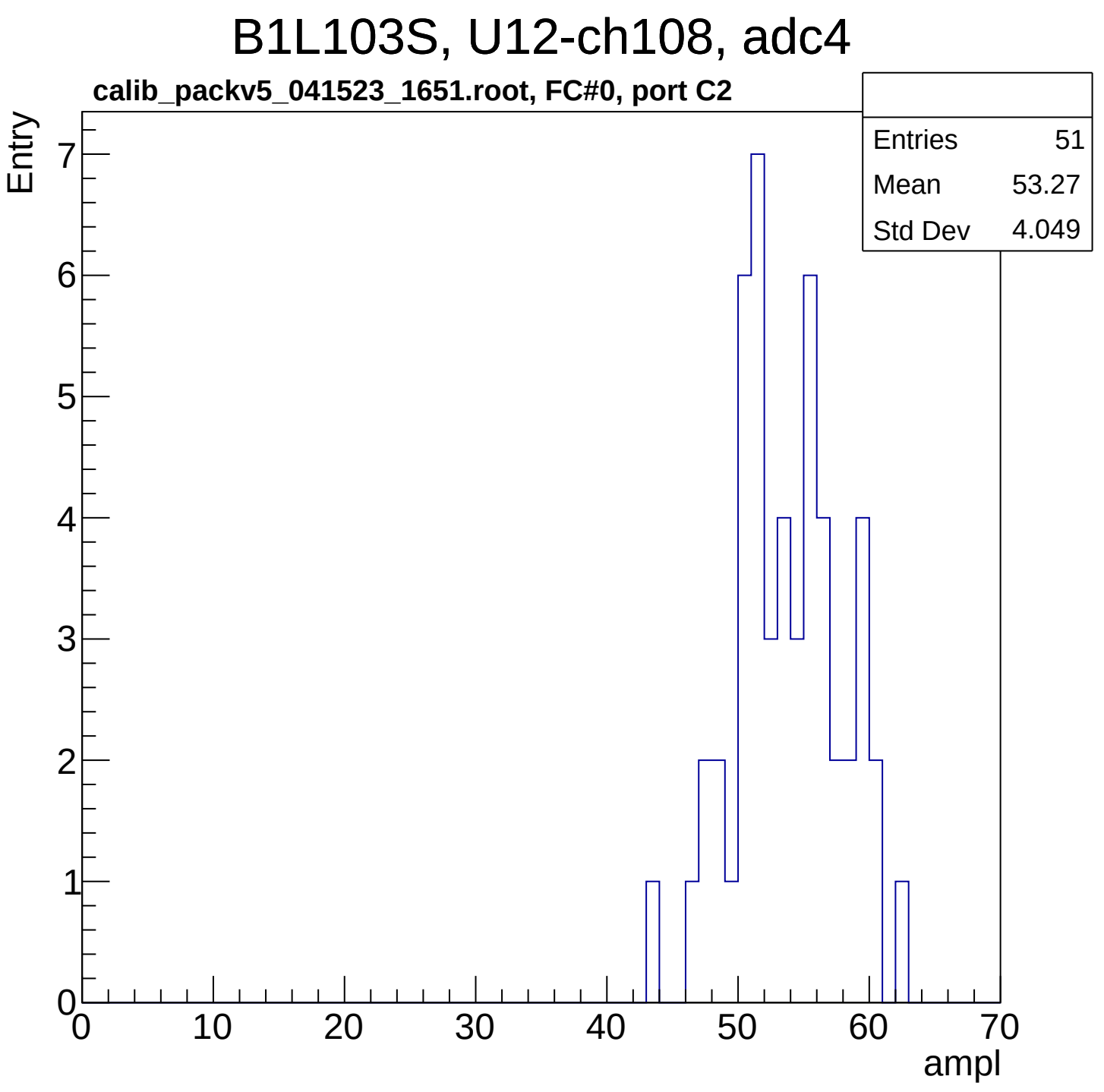
B1L103S, U12-ch108, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 53.27
Std Dev 4.049
Entry
ampl
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1
2
3
4
5
6
7
0
10
20
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40
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60
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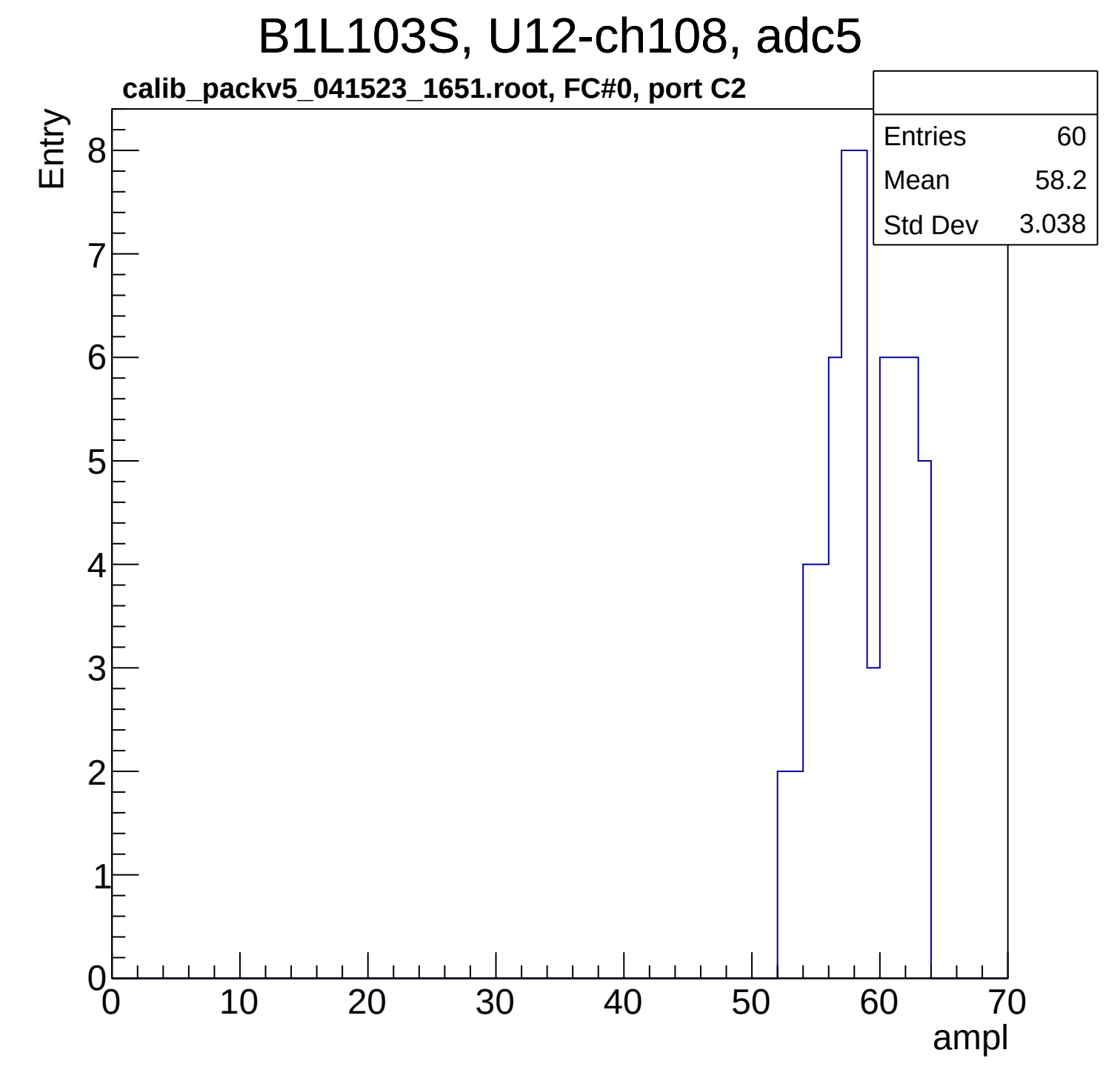
B1L103S, U12-ch108, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 58.2
Std Dev 3.038
Entry
ampl
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2
3
4
5
6
7
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0
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40
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60
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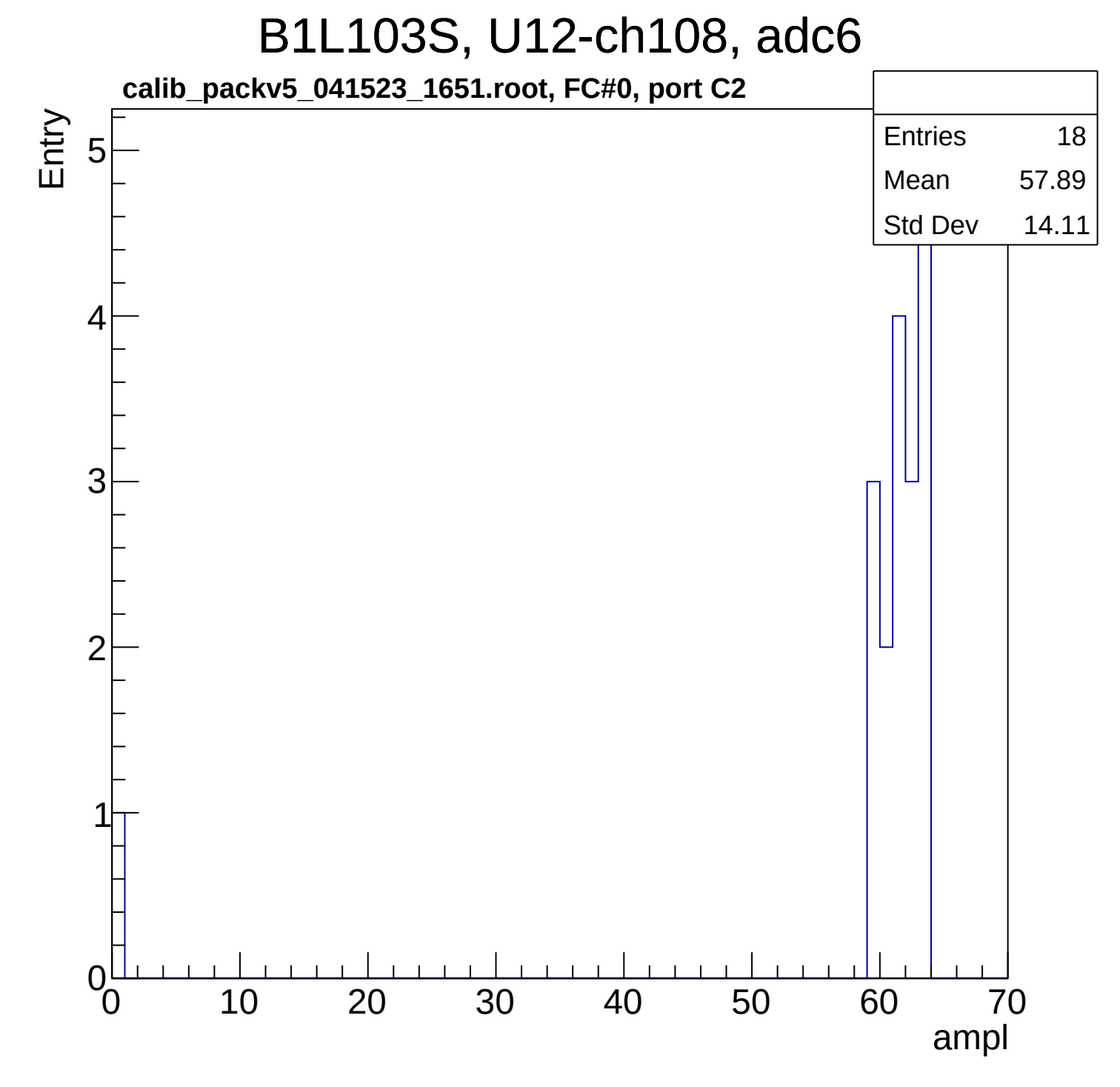
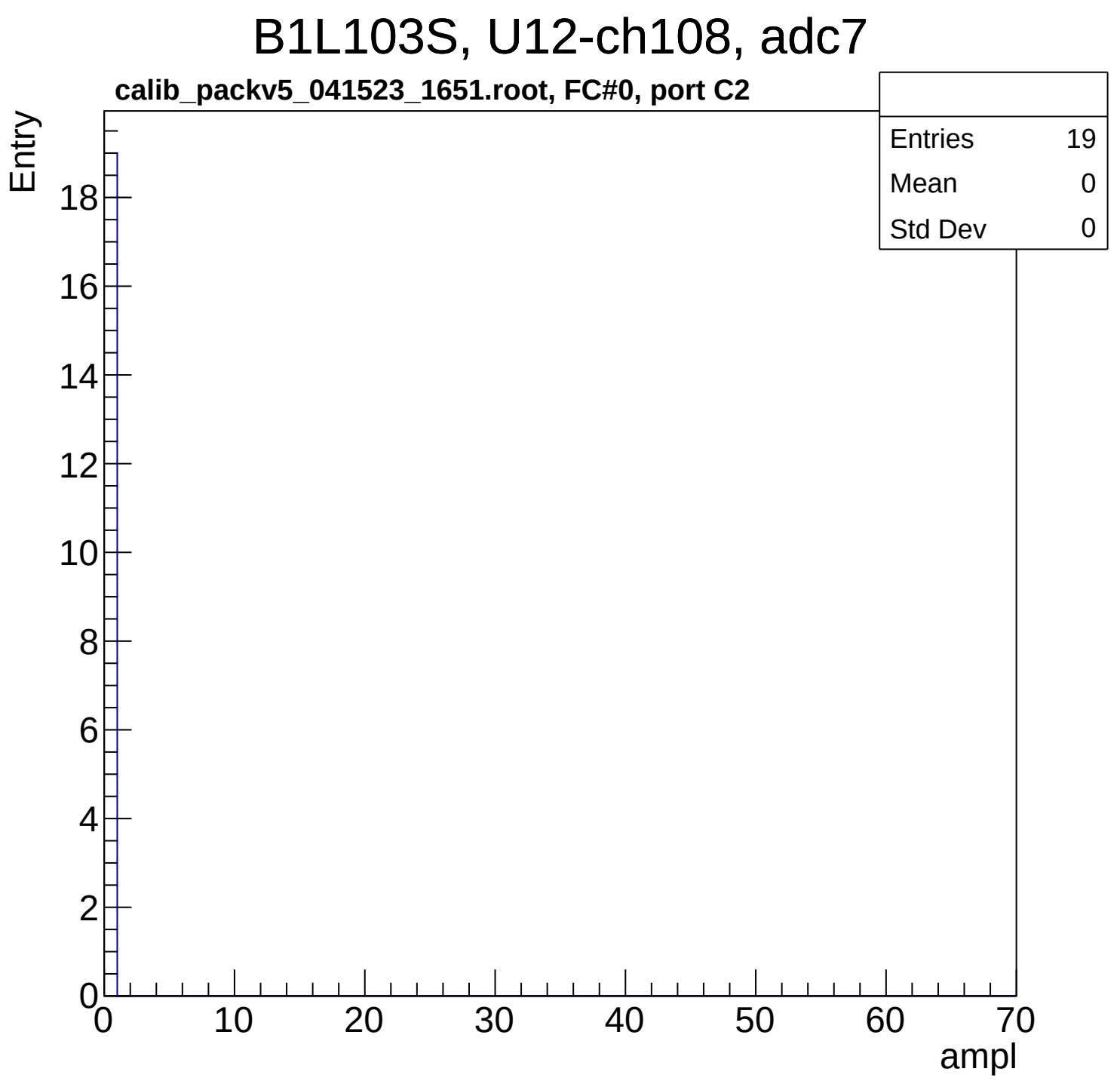

B1L103S, U12-ch108, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 57.89
Std Dev 14.11
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch108, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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2
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6
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10
12
14
16
18
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10
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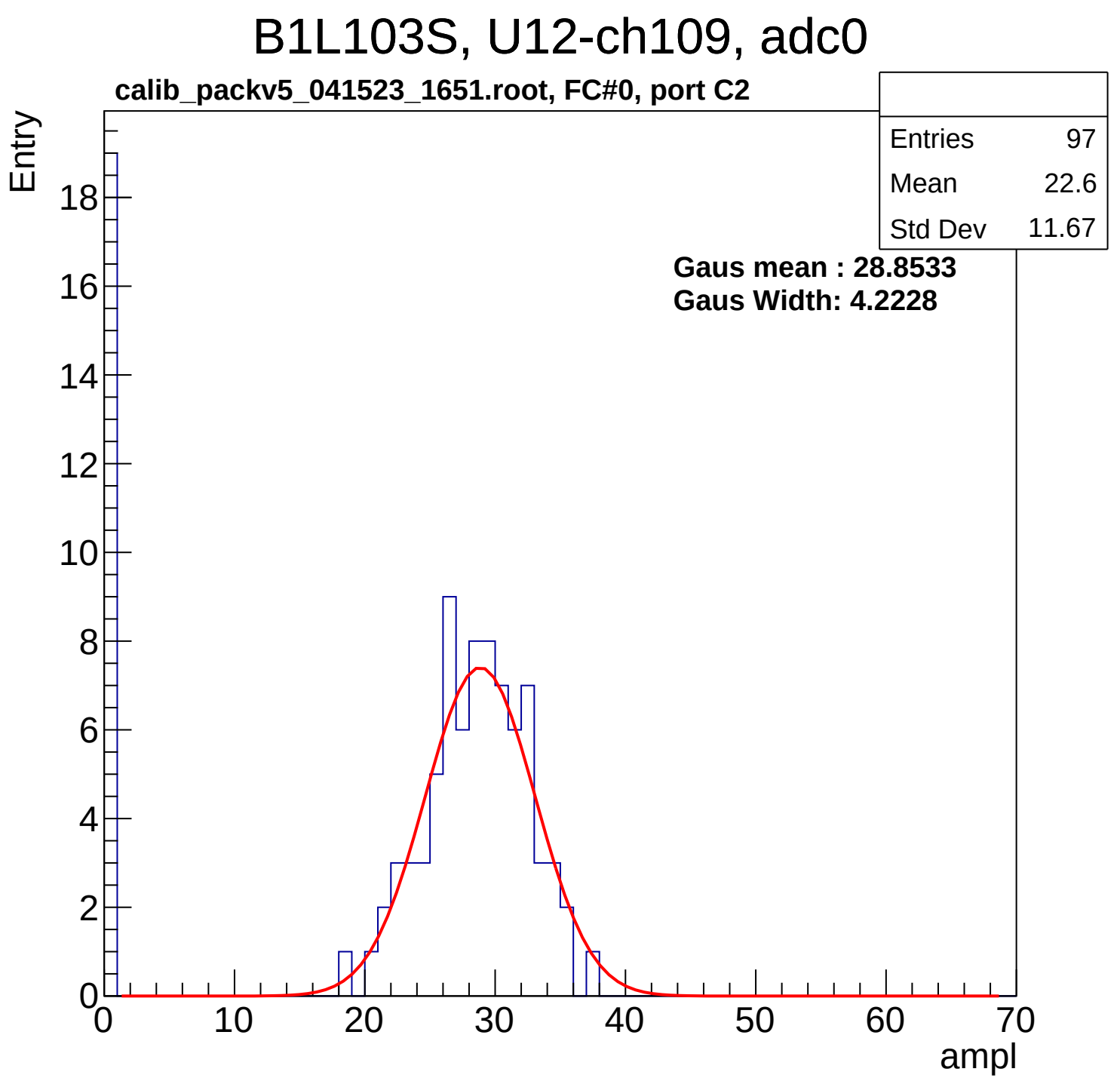
50
60
70
ampl


B1L103S, U12-ch109, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 22.6
Std Dev 11.67
Gaus mean : 28.8533
Gaus Width: 4.2228
Entry
ampl
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4
6
8
10
12
14
16
18
0
10
20
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40
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60
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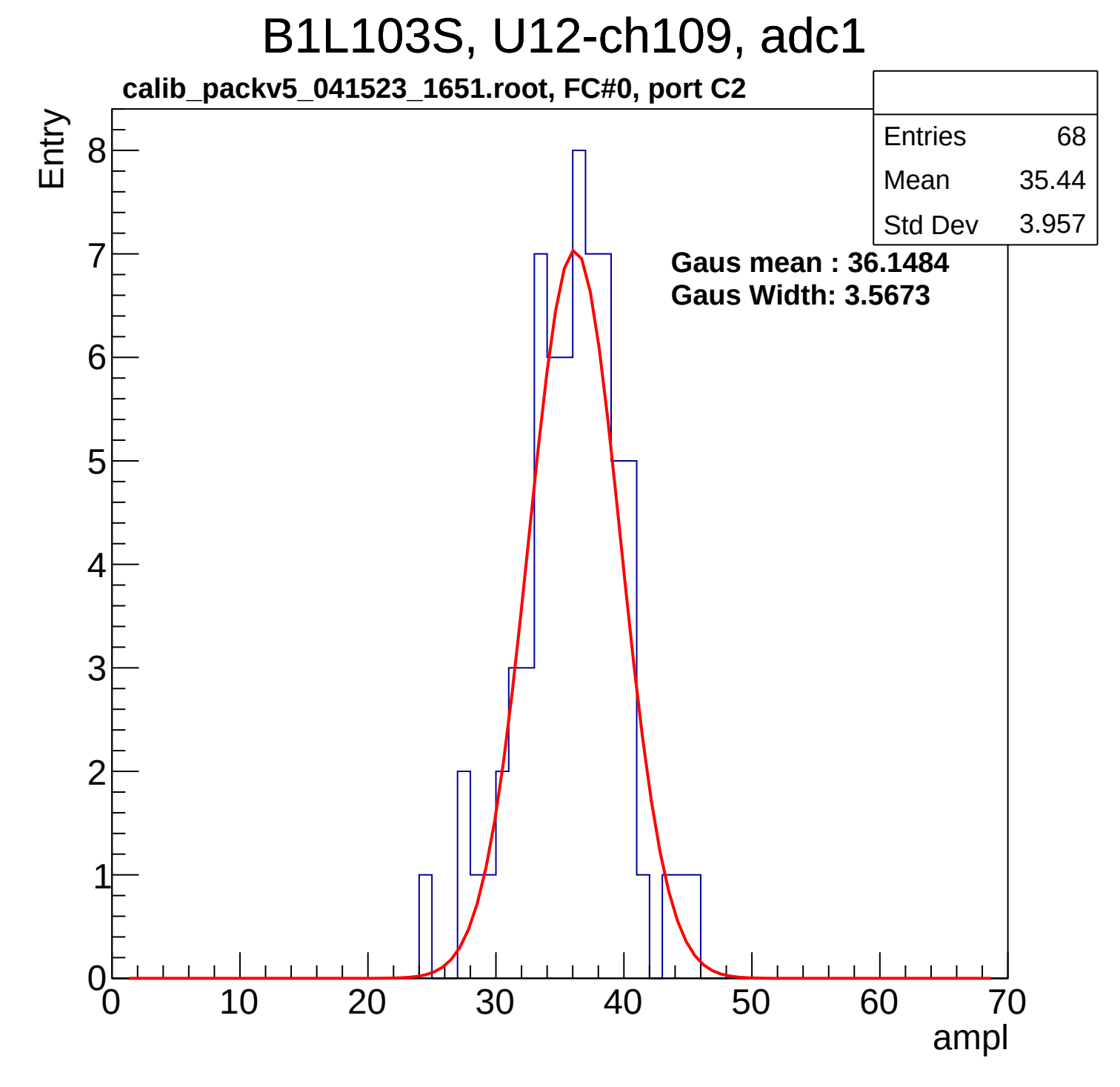
B1L103S, U12-ch109, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 35.44
Std Dev 3.957
Gaus mean : 36.1484
Gaus Width: 3.5673
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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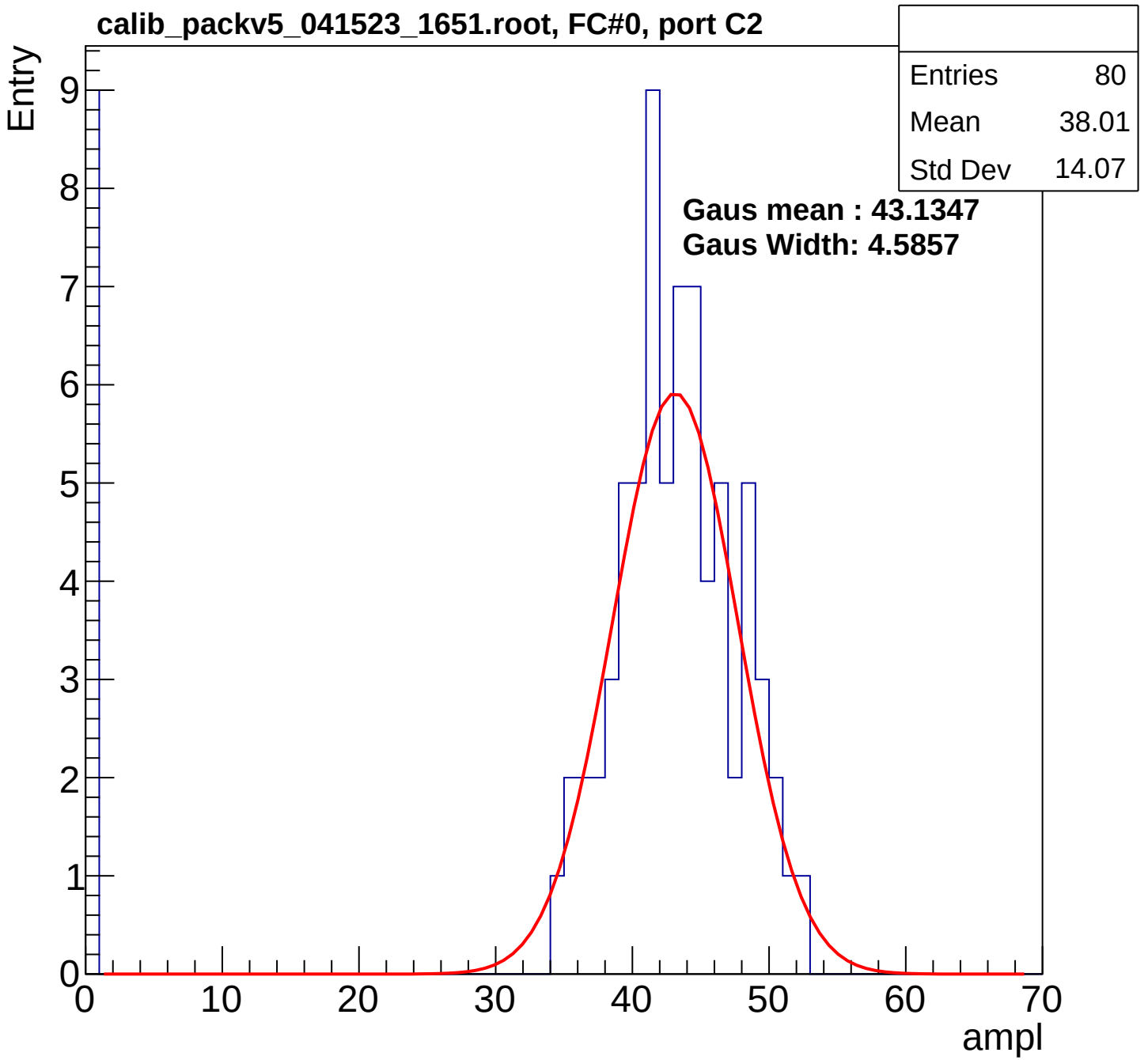
B1L103S, U12-ch109, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 80
Mean 38.01
Std Dev 14.07
Gaus mean : 43.1347
Gaus Width: 4.5857
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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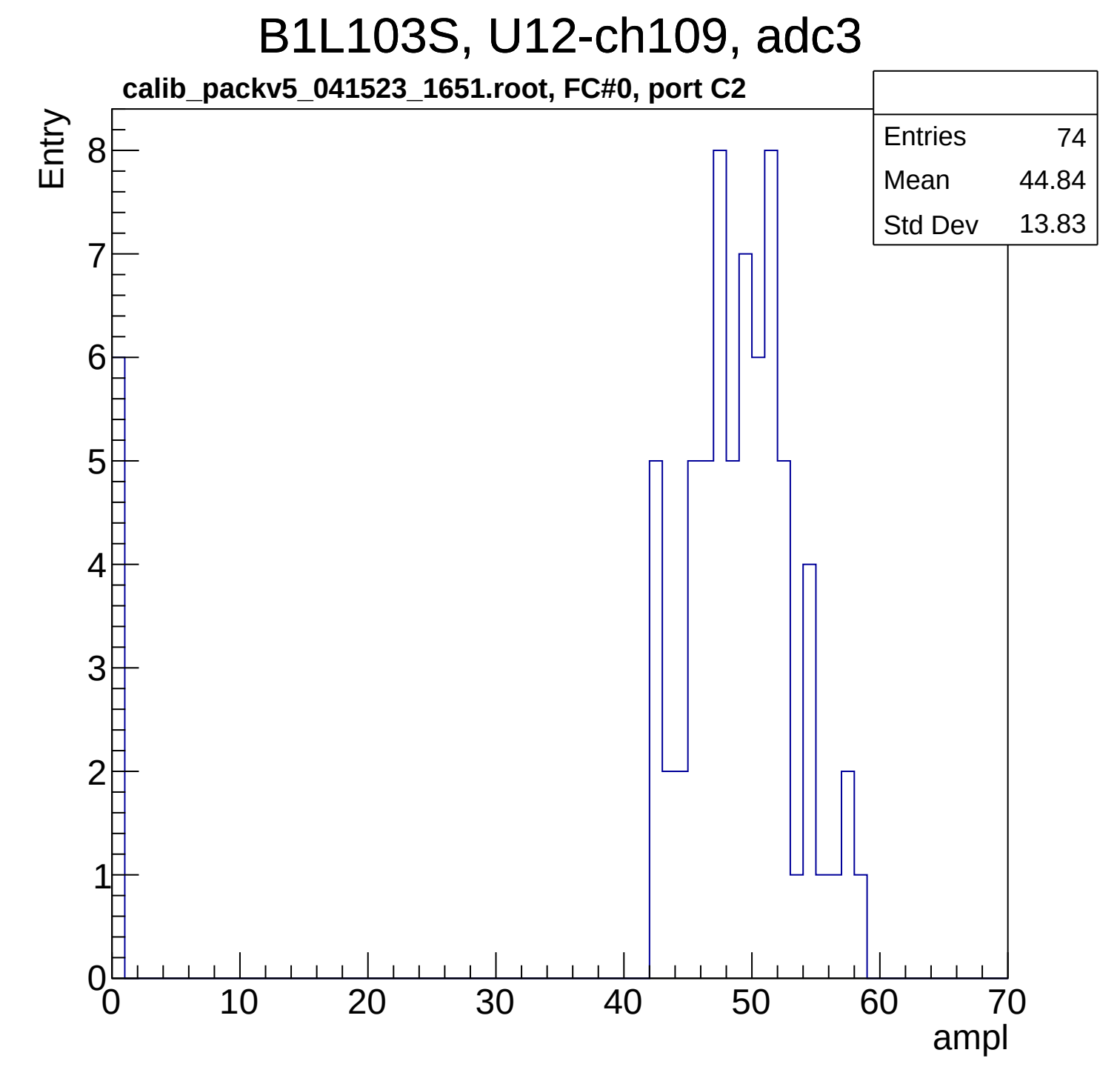
B1L103S, U12-ch109, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 44.84
Std Dev 13.83
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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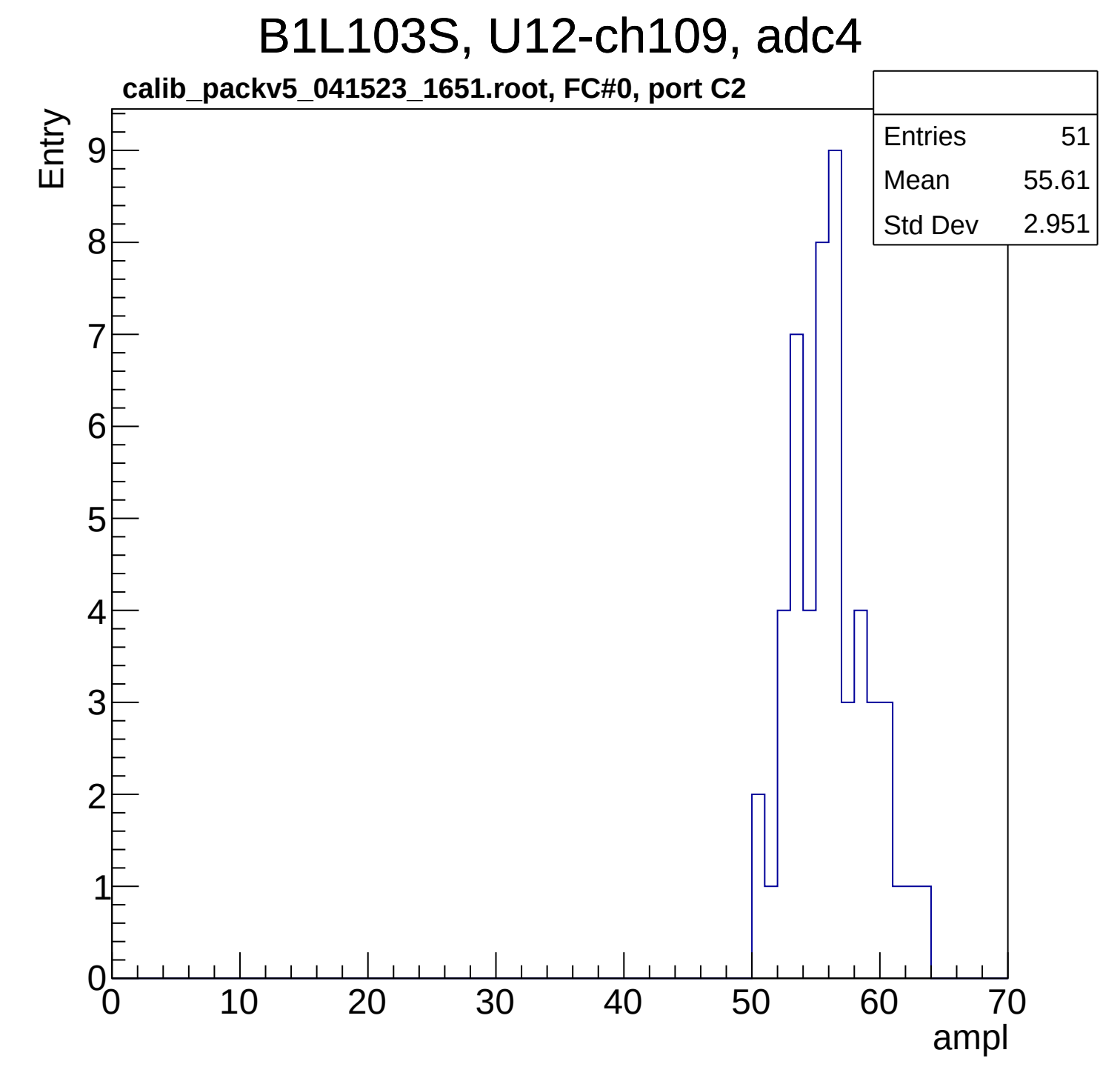
B1L103S, U12-ch109, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 55.61
Std Dev 2.951
Entry
ampl
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2
3
4
5
6
7
8
9
0
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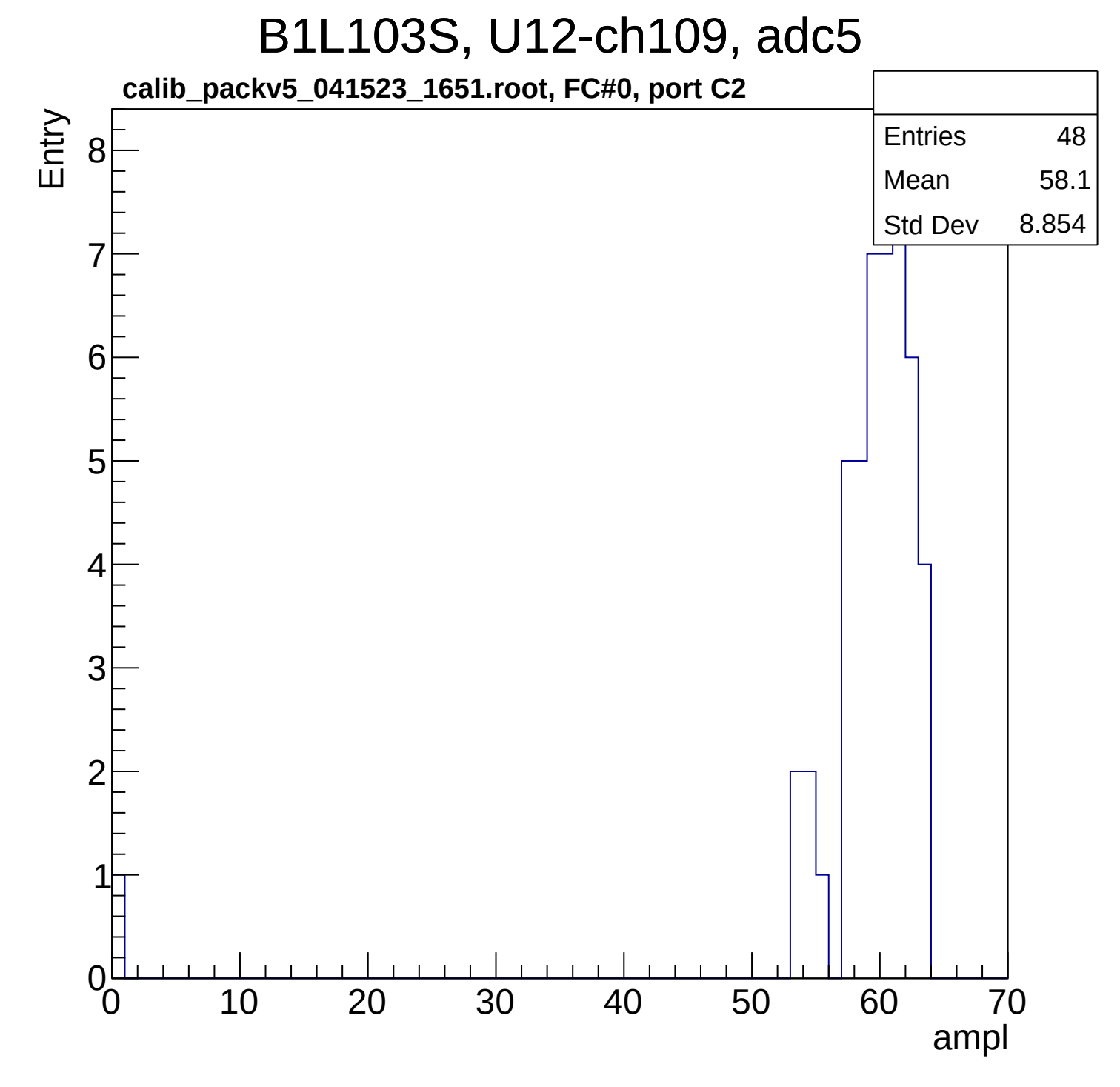
B1L103S, U12-ch109, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.1
Std Dev 8.854
Entry
ampl
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2
3
4
5
6
7
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0
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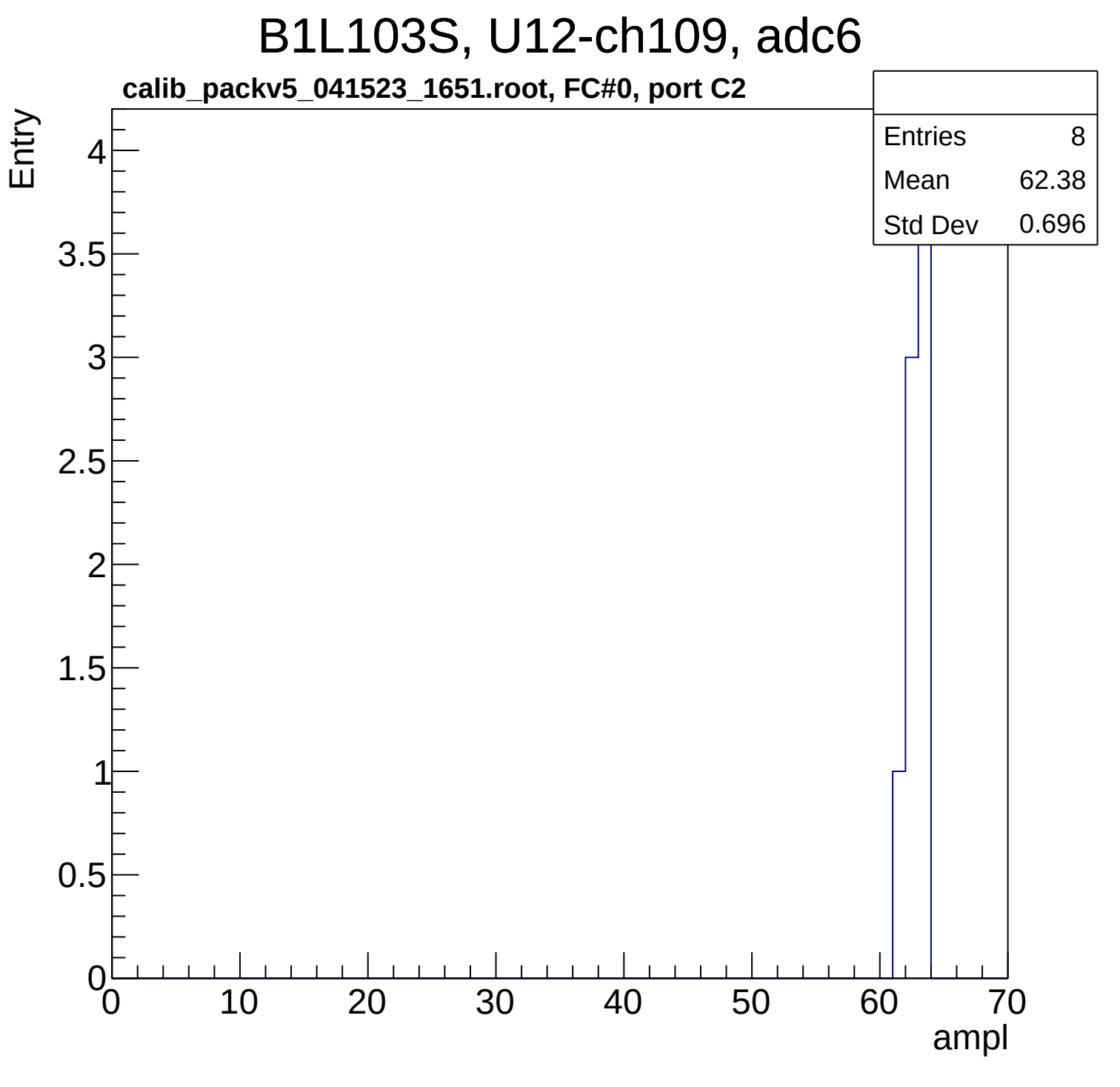
B1L103S, U12-ch109, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 62.38
Std Dev 0.696
Entry
ampl
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0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
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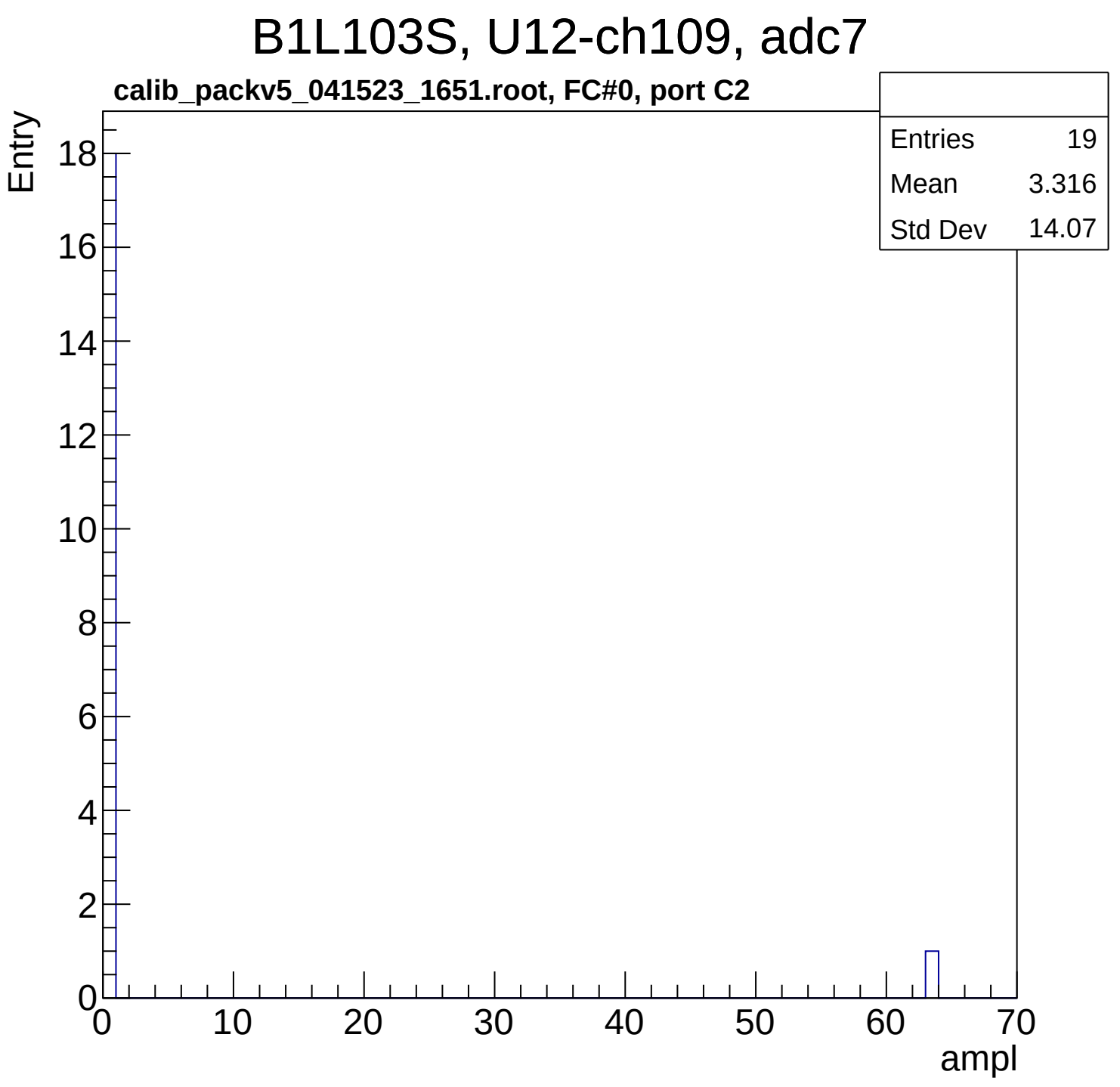
B1L103S, U12-ch109, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 3.316
Std Dev 14.07
Entry
0
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4
6
8
10
12
14
16
18
0
10
20
30
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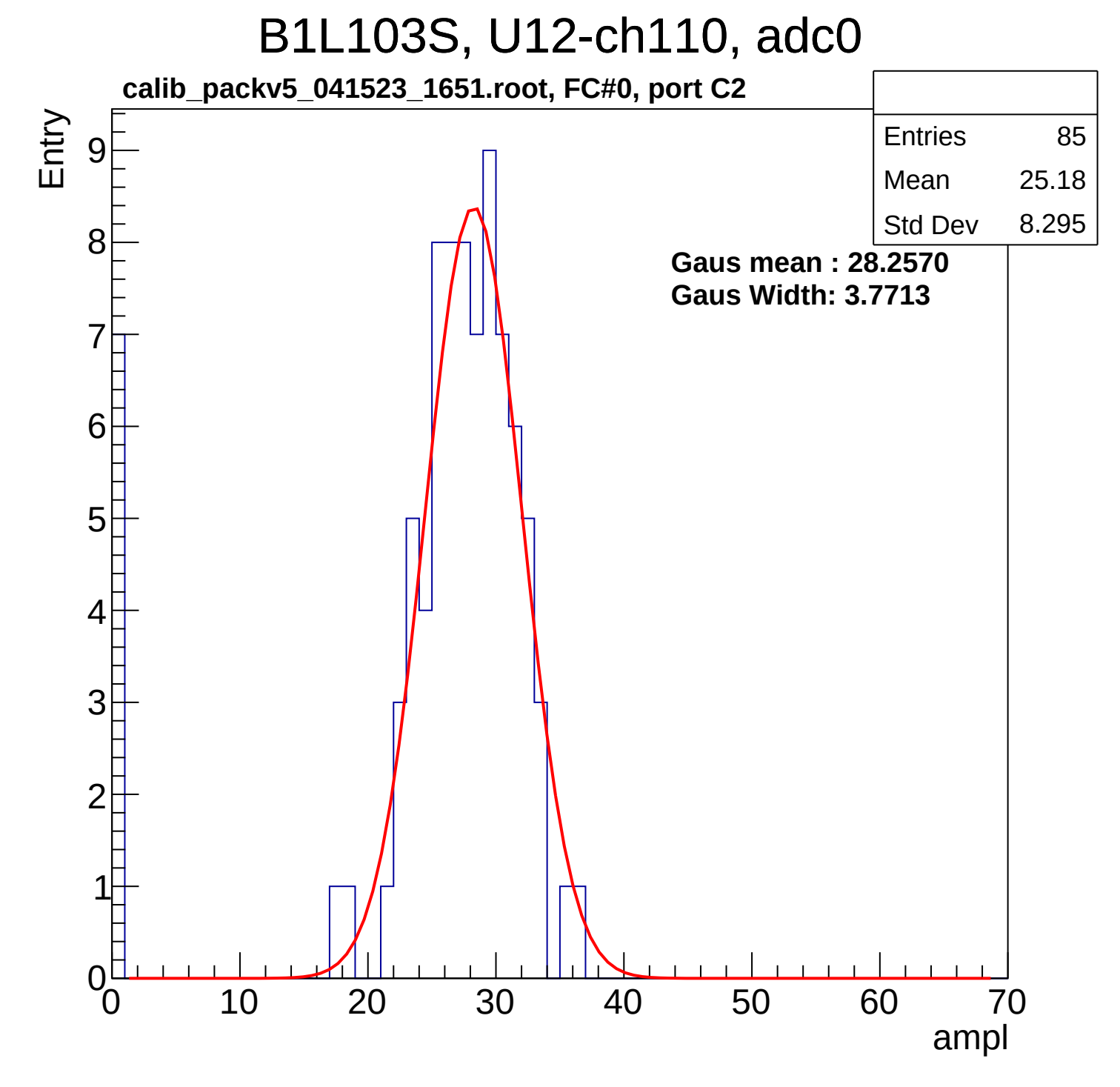
50
60
70
ampl


B1L103S, U12-ch110, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 25.18
Std Dev 8.295
Gaus mean : 28.2570
Gaus Width: 3.7713
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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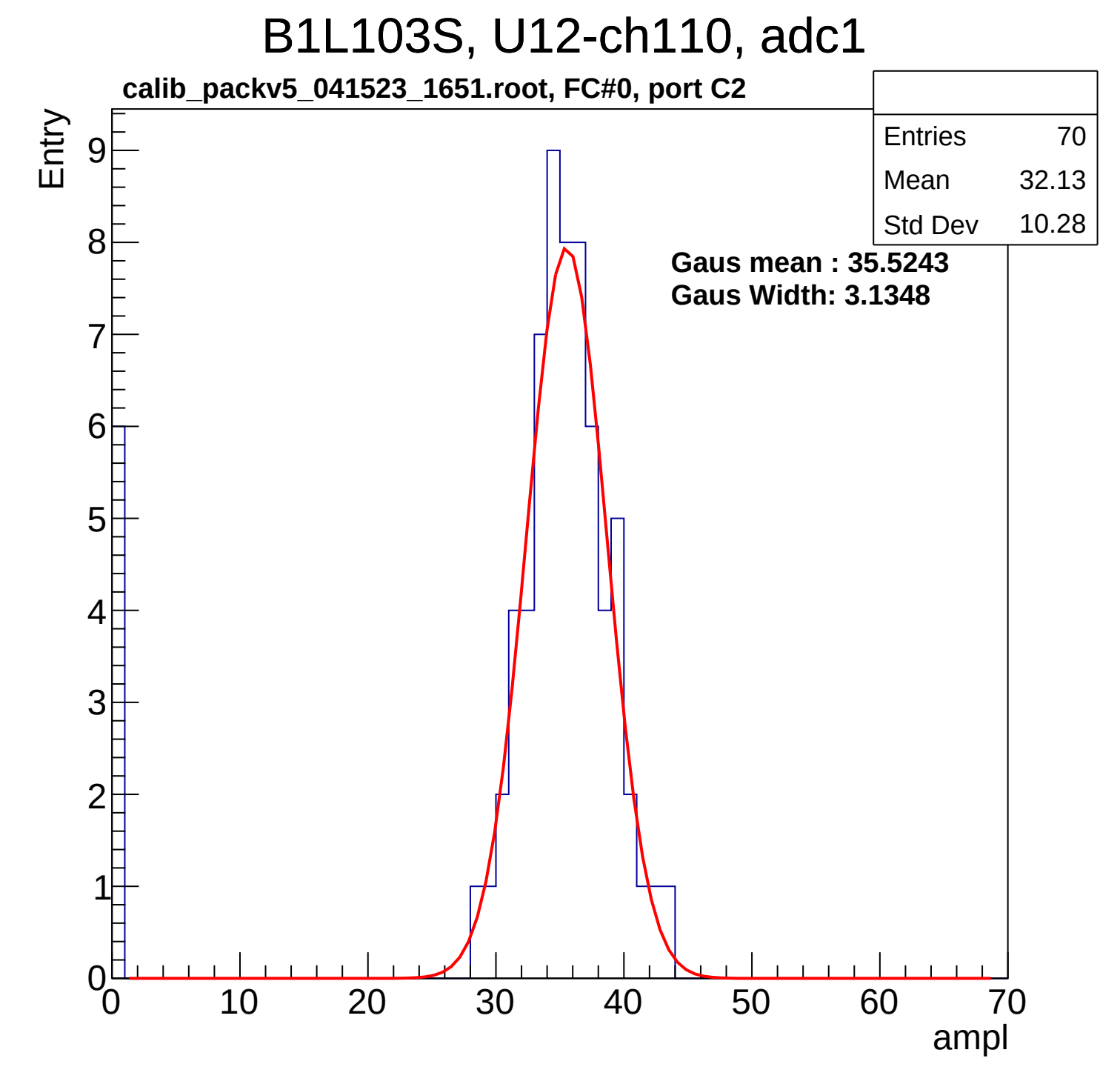
B1L103S, U12-ch110, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 32.13
Std Dev 10.28
Gaus mean : 35.5243
Gaus Width: 3.1348
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
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40
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60
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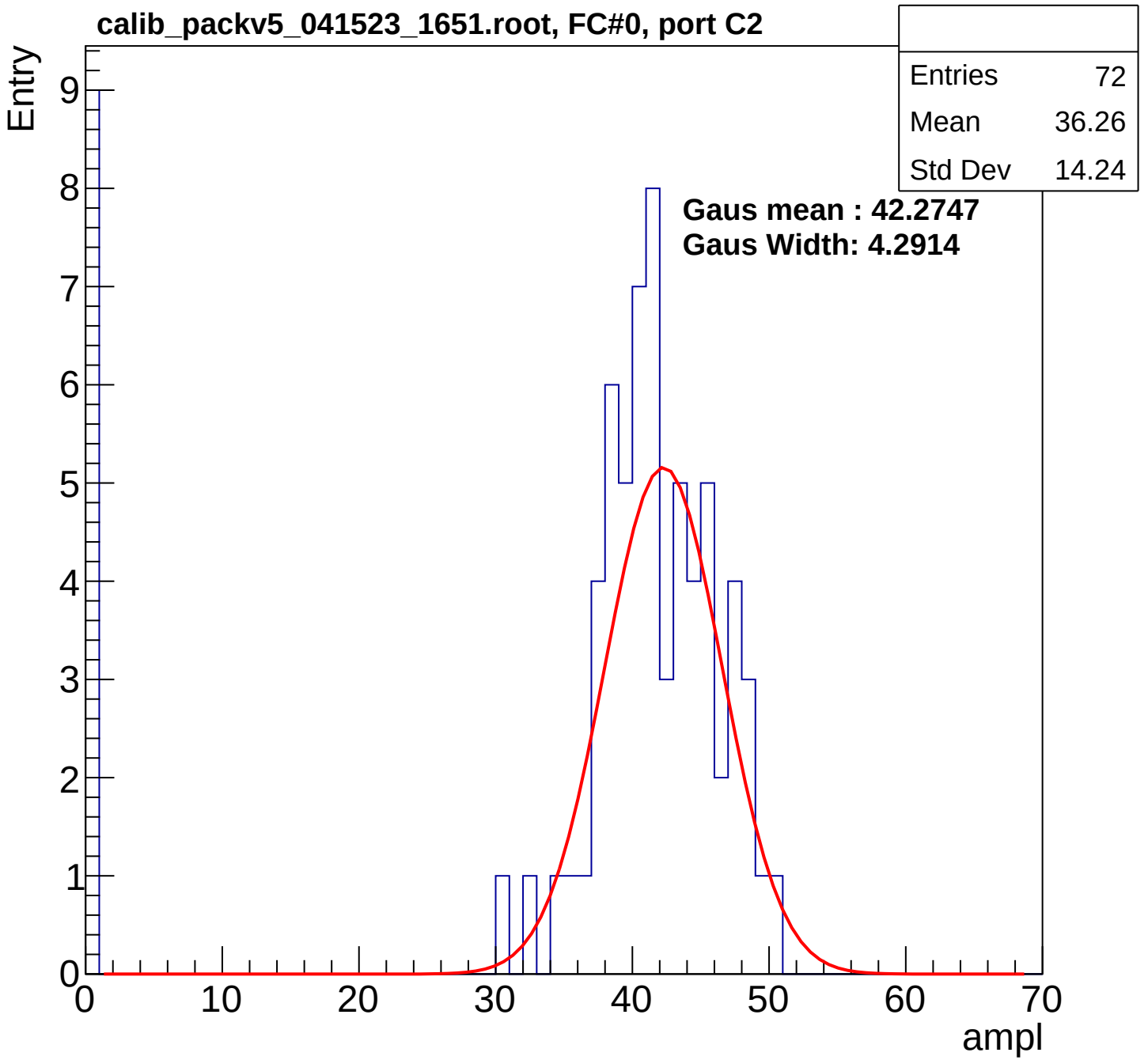
B1L103S, U12-ch110, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 72
Mean 36.26
Std Dev 14.24
Gaus mean : 42.2747
Gaus Width: 4.2914
Entry
ampl
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2
3
4
5
6
7
8
9
0
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20
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40
50
60
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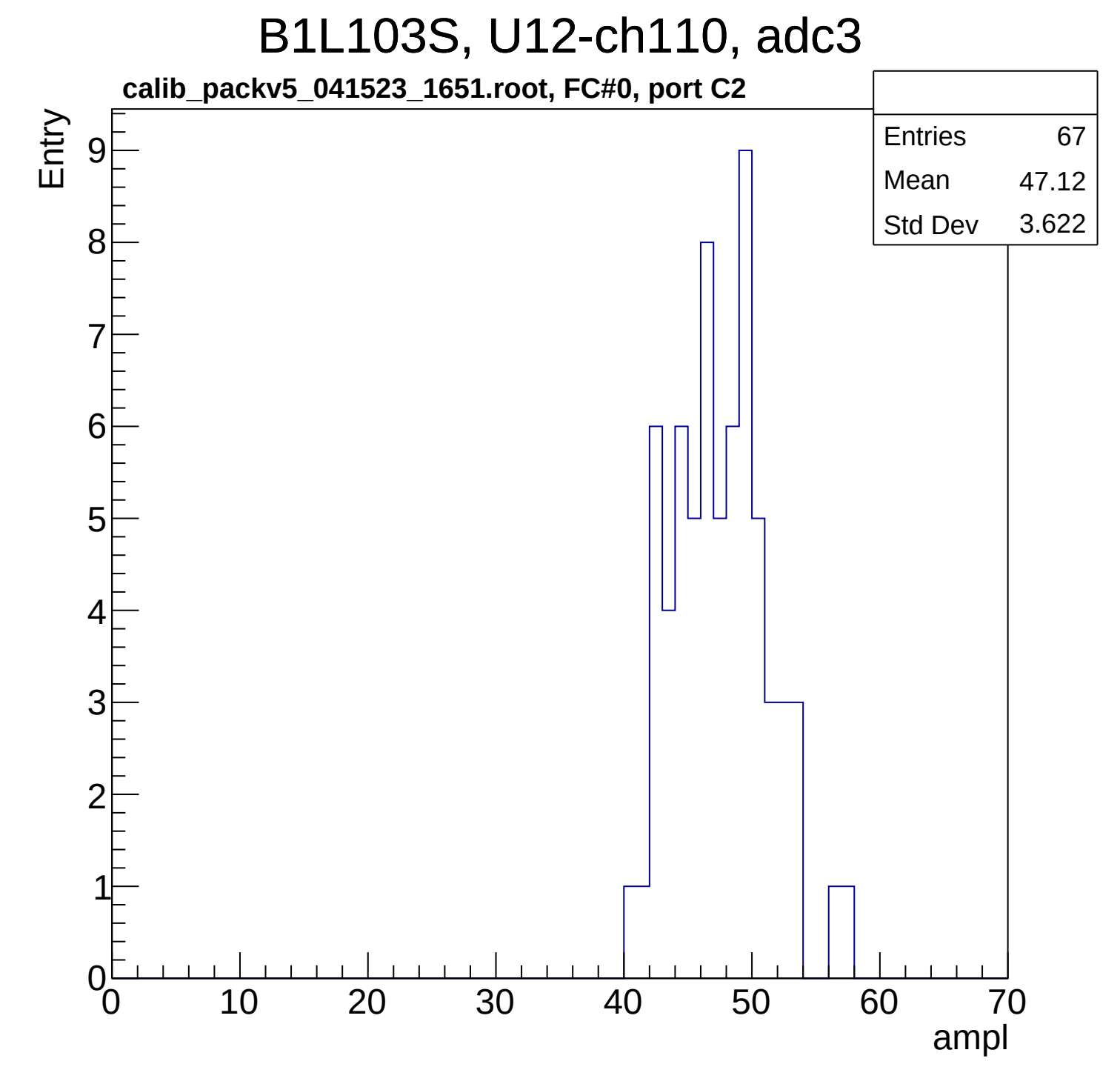
B1L103S, U12-ch110, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 47.12
Std Dev 3.622
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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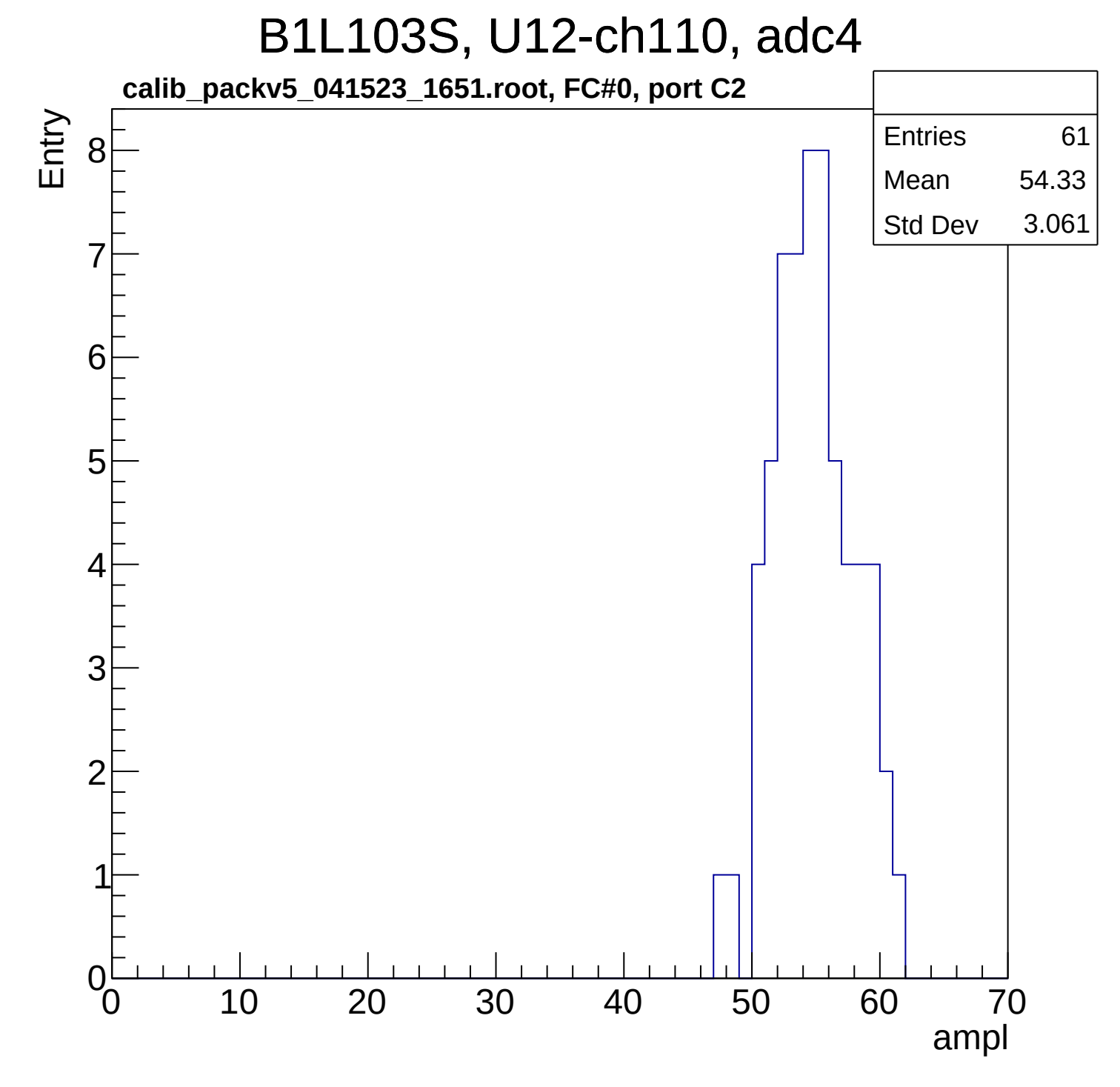
B1L103S, U12-ch110, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 54.33
Std Dev 3.061
Entry
ampl
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2
3
4
5
6
7
8
0
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20
30
40
50
60
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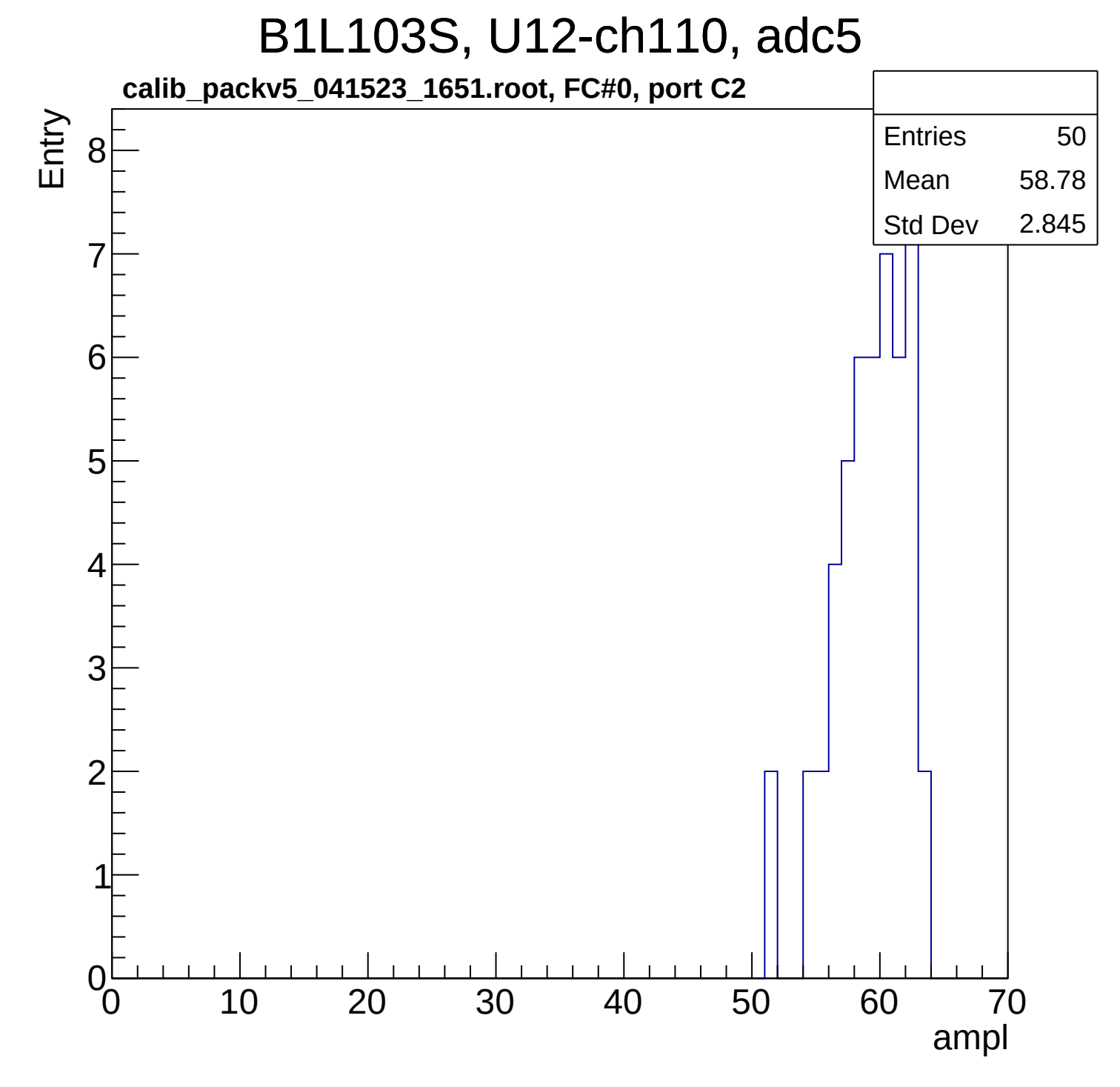
B1L103S, U12-ch110, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 58.78
Std Dev 2.845
Entry
ampl
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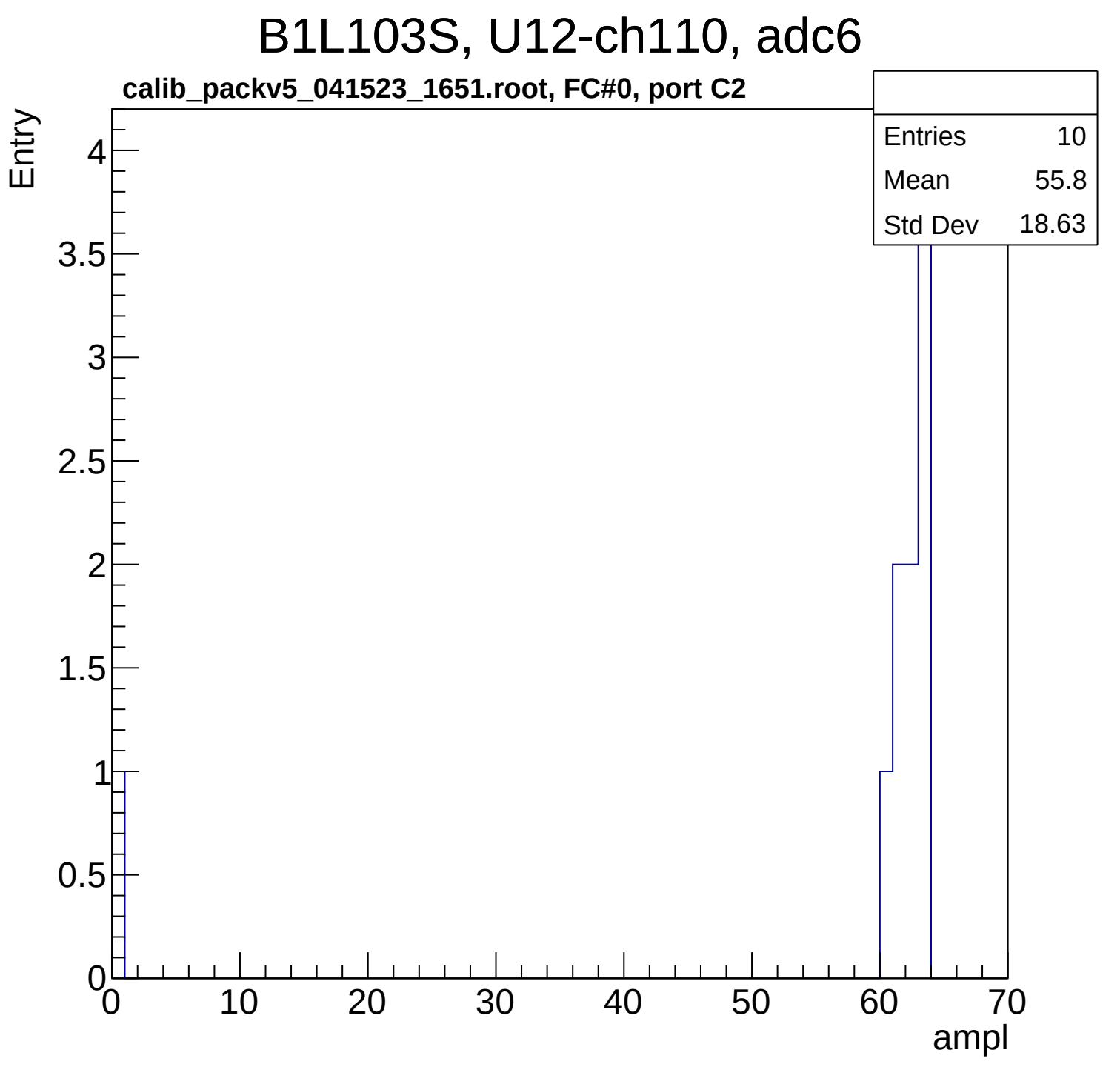
B1L103S, U12-ch110, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.8
Std Dev 18.63
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
10
20
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40
50
60
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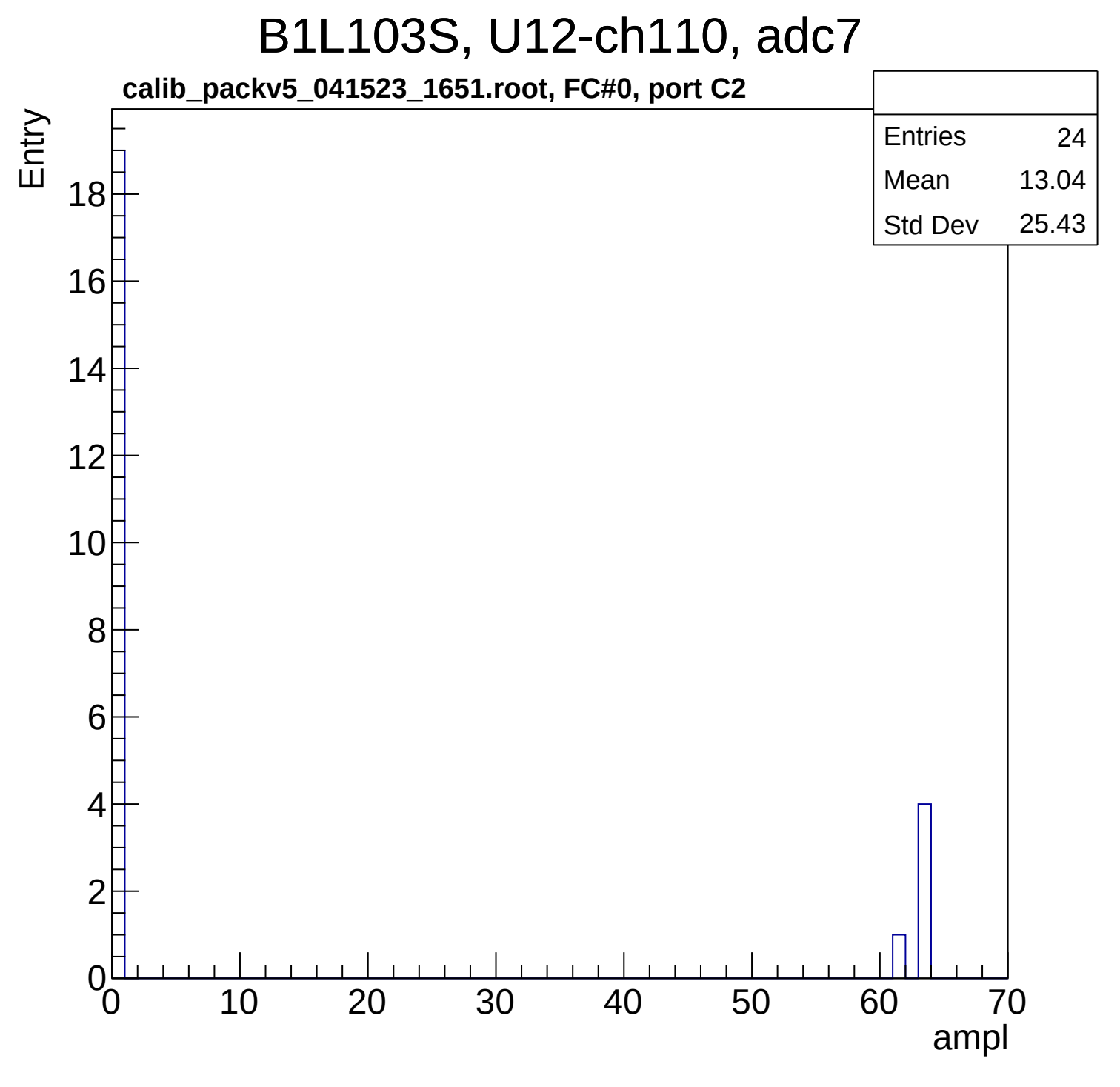
B1L103S, U12-ch110, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 24
Mean 13.04
Std Dev 25.43
Entry
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6
8
10
12
14
16
18
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10
20
30
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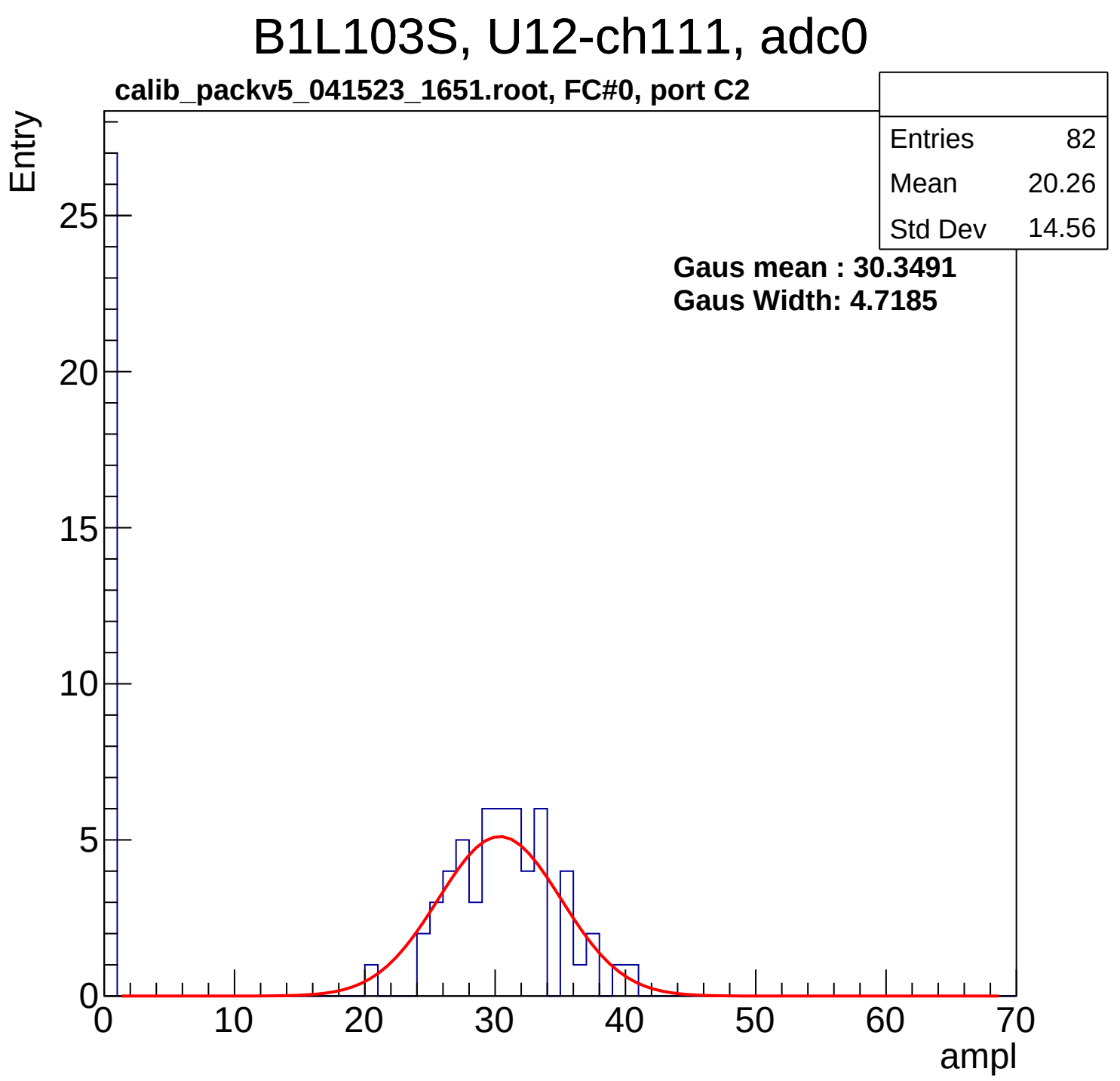
50
60
70
ampl


B1L103S, U12-ch111, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 20.26
Std Dev 14.56
Gaus mean : 30.3491
Gaus Width: 4.7185
Entry
ampl
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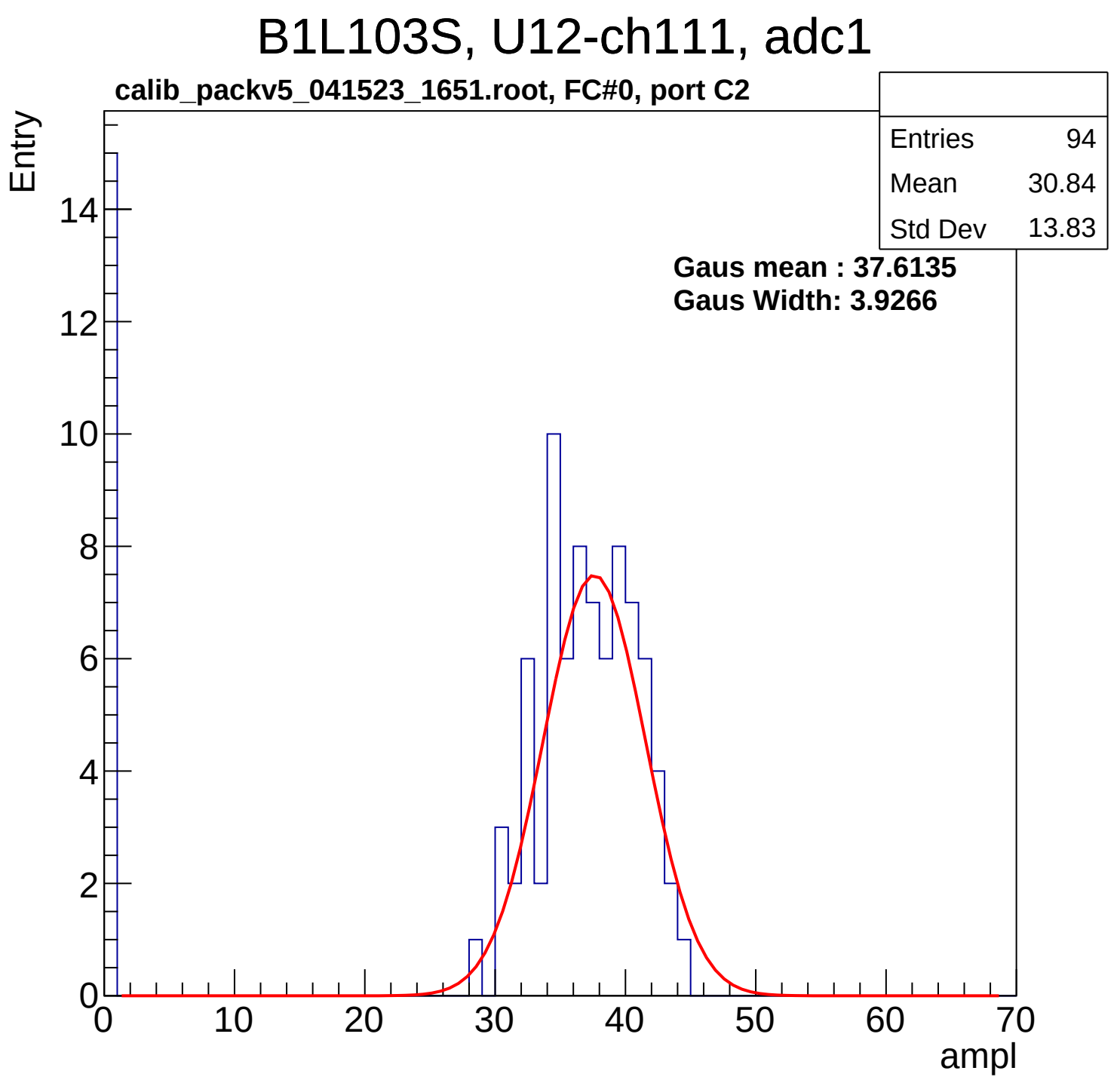
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U12-ch111, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 94
Mean 30.84
Std Dev 13.83
Gaus mean : 37.6135
Gaus Width: 3.9266
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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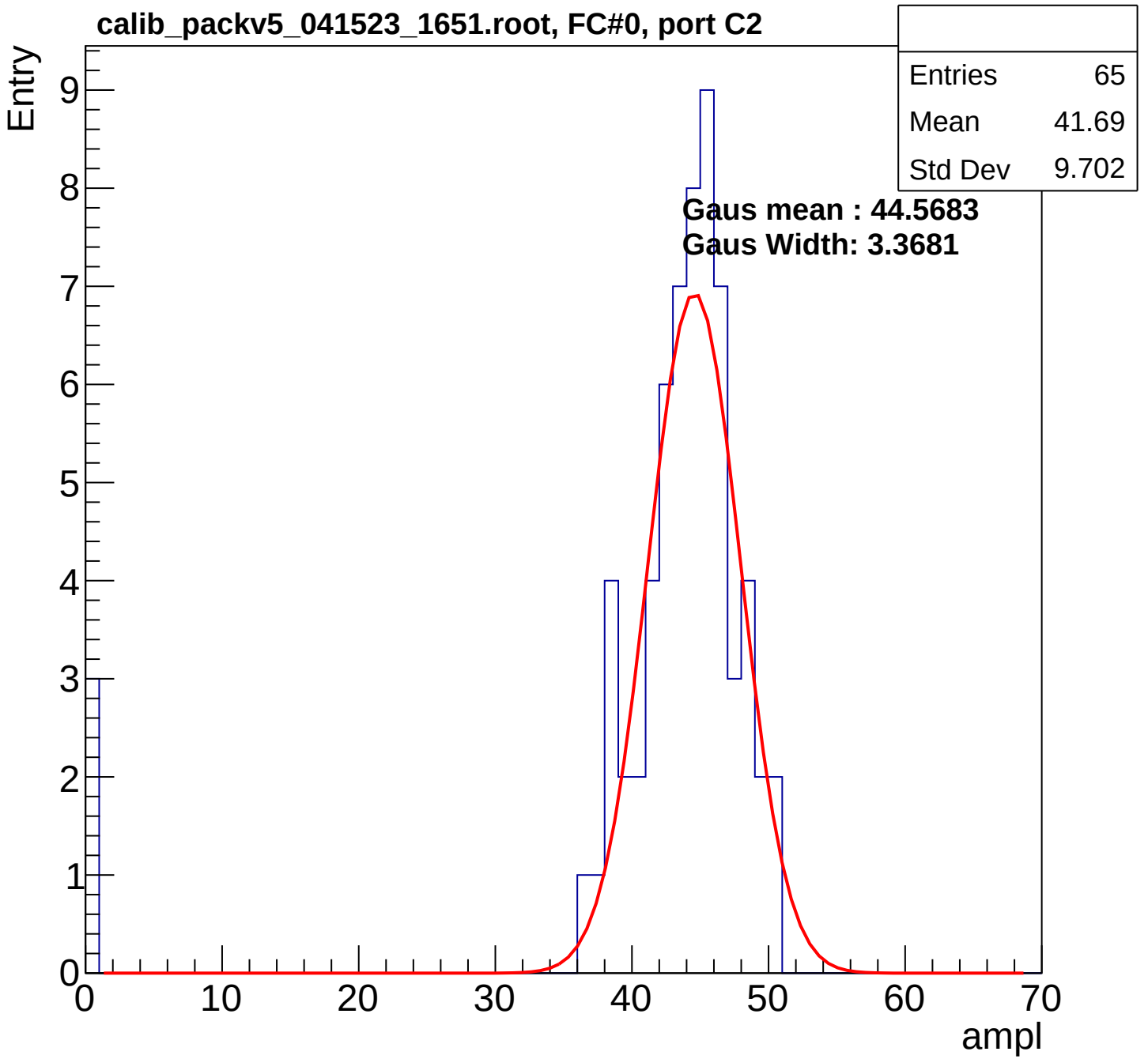
B1L103S, U12-ch111, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 41.69
Std Dev 9.702
Gaus mean : 44.5683
Gaus Width: 3.3681
Entry
ampl
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2
3
4
5
6
7
8
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0
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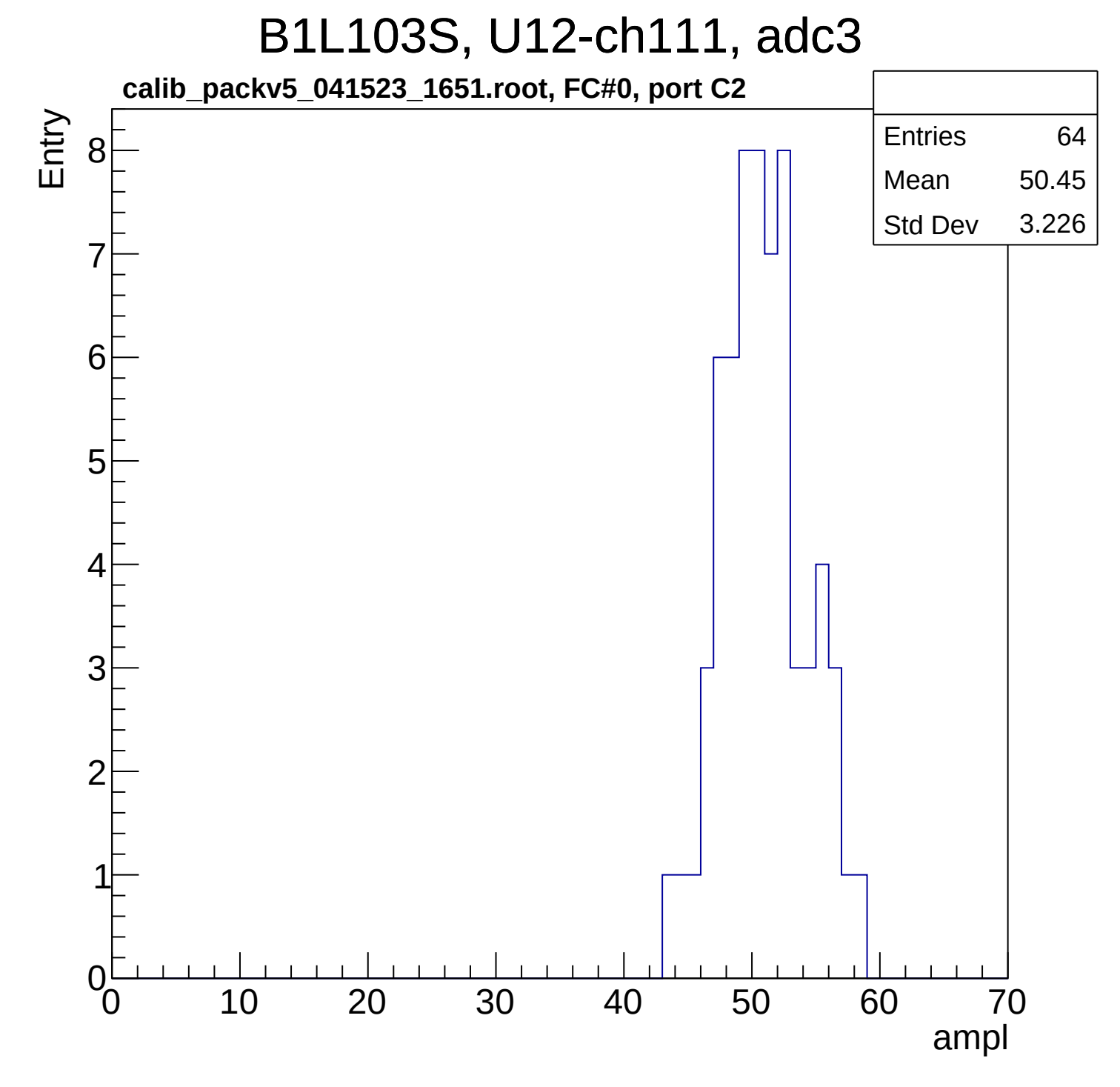
B1L103S, U12-ch111, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 50.45
Std Dev 3.226
Entry
ampl
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4
5
6
7
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0
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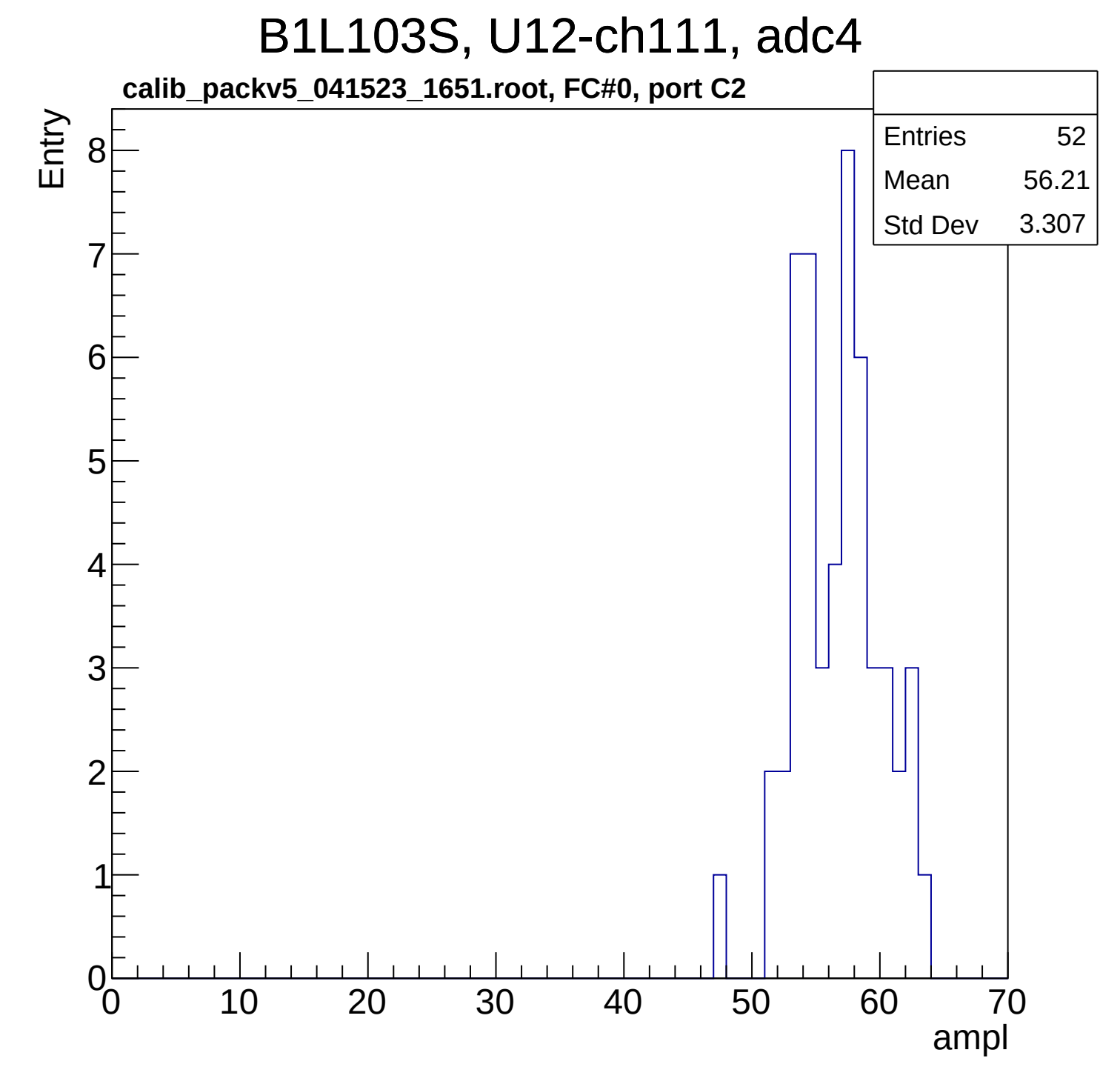
B1L103S, U12-ch111, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 56.21
Std Dev 3.307
Entry
ampl
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7
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0
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20
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40
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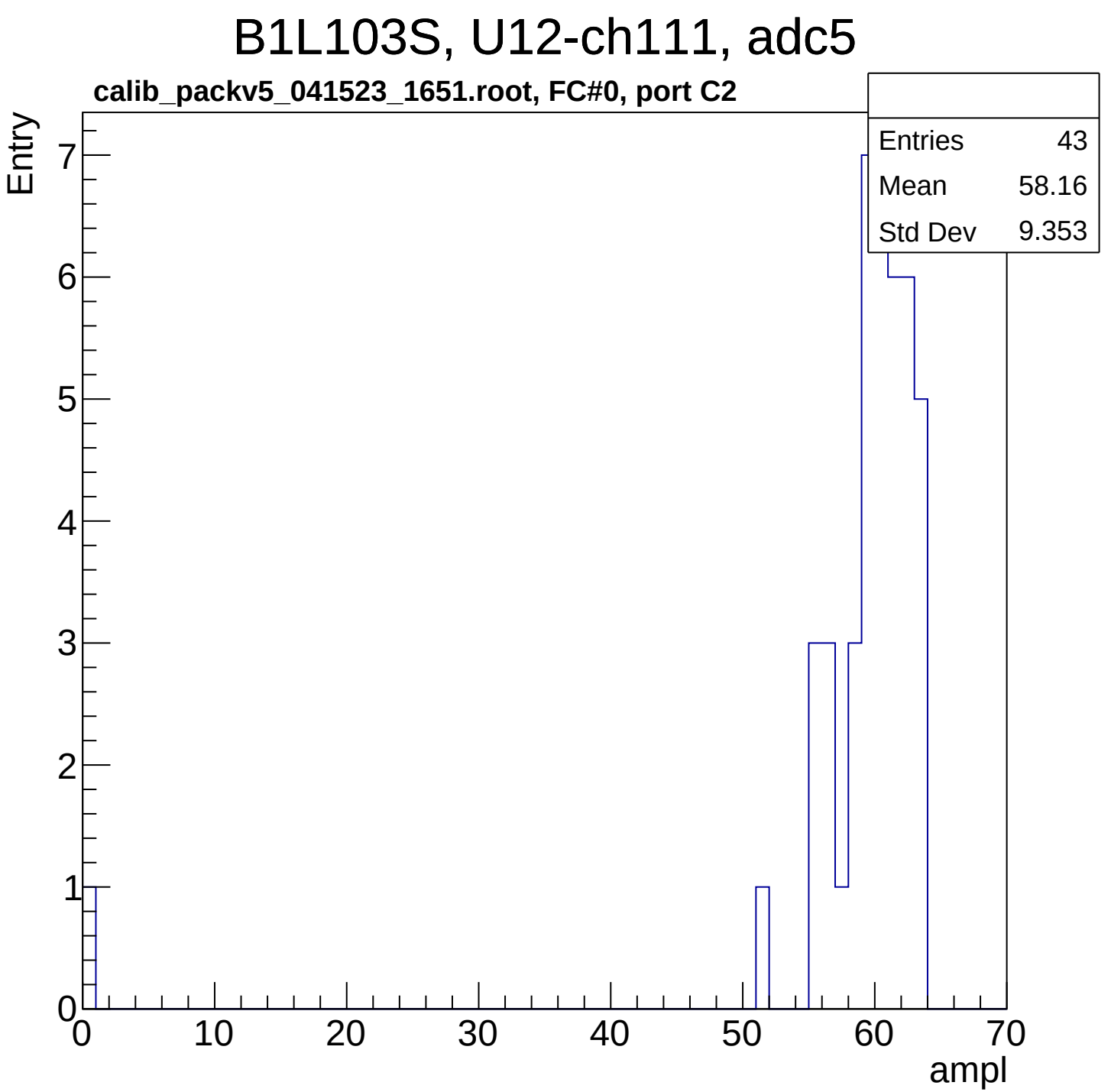
B1L103S, U12-ch111, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 58.16
Std Dev 9.353
Entry
ampl
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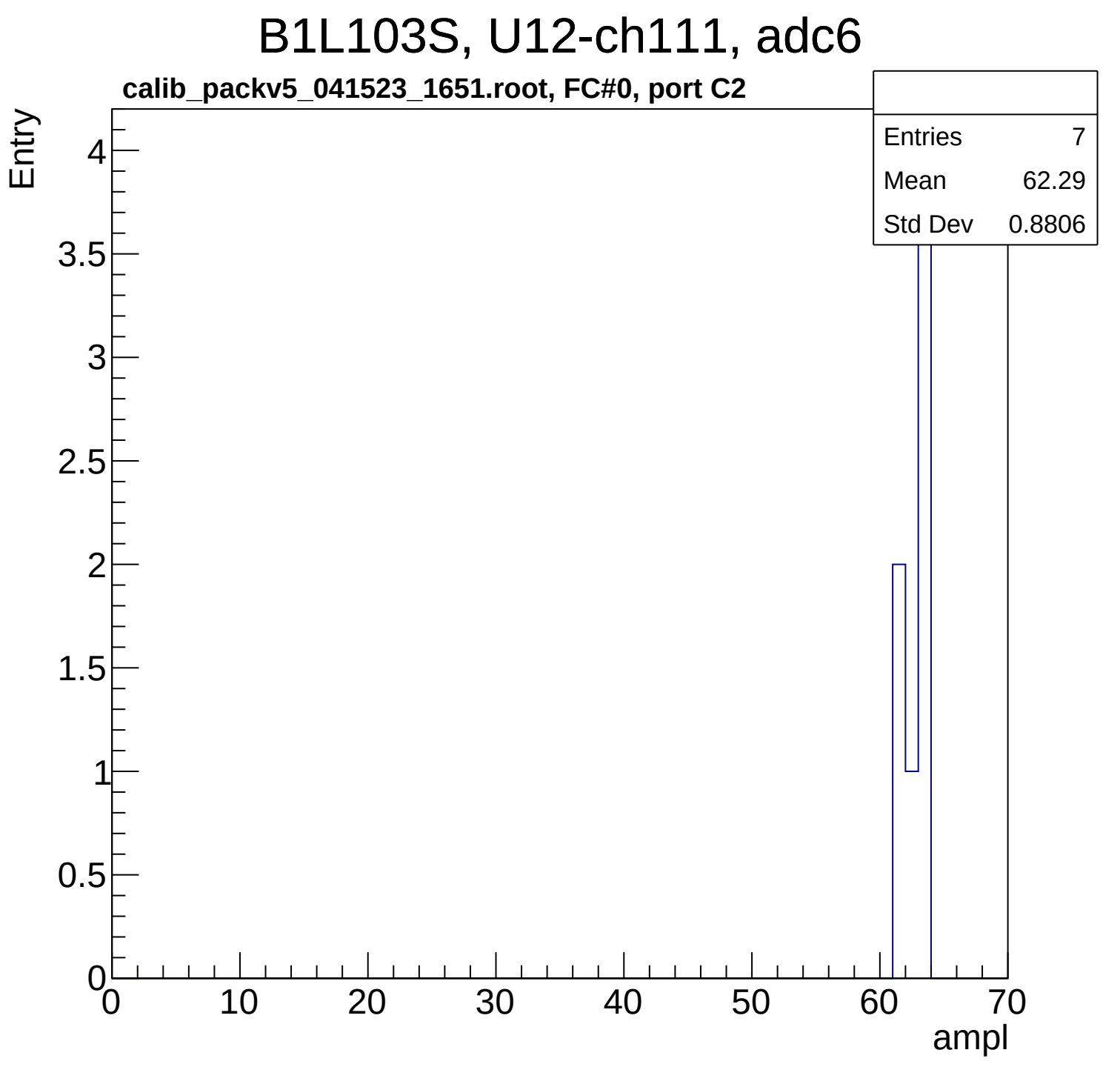
B1L103S, U12-ch111, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 62.29
Std Dev 0.8806
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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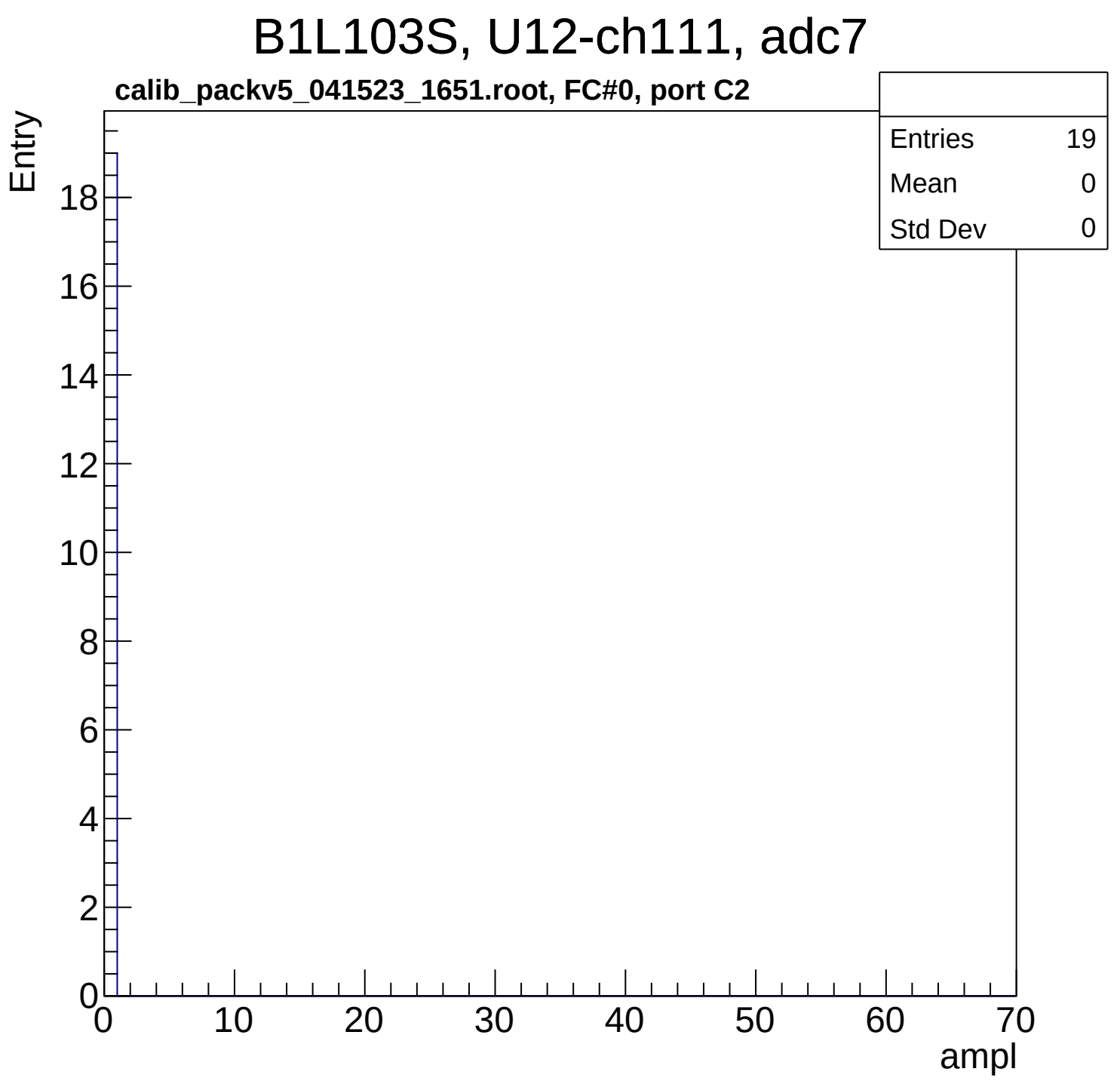
B1L103S, U12-ch111, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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2
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6
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10
12
14
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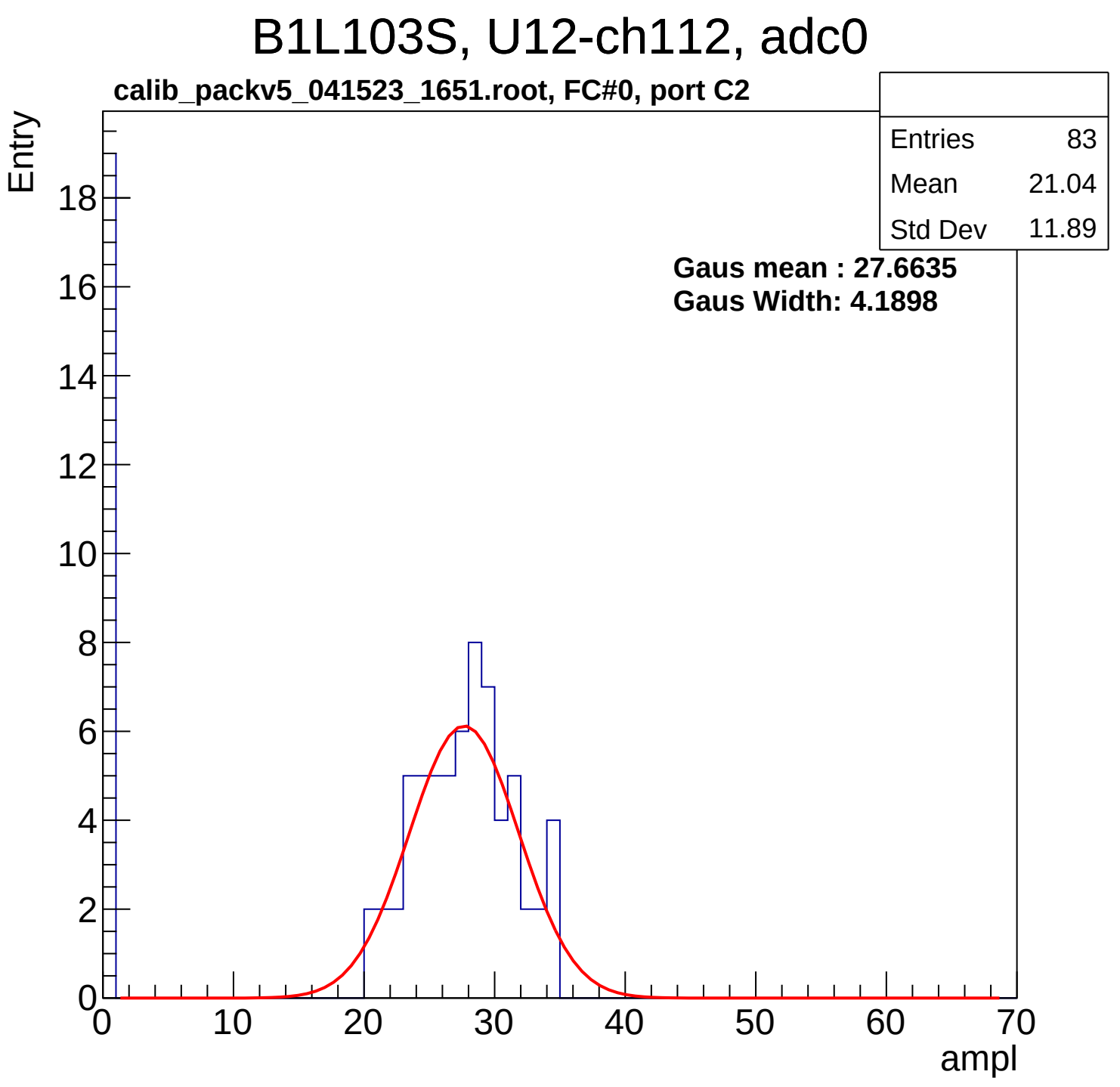
70
ampl


B1L103S, U12-ch112, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 21.04
Std Dev 11.89
Gaus mean : 27.6635
Gaus Width: 4.1898
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
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40
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60
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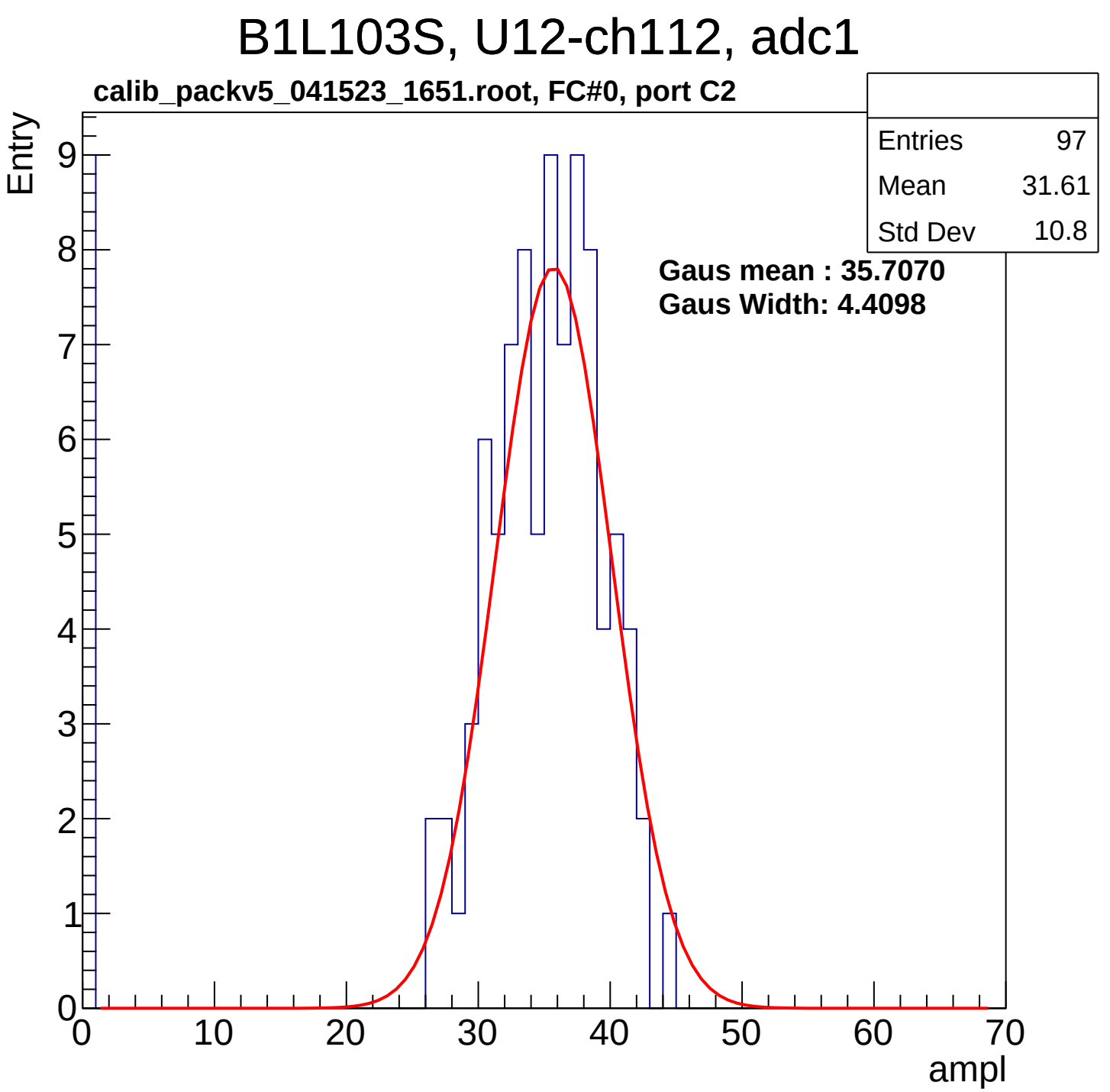
B1L103S, U12-ch112, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 31.61
Std Dev 10.8
Gaus mean : 35.7070
Gaus Width: 4.4098
Entry
ampl
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2
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0
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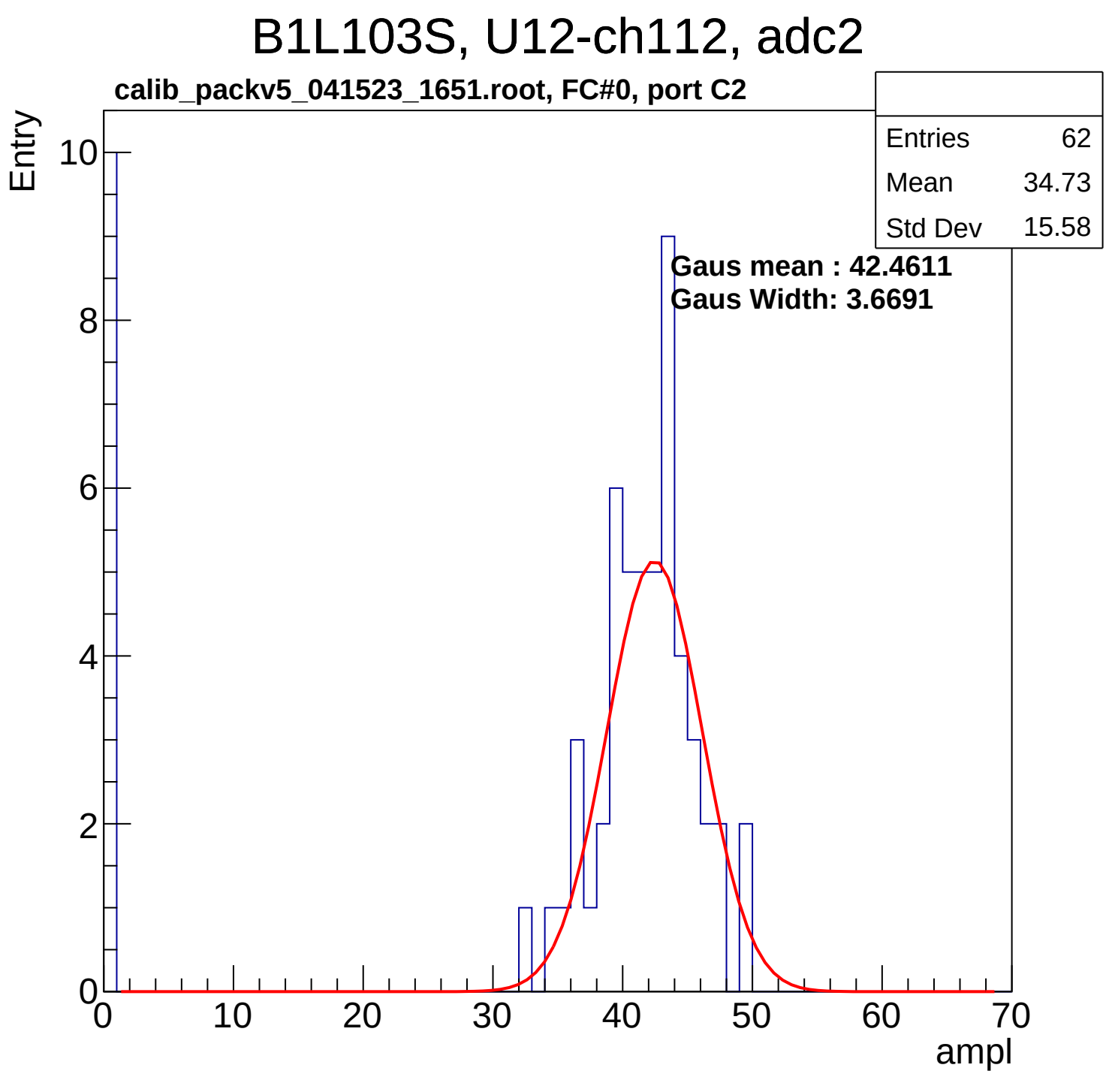
B1L103S, U12-ch112, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 34.73
Std Dev 15.58
Gaus mean : 42.4611
Gaus Width: 3.6691
Entry
ampl
0
2
4
6
8
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0
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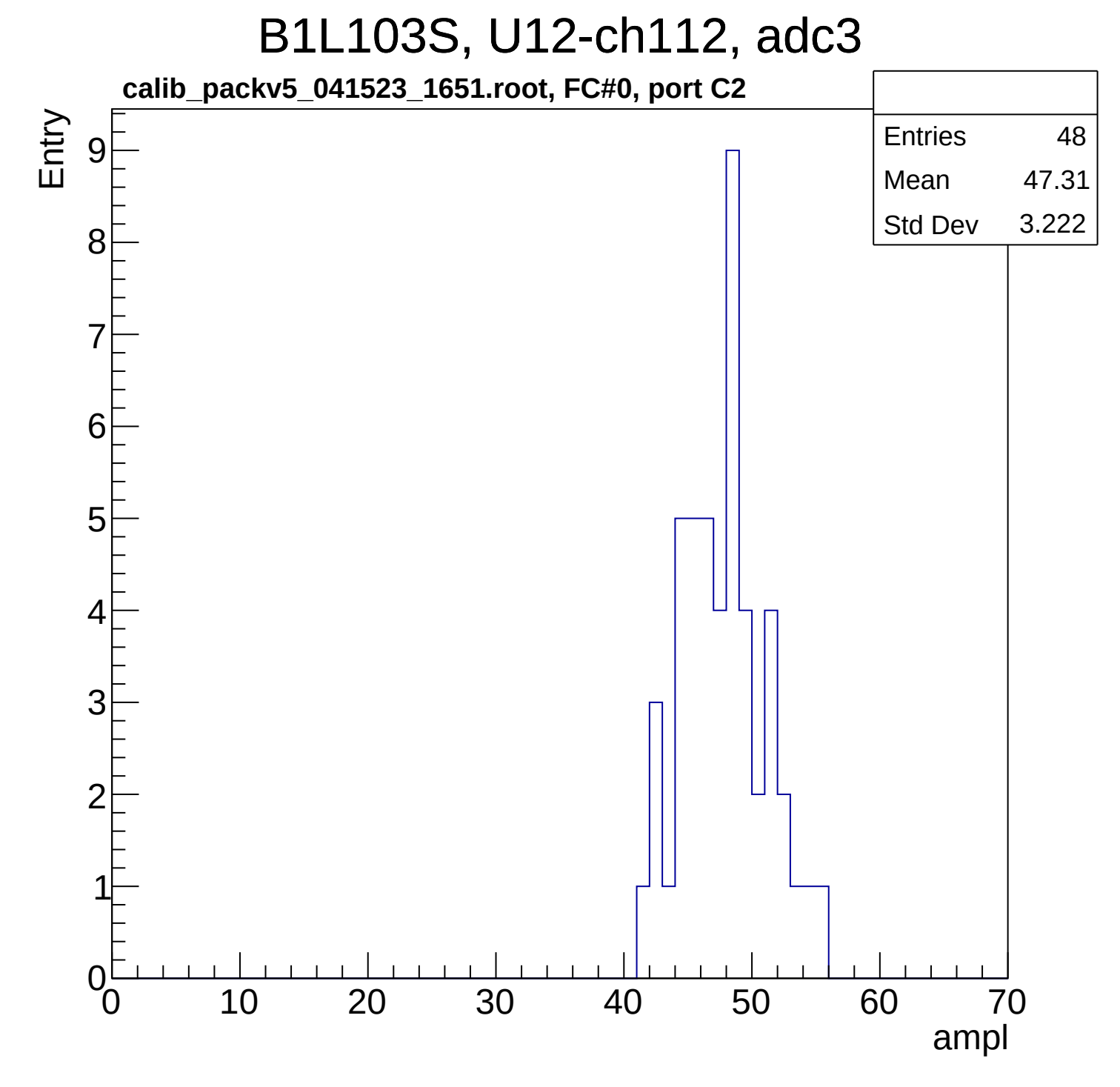
B1L103S, U12-ch112, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 47.31
Std Dev 3.222
Entry
ampl
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2
3
4
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6
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0
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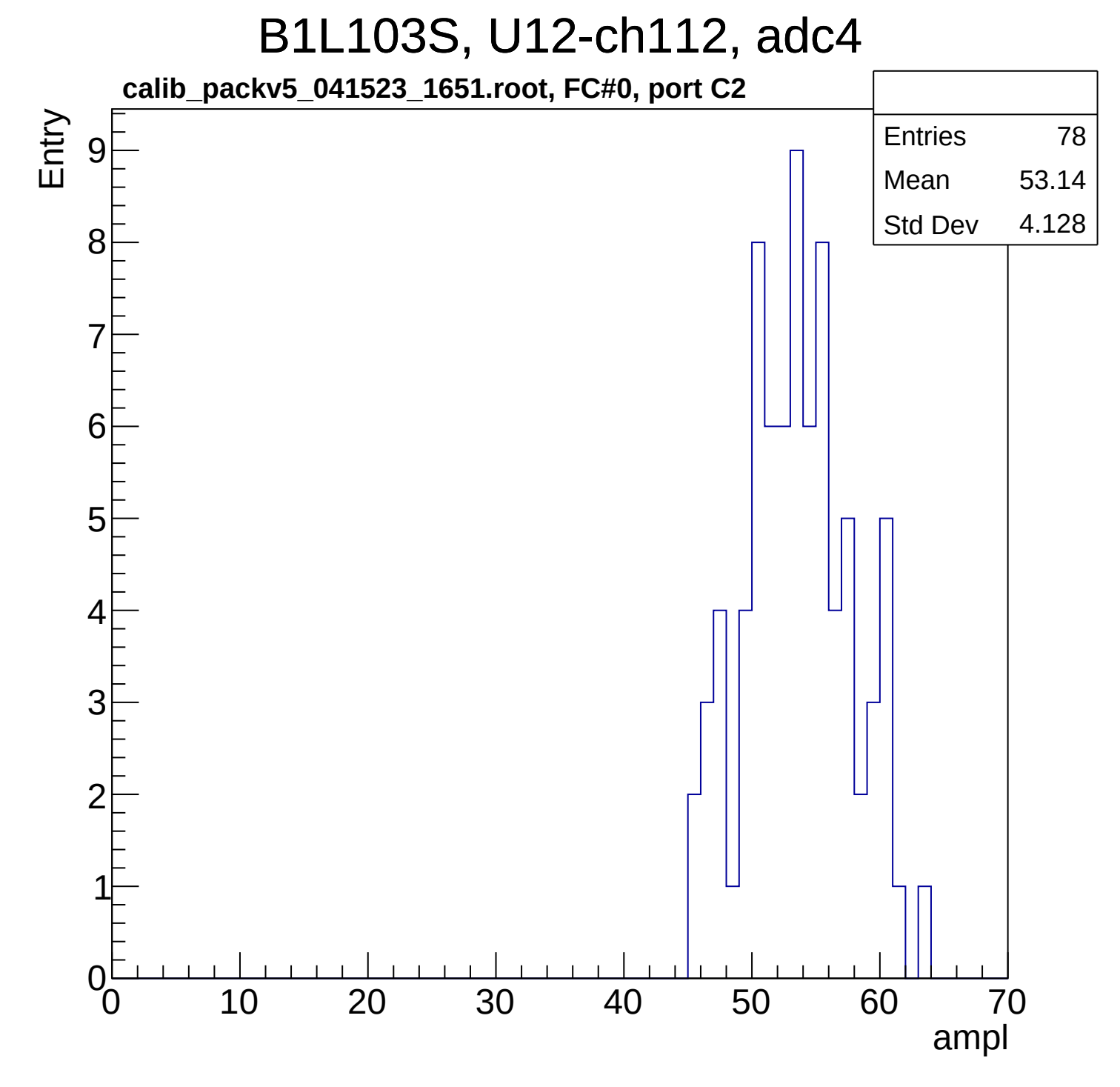
B1L103S, U12-ch112, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 78
Mean 53.14
Std Dev 4.128
Entry
ampl
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3
4
5
6
7
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0
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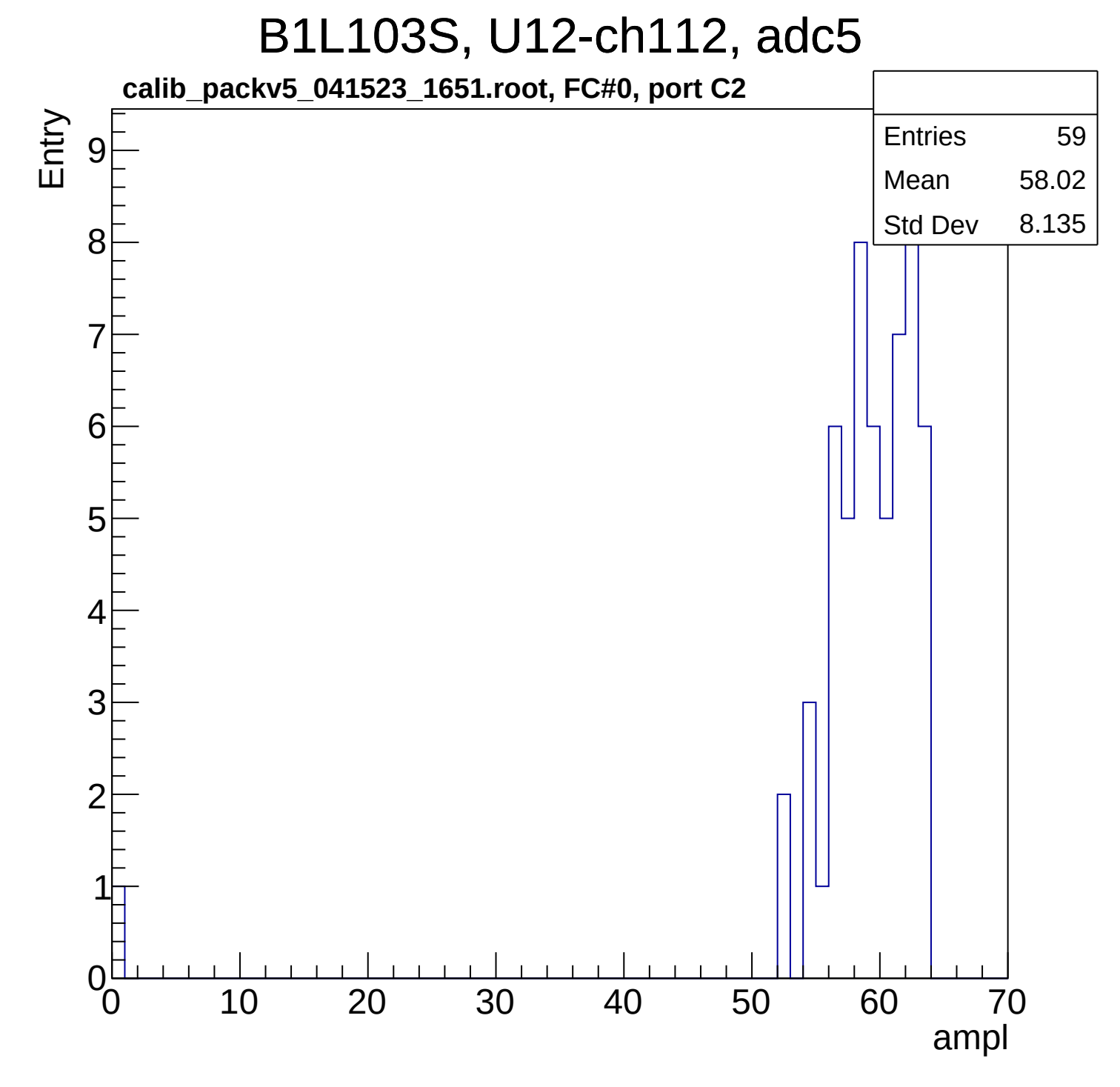
B1L103S, U12-ch112, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 59
Mean 58.02
Std Dev 8.135
Entry
ampl
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2
3
4
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6
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8
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0
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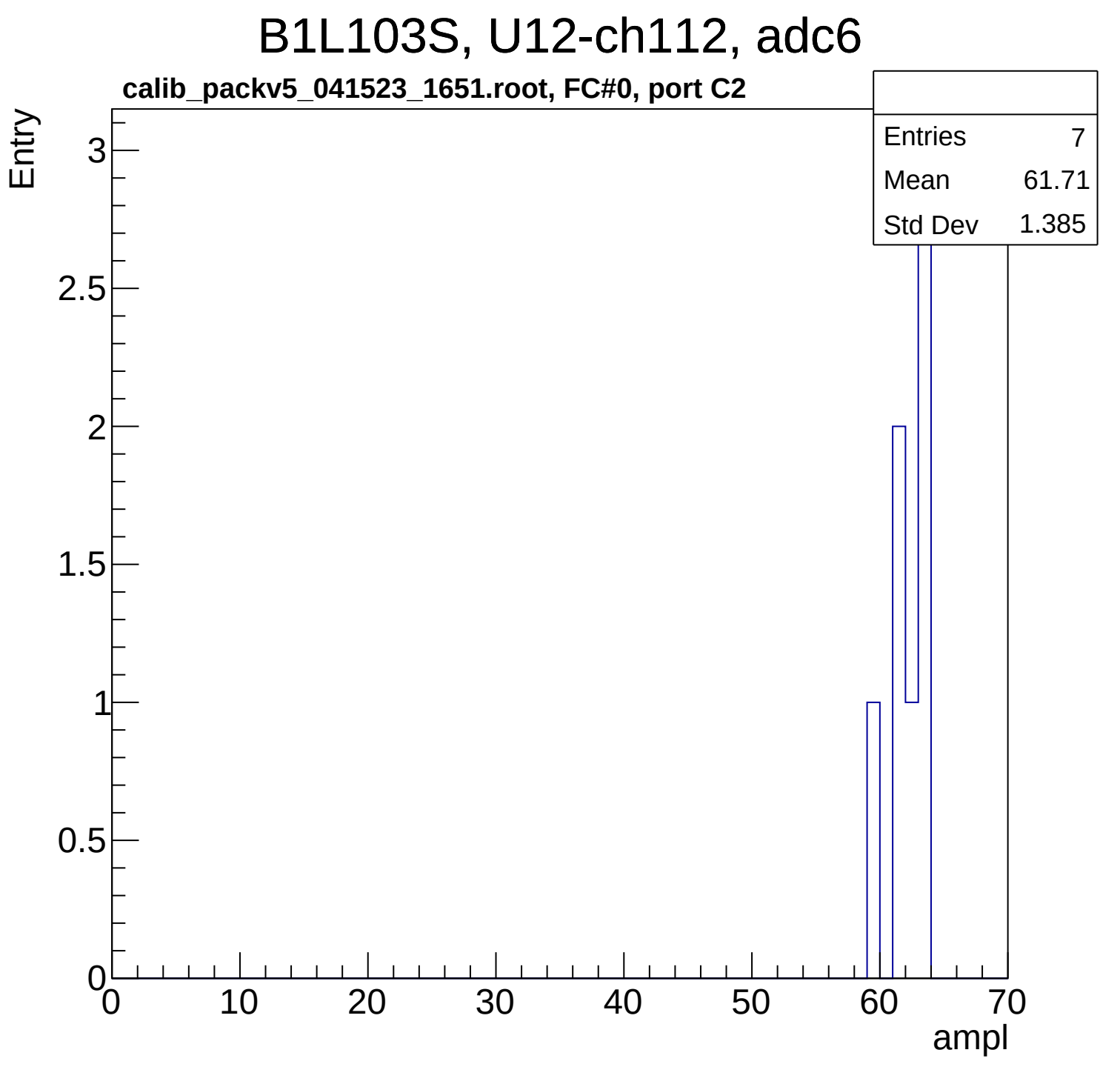
B1L103S, U12-ch112, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.71
Std Dev 1.385
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
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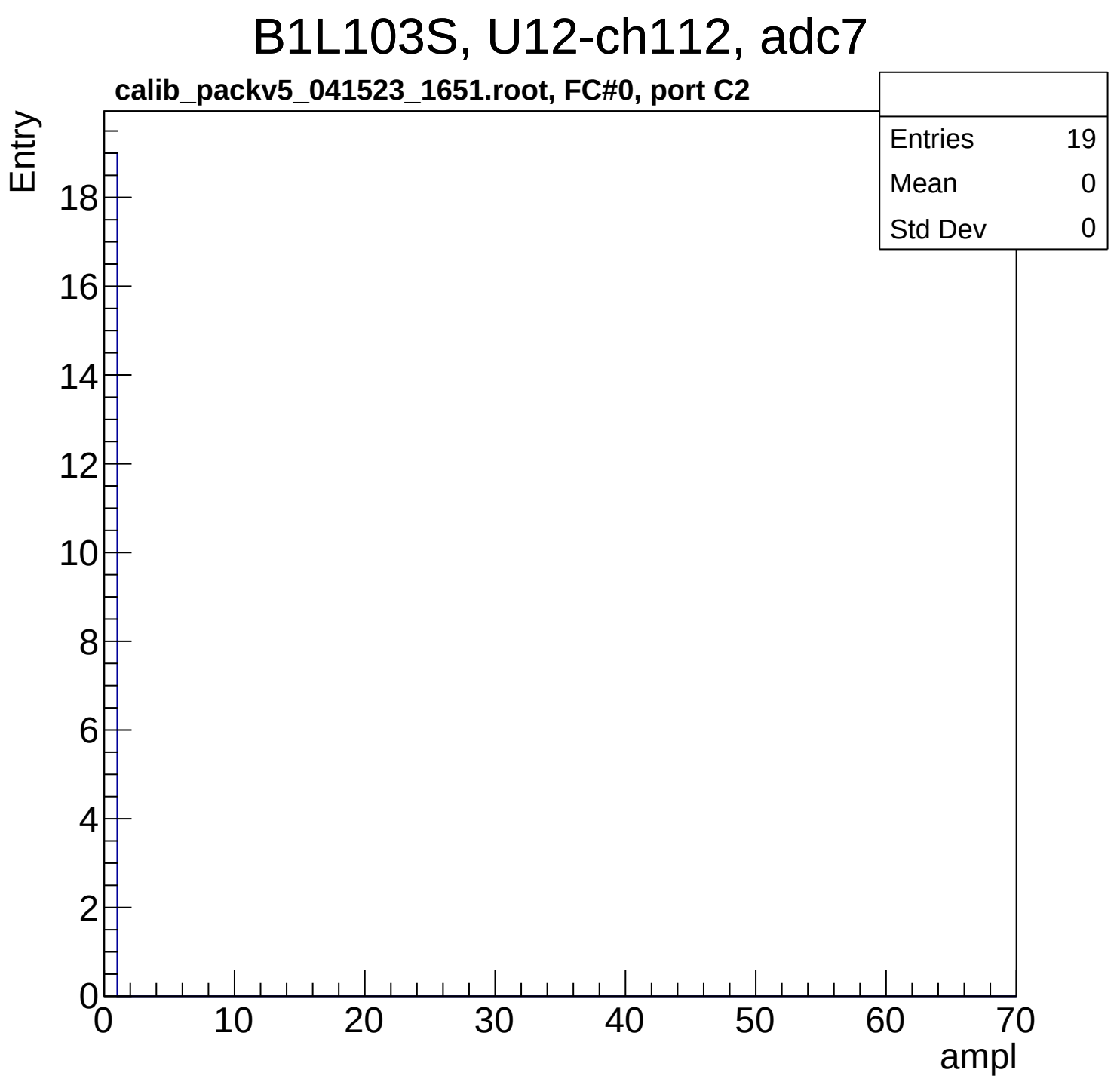
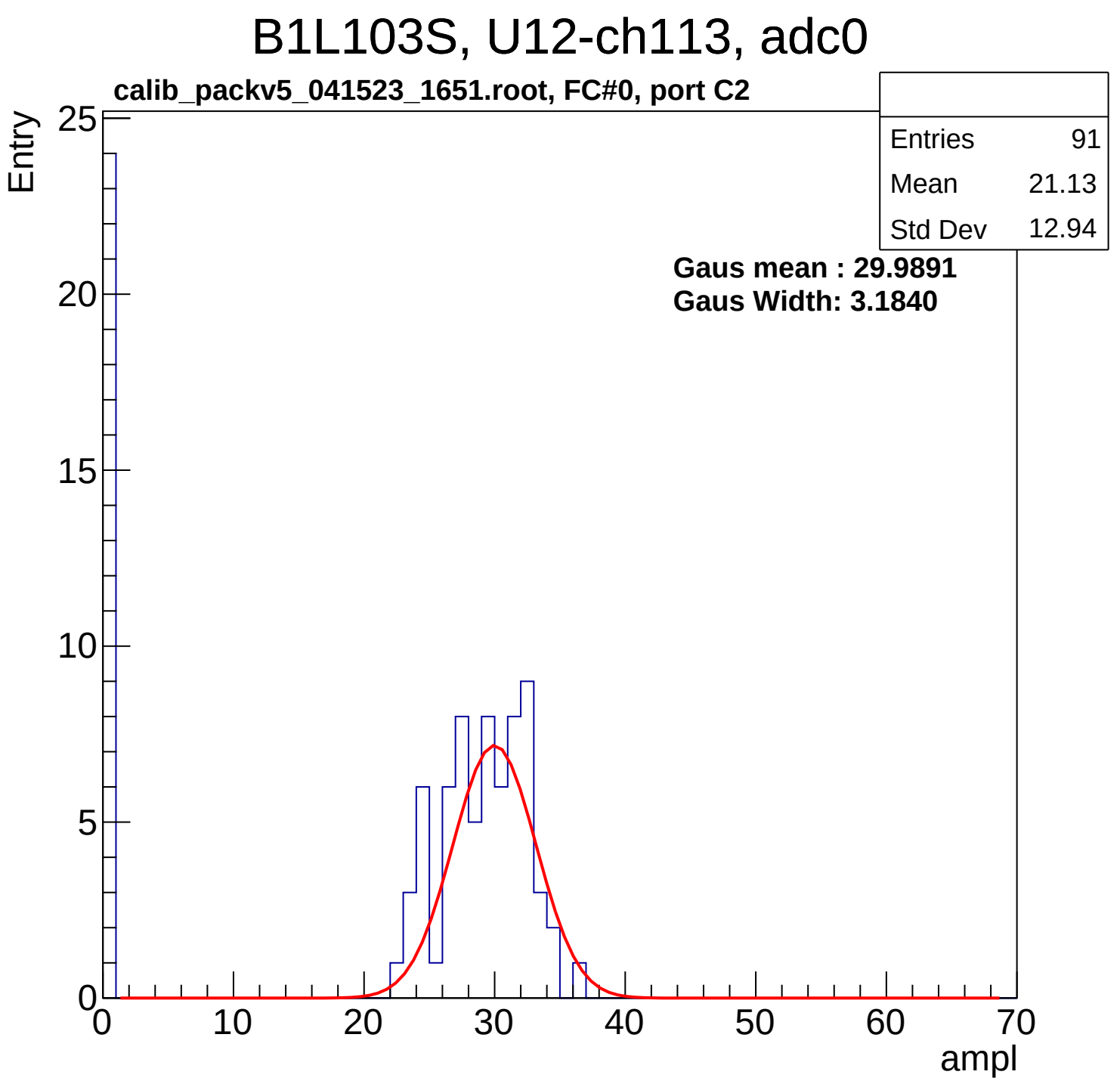
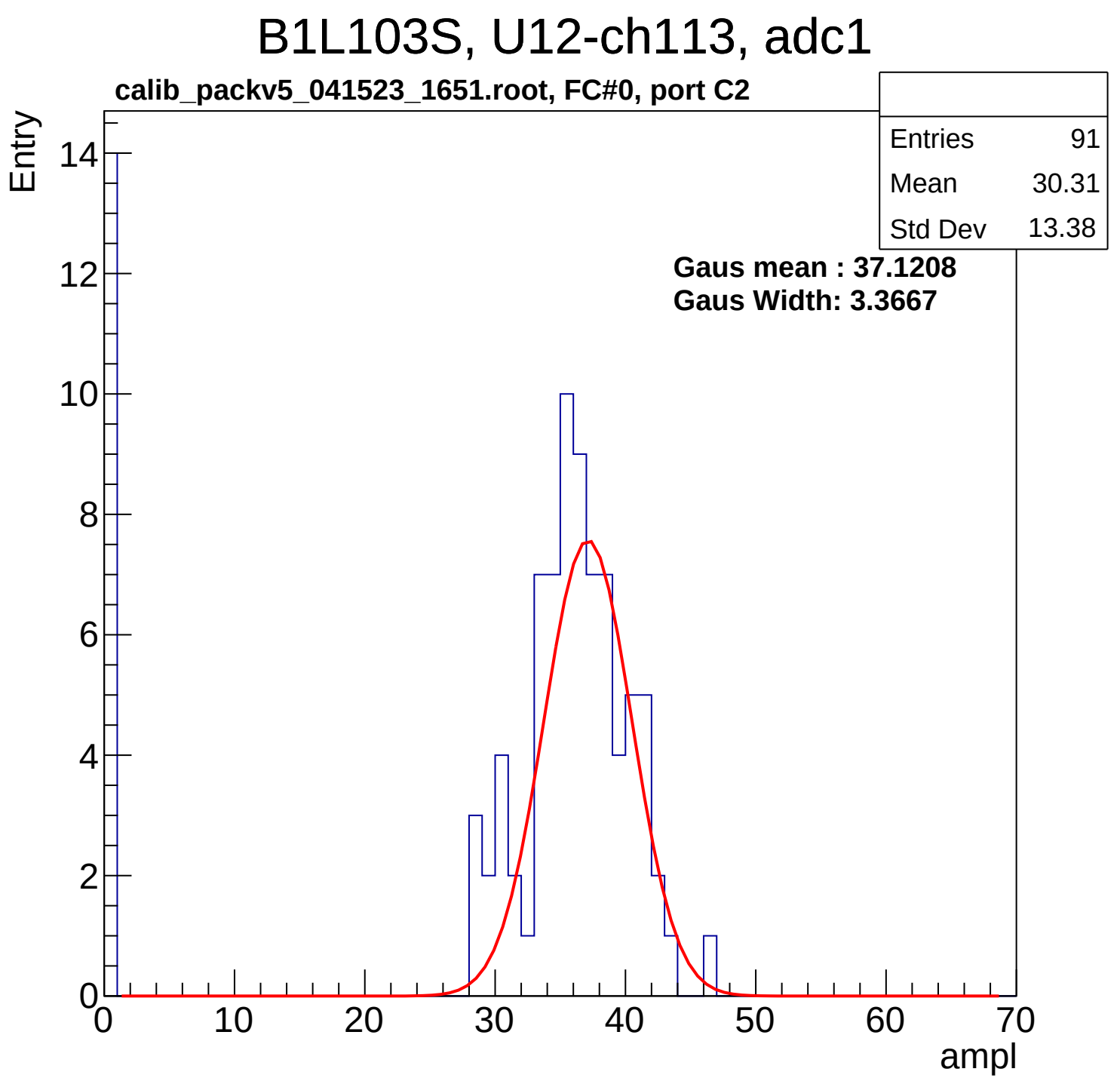

B1L103S, U12-ch112, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch113, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 21.13
Std Dev 12.94
Gaus mean : 29.9891
Gaus Width: 3.1840
Entry
ampl
0
5
10
15
20
25
0
10
20
30
40
50
60
70


B1L103S, U12-ch113, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 91
Mean 30.31
Std Dev 13.38
Gaus mean : 37.1208
Gaus Width: 3.3667
Entry
ampl
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2
4
6
8
10
12
14
0
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40
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60
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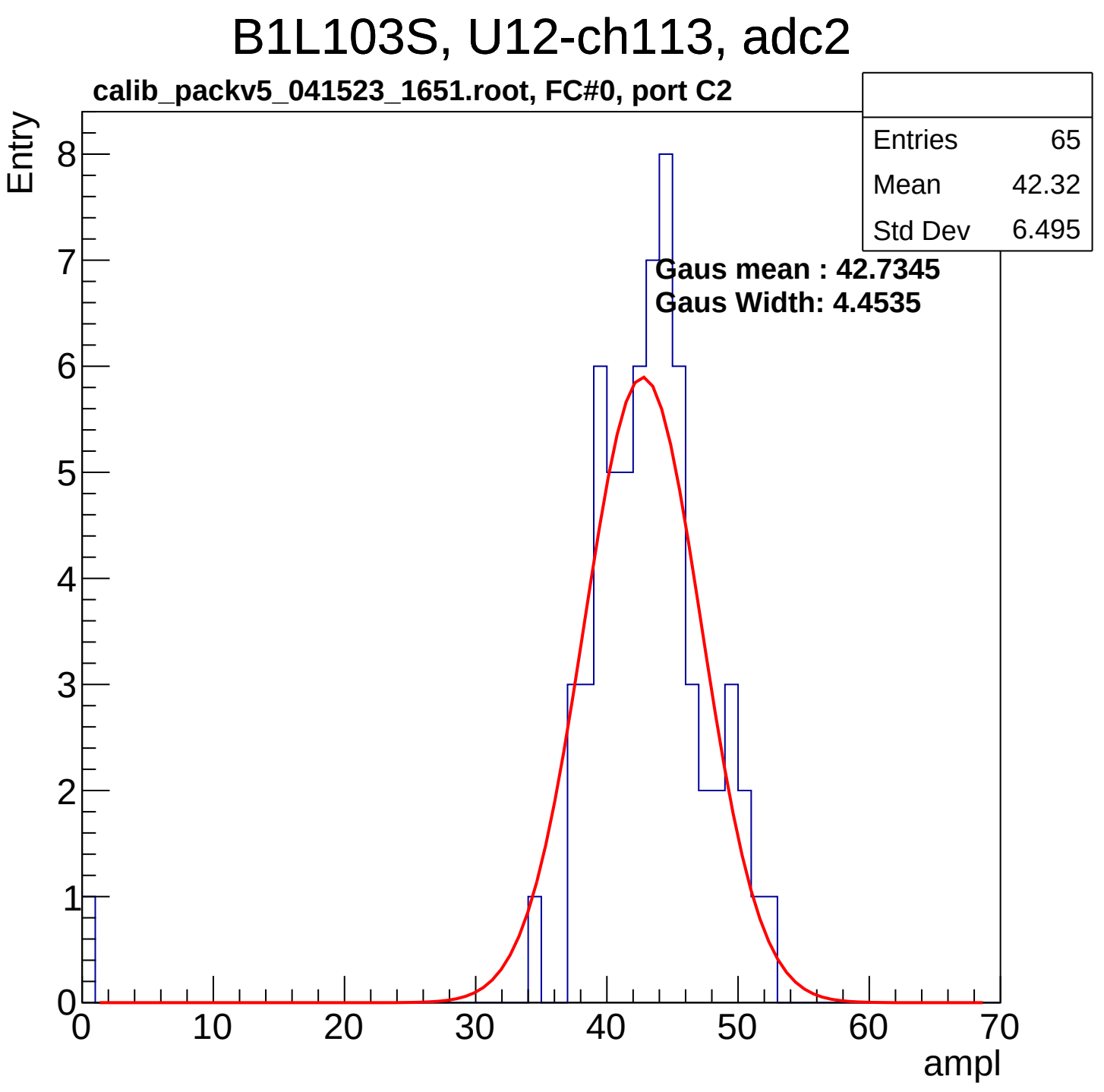
B1L103S, U12-ch113, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 42.32
Std Dev 6.495
Gaus mean : 42.7345
Gaus Width: 4.4535
Entry
ampl
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2
3
4
5
6
7
8
0
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20
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40
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60
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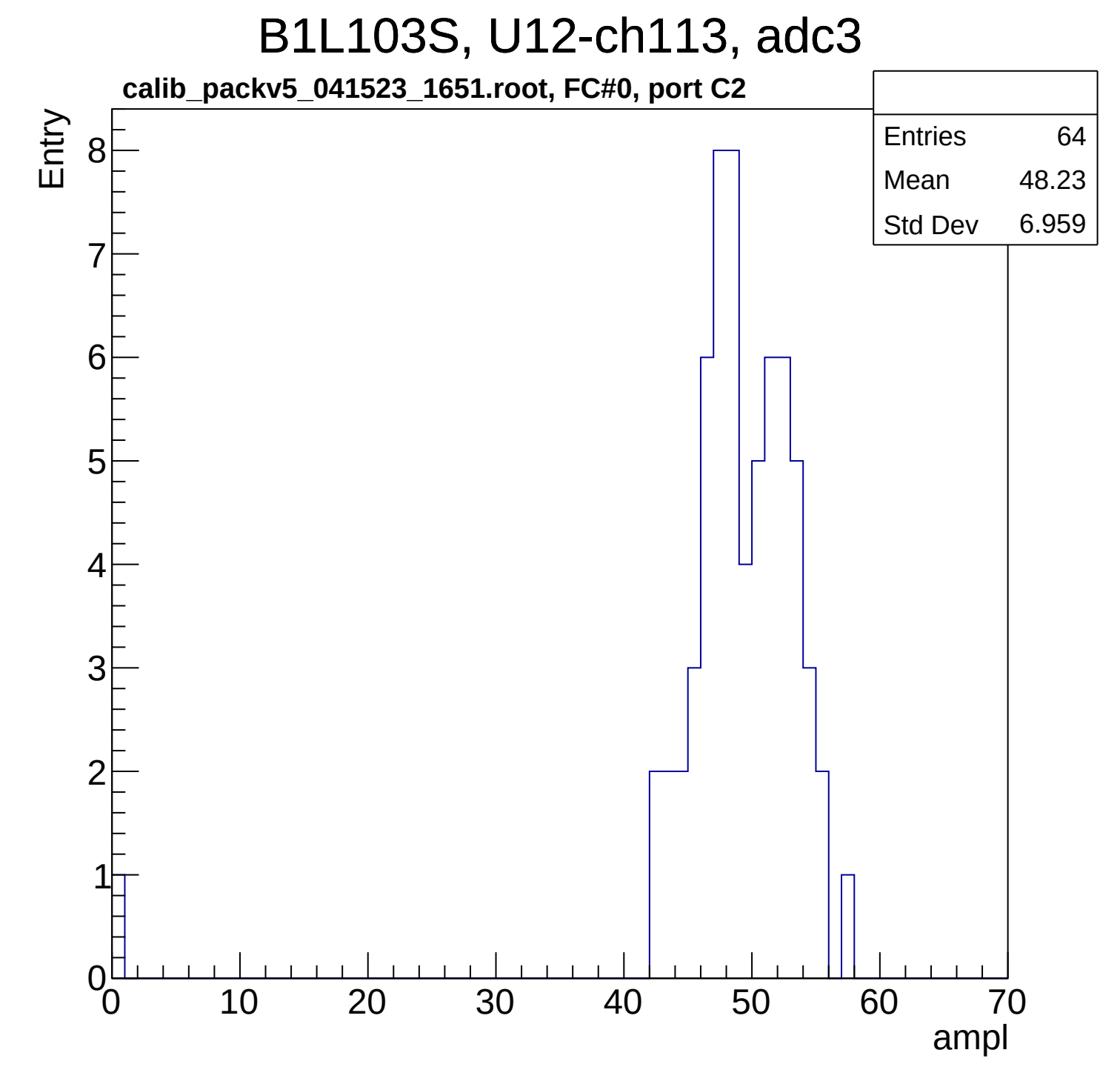
B1L103S, U12-ch113, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 48.23
Std Dev 6.959
Entry
ampl
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2
3
4
5
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7
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0
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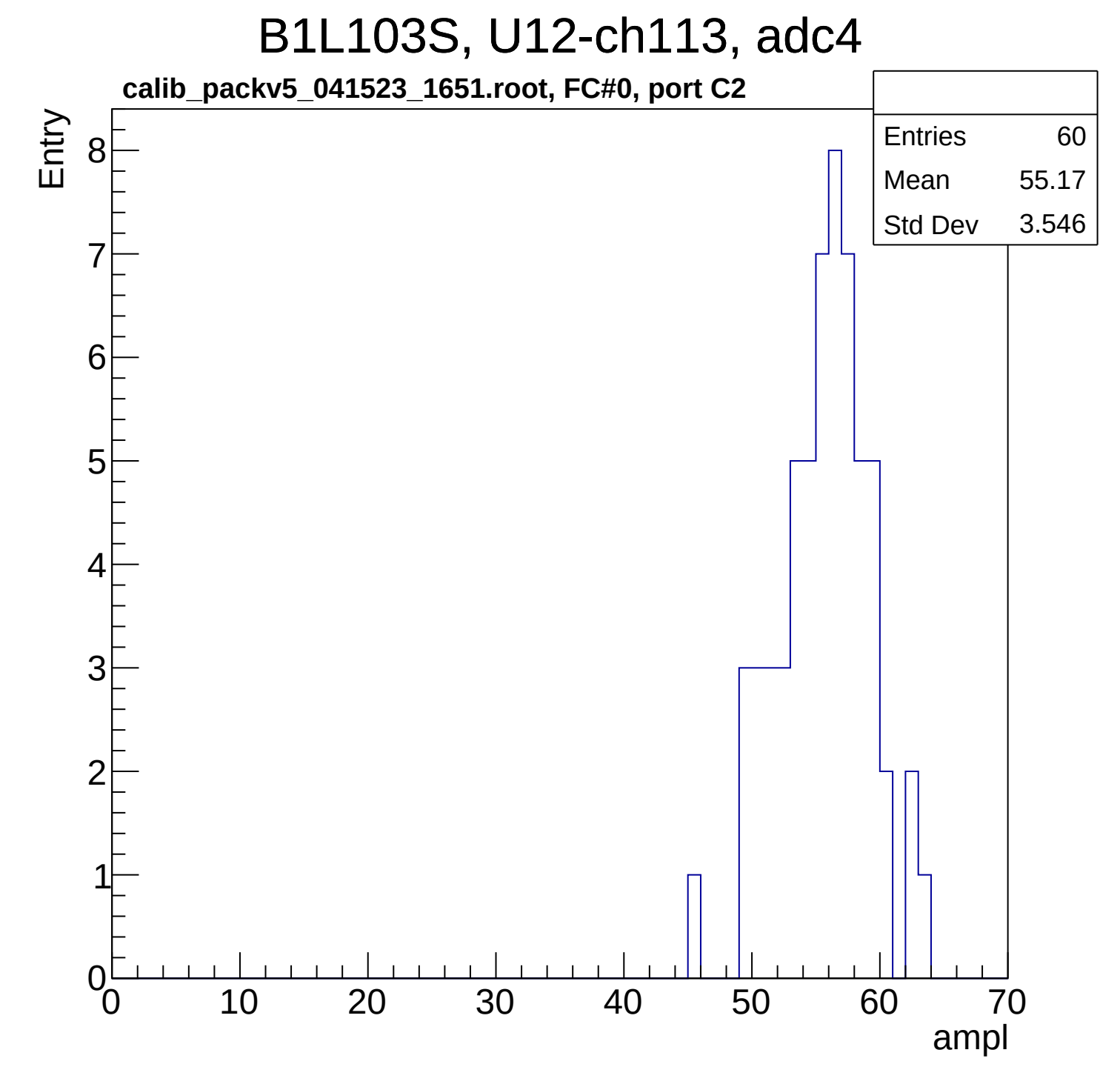
B1L103S, U12-ch113, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 55.17
Std Dev 3.546
Entry
ampl
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3
4
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0
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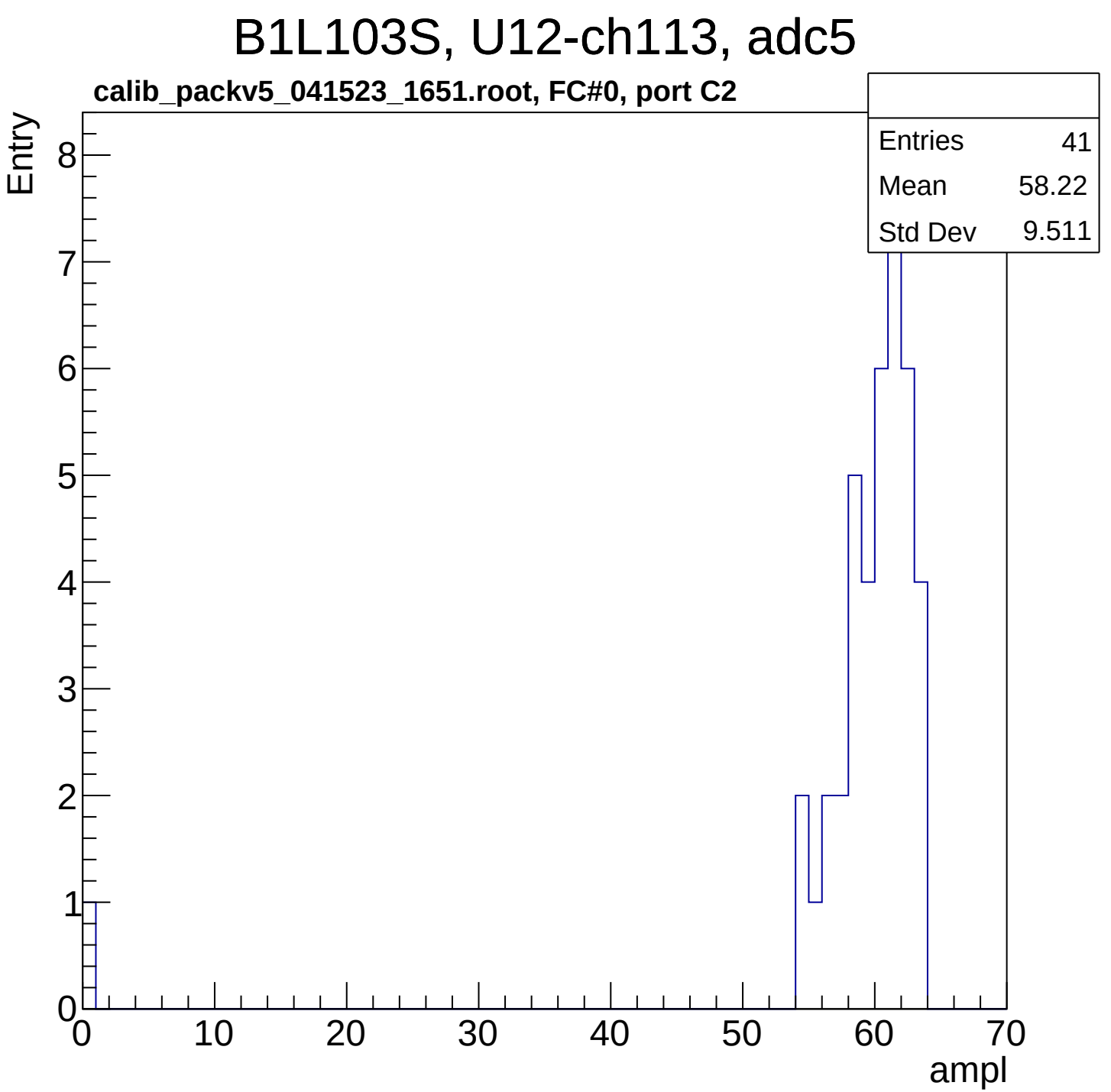
B1L103S, U12-ch113, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 58.22
Std Dev 9.511
Entry
ampl
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2
3
4
5
6
7
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0
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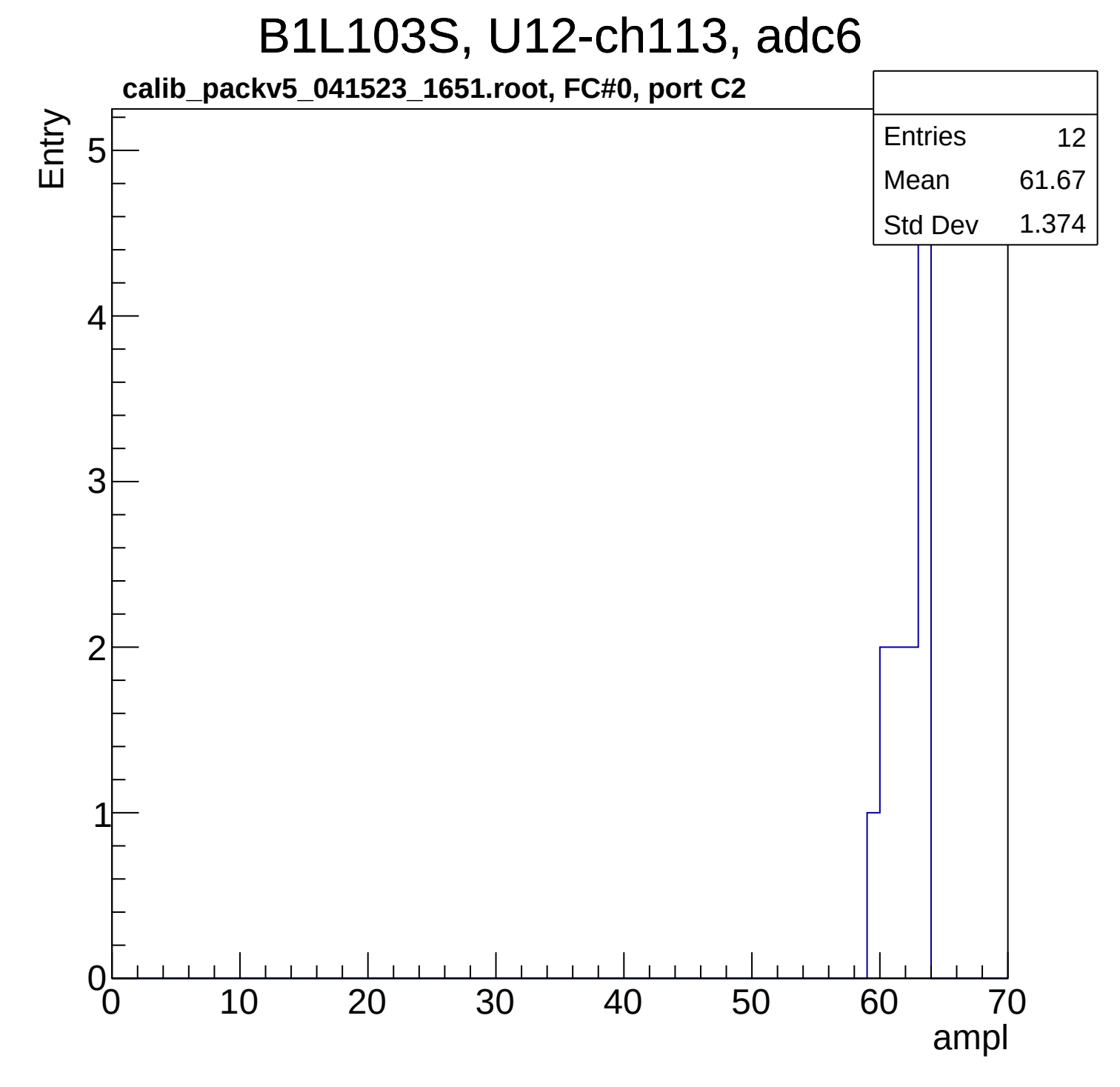
B1L103S, U12-ch113, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.67
Std Dev 1.374
Entry
ampl
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3
4
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0
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20
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40
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60
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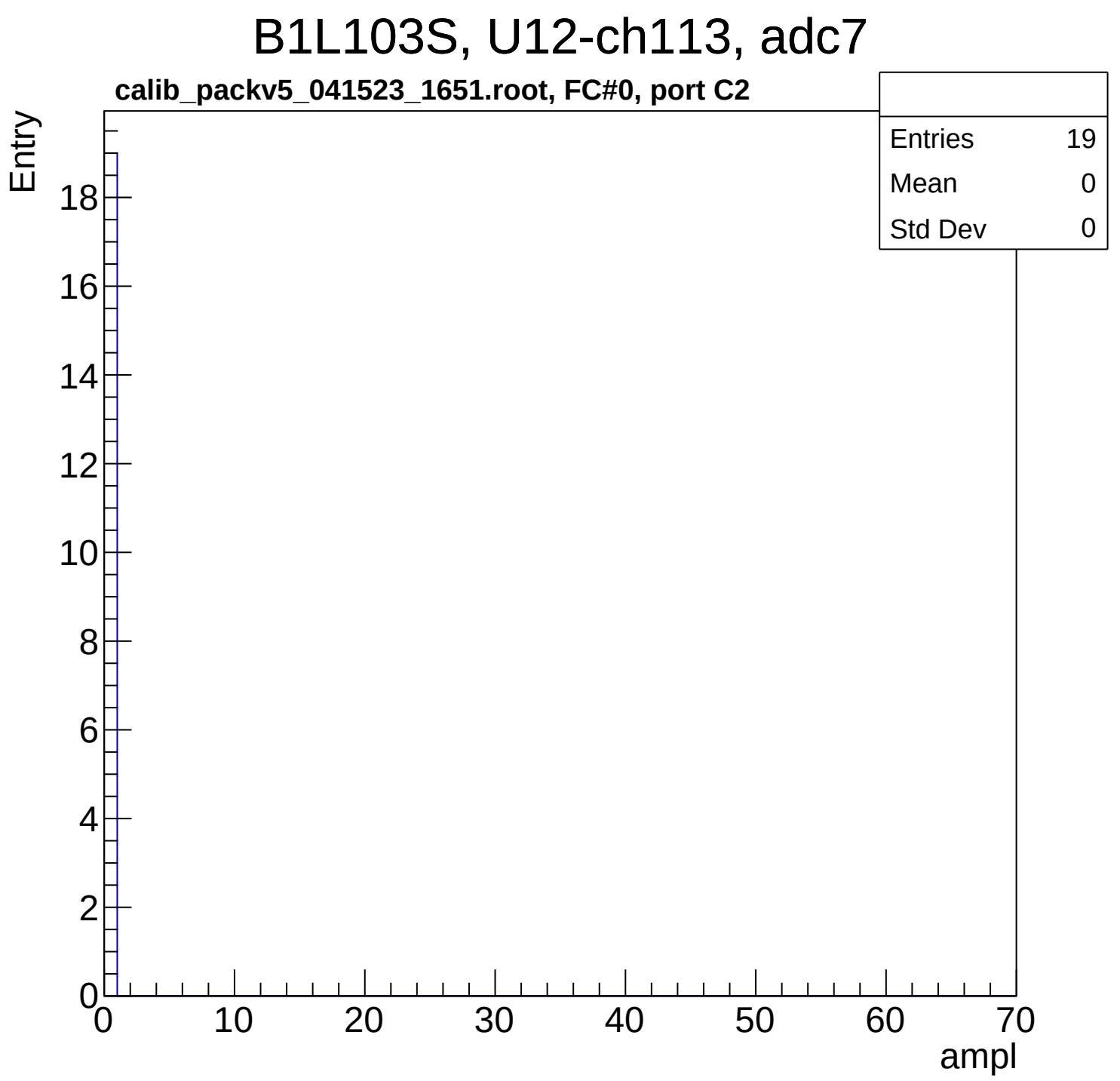
B1L103S, U12-ch113, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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2
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6
8
10
12
14
16
18
0
10
20
30
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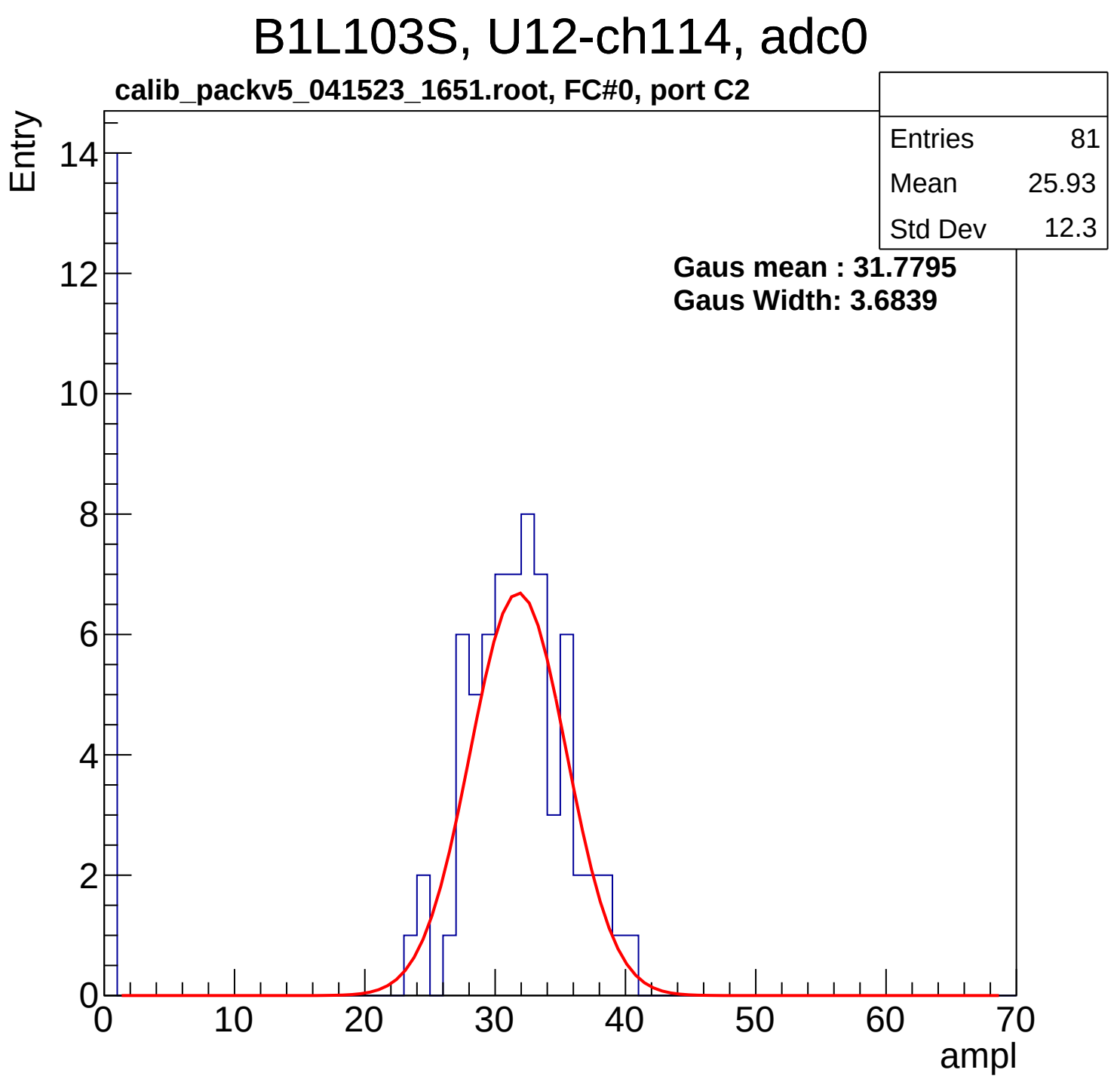
50
60
70
ampl


B1L103S, U12-ch114, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 25.93
Std Dev 12.3
Gaus mean : 31.7795
Gaus Width: 3.6839
Entry
ampl
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4
6
8
10
12
14
0
10
20
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40
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60
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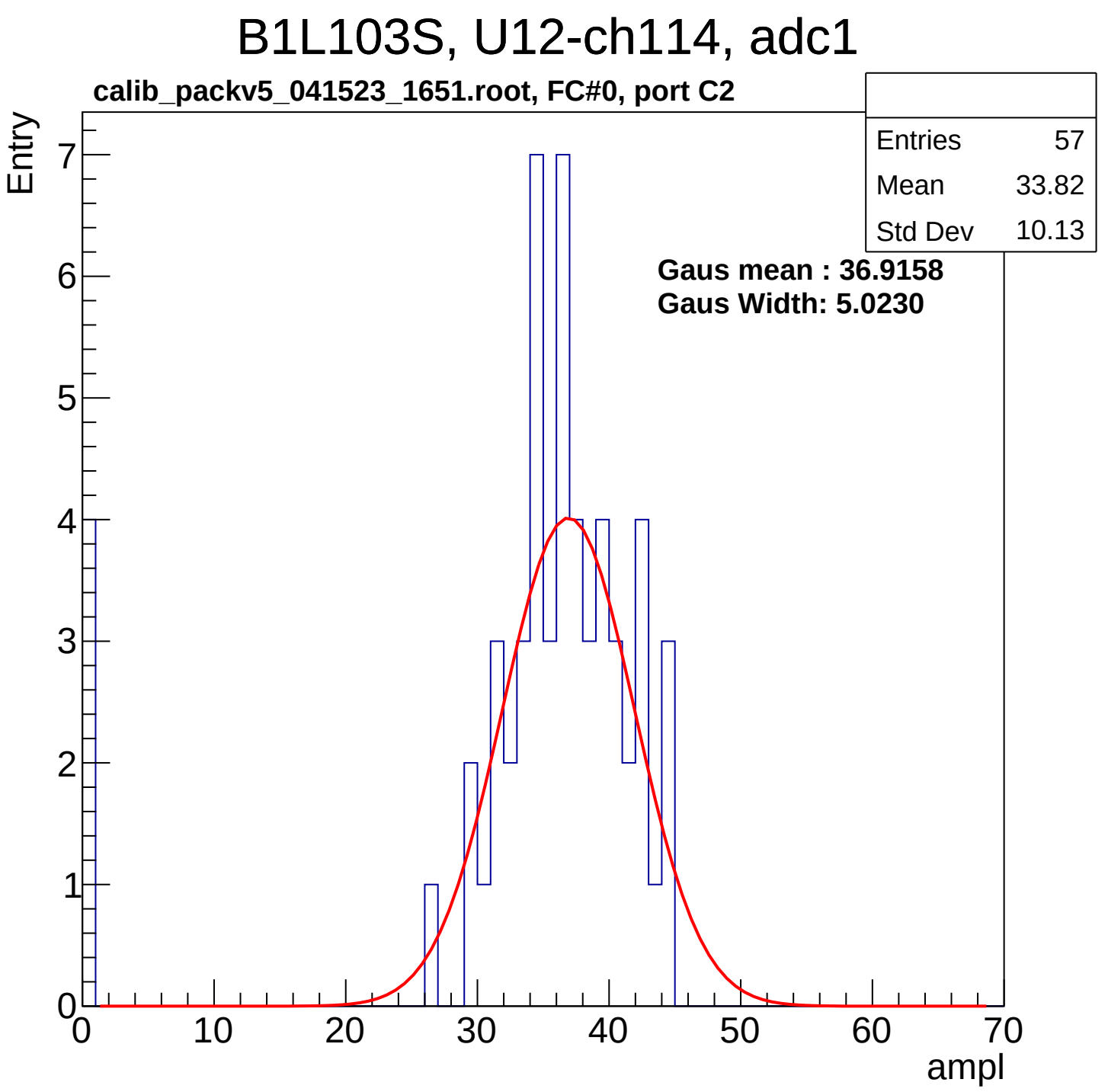
B1L103S, U12-ch114, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 57
Mean 33.82
Std Dev 10.13
Gaus mean : 36.9158
Gaus Width: 5.0230
Entry
ampl
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1
2
3
4
5
6
7
0
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20
30
40
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60
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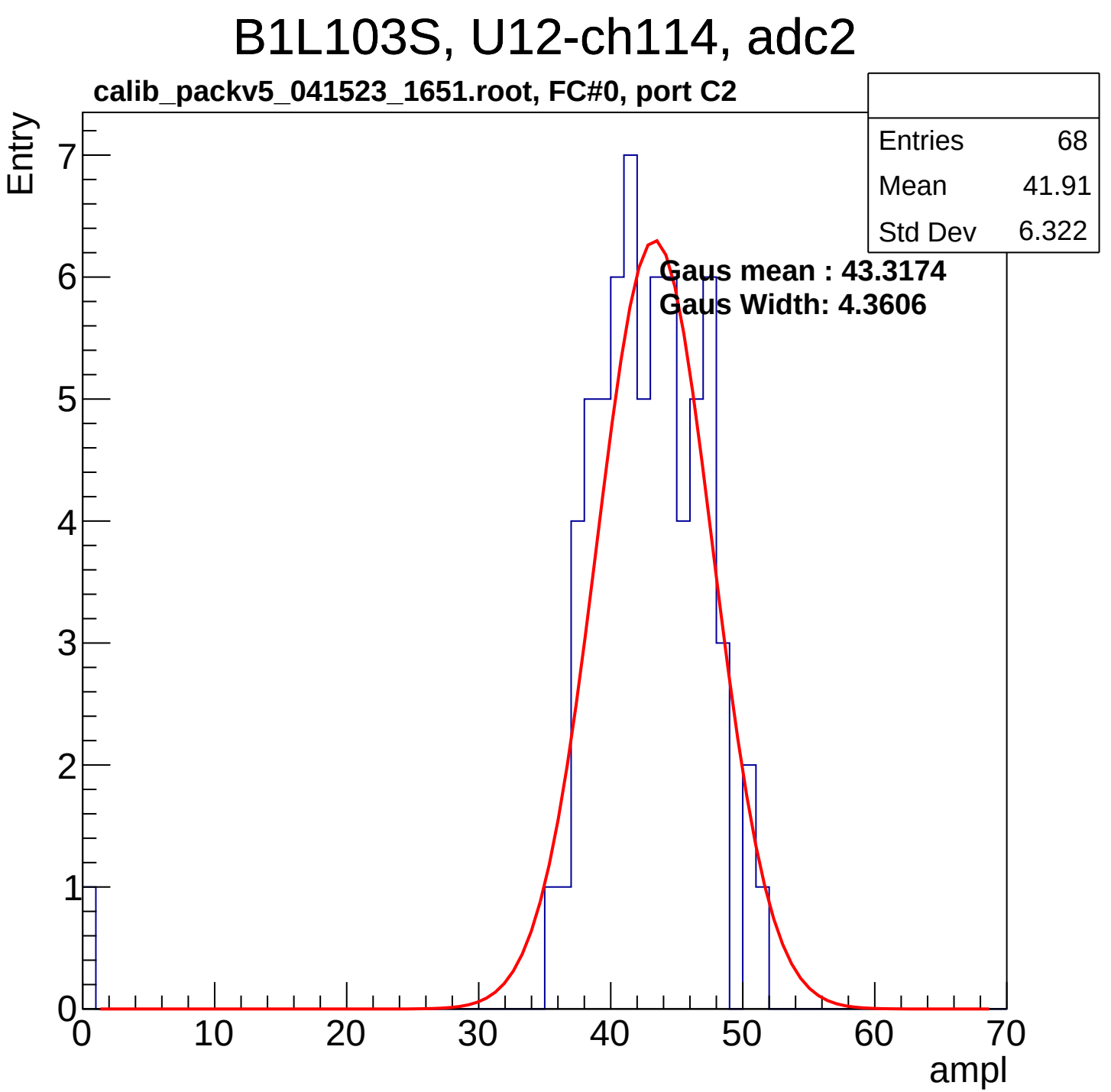
B1L103S, U12-ch114, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 41.91
Std Dev 6.322
Gaus mean : 43.3174
Gaus Width: 4.3606
Entry
ampl
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1
2
3
4
5
6
7
0
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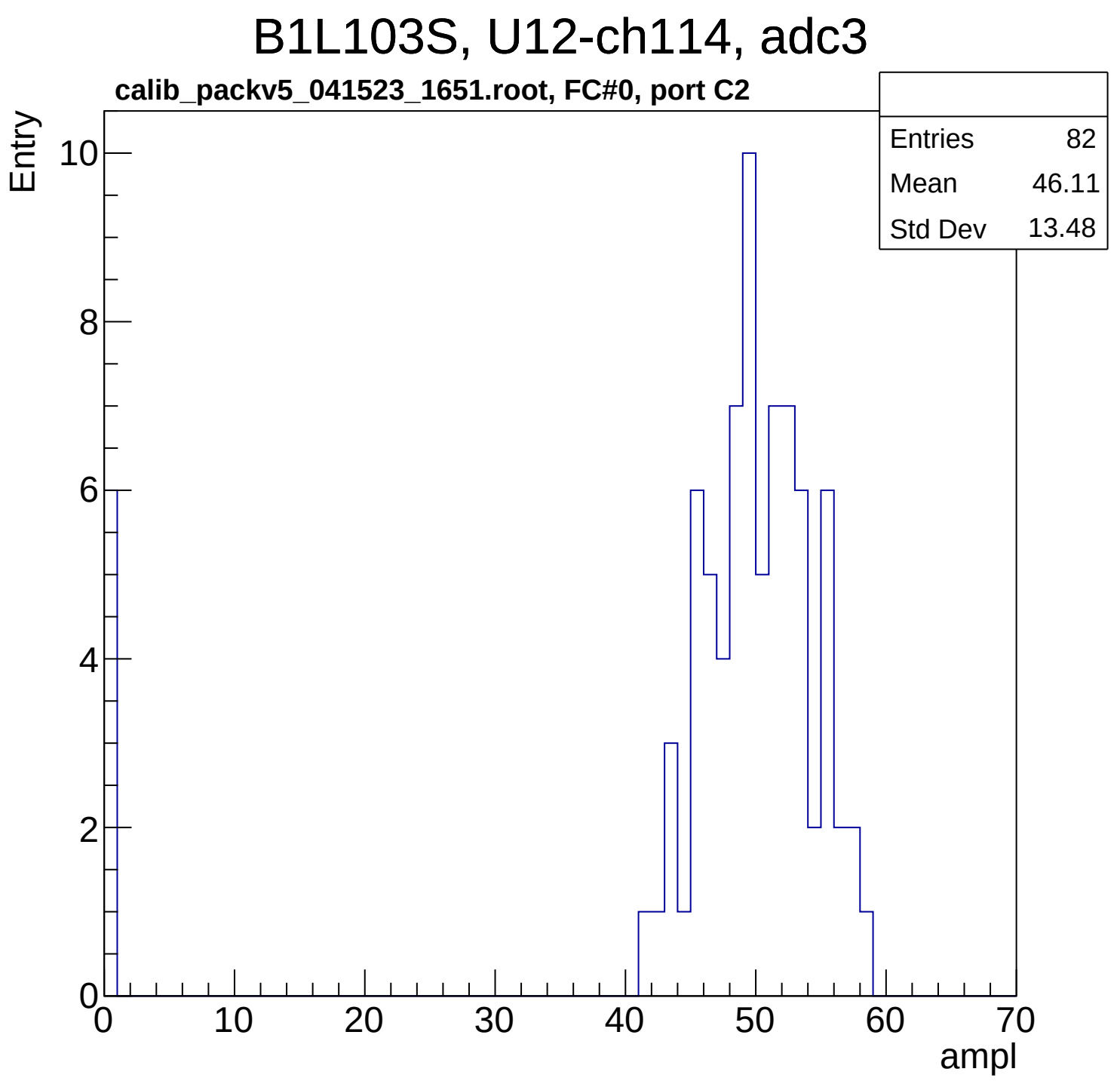
B1L103S, U12-ch114, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 82
Mean 46.11
Std Dev 13.48
Entry
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6
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10
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50
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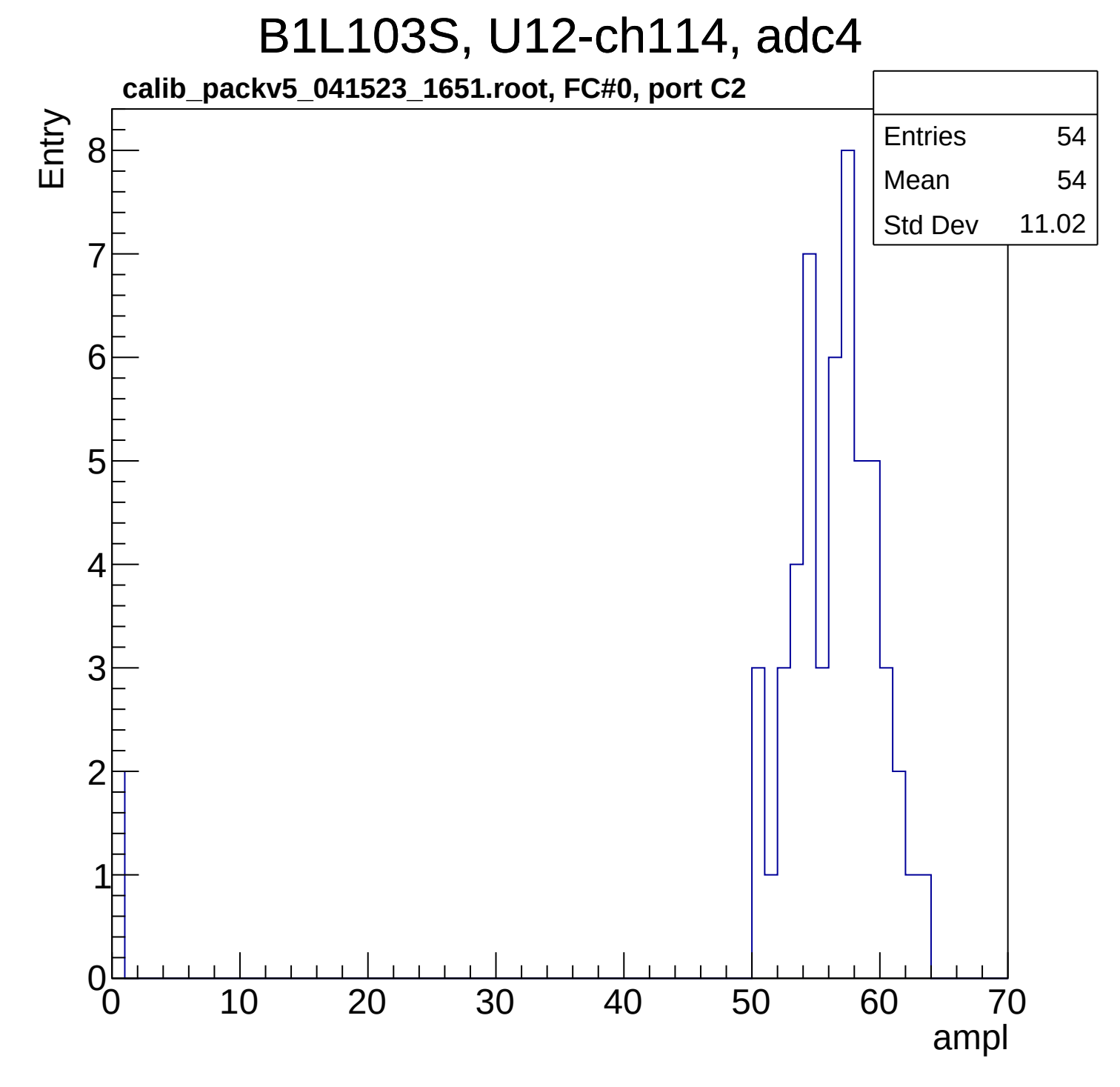
70
ampl


B1L103S, U12-ch114, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 54
Std Dev 11.02
Entry
ampl
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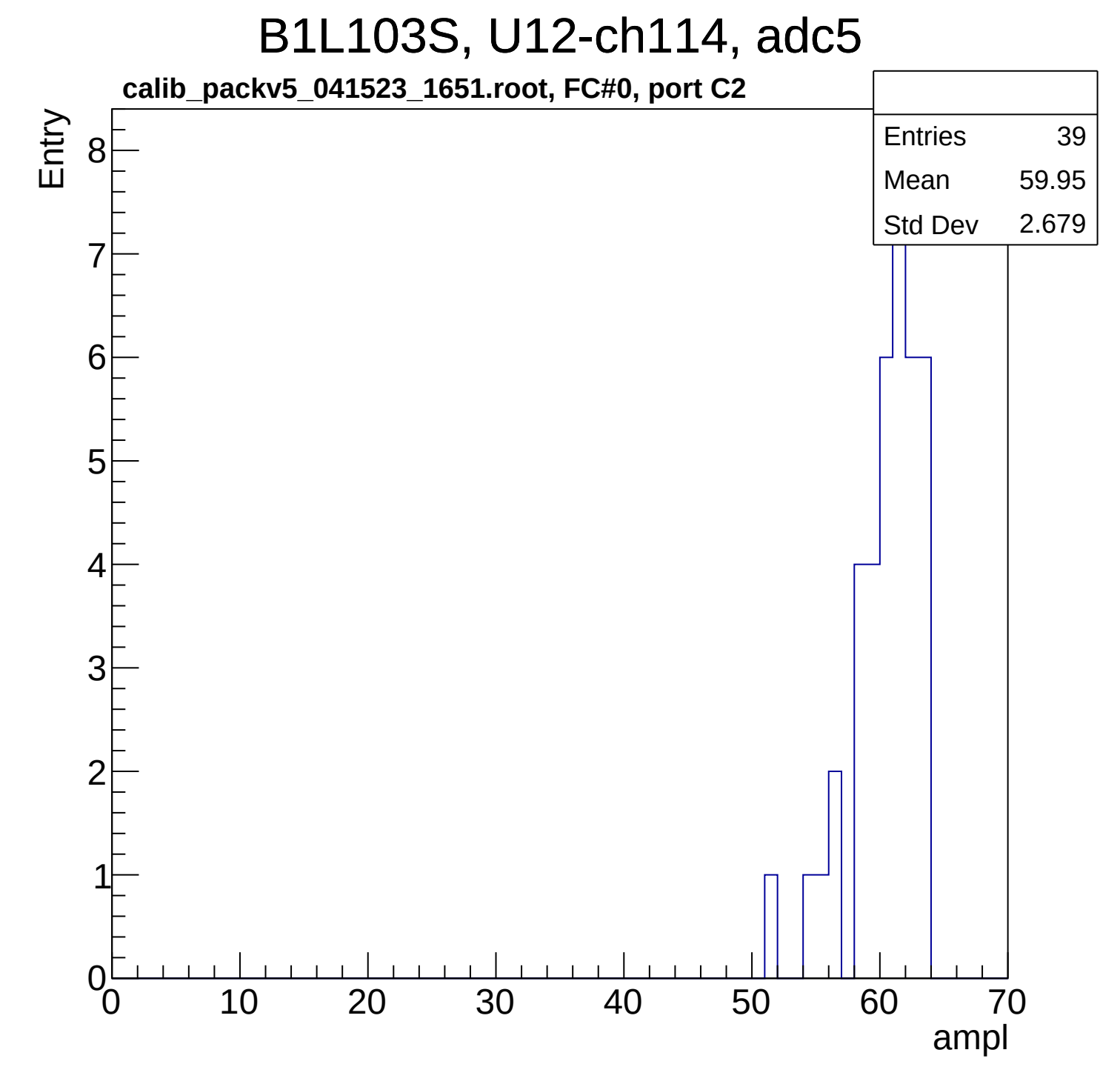
B1L103S, U12-ch114, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 59.95
Std Dev 2.679
Entry
ampl
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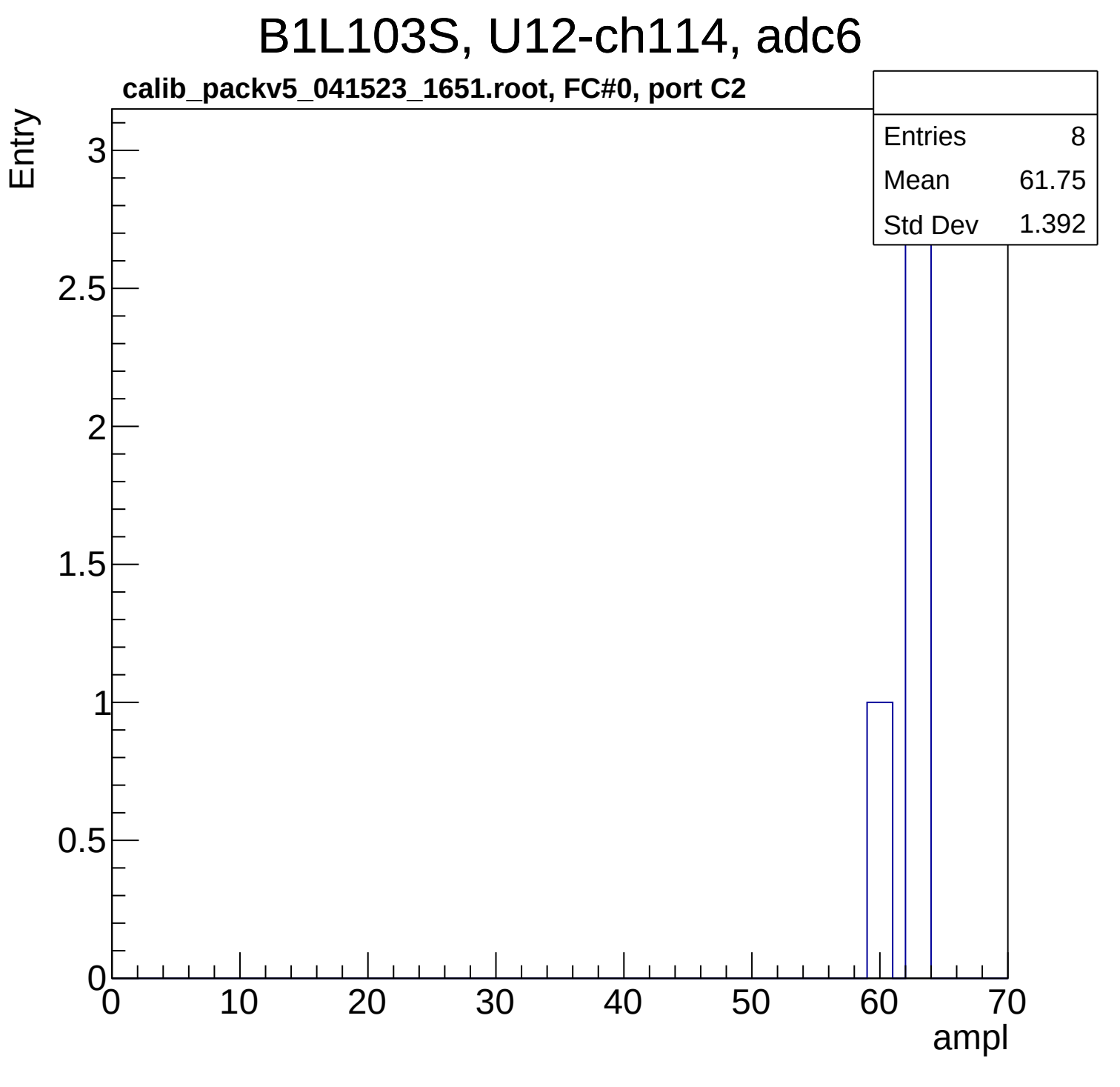
B1L103S, U12-ch114, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 8
Mean 61.75
Std Dev 1.392
Entry
ampl
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1.5
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2.5
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0
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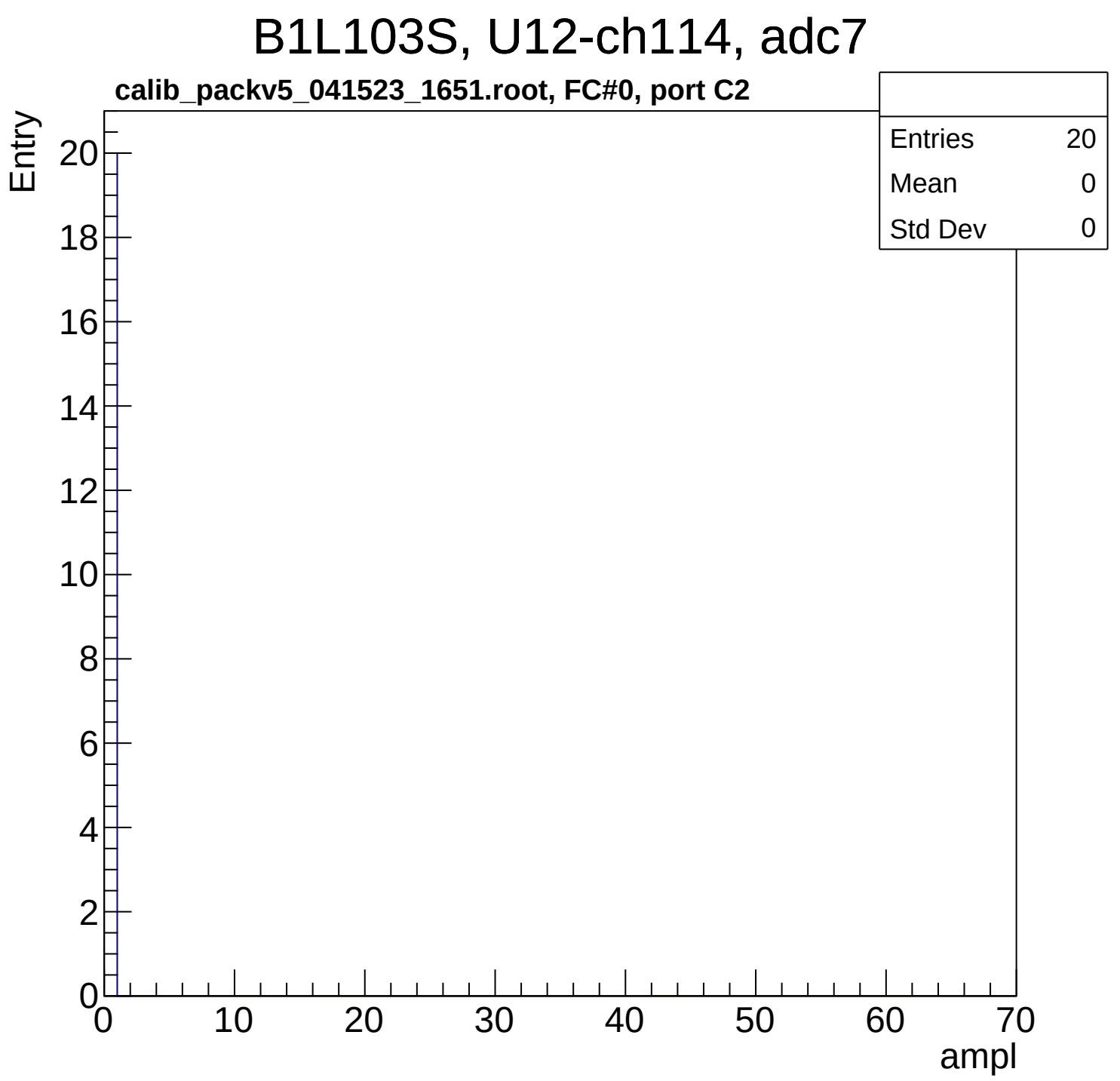
B1L103S, U12-ch114, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 0
Std Dev 0
Entry
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12
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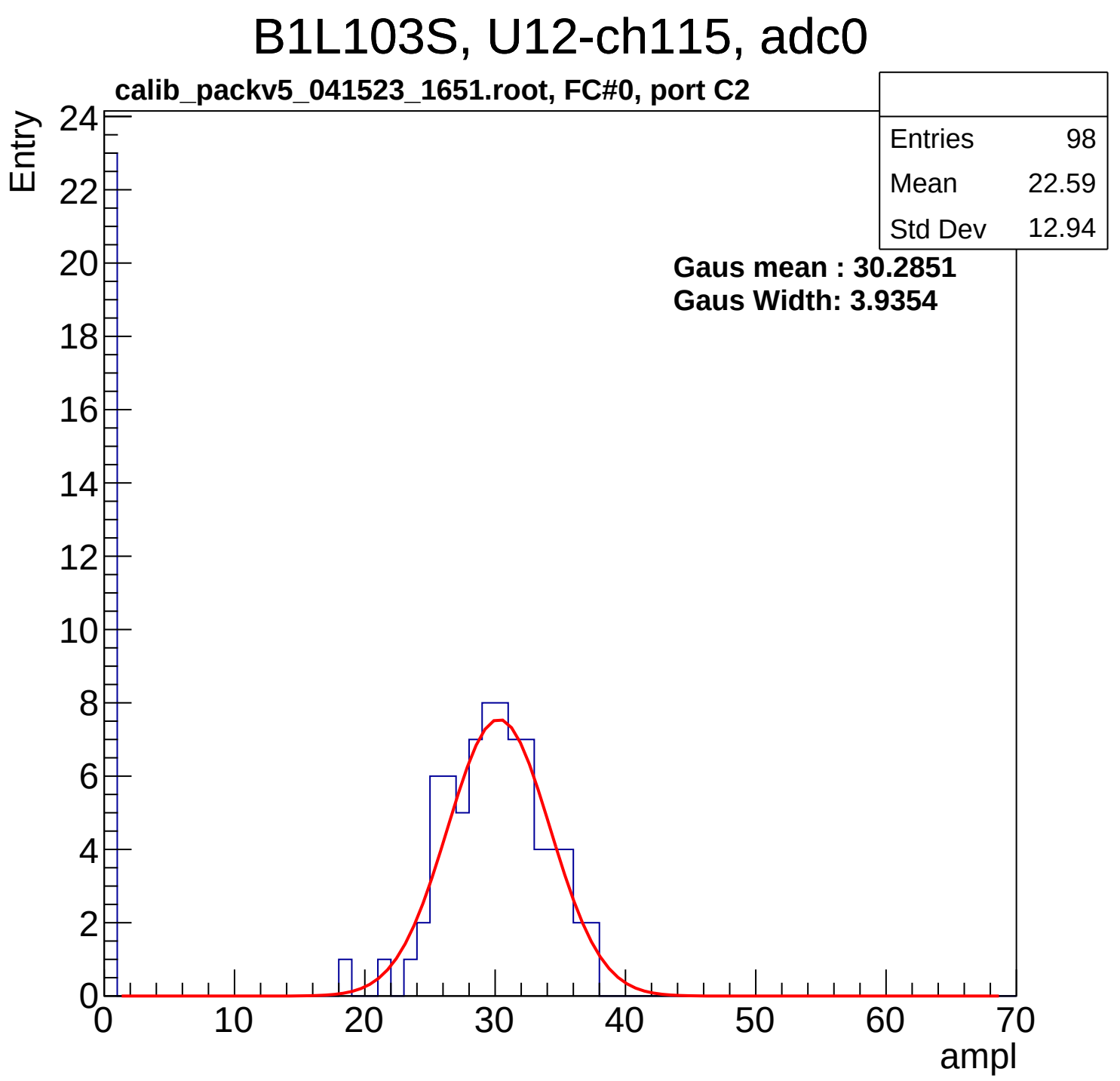
50
60
70
ampl


B1L103S, U12-ch115, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 22.59
Std Dev 12.94
Gaus mean : 30.2851
Gaus Width: 3.9354
Entry
ampl
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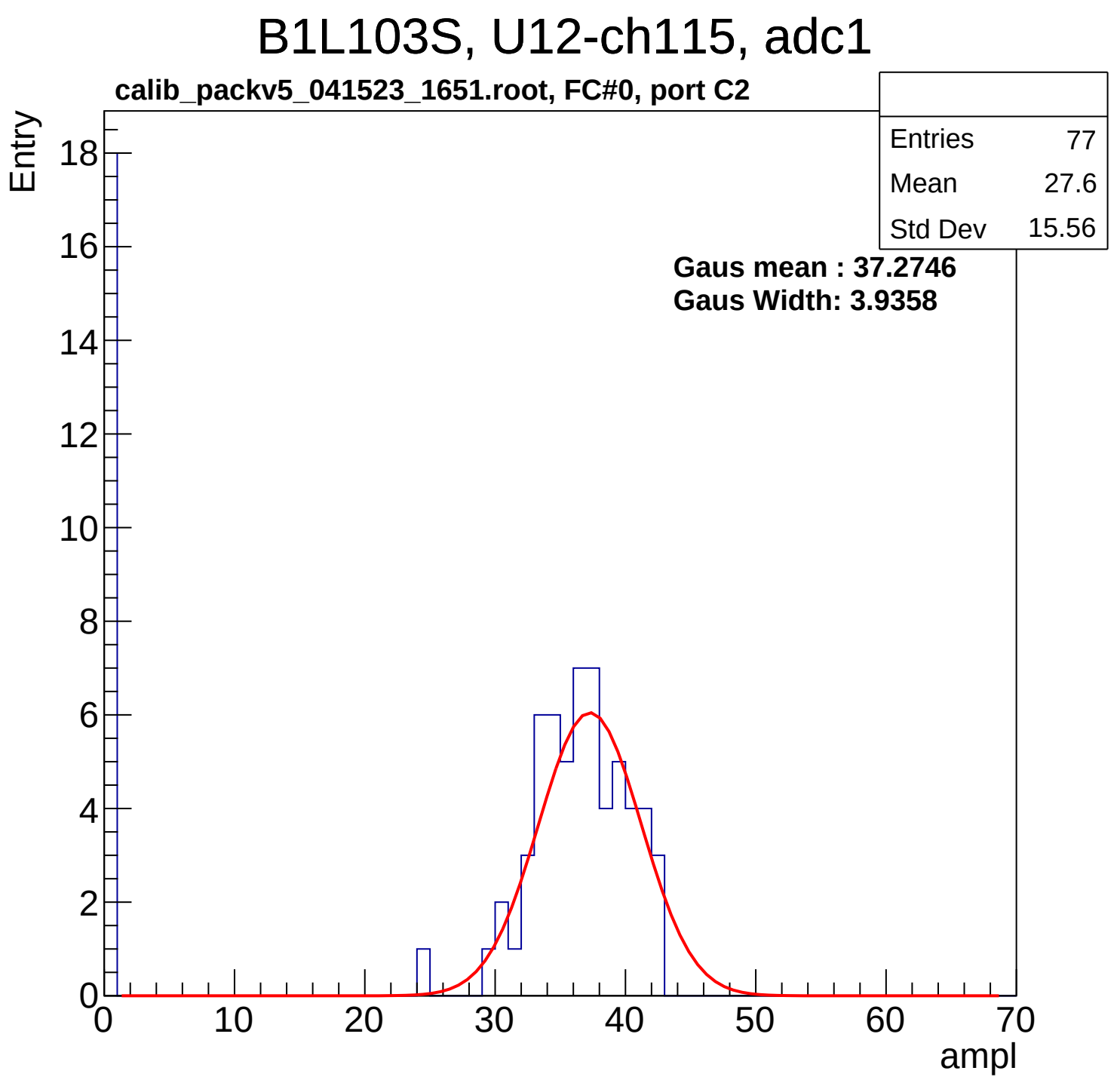
B1L103S, U12-ch115, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 77
Mean 27.6
Std Dev 15.56
Gaus mean : 37.2746
Gaus Width: 3.9358
Entry
ampl
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4
6
8
10
12
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0
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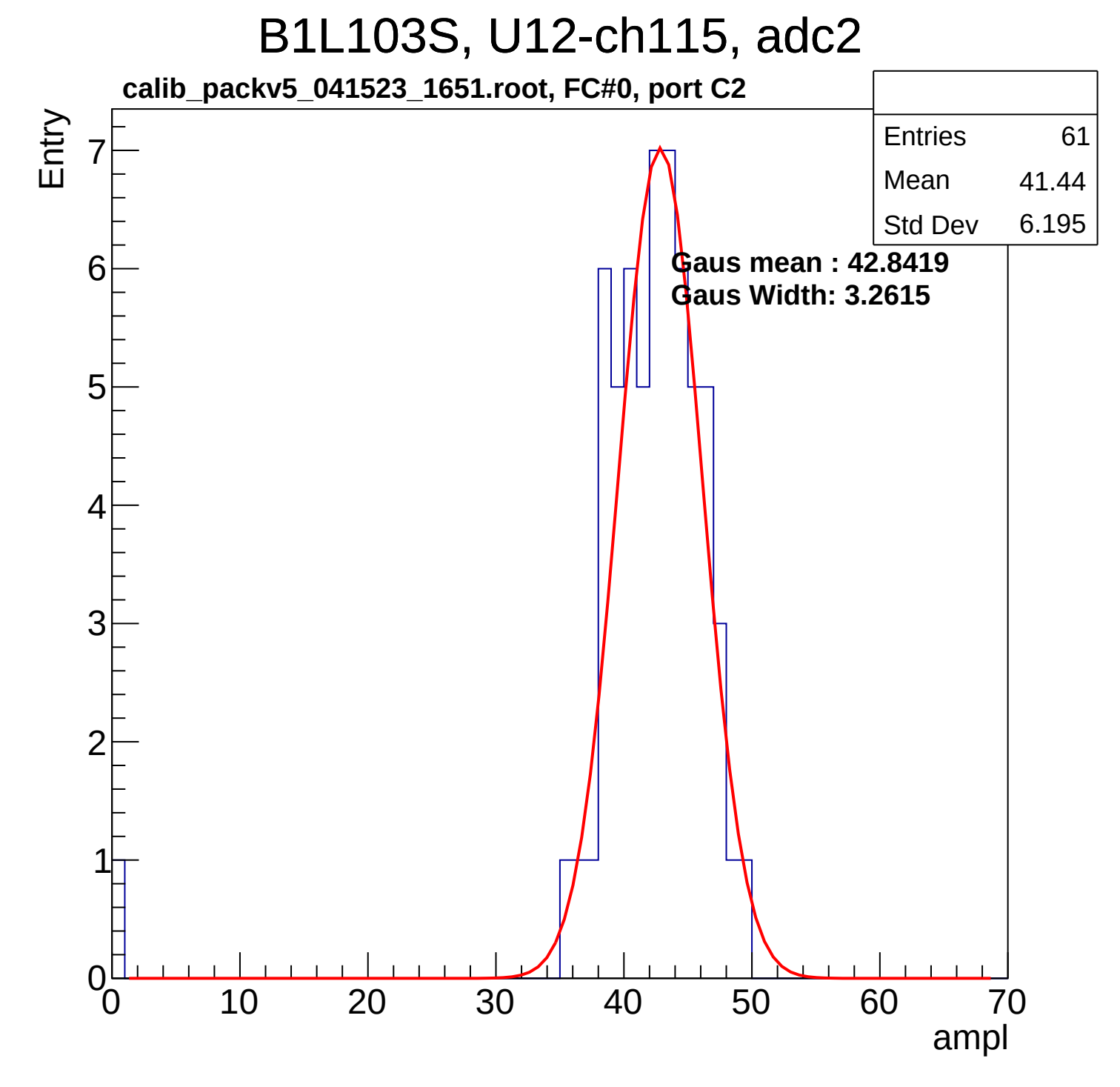
B1L103S, U12-ch115, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 41.44
Std Dev 6.195
Gaus mean : 42.8419
Gaus Width: 3.2615
Entry
ampl
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0
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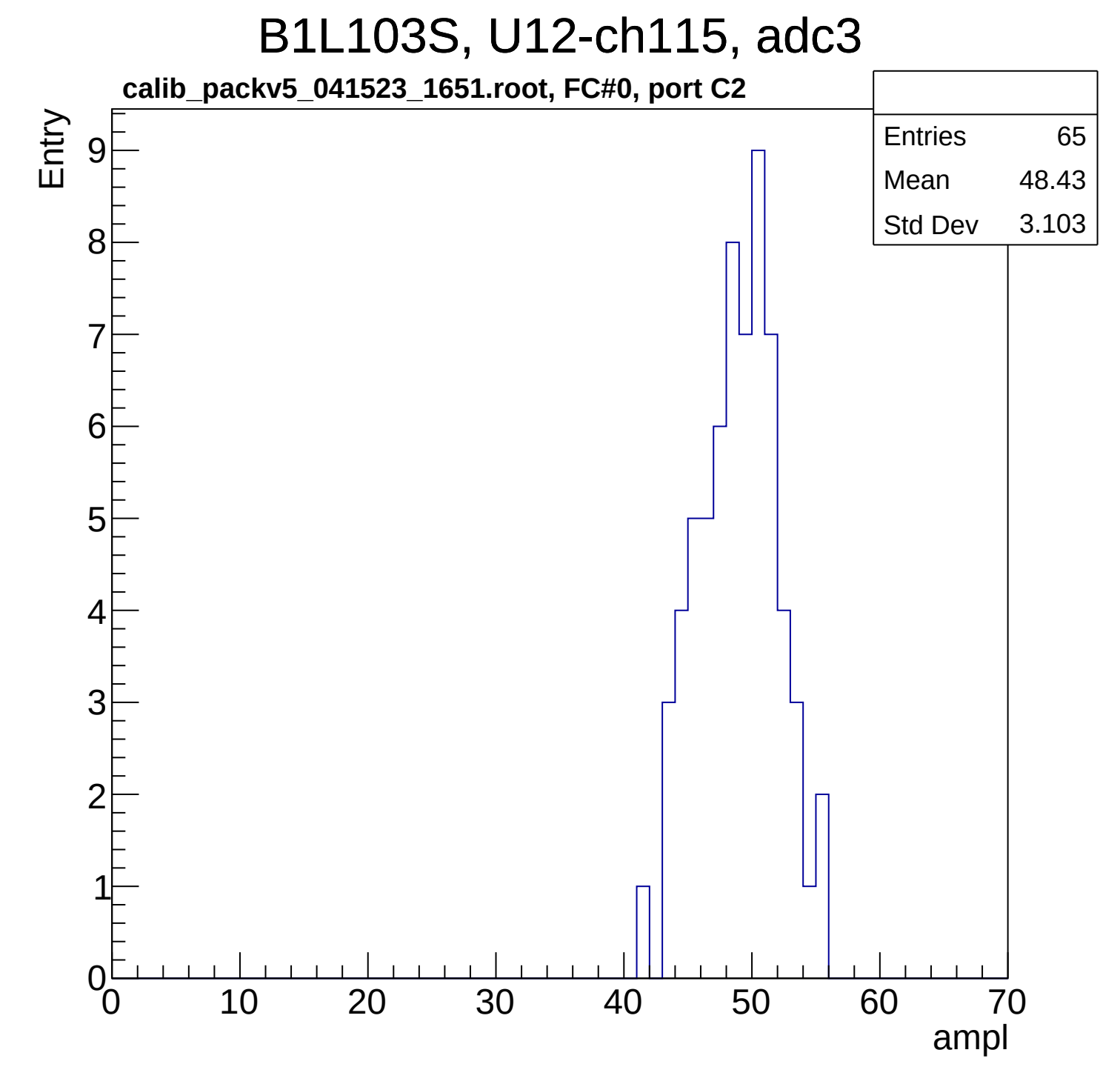
B1L103S, U12-ch115, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 48.43
Std Dev 3.103
Entry
ampl
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3
4
5
6
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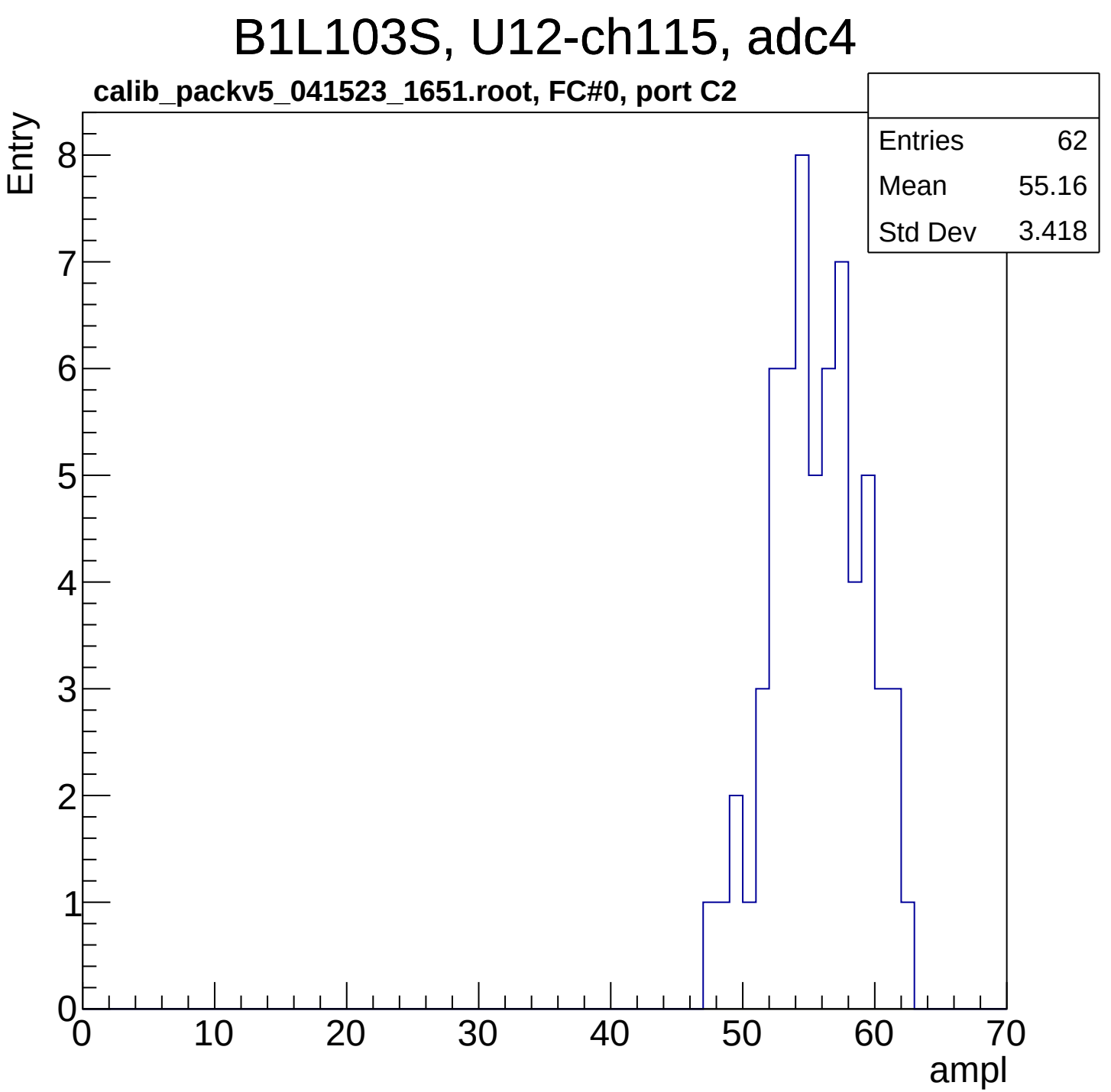
B1L103S, U12-ch115, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 55.16
Std Dev 3.418
Entry
ampl
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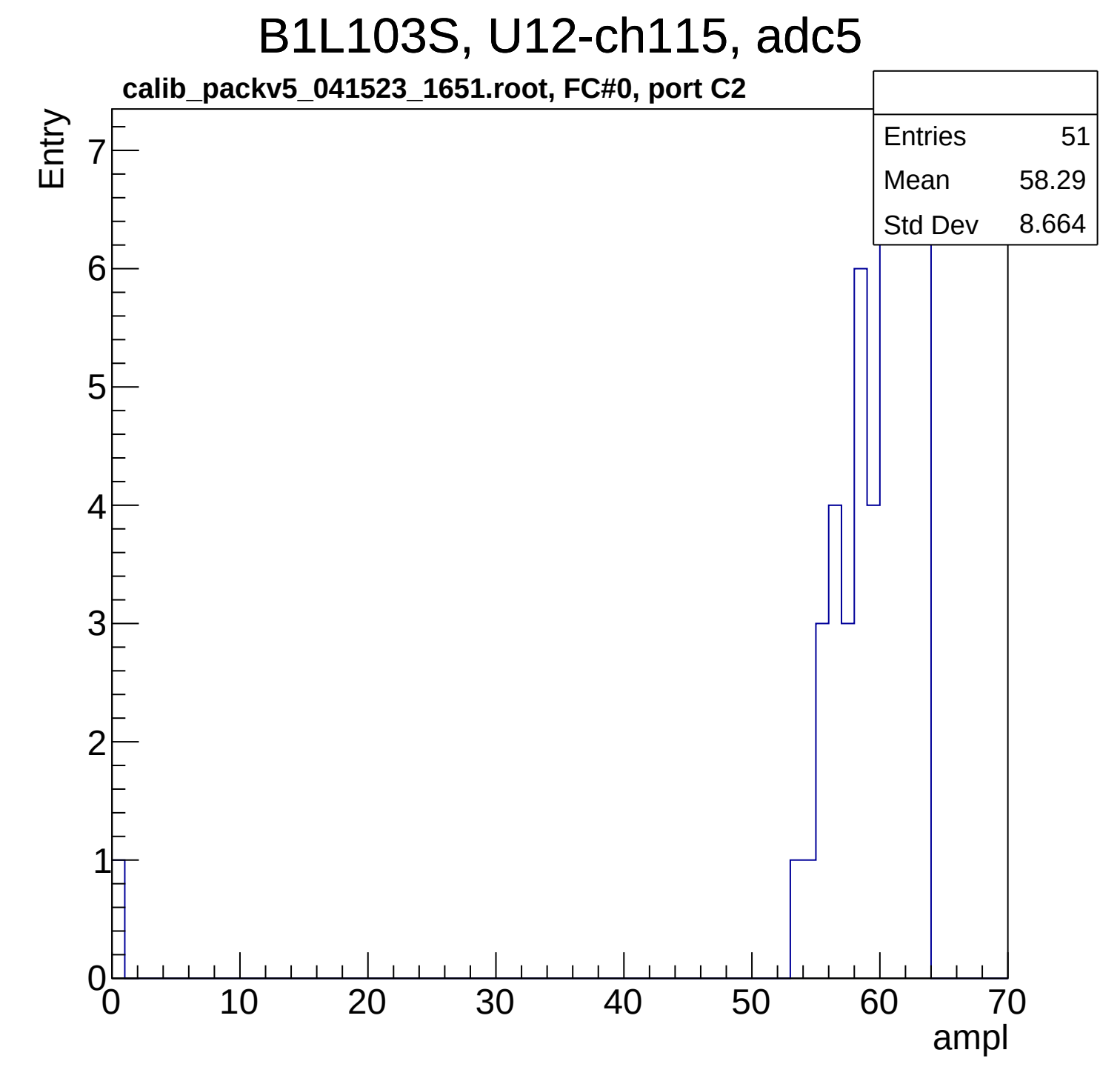
B1L103S, U12-ch115, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 58.29
Std Dev 8.664
Entry
ampl
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60
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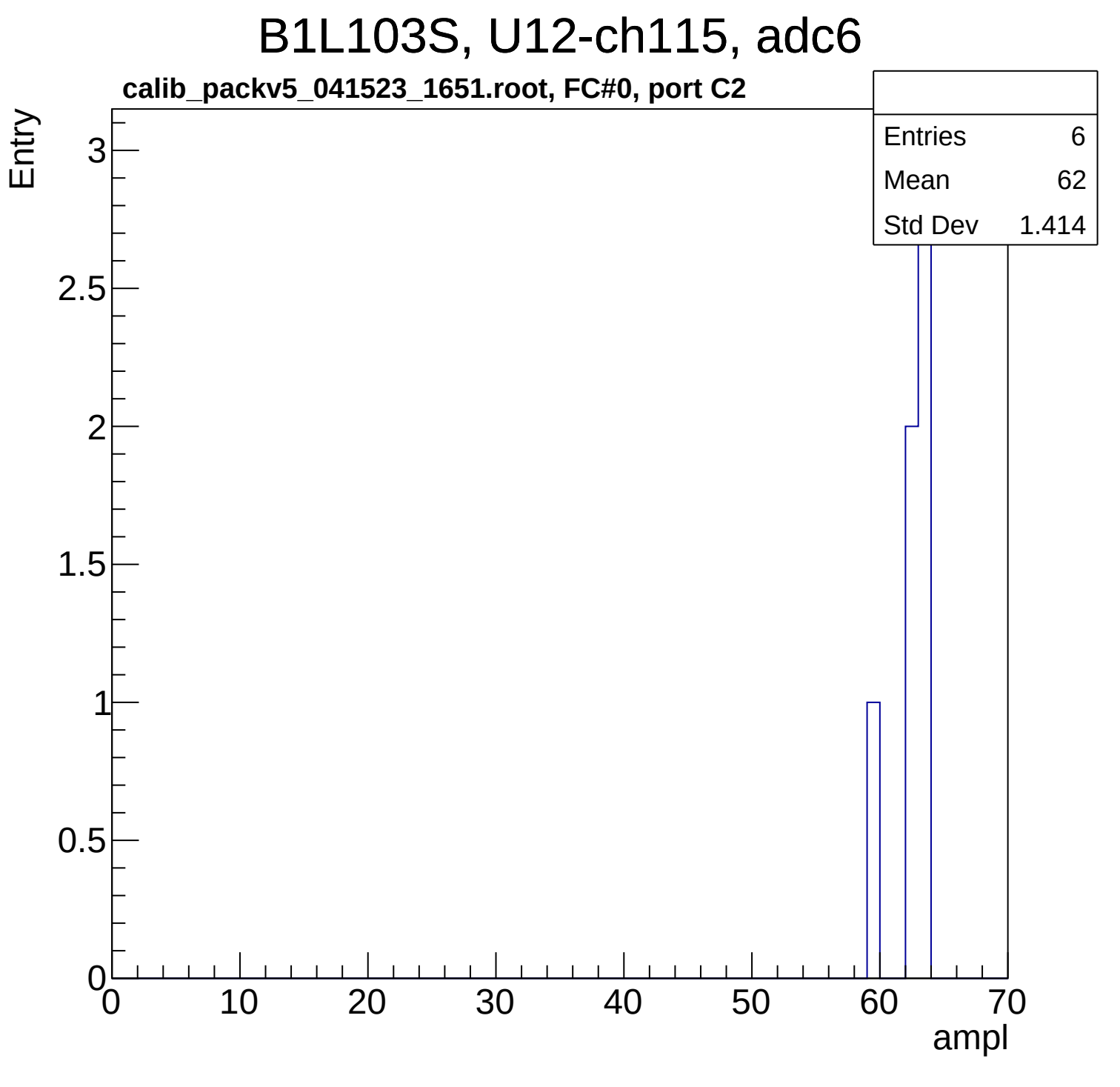
B1L103S, U12-ch115, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62
Std Dev 1.414
Entry
ampl
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1.5
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0
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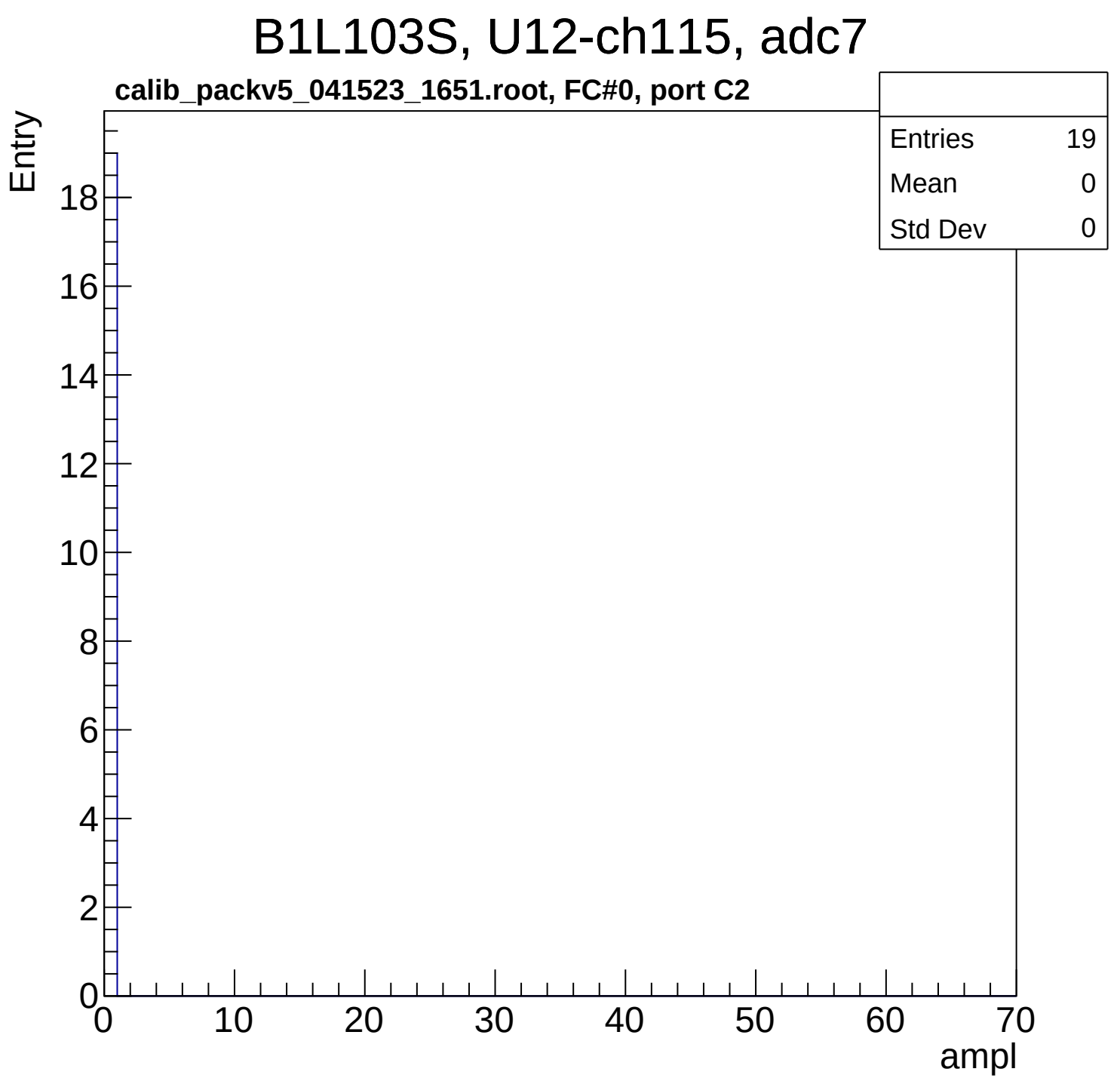
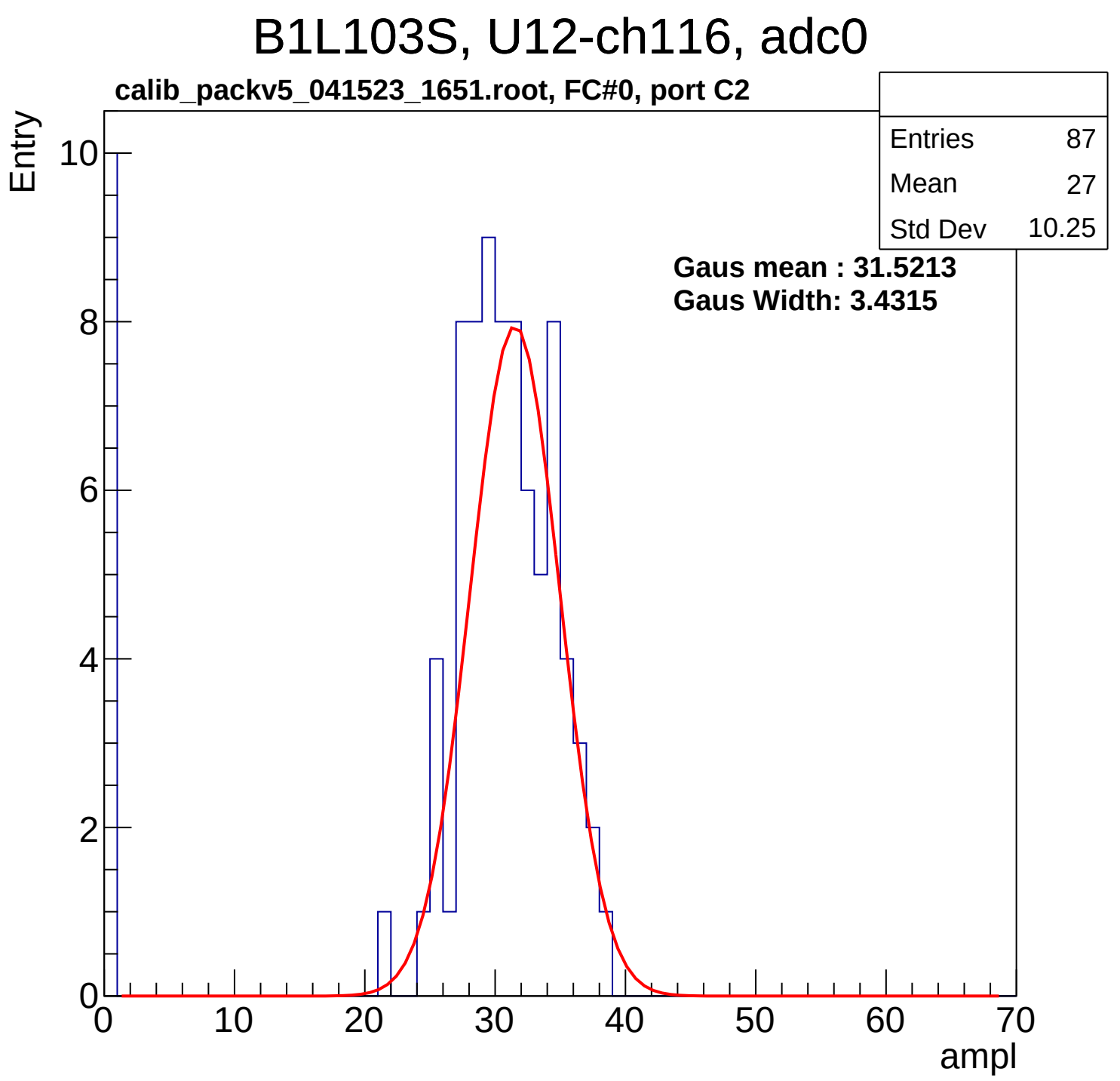
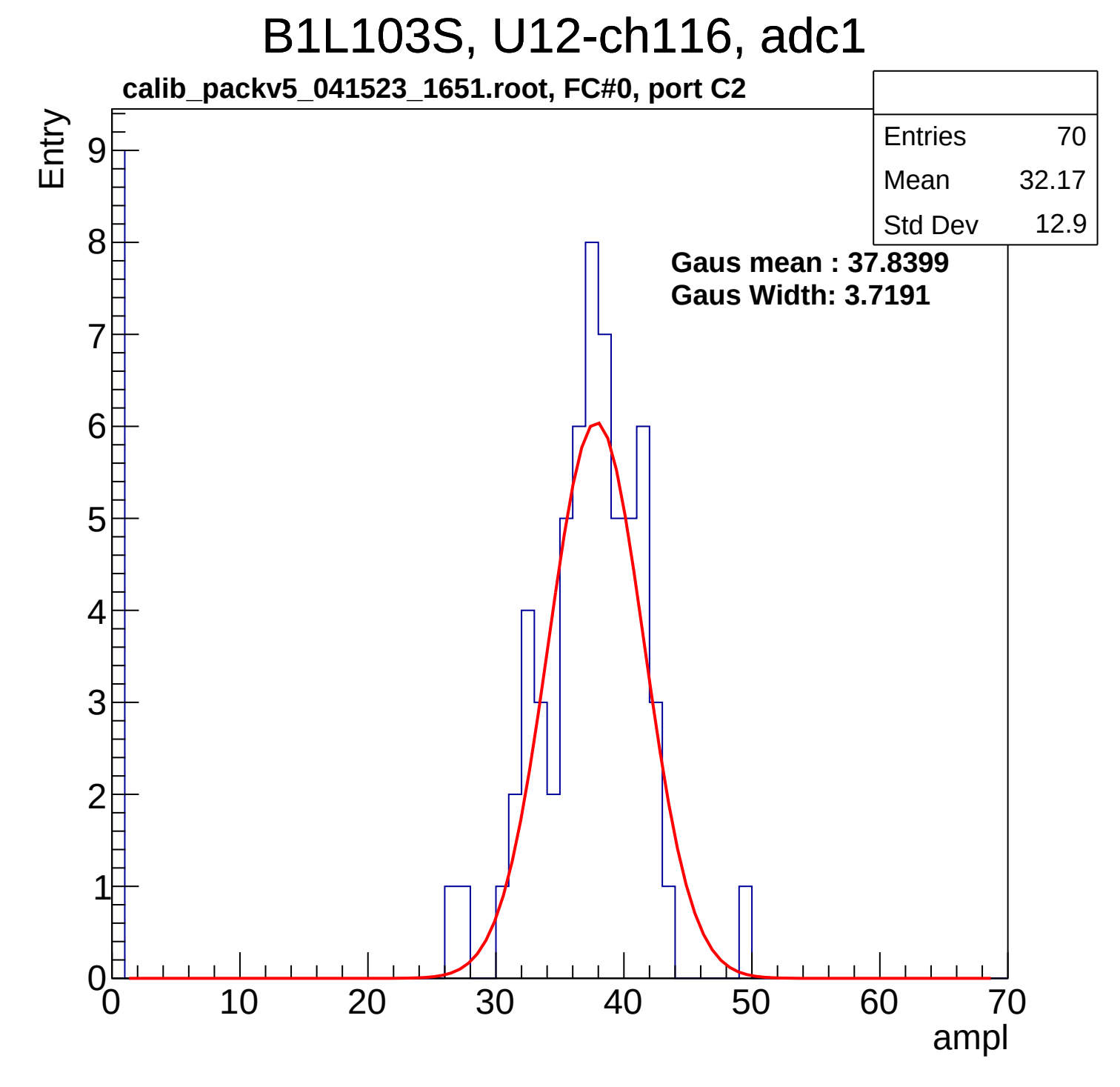

B1L103S, U12-ch115, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch116, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 27
Std Dev 10.25
Gaus mean : 31.5213
Gaus Width: 3.4315
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch116, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 32.17
Std Dev 12.9
Gaus mean : 37.8399
Gaus Width: 3.7191
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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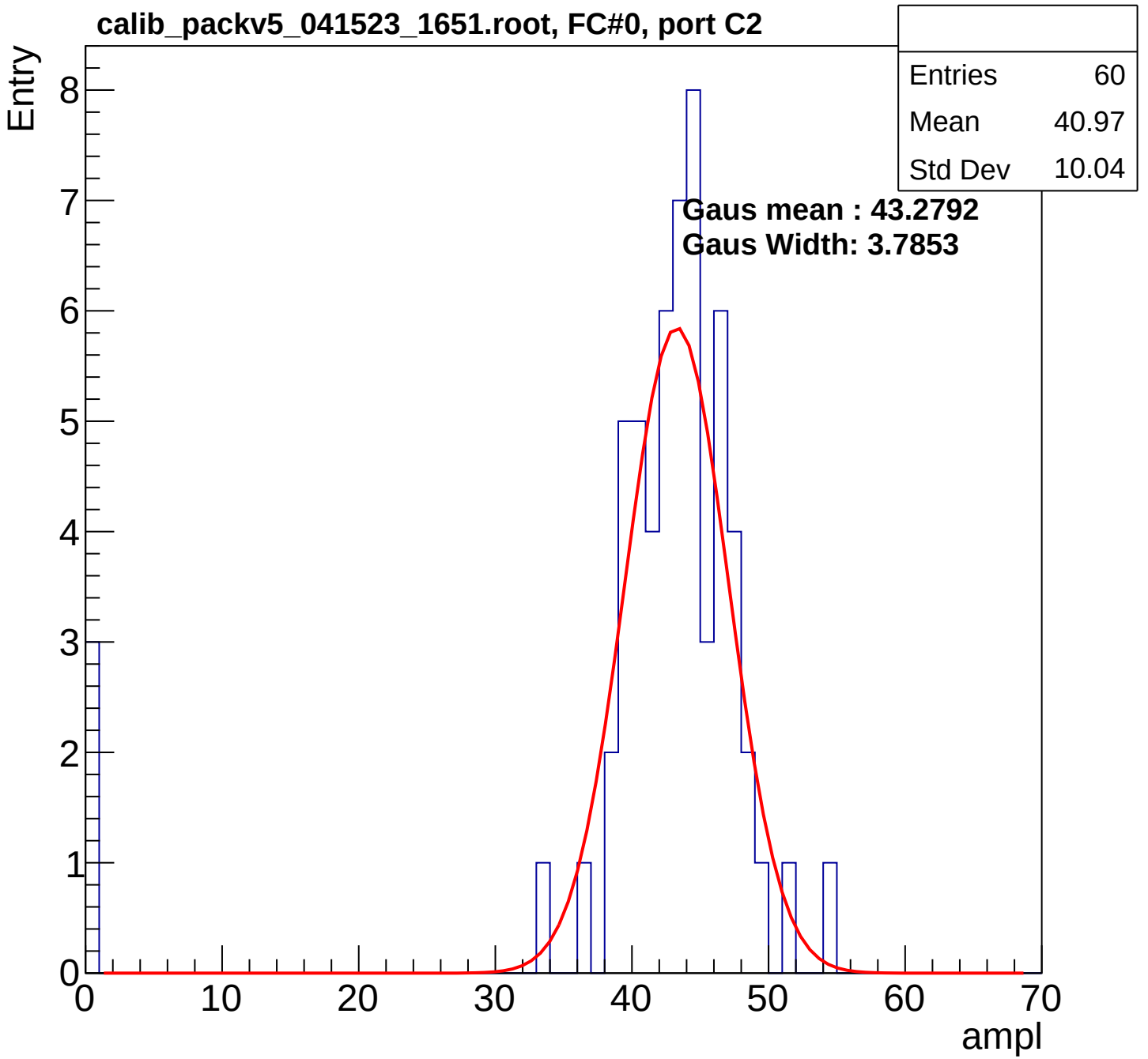
B1L103S, U12-ch116, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 40.97
Std Dev 10.04
Gaus mean : 43.2792
Gaus Width: 3.7853
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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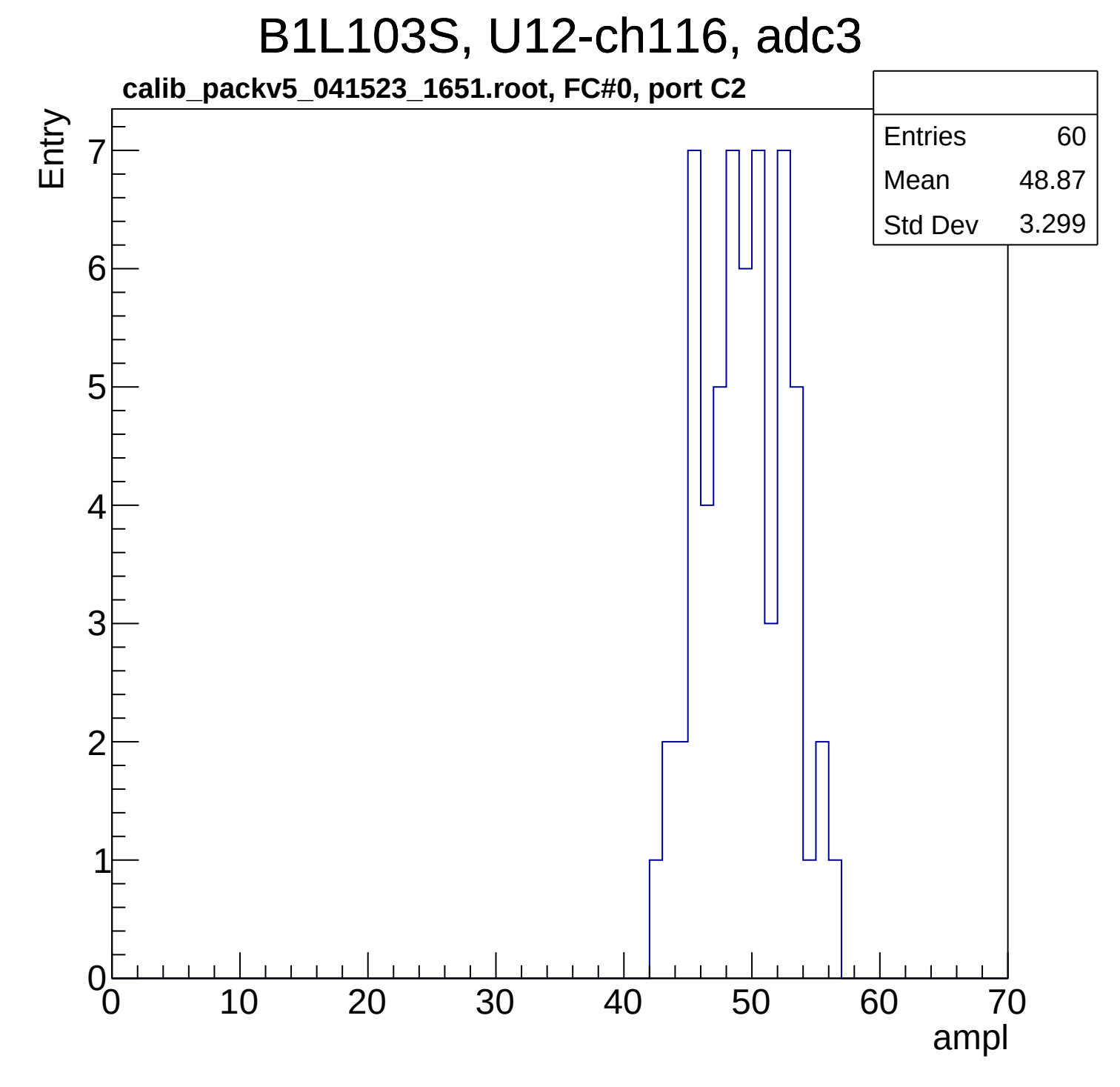
B1L103S, U12-ch116, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 48.87
Std Dev 3.299
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
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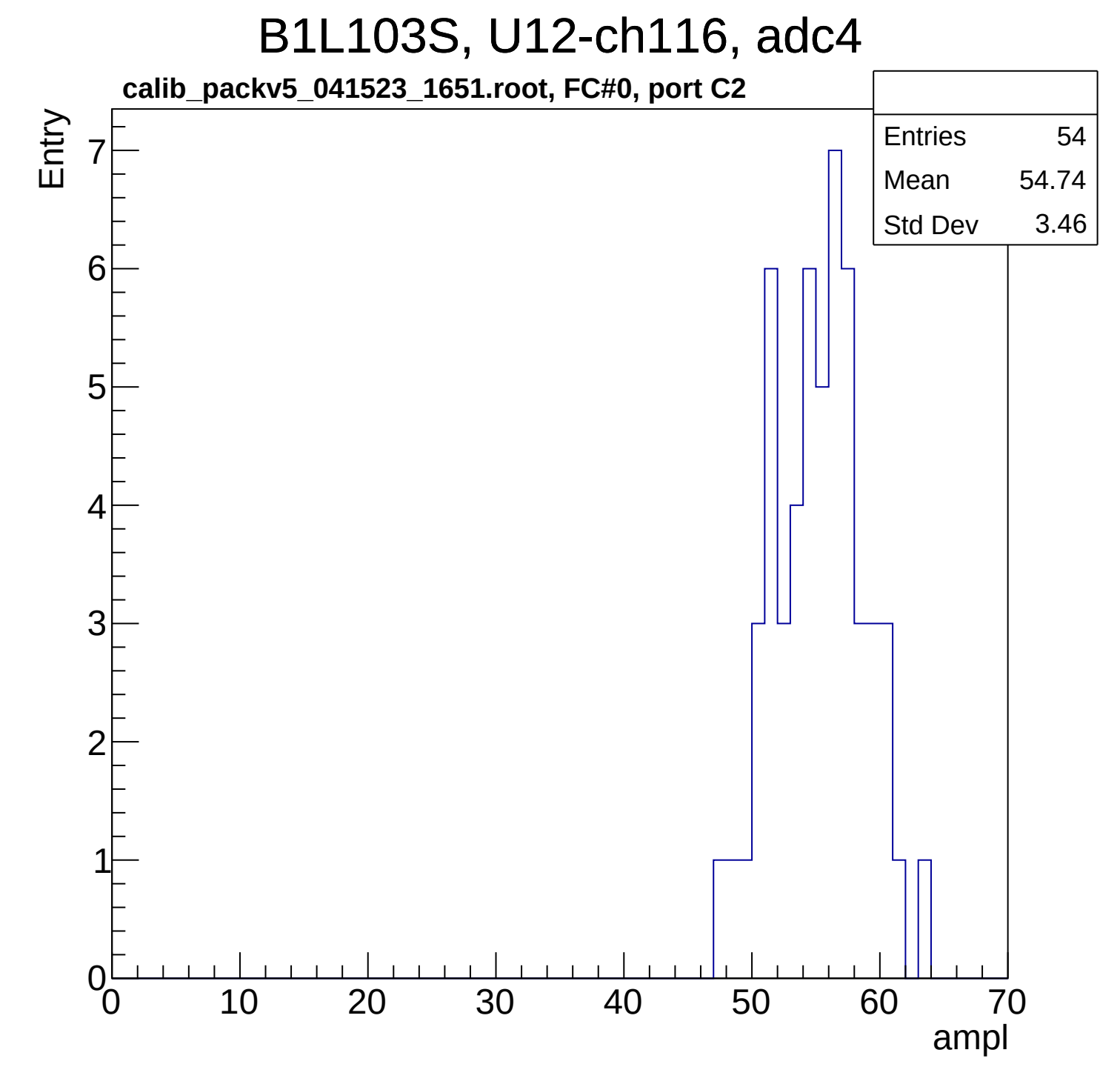
B1L103S, U12-ch116, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 54.74
Std Dev 3.46
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
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40
50
60
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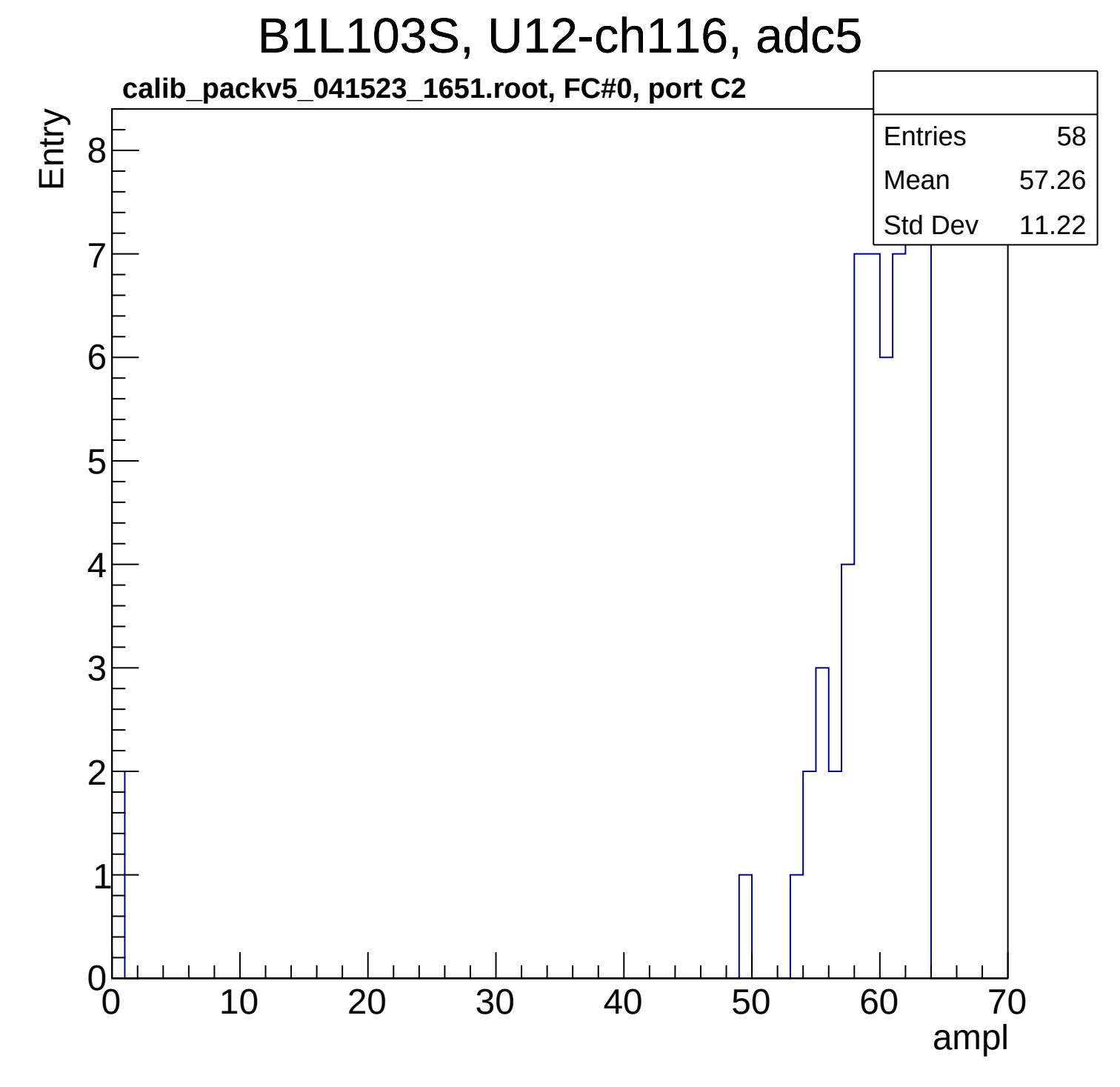
B1L103S, U12-ch116, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 58
Mean 57.26
Std Dev 11.22
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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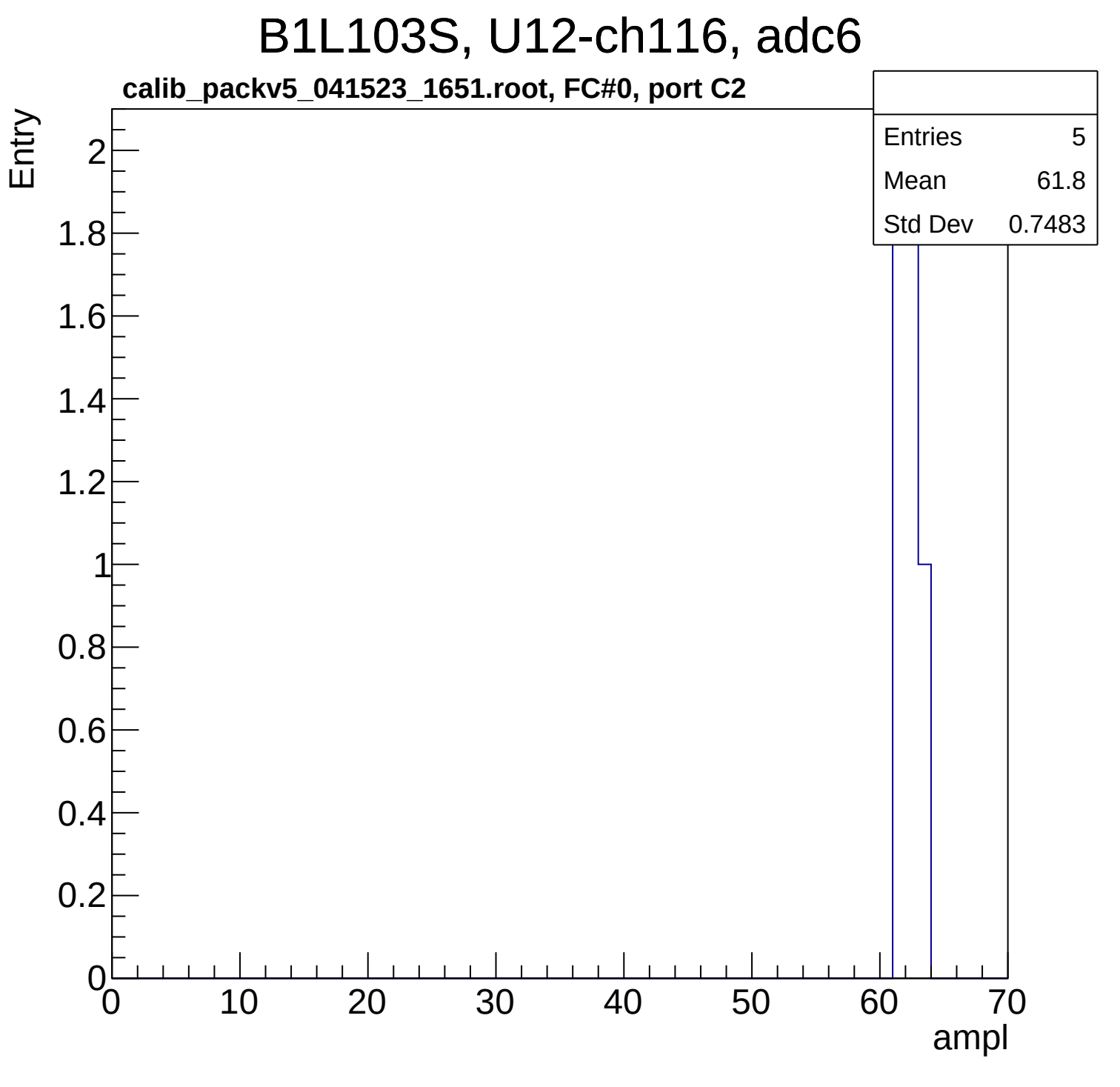
B1L103S, U12-ch116, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 5
Mean 61.8
Std Dev 0.7483
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
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20
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40
50
60
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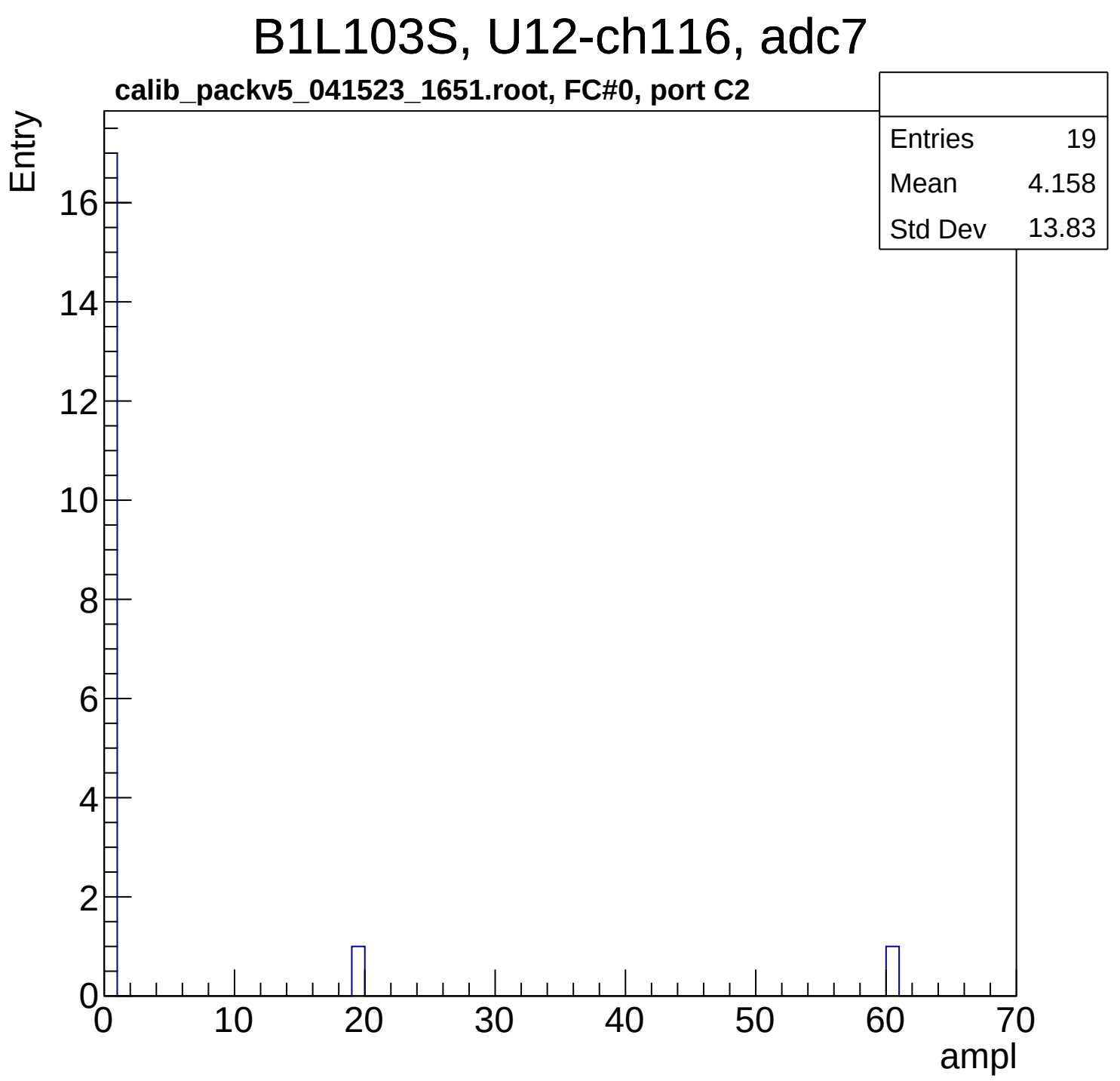
B1L103S, U12-ch116, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 4.158
Std Dev 13.83
Entry
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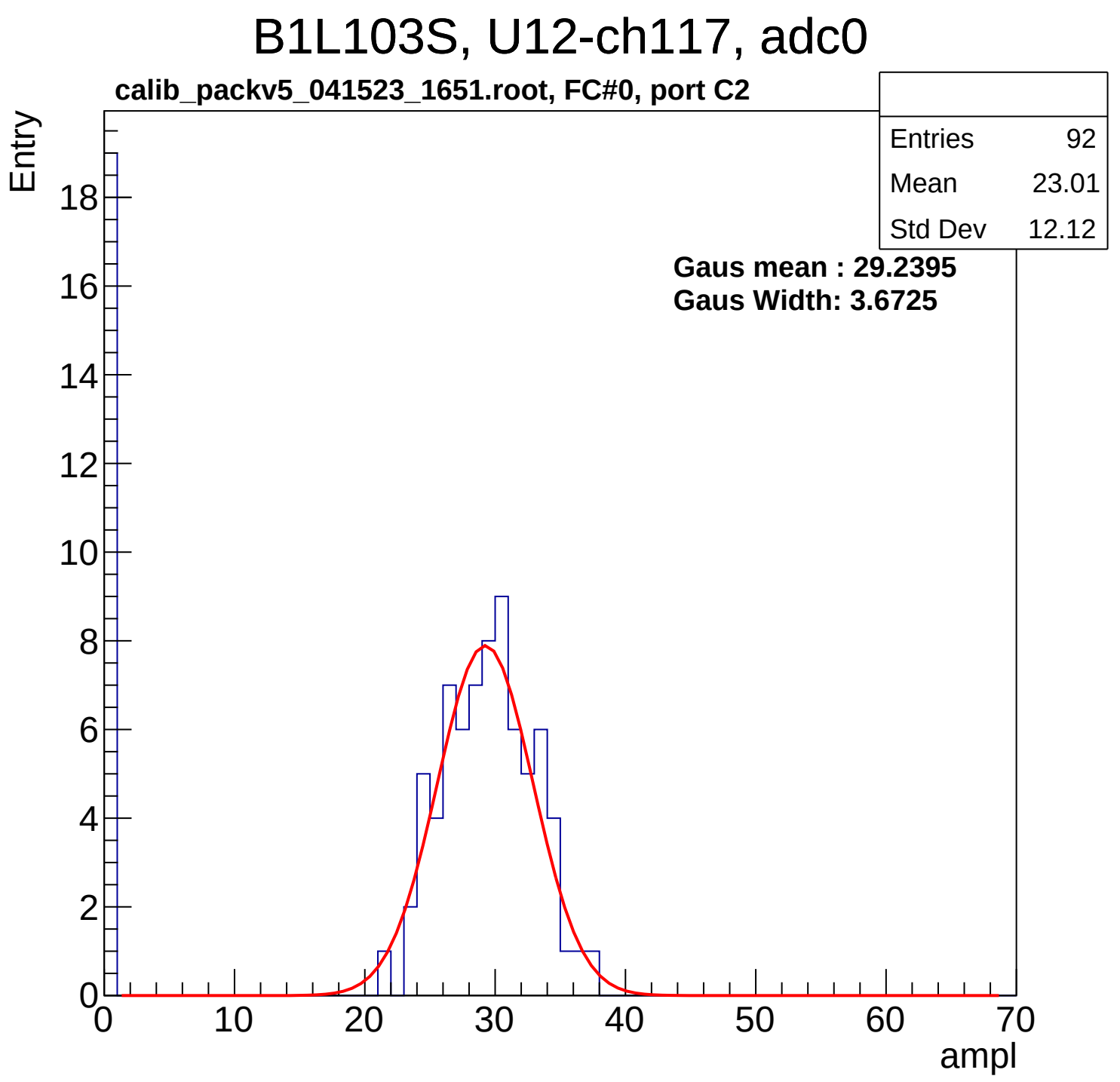
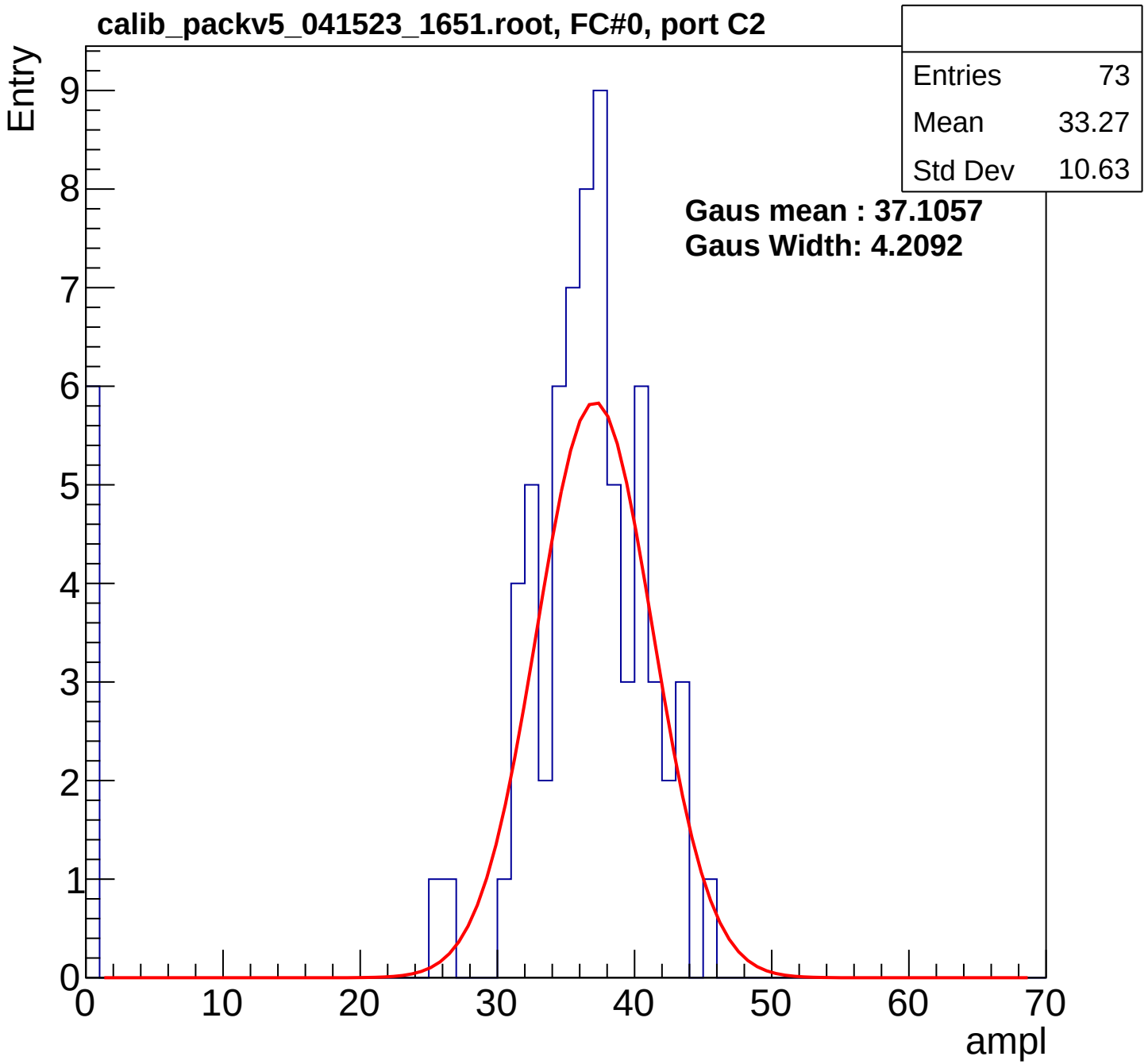
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch117, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 92
Mean 23.01
Std Dev 12.12
Gaus mean : 29.2395
Gaus Width: 3.6725
Entry
ampl
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70


B1L103S, U12-ch117, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 33.27
Std Dev 10.63
Gaus mean : 37.1057
Gaus Width: 4.2092
Entry
ampl
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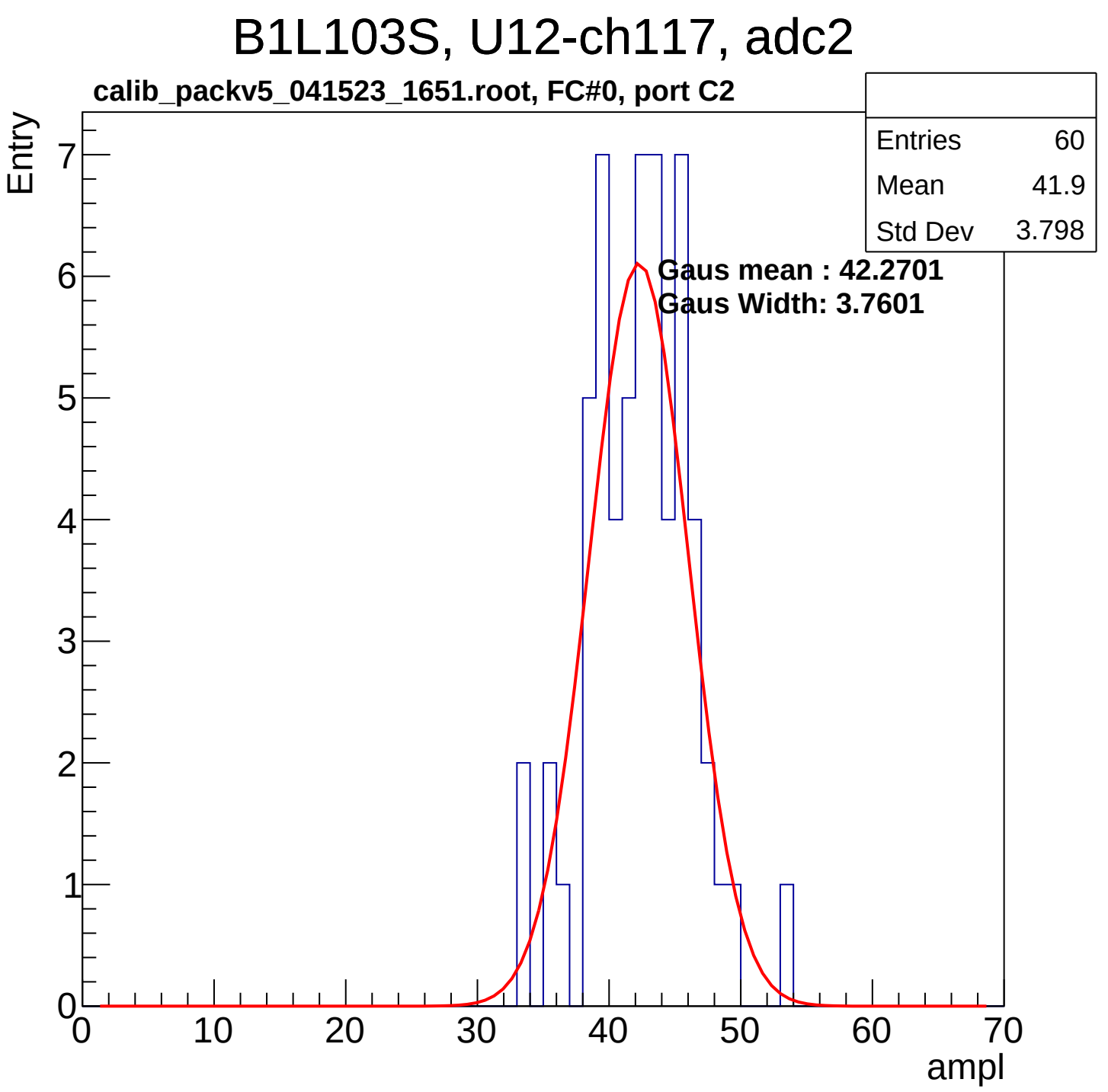
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch117, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 60
Mean 41.9
Std Dev 3.798
Gaus mean : 42.2701
Gaus Width: 3.7601
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
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60
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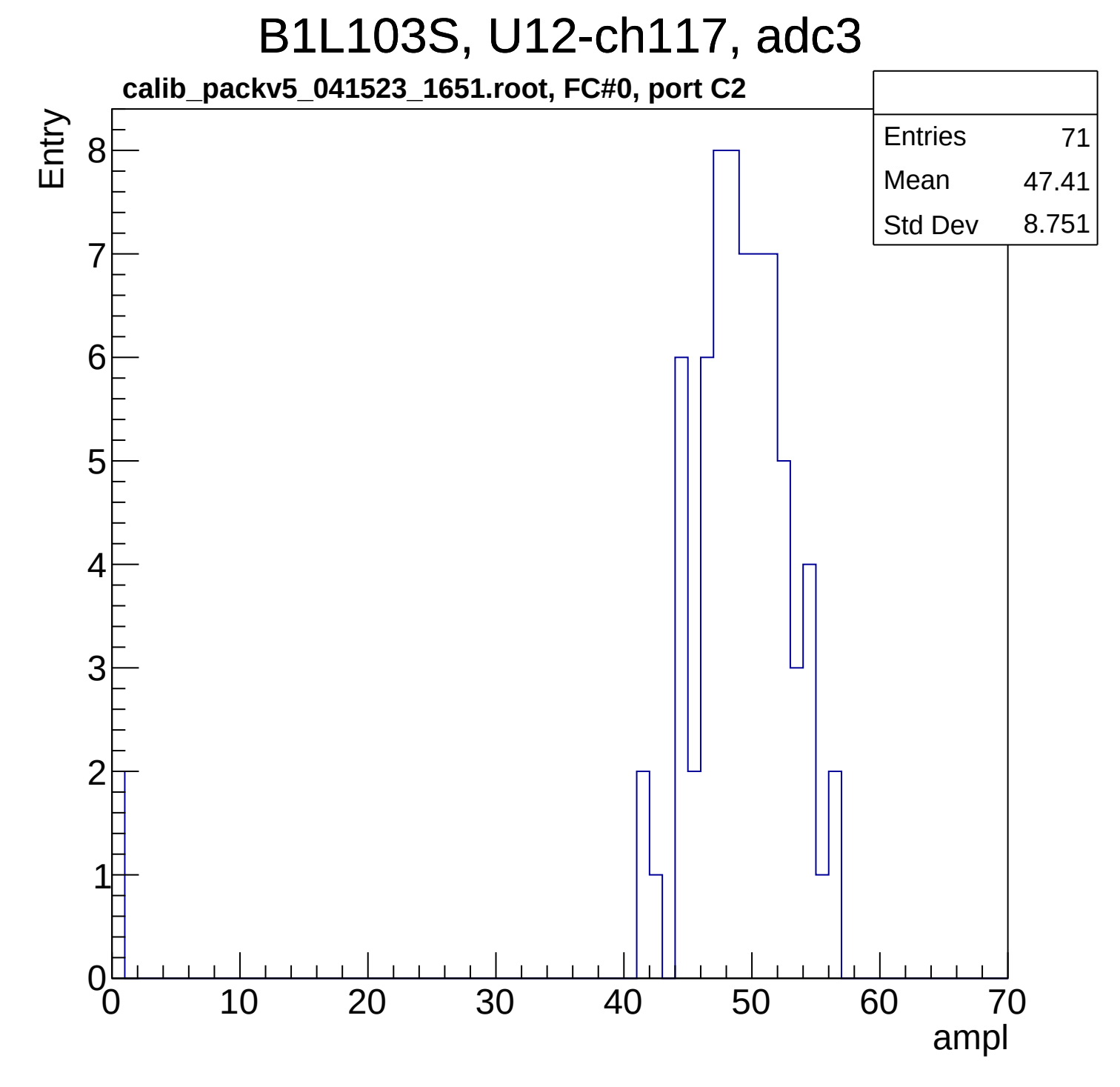
B1L103S, U12-ch117, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 47.41
Std Dev 8.751
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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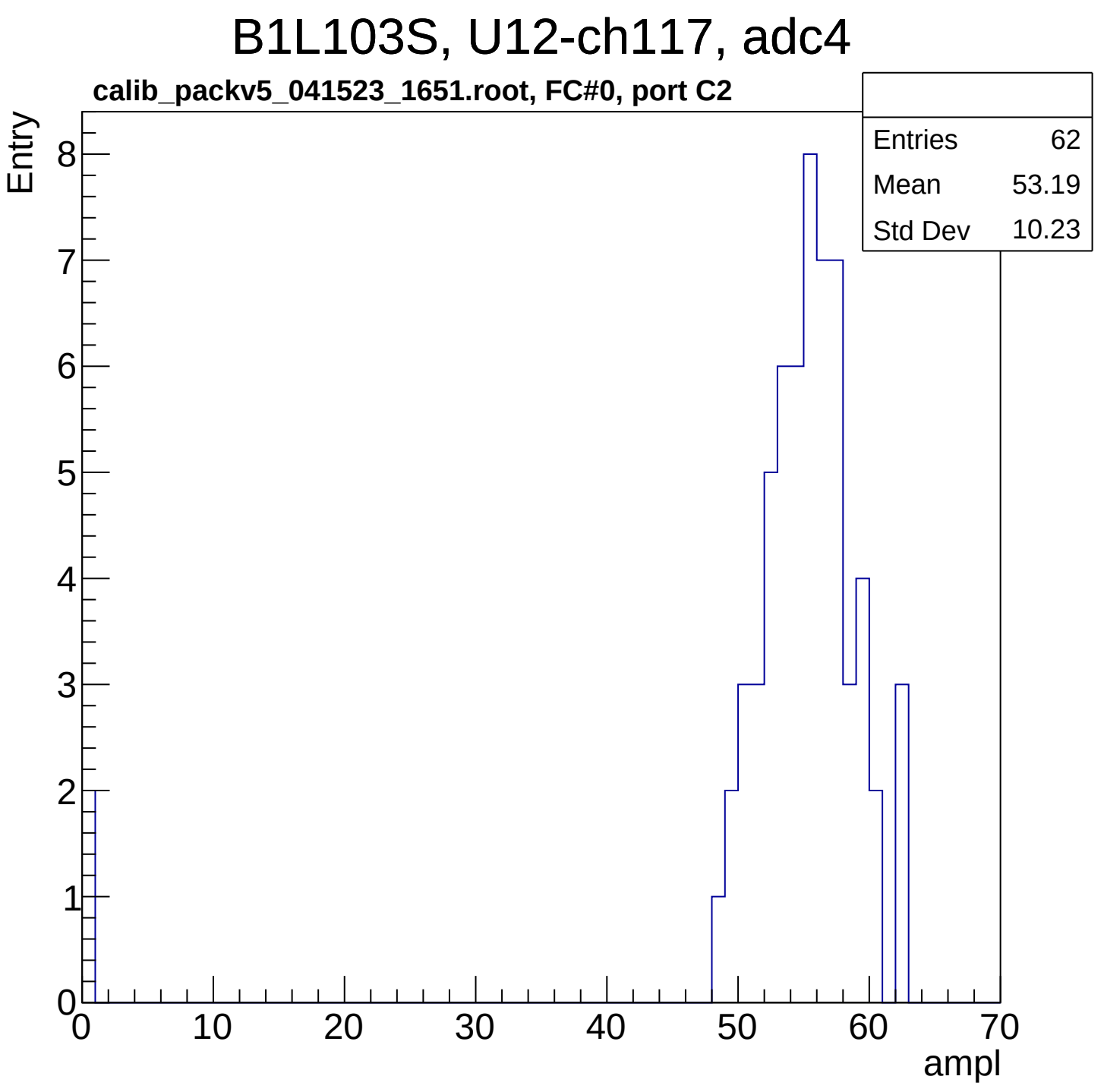
B1L103S, U12-ch117, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 53.19
Std Dev 10.23
Entry
ampl
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1
2
3
4
5
6
7
8
0
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20
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40
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60
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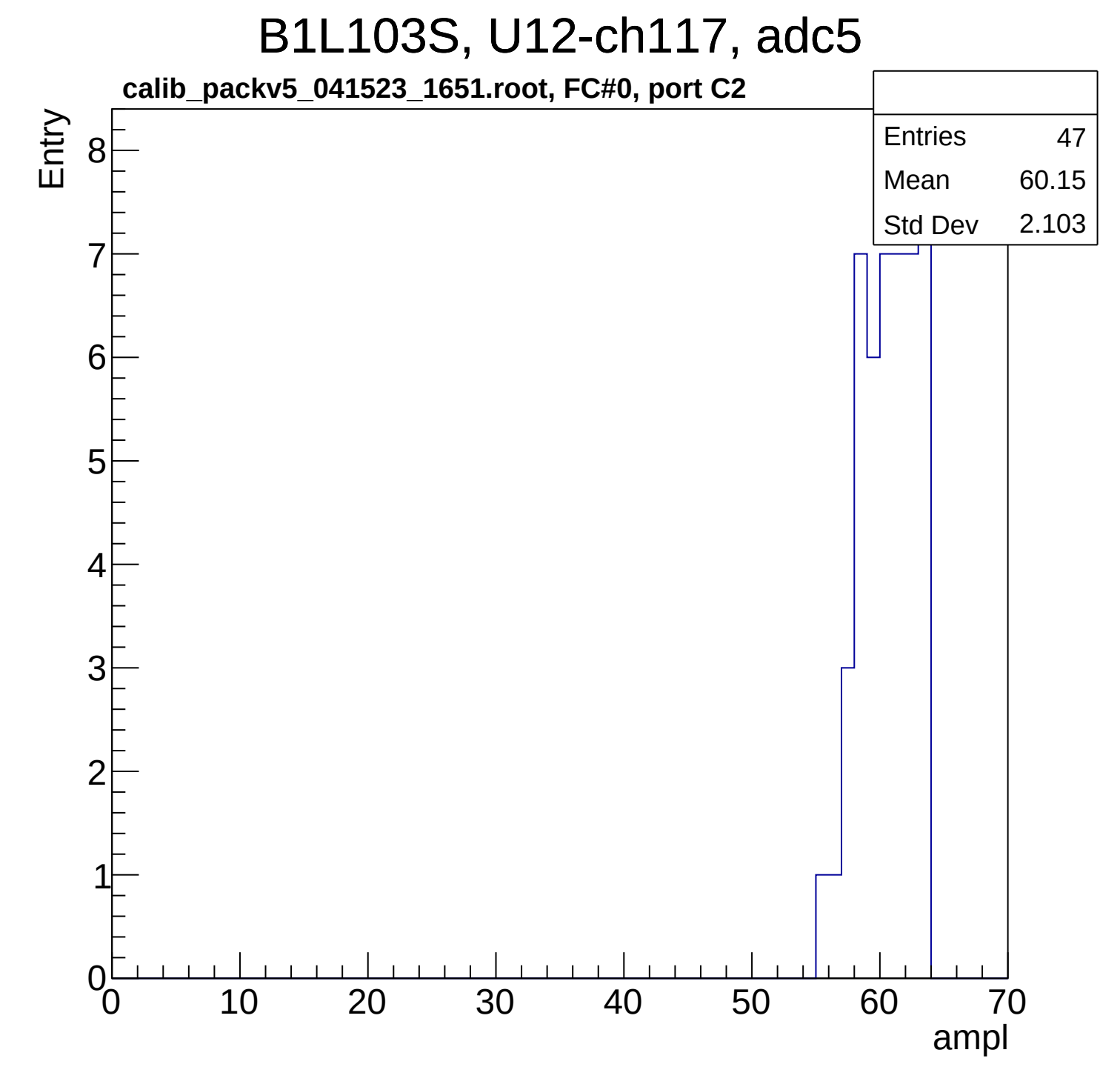
B1L103S, U12-ch117, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 47
Mean 60.15
Std Dev 2.103
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
50
60
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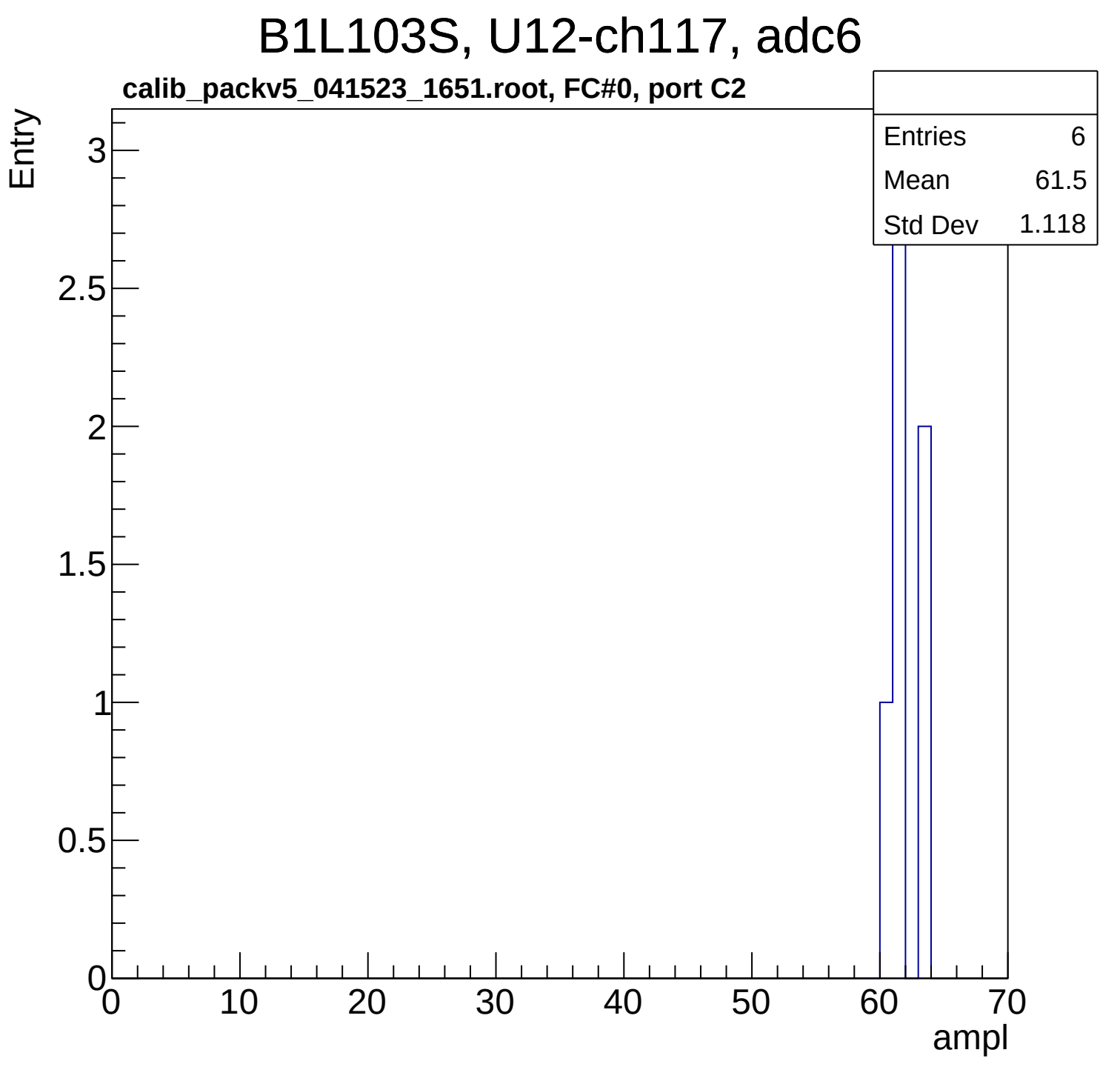
B1L103S, U12-ch117, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.5
Std Dev 1.118
Entry
ampl
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0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
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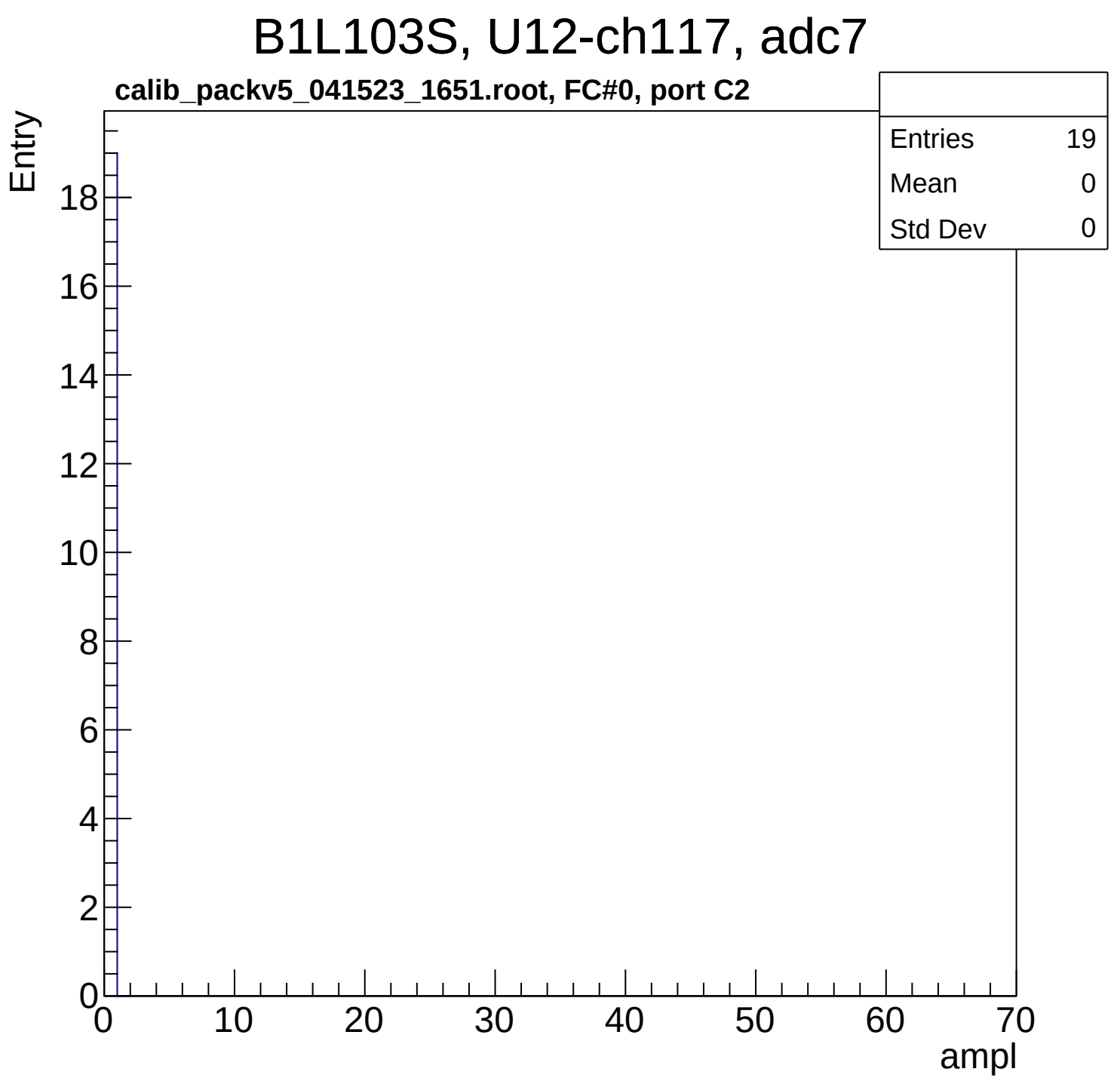
B1L103S, U12-ch117, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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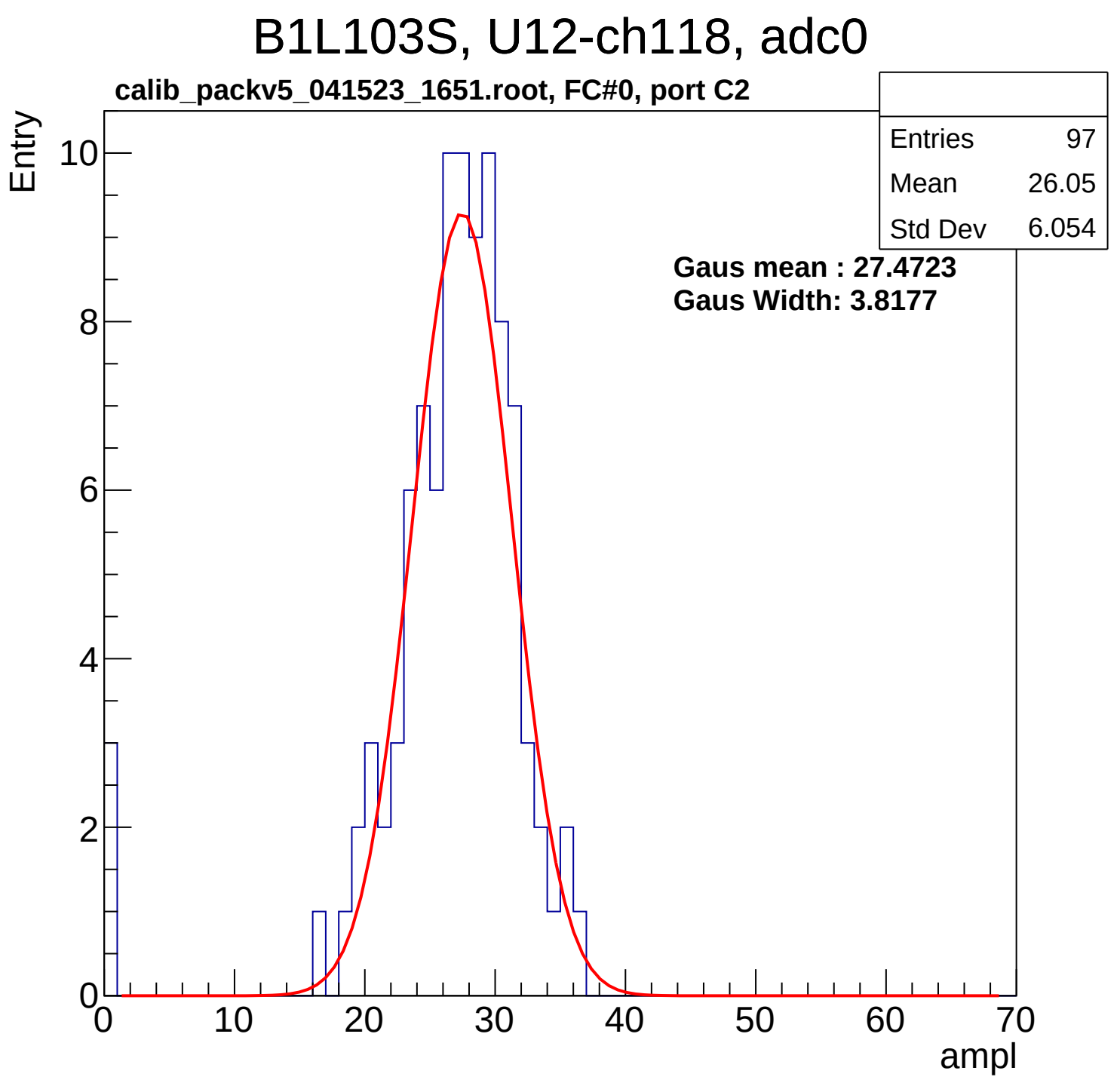
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch118, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 26.05
Std Dev 6.054
Gaus mean : 27.4723
Gaus Width: 3.8177
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
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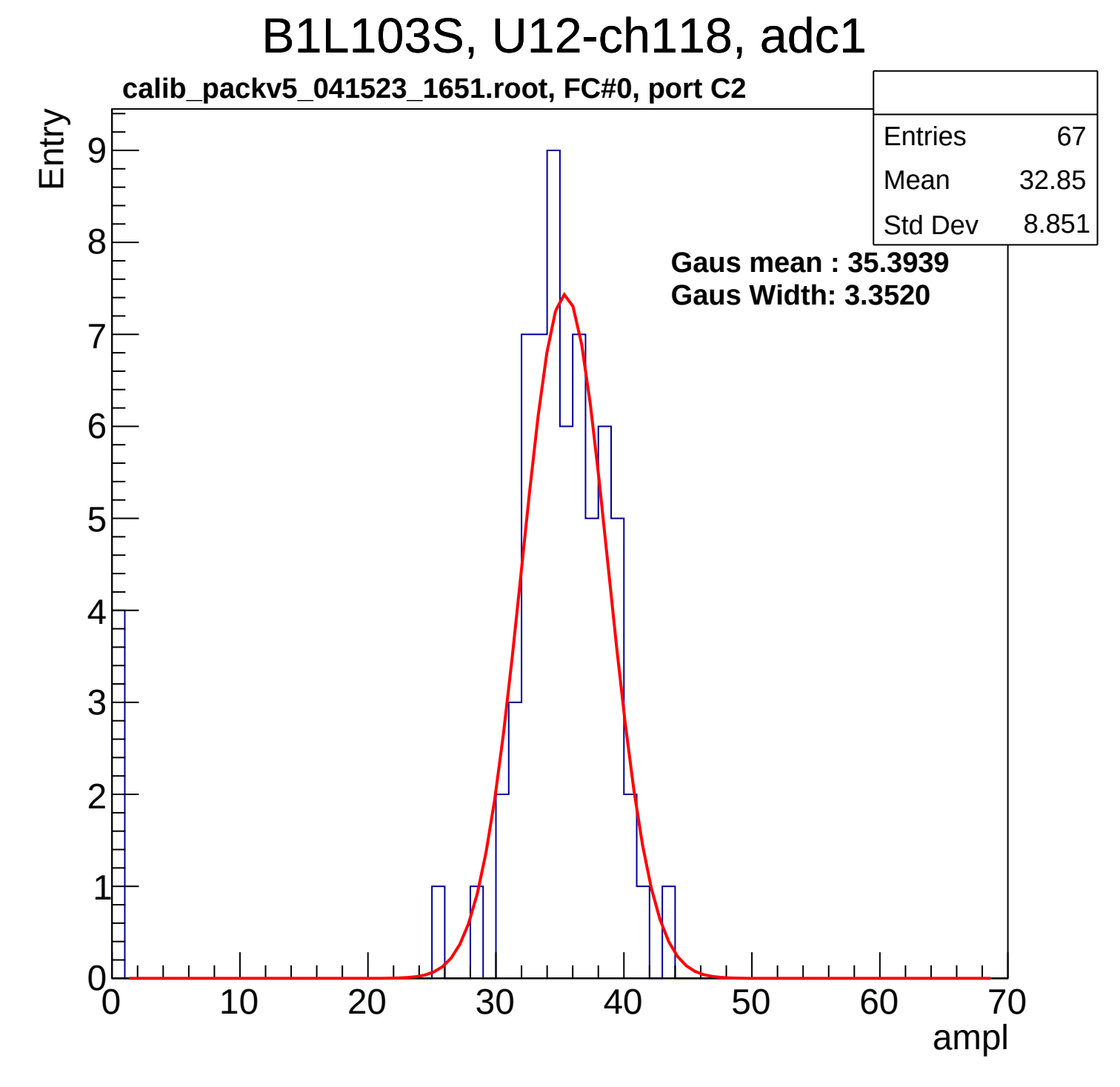
B1L103S, U12-ch118, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 32.85
Std Dev 8.851
Gaus mean : 35.3939
Gaus Width: 3.3520
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
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60
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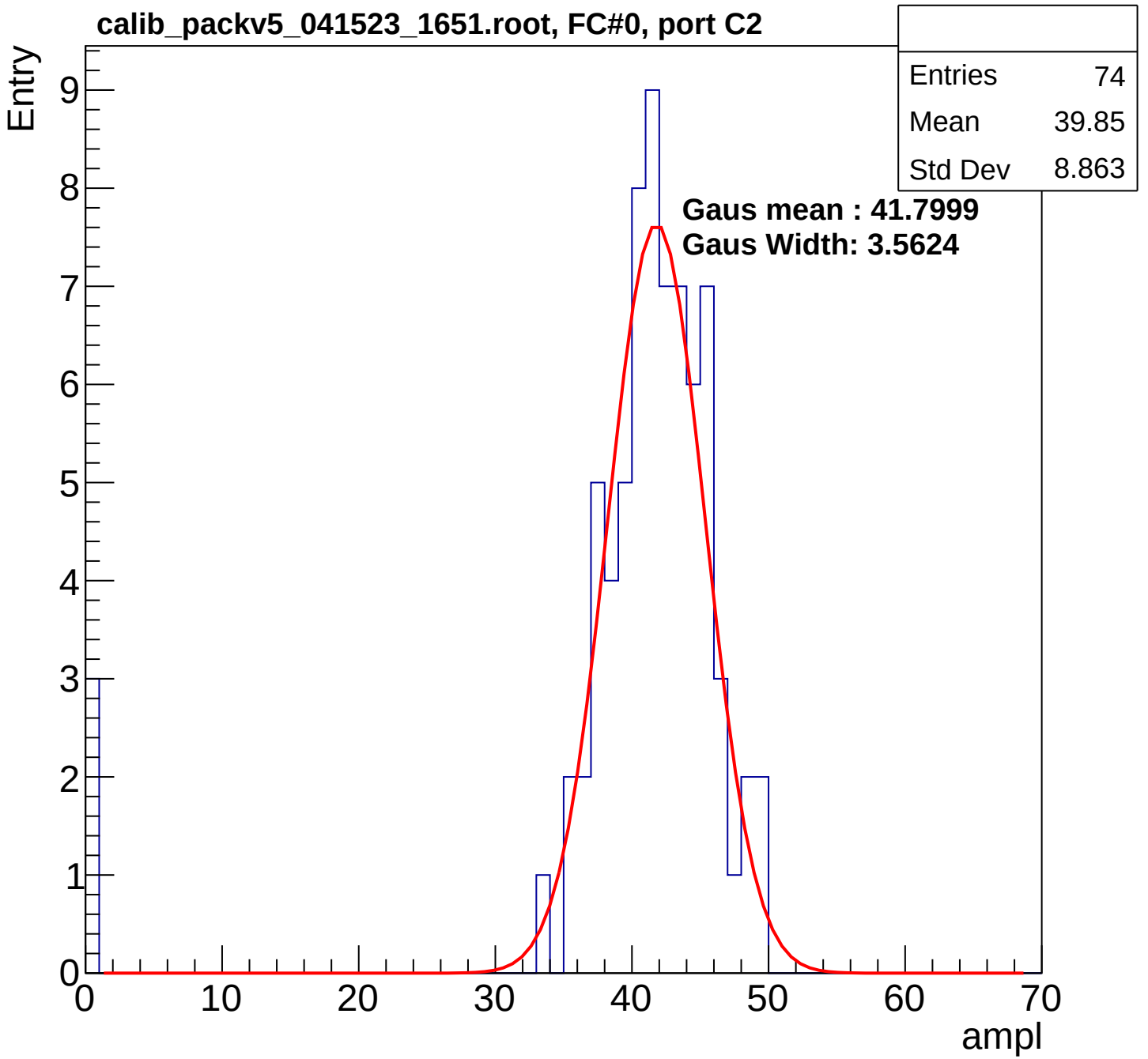
B1L103S, U12-ch118, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 74
Mean 39.85
Std Dev 8.863
Gaus mean : 41.7999
Gaus Width: 3.5624
Entry
ampl
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2
3
4
5
6
7
8
9
0
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60
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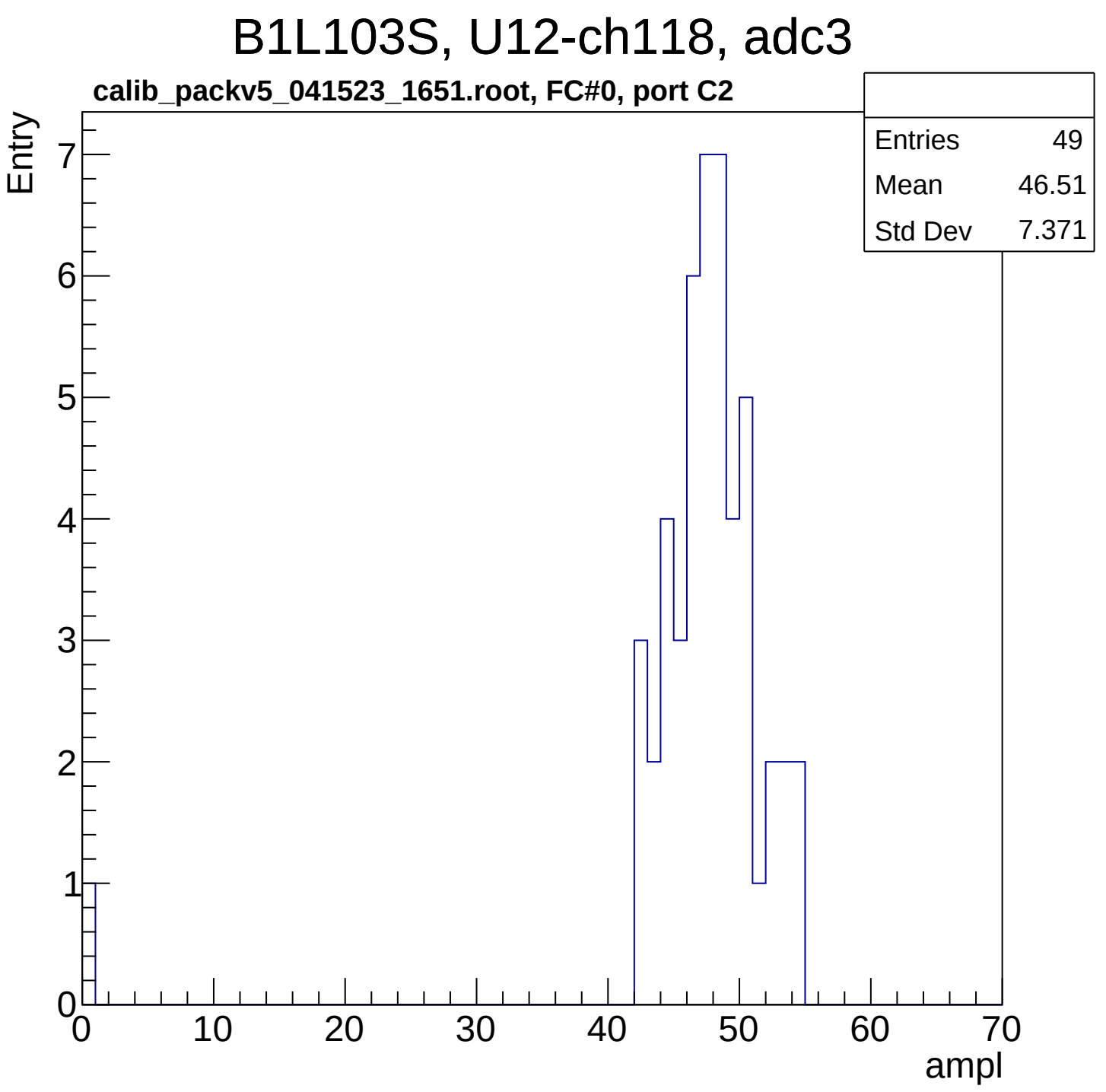
B1L103S, U12-ch118, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 49
Mean 46.51
Std Dev 7.371
Entry
ampl
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6
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0
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40
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60
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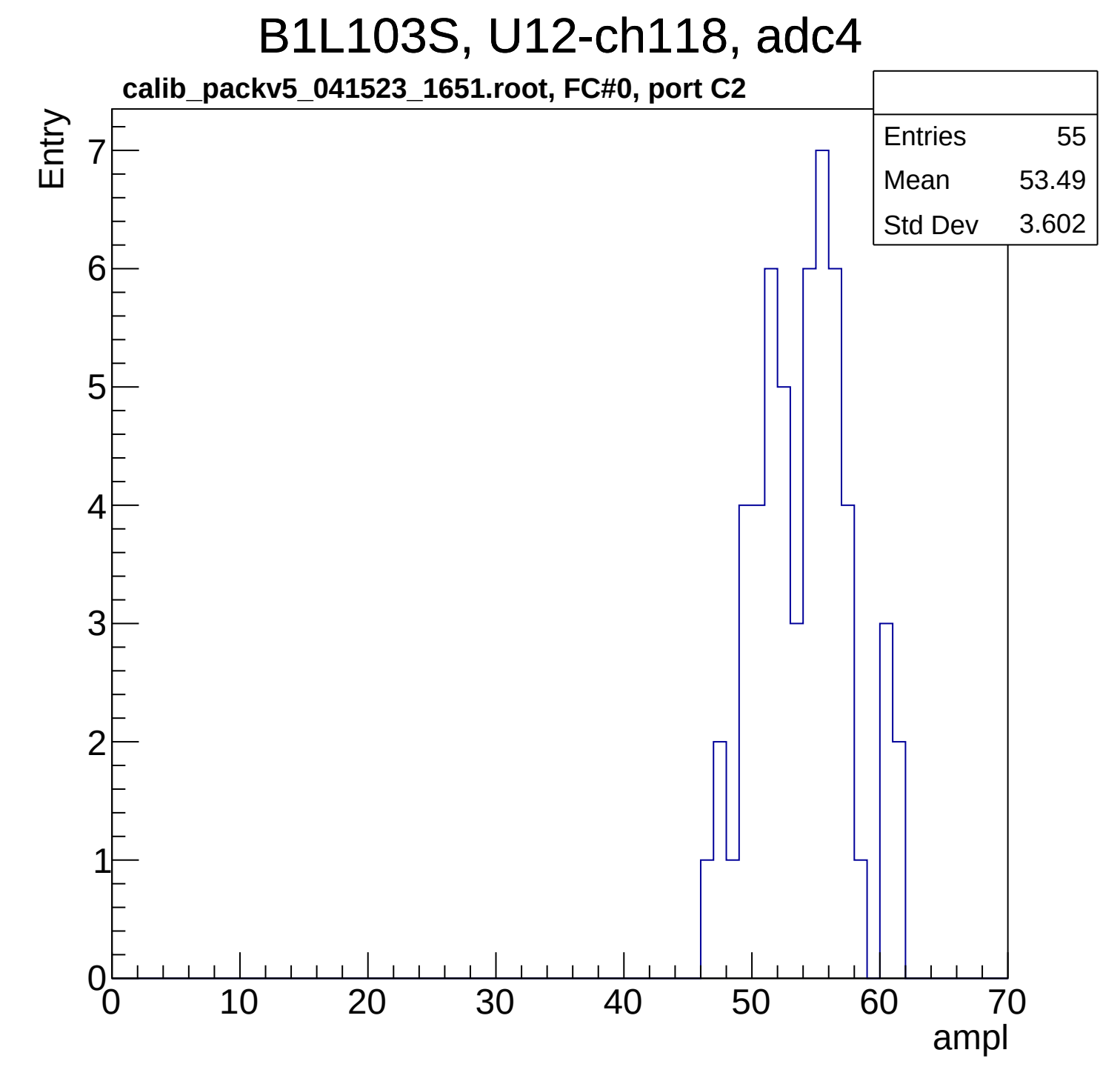
B1L103S, U12-ch118, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 53.49
Std Dev 3.602
Entry
ampl
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3
4
5
6
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0
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40
50
60
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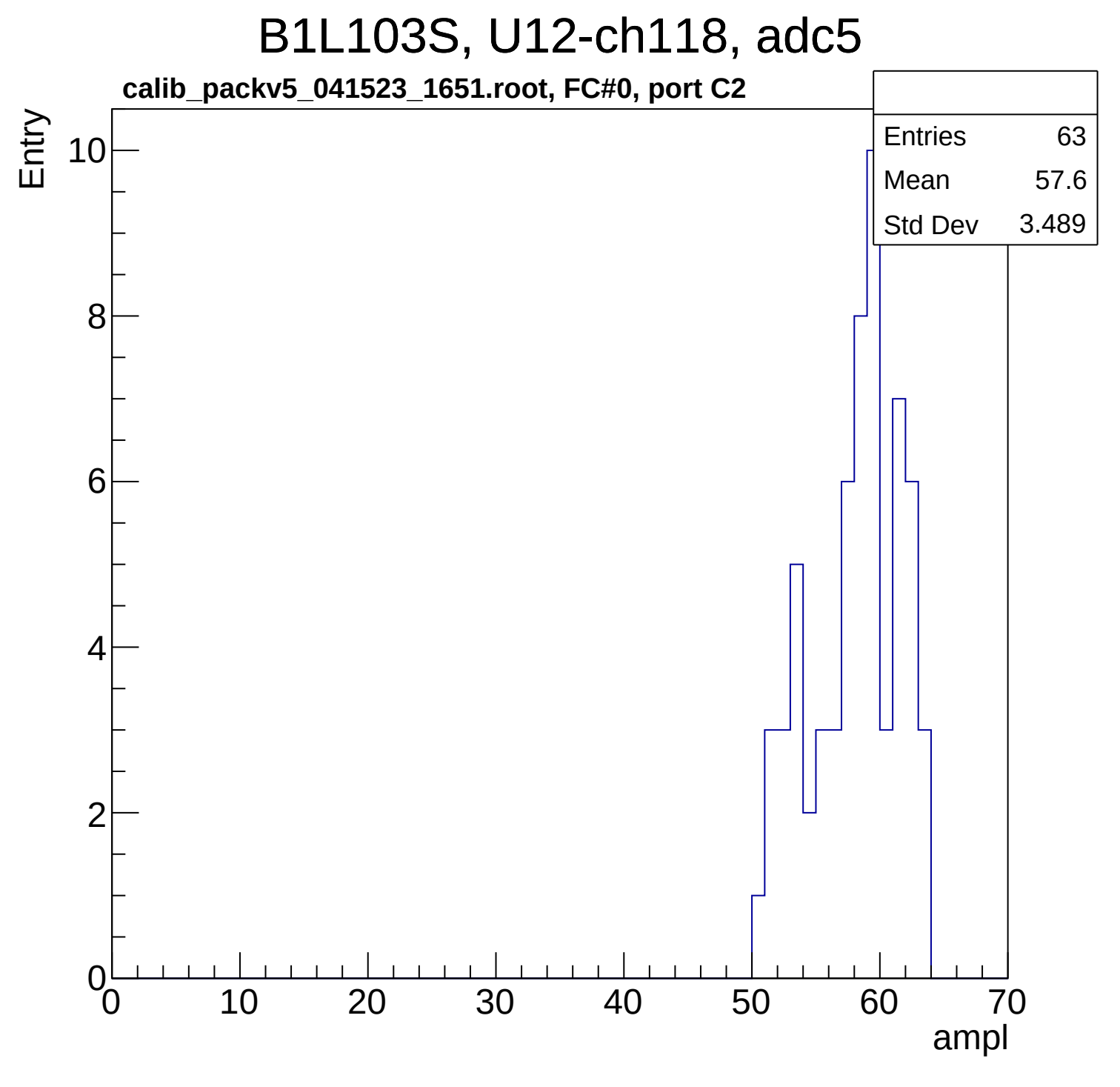
B1L103S, U12-ch118, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 63
Mean 57.6
Std Dev 3.489
Entry
ampl
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2
4
6
8
10
0
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20
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60
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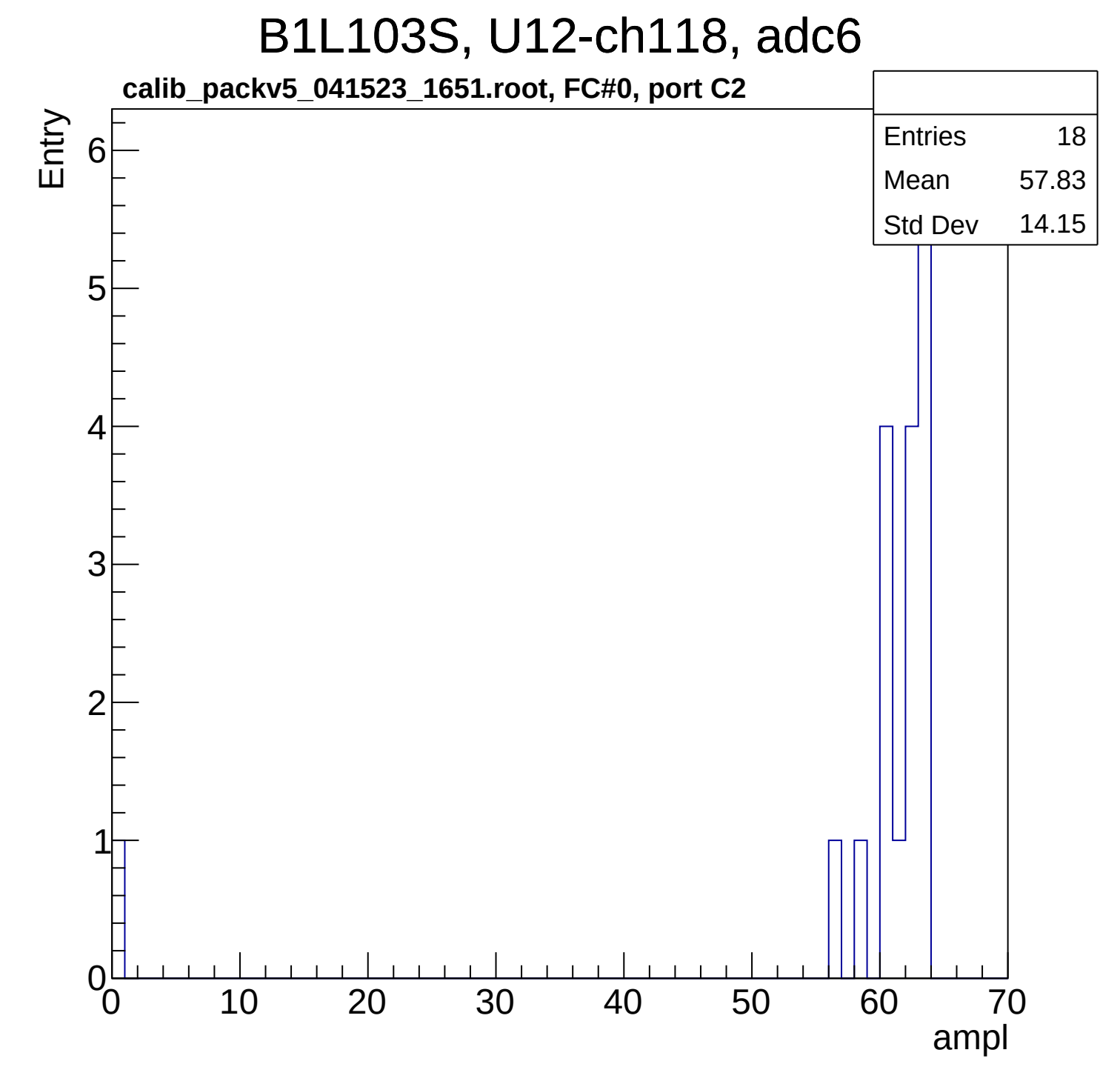
B1L103S, U12-ch118, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 57.83
Std Dev 14.15
Entry
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4
5
6
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10
20
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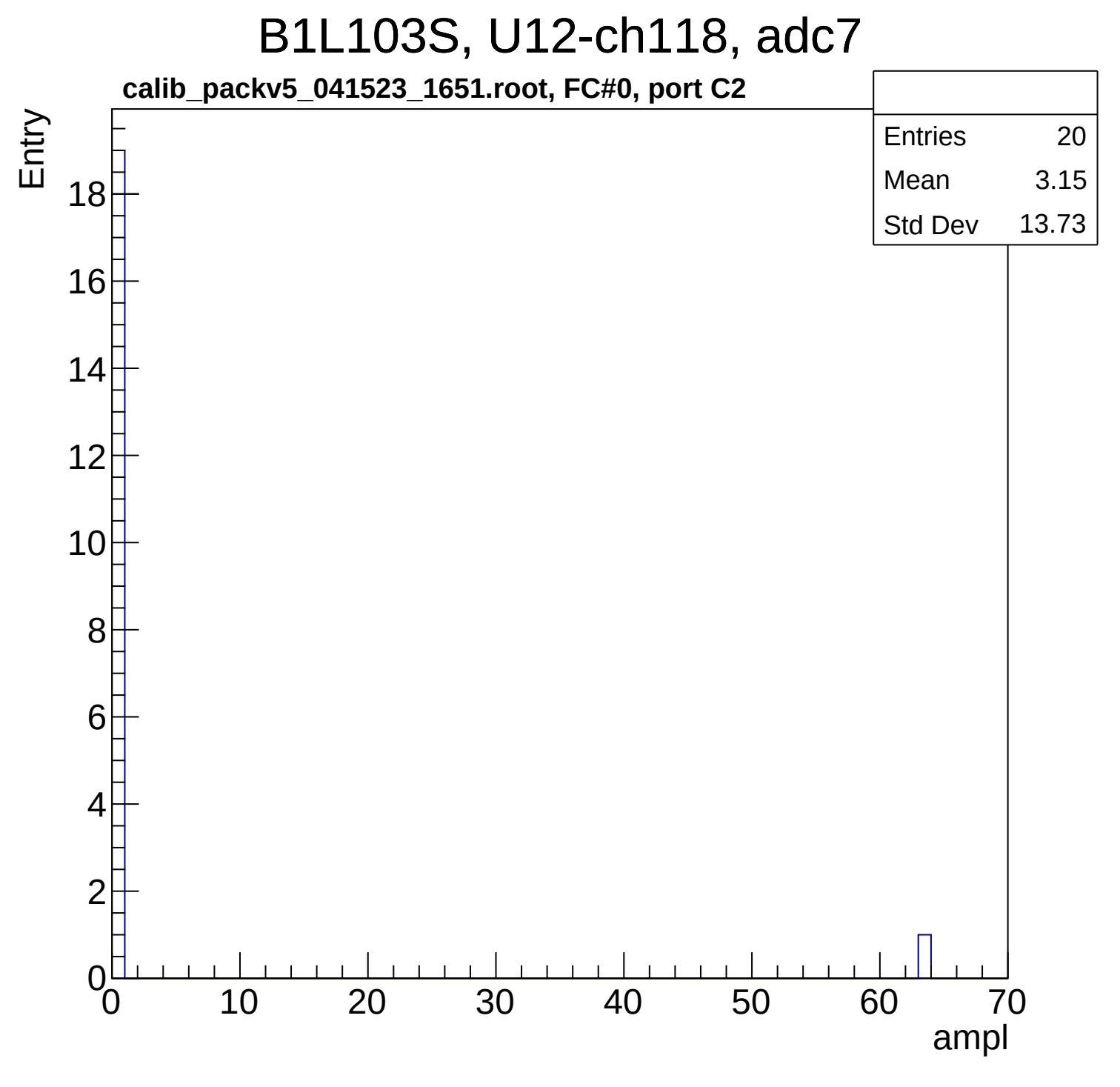
50
60
70
ampl


B1L103S, U12-ch118, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
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10
12
14
16
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10
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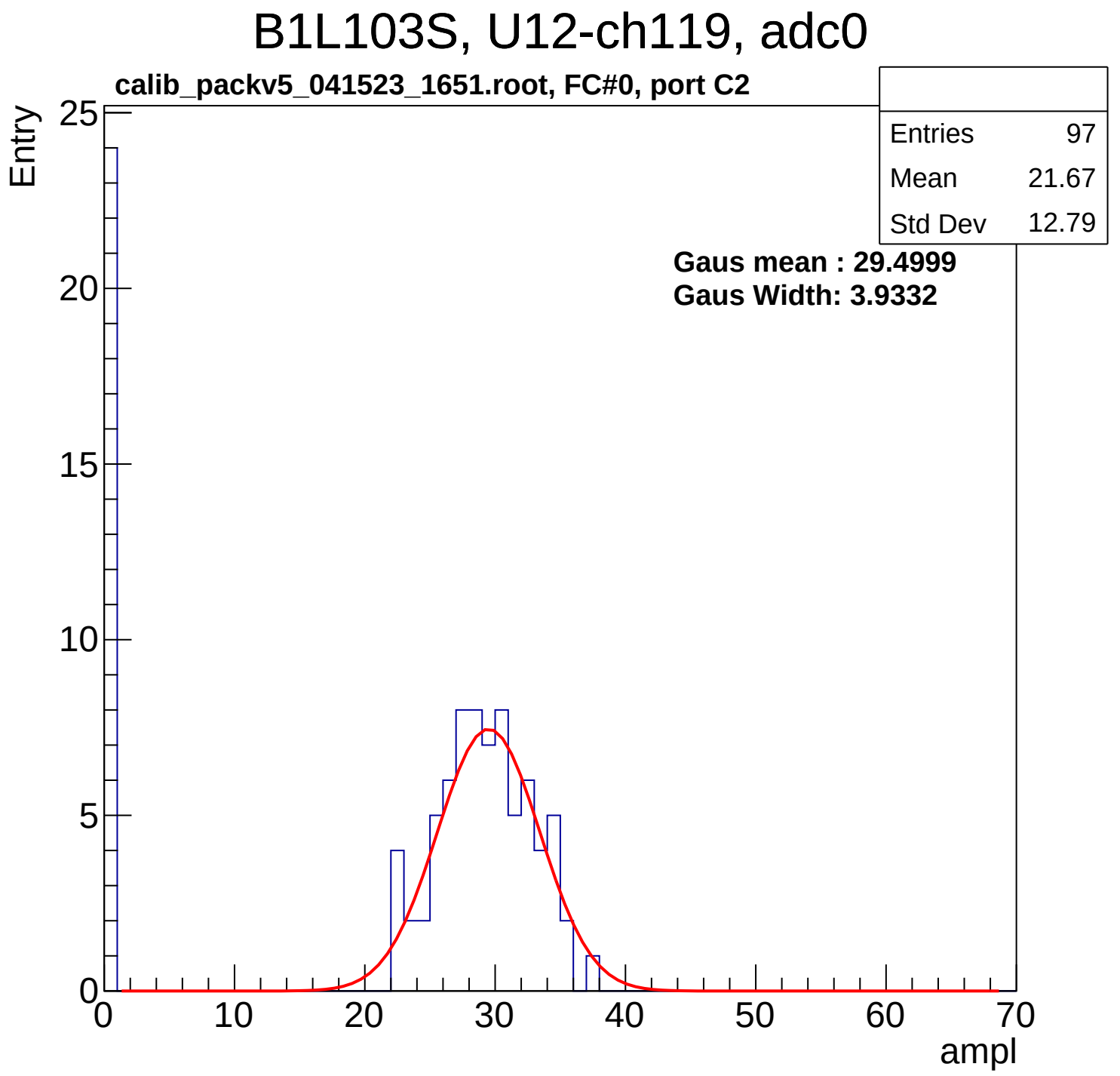
70
ampl


B1L103S, U12-ch119, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 97
Mean 21.67
Std Dev 12.79
Gaus mean : 29.4999
Gaus Width: 3.9332
Entry
ampl
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5
10
15
20
25
0
10
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40
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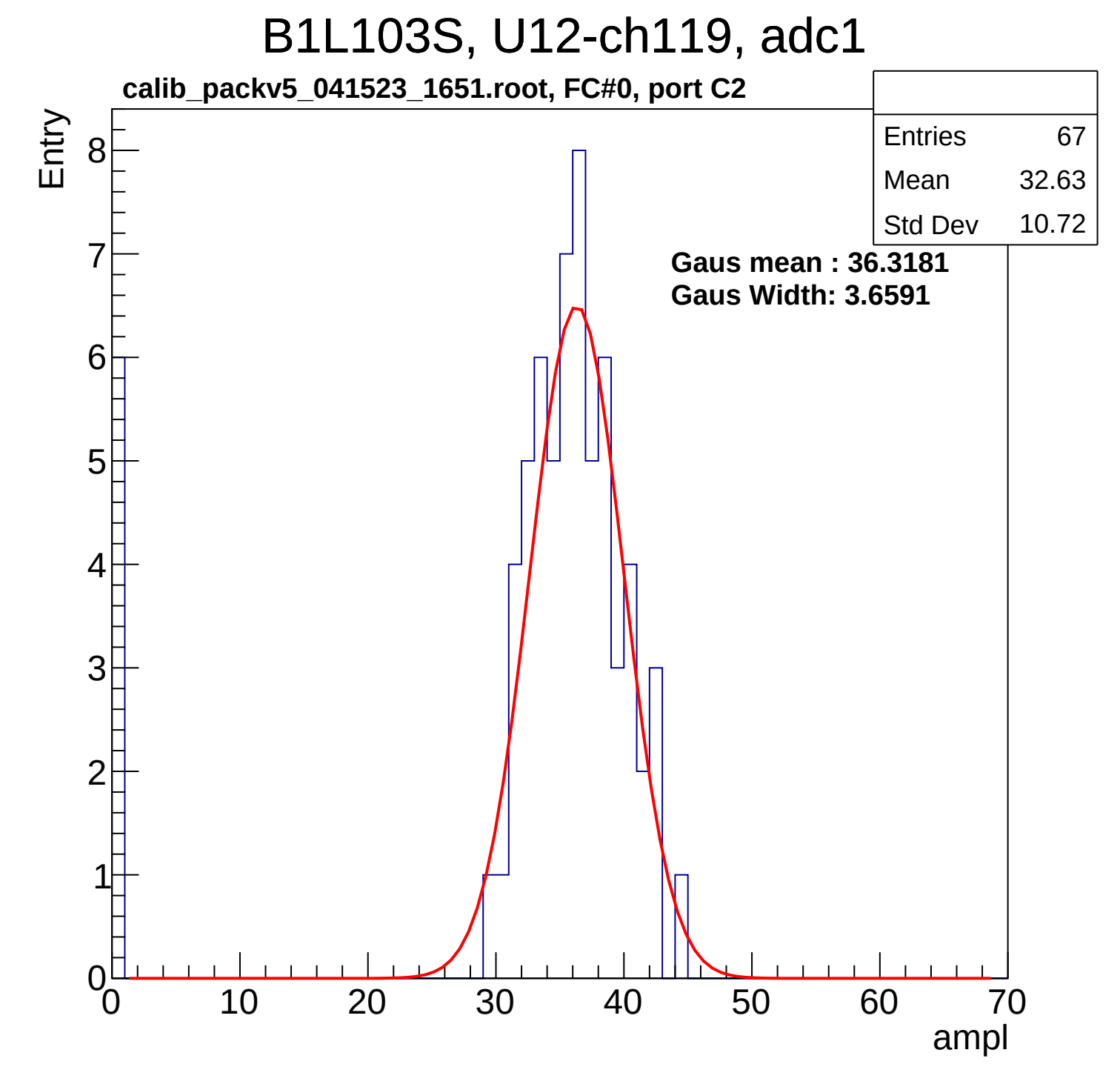
B1L103S, U12-ch119, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 32.63
Std Dev 10.72
Gaus mean : 36.3181
Gaus Width: 3.6591
Entry
ampl
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1
2
3
4
5
6
7
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0
10
20
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40
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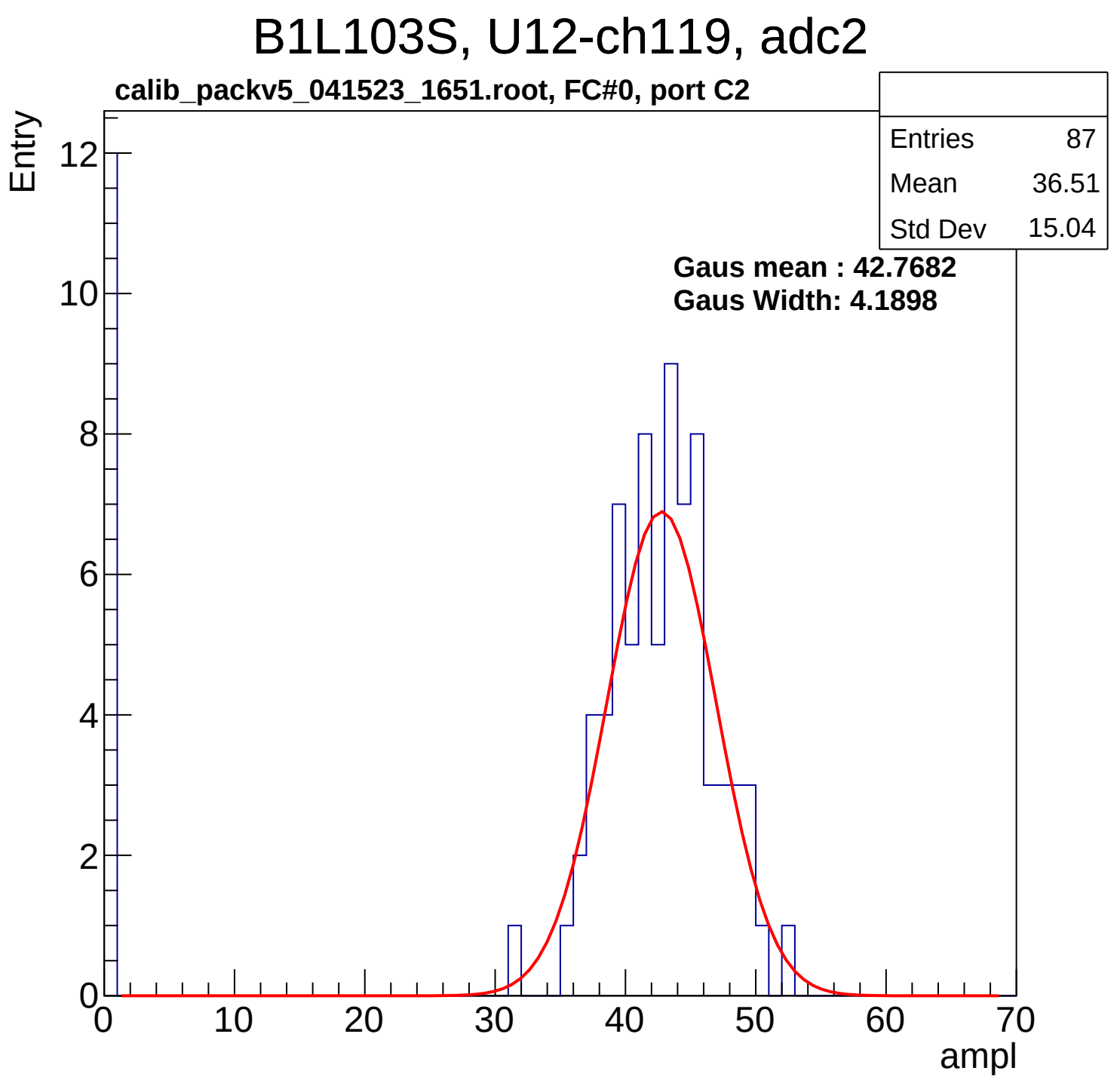
B1L103S, U12-ch119, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 36.51
Std Dev 15.04
Gaus mean : 42.7682
Gaus Width: 4.1898
Entry
ampl
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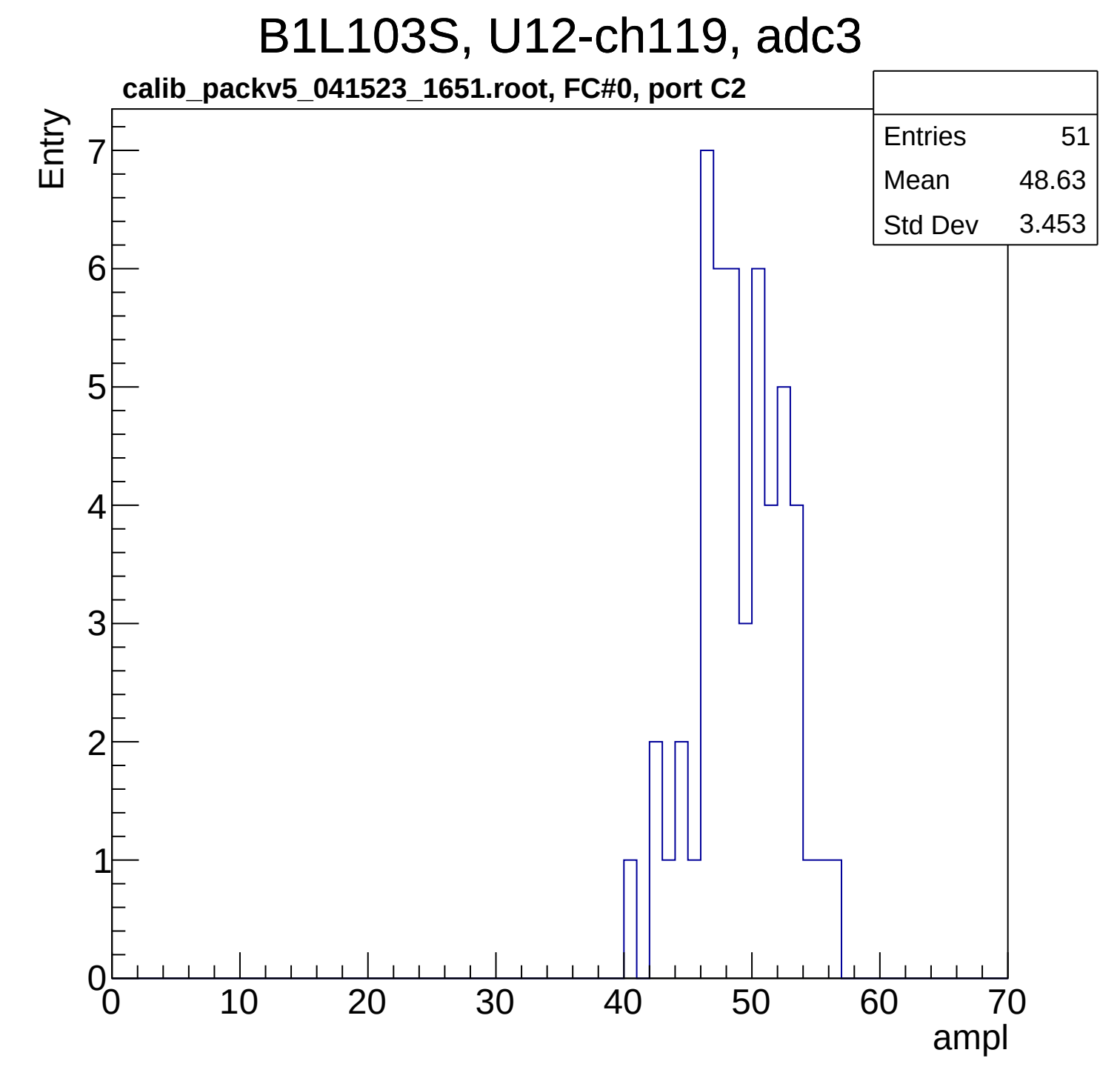
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U12-ch119, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 51
Mean 48.63
Std Dev 3.453
Entry
ampl
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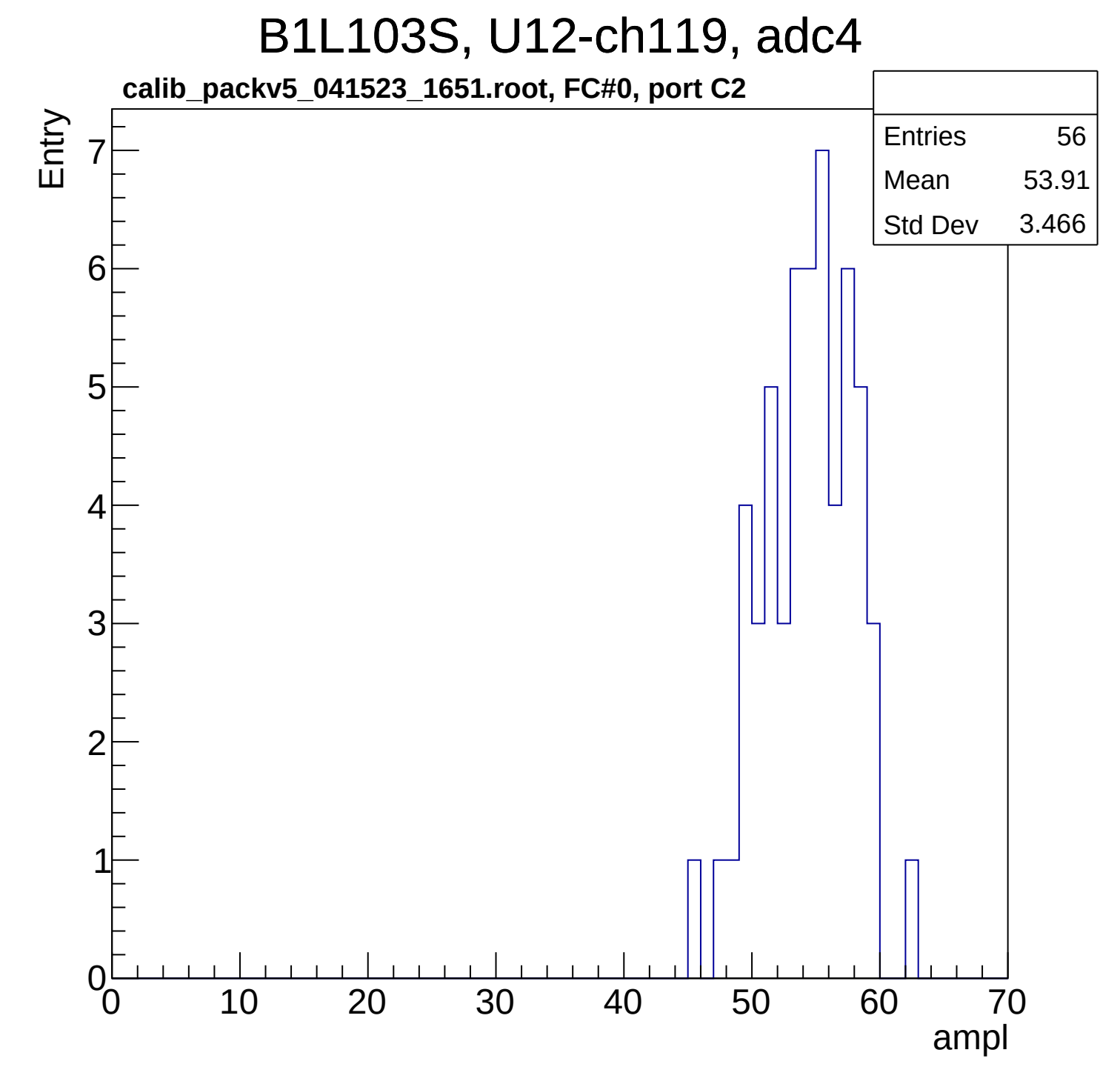
B1L103S, U12-ch119, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 53.91
Std Dev 3.466
Entry
ampl
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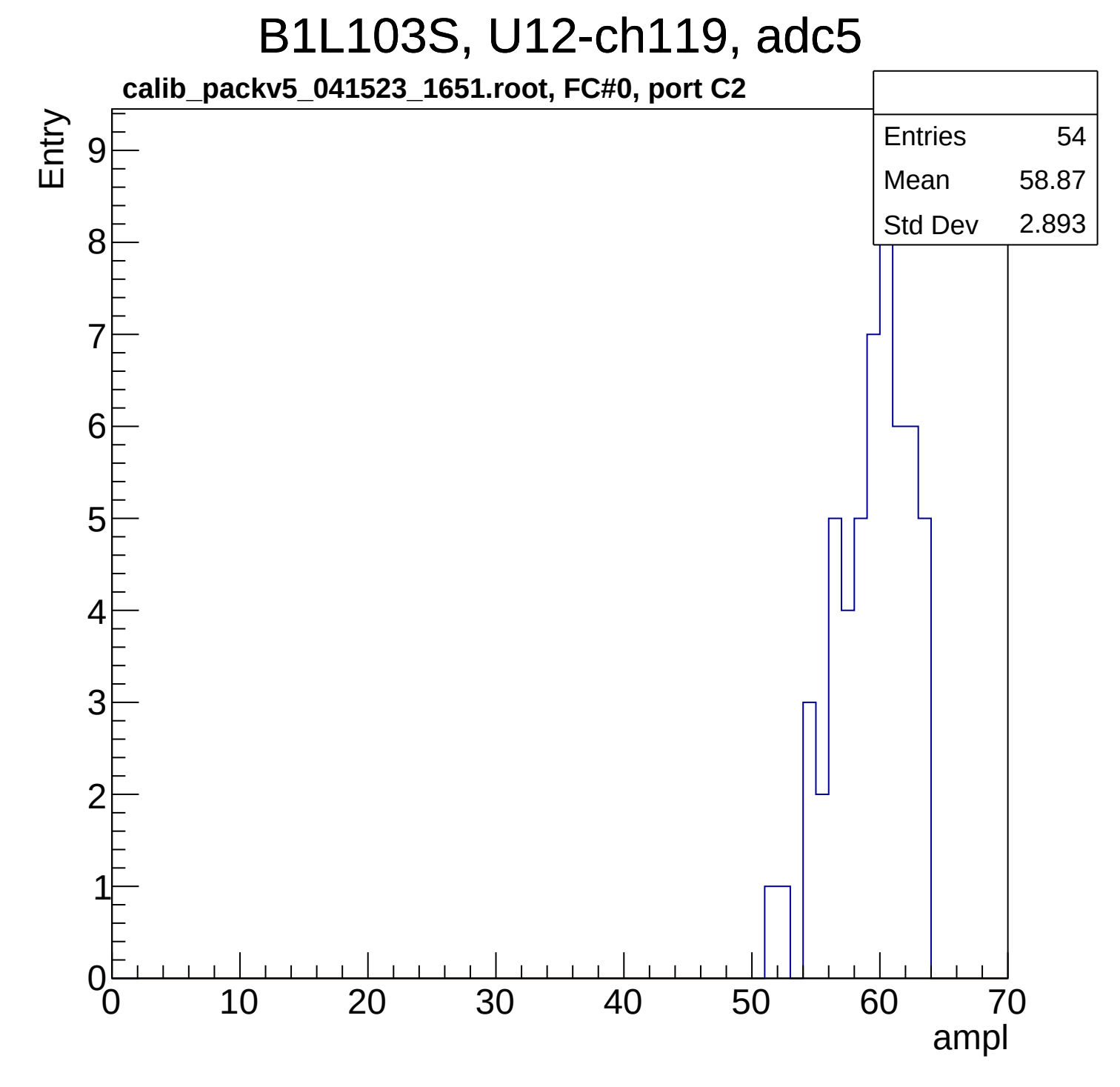
B1L103S, U12-ch119, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 58.87
Std Dev 2.893
Entry
ampl
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0
10
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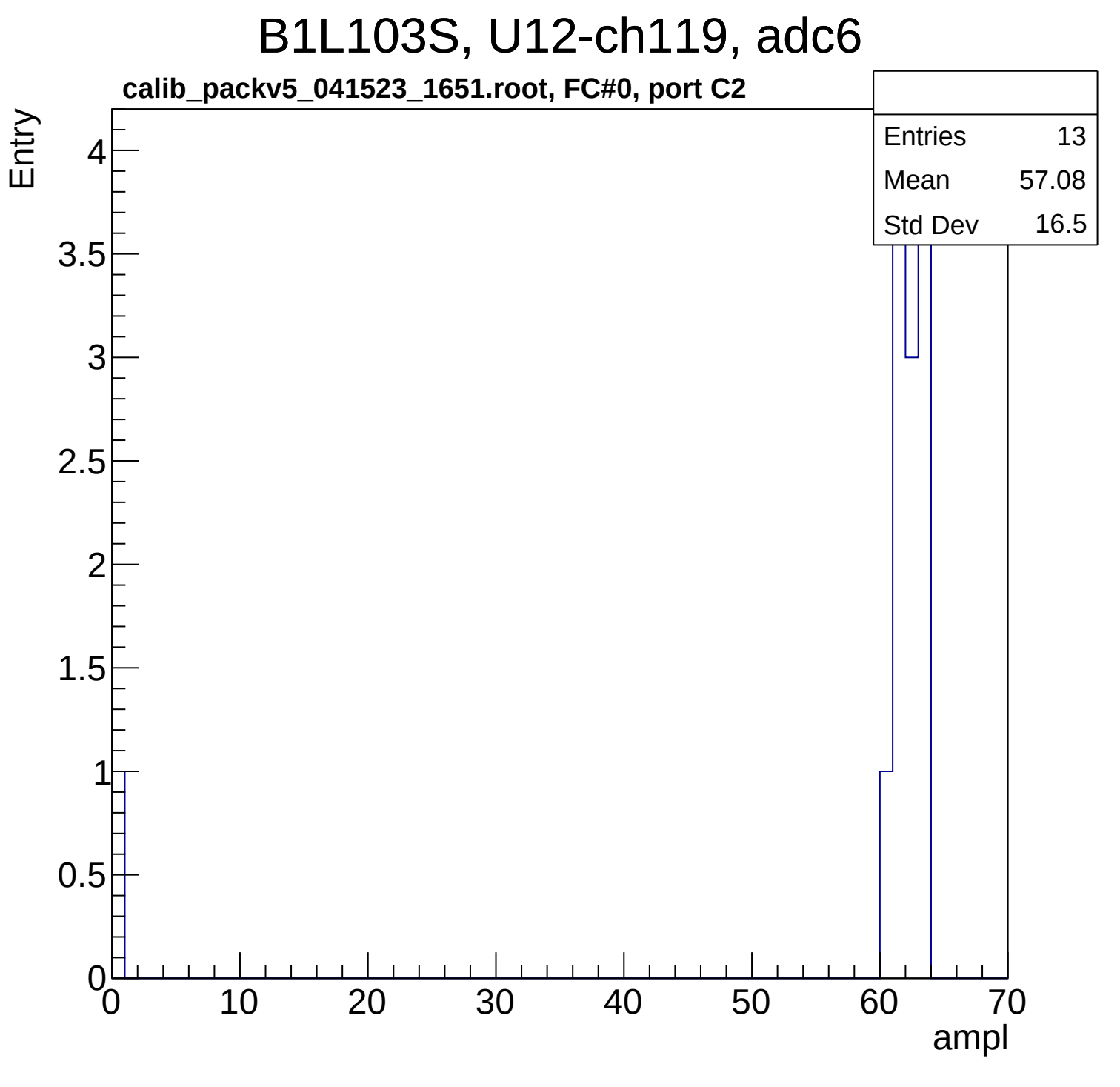
B1L103S, U12-ch119, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 13
Mean 57.08
Std Dev 16.5
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
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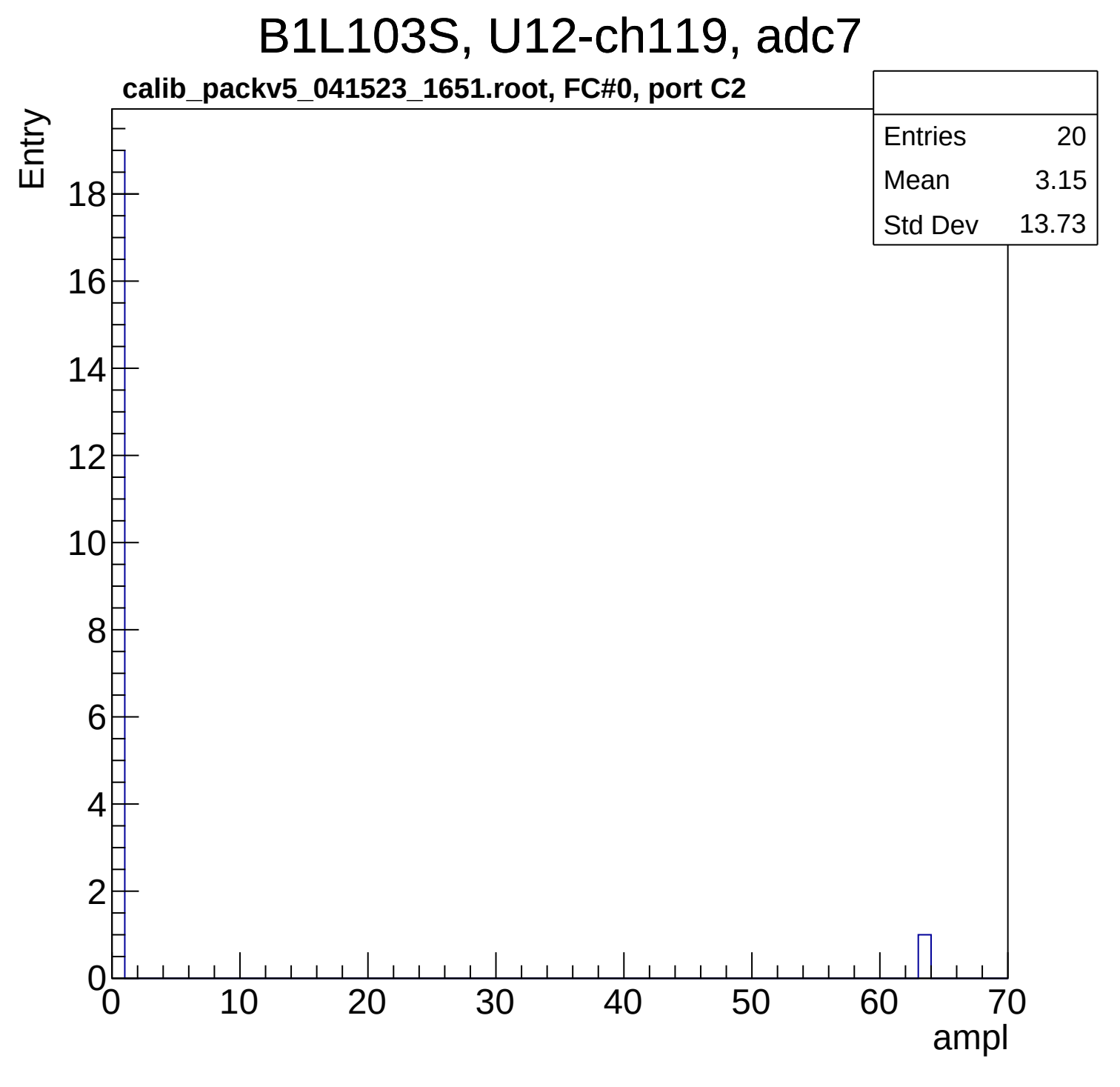
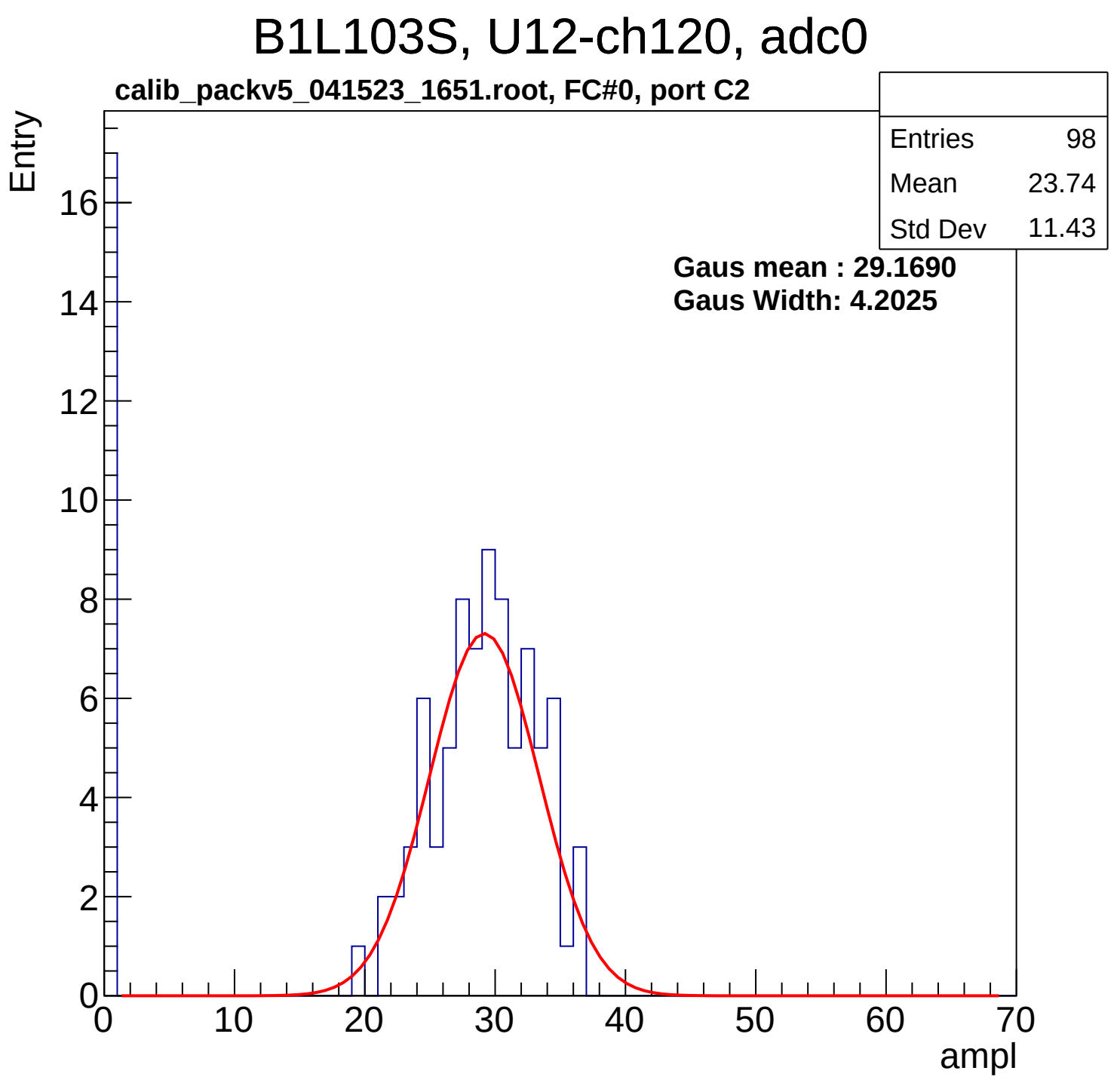
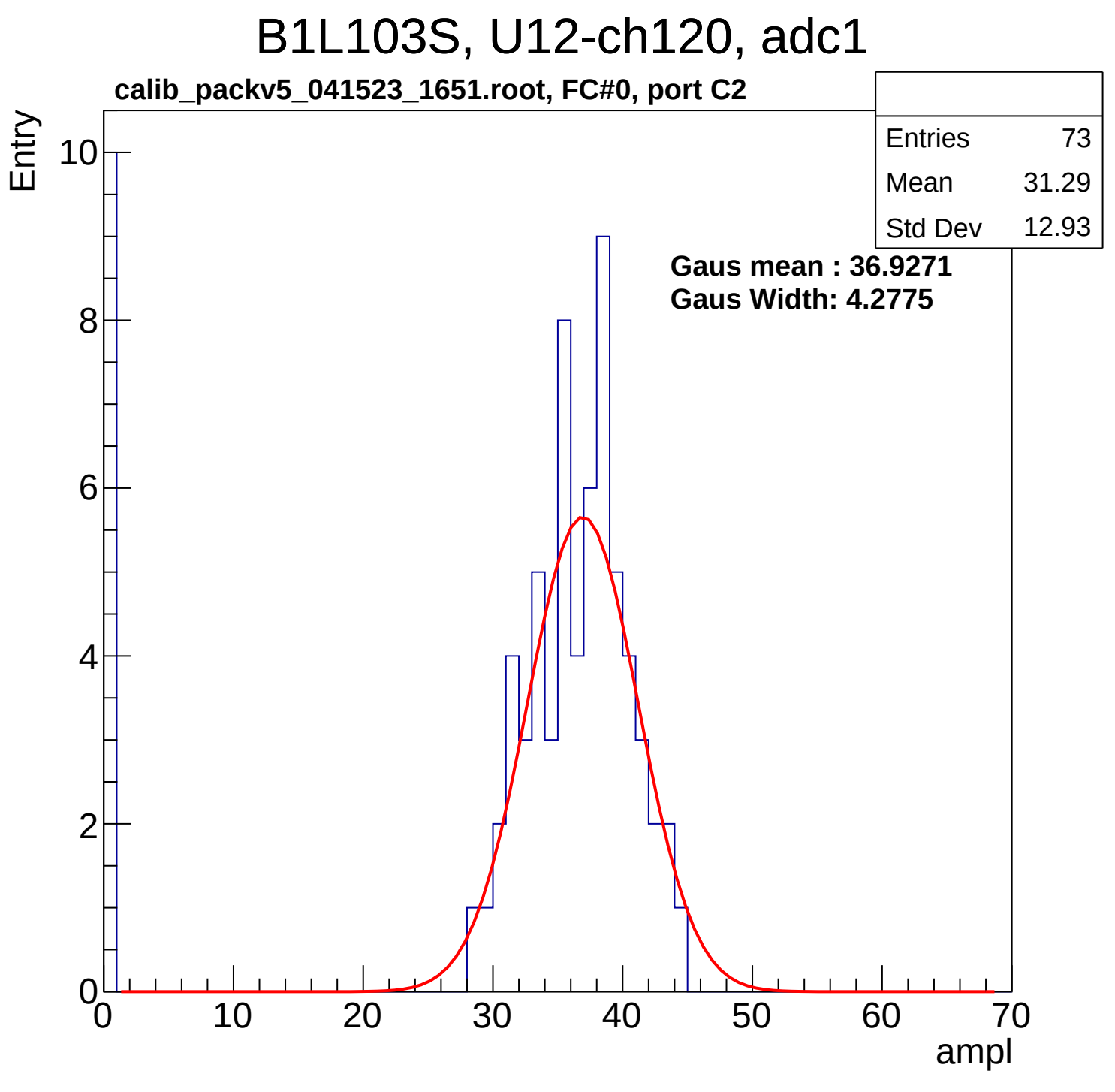
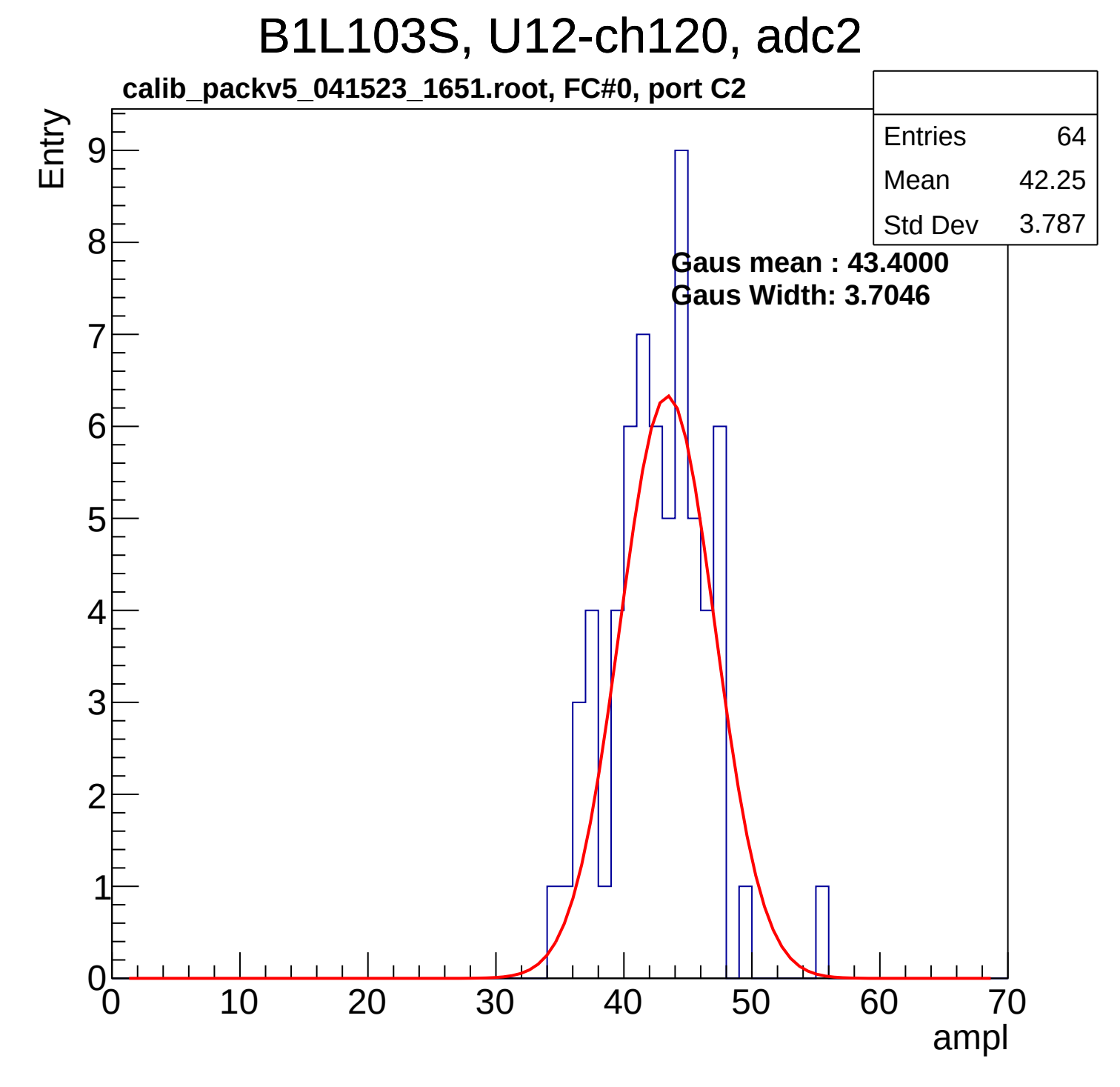
20
30
40
50
60
70


B1L103S, U12-ch119, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.15
Std Dev 13.73
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch120, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 98
Mean 23.74
Std Dev 11.43
Gaus mean : 29.1690
Gaus Width: 4.2025
Entry
ampl
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70


B1L103S, U12-ch120, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 31.29
Std Dev 12.93
Gaus mean : 36.9271
Gaus Width: 4.2775
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch120, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 64
Mean 42.25
Std Dev 3.787
Gaus mean : 43.4000
Gaus Width: 3.7046
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
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60
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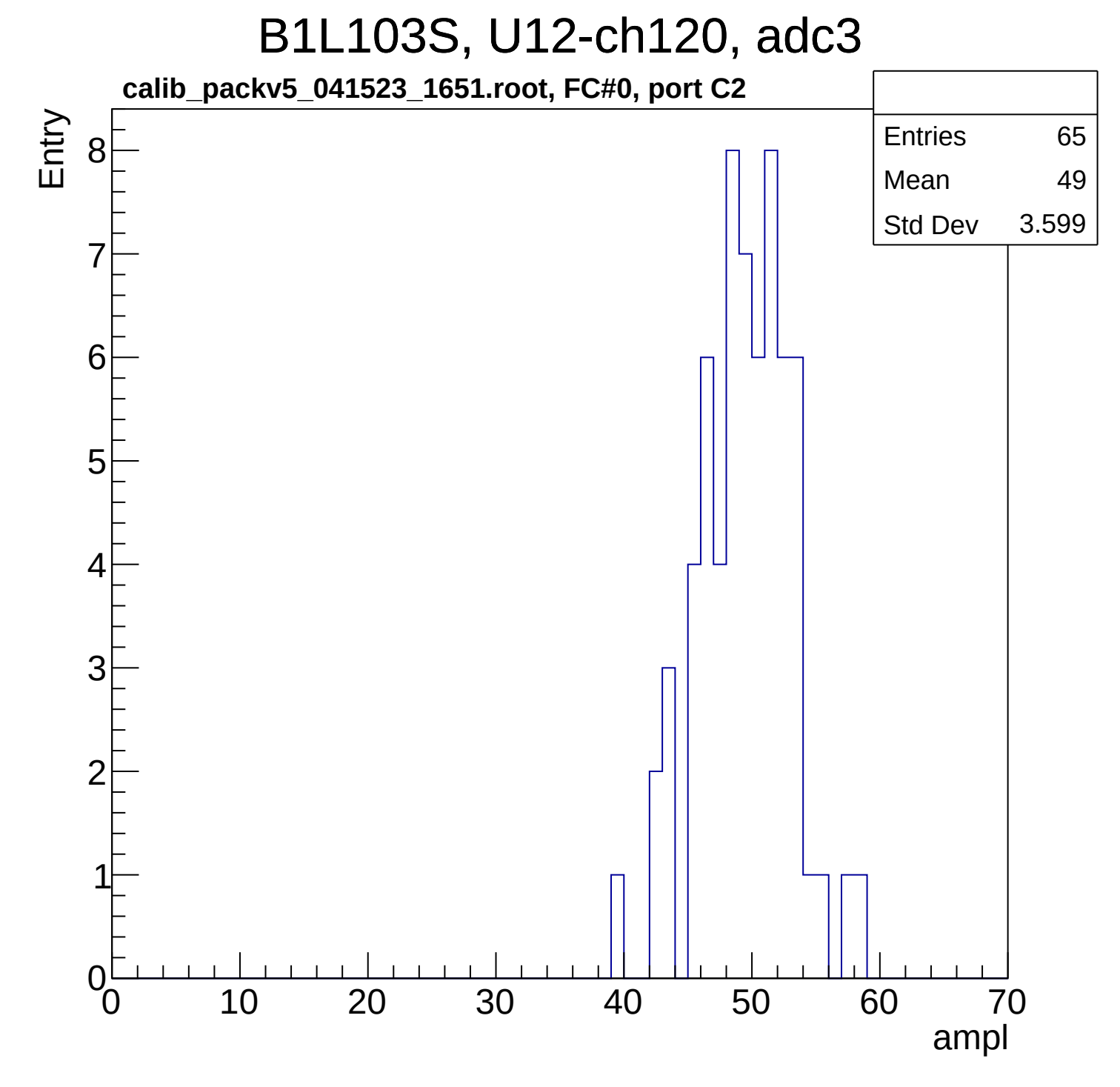
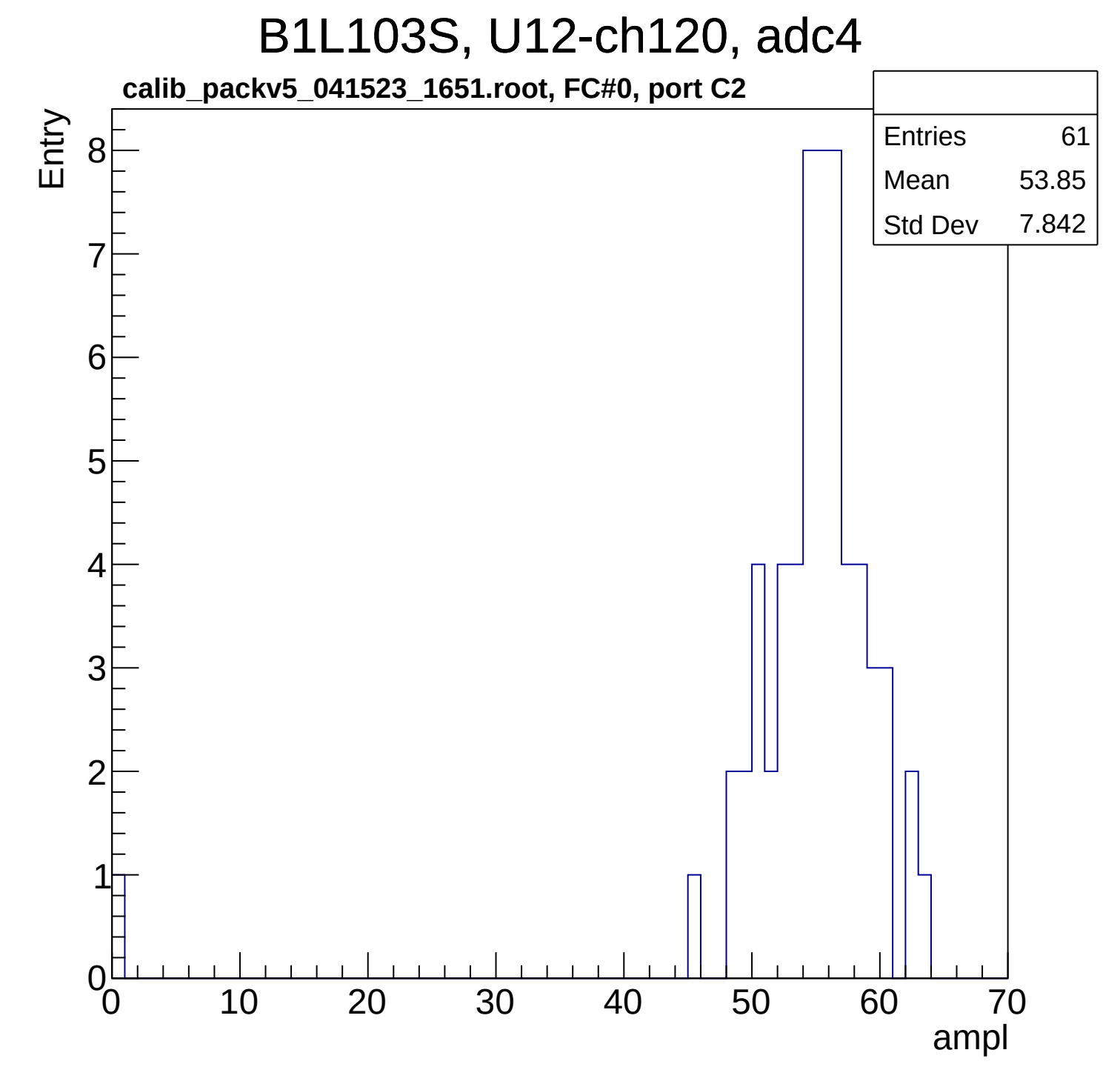
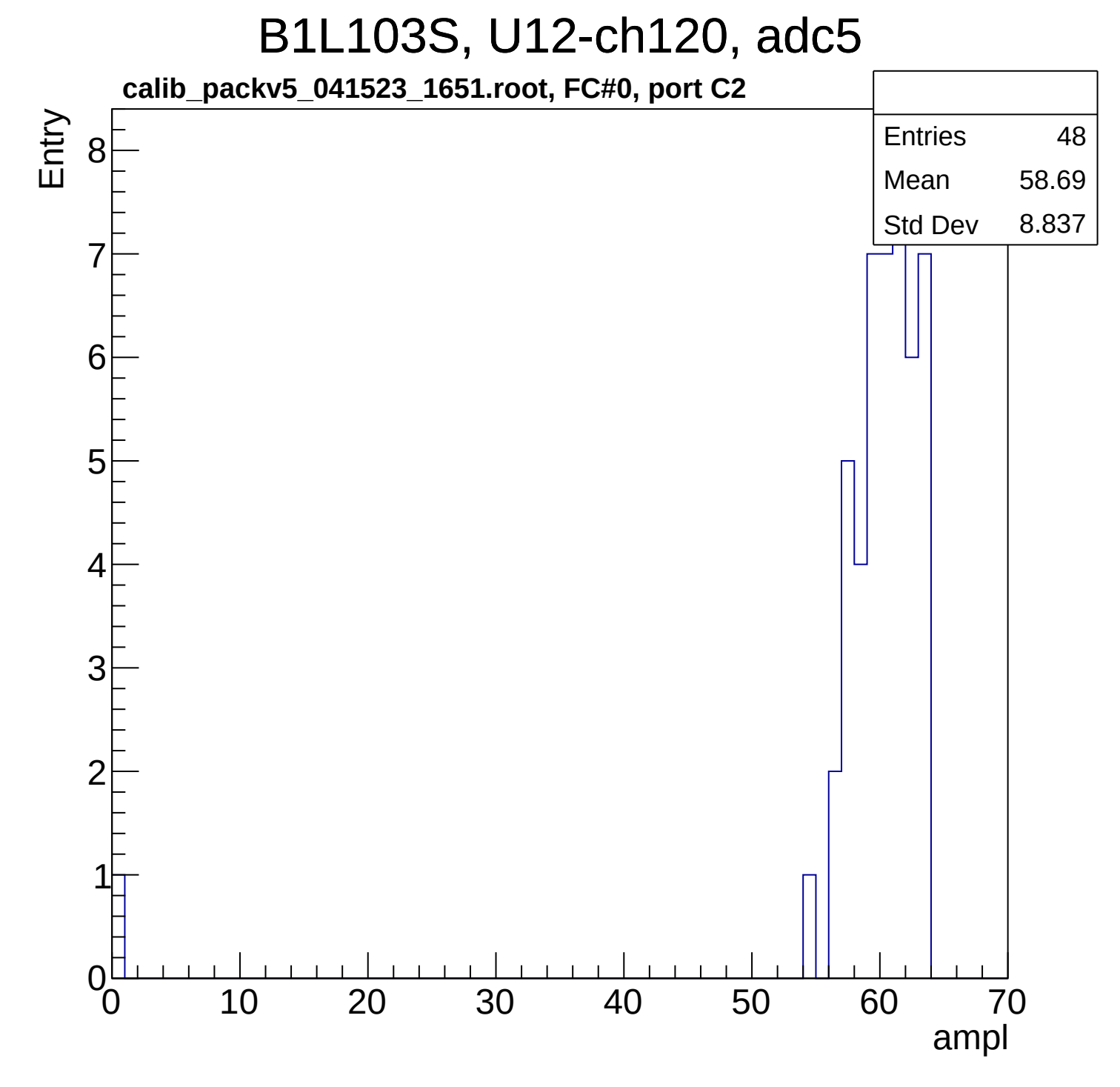

B1L103S, U12-ch120, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 49
Std Dev 3.599
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U12-ch120, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 53.85
Std Dev 7.842
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U12-ch120, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 48
Mean 58.69
Std Dev 8.837
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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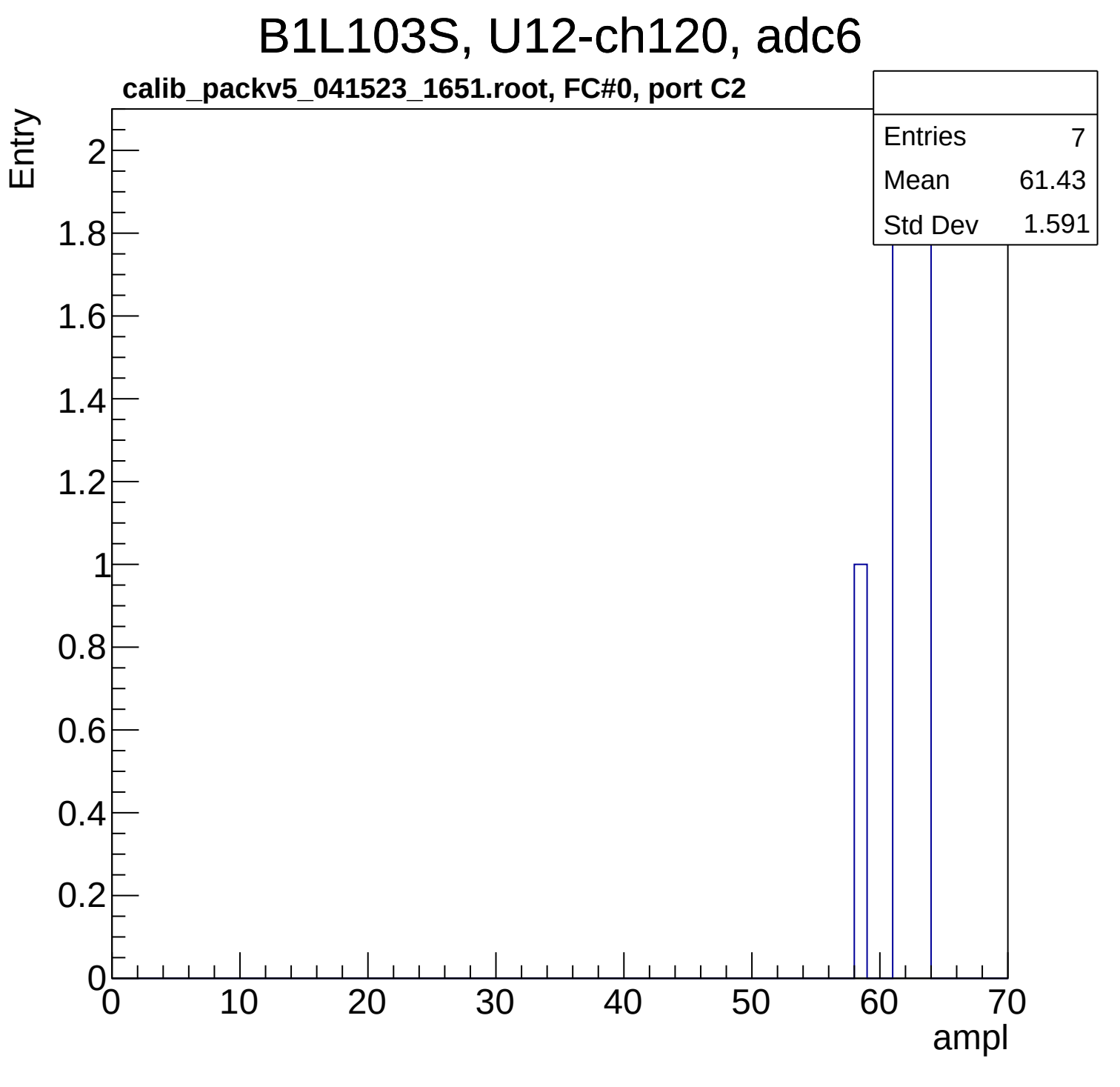
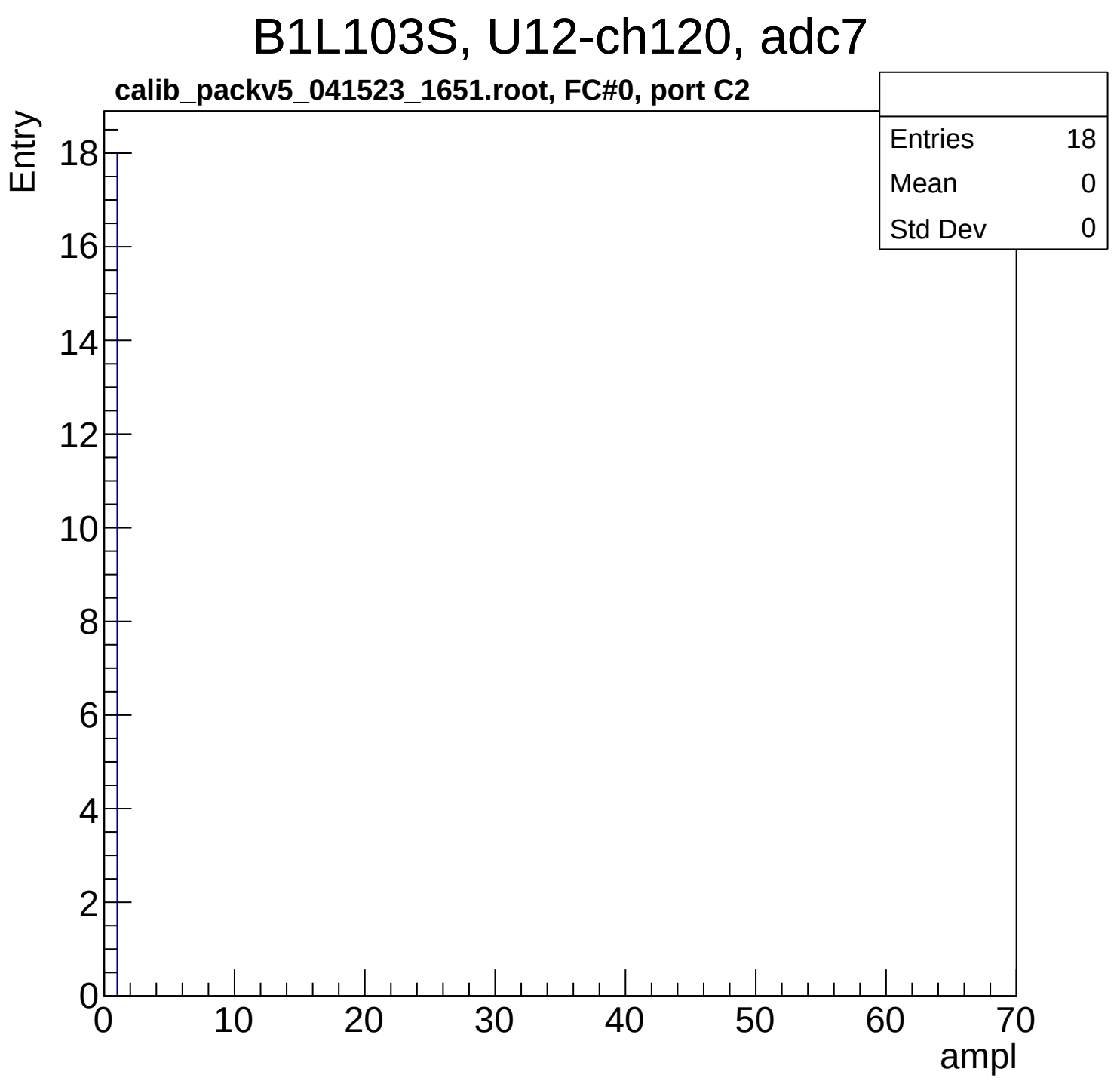
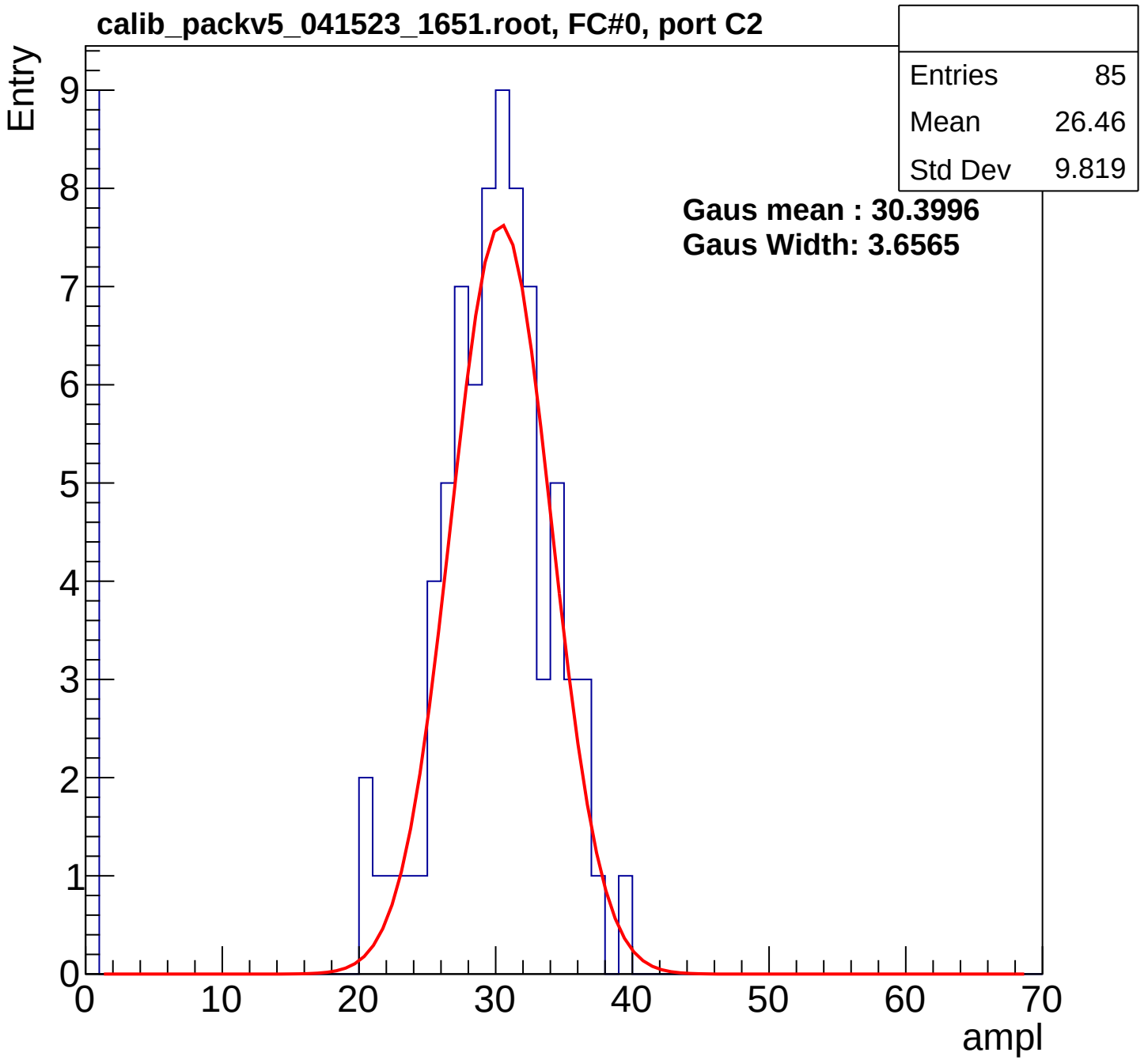

B1L103S, U12-ch120, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 7
Mean 61.43
Std Dev 1.591
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U12-ch120, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 18
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch121, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 85
Mean 26.46
Std Dev 9.819
Gaus mean : 30.3996
Gaus Width: 3.6565
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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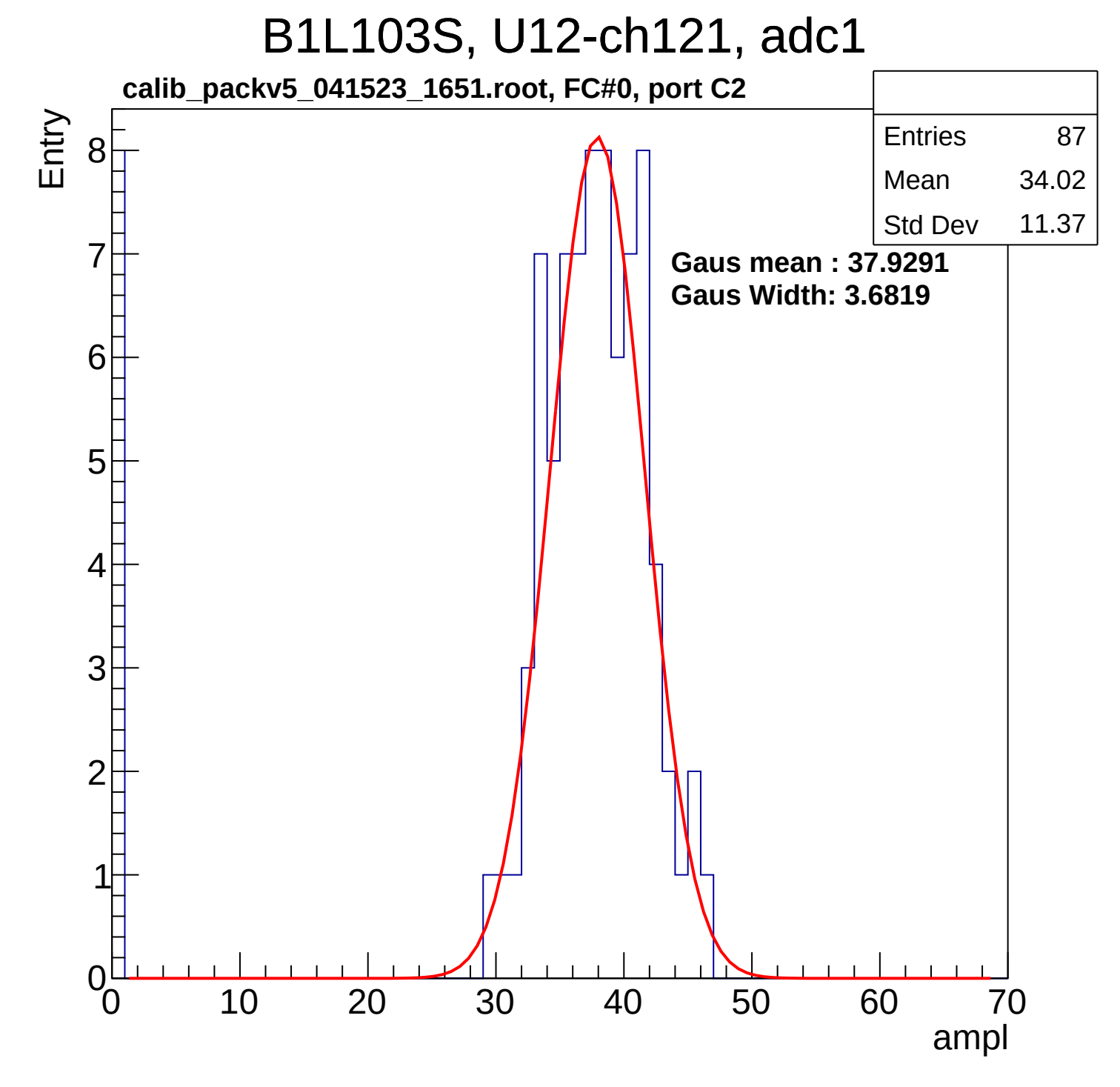
B1L103S, U12-ch121, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 34.02
Std Dev 11.37
Gaus mean : 37.9291
Gaus Width: 3.6819
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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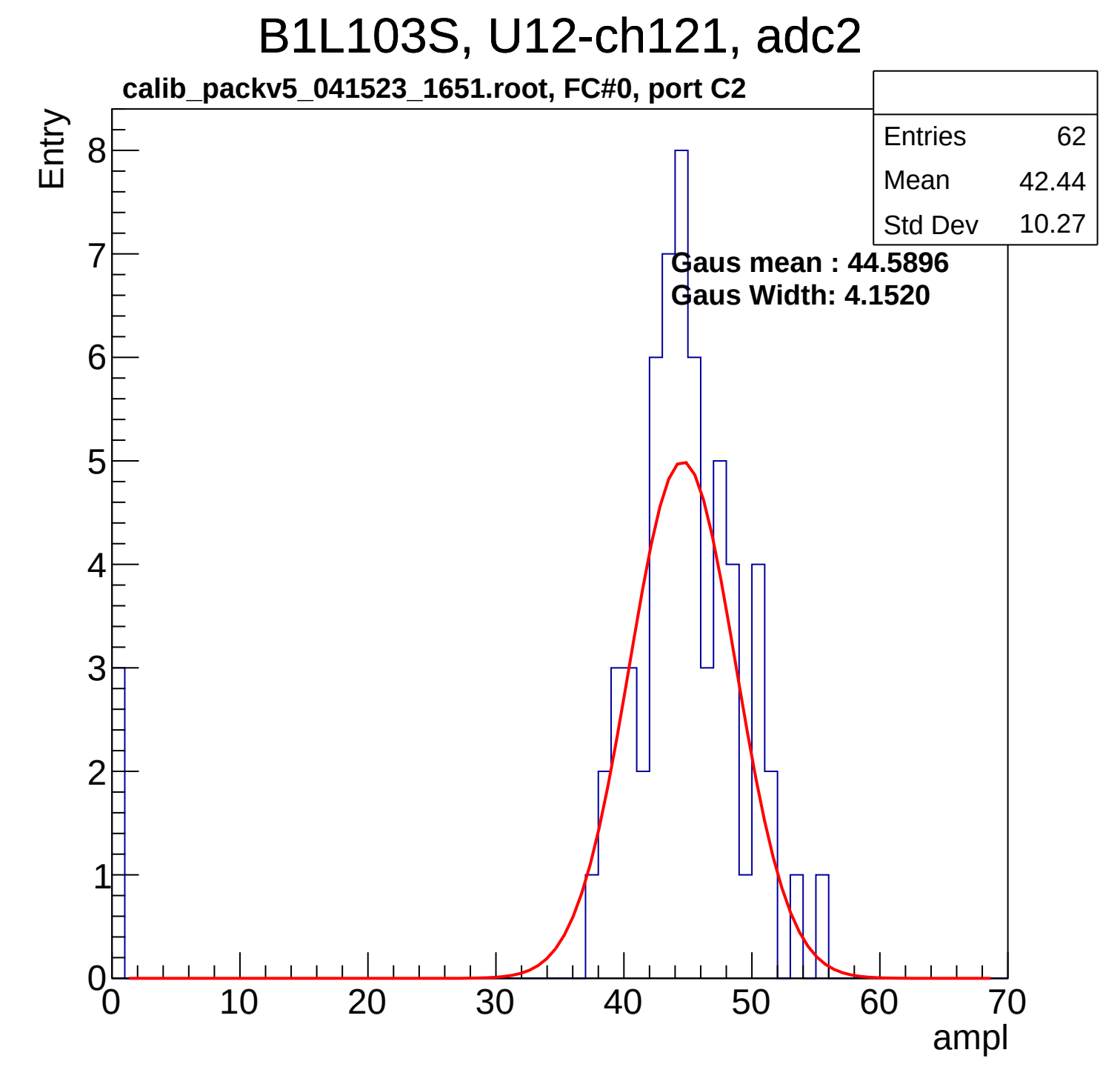
B1L103S, U12-ch121, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 42.44
Std Dev 10.27
Gaus mean : 44.5896
Gaus Width: 4.1520
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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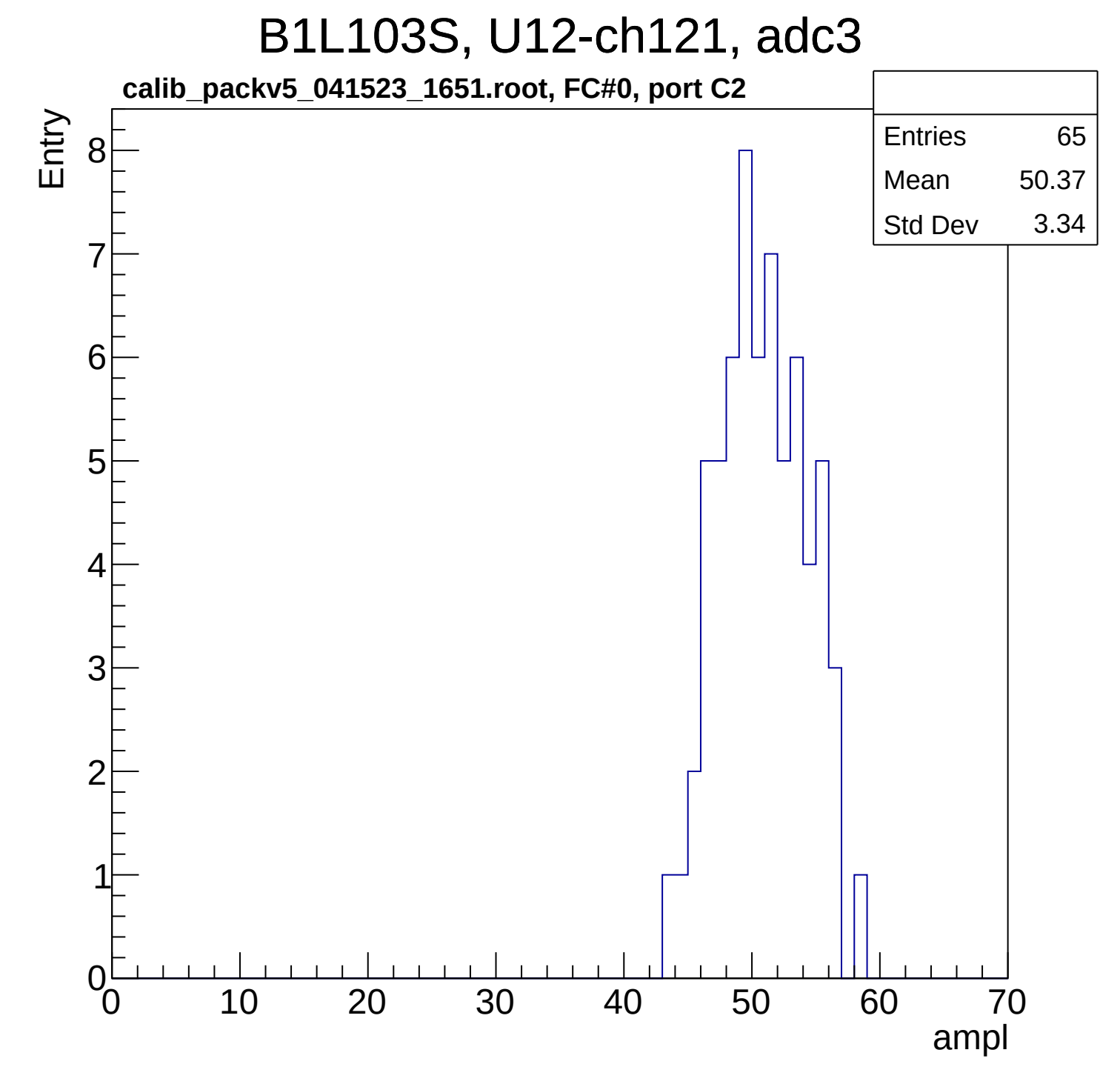
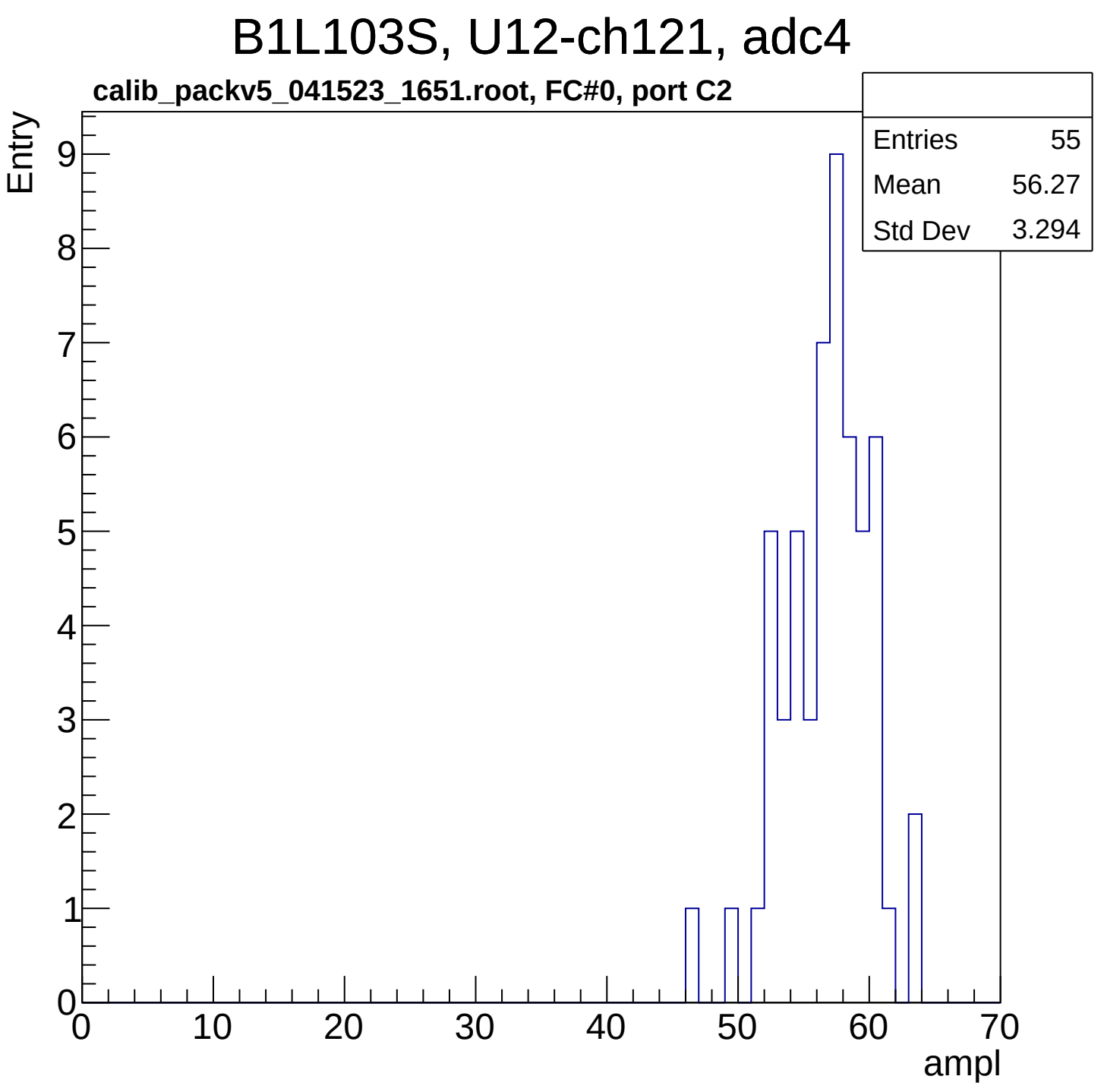

B1L103S, U12-ch121, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 65
Mean 50.37
Std Dev 3.34
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U12-ch121, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 56.27
Std Dev 3.294
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
30
40
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60
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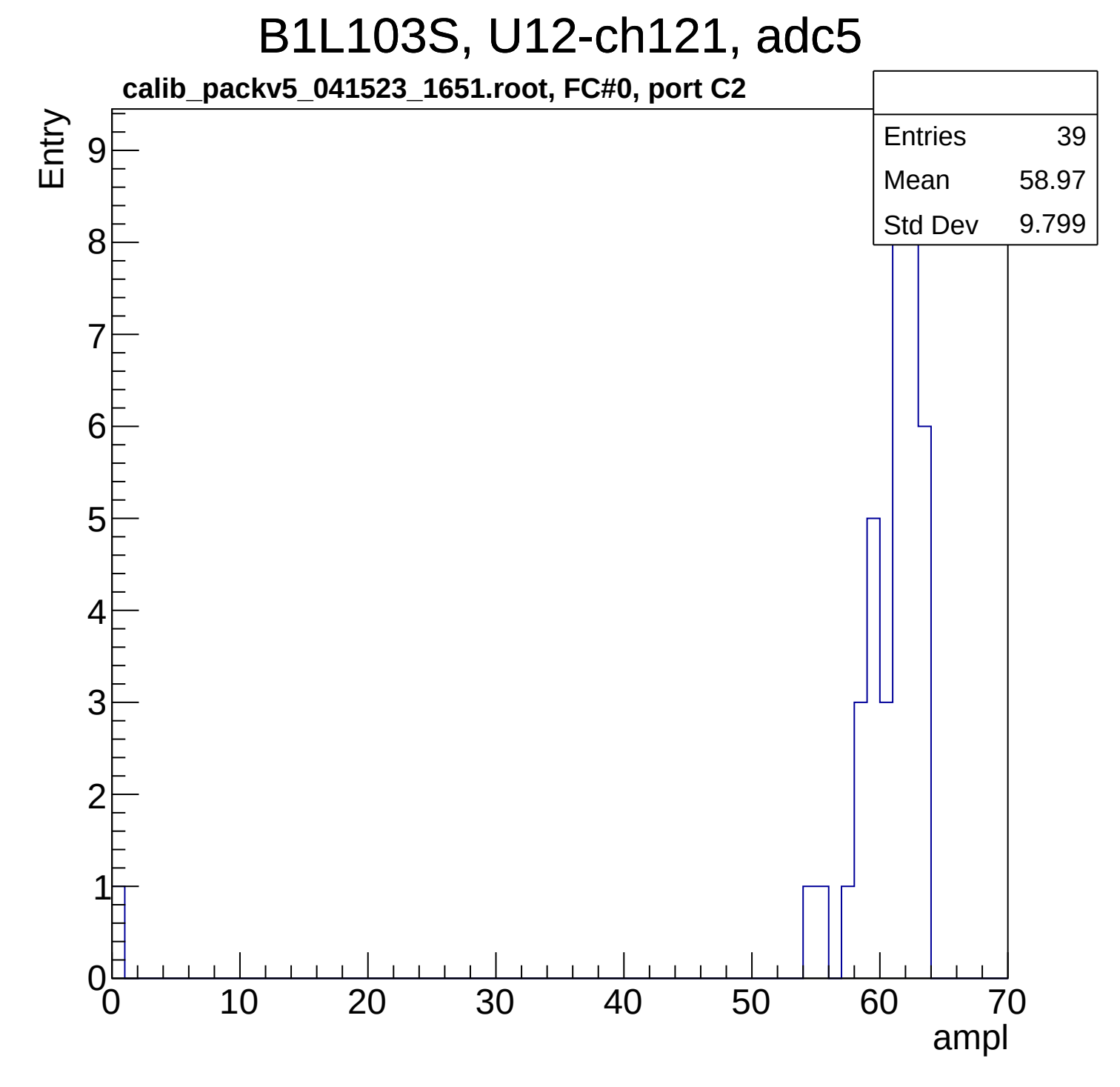
B1L103S, U12-ch121, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 39
Mean 58.97
Std Dev 9.799
Entry
ampl
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1
2
3
4
5
6
7
8
9
0
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20
30
40
50
60
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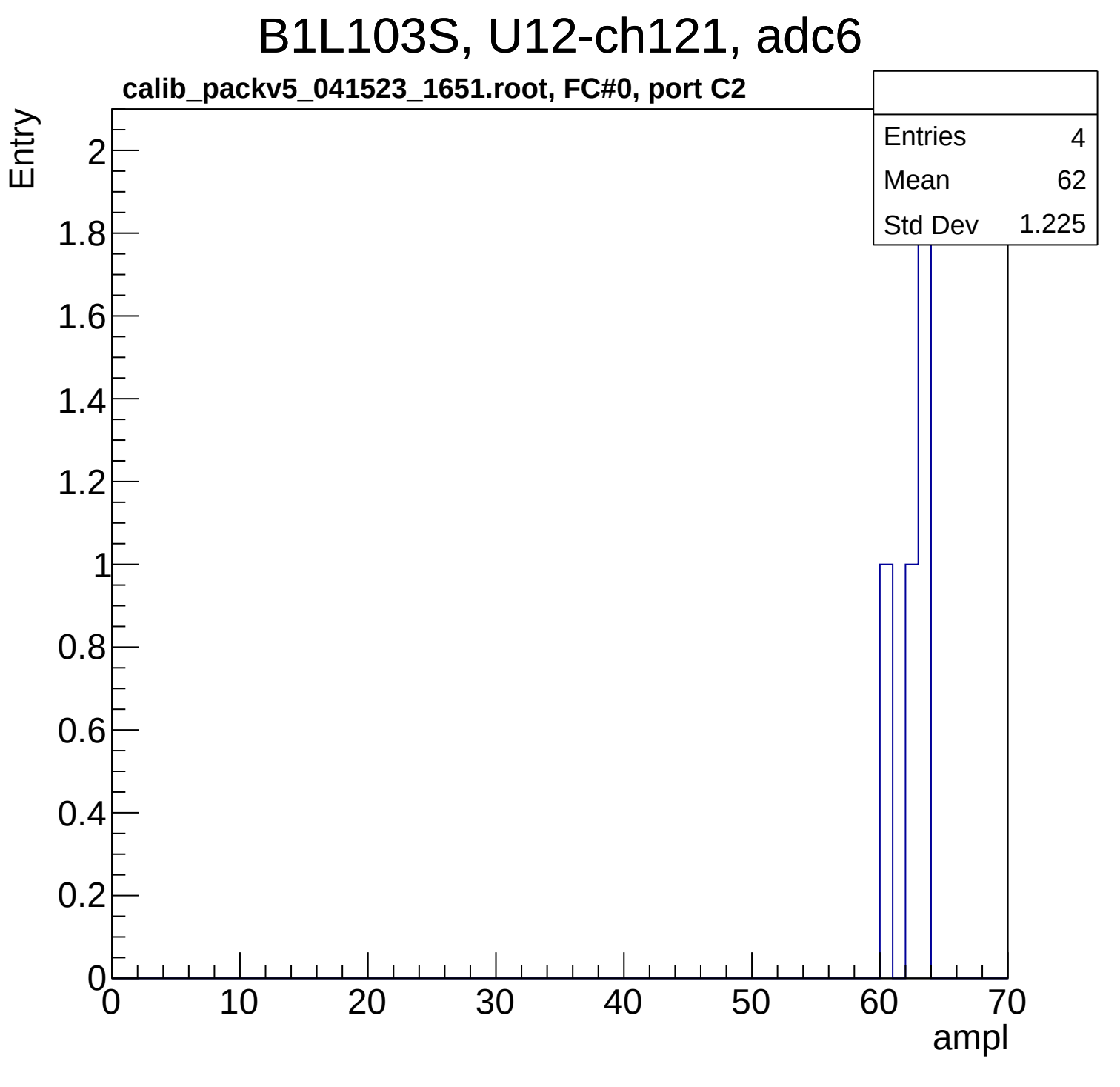
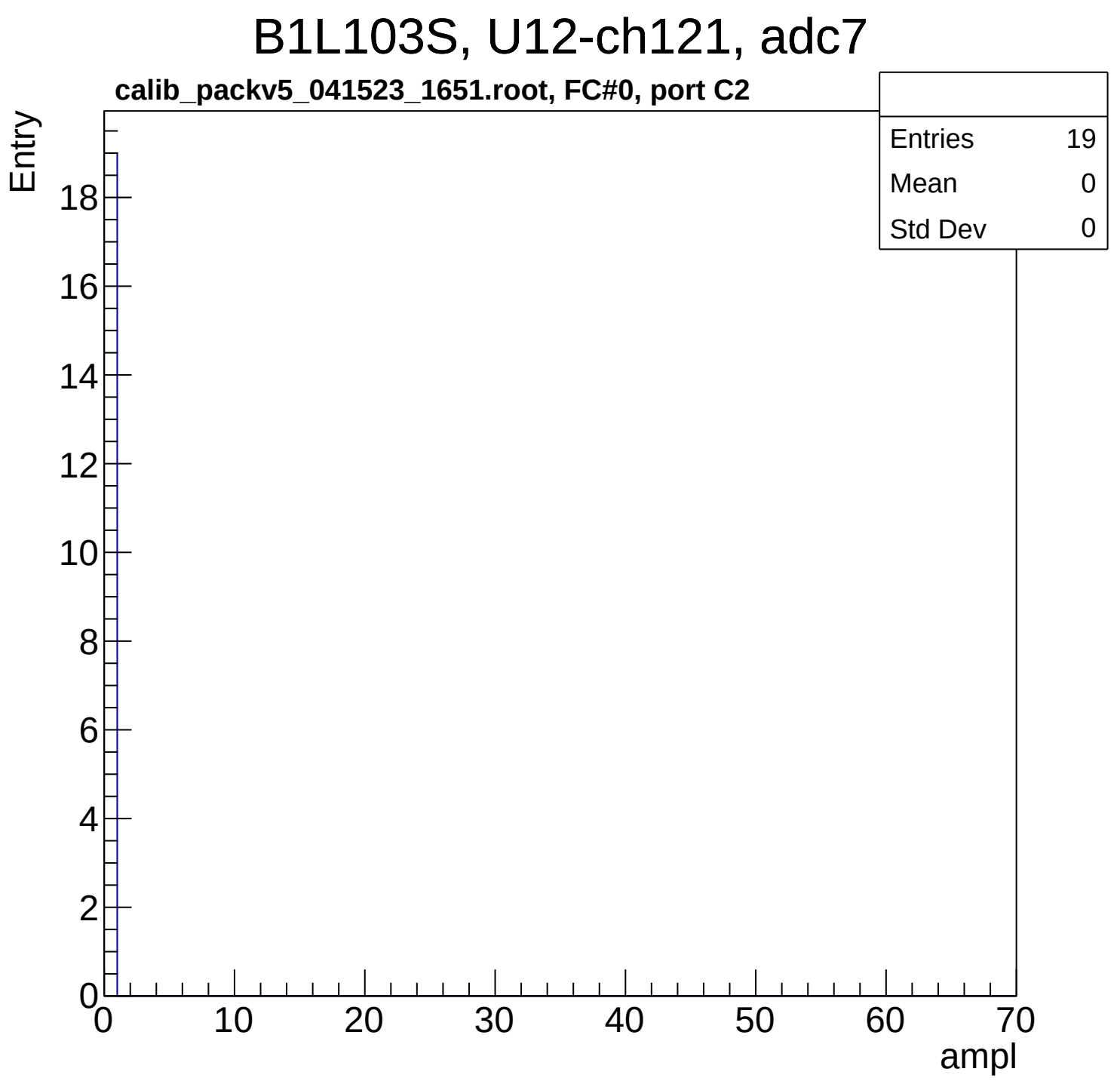
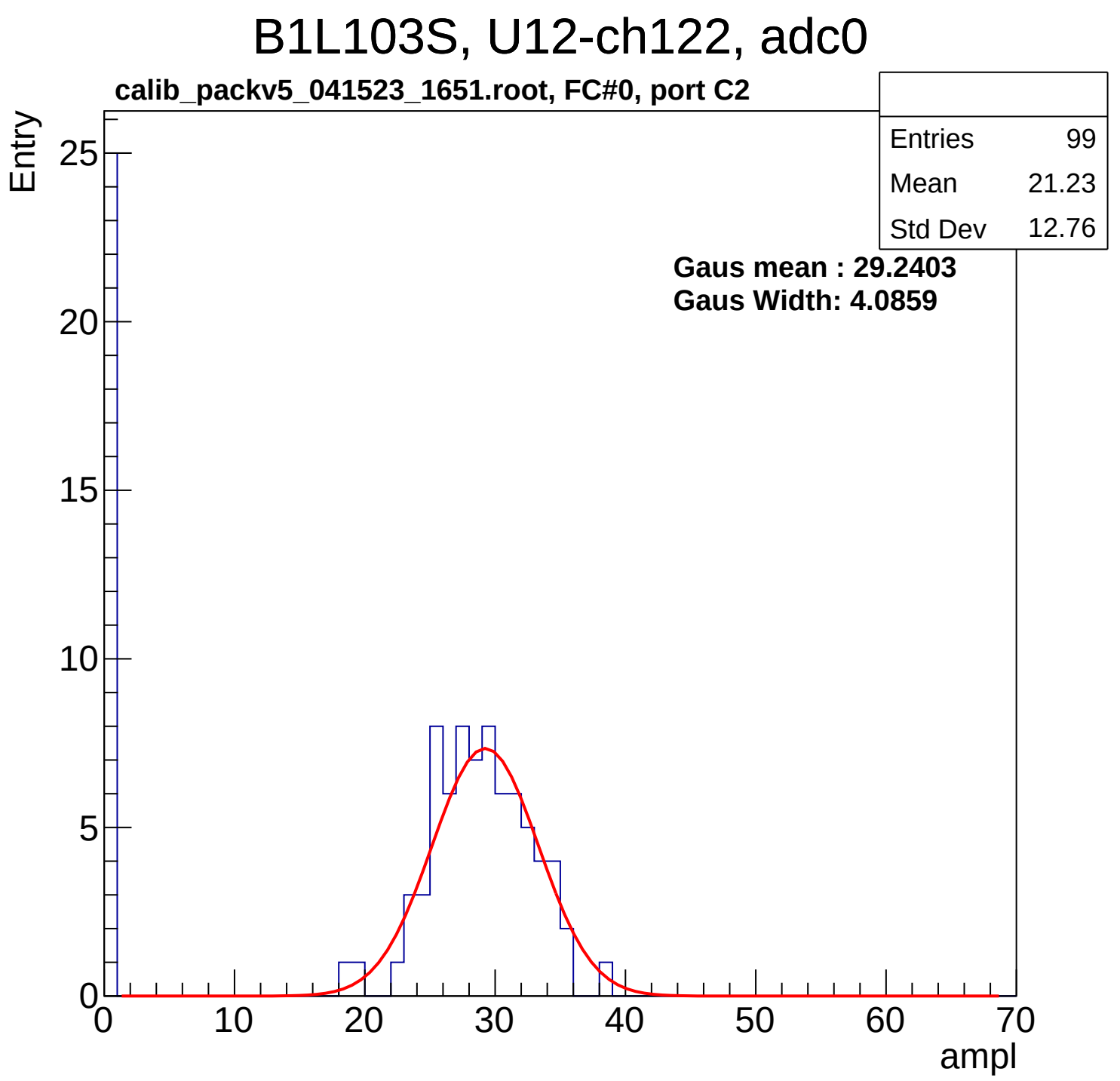

B1L103S, U12-ch121, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 4
Mean 62
Std Dev 1.225
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70


B1L103S, U12-ch121, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch122, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 99
Mean 21.23
Std Dev 12.76
Gaus mean : 29.2403
Gaus Width: 4.0859
Entry
ampl
0
5
10
15
20
25
0
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20
30
40
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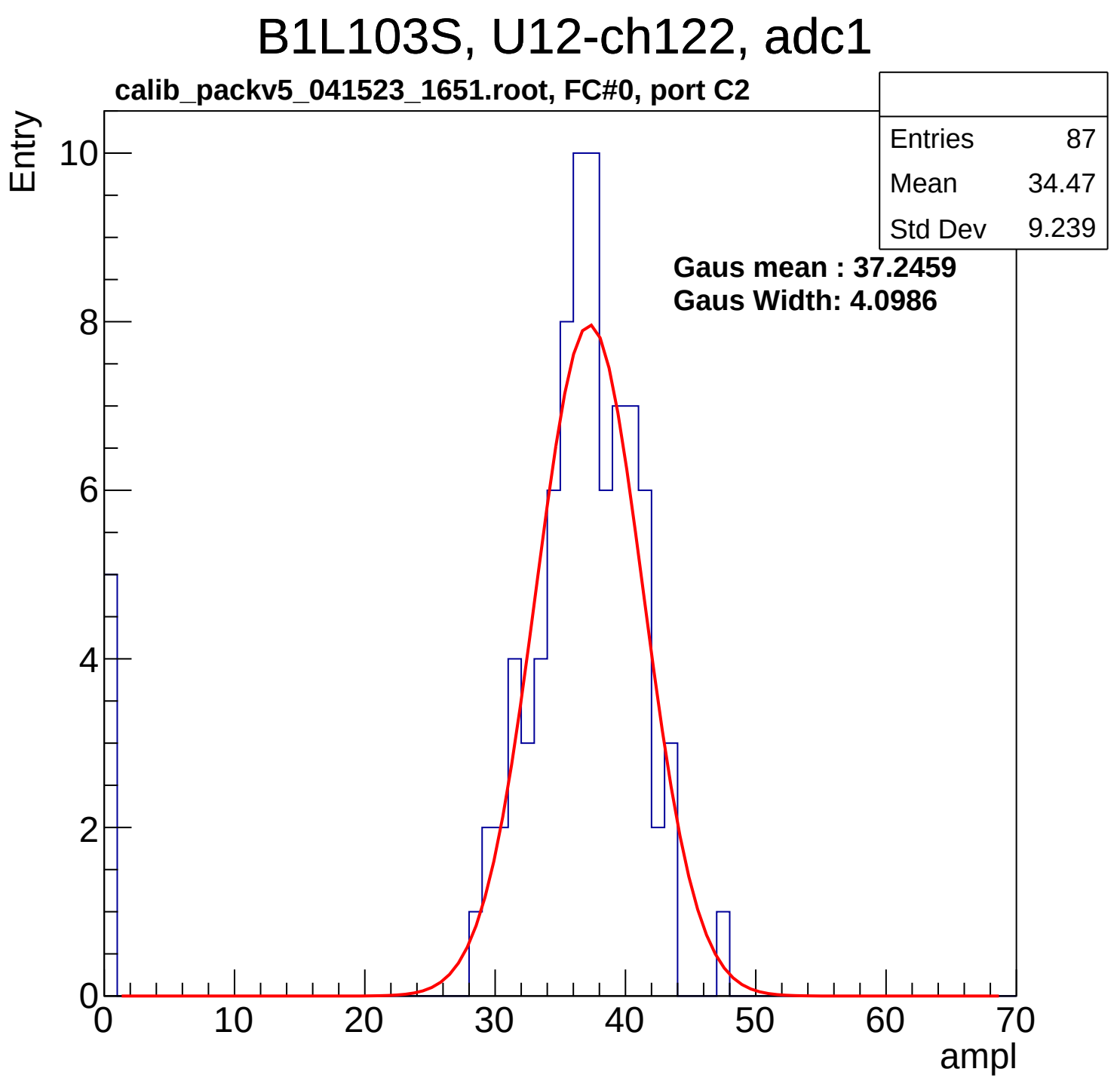
60
70


B1L103S, U12-ch122, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 87
Mean 34.47
Std Dev 9.239
Gaus mean : 37.2459
Gaus Width: 4.0986
Entry
ampl
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2
4
6
8
10
0
10
20
30
40
50
60
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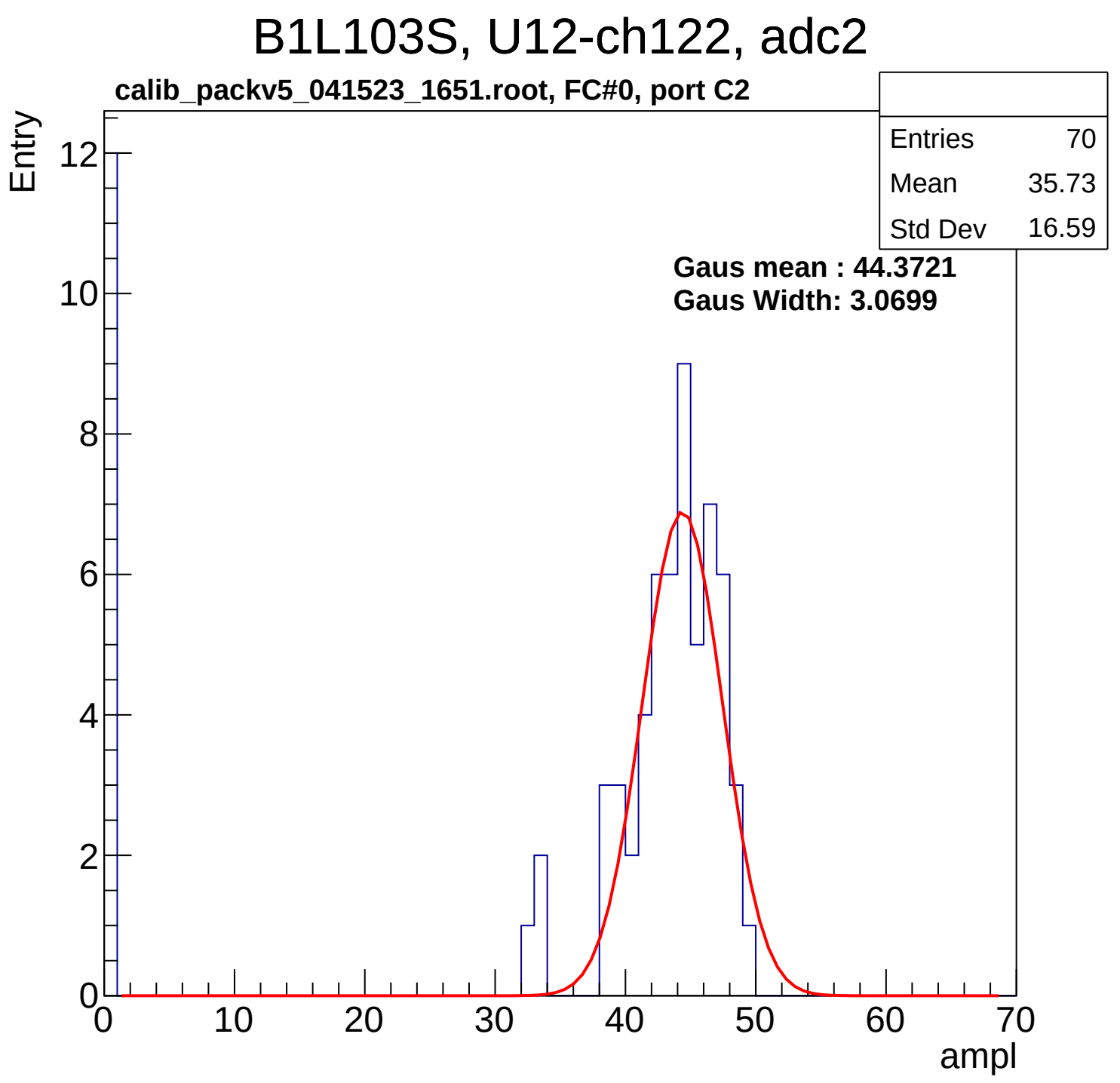
B1L103S, U12-ch122, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 70
Mean 35.73
Std Dev 16.59
Gaus mean : 44.3721
Gaus Width: 3.0699
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
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60
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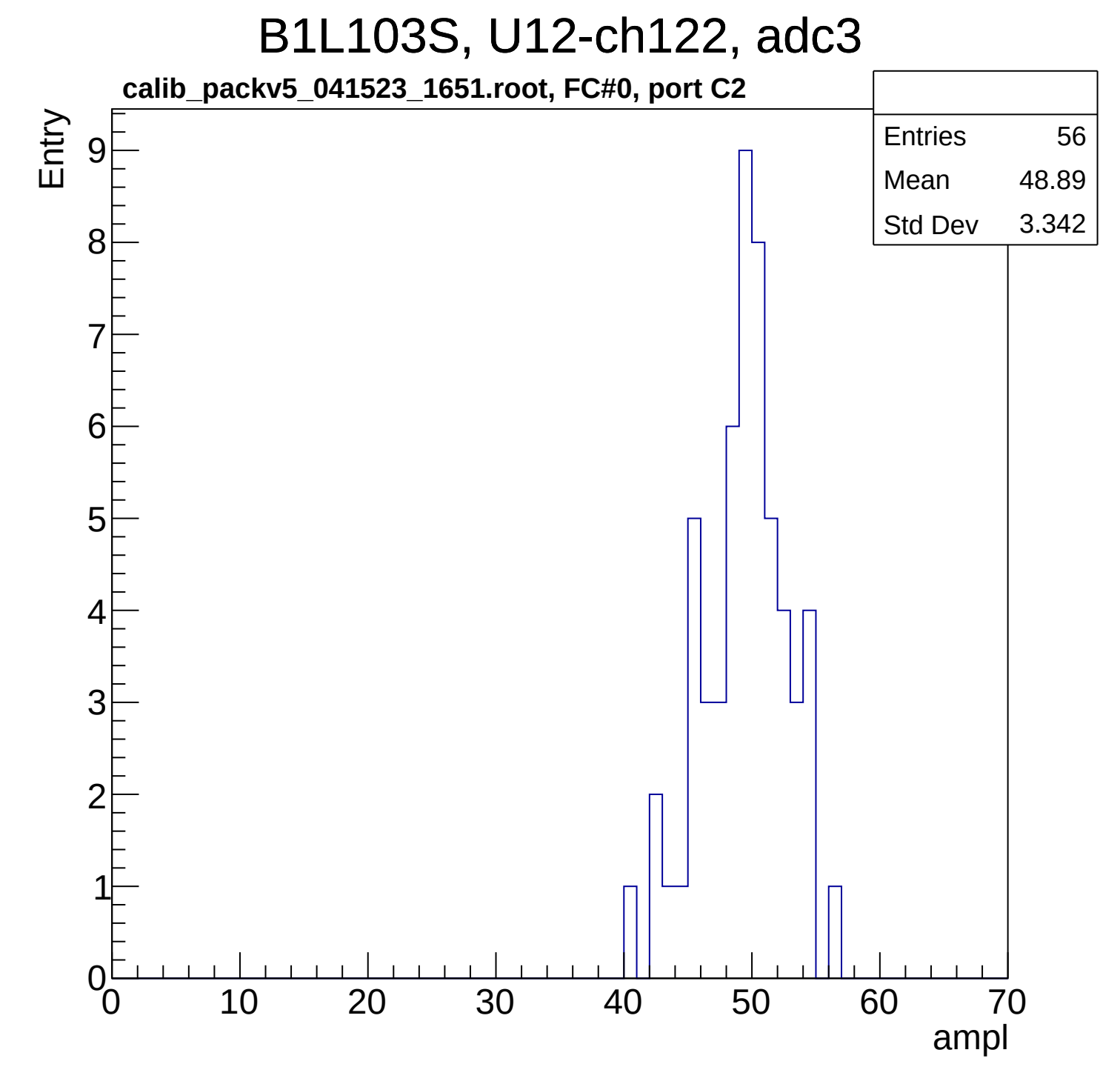
B1L103S, U12-ch122, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 56
Mean 48.89
Std Dev 3.342
Entry
ampl
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4
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6
7
8
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0
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60
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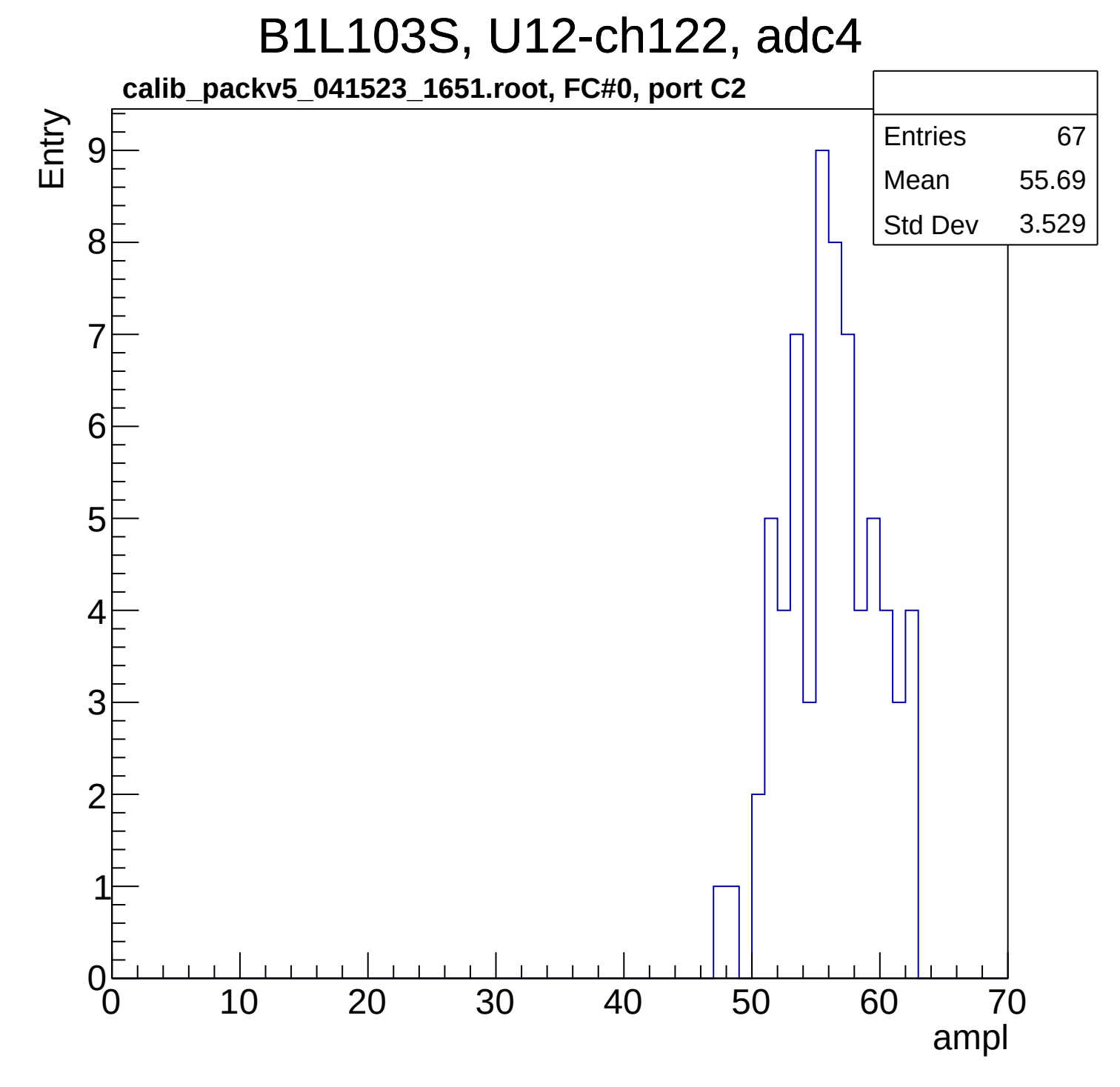
B1L103S, U12-ch122, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 55.69
Std Dev 3.529
Entry
ampl
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2
3
4
5
6
7
8
9
0
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40
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60
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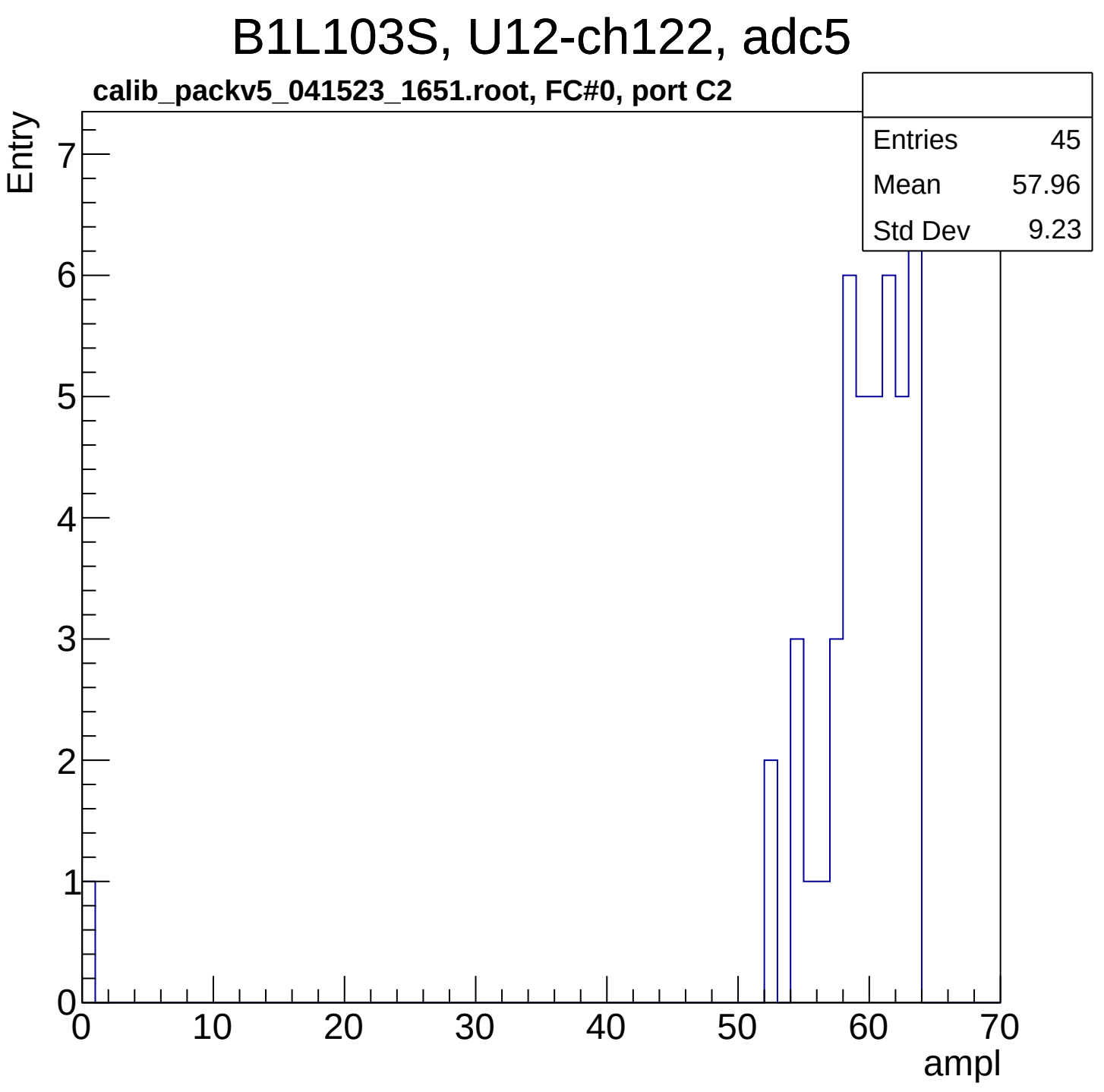
B1L103S, U12-ch122, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 45
Mean 57.96
Std Dev 9.23
Entry
ampl
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3
4
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6
7
0
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20
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60
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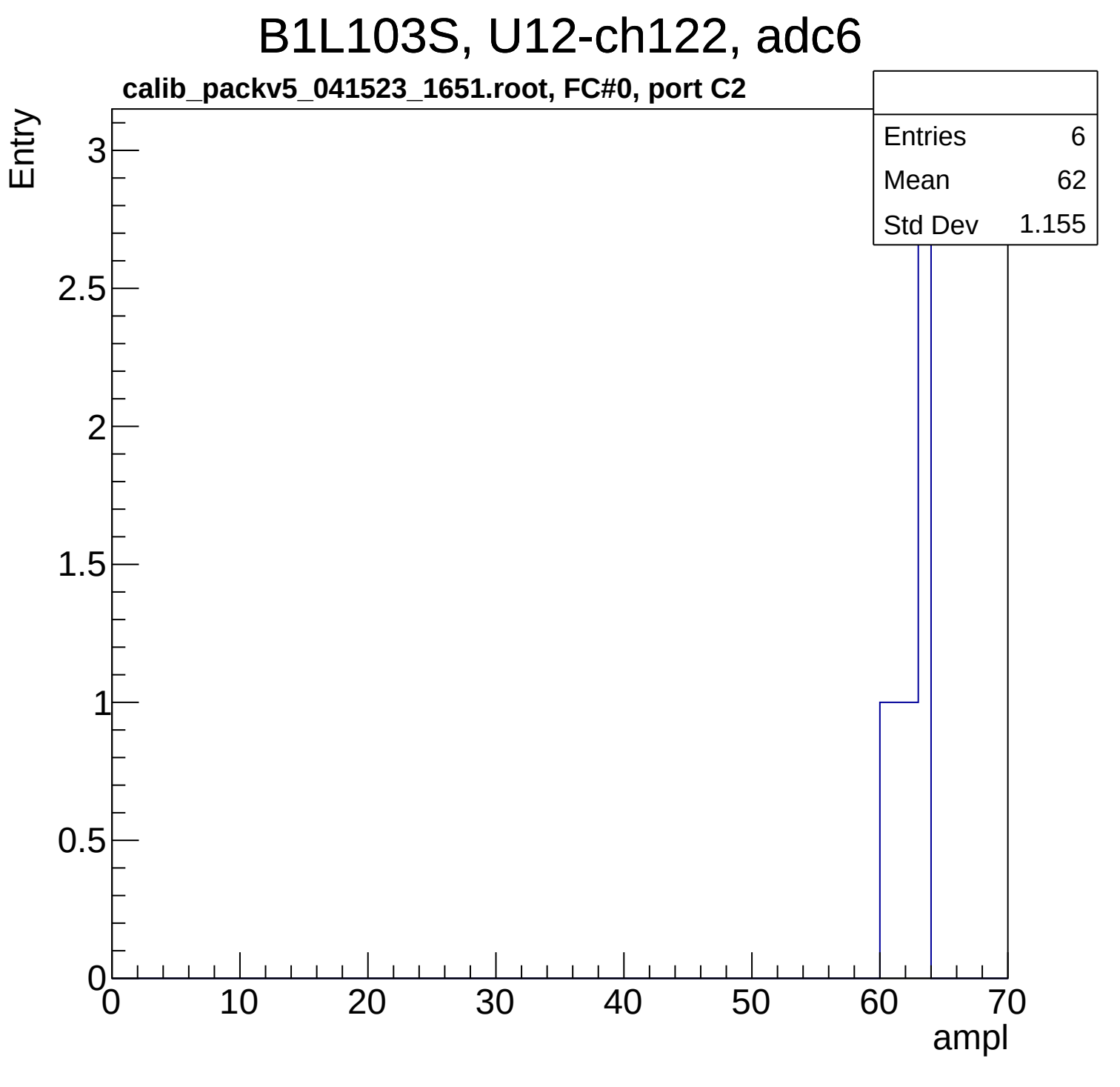
B1L103S, U12-ch122, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 62
Std Dev 1.155
Entry
ampl
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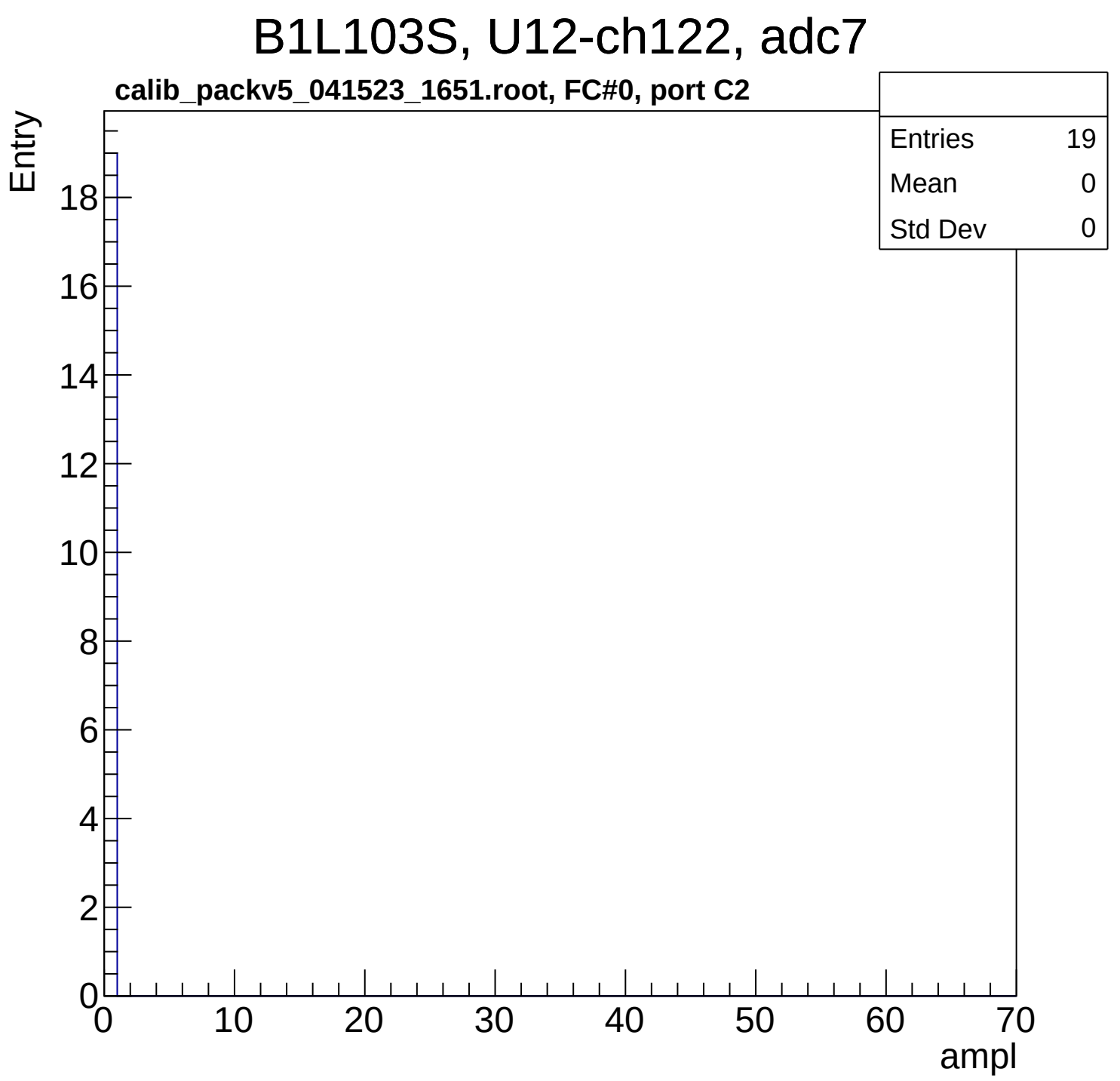
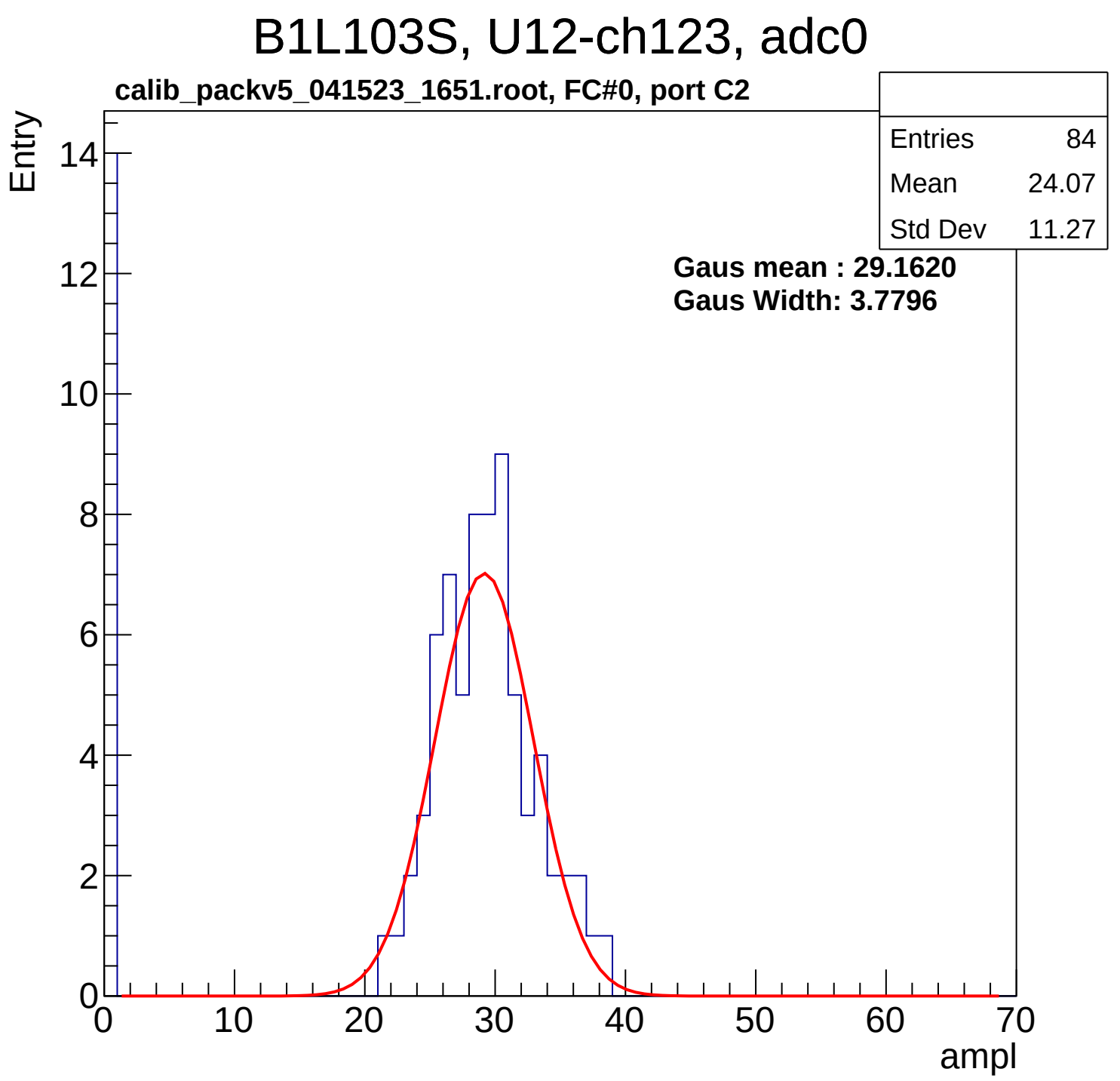
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U12-ch122, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch123, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 24.07
Std Dev 11.27
Gaus mean : 29.1620
Gaus Width: 3.7796
Entry
ampl
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2
4
6
8
10
12
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0
10
20
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40
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60
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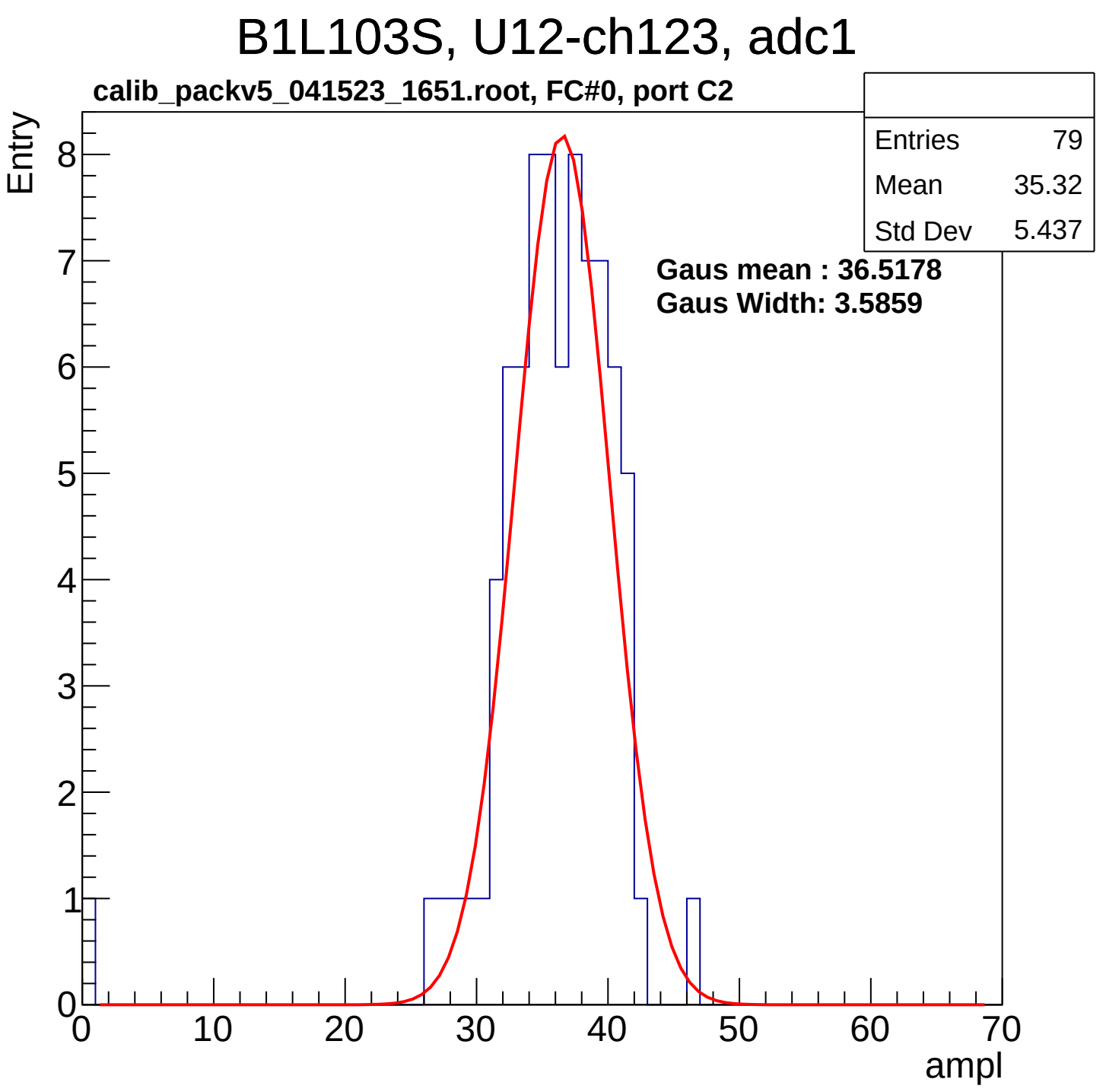
B1L103S, U12-ch123, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 35.32
Std Dev 5.437
Gaus mean : 36.5178
Gaus Width: 3.5859
Entry
ampl
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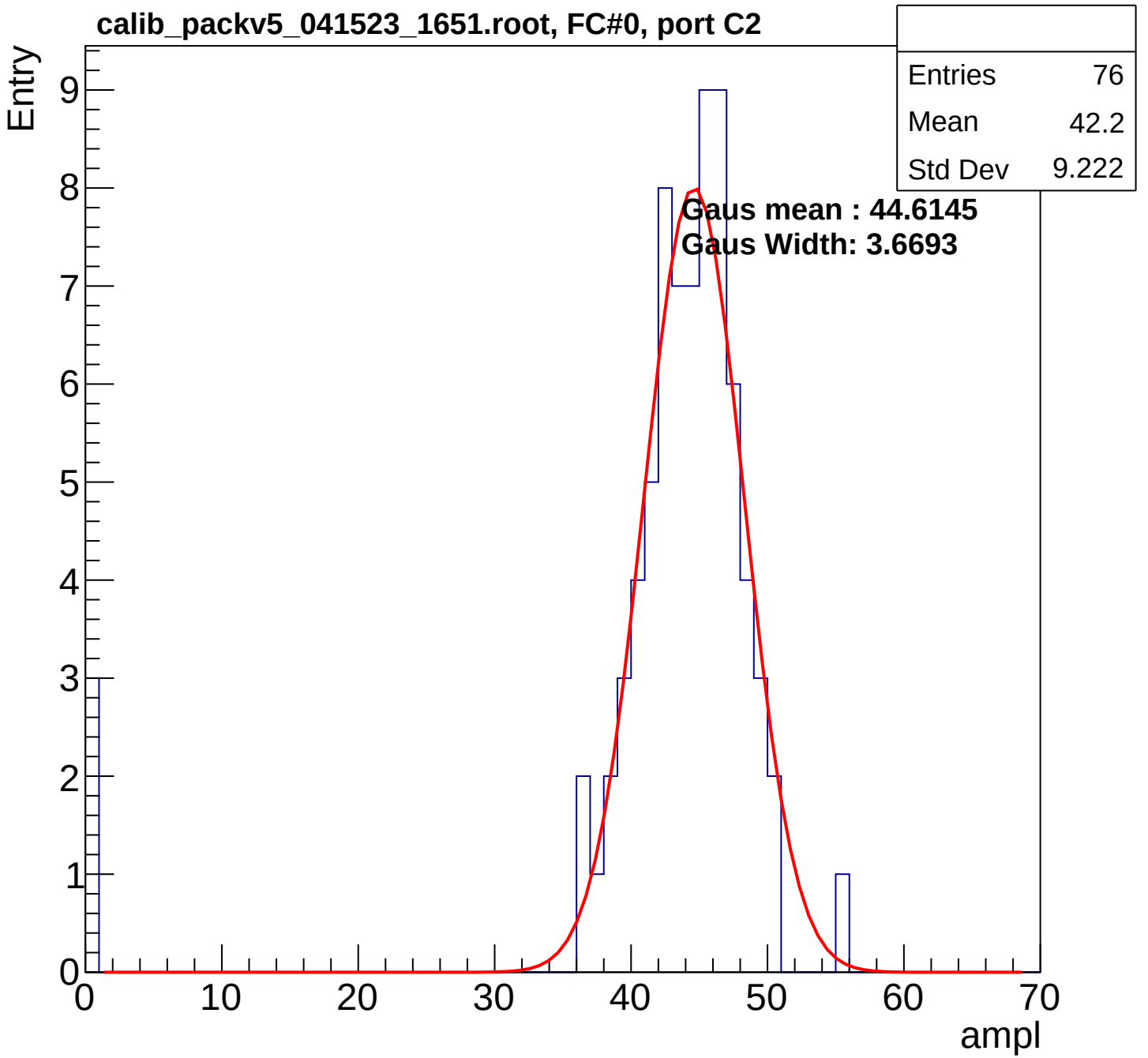
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L103S, U12-ch123, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 42.2
Std Dev 9.222
Gaus mean : 44.6145
Gaus Width: 3.6693
Entry
ampl
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2
3
4
5
6
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0
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60
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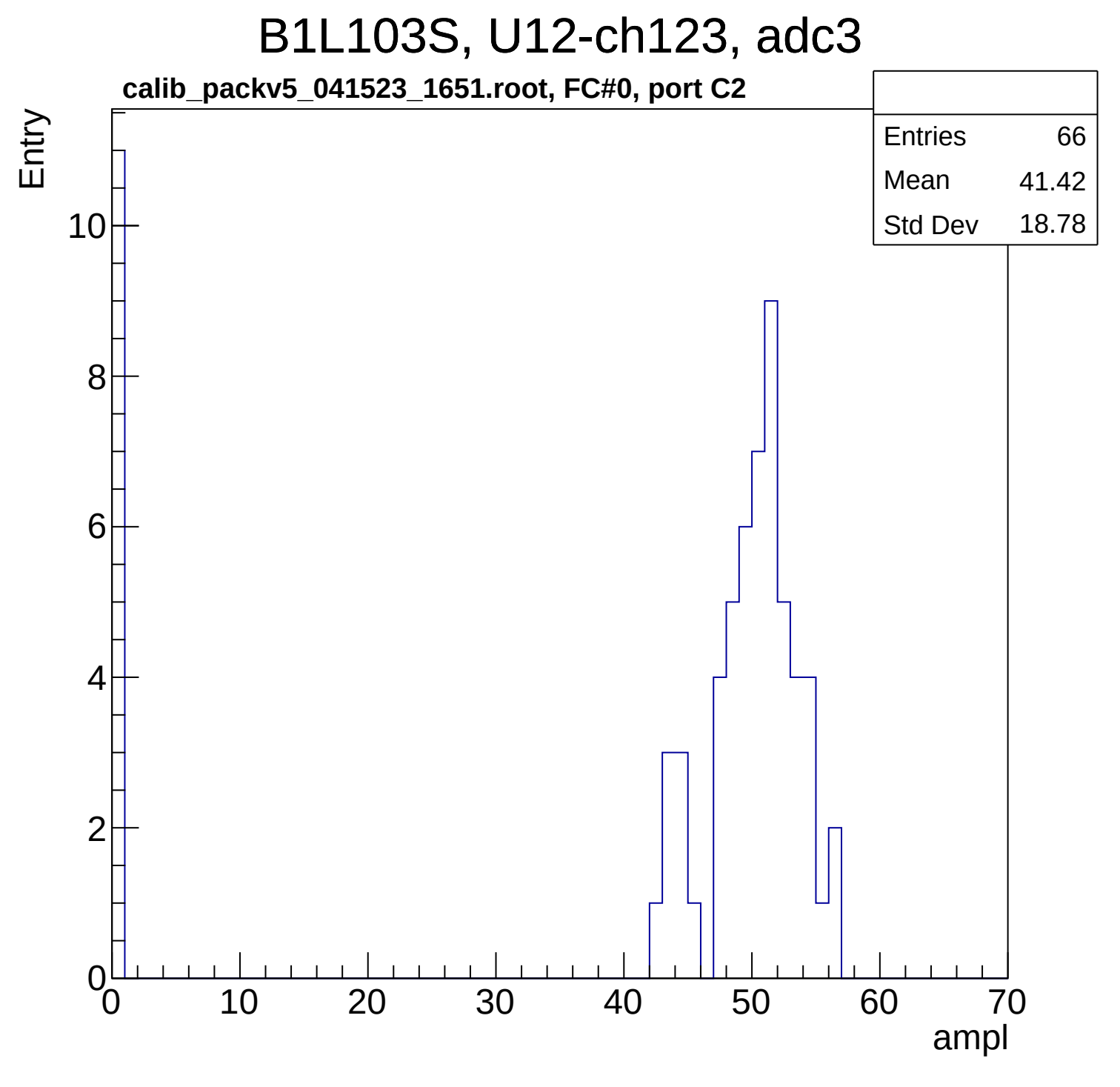
B1L103S, U12-ch123, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 66
Mean 41.42
Std Dev 18.78
Entry
ampl
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4
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60
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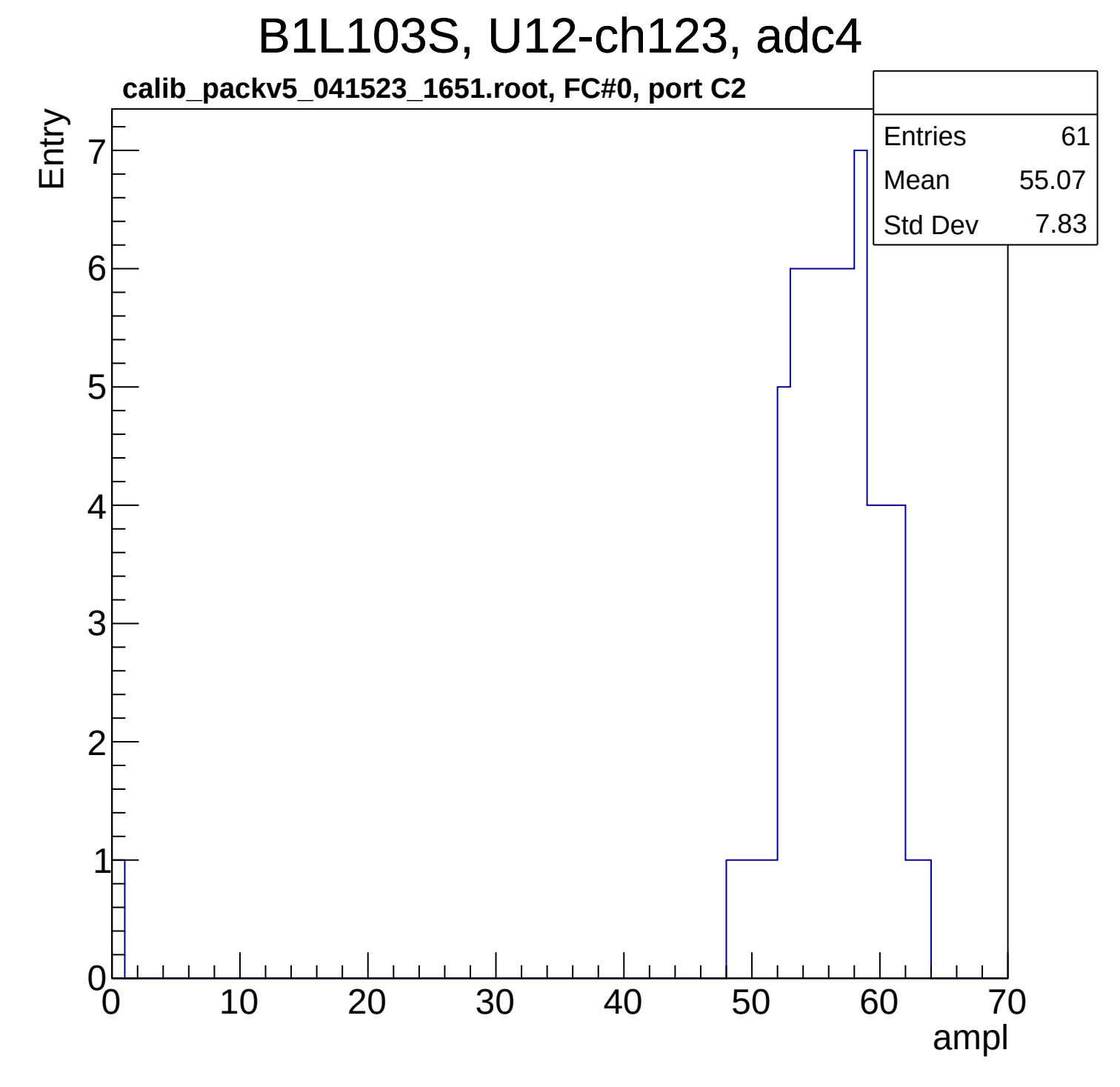
B1L103S, U12-ch123, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 61
Mean 55.07
Std Dev 7.83
Entry
ampl
0
1
2
3
4
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0
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60
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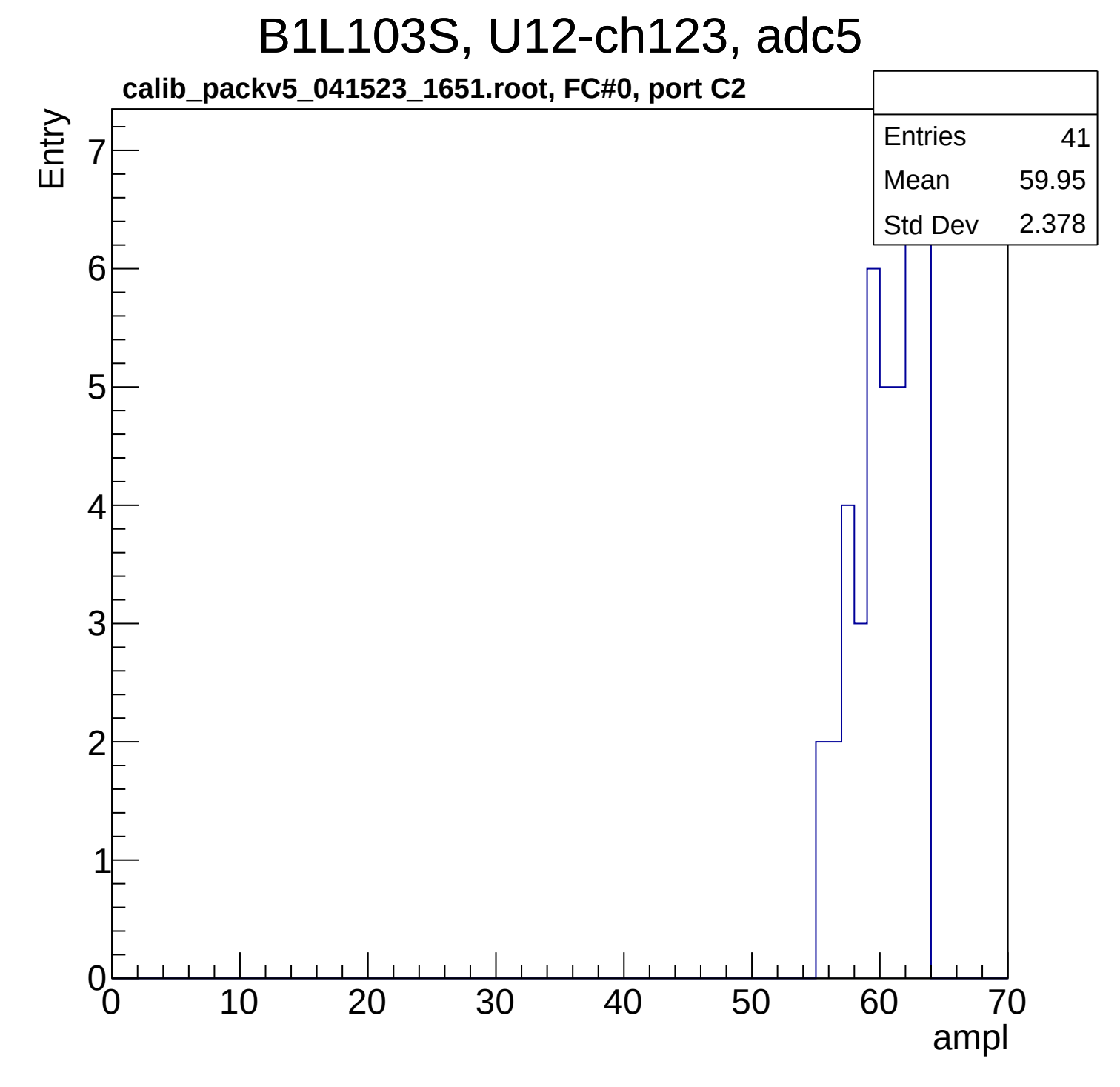
B1L103S, U12-ch123, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 41
Mean 59.95
Std Dev 2.378
Entry
ampl
0
1
2
3
4
5
6
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0
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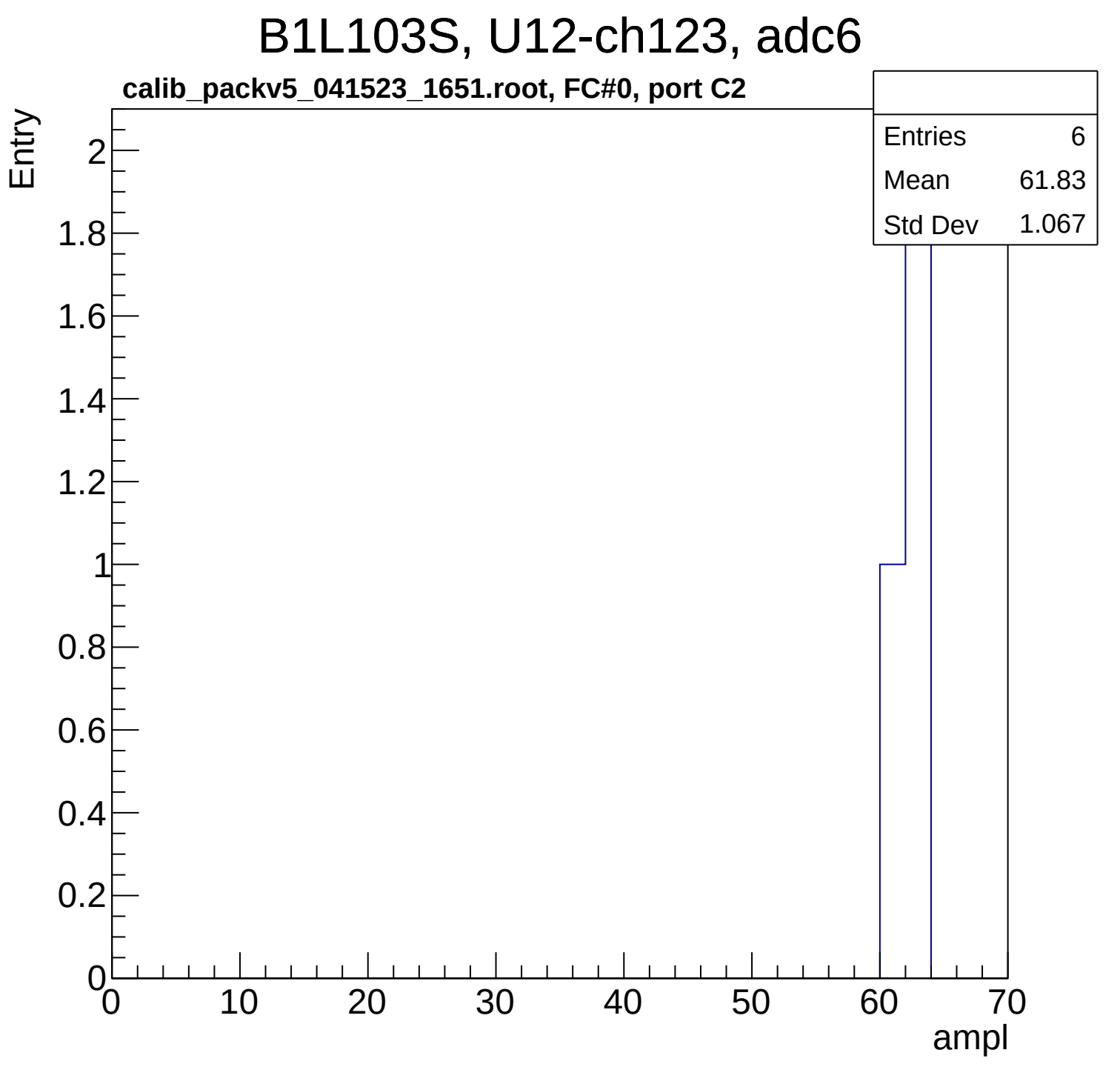
B1L103S, U12-ch123, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 6
Mean 61.83
Std Dev 1.067
Entry
ampl
0
0.2
0.4
0.6
0.8
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1.2
1.4
1.6
1.8
2
0
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60
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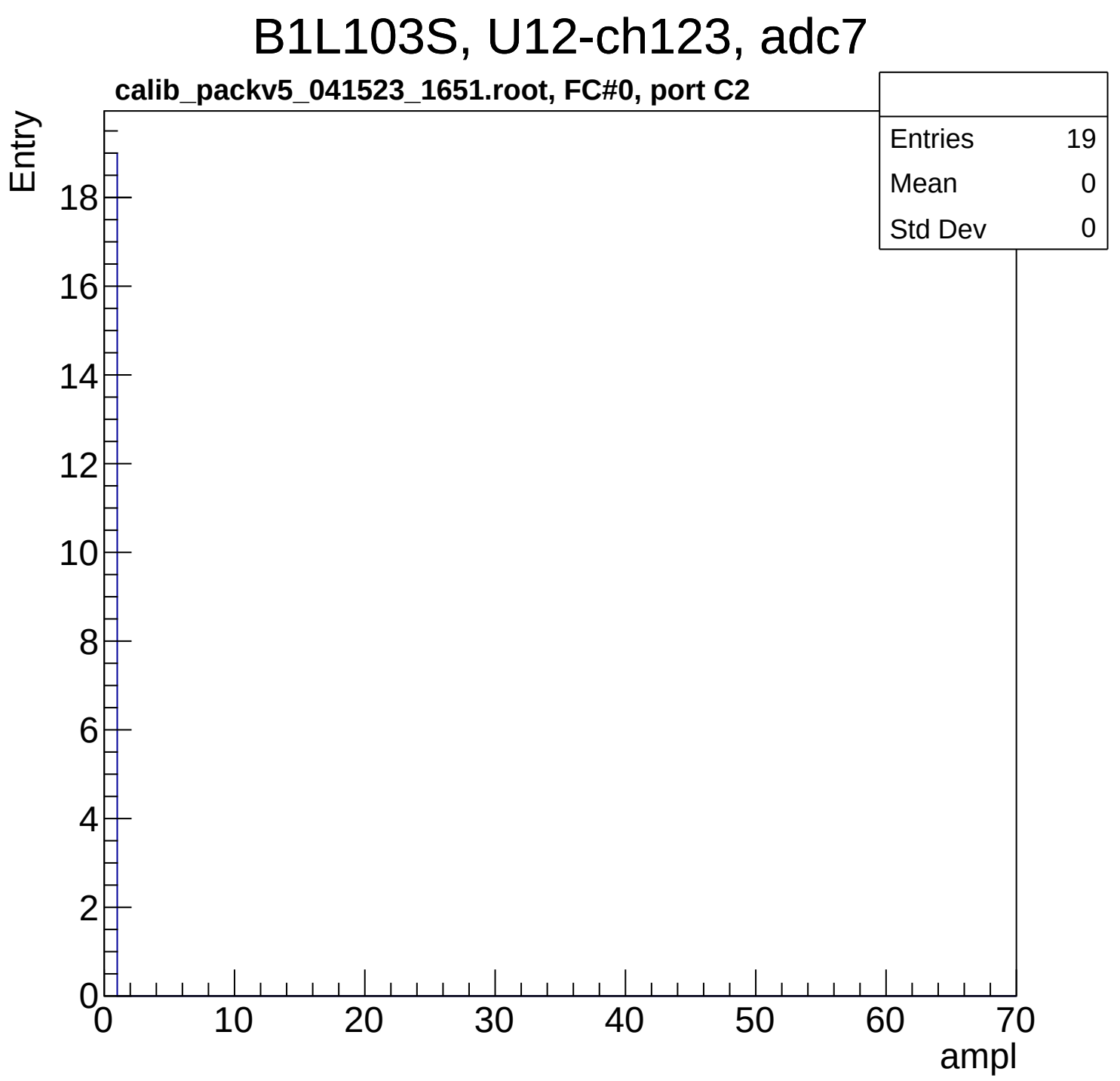
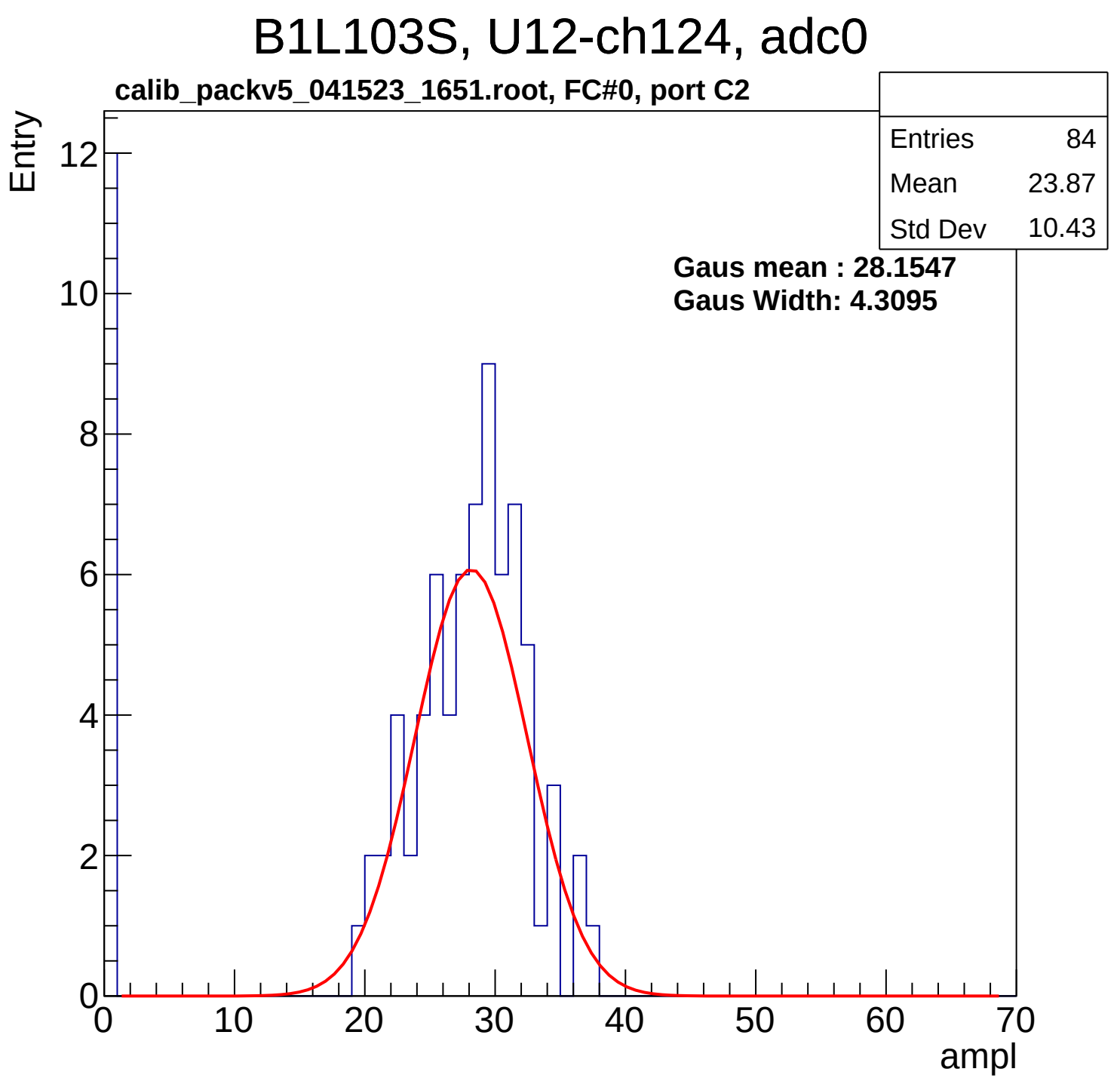
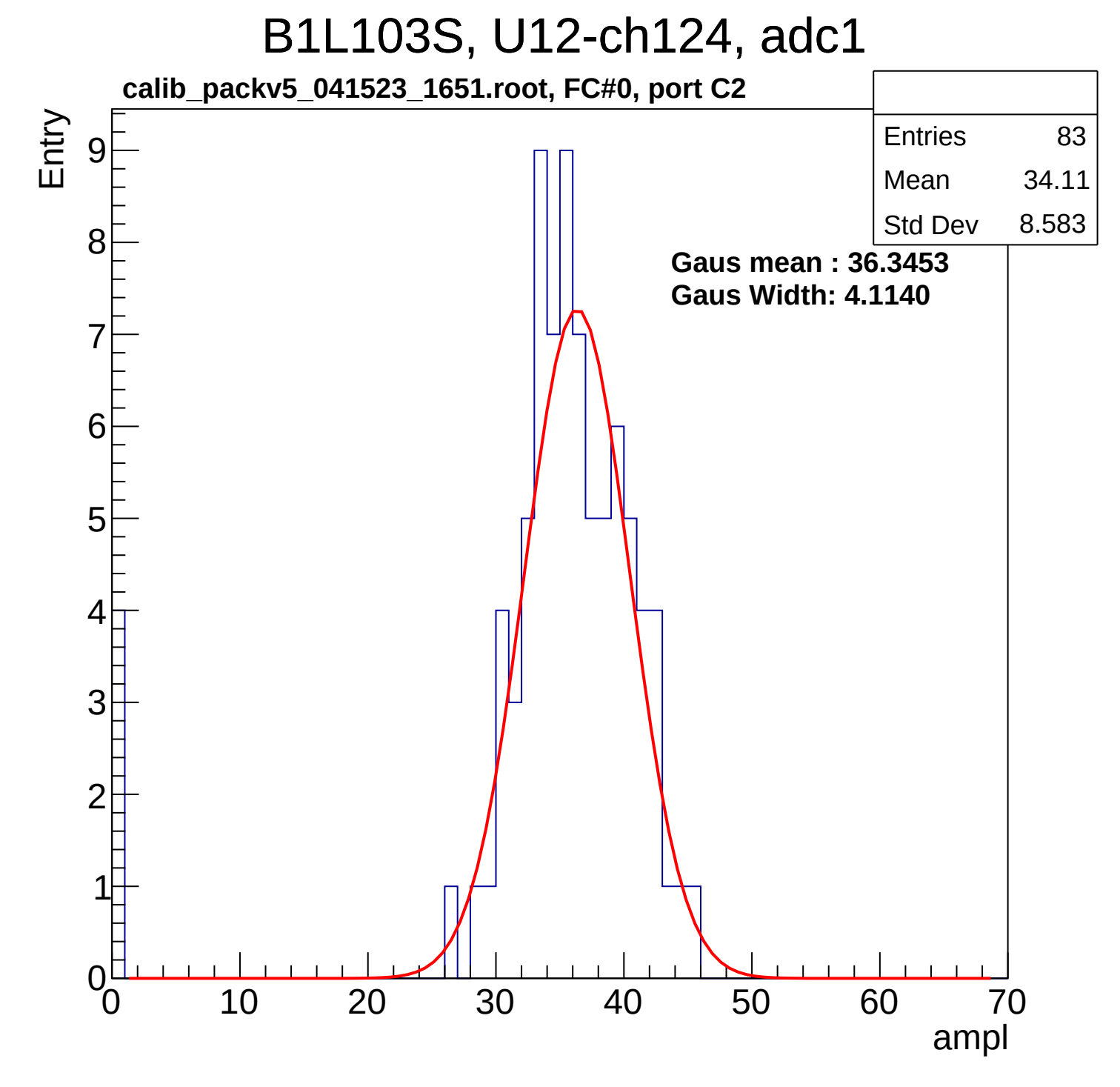

B1L103S, U12-ch123, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch124, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 84
Mean 23.87
Std Dev 10.43
Gaus mean : 28.1547
Gaus Width: 4.3095
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
70


B1L103S, U12-ch124, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 83
Mean 34.11
Std Dev 8.583
Gaus mean : 36.3453
Gaus Width: 4.1140
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
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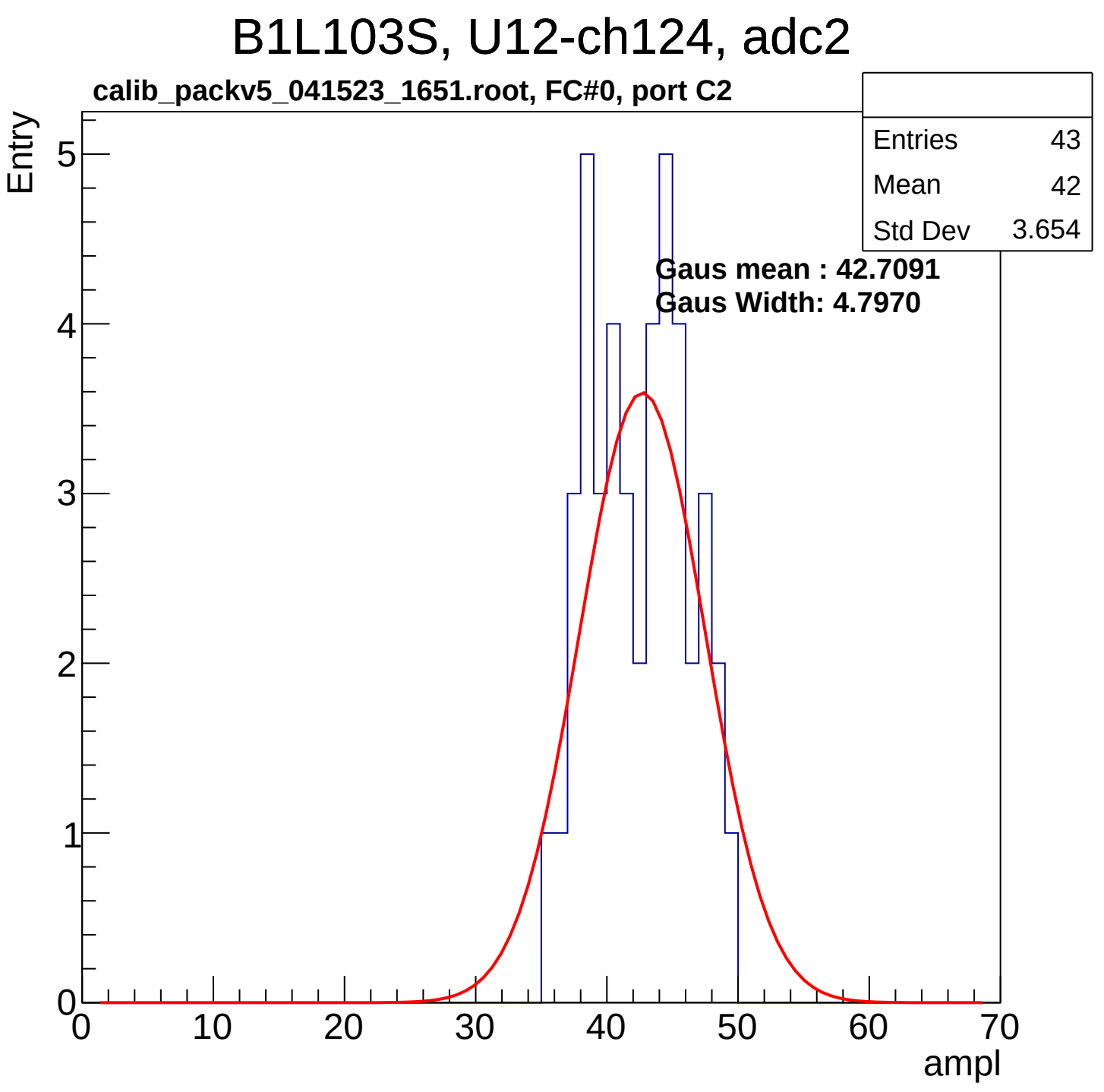
B1L103S, U12-ch124, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 42
Std Dev 3.654
Gaus mean : 42.7091
Gaus Width: 4.7970
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
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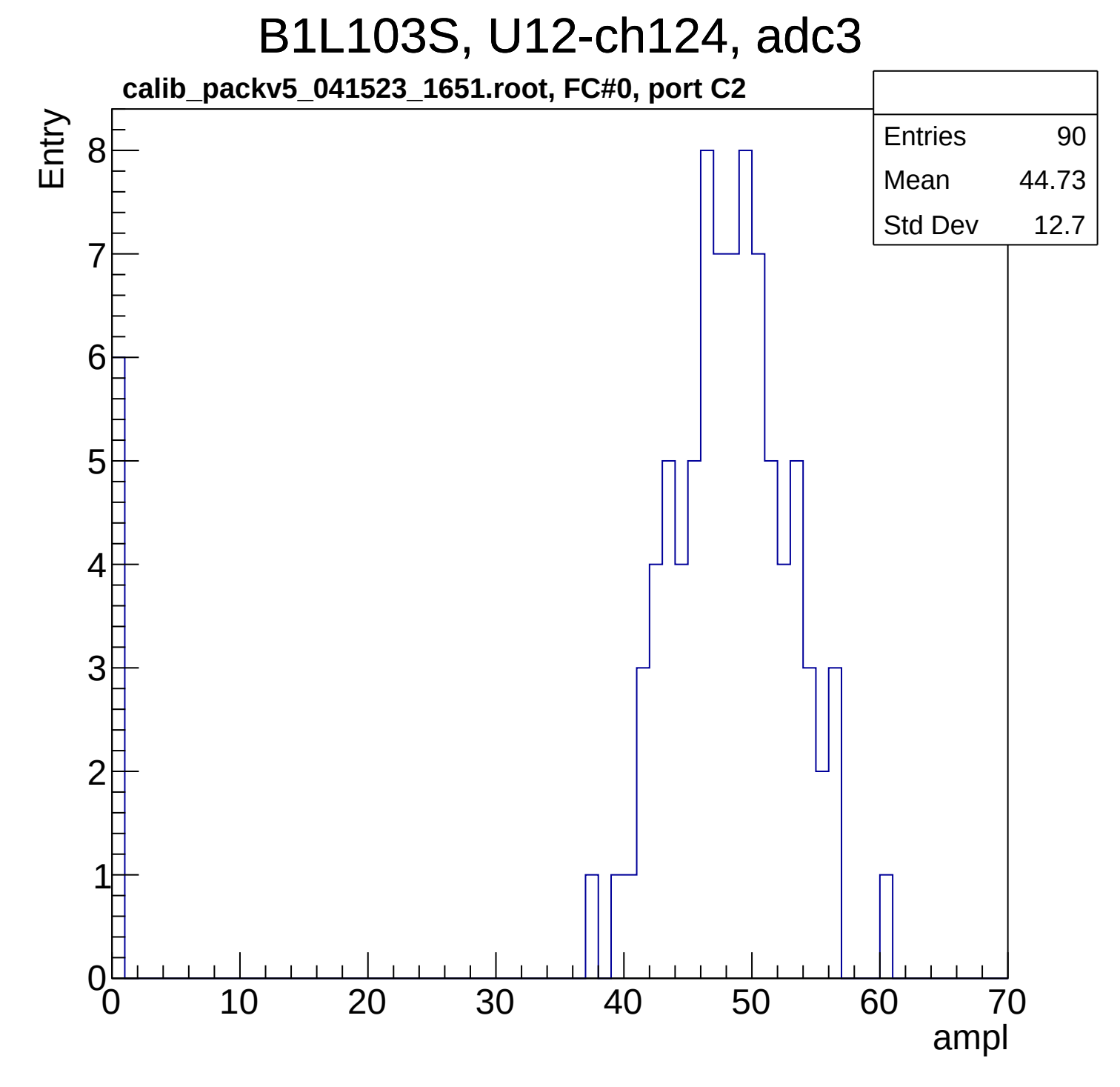
B1L103S, U12-ch124, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 44.73
Std Dev 12.7
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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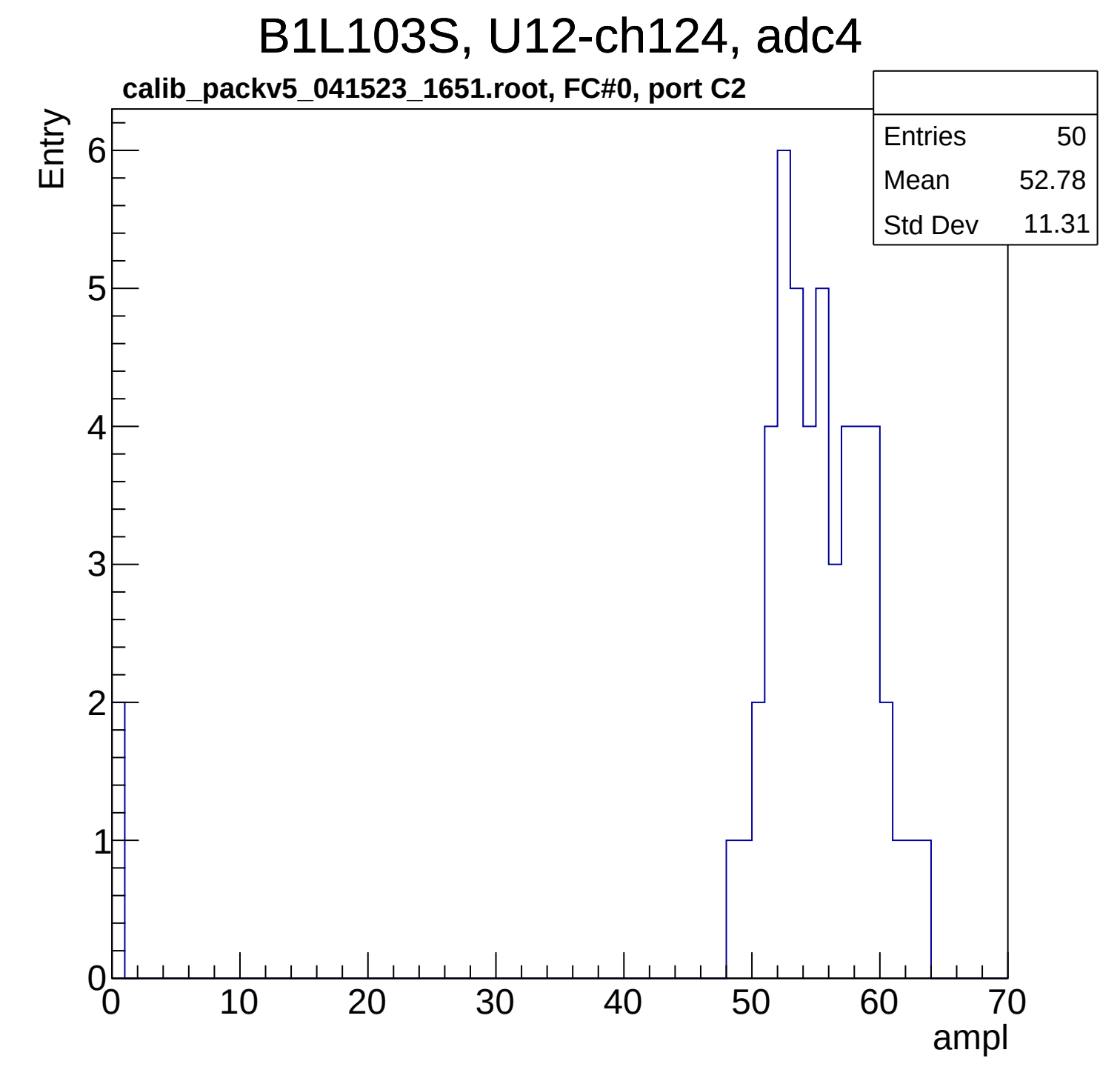
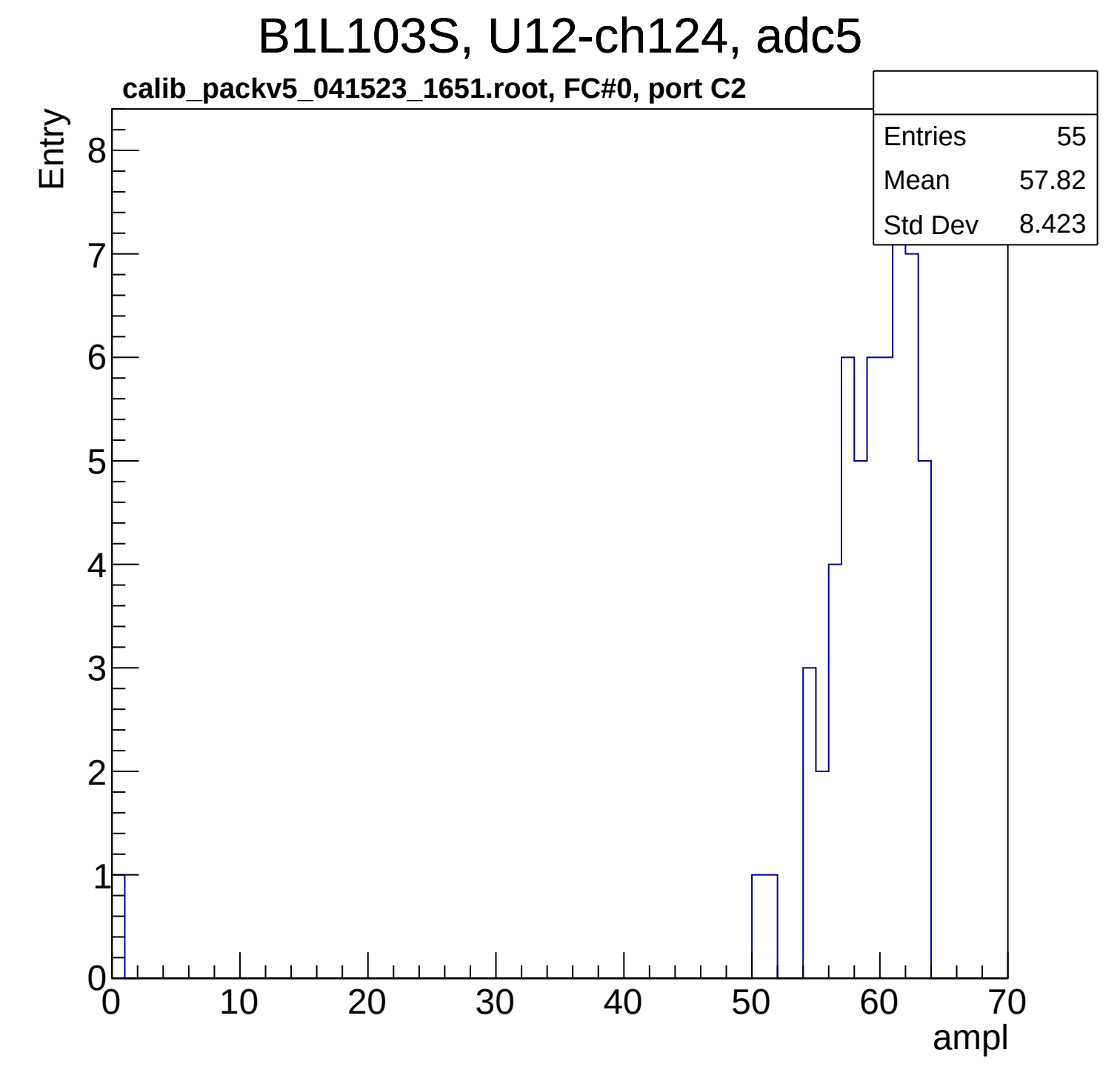

B1L103S, U12-ch124, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 50
Mean 52.78
Std Dev 11.31
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U12-ch124, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 57.82
Std Dev 8.423
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
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40
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60
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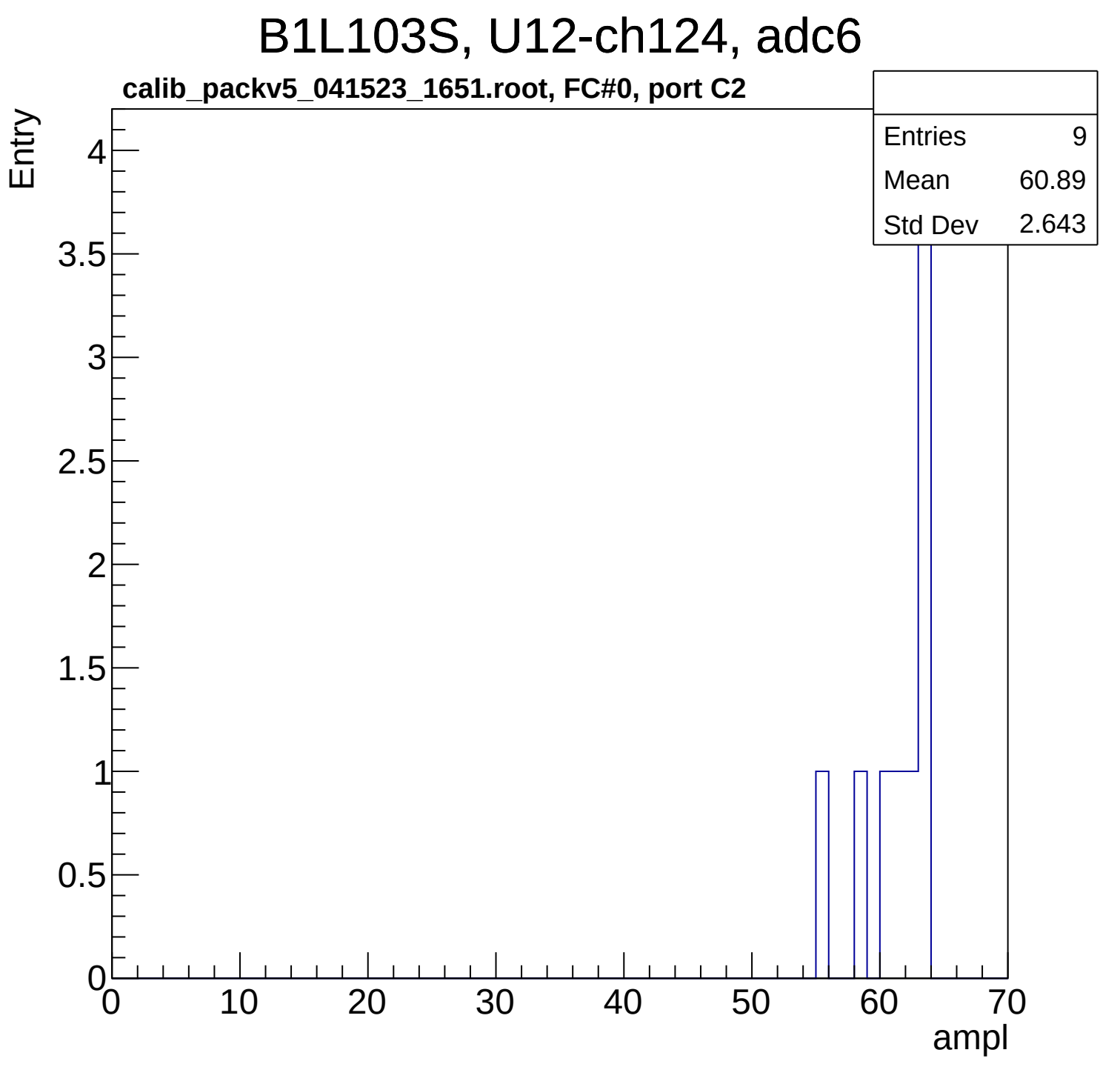
B1L103S, U12-ch124, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 9
Mean 60.89
Std Dev 2.643
Entry
ampl
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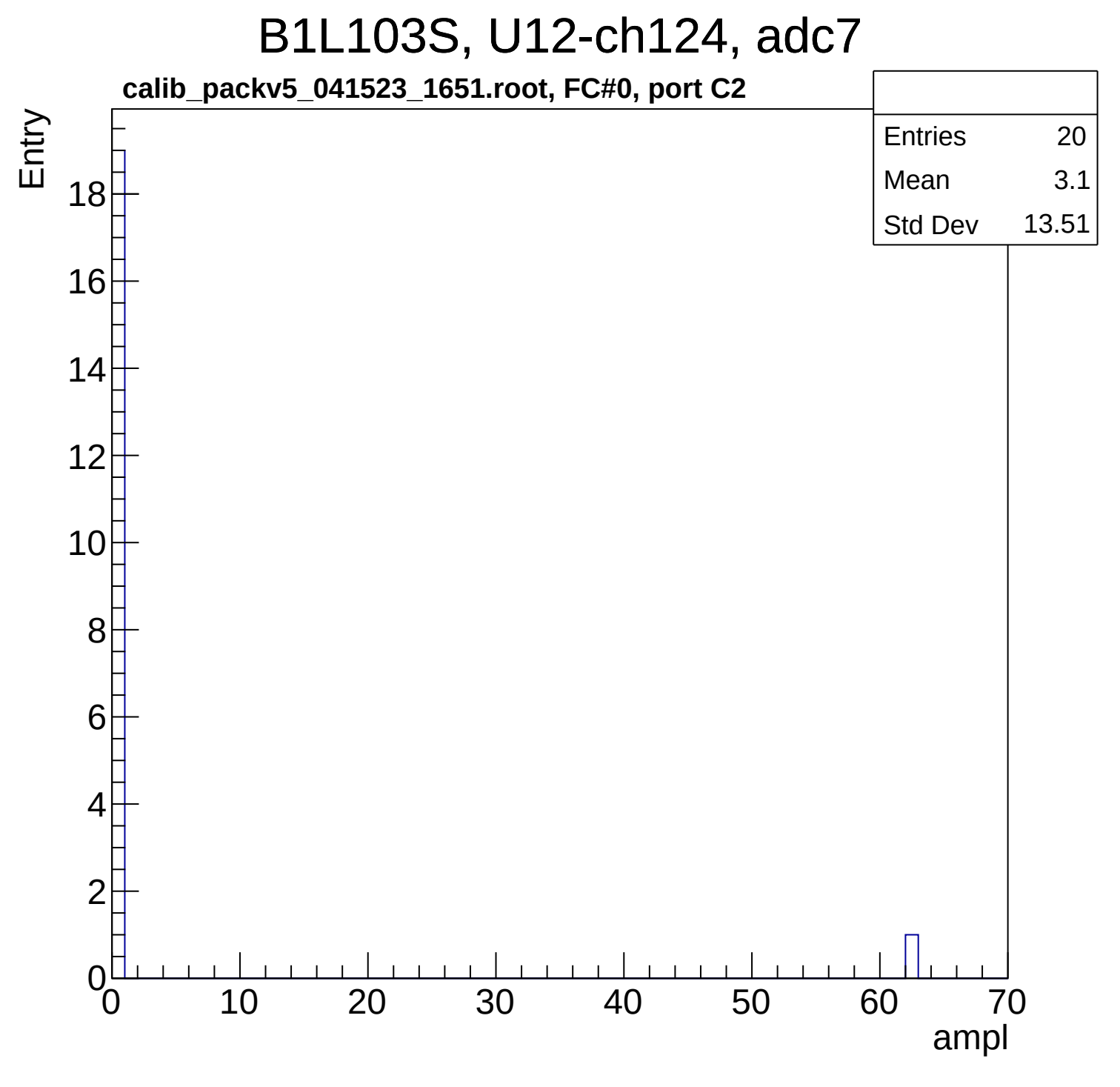
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L103S, U12-ch124, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 20
Mean 3.1
Std Dev 13.51
Entry
0
2
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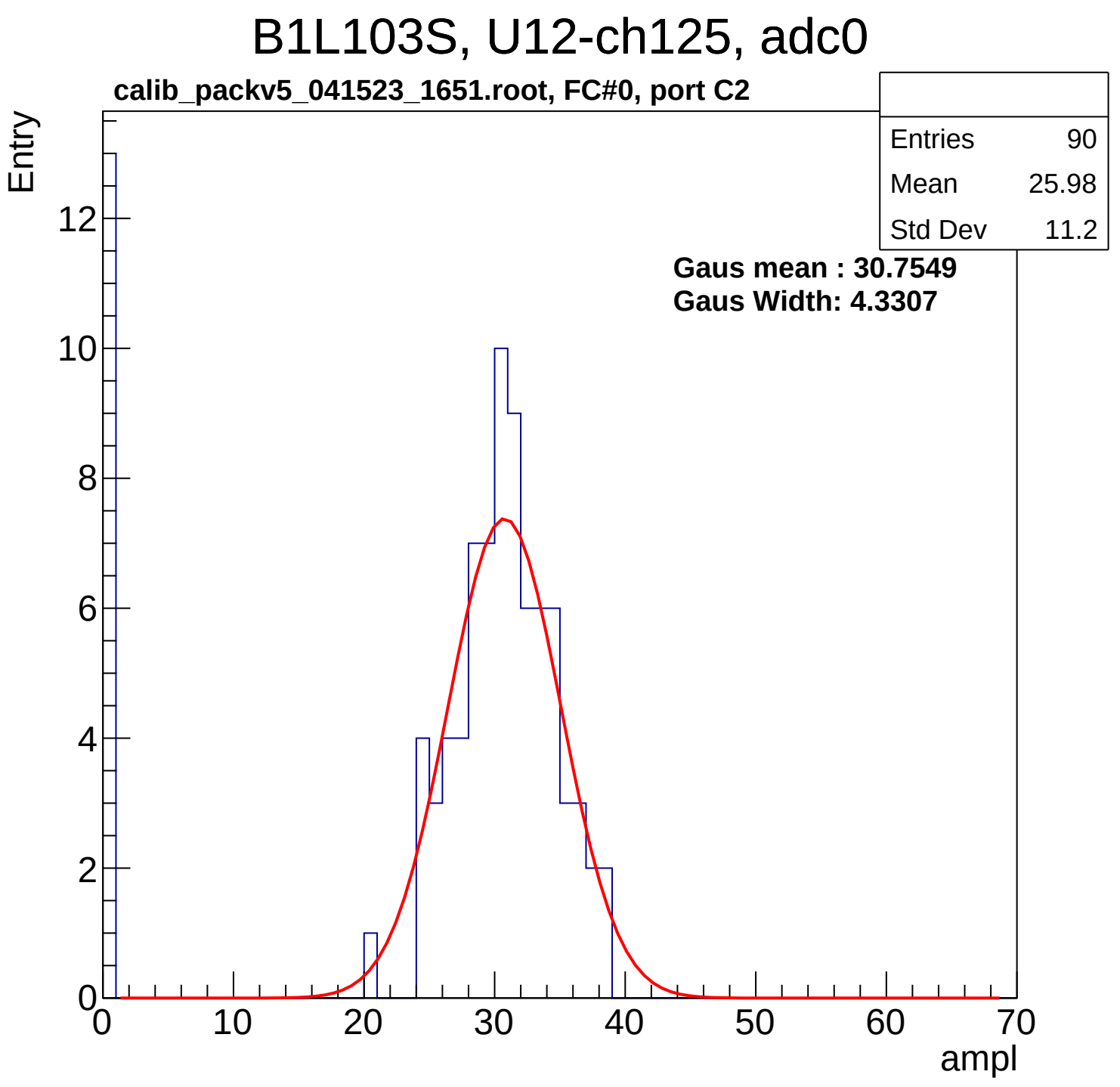
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch125, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 25.98
Std Dev 11.2
Gaus mean : 30.7549
Gaus Width: 4.3307
Entry
ampl
0
2
4
6
8
10
12
0
10
20
30
40
50
60
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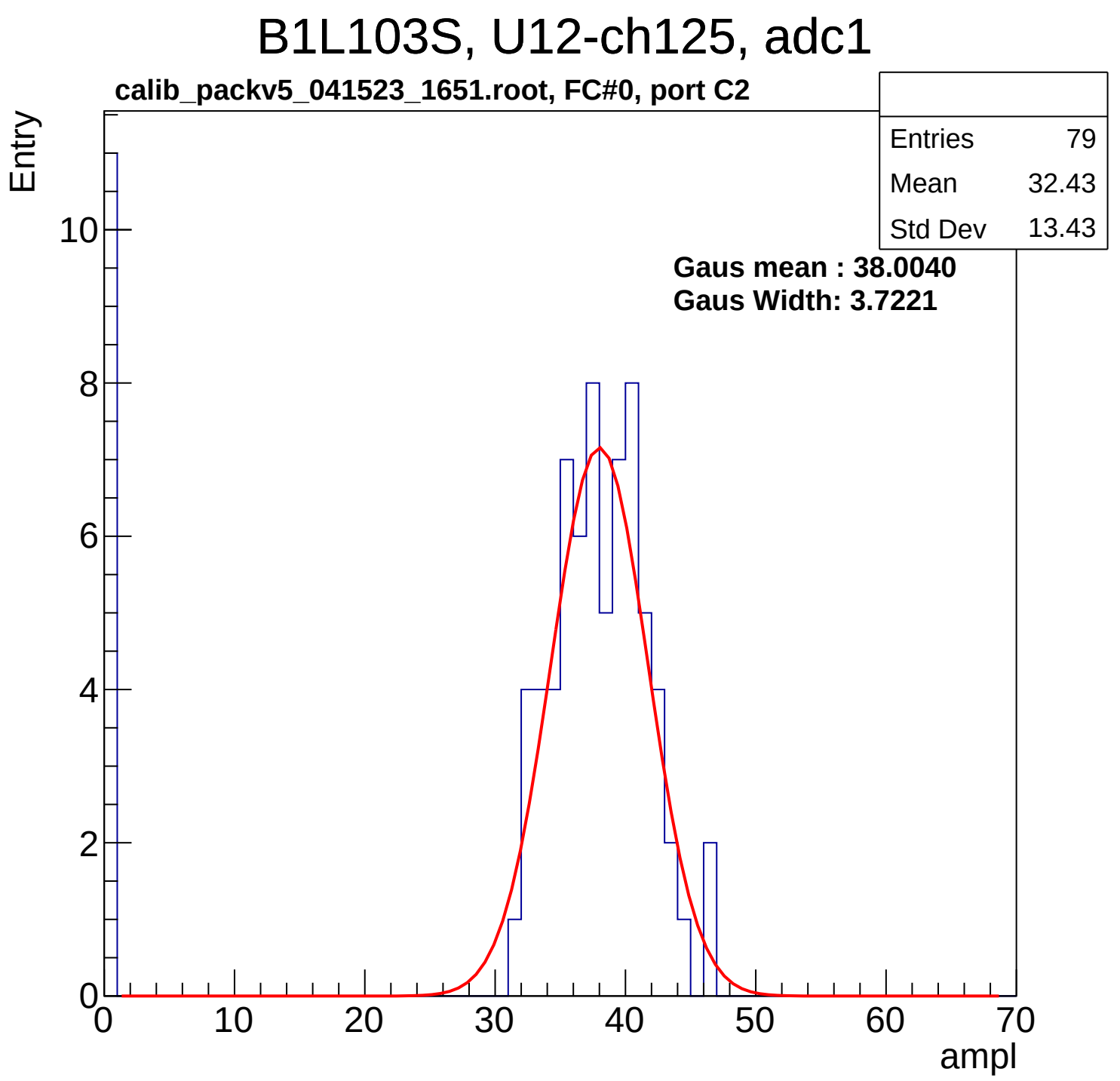
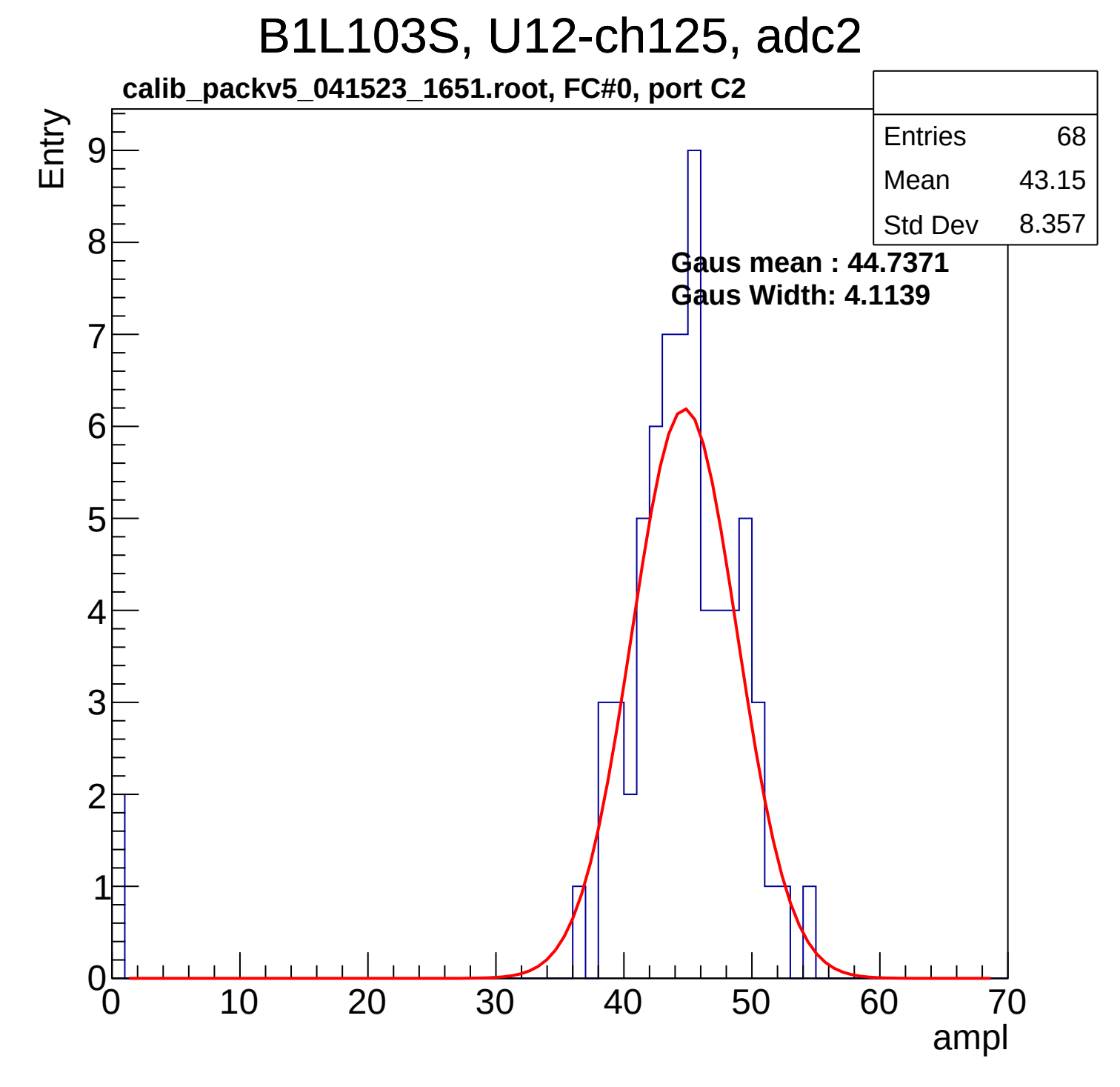

B1L103S, U12-ch125, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 79
Mean 32.43
Std Dev 13.43
Gaus mean : 38.0040
Gaus Width: 3.7221
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70


B1L103S, U12-ch125, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 68
Mean 43.15
Std Dev 8.357
Gaus mean : 44.7371
Gaus Width: 4.1139
Entry
ampl
0
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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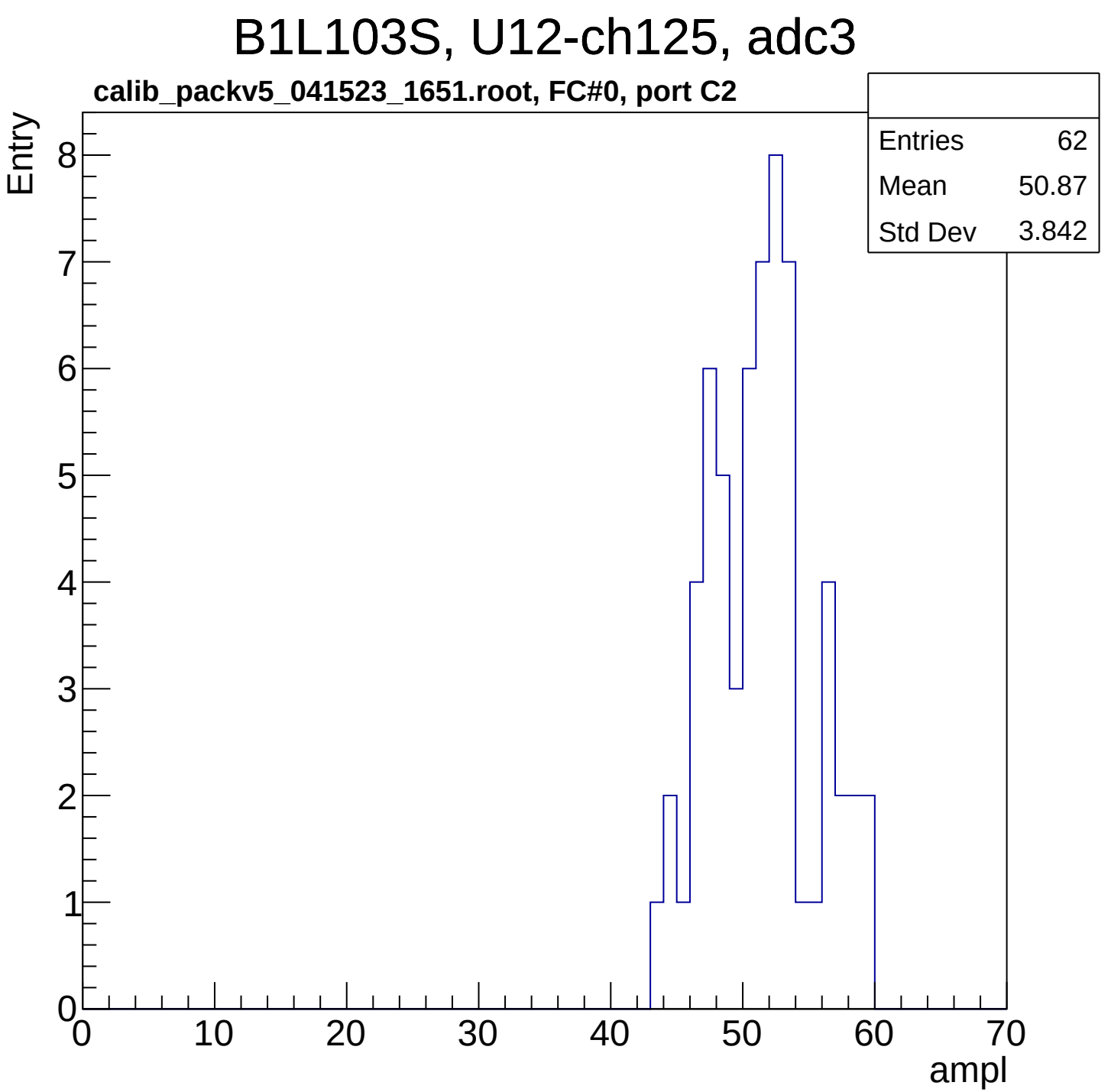
B1L103S, U12-ch125, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 62
Mean 50.87
Std Dev 3.842
Entry
ampl
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1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
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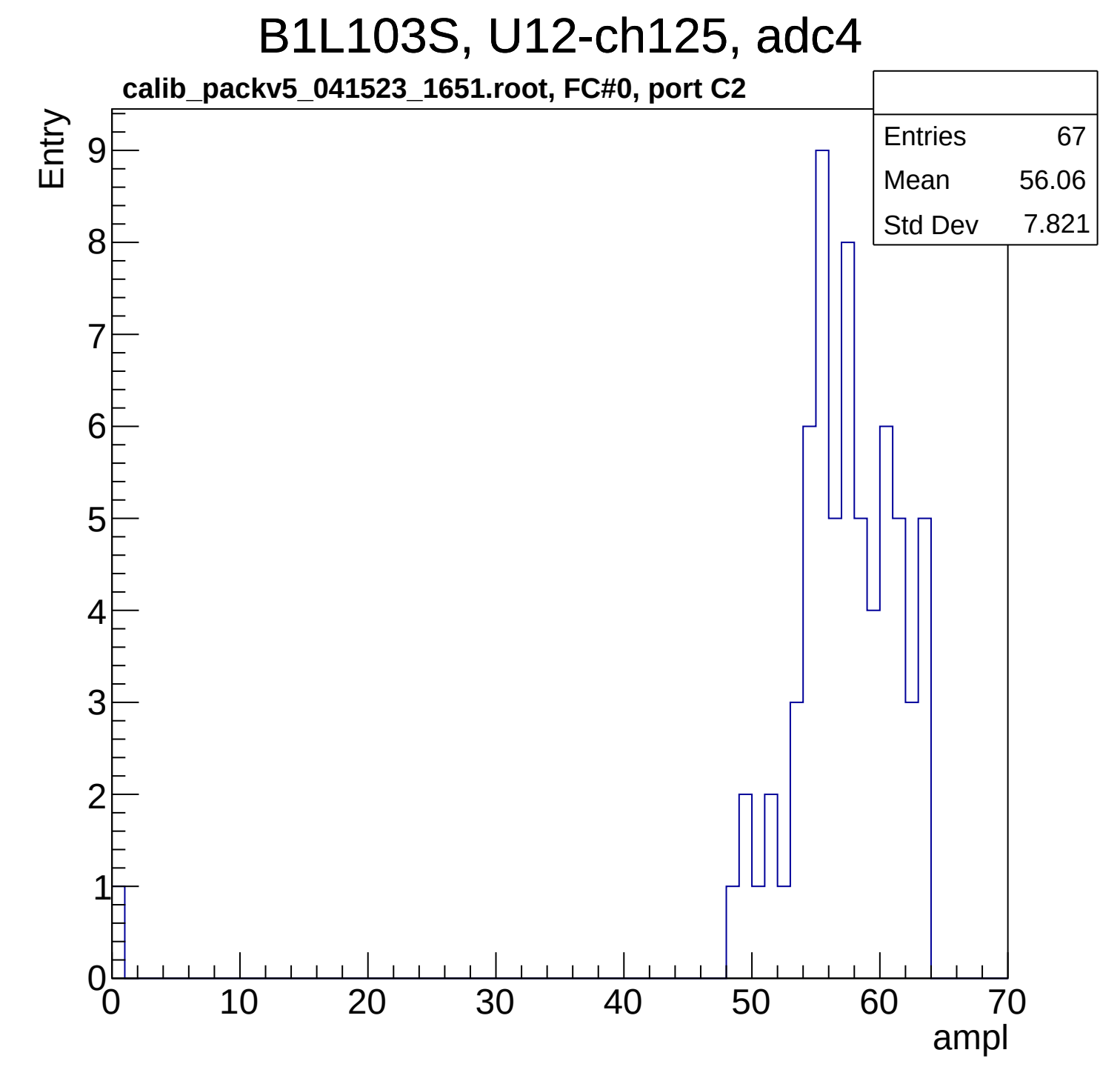
B1L103S, U12-ch125, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 67
Mean 56.06
Std Dev 7.821
Entry
ampl
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2
3
4
5
6
7
8
9
0
10
20
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40
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60
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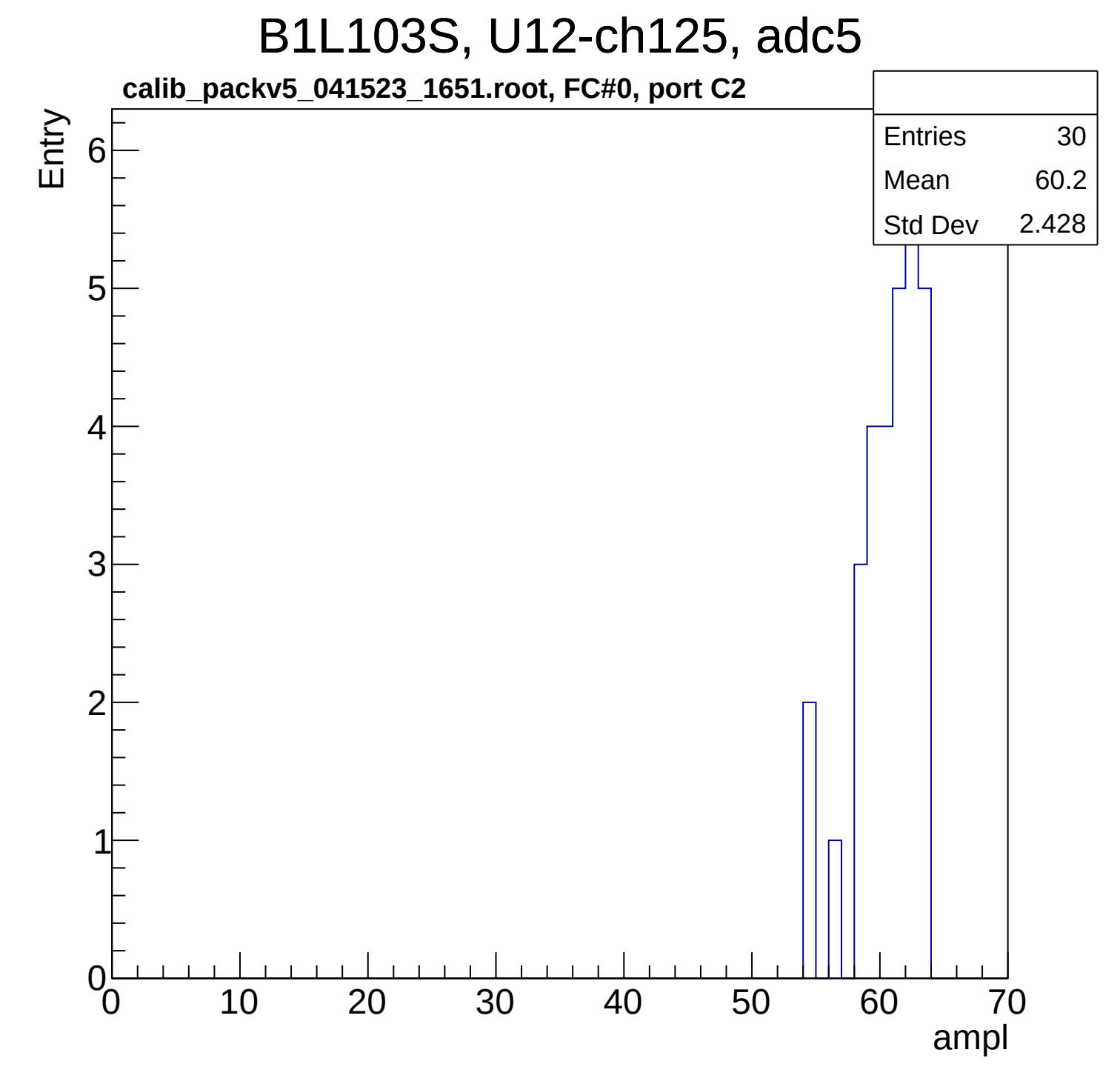
B1L103S, U12-ch125, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 30
Mean 60.2
Std Dev 2.428
Entry
ampl
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2
3
4
5
6
0
10
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40
50
60
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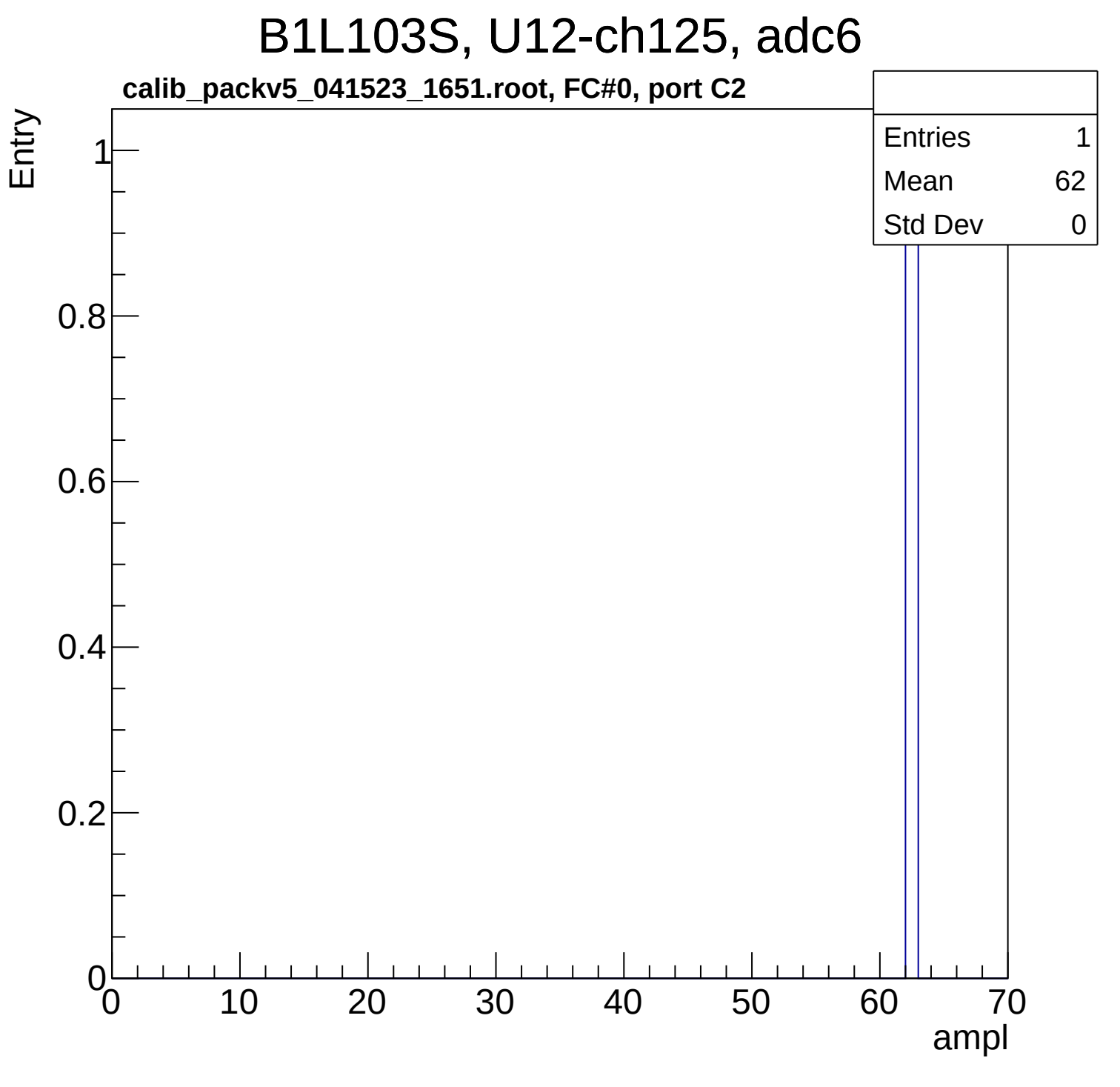
B1L103S, U12-ch125, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 1
Mean 62
Std Dev 0
Entry
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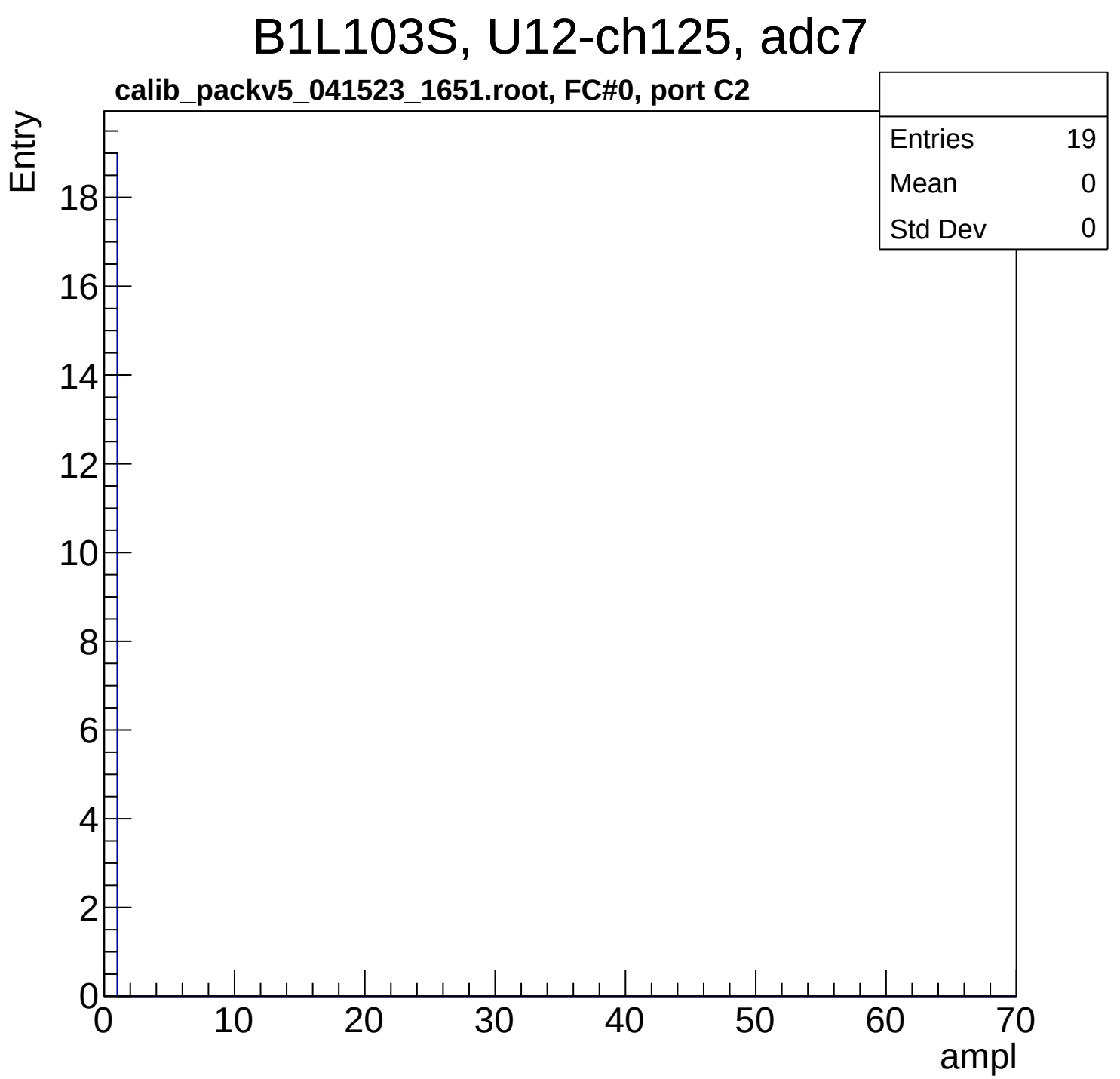
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch125, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
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2
4
6
8
10
12
14
16
18
0
10
20
30
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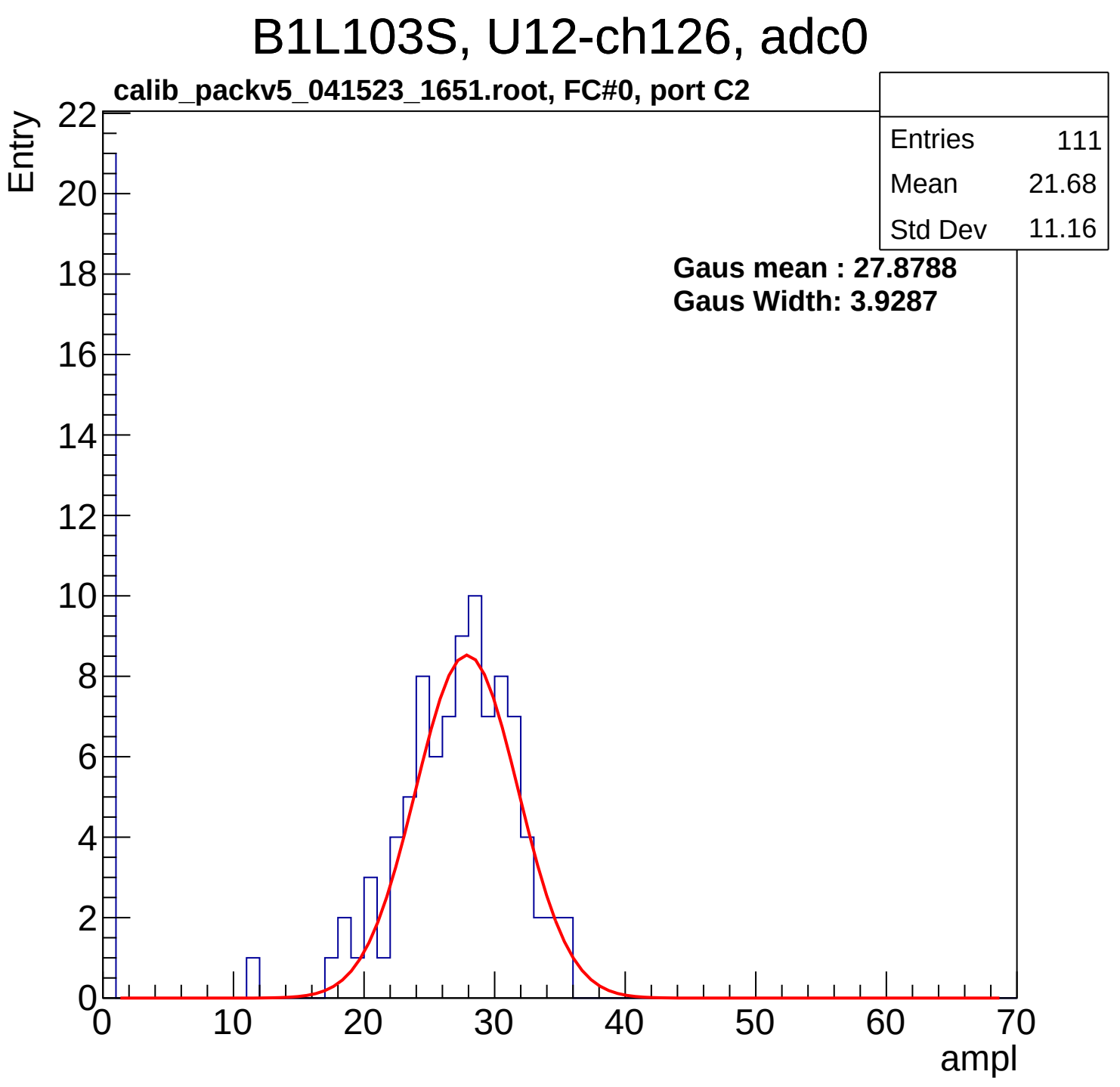
50
60
70
ampl


B1L103S, U12-ch126, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 111
Mean 21.68
Std Dev 11.16
Gaus mean : 27.8788
Gaus Width: 3.9287
Entry
ampl
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8
10
12
14
16
18
20
22
0
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40
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60
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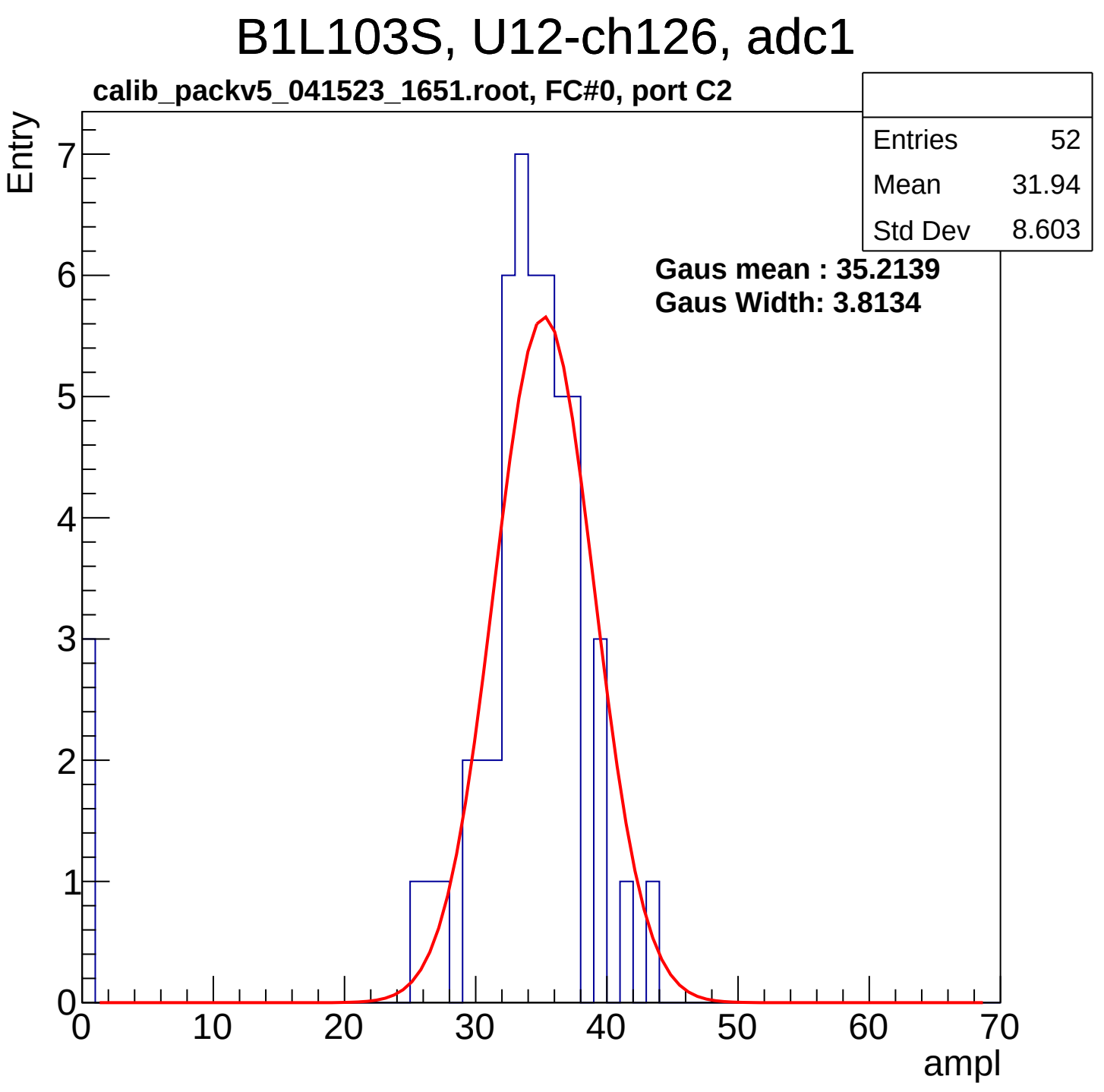
B1L103S, U12-ch126, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 52
Mean 31.94
Std Dev 8.603
Gaus mean : 35.2139
Gaus Width: 3.8134
Entry
ampl
0
1
2
3
4
5
6
7
0
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20
30
40
50
60
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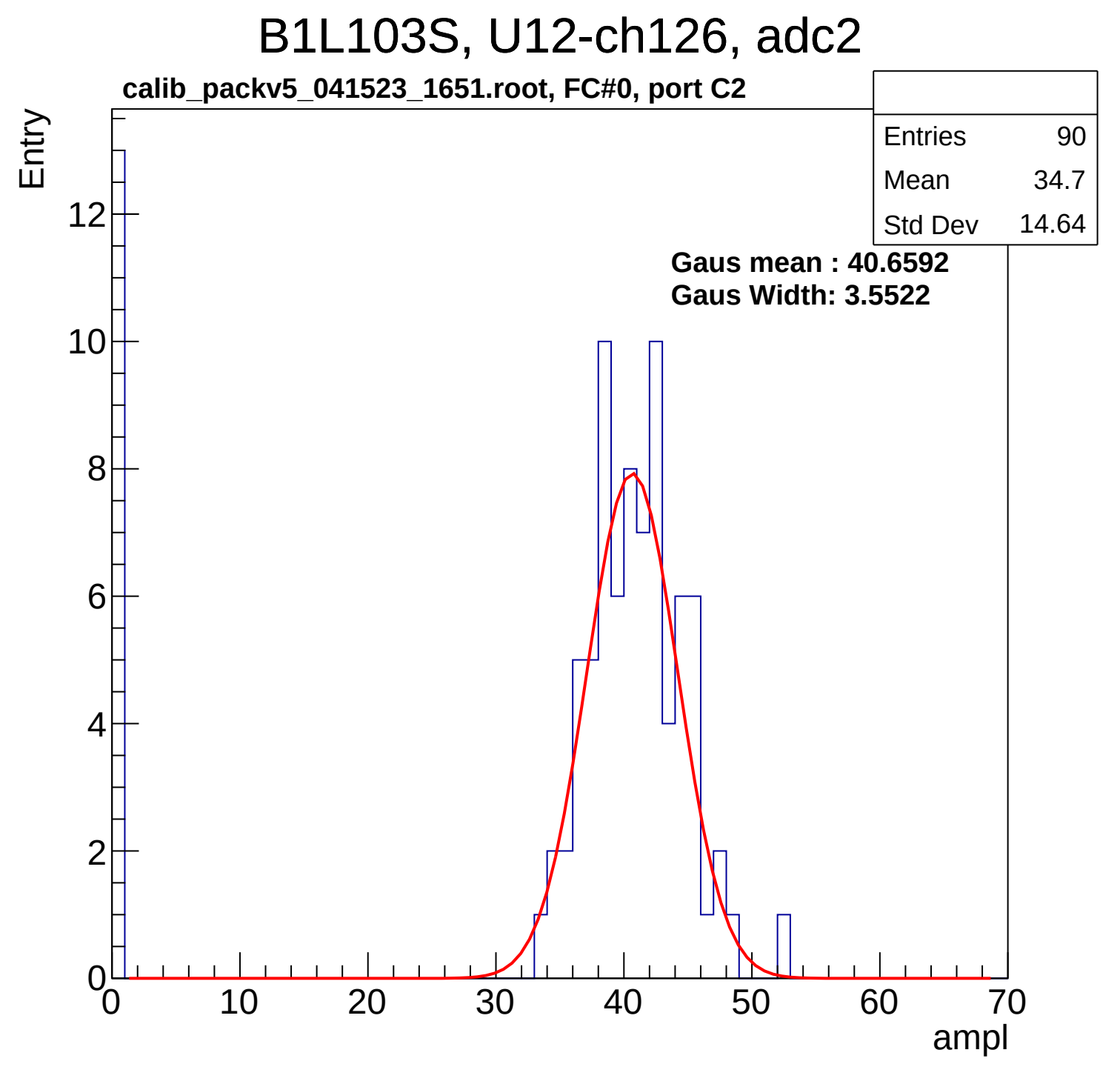
B1L103S, U12-ch126, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 90
Mean 34.7
Std Dev 14.64
Gaus mean : 40.6592
Gaus Width: 3.5522
Entry
ampl
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6
8
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12
0
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60
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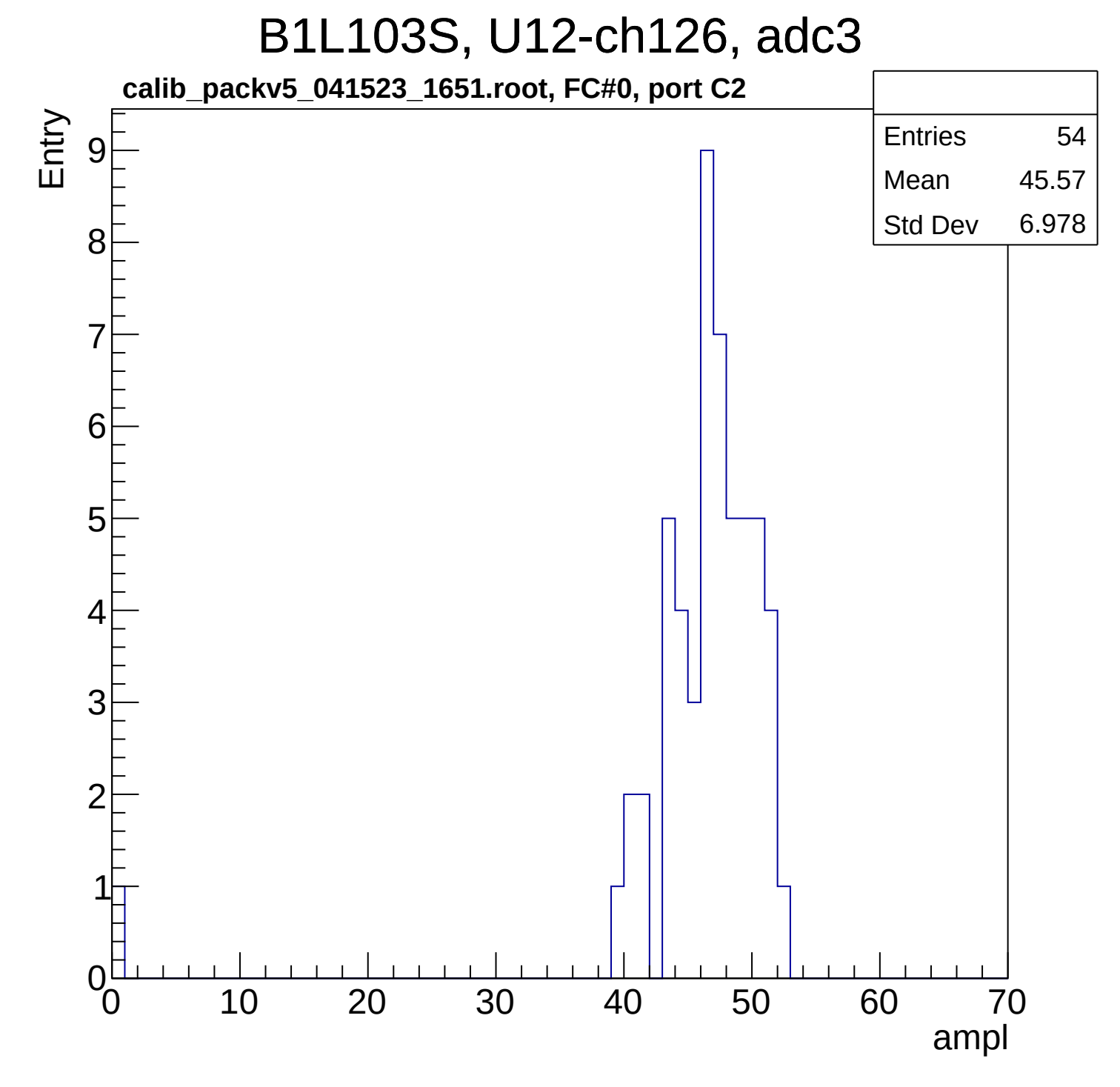
B1L103S, U12-ch126, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 45.57
Std Dev 6.978
Entry
ampl
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4
5
6
7
8
9
0
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20
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60
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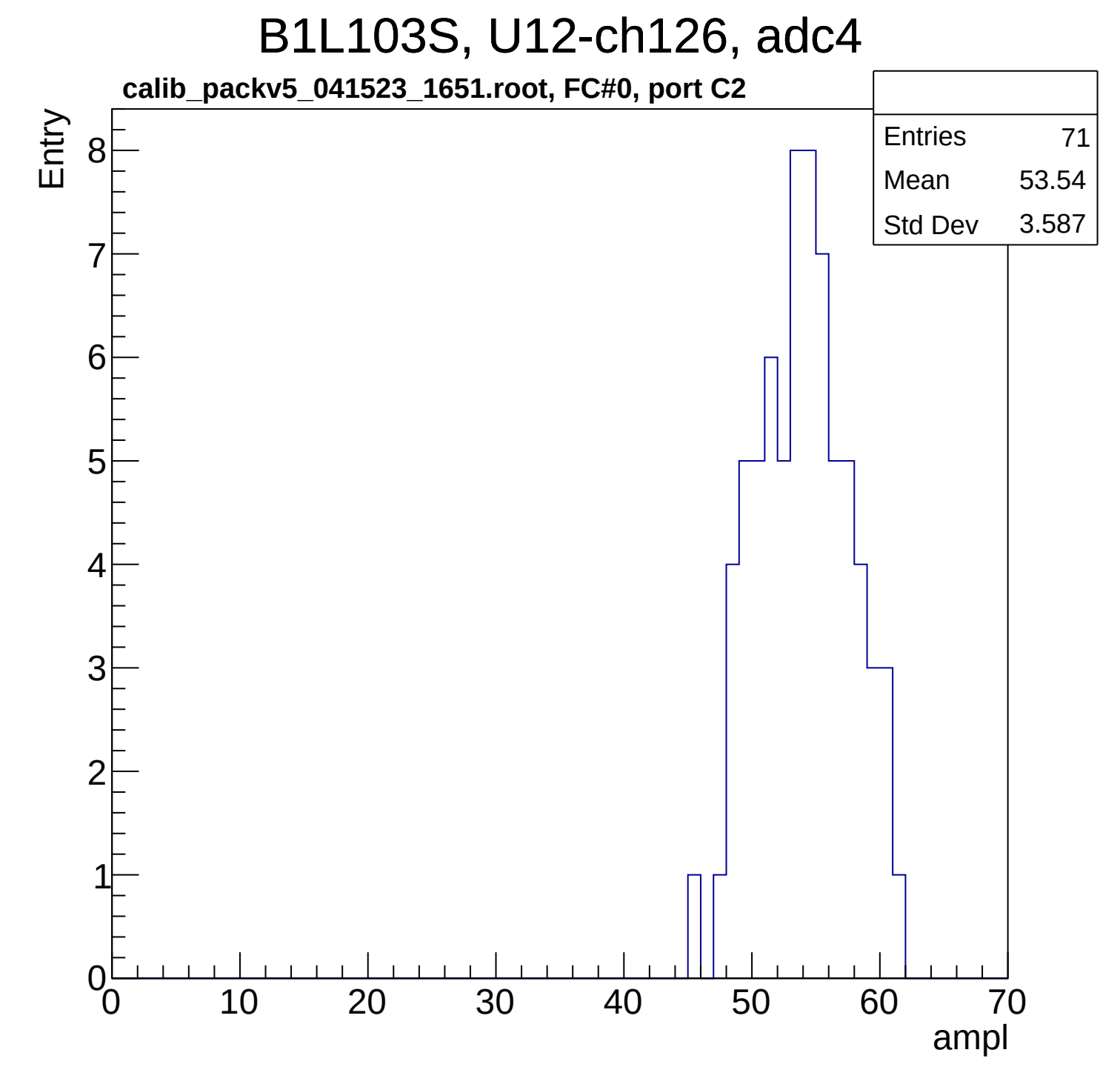
B1L103S, U12-ch126, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 71
Mean 53.54
Std Dev 3.587
Entry
ampl
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2
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4
5
6
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0
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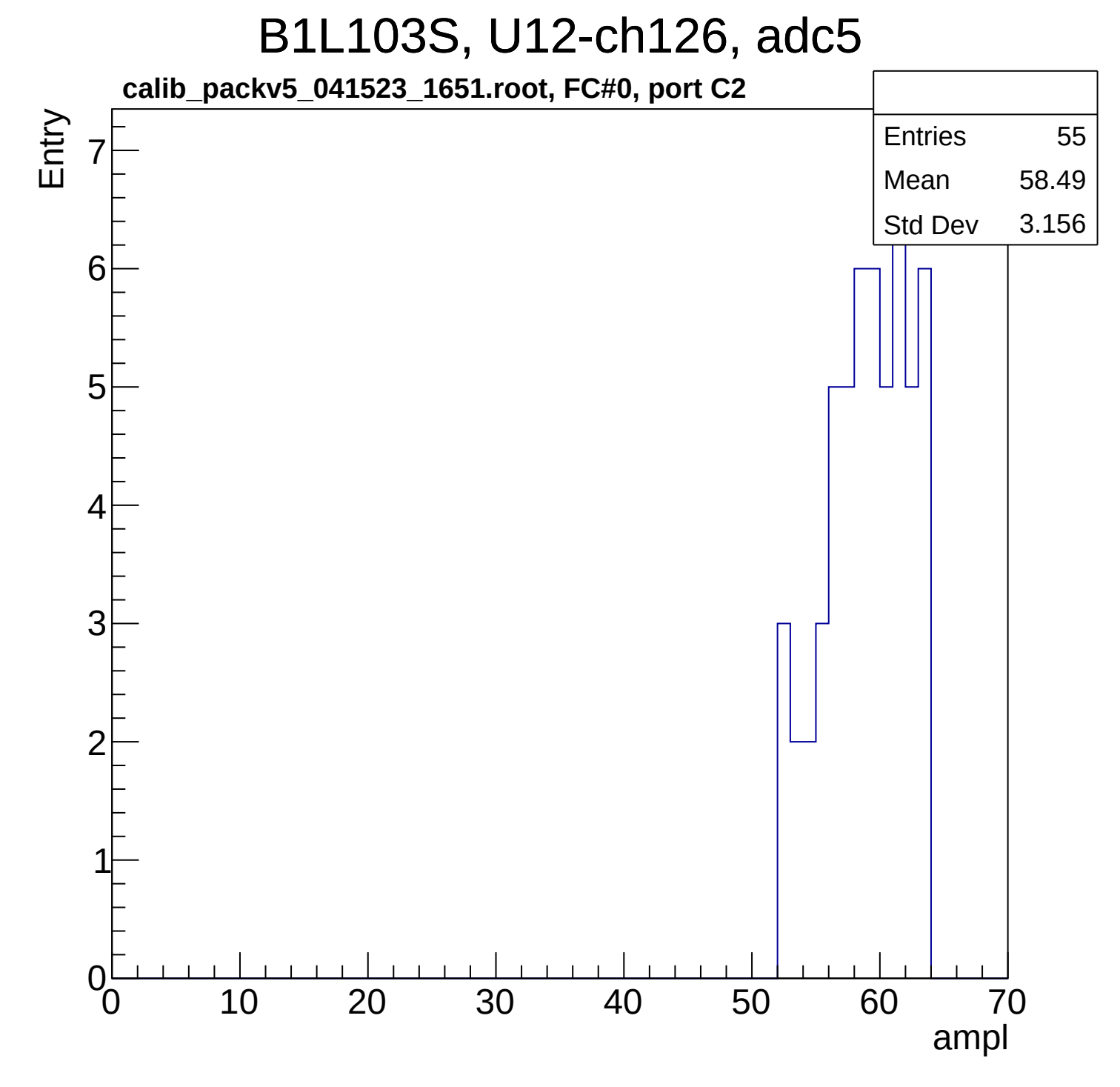
B1L103S, U12-ch126, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 55
Mean 58.49
Std Dev 3.156
Entry
ampl
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2
3
4
5
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0
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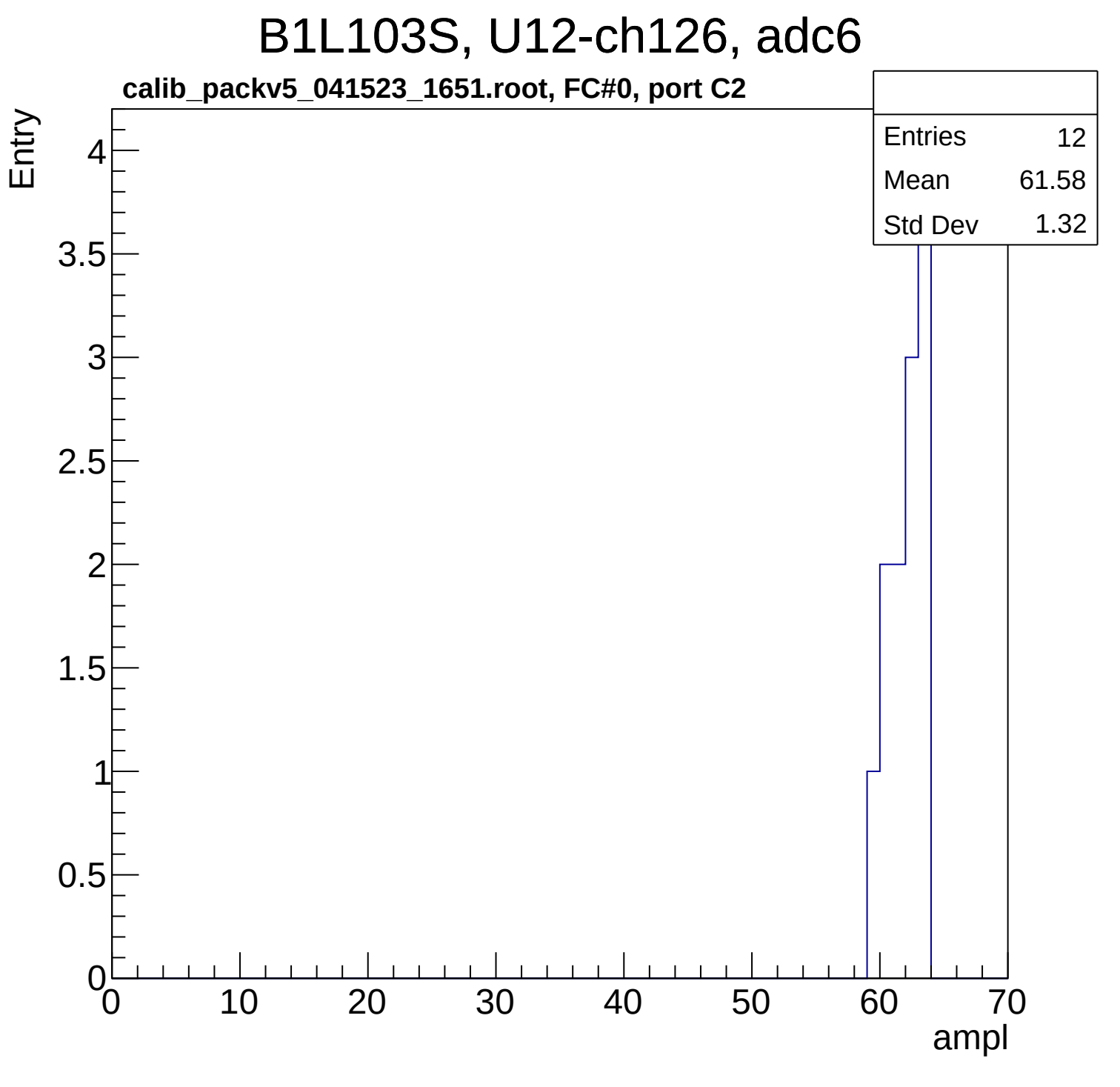
B1L103S, U12-ch126, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 12
Mean 61.58
Std Dev 1.32
Entry
ampl
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1.5
2
2.5
3
3.5
4
0
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60
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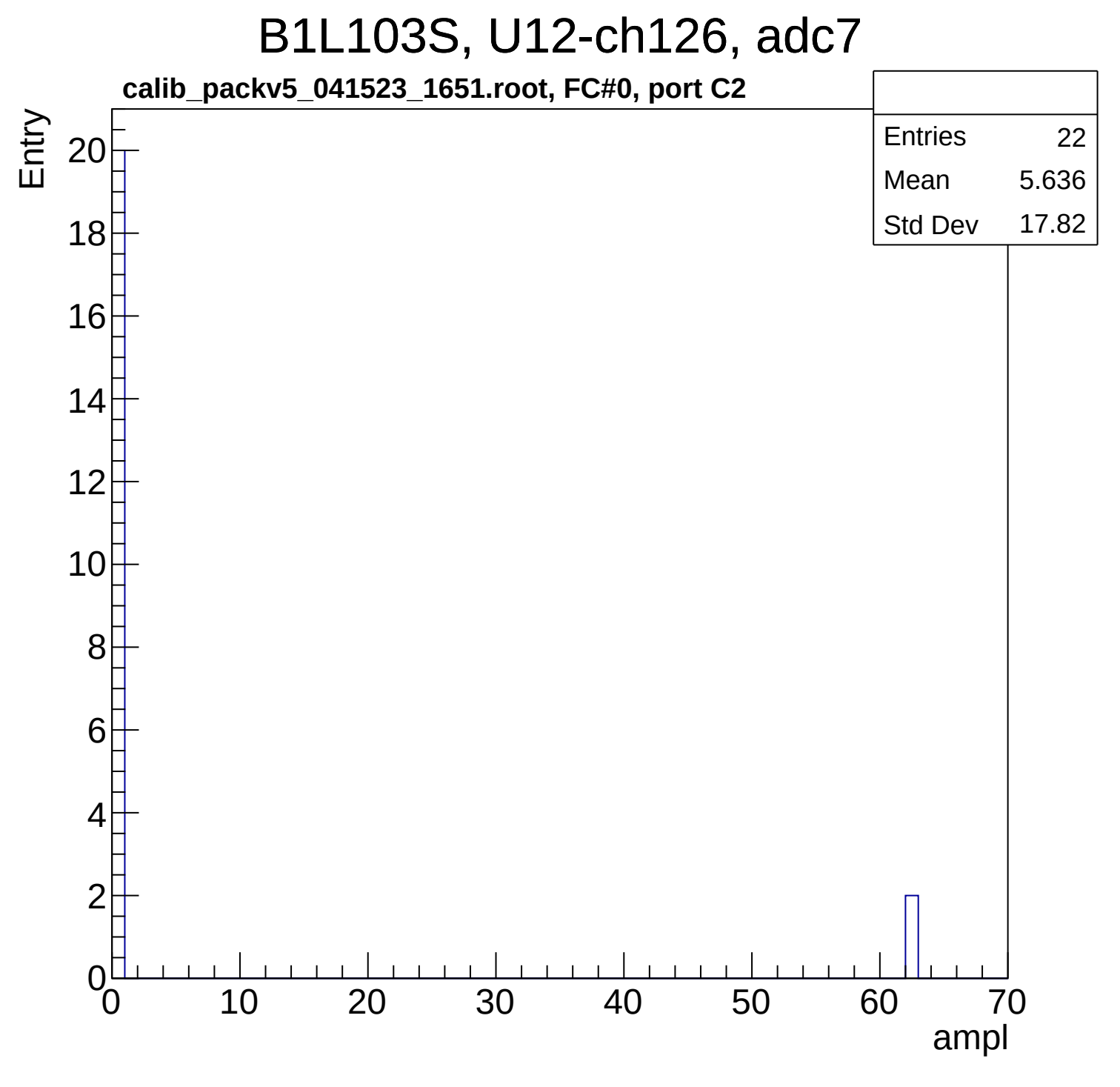
B1L103S, U12-ch126, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 22
Mean 5.636
Std Dev 17.82
Entry
ampl
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6
8
10
12
14
16
18
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0
10
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40
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60
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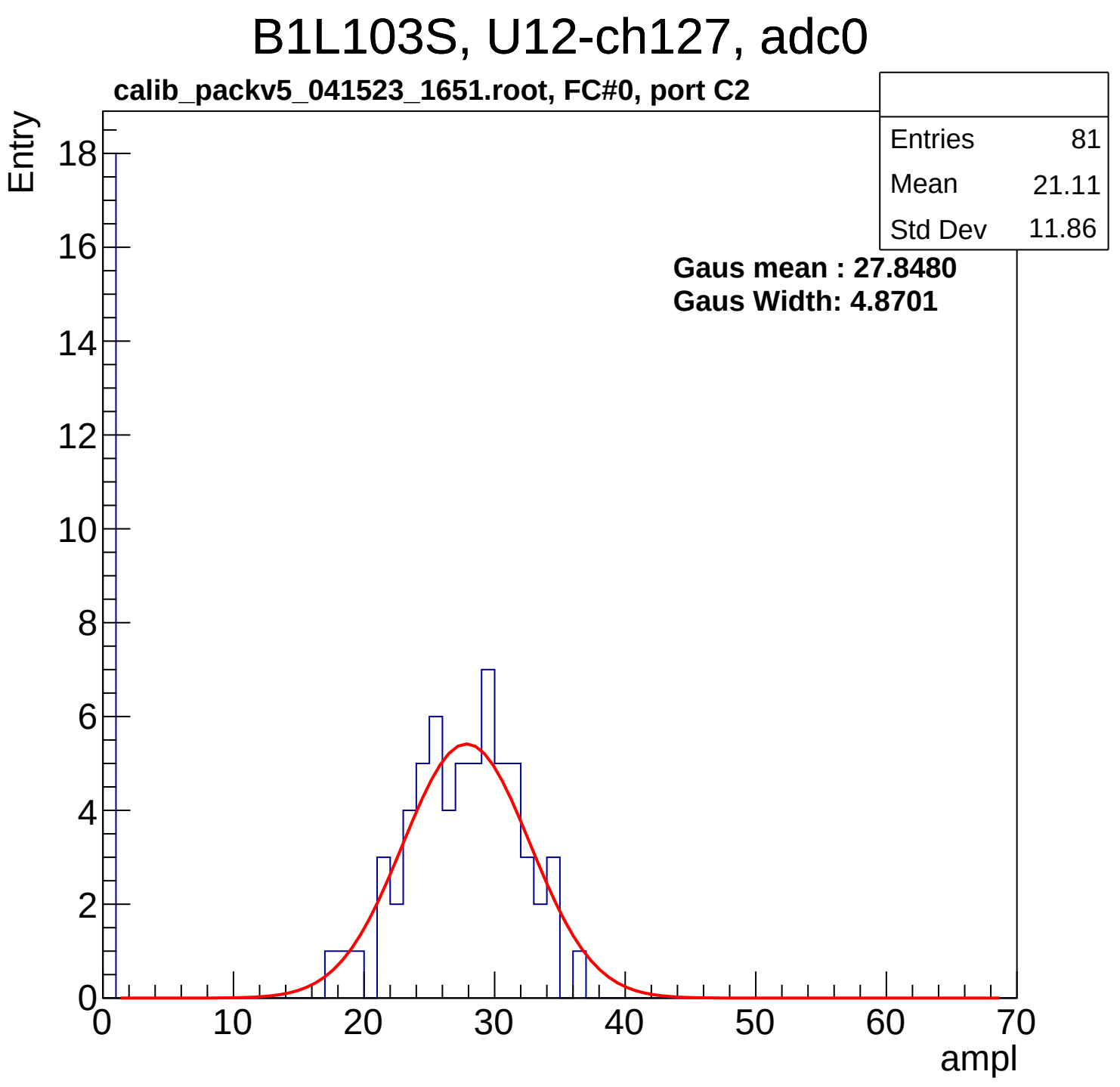
B1L103S, U12-ch127, adc0
calib_packv5_041523_1651.root, FC#0, port C2
Entries 81
Mean 21.11
Std Dev 11.86
Gaus mean : 27.8480
Gaus Width: 4.8701
Entry
ampl
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4
6
8
10
12
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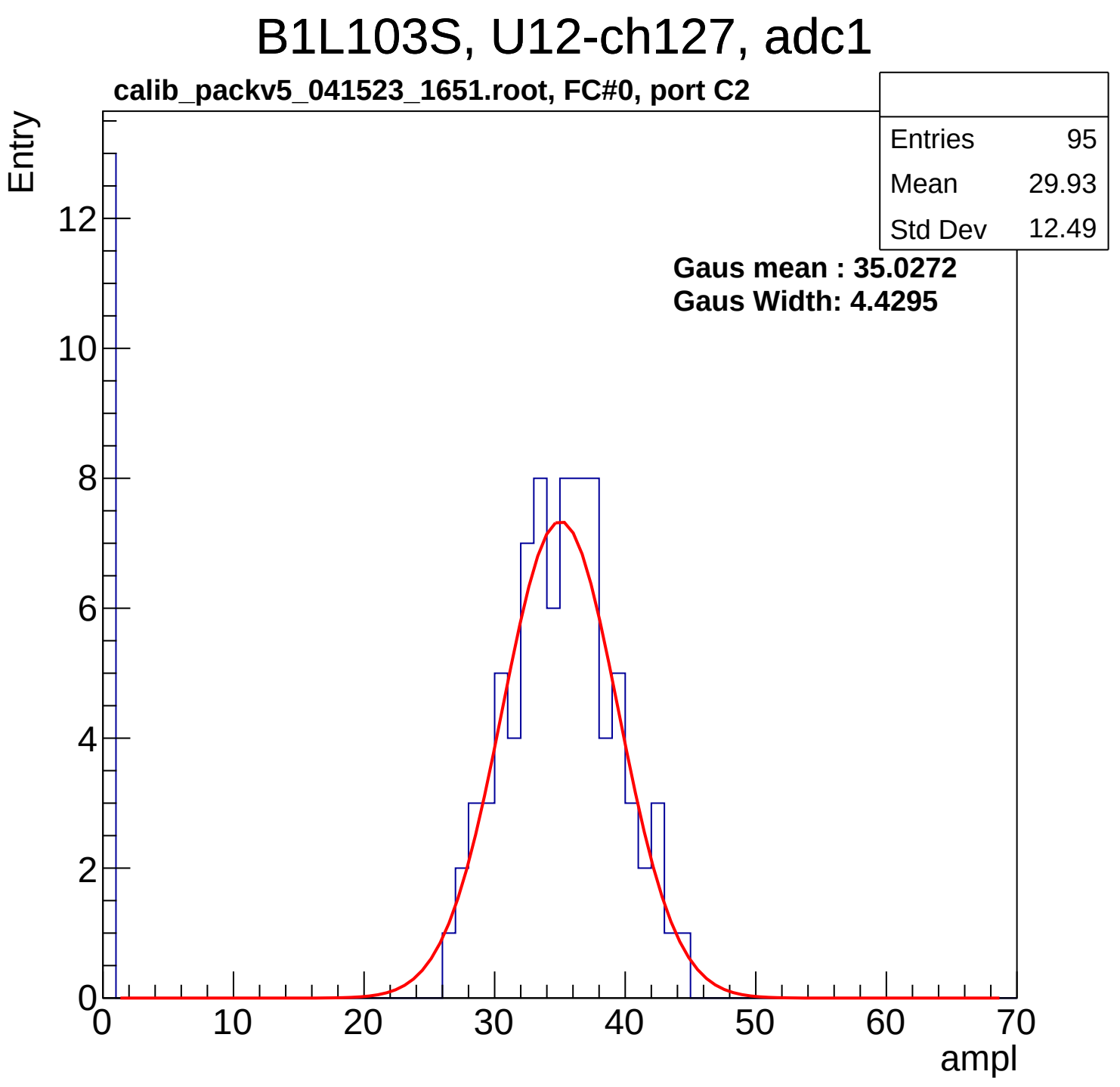
B1L103S, U12-ch127, adc1
calib_packv5_041523_1651.root, FC#0, port C2
Entries 95
Mean 29.93
Std Dev 12.49
Gaus mean : 35.0272
Gaus Width: 4.4295
Entry
ampl
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6
8
10
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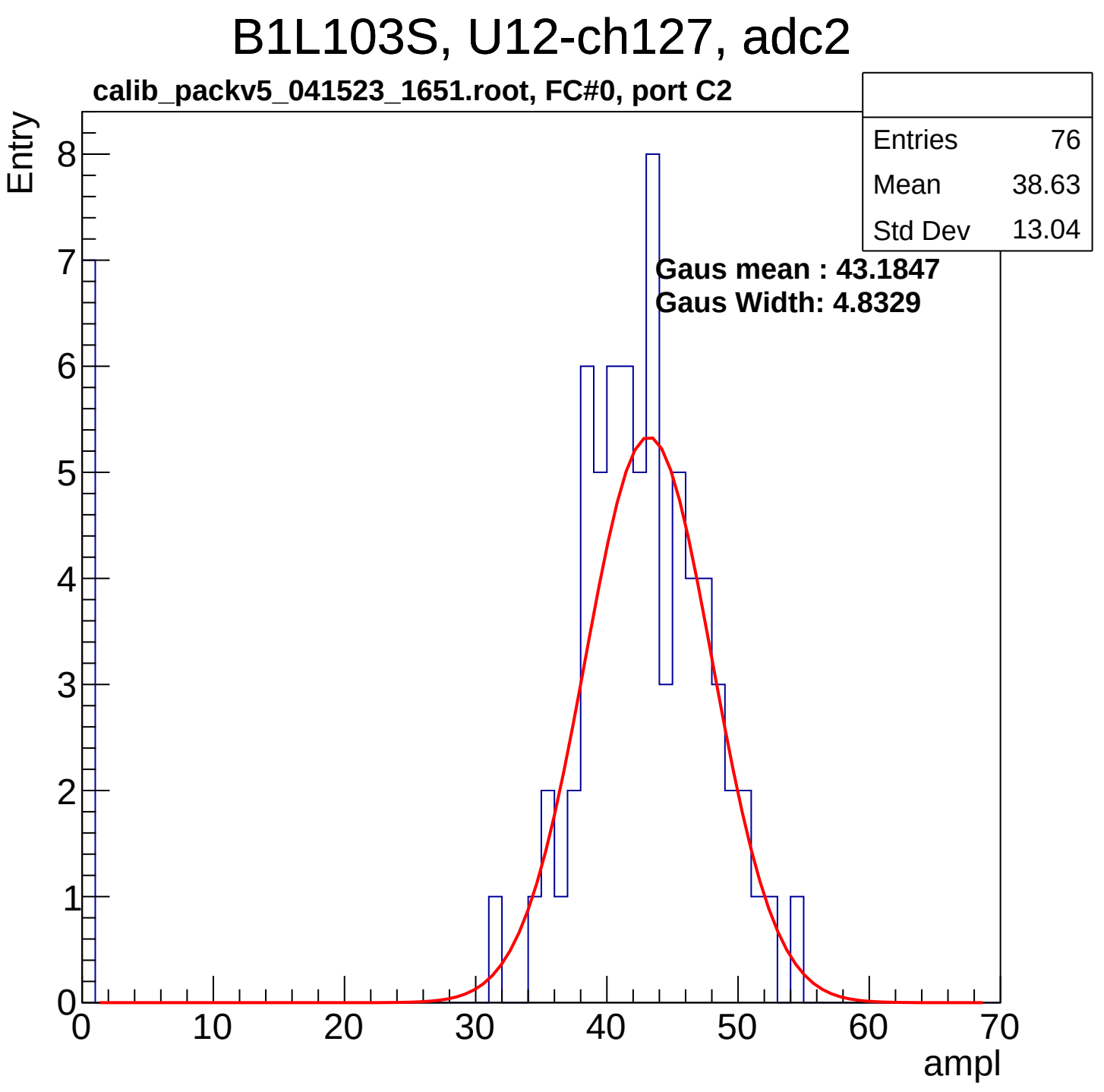
B1L103S, U12-ch127, adc2
calib_packv5_041523_1651.root, FC#0, port C2
Entries 76
Mean 38.63
Std Dev 13.04
Gaus mean : 43.1847
Gaus Width: 4.8329
Entry
ampl
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2
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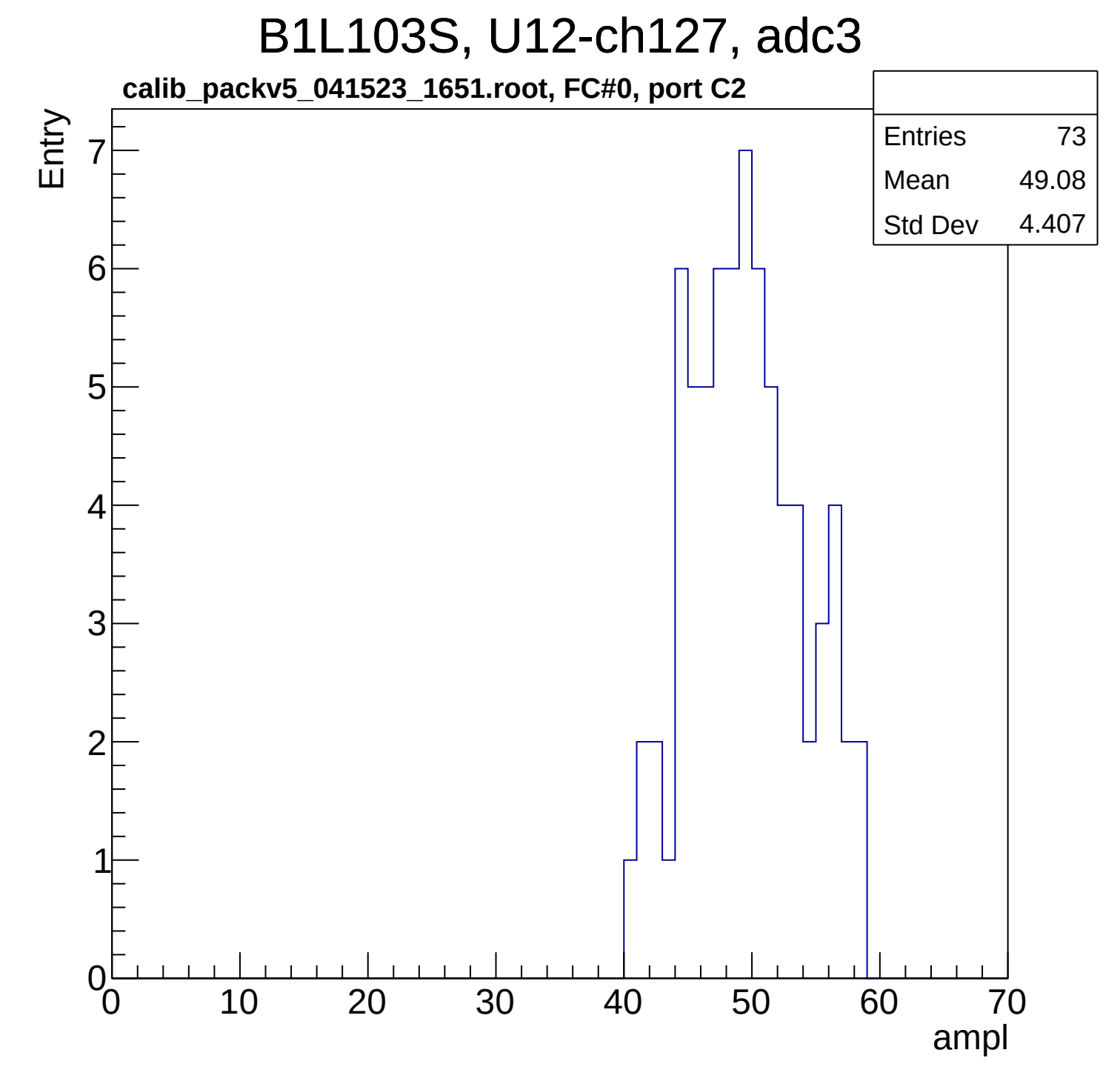
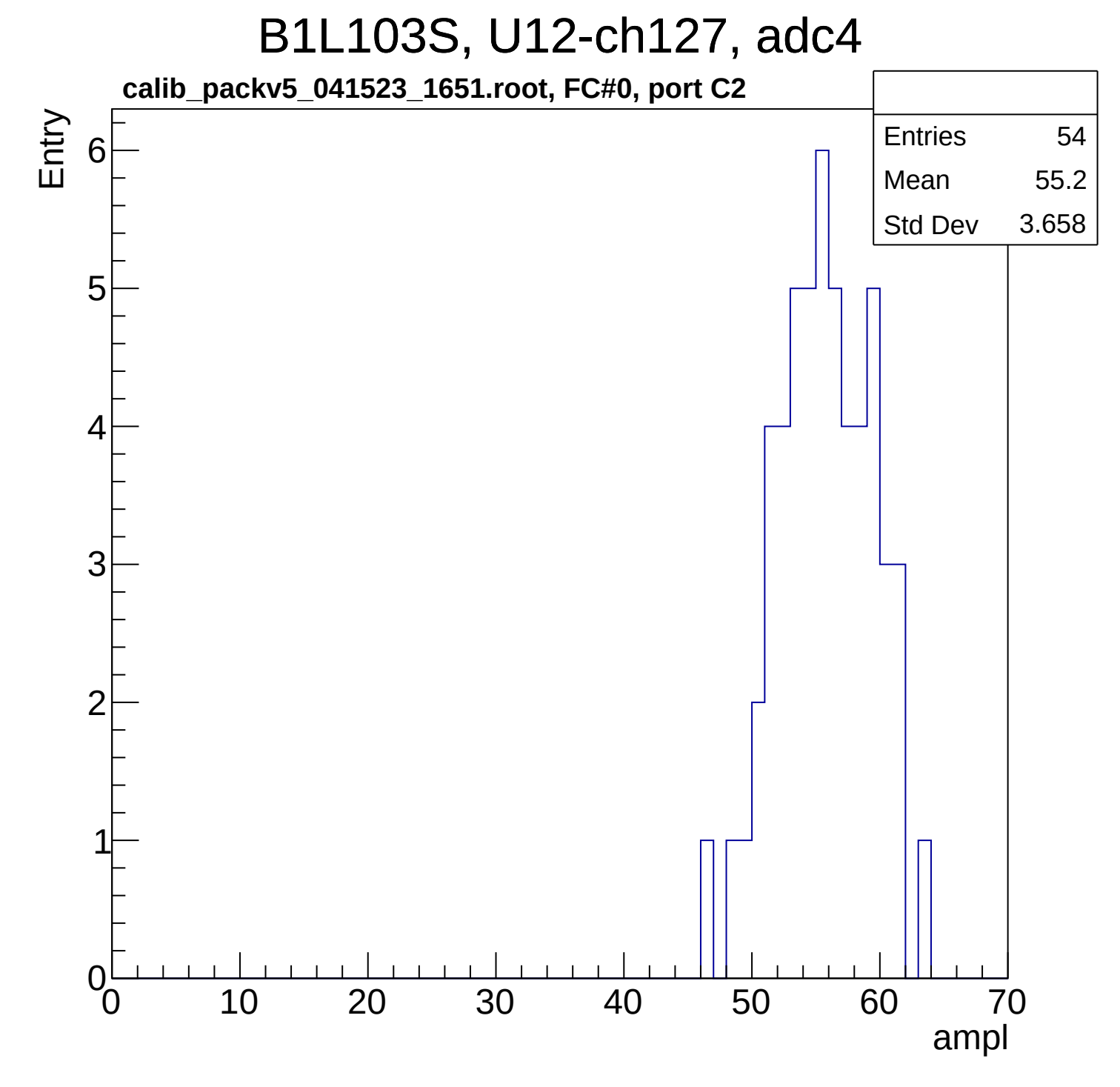
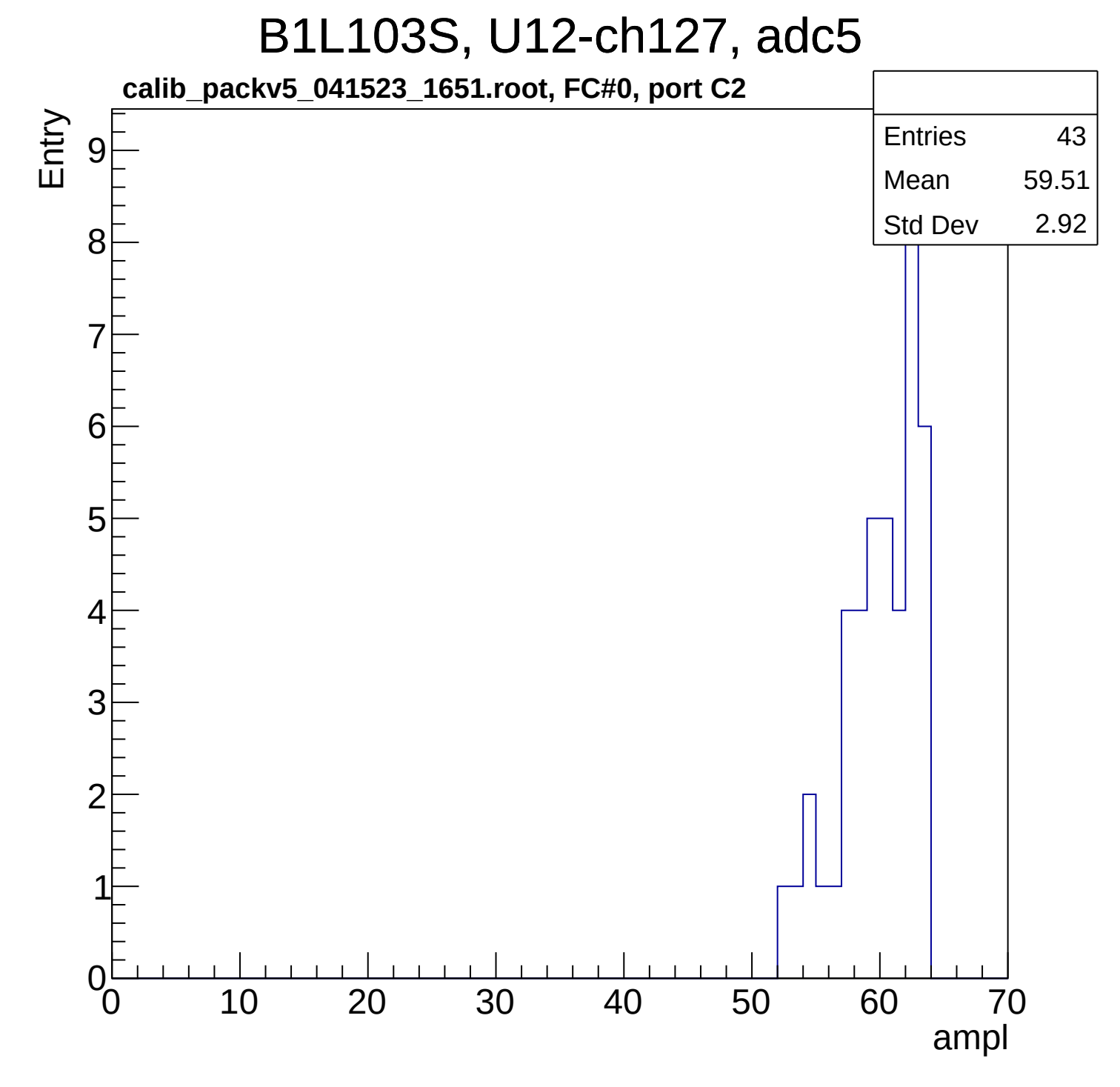
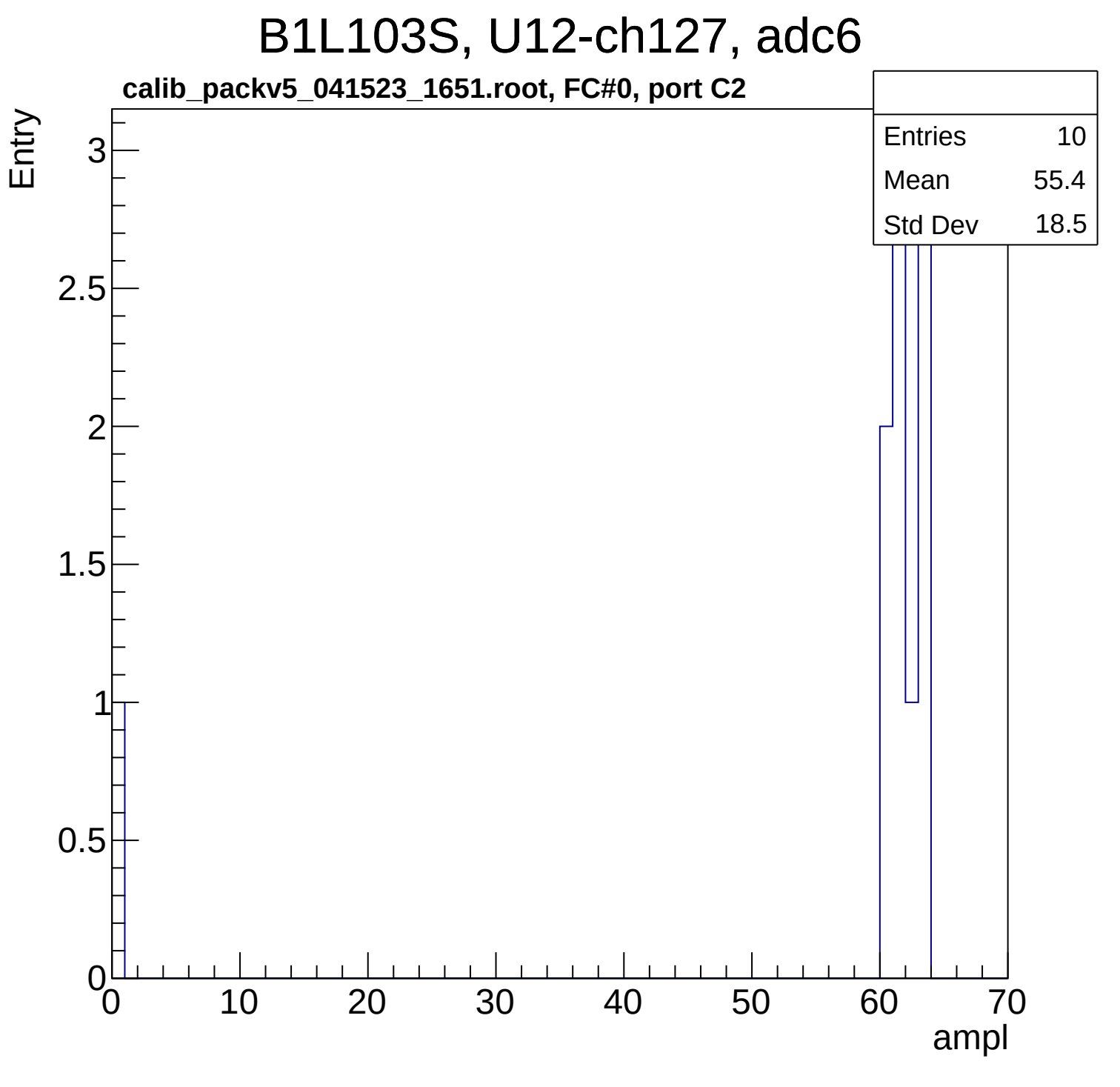
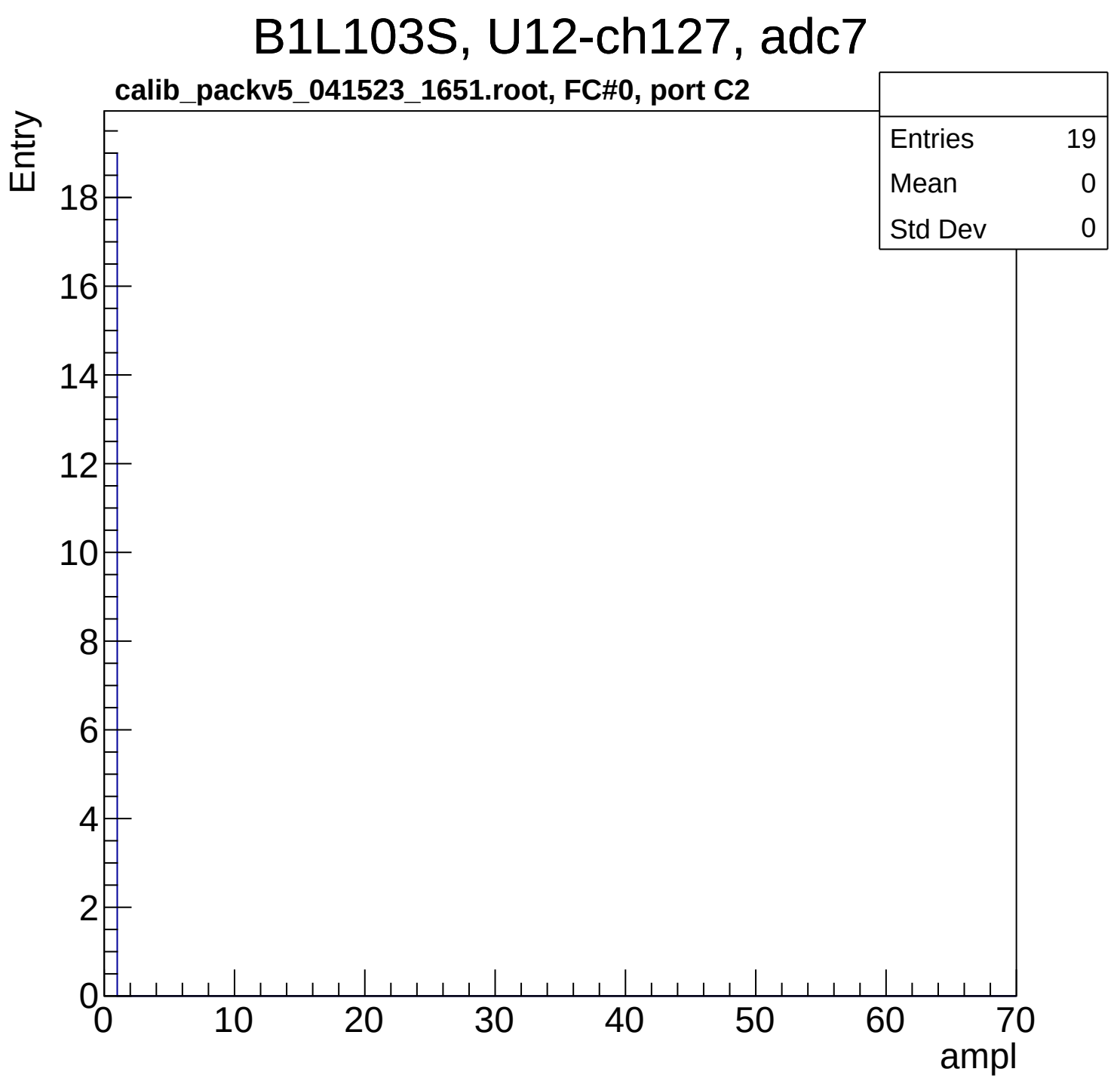
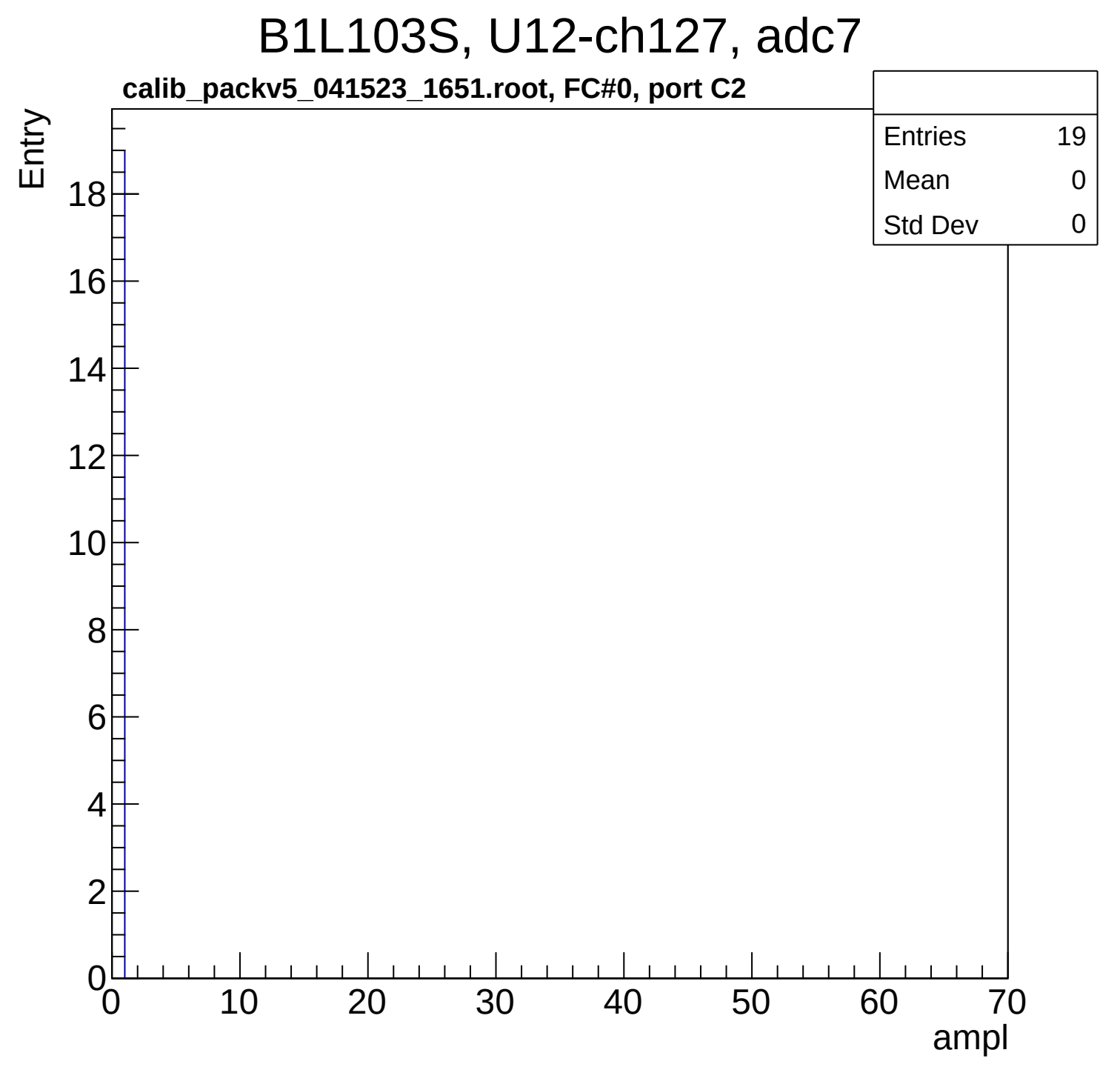

B1L103S, U12-ch127, adc3
calib_packv5_041523_1651.root, FC#0, port C2
Entries 73
Mean 49.08
Std Dev 4.407
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L103S, U12-ch127, adc4
calib_packv5_041523_1651.root, FC#0, port C2
Entries 54
Mean 55.2
Std Dev 3.658
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L103S, U12-ch127, adc5
calib_packv5_041523_1651.root, FC#0, port C2
Entries 43
Mean 59.51
Std Dev 2.92
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L103S, U12-ch127, adc6
calib_packv5_041523_1651.root, FC#0, port C2
Entries 10
Mean 55.4
Std Dev 18.5
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70


B1L103S, U12-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl


B1L103S, U12-ch127, adc7
calib_packv5_041523_1651.root, FC#0, port C2
Entries 19
Mean 0
Std Dev 0
Entry
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40
50
60
70
ampl