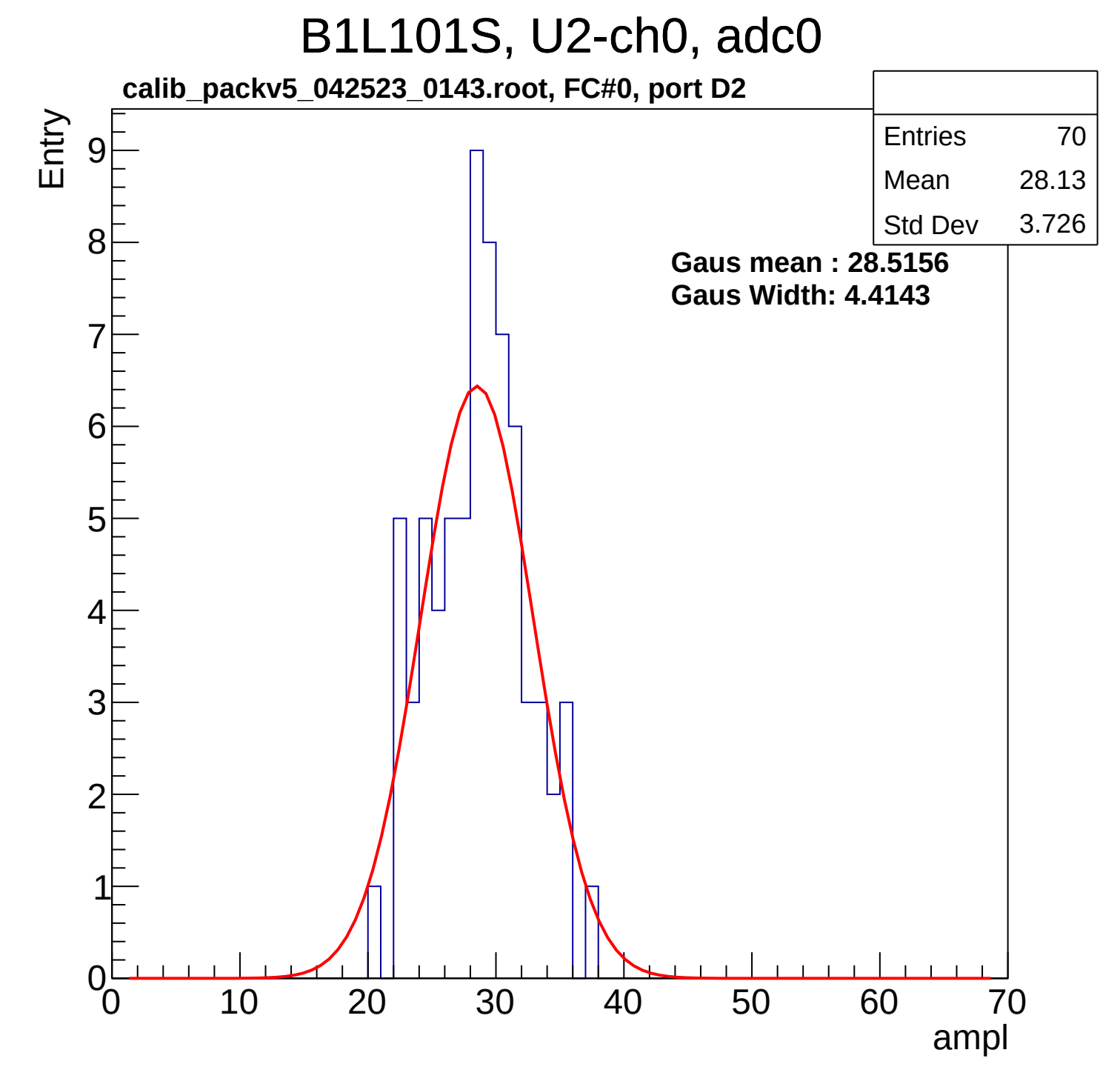
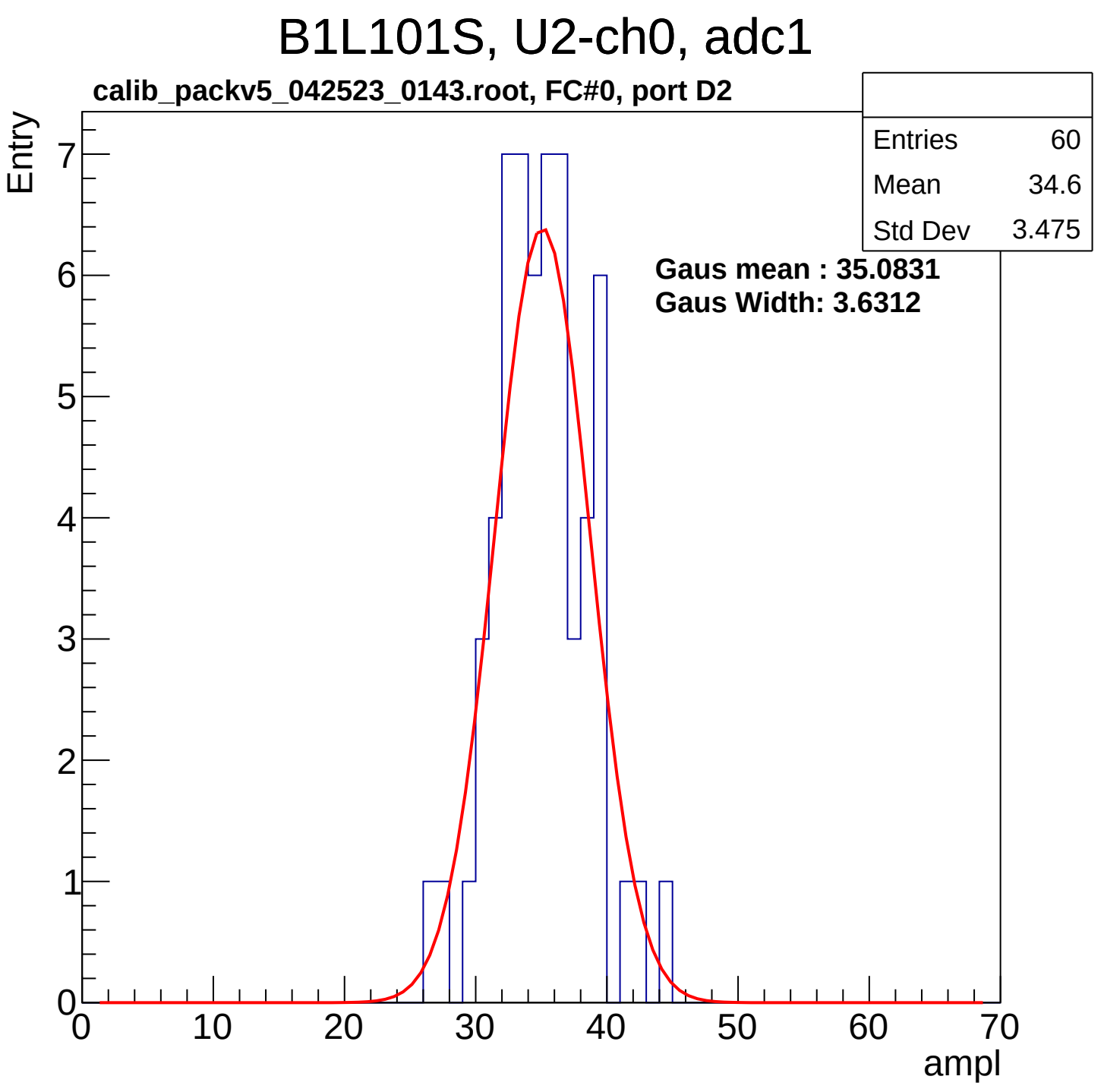
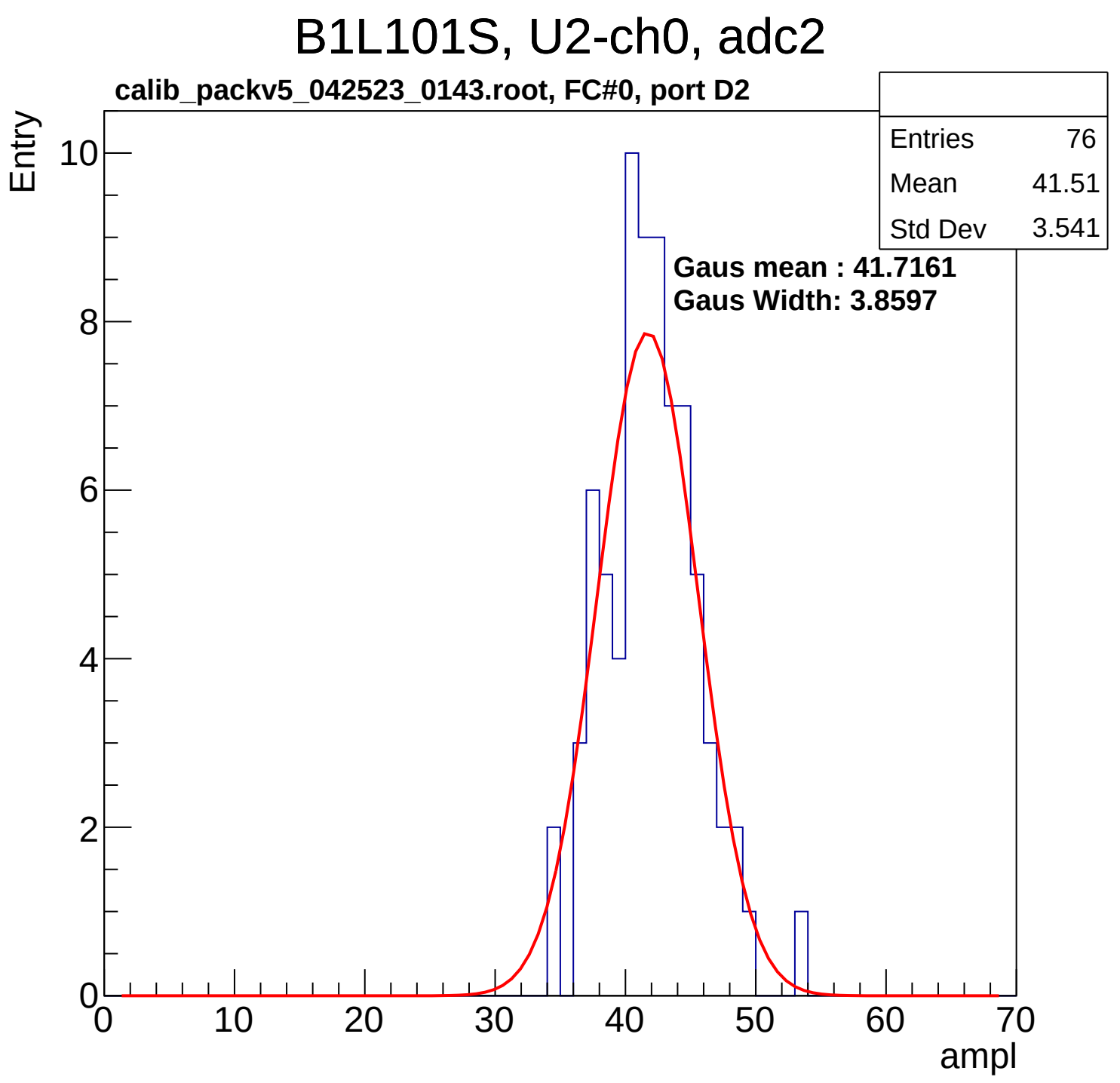
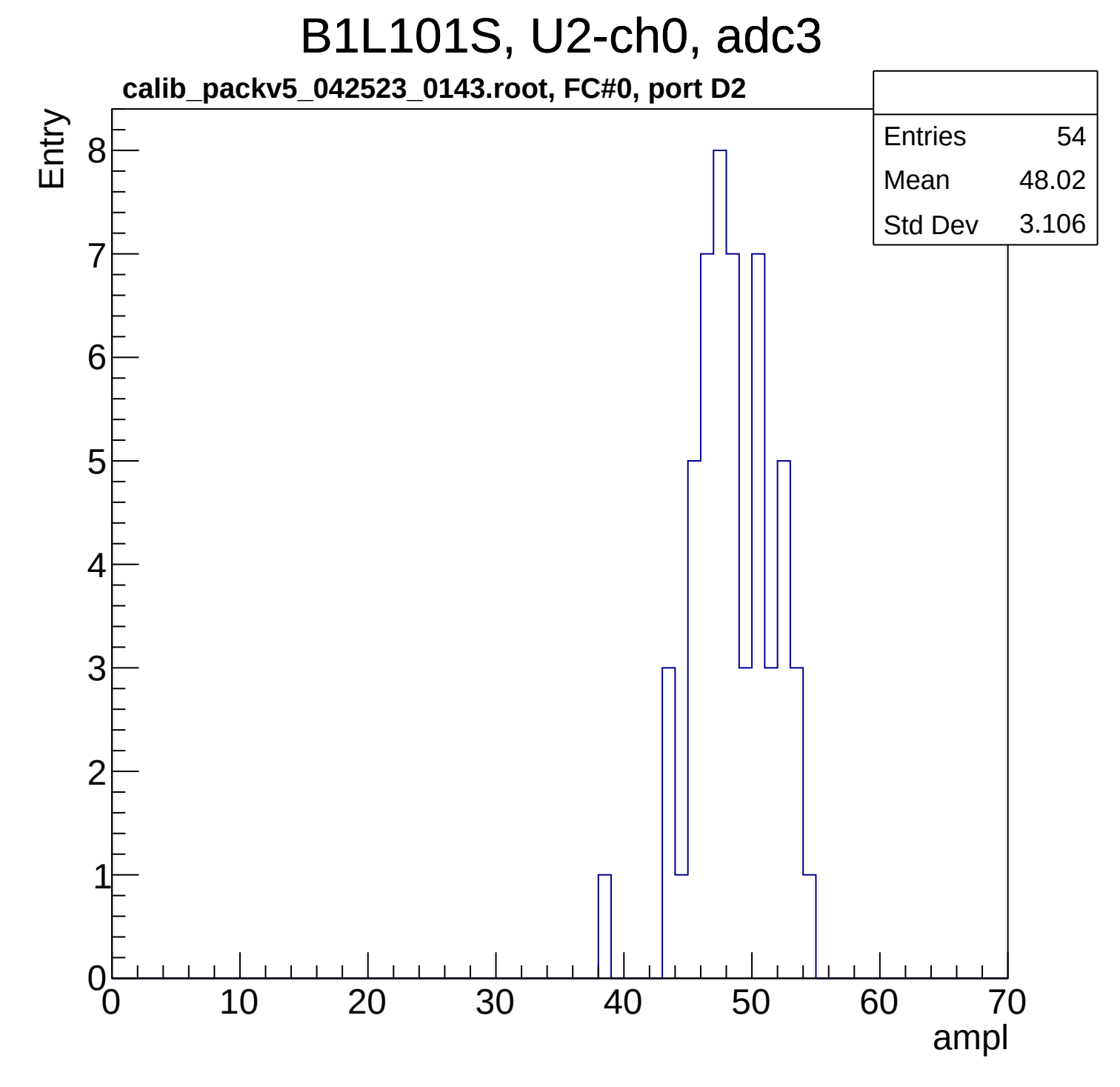
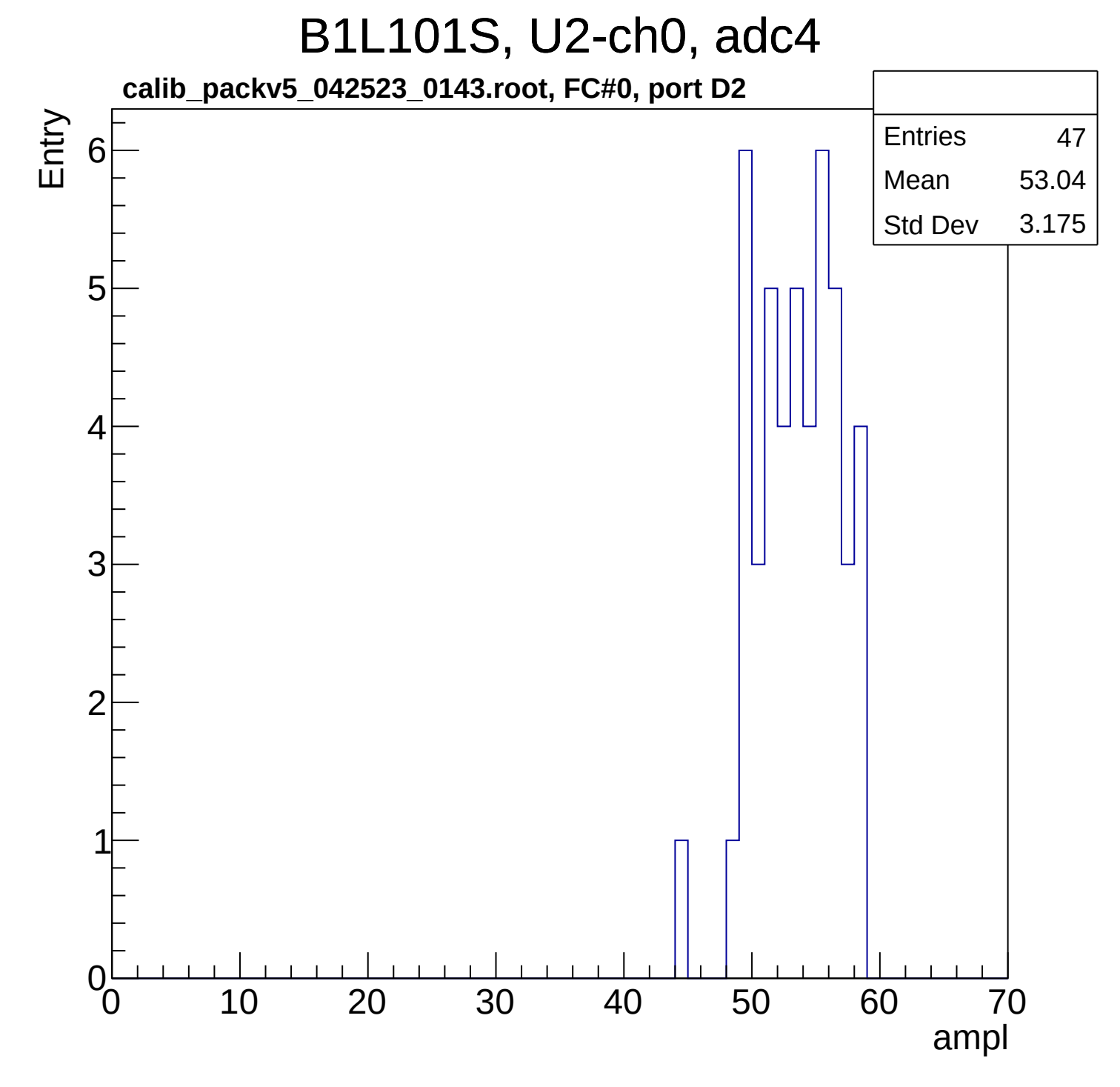
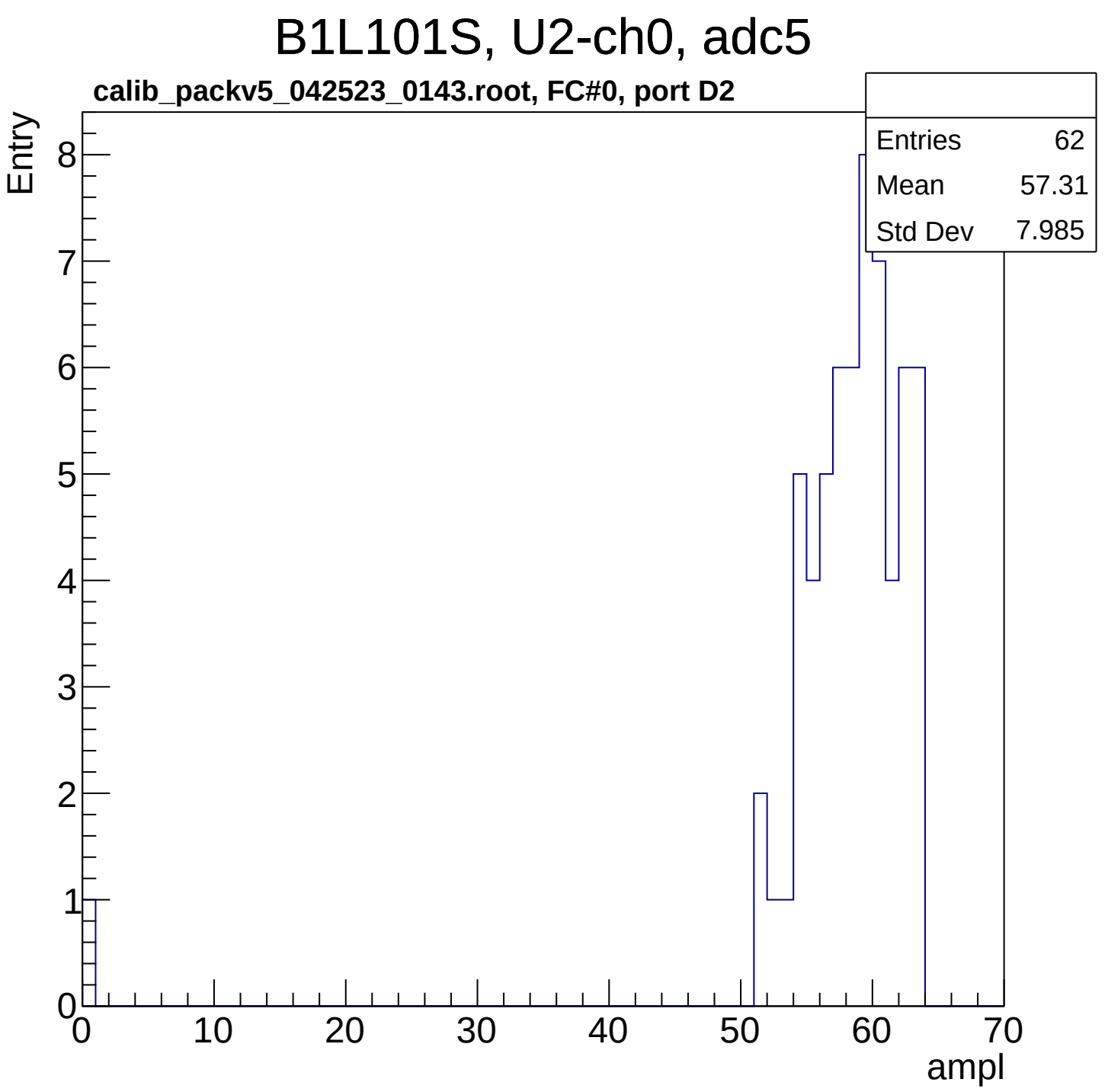

B1L101S, U2-ch0, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 28.13
Std Dev 3.726
Gaus mean : 28.5156
Gaus Width: 4.4143
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

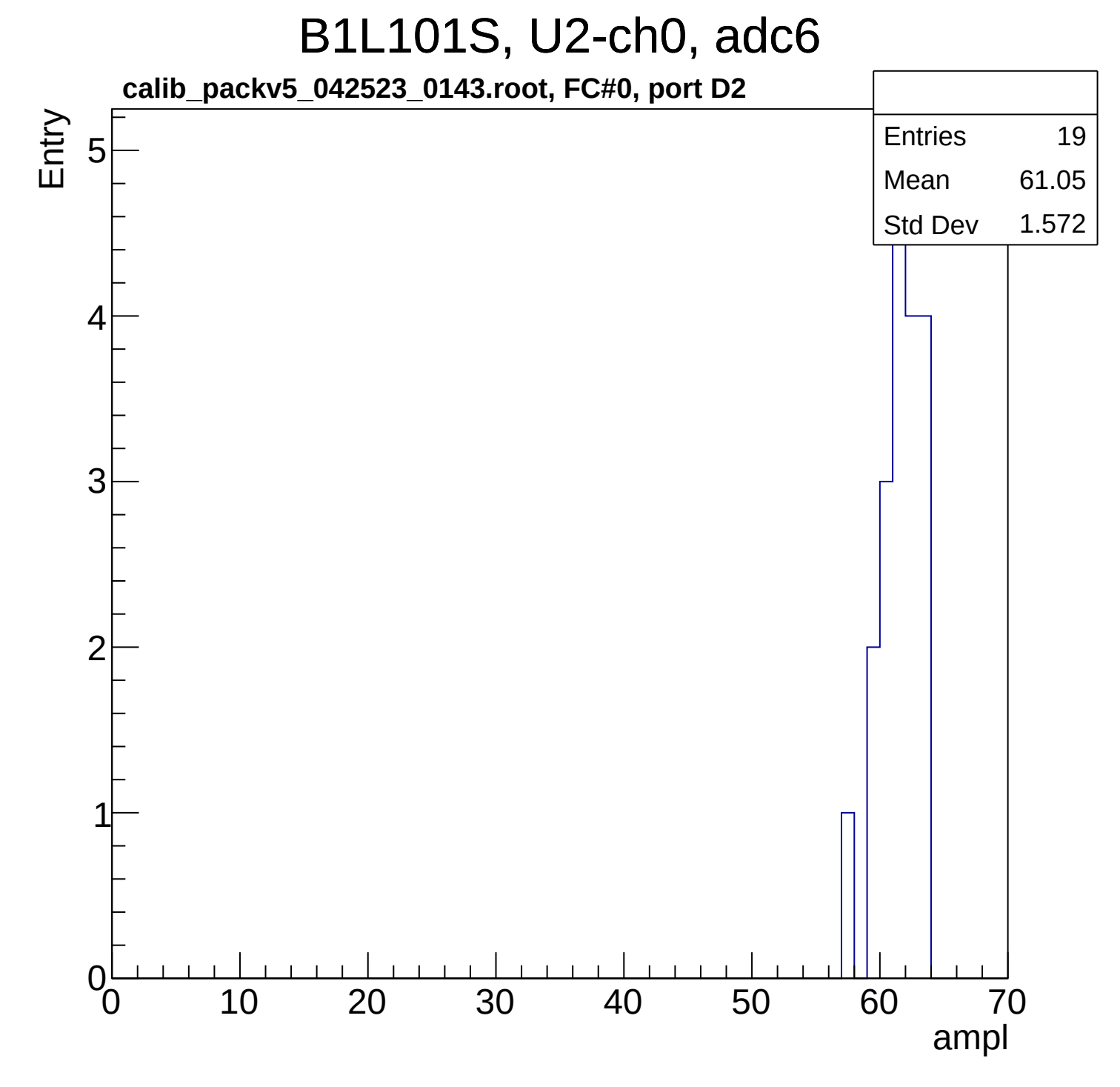

B1L101S, U2-ch0, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 34.6
Std Dev 3.475
Gaus mean : 35.0831
Gaus Width: 3.6312
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

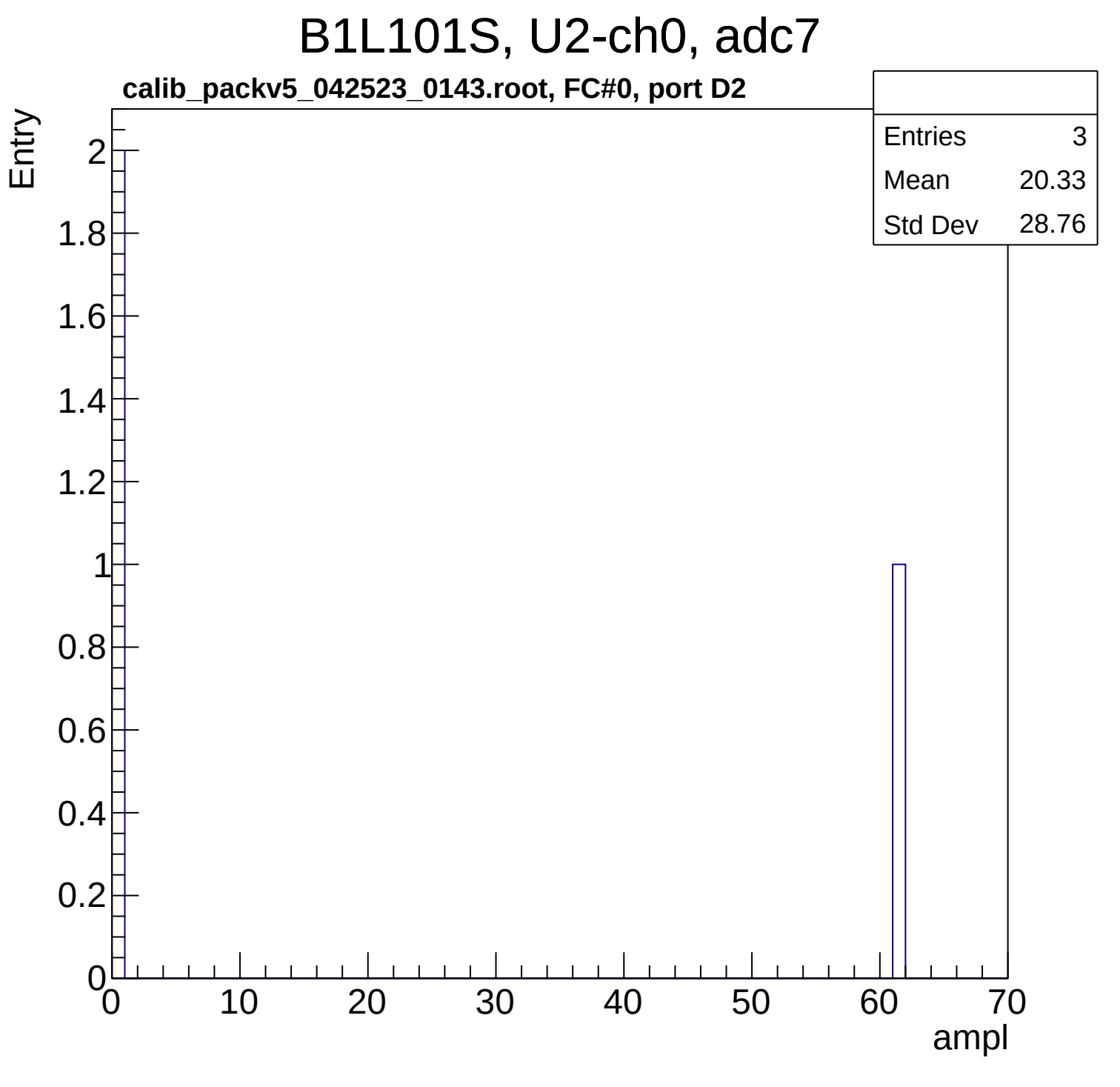

B1L101S, U2-ch0, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 41.51
Std Dev 3.541
Gaus mean : 41.7161
Gaus Width: 3.8597
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

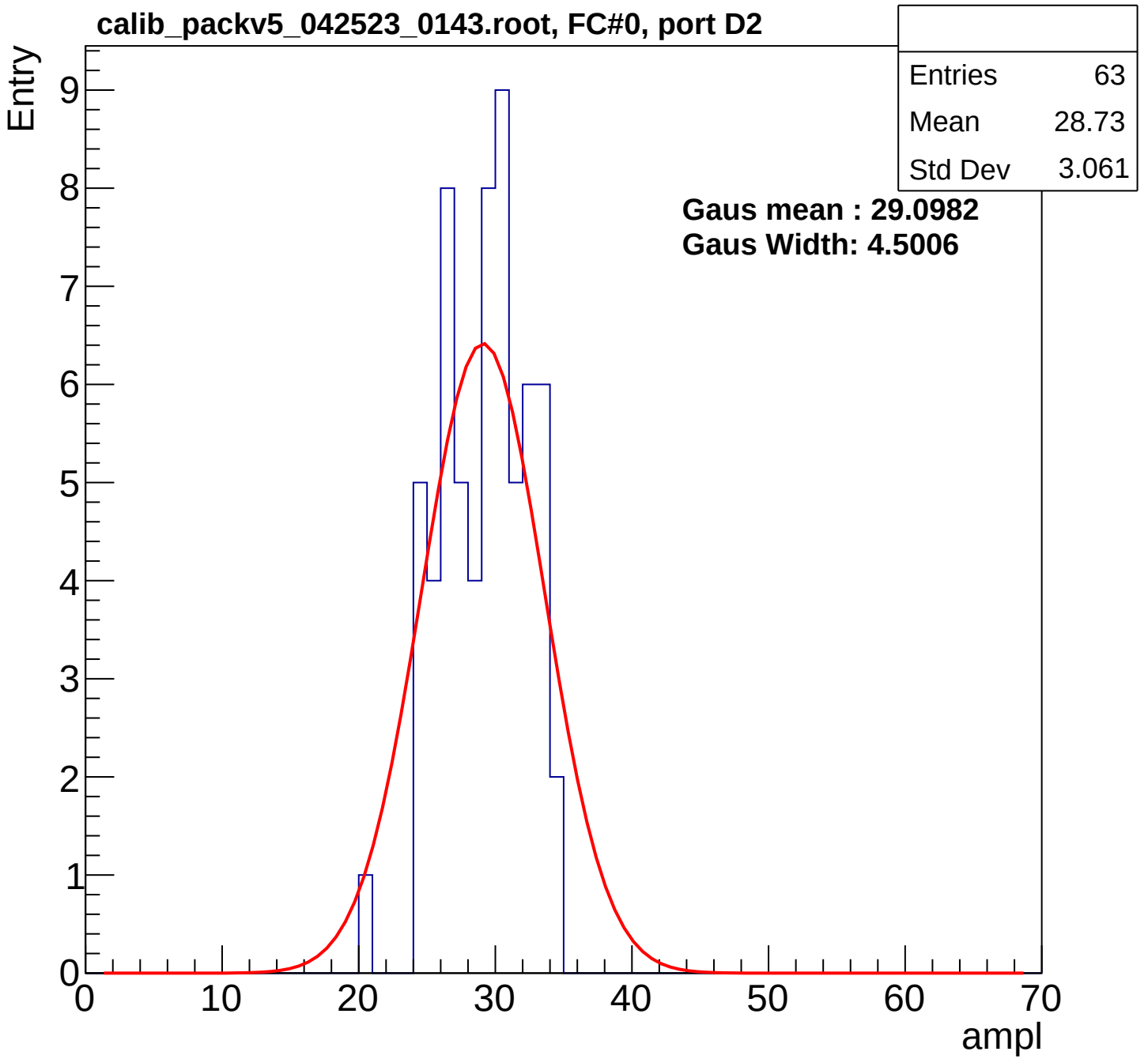

B1L101S, U2-ch0, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 48.02
Std Dev 3.106
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

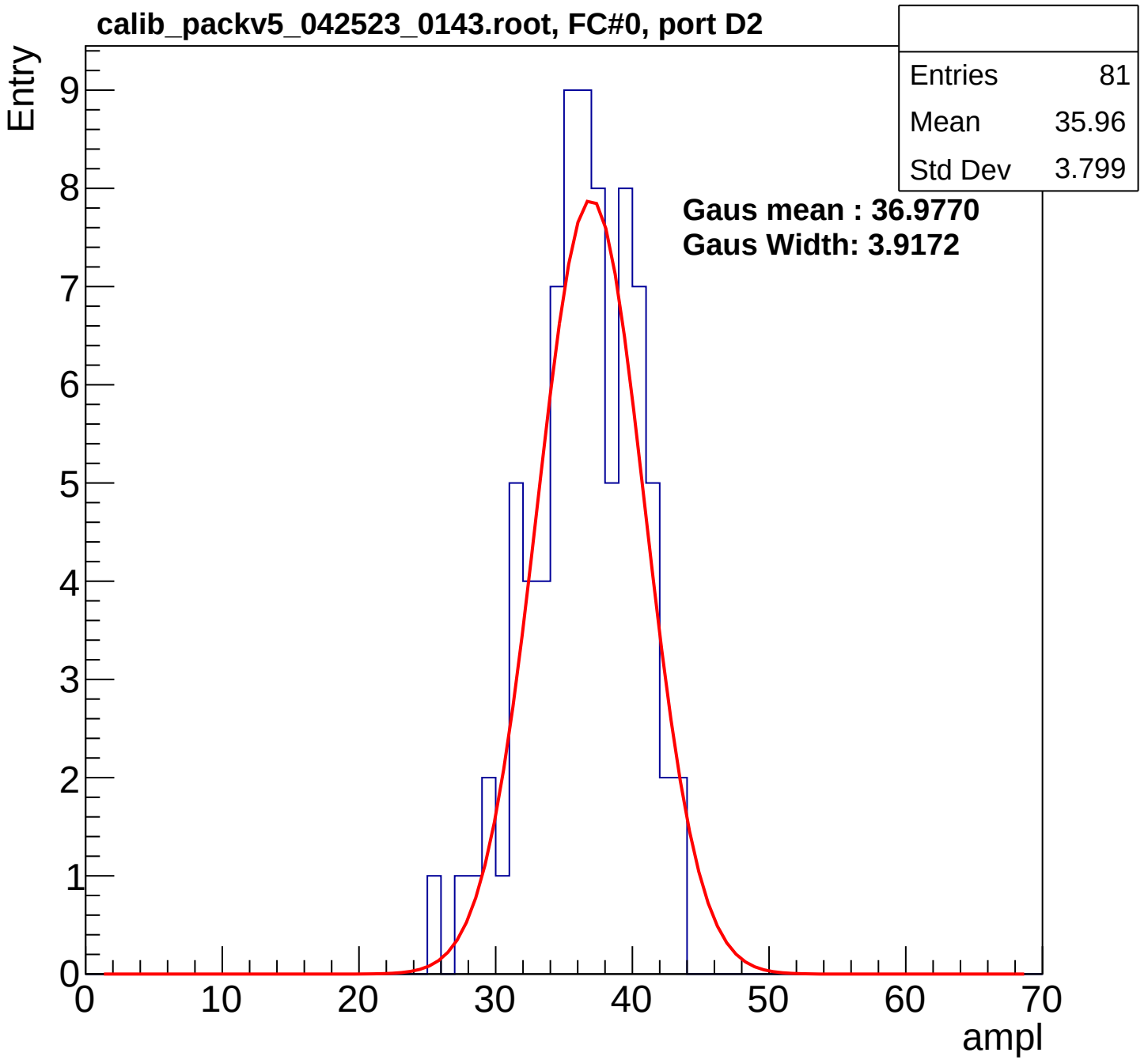

B1L101S, U2-ch0, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 53.04
Std Dev 3.175
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

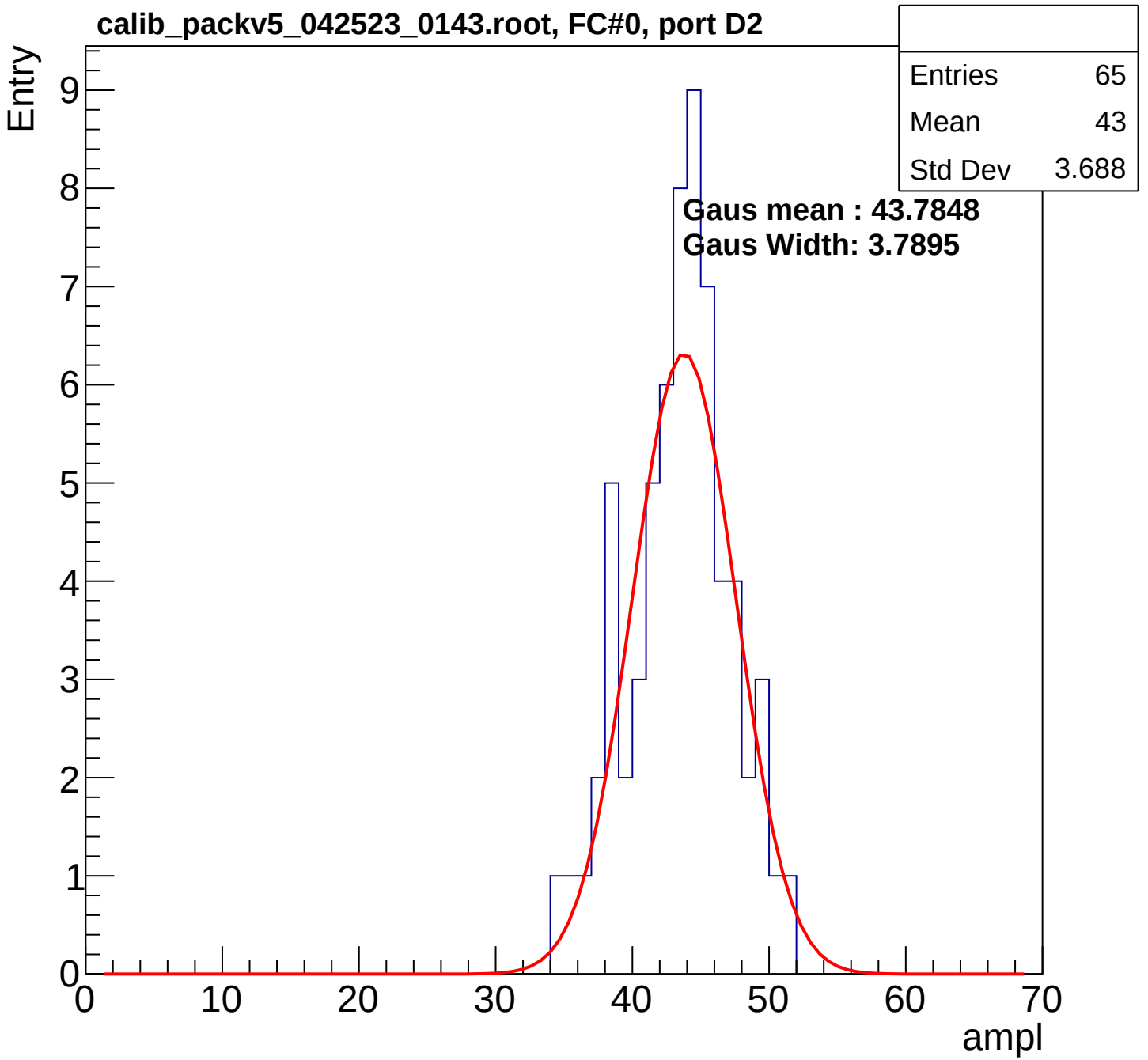

B1L101S, U2-ch0, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 57.31
Std Dev 7.985
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

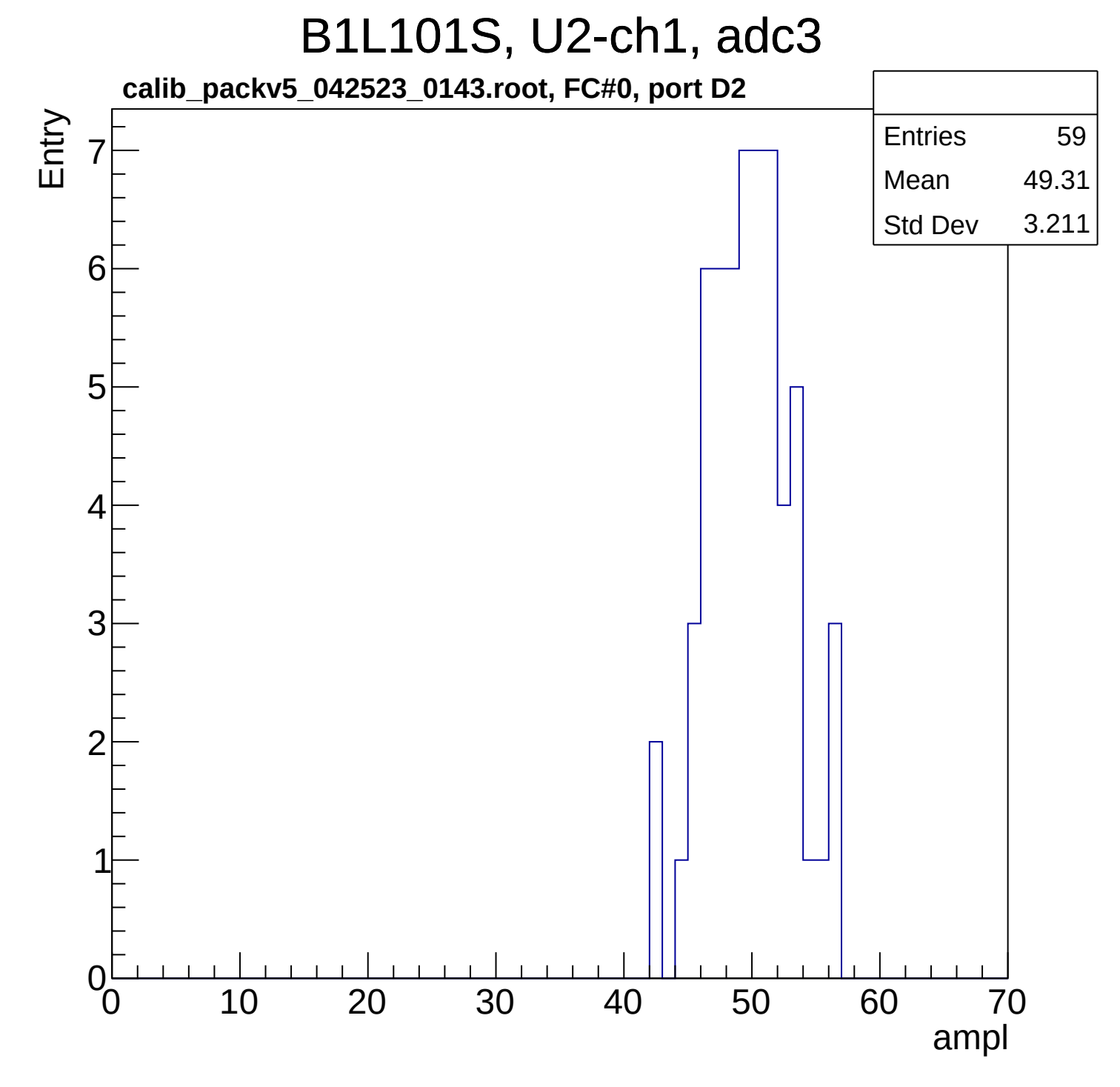

B1L101S, U2-ch0, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 19
Mean 61.05
Std Dev 1.572
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

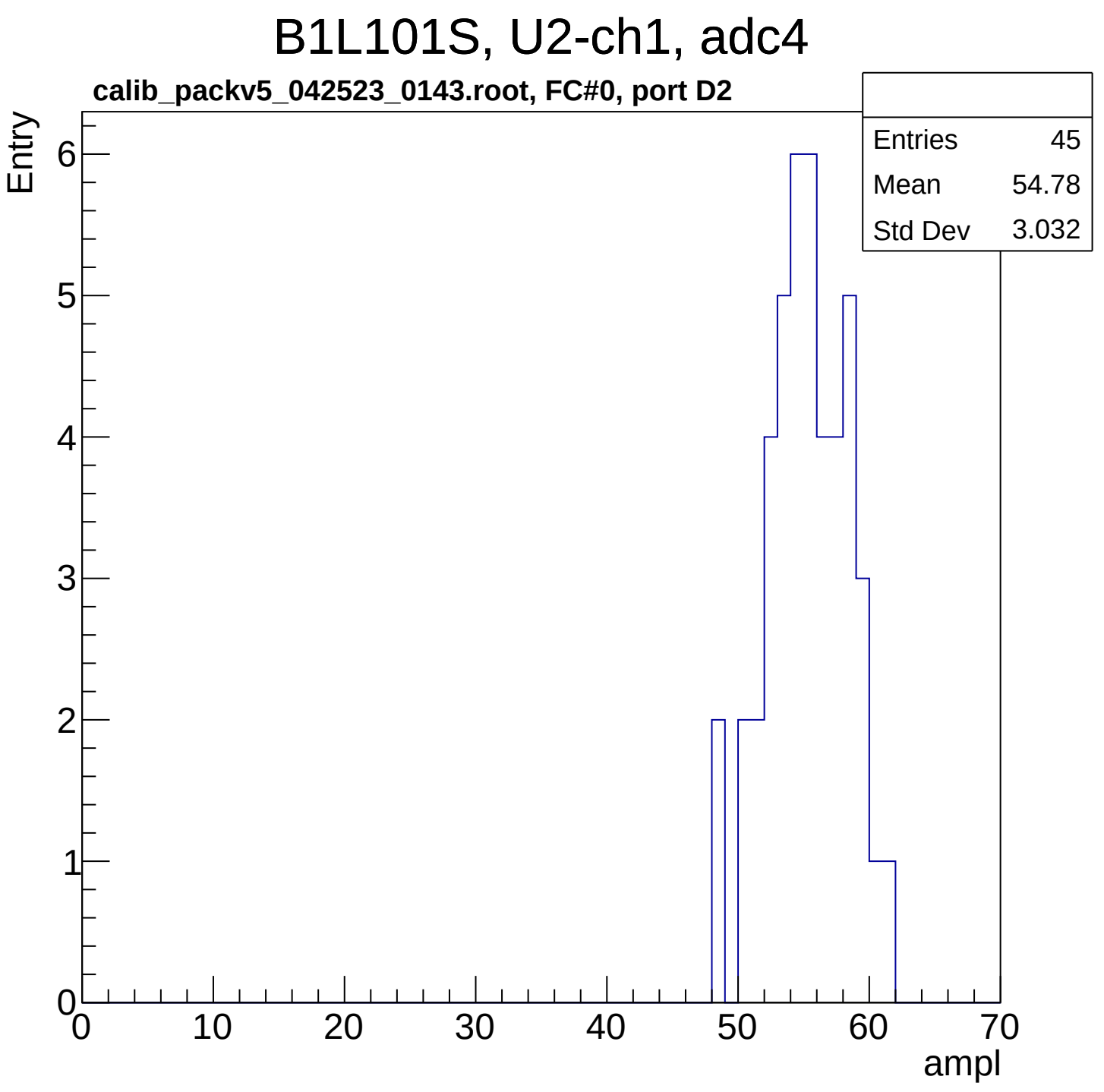

B1L101S, U2-ch0, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 20.33
Std Dev 28.76
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

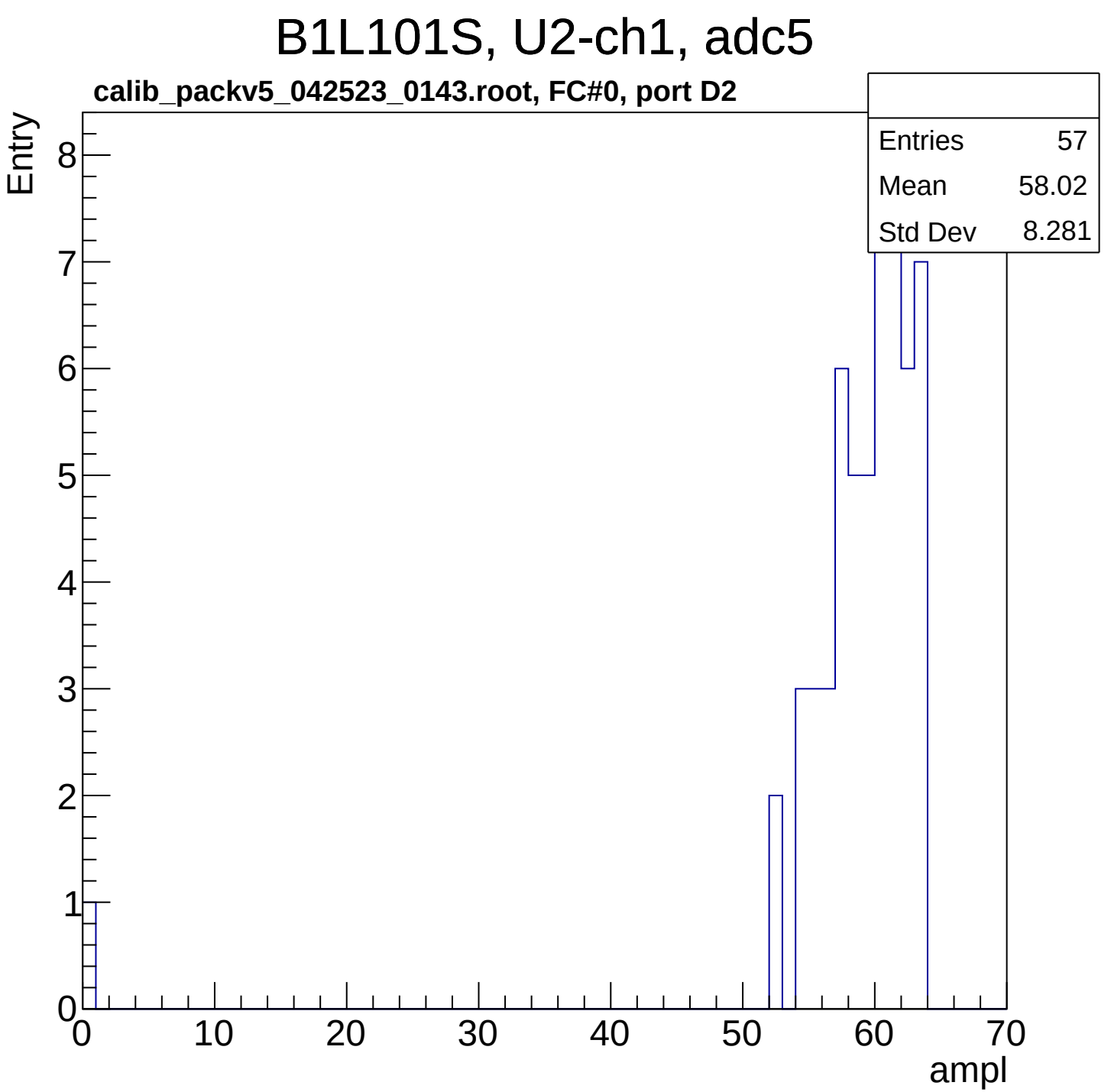

B1L101S, U2-ch1, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 28.73
Std Dev 3.061
Gaus mean : 29.0982
Gaus Width: 4.5006
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

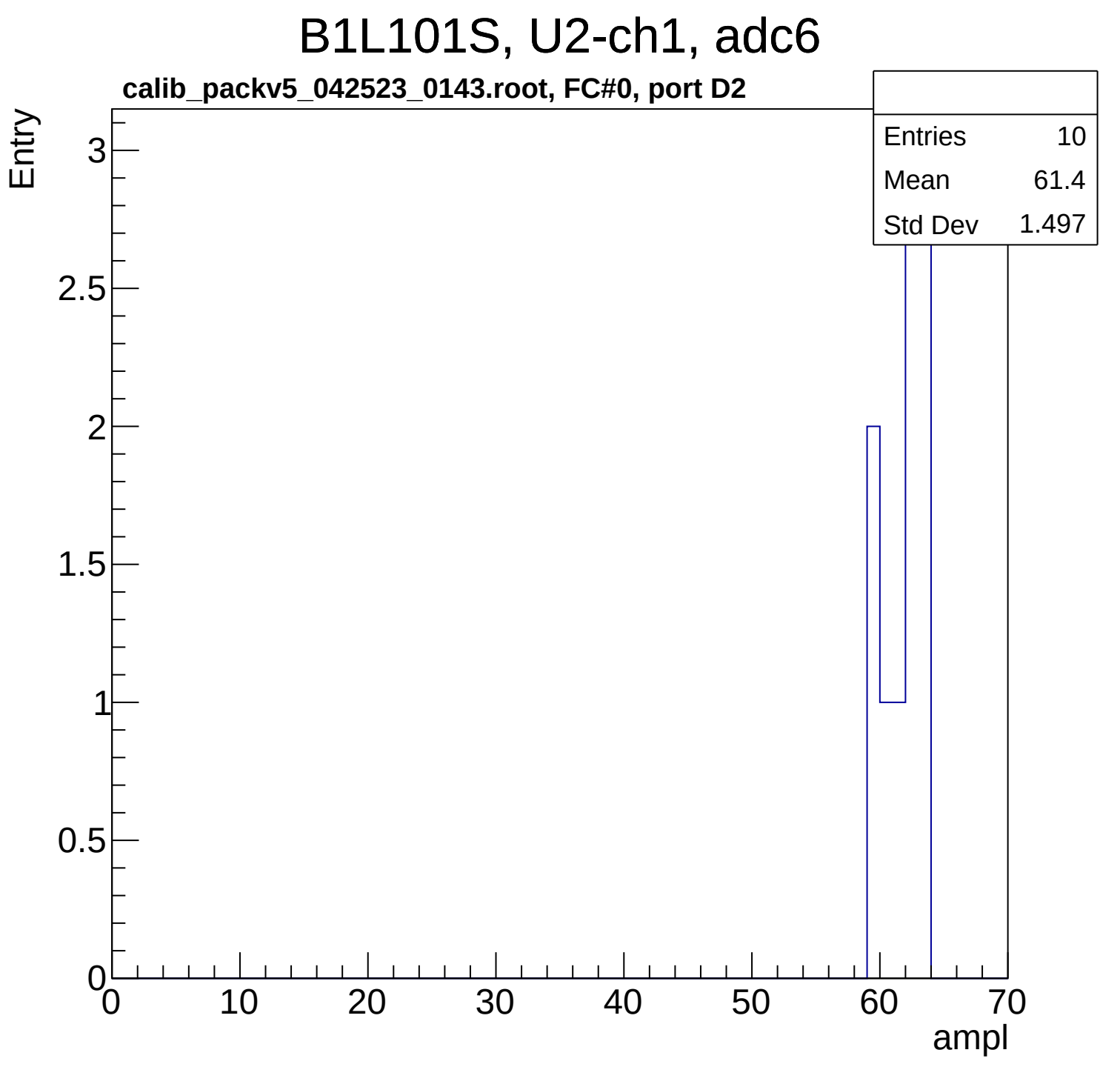

B1L101S, U2-ch1, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 81
Mean 35.96
Std Dev 3.799
Gaus mean : 36.9770
Gaus Width: 3.9172
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

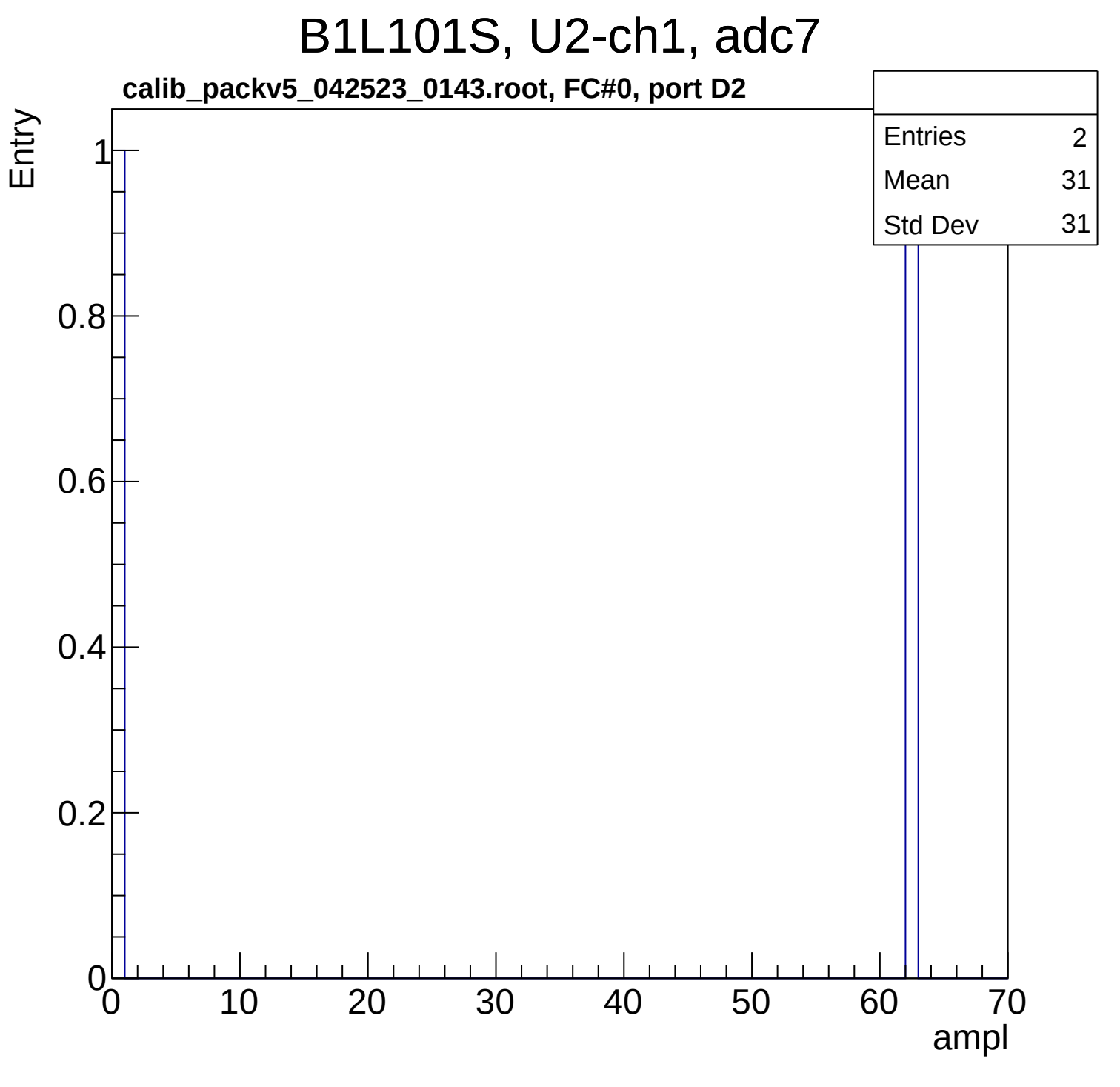

B1L101S, U2-ch1, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 43
Std Dev 3.688
Gaus mean : 43.7848
Gaus Width: 3.7895
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

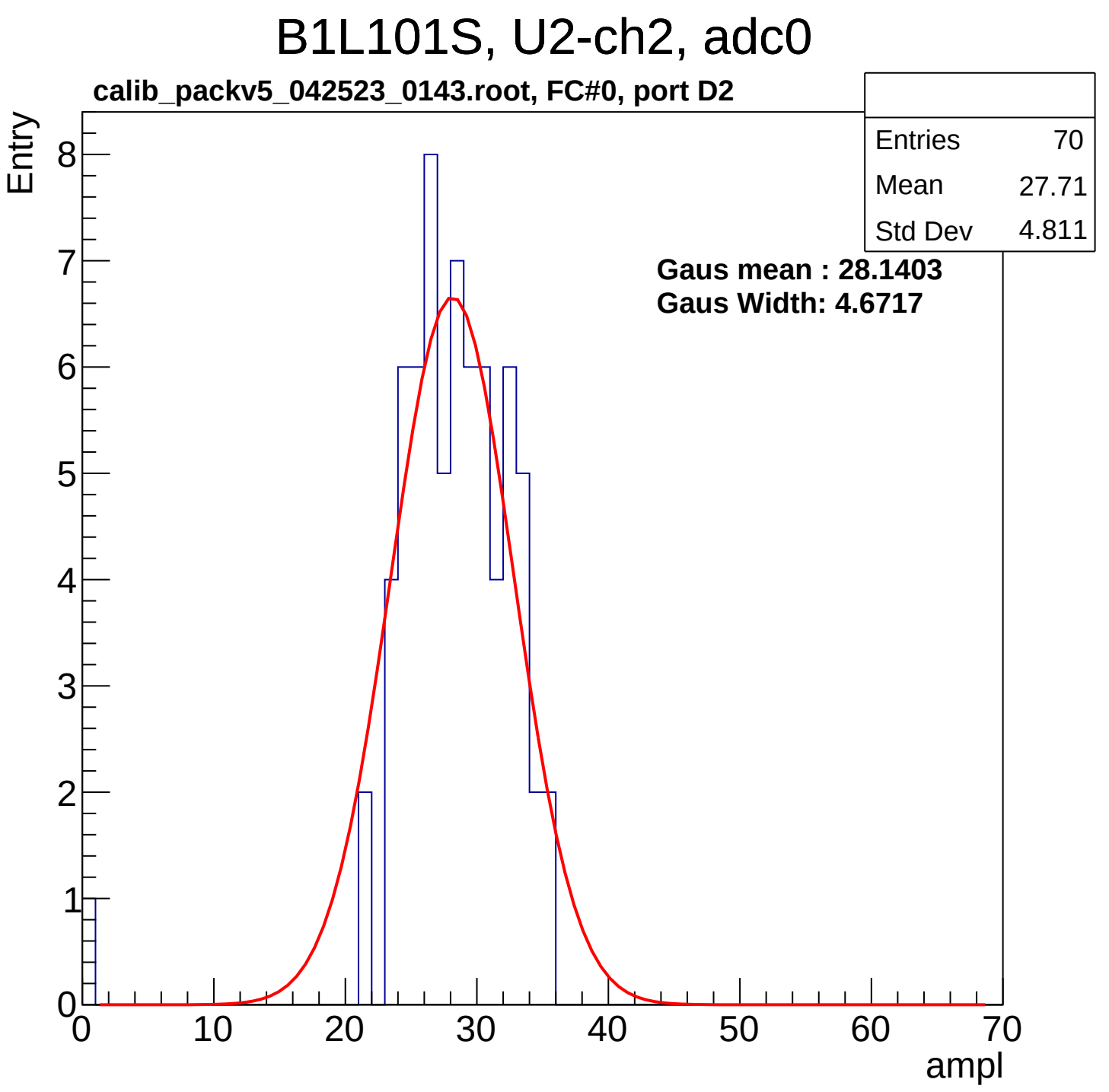

B1L101S, U2-ch1, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 49.31
Std Dev 3.211
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

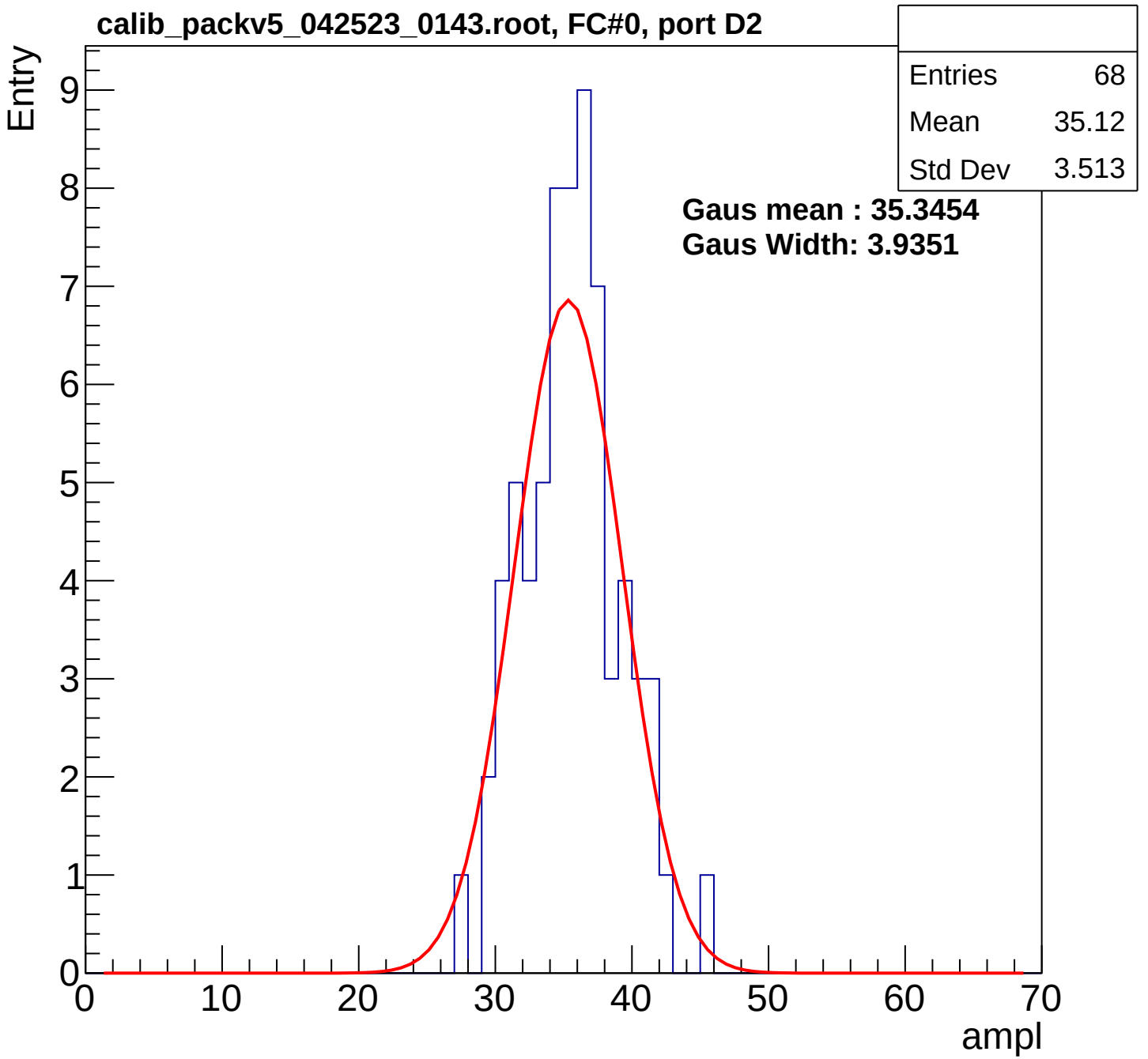

B1L101S, U2-ch1, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 54.78
Std Dev 3.032
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

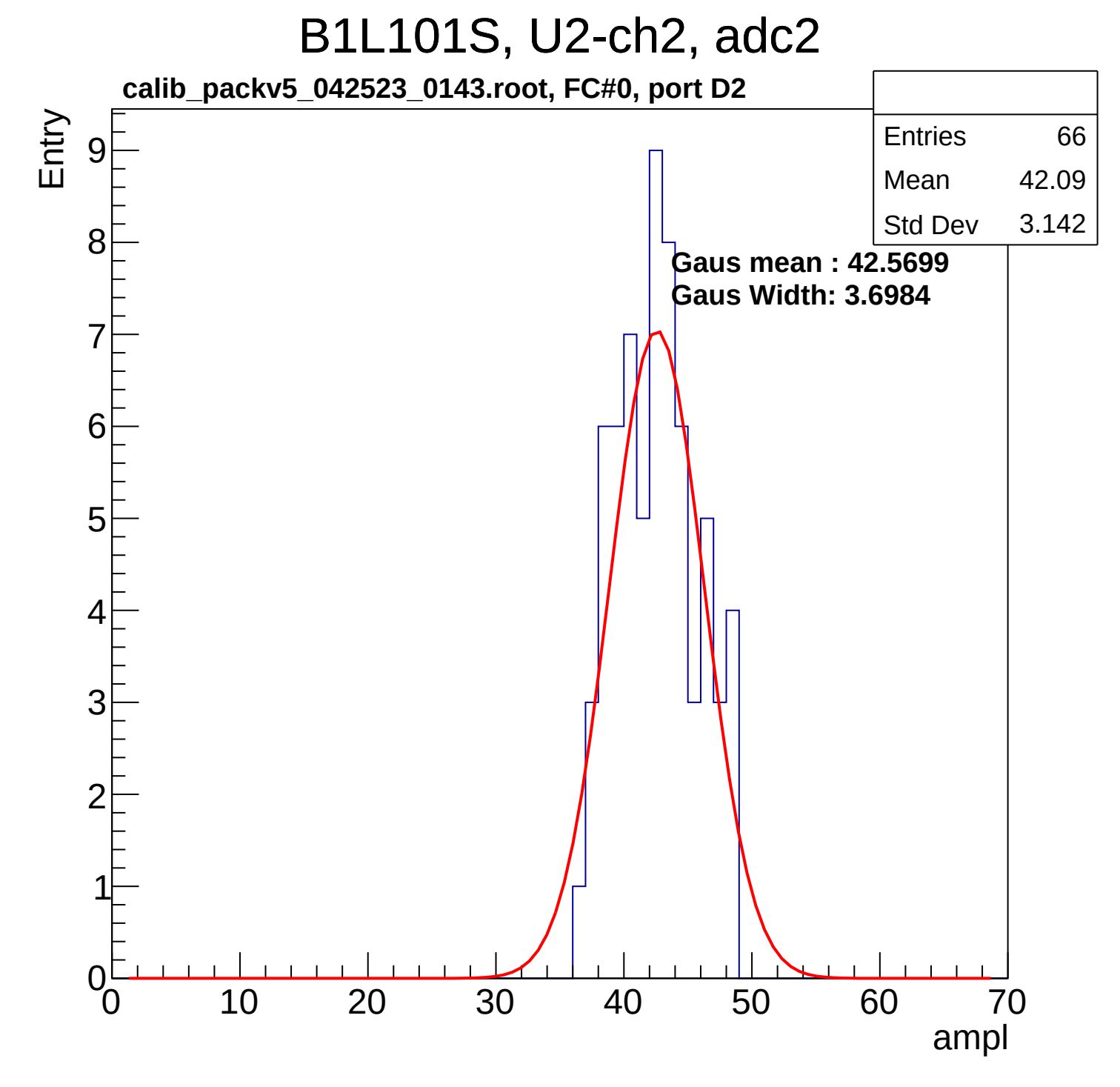

B1L101S, U2-ch1, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 58.02
Std Dev 8.281
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

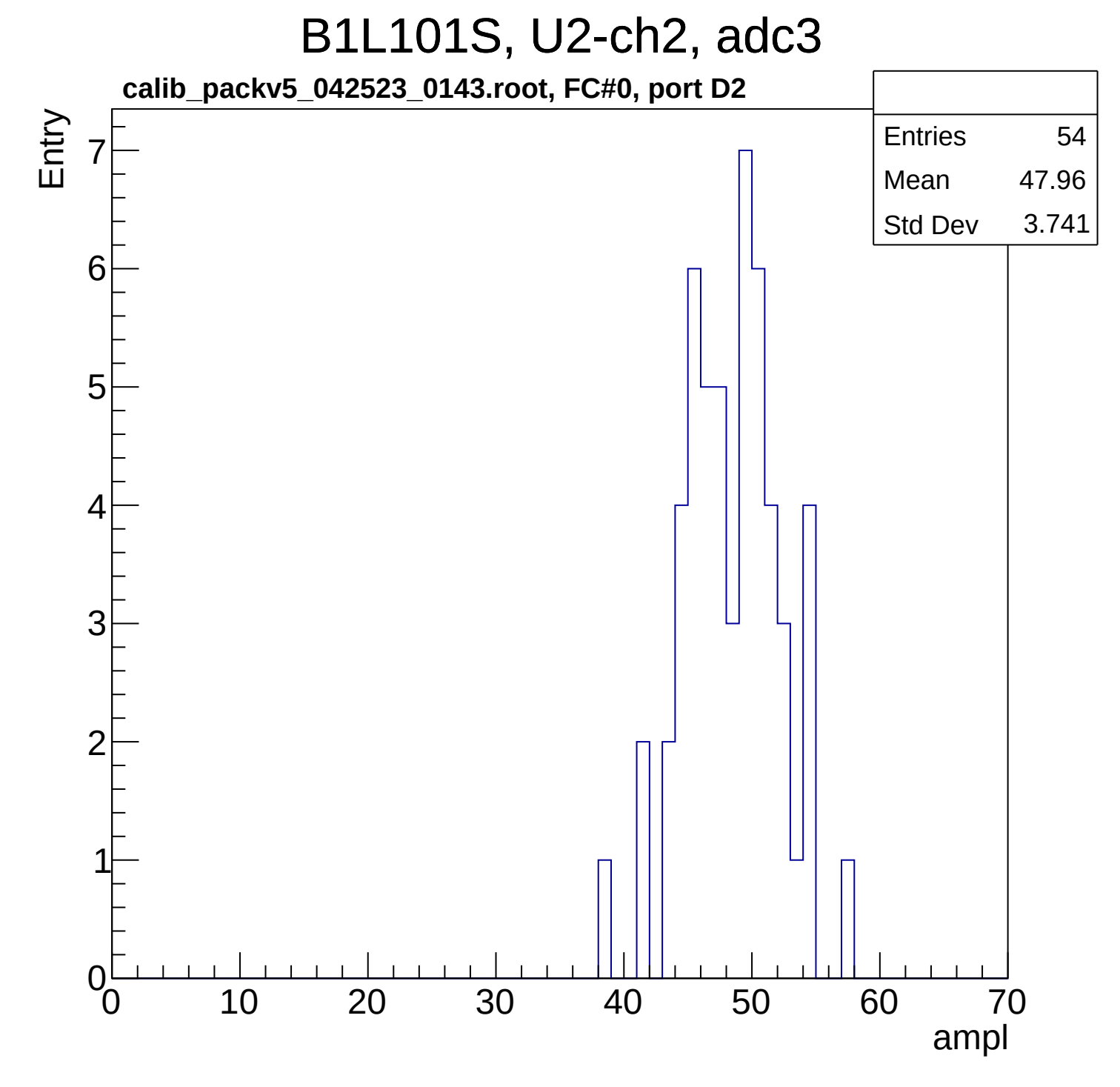

B1L101S, U2-ch1, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 61.4
Std Dev 1.497
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

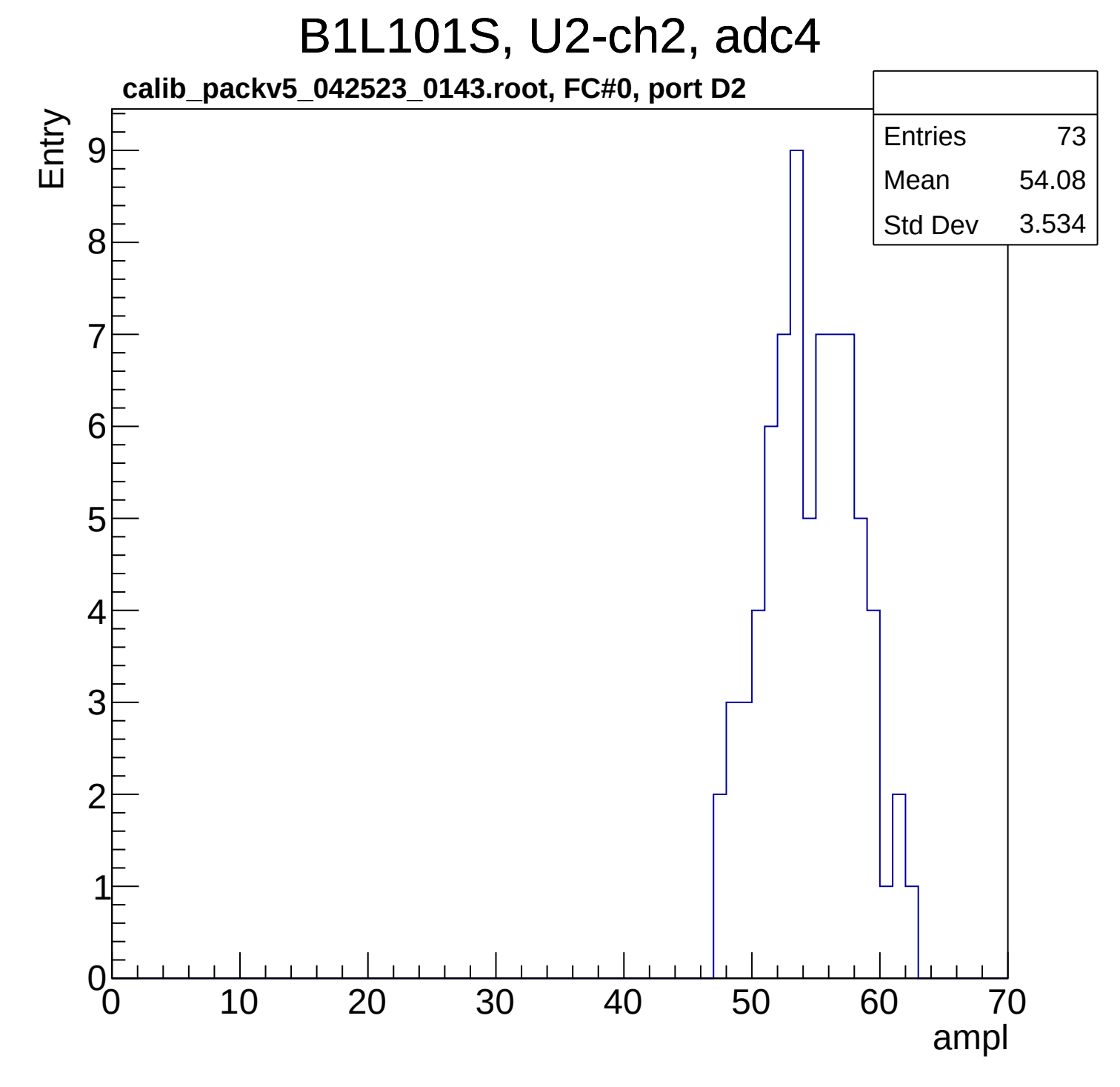

B1L101S, U2-ch1, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 31
Std Dev 31
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

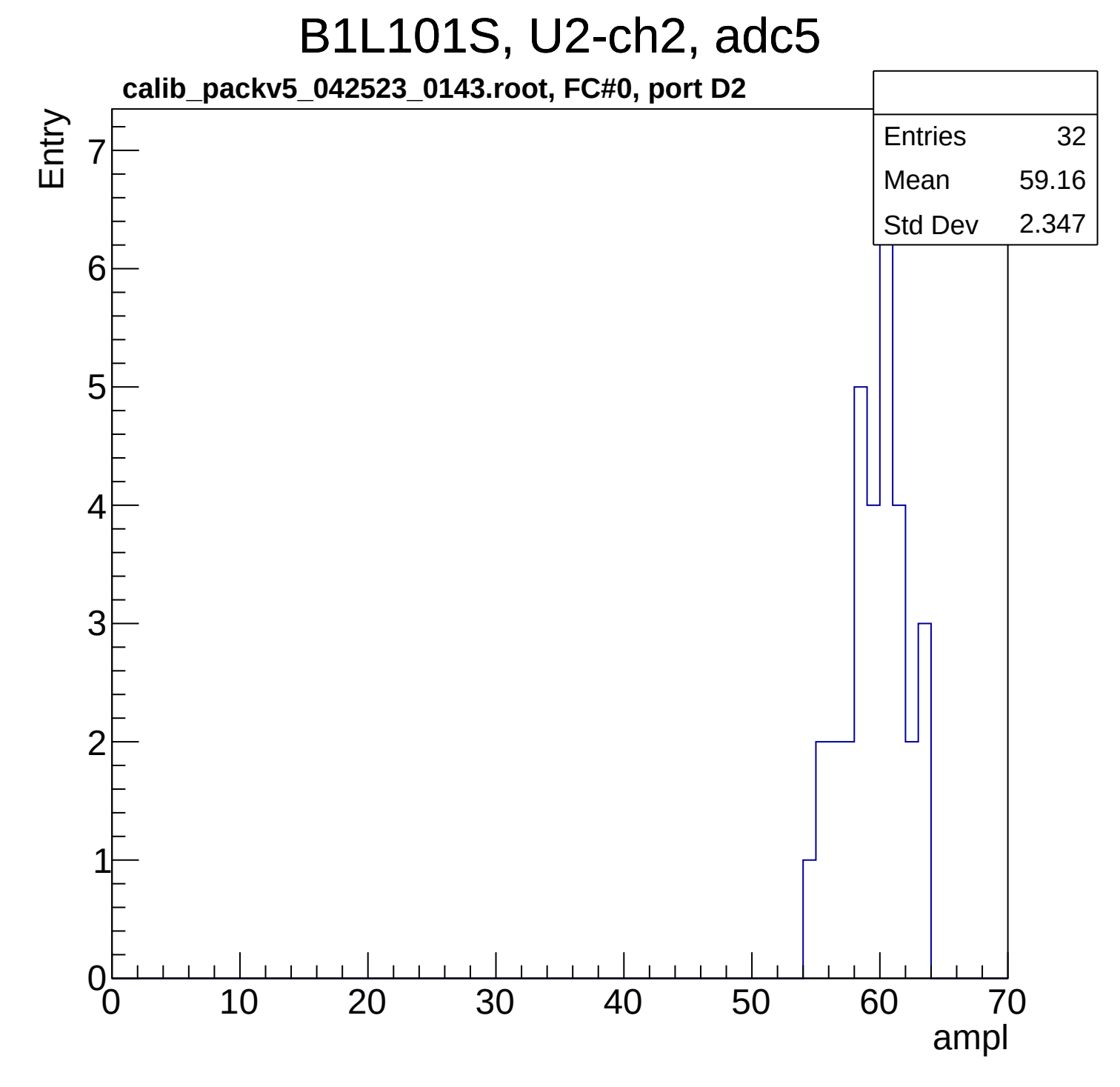

B1L101S, U2-ch2, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 27.71
Std Dev 4.811
Gaus mean : 28.1403
Gaus Width: 4.6717
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

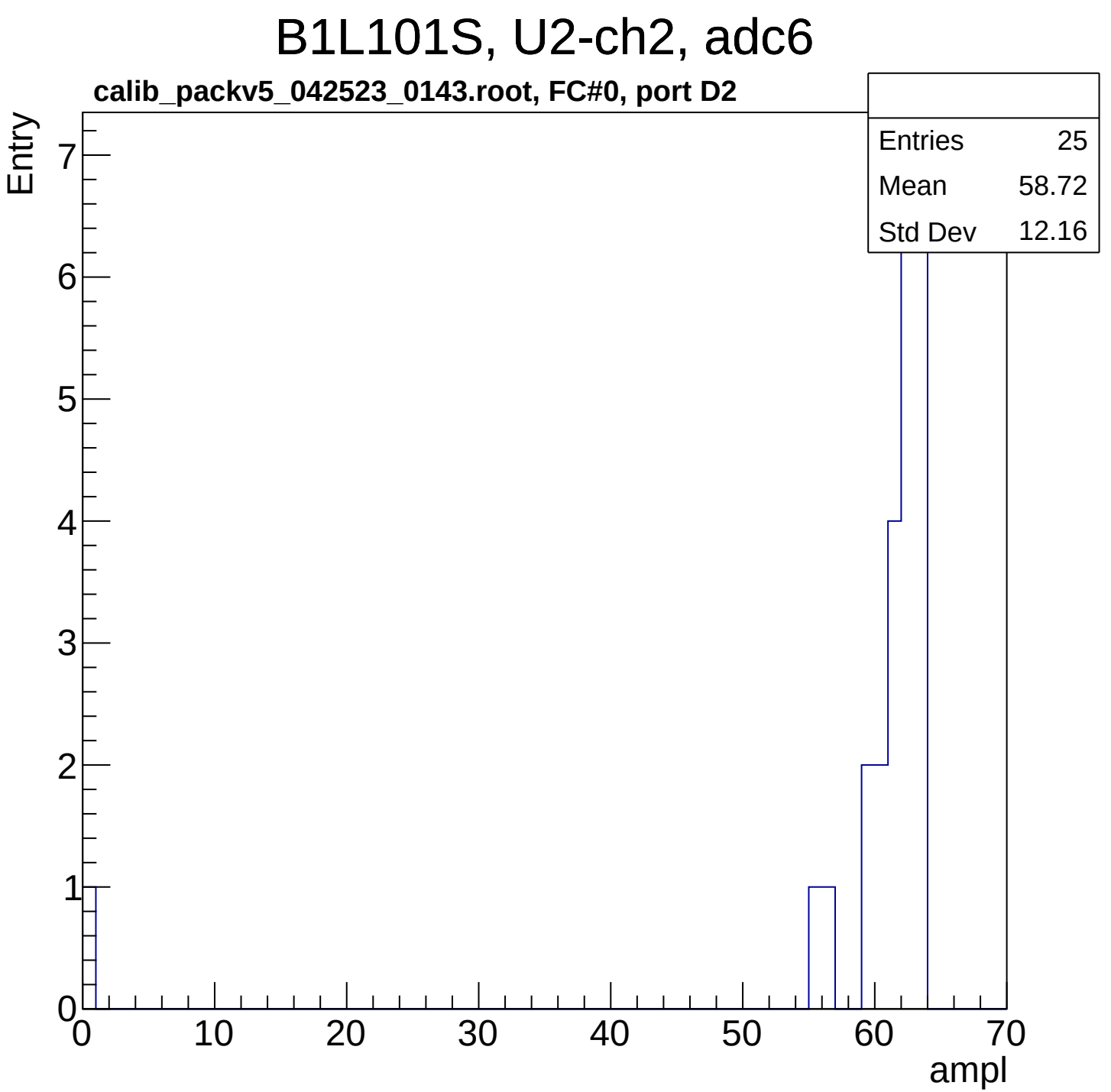

B1L101S, U2-ch2, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 35.12
Std Dev 3.513
Gaus mean : 35.3454
Gaus Width: 3.9351
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

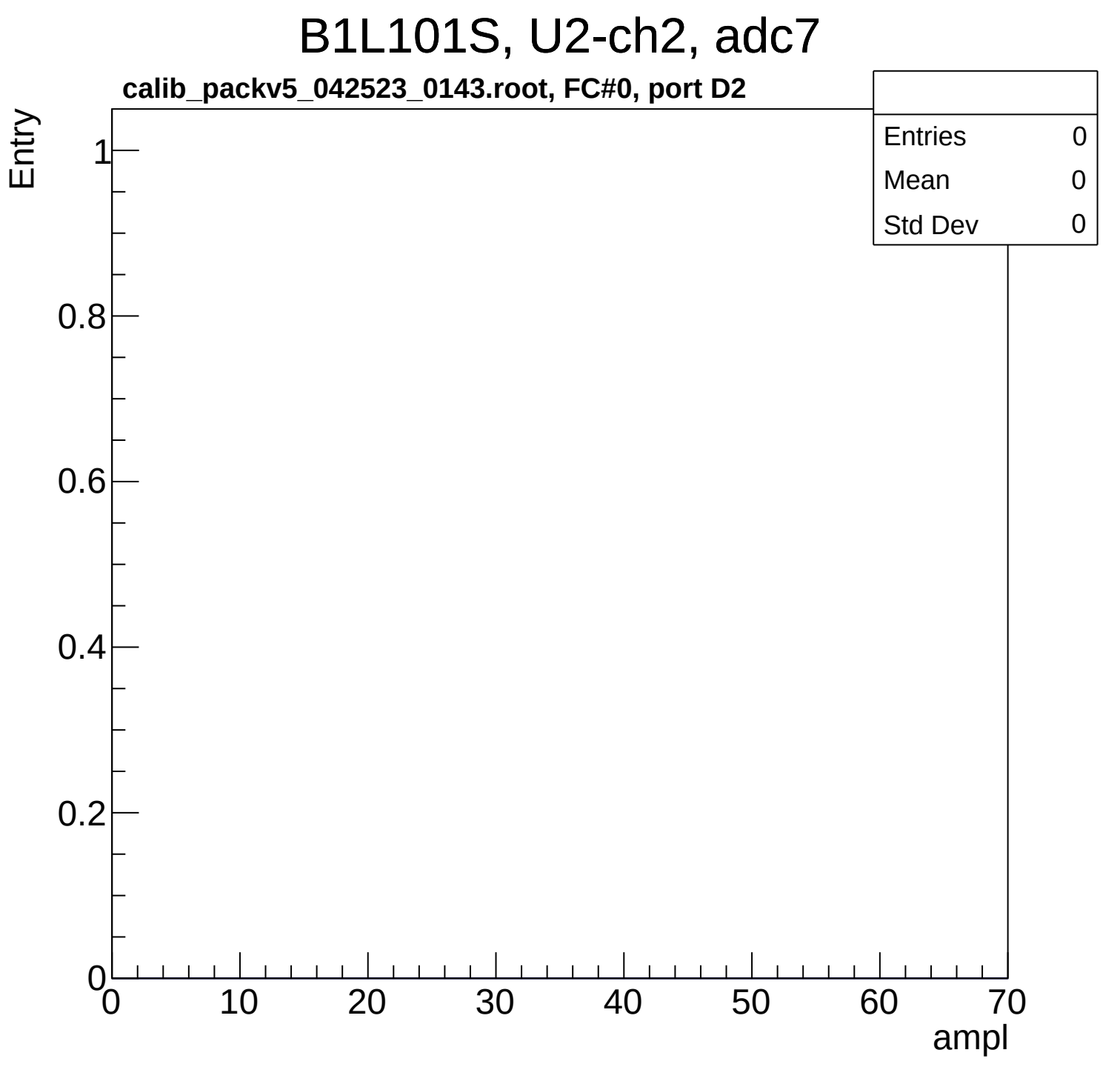

B1L101S, U2-ch2, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 42.09
Std Dev 3.142
Gaus mean : 42.5699
Gaus Width: 3.6984
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

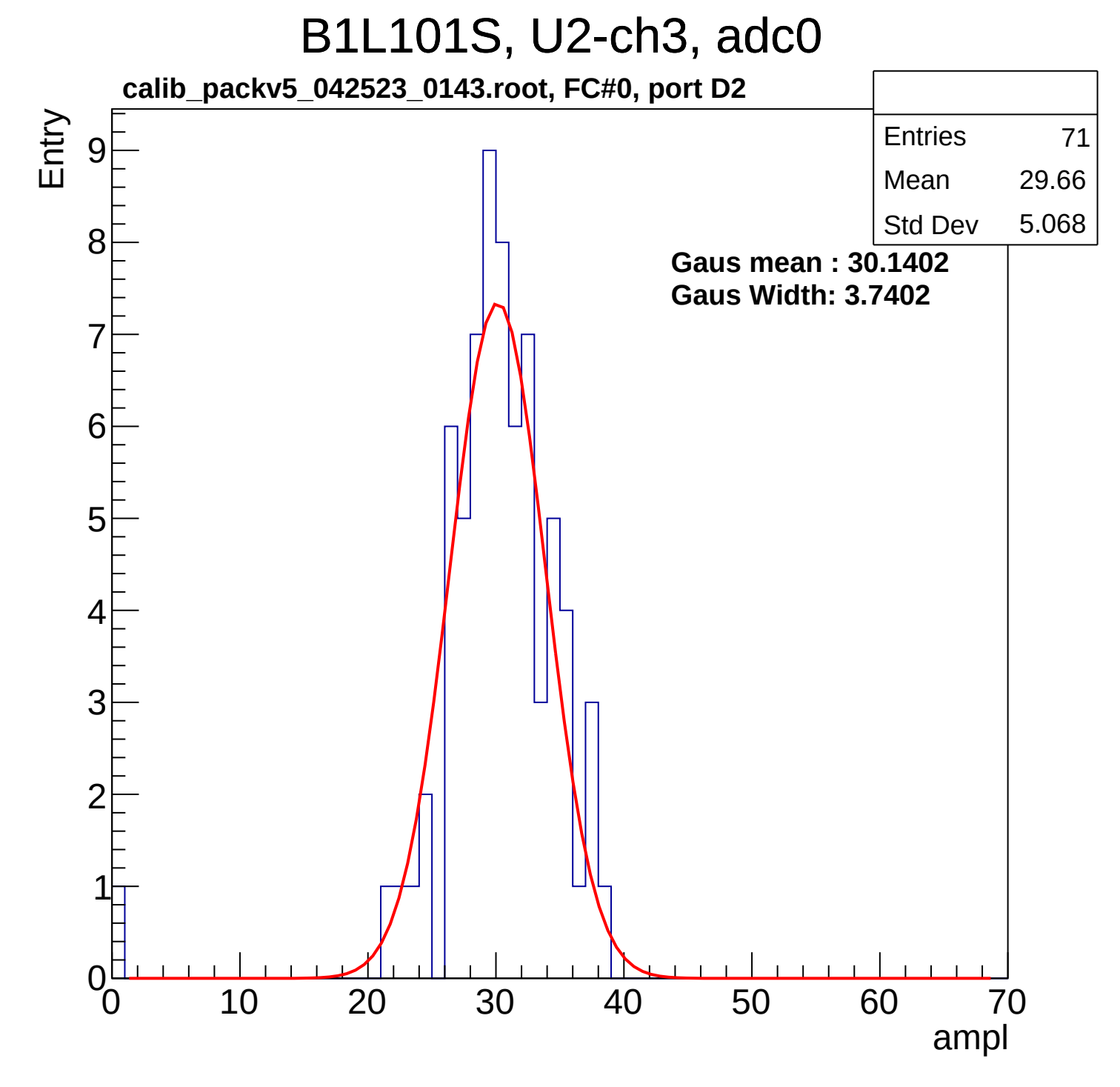

B1L101S, U2-ch2, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 47.96
Std Dev 3.741
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

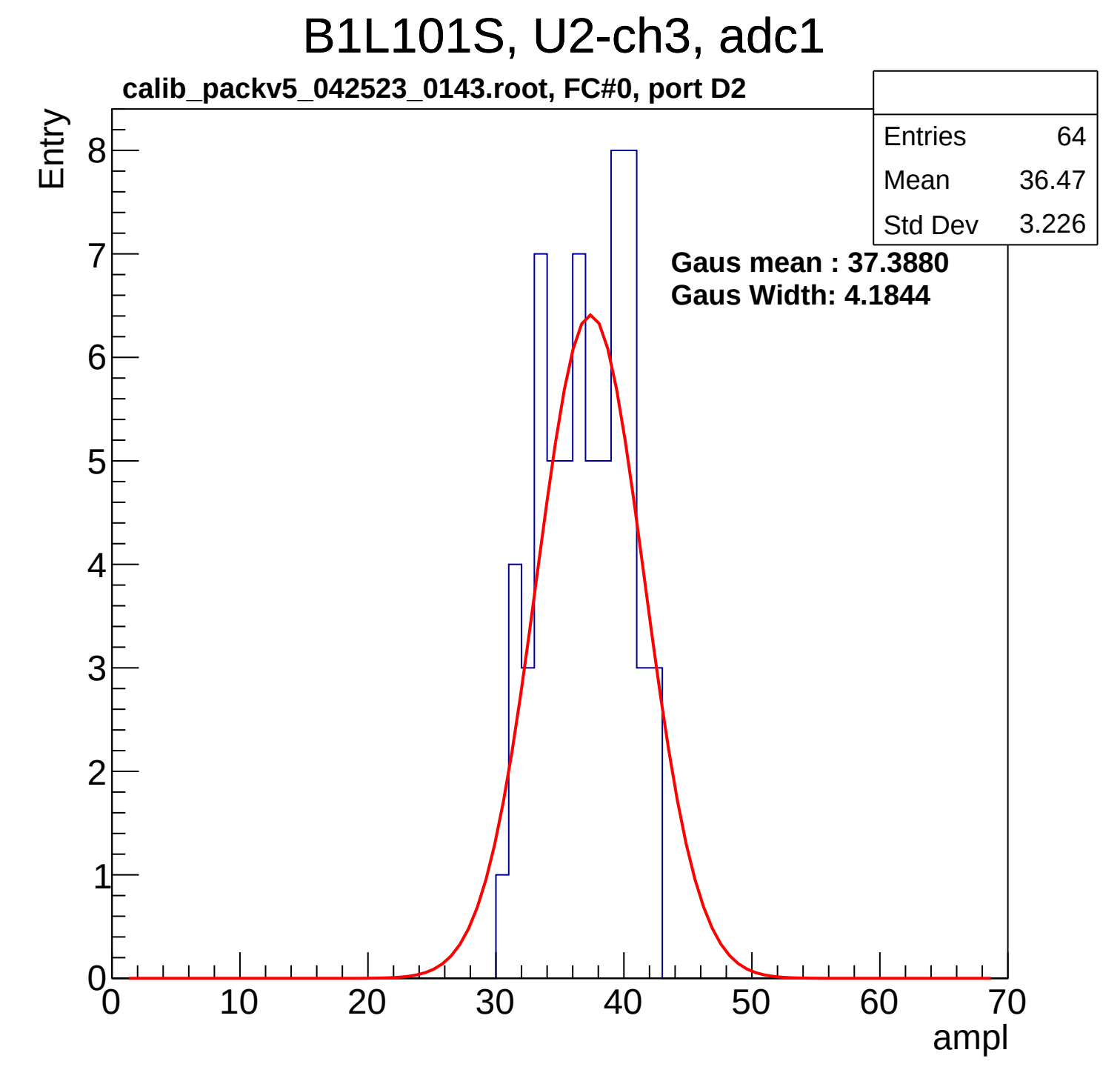

B1L101S, U2-ch2, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 54.08
Std Dev 3.534
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

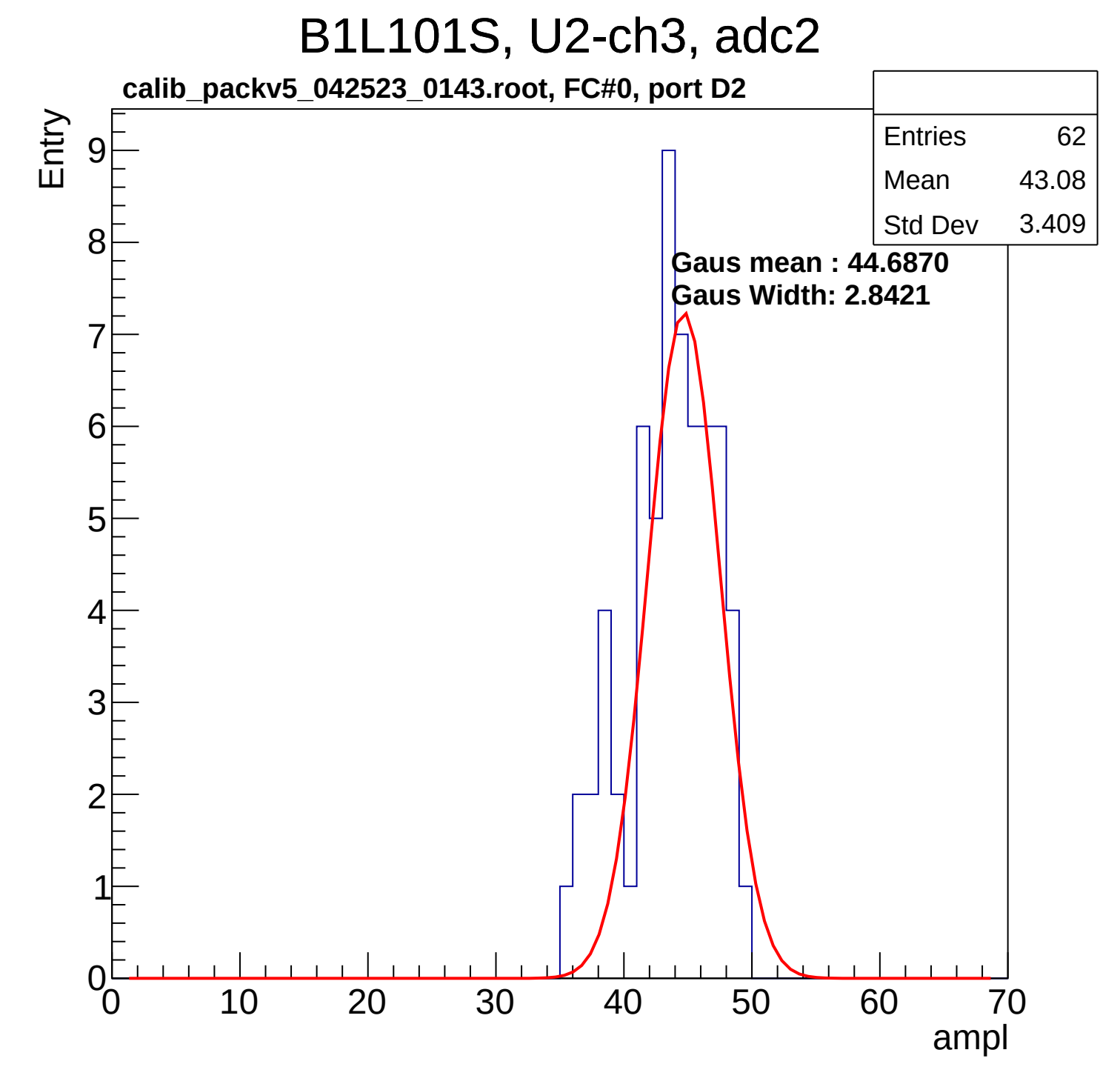

B1L101S, U2-ch2, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 32
Mean 59.16
Std Dev 2.347
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

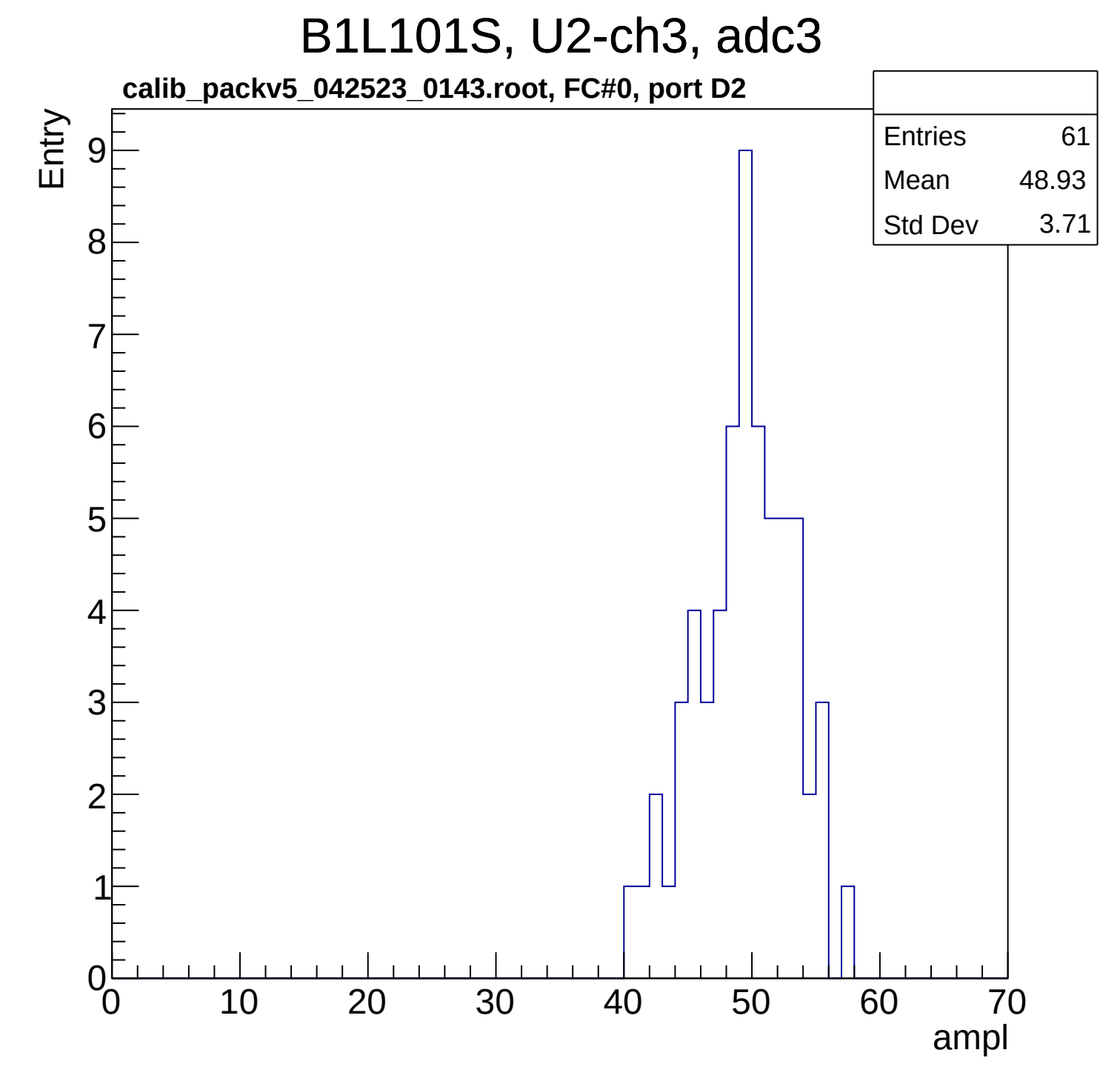

B1L101S, U2-ch2, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 25
Mean 58.72
Std Dev 12.16
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

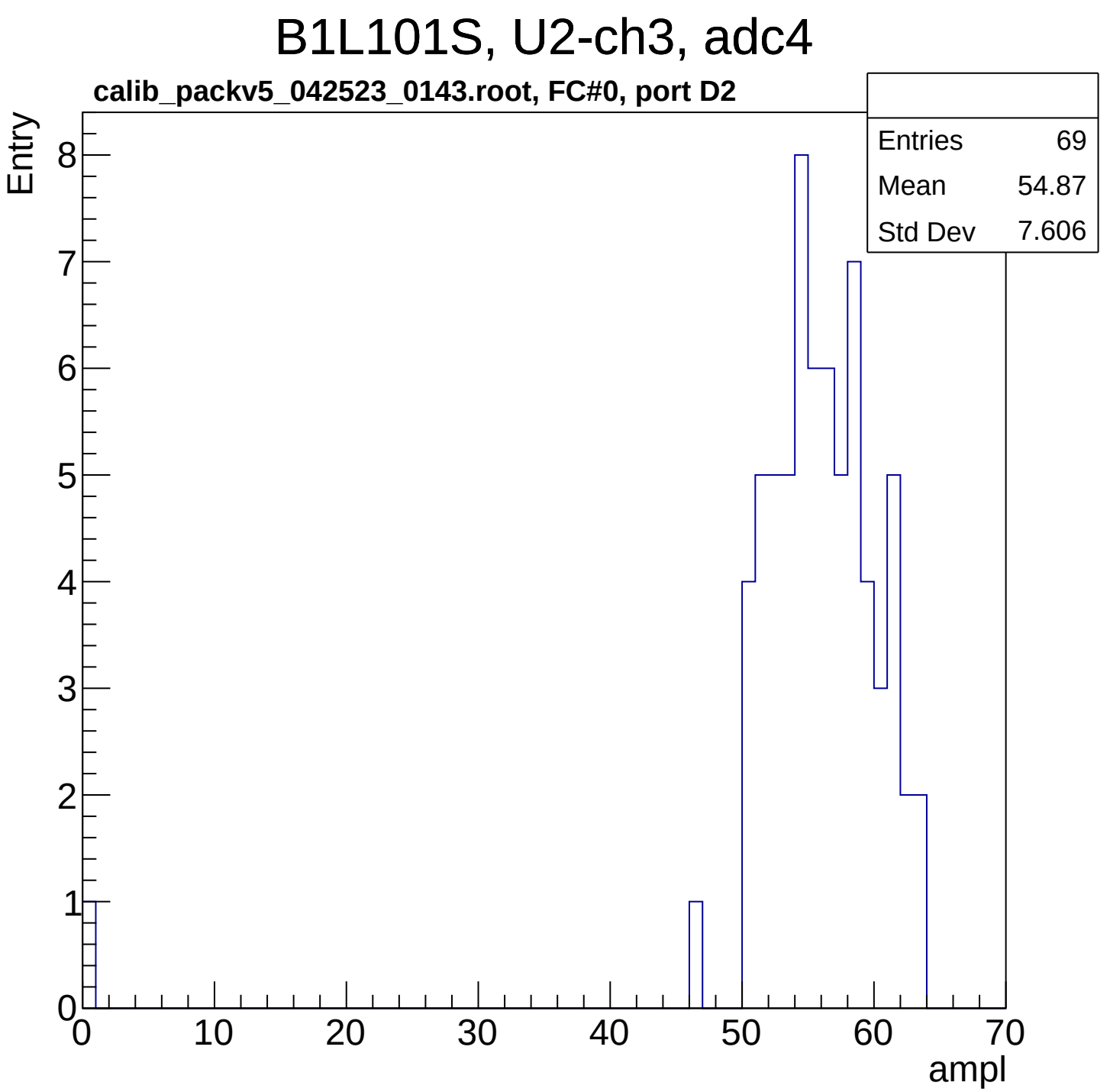

B1L101S, U2-ch2, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

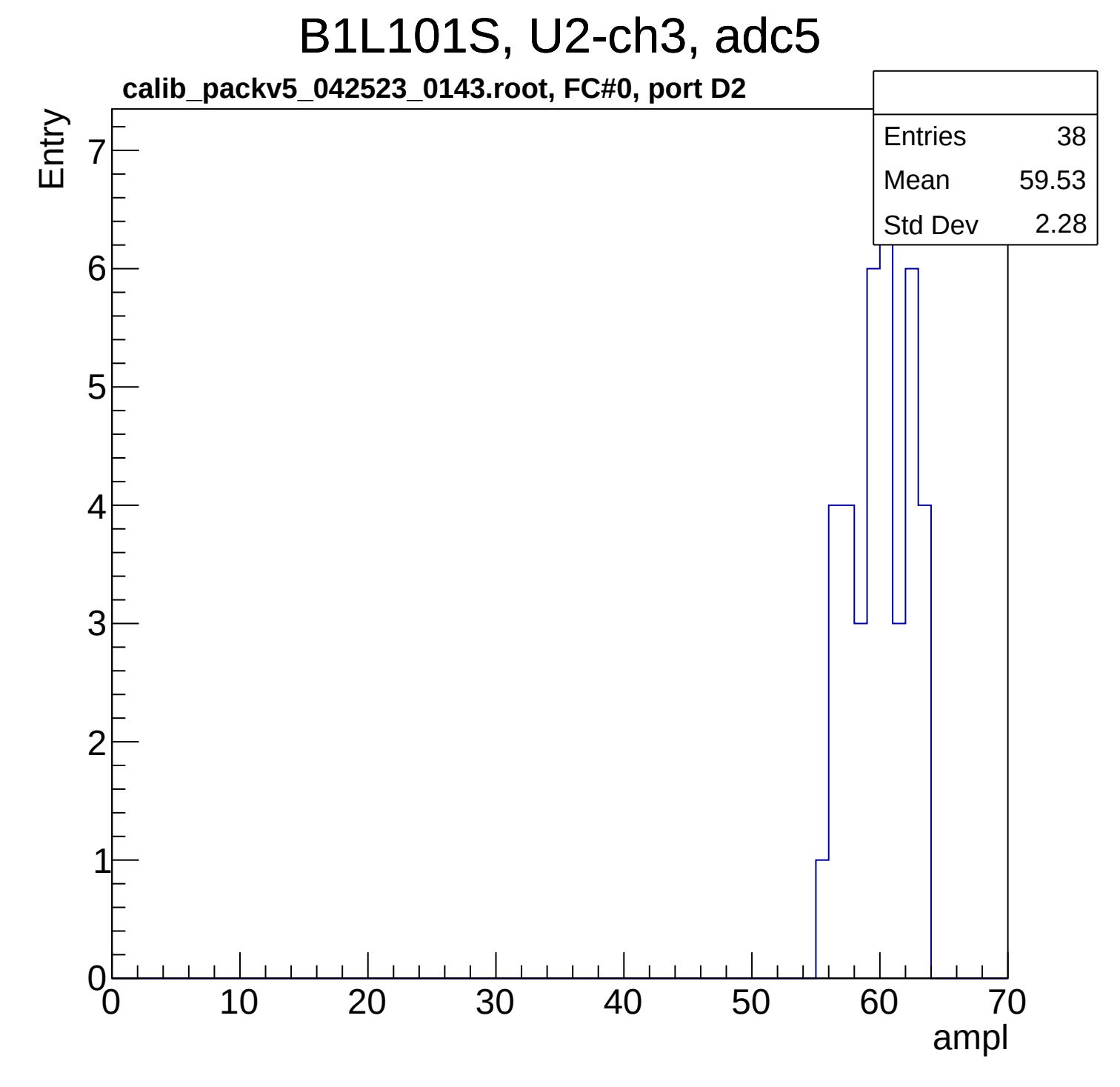

B1L101S, U2-ch3, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 29.66
Std Dev 5.068
Gaus mean : 30.1402
Gaus Width: 3.7402
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

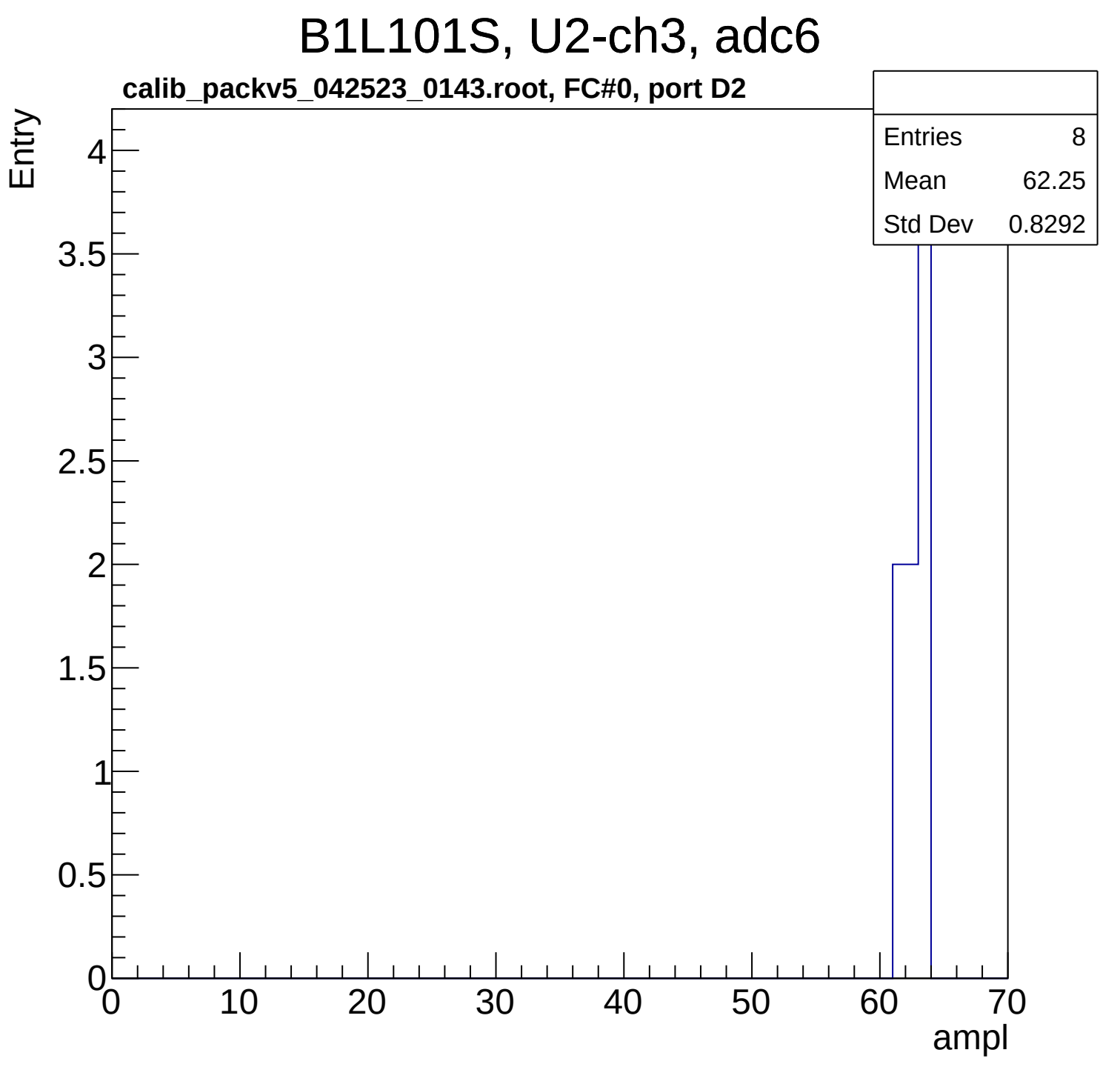

B1L101S, U2-ch3, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 36.47
Std Dev 3.226
Gaus mean : 37.3880
Gaus Width: 4.1844
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

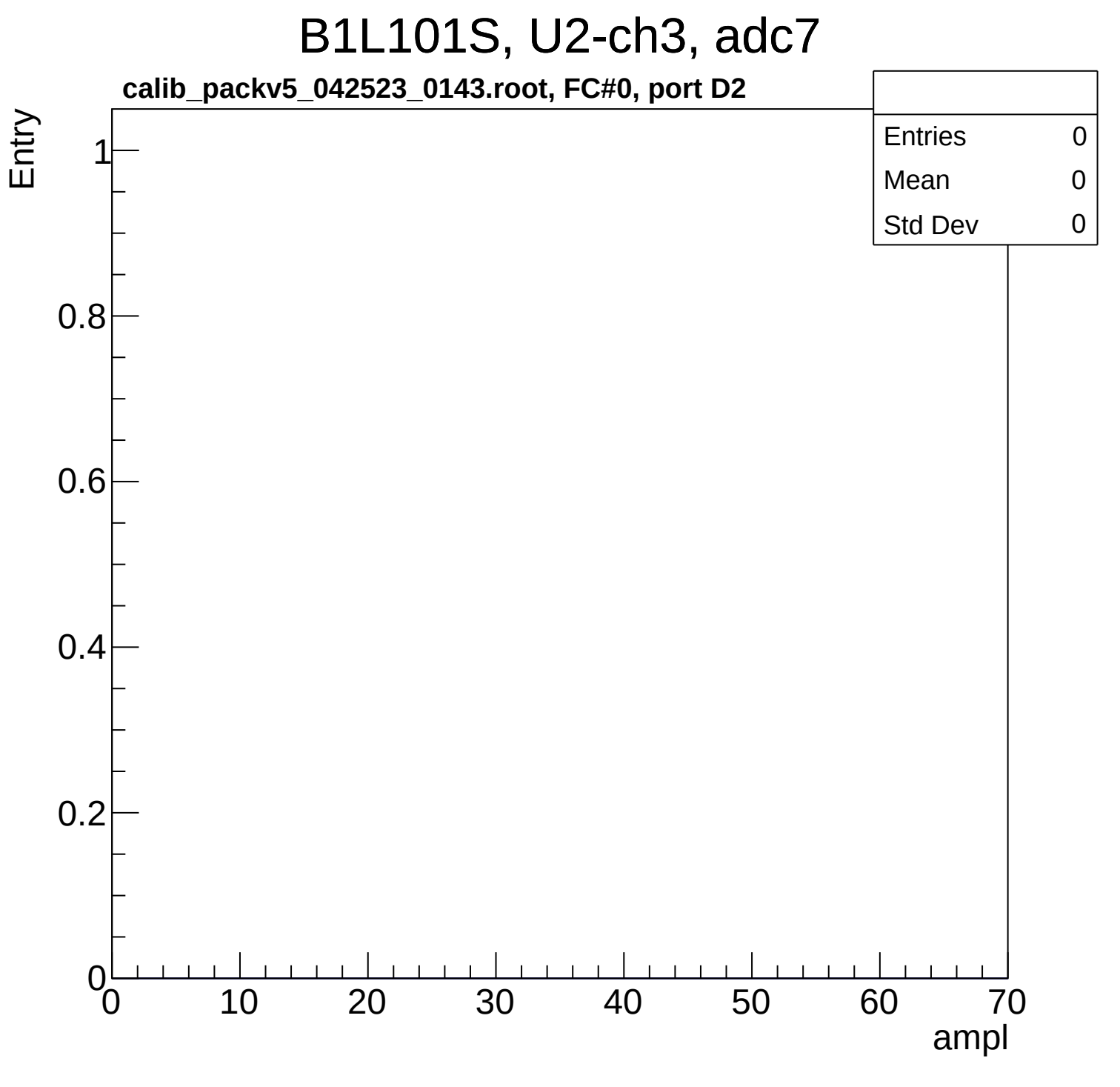

B1L101S, U2-ch3, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 43.08
Std Dev 3.409
Gaus mean : 44.6870
Gaus Width: 2.8421
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

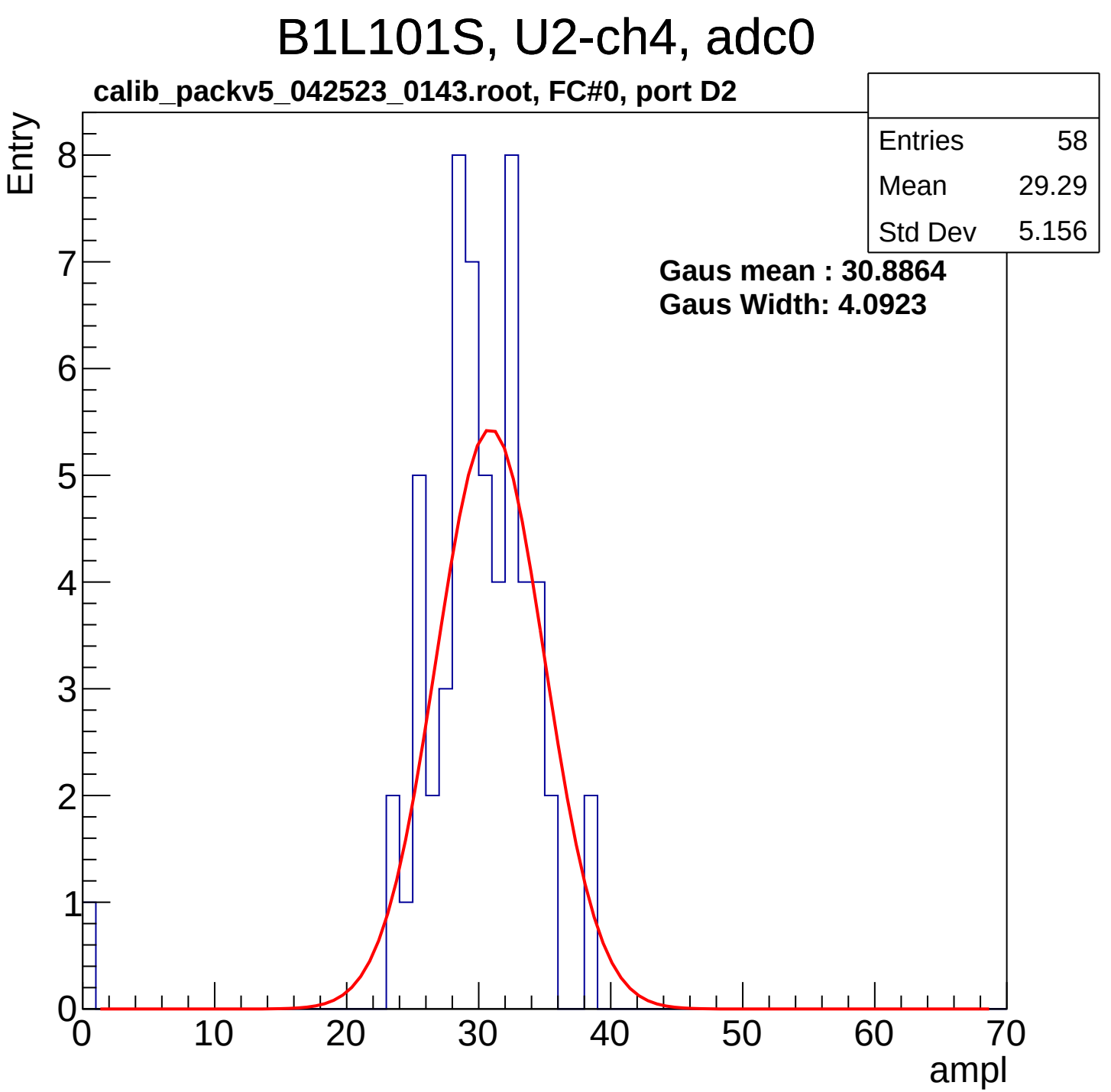

B1L101S, U2-ch3, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 48.93
Std Dev 3.71
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

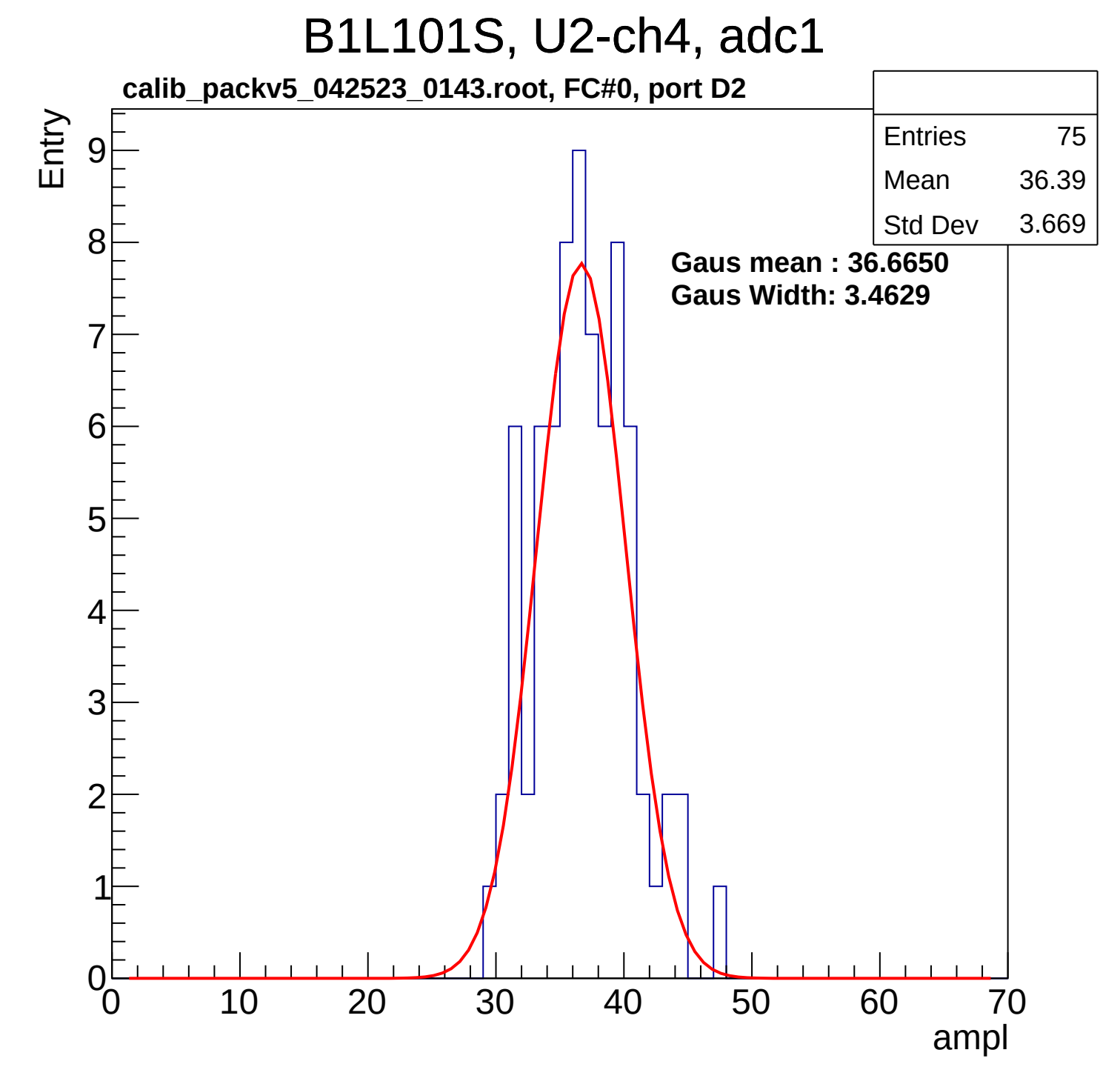

B1L101S, U2-ch3, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 54.87
Std Dev 7.606
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

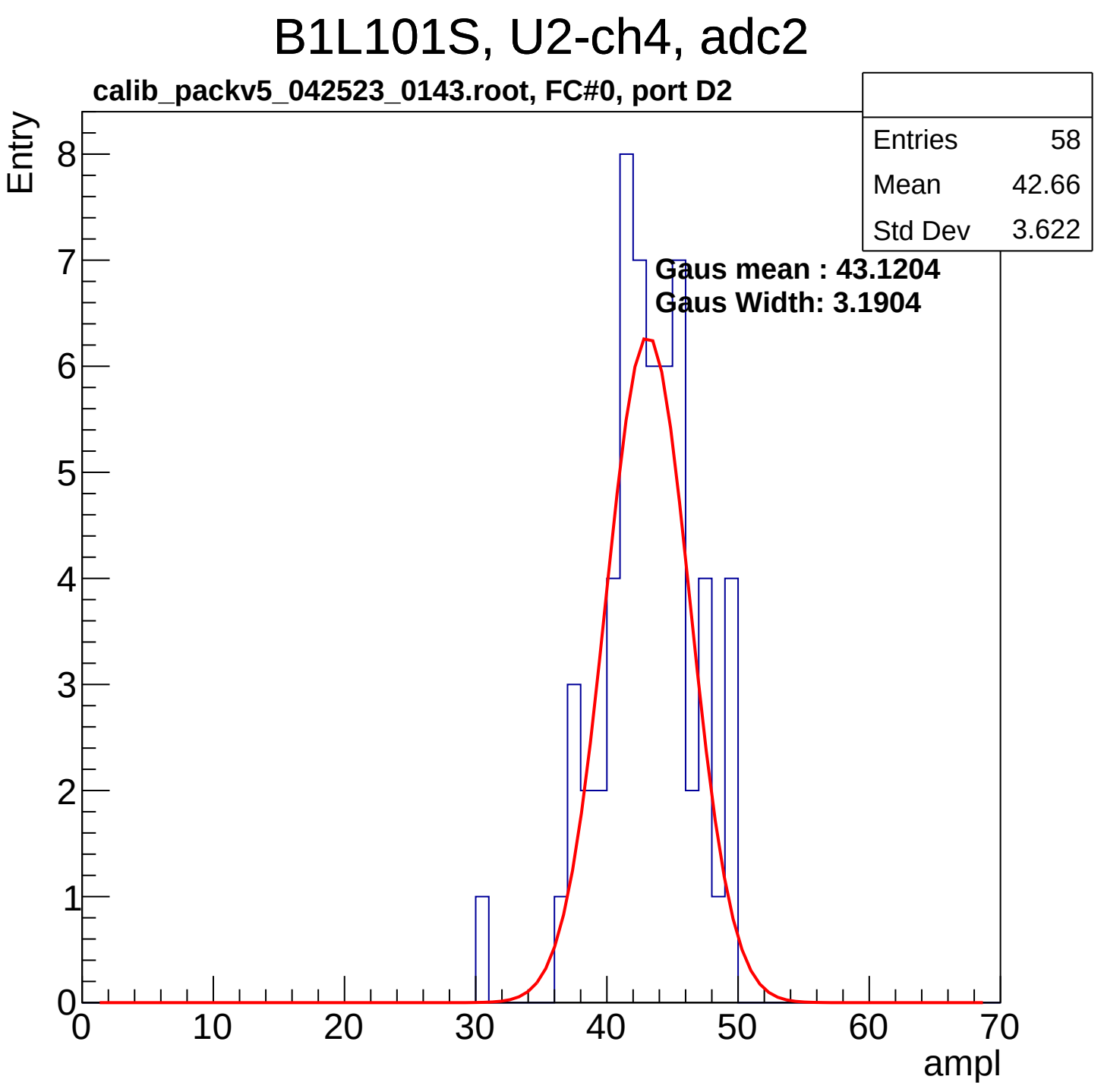

B1L101S, U2-ch3, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 38
Mean 59.53
Std Dev 2.28
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

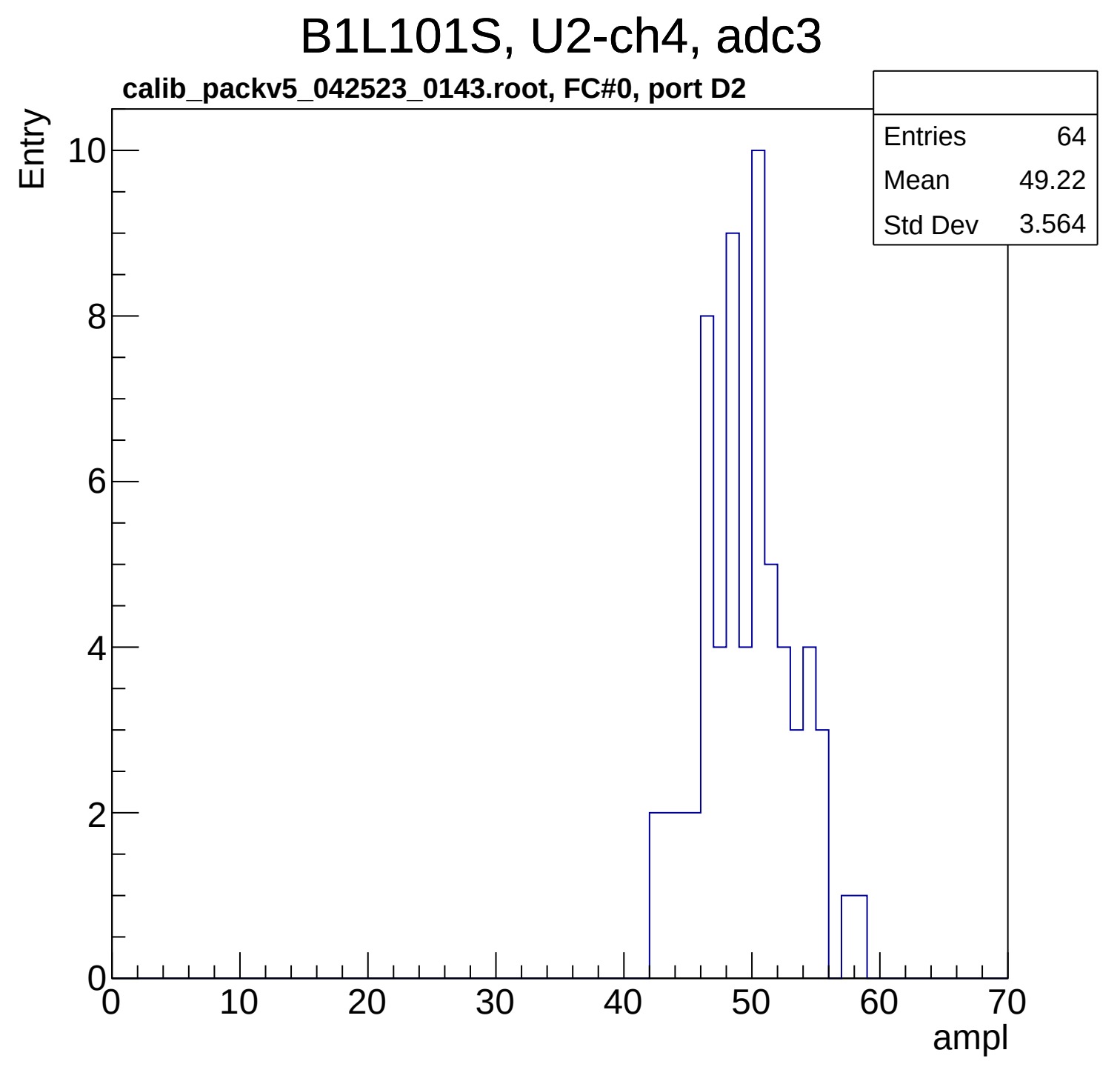

B1L101S, U2-ch3, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

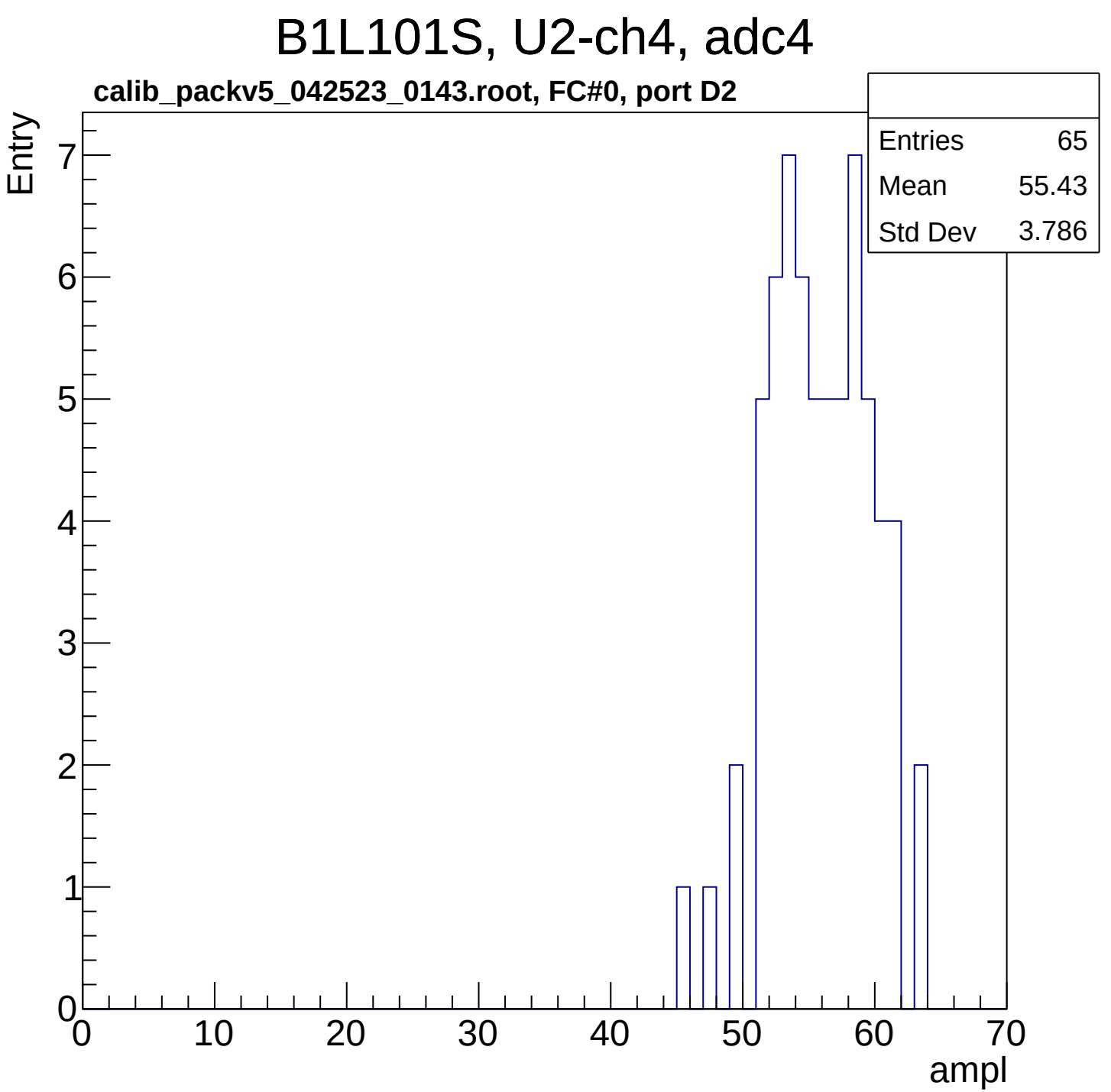

B1L101S, U2-ch3, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

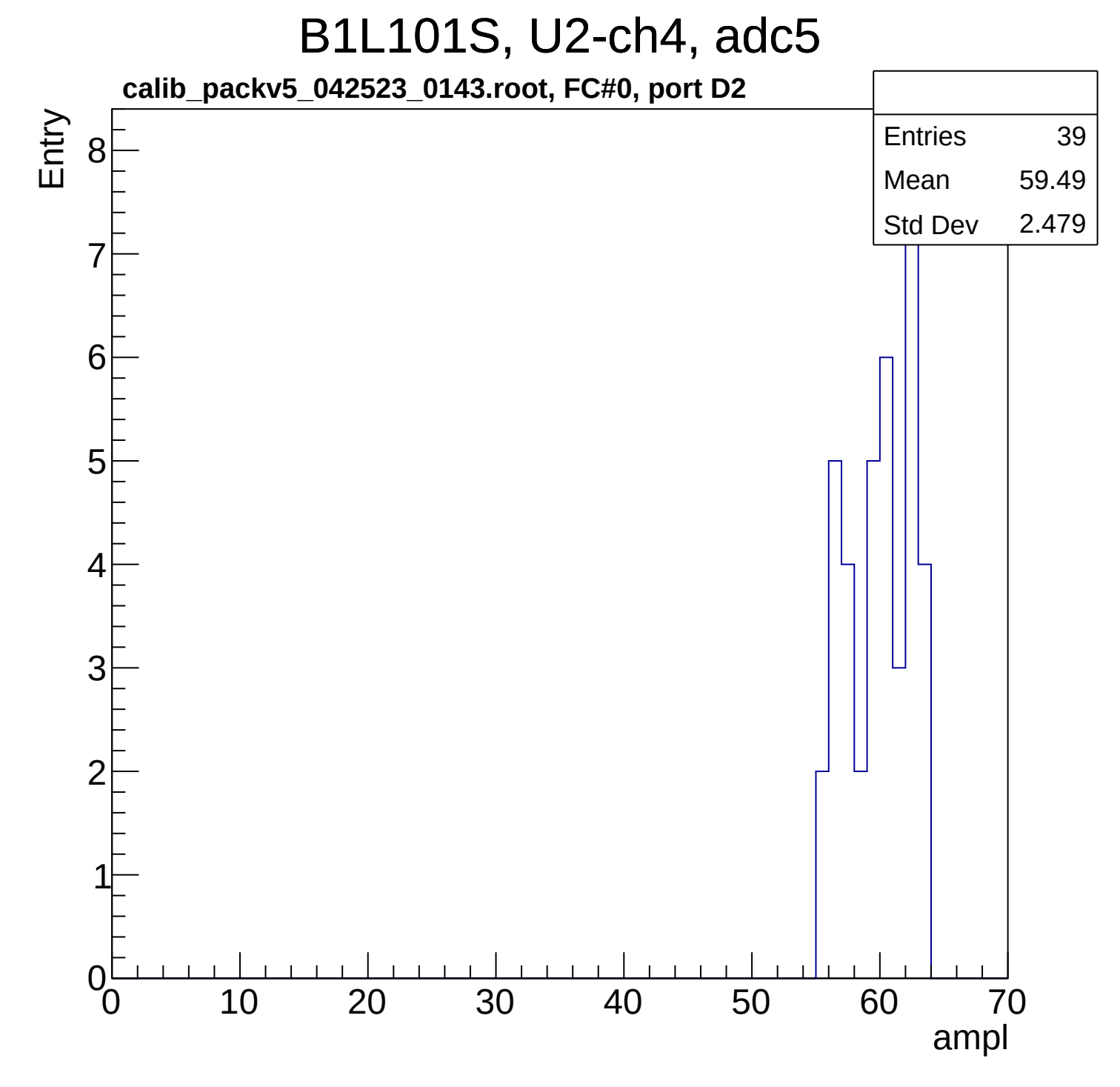

B1L101S, U2-ch4, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 29.29
Std Dev 5.156
Gaus mean : 30.8864
Gaus Width: 4.0923
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

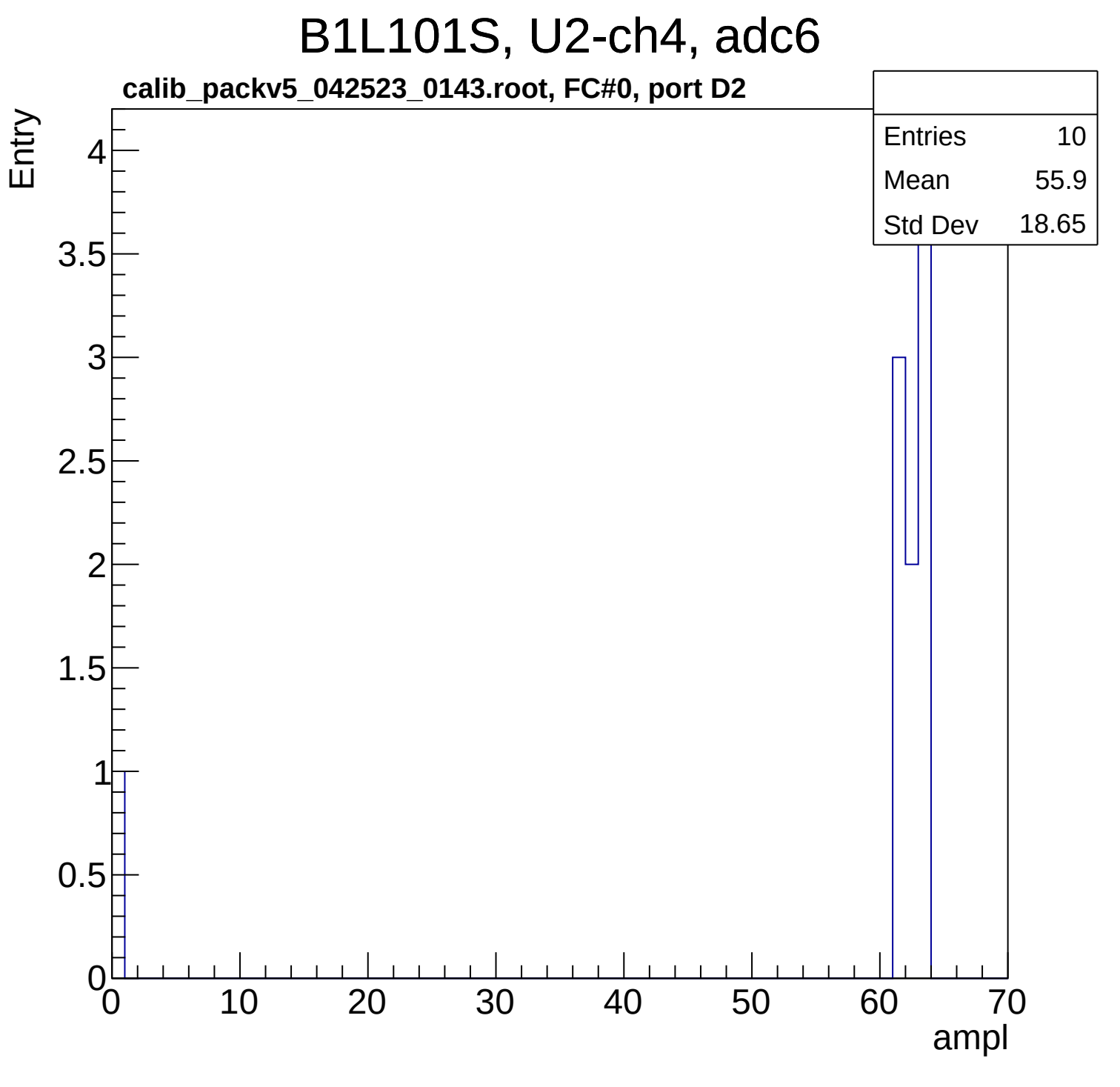

B1L101S, U2-ch4, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 36.39
Std Dev 3.669
Gaus mean : 36.6650
Gaus Width: 3.4629
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

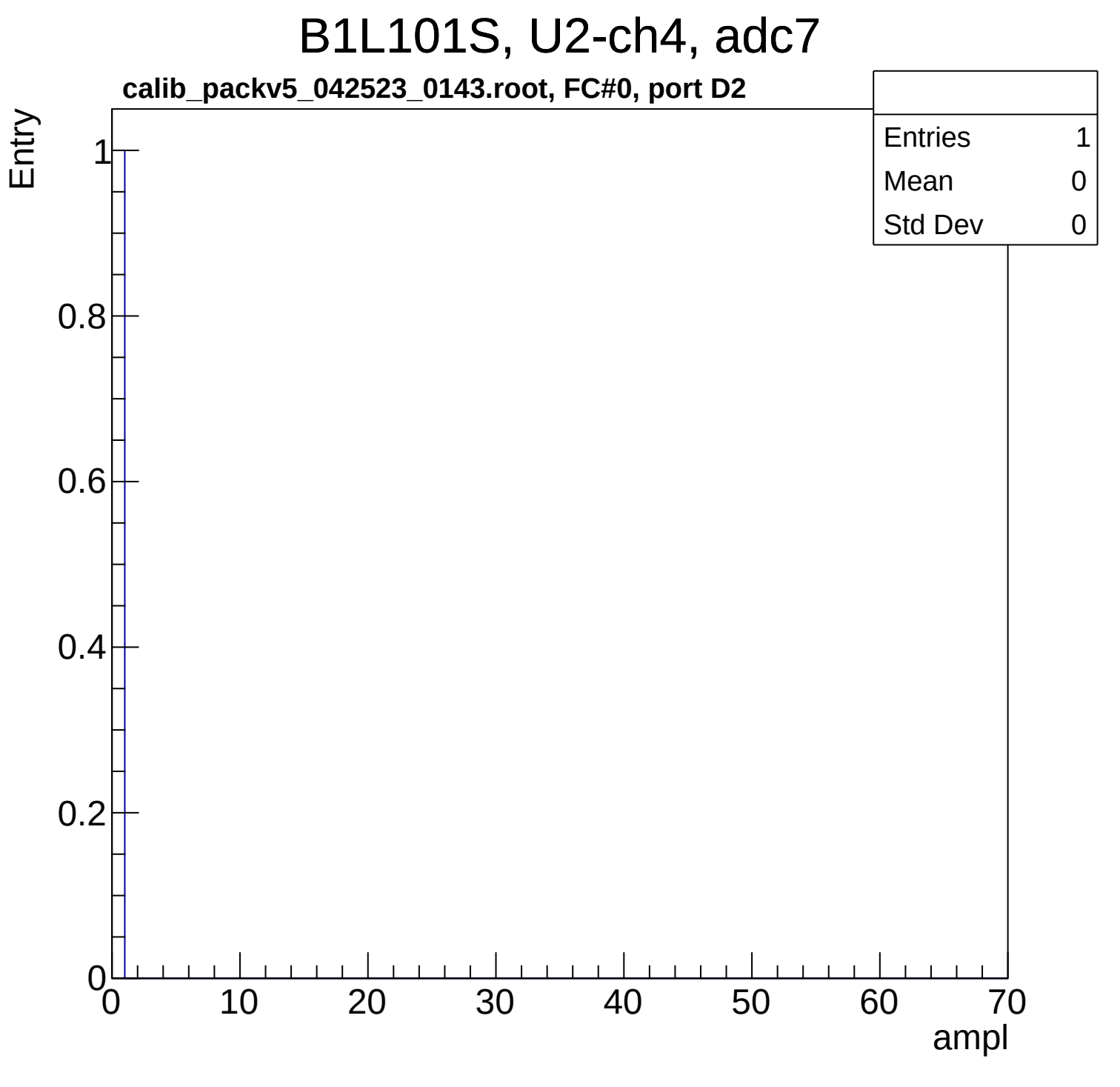

B1L101S, U2-ch4, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 42.66
Std Dev 3.622
Gaus mean : 43.1204
Gaus Width: 3.1904
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

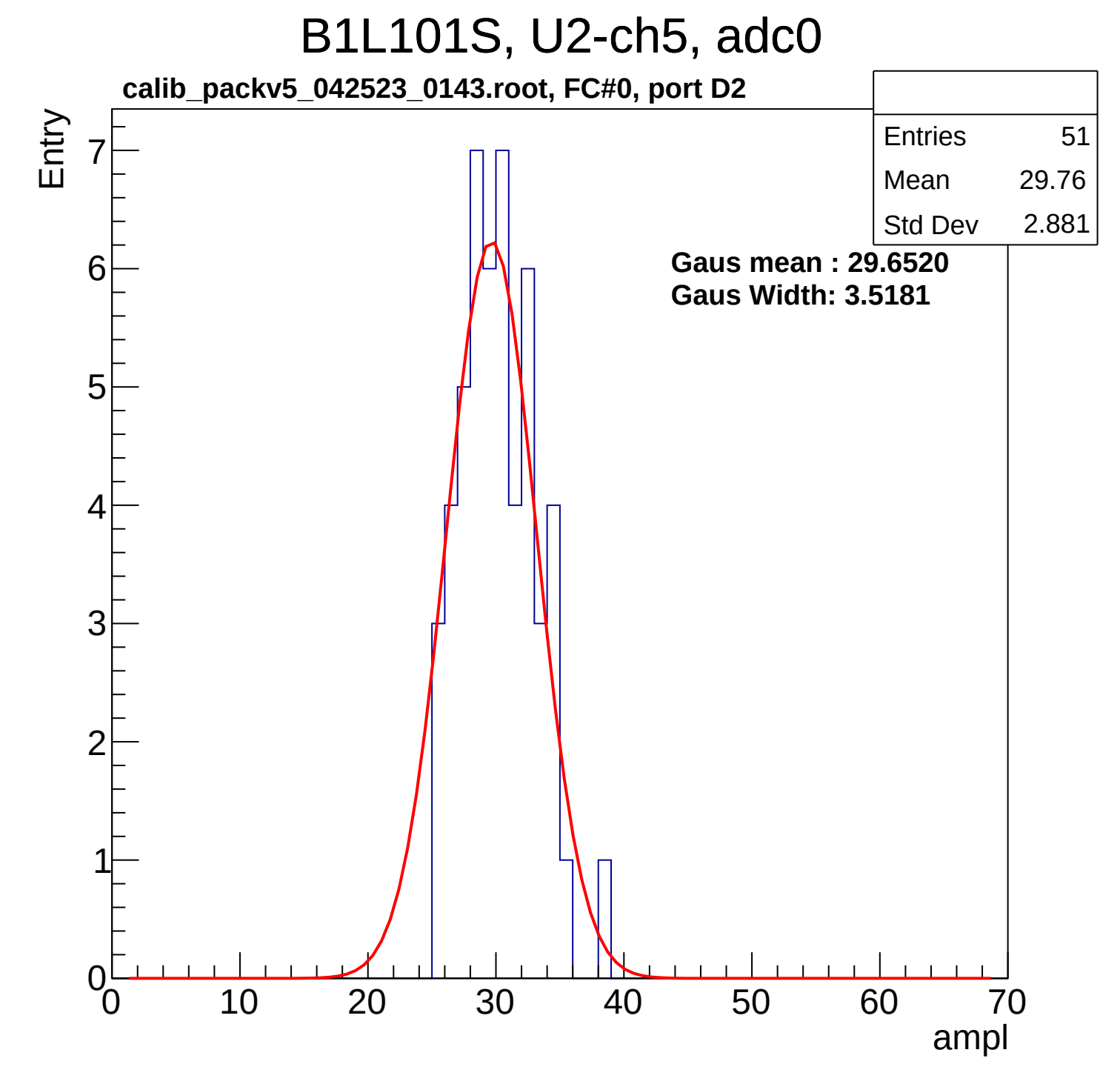

B1L101S, U2-ch4, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 49.22
Std Dev 3.564
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

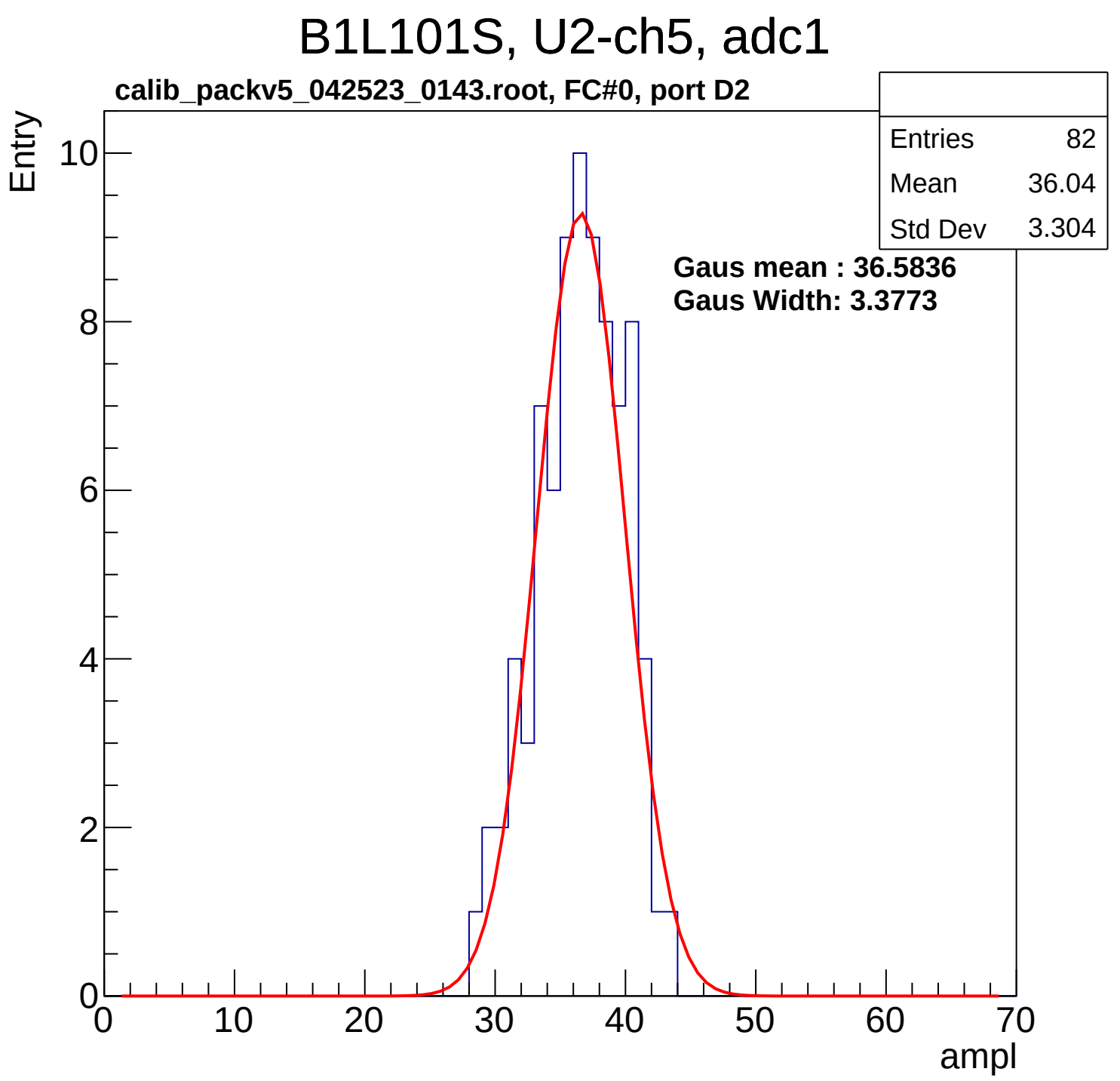

B1L101S, U2-ch4, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 55.43
Std Dev 3.786
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

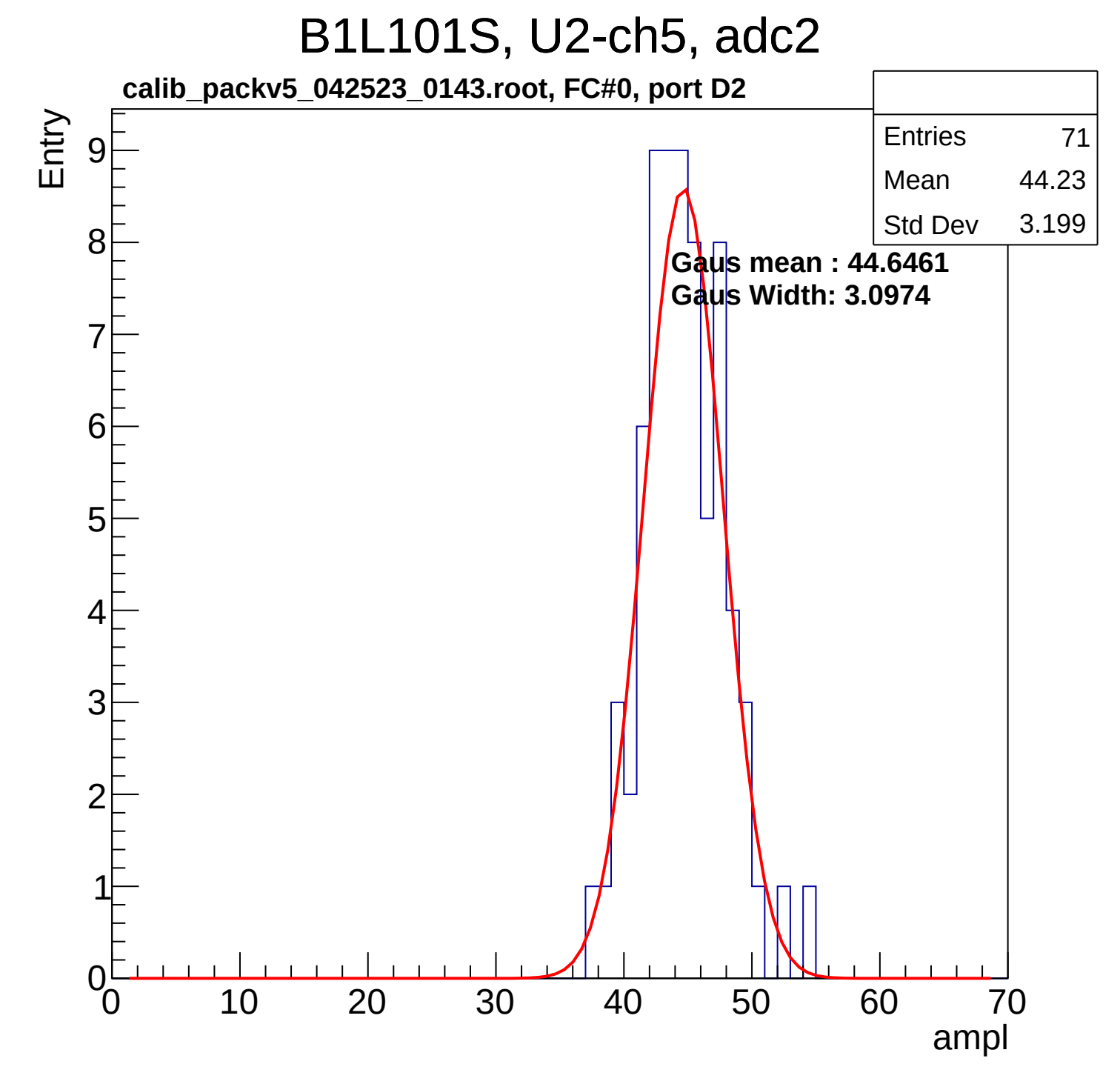

B1L101S, U2-ch4, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 39
Mean 59.49
Std Dev 2.479
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

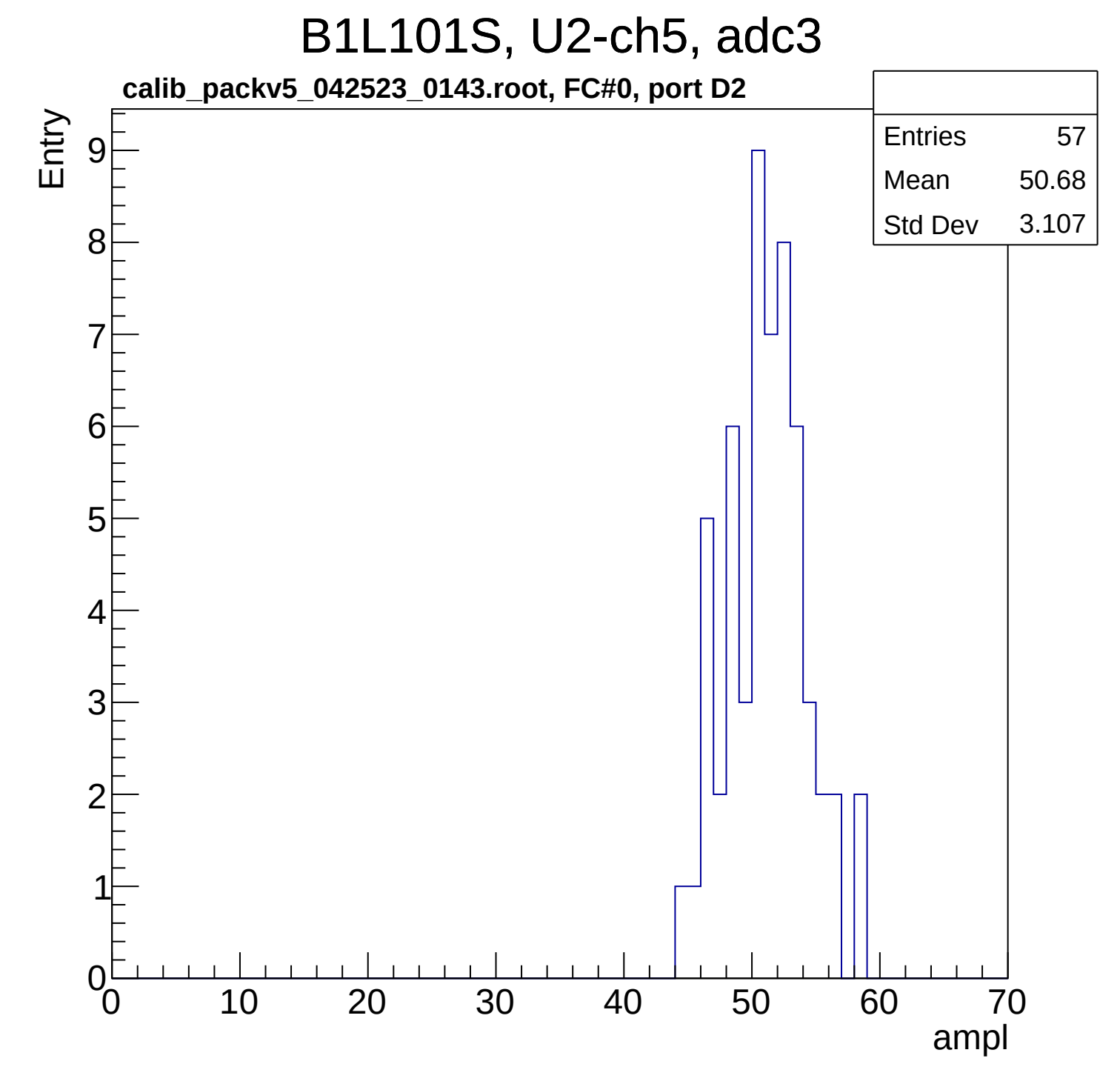

B1L101S, U2-ch4, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 55.9
Std Dev 18.65
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

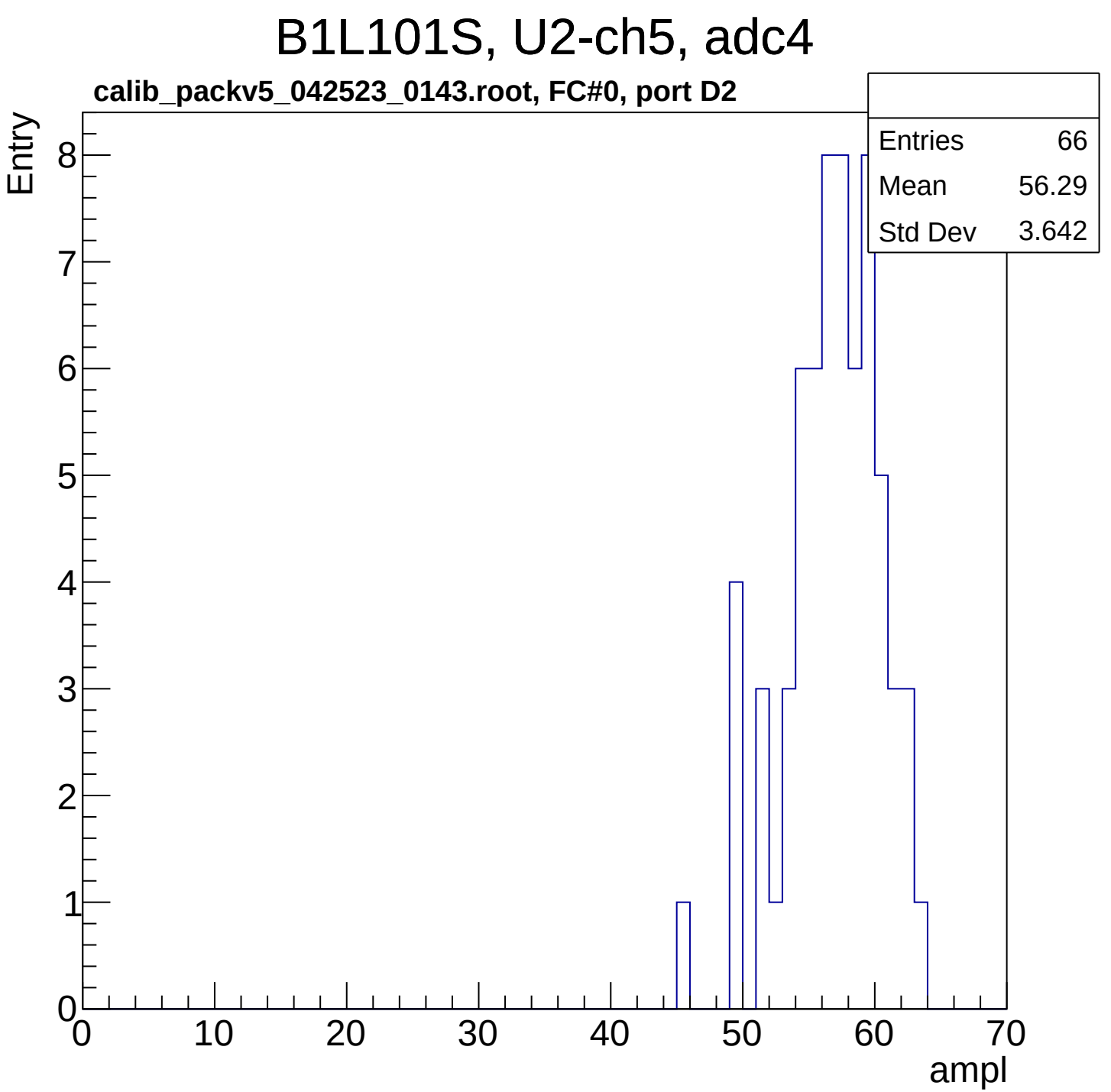

B1L101S, U2-ch4, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

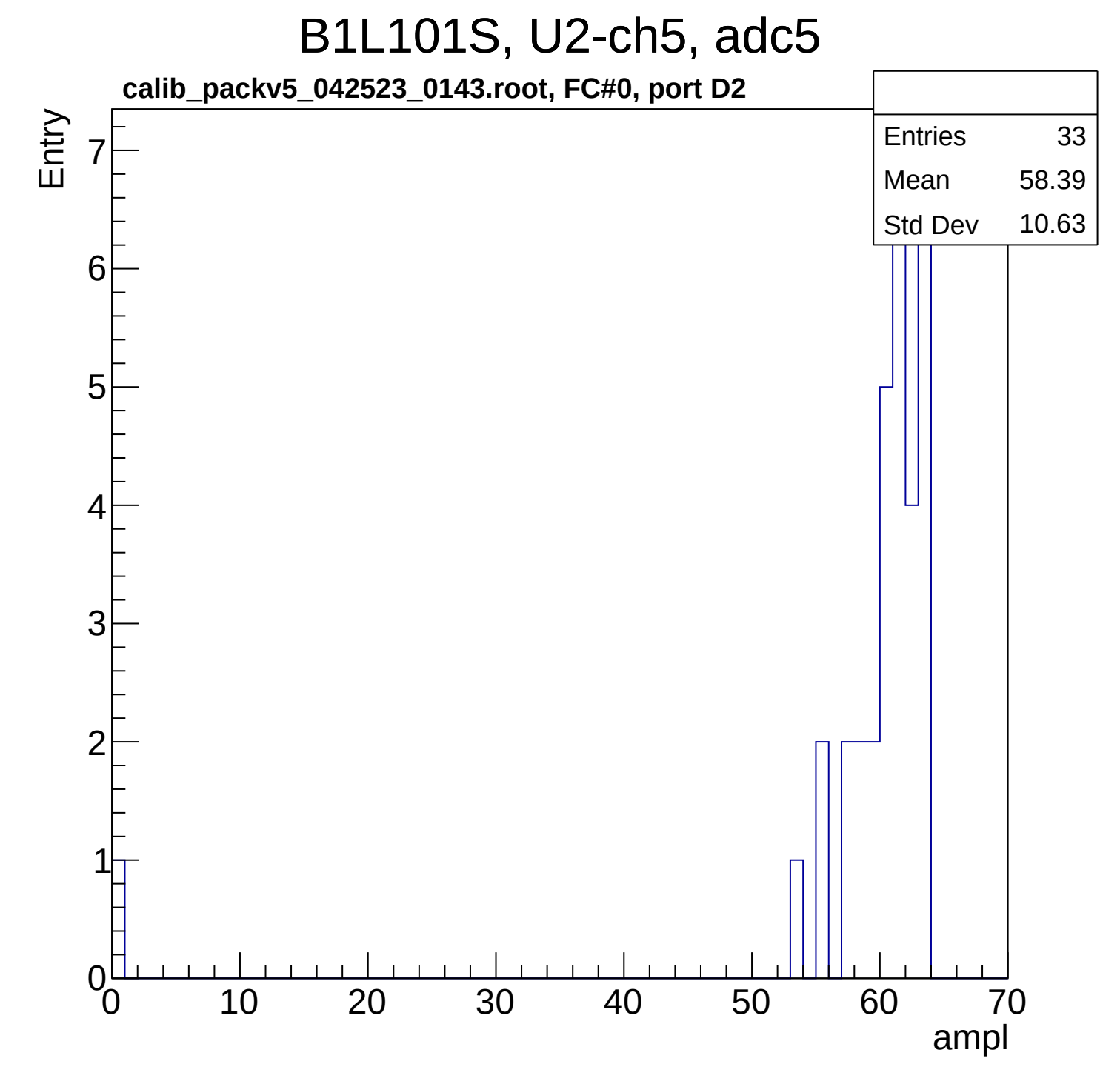

B1L101S, U2-ch5, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 29.76
Std Dev 2.881
Gaus mean : 29.6520
Gaus Width: 3.5181
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

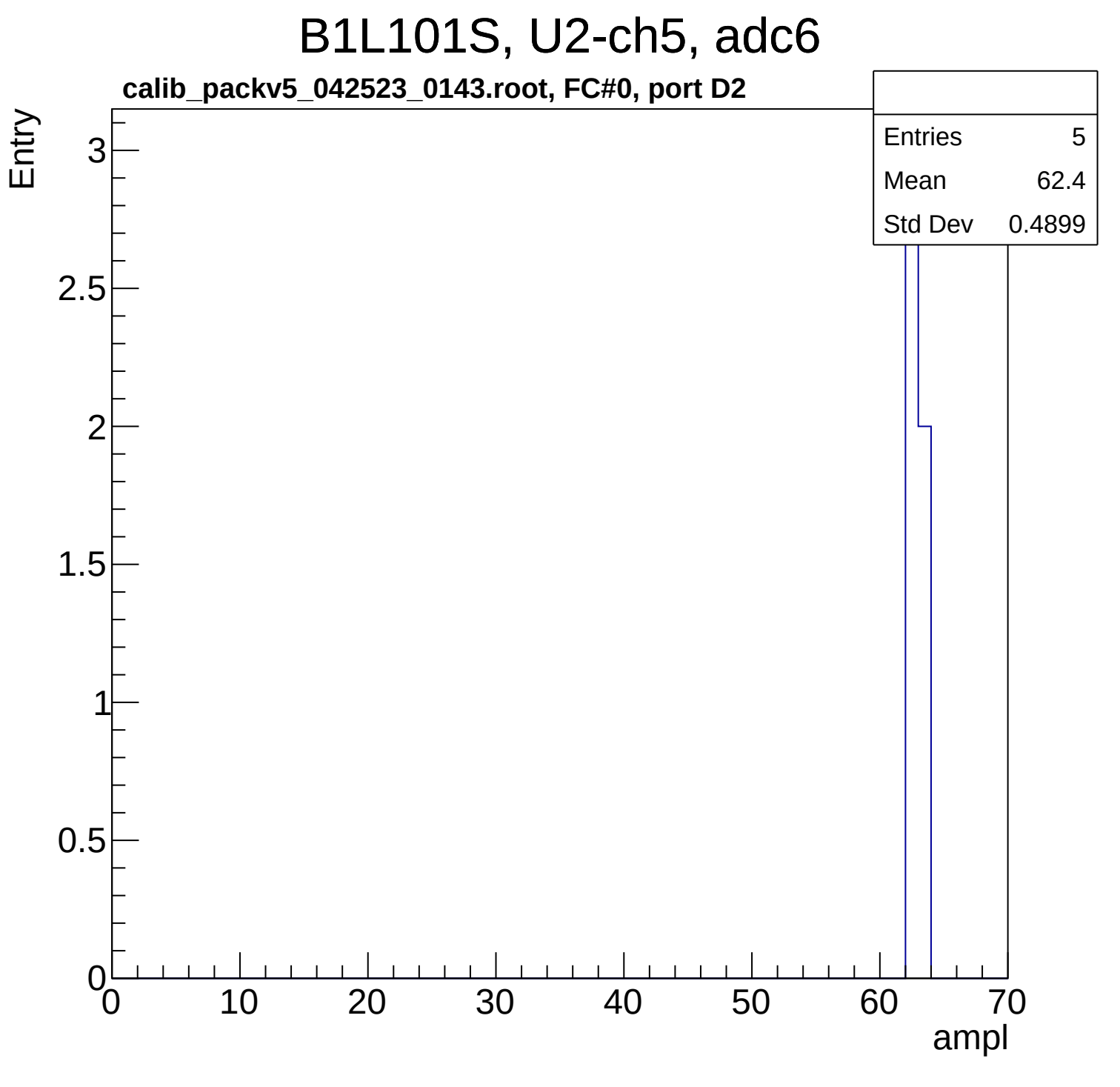

B1L101S, U2-ch5, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 82
Mean 36.04
Std Dev 3.304
Gaus mean : 36.5836
Gaus Width: 3.3773
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

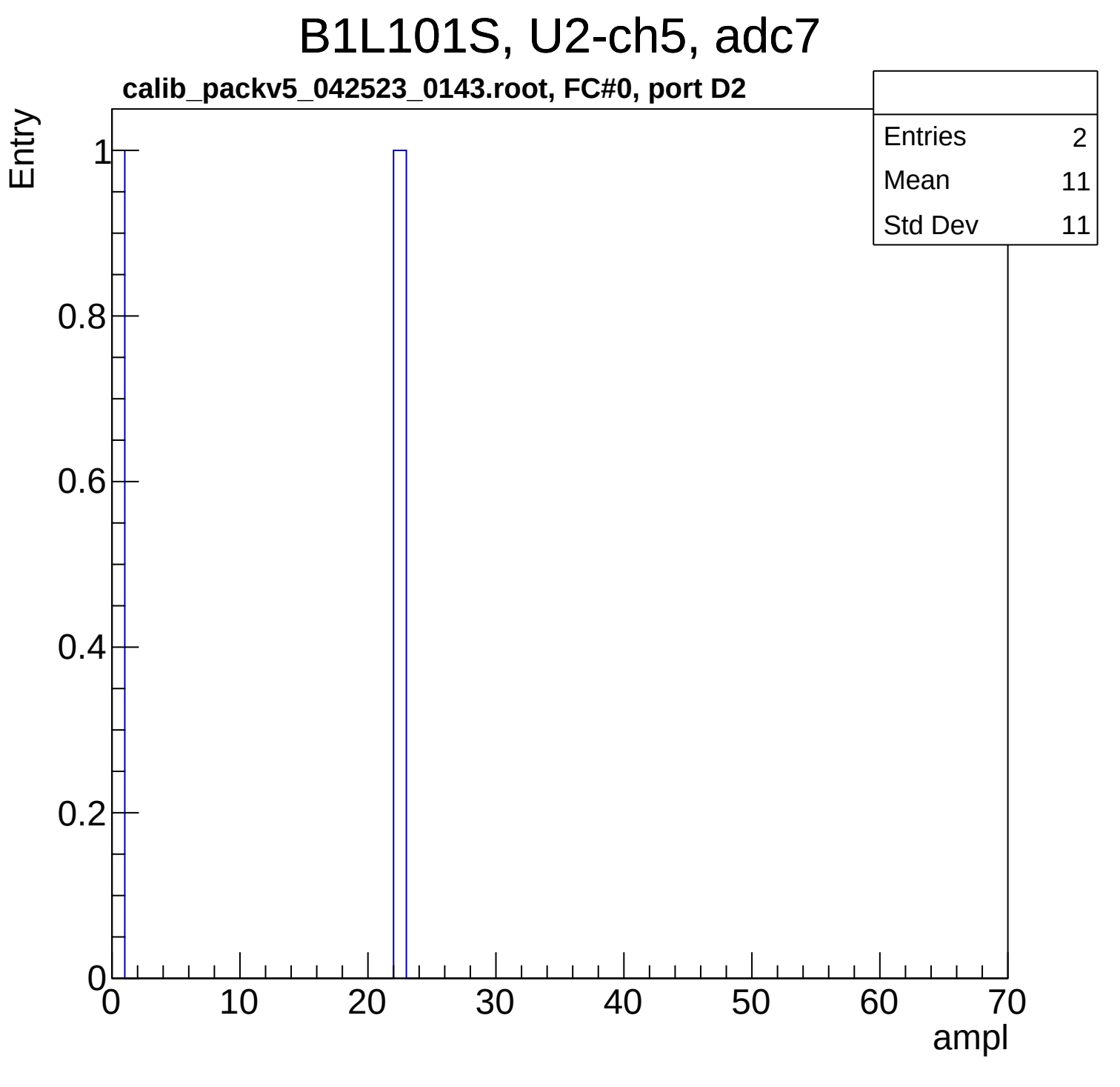

B1L101S, U2-ch5, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 44.23
Std Dev 3.199
Gaus mean : 44.6461
Gaus Width: 3.0974
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

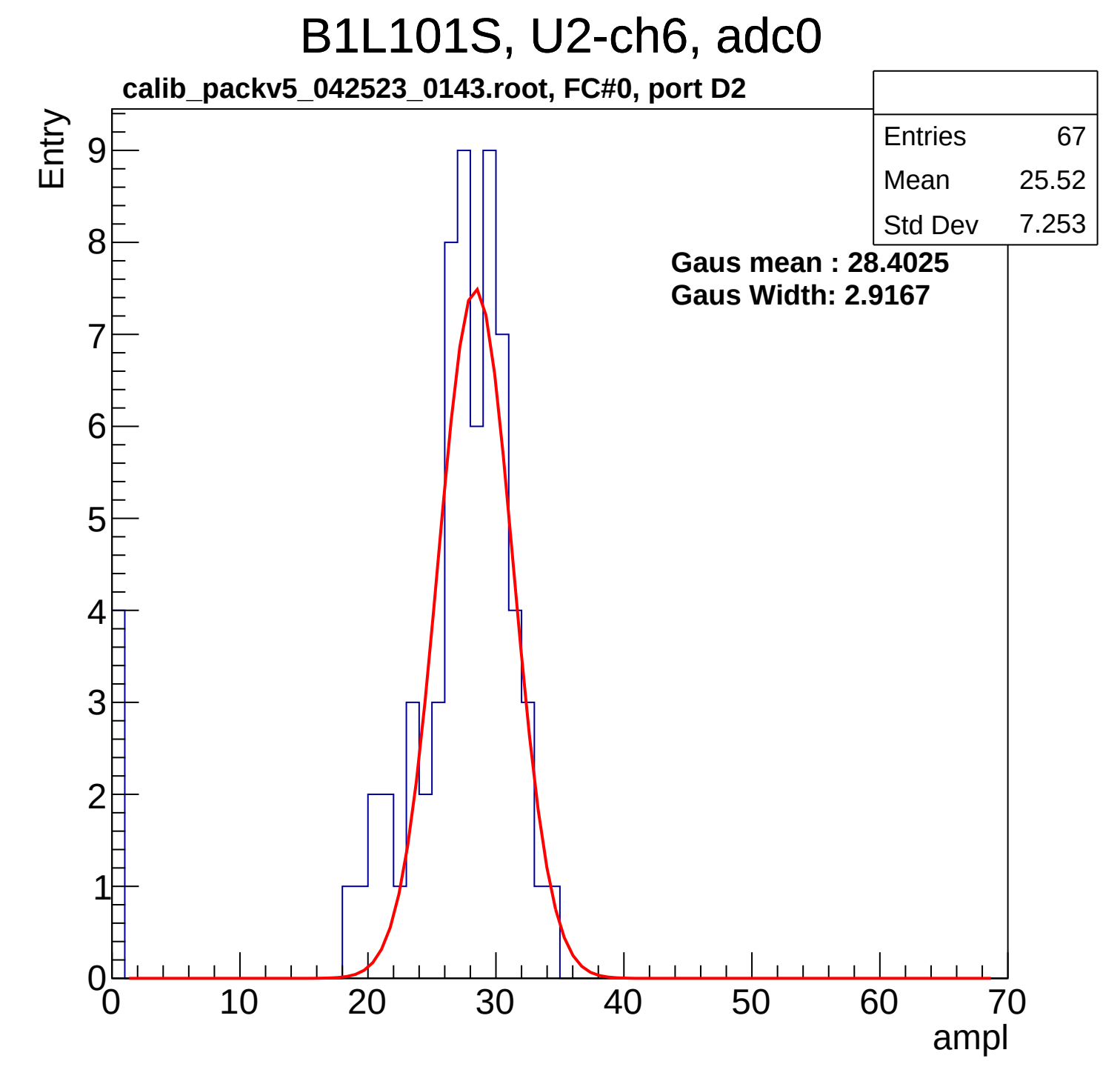

B1L101S, U2-ch5, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 50.68
Std Dev 3.107
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

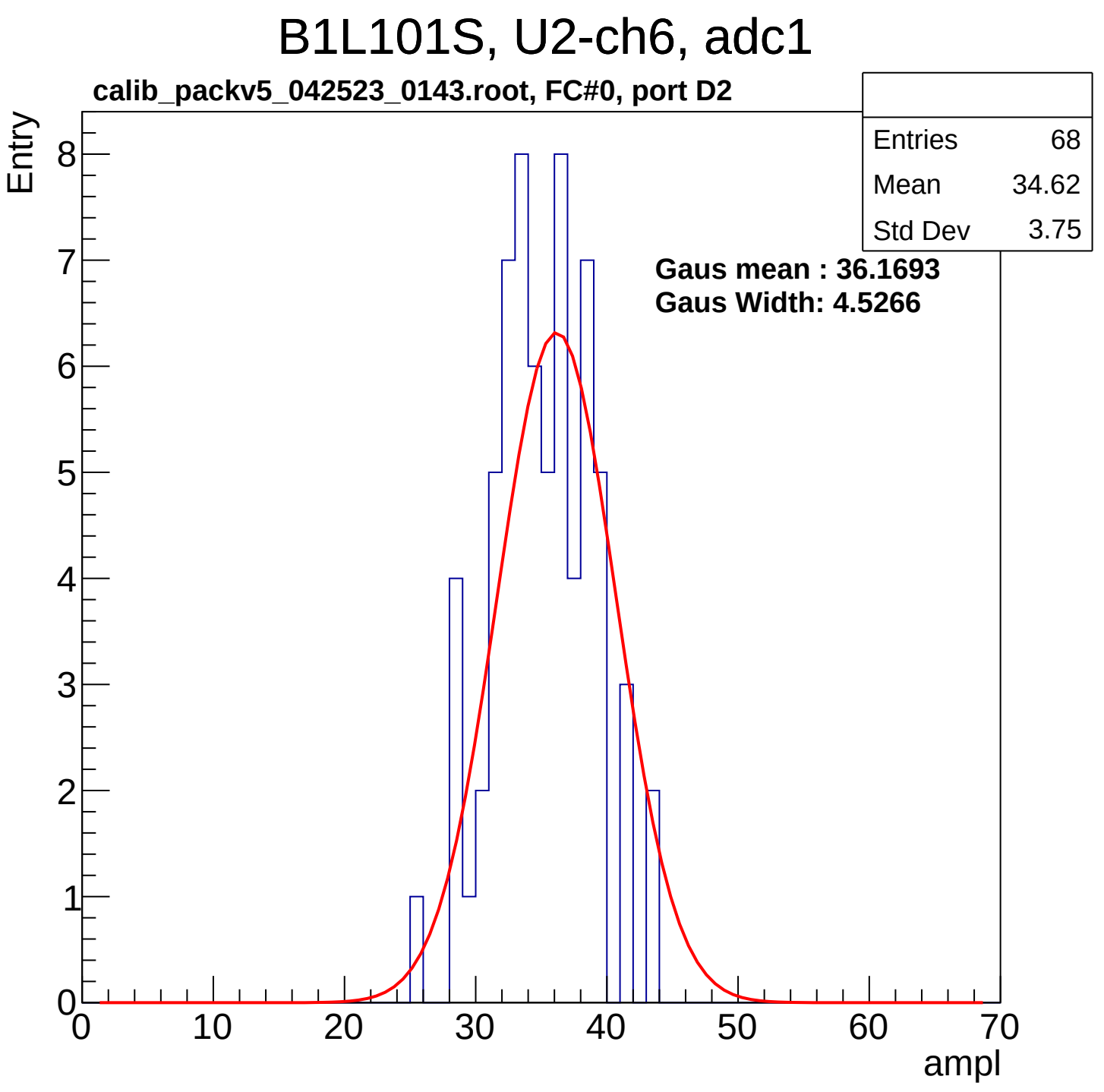

B1L101S, U2-ch5, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 56.29
Std Dev 3.642
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

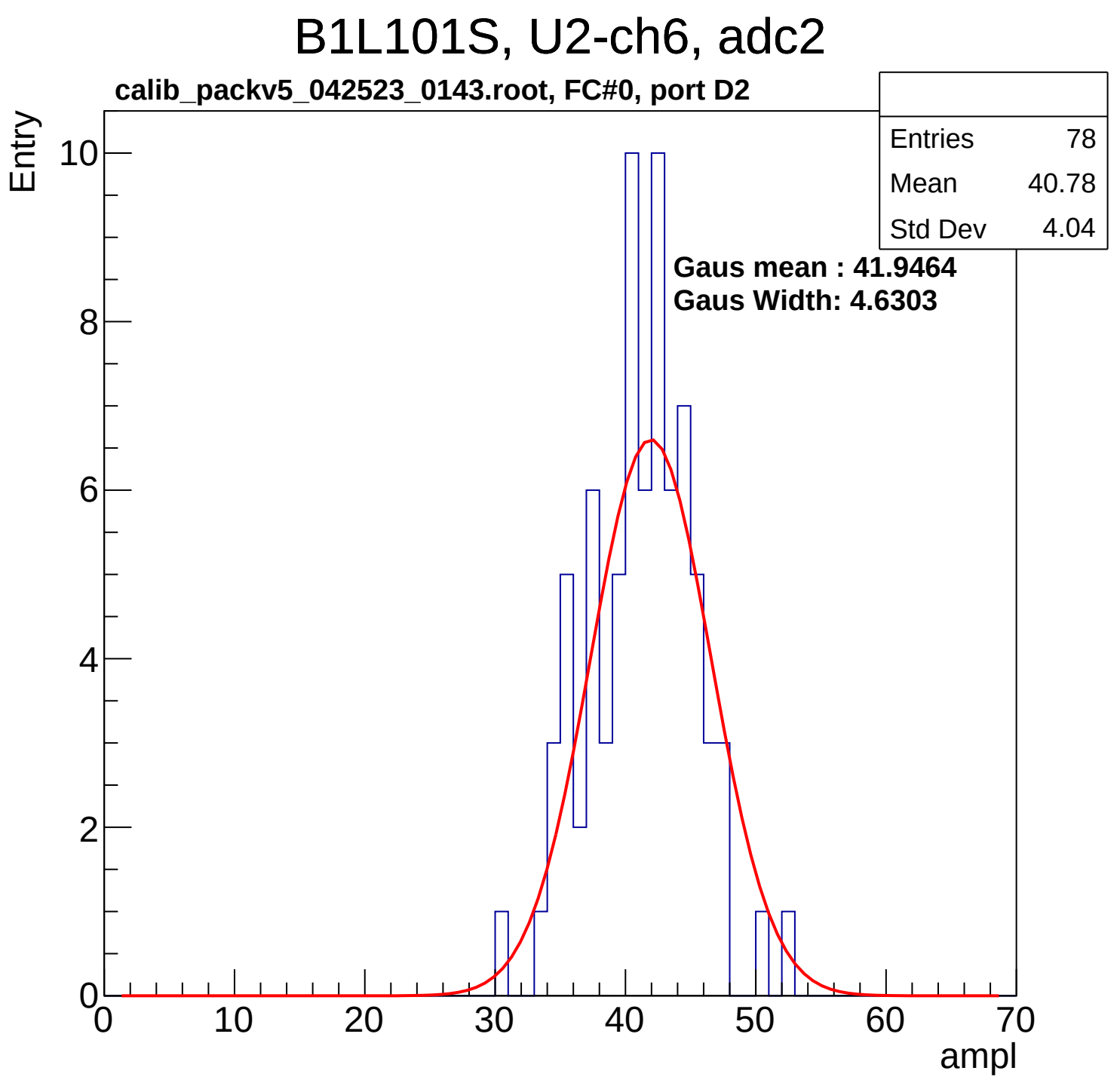

B1L101S, U2-ch5, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 33
Mean 58.39
Std Dev 10.63
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

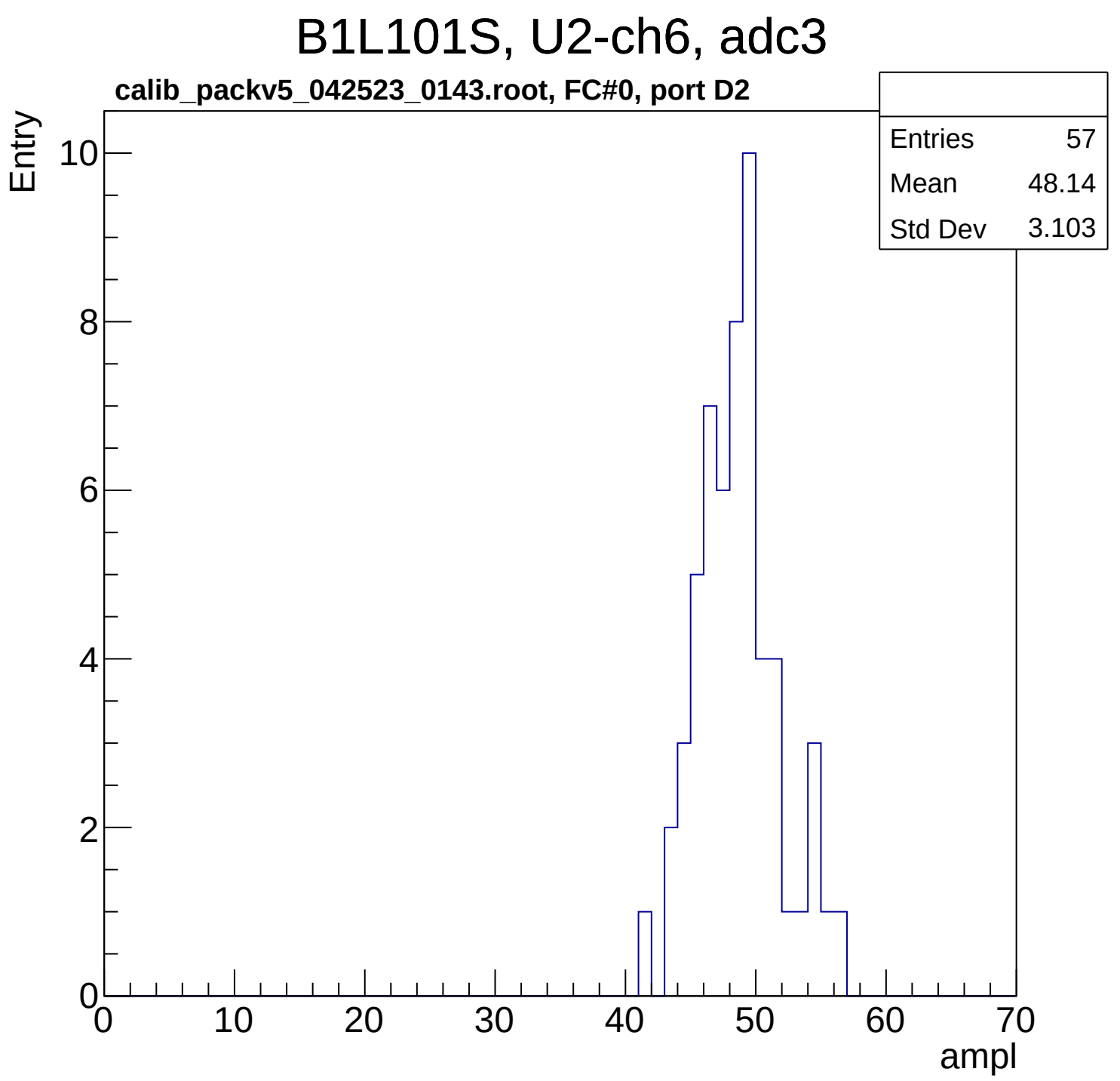

B1L101S, U2-ch5, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 62.4
Std Dev 0.4899
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

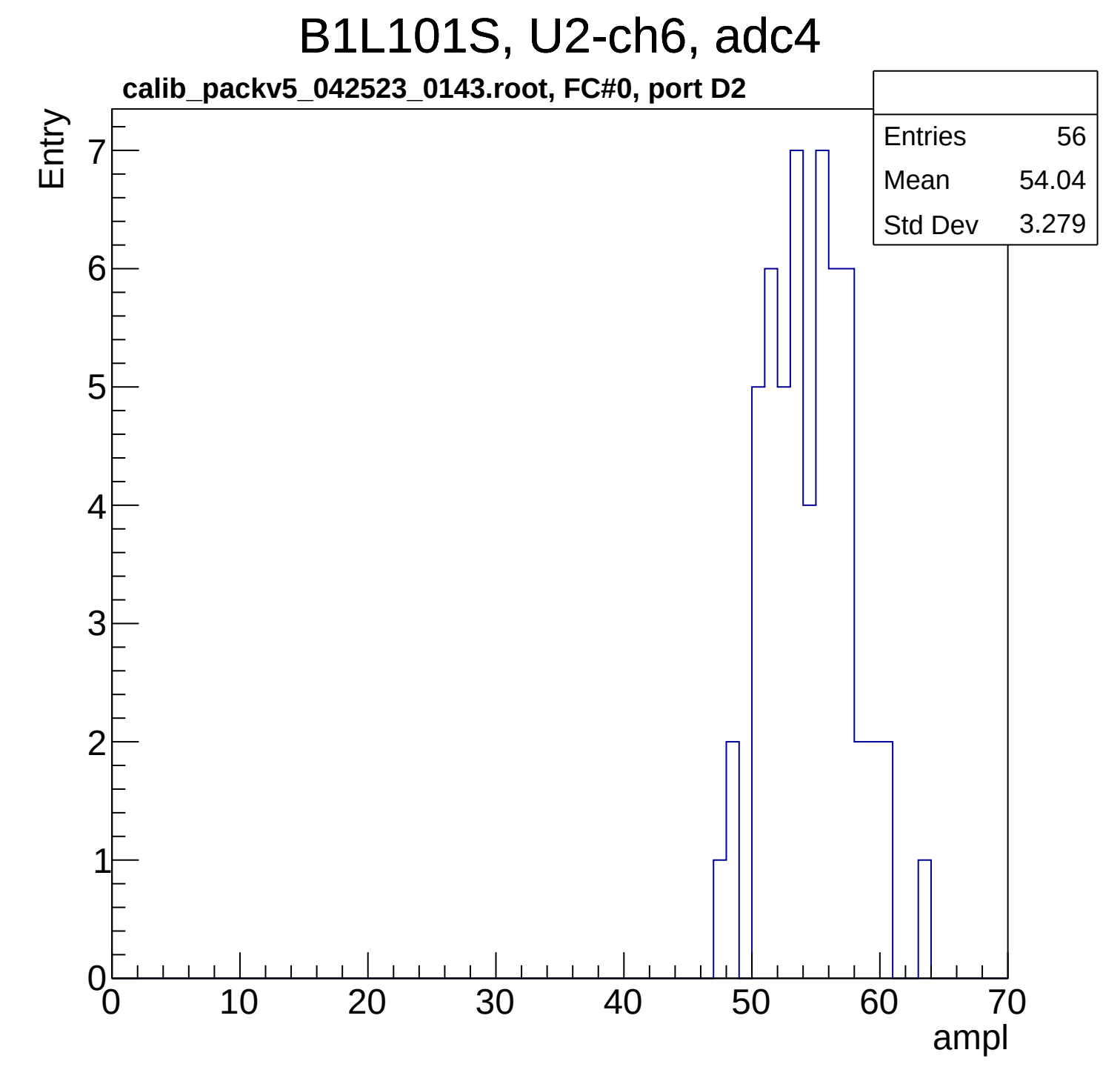

B1L101S, U2-ch5, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 11
Std Dev 11
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

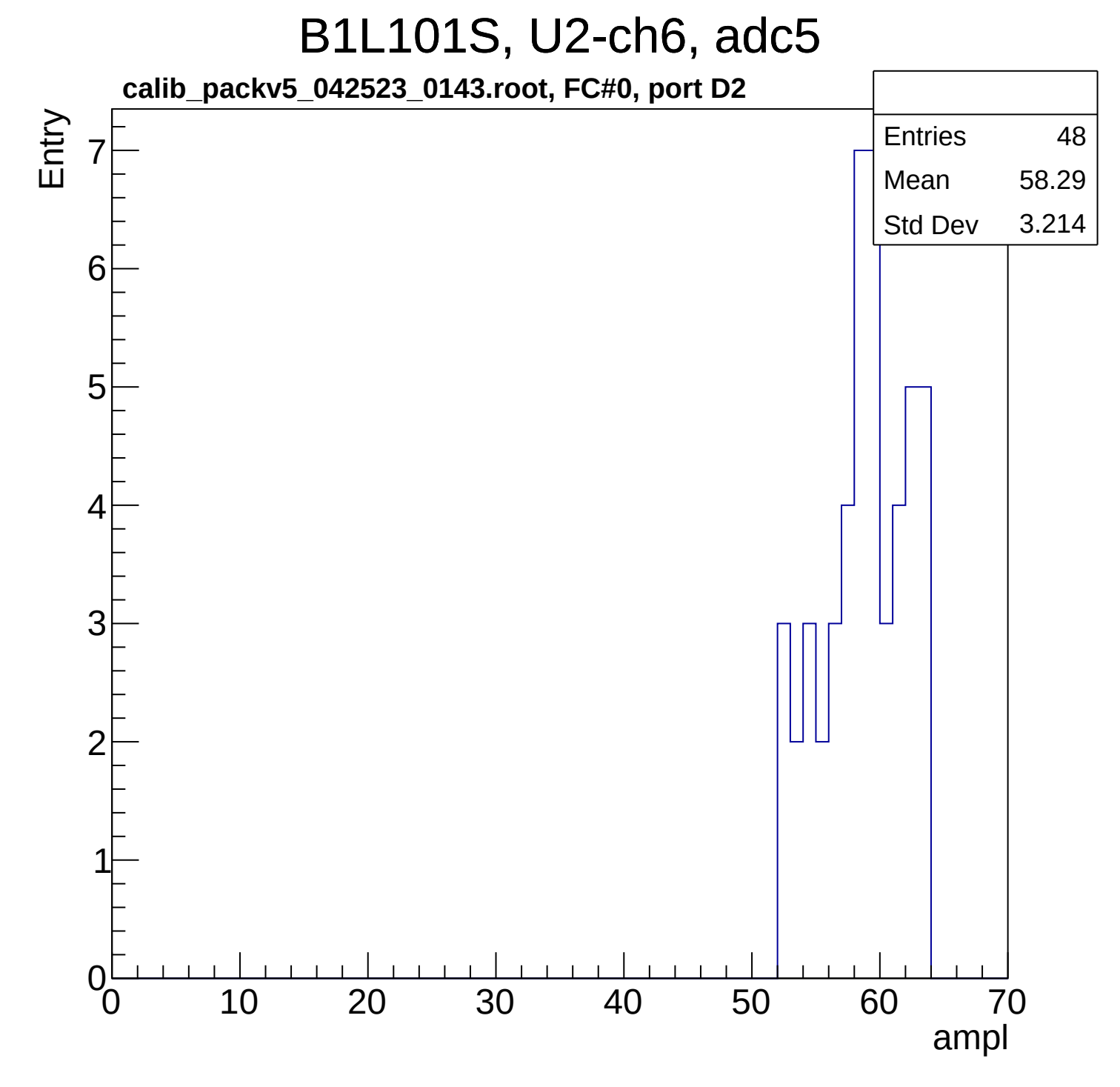

B1L101S, U2-ch6, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 25.52
Std Dev 7.253
Gaus mean : 28.4025
Gaus Width: 2.9167
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

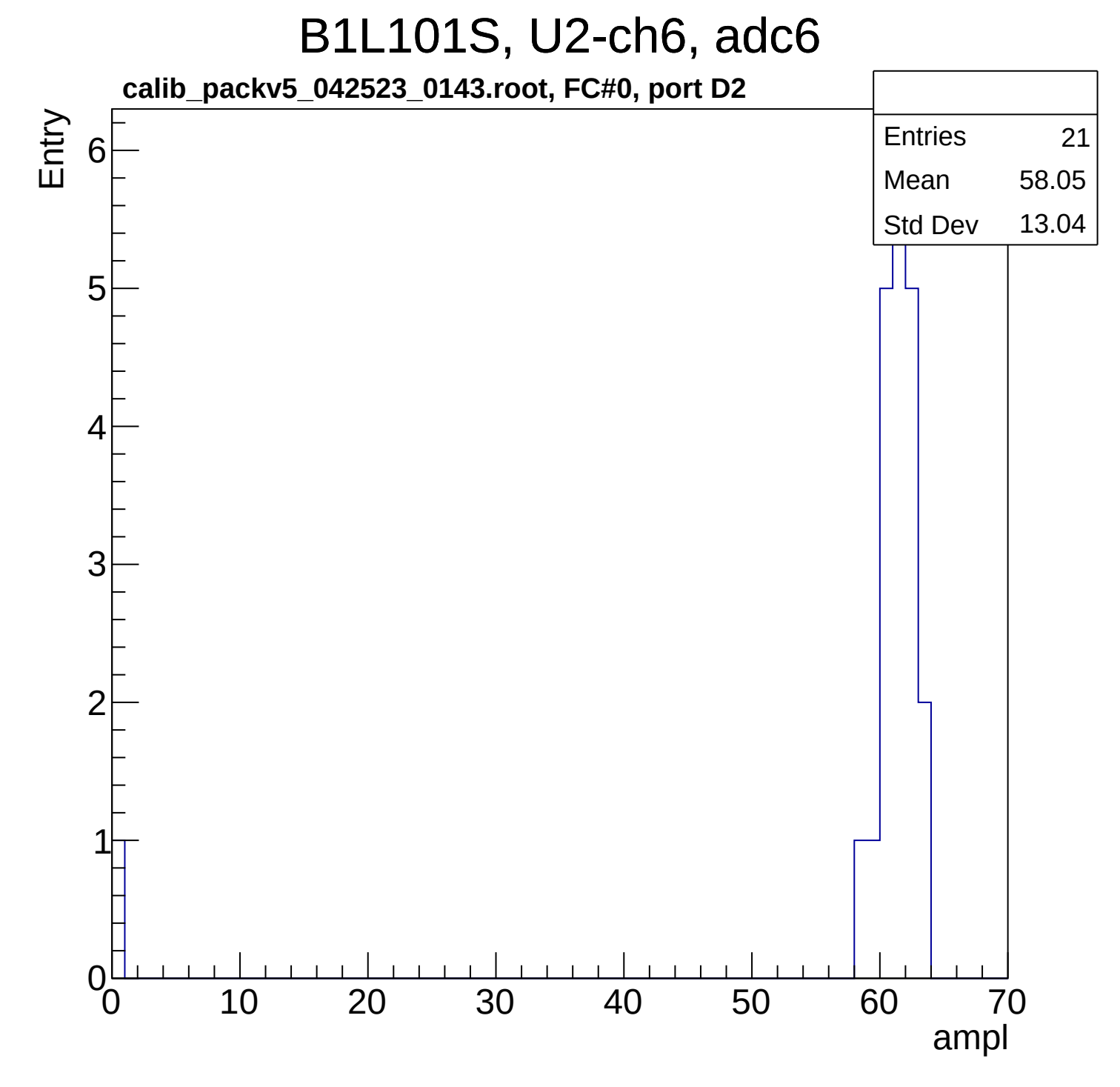

B1L101S, U2-ch6, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 34.62
Std Dev 3.75
Gaus mean : 36.1693
Gaus Width: 4.5266
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

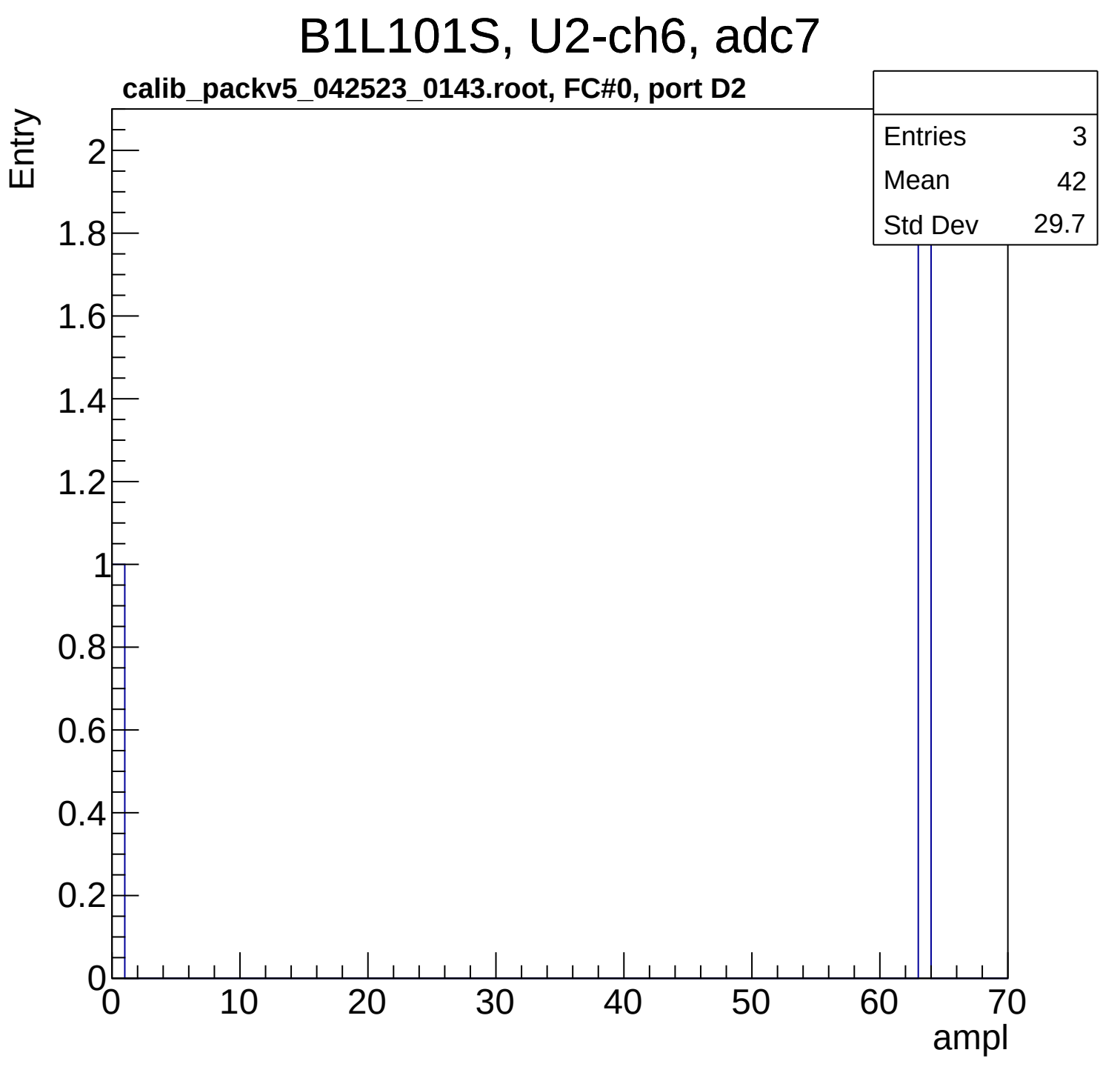

B1L101S, U2-ch6, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 40.78
Std Dev 4.04
Gaus mean : 41.9464
Gaus Width: 4.6303
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

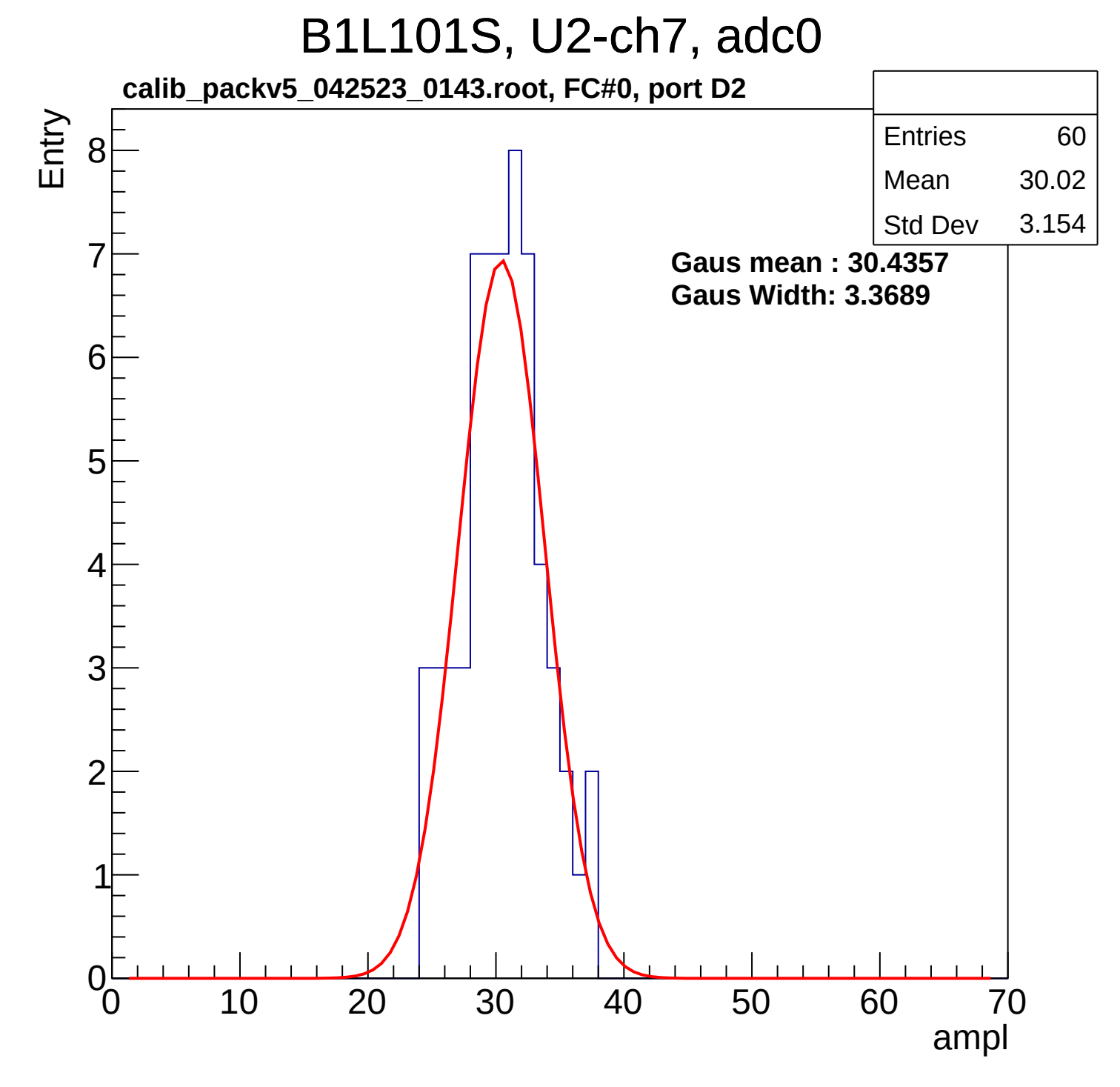

B1L101S, U2-ch6, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 48.14
Std Dev 3.103
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

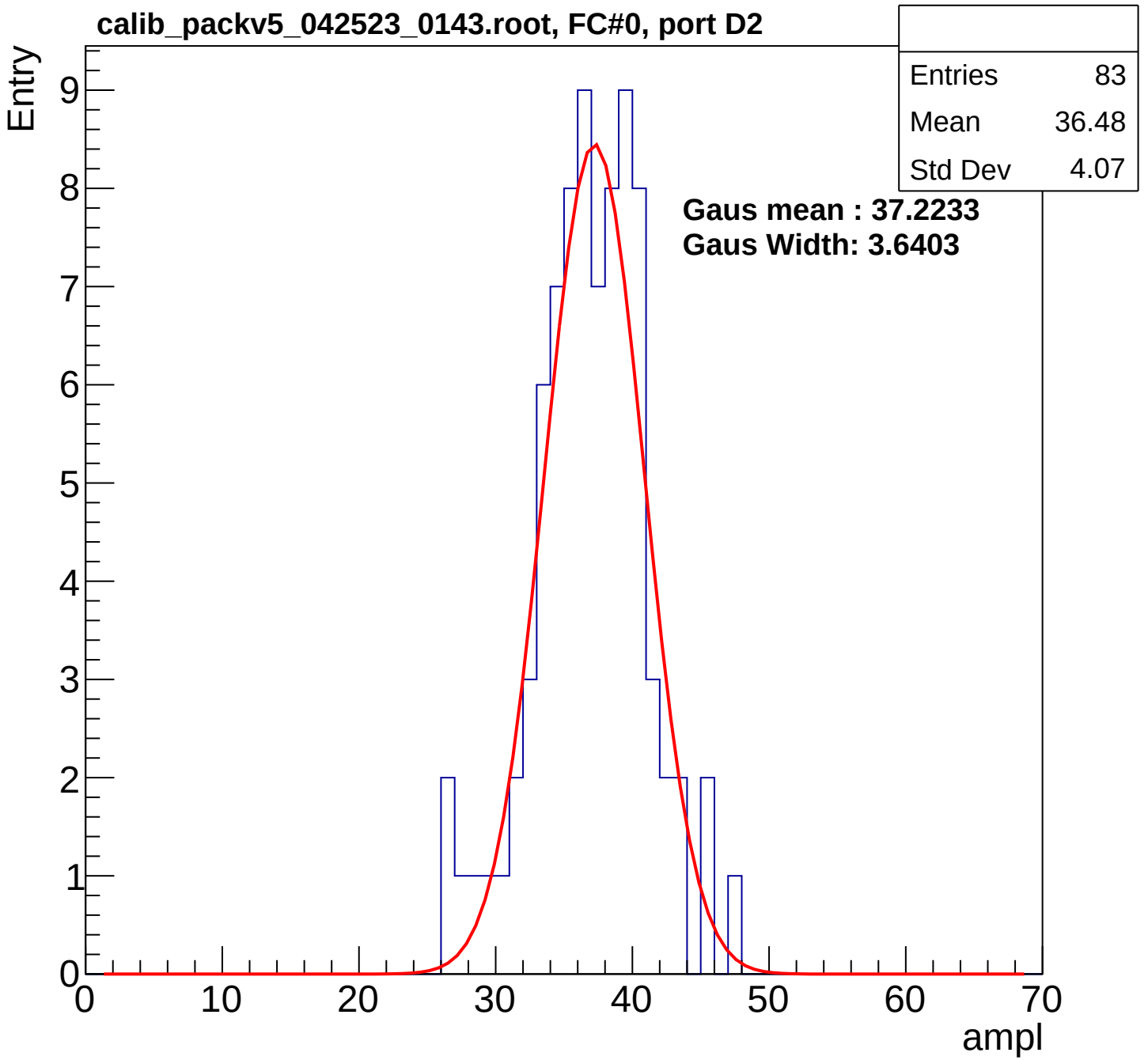

B1L101S, U2-ch6, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 54.04
Std Dev 3.279
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

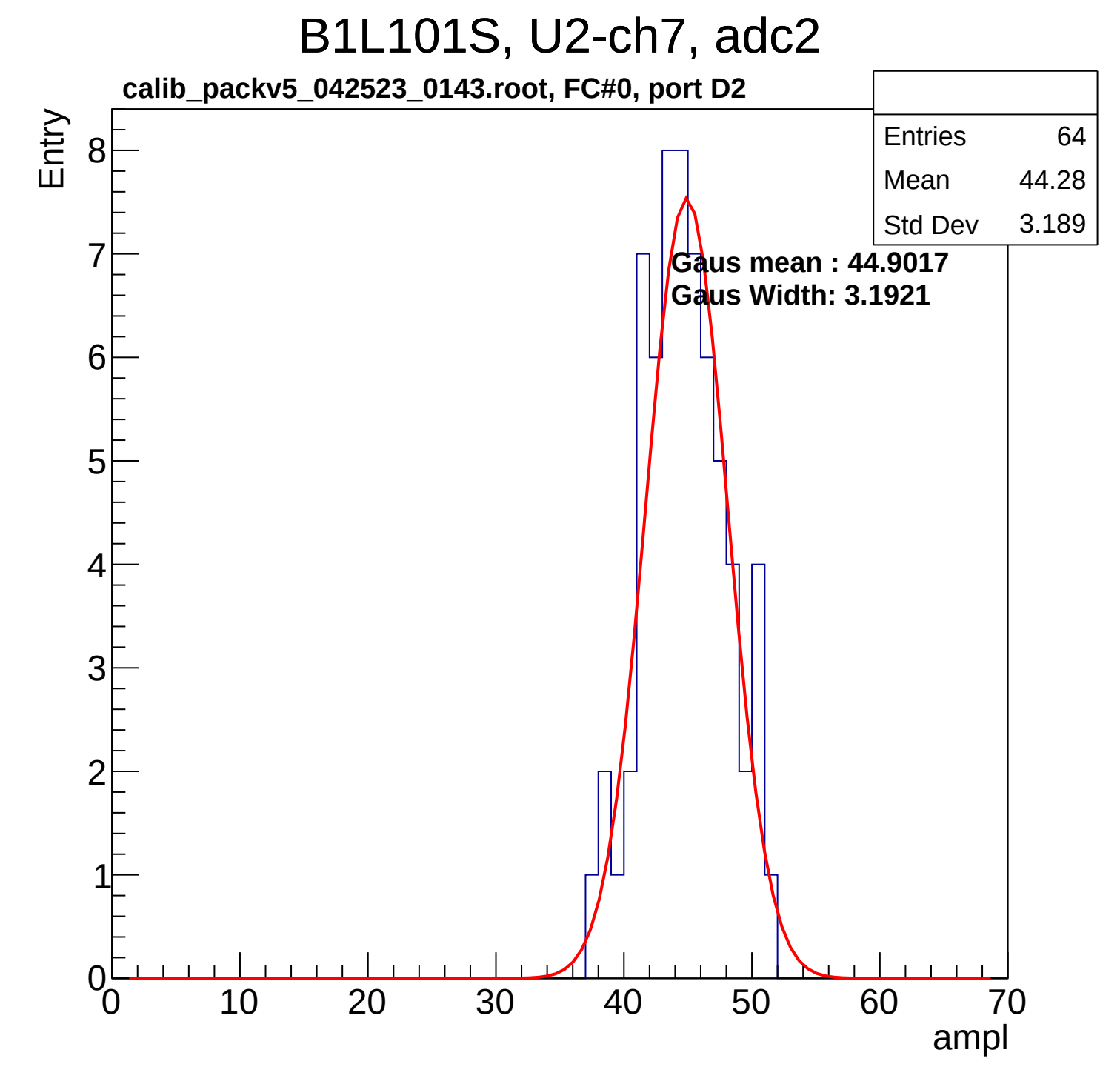

B1L101S, U2-ch6, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 58.29
Std Dev 3.214
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

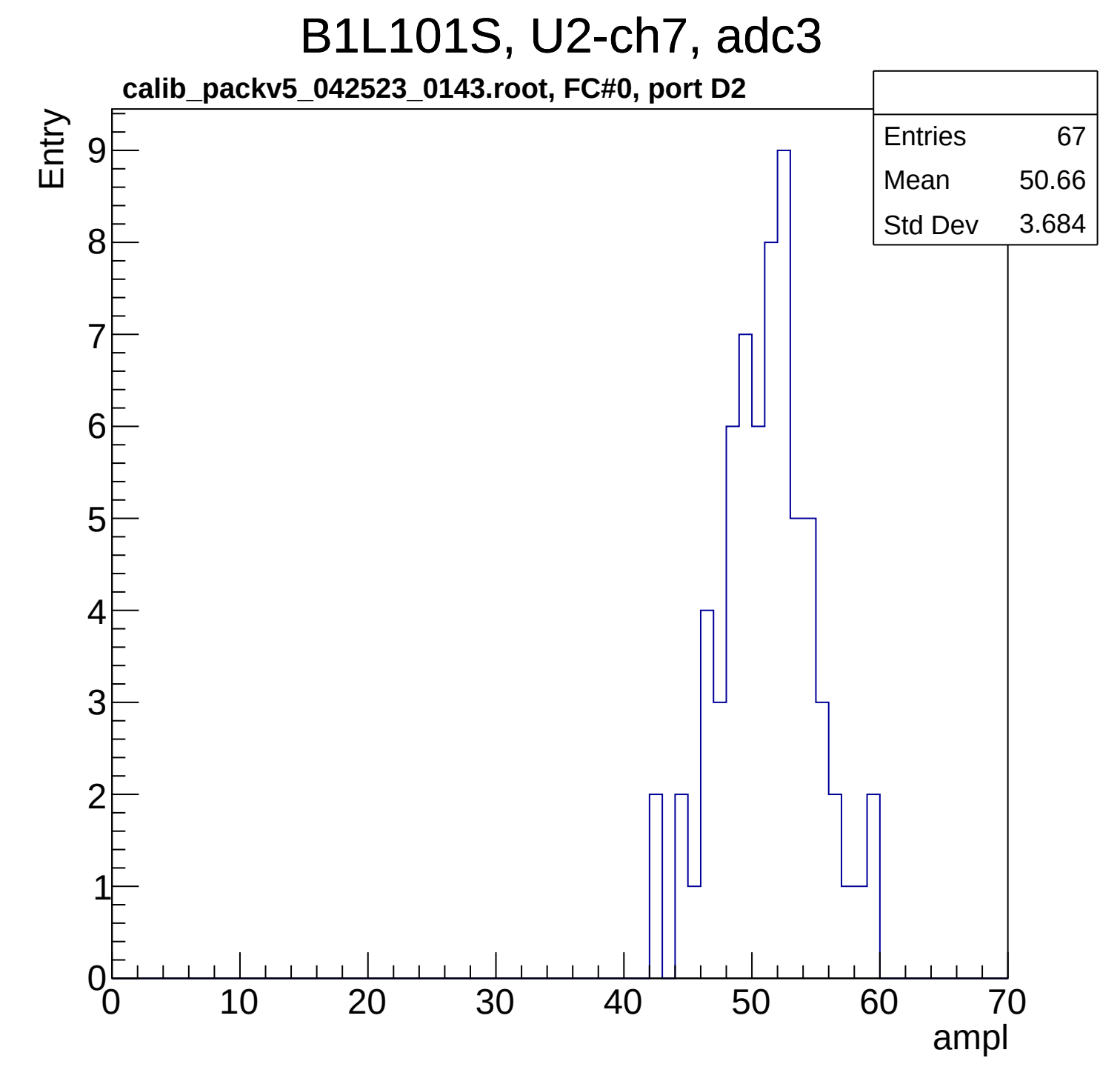

B1L101S, U2-ch6, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 21
Mean 58.05
Std Dev 13.04
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

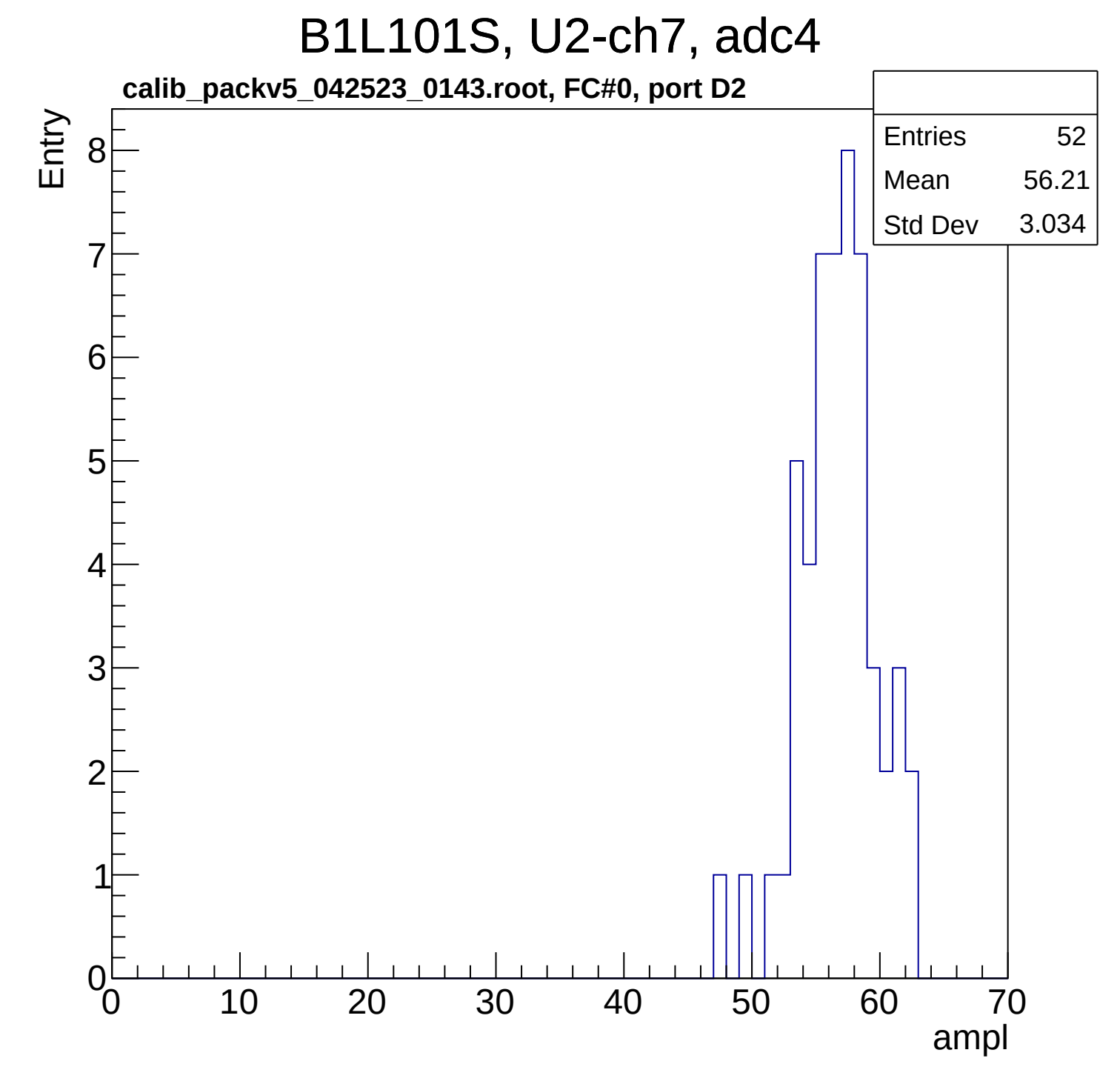

B1L101S, U2-ch6, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 42
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

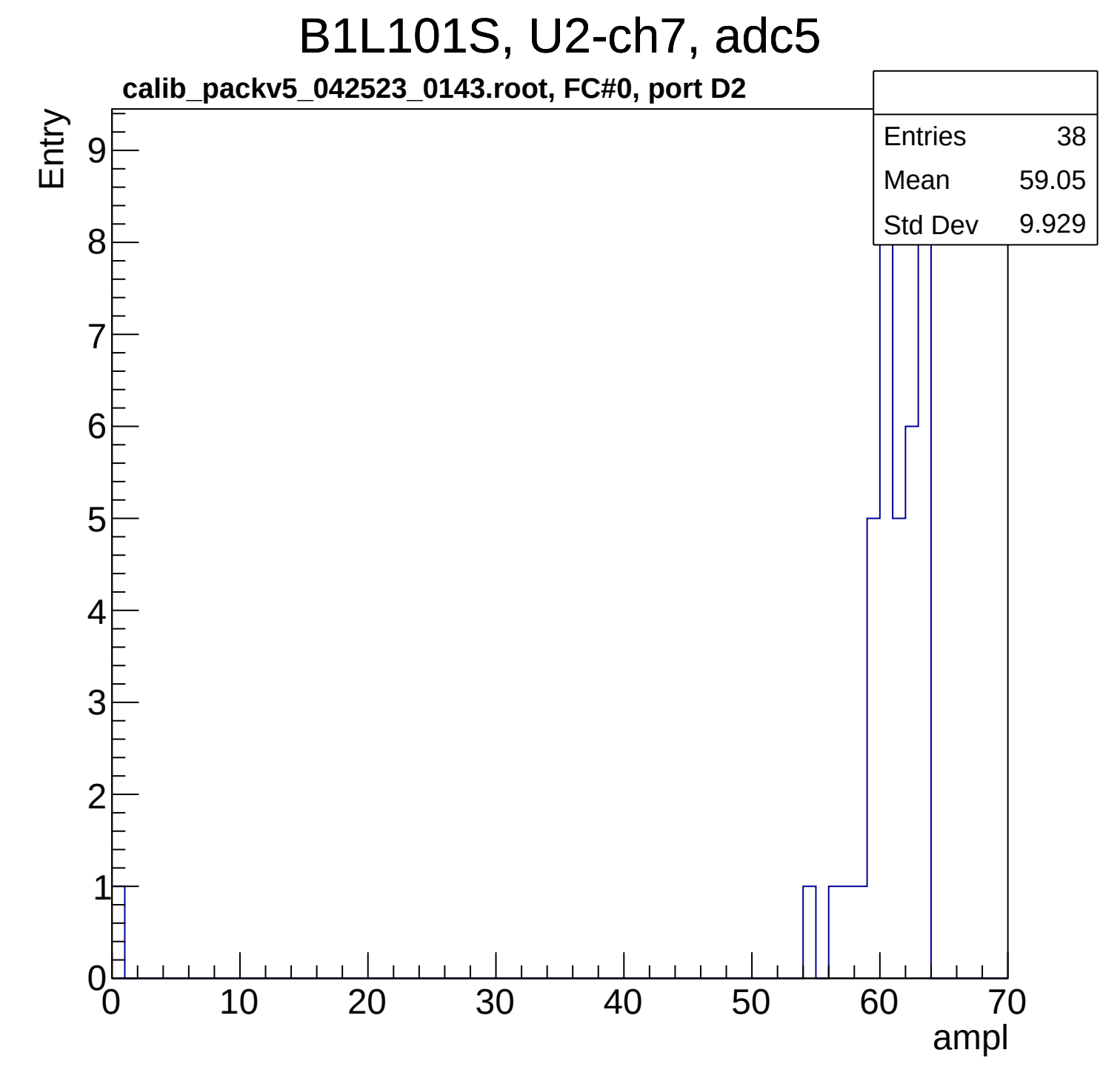

B1L101S, U2-ch7, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 30.02
Std Dev 3.154
Gaus mean : 30.4357
Gaus Width: 3.3689
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

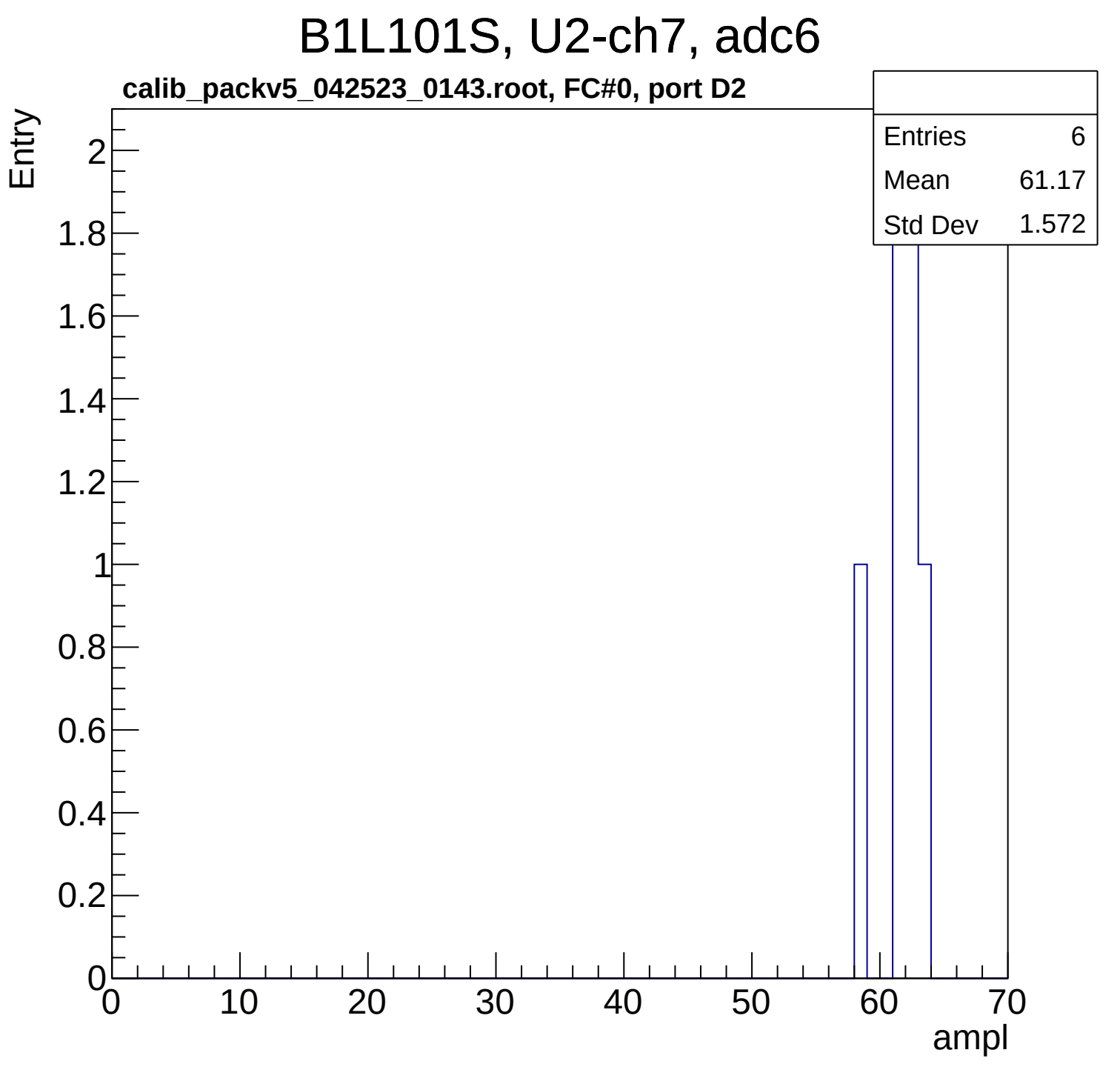

B1L101S, U2-ch7, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 83
Mean 36.48
Std Dev 4.07
Gaus mean : 37.2233
Gaus Width: 3.6403
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

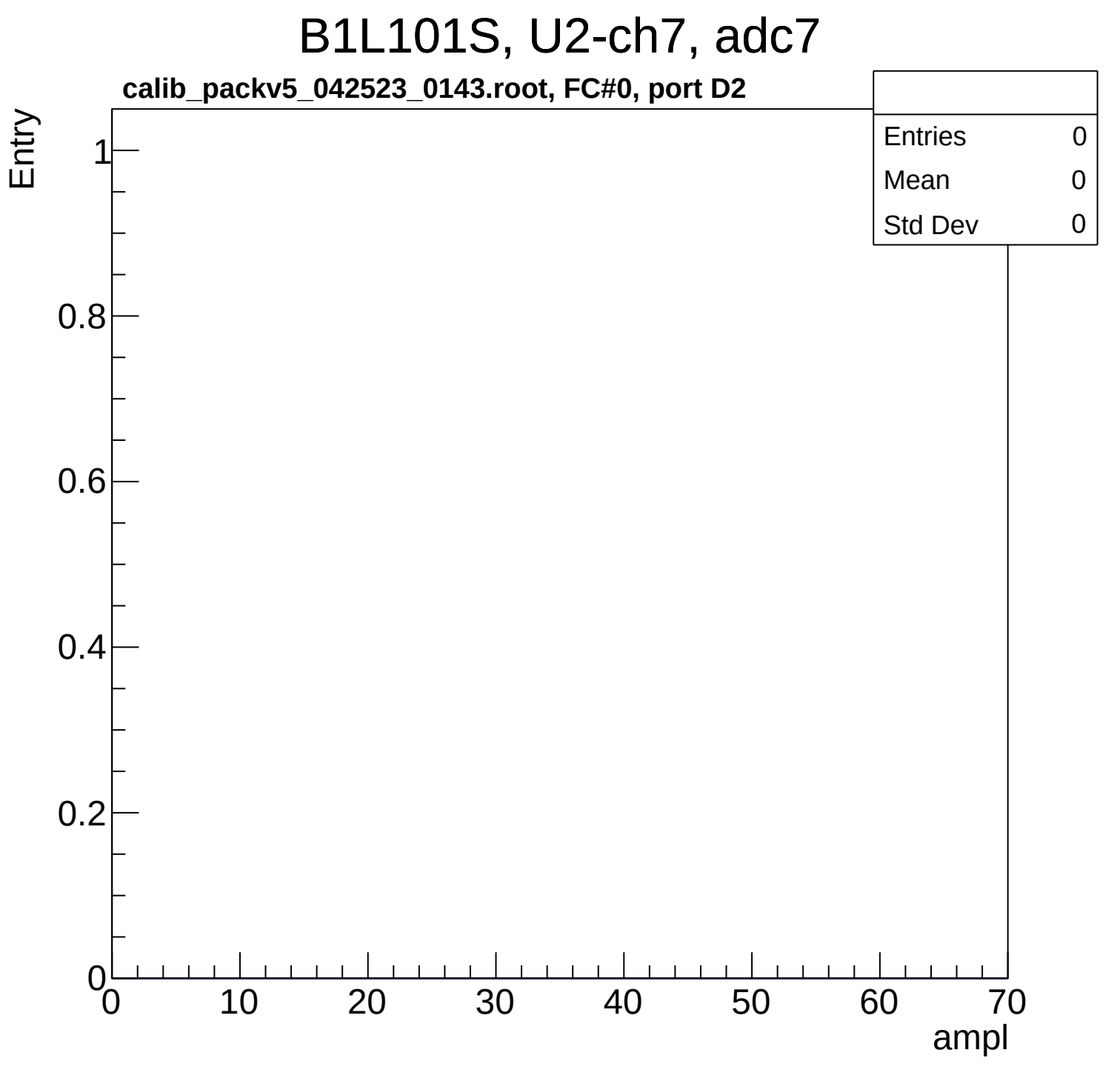

B1L101S, U2-ch7, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 44.28
Std Dev 3.189
Gaus mean : 44.9017
Gaus Width: 3.1921
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

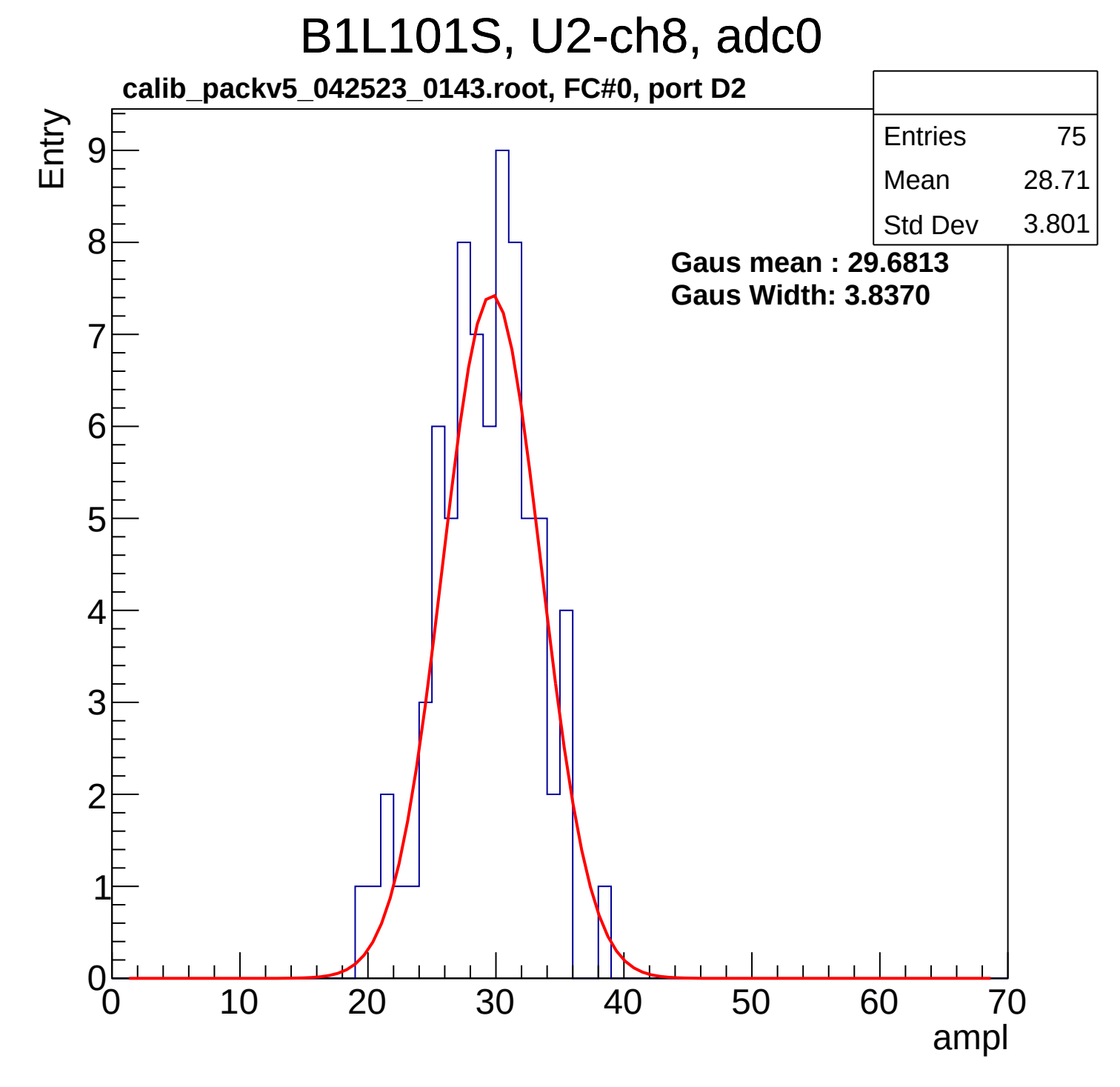

B1L101S, U2-ch7, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 50.66
Std Dev 3.684
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

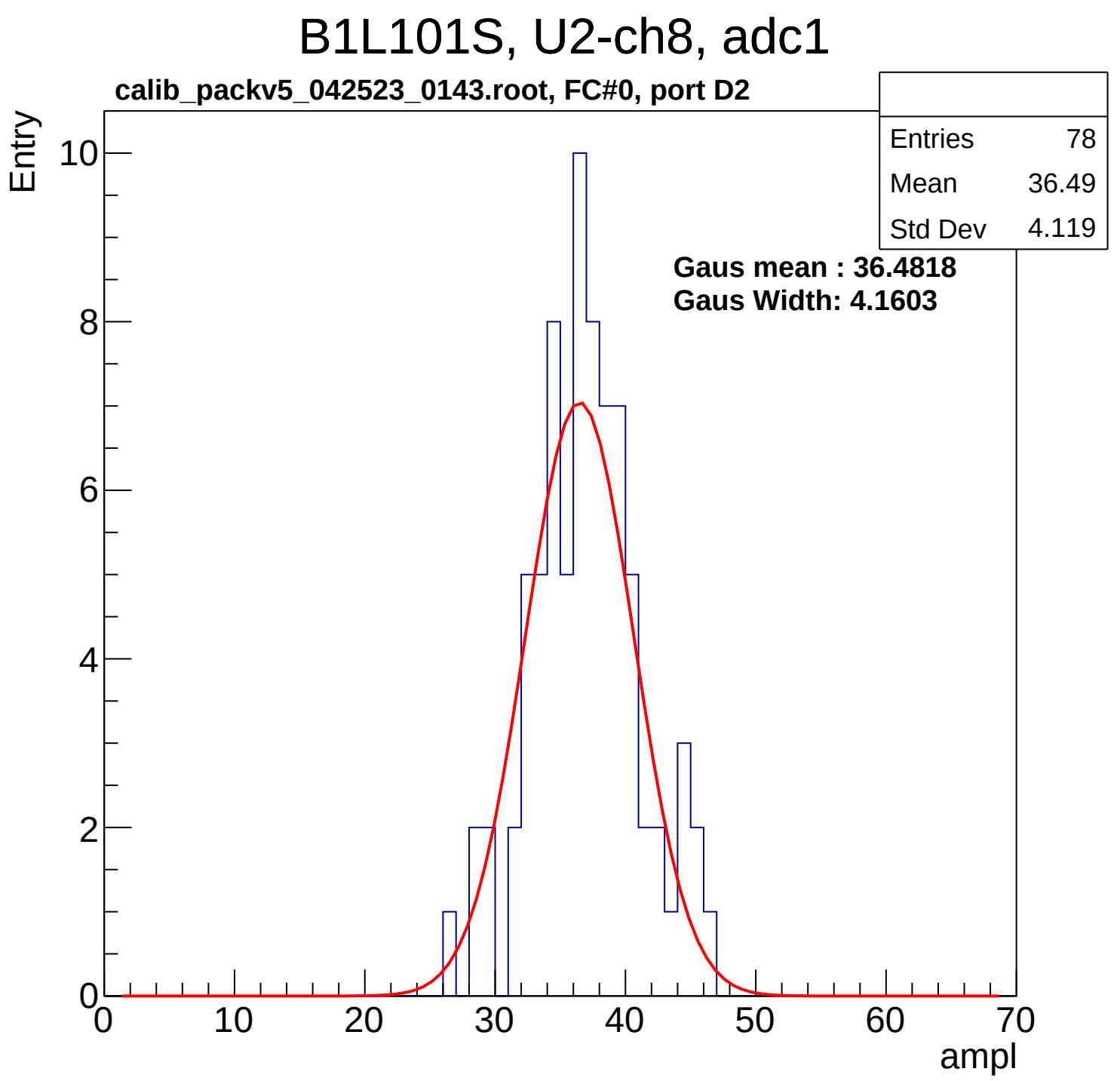

B1L101S, U2-ch7, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 56.21
Std Dev 3.034
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

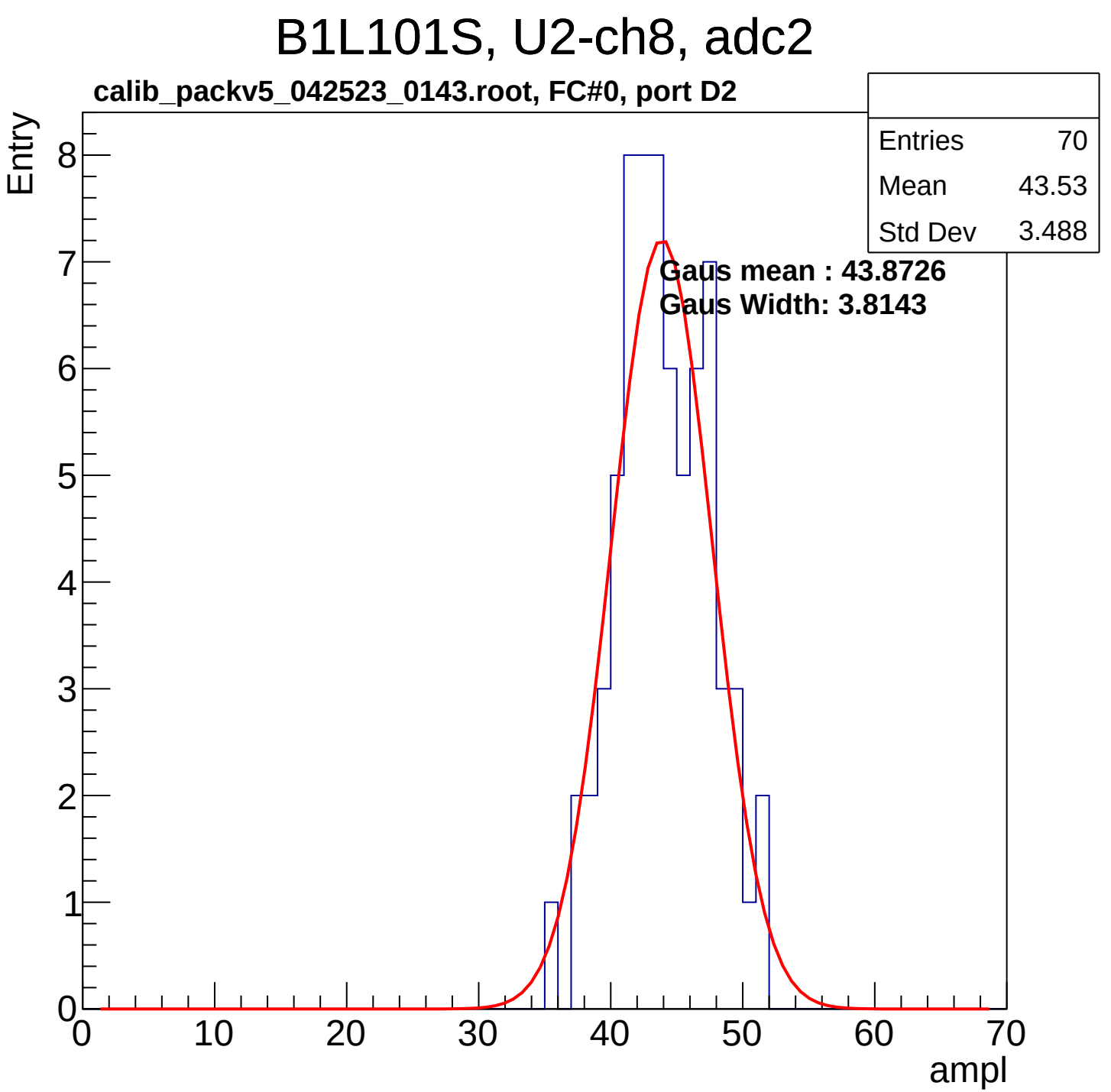

B1L101S, U2-ch7, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 38
Mean 59.05
Std Dev 9.929
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

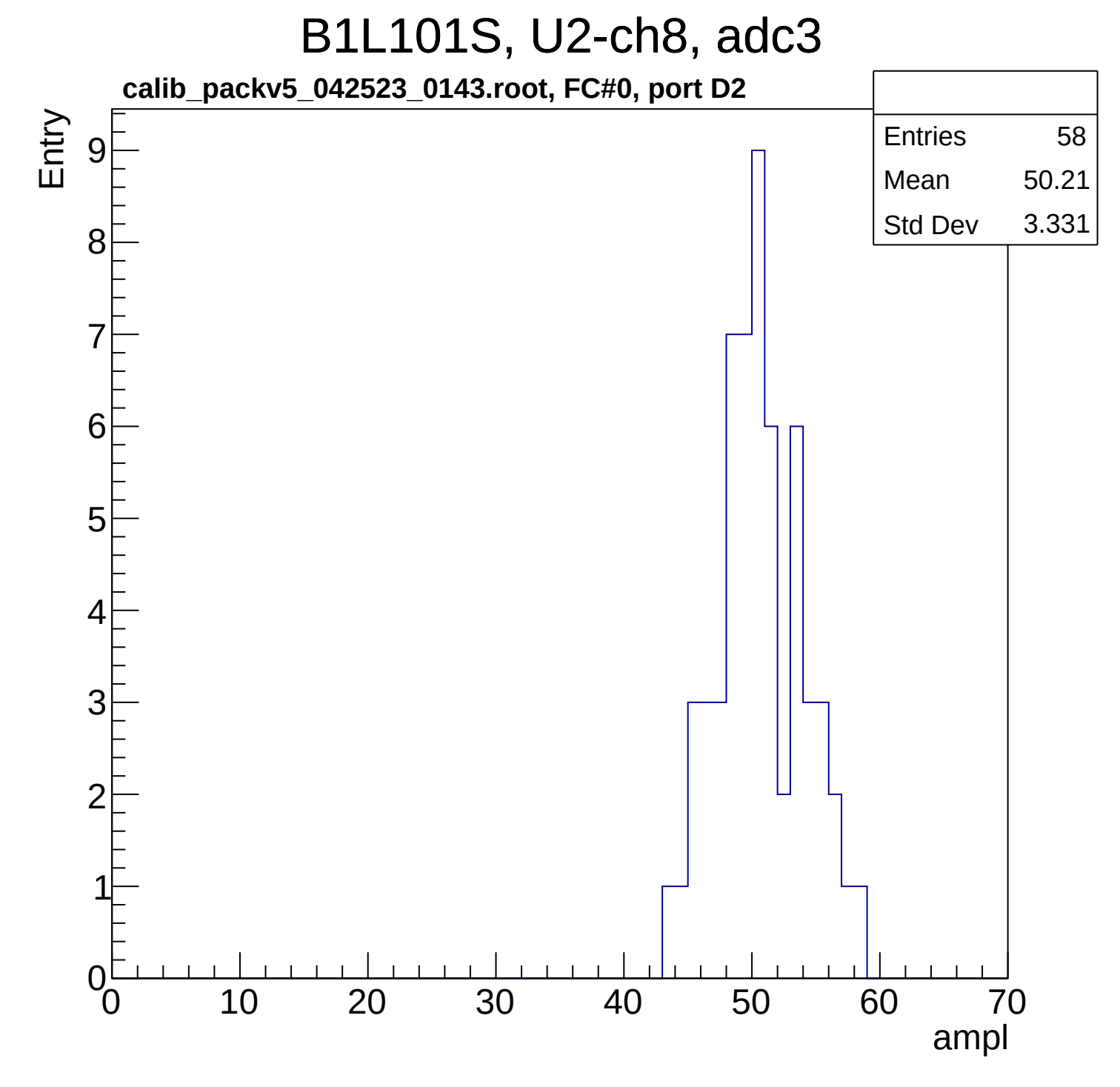

B1L101S, U2-ch7, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 61.17
Std Dev 1.572
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

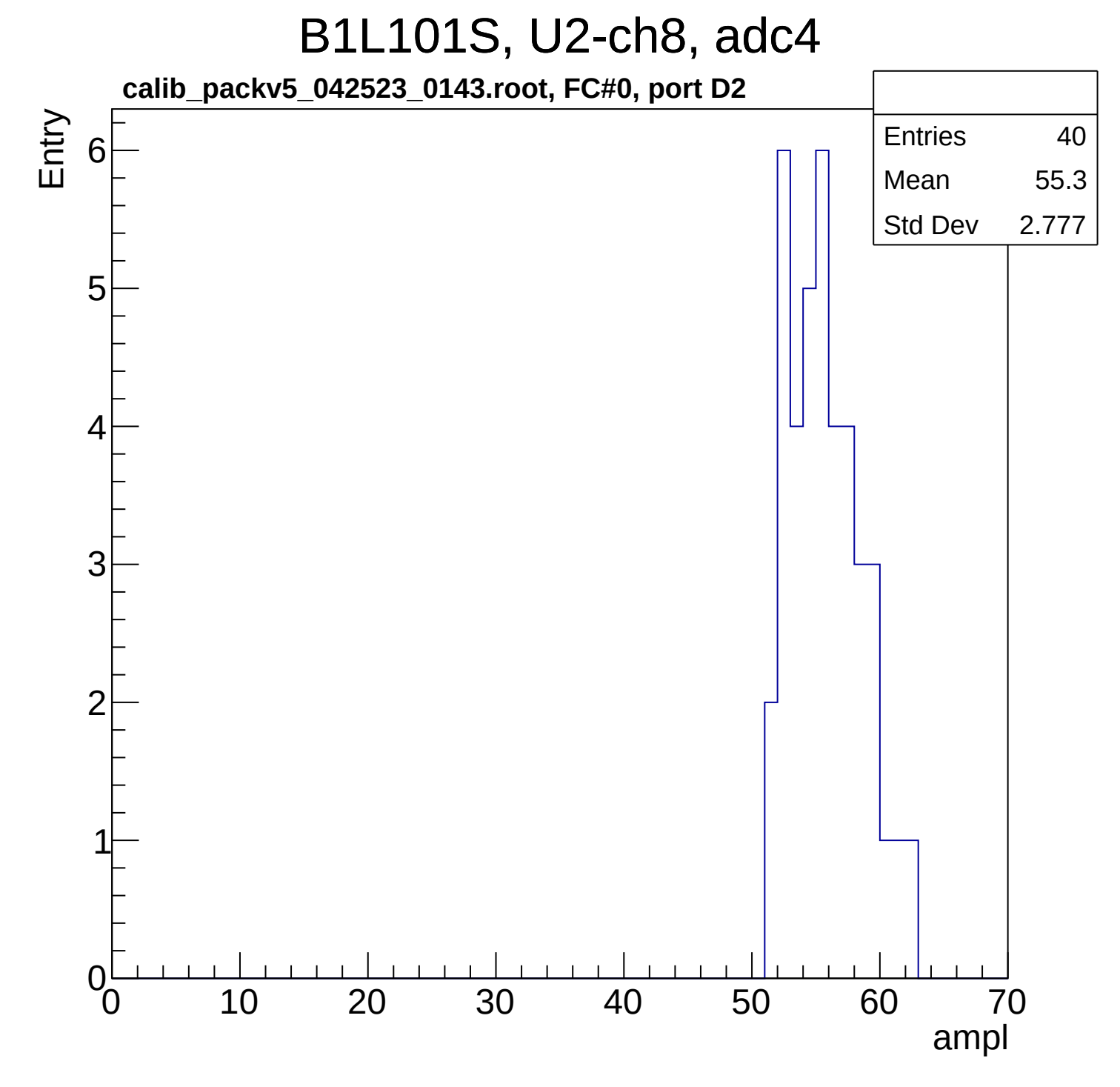

B1L101S, U2-ch7, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

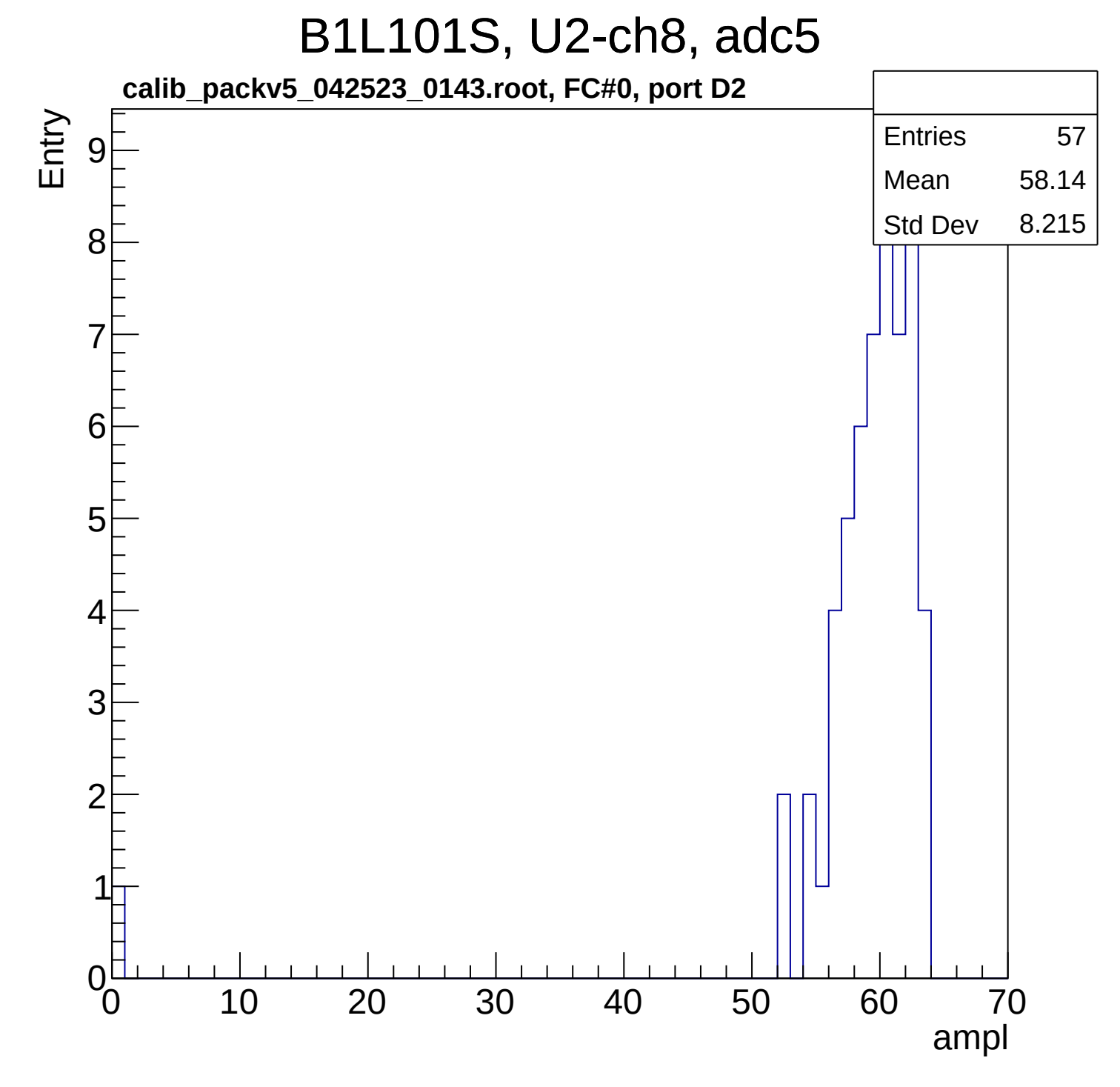

B1L101S, U2-ch8, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 28.71
Std Dev 3.801
Gaus mean : 29.6813
Gaus Width: 3.8370
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

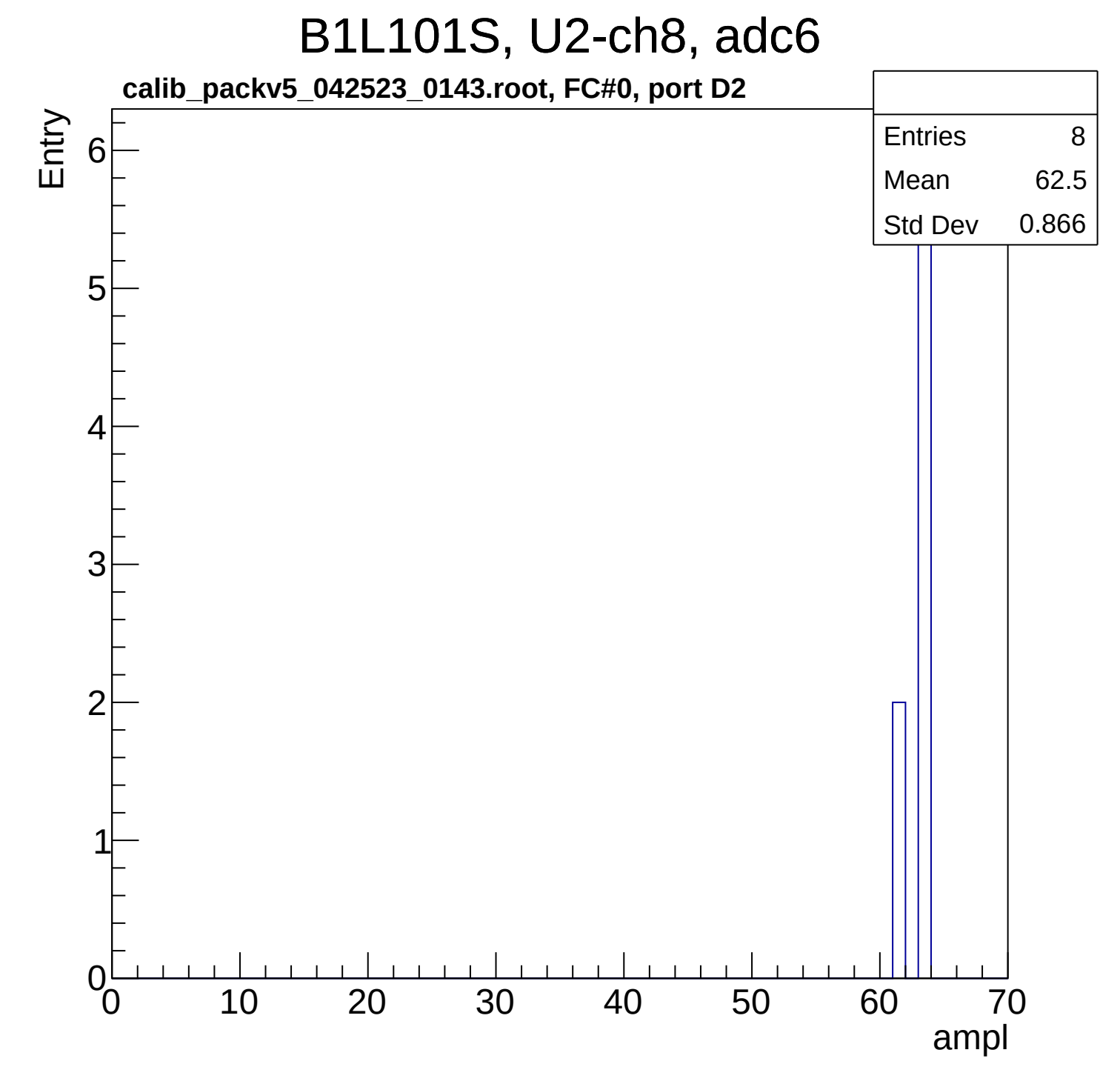

B1L101S, U2-ch8, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 36.49
Std Dev 4.119
Gaus mean : 36.4818
Gaus Width: 4.1603
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

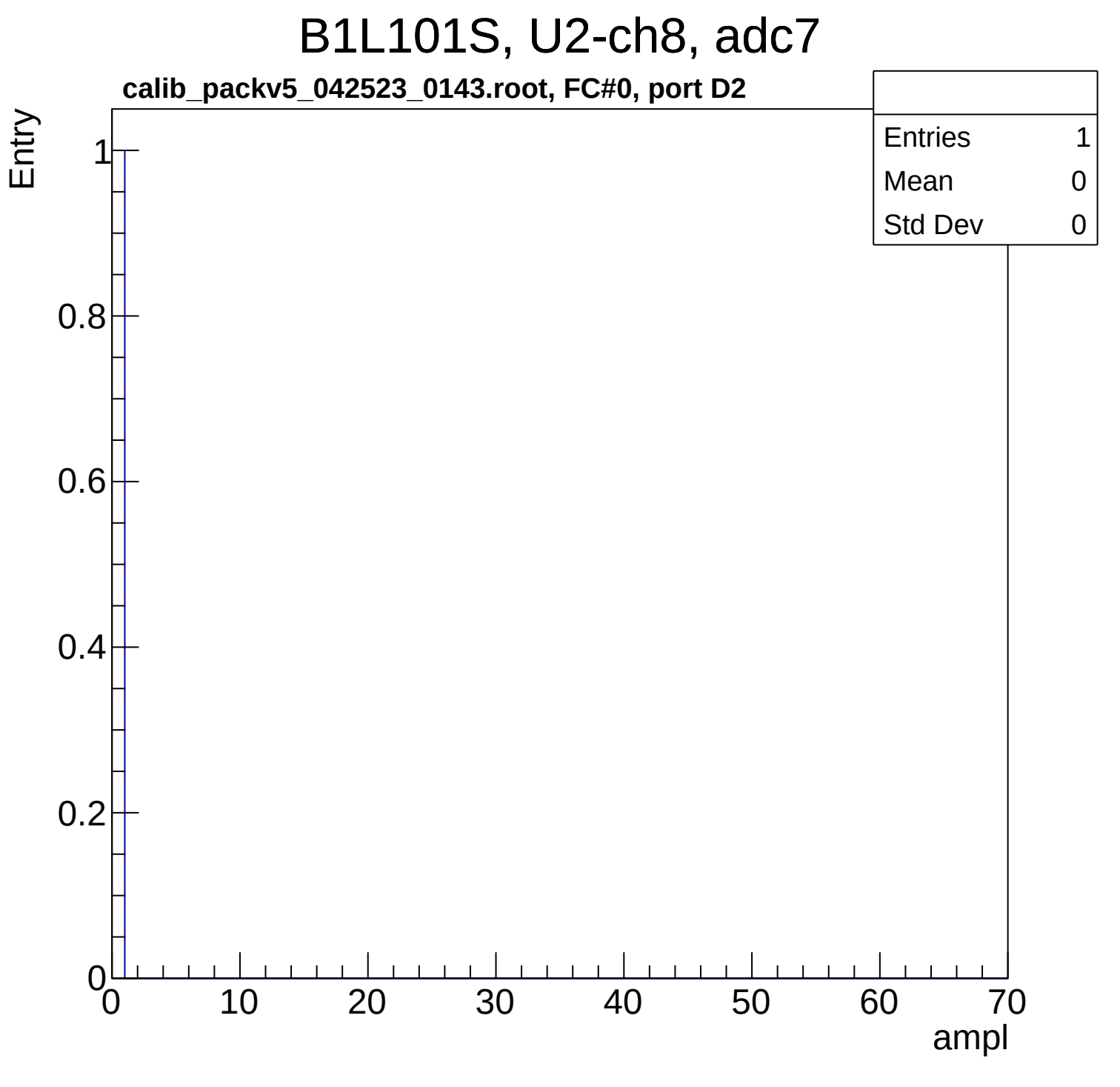

B1L101S, U2-ch8, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 43.53
Std Dev 3.488
Gaus mean : 43.8726
Gaus Width: 3.8143
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

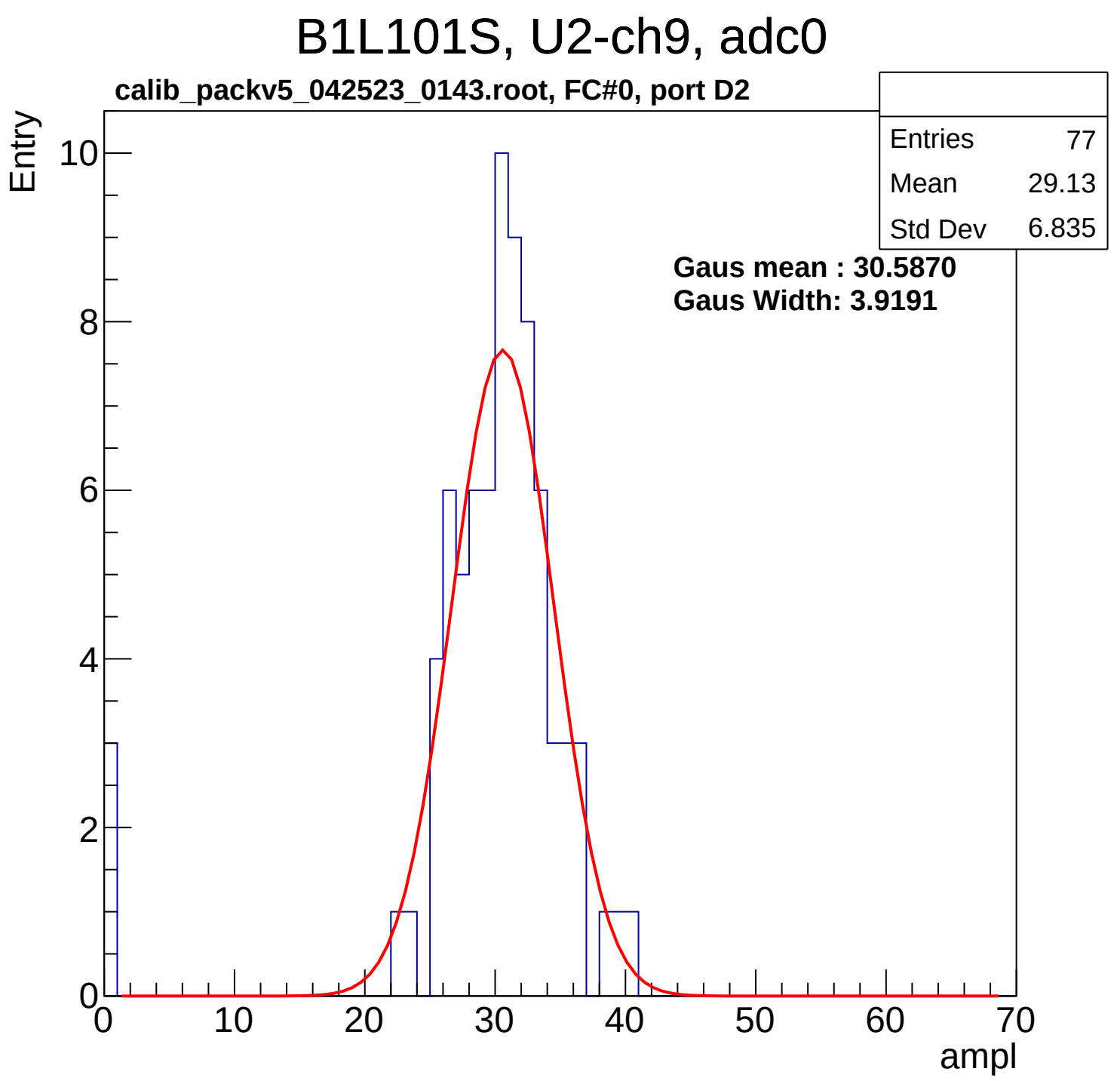

B1L101S, U2-ch8, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 50.21
Std Dev 3.331
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

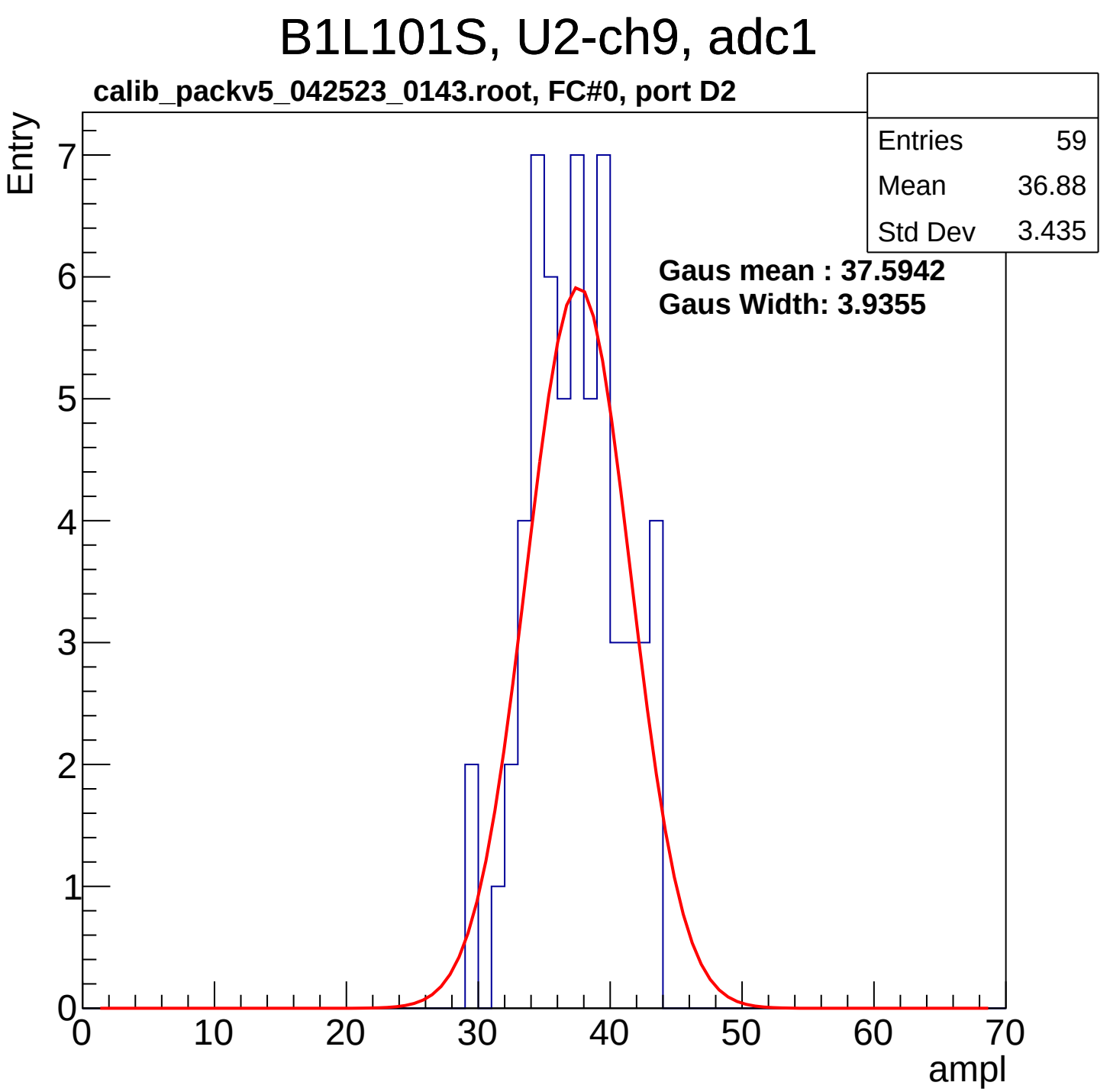

B1L101S, U2-ch8, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 40
Mean 55.3
Std Dev 2.777
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

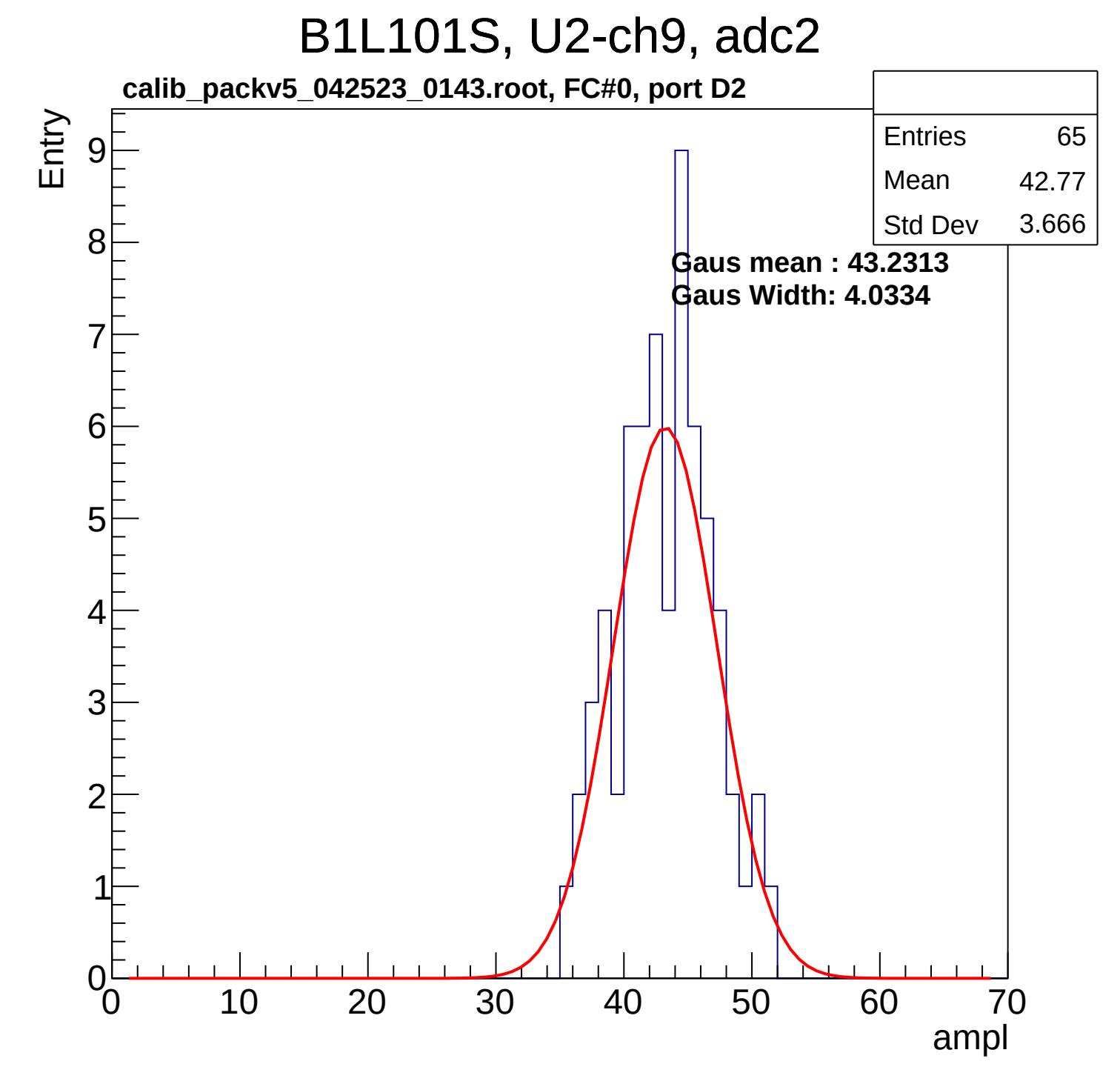

B1L101S, U2-ch8, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 58.14
Std Dev 8.215
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

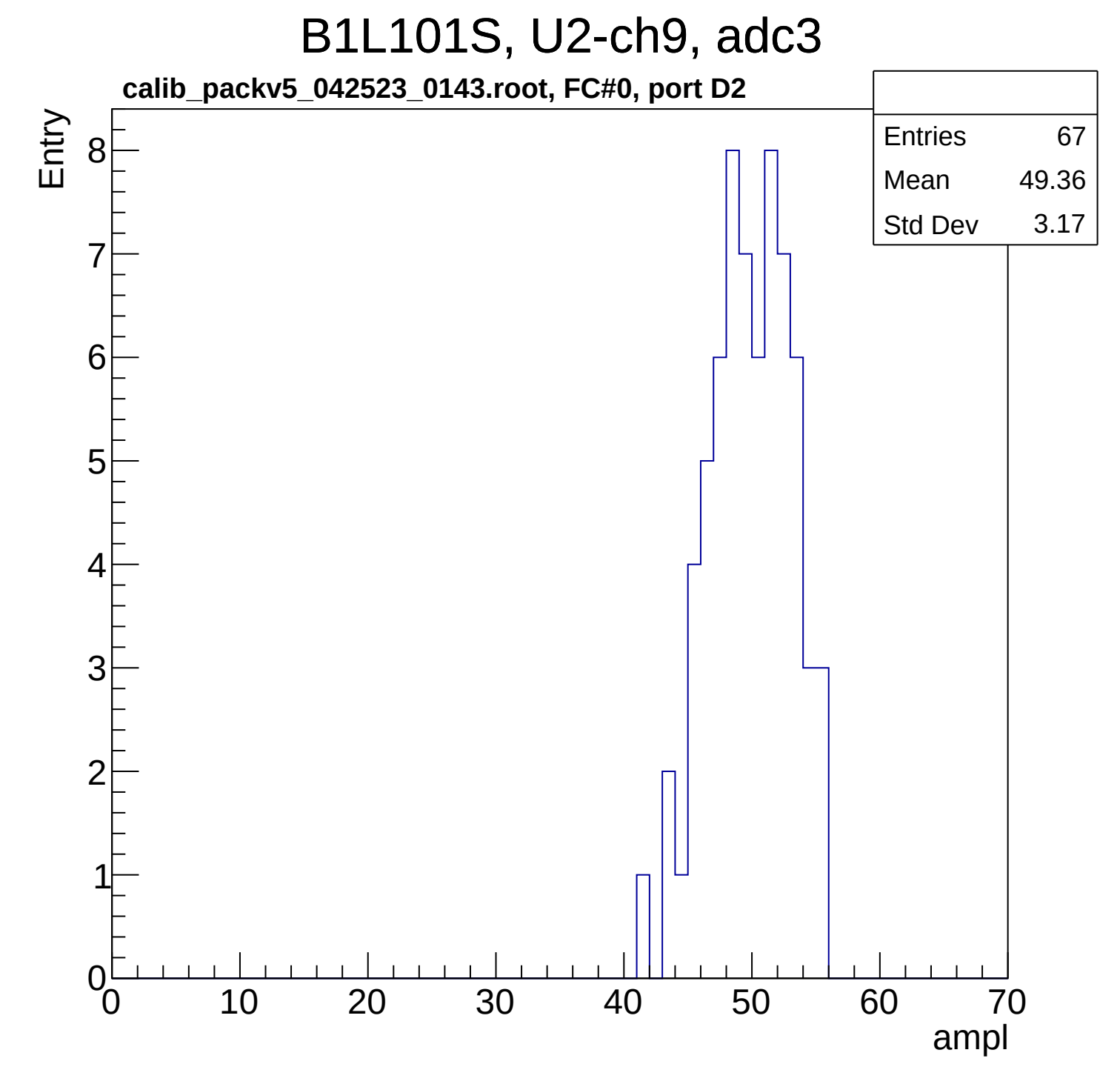

B1L101S, U2-ch8, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 62.5
Std Dev 0.866
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

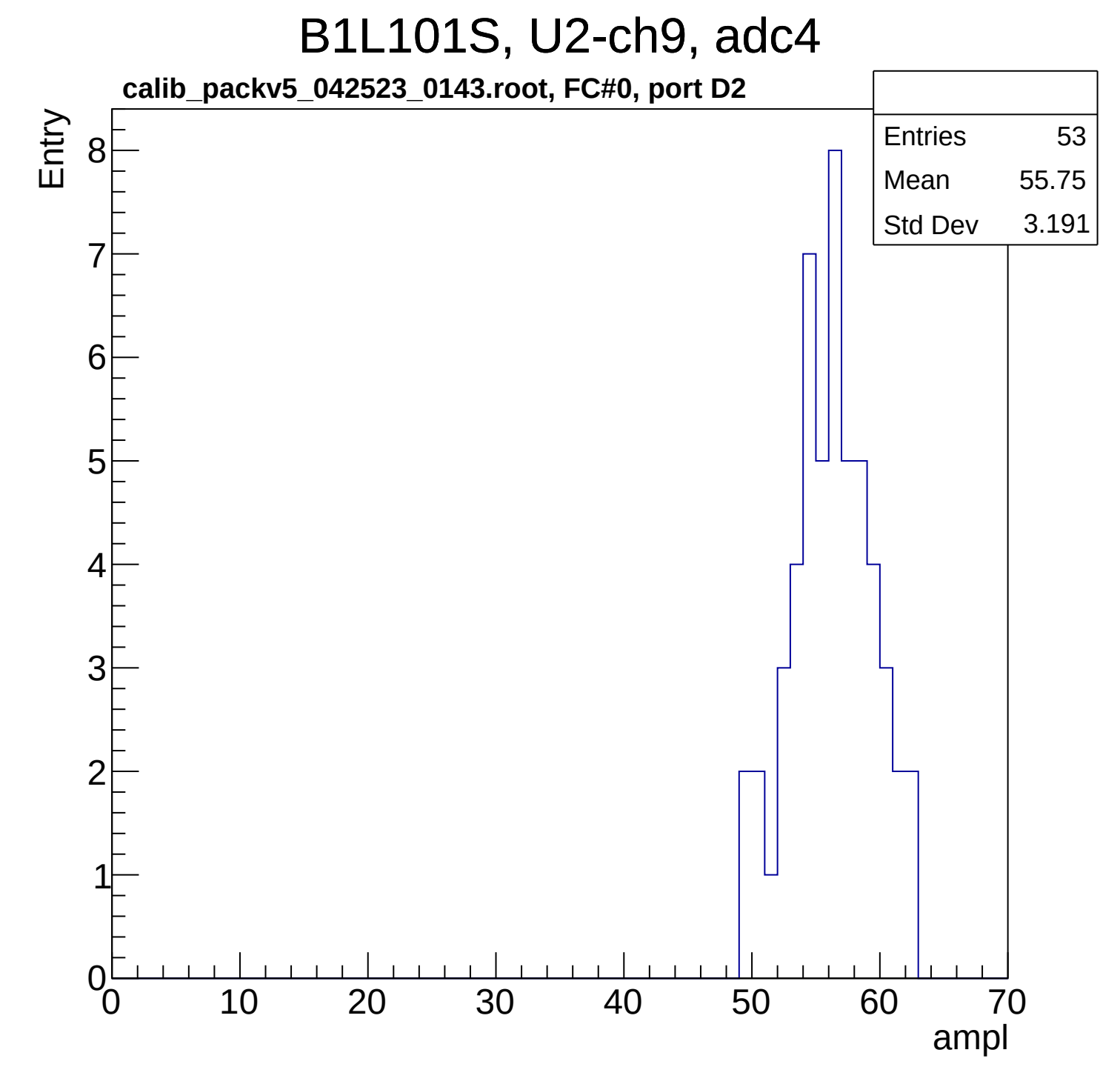

B1L101S, U2-ch8, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

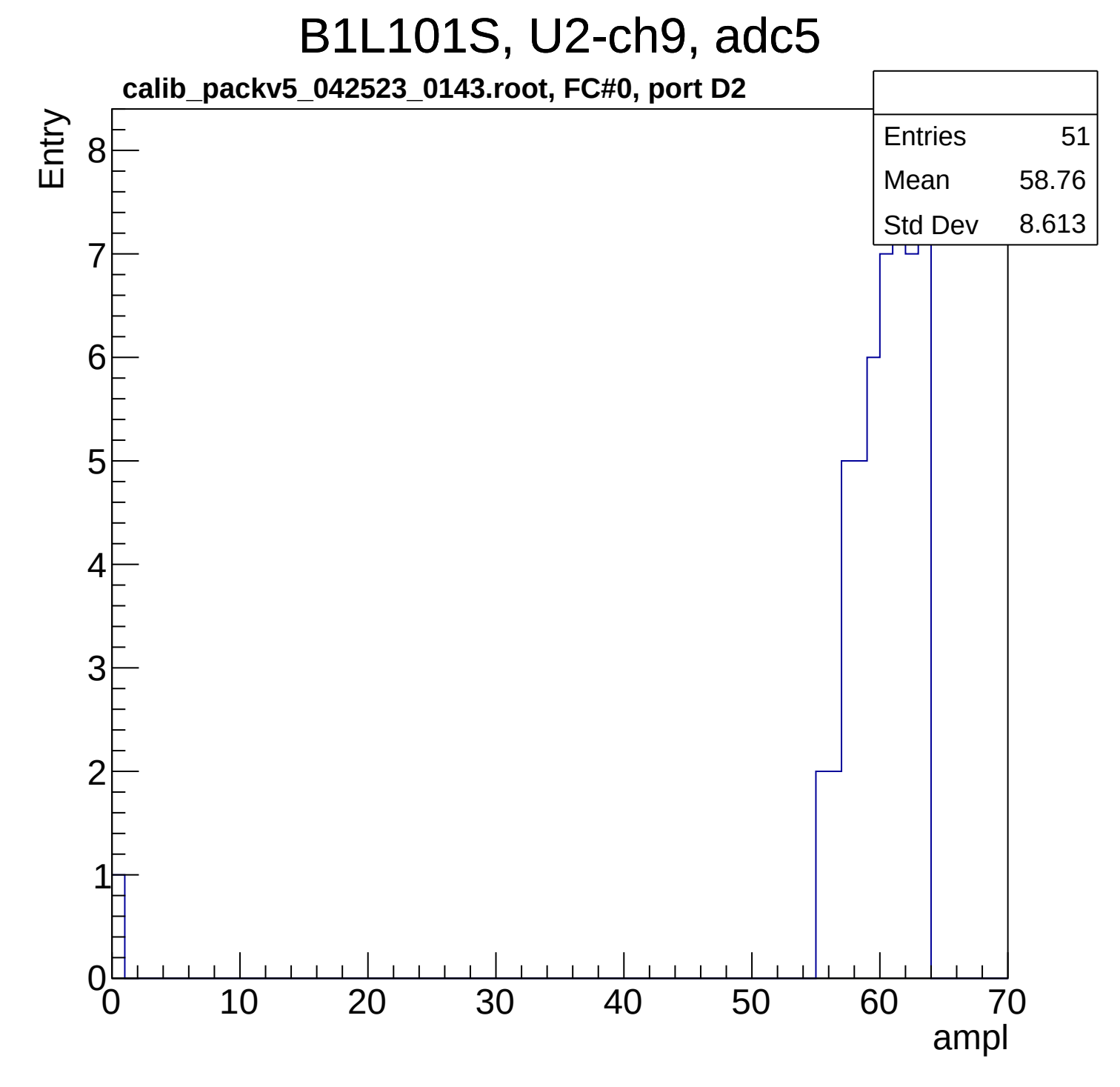

B1L101S, U2-ch9, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 29.13
Std Dev 6.835
Gaus mean : 30.5870
Gaus Width: 3.9191
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

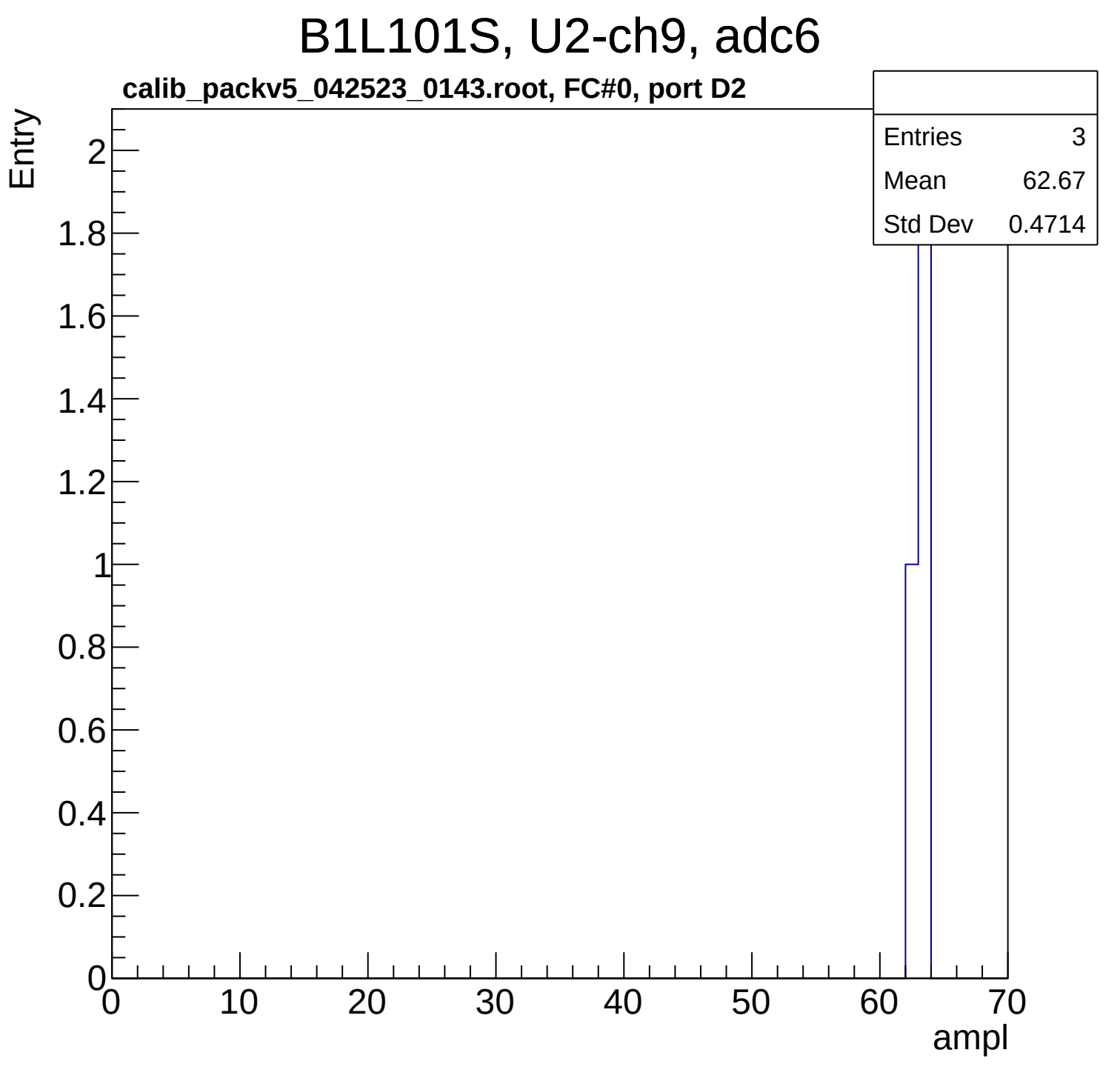

B1L101S, U2-ch9, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 36.88
Std Dev 3.435
Gaus mean : 37.5942
Gaus Width: 3.9355
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

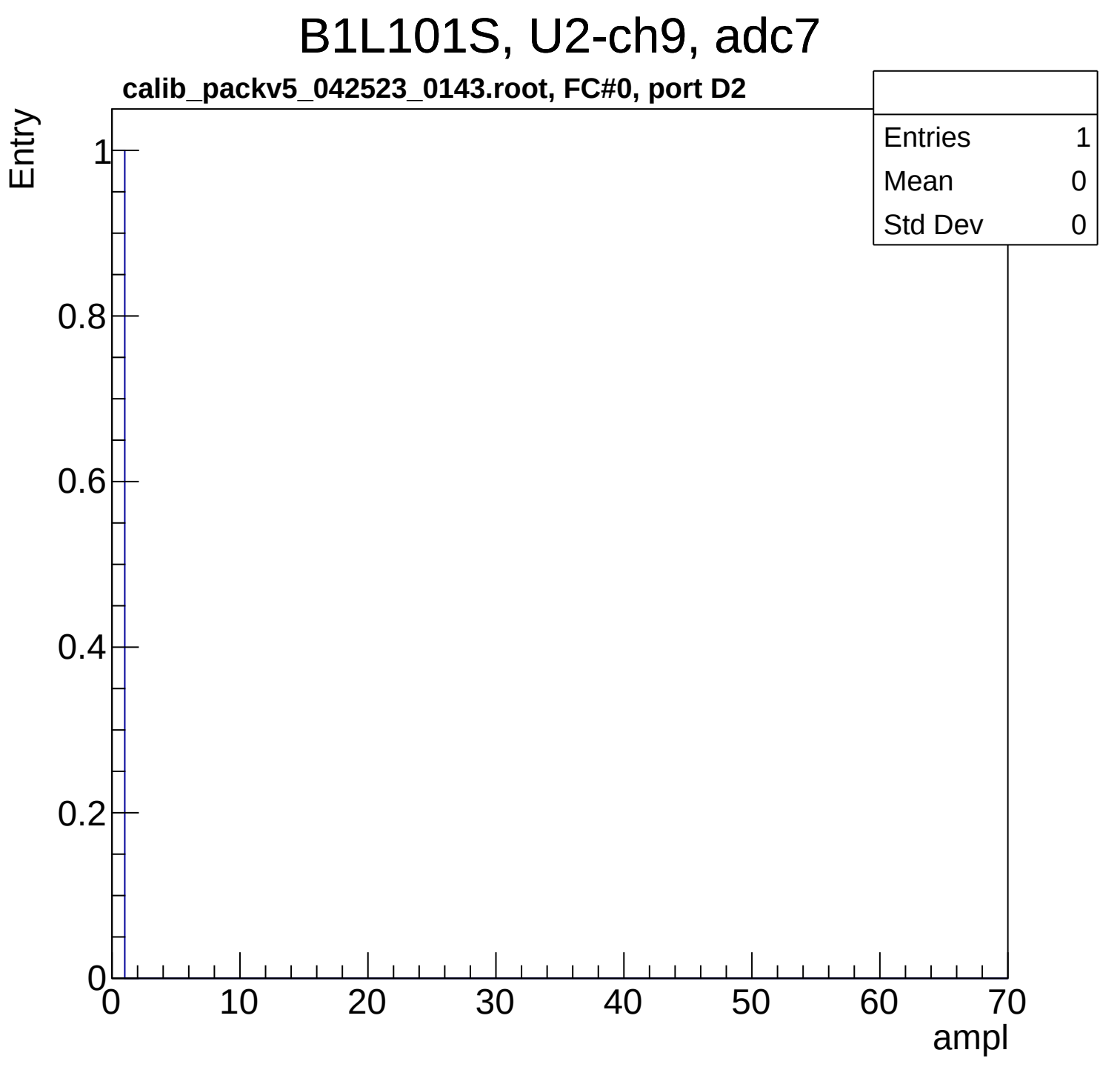

B1L101S, U2-ch9, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 42.77
Std Dev 3.666
Gaus mean : 43.2313
Gaus Width: 4.0334
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

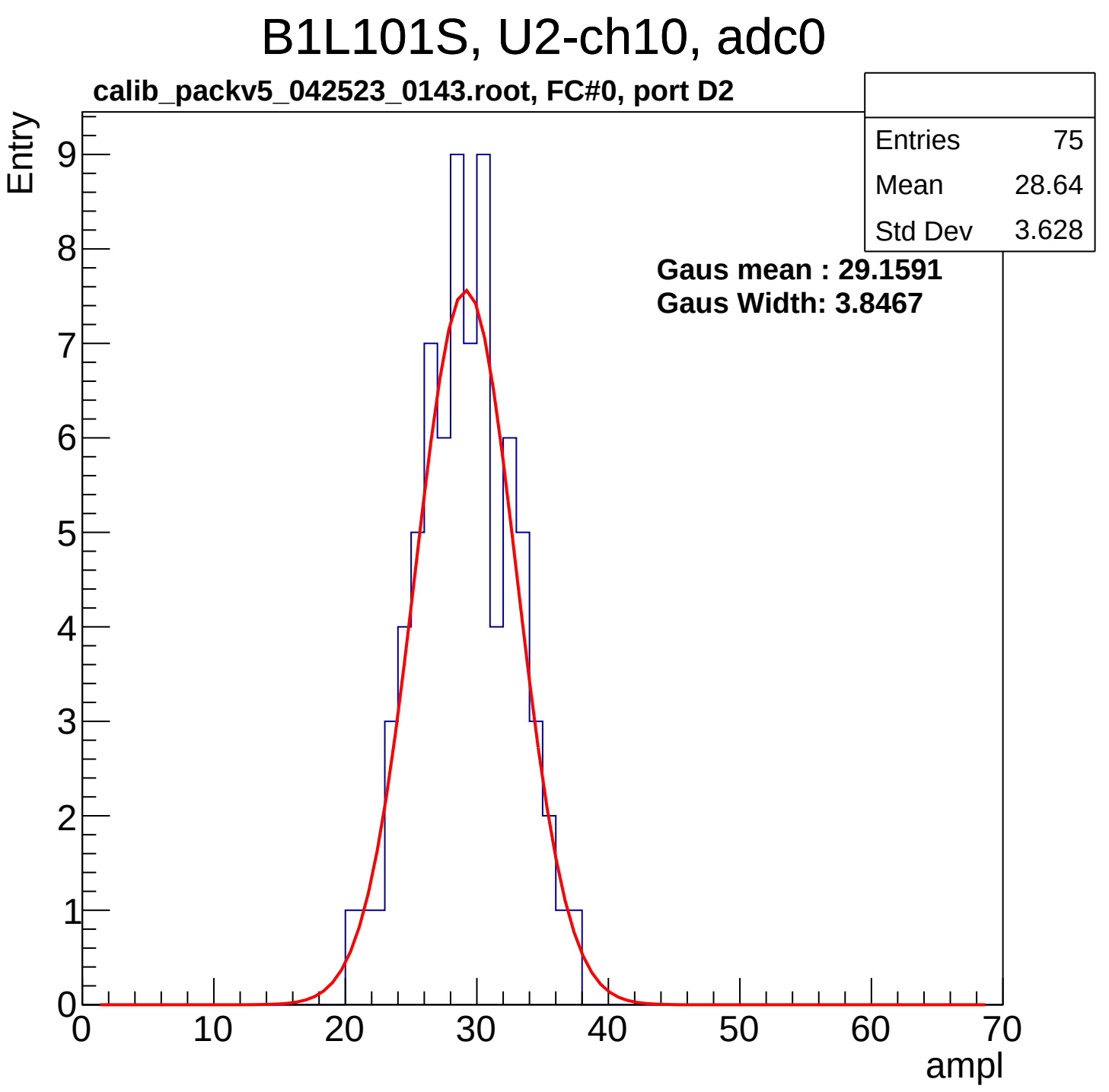

B1L101S, U2-ch9, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 49.36
Std Dev 3.17
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

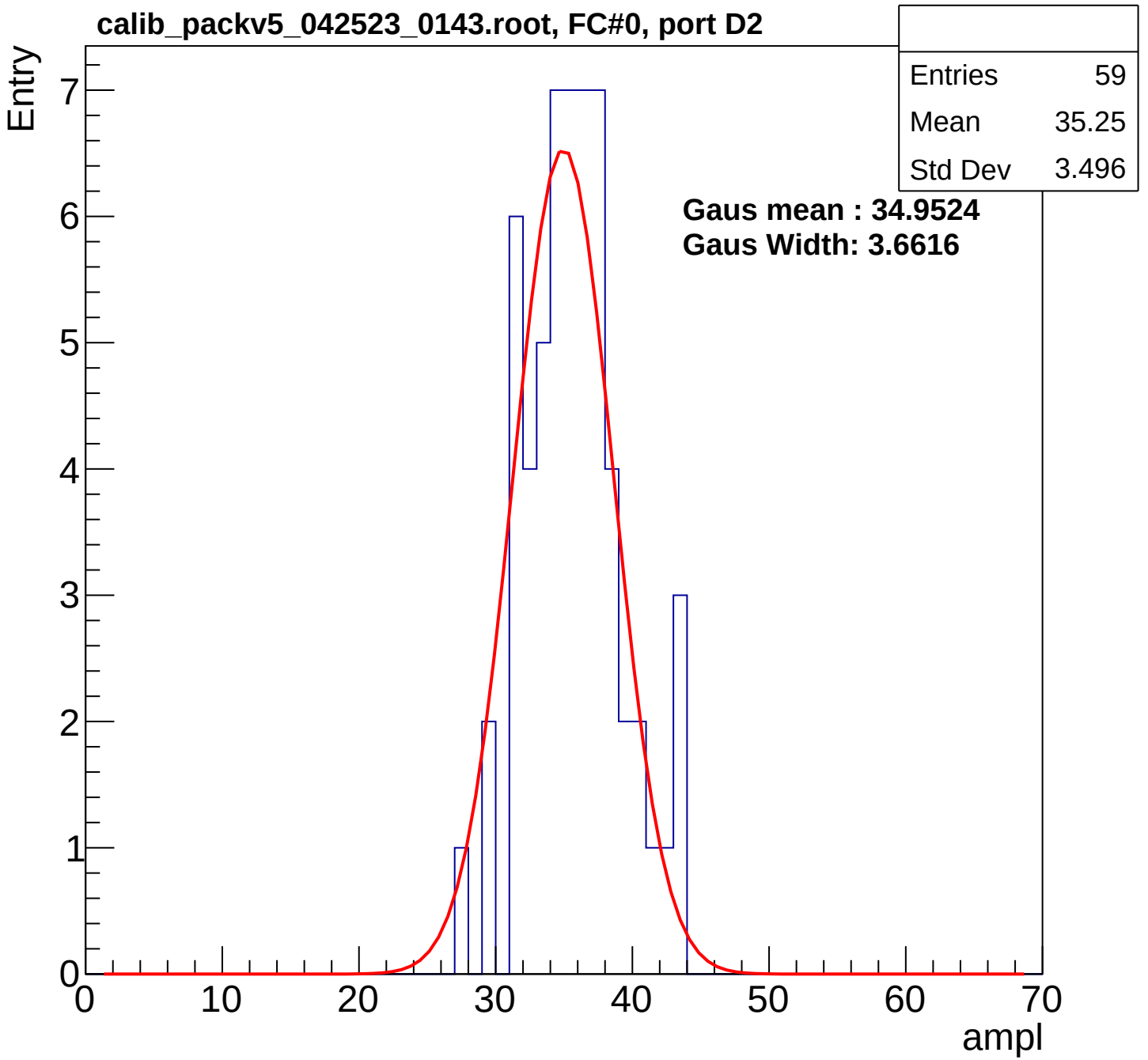

B1L101S, U2-ch9, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 55.75
Std Dev 3.191
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

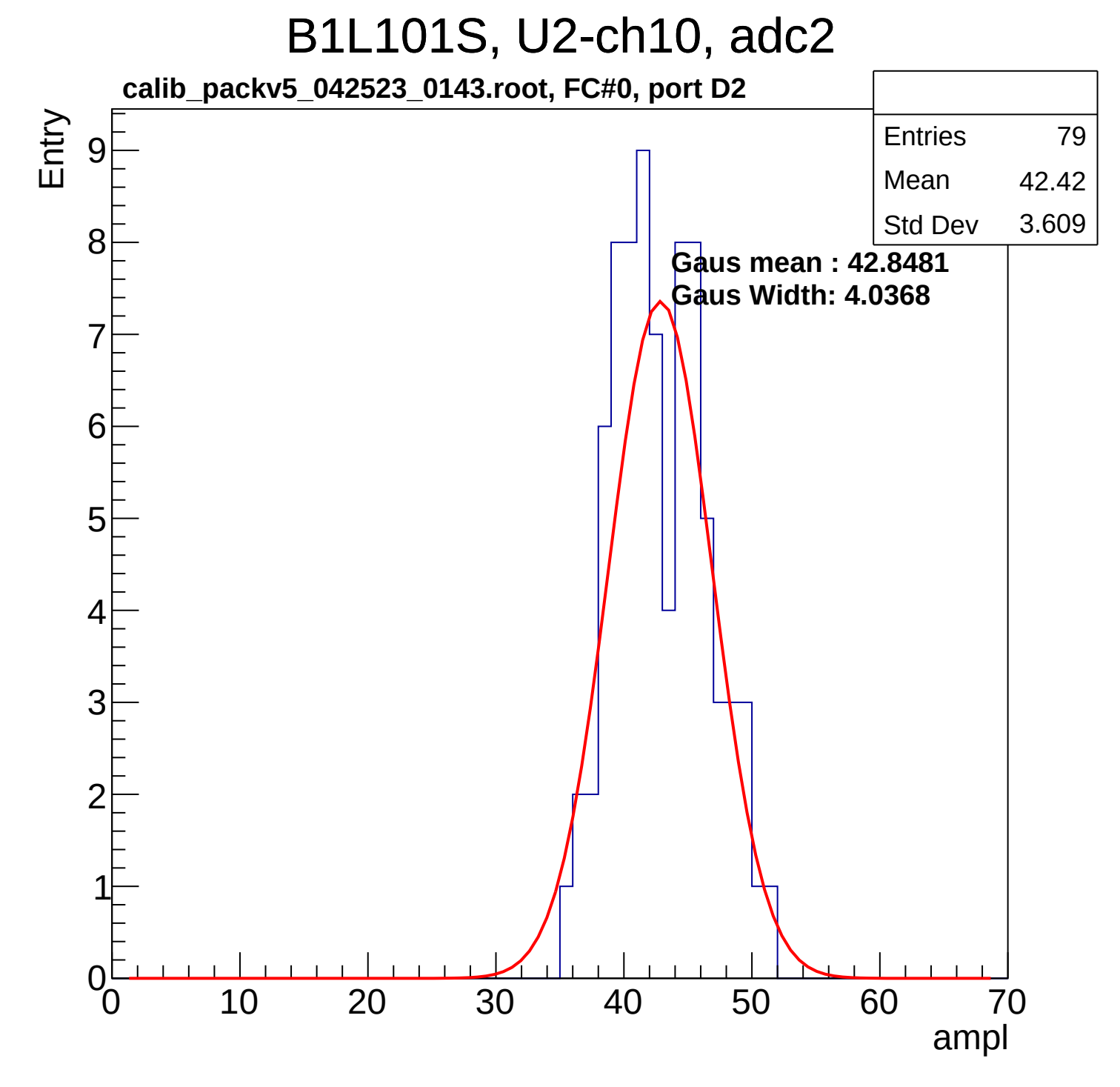

B1L101S, U2-ch9, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 58.76
Std Dev 8.613
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

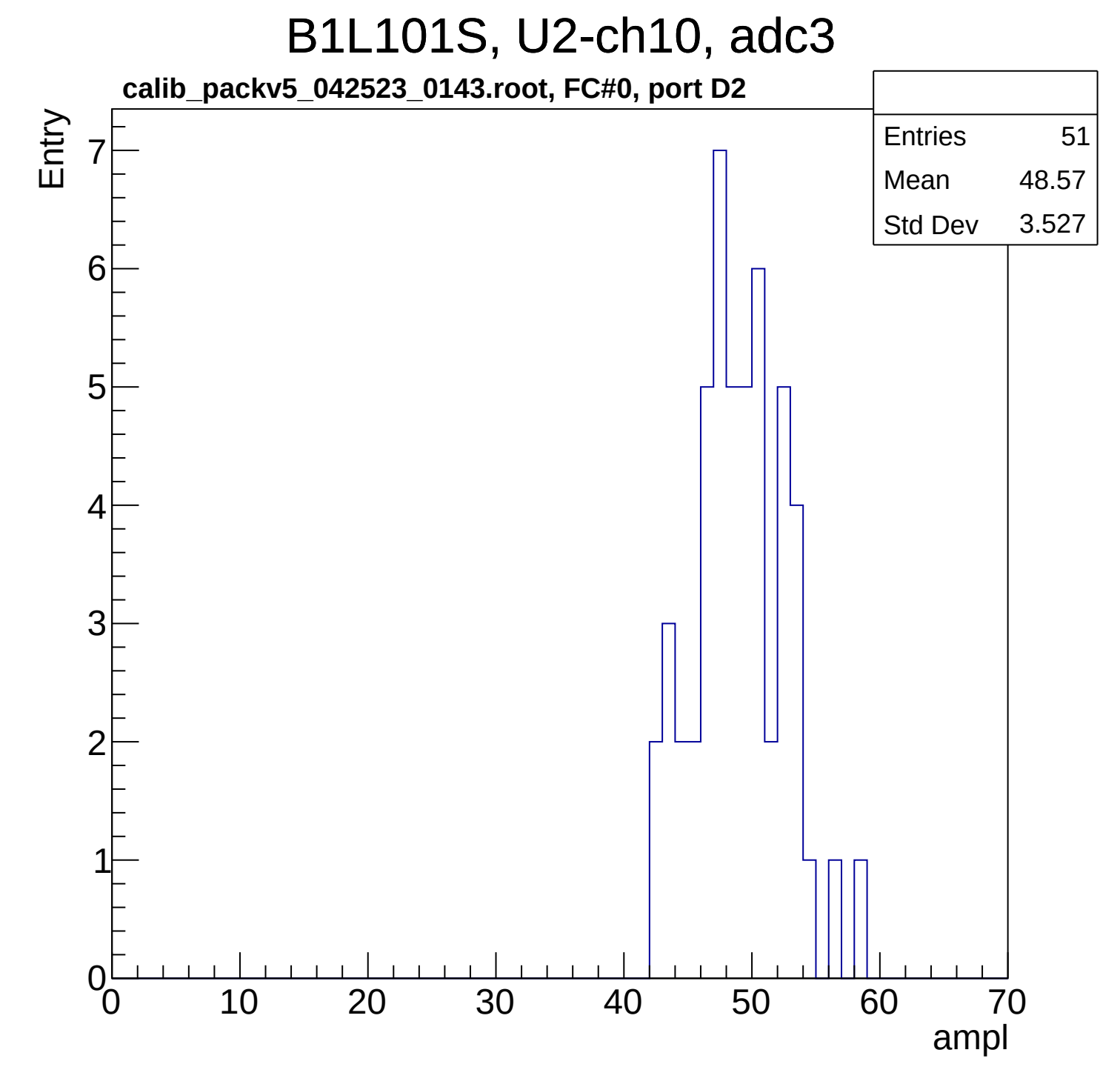

B1L101S, U2-ch9, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

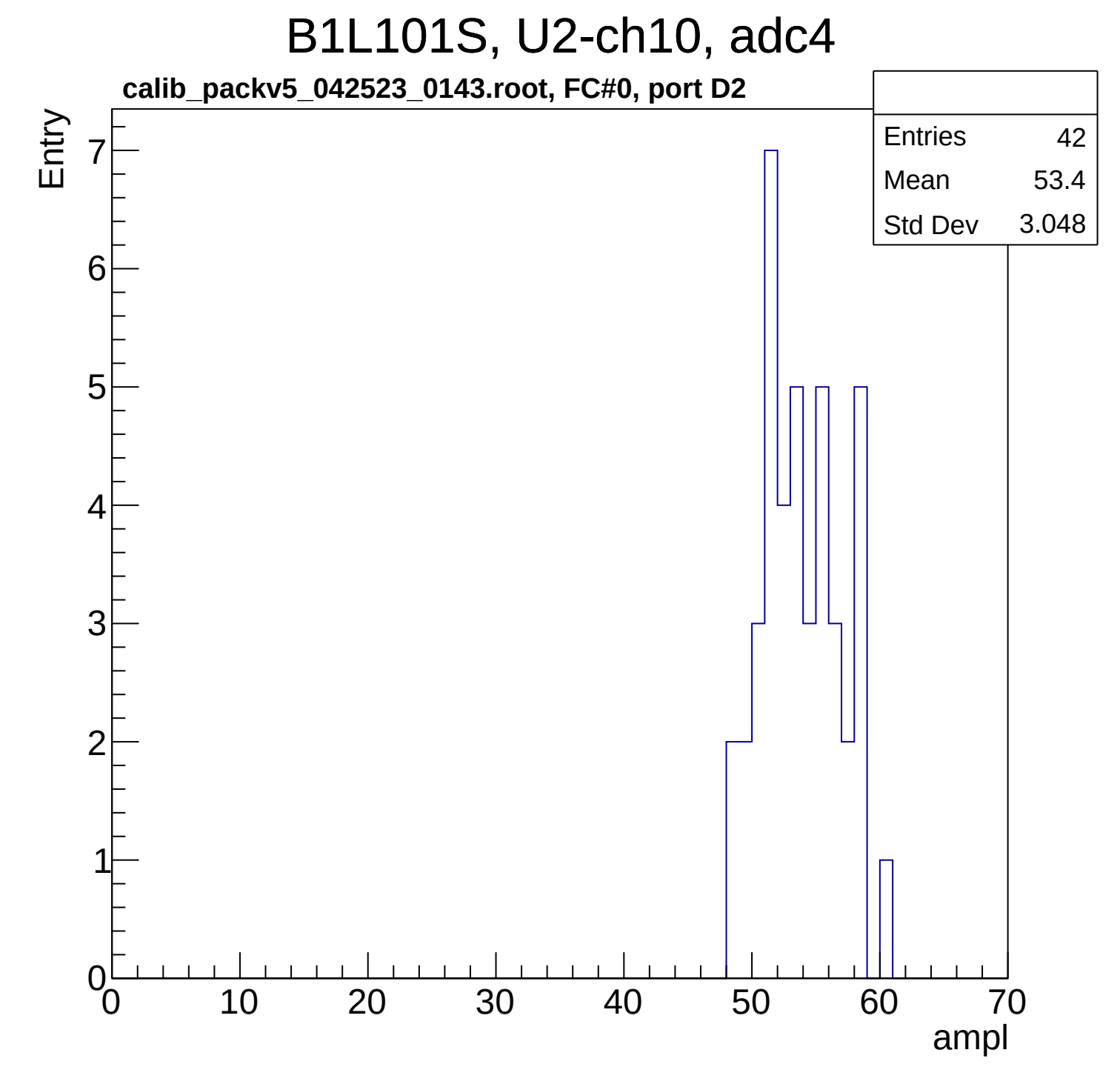

B1L101S, U2-ch9, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

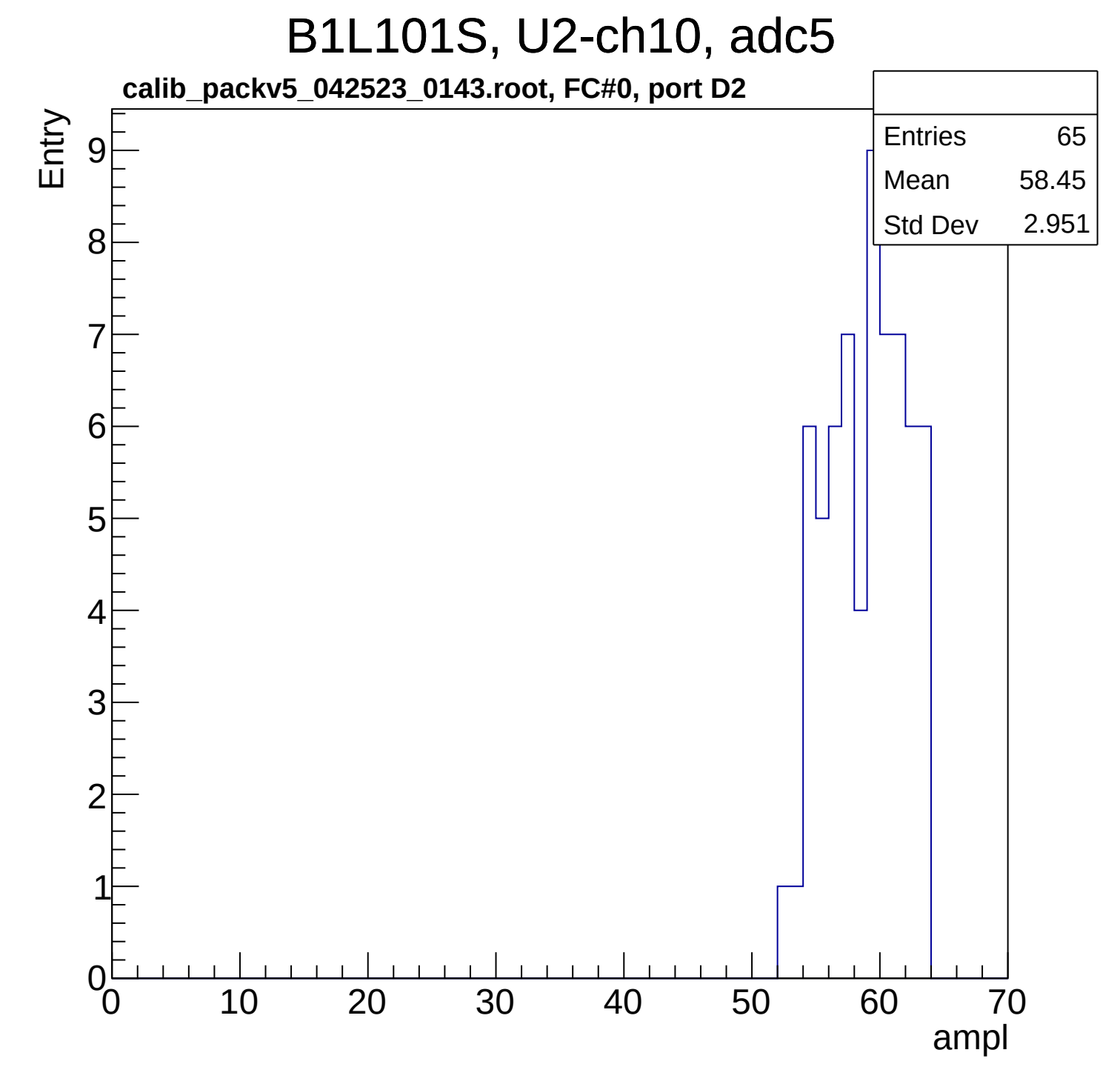

B1L101S, U2-ch10, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 28.64
Std Dev 3.628
Gaus mean : 29.1591
Gaus Width: 3.8467
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

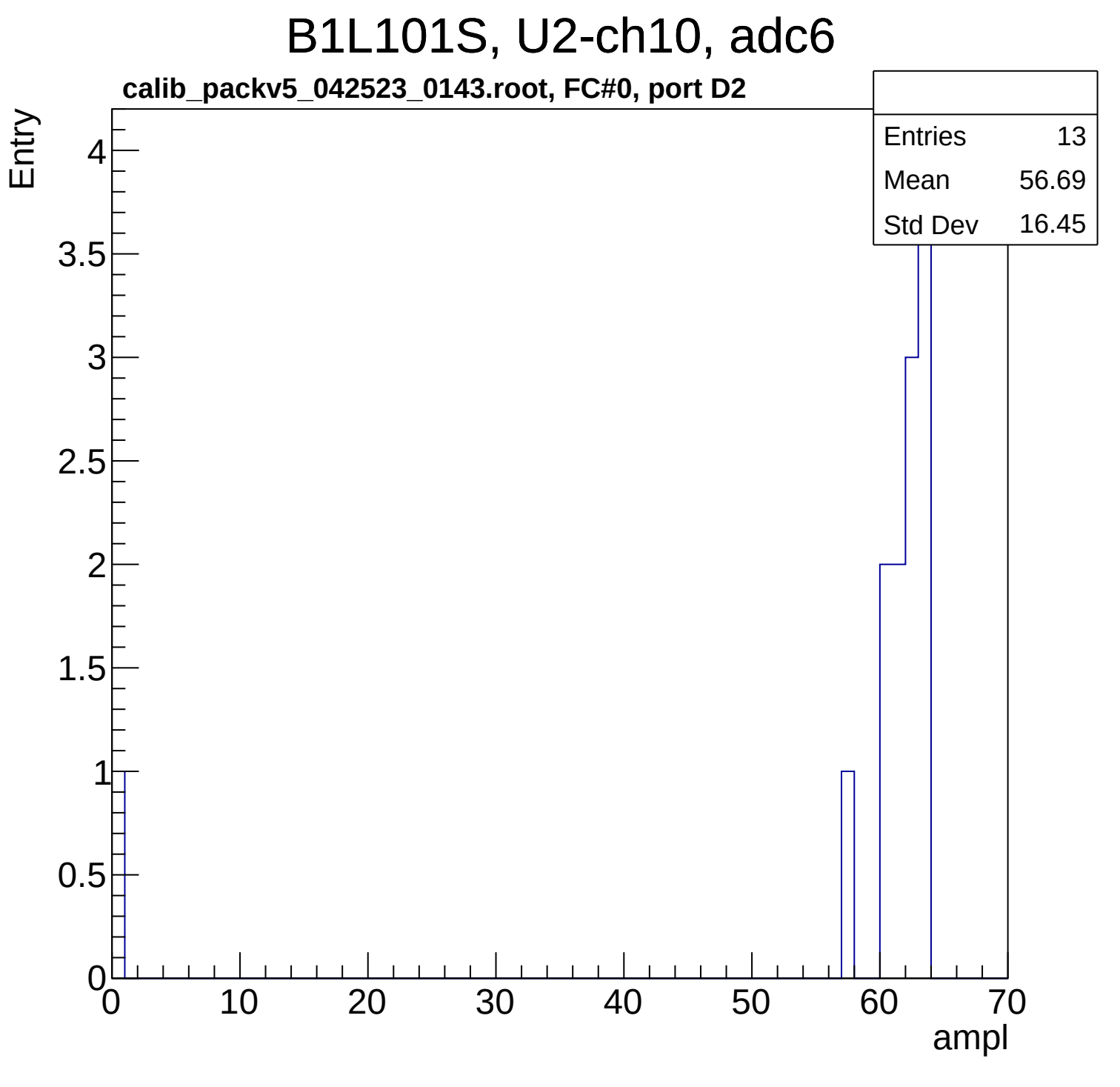

B1L101S, U2-ch10, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 35.25
Std Dev 3.496
Gaus mean : 34.9524
Gaus Width: 3.6616
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

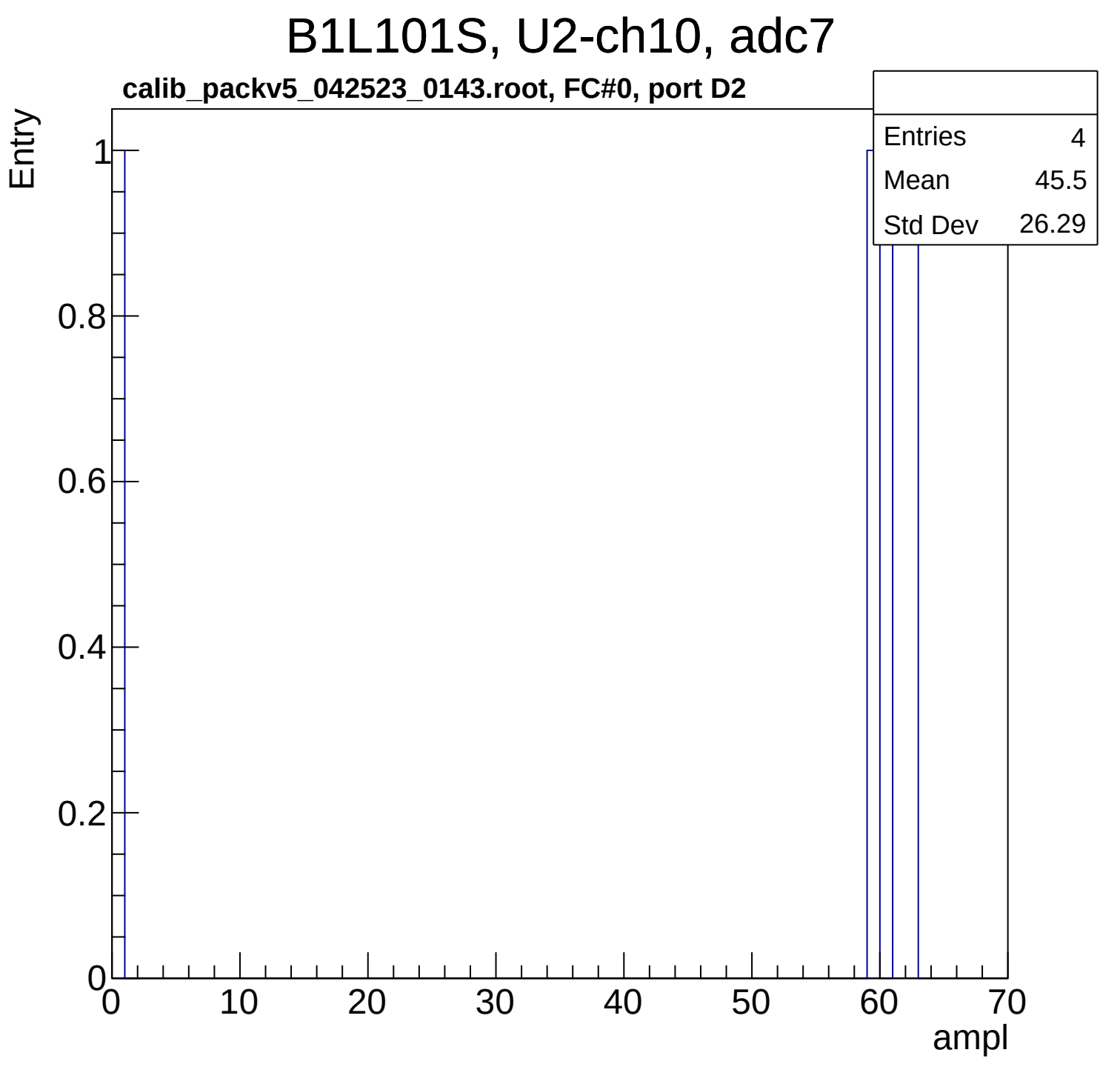

B1L101S, U2-ch10, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 42.42
Std Dev 3.609
Gaus mean : 42.8481
Gaus Width: 4.0368
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

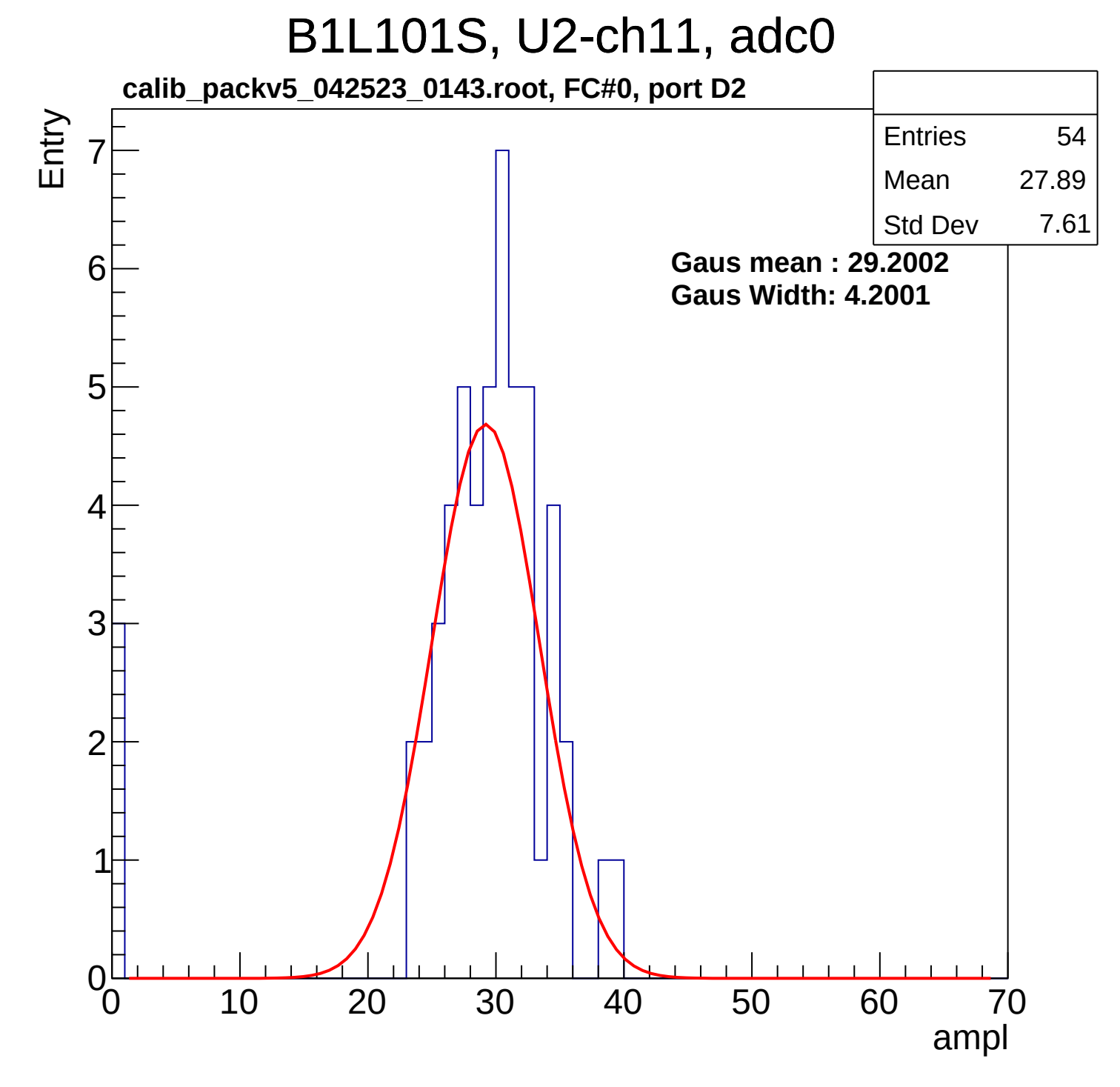

B1L101S, U2-ch10, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 48.57
Std Dev 3.527
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

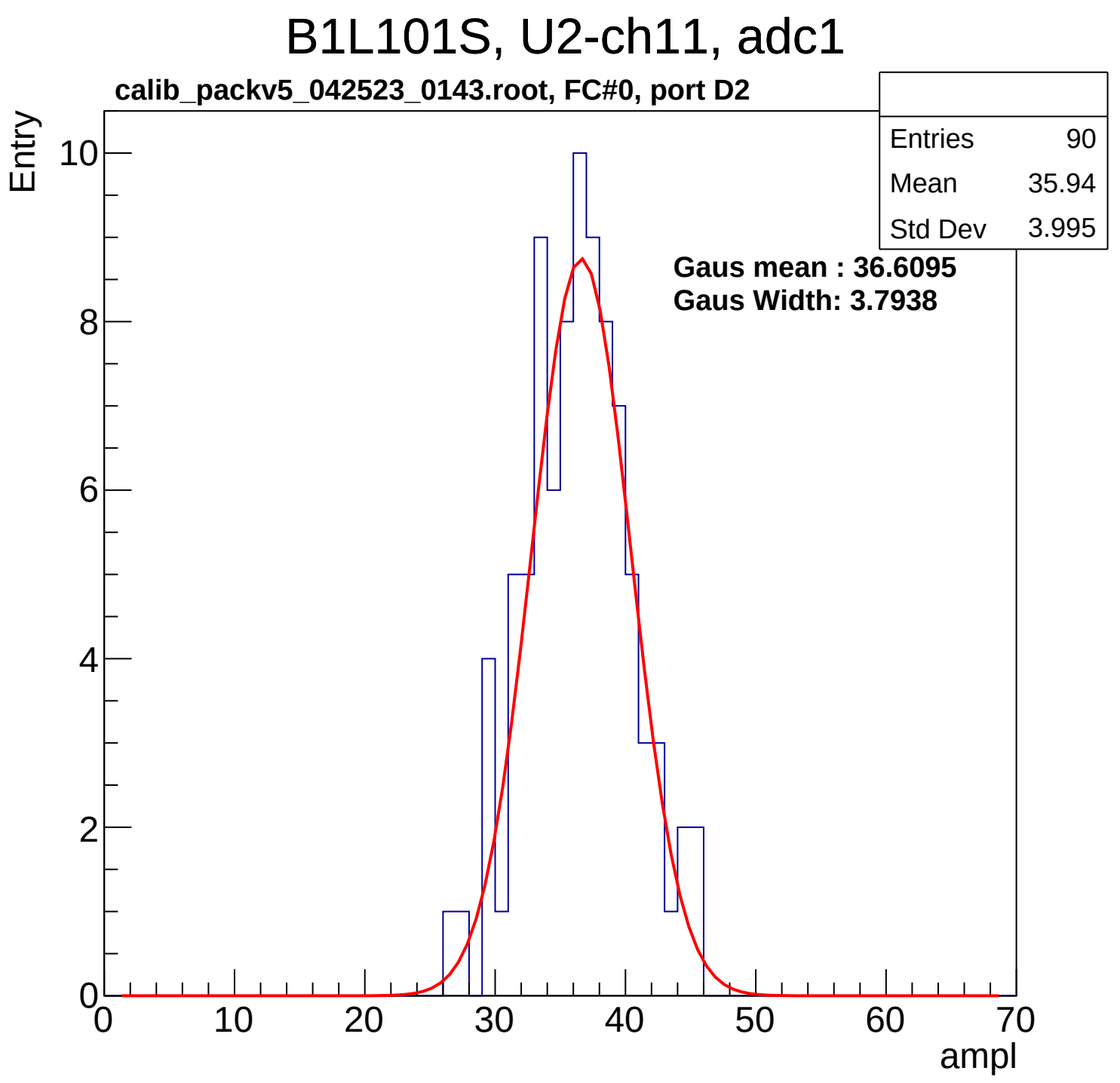

B1L101S, U2-ch10, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 53.4
Std Dev 3.048
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

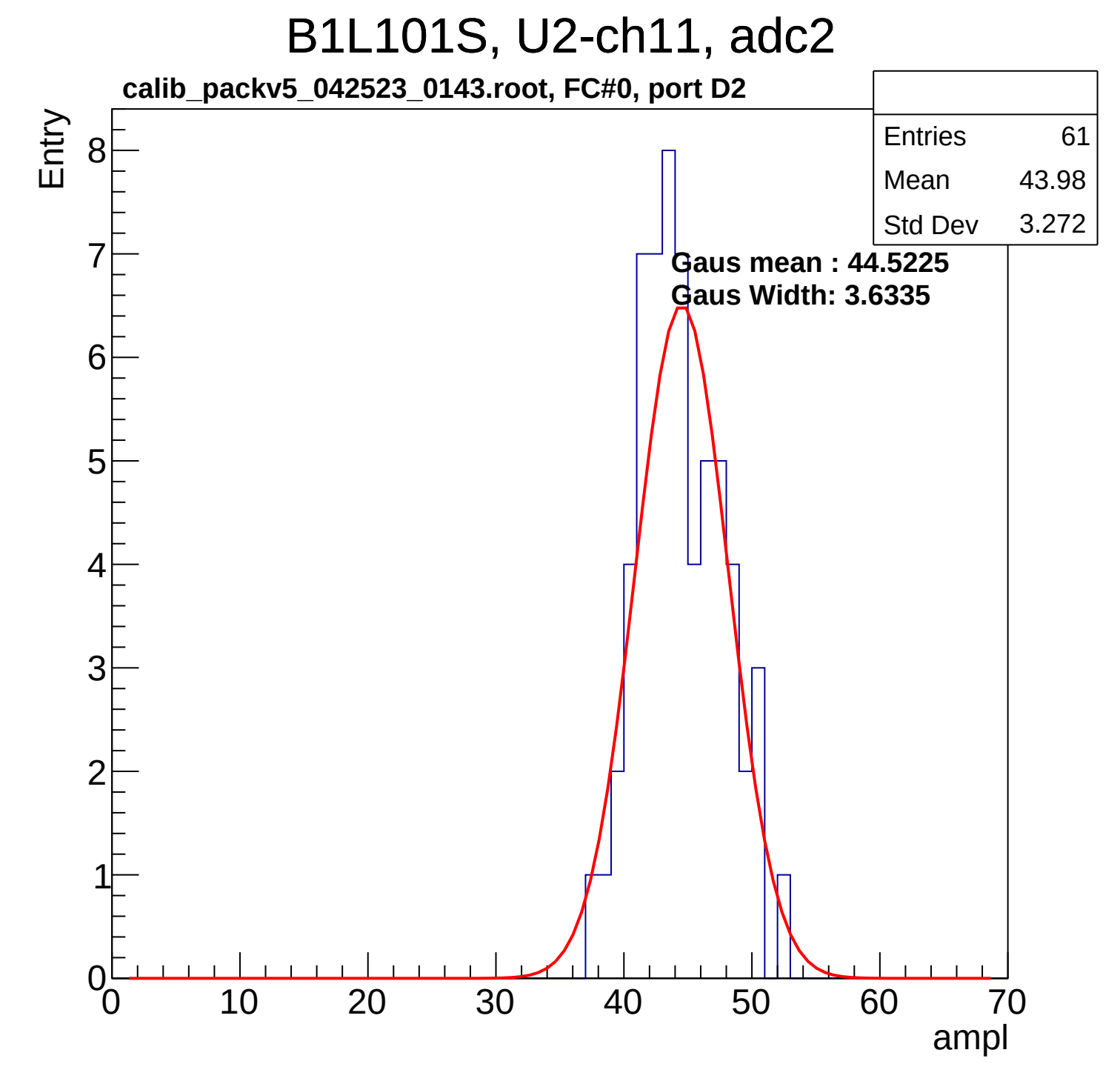

B1L101S, U2-ch10, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 58.45
Std Dev 2.951
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

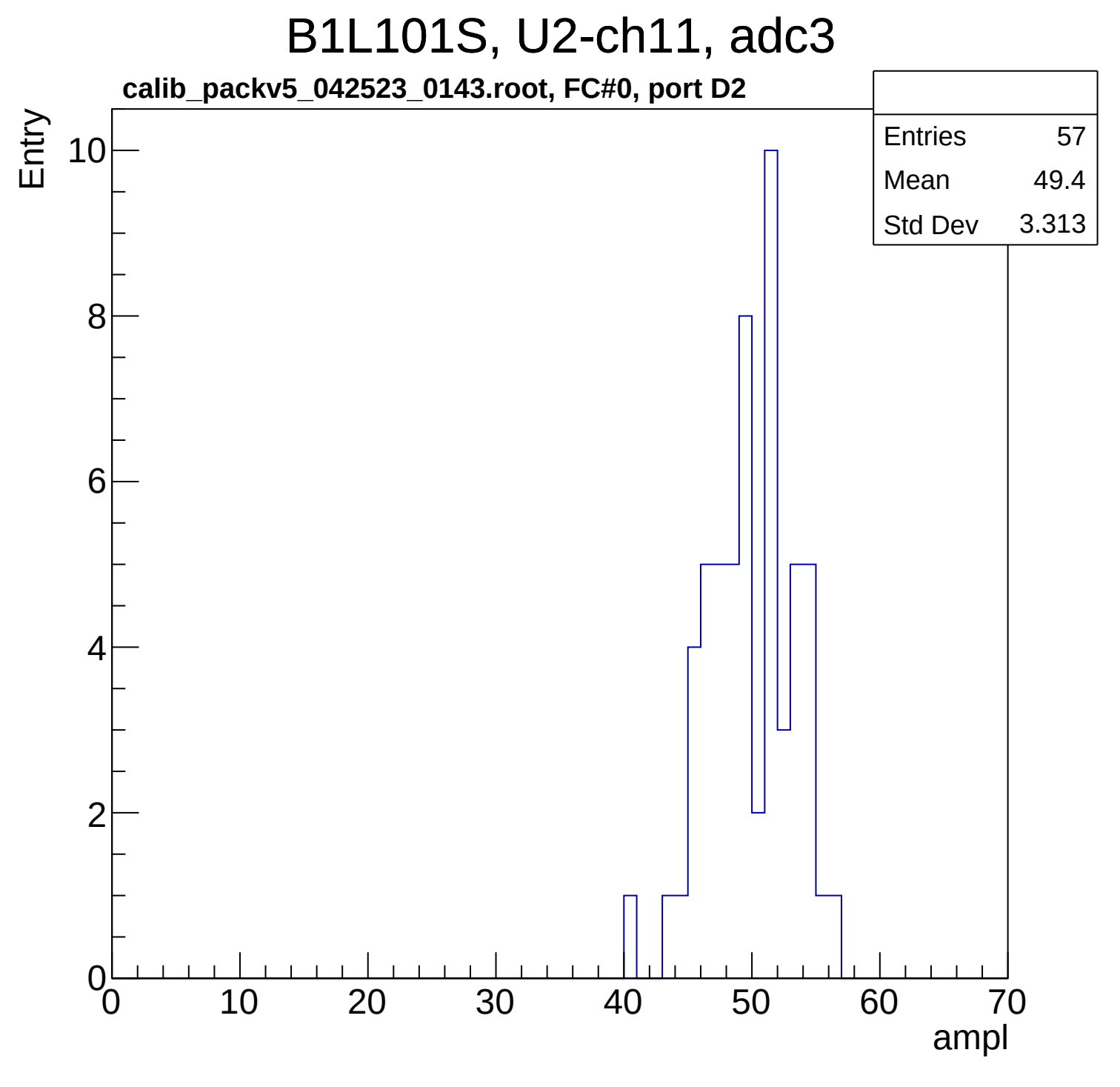

B1L101S, U2-ch10, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 13
Mean 56.69
Std Dev 16.45
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

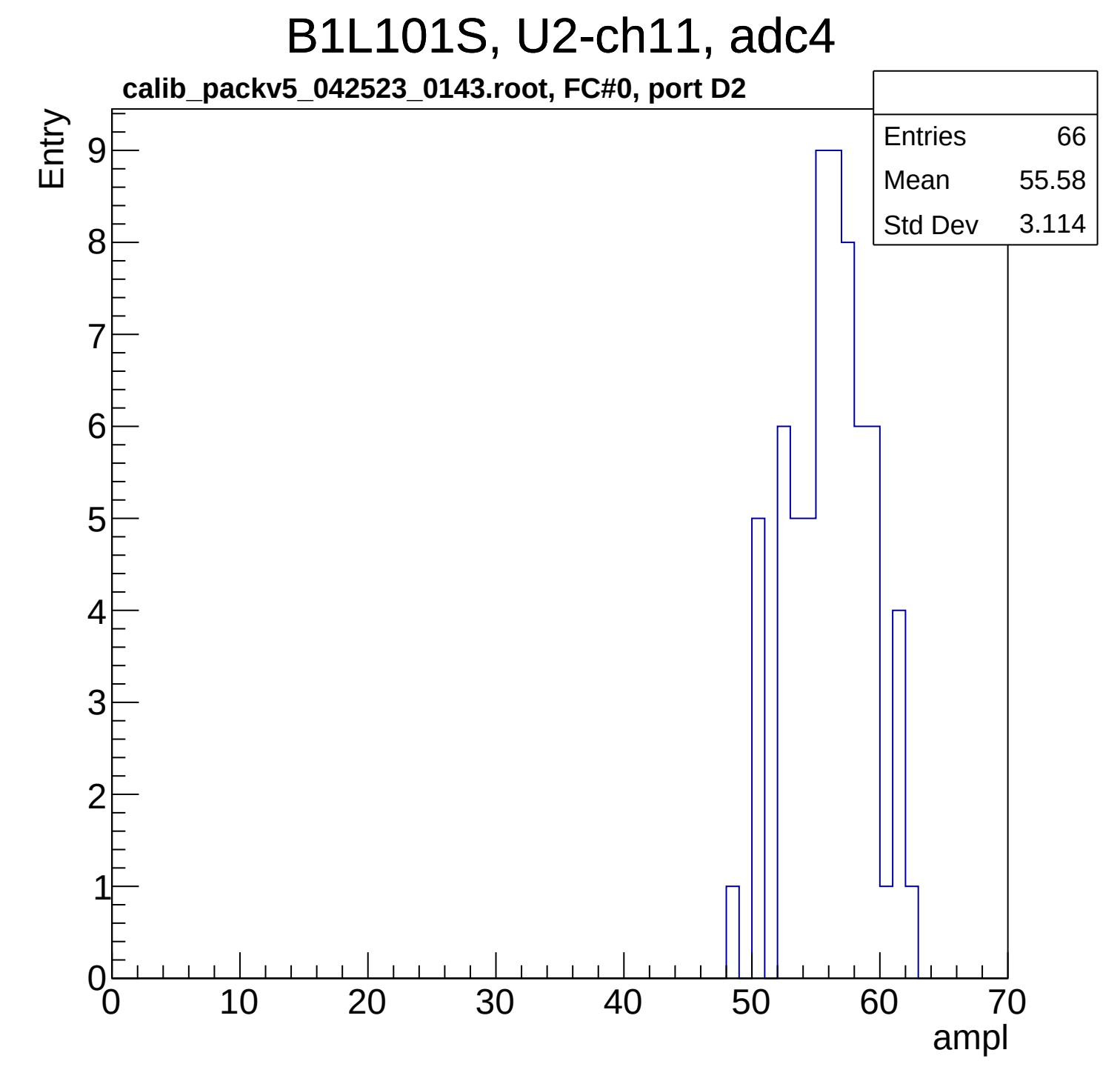

B1L101S, U2-ch10, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 45.5
Std Dev 26.29
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

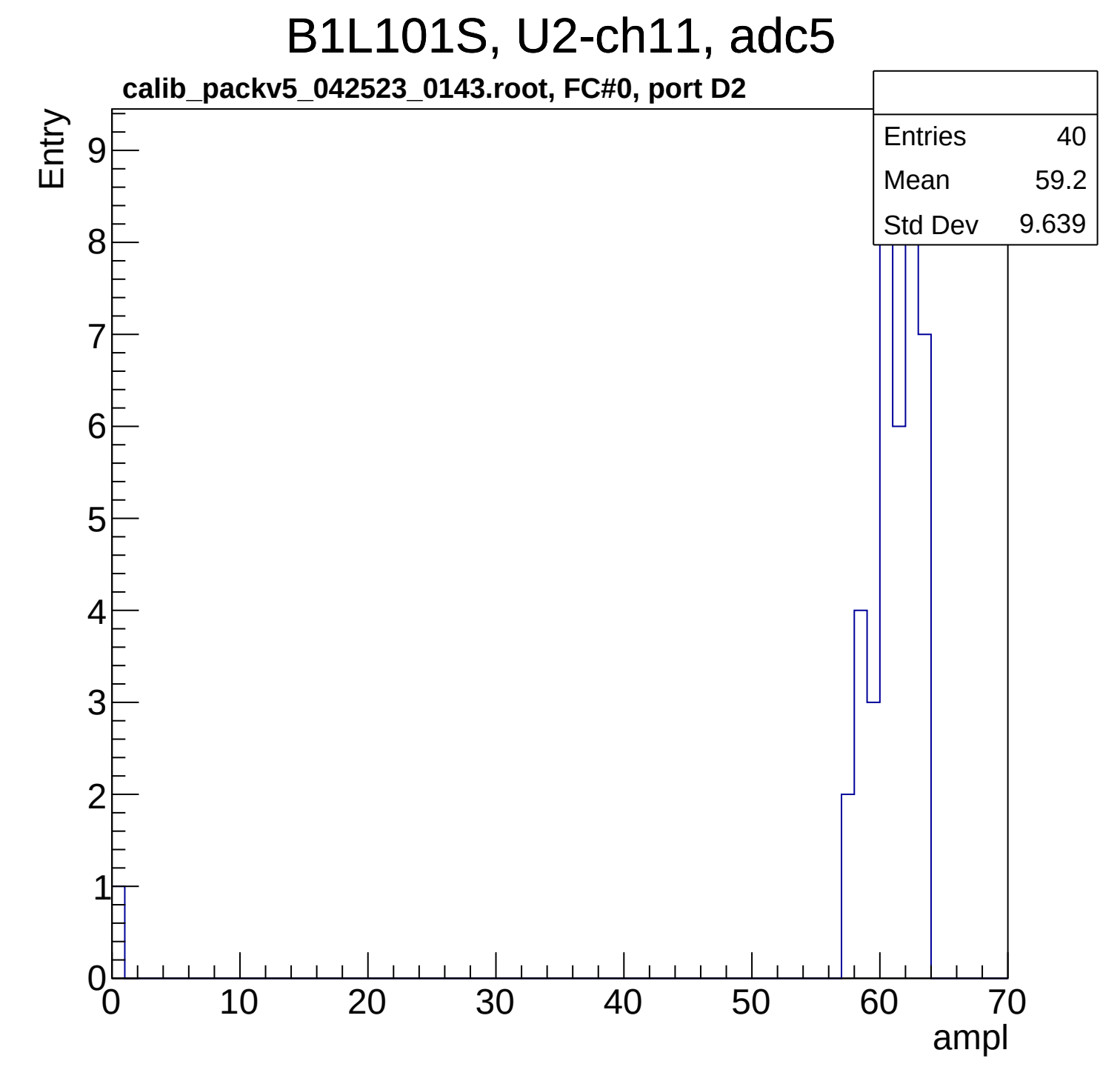

B1L101S, U2-ch11, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 27.89
Std Dev 7.61
Gaus mean : 29.2002
Gaus Width: 4.2001
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

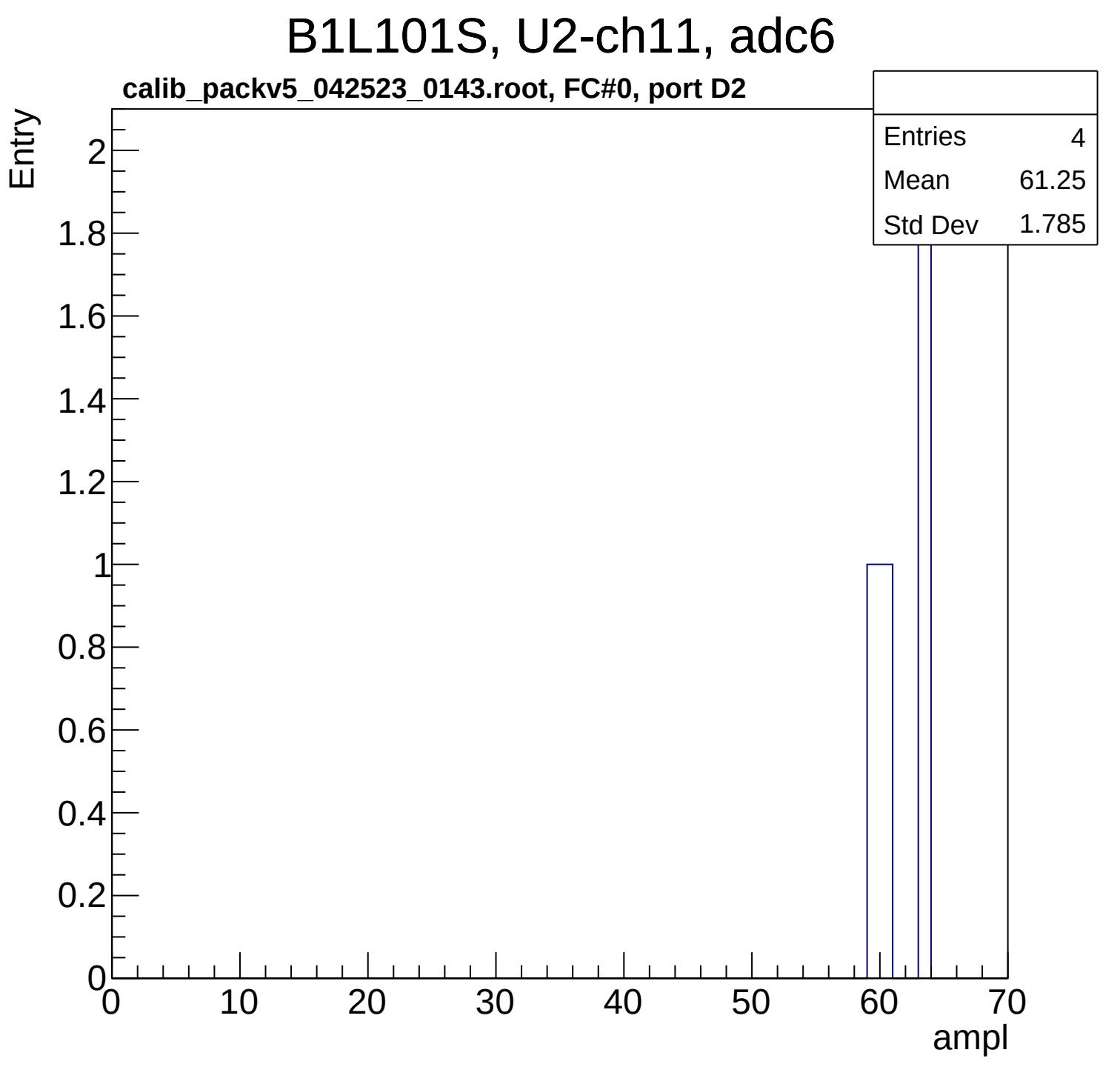

B1L101S, U2-ch11, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 90
Mean 35.94
Std Dev 3.995
Gaus mean : 36.6095
Gaus Width: 3.7938
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

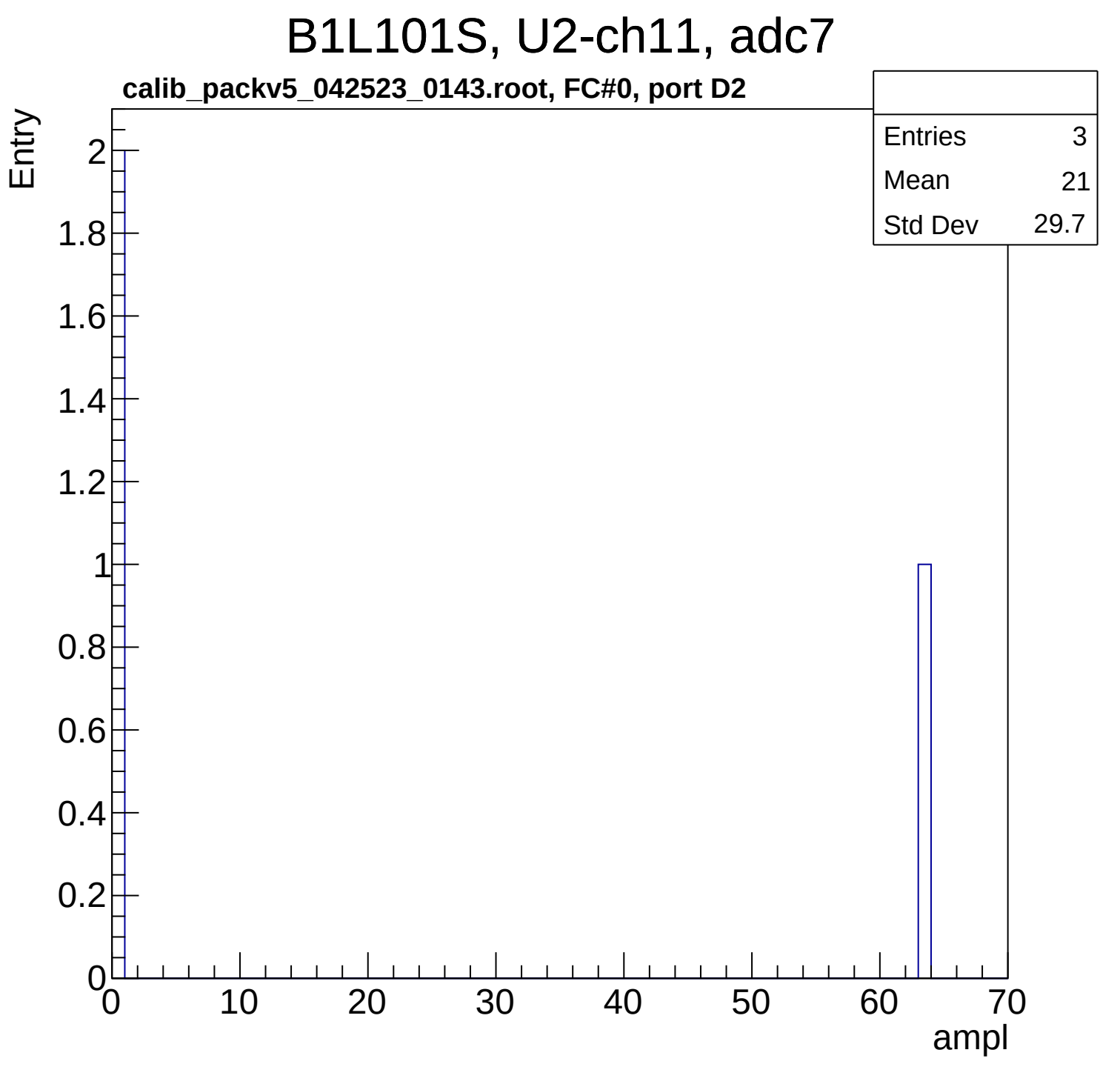

B1L101S, U2-ch11, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 43.98
Std Dev 3.272
Gaus mean : 44.5225
Gaus Width: 3.6335
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

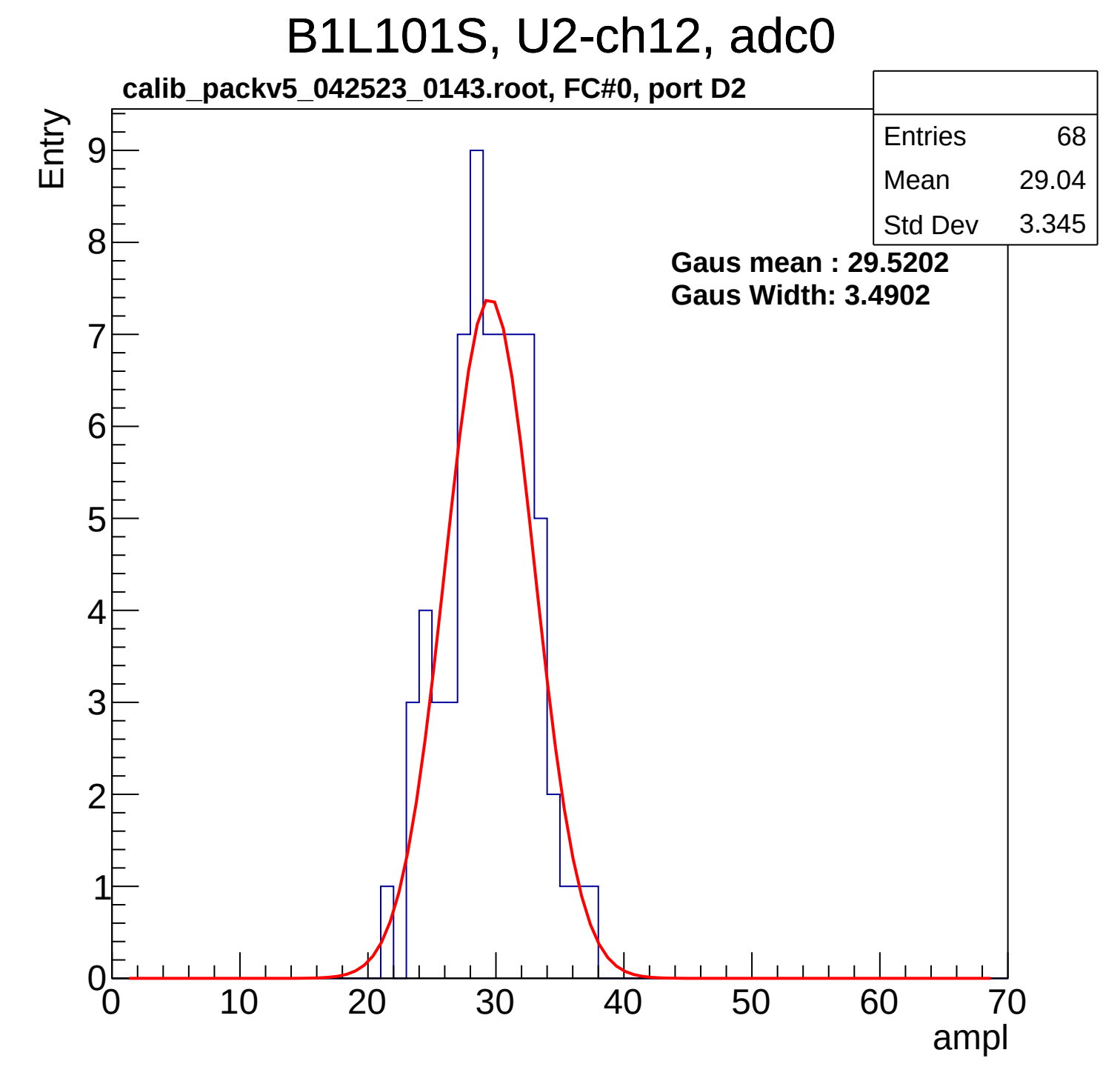

B1L101S, U2-ch11, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 49.4
Std Dev 3.313
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

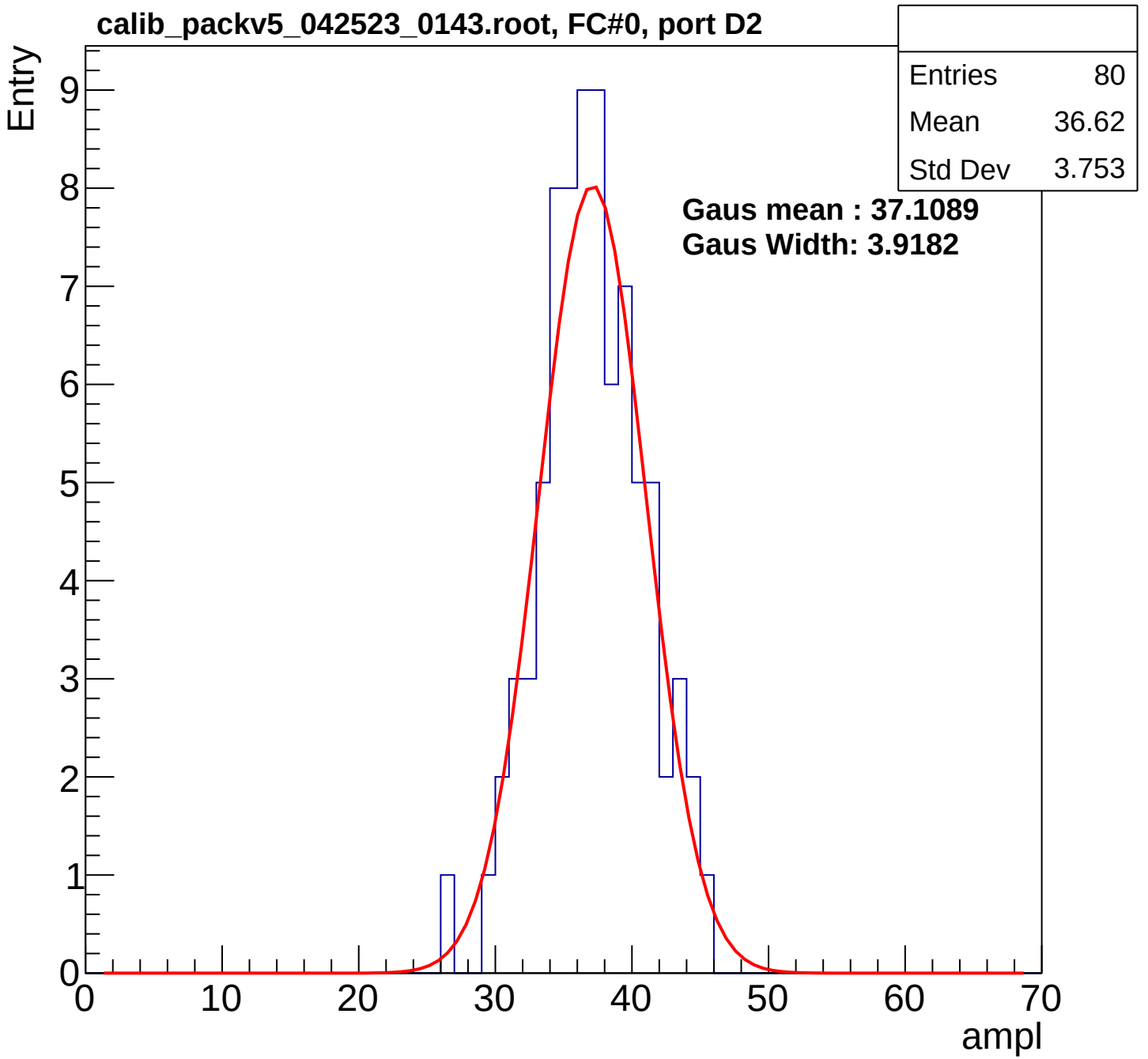

B1L101S, U2-ch11, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 55.58
Std Dev 3.114
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

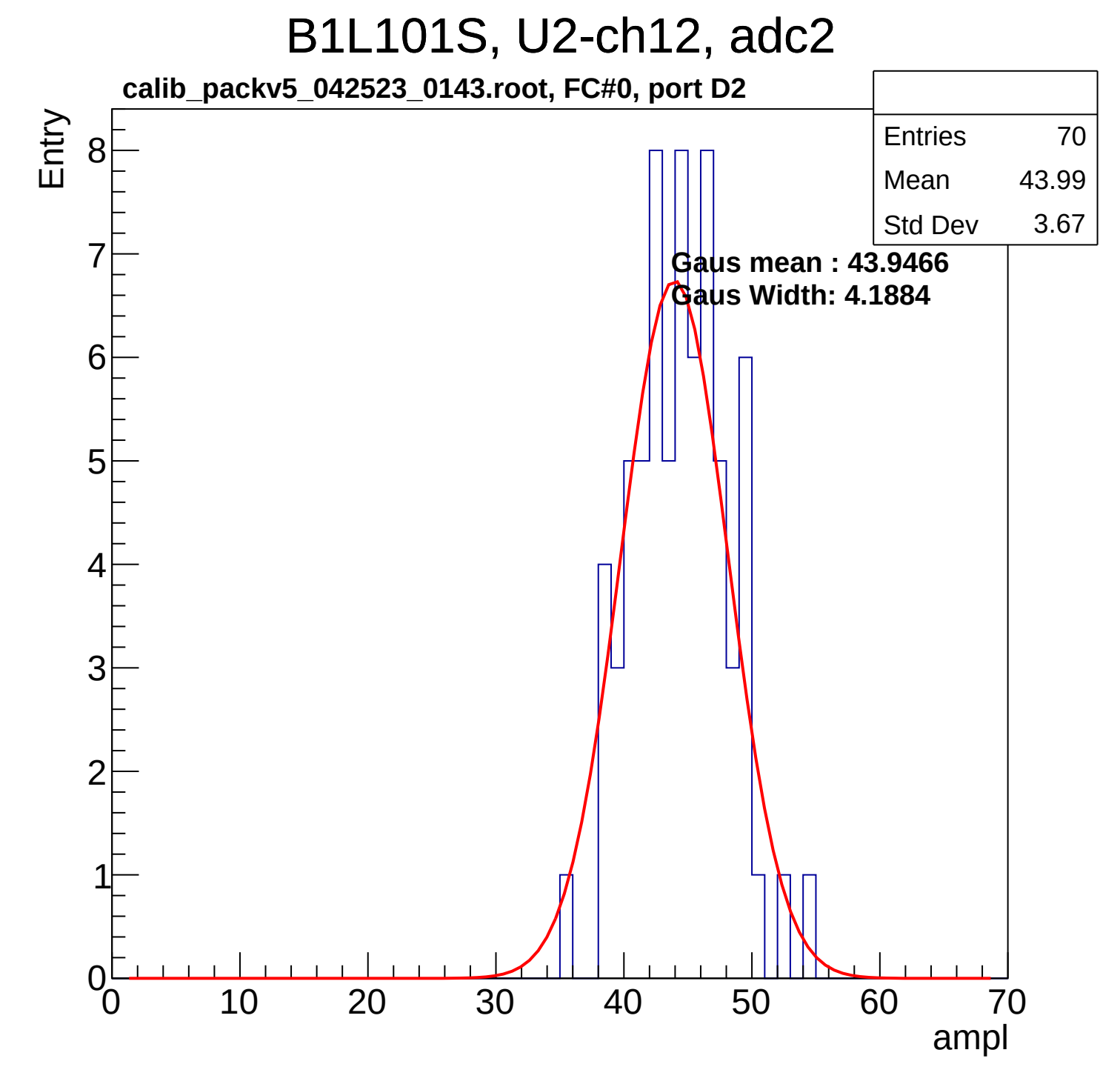

B1L101S, U2-ch11, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 40
Mean 59.2
Std Dev 9.639
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

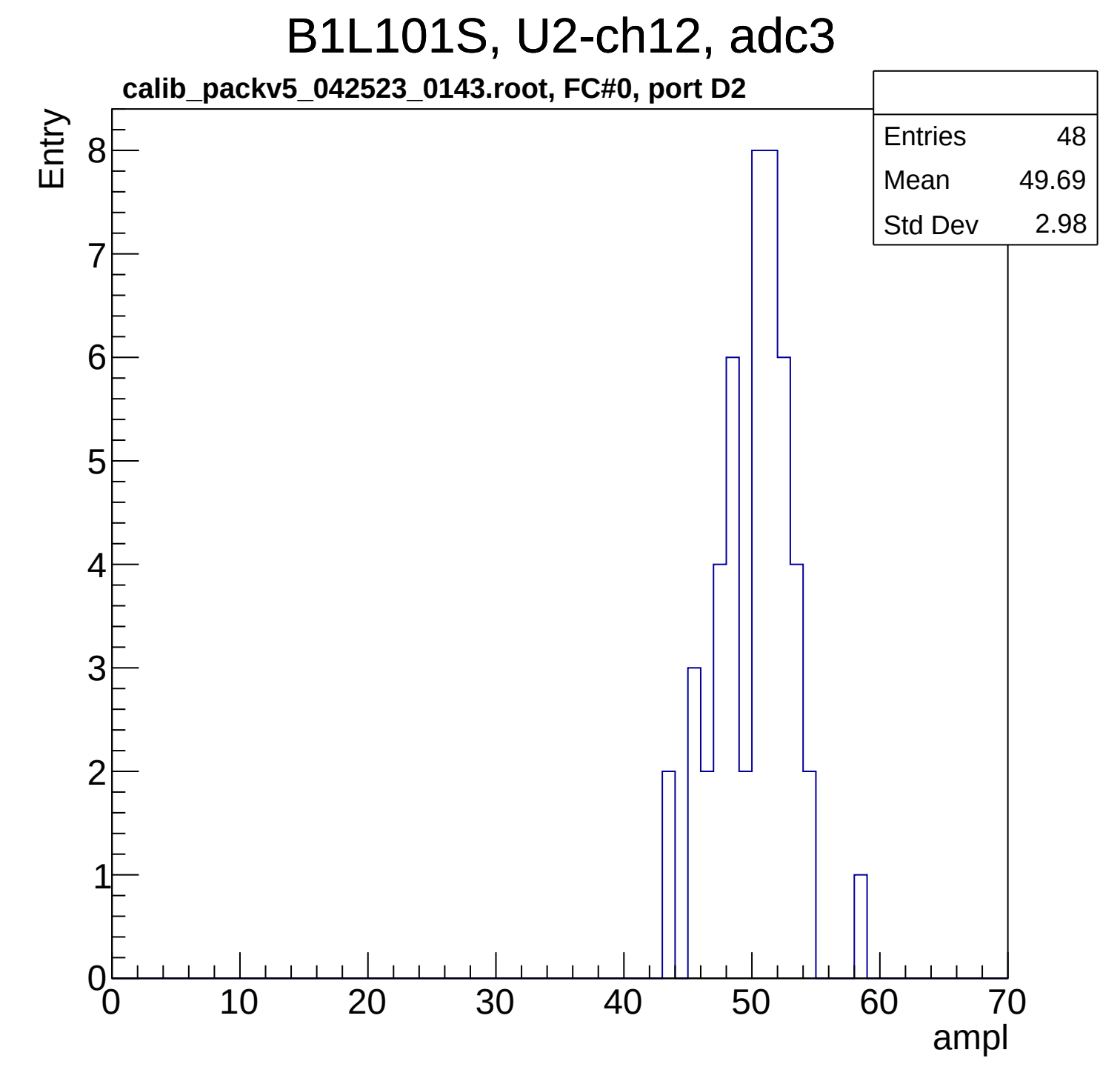

B1L101S, U2-ch11, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 61.25
Std Dev 1.785
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

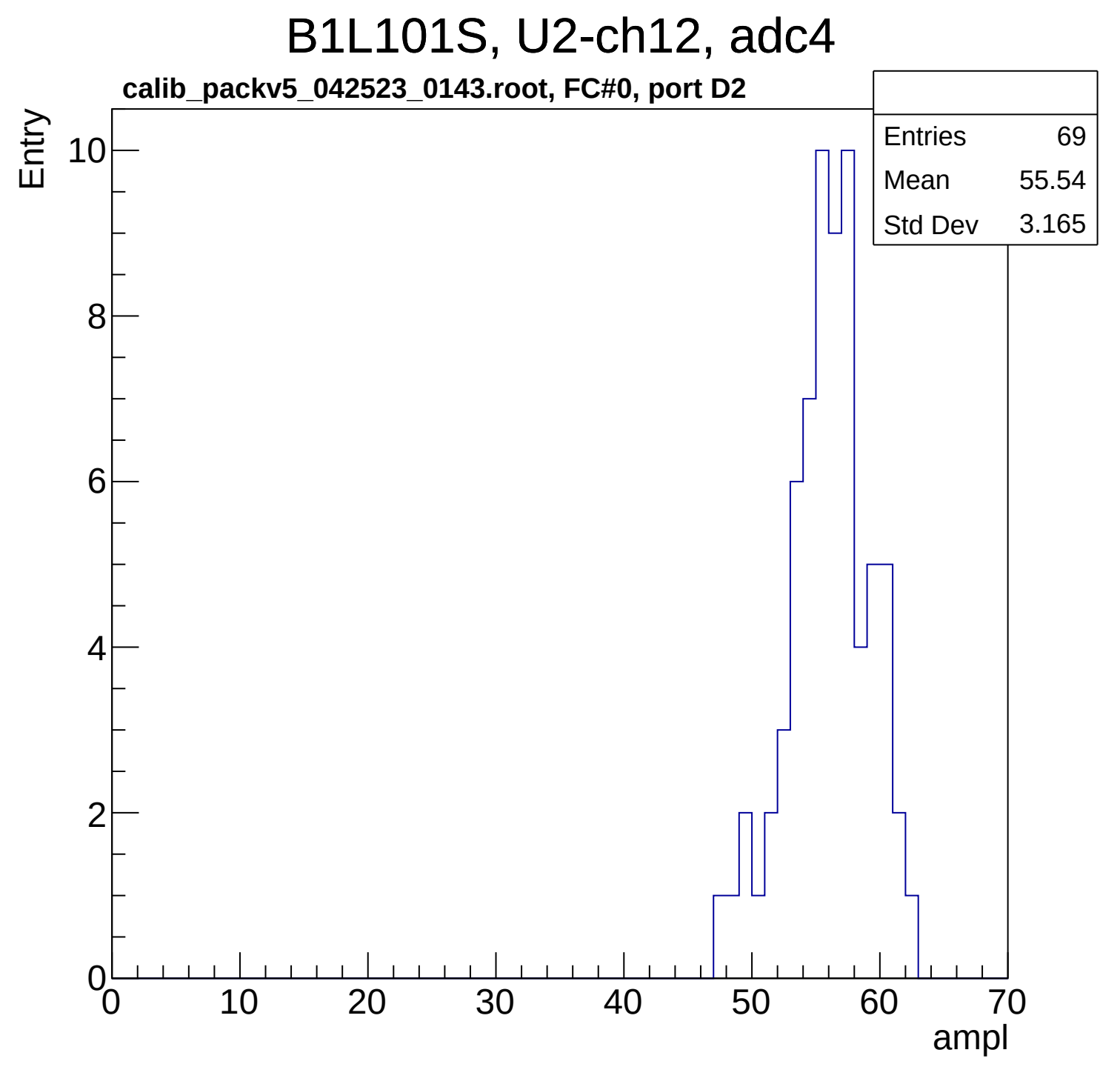

B1L101S, U2-ch11, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 21
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

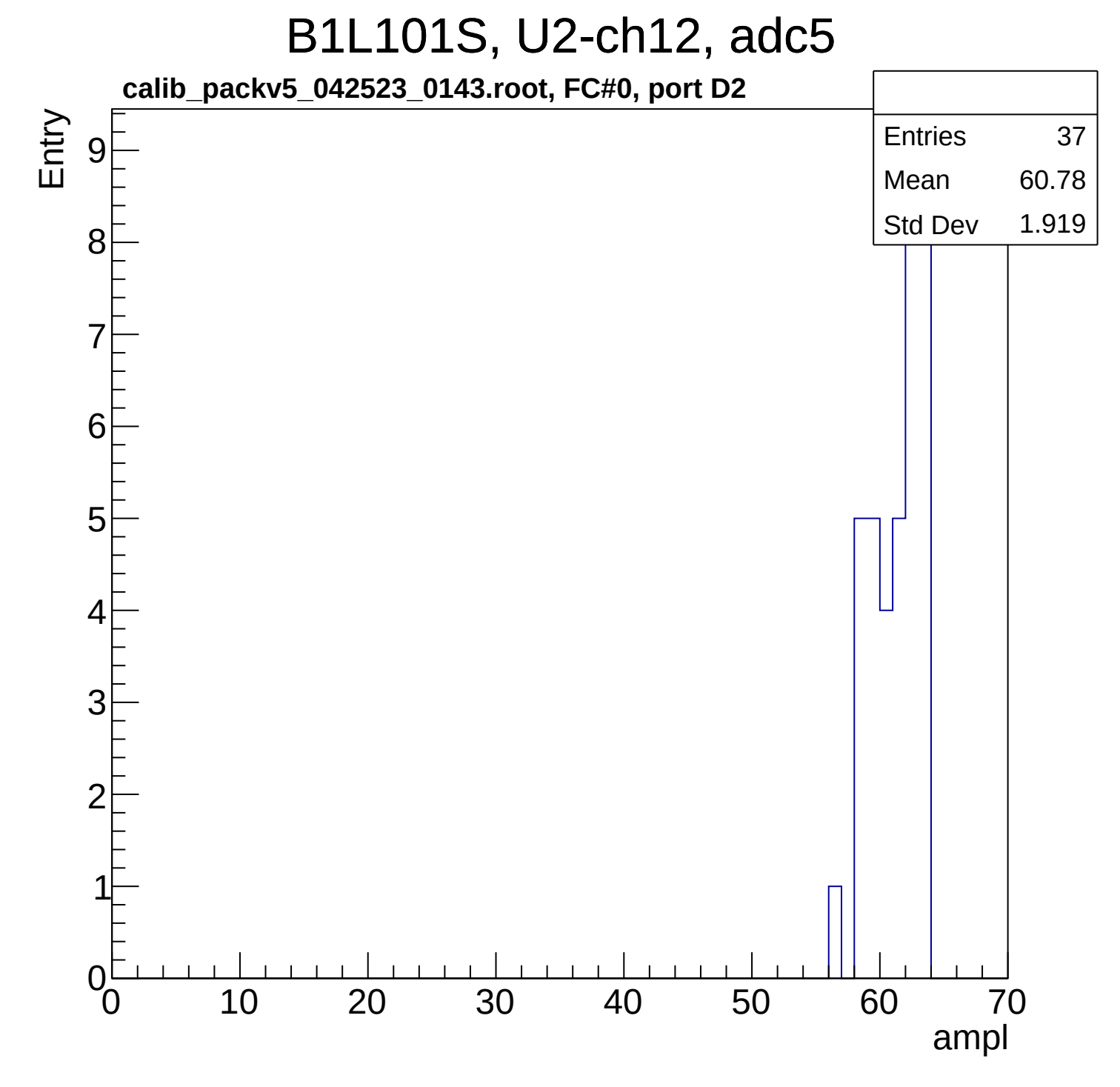

B1L101S, U2-ch12, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 29.04
Std Dev 3.345
Gaus mean : 29.5202
Gaus Width: 3.4902
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

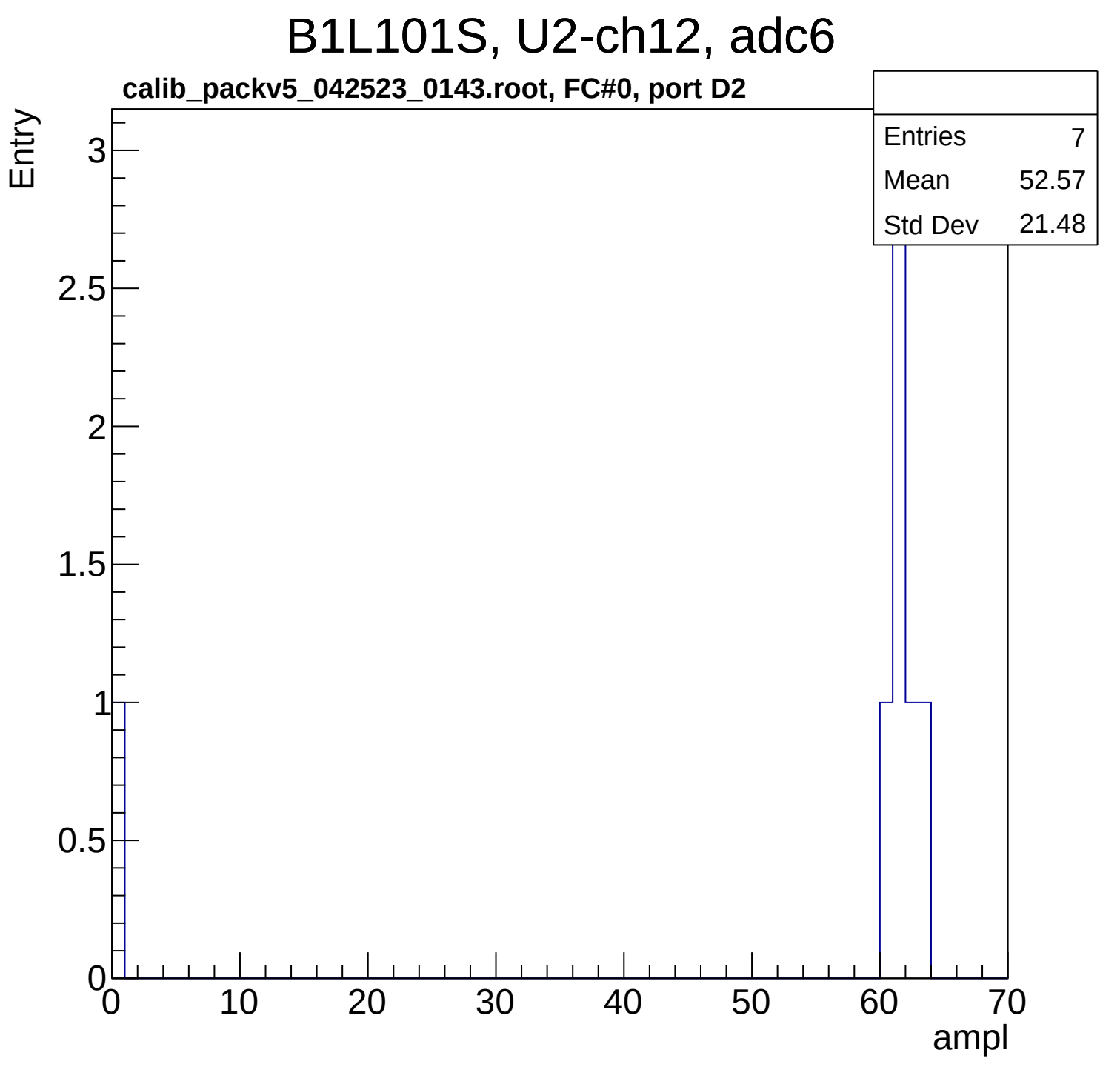

B1L101S, U2-ch12, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 80
Mean 36.62
Std Dev 3.753
Gaus mean : 37.1089
Gaus Width: 3.9182
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

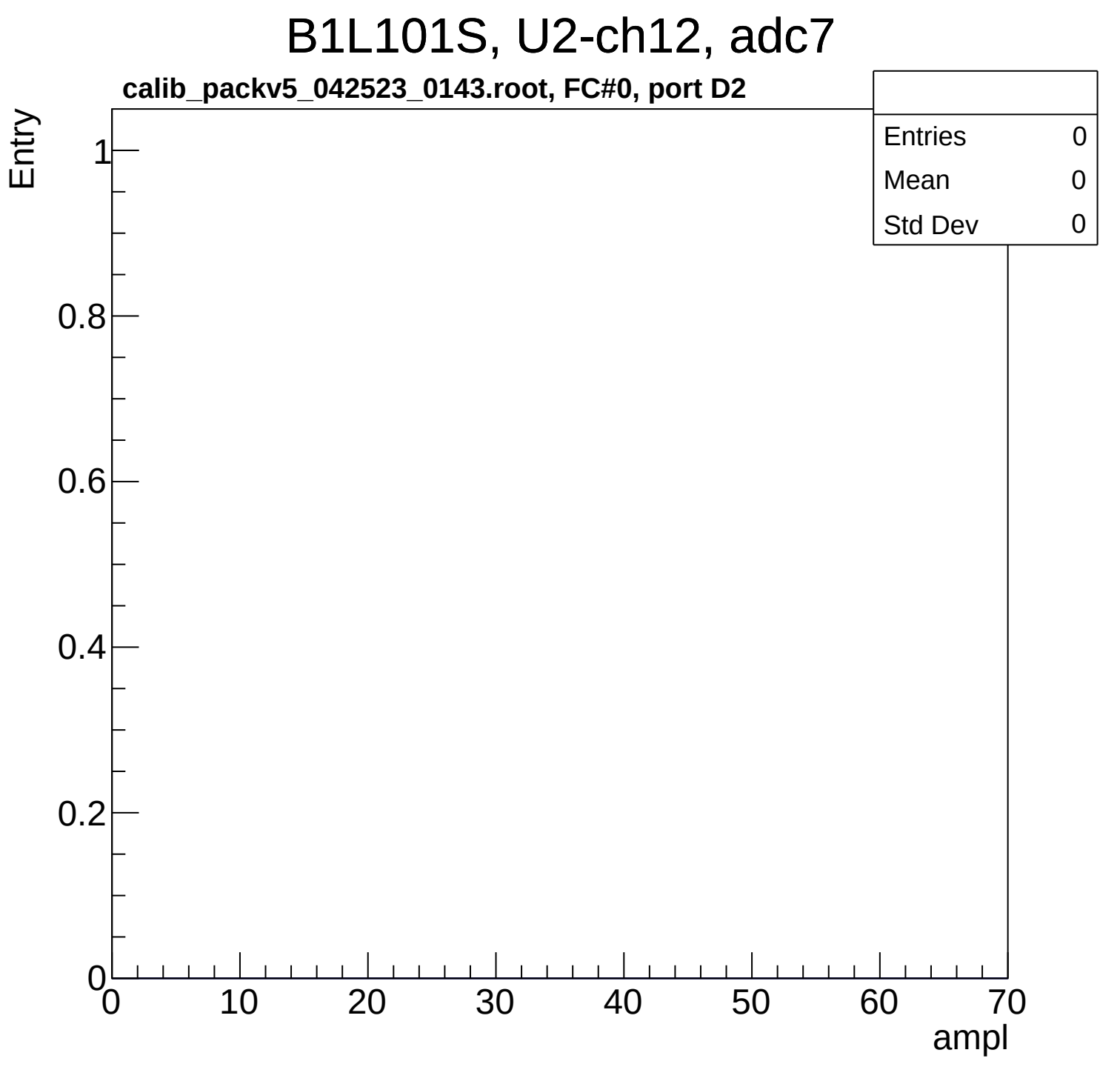

B1L101S, U2-ch12, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 43.99
Std Dev 3.67
Gaus mean : 43.9466
Gaus Width: 4.1884
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

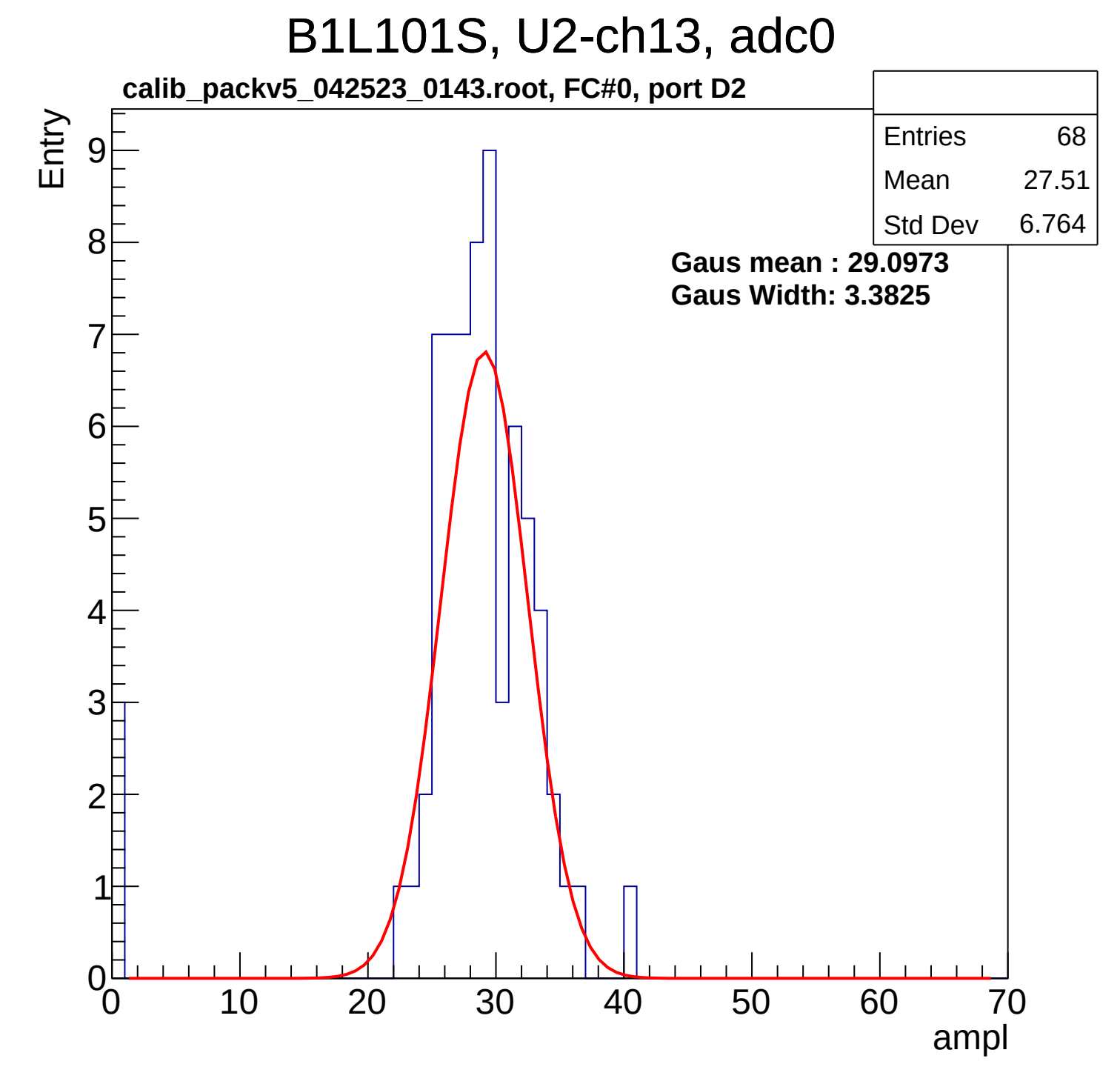

B1L101S, U2-ch12, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 49.69
Std Dev 2.98
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

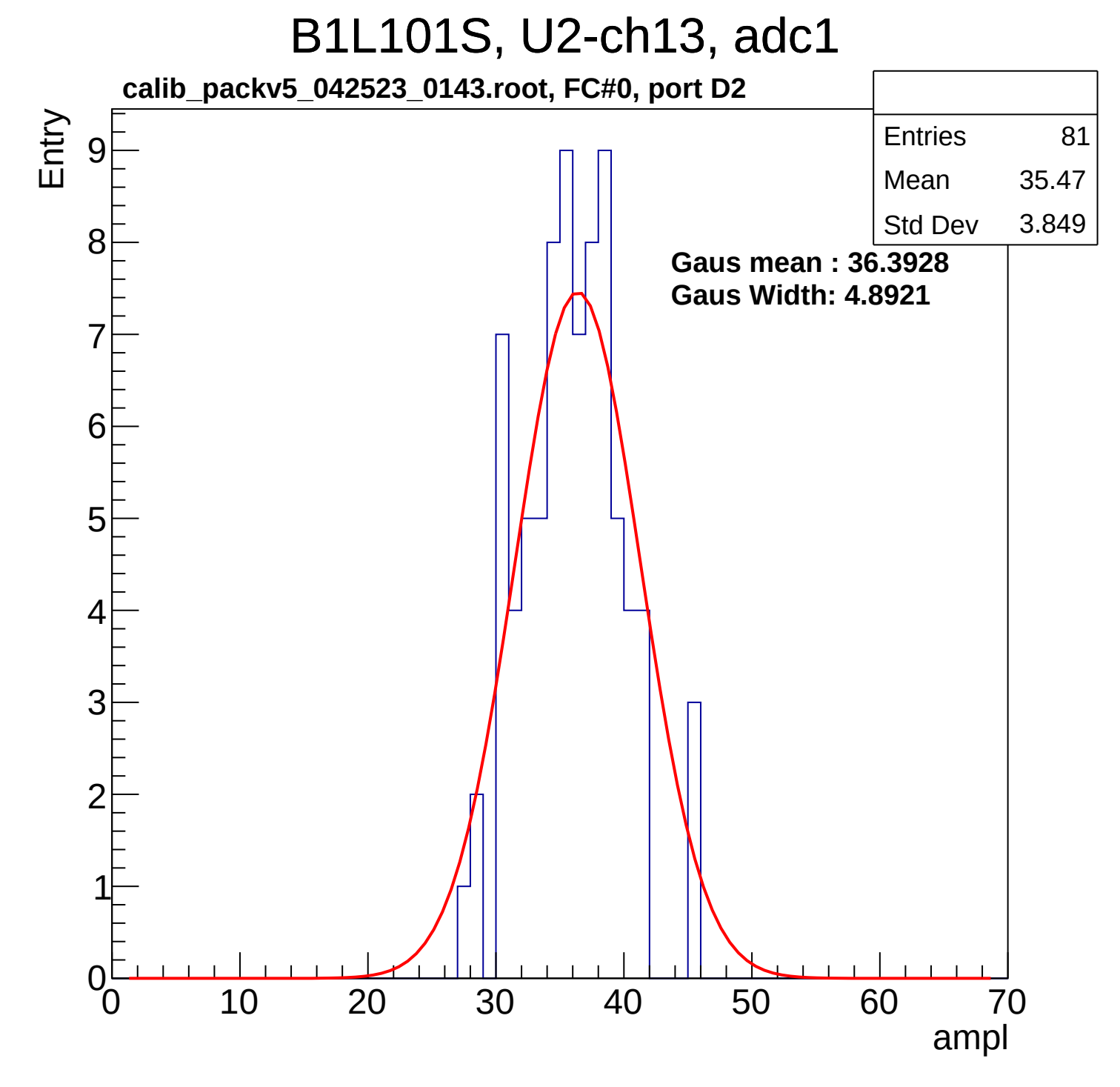

B1L101S, U2-ch12, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 55.54
Std Dev 3.165
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

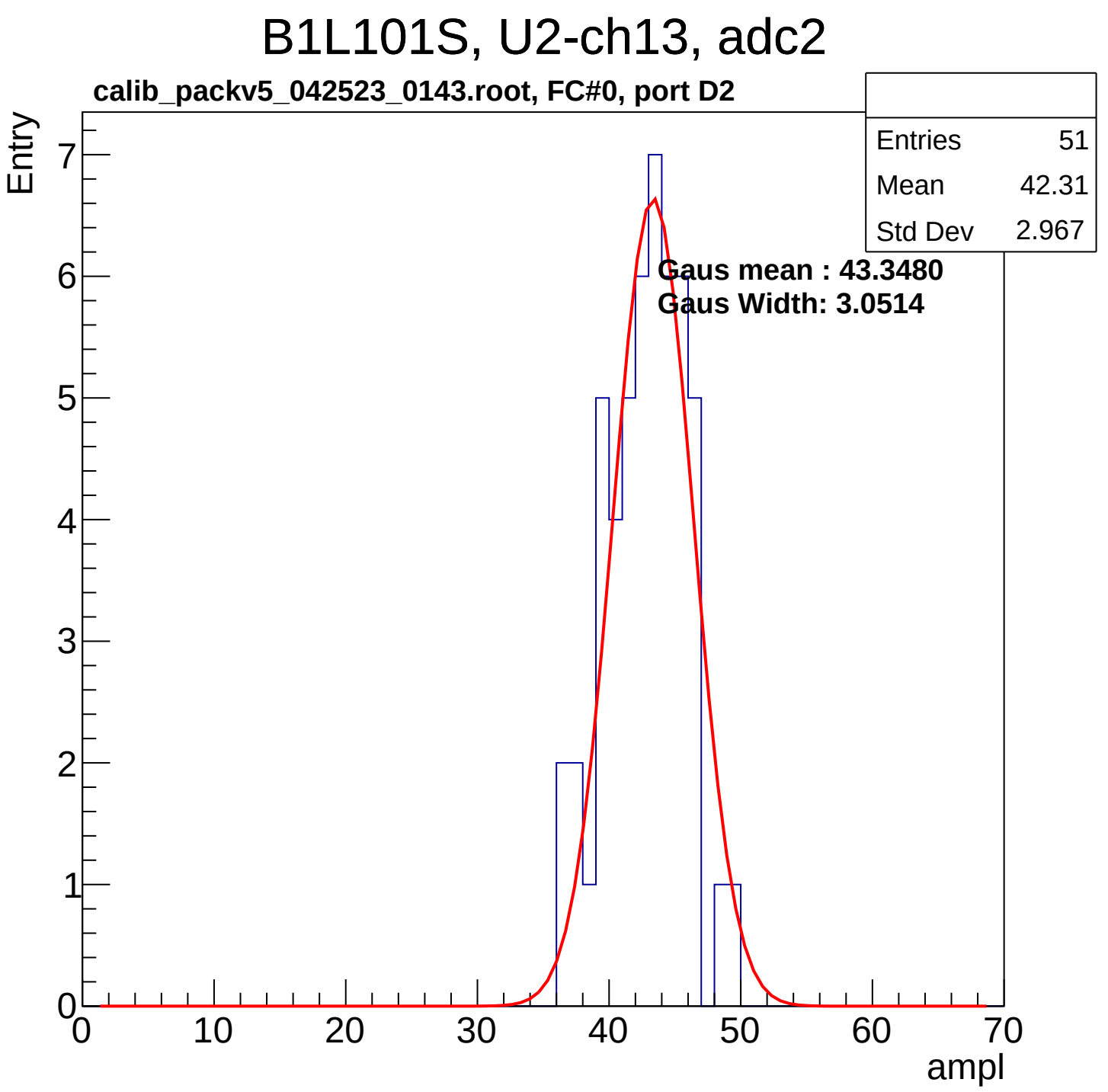

B1L101S, U2-ch12, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 37
Mean 60.78
Std Dev 1.919
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

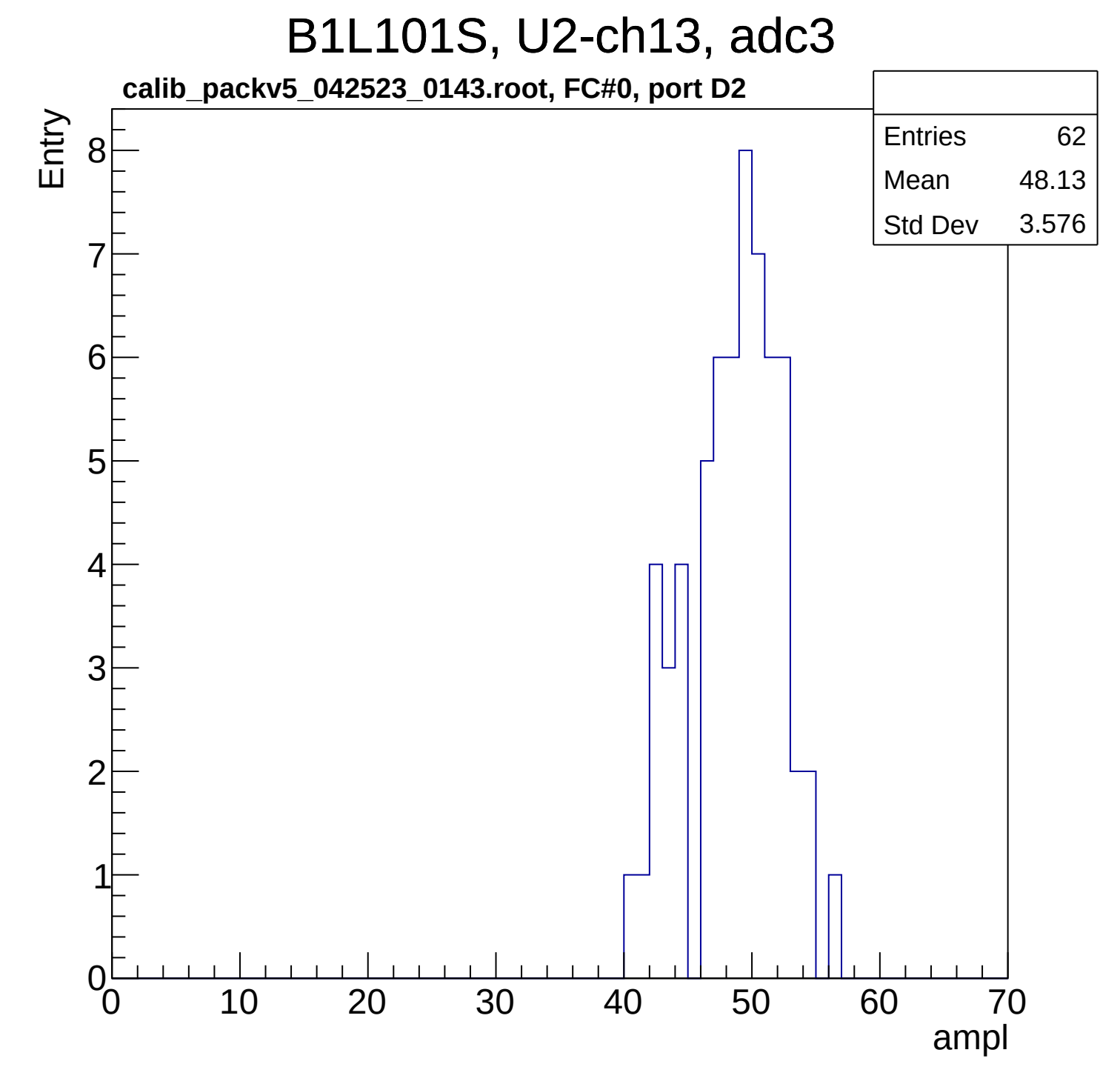

B1L101S, U2-ch12, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 52.57
Std Dev 21.48
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

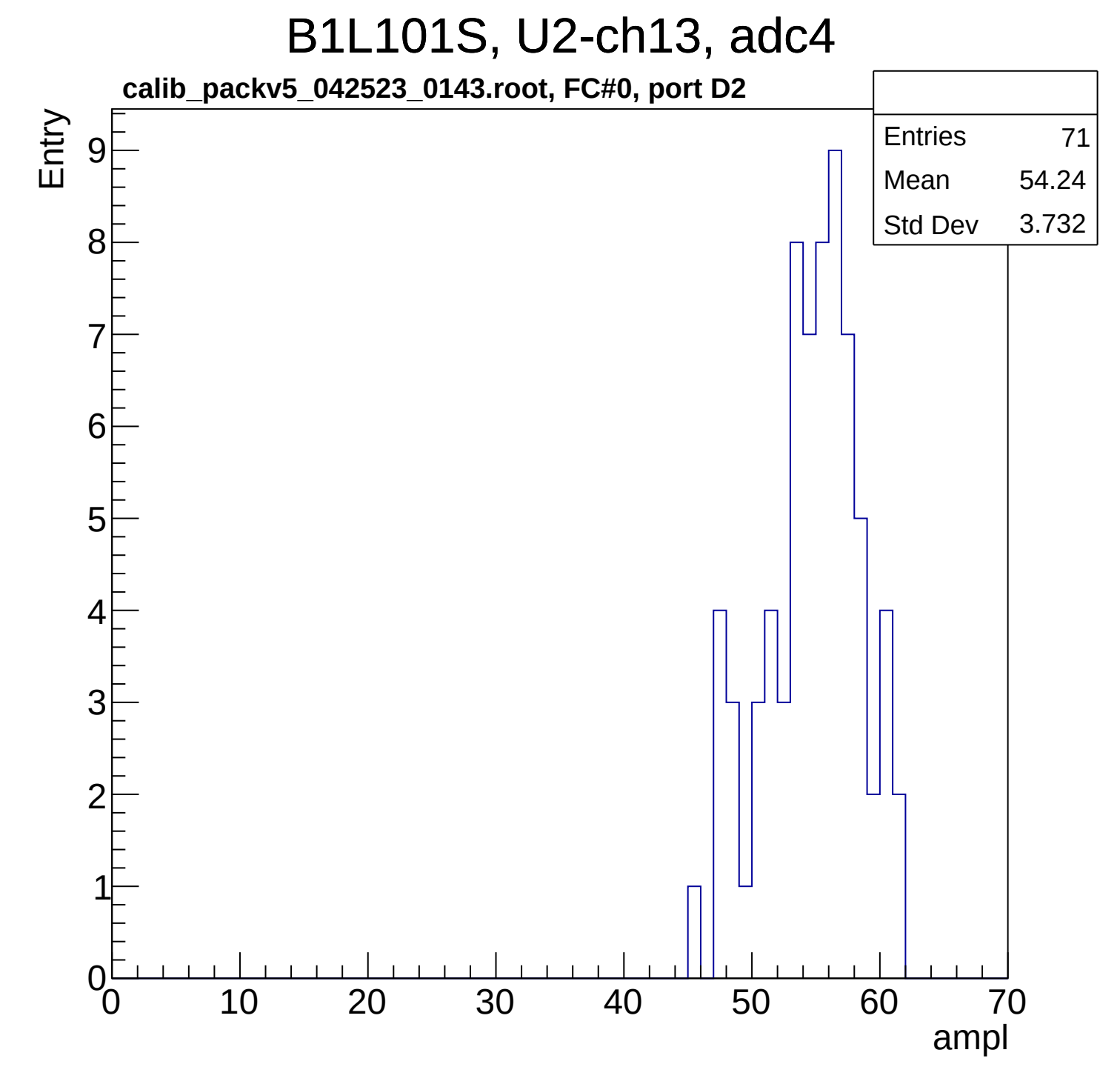

B1L101S, U2-ch12, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

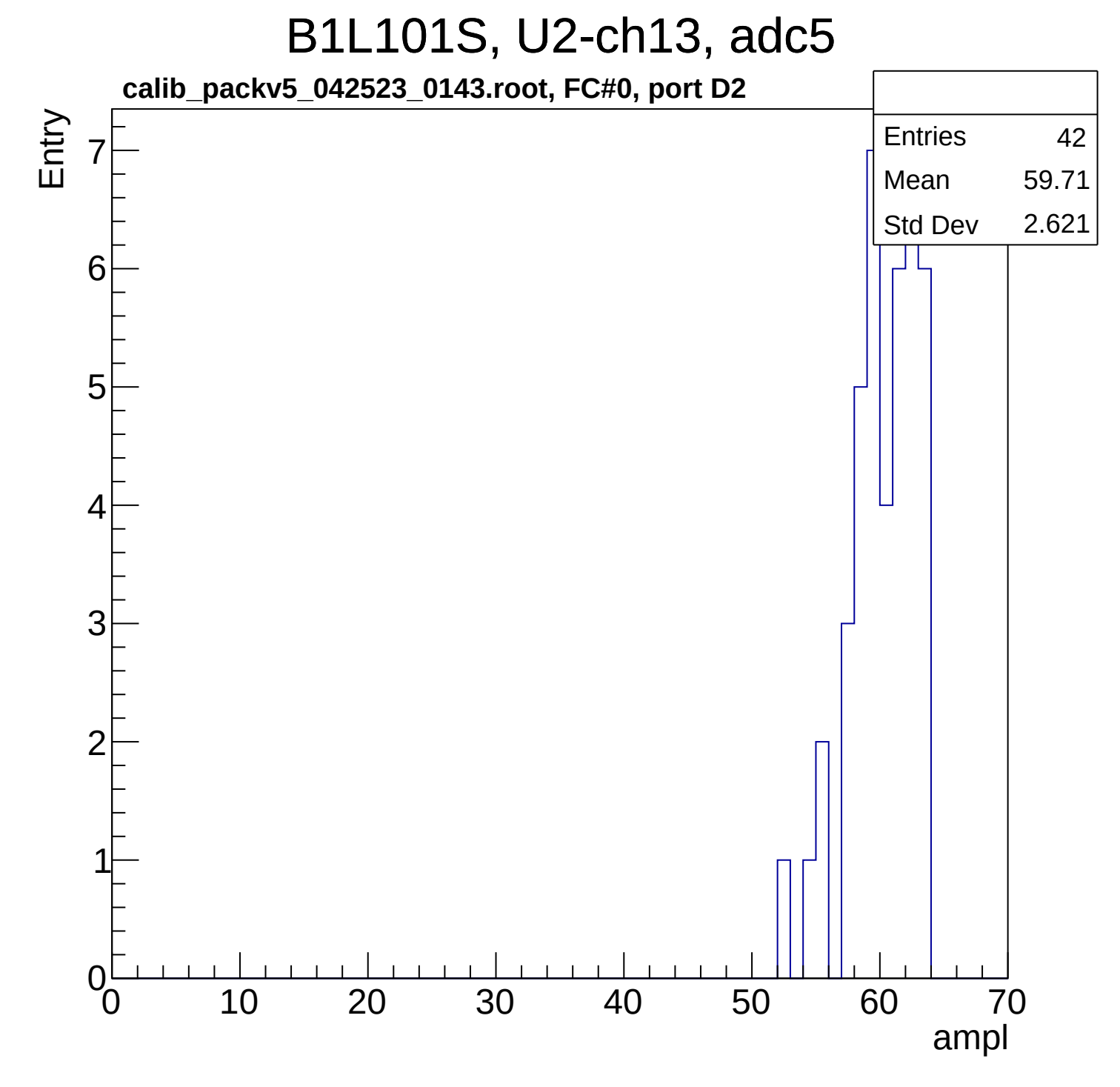

B1L101S, U2-ch13, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 27.51
Std Dev 6.764
Gaus mean : 29.0973
Gaus Width: 3.3825
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

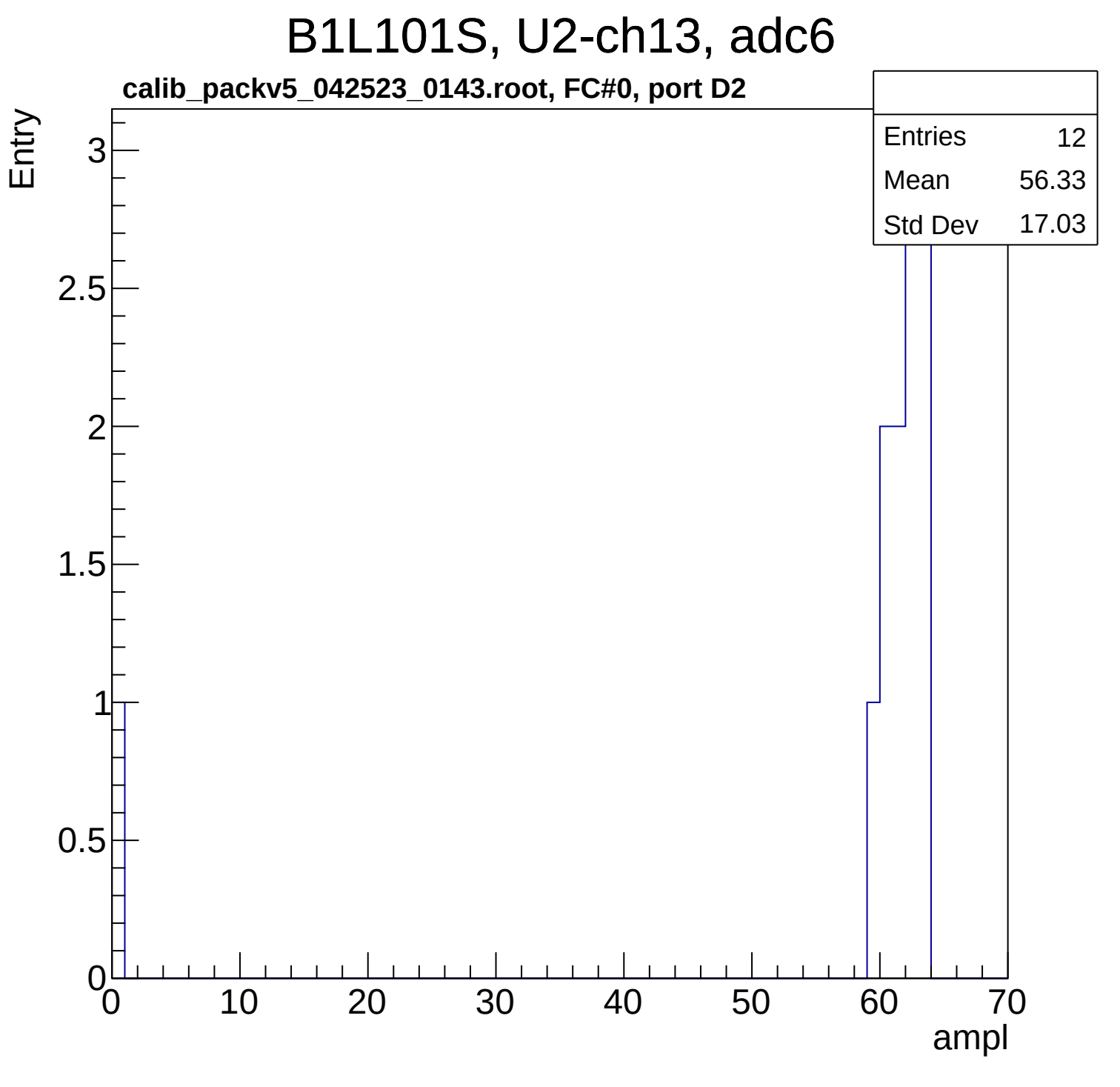

B1L101S, U2-ch13, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 81
Mean 35.47
Std Dev 3.849
Gaus mean : 36.3928
Gaus Width: 4.8921
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

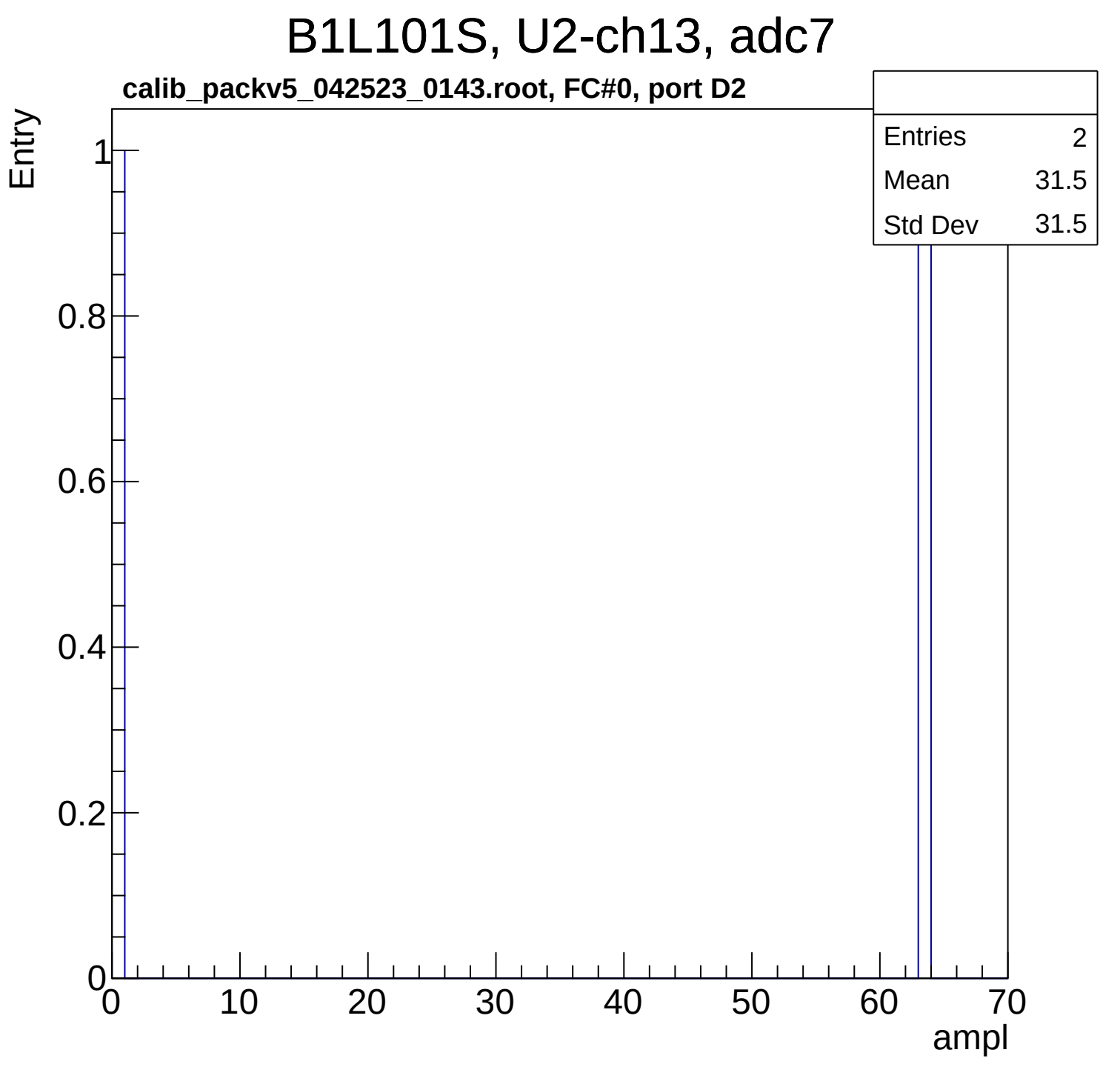

B1L101S, U2-ch13, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 42.31
Std Dev 2.967
Gaus mean : 43.3480
Gaus Width: 3.0514
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

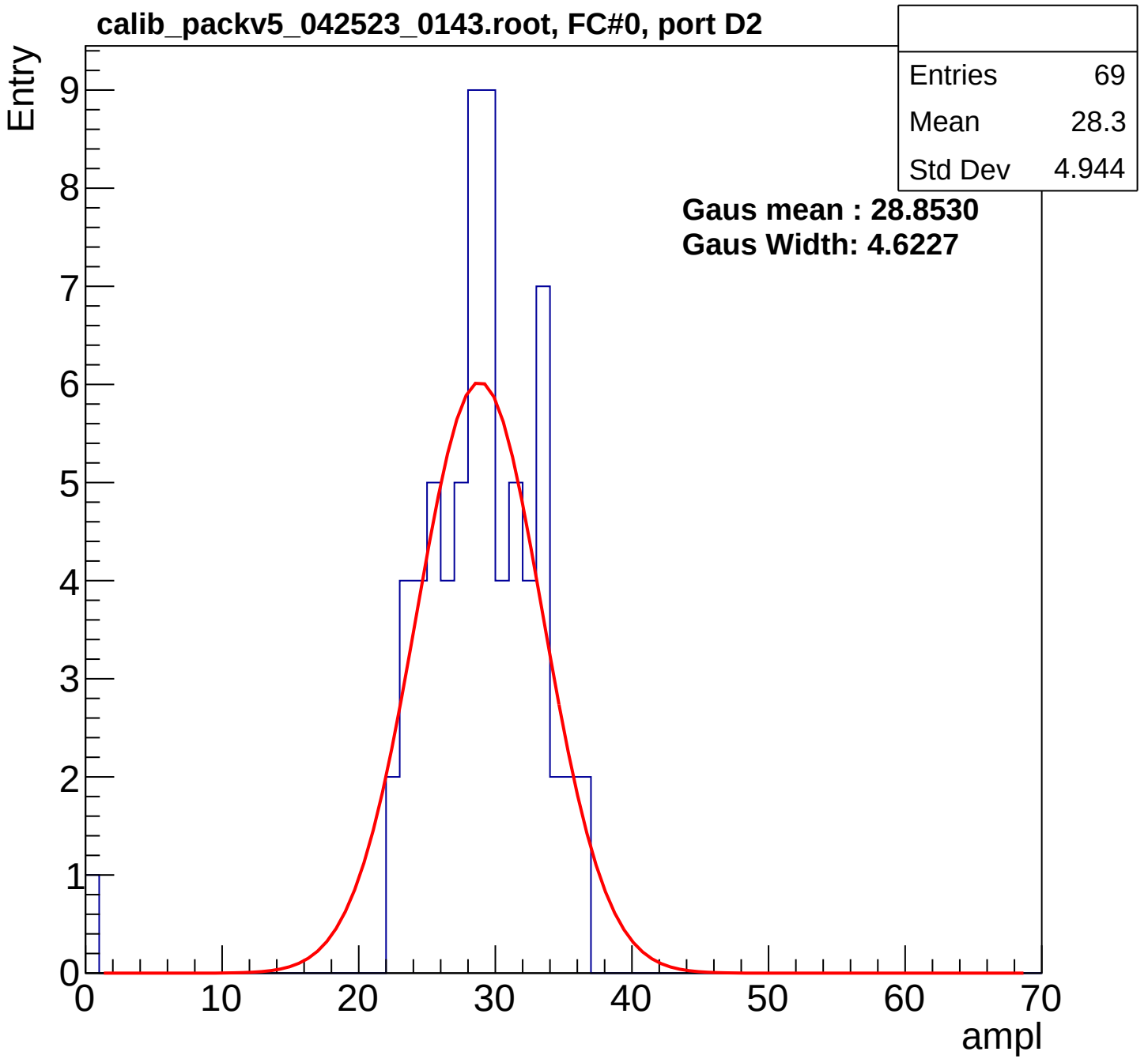

B1L101S, U2-ch13, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 48.13
Std Dev 3.576
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

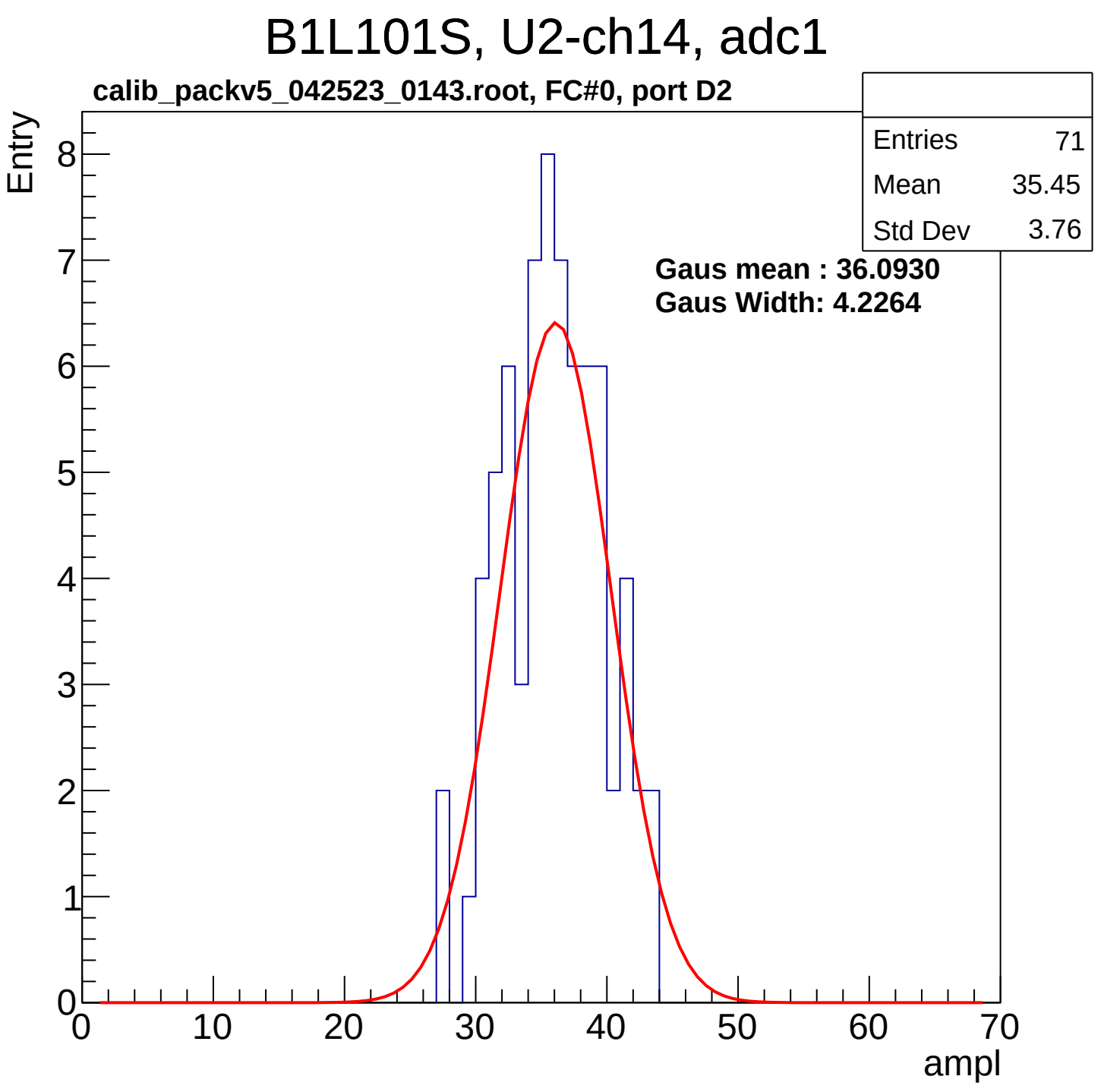

B1L101S, U2-ch13, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 54.24
Std Dev 3.732
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

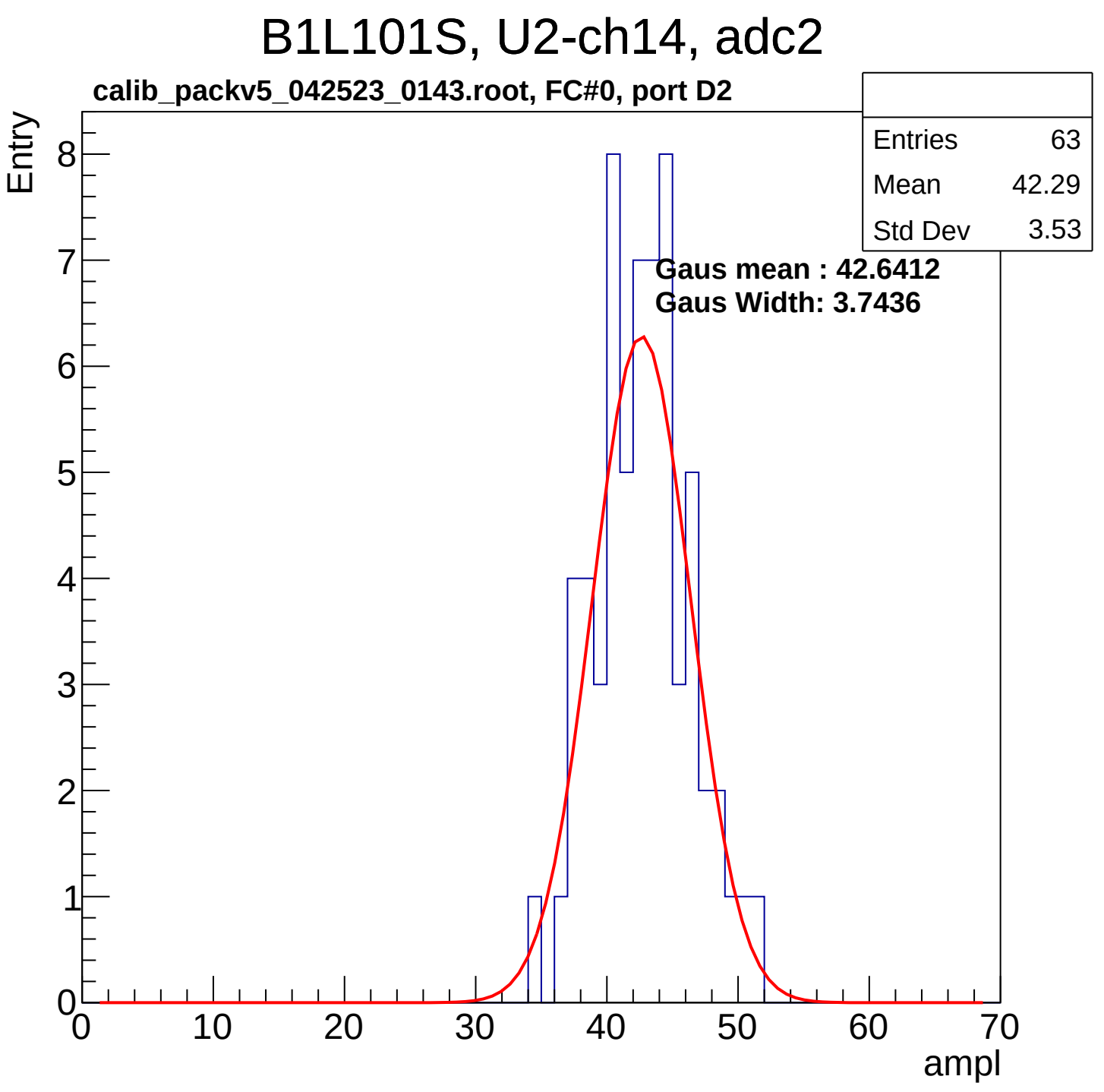

B1L101S, U2-ch13, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 59.71
Std Dev 2.621
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

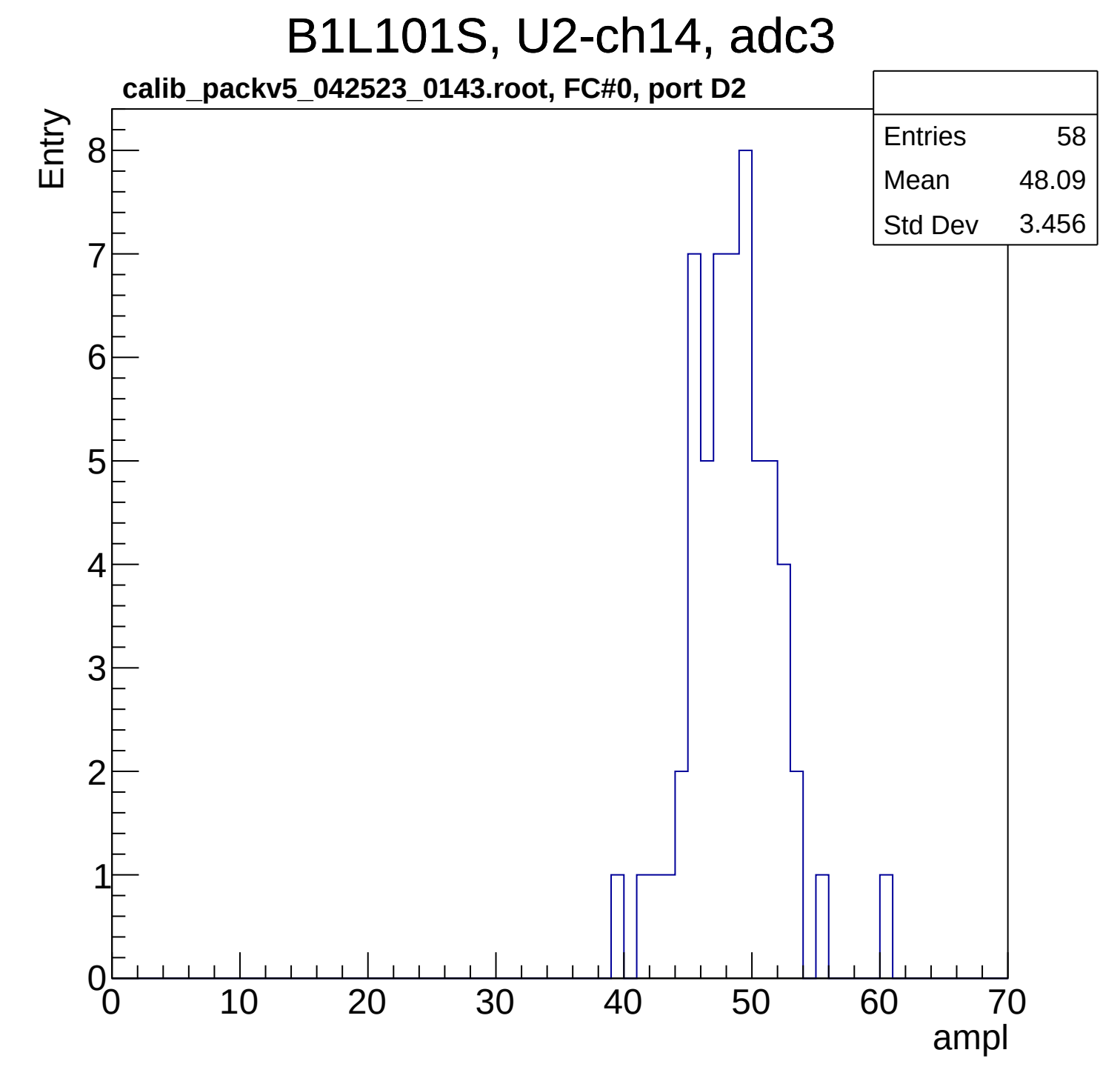

B1L101S, U2-ch13, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 12
Mean 56.33
Std Dev 17.03
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl

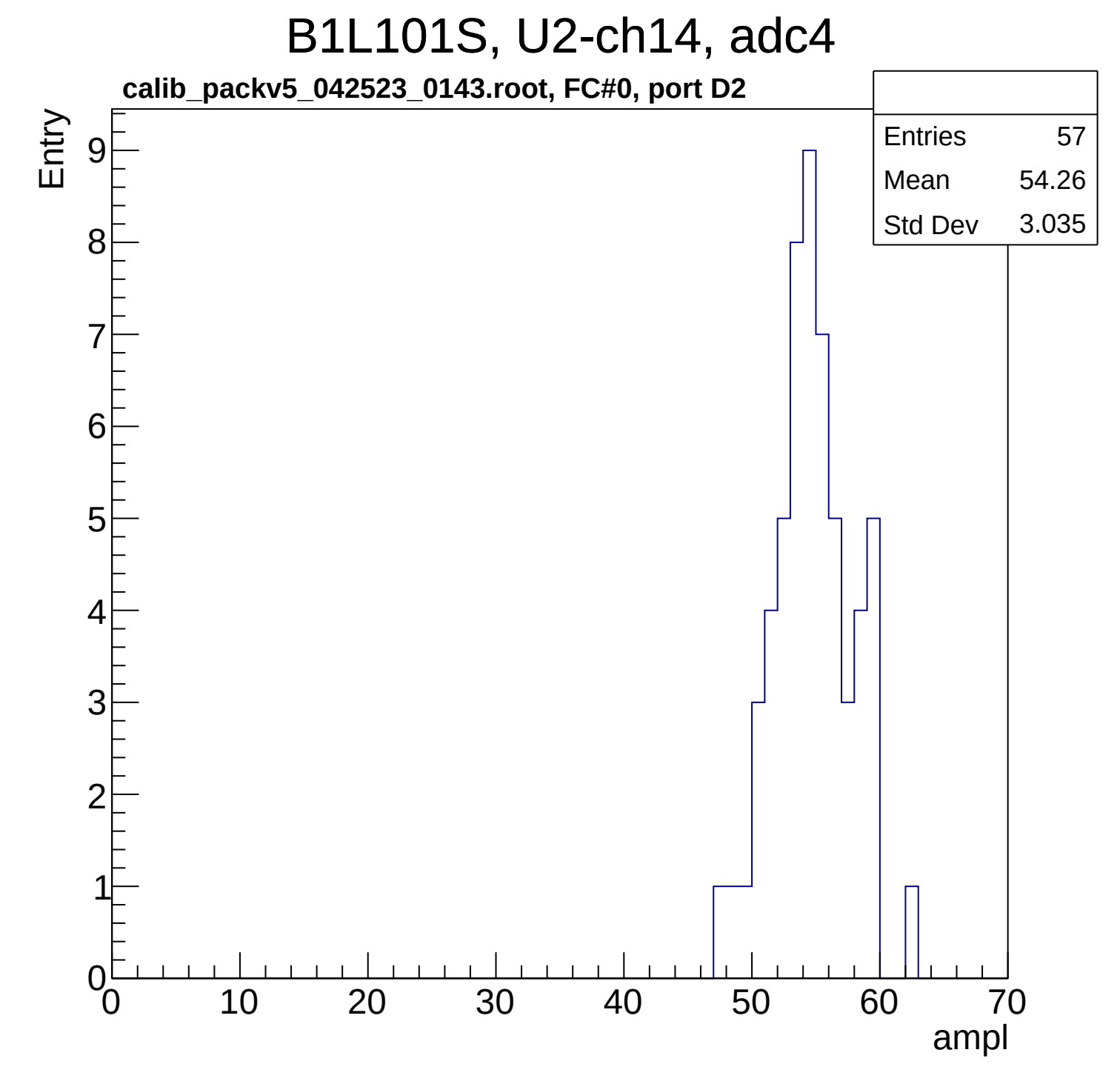

B1L101S, U2-ch13, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

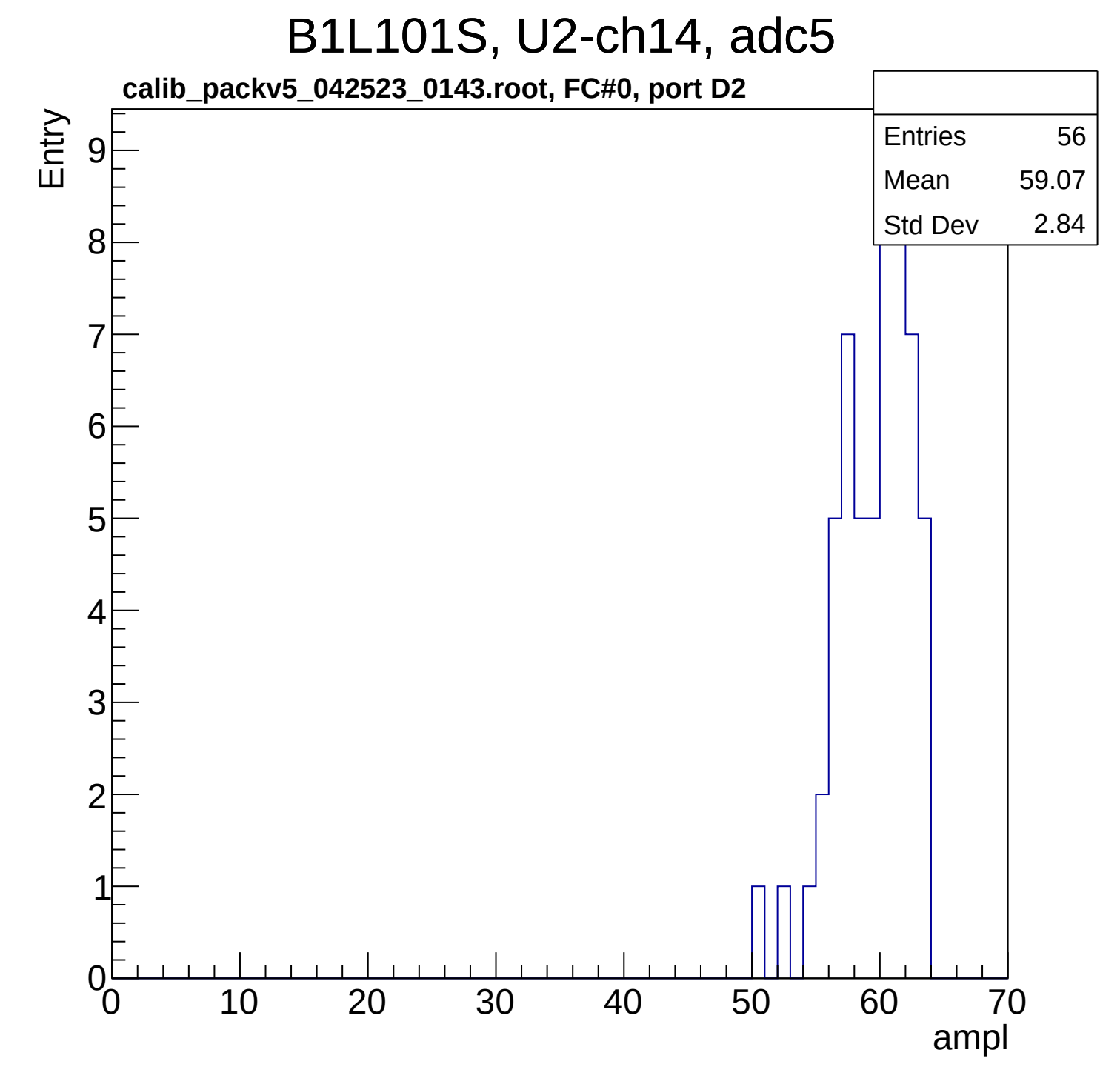

B1L101S, U2-ch14, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 28.3
Std Dev 4.944
Gaus mean : 28.8530
Gaus Width: 4.6227
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

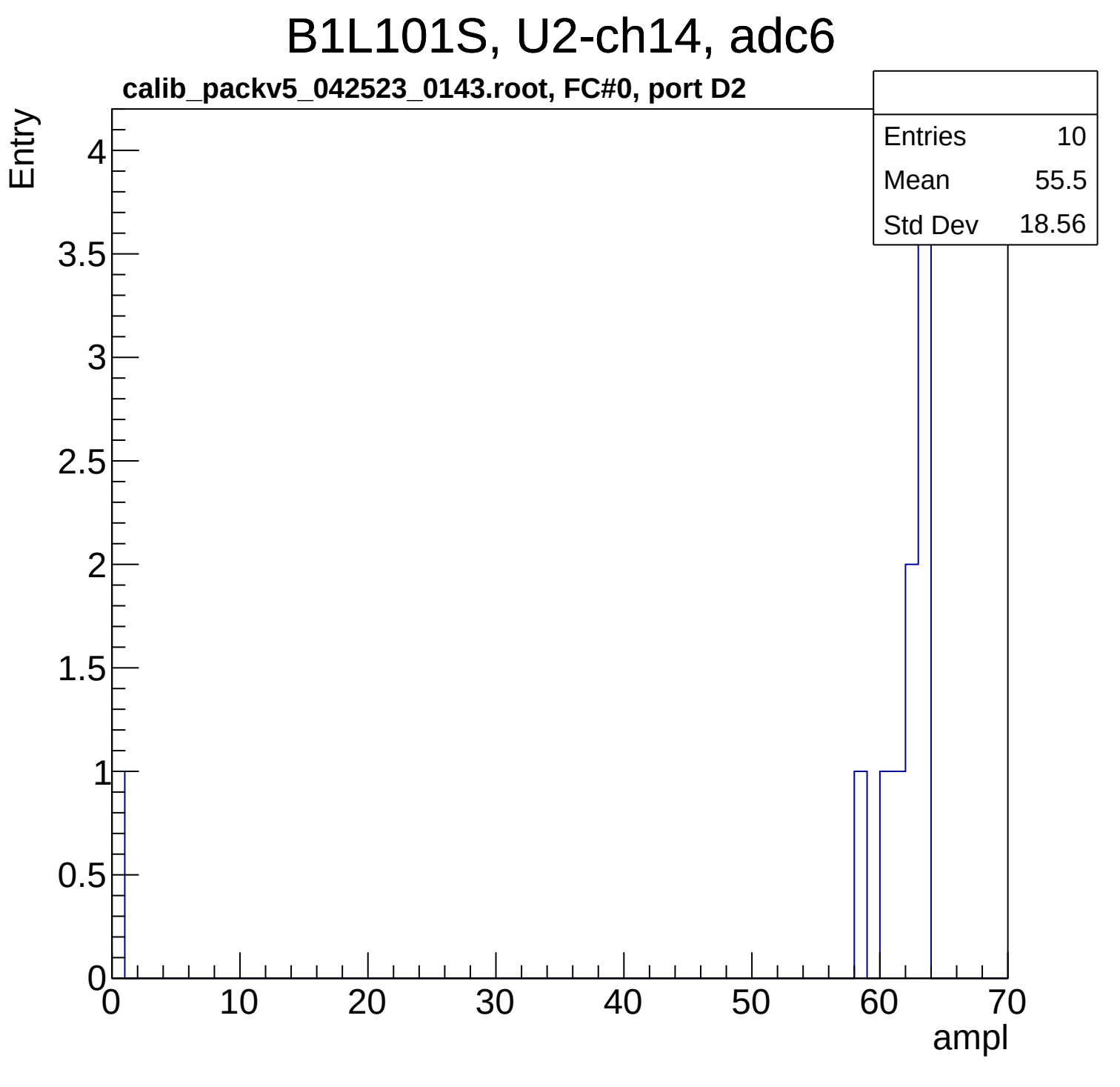

B1L101S, U2-ch14, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 35.45
Std Dev 3.76
Gaus mean : 36.0930
Gaus Width: 4.2264
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

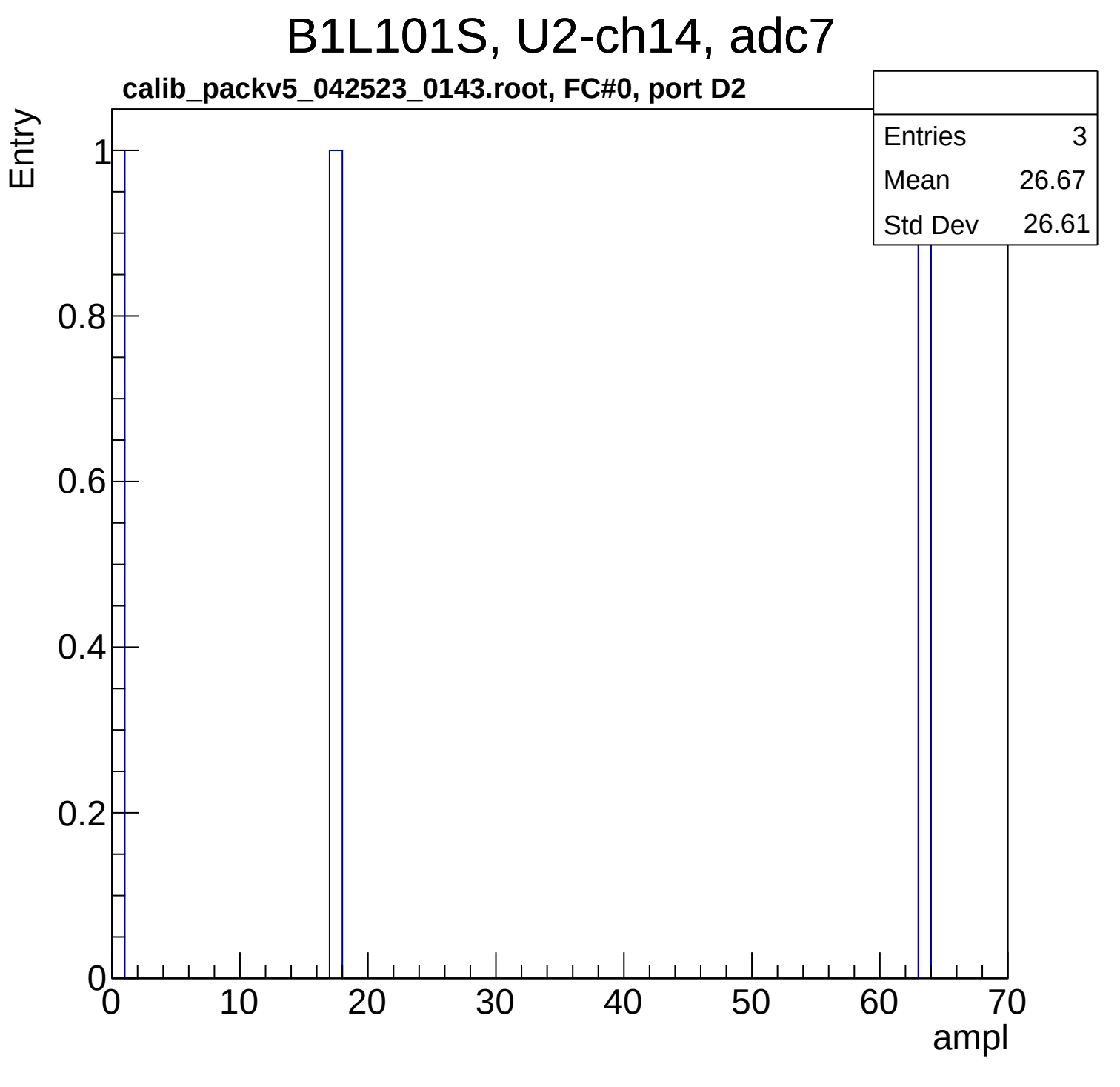

B1L101S, U2-ch14, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 42.29
Std Dev 3.53
Gaus mean : 42.6412
Gaus Width: 3.7436
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

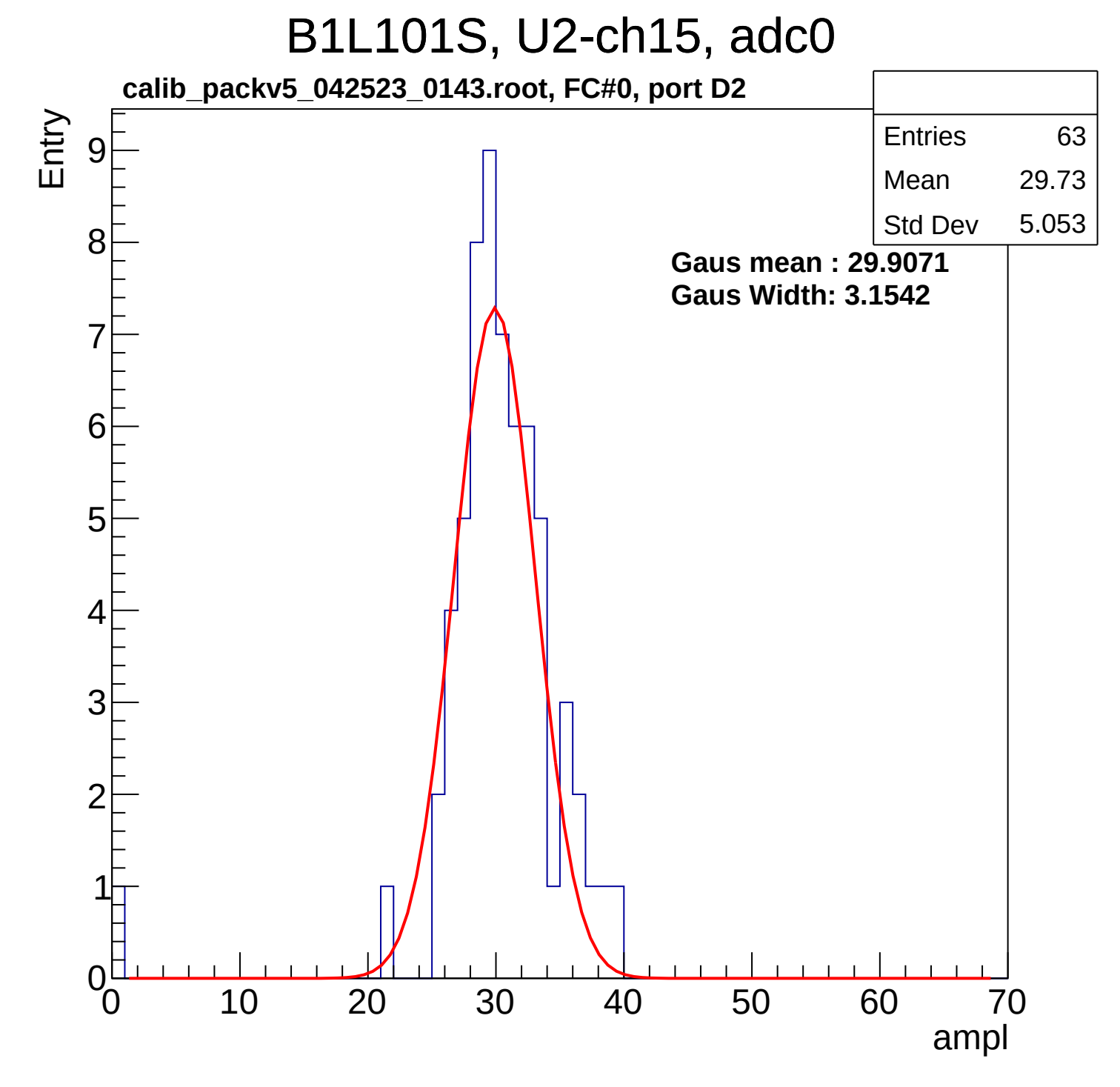

B1L101S, U2-ch14, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 48.09
Std Dev 3.456
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

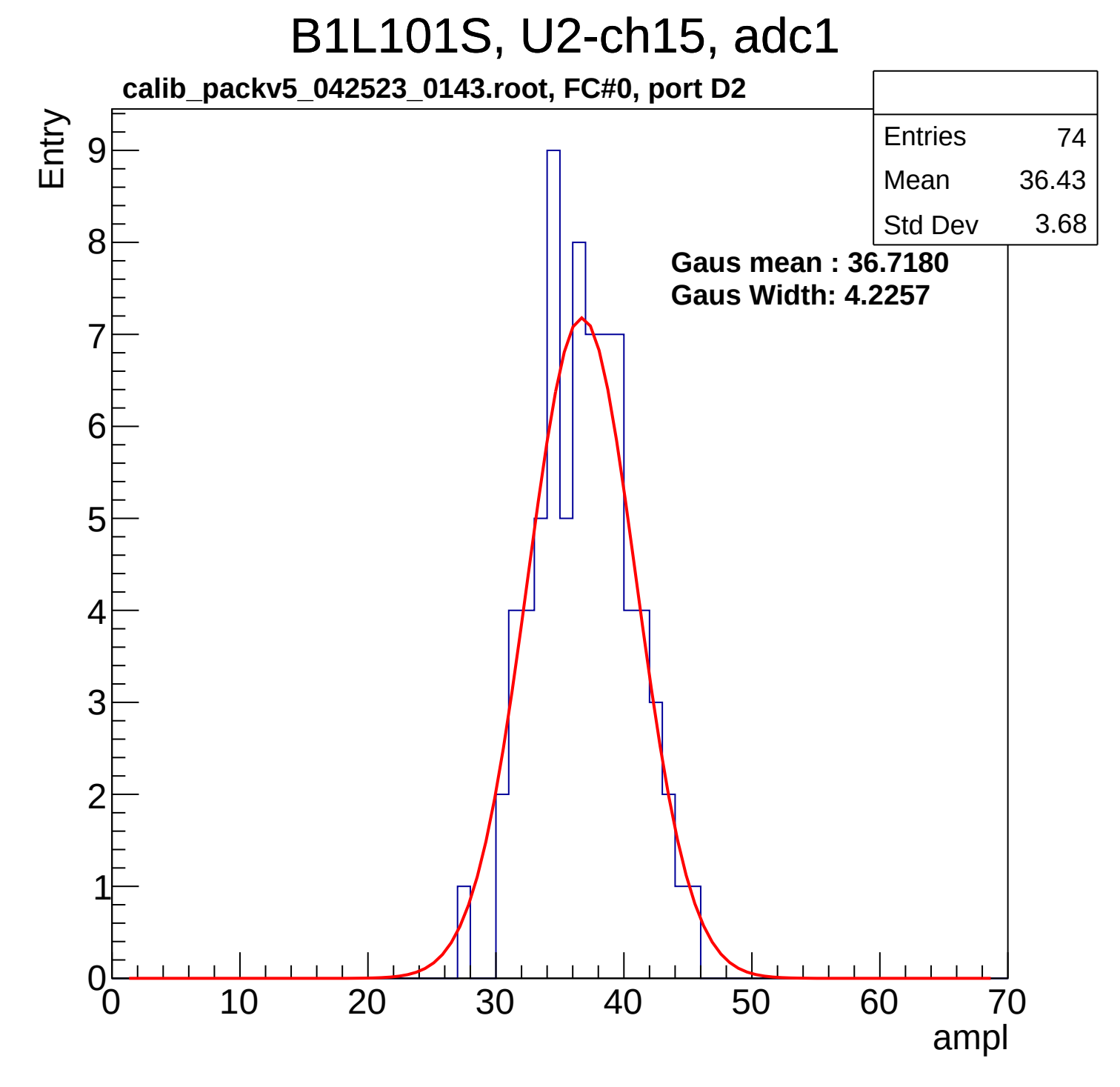

B1L101S, U2-ch14, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 54.26
Std Dev 3.035
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

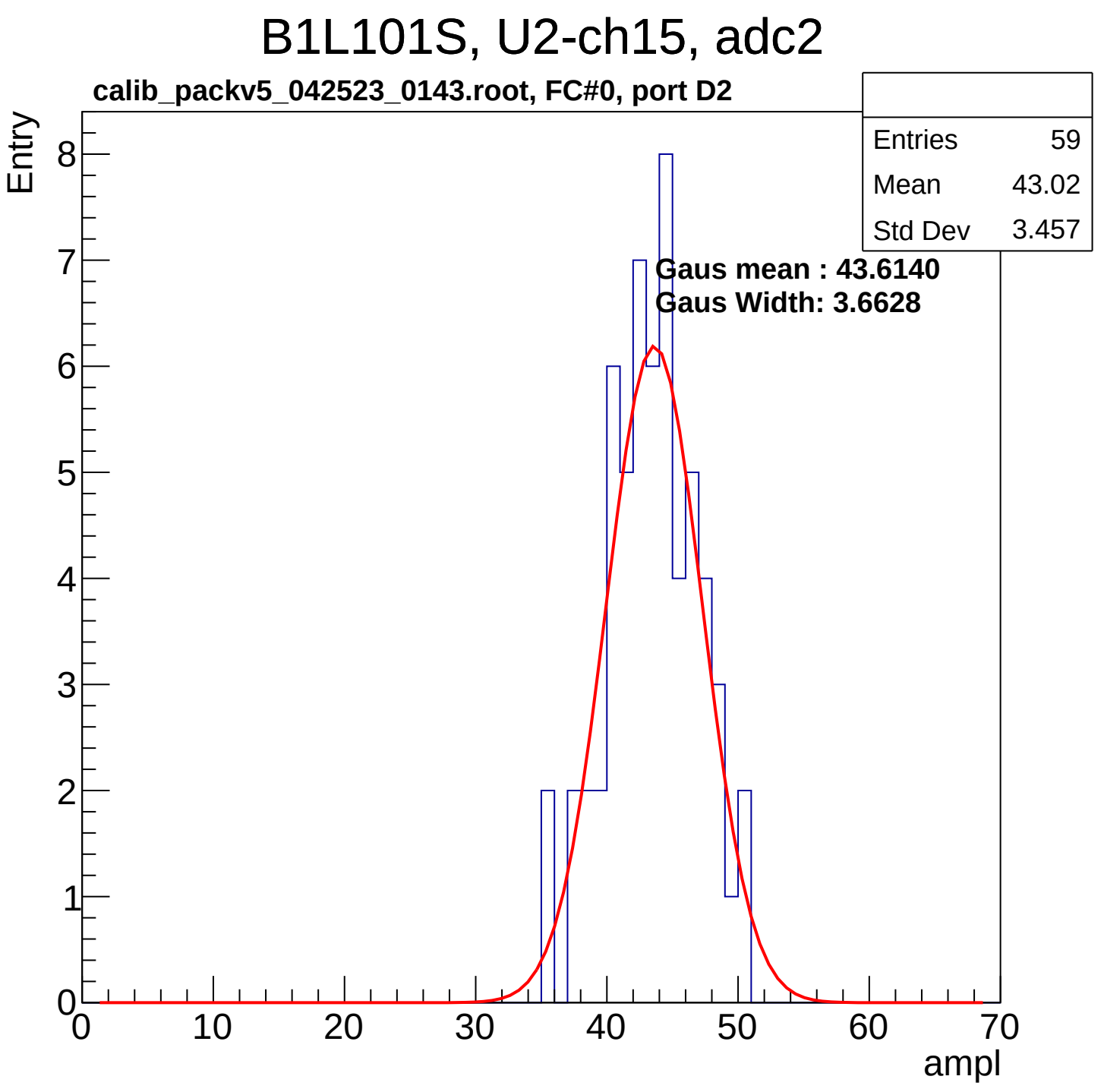

B1L101S, U2-ch14, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 59.07
Std Dev 2.84
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

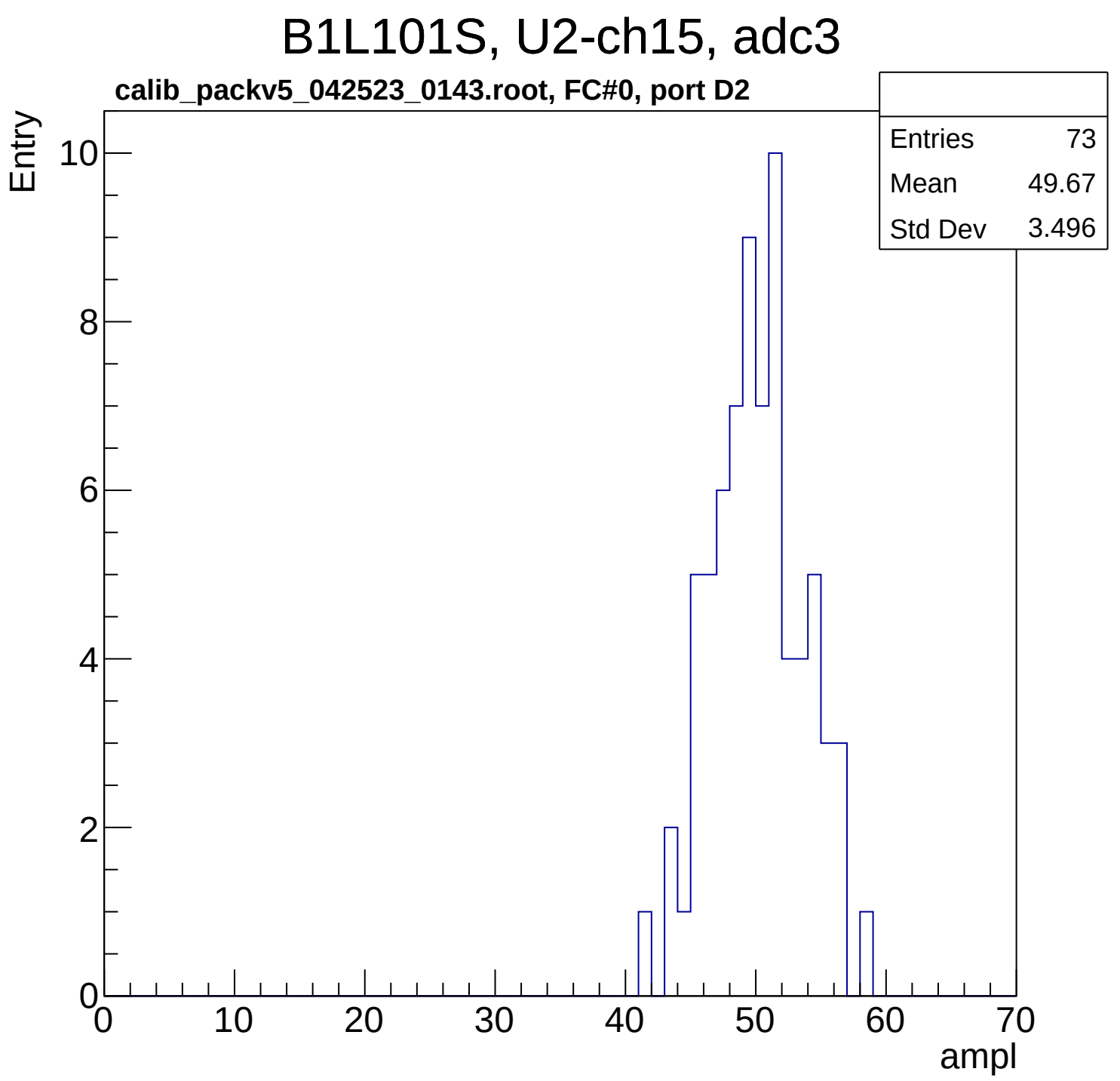

B1L101S, U2-ch14, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 55.5
Std Dev 18.56
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

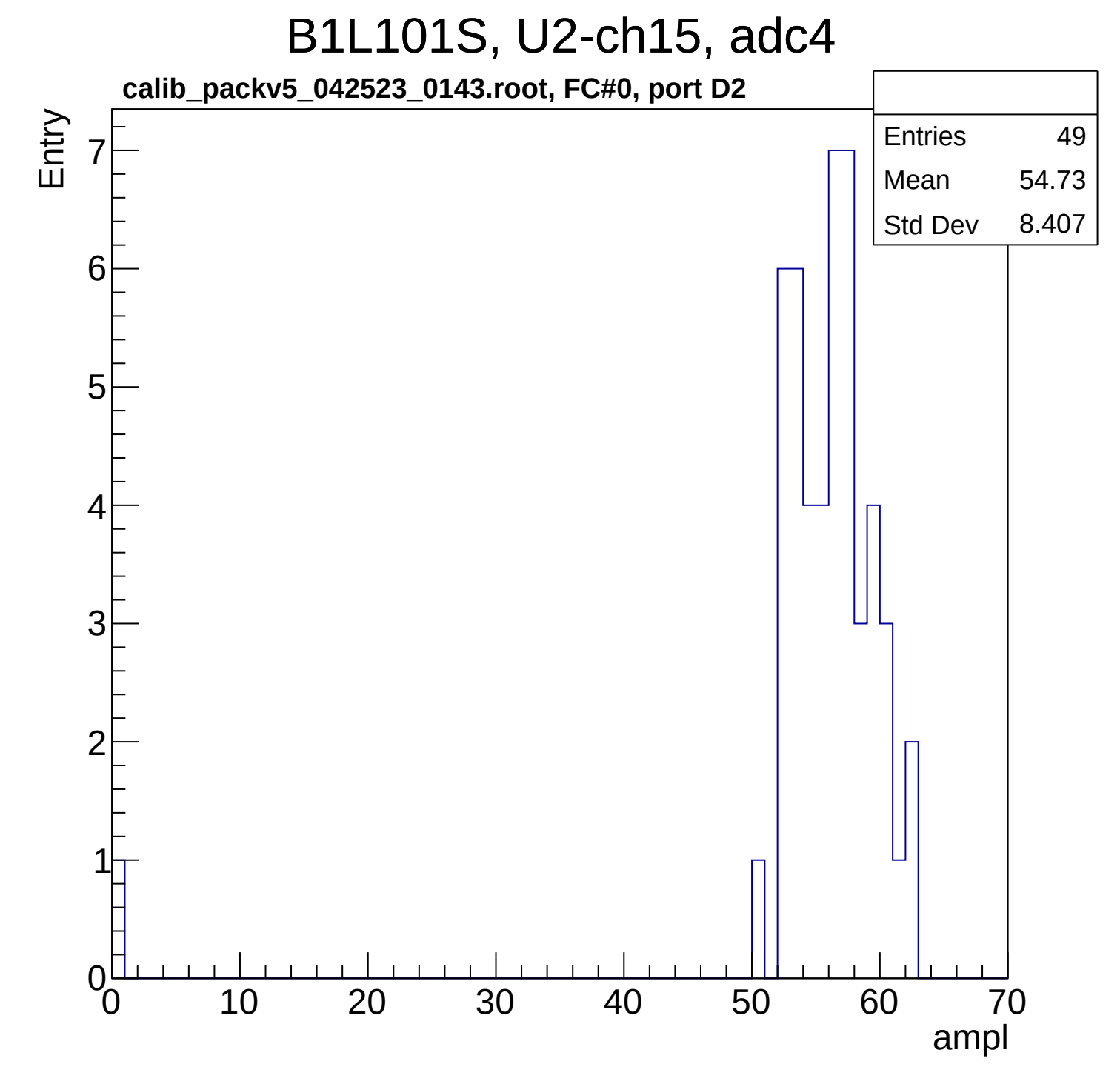

B1L101S, U2-ch14, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 26.67
Std Dev 26.61
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

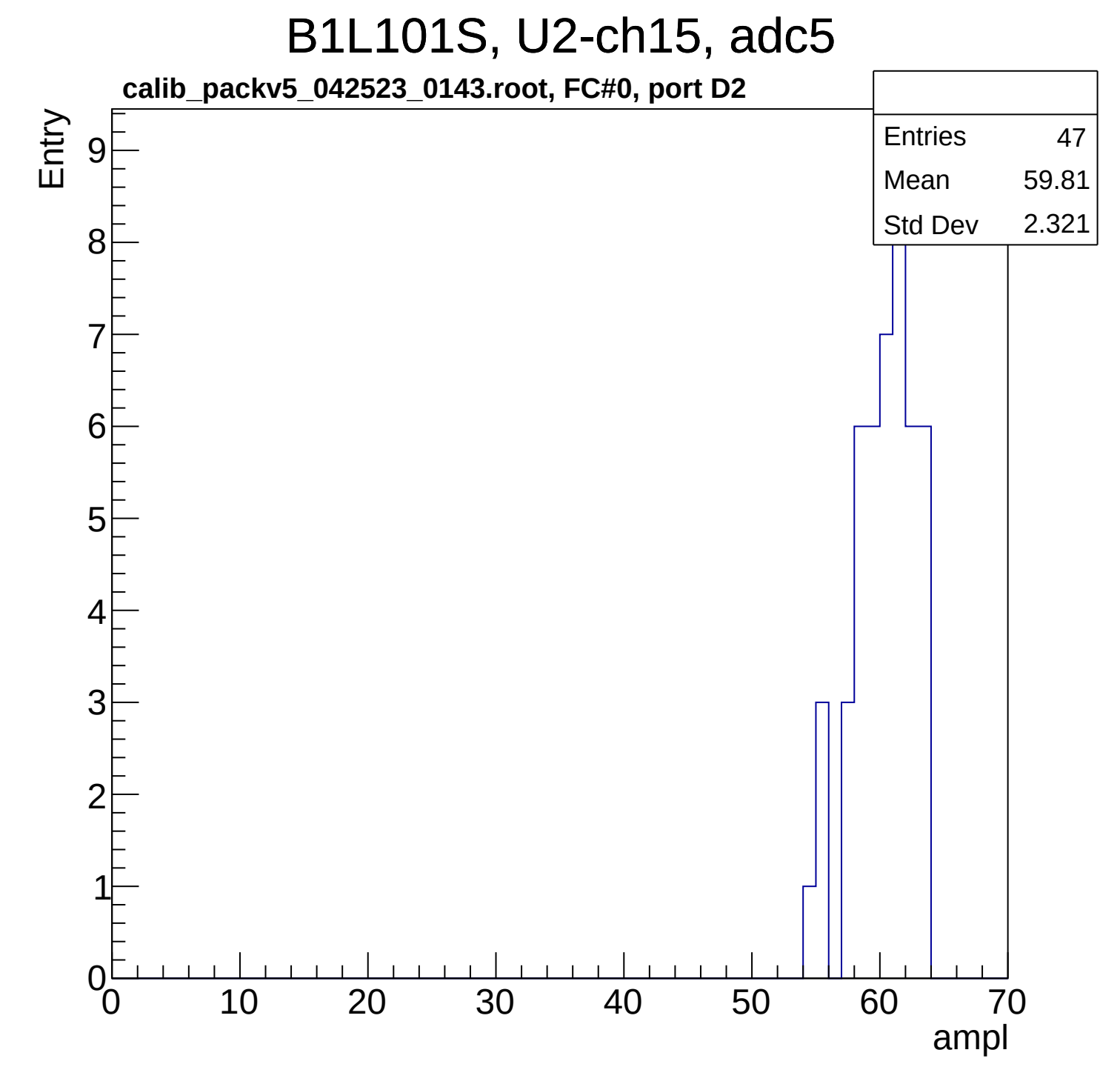

B1L101S, U2-ch15, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 29.73
Std Dev 5.053
Gaus mean : 29.9071
Gaus Width: 3.1542
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

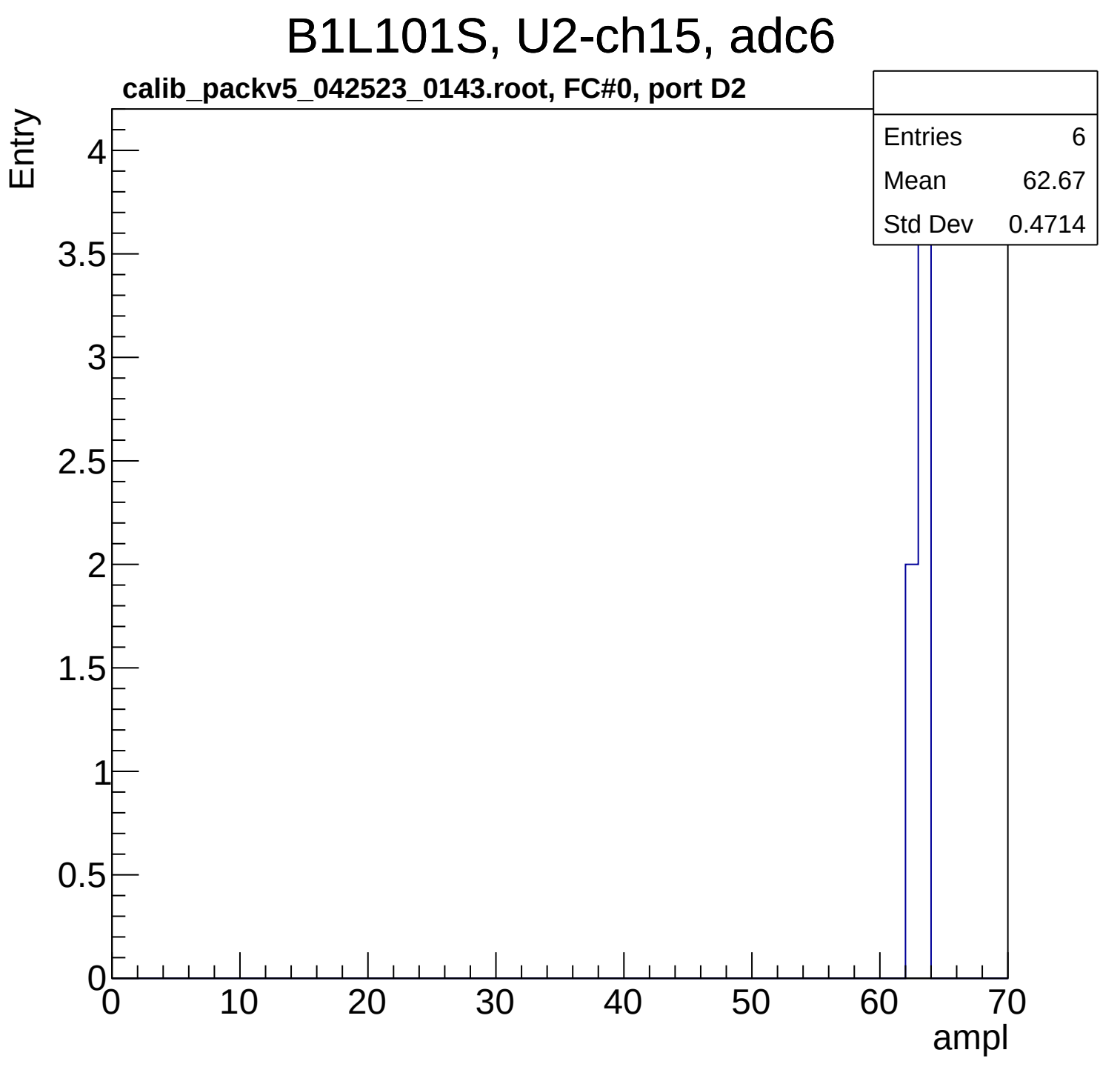

B1L101S, U2-ch15, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 36.43
Std Dev 3.68
Gaus mean : 36.7180
Gaus Width: 4.2257
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

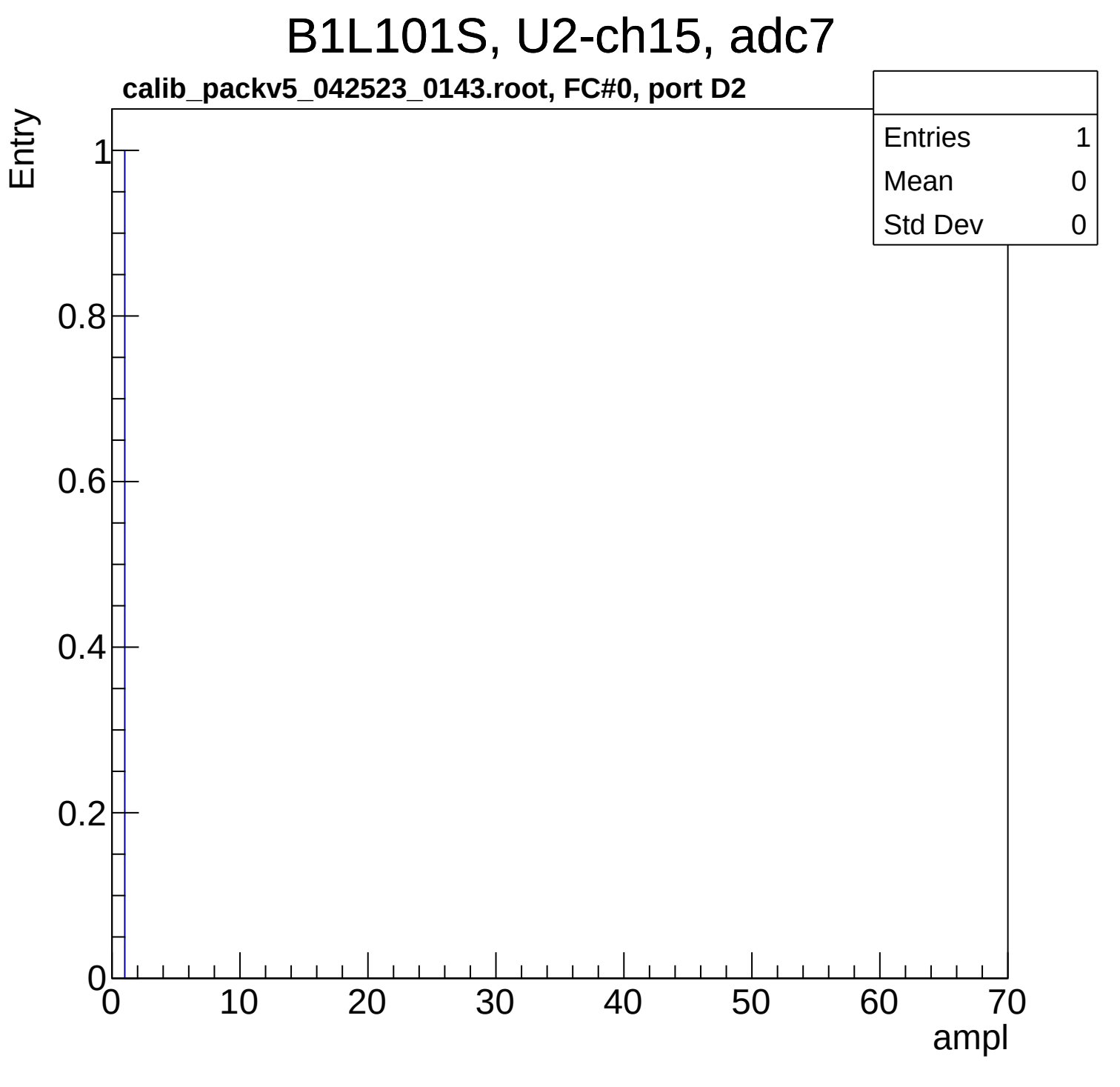

B1L101S, U2-ch15, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 43.02
Std Dev 3.457
Gaus mean : 43.6140
Gaus Width: 3.6628
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

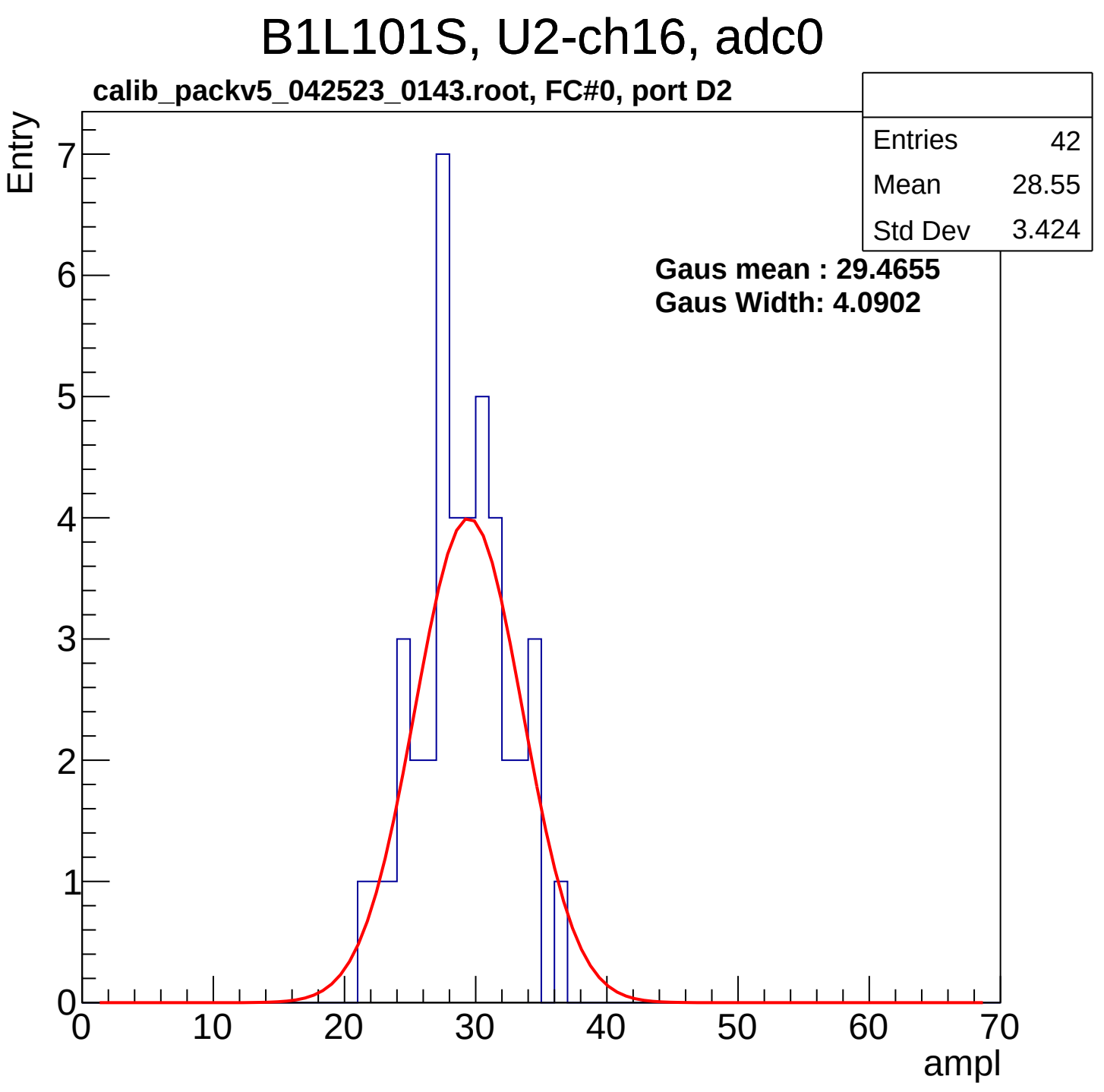

B1L101S, U2-ch15, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 49.67
Std Dev 3.496
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

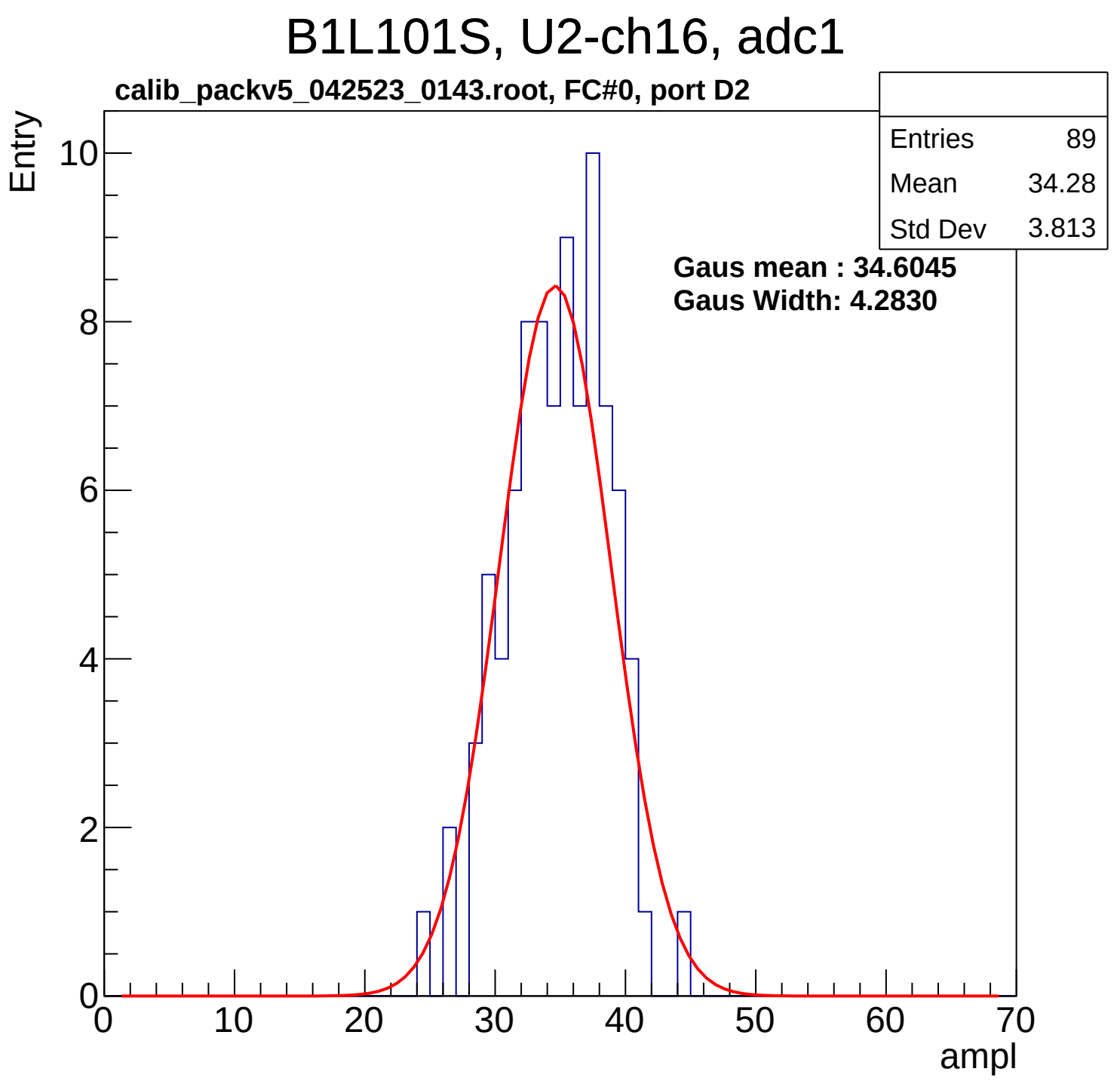

B1L101S, U2-ch15, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 54.73
Std Dev 8.407
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

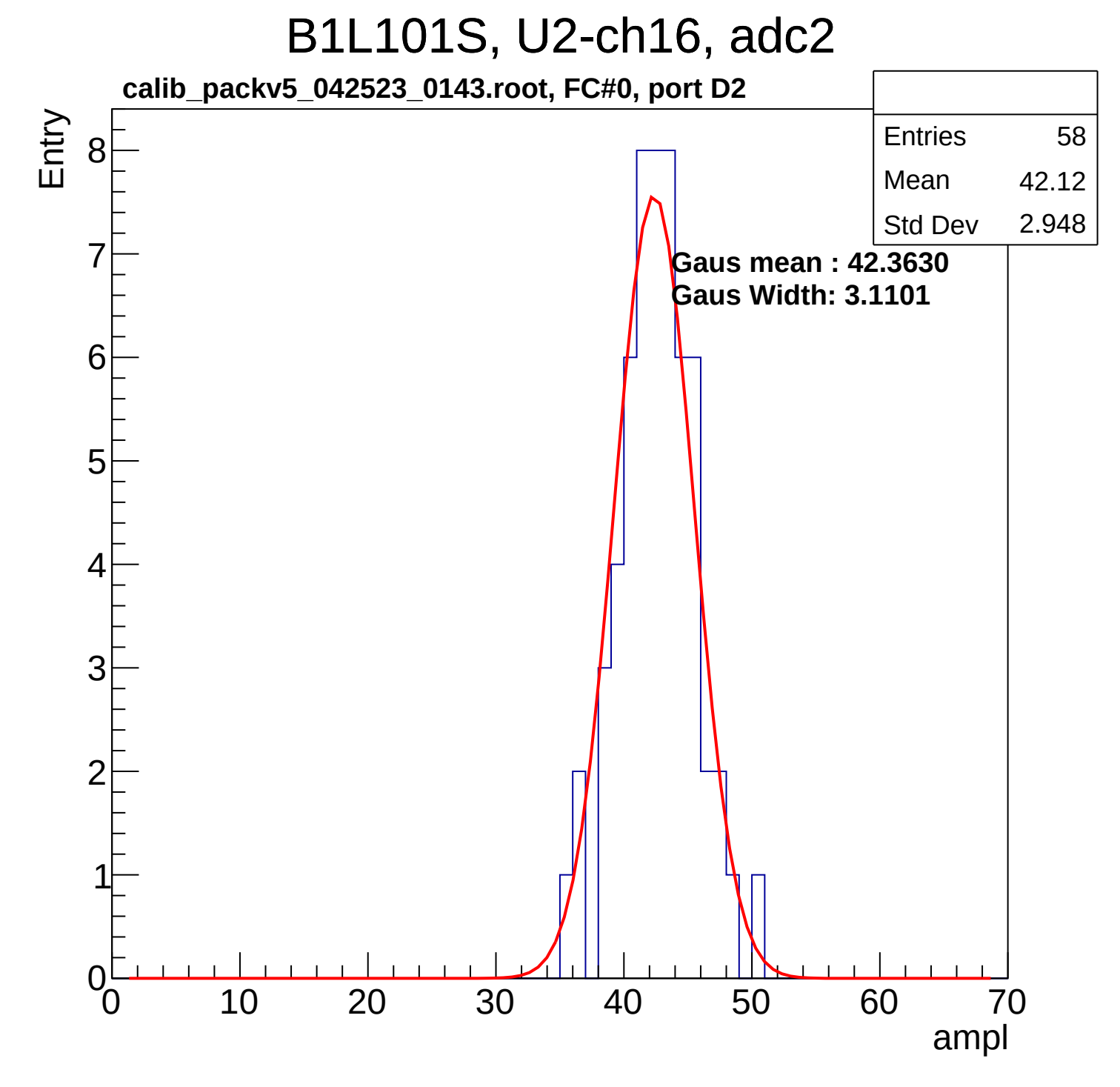

B1L101S, U2-ch15, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 59.81
Std Dev 2.321
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

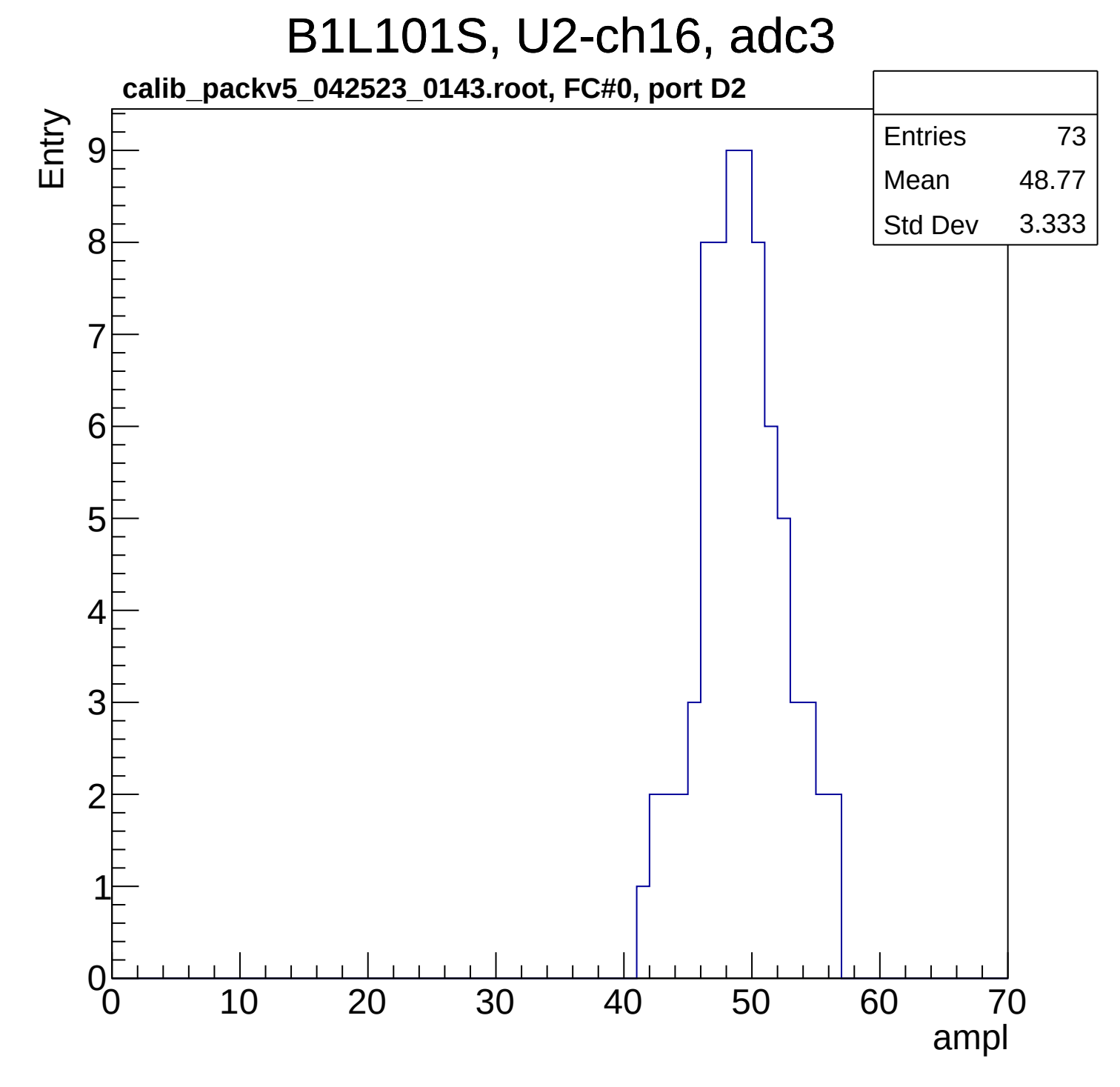

B1L101S, U2-ch15, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

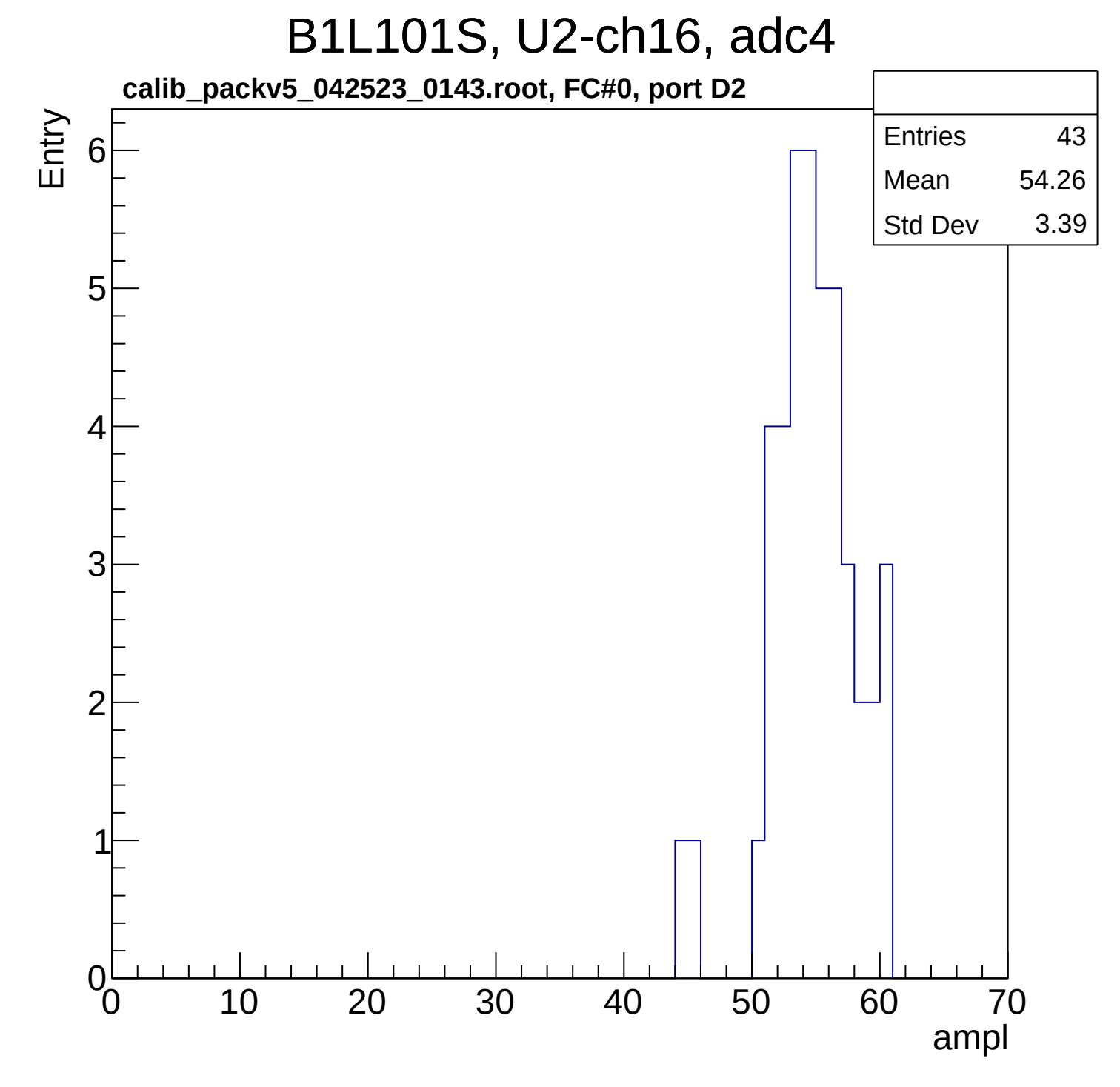

B1L101S, U2-ch15, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

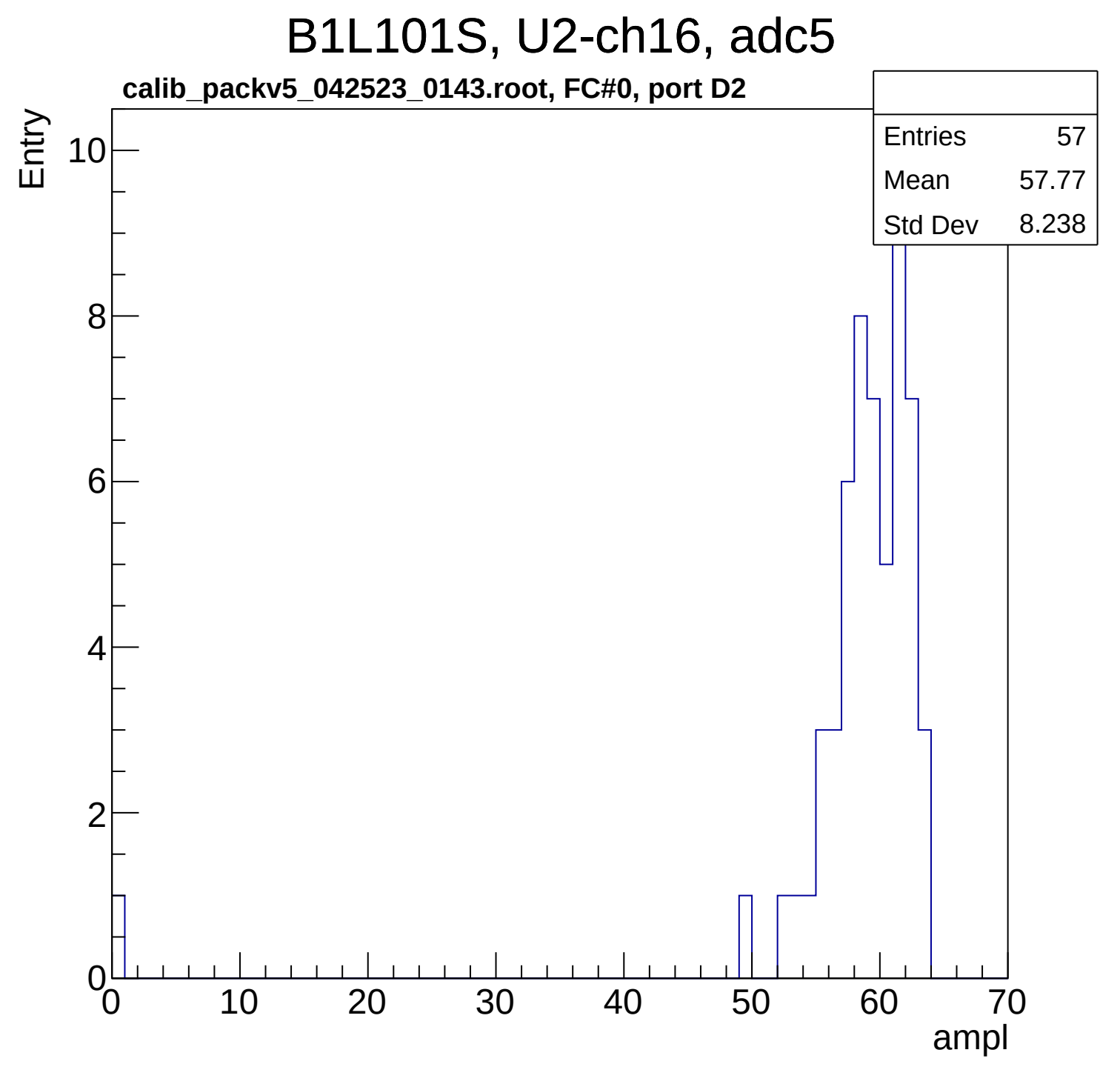

B1L101S, U2-ch16, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 28.55
Std Dev 3.424
Gaus mean : 29.4655
Gaus Width: 4.0902
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

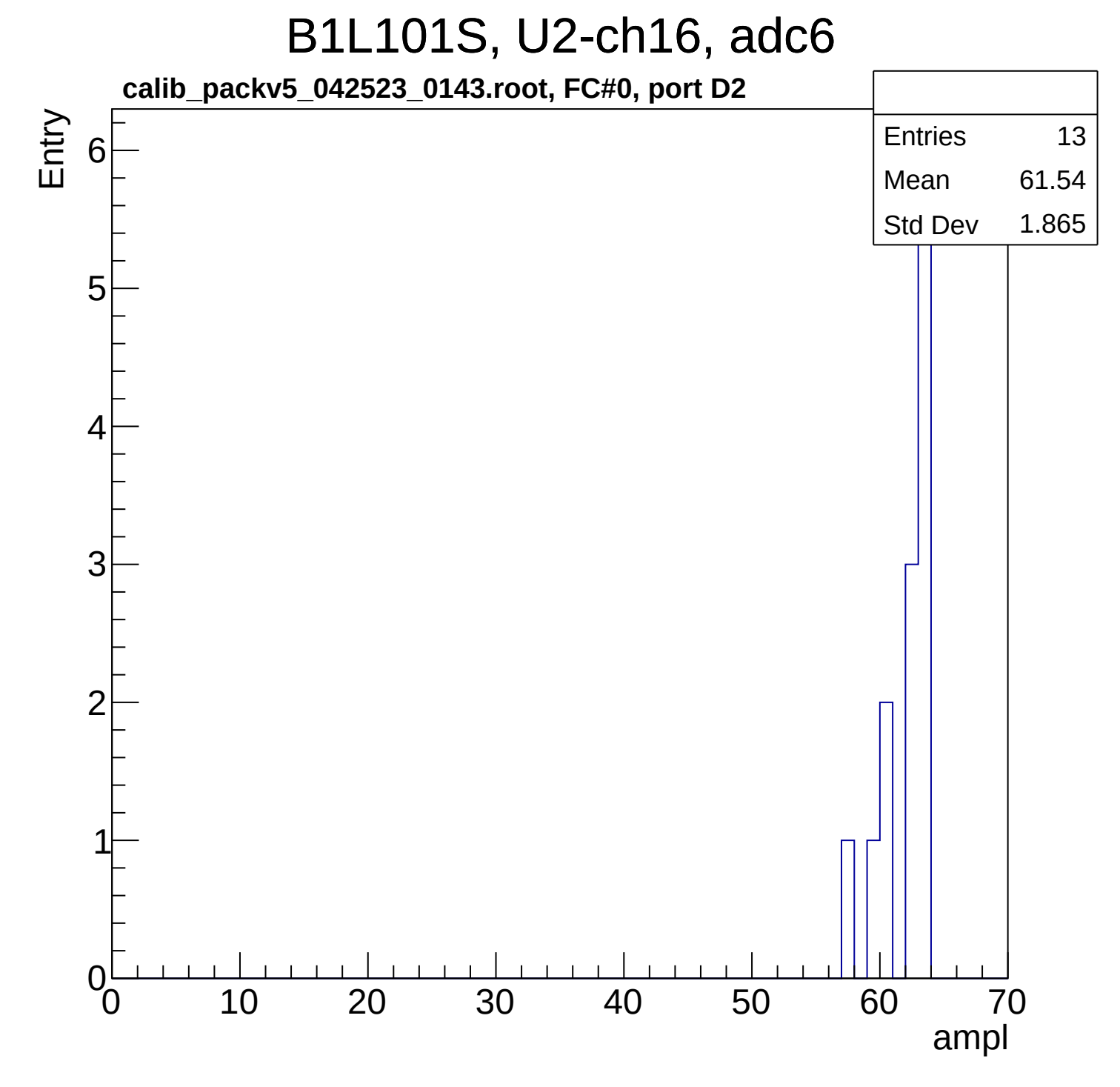

B1L101S, U2-ch16, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 89
Mean 34.28
Std Dev 3.813
Gaus mean : 34.6045
Gaus Width: 4.2830
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

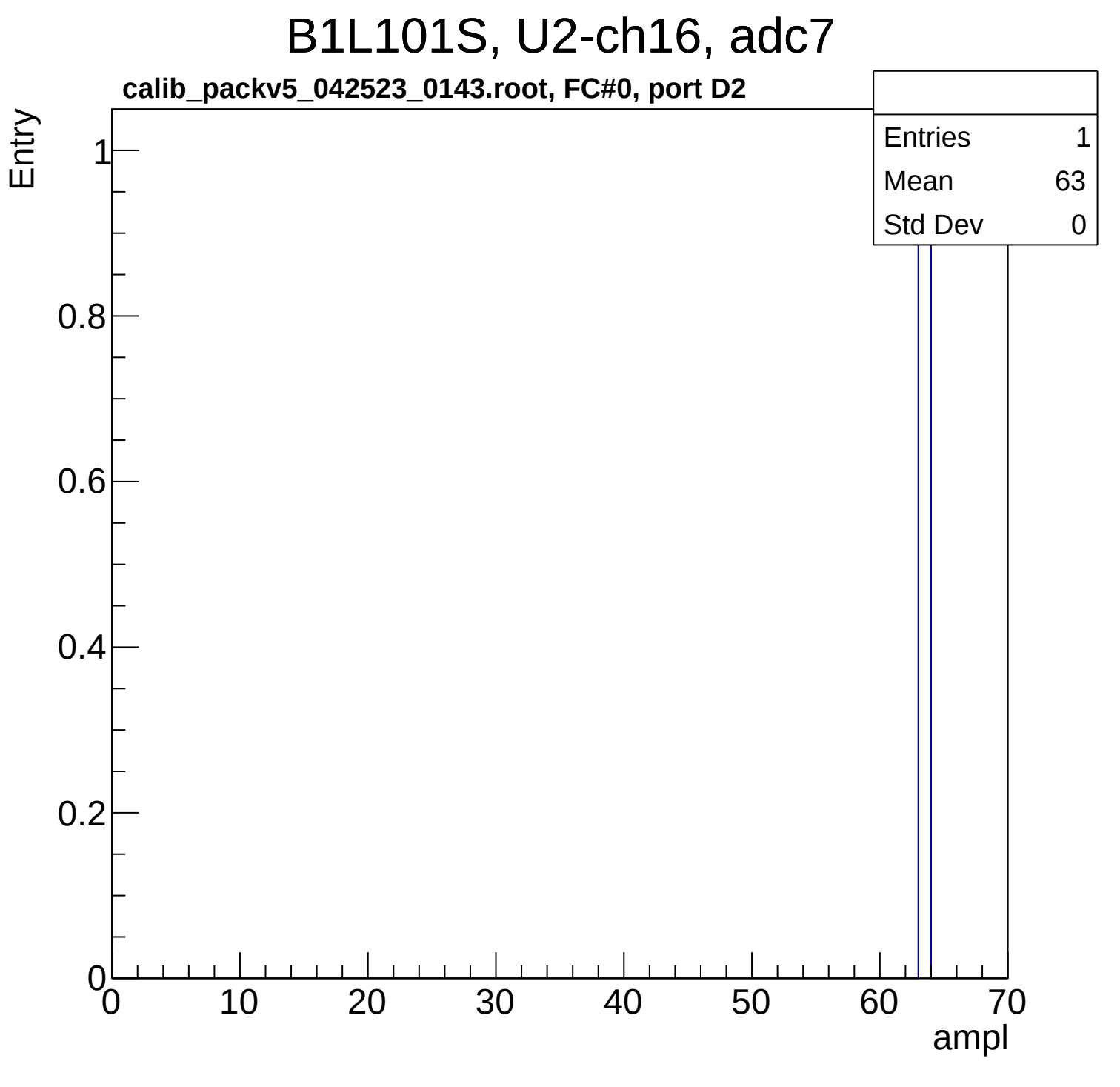

B1L101S, U2-ch16, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 42.12
Std Dev 2.948
Gaus mean : 42.3630
Gaus Width: 3.1101
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

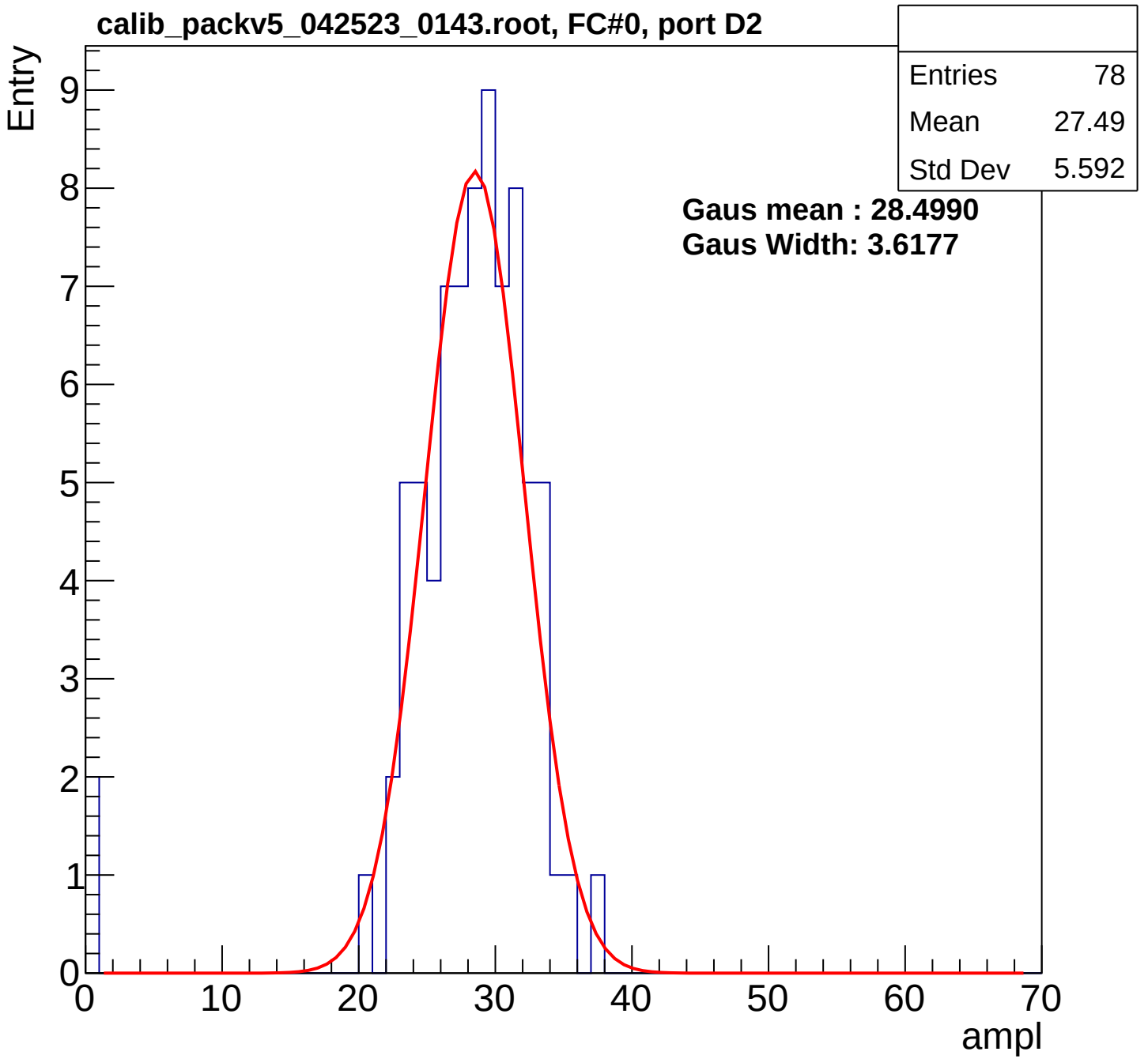

B1L101S, U2-ch16, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 48.77
Std Dev 3.333
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

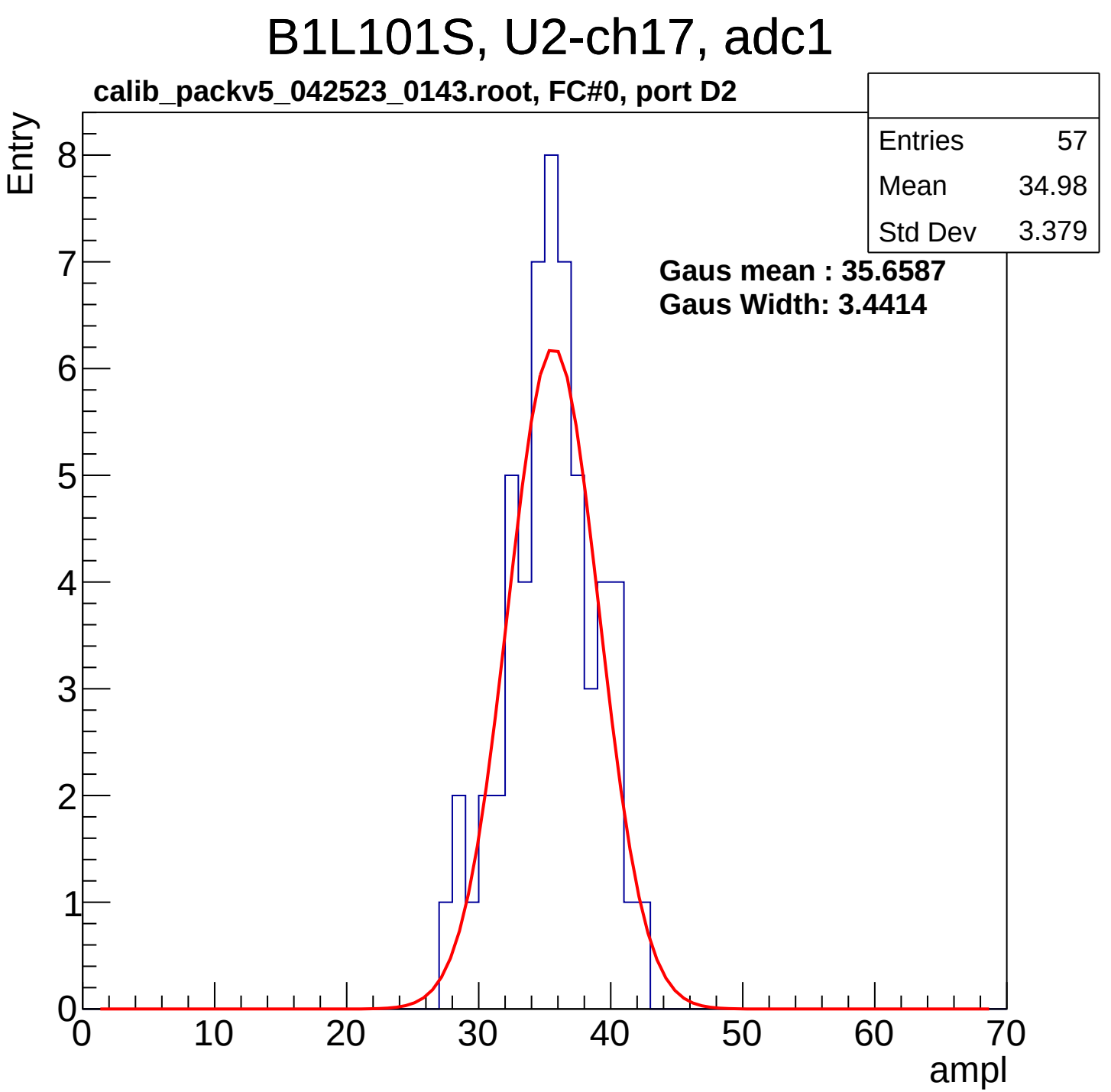

B1L101S, U2-ch16, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 43
Mean 54.26
Std Dev 3.39
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

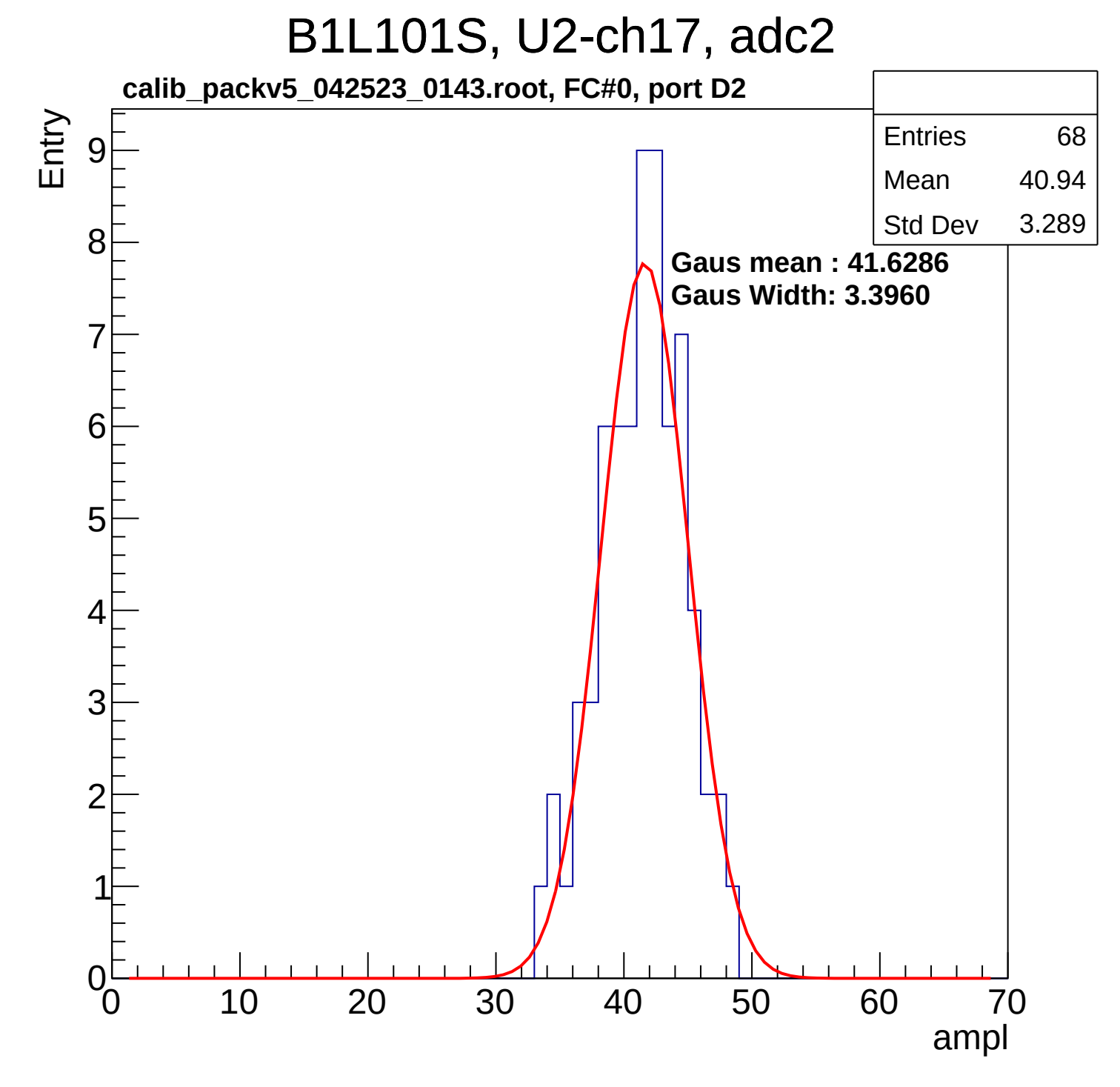

B1L101S, U2-ch16, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 57.77
Std Dev 8.238
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

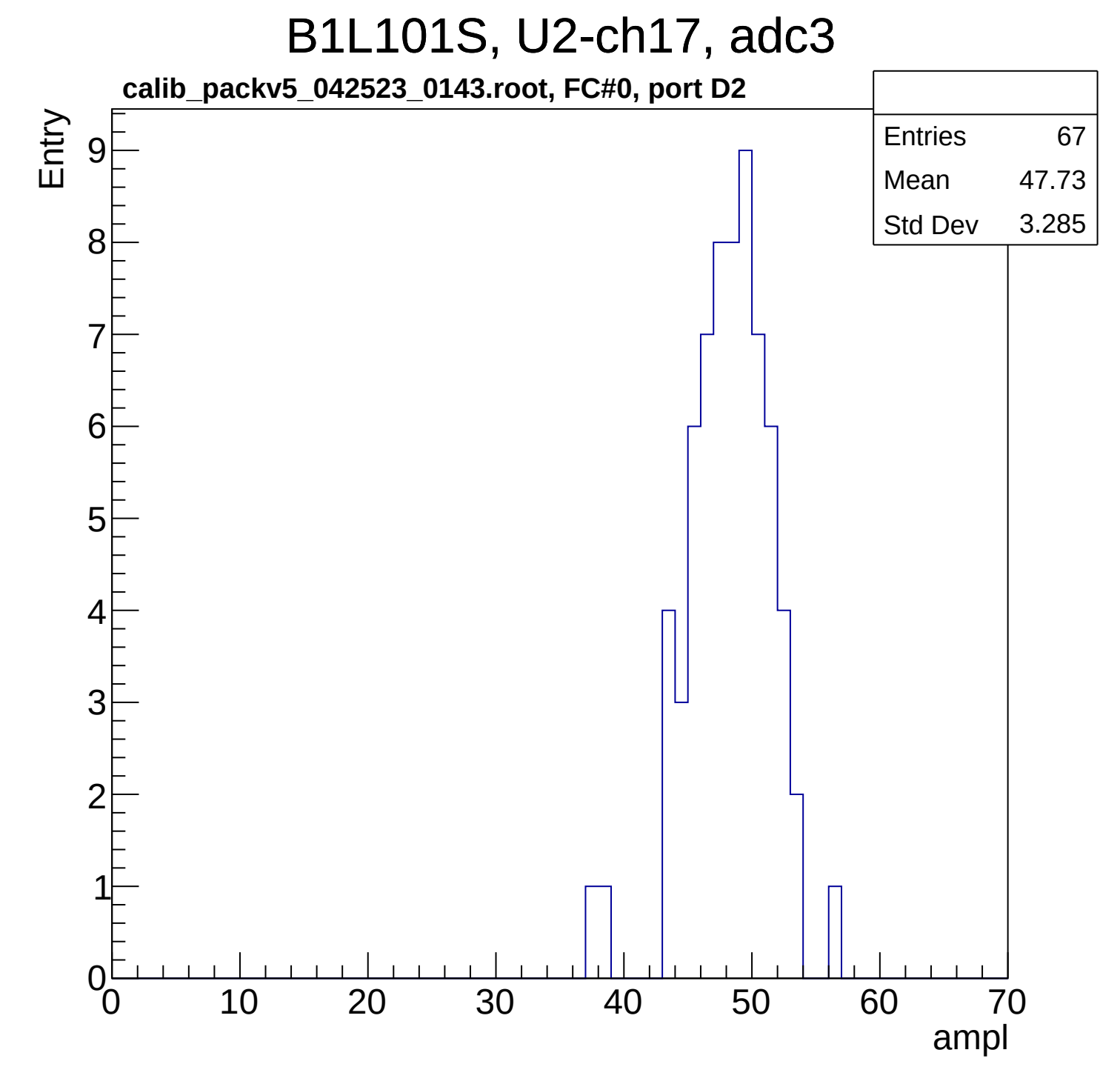

B1L101S, U2-ch16, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 13
Mean 61.54
Std Dev 1.865
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

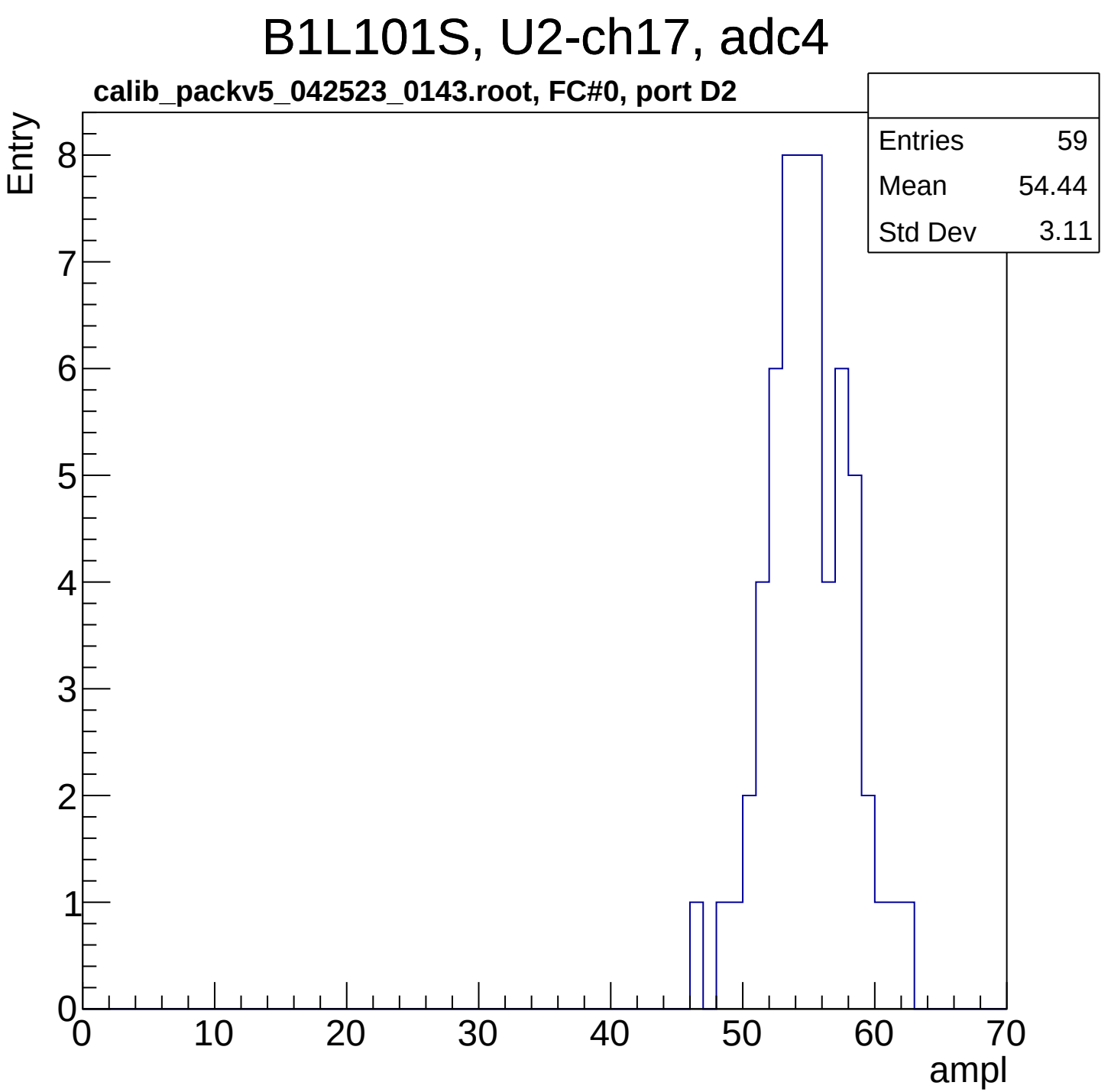

B1L101S, U2-ch16, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

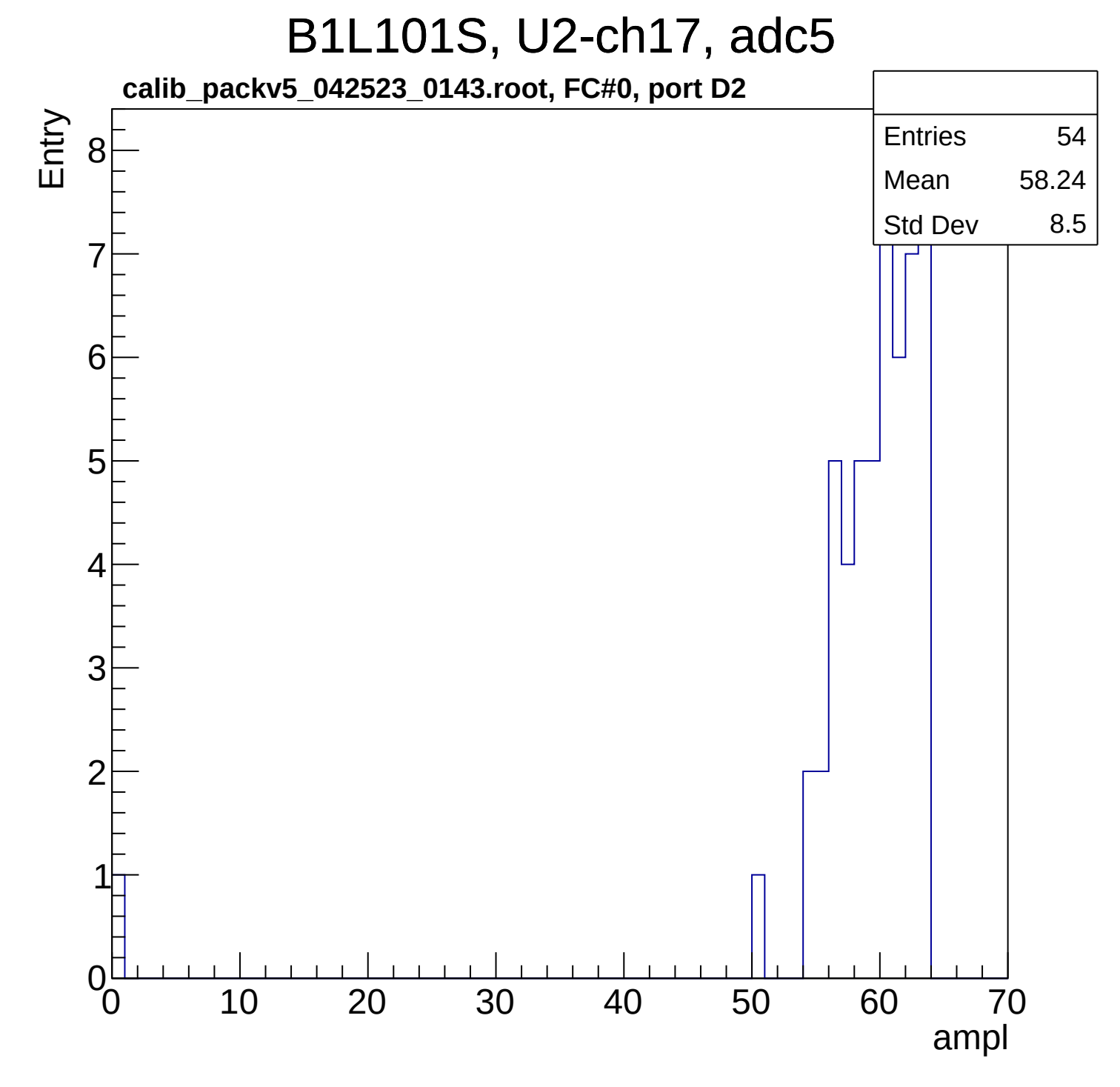

B1L101S, U2-ch17, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 27.49
Std Dev 5.592
Gaus mean : 28.4990
Gaus Width: 3.6177
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

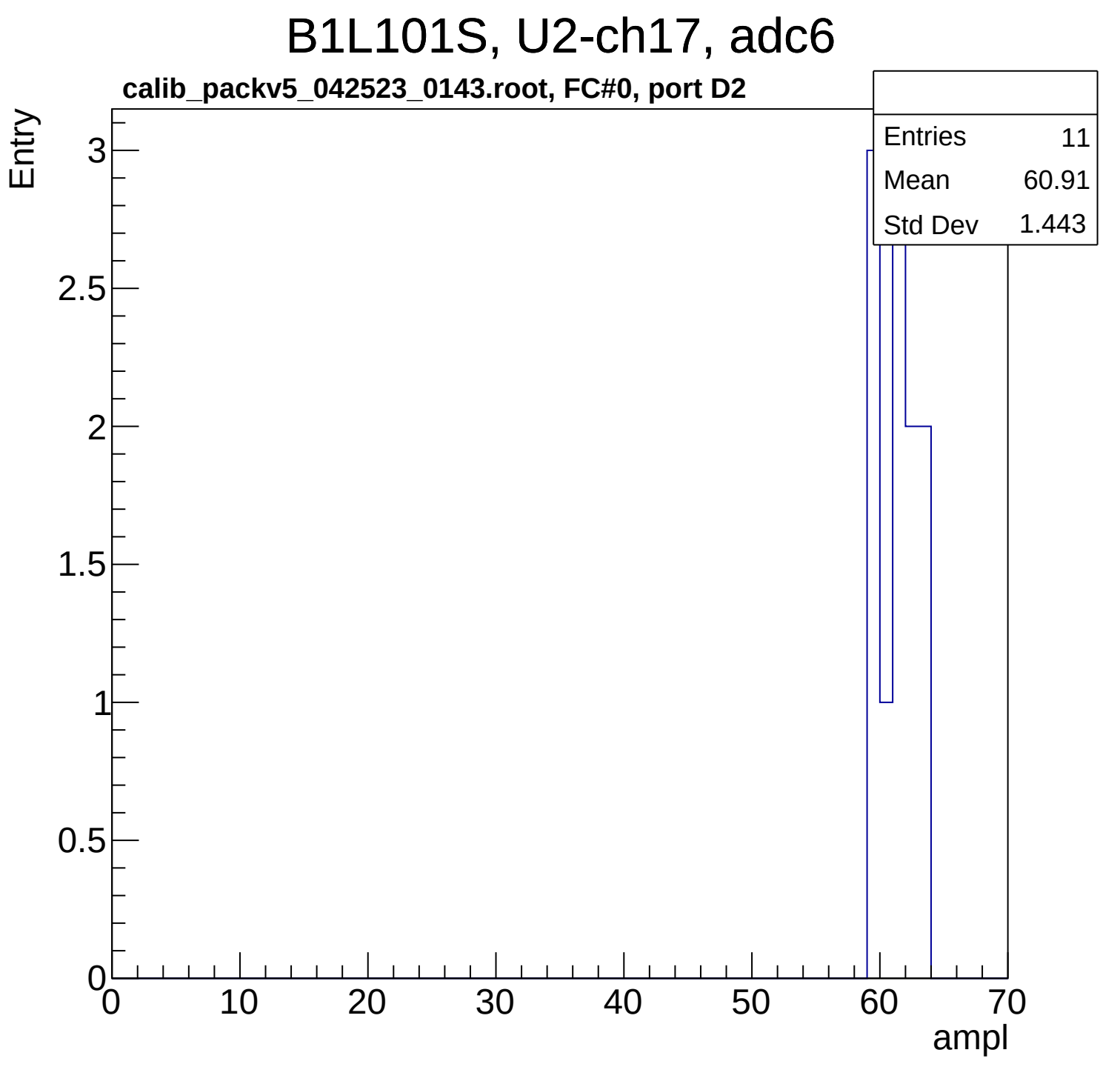

B1L101S, U2-ch17, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 34.98
Std Dev 3.379
Gaus mean : 35.6587
Gaus Width: 3.4414
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

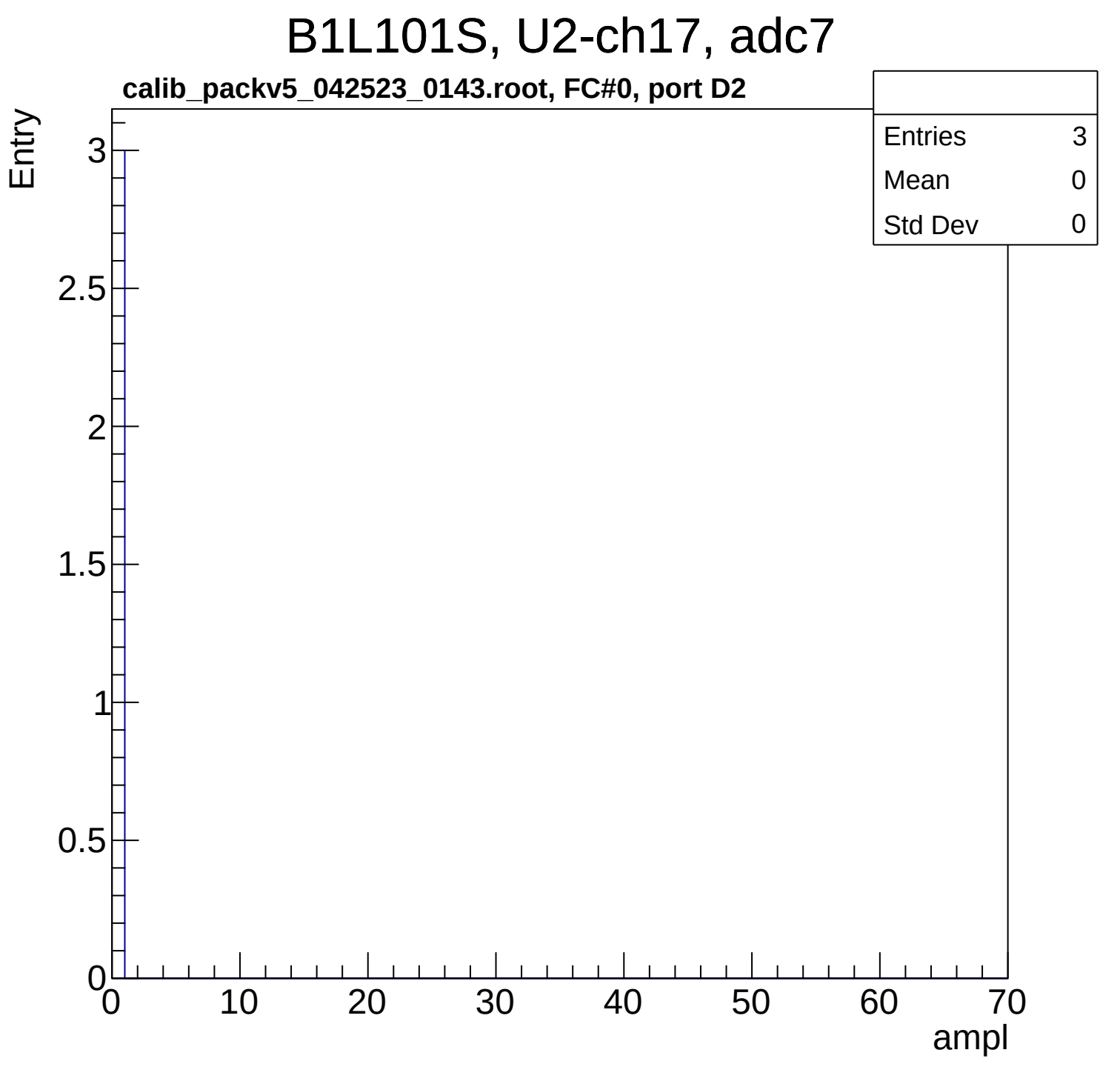

B1L101S, U2-ch17, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 40.94
Std Dev 3.289
Gaus mean : 41.6286
Gaus Width: 3.3960
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

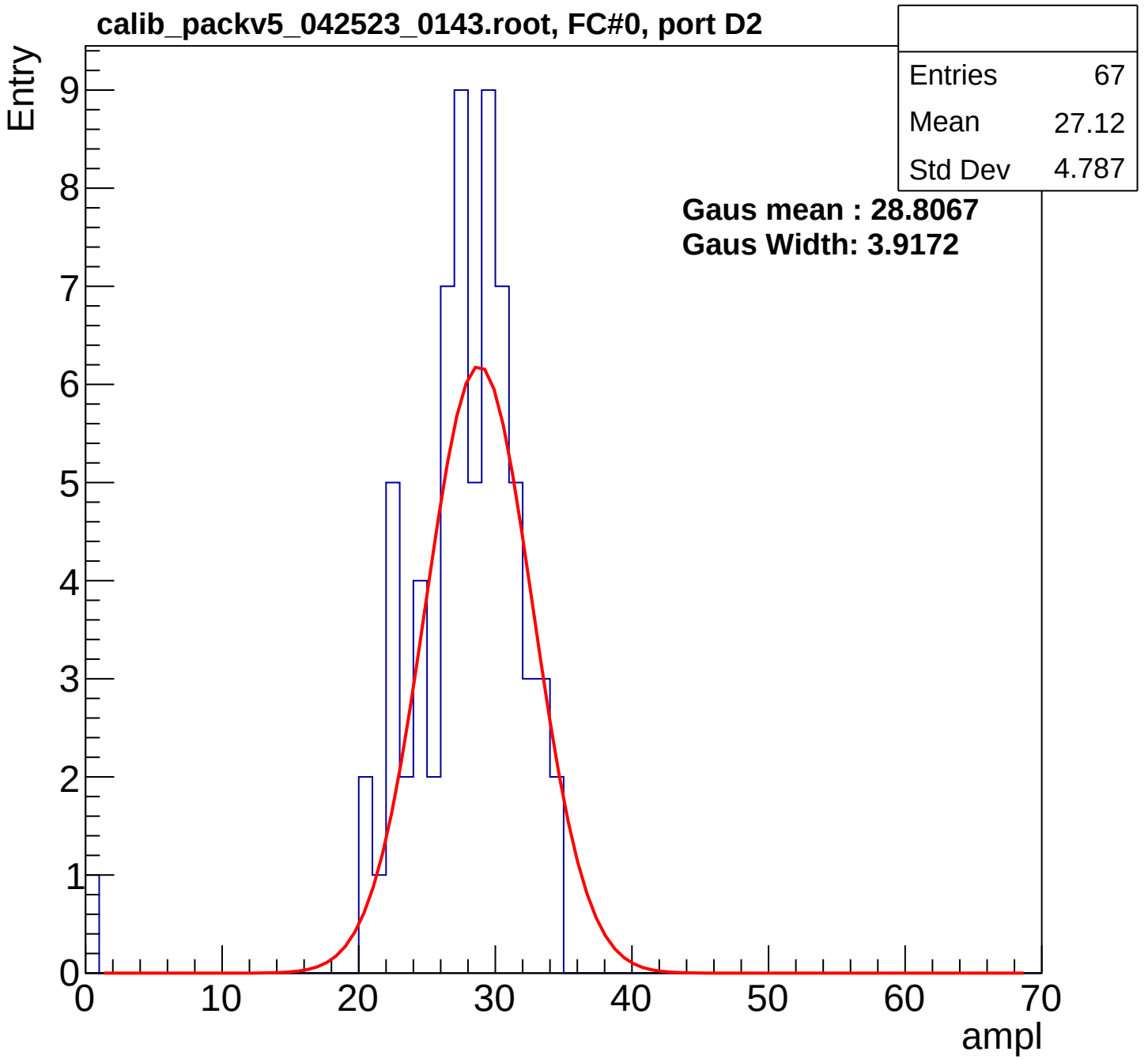

B1L101S, U2-ch17, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 47.73
Std Dev 3.285
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

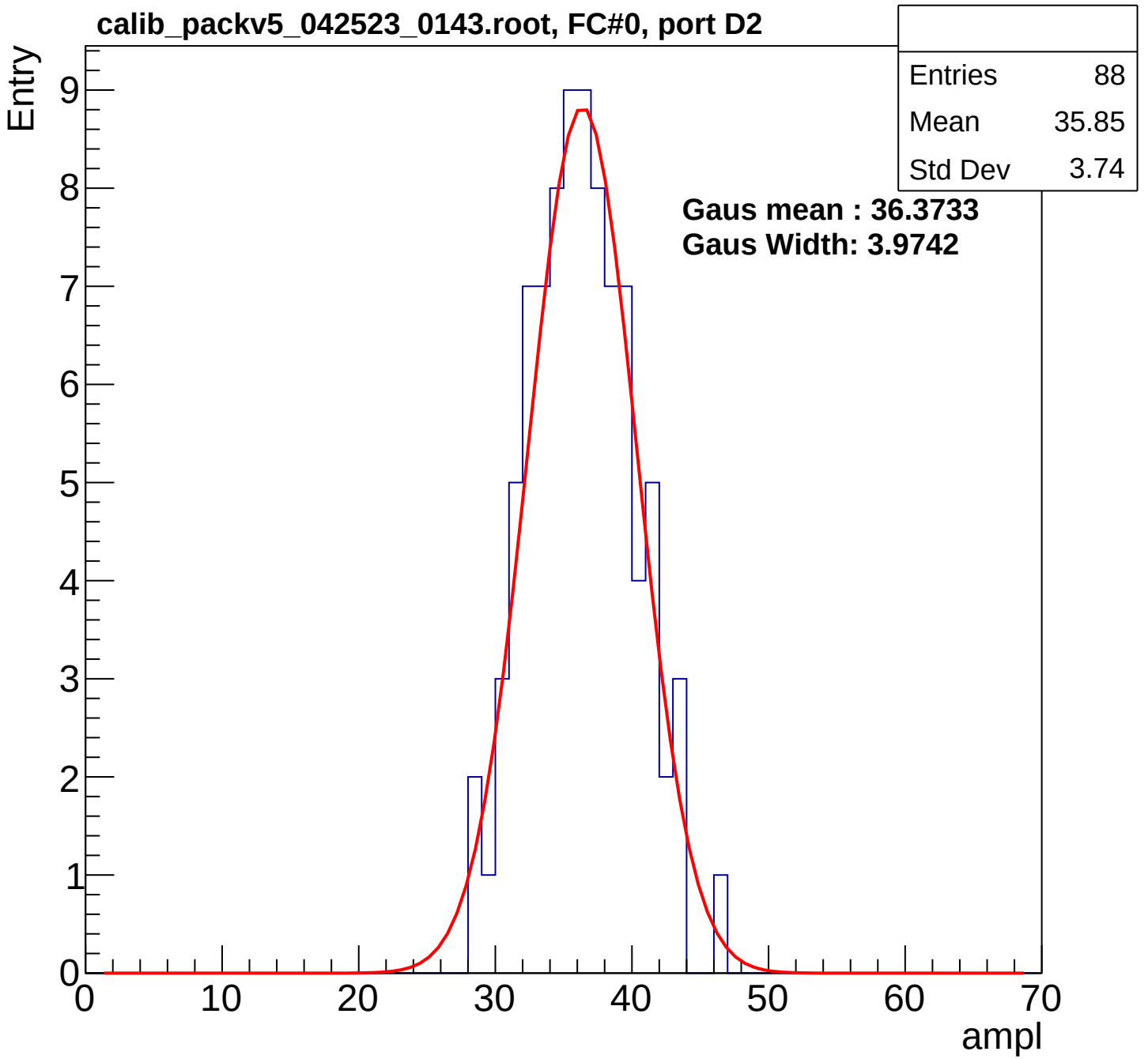

B1L101S, U2-ch17, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 54.44
Std Dev 3.11
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

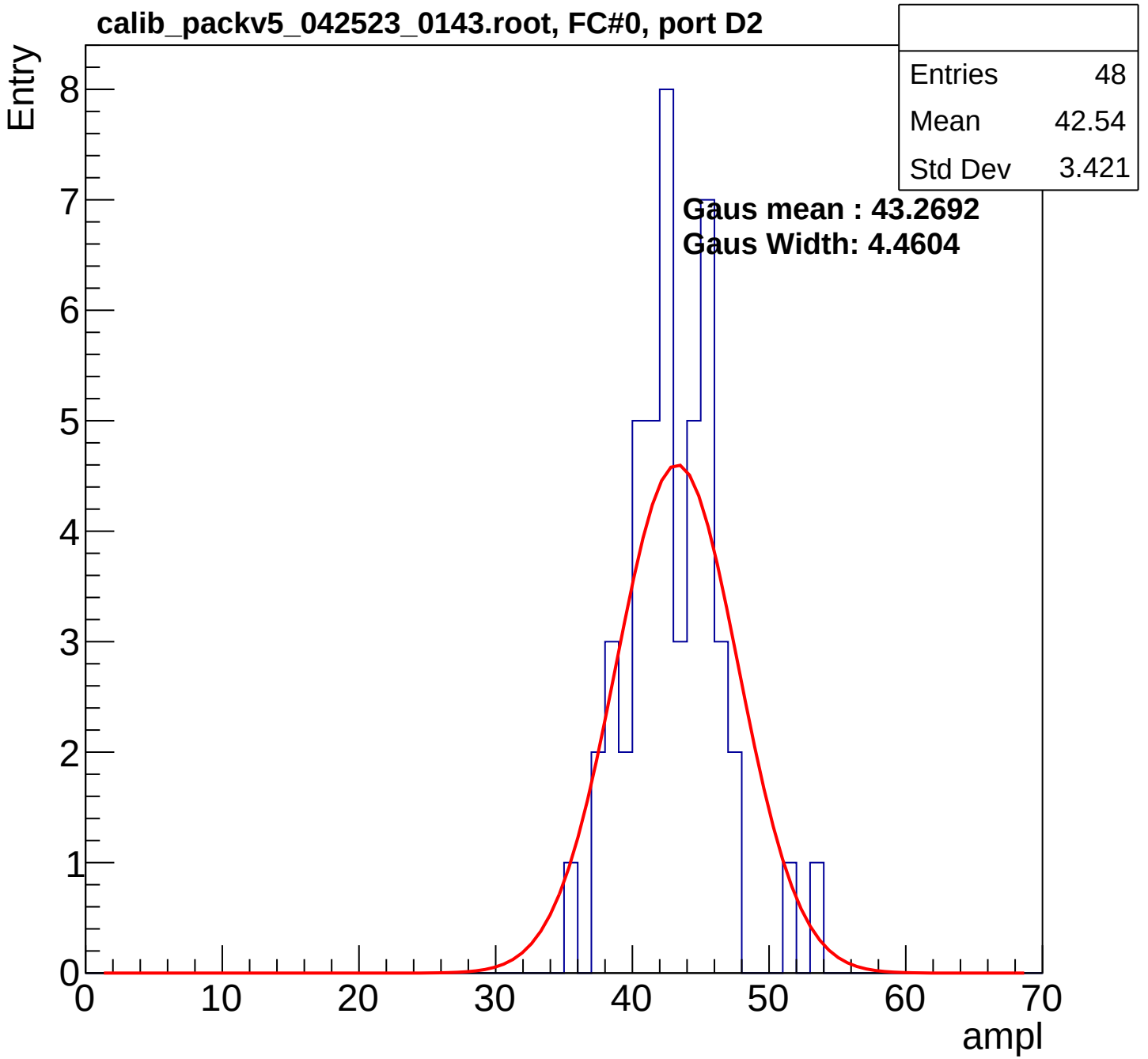

B1L101S, U2-ch17, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 58.24
Std Dev 8.5
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

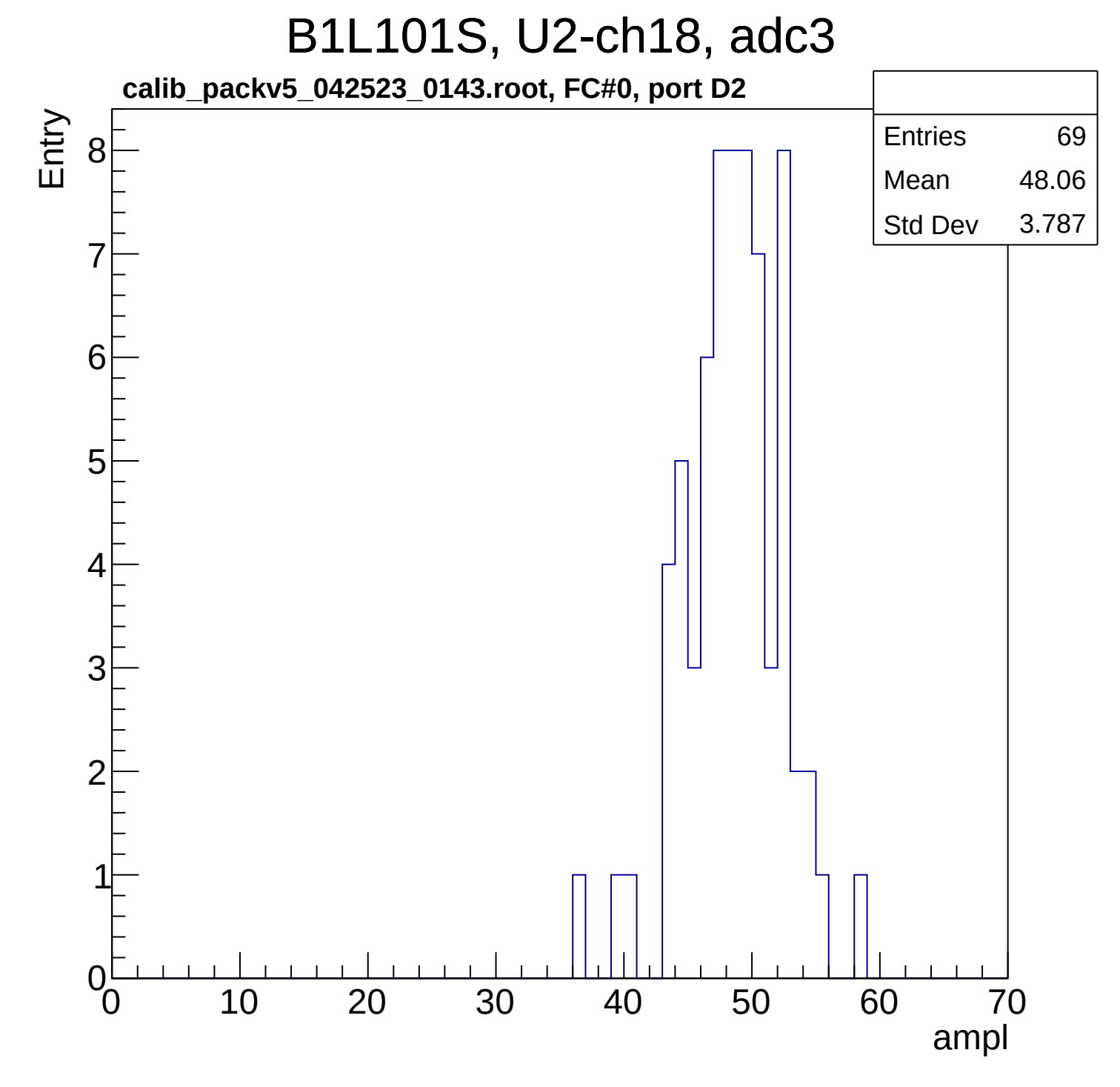

B1L101S, U2-ch17, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 11
Mean 60.91
Std Dev 1.443
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

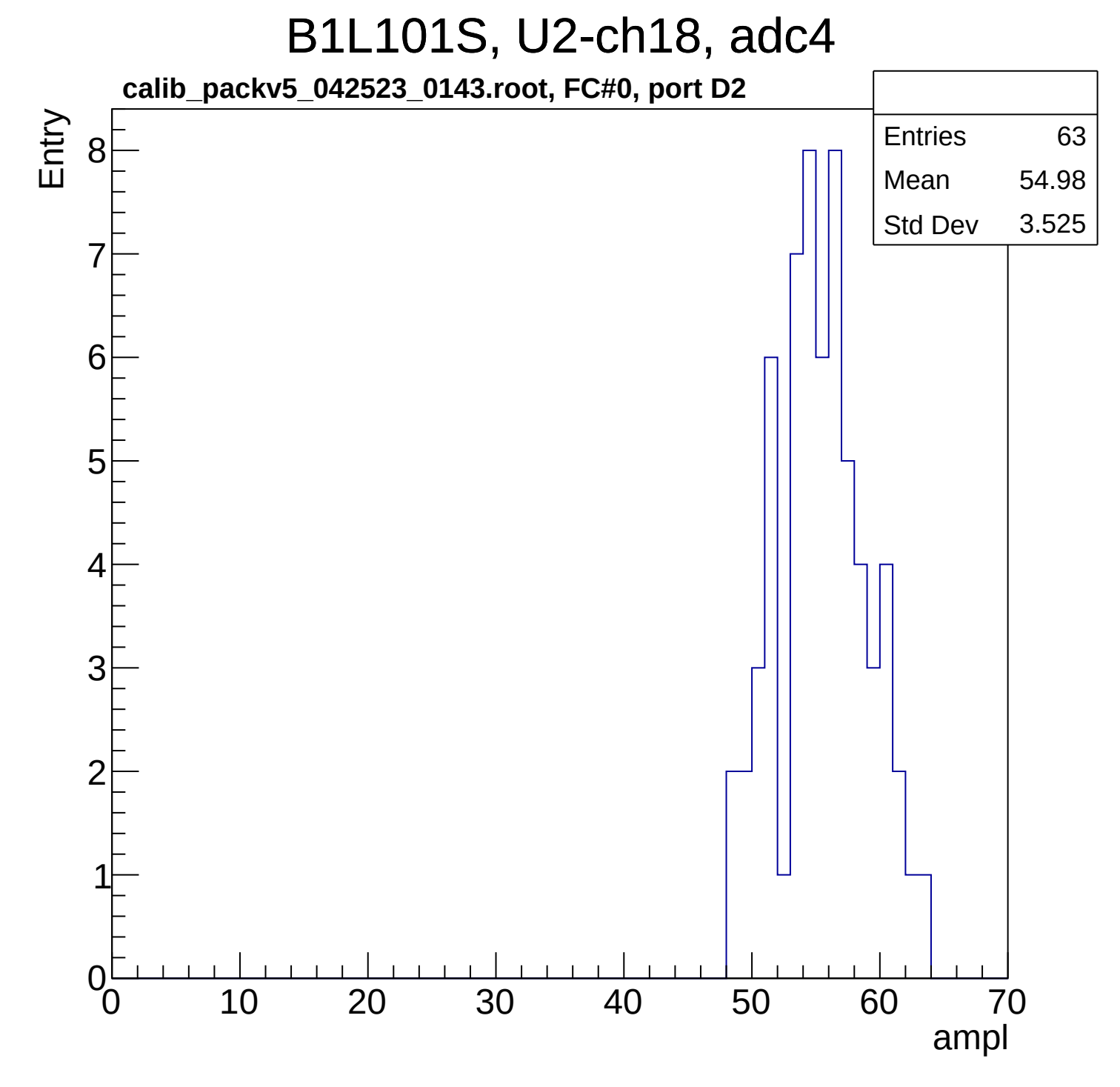

B1L101S, U2-ch17, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 0
Std Dev 0
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl

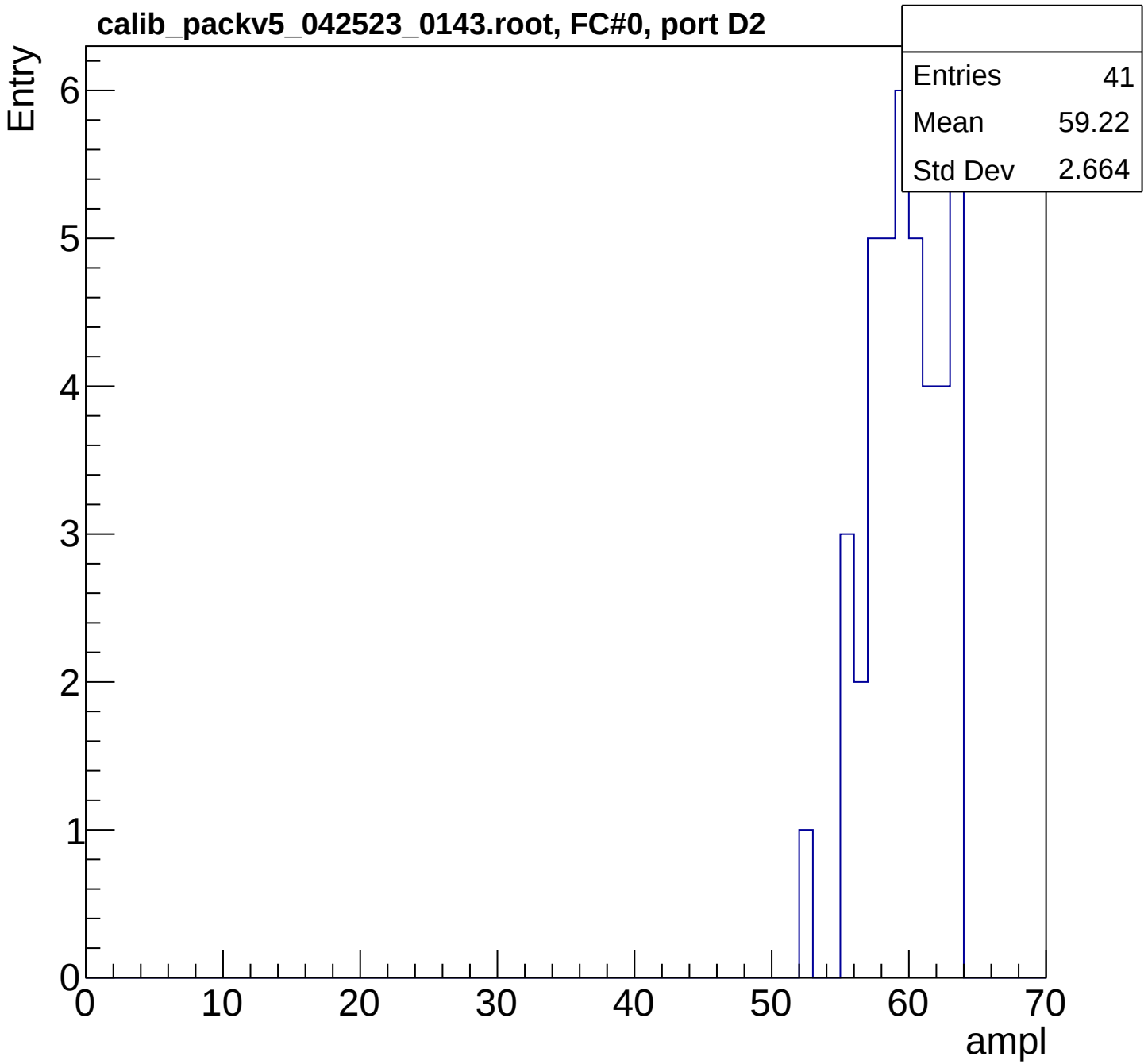

B1L101S, U2-ch18, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 27.12
Std Dev 4.787
Gaus mean : 28.8067
Gaus Width: 3.9172
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

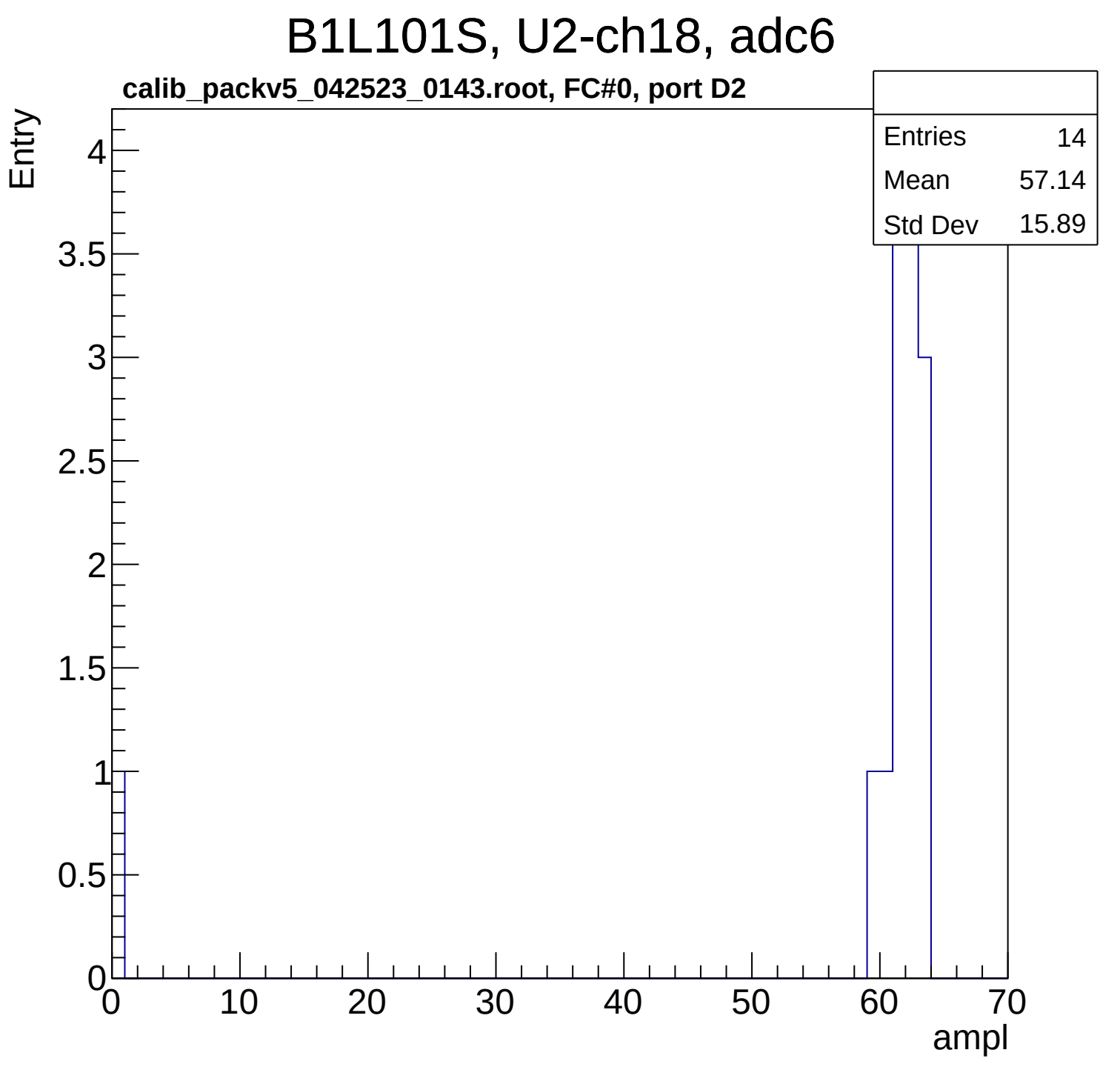

B1L101S, U2-ch18, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 88
Mean 35.85
Std Dev 3.74
Gaus mean : 36.3733
Gaus Width: 3.9742
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

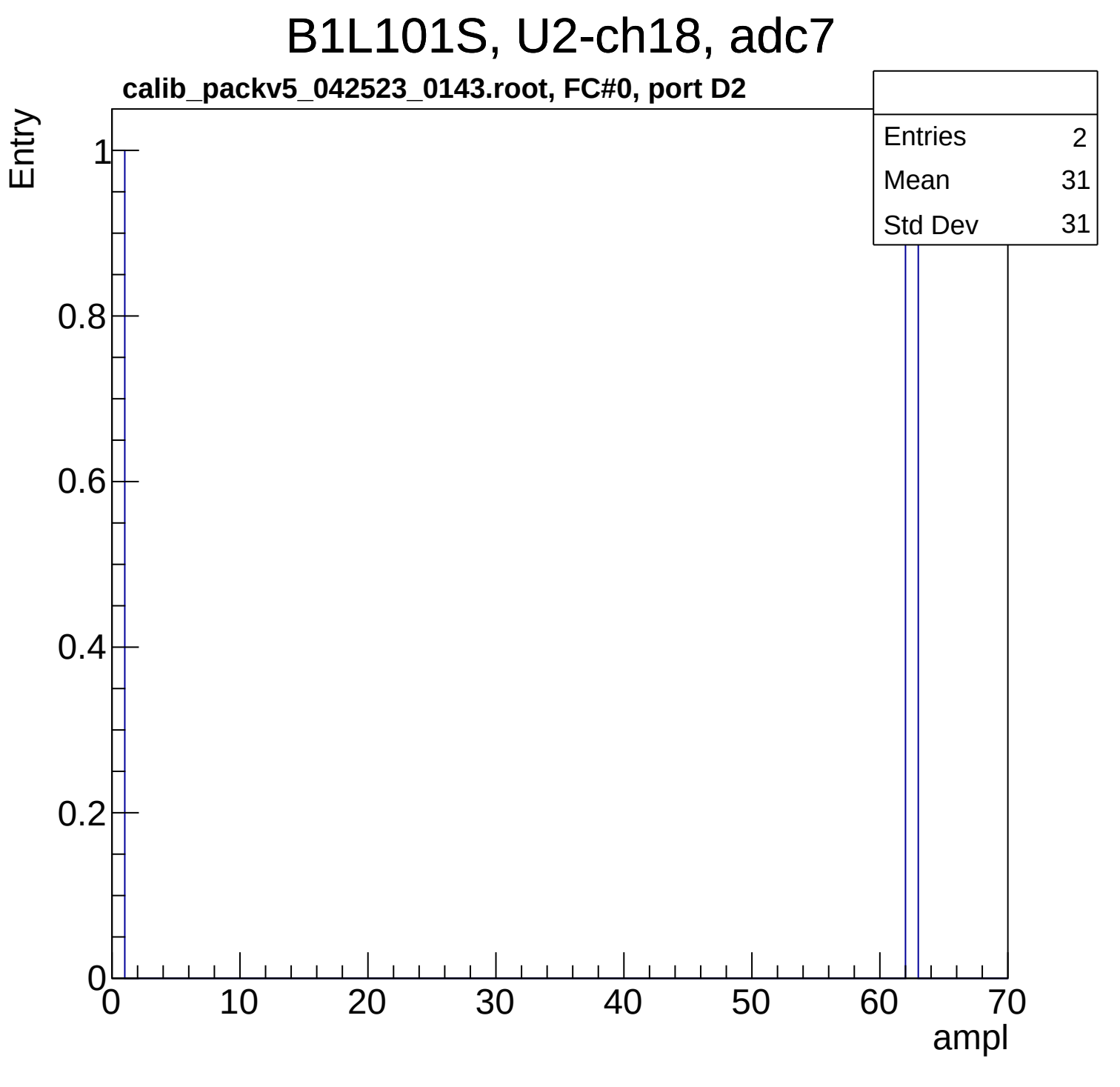

B1L101S, U2-ch18, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 42.54
Std Dev 3.421
Gaus mean : 43.2692
Gaus Width: 4.4604
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

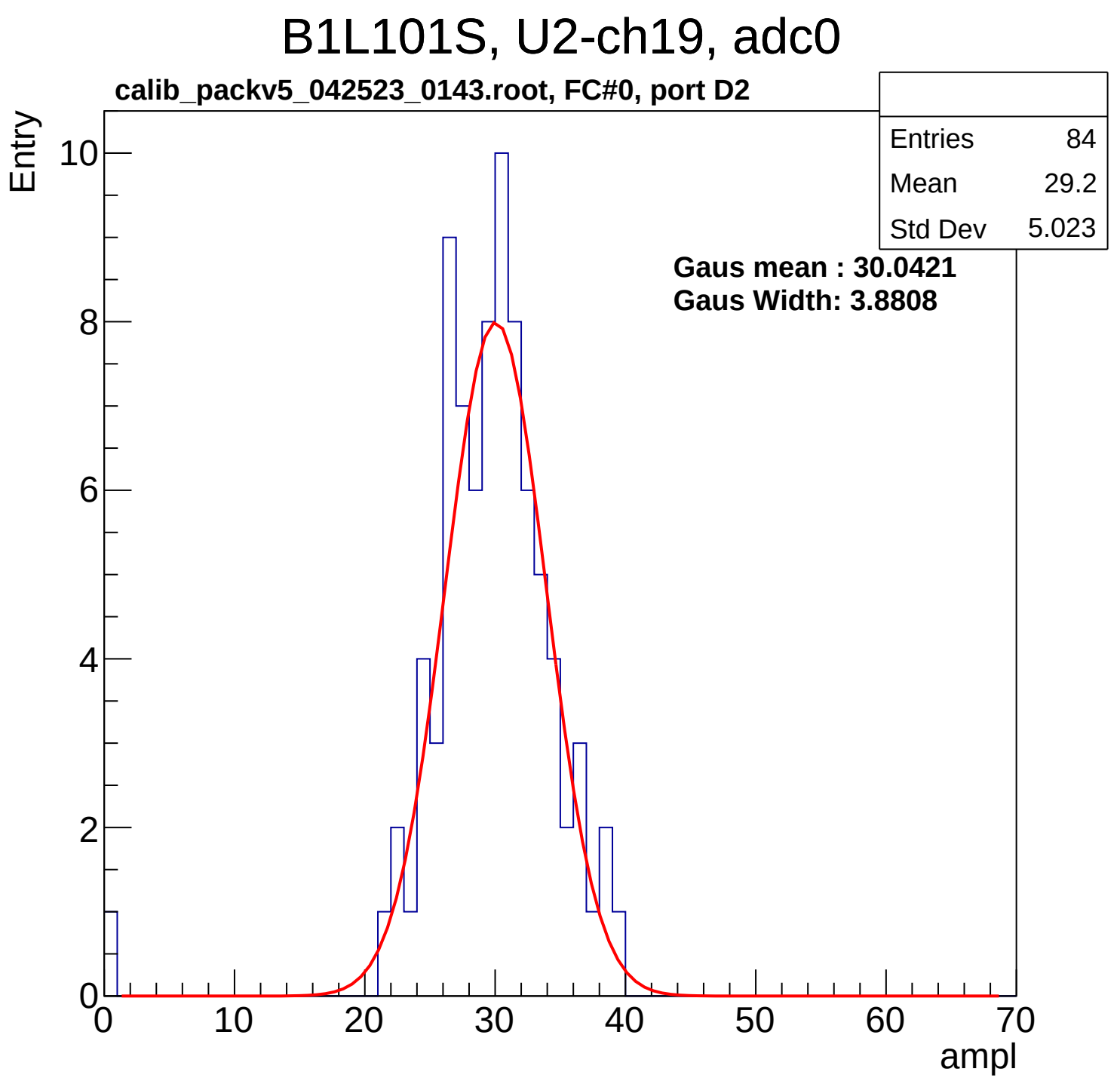

B1L101S, U2-ch18, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 48.06
Std Dev 3.787
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

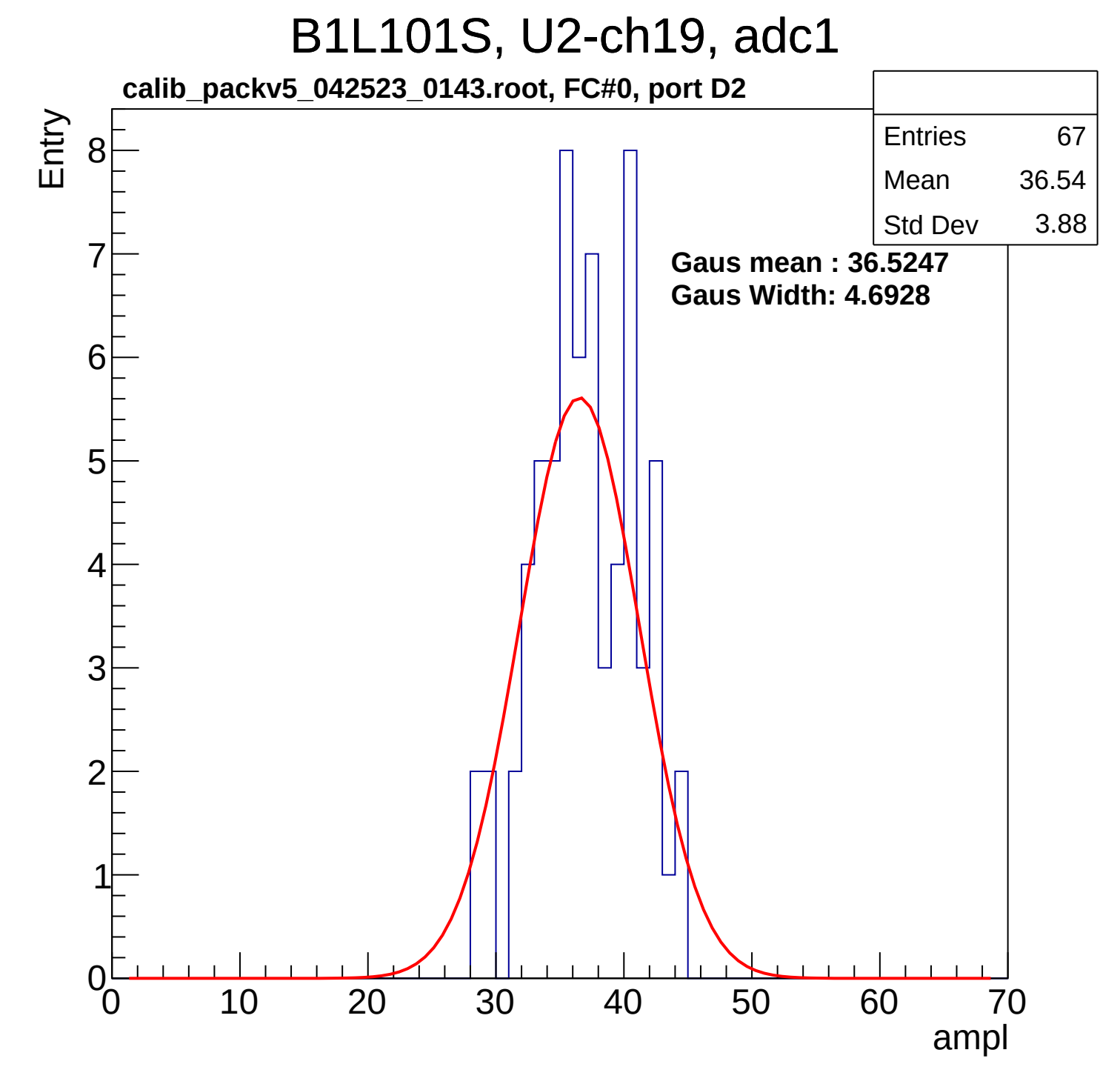

B1L101S, U2-ch18, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 54.98
Std Dev 3.525
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

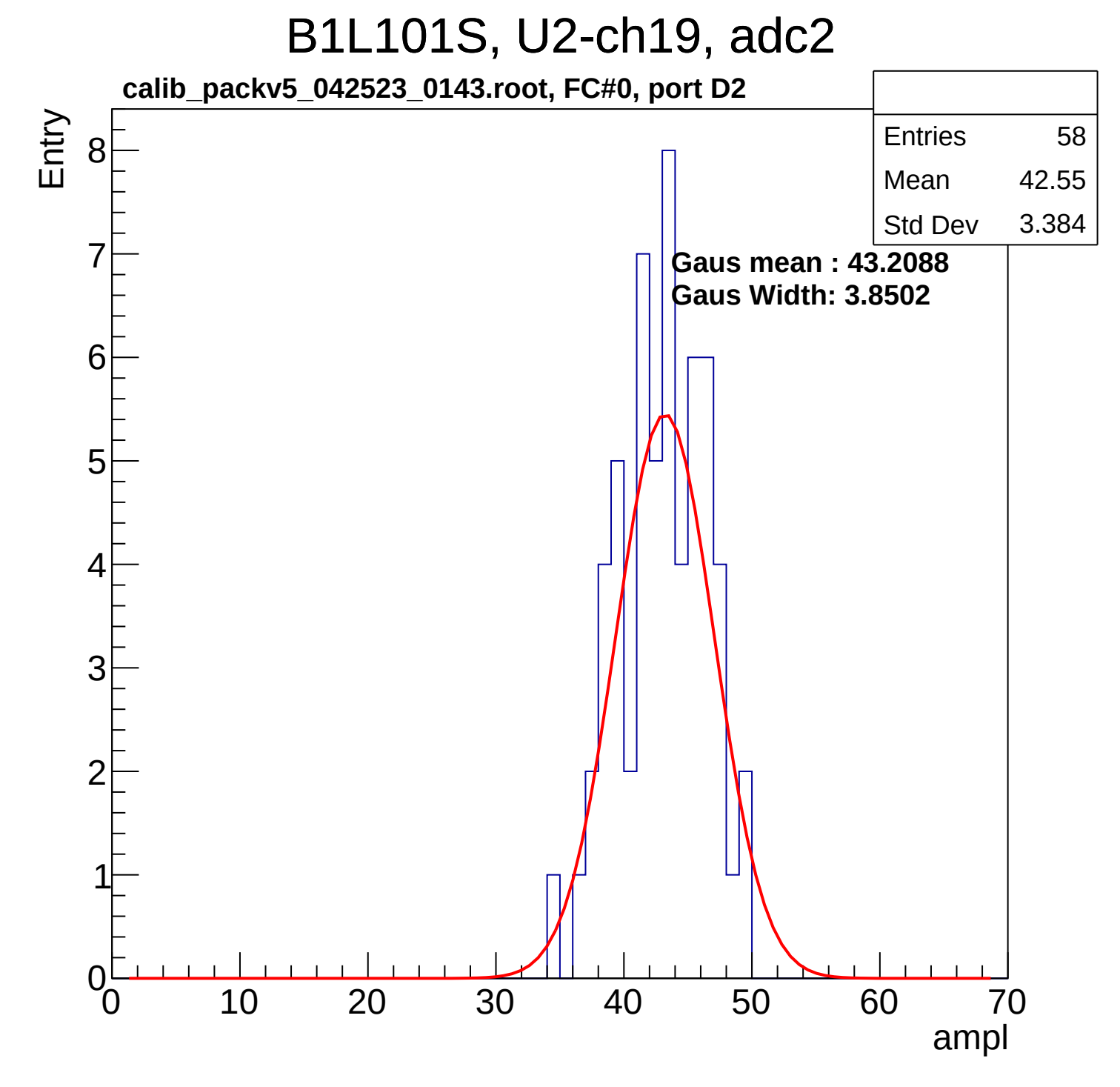

B1L101S, U2-ch18, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 41
Mean 59.22
Std Dev 2.664
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

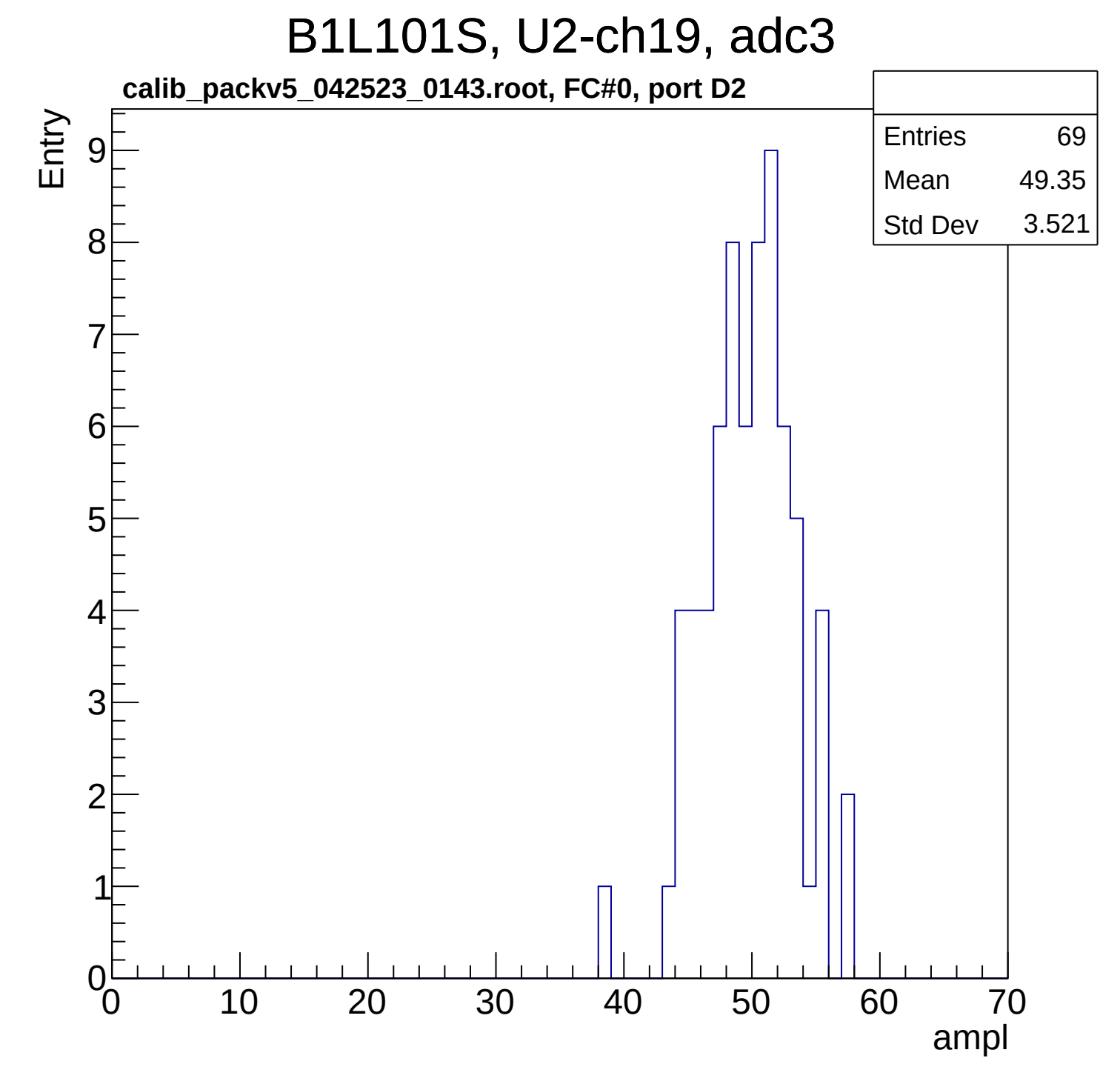

B1L101S, U2-ch18, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 14
Mean 57.14
Std Dev 15.89
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

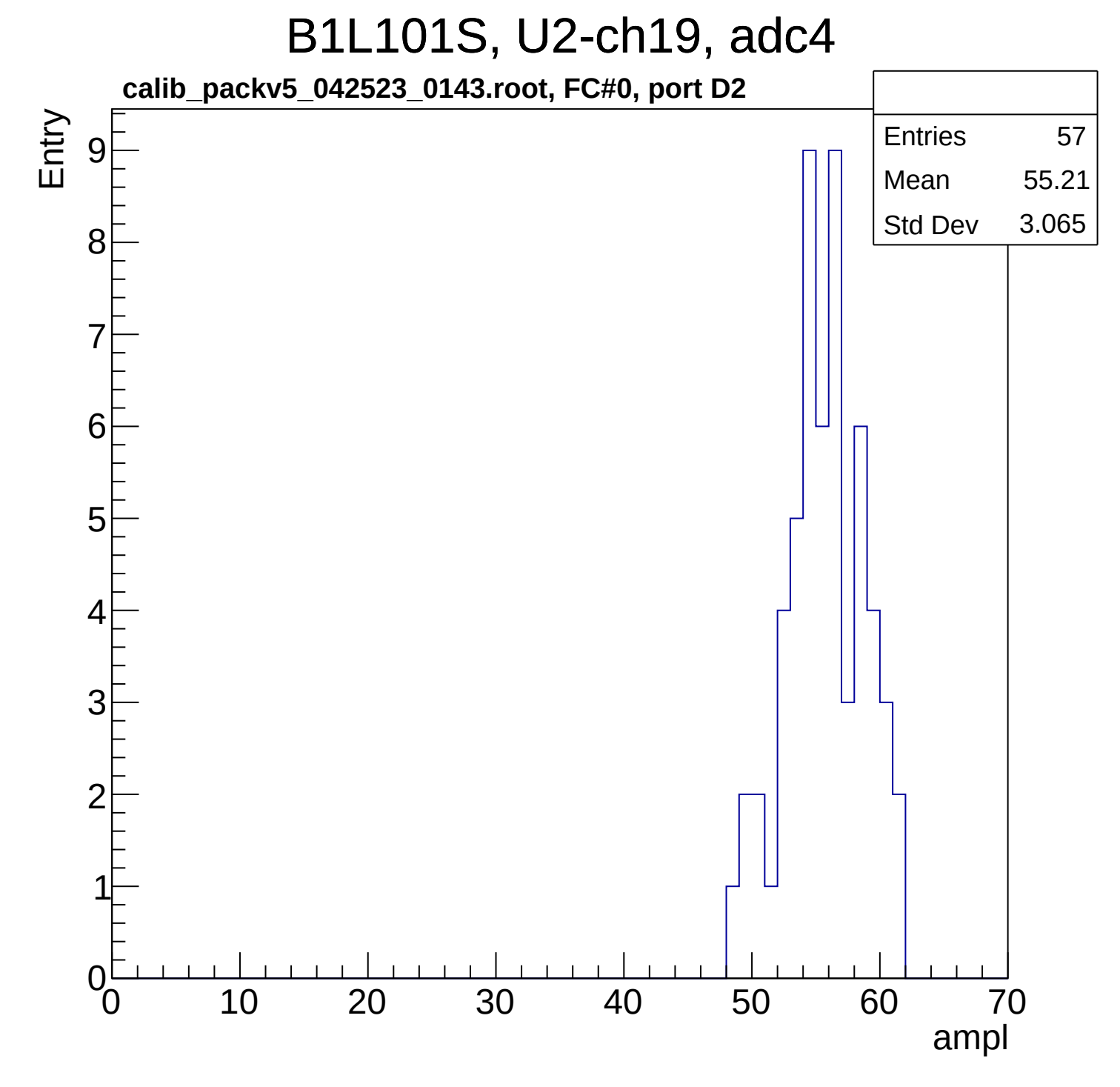

B1L101S, U2-ch18, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 31
Std Dev 31
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

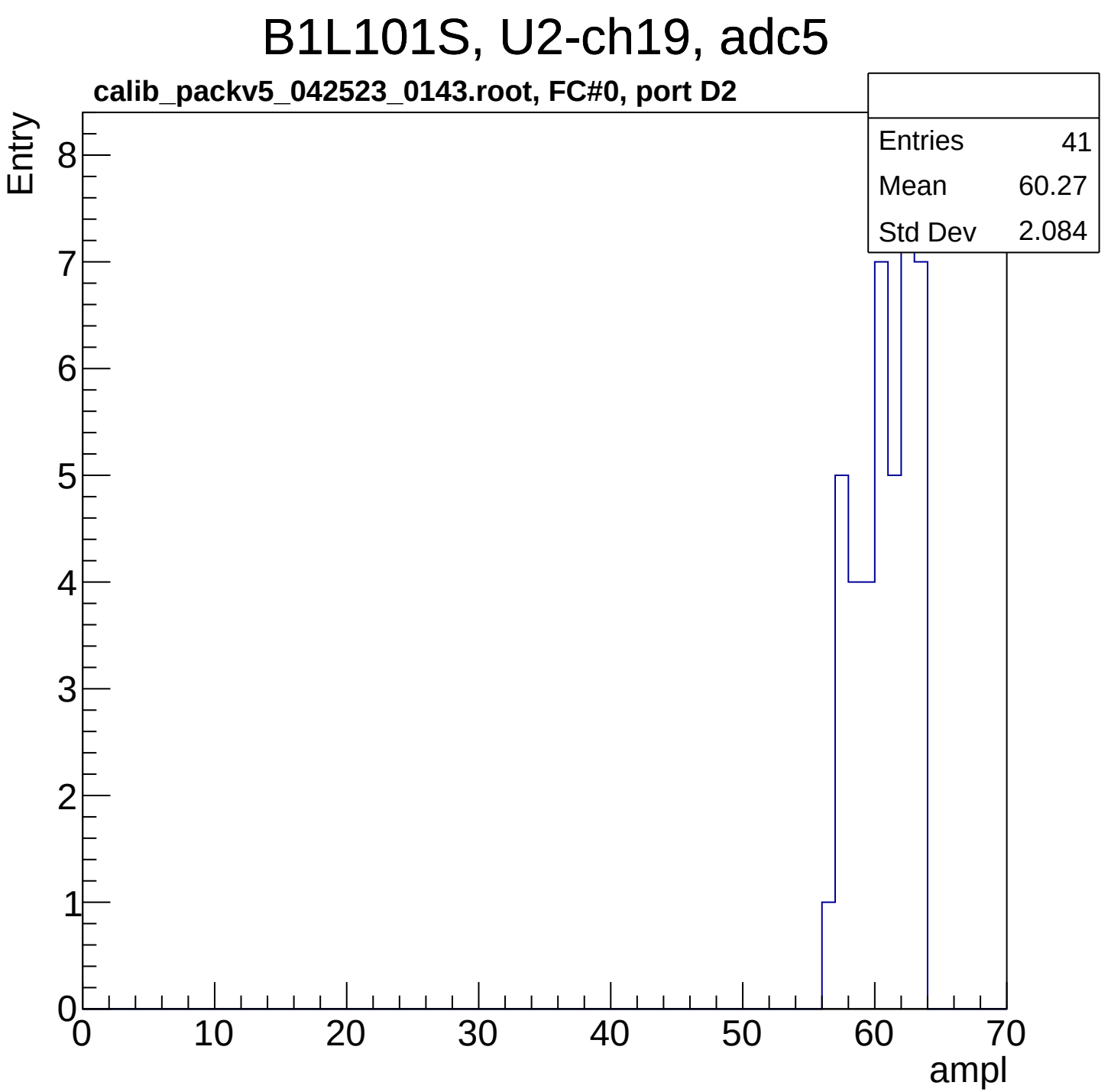

B1L101S, U2-ch19, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 84
Mean 29.2
Std Dev 5.023
Gaus mean : 30.0421
Gaus Width: 3.8808
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

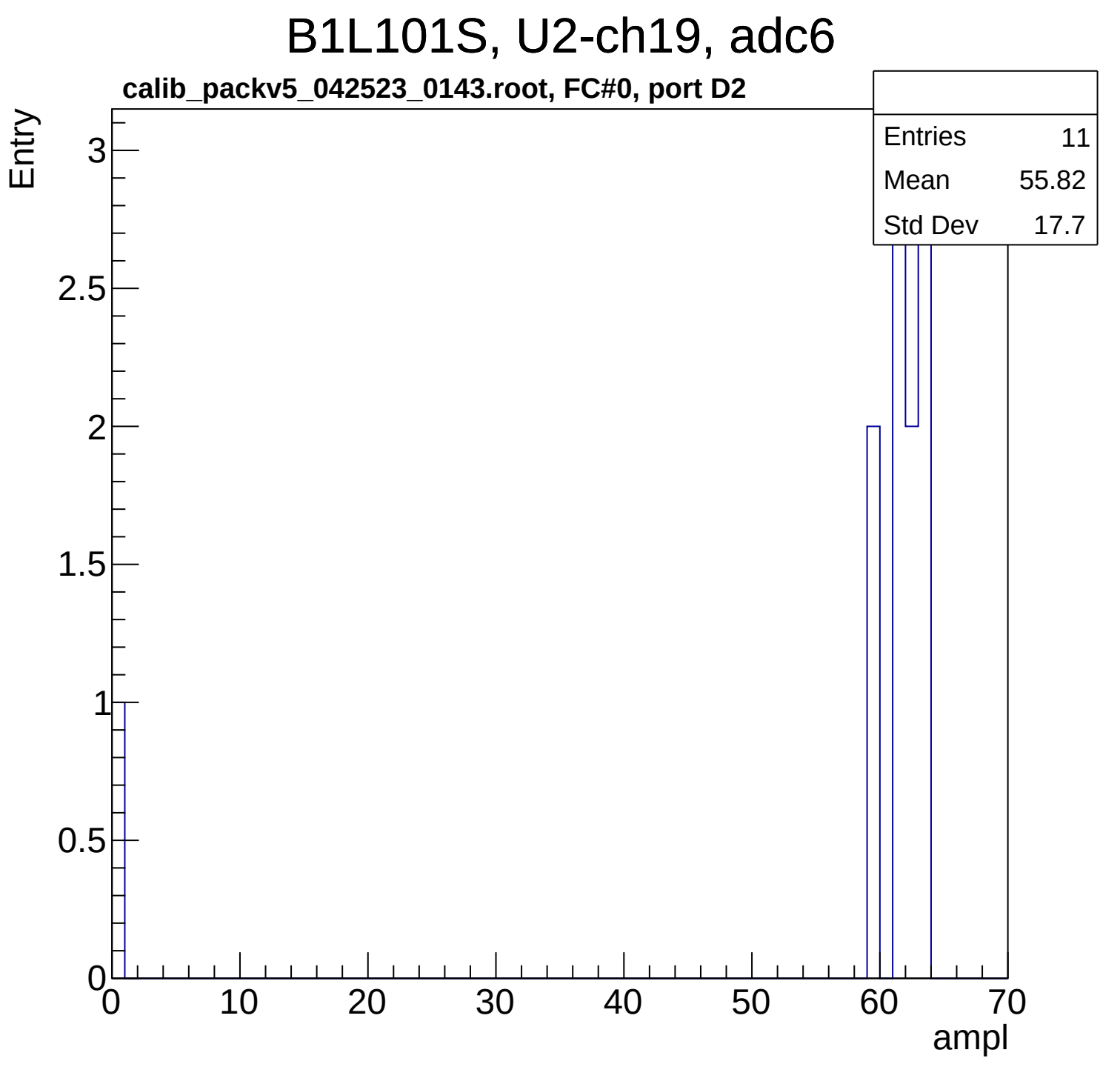

B1L101S, U2-ch19, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 36.54
Std Dev 3.88
Gaus mean : 36.5247
Gaus Width: 4.6928
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

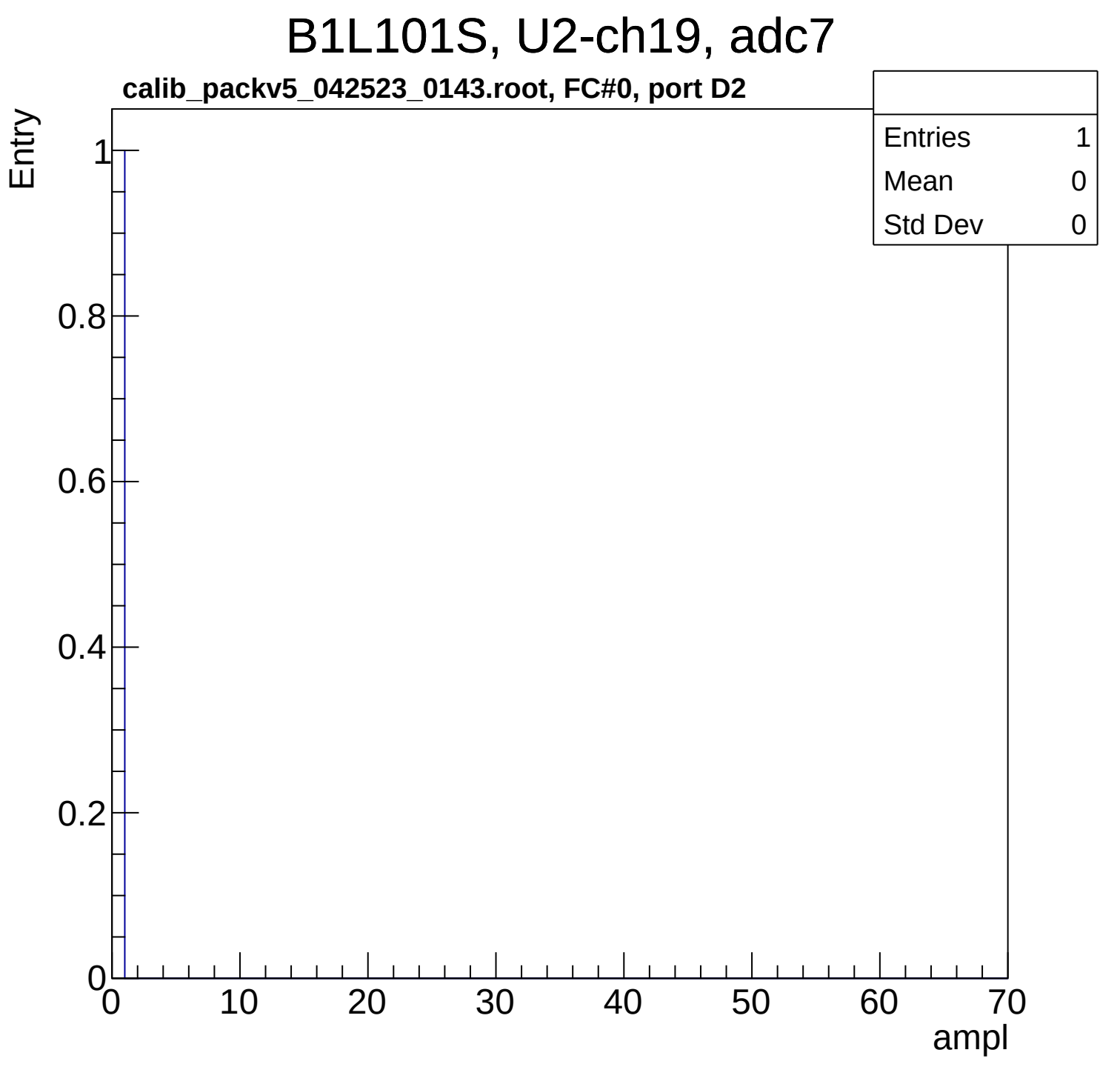

B1L101S, U2-ch19, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 42.55
Std Dev 3.384
Gaus mean : 43.2088
Gaus Width: 3.8502
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

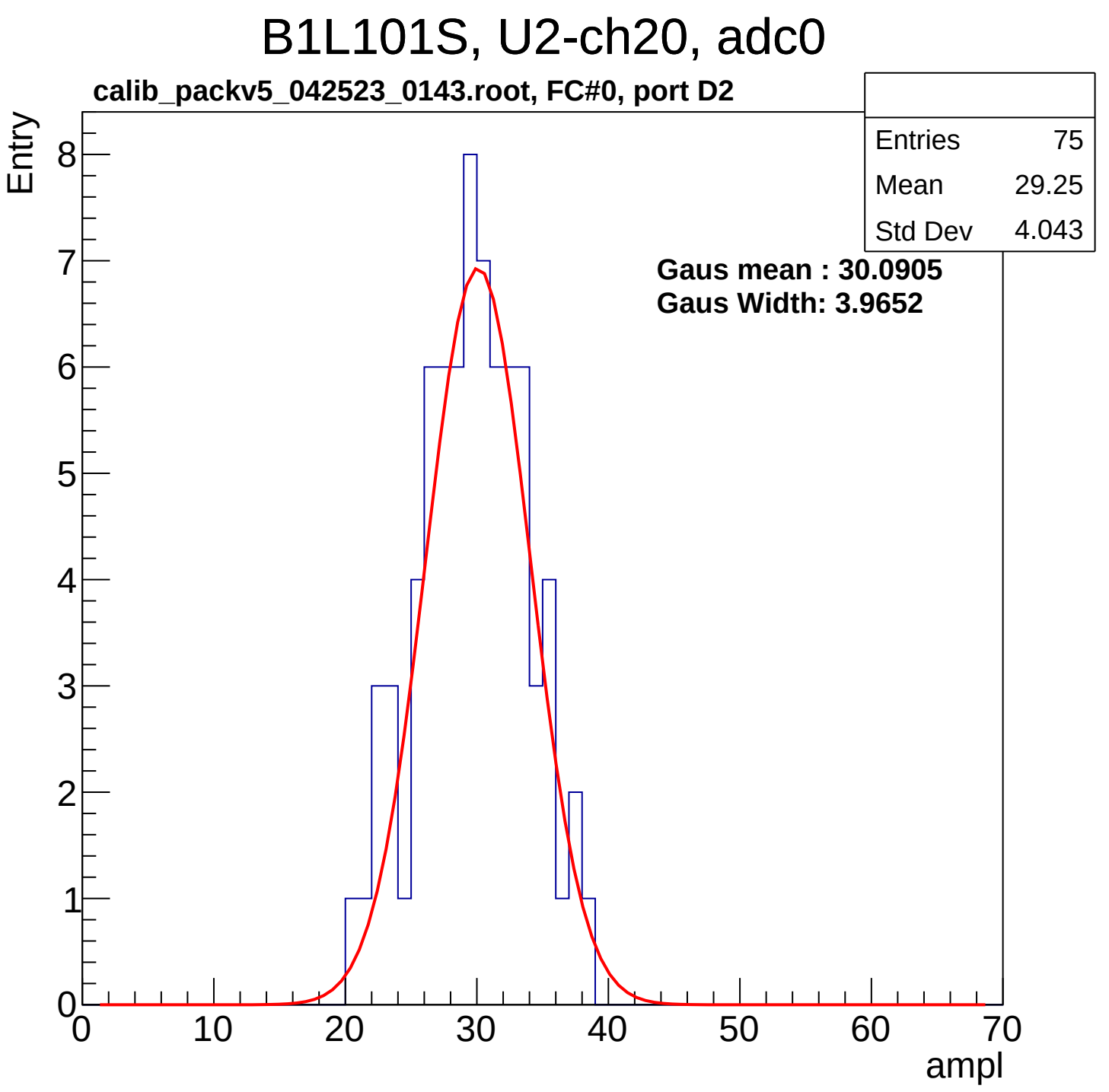

B1L101S, U2-ch19, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 49.35
Std Dev 3.521
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

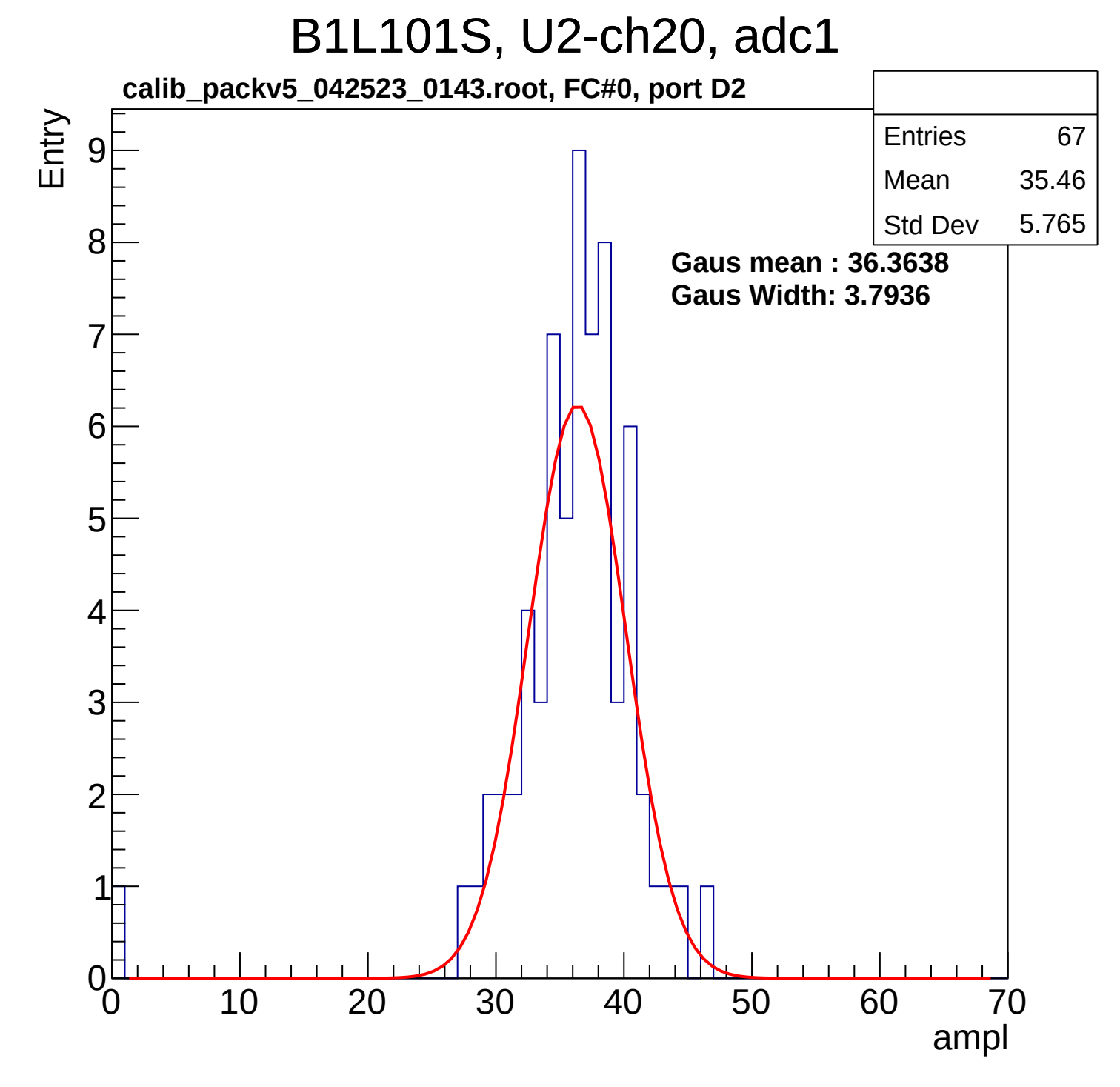

B1L101S, U2-ch19, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 55.21
Std Dev 3.065
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

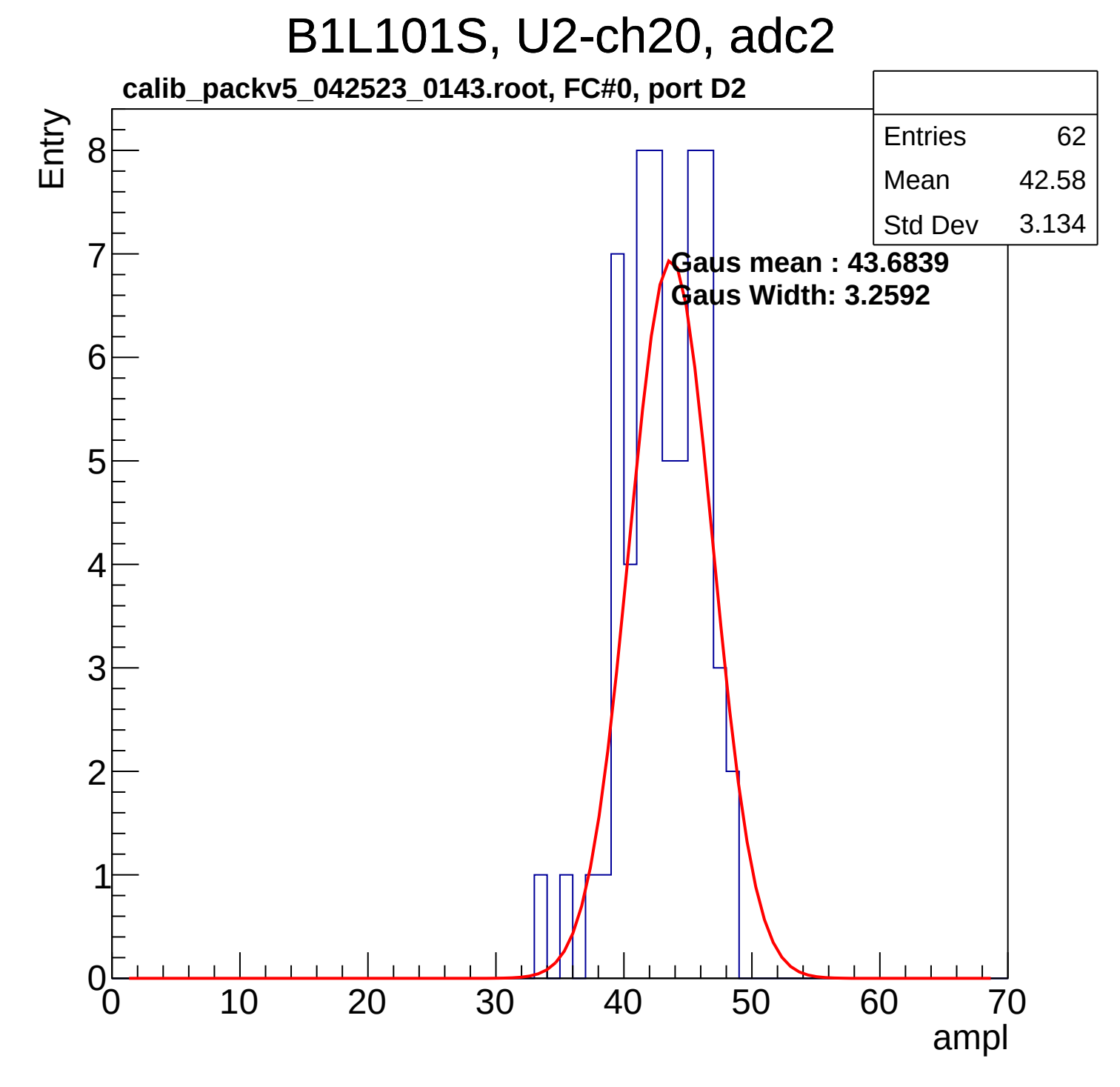

B1L101S, U2-ch19, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 41
Mean 60.27
Std Dev 2.084
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

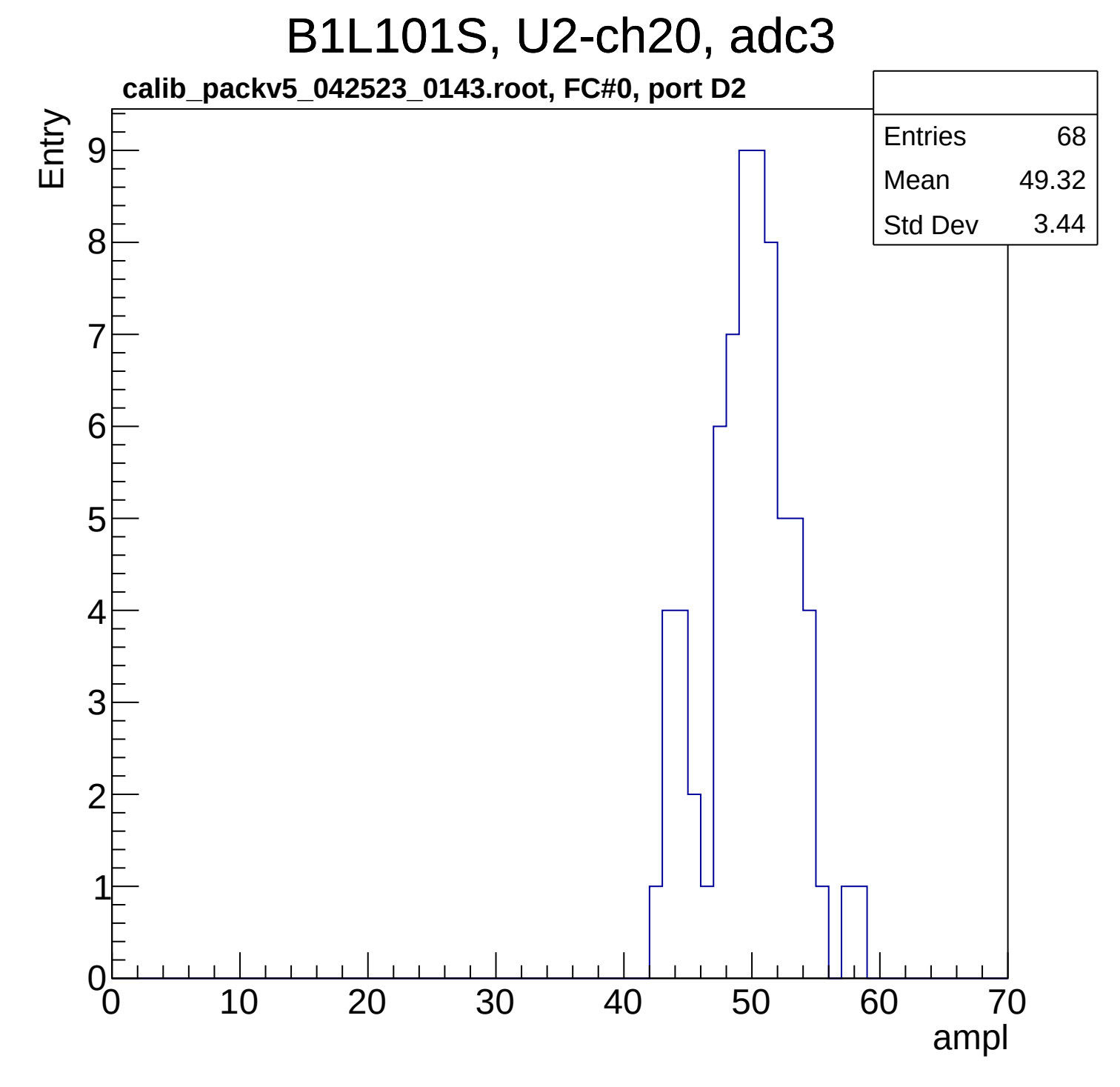

B1L101S, U2-ch19, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 11
Mean 55.82
Std Dev 17.7
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl

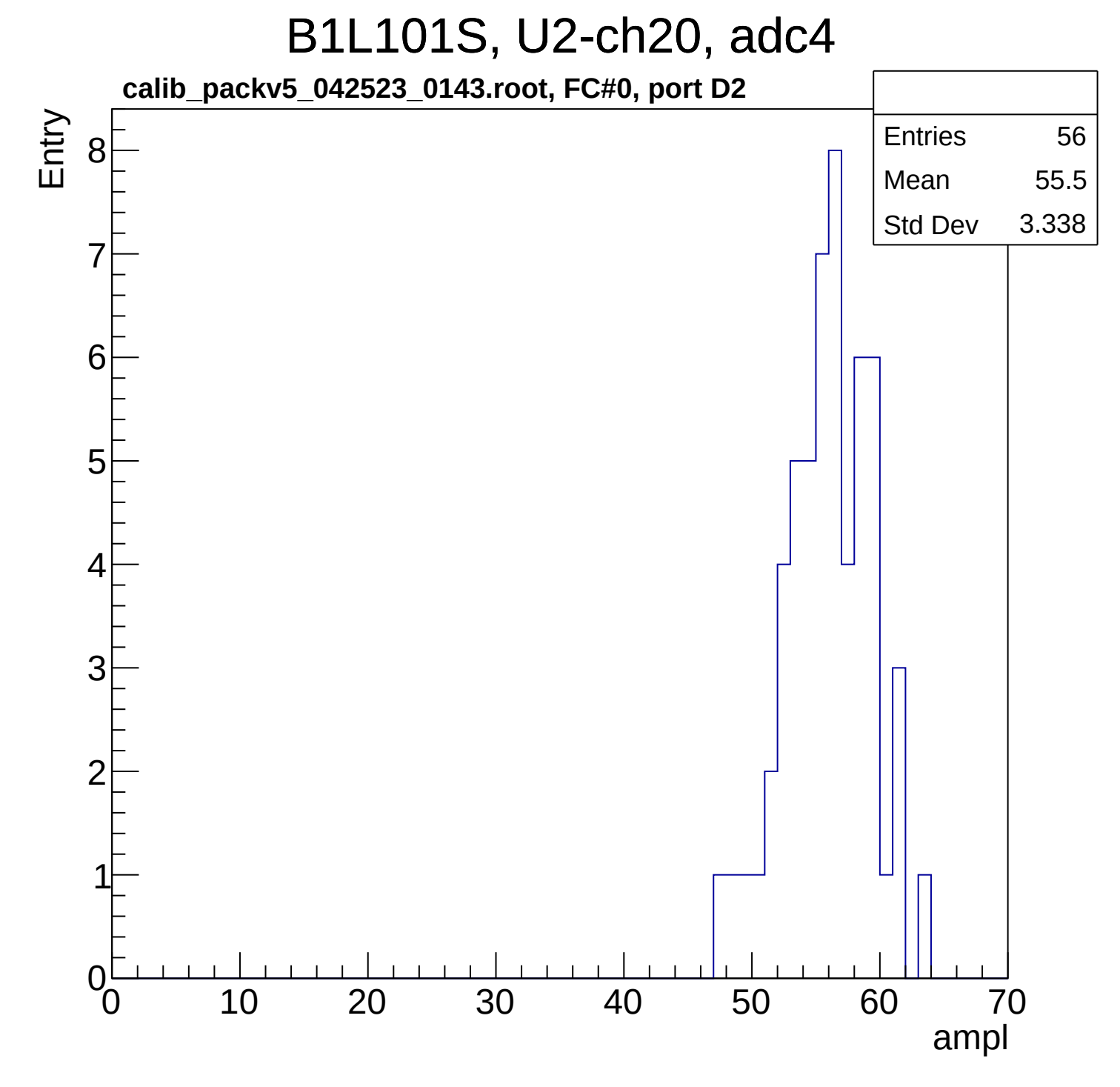

B1L101S, U2-ch19, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

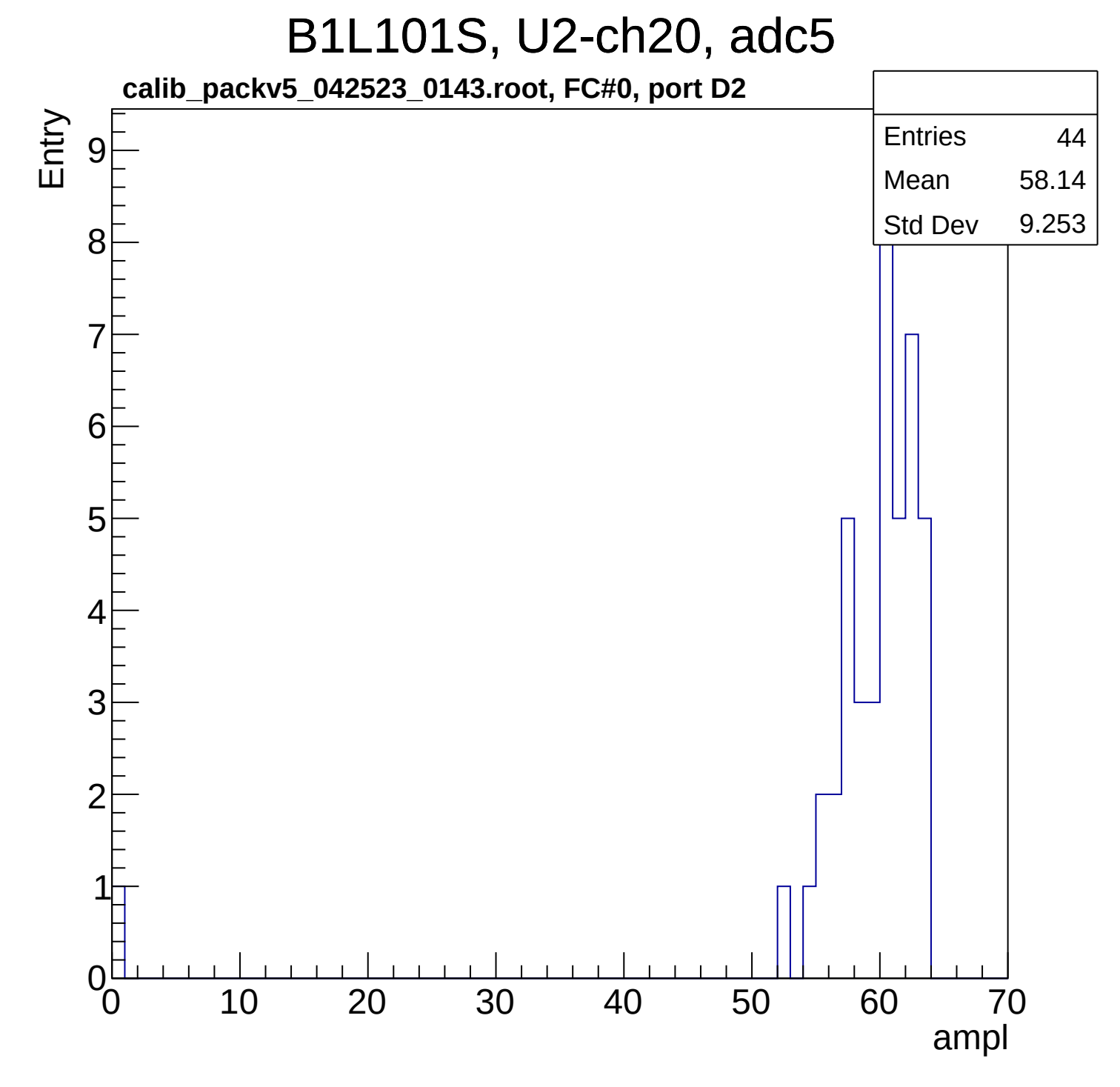

B1L101S, U2-ch20, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 29.25
Std Dev 4.043
Gaus mean : 30.0905
Gaus Width: 3.9652
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

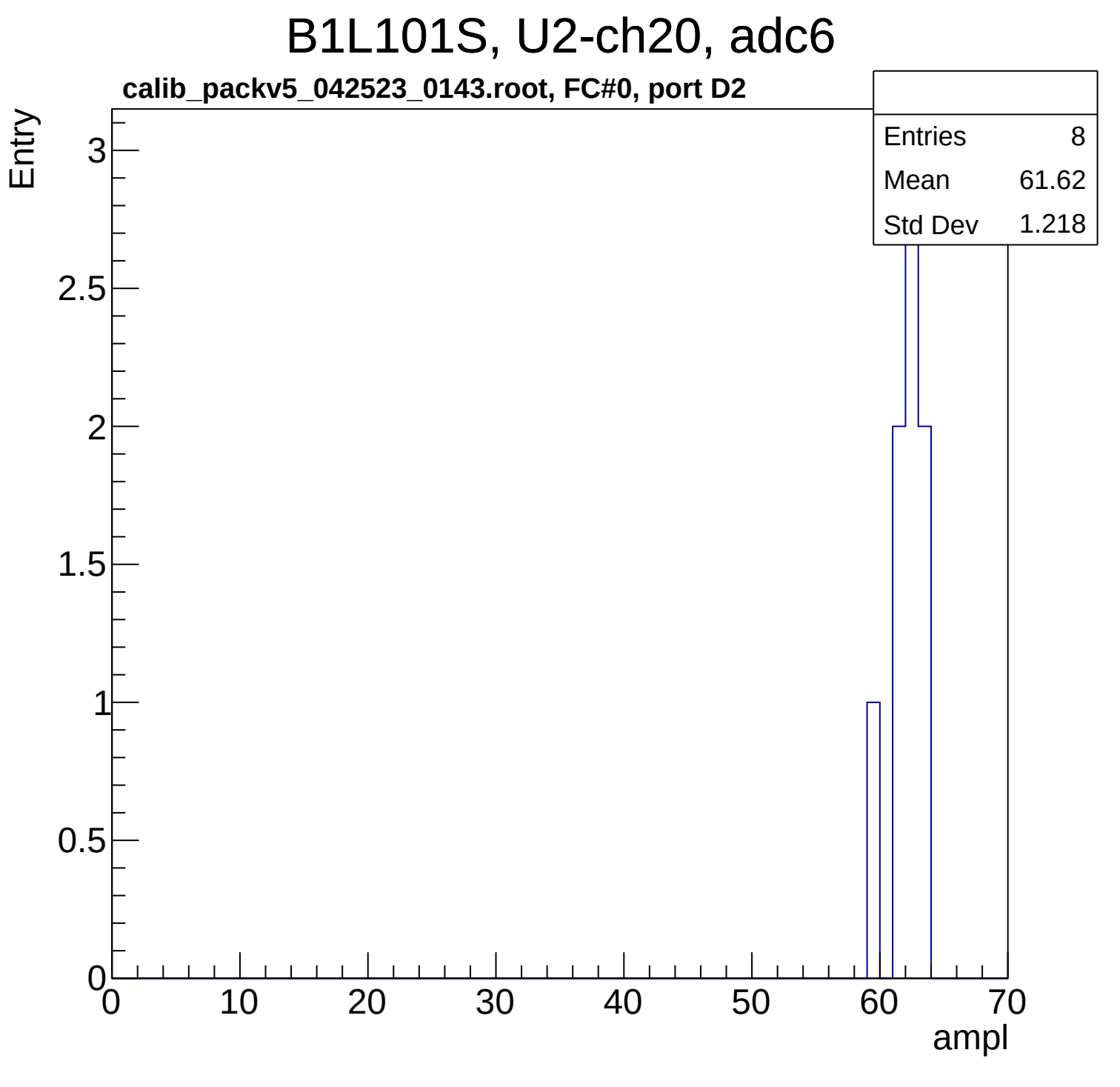

B1L101S, U2-ch20, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 35.46
Std Dev 5.765
Gaus mean : 36.3638
Gaus Width: 3.7936
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

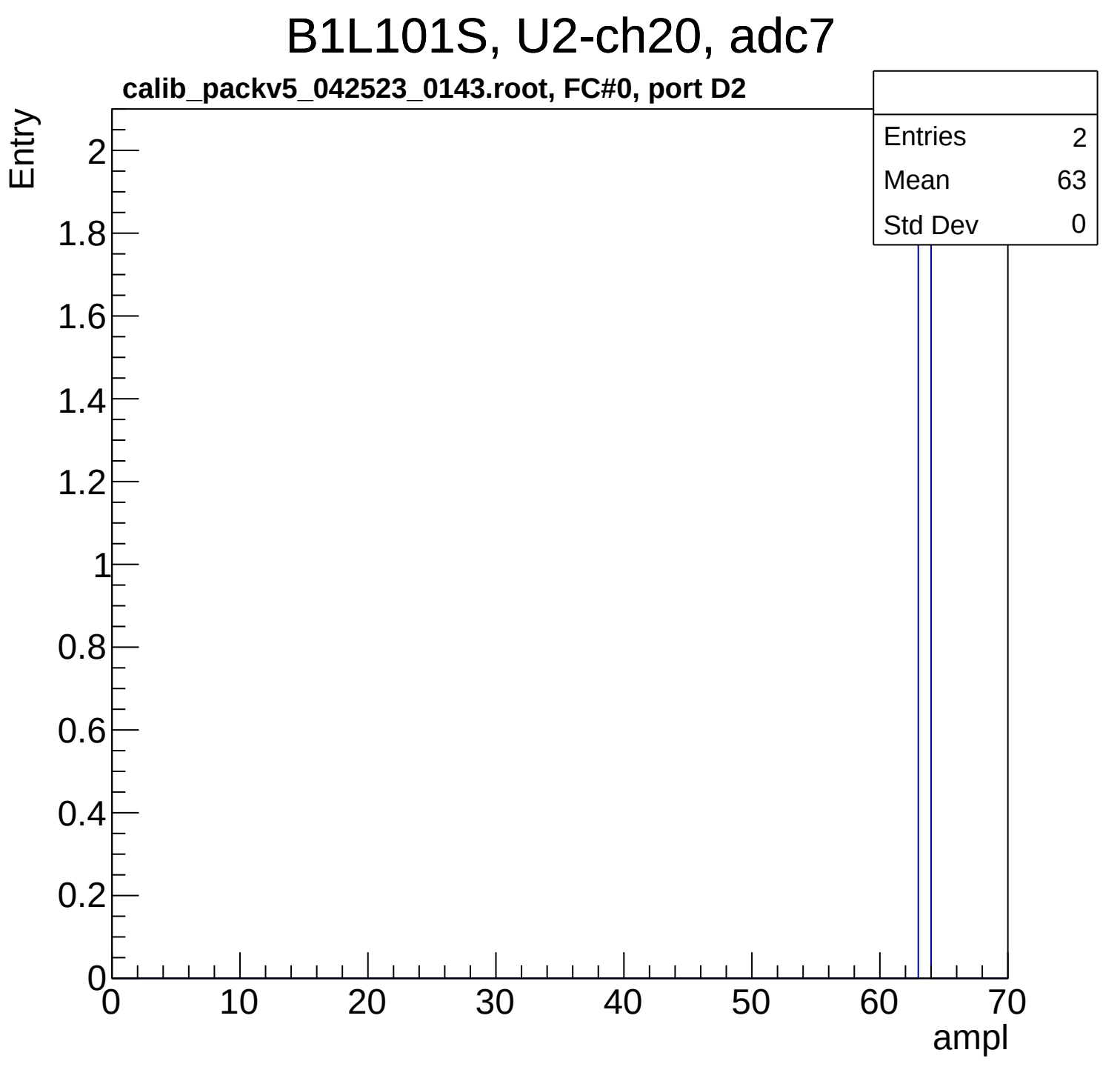

B1L101S, U2-ch20, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 42.58
Std Dev 3.134
Gaus mean : 43.6839
Gaus Width: 3.2592
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

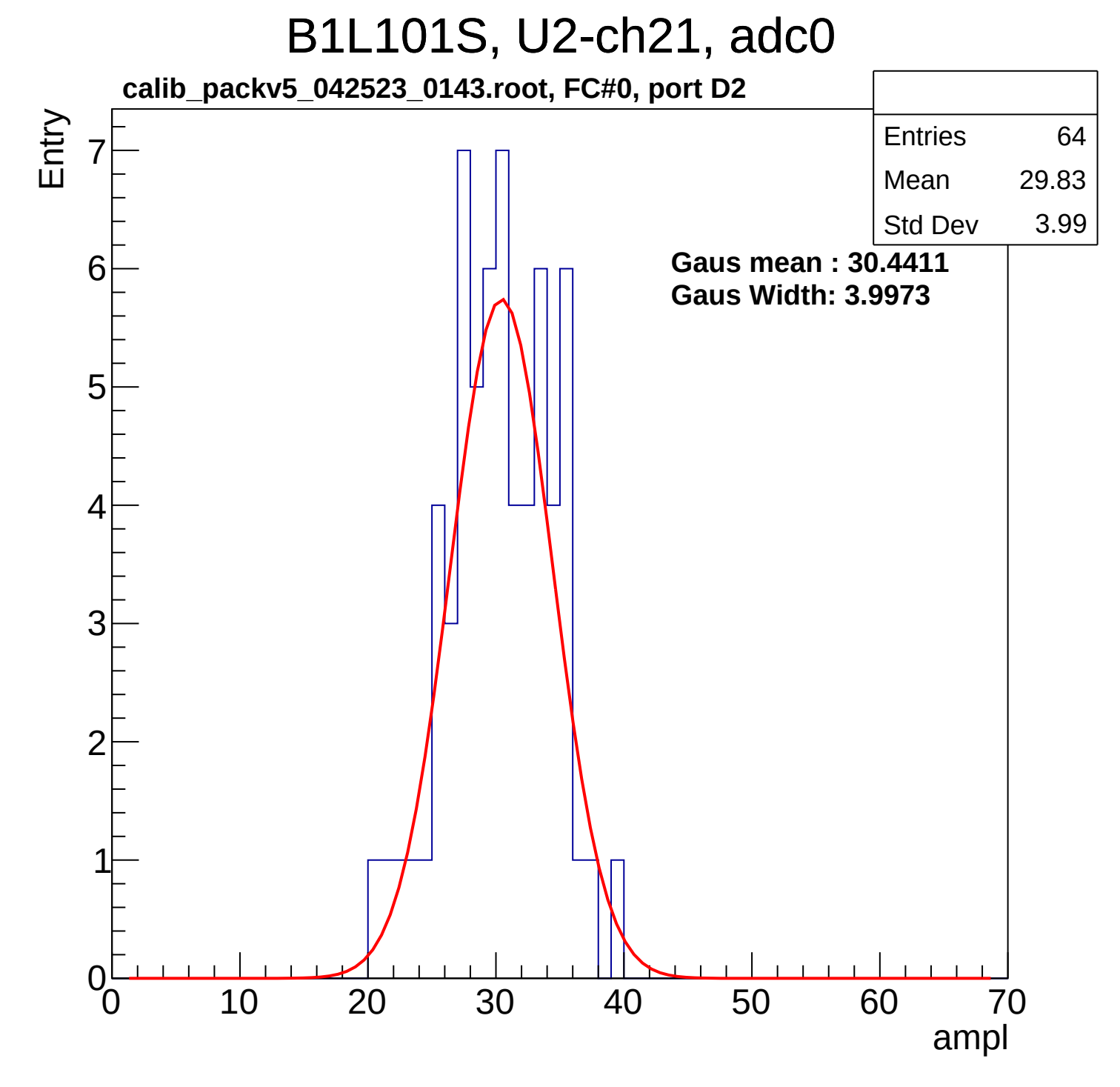

B1L101S, U2-ch20, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 49.32
Std Dev 3.44
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

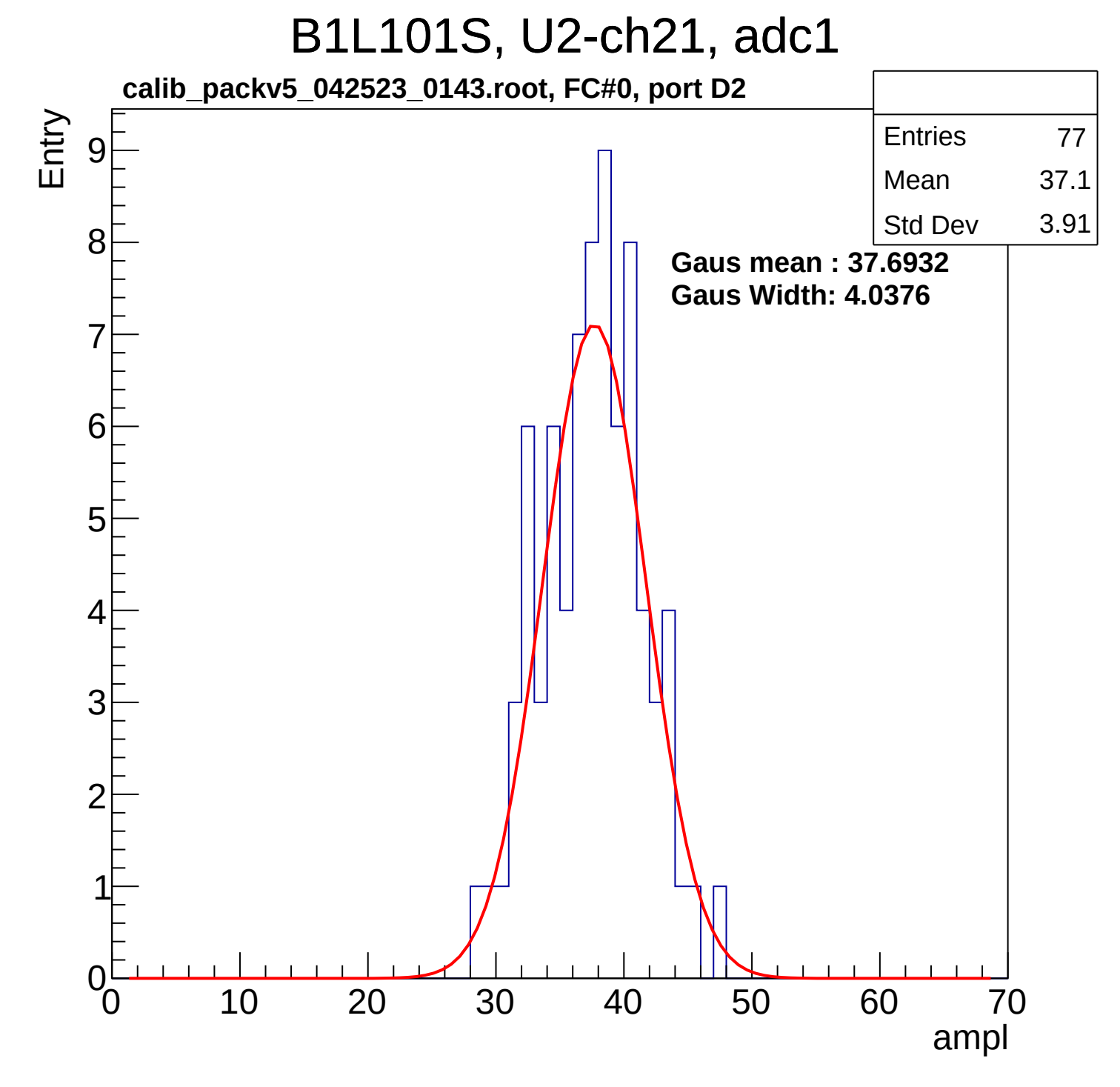

B1L101S, U2-ch20, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 55.5
Std Dev 3.338
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

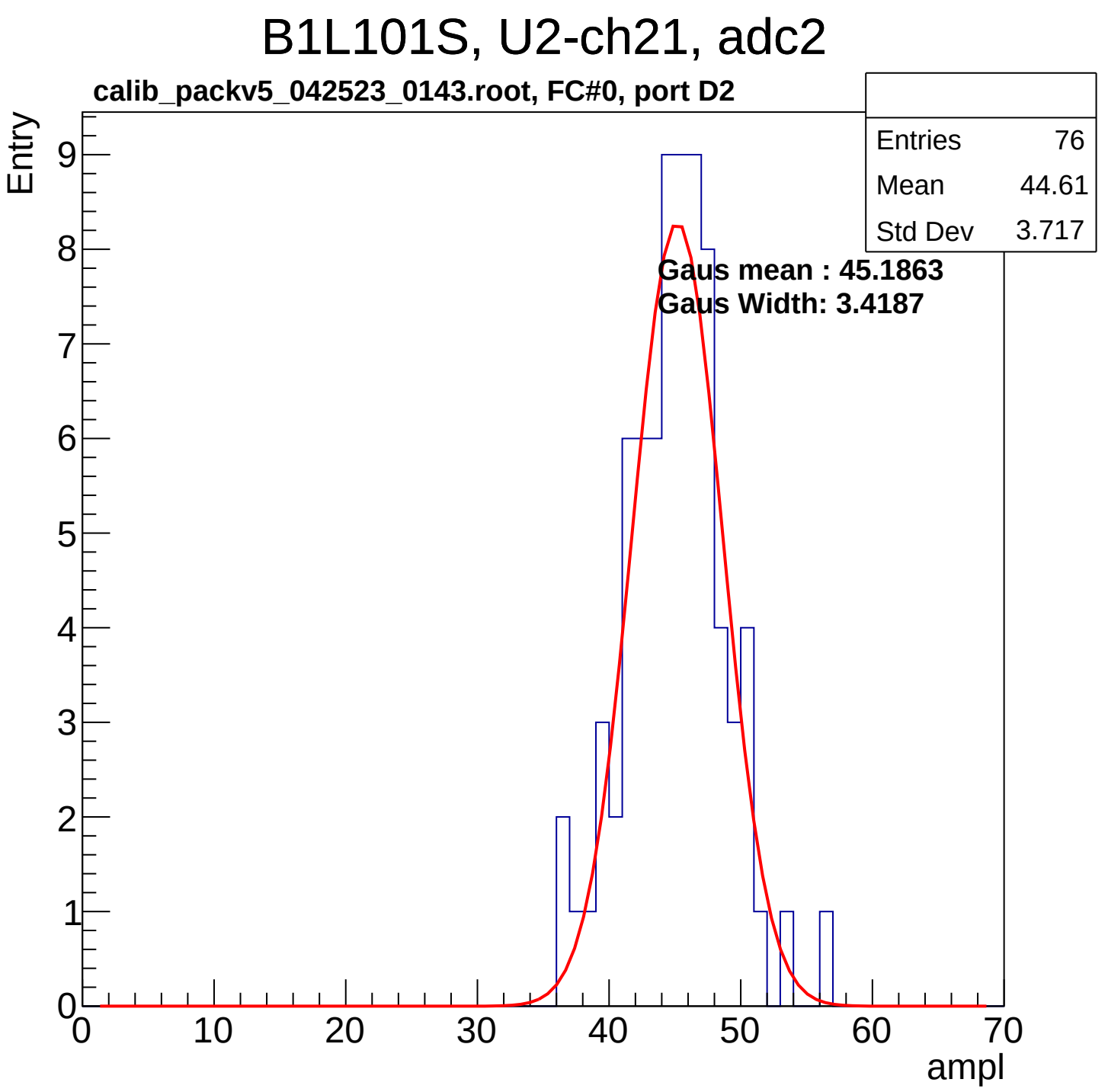

B1L101S, U2-ch20, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 44
Mean 58.14
Std Dev 9.253
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

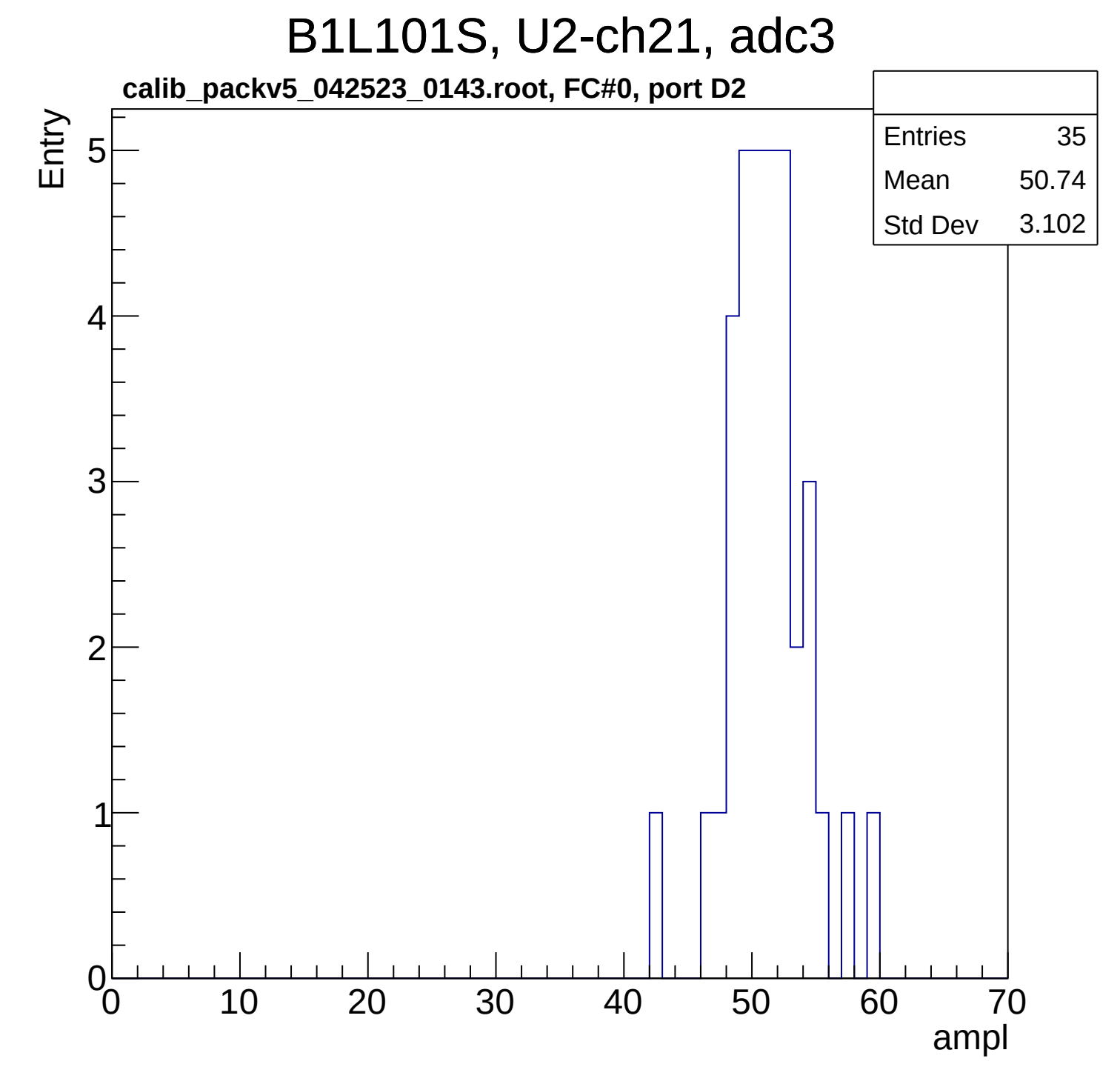

B1L101S, U2-ch20, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 61.62
Std Dev 1.218
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

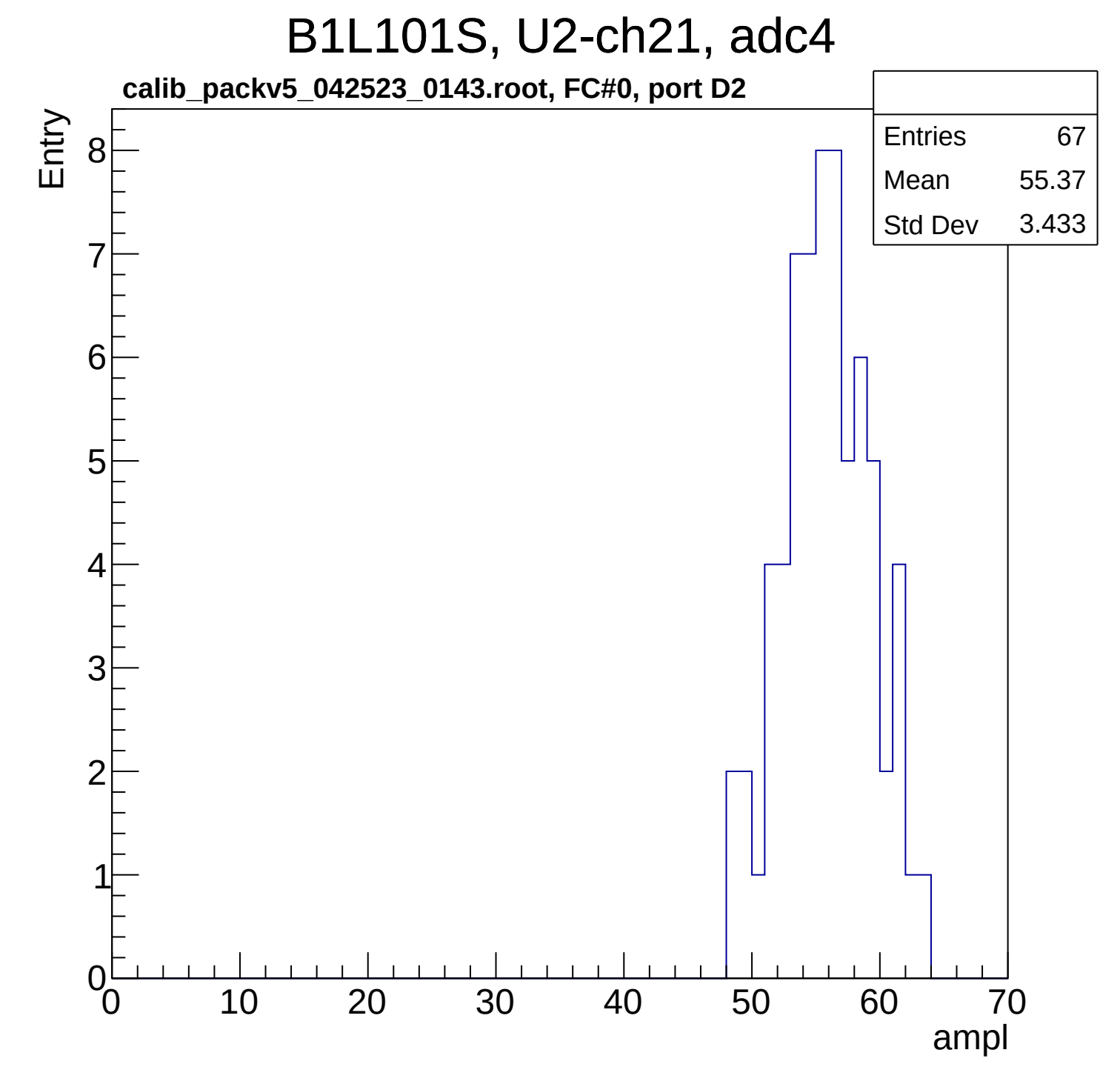

B1L101S, U2-ch20, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

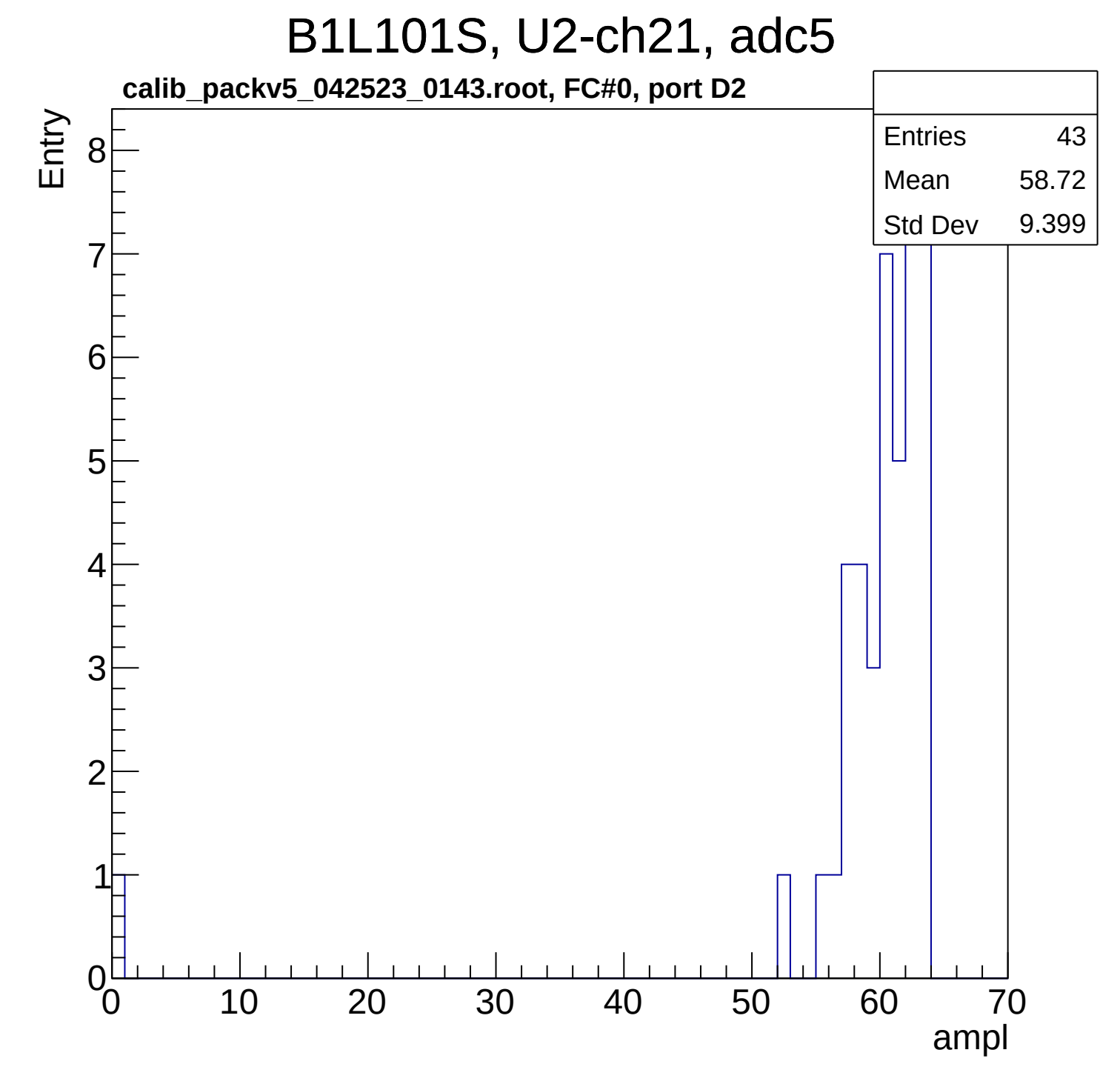

B1L101S, U2-ch21, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 29.83
Std Dev 3.99
Gaus mean : 30.4411
Gaus Width: 3.9973
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

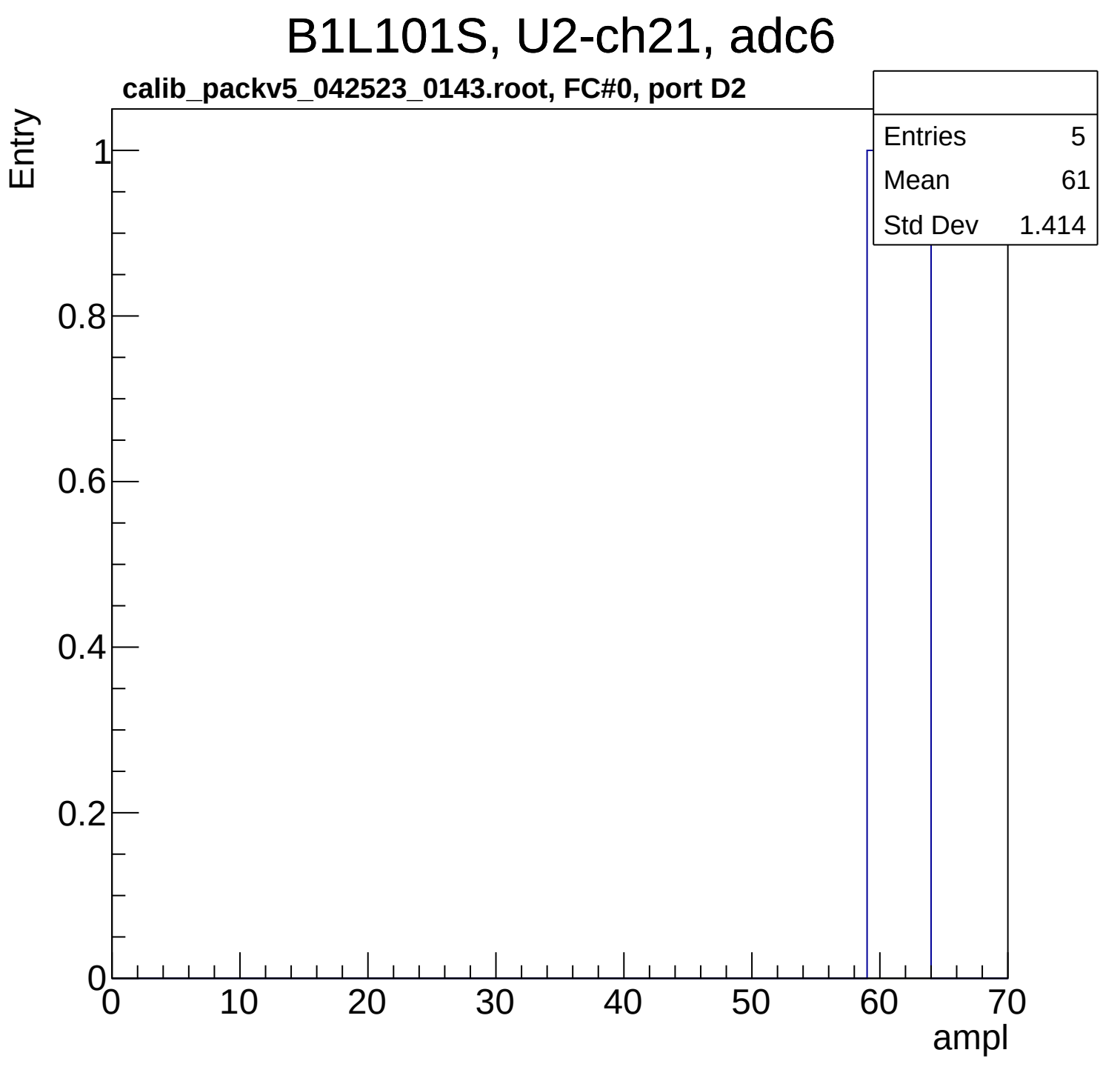

B1L101S, U2-ch21, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 37.1
Std Dev 3.91
Gaus mean : 37.6932
Gaus Width: 4.0376
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

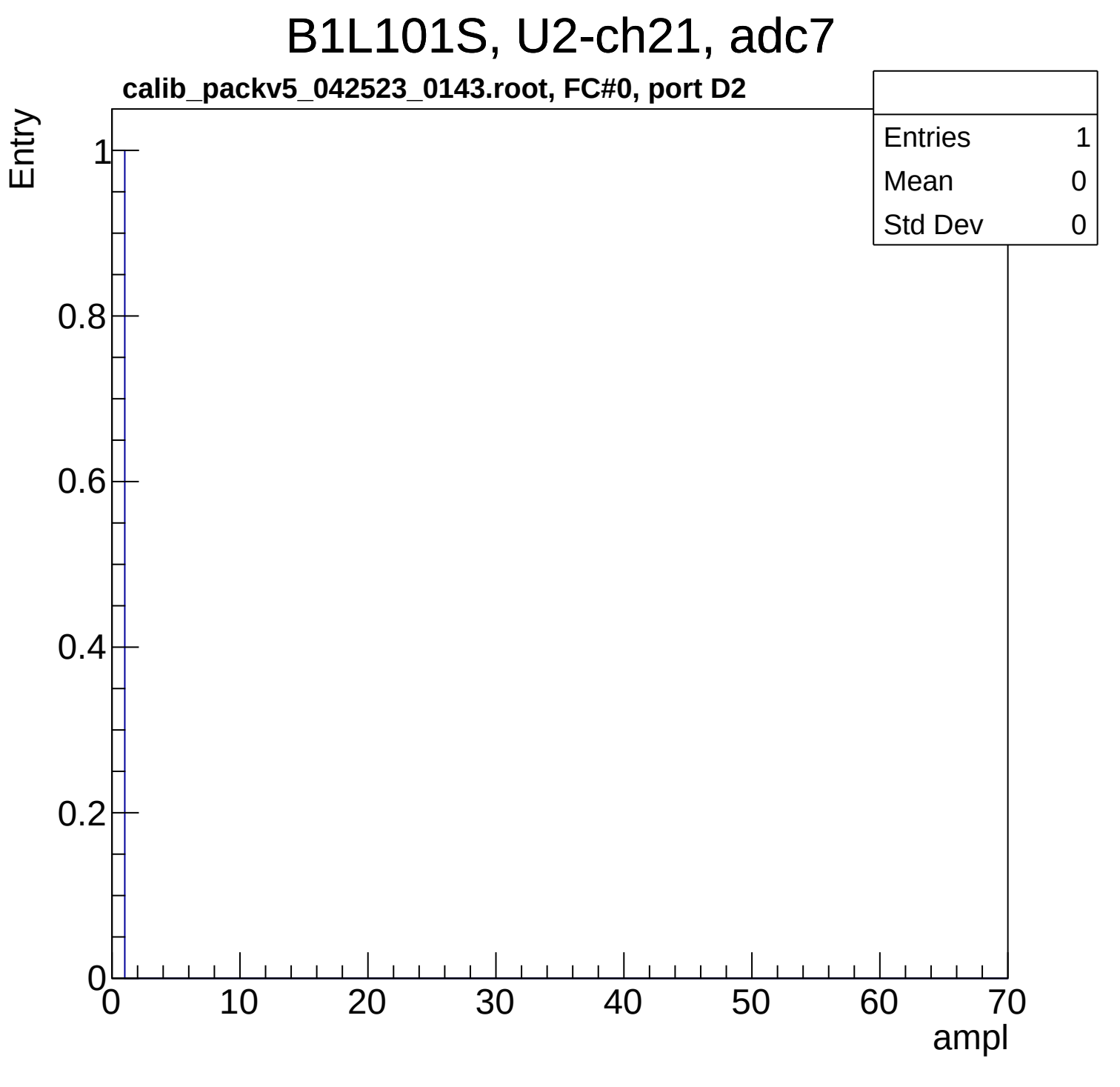

B1L101S, U2-ch21, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 44.61
Std Dev 3.717
Gaus mean : 45.1863
Gaus Width: 3.4187
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

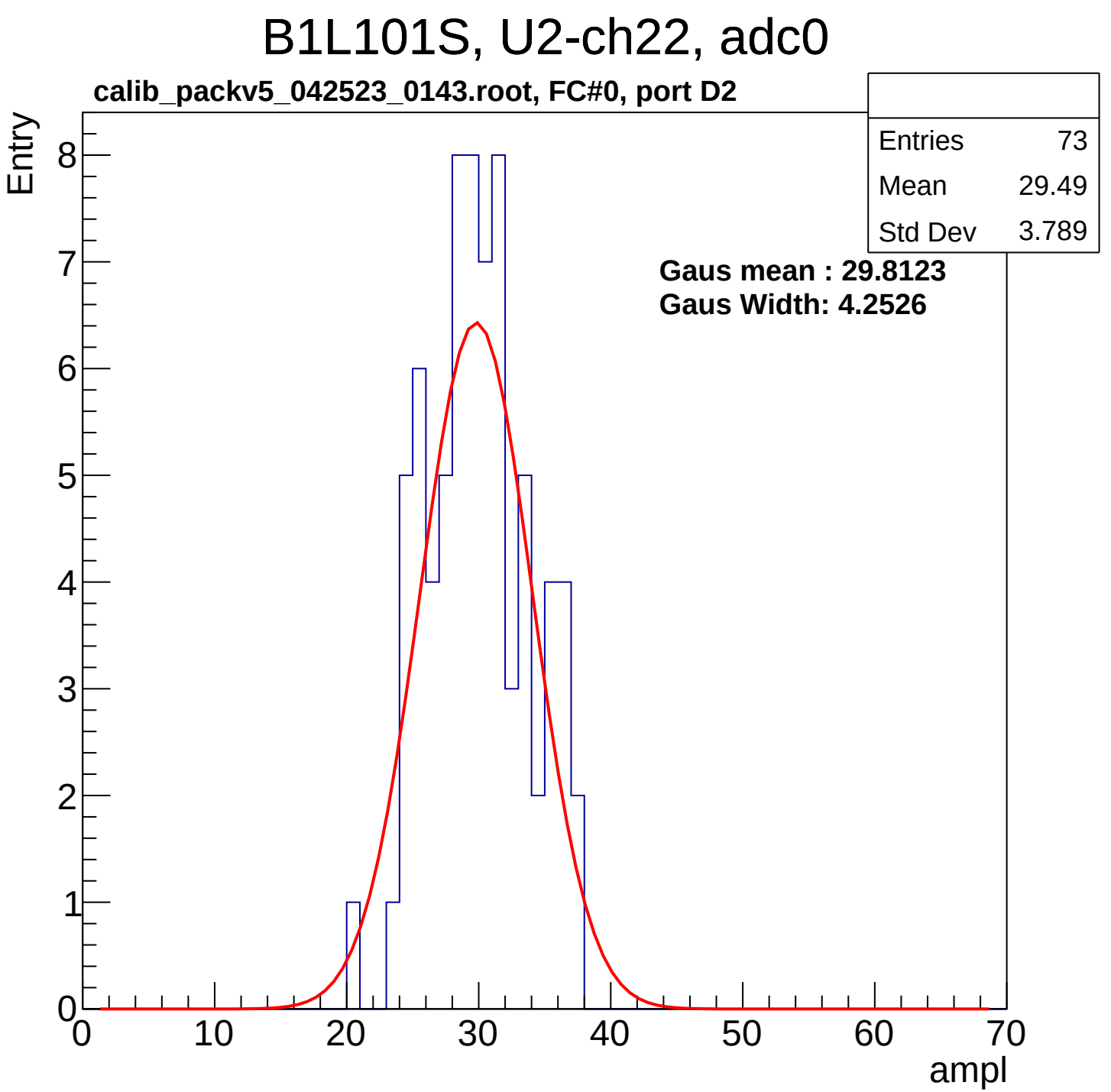

B1L101S, U2-ch21, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 35
Mean 50.74
Std Dev 3.102
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

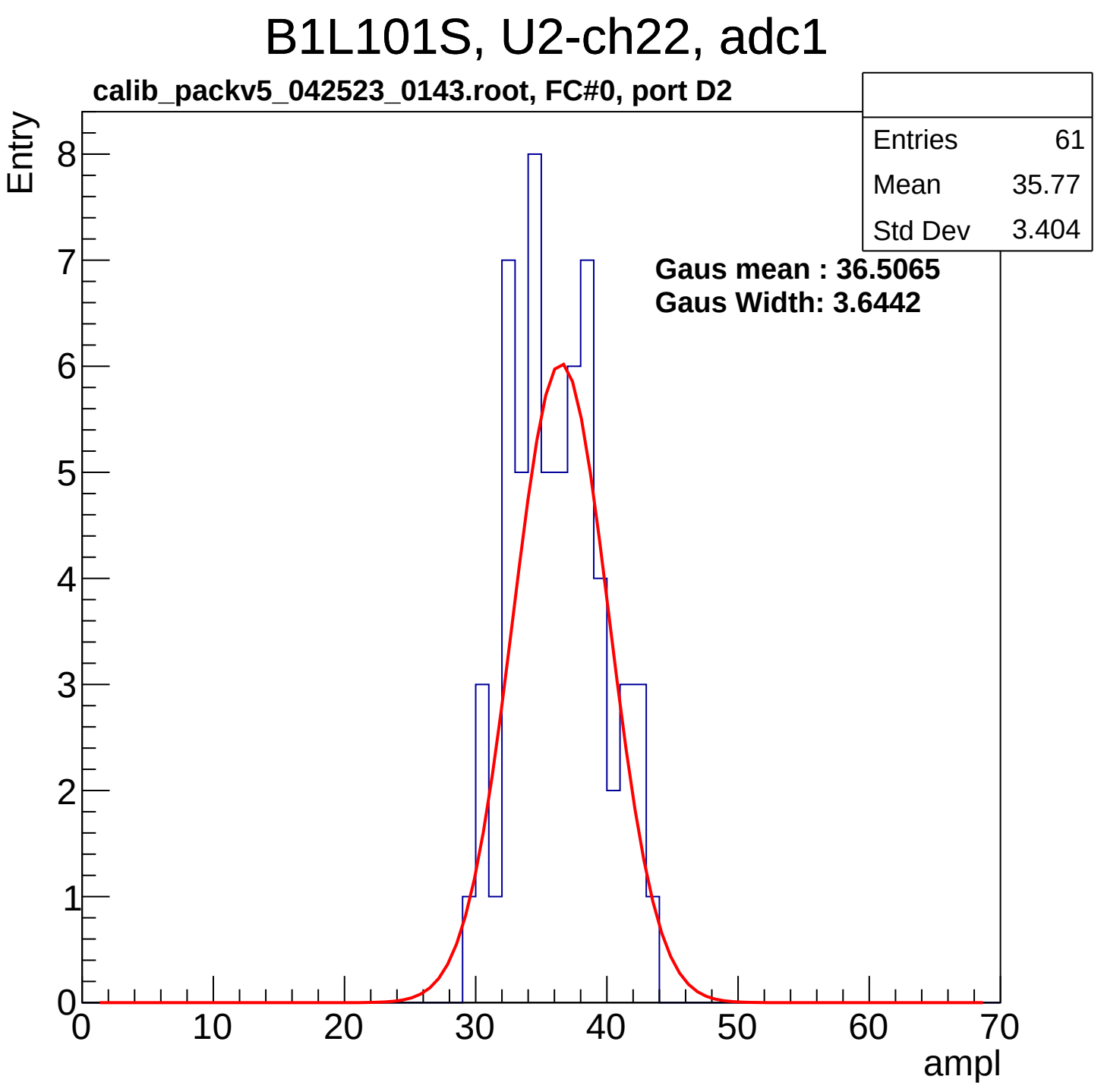

B1L101S, U2-ch21, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 55.37
Std Dev 3.433
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

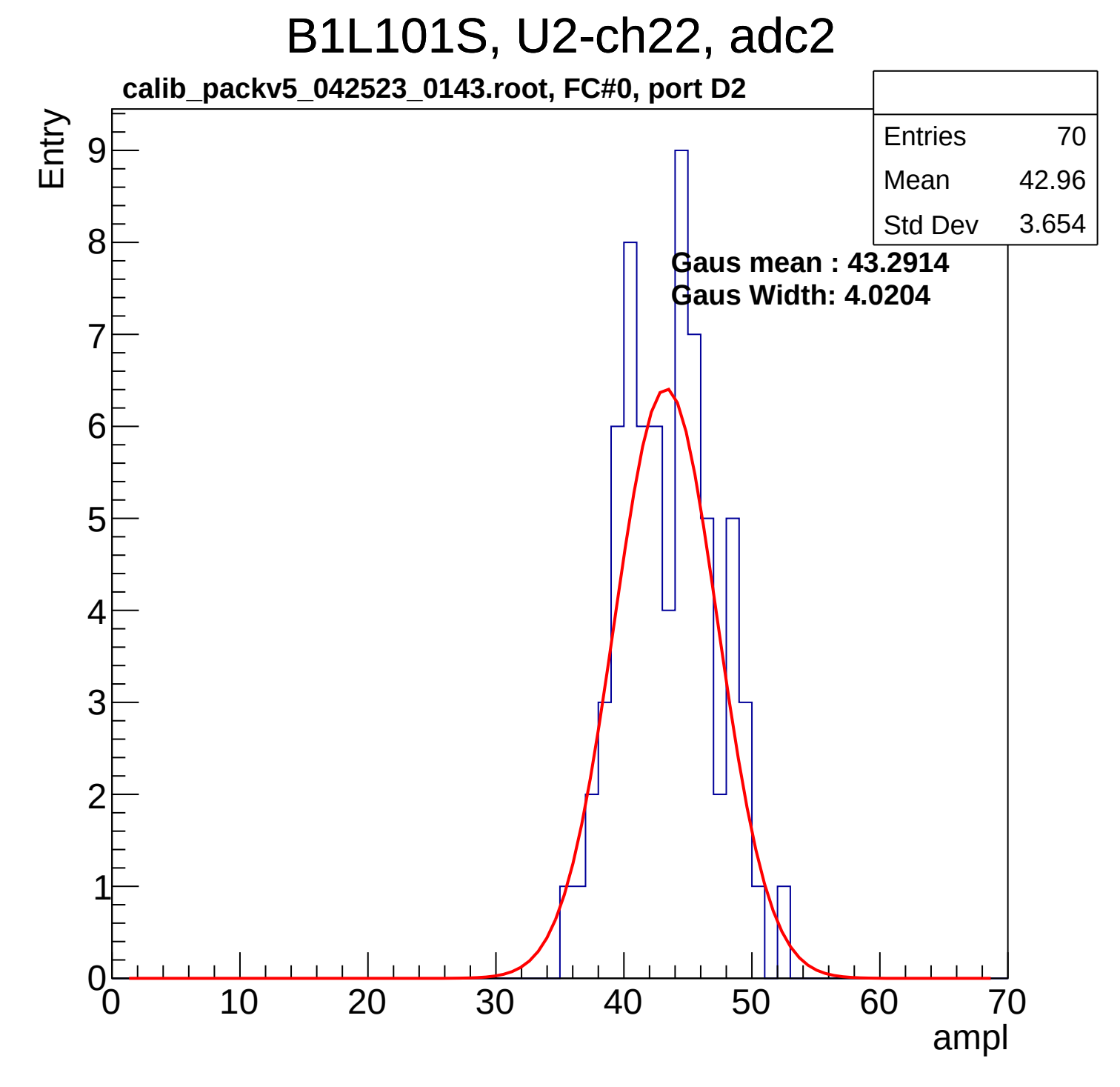

B1L101S, U2-ch21, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 43
Mean 58.72
Std Dev 9.399
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

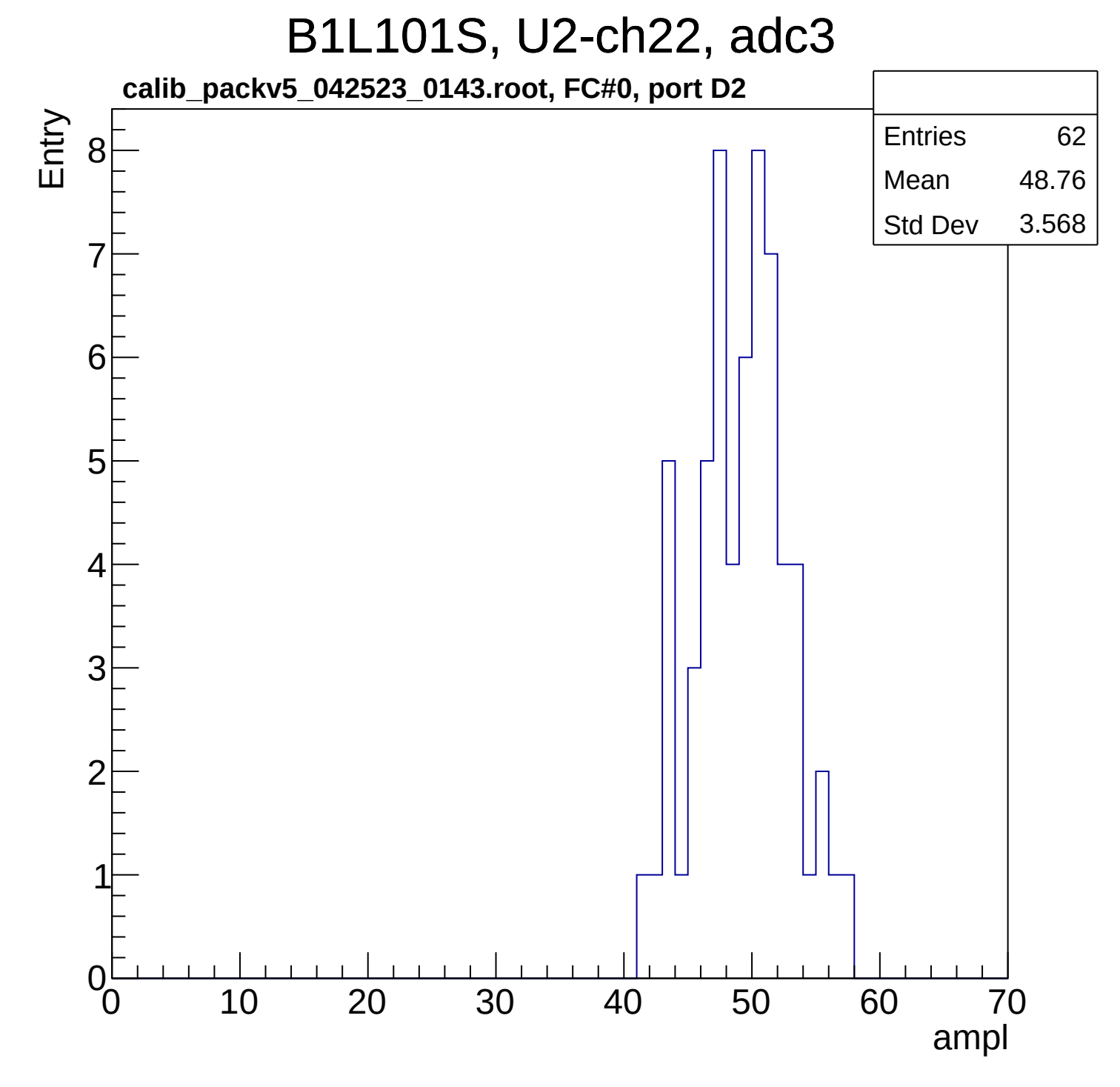

B1L101S, U2-ch21, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 61
Std Dev 1.414
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

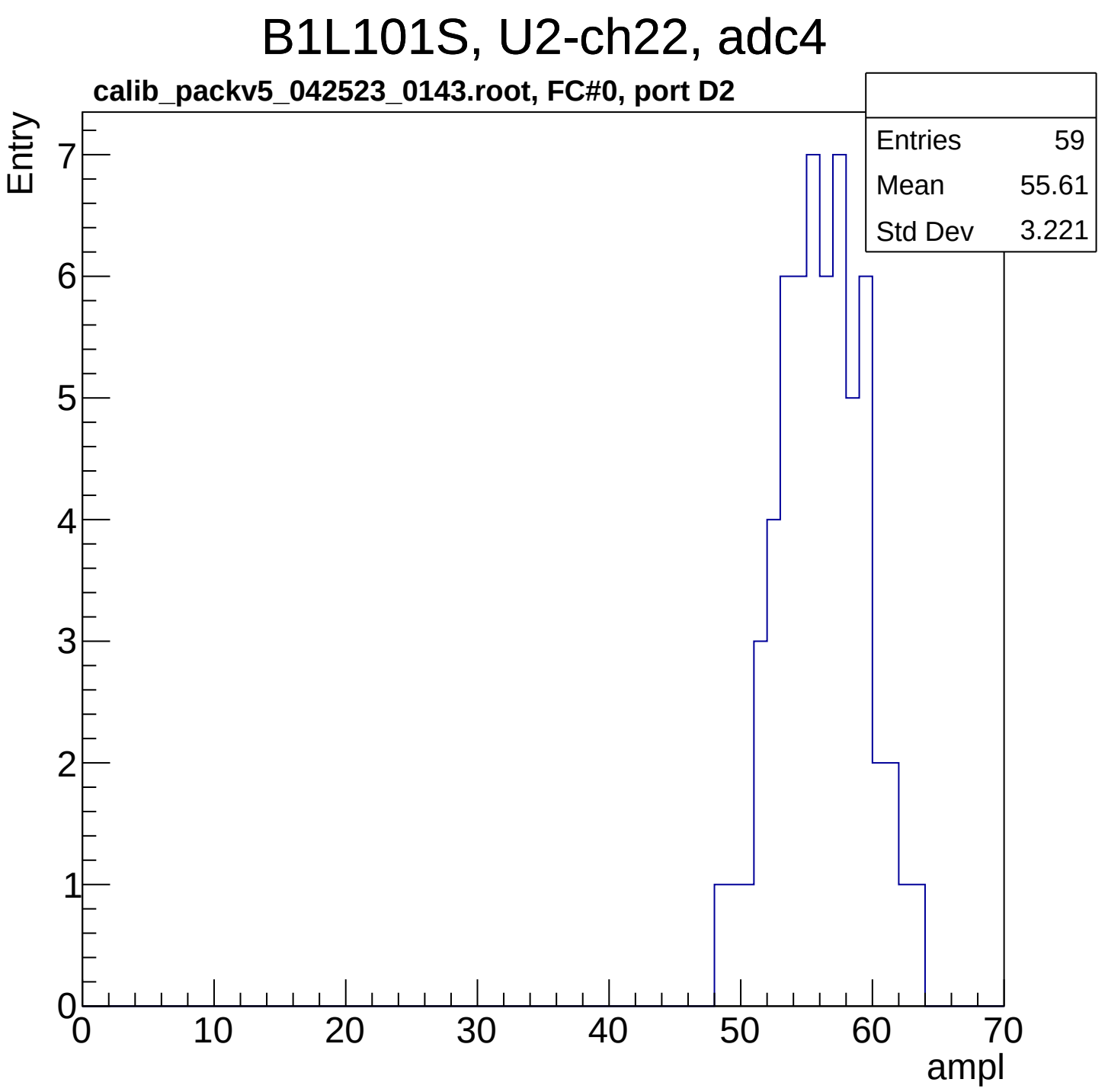

B1L101S, U2-ch21, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

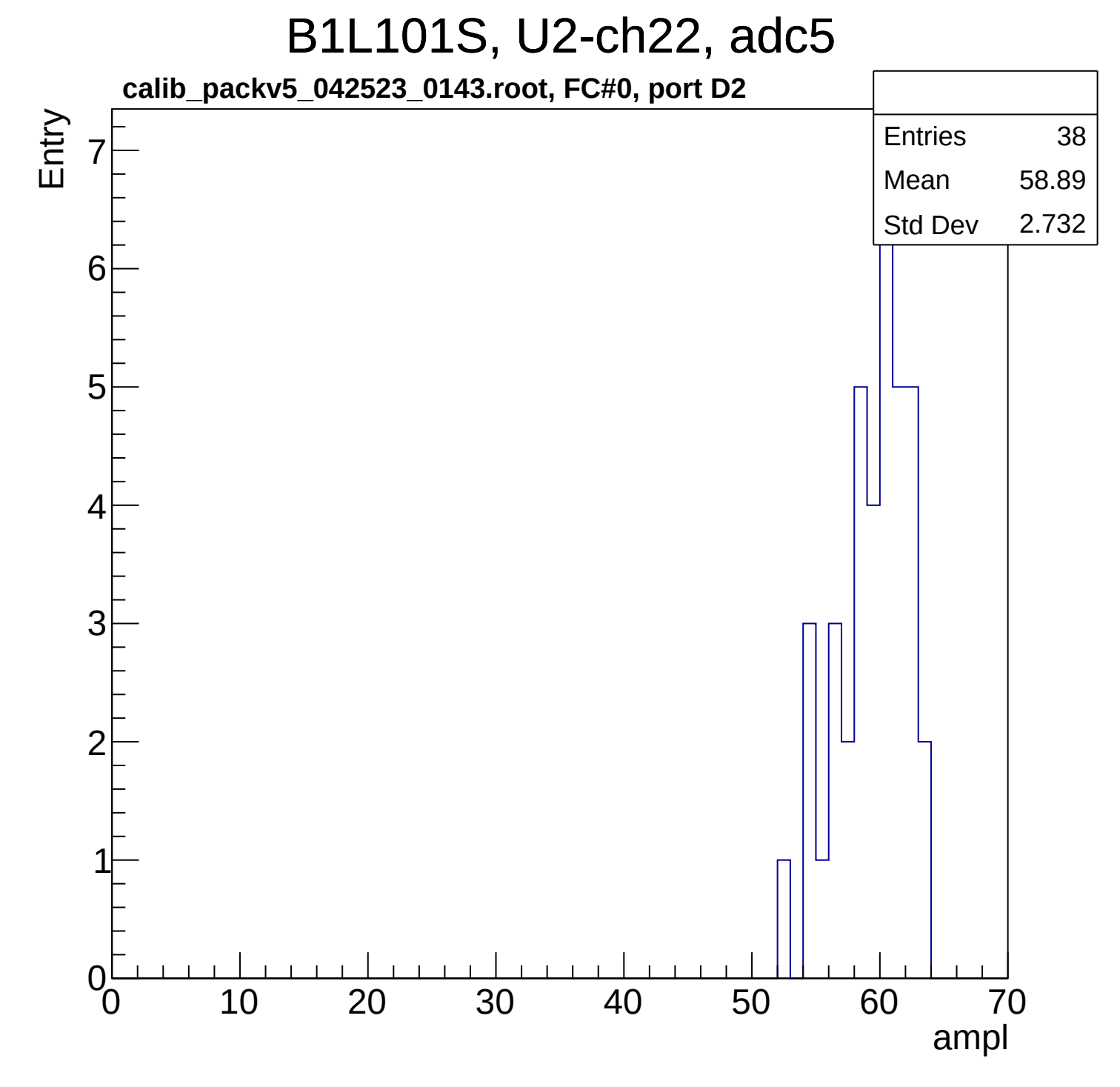

B1L101S, U2-ch22, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 29.49
Std Dev 3.789
Gaus mean : 29.8123
Gaus Width: 4.2526
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

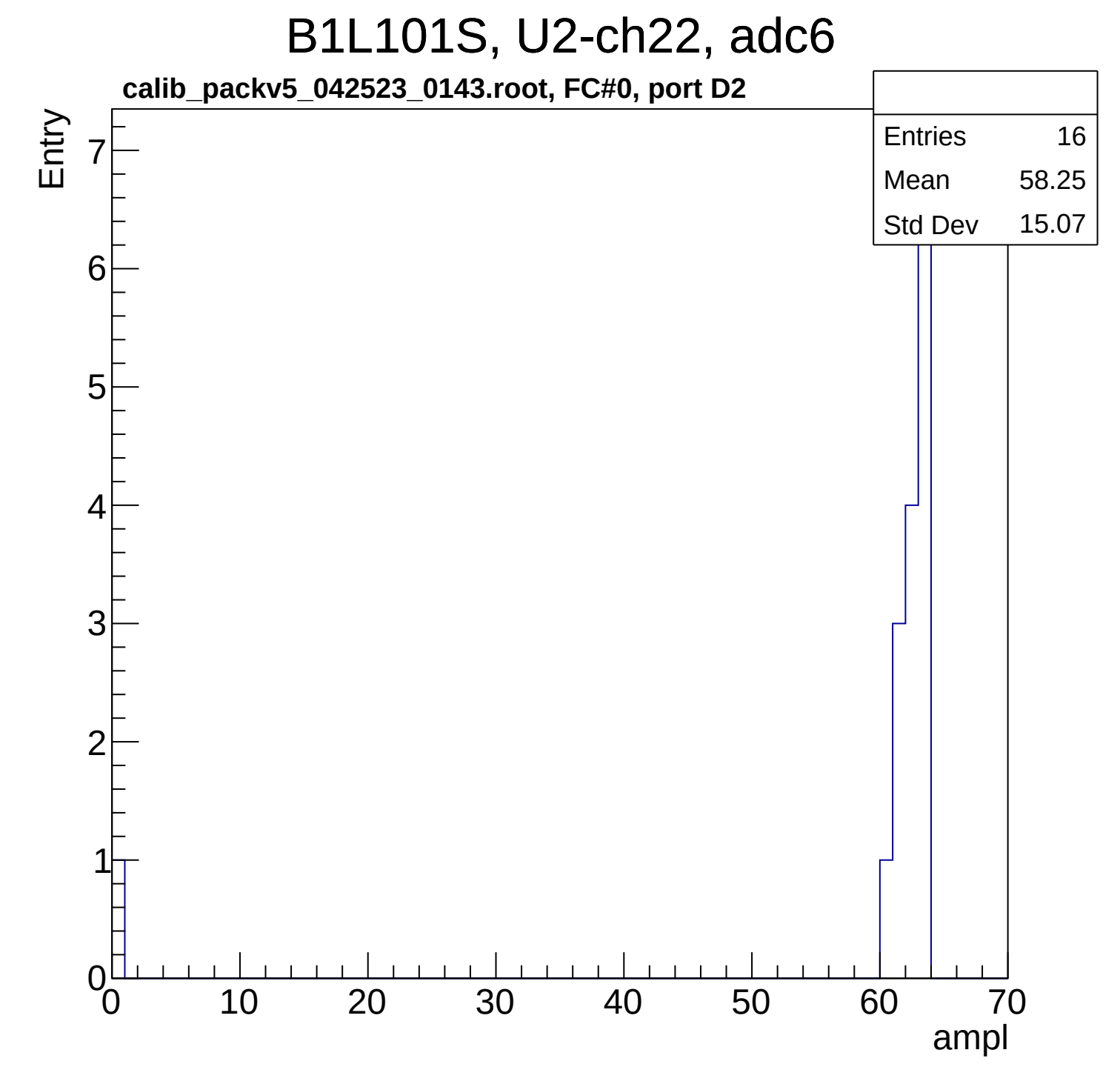

B1L101S, U2-ch22, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 35.77
Std Dev 3.404
Gaus mean : 36.5065
Gaus Width: 3.6442
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

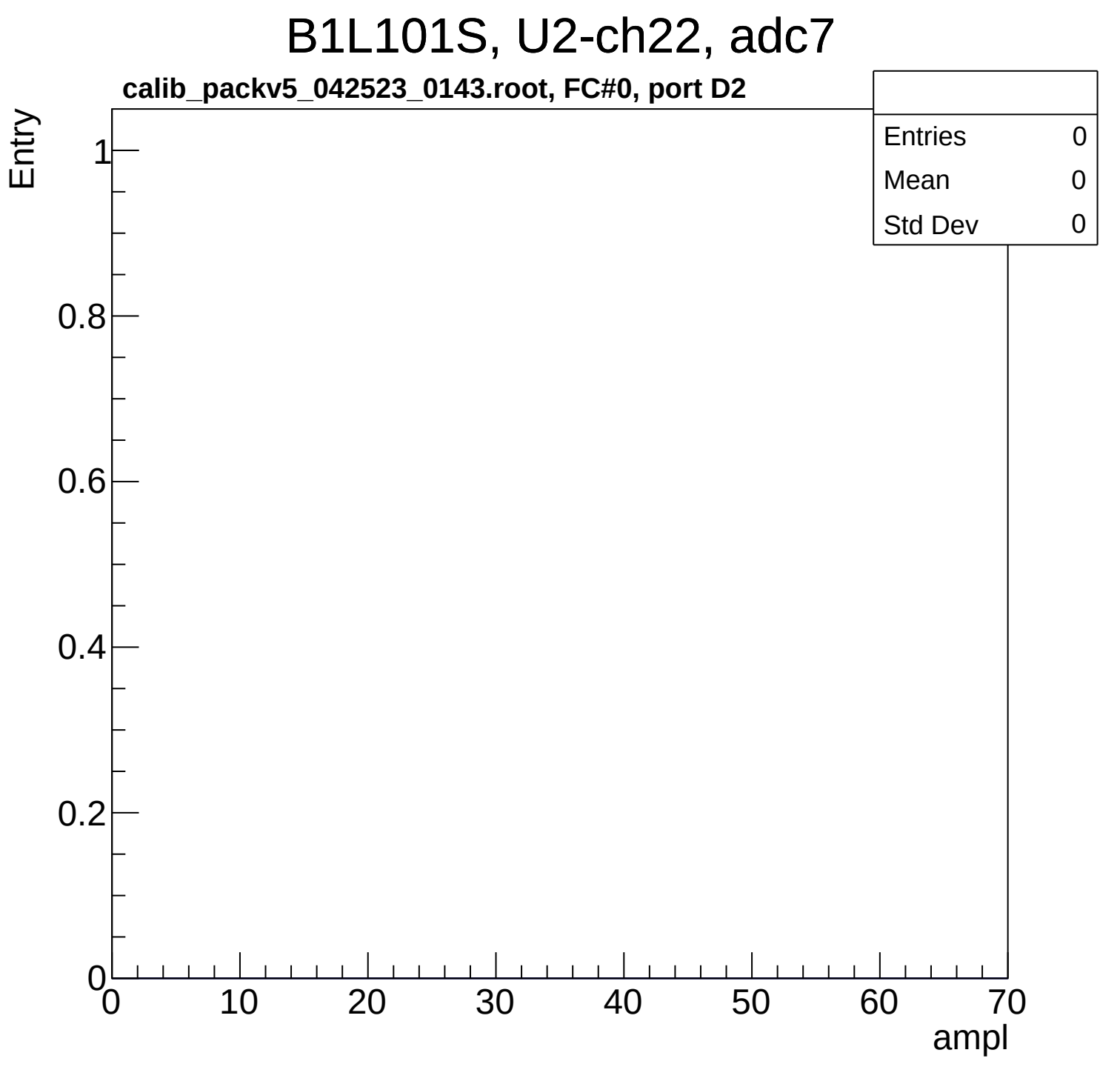

B1L101S, U2-ch22, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 42.96
Std Dev 3.654
Gaus mean : 43.2914
Gaus Width: 4.0204
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

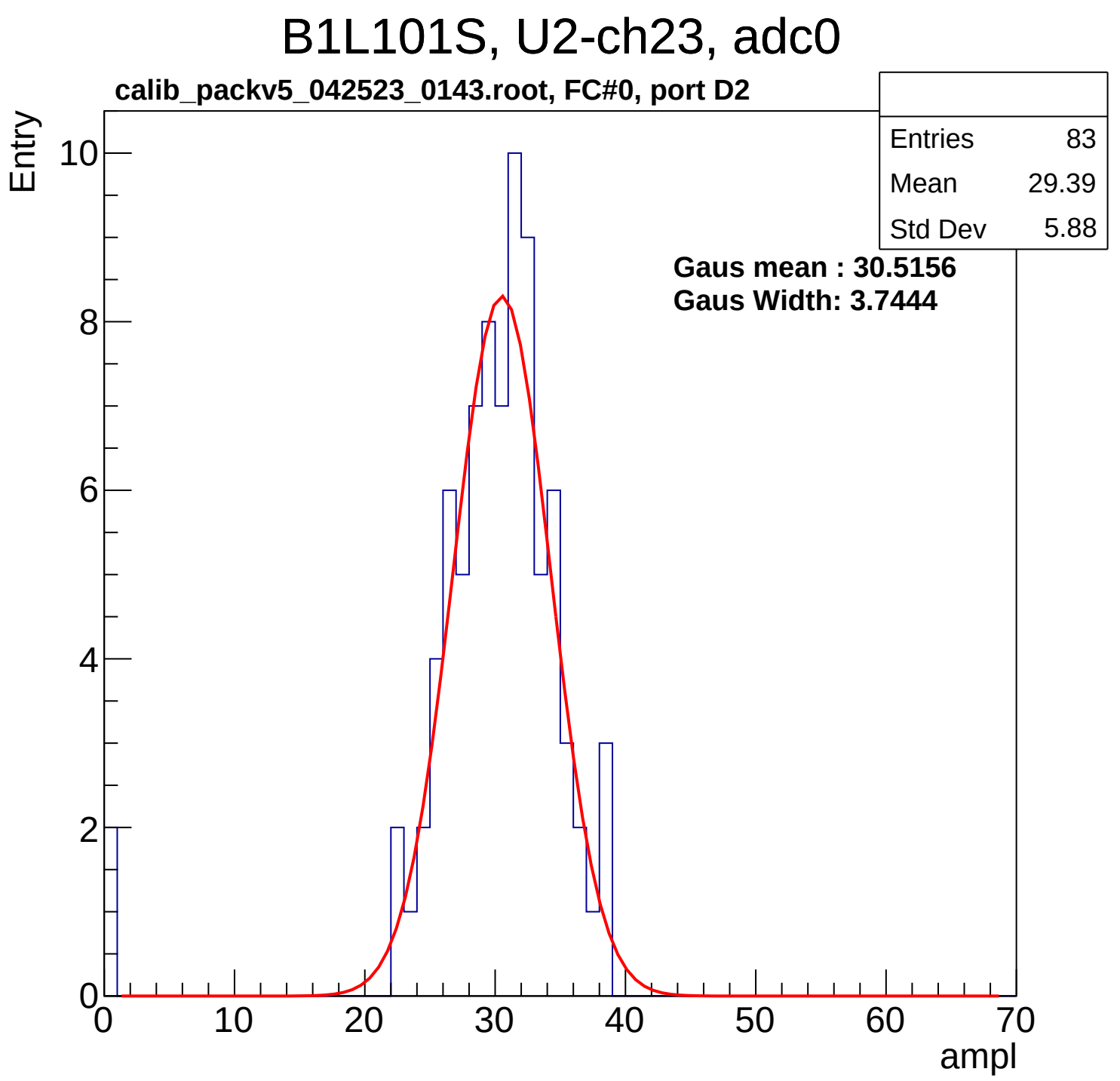

B1L101S, U2-ch22, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 48.76
Std Dev 3.568
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

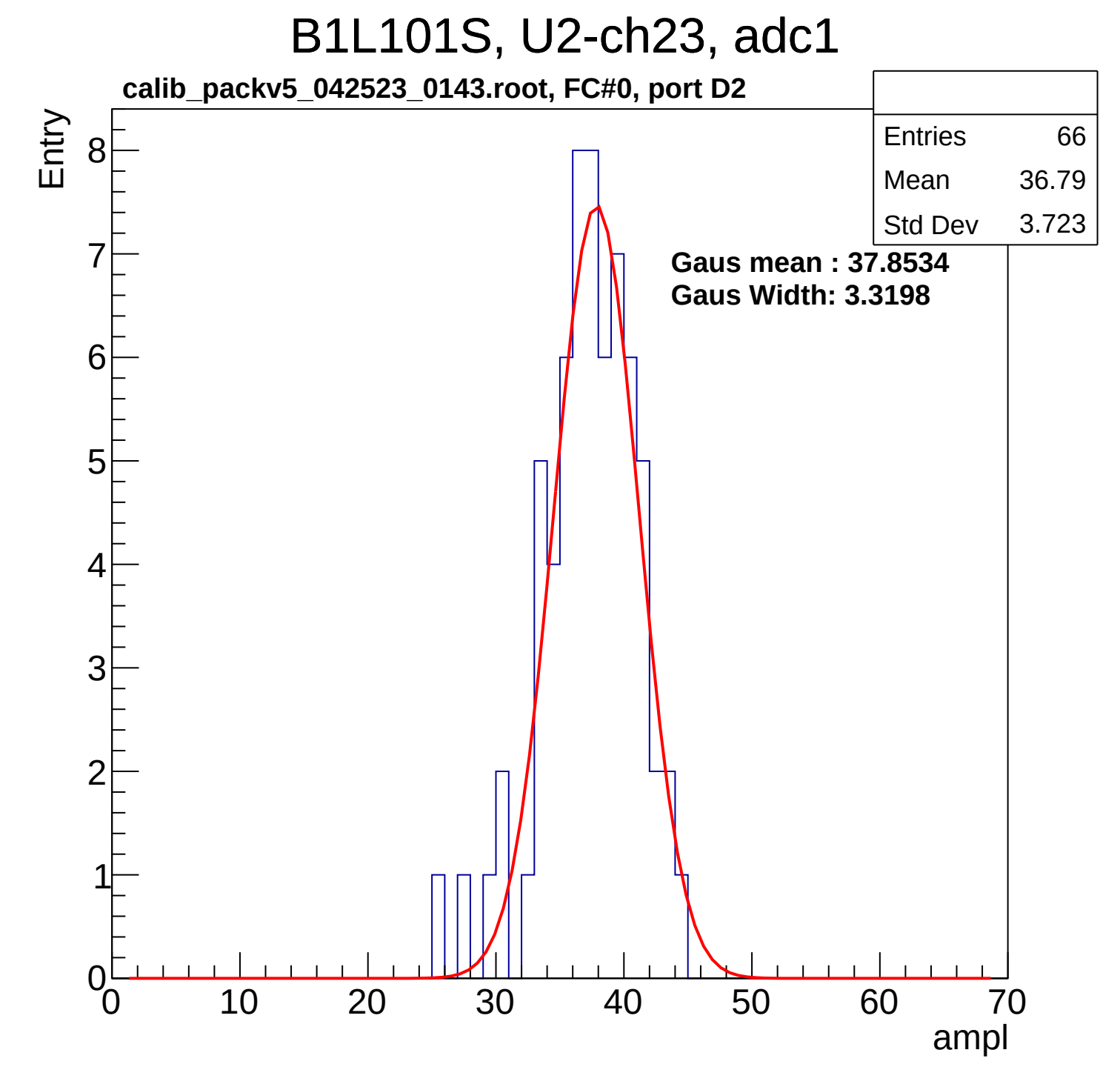

B1L101S, U2-ch22, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 55.61
Std Dev 3.221
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

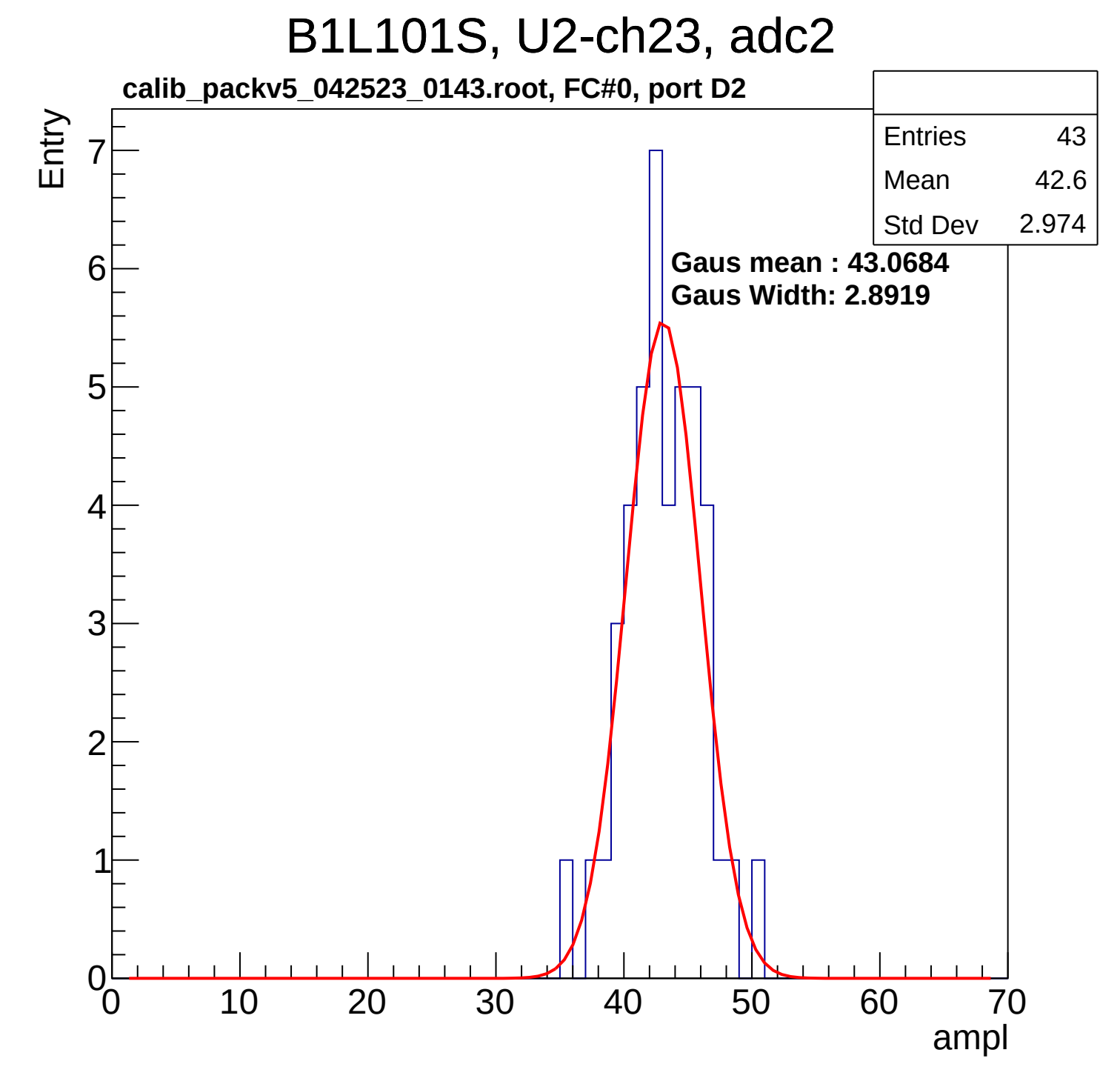

B1L101S, U2-ch22, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 38
Mean 58.89
Std Dev 2.732
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

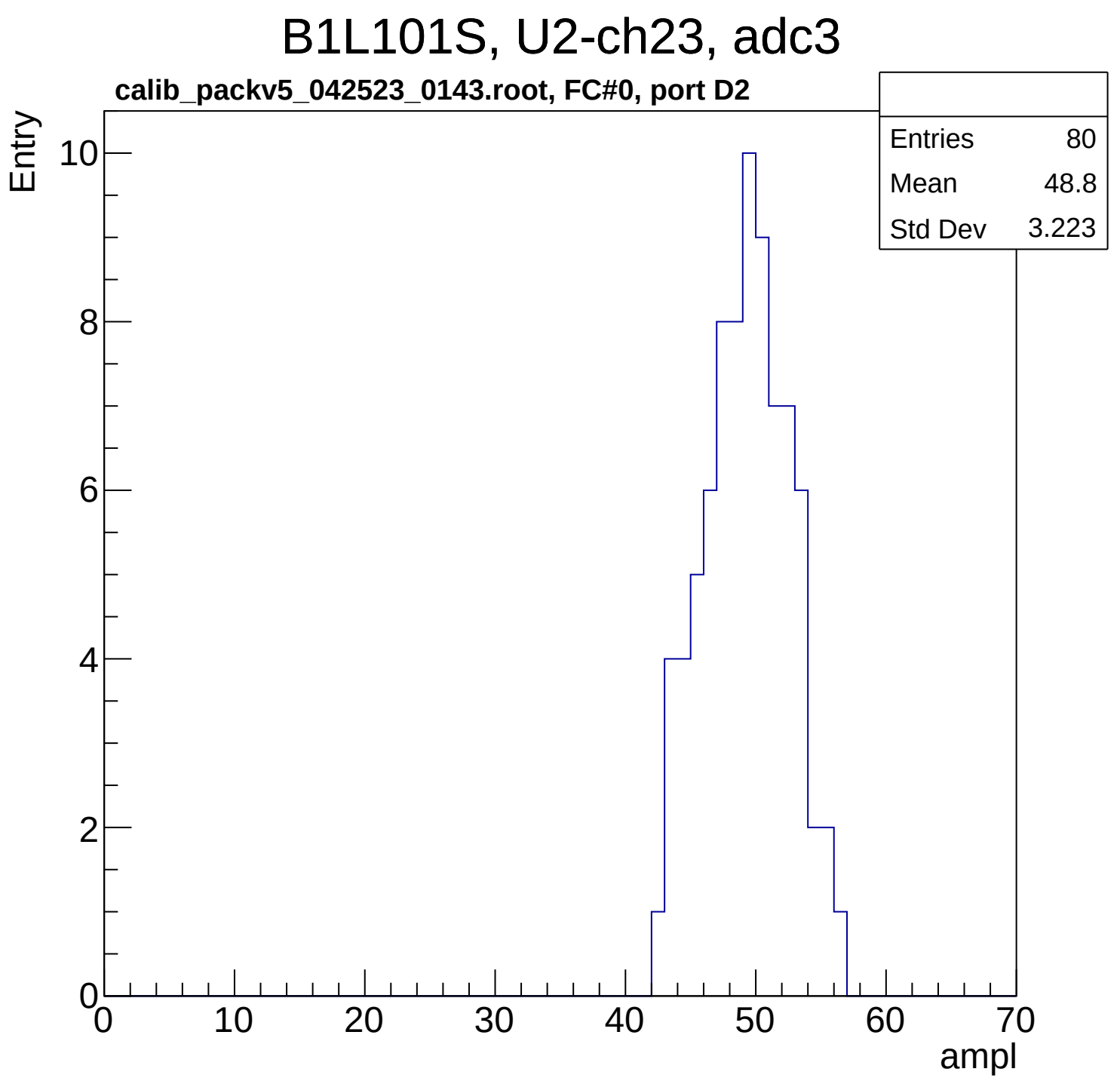

B1L101S, U2-ch22, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 16
Mean 58.25
Std Dev 15.07
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

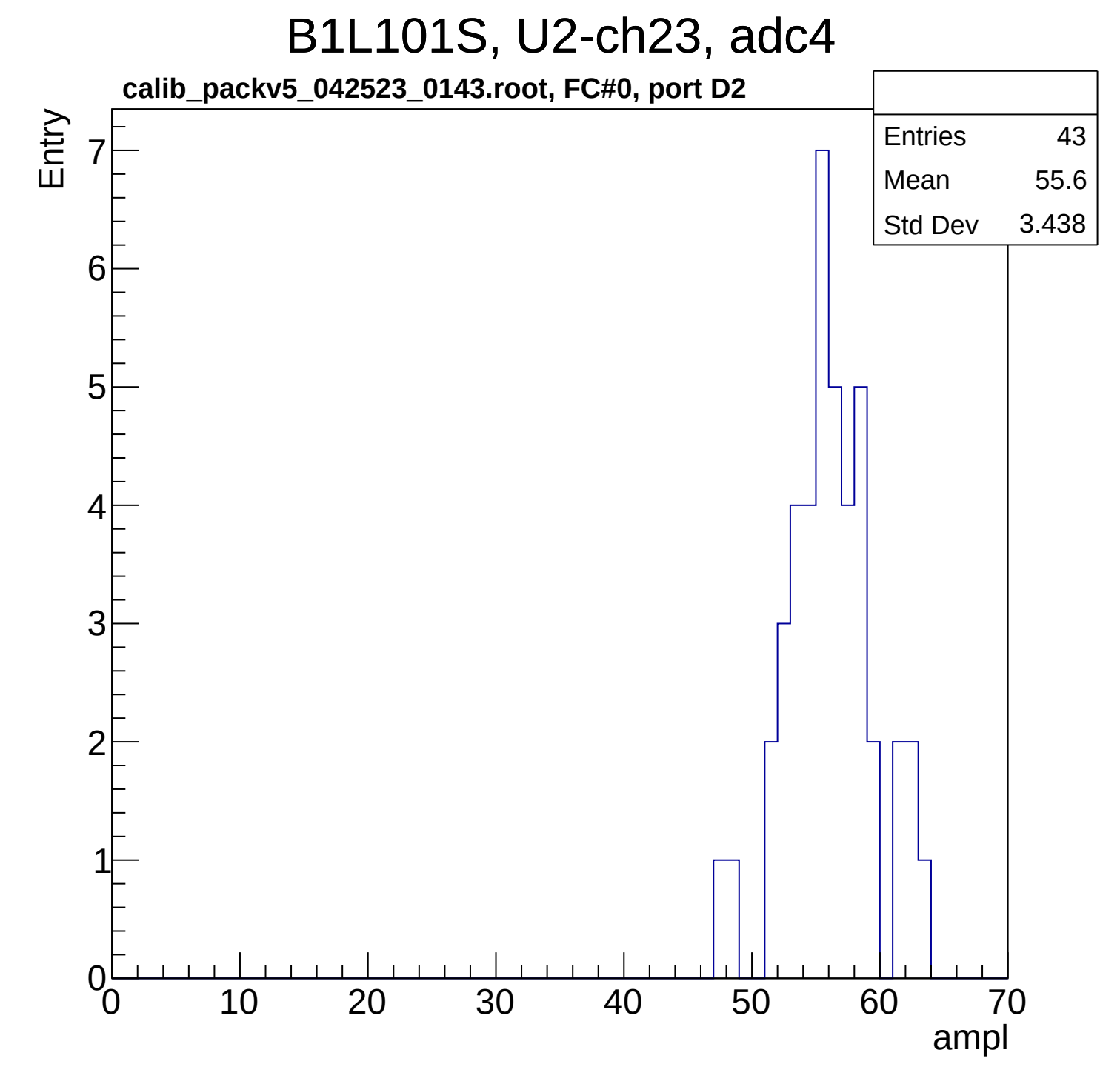

B1L101S, U2-ch22, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

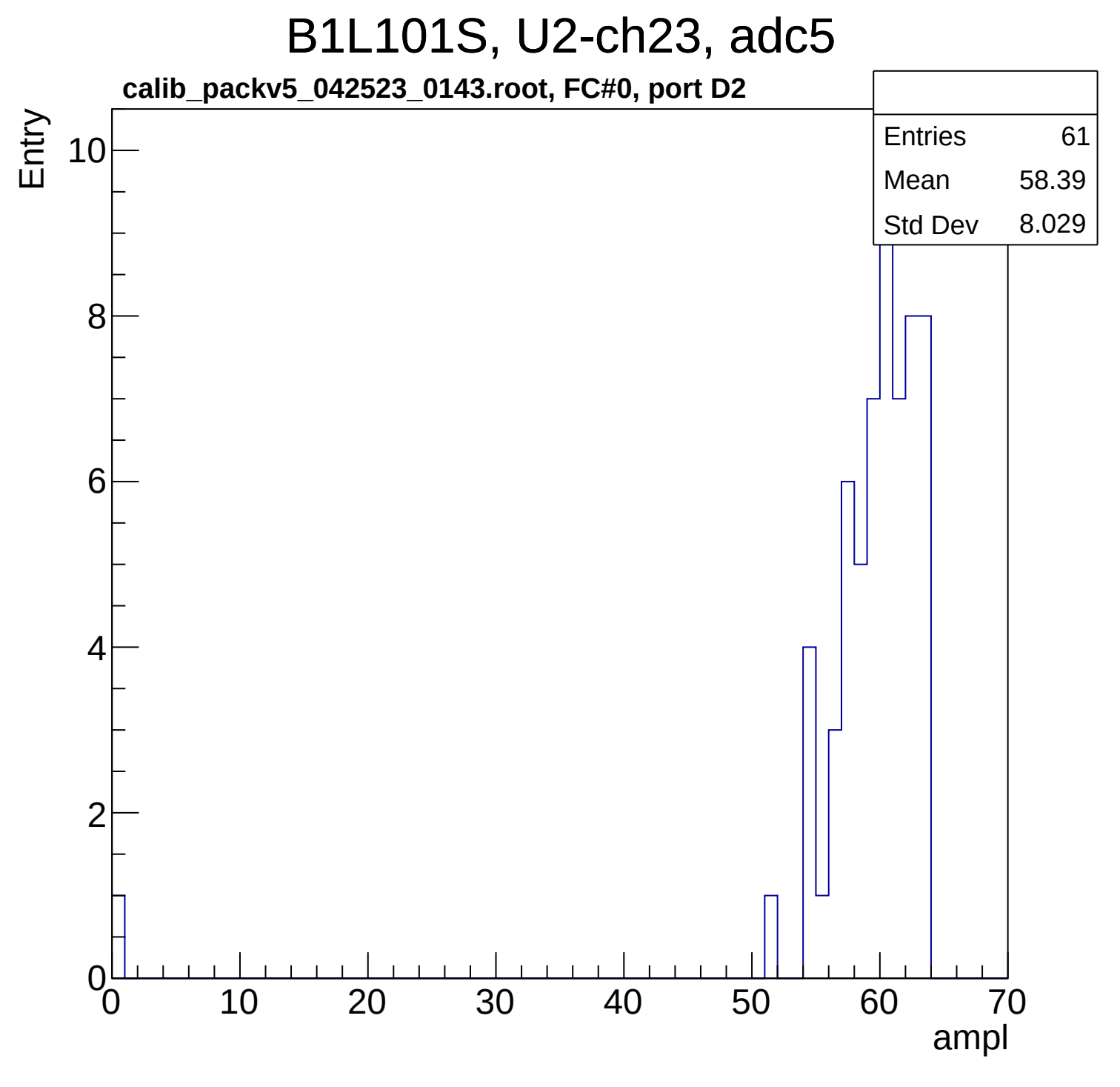

B1L101S, U2-ch23, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 83
Mean 29.39
Std Dev 5.88
Gaus mean : 30.5156
Gaus Width: 3.7444
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

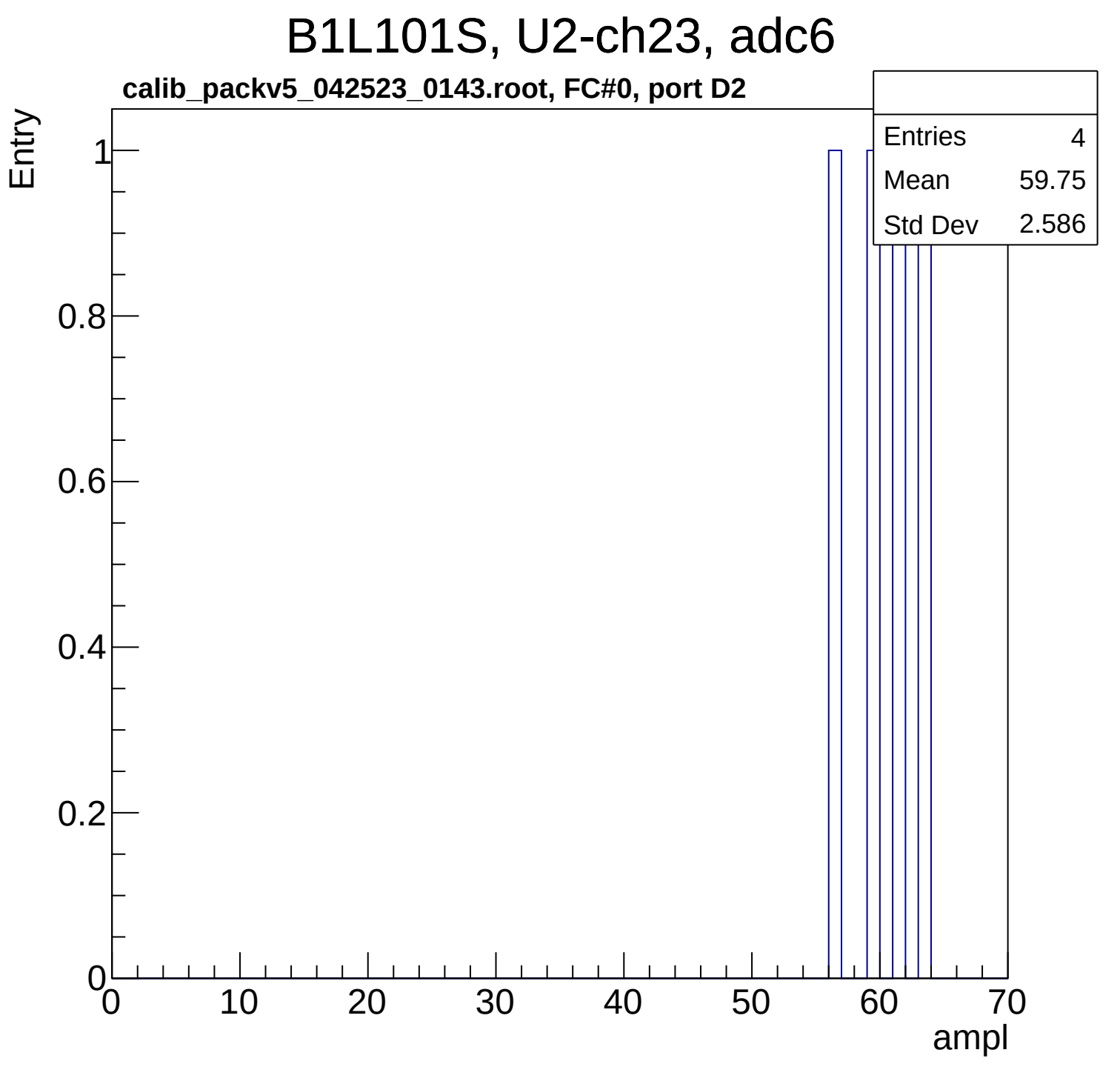

B1L101S, U2-ch23, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 36.79
Std Dev 3.723
Gaus mean : 37.8534
Gaus Width: 3.3198
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

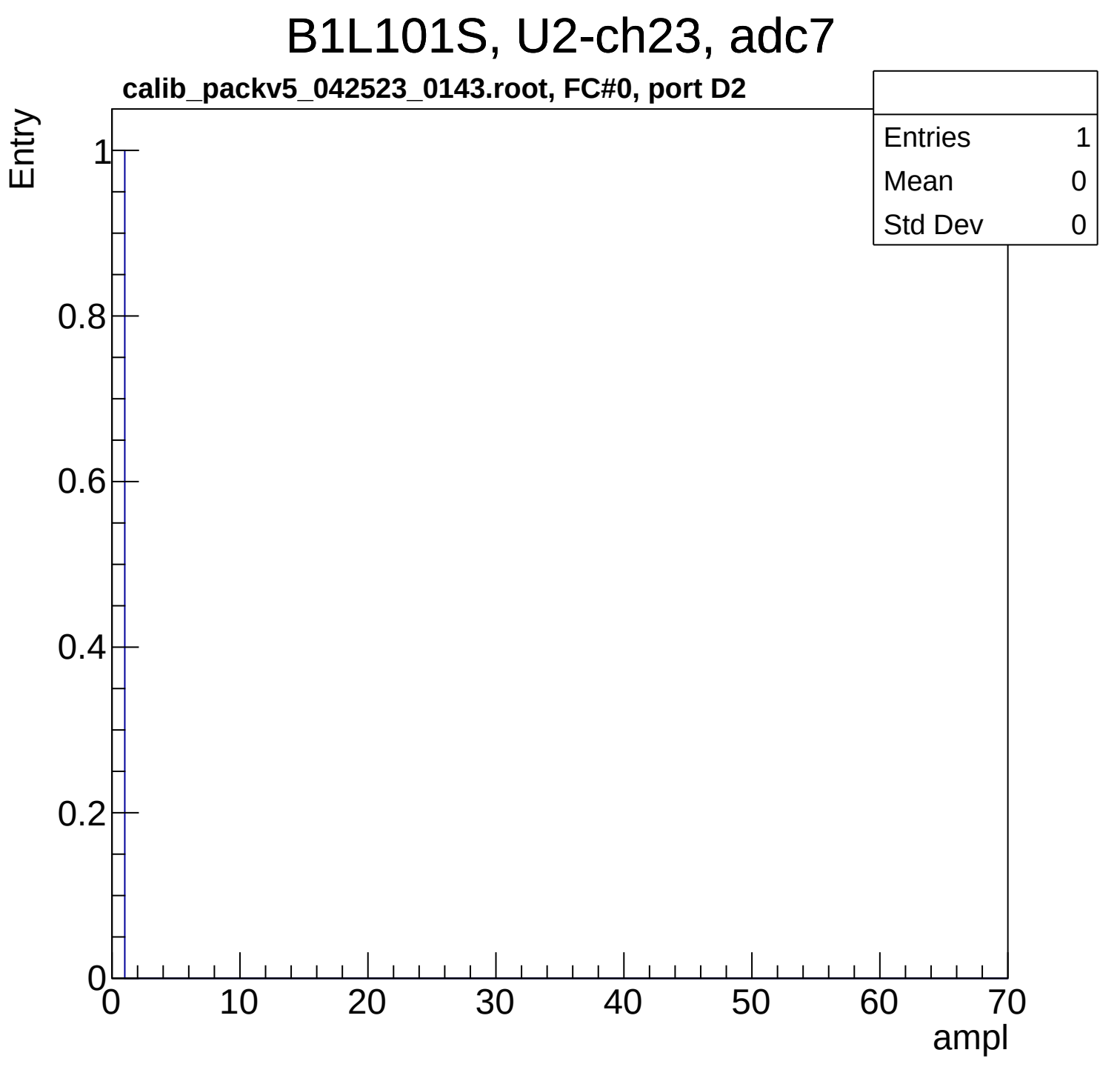

B1L101S, U2-ch23, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 43
Mean 42.6
Std Dev 2.974
Gaus mean : 43.0684
Gaus Width: 2.8919
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

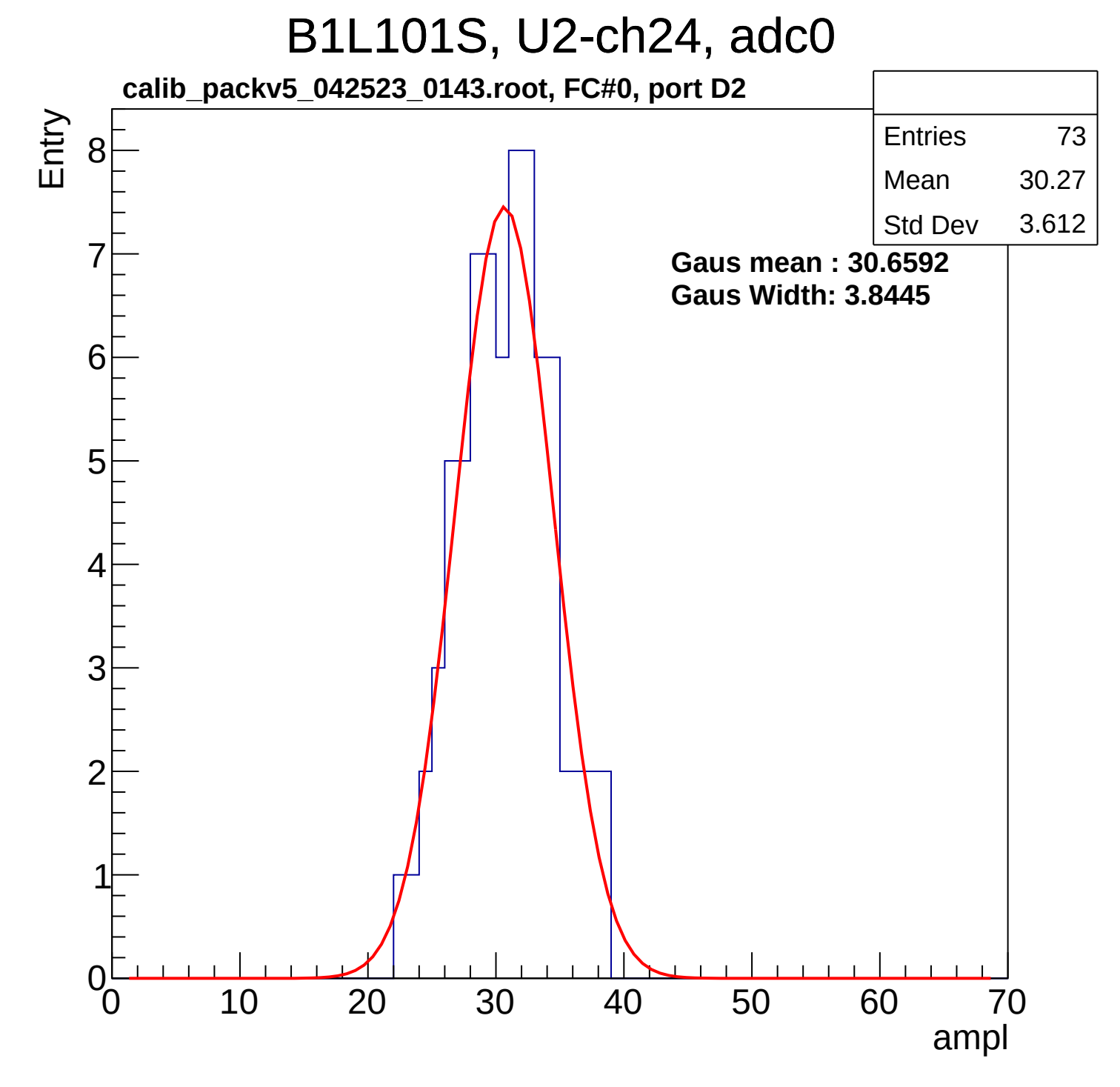

B1L101S, U2-ch23, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 80
Mean 48.8
Std Dev 3.223
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

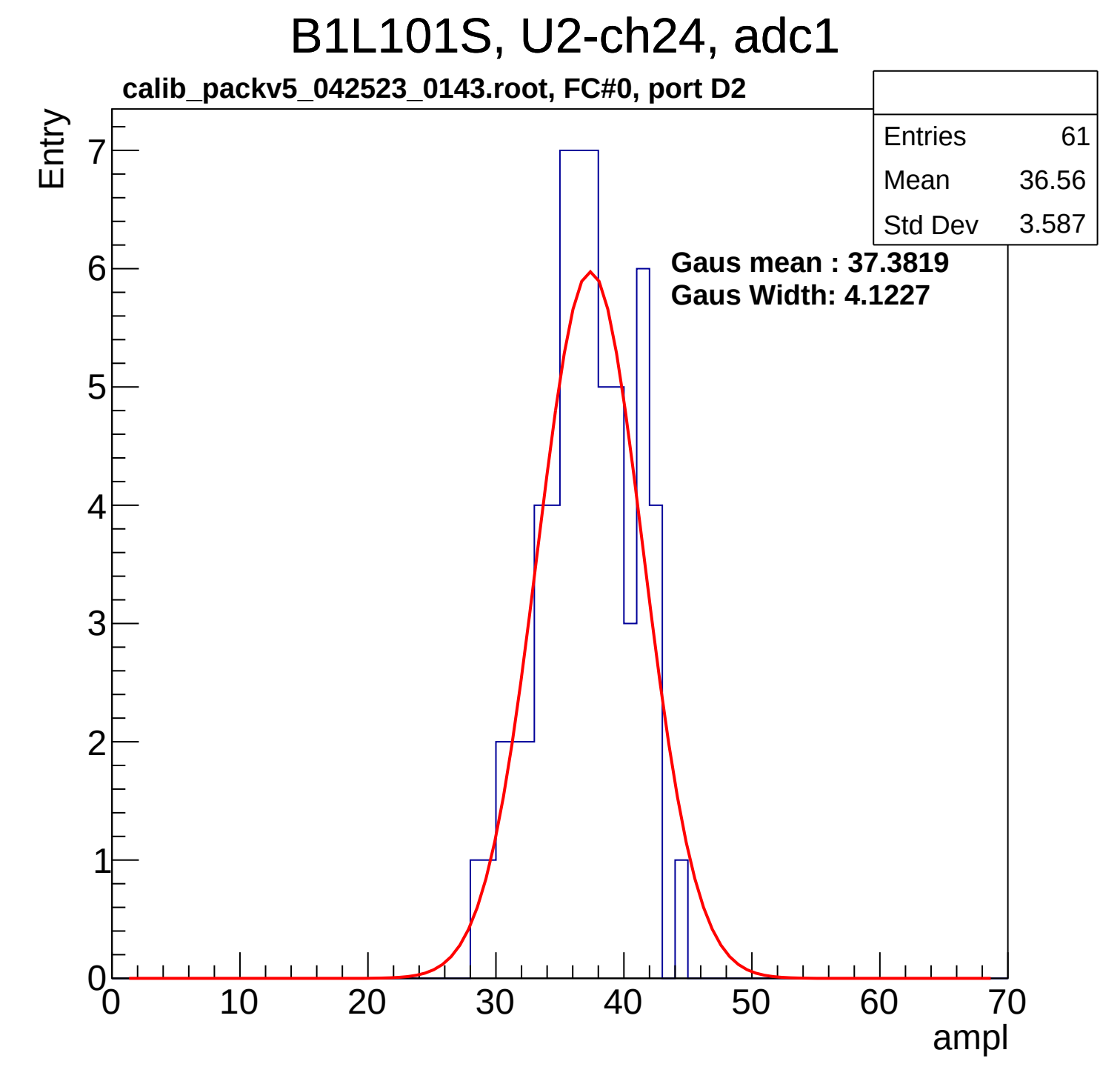

B1L101S, U2-ch23, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 43
Mean 55.6
Std Dev 3.438
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

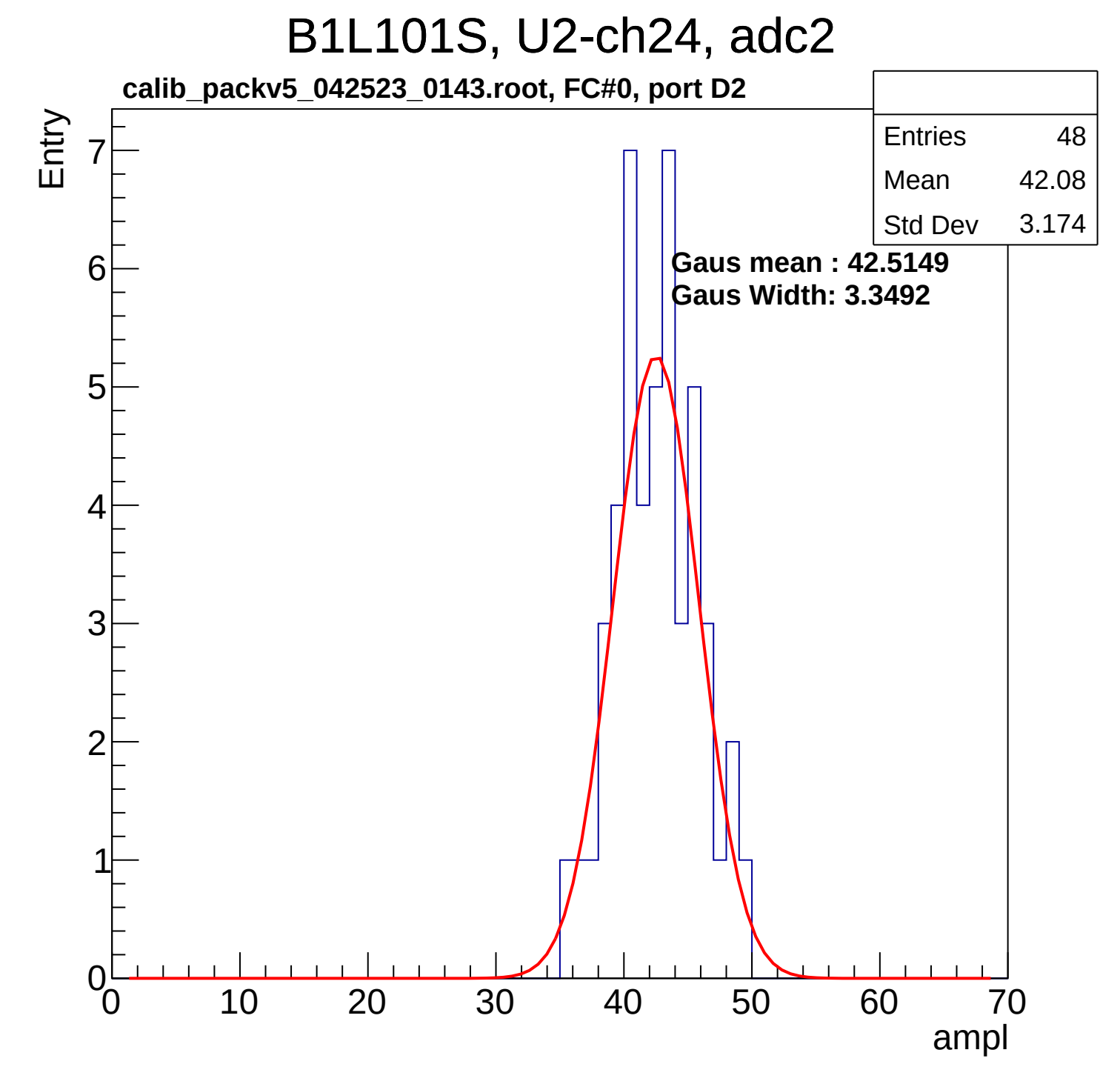

B1L101S, U2-ch23, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 58.39
Std Dev 8.029
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

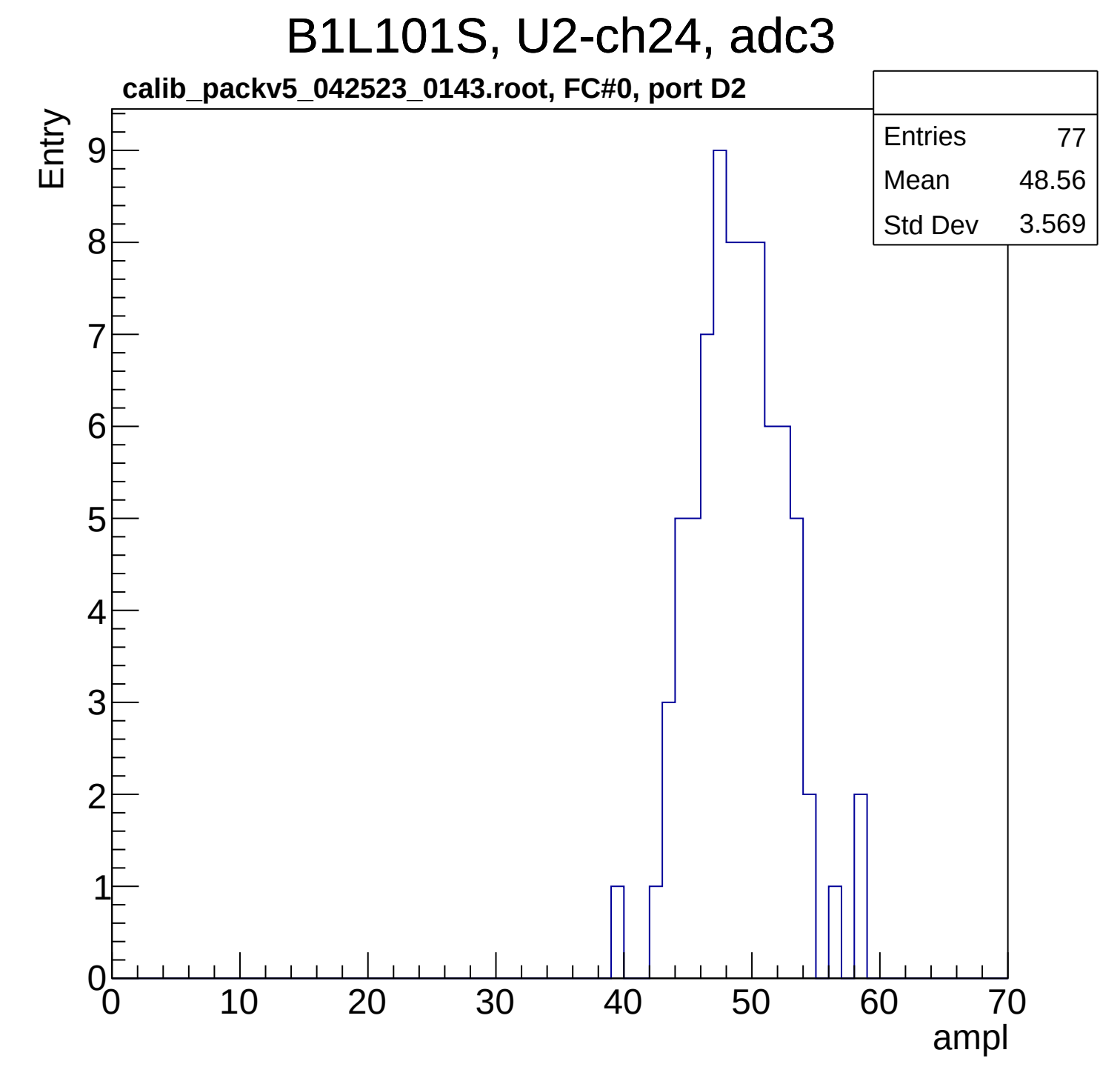

B1L101S, U2-ch23, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 59.75
Std Dev 2.586
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

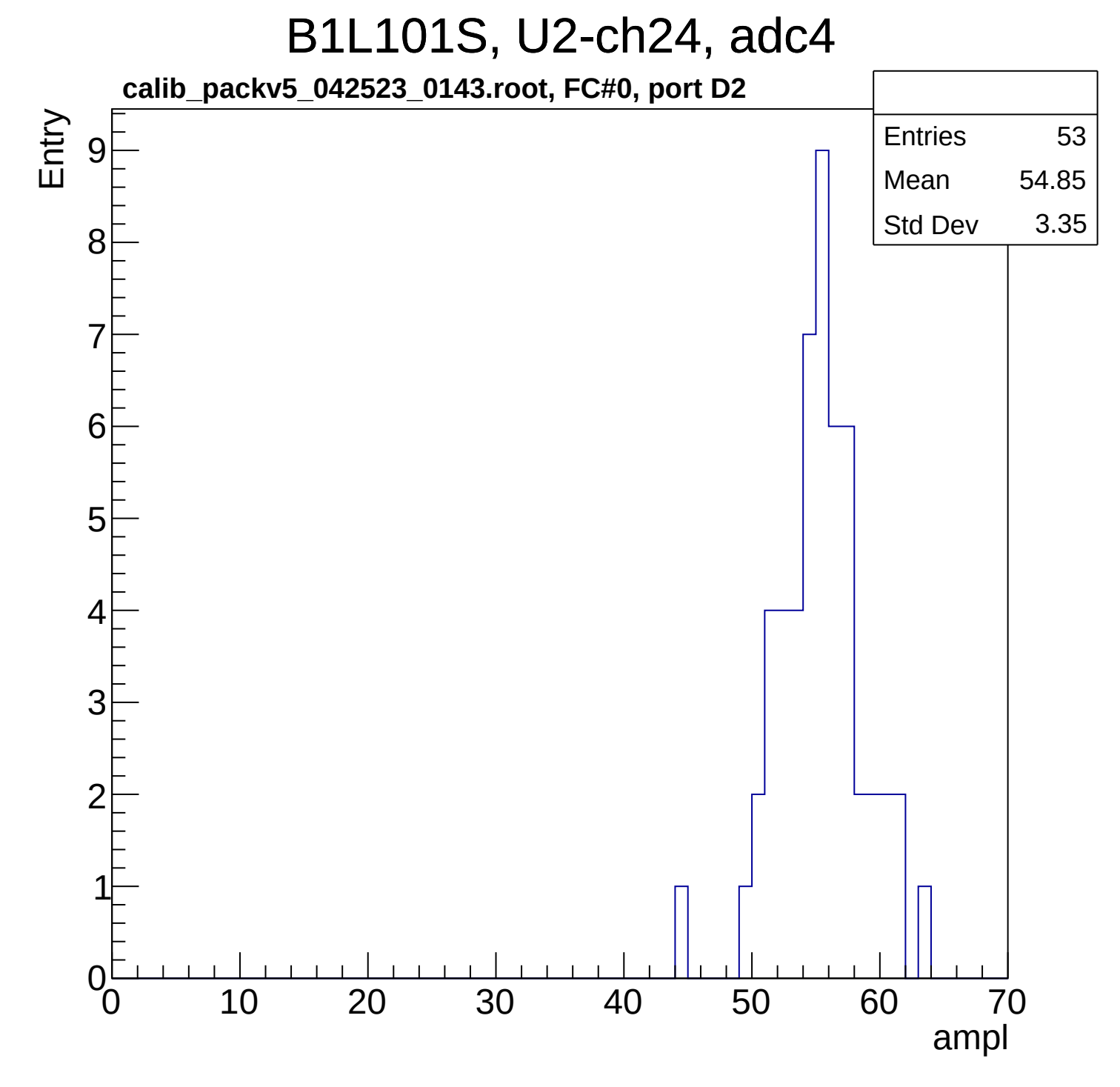

B1L101S, U2-ch23, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

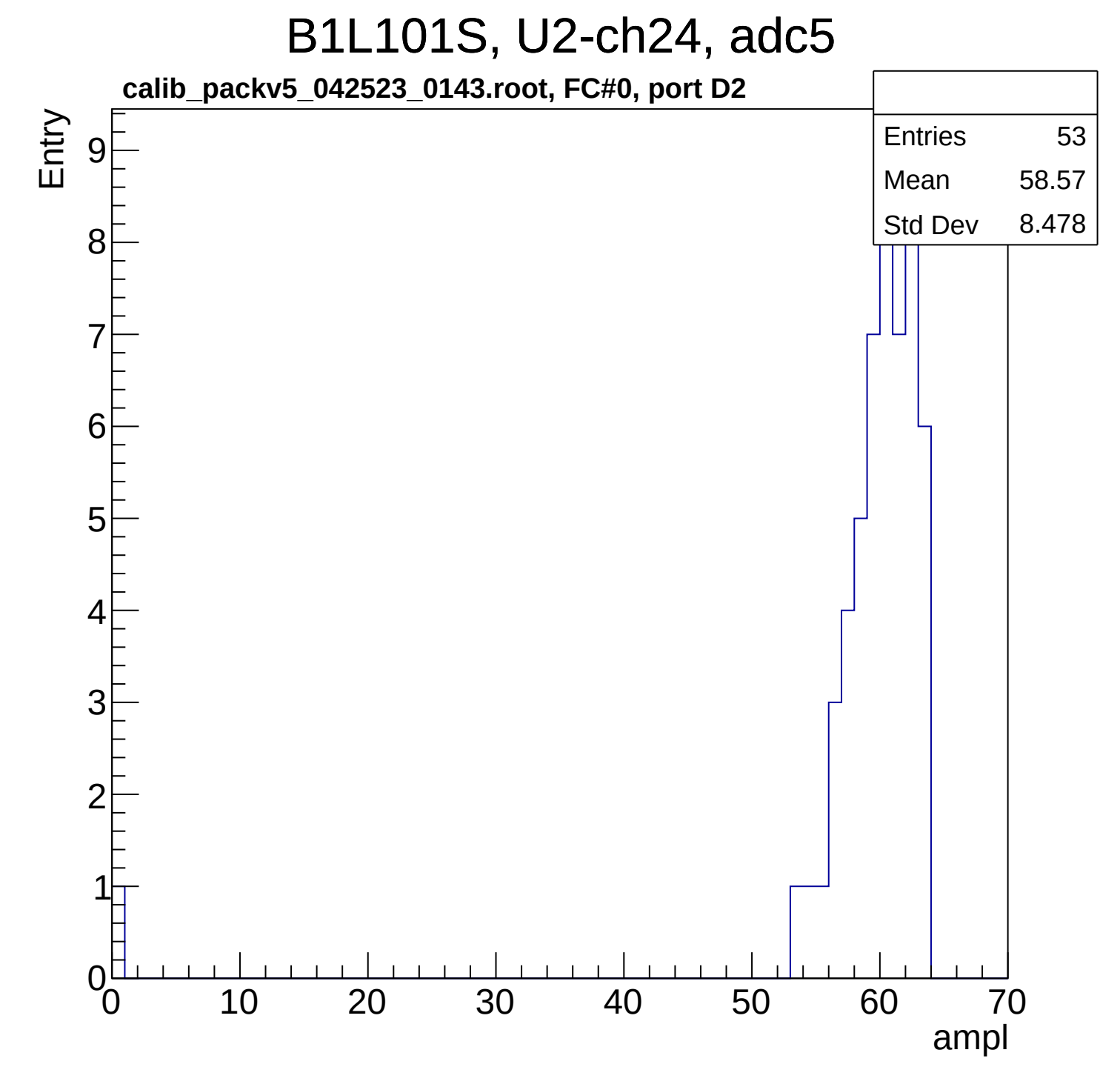

B1L101S, U2-ch24, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 30.27
Std Dev 3.612
Gaus mean : 30.6592
Gaus Width: 3.8445
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

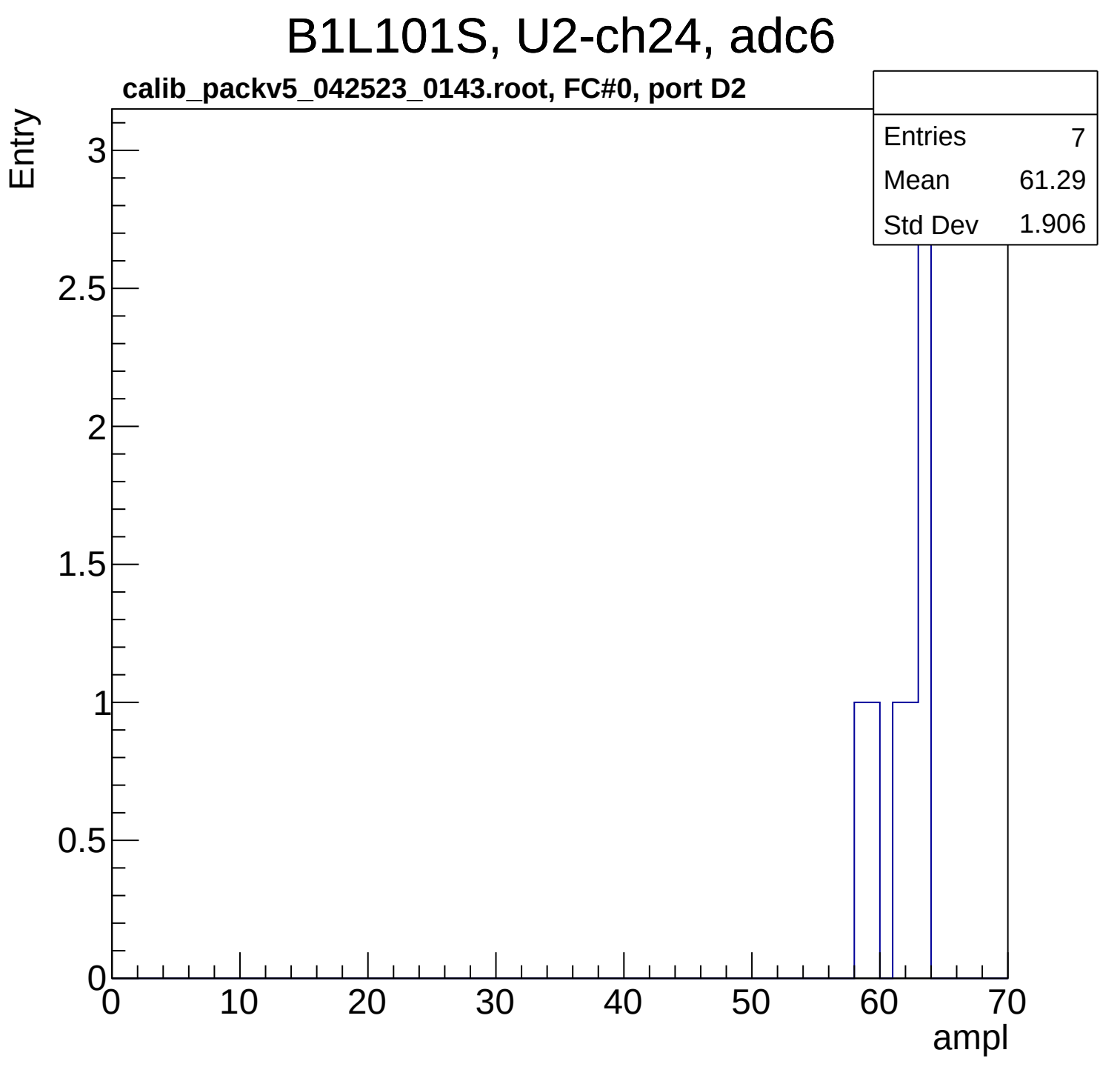

B1L101S, U2-ch24, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 36.56
Std Dev 3.587
Gaus mean : 37.3819
Gaus Width: 4.1227
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

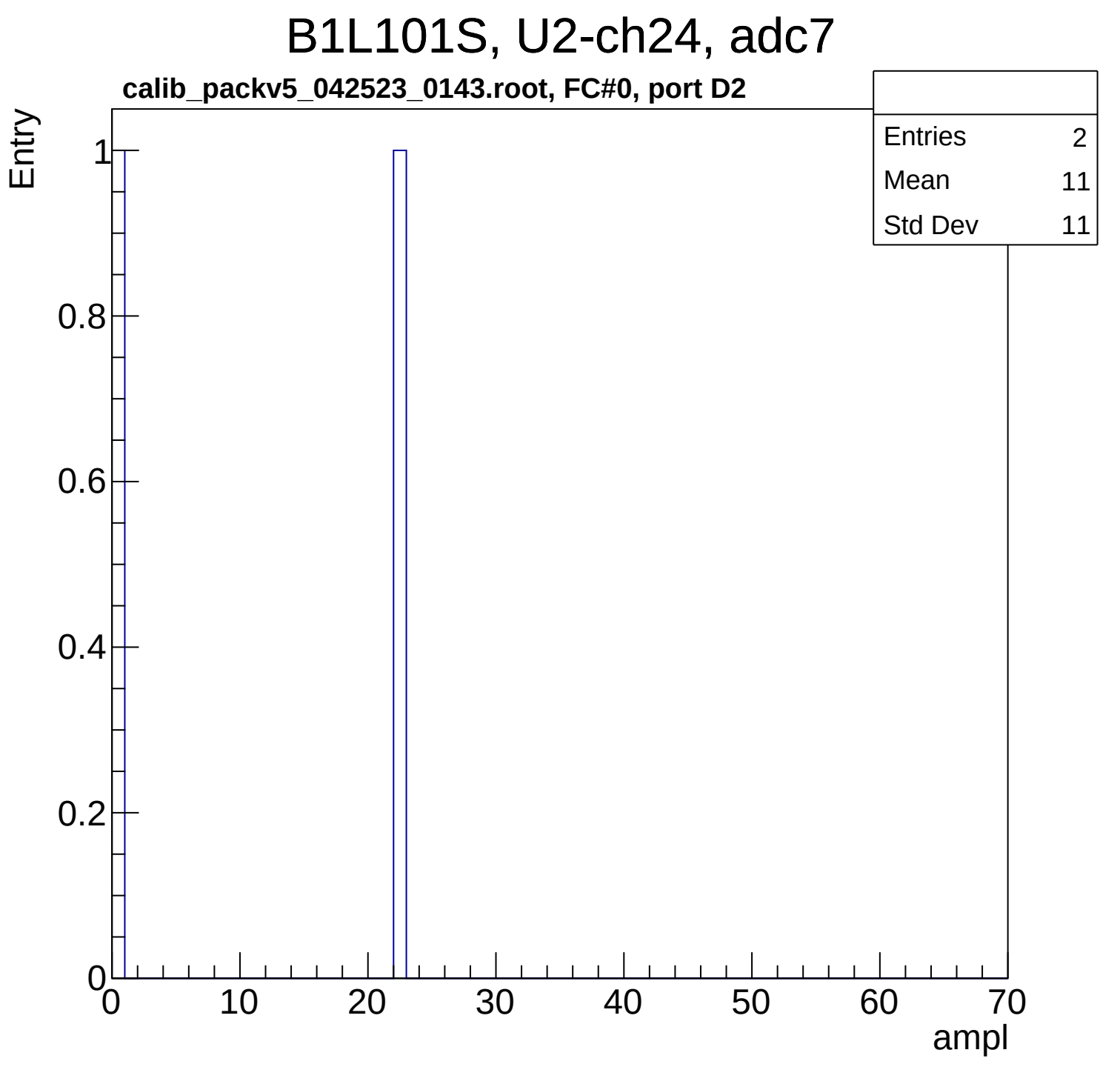

B1L101S, U2-ch24, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 42.08
Std Dev 3.174
Gaus mean : 42.5149
Gaus Width: 3.3492
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

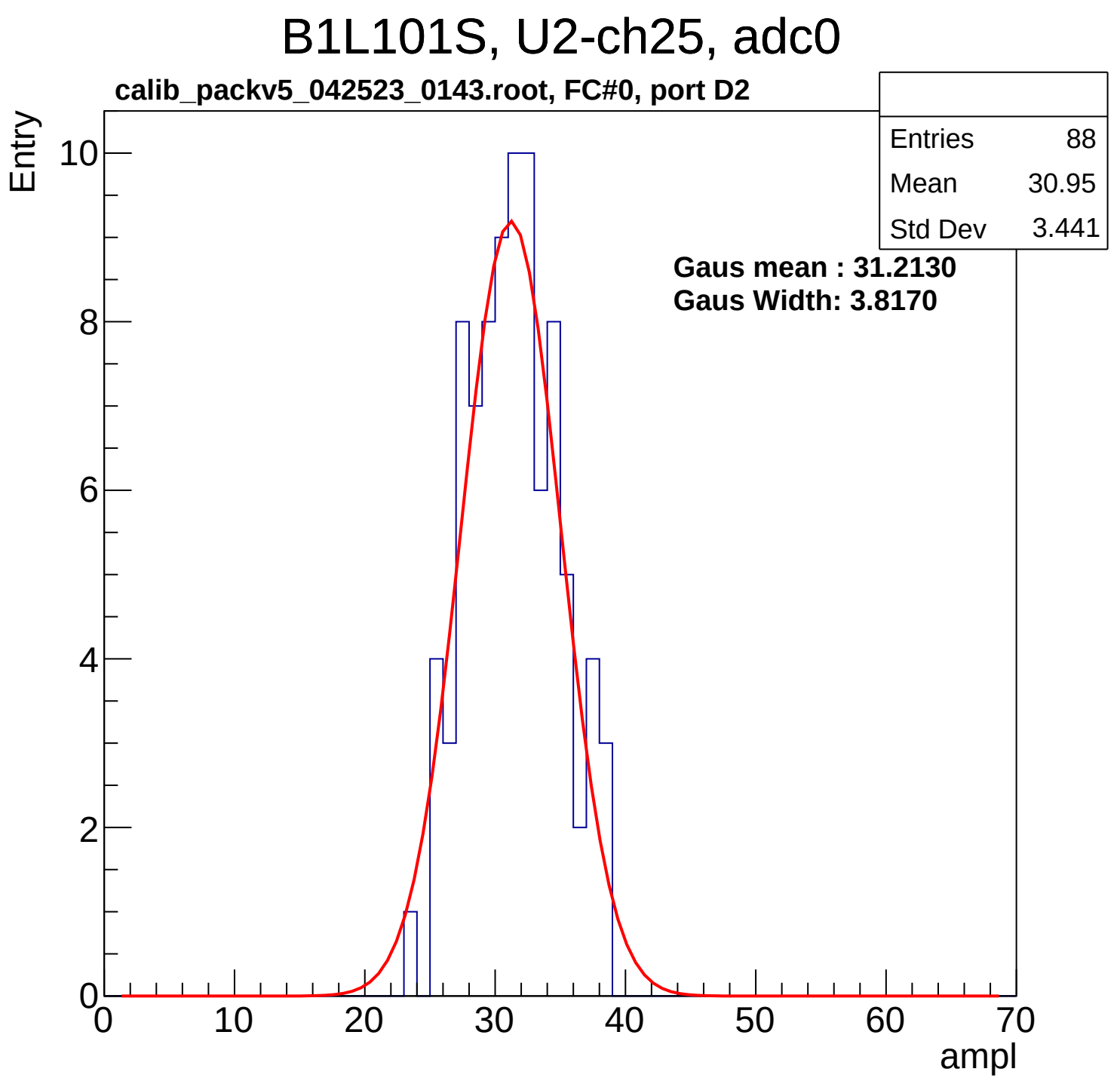

B1L101S, U2-ch24, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 48.56
Std Dev 3.569
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

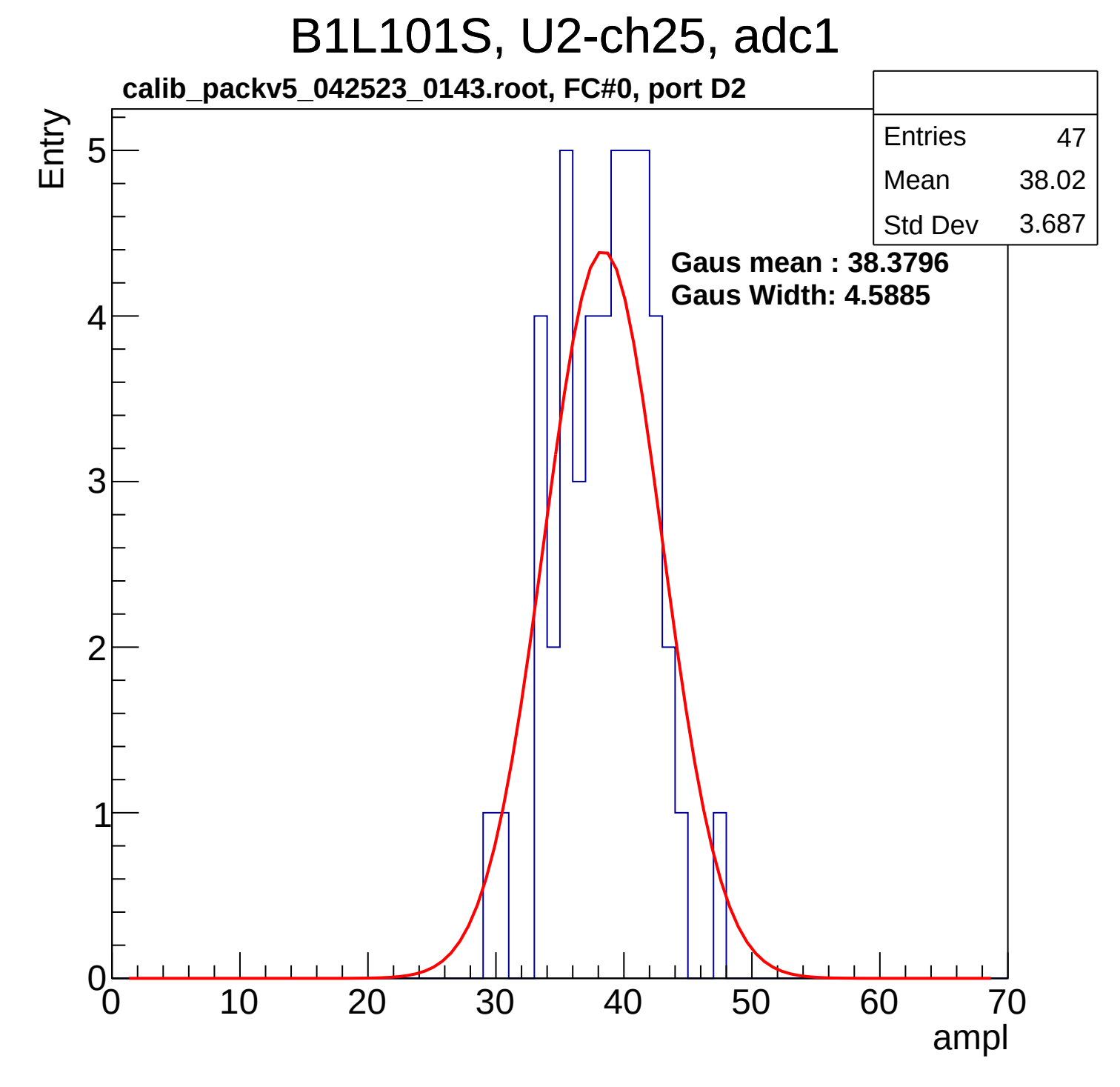

B1L101S, U2-ch24, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 54.85
Std Dev 3.35
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

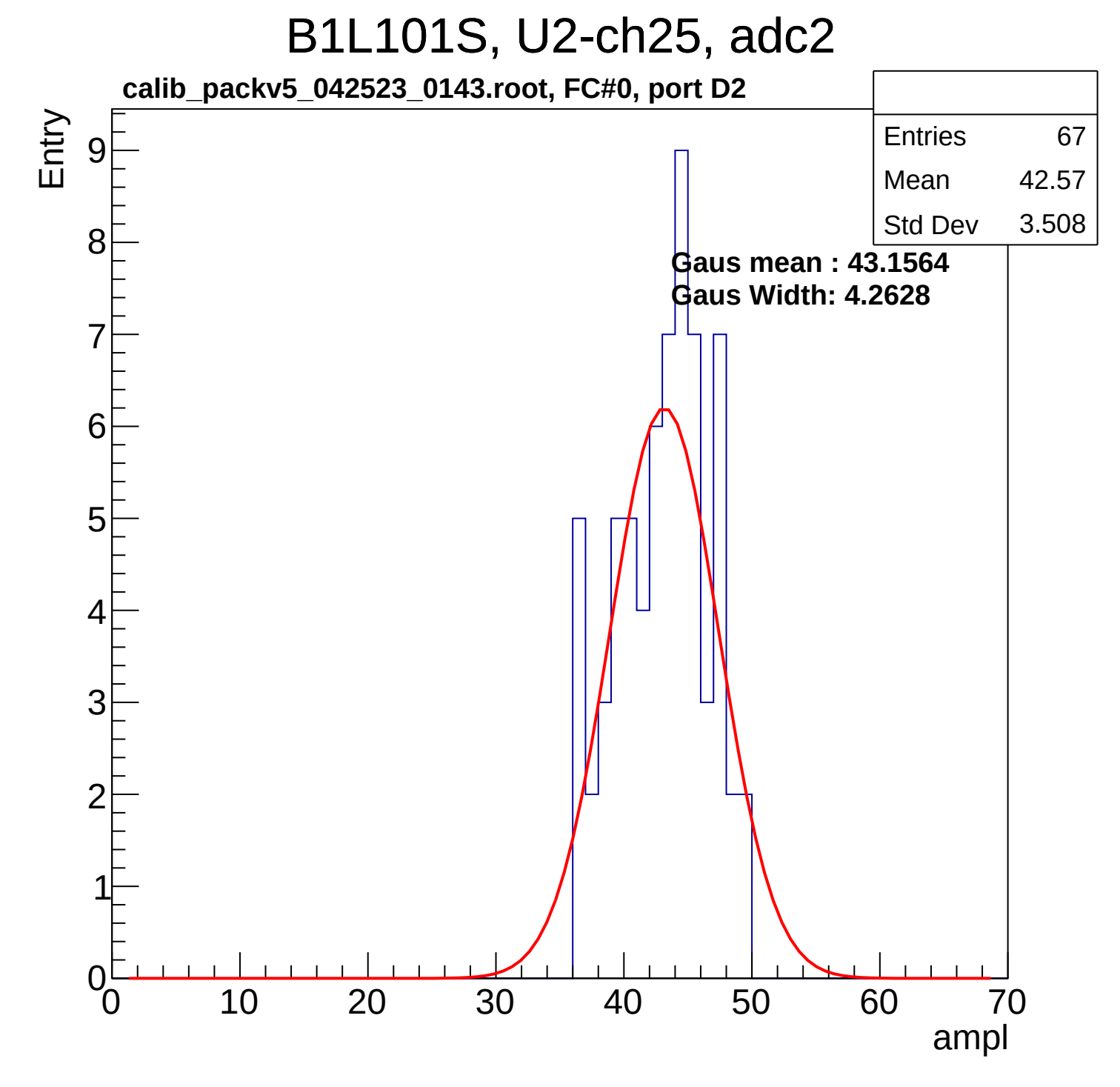

B1L101S, U2-ch24, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 58.57
Std Dev 8.478
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

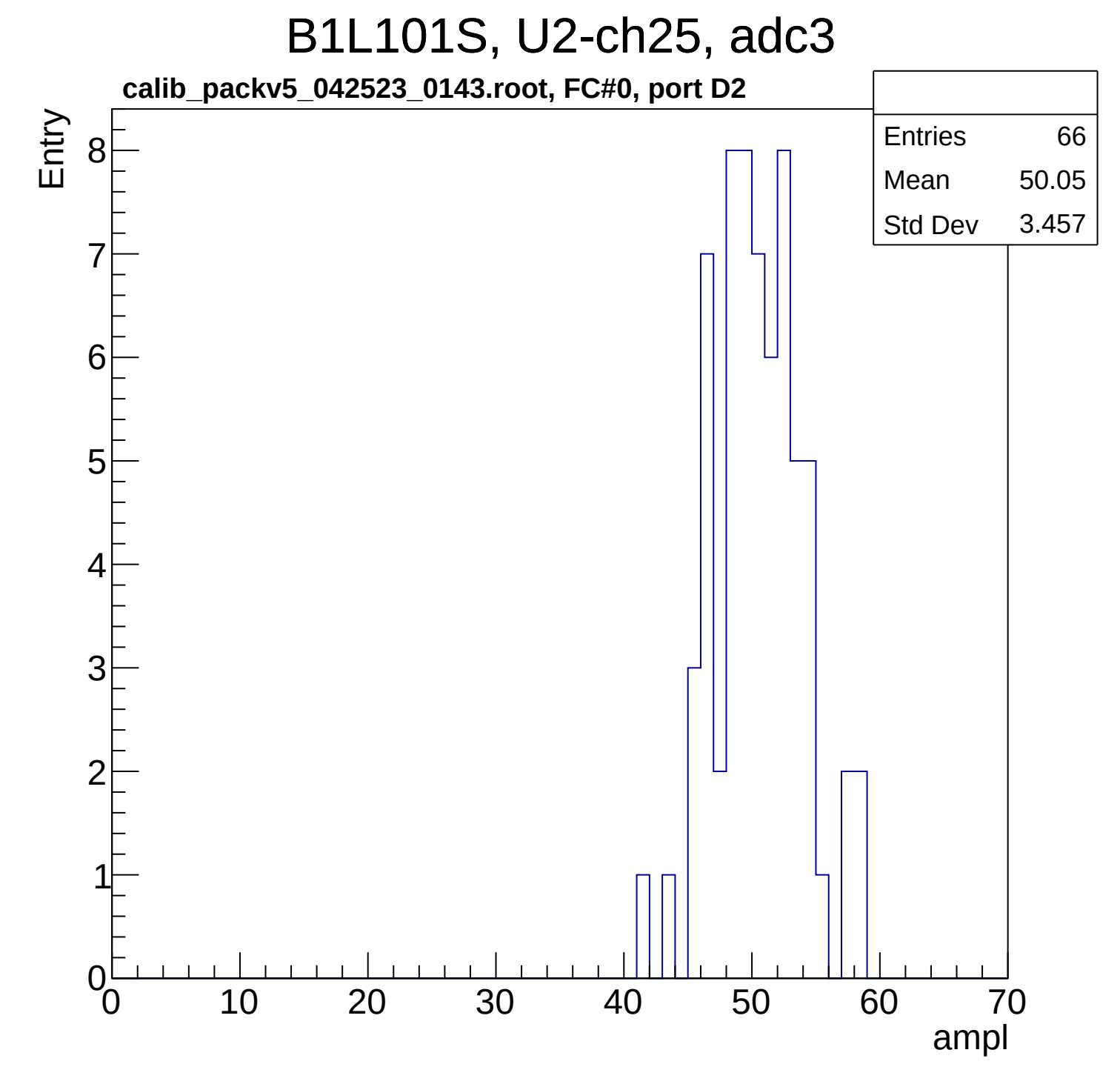

B1L101S, U2-ch24, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 61.29
Std Dev 1.906
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

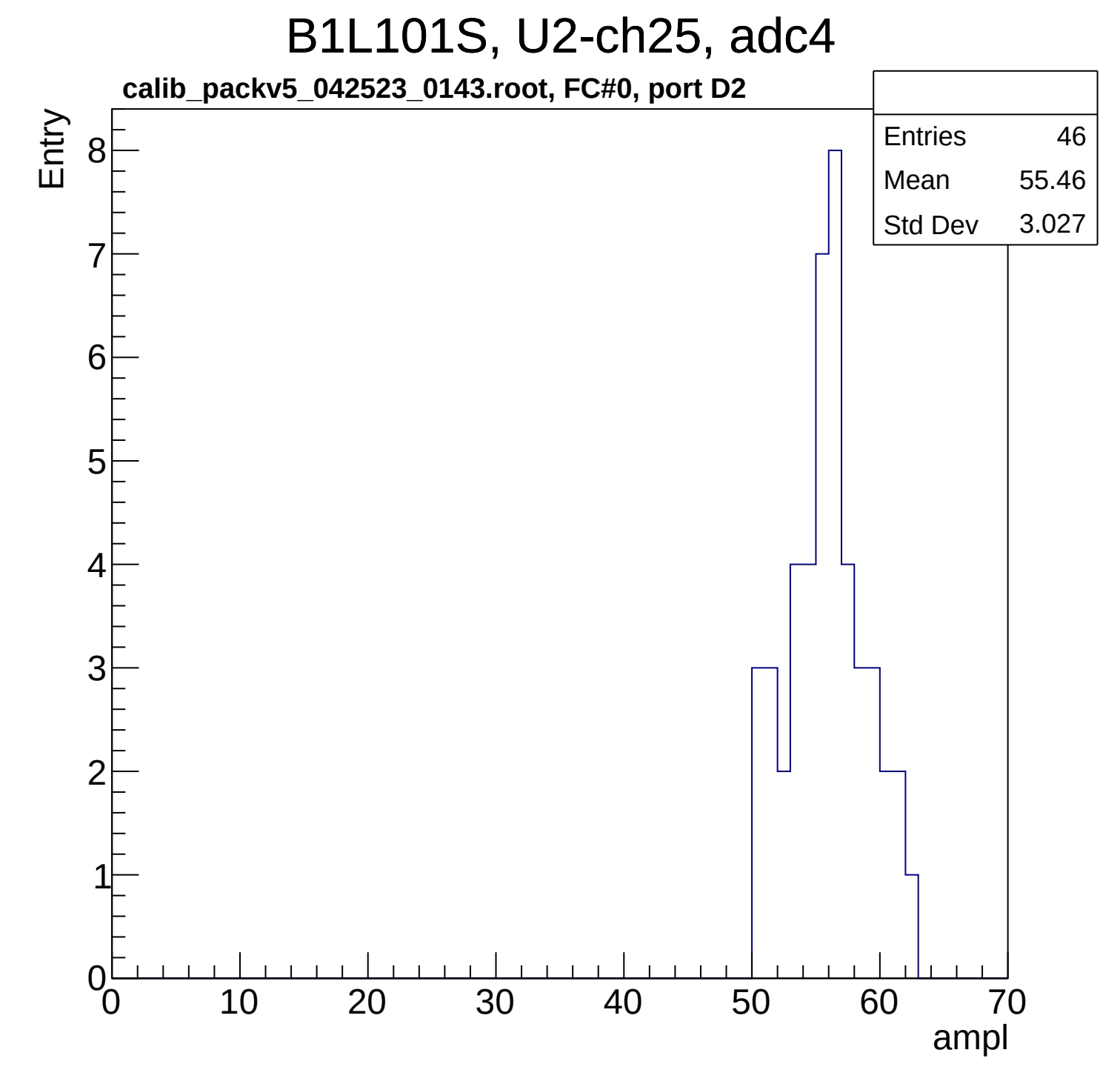

B1L101S, U2-ch24, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 11
Std Dev 11
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

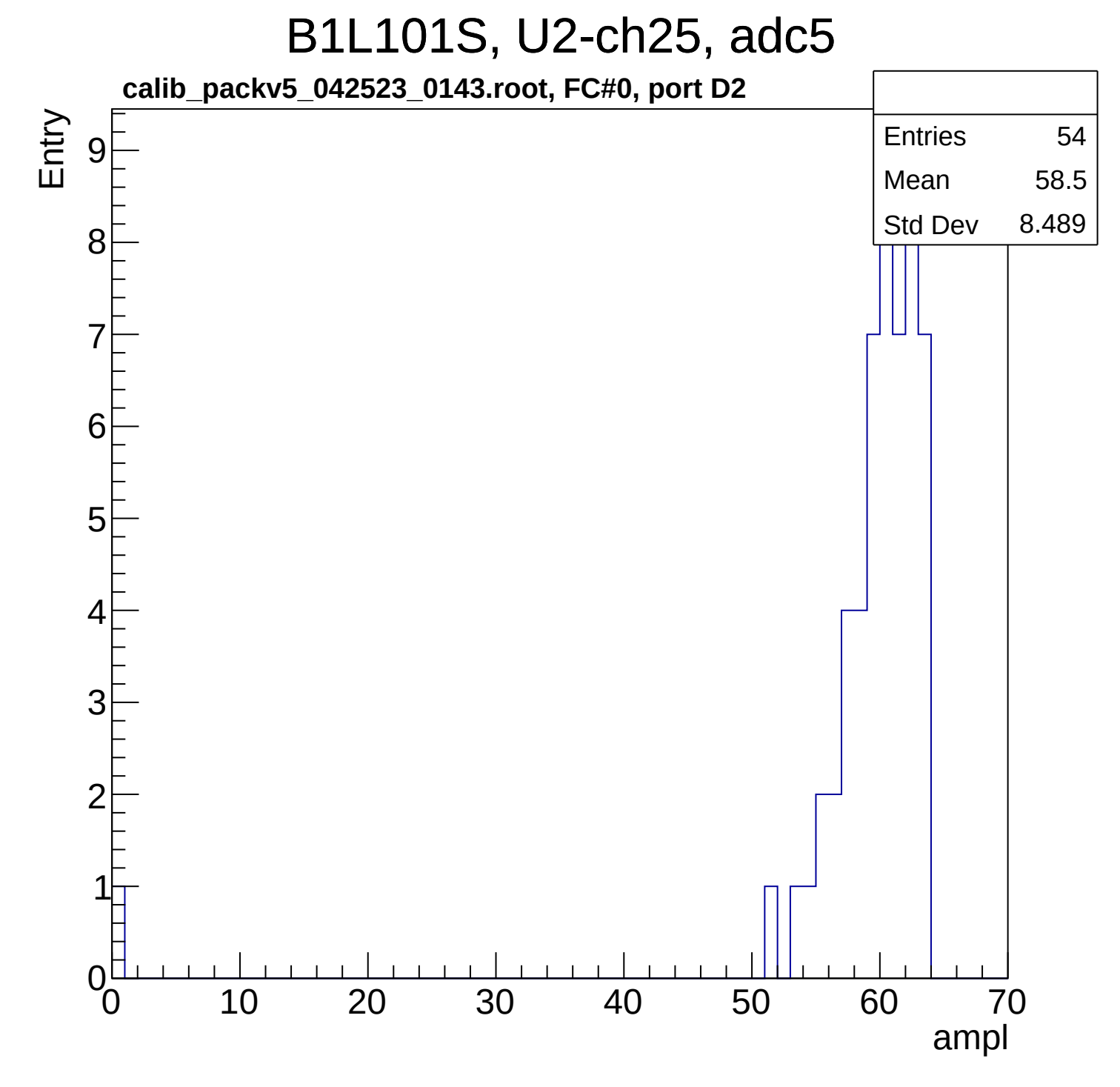

B1L101S, U2-ch25, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 88
Mean 30.95
Std Dev 3.441
Gaus mean : 31.2130
Gaus Width: 3.8170
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

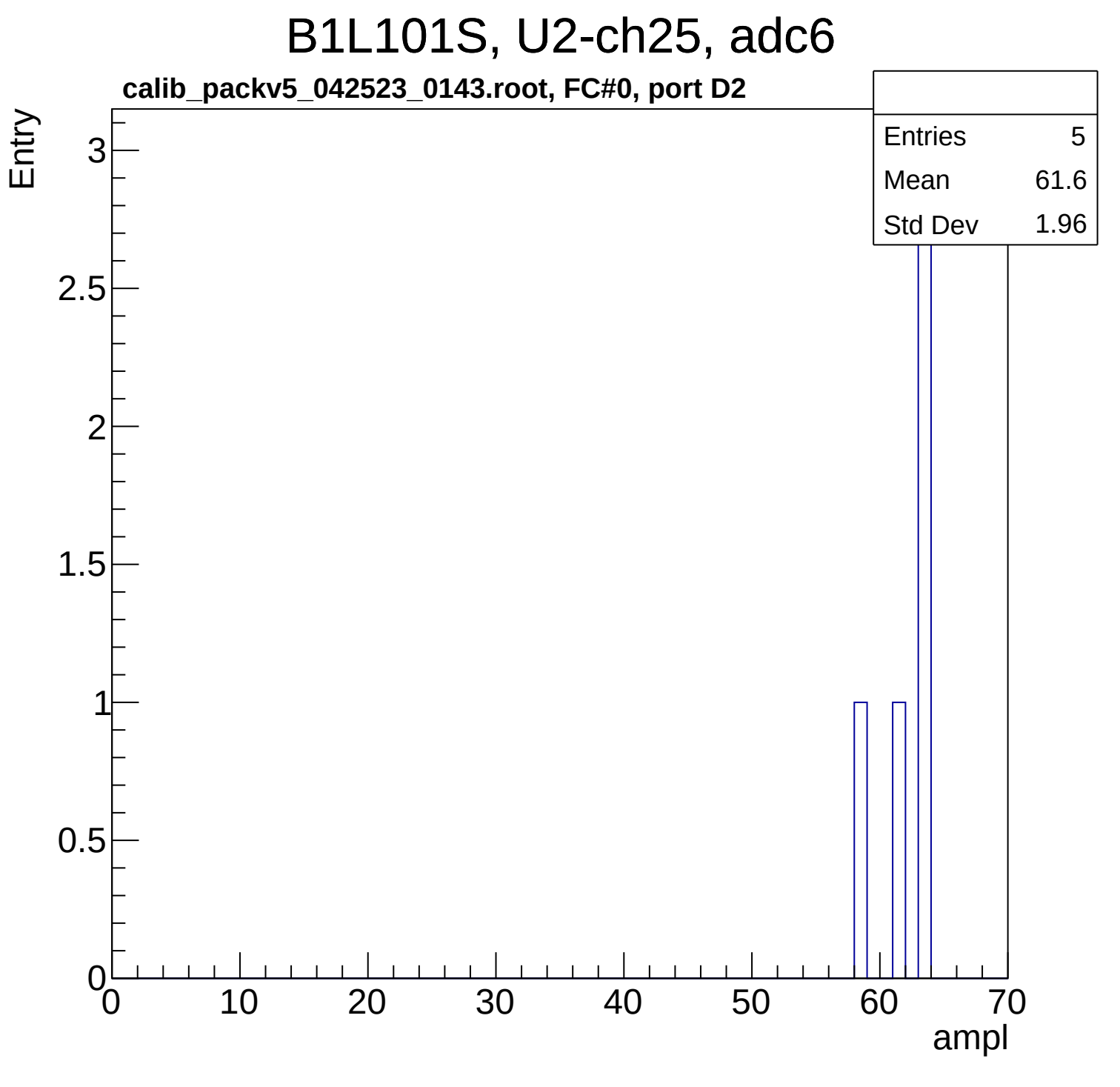

B1L101S, U2-ch25, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 38.02
Std Dev 3.687
Gaus mean : 38.3796
Gaus Width: 4.5885
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

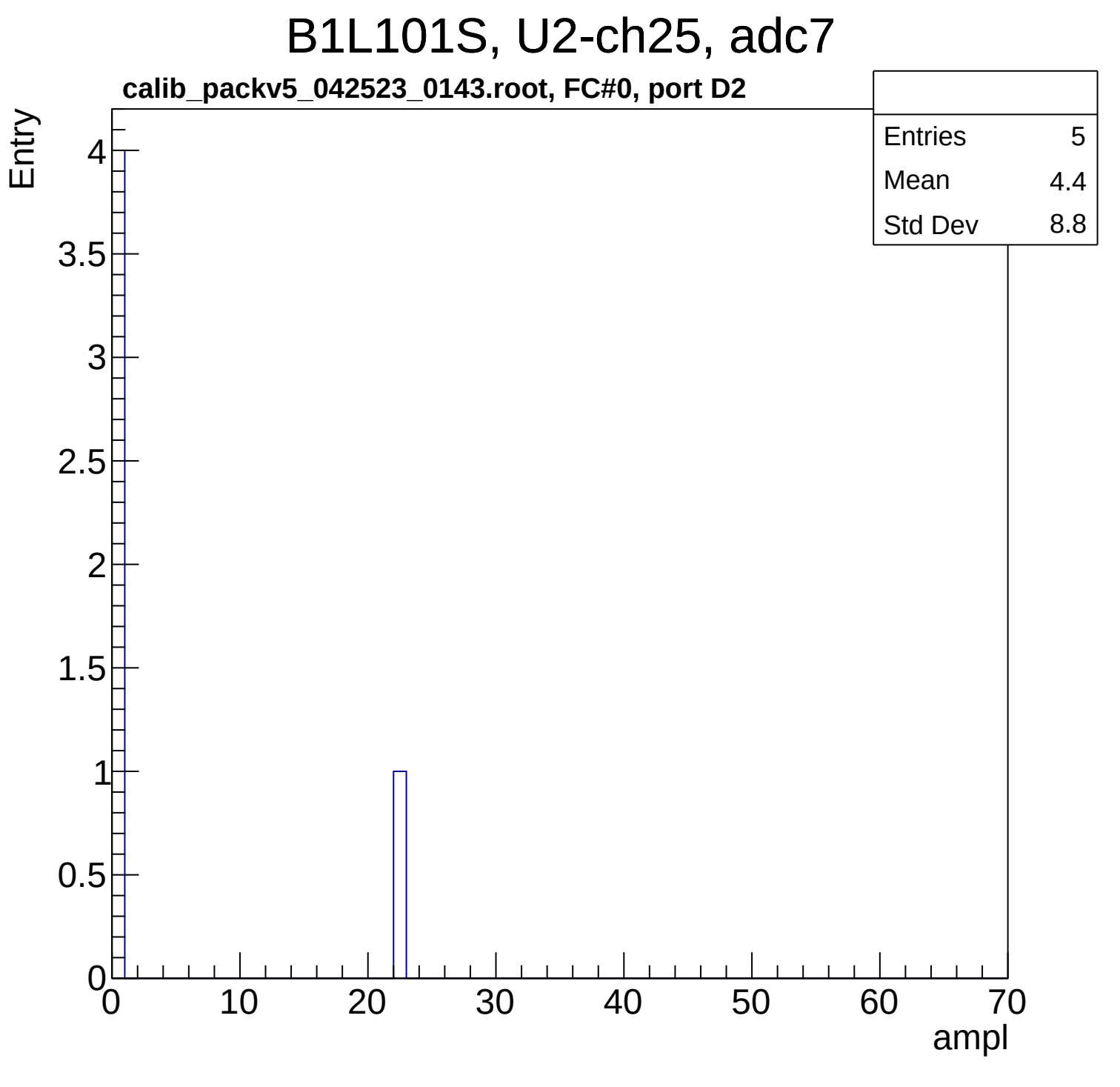

B1L101S, U2-ch25, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 42.57
Std Dev 3.508
Gaus mean : 43.1564
Gaus Width: 4.2628
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

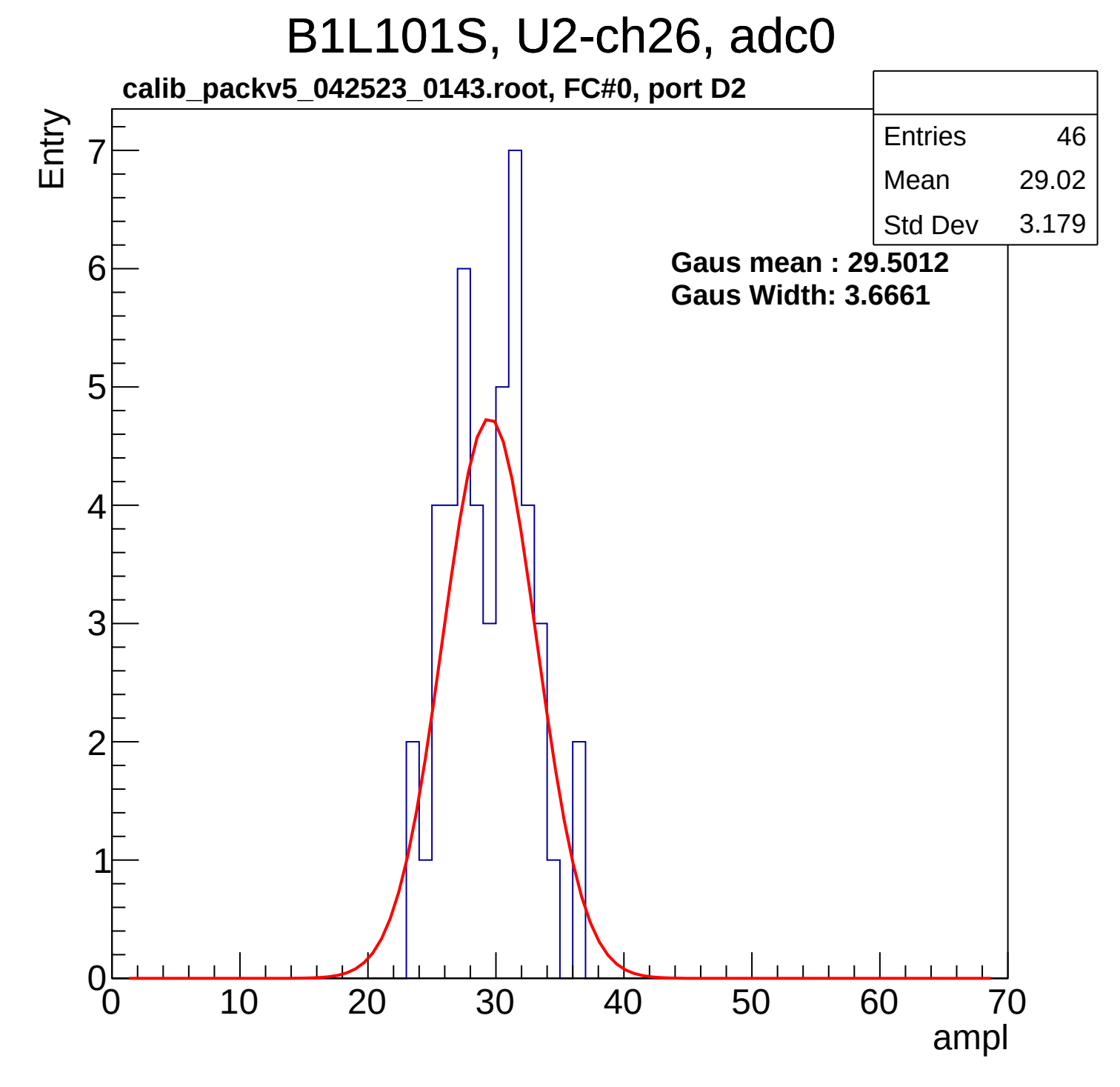

B1L101S, U2-ch25, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 50.05
Std Dev 3.457
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

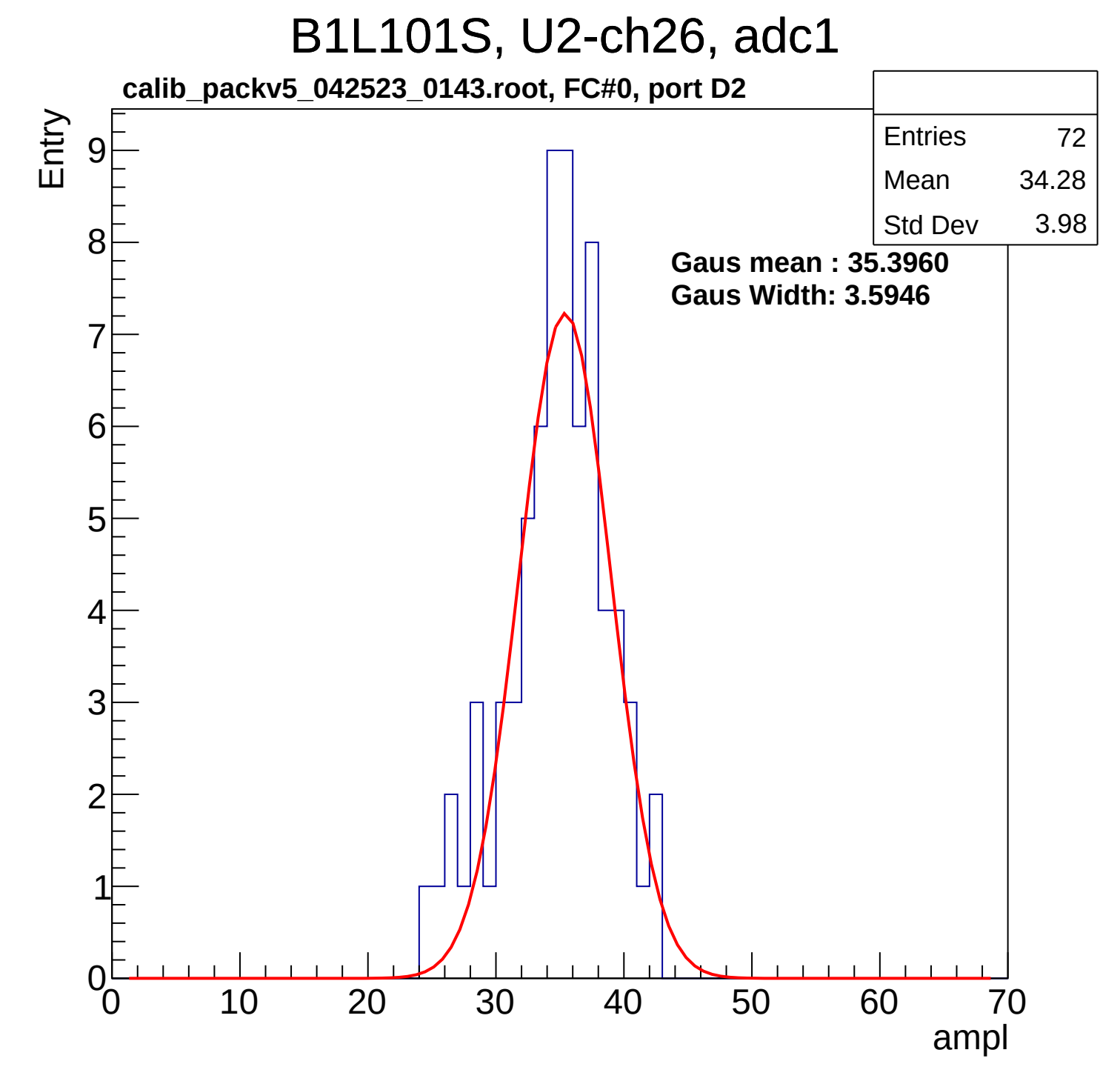

B1L101S, U2-ch25, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 55.46
Std Dev 3.027
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

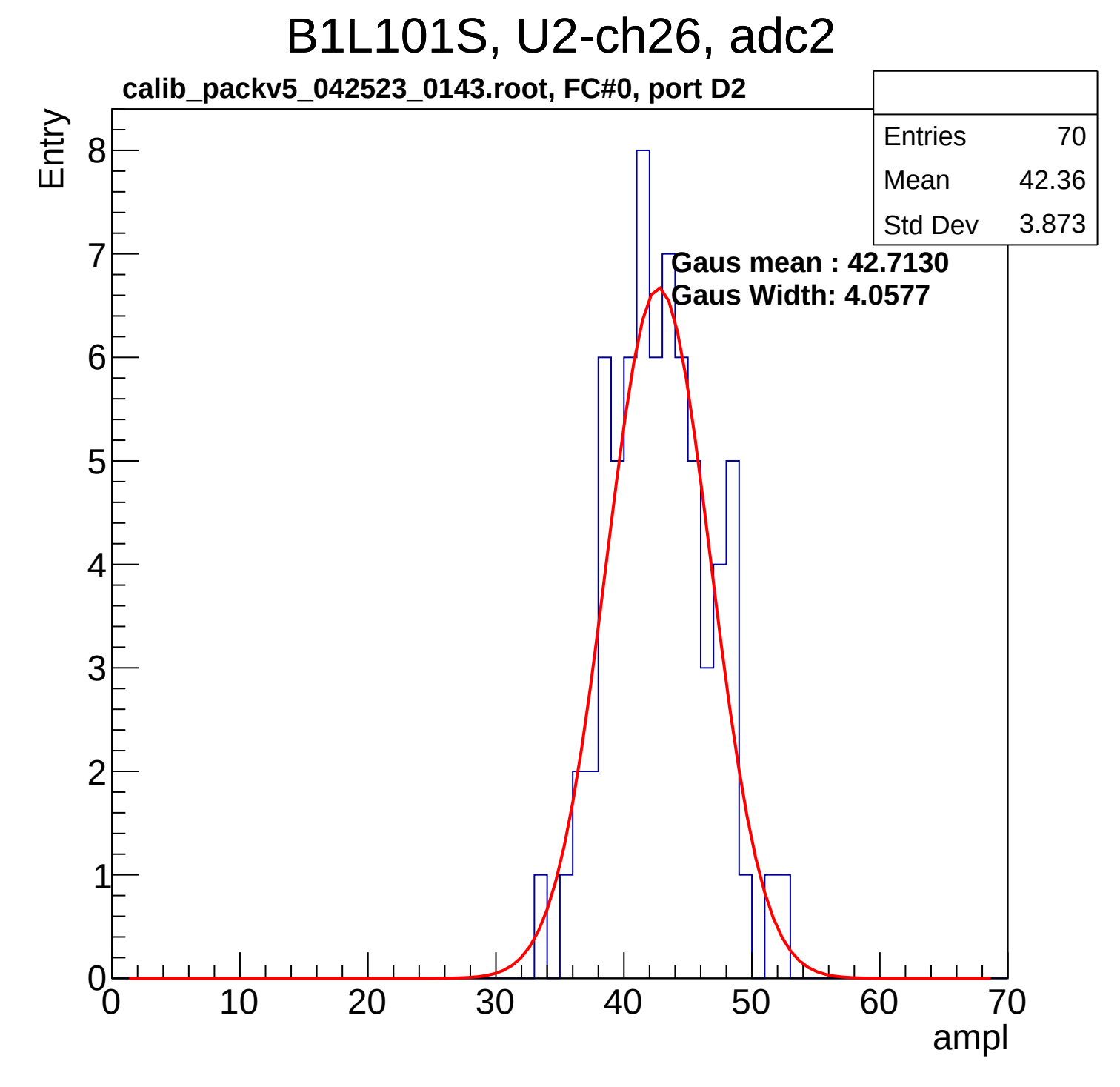

B1L101S, U2-ch25, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 58.5
Std Dev 8.489
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

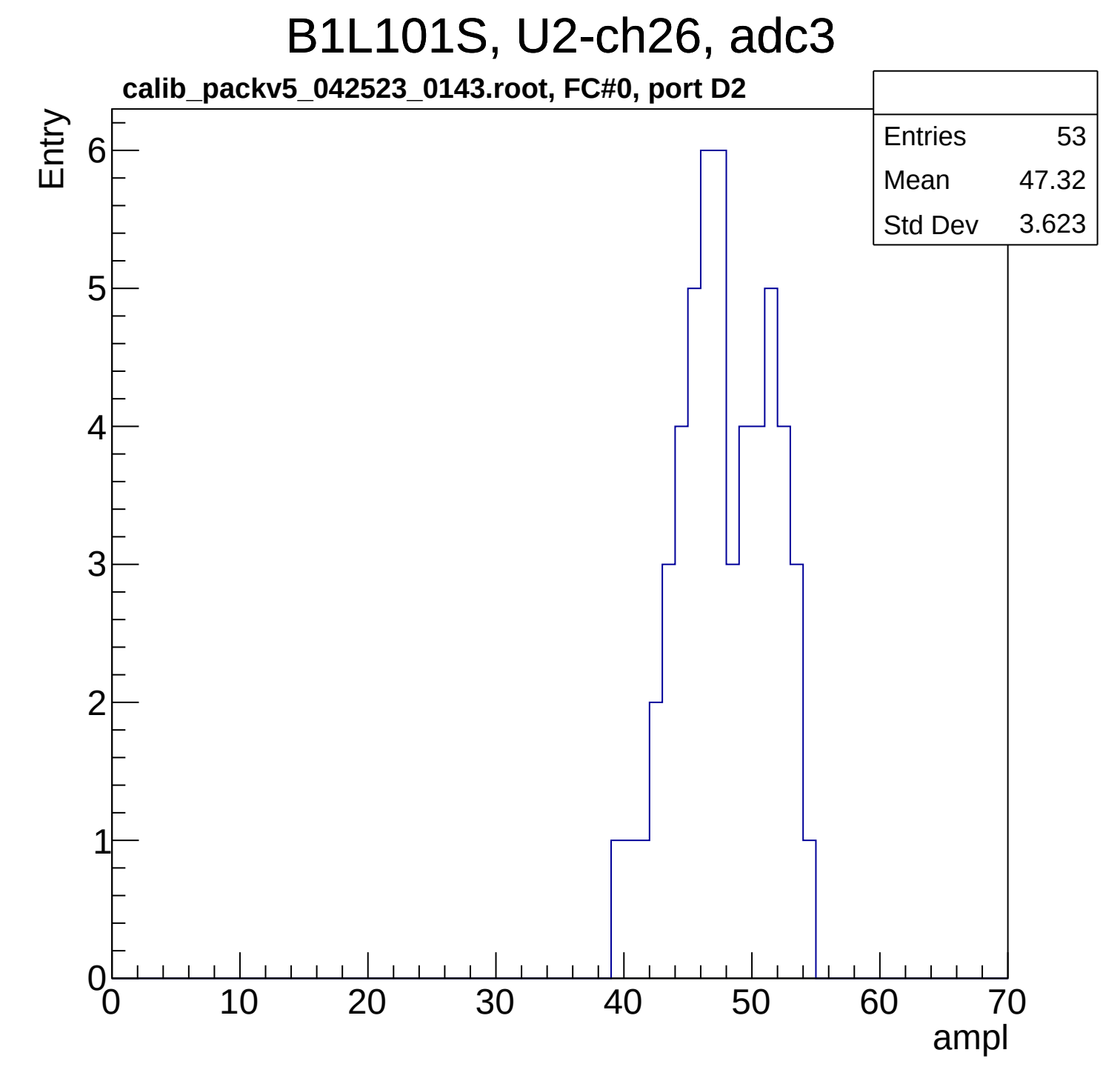

B1L101S, U2-ch25, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 61.6
Std Dev 1.96
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl

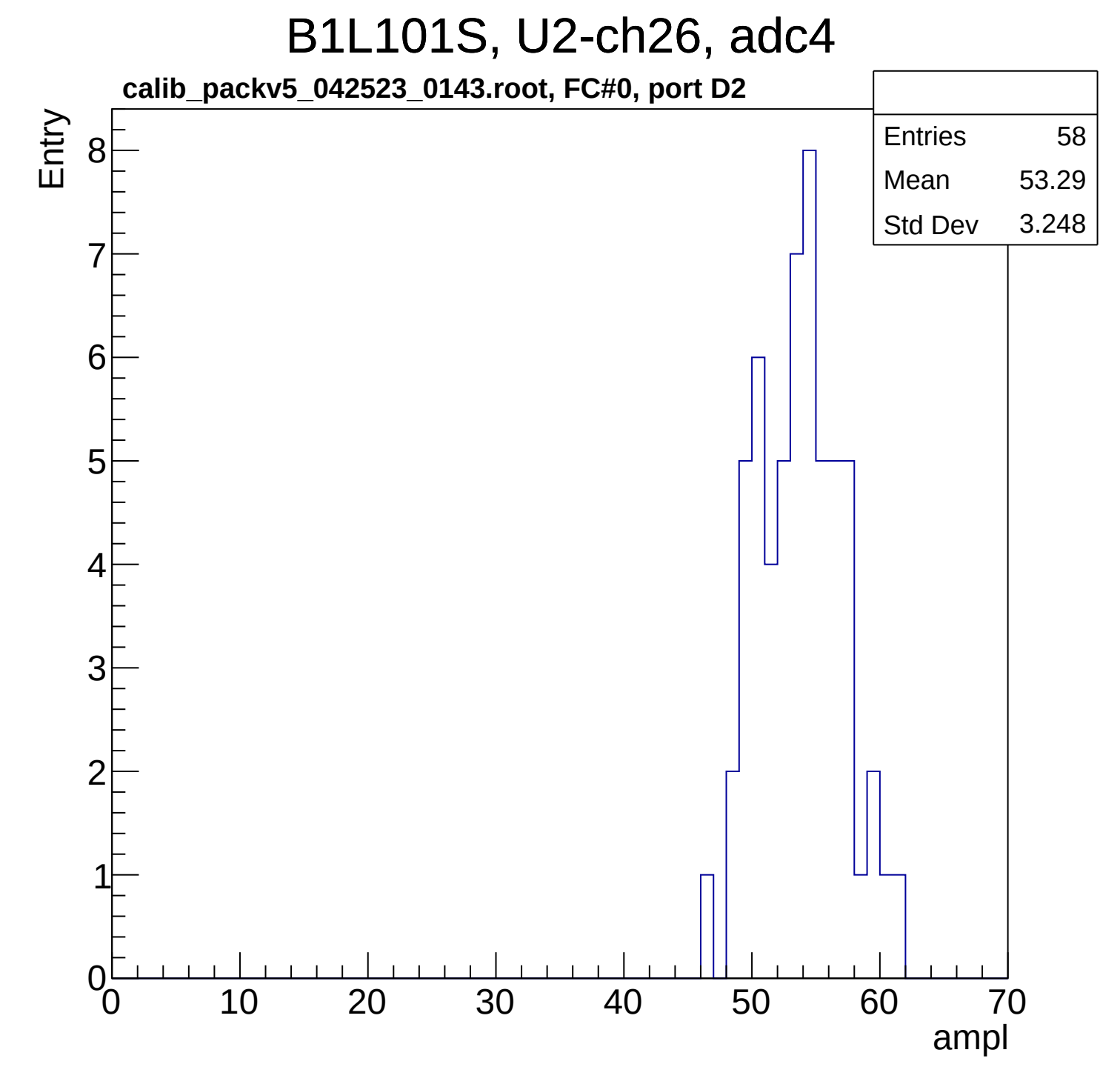

B1L101S, U2-ch25, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 4.4
Std Dev 8.8
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

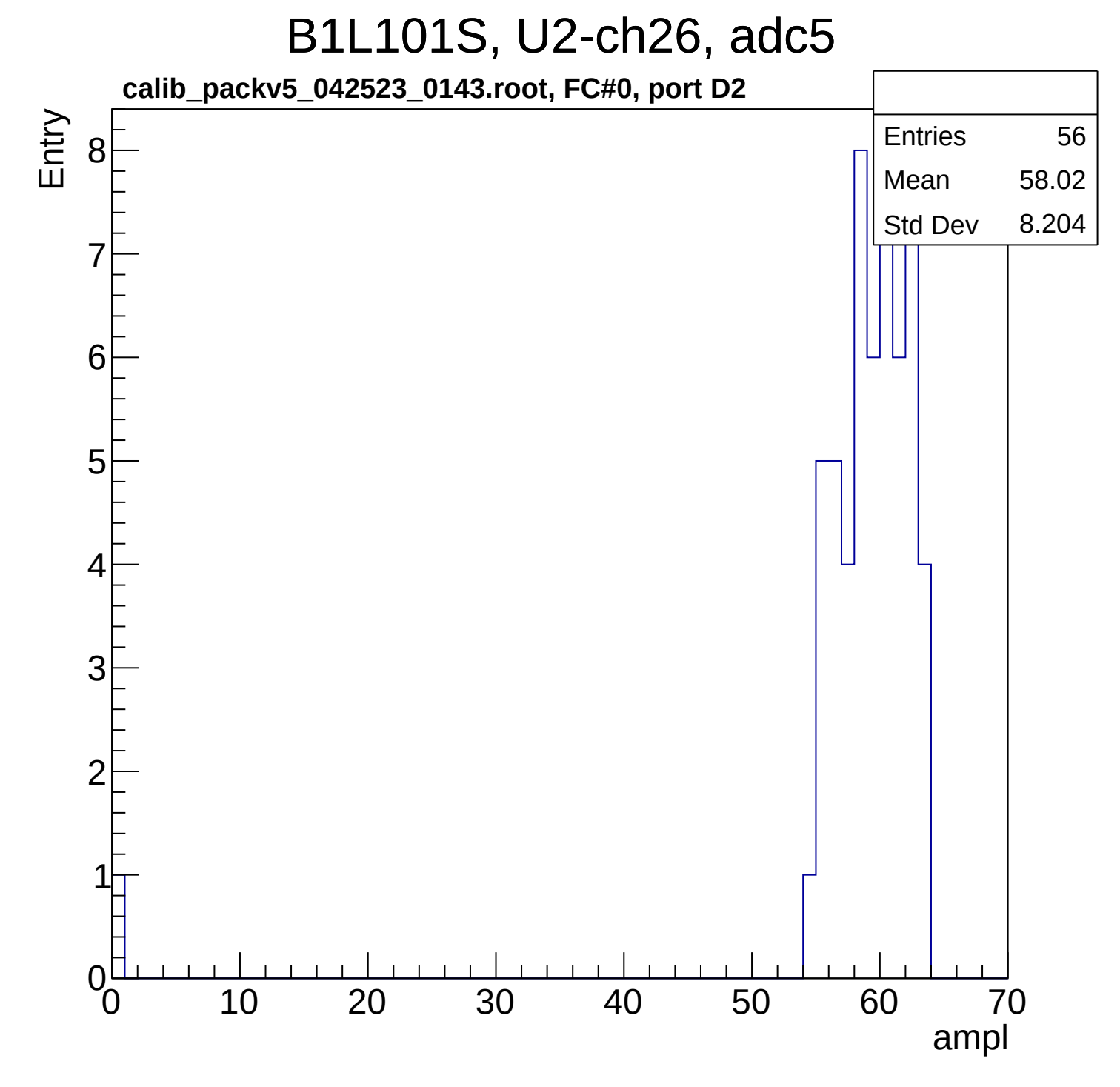

B1L101S, U2-ch26, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 29.02
Std Dev 3.179
Gaus mean : 29.5012
Gaus Width: 3.6661
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

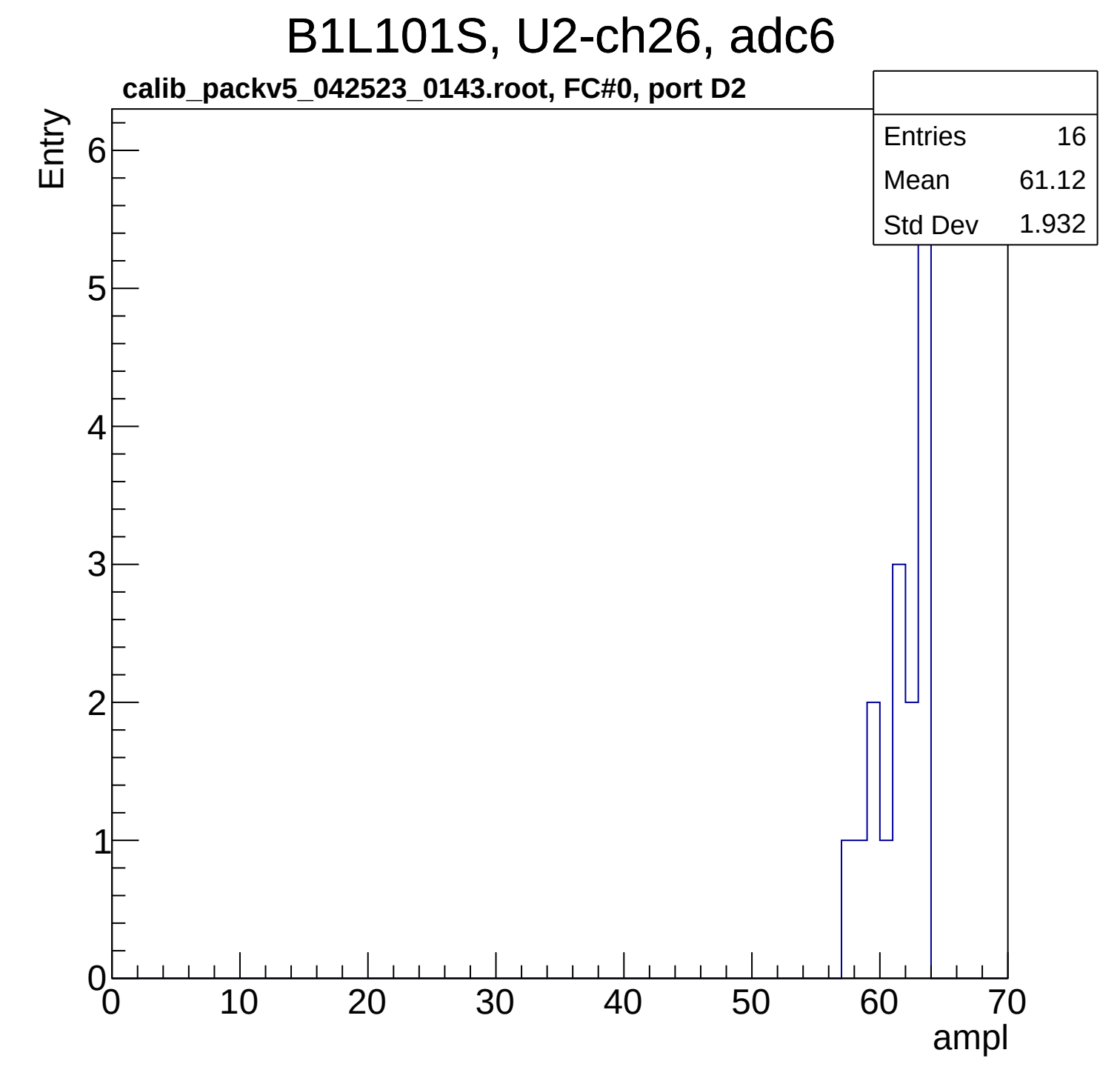

B1L101S, U2-ch26, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 34.28
Std Dev 3.98
Gaus mean : 35.3960
Gaus Width: 3.5946
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

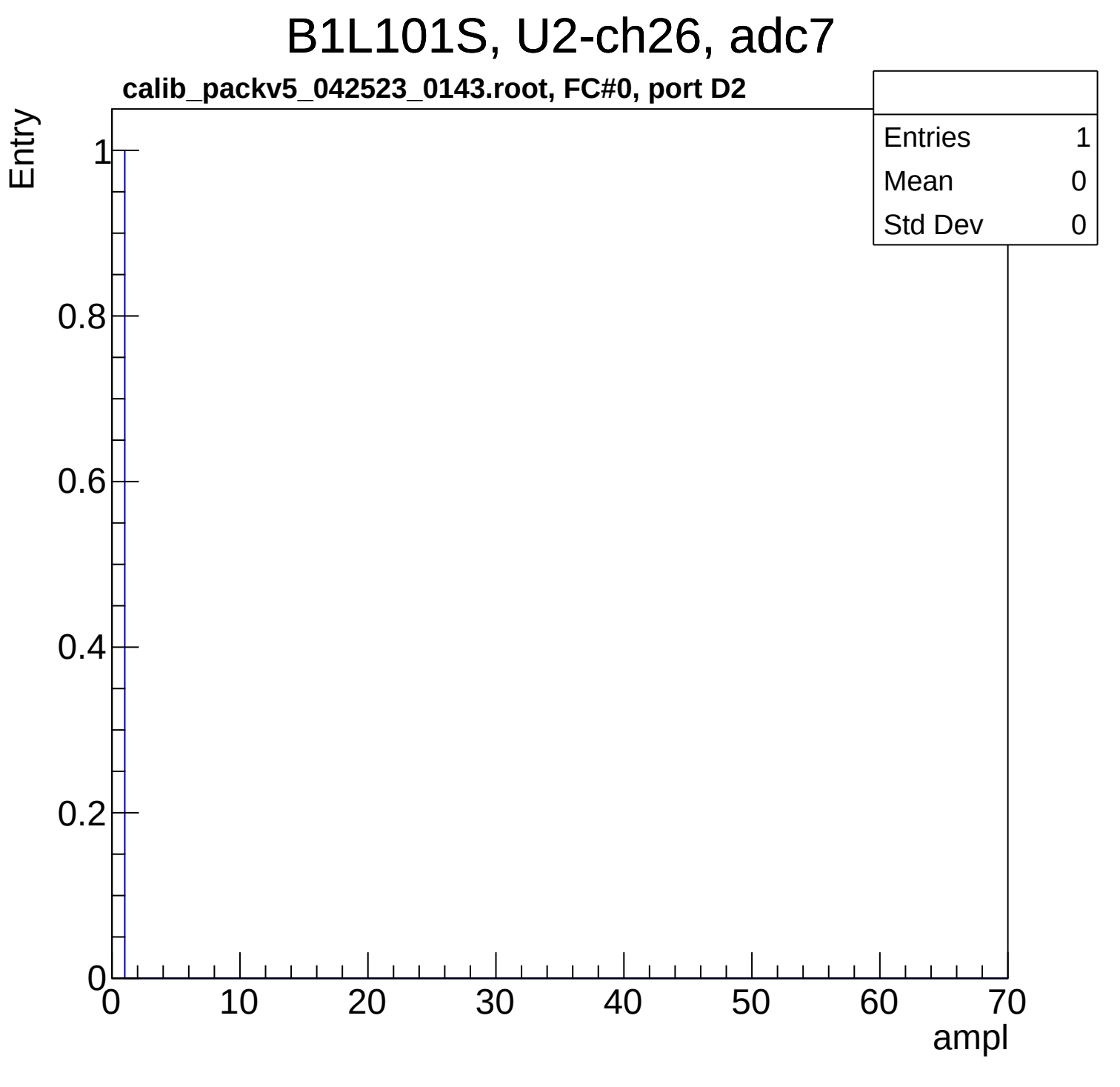

B1L101S, U2-ch26, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 42.36
Std Dev 3.873
Gaus mean : 42.7130
Gaus Width: 4.0577
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

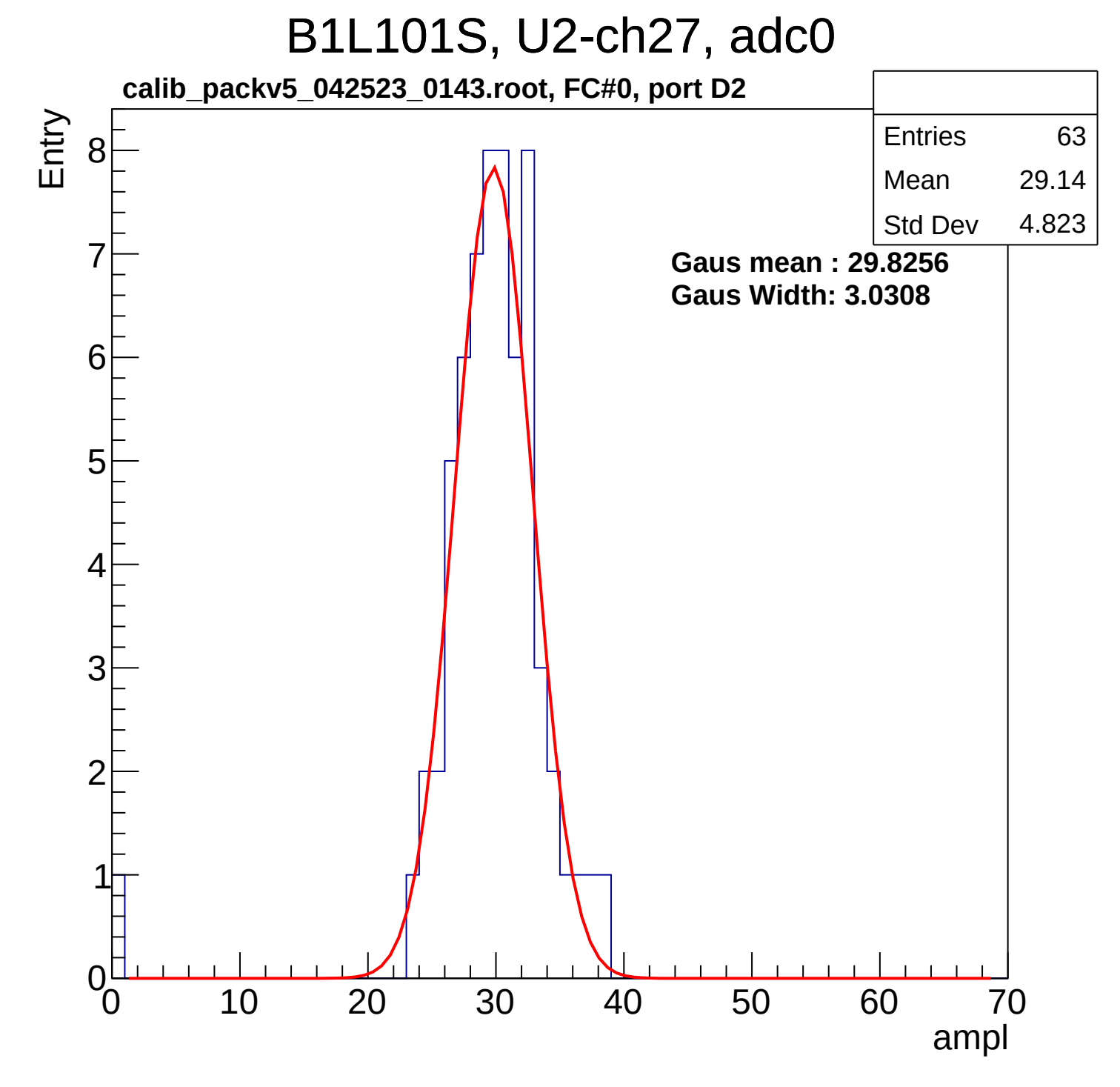

B1L101S, U2-ch26, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 47.32
Std Dev 3.623
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

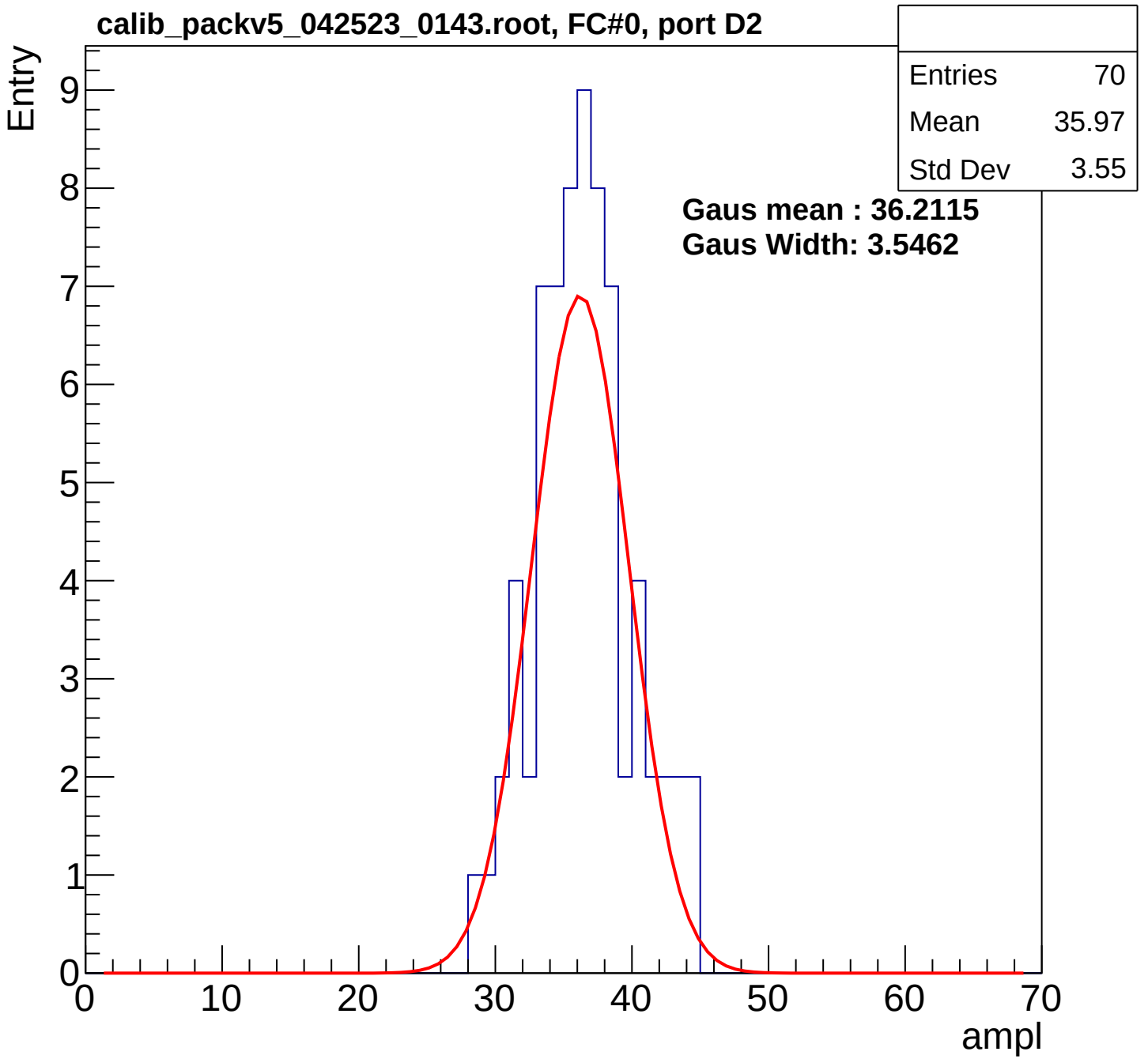

B1L101S, U2-ch26, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 53.29
Std Dev 3.248
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

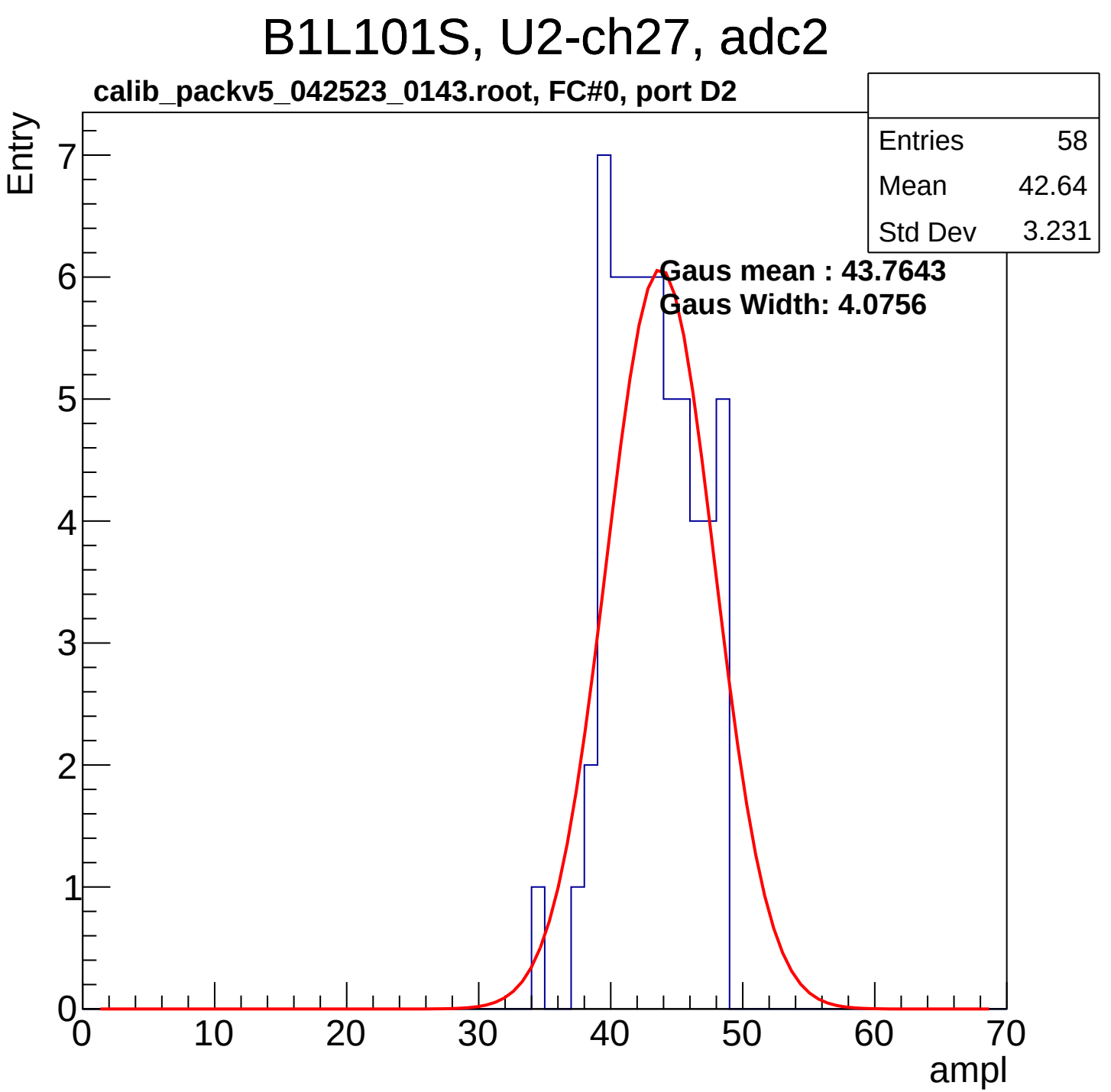

B1L101S, U2-ch26, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 58.02
Std Dev 8.204
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

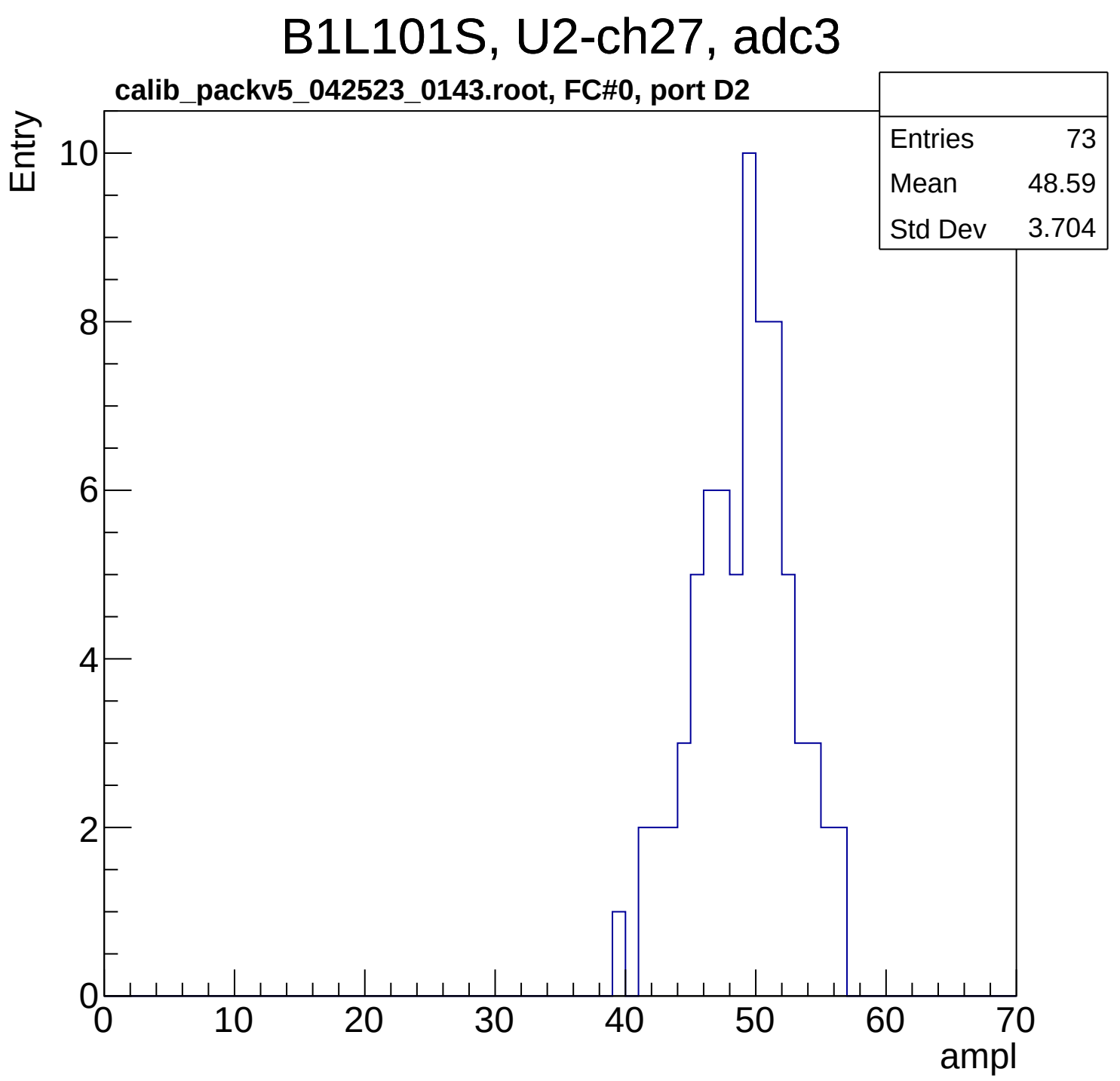

B1L101S, U2-ch26, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 16
Mean 61.12
Std Dev 1.932
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

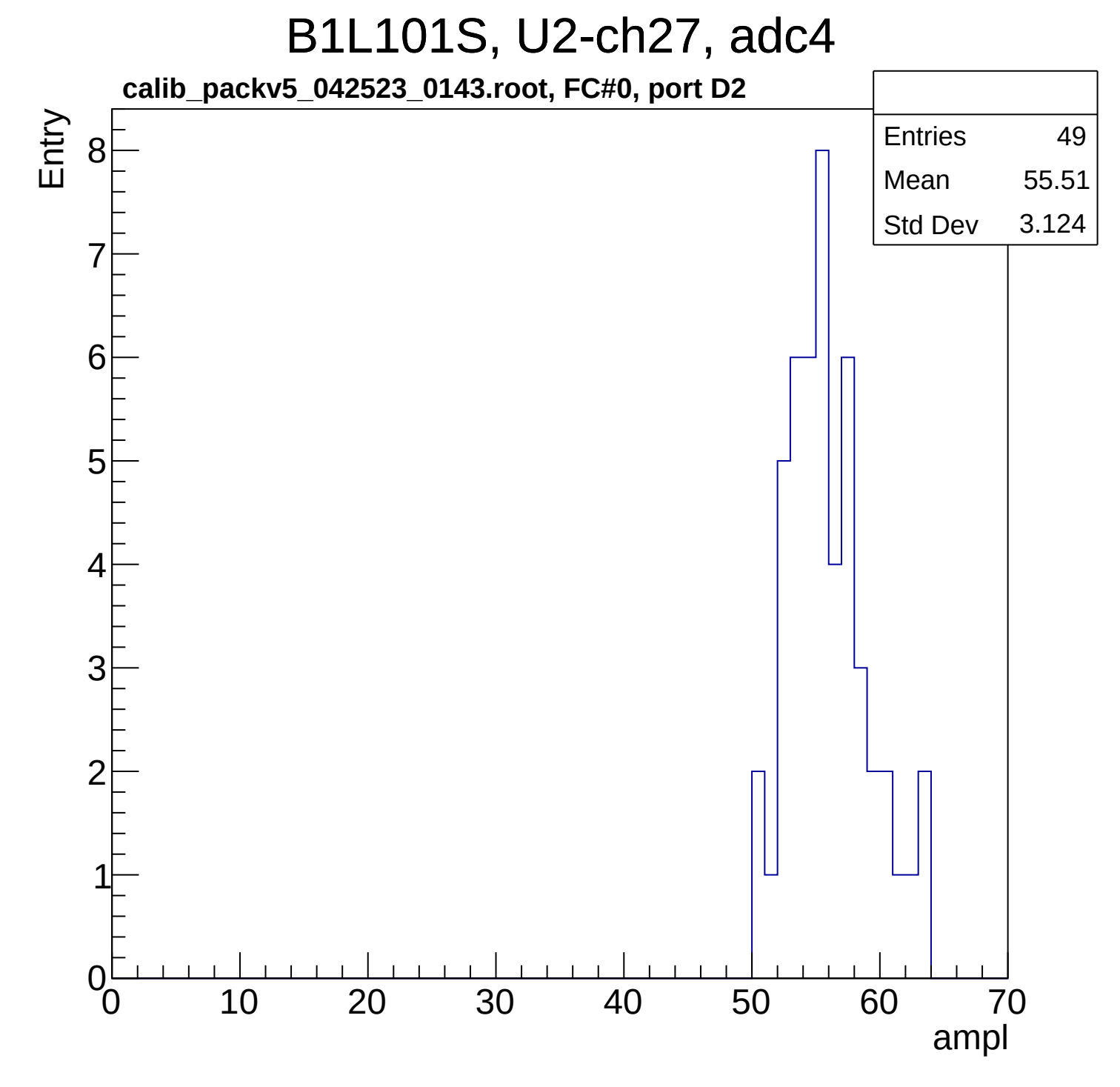

B1L101S, U2-ch26, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

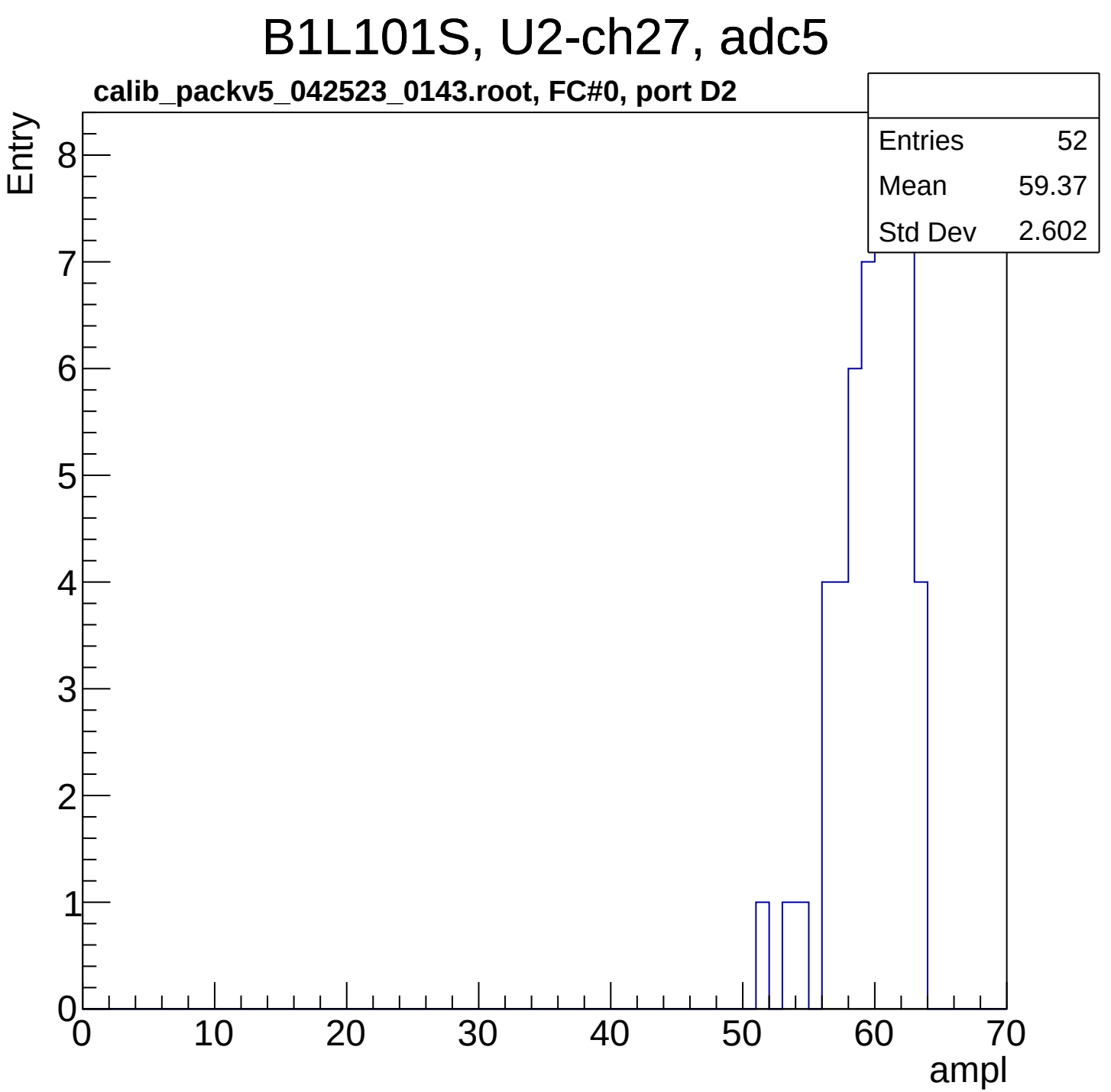

B1L101S, U2-ch27, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 29.14
Std Dev 4.823
Gaus mean : 29.8256
Gaus Width: 3.0308
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

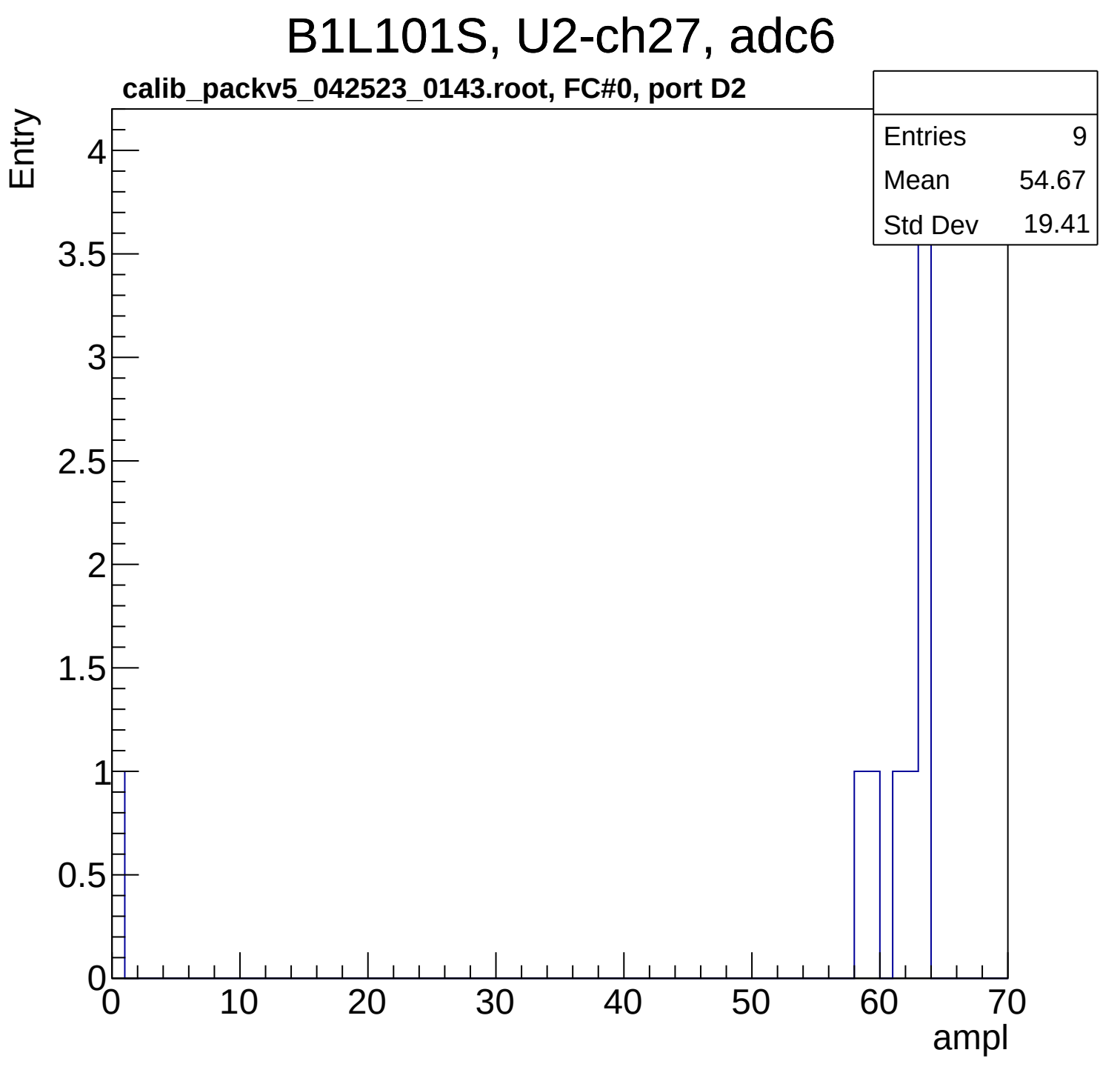

B1L101S, U2-ch27, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 35.97
Std Dev 3.55
Gaus mean : 36.2115
Gaus Width: 3.5462
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

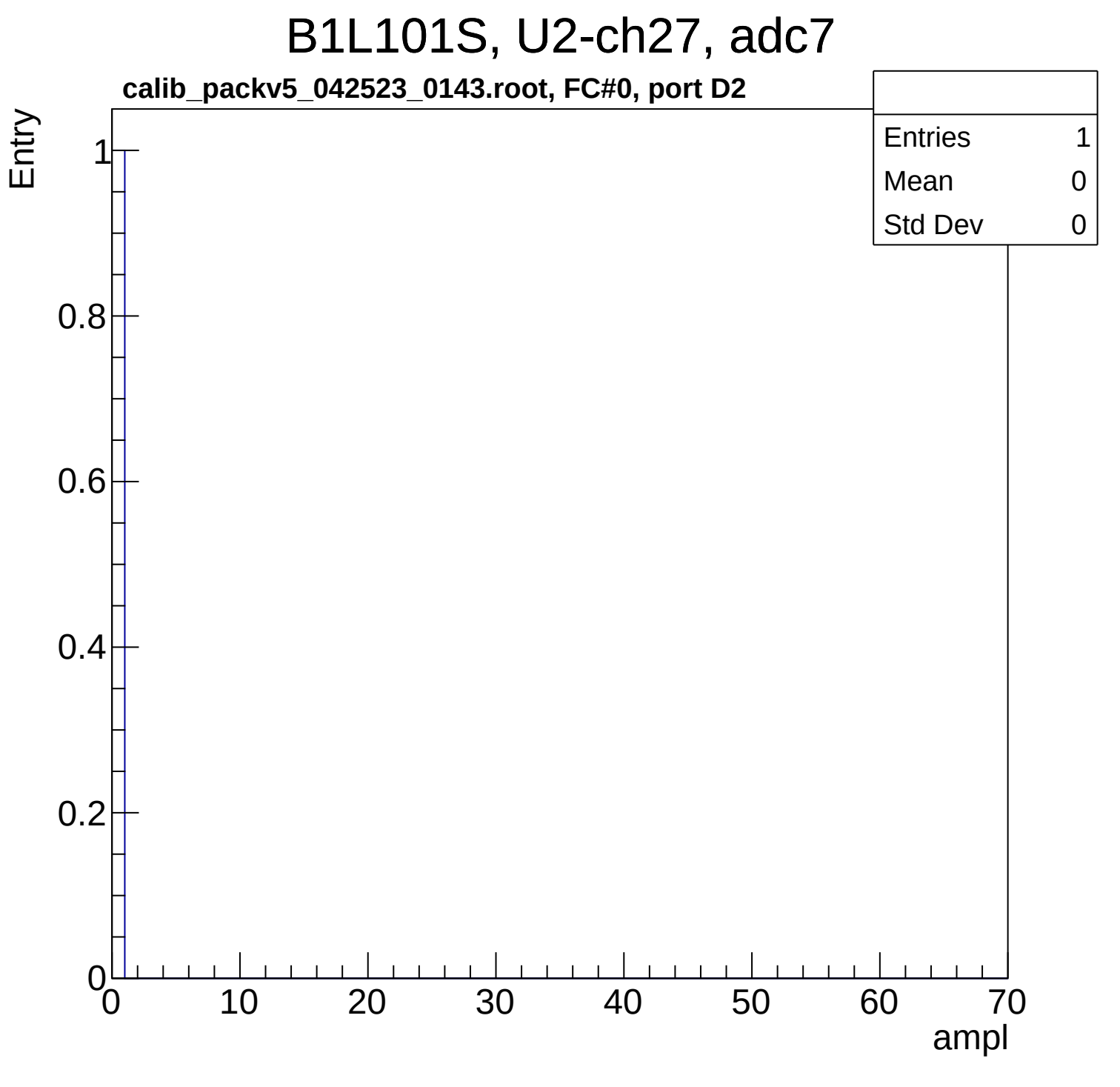

B1L101S, U2-ch27, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 42.64
Std Dev 3.231
Gaus mean : 43.7643
Gaus Width: 4.0756
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

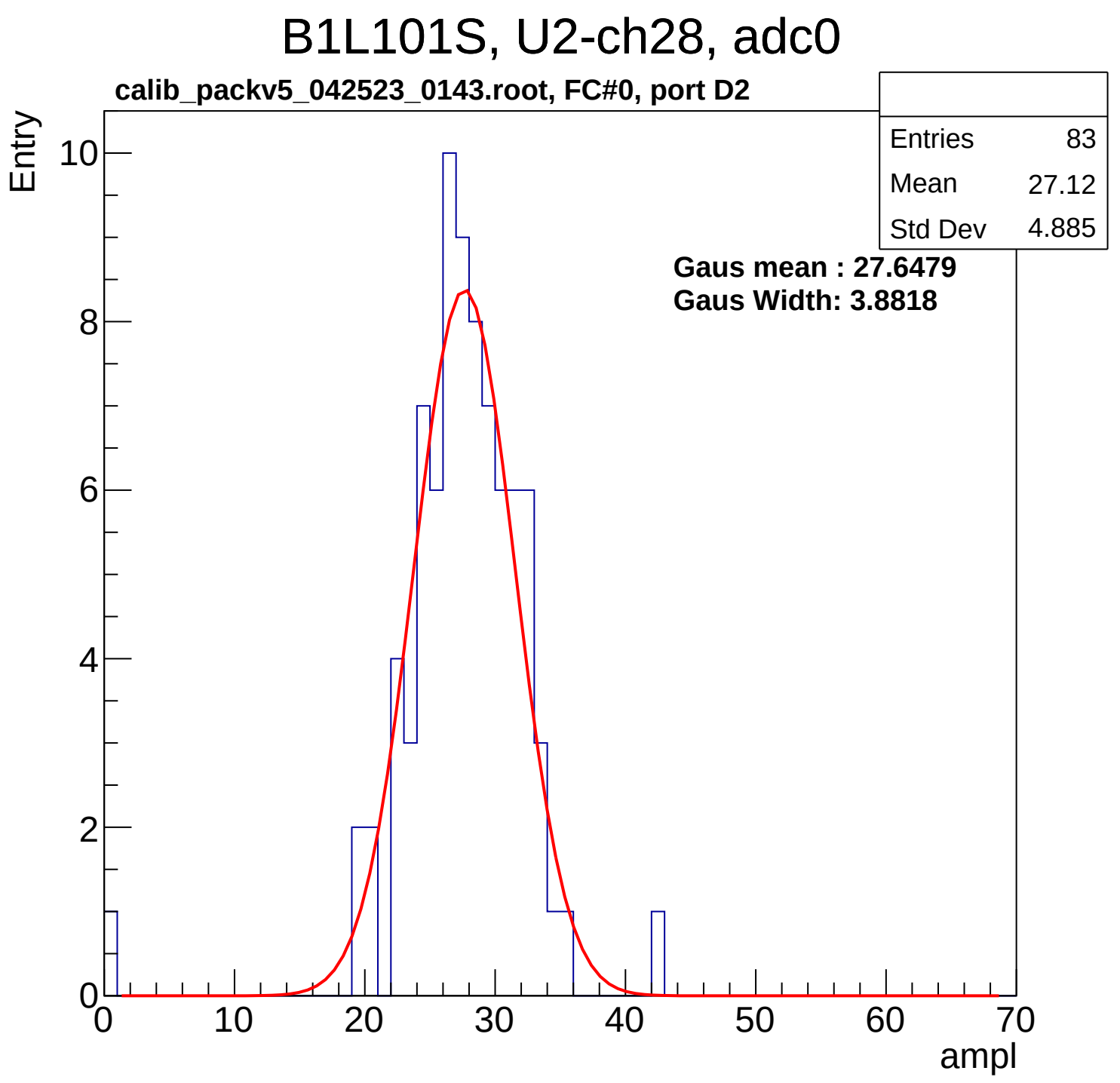

B1L101S, U2-ch27, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 48.59
Std Dev 3.704
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

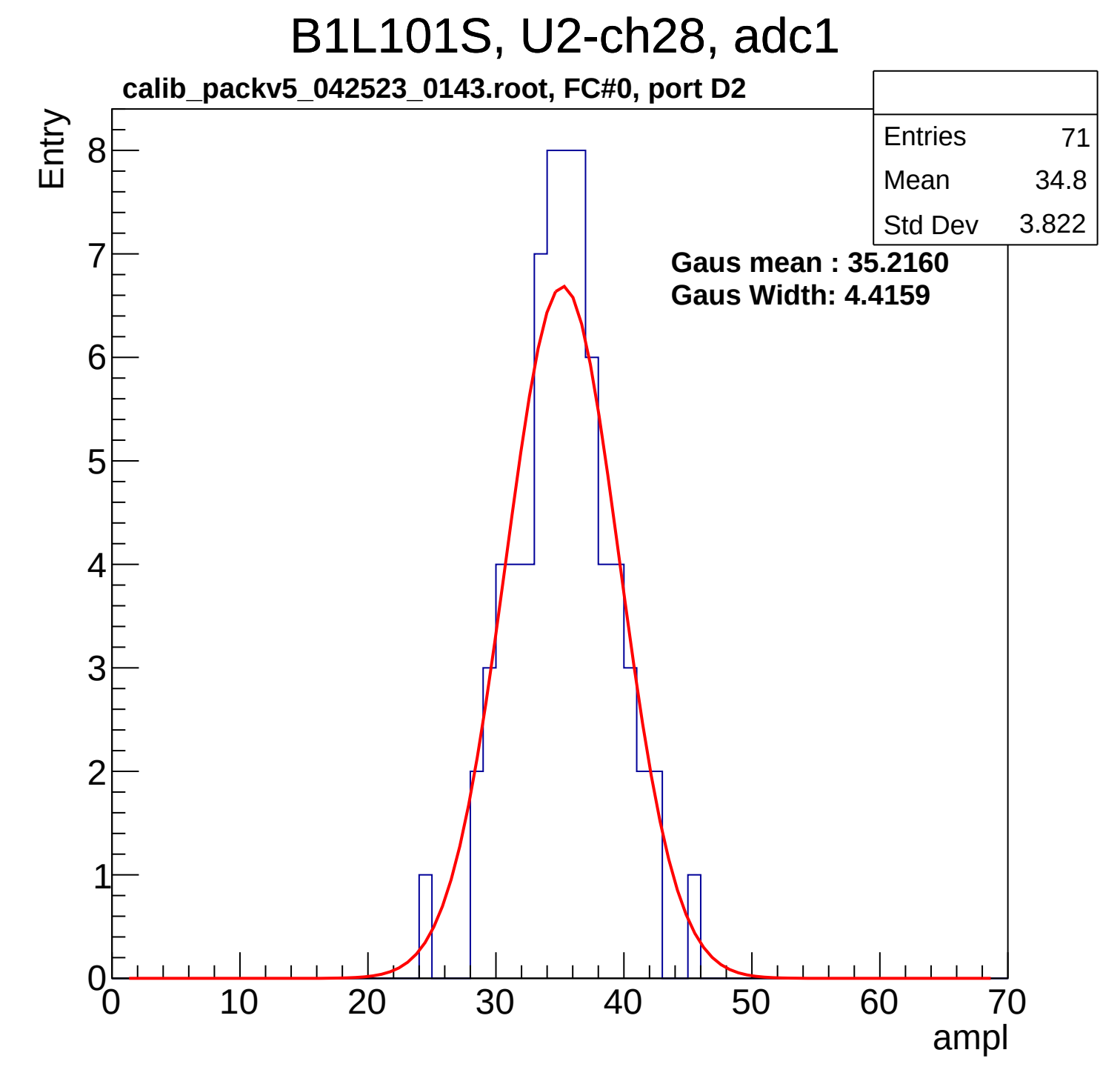

B1L101S, U2-ch27, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 55.51
Std Dev 3.124
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

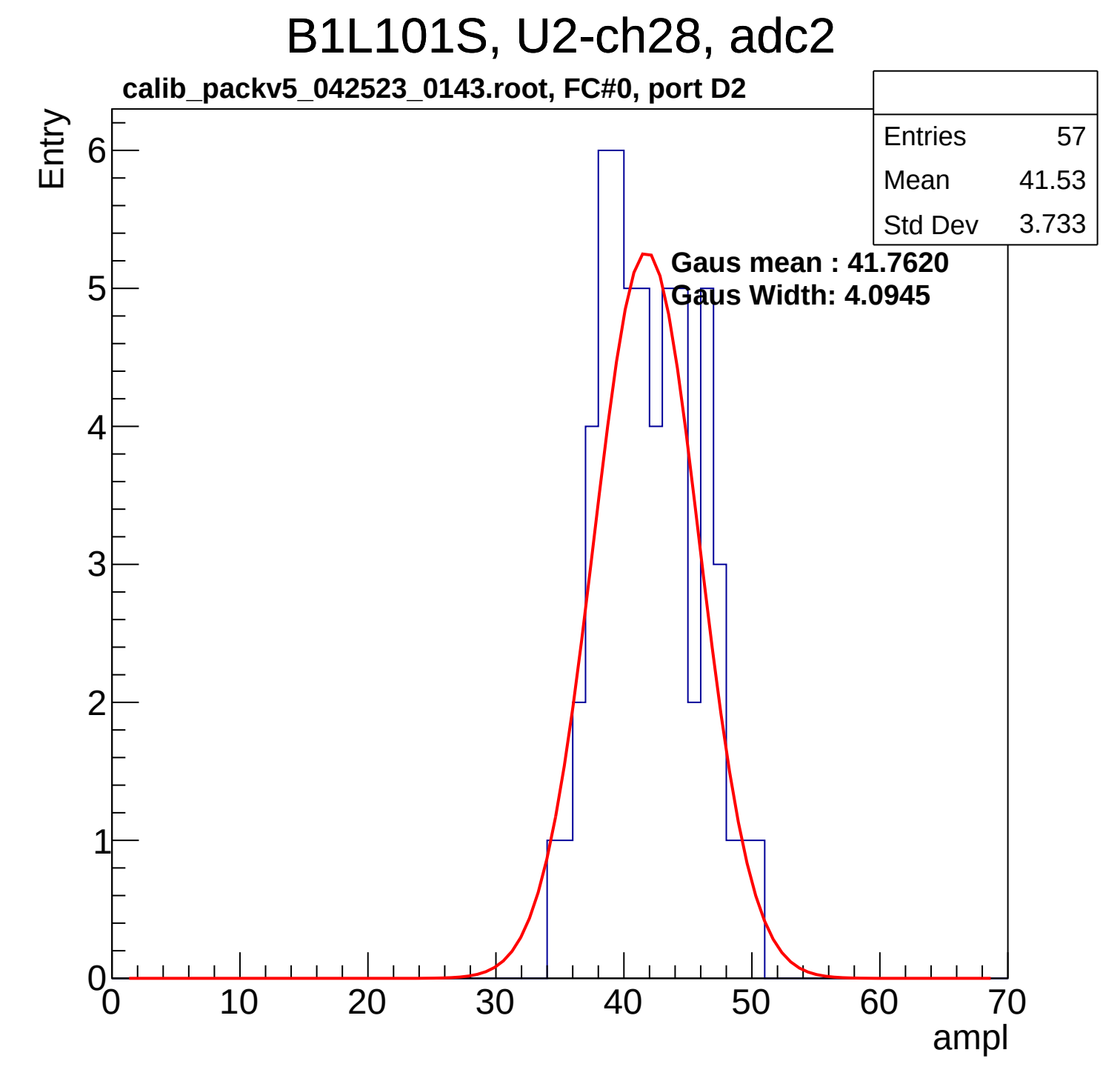

B1L101S, U2-ch27, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 59.37
Std Dev 2.602
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

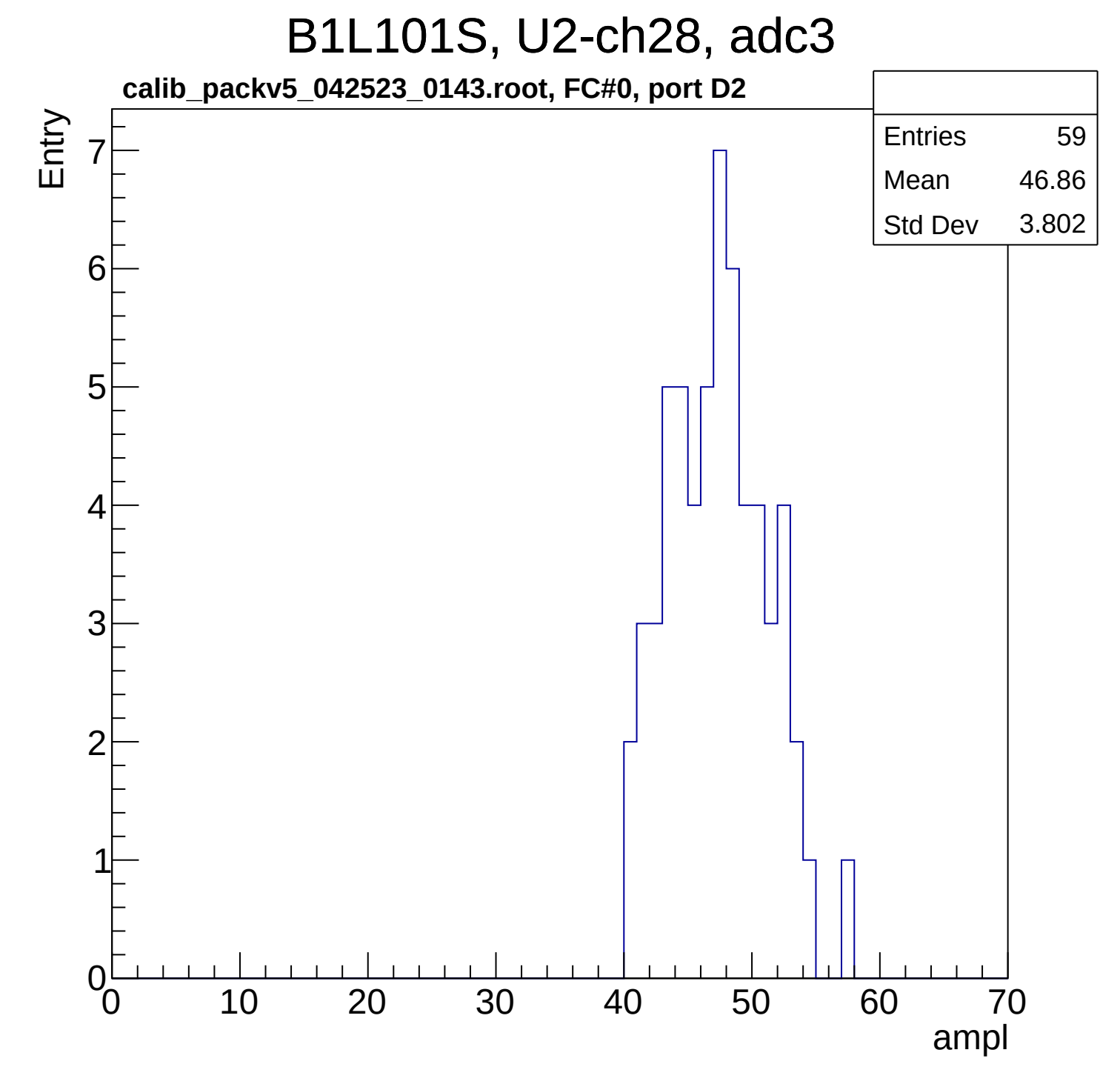

B1L101S, U2-ch27, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 54.67
Std Dev 19.41
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

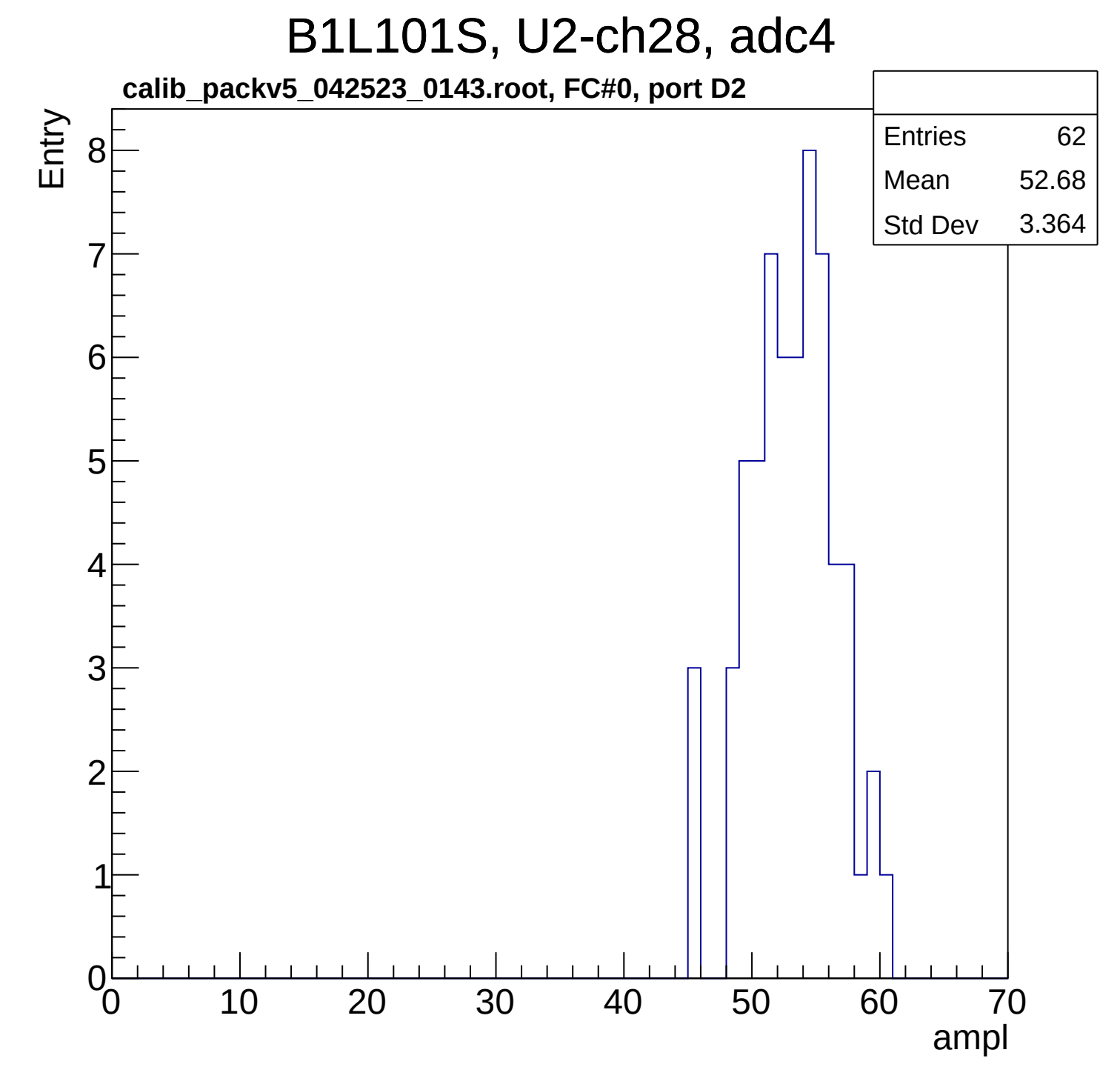

B1L101S, U2-ch27, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

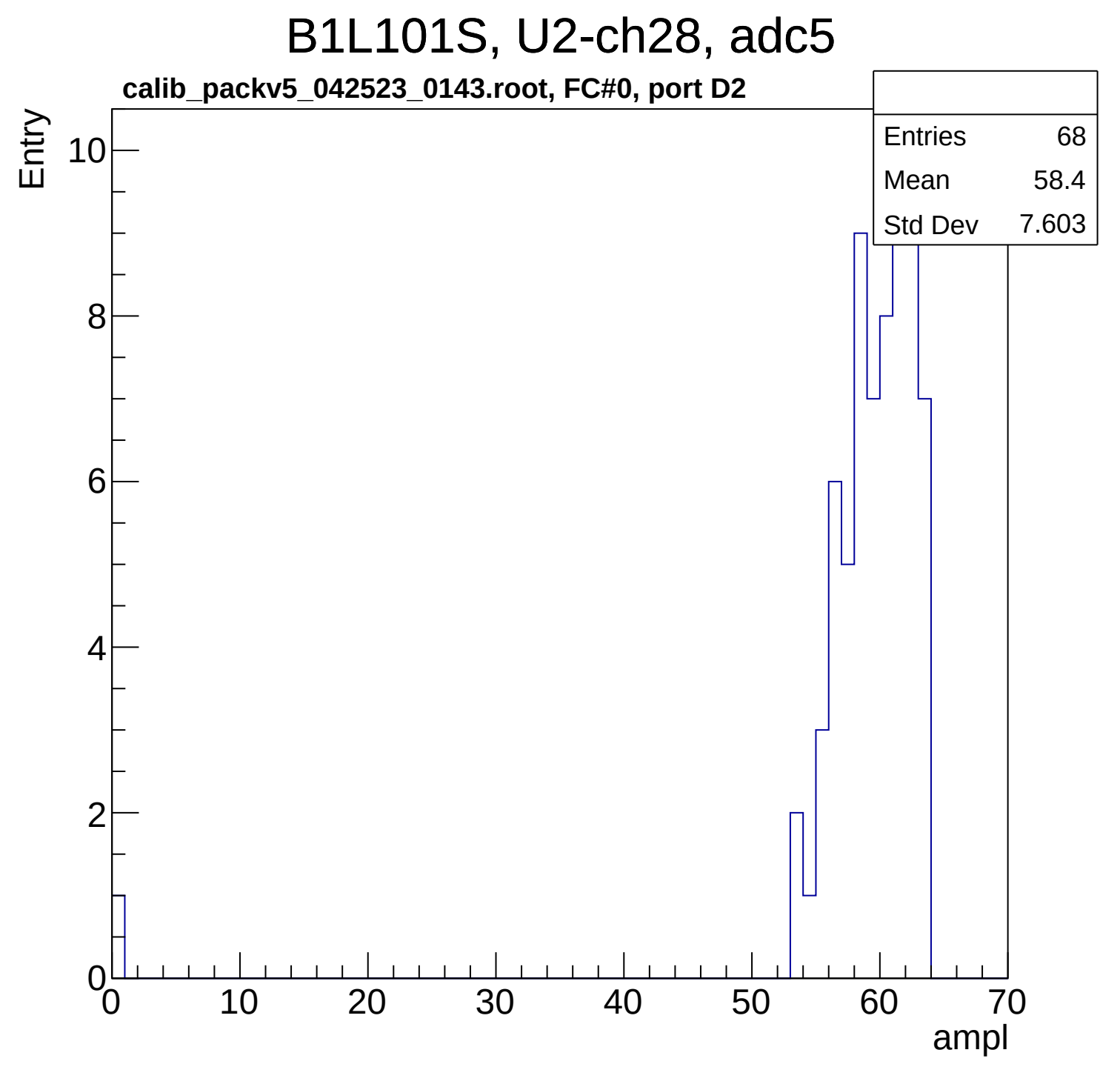

B1L101S, U2-ch28, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 83
Mean 27.12
Std Dev 4.885
Gaus mean : 27.6479
Gaus Width: 3.8818
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

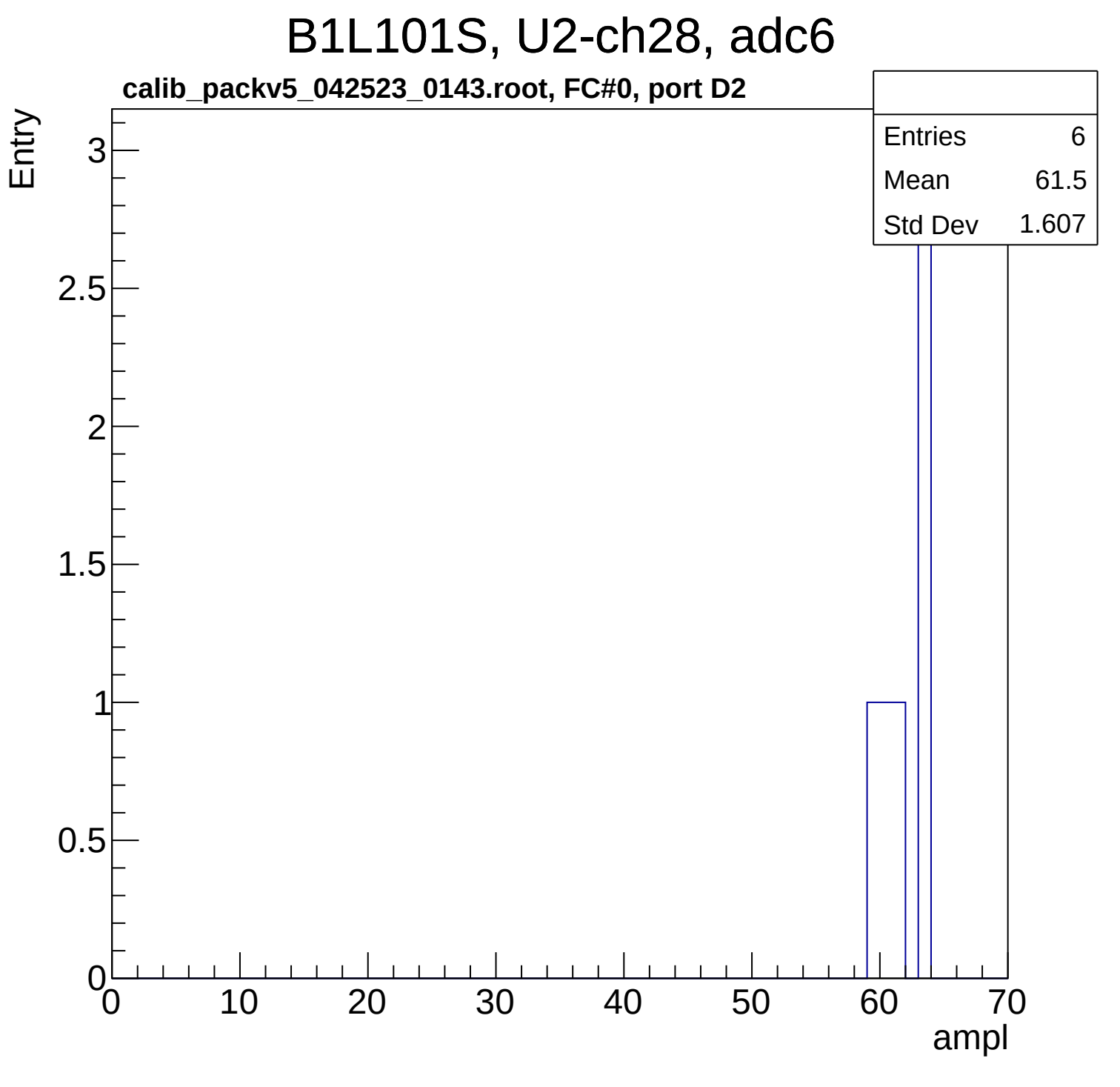

B1L101S, U2-ch28, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 34.8
Std Dev 3.822
Gaus mean : 35.2160
Gaus Width: 4.4159
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

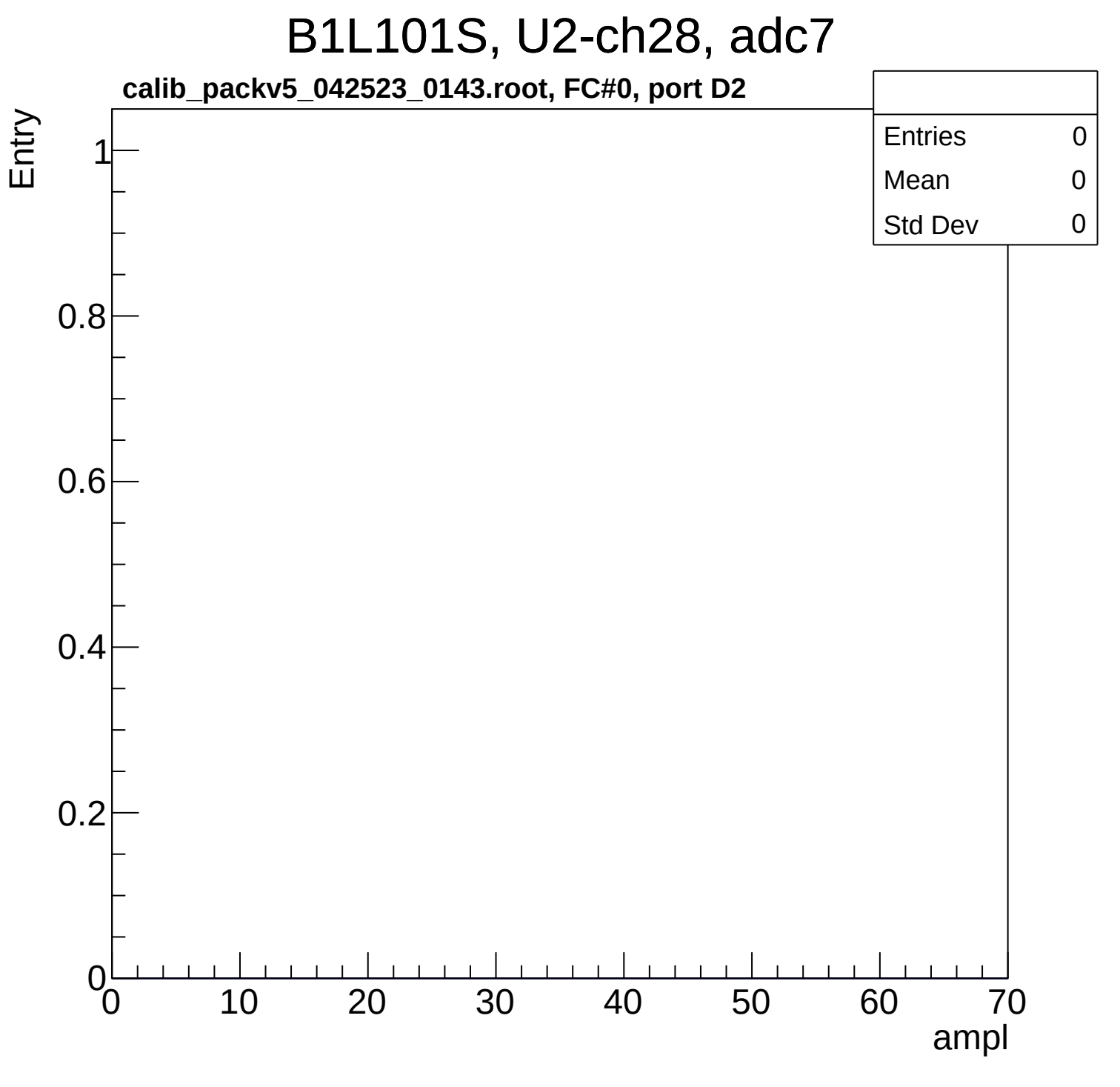

B1L101S, U2-ch28, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 41.53
Std Dev 3.733
Gaus mean : 41.7620
Gaus Width: 4.0945
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

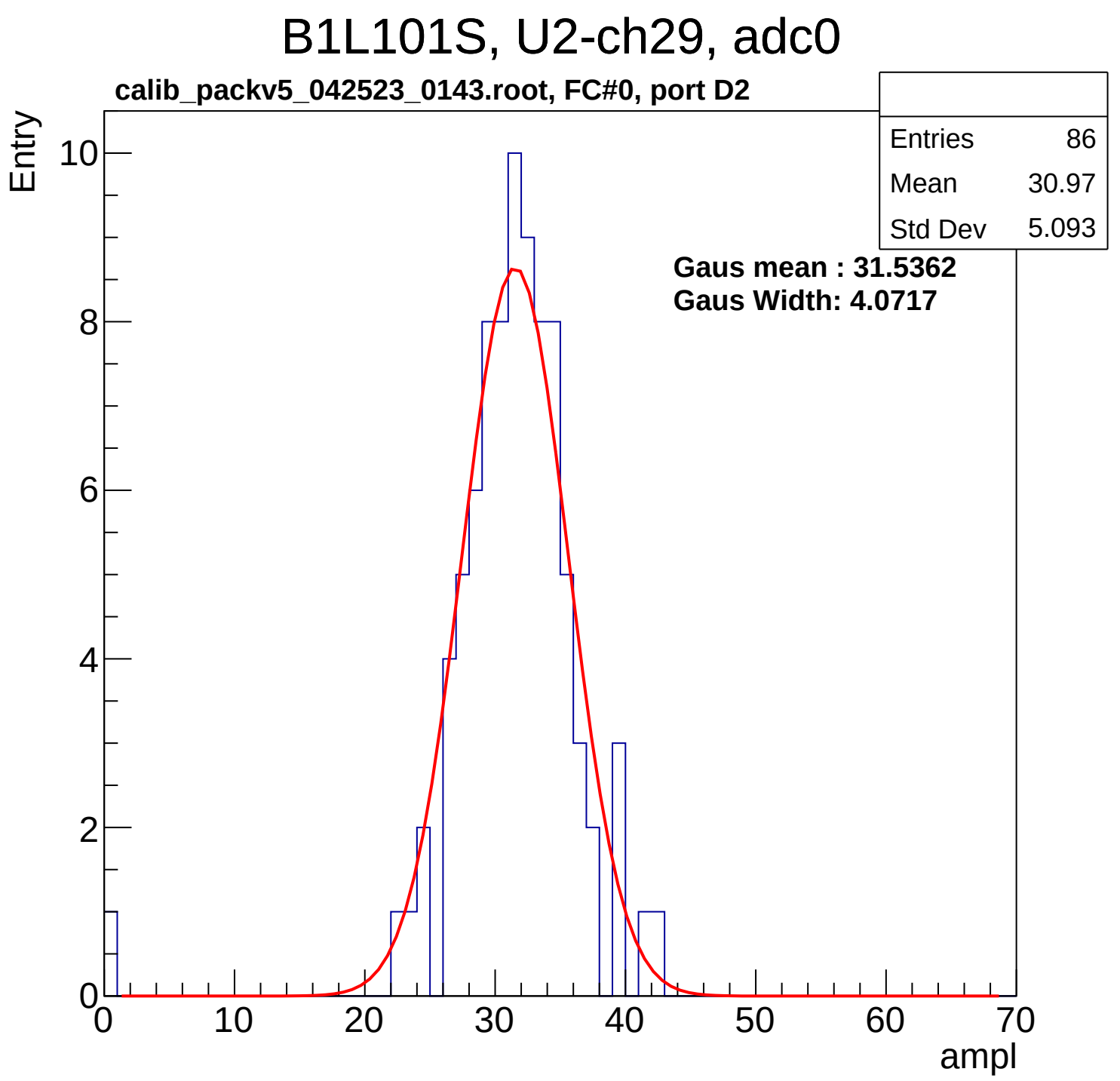

B1L101S, U2-ch28, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 46.86
Std Dev 3.802
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

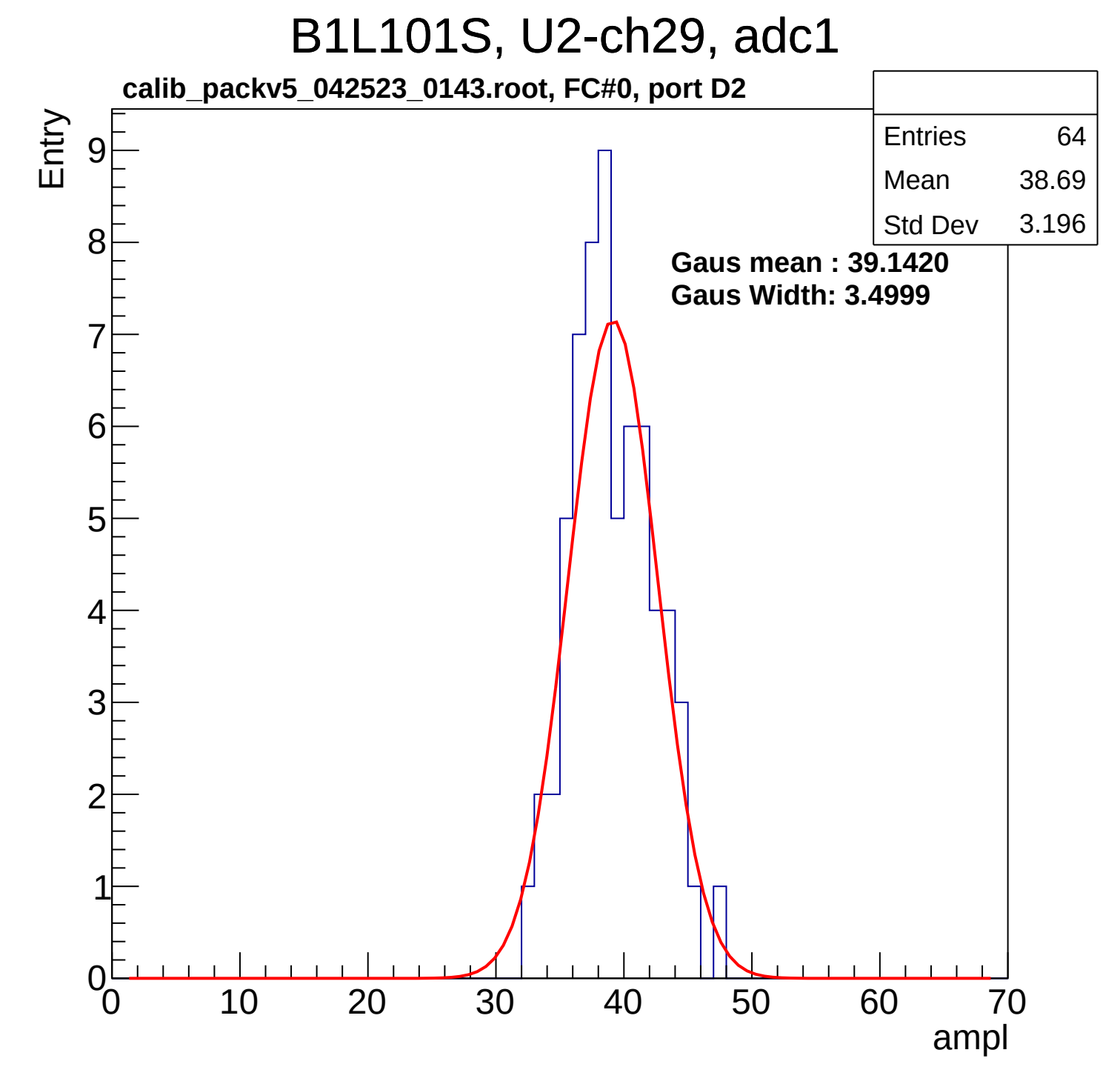

B1L101S, U2-ch28, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 52.68
Std Dev 3.364
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

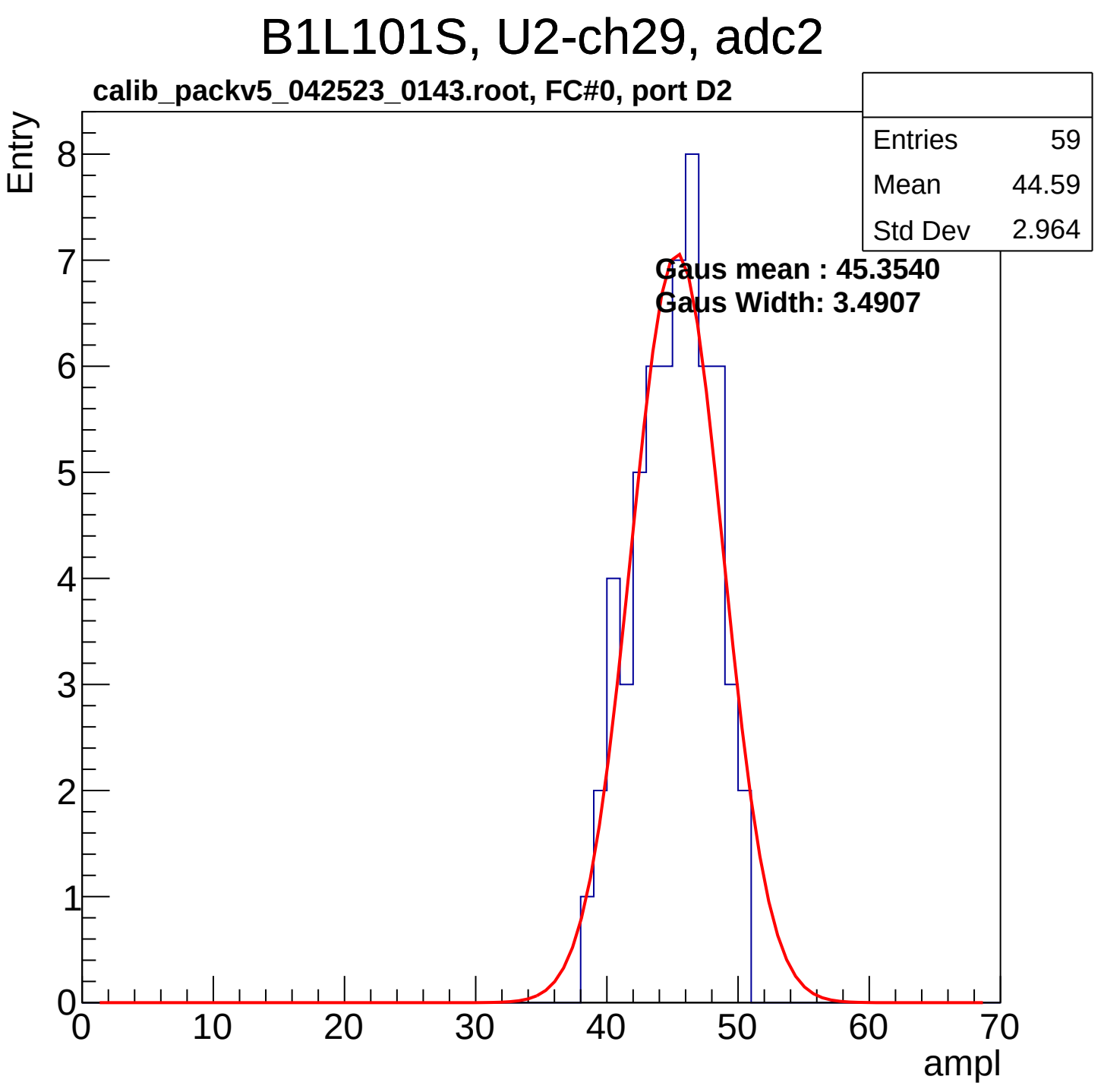

B1L101S, U2-ch28, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 58.4
Std Dev 7.603
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

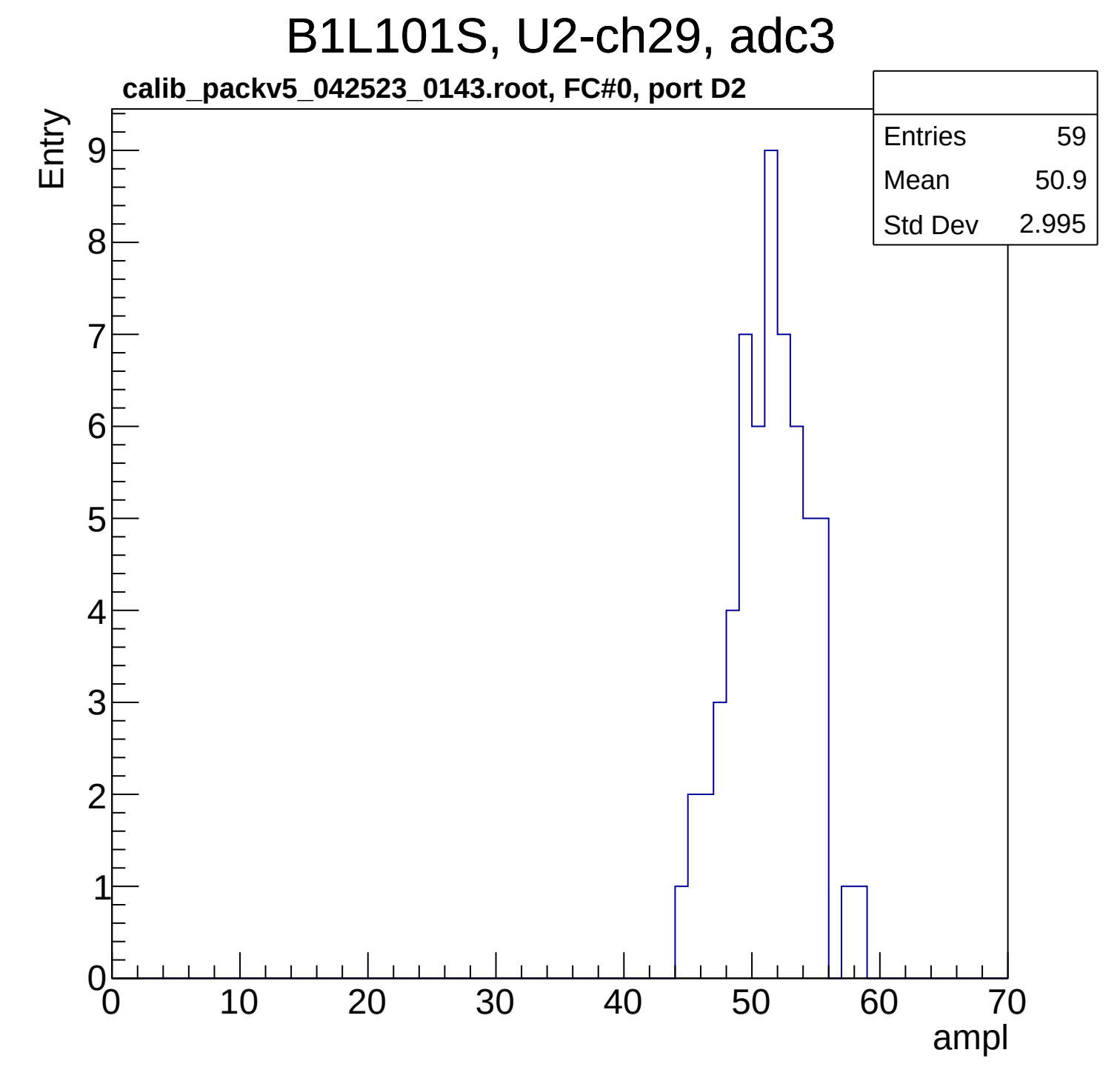

B1L101S, U2-ch28, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 61.5
Std Dev 1.607
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

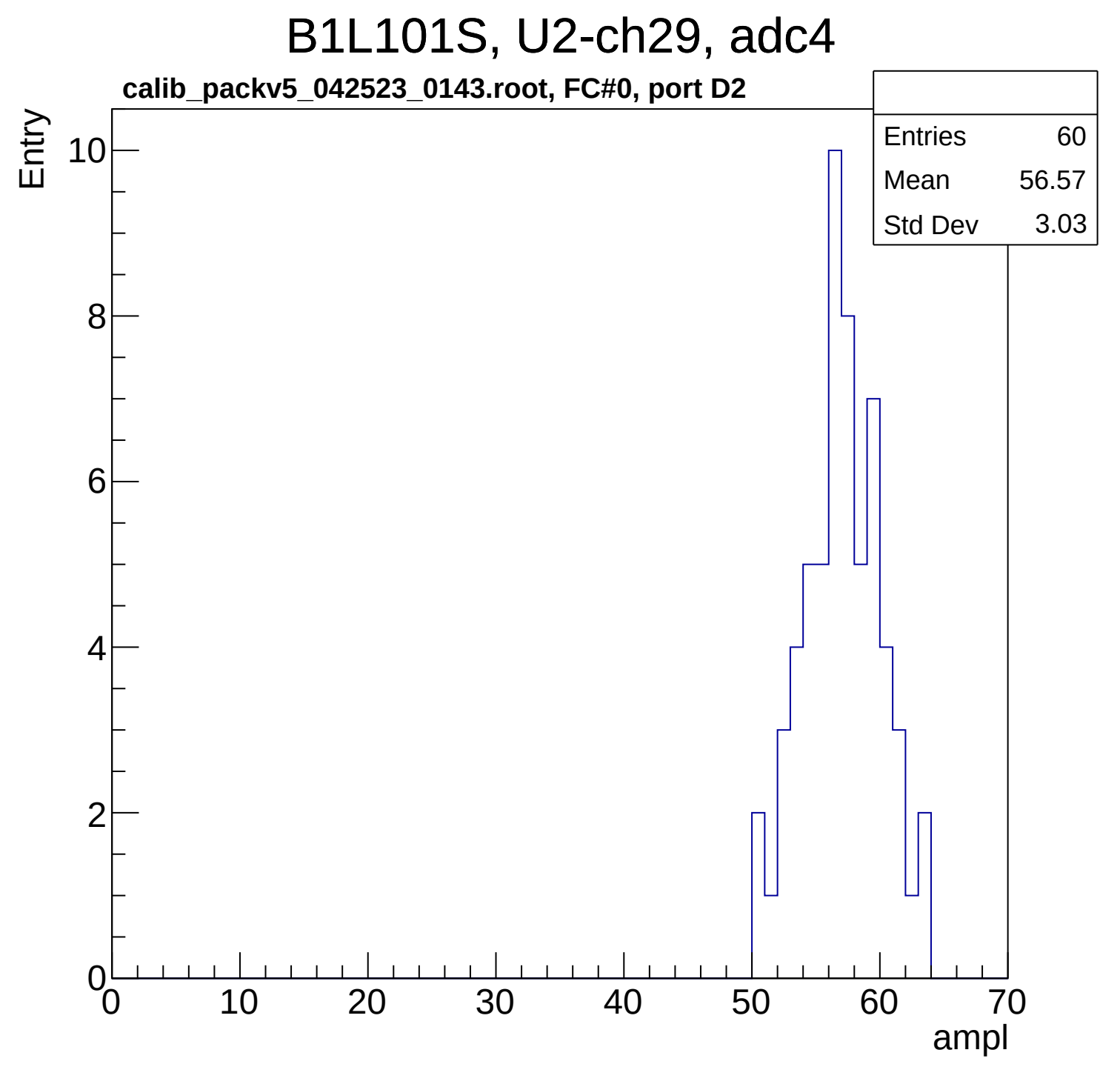

B1L101S, U2-ch28, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

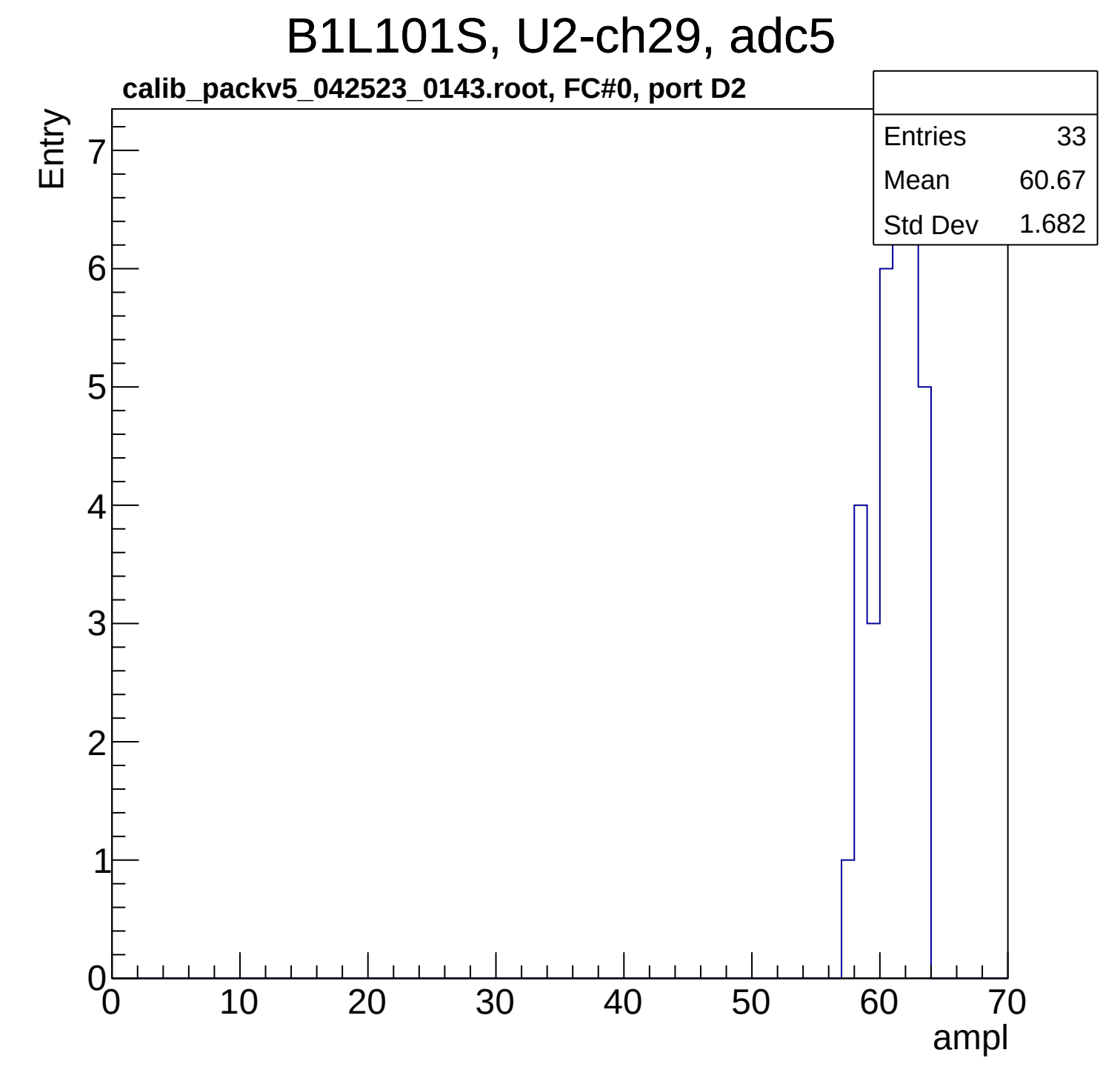

B1L101S, U2-ch29, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 86
Mean 30.97
Std Dev 5.093
Gaus mean : 31.5362
Gaus Width: 4.0717
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

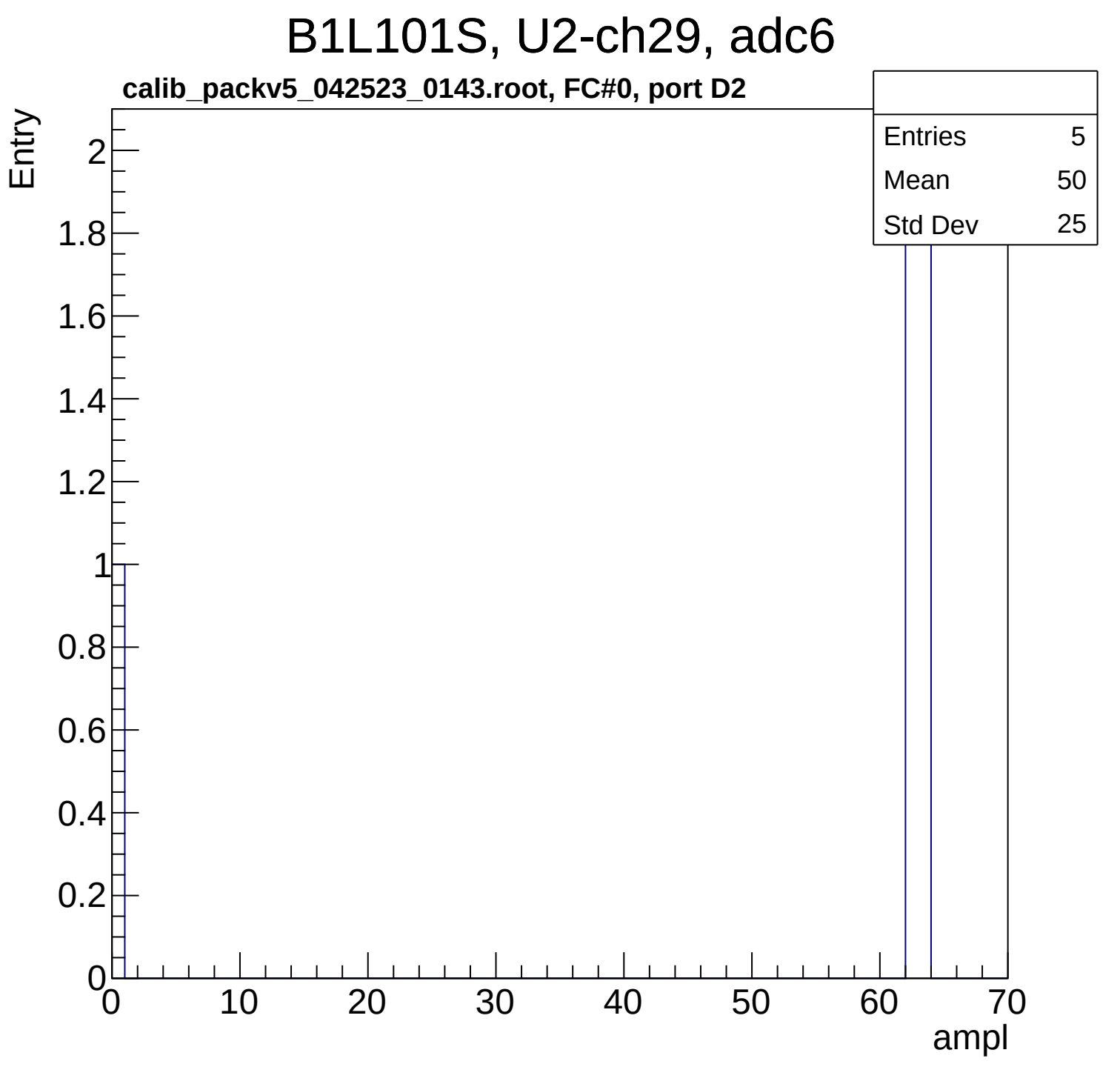

B1L101S, U2-ch29, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 38.69
Std Dev 3.196
Gaus mean : 39.1420
Gaus Width: 3.4999
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

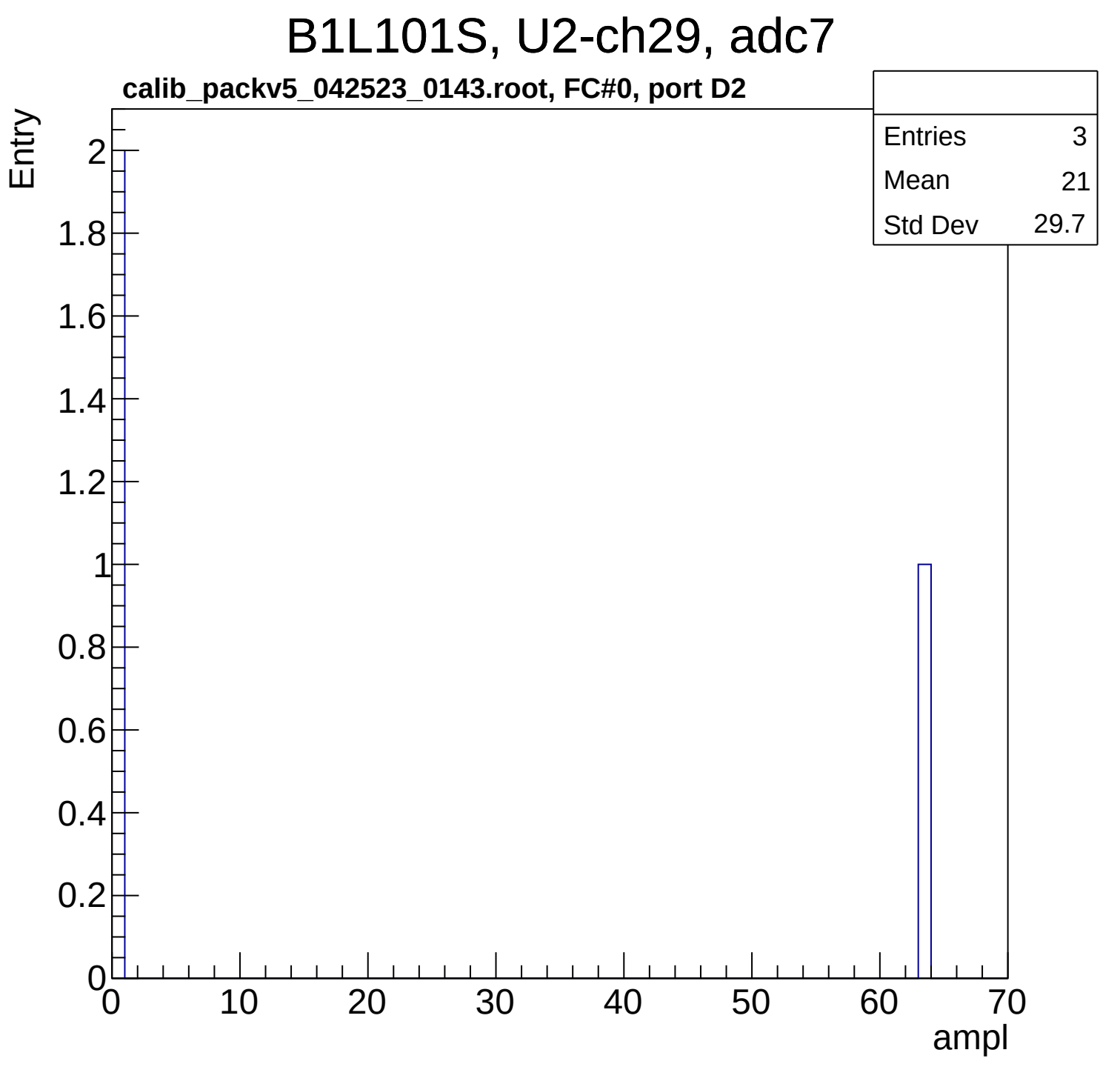

B1L101S, U2-ch29, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 44.59
Std Dev 2.964
Gaus mean : 45.3540
Gaus Width: 3.4907
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

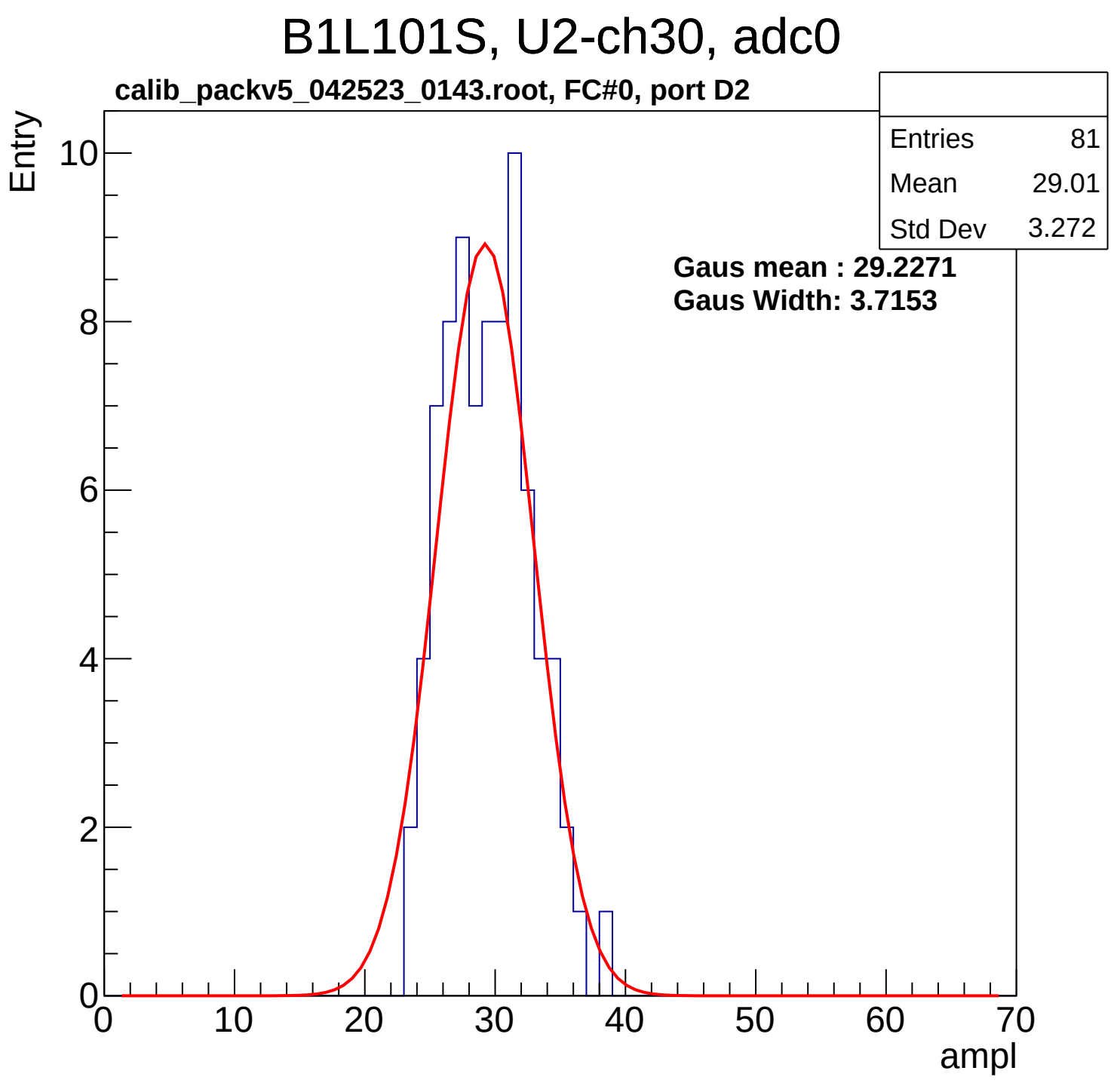

B1L101S, U2-ch29, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 50.9
Std Dev 2.995
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

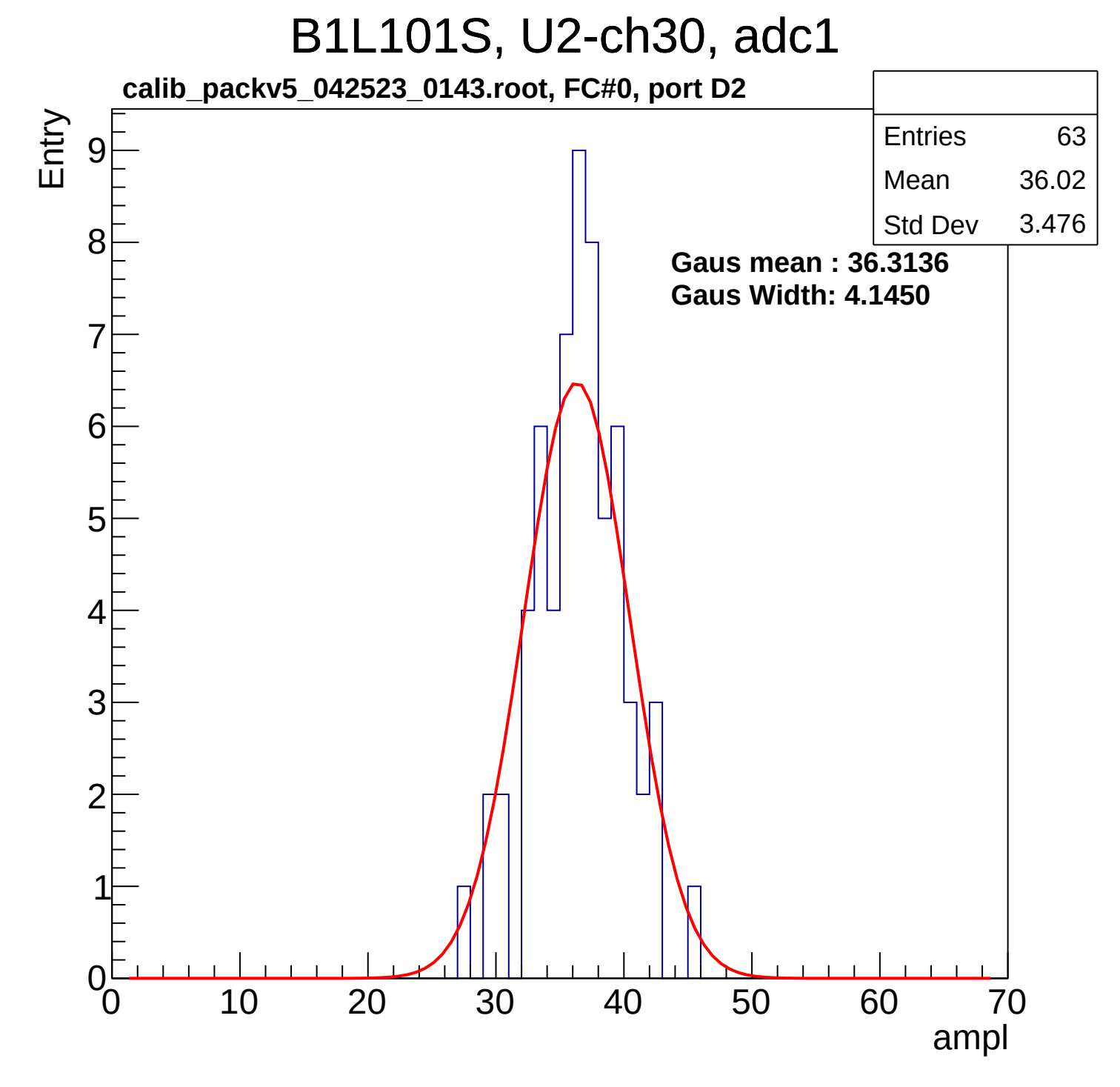

B1L101S, U2-ch29, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 56.57
Std Dev 3.03
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

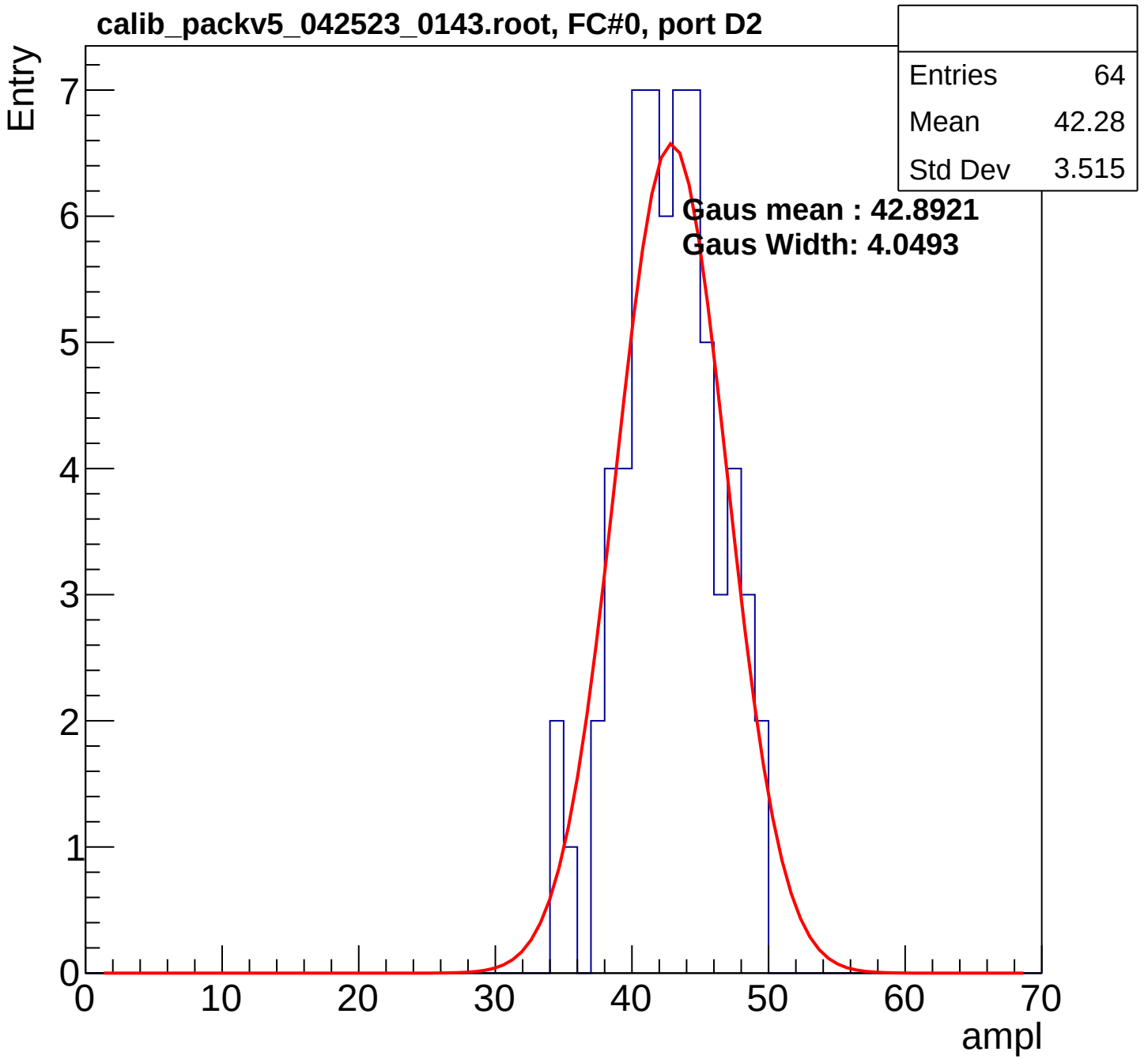

B1L101S, U2-ch29, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 33
Mean 60.67
Std Dev 1.682
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

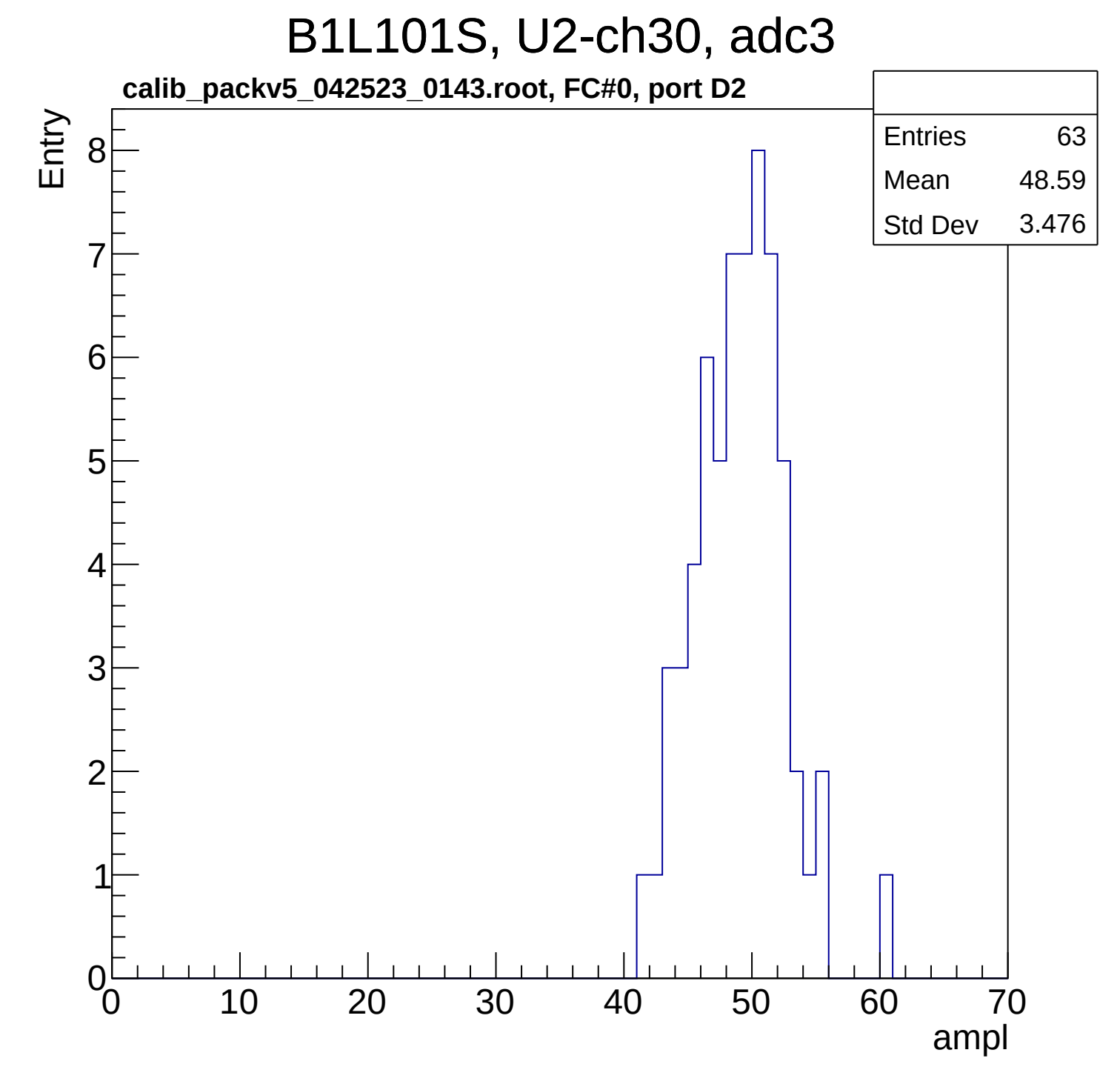

B1L101S, U2-ch29, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 50
Std Dev 25
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

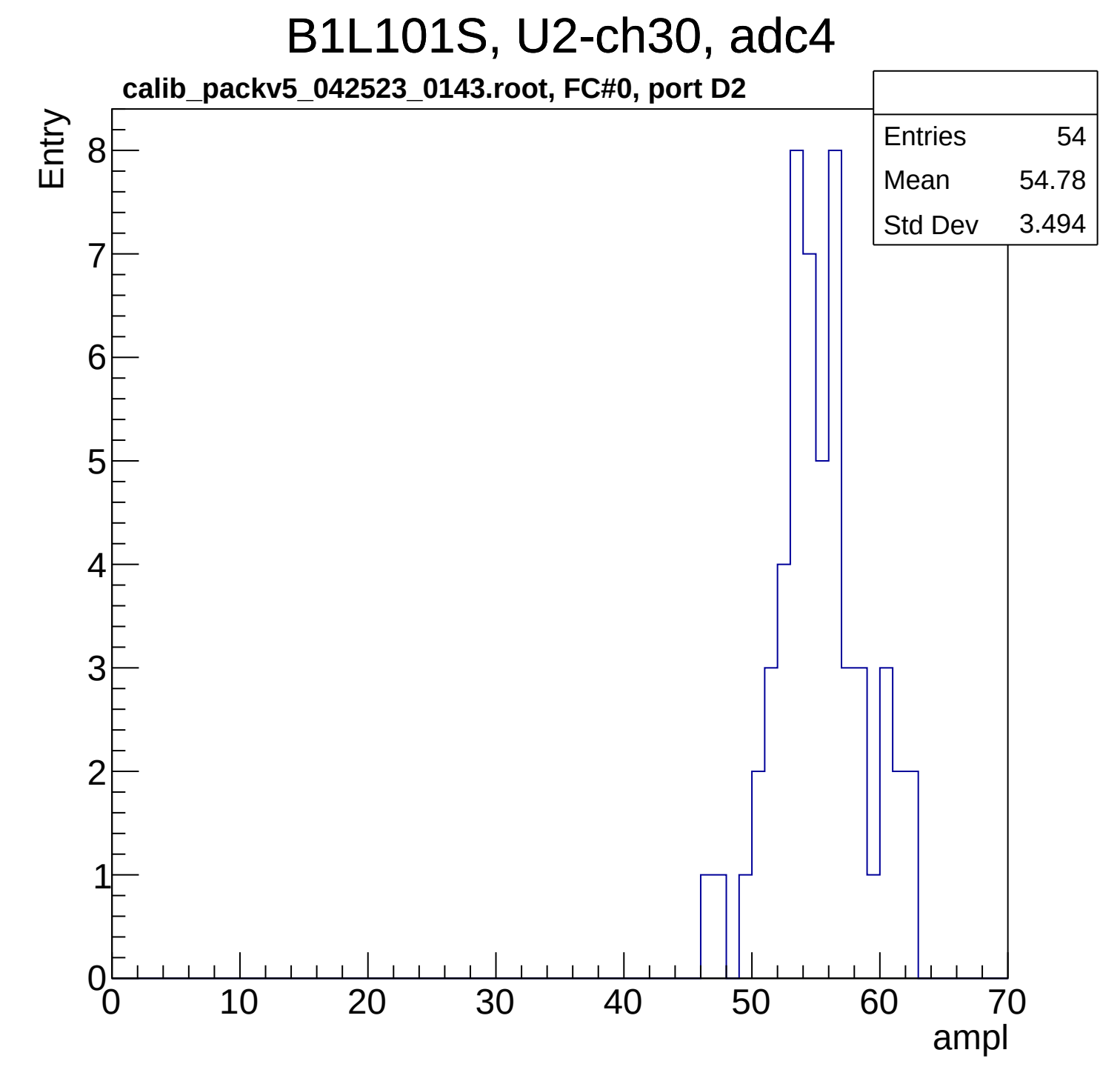

B1L101S, U2-ch29, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 21
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

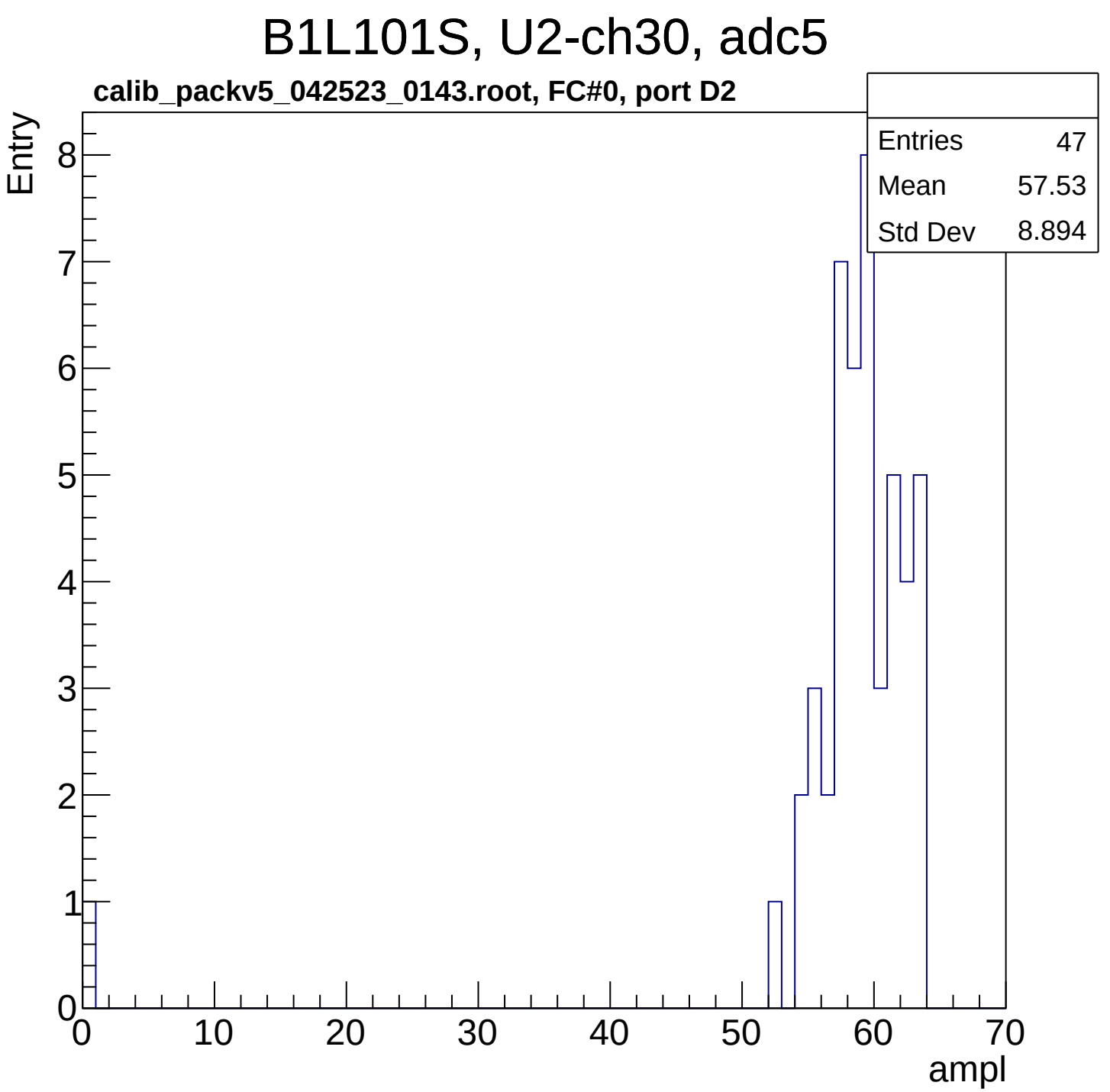

B1L101S, U2-ch30, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 81
Mean 29.01
Std Dev 3.272
Gaus mean : 29.2271
Gaus Width: 3.7153
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

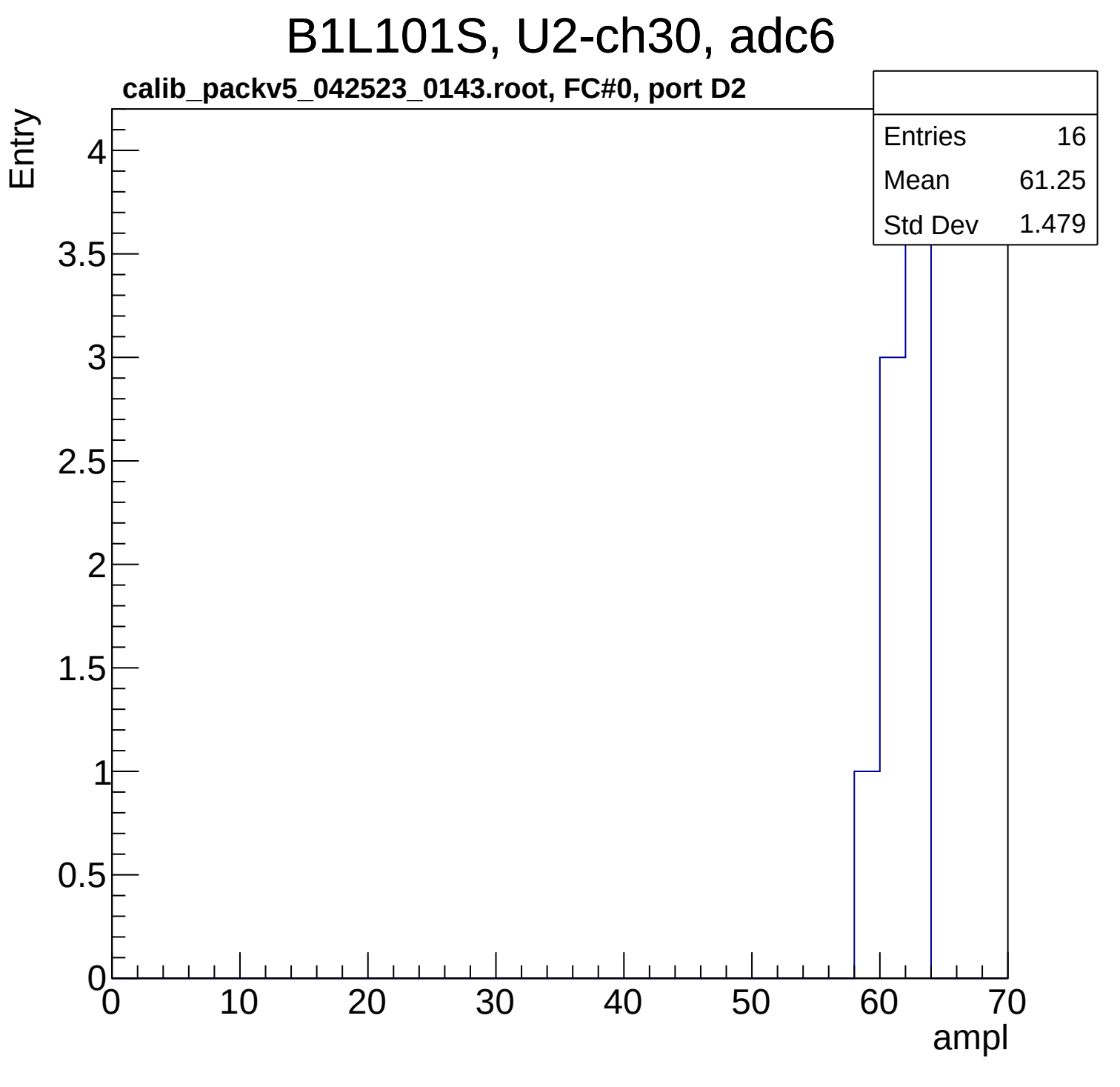

B1L101S, U2-ch30, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 36.02
Std Dev 3.476
Gaus mean : 36.3136
Gaus Width: 4.1450
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

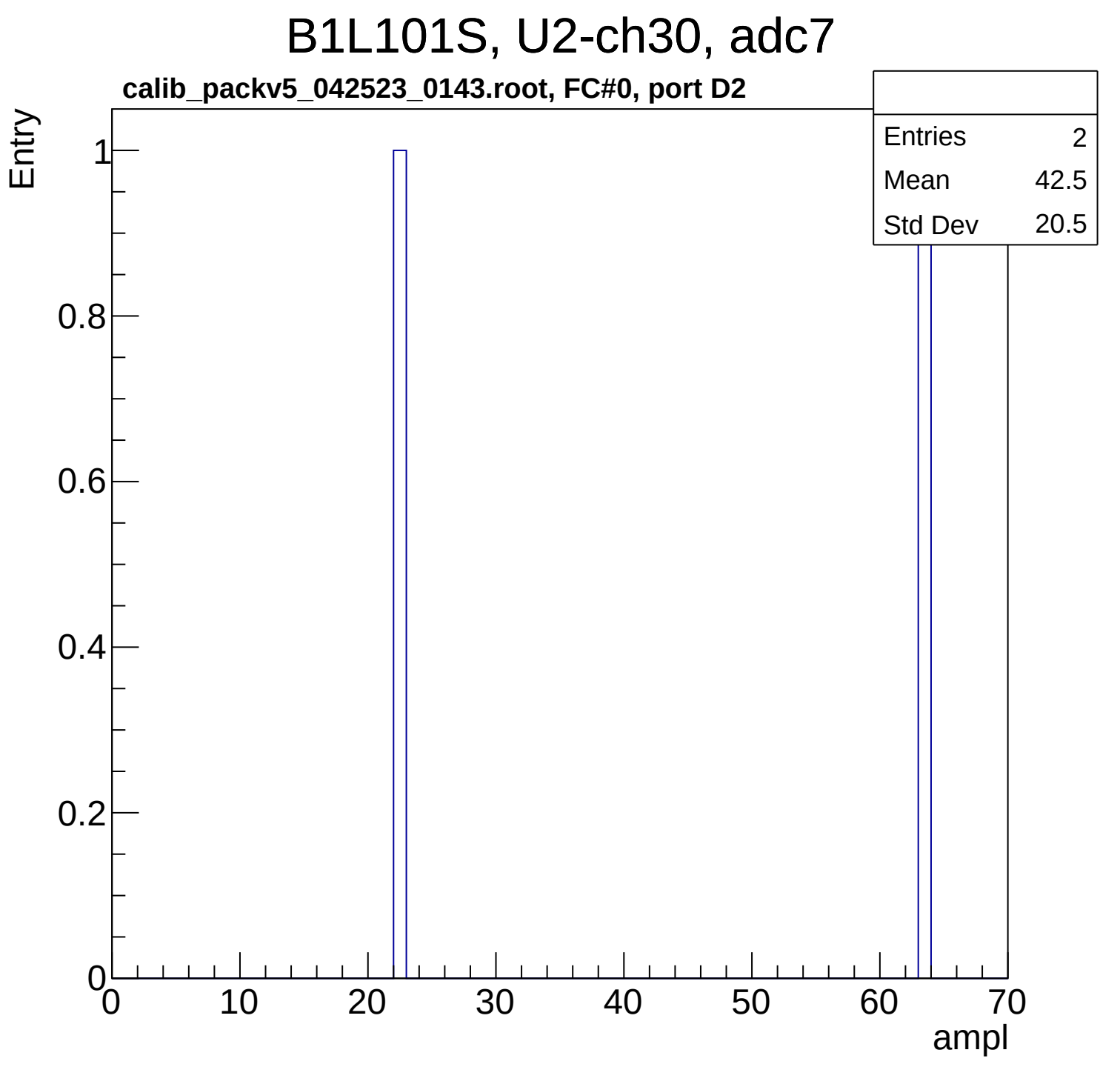

B1L101S, U2-ch30, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 42.28
Std Dev 3.515
Gaus mean : 42.8921
Gaus Width: 4.0493
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

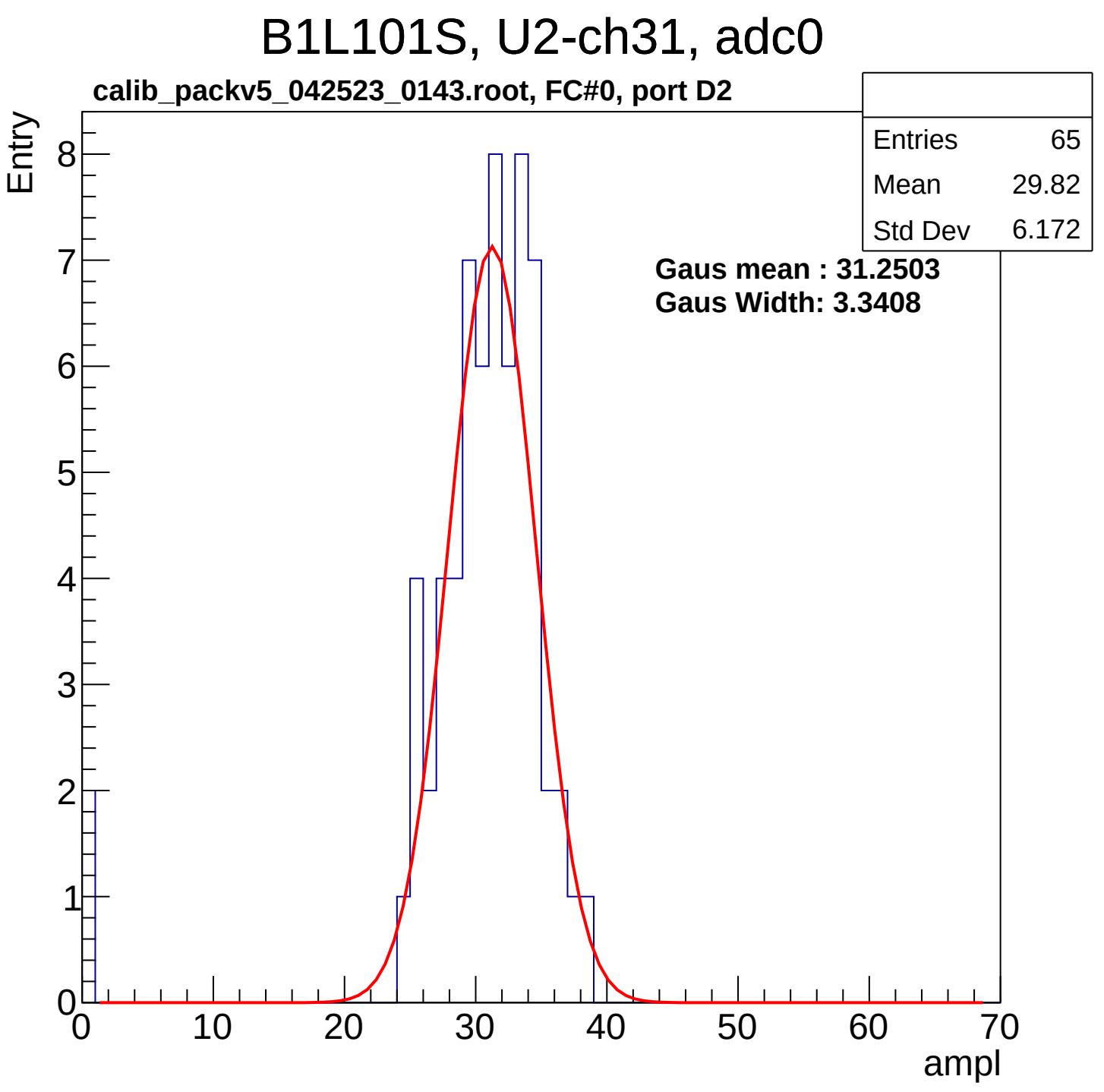

B1L101S, U2-ch30, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 48.59
Std Dev 3.476
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

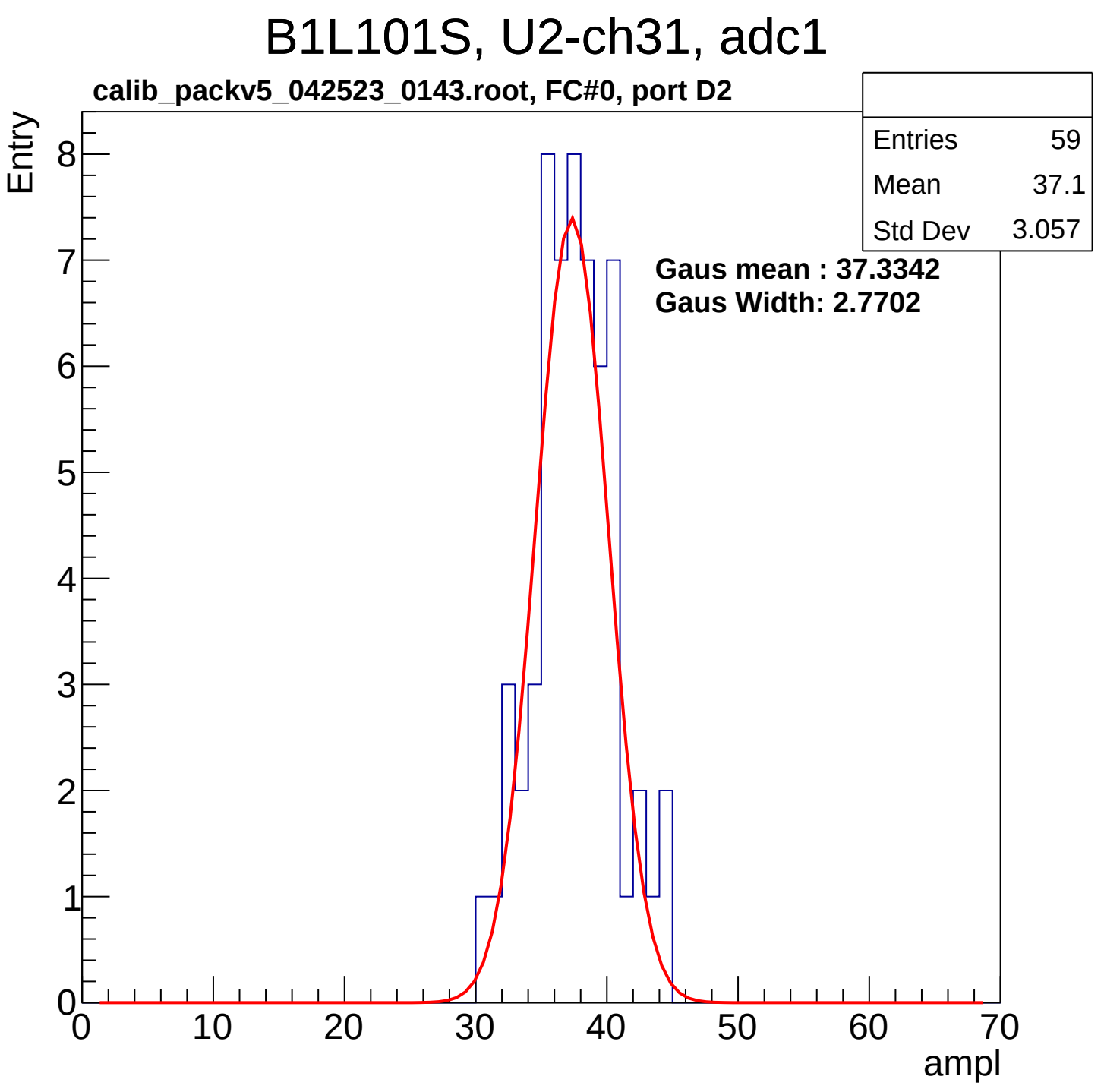

B1L101S, U2-ch30, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 54.78
Std Dev 3.494
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

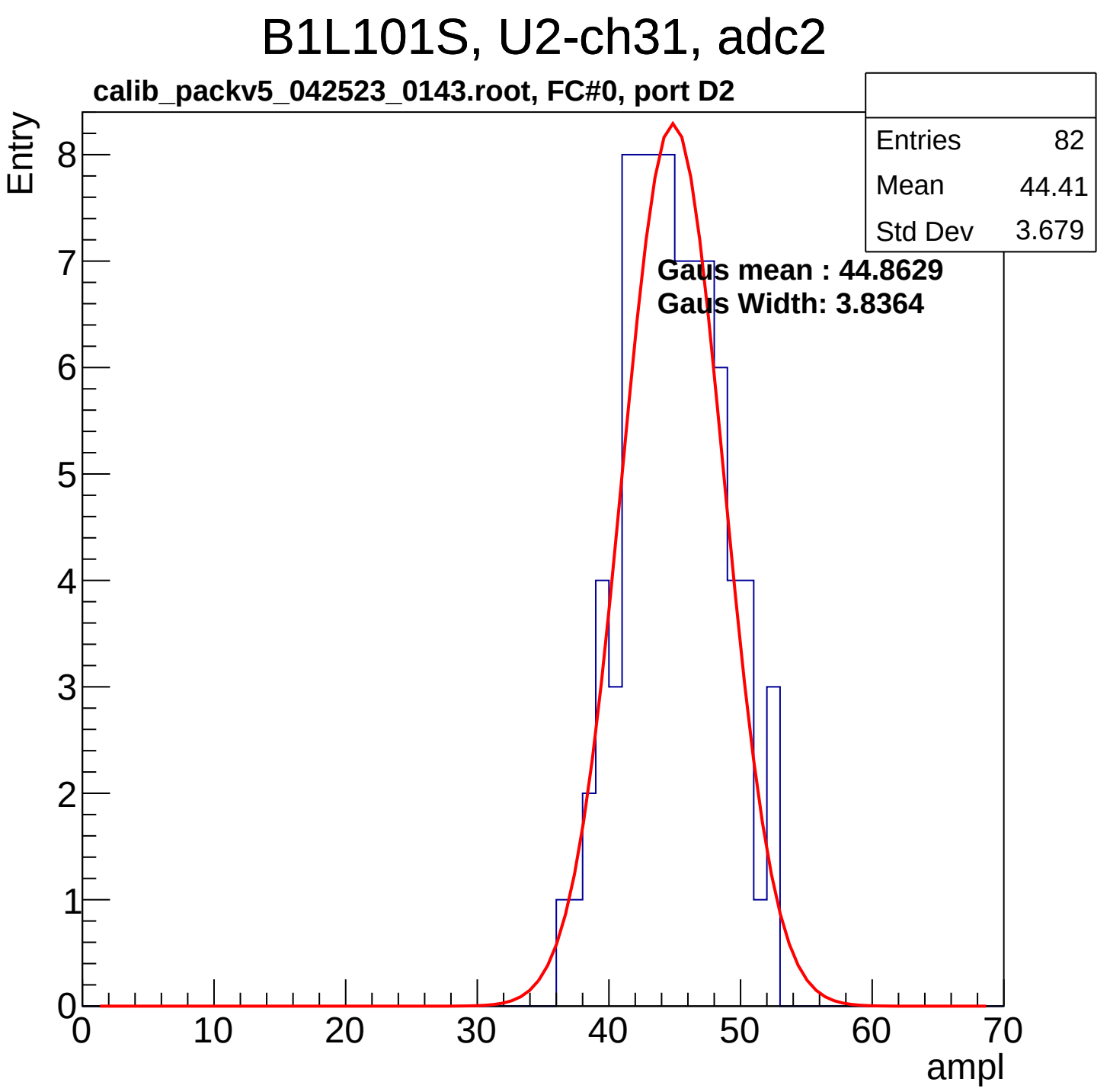

B1L101S, U2-ch30, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 57.53
Std Dev 8.894
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

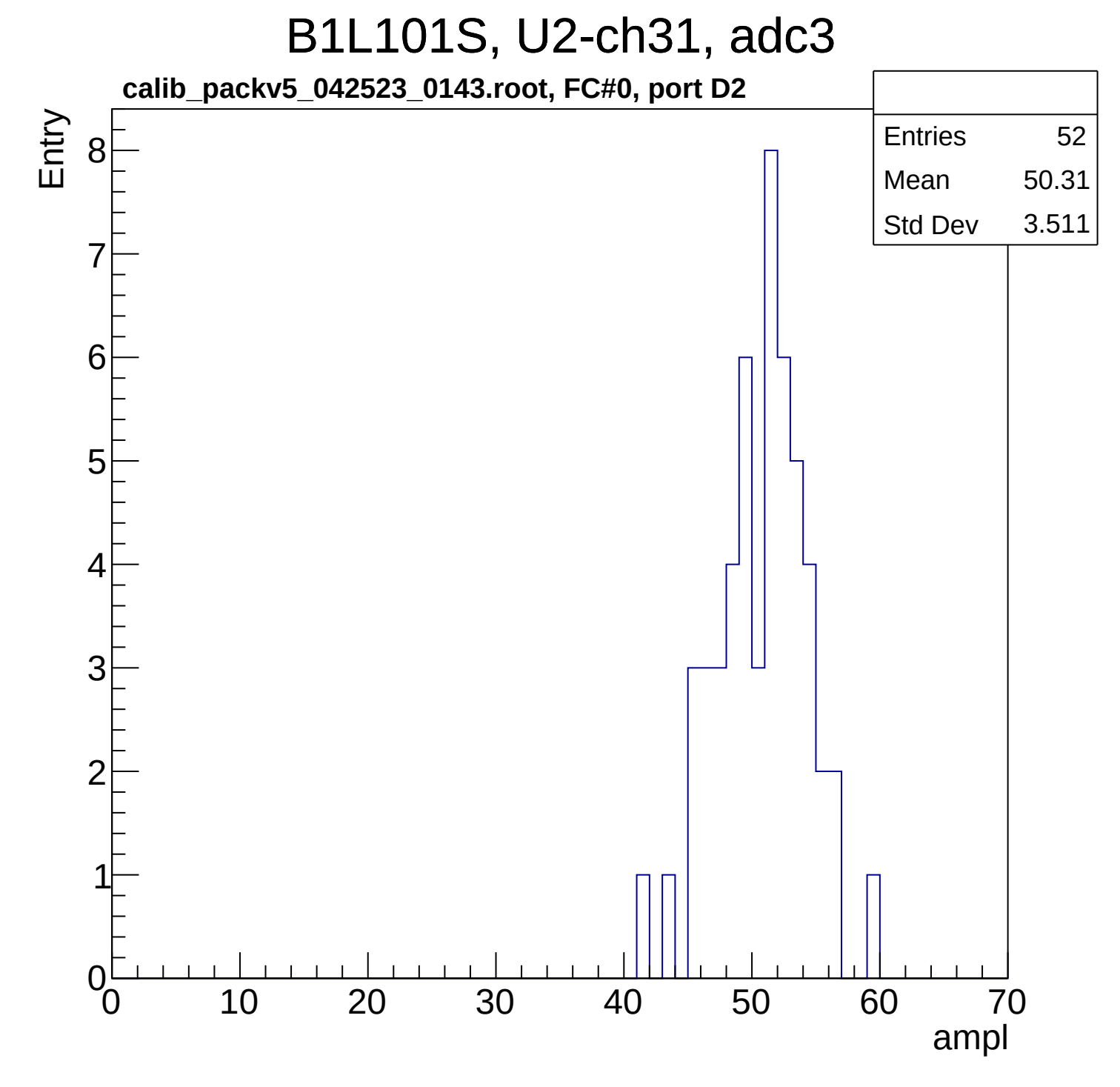

B1L101S, U2-ch30, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 16
Mean 61.25
Std Dev 1.479
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

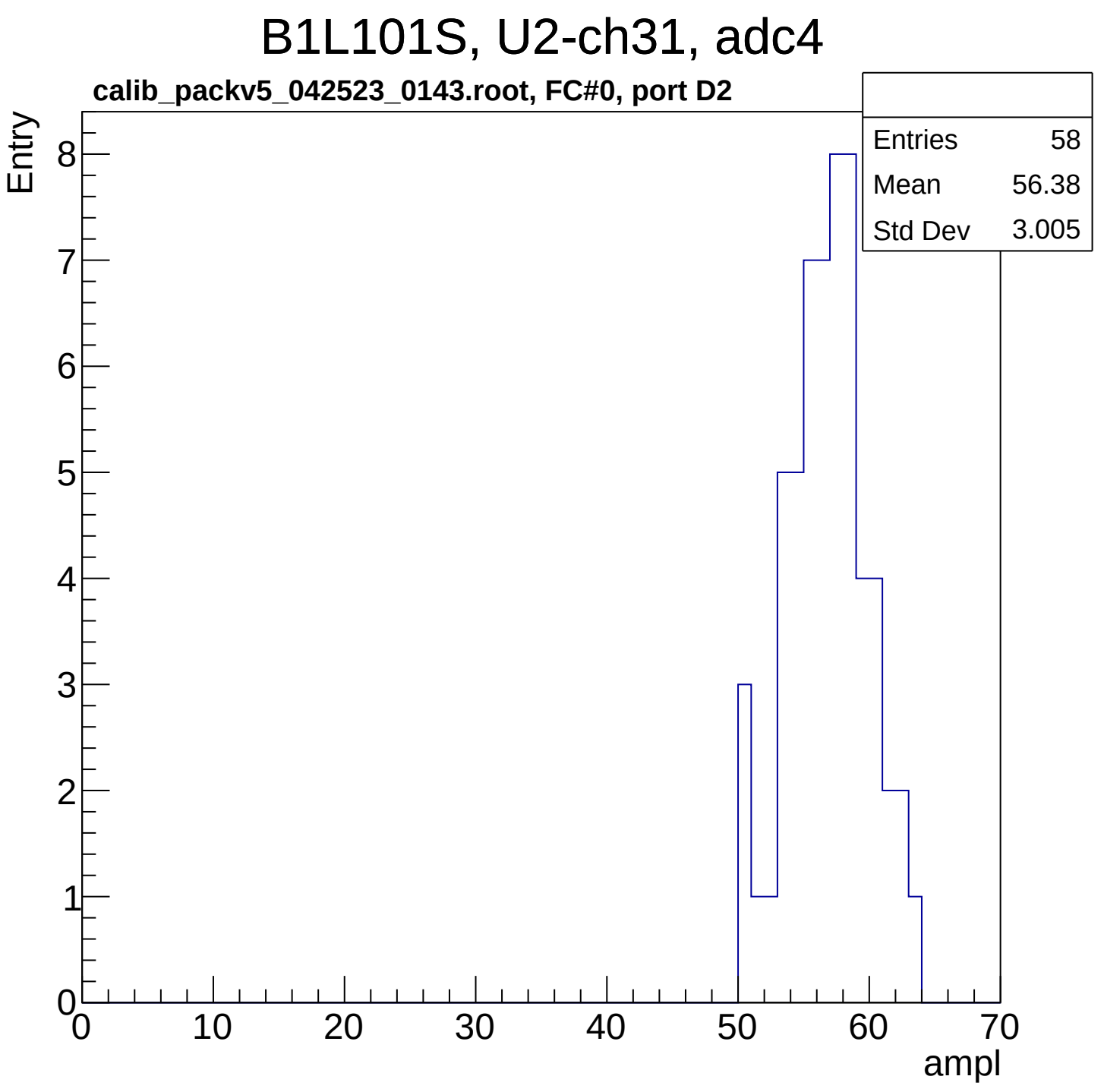

B1L101S, U2-ch30, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 42.5
Std Dev 20.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

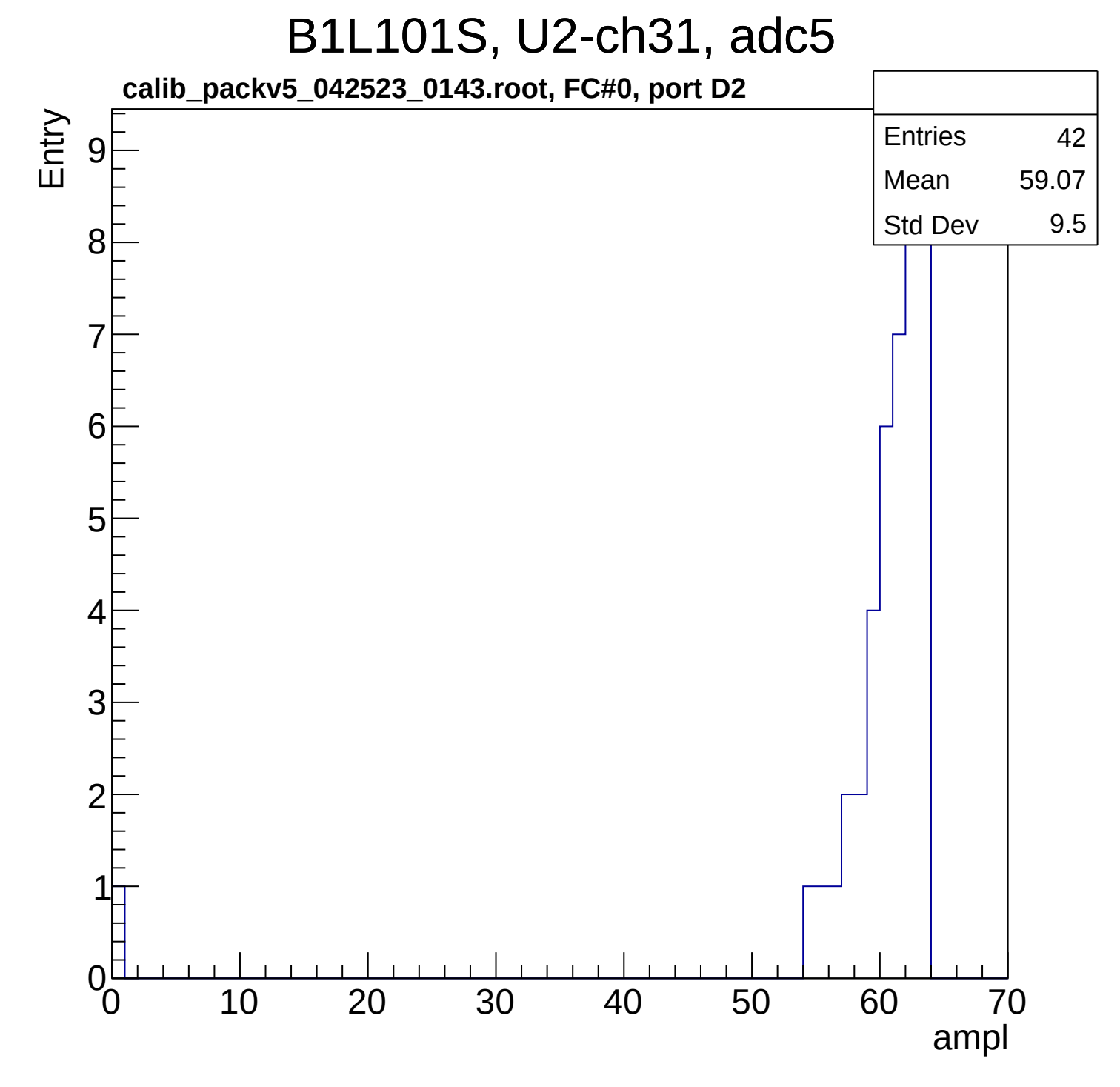

B1L101S, U2-ch31, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 29.82
Std Dev 6.172
Gaus mean : 31.2503
Gaus Width: 3.3408
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

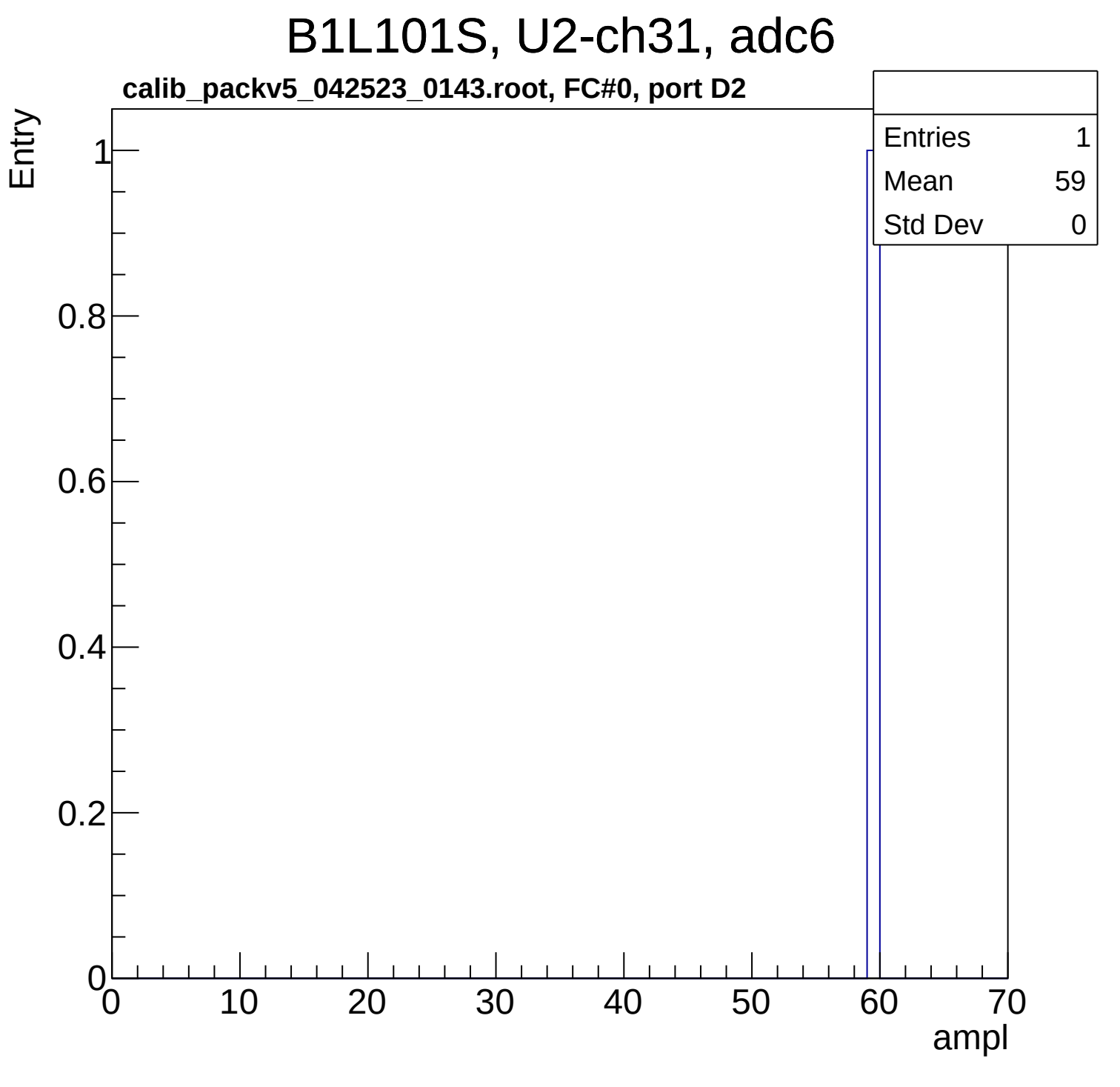

B1L101S, U2-ch31, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 37.1
Std Dev 3.057
Gaus mean : 37.3342
Gaus Width: 2.7702
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

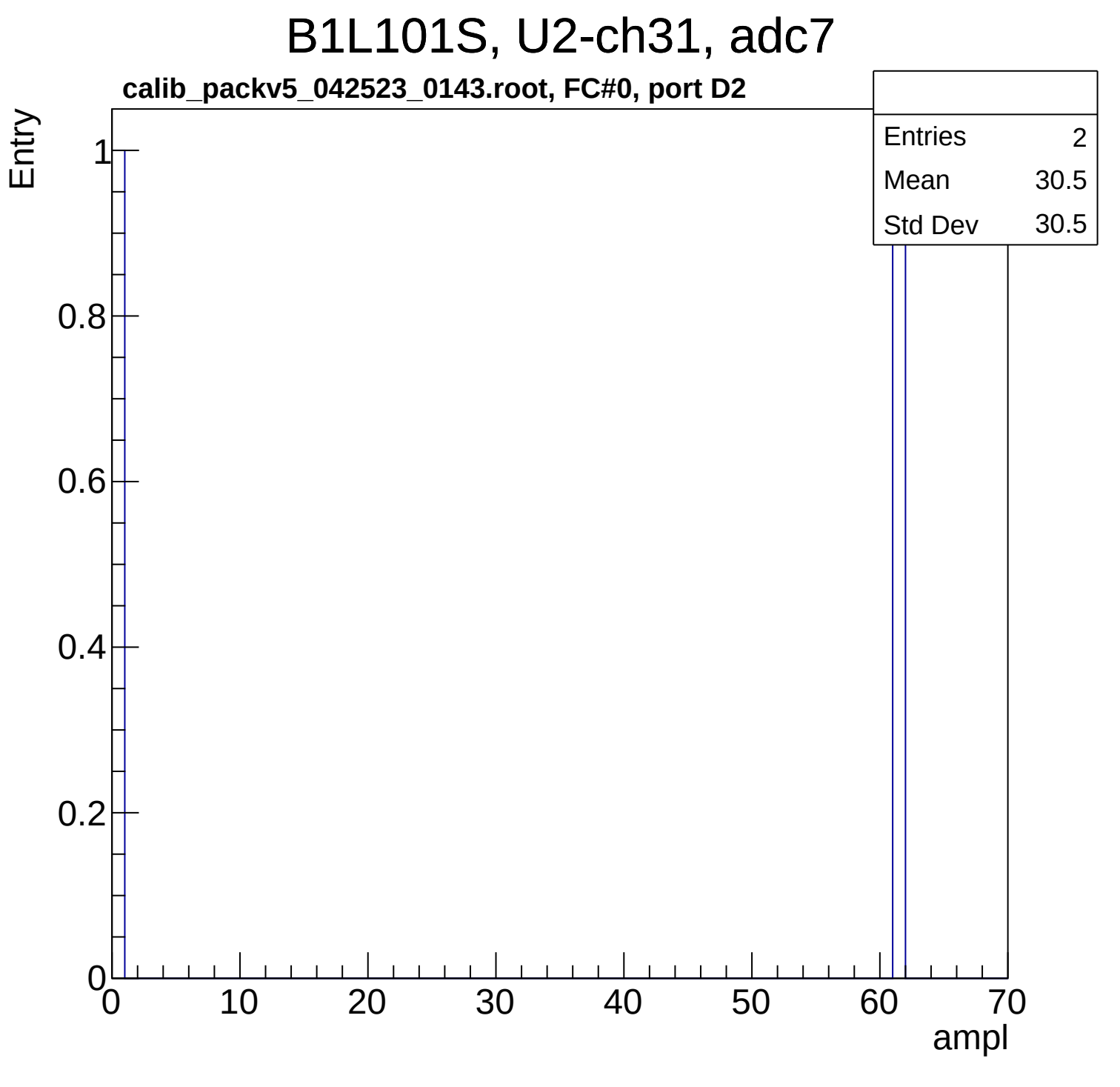

B1L101S, U2-ch31, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 82
Mean 44.41
Std Dev 3.679
Gaus mean : 44.8629
Gaus Width: 3.8364
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

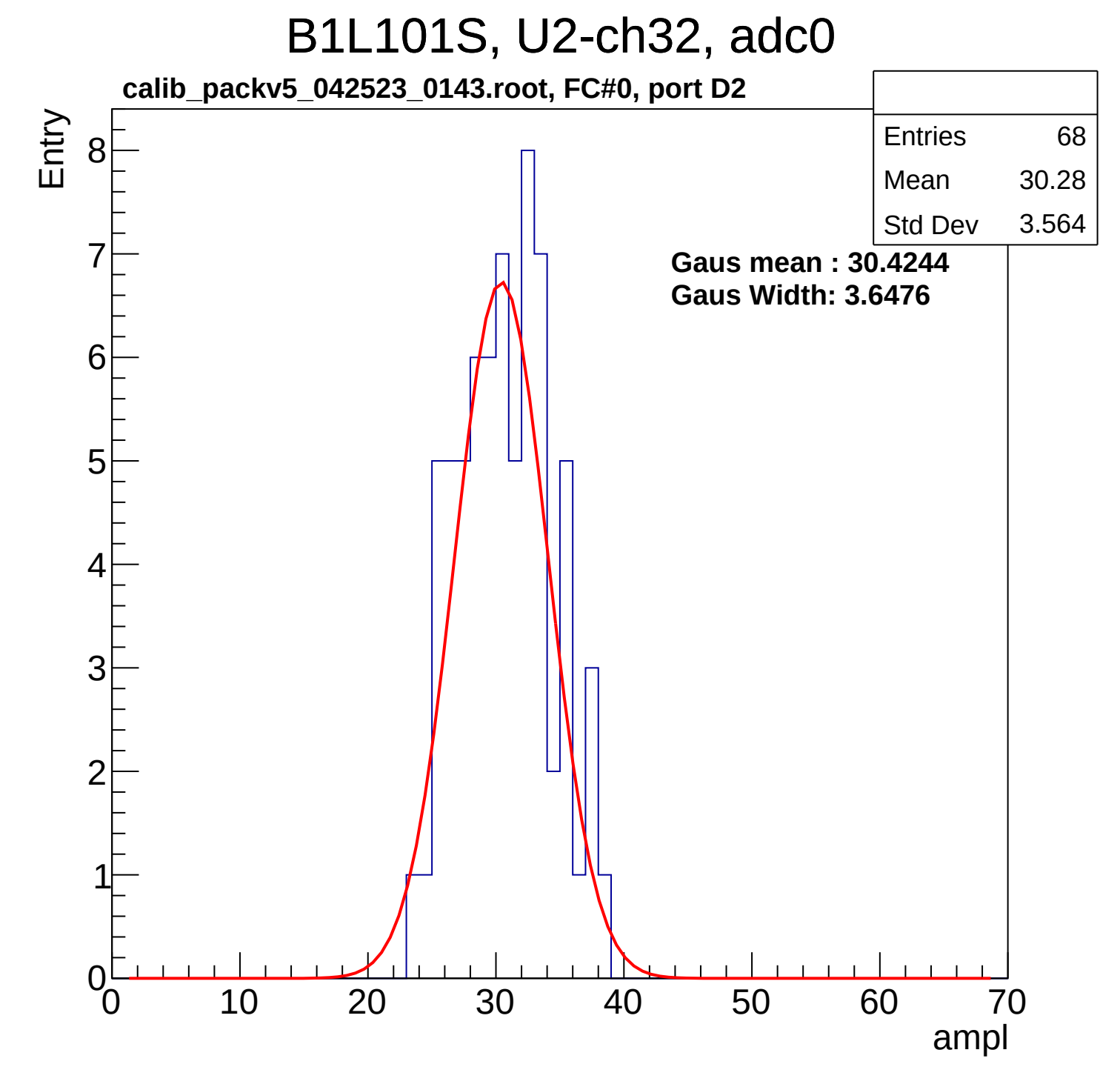

B1L101S, U2-ch31, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 50.31
Std Dev 3.511
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

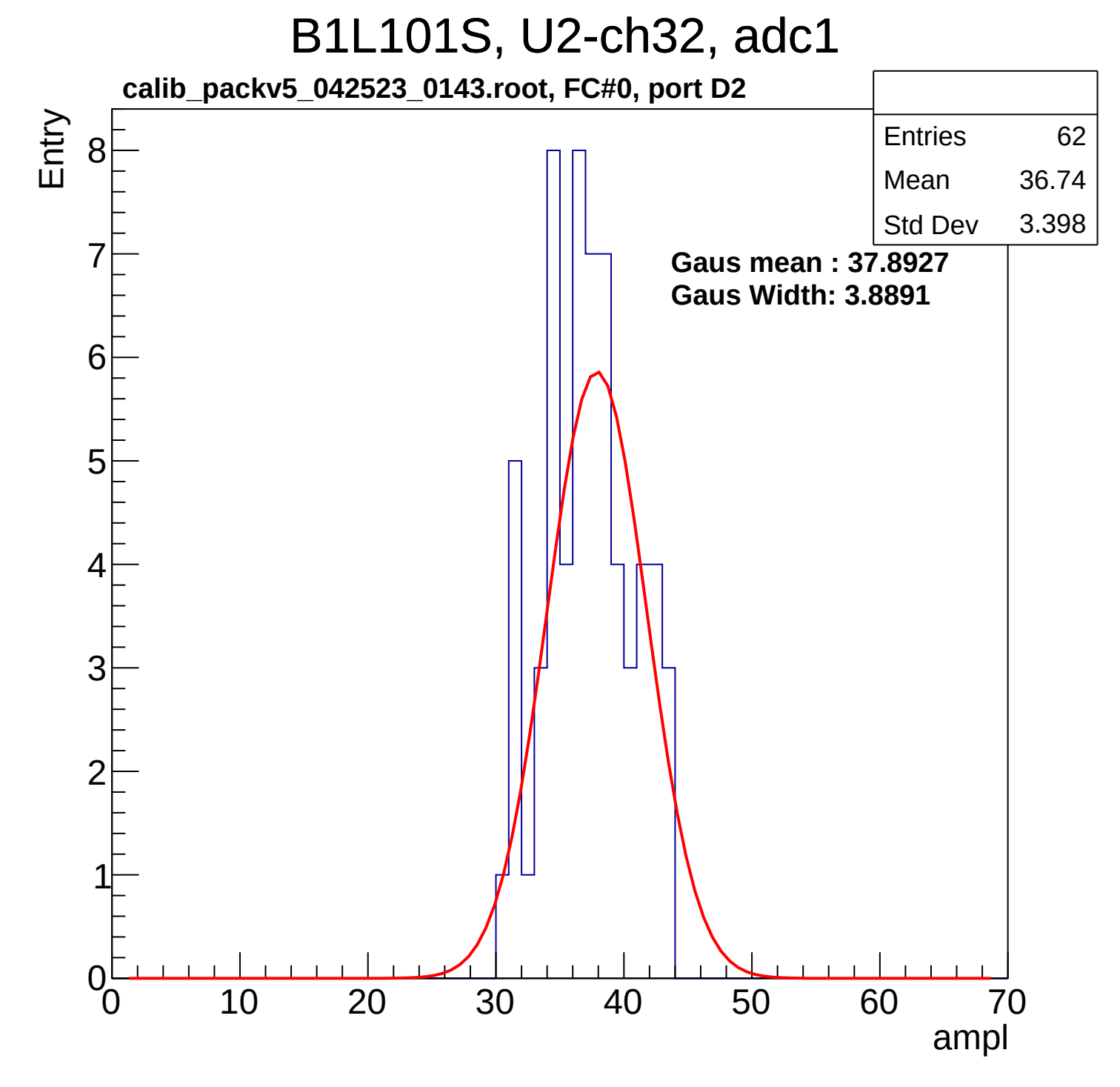

B1L101S, U2-ch31, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 56.38
Std Dev 3.005
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

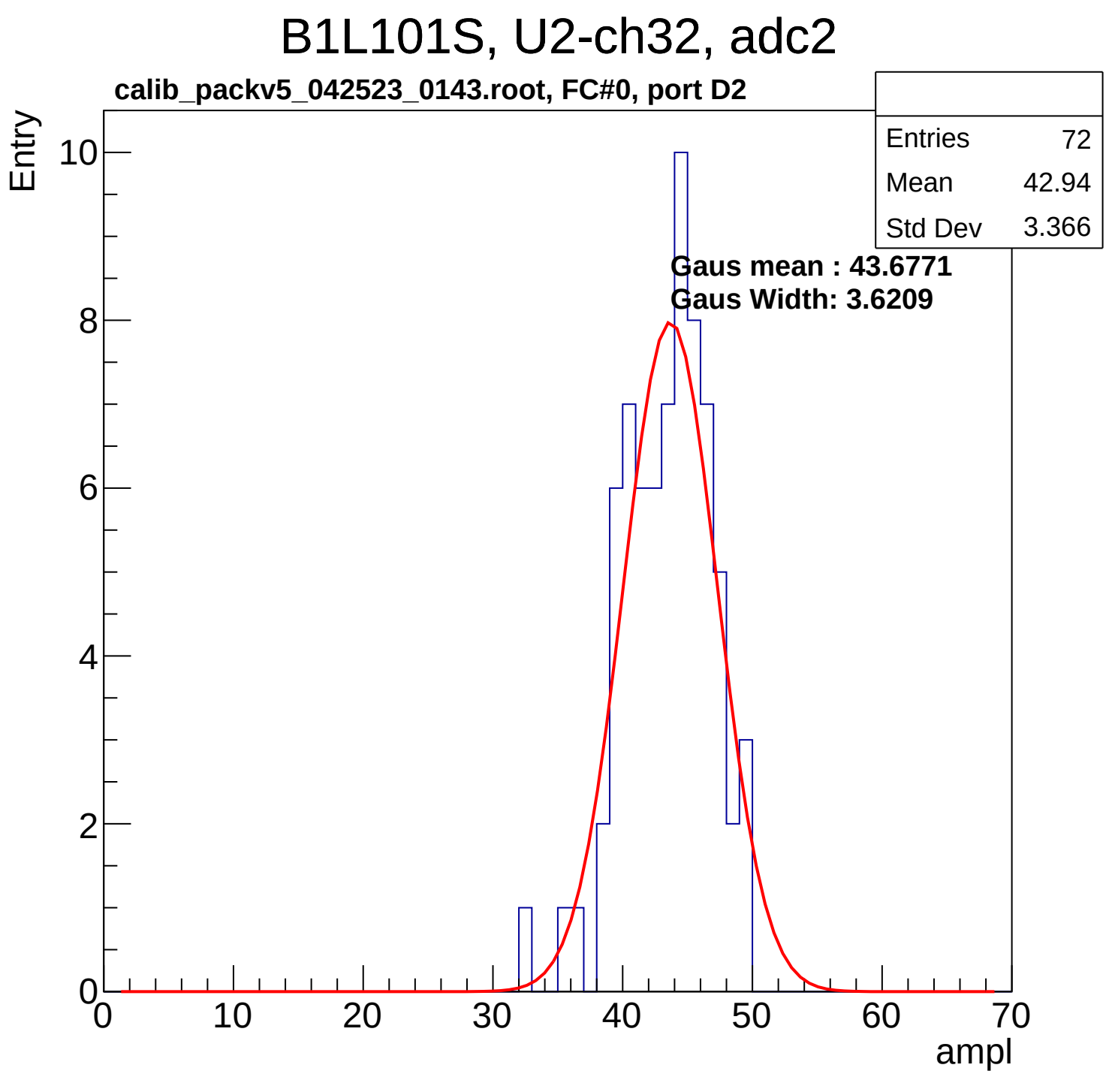

B1L101S, U2-ch31, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 59.07
Std Dev 9.5
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

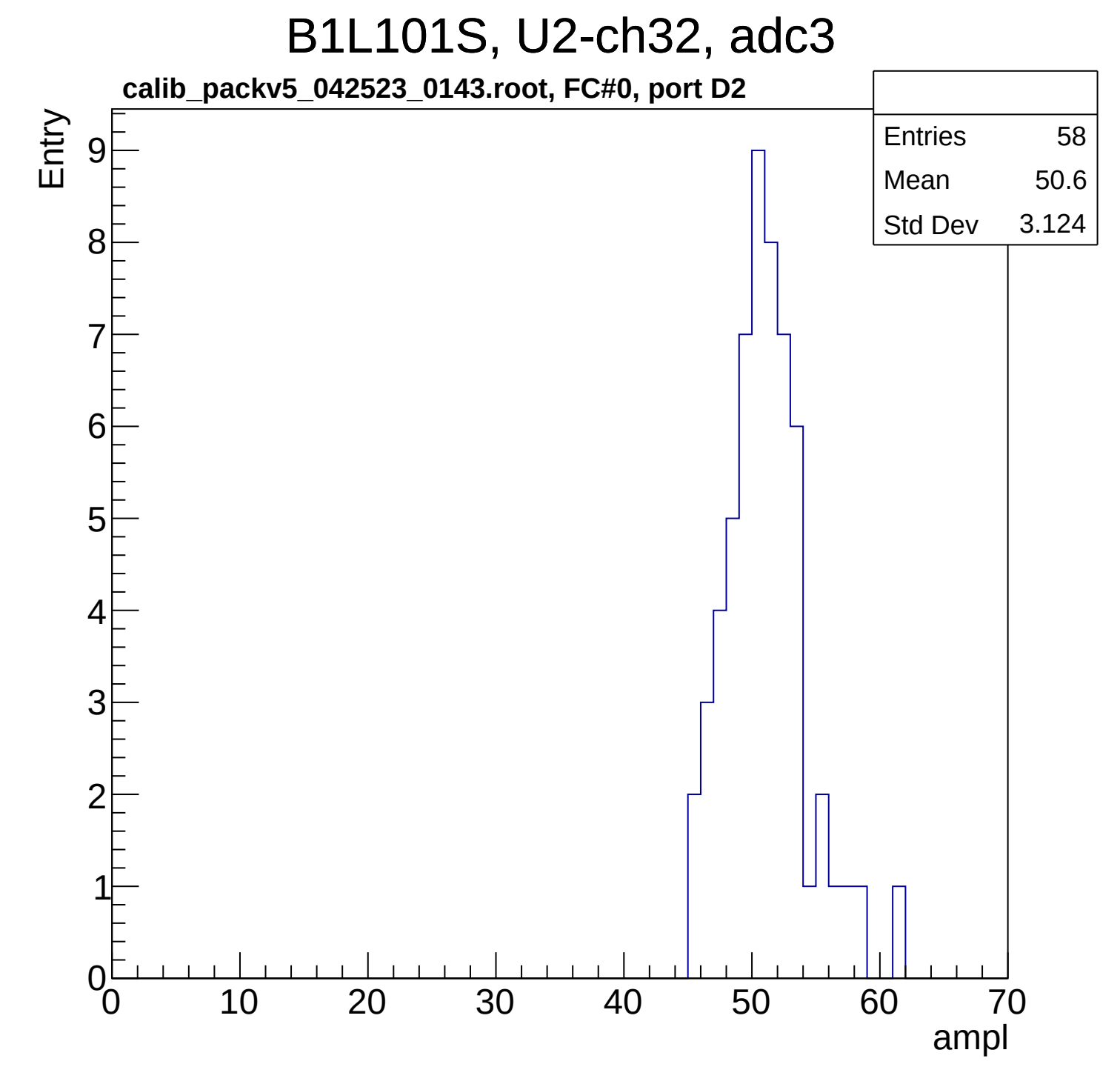

B1L101S, U2-ch31, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 59
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

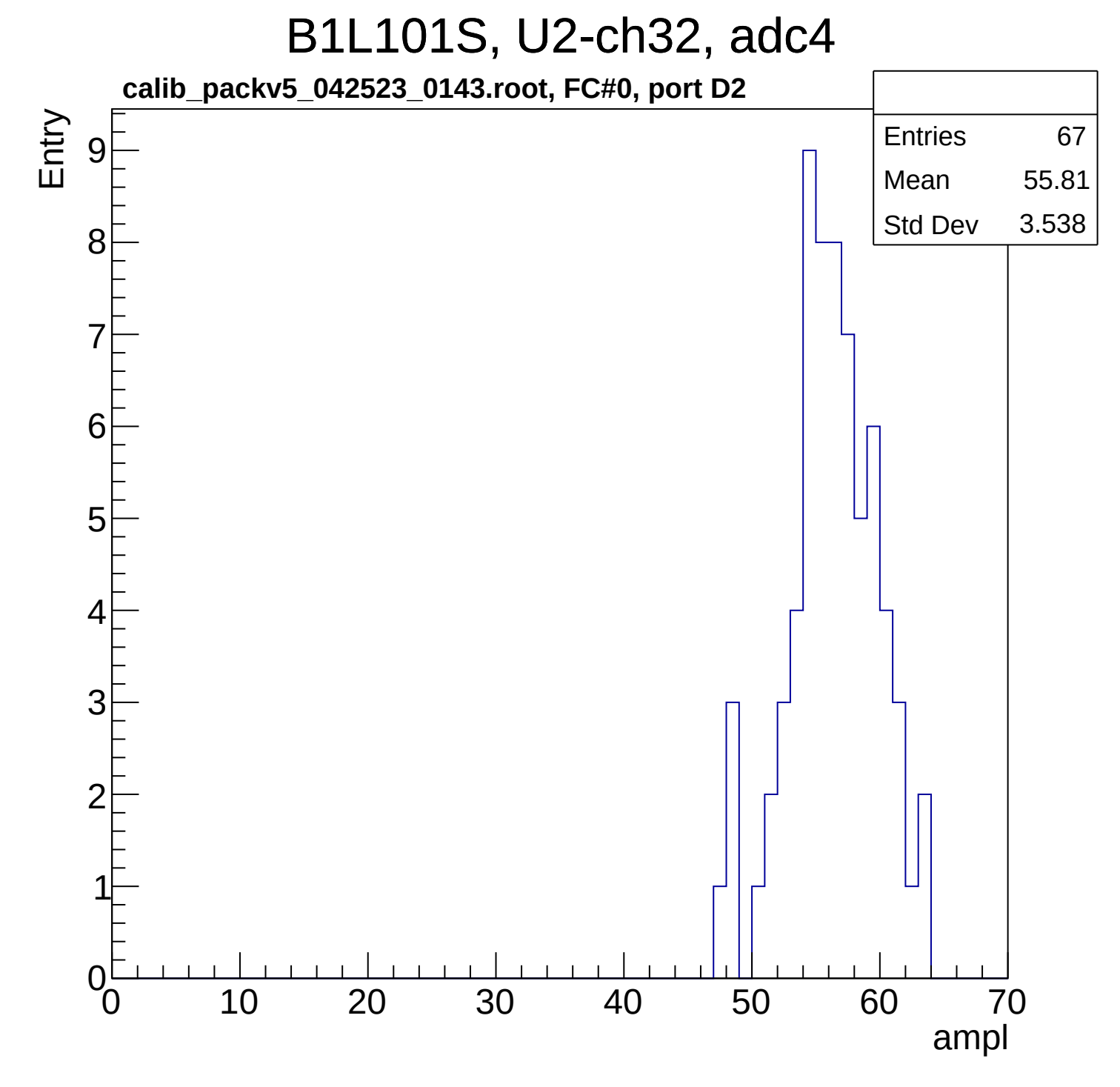

B1L101S, U2-ch31, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 30.5
Std Dev 30.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

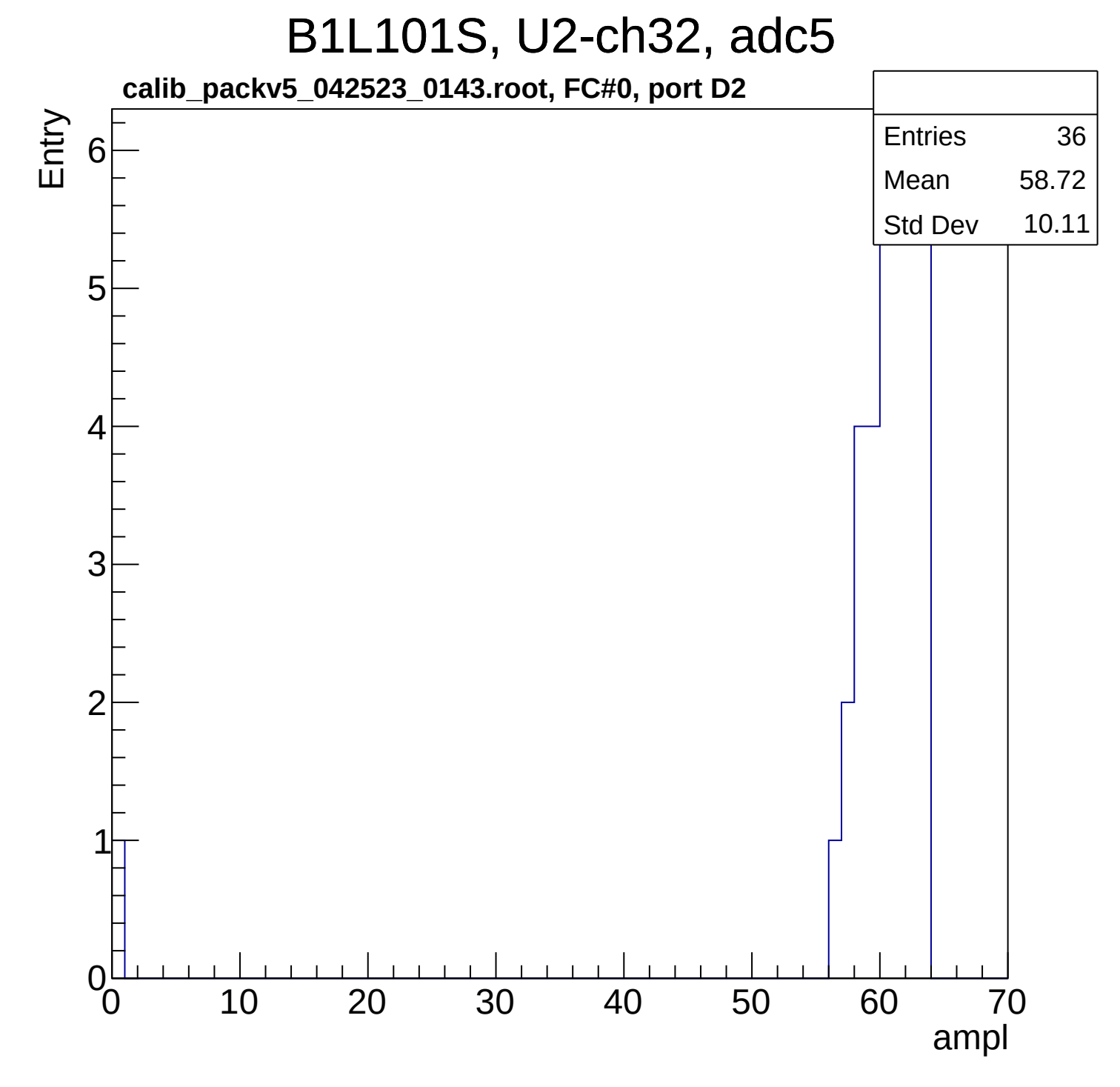

B1L101S, U2-ch32, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 30.28
Std Dev 3.564
Gaus mean : 30.4244
Gaus Width: 3.6476
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

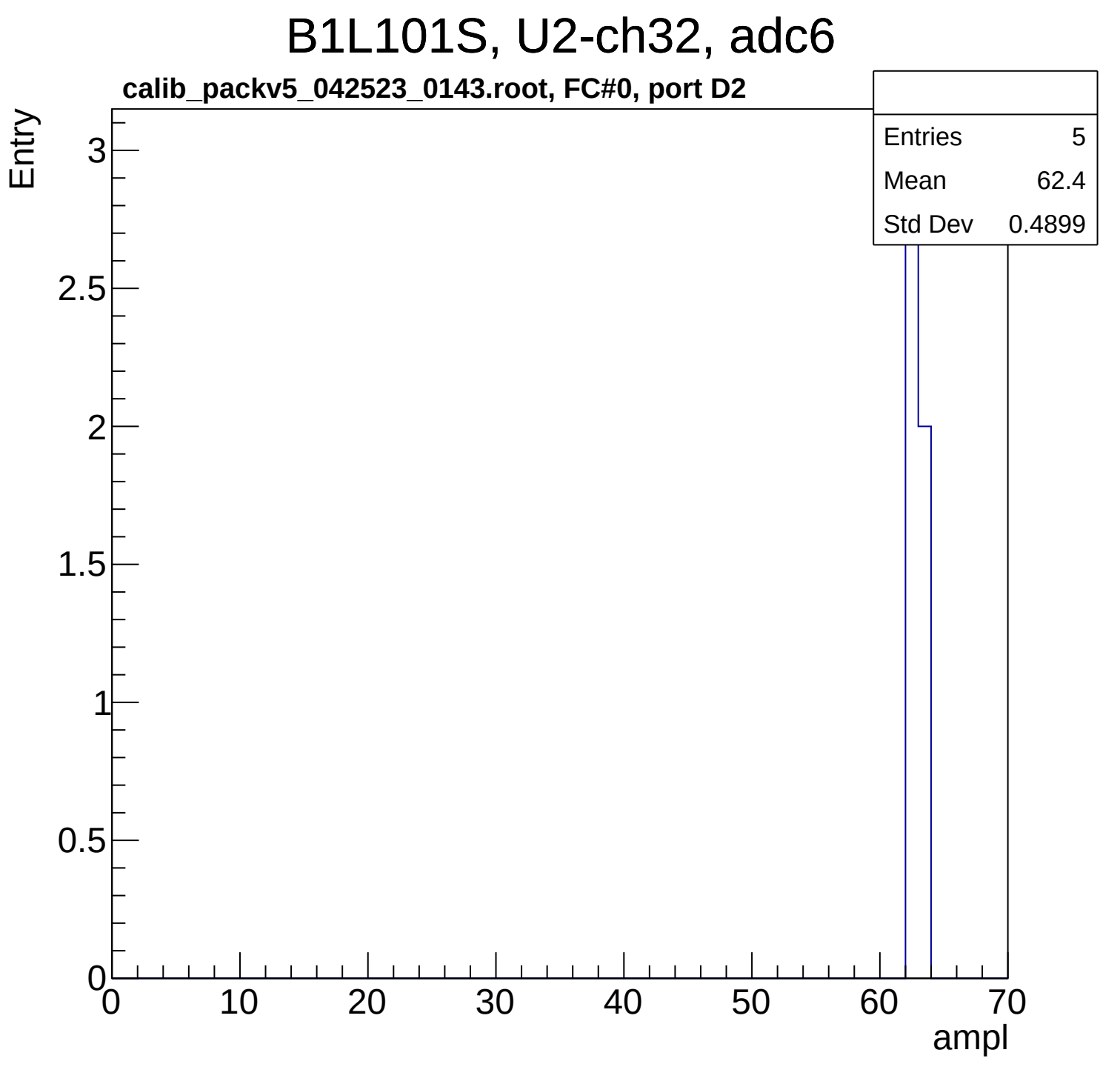

B1L101S, U2-ch32, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 36.74
Std Dev 3.398
Gaus mean : 37.8927
Gaus Width: 3.8891
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

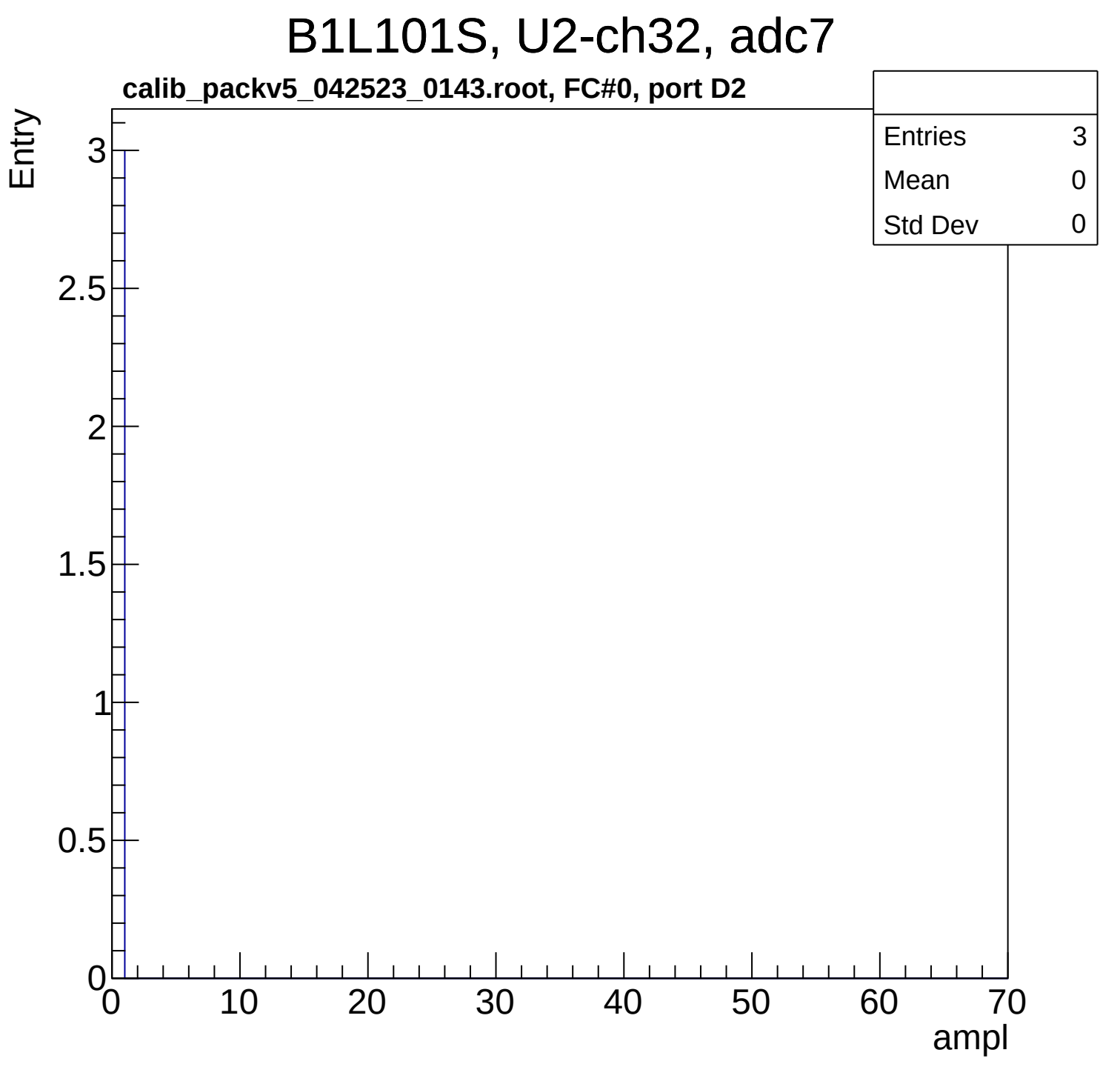

B1L101S, U2-ch32, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 42.94
Std Dev 3.366
Gaus mean : 43.6771
Gaus Width: 3.6209
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

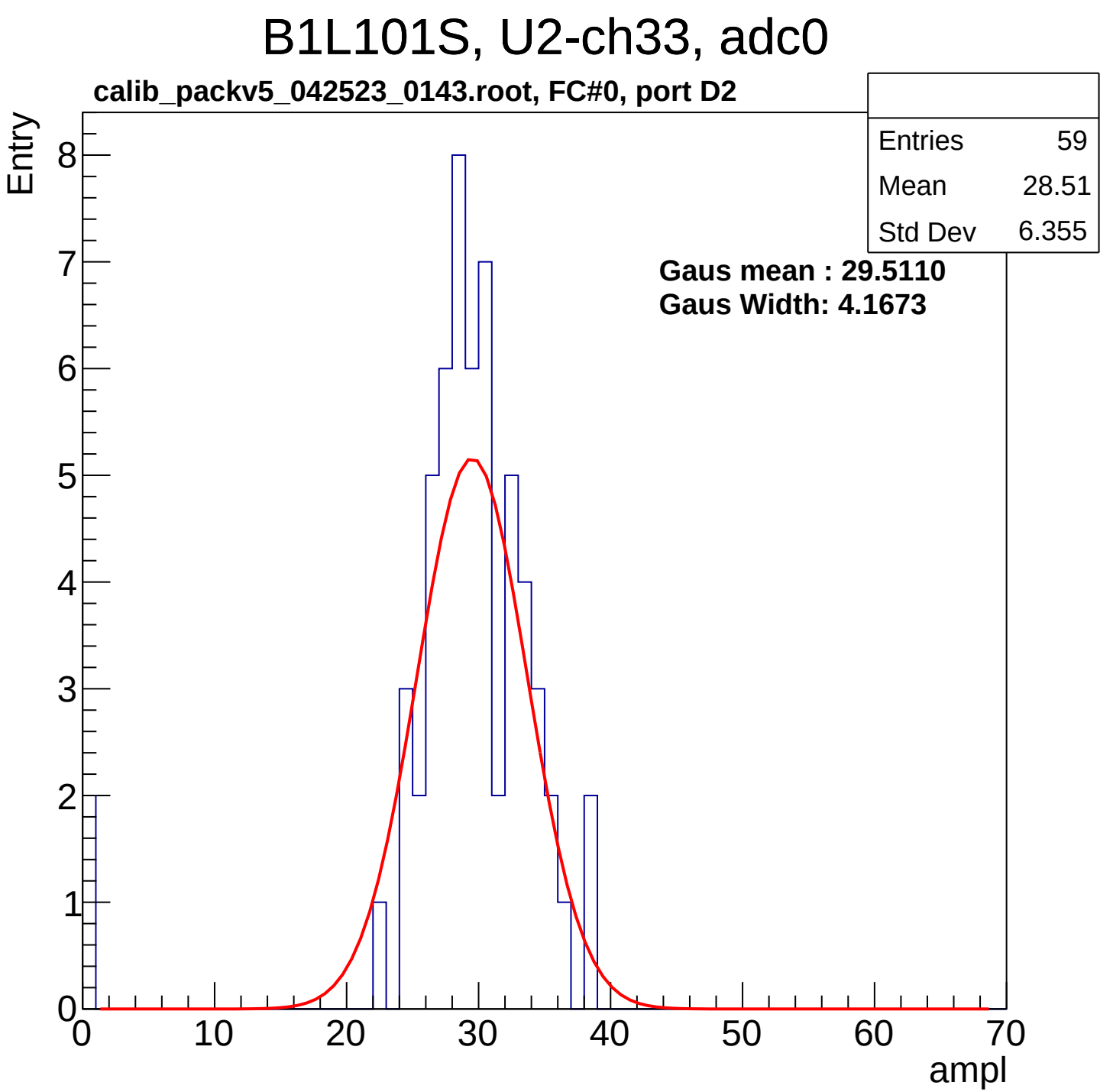

B1L101S, U2-ch32, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 50.6
Std Dev 3.124
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

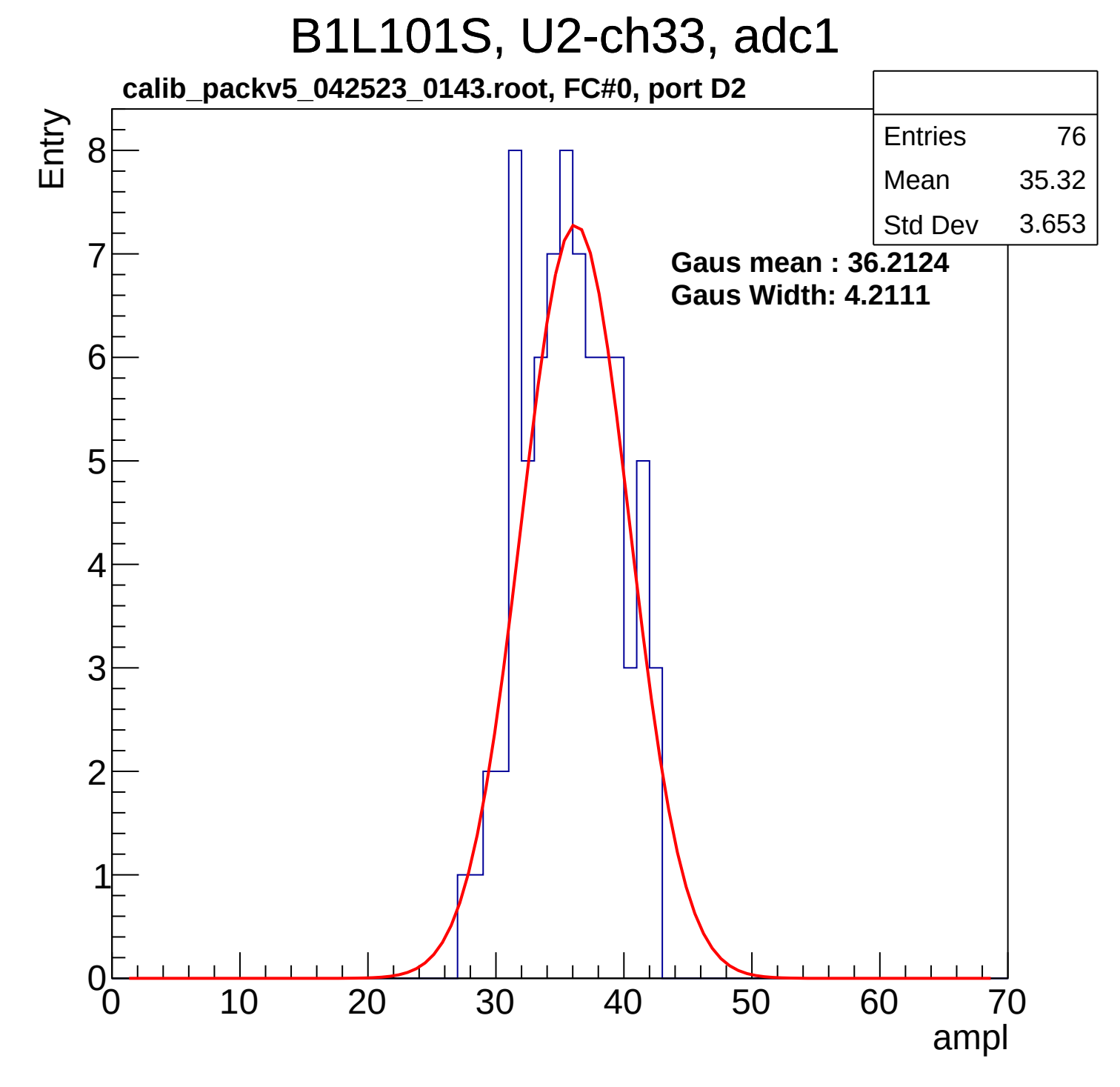

B1L101S, U2-ch32, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 55.81
Std Dev 3.538
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

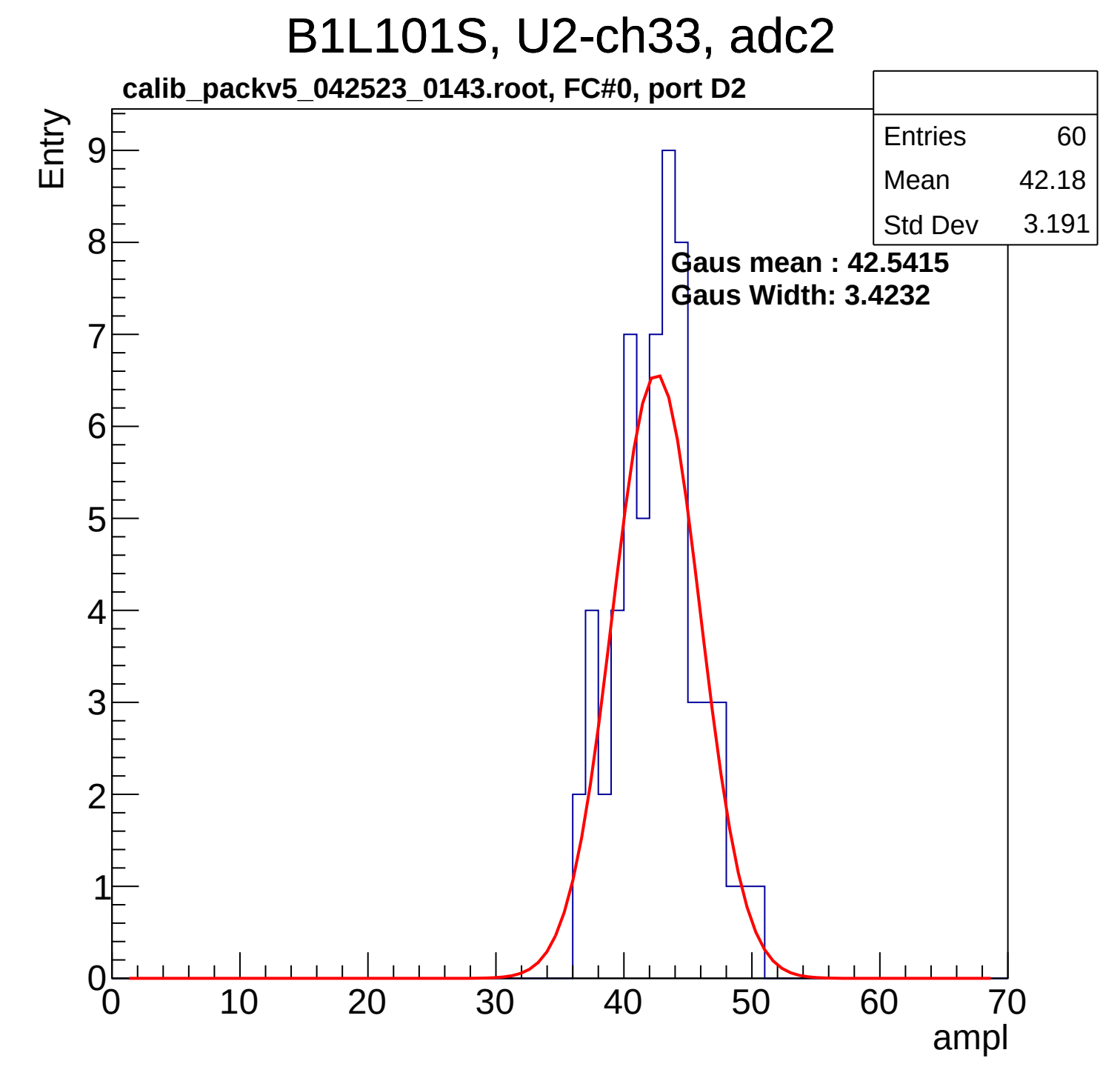

B1L101S, U2-ch32, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 36
Mean 58.72
Std Dev 10.11
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

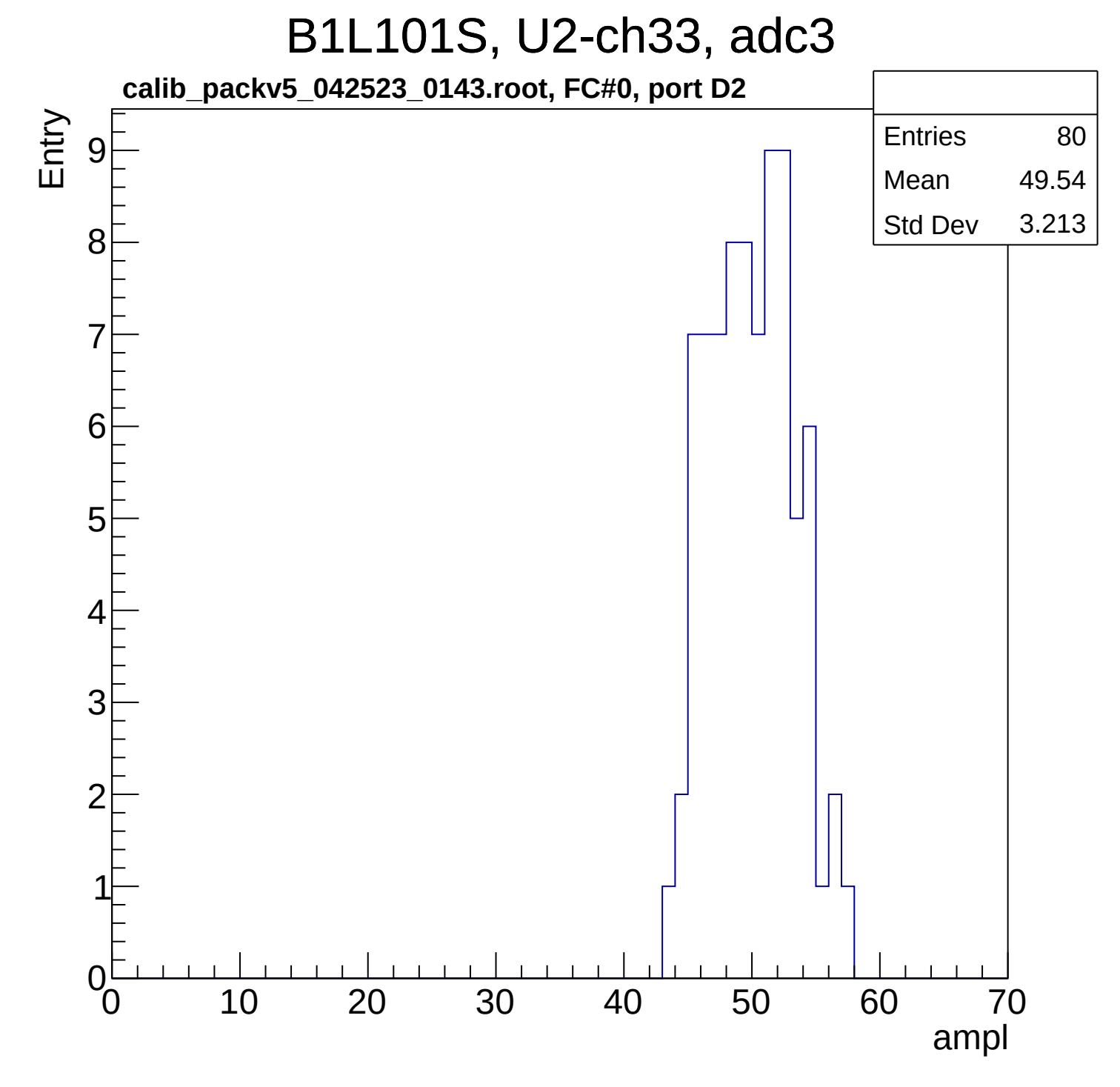

B1L101S, U2-ch32, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 62.4
Std Dev 0.4899
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

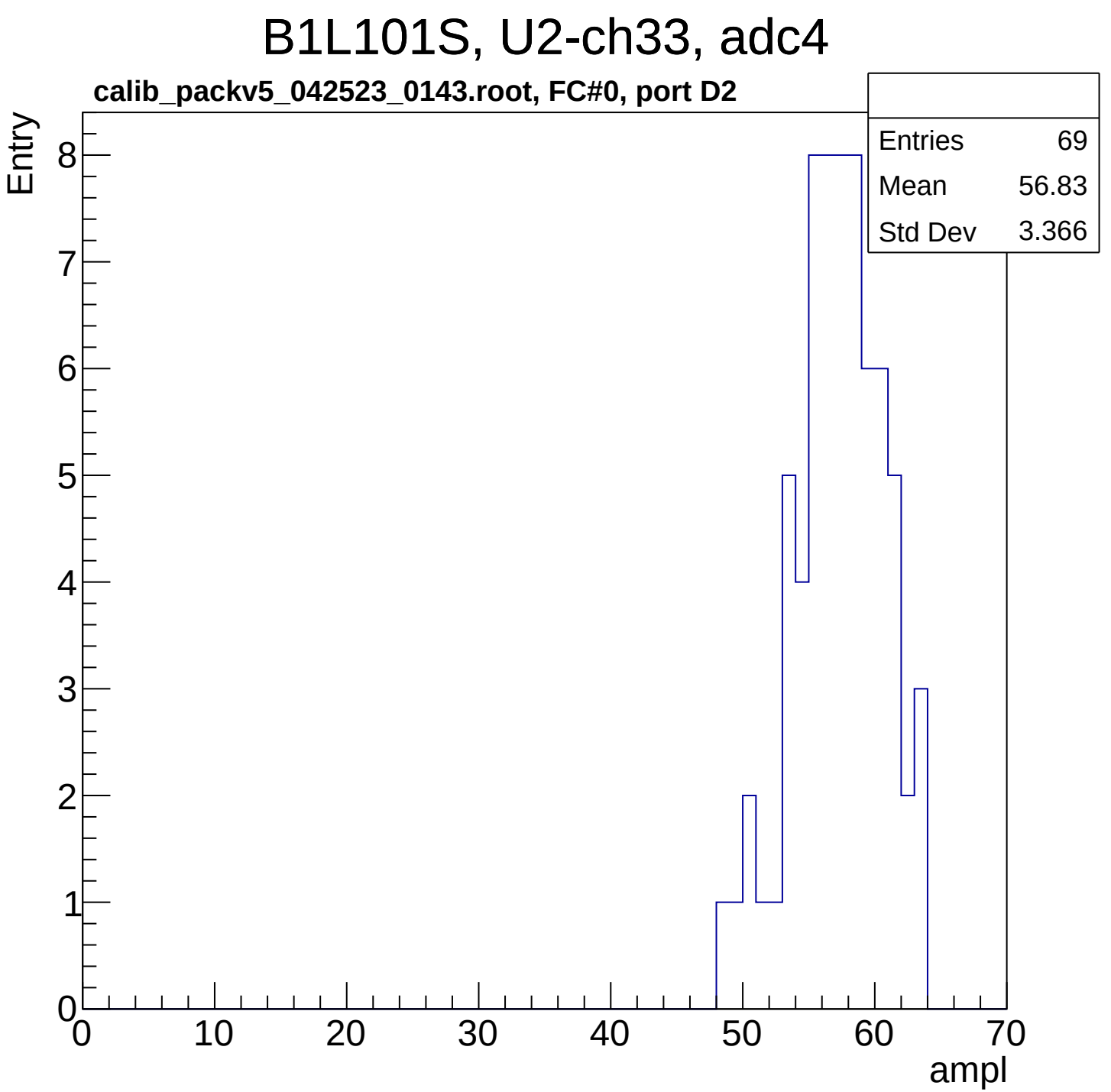

B1L101S, U2-ch32, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 0
Std Dev 0
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl

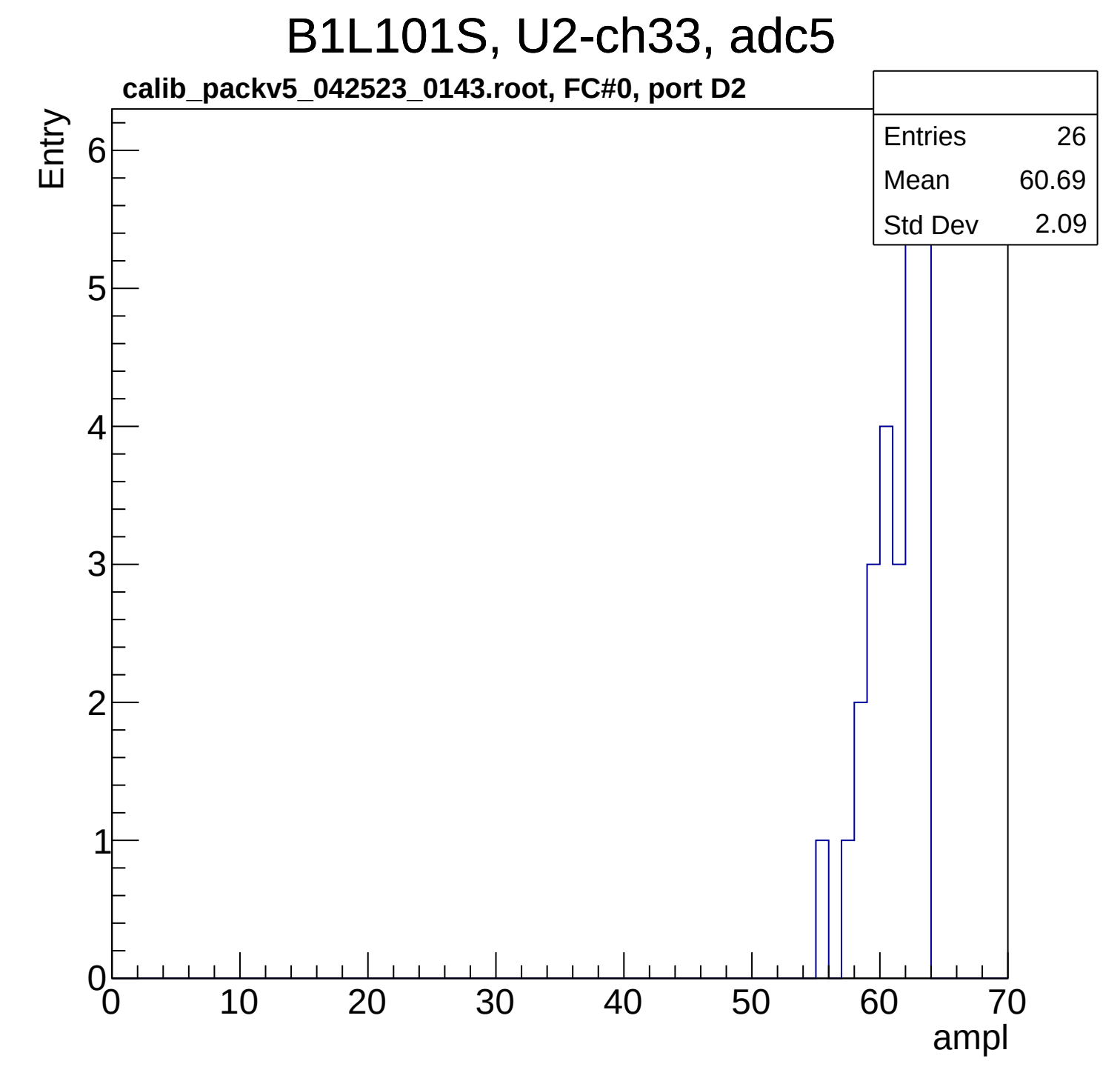

B1L101S, U2-ch33, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 28.51
Std Dev 6.355
Gaus mean : 29.5110
Gaus Width: 4.1673
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

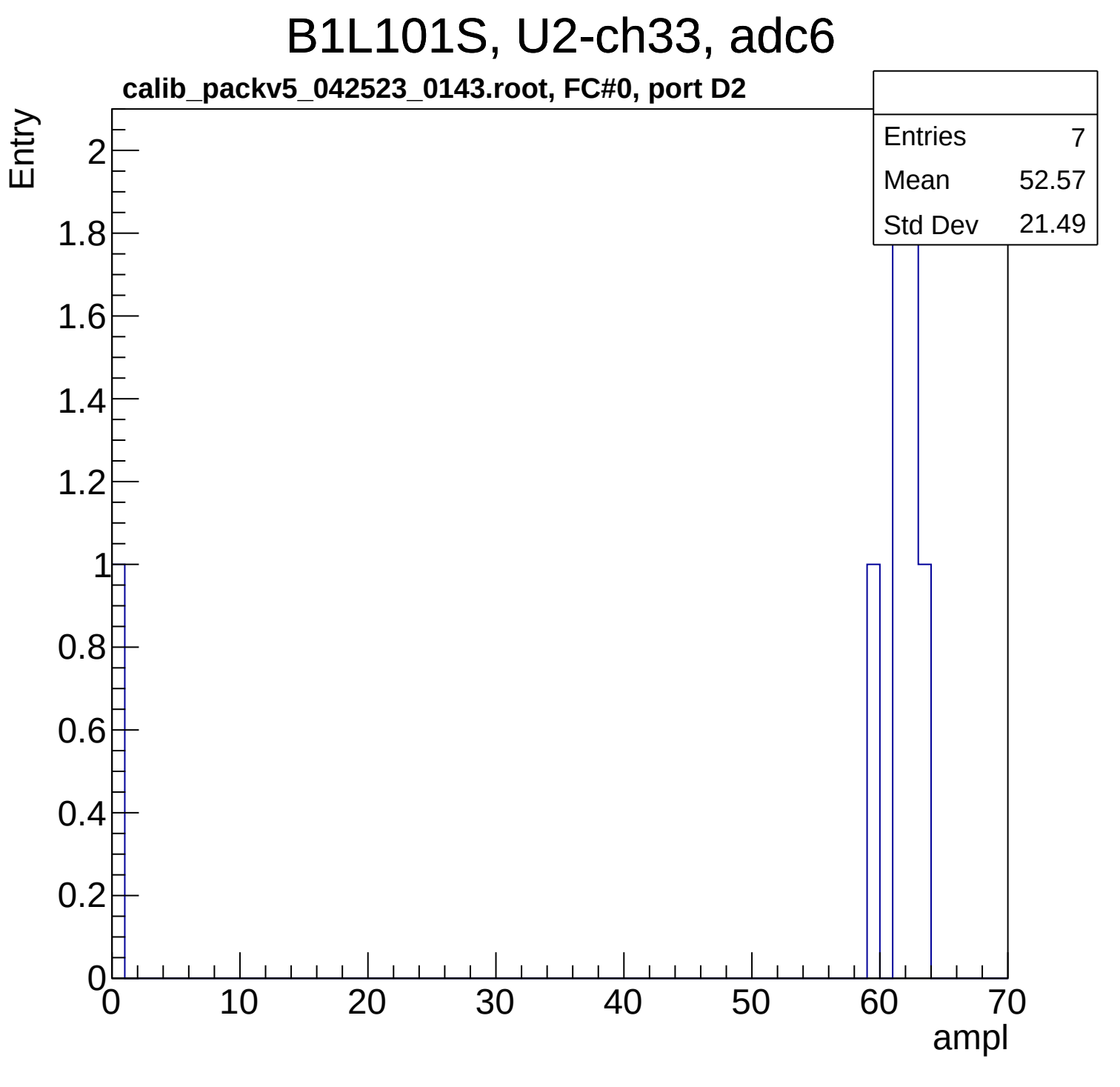

B1L101S, U2-ch33, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 35.32
Std Dev 3.653
Gaus mean : 36.2124
Gaus Width: 4.2111
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

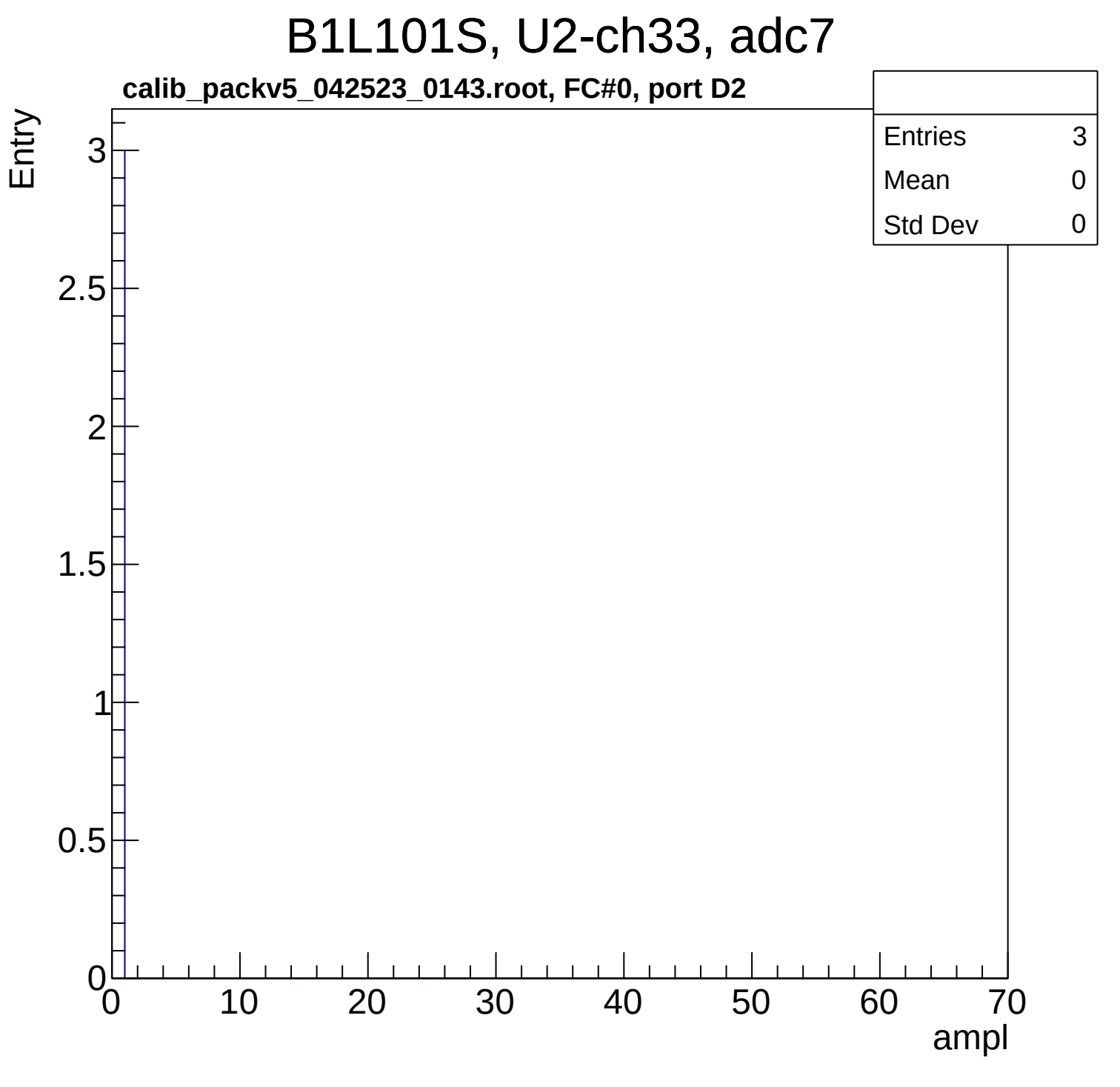

B1L101S, U2-ch33, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 42.18
Std Dev 3.191
Gaus mean : 42.5415
Gaus Width: 3.4232
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

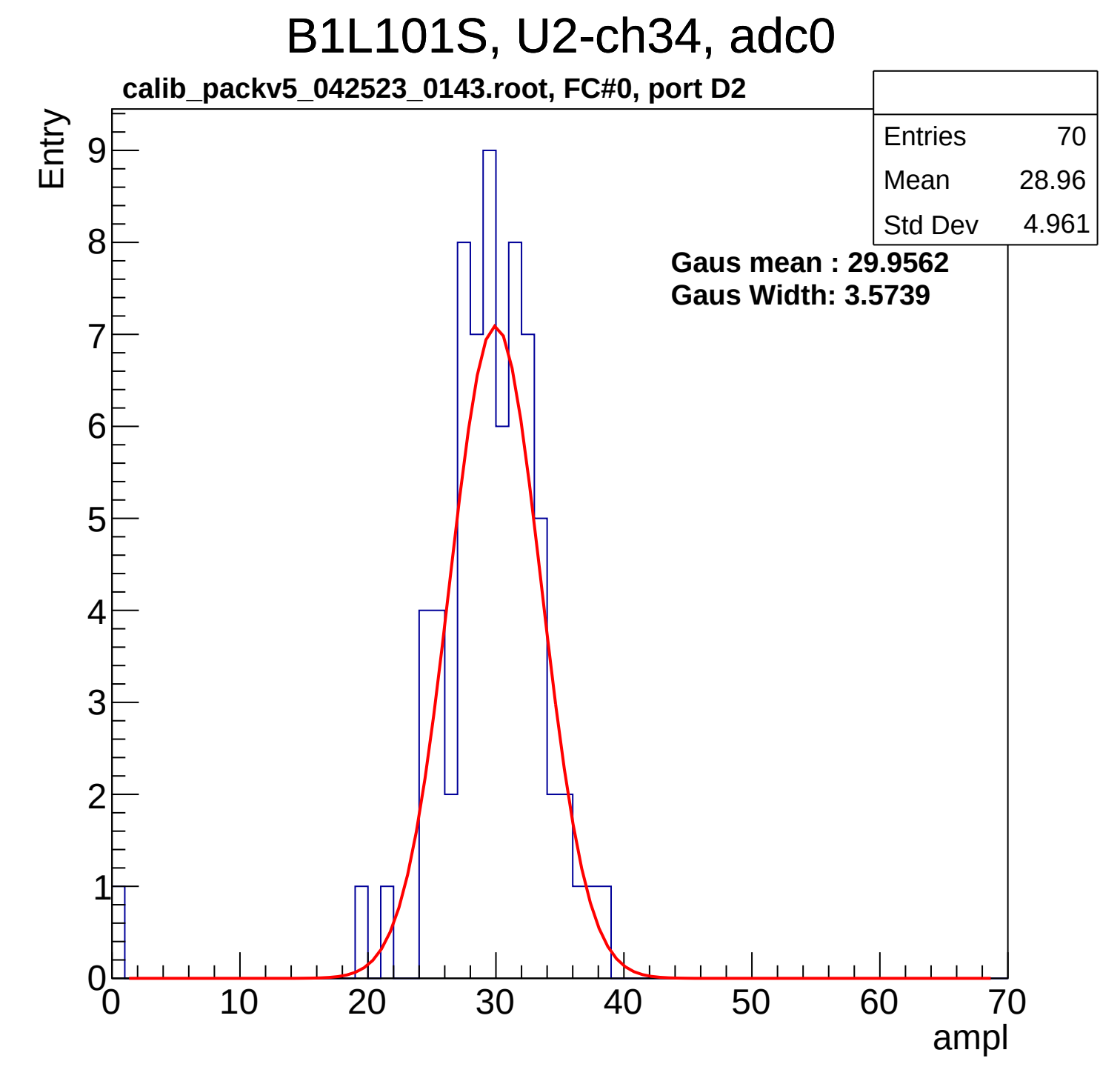

B1L101S, U2-ch33, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 80
Mean 49.54
Std Dev 3.213
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

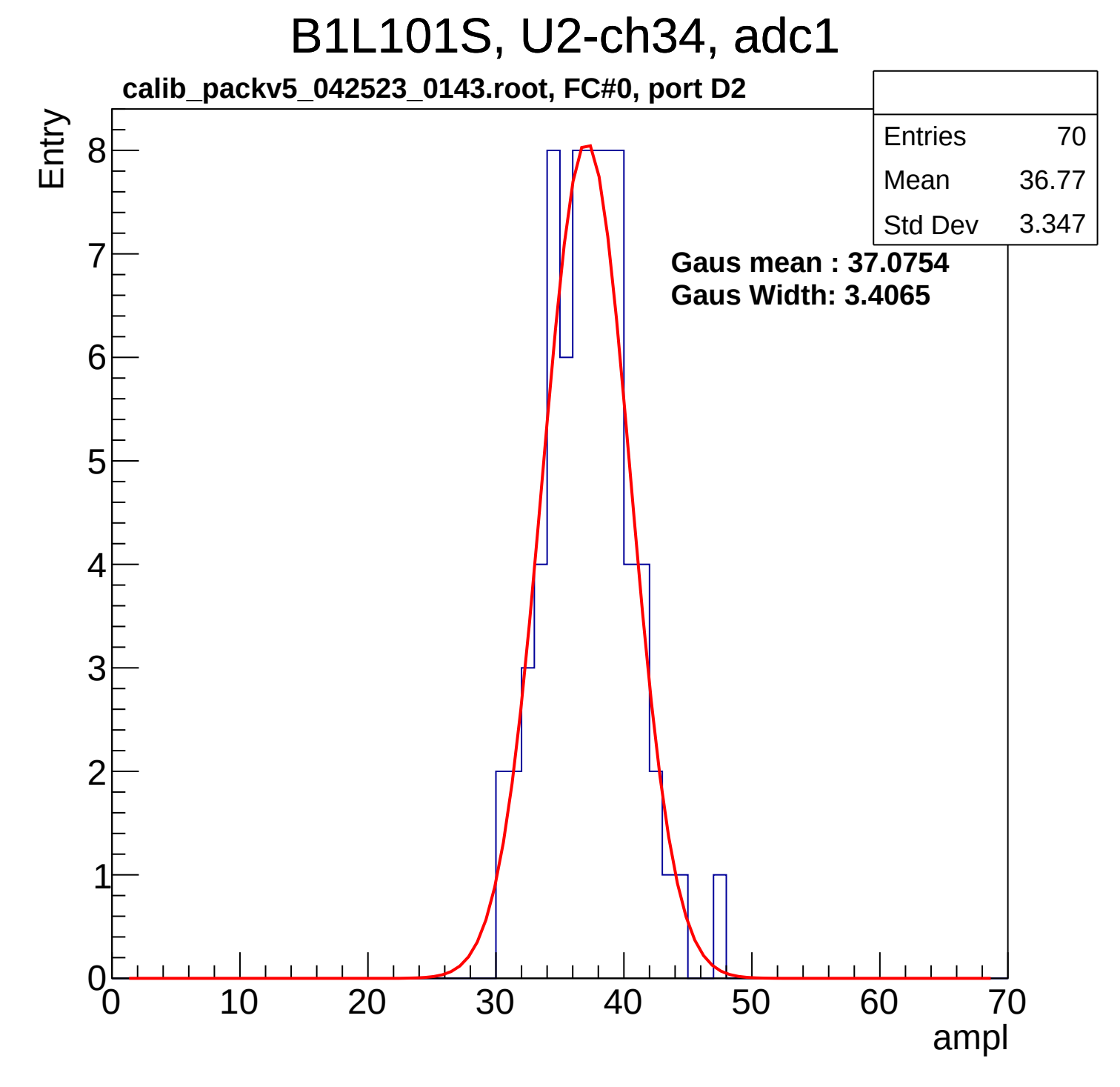

B1L101S, U2-ch33, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 56.83
Std Dev 3.366
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

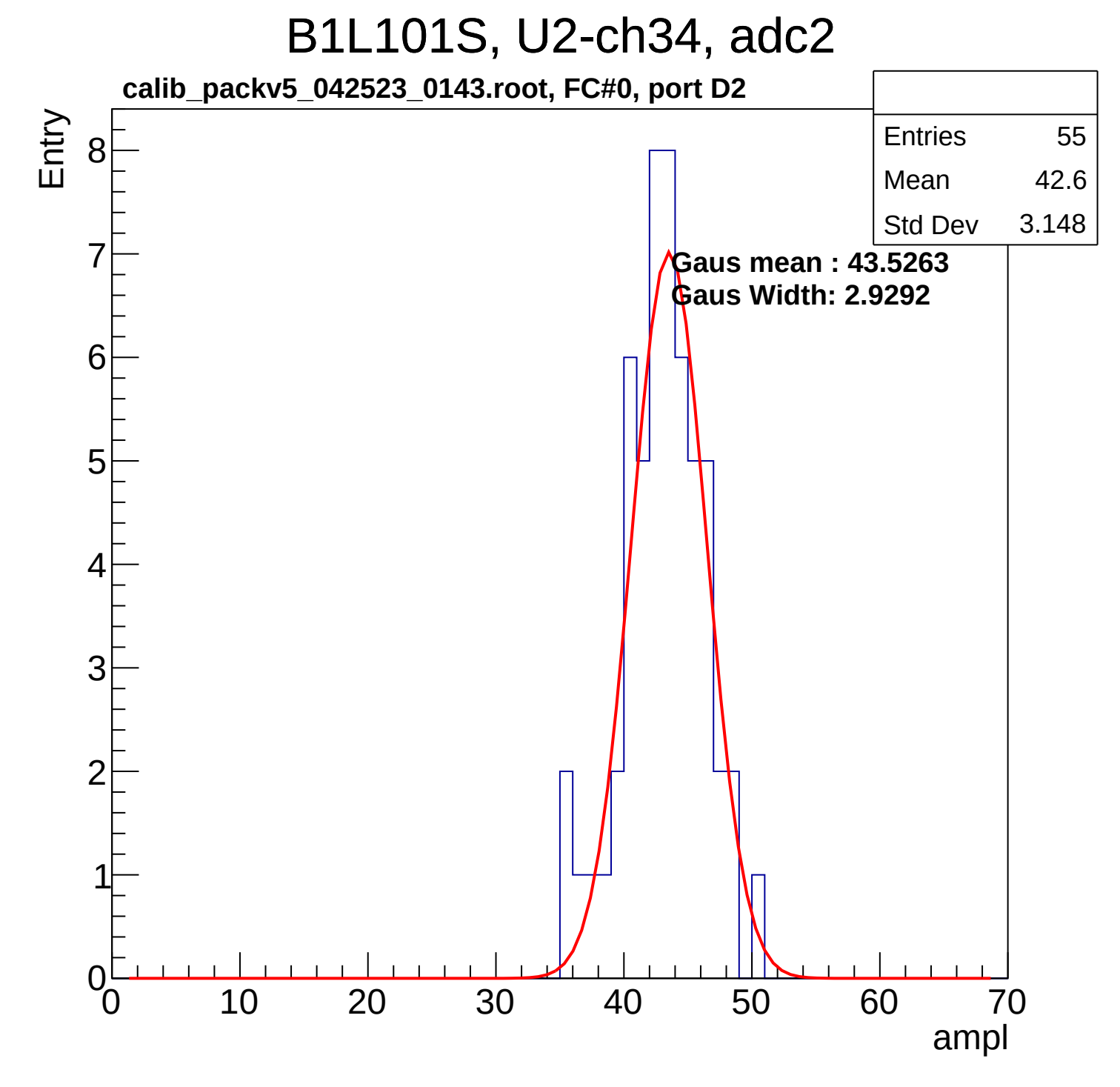

B1L101S, U2-ch33, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 26
Mean 60.69
Std Dev 2.09
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

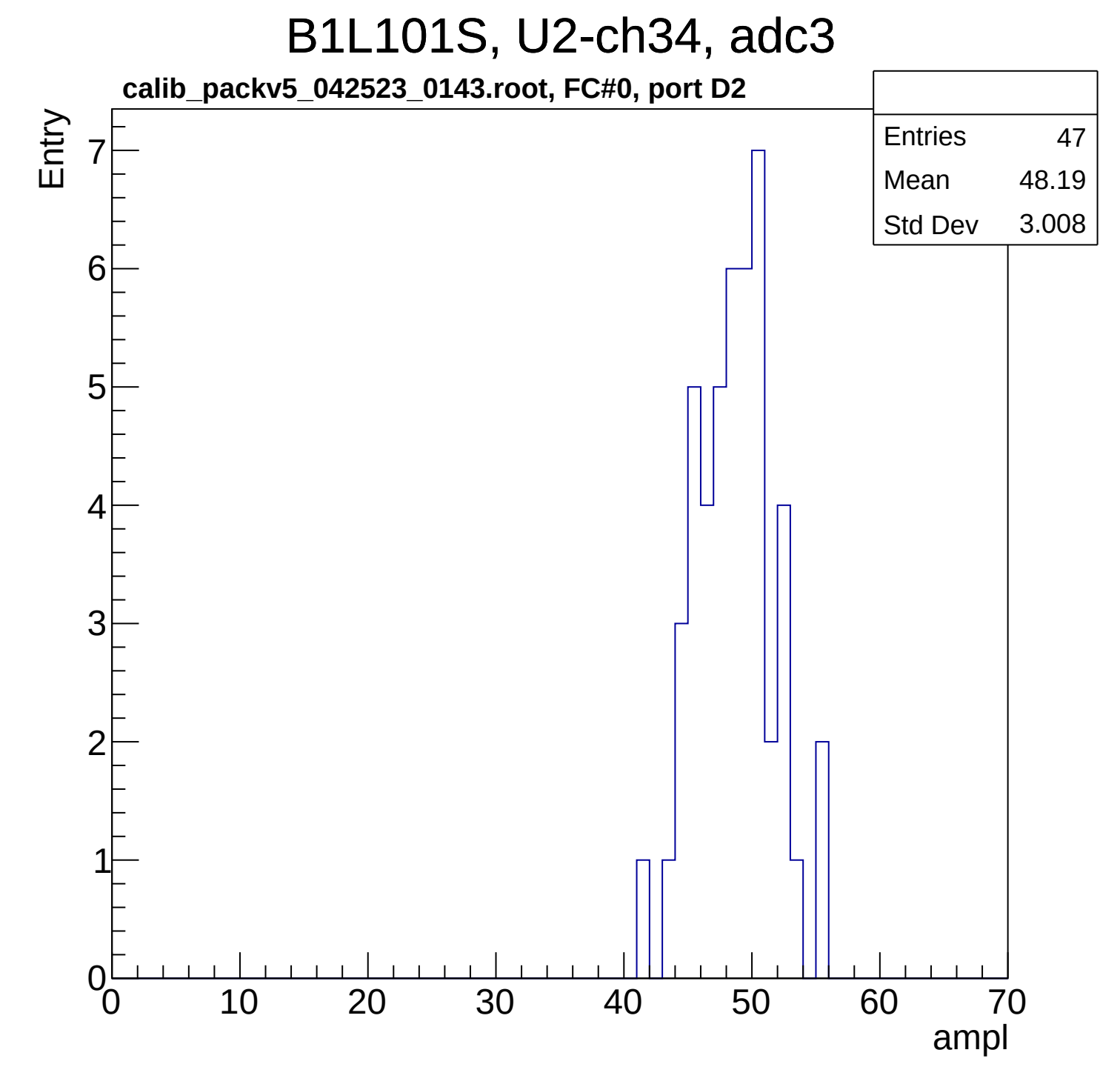

B1L101S, U2-ch33, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 52.57
Std Dev 21.49
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

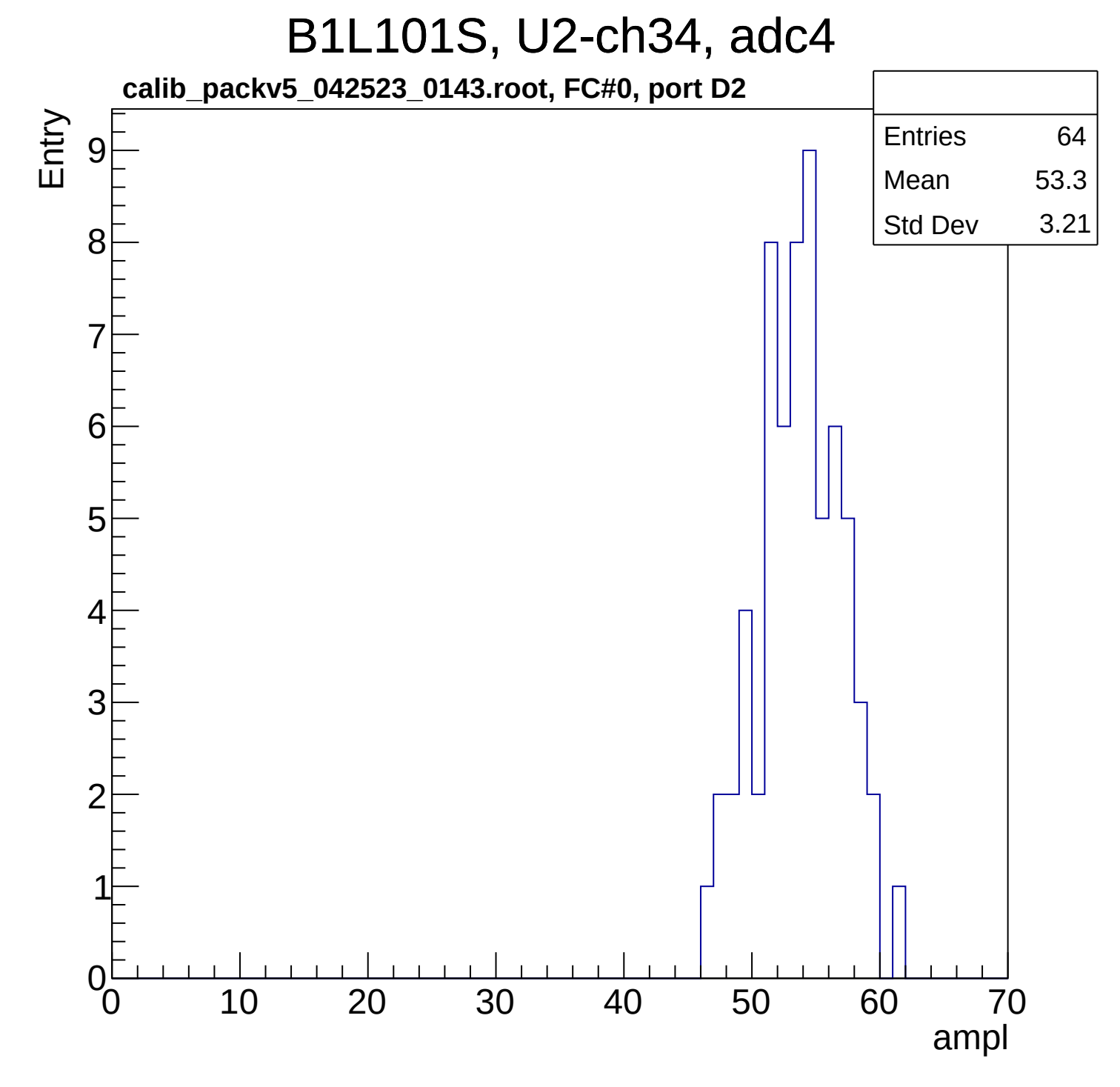

B1L101S, U2-ch33, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 0
Std Dev 0
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl

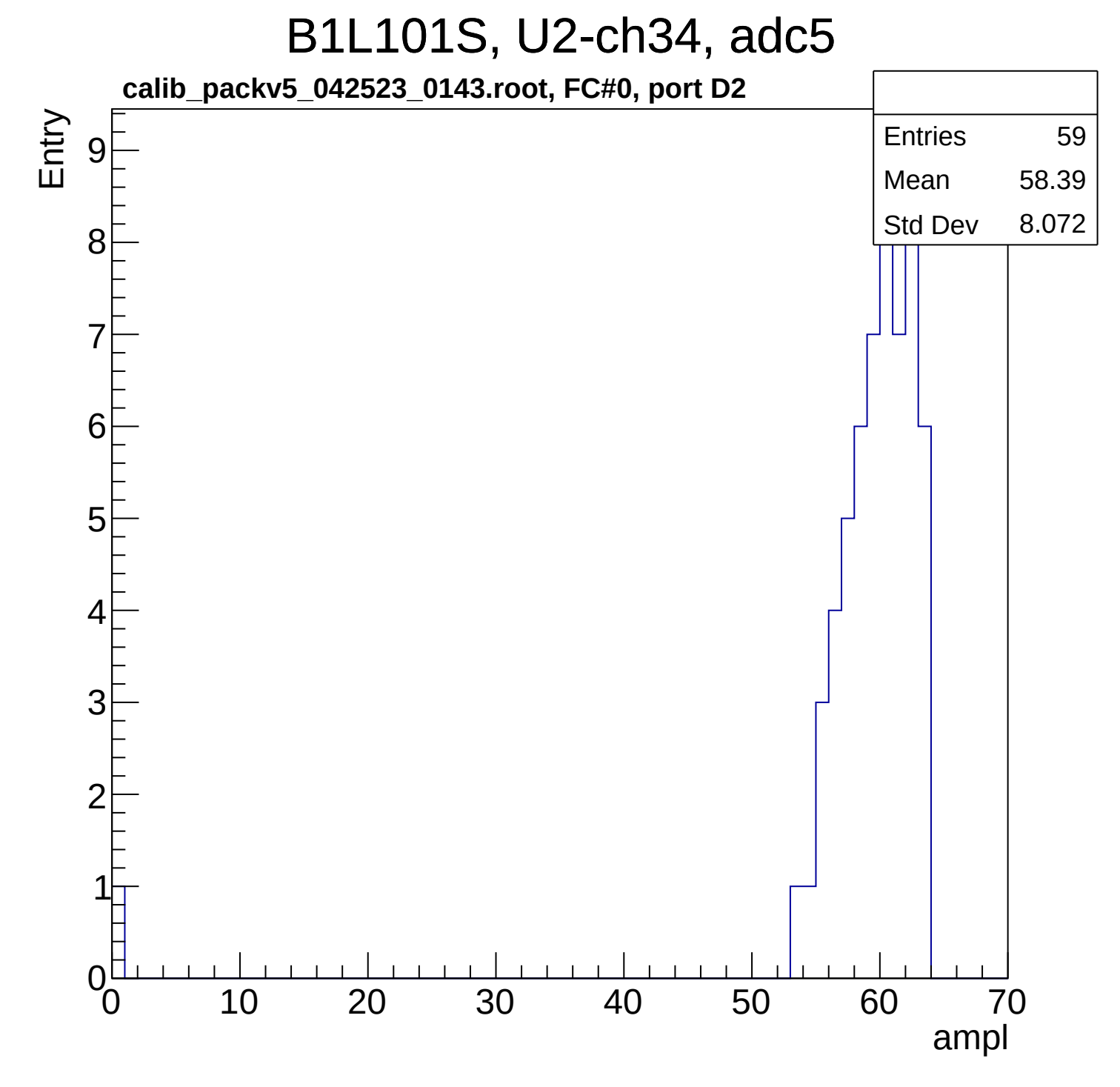

B1L101S, U2-ch34, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 28.96
Std Dev 4.961
Gaus mean : 29.9562
Gaus Width: 3.5739
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

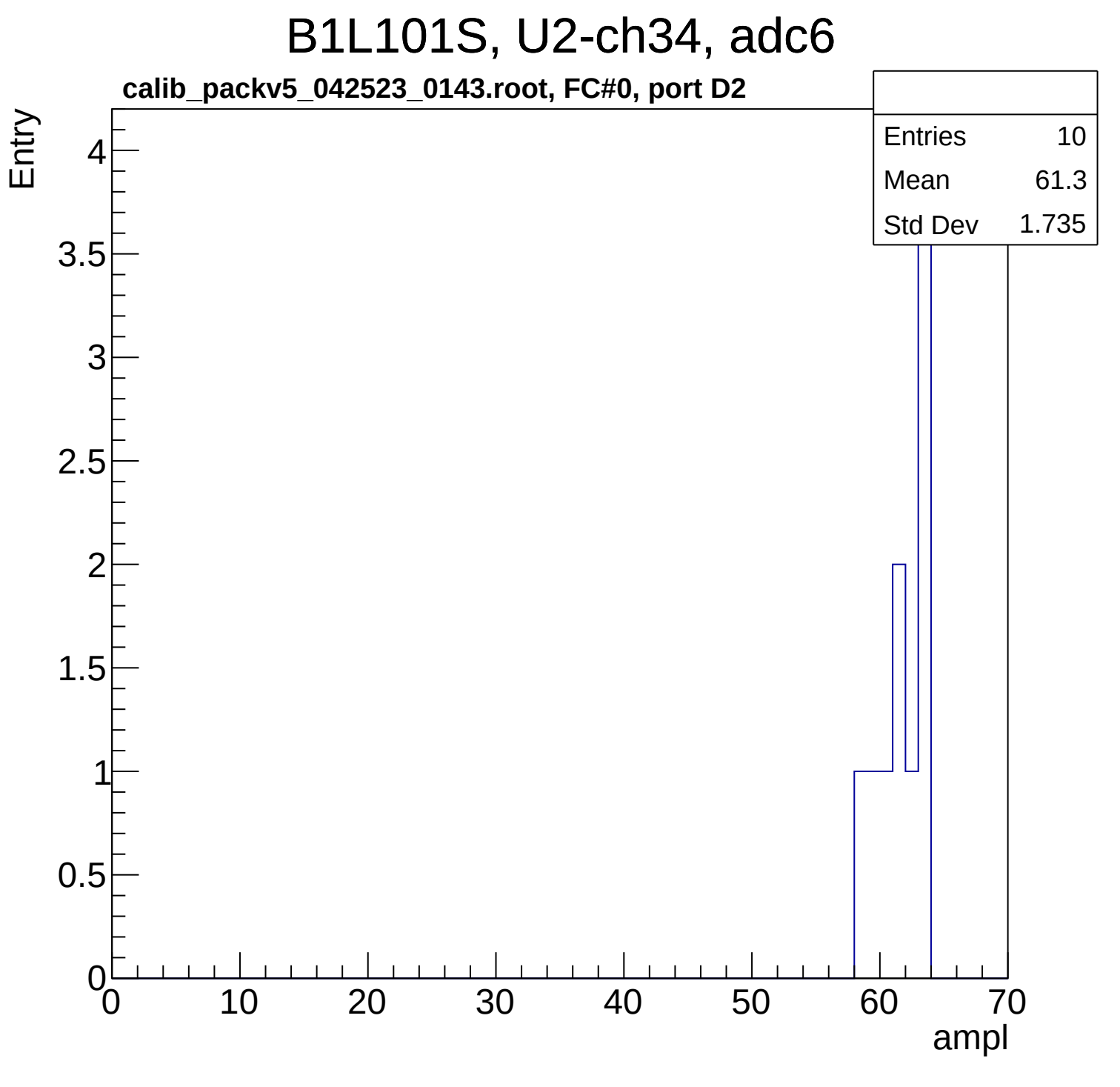

B1L101S, U2-ch34, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 36.77
Std Dev 3.347
Gaus mean : 37.0754
Gaus Width: 3.4065
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

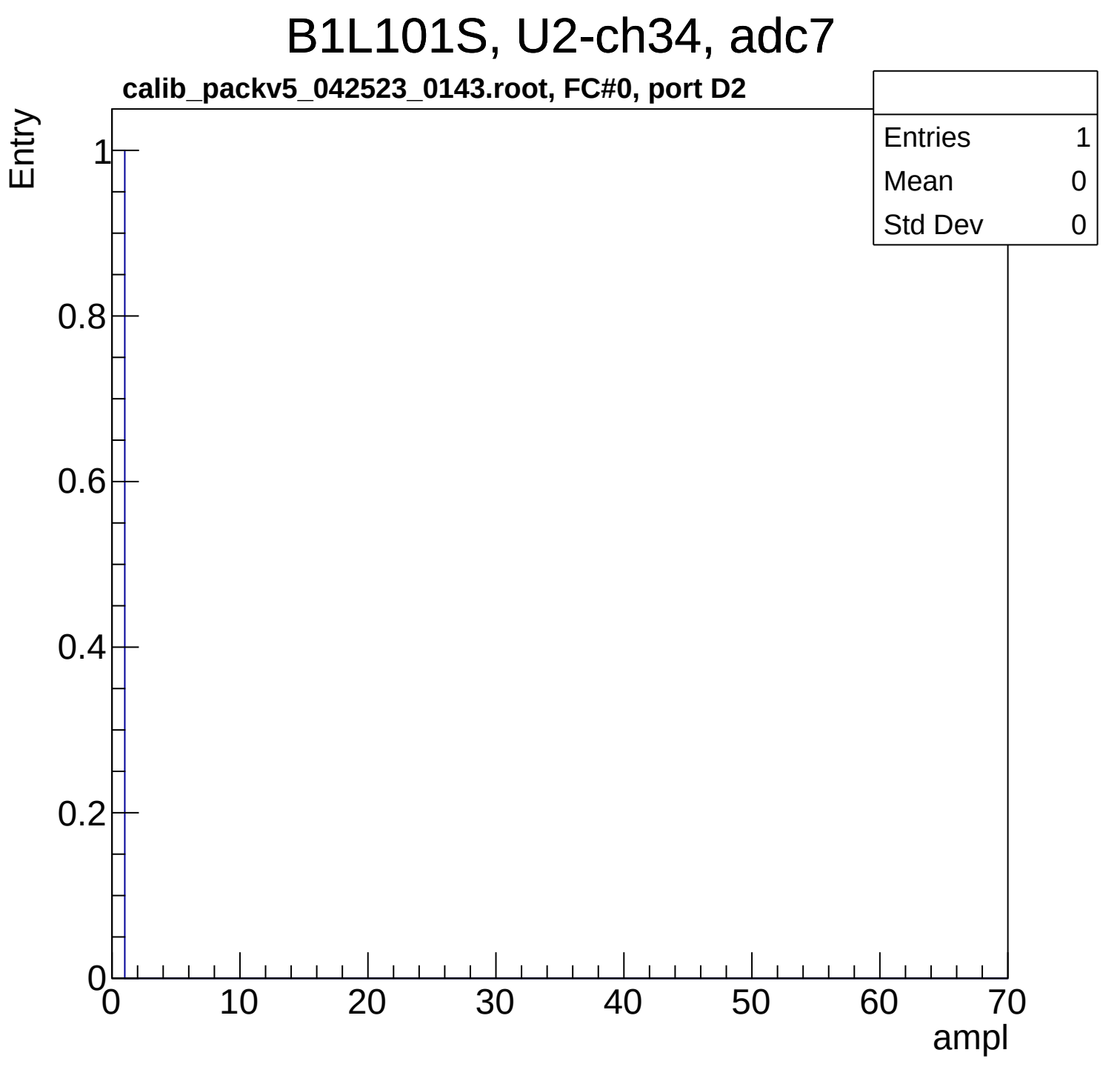

B1L101S, U2-ch34, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 42.6
Std Dev 3.148
Gaus mean : 43.5263
Gaus Width: 2.9292
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

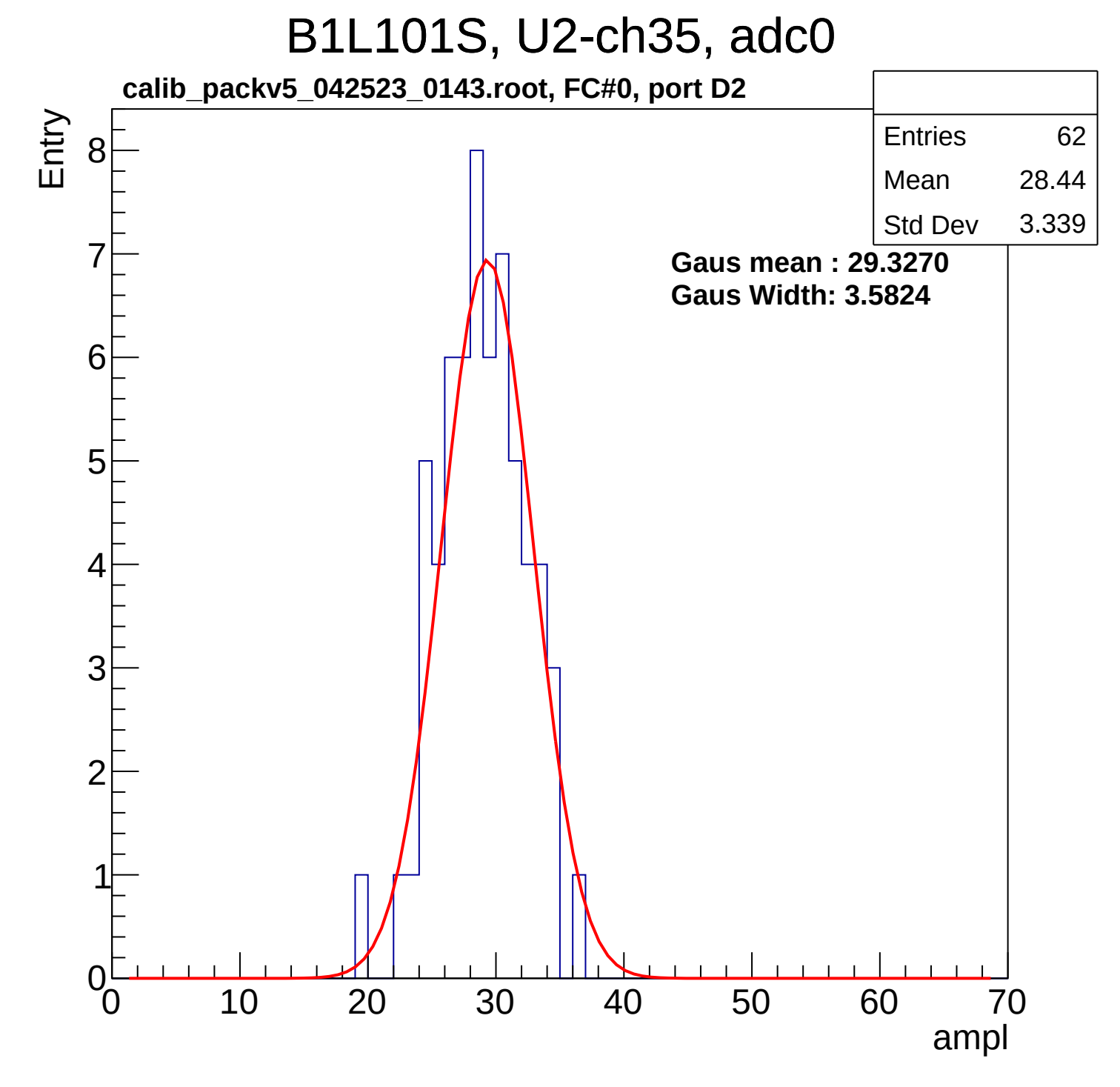

B1L101S, U2-ch34, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 48.19
Std Dev 3.008
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

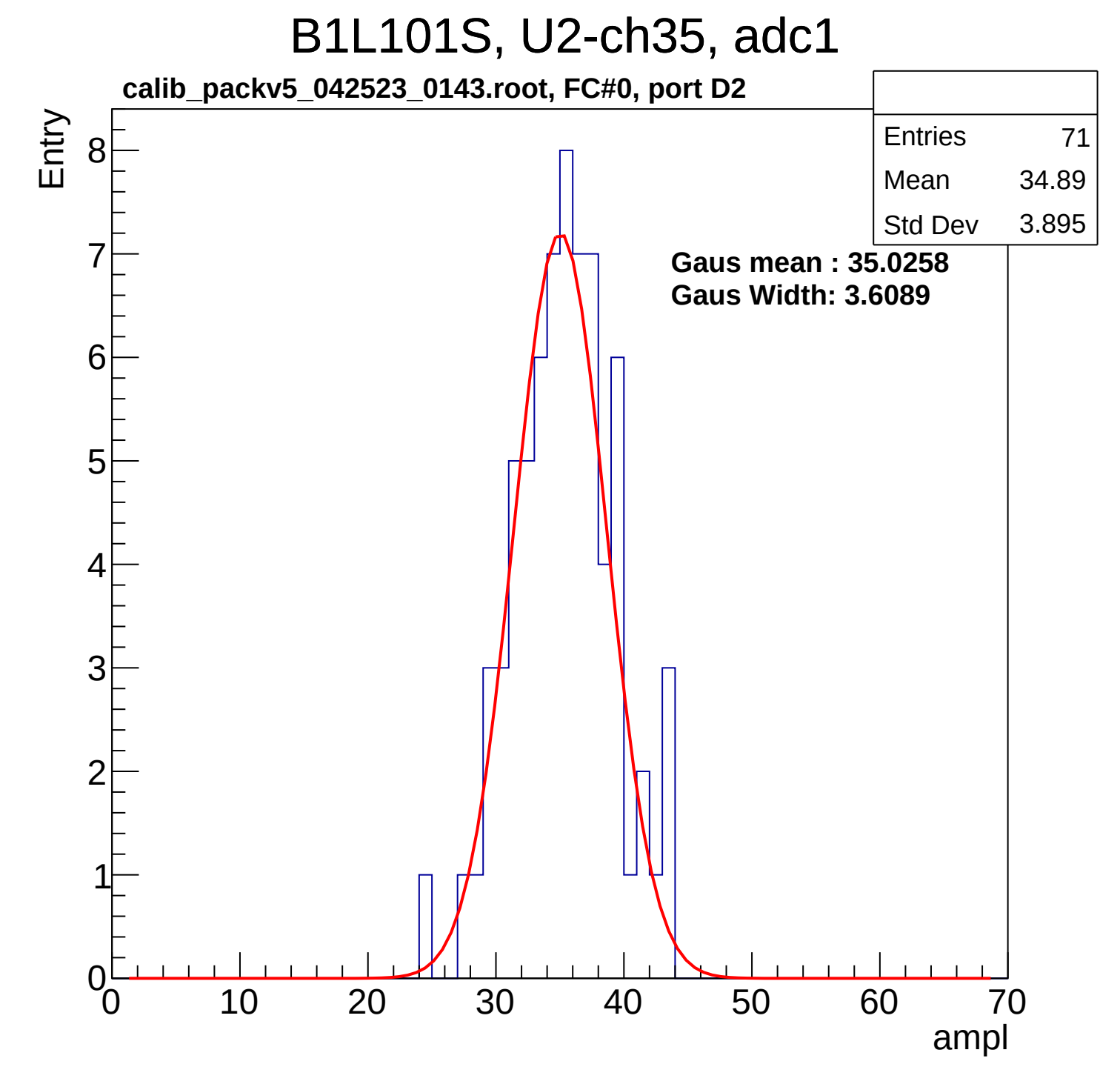

B1L101S, U2-ch34, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 53.3
Std Dev 3.21
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

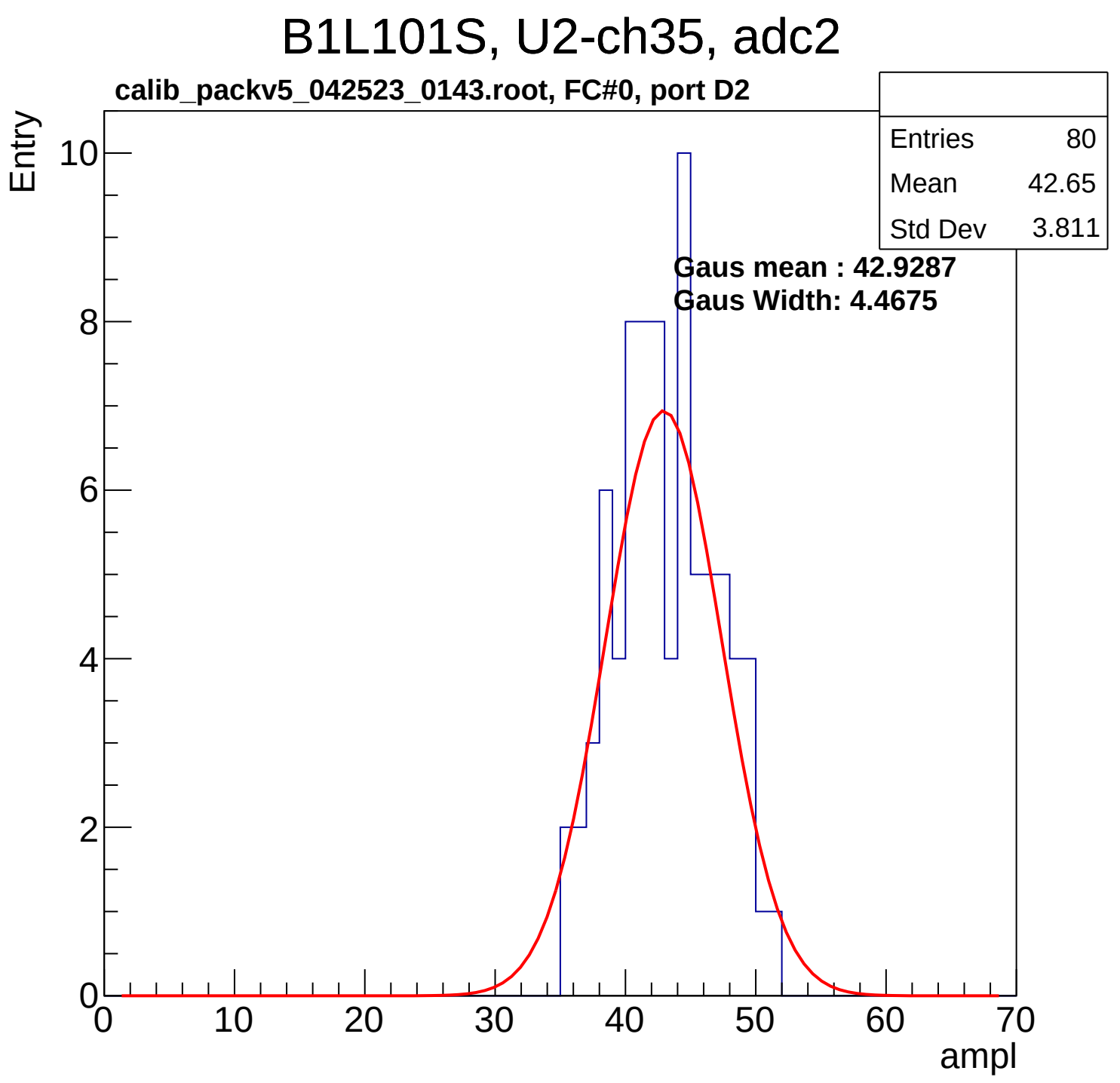

B1L101S, U2-ch34, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 58.39
Std Dev 8.072
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

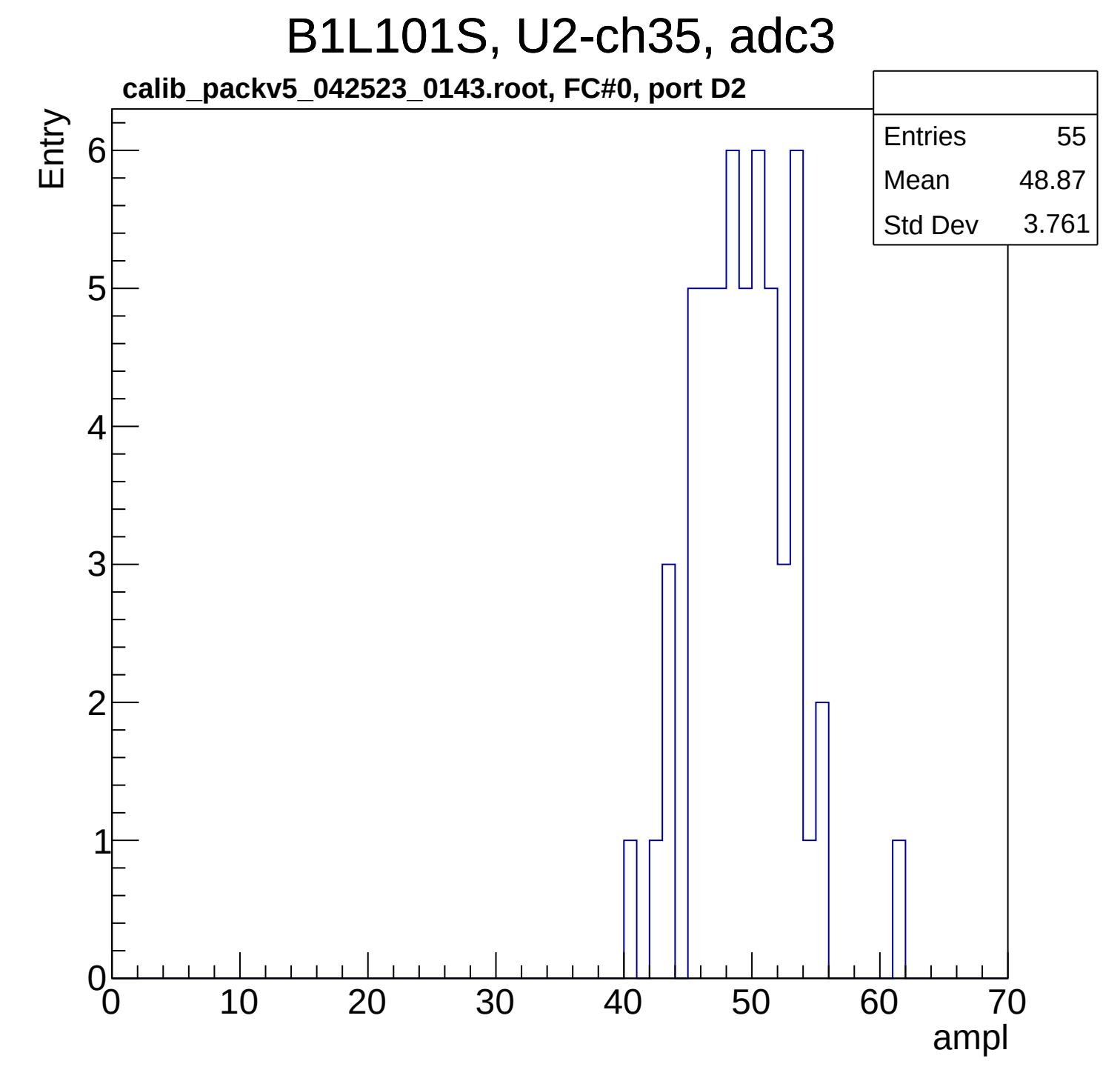

B1L101S, U2-ch34, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 61.3
Std Dev 1.735
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

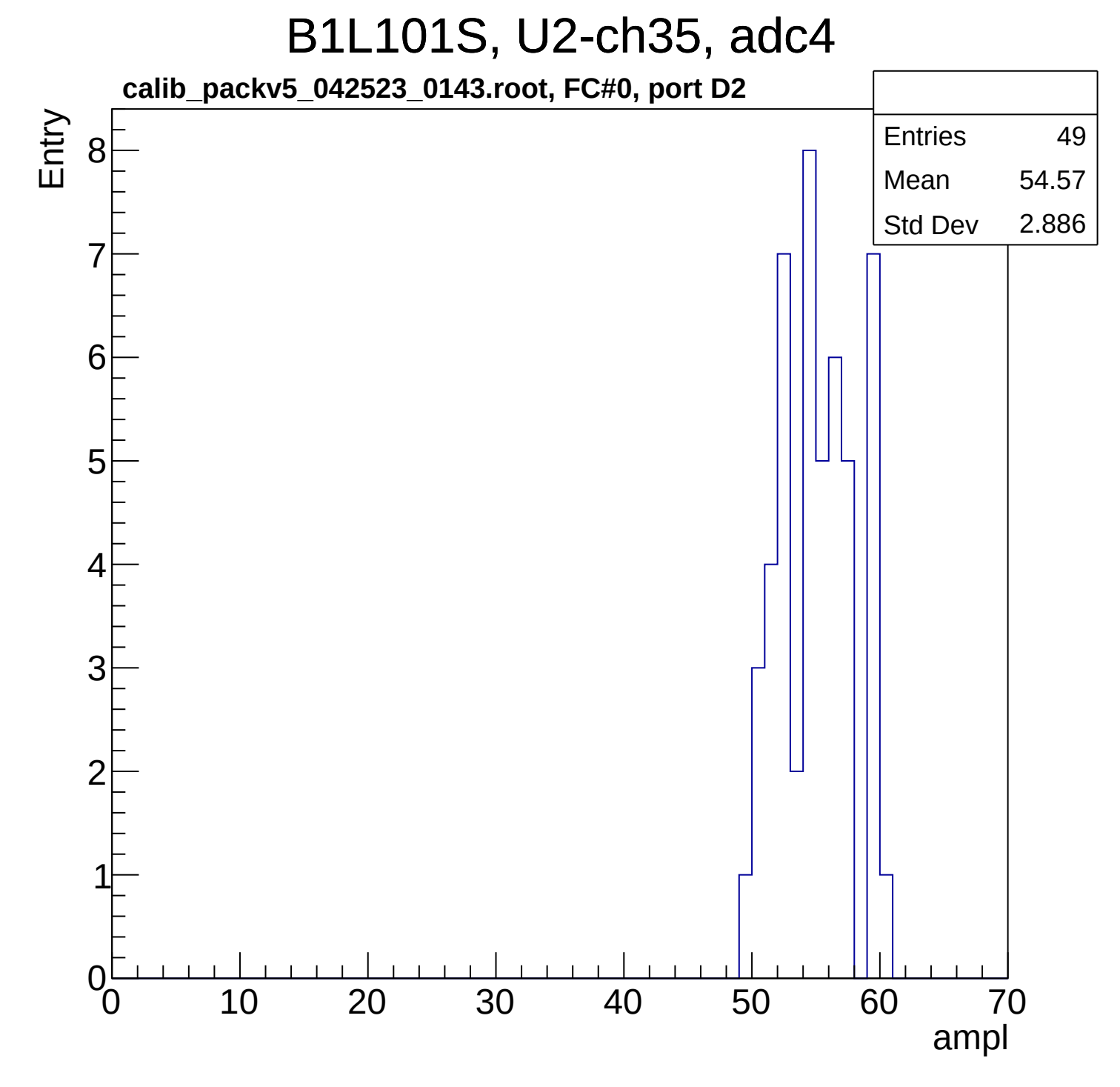

B1L101S, U2-ch34, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

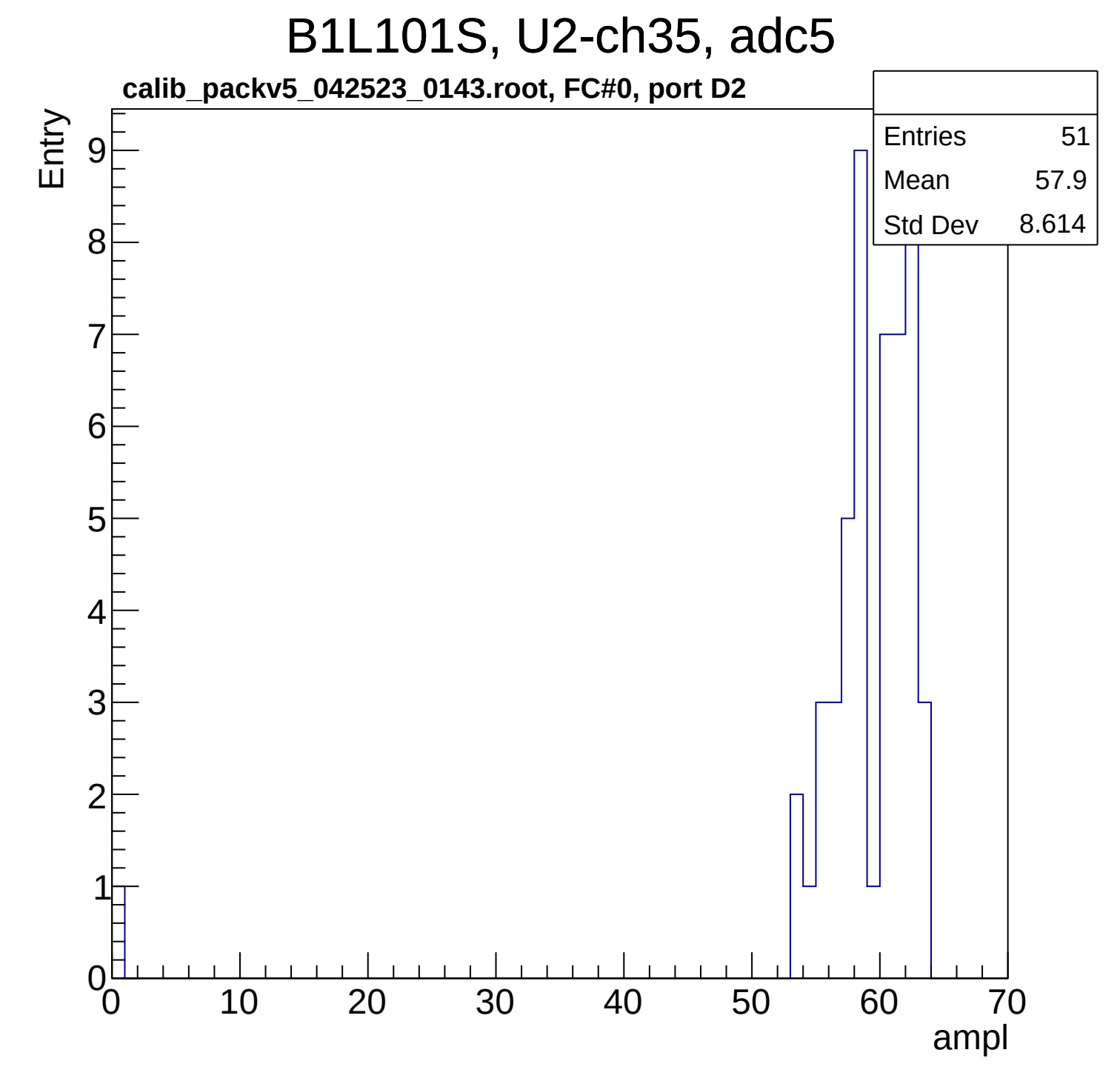

B1L101S, U2-ch35, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 28.44
Std Dev 3.339
Gaus mean : 29.3270
Gaus Width: 3.5824
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

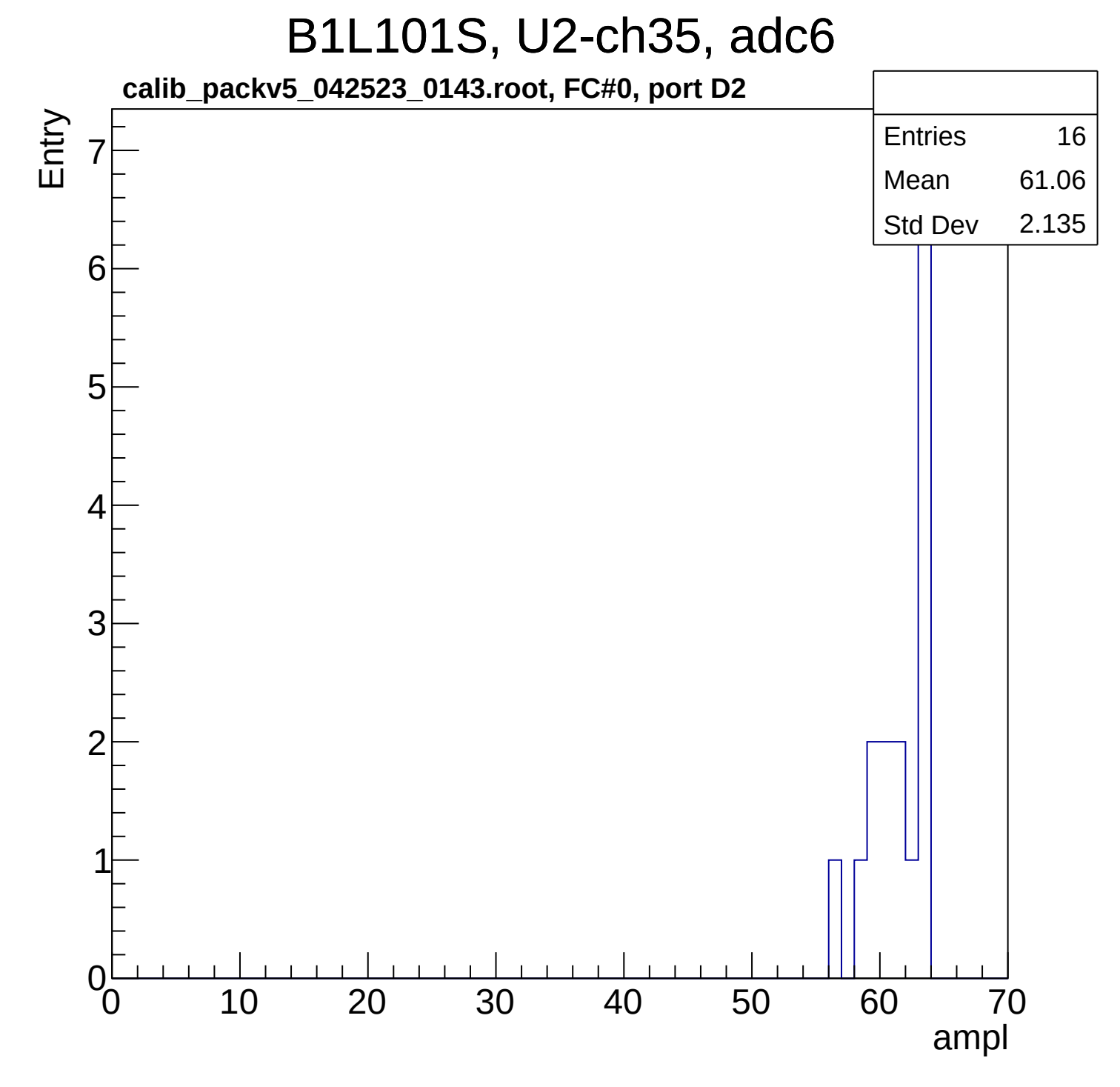

B1L101S, U2-ch35, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 34.89
Std Dev 3.895
Gaus mean : 35.0258
Gaus Width: 3.6089
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

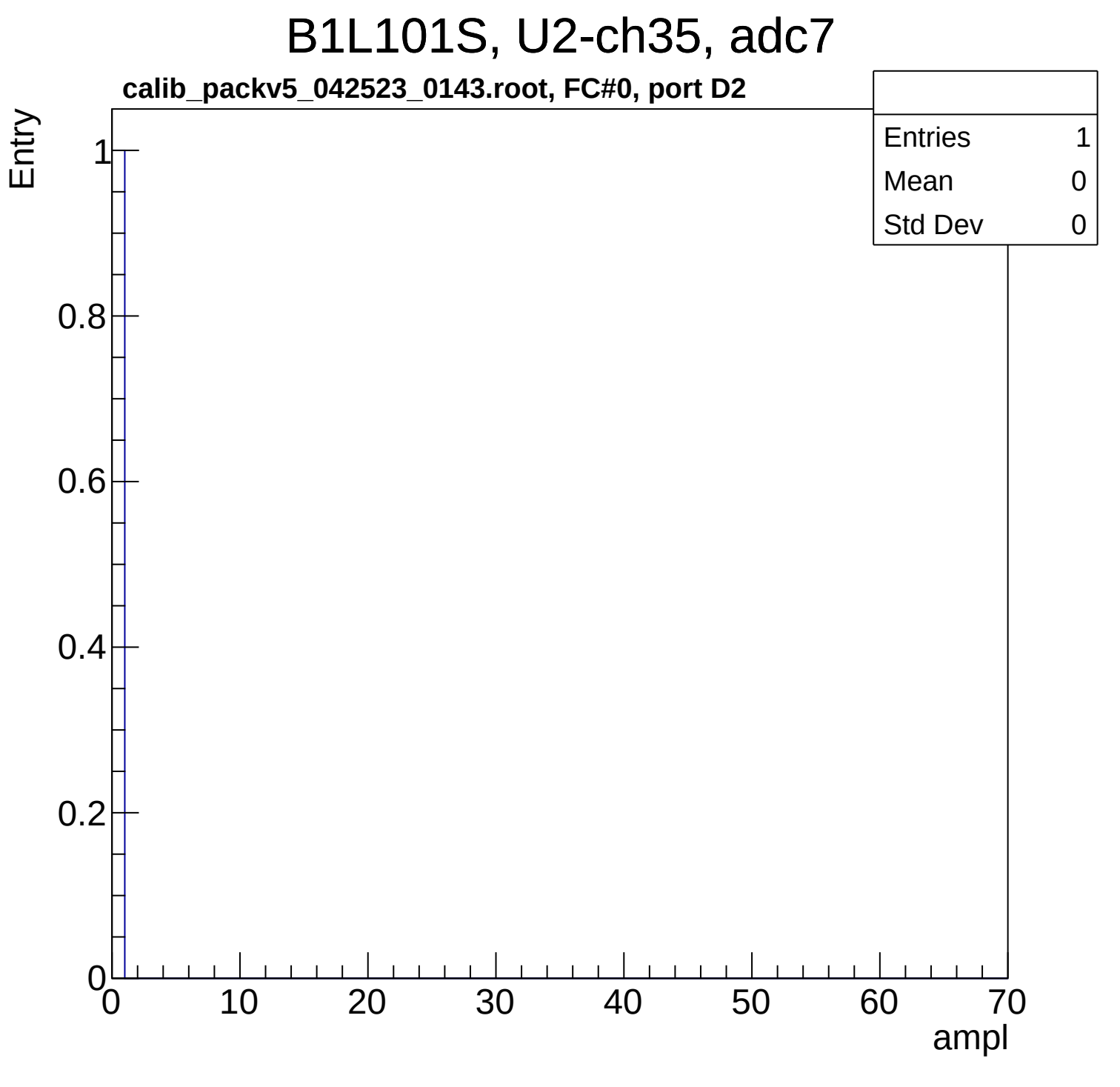

B1L101S, U2-ch35, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 80
Mean 42.65
Std Dev 3.811
Gaus mean : 42.9287
Gaus Width: 4.4675
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

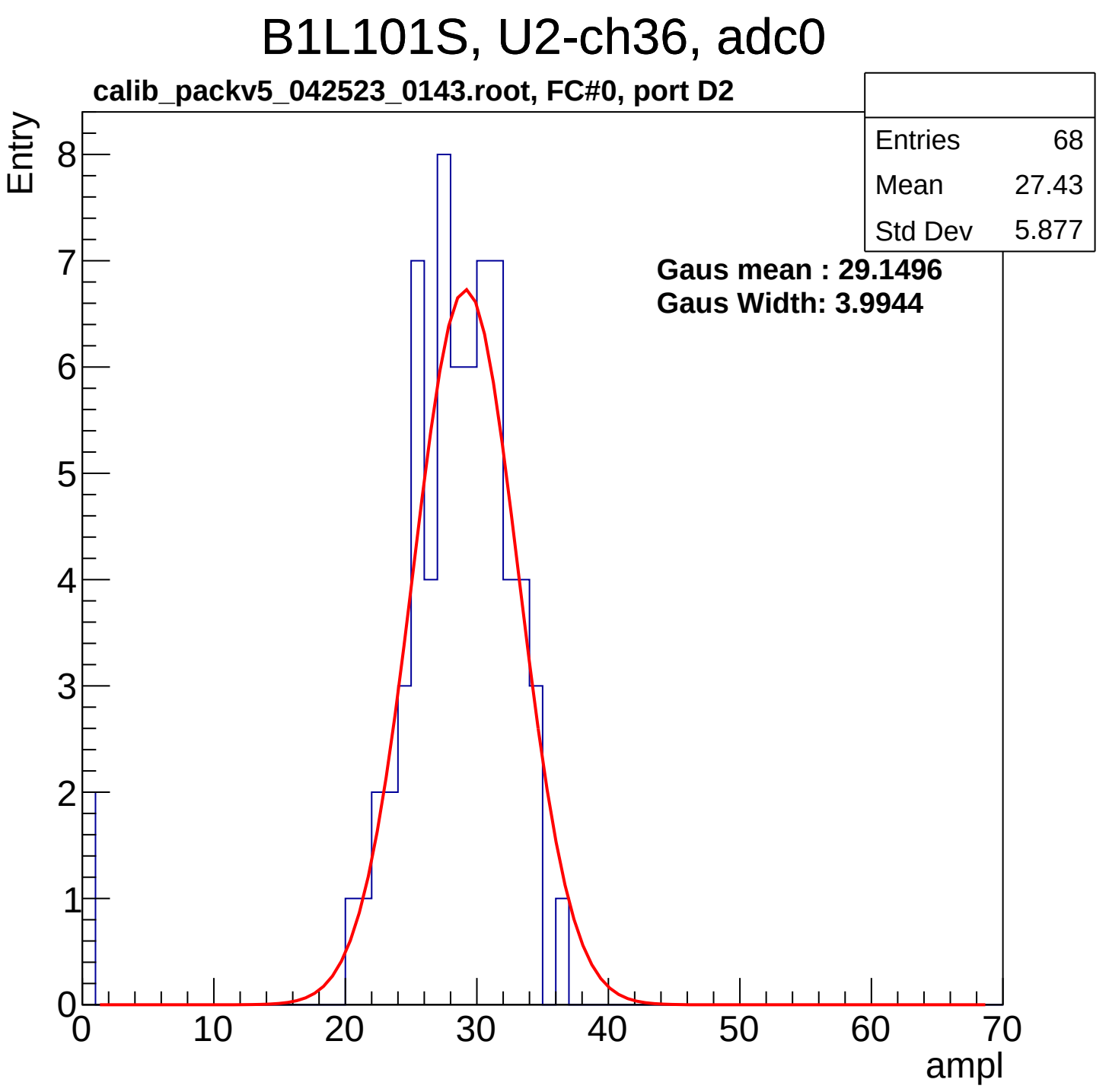

B1L101S, U2-ch35, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 48.87
Std Dev 3.761
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

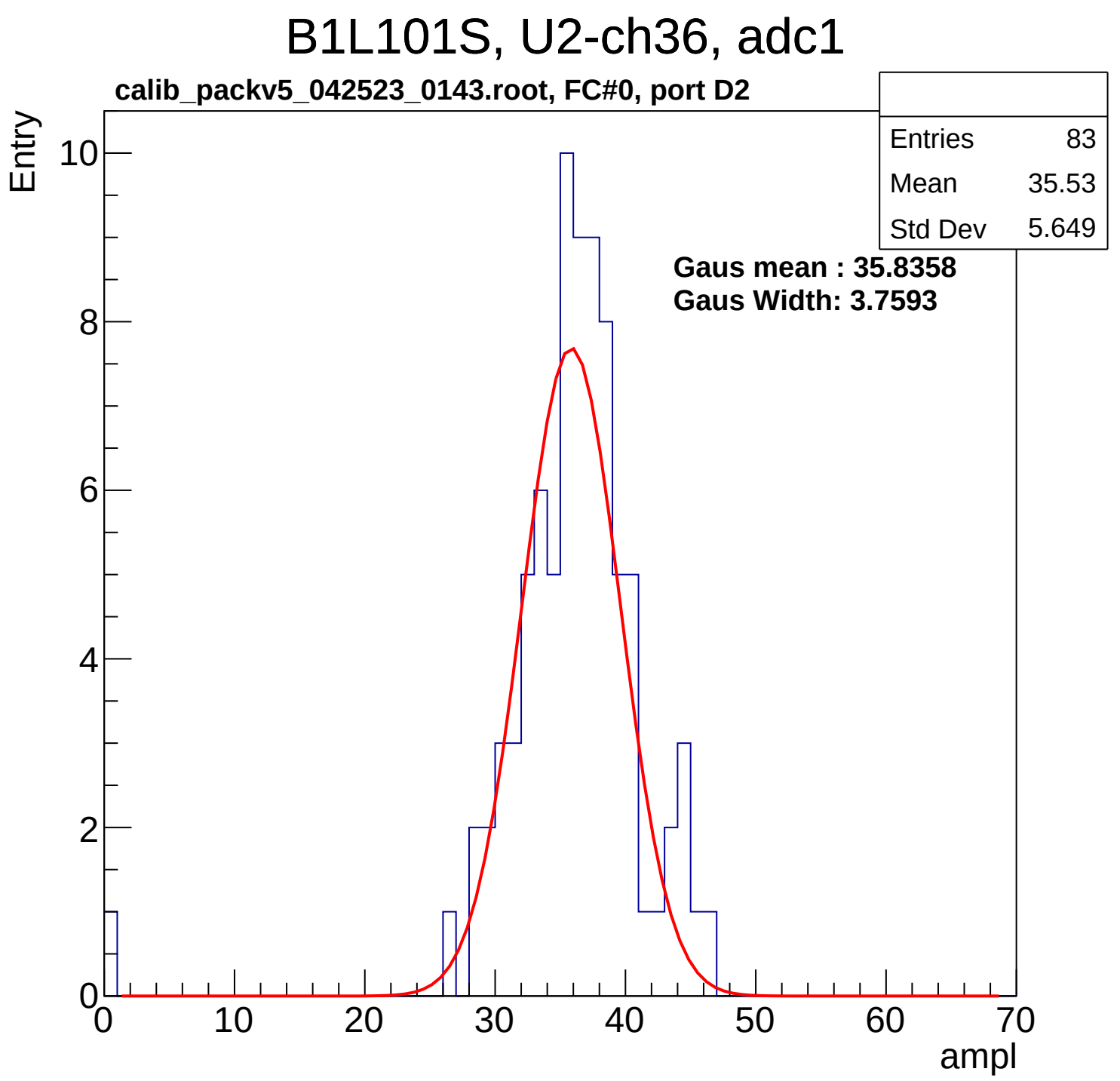

B1L101S, U2-ch35, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 54.57
Std Dev 2.886
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

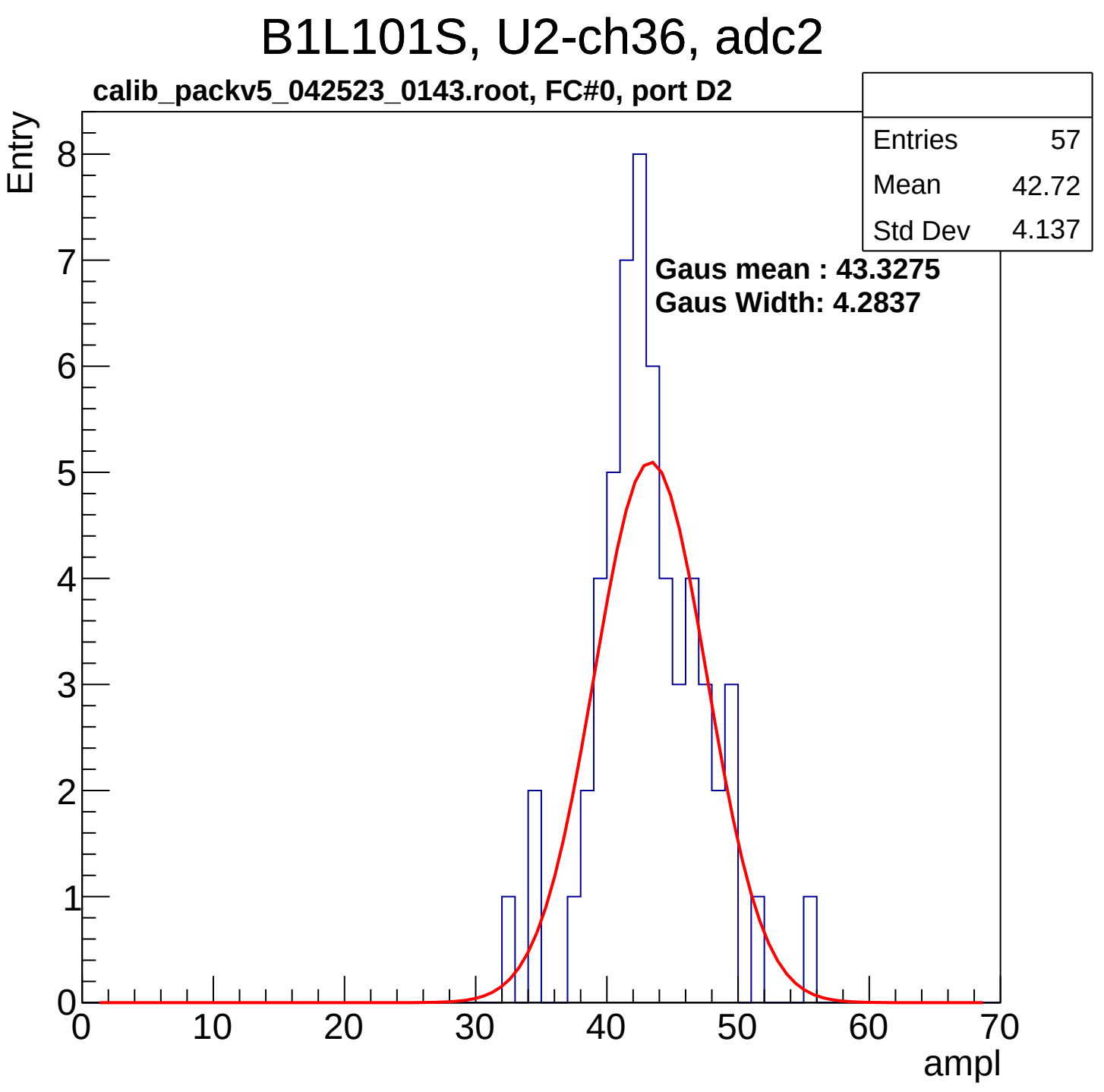

B1L101S, U2-ch35, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 57.9
Std Dev 8.614
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

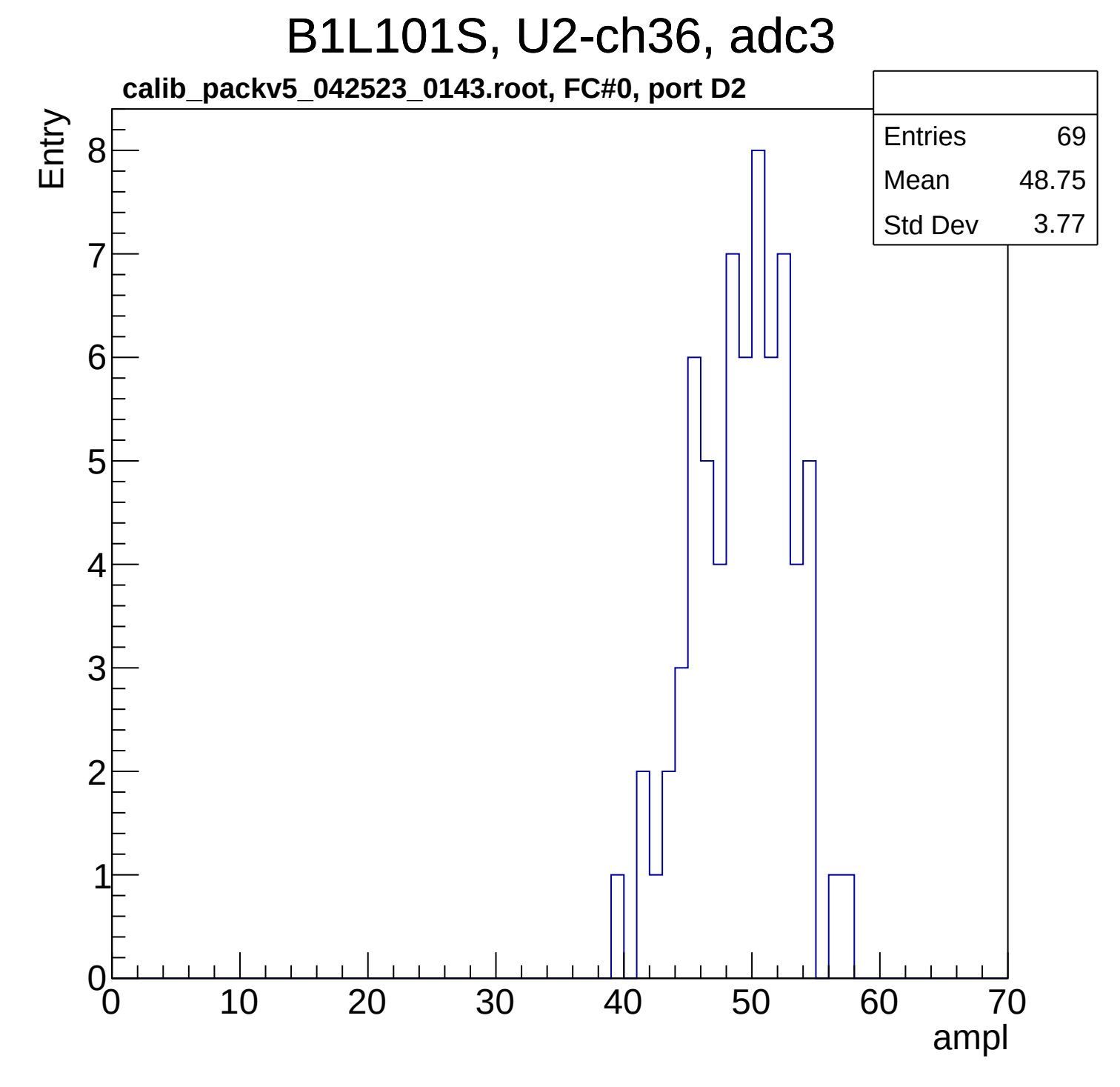

B1L101S, U2-ch35, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 16
Mean 61.06
Std Dev 2.135
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

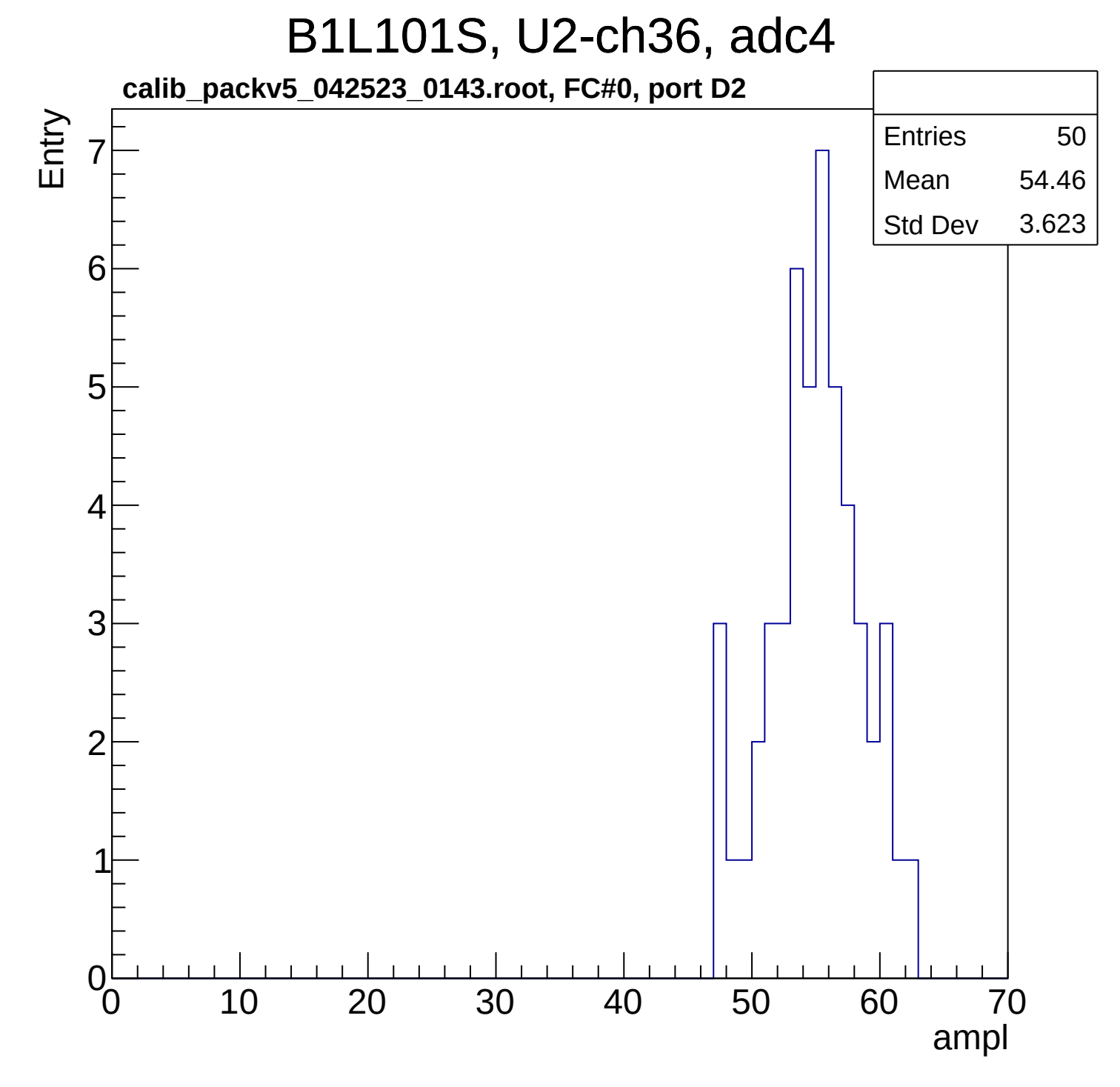

B1L101S, U2-ch35, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

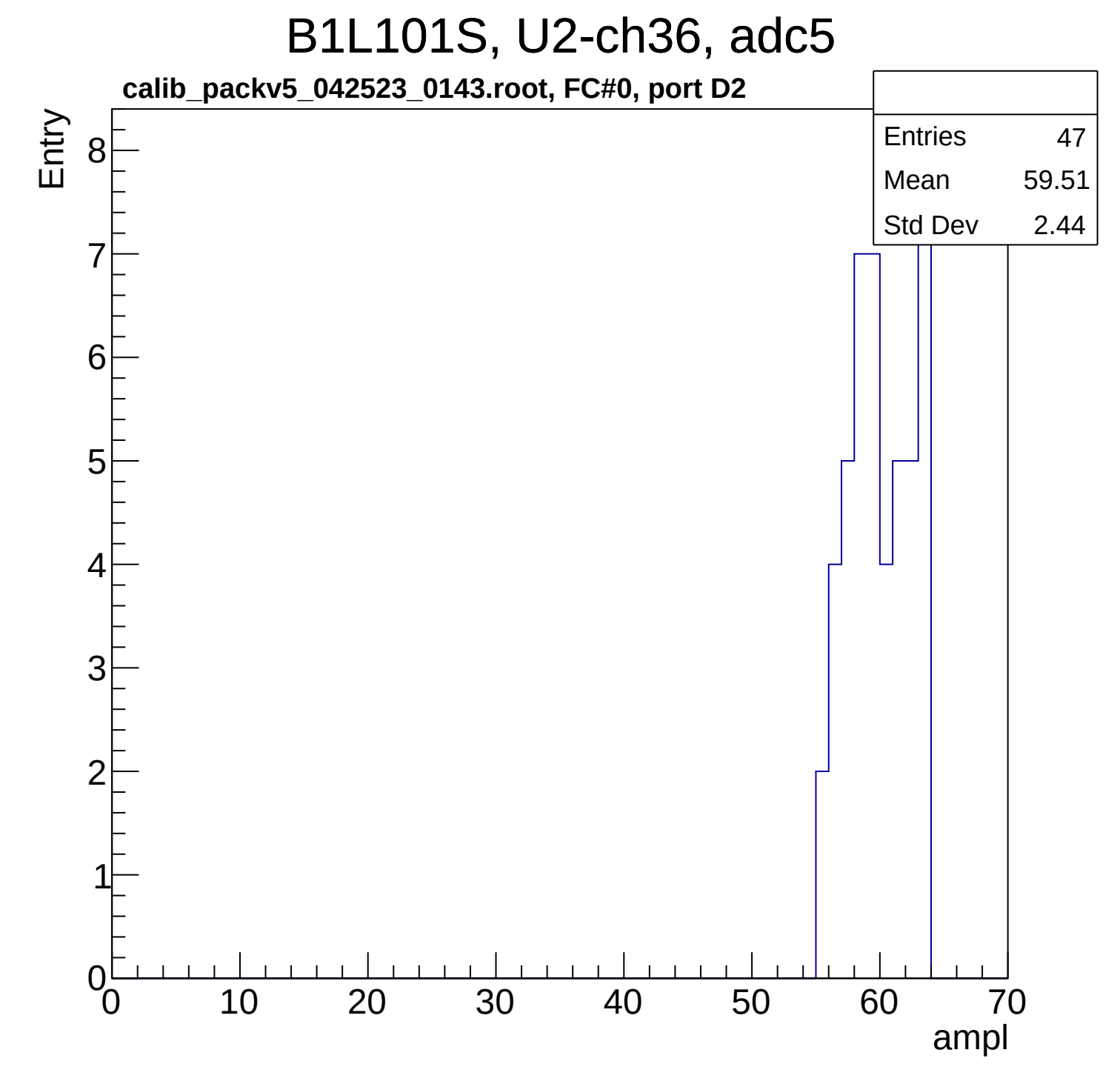

B1L101S, U2-ch36, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 27.43
Std Dev 5.877
Gaus mean : 29.1496
Gaus Width: 3.9944
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

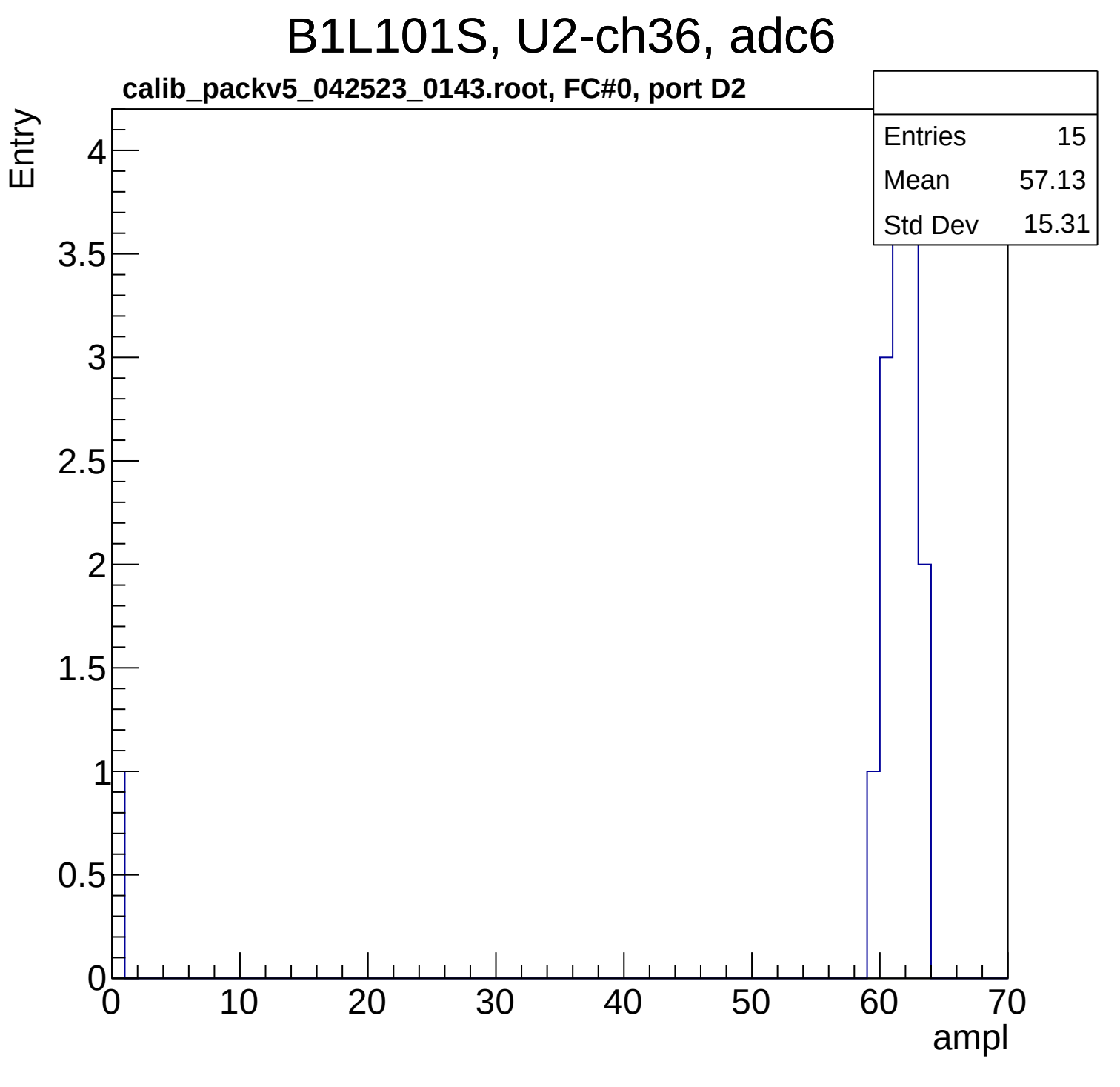

B1L101S, U2-ch36, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 83
Mean 35.53
Std Dev 5.649
Gaus mean : 35.8358
Gaus Width: 3.7593
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

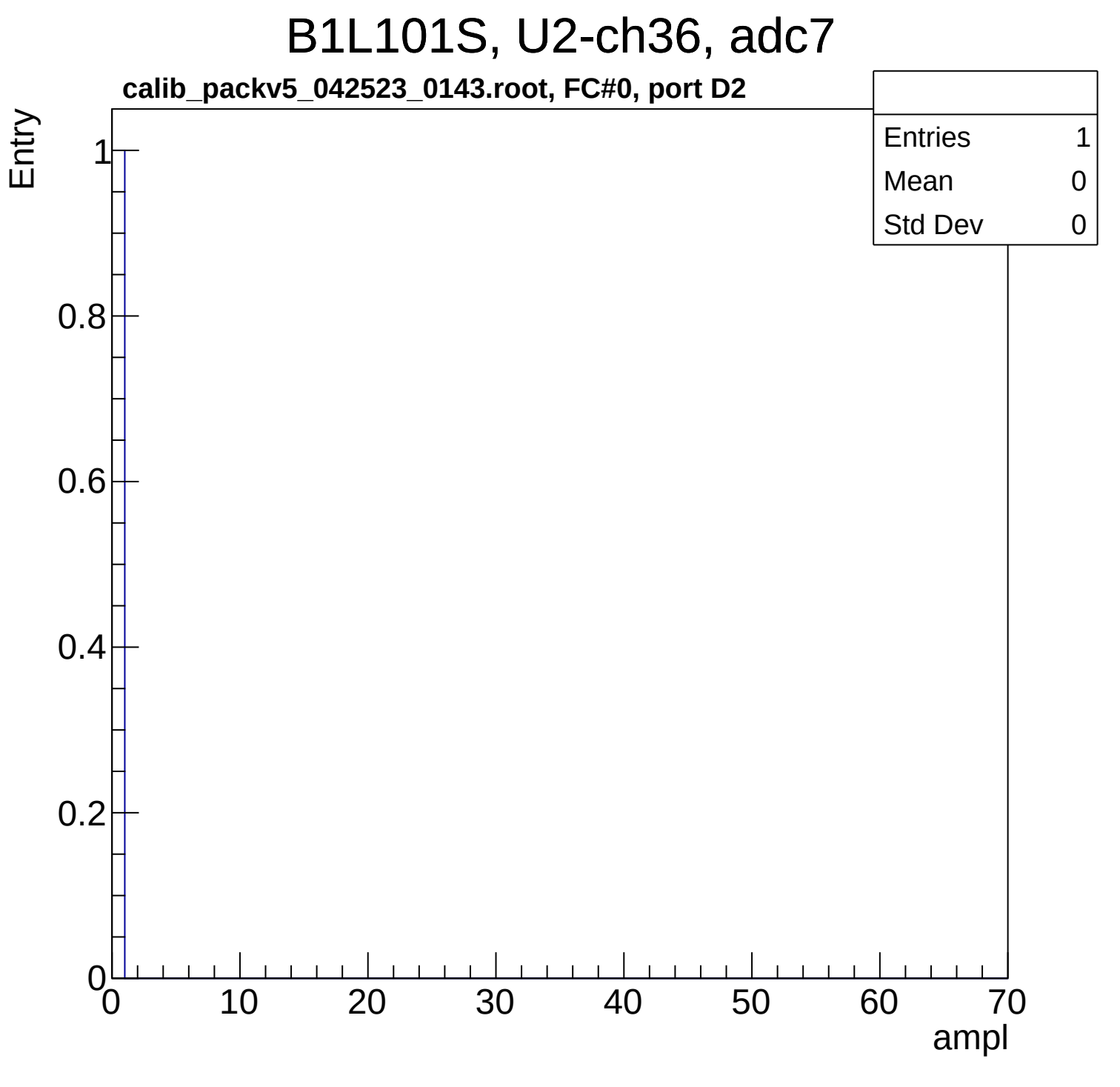

B1L101S, U2-ch36, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 42.72
Std Dev 4.137
Gaus mean : 43.3275
Gaus Width: 4.2837
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

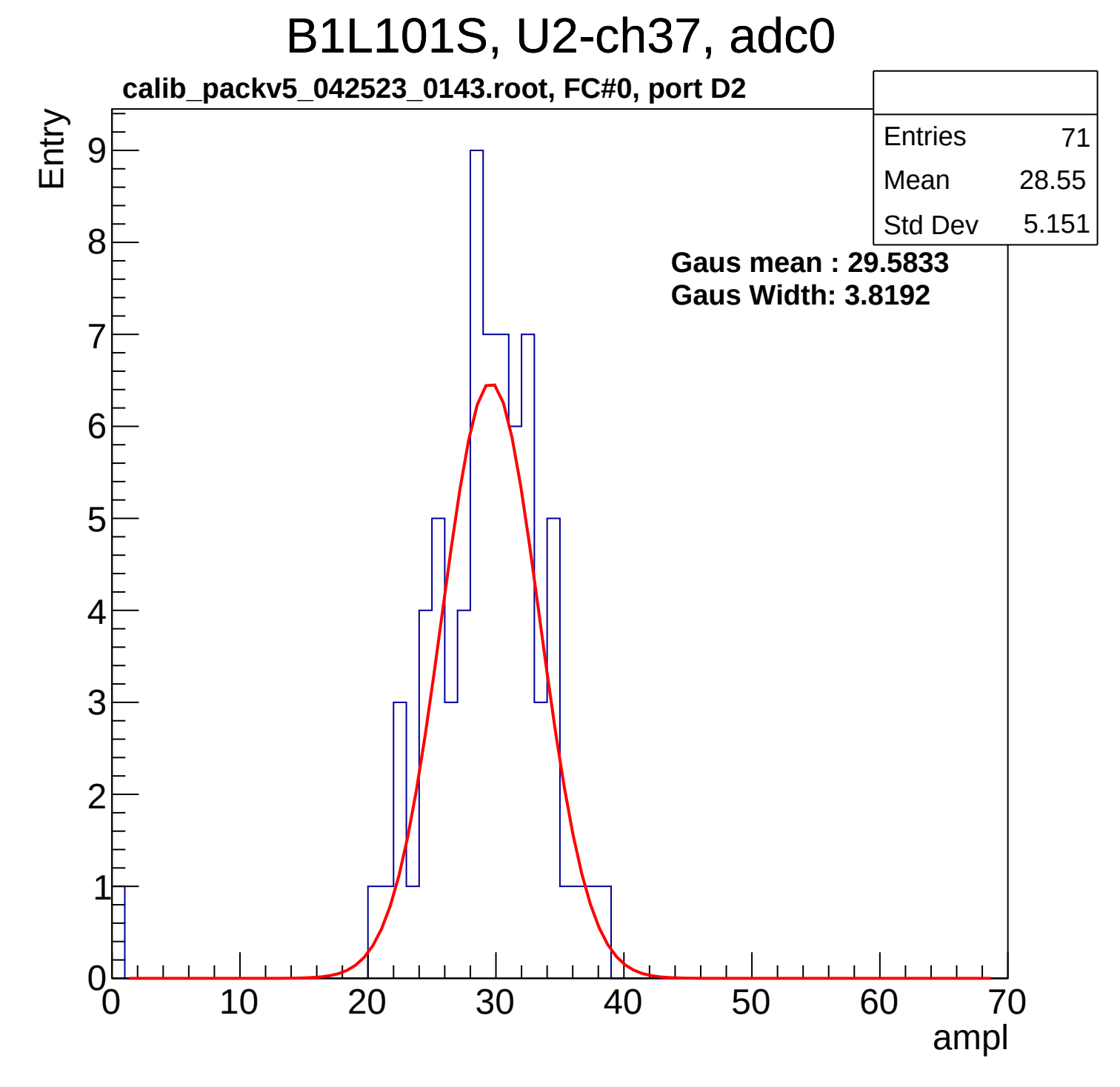

B1L101S, U2-ch36, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 48.75
Std Dev 3.77
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

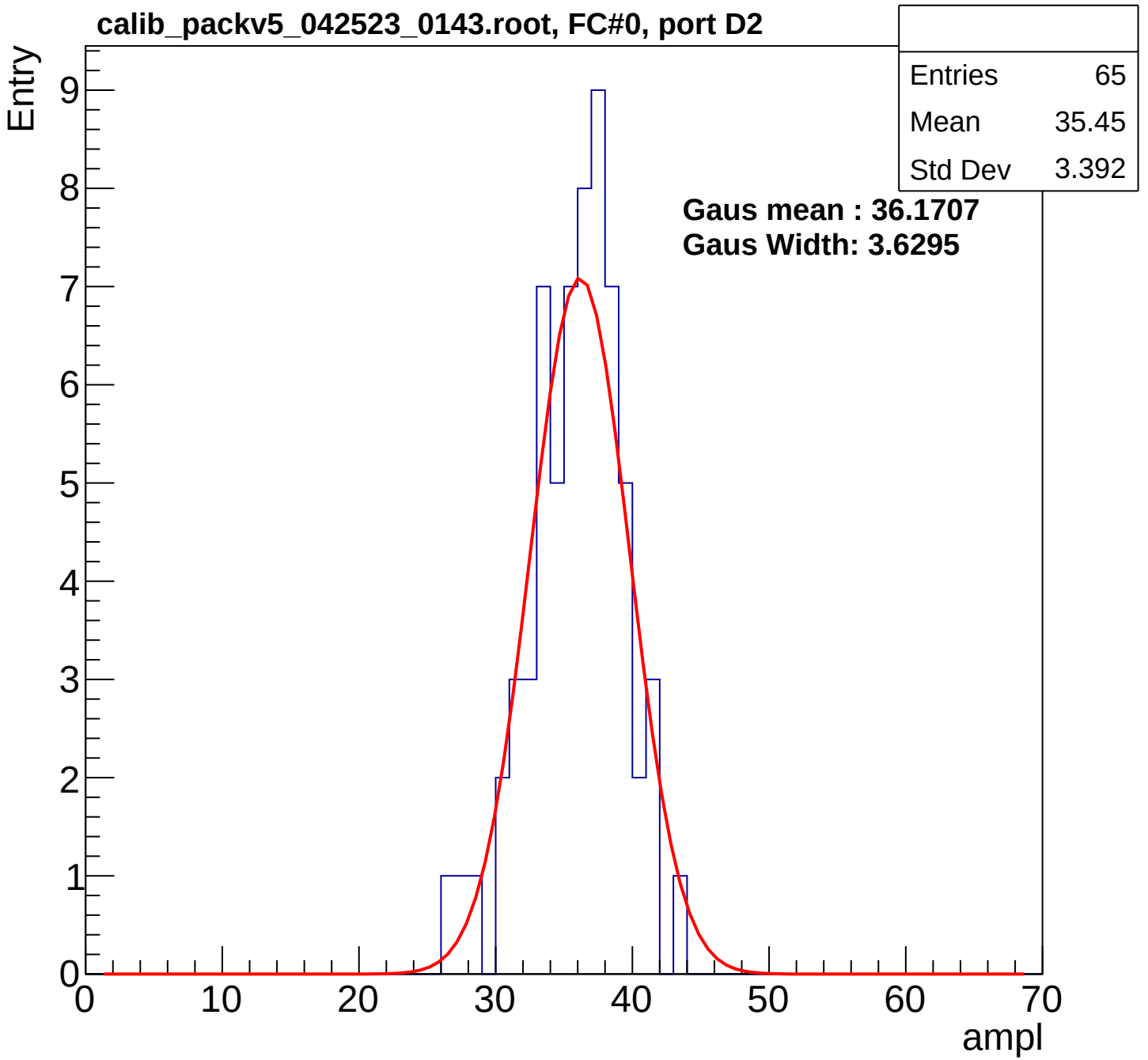

B1L101S, U2-ch36, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 54.46
Std Dev 3.623
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

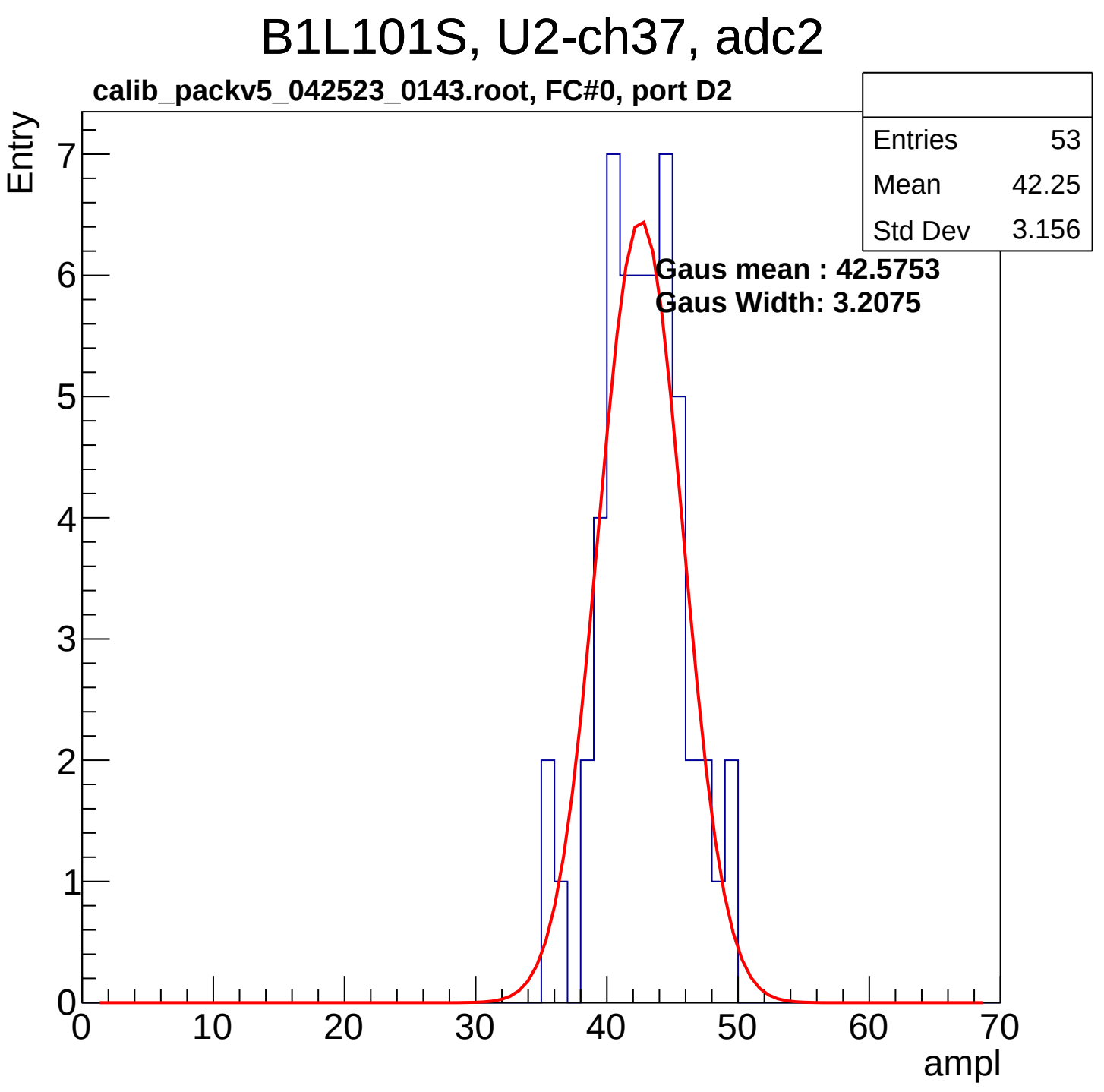

B1L101S, U2-ch36, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 59.51
Std Dev 2.44
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

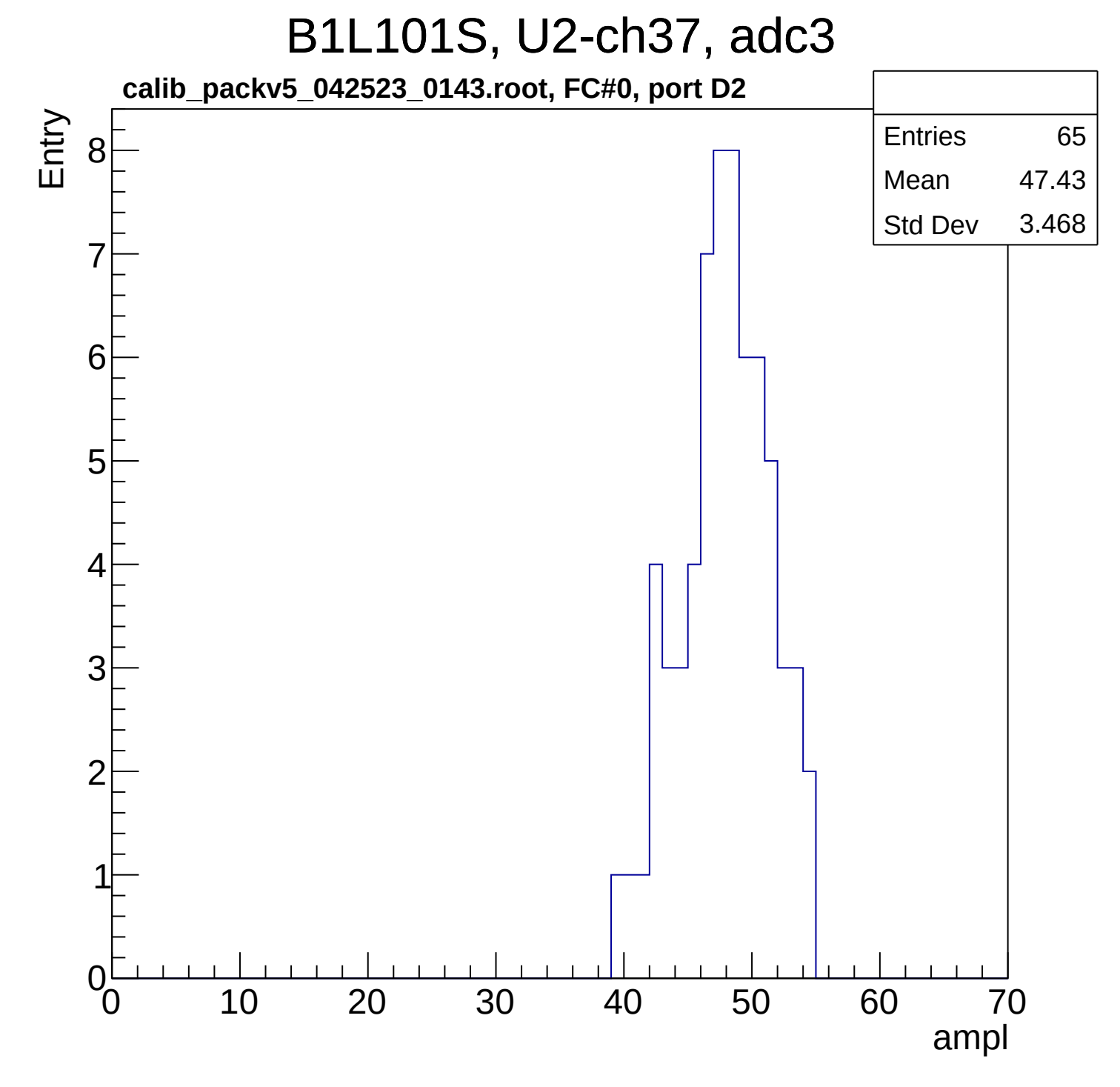

B1L101S, U2-ch36, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 15
Mean 57.13
Std Dev 15.31
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

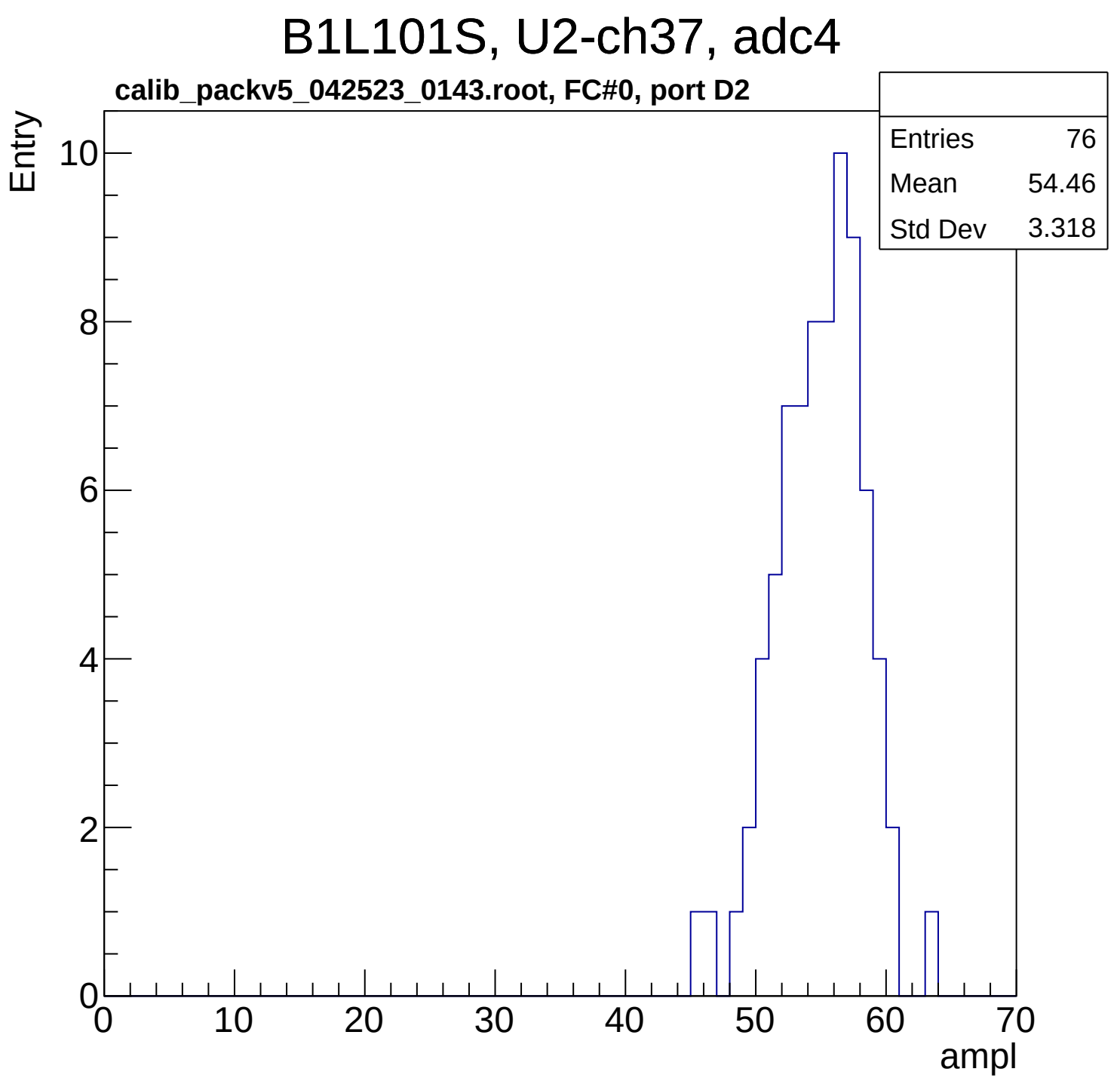

B1L101S, U2-ch36, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

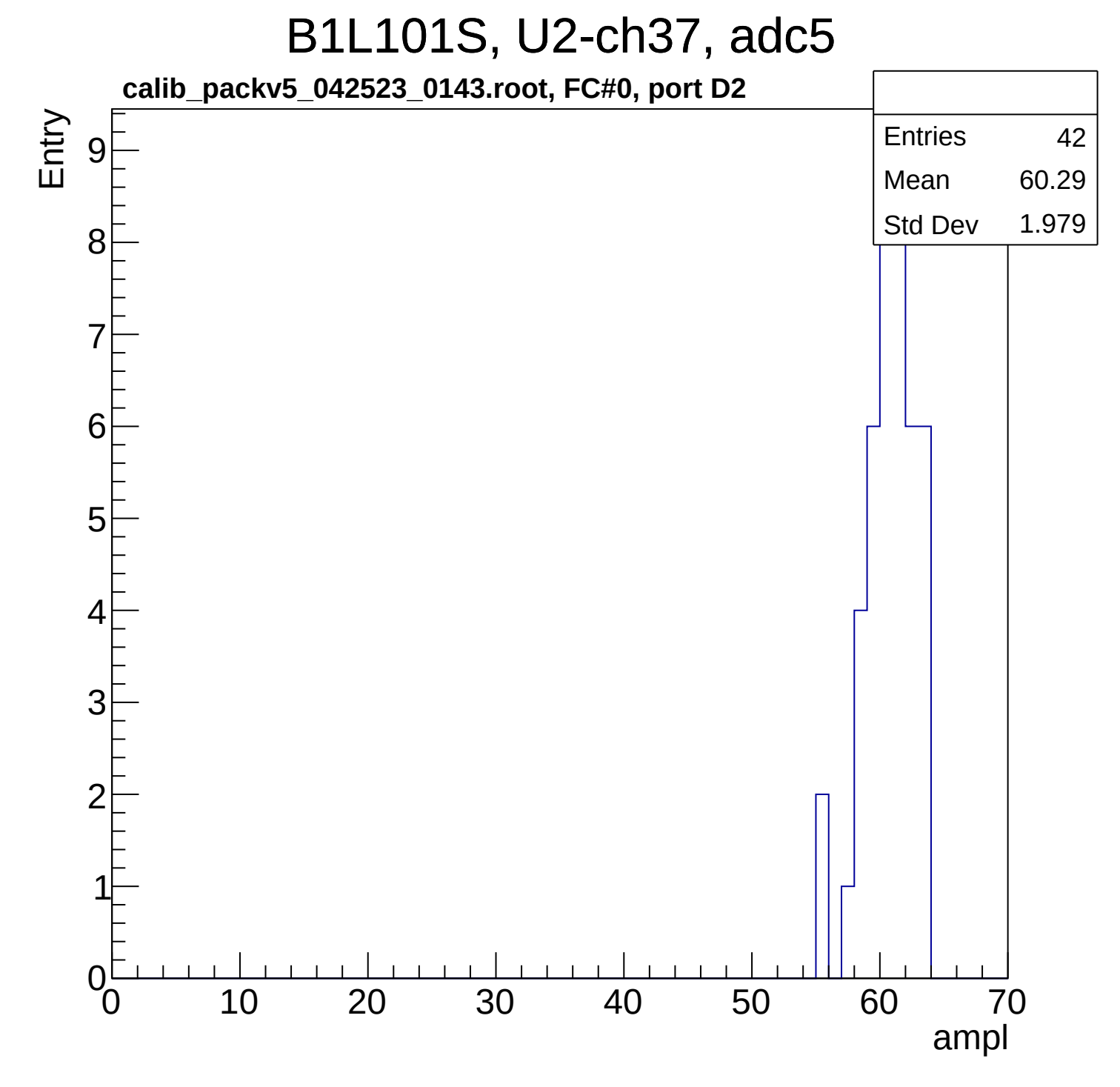

B1L101S, U2-ch37, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 28.55
Std Dev 5.151
Gaus mean : 29.5833
Gaus Width: 3.8192
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

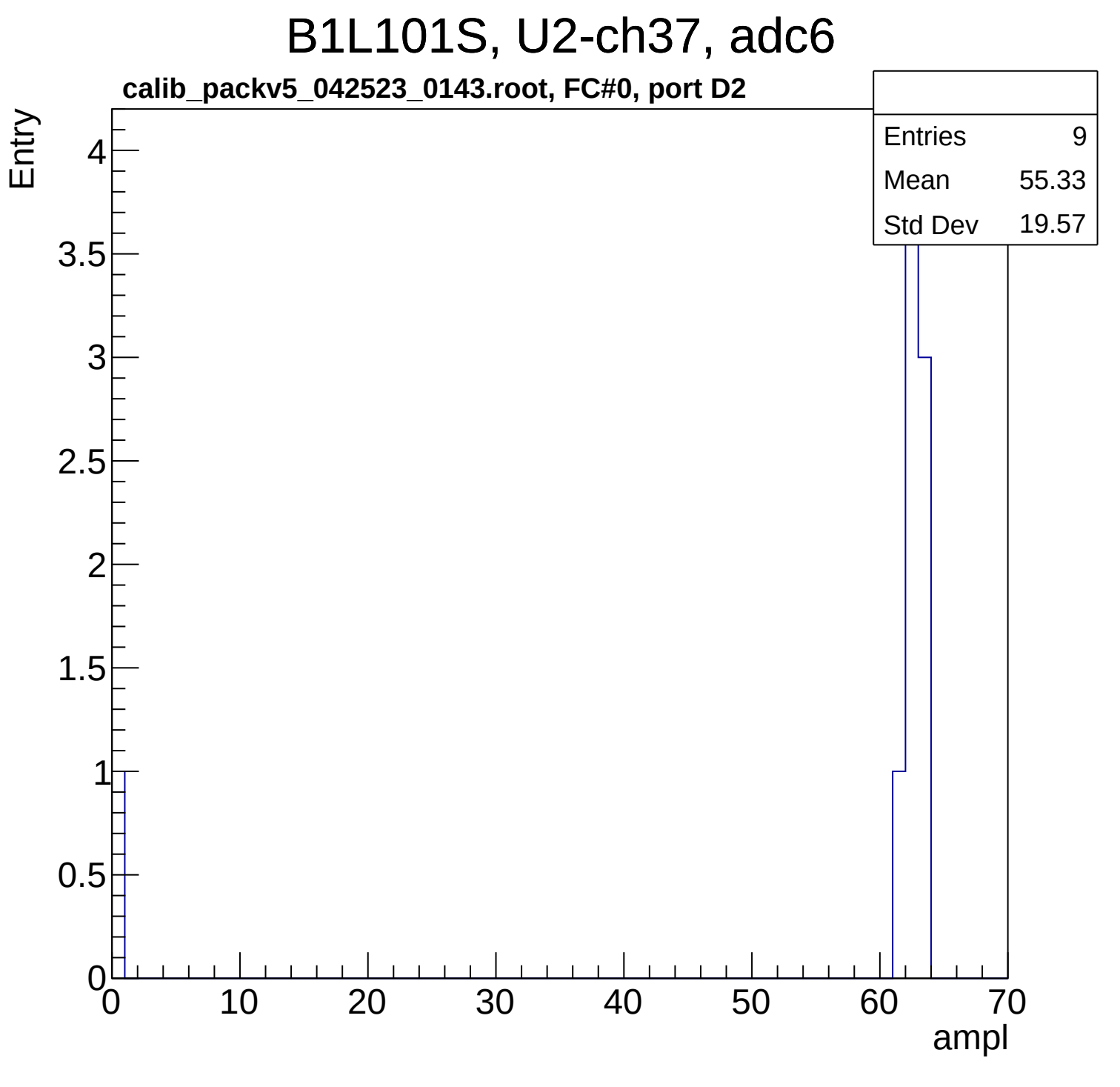

B1L101S, U2-ch37, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 35.45
Std Dev 3.392
Gaus mean : 36.1707
Gaus Width: 3.6295
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

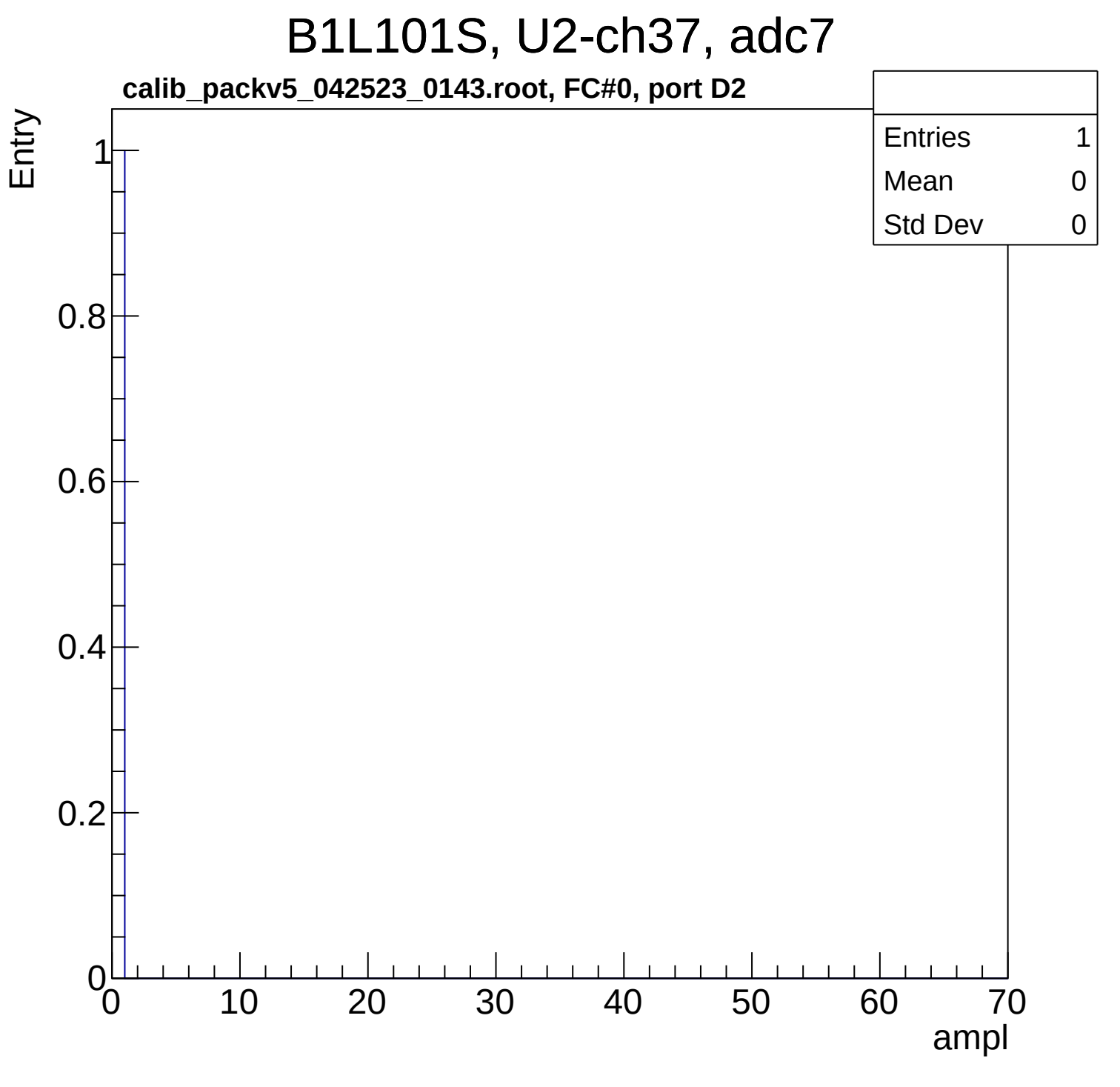

B1L101S, U2-ch37, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 42.25
Std Dev 3.156
Gaus mean : 42.5753
Gaus Width: 3.2075
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

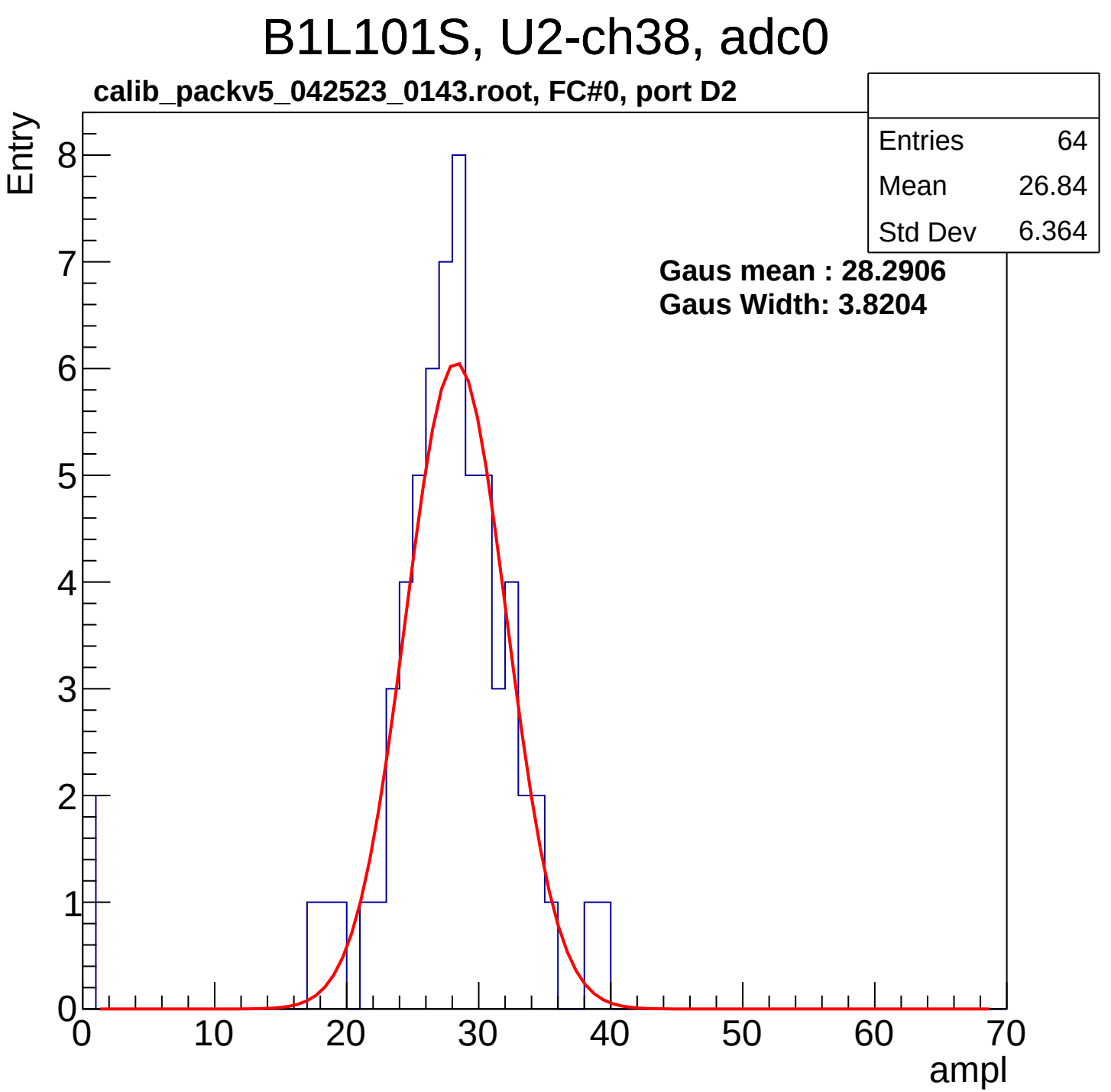

B1L101S, U2-ch37, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 47.43
Std Dev 3.468
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

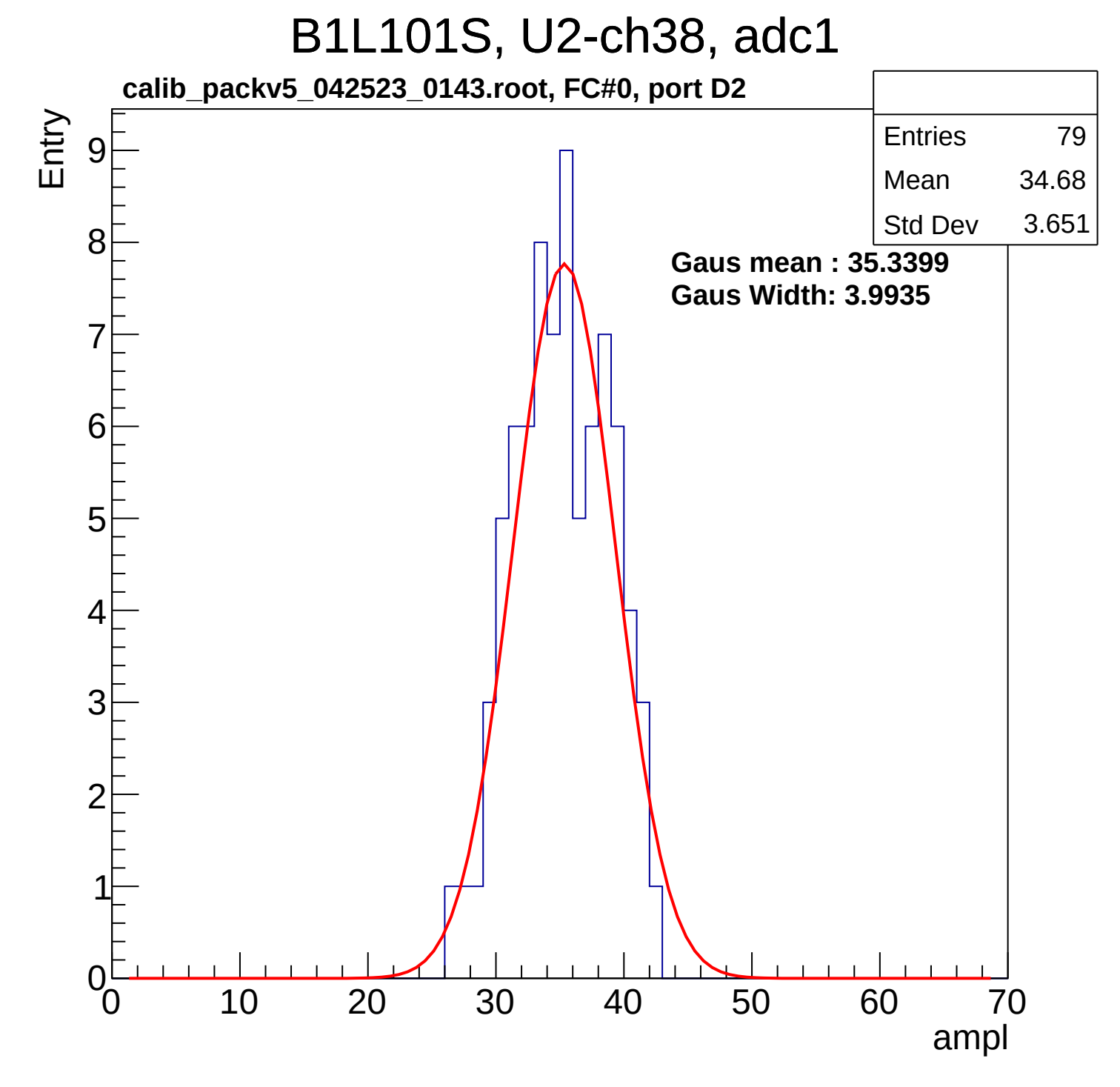

B1L101S, U2-ch37, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 54.46
Std Dev 3.318
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

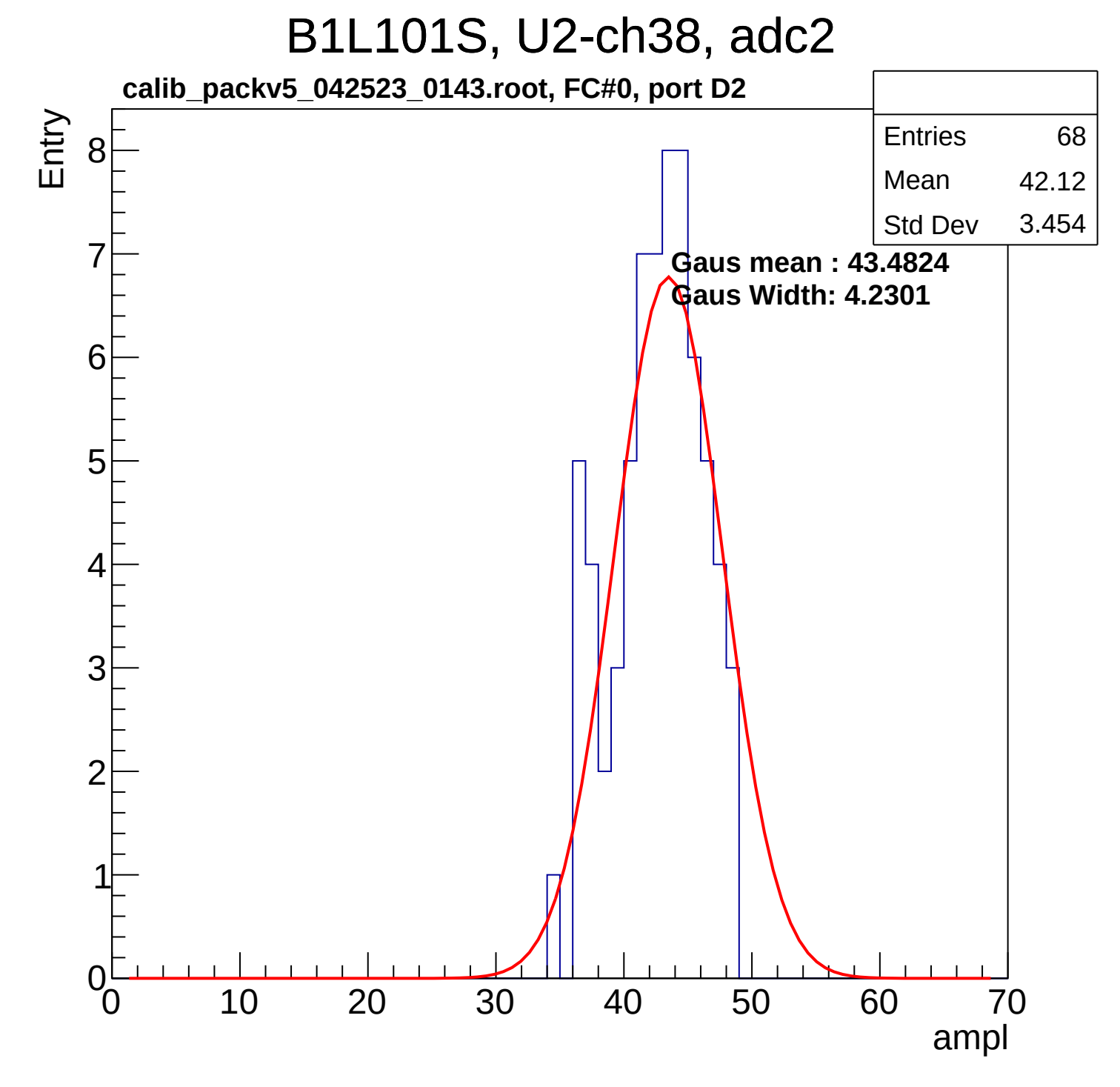

B1L101S, U2-ch37, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 60.29
Std Dev 1.979
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

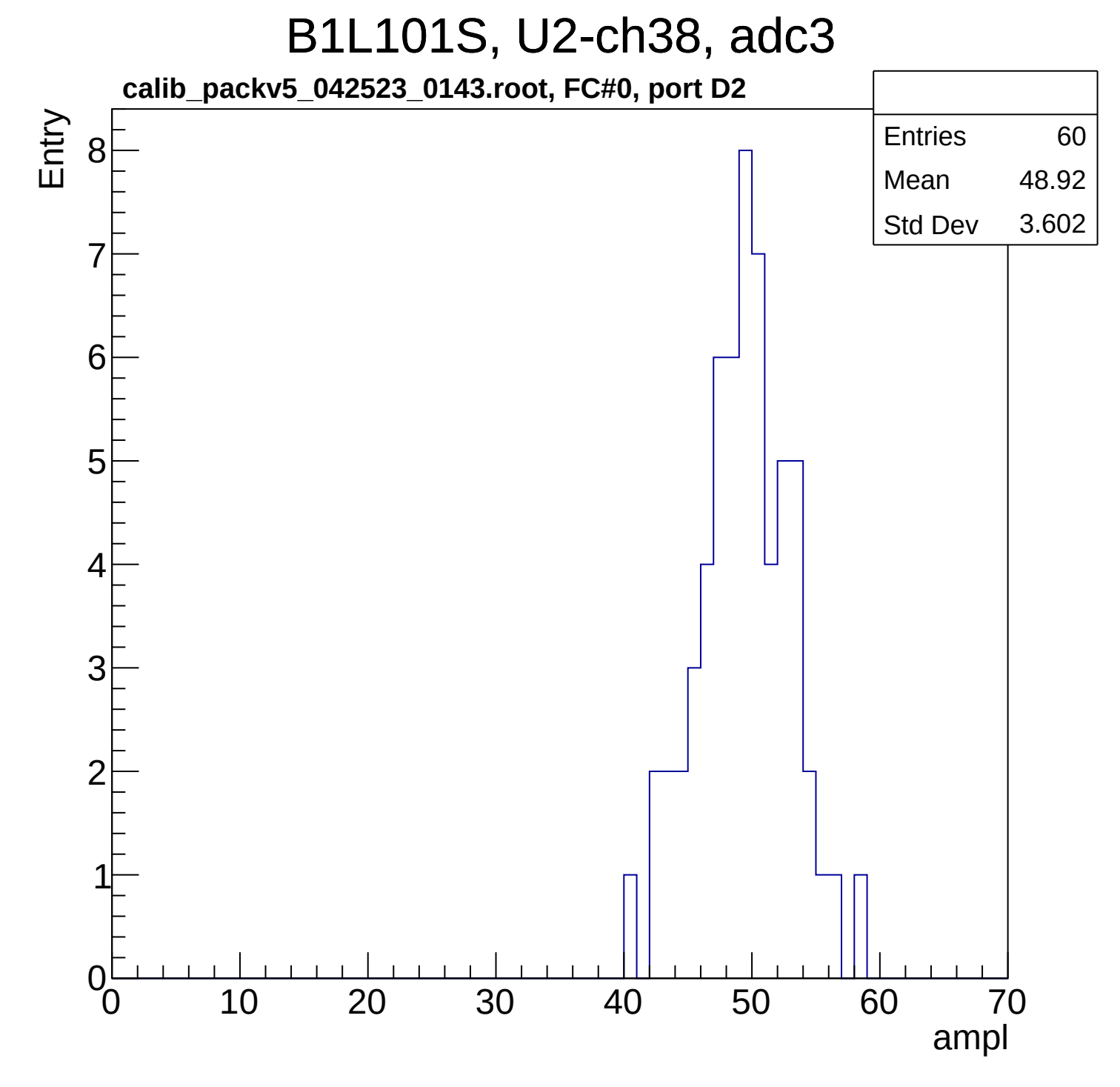

B1L101S, U2-ch37, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 55.33
Std Dev 19.57
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

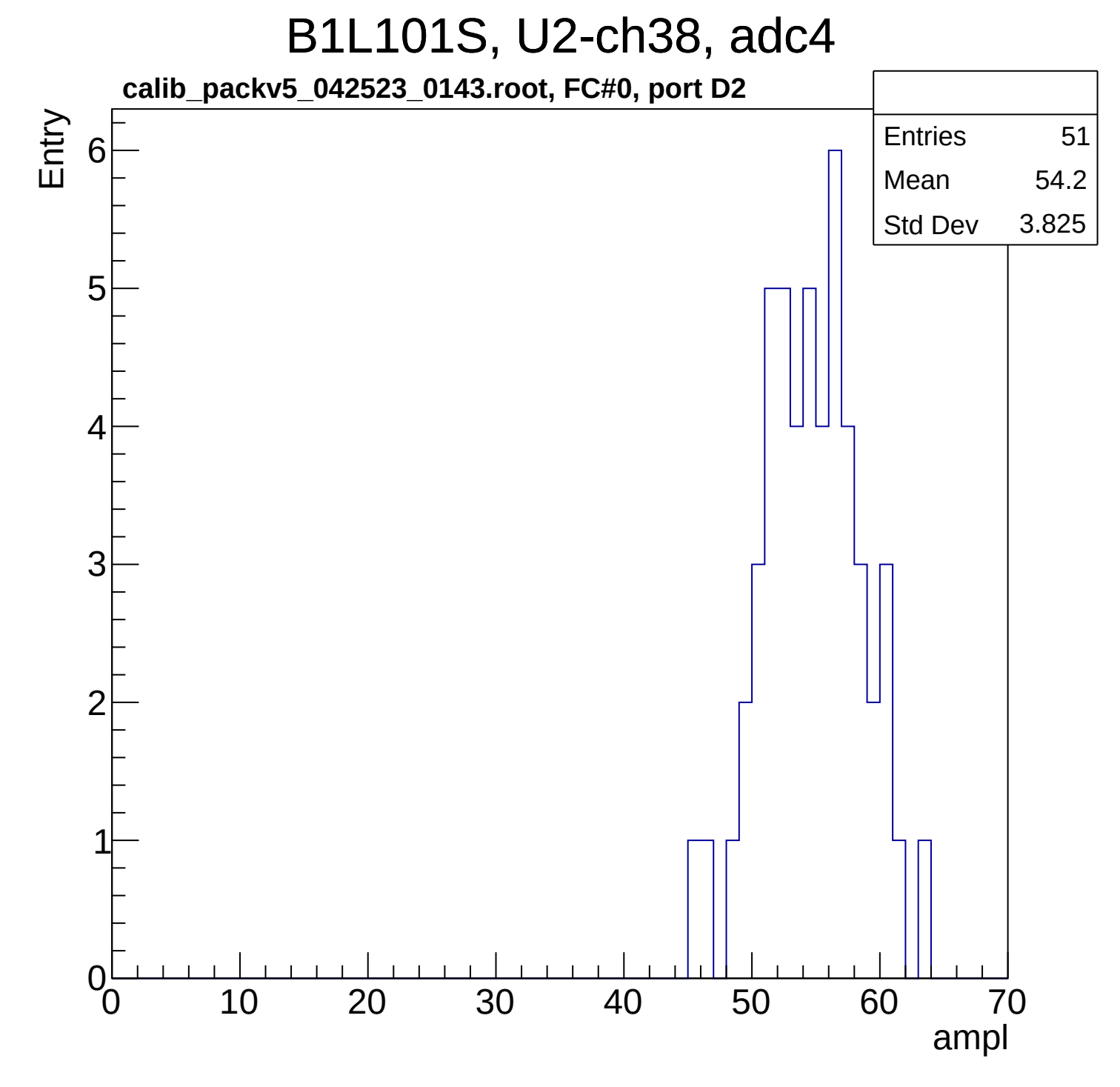

B1L101S, U2-ch37, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

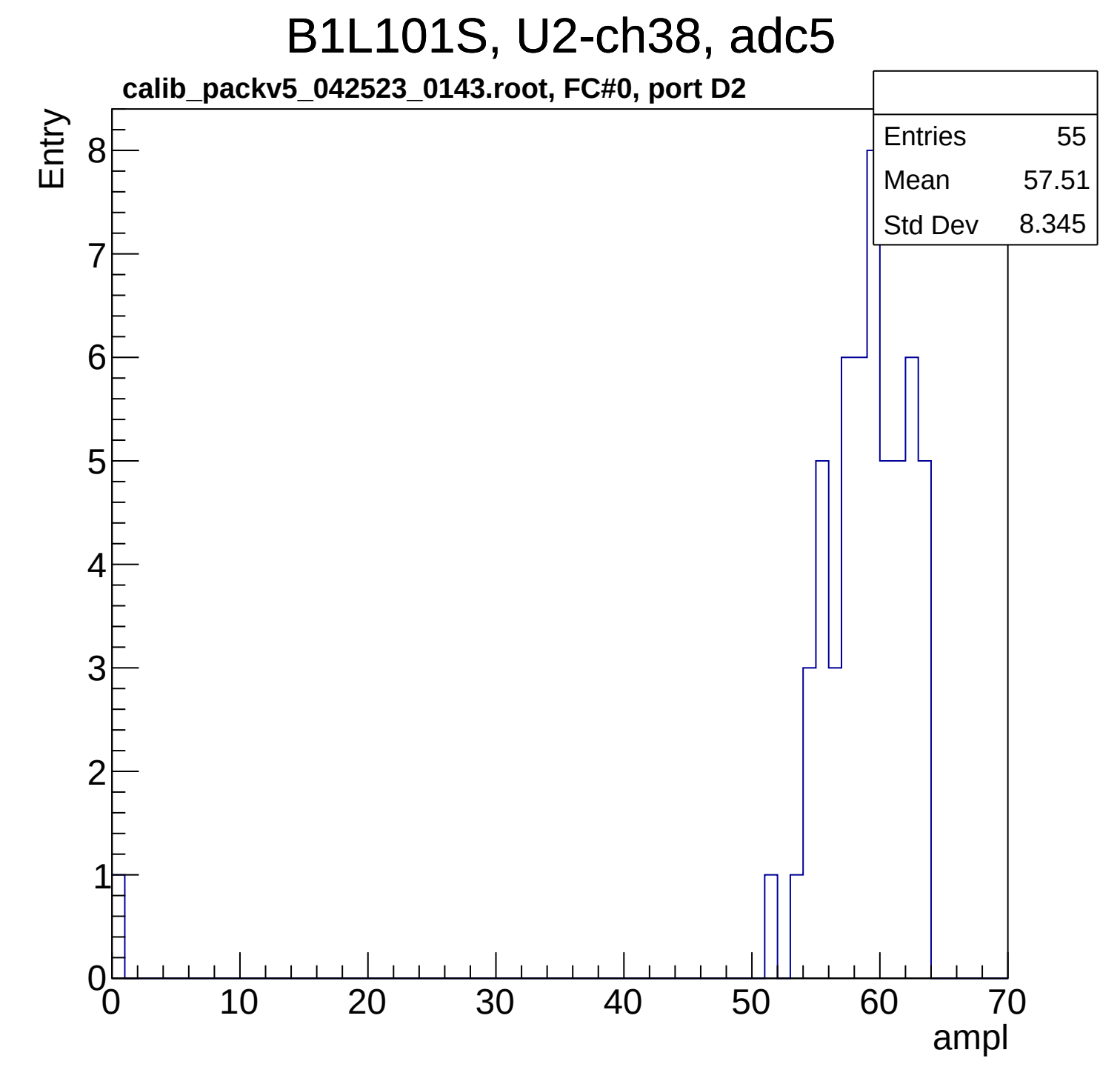

B1L101S, U2-ch38, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 26.84
Std Dev 6.364
Gaus mean : 28.2906
Gaus Width: 3.8204
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

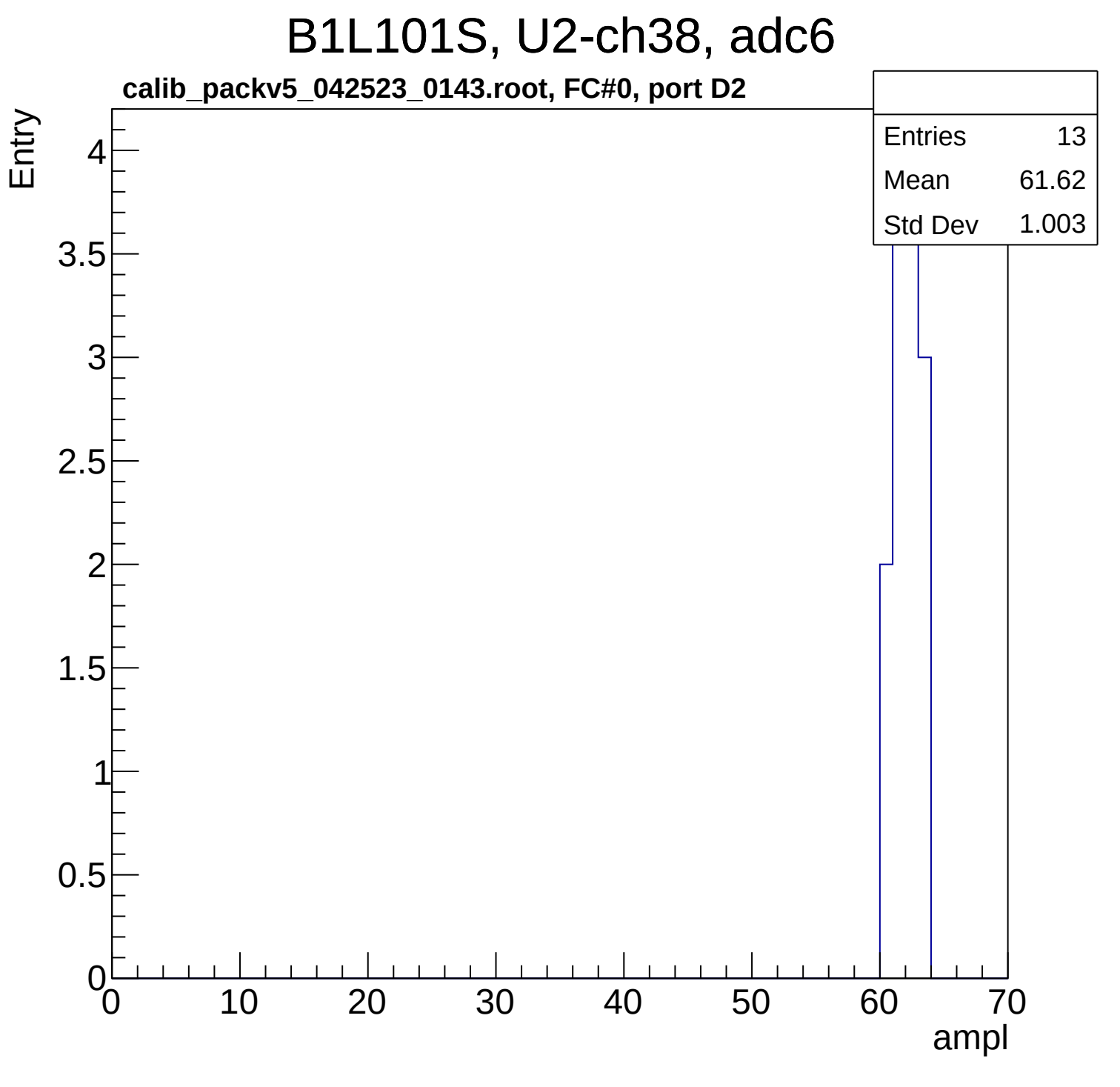

B1L101S, U2-ch38, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 34.68
Std Dev 3.651
Gaus mean : 35.3399
Gaus Width: 3.9935
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

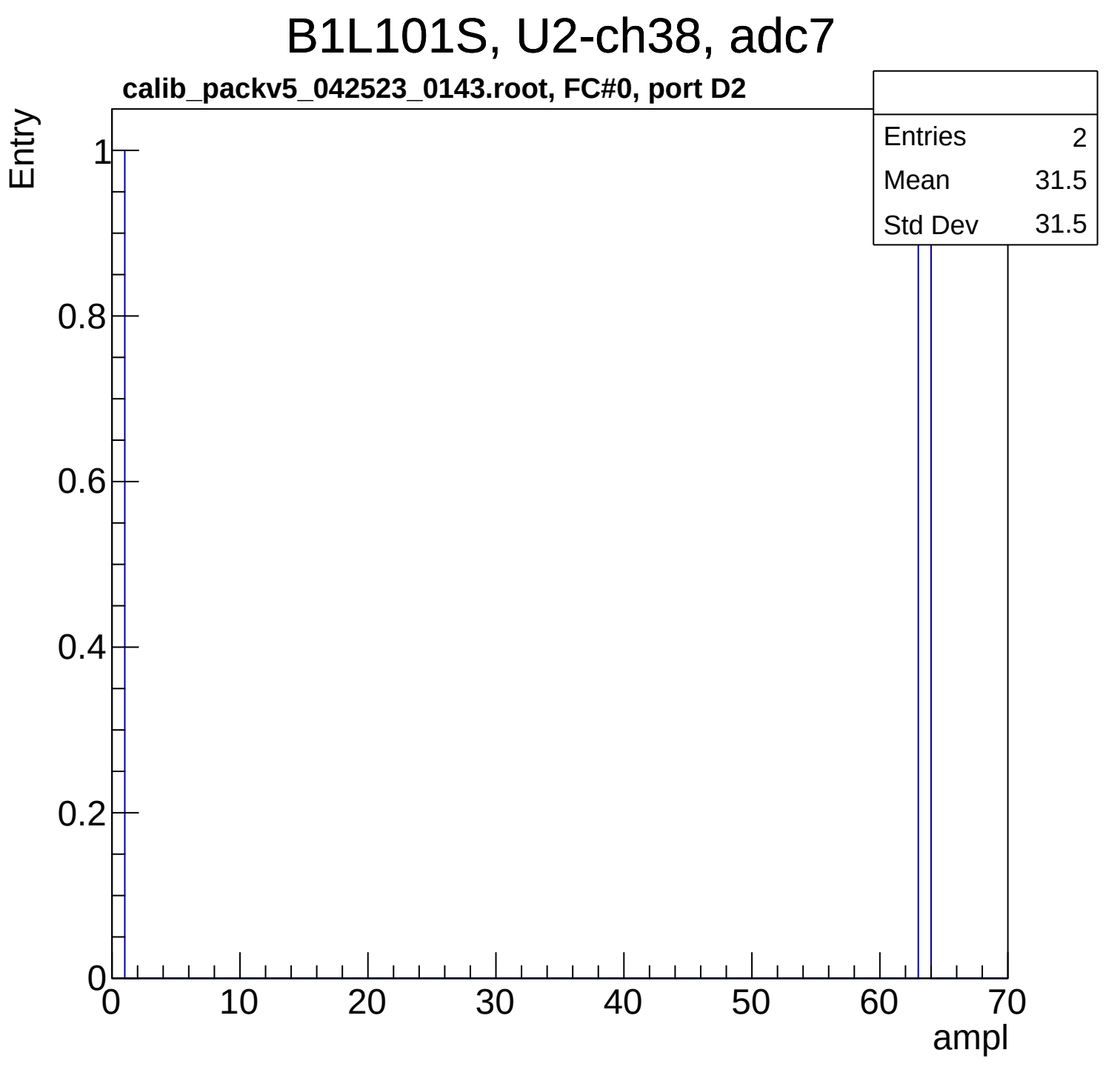

B1L101S, U2-ch38, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 42.12
Std Dev 3.454
Gaus mean : 43.4824
Gaus Width: 4.2301
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

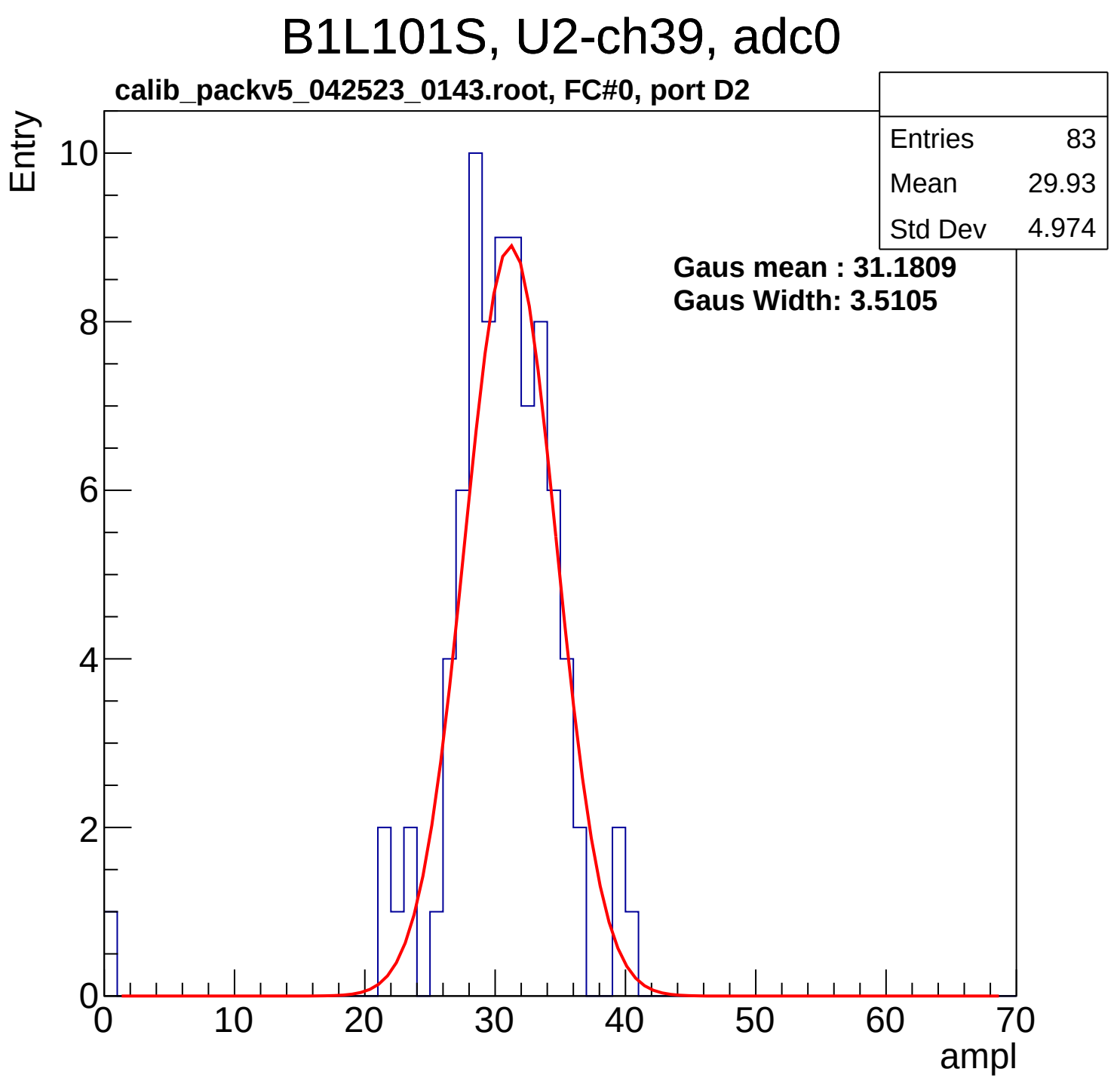

B1L101S, U2-ch38, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 48.92
Std Dev 3.602
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

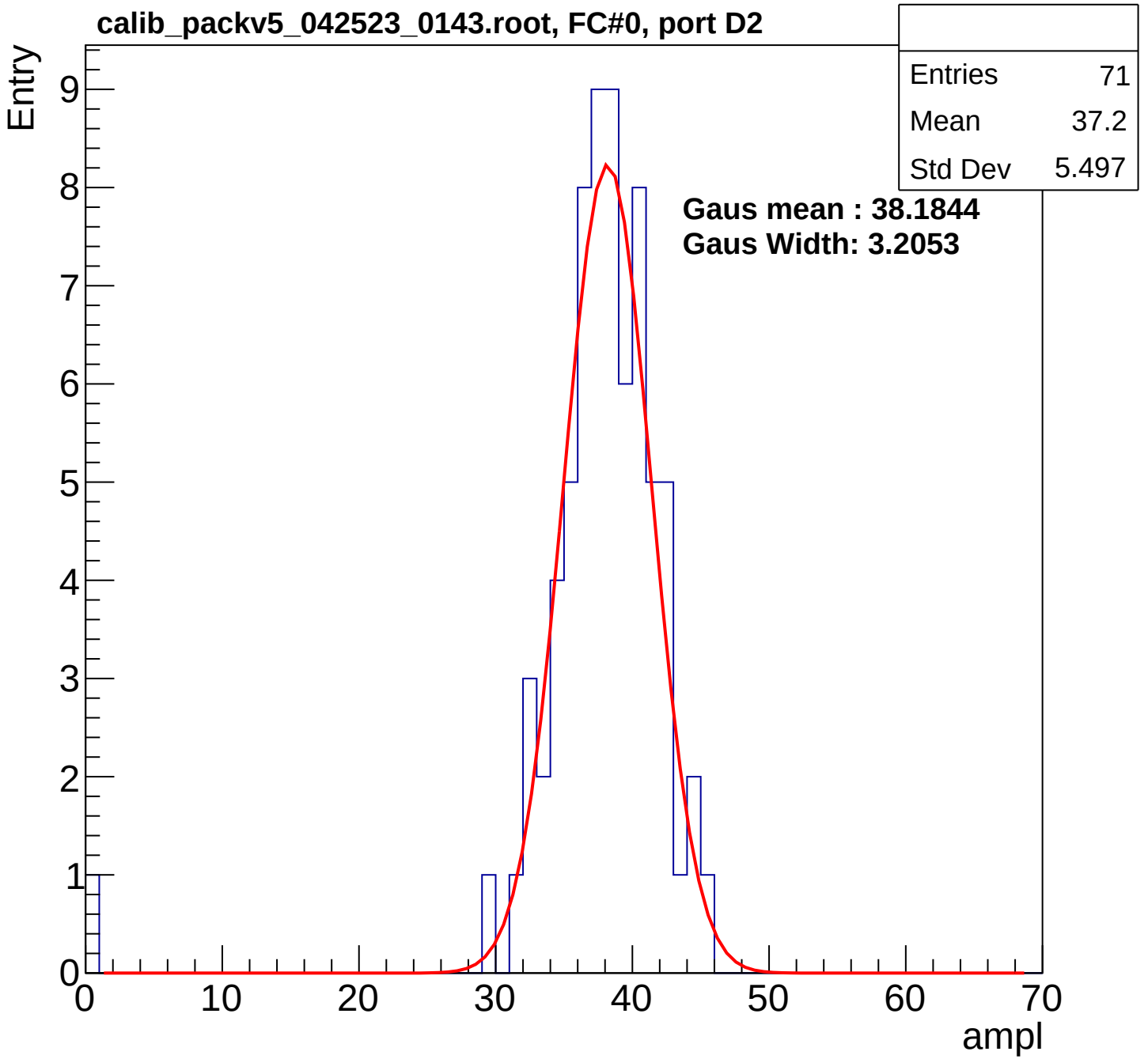

B1L101S, U2-ch38, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 54.2
Std Dev 3.825
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

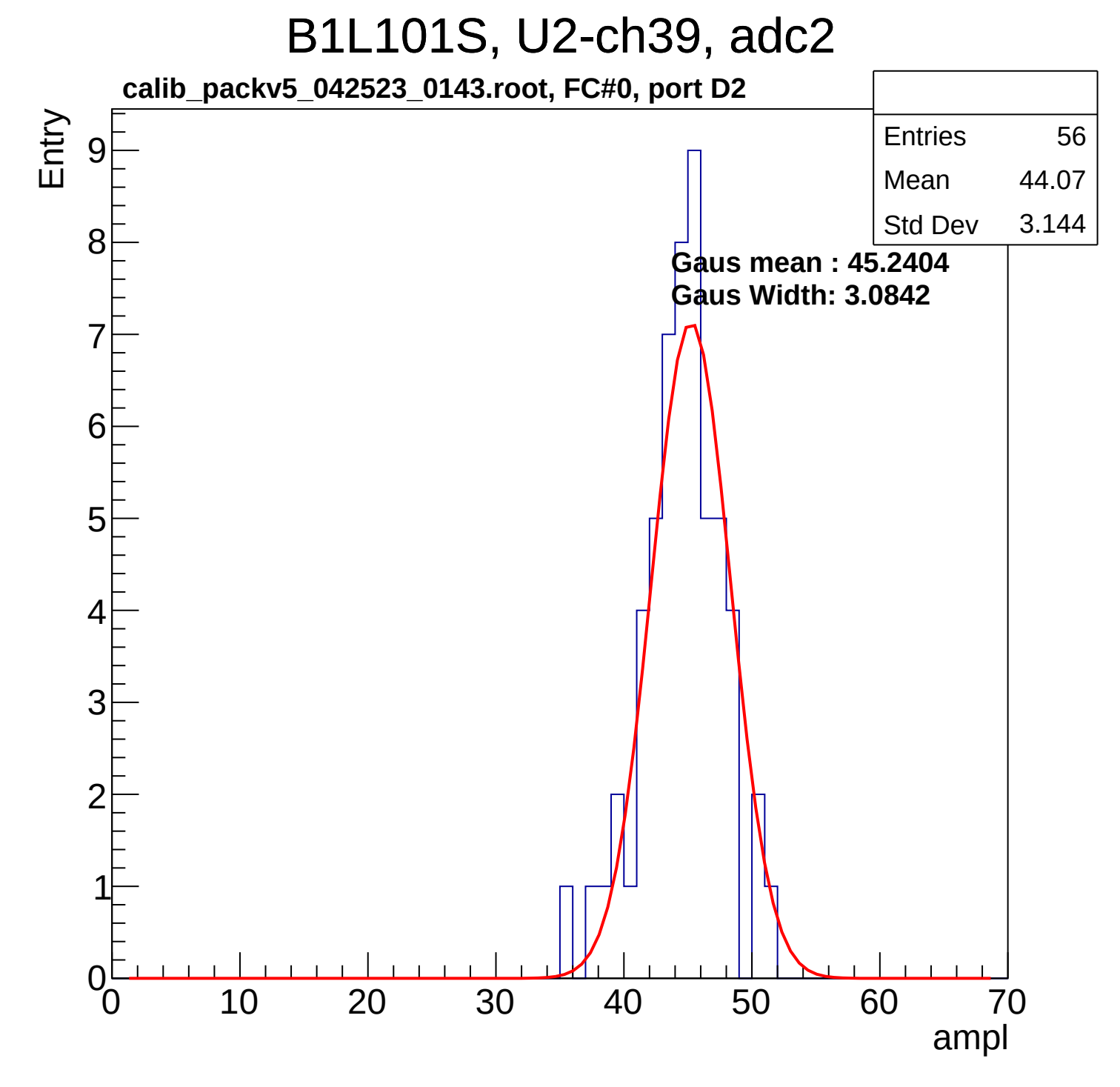

B1L101S, U2-ch38, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 57.51
Std Dev 8.345
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

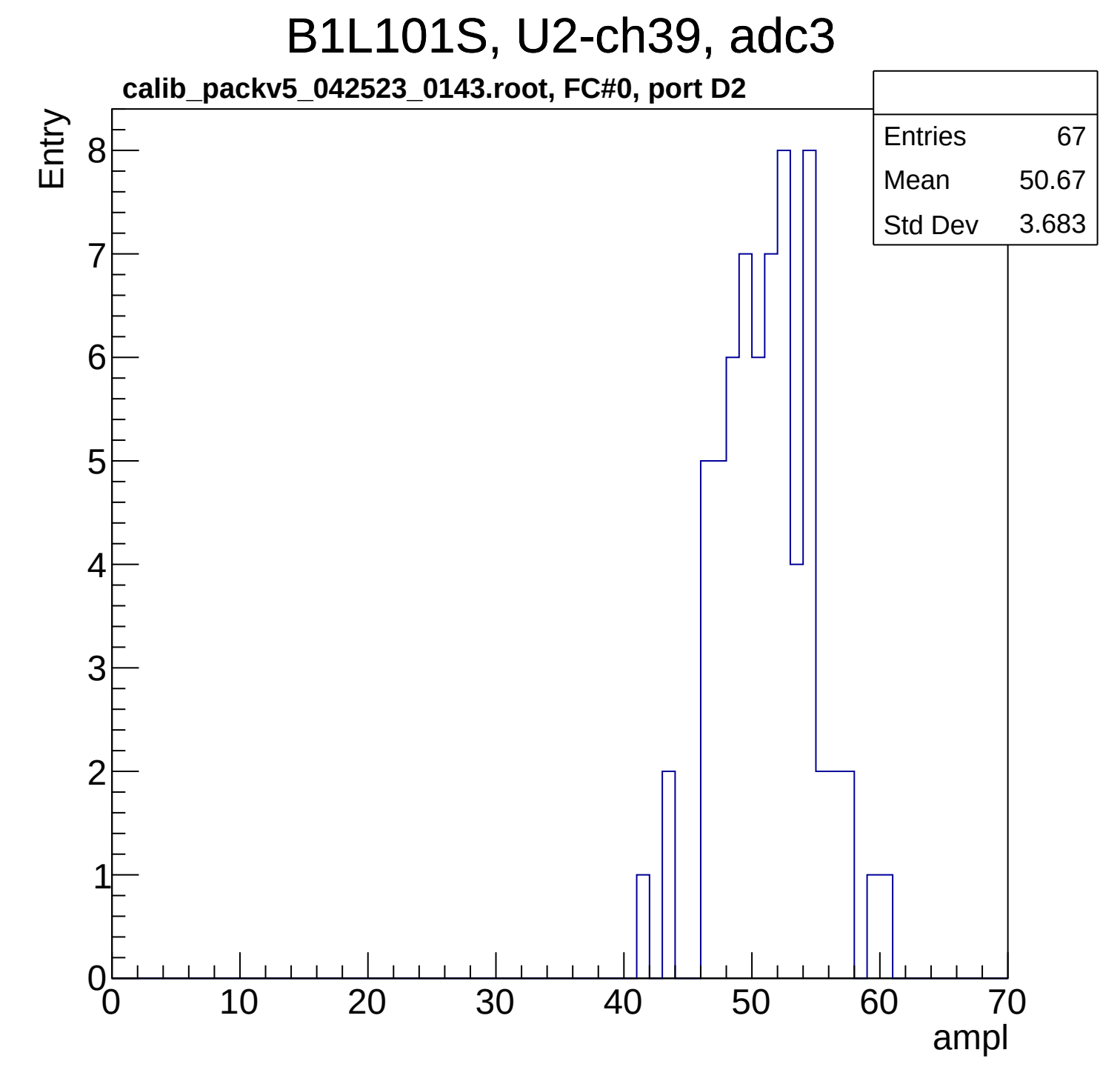

B1L101S, U2-ch38, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 13
Mean 61.62
Std Dev 1.003
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

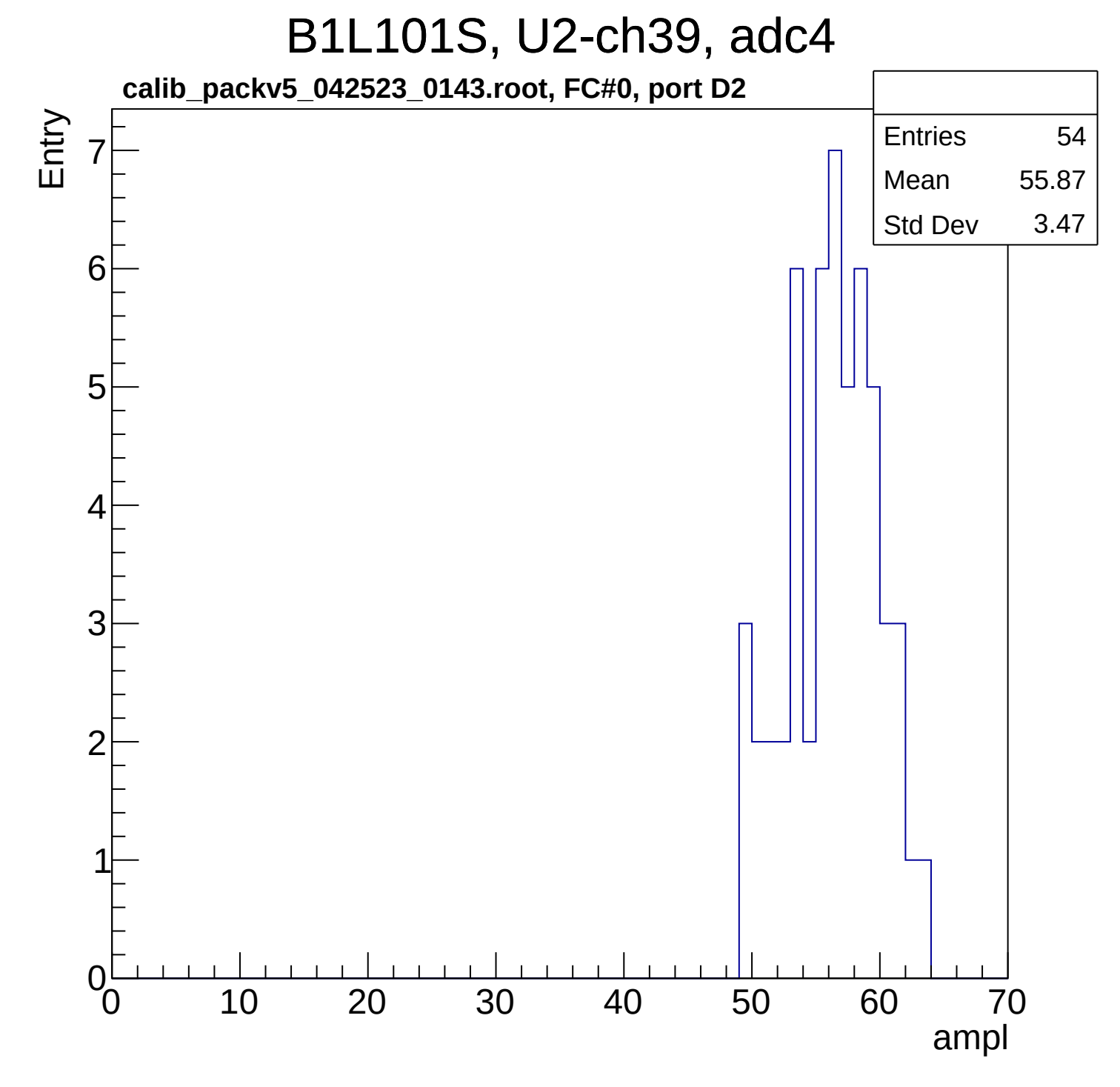

B1L101S, U2-ch38, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

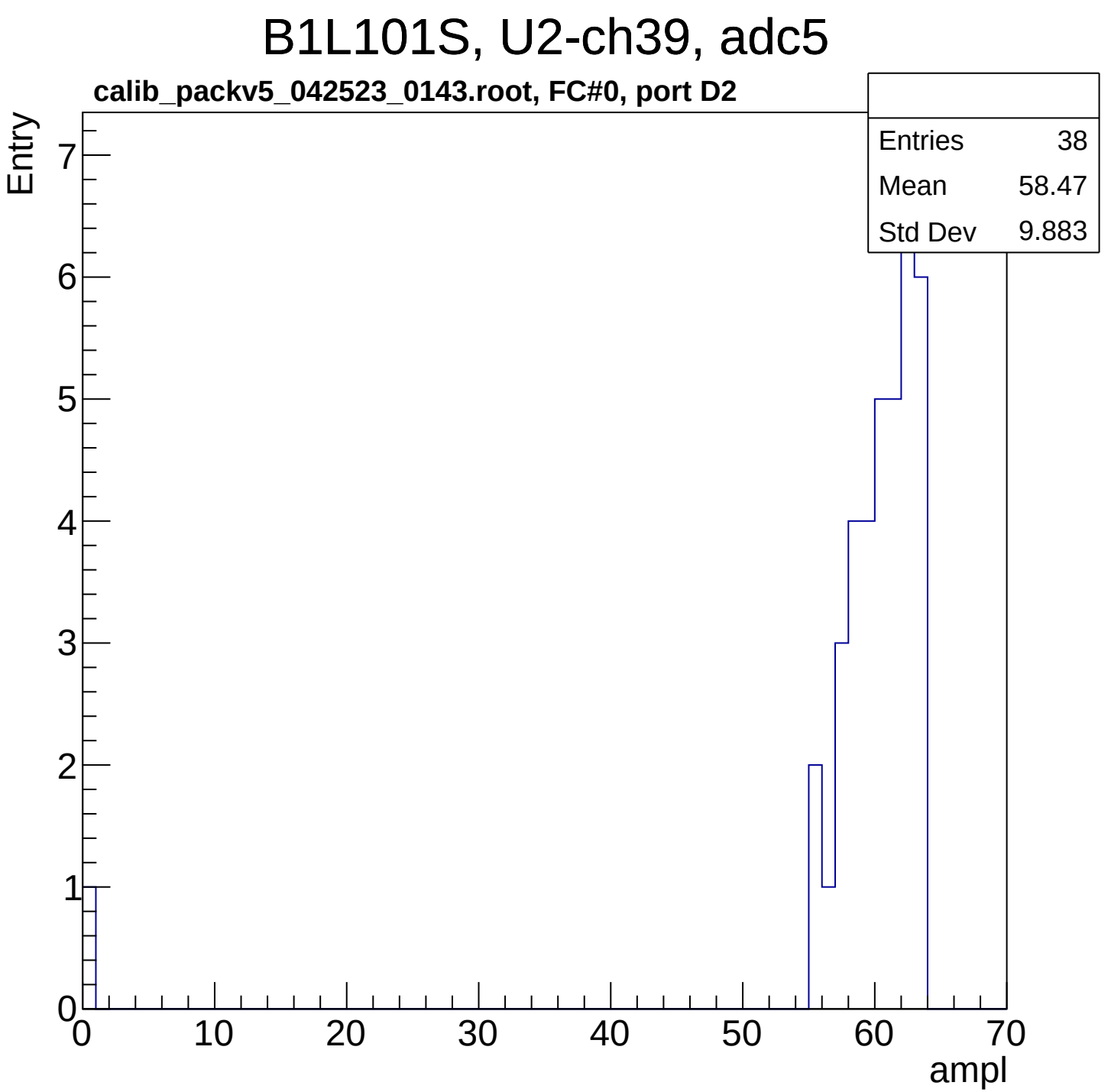

B1L101S, U2-ch39, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 83
Mean 29.93
Std Dev 4.974
Gaus mean : 31.1809
Gaus Width: 3.5105
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

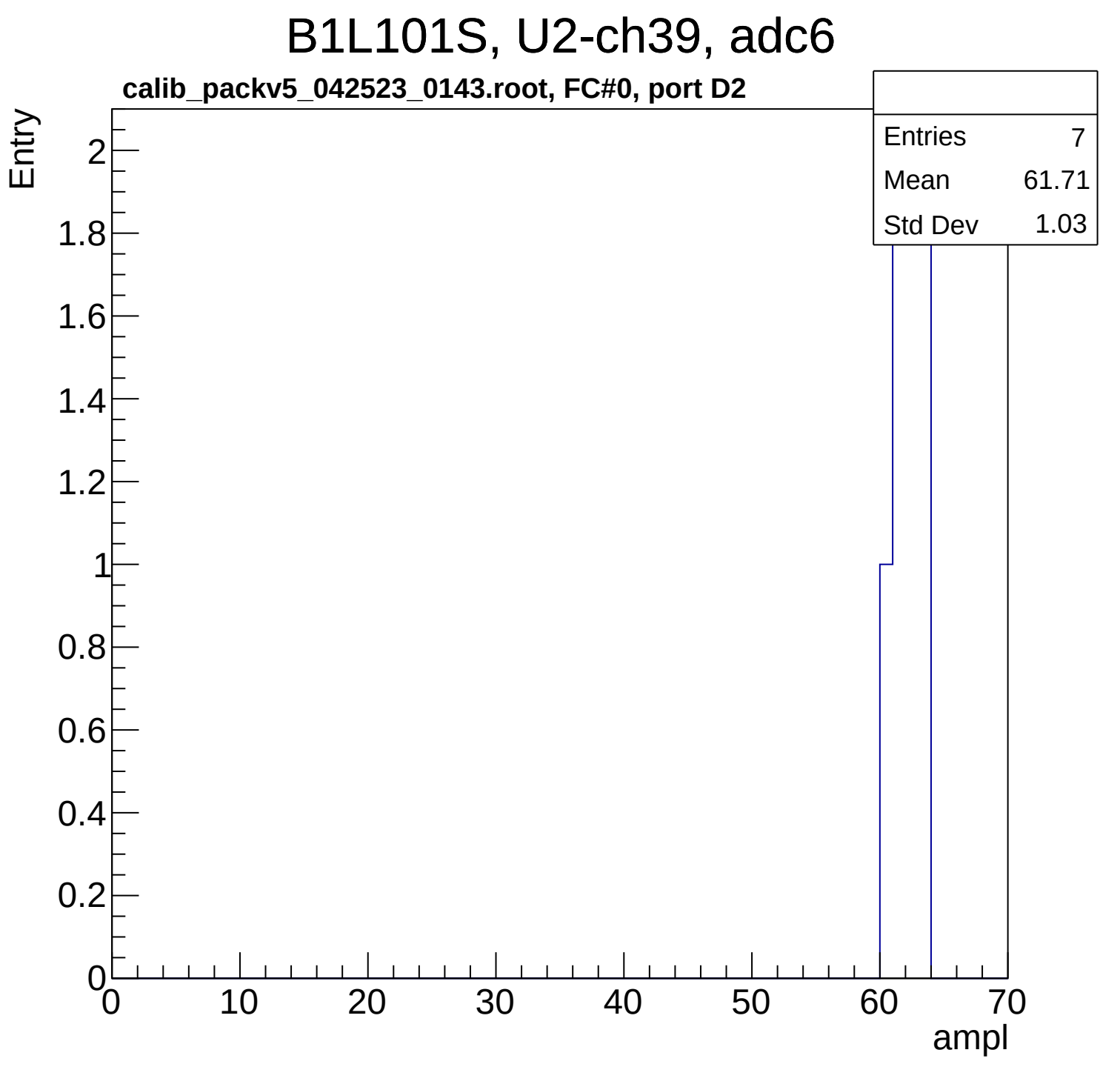

B1L101S, U2-ch39, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 37.2
Std Dev 5.497
Gaus mean : 38.1844
Gaus Width: 3.2053
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

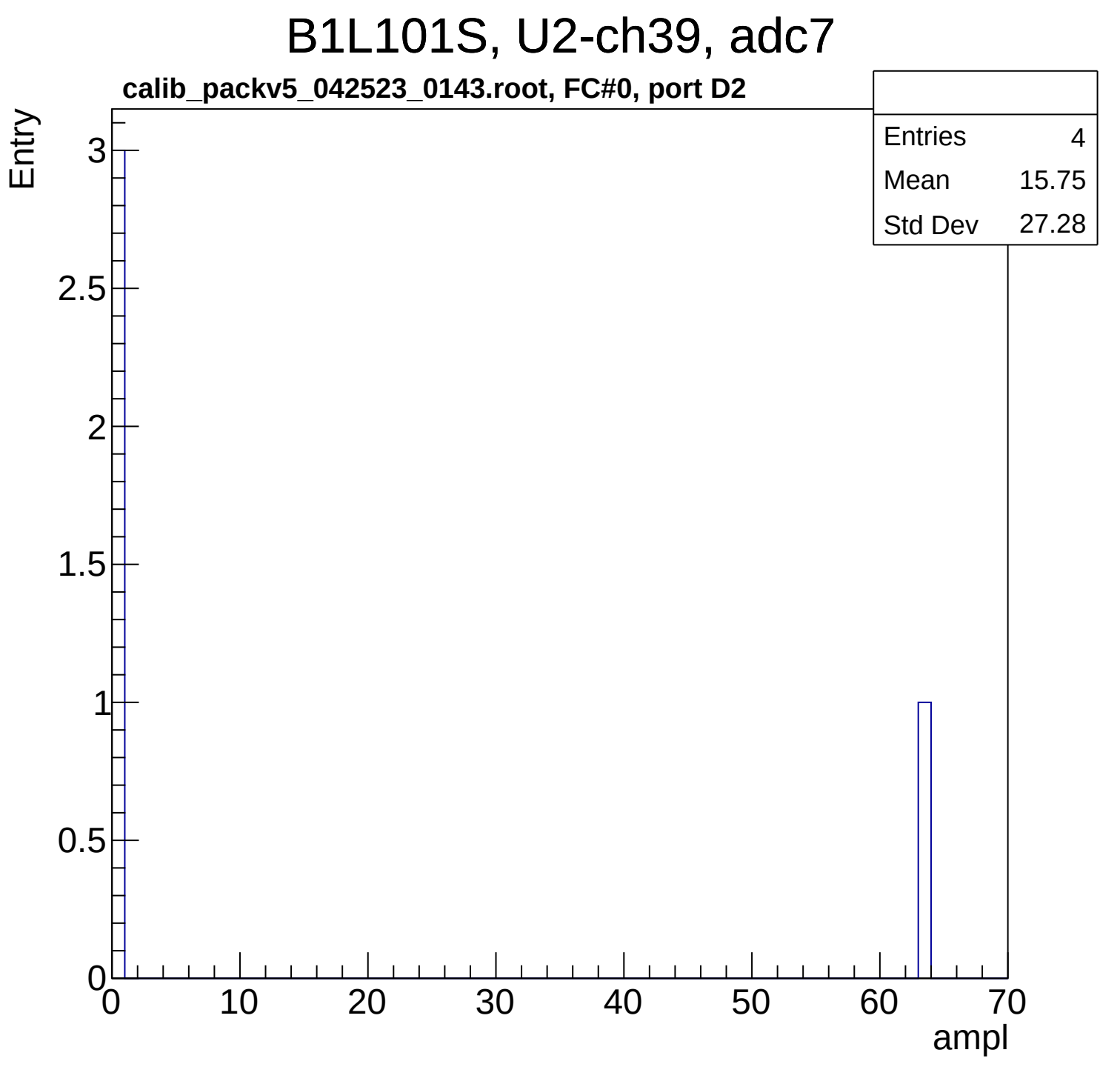

B1L101S, U2-ch39, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 44.07
Std Dev 3.144
Gaus mean : 45.2404
Gaus Width: 3.0842
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

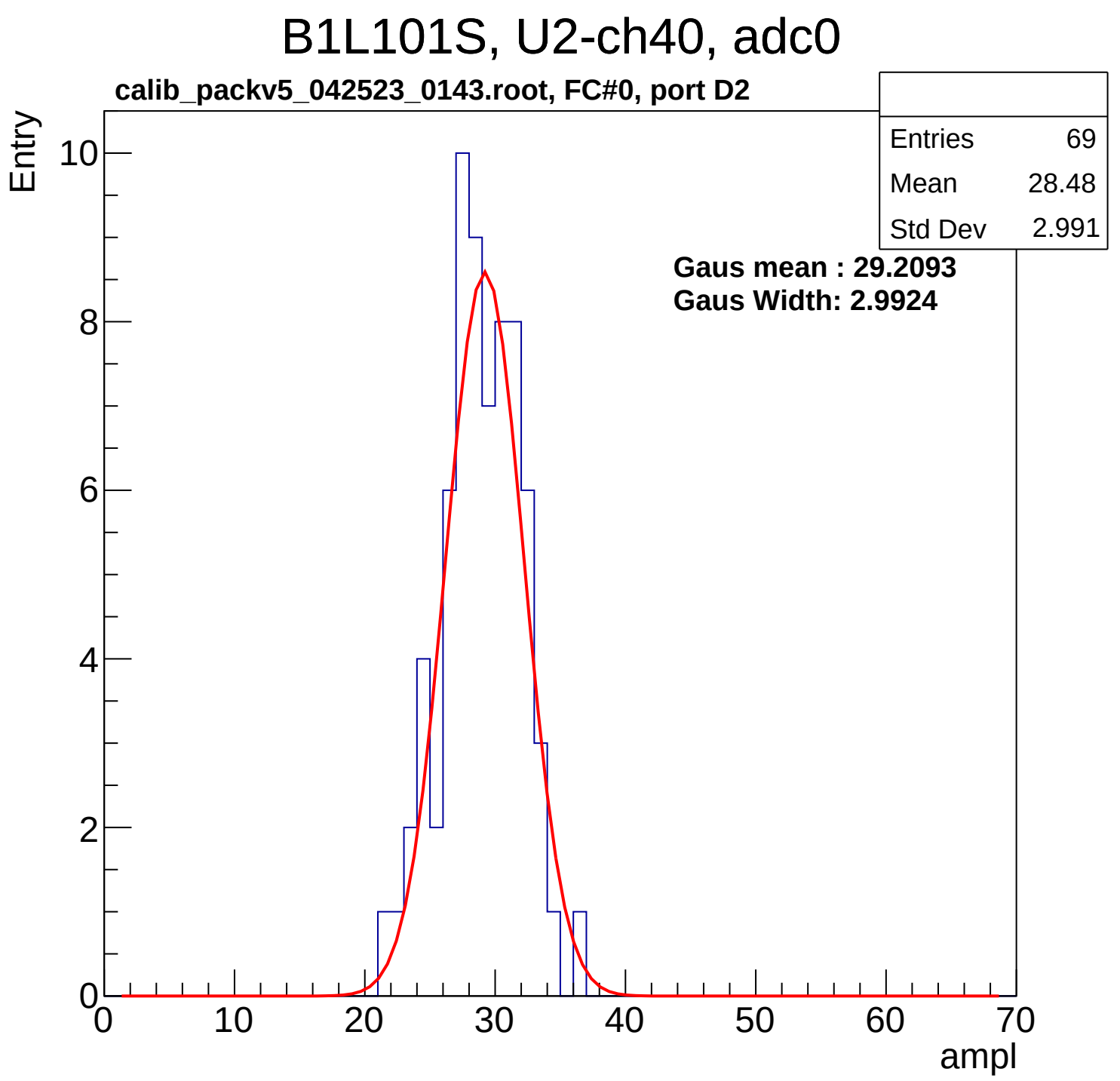

B1L101S, U2-ch39, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 50.67
Std Dev 3.683
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

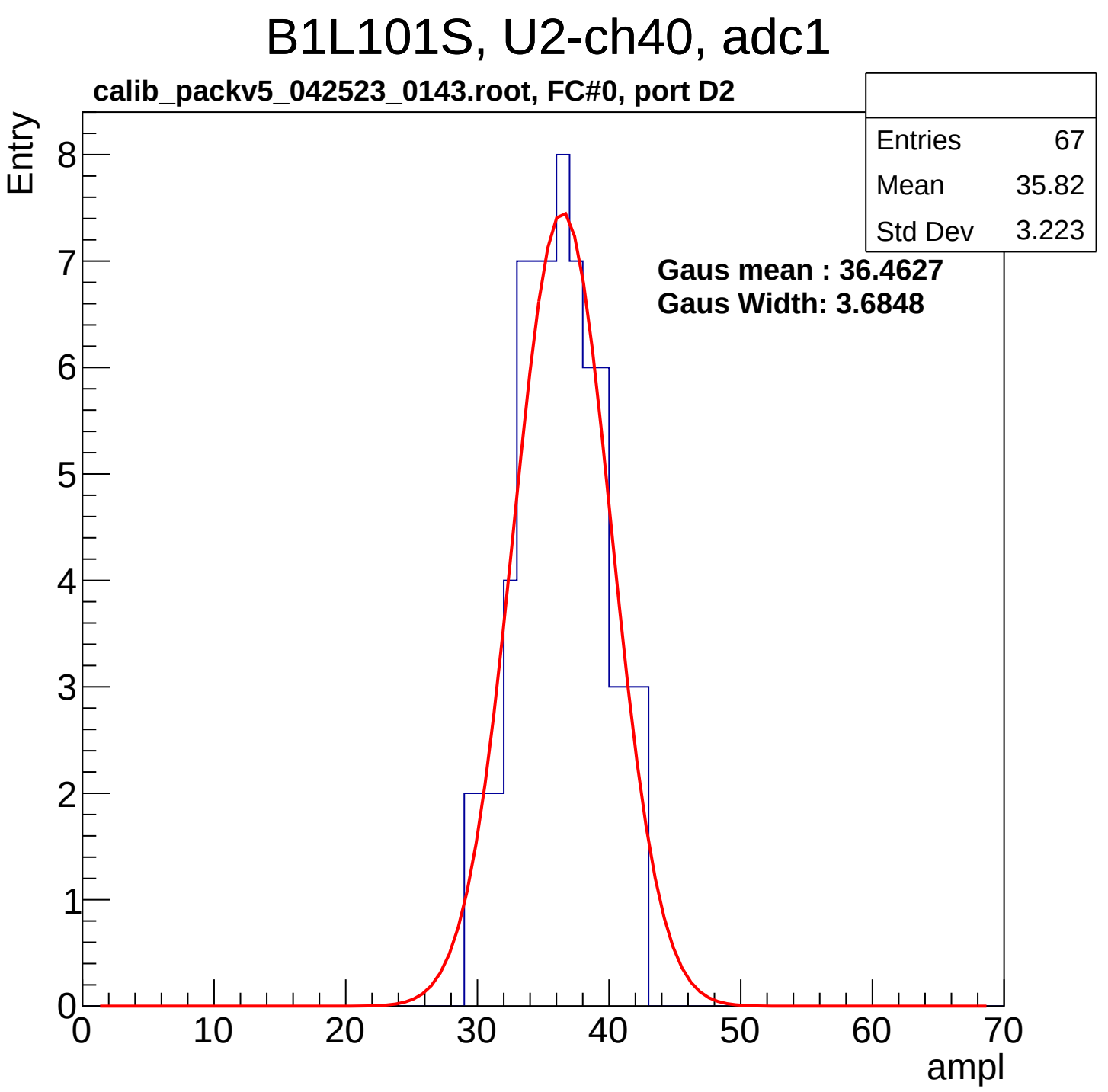

B1L101S, U2-ch39, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 55.87
Std Dev 3.47
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

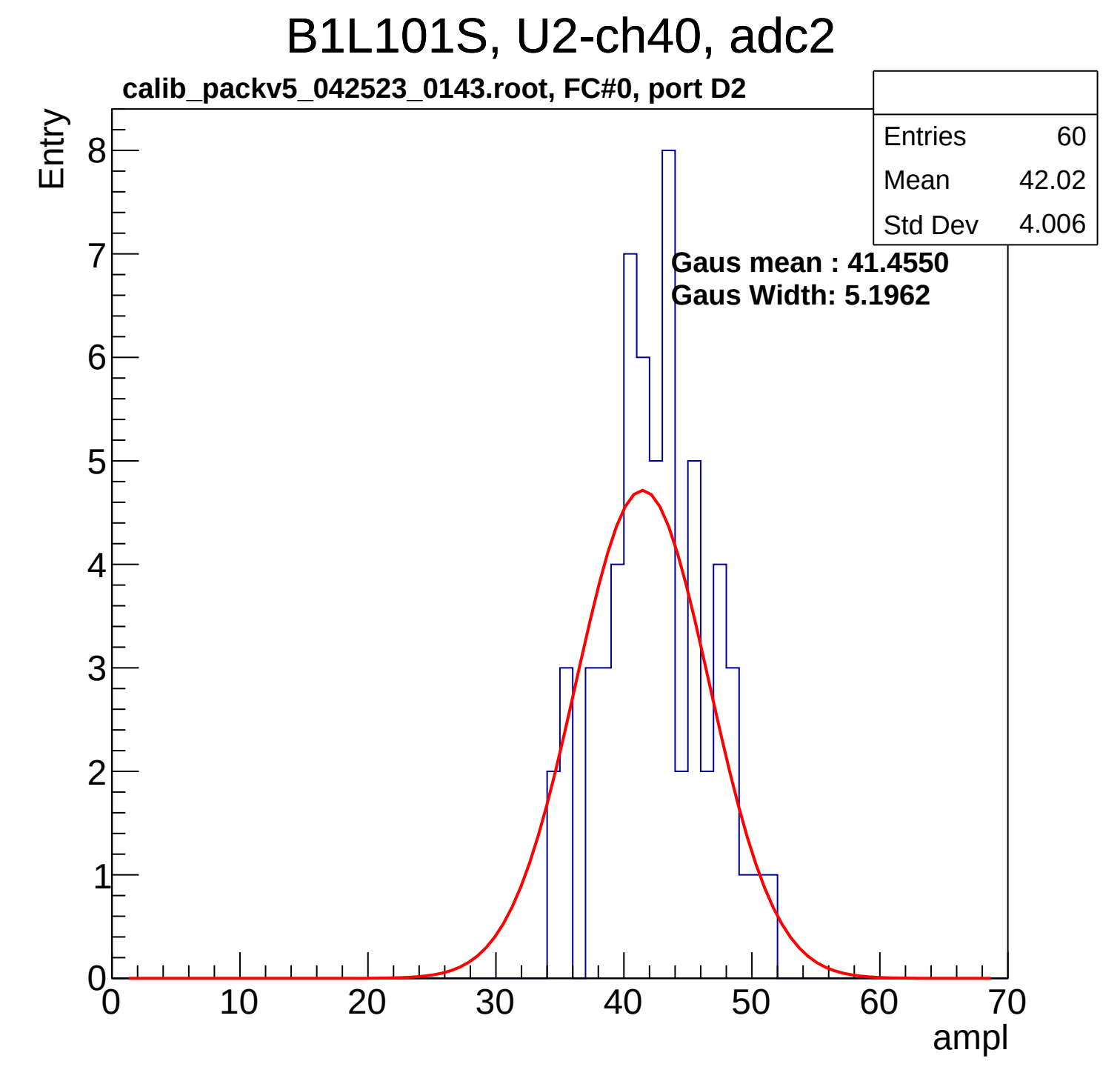

B1L101S, U2-ch39, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 38
Mean 58.47
Std Dev 9.883
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

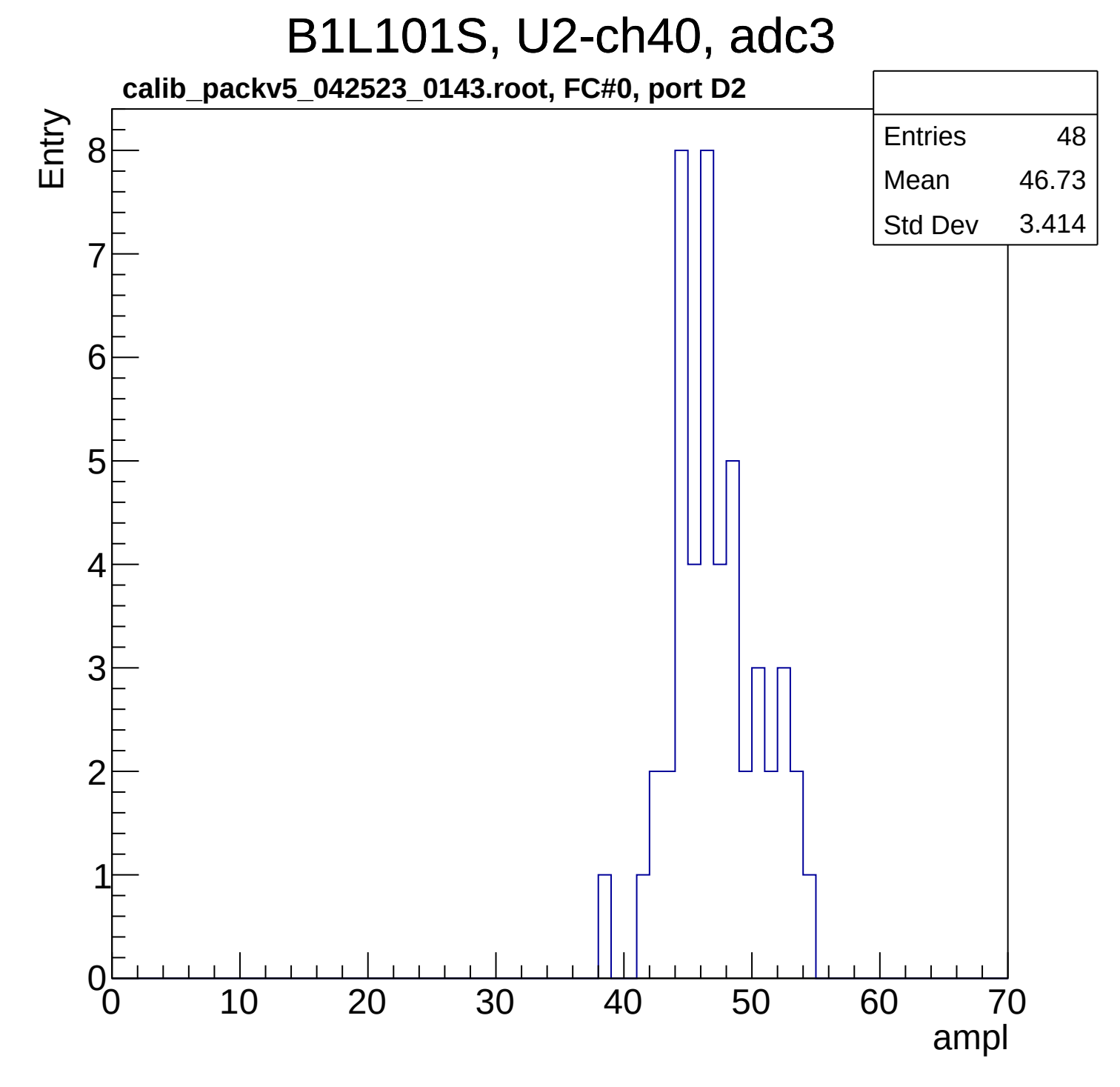

B1L101S, U2-ch39, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 61.71
Std Dev 1.03
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

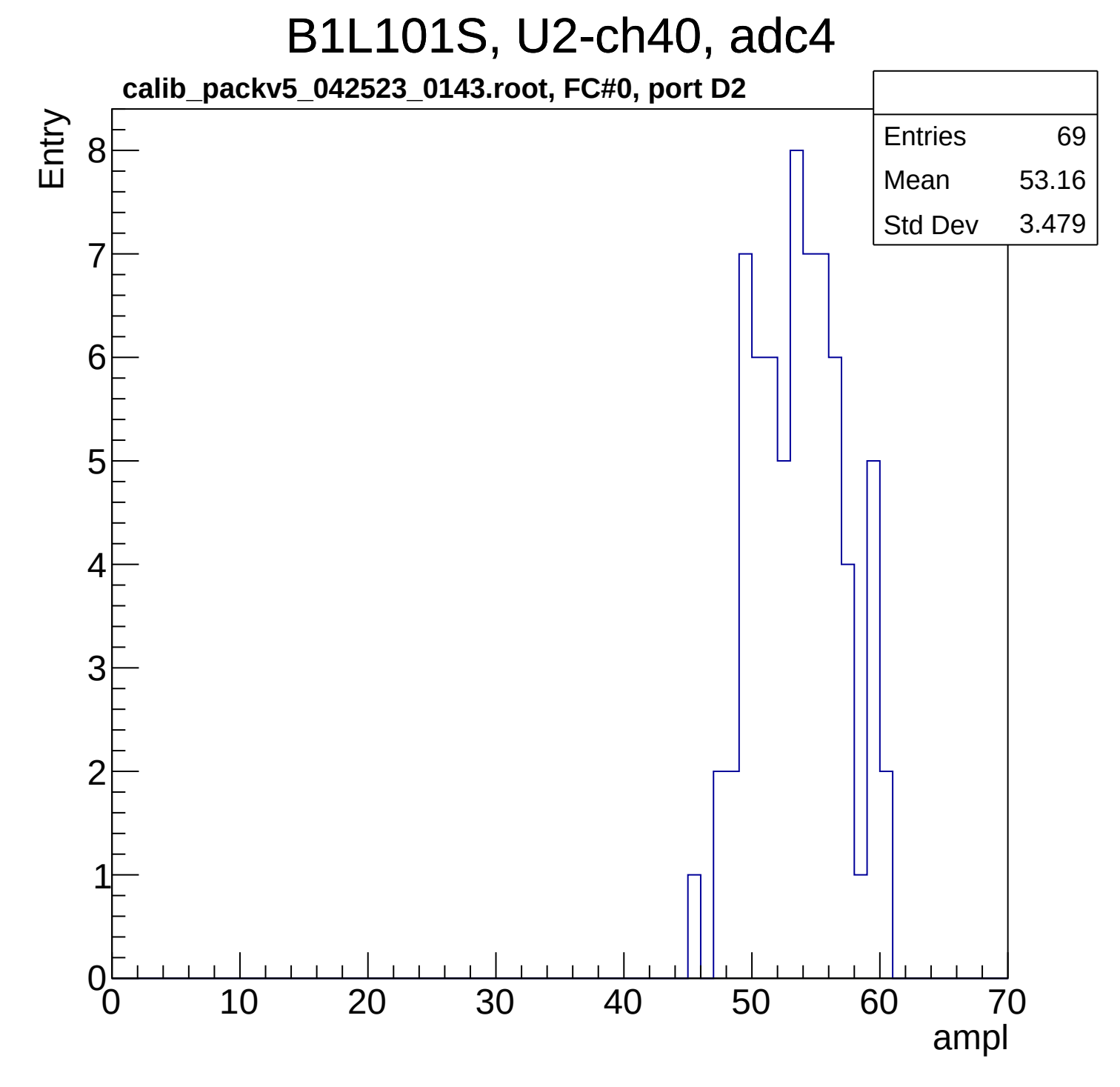

B1L101S, U2-ch39, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 15.75
Std Dev 27.28
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

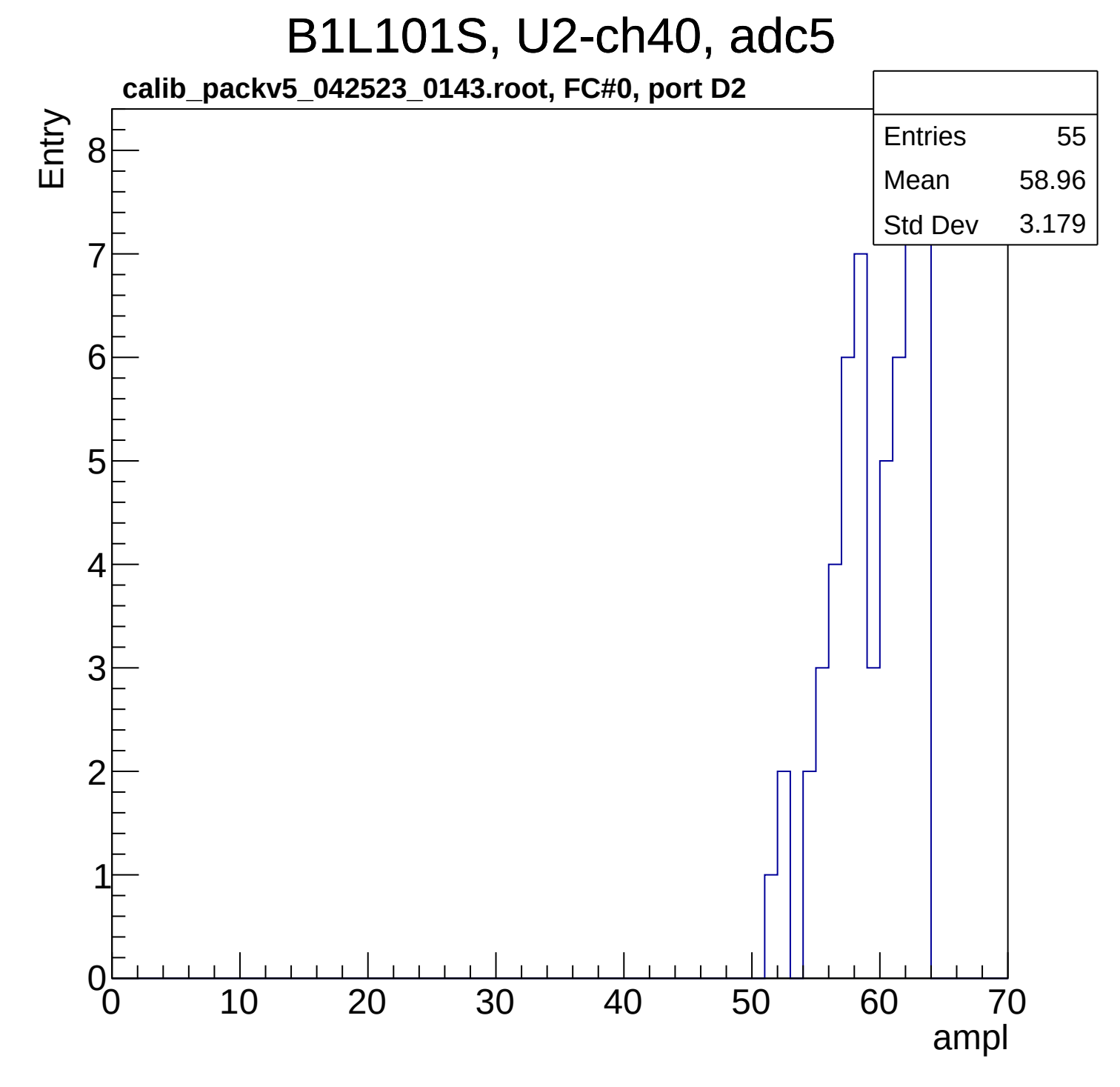

B1L101S, U2-ch40, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 28.48
Std Dev 2.991
Gaus mean : 29.2093
Gaus Width: 2.9924
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

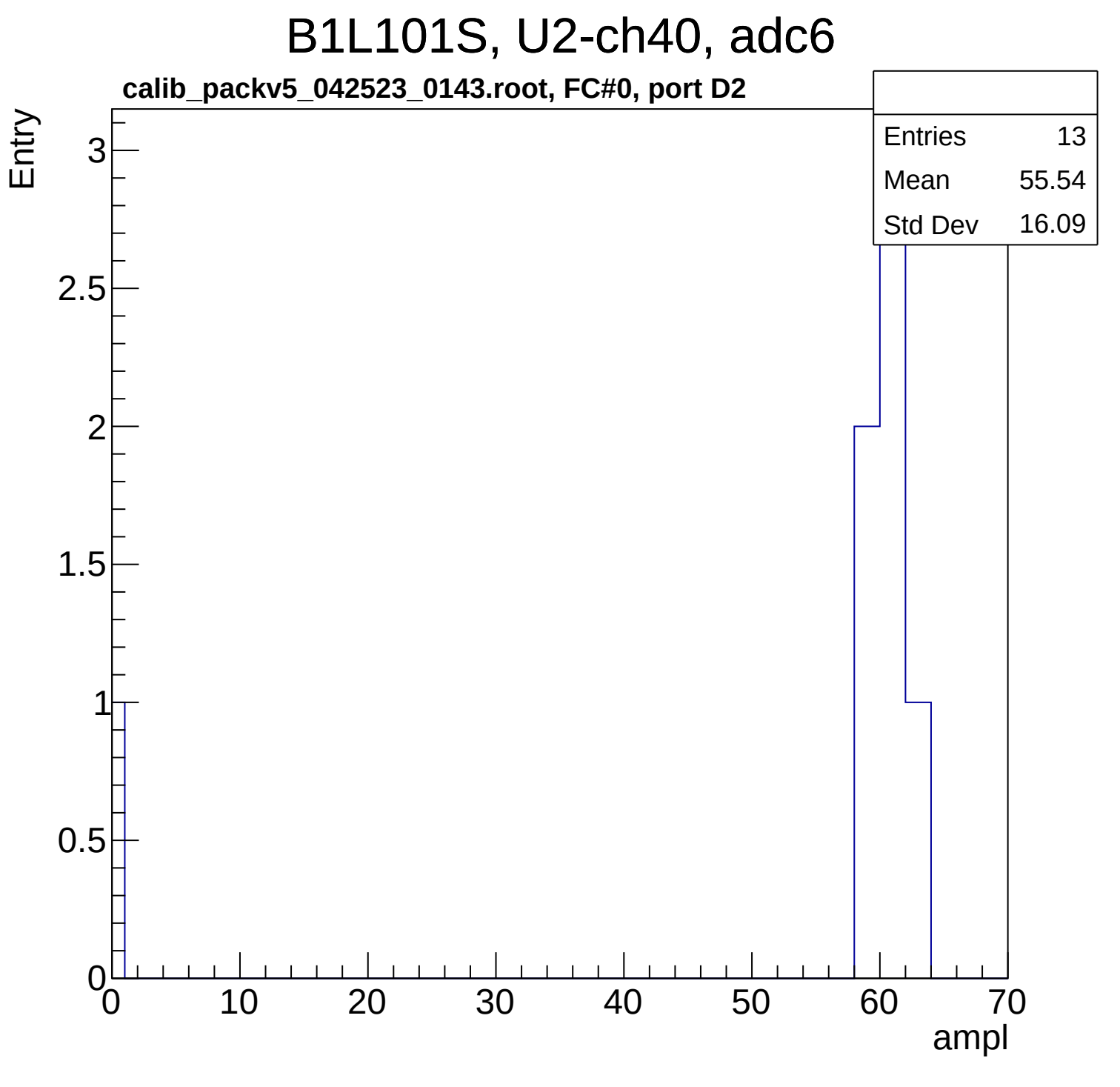

B1L101S, U2-ch40, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 35.82
Std Dev 3.223
Gaus mean : 36.4627
Gaus Width: 3.6848
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

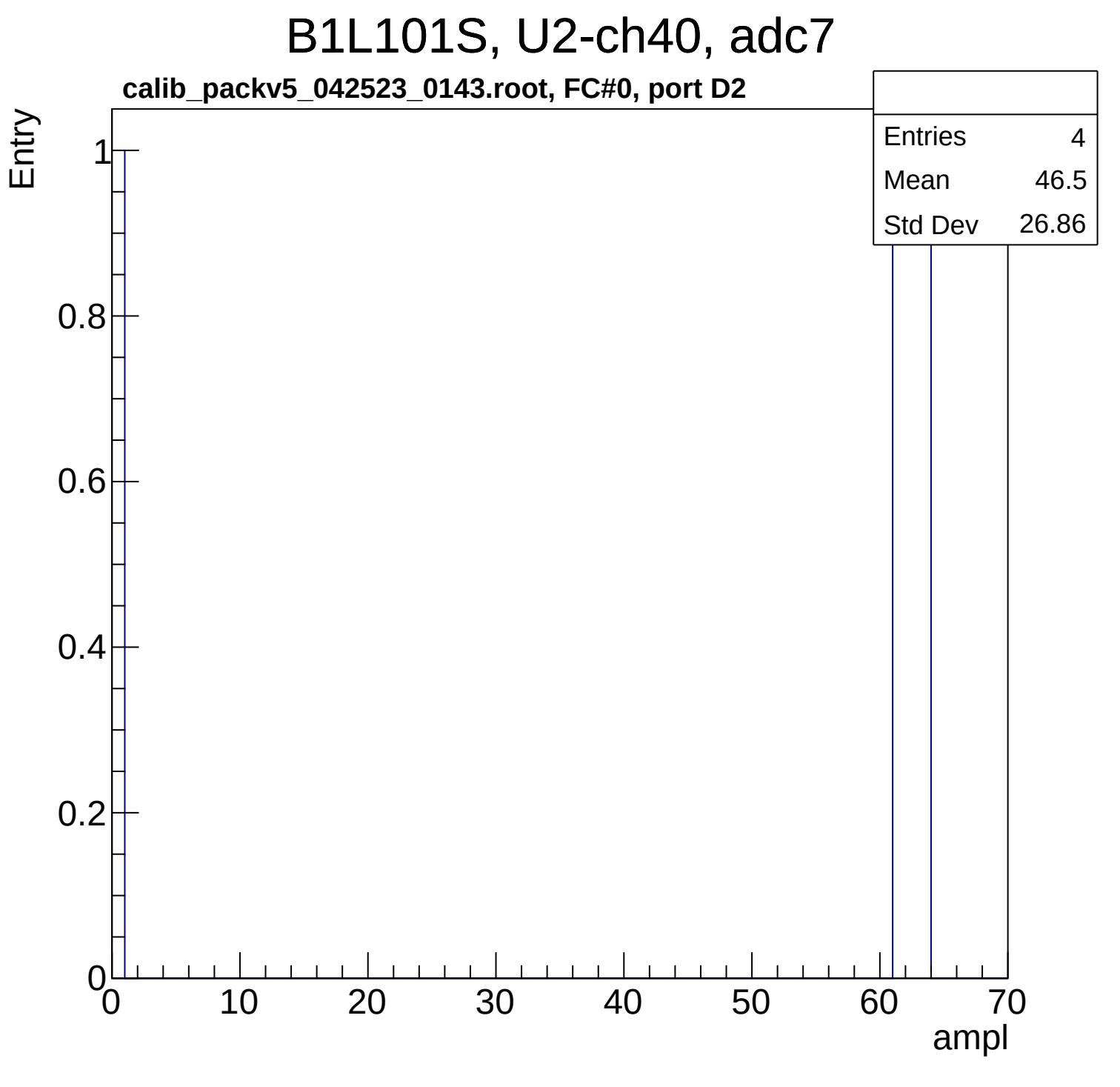

B1L101S, U2-ch40, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 42.02
Std Dev 4.006
Gaus mean : 41.4550
Gaus Width: 5.1962
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

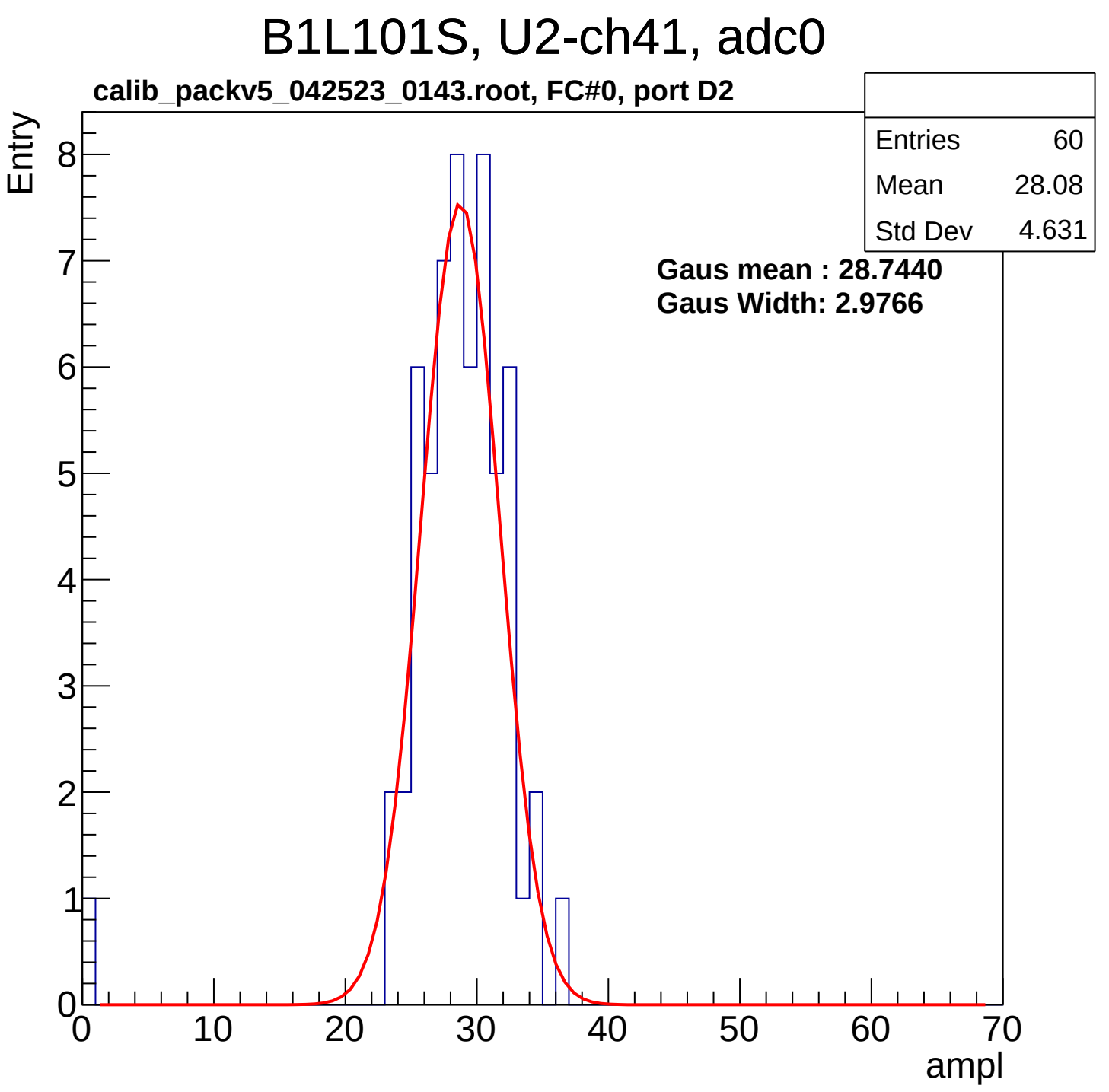

B1L101S, U2-ch40, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 46.73
Std Dev 3.414
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

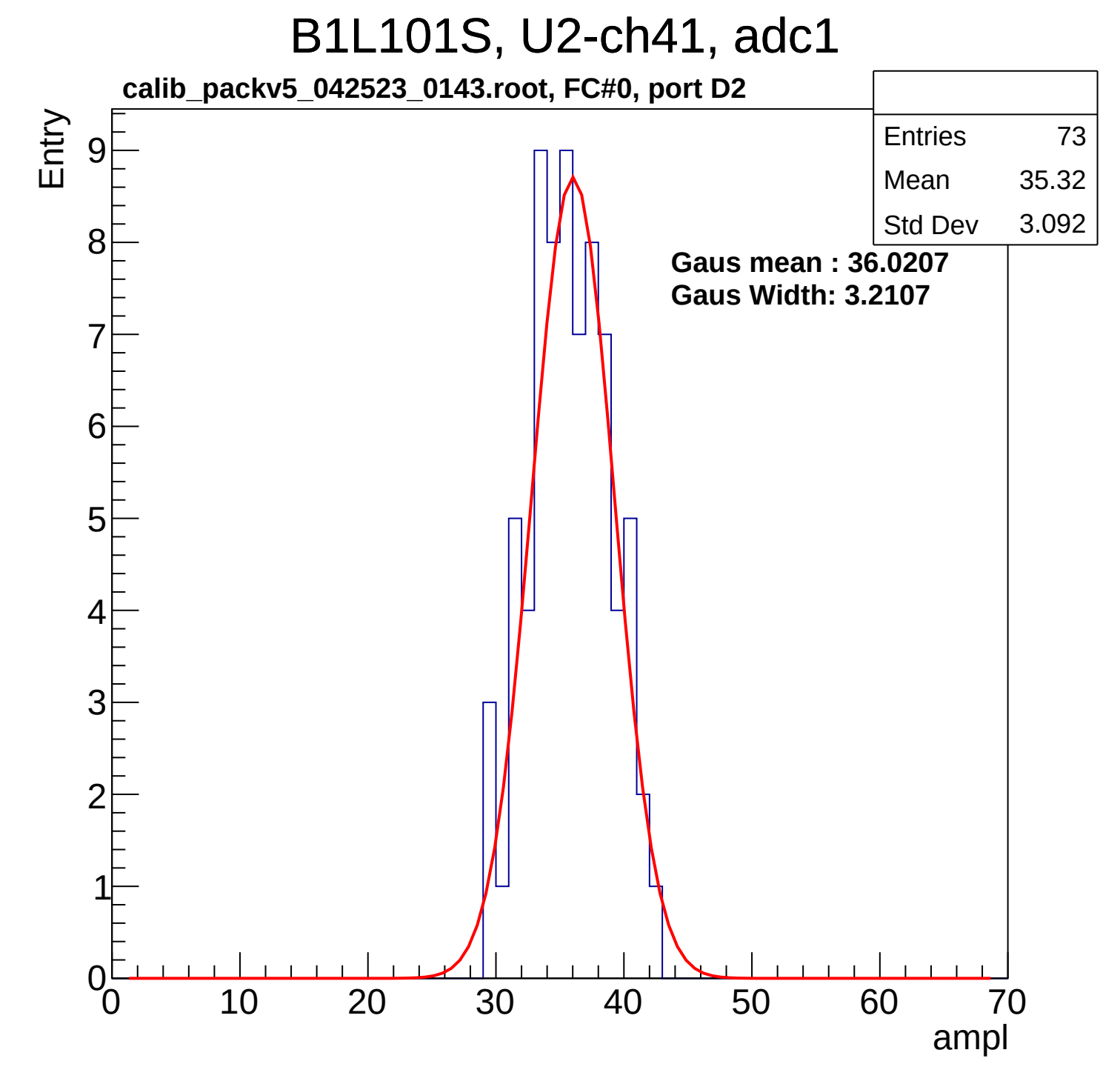

B1L101S, U2-ch40, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 53.16
Std Dev 3.479
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

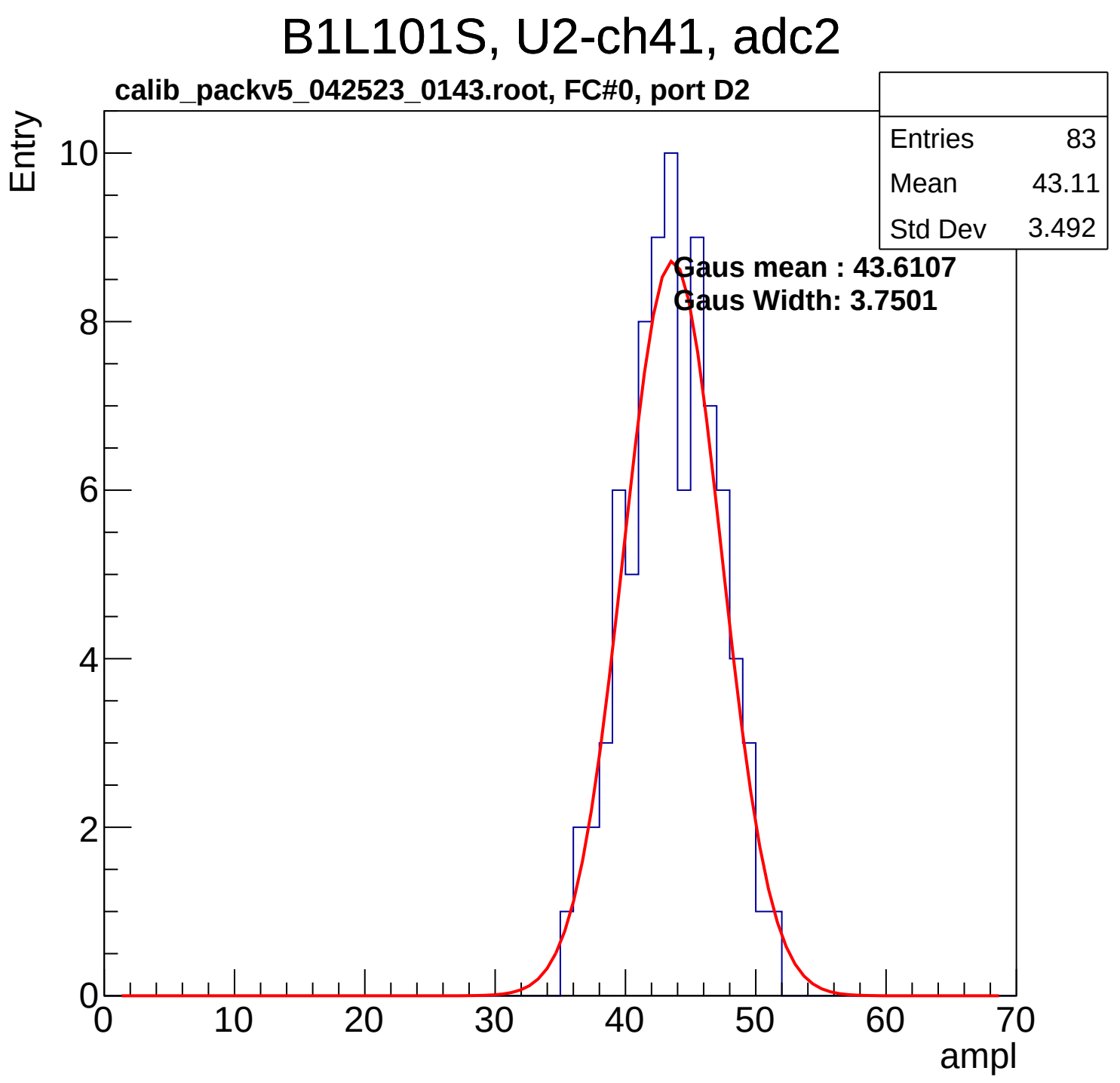

B1L101S, U2-ch40, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 58.96
Std Dev 3.179
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

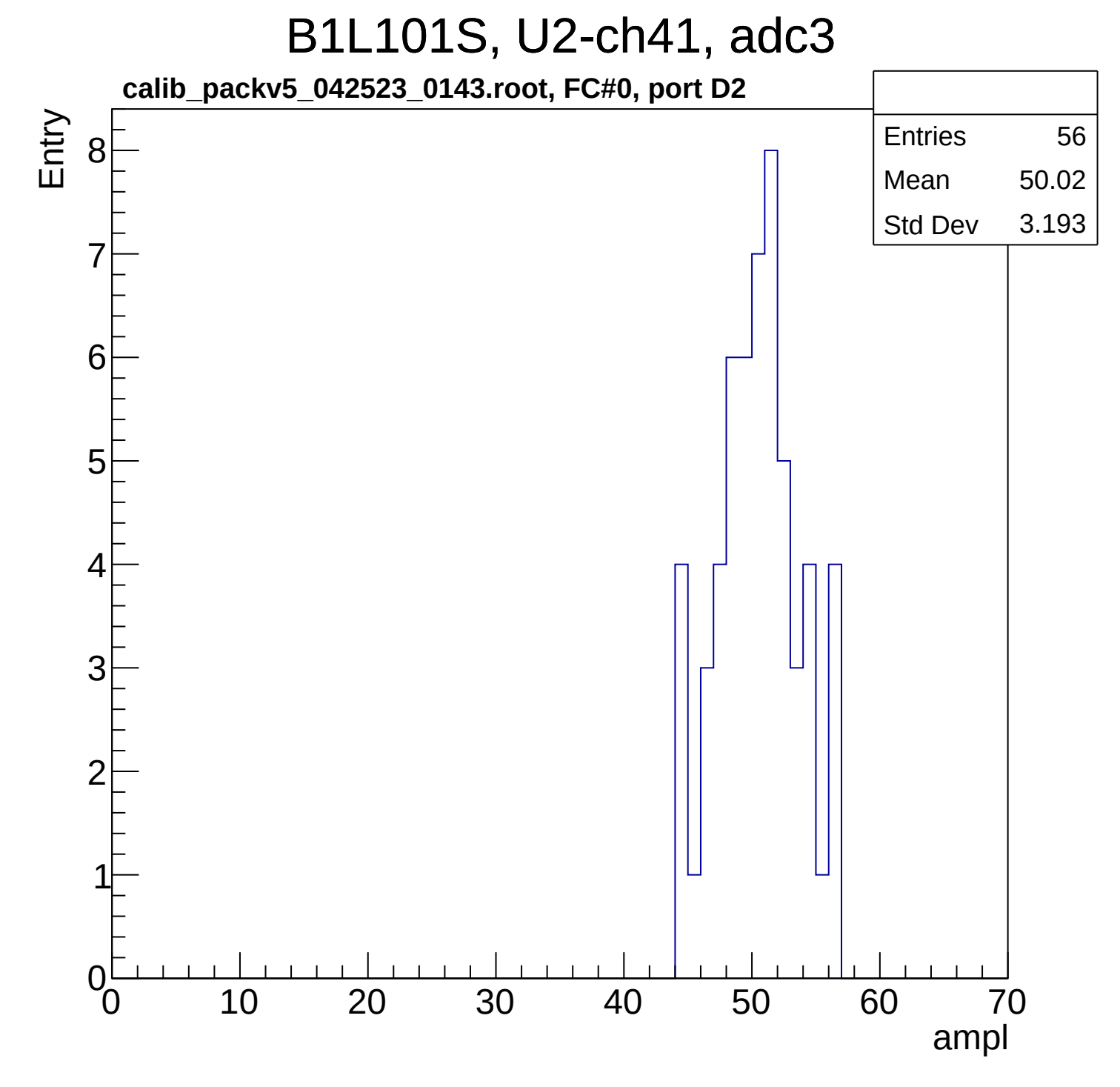

B1L101S, U2-ch40, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 13
Mean 55.54
Std Dev 16.09
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl

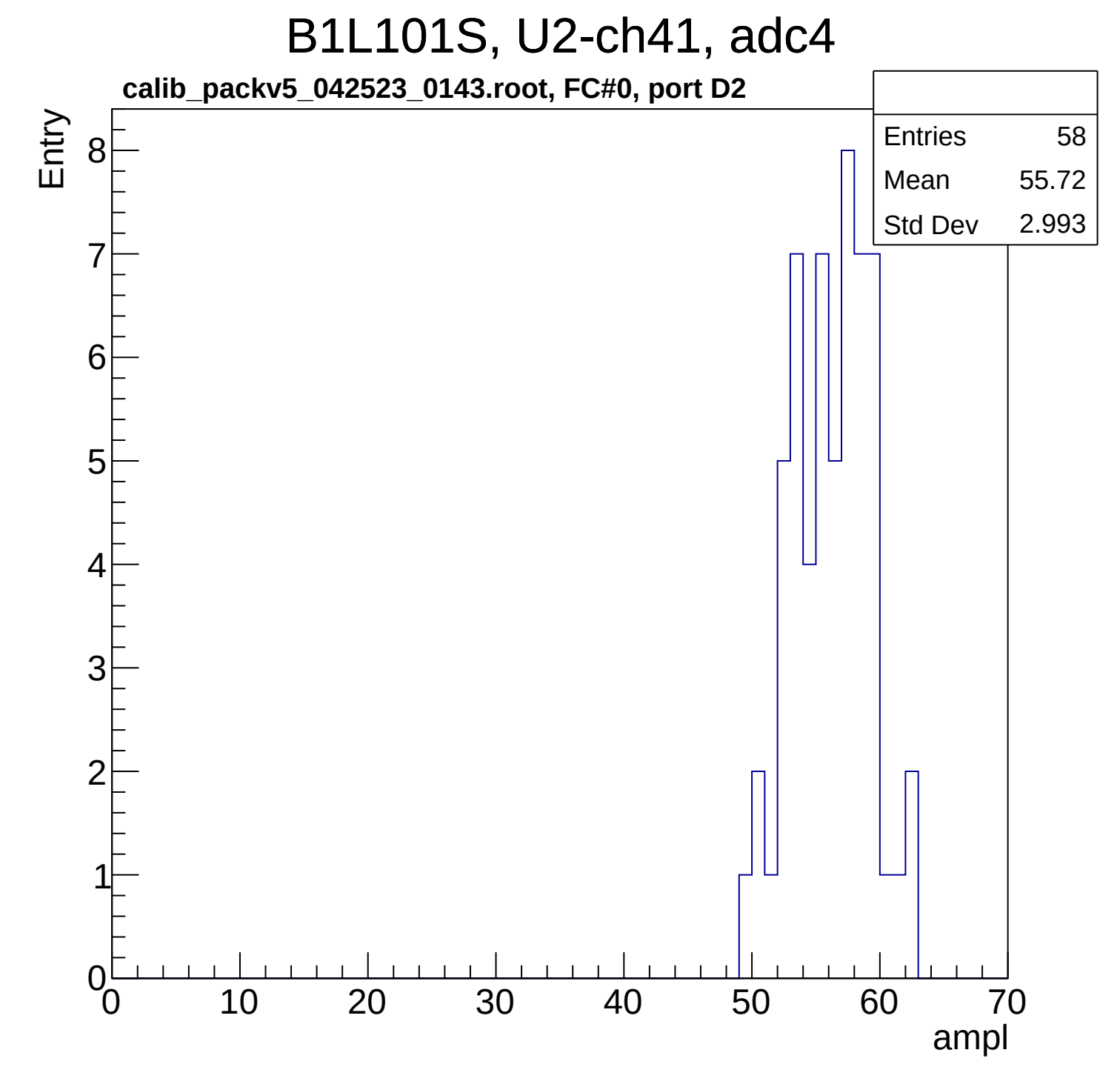

B1L101S, U2-ch40, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 46.5
Std Dev 26.86
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

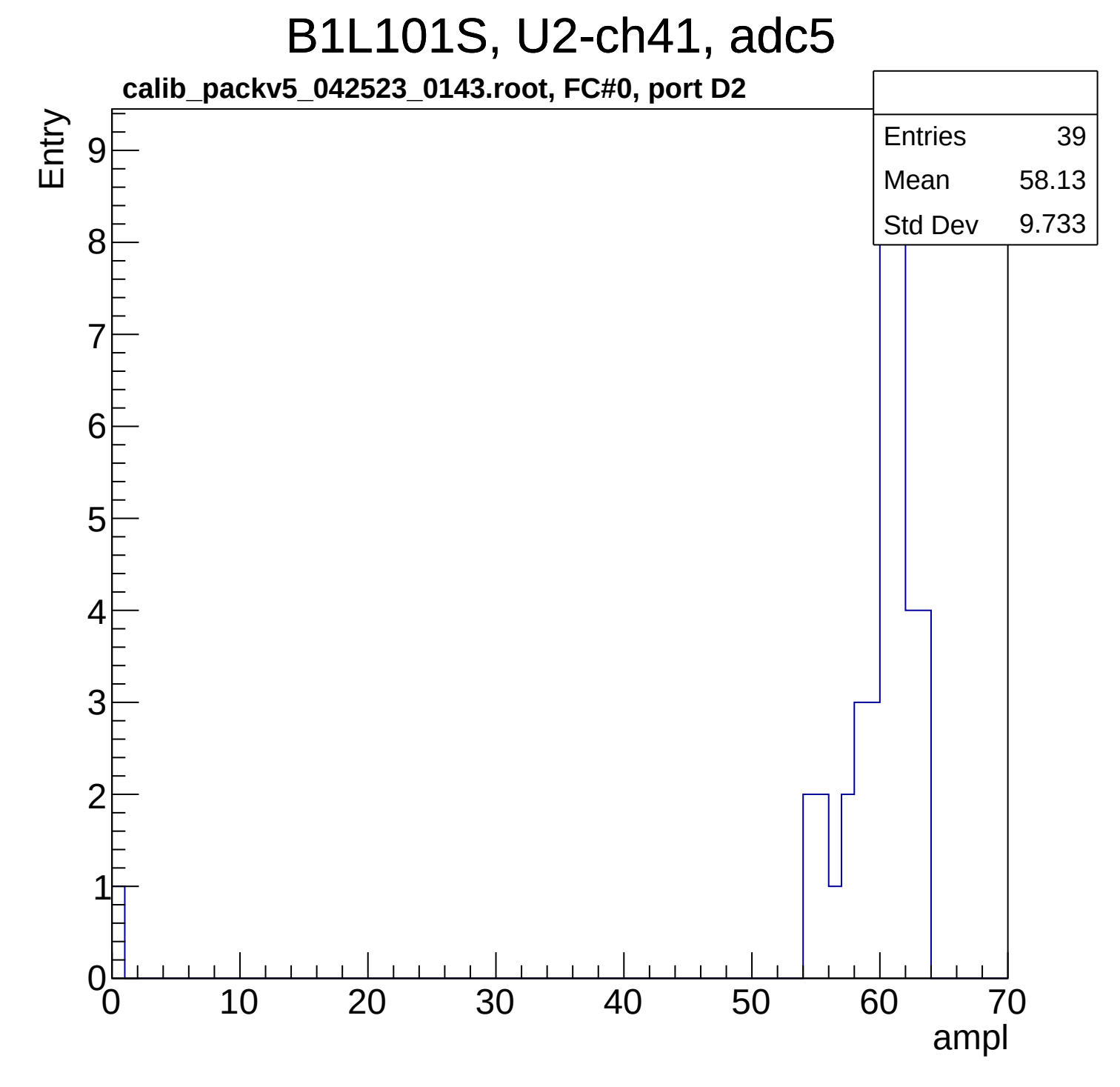

B1L101S, U2-ch41, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 28.08
Std Dev 4.631
Gaus mean : 28.7440
Gaus Width: 2.9766
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

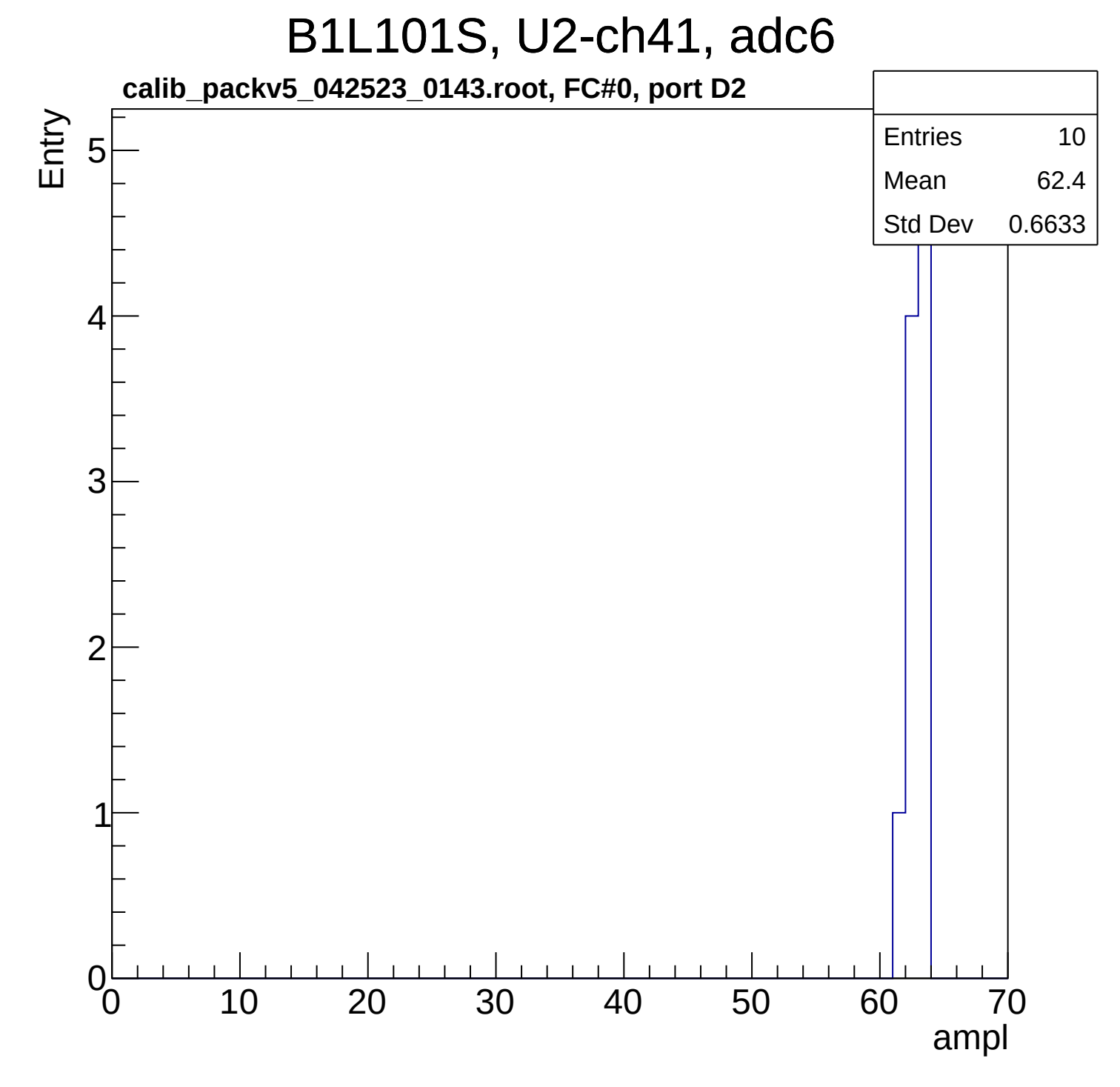

B1L101S, U2-ch41, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 35.32
Std Dev 3.092
Gaus mean : 36.0207
Gaus Width: 3.2107
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

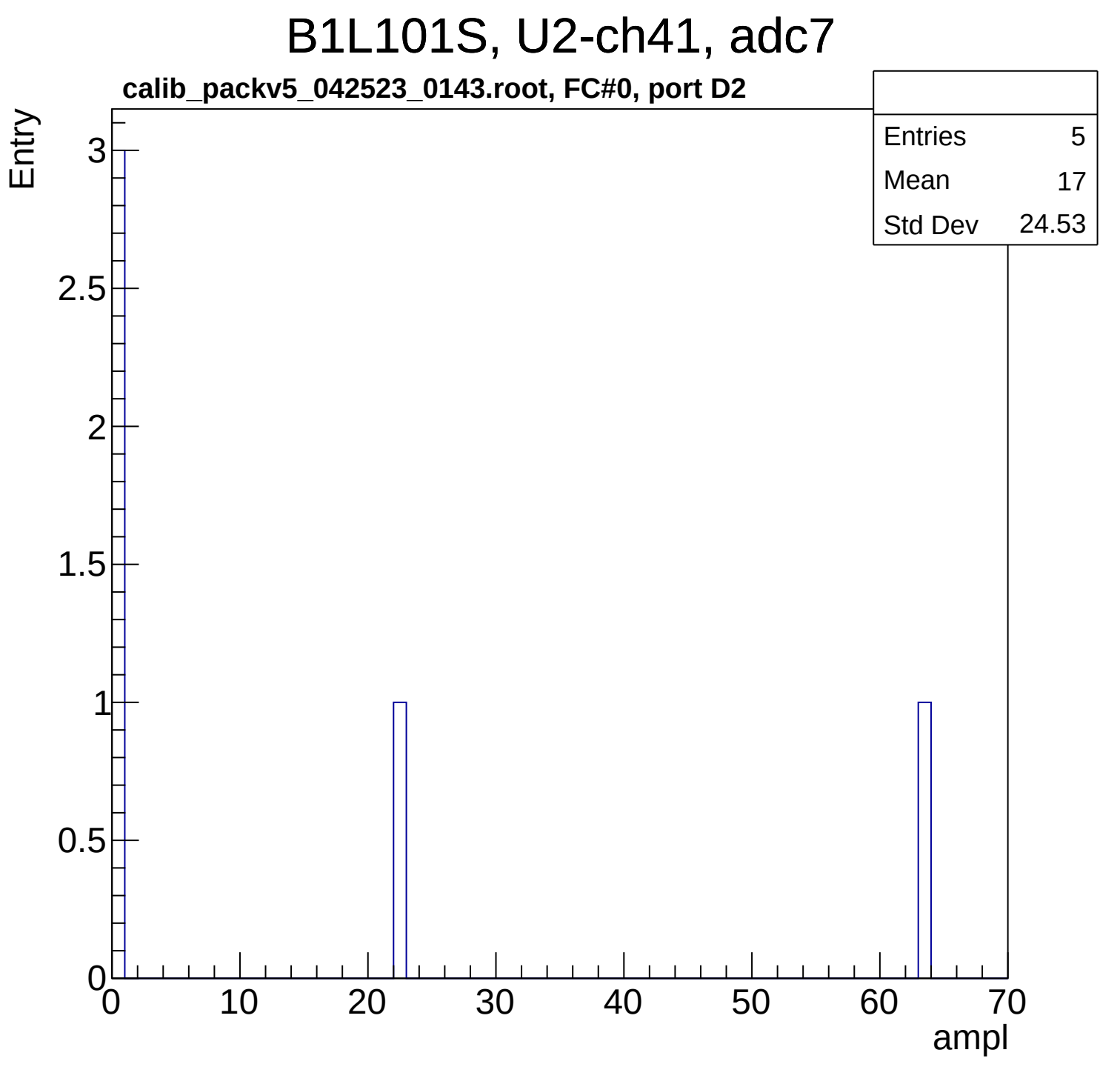

B1L101S, U2-ch41, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 83
Mean 43.11
Std Dev 3.492
Gaus mean : 43.6107
Gaus Width: 3.7501
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

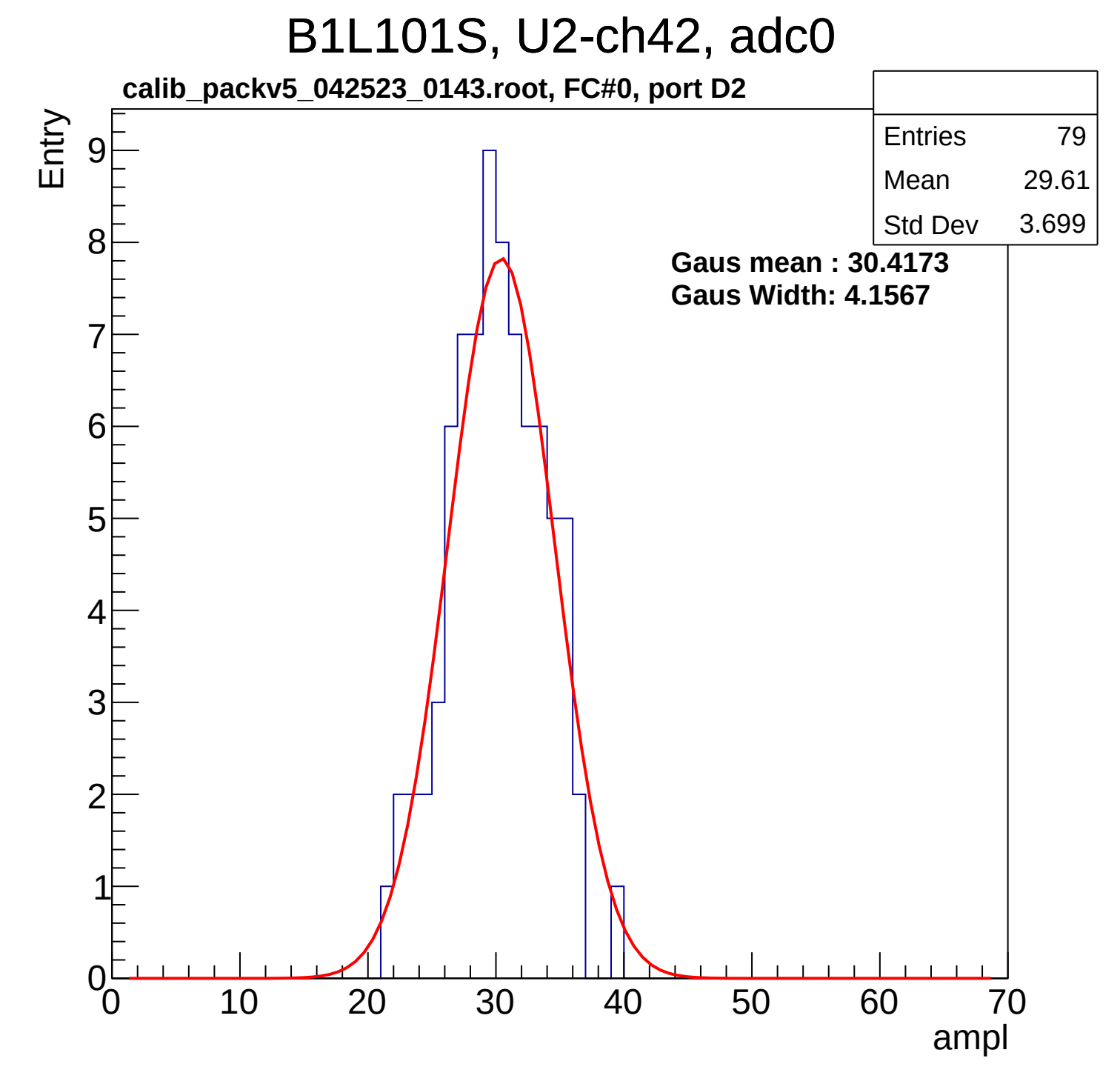

B1L101S, U2-ch41, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 50.02
Std Dev 3.193
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

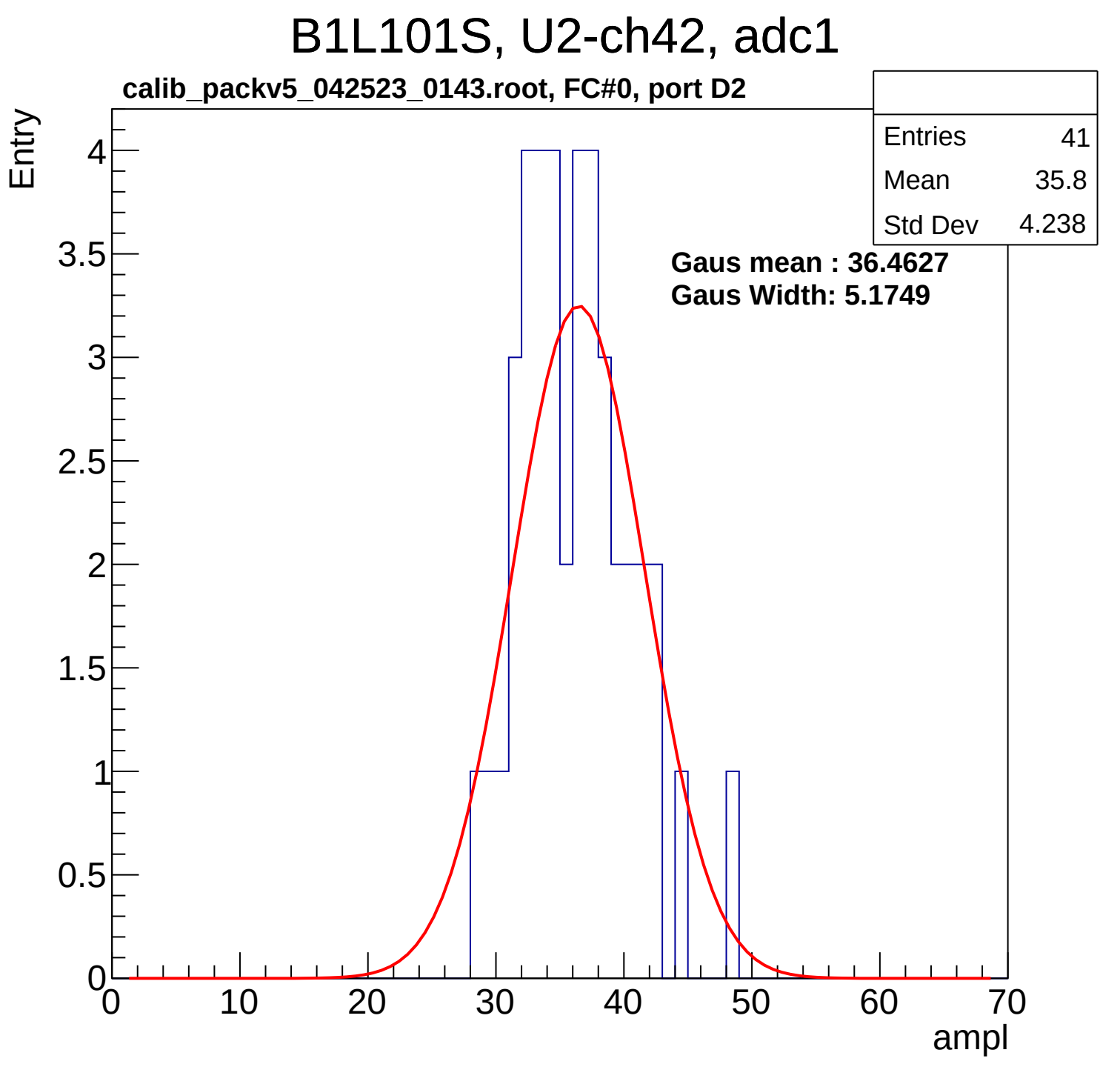

B1L101S, U2-ch41, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 55.72
Std Dev 2.993
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

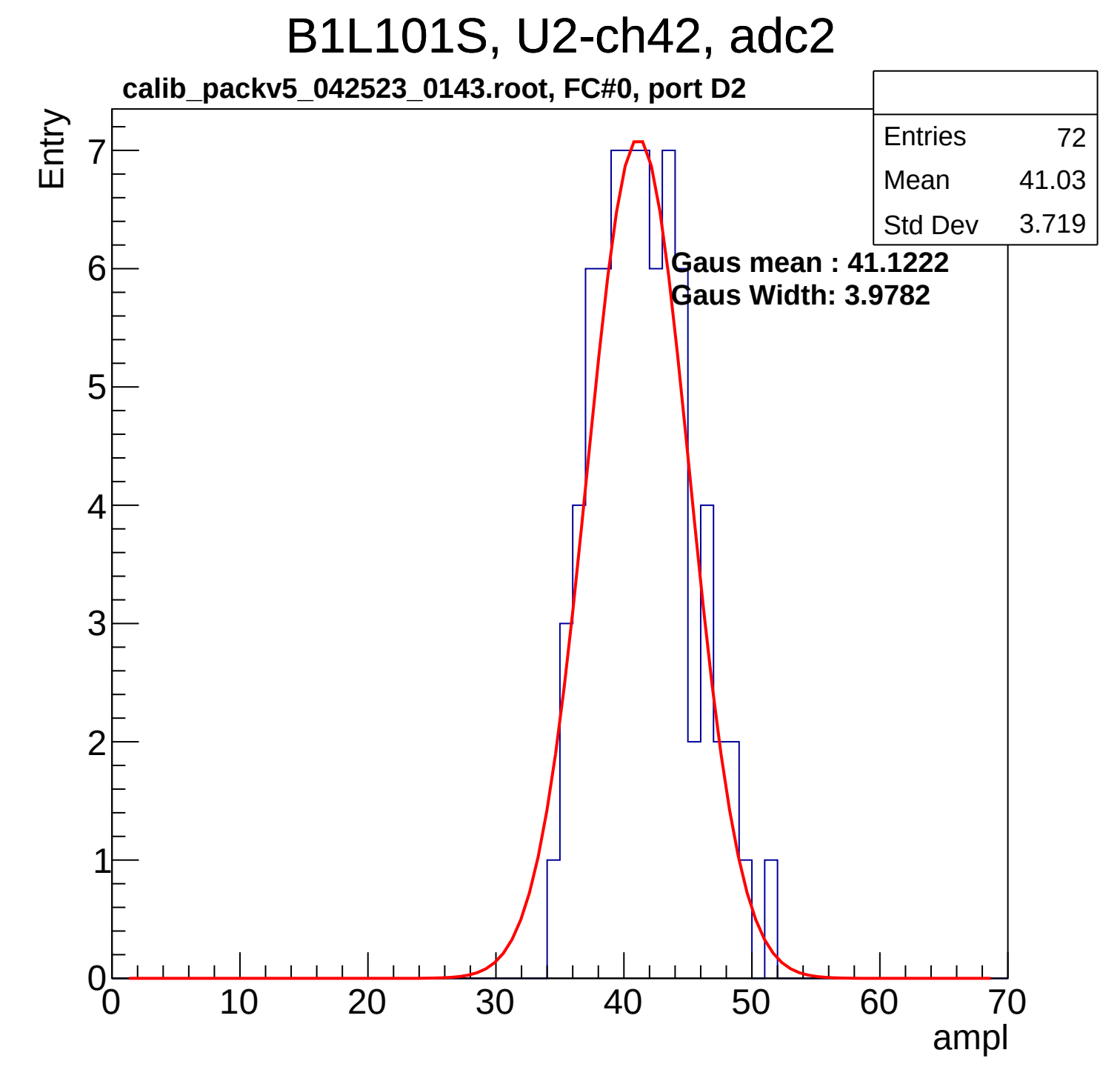

B1L101S, U2-ch41, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 39
Mean 58.13
Std Dev 9.733
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

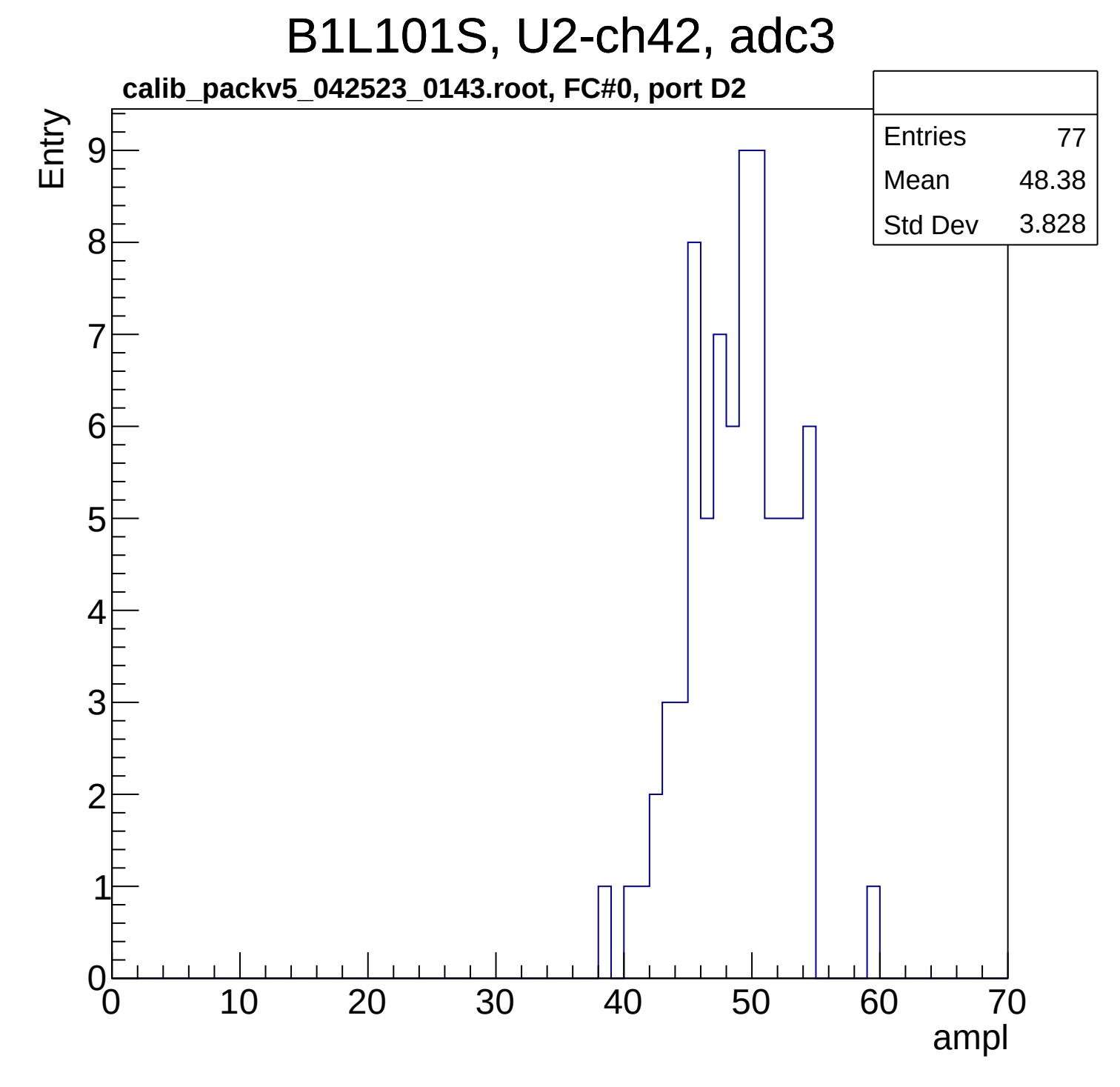

B1L101S, U2-ch41, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 62.4
Std Dev 0.6633
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

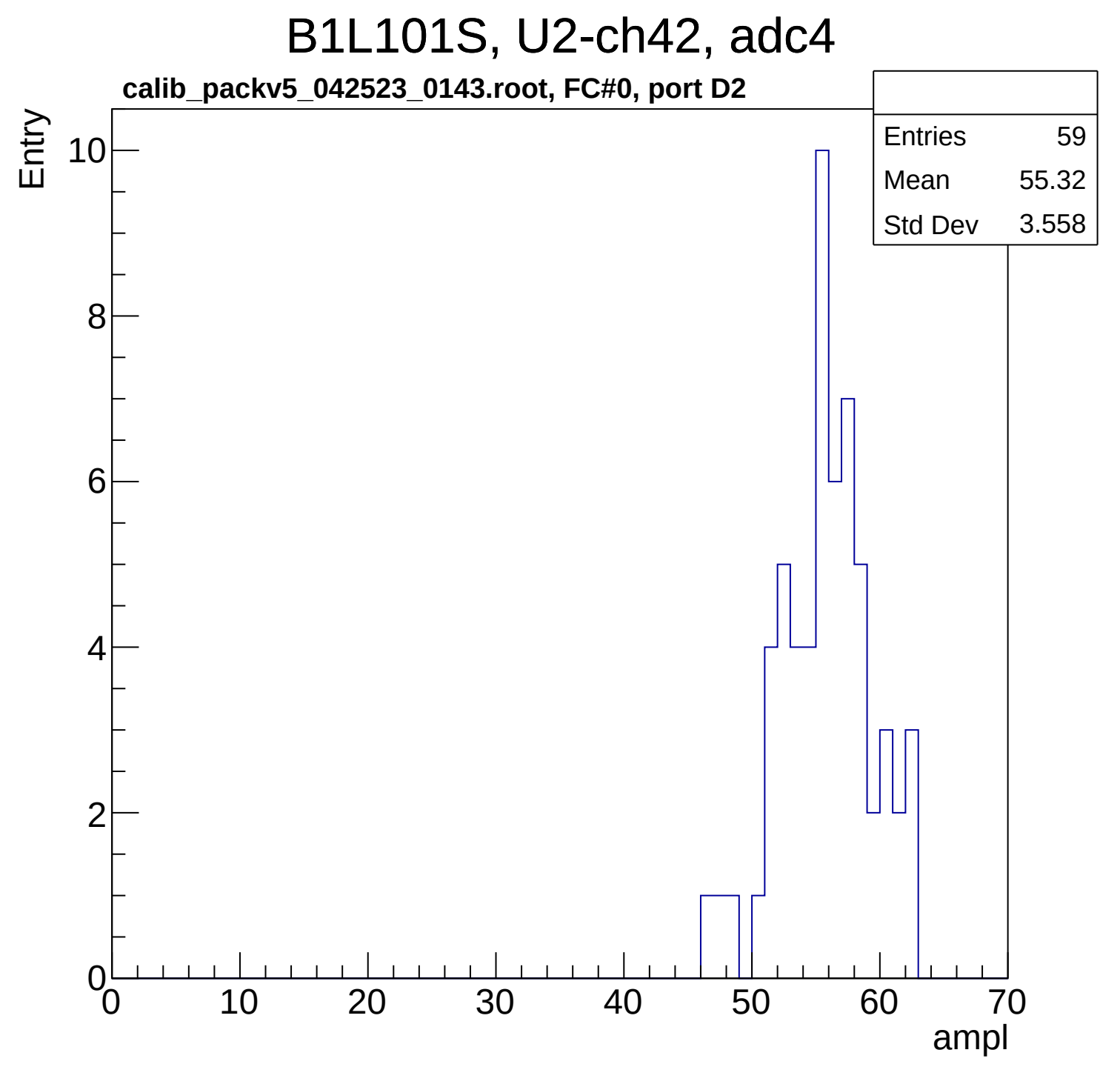

B1L101S, U2-ch41, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 17
Std Dev 24.53
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

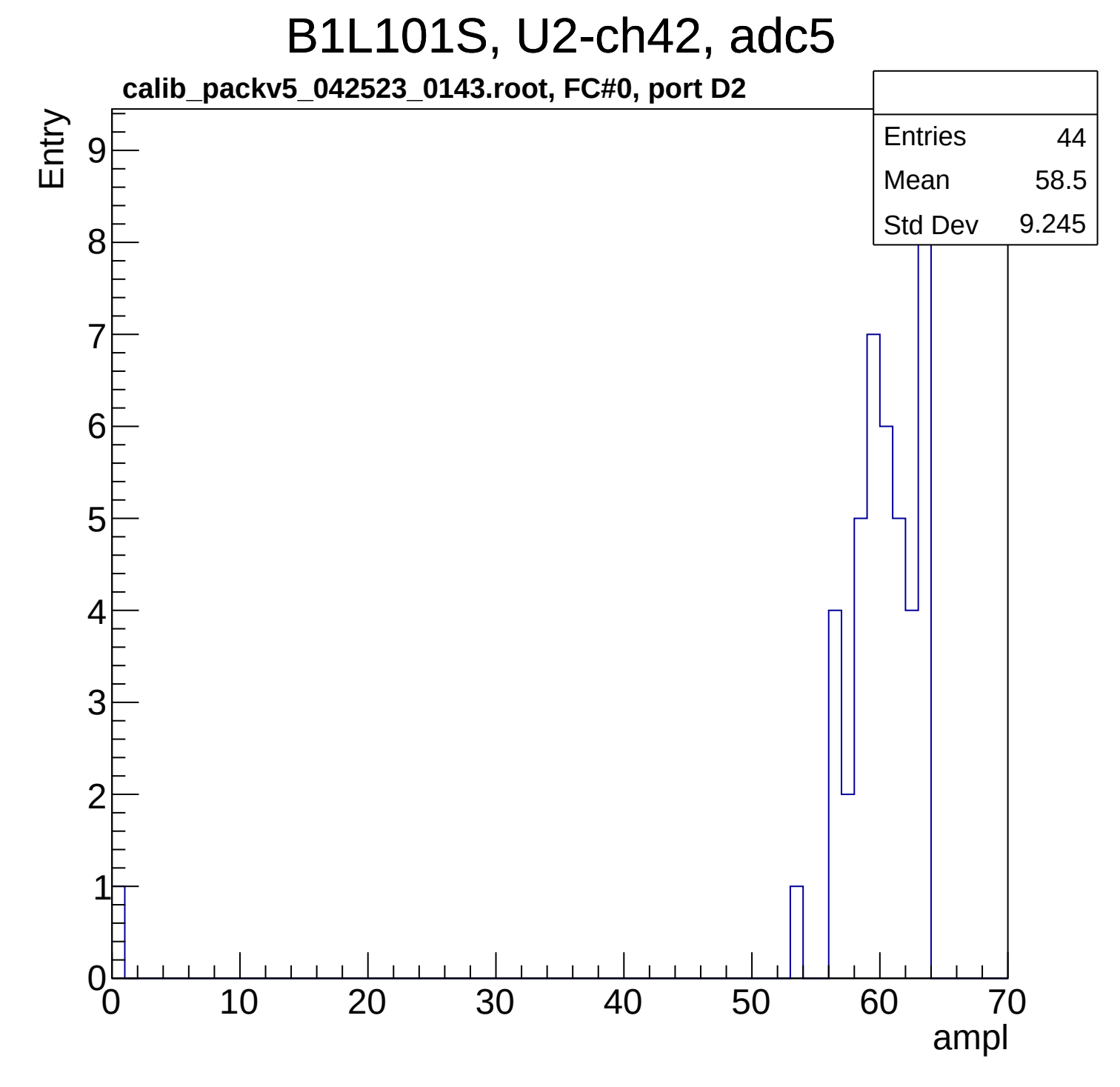

B1L101S, U2-ch42, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 29.61
Std Dev 3.699
Gaus mean : 30.4173
Gaus Width: 4.1567
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

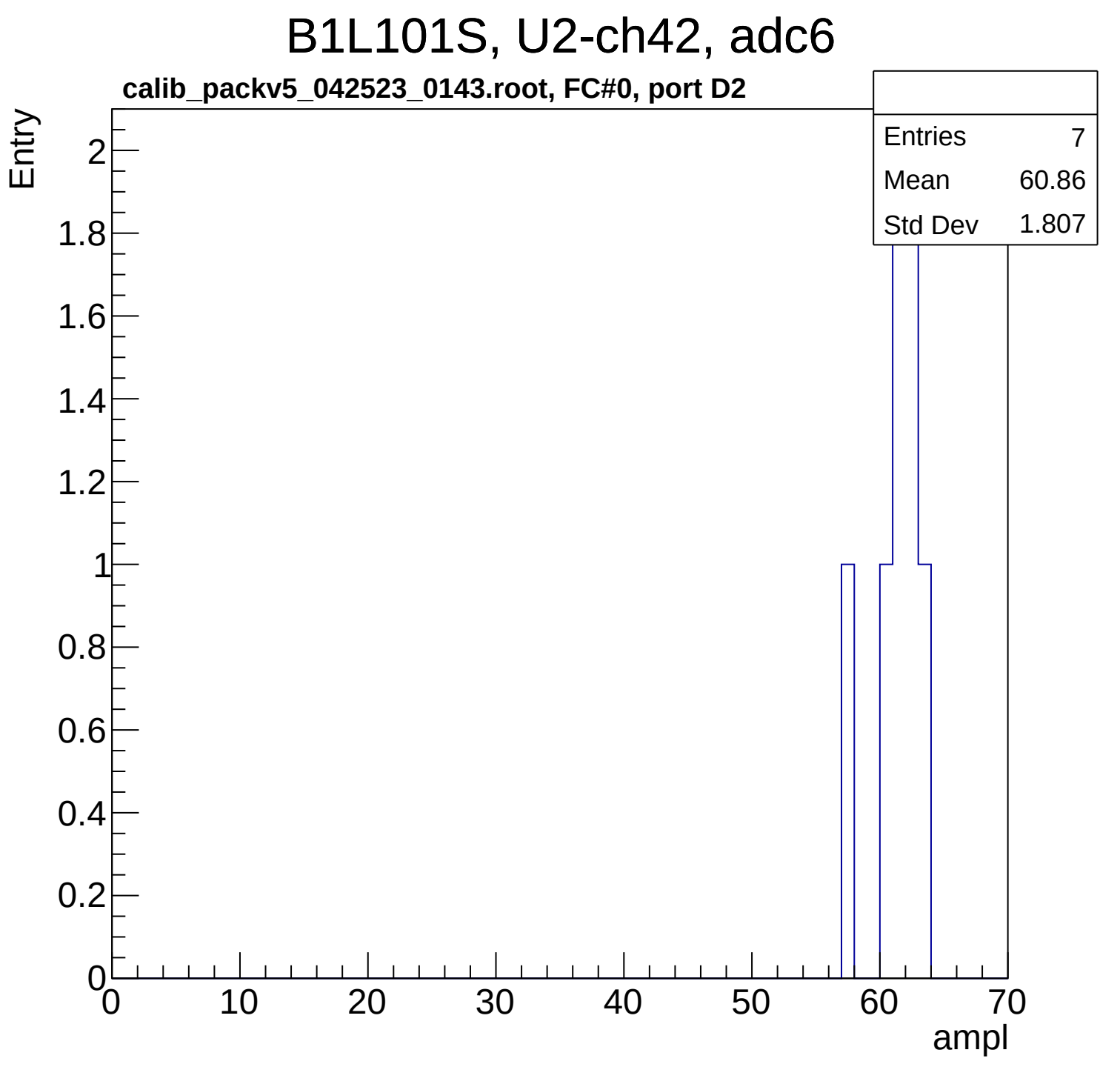

B1L101S, U2-ch42, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 41
Mean 35.8
Std Dev 4.238
Gaus mean : 36.4627
Gaus Width: 5.1749
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

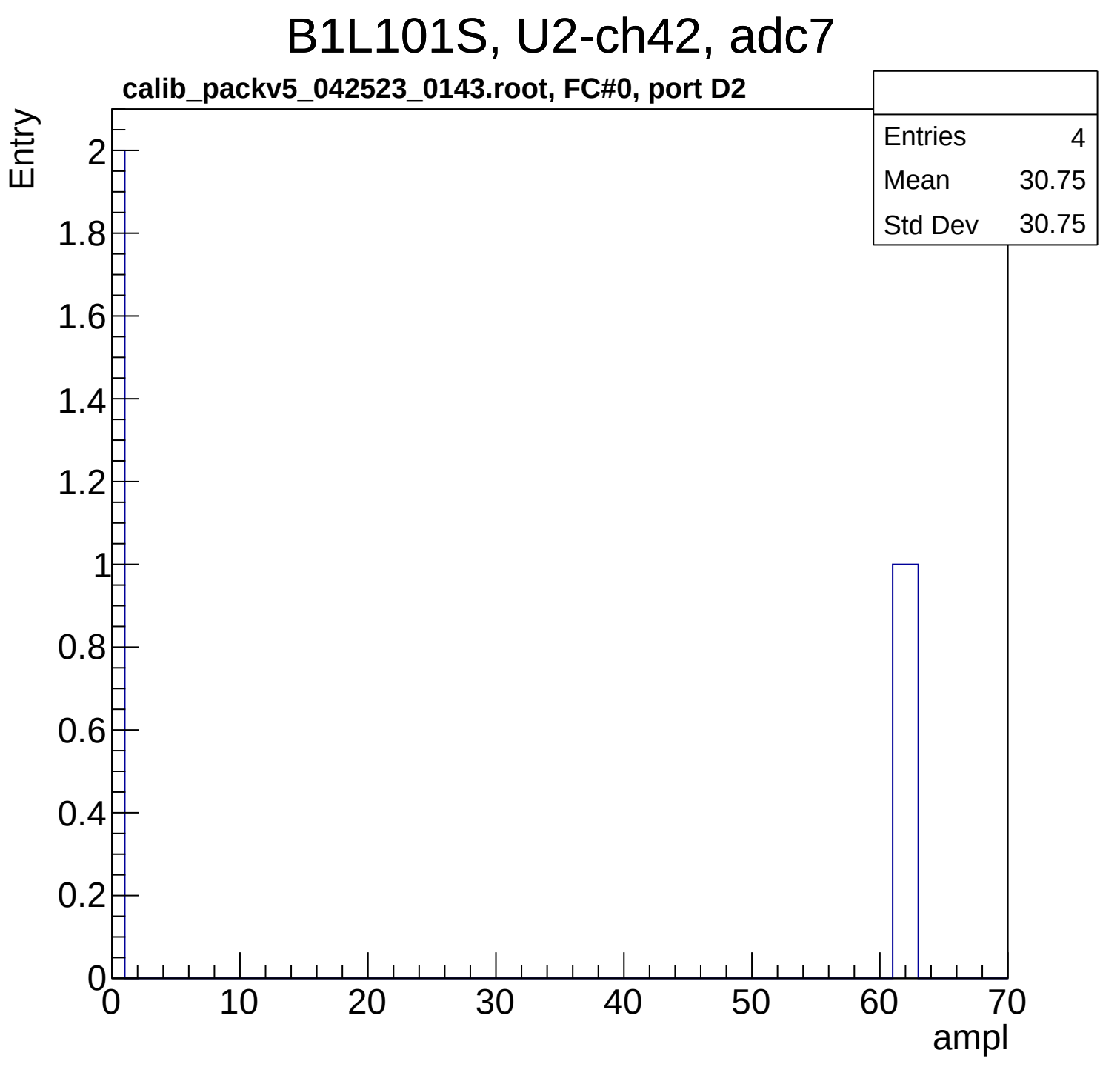

B1L101S, U2-ch42, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 41.03
Std Dev 3.719
Gaus mean : 41.1222
Gaus Width: 3.9782
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

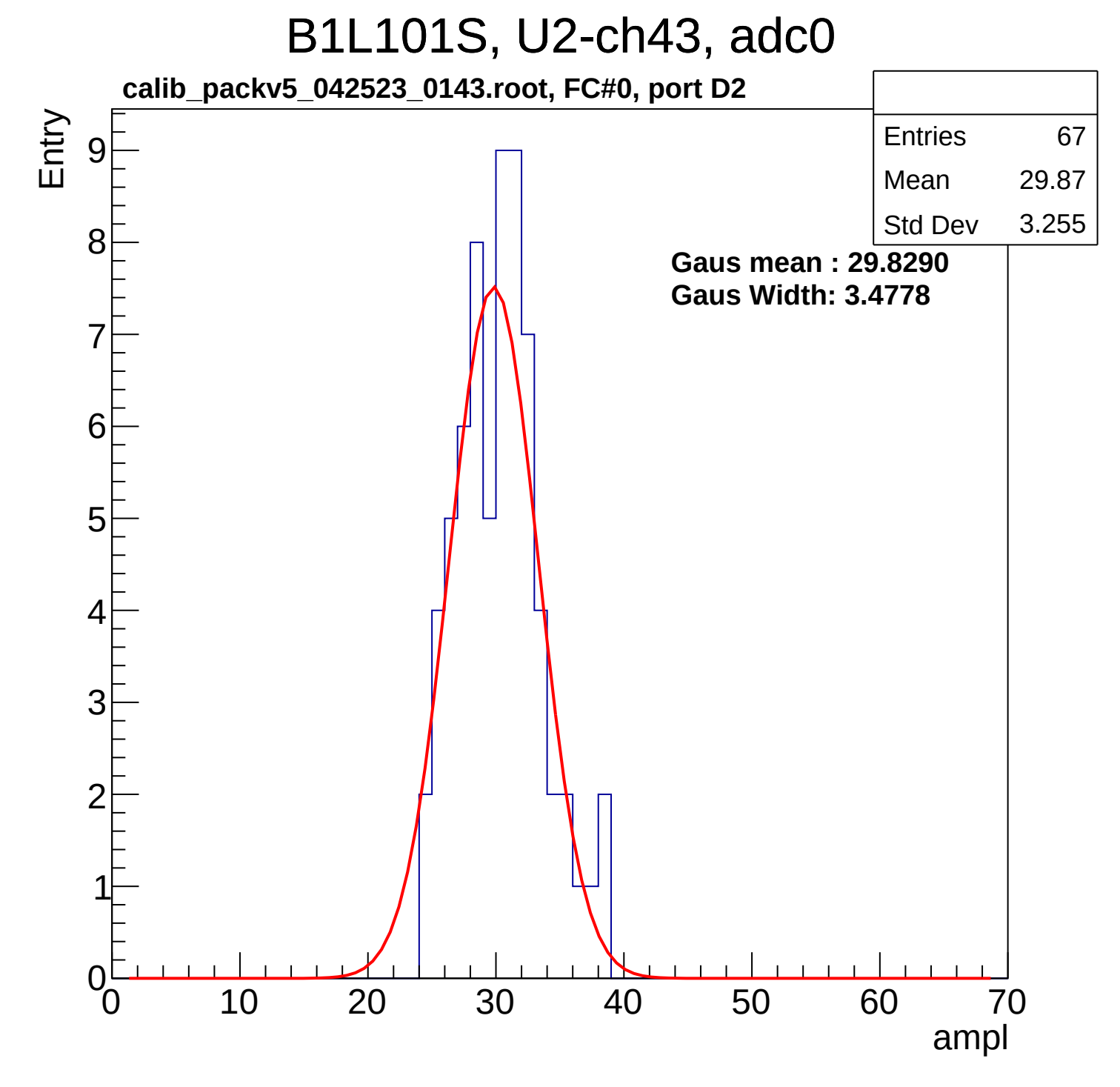

B1L101S, U2-ch42, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 48.38
Std Dev 3.828
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

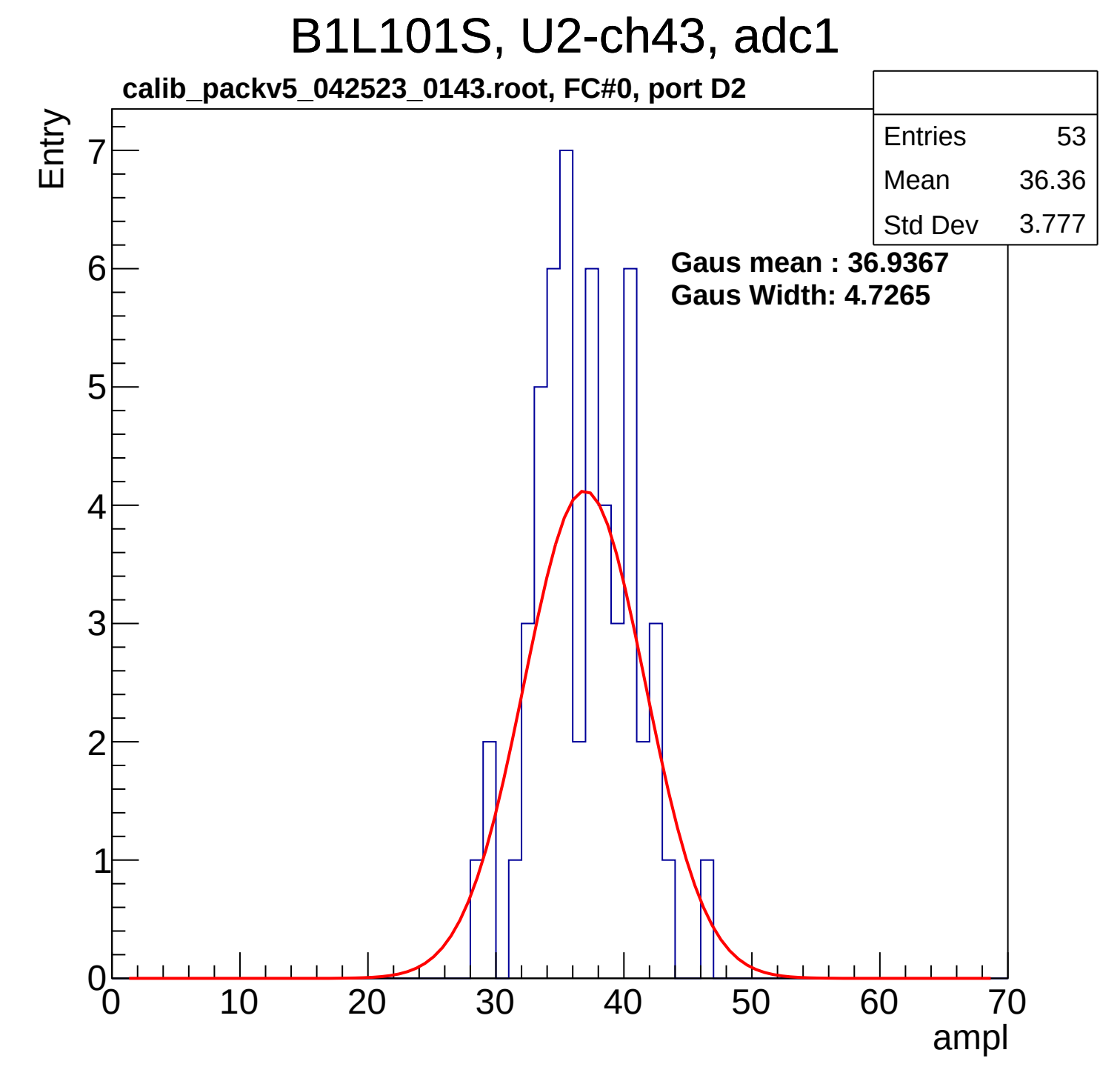

B1L101S, U2-ch42, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 55.32
Std Dev 3.558
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

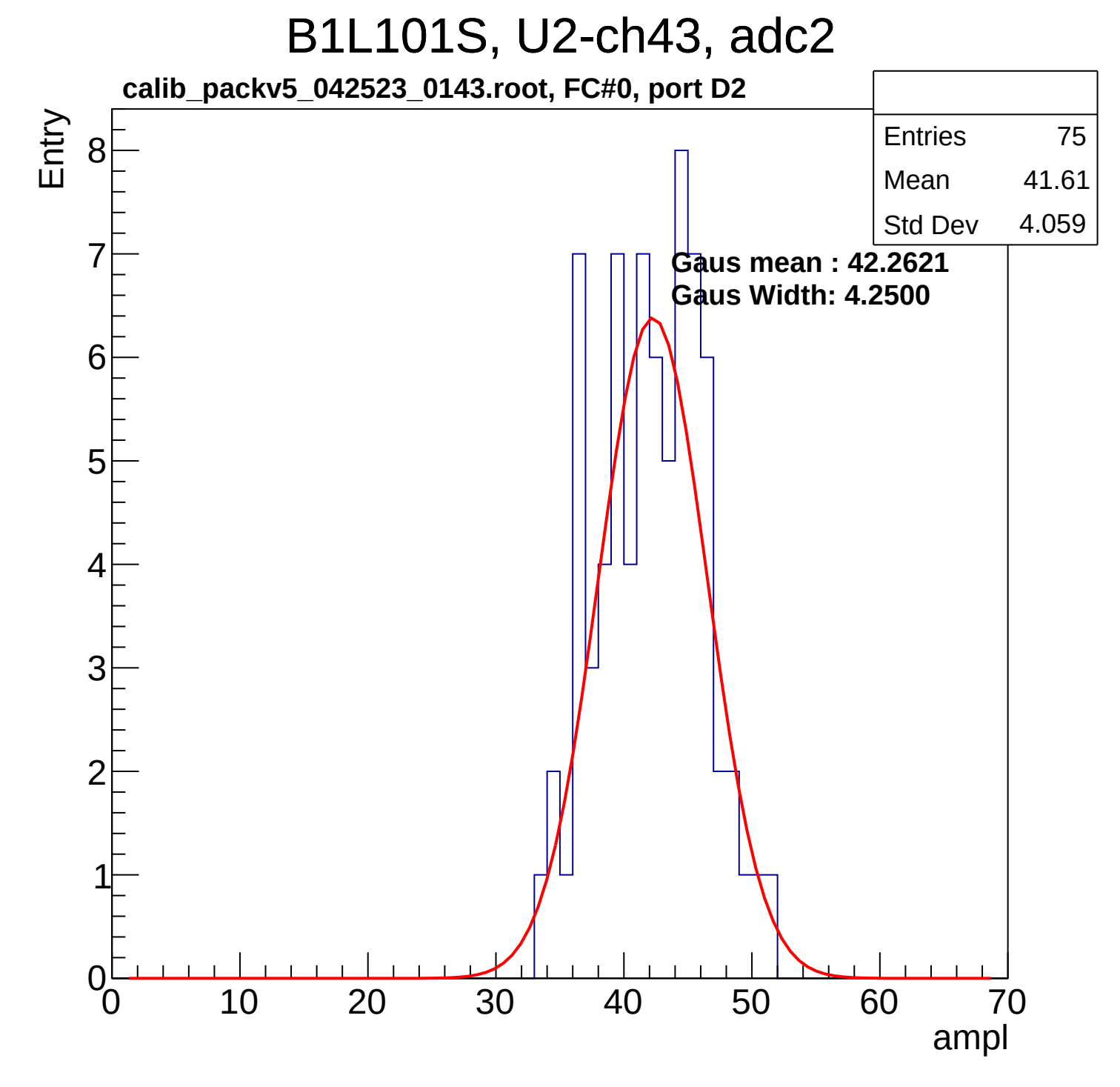

B1L101S, U2-ch42, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 44
Mean 58.5
Std Dev 9.245
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

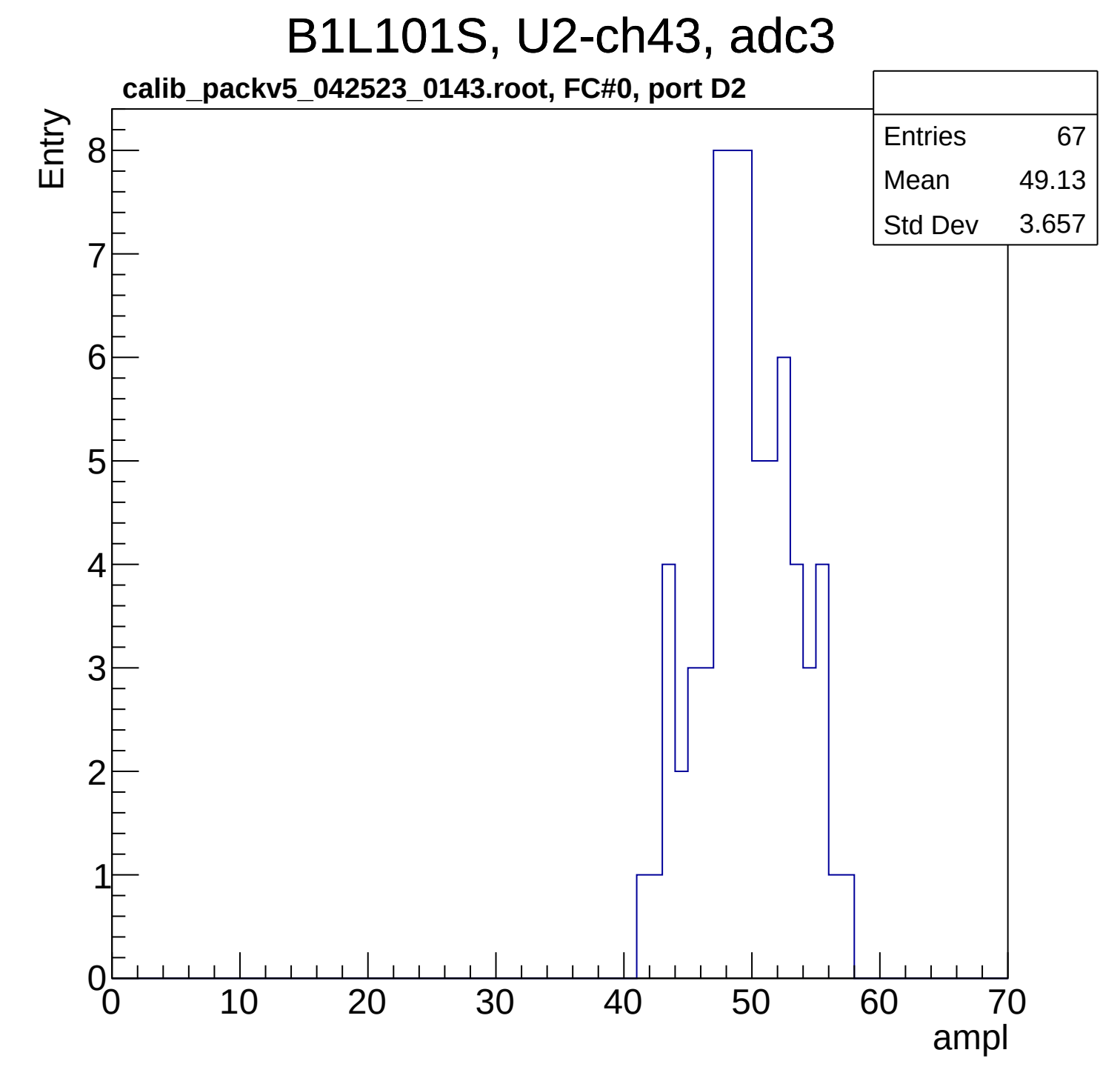

B1L101S, U2-ch42, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 60.86
Std Dev 1.807
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

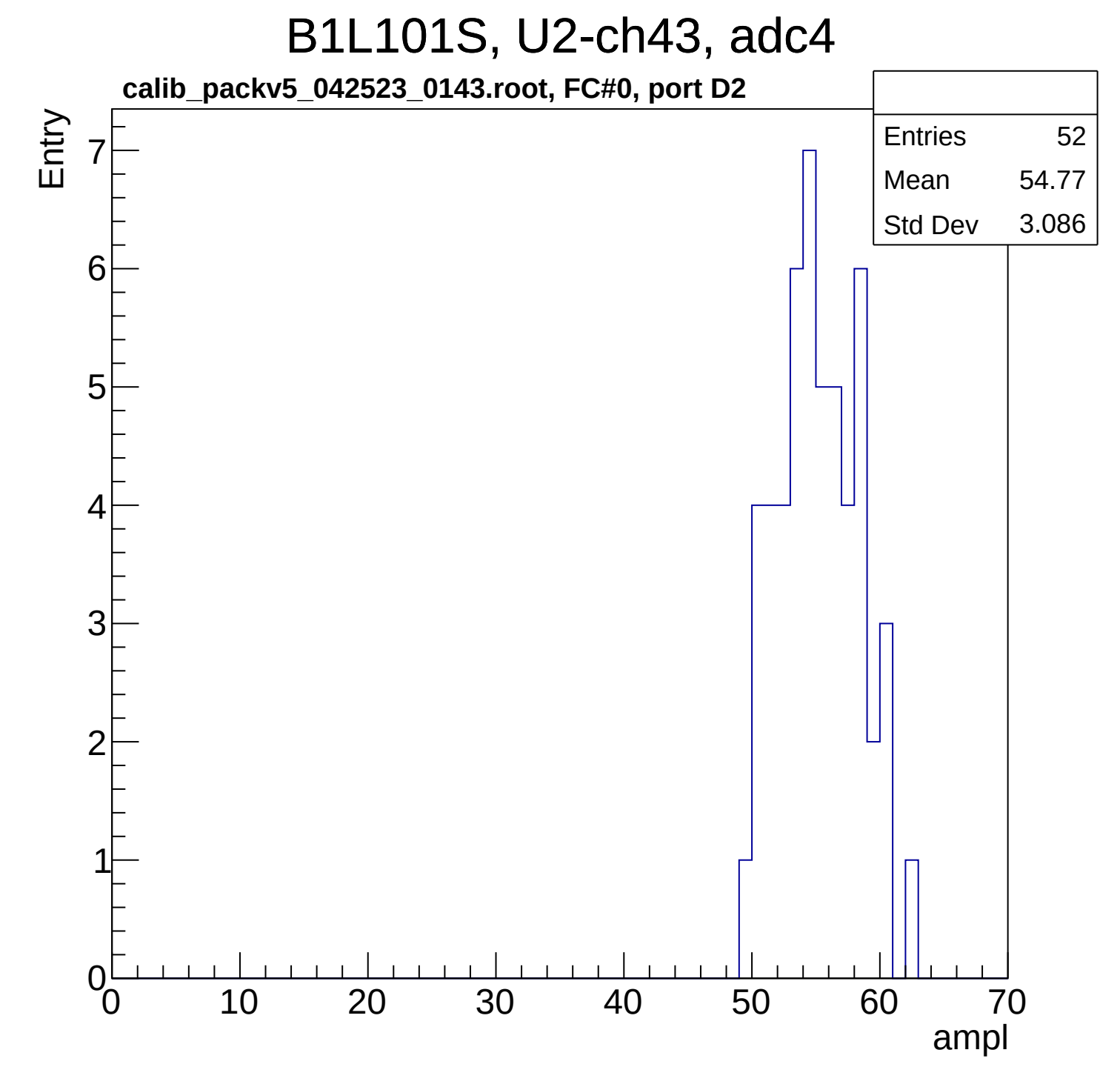

B1L101S, U2-ch42, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 30.75
Std Dev 30.75
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

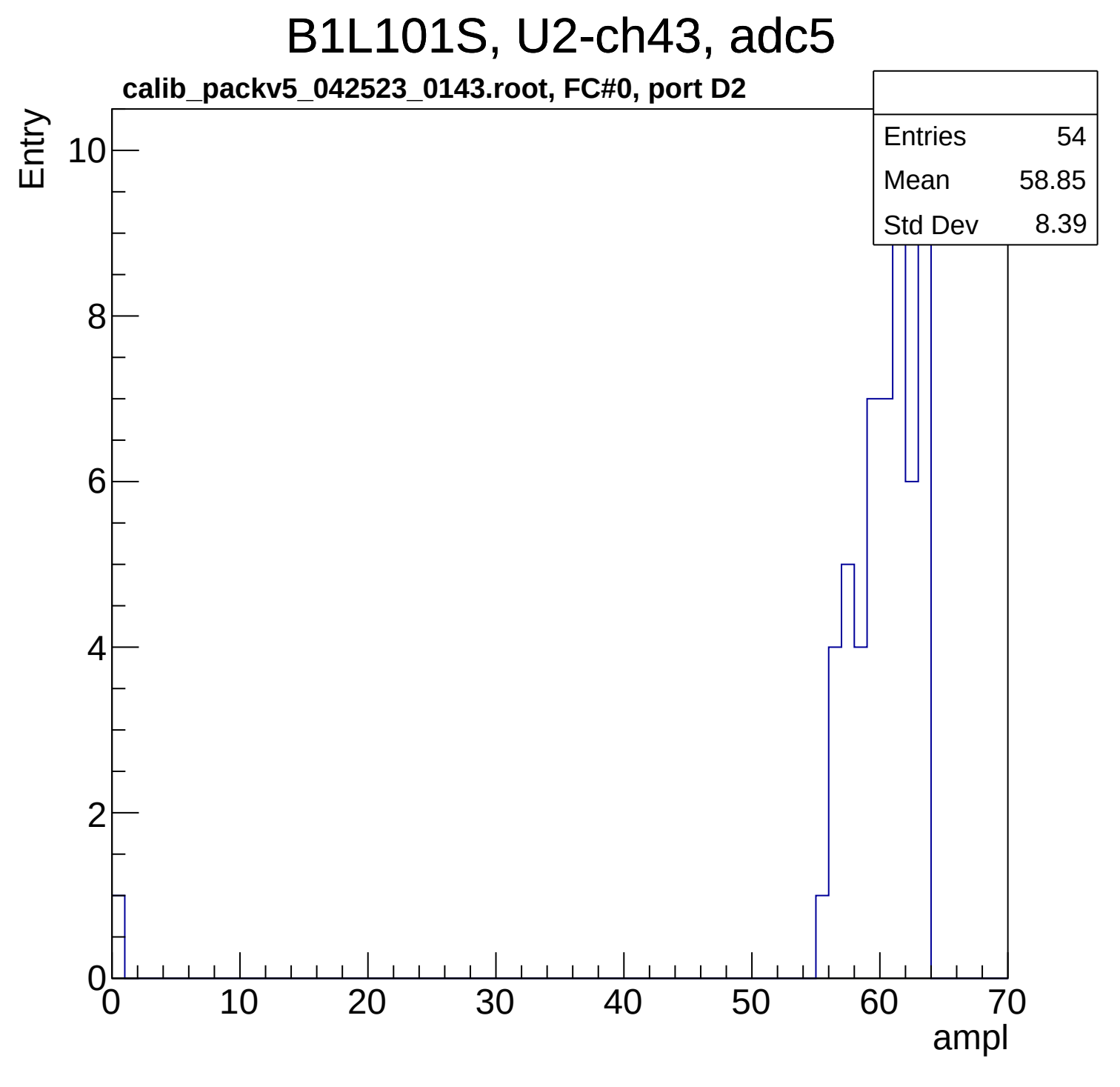

B1L101S, U2-ch43, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 29.87
Std Dev 3.255
Gaus mean : 29.8290
Gaus Width: 3.4778
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

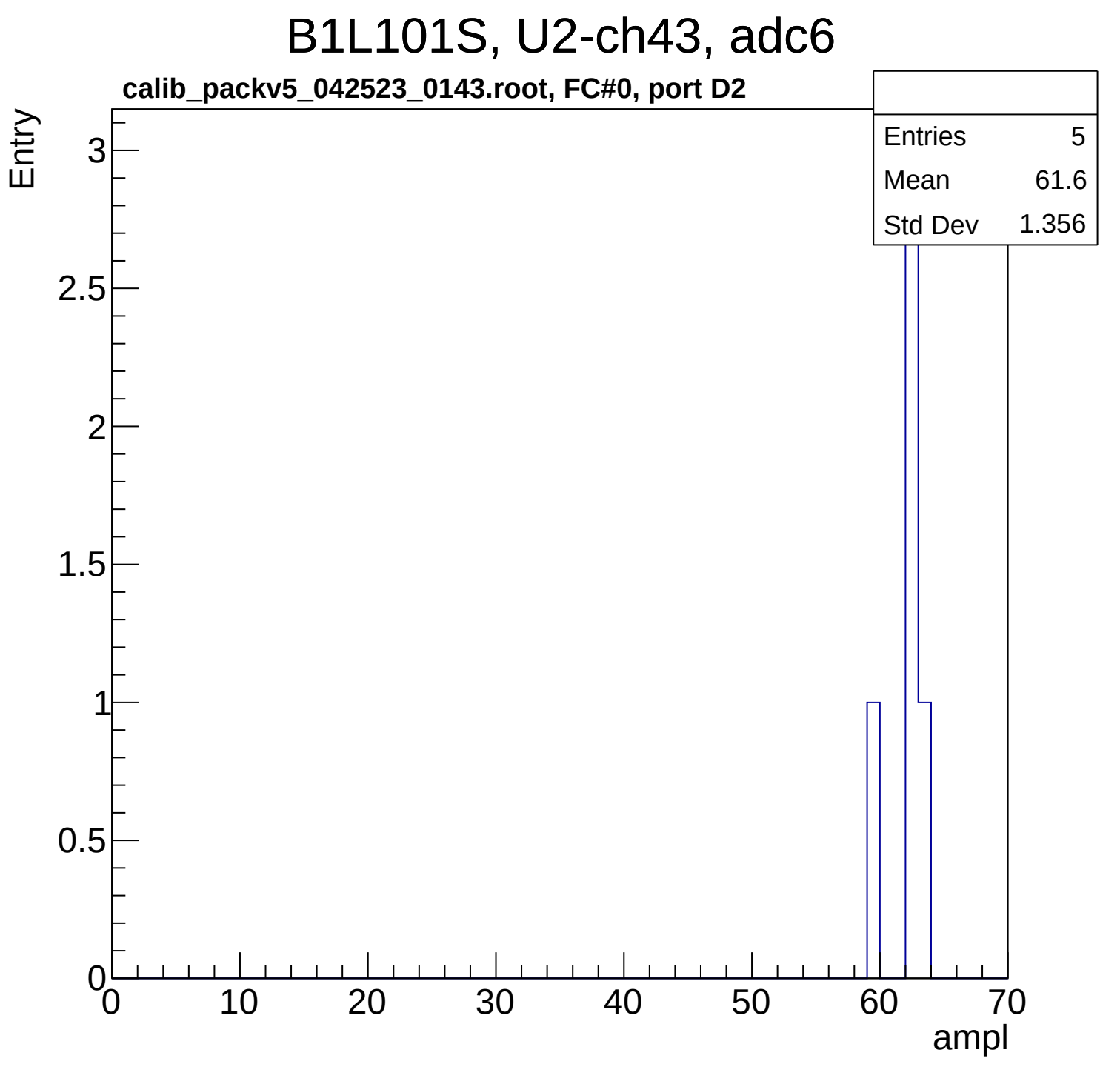

B1L101S, U2-ch43, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 36.36
Std Dev 3.777
Gaus mean : 36.9367
Gaus Width: 4.7265
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

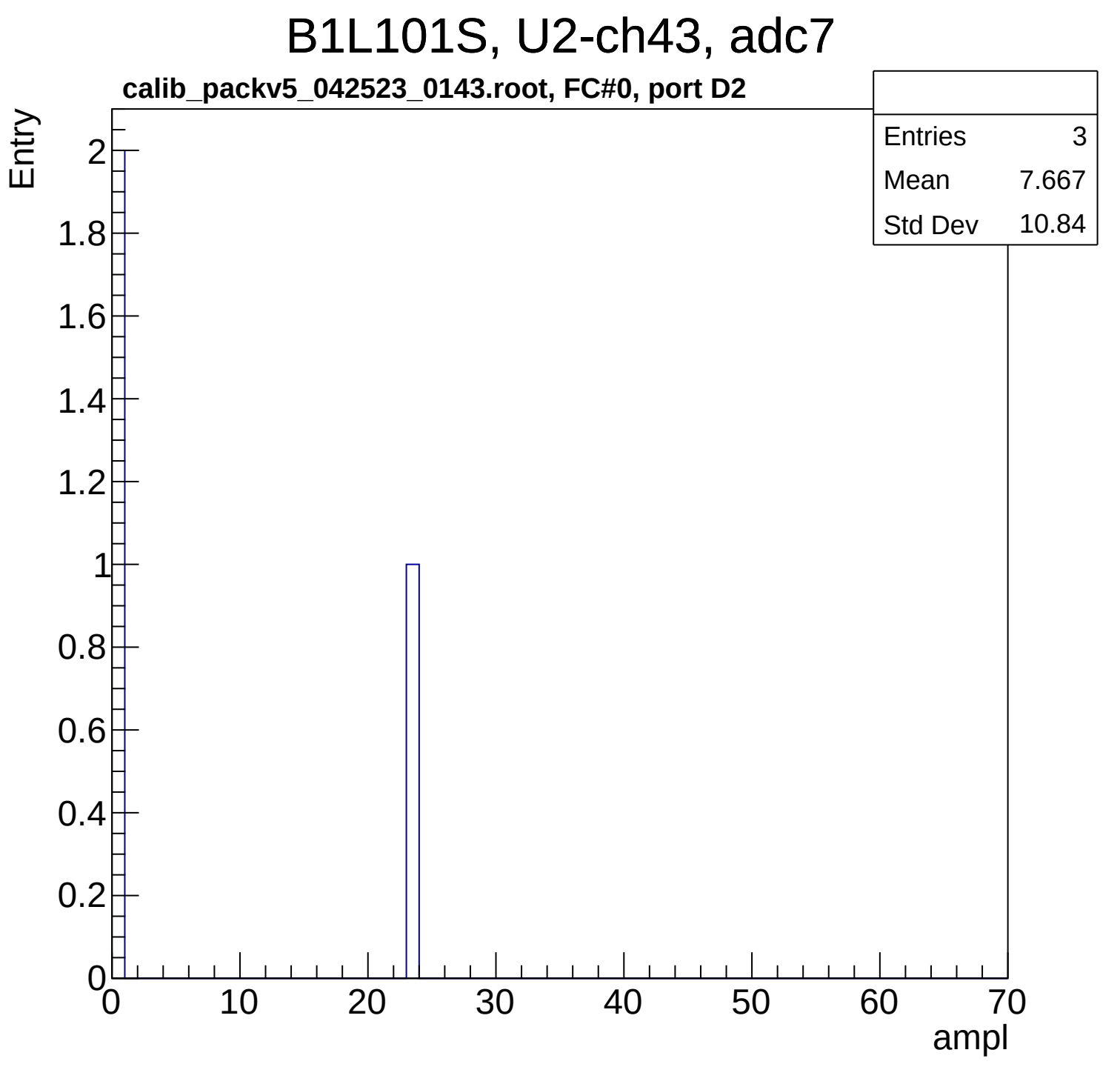

B1L101S, U2-ch43, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 41.61
Std Dev 4.059
Gaus mean : 42.2621
Gaus Width: 4.2500
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

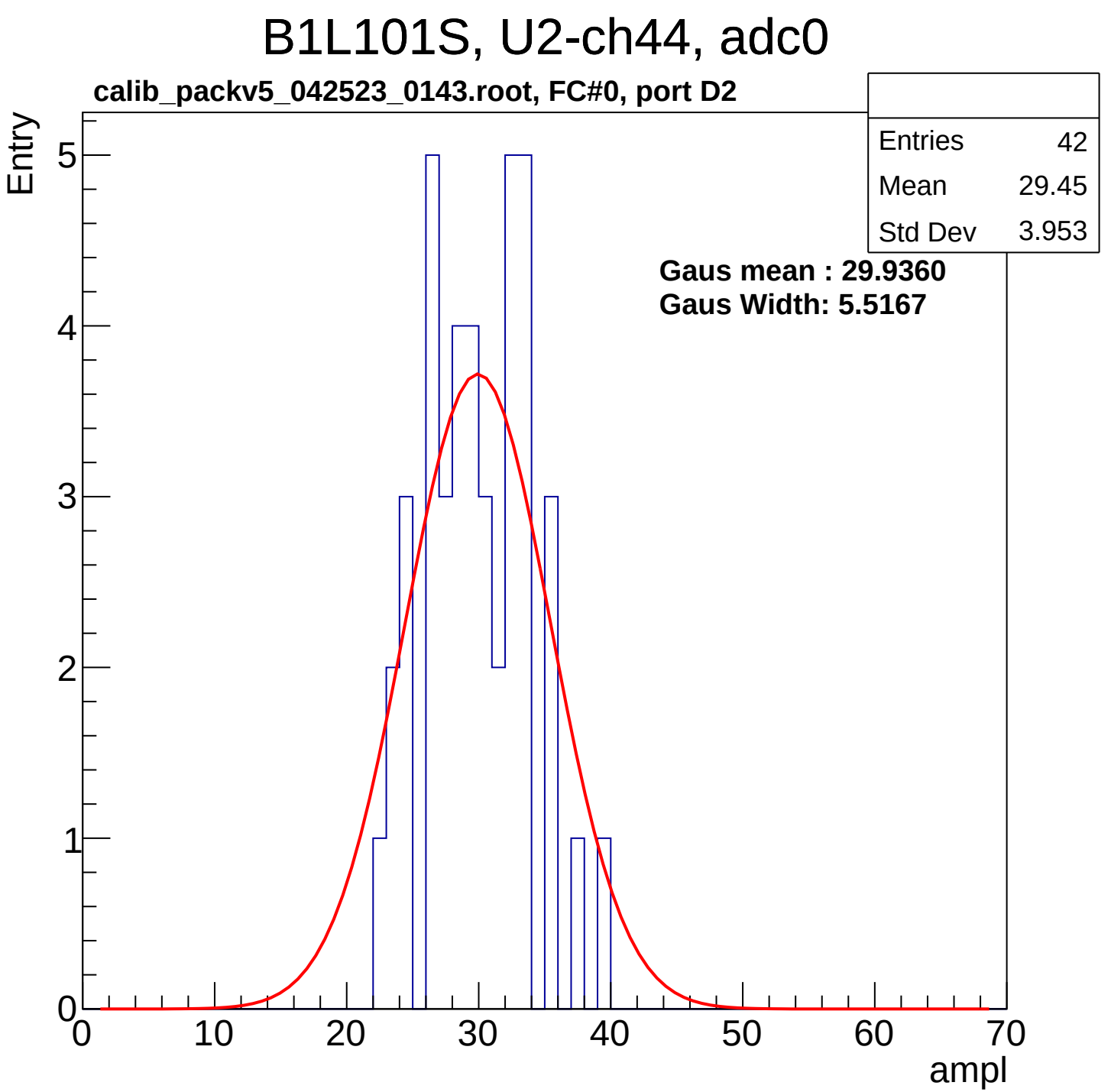

B1L101S, U2-ch43, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 49.13
Std Dev 3.657
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

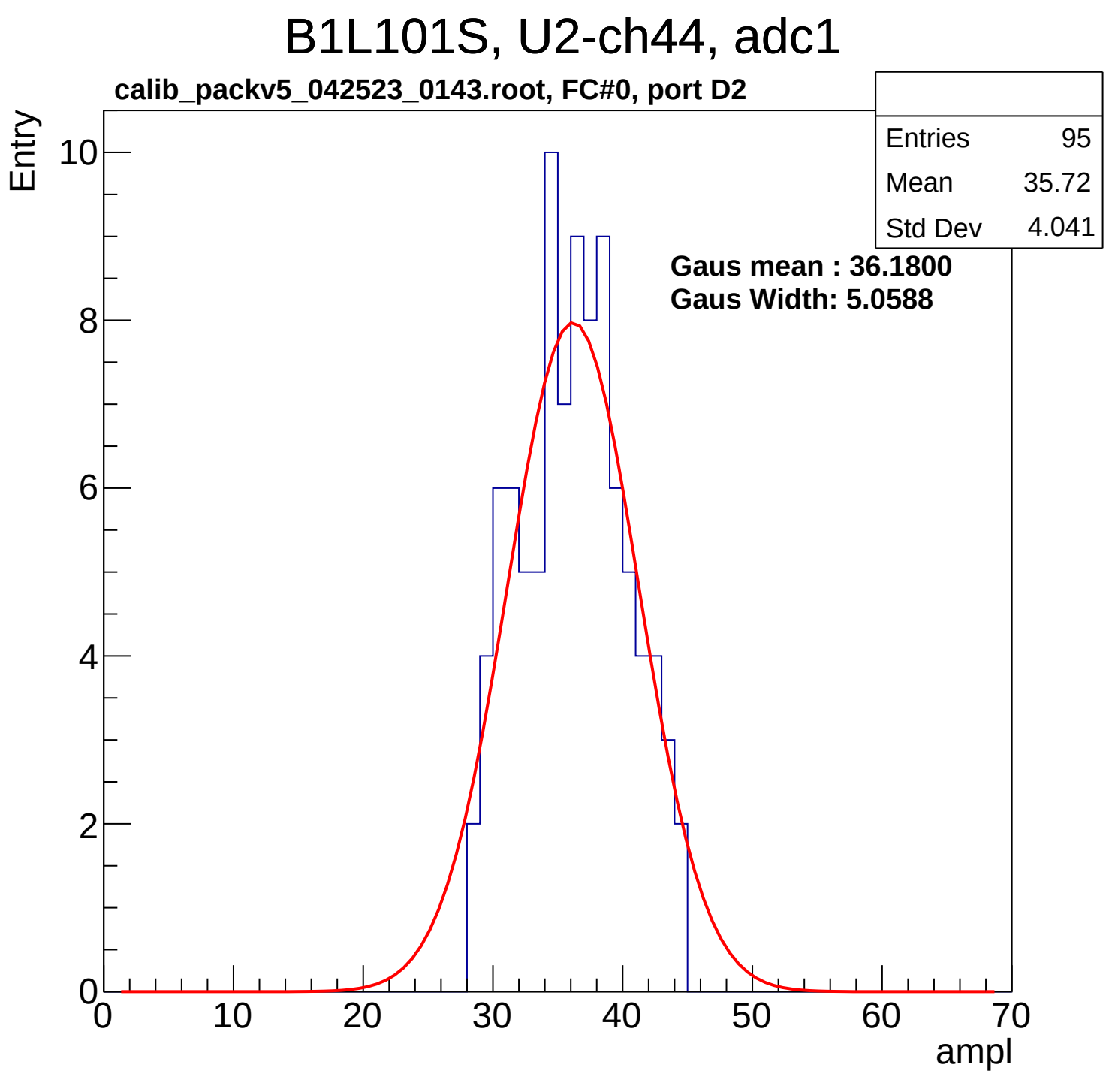

B1L101S, U2-ch43, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 54.77
Std Dev 3.086
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

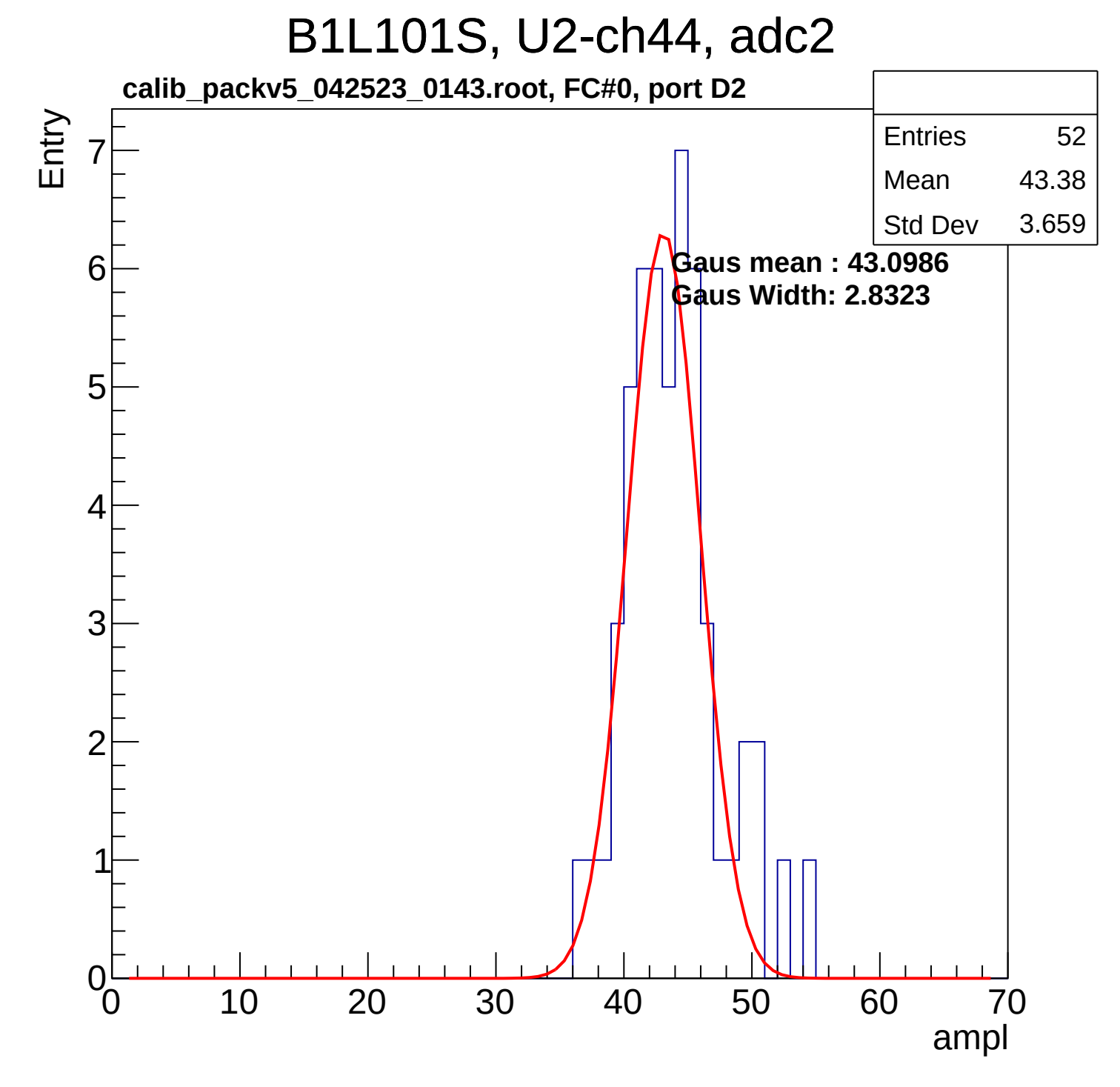

B1L101S, U2-ch43, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 58.85
Std Dev 8.39
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

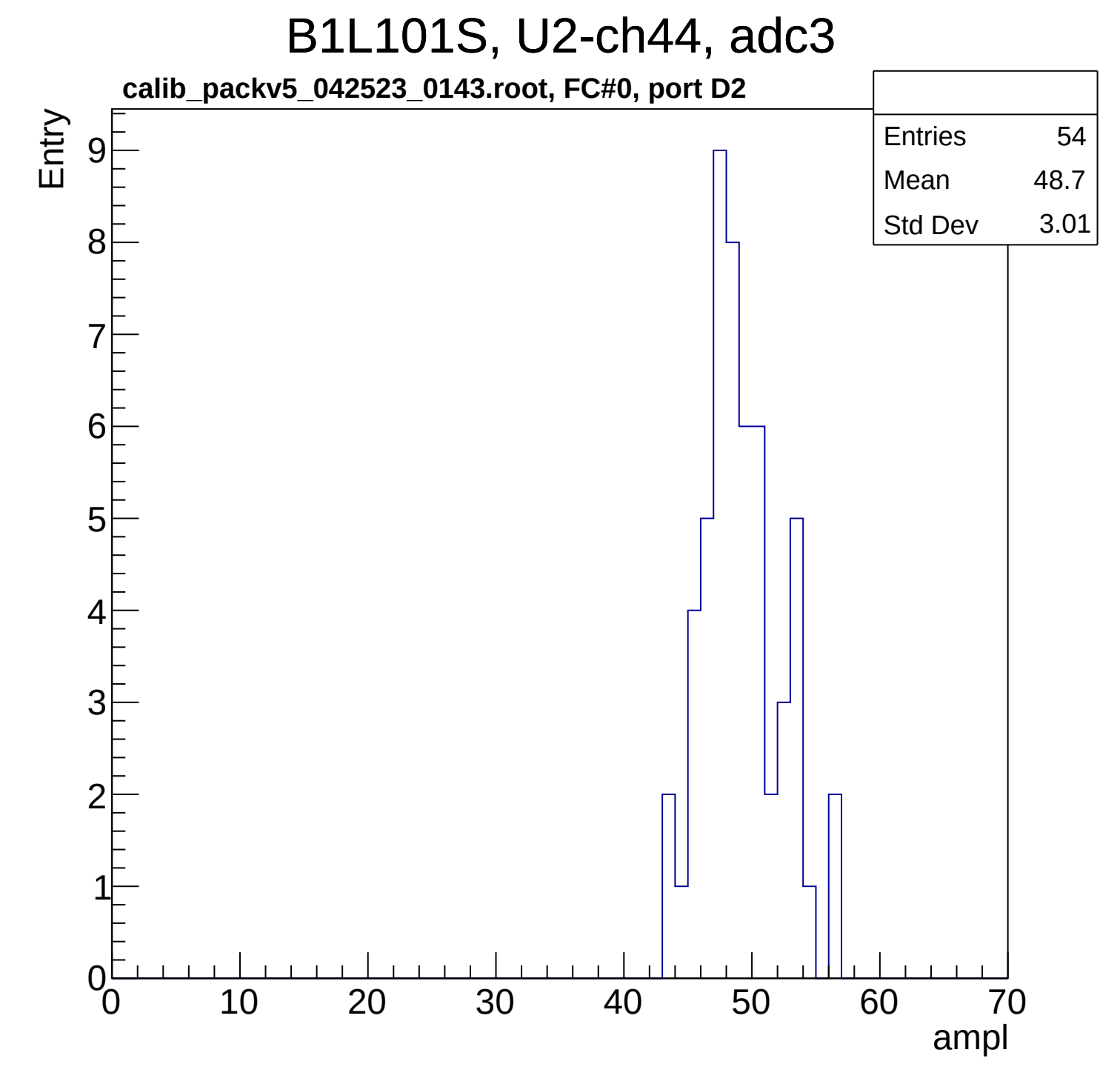

B1L101S, U2-ch43, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 61.6
Std Dev 1.356
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

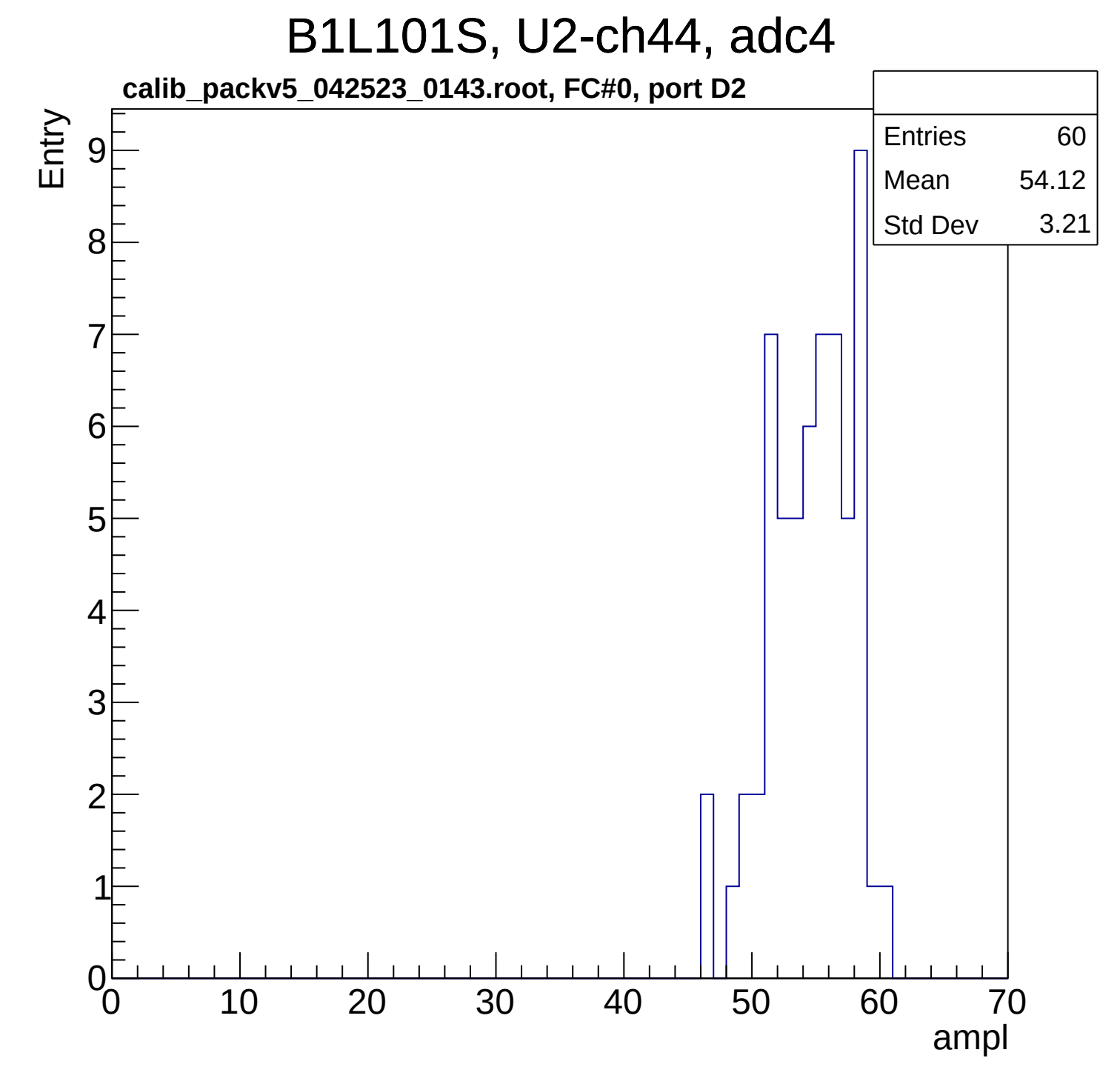

B1L101S, U2-ch43, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 7.667
Std Dev 10.84
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

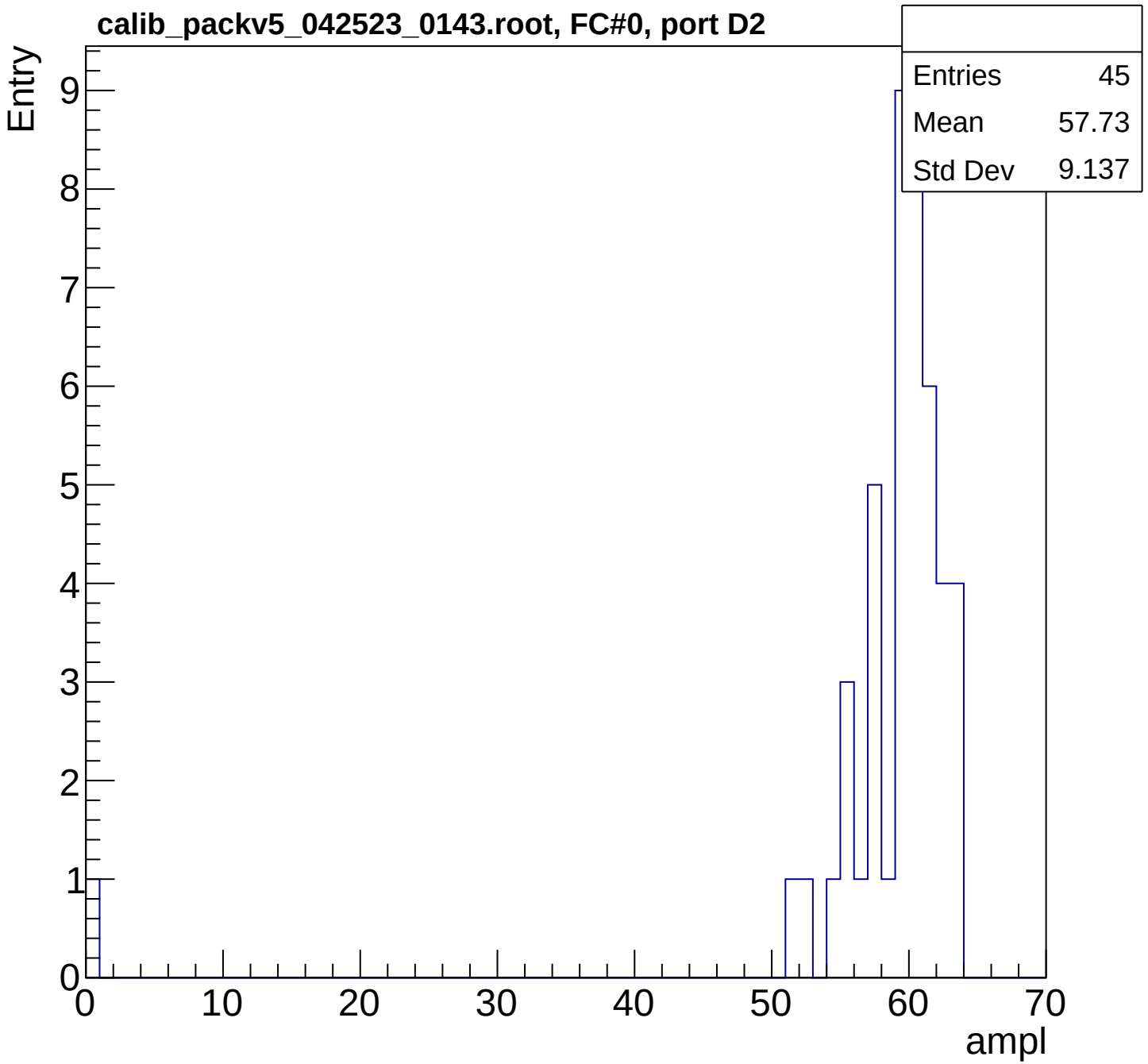

B1L101S, U2-ch44, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 29.45
Std Dev 3.953
Gaus mean : 29.9360
Gaus Width: 5.5167
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

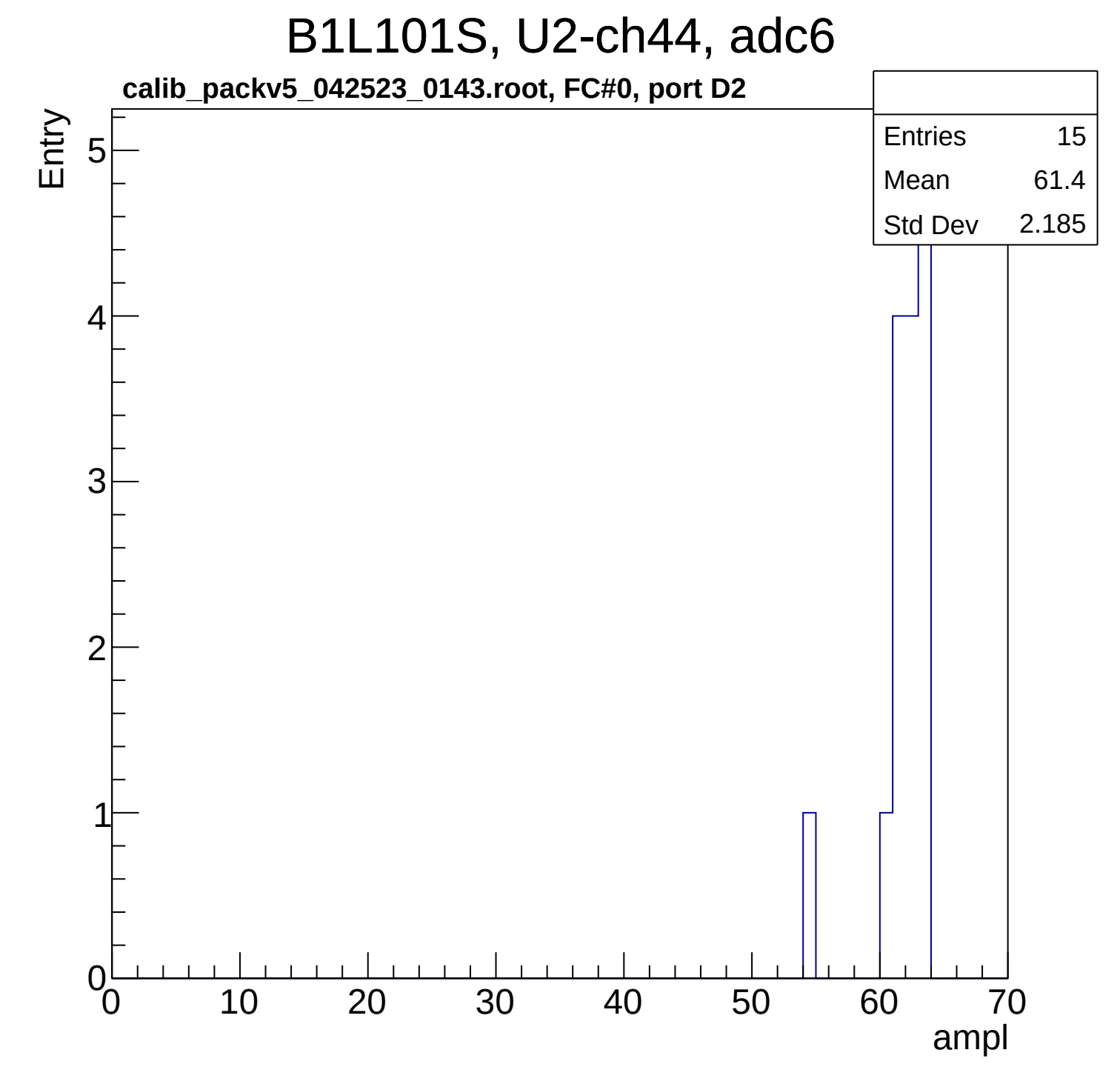

B1L101S, U2-ch44, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 95
Mean 35.72
Std Dev 4.041
Gaus mean : 36.1800
Gaus Width: 5.0588
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

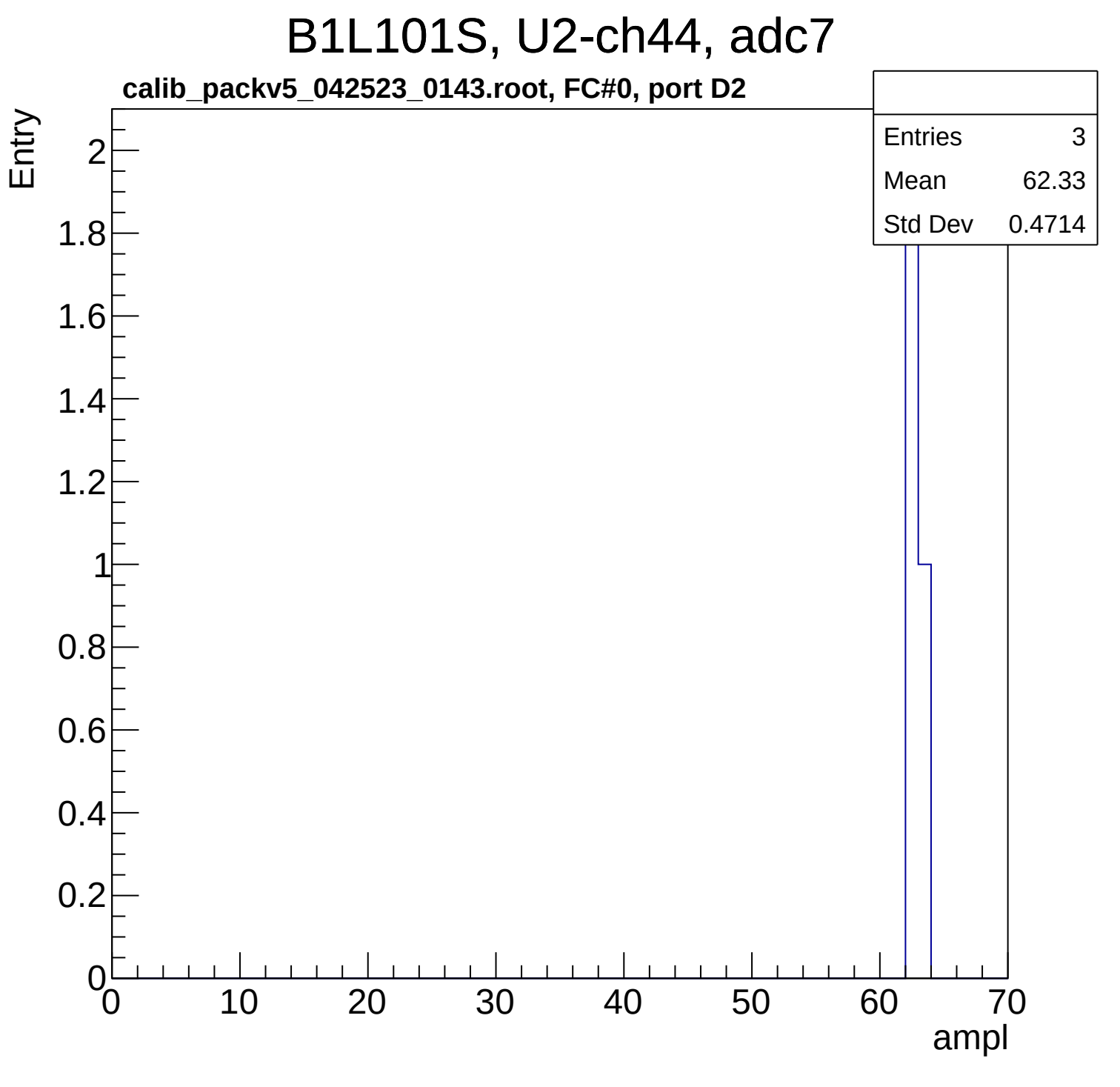

B1L101S, U2-ch44, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 43.38
Std Dev 3.659
Gaus mean : 43.0986
Gaus Width: 2.8323
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

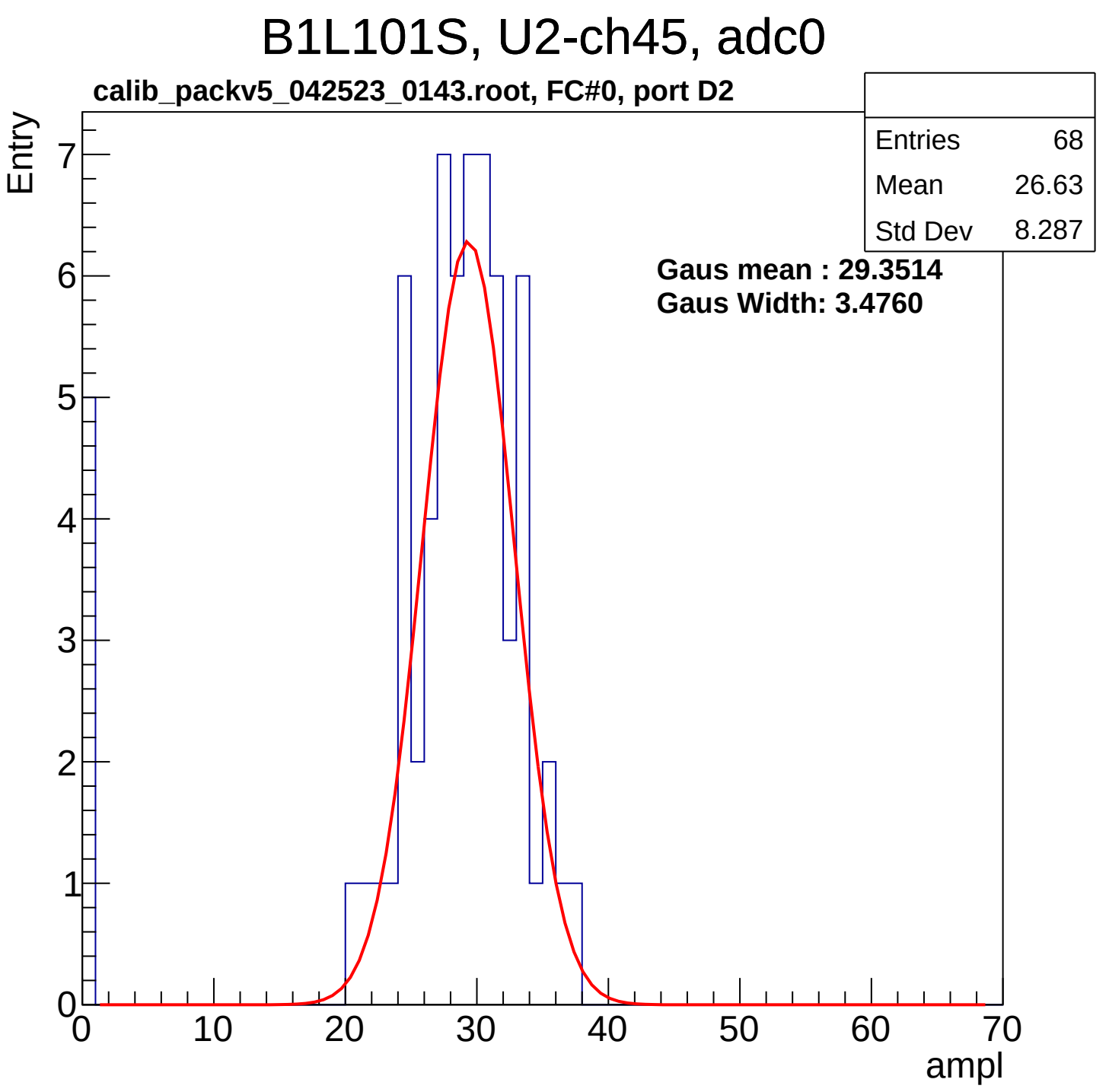

B1L101S, U2-ch44, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 48.7
Std Dev 3.01
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

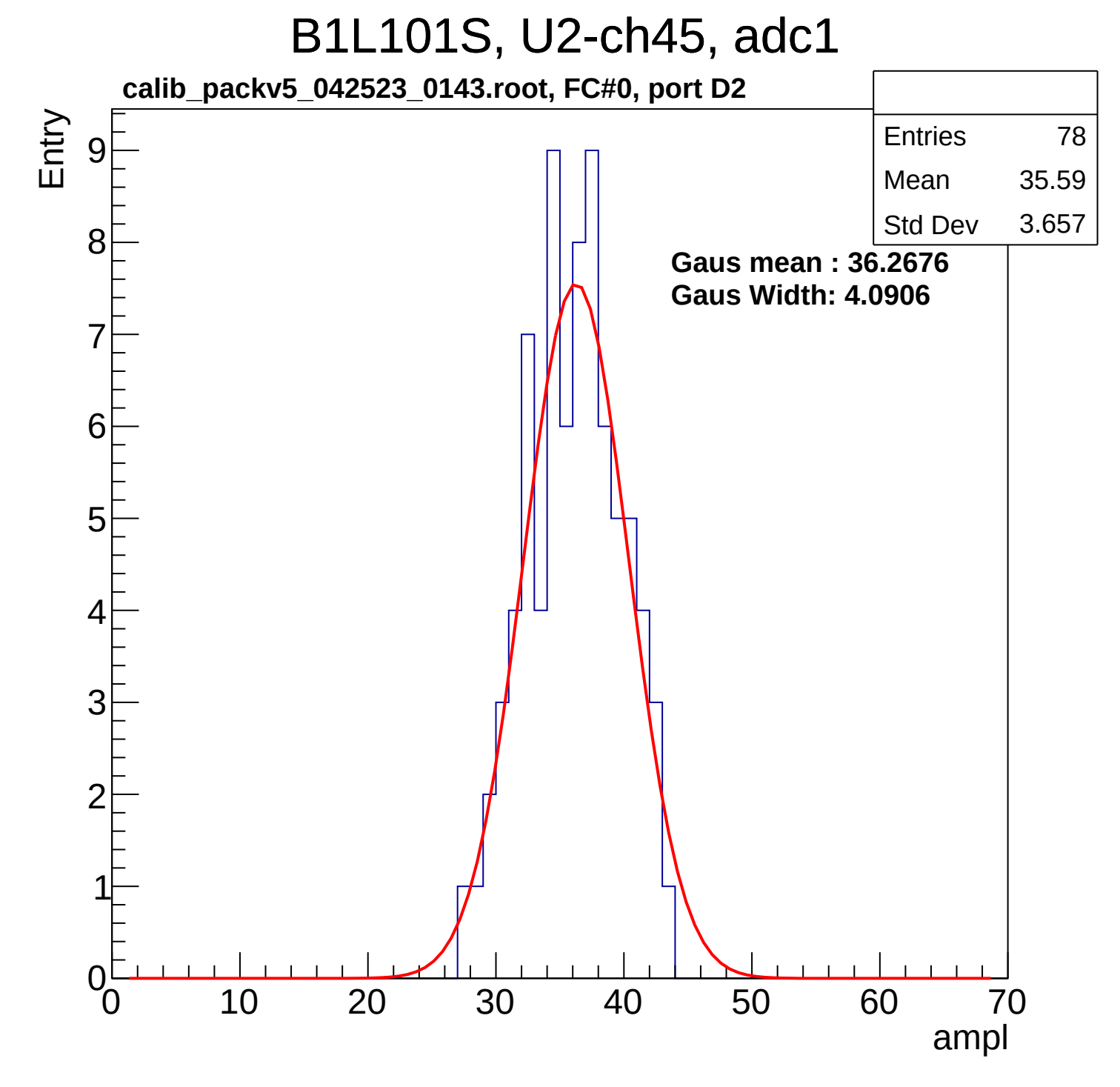

B1L101S, U2-ch44, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 54.12
Std Dev 3.21
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

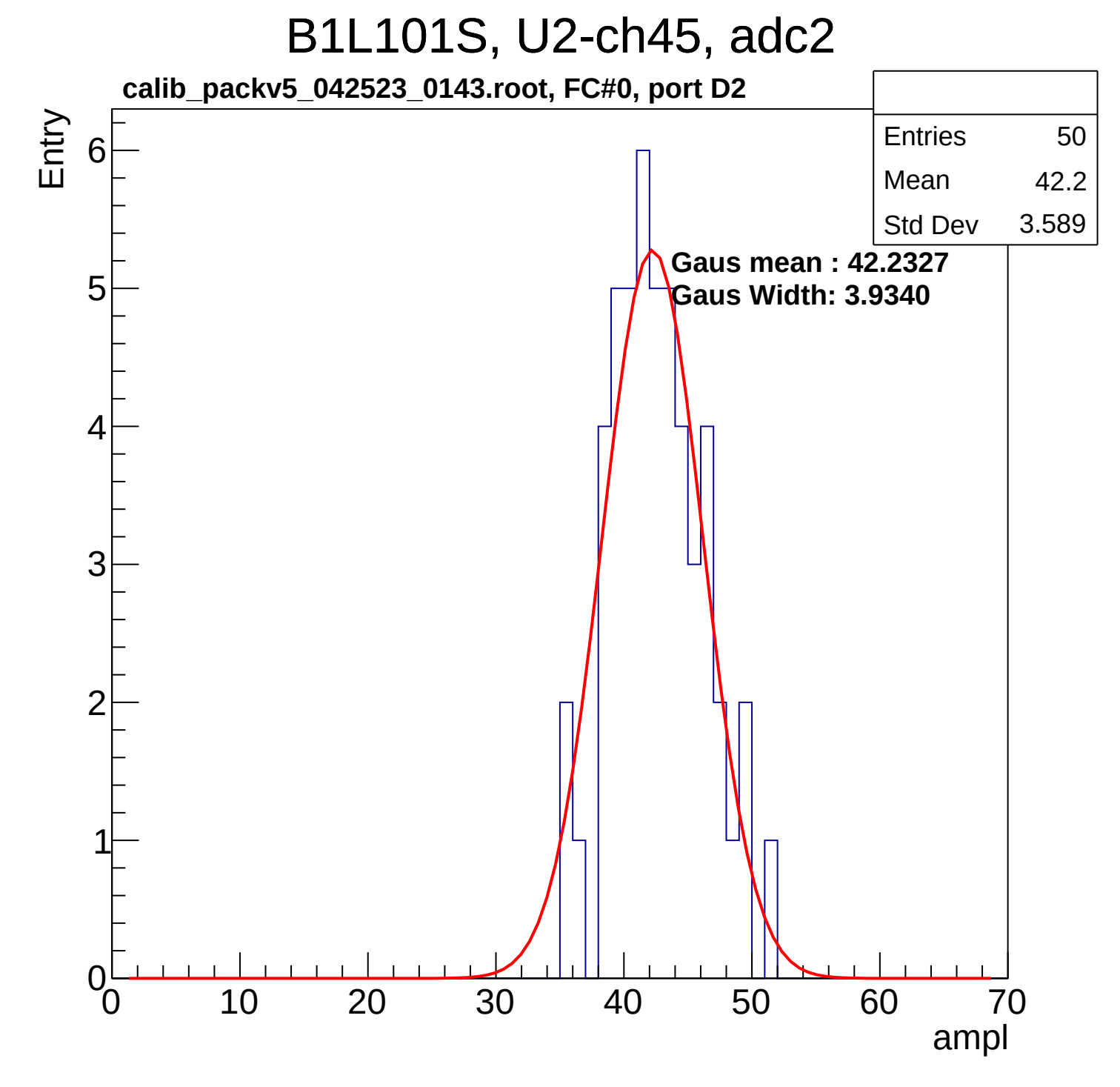

B1L101S, U2-ch44, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 57.73
Std Dev 9.137
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

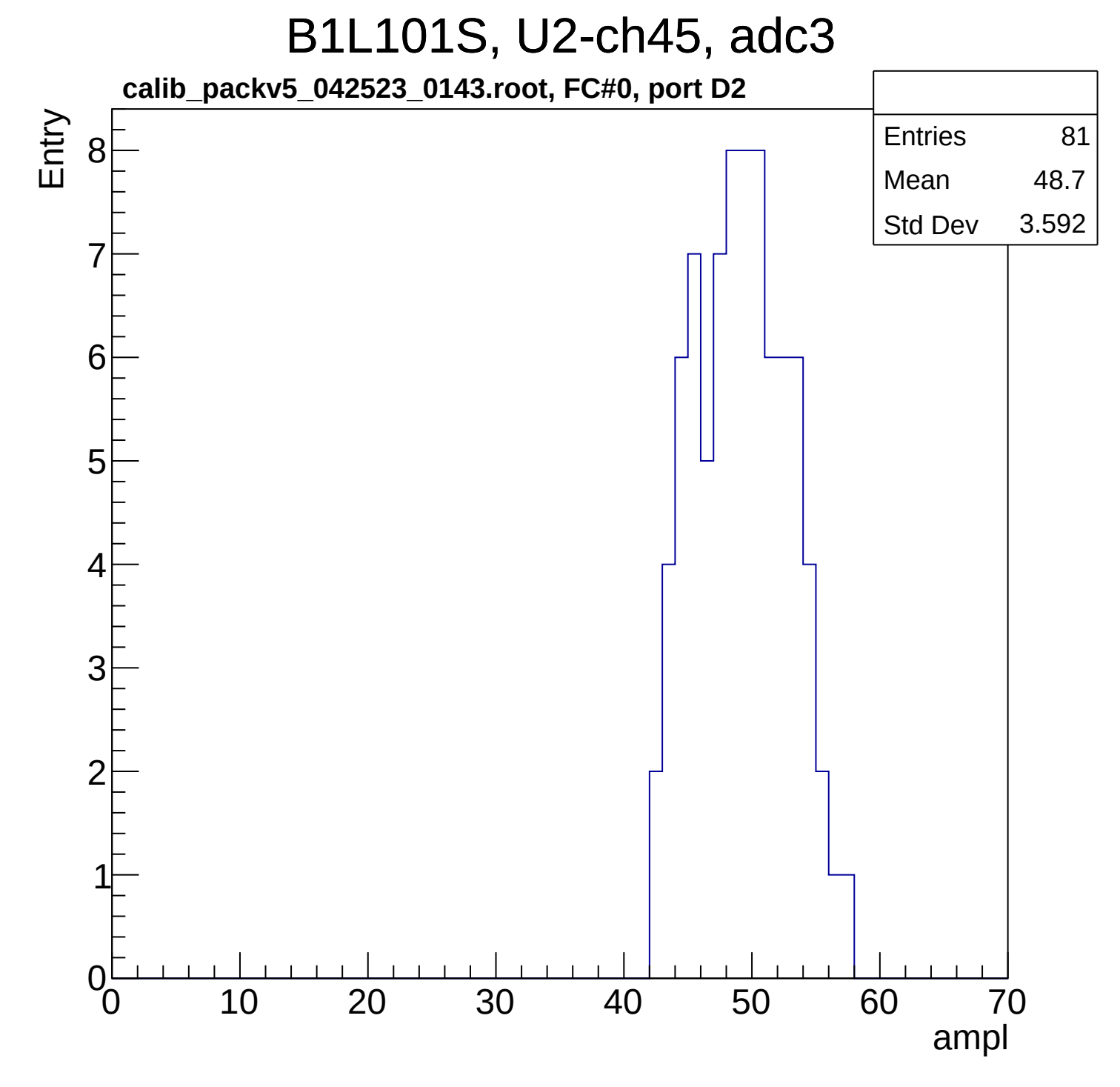

B1L101S, U2-ch44, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 15
Mean 61.4
Std Dev 2.185
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

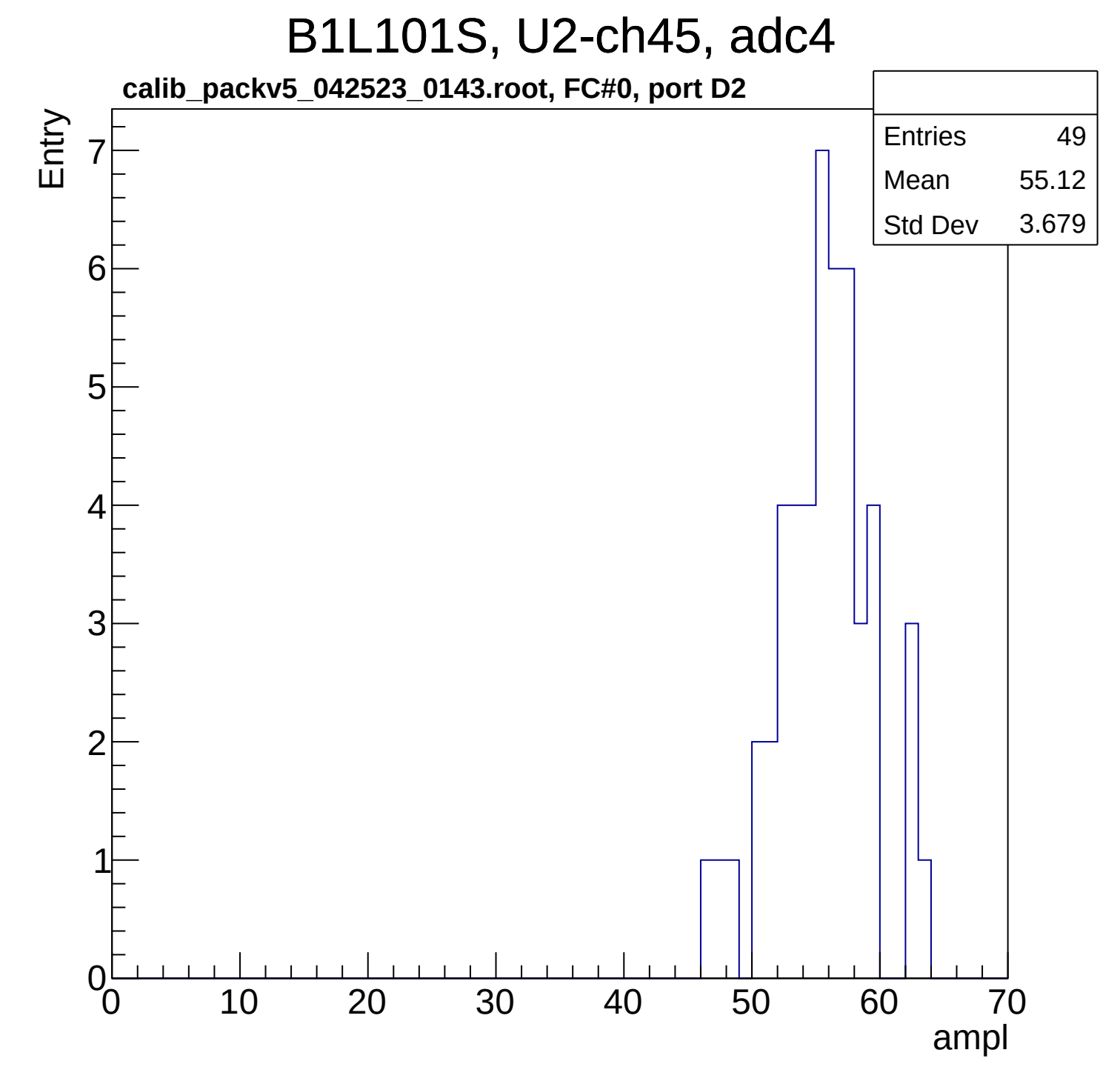

B1L101S, U2-ch44, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

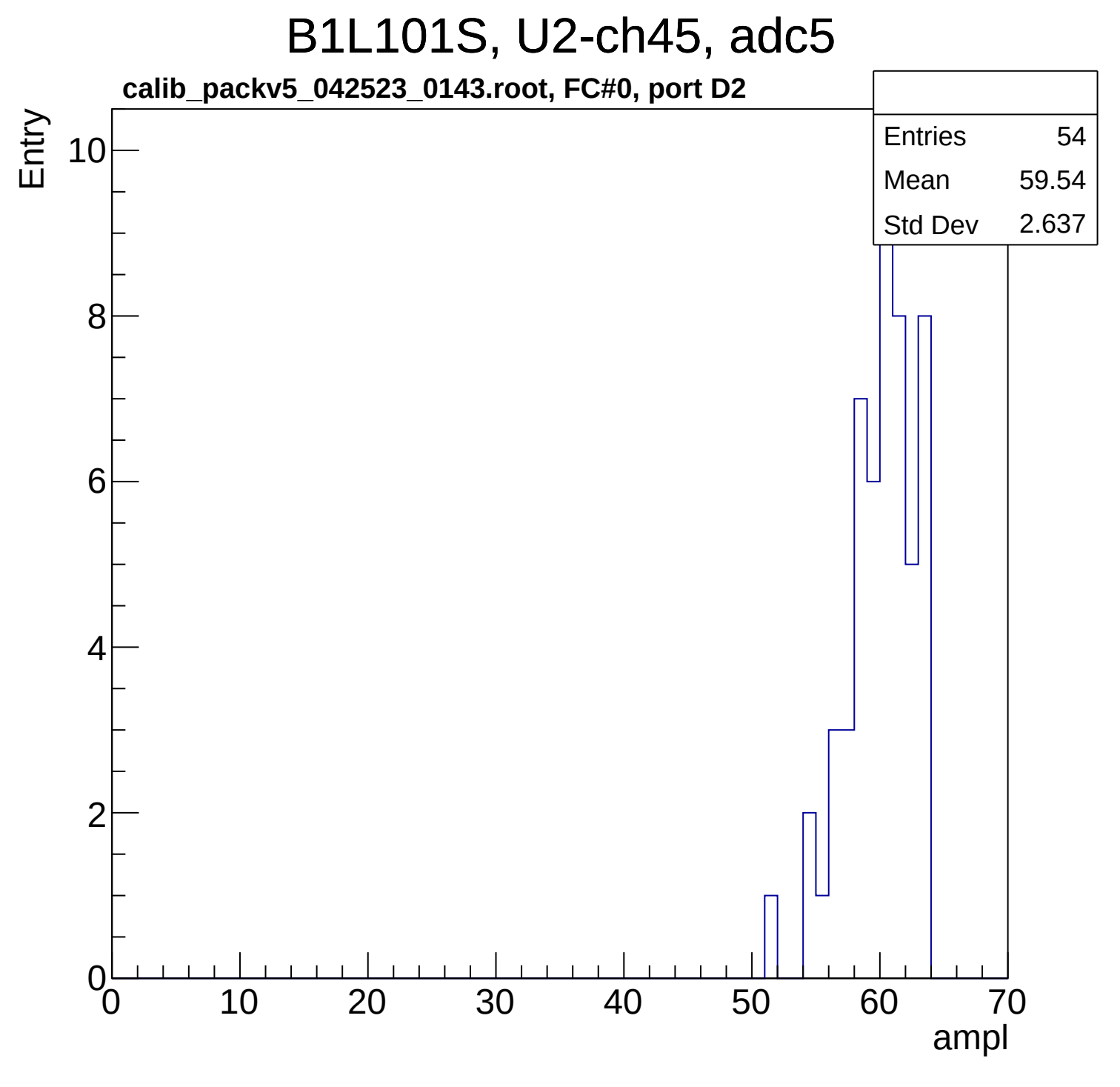

B1L101S, U2-ch45, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 26.63
Std Dev 8.287
Gaus mean : 29.3514
Gaus Width: 3.4760
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

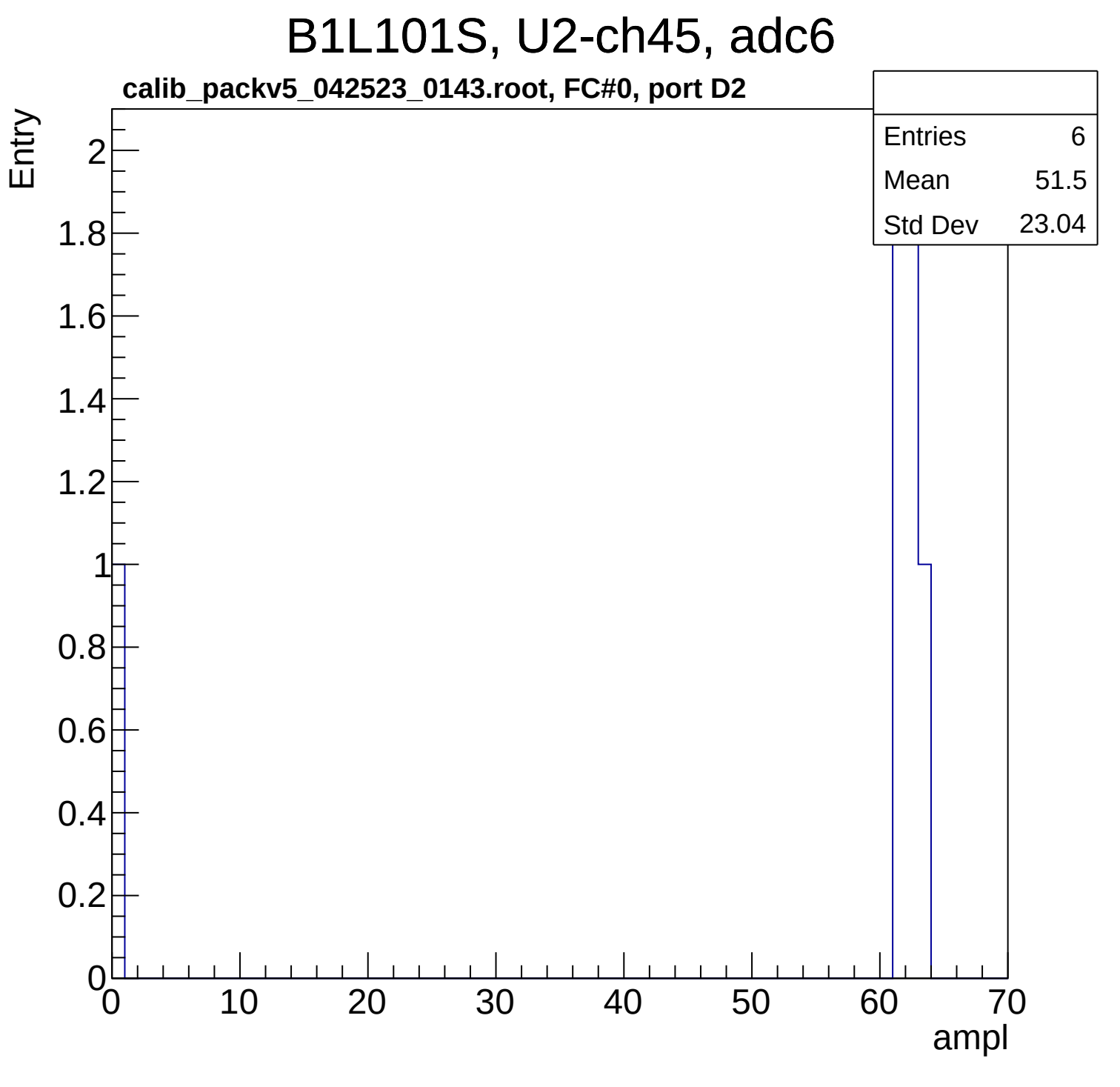

B1L101S, U2-ch45, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 35.59
Std Dev 3.657
Gaus mean : 36.2676
Gaus Width: 4.0906
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

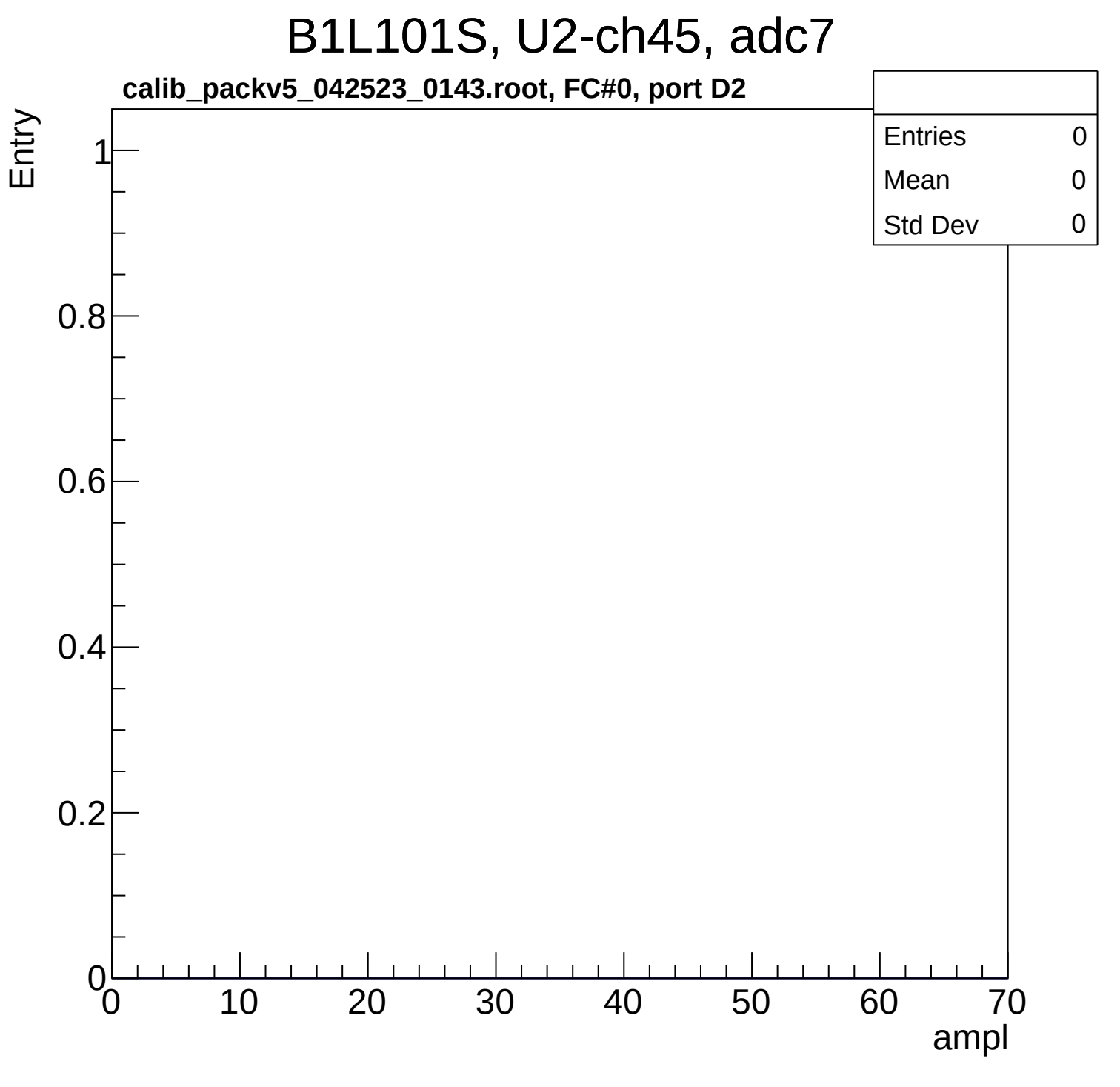

B1L101S, U2-ch45, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 42.2
Std Dev 3.589
Gaus mean : 42.2327
Gaus Width: 3.9340
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

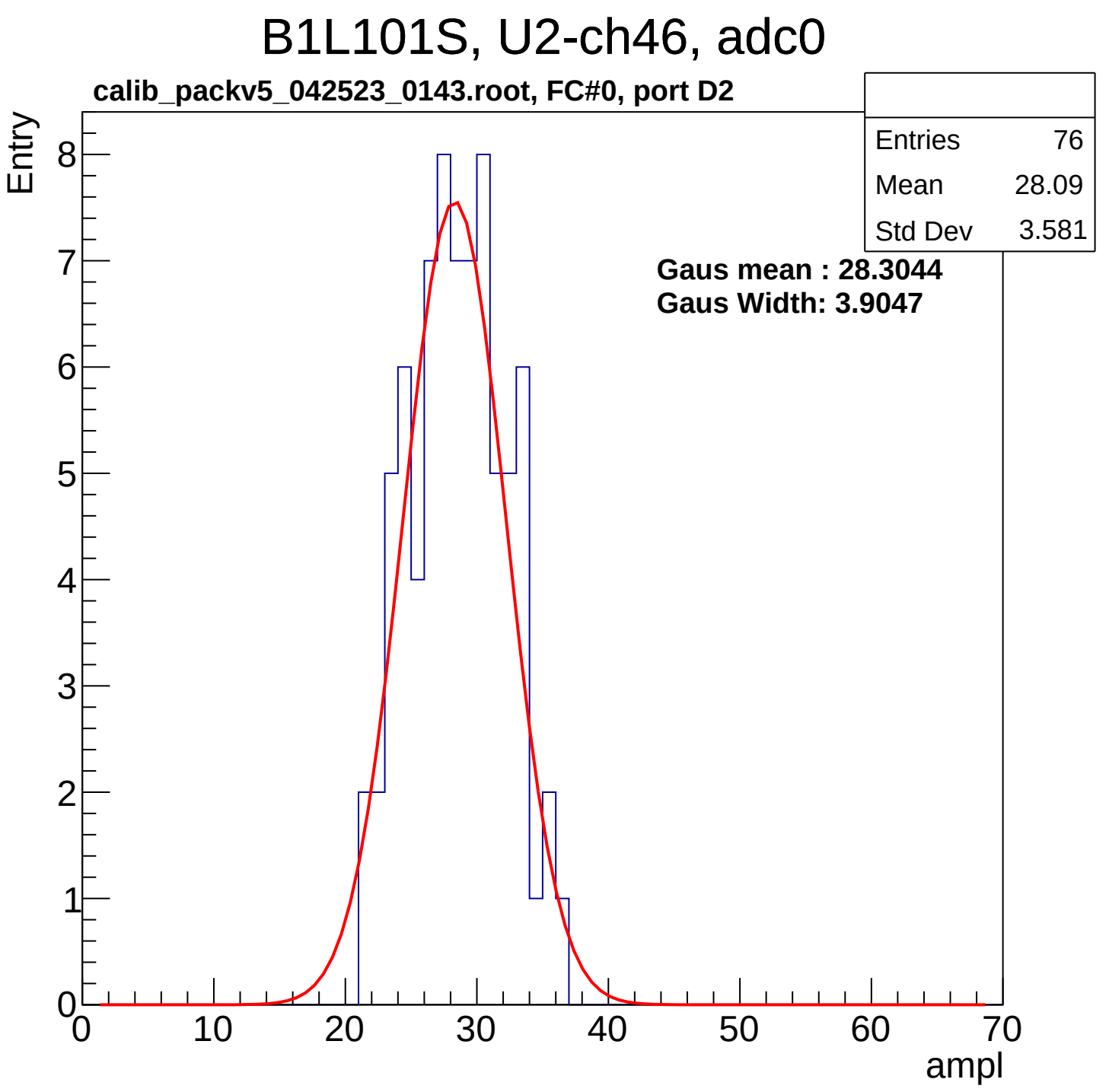

B1L101S, U2-ch45, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 81
Mean 48.7
Std Dev 3.592
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

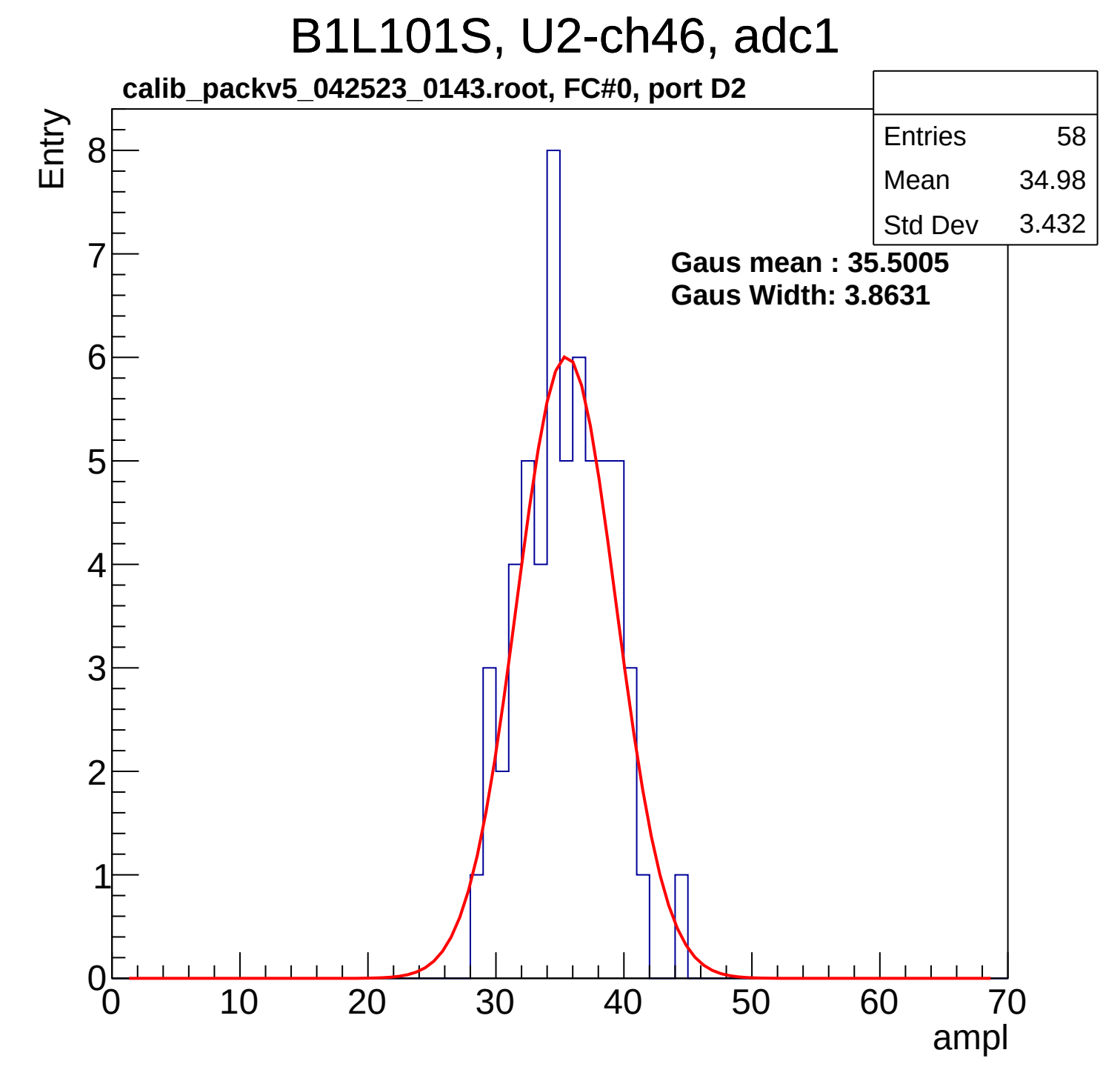

B1L101S, U2-ch45, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 55.12
Std Dev 3.679
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

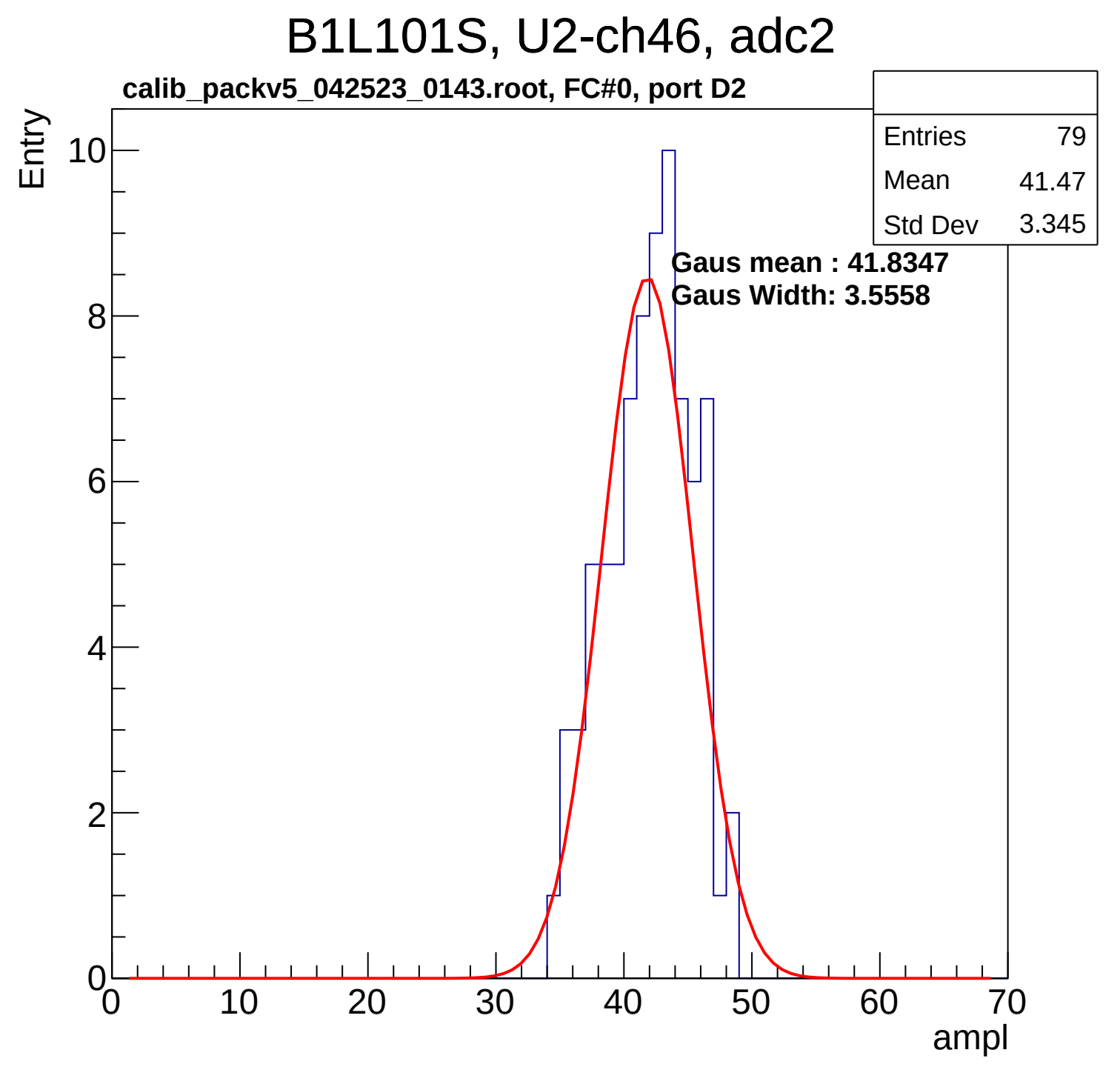

B1L101S, U2-ch45, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 59.54
Std Dev 2.637
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

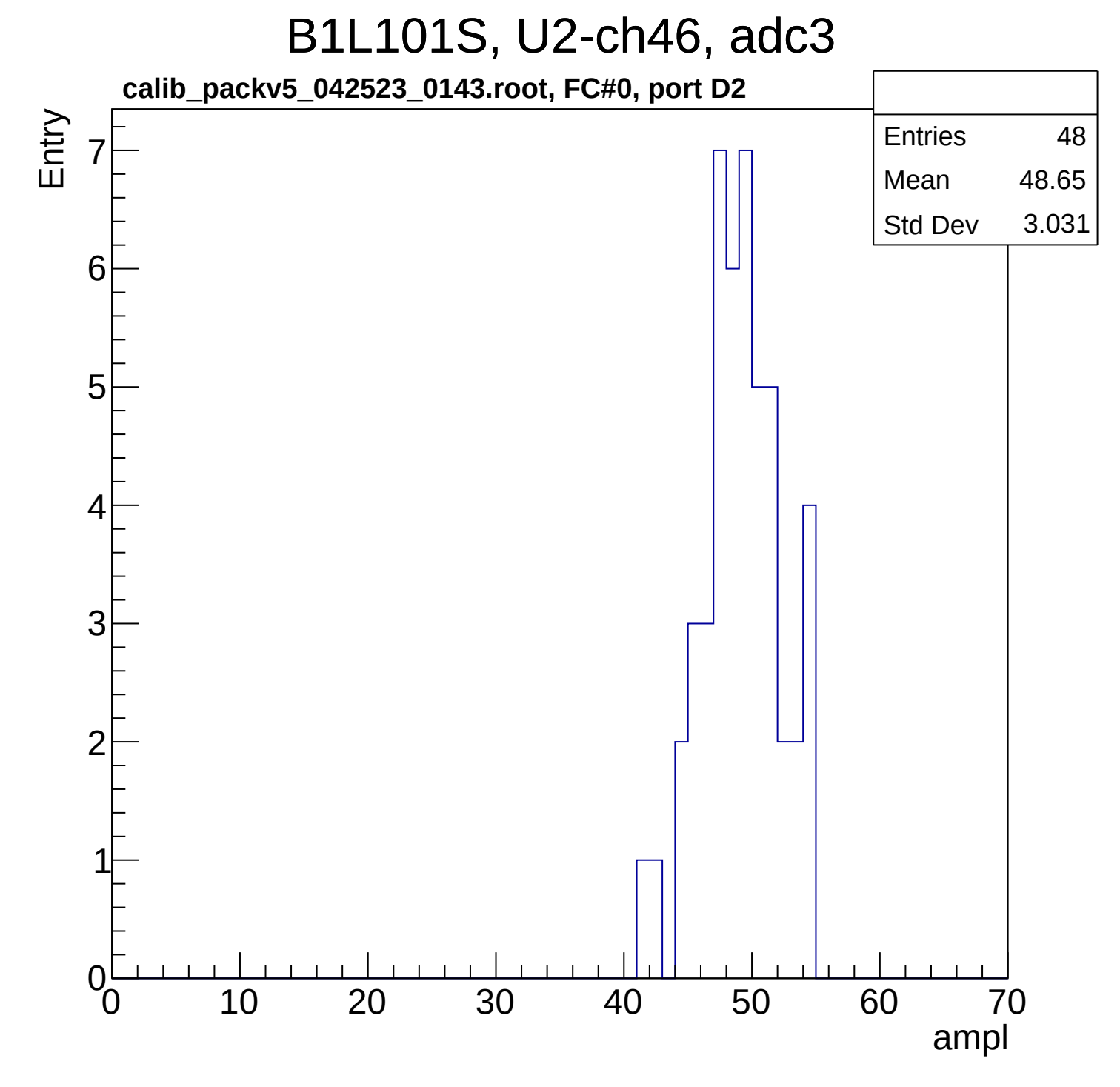

B1L101S, U2-ch45, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 51.5
Std Dev 23.04
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

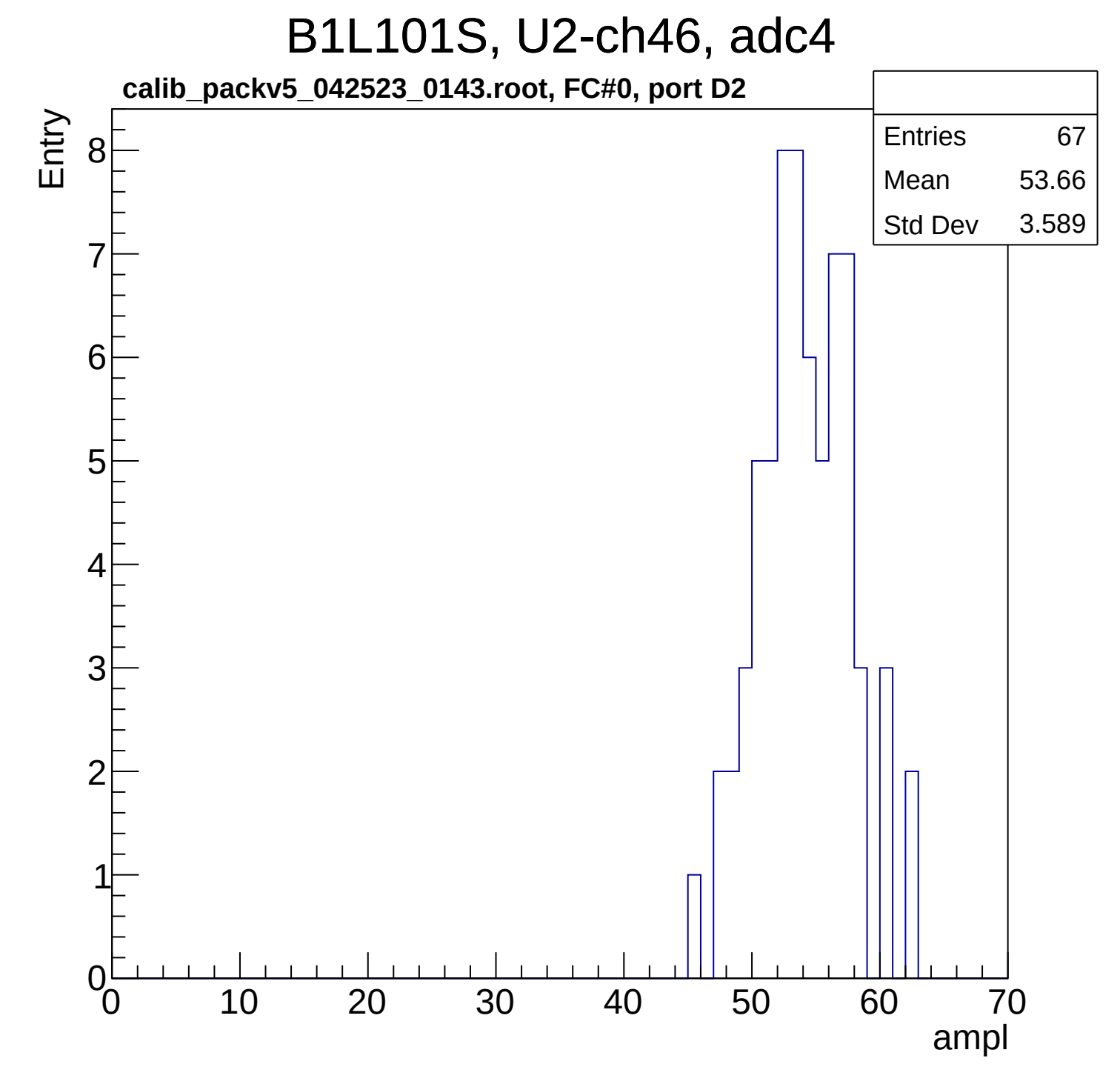

B1L101S, U2-ch45, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

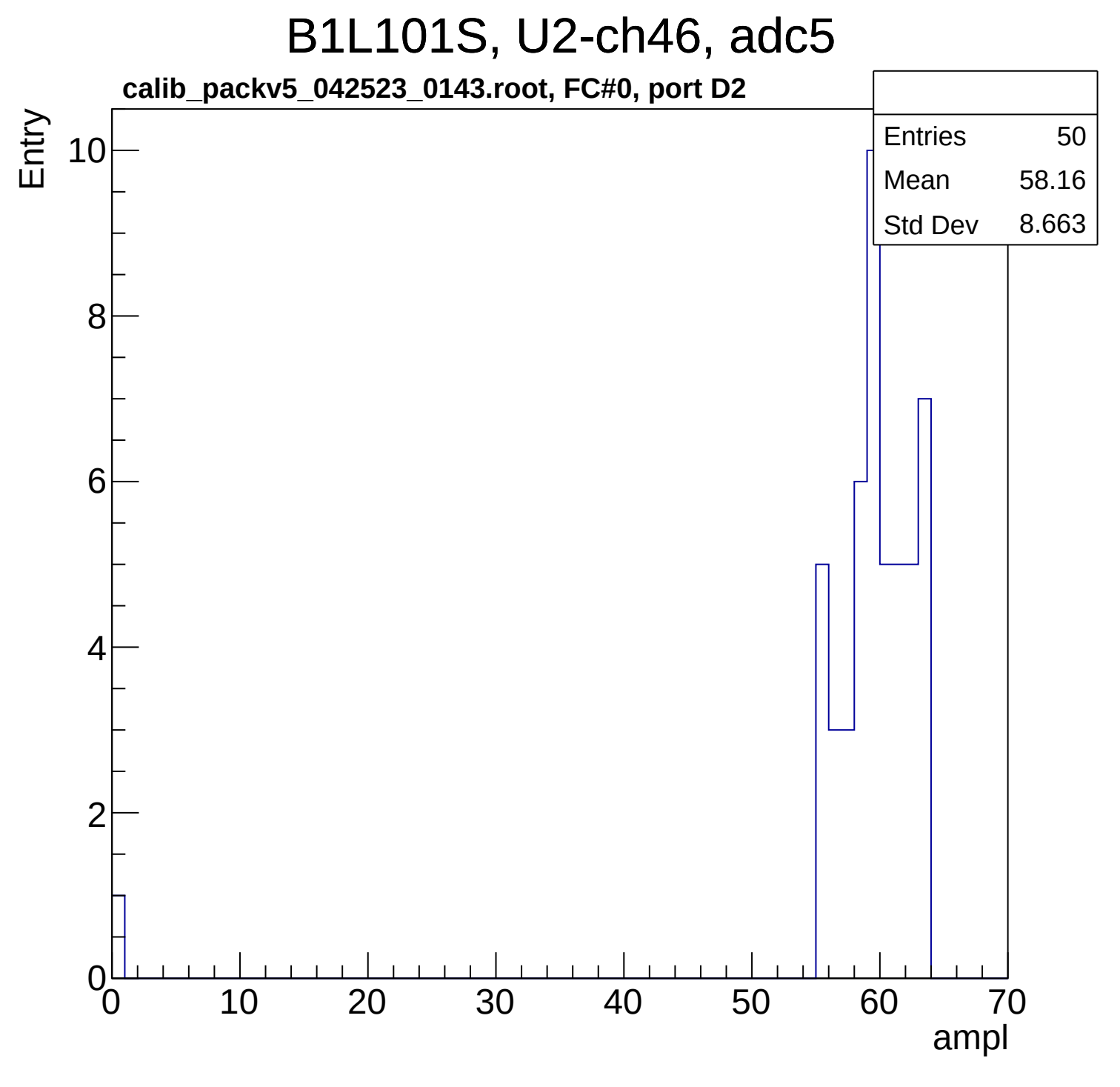

B1L101S, U2-ch46, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 28.09
Std Dev 3.581
Gaus mean : 28.3044
Gaus Width: 3.9047
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

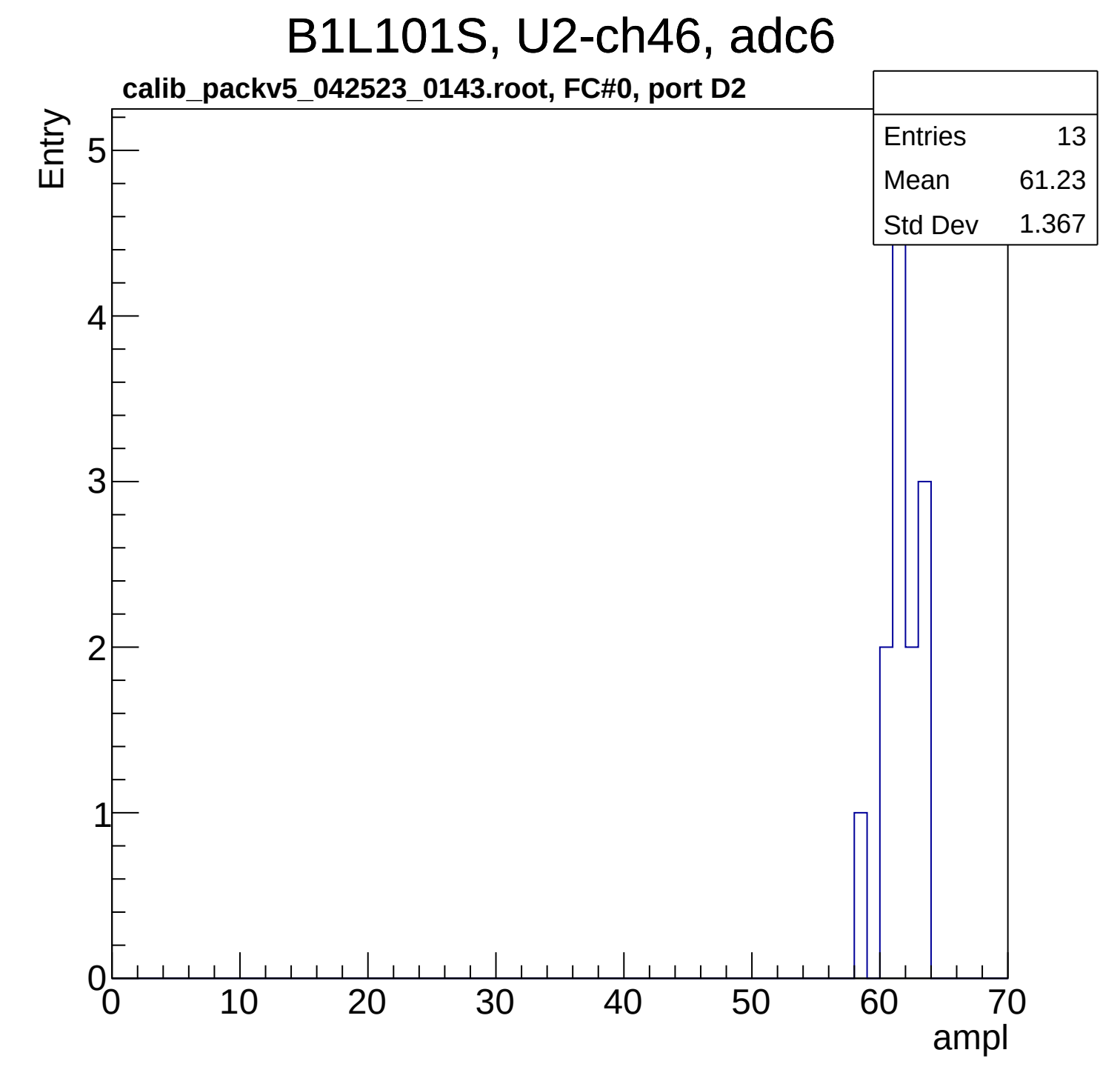

B1L101S, U2-ch46, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 34.98
Std Dev 3.432
Gaus mean : 35.5005
Gaus Width: 3.8631
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

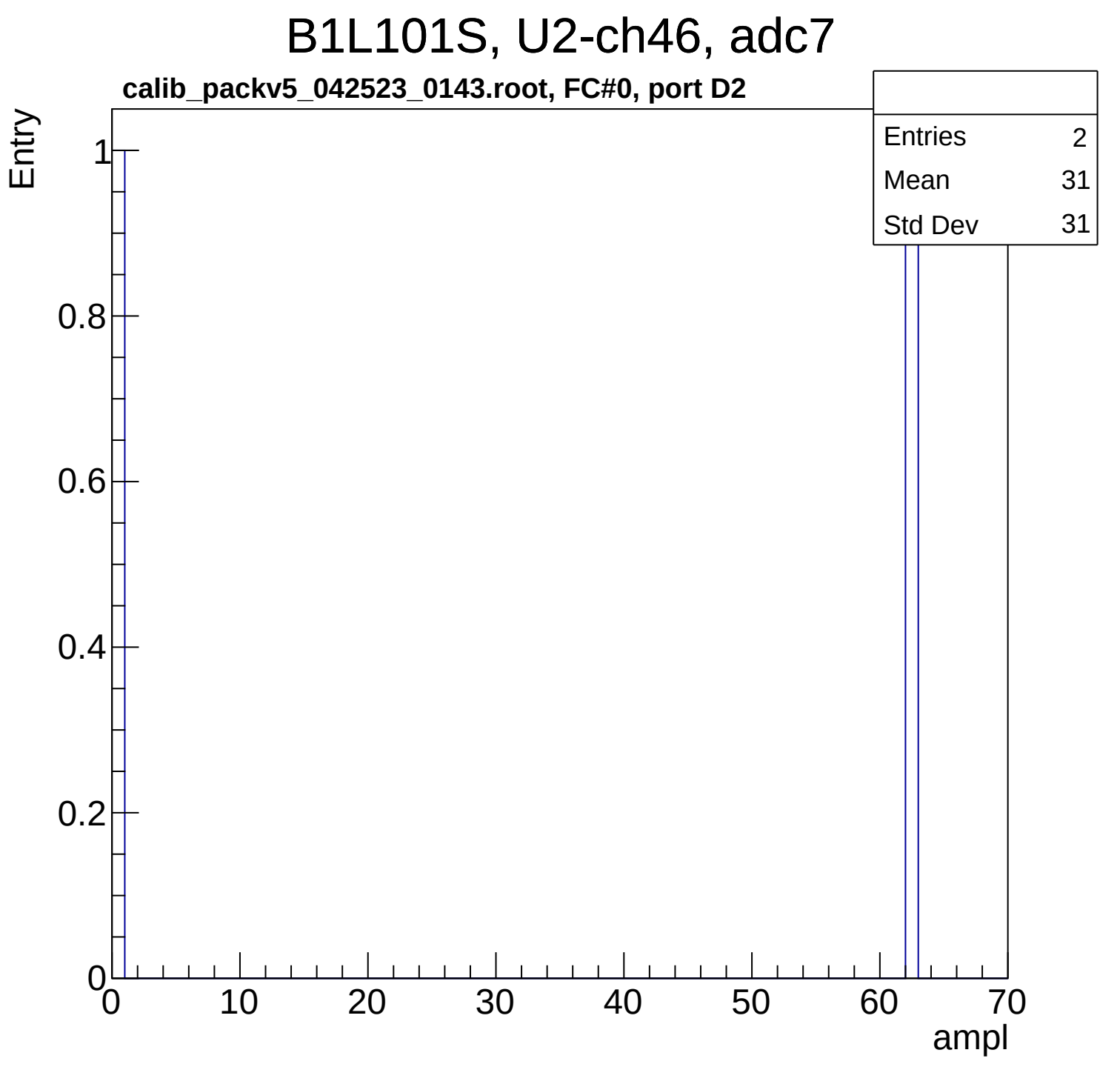

B1L101S, U2-ch46, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 41.47
Std Dev 3.345
Gaus mean : 41.8347
Gaus Width: 3.5558
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

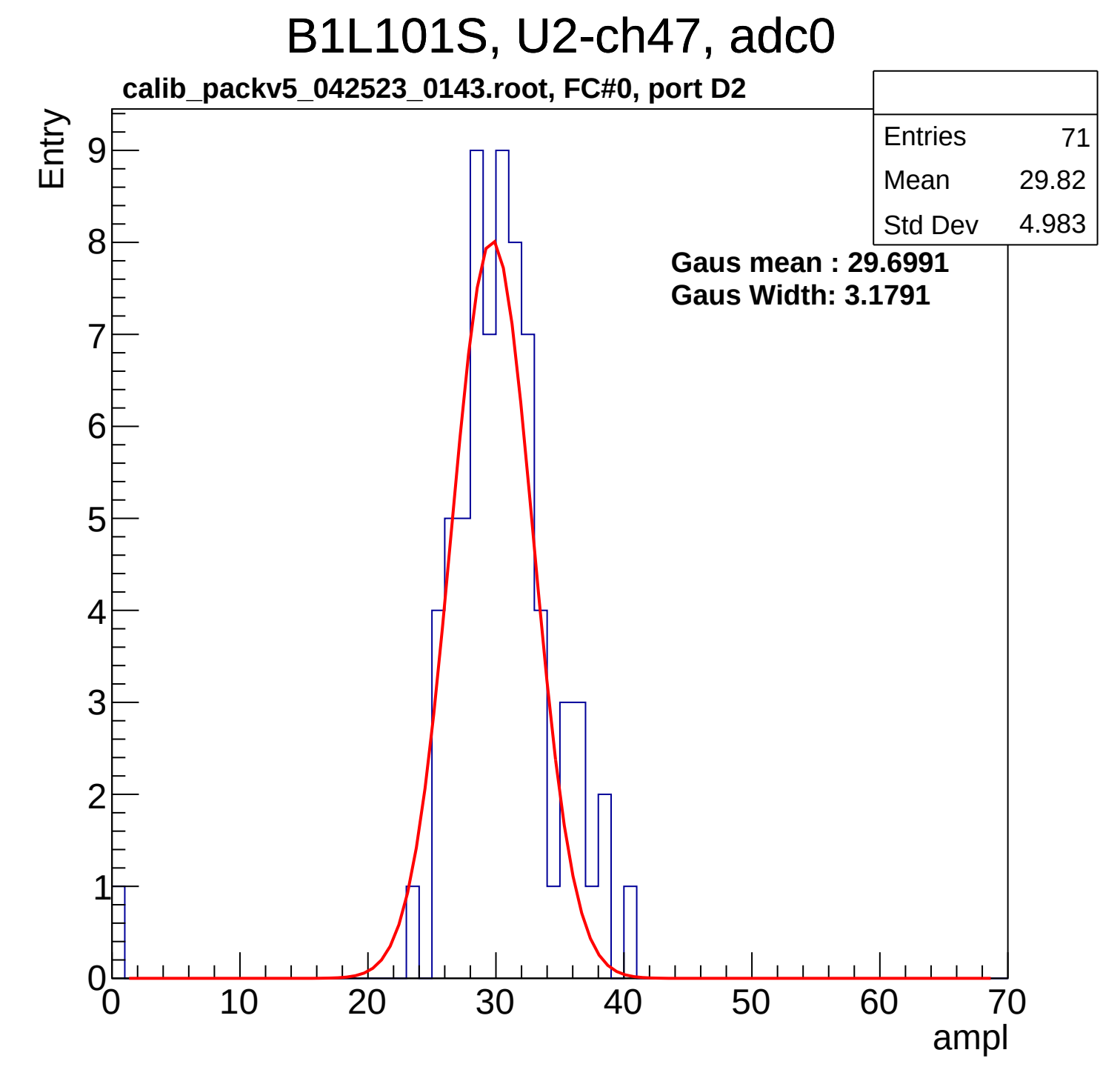

B1L101S, U2-ch46, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 48.65
Std Dev 3.031
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

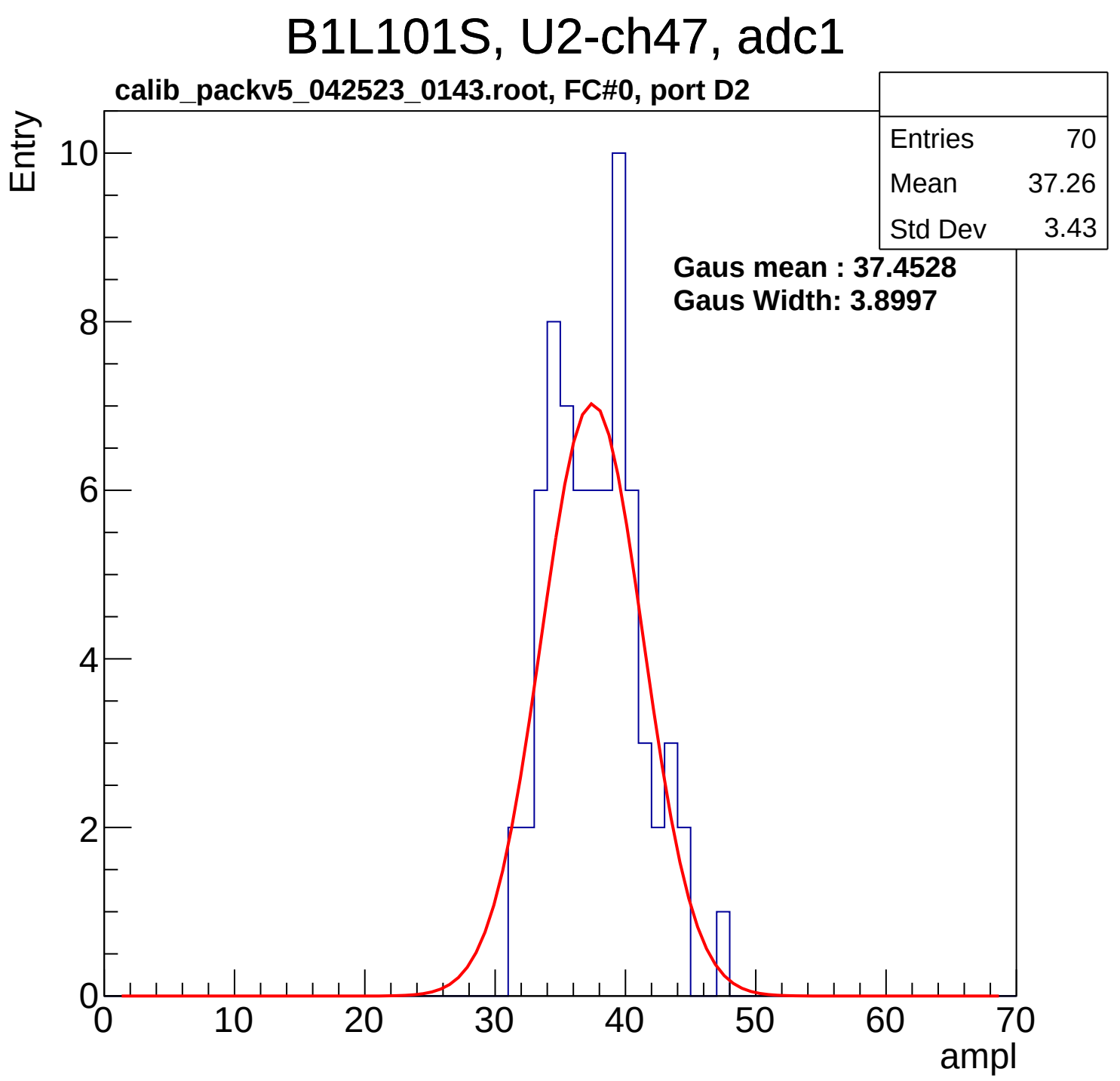

B1L101S, U2-ch46, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 53.66
Std Dev 3.589
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

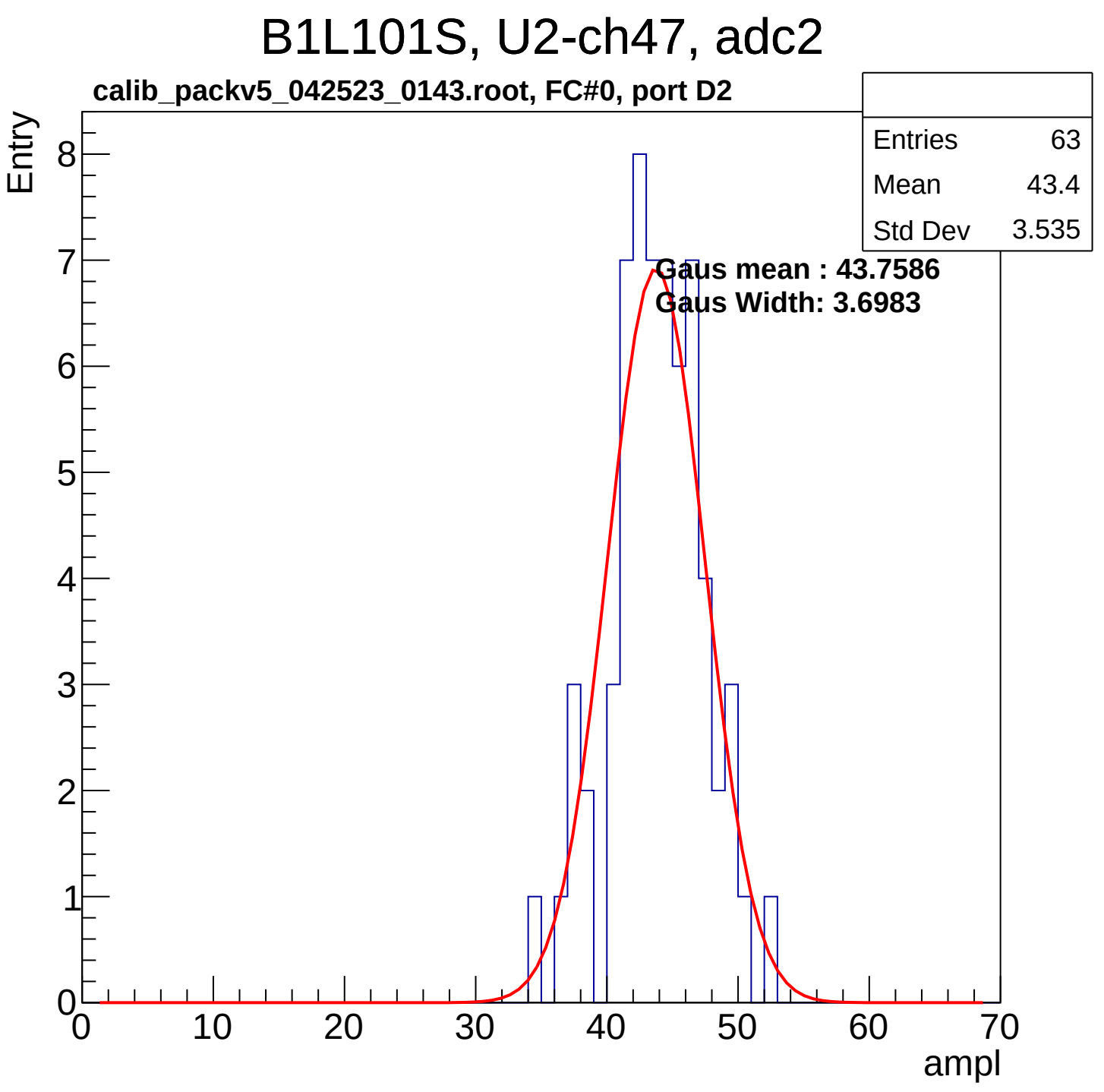

B1L101S, U2-ch46, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 58.16
Std Dev 8.663
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

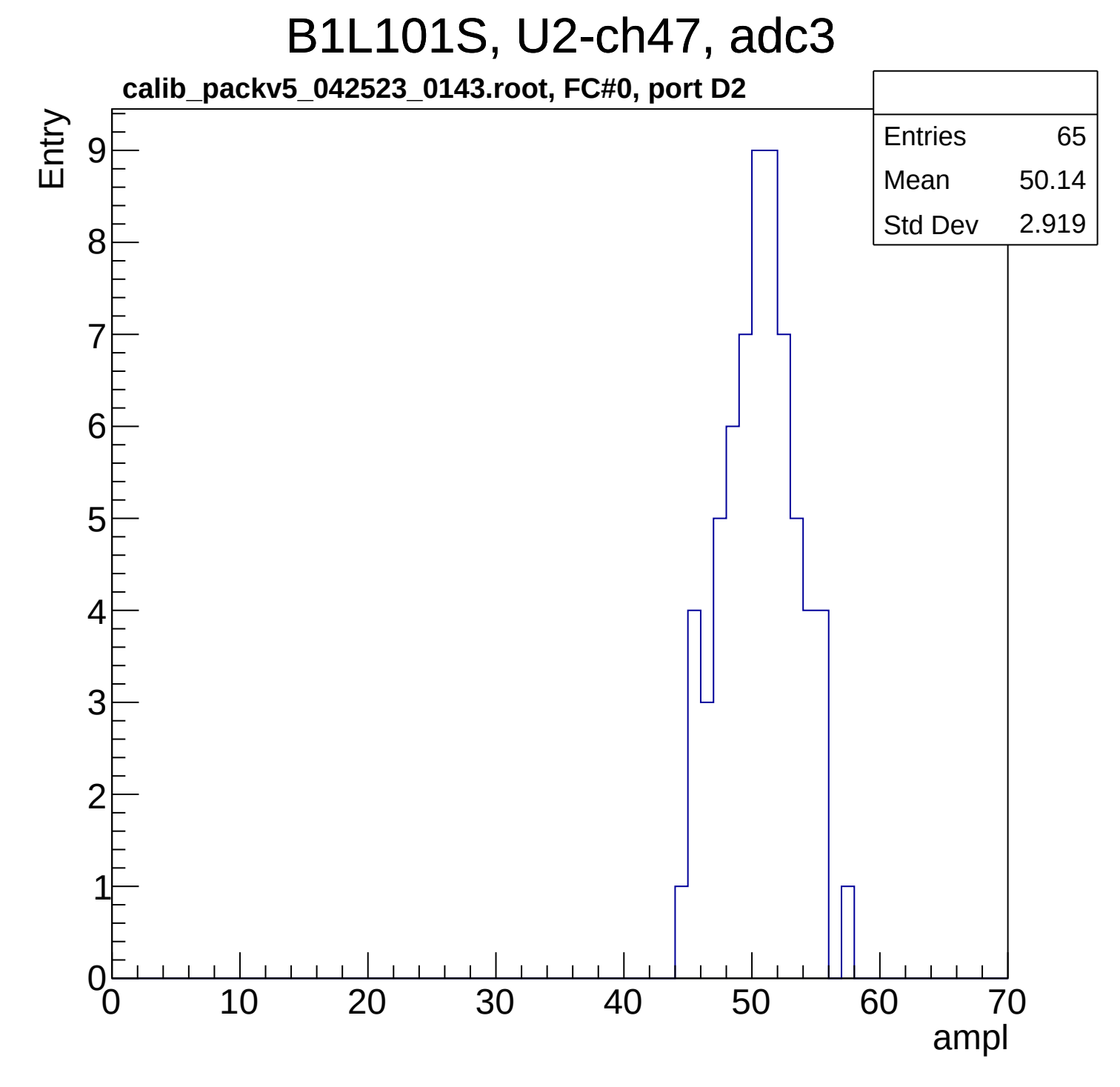

B1L101S, U2-ch46, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 13
Mean 61.23
Std Dev 1.367
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

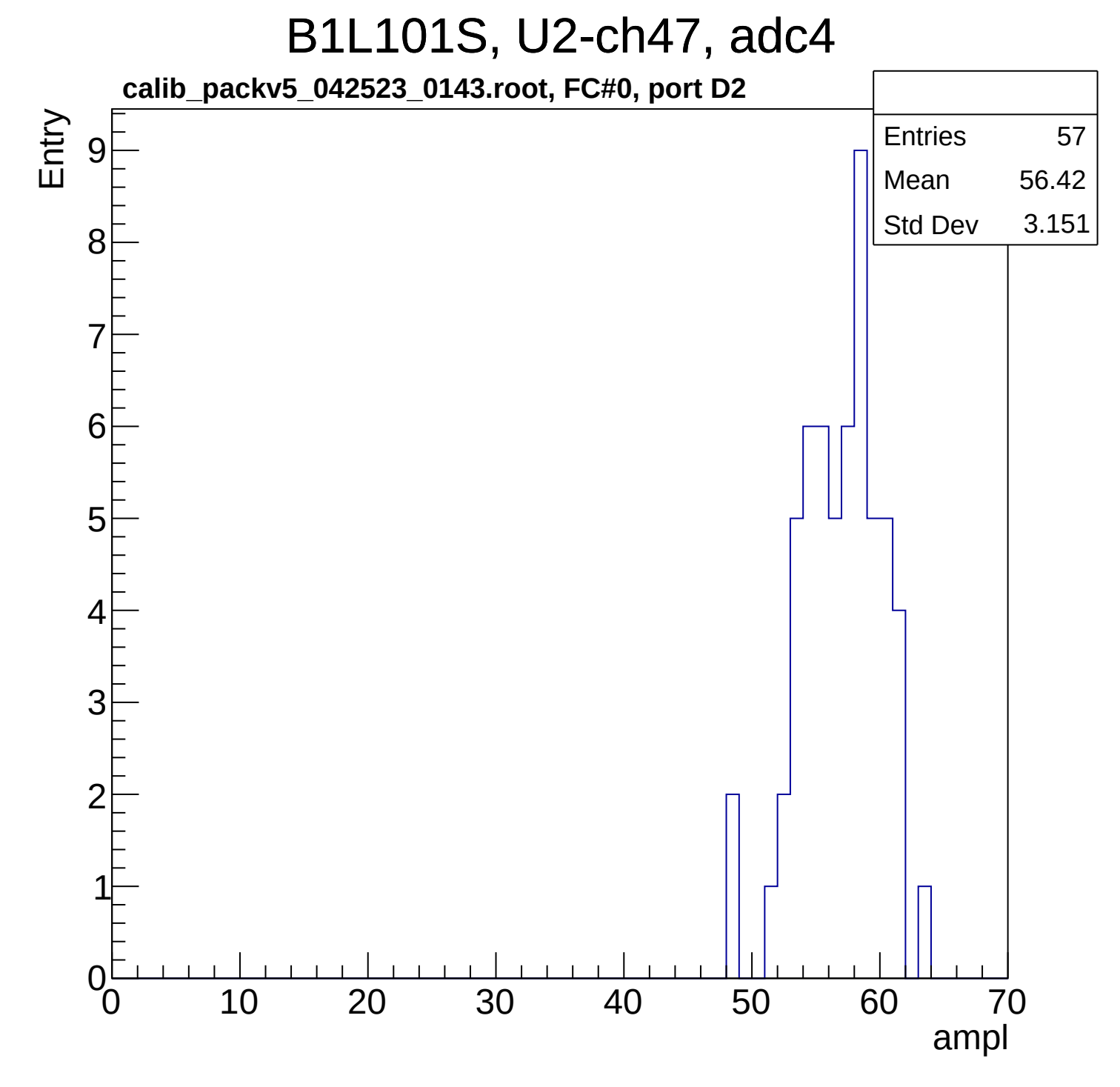

B1L101S, U2-ch46, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 31
Std Dev 31
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

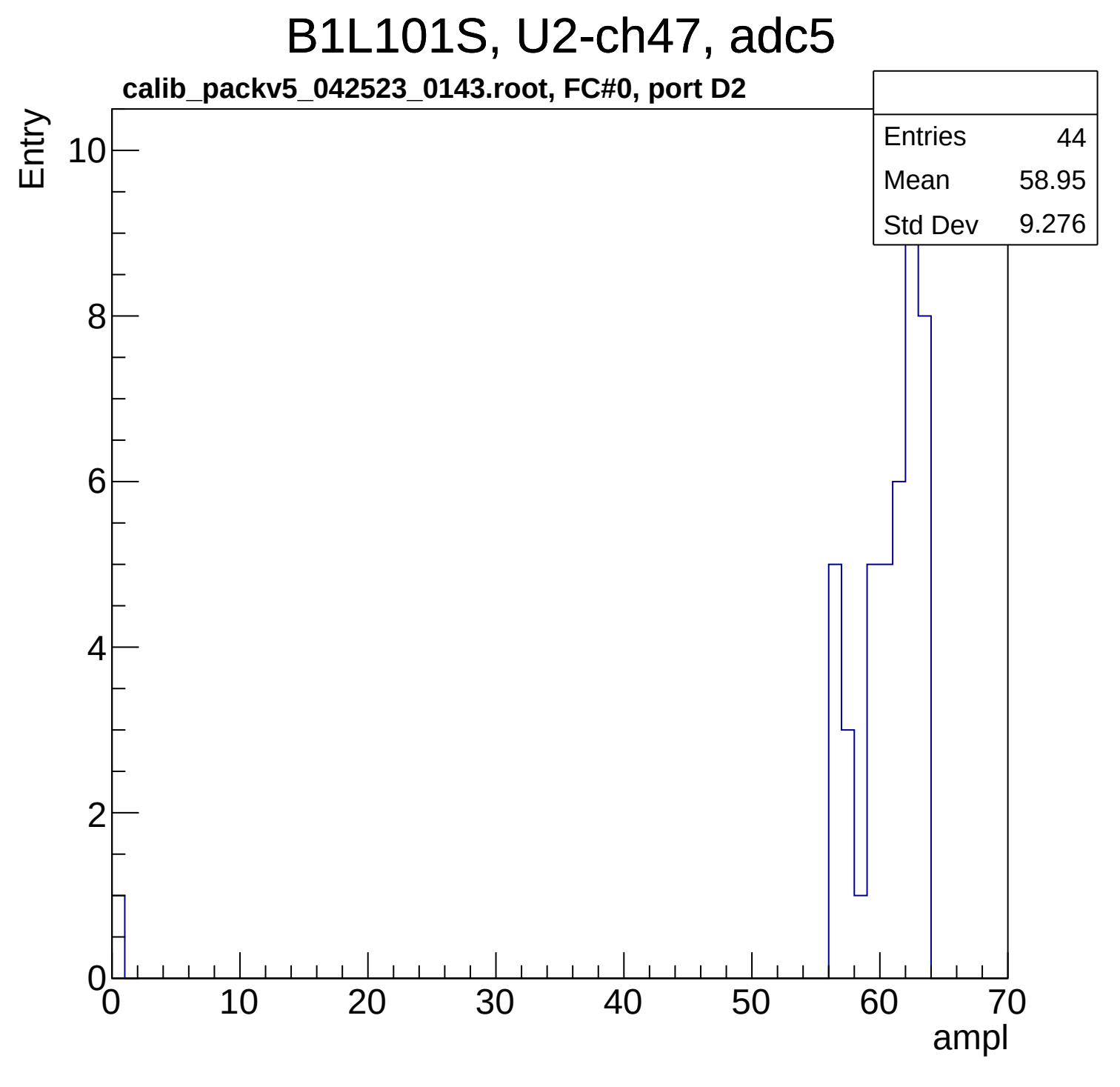

B1L101S, U2-ch47, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 29.82
Std Dev 4.983
Gaus mean : 29.6991
Gaus Width: 3.1791
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

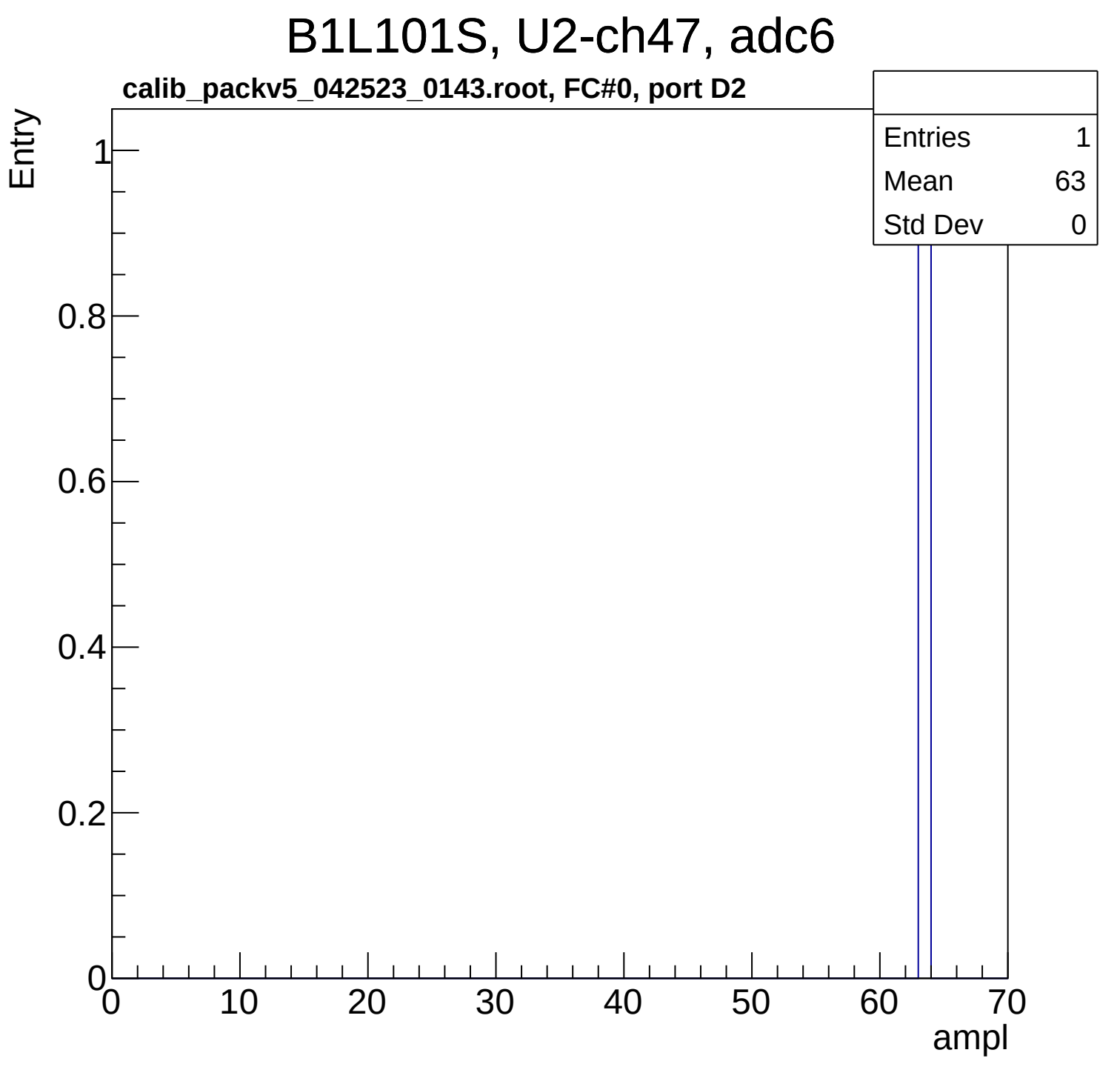

B1L101S, U2-ch47, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 37.26
Std Dev 3.43
Gaus mean : 37.4528
Gaus Width: 3.8997
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

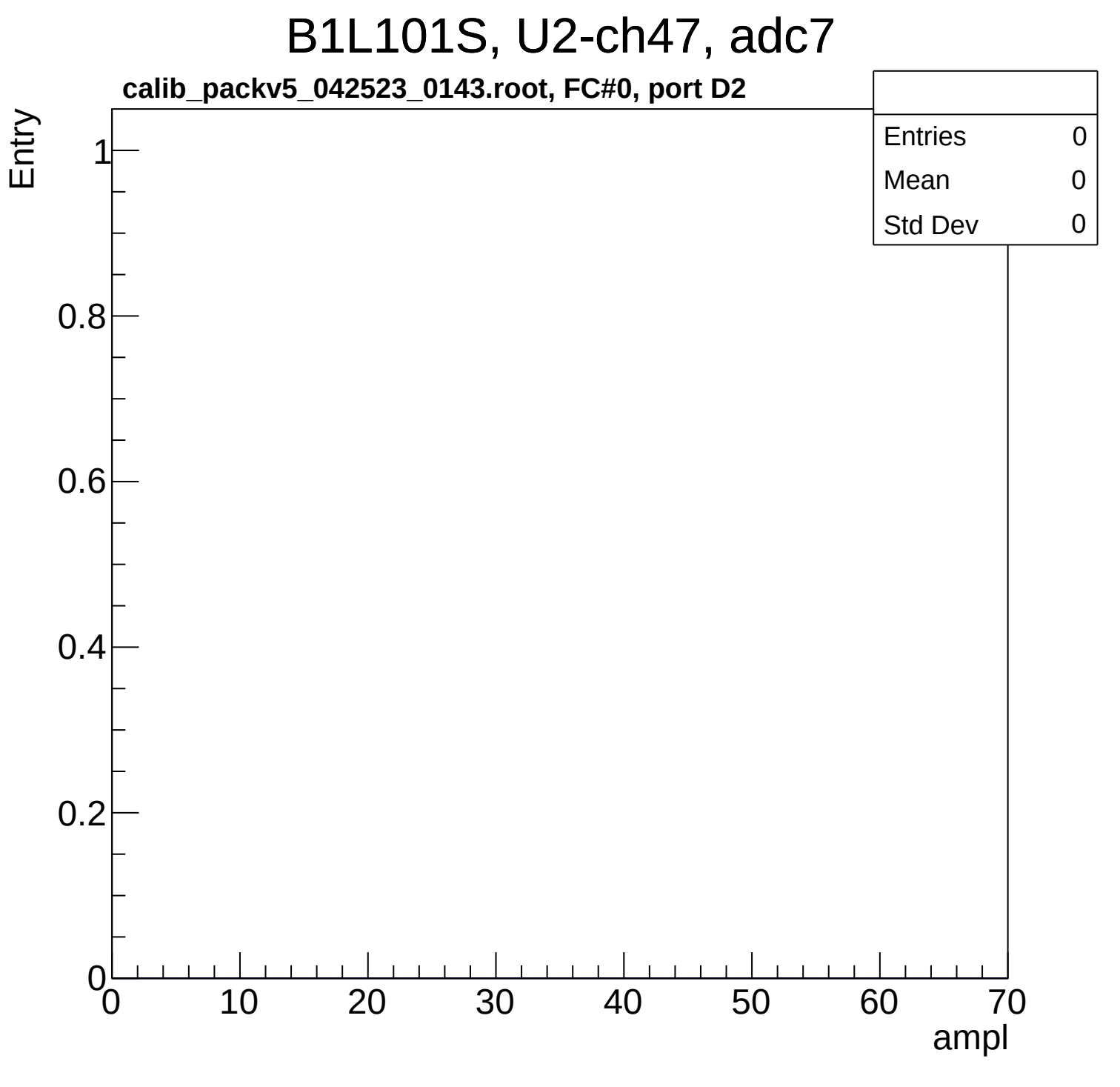

B1L101S, U2-ch47, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 43.4
Std Dev 3.535
Gaus mean : 43.7586
Gaus Width: 3.6983
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

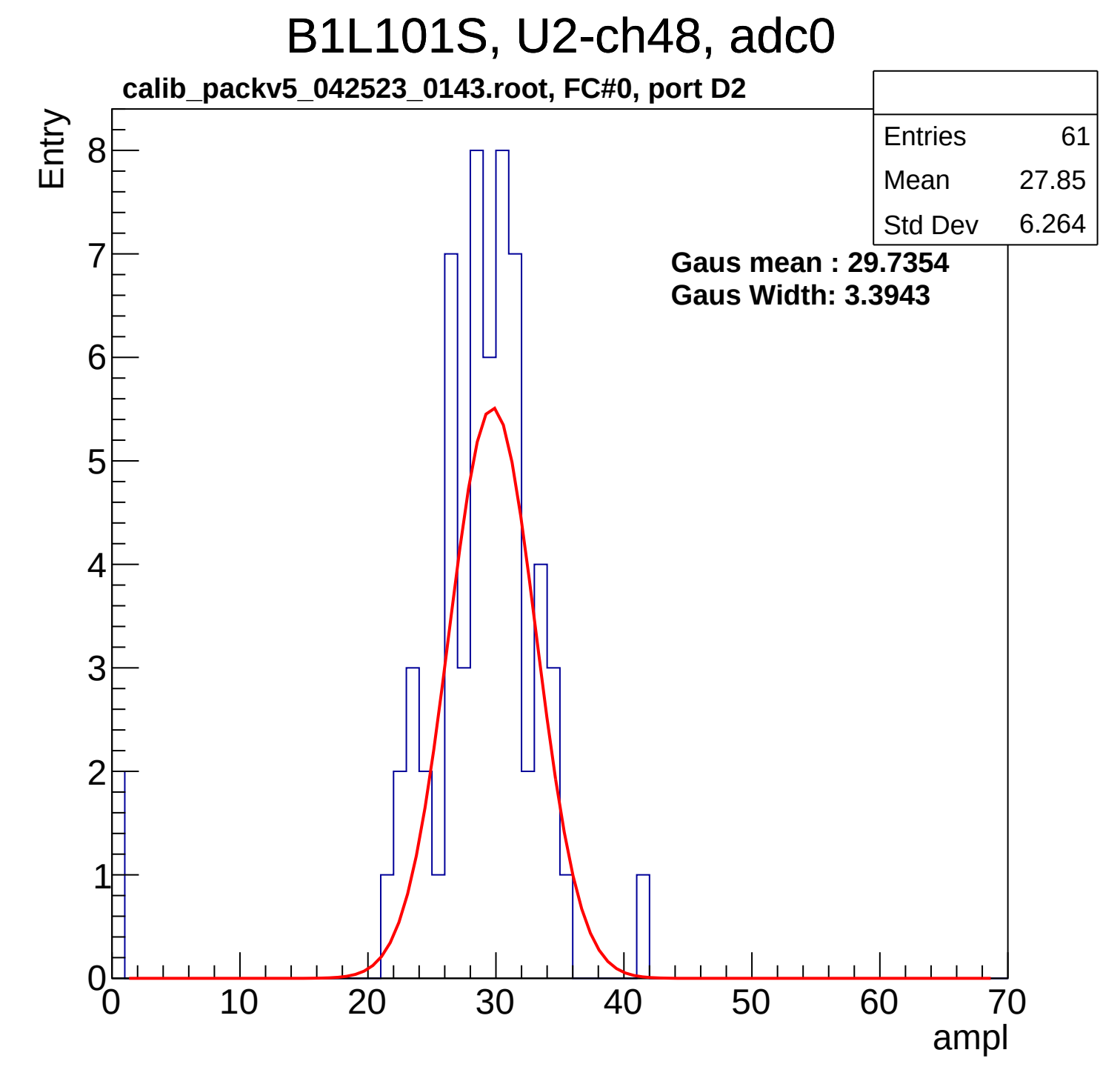

B1L101S, U2-ch47, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 50.14
Std Dev 2.919
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

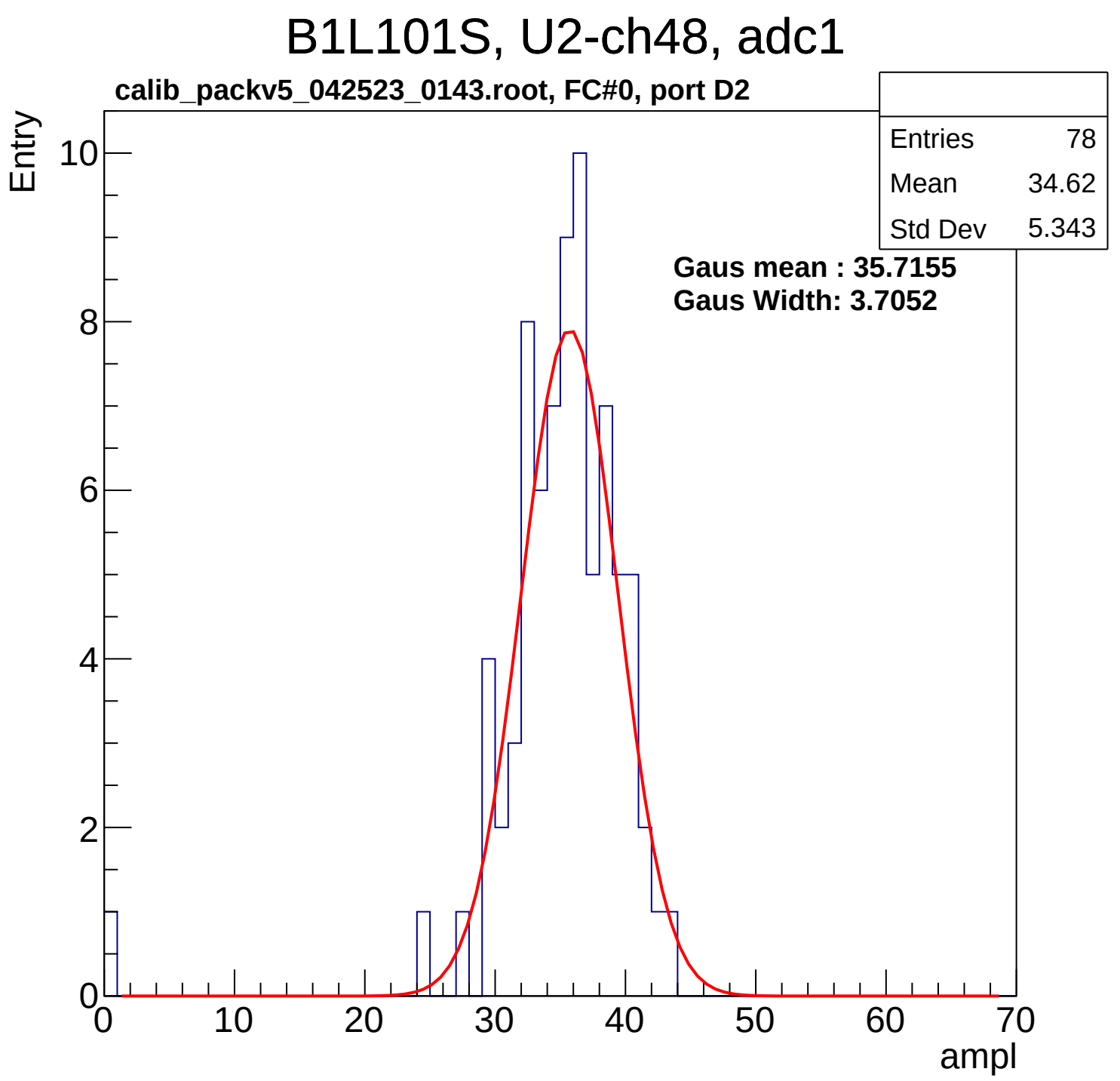

B1L101S, U2-ch47, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 56.42
Std Dev 3.151
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

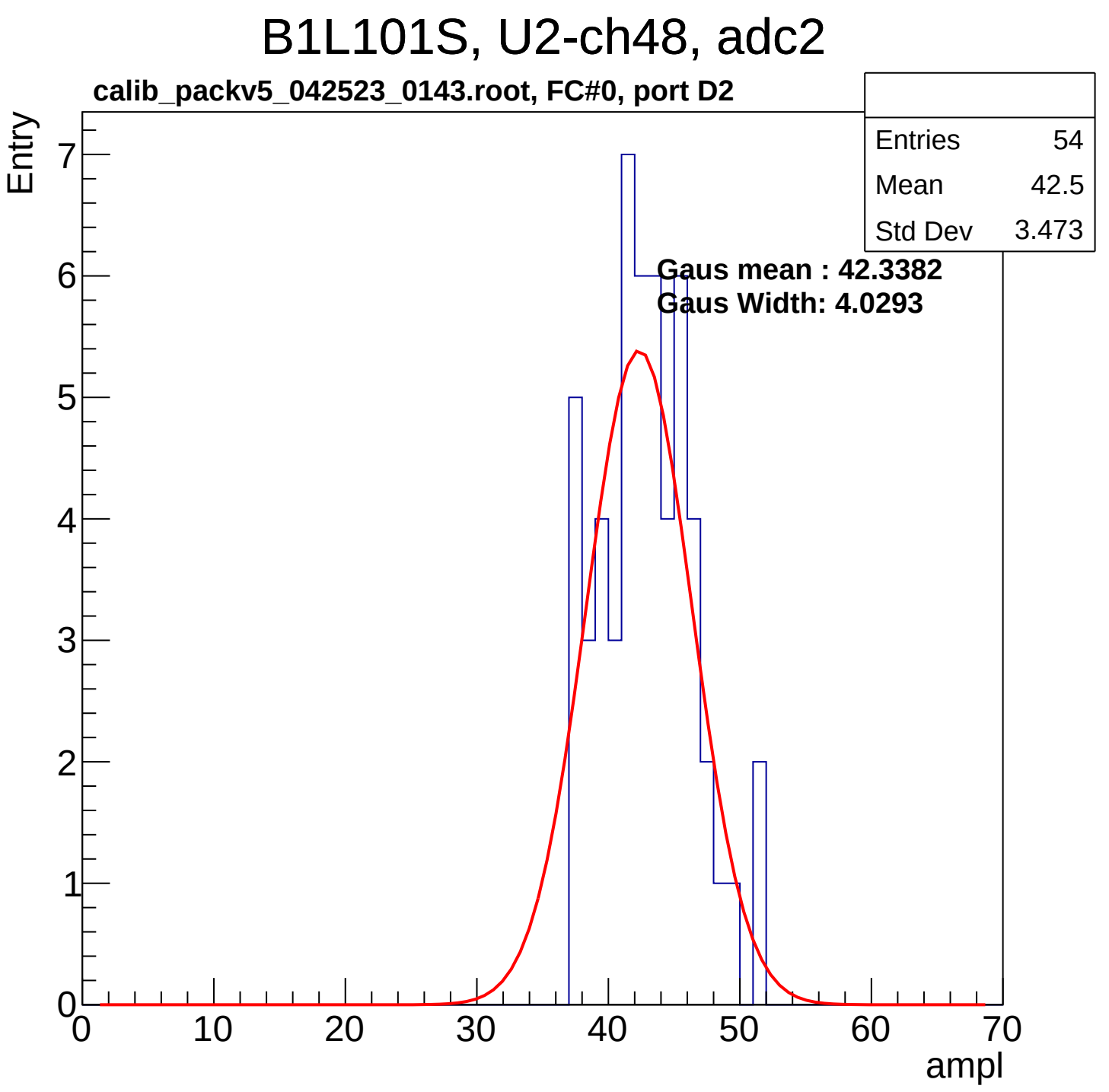

B1L101S, U2-ch47, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 44
Mean 58.95
Std Dev 9.276
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

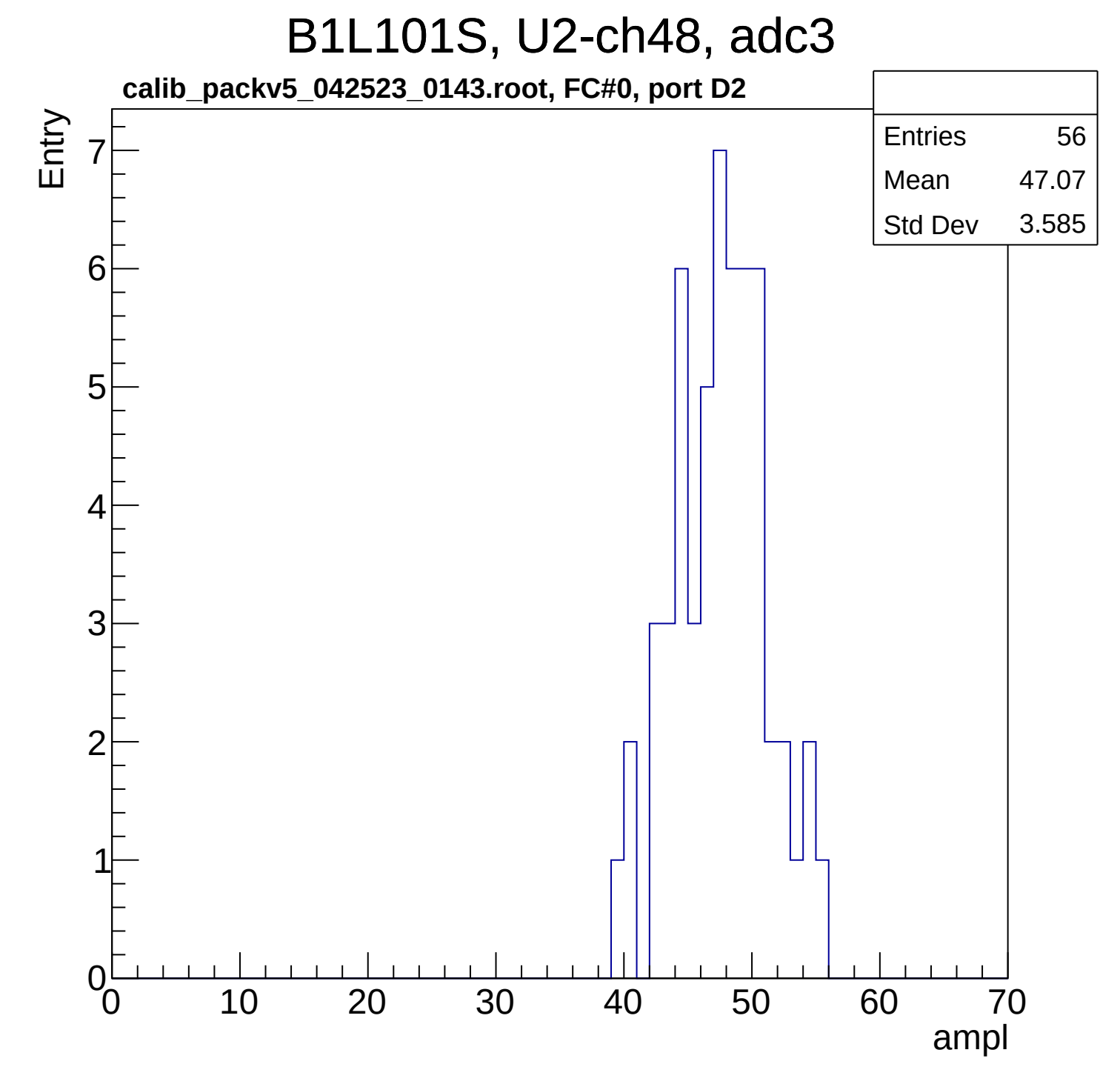

B1L101S, U2-ch47, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

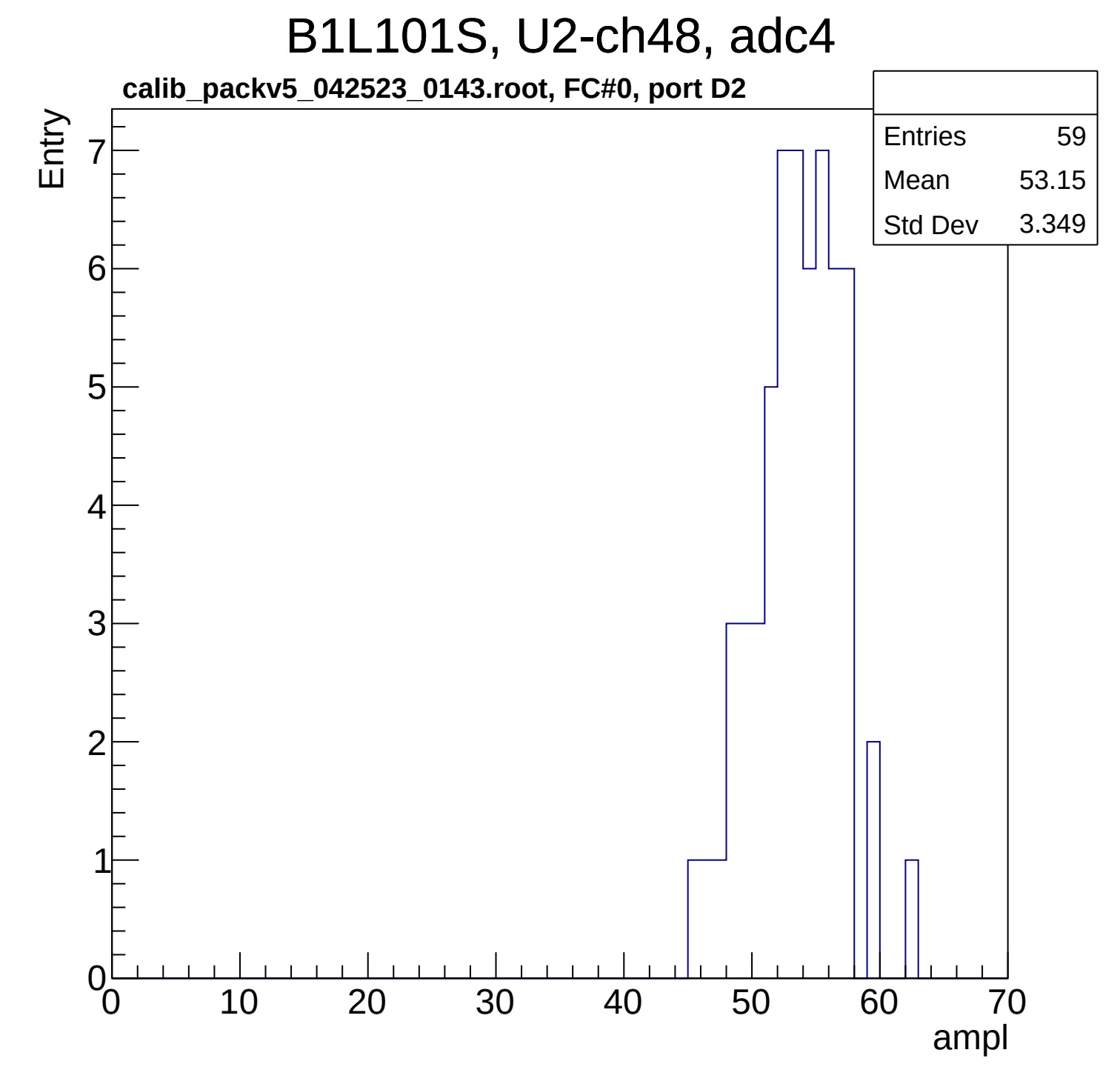

B1L101S, U2-ch47, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

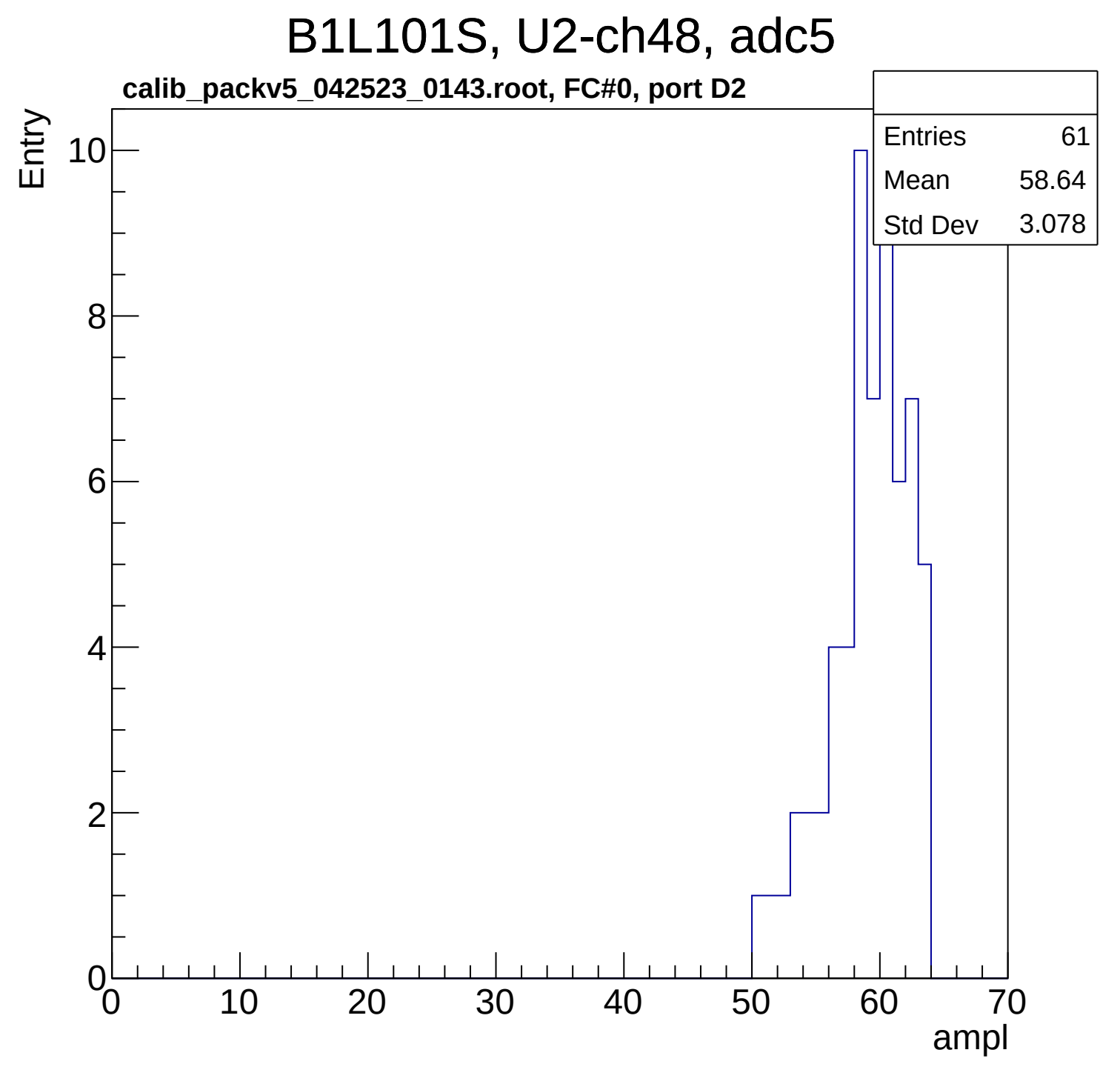

B1L101S, U2-ch48, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 27.85
Std Dev 6.264
Gaus mean : 29.7354
Gaus Width: 3.3943
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

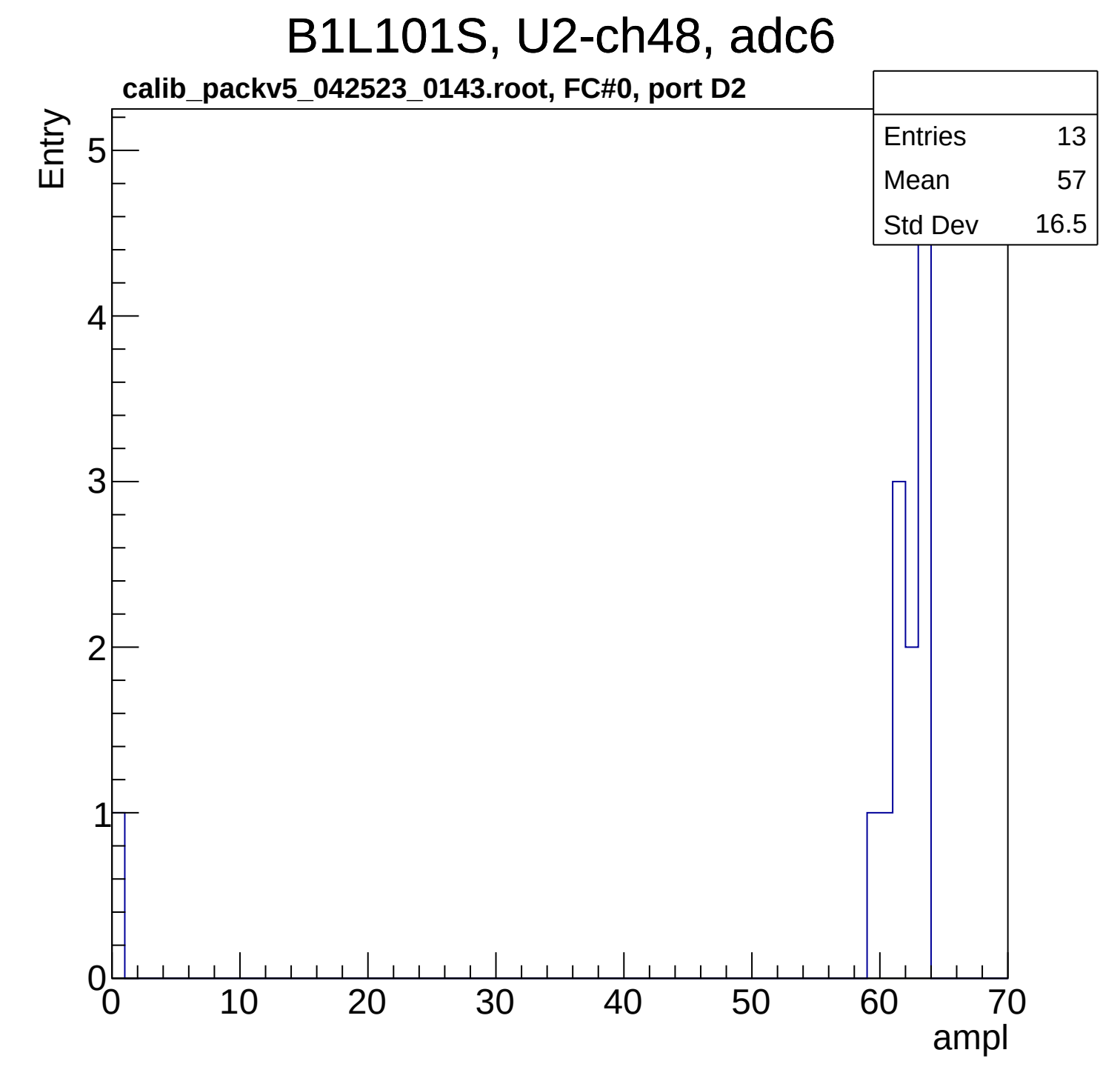

B1L101S, U2-ch48, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 34.62
Std Dev 5.343
Gaus mean : 35.7155
Gaus Width: 3.7052
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

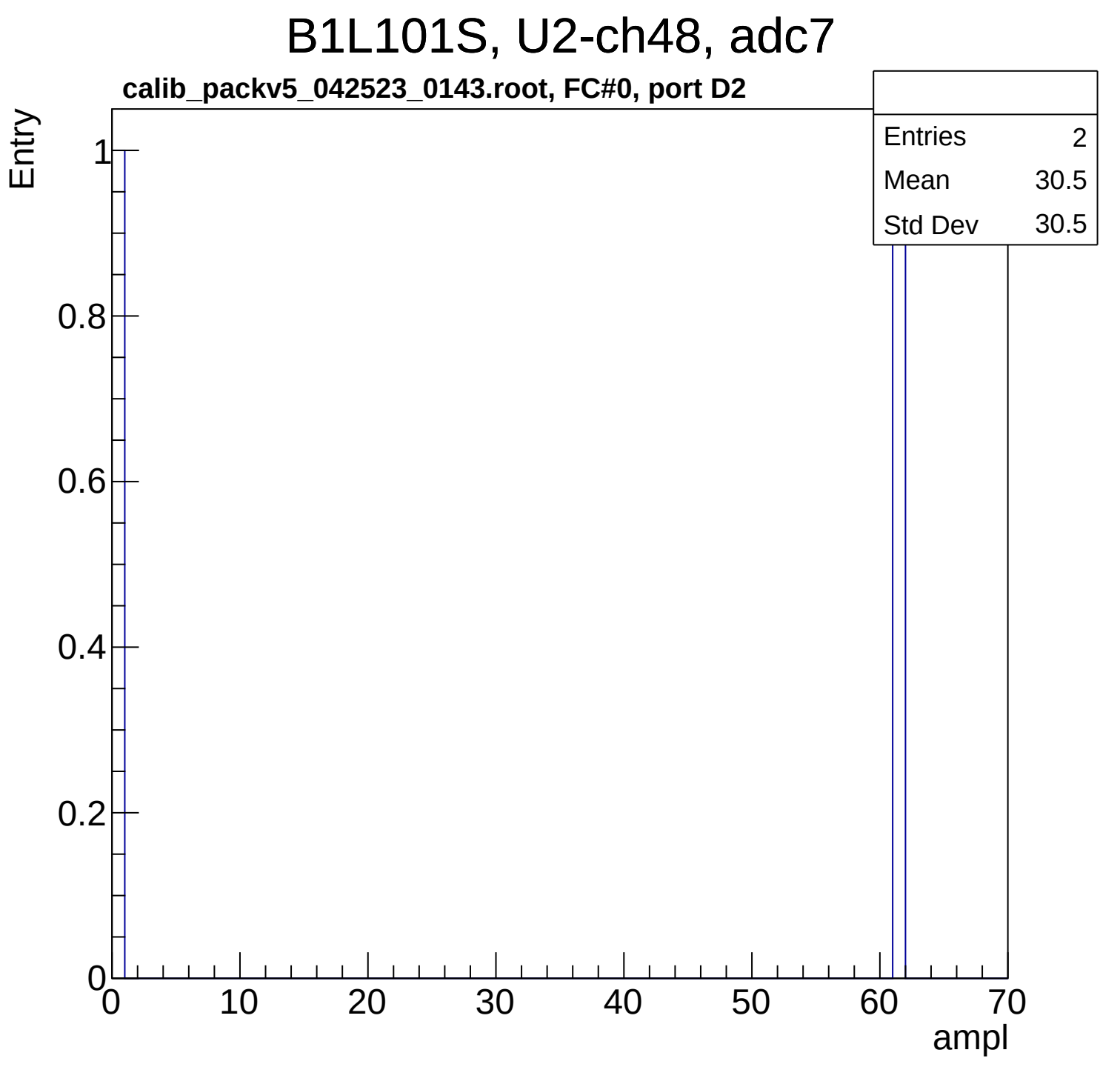

B1L101S, U2-ch48, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 42.5
Std Dev 3.473
Gaus mean : 42.3382
Gaus Width: 4.0293
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

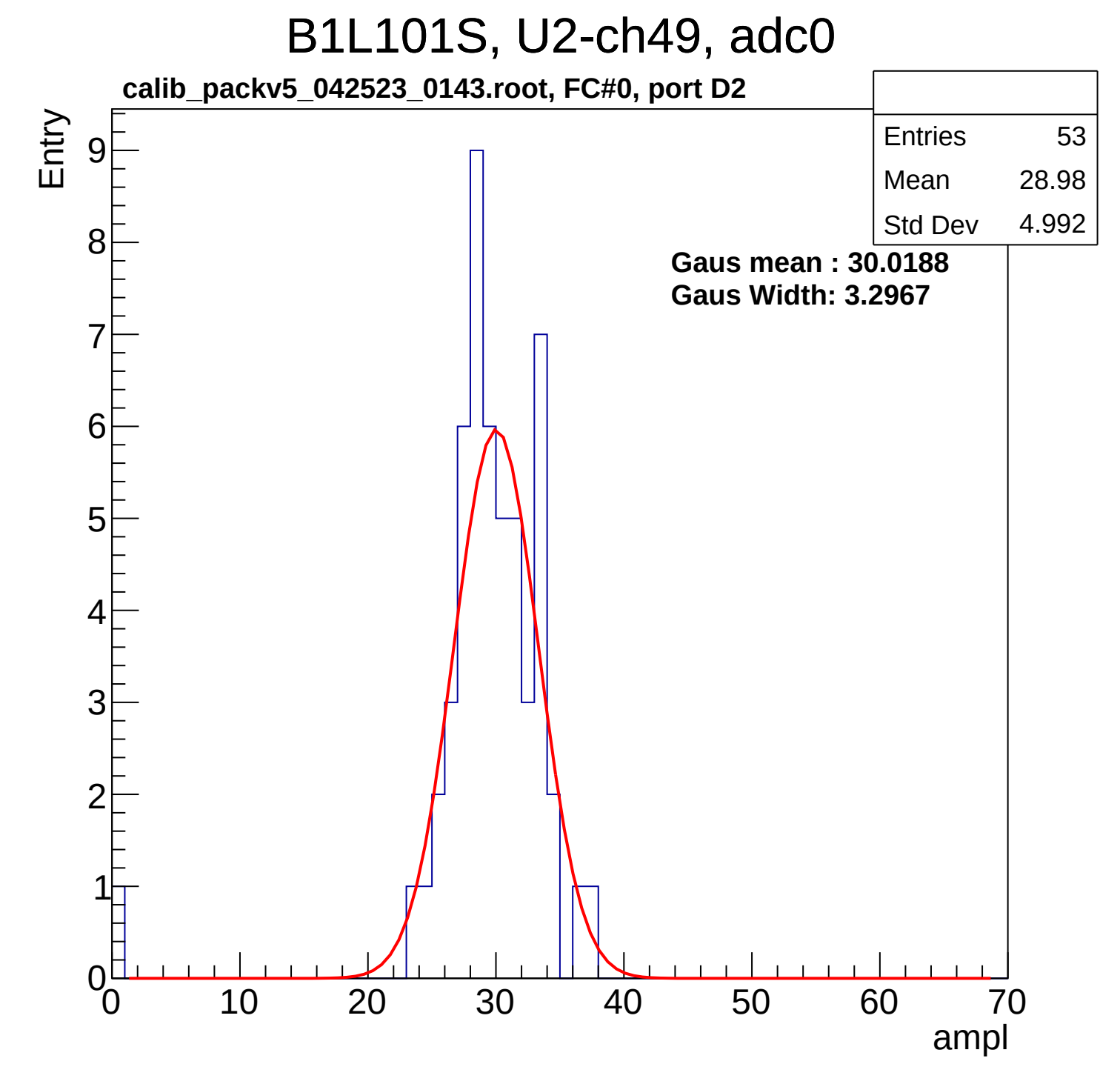

B1L101S, U2-ch48, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 47.07
Std Dev 3.585
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

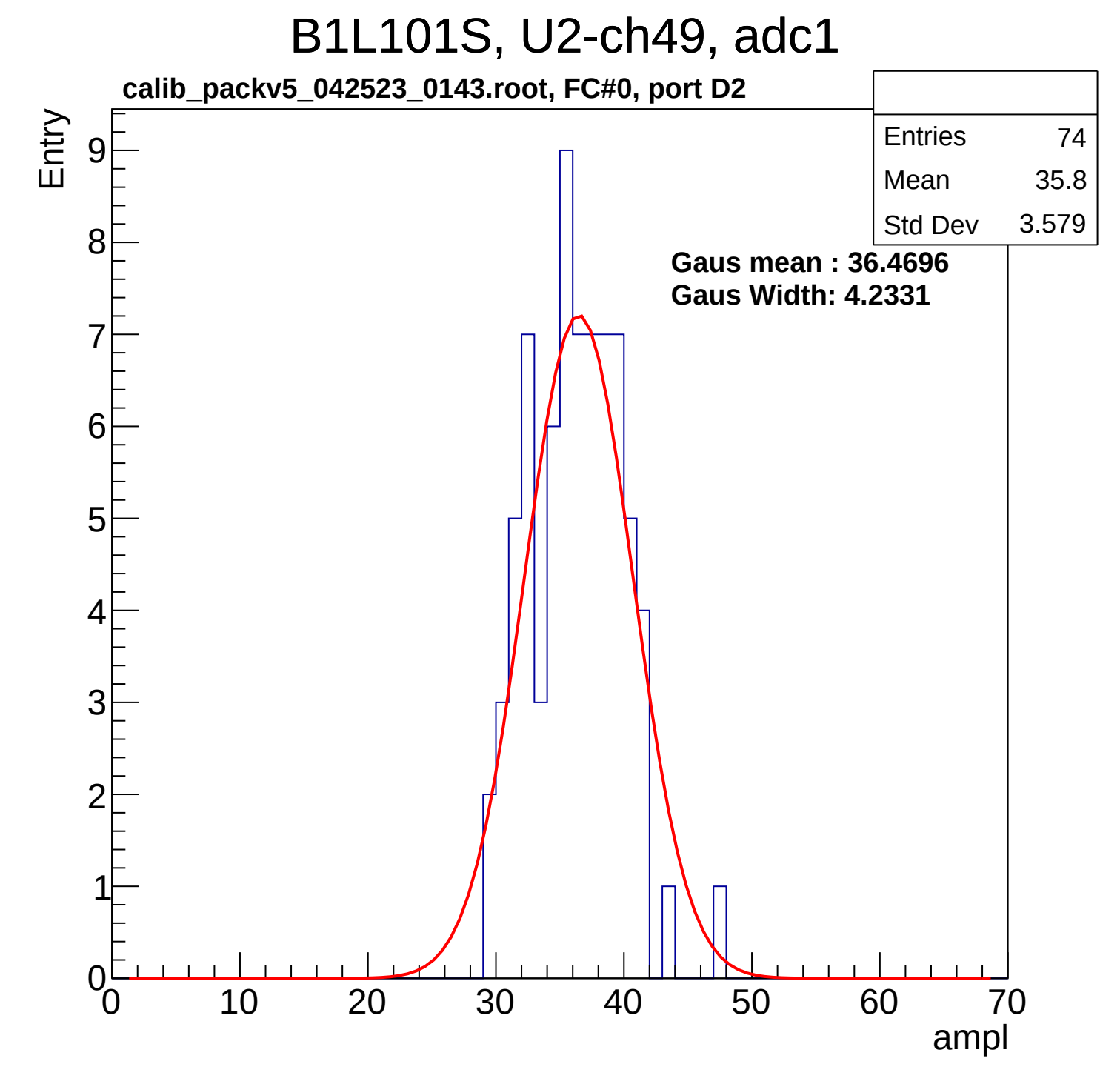

B1L101S, U2-ch48, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 53.15
Std Dev 3.349
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

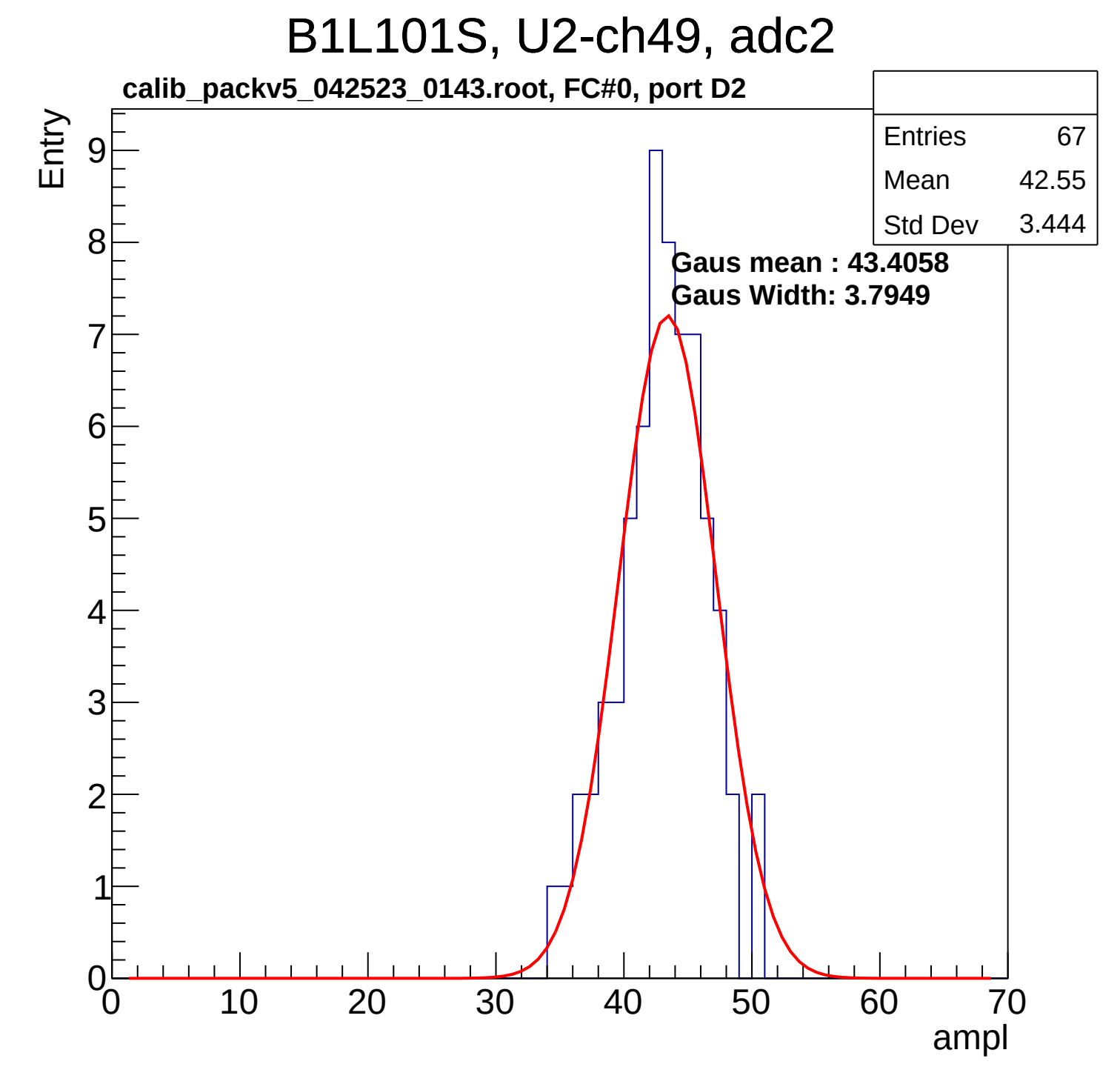

B1L101S, U2-ch48, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 58.64
Std Dev 3.078
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

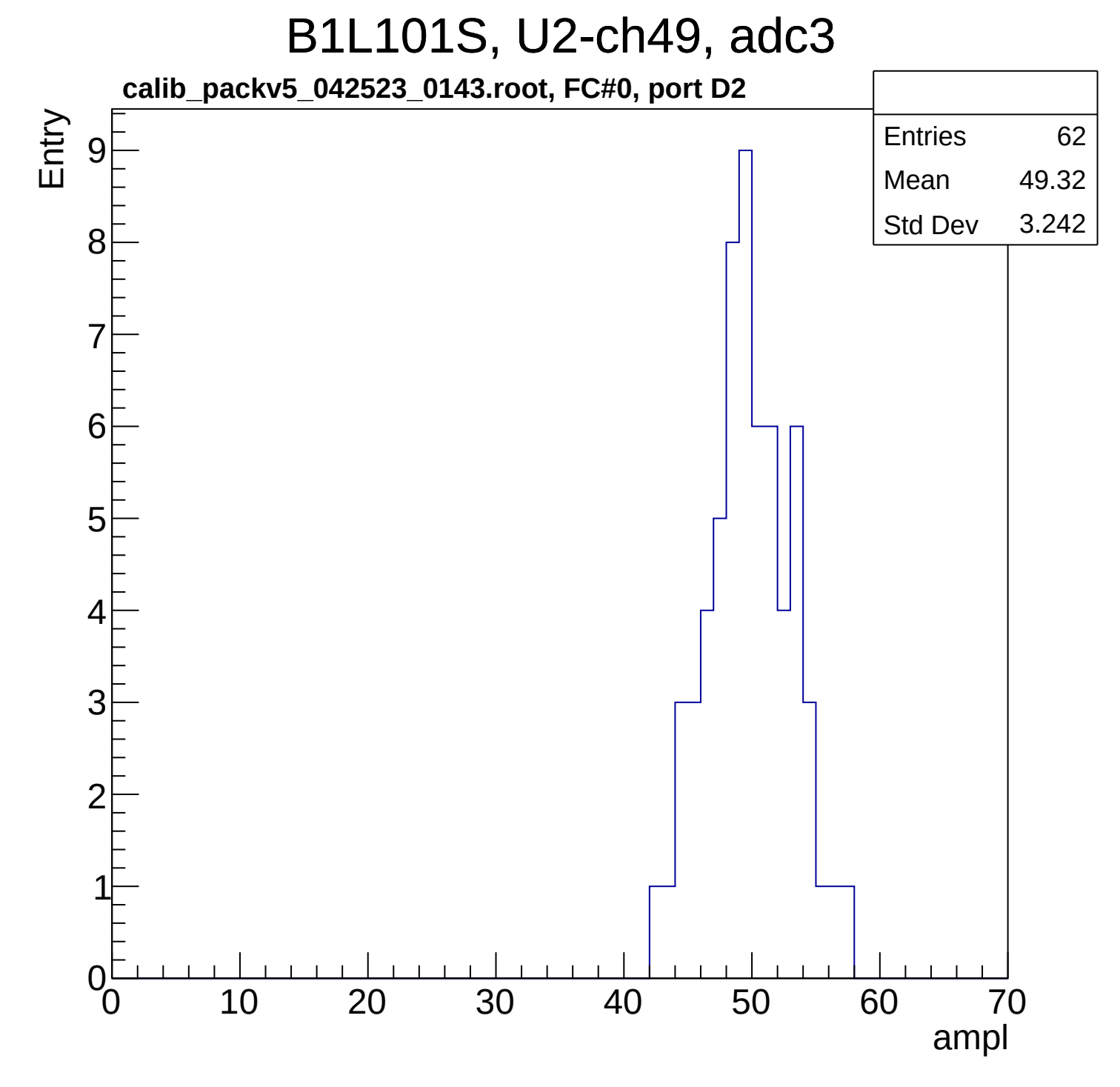

B1L101S, U2-ch48, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 13
Mean 57
Std Dev 16.5
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

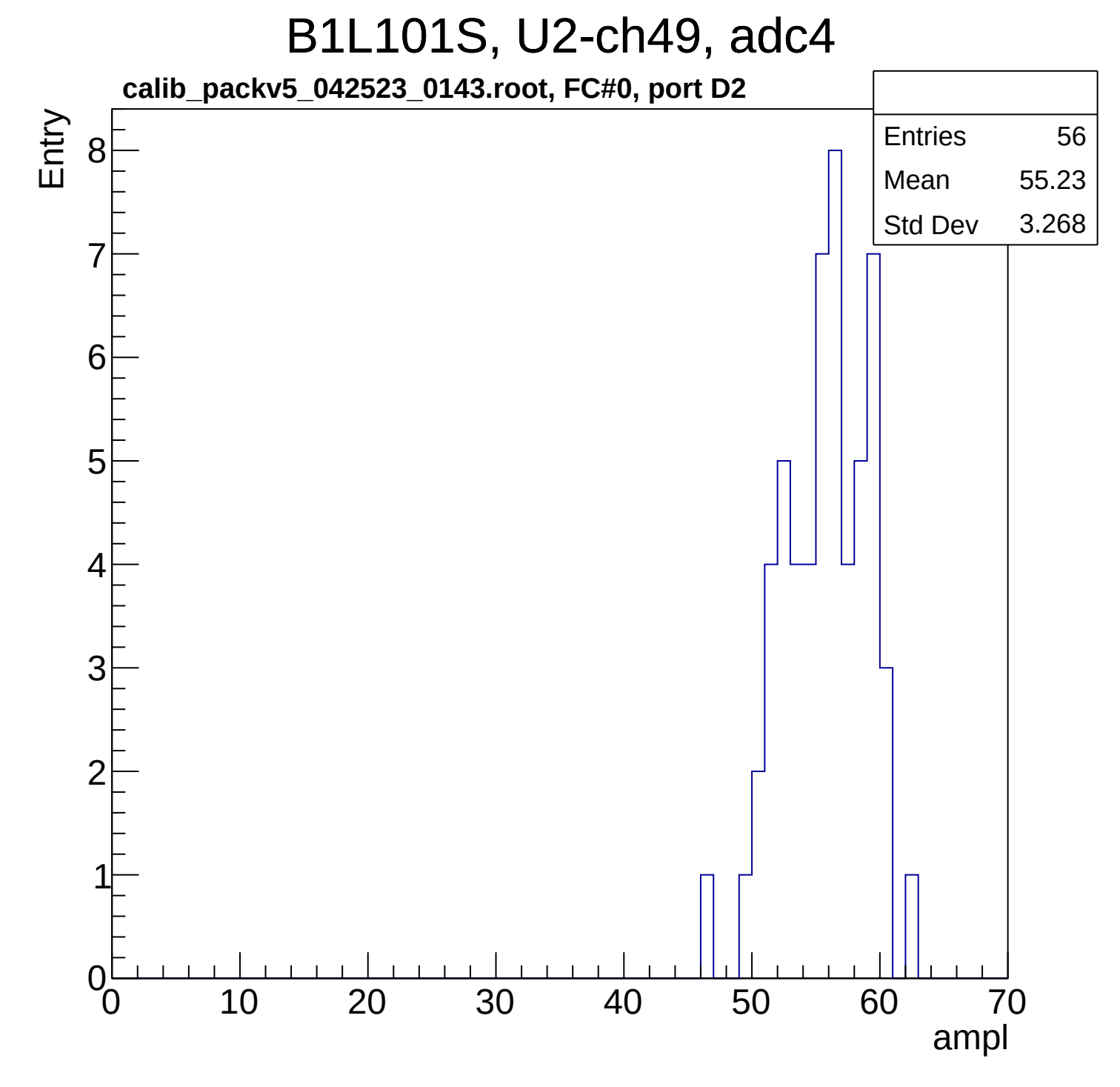

B1L101S, U2-ch48, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 30.5
Std Dev 30.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

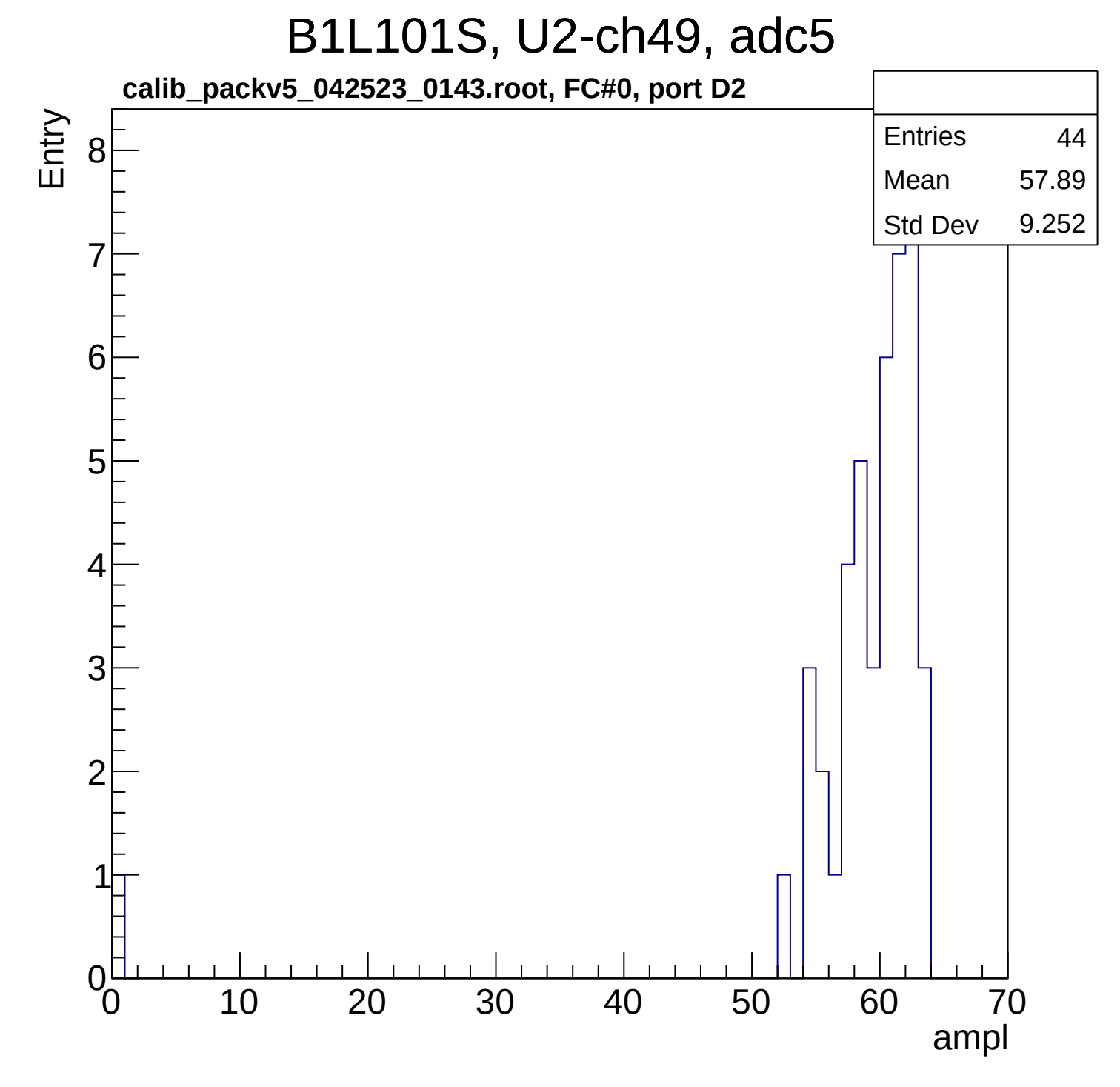

B1L101S, U2-ch49, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 28.98
Std Dev 4.992
Gaus mean : 30.0188
Gaus Width: 3.2967
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

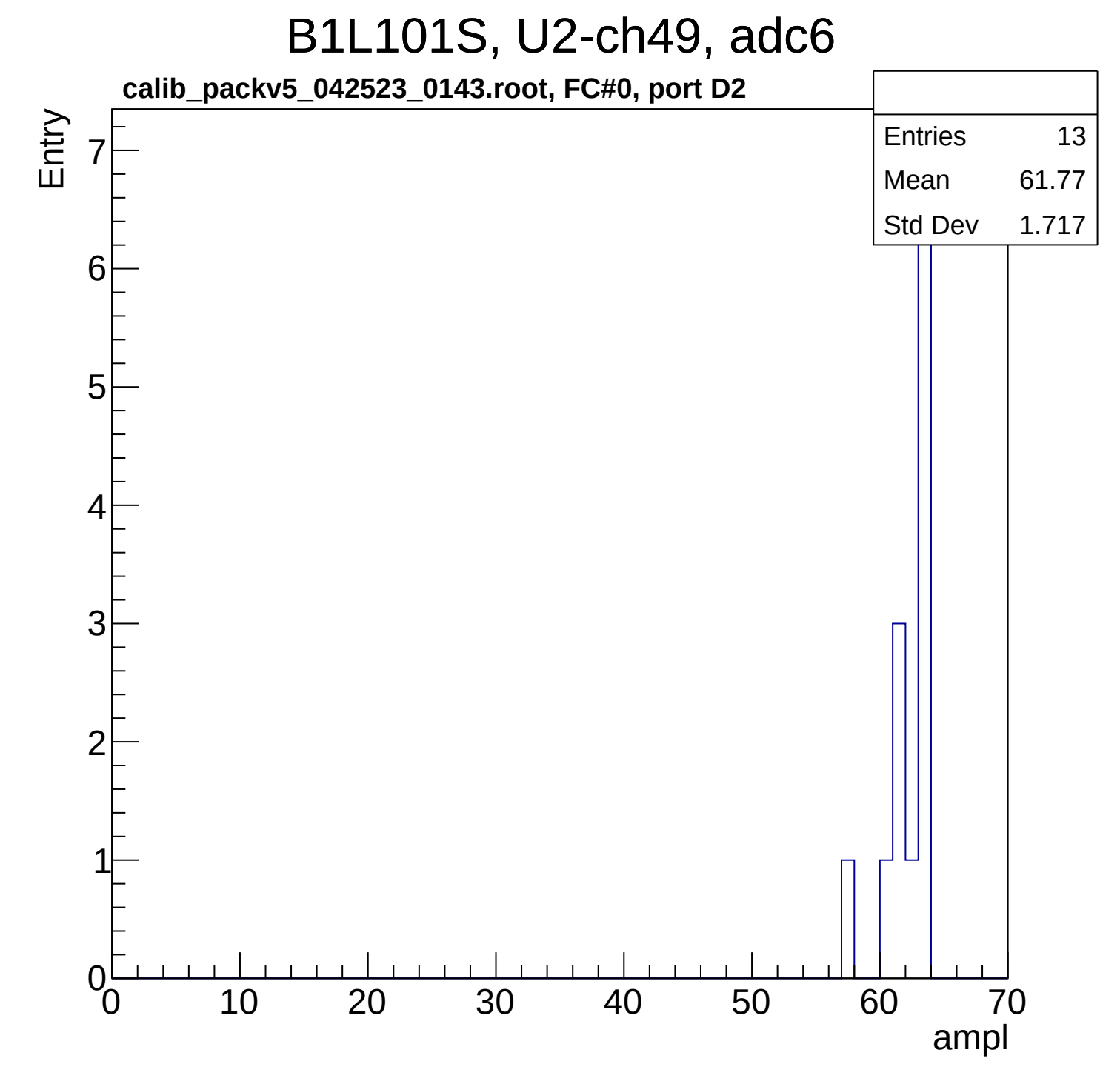

B1L101S, U2-ch49, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 35.8
Std Dev 3.579
Gaus mean : 36.4696
Gaus Width: 4.2331
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

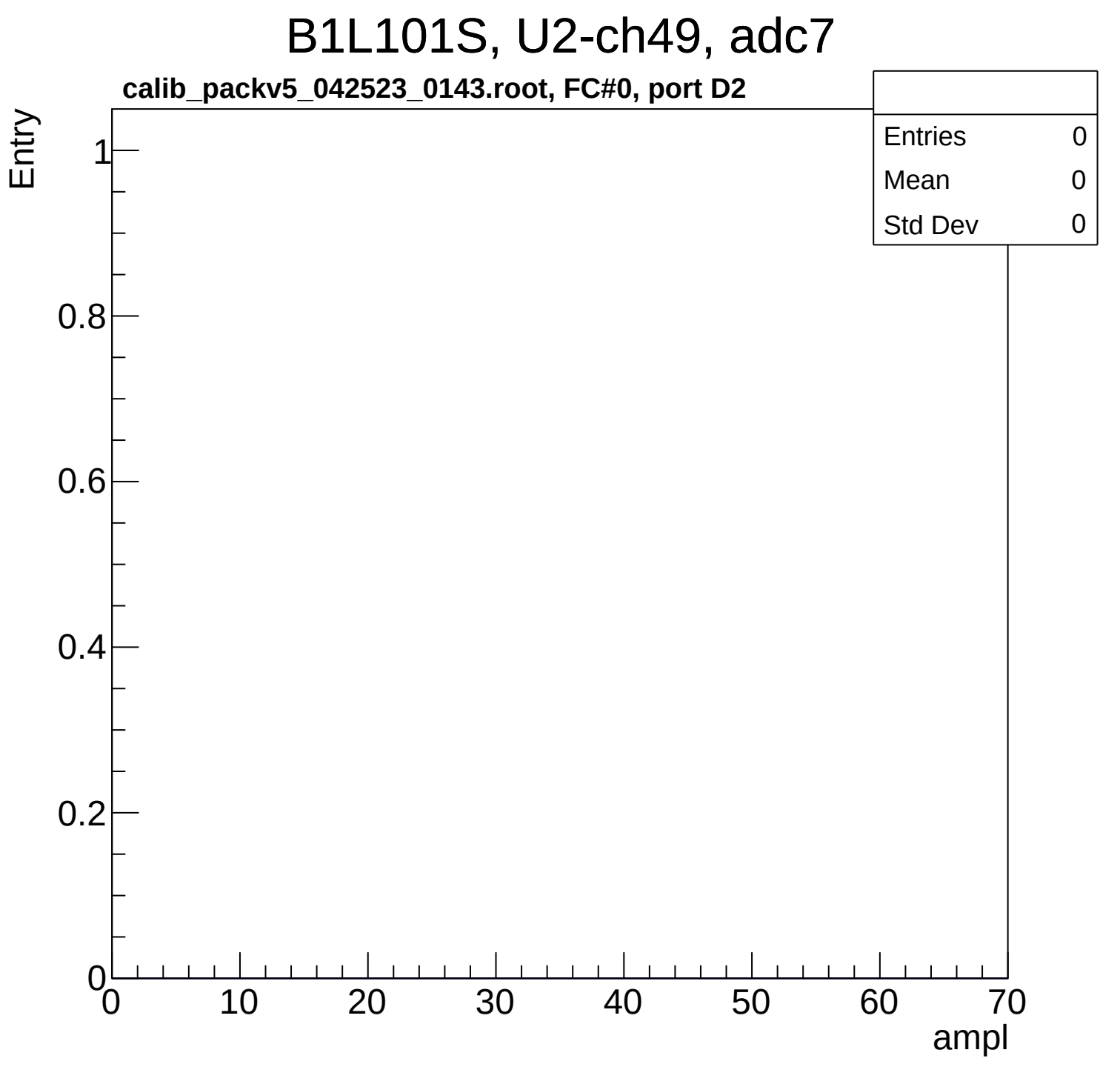

B1L101S, U2-ch49, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 42.55
Std Dev 3.444
Gaus mean : 43.4058
Gaus Width: 3.7949
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

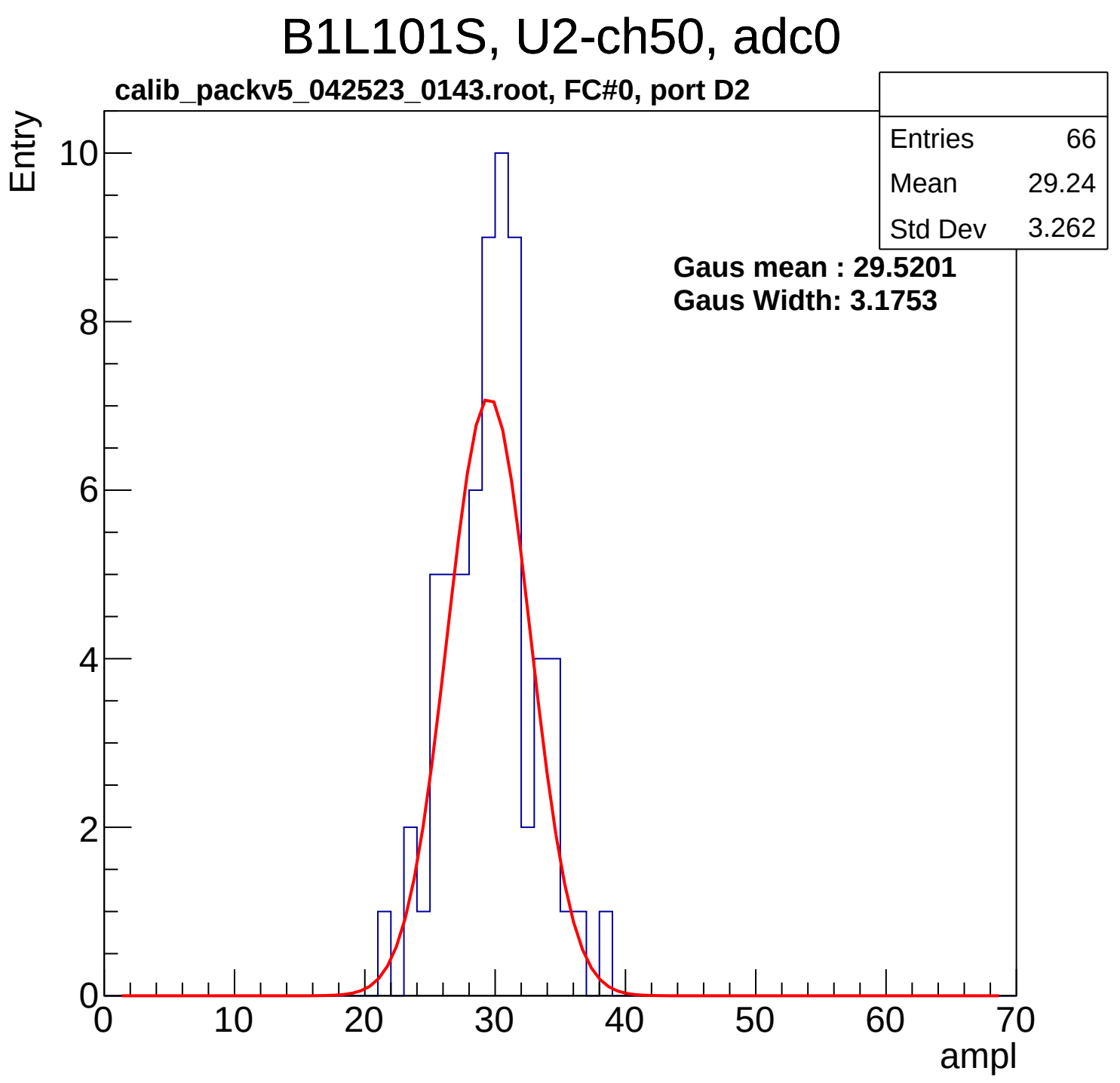

B1L101S, U2-ch49, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 49.32
Std Dev 3.242
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

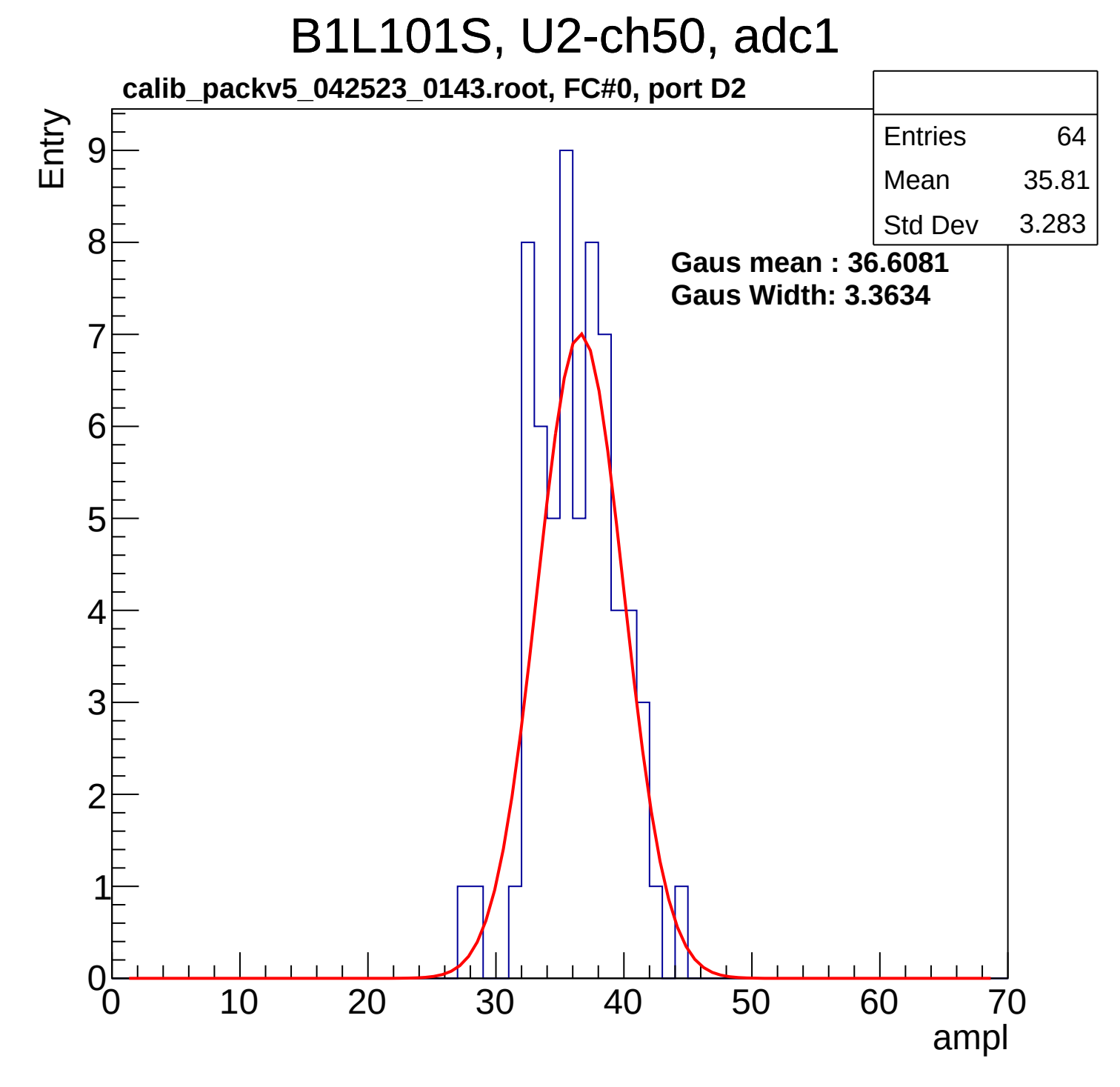

B1L101S, U2-ch49, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 55.23
Std Dev 3.268
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

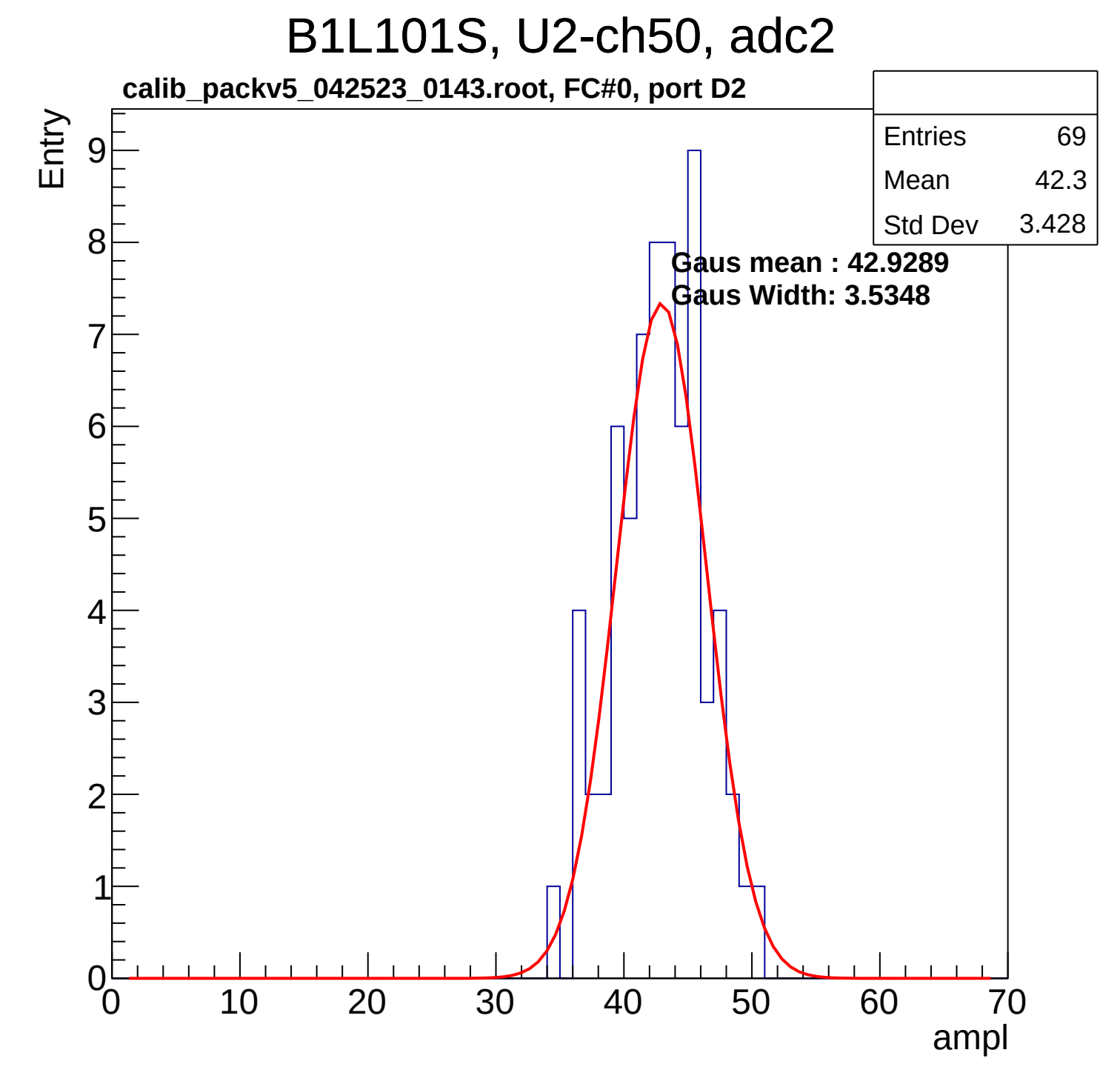

B1L101S, U2-ch49, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 44
Mean 57.89
Std Dev 9.252
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

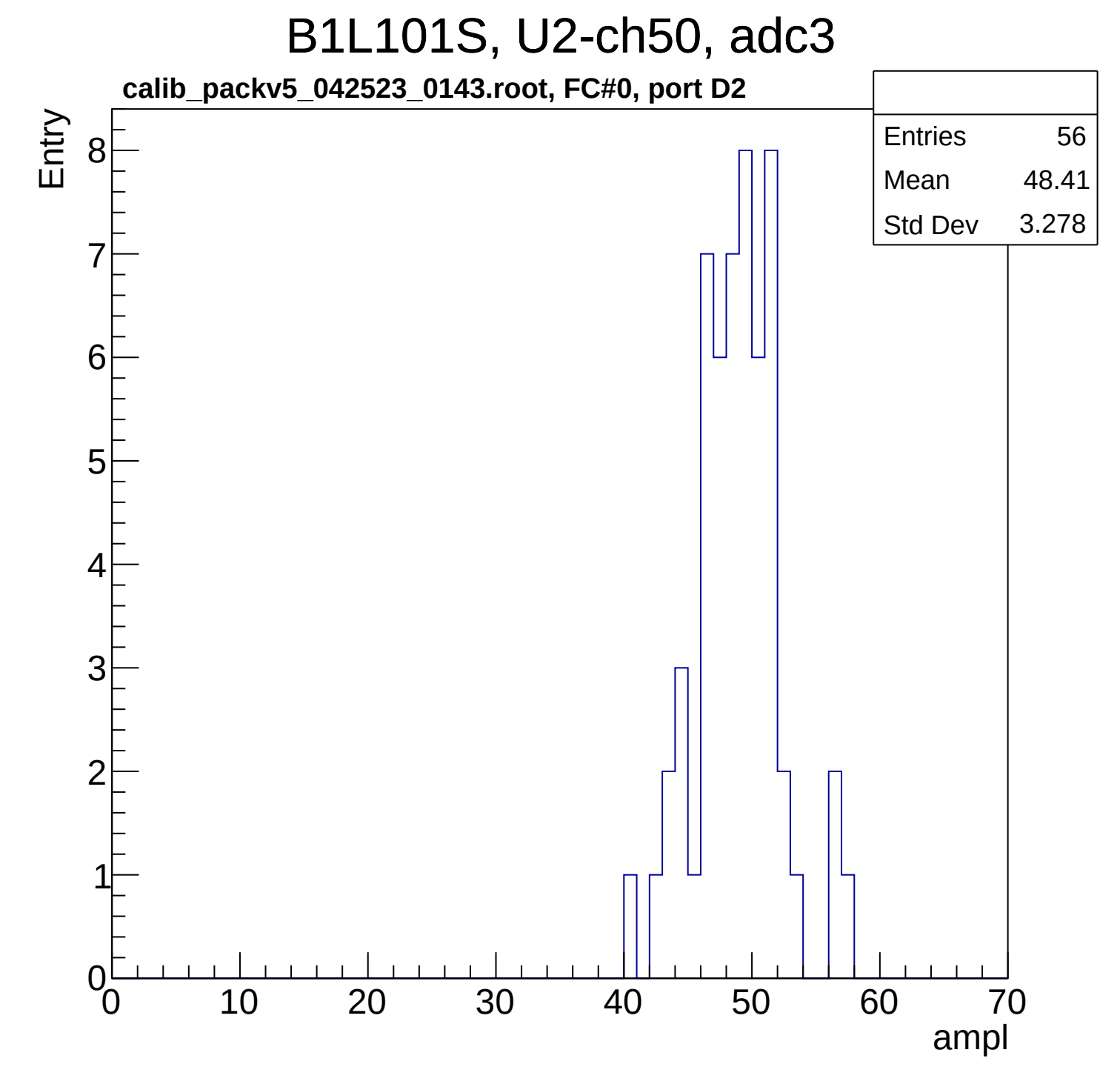

B1L101S, U2-ch49, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 13
Mean 61.77
Std Dev 1.717
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

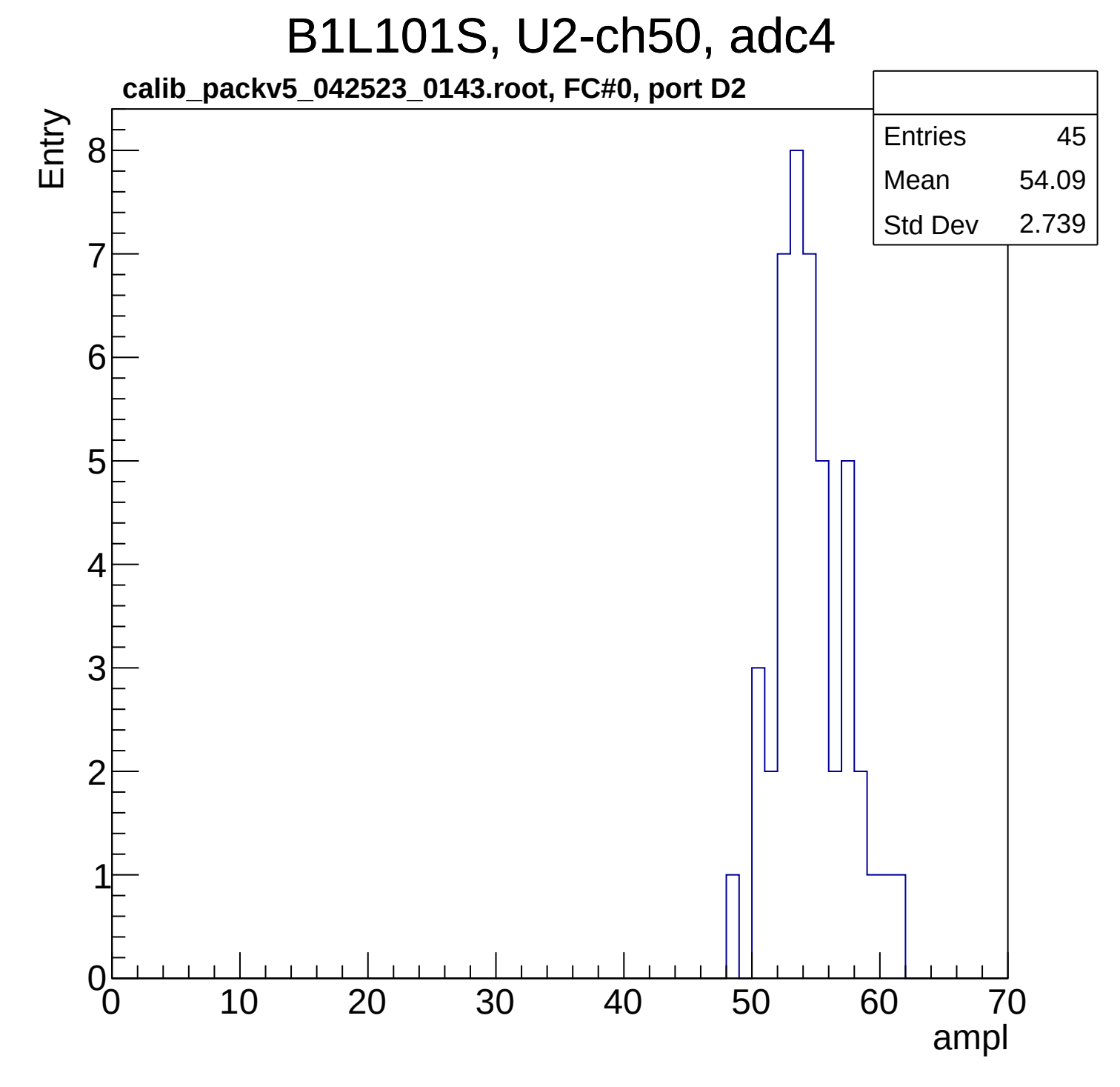

B1L101S, U2-ch49, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

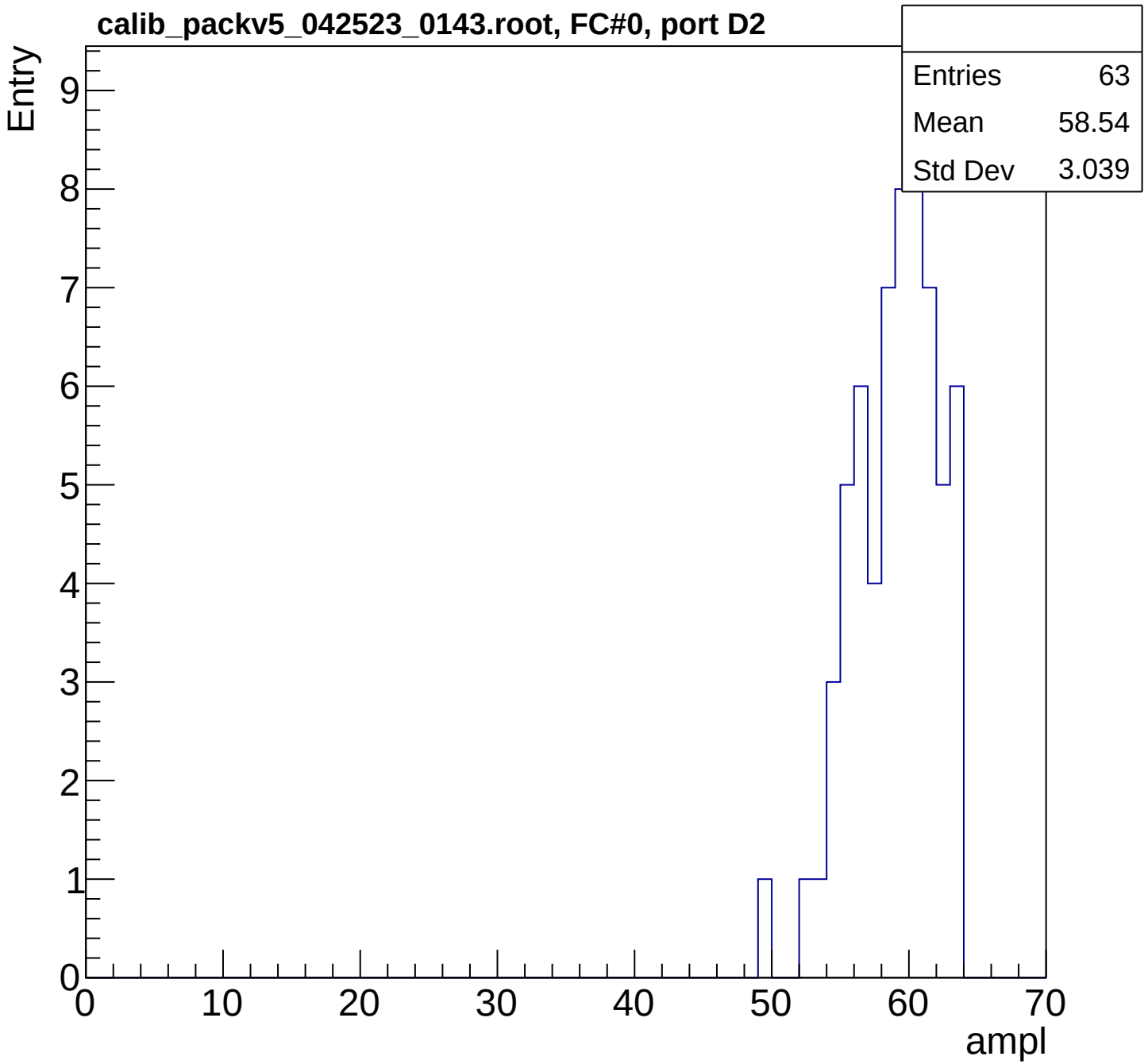

B1L101S, U2-ch50, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 29.24
Std Dev 3.262
Gaus mean : 29.5201
Gaus Width: 3.1753
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

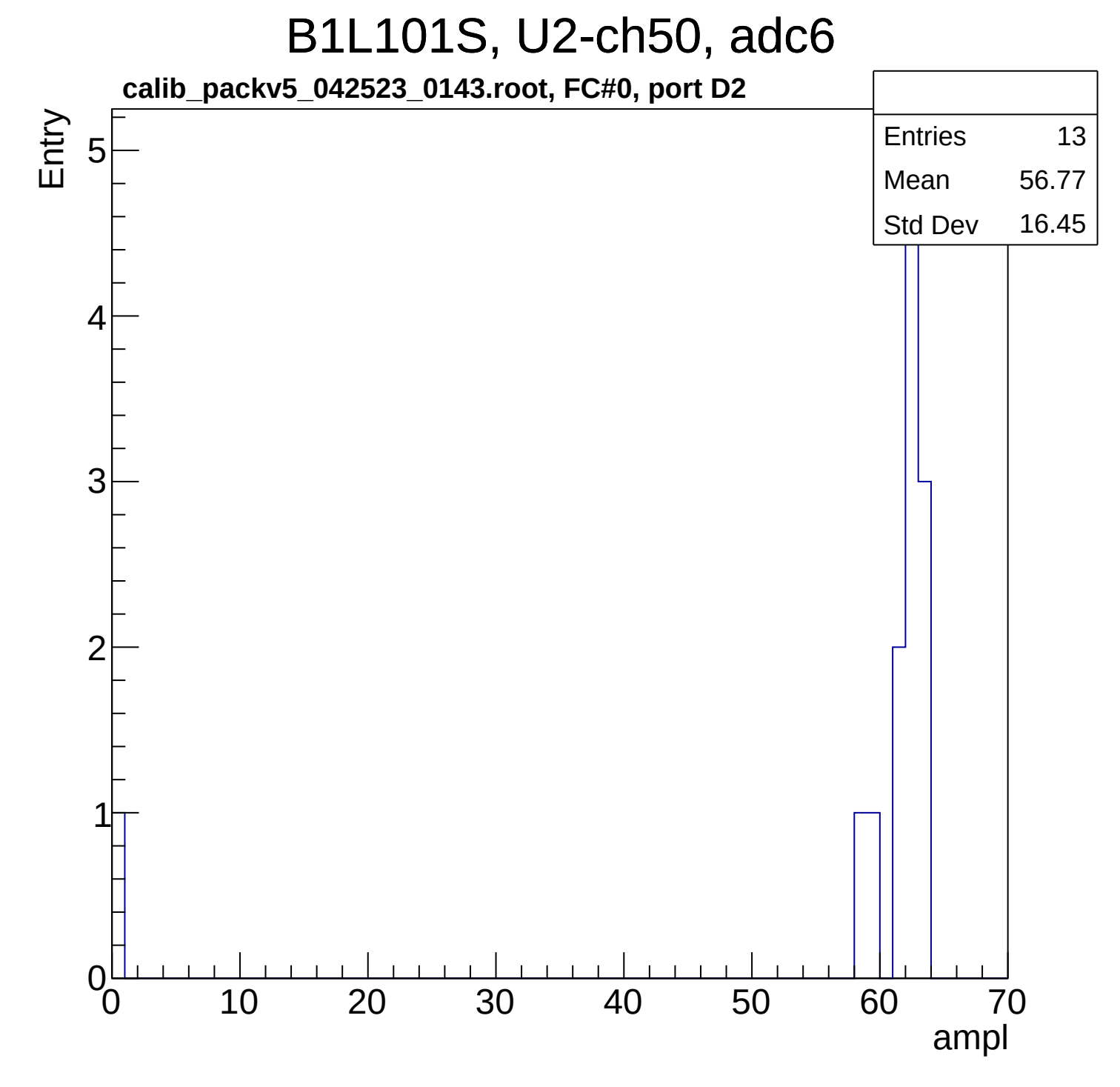

B1L101S, U2-ch50, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 35.81
Std Dev 3.283
Gaus mean : 36.6081
Gaus Width: 3.3634
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

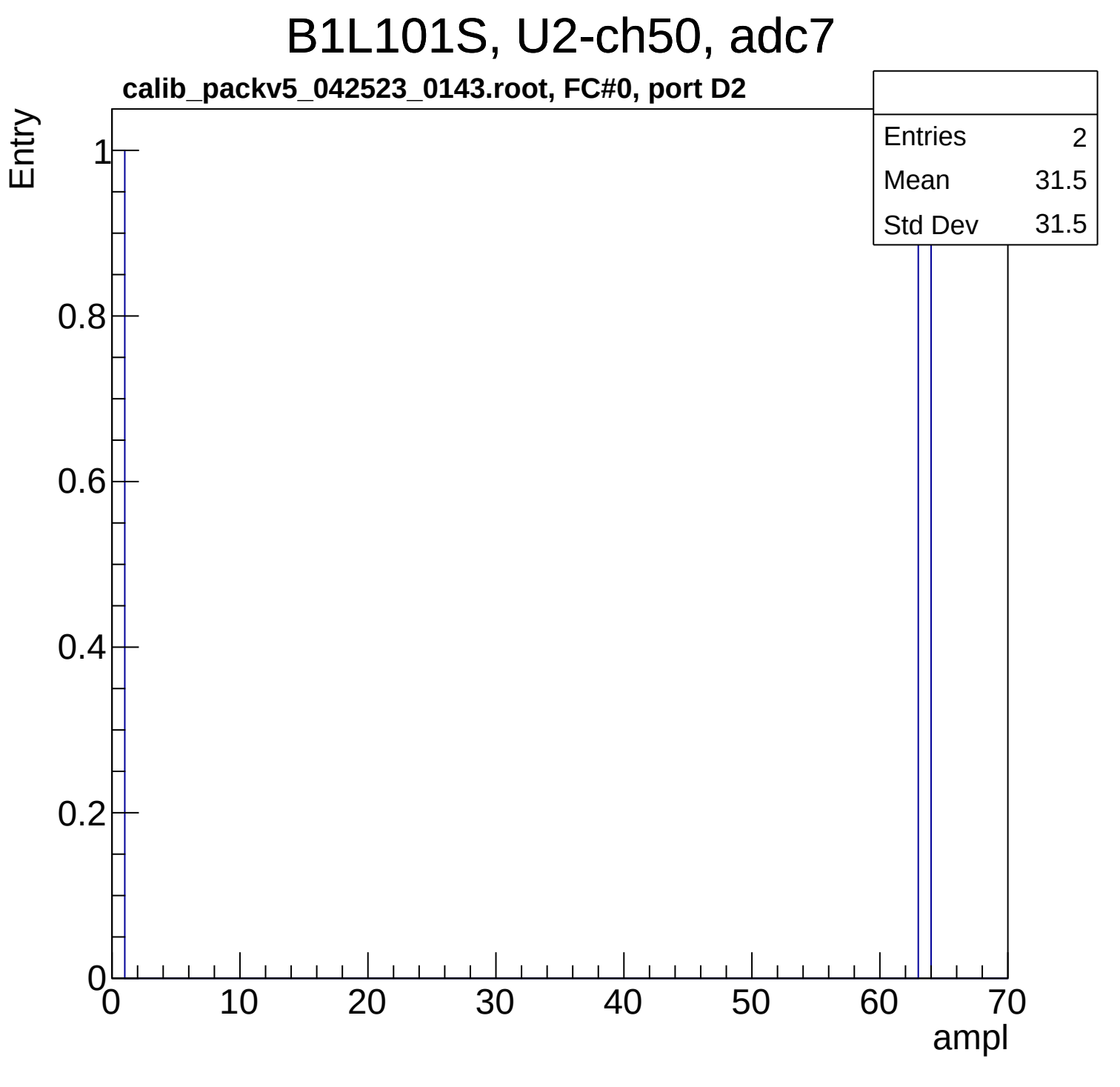

B1L101S, U2-ch50, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 42.3
Std Dev 3.428
Gaus mean : 42.9289
Gaus Width: 3.5348
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

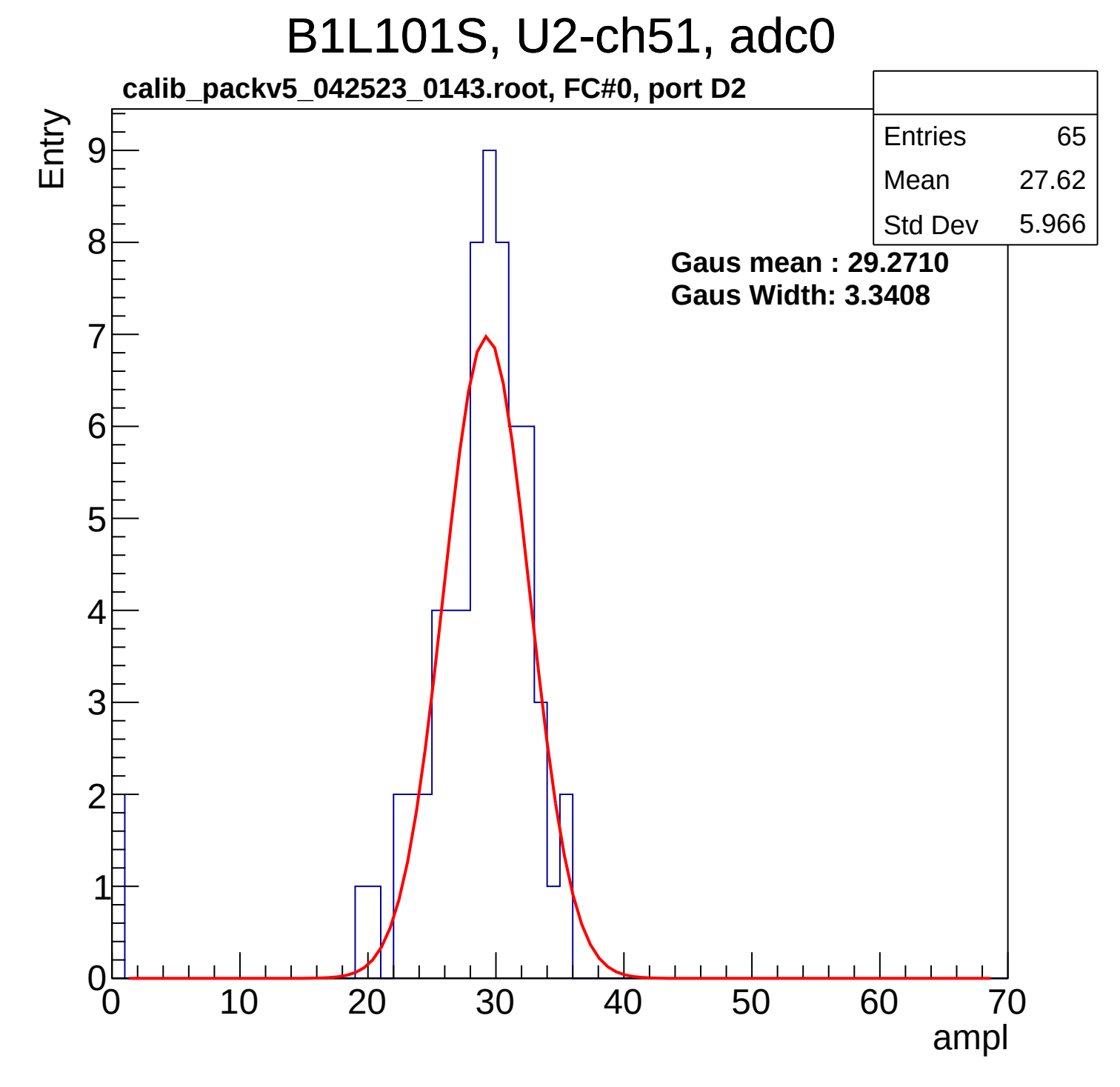

B1L101S, U2-ch50, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 48.41
Std Dev 3.278
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

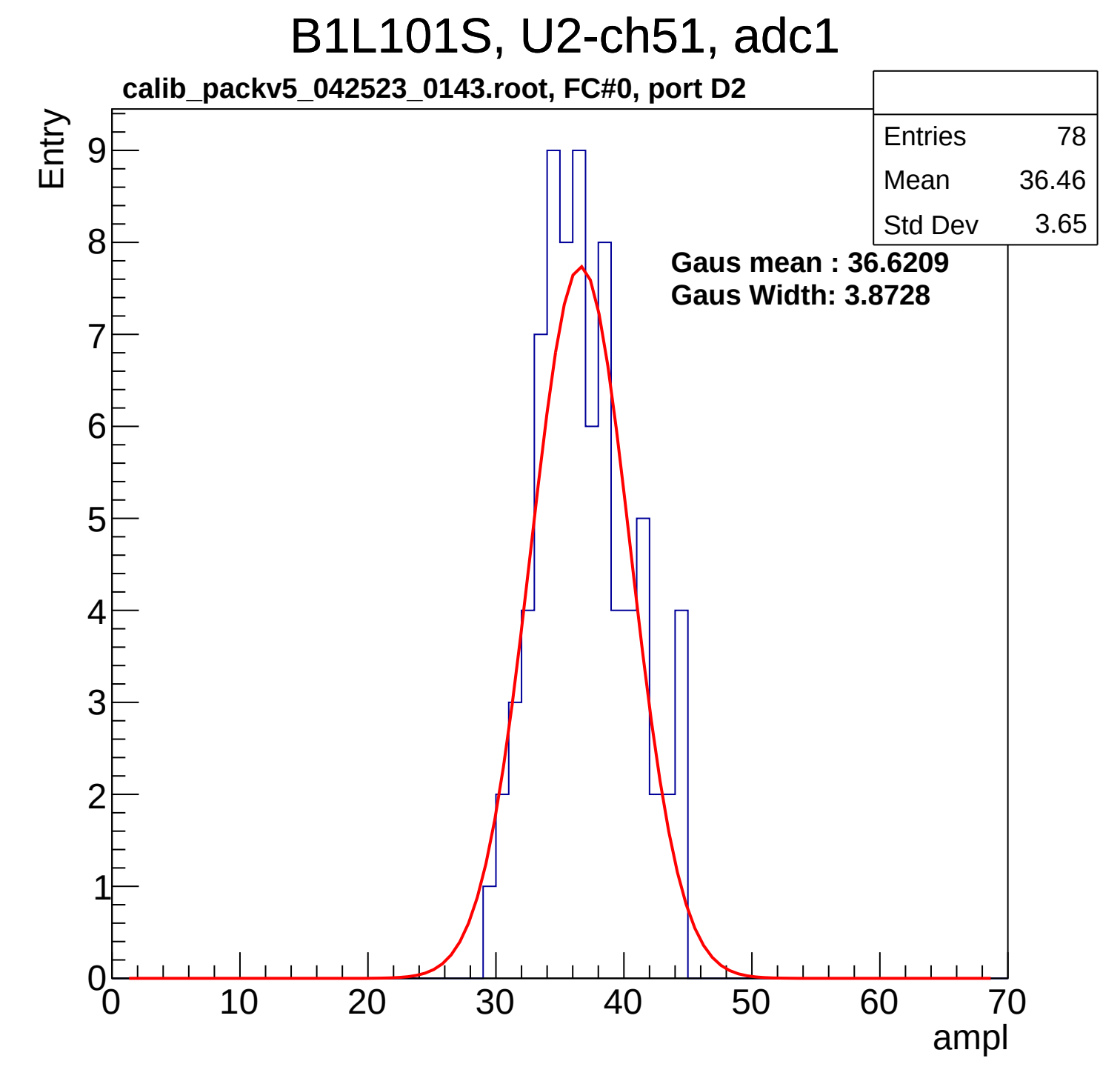

B1L101S, U2-ch50, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 54.09
Std Dev 2.739
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

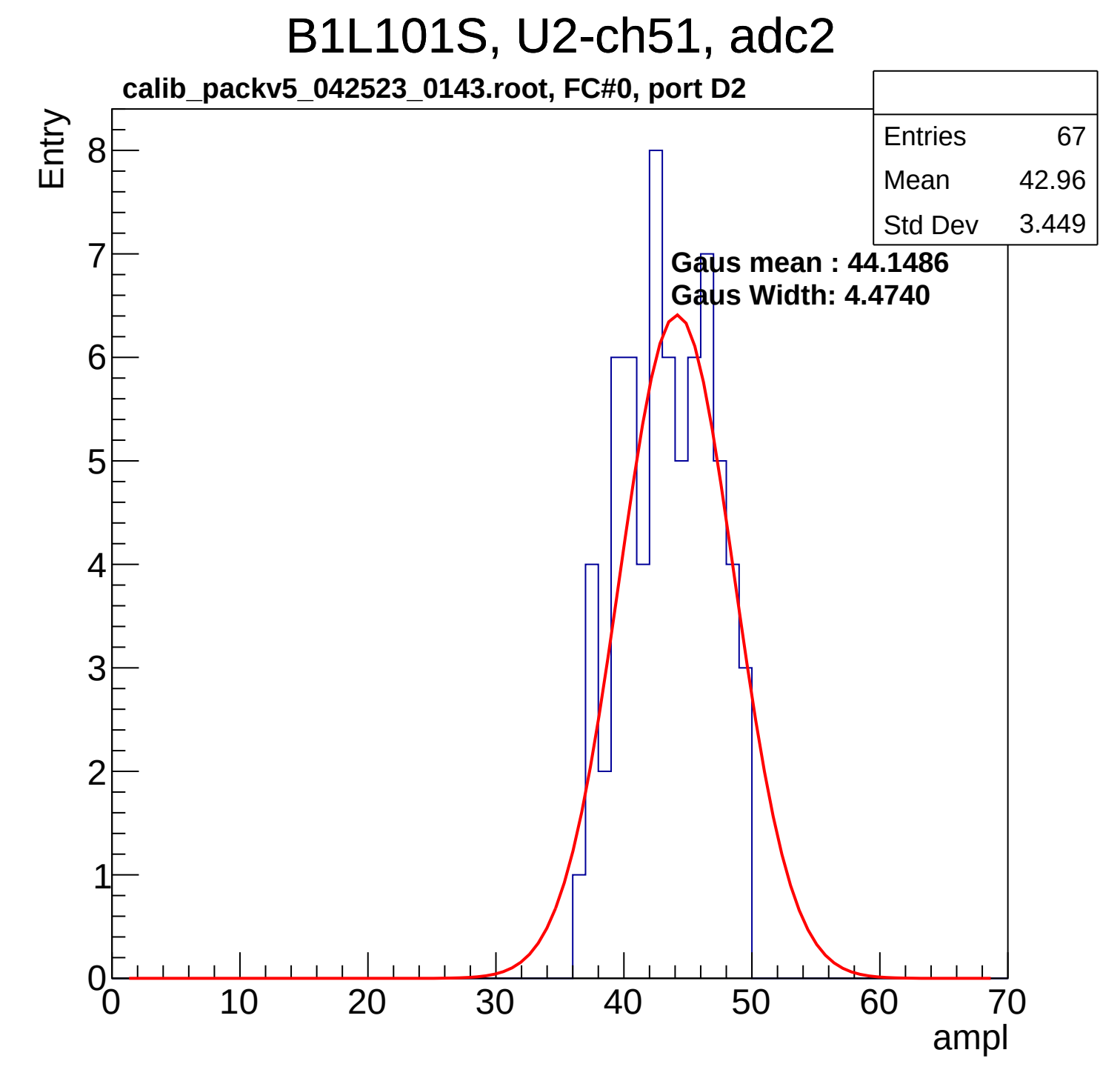

B1L101S, U2-ch50, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 58.54
Std Dev 3.039
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

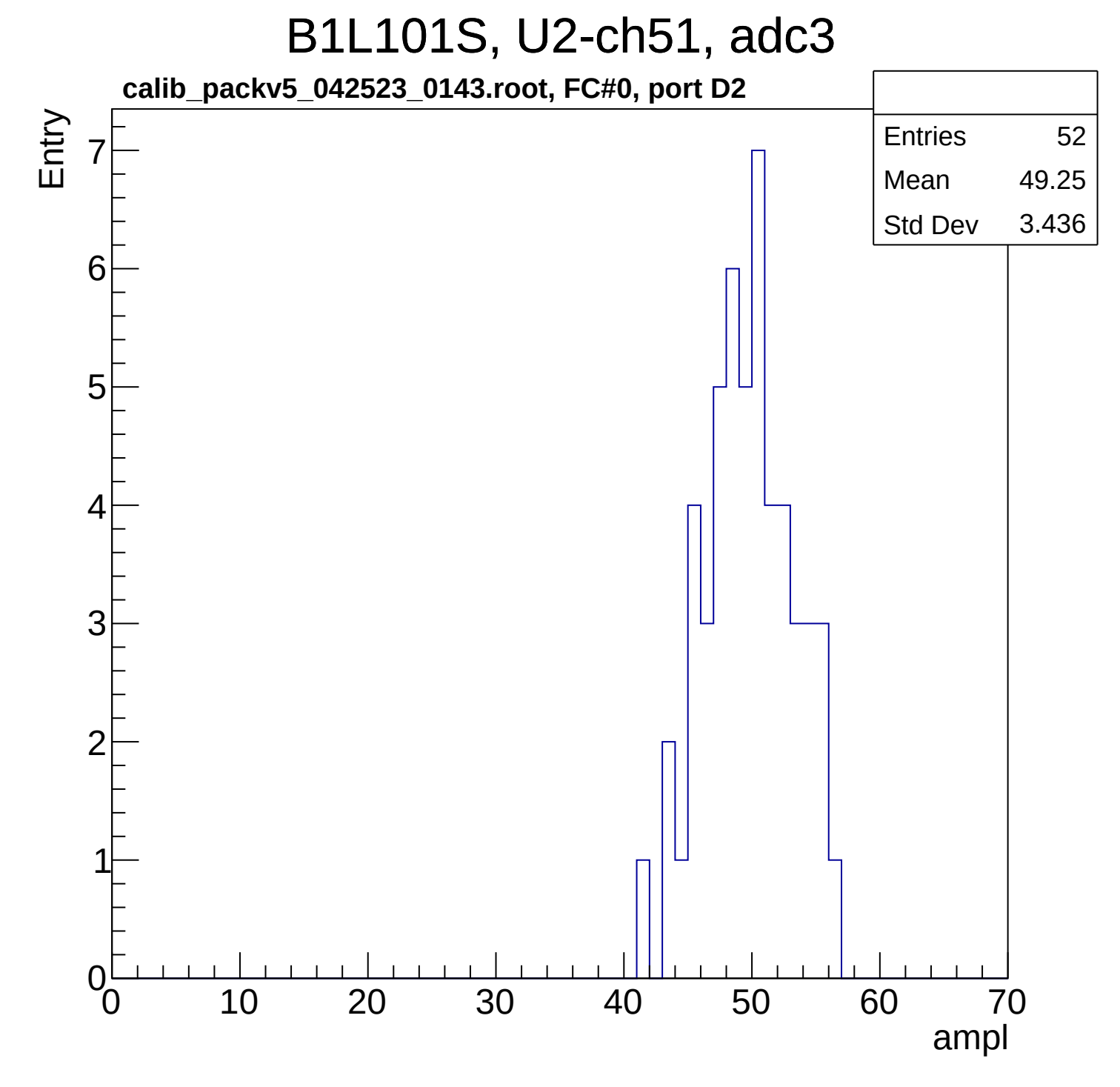

B1L101S, U2-ch50, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 13
Mean 56.77
Std Dev 16.45
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

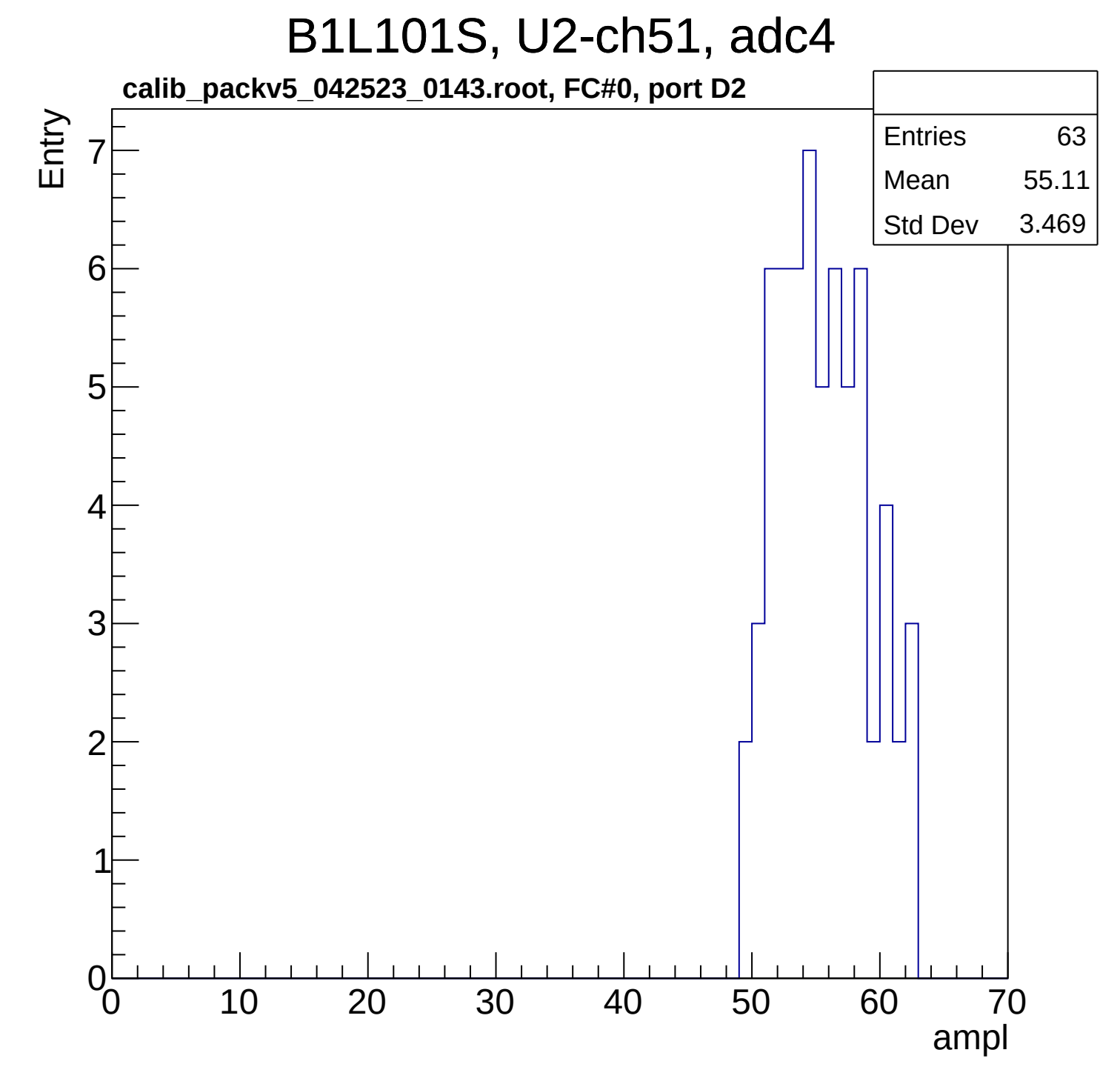

B1L101S, U2-ch50, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

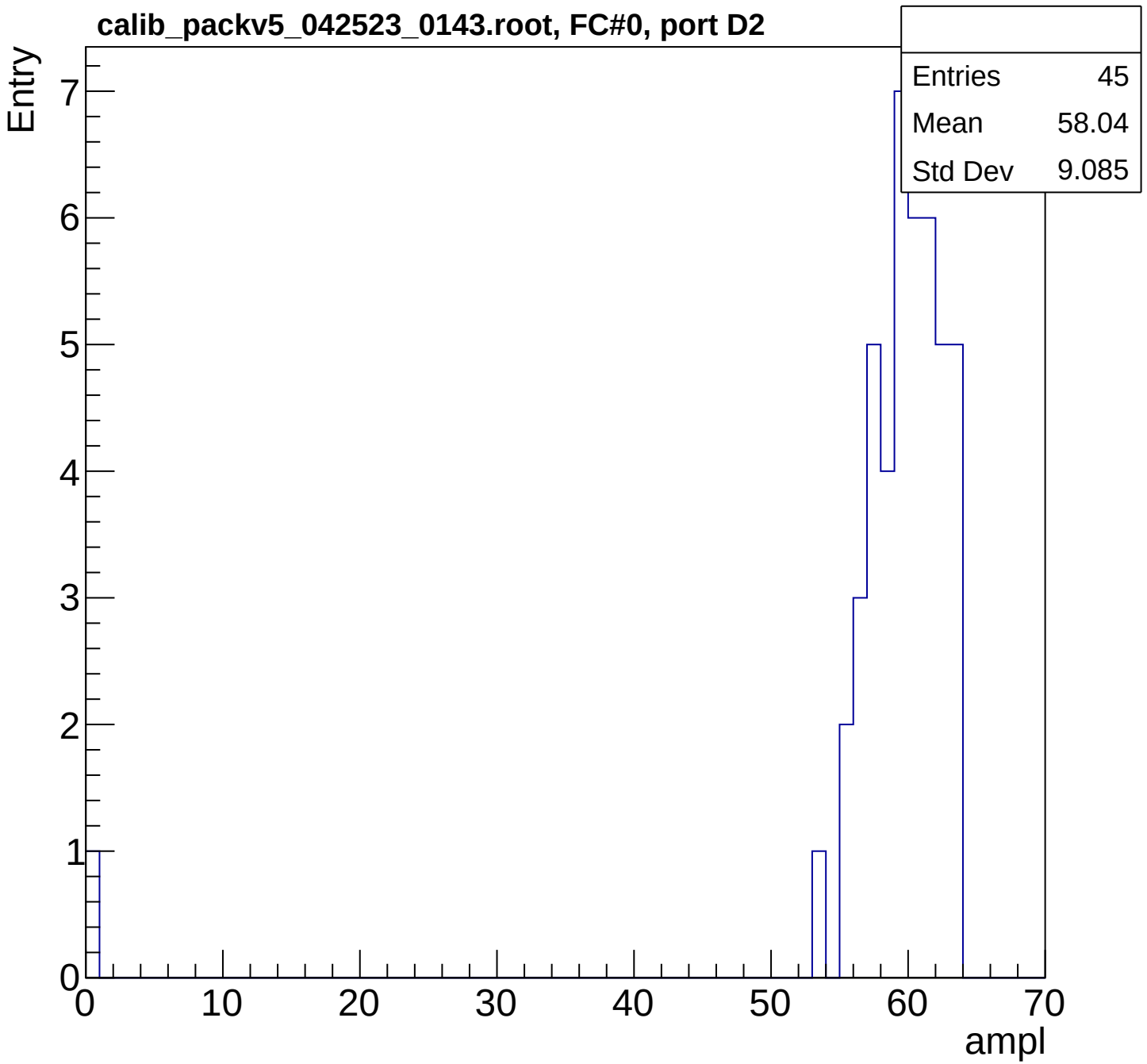

B1L101S, U2-ch51, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 27.62
Std Dev 5.966
Gaus mean : 29.2710
Gaus Width: 3.3408
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

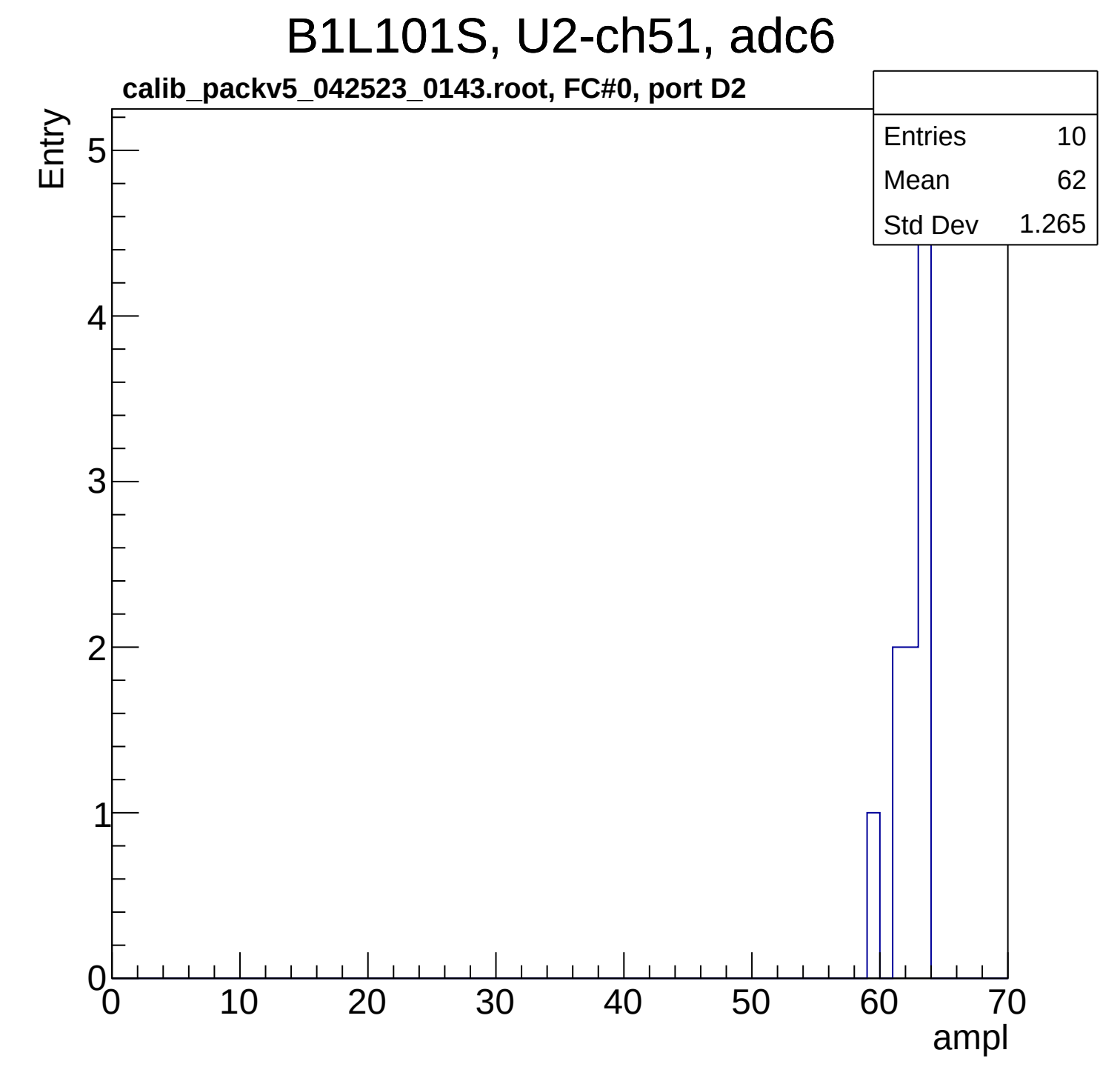

B1L101S, U2-ch51, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 36.46
Std Dev 3.65
Gaus mean : 36.6209
Gaus Width: 3.8728
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

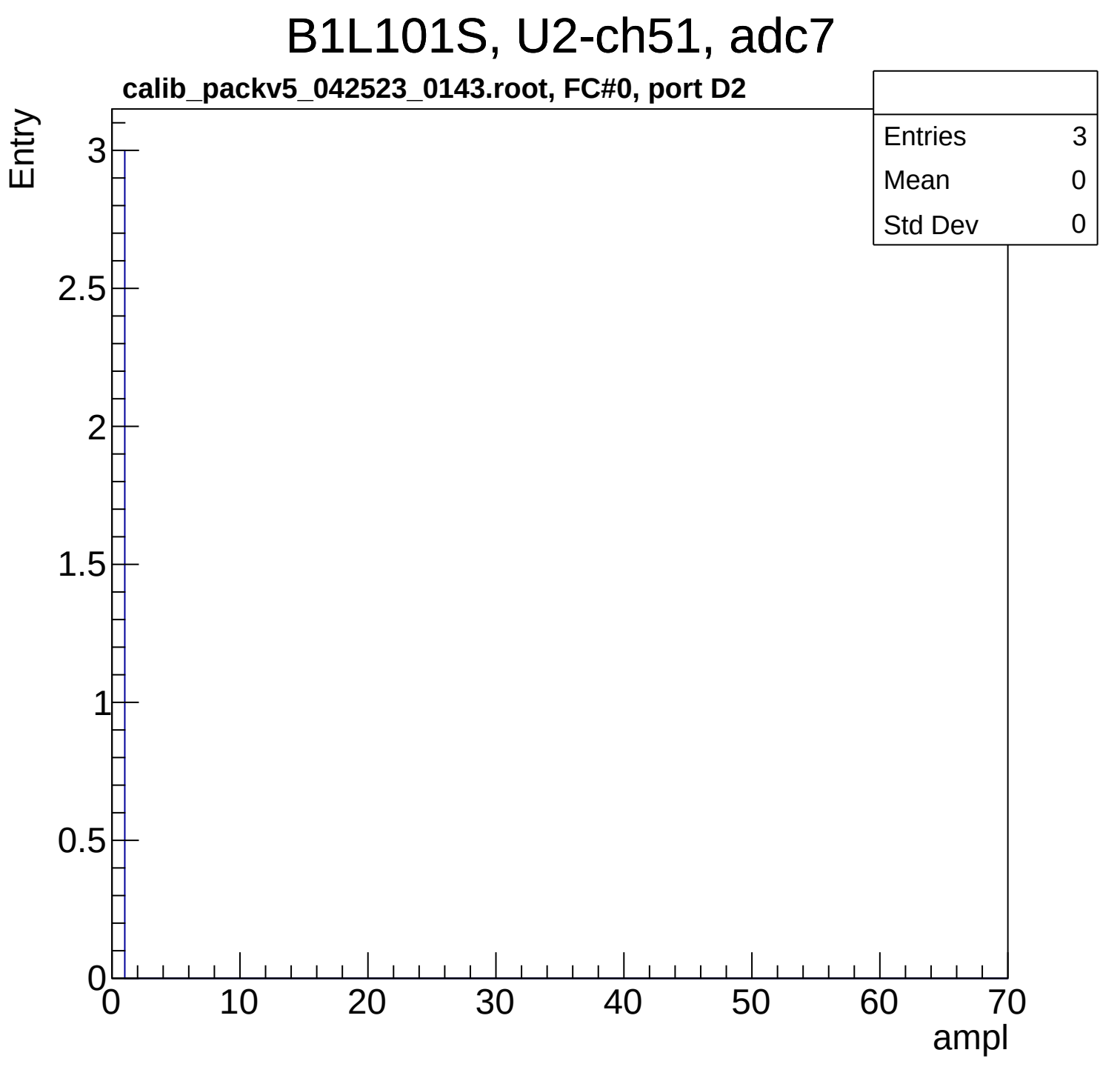

B1L101S, U2-ch51, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 42.96
Std Dev 3.449
Gaus mean : 44.1486
Gaus Width: 4.4740
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

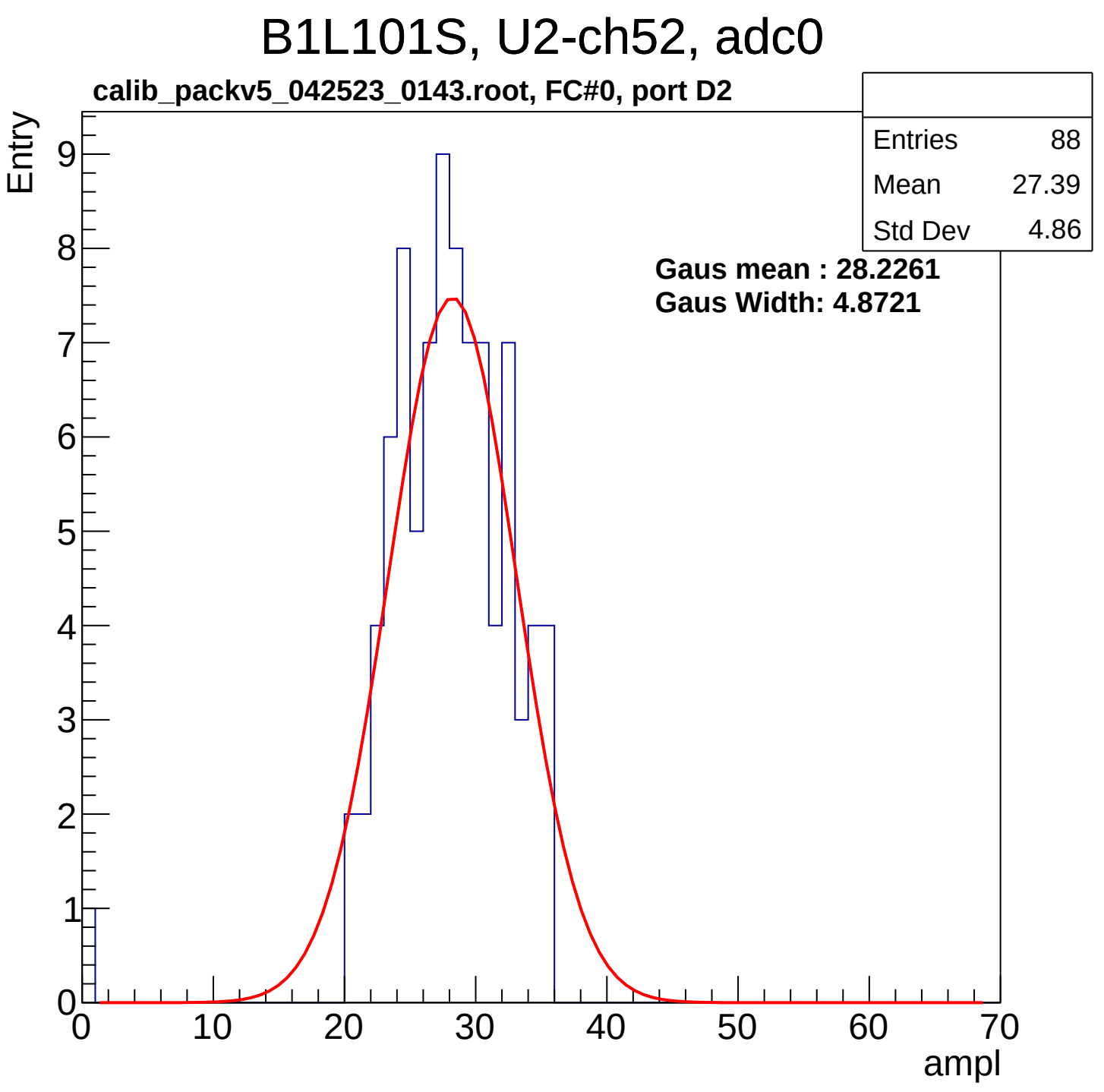

B1L101S, U2-ch51, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 49.25
Std Dev 3.436
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

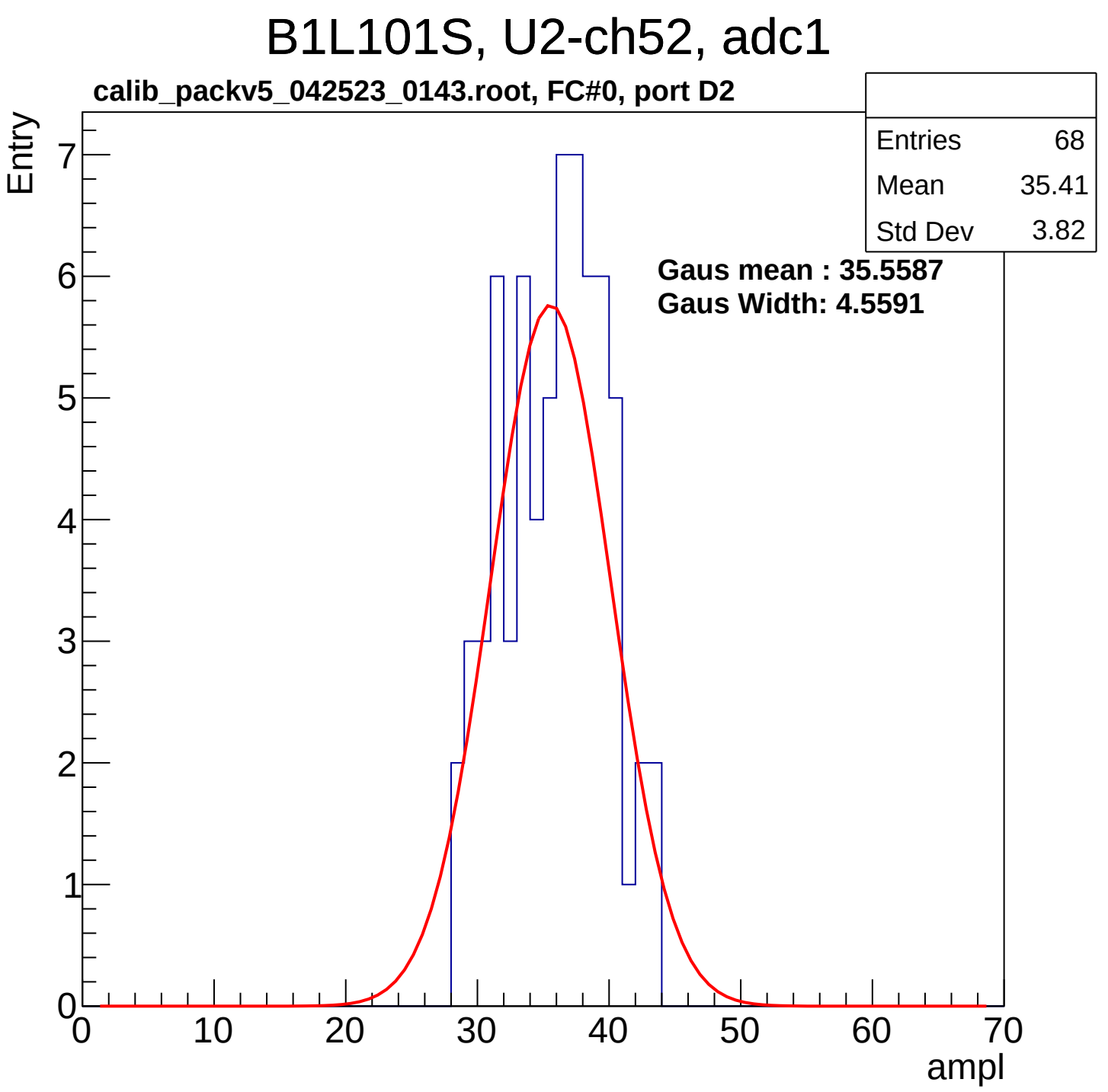

B1L101S, U2-ch51, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 55.11
Std Dev 3.469
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

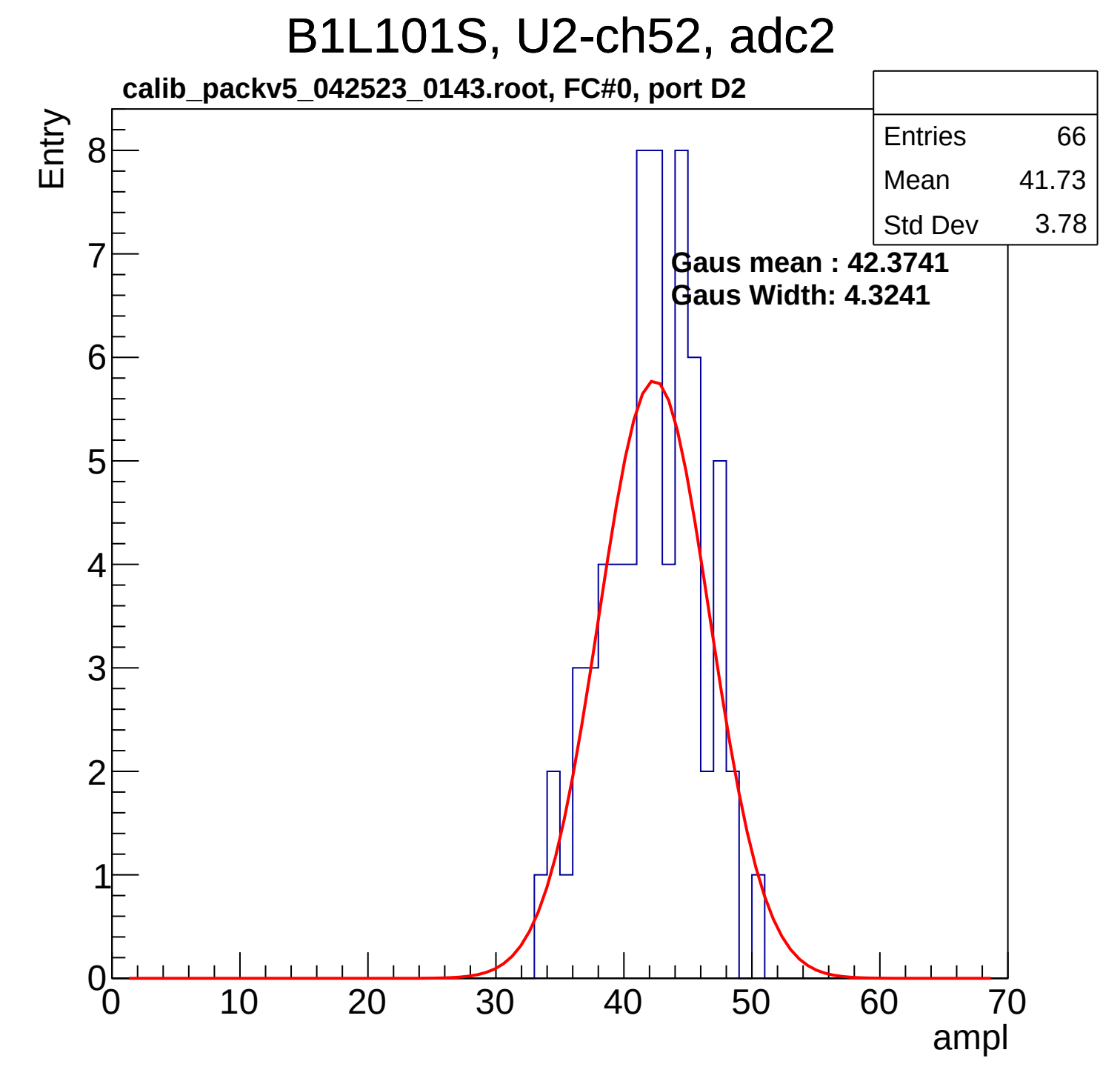

B1L101S, U2-ch51, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 58.04
Std Dev 9.085
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

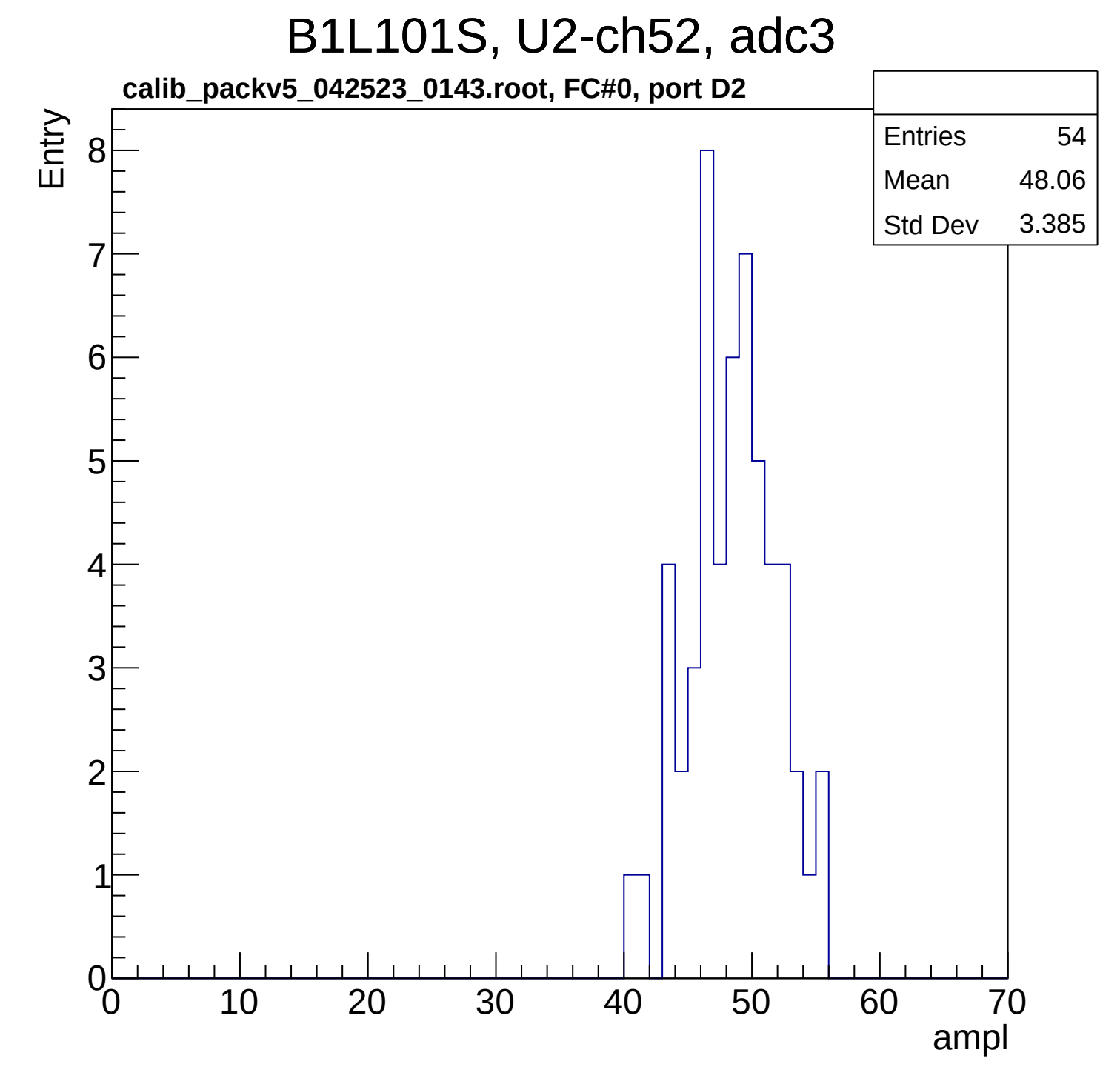

B1L101S, U2-ch51, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 62
Std Dev 1.265
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

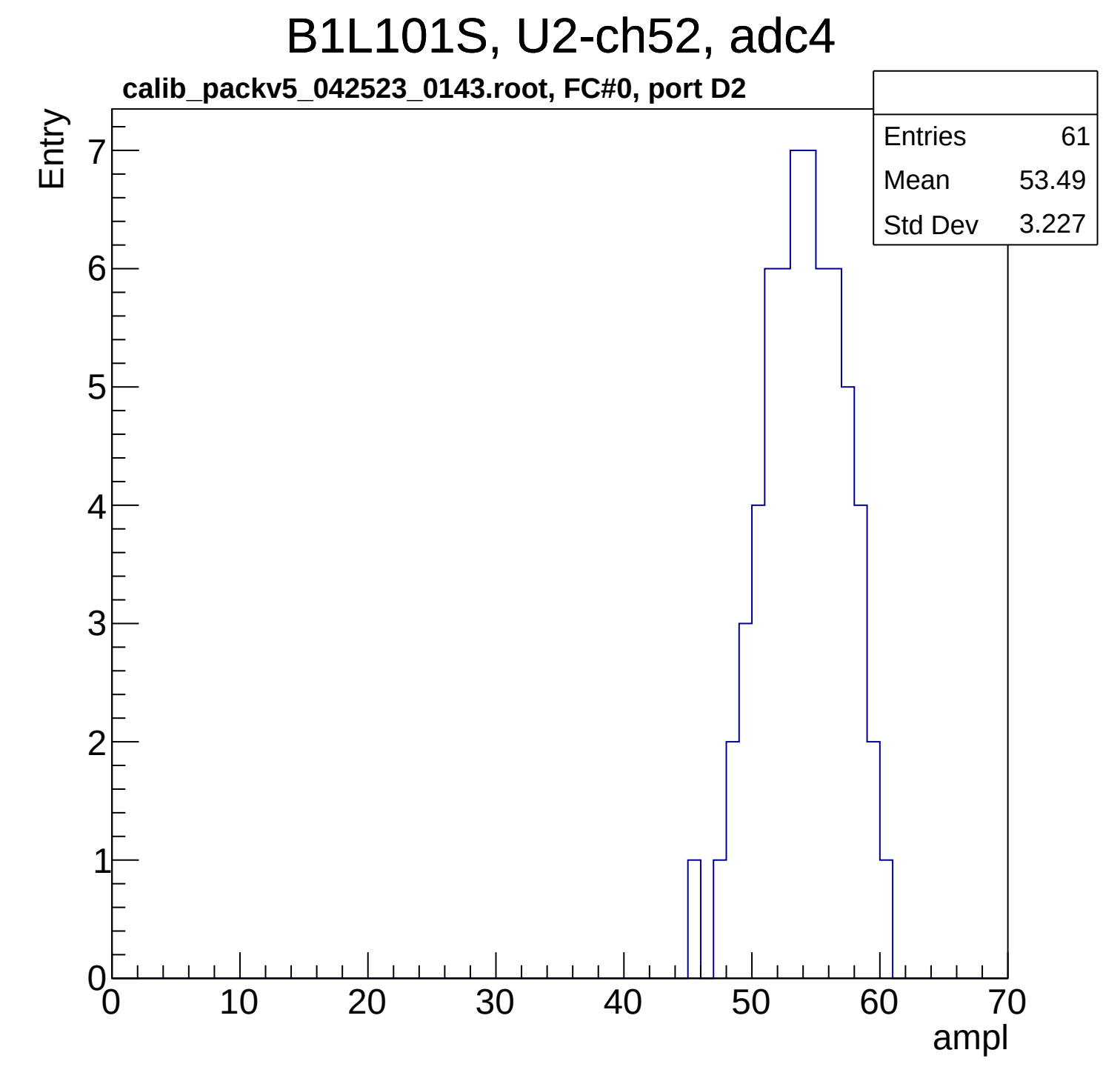

B1L101S, U2-ch51, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 0
Std Dev 0
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl

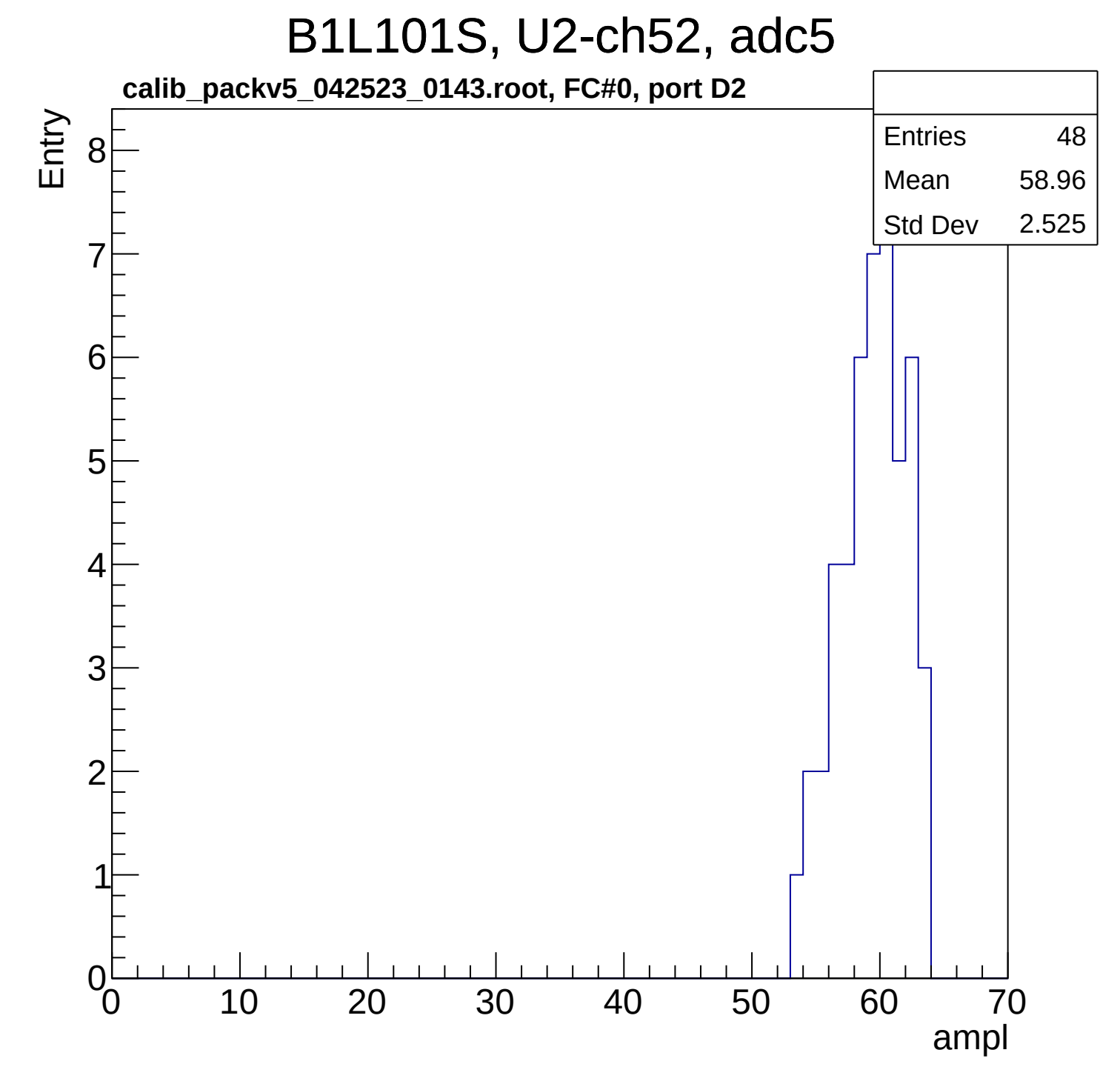

B1L101S, U2-ch52, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 88
Mean 27.39
Std Dev 4.86
Gaus mean : 28.2261
Gaus Width: 4.8721
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

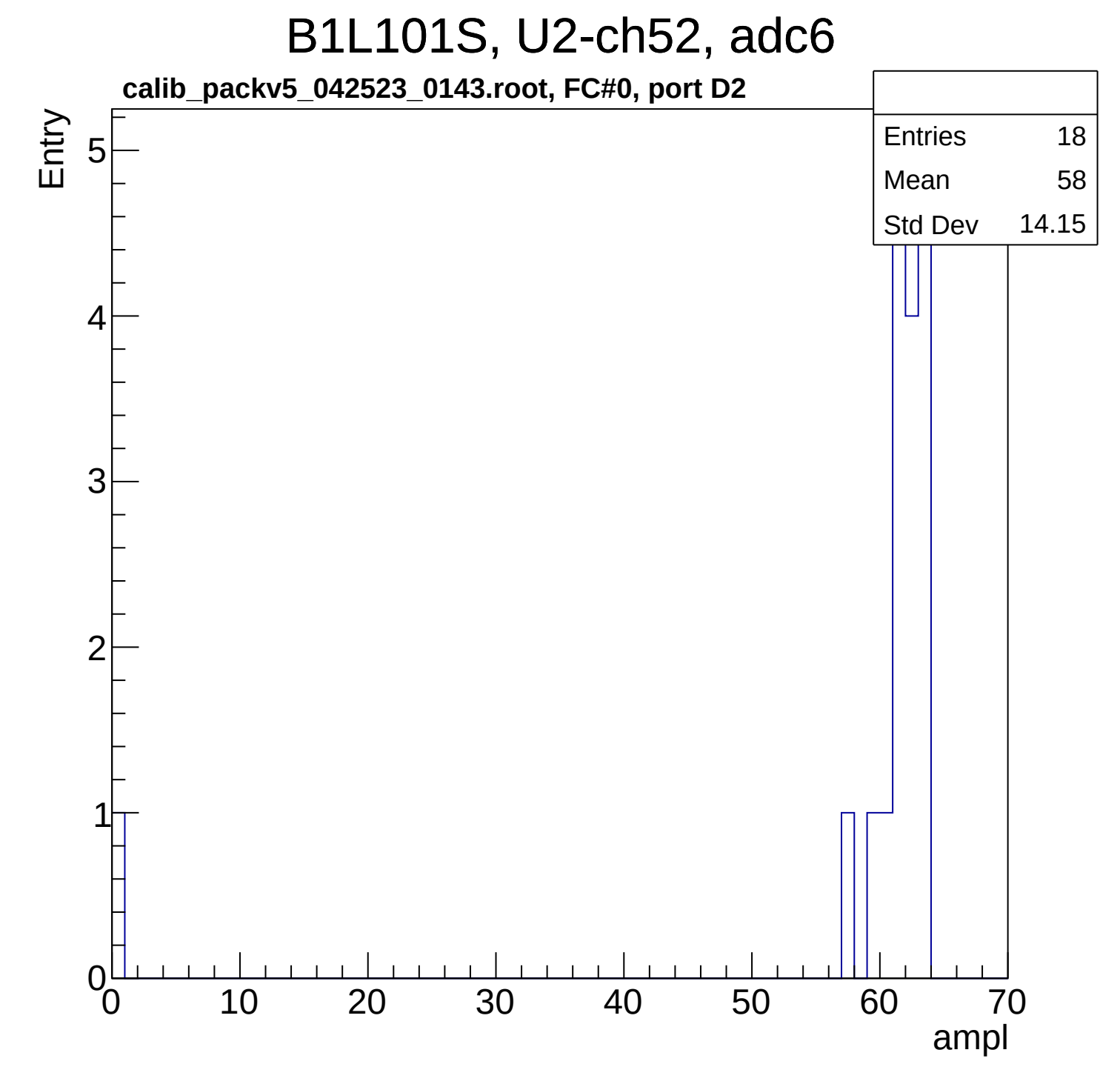

B1L101S, U2-ch52, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 35.41
Std Dev 3.82
Gaus mean : 35.5587
Gaus Width: 4.5591
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

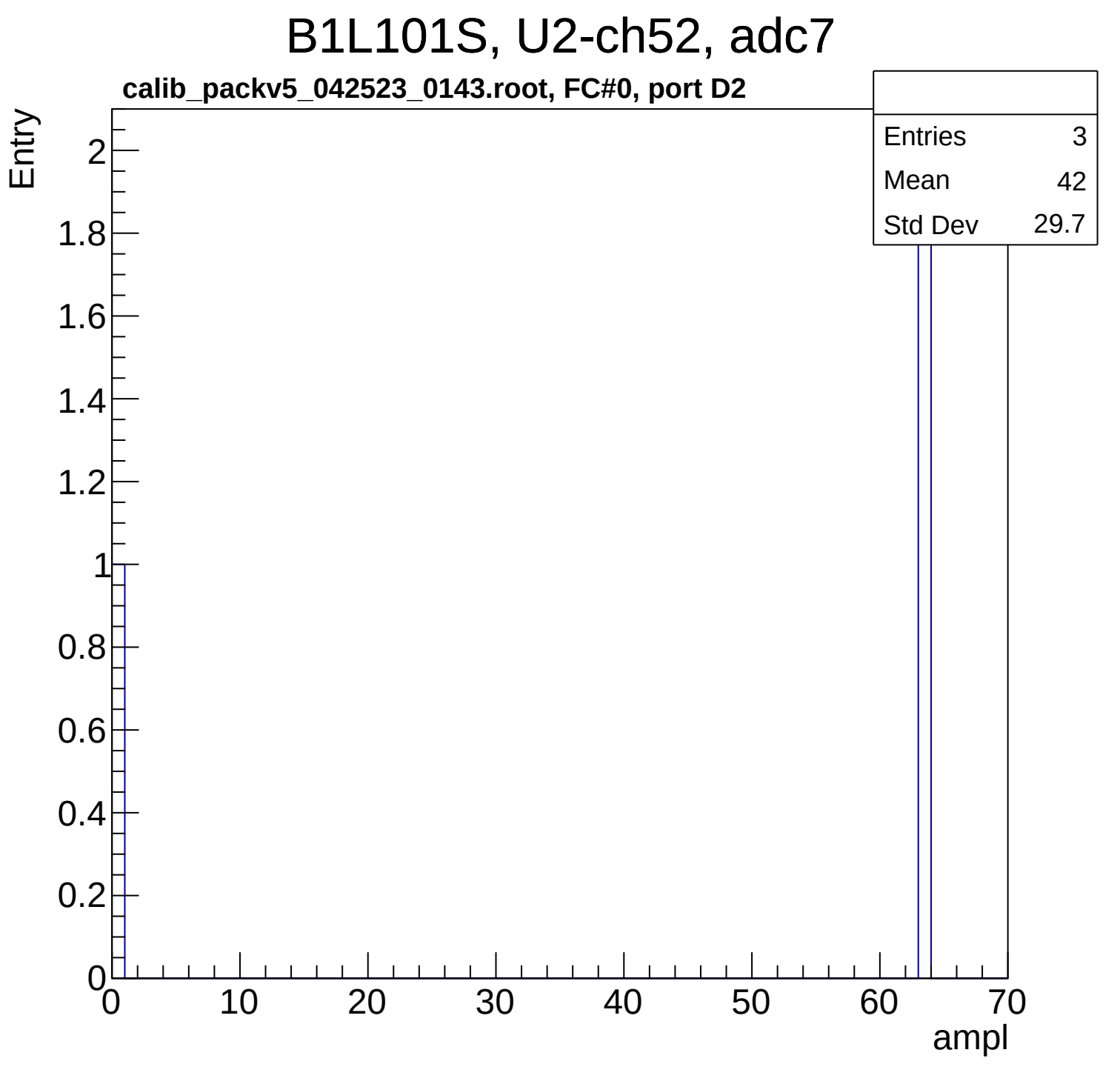

B1L101S, U2-ch52, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 41.73
Std Dev 3.78
Gaus mean : 42.3741
Gaus Width: 4.3241
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

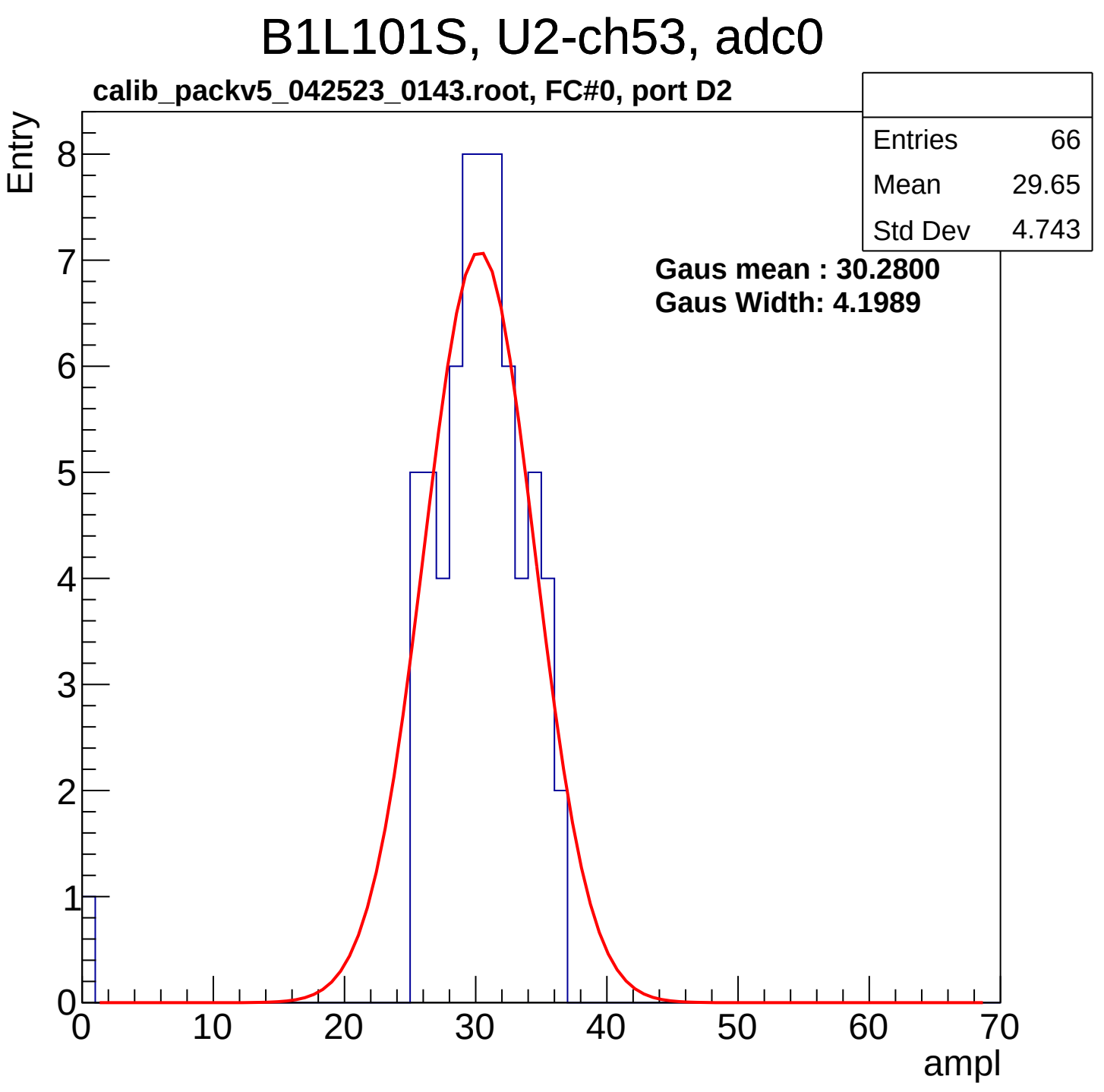

B1L101S, U2-ch52, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 48.06
Std Dev 3.385
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

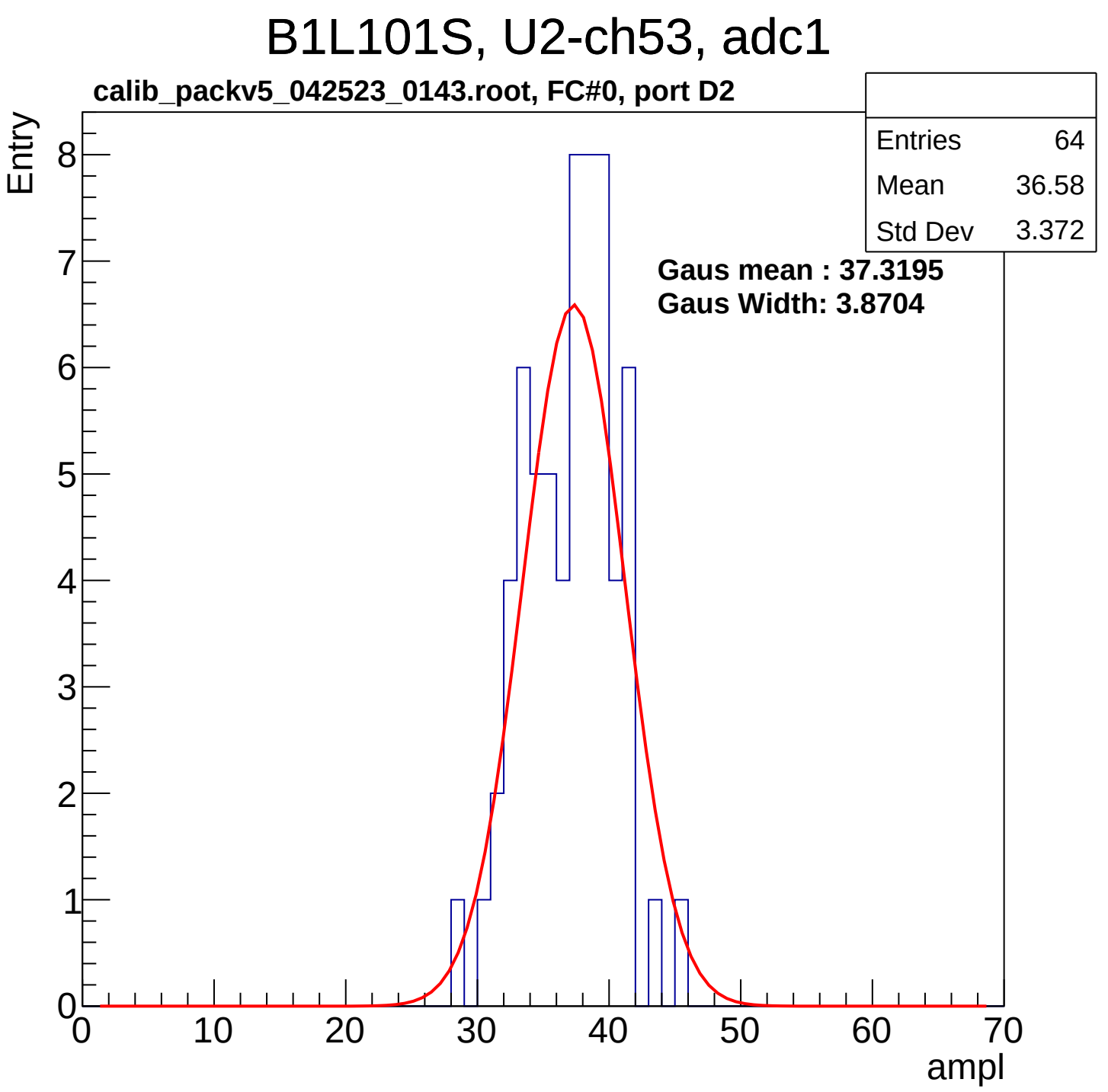

B1L101S, U2-ch52, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 53.49
Std Dev 3.227
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

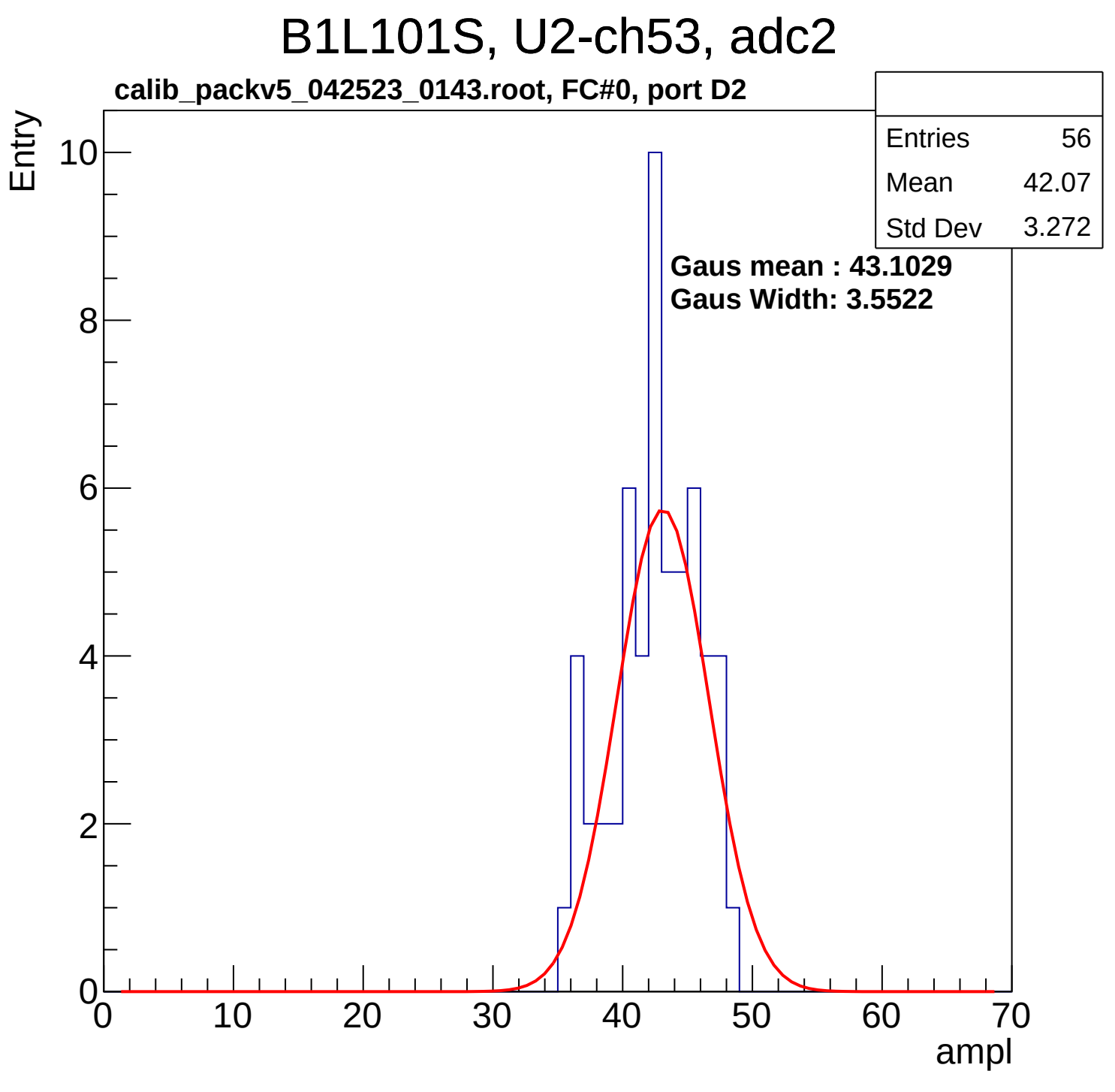

B1L101S, U2-ch52, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 58.96
Std Dev 2.525
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

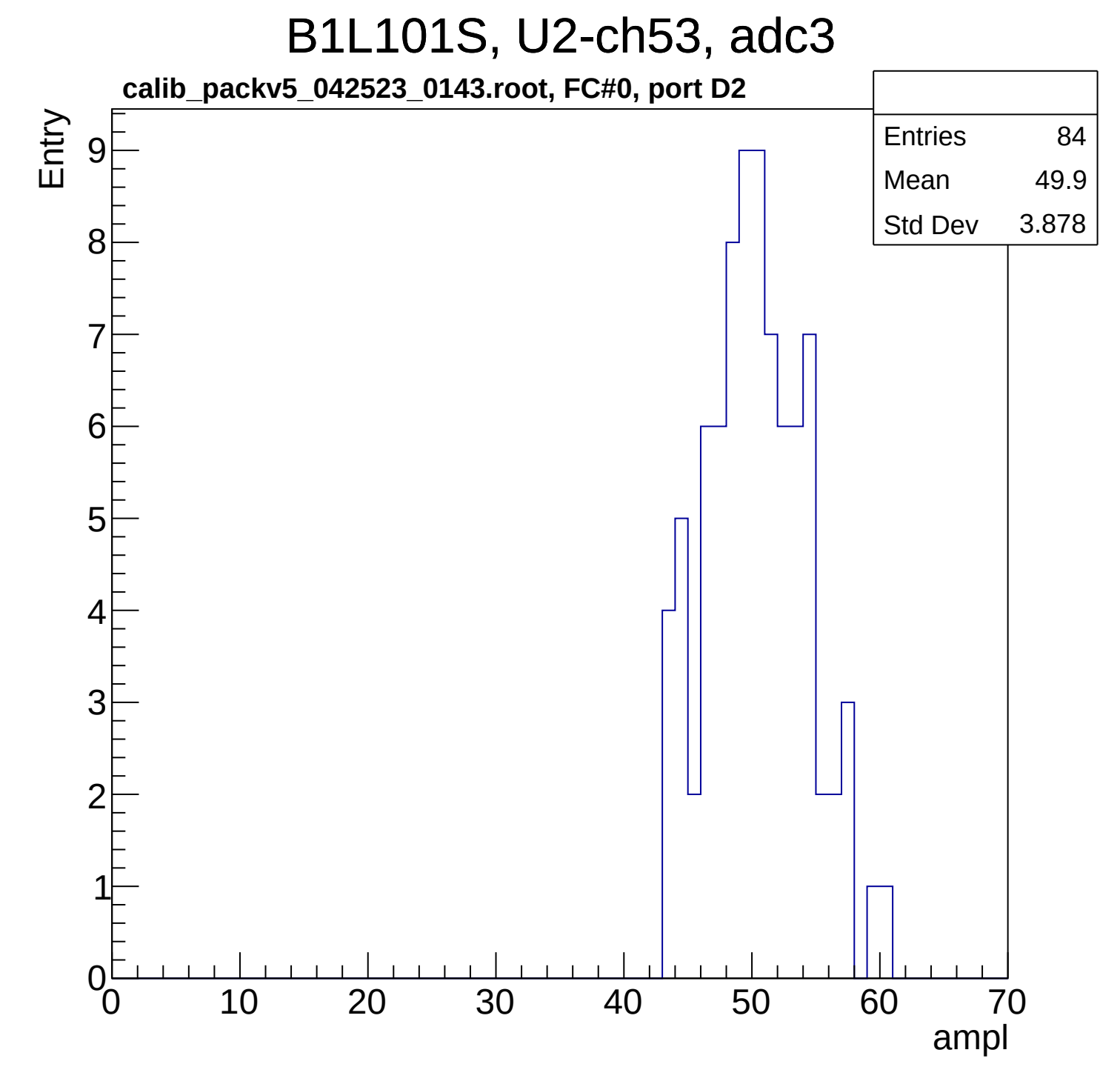

B1L101S, U2-ch52, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 18
Mean 58
Std Dev 14.15
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

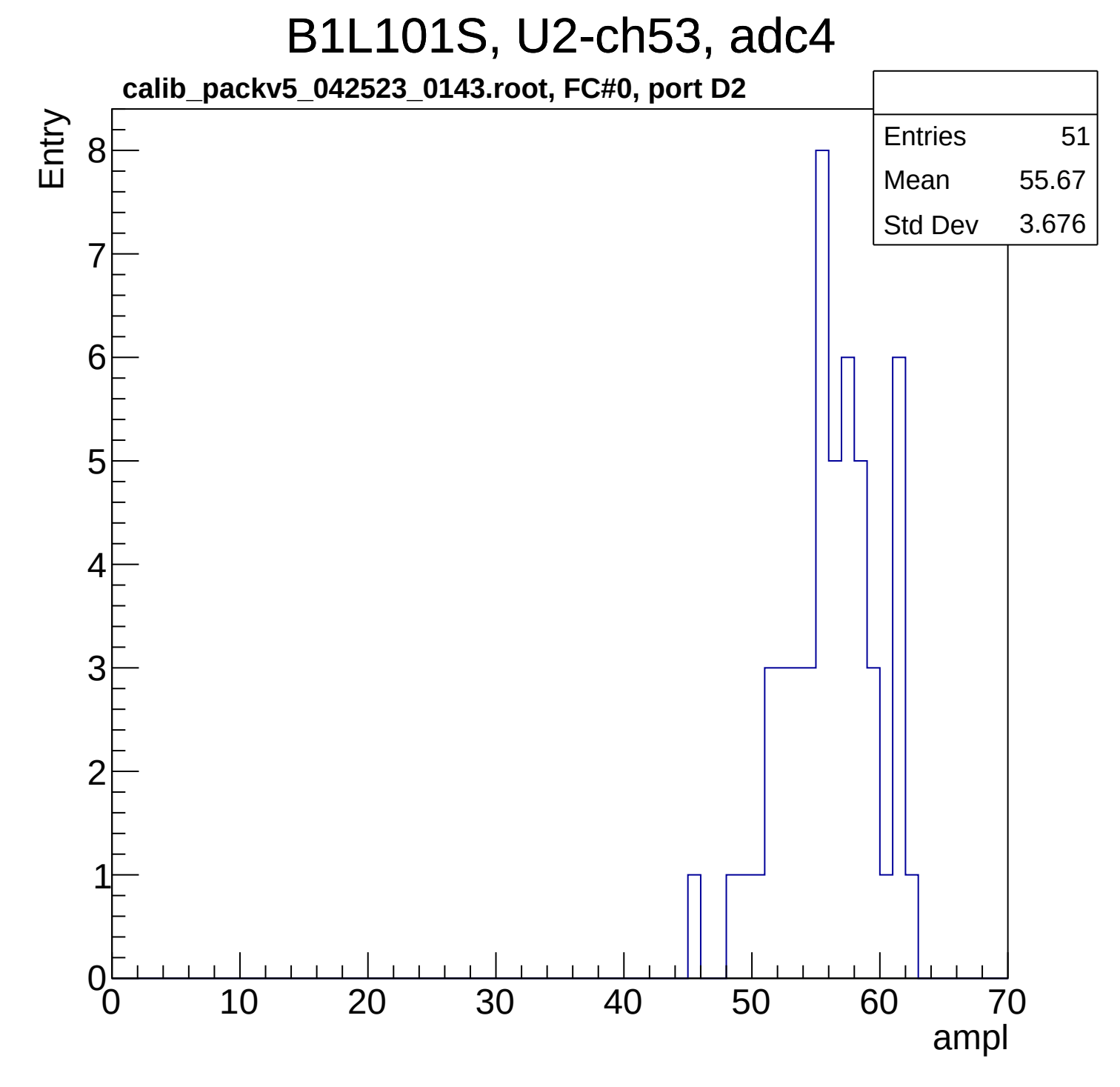

B1L101S, U2-ch52, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 42
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

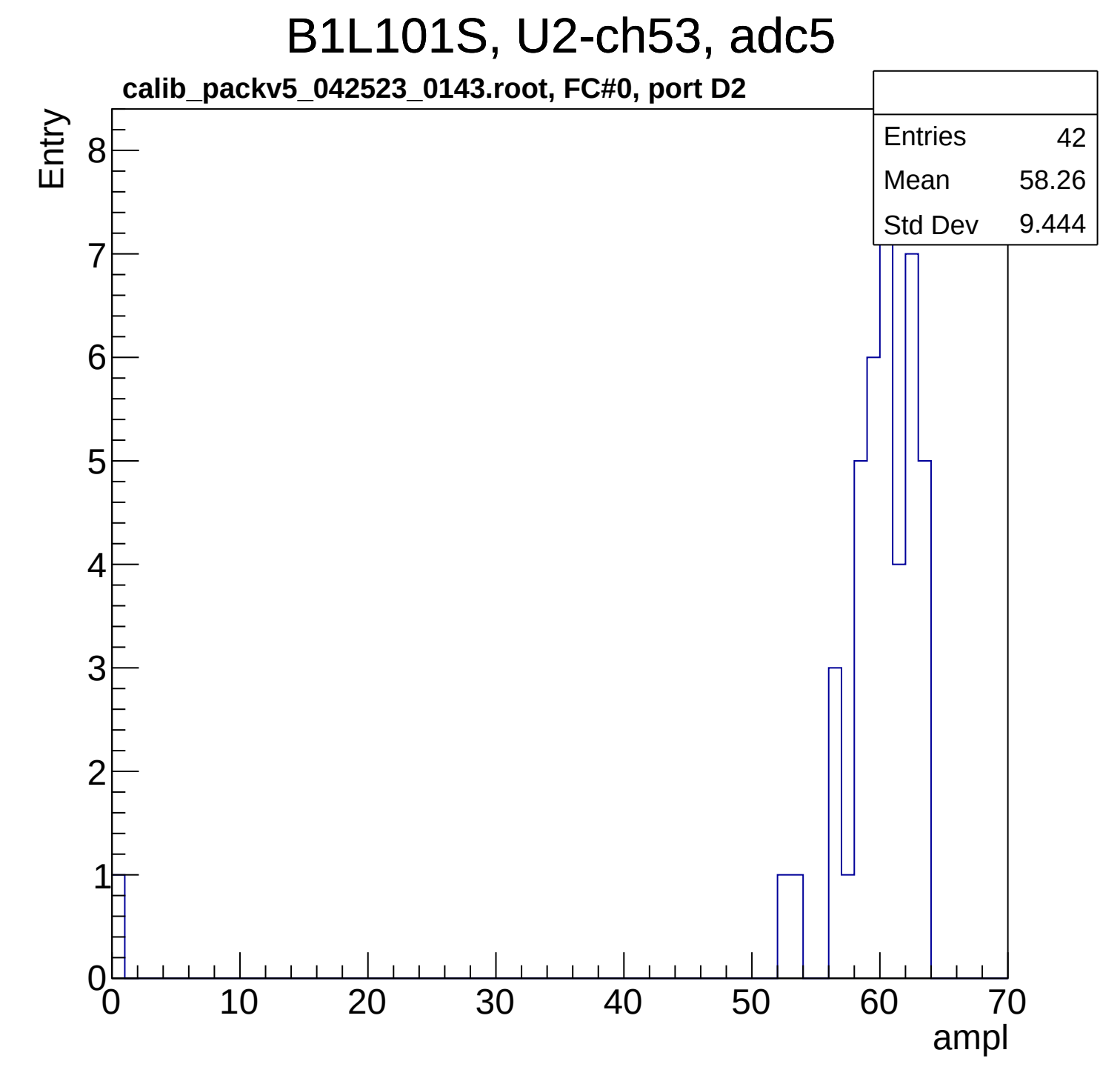

B1L101S, U2-ch53, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 29.65
Std Dev 4.743
Gaus mean : 30.2800
Gaus Width: 4.1989
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

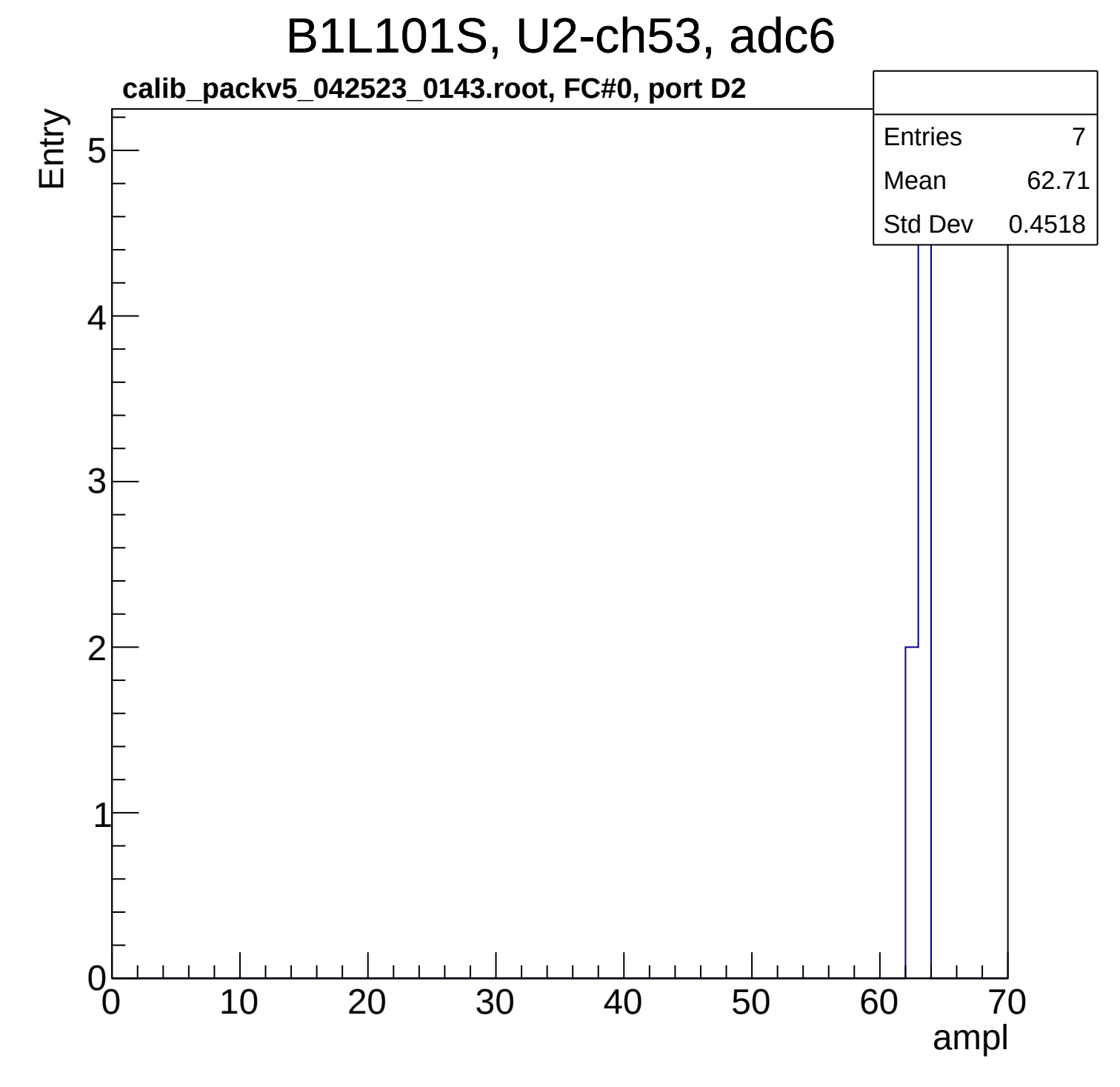

B1L101S, U2-ch53, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 36.58
Std Dev 3.372
Gaus mean : 37.3195
Gaus Width: 3.8704
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

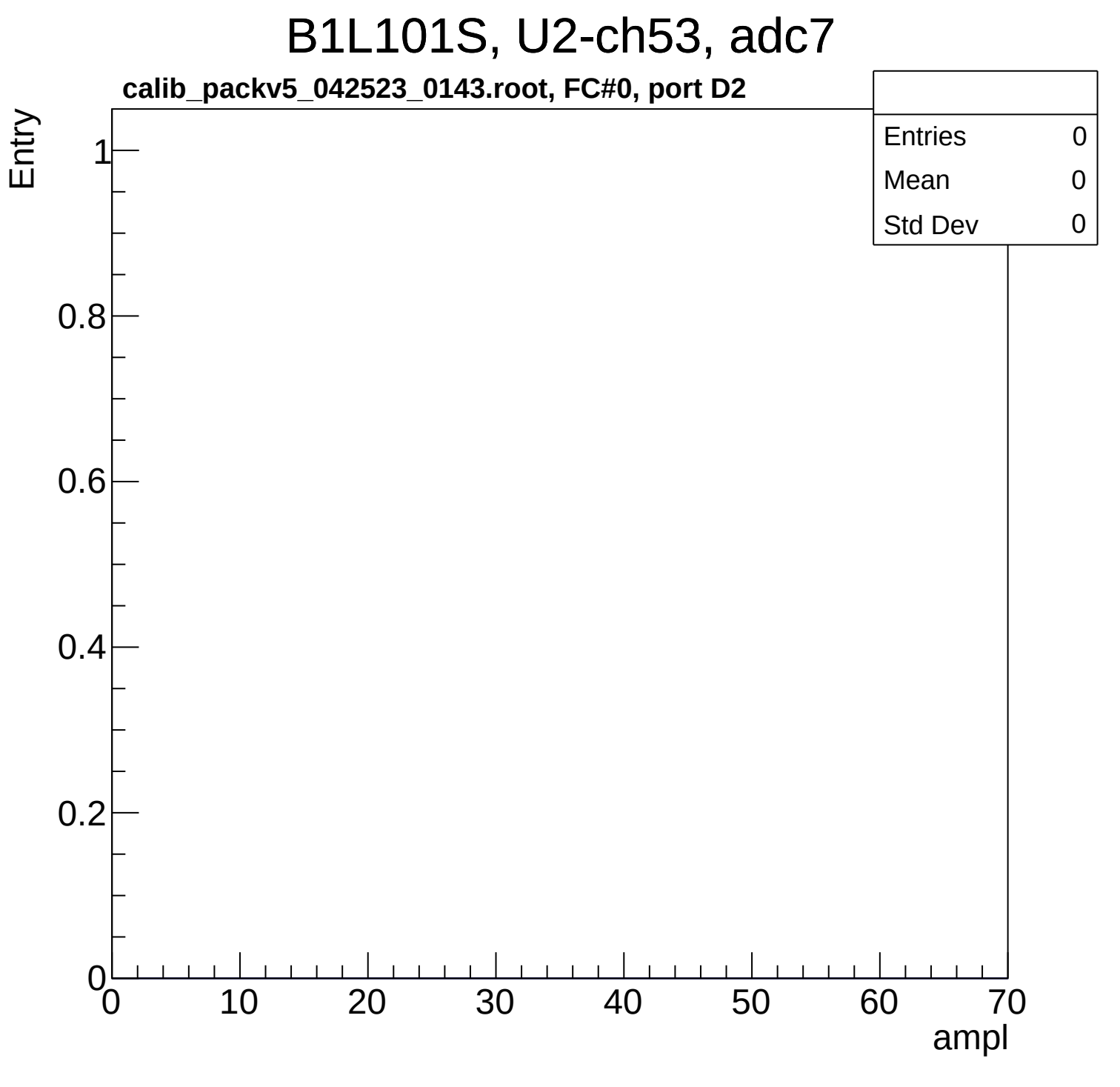

B1L101S, U2-ch53, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 42.07
Std Dev 3.272
Gaus mean : 43.1029
Gaus Width: 3.5522
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

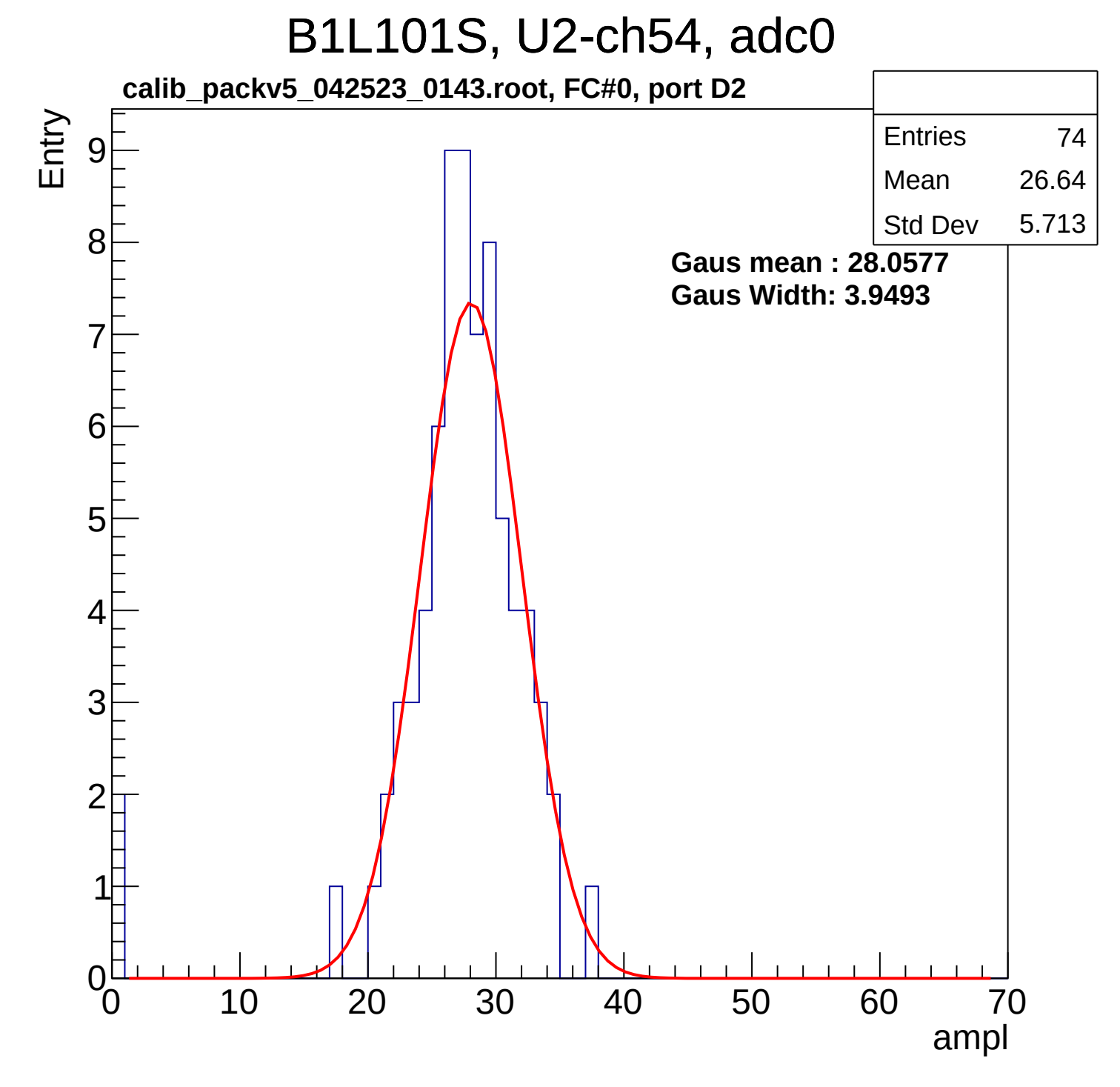

B1L101S, U2-ch53, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 84
Mean 49.9
Std Dev 3.878
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

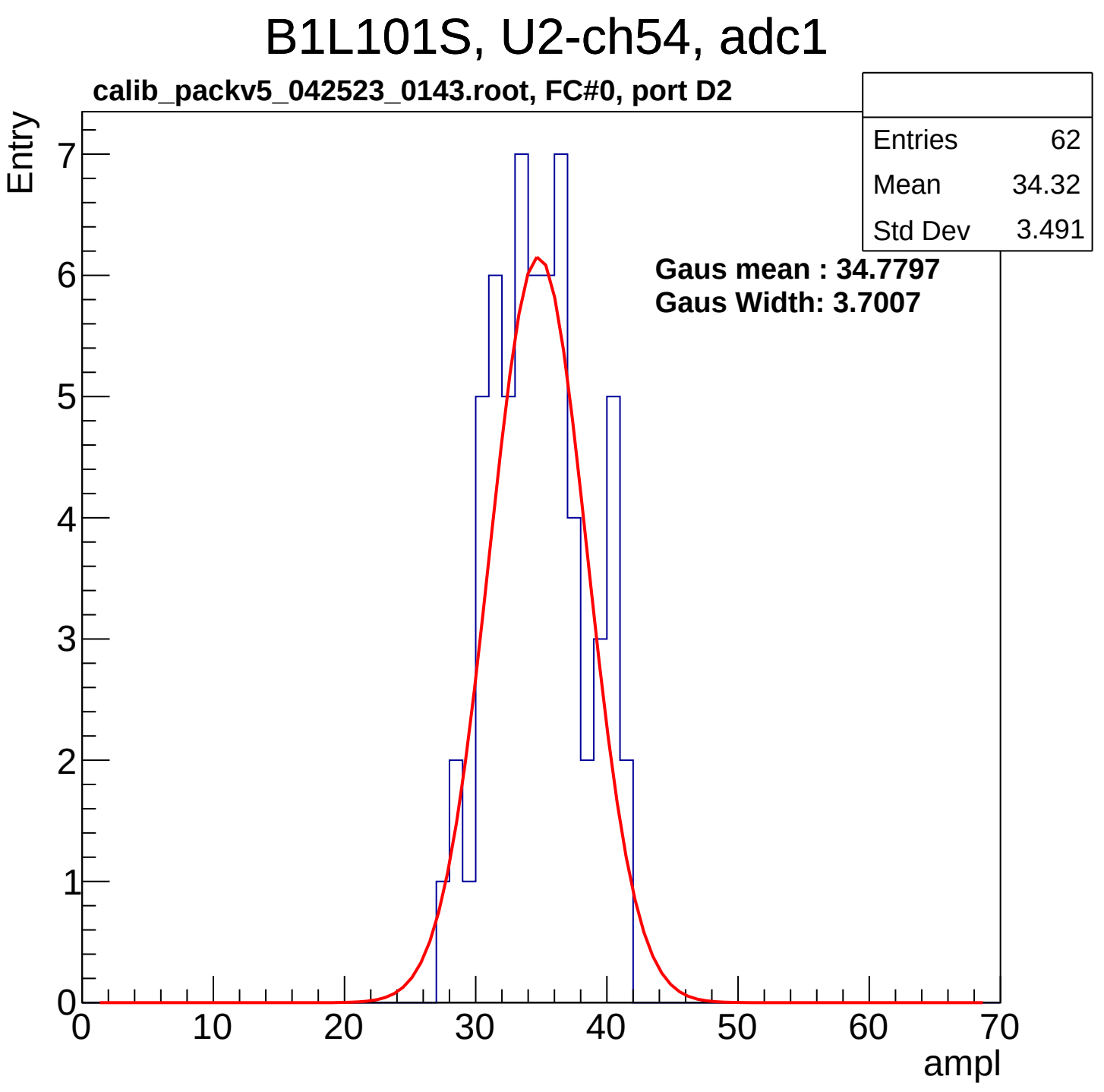

B1L101S, U2-ch53, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 55.67
Std Dev 3.676
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

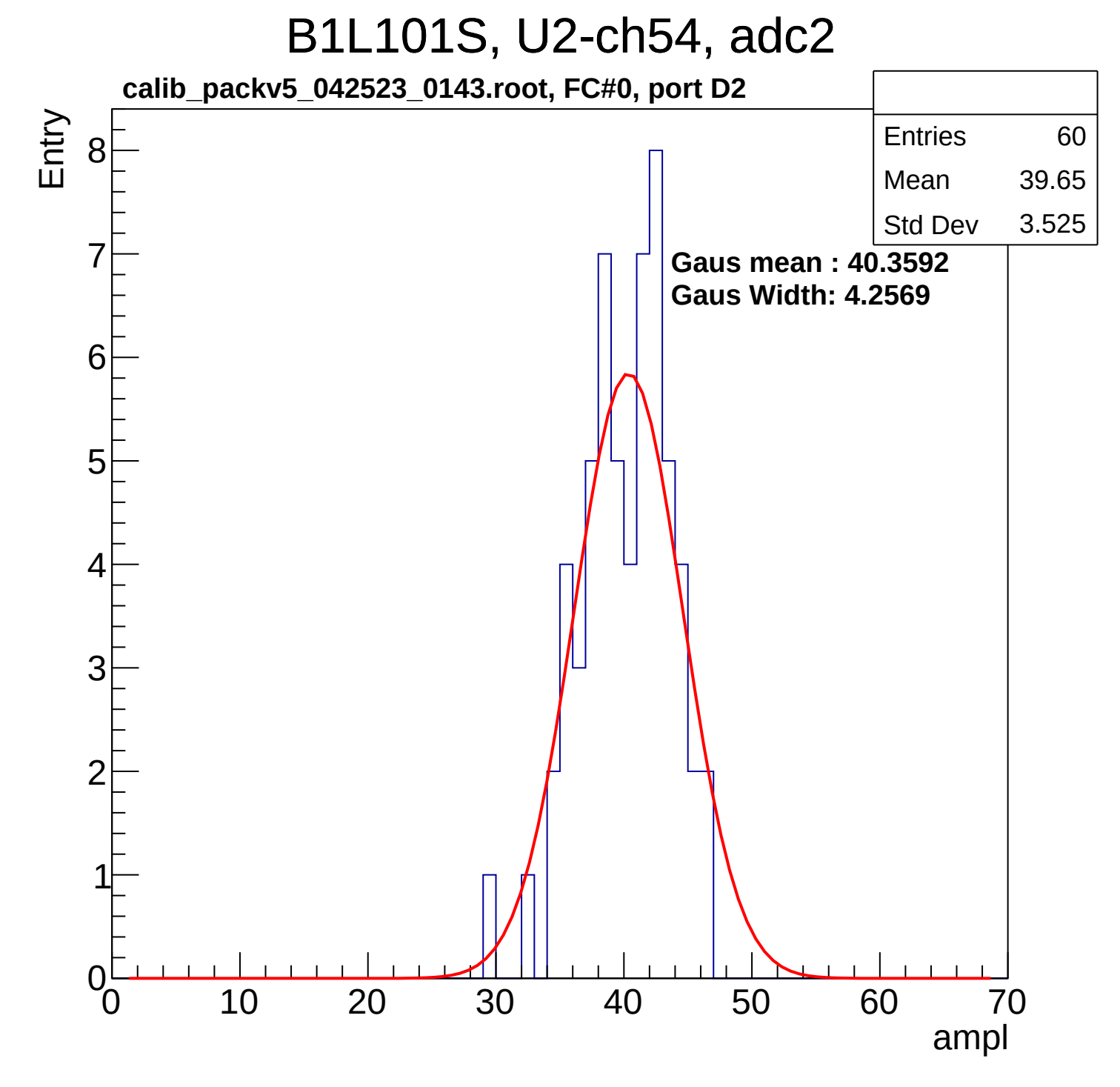

B1L101S, U2-ch53, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 58.26
Std Dev 9.444
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

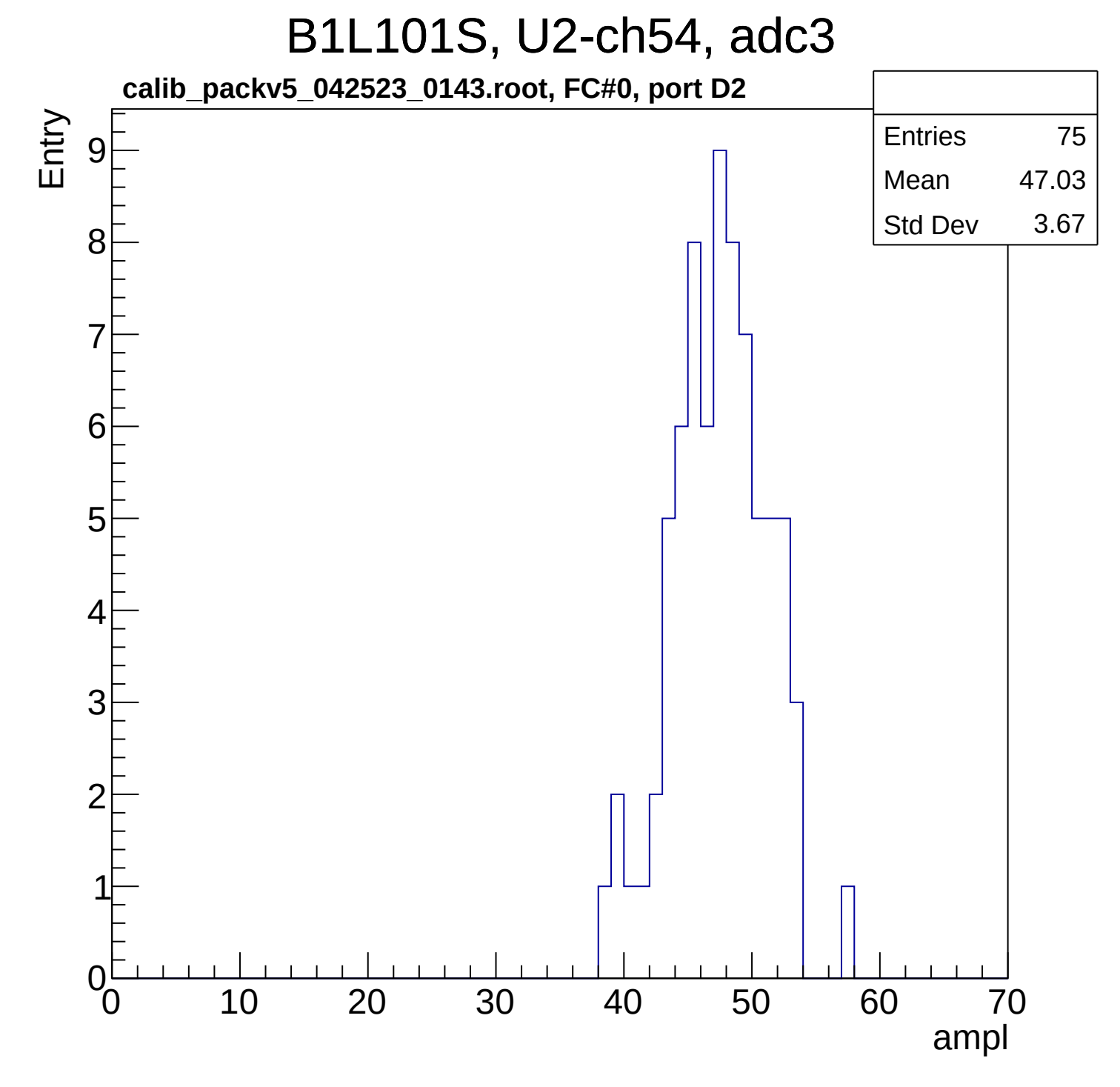

B1L101S, U2-ch53, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 62.71
Std Dev 0.4518
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

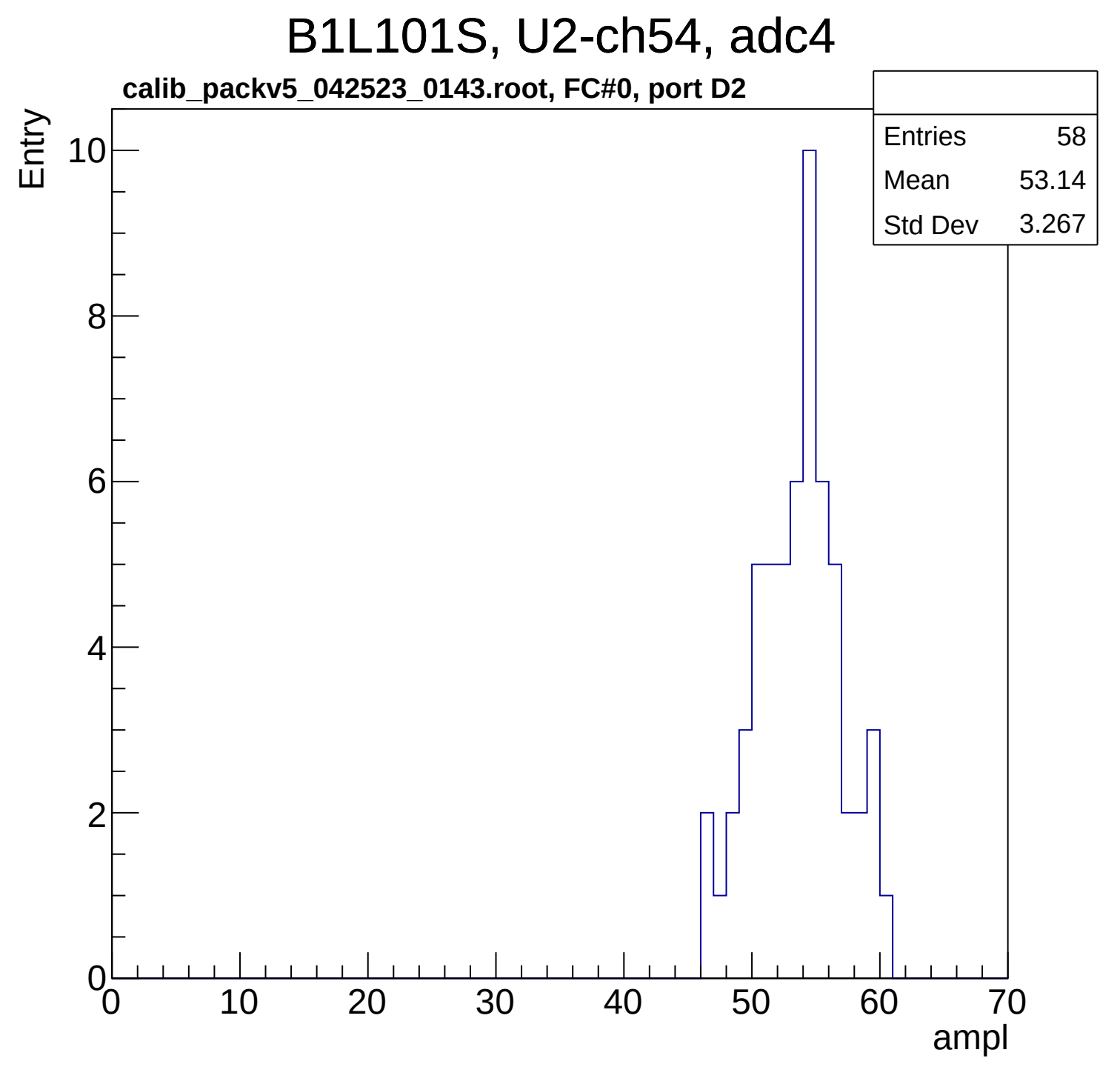

B1L101S, U2-ch53, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

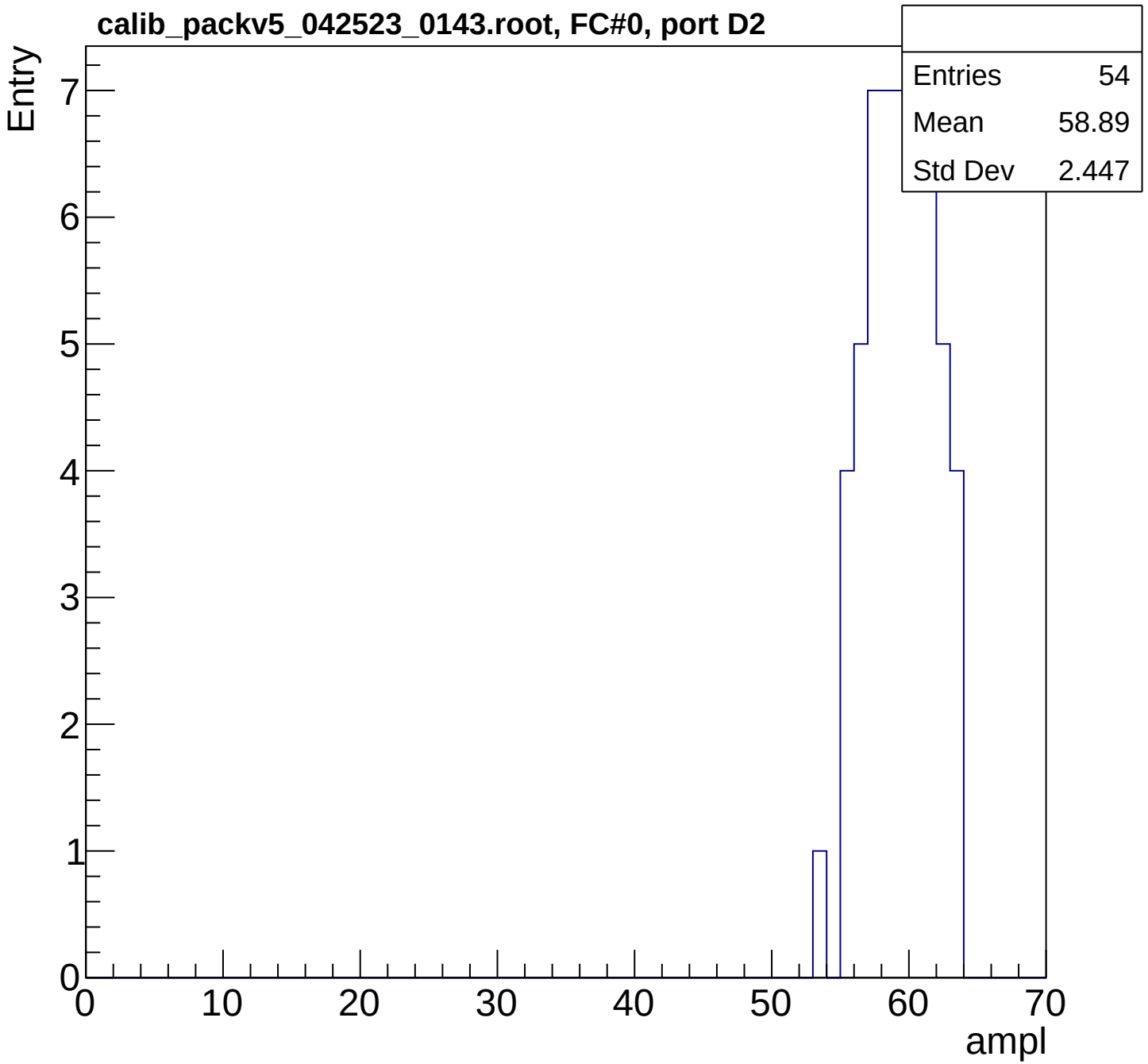

B1L101S, U2-ch54, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 26.64
Std Dev 5.713
Gaus mean : 28.0577
Gaus Width: 3.9493
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

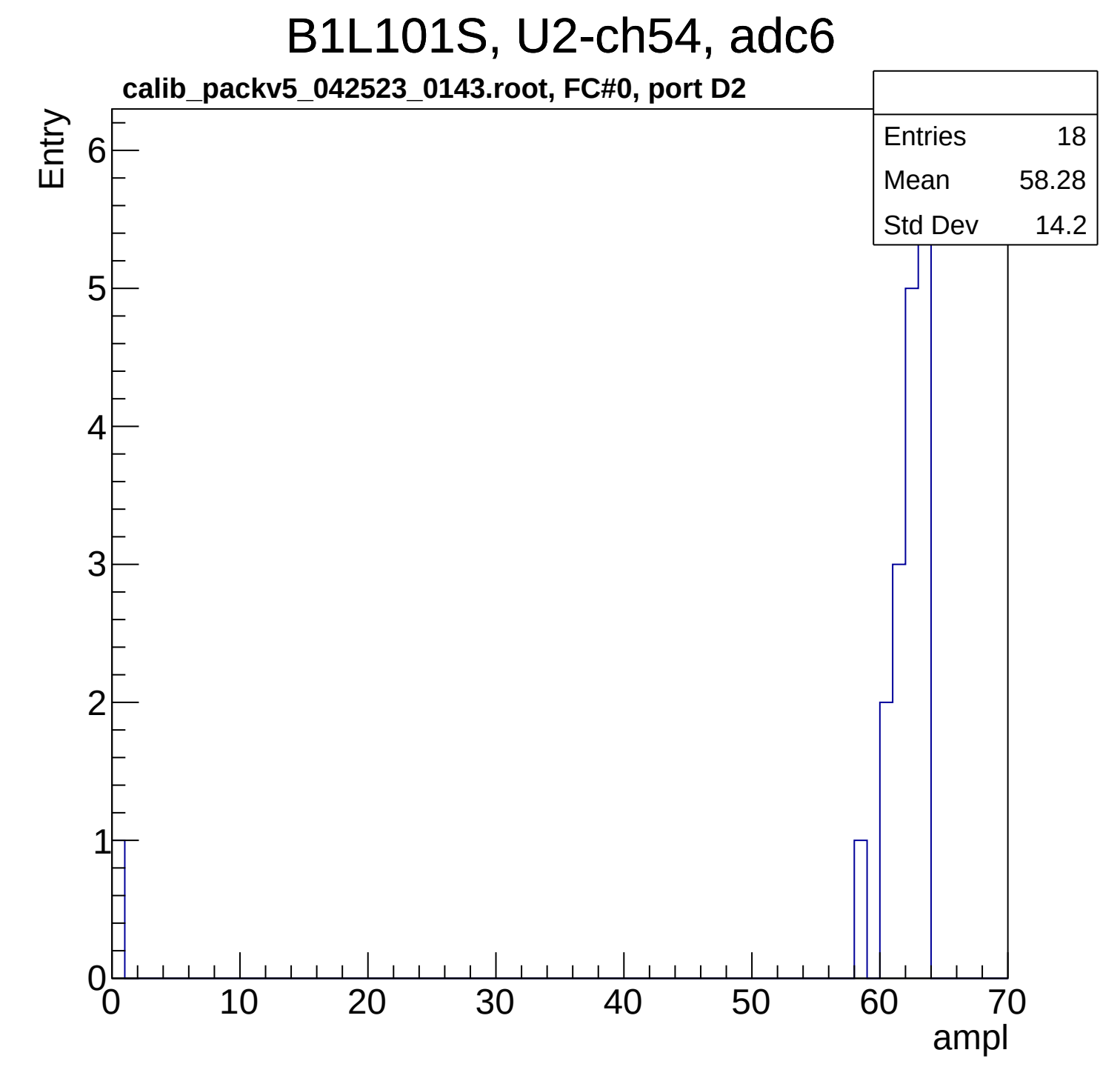

B1L101S, U2-ch54, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 34.32
Std Dev 3.491
Gaus mean : 34.7797
Gaus Width: 3.7007
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

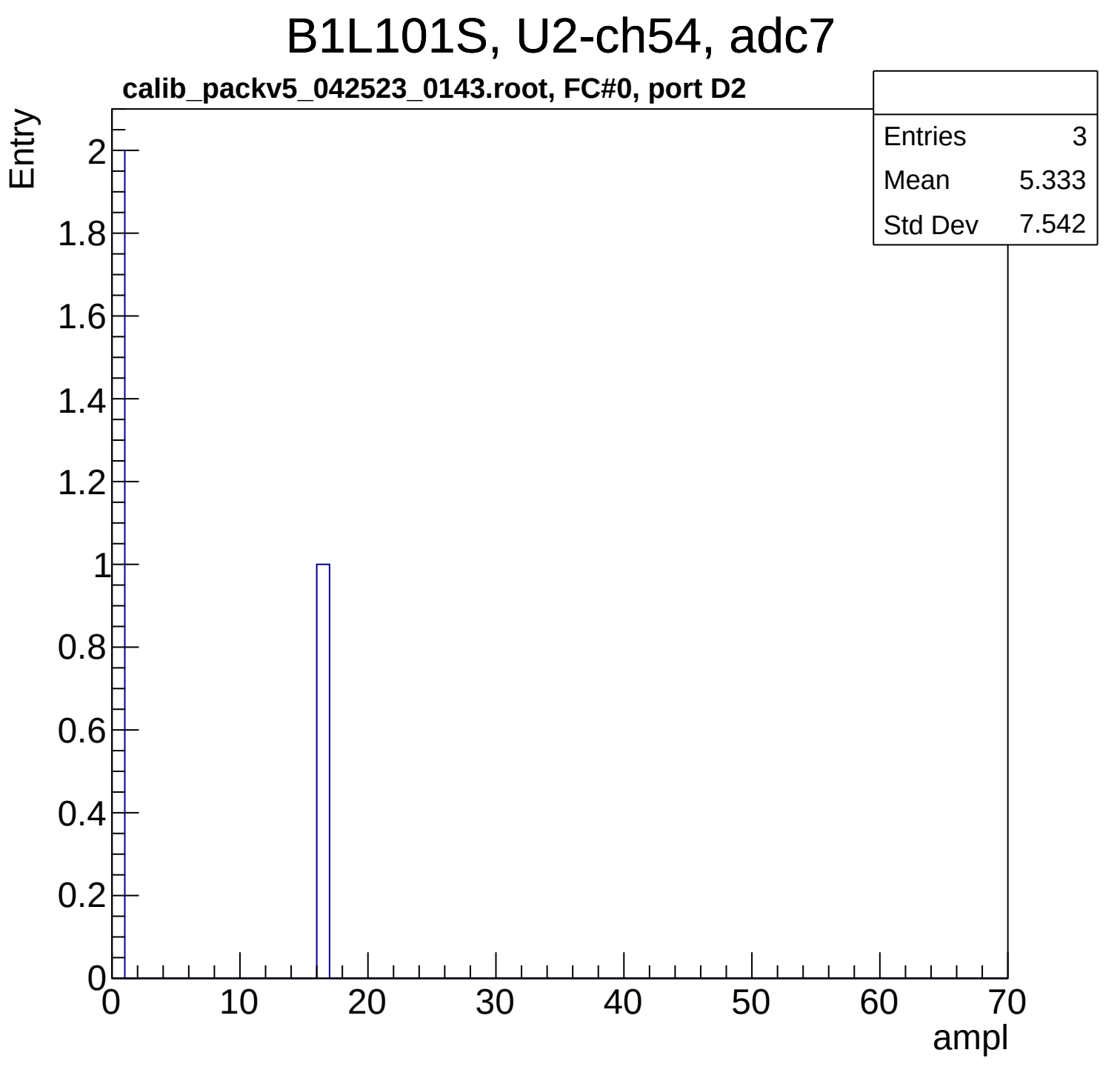

B1L101S, U2-ch54, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 39.65
Std Dev 3.525
Gaus mean : 40.3592
Gaus Width: 4.2569
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

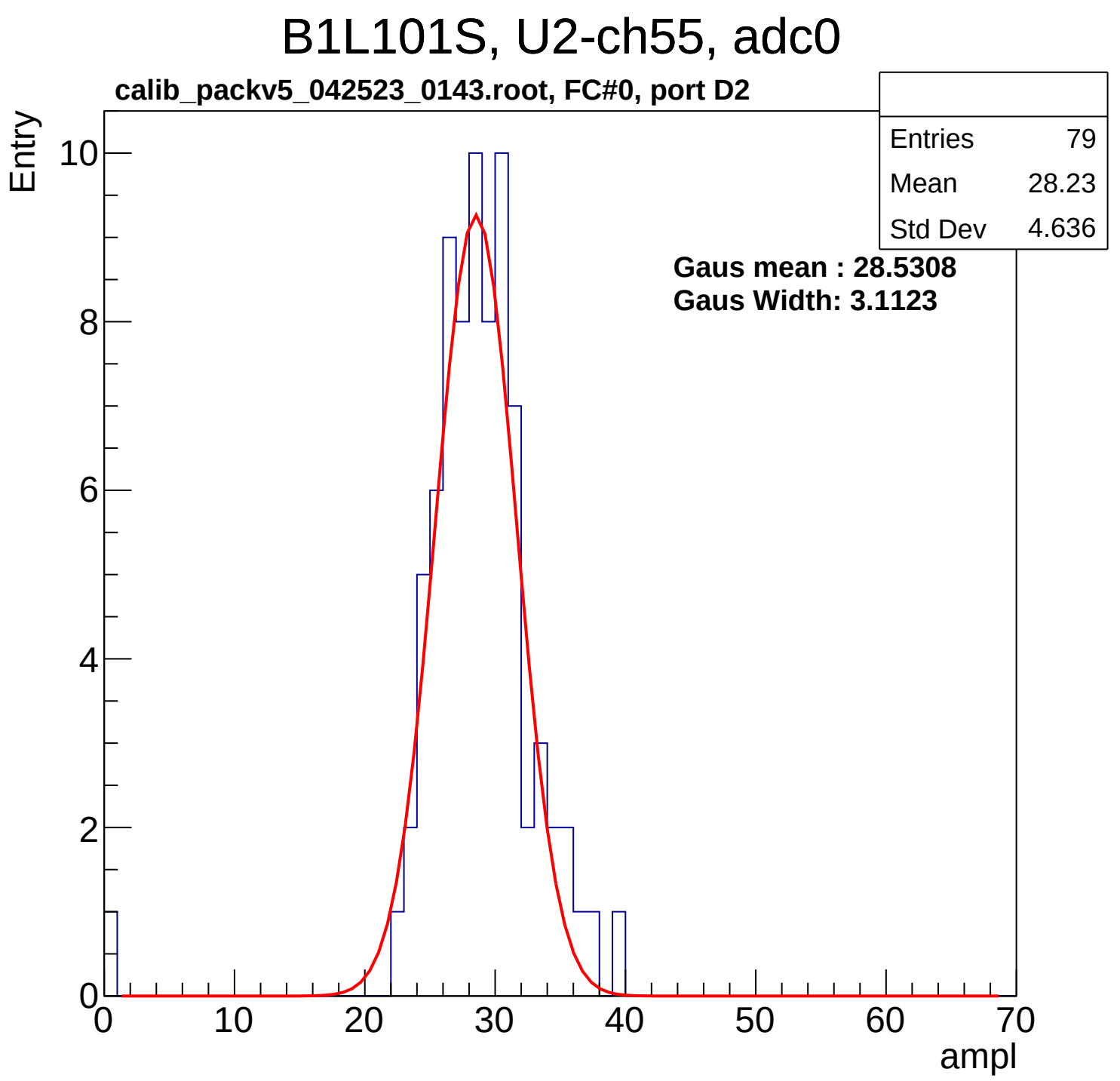

B1L101S, U2-ch54, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 47.03
Std Dev 3.67
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

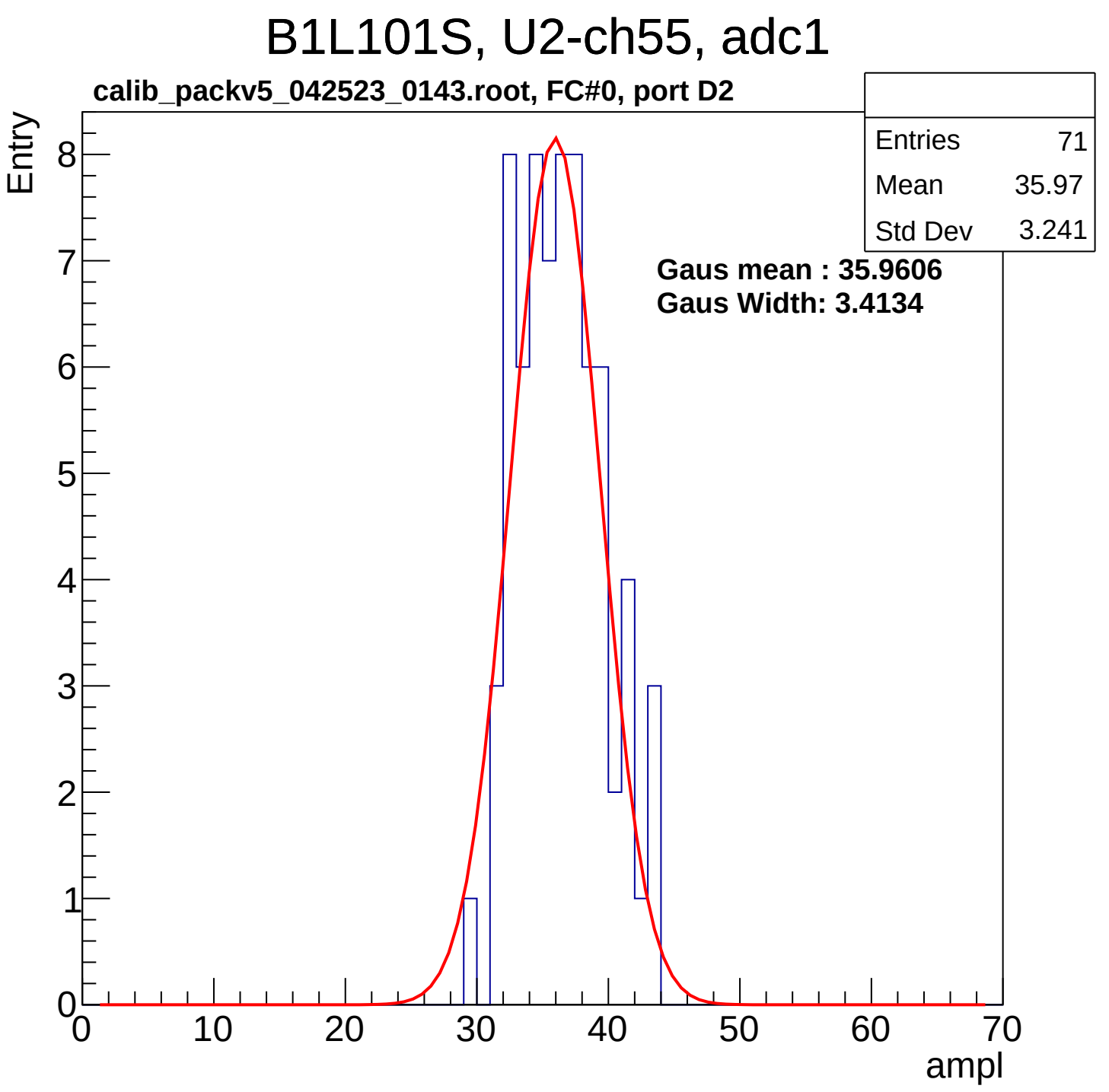

B1L101S, U2-ch54, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 53.14
Std Dev 3.267
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

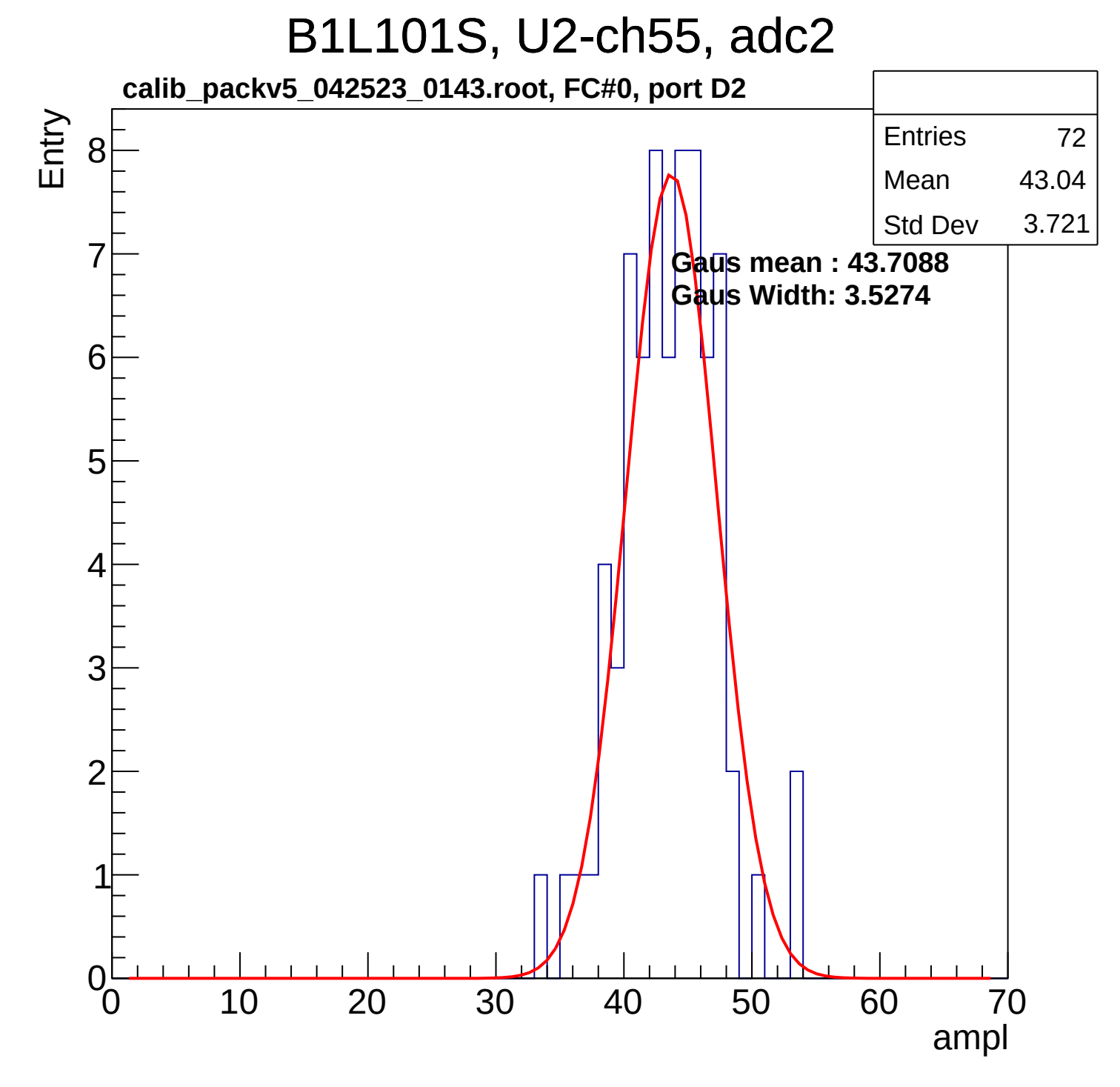

B1L101S, U2-ch54, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 58.89
Std Dev 2.447
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

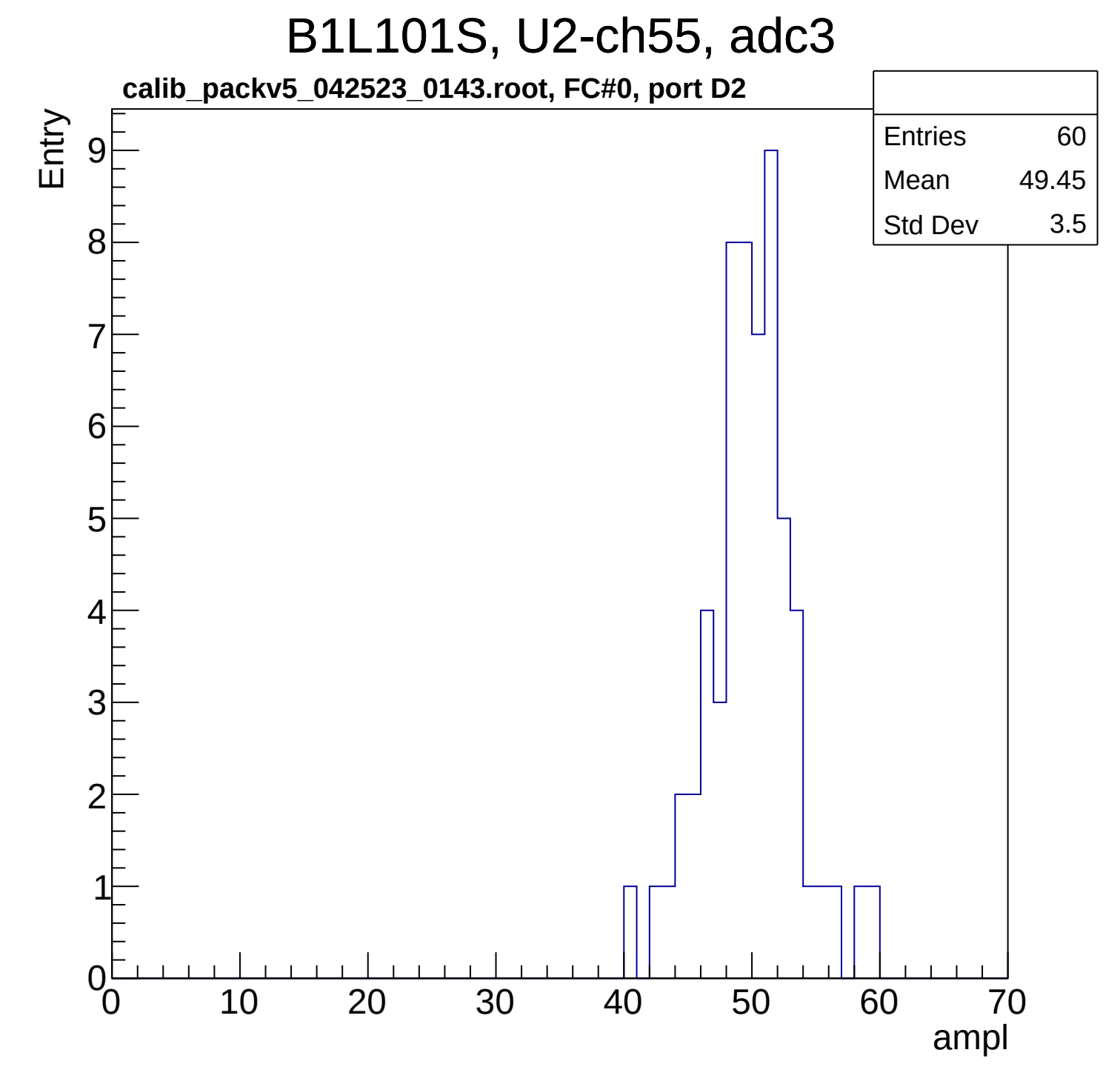

B1L101S, U2-ch54, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 18
Mean 58.28
Std Dev 14.2
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

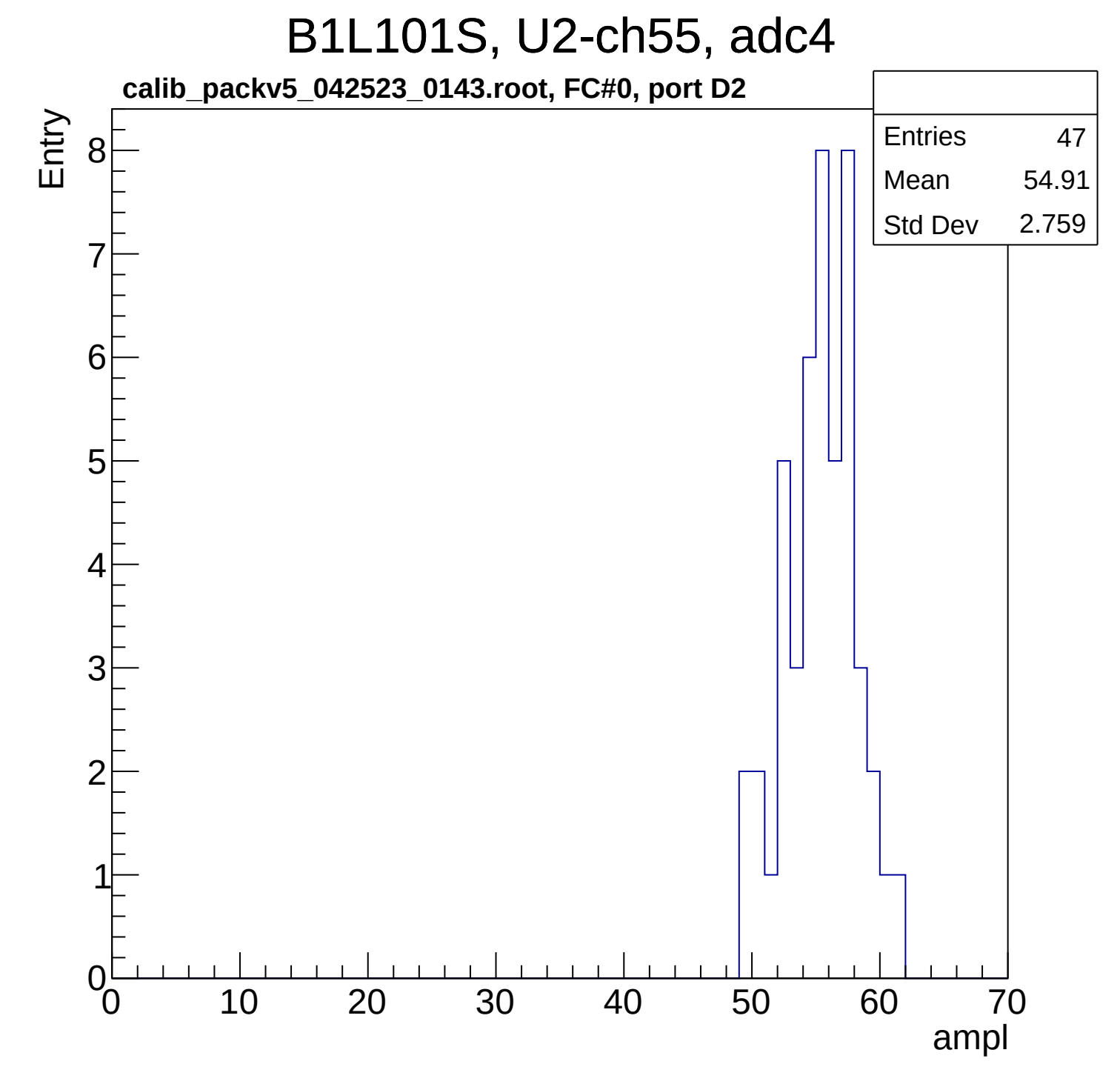

B1L101S, U2-ch54, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 5.333
Std Dev 7.542
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

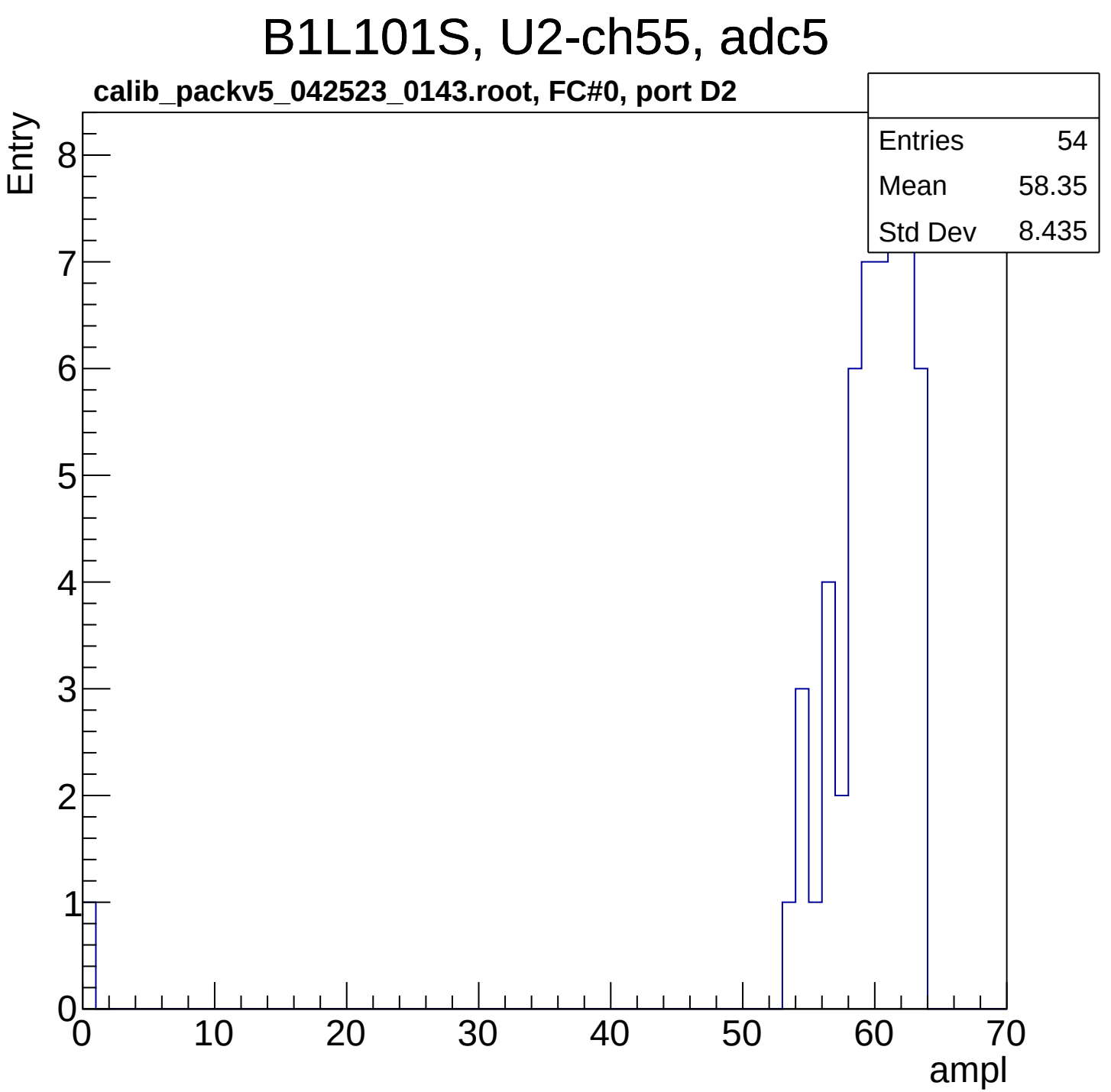

B1L101S, U2-ch55, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 28.23
Std Dev 4.636
Gaus mean : 28.5308
Gaus Width: 3.1123
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

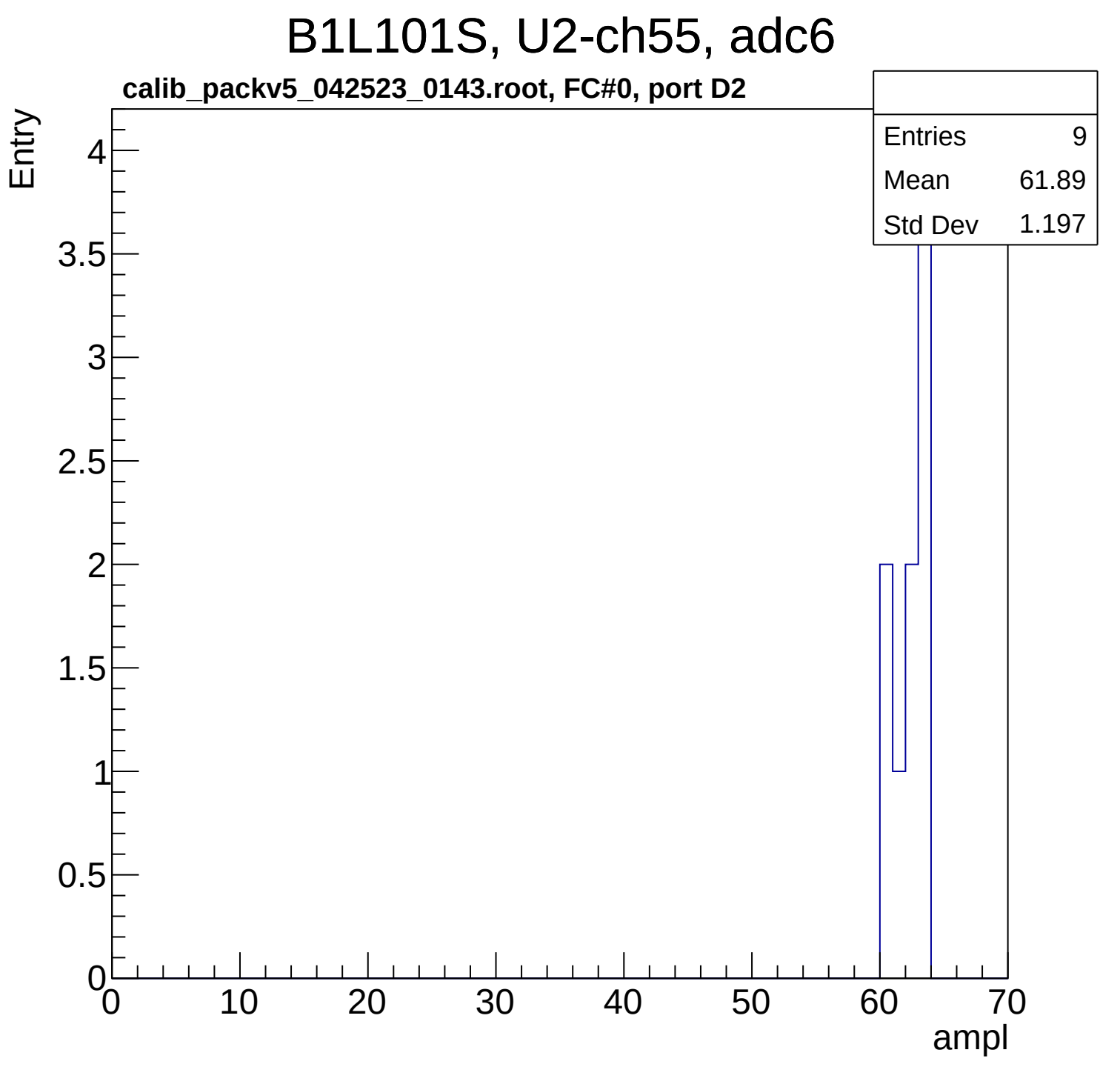

B1L101S, U2-ch55, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 35.97
Std Dev 3.241
Gaus mean : 35.9606
Gaus Width: 3.4134
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

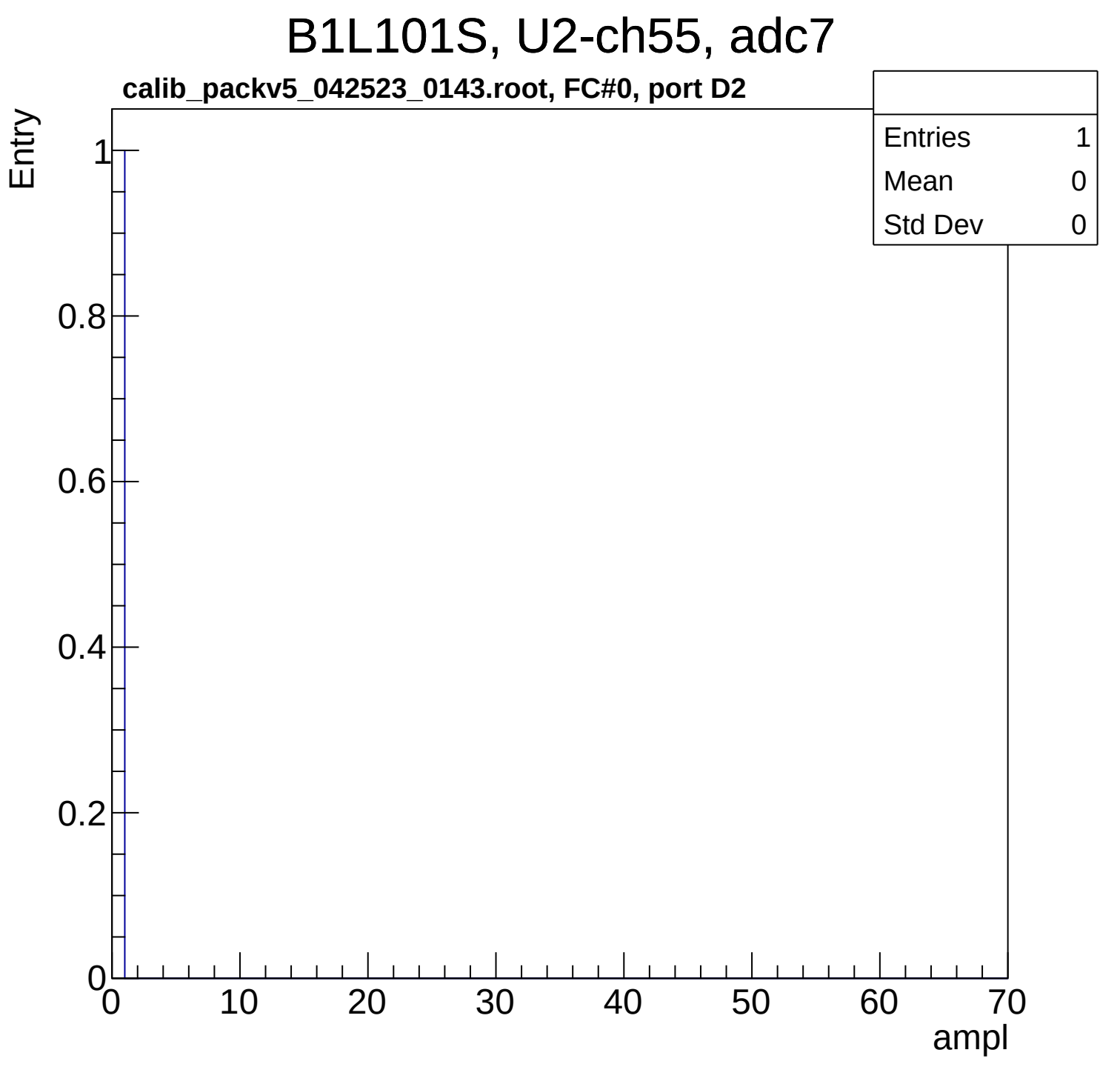

B1L101S, U2-ch55, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 43.04
Std Dev 3.721
Gaus mean : 43.7088
Gaus Width: 3.5274
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

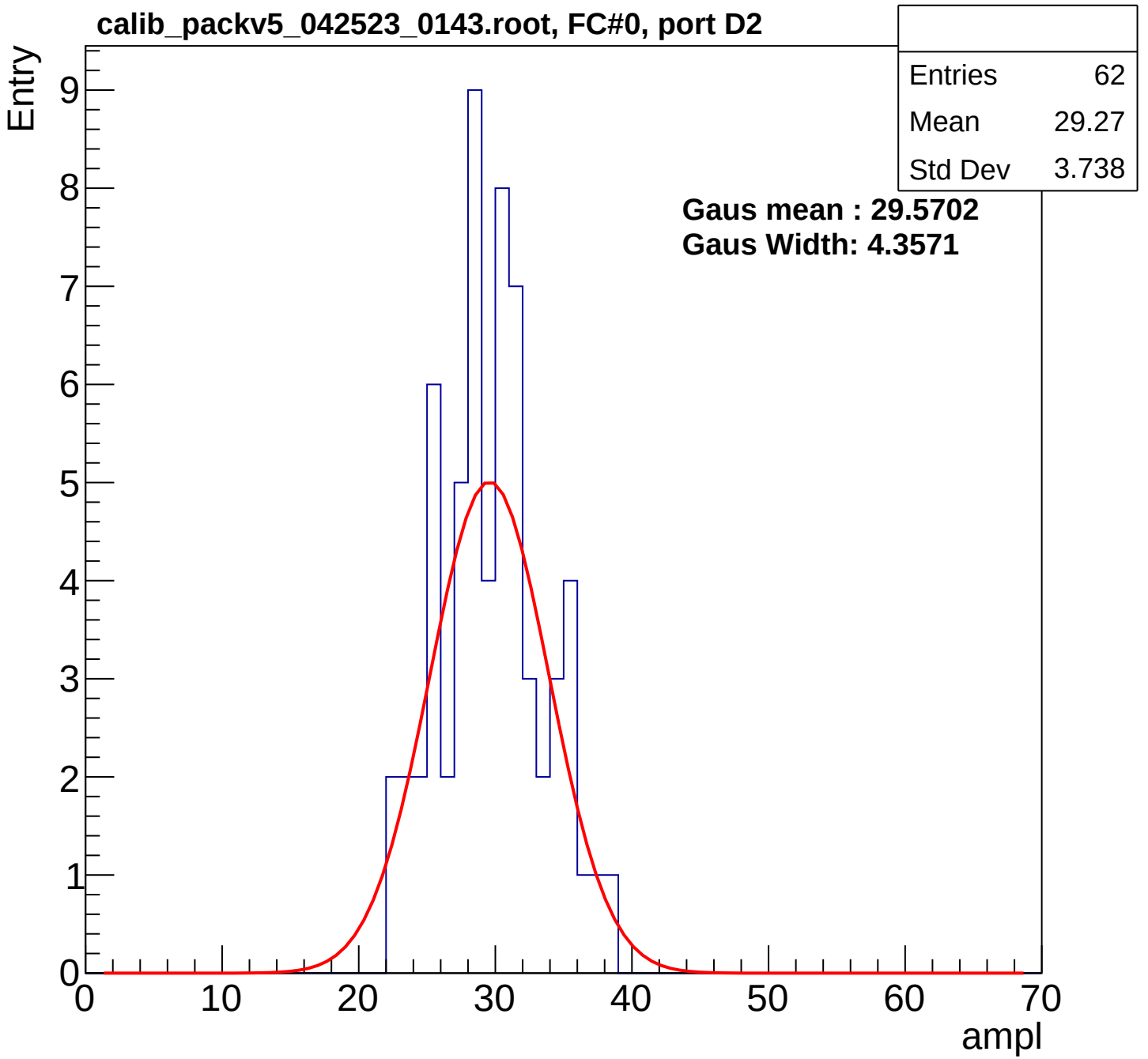

B1L101S, U2-ch55, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 49.45
Std Dev 3.5
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

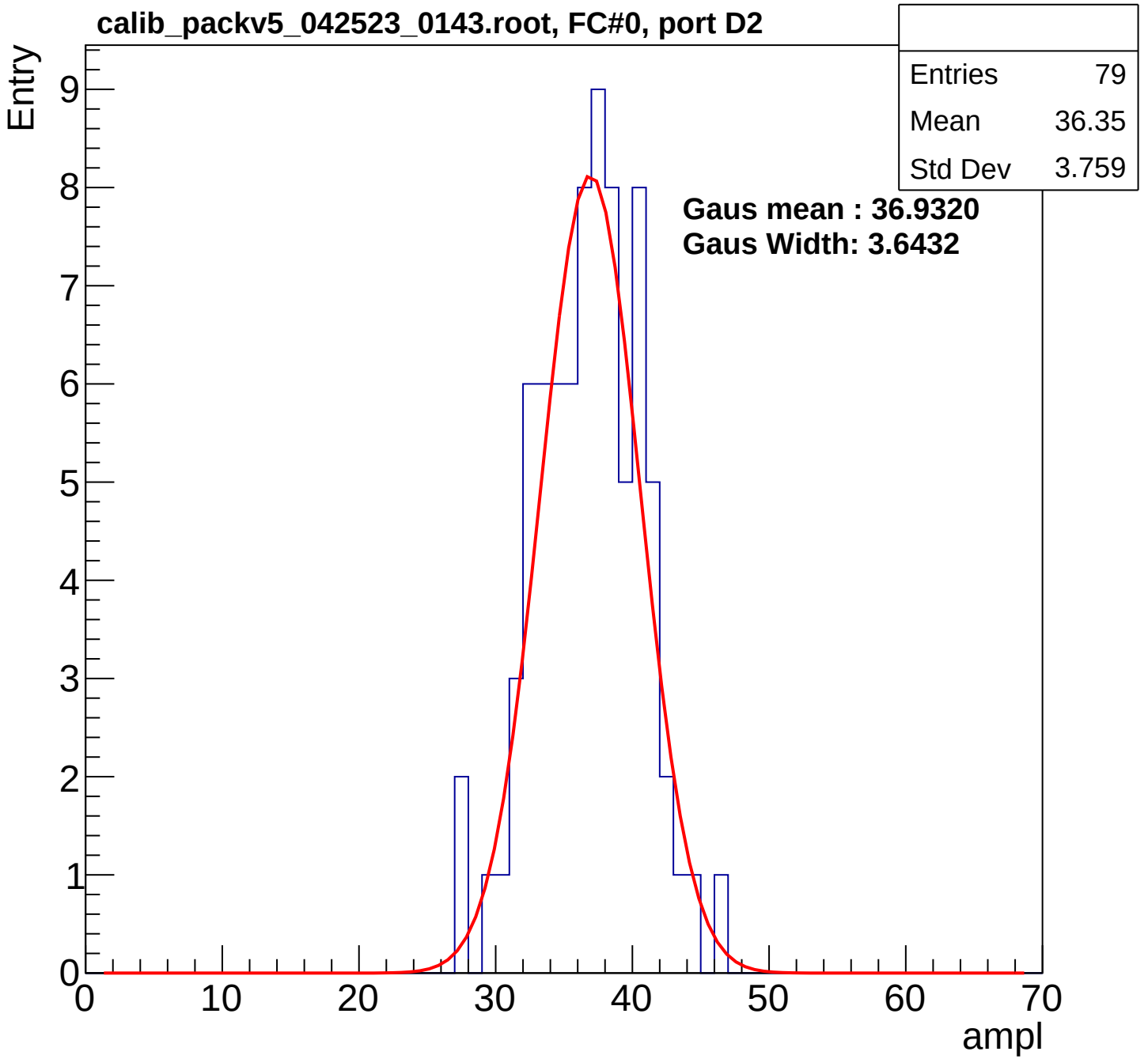

B1L101S, U2-ch55, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 54.91
Std Dev 2.759
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

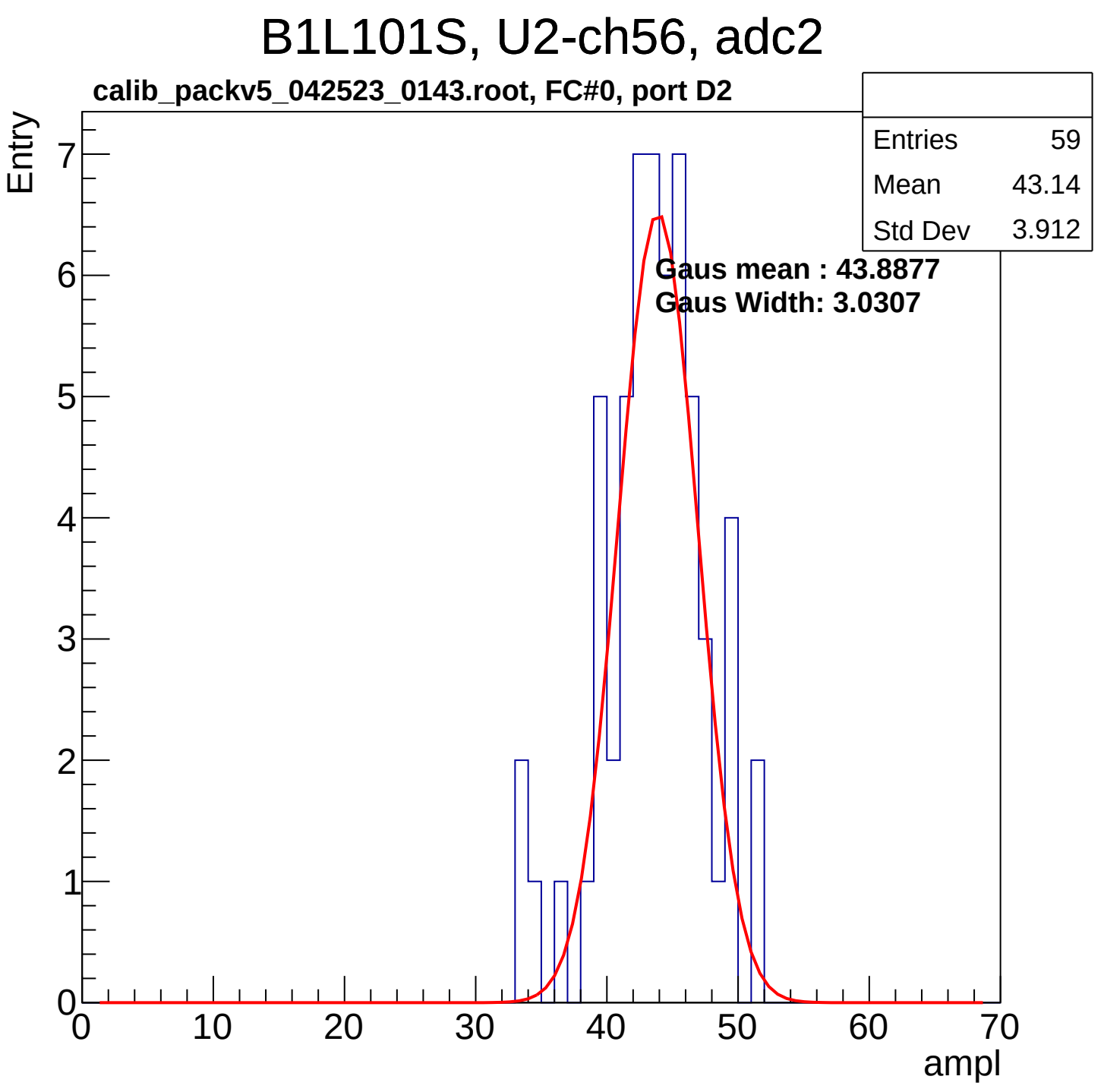

B1L101S, U2-ch55, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 58.35
Std Dev 8.435
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

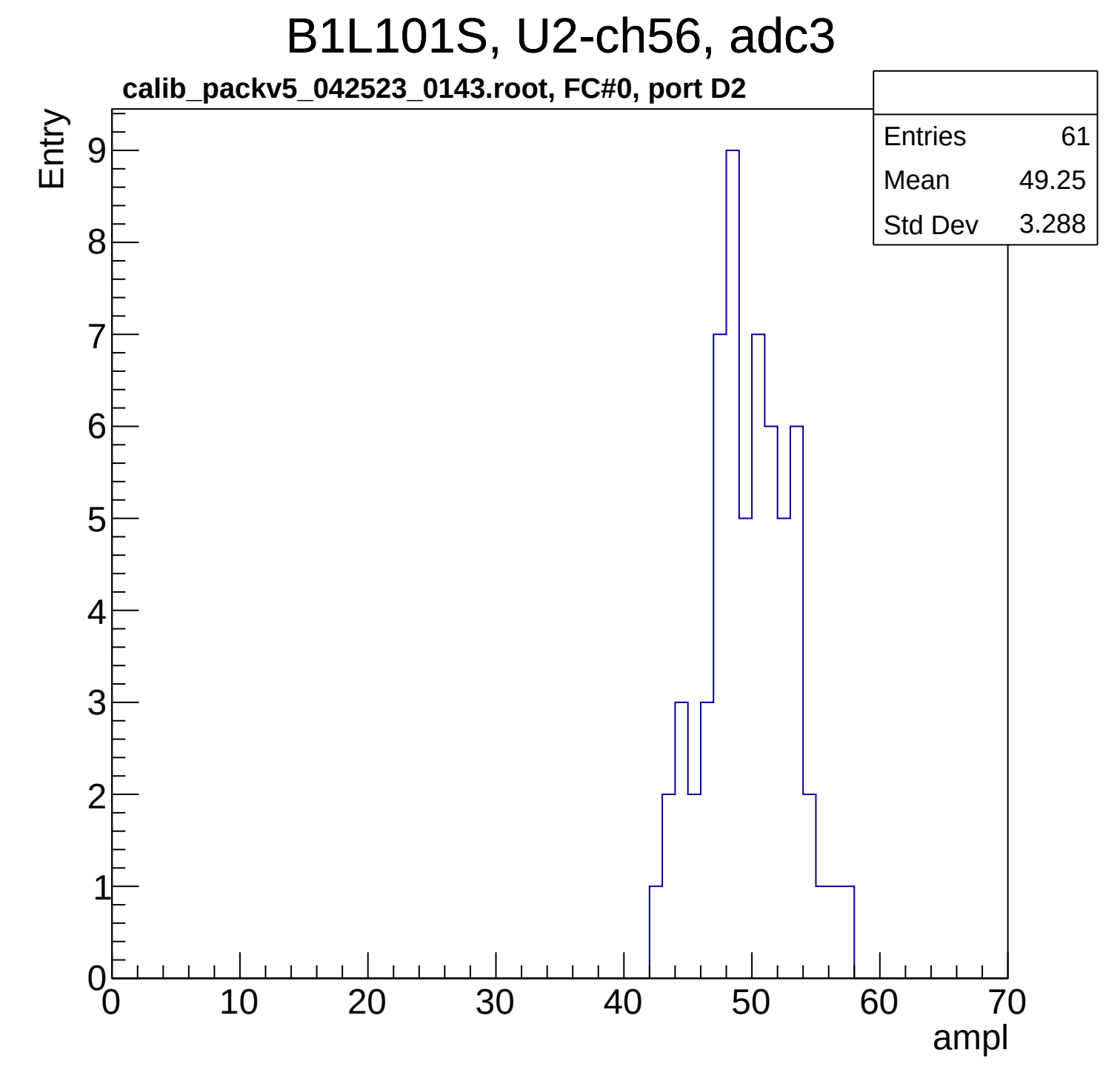

B1L101S, U2-ch55, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 61.89
Std Dev 1.197
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

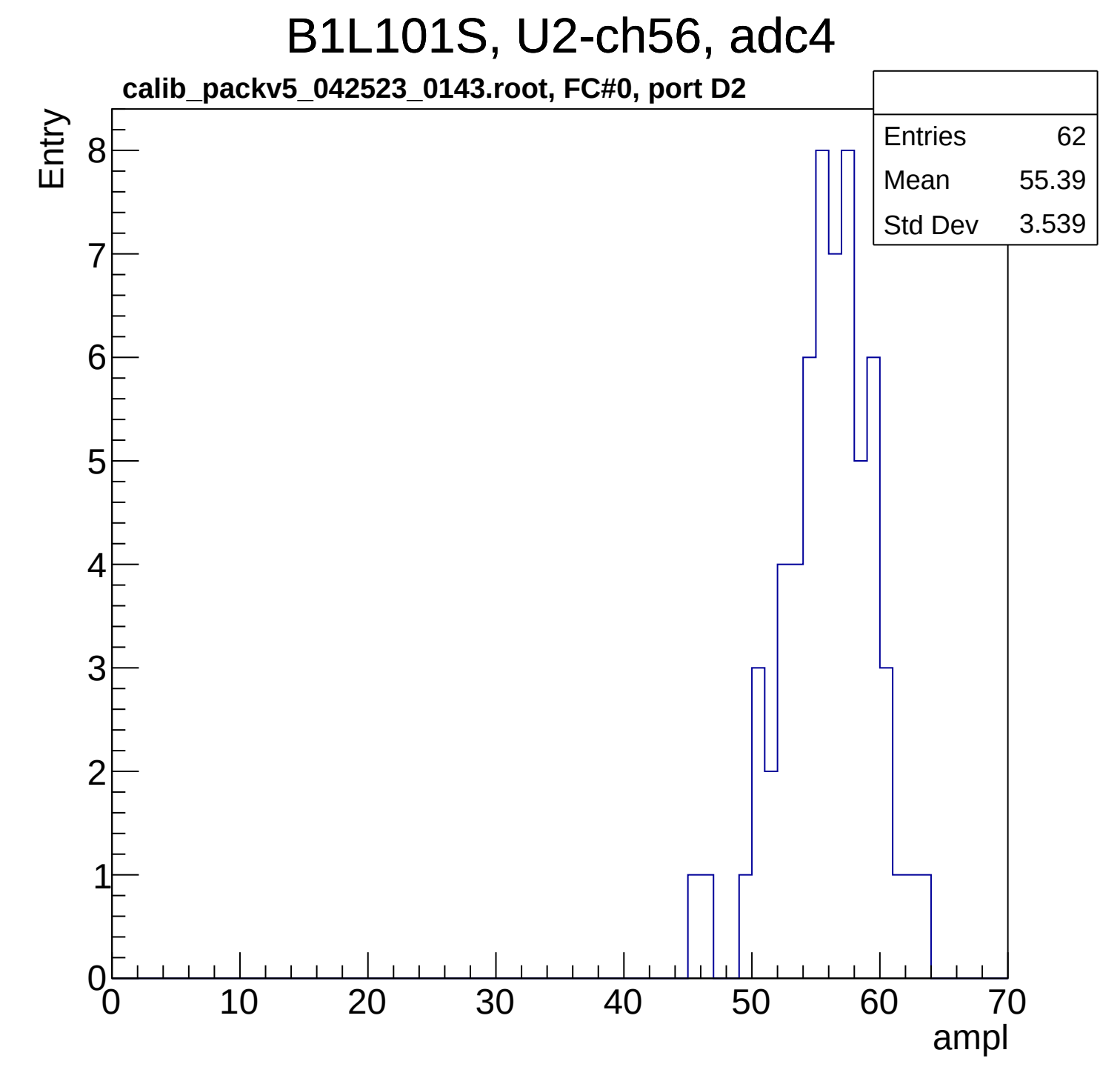

B1L101S, U2-ch55, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

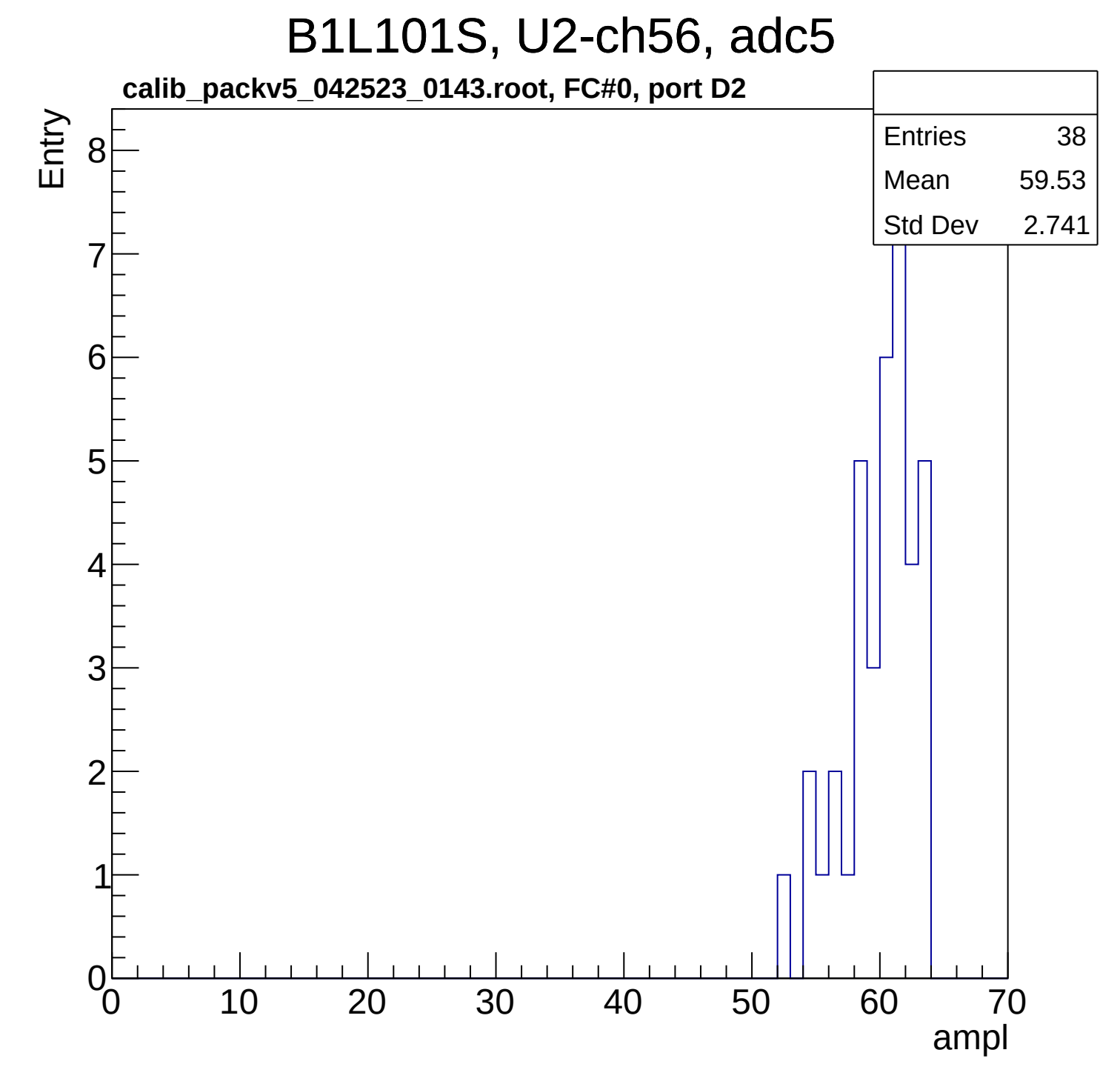

B1L101S, U2-ch56, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 29.27
Std Dev 3.738
Gaus mean : 29.5702
Gaus Width: 4.3571
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

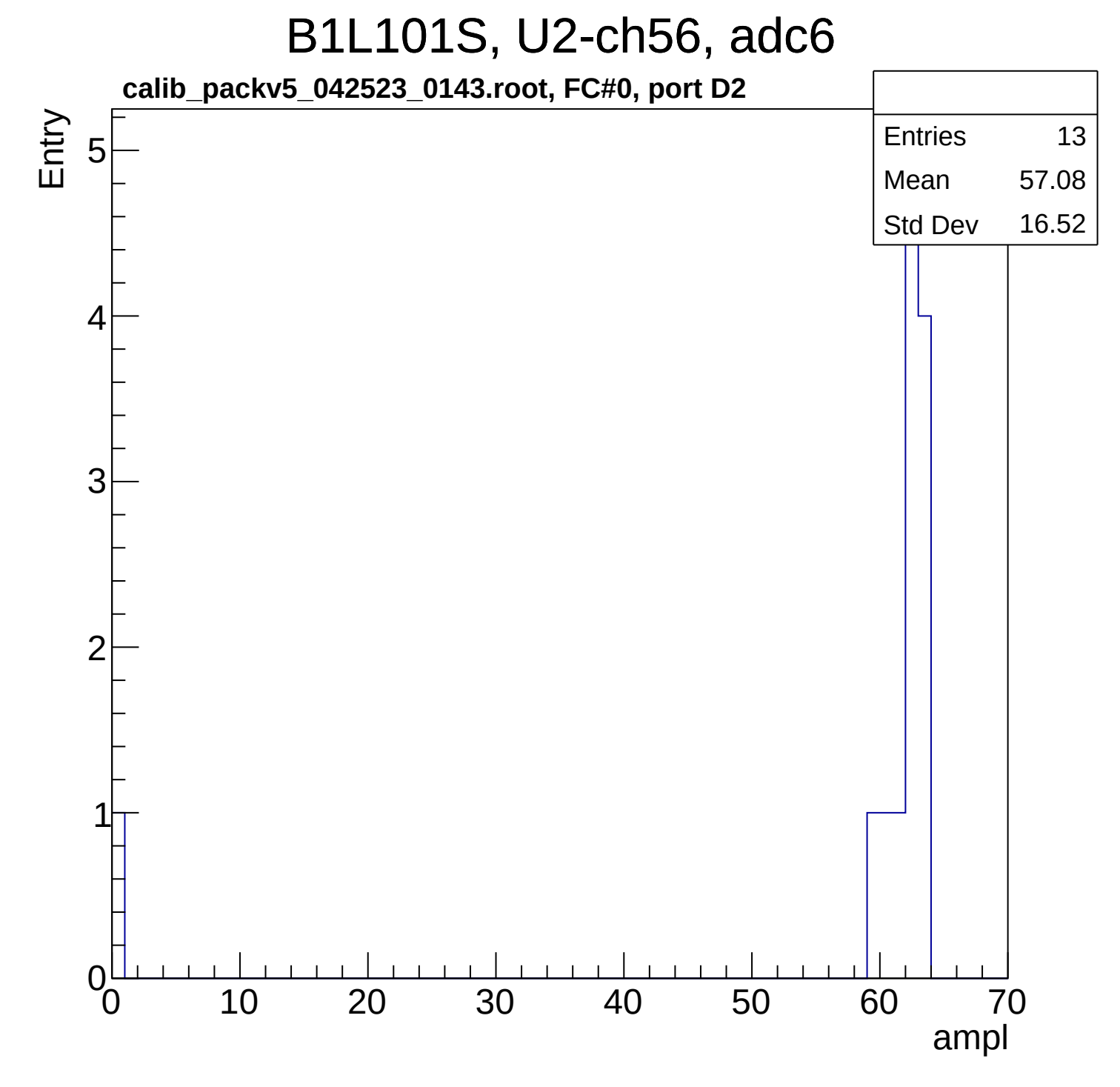

B1L101S, U2-ch56, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 36.35
Std Dev 3.759
Gaus mean : 36.9320
Gaus Width: 3.6432
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

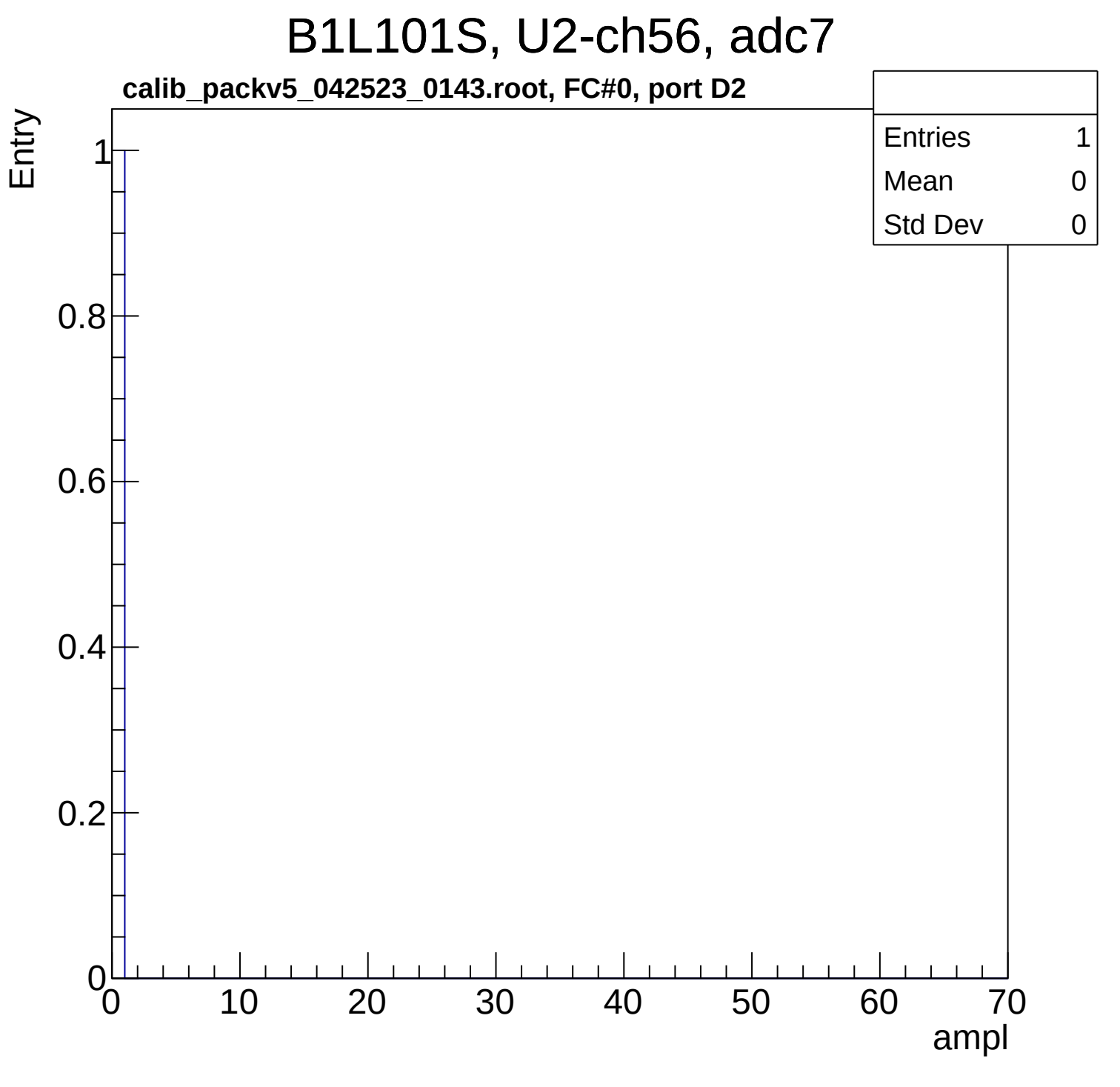

B1L101S, U2-ch56, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 43.14
Std Dev 3.912
Gaus mean : 43.8877
Gaus Width: 3.0307
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

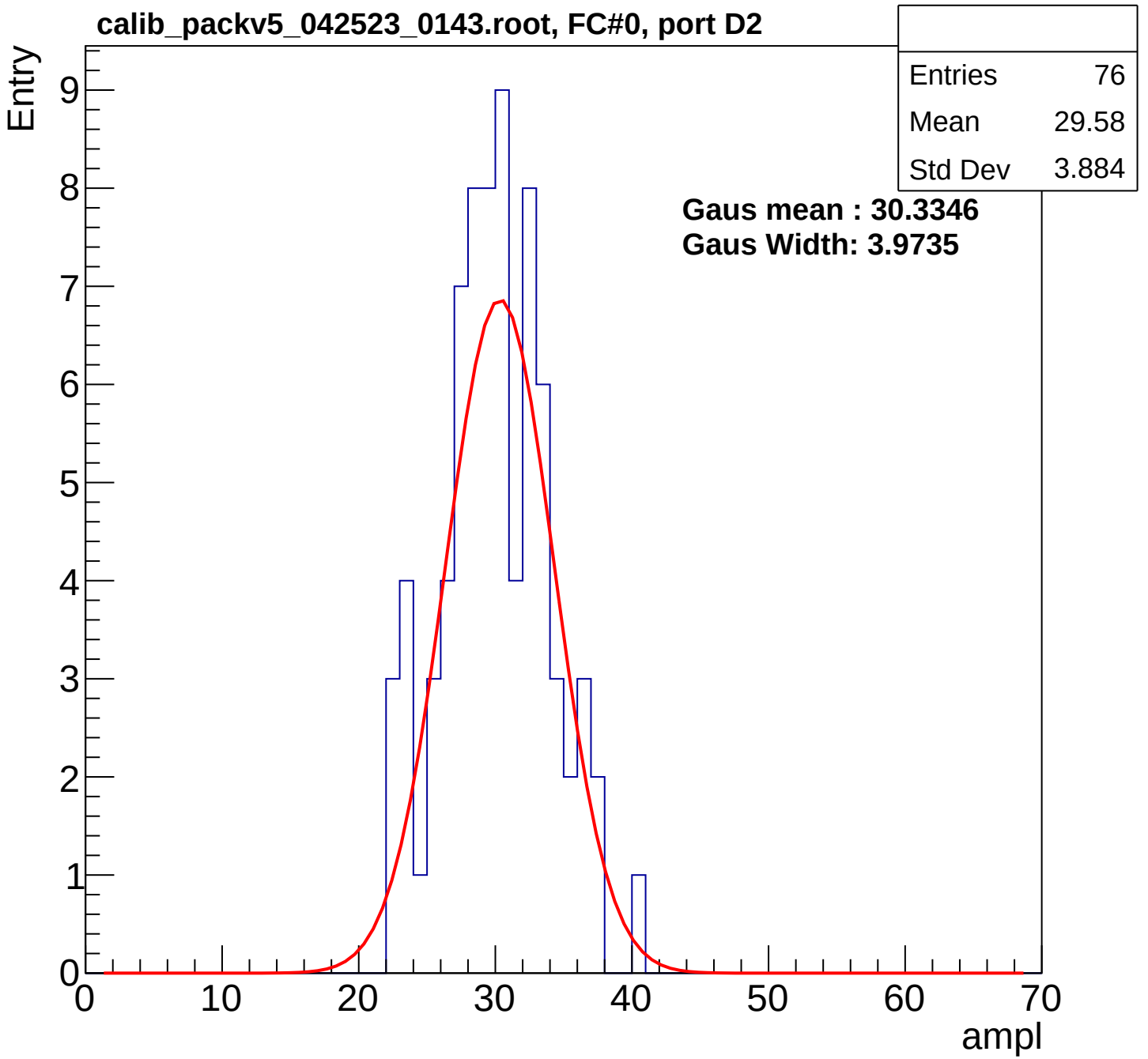

B1L101S, U2-ch56, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 49.25
Std Dev 3.288
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

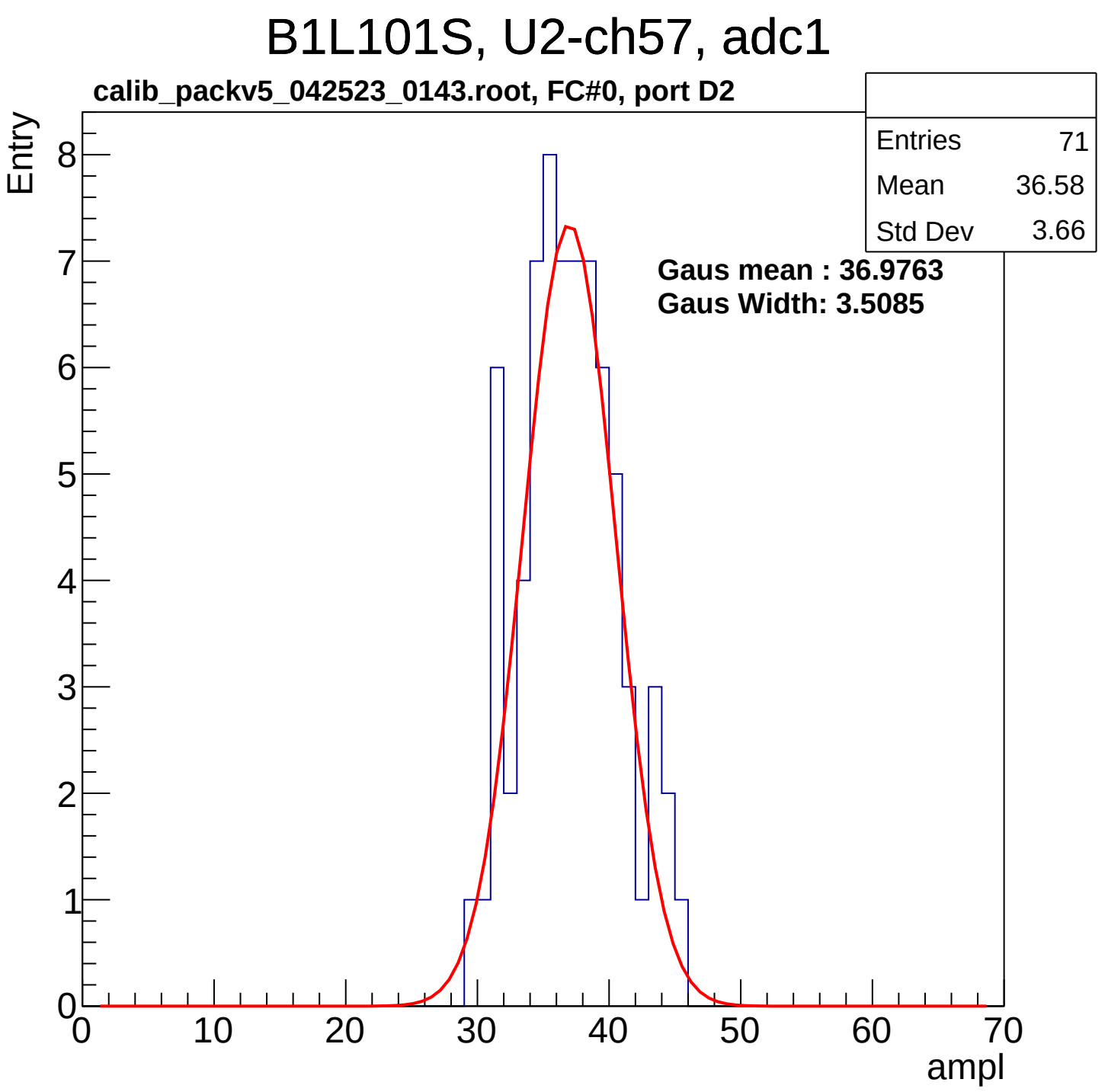

B1L101S, U2-ch56, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 55.39
Std Dev 3.539
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

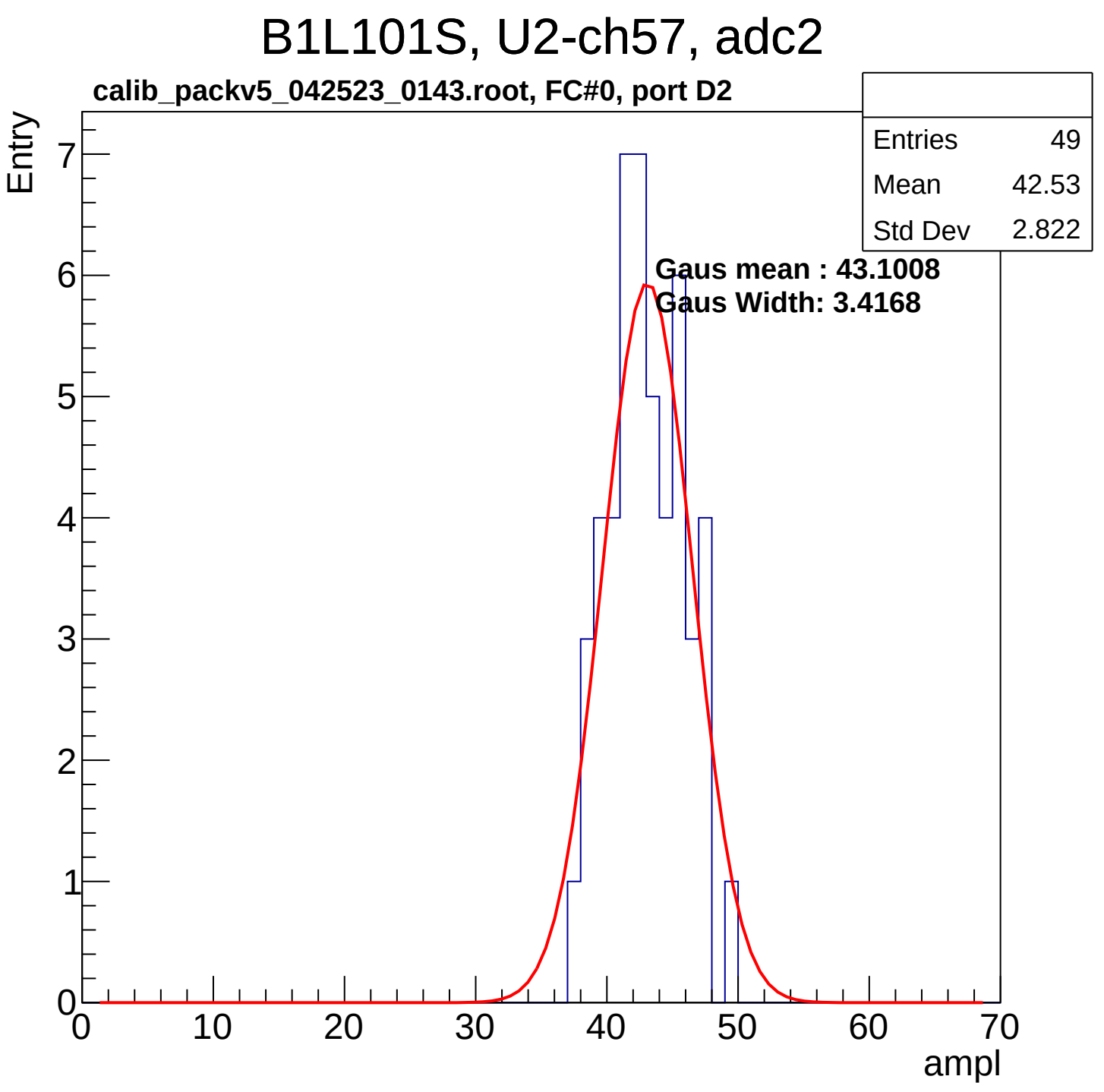

B1L101S, U2-ch56, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 38
Mean 59.53
Std Dev 2.741
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

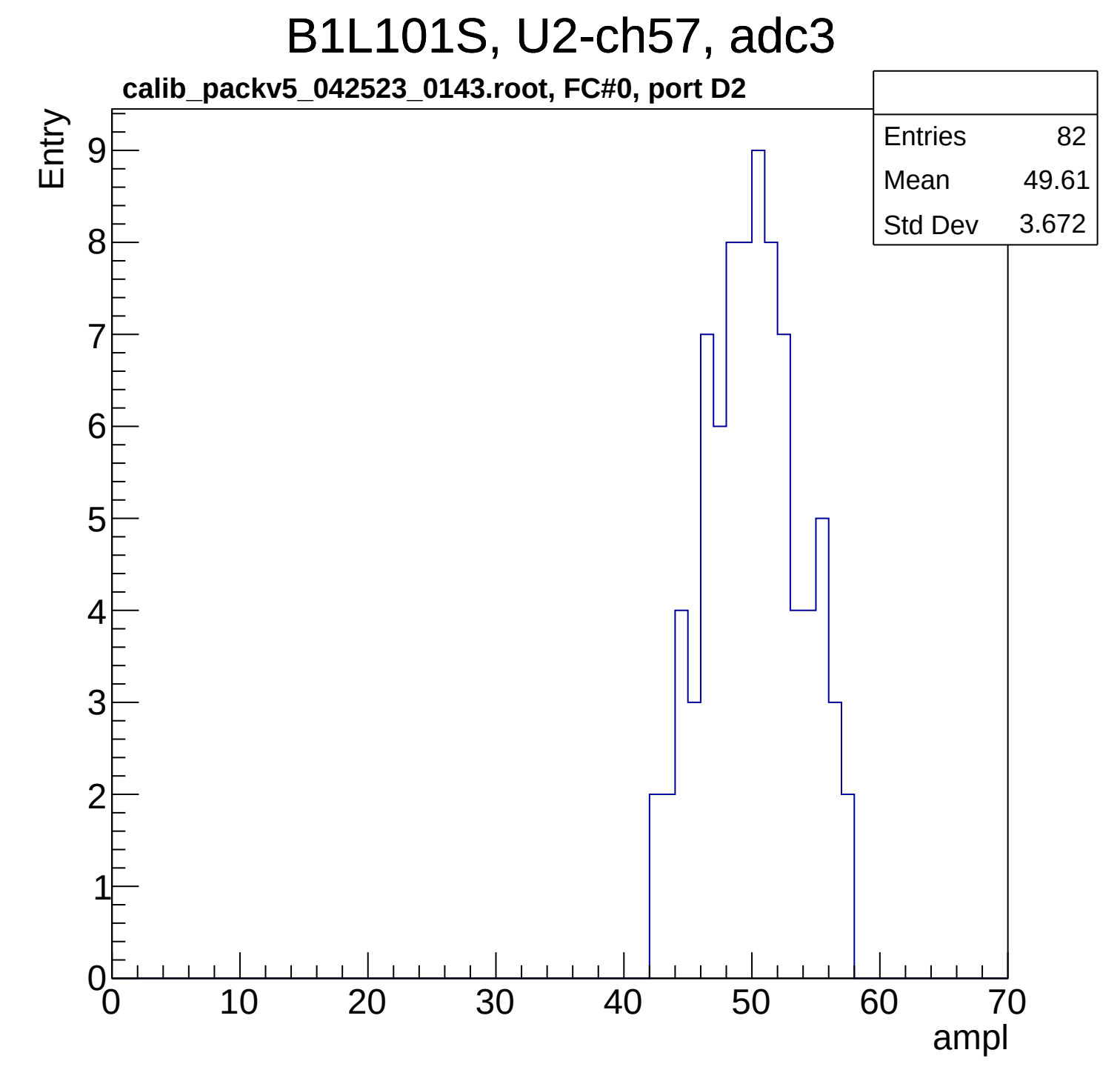

B1L101S, U2-ch56, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 13
Mean 57.08
Std Dev 16.52
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

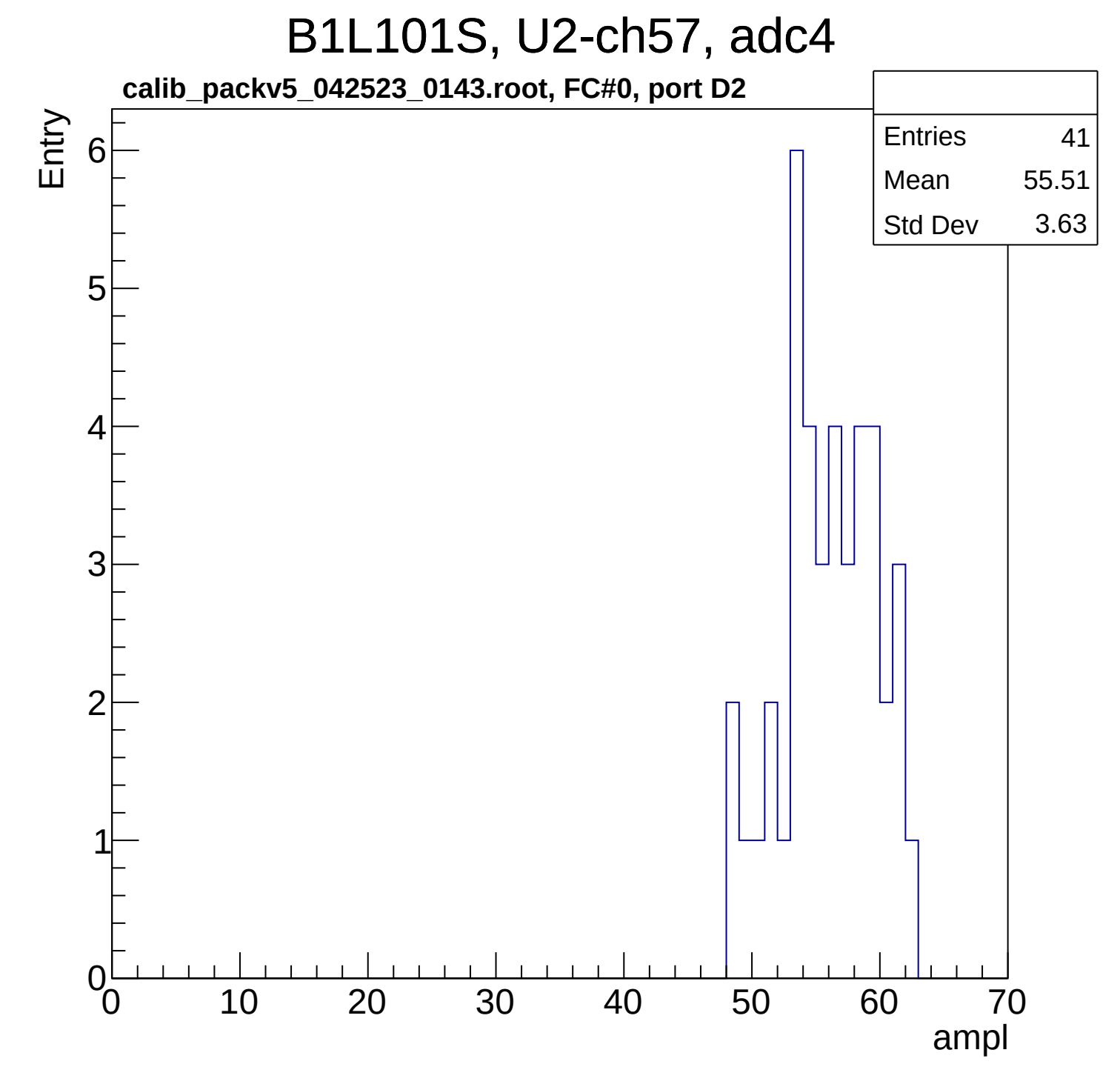

B1L101S, U2-ch56, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

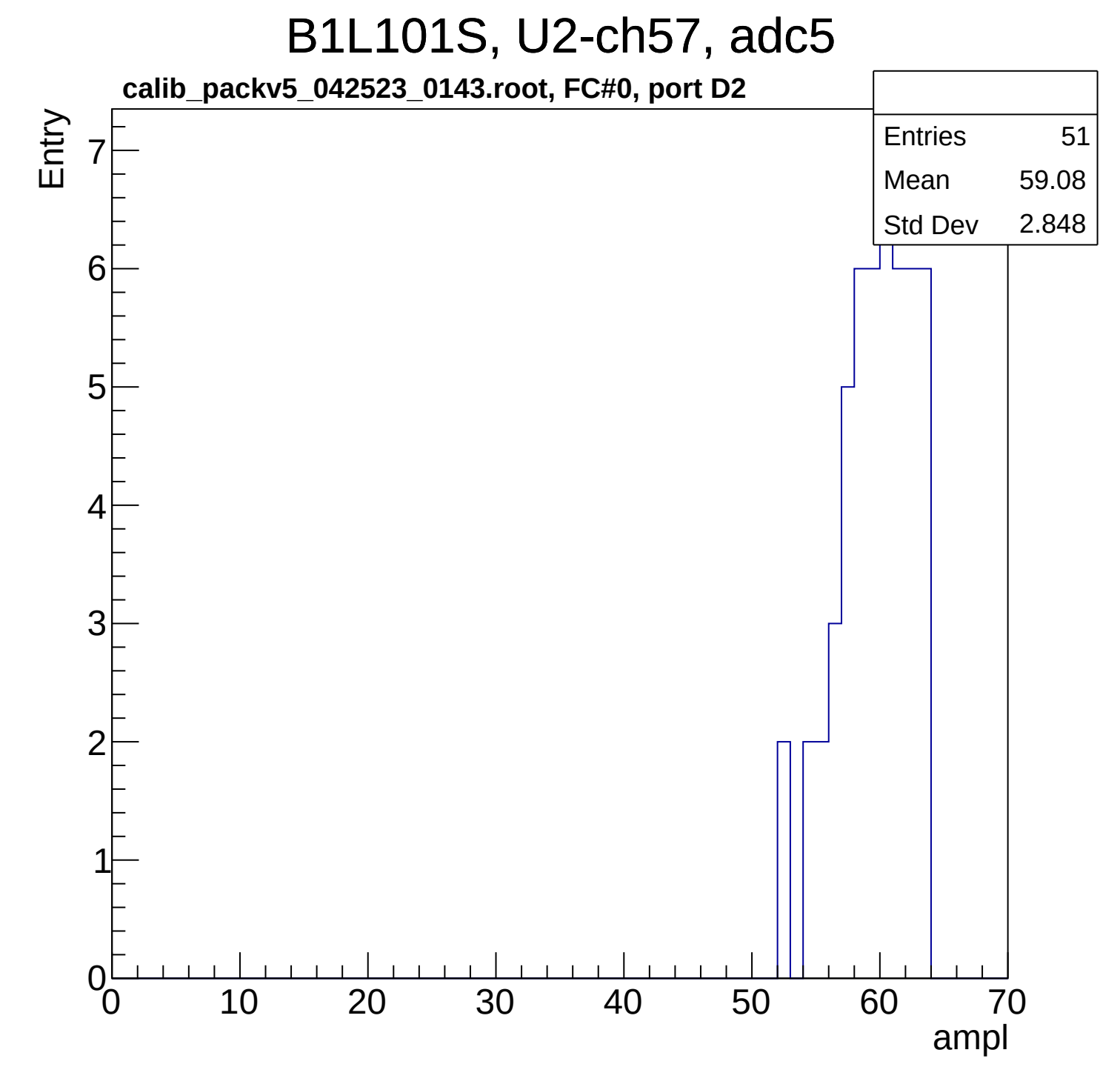

B1L101S, U2-ch57, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 29.58
Std Dev 3.884
Gaus mean : 30.3346
Gaus Width: 3.9735
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

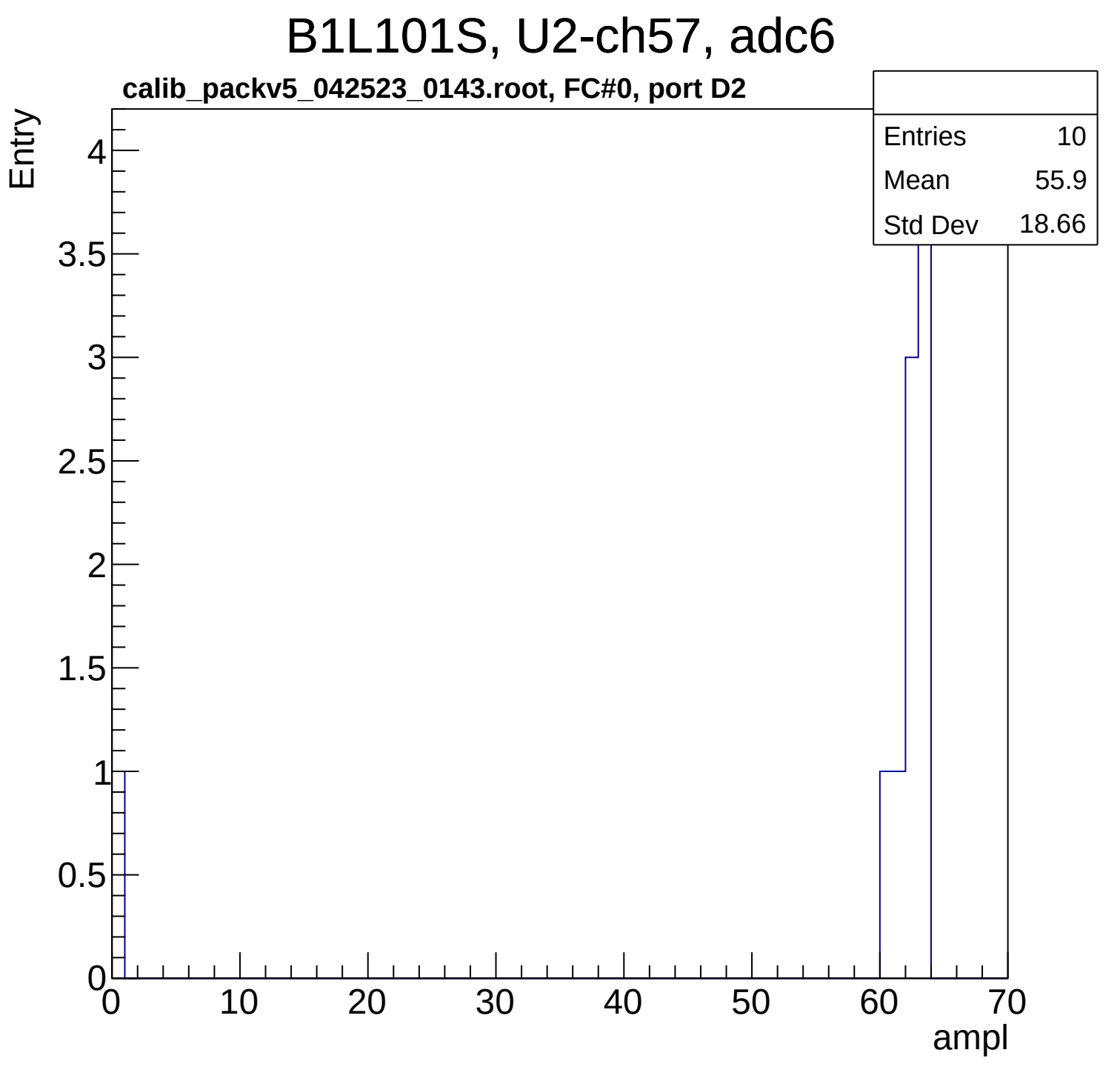

B1L101S, U2-ch57, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 36.58
Std Dev 3.66
Gaus mean : 36.9763
Gaus Width: 3.5085
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

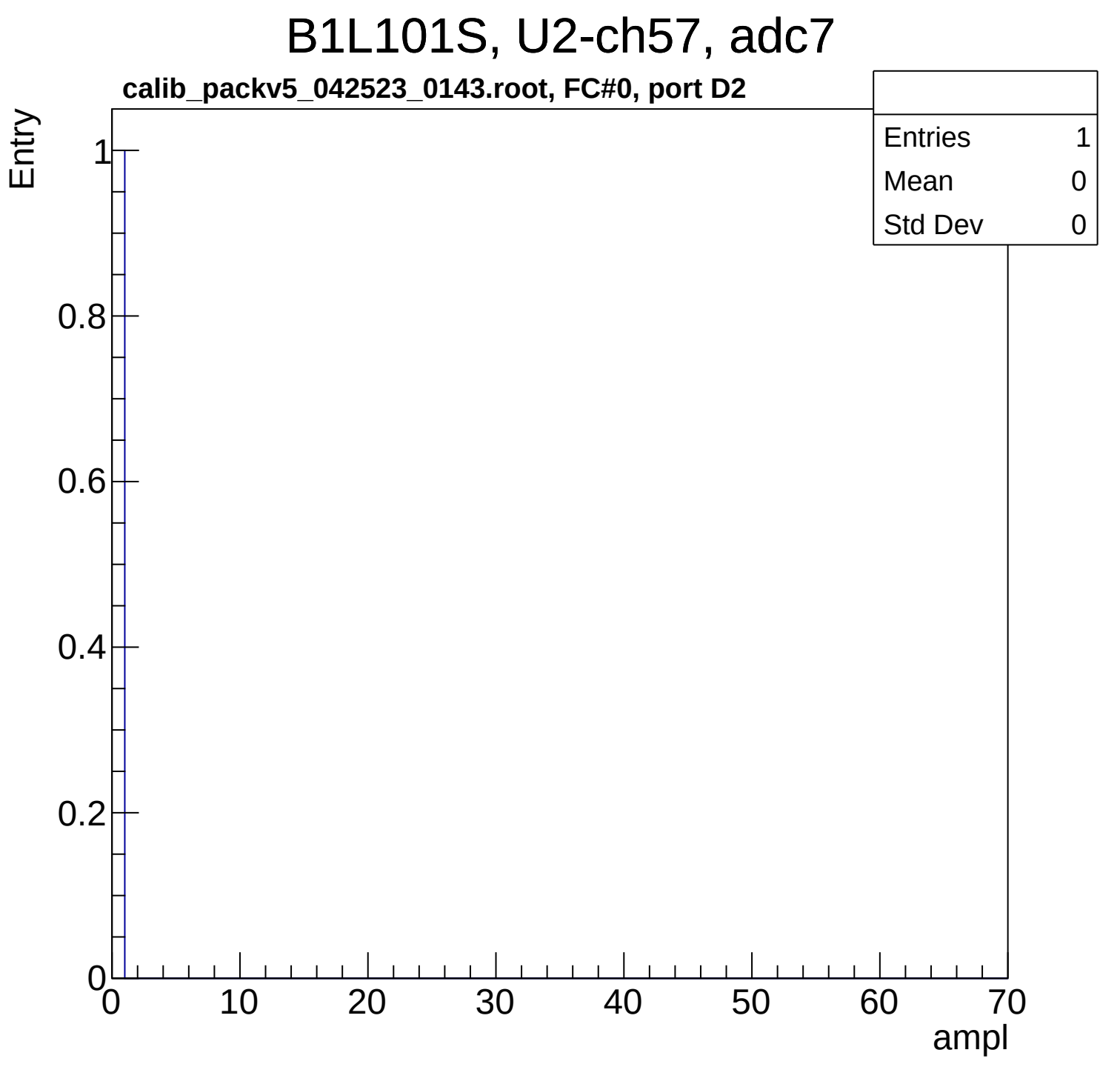

B1L101S, U2-ch57, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 42.53
Std Dev 2.822
Gaus mean : 43.1008
Gaus Width: 3.4168
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

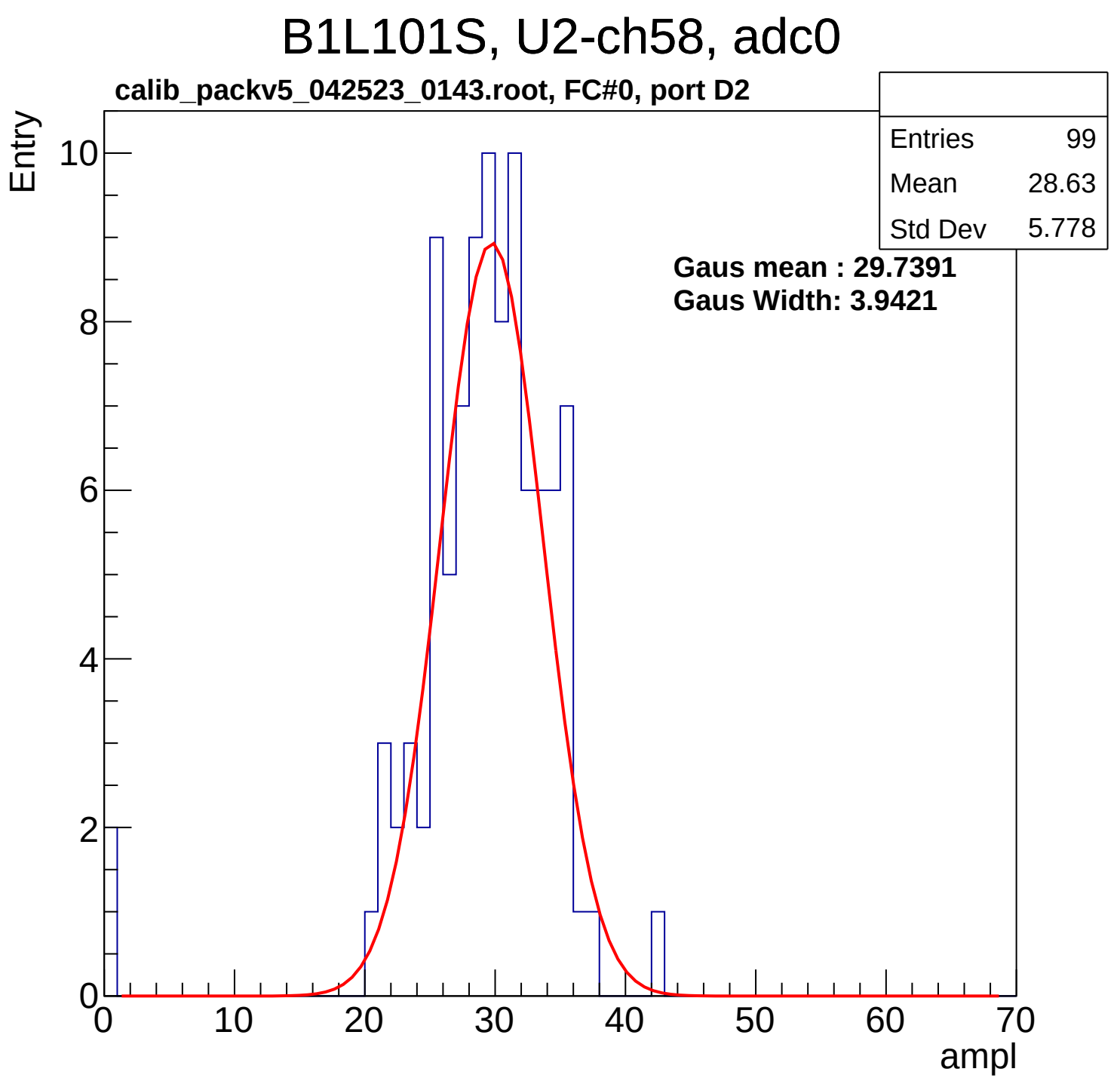

B1L101S, U2-ch57, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 82
Mean 49.61
Std Dev 3.672
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

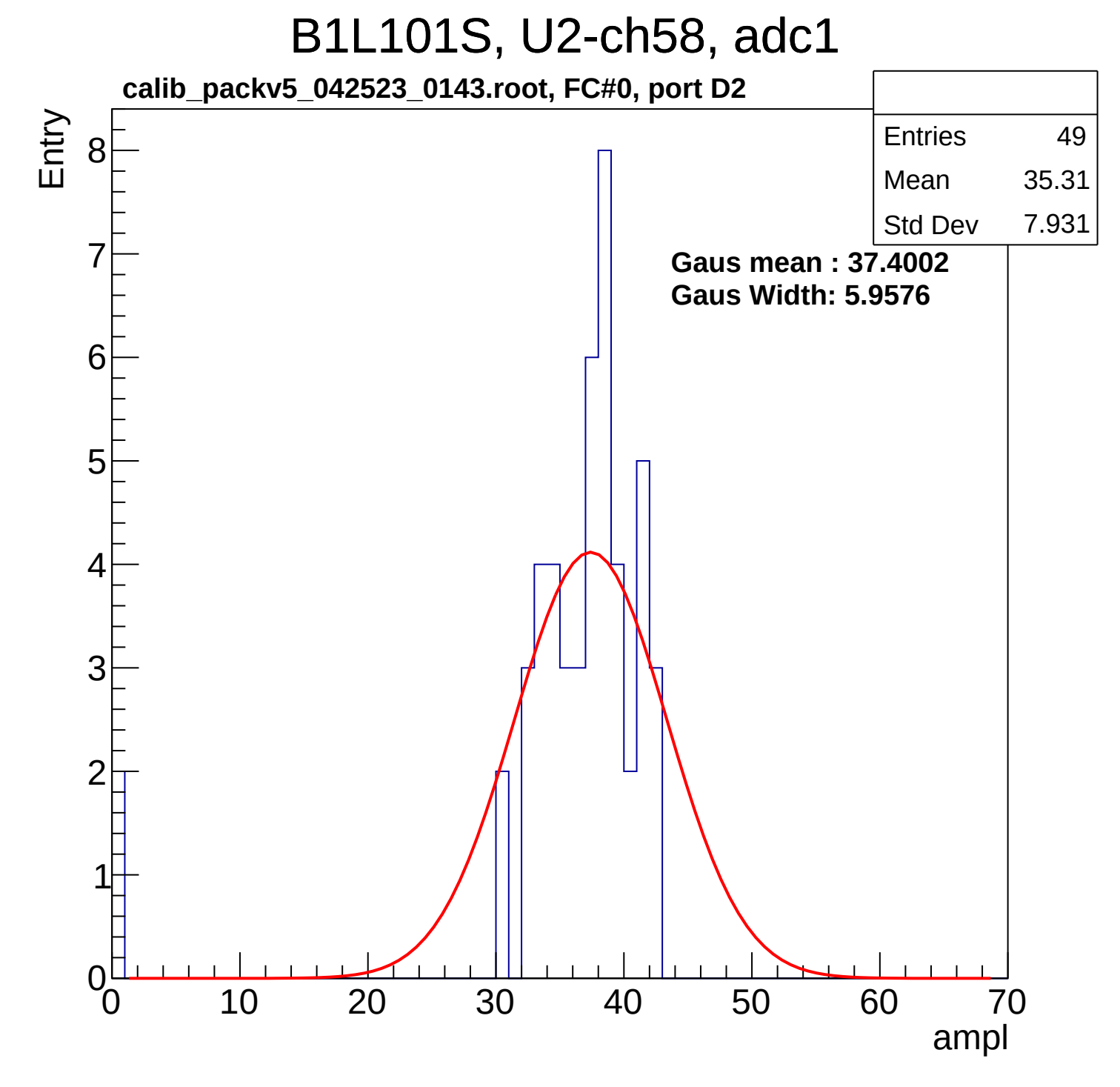

B1L101S, U2-ch57, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 41
Mean 55.51
Std Dev 3.63
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

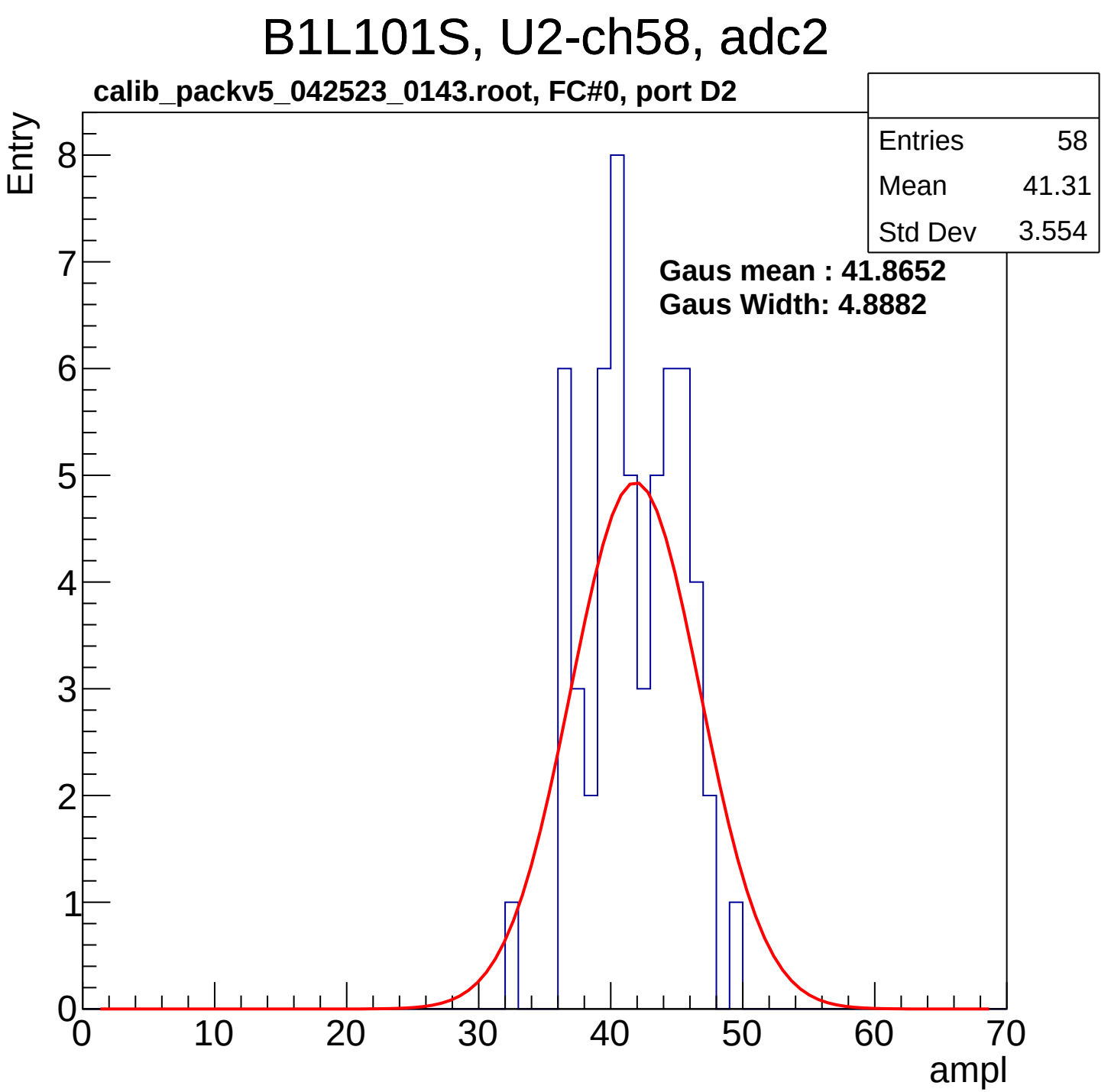

B1L101S, U2-ch57, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 59.08
Std Dev 2.848
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

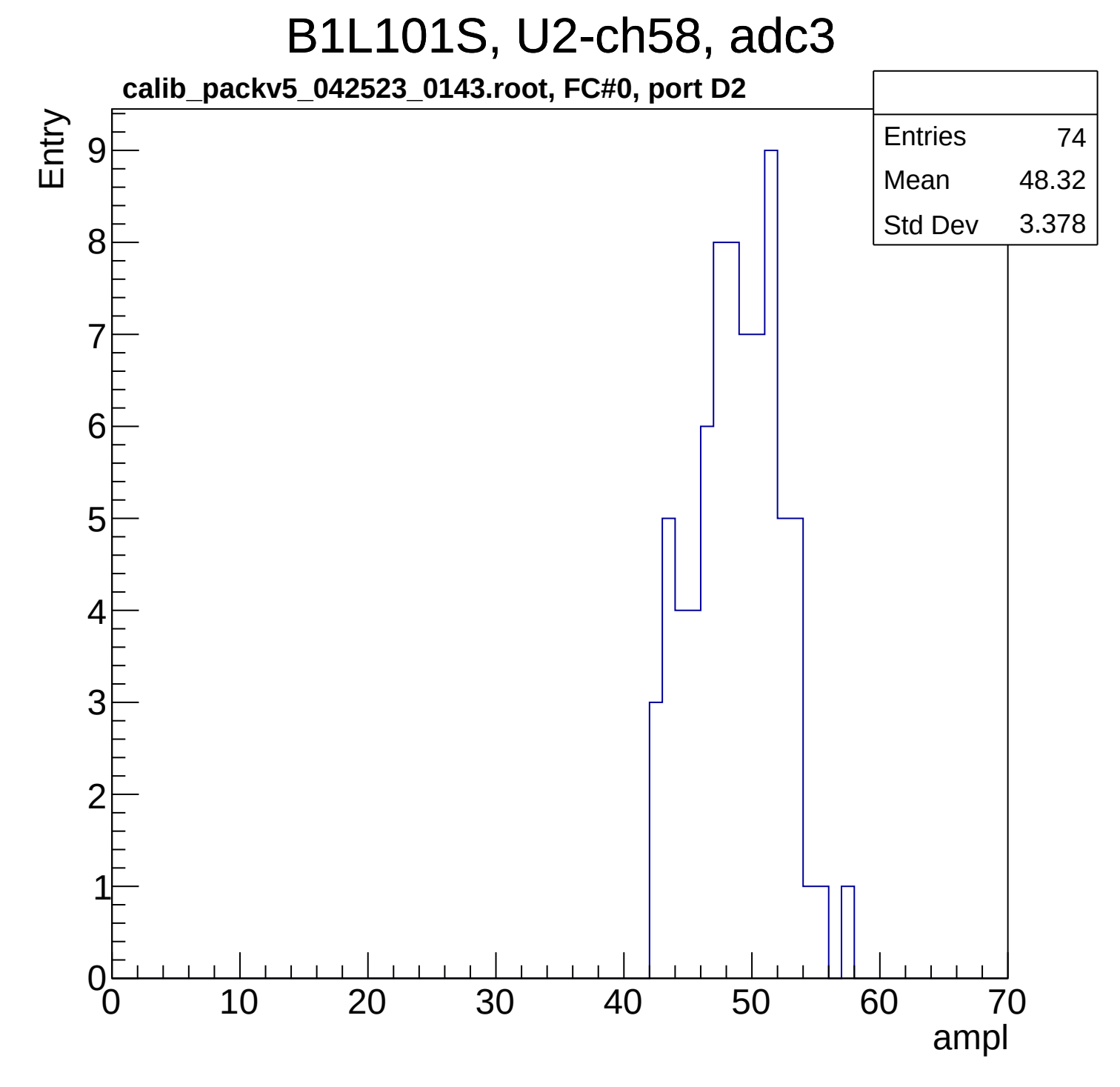

B1L101S, U2-ch57, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 55.9
Std Dev 18.66
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

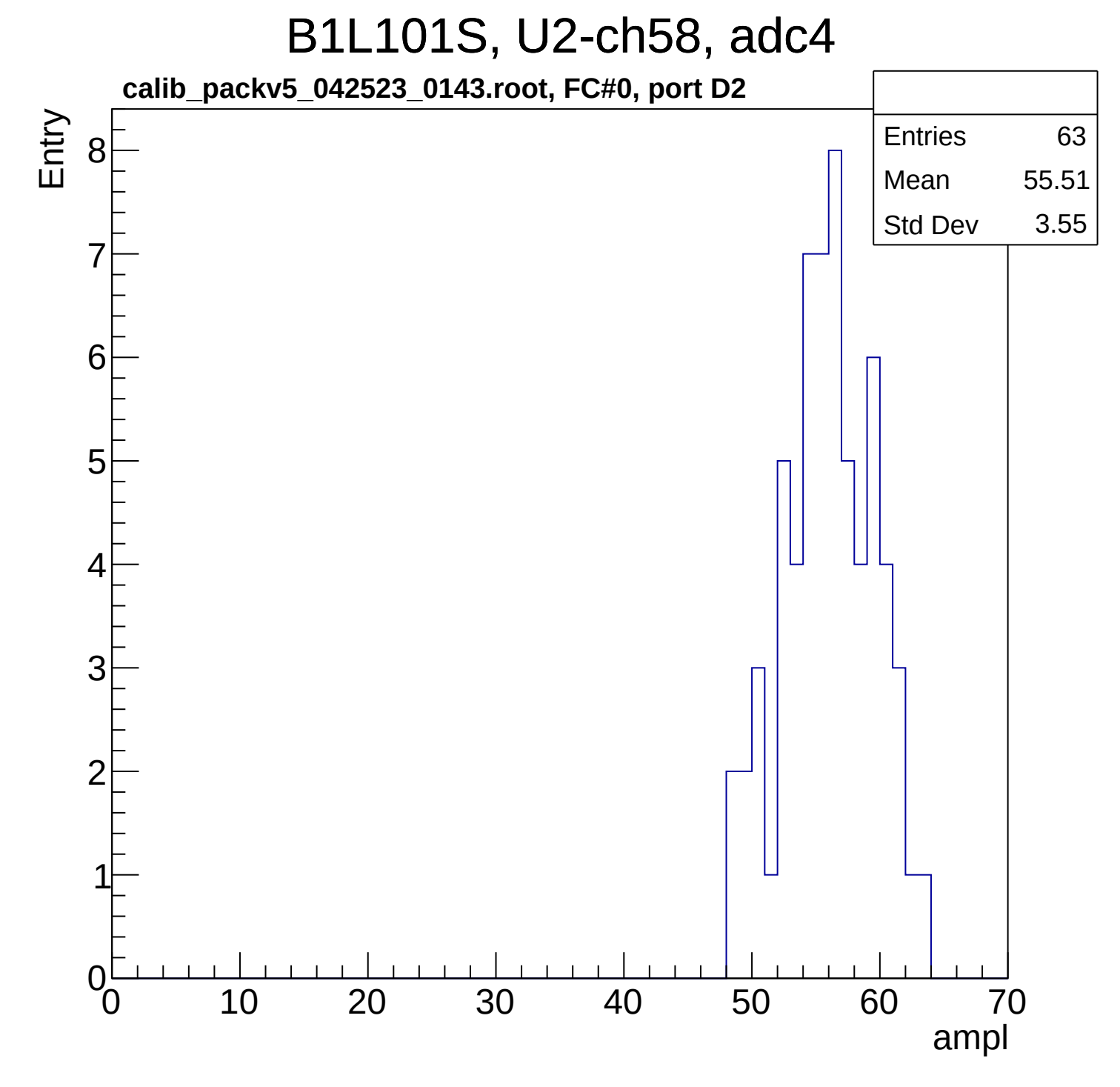

B1L101S, U2-ch57, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

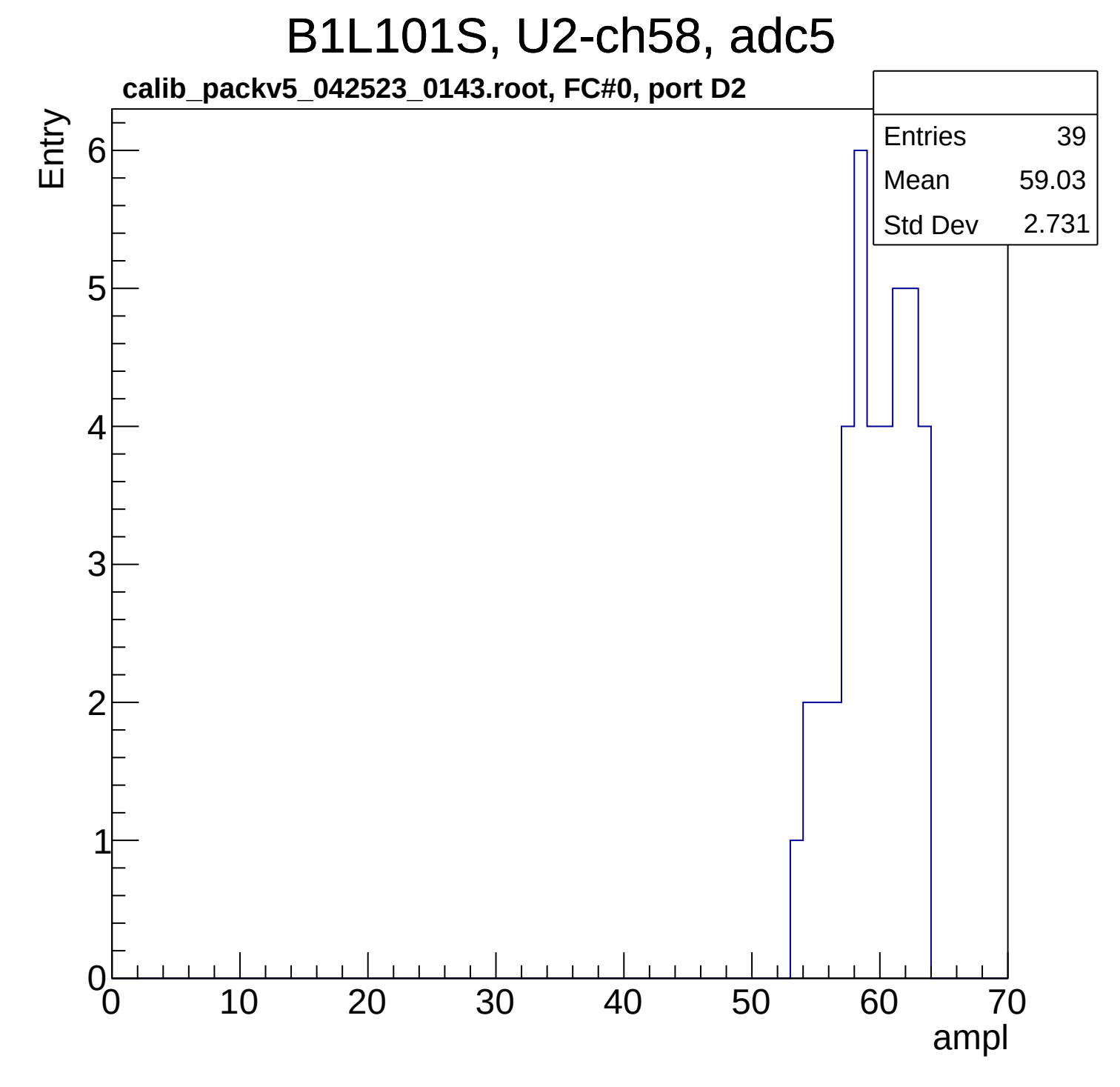

B1L101S, U2-ch58, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 99
Mean 28.63
Std Dev 5.778
Gaus mean : 29.7391
Gaus Width: 3.9421
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

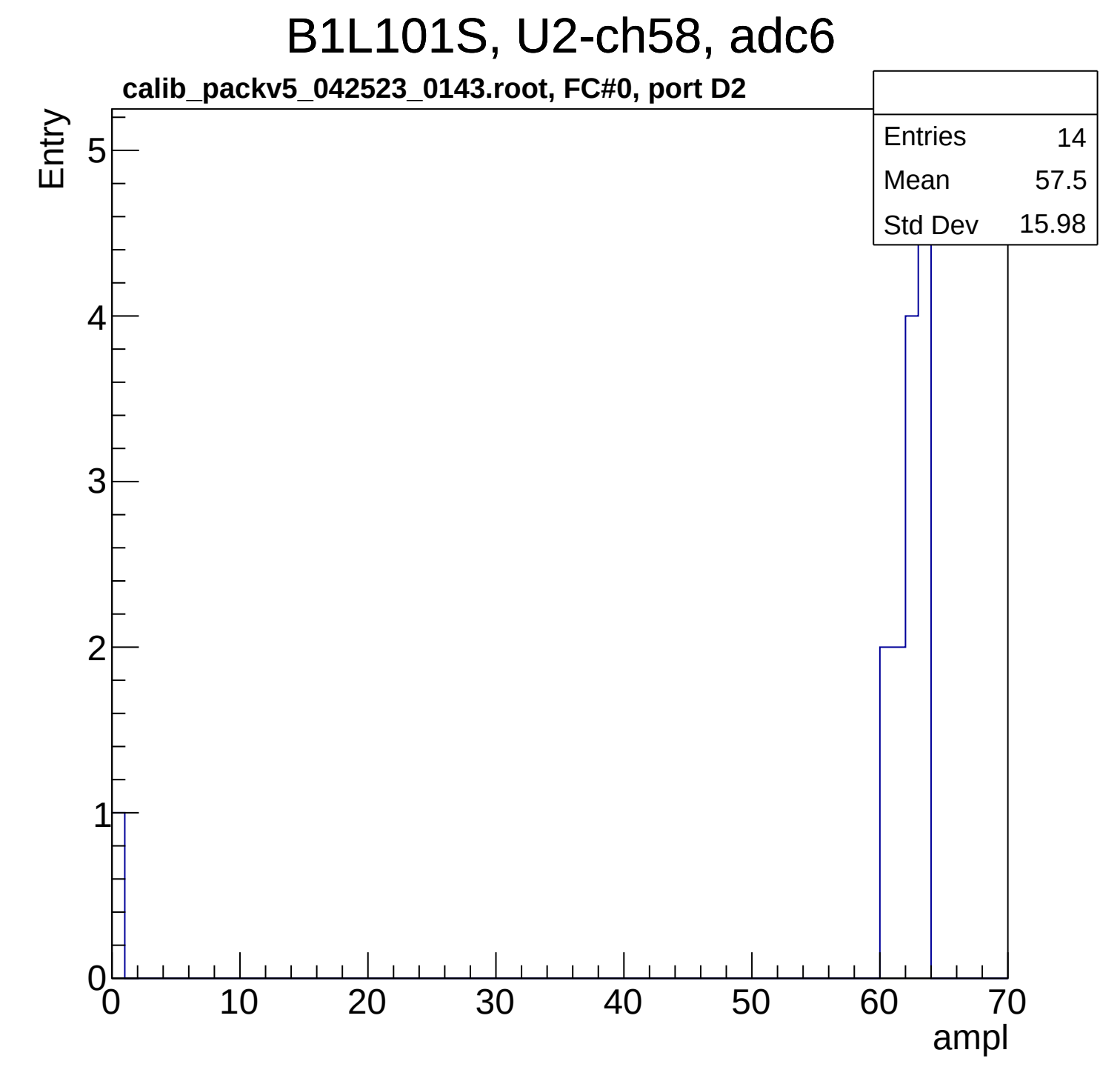

B1L101S, U2-ch58, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 35.31
Std Dev 7.931
Gaus mean : 37.4002
Gaus Width: 5.9576
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

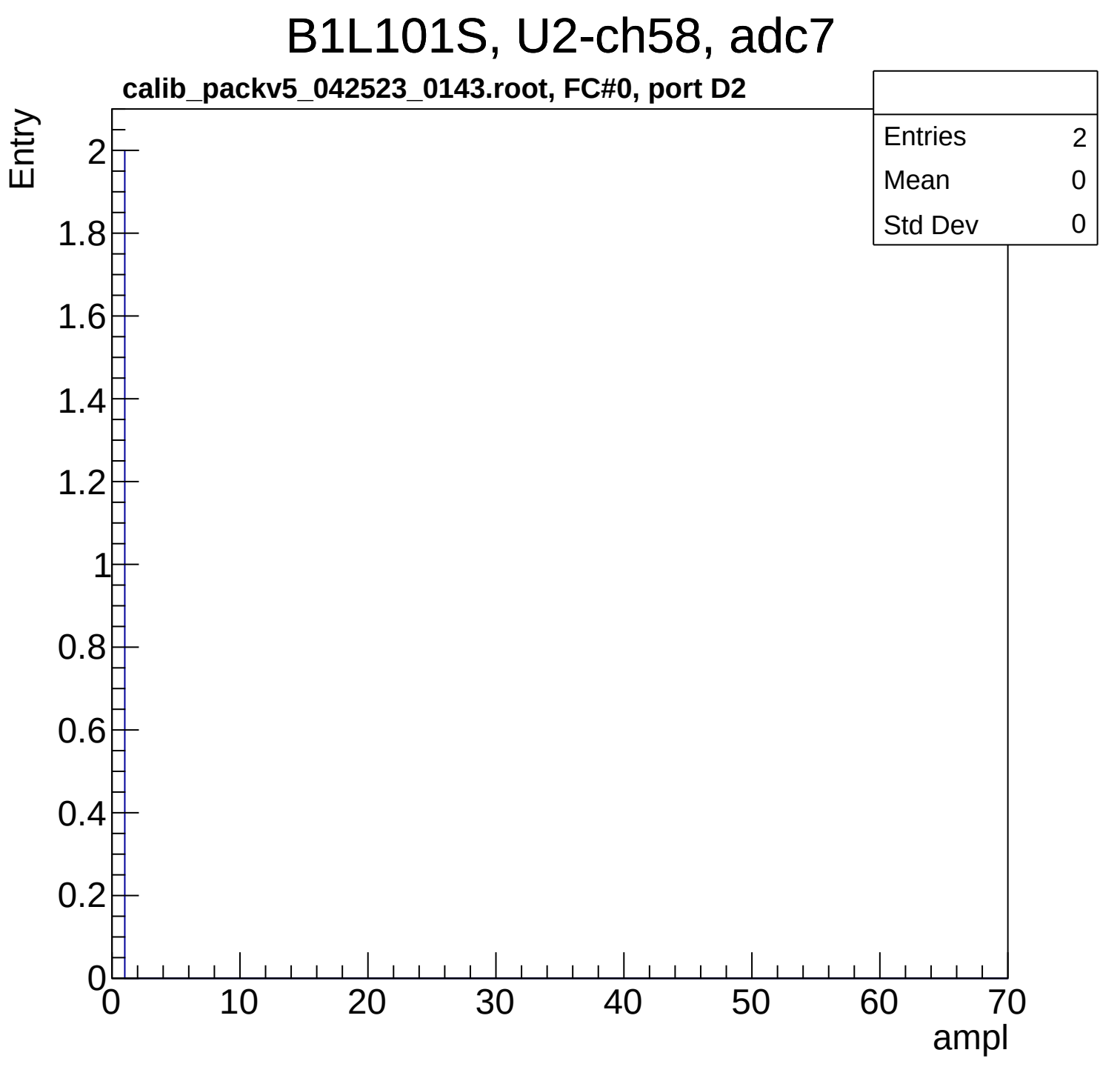

B1L101S, U2-ch58, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 41.31
Std Dev 3.554
Gaus mean : 41.8652
Gaus Width: 4.8882
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

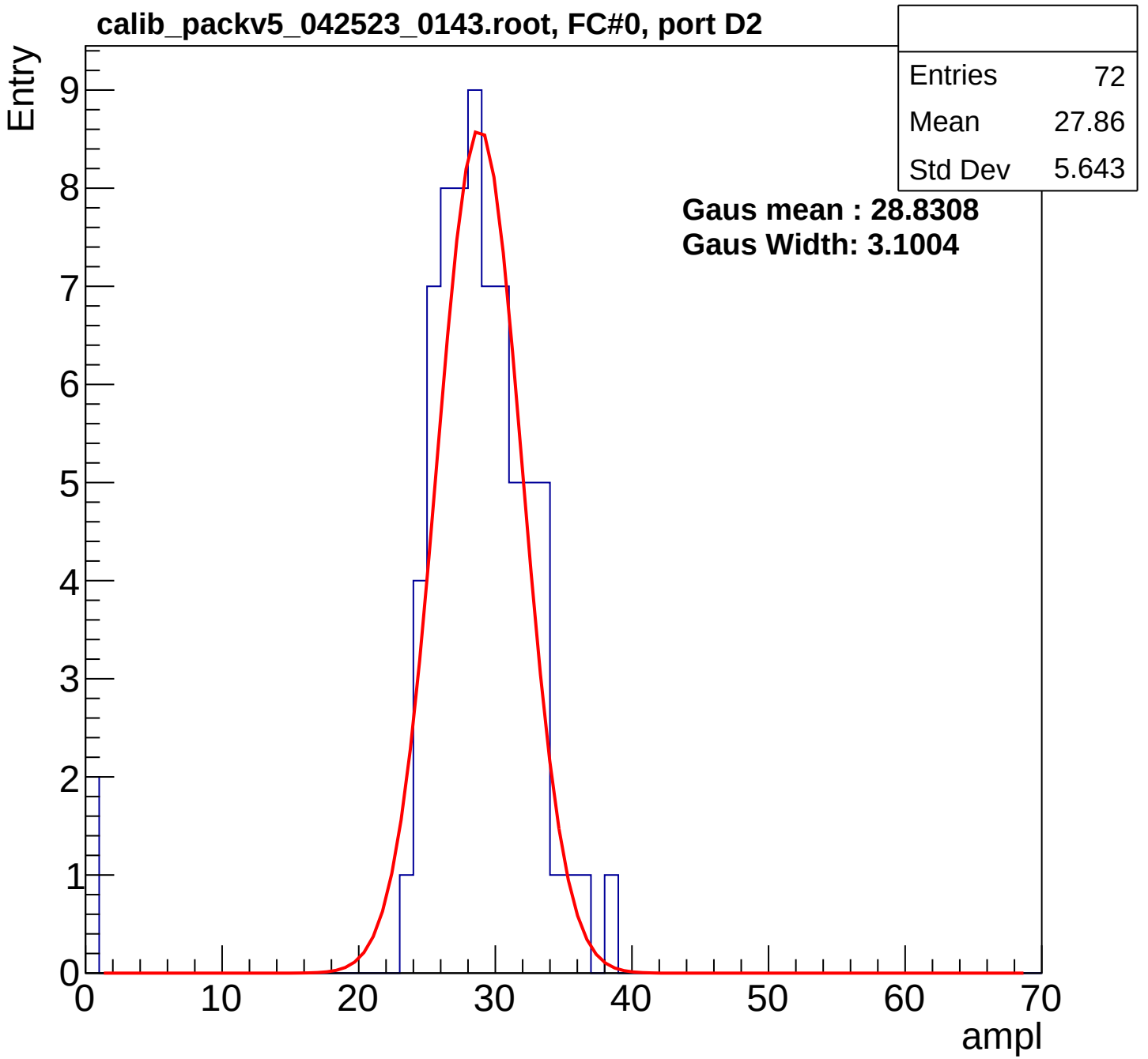

B1L101S, U2-ch58, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 48.32
Std Dev 3.378
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

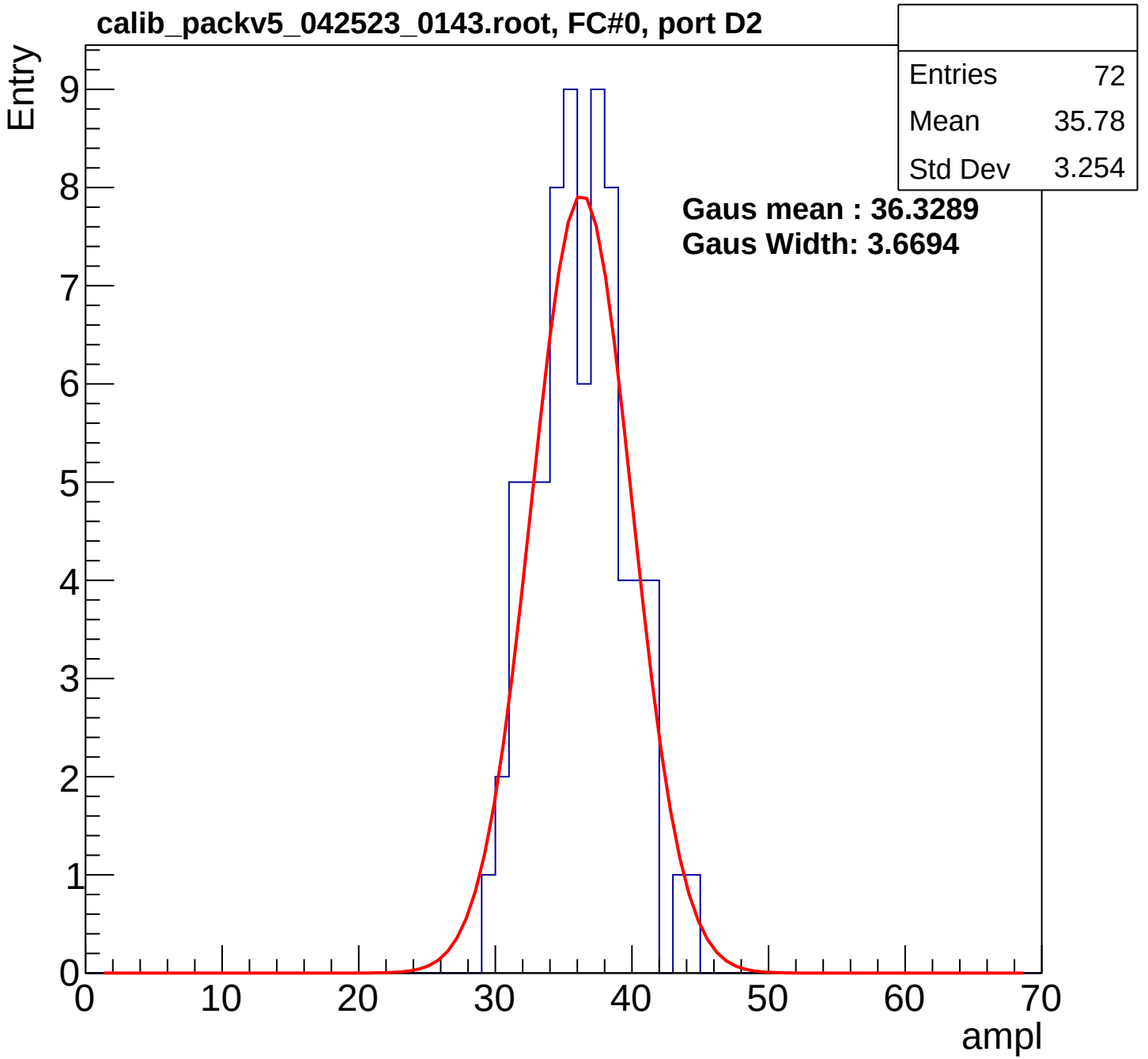

B1L101S, U2-ch58, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 55.51
Std Dev 3.55
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

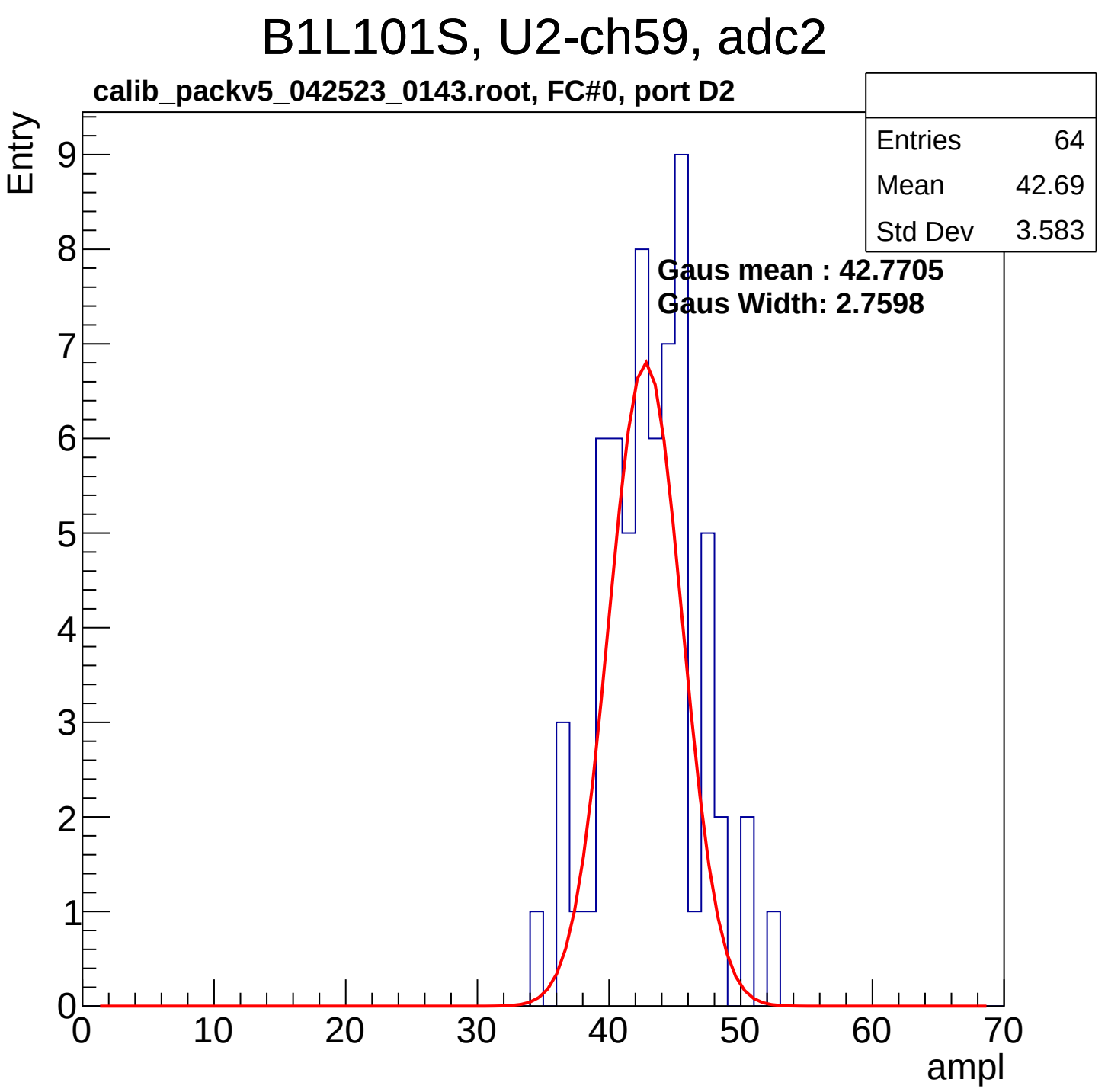

B1L101S, U2-ch58, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 39
Mean 59.03
Std Dev 2.731
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

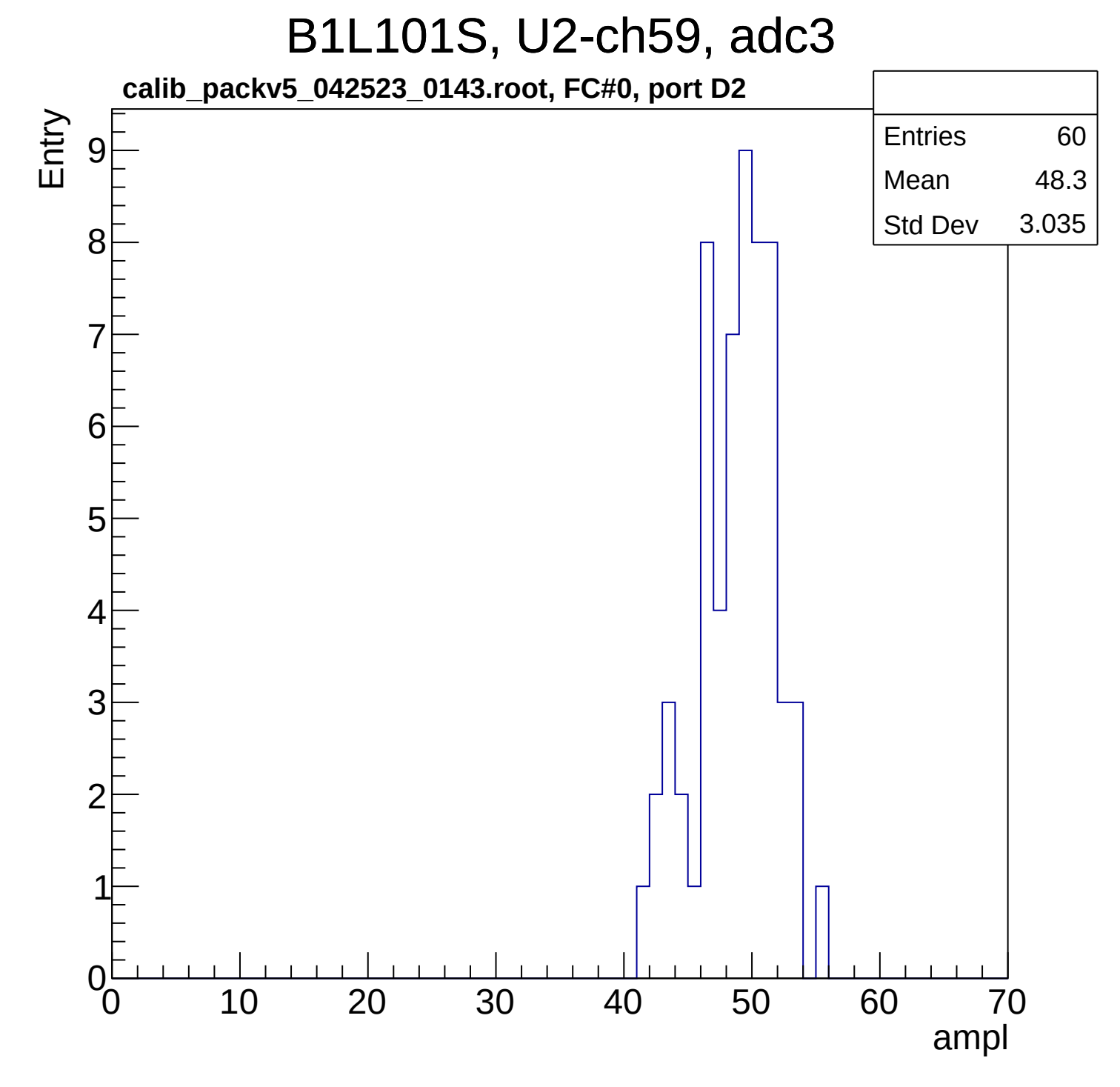

B1L101S, U2-ch58, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 14
Mean 57.5
Std Dev 15.98
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

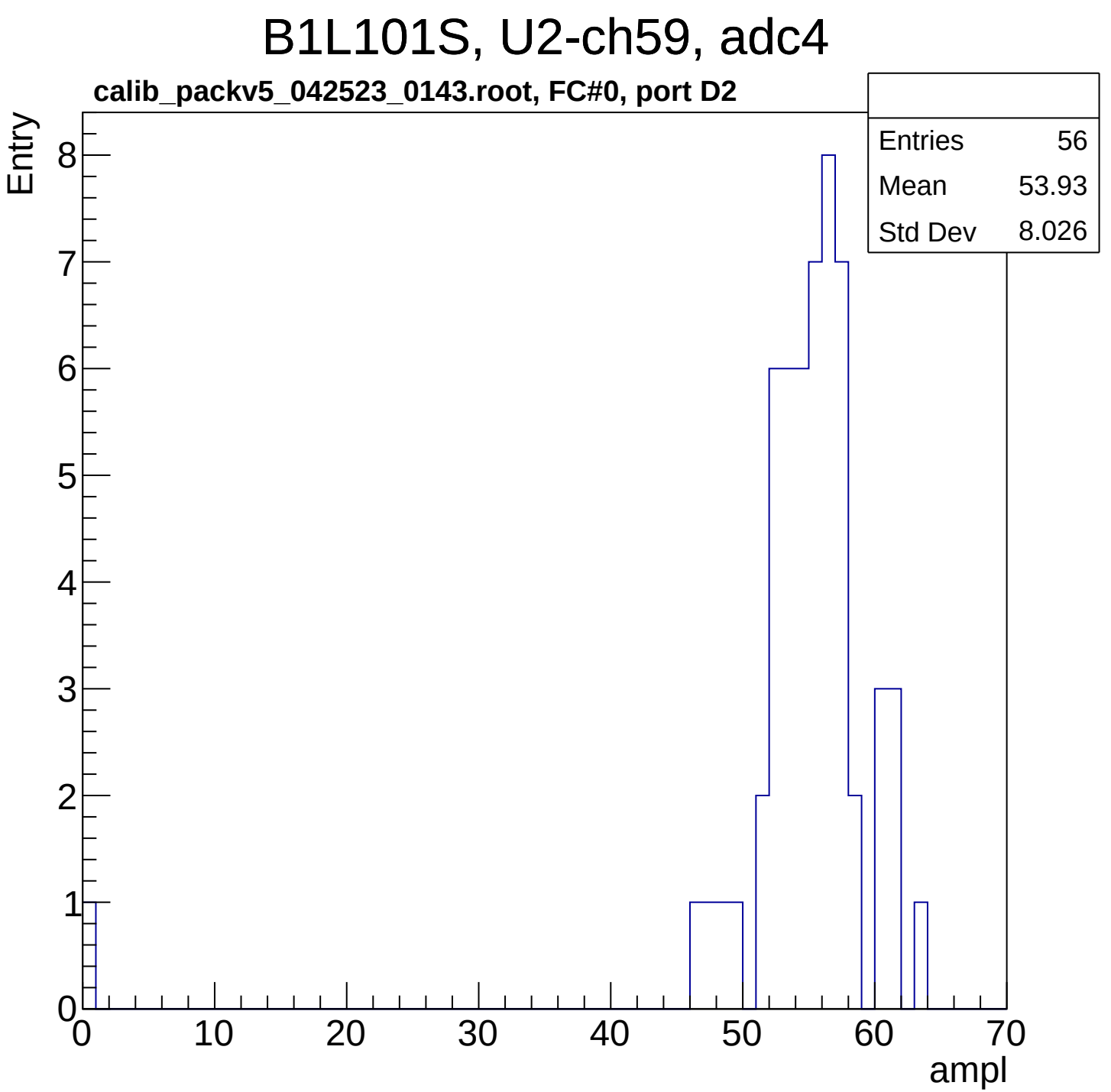

B1L101S, U2-ch58, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

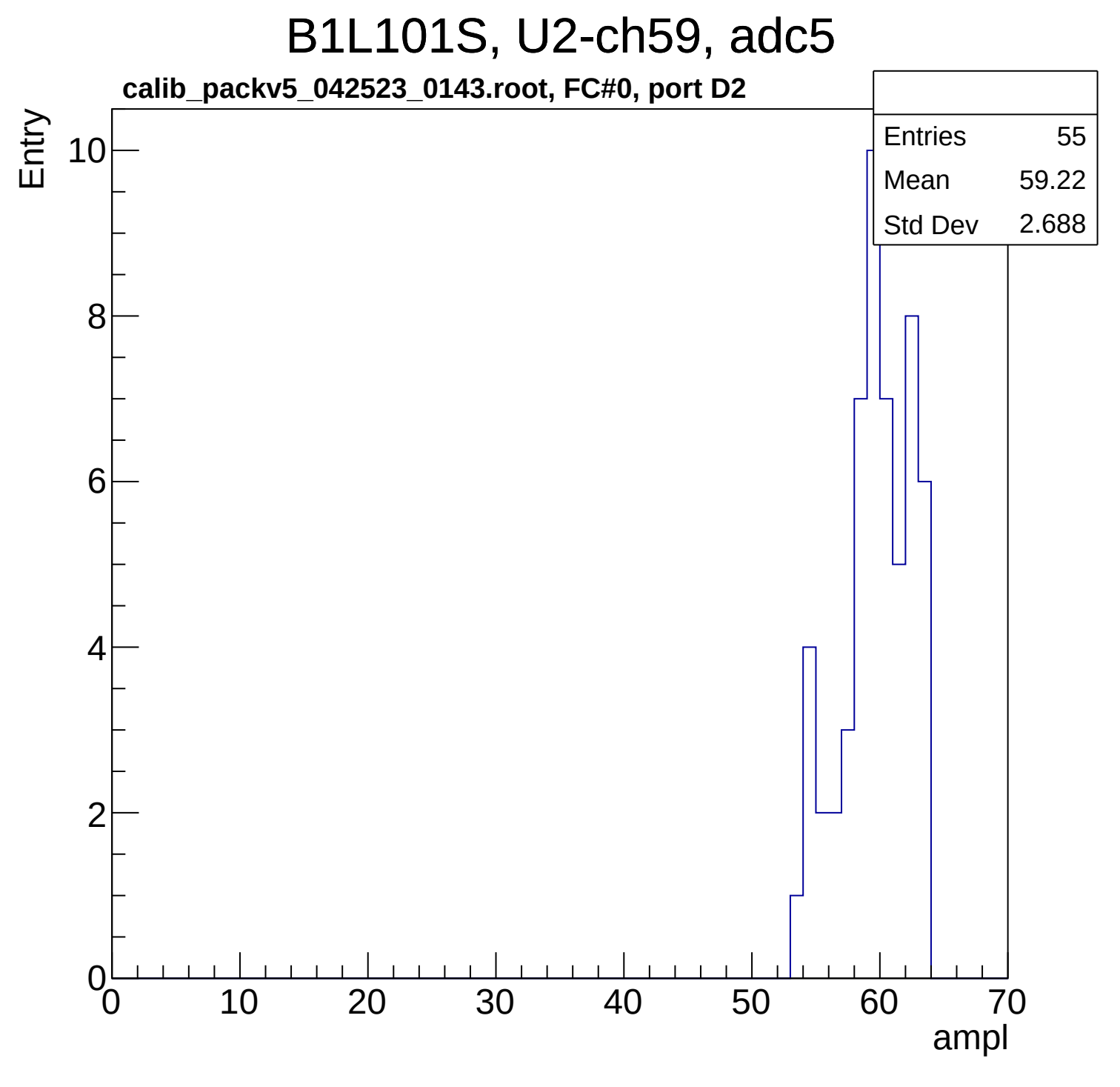

B1L101S, U2-ch59, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 27.86
Std Dev 5.643
Gaus mean : 28.8308
Gaus Width: 3.1004
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

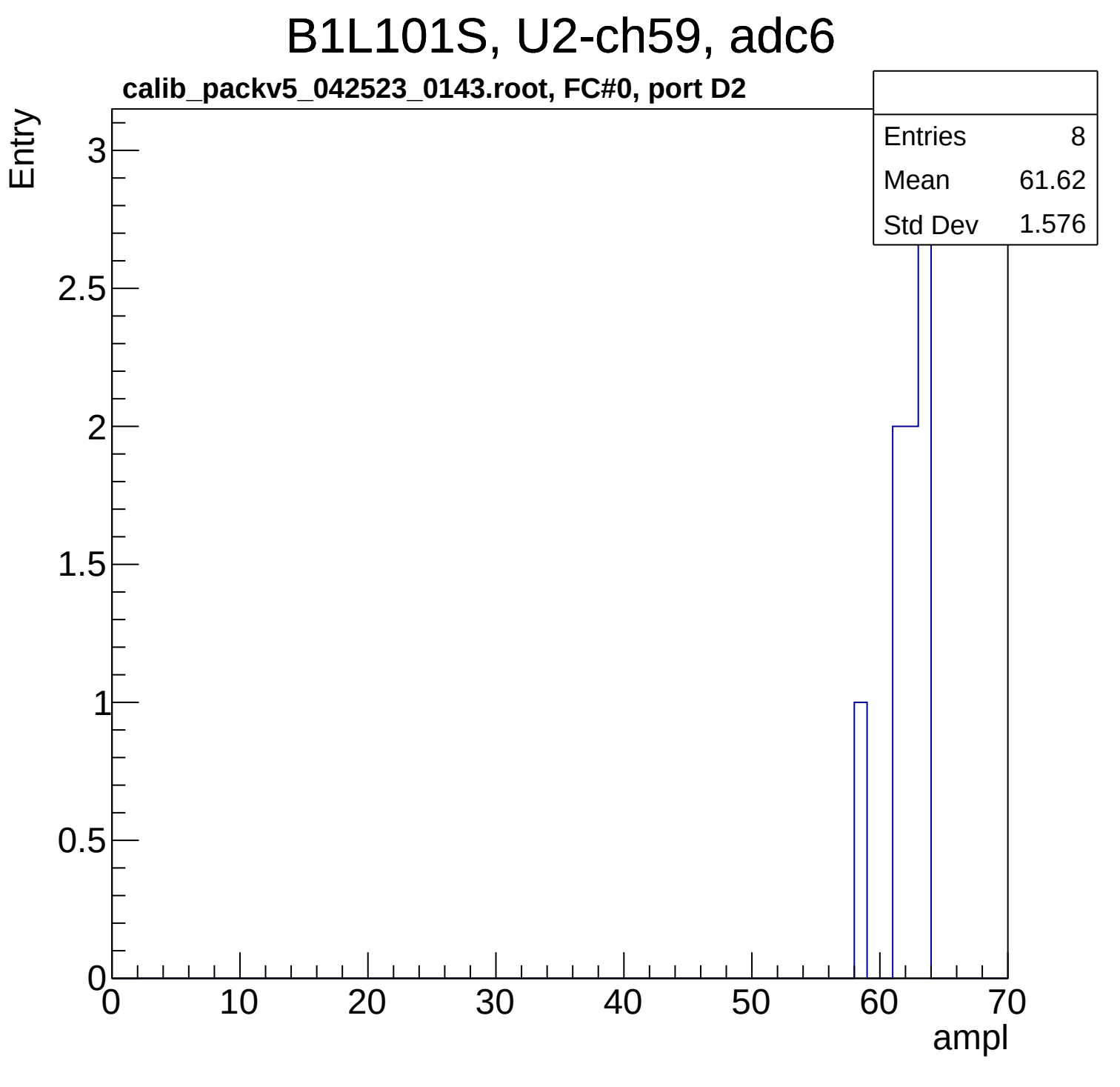

B1L101S, U2-ch59, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 35.78
Std Dev 3.254
Gaus mean : 36.3289
Gaus Width: 3.6694
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

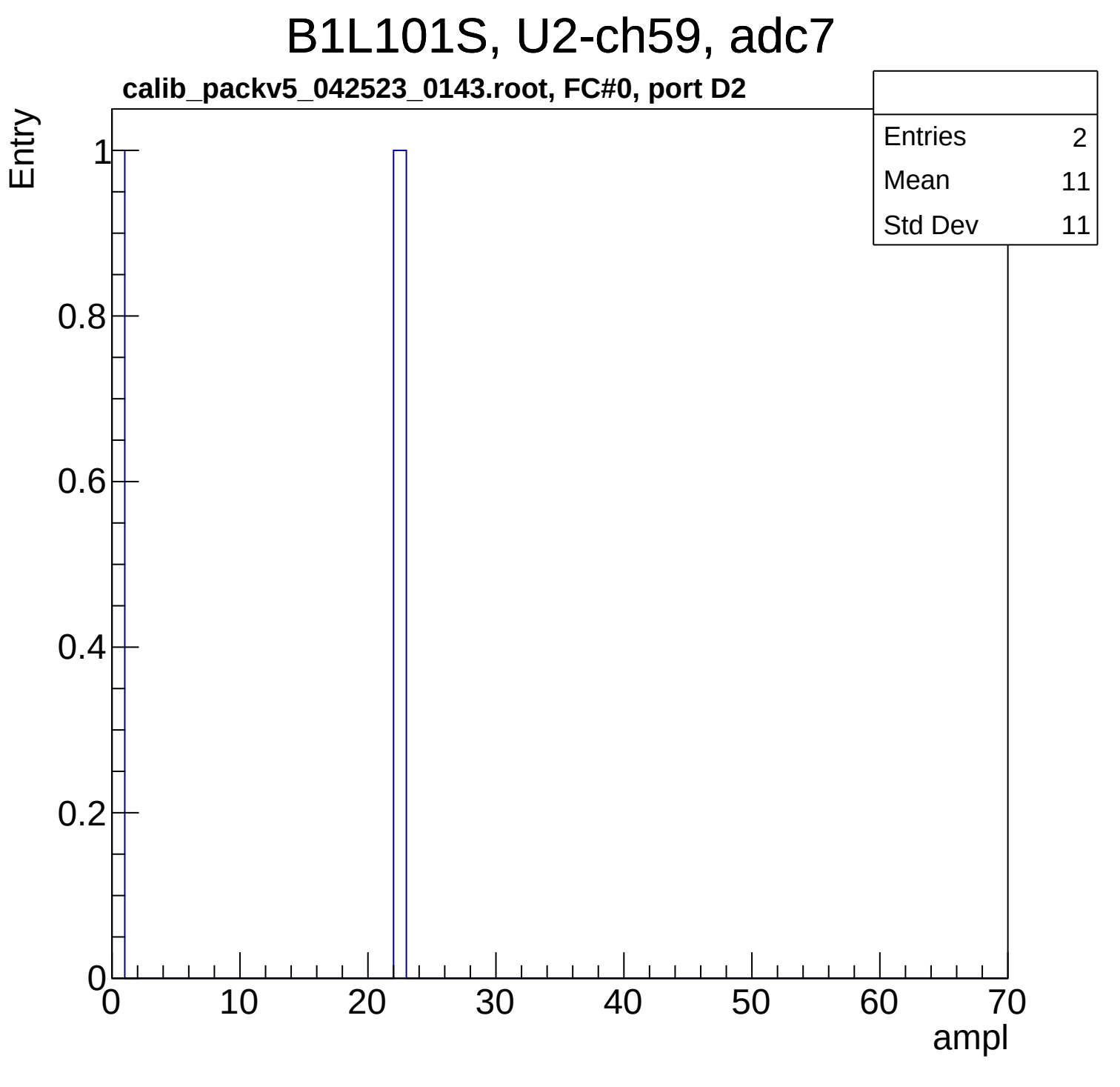

B1L101S, U2-ch59, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 42.69
Std Dev 3.583
Gaus mean : 42.7705
Gaus Width: 2.7598
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

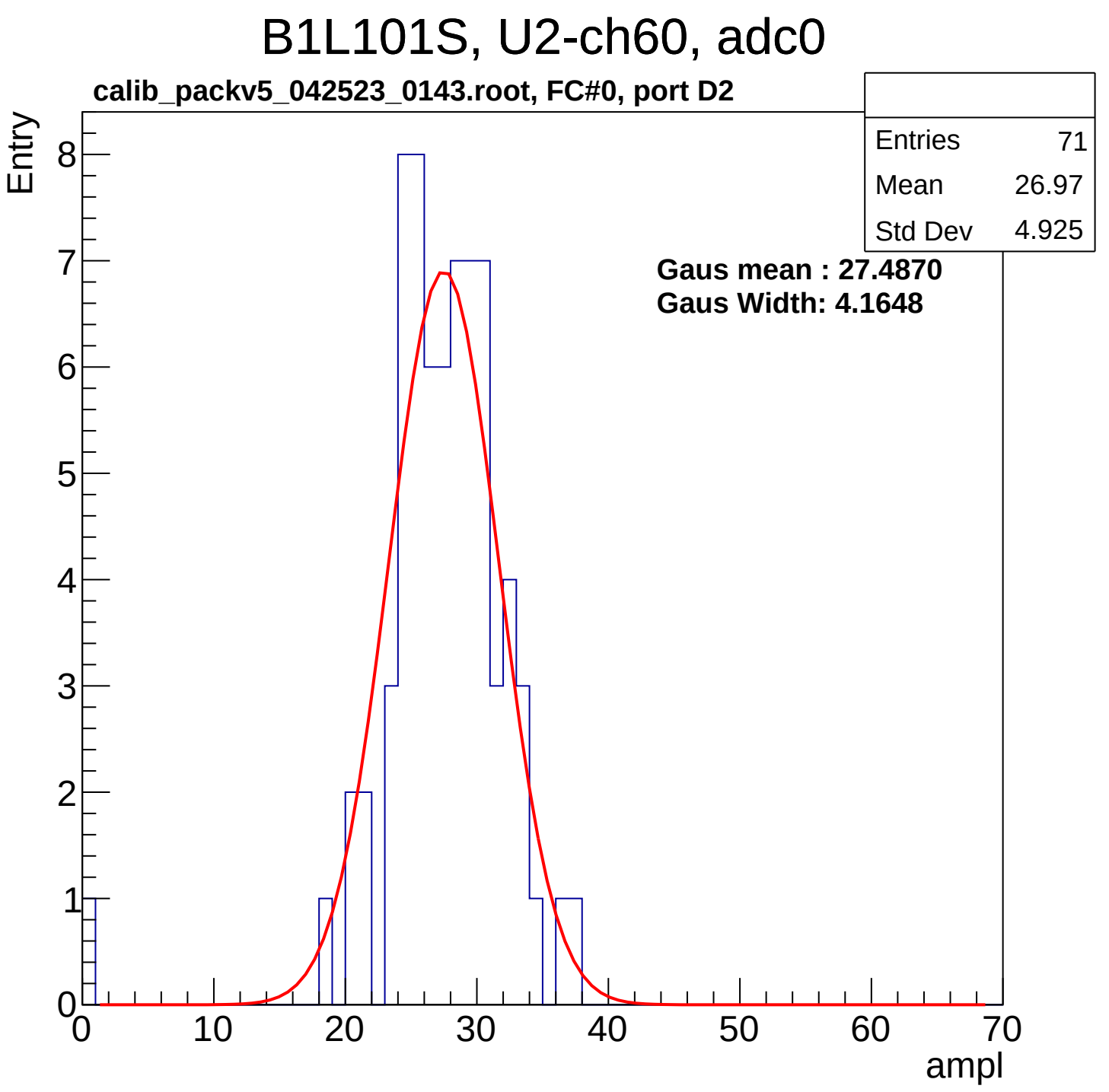

B1L101S, U2-ch59, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 48.3
Std Dev 3.035
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

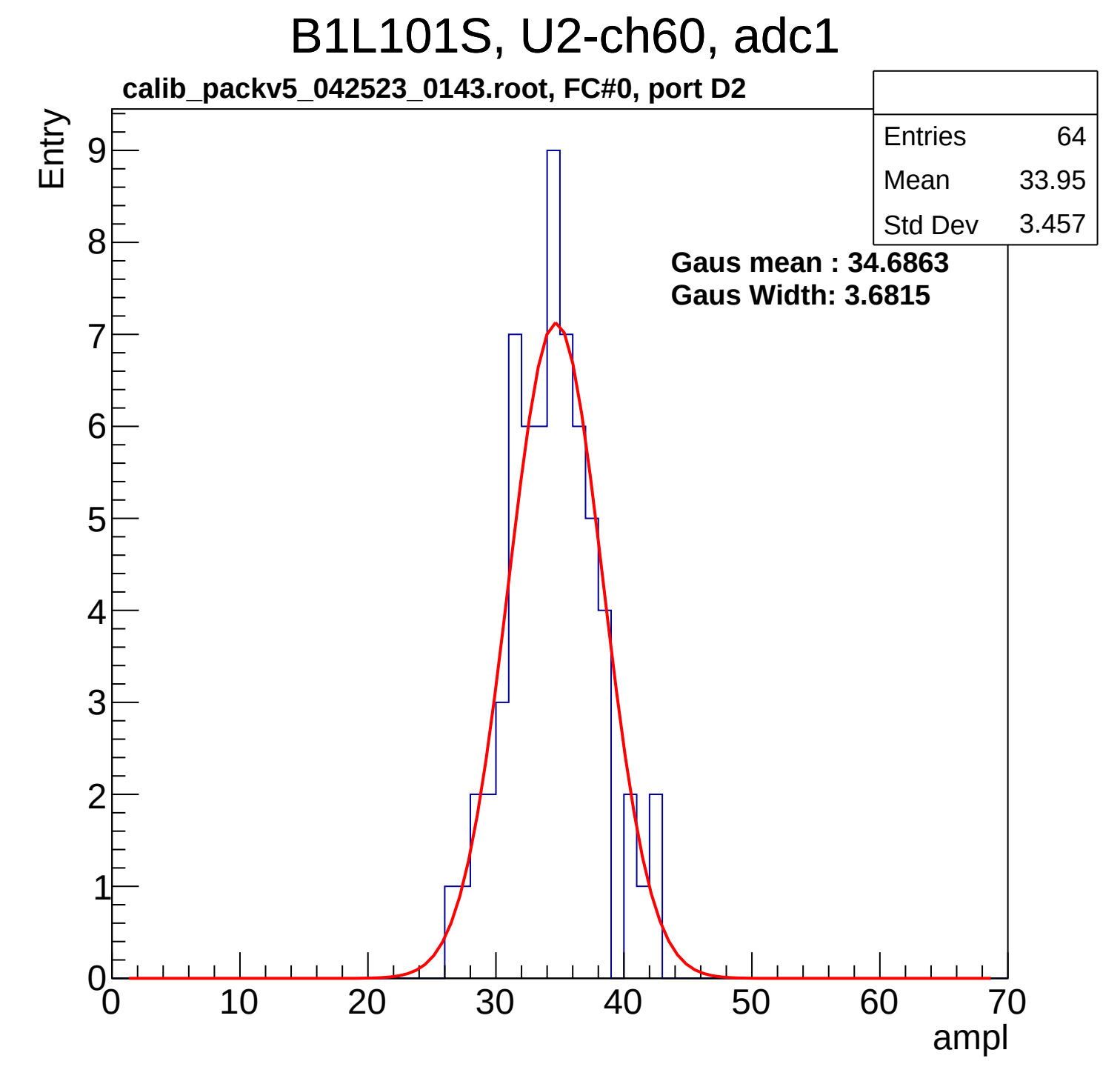

B1L101S, U2-ch59, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 53.93
Std Dev 8.026
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

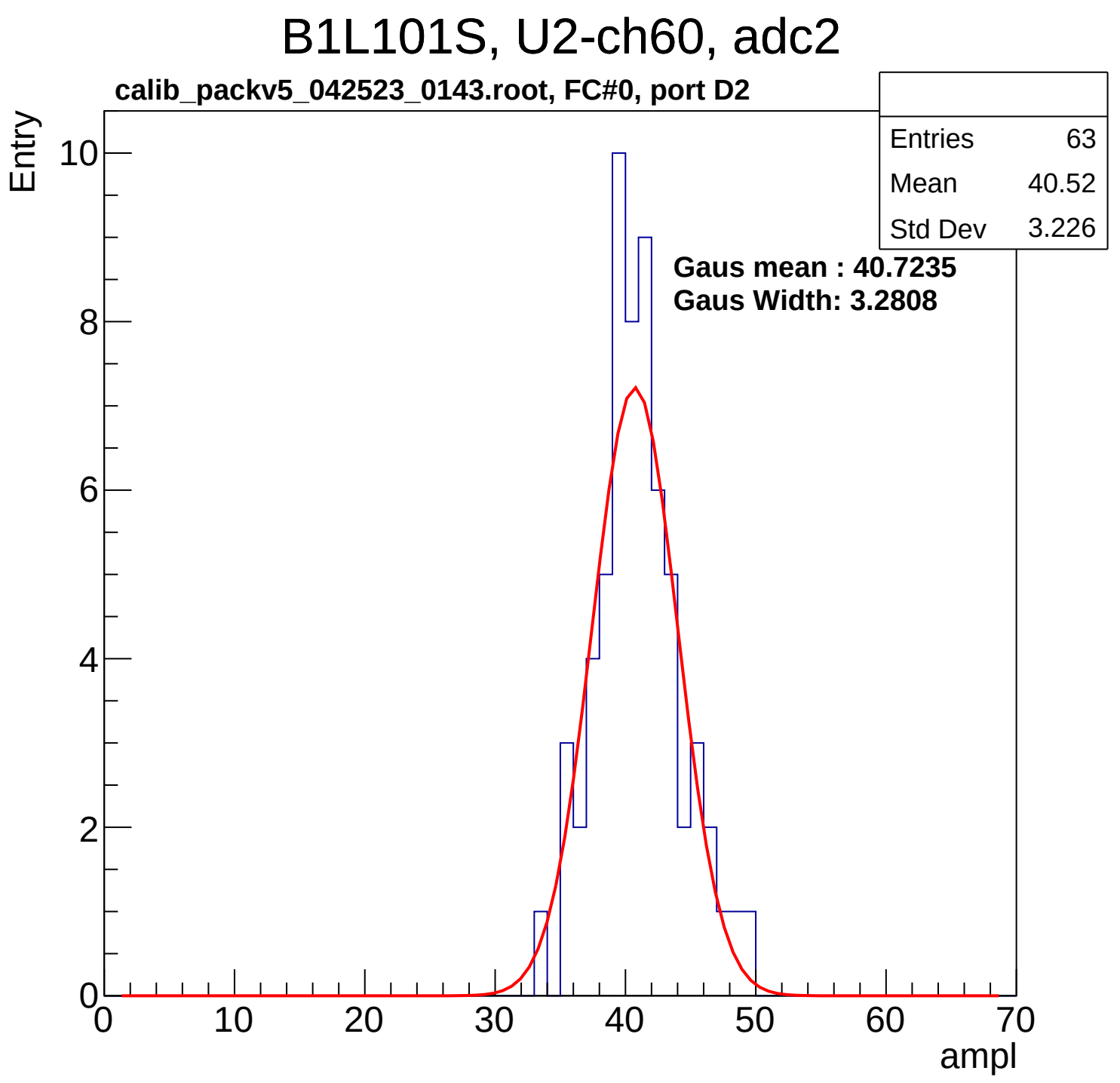

B1L101S, U2-ch59, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 59.22
Std Dev 2.688
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

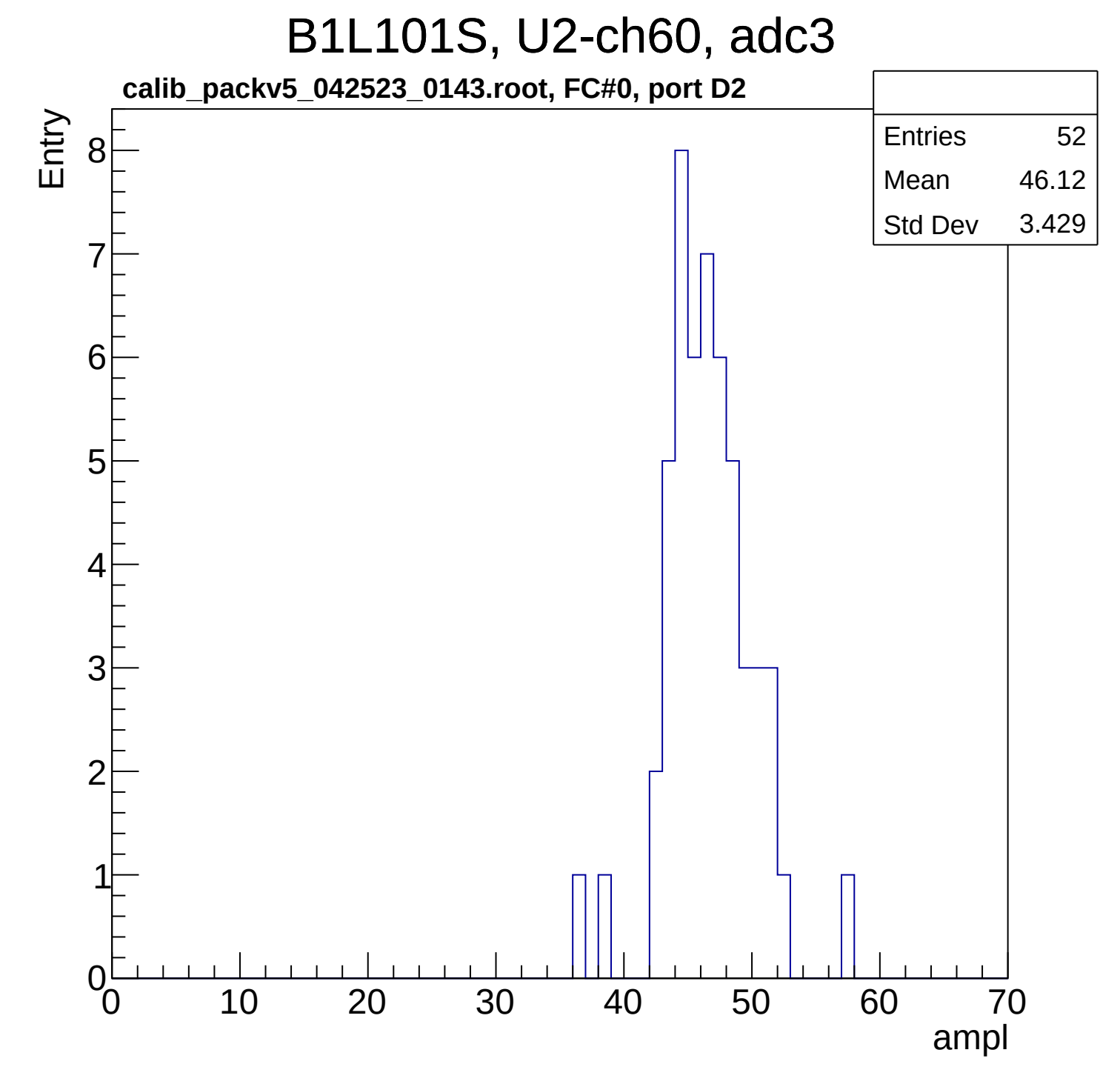

B1L101S, U2-ch59, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 61.62
Std Dev 1.576
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

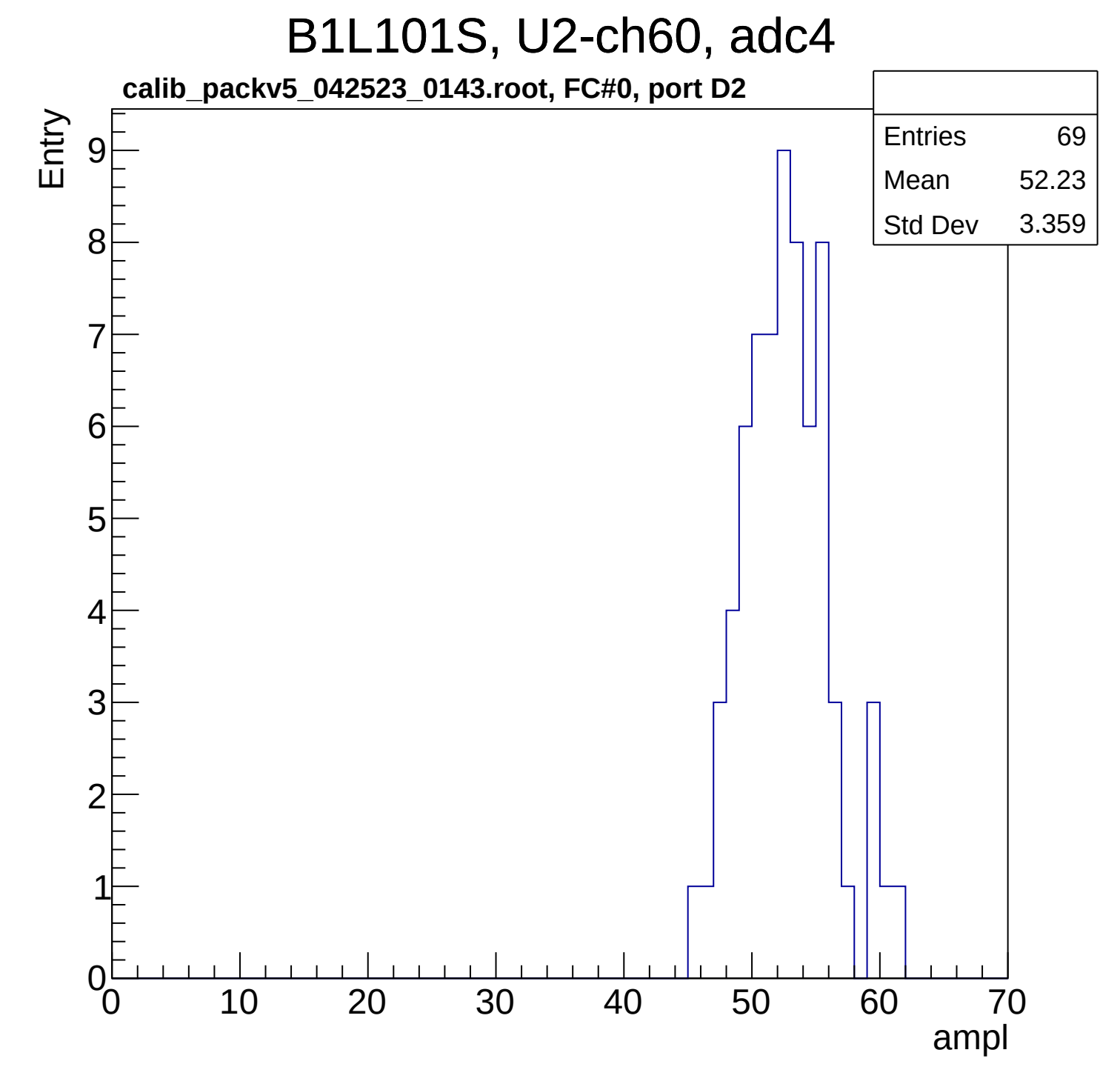

B1L101S, U2-ch59, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 11
Std Dev 11
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

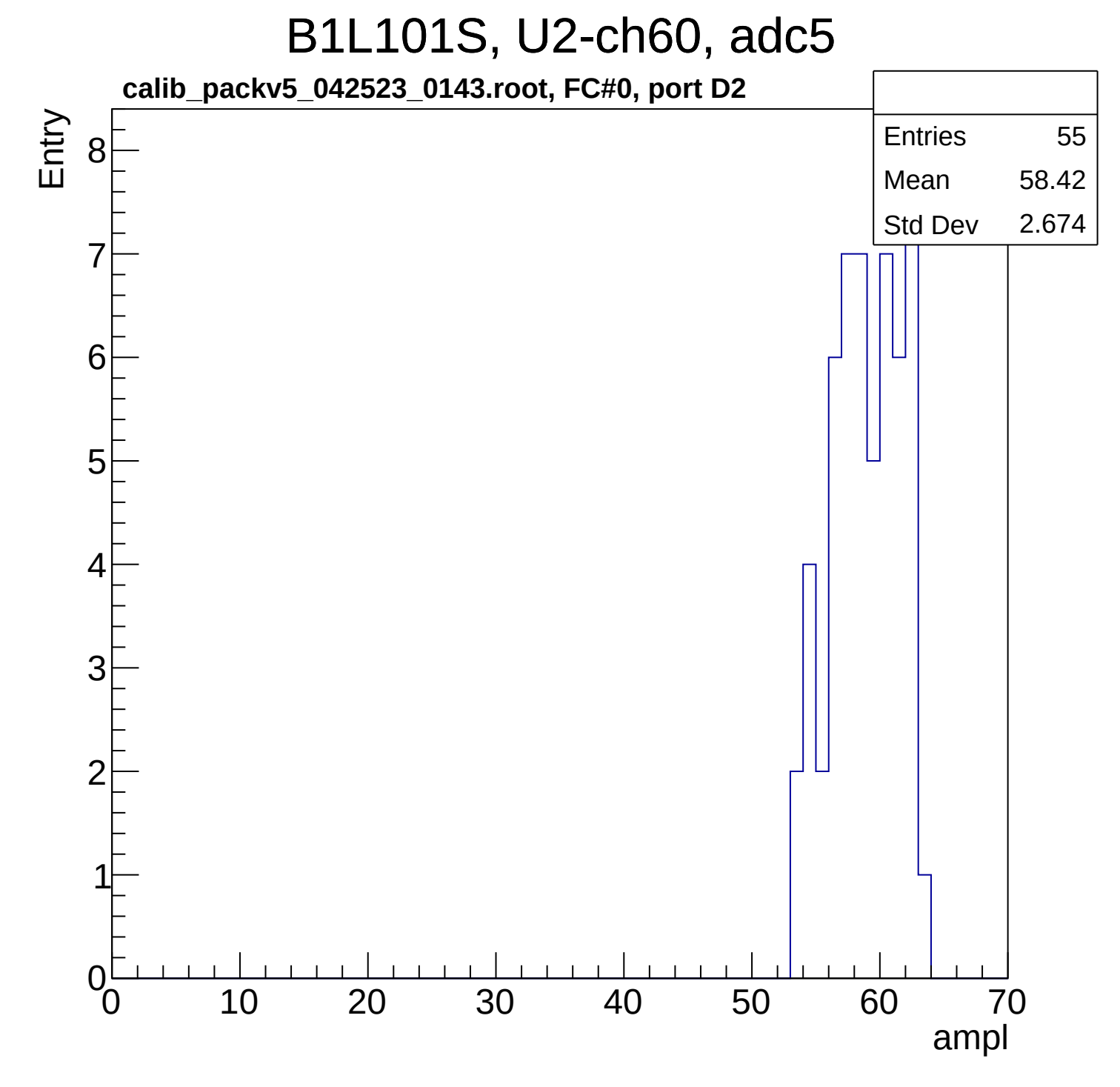

B1L101S, U2-ch60, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 26.97
Std Dev 4.925
Gaus mean : 27.4870
Gaus Width: 4.1648
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

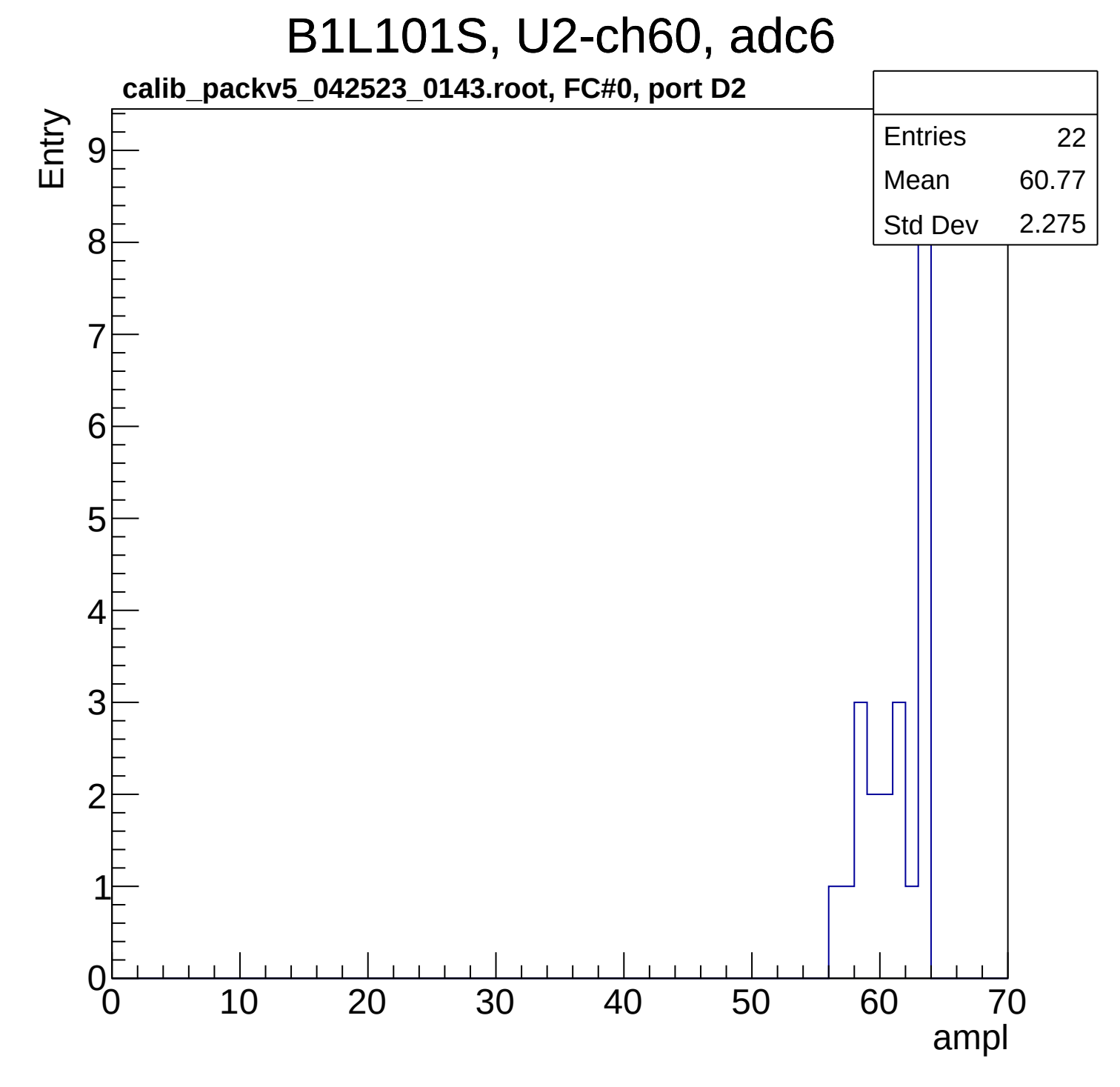

B1L101S, U2-ch60, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 33.95
Std Dev 3.457
Gaus mean : 34.6863
Gaus Width: 3.6815
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

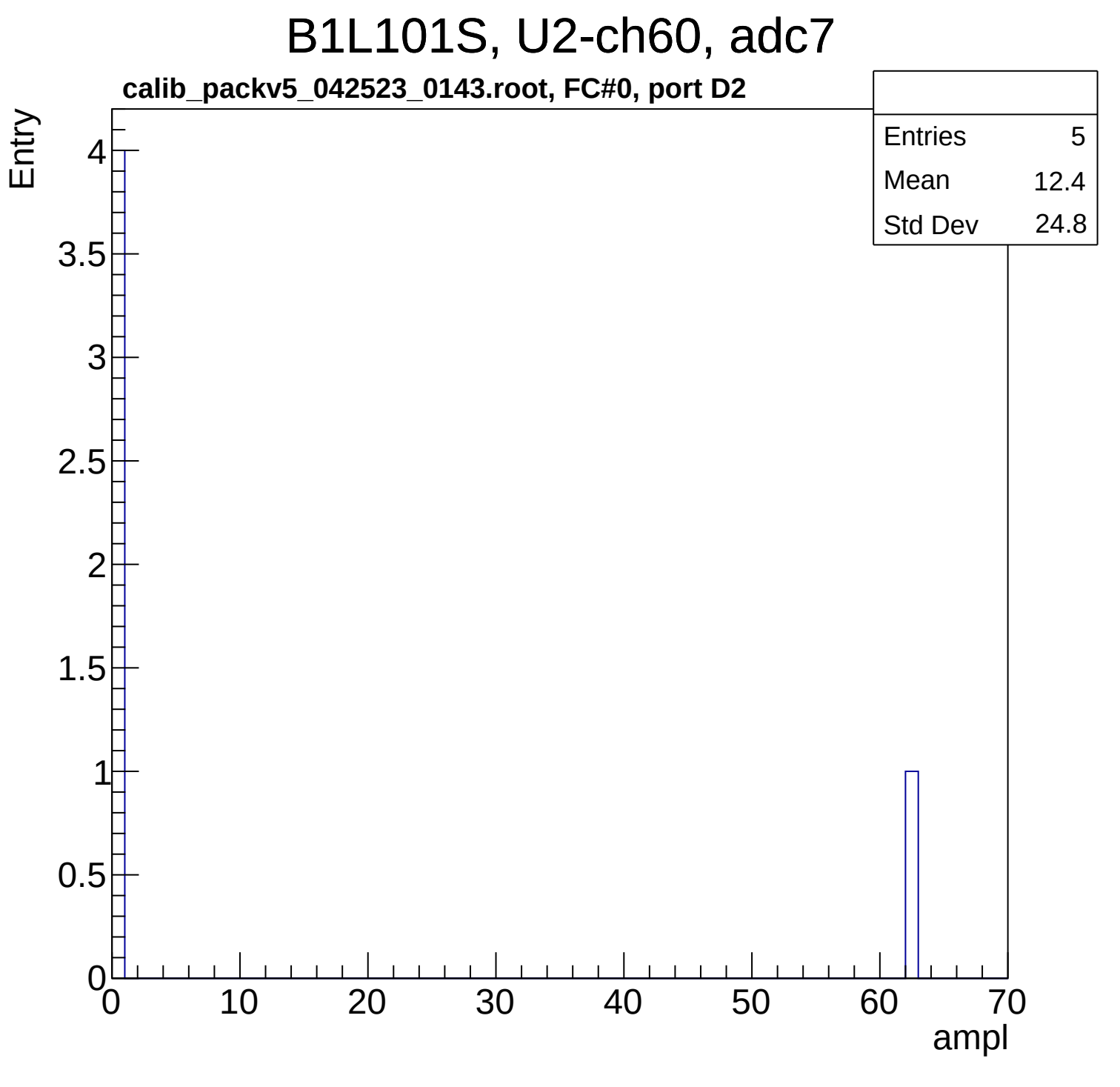

B1L101S, U2-ch60, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 40.52
Std Dev 3.226
Gaus mean : 40.7235
Gaus Width: 3.2808
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

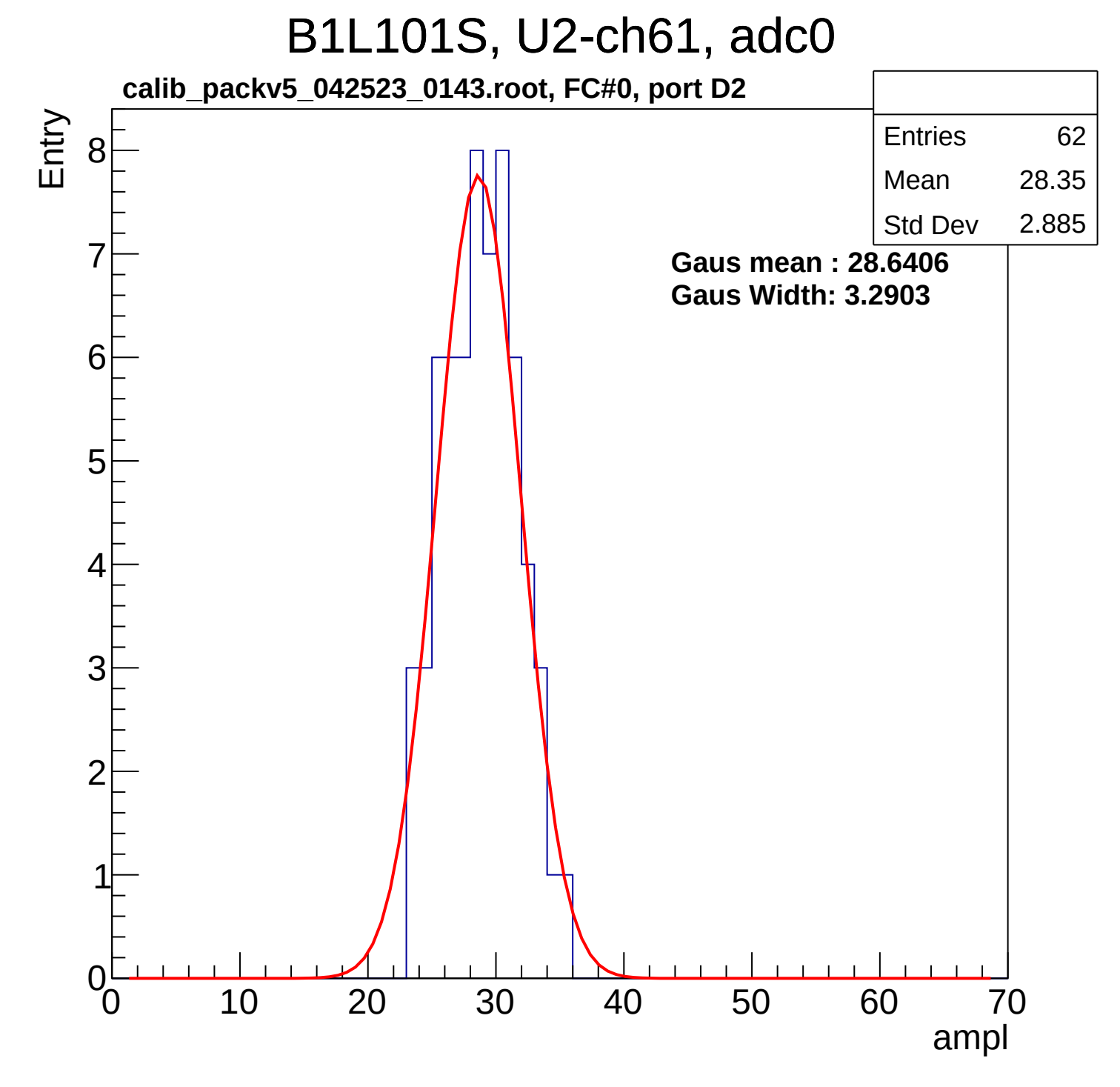

B1L101S, U2-ch60, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 46.12
Std Dev 3.429
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

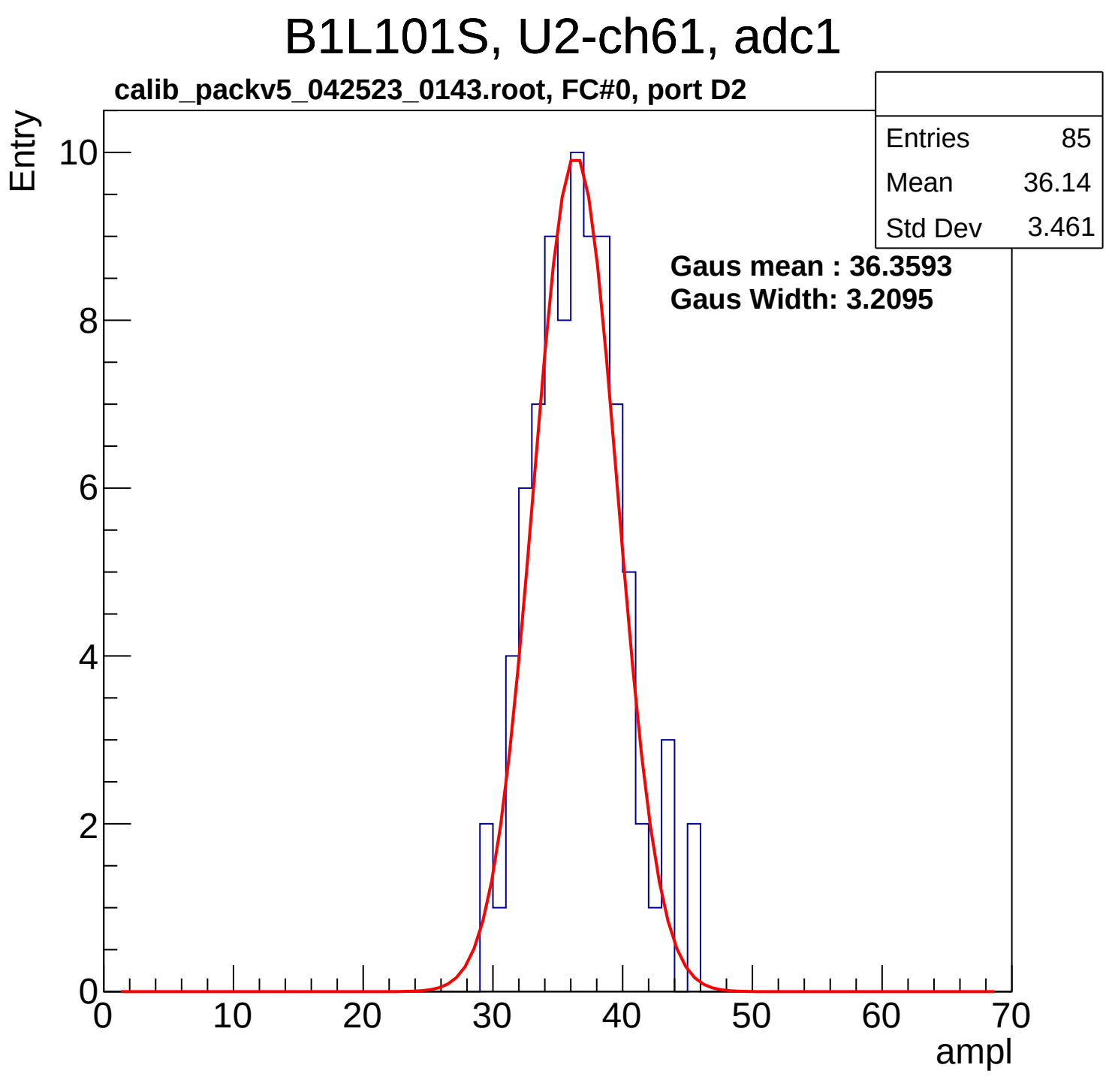

B1L101S, U2-ch60, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 52.23
Std Dev 3.359
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

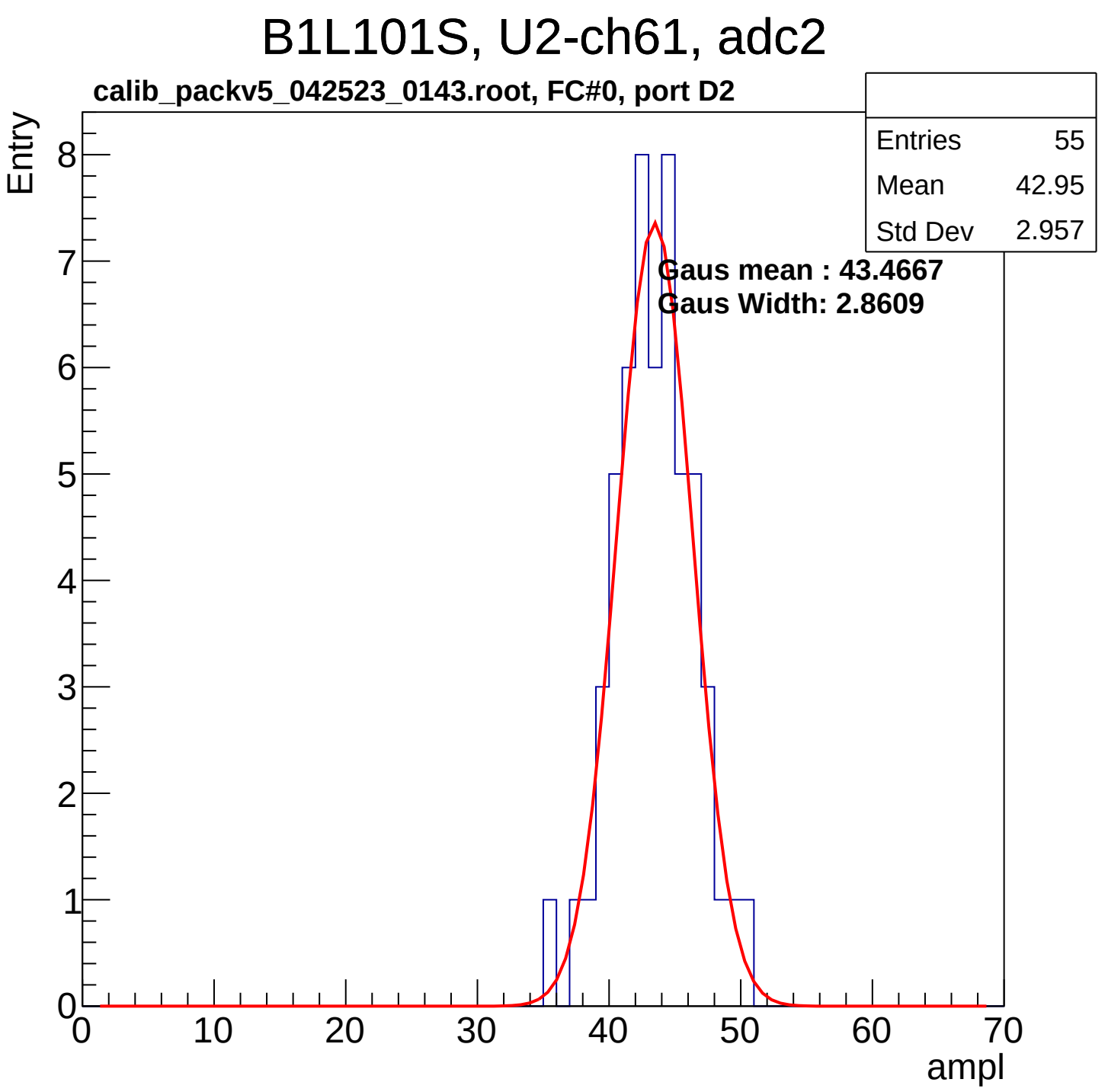

B1L101S, U2-ch60, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 58.42
Std Dev 2.674
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

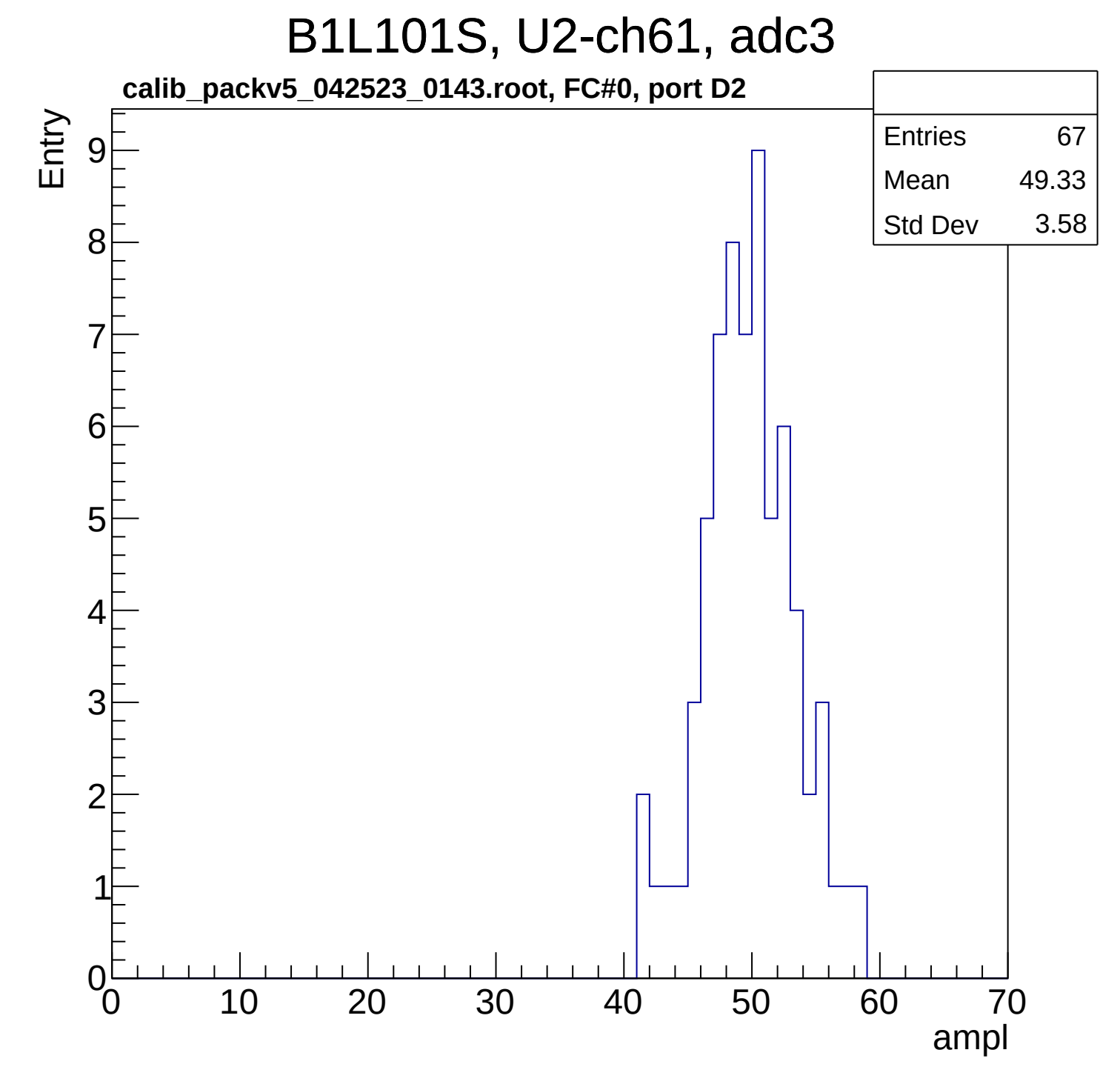

B1L101S, U2-ch60, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 22
Mean 60.77
Std Dev 2.275
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

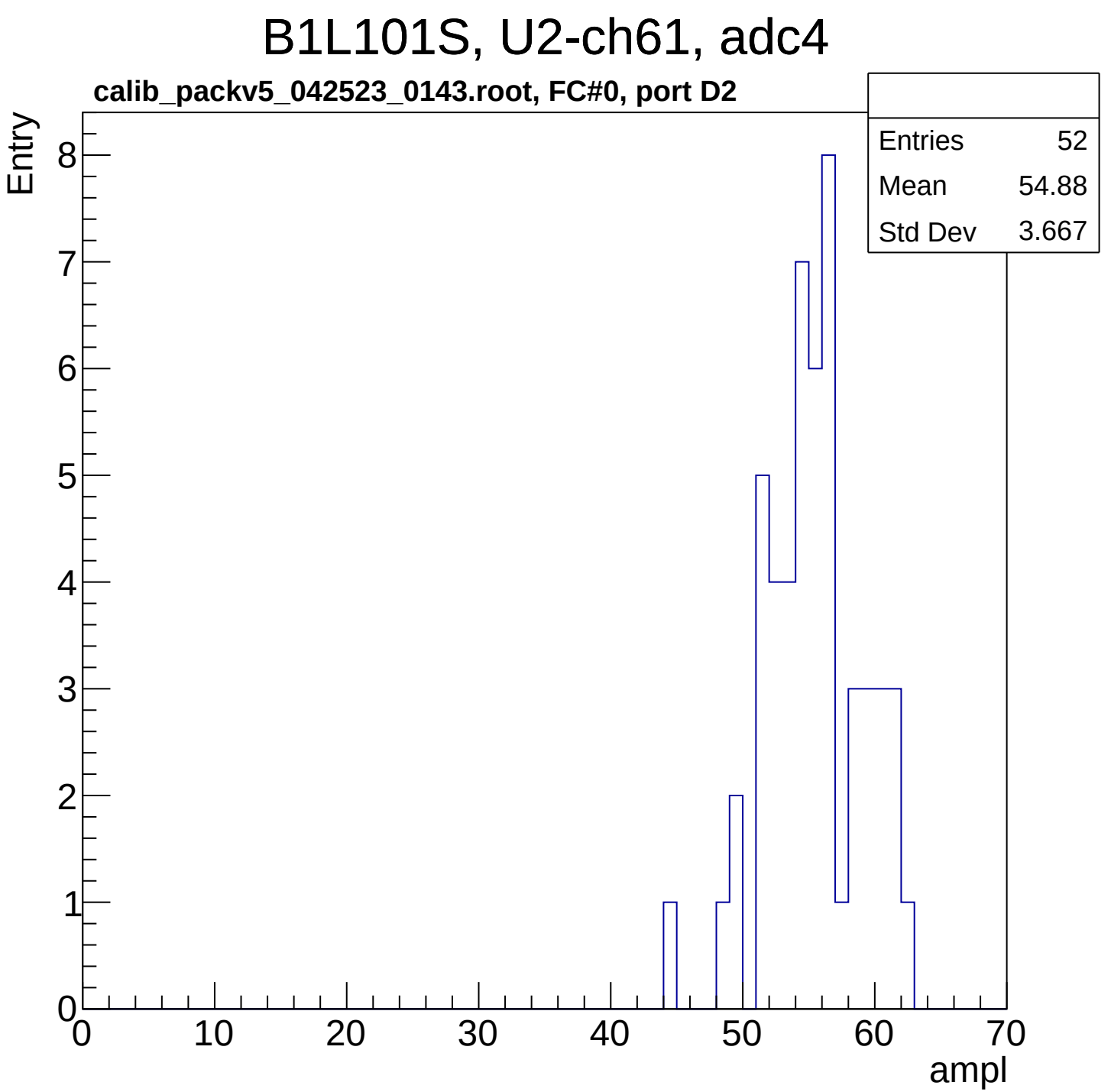

B1L101S, U2-ch60, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 12.4
Std Dev 24.8
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

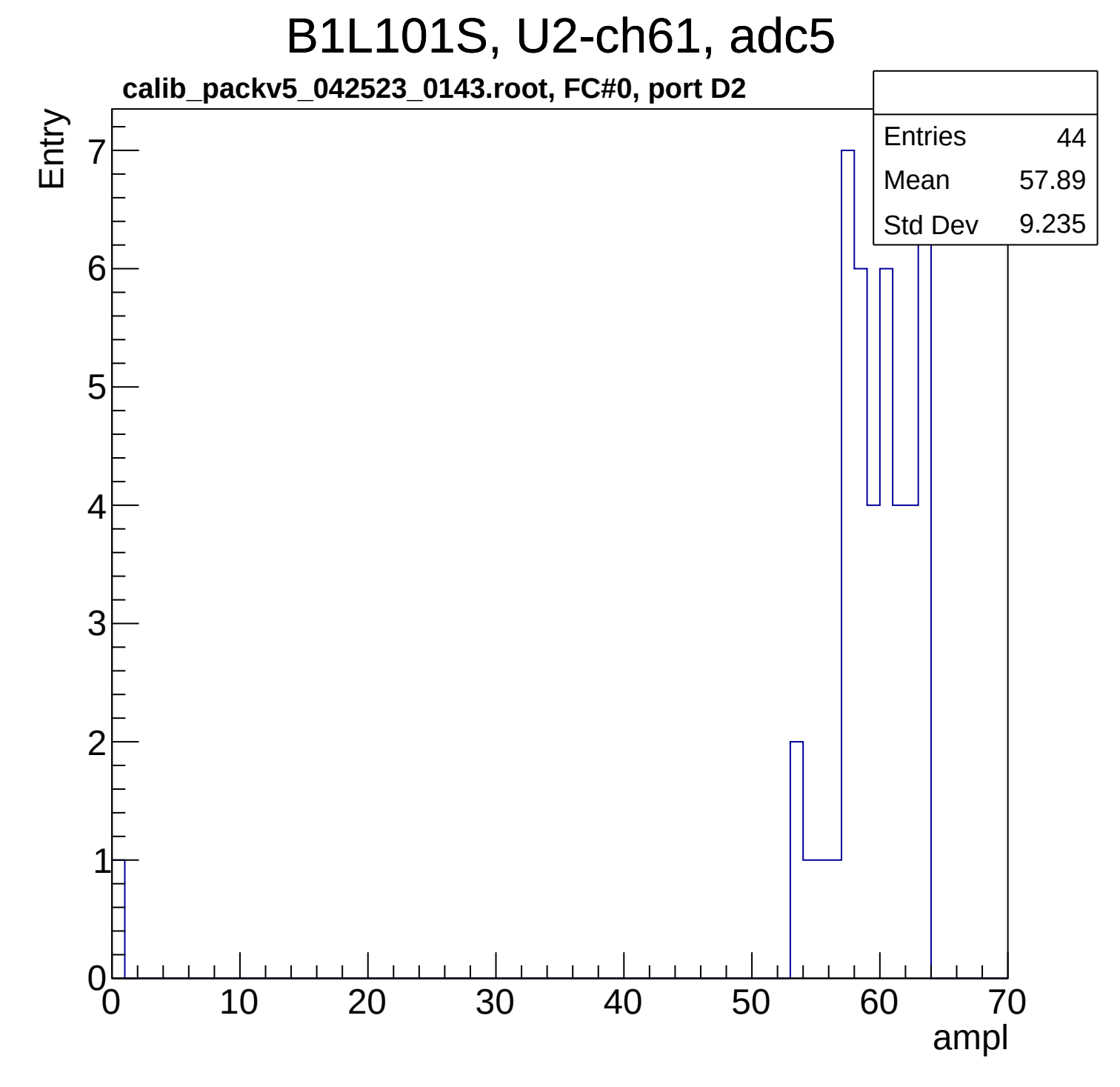

B1L101S, U2-ch61, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 28.35
Std Dev 2.885
Gaus mean : 28.6406
Gaus Width: 3.2903
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

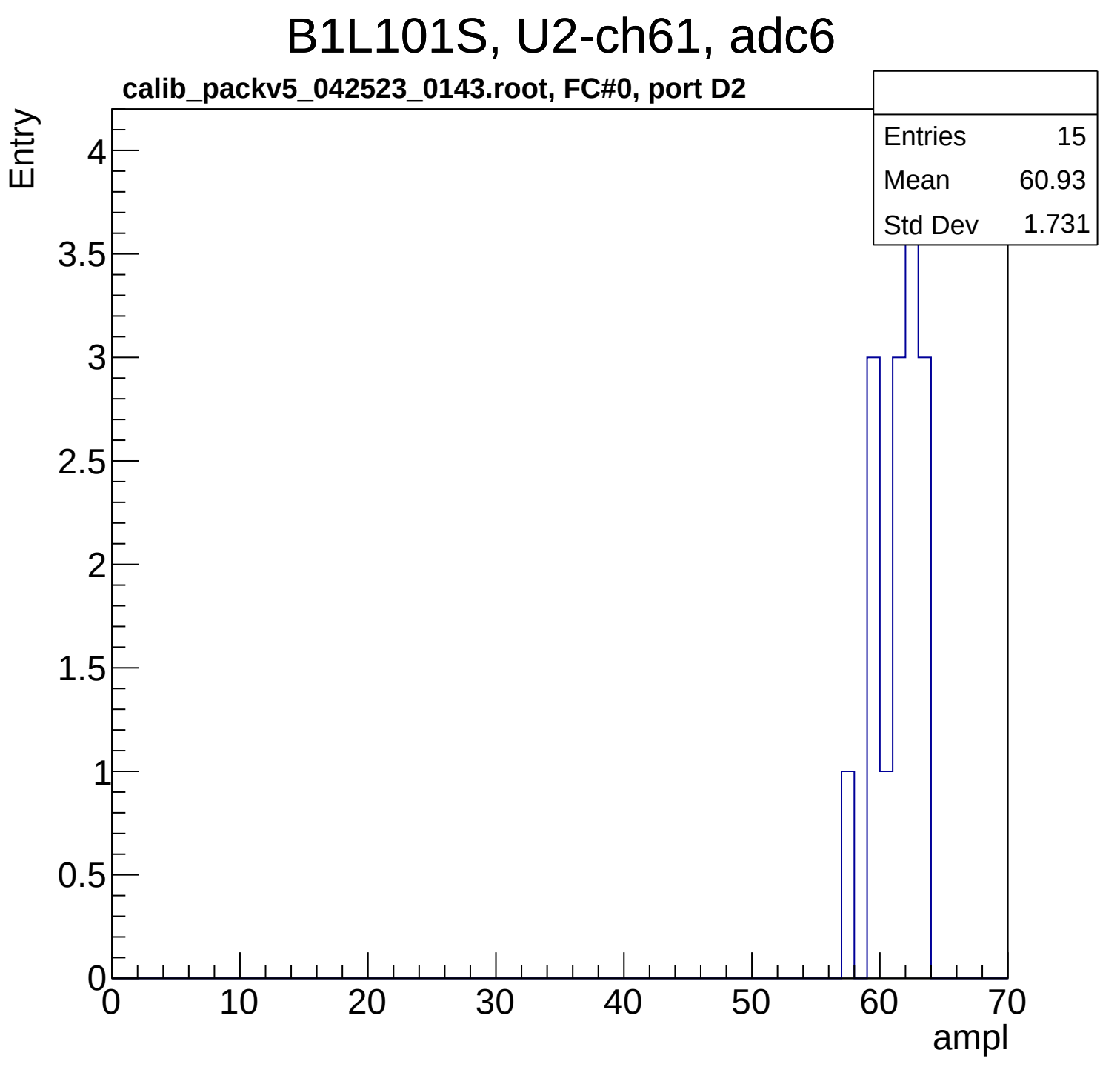

B1L101S, U2-ch61, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 85
Mean 36.14
Std Dev 3.461
Gaus mean : 36.3593
Gaus Width: 3.2095
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

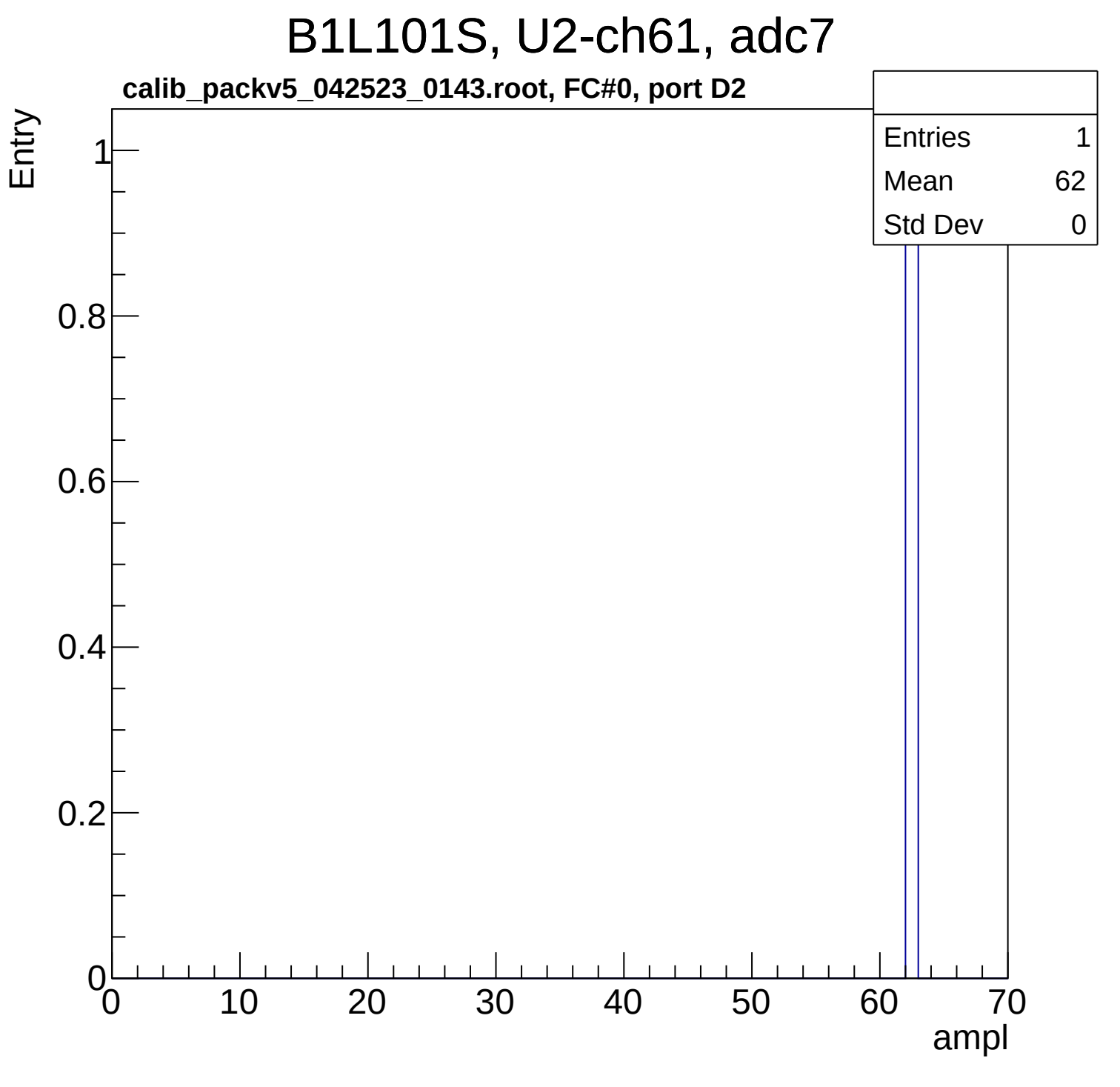

B1L101S, U2-ch61, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 42.95
Std Dev 2.957
Gaus mean : 43.4667
Gaus Width: 2.8609
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

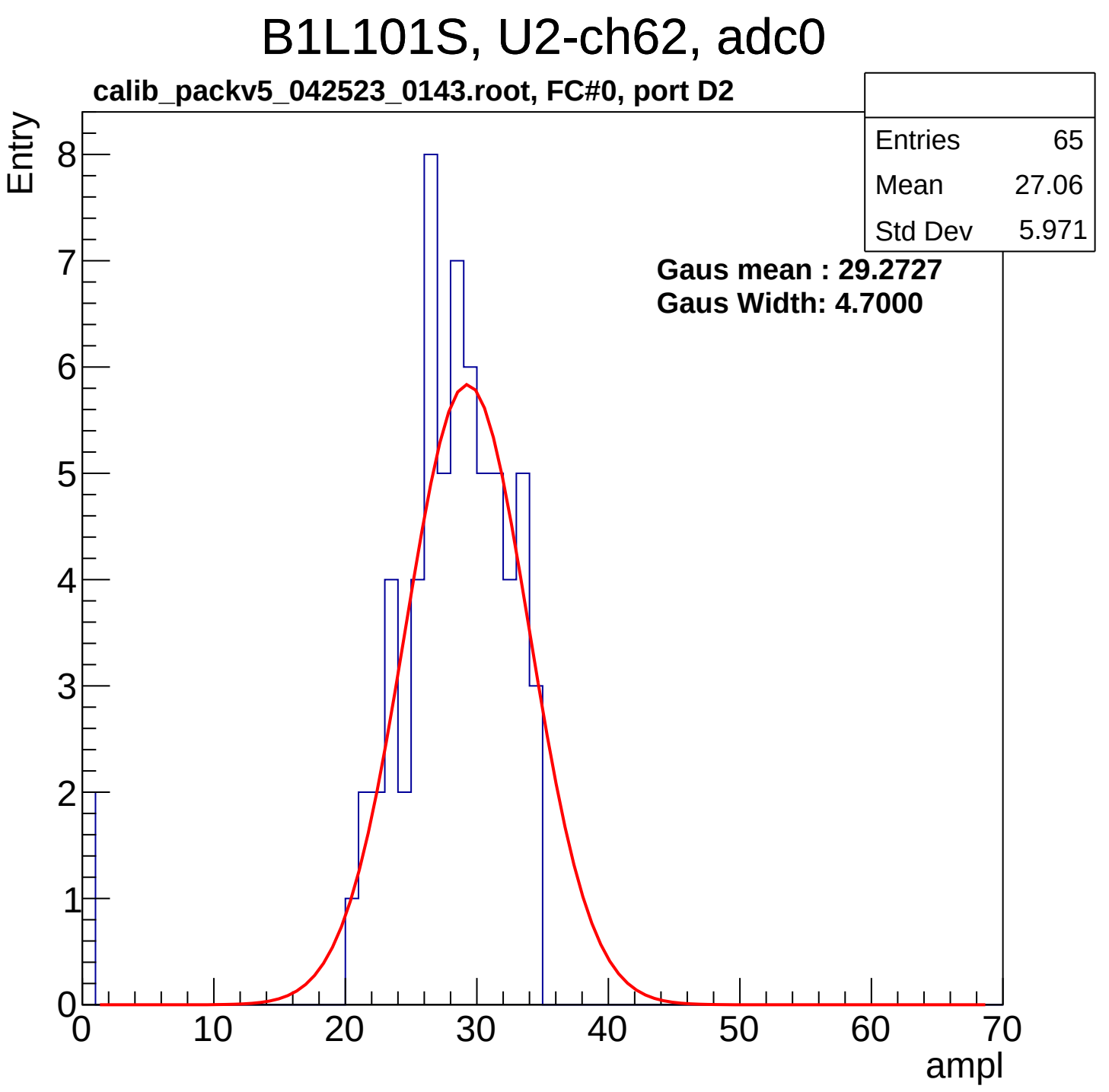

B1L101S, U2-ch61, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 49.33
Std Dev 3.58
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

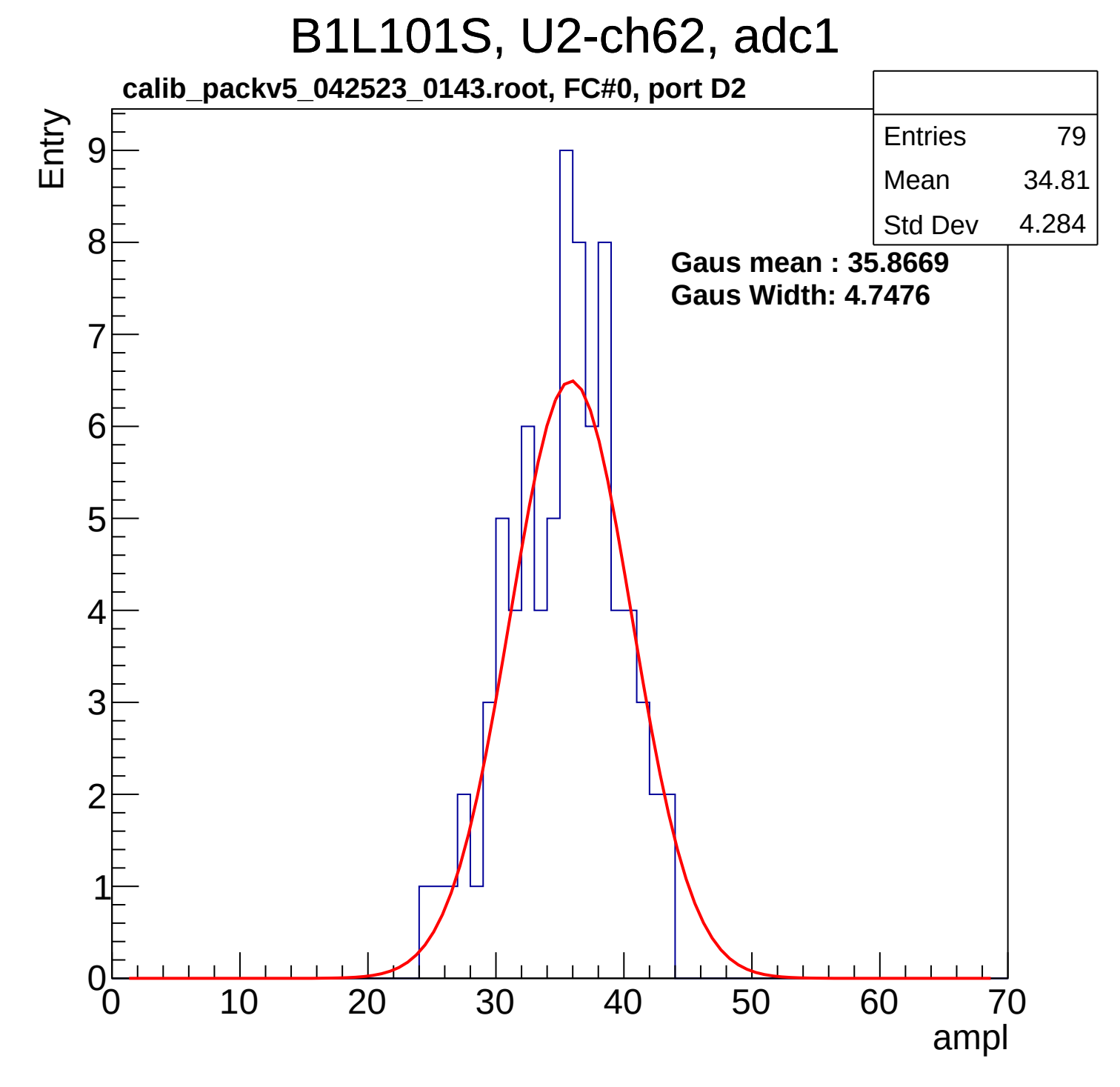

B1L101S, U2-ch61, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 54.88
Std Dev 3.667
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

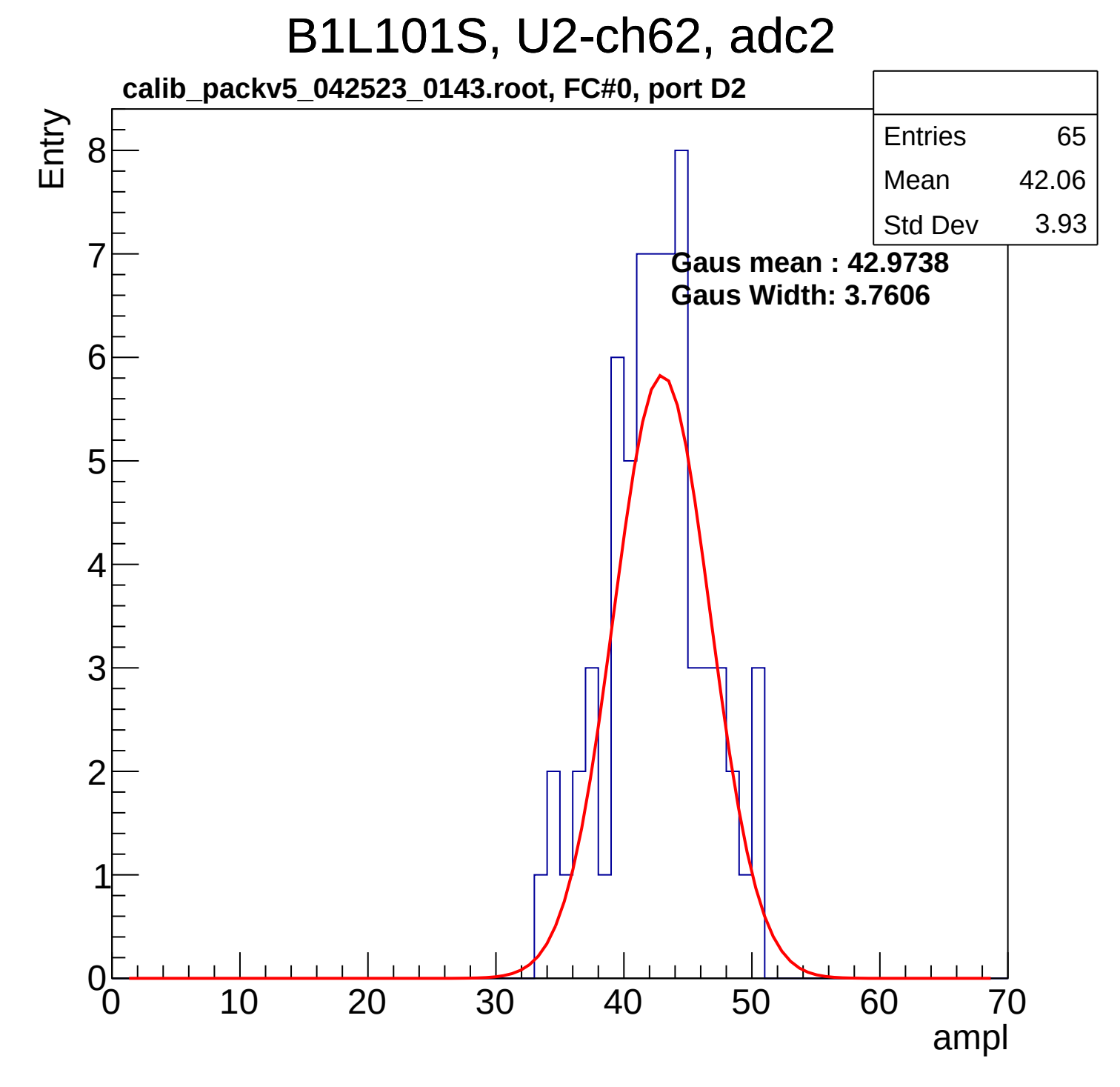

B1L101S, U2-ch61, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 44
Mean 57.89
Std Dev 9.235
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

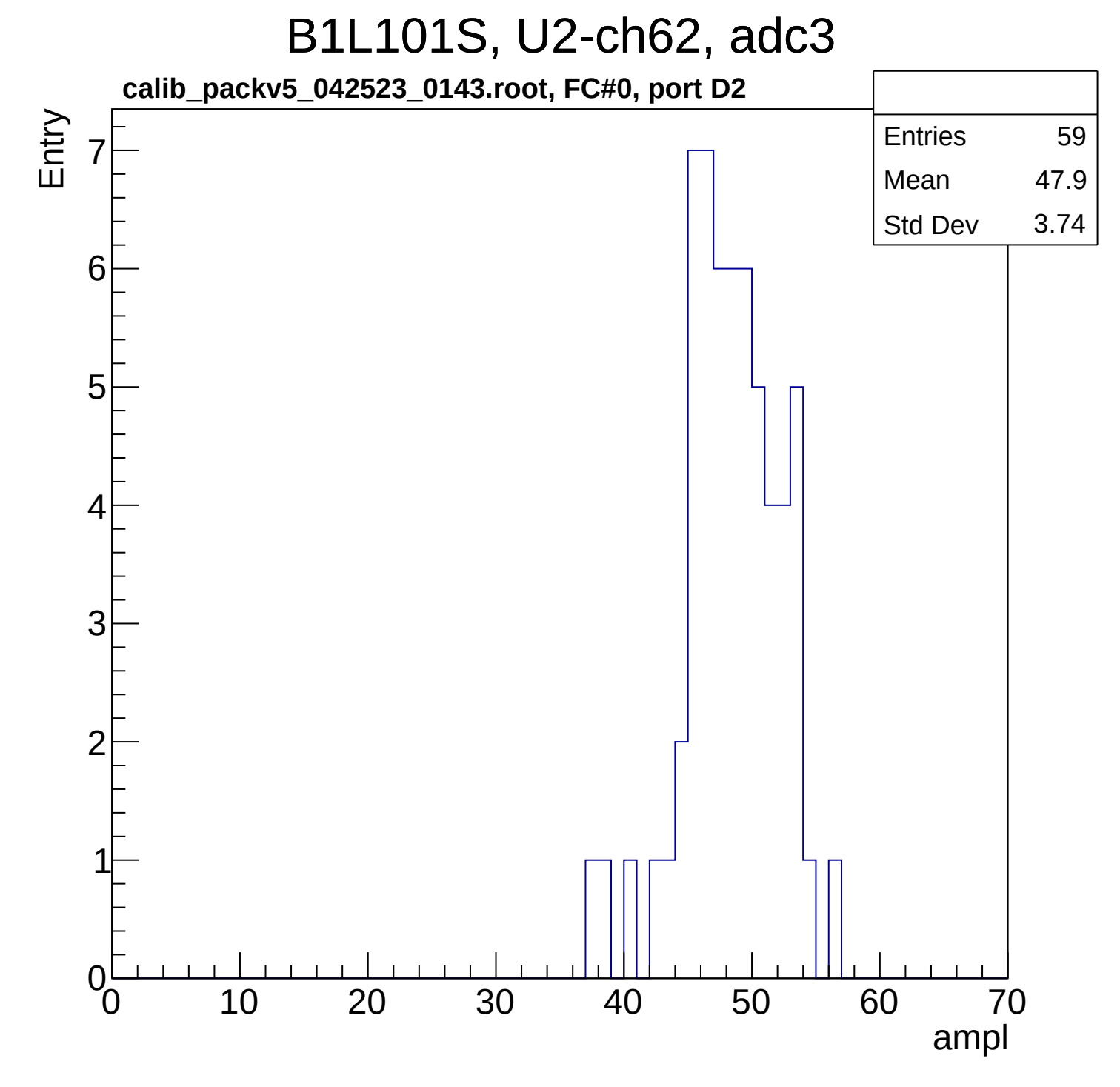

B1L101S, U2-ch61, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 15
Mean 60.93
Std Dev 1.731
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

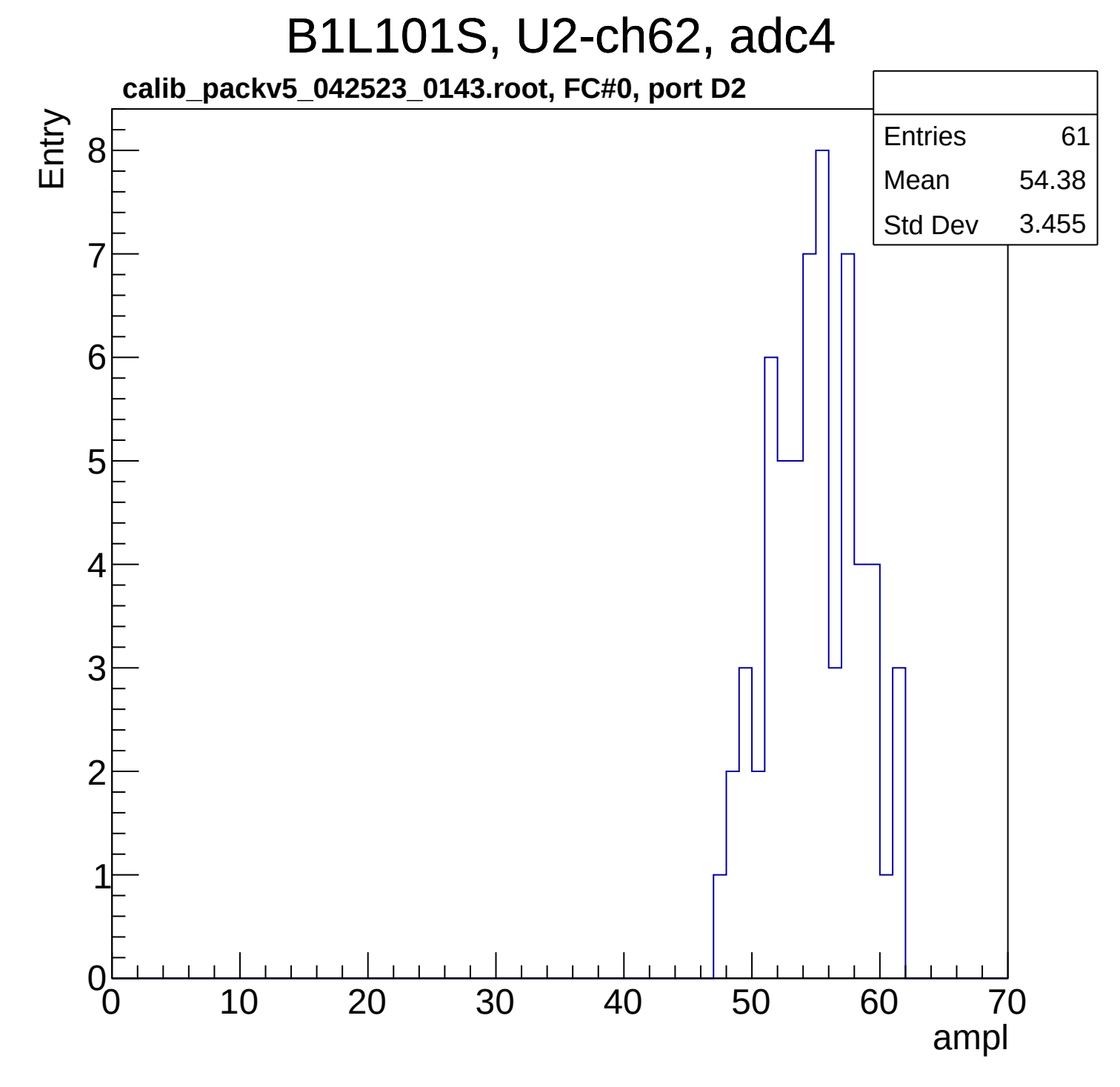

B1L101S, U2-ch61, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

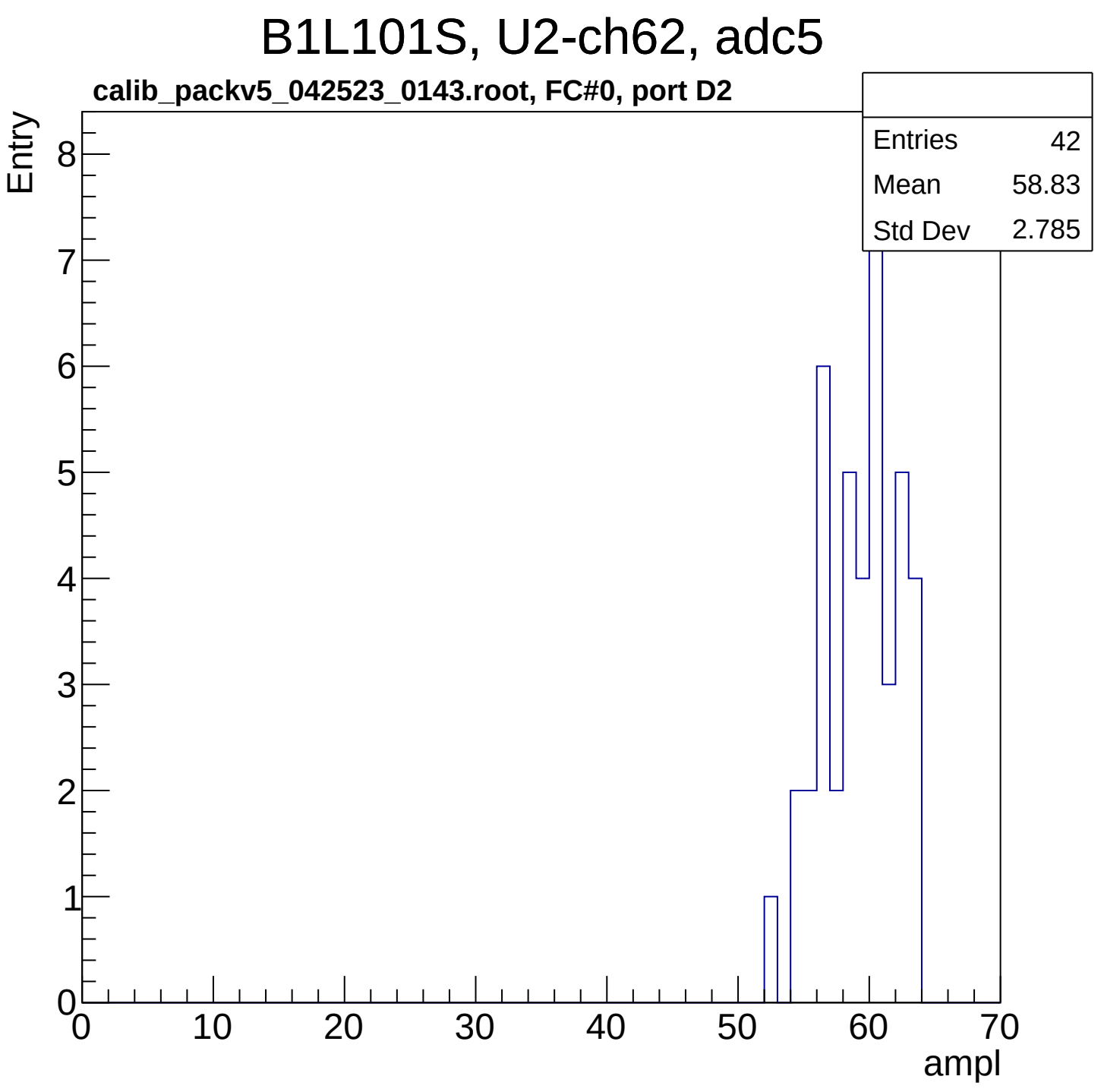

B1L101S, U2-ch62, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 27.06
Std Dev 5.971
Gaus mean : 29.2727
Gaus Width: 4.7000
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

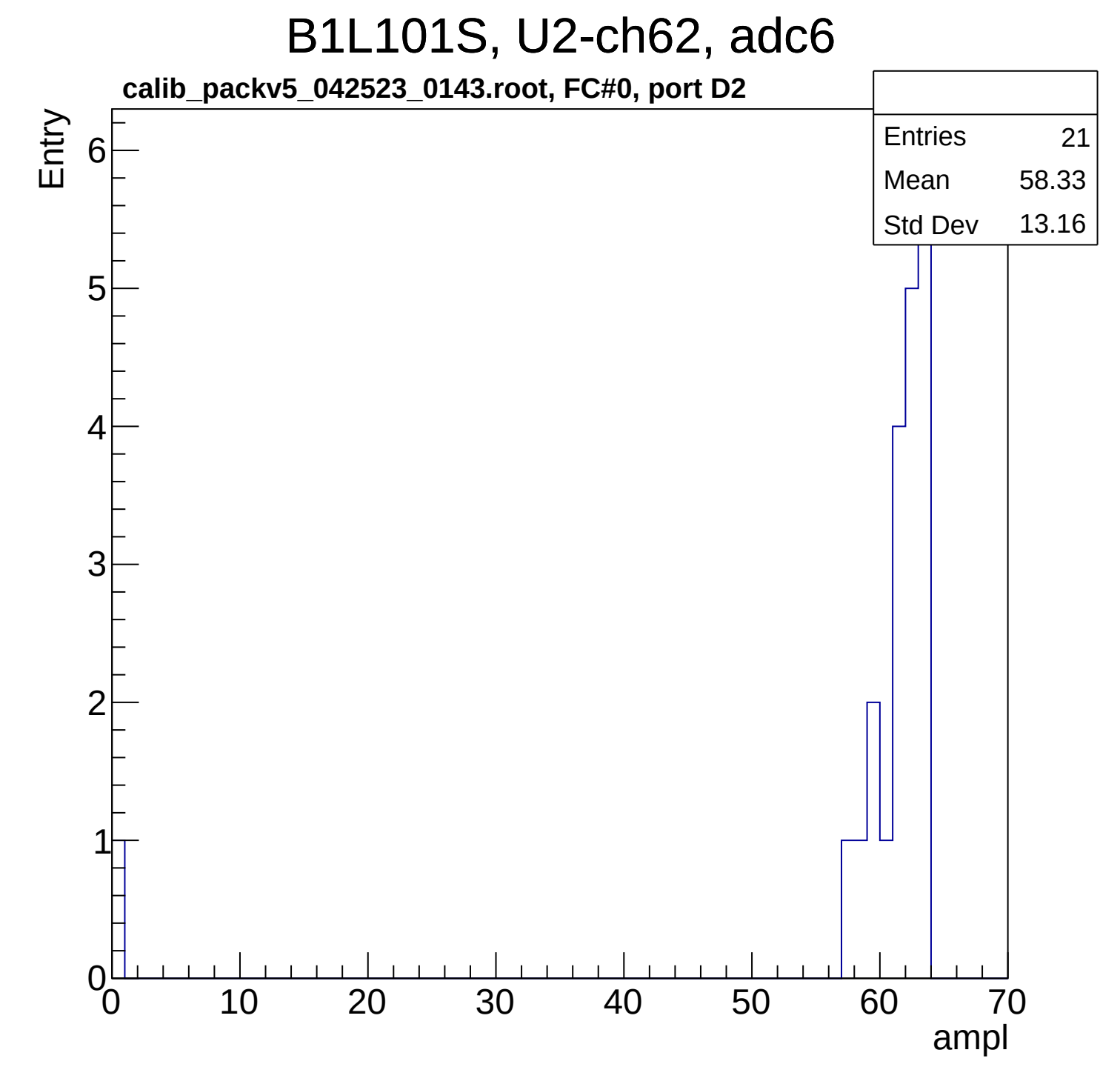

B1L101S, U2-ch62, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 34.81
Std Dev 4.284
Gaus mean : 35.8669
Gaus Width: 4.7476
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

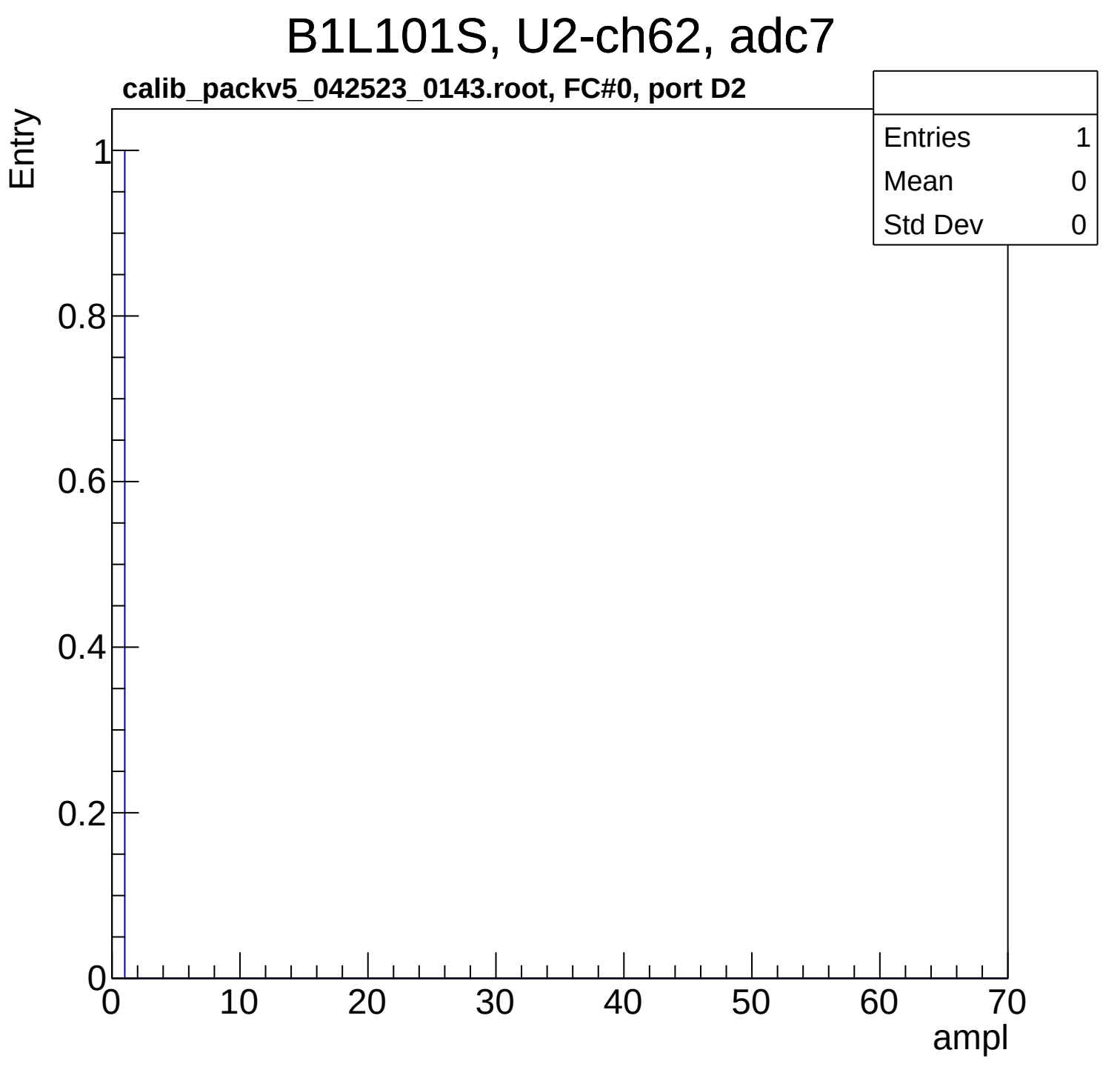

B1L101S, U2-ch62, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 42.06
Std Dev 3.93
Gaus mean : 42.9738
Gaus Width: 3.7606
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

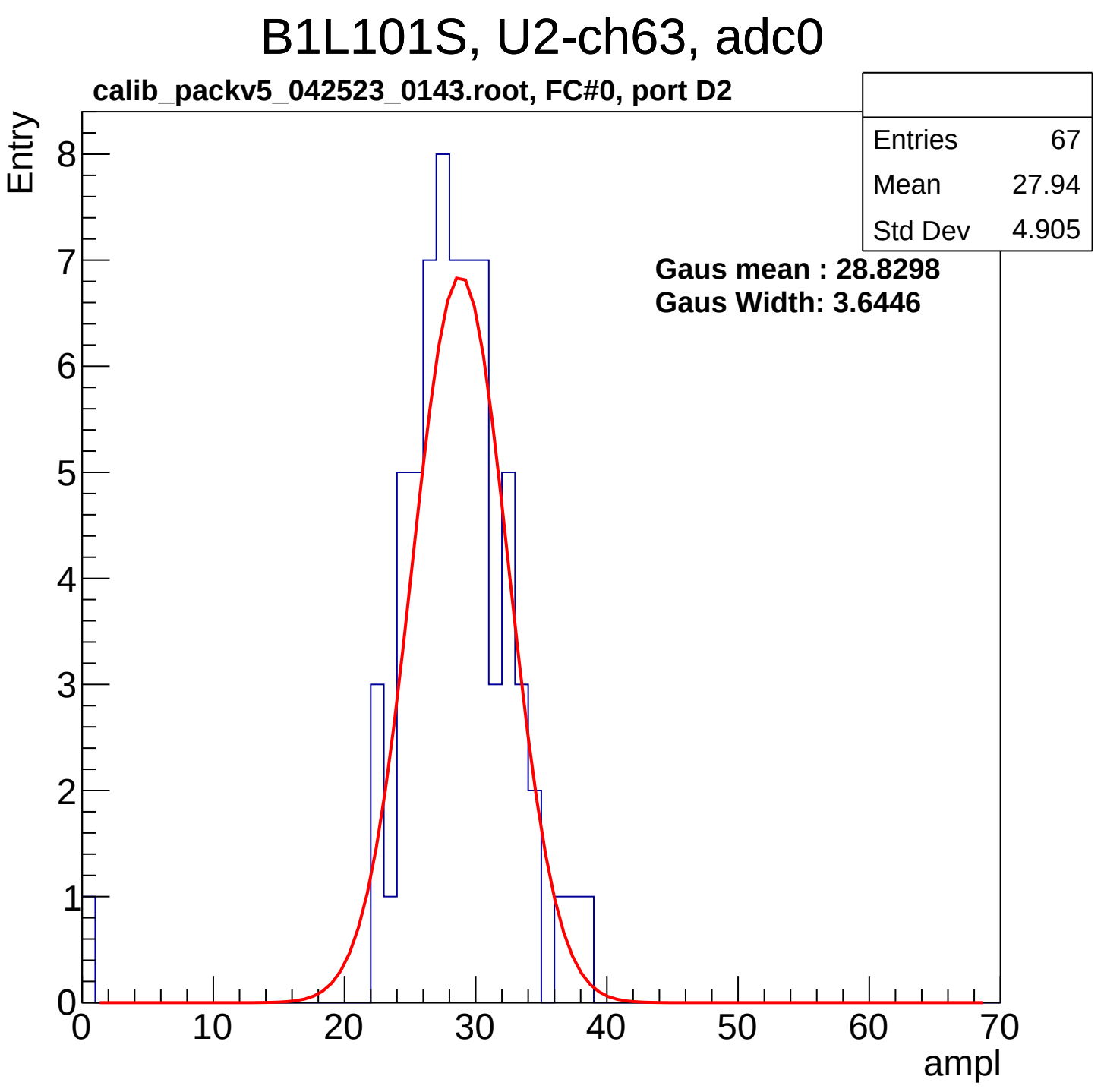

B1L101S, U2-ch62, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 47.9
Std Dev 3.74
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

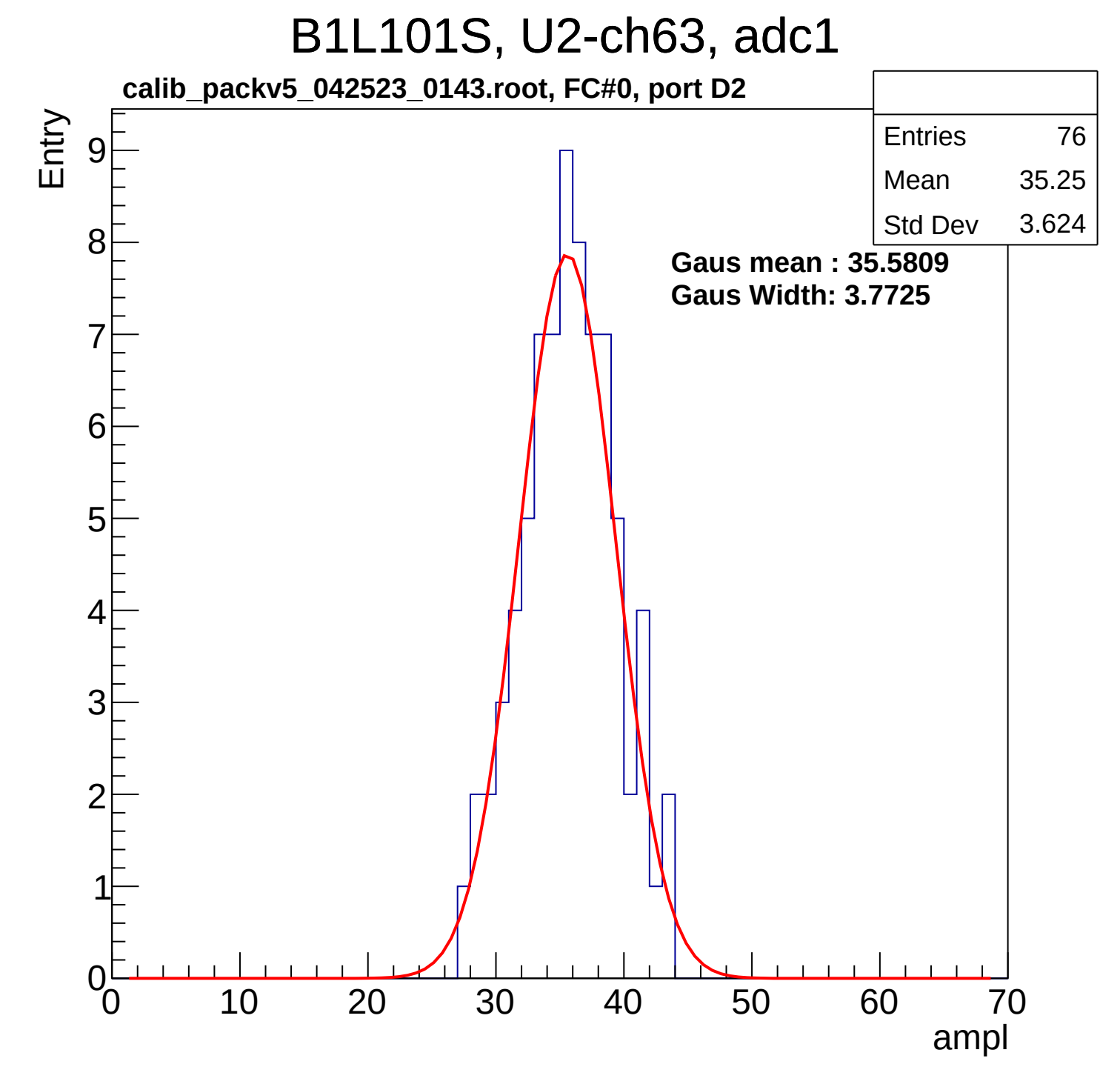

B1L101S, U2-ch62, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 54.38
Std Dev 3.455
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

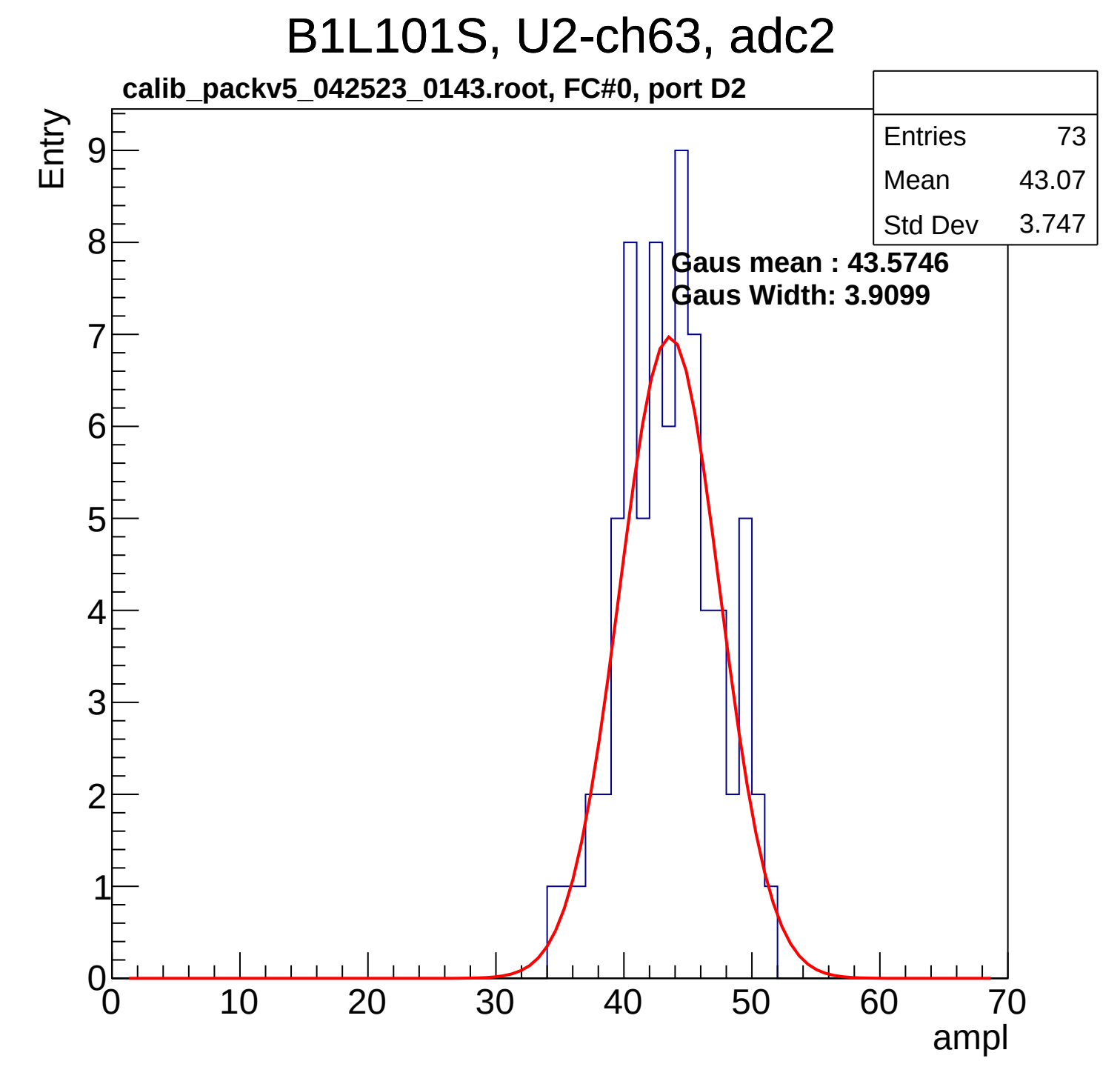

B1L101S, U2-ch62, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 58.83
Std Dev 2.785
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

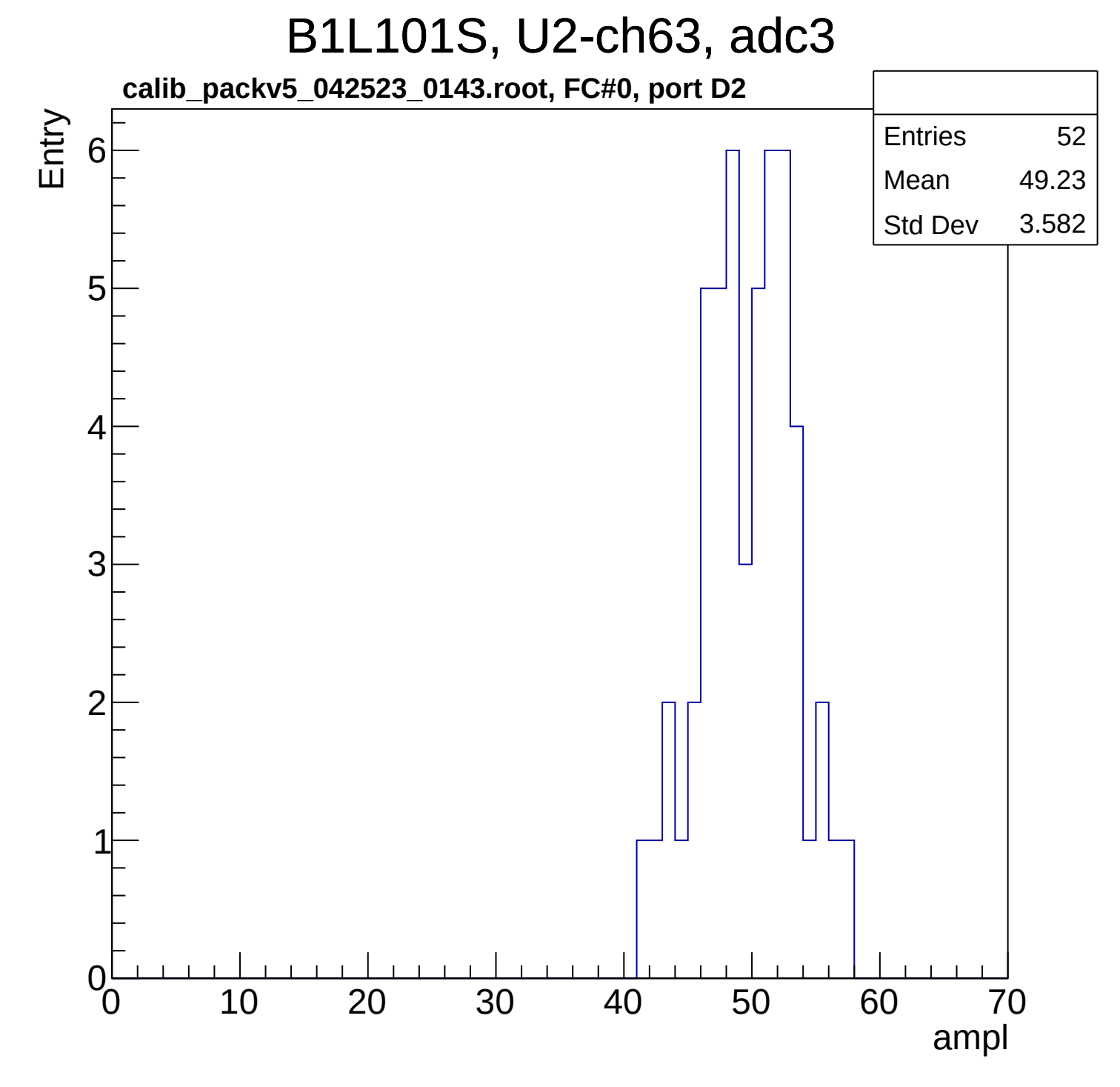

B1L101S, U2-ch62, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 21
Mean 58.33
Std Dev 13.16
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

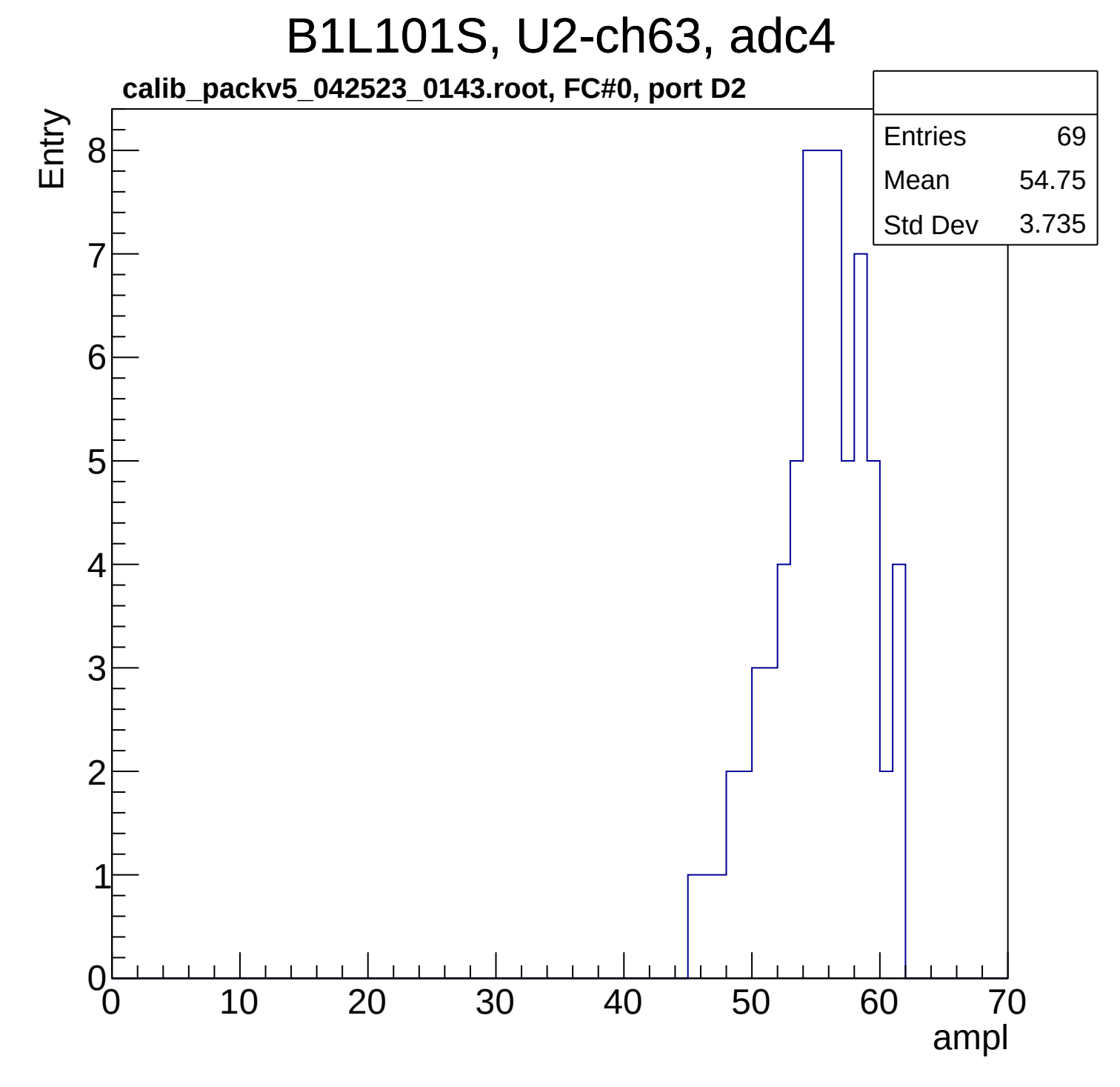

B1L101S, U2-ch62, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

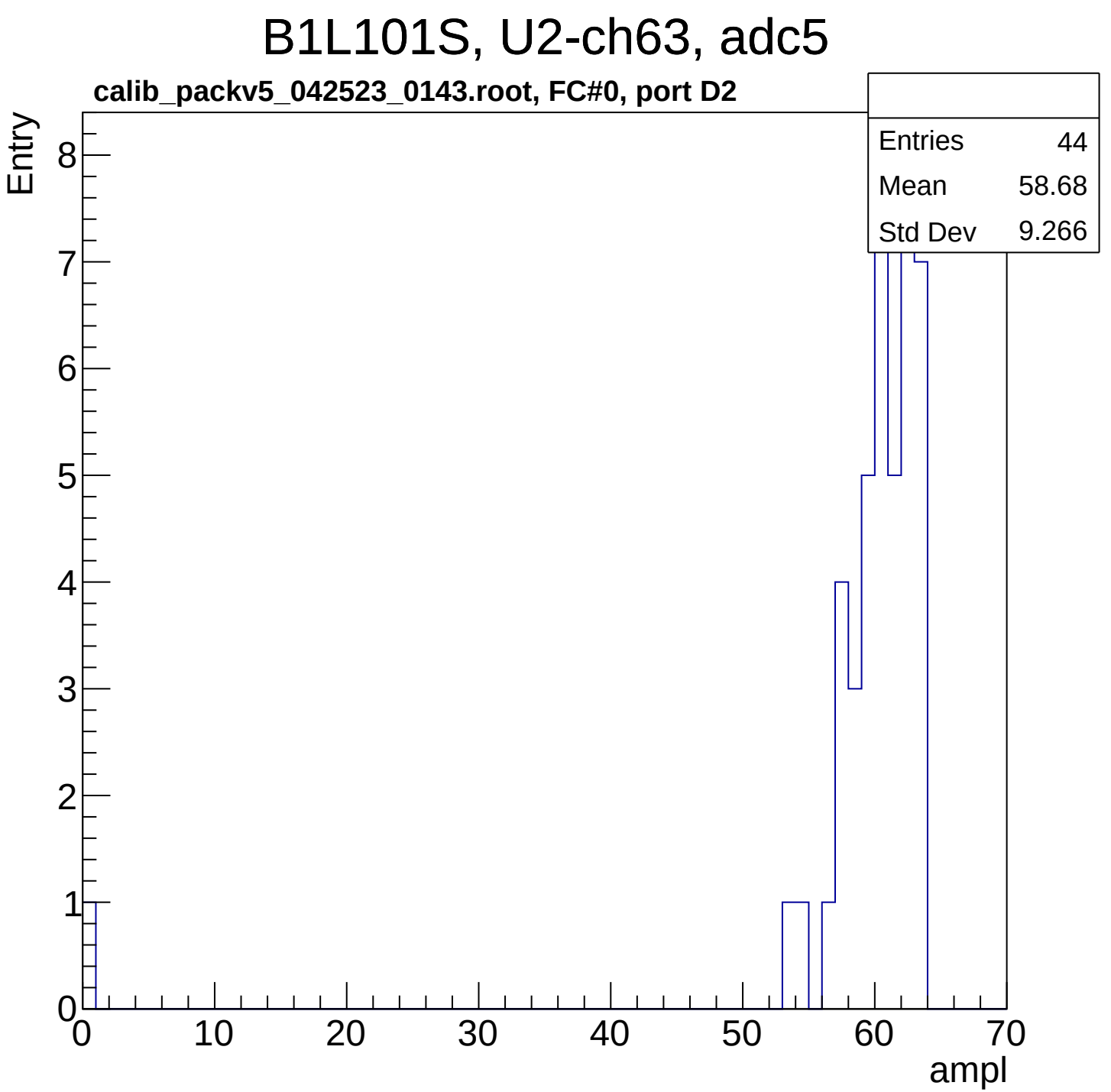

B1L101S, U2-ch63, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 27.94
Std Dev 4.905
Gaus mean : 28.8298
Gaus Width: 3.6446
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

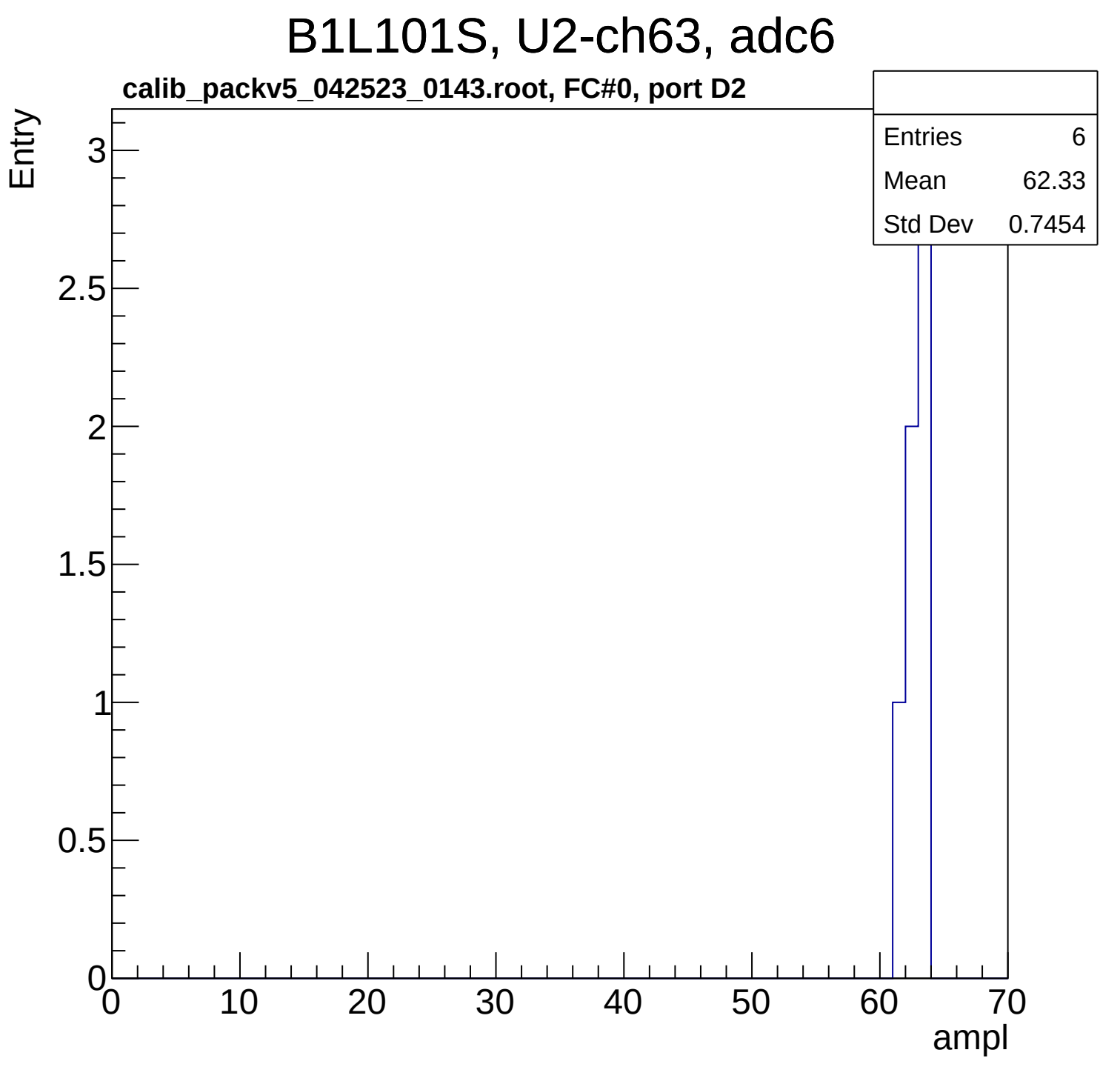

B1L101S, U2-ch63, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 35.25
Std Dev 3.624
Gaus mean : 35.5809
Gaus Width: 3.7725
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

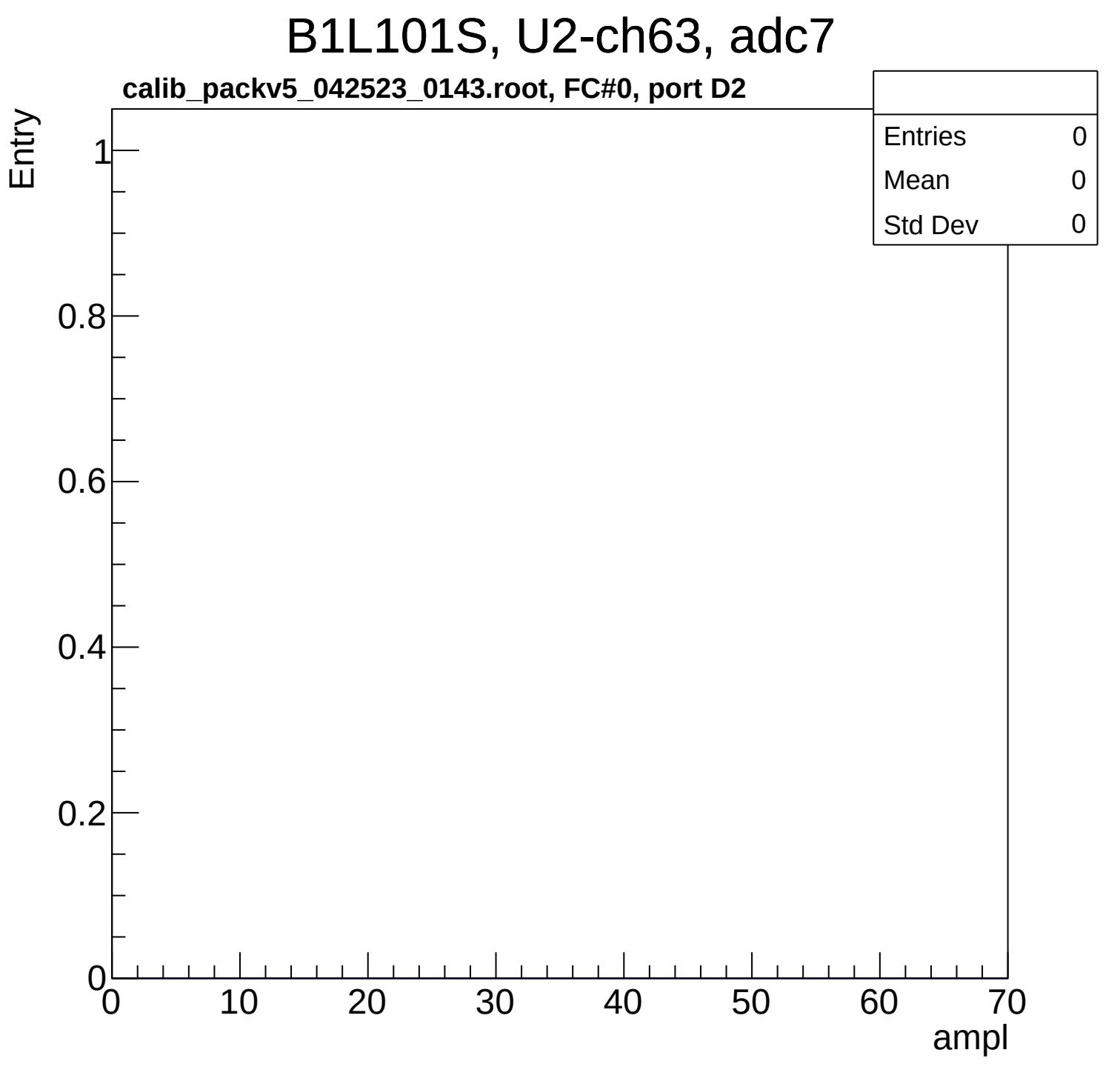

B1L101S, U2-ch63, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 43.07
Std Dev 3.747
Gaus mean : 43.5746
Gaus Width: 3.9099
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

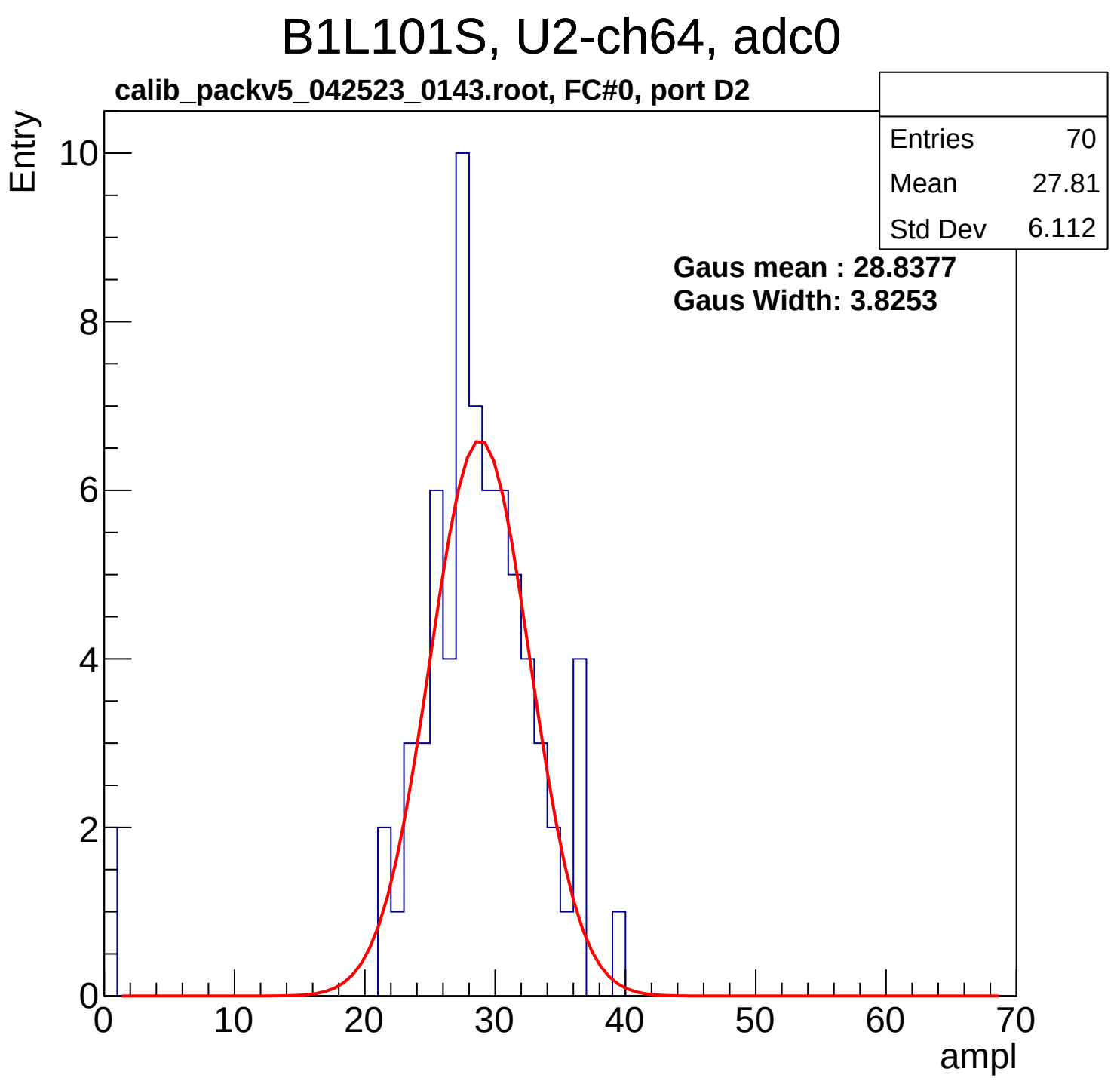

B1L101S, U2-ch63, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 49.23
Std Dev 3.582
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

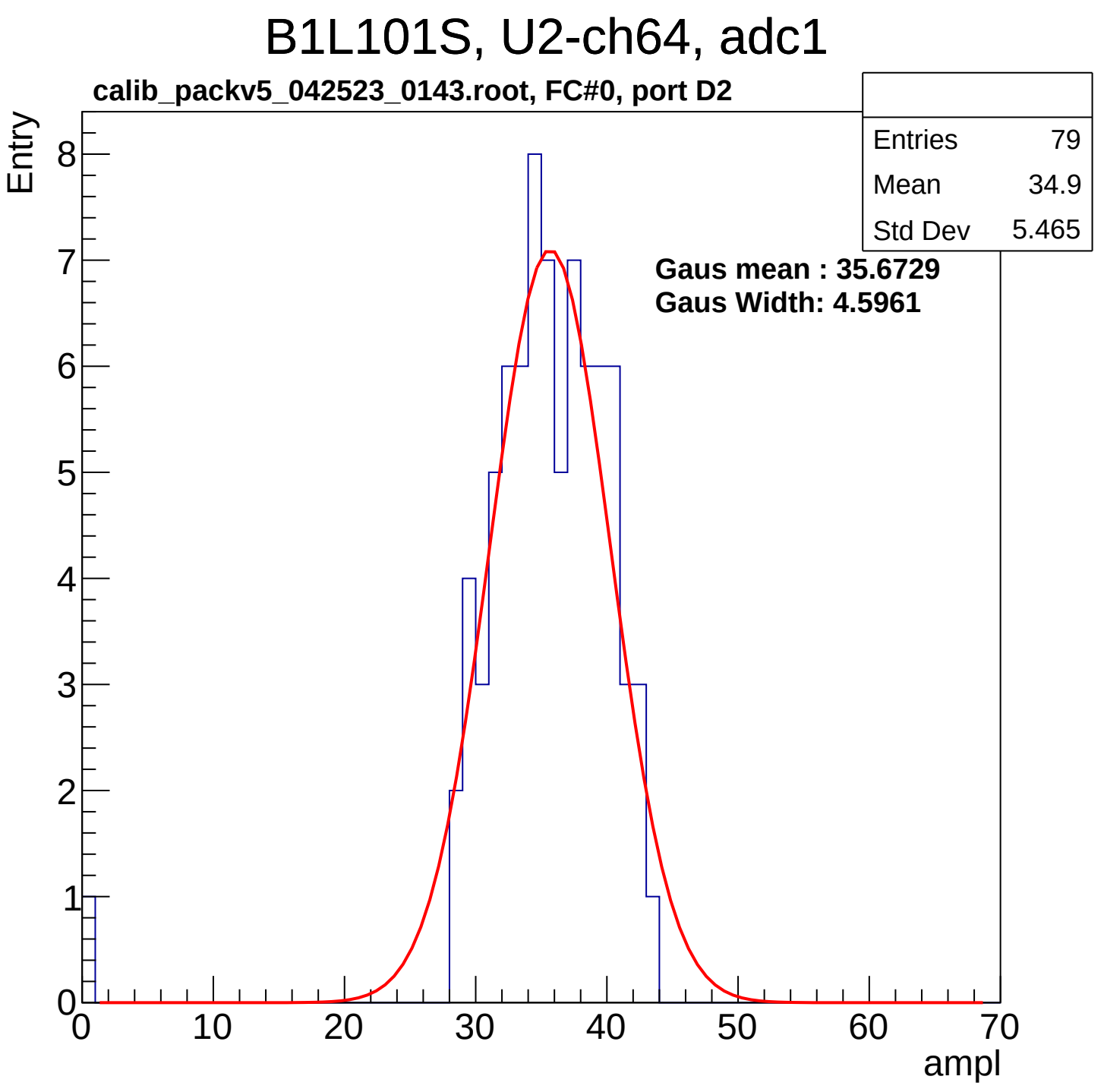

B1L101S, U2-ch63, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 54.75
Std Dev 3.735
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

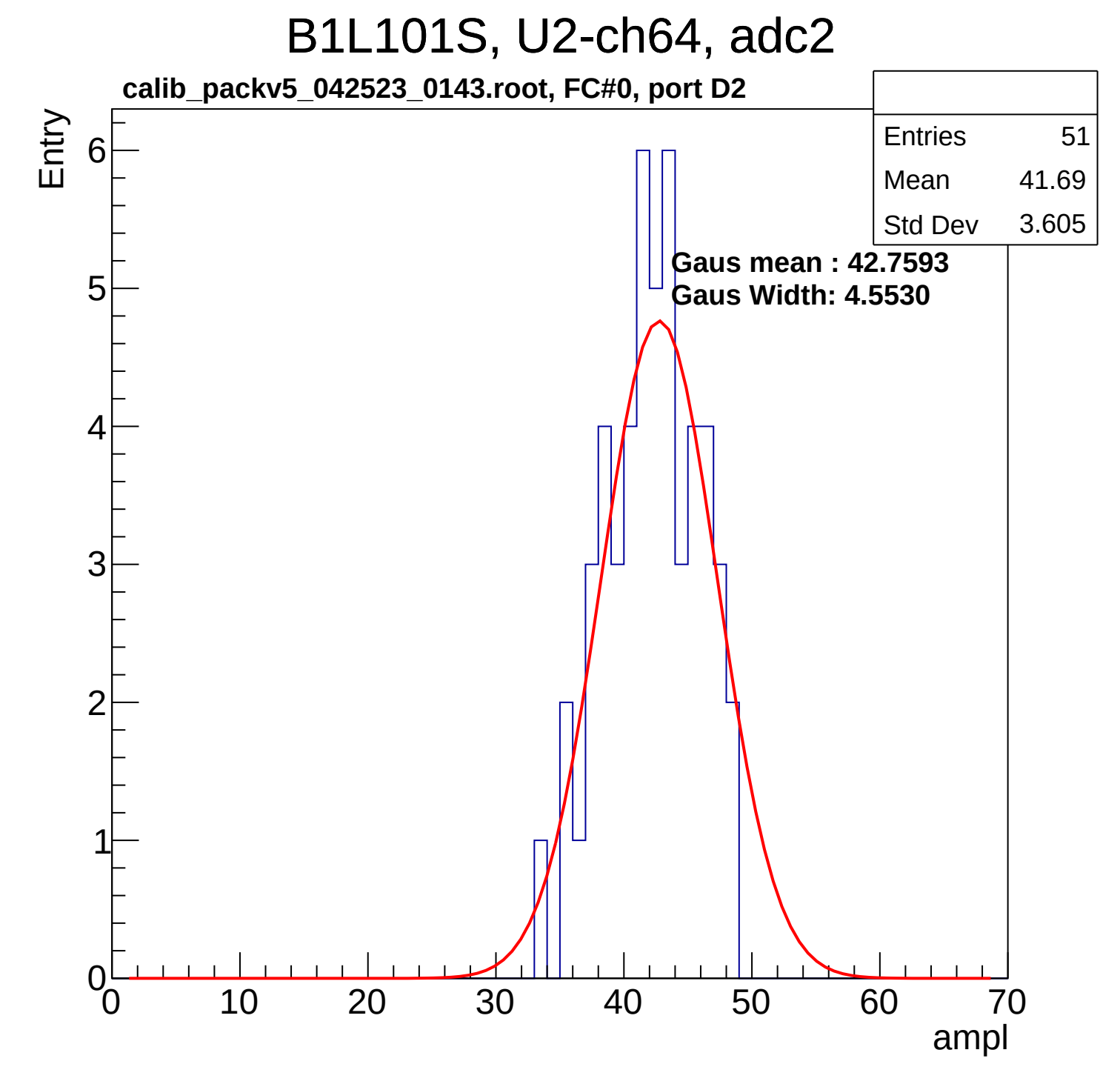

B1L101S, U2-ch63, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 44
Mean 58.68
Std Dev 9.266
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

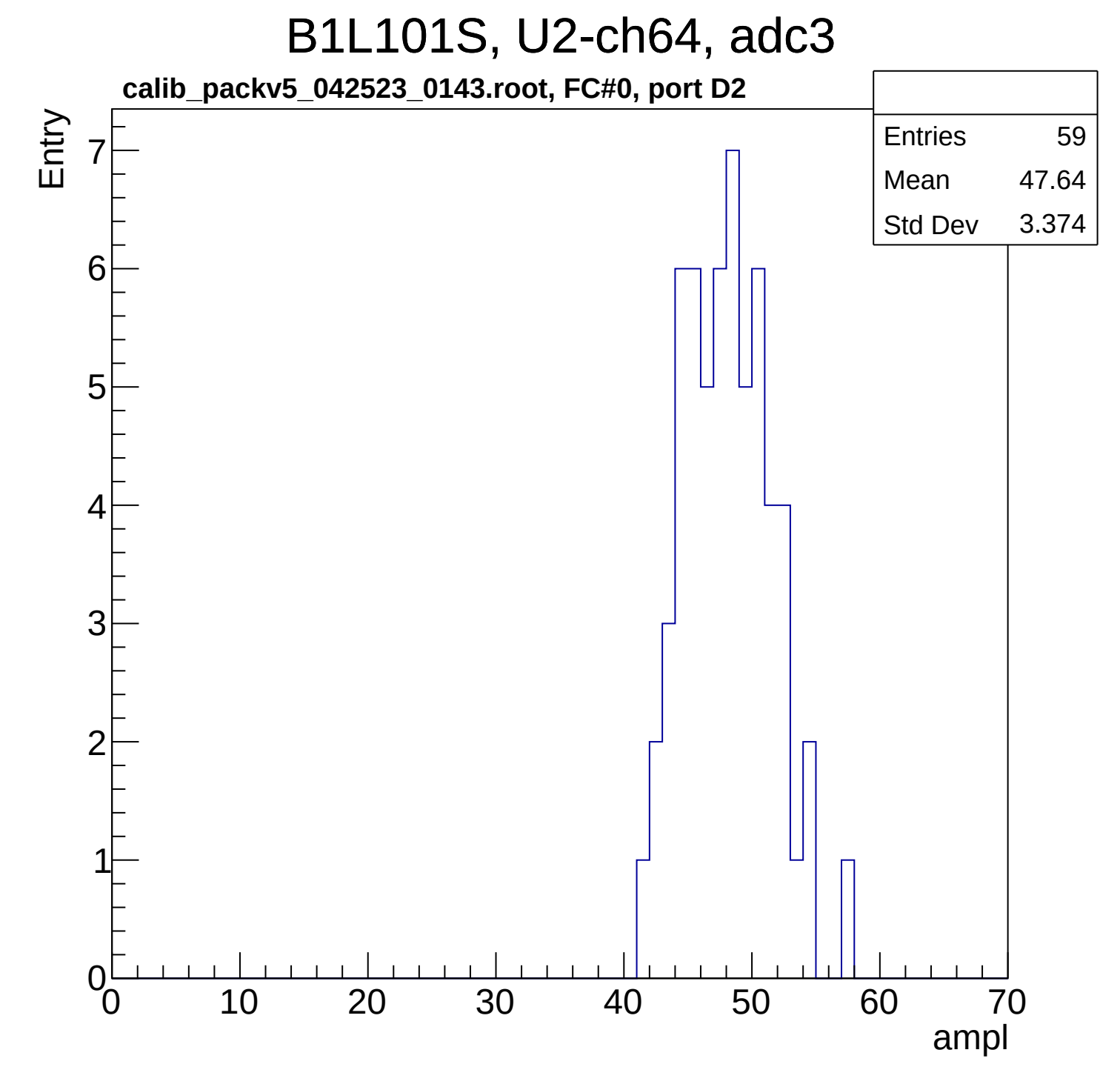

B1L101S, U2-ch63, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 62.33
Std Dev 0.7454
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

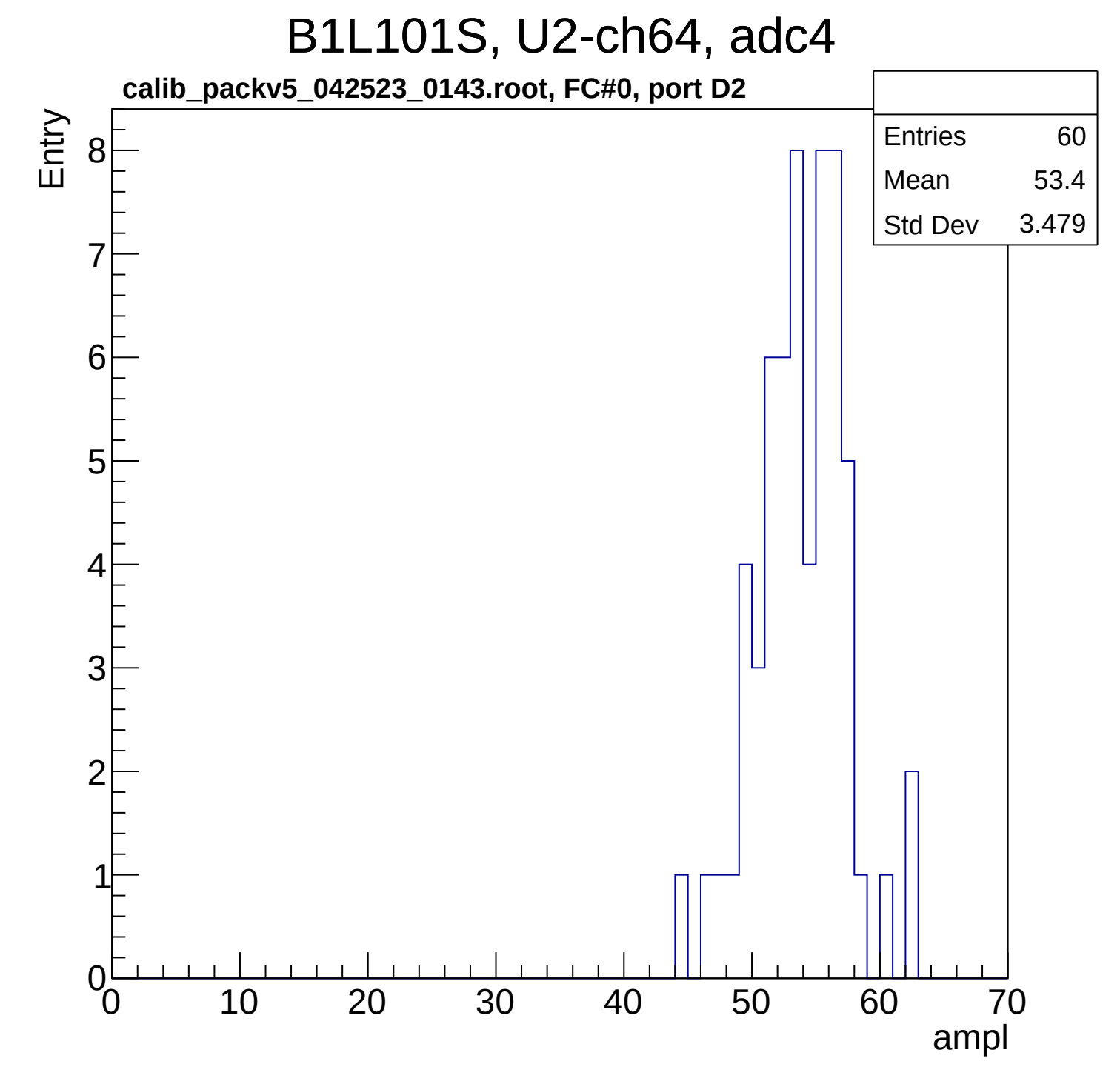

B1L101S, U2-ch63, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

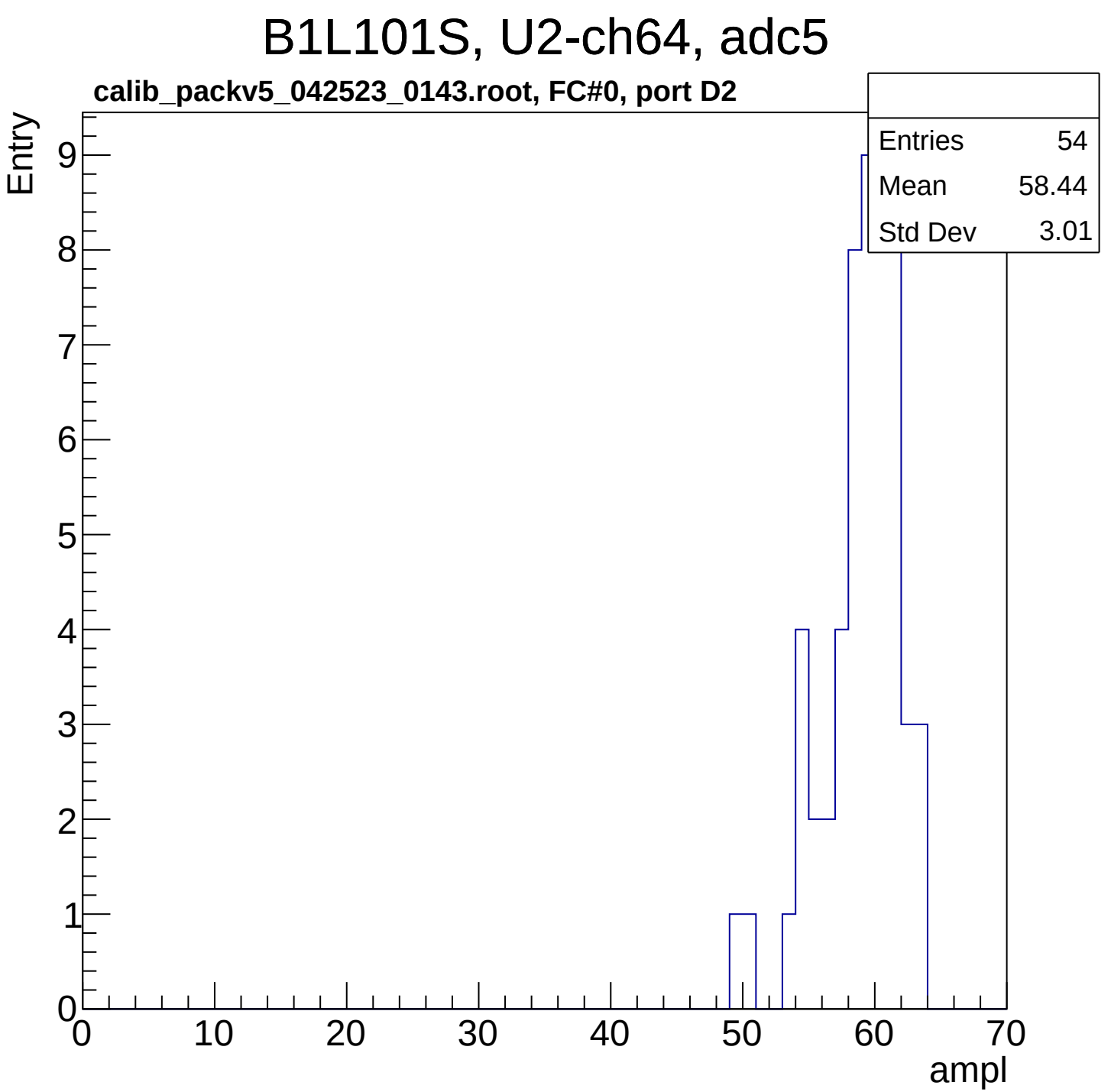

B1L101S, U2-ch64, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 27.81
Std Dev 6.112
Gaus mean : 28.8377
Gaus Width: 3.8253
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

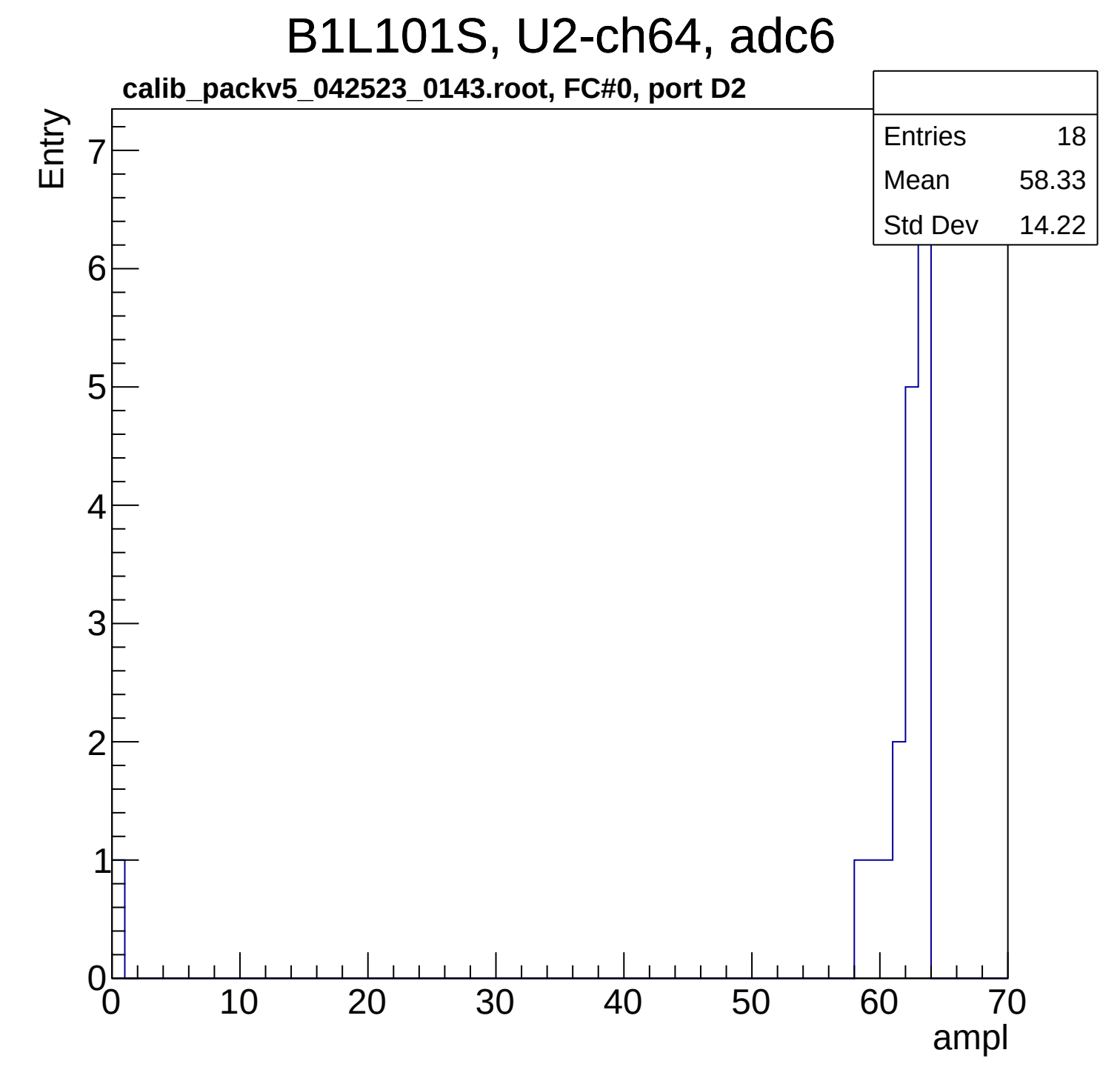

B1L101S, U2-ch64, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 34.9
Std Dev 5.465
Gaus mean : 35.6729
Gaus Width: 4.5961
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

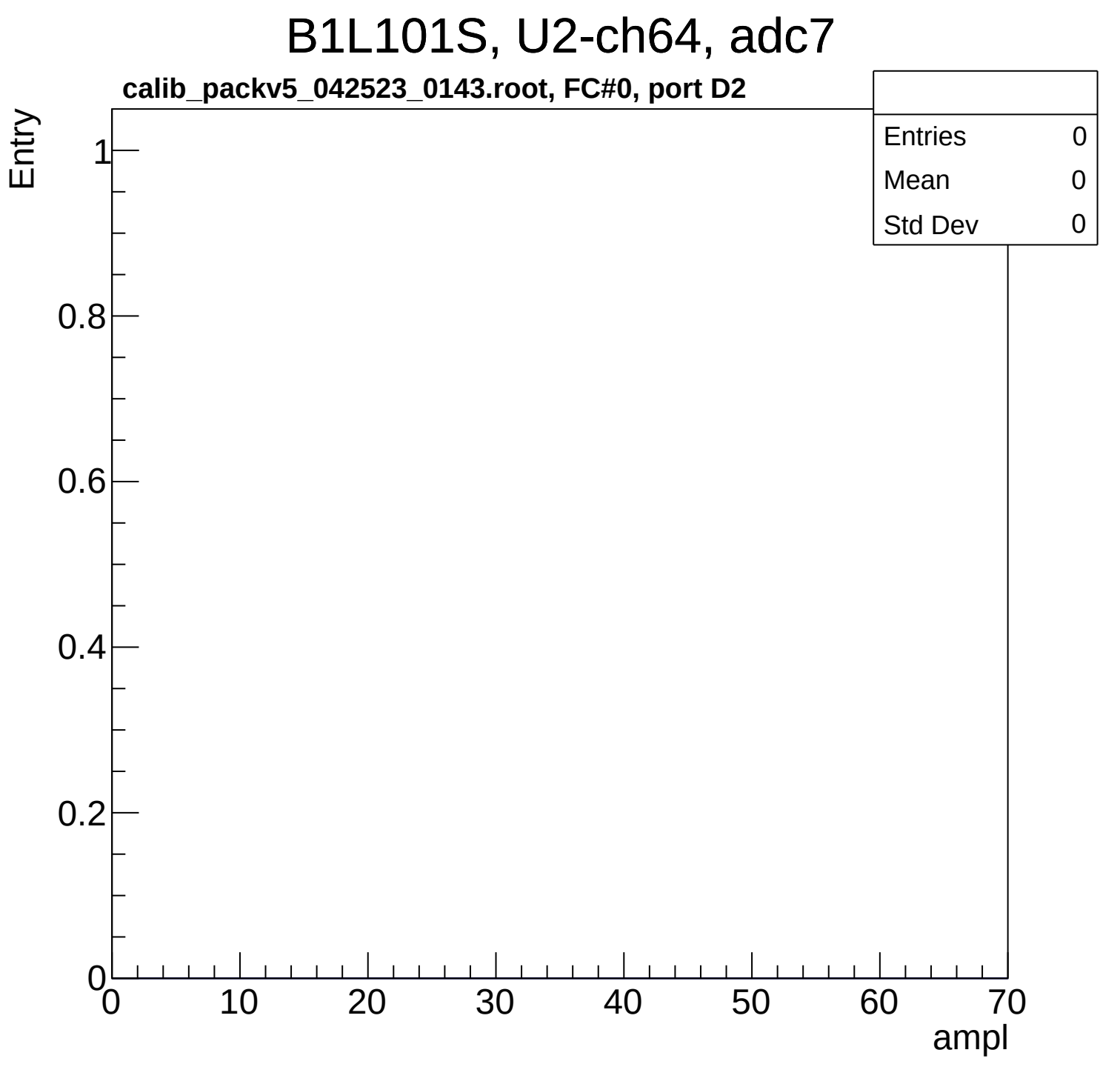

B1L101S, U2-ch64, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 41.69
Std Dev 3.605
Gaus mean : 42.7593
Gaus Width: 4.5530
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

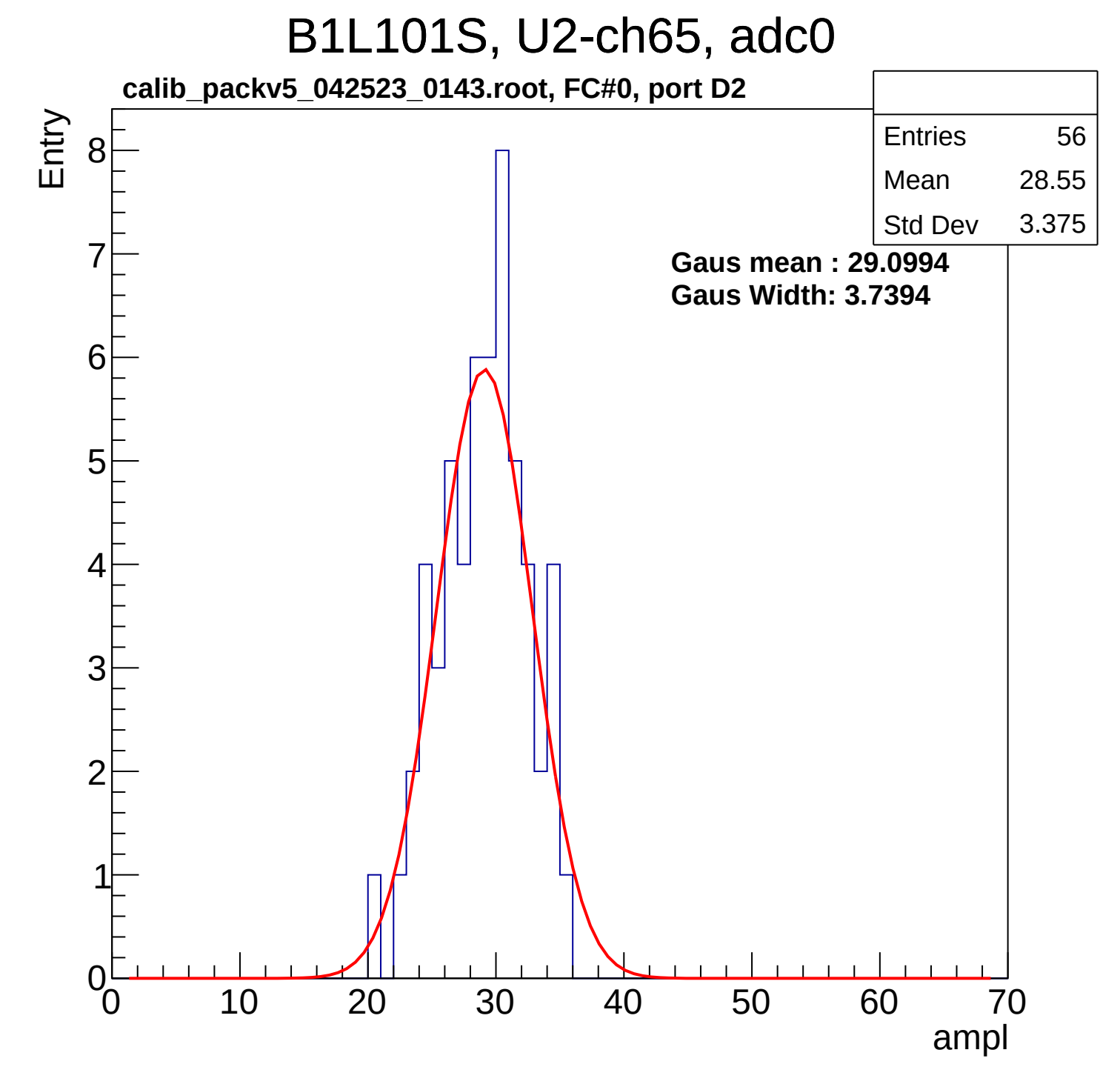

B1L101S, U2-ch64, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 47.64
Std Dev 3.374
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

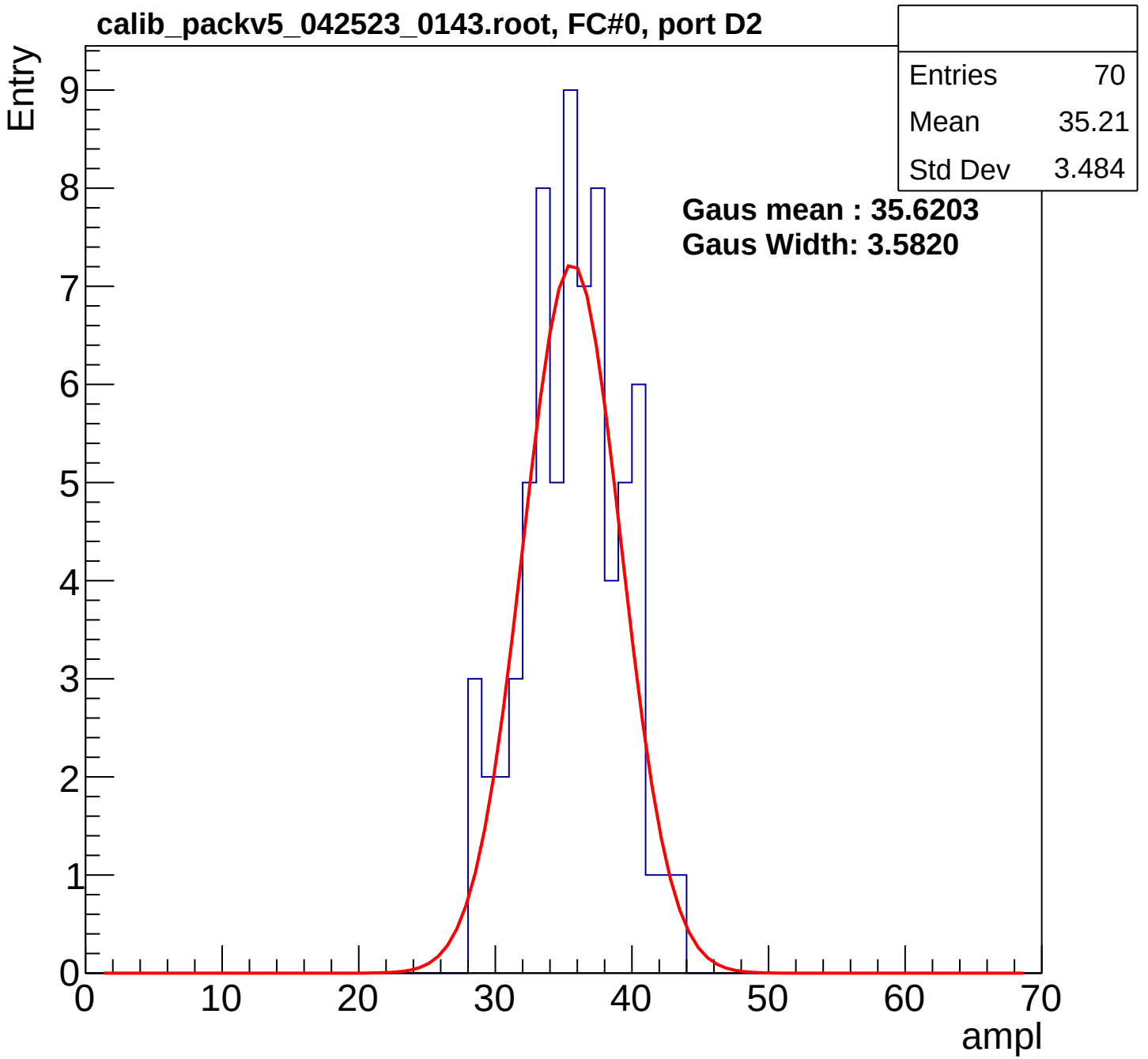

B1L101S, U2-ch64, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 53.4
Std Dev 3.479
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

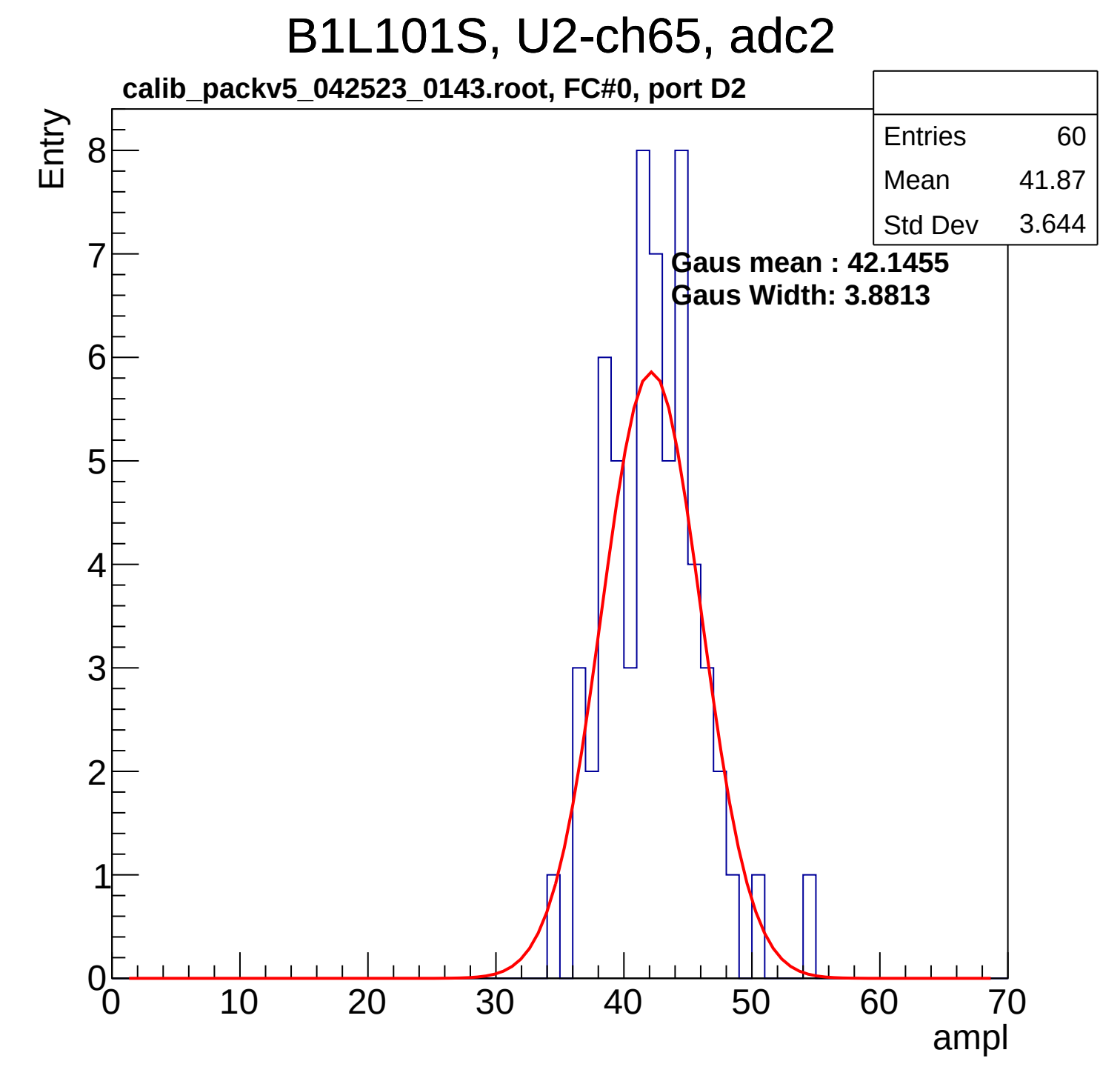

B1L101S, U2-ch64, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 58.44
Std Dev 3.01
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

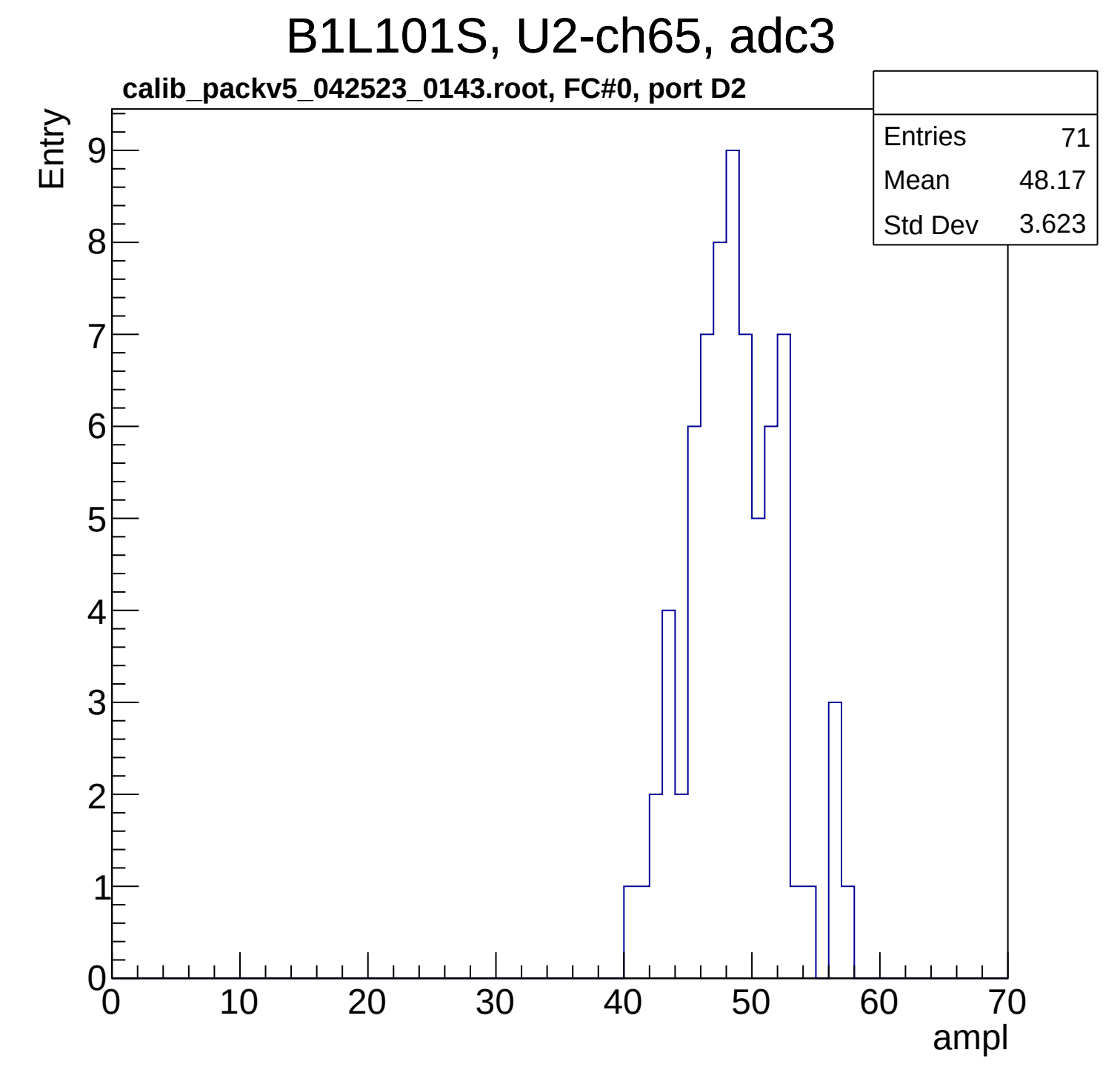

B1L101S, U2-ch64, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 18
Mean 58.33
Std Dev 14.22
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

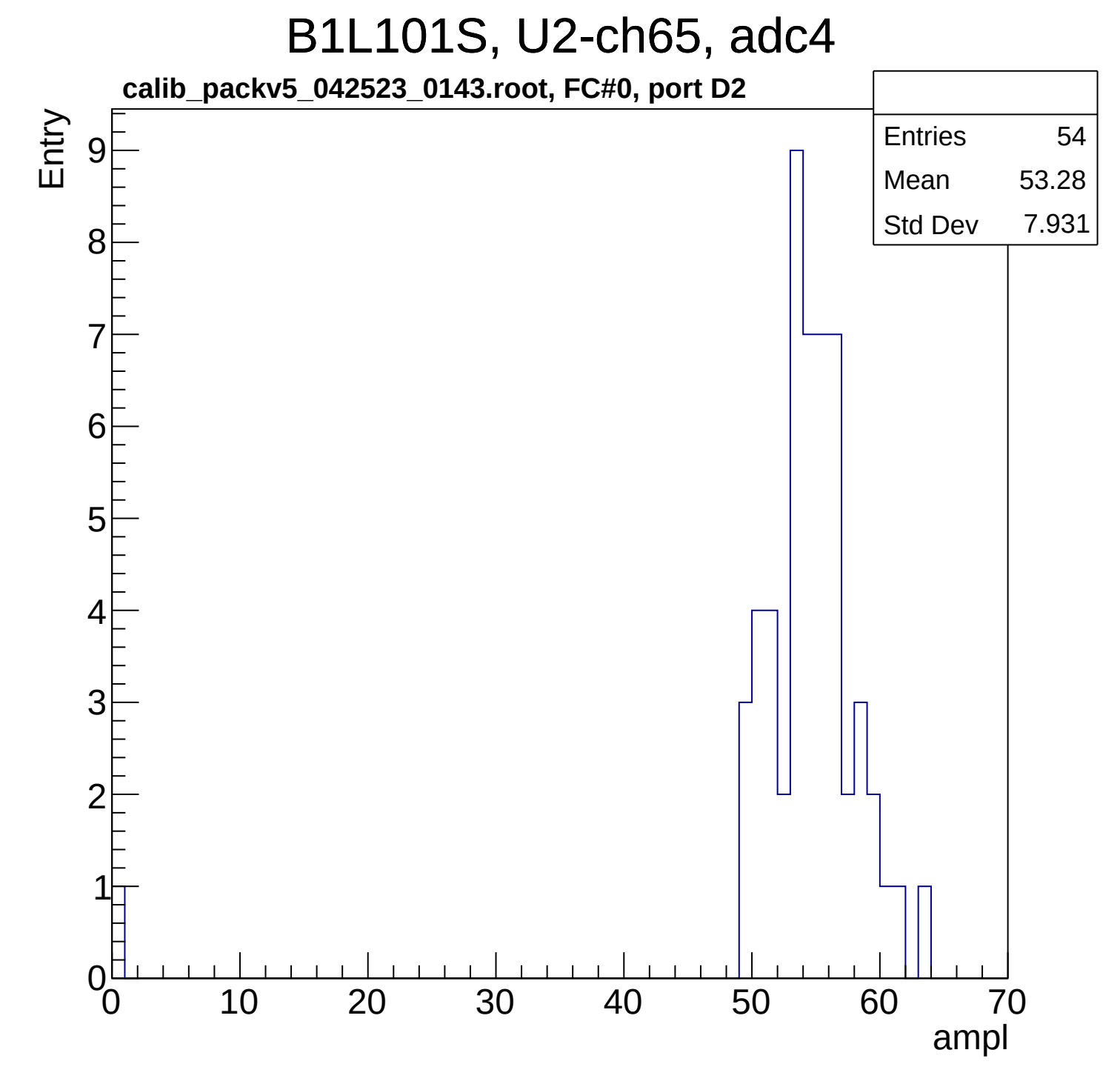

B1L101S, U2-ch64, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

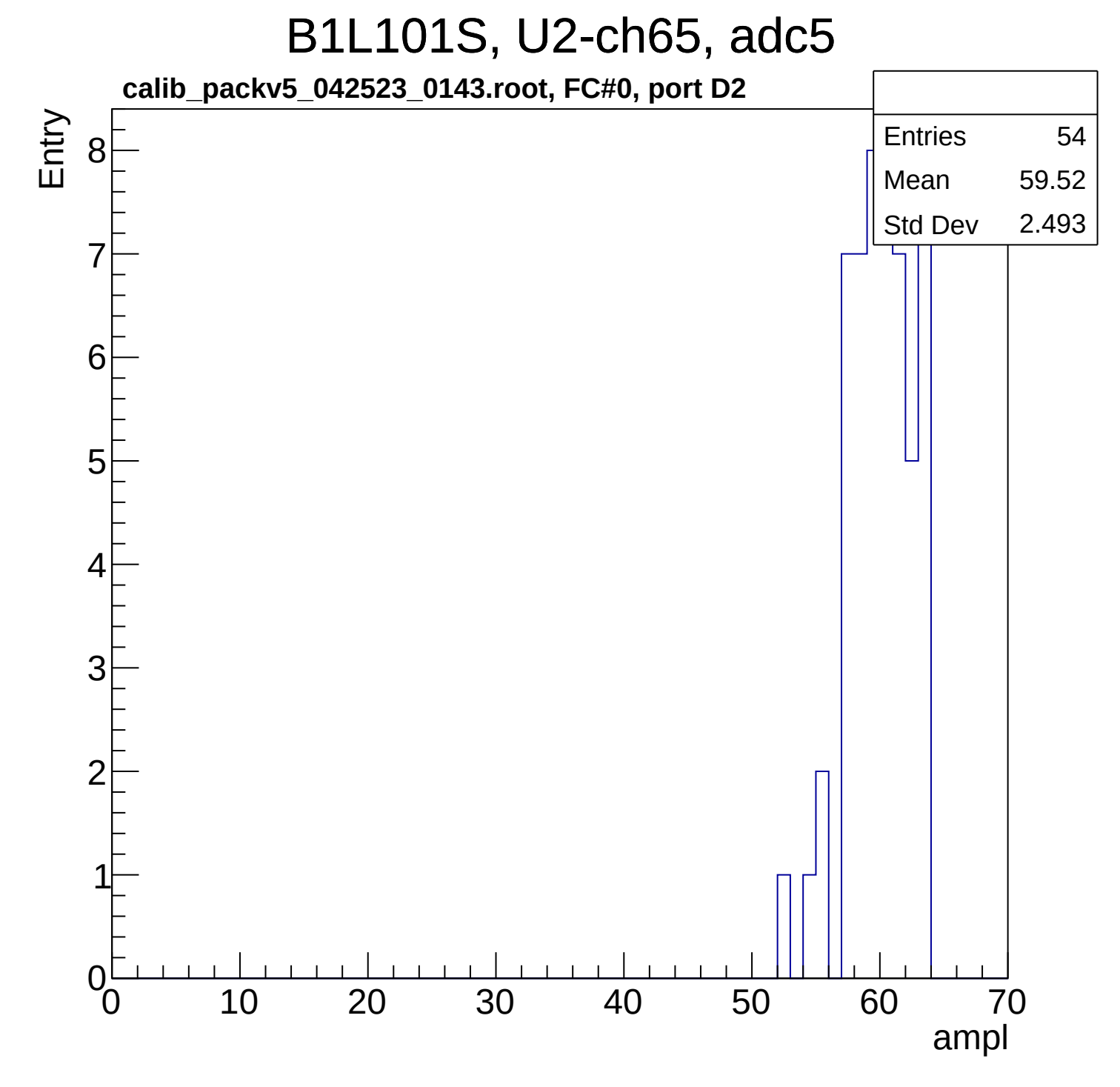

B1L101S, U2-ch65, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 28.55
Std Dev 3.375
Gaus mean : 29.0994
Gaus Width: 3.7394
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

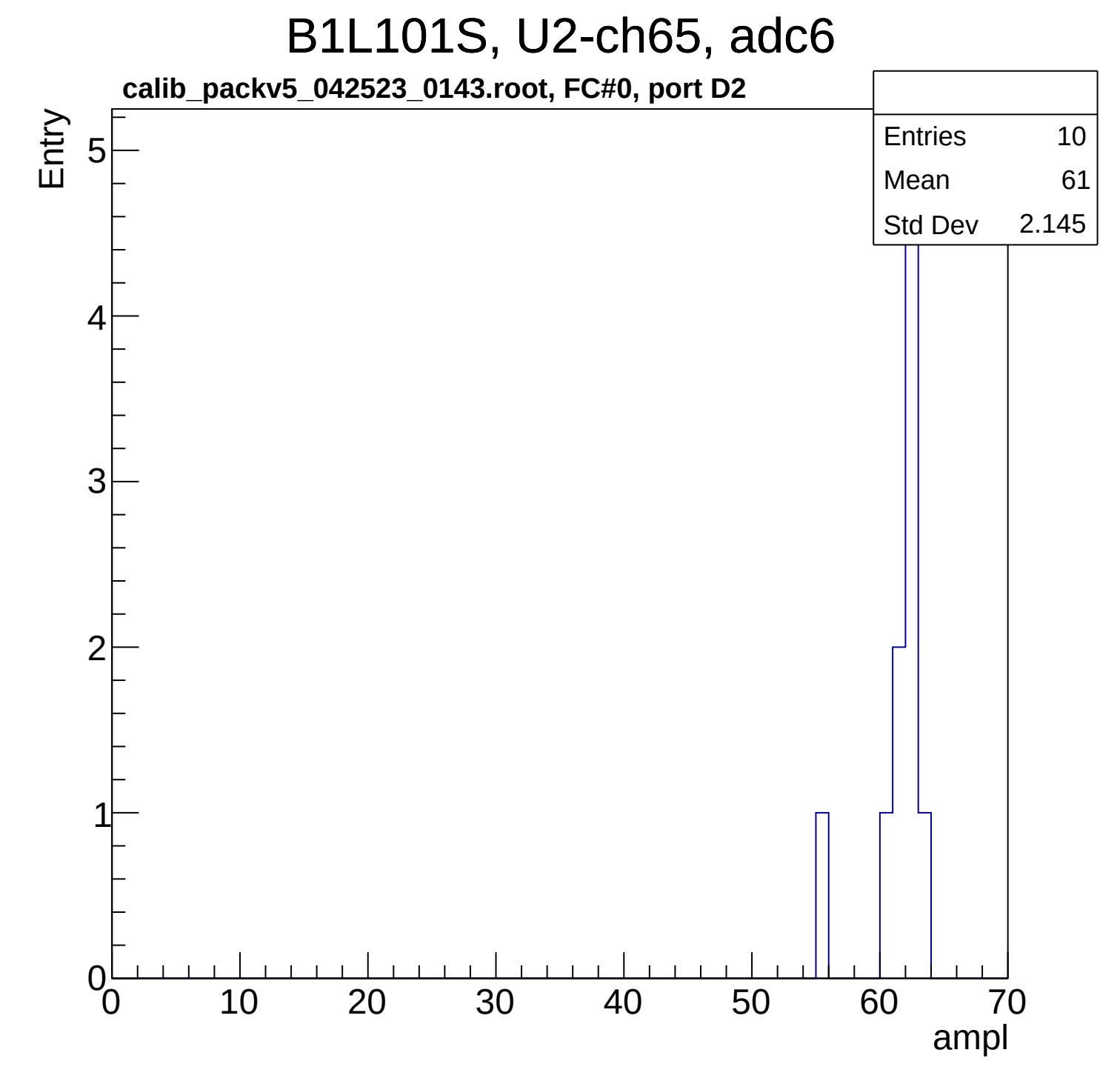

B1L101S, U2-ch65, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 35.21
Std Dev 3.484
Gaus mean : 35.6203
Gaus Width: 3.5820
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

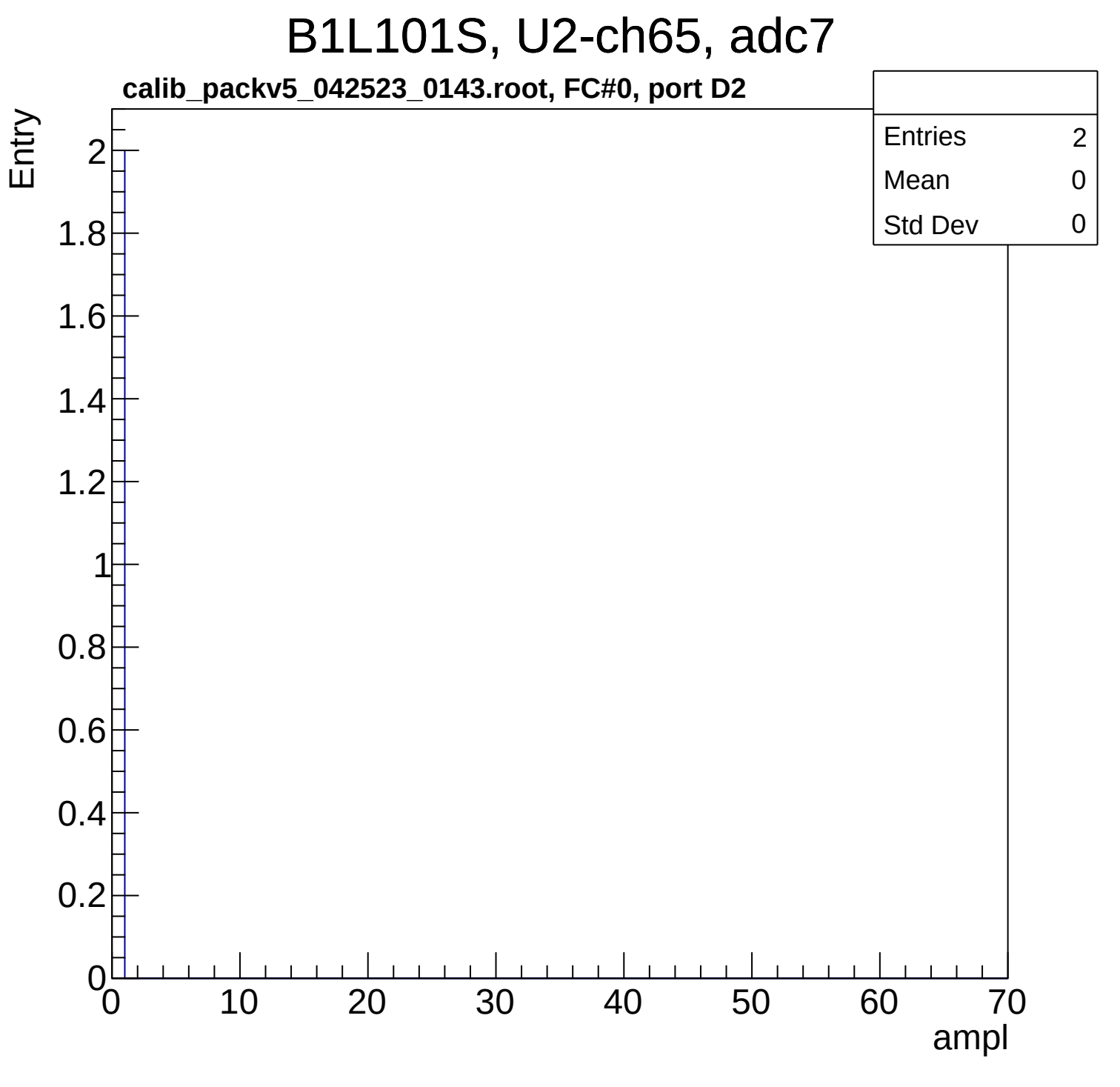

B1L101S, U2-ch65, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 41.87
Std Dev 3.644
Gaus mean : 42.1455
Gaus Width: 3.8813
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

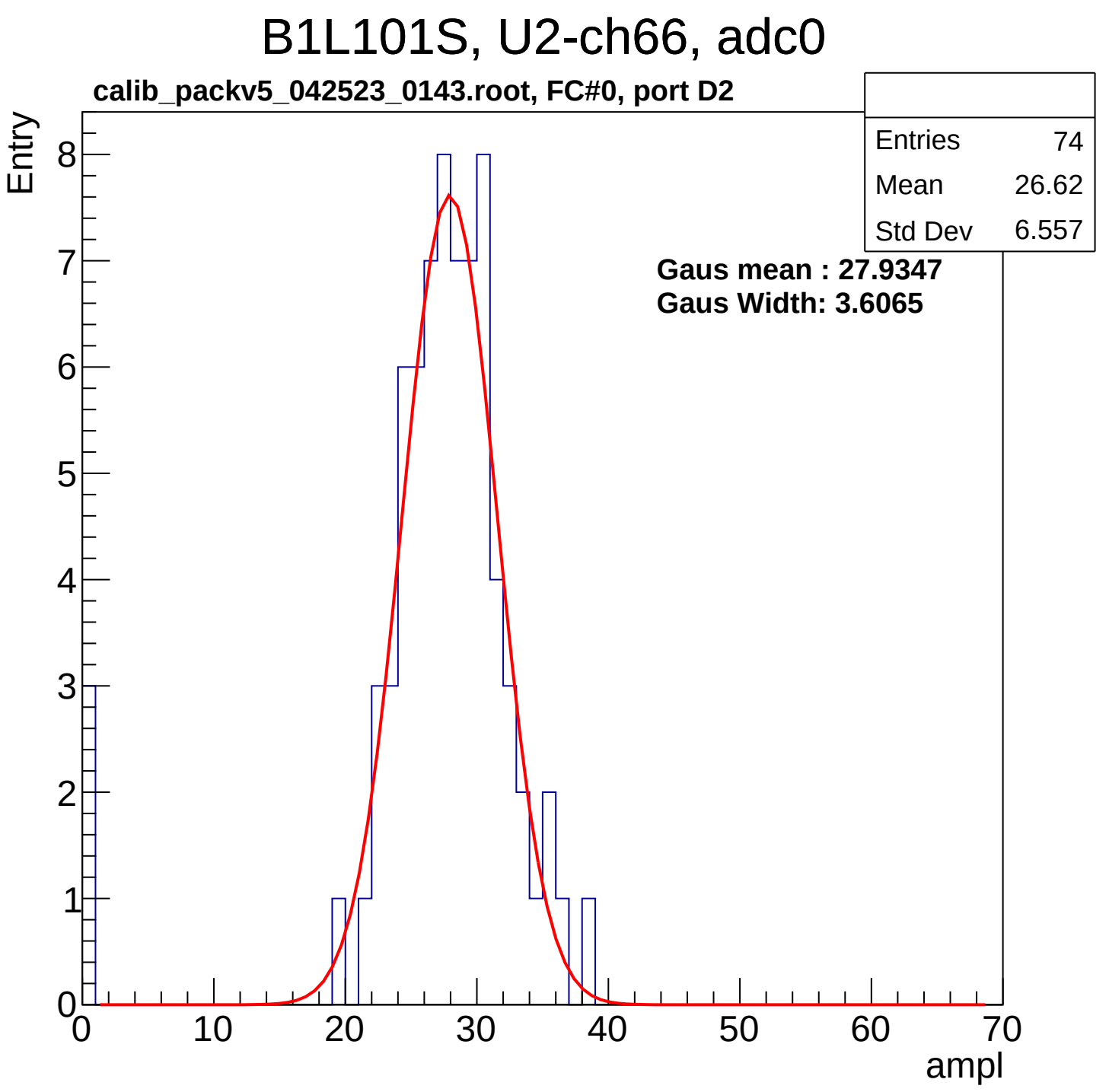

B1L101S, U2-ch65, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 48.17
Std Dev 3.623
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

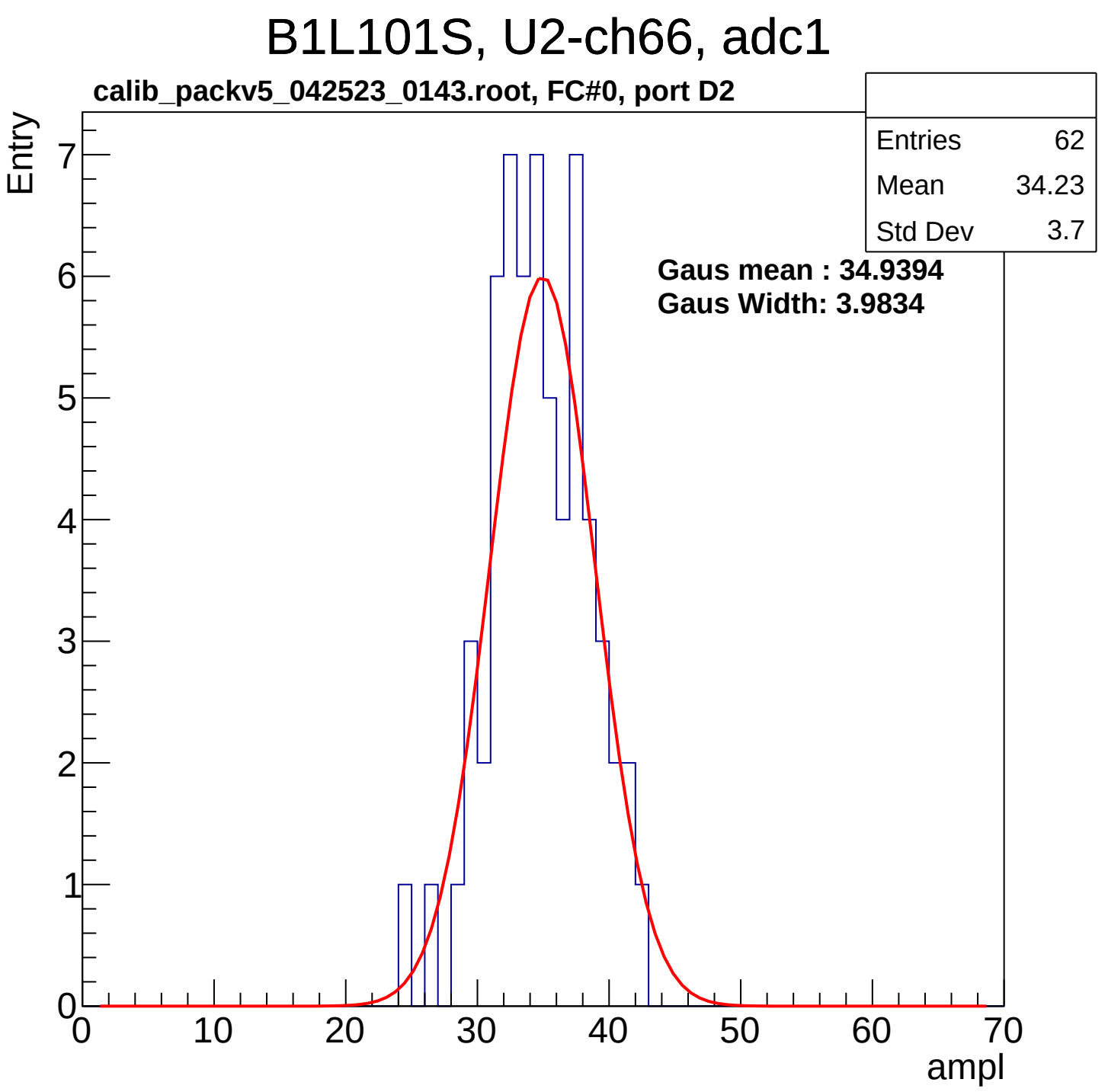

B1L101S, U2-ch65, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 53.28
Std Dev 7.931
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

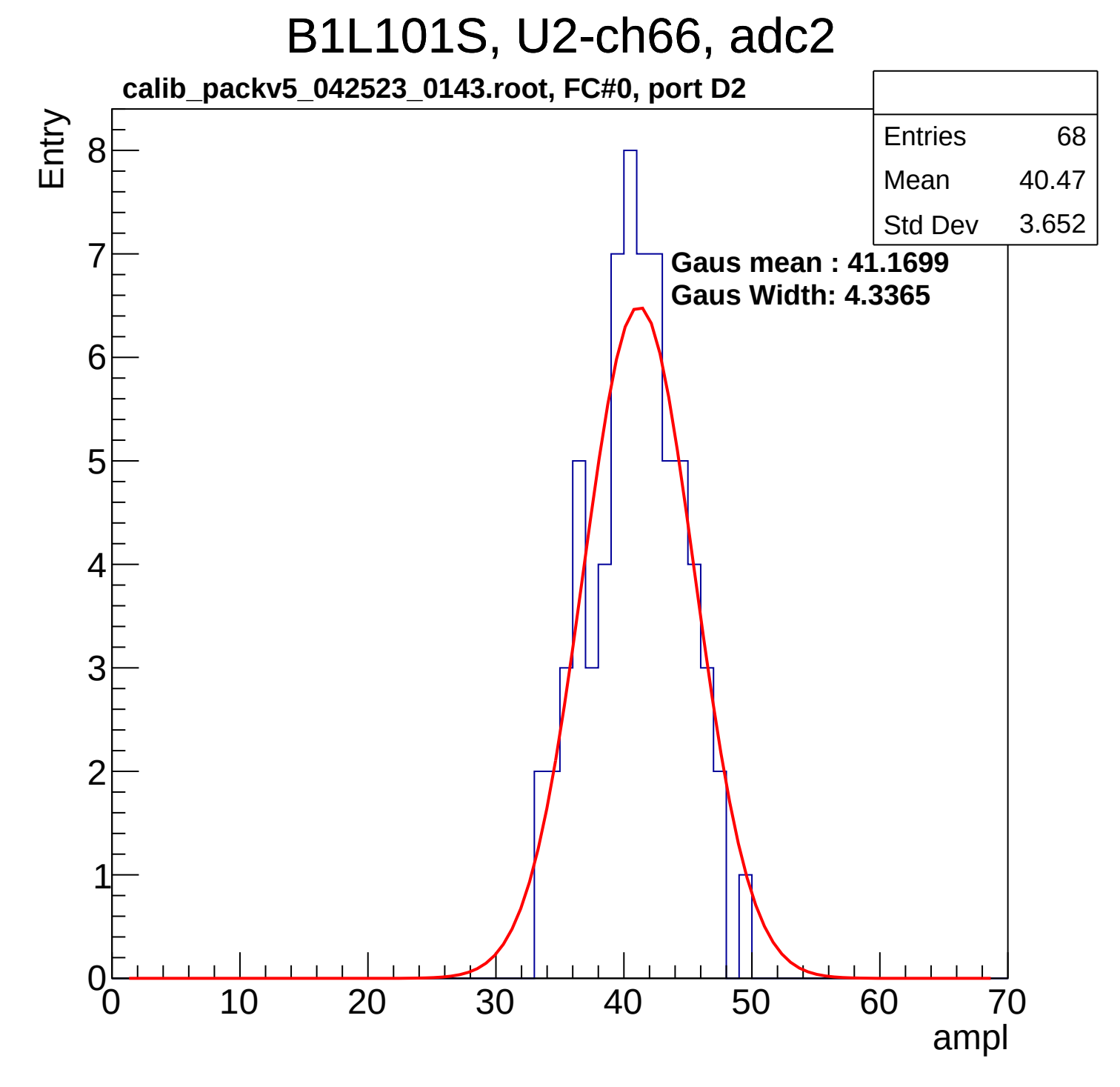

B1L101S, U2-ch65, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 59.52
Std Dev 2.493
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

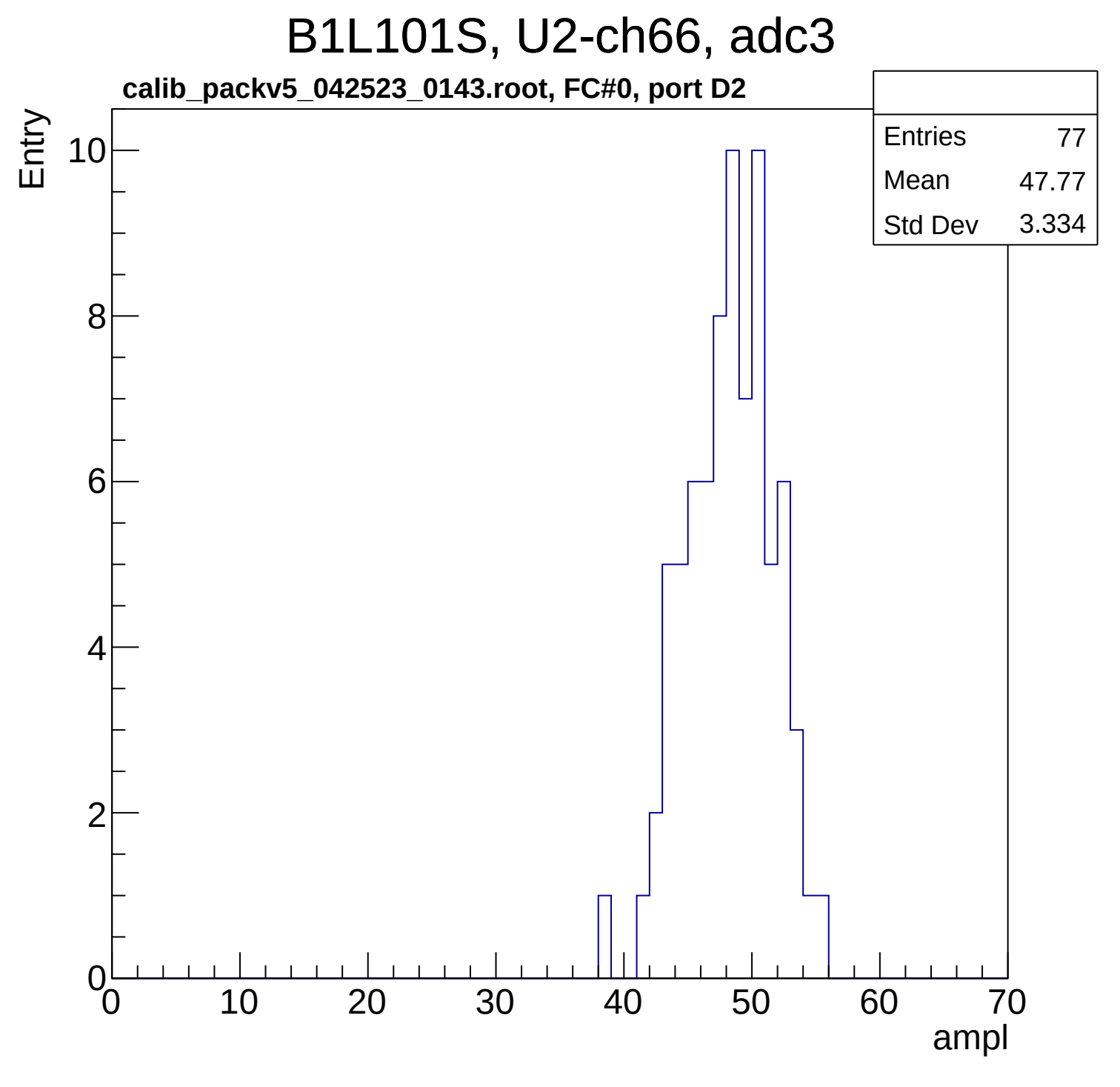

B1L101S, U2-ch65, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 61
Std Dev 2.145
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

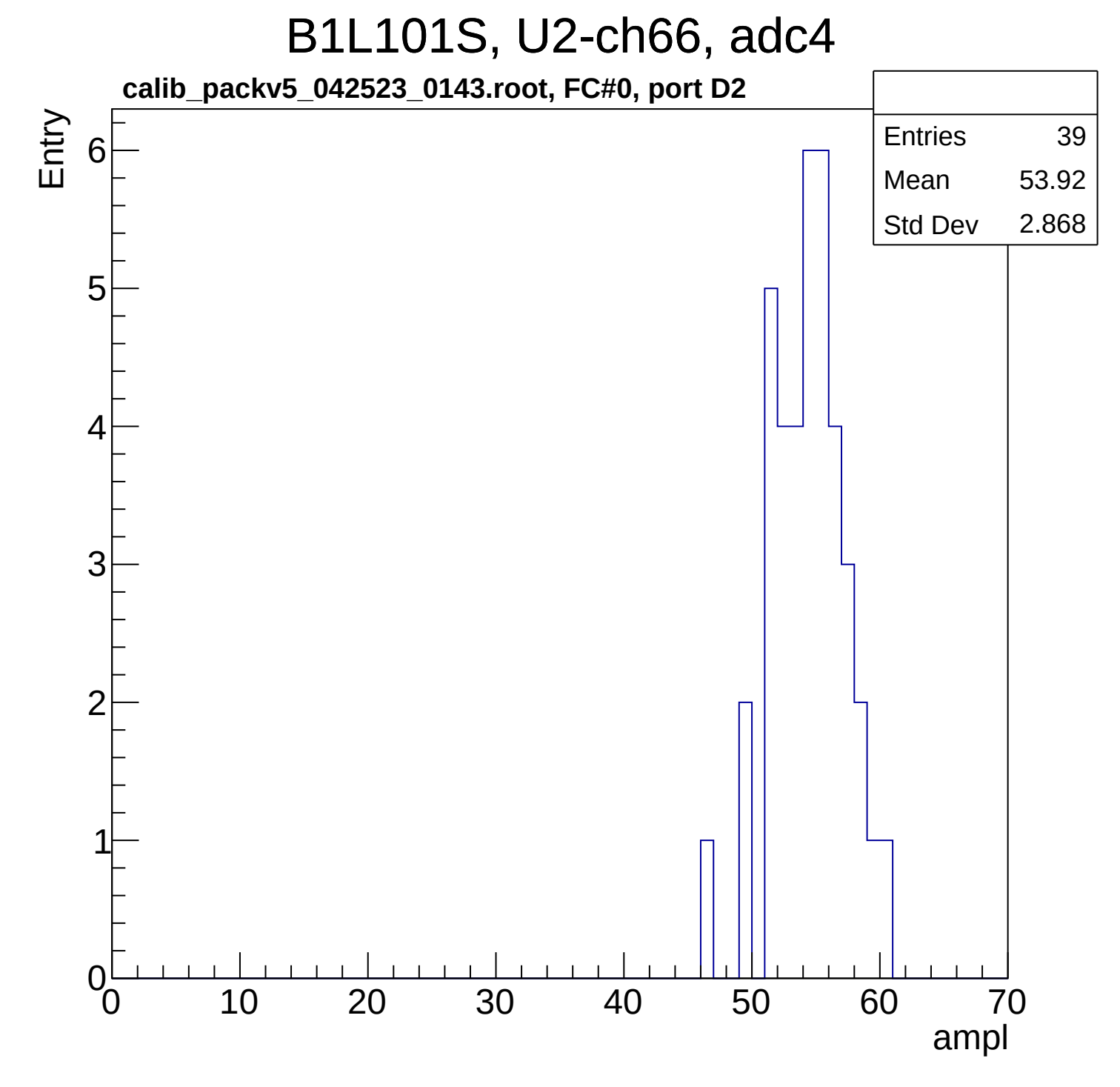

B1L101S, U2-ch65, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

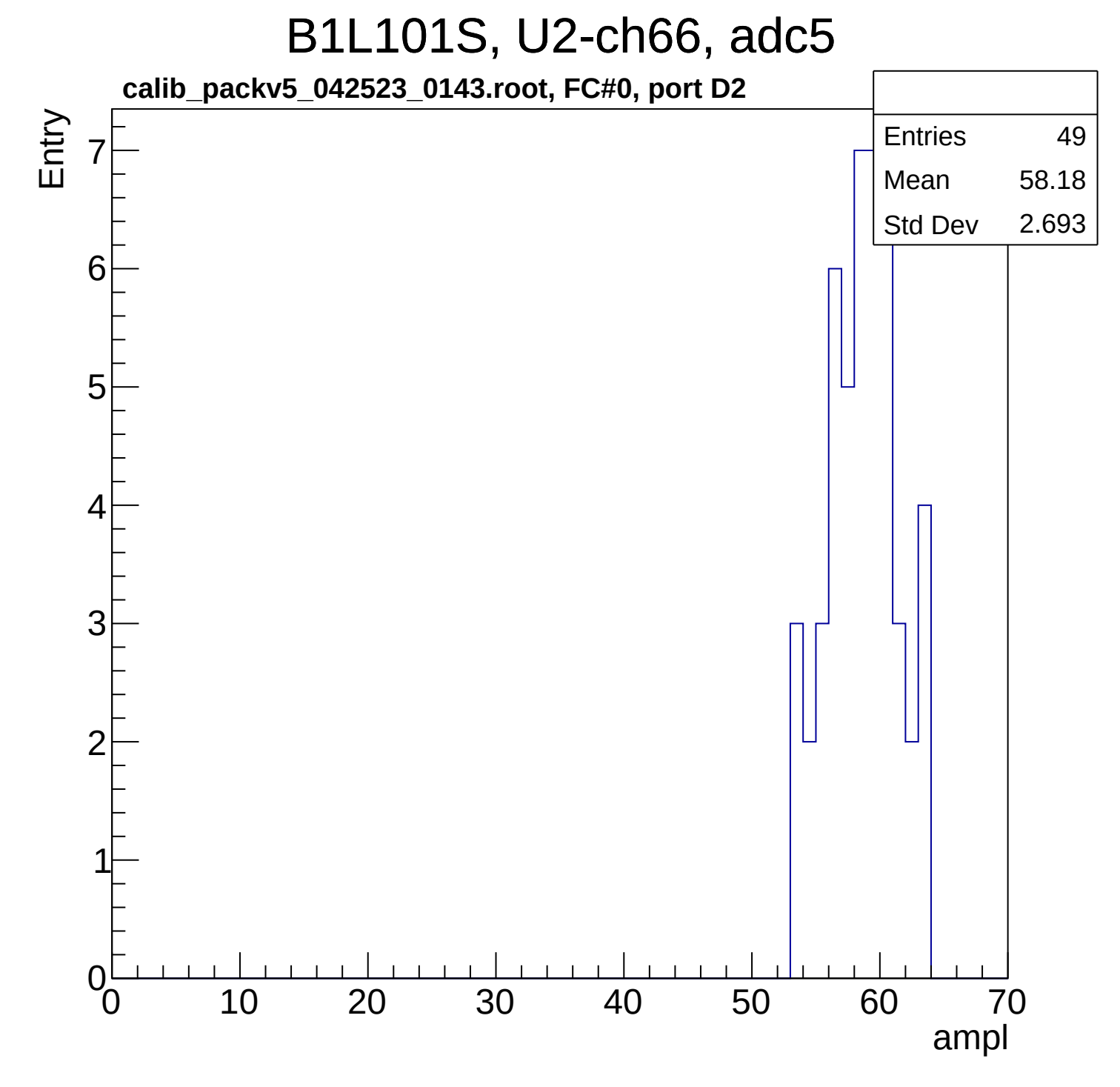

B1L101S, U2-ch66, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 26.62
Std Dev 6.557
Gaus mean : 27.9347
Gaus Width: 3.6065
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

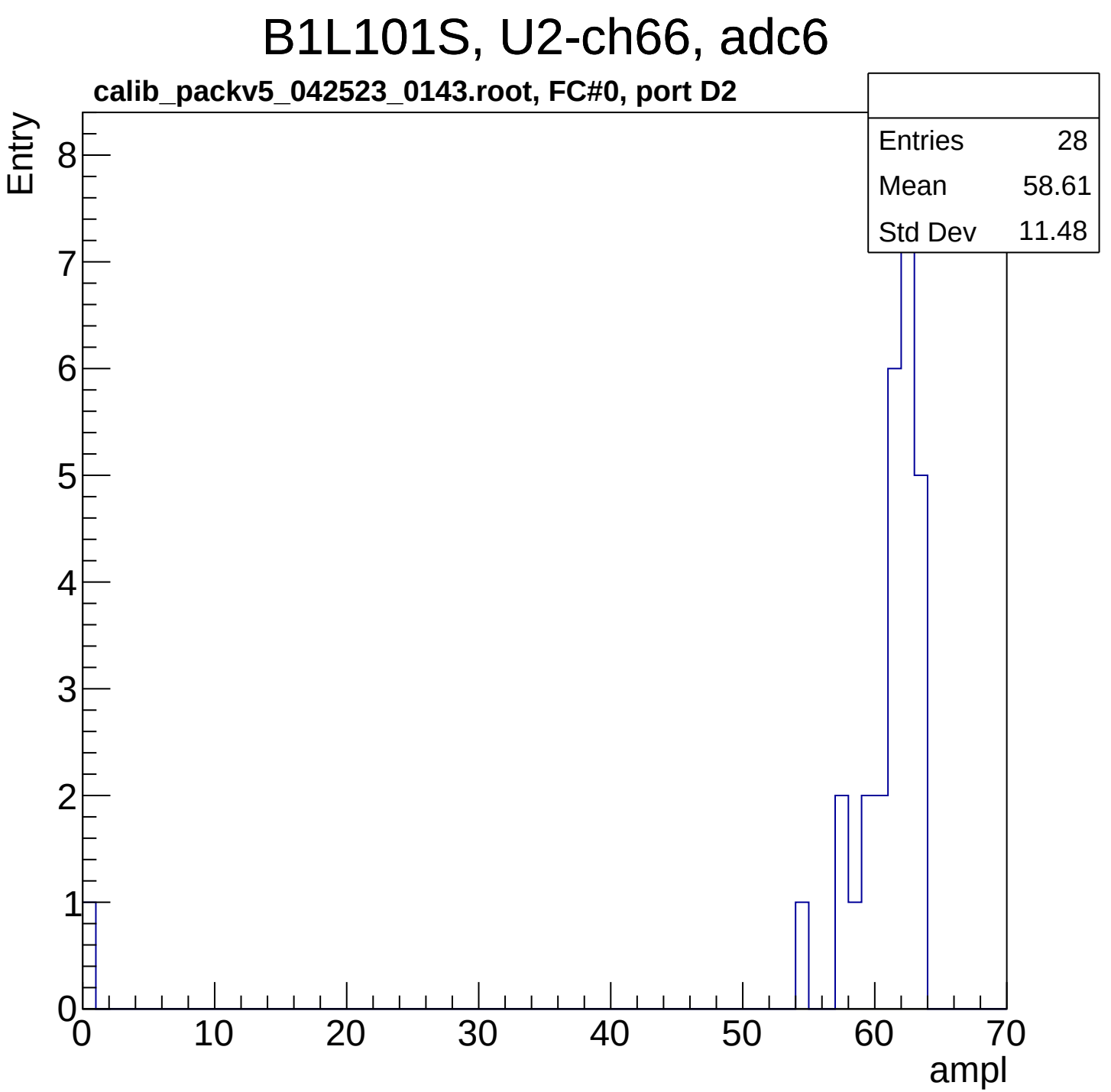

B1L101S, U2-ch66, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 34.23
Std Dev 3.7
Gaus mean : 34.9394
Gaus Width: 3.9834
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

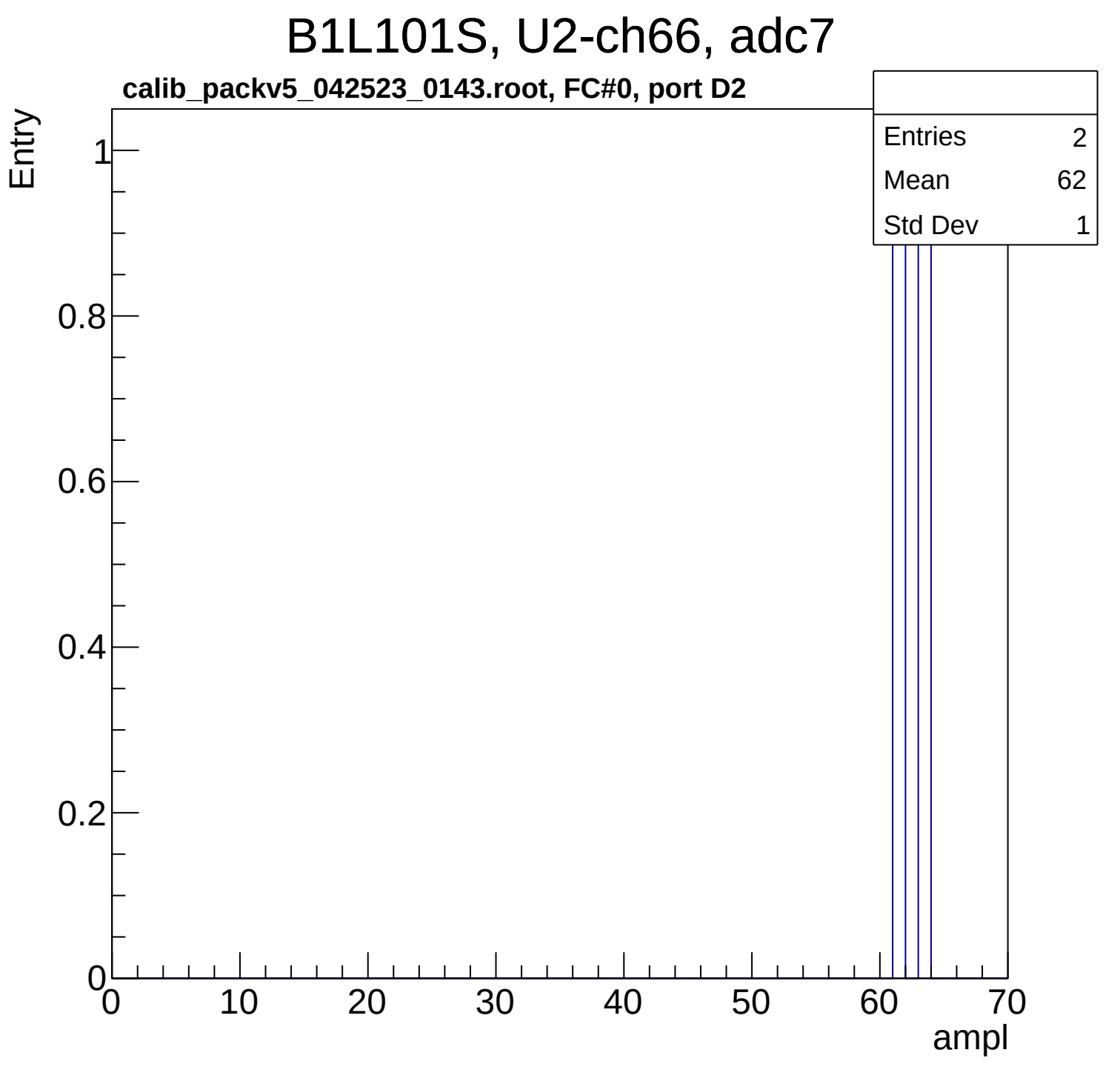

B1L101S, U2-ch66, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 40.47
Std Dev 3.652
Gaus mean : 41.1699
Gaus Width: 4.3365
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

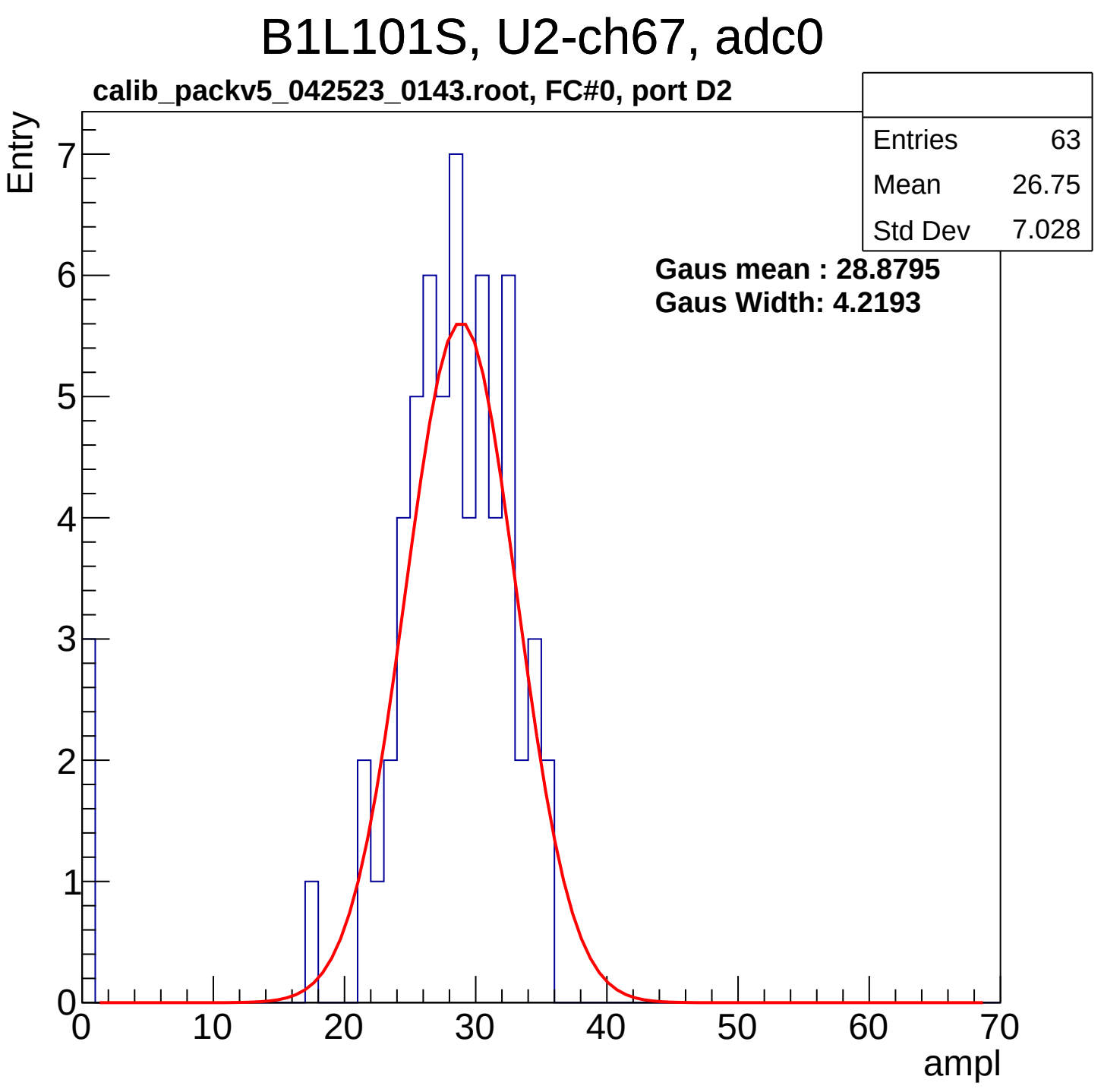

B1L101S, U2-ch66, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 47.77
Std Dev 3.334
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

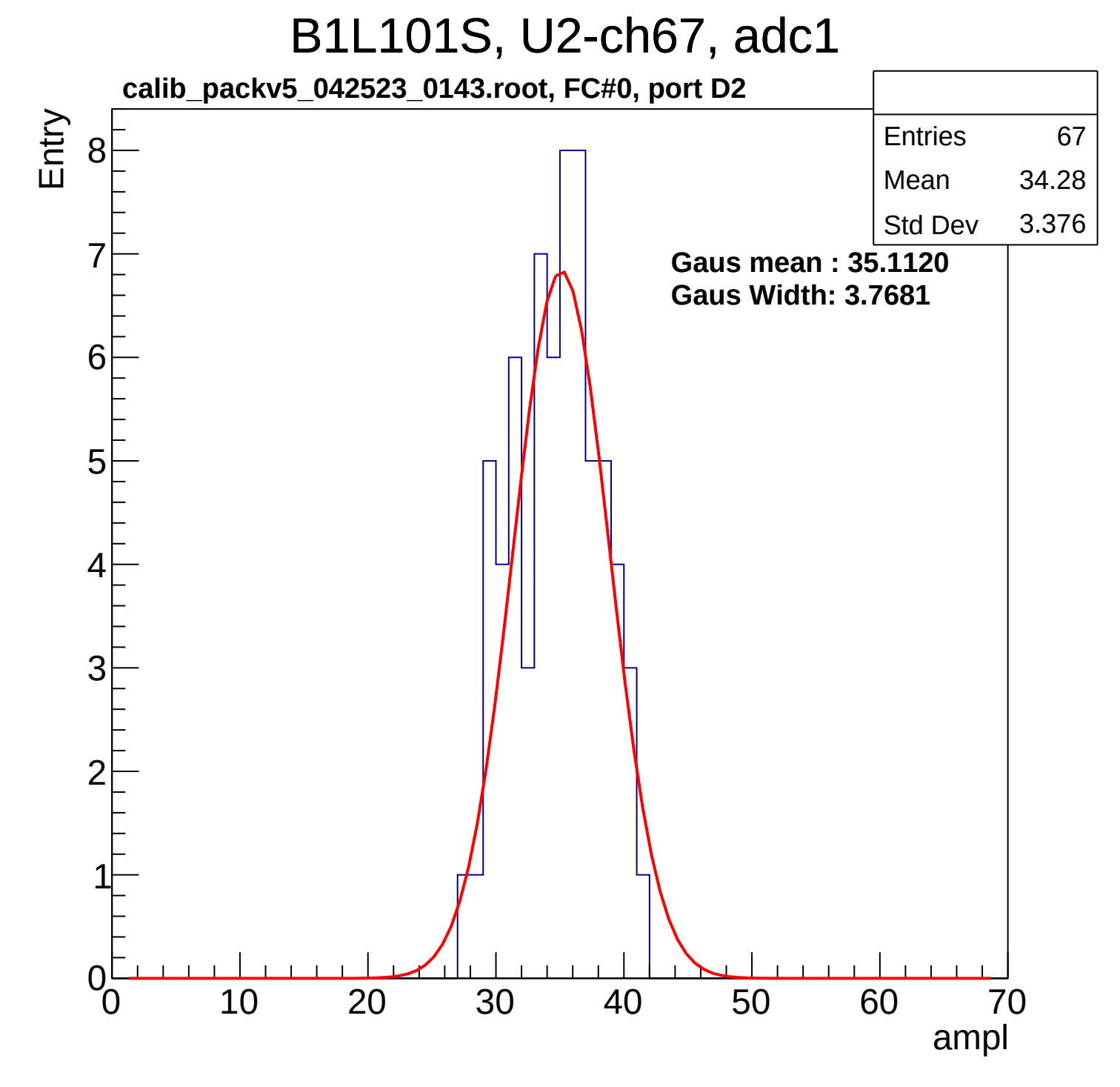

B1L101S, U2-ch66, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 39
Mean 53.92
Std Dev 2.868
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

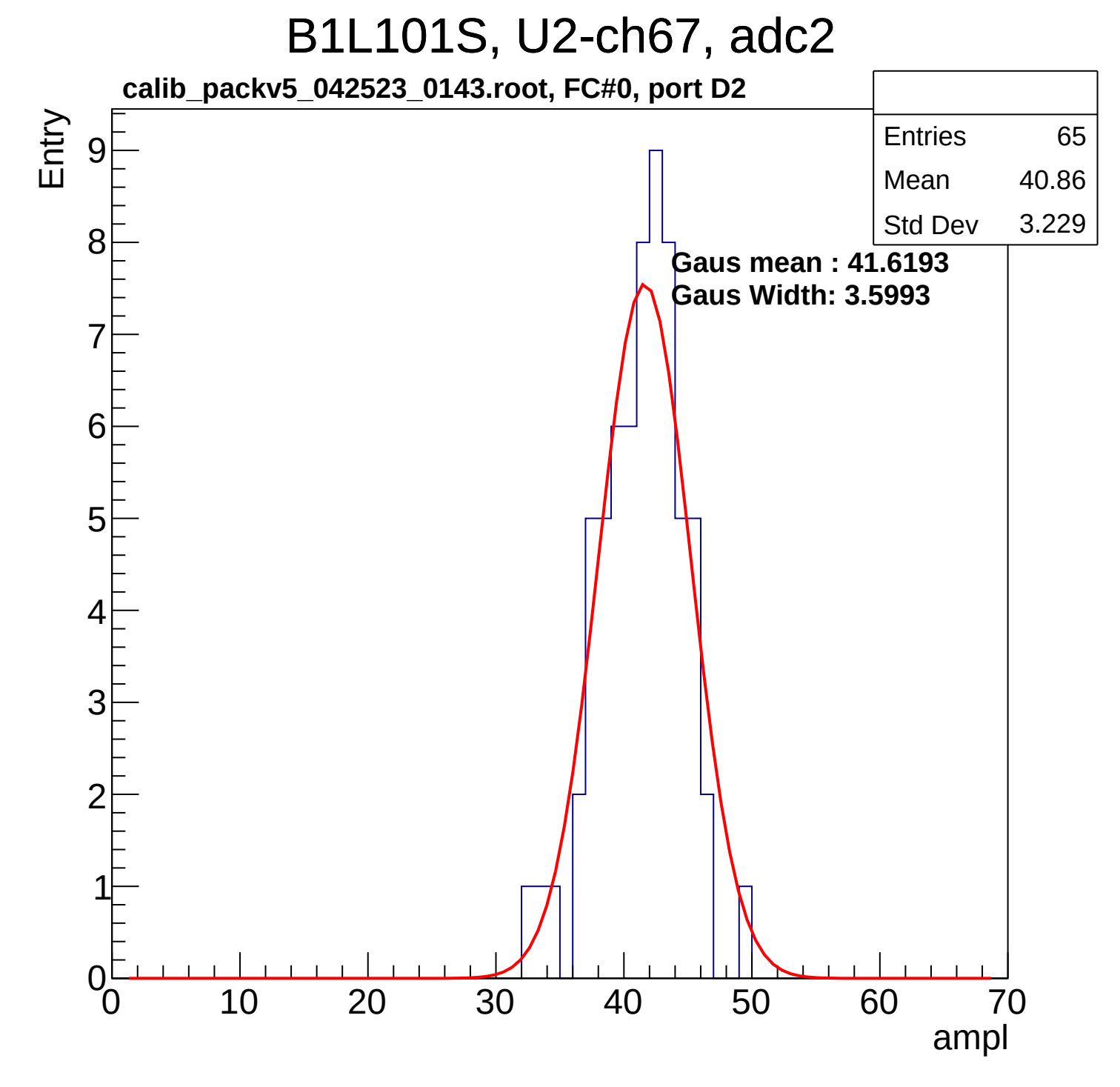

B1L101S, U2-ch66, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 58.18
Std Dev 2.693
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

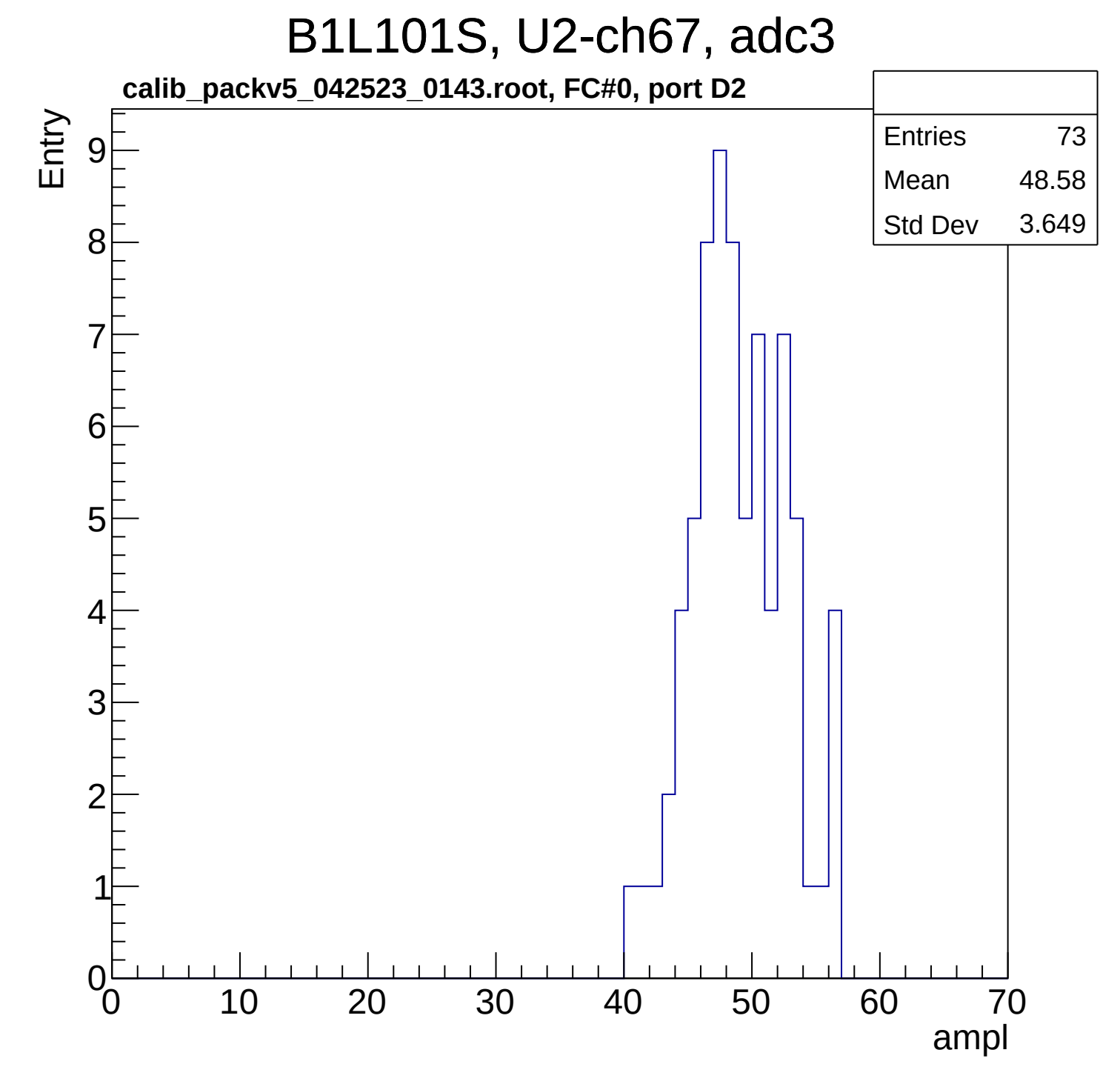

B1L101S, U2-ch66, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 28
Mean 58.61
Std Dev 11.48
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

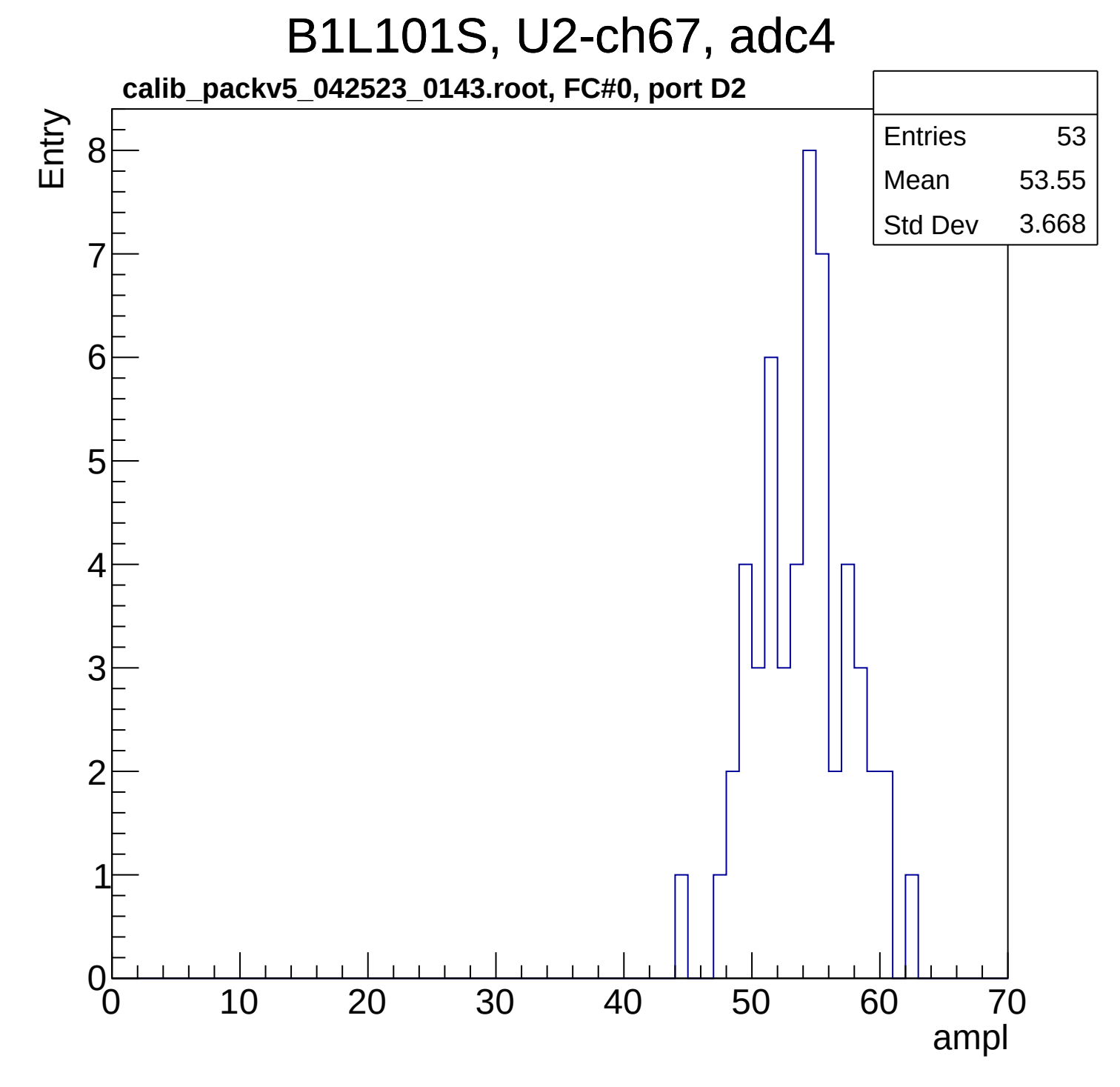

B1L101S, U2-ch66, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 62
Std Dev 1
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

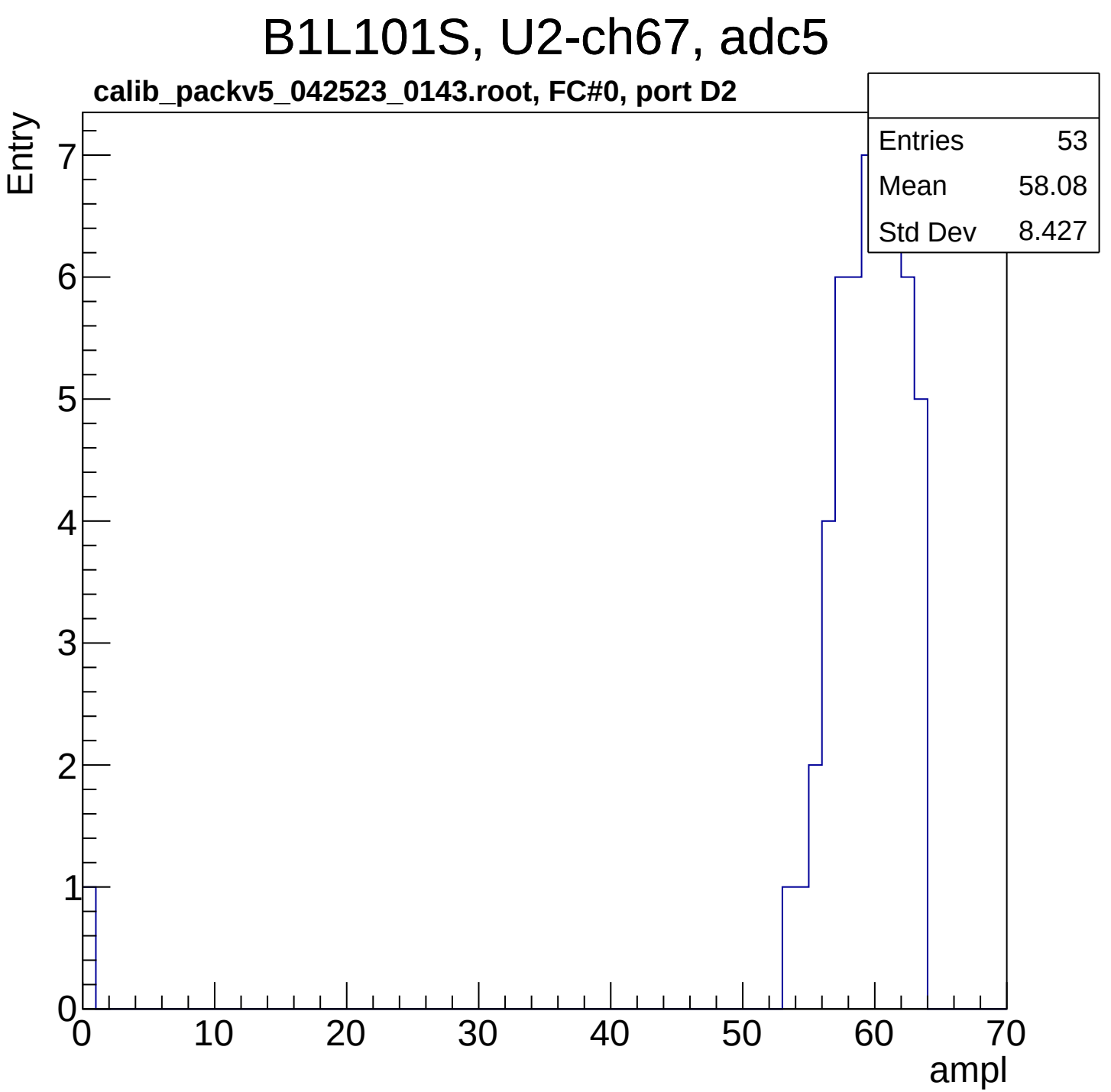

B1L101S, U2-ch67, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 26.75
Std Dev 7.028
Gaus mean : 28.8795
Gaus Width: 4.2193
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

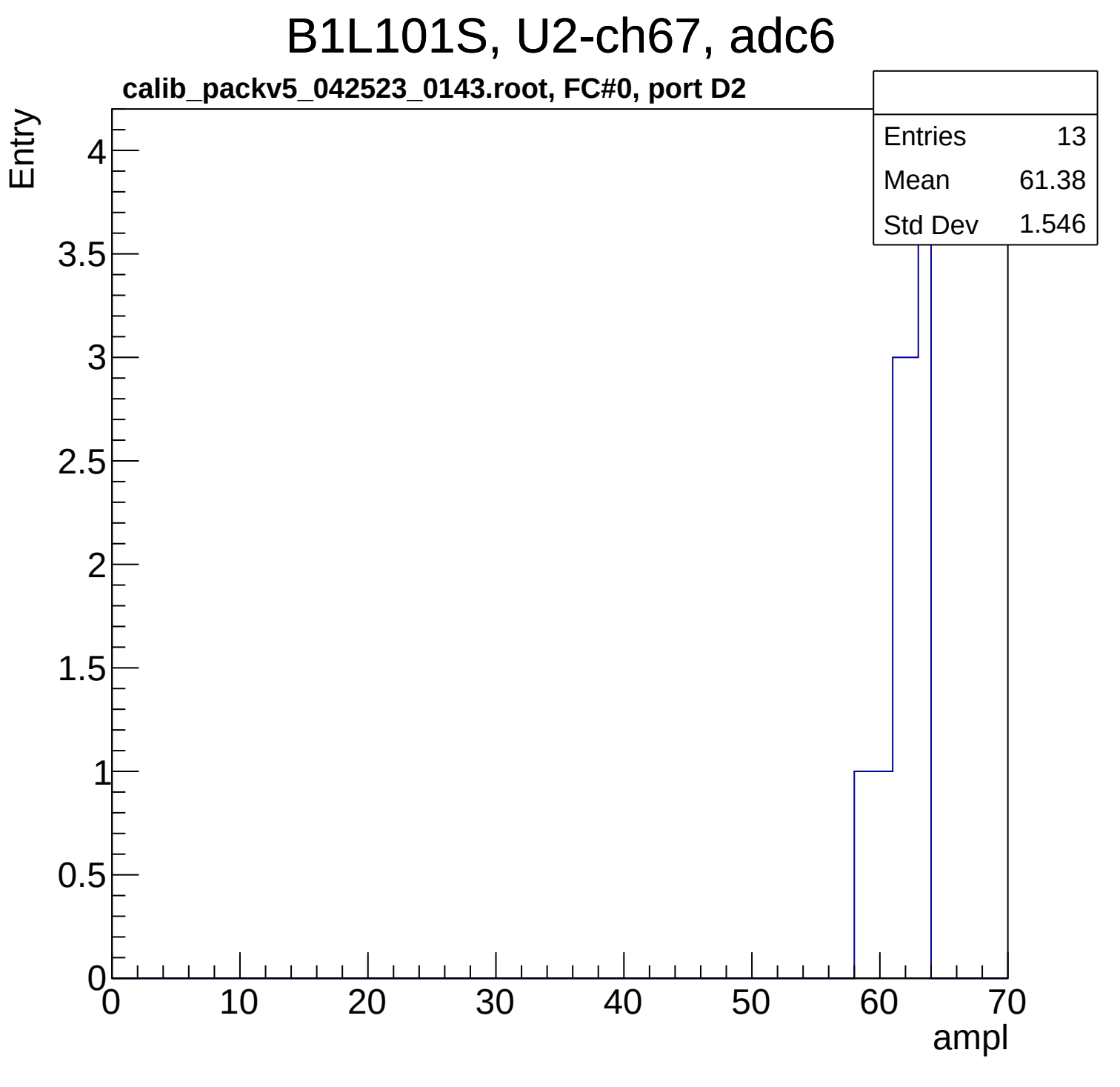

B1L101S, U2-ch67, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 34.28
Std Dev 3.376
Gaus mean : 35.1120
Gaus Width: 3.7681
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

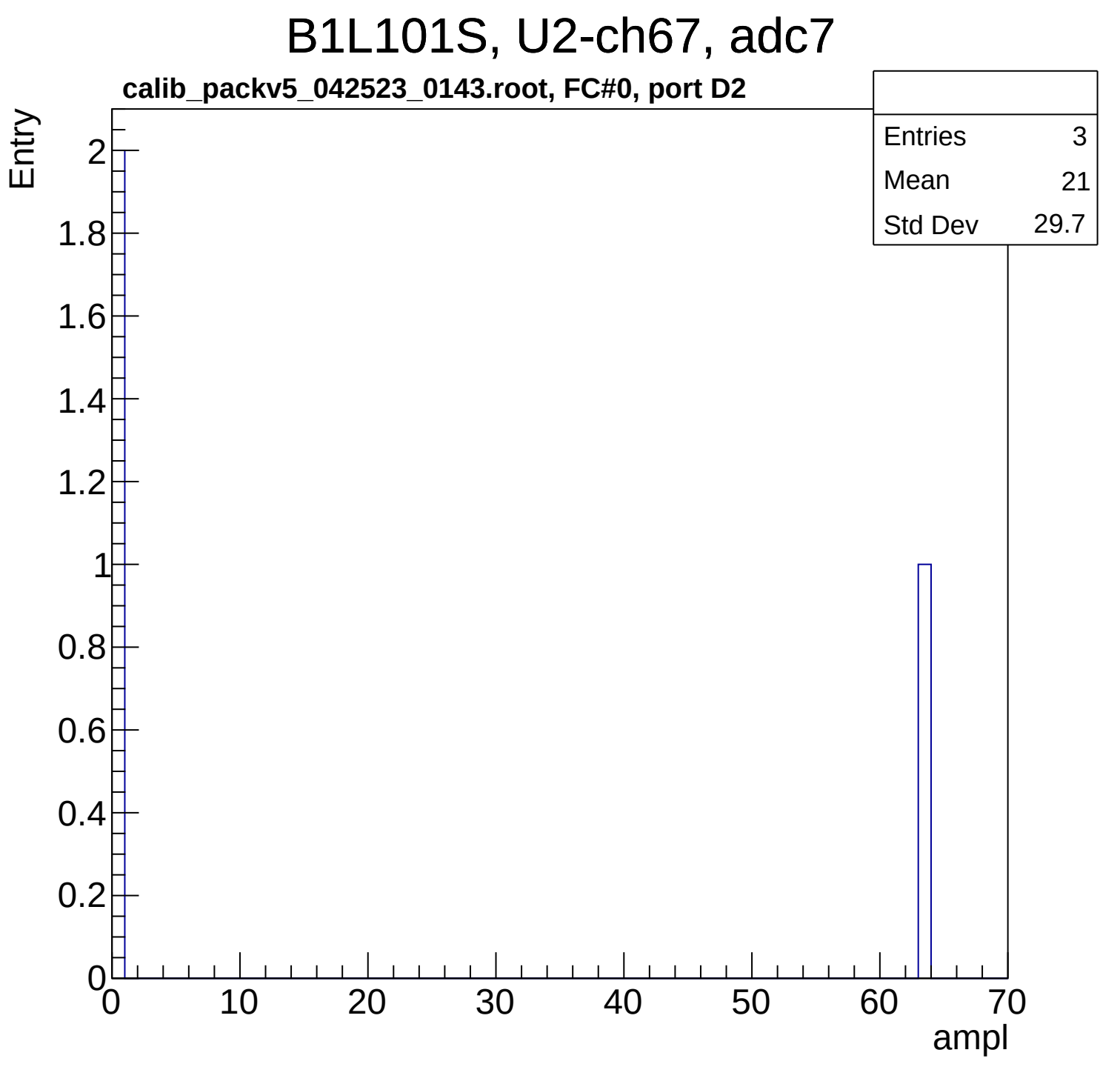

B1L101S, U2-ch67, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 40.86
Std Dev 3.229
Gaus mean : 41.6193
Gaus Width: 3.5993
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

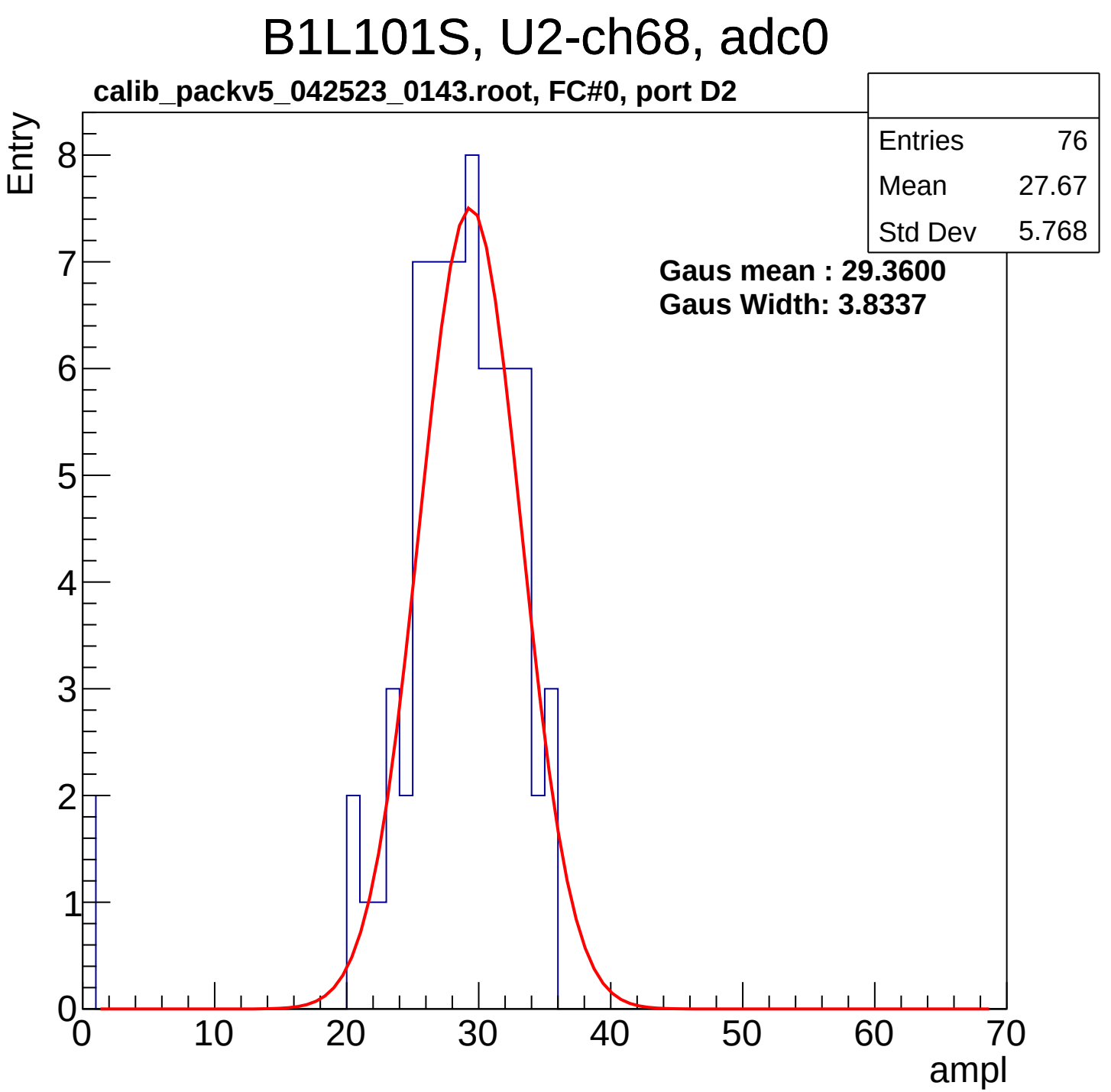

B1L101S, U2-ch67, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 48.58
Std Dev 3.649
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

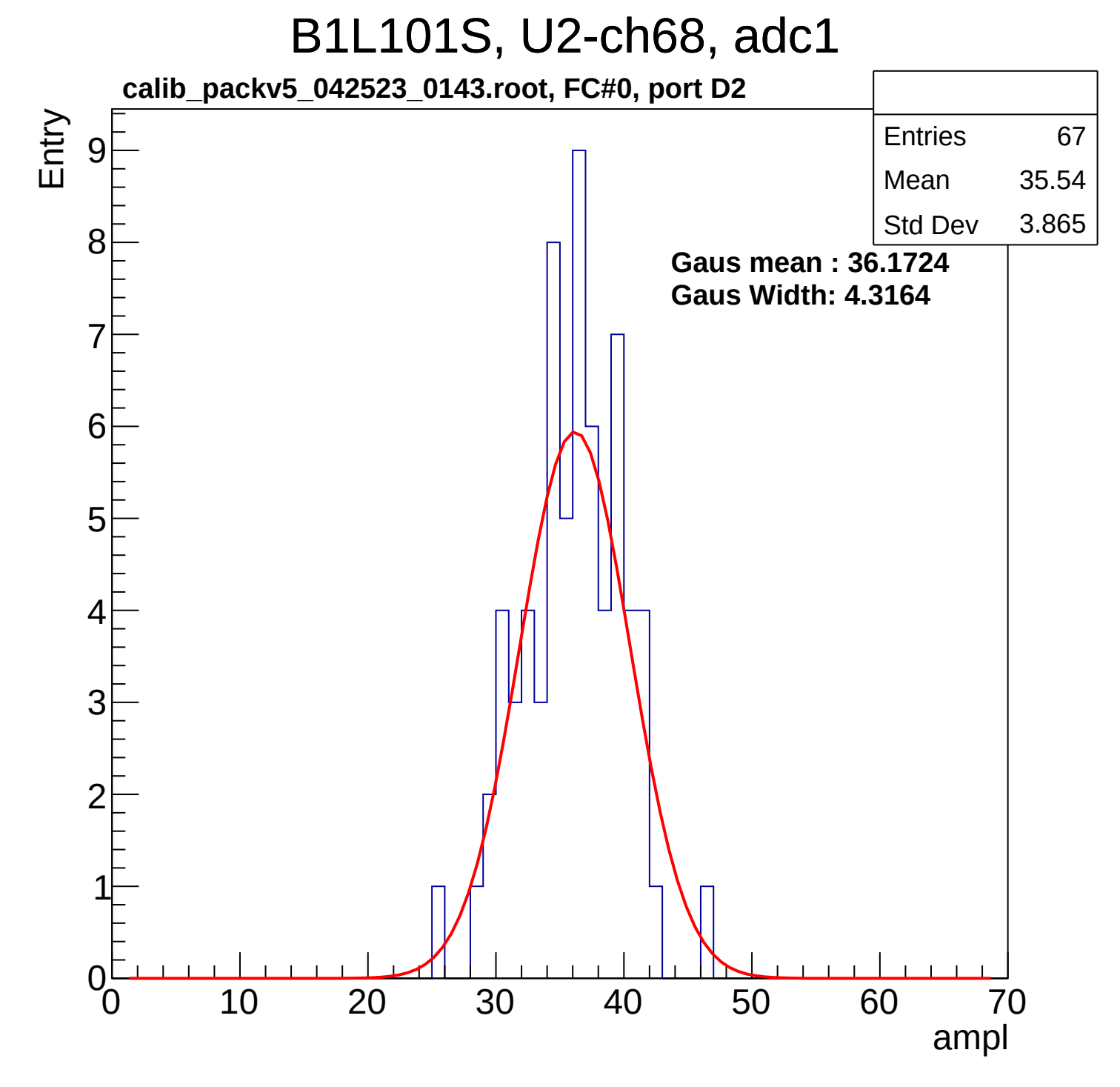

B1L101S, U2-ch67, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 53.55
Std Dev 3.668
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

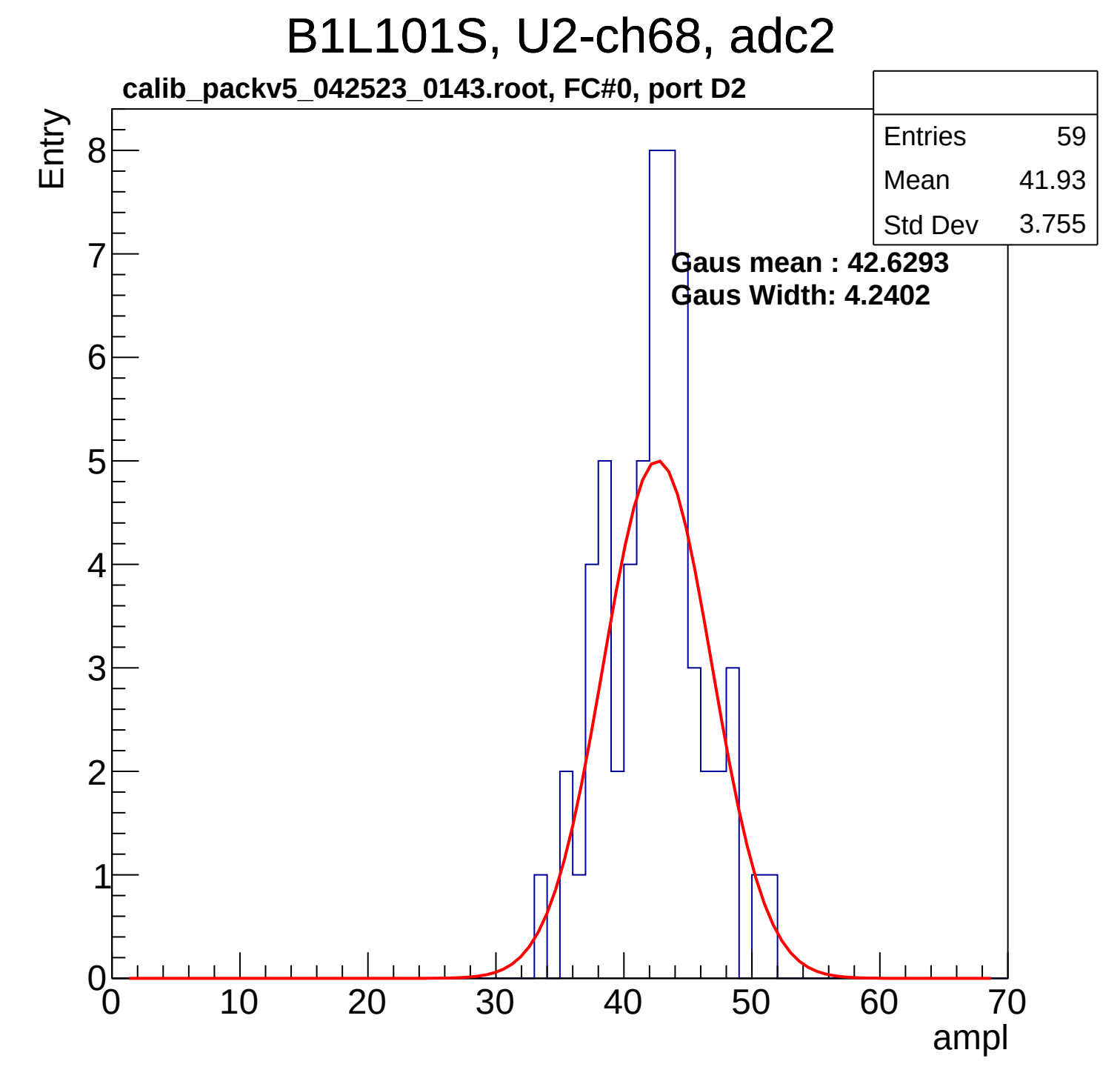

B1L101S, U2-ch67, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 58.08
Std Dev 8.427
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

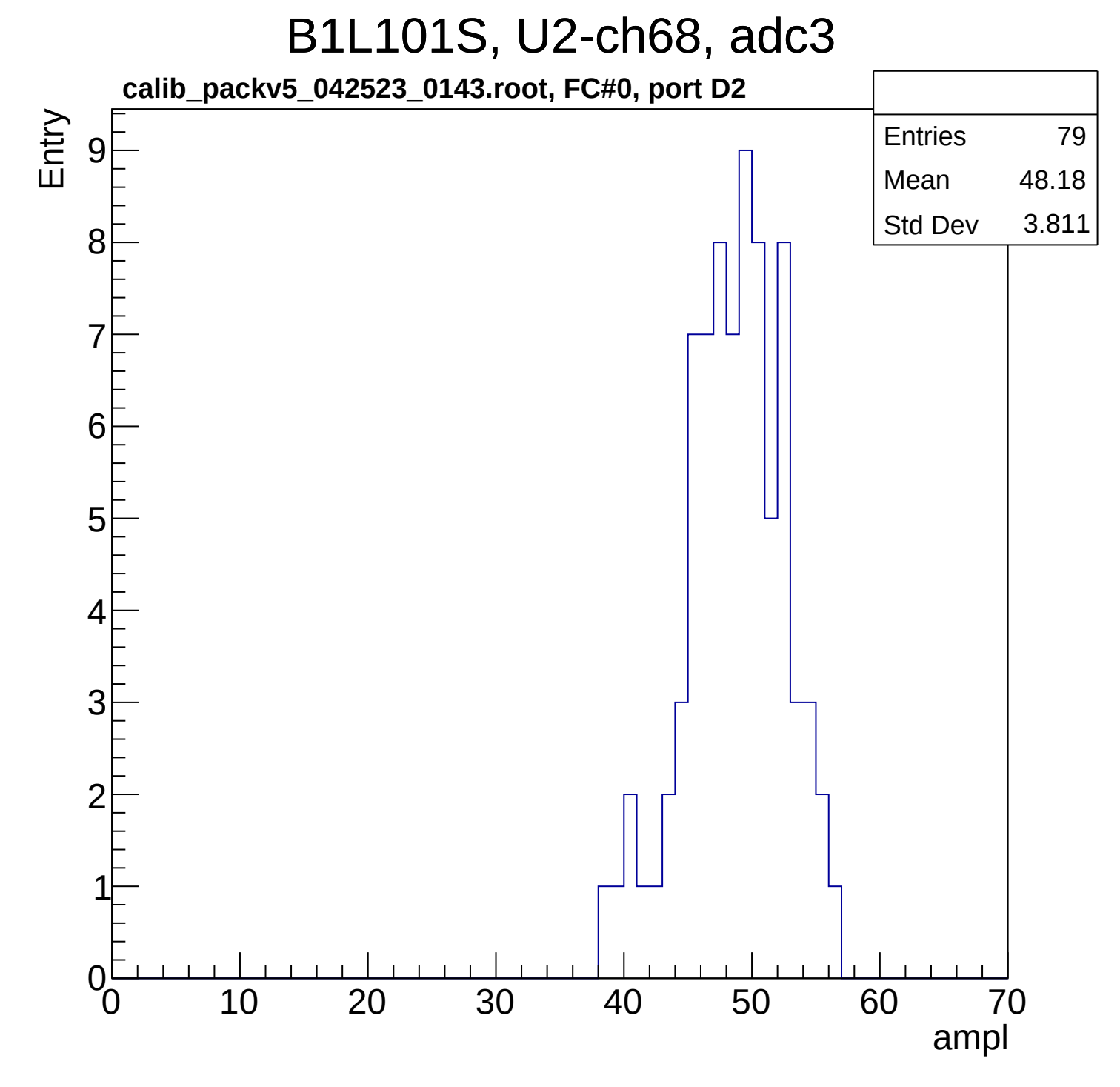

B1L101S, U2-ch67, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 13
Mean 61.38
Std Dev 1.546
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

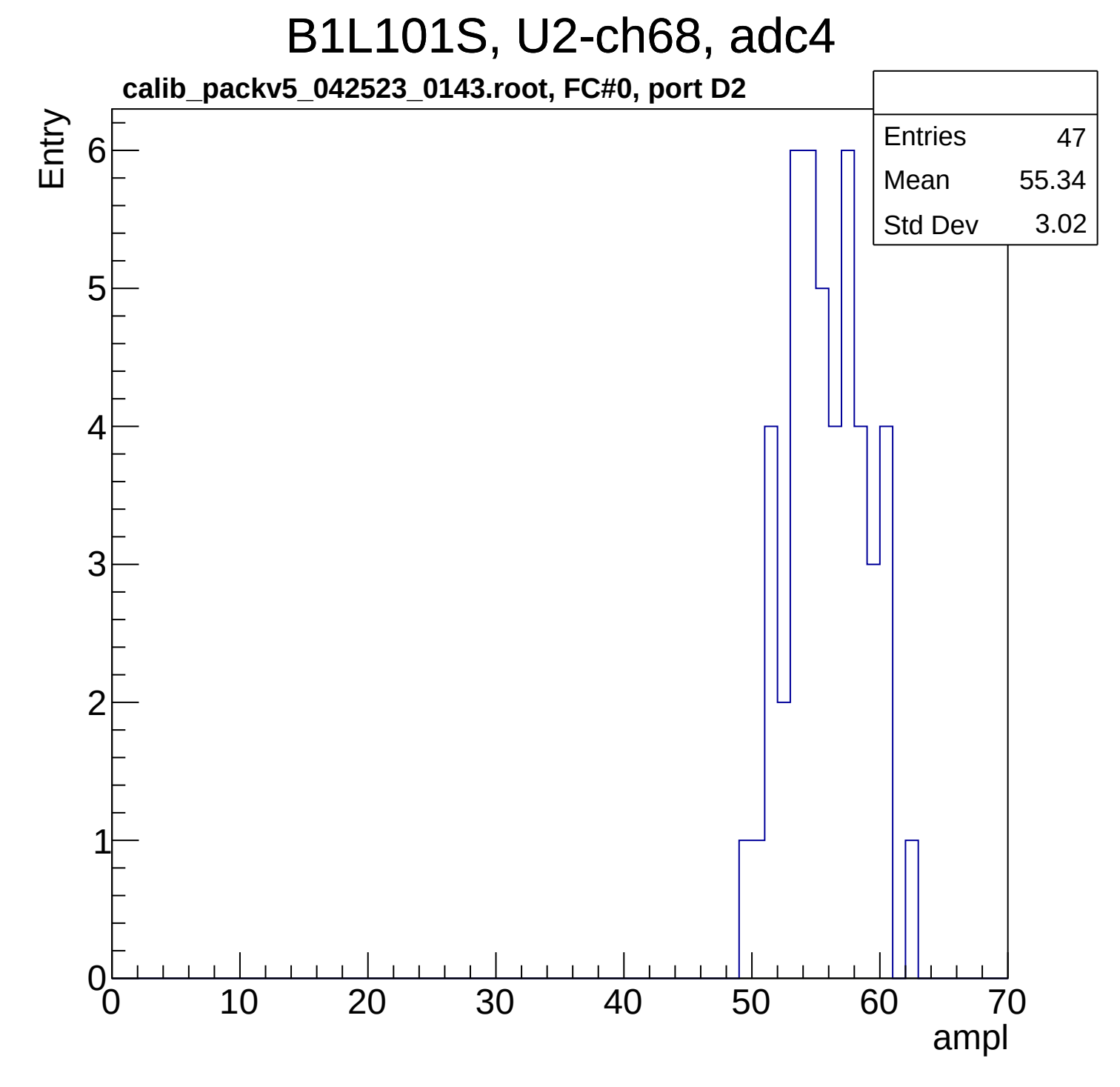

B1L101S, U2-ch67, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 21
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

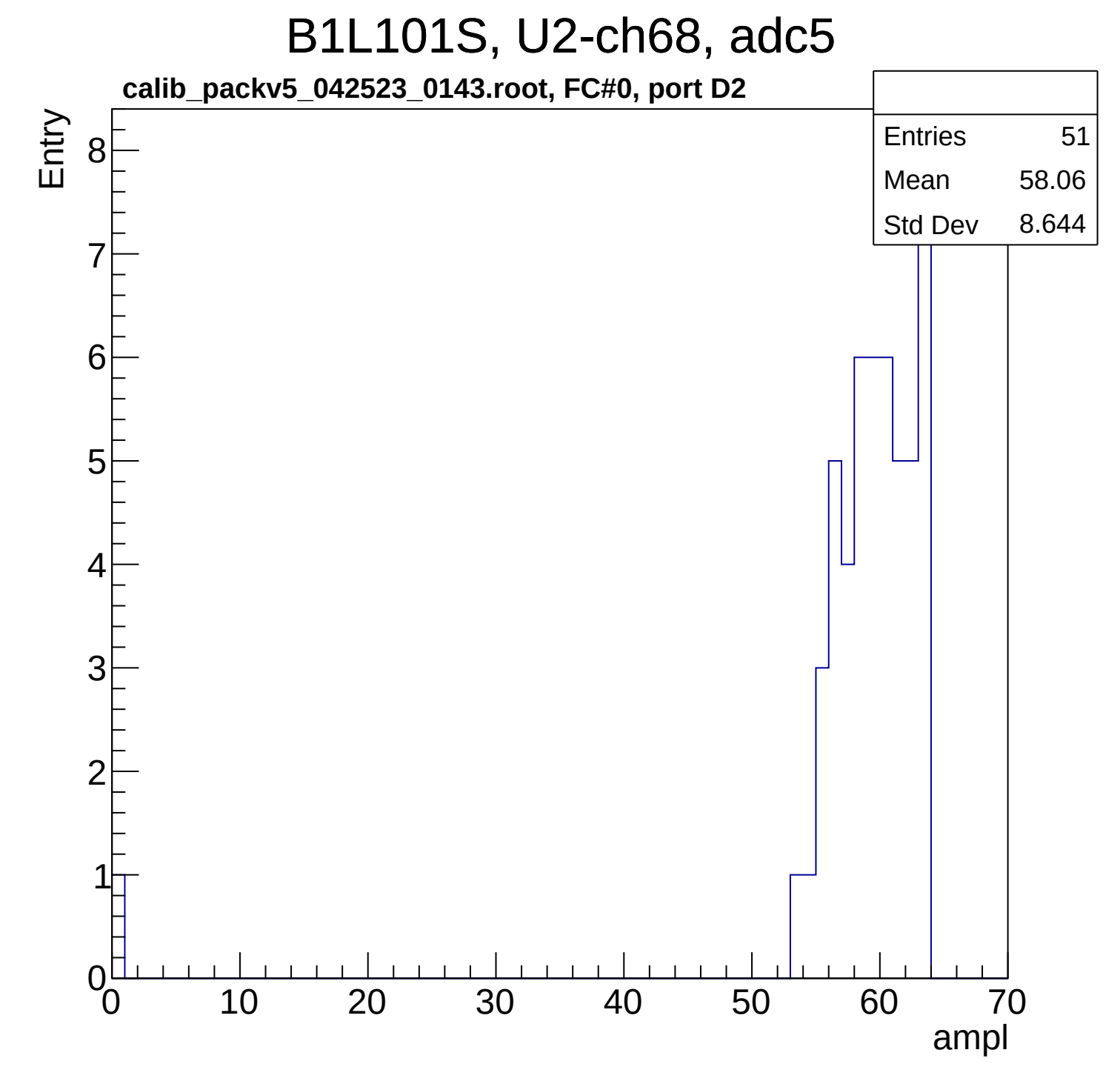

B1L101S, U2-ch68, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 27.67
Std Dev 5.768
Gaus mean : 29.3600
Gaus Width: 3.8337
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

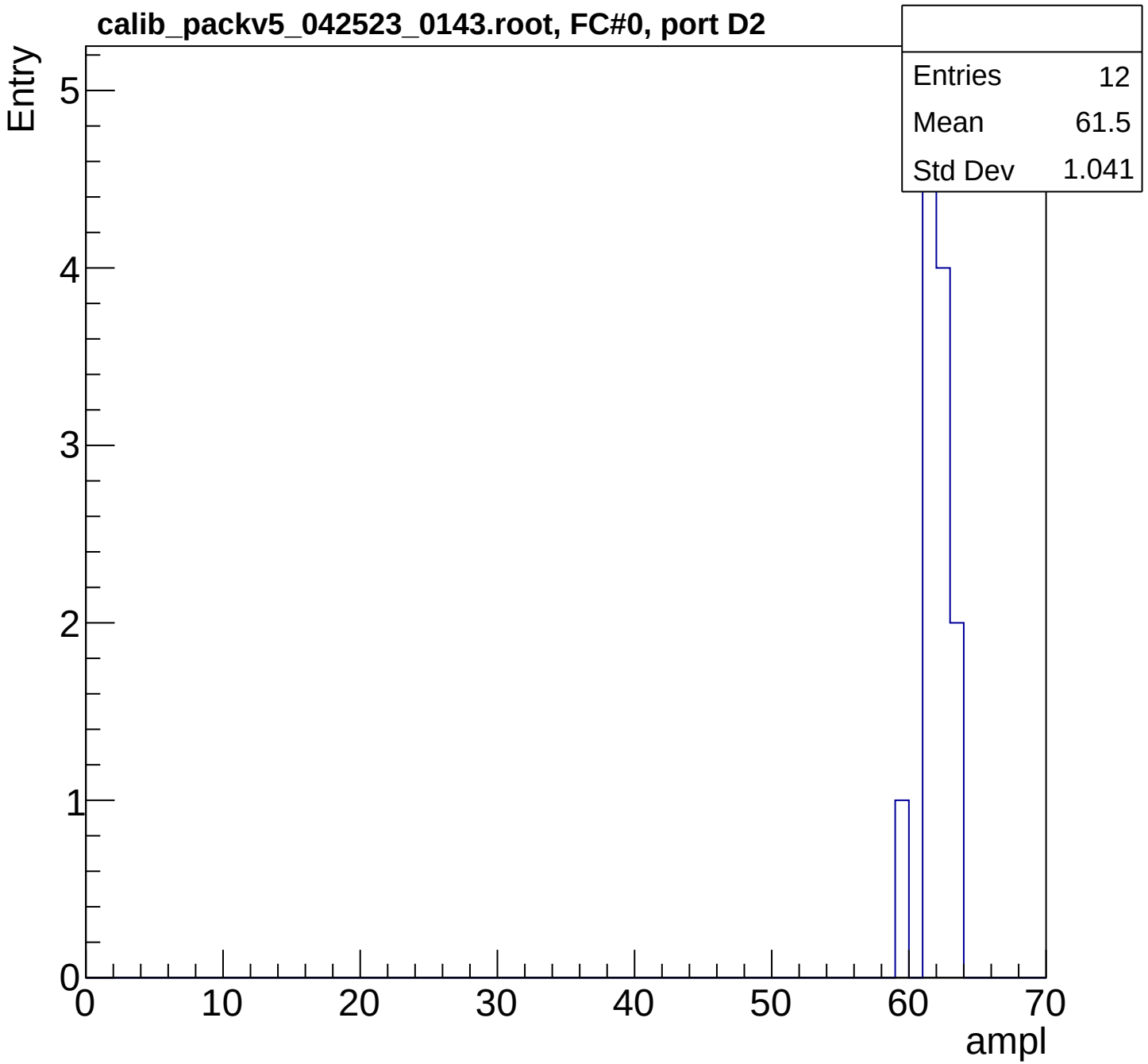

B1L101S, U2-ch68, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 35.54
Std Dev 3.865
Gaus mean : 36.1724
Gaus Width: 4.3164
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

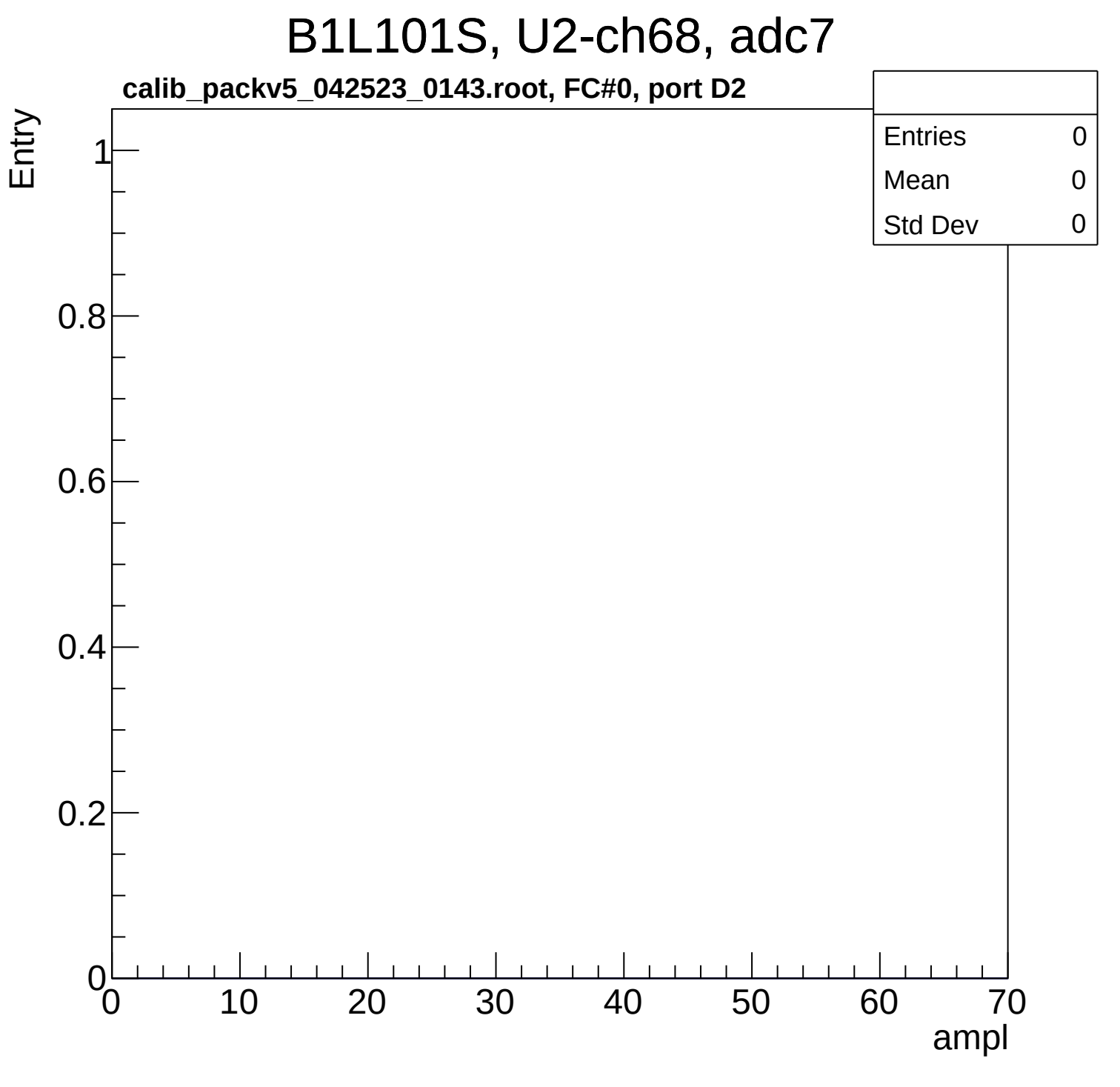

B1L101S, U2-ch68, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 41.93
Std Dev 3.755
Gaus mean : 42.6293
Gaus Width: 4.2402
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

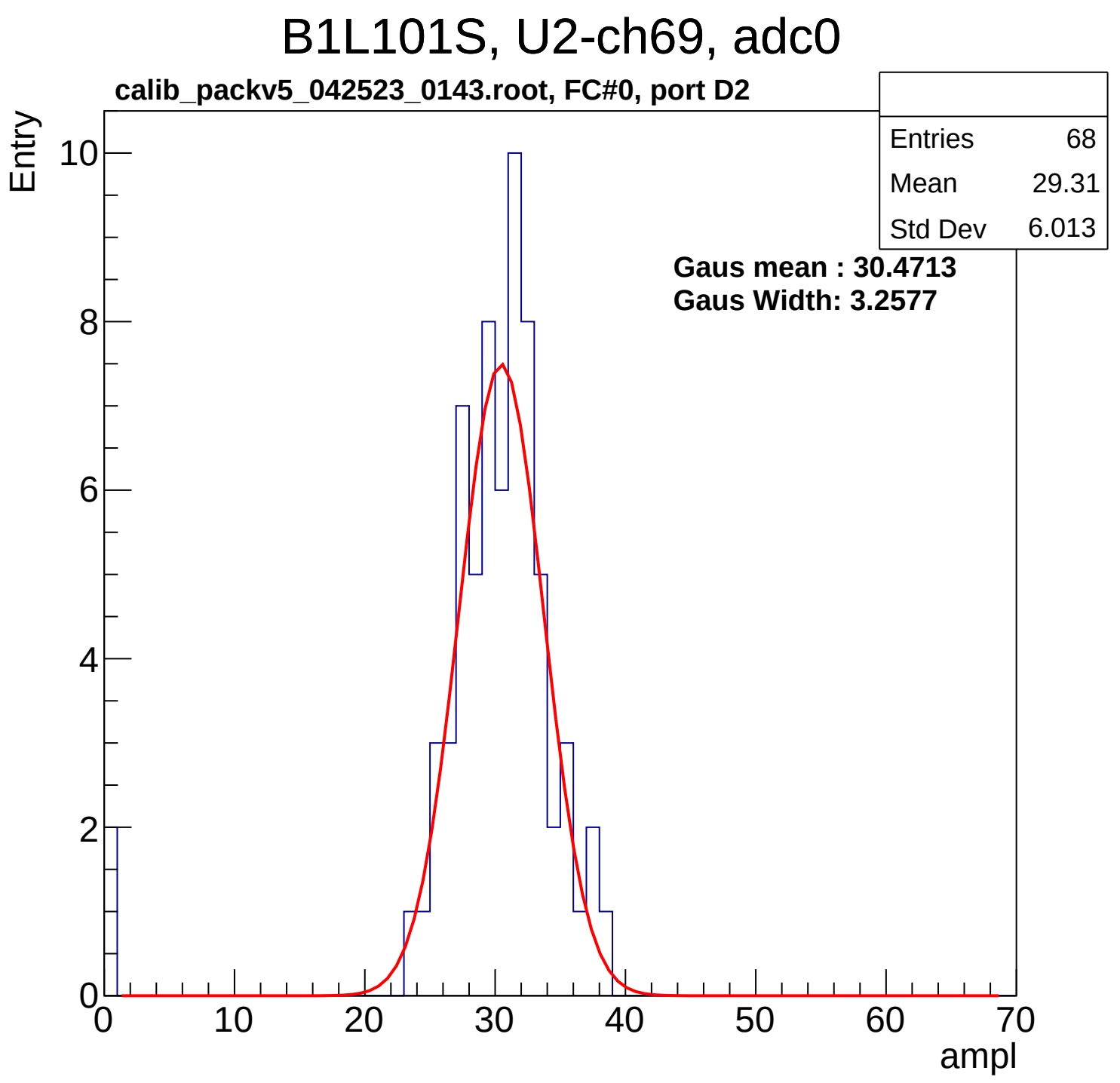

B1L101S, U2-ch68, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 48.18
Std Dev 3.811
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

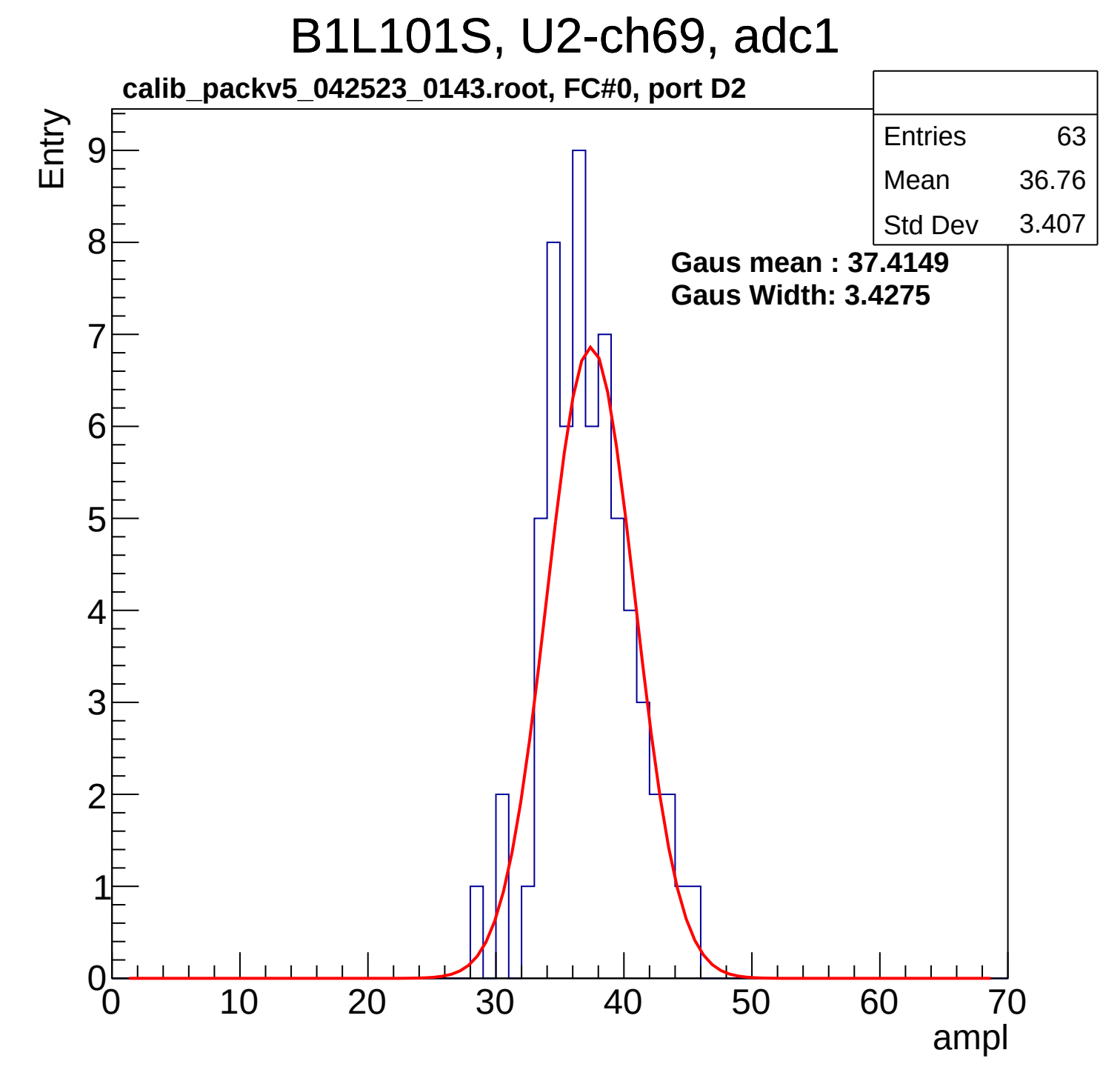

B1L101S, U2-ch68, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 55.34
Std Dev 3.02
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

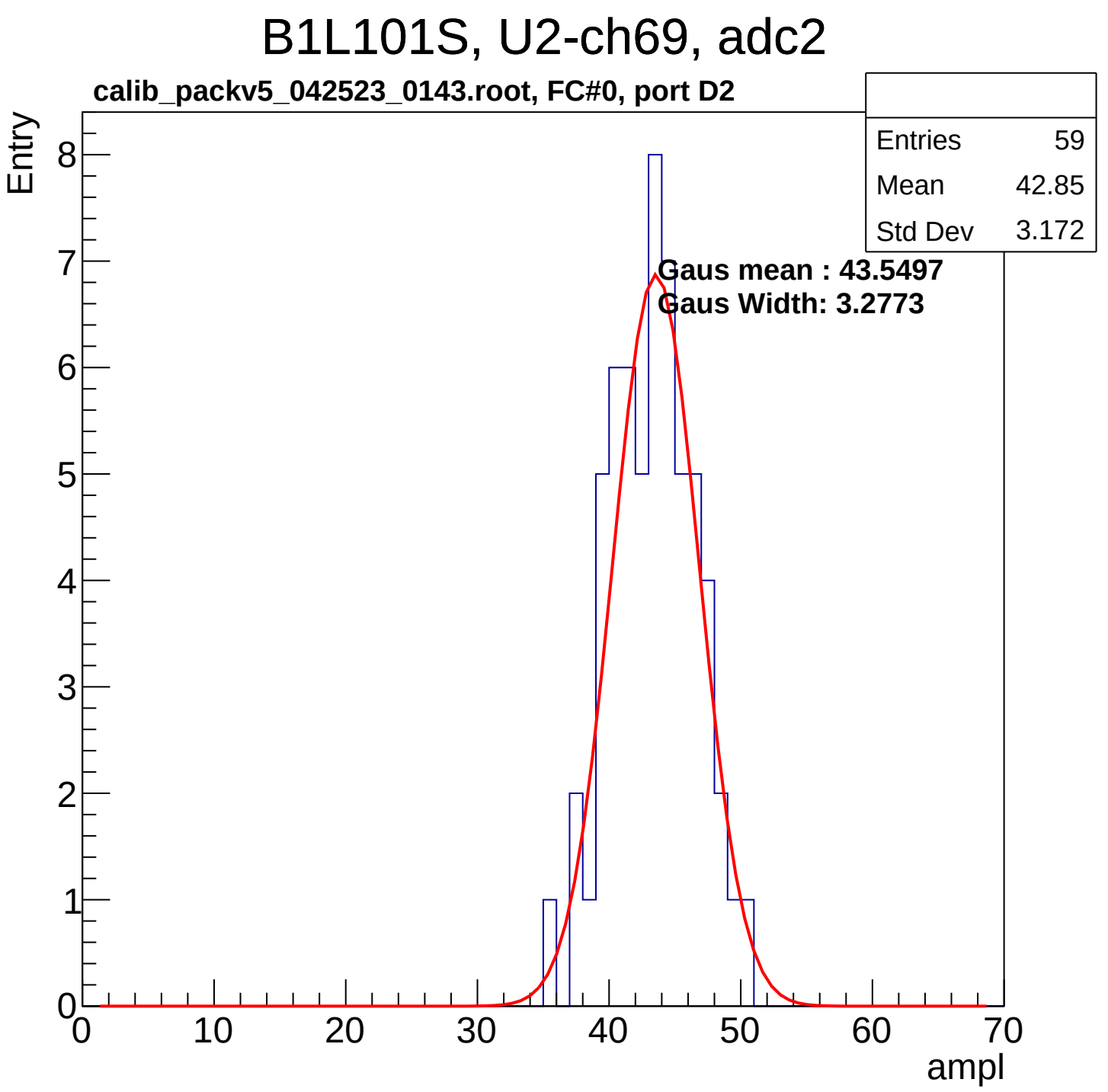

B1L101S, U2-ch68, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 58.06
Std Dev 8.644
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

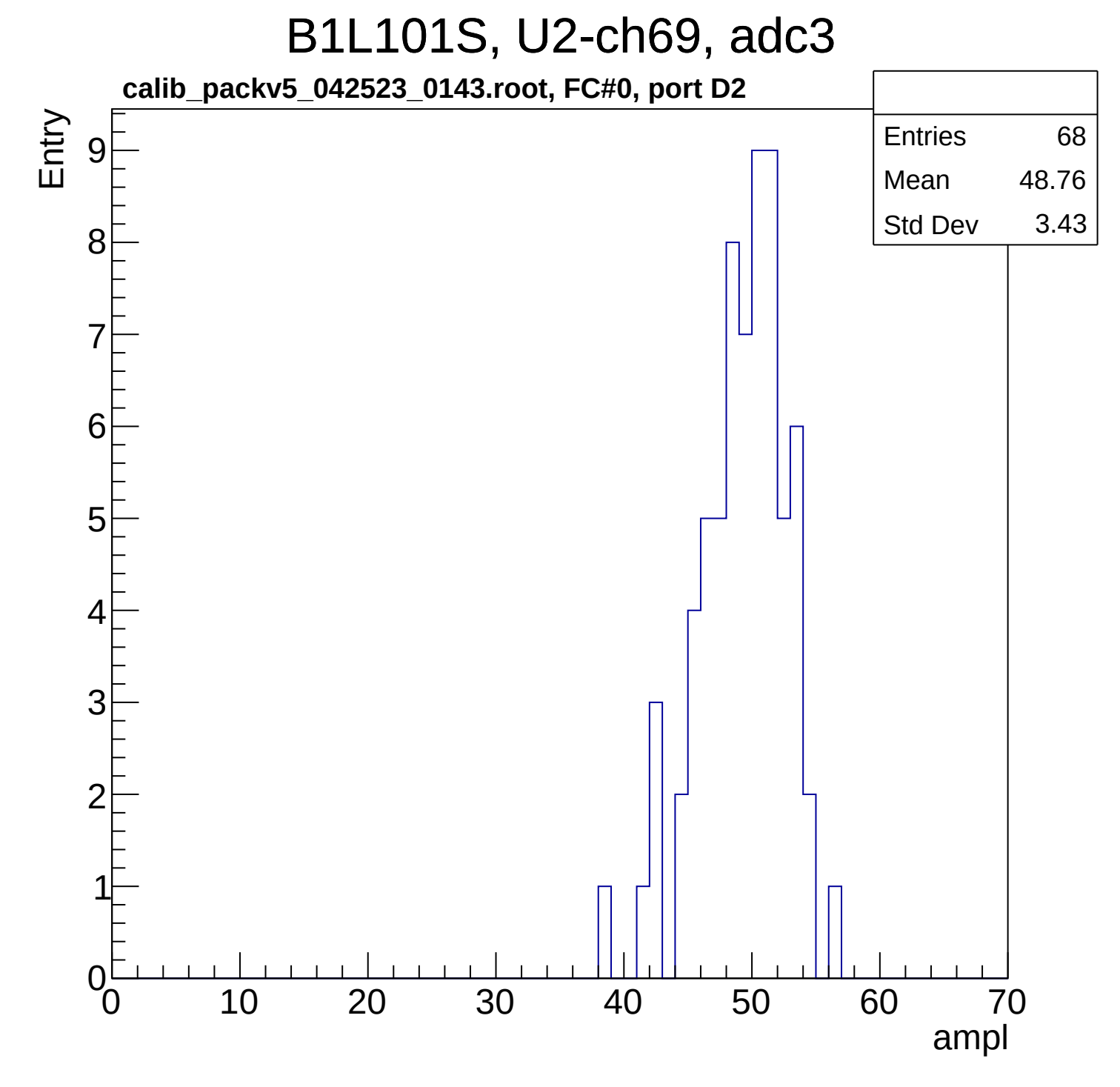

B1L101S, U2-ch68, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 12
Mean 61.5
Std Dev 1.041
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

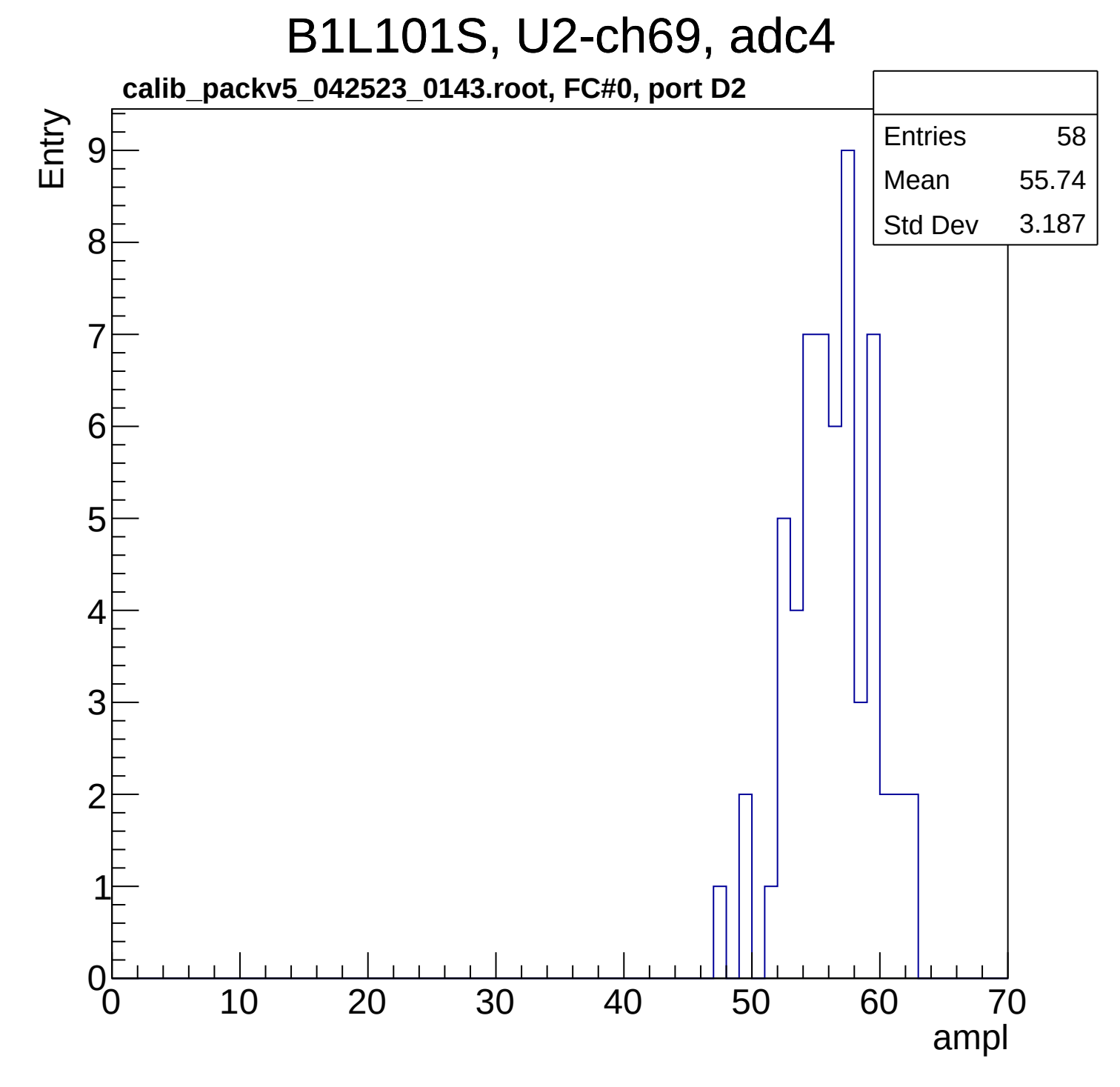

B1L101S, U2-ch68, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

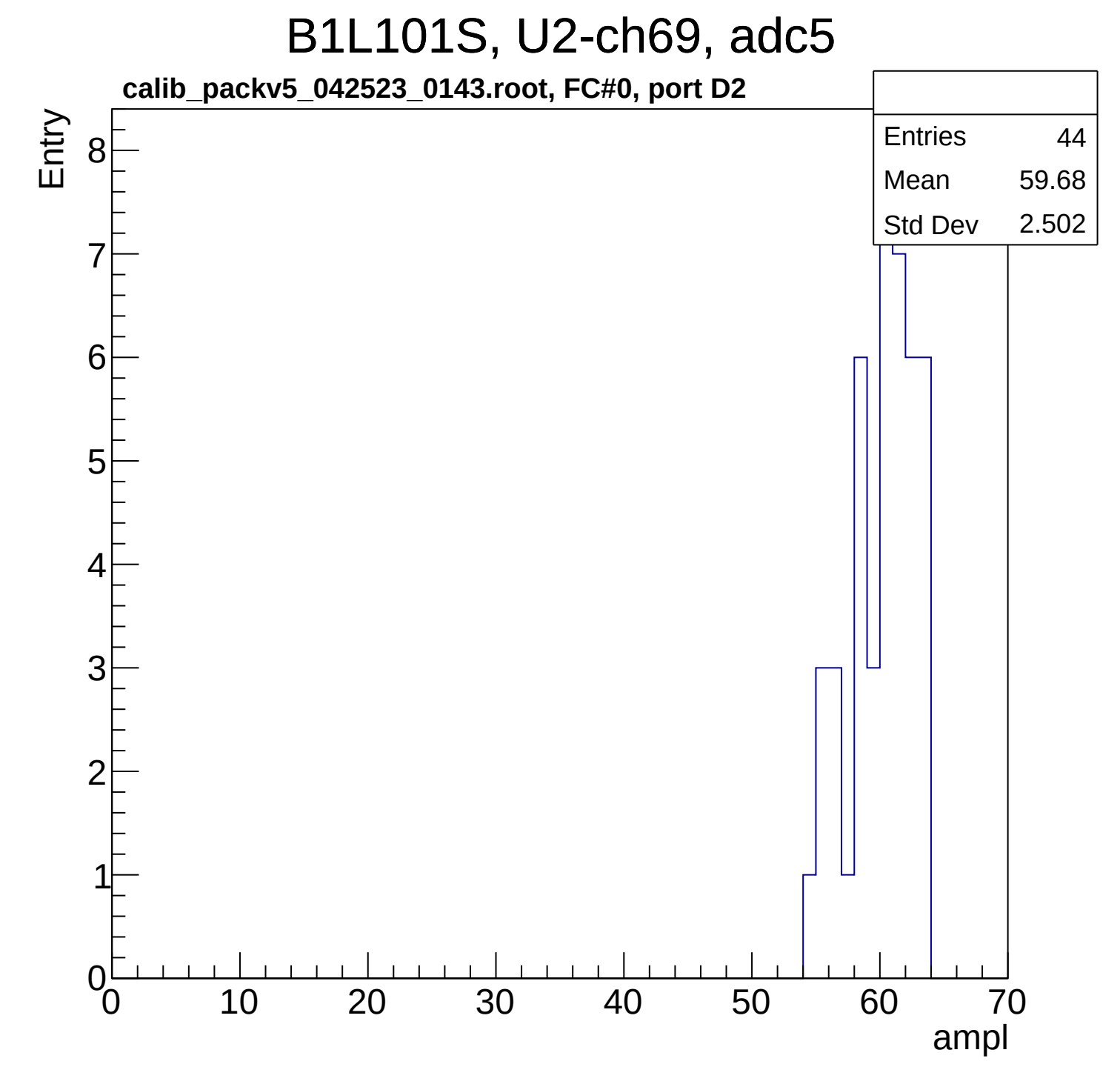

B1L101S, U2-ch69, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 29.31
Std Dev 6.013
Gaus mean : 30.4713
Gaus Width: 3.2577
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

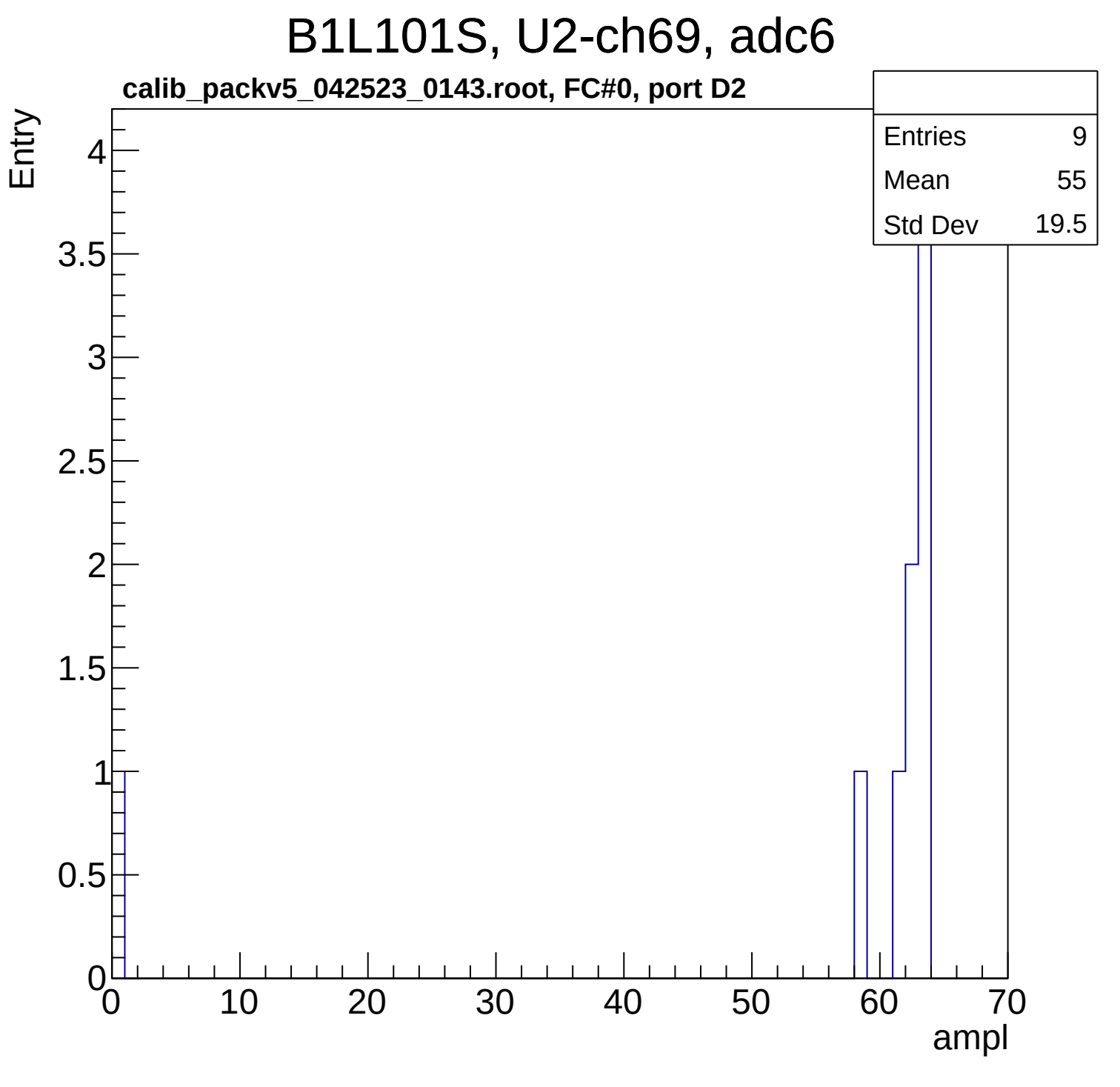

B1L101S, U2-ch69, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 36.76
Std Dev 3.407
Gaus mean : 37.4149
Gaus Width: 3.4275
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

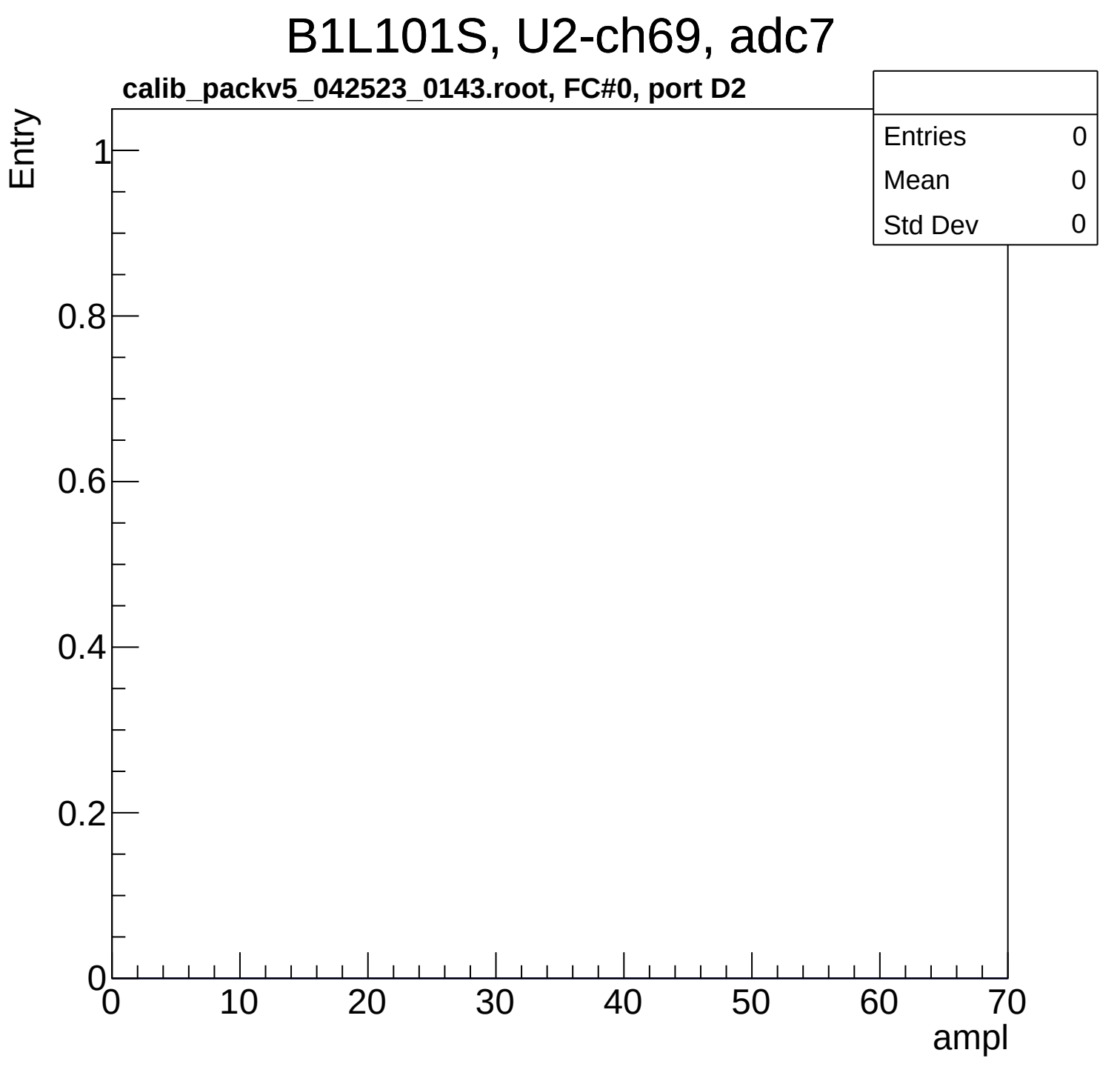

B1L101S, U2-ch69, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 42.85
Std Dev 3.172
Gaus mean : 43.5497
Gaus Width: 3.2773
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

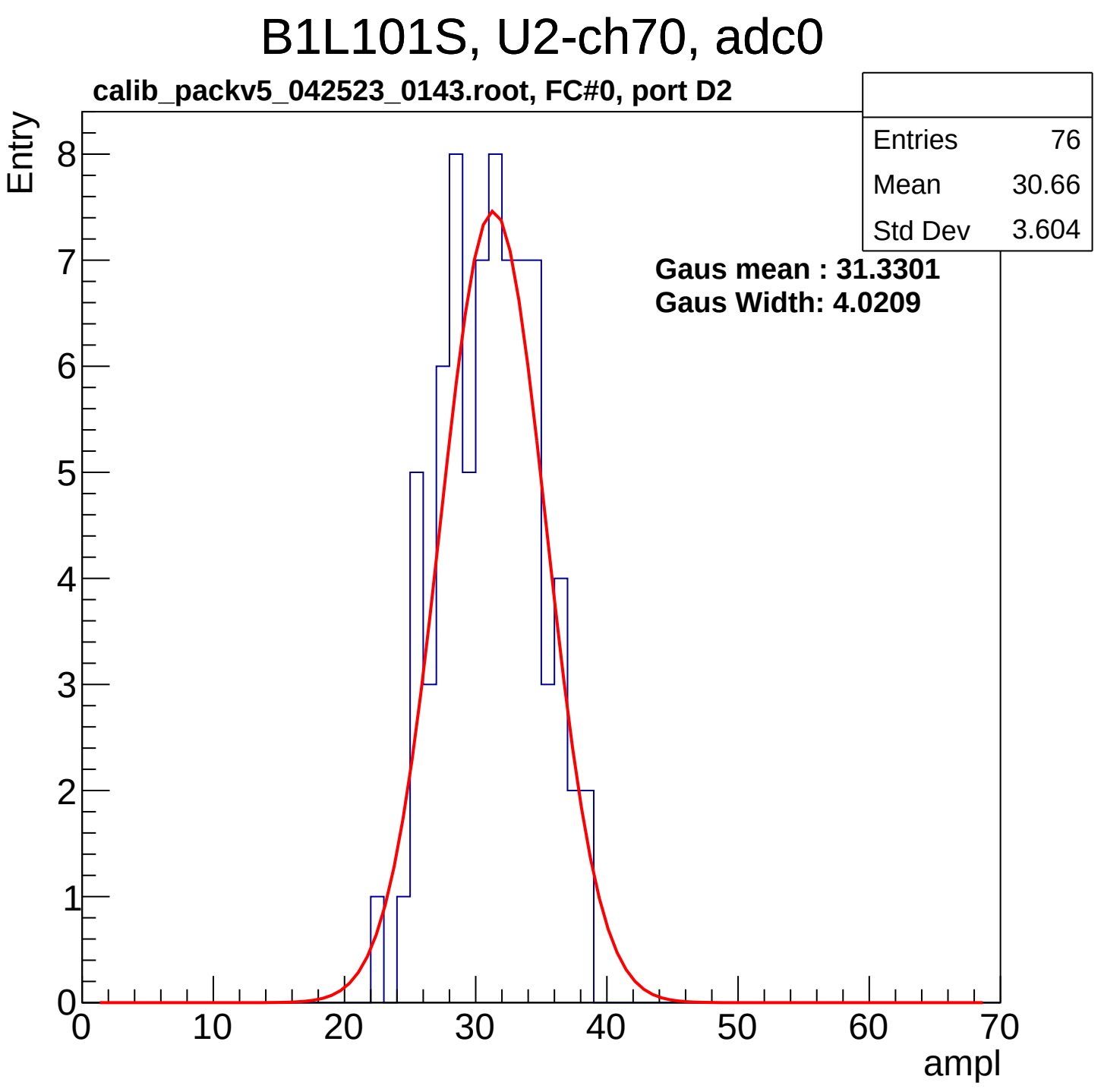

B1L101S, U2-ch69, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 48.76
Std Dev 3.43
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

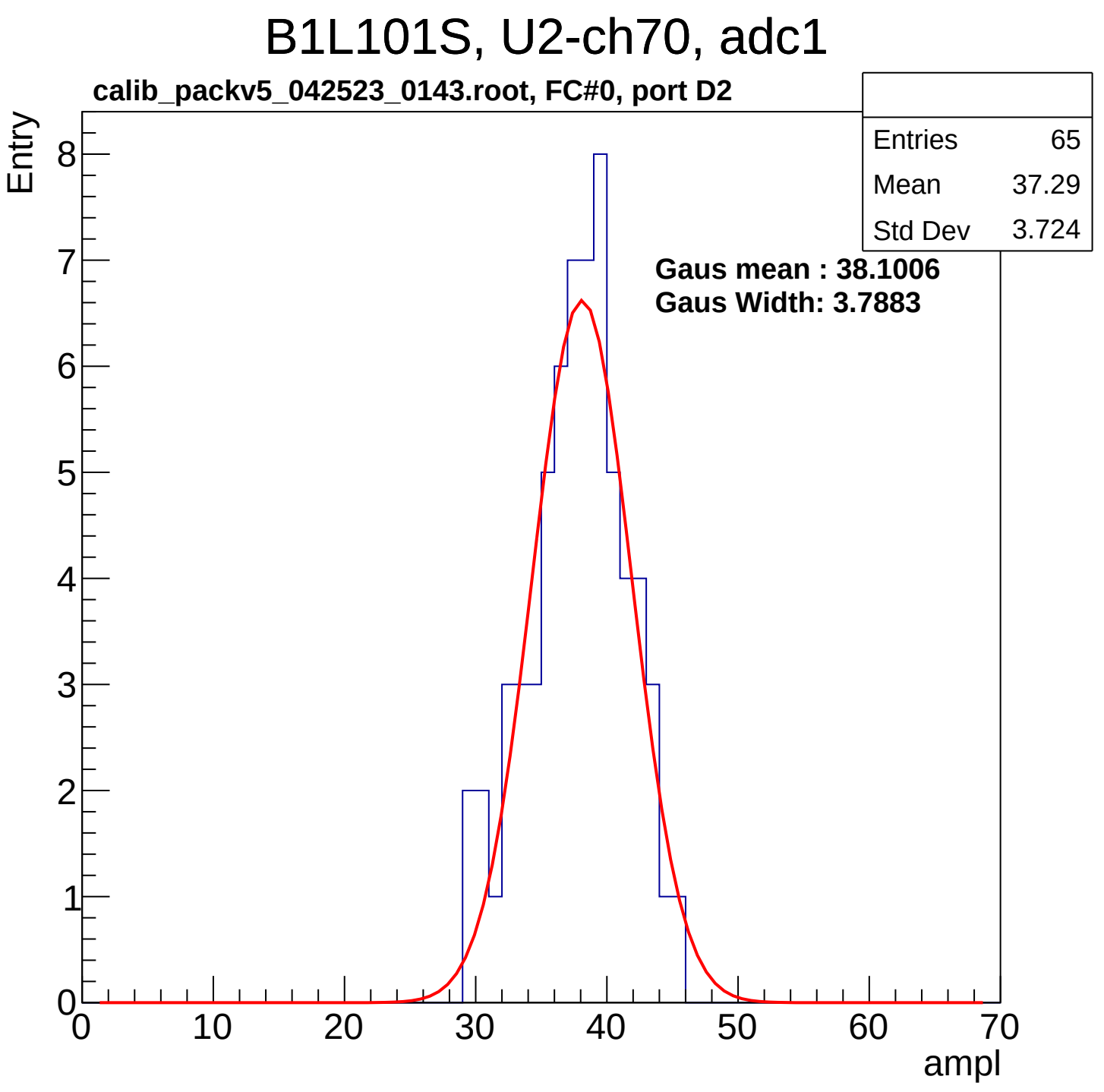

B1L101S, U2-ch69, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 55.74
Std Dev 3.187
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

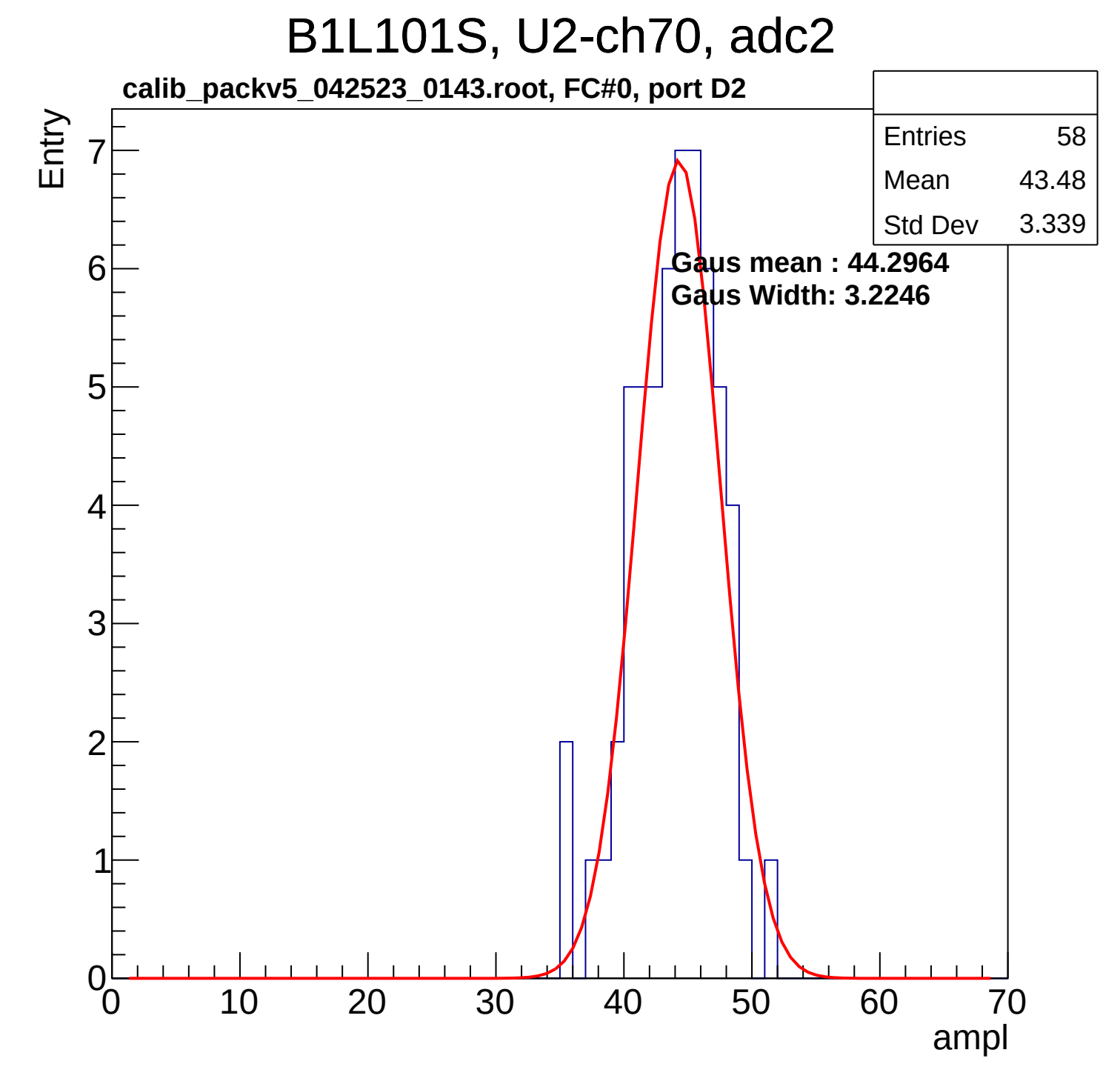

B1L101S, U2-ch69, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 44
Mean 59.68
Std Dev 2.502
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

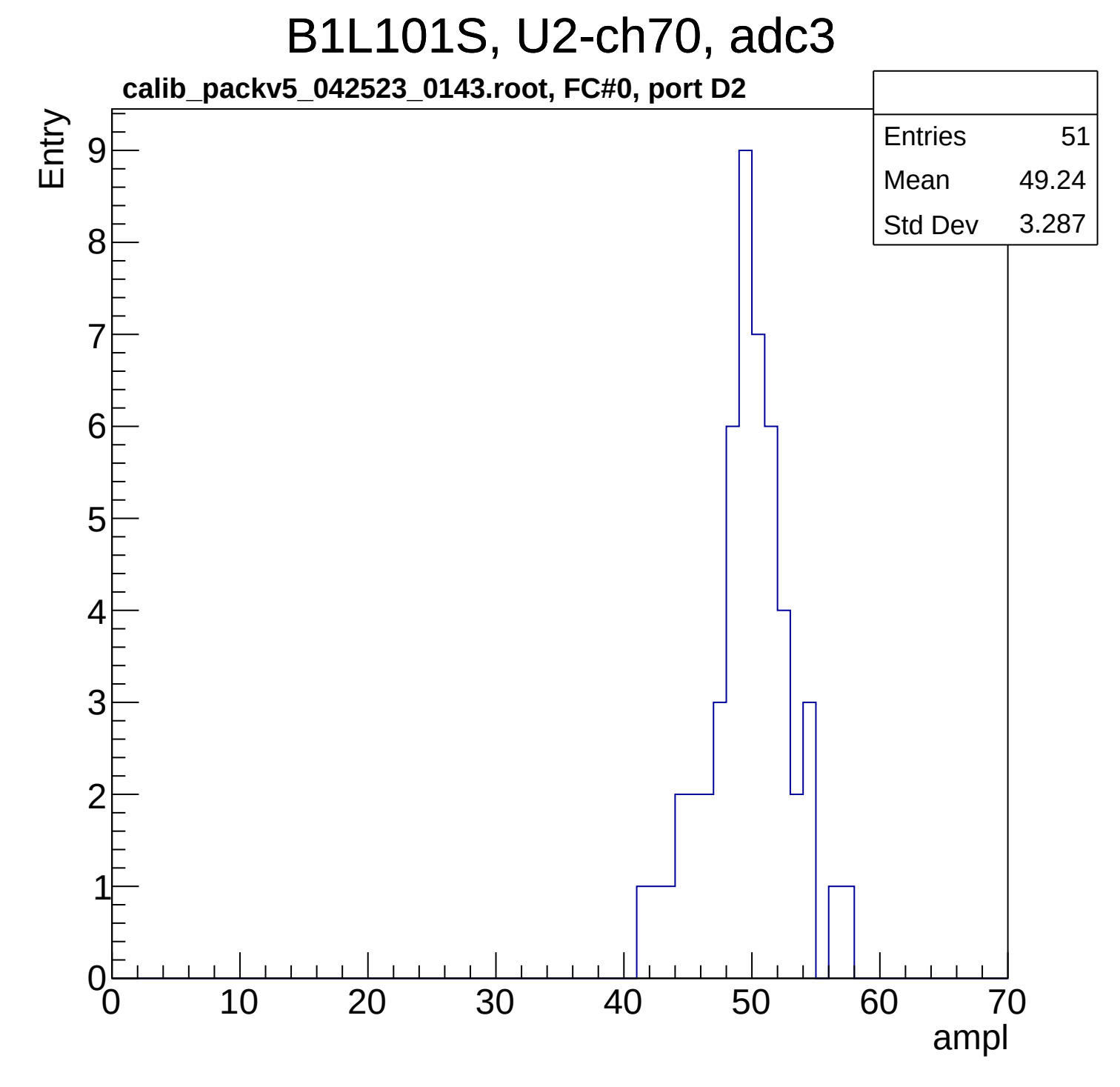

B1L101S, U2-ch69, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 55
Std Dev 19.5
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

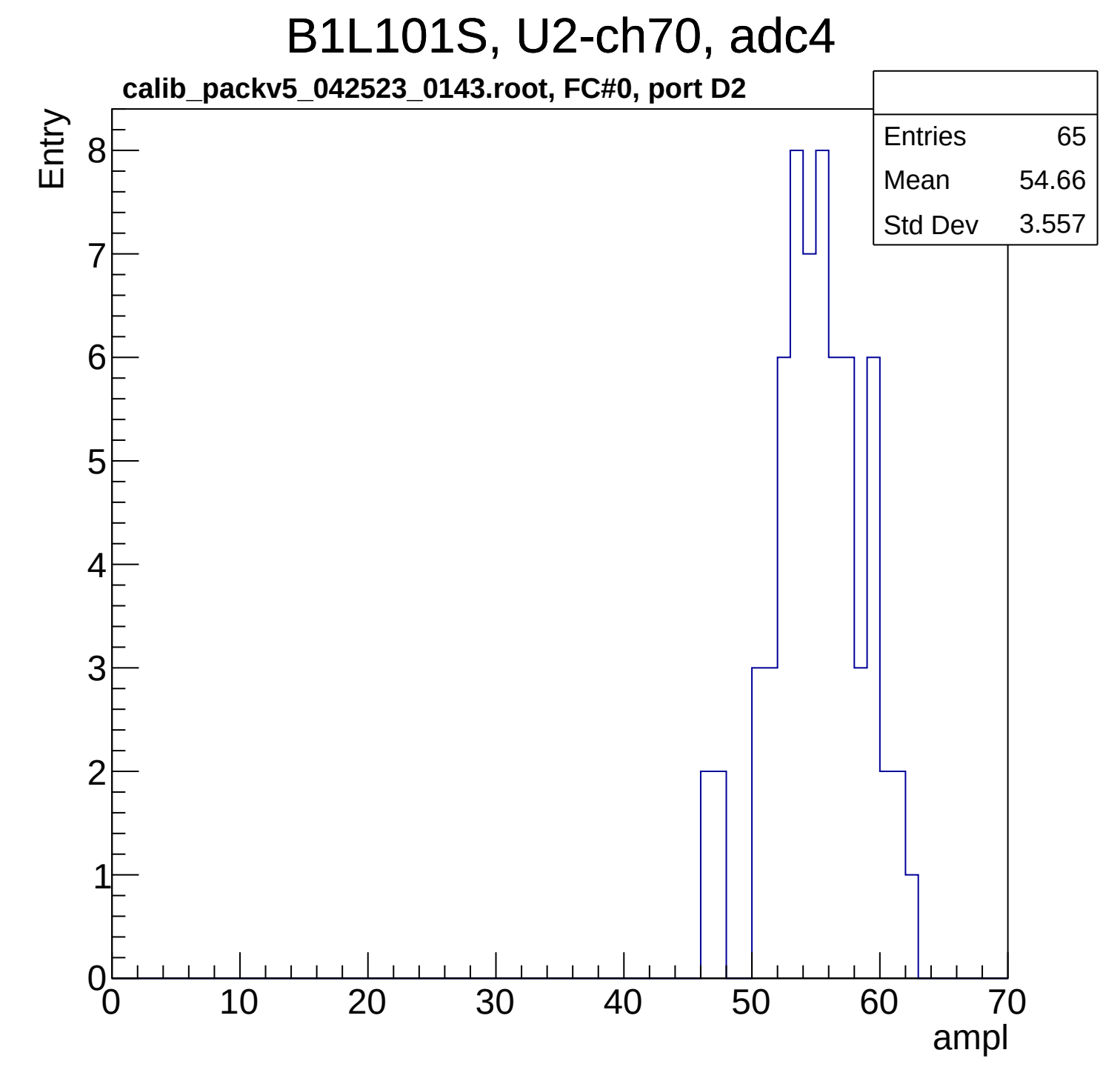

B1L101S, U2-ch69, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

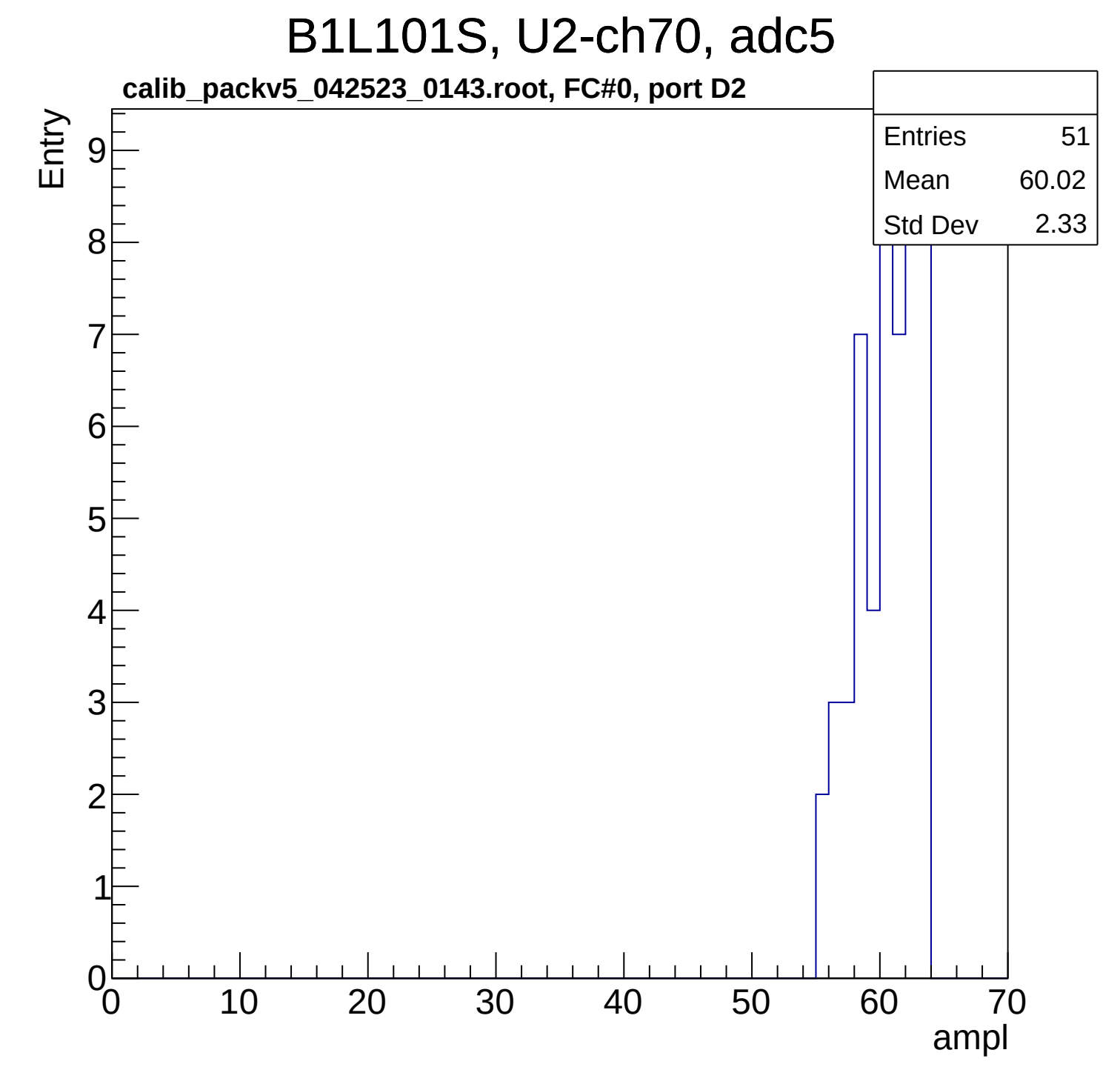

B1L101S, U2-ch70, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 30.66
Std Dev 3.604
Gaus mean : 31.3301
Gaus Width: 4.0209
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

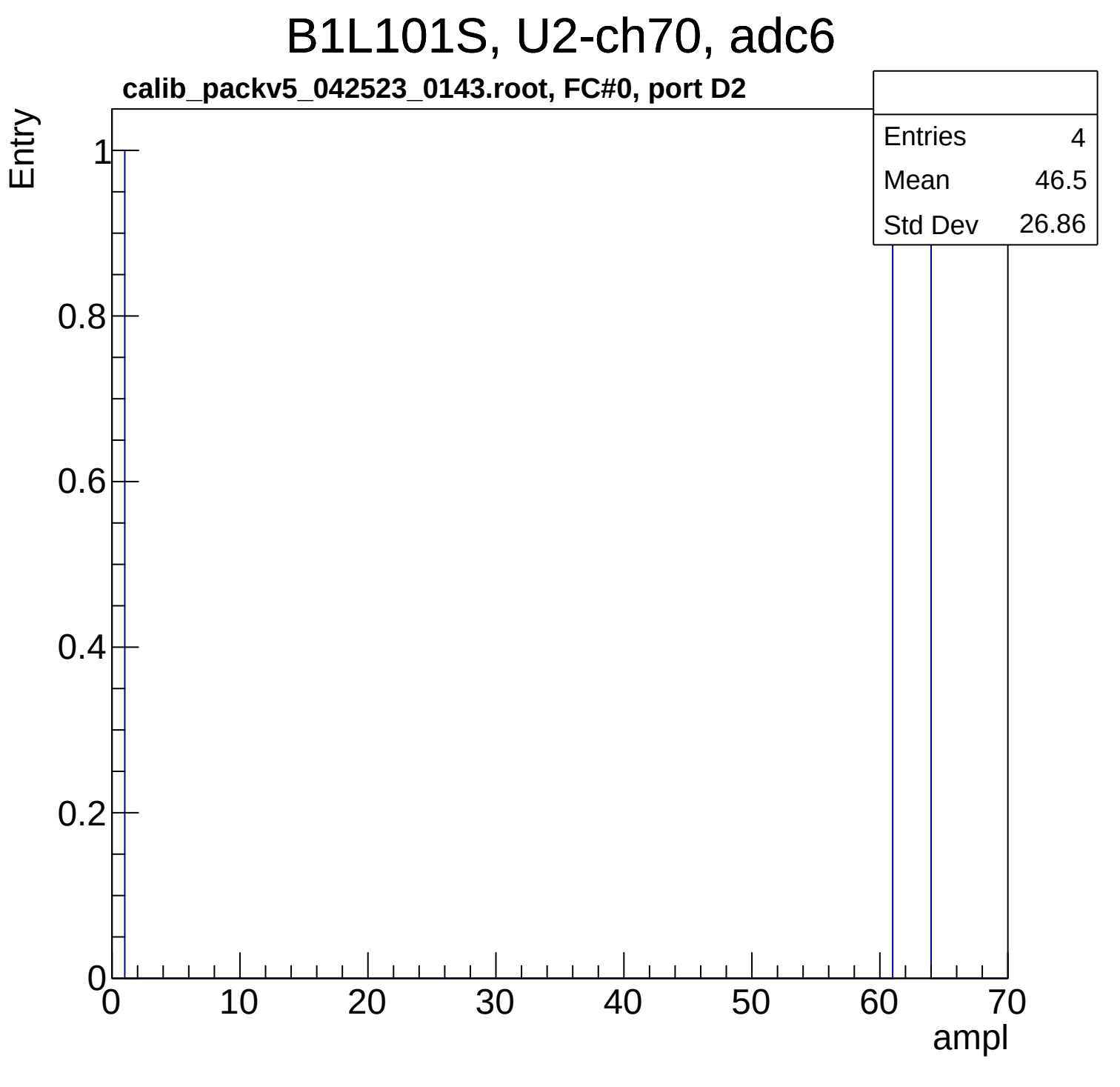

B1L101S, U2-ch70, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 37.29
Std Dev 3.724
Gaus mean : 38.1006
Gaus Width: 3.7883
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

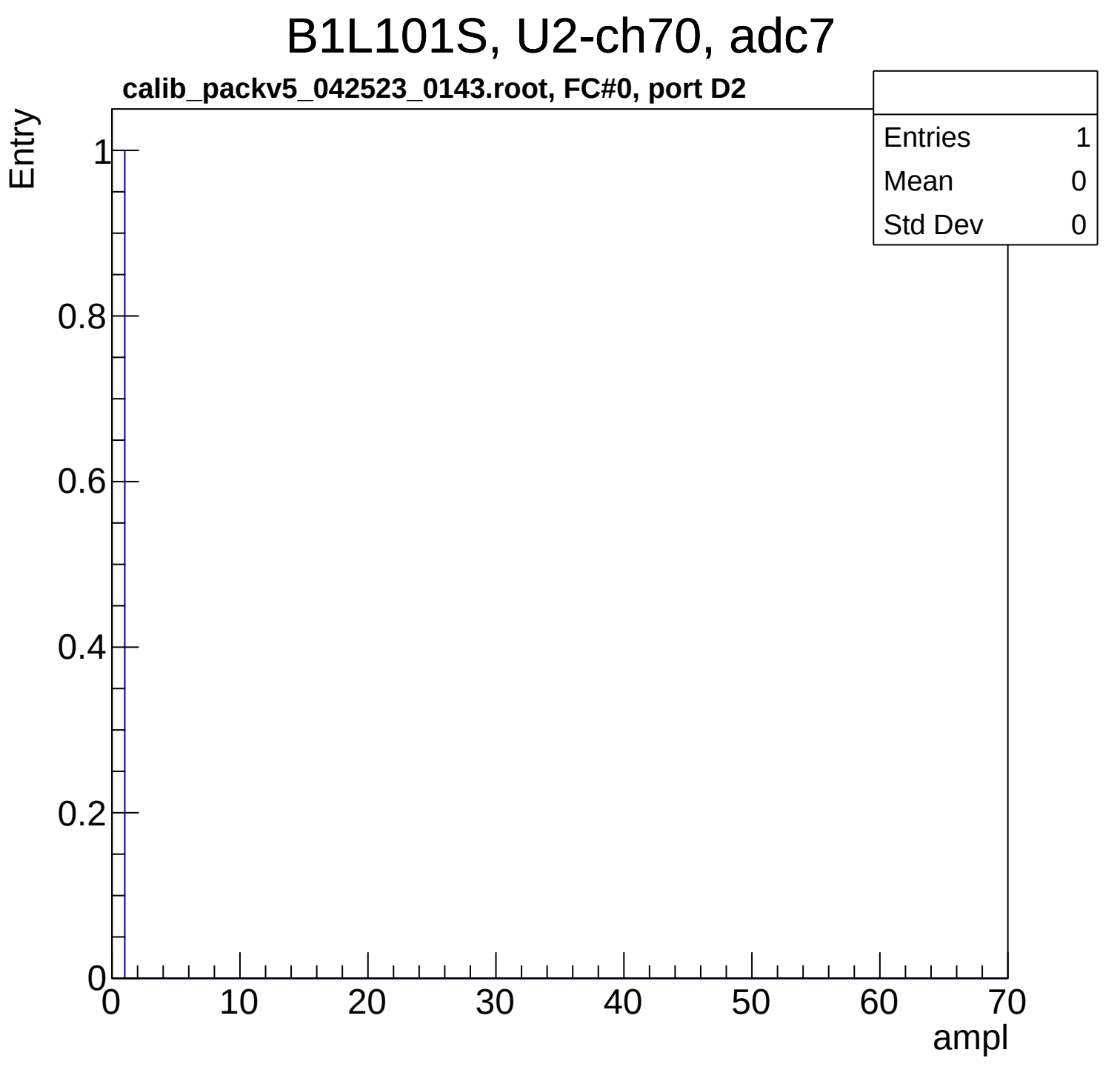

B1L101S, U2-ch70, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 43.48
Std Dev 3.339
Gaus mean : 44.2964
Gaus Width: 3.2246
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

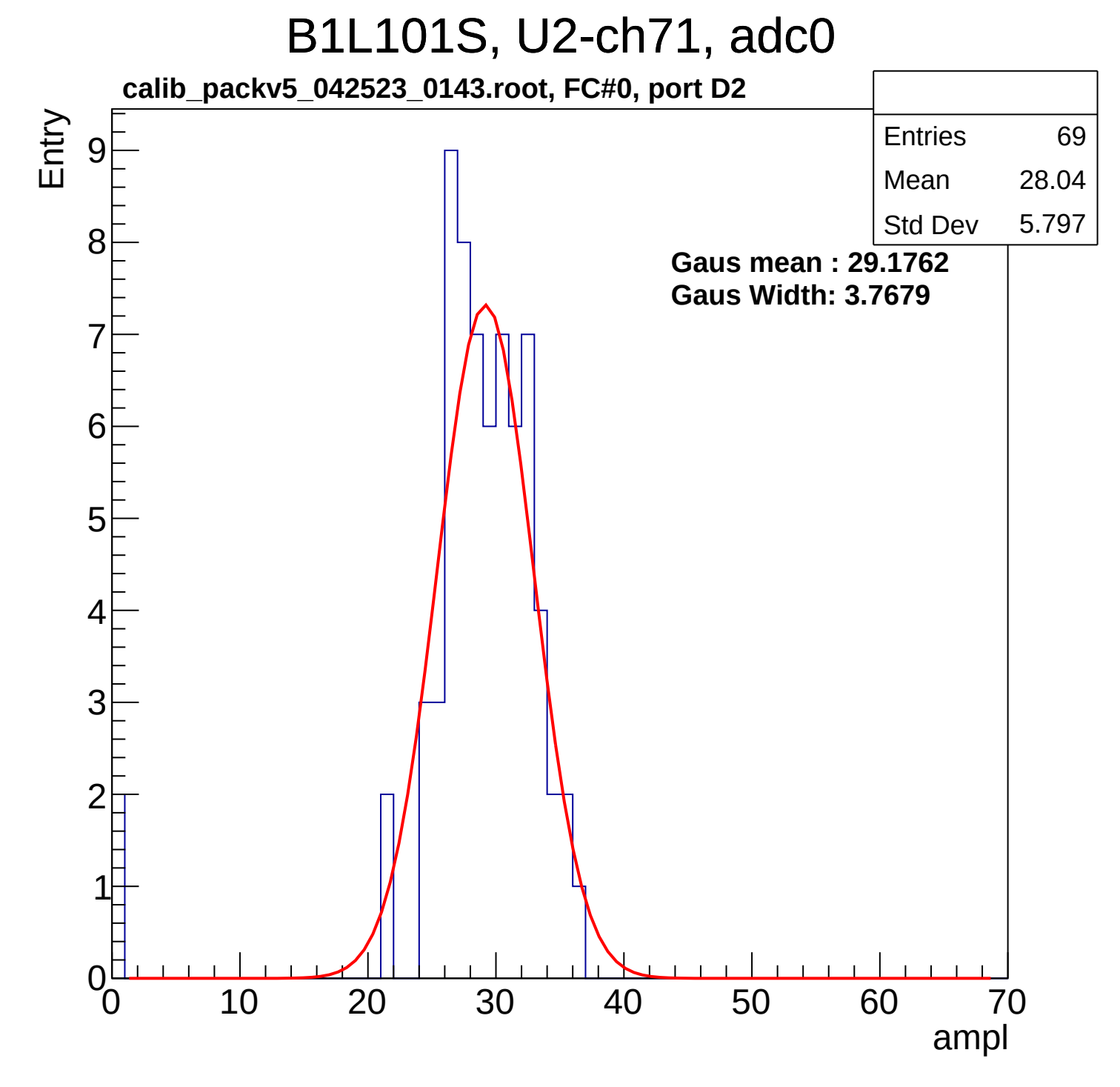

B1L101S, U2-ch70, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 49.24
Std Dev 3.287
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

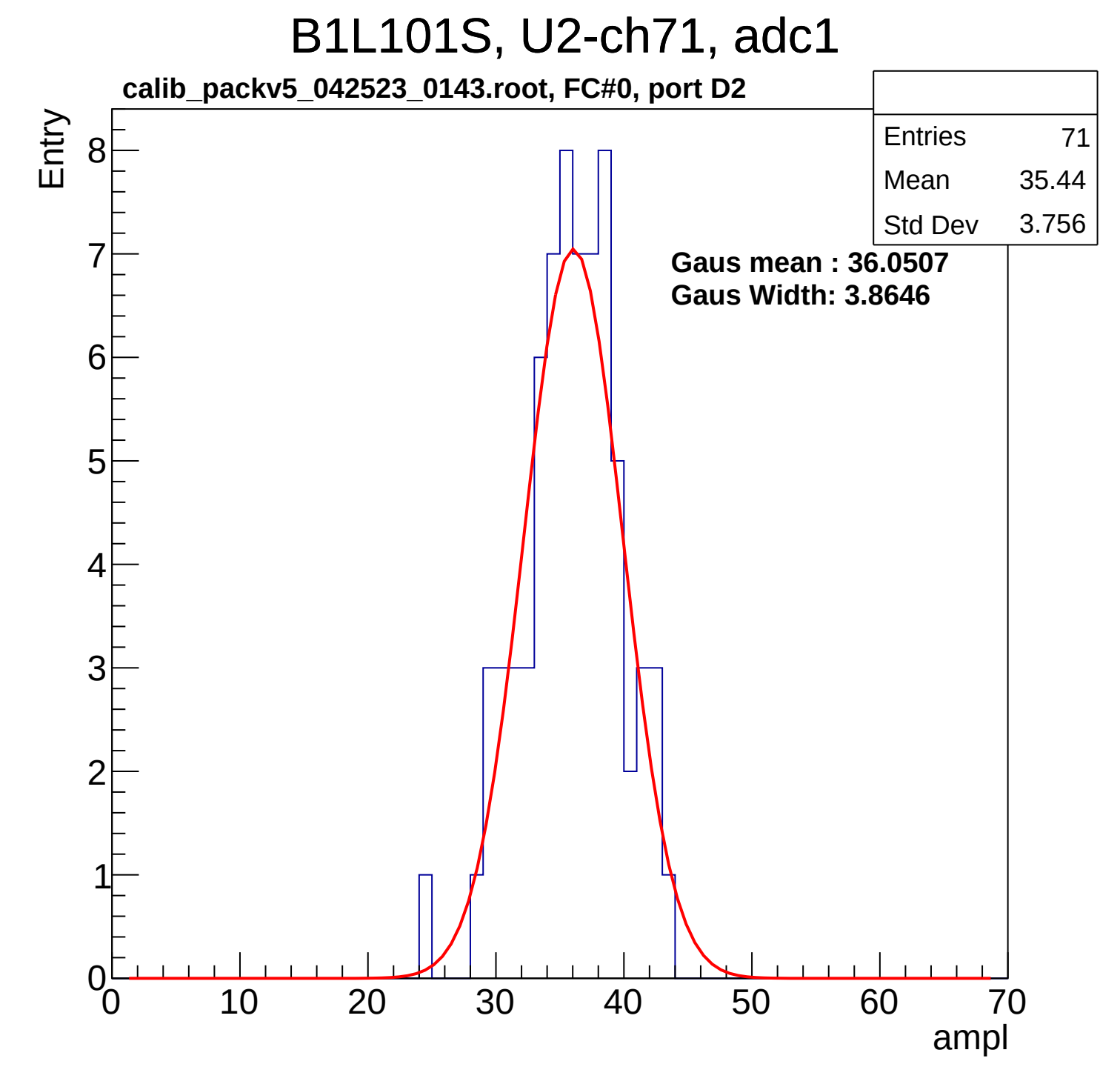

B1L101S, U2-ch70, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 54.66
Std Dev 3.557
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

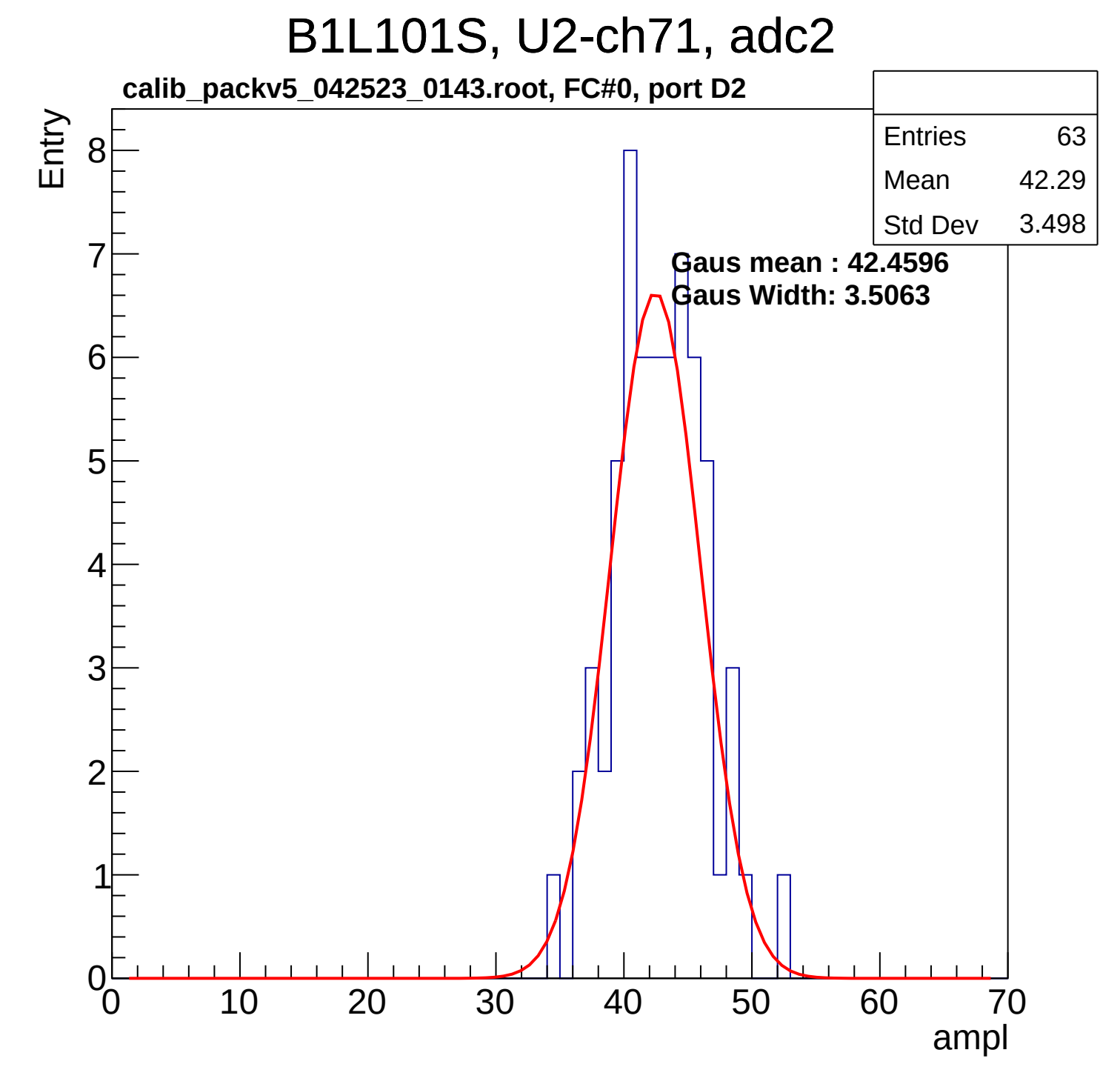

B1L101S, U2-ch70, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 60.02
Std Dev 2.33
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

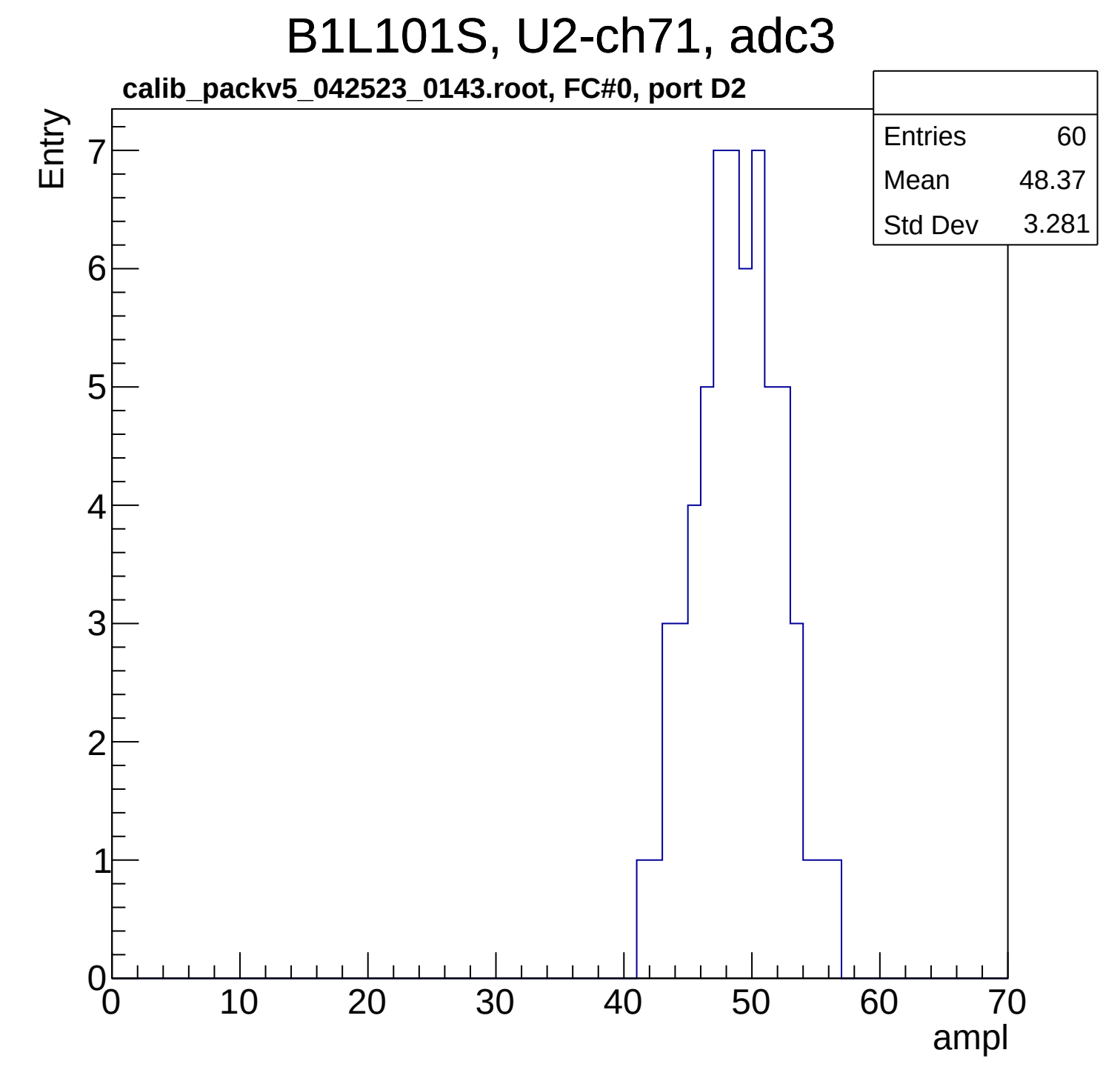

B1L101S, U2-ch70, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 46.5
Std Dev 26.86
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

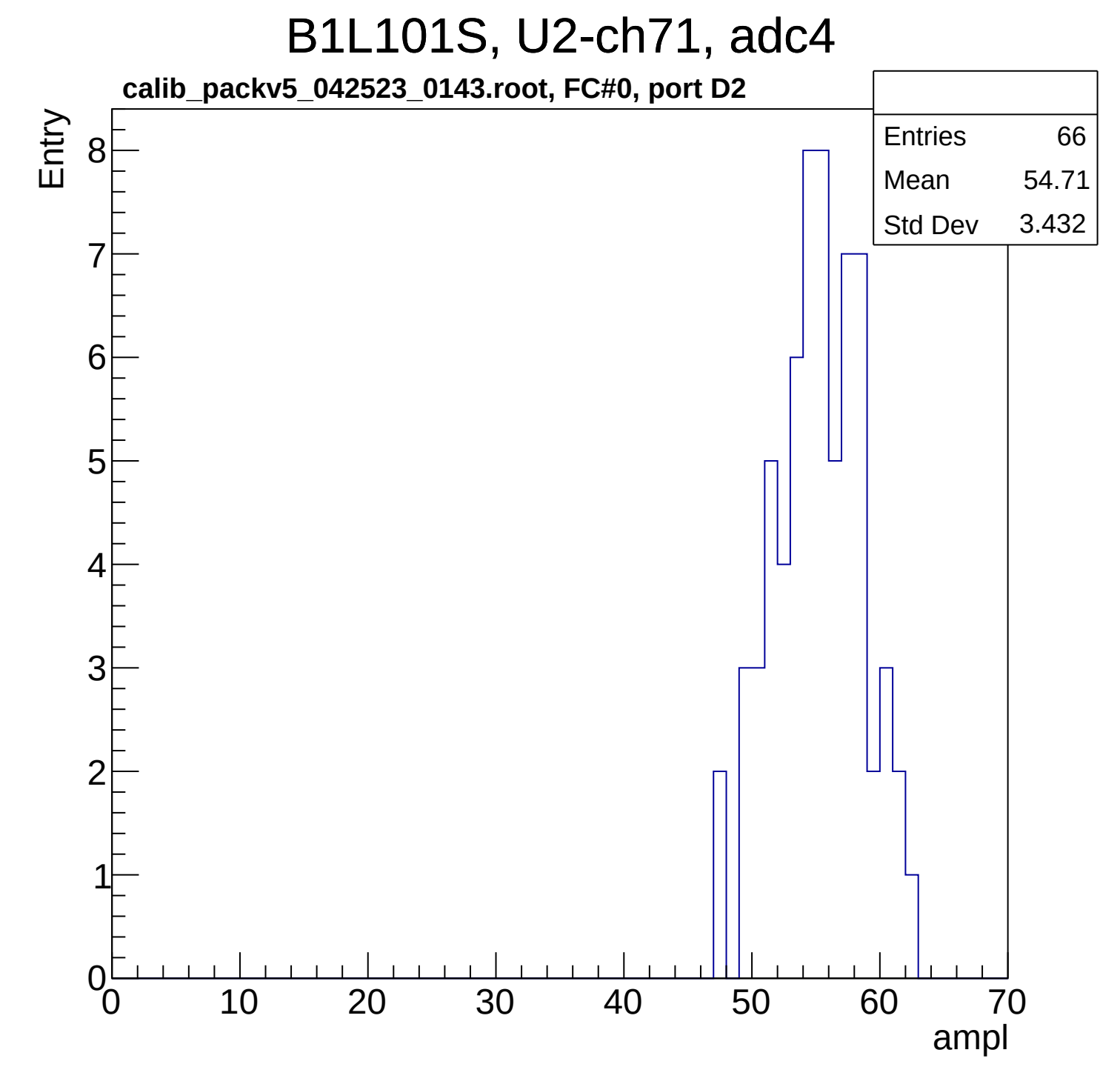

B1L101S, U2-ch70, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

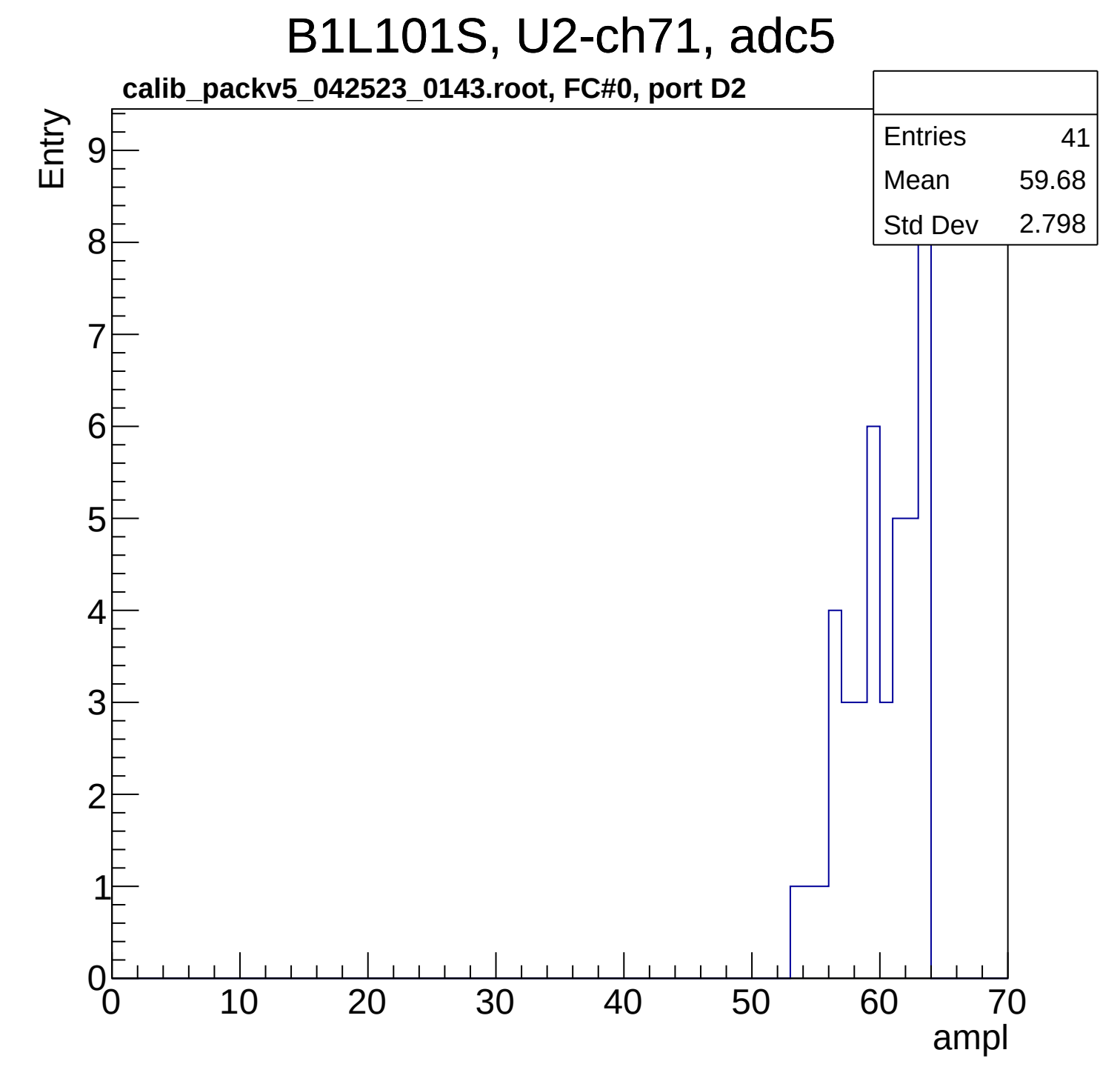

B1L101S, U2-ch71, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 28.04
Std Dev 5.797
Gaus mean : 29.1762
Gaus Width: 3.7679
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

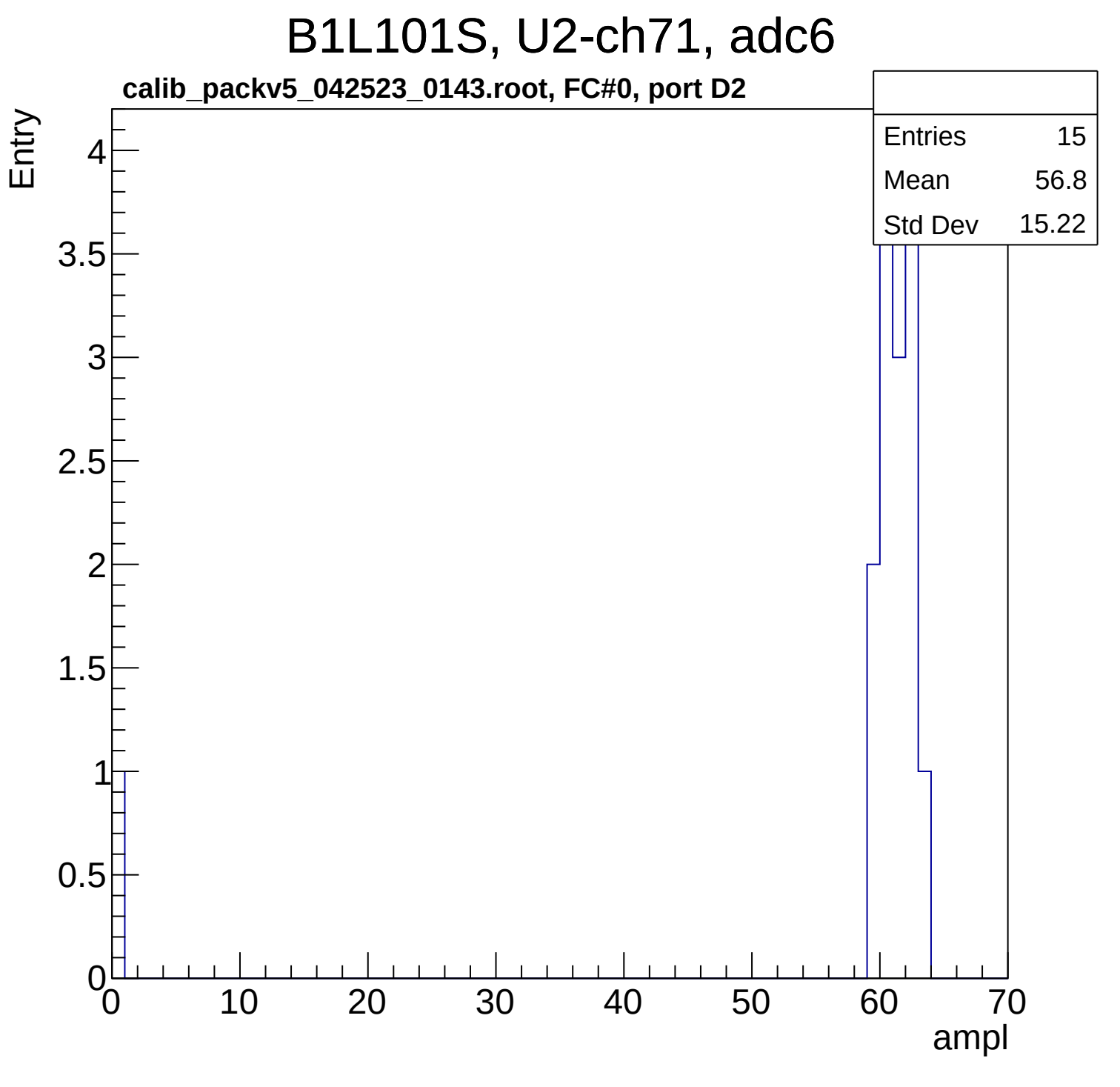

B1L101S, U2-ch71, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 35.44
Std Dev 3.756
Gaus mean : 36.0507
Gaus Width: 3.8646
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

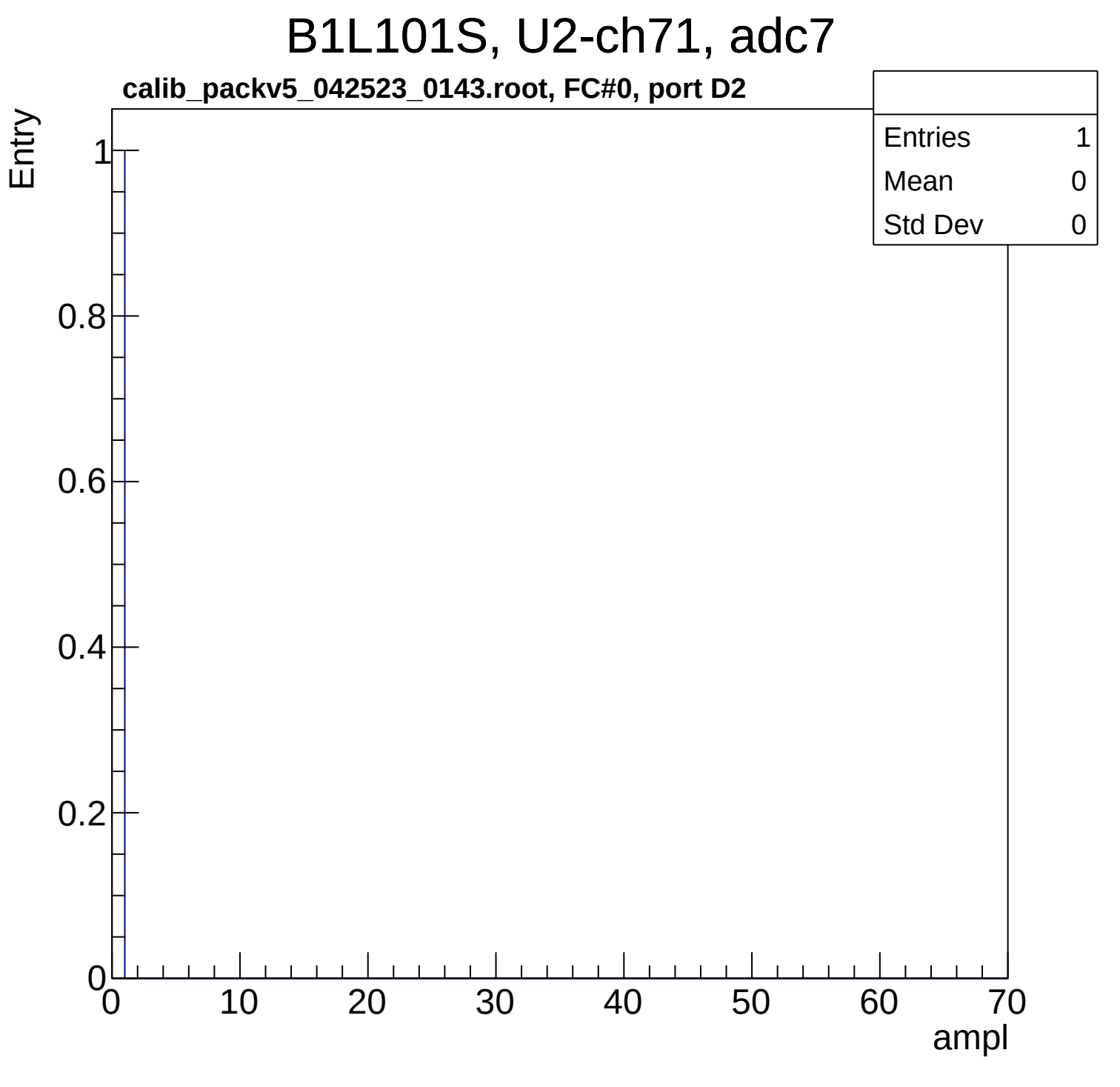

B1L101S, U2-ch71, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 42.29
Std Dev 3.498
Gaus mean : 42.4596
Gaus Width: 3.5063
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

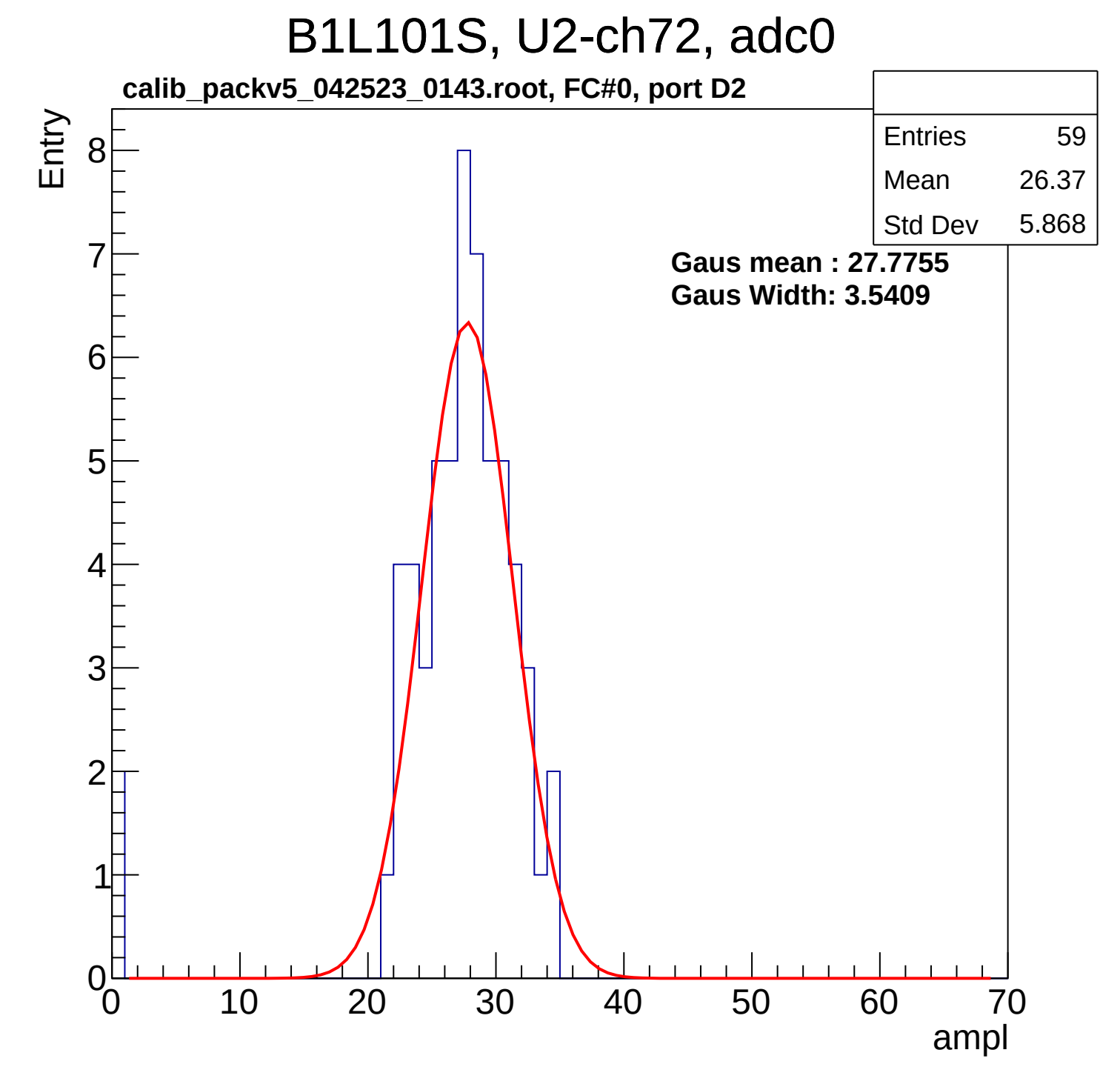

B1L101S, U2-ch71, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 48.37
Std Dev 3.281
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

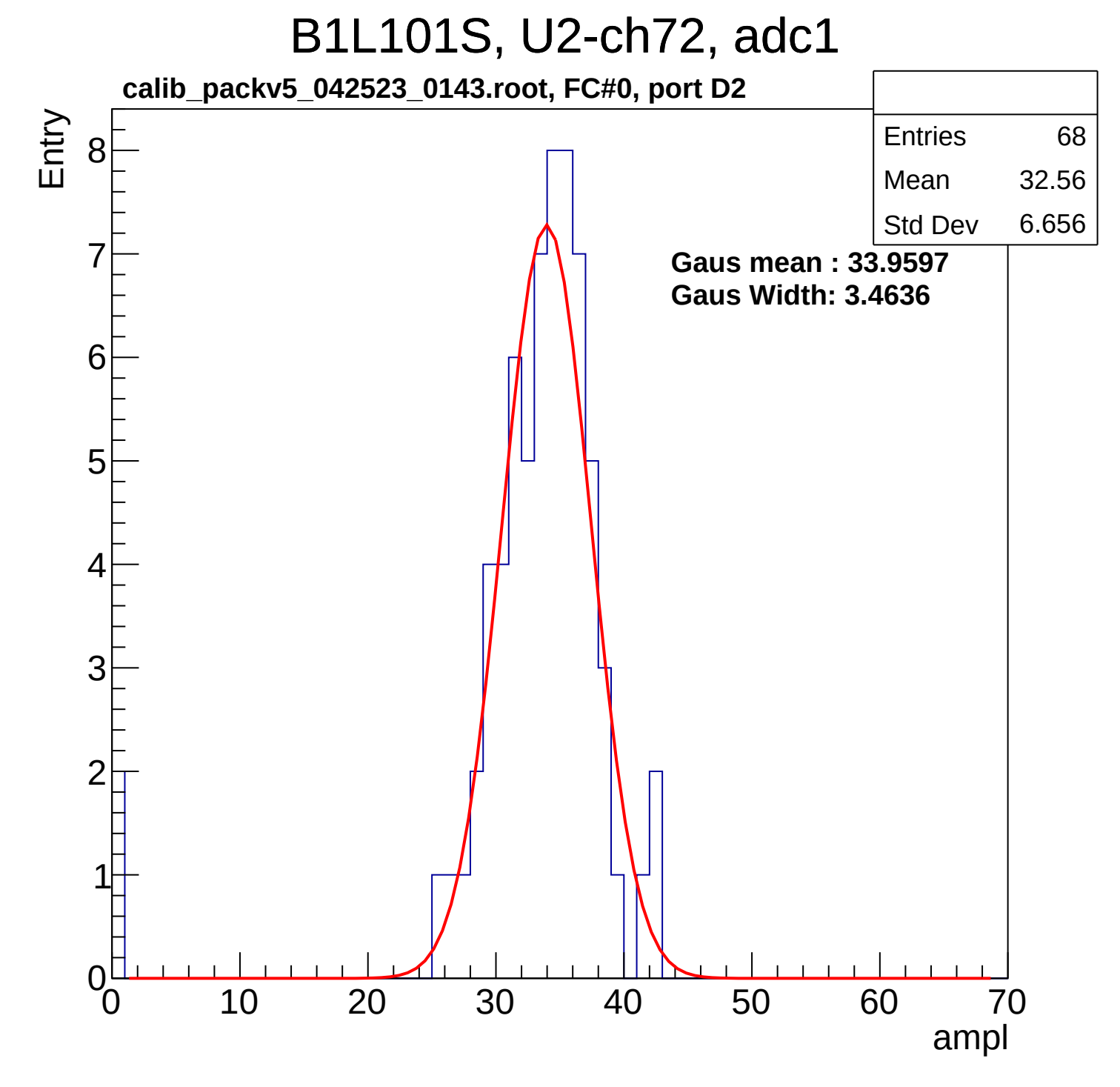

B1L101S, U2-ch71, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 54.71
Std Dev 3.432
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

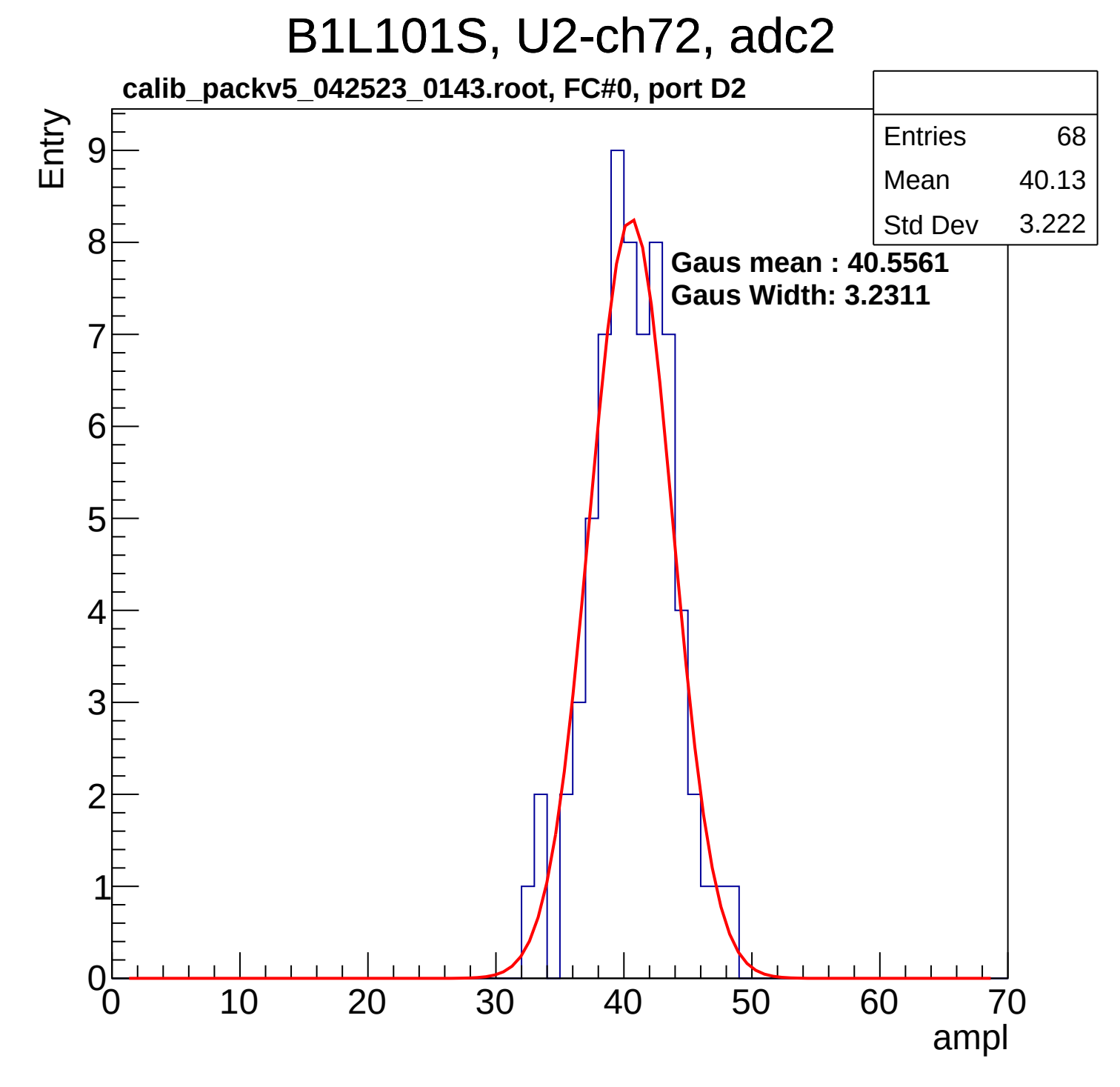

B1L101S, U2-ch71, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 41
Mean 59.68
Std Dev 2.798
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

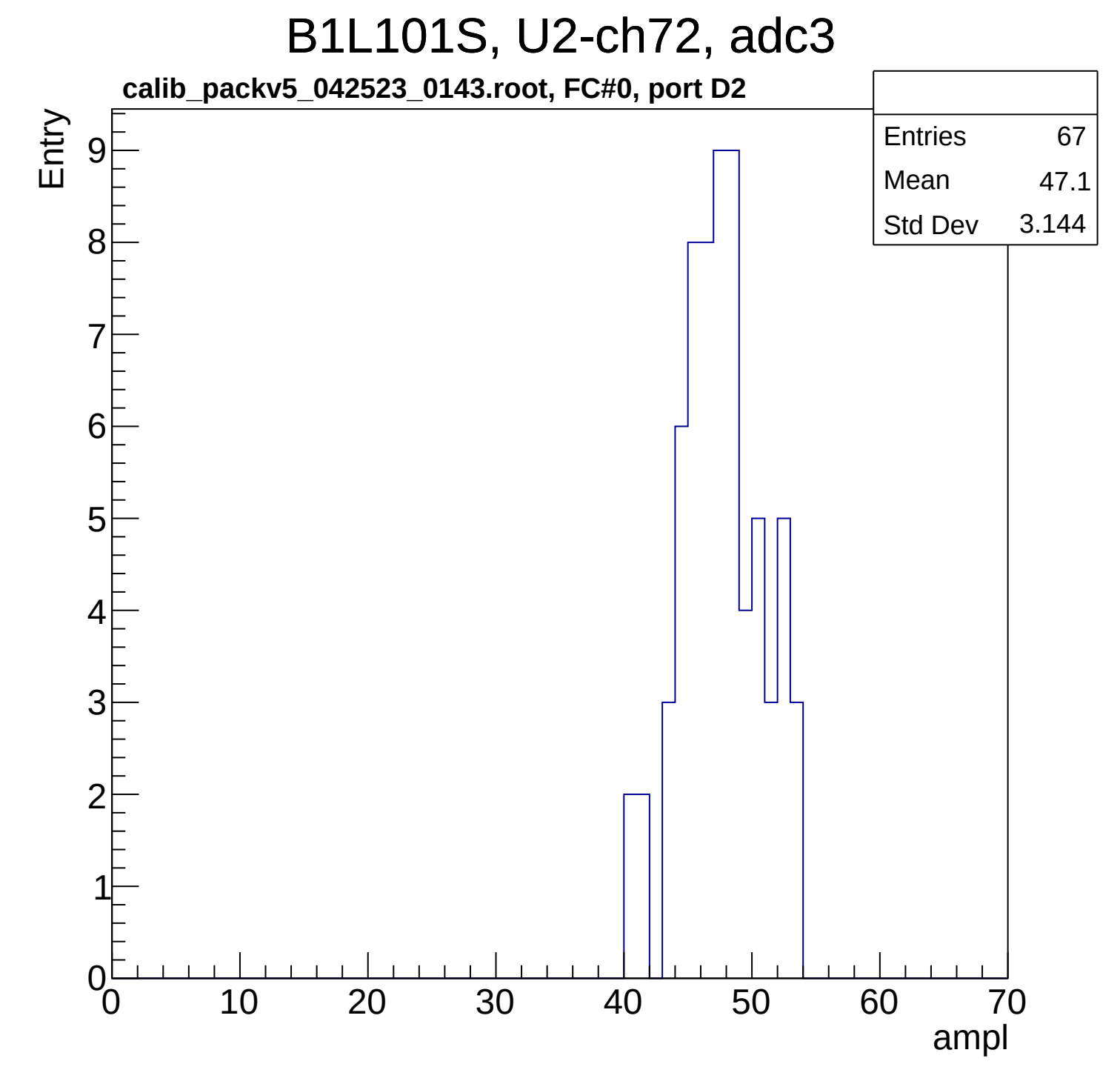

B1L101S, U2-ch71, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 15
Mean 56.8
Std Dev 15.22
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

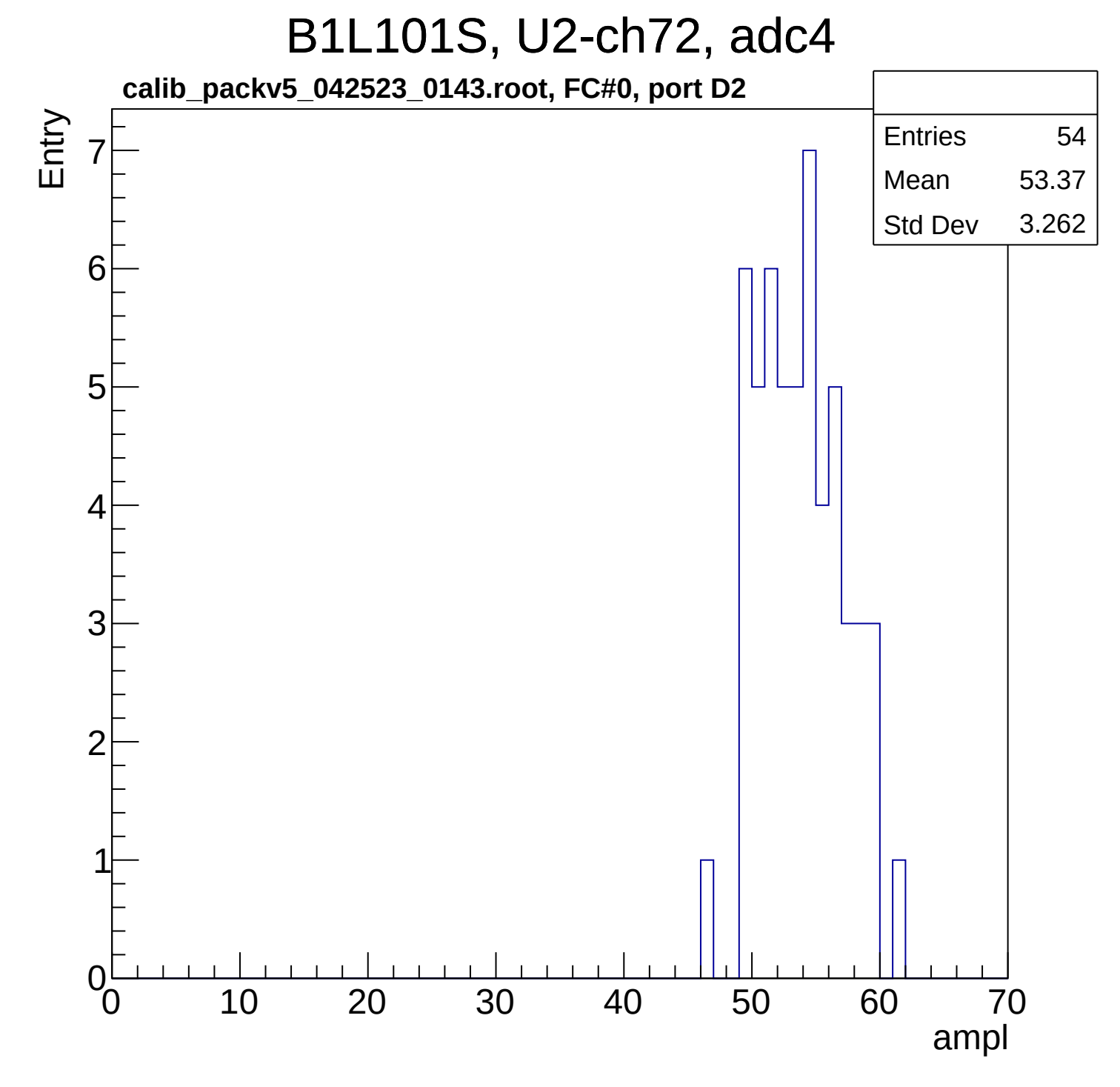

B1L101S, U2-ch71, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

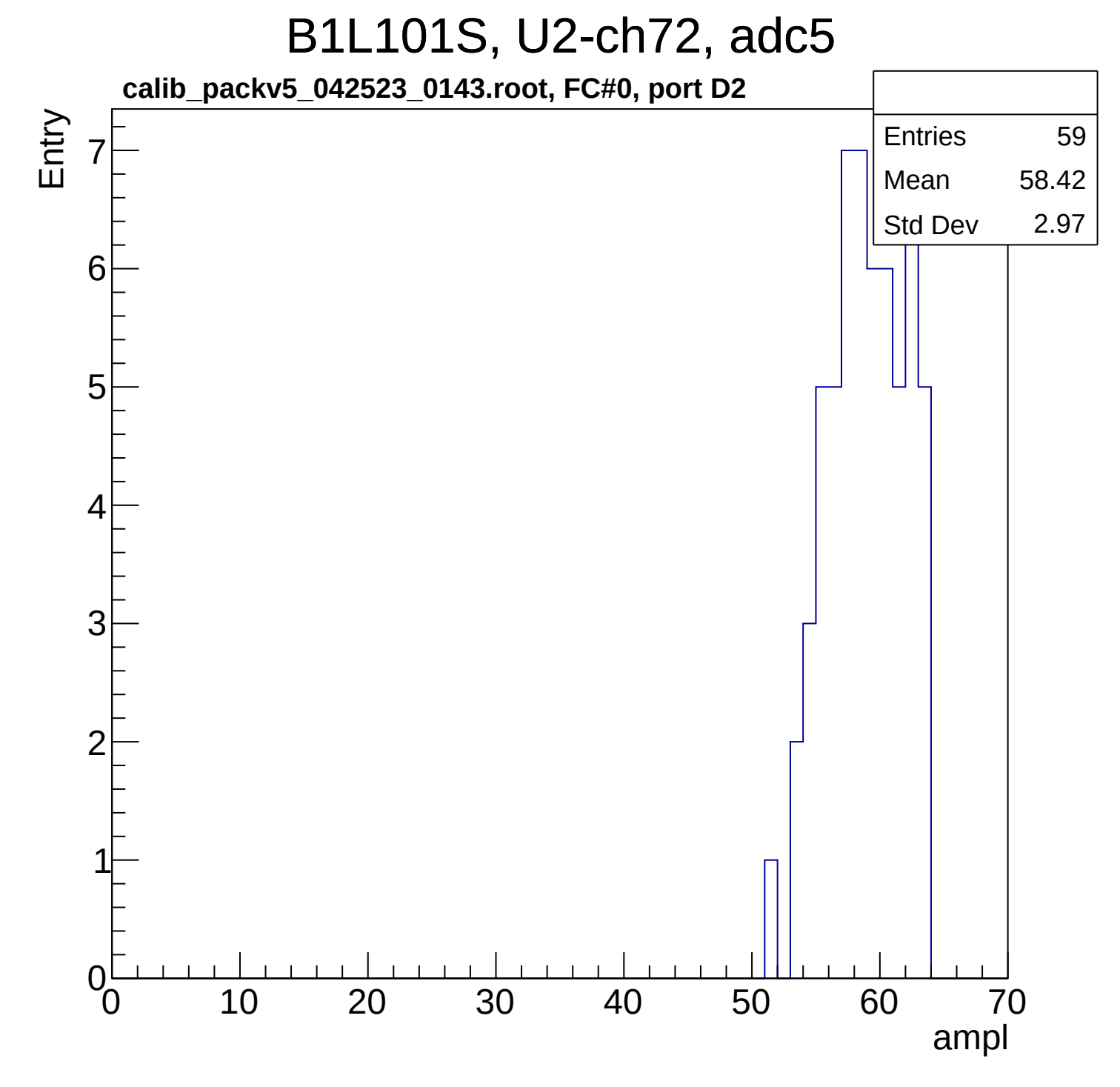

B1L101S, U2-ch72, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 26.37
Std Dev 5.868
Gaus mean : 27.7755
Gaus Width: 3.5409
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

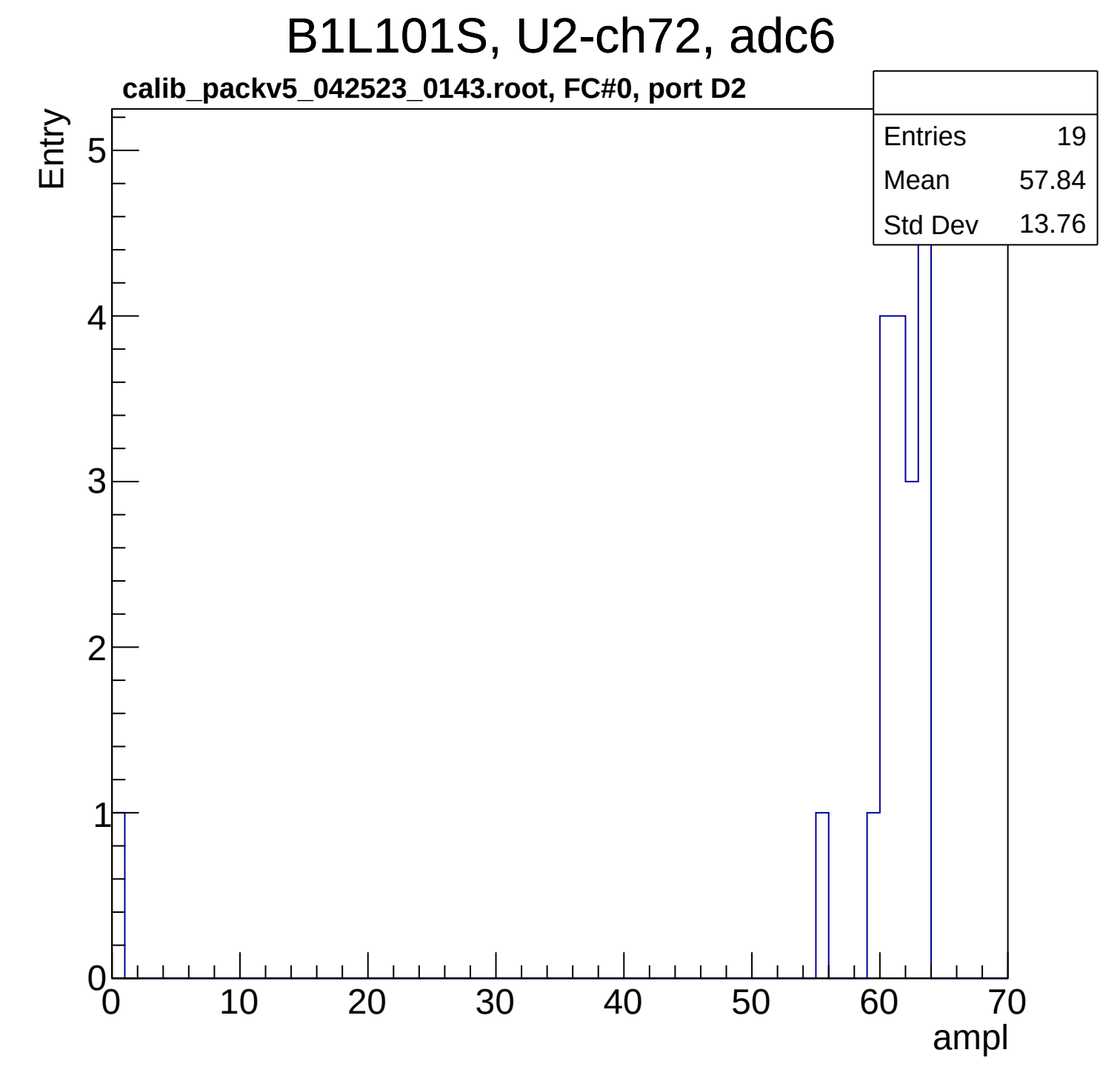

B1L101S, U2-ch72, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 32.56
Std Dev 6.656
Gaus mean : 33.9597
Gaus Width: 3.4636
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

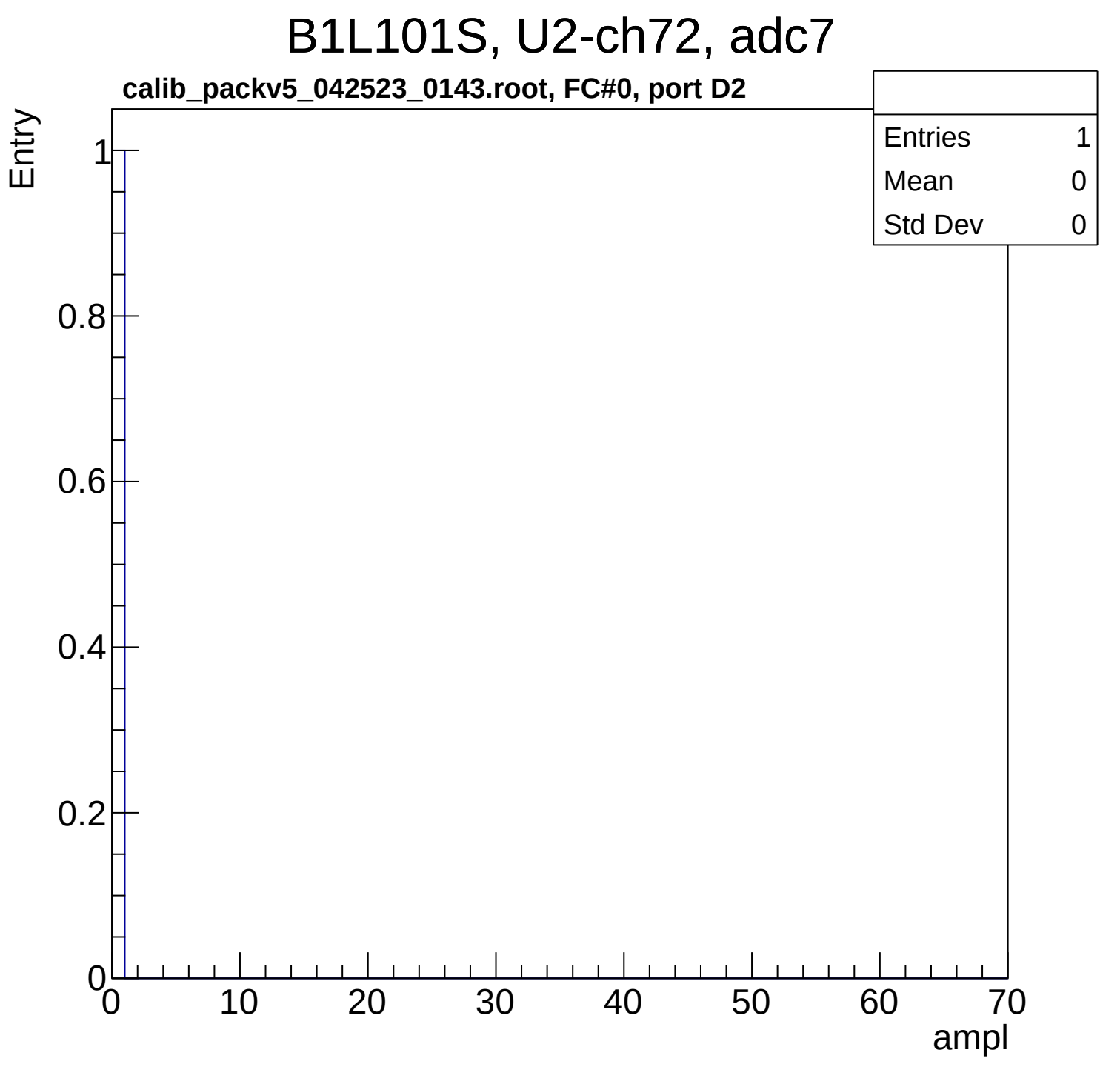

B1L101S, U2-ch72, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 40.13
Std Dev 3.222
Gaus mean : 40.5561
Gaus Width: 3.2311
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

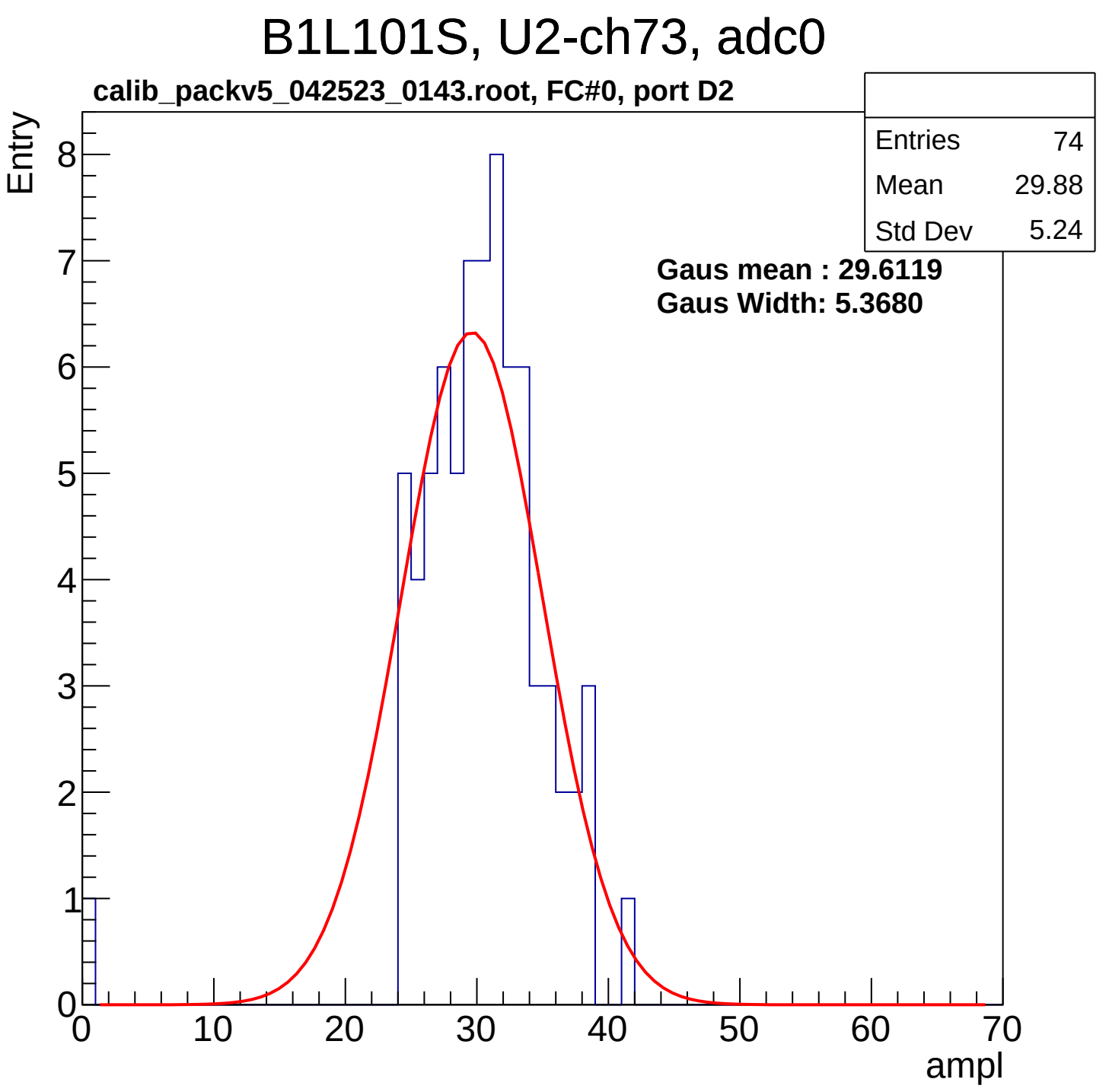

B1L101S, U2-ch72, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 47.1
Std Dev 3.144
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

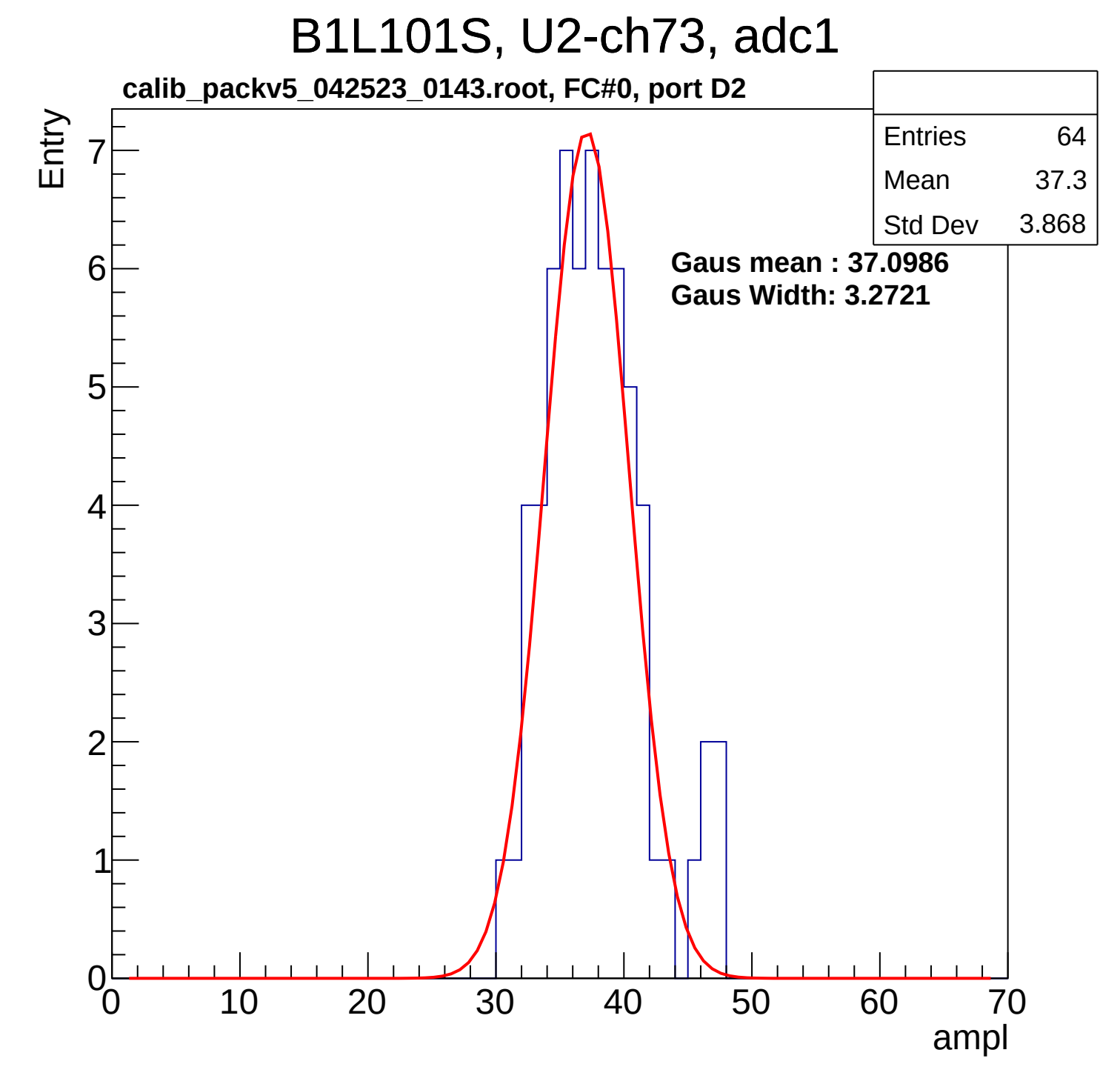

B1L101S, U2-ch72, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 53.37
Std Dev 3.262
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

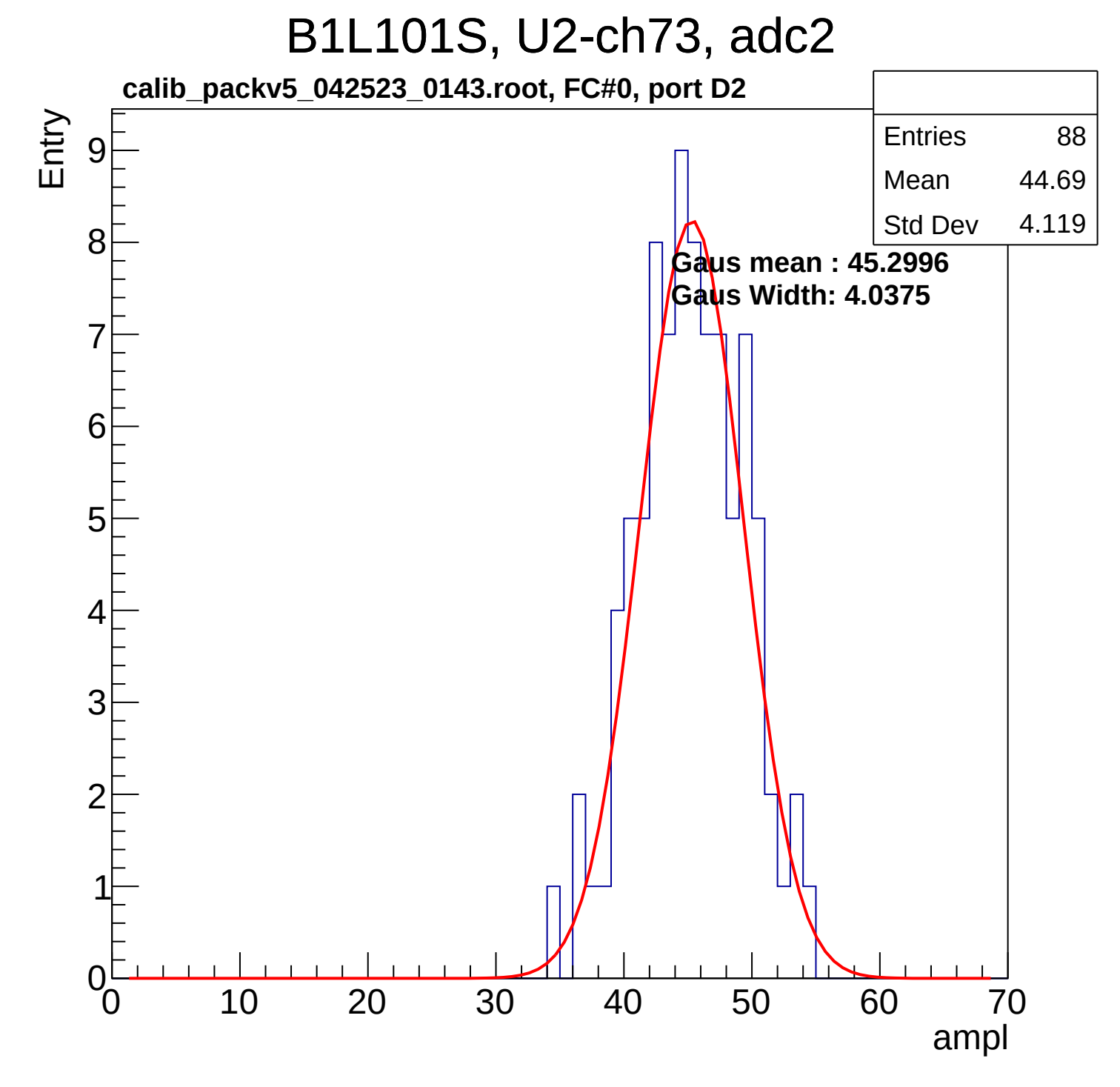

B1L101S, U2-ch72, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 58.42
Std Dev 2.97
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

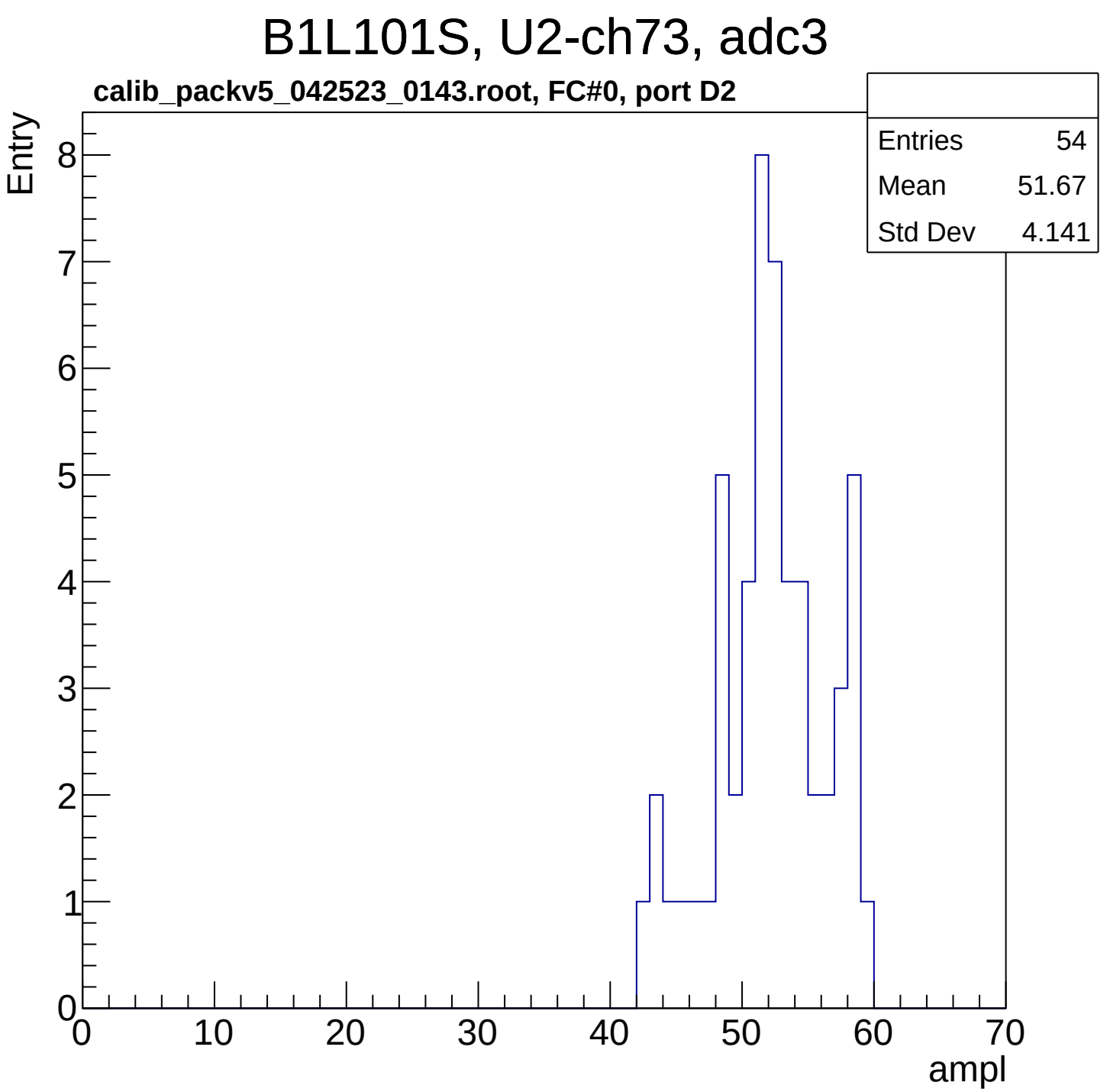

B1L101S, U2-ch72, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 19
Mean 57.84
Std Dev 13.76
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

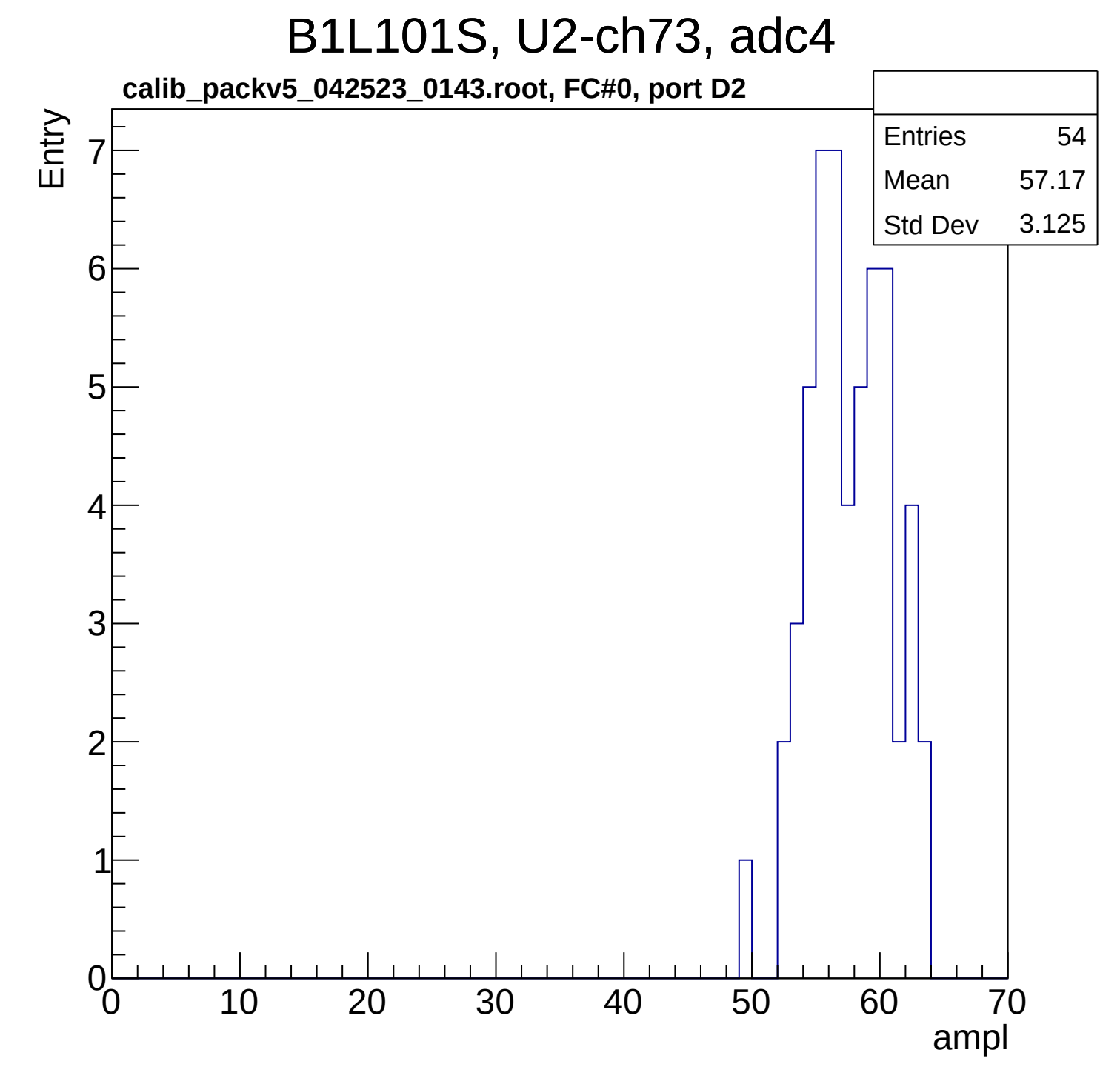

B1L101S, U2-ch72, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

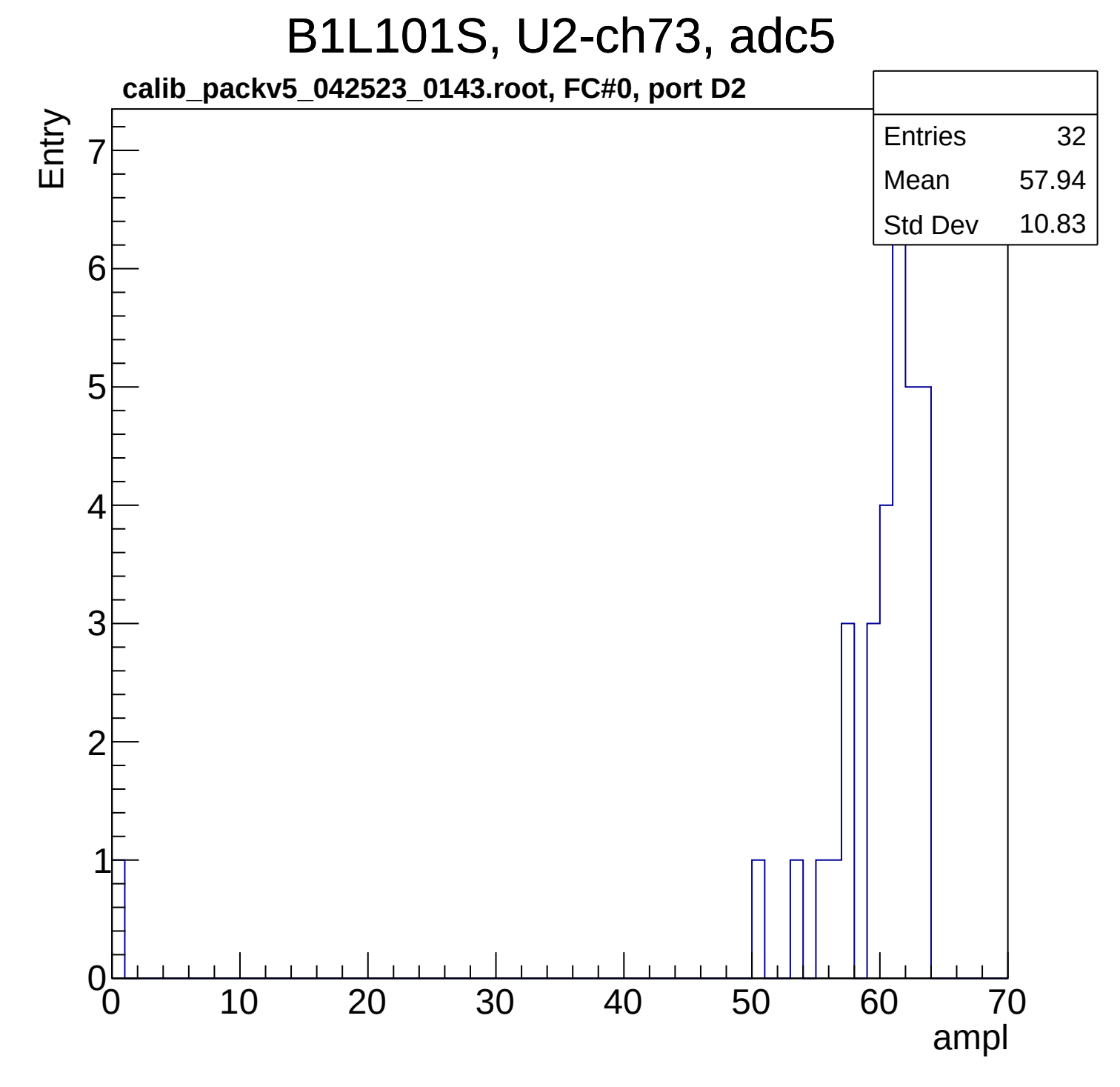

B1L101S, U2-ch73, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 29.88
Std Dev 5.24
Gaus mean : 29.6119
Gaus Width: 5.3680
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

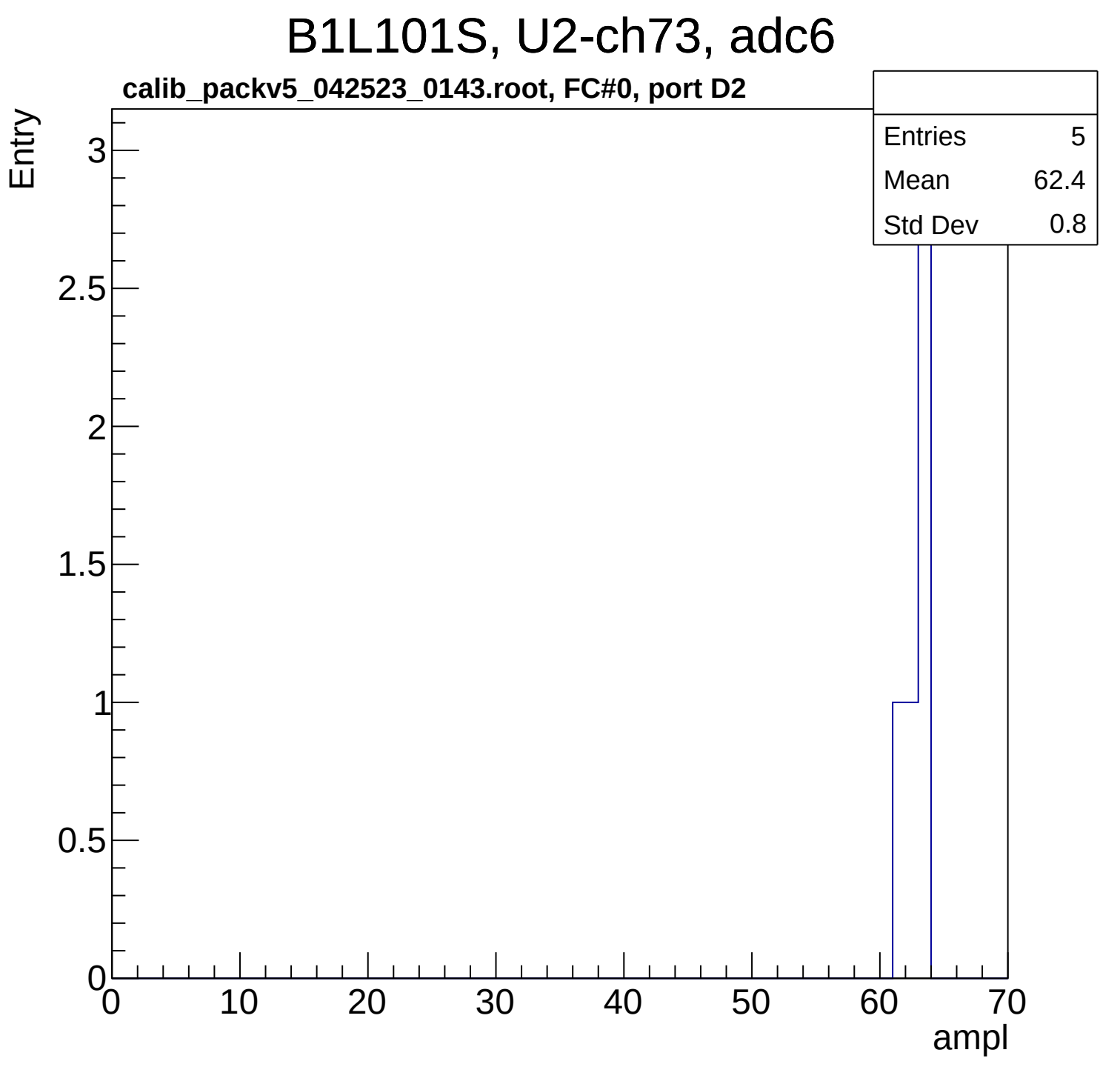

B1L101S, U2-ch73, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 37.3
Std Dev 3.868
Gaus mean : 37.0986
Gaus Width: 3.2721
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

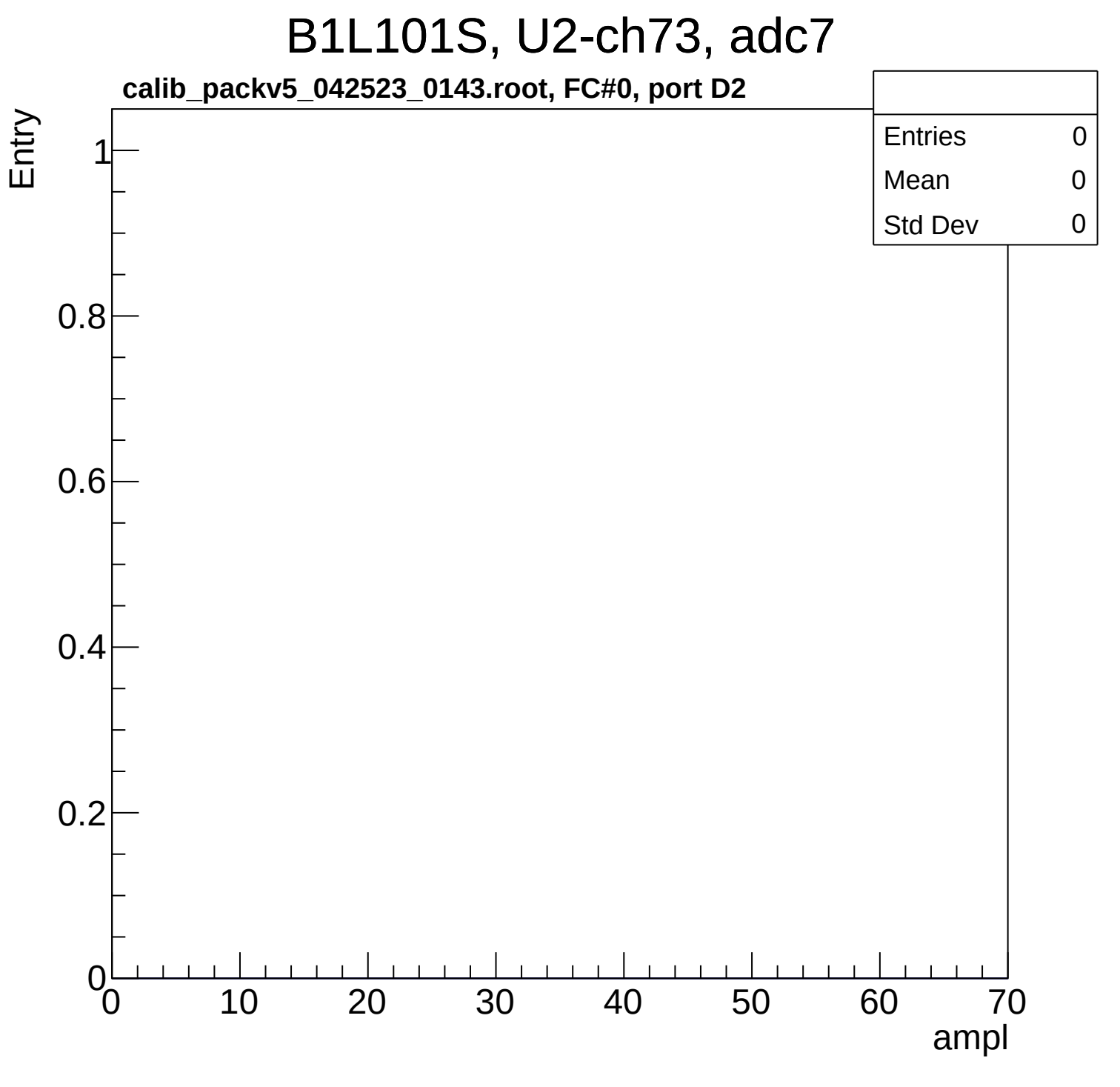

B1L101S, U2-ch73, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 88
Mean 44.69
Std Dev 4.119
Gaus mean : 45.2996
Gaus Width: 4.0375
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

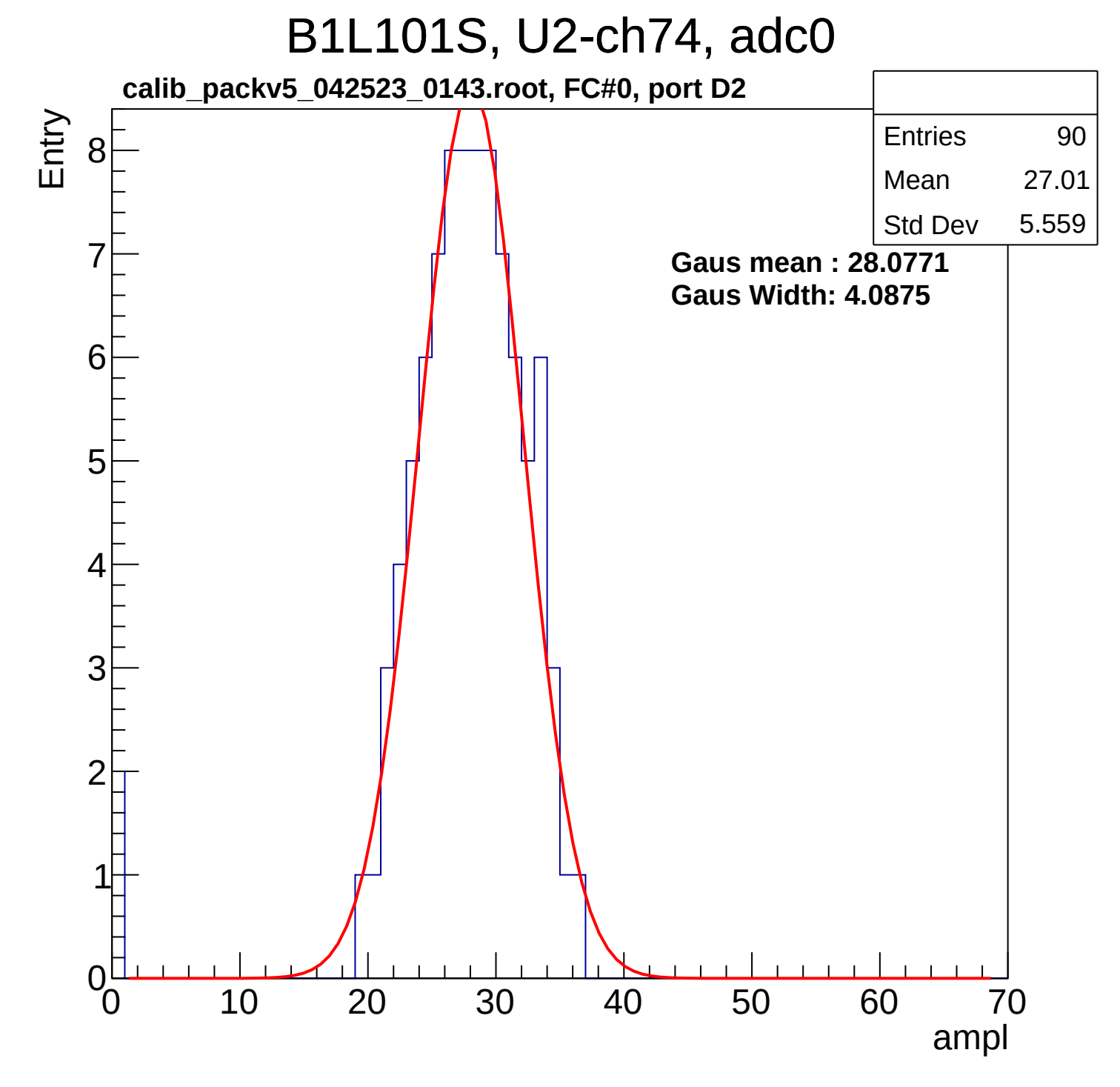

B1L101S, U2-ch73, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 51.67
Std Dev 4.141
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

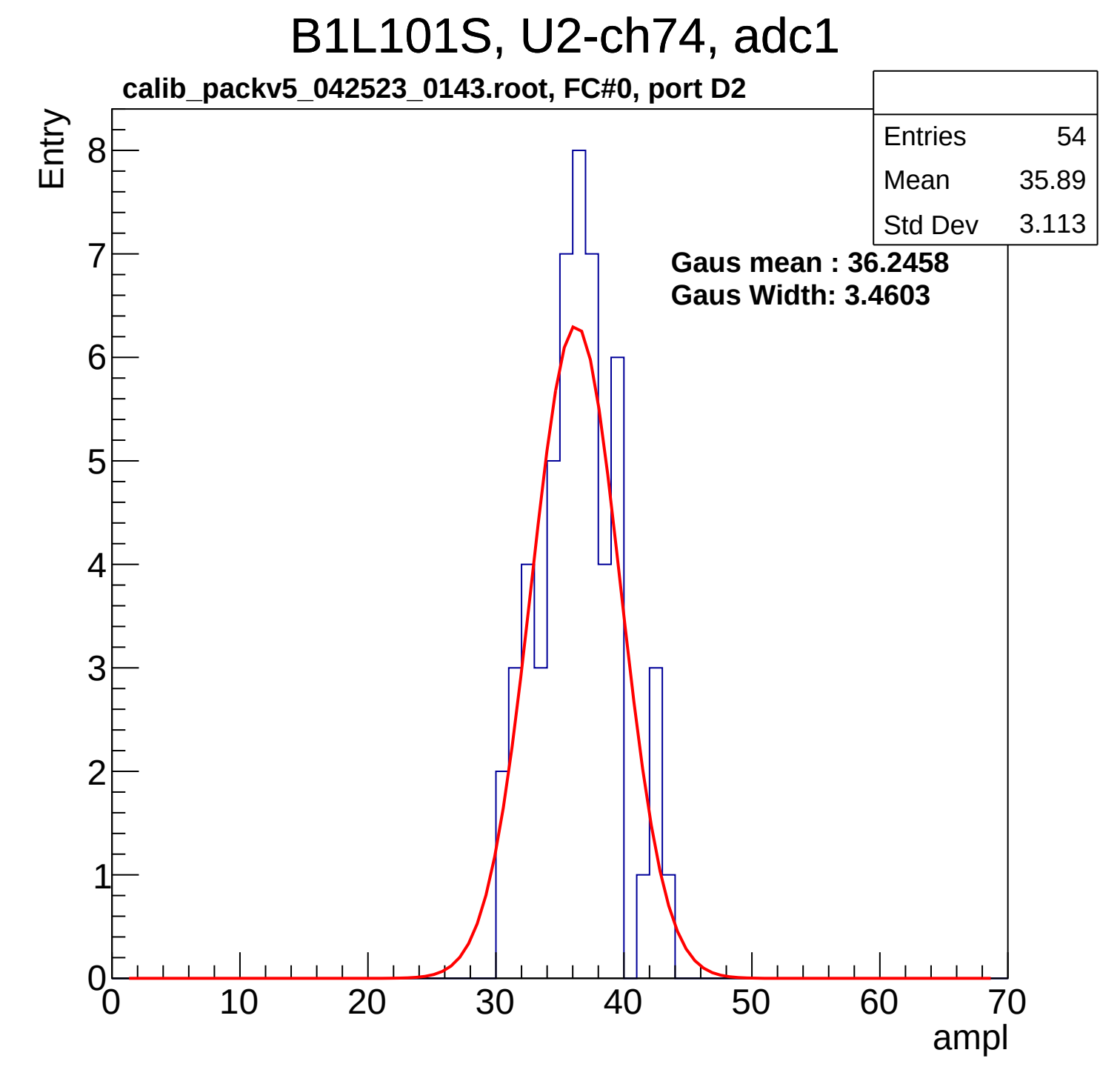

B1L101S, U2-ch73, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 57.17
Std Dev 3.125
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

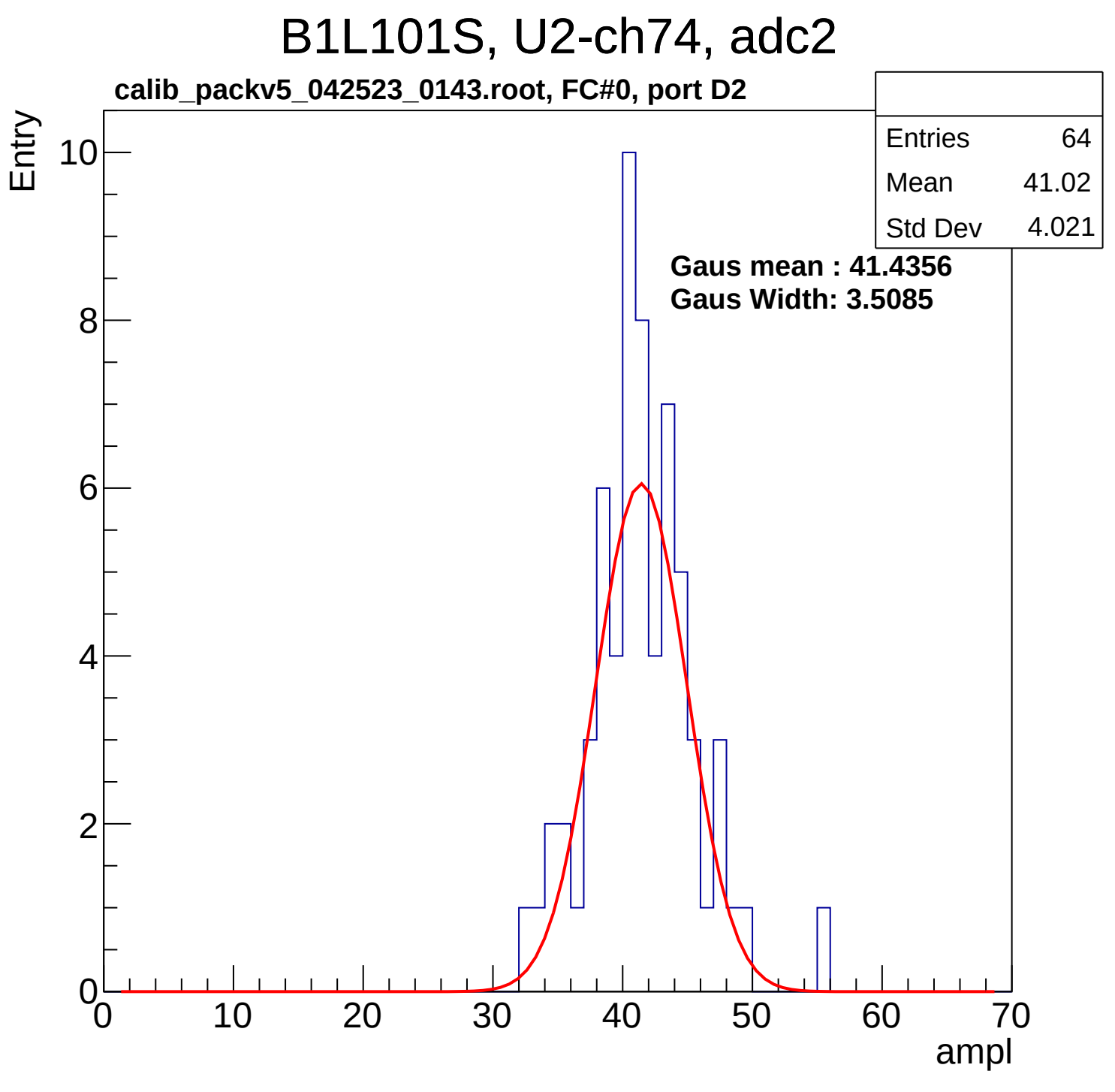

B1L101S, U2-ch73, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 32
Mean 57.94
Std Dev 10.83
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

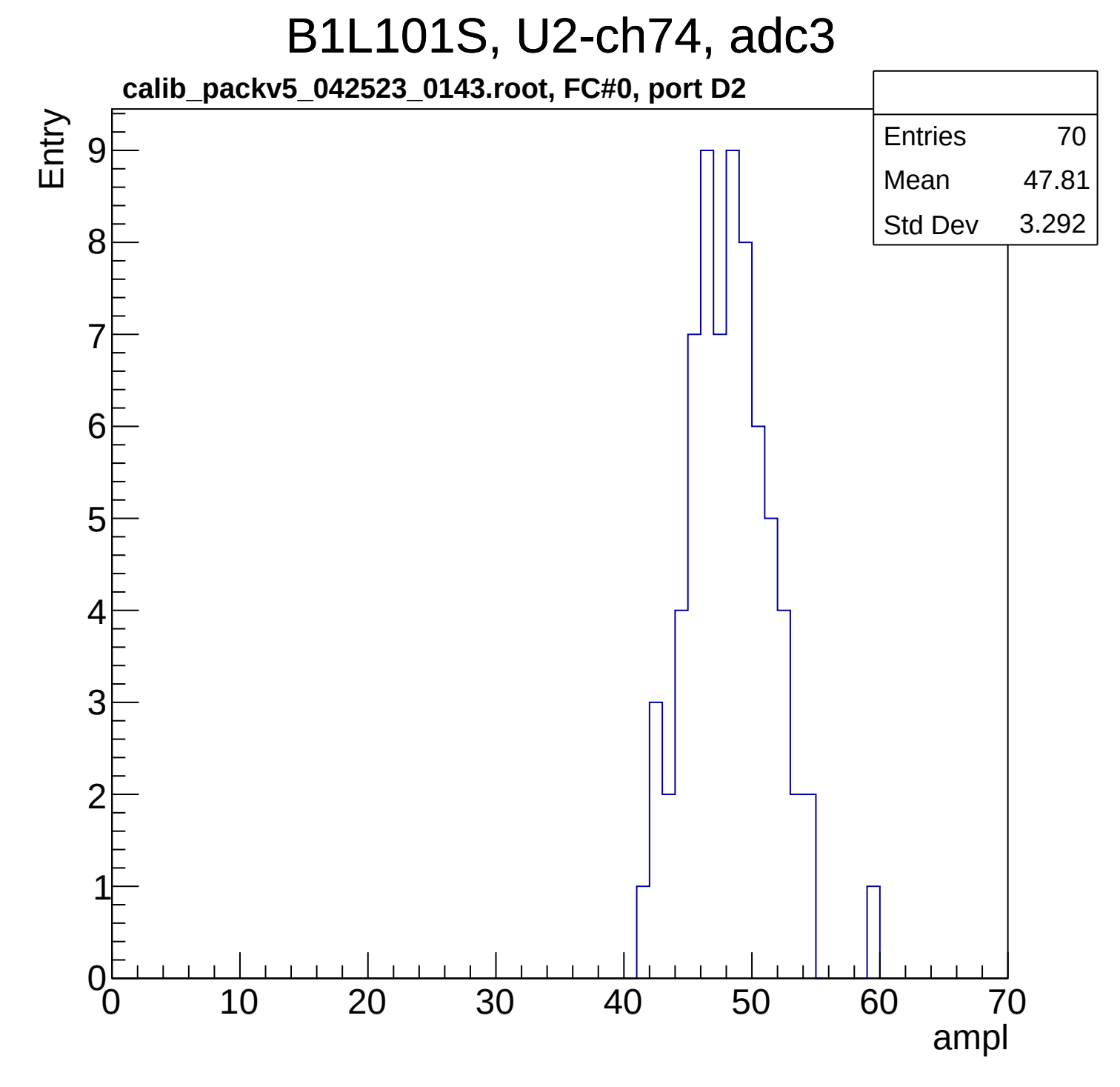

B1L101S, U2-ch73, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 62.4
Std Dev 0.8
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

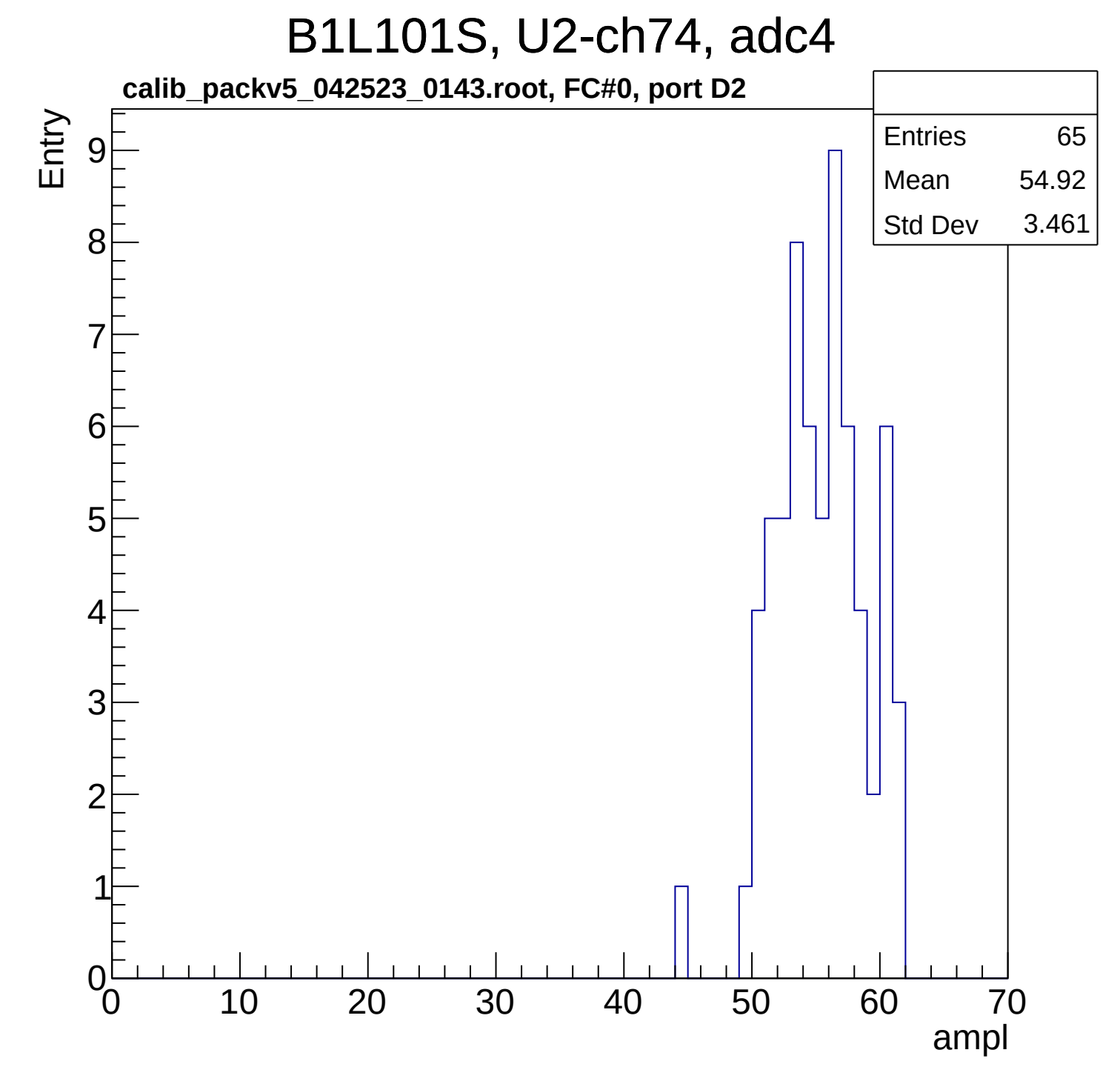

B1L101S, U2-ch73, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

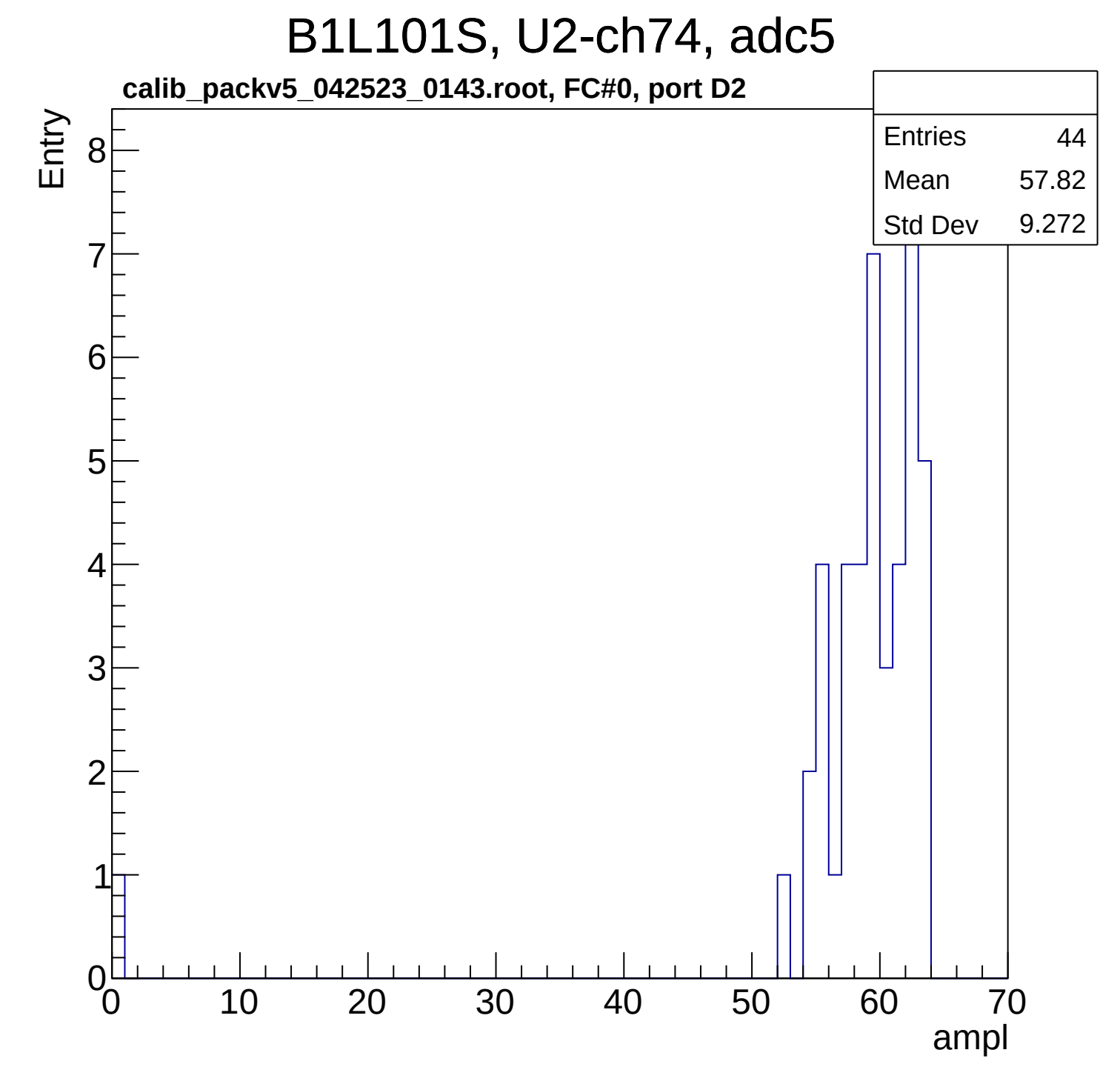

B1L101S, U2-ch74, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 90
Mean 27.01
Std Dev 5.559
Gaus mean : 28.0771
Gaus Width: 4.0875
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

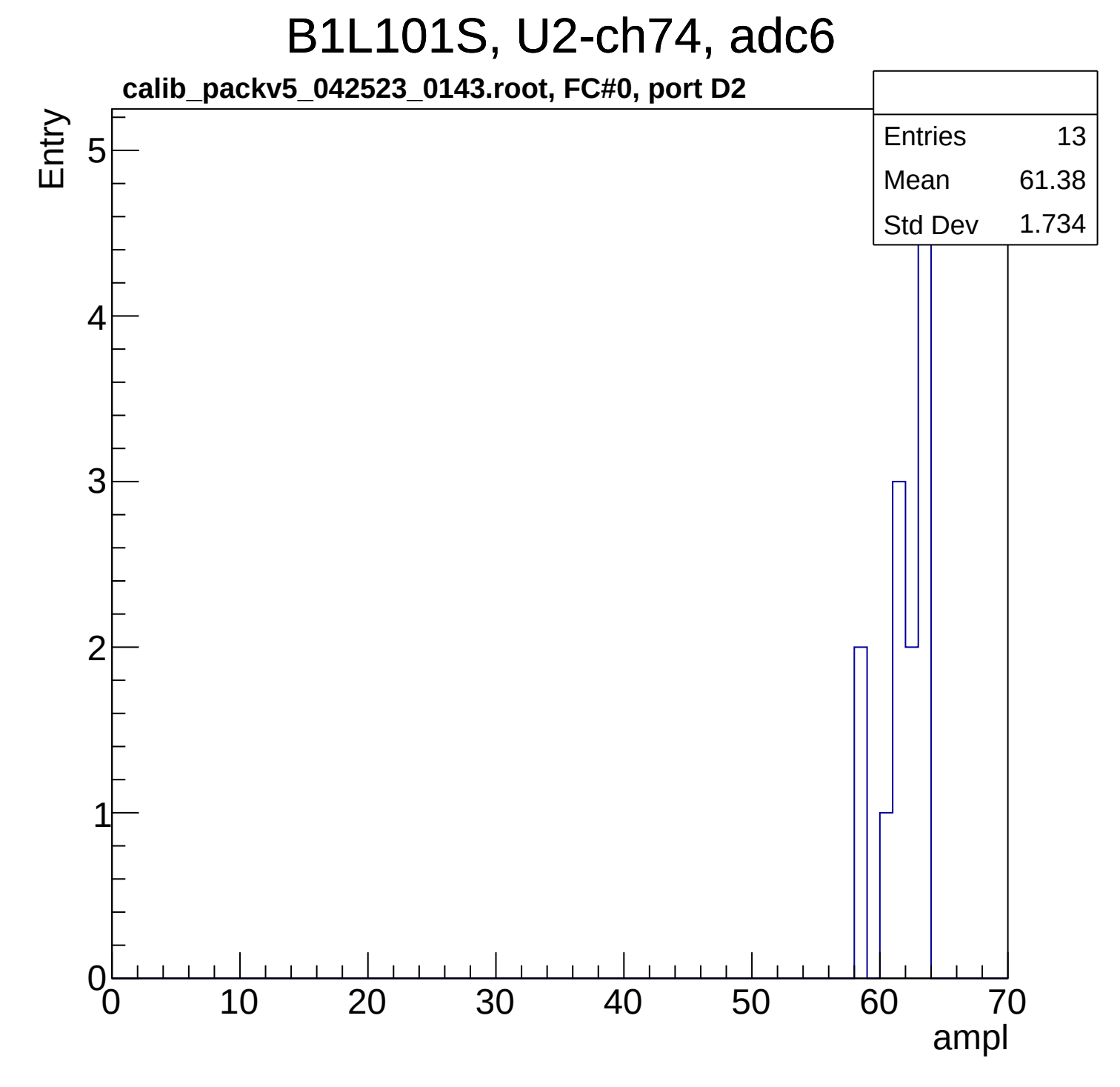

B1L101S, U2-ch74, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 35.89
Std Dev 3.113
Gaus mean : 36.2458
Gaus Width: 3.4603
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

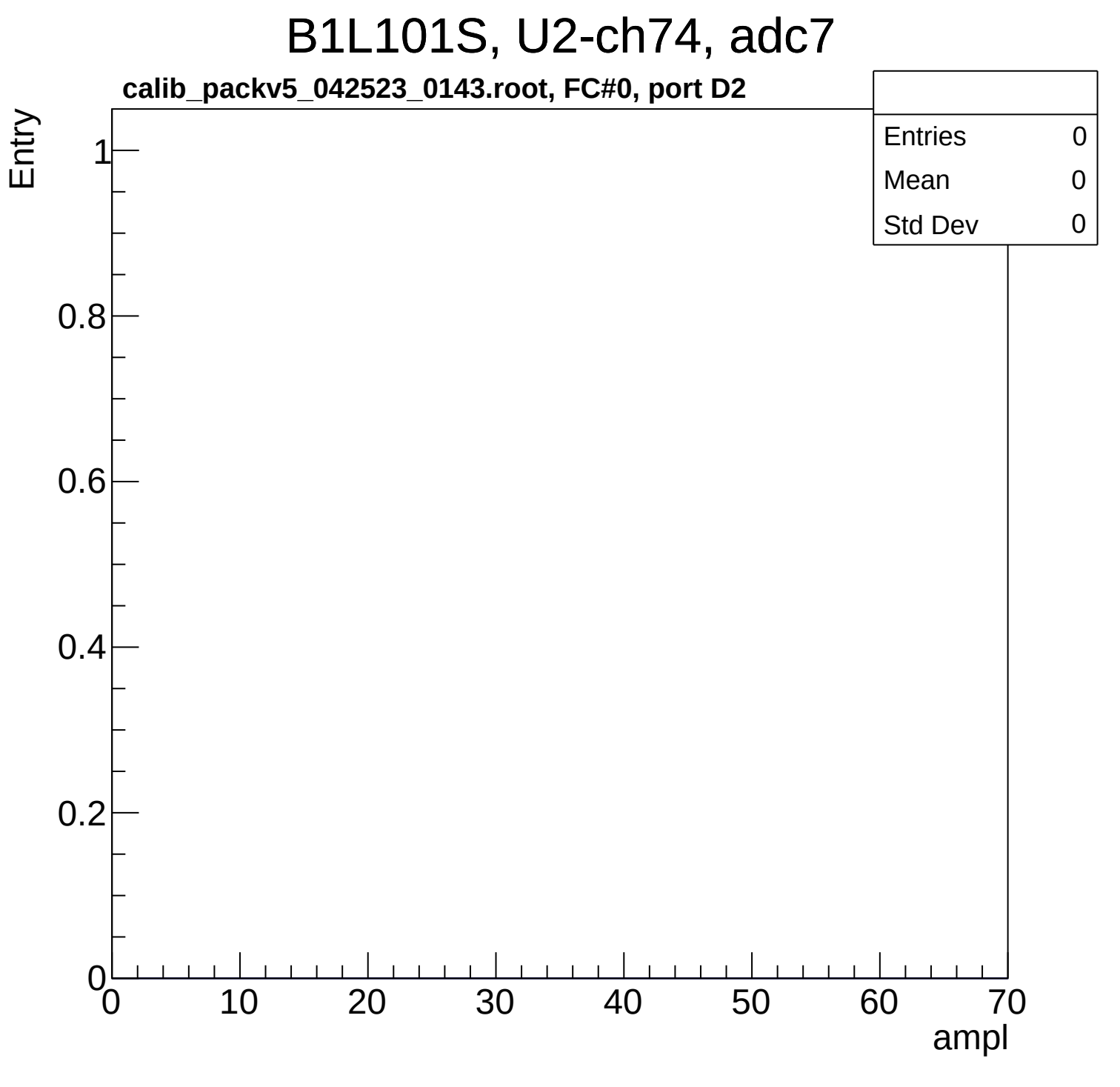

B1L101S, U2-ch74, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 41.02
Std Dev 4.021
Gaus mean : 41.4356
Gaus Width: 3.5085
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

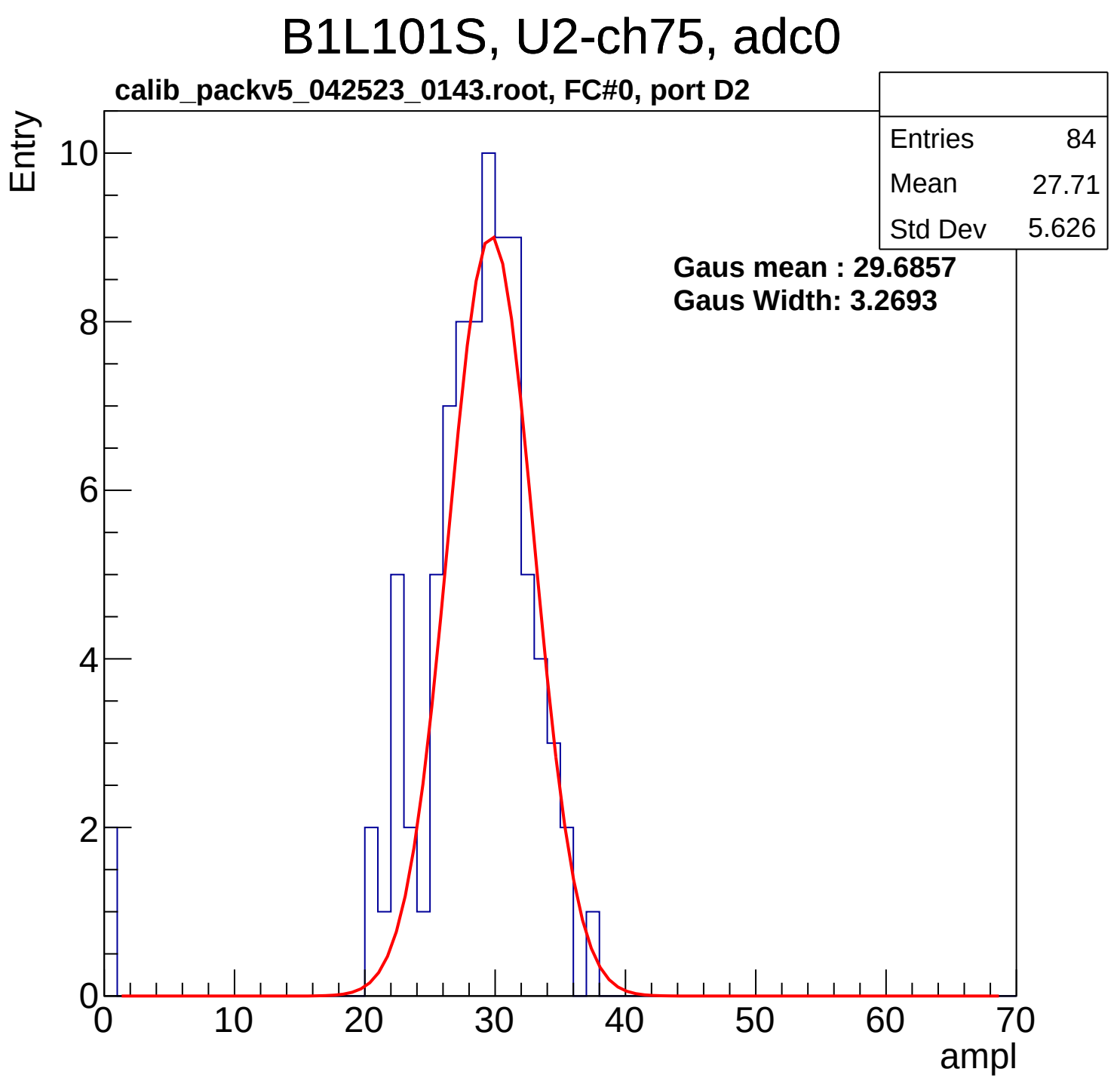

B1L101S, U2-ch74, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 47.81
Std Dev 3.292
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

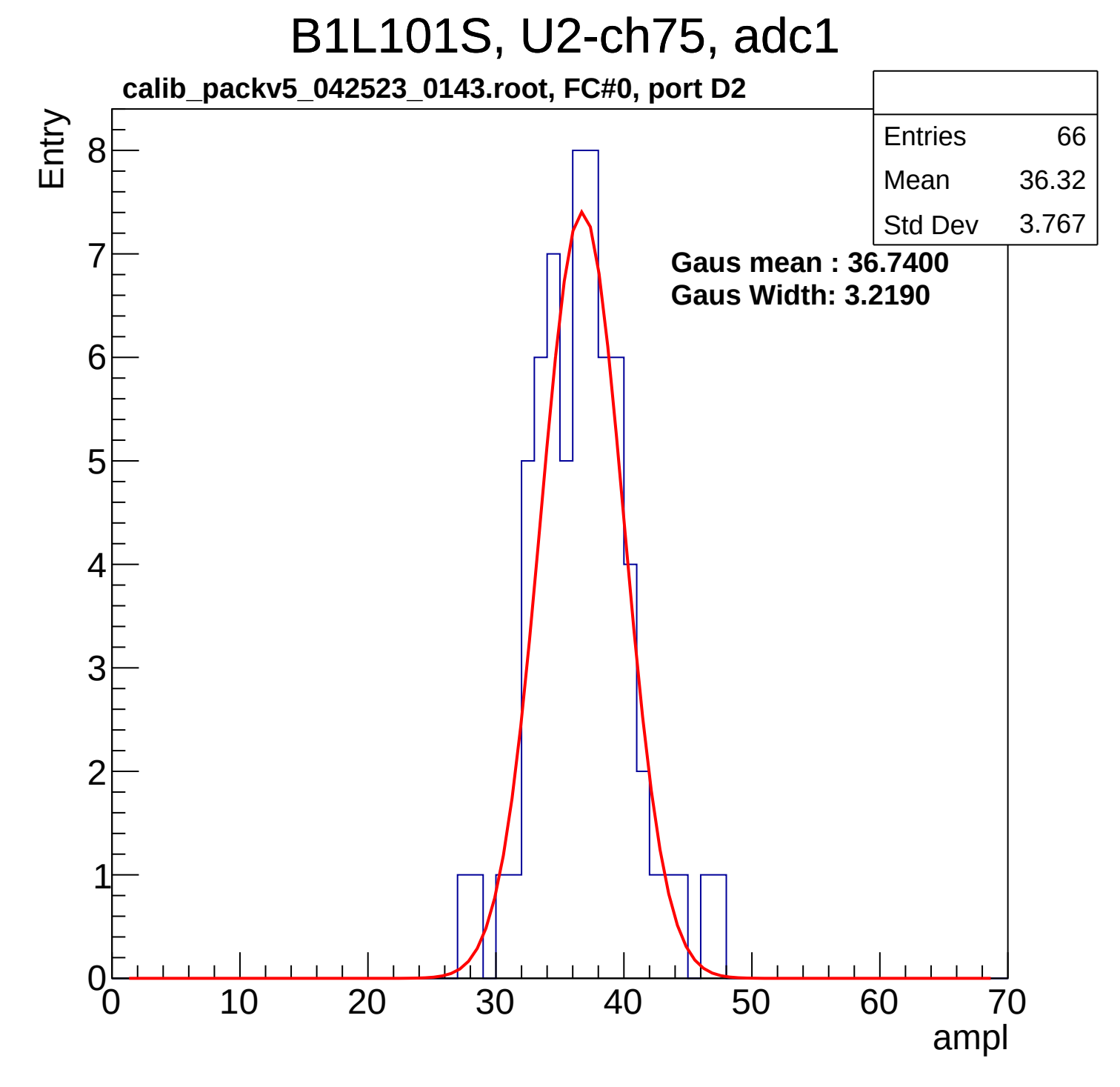

B1L101S, U2-ch74, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 54.92
Std Dev 3.461
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

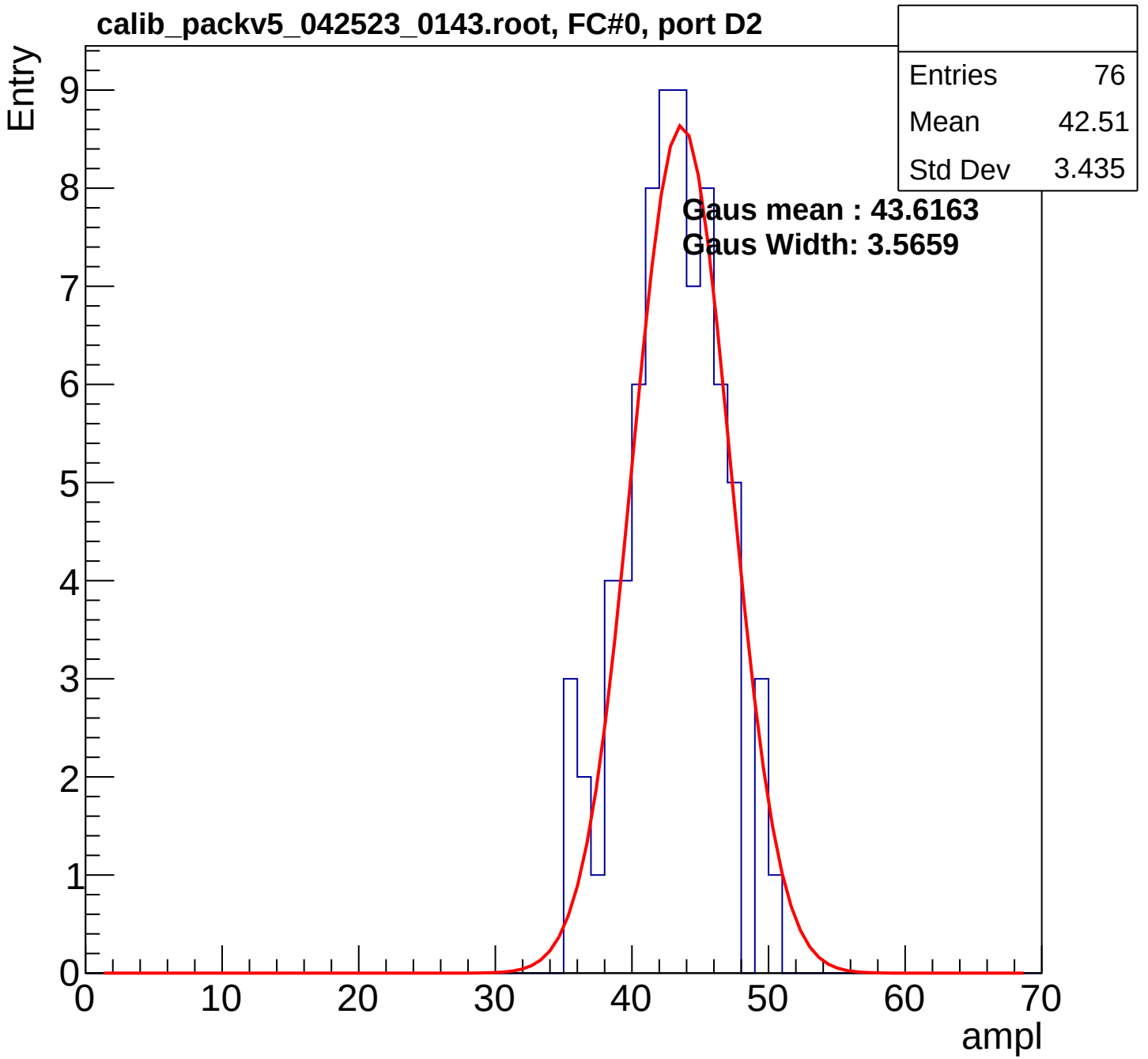

B1L101S, U2-ch74, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 44
Mean 57.82
Std Dev 9.272
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

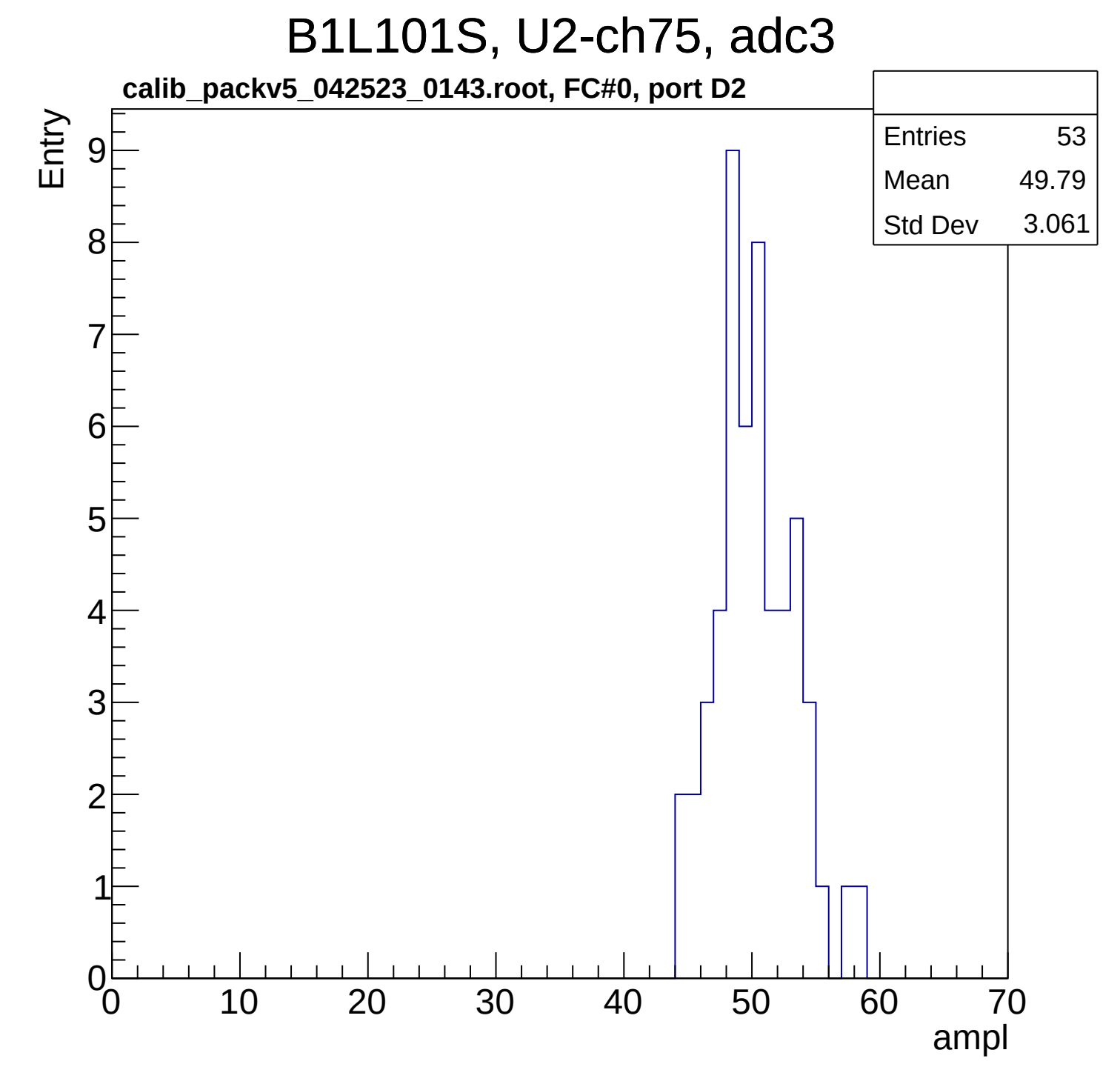

B1L101S, U2-ch74, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 13
Mean 61.38
Std Dev 1.734
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

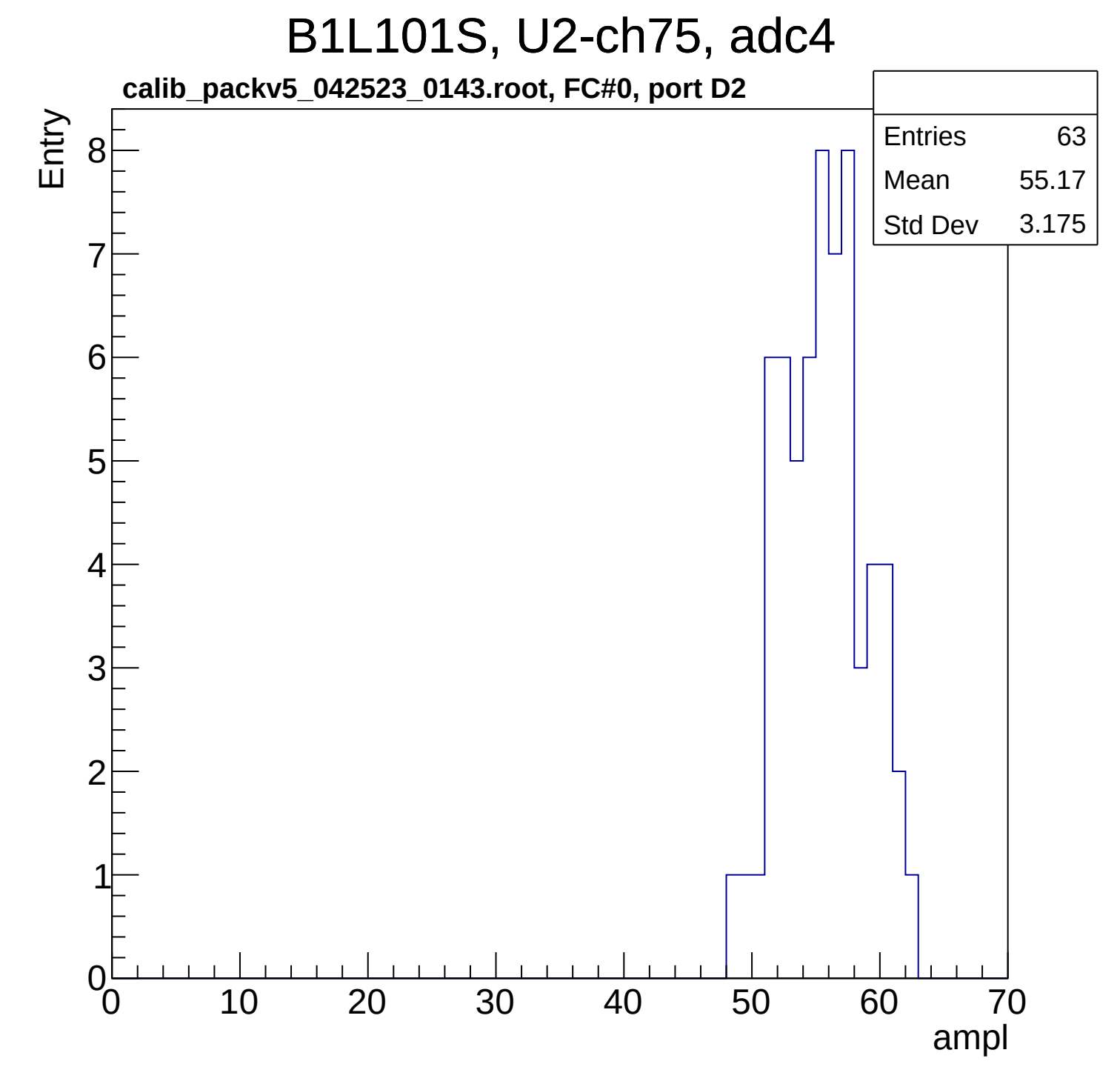

B1L101S, U2-ch74, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

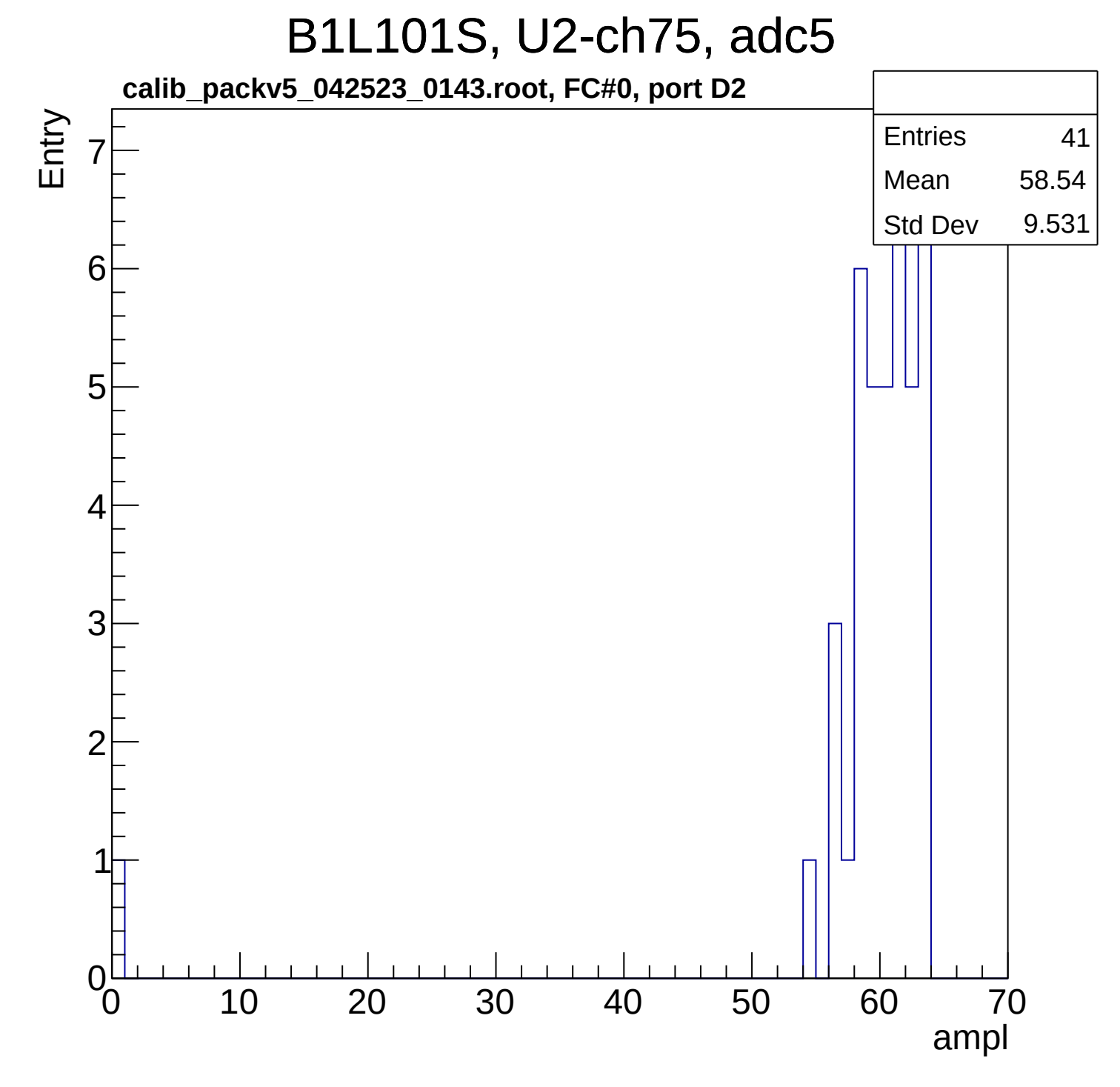

B1L101S, U2-ch75, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 84
Mean 27.71
Std Dev 5.626
Gaus mean : 29.6857
Gaus Width: 3.2693
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

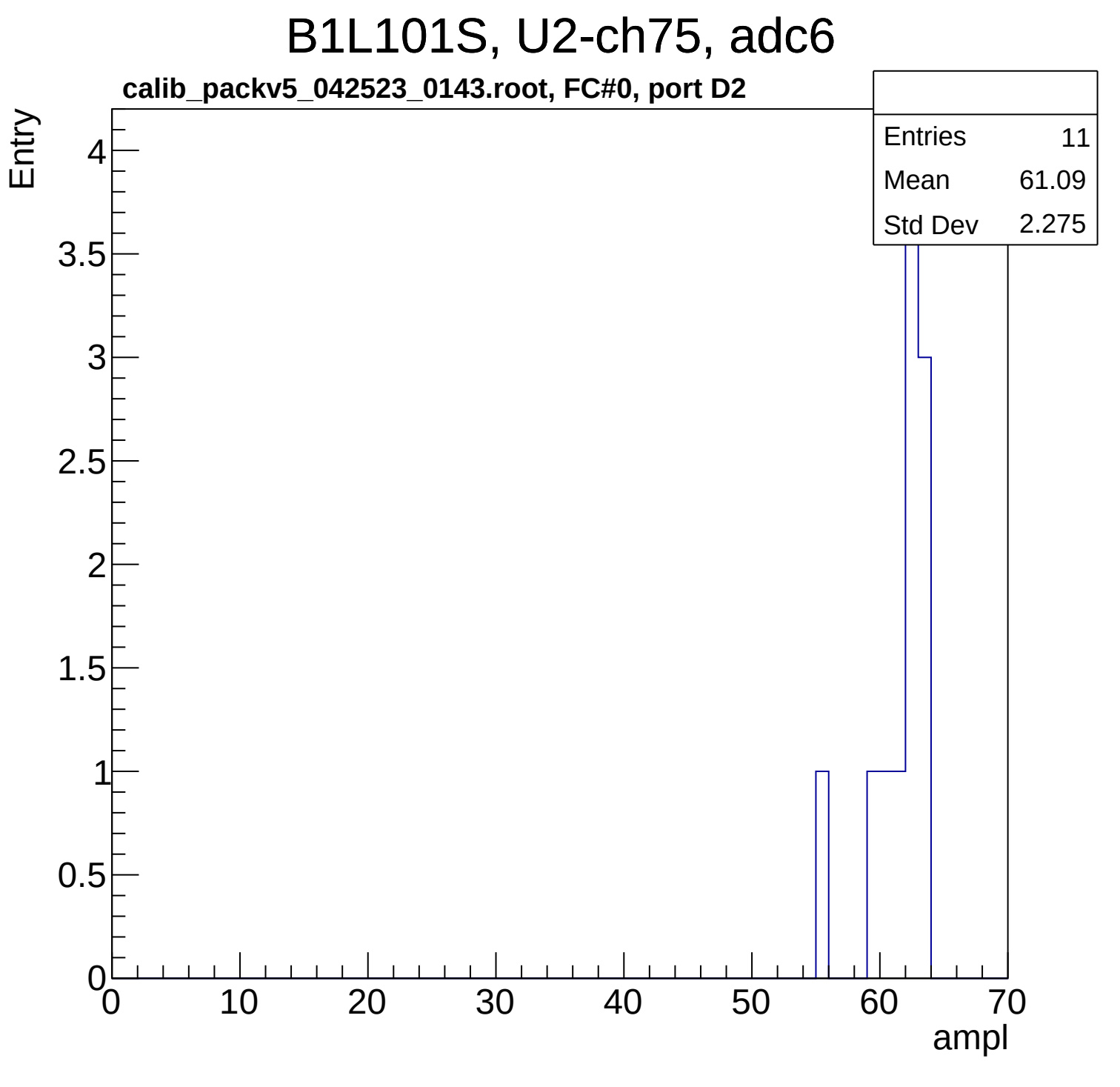

B1L101S, U2-ch75, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 36.32
Std Dev 3.767
Gaus mean : 36.7400
Gaus Width: 3.2190
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

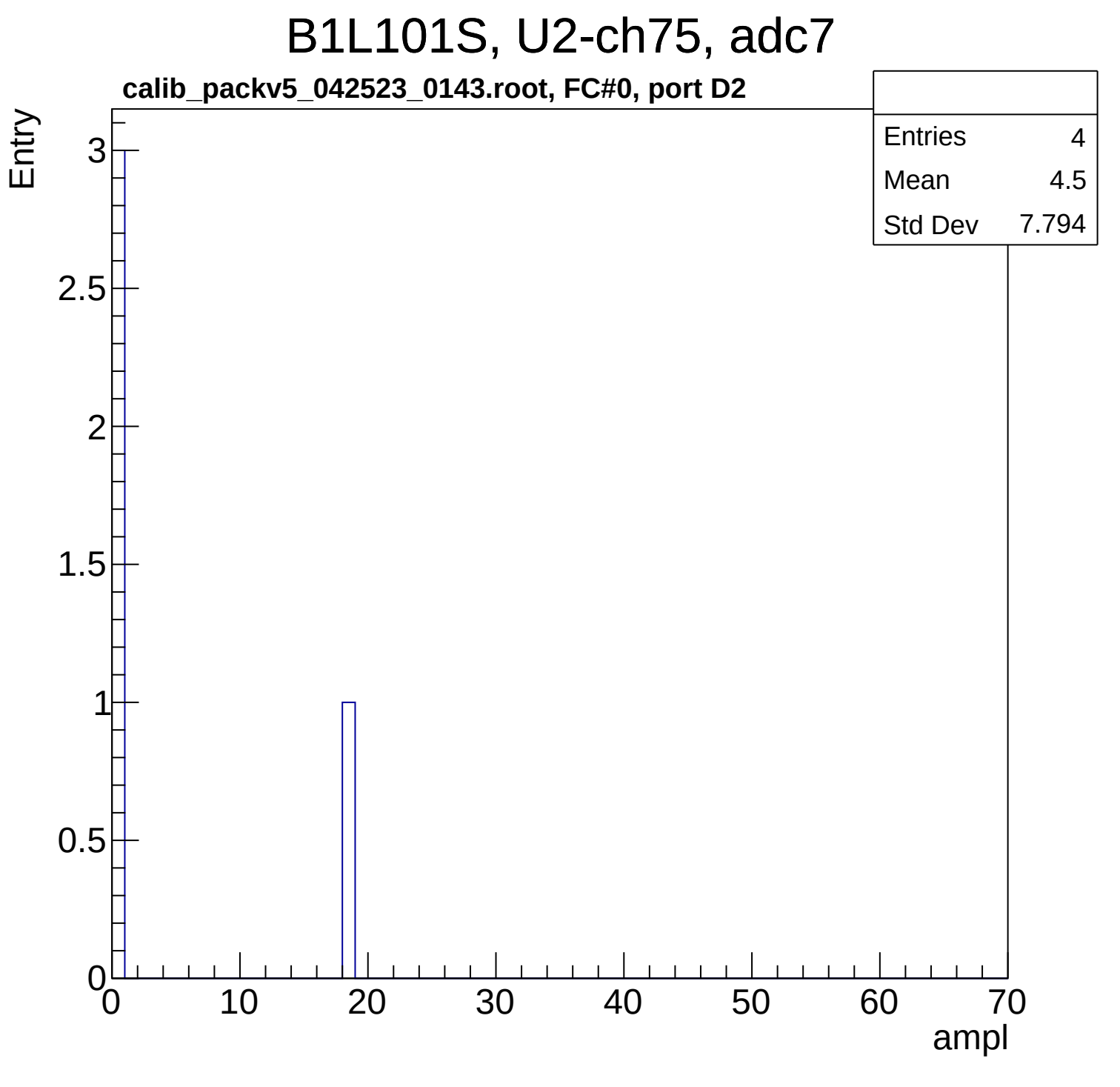

B1L101S, U2-ch75, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 42.51
Std Dev 3.435
Gaus mean : 43.6163
Gaus Width: 3.5659
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

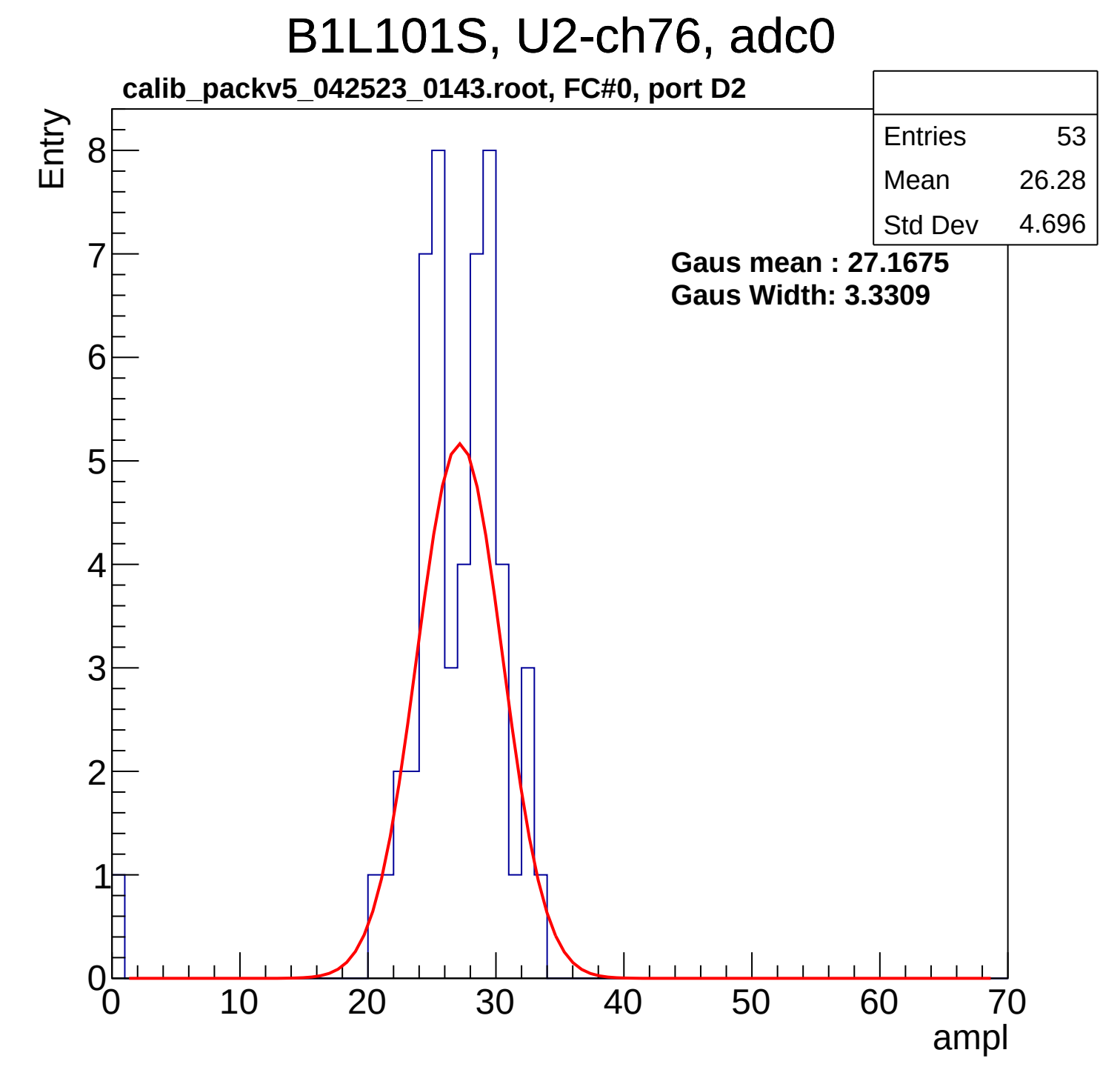

B1L101S, U2-ch75, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 49.79
Std Dev 3.061
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

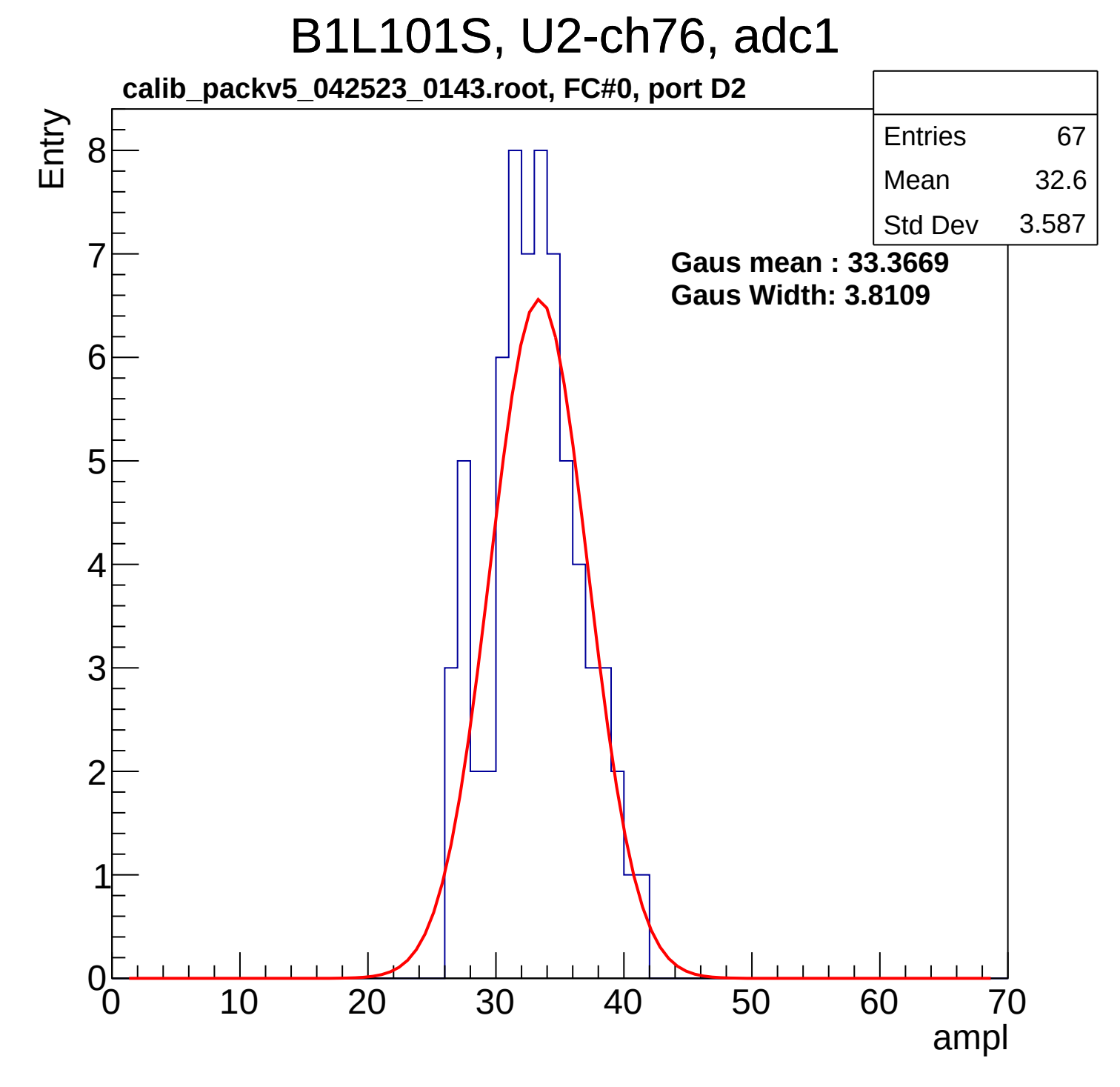

B1L101S, U2-ch75, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 55.17
Std Dev 3.175
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

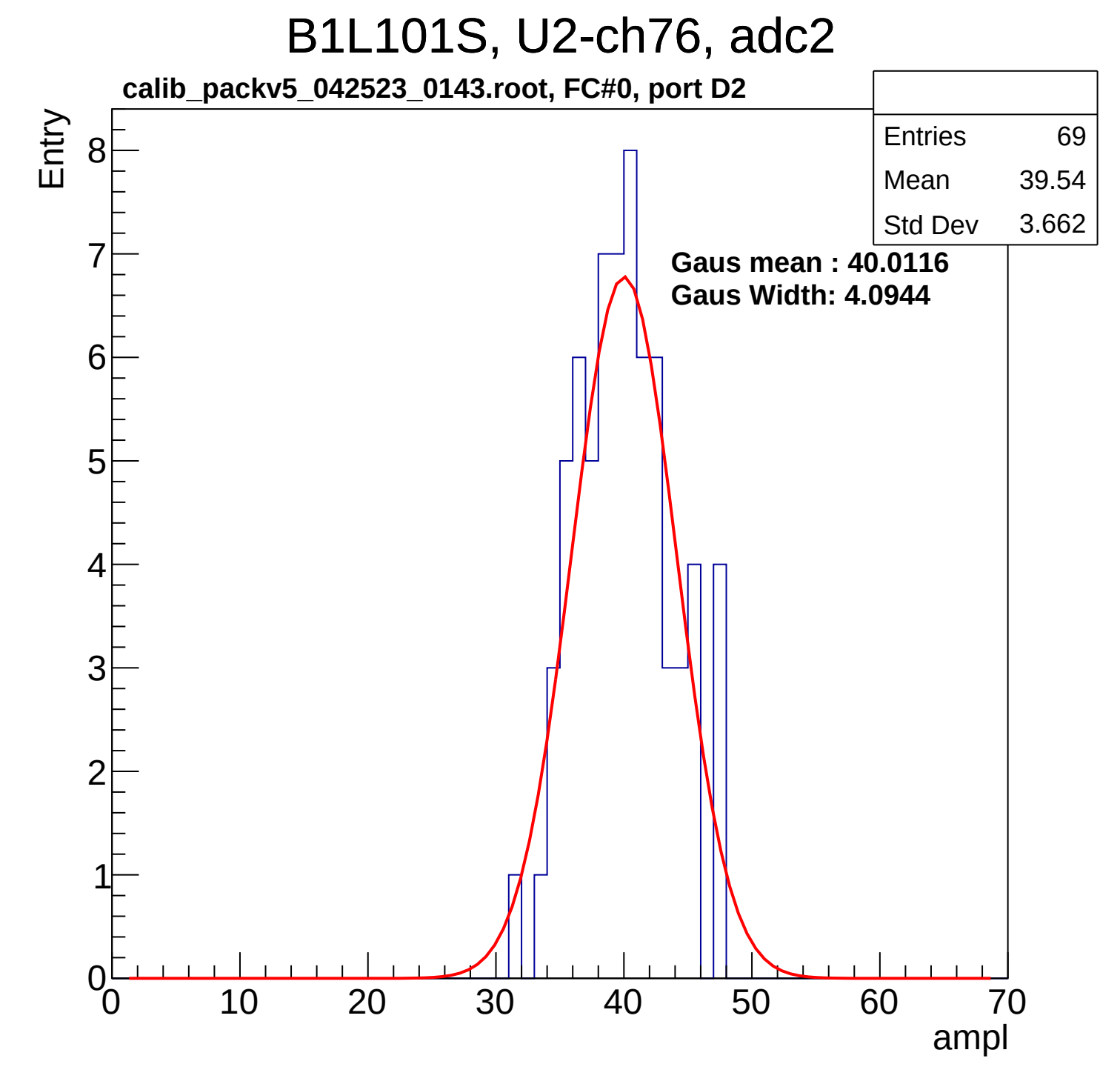

B1L101S, U2-ch75, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 41
Mean 58.54
Std Dev 9.531
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

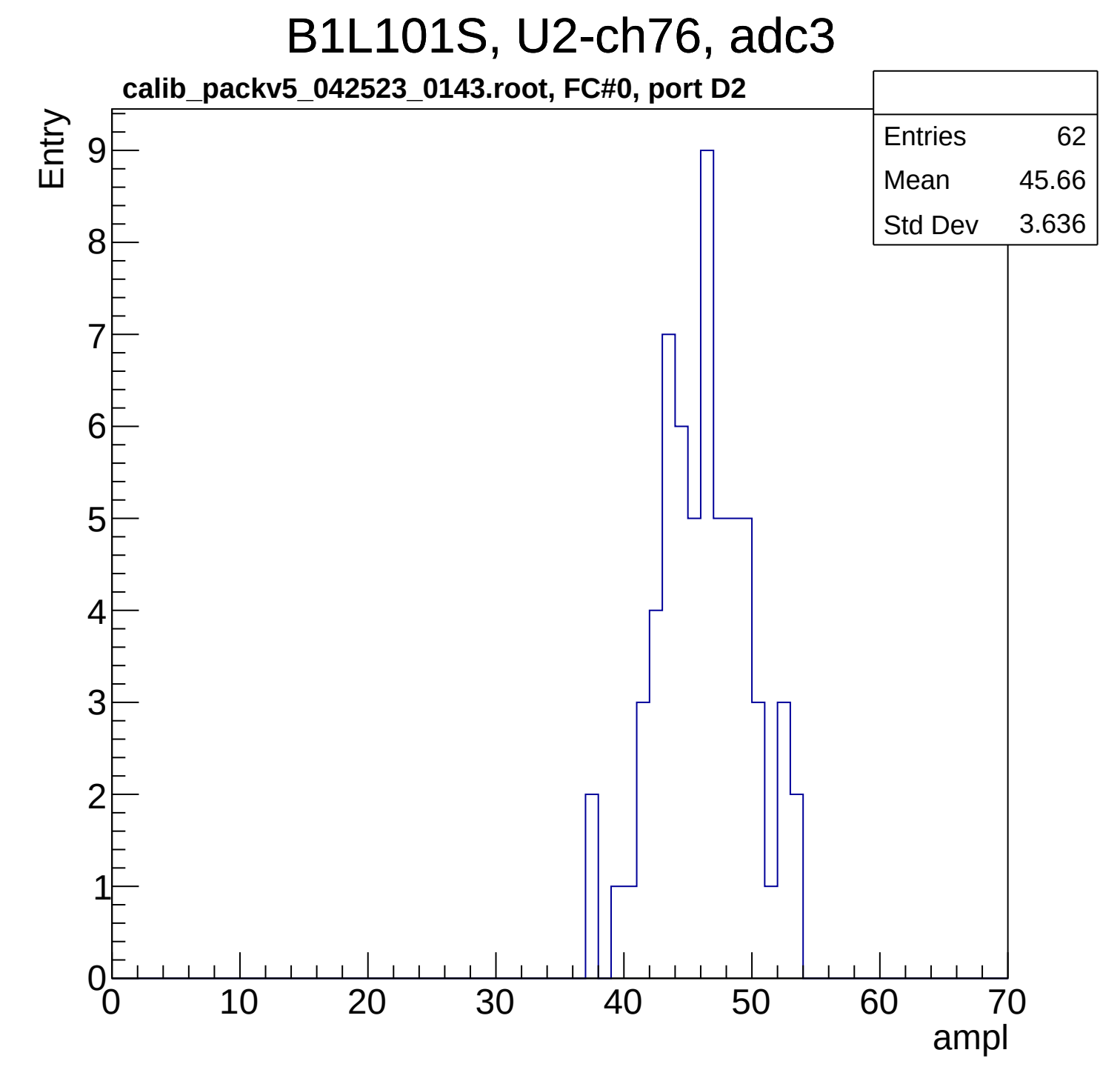

B1L101S, U2-ch75, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 11
Mean 61.09
Std Dev 2.275
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

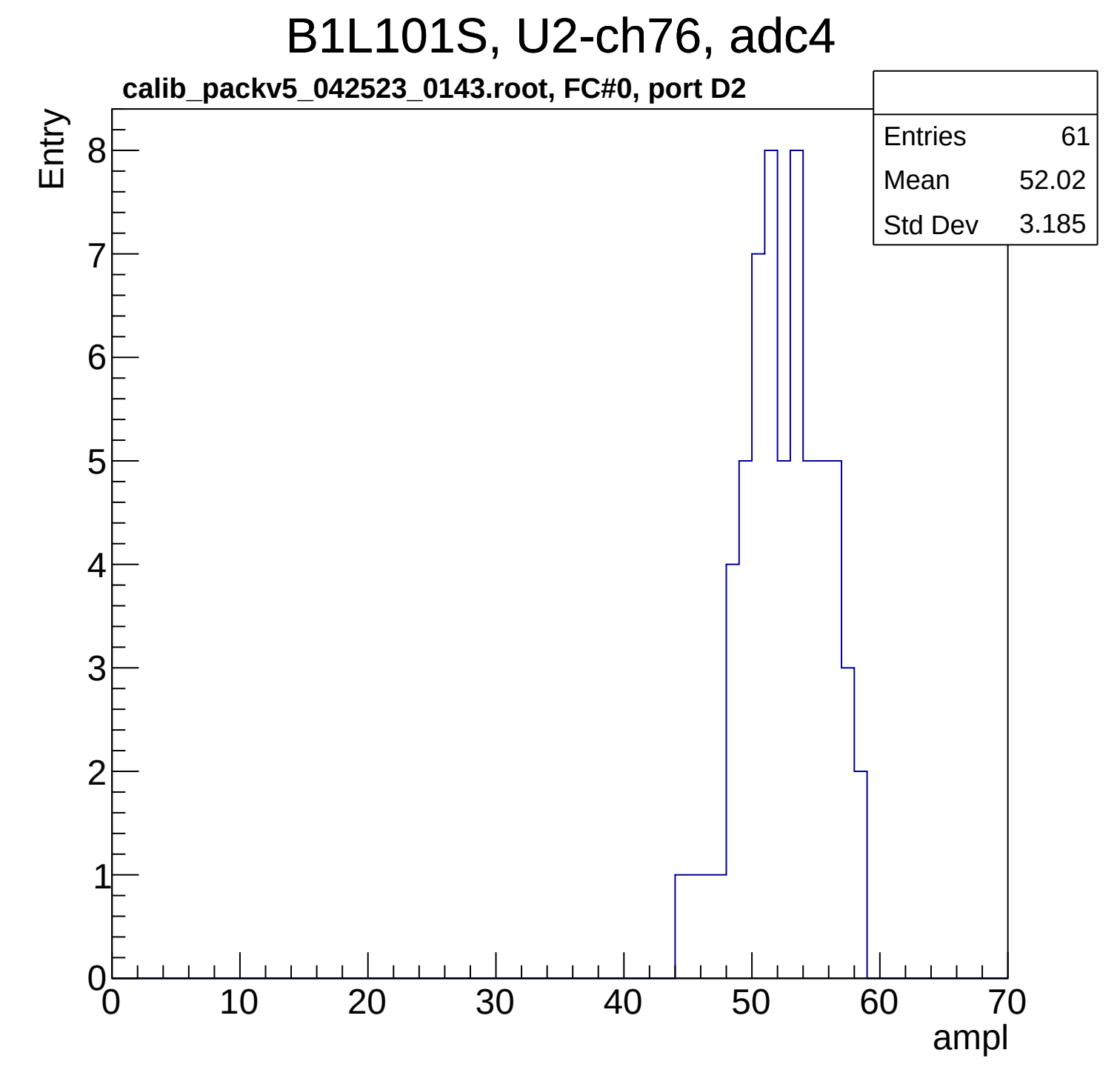

B1L101S, U2-ch75, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 4.5
Std Dev 7.794
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

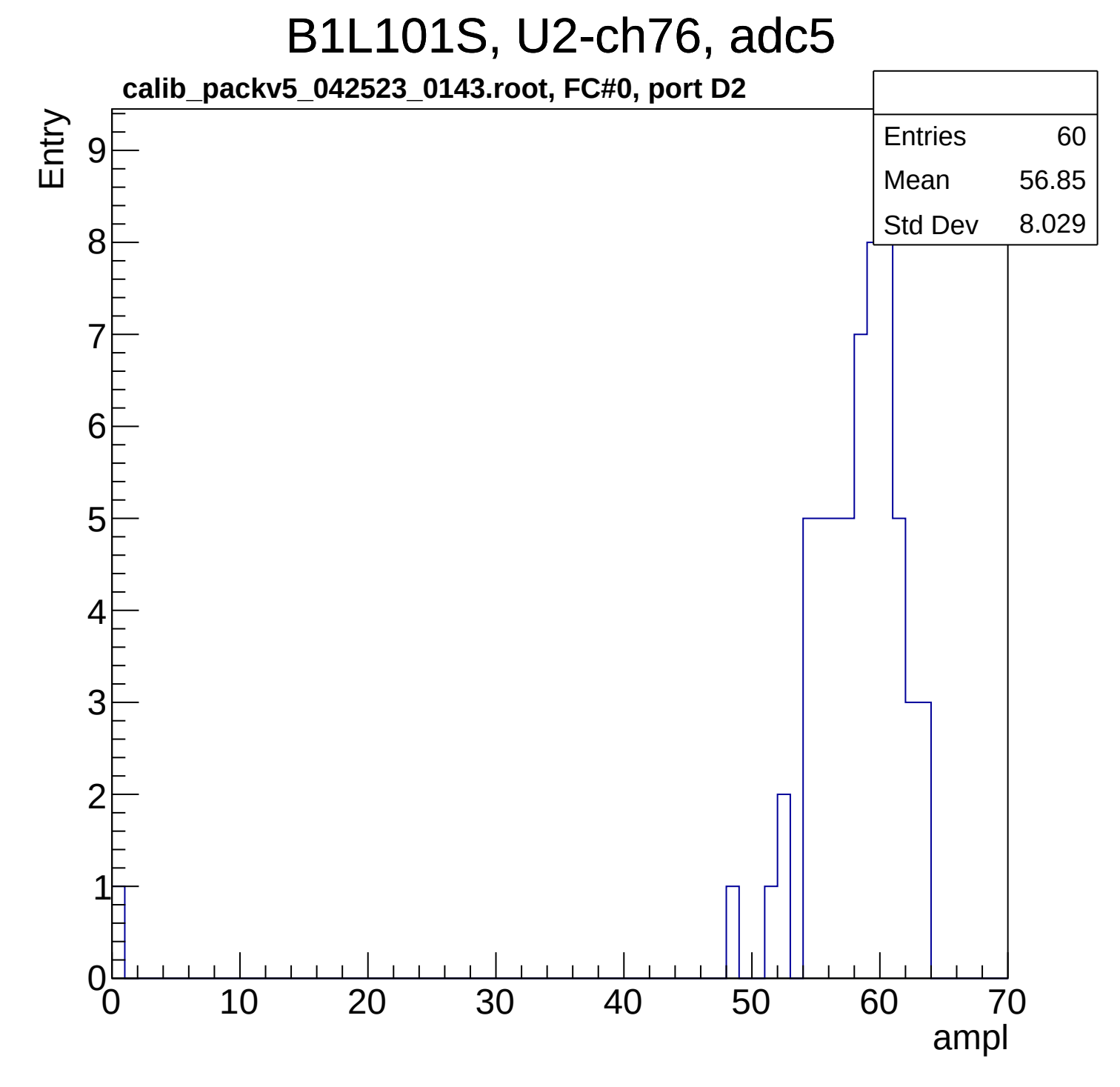

B1L101S, U2-ch76, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 26.28
Std Dev 4.696
Gaus mean : 27.1675
Gaus Width: 3.3309
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

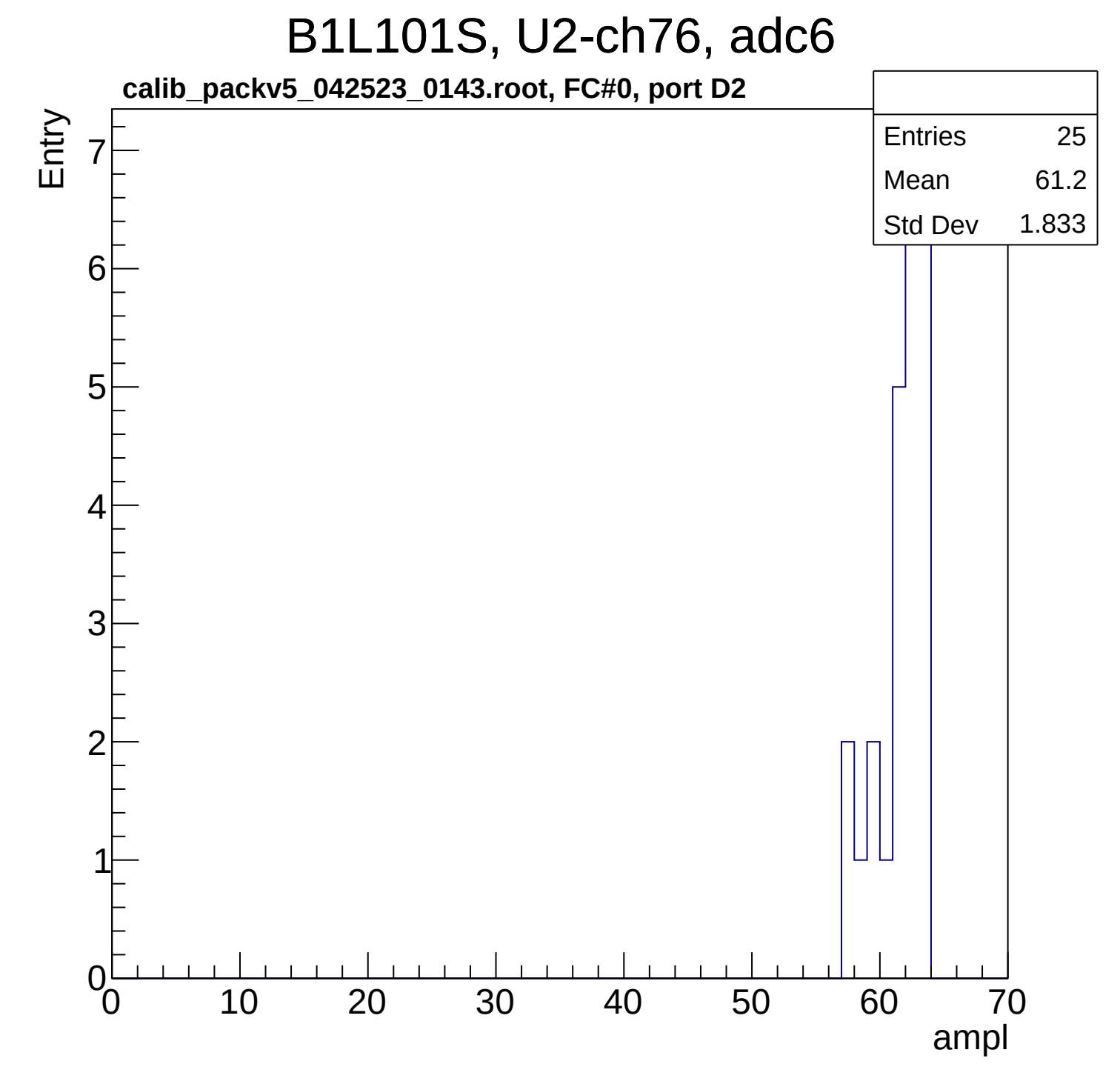

B1L101S, U2-ch76, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 32.6
Std Dev 3.587
Gaus mean : 33.3669
Gaus Width: 3.8109
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

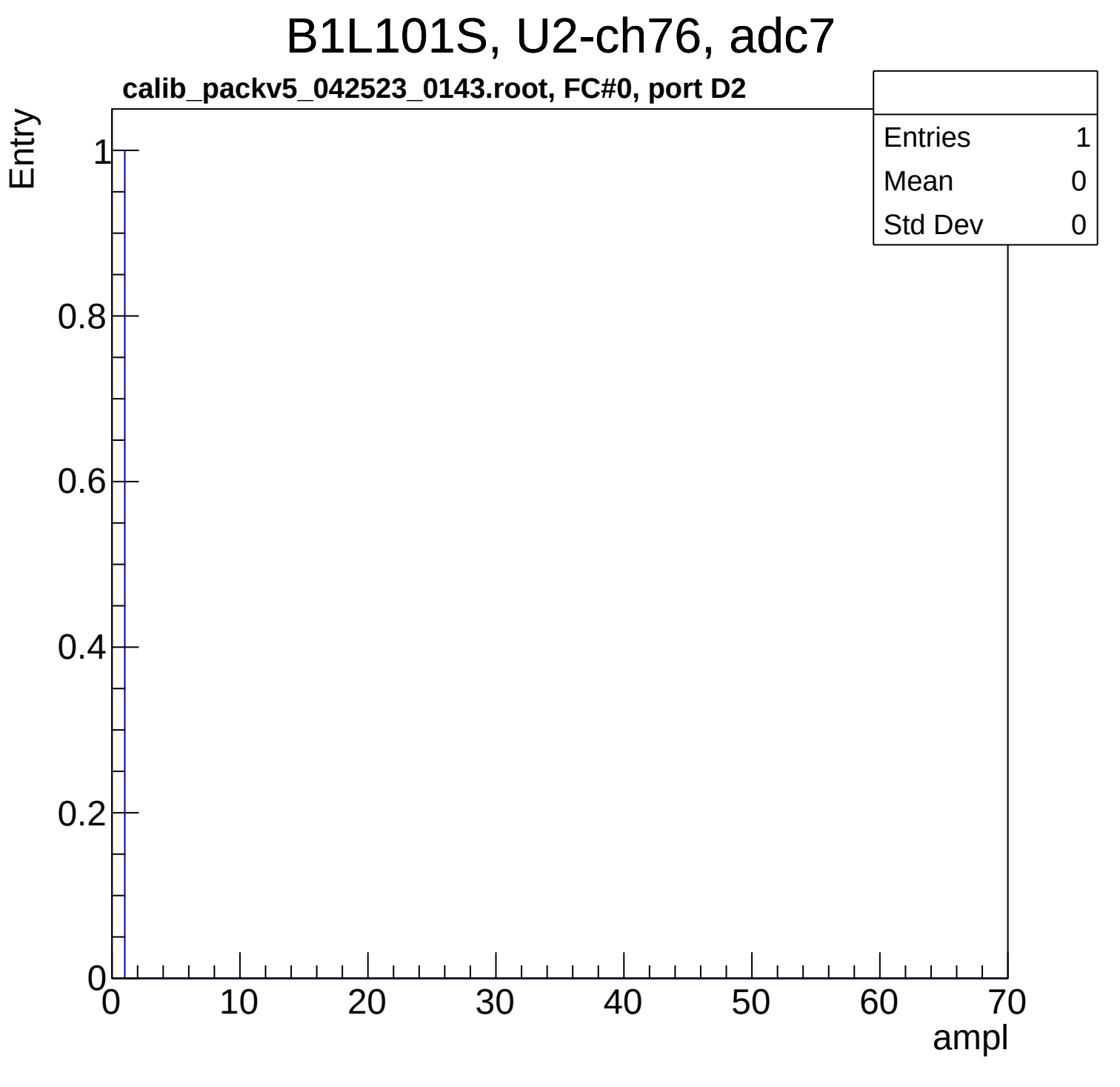

B1L101S, U2-ch76, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 39.54
Std Dev 3.662
Gaus mean : 40.0116
Gaus Width: 4.0944
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

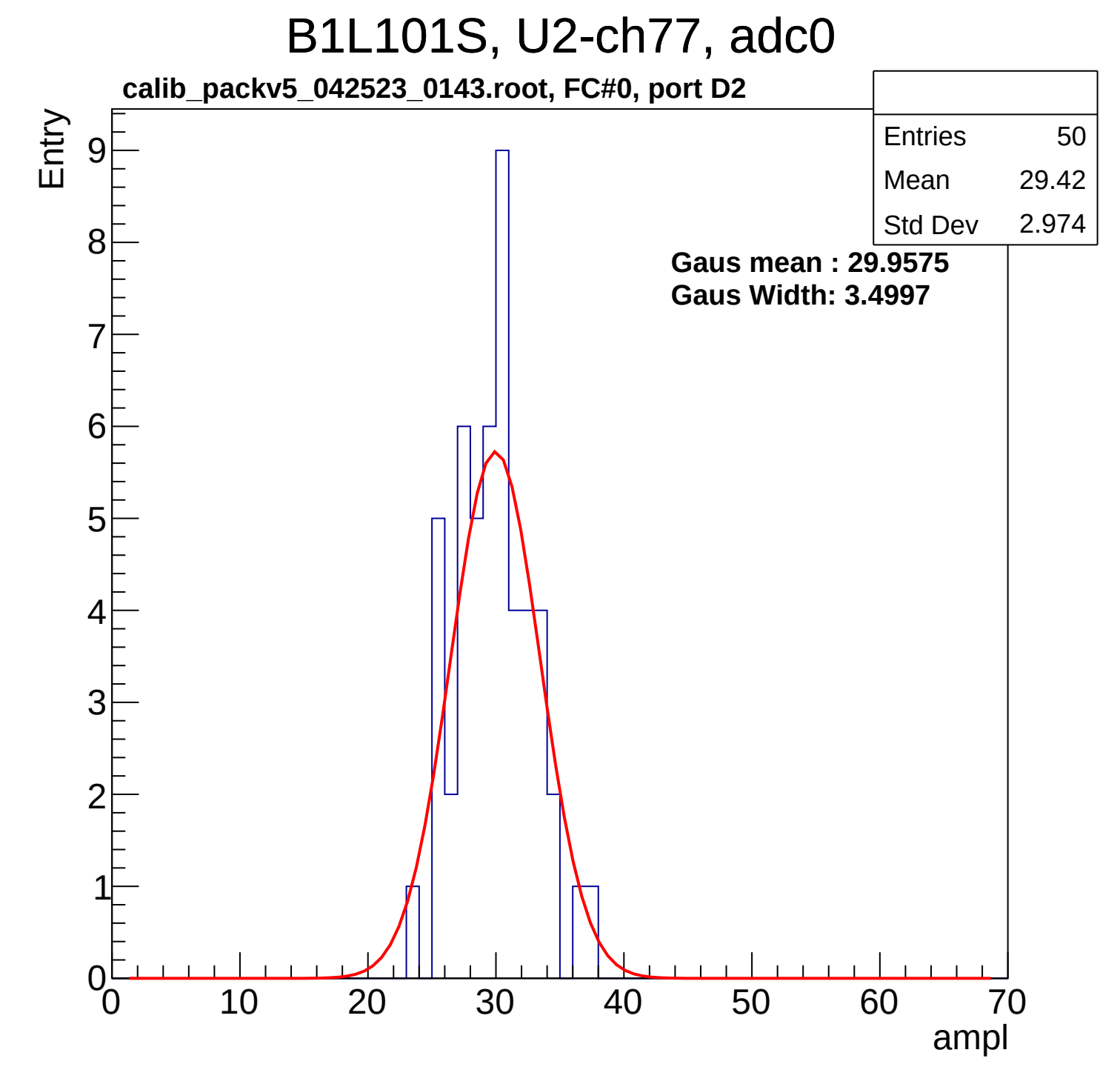

B1L101S, U2-ch76, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 45.66
Std Dev 3.636
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

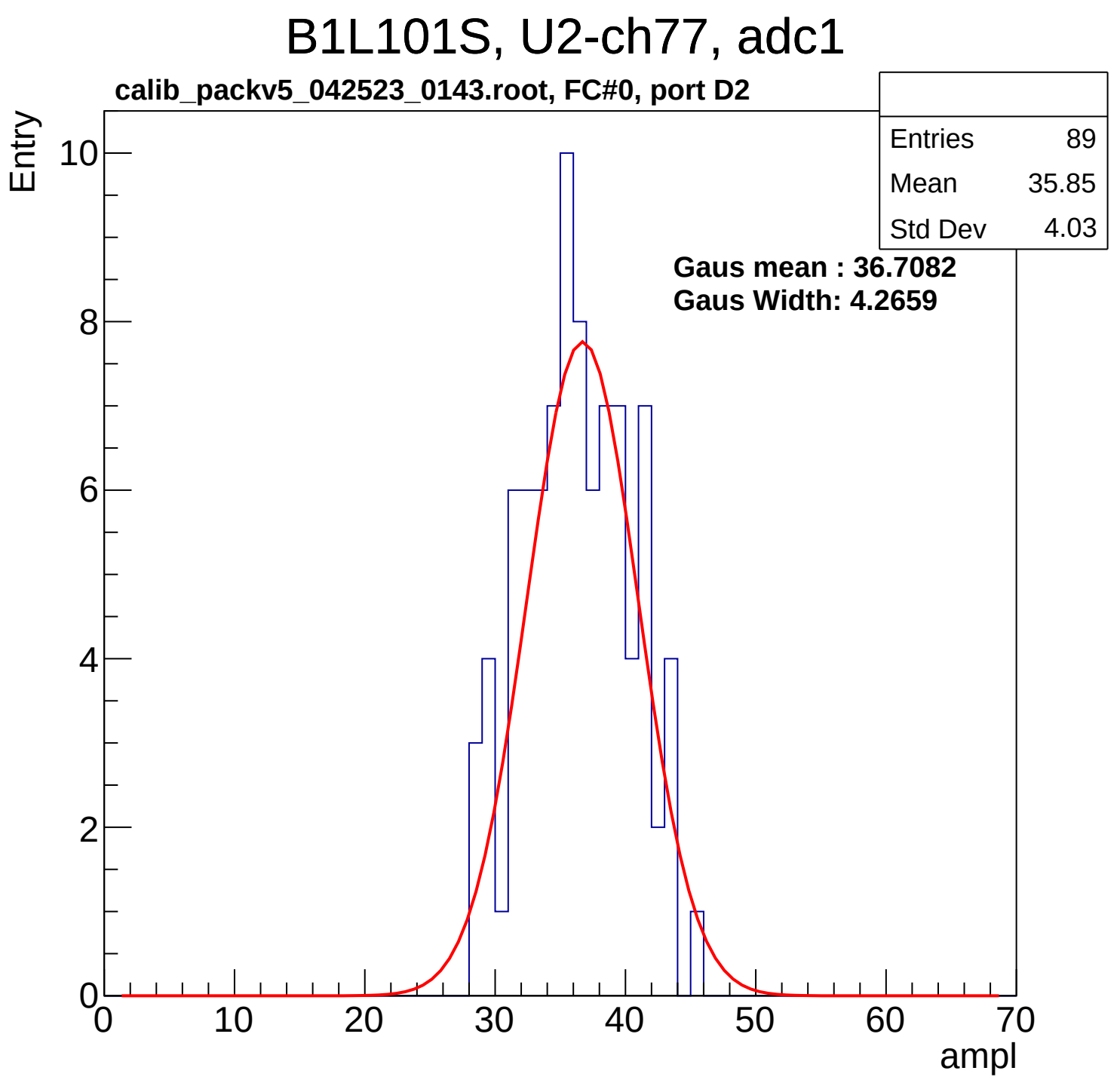

B1L101S, U2-ch76, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 52.02
Std Dev 3.185
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

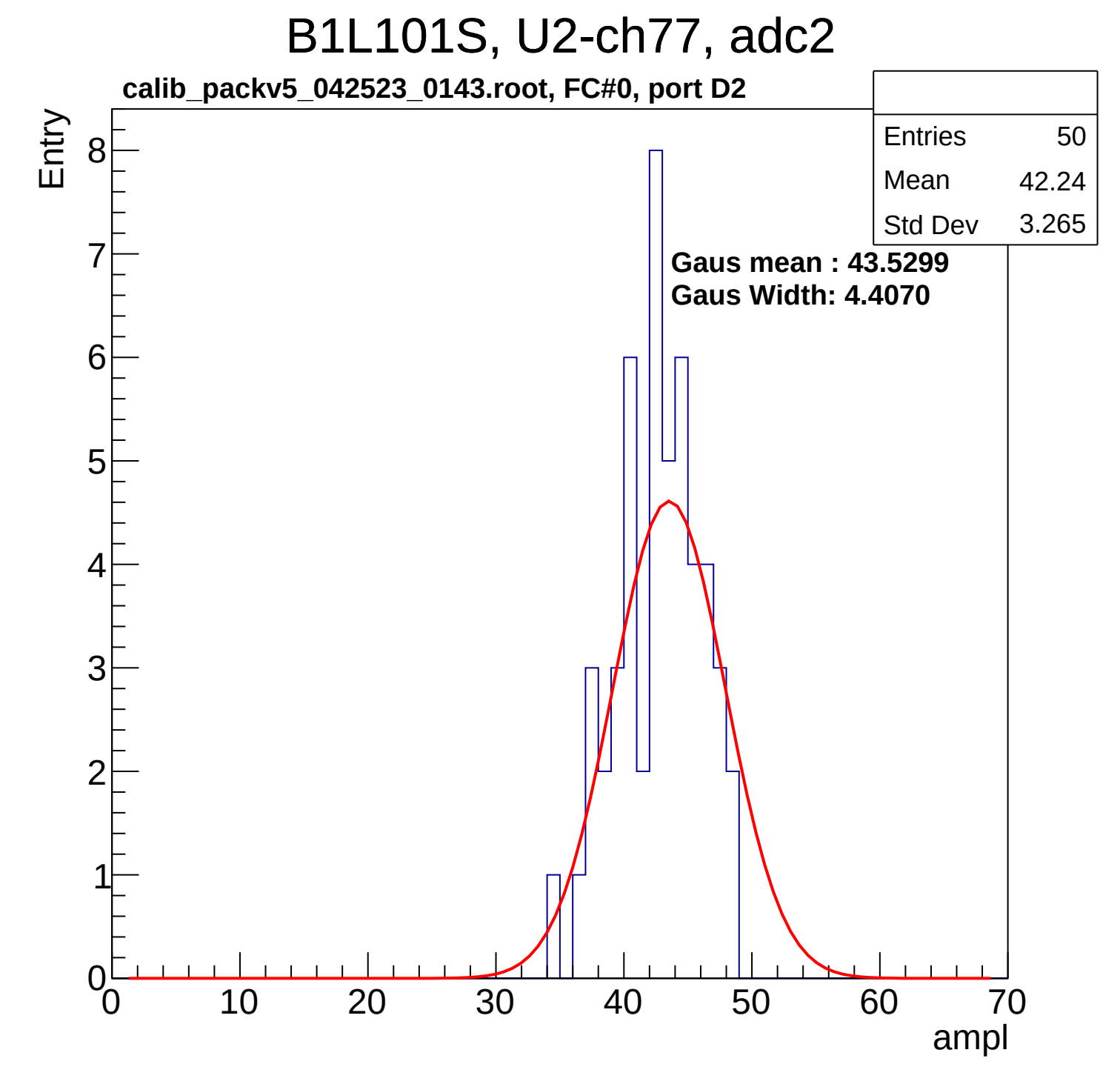

B1L101S, U2-ch76, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 56.85
Std Dev 8.029
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

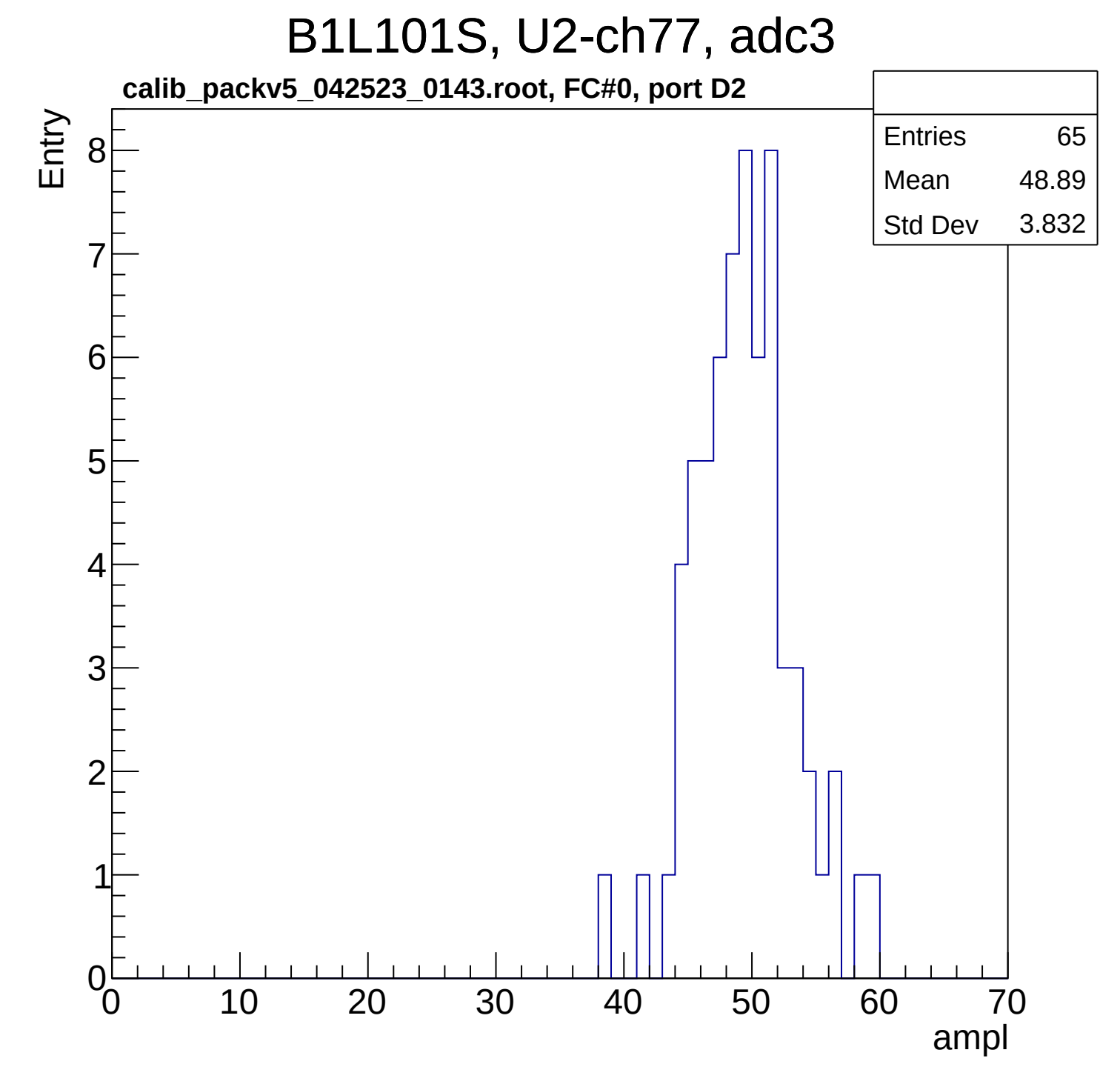

B1L101S, U2-ch76, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 25
Mean 61.2
Std Dev 1.833
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

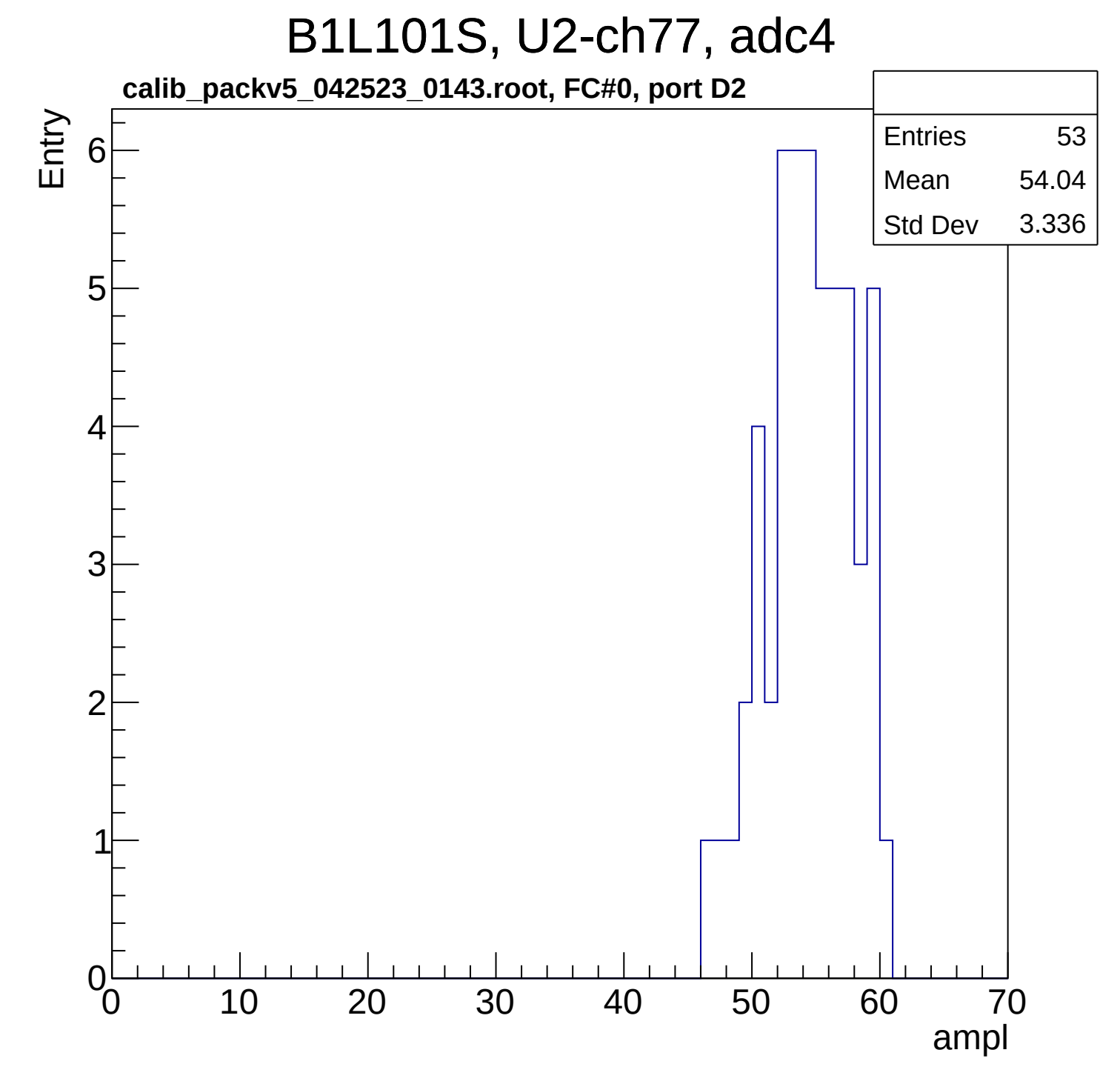

B1L101S, U2-ch76, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

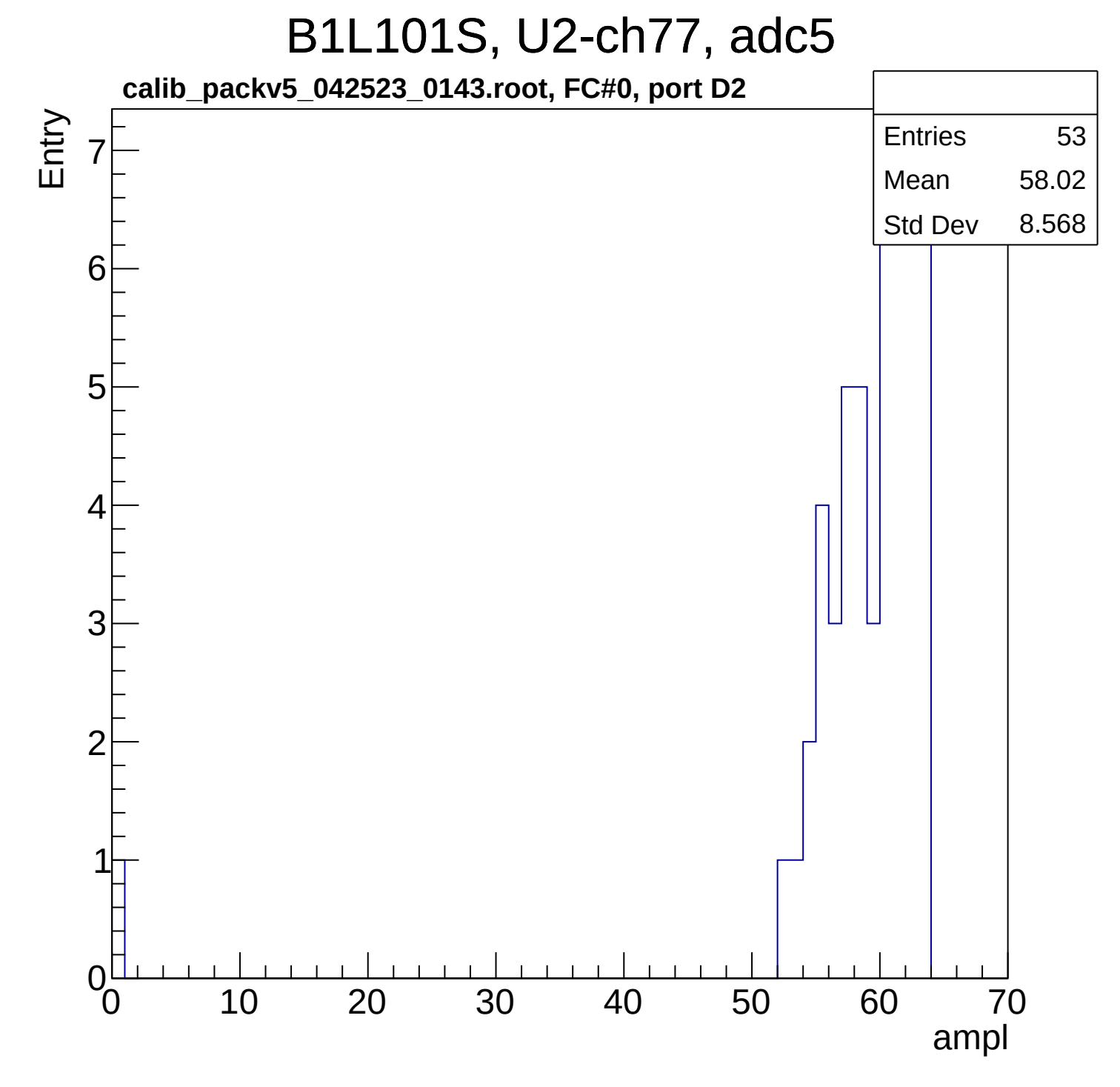

B1L101S, U2-ch77, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 29.42
Std Dev 2.974
Gaus mean : 29.9575
Gaus Width: 3.4997
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

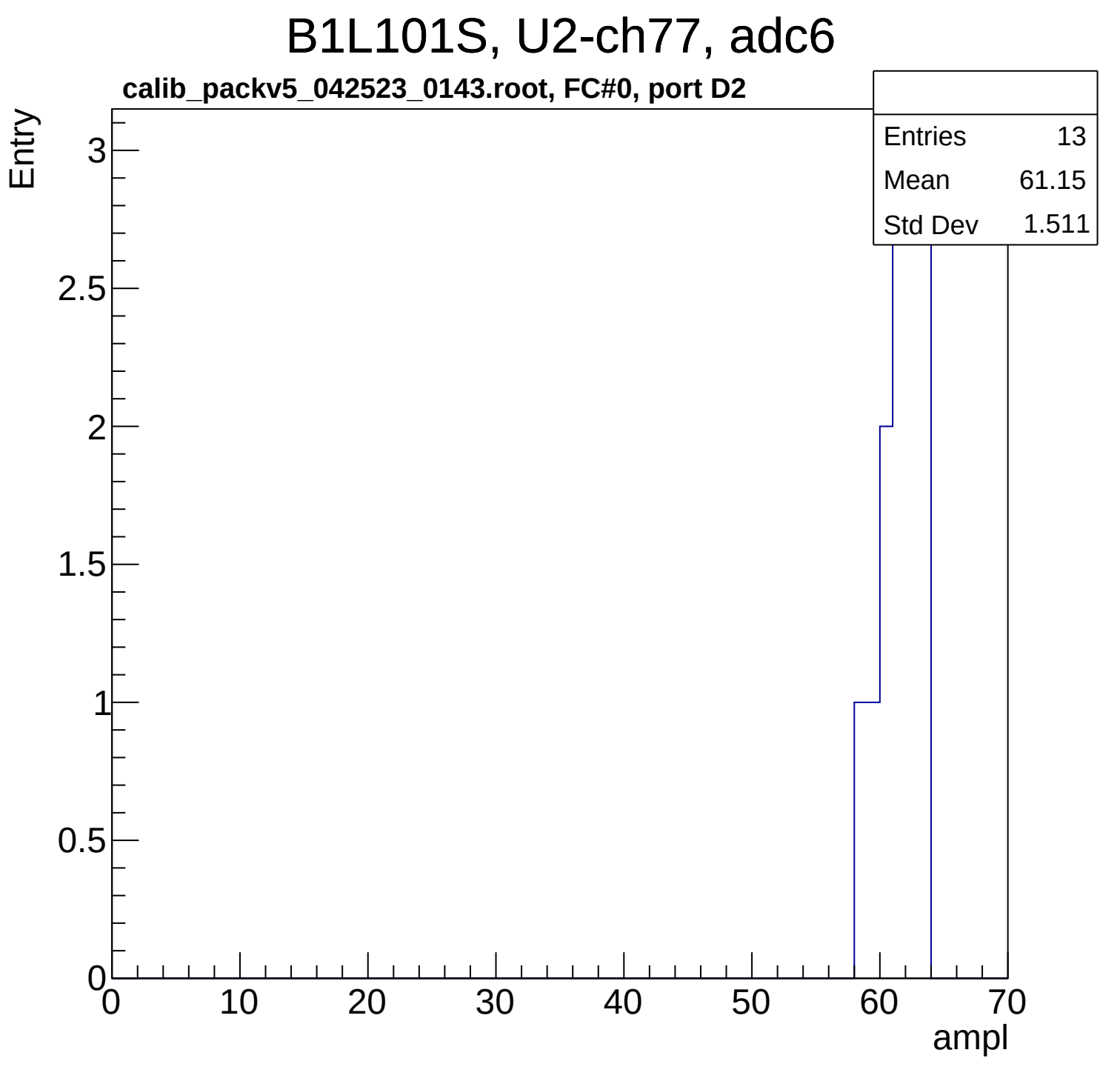

B1L101S, U2-ch77, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 89
Mean 35.85
Std Dev 4.03
Gaus mean : 36.7082
Gaus Width: 4.2659
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

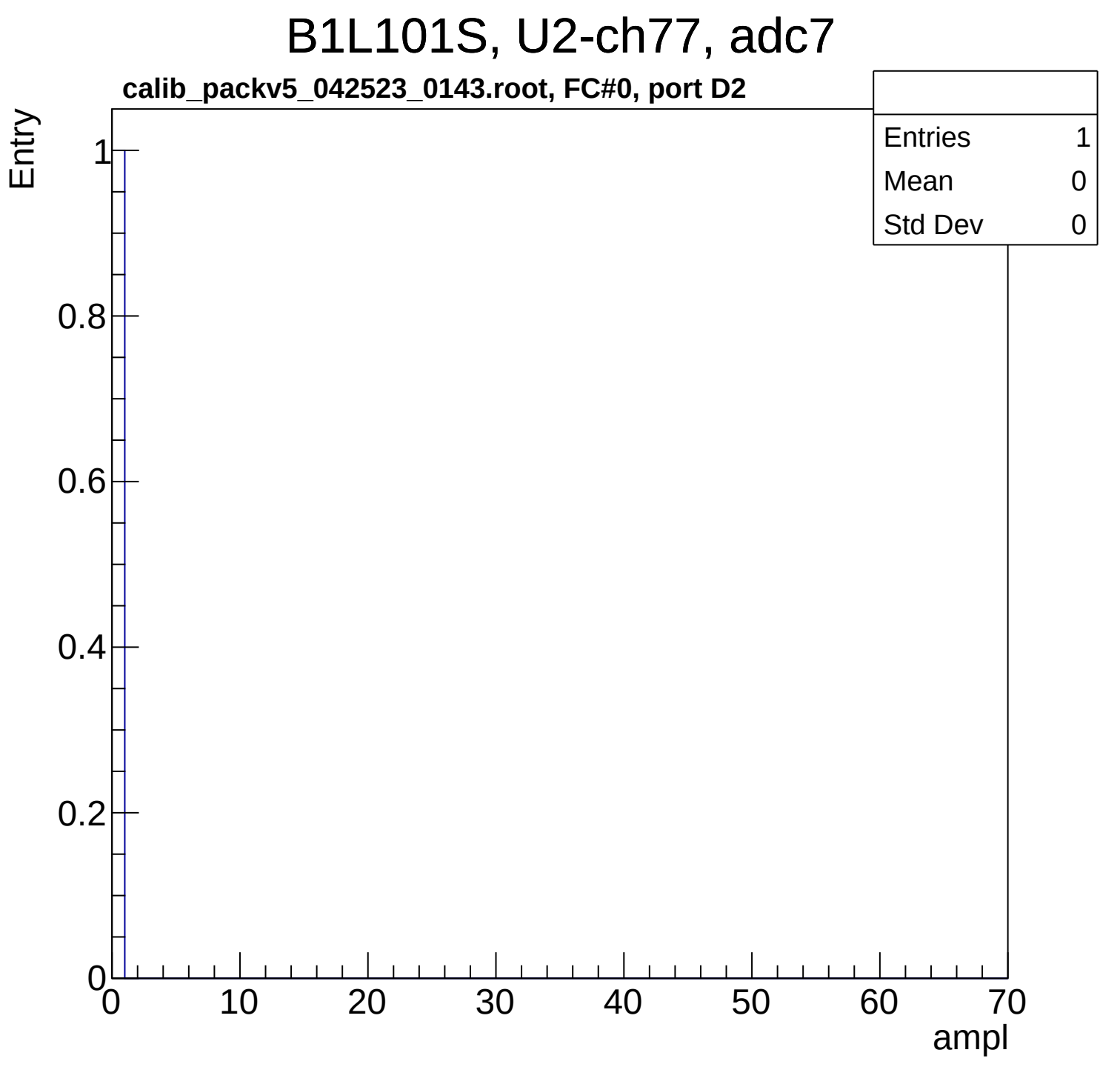

B1L101S, U2-ch77, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 42.24
Std Dev 3.265
Gaus mean : 43.5299
Gaus Width: 4.4070
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

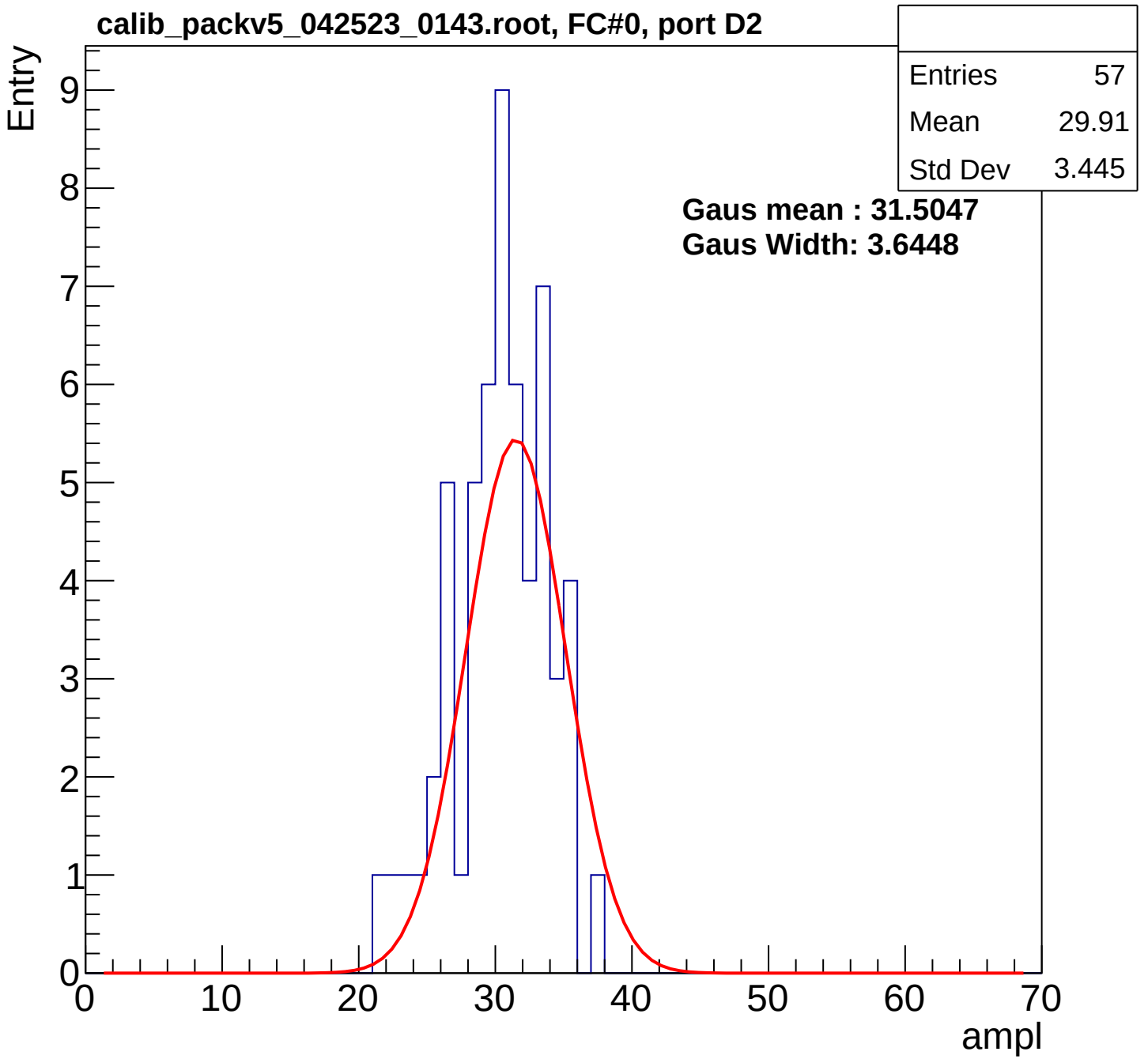

B1L101S, U2-ch77, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 48.89
Std Dev 3.832
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

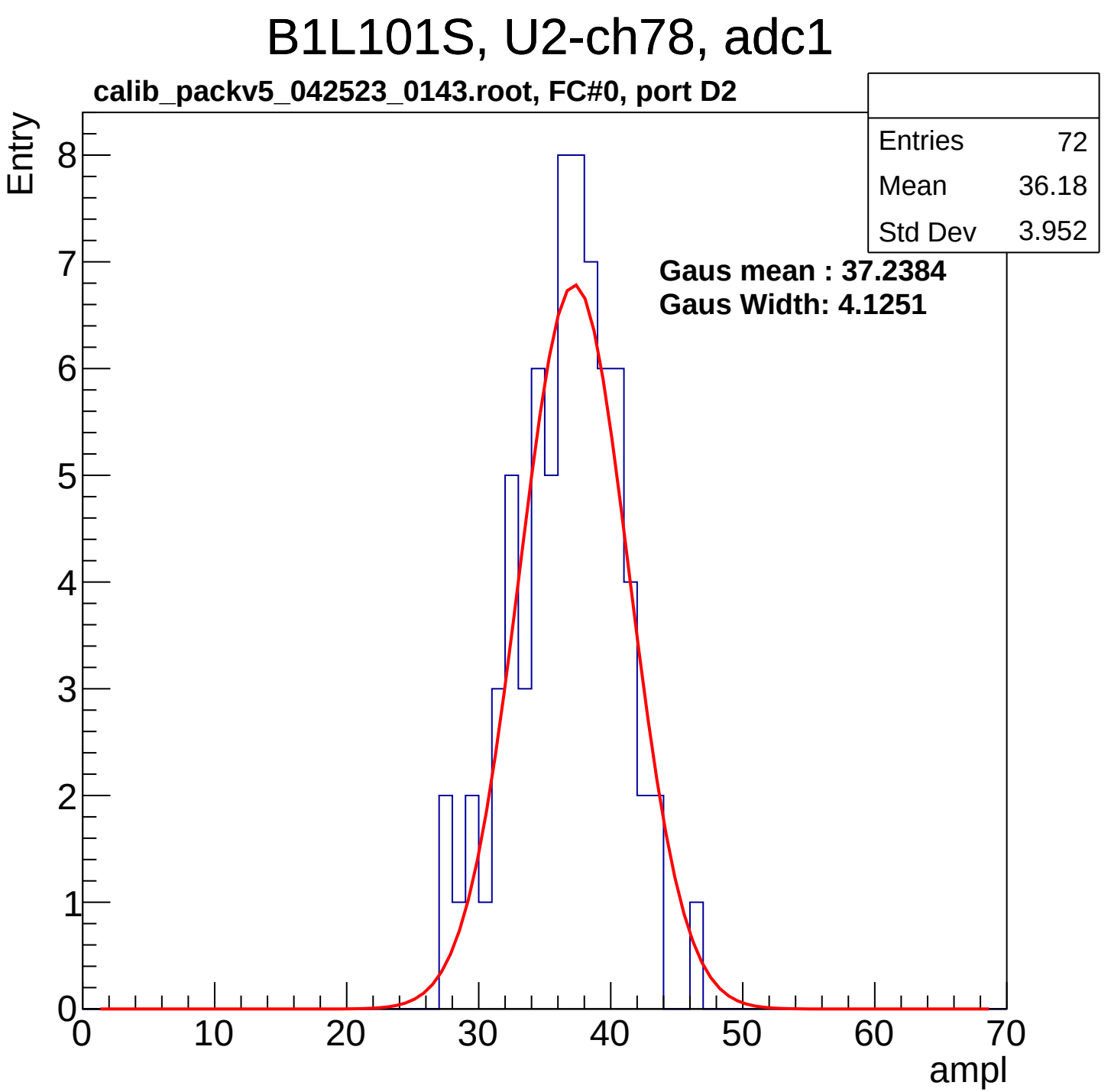

B1L101S, U2-ch77, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 54.04
Std Dev 3.336
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

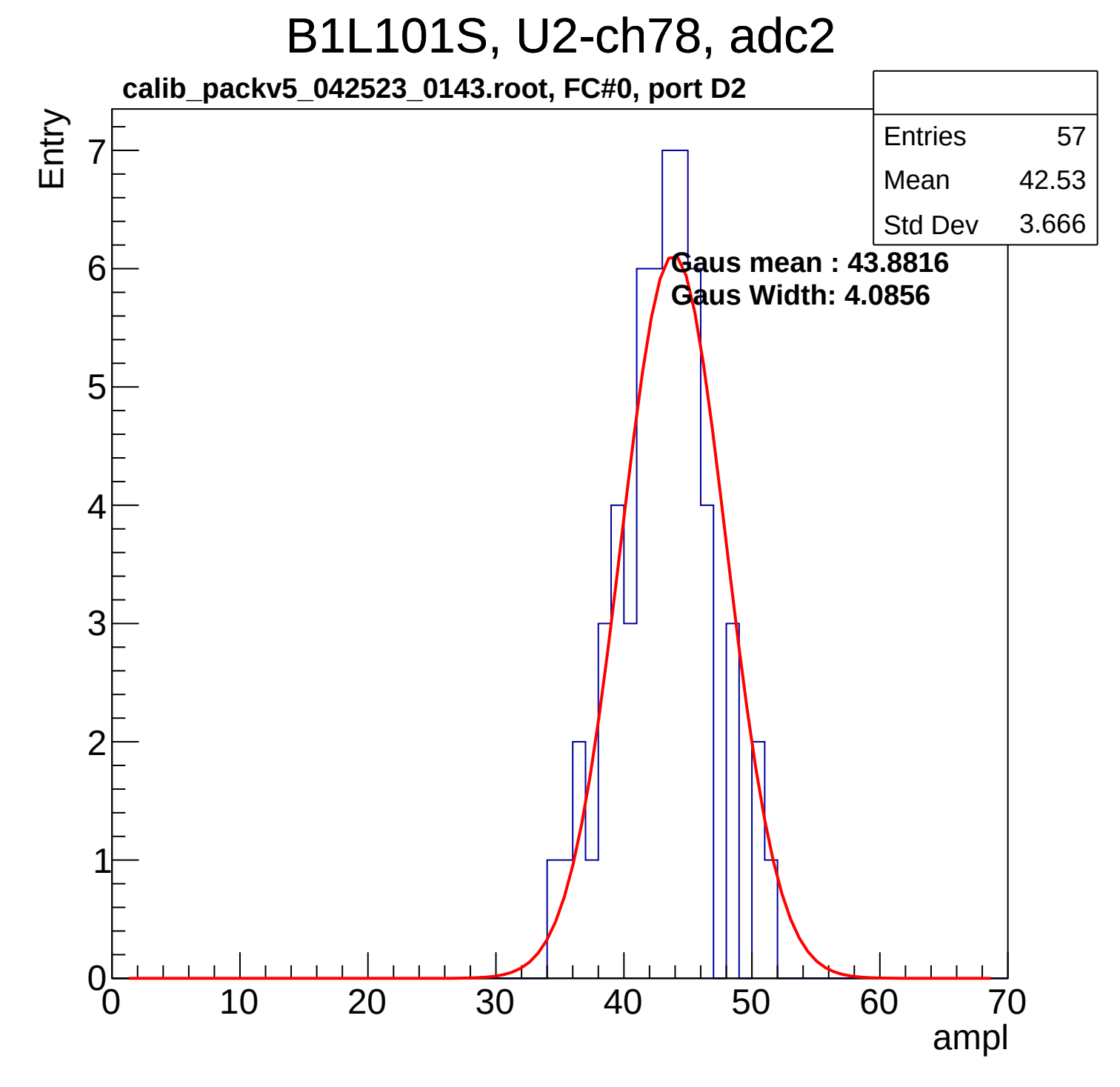

B1L101S, U2-ch77, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 58.02
Std Dev 8.568
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

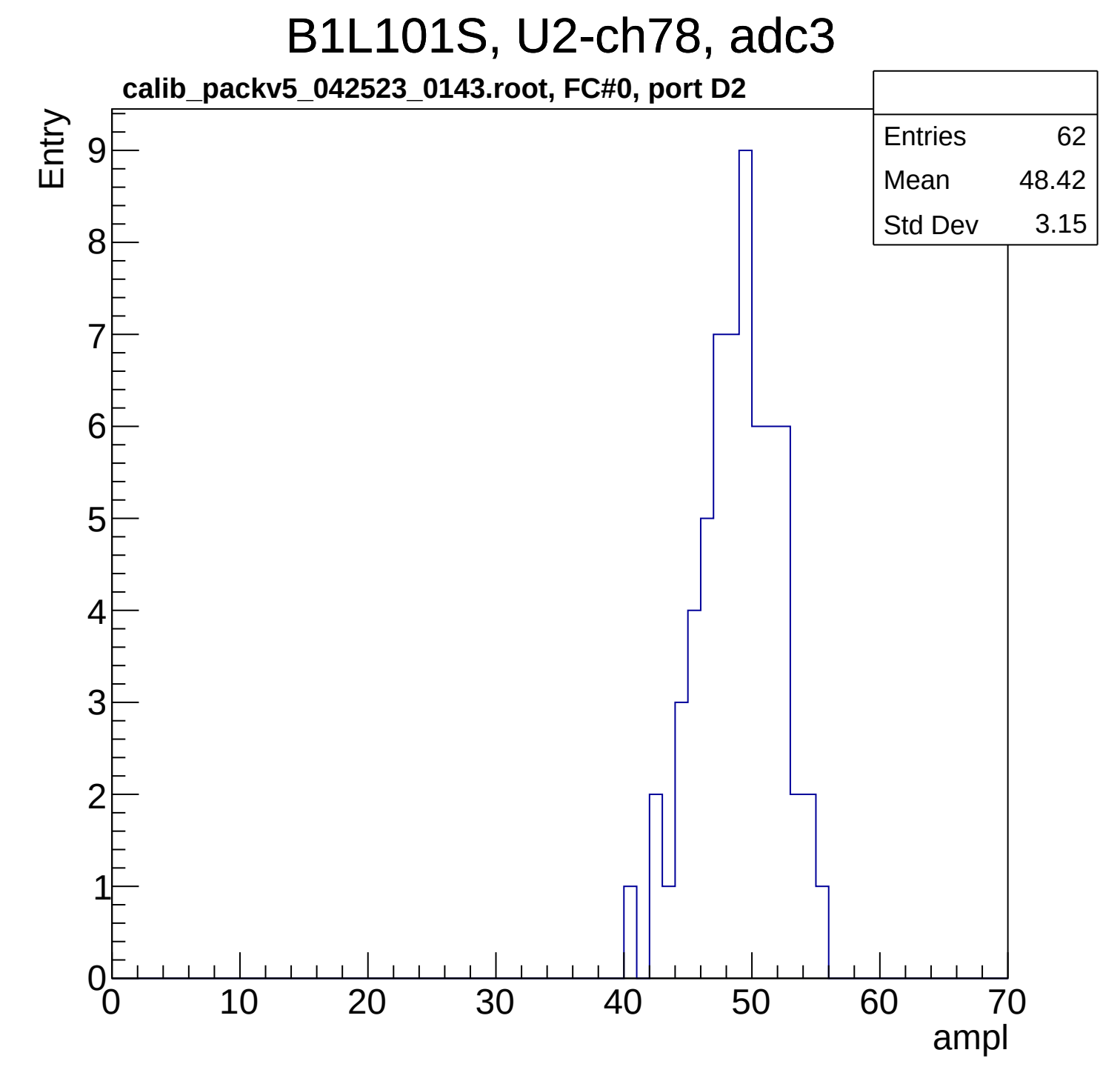

B1L101S, U2-ch77, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 13
Mean 61.15
Std Dev 1.511
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

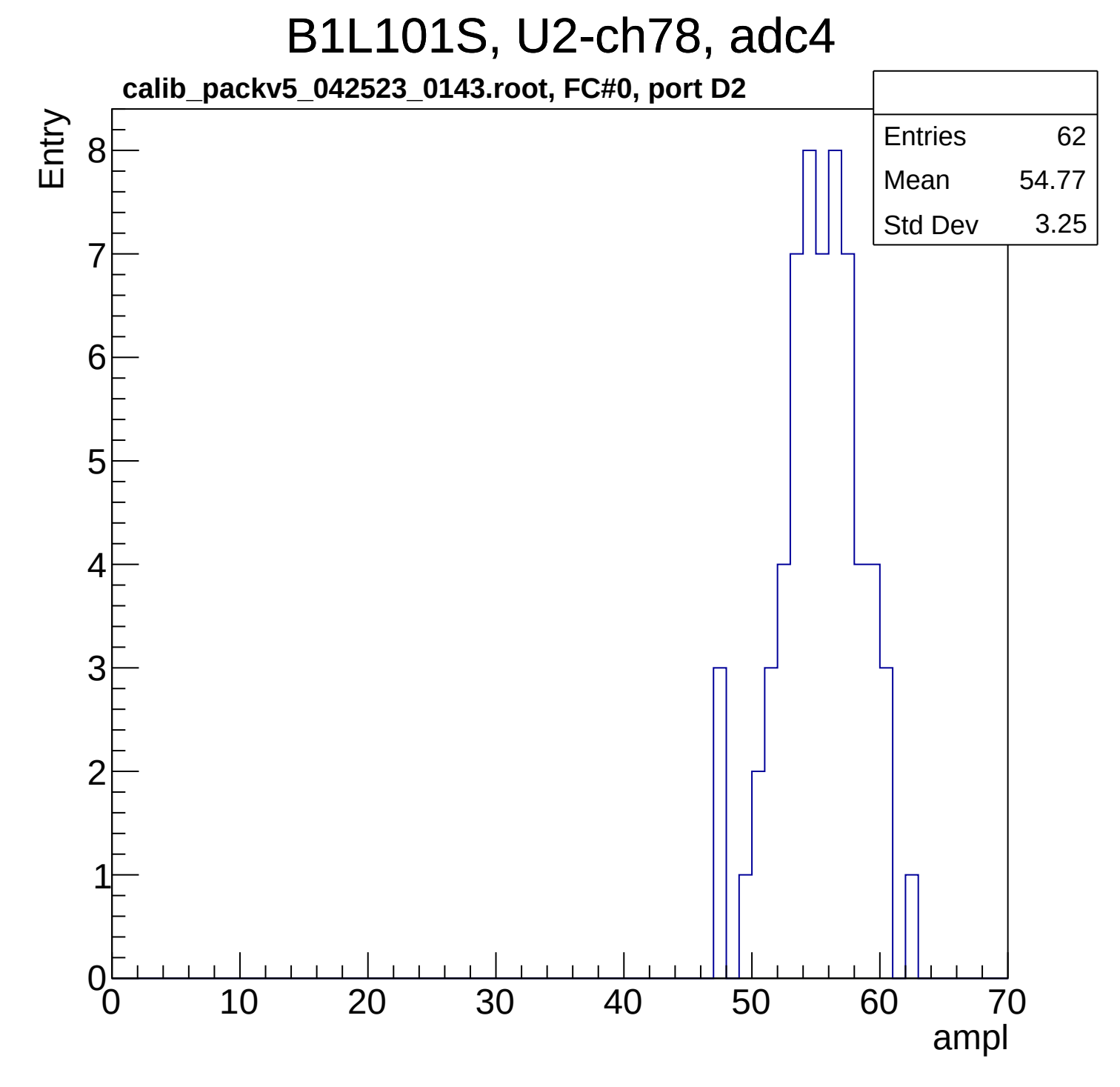

B1L101S, U2-ch77, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

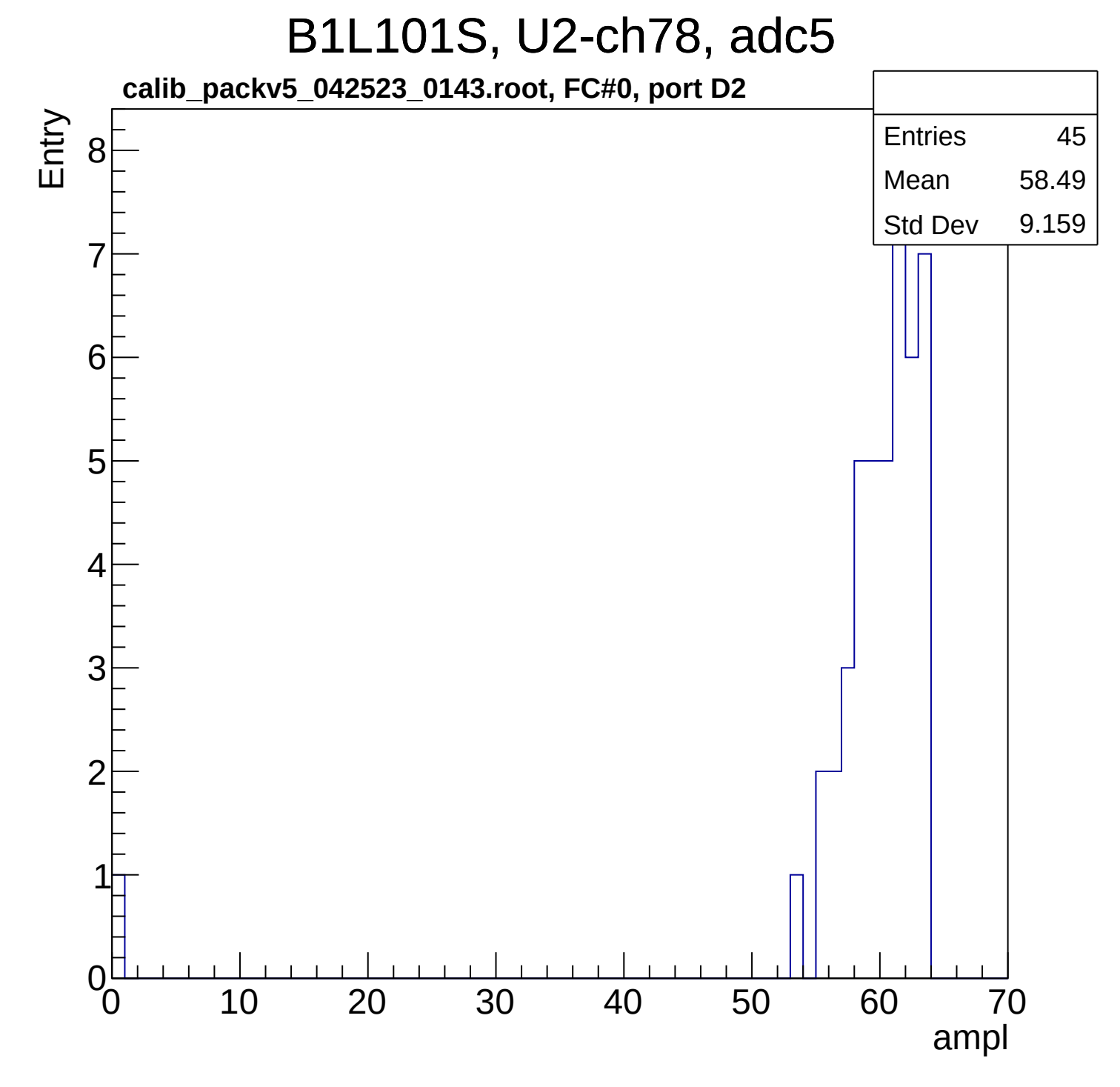

B1L101S, U2-ch78, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 29.91
Std Dev 3.445
Gaus mean : 31.5047
Gaus Width: 3.6448
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

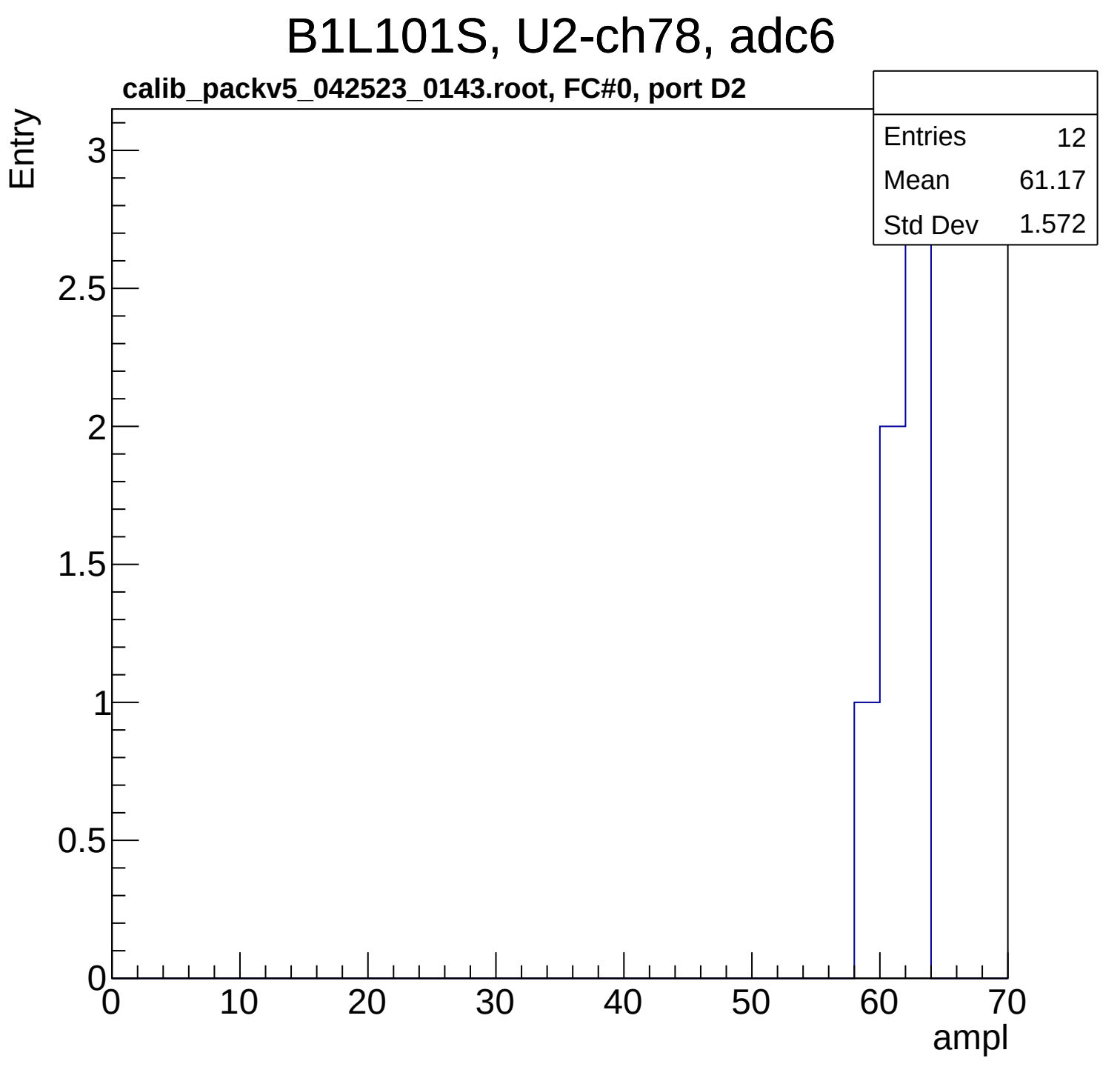

B1L101S, U2-ch78, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 36.18
Std Dev 3.952
Gaus mean : 37.2384
Gaus Width: 4.1251
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

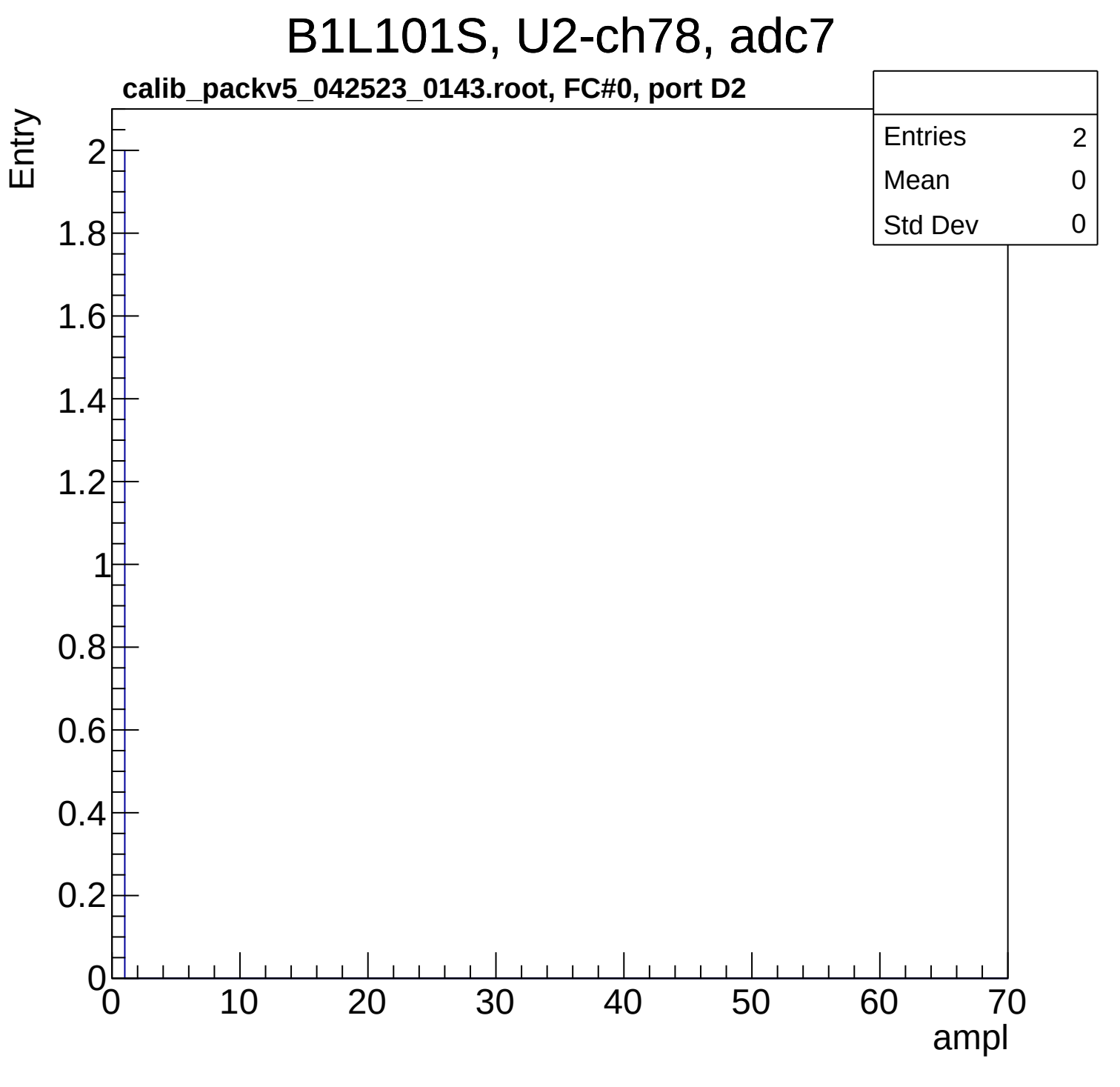

B1L101S, U2-ch78, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 42.53
Std Dev 3.666
Gaus mean : 43.8816
Gaus Width: 4.0856
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

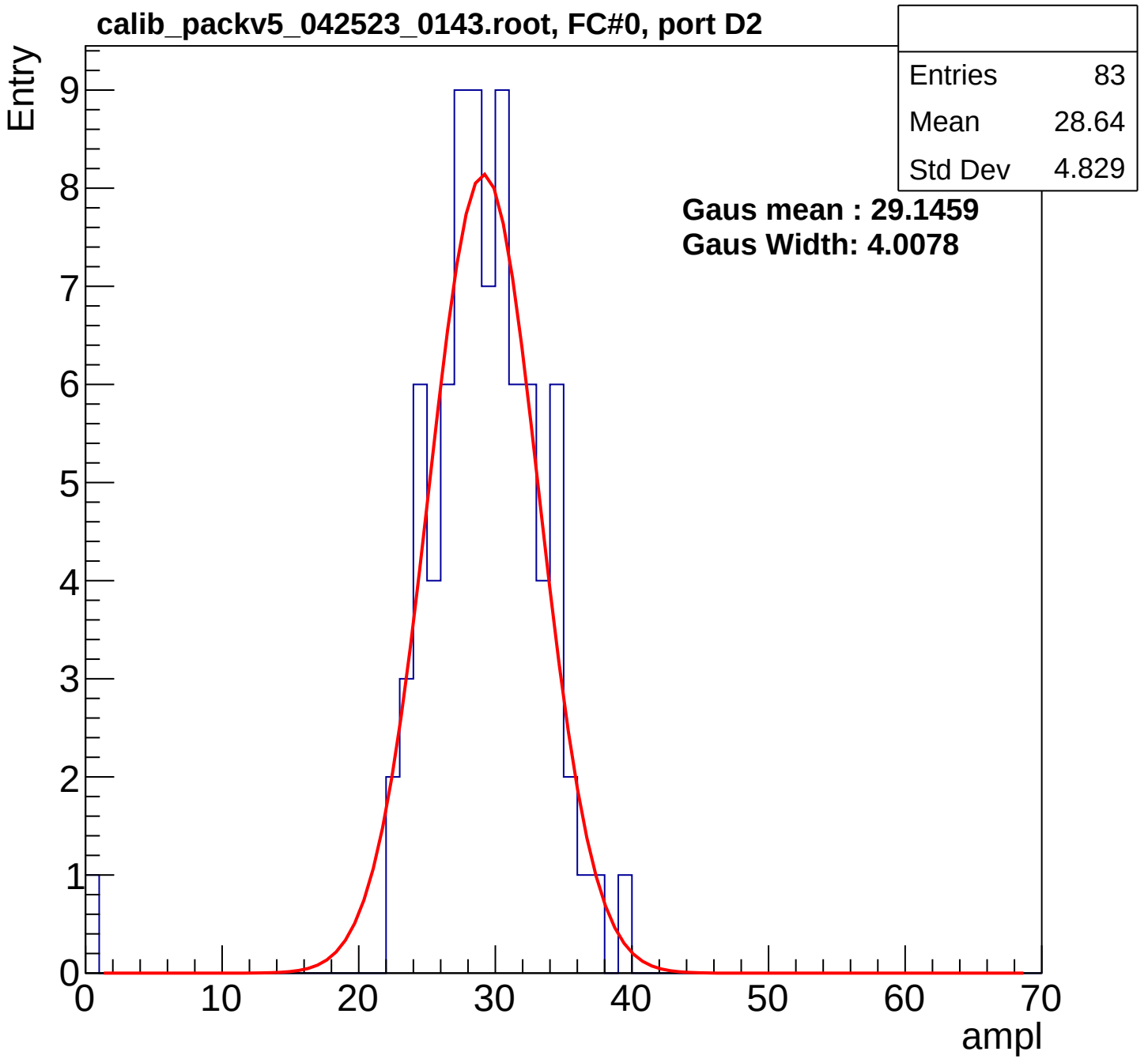

B1L101S, U2-ch78, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 48.42
Std Dev 3.15
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

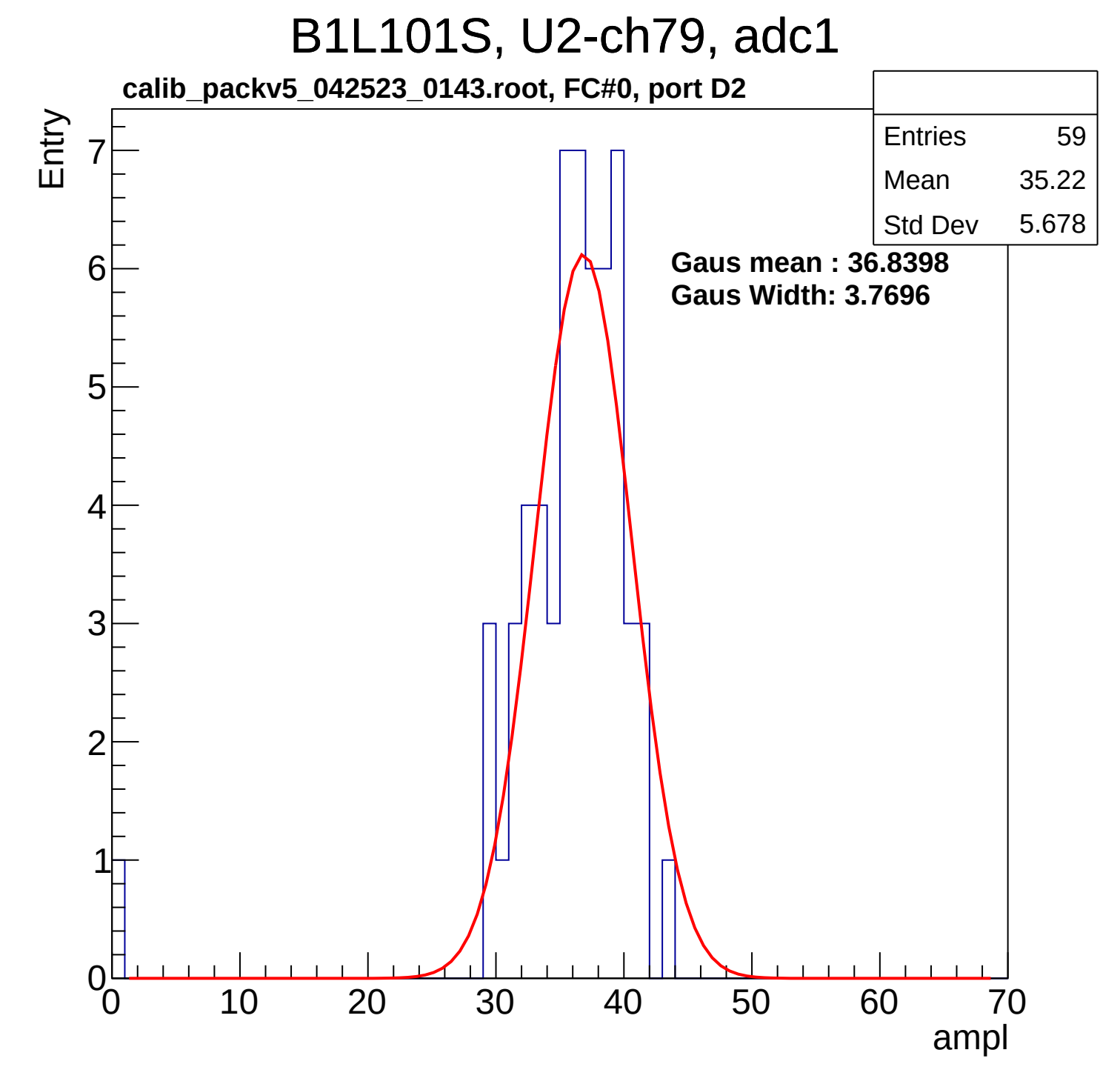

B1L101S, U2-ch78, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 54.77
Std Dev 3.25
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

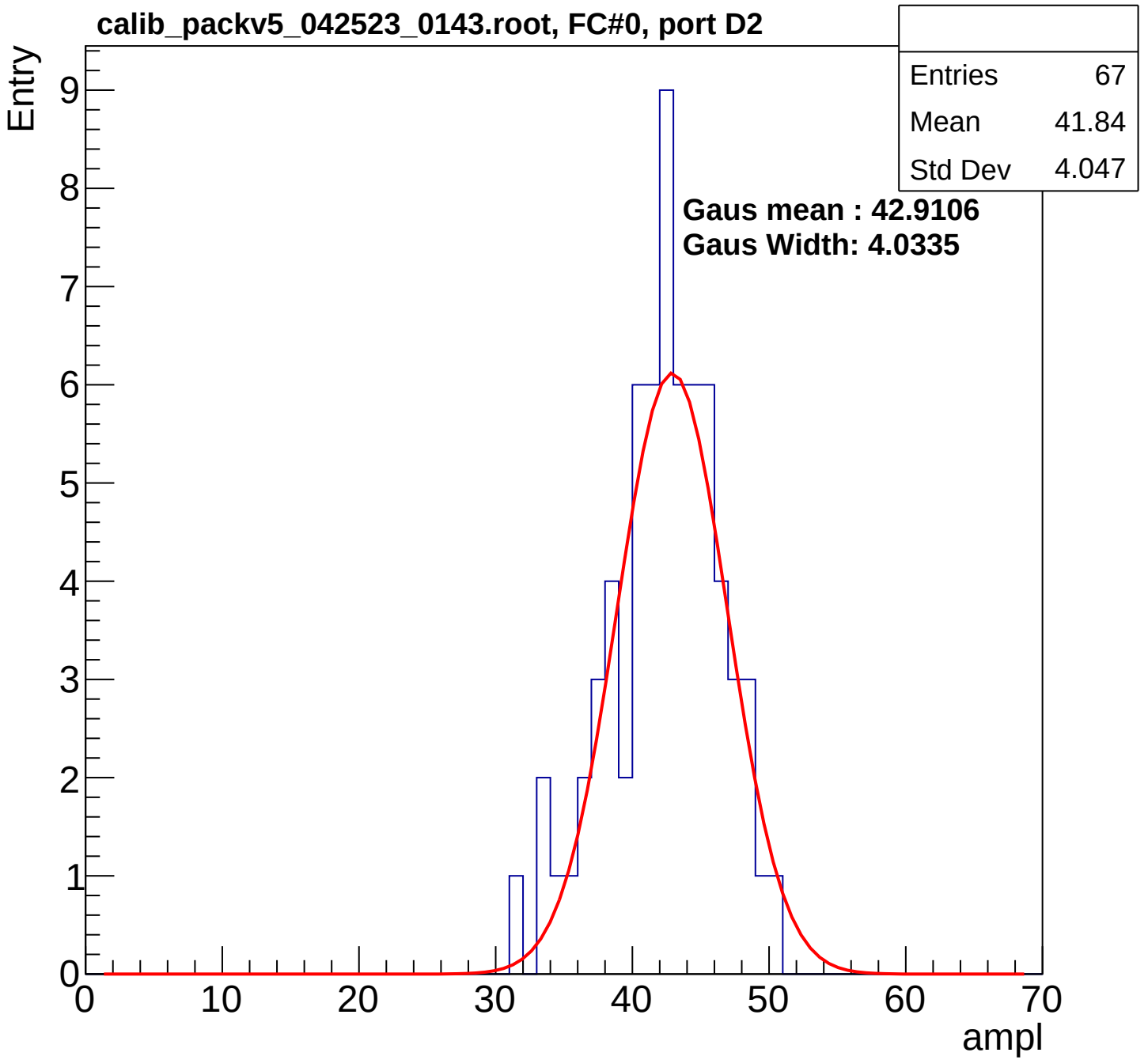

B1L101S, U2-ch78, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 58.49
Std Dev 9.159
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

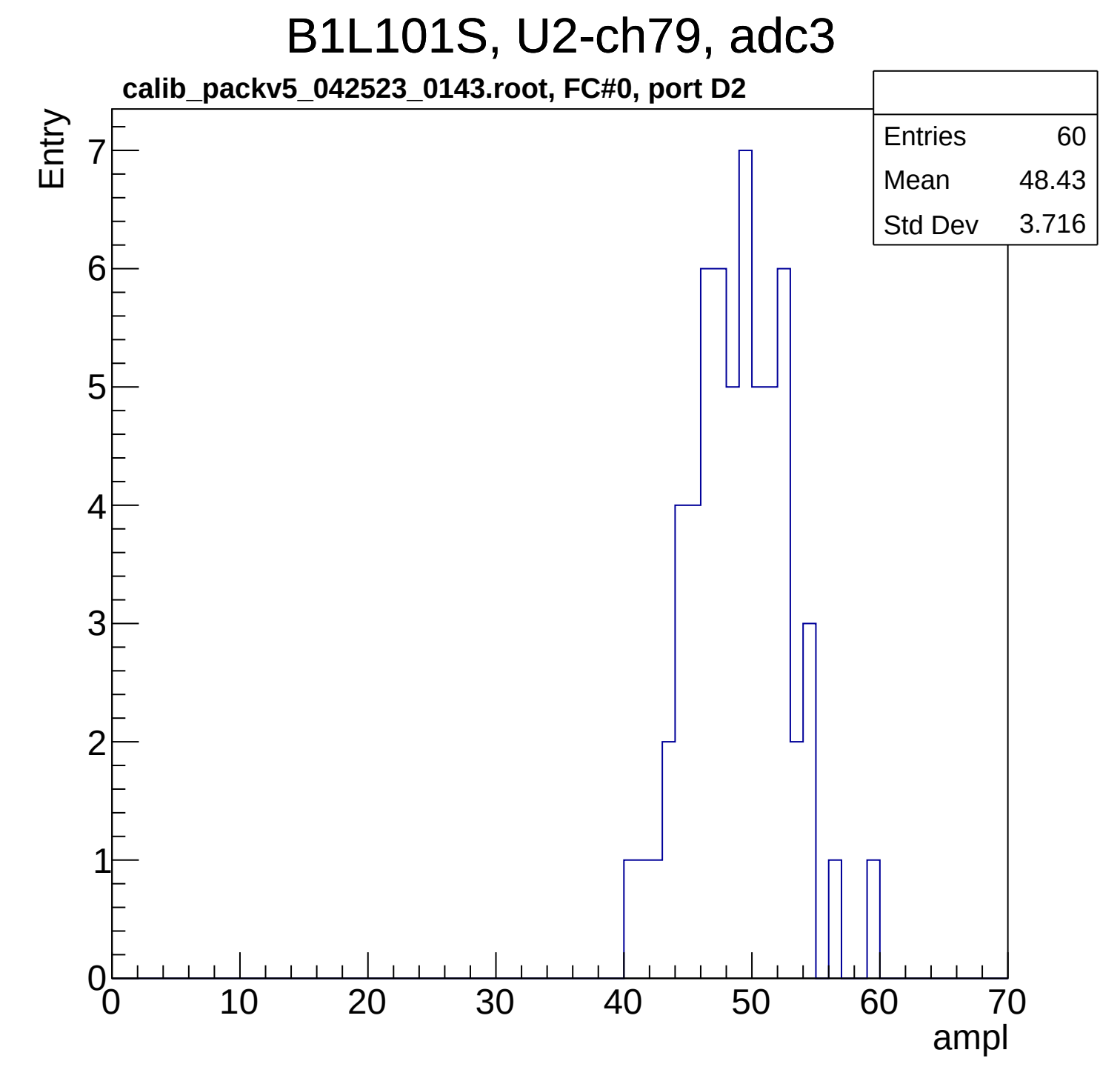

B1L101S, U2-ch78, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 12
Mean 61.17
Std Dev 1.572
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

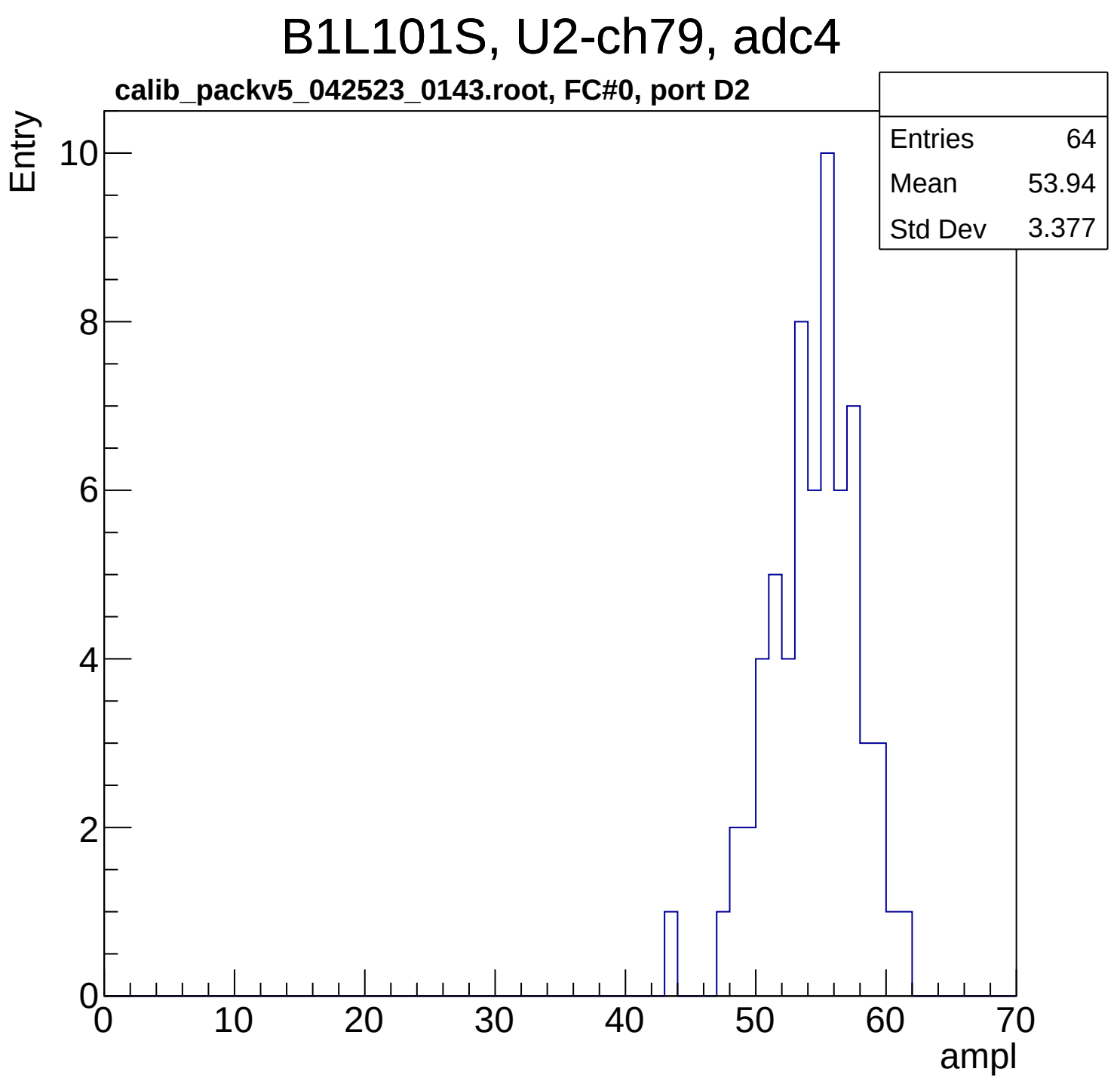

B1L101S, U2-ch78, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

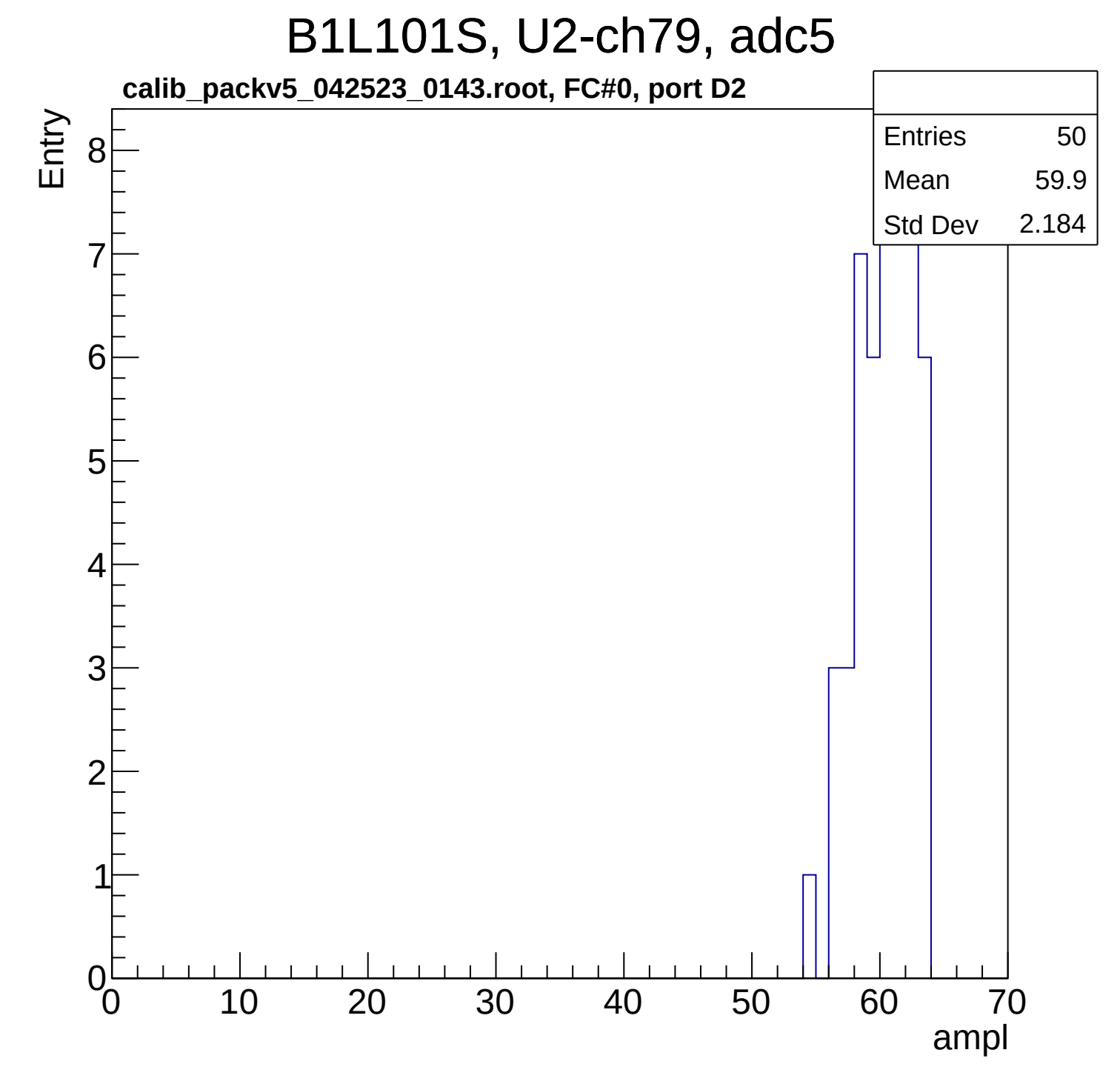

B1L101S, U2-ch79, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 83
Mean 28.64
Std Dev 4.829
Gaus mean : 29.1459
Gaus Width: 4.0078
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

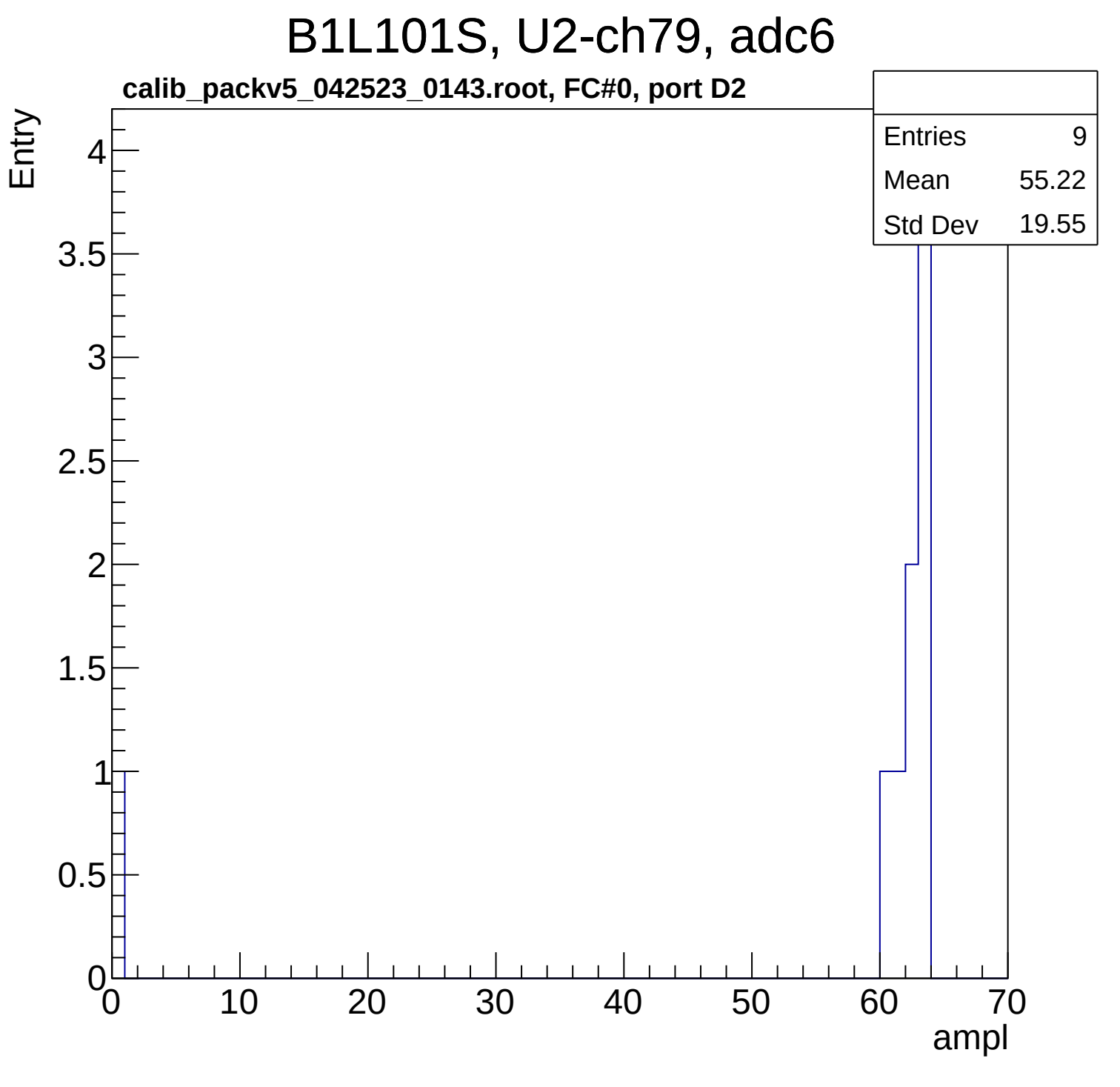

B1L101S, U2-ch79, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 35.22
Std Dev 5.678
Gaus mean : 36.8398
Gaus Width: 3.7696
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

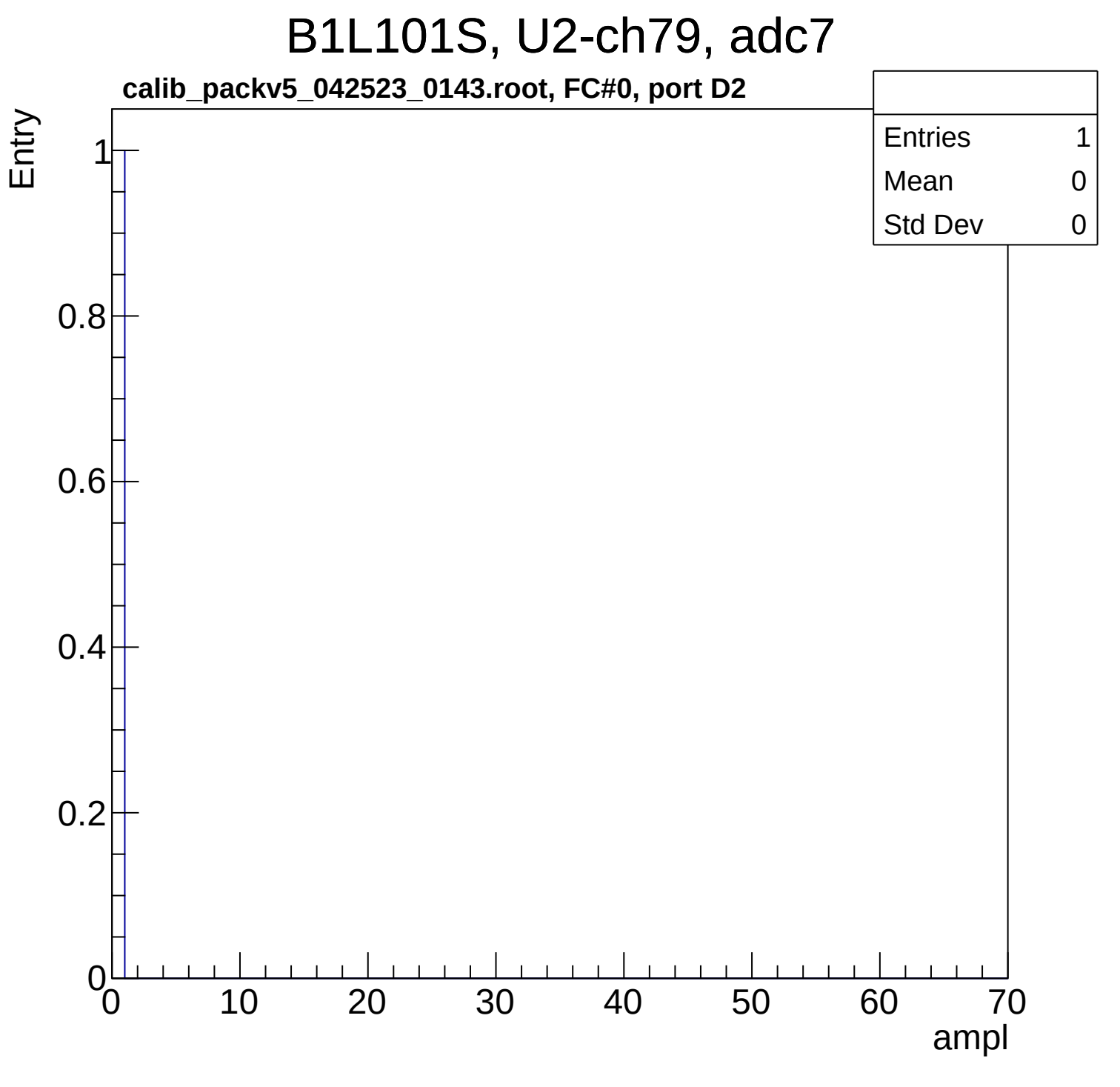

B1L101S, U2-ch79, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 41.84
Std Dev 4.047
Gaus mean : 42.9106
Gaus Width: 4.0335
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

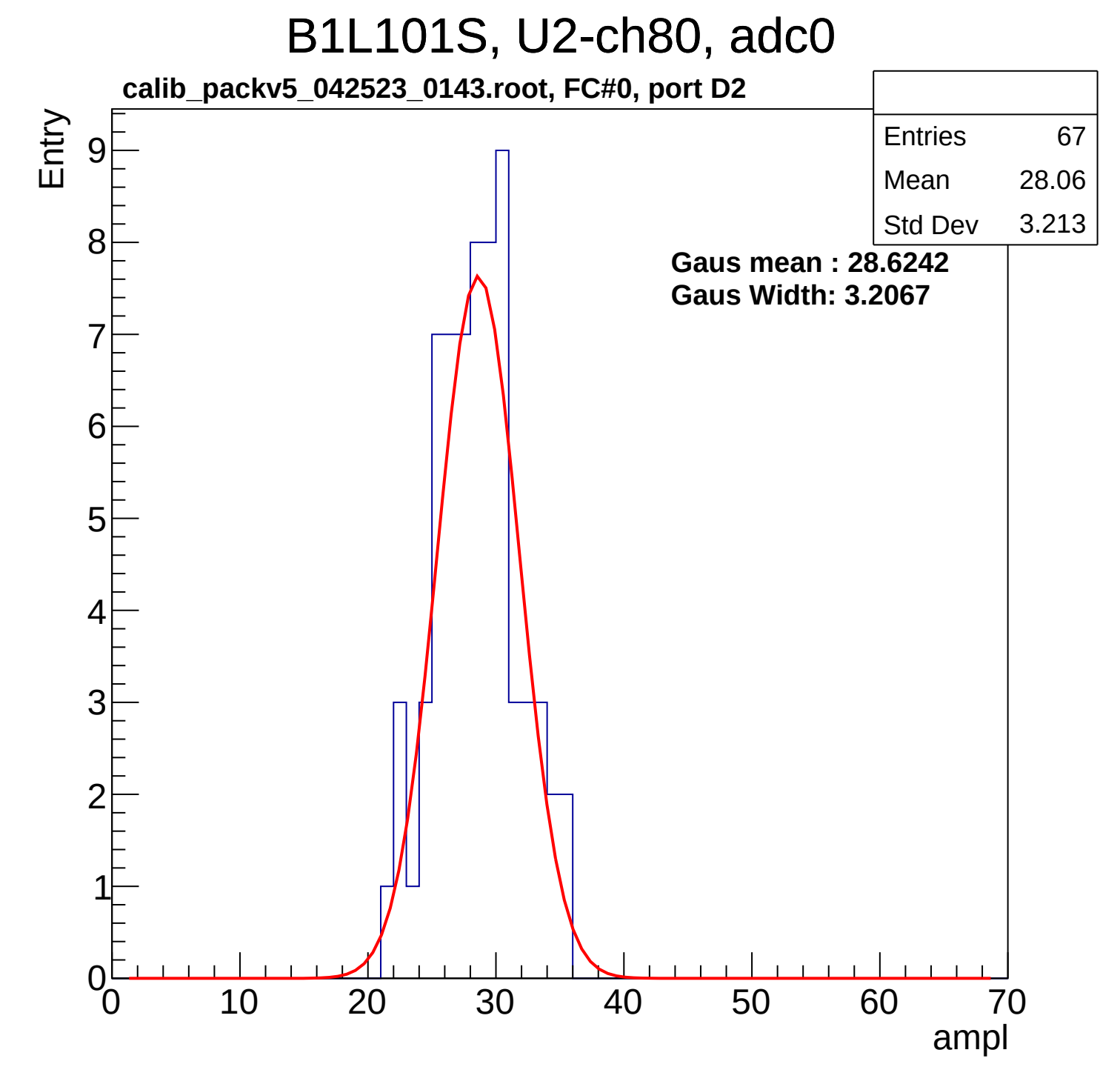

B1L101S, U2-ch79, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 48.43
Std Dev 3.716
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

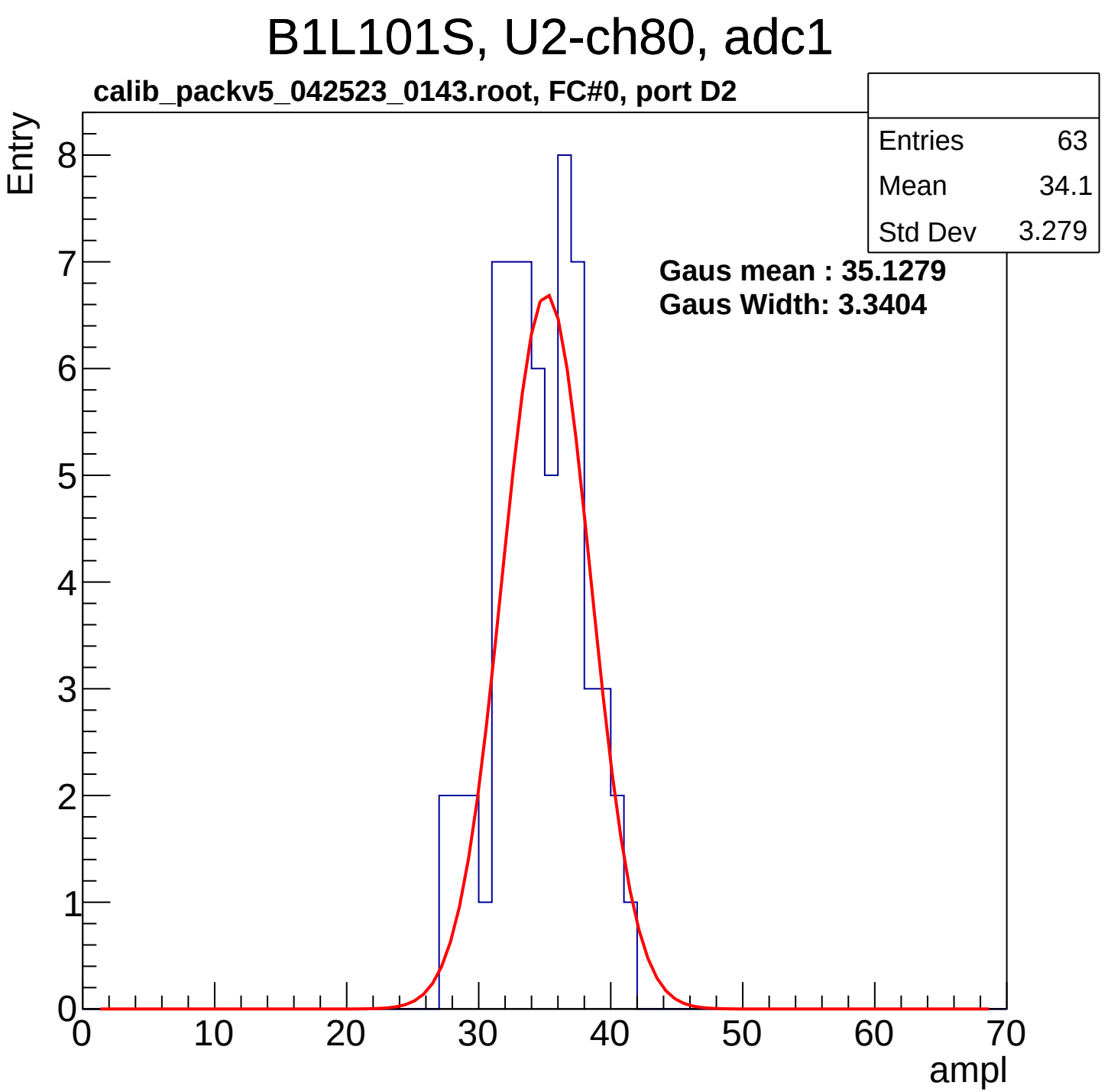

B1L101S, U2-ch79, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 53.94
Std Dev 3.377
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

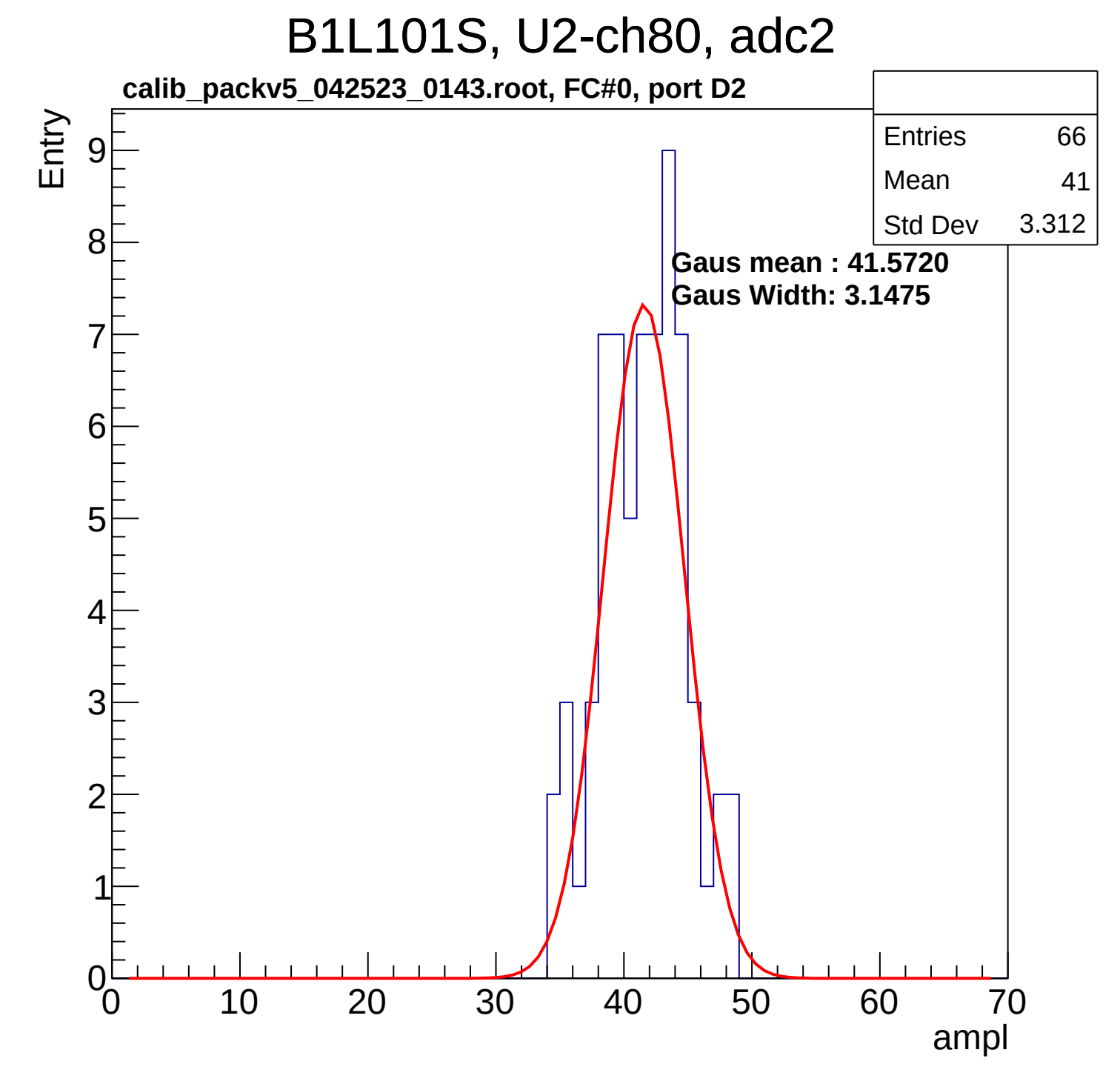

B1L101S, U2-ch79, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 59.9
Std Dev 2.184
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

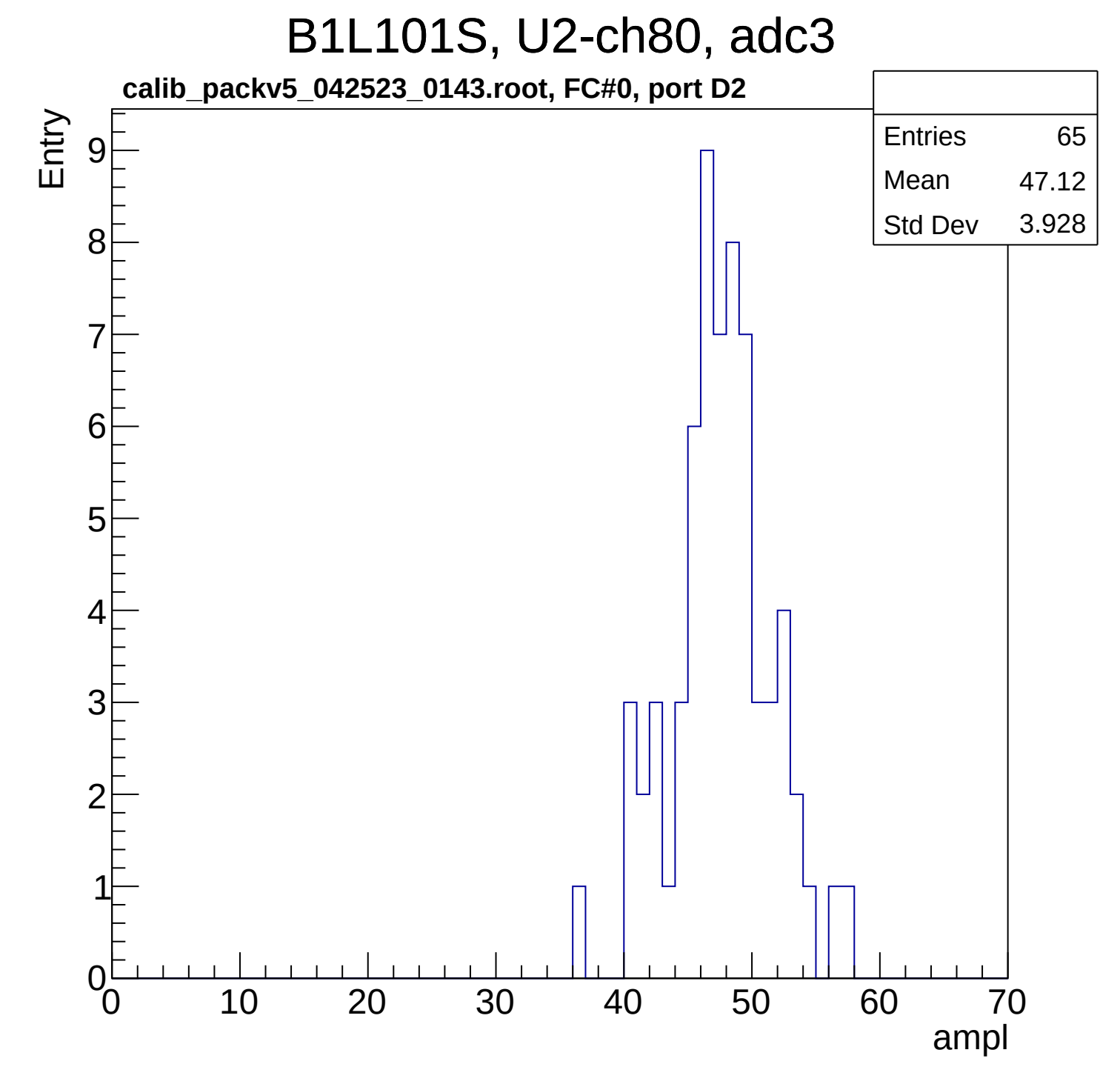

B1L101S, U2-ch79, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 55.22
Std Dev 19.55
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

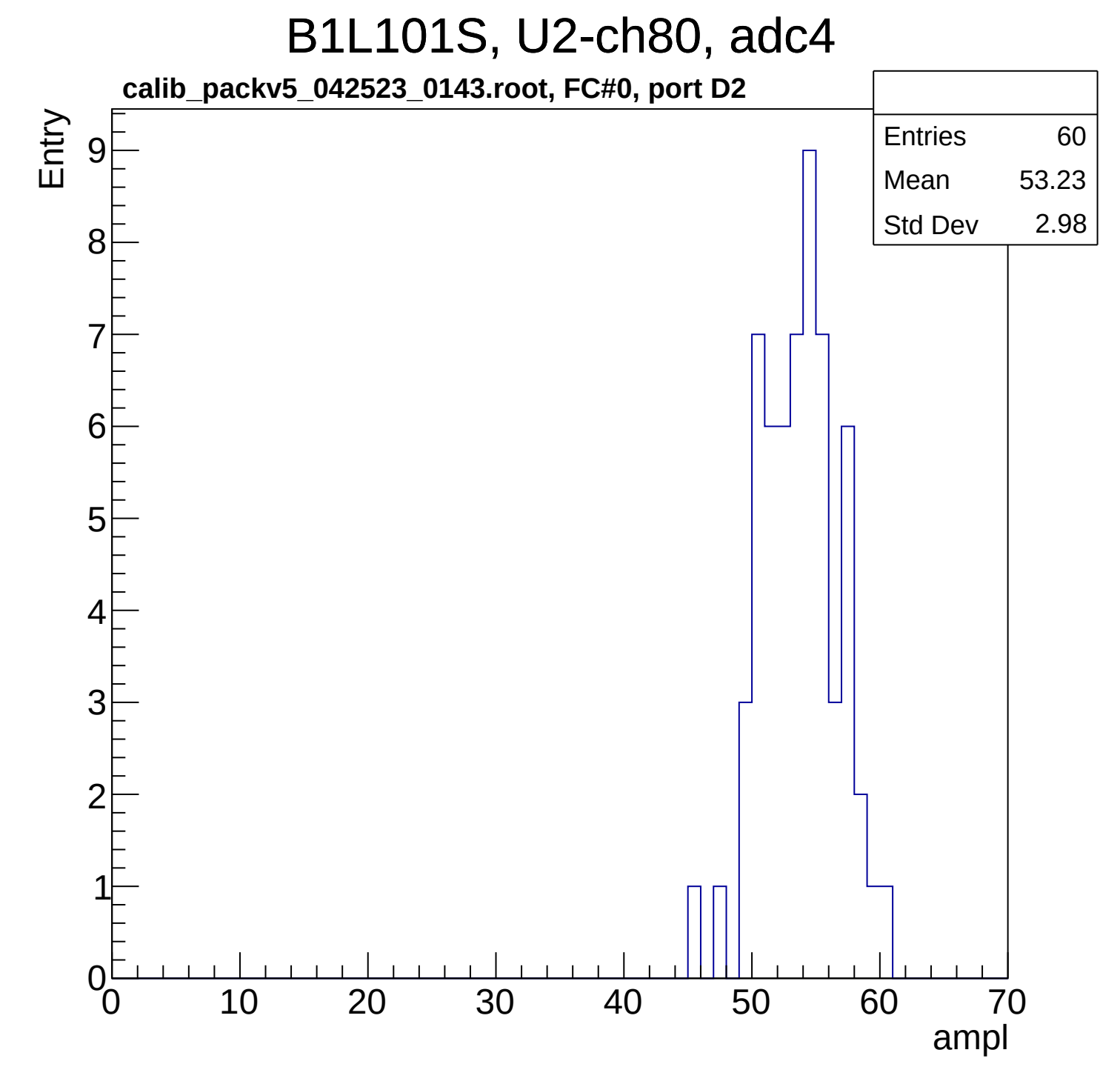

B1L101S, U2-ch79, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

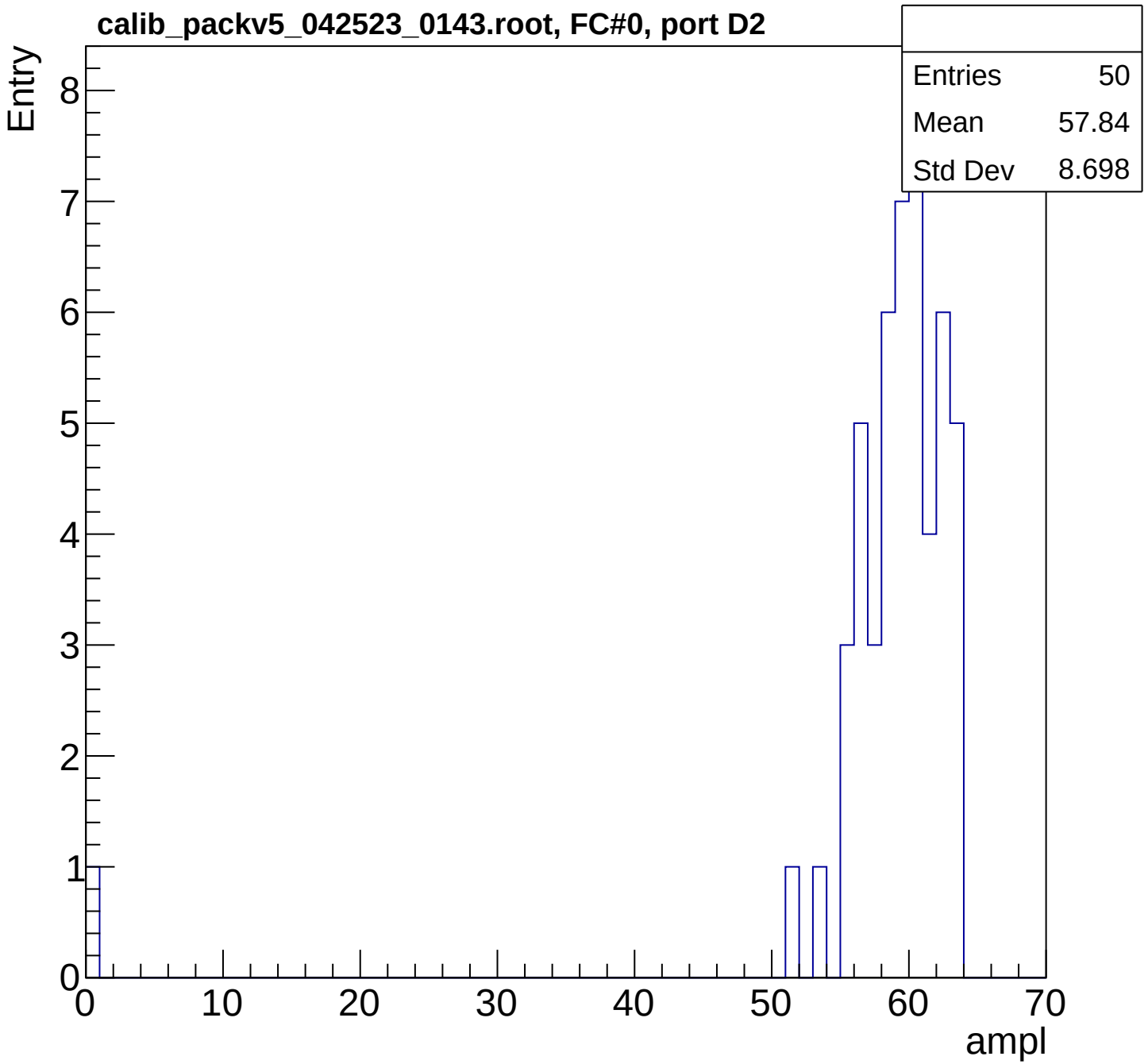

B1L101S, U2-ch80, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 28.06
Std Dev 3.213
Gaus mean : 28.6242
Gaus Width: 3.2067
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

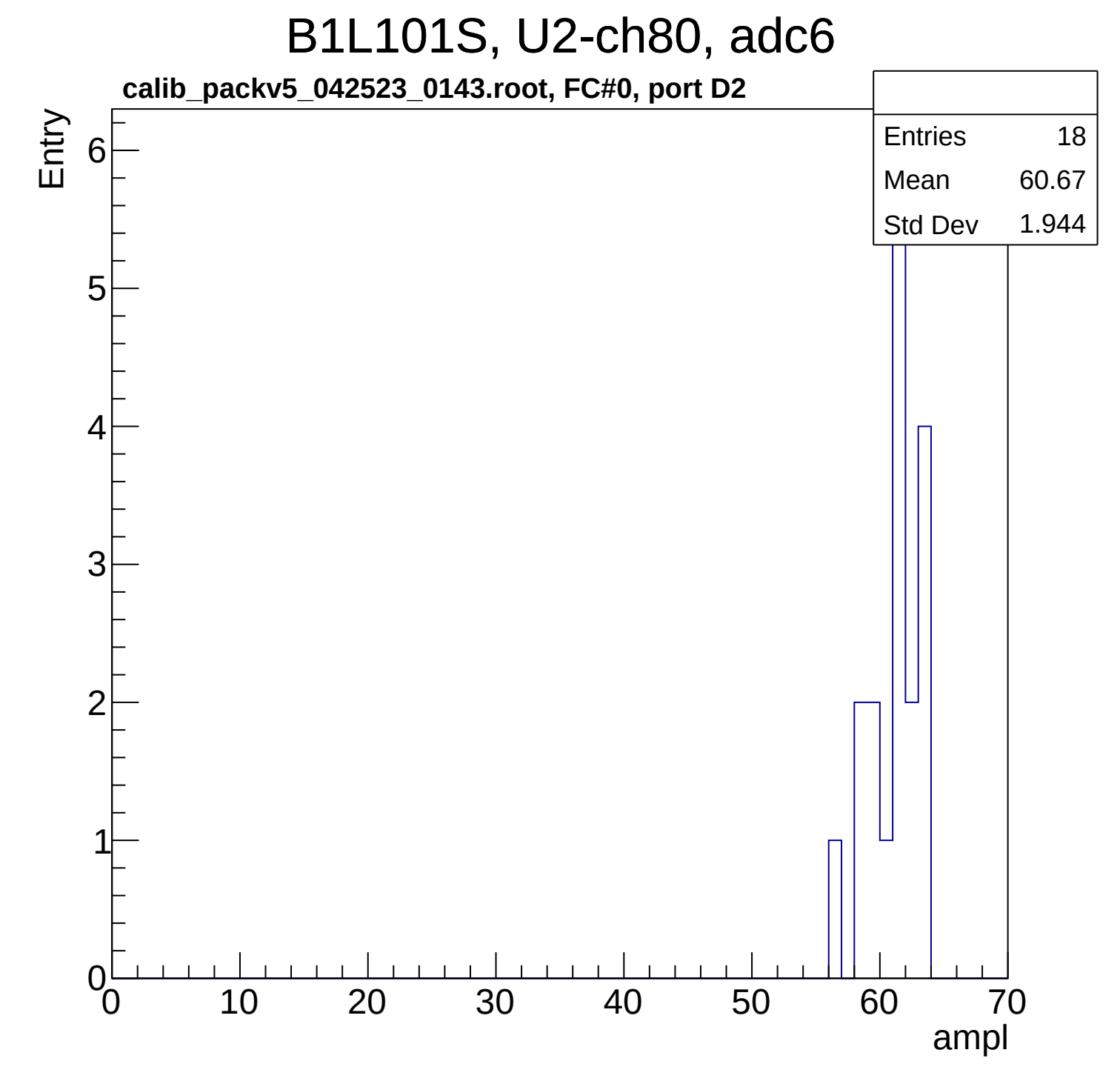

B1L101S, U2-ch80, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 34.1
Std Dev 3.279
Gaus mean : 35.1279
Gaus Width: 3.3404
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

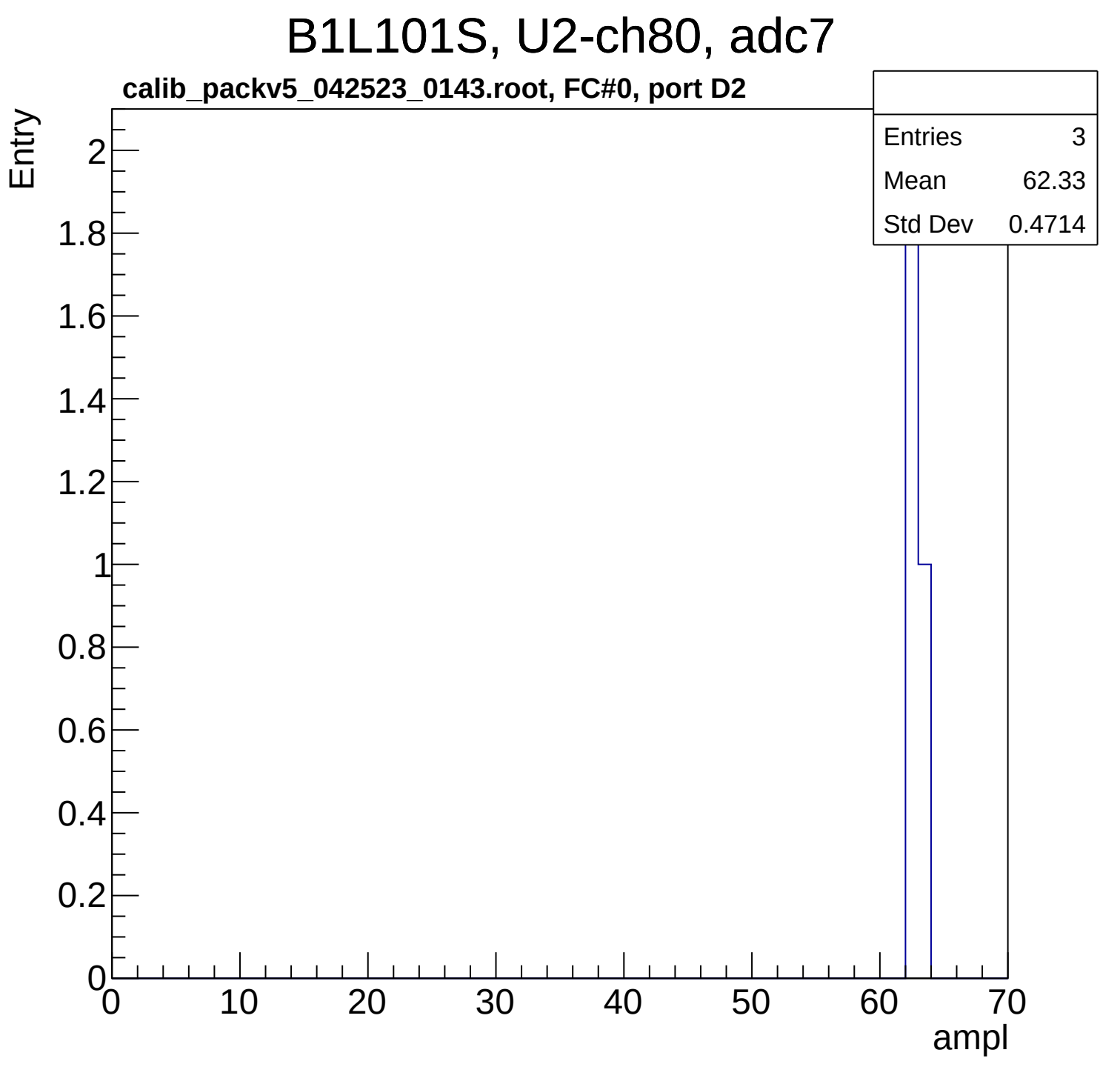

B1L101S, U2-ch80, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 41
Std Dev 3.312
Gaus mean : 41.5720
Gaus Width: 3.1475
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

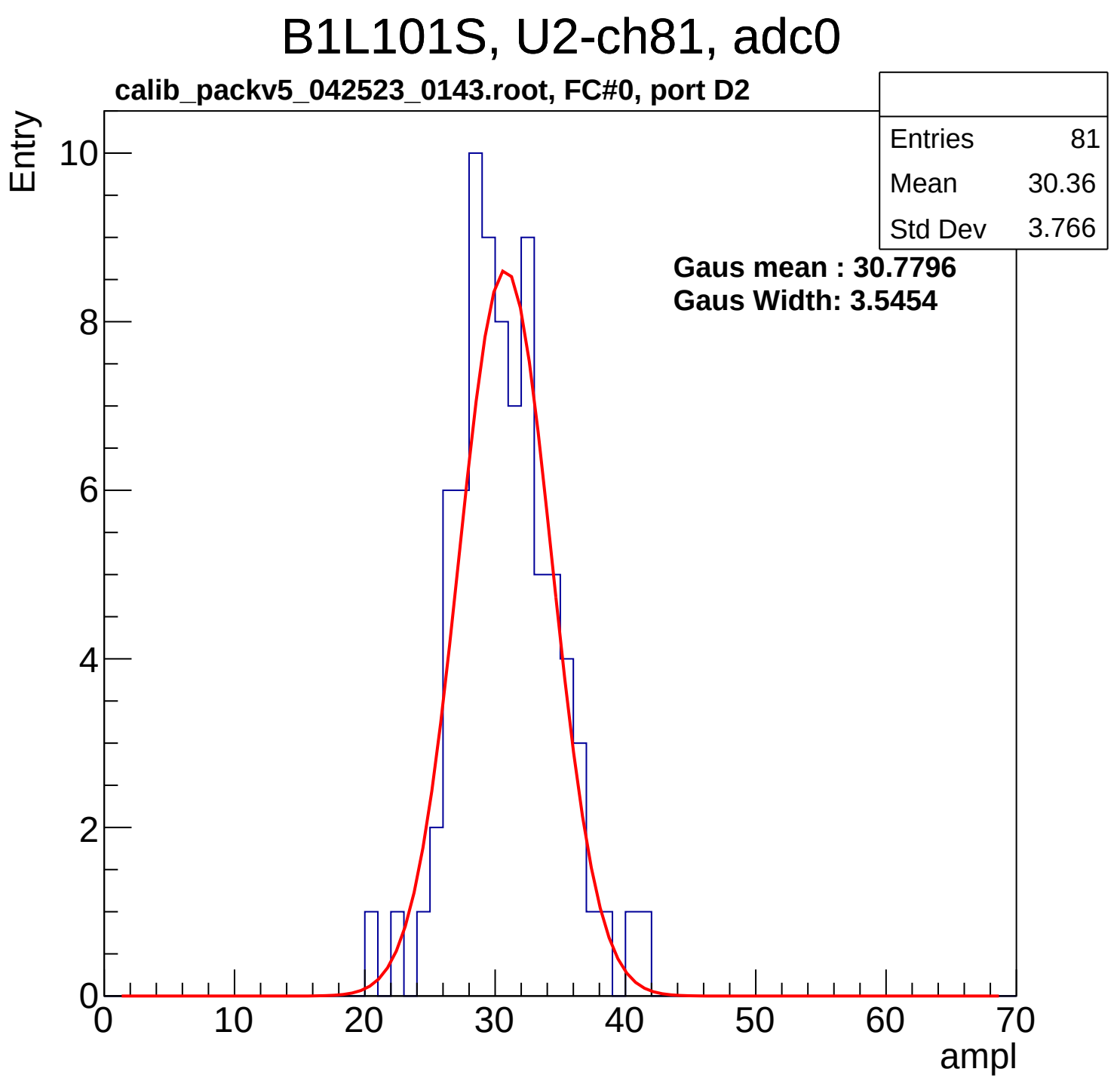

B1L101S, U2-ch80, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 47.12
Std Dev 3.928
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

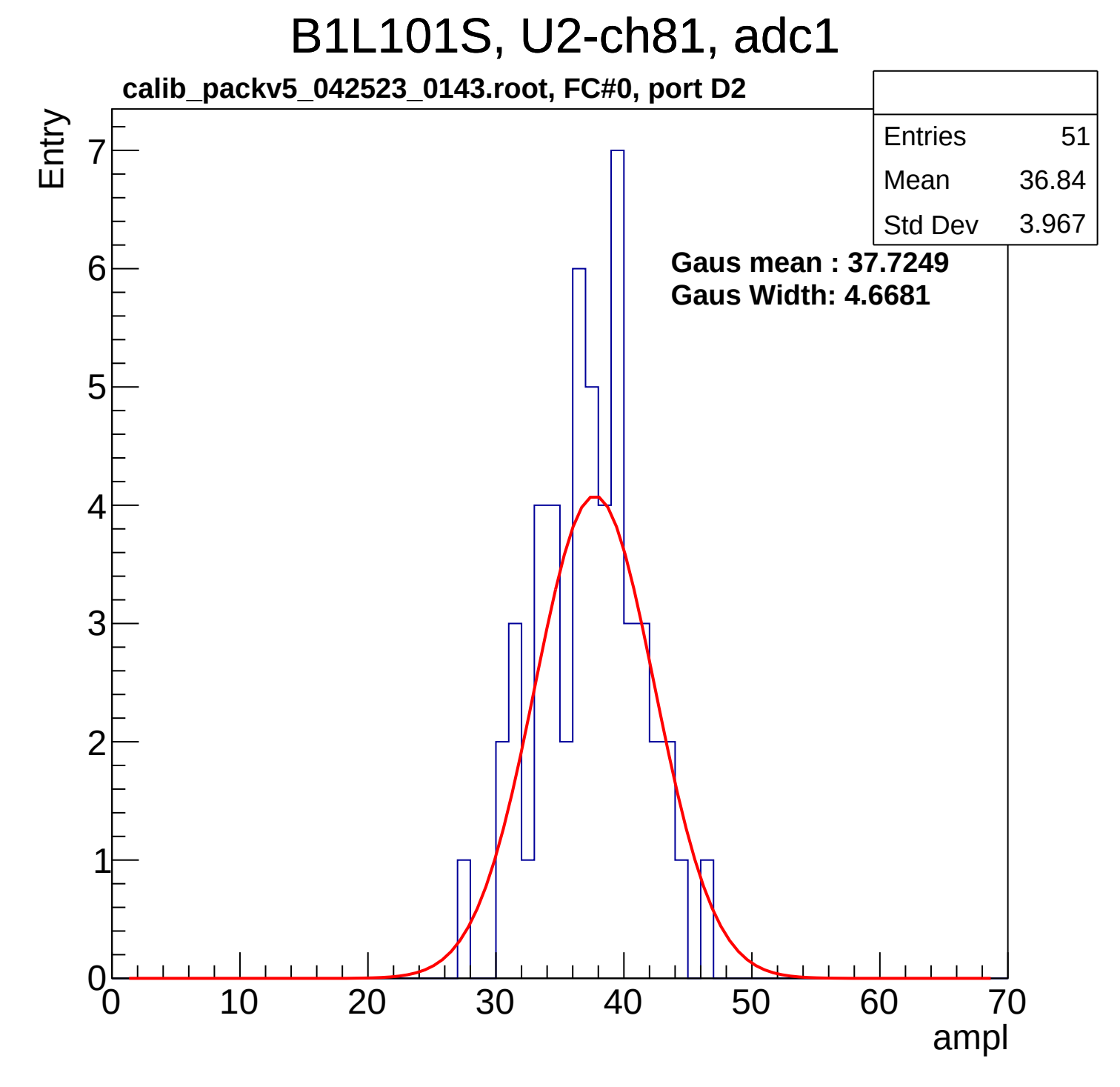

B1L101S, U2-ch80, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 53.23
Std Dev 2.98
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

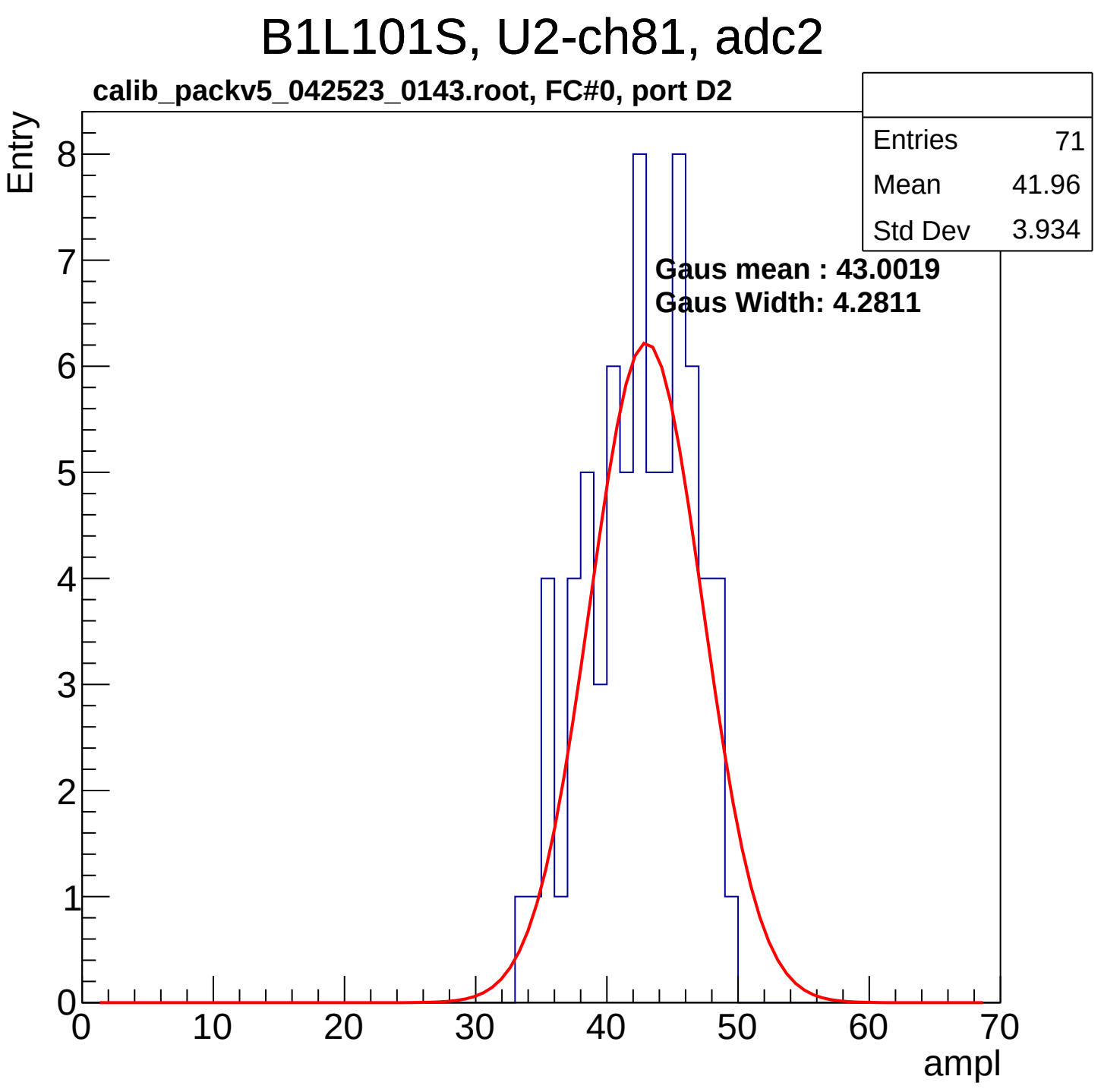

B1L101S, U2-ch80, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 57.84
Std Dev 8.698
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

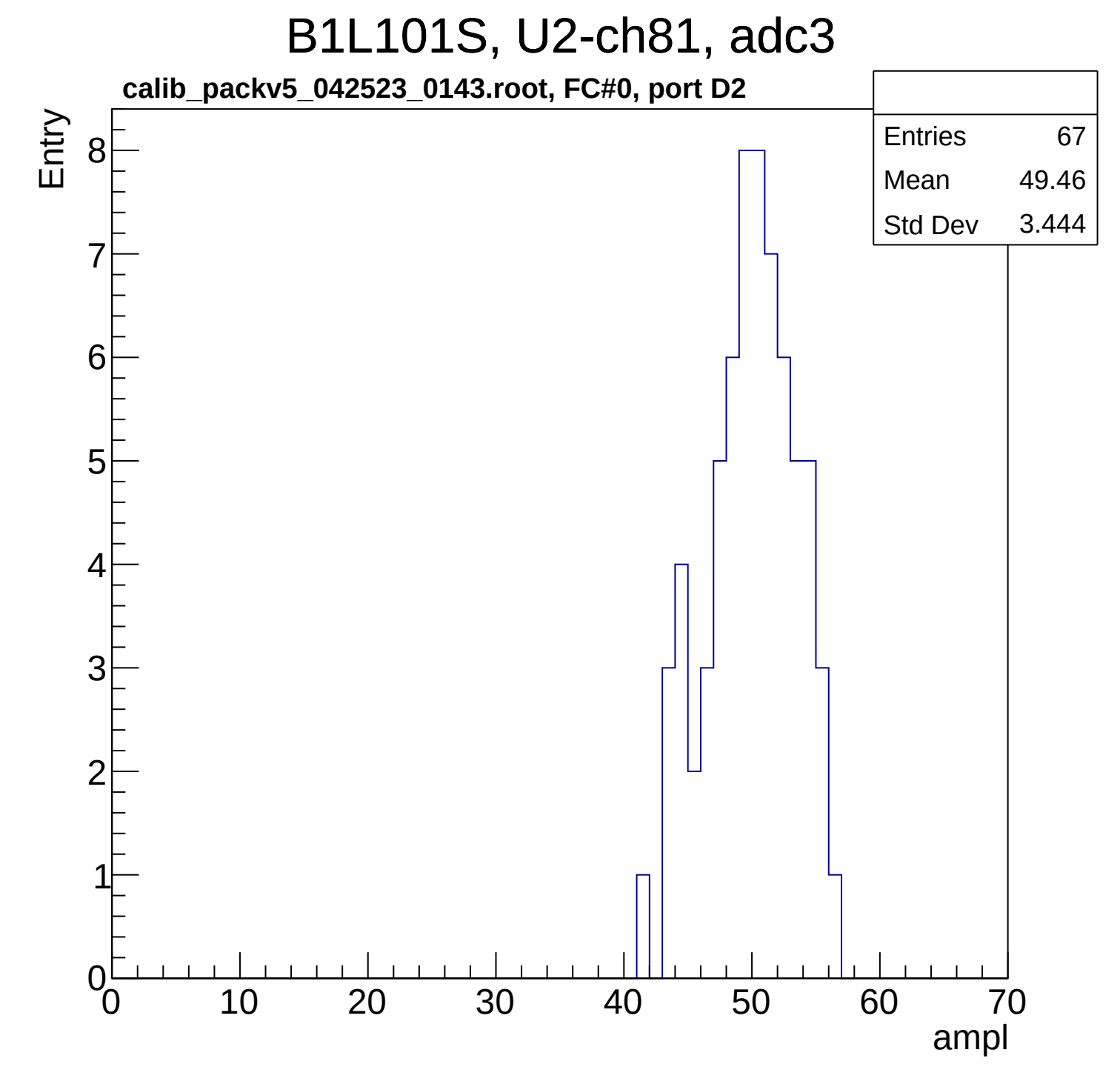

B1L101S, U2-ch80, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 18
Mean 60.67
Std Dev 1.944
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

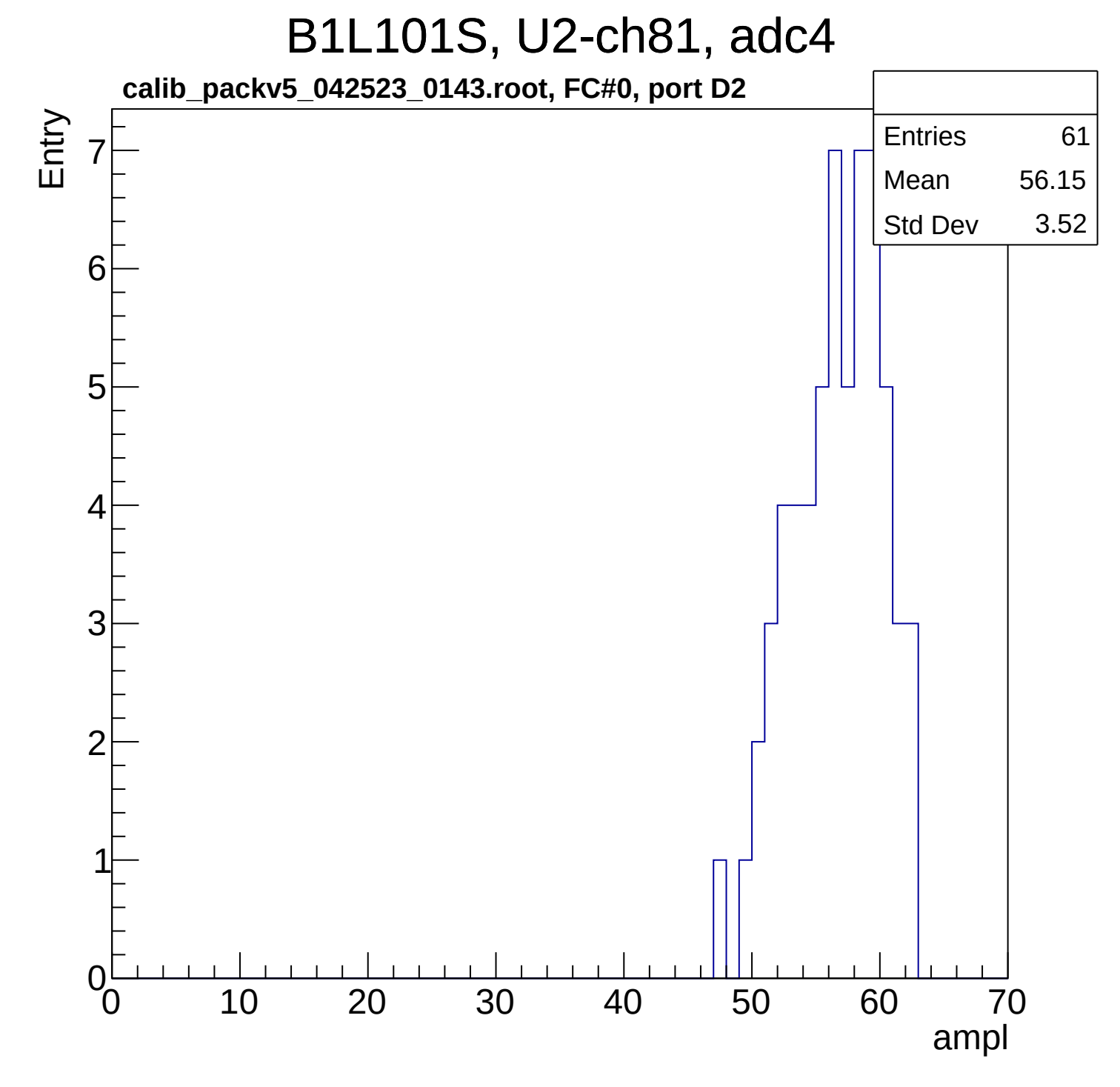

B1L101S, U2-ch80, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

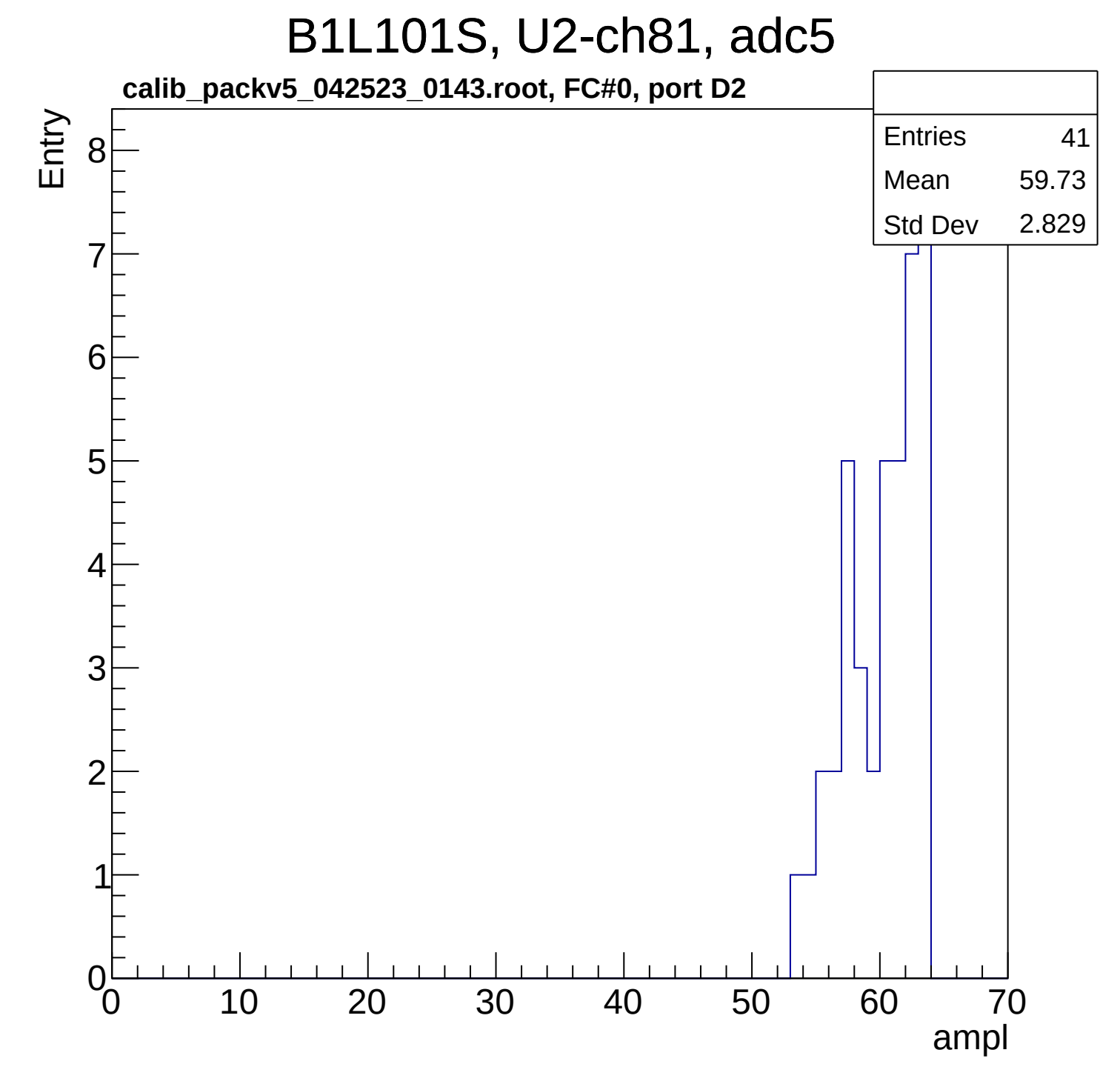

B1L101S, U2-ch81, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 81
Mean 30.36
Std Dev 3.766
Gaus mean : 30.7796
Gaus Width: 3.5454
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

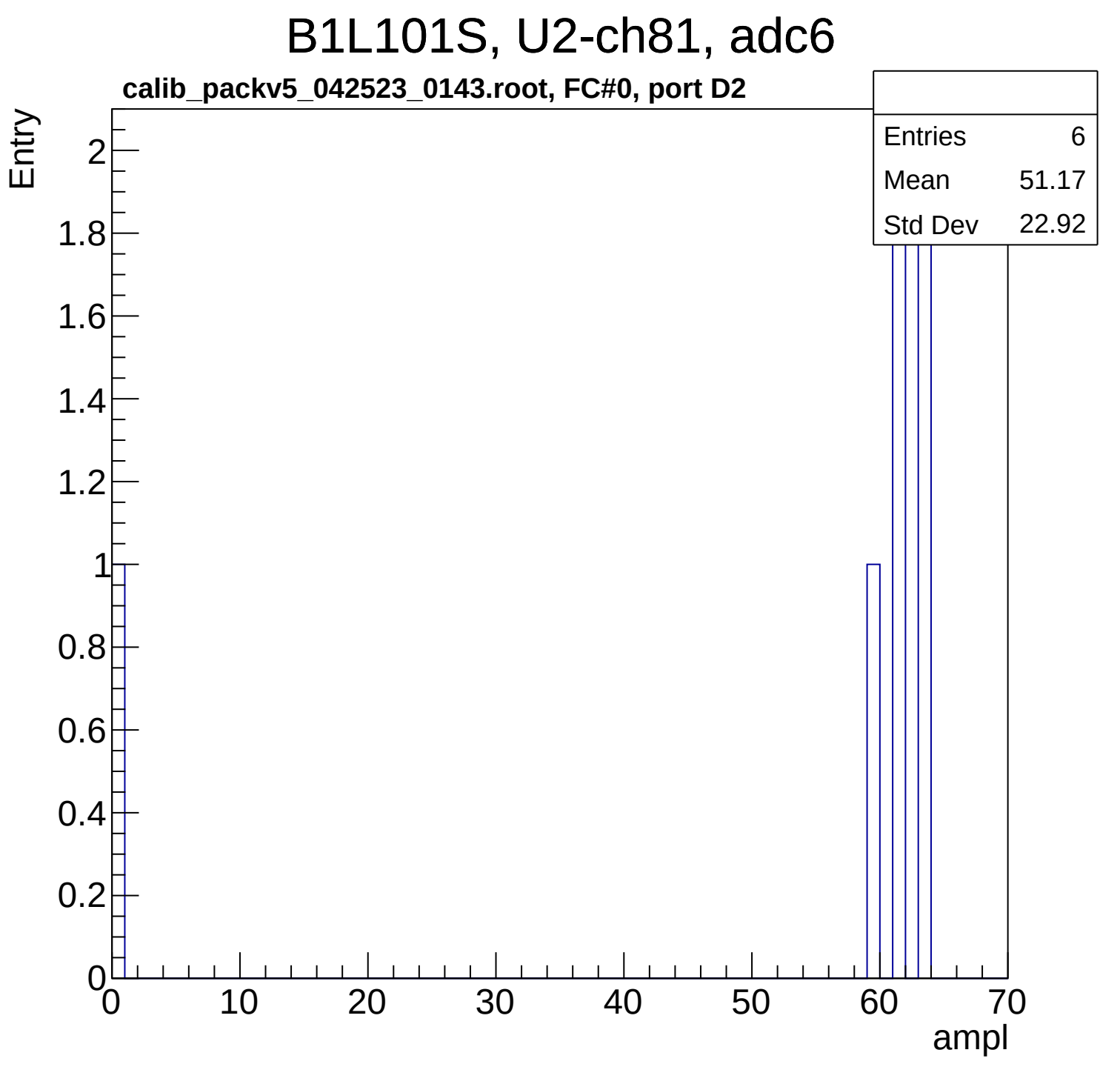

B1L101S, U2-ch81, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 36.84
Std Dev 3.967
Gaus mean : 37.7249
Gaus Width: 4.6681
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

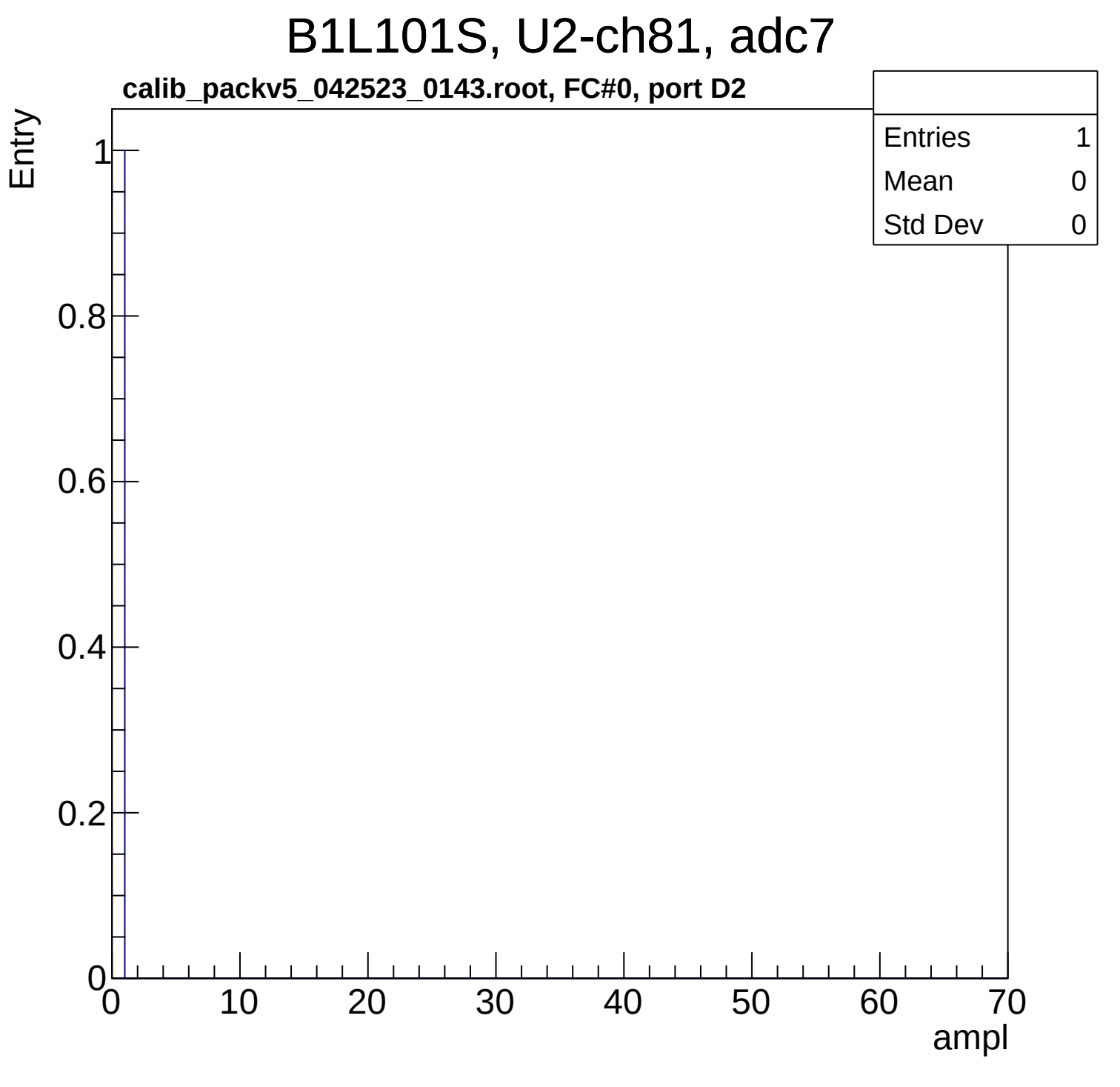

B1L101S, U2-ch81, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 41.96
Std Dev 3.934
Gaus mean : 43.0019
Gaus Width: 4.2811
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

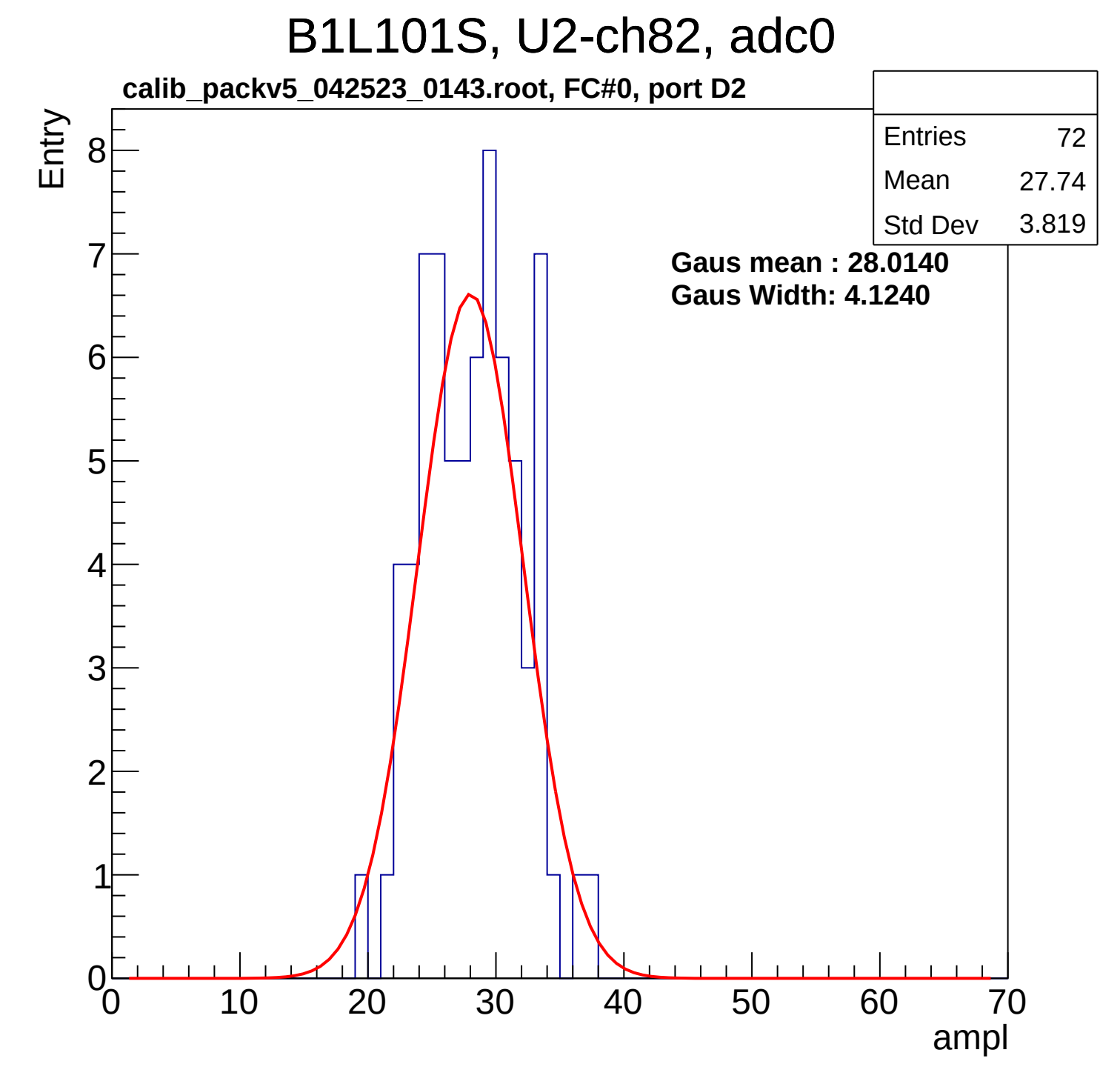

B1L101S, U2-ch81, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 49.46
Std Dev 3.444
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

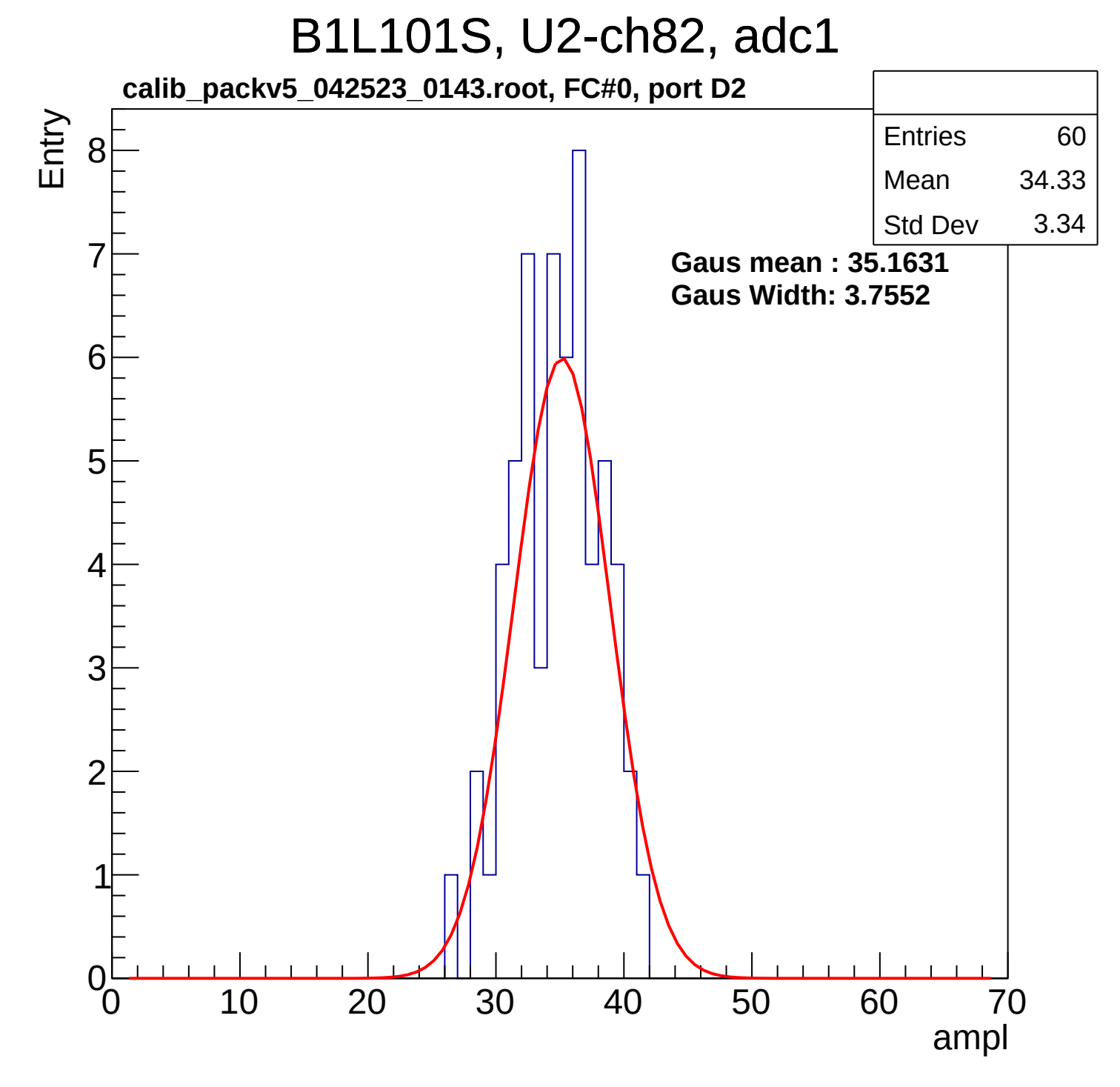

B1L101S, U2-ch81, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 56.15
Std Dev 3.52
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

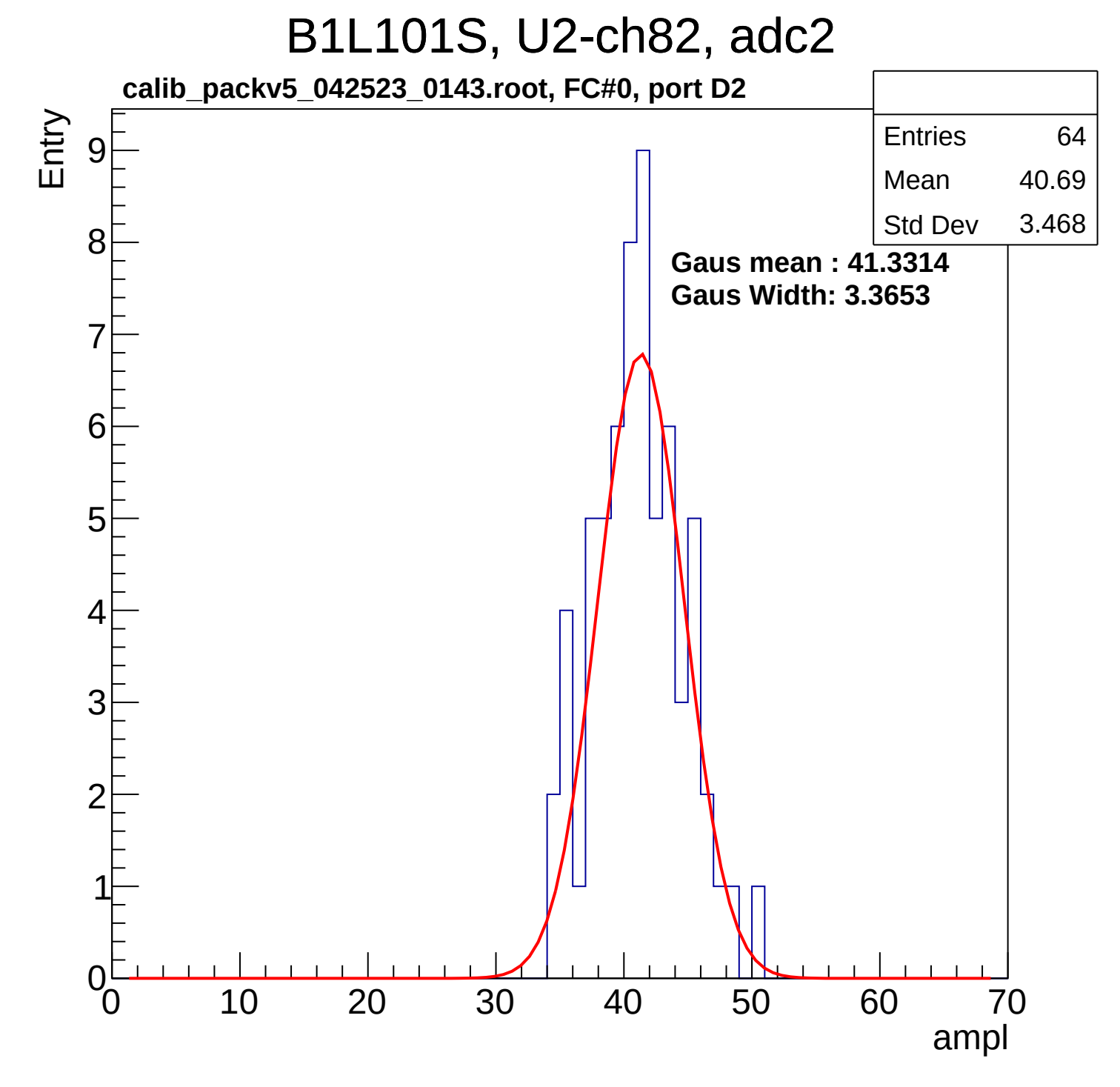

B1L101S, U2-ch81, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 41
Mean 59.73
Std Dev 2.829
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

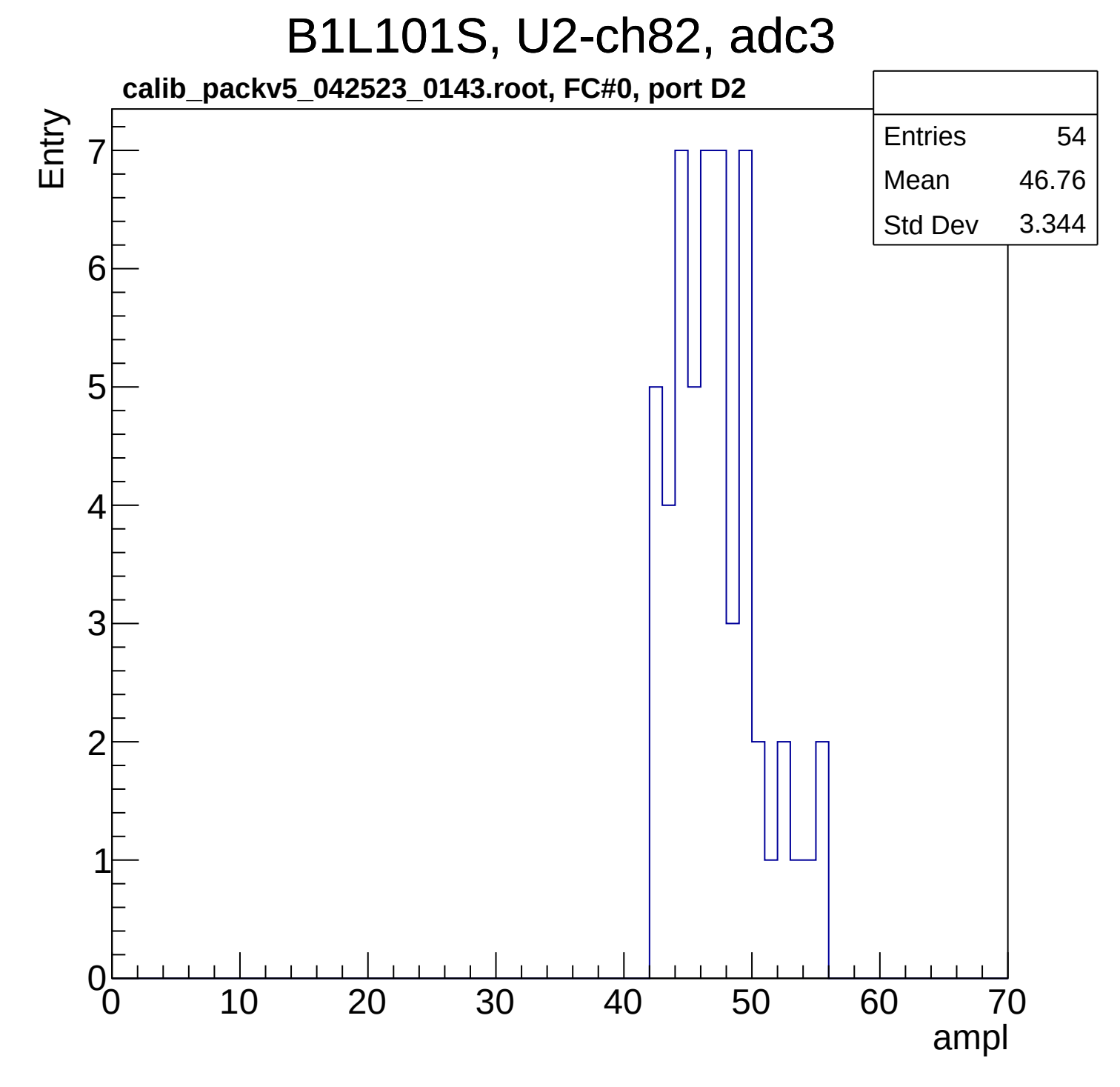

B1L101S, U2-ch81, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 51.17
Std Dev 22.92
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

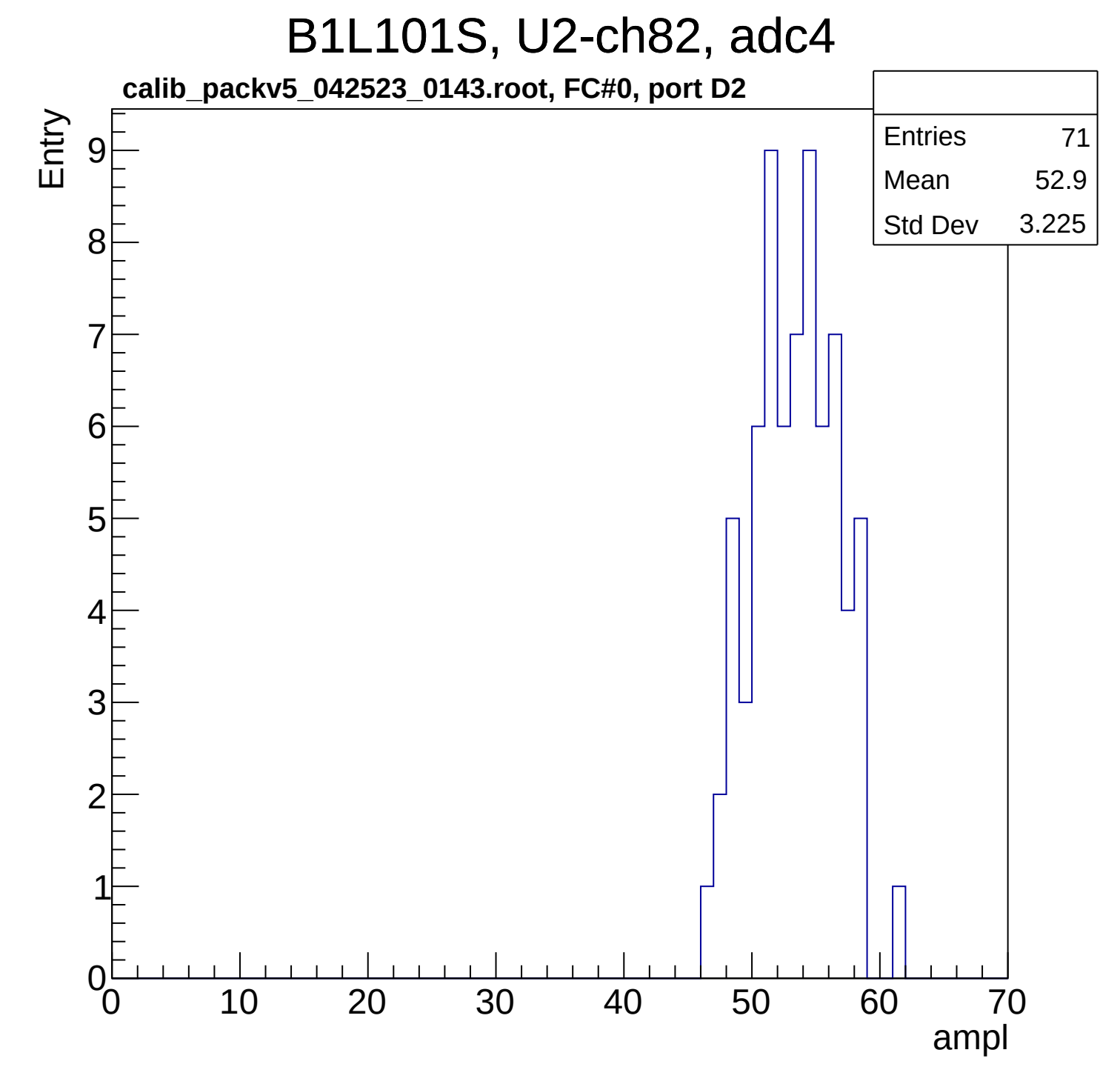

B1L101S, U2-ch81, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

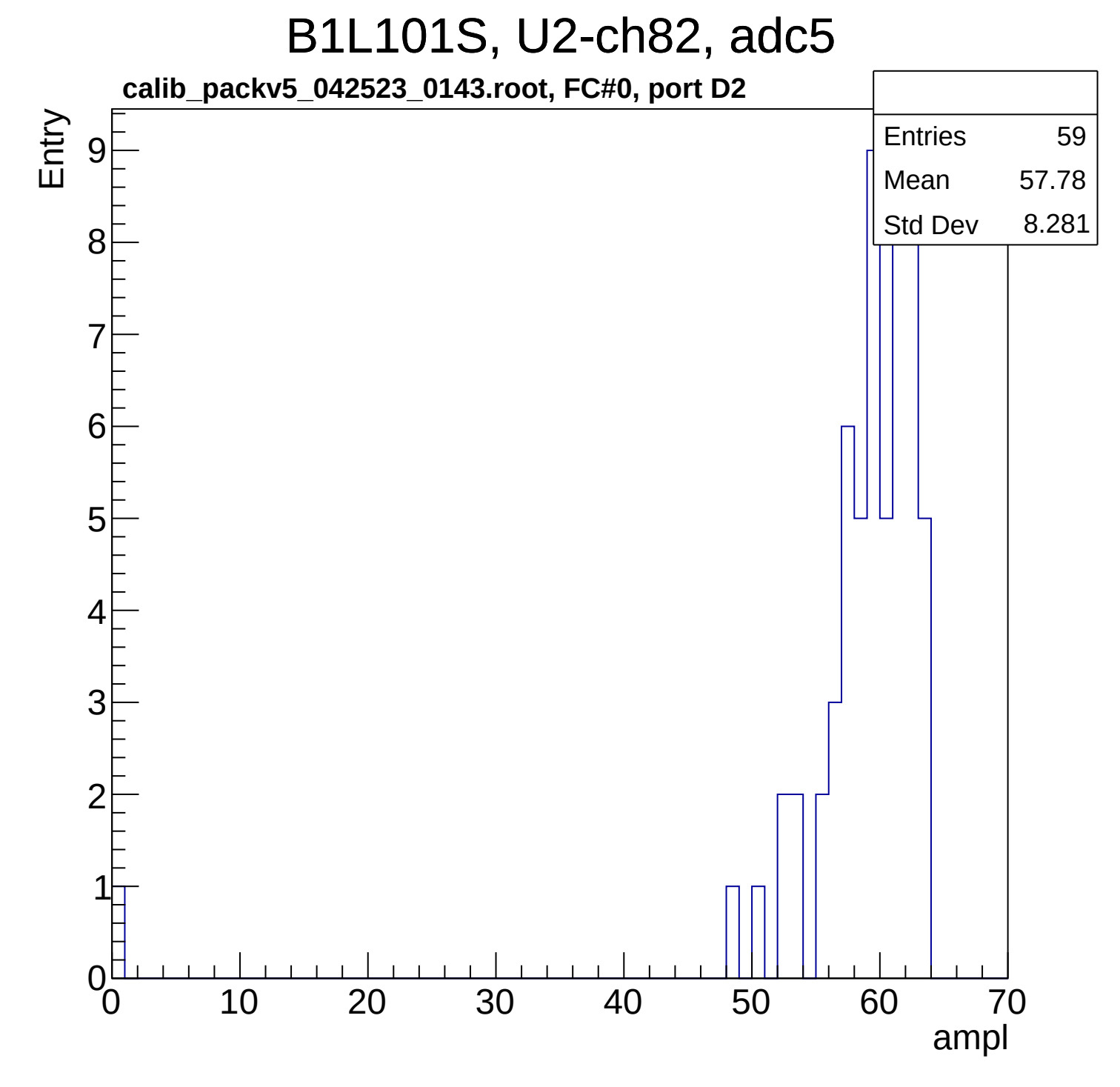

B1L101S, U2-ch82, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 27.74
Std Dev 3.819
Gaus mean : 28.0140
Gaus Width: 4.1240
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

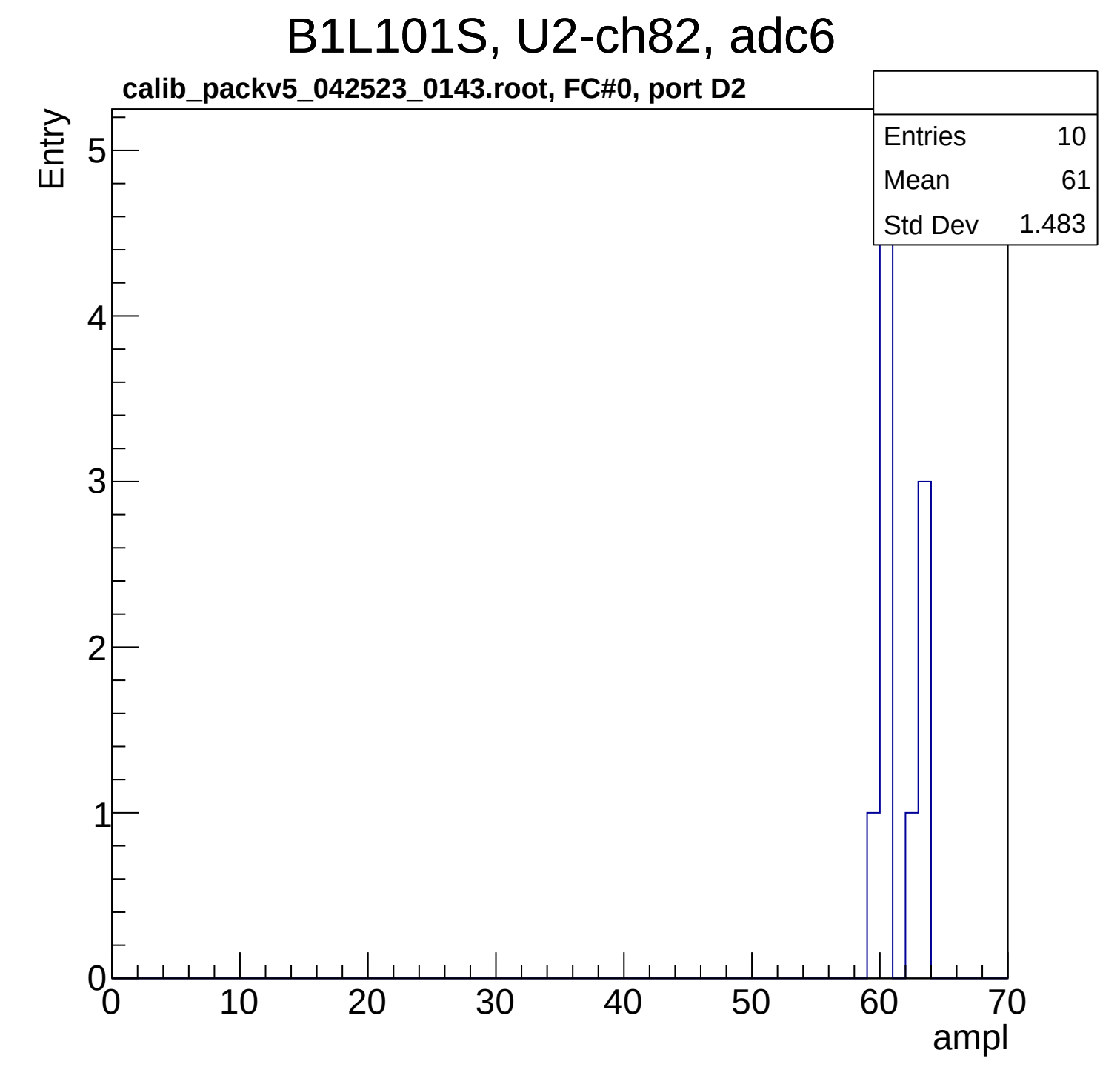

B1L101S, U2-ch82, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 34.33
Std Dev 3.34
Gaus mean : 35.1631
Gaus Width: 3.7552
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

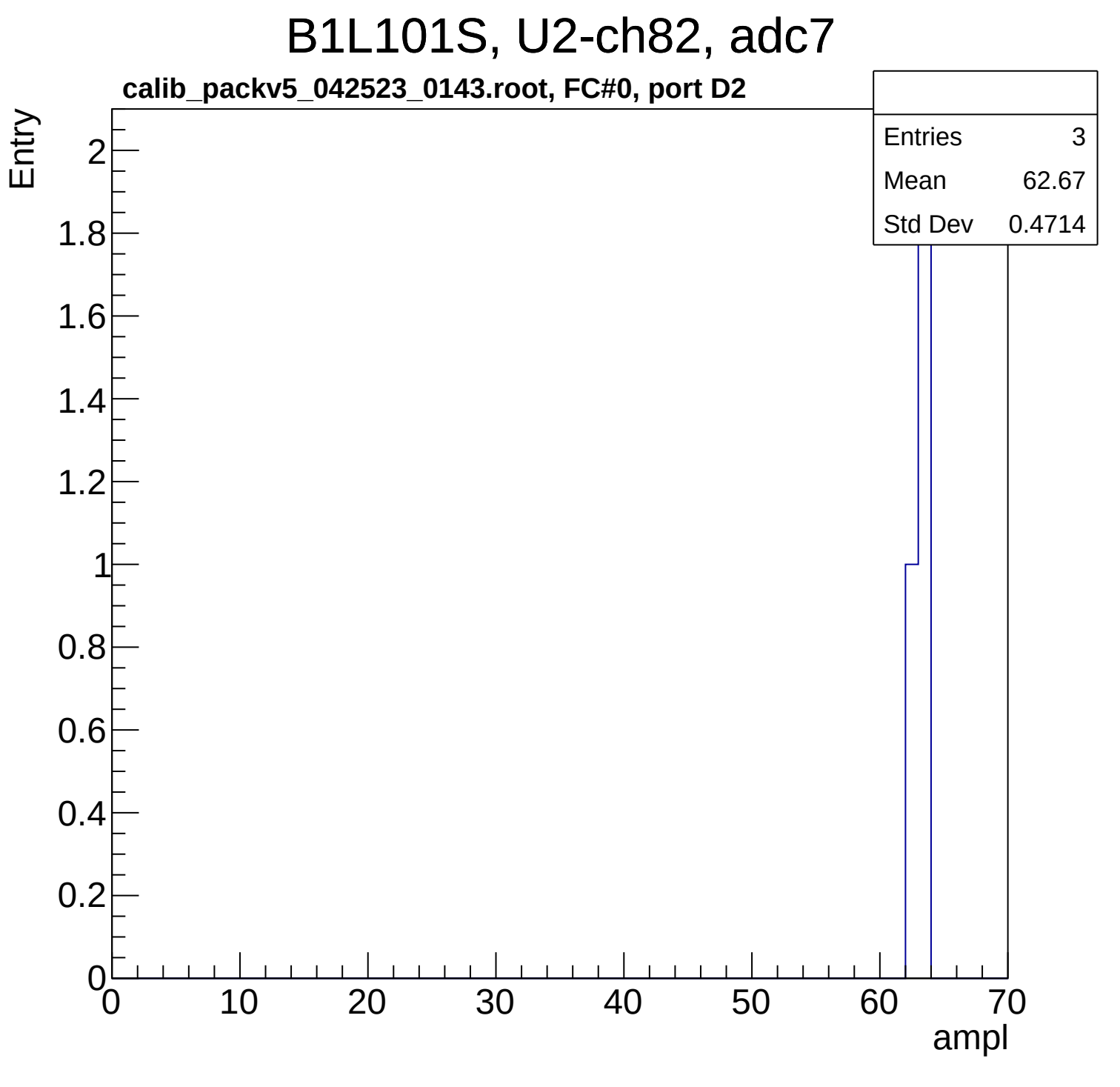

B1L101S, U2-ch82, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 40.69
Std Dev 3.468
Gaus mean : 41.3314
Gaus Width: 3.3653
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

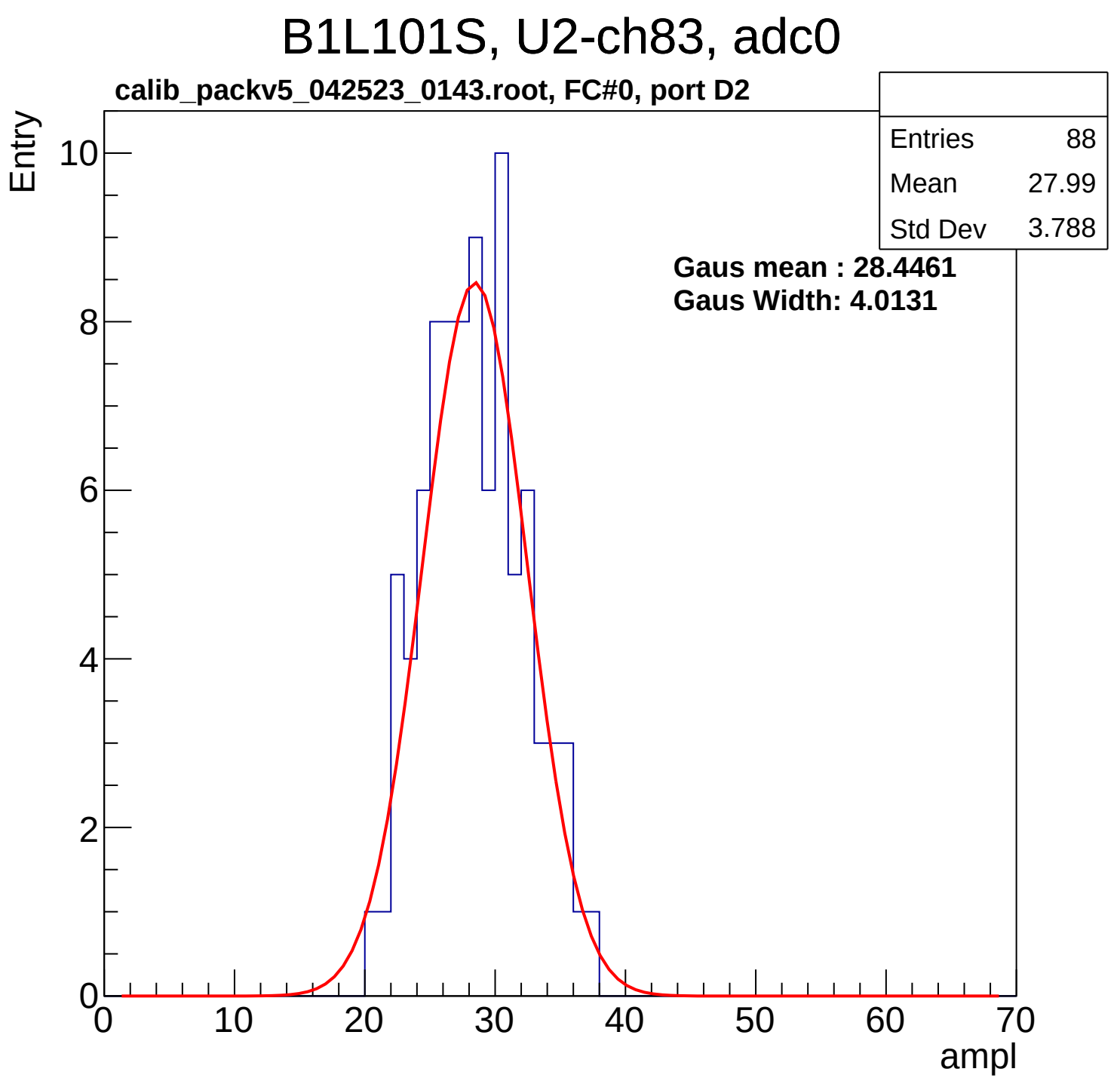

B1L101S, U2-ch82, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 46.76
Std Dev 3.344
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

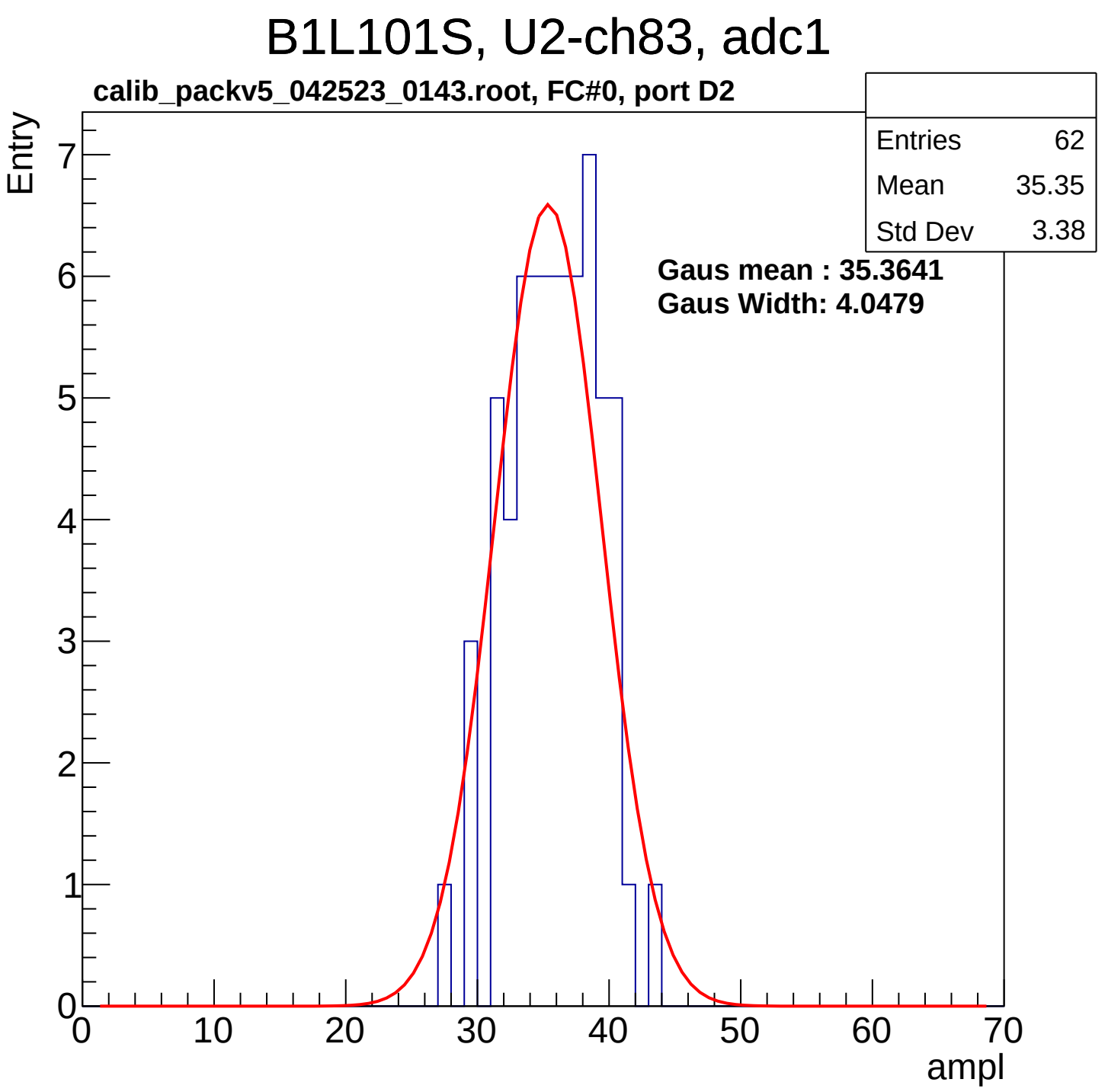

B1L101S, U2-ch82, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 52.9
Std Dev 3.225
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

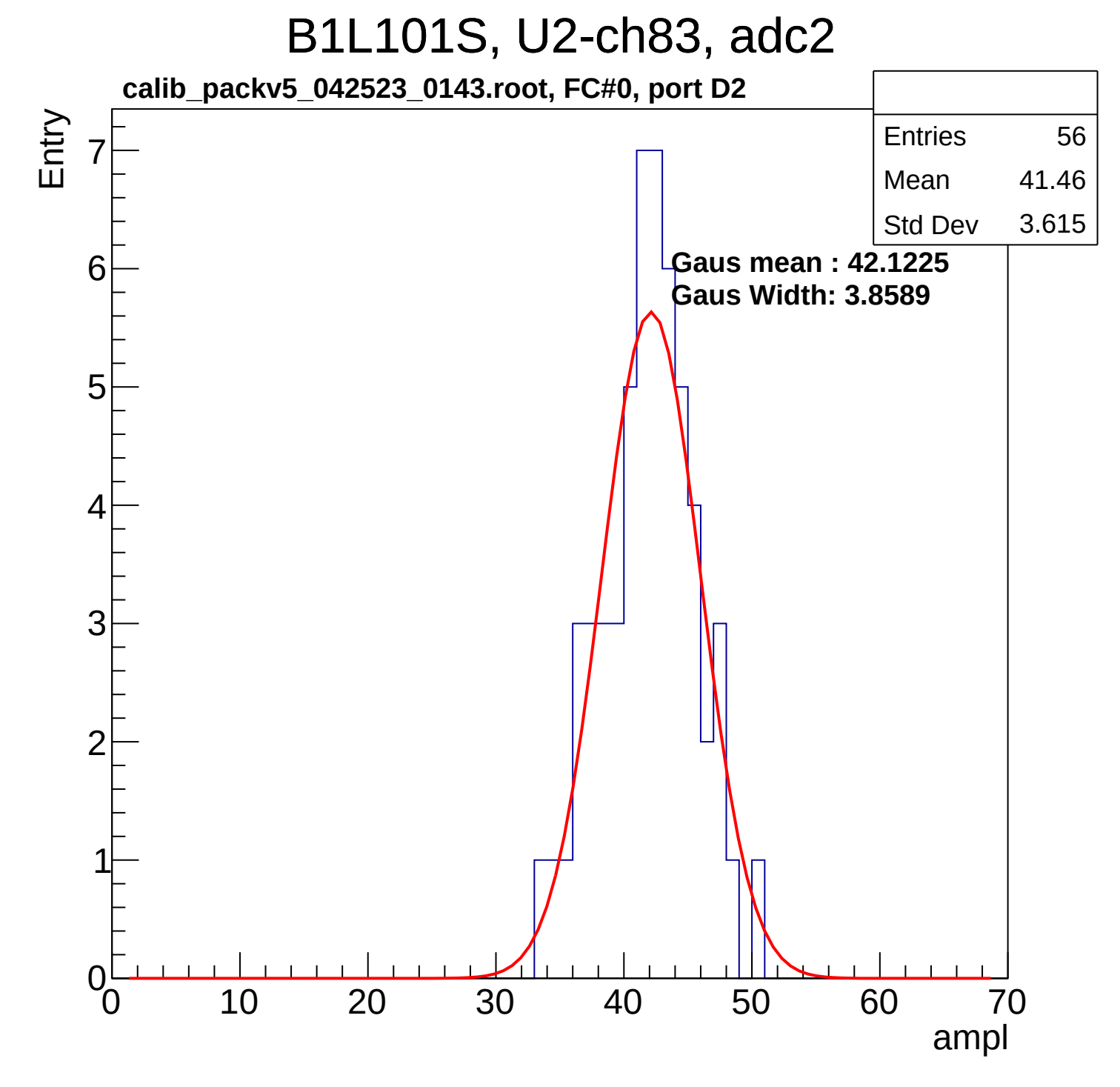

B1L101S, U2-ch82, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 57.78
Std Dev 8.281
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

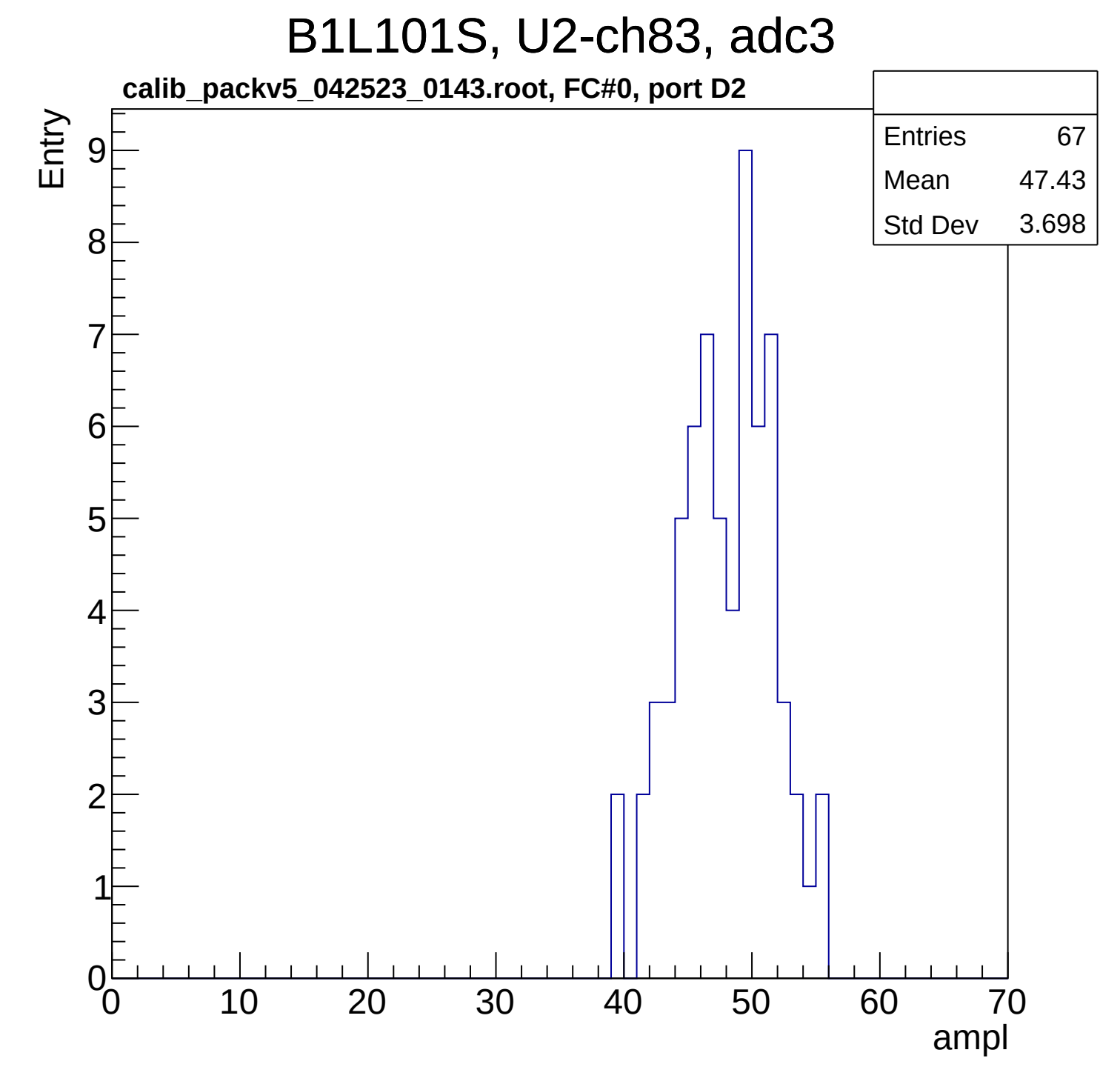

B1L101S, U2-ch82, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 61
Std Dev 1.483
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

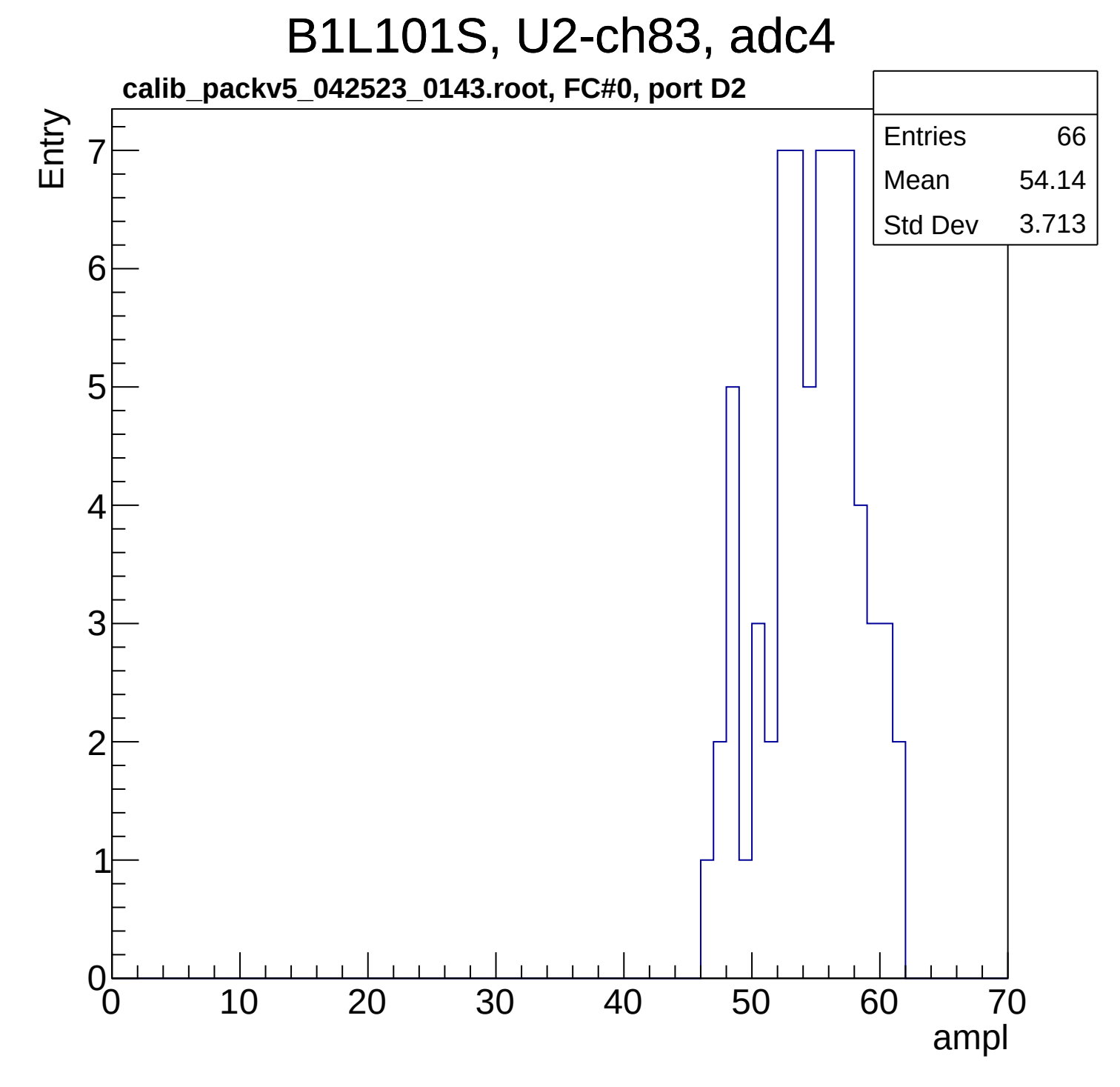

B1L101S, U2-ch82, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

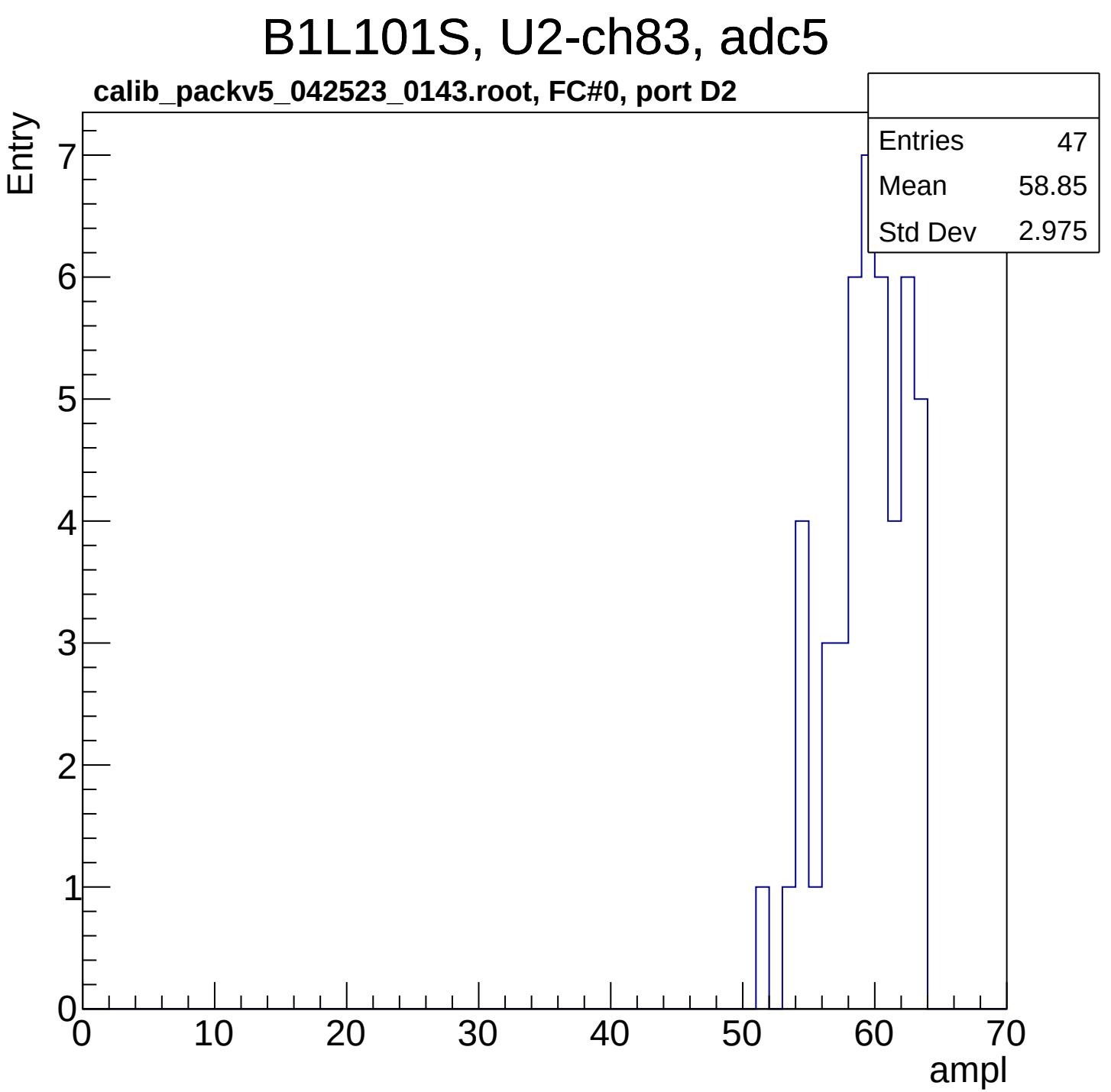

B1L101S, U2-ch83, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 88
Mean 27.99
Std Dev 3.788
Gaus mean : 28.4461
Gaus Width: 4.0131
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

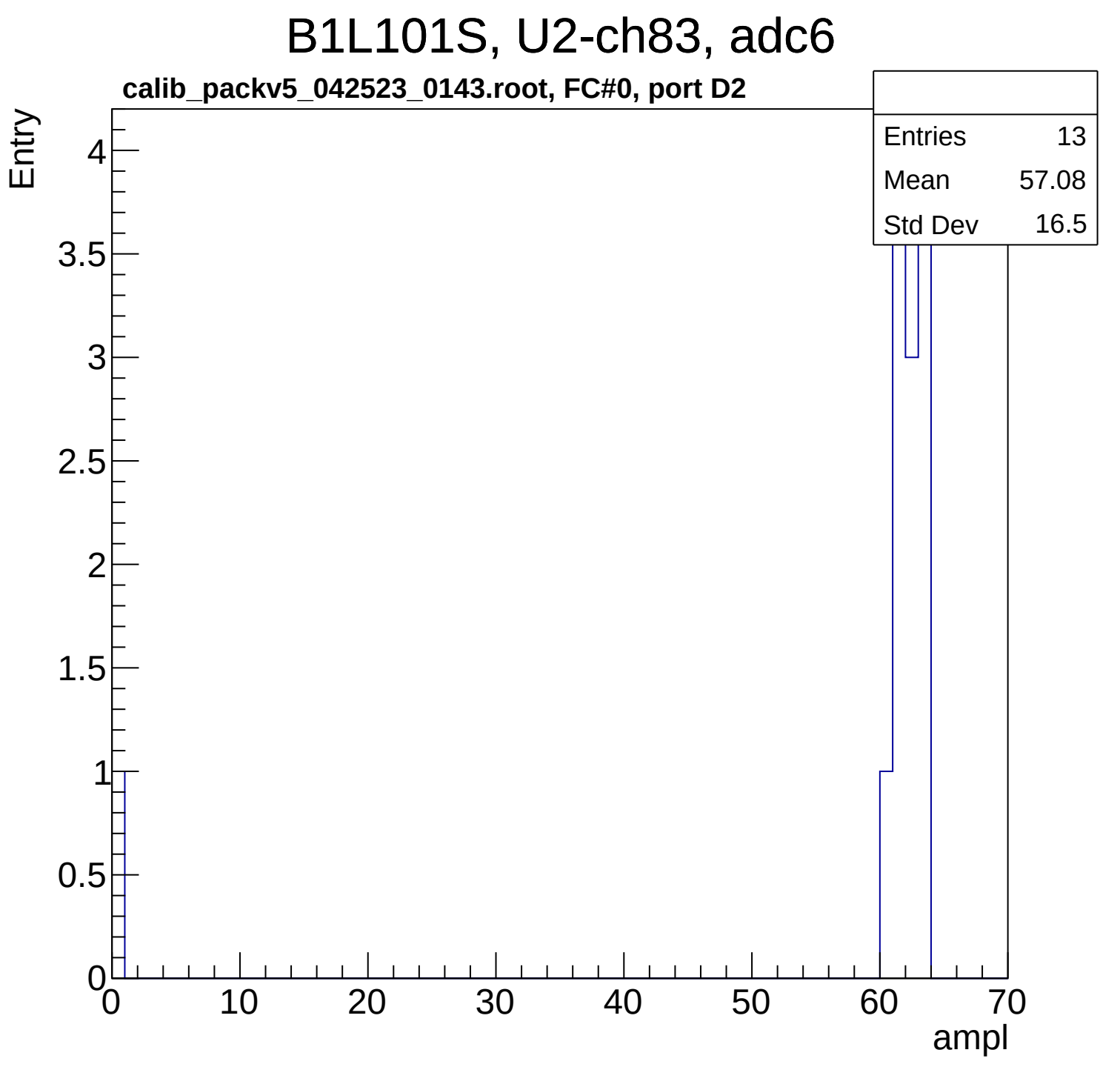

B1L101S, U2-ch83, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 35.35
Std Dev 3.38
Gaus mean : 35.3641
Gaus Width: 4.0479
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

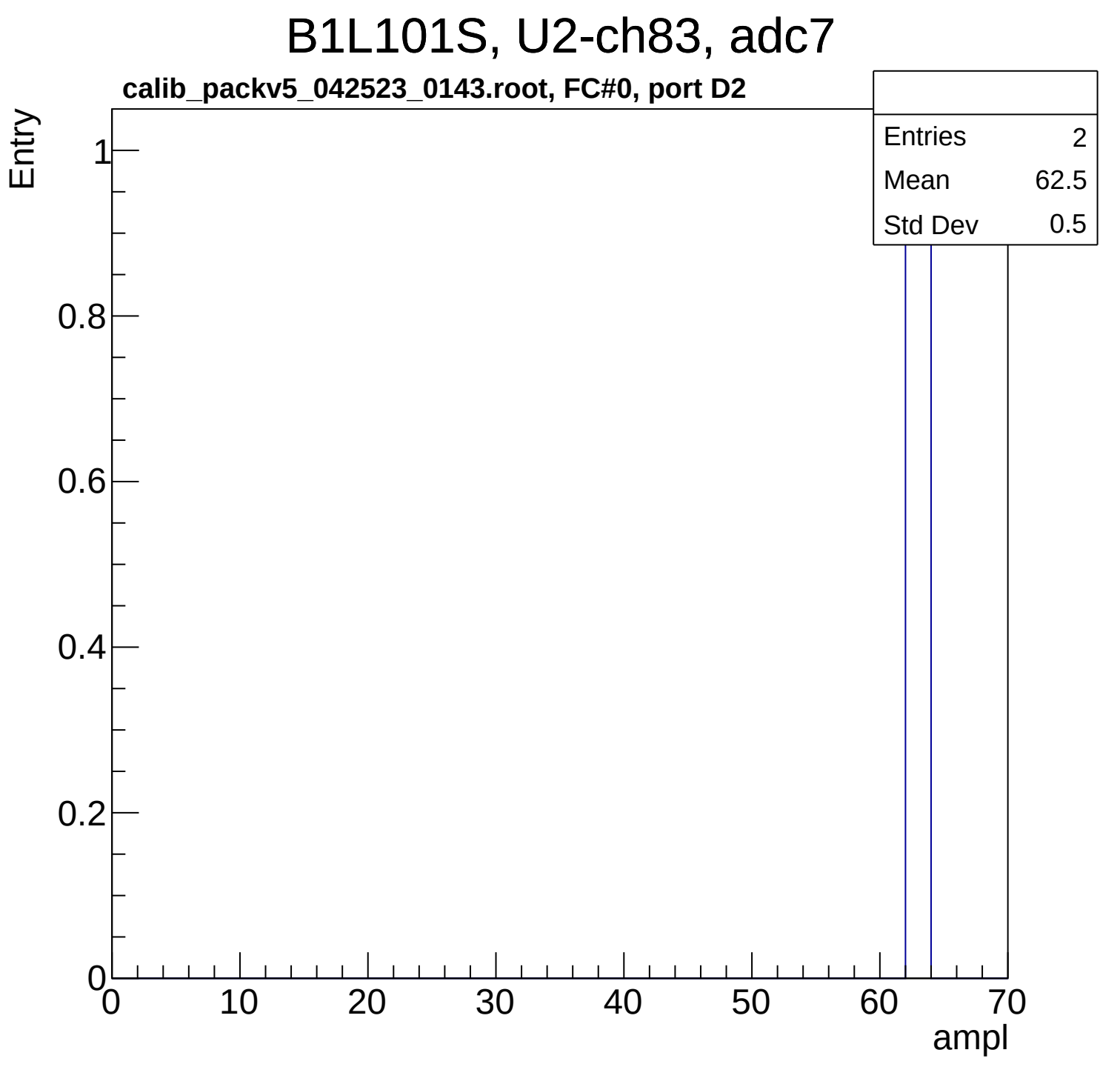

B1L101S, U2-ch83, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 41.46
Std Dev 3.615
Gaus mean : 42.1225
Gaus Width: 3.8589
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

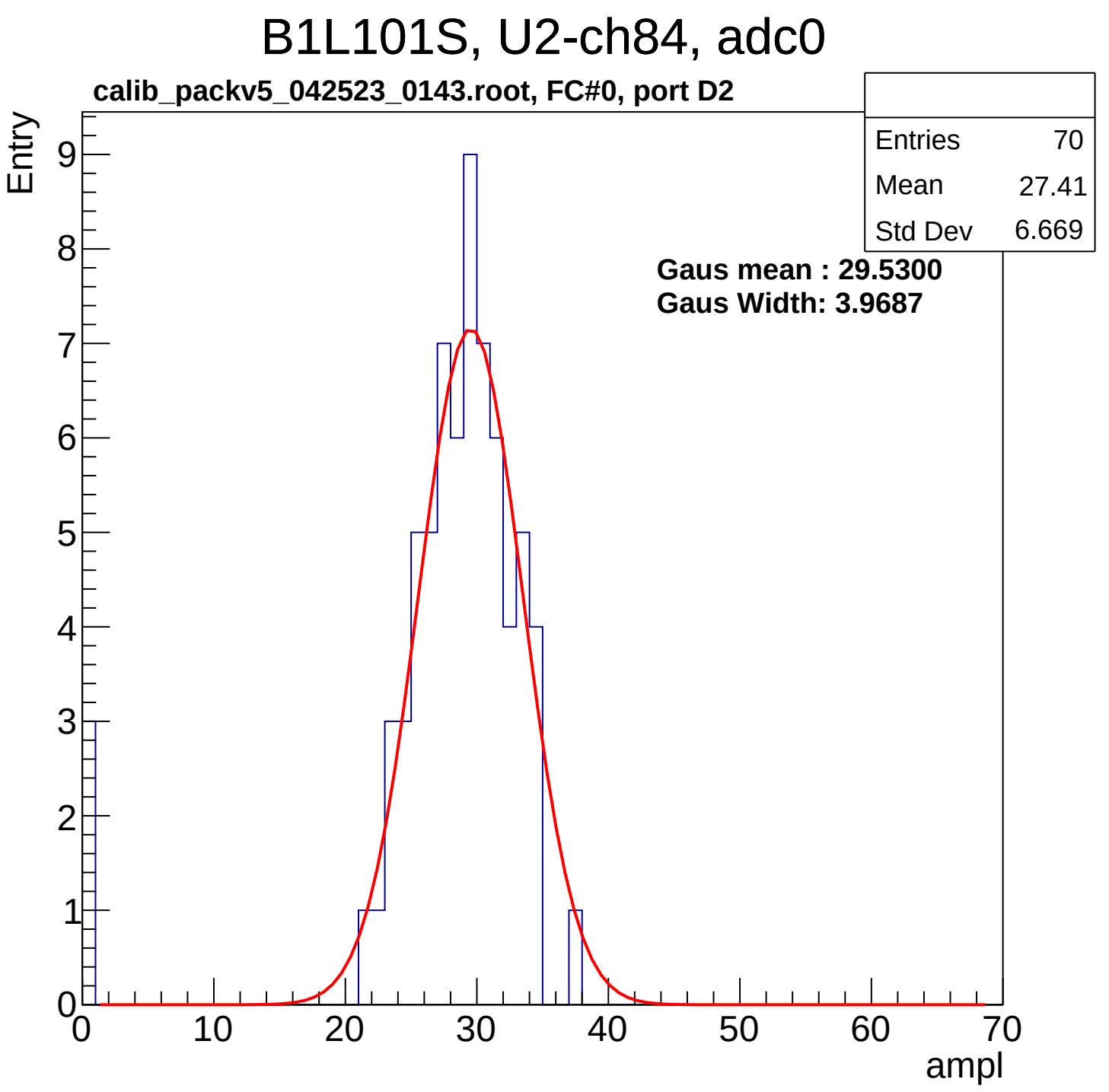

B1L101S, U2-ch83, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 47.43
Std Dev 3.698
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

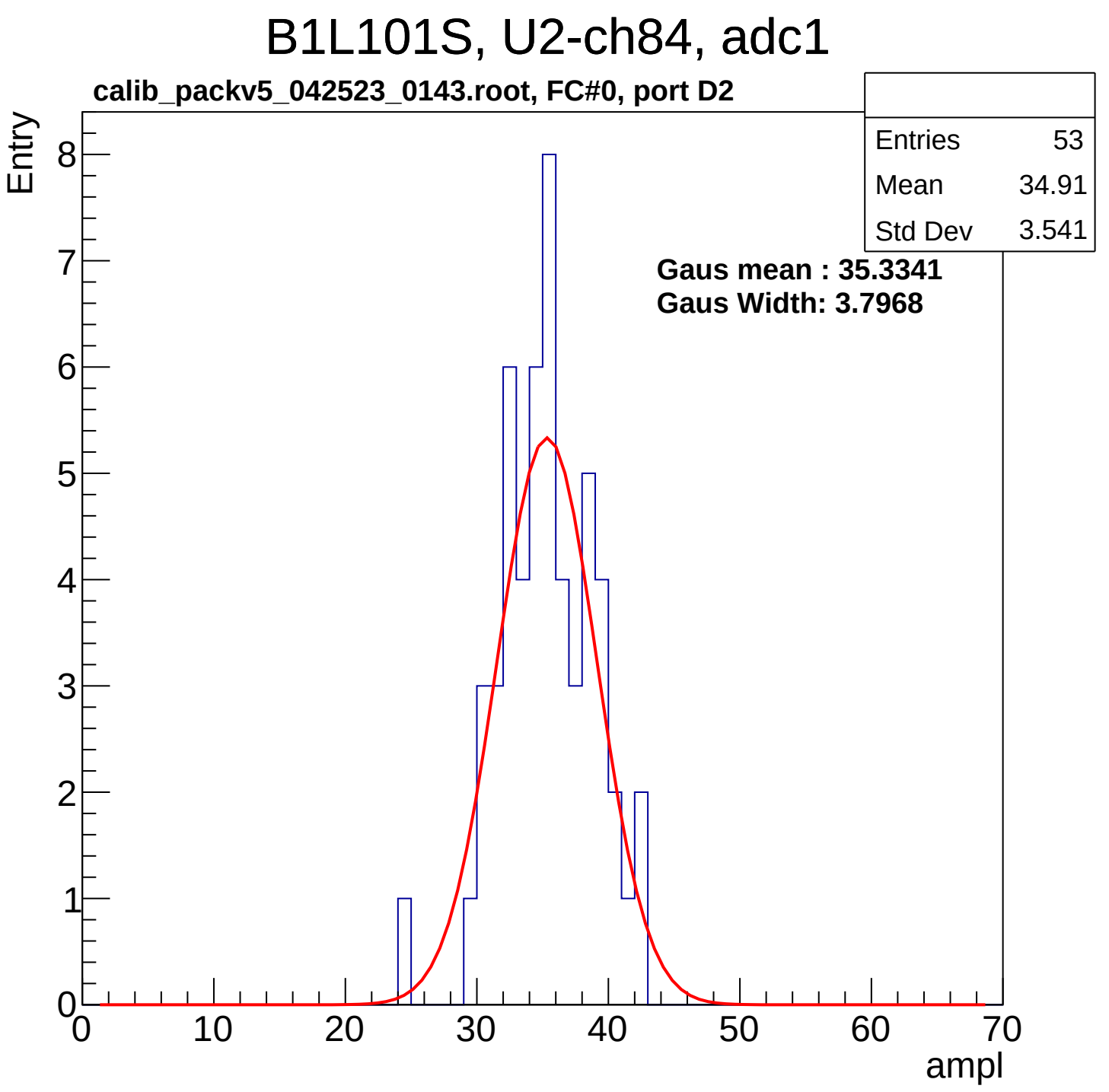

B1L101S, U2-ch83, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 54.14
Std Dev 3.713
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

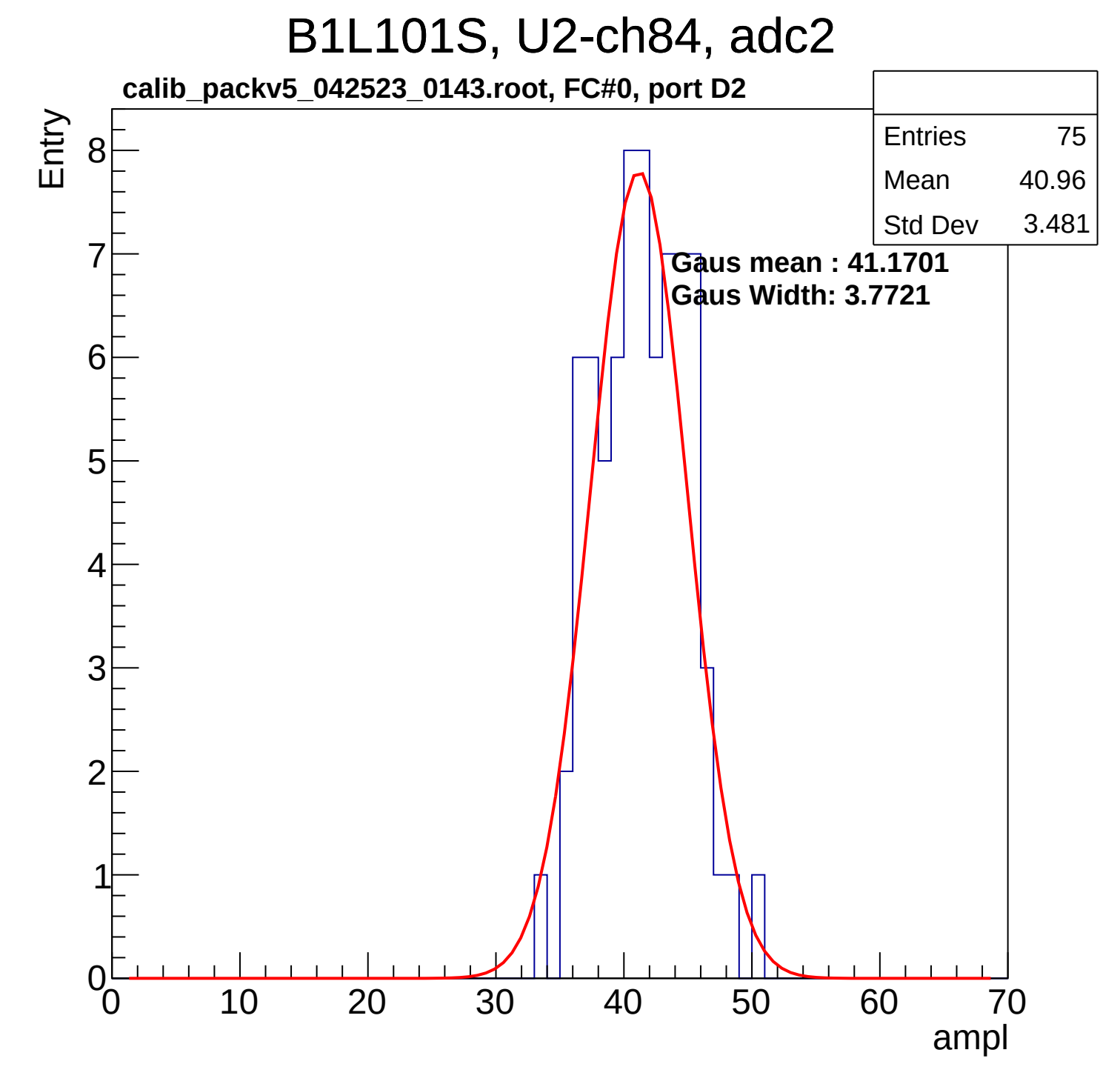

B1L101S, U2-ch83, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 58.85
Std Dev 2.975
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

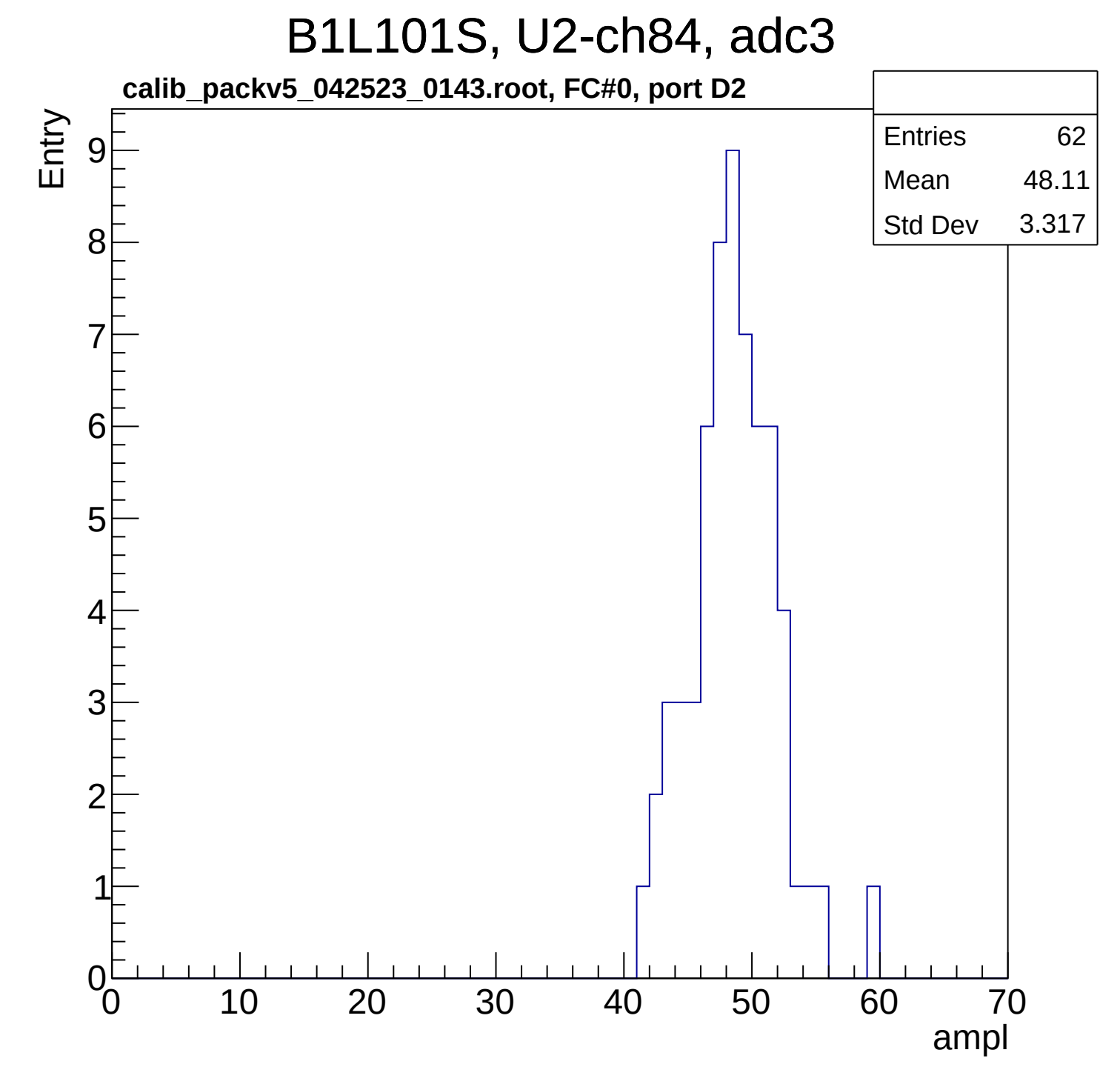

B1L101S, U2-ch83, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 13
Mean 57.08
Std Dev 16.5
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

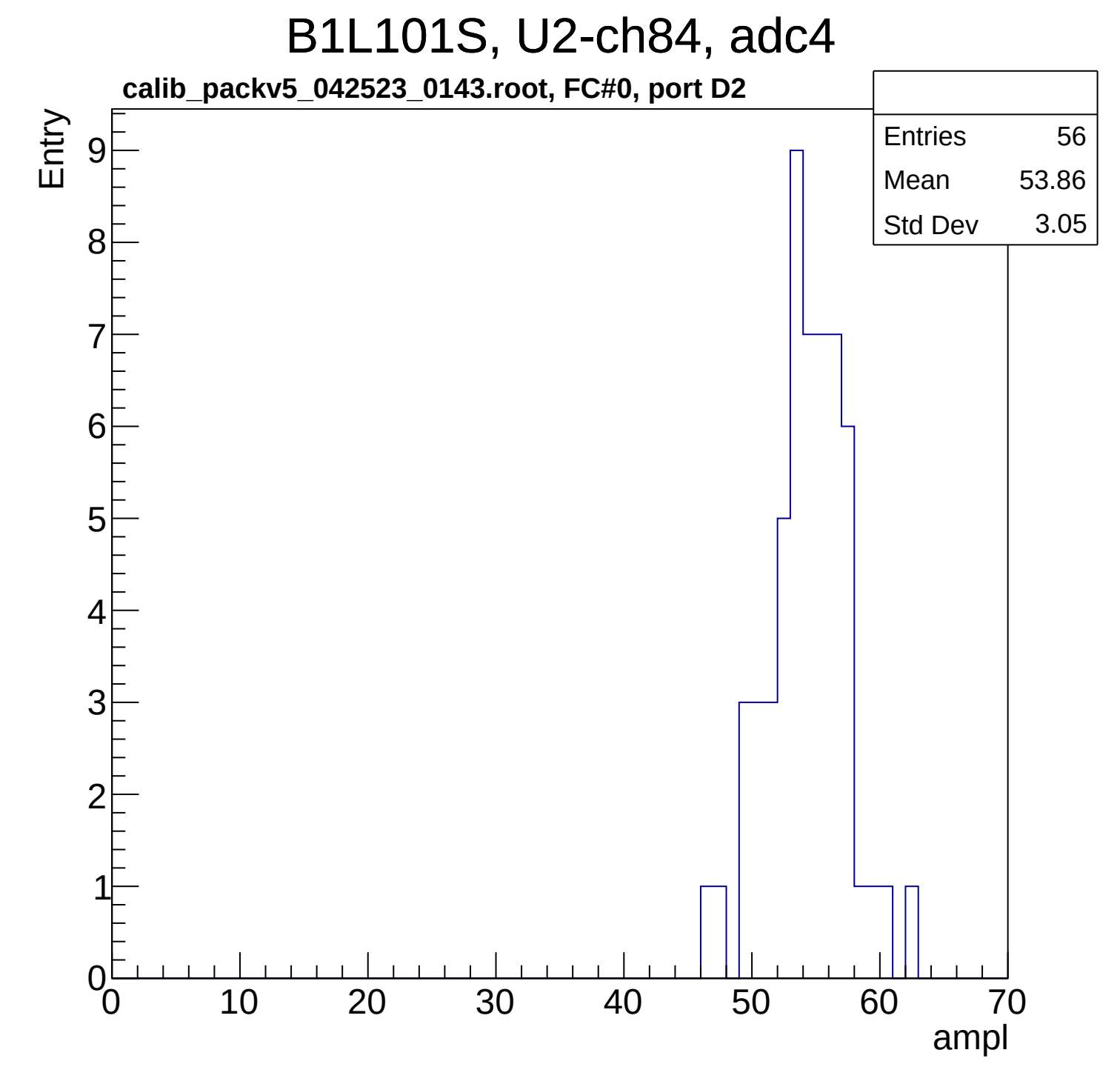

B1L101S, U2-ch83, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

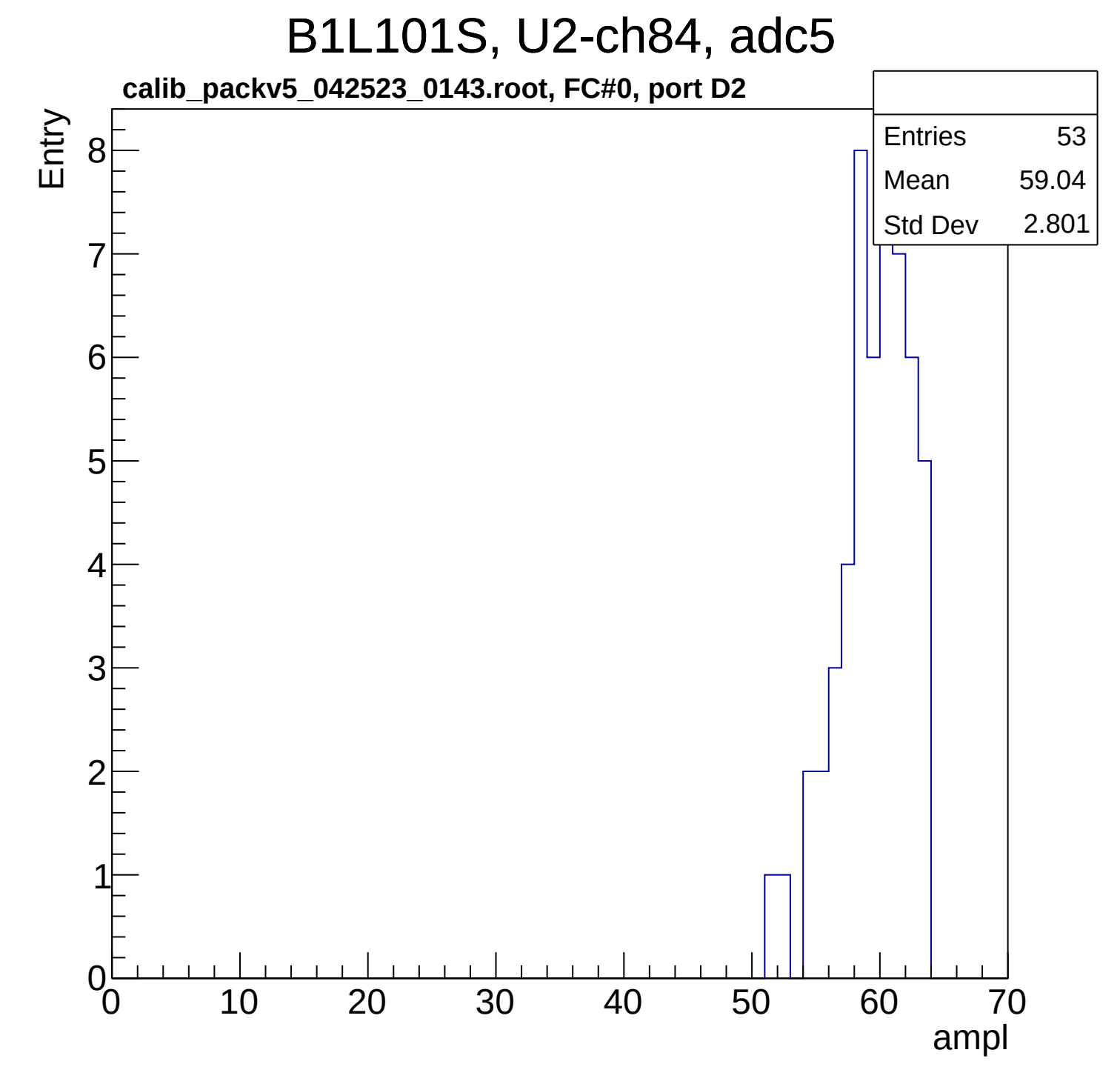

B1L101S, U2-ch84, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 27.41
Std Dev 6.669
Gaus mean : 29.5300
Gaus Width: 3.9687
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

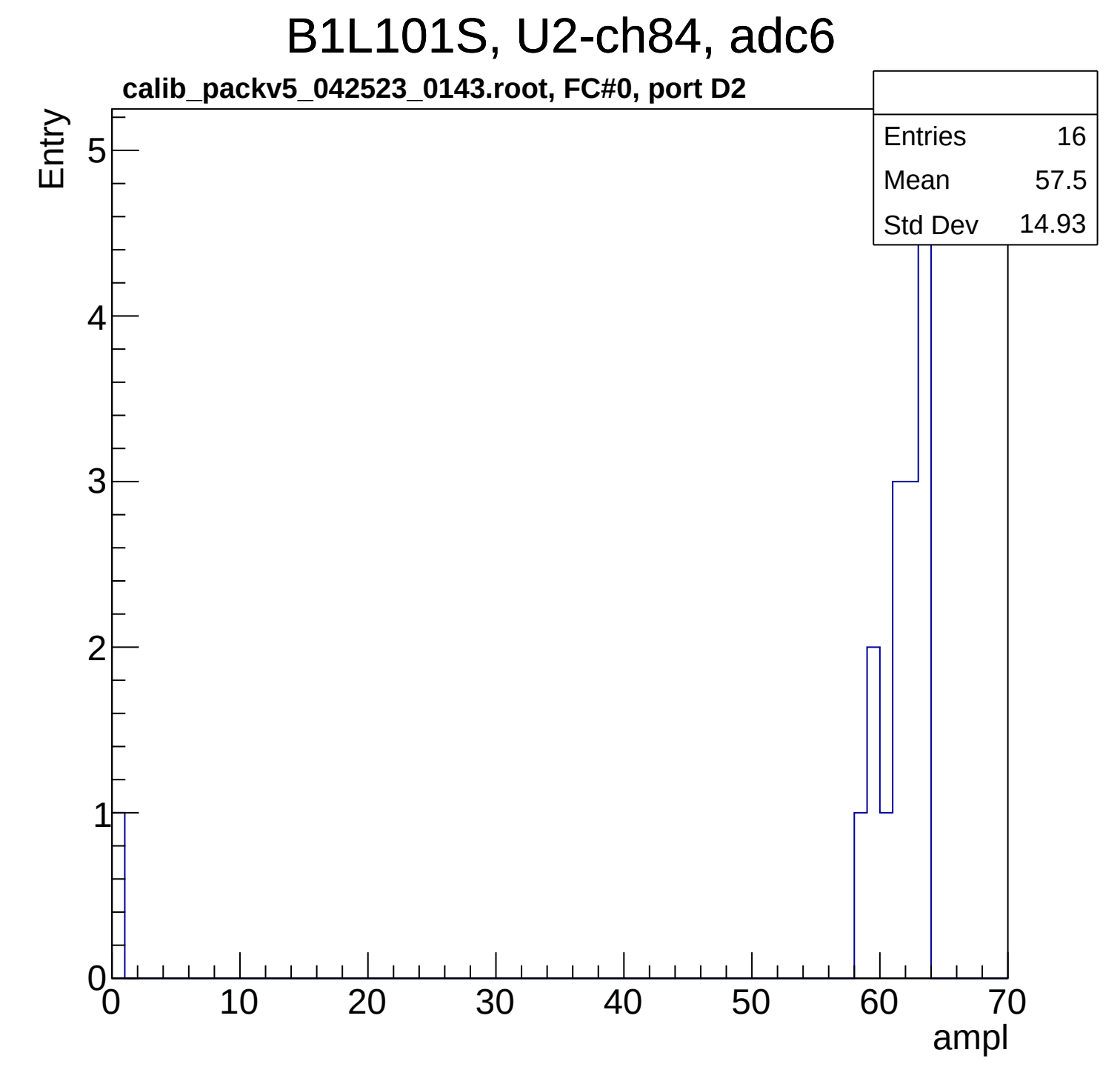

B1L101S, U2-ch84, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 34.91
Std Dev 3.541
Gaus mean : 35.3341
Gaus Width: 3.7968
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

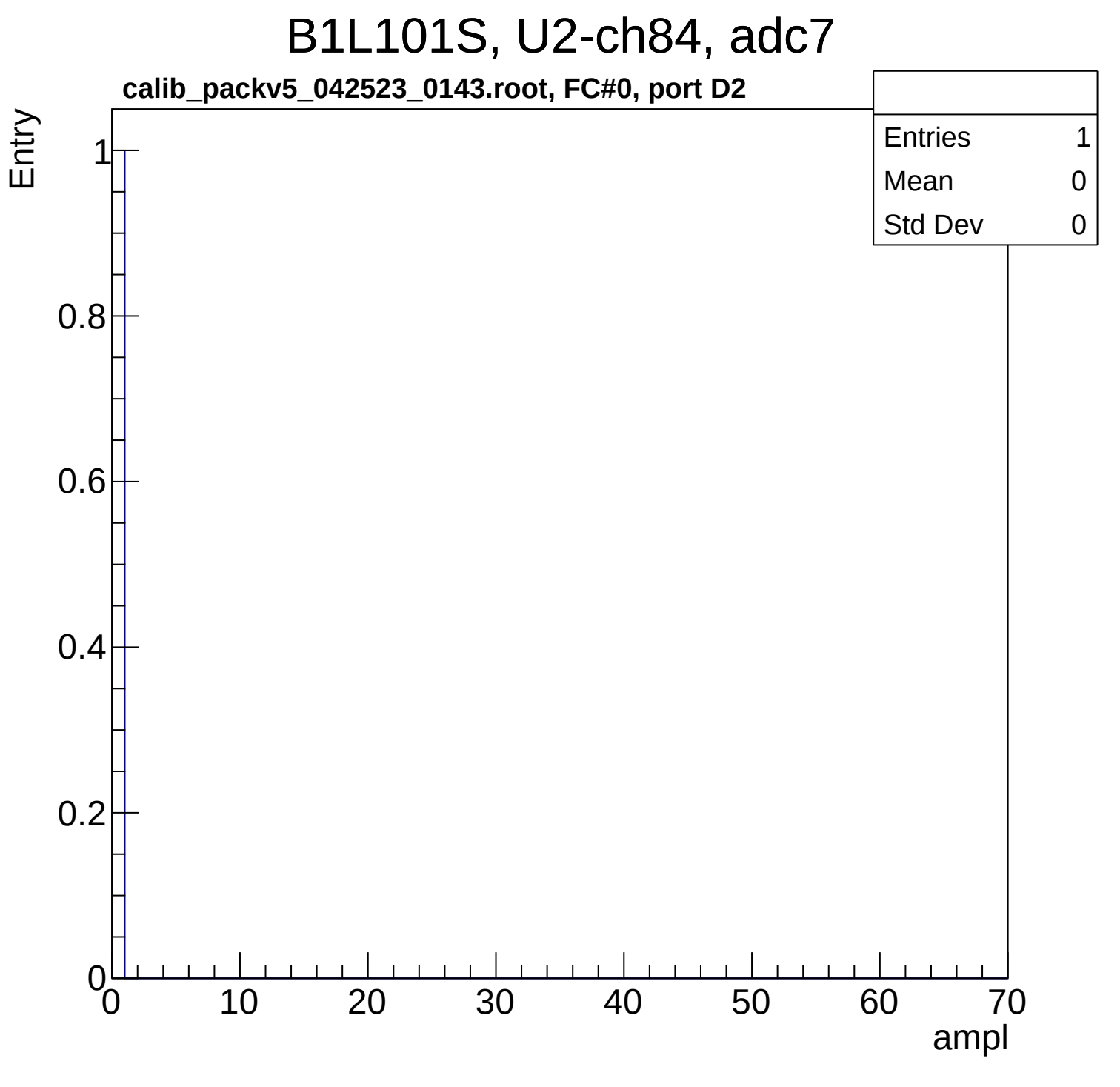

B1L101S, U2-ch84, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 40.96
Std Dev 3.481
Gaus mean : 41.1701
Gaus Width: 3.7721
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

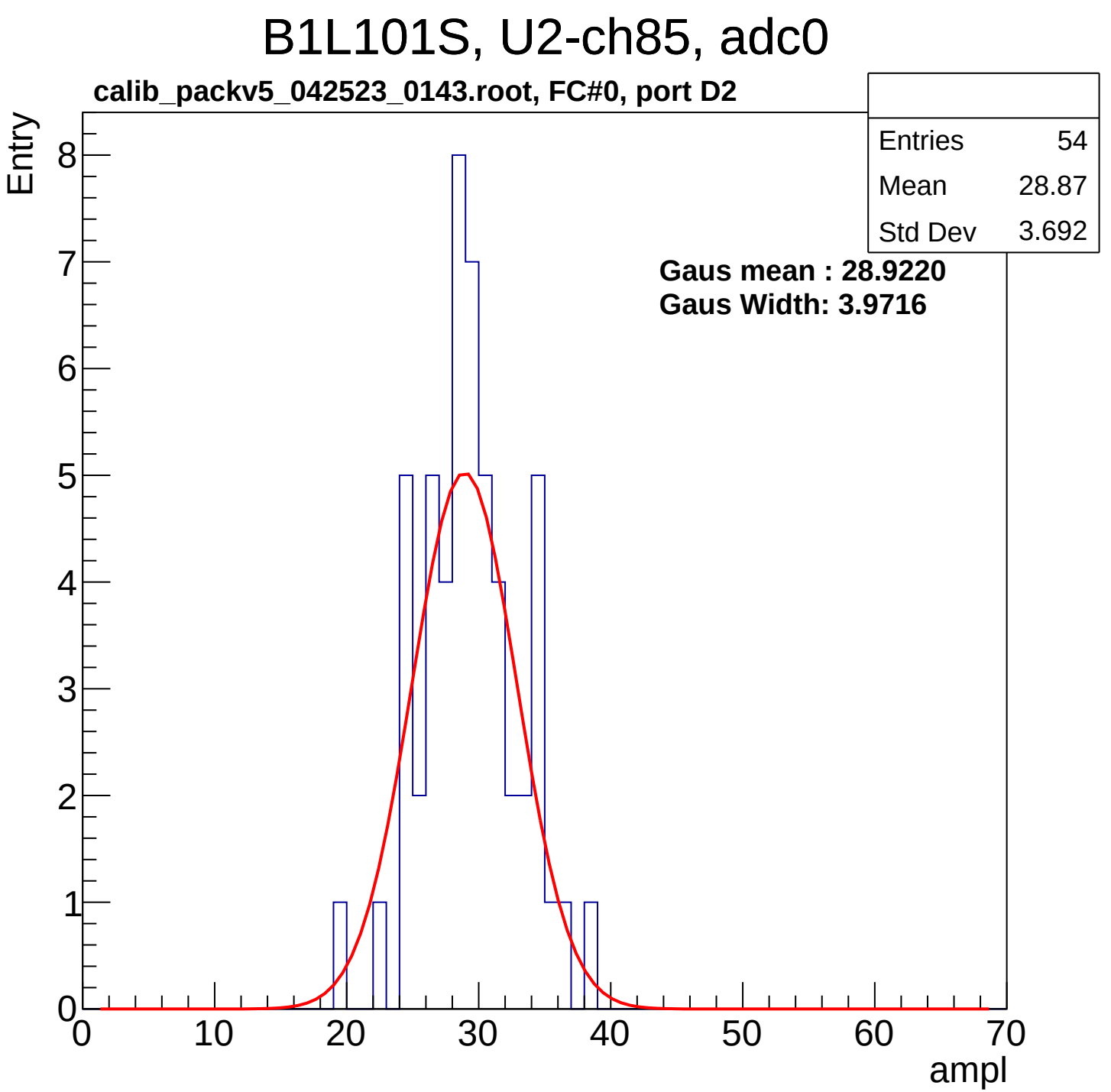

B1L101S, U2-ch84, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 48.11
Std Dev 3.317
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

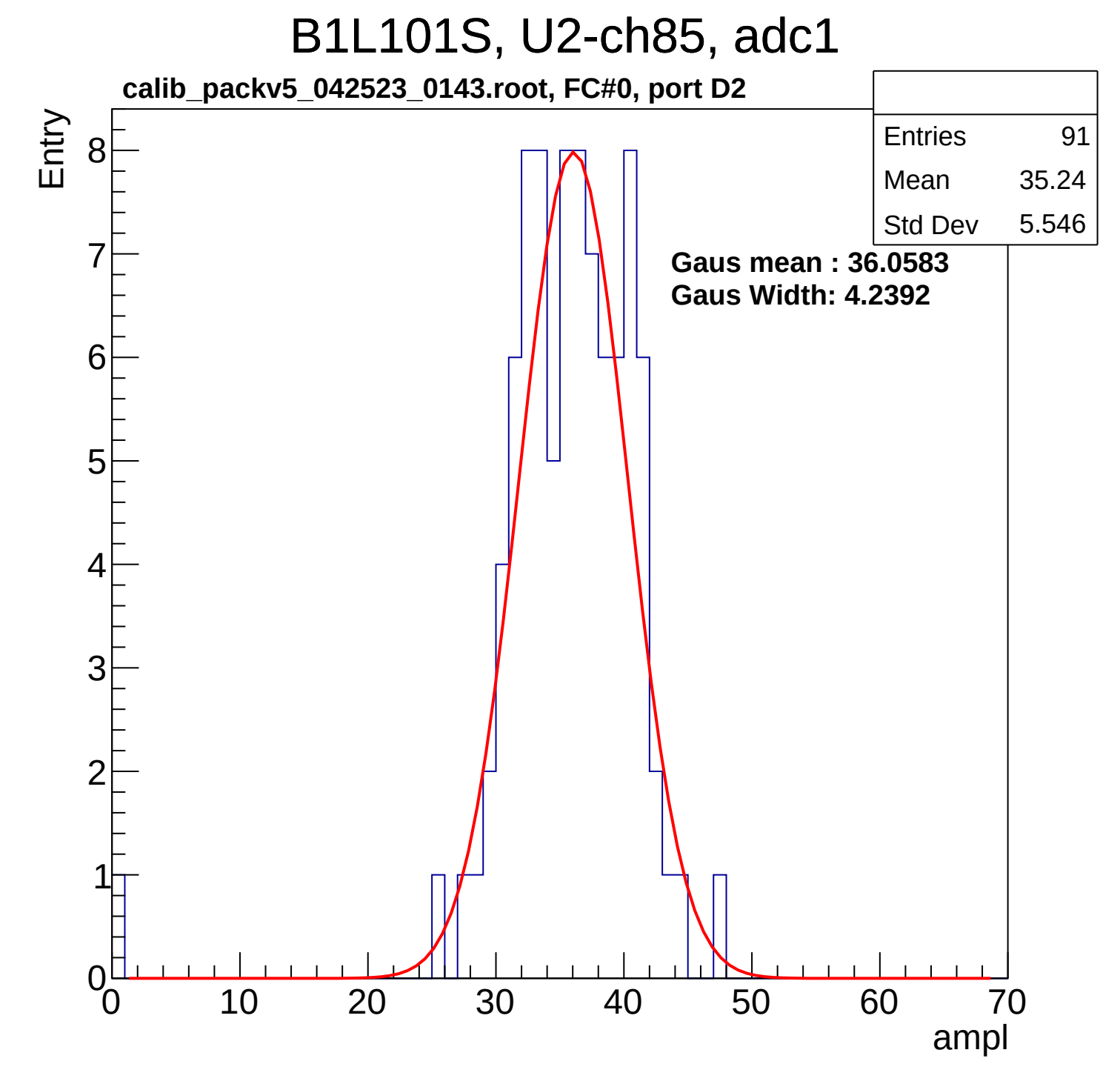

B1L101S, U2-ch84, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 53.86
Std Dev 3.05
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

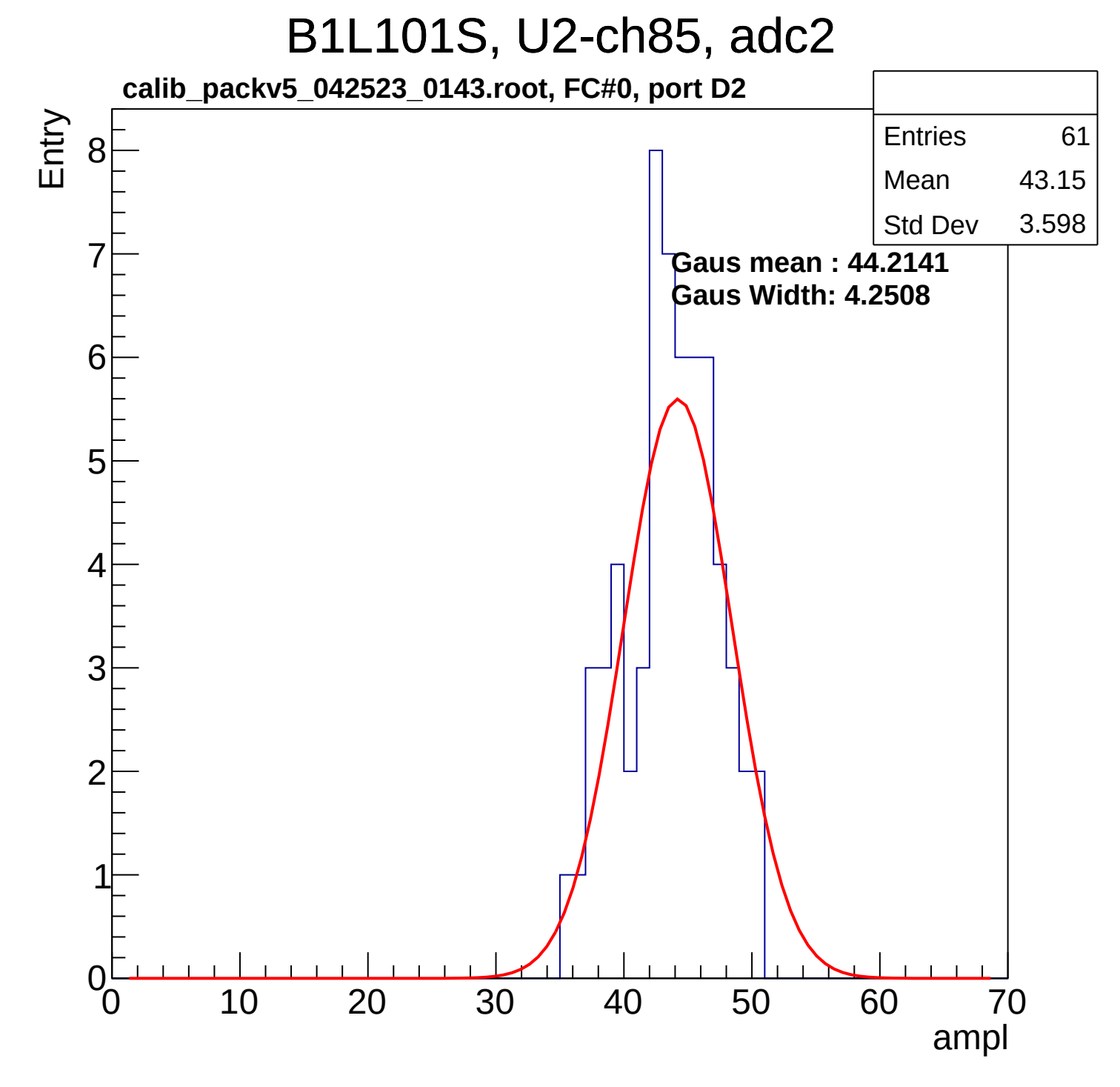

B1L101S, U2-ch84, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 59.04
Std Dev 2.801
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

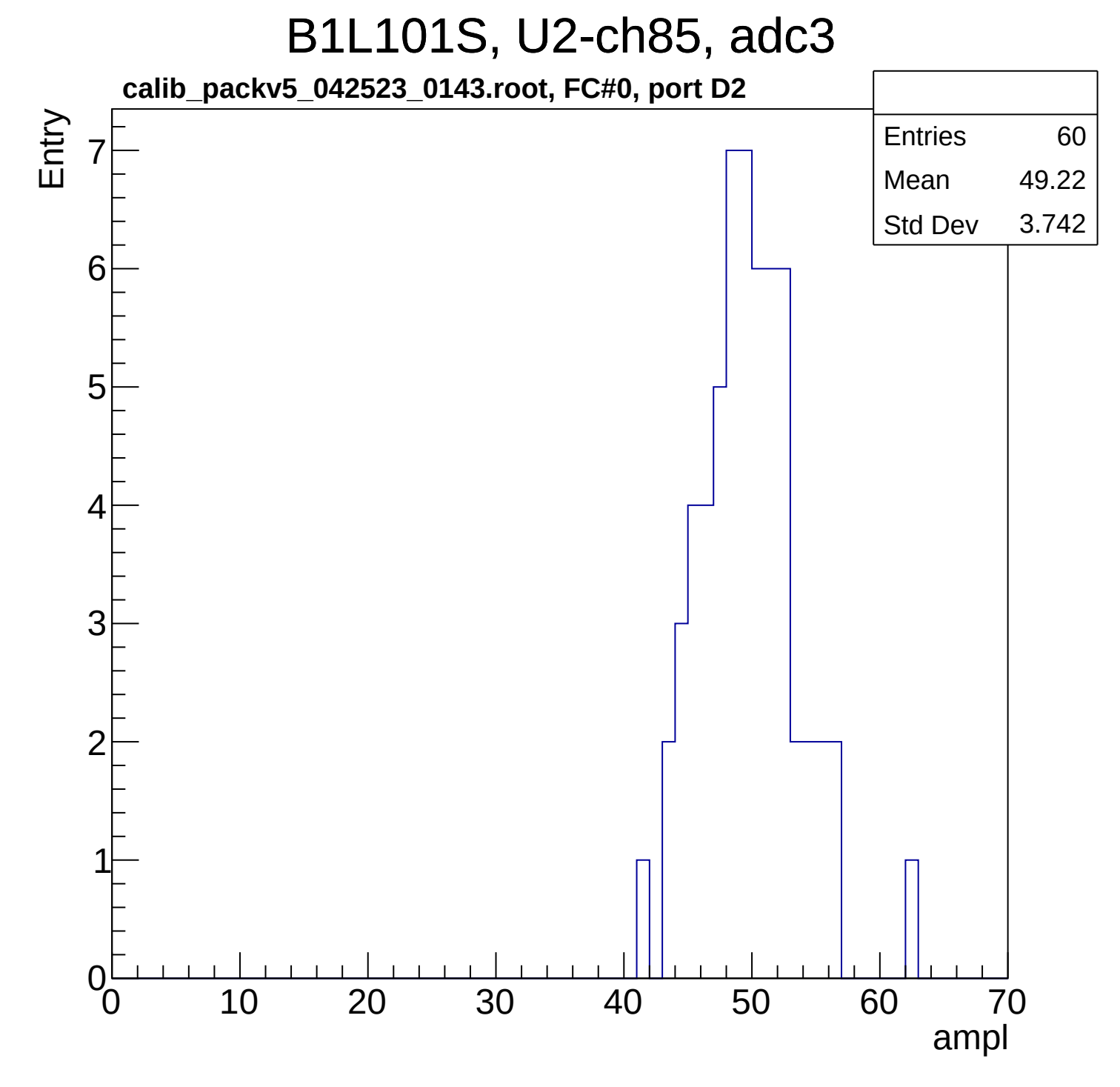

B1L101S, U2-ch84, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 16
Mean 57.5
Std Dev 14.93
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

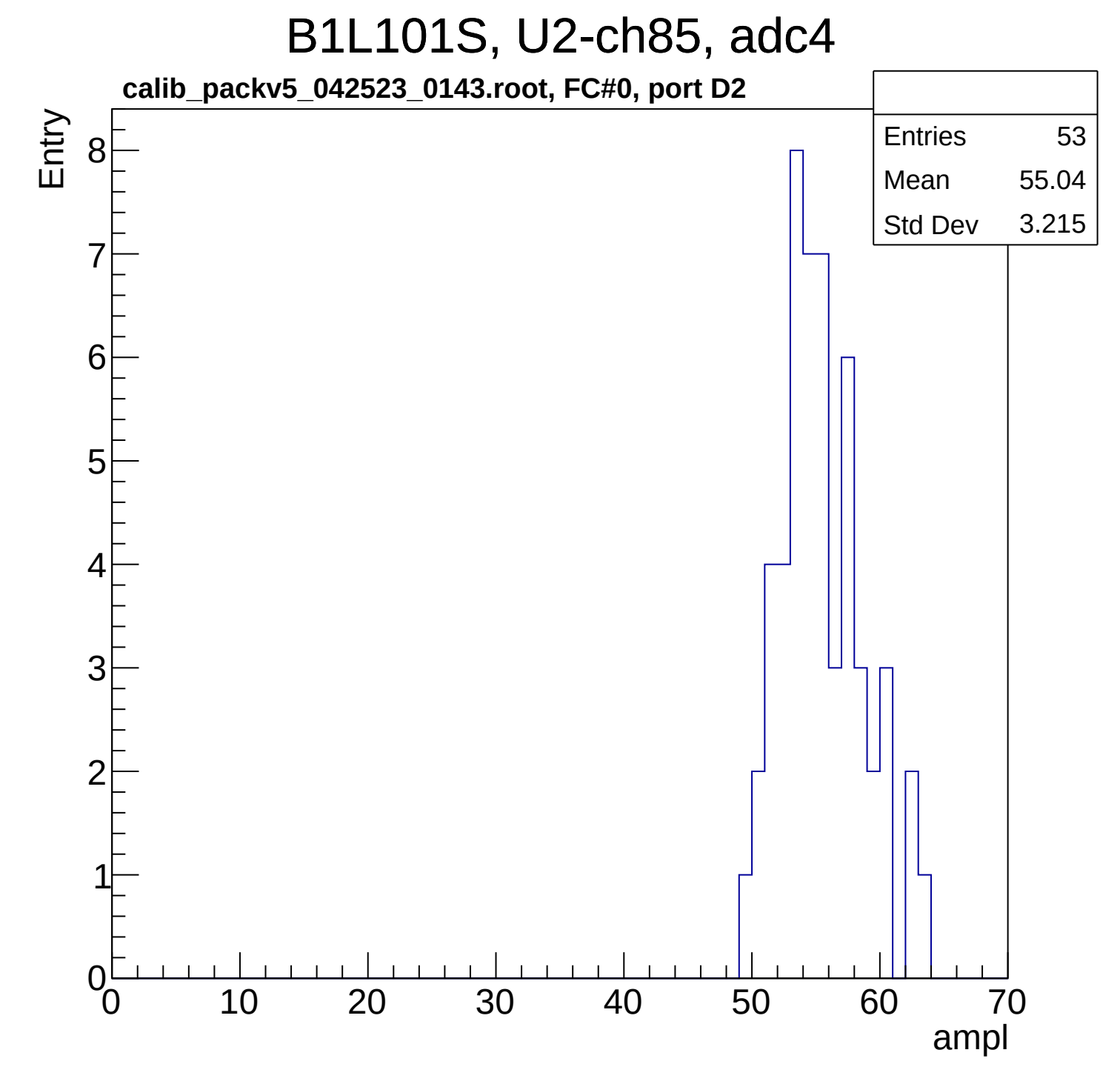

B1L101S, U2-ch84, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

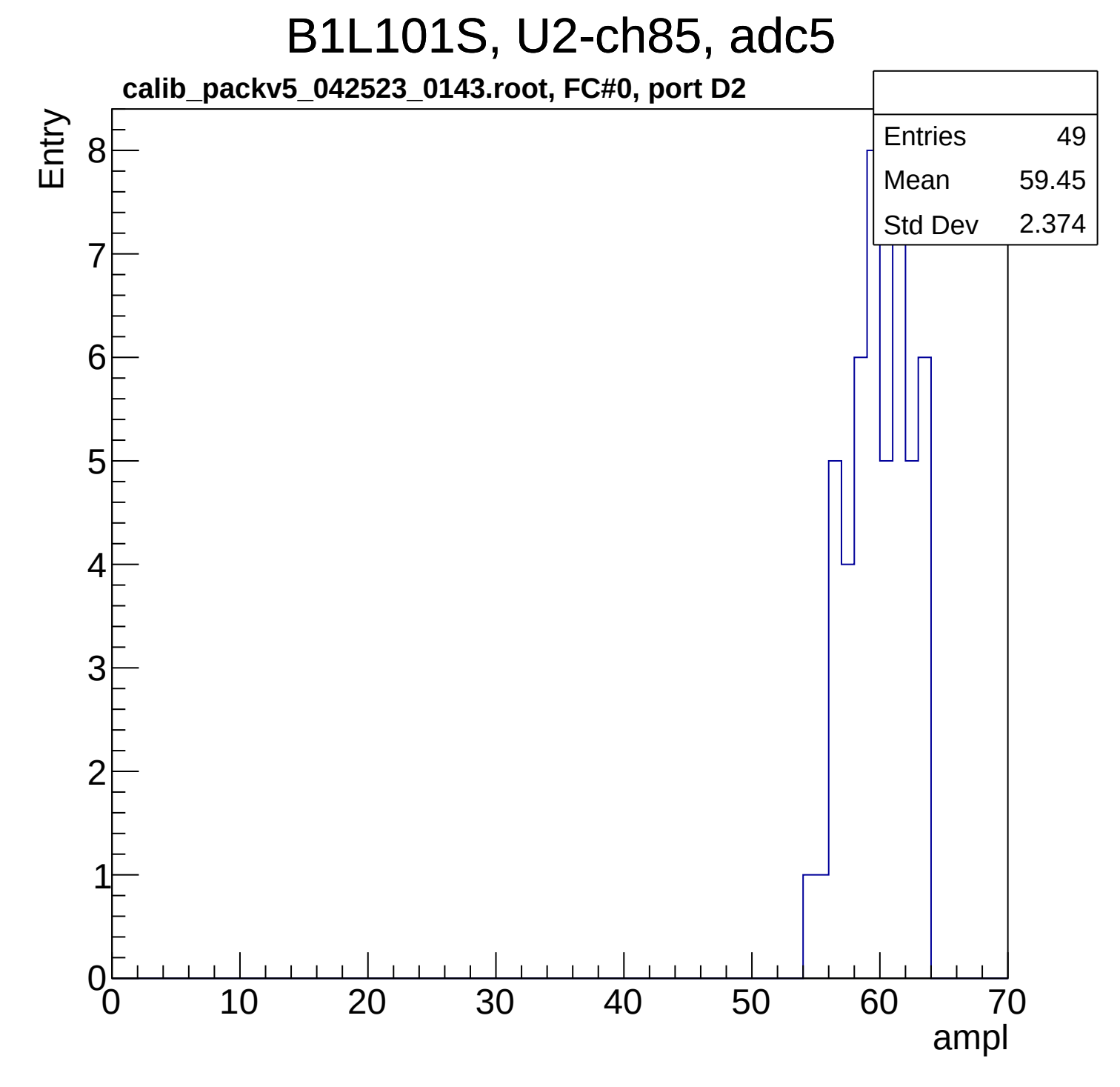

B1L101S, U2-ch85, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 28.87
Std Dev 3.692
Gaus mean : 28.9220
Gaus Width: 3.9716
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

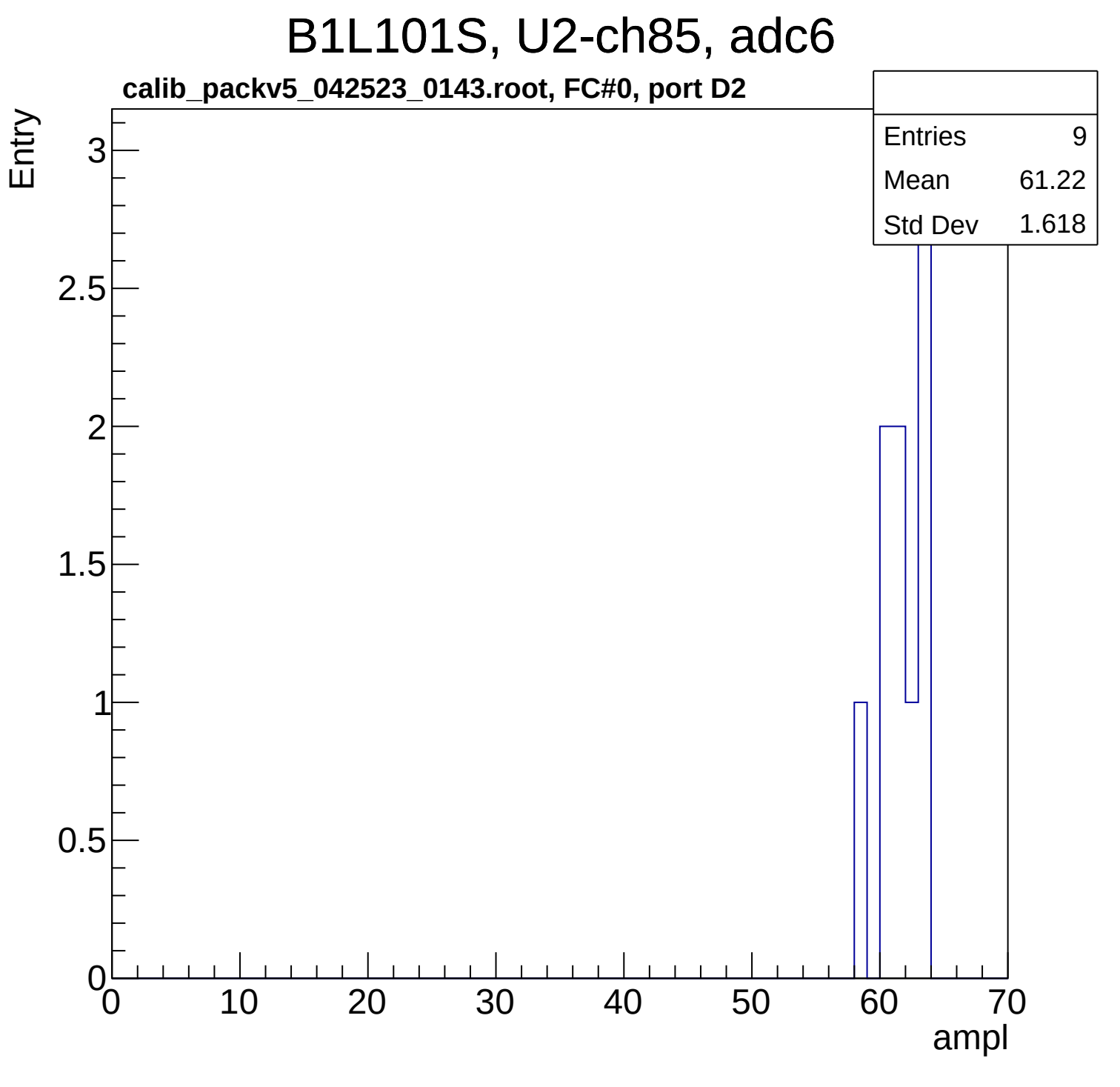

B1L101S, U2-ch85, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 91
Mean 35.24
Std Dev 5.546
Gaus mean : 36.0583
Gaus Width: 4.2392
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

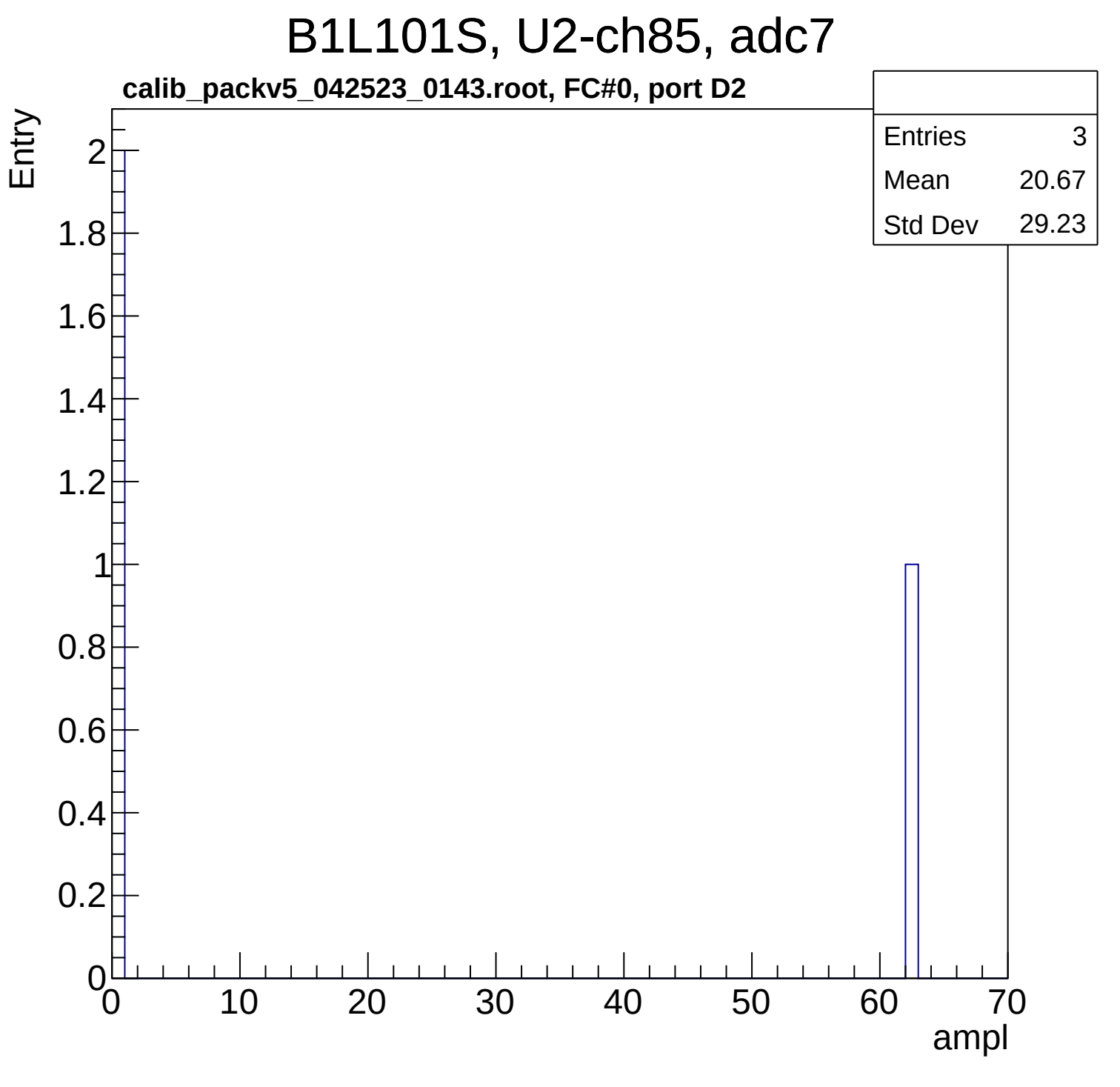

B1L101S, U2-ch85, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 43.15
Std Dev 3.598
Gaus mean : 44.2141
Gaus Width: 4.2508
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

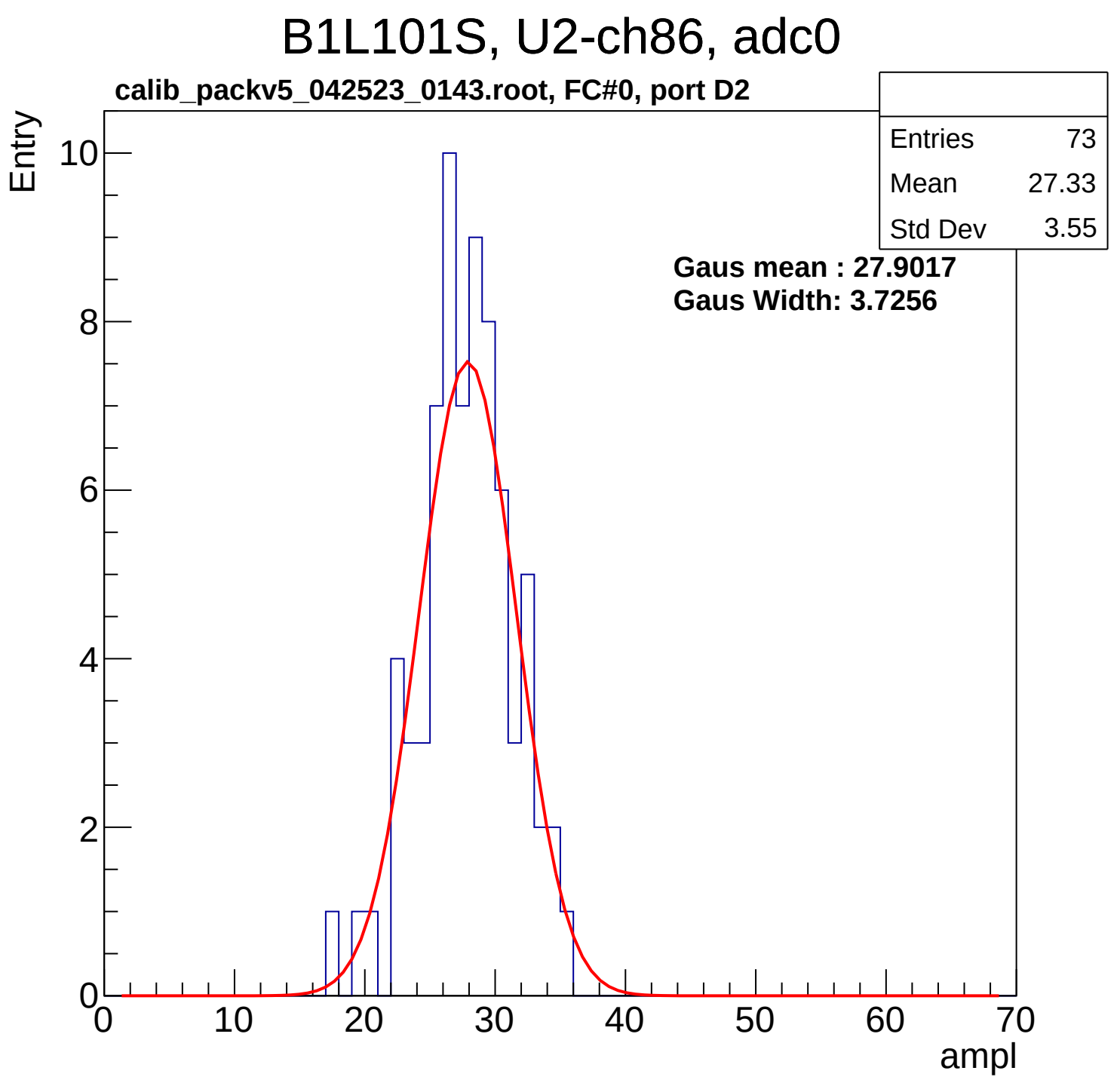

B1L101S, U2-ch85, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 49.22
Std Dev 3.742
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

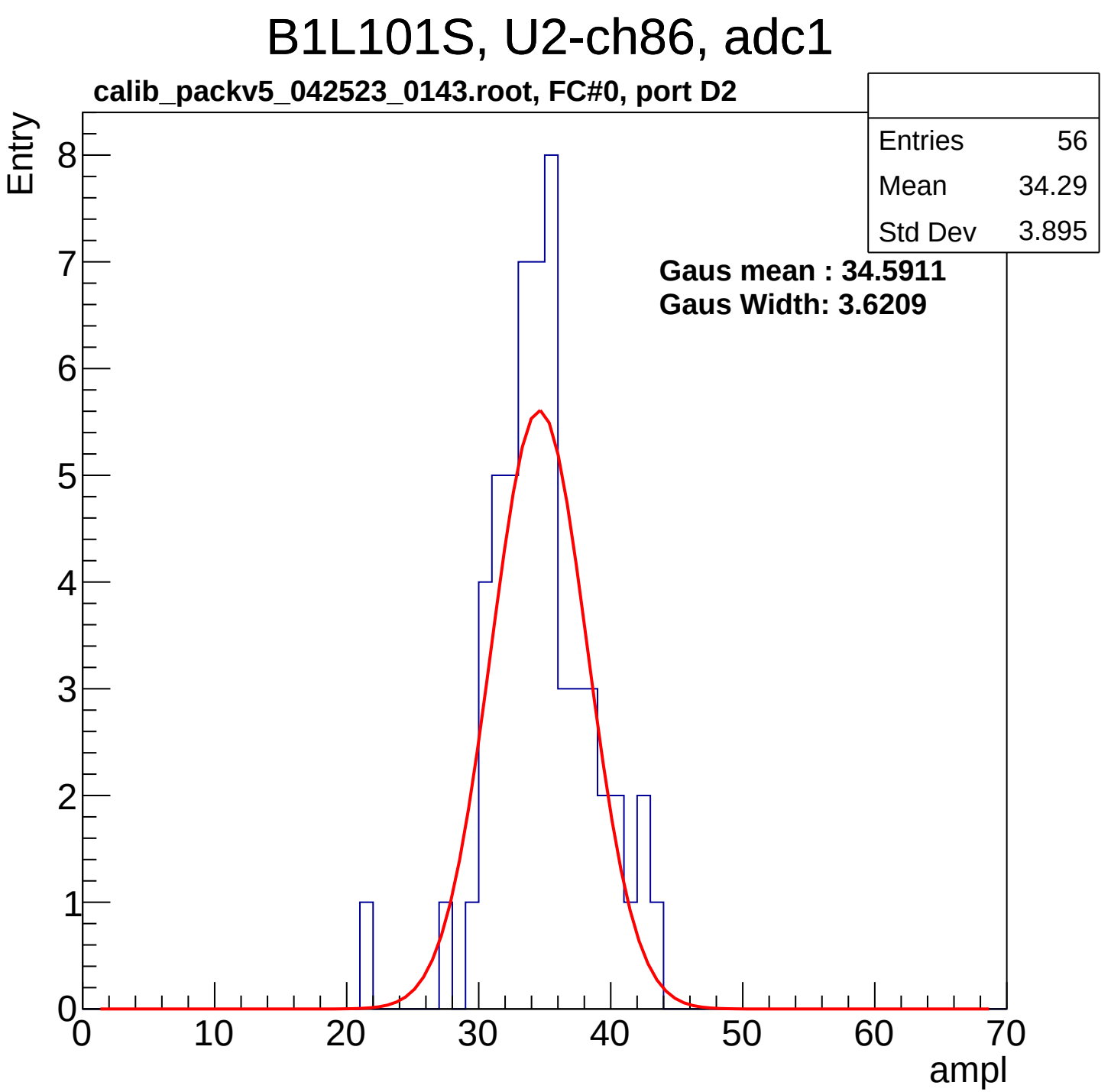

B1L101S, U2-ch85, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 55.04
Std Dev 3.215
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

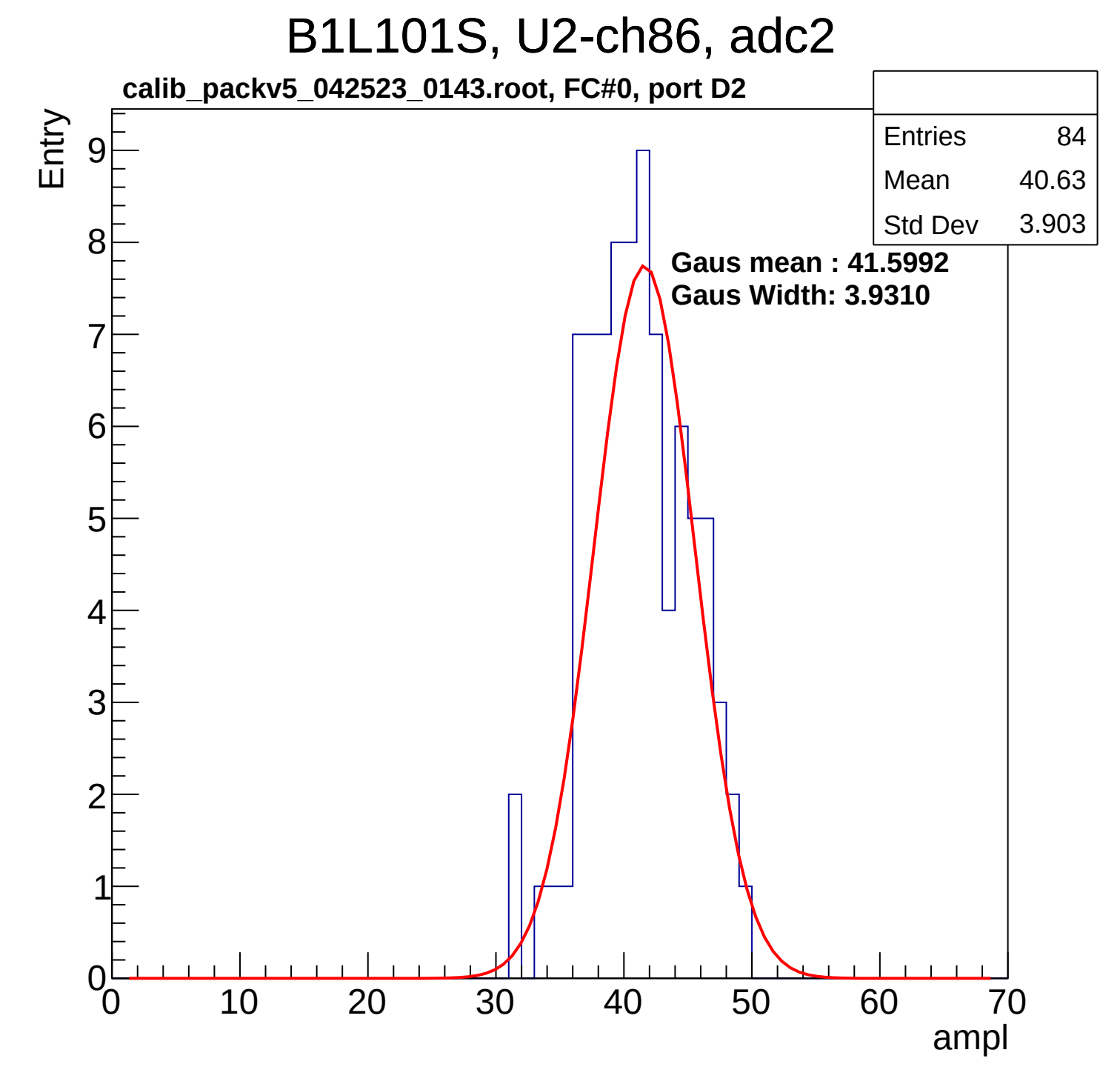

B1L101S, U2-ch85, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 59.45
Std Dev 2.374
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

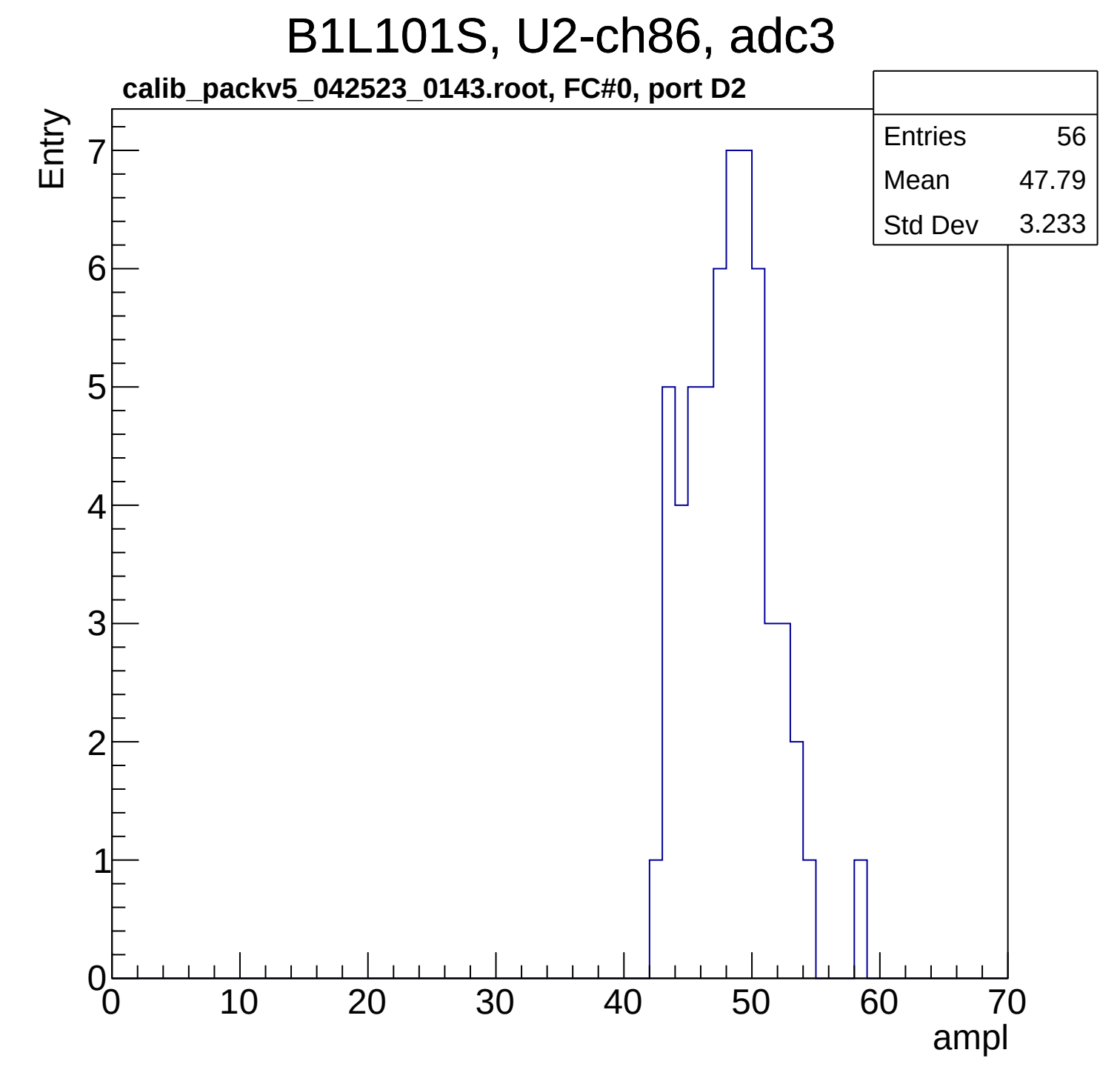

B1L101S, U2-ch85, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 61.22
Std Dev 1.618
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

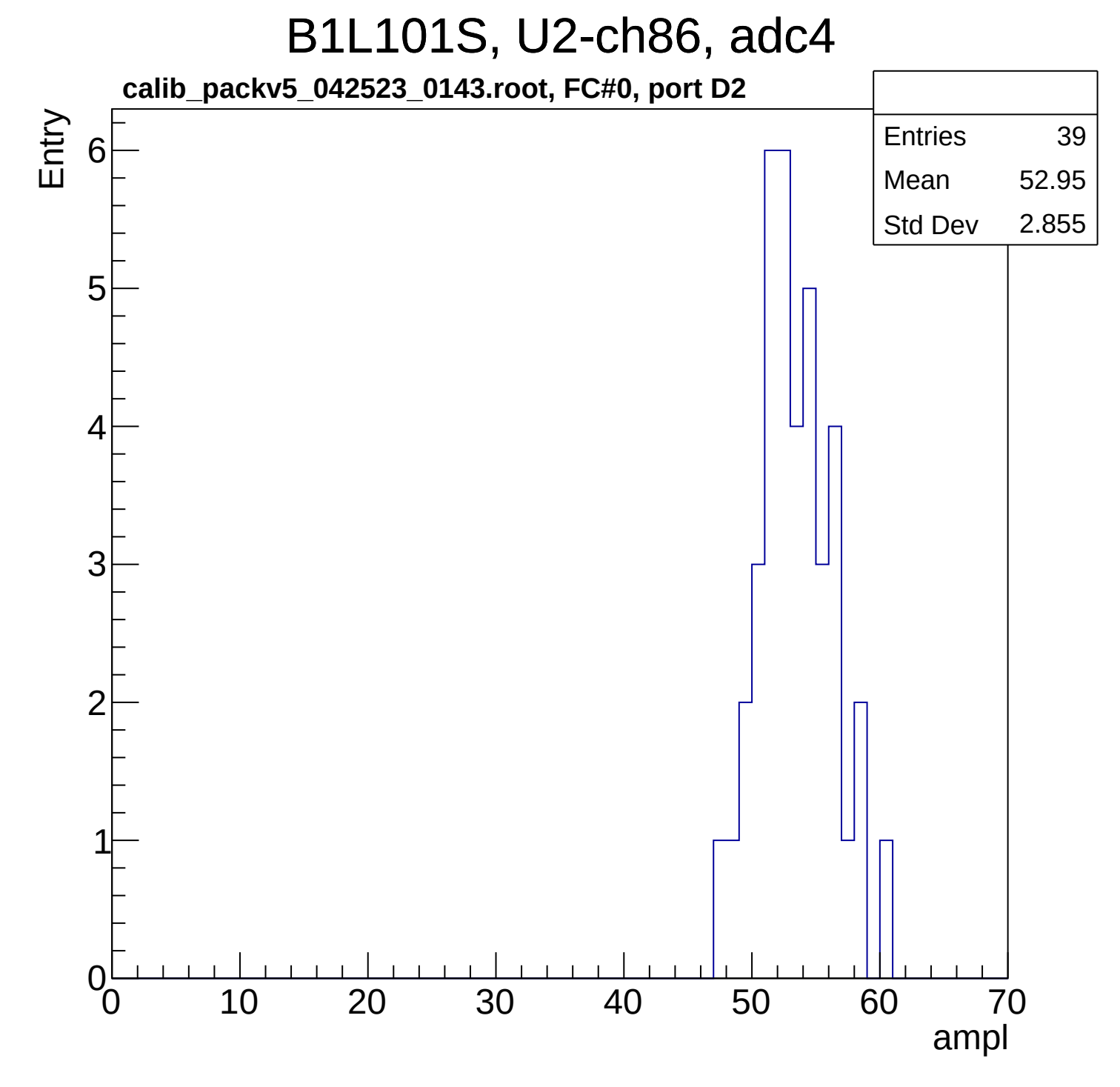

B1L101S, U2-ch85, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 20.67
Std Dev 29.23
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

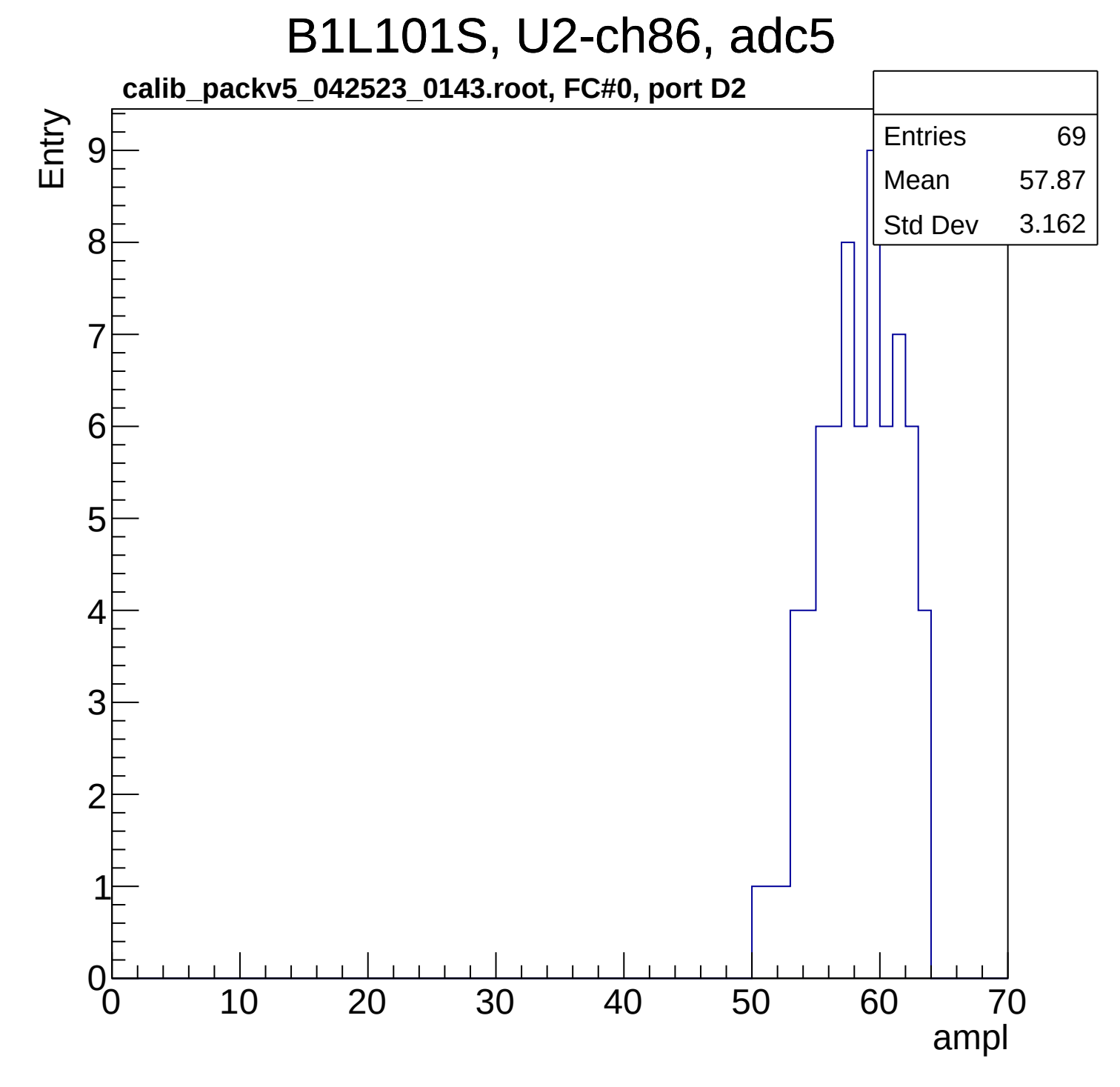

B1L101S, U2-ch86, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 27.33
Std Dev 3.55
Gaus mean : 27.9017
Gaus Width: 3.7256
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

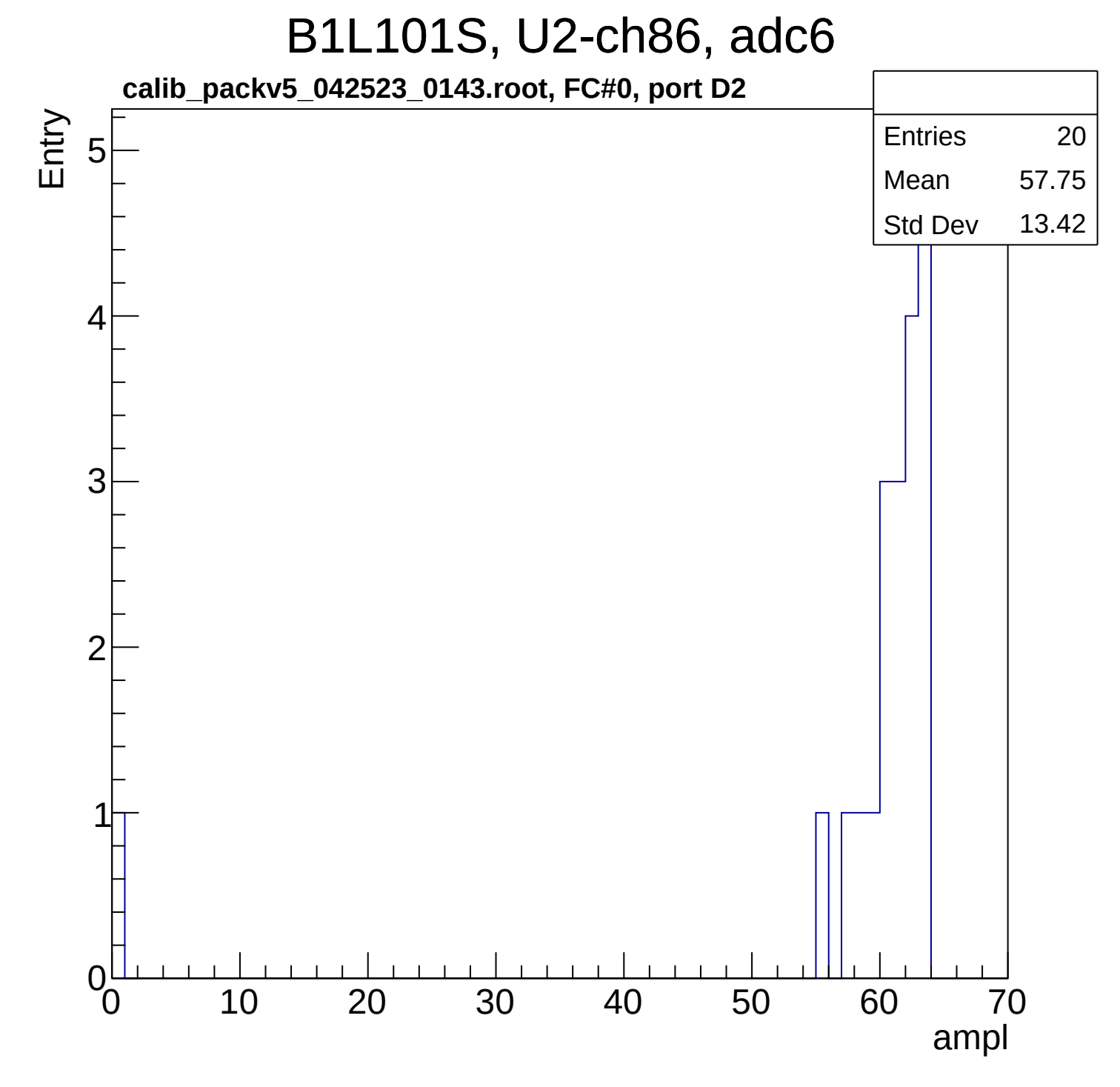

B1L101S, U2-ch86, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 34.29
Std Dev 3.895
Gaus mean : 34.5911
Gaus Width: 3.6209
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

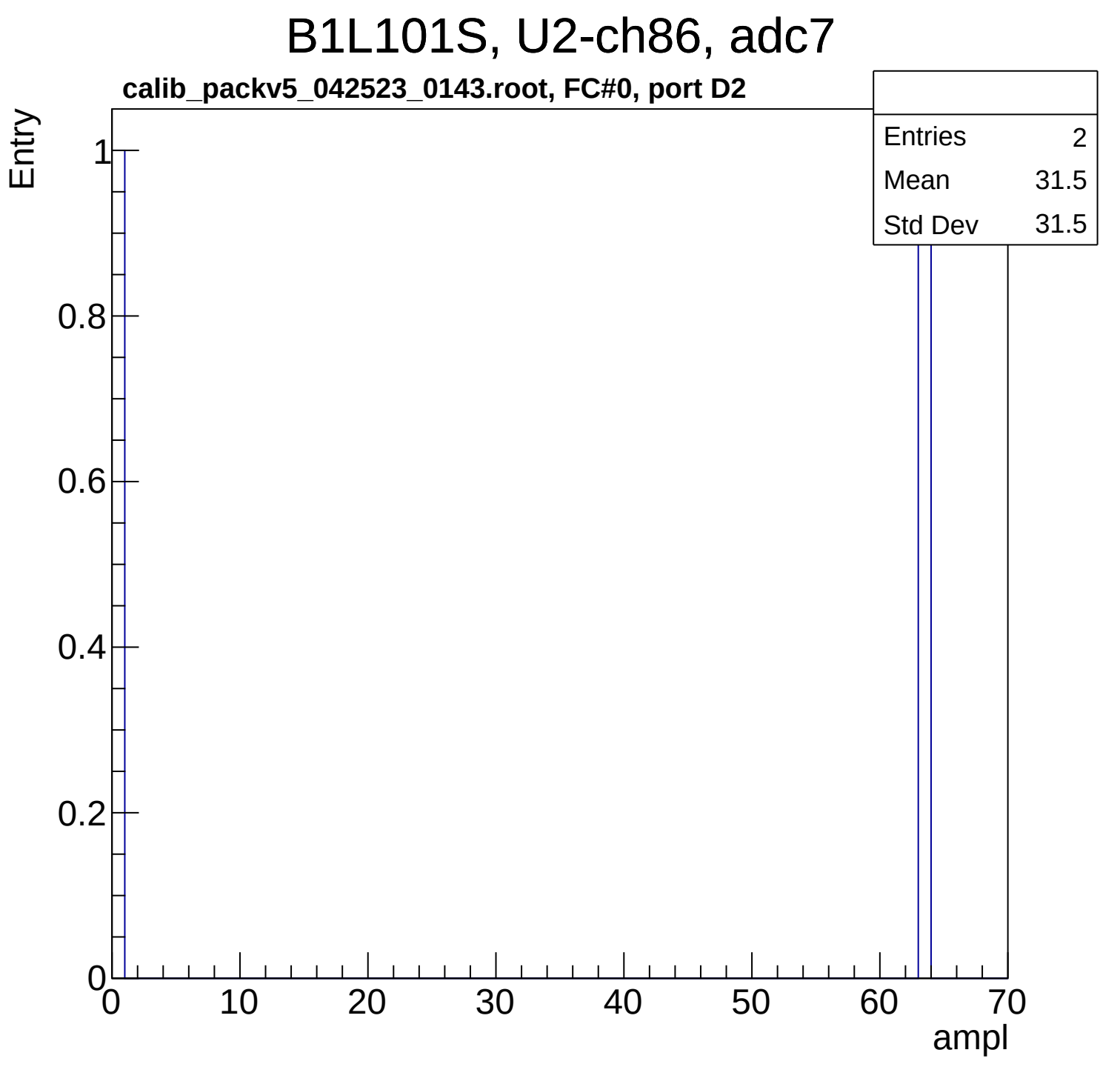

B1L101S, U2-ch86, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 84
Mean 40.63
Std Dev 3.903
Gaus mean : 41.5992
Gaus Width: 3.9310
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

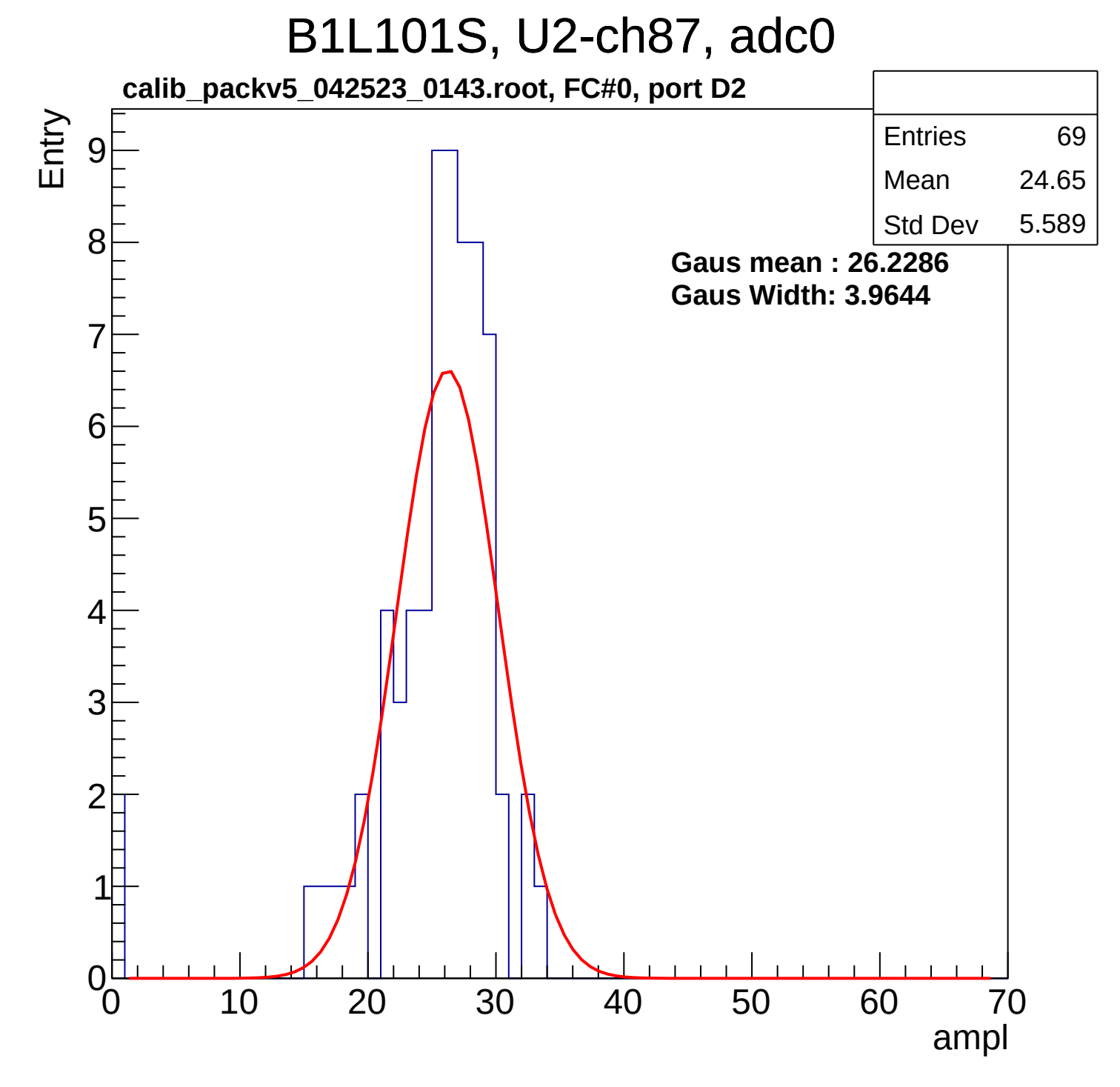

B1L101S, U2-ch86, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 47.79
Std Dev 3.233
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

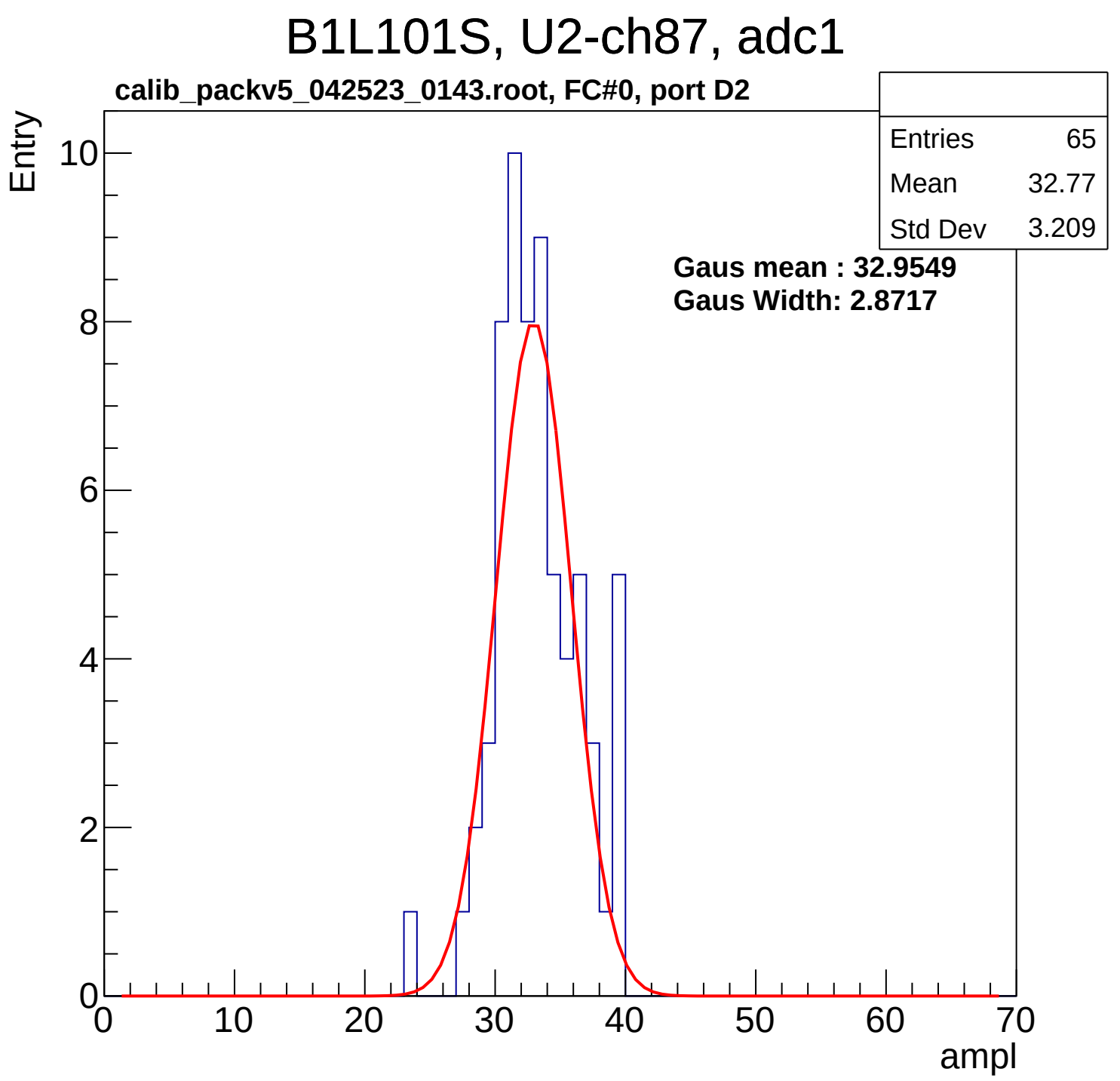

B1L101S, U2-ch86, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 39
Mean 52.95
Std Dev 2.855
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

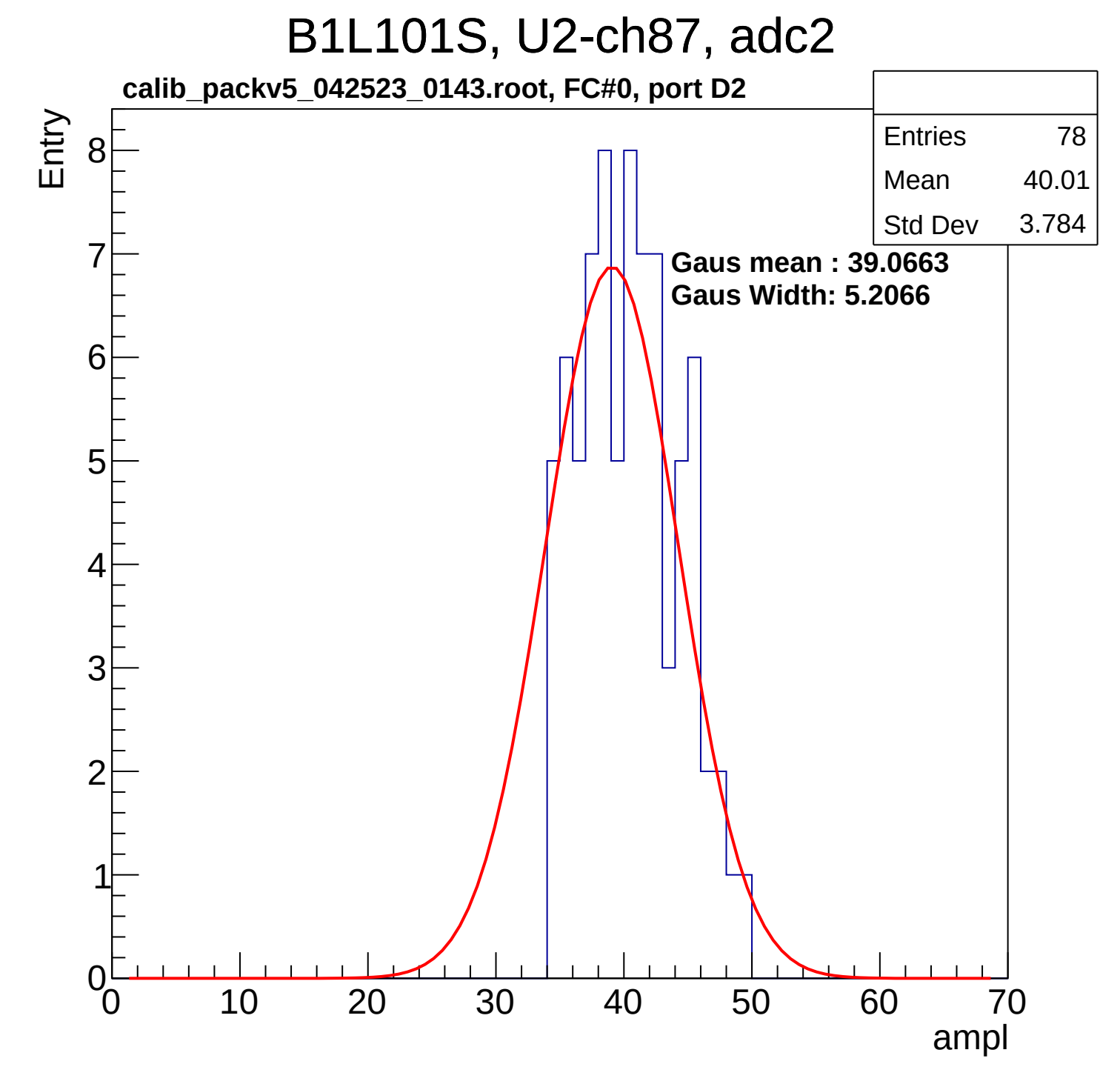

B1L101S, U2-ch86, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 57.87
Std Dev 3.162
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

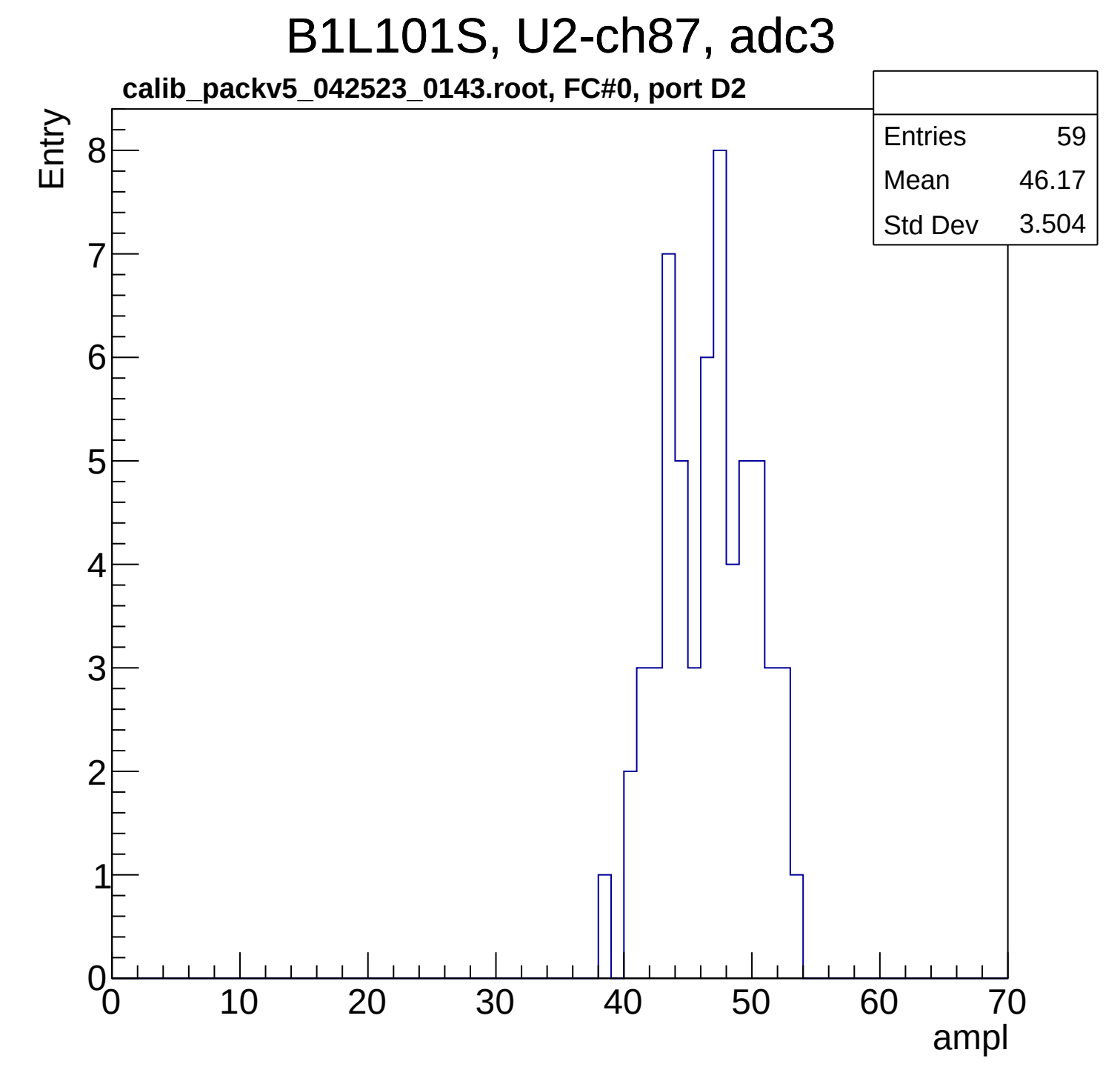

B1L101S, U2-ch86, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 20
Mean 57.75
Std Dev 13.42
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

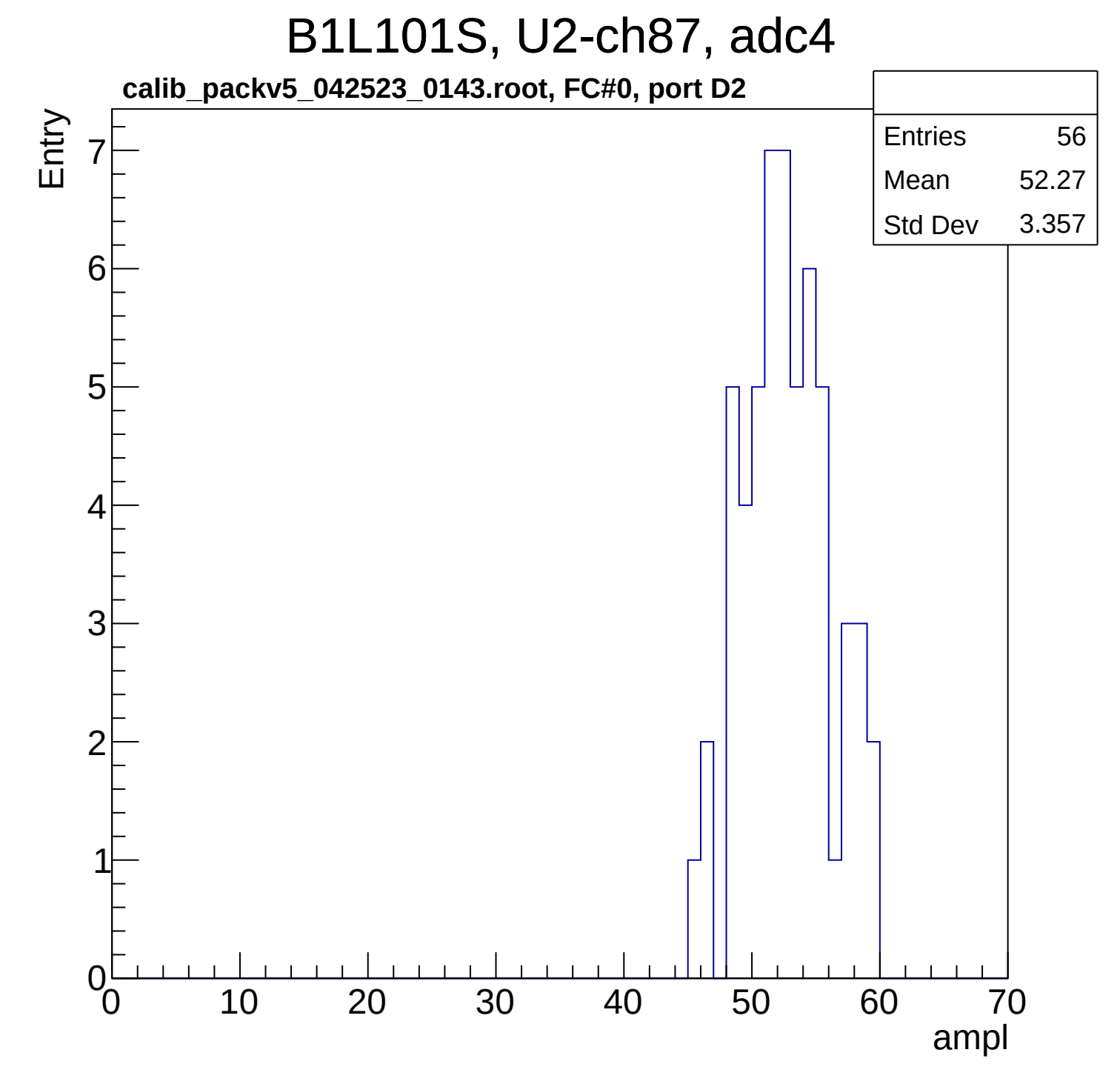

B1L101S, U2-ch86, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

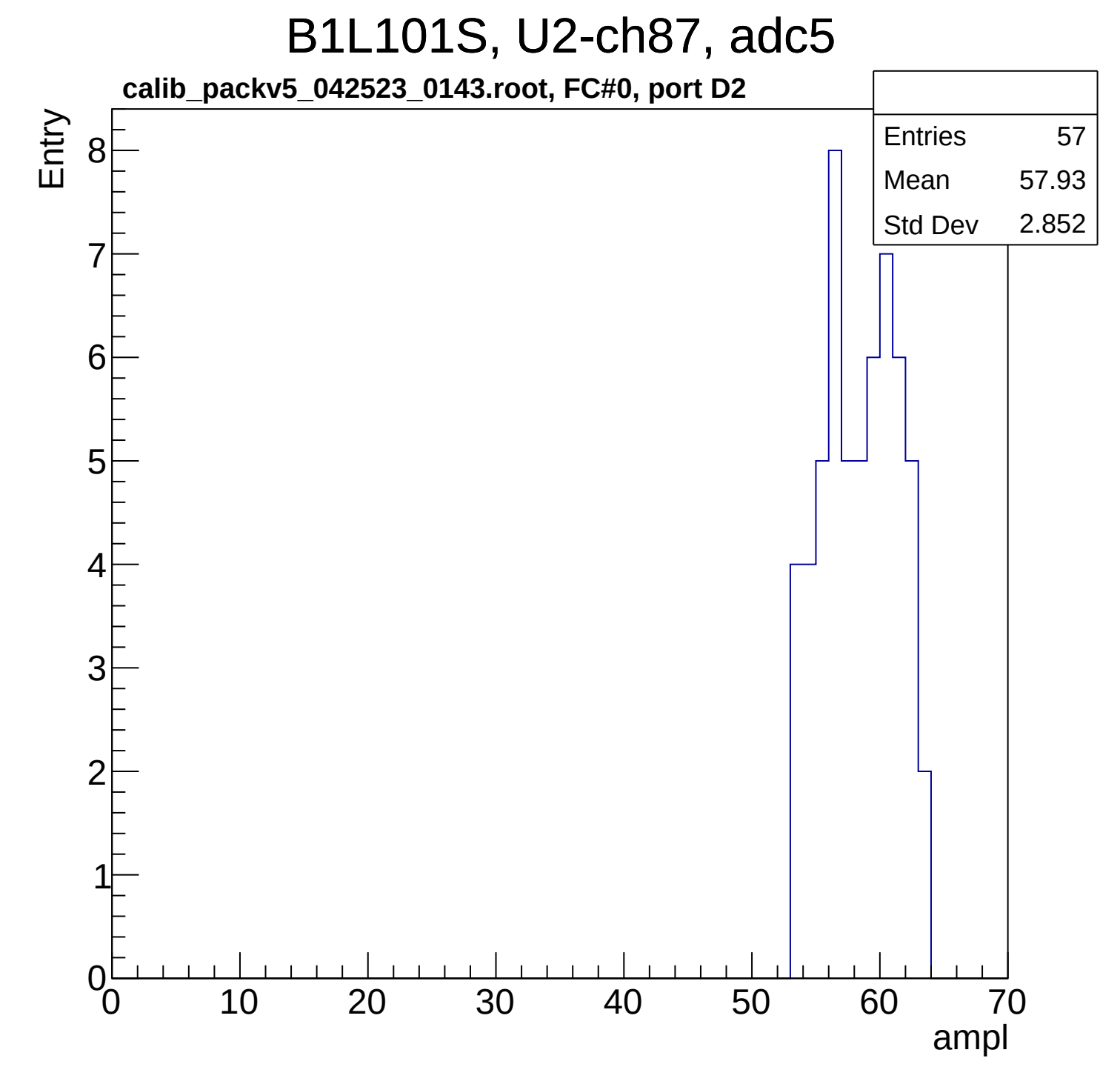

B1L101S, U2-ch87, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 24.65
Std Dev 5.589
Gaus mean : 26.2286
Gaus Width: 3.9644
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

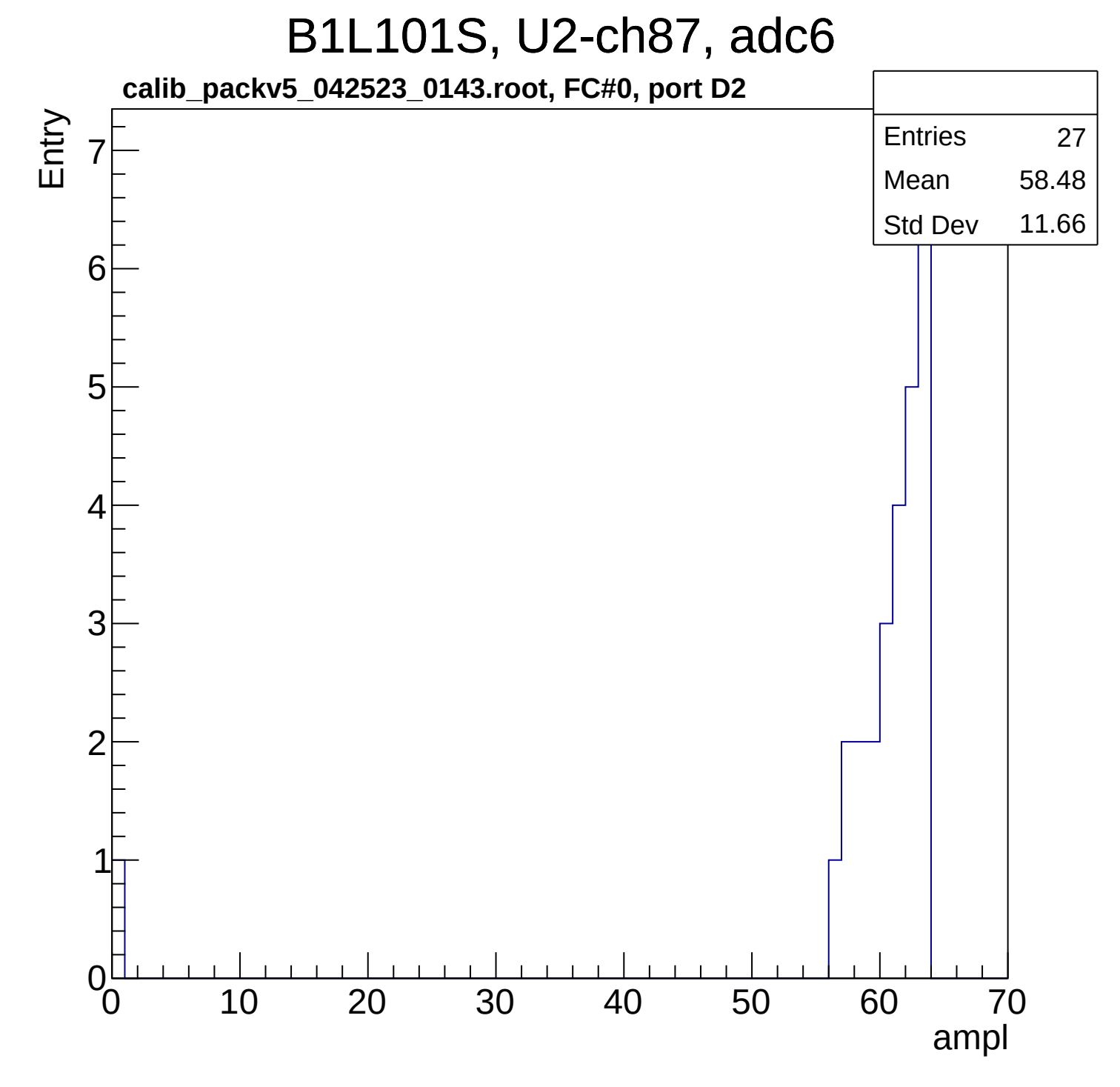

B1L101S, U2-ch87, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 32.77
Std Dev 3.209
Gaus mean : 32.9549
Gaus Width: 2.8717
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

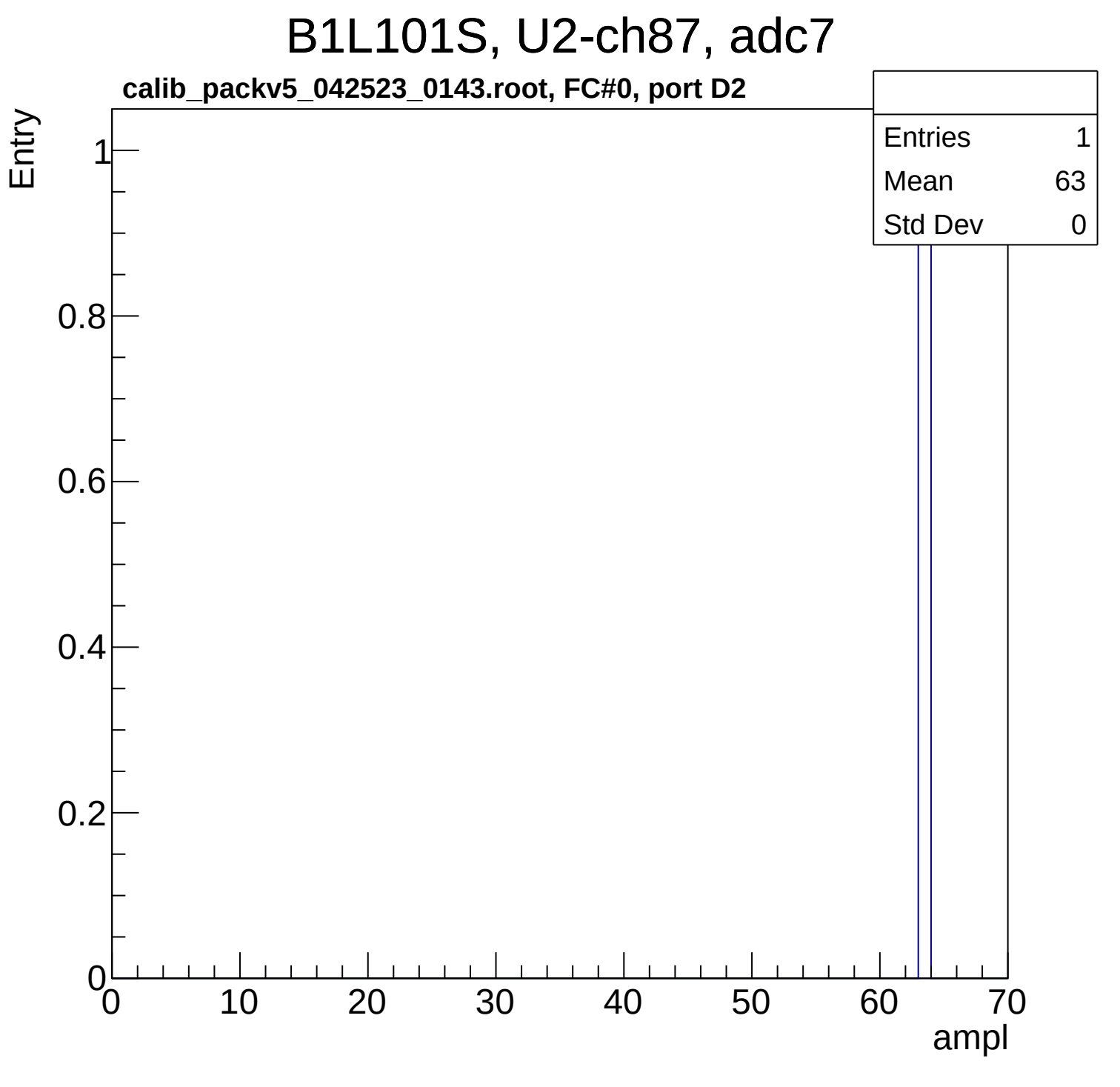

B1L101S, U2-ch87, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 40.01
Std Dev 3.784
Gaus mean : 39.0663
Gaus Width: 5.2066
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

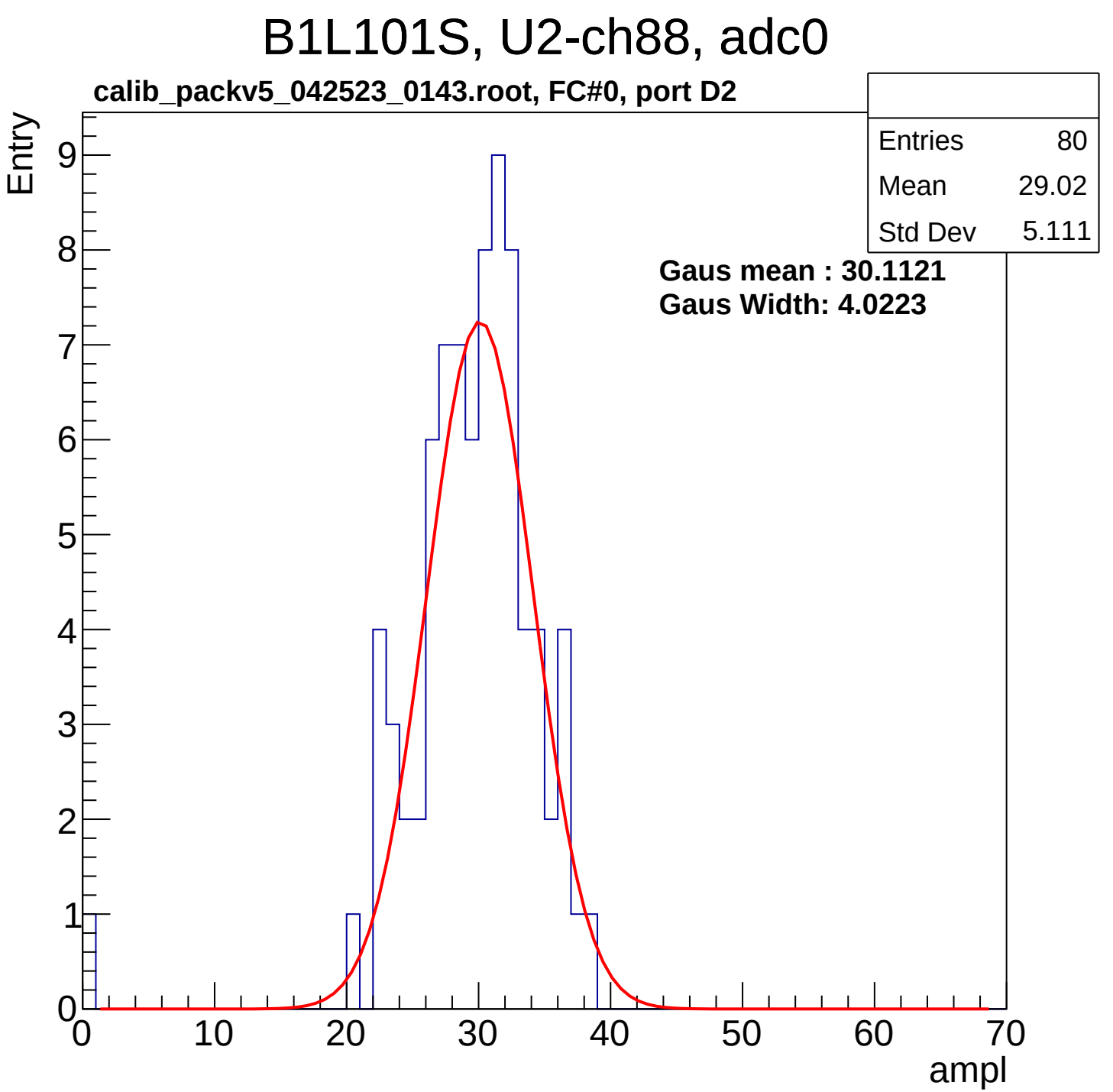

B1L101S, U2-ch87, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 46.17
Std Dev 3.504
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

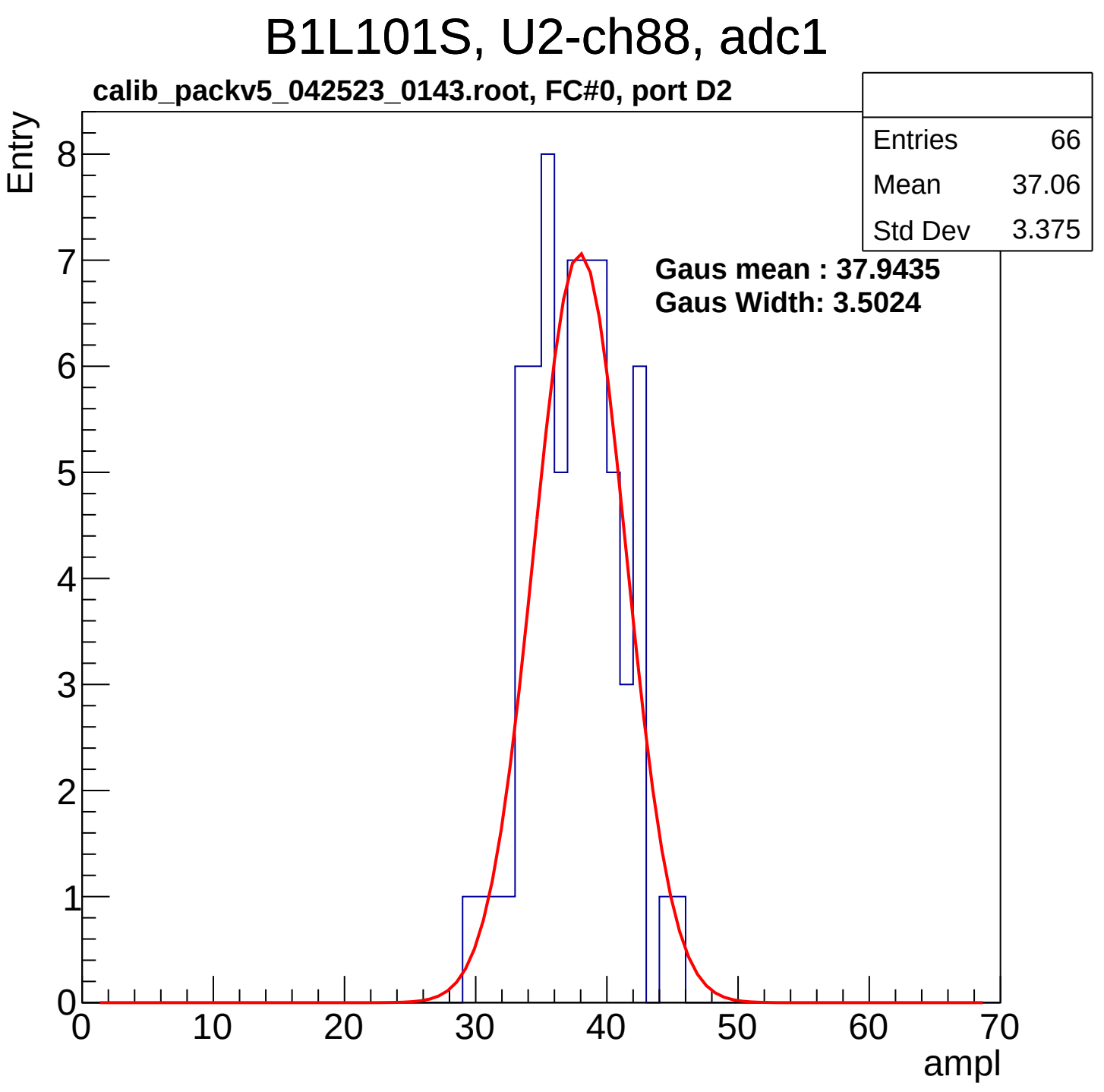

B1L101S, U2-ch87, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 52.27
Std Dev 3.357
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

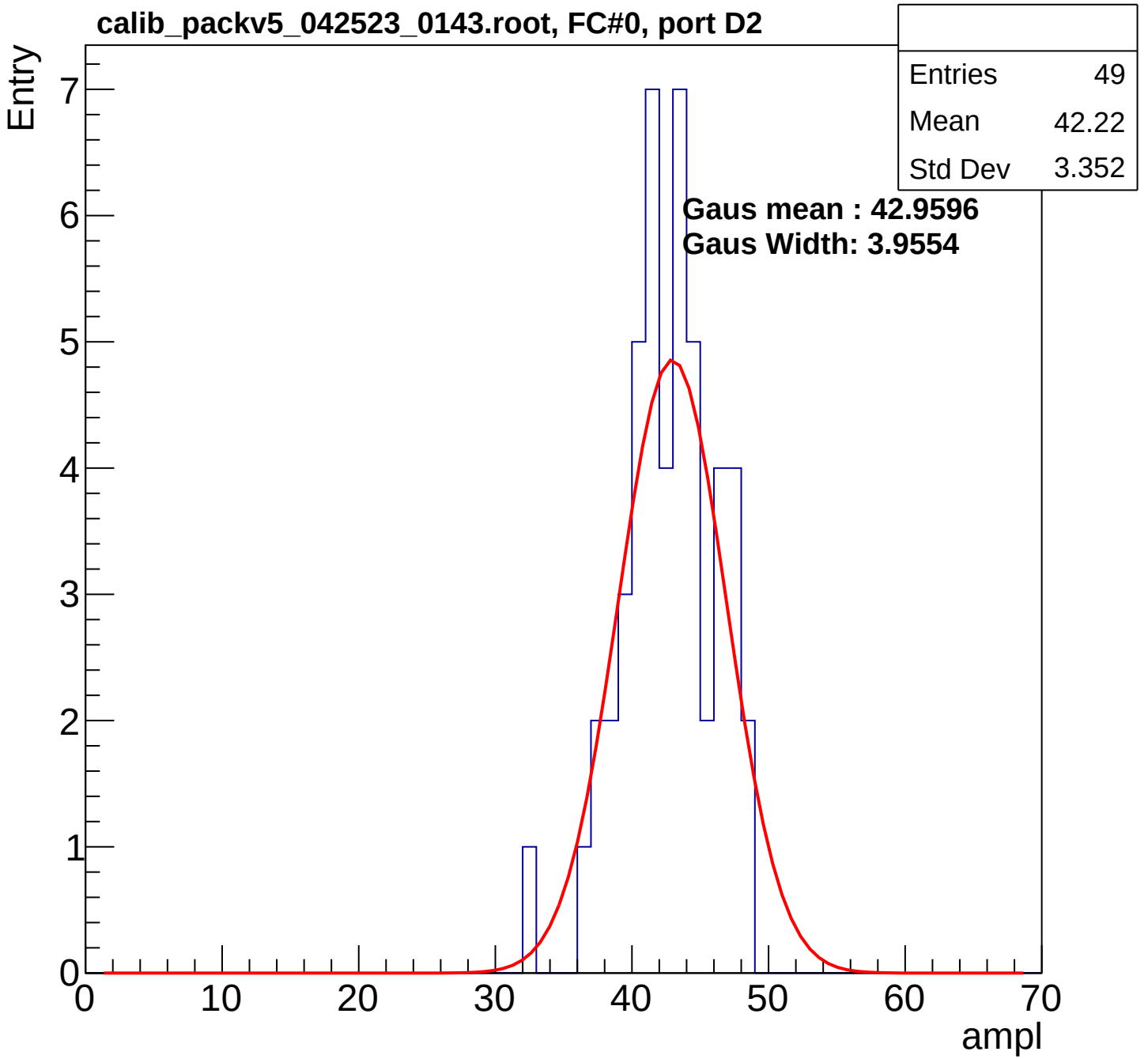

B1L101S, U2-ch87, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 57.93
Std Dev 2.852
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

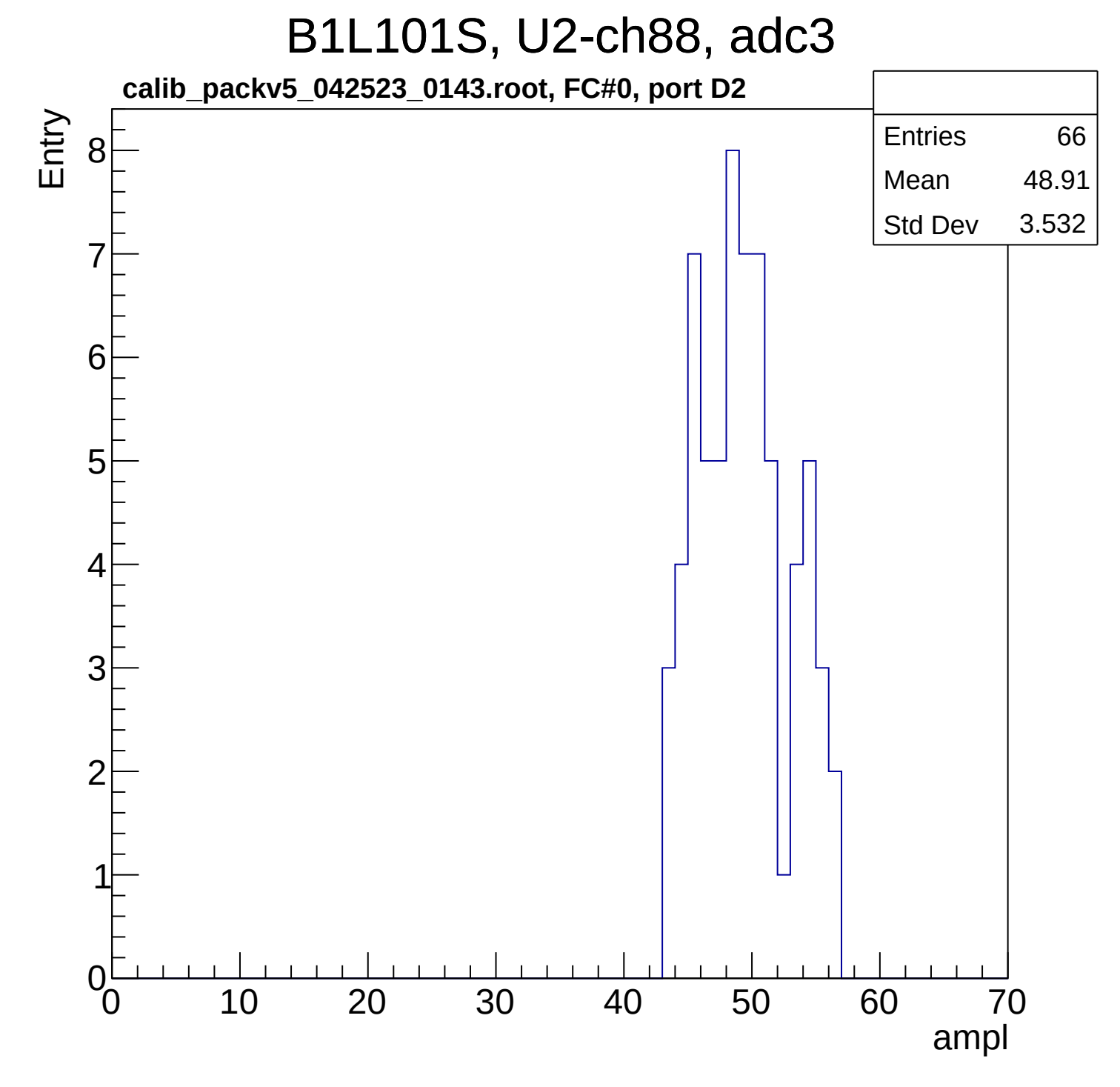

B1L101S, U2-ch87, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 27
Mean 58.48
Std Dev 11.66
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

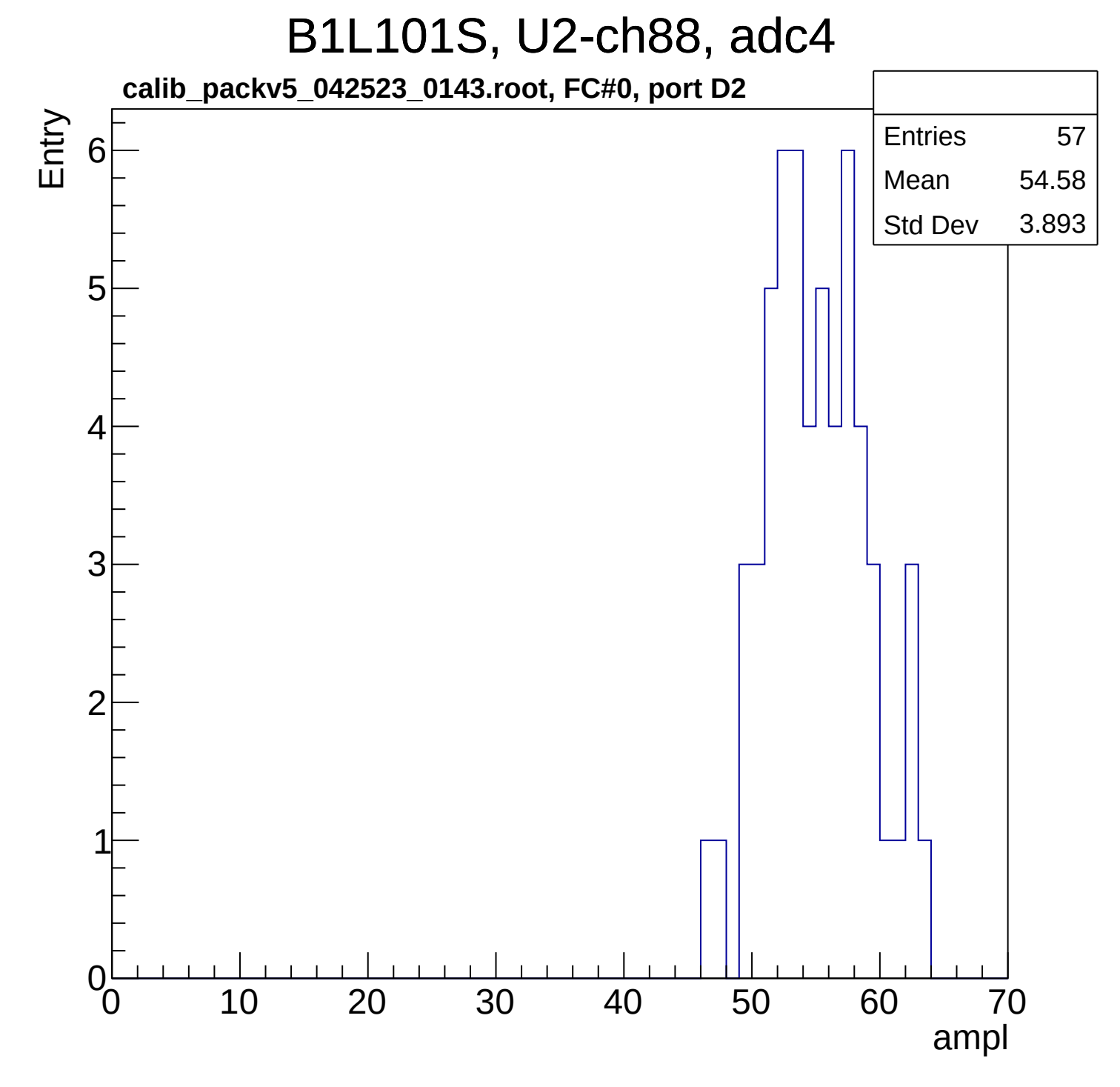

B1L101S, U2-ch87, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

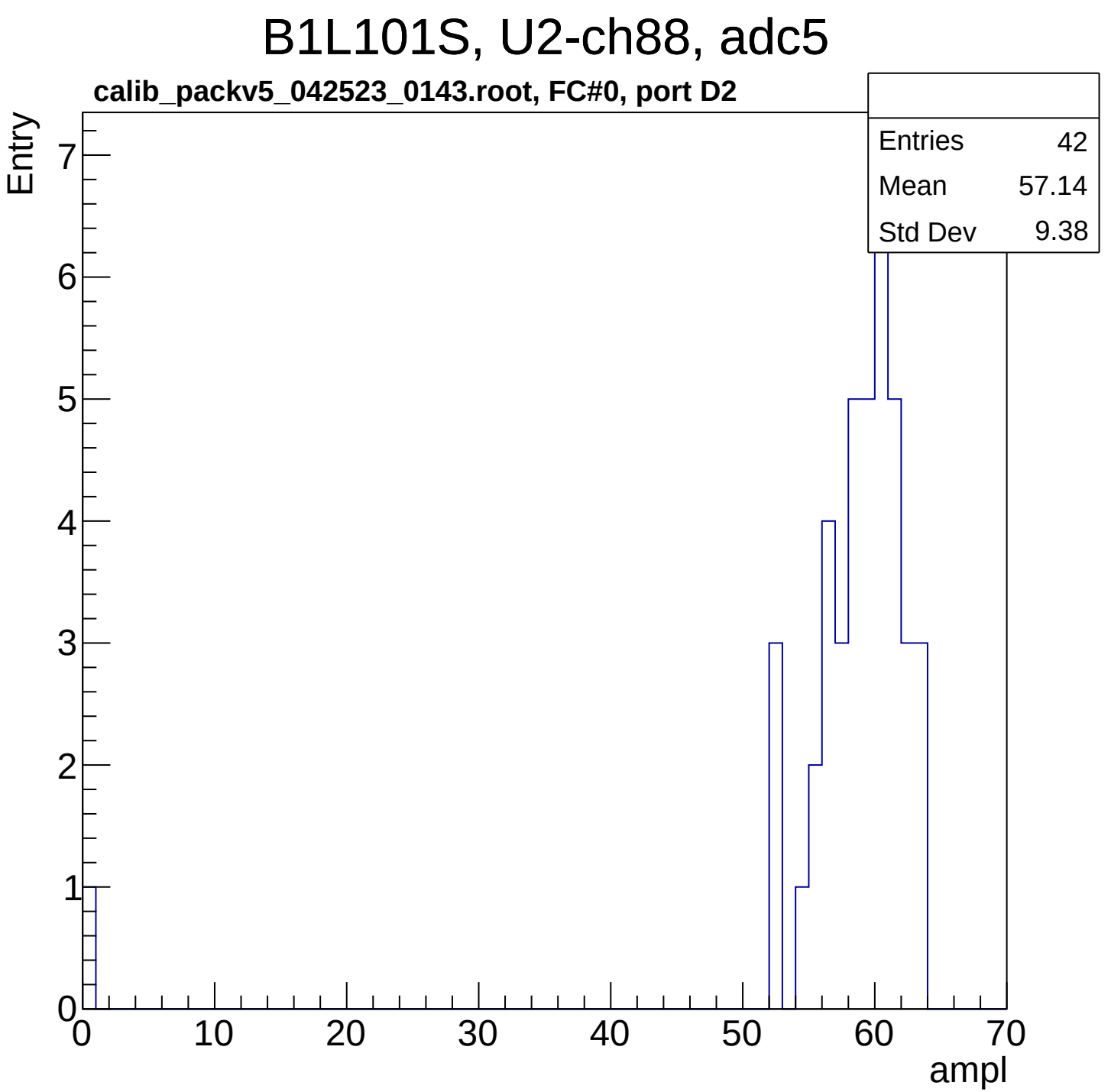

B1L101S, U2-ch88, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 80
Mean 29.02
Std Dev 5.111
Gaus mean : 30.1121
Gaus Width: 4.0223
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

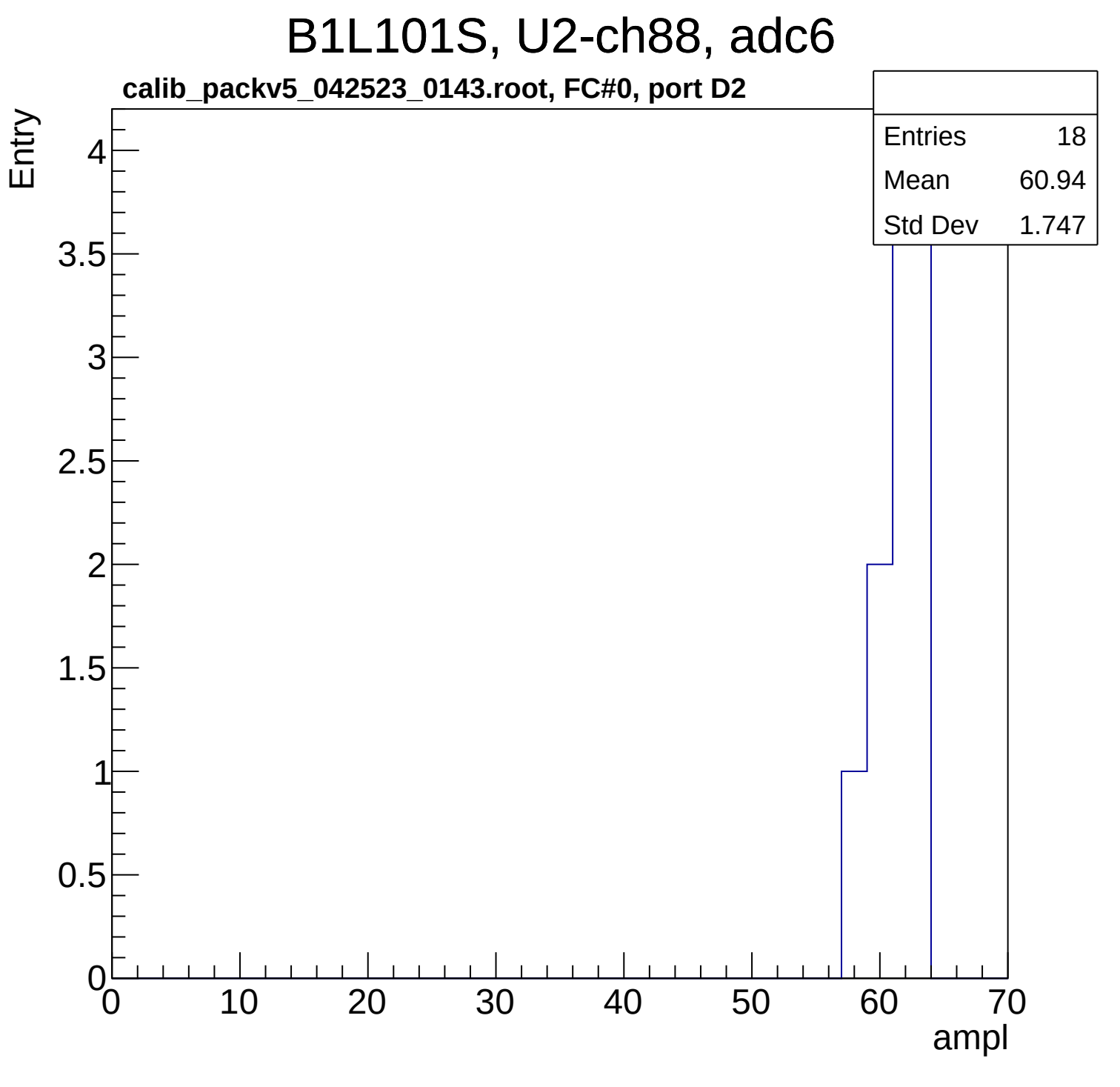

B1L101S, U2-ch88, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 37.06
Std Dev 3.375
Gaus mean : 37.9435
Gaus Width: 3.5024
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

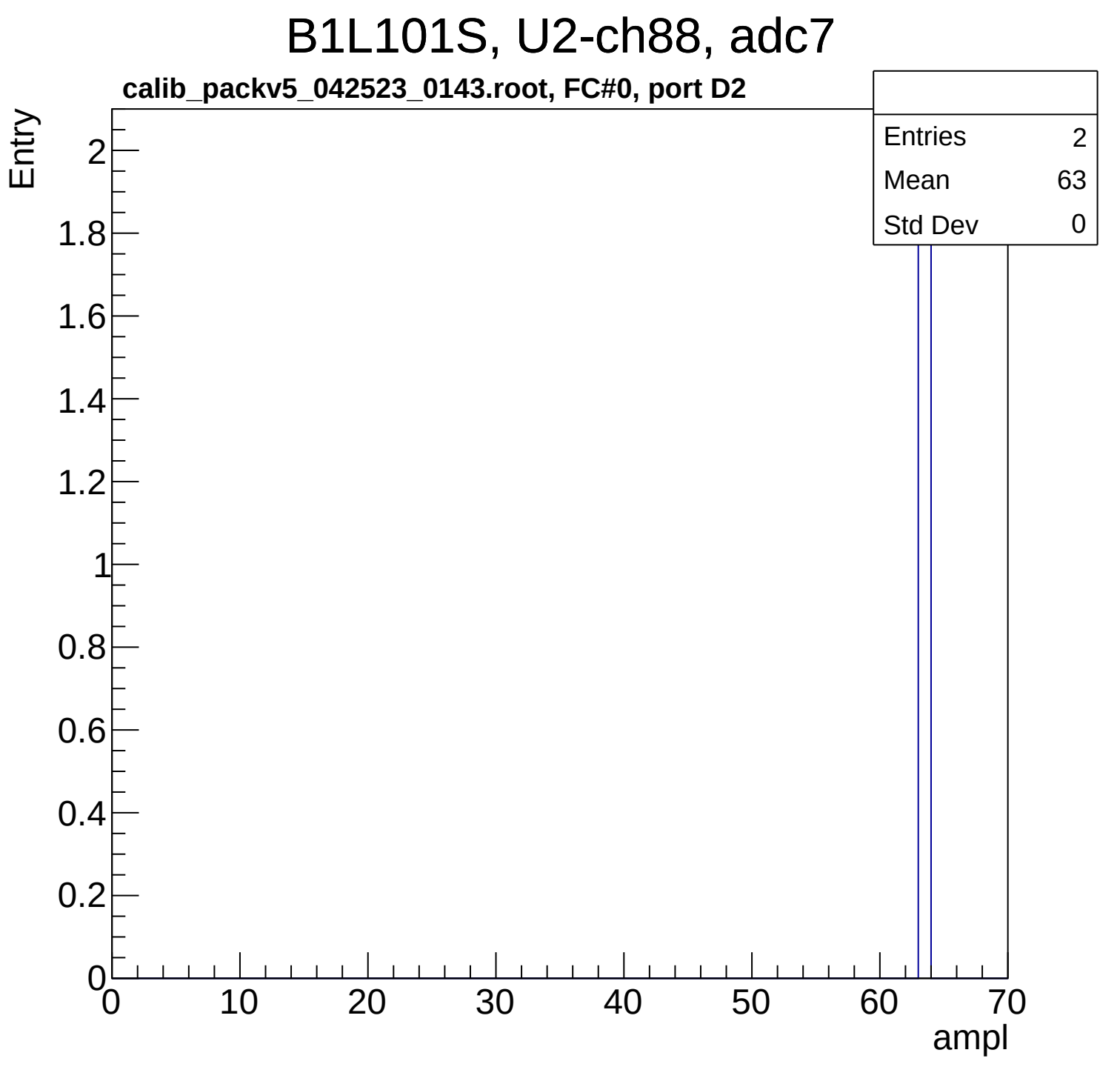

B1L101S, U2-ch88, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 42.22
Std Dev 3.352
Gaus mean : 42.9596
Gaus Width: 3.9554
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

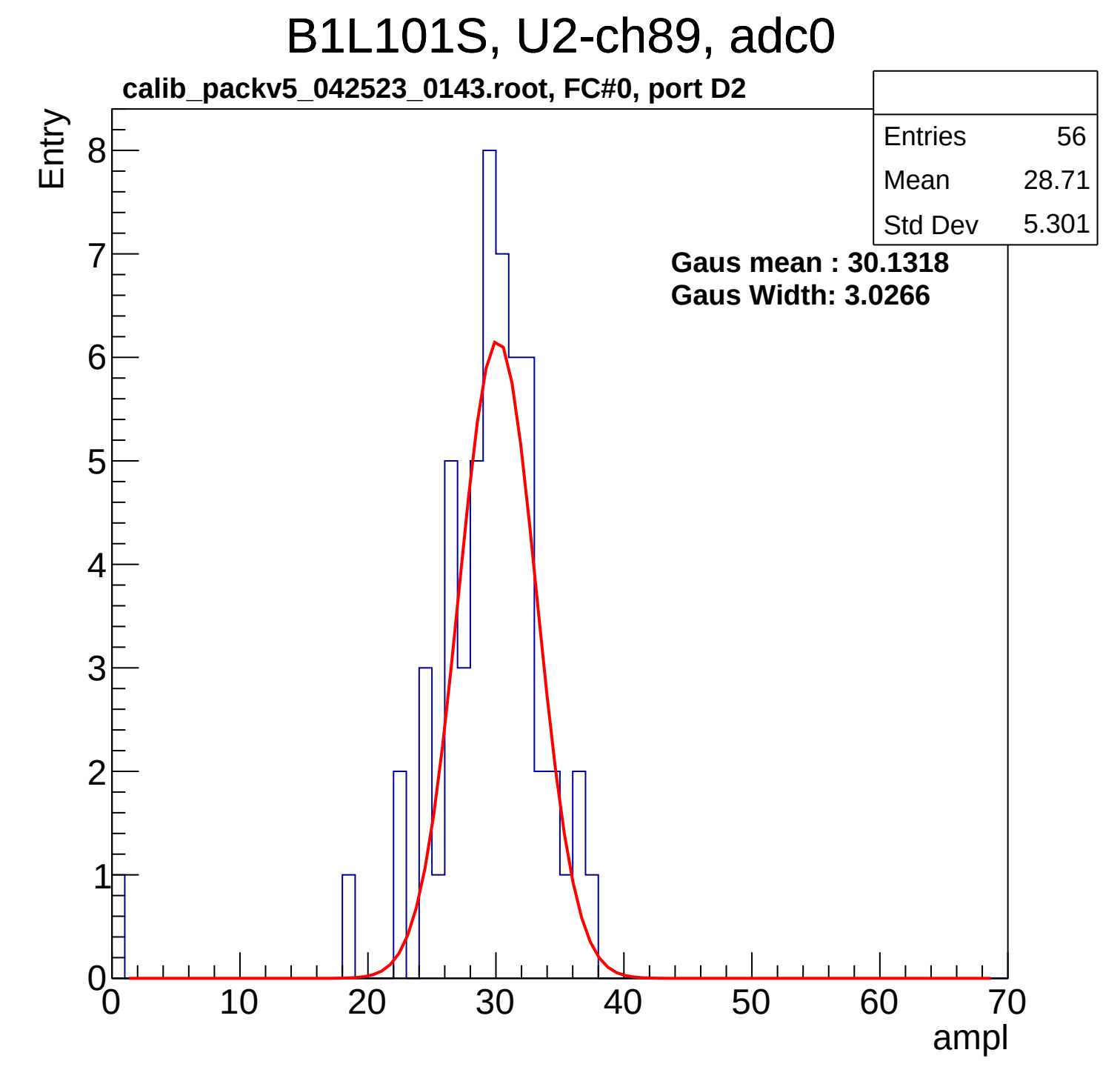

B1L101S, U2-ch88, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 48.91
Std Dev 3.532
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

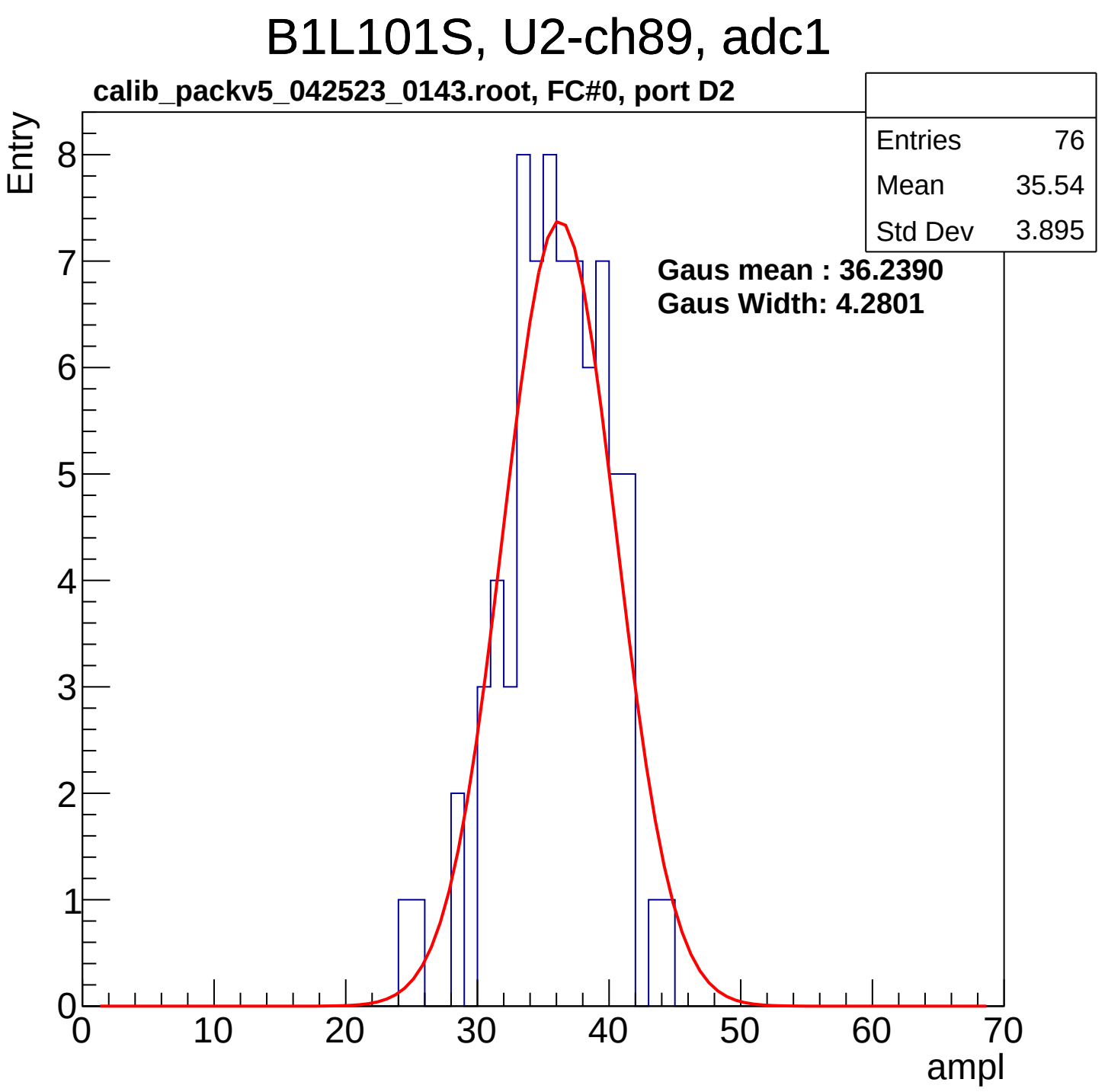

B1L101S, U2-ch88, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 54.58
Std Dev 3.893
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

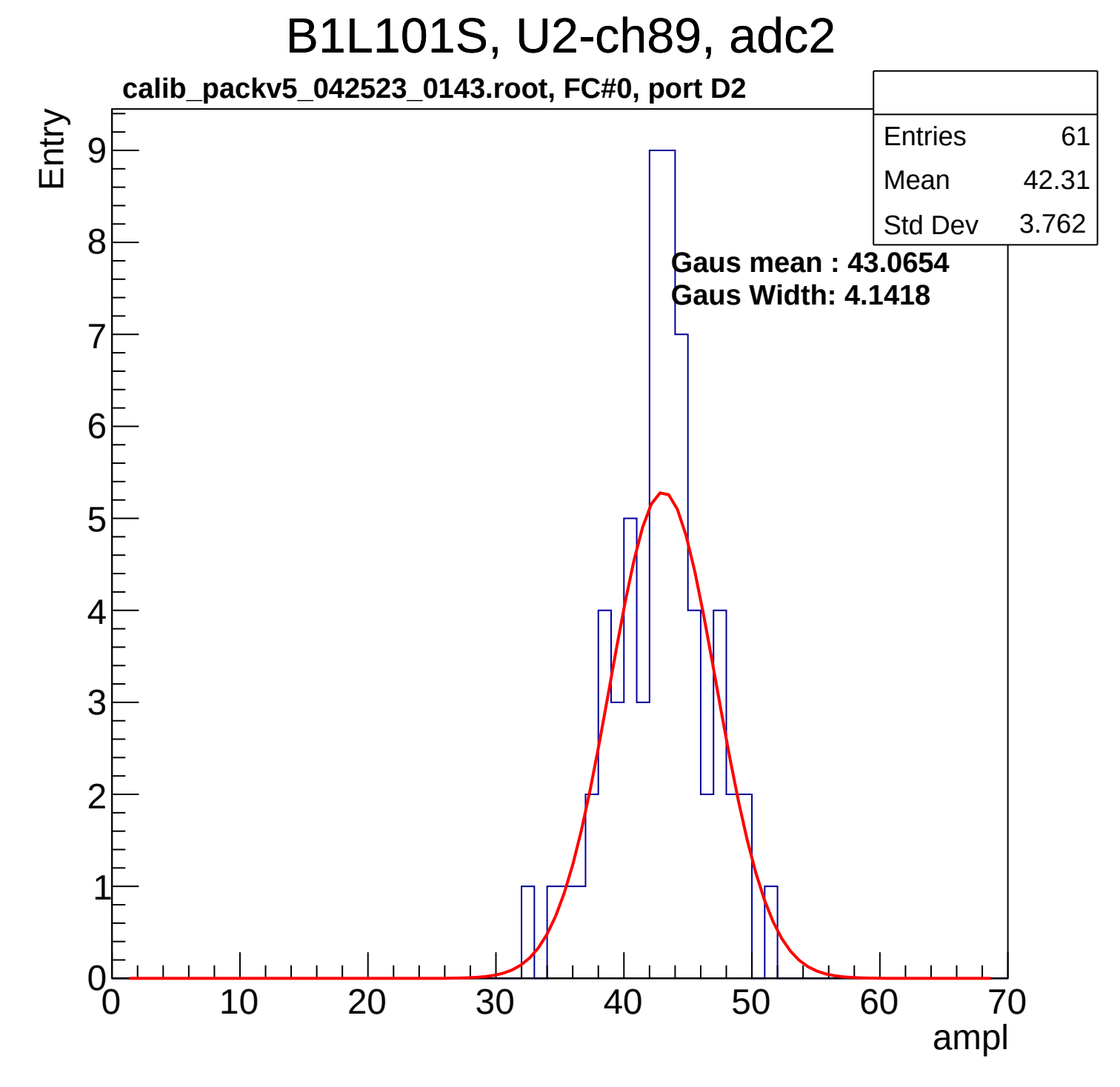

B1L101S, U2-ch88, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 57.14
Std Dev 9.38
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

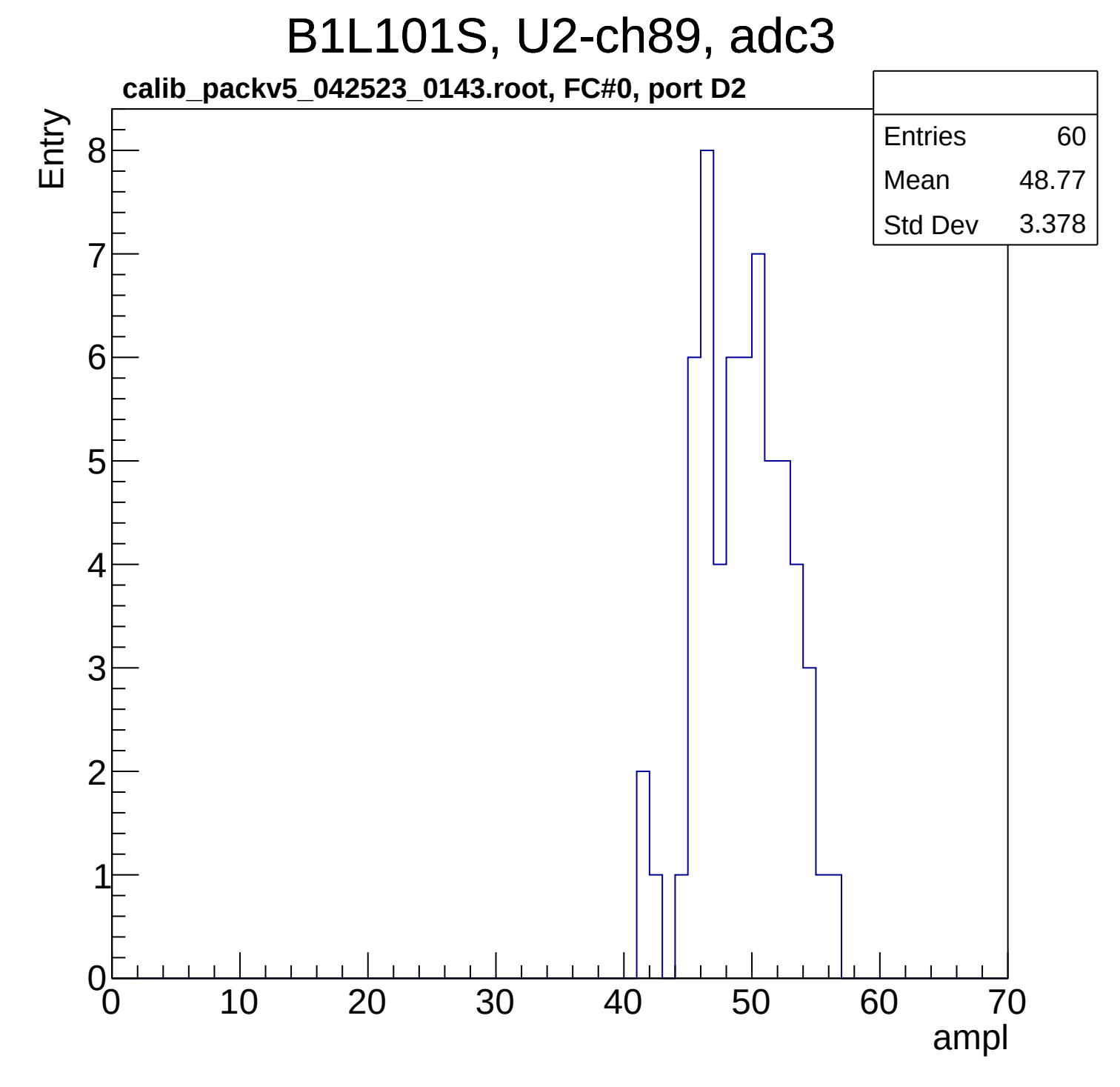

B1L101S, U2-ch88, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 18
Mean 60.94
Std Dev 1.747
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

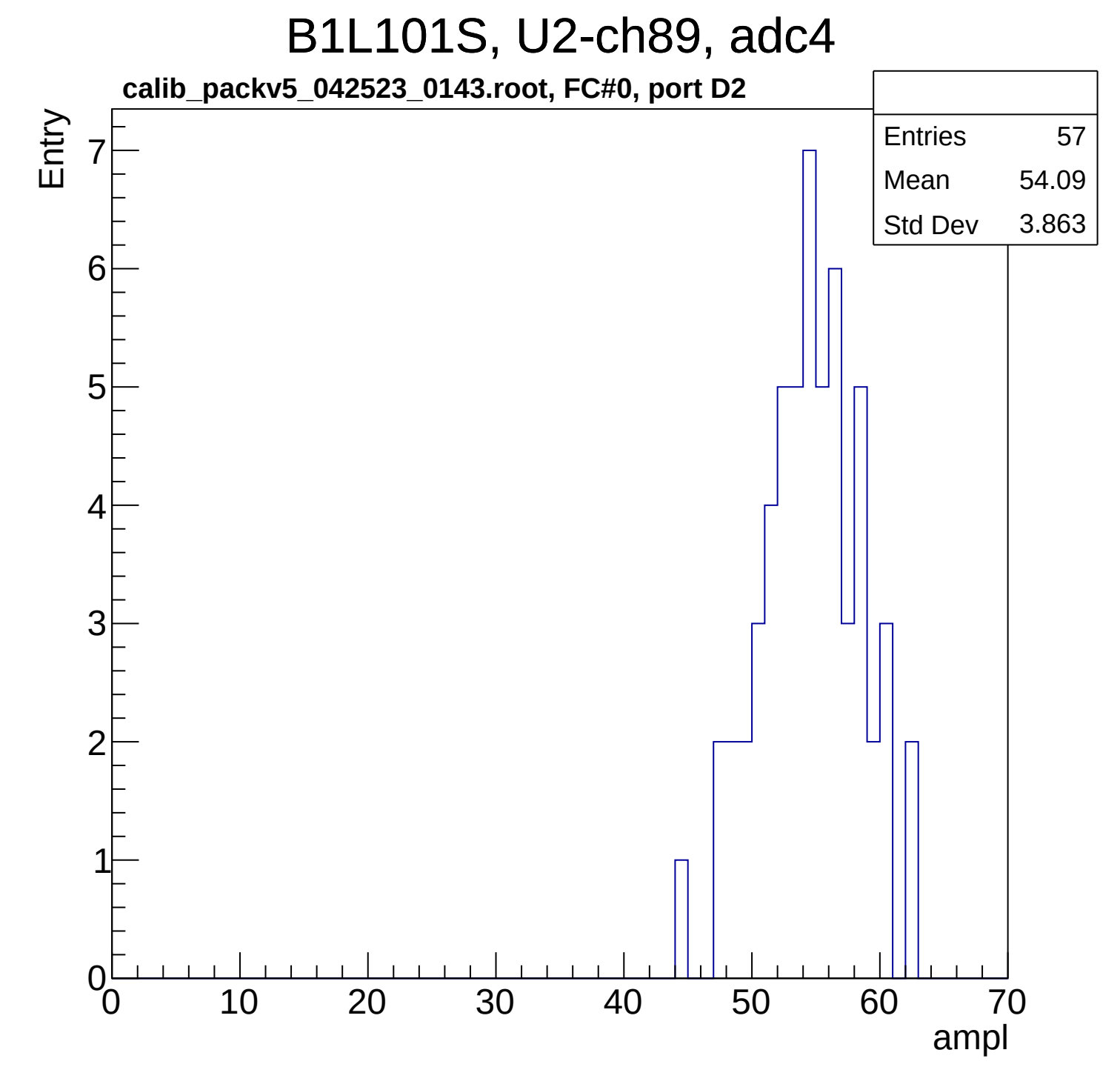

B1L101S, U2-ch88, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

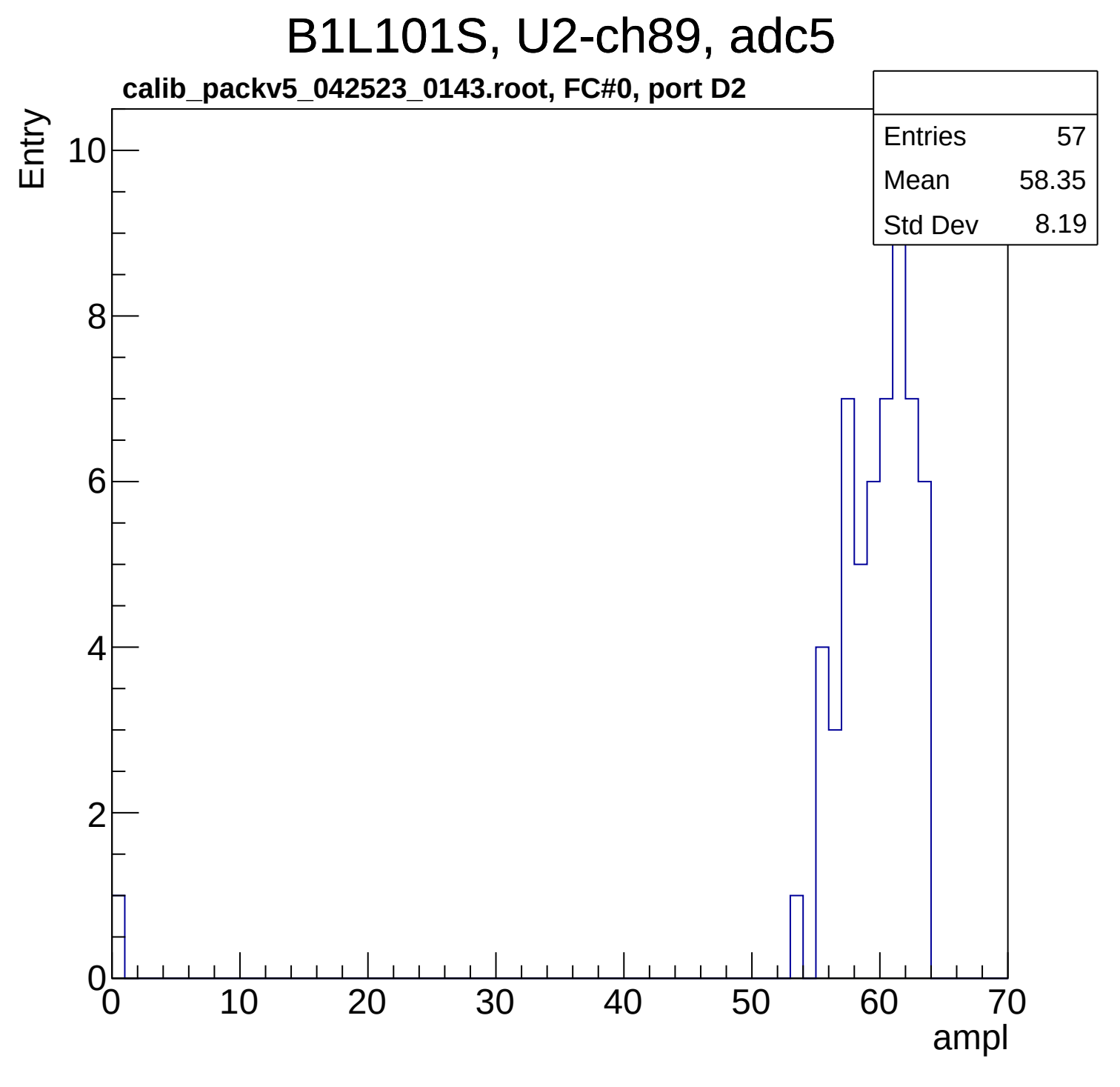

B1L101S, U2-ch89, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 28.71
Std Dev 5.301
Gaus mean : 30.1318
Gaus Width: 3.0266
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

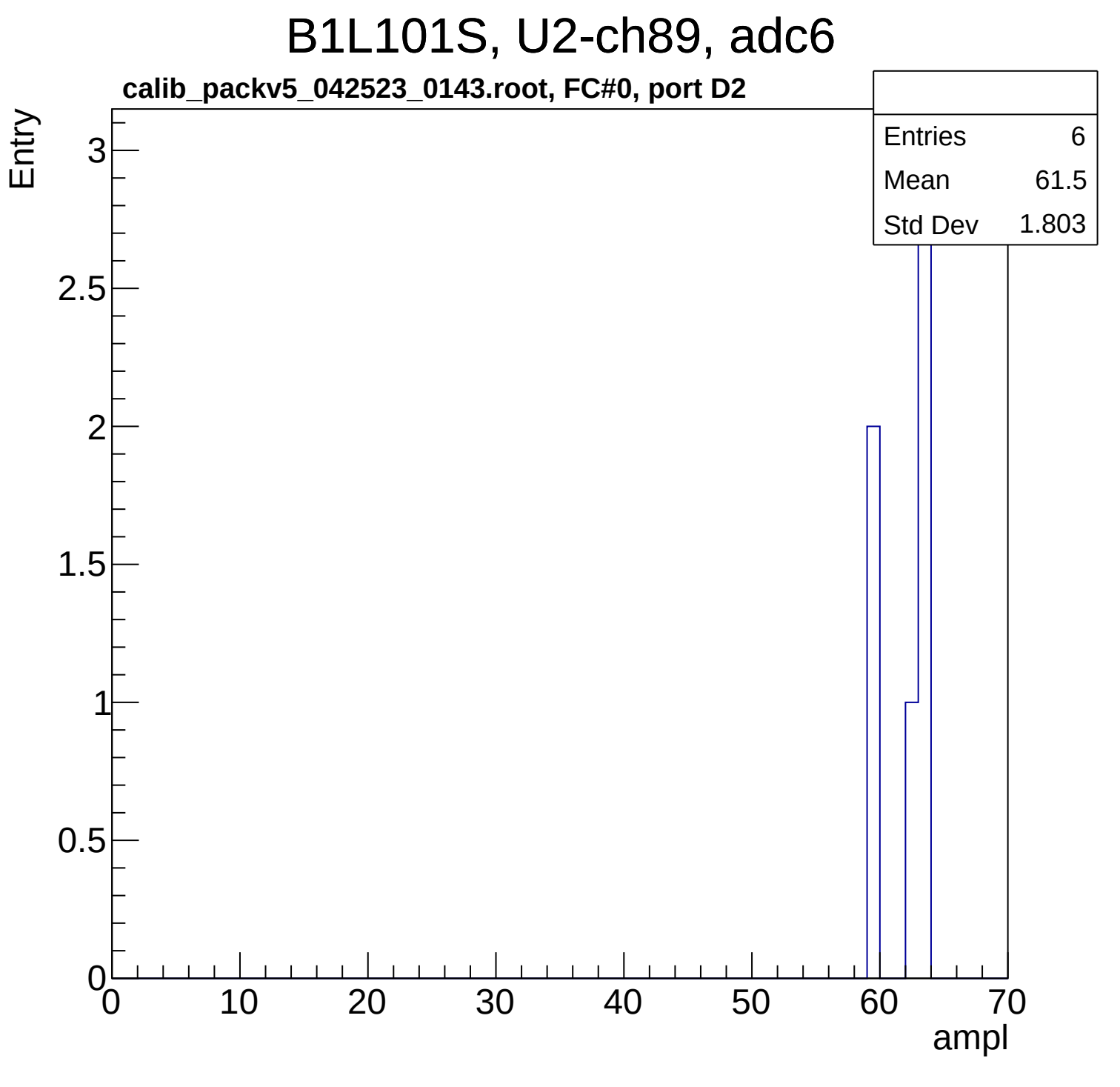

B1L101S, U2-ch89, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 35.54
Std Dev 3.895
Gaus mean : 36.2390
Gaus Width: 4.2801
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

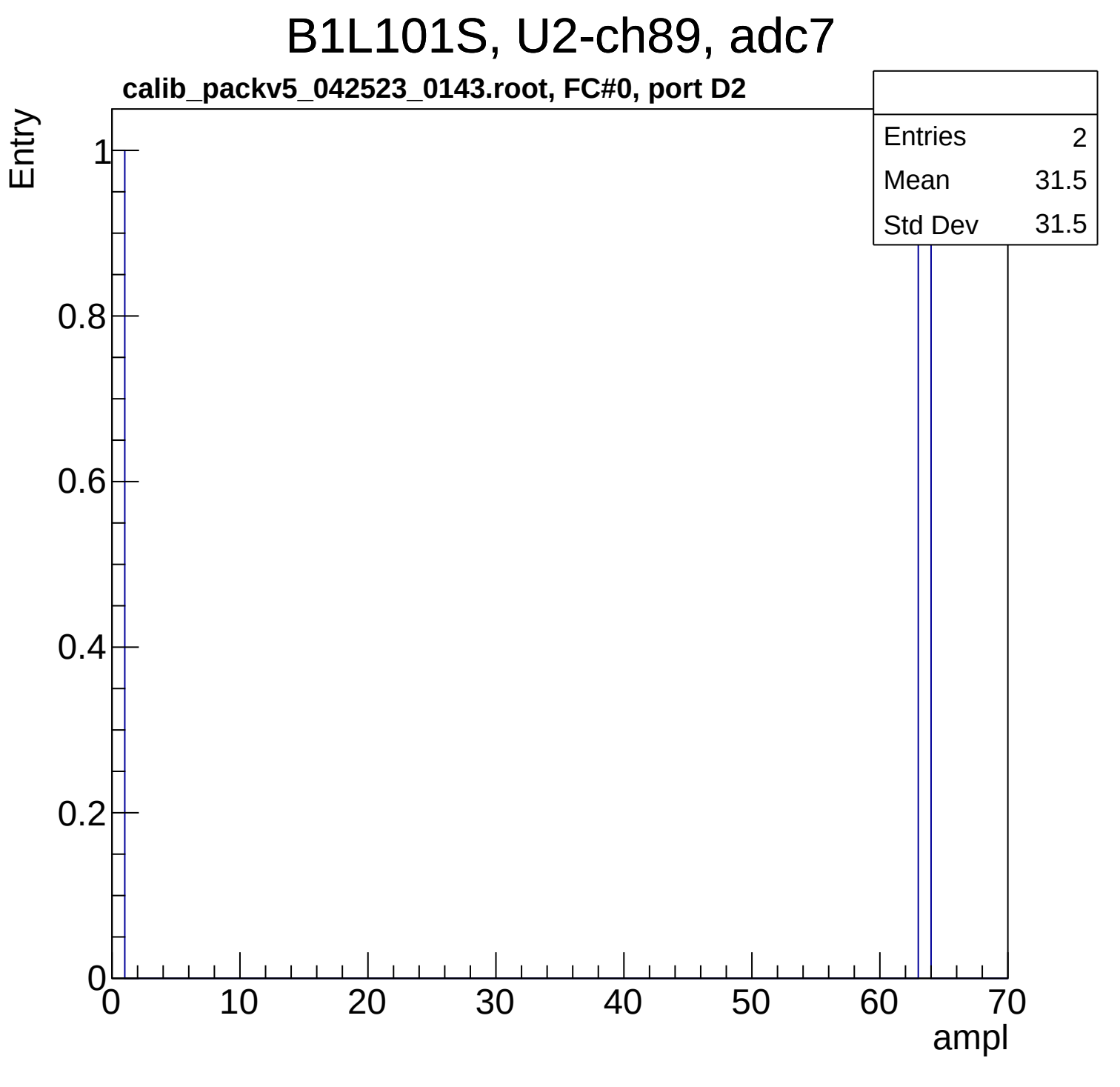

B1L101S, U2-ch89, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 42.31
Std Dev 3.762
Gaus mean : 43.0654
Gaus Width: 4.1418
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

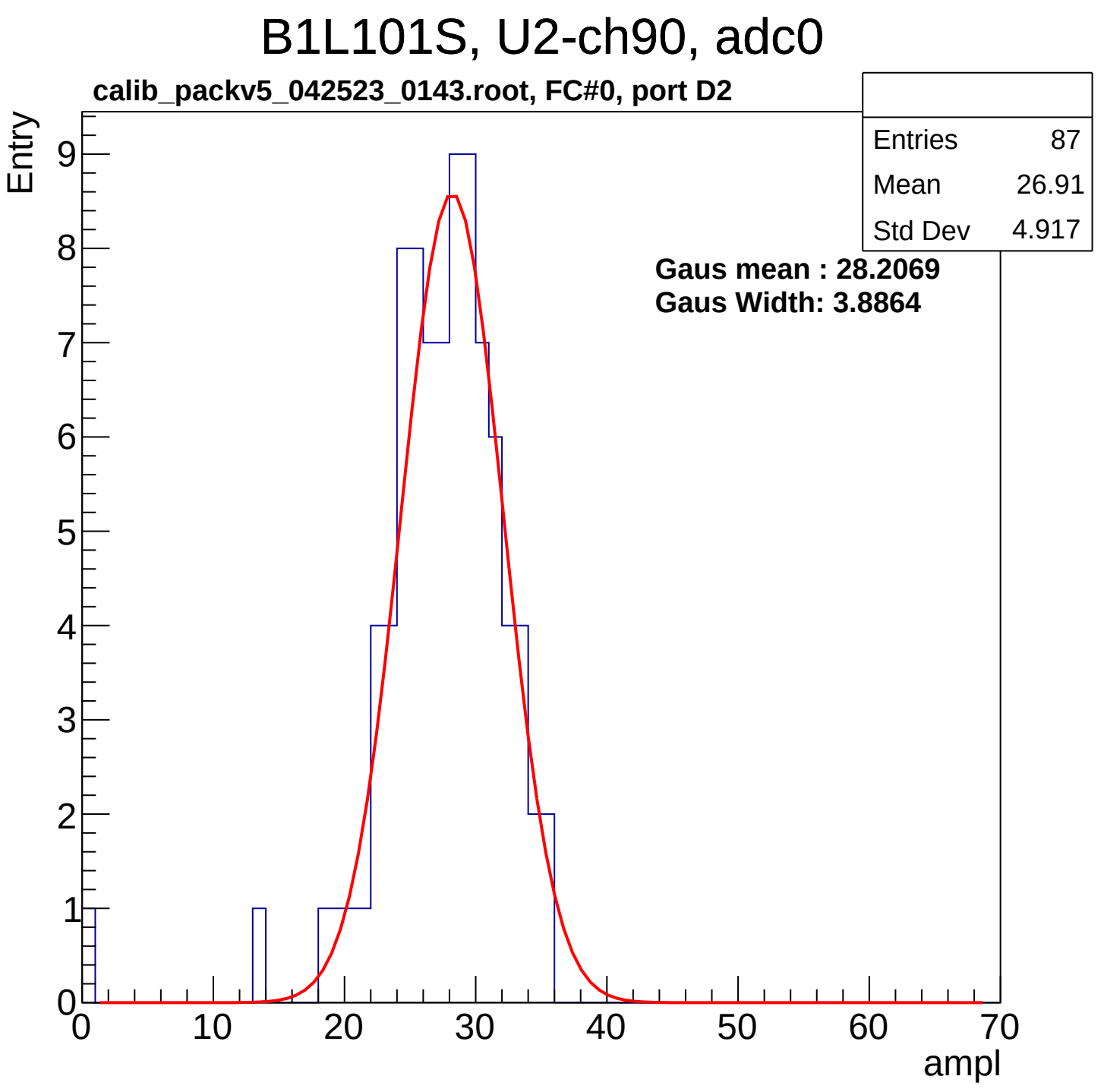

B1L101S, U2-ch89, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 48.77
Std Dev 3.378
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

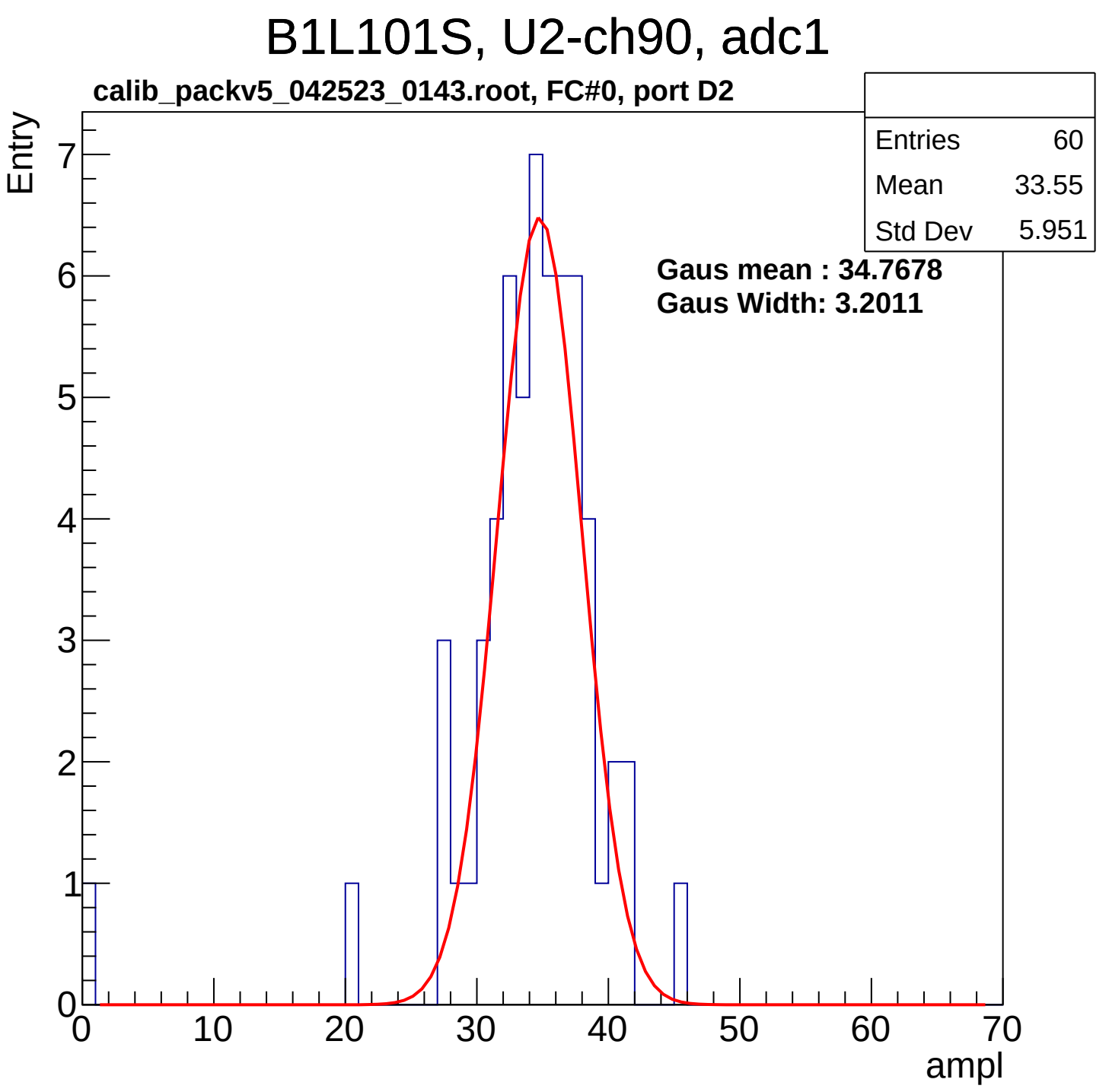

B1L101S, U2-ch89, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 54.09
Std Dev 3.863
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

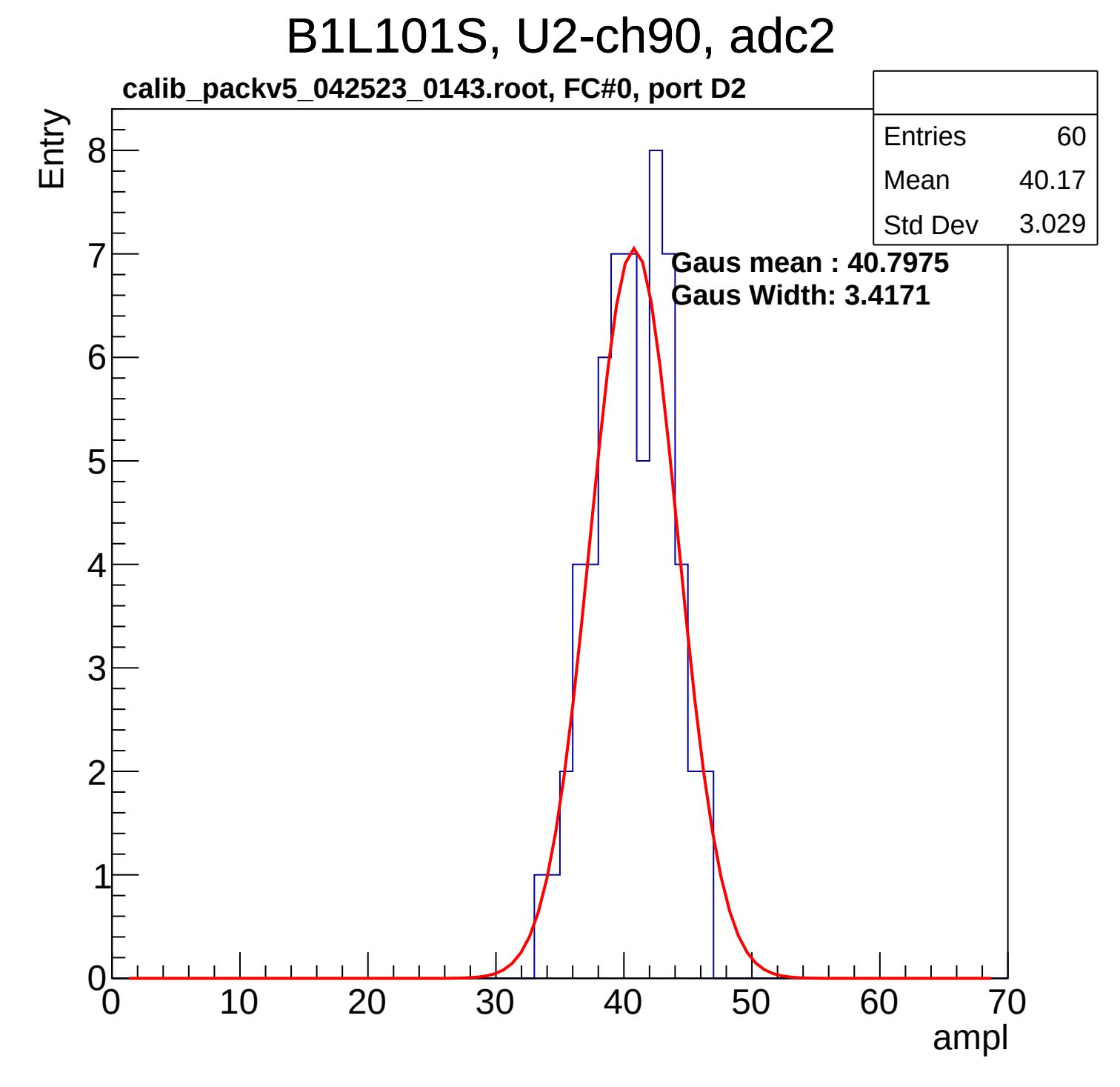

B1L101S, U2-ch89, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 58.35
Std Dev 8.19
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

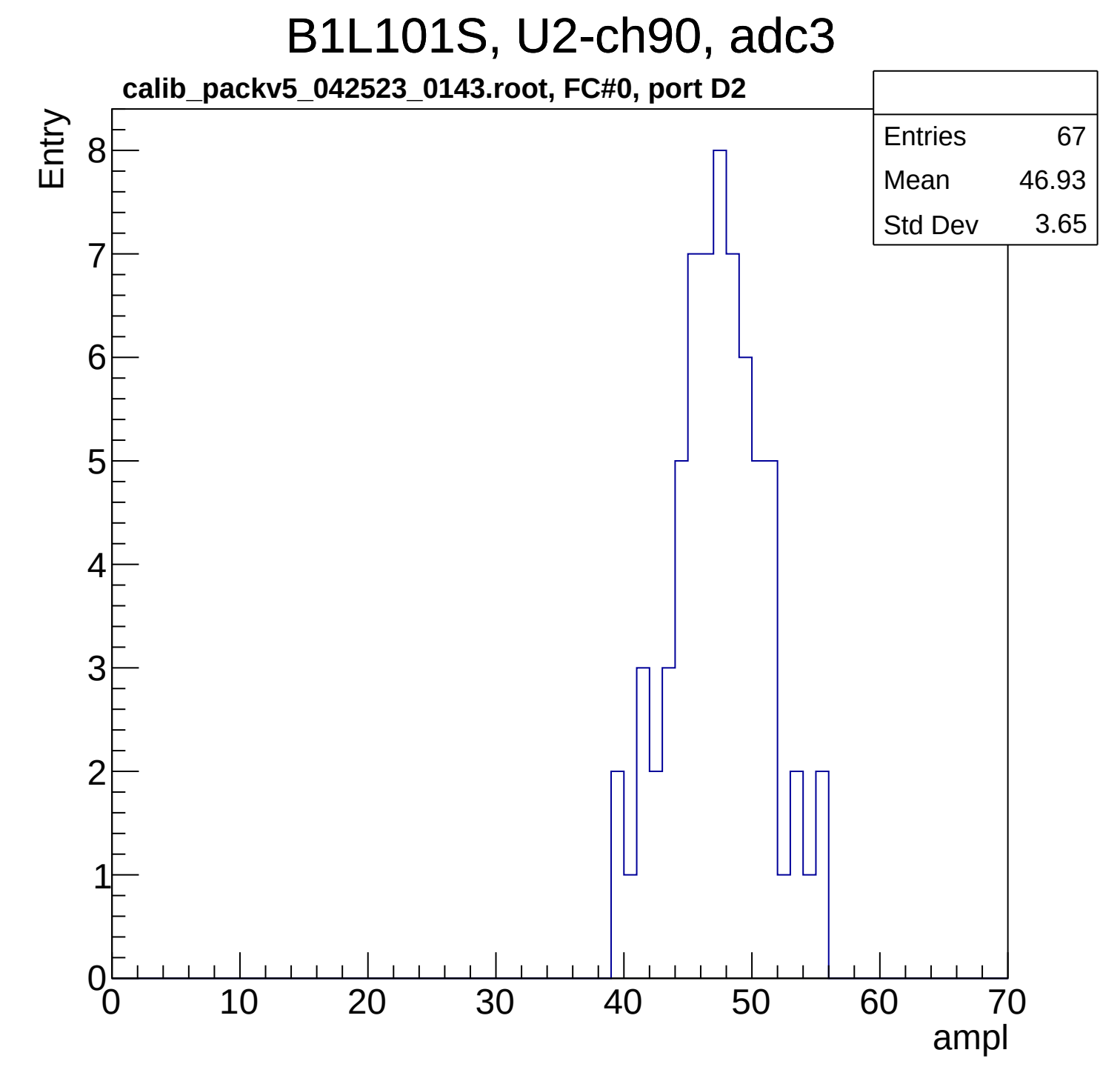

B1L101S, U2-ch89, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 61.5
Std Dev 1.803
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

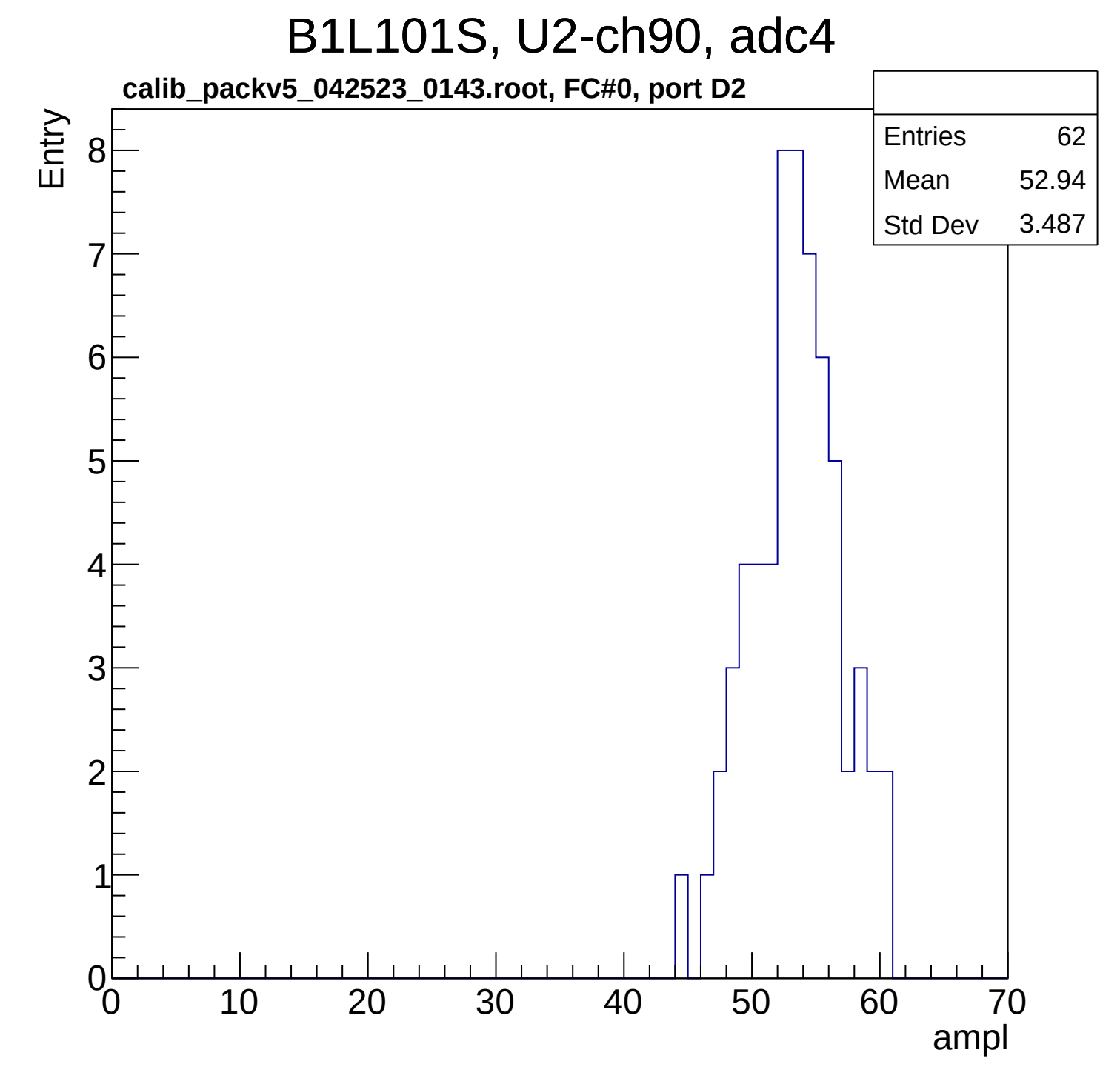

B1L101S, U2-ch89, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

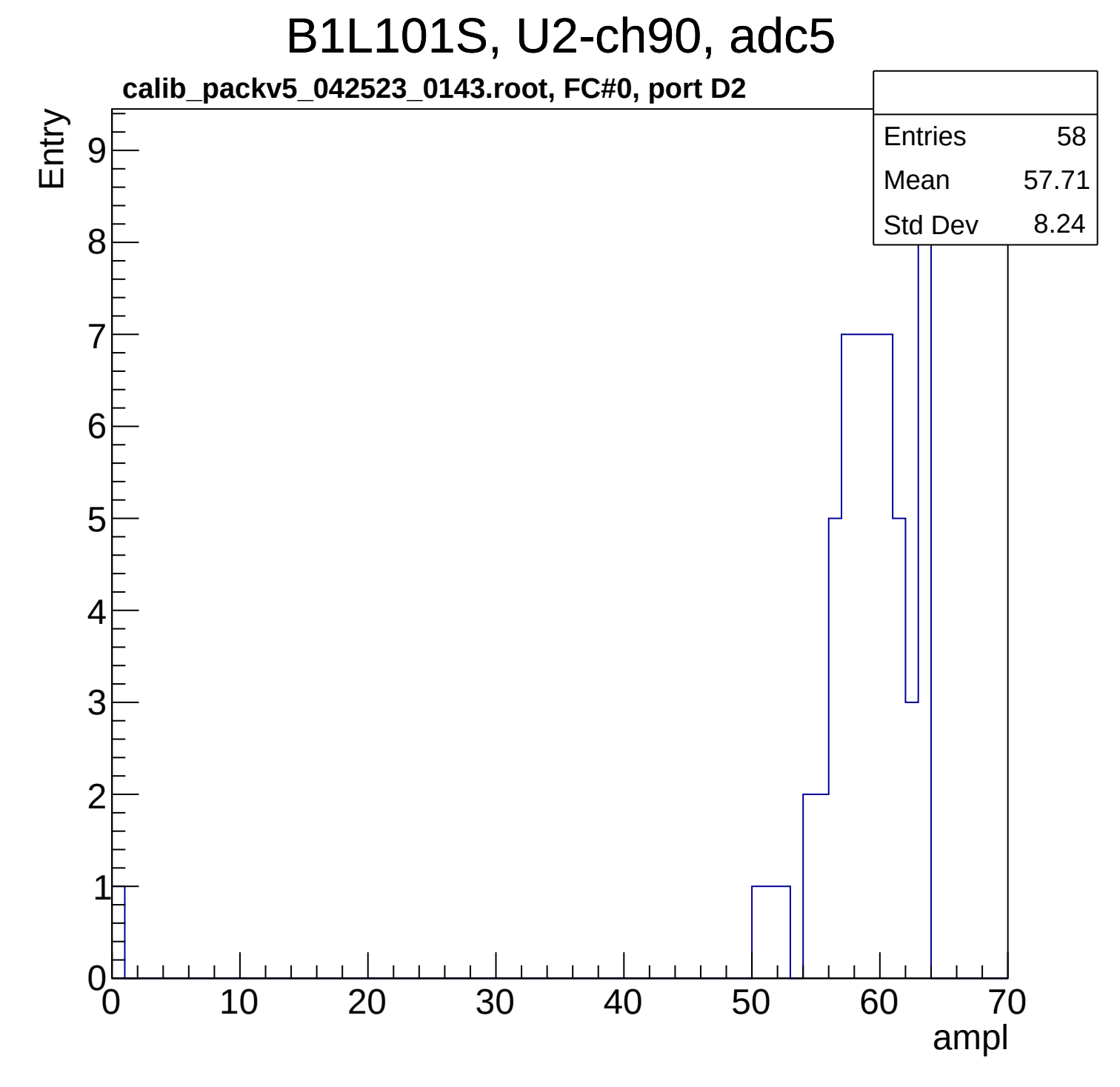

B1L101S, U2-ch90, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 87
Mean 26.91
Std Dev 4.917
Gaus mean : 28.2069
Gaus Width: 3.8864
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

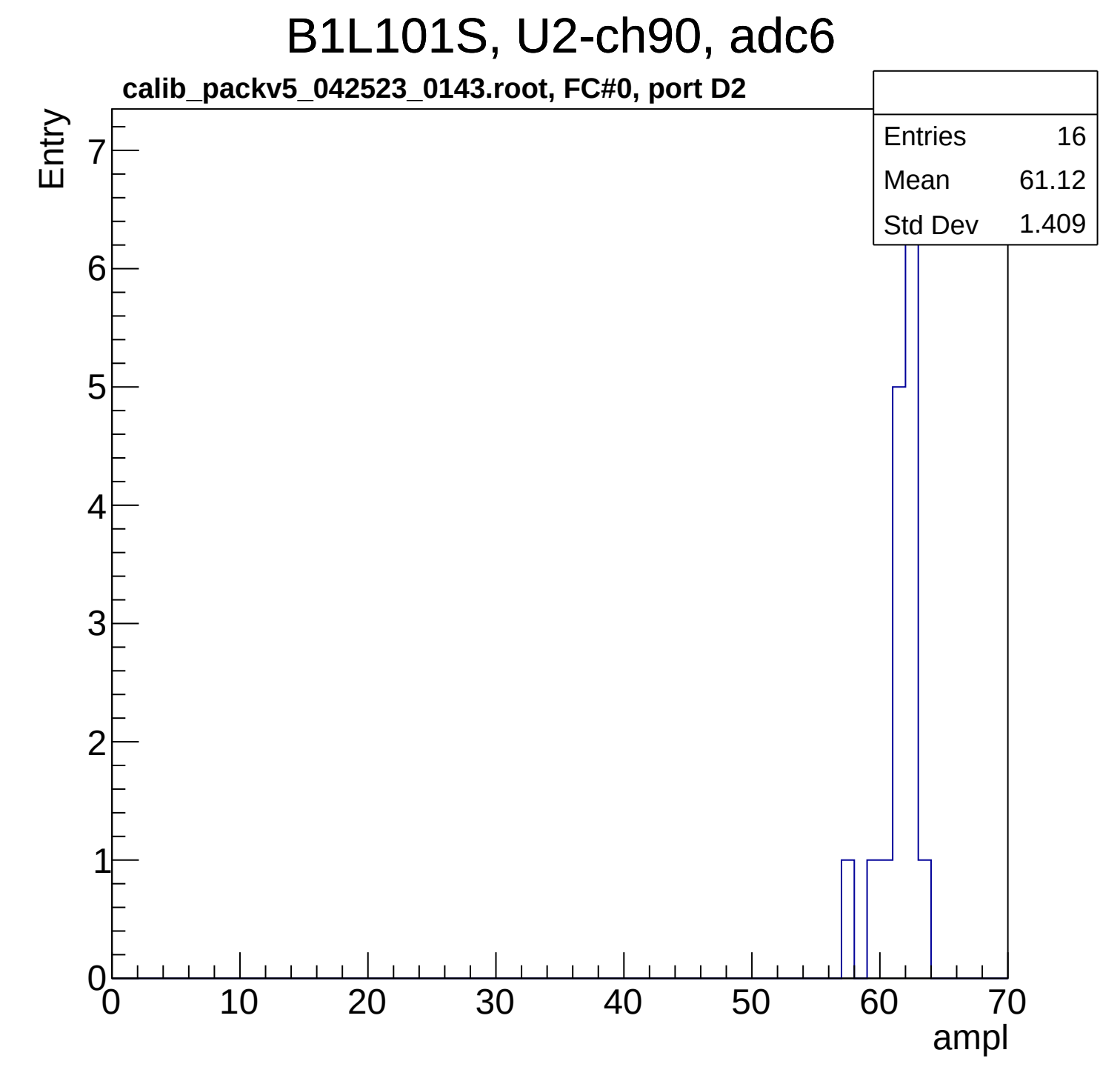

B1L101S, U2-ch90, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 33.55
Std Dev 5.951
Gaus mean : 34.7678
Gaus Width: 3.2011
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

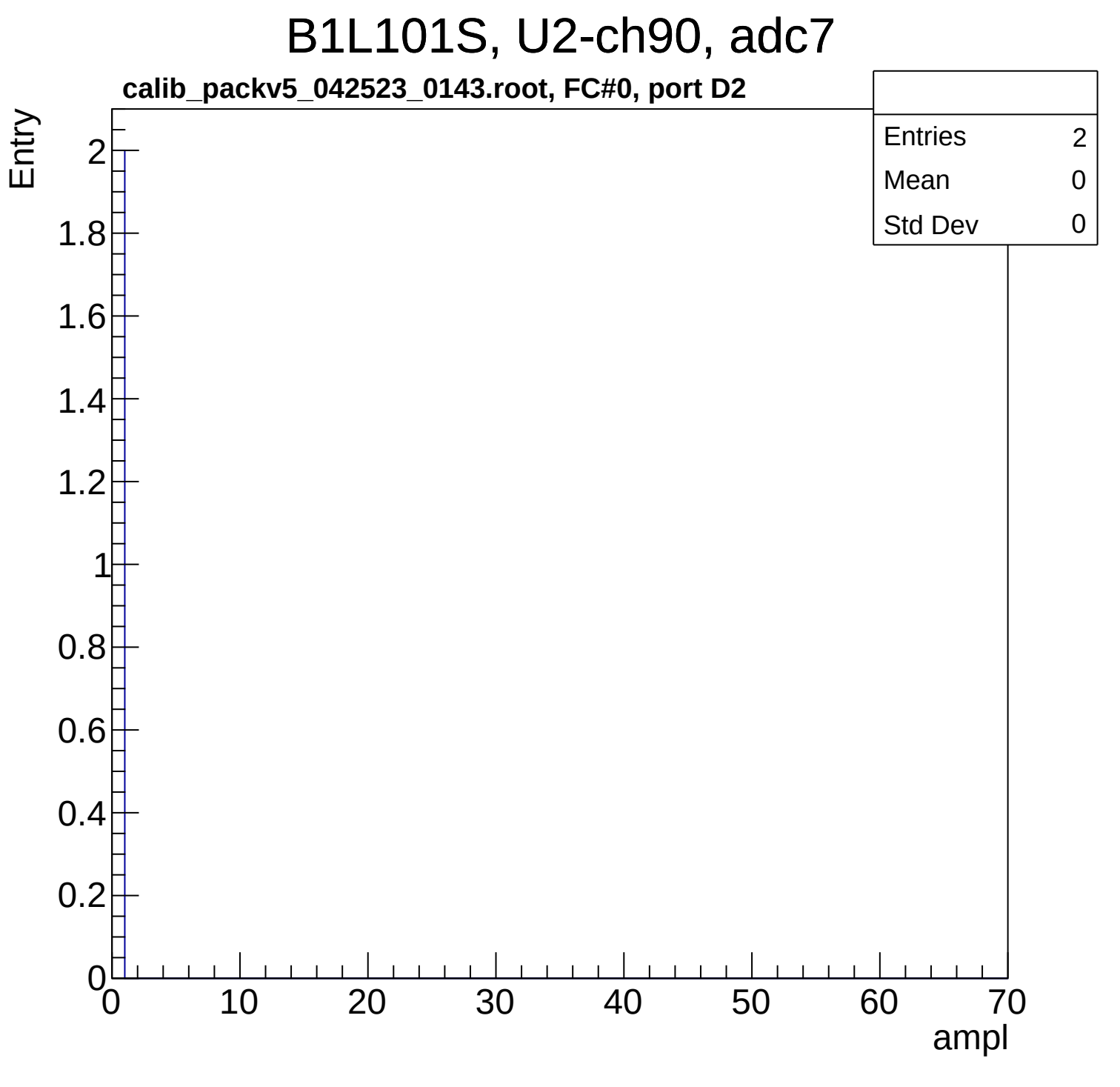

B1L101S, U2-ch90, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 40.17
Std Dev 3.029
Gaus mean : 40.7975
Gaus Width: 3.4171
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

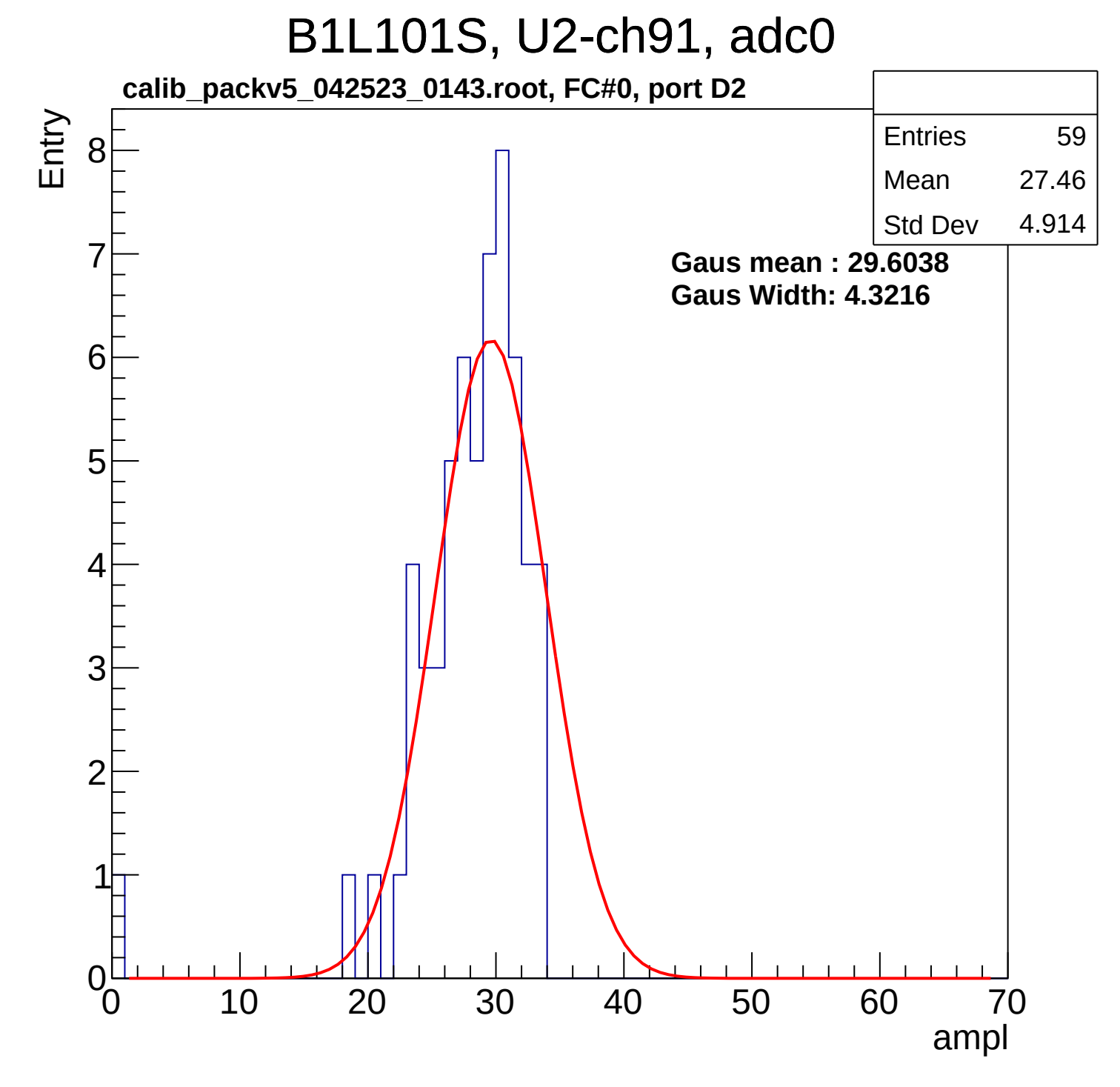

B1L101S, U2-ch90, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 46.93
Std Dev 3.65
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

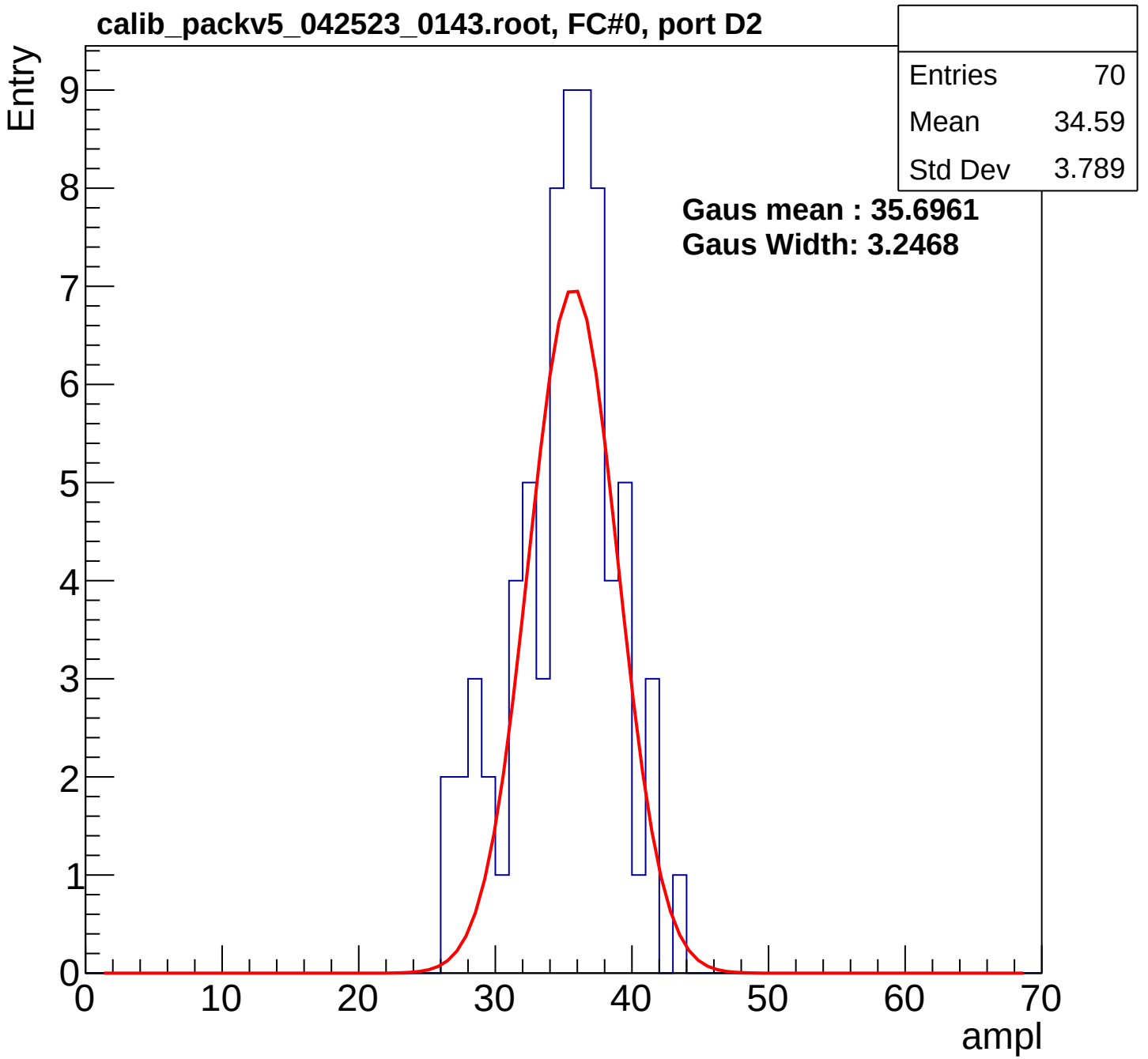

B1L101S, U2-ch90, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 52.94
Std Dev 3.487
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

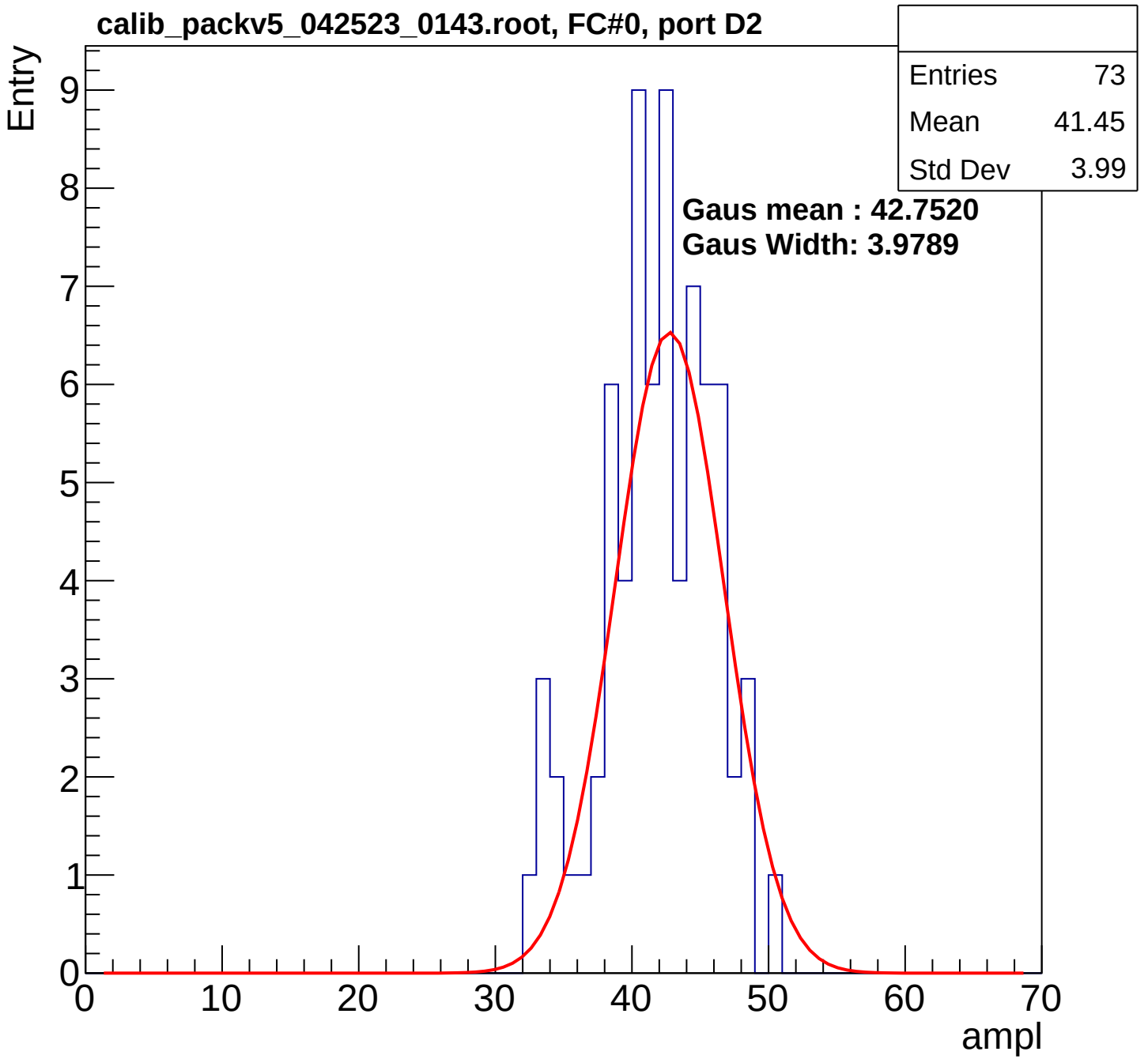

B1L101S, U2-ch90, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 57.71
Std Dev 8.24
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

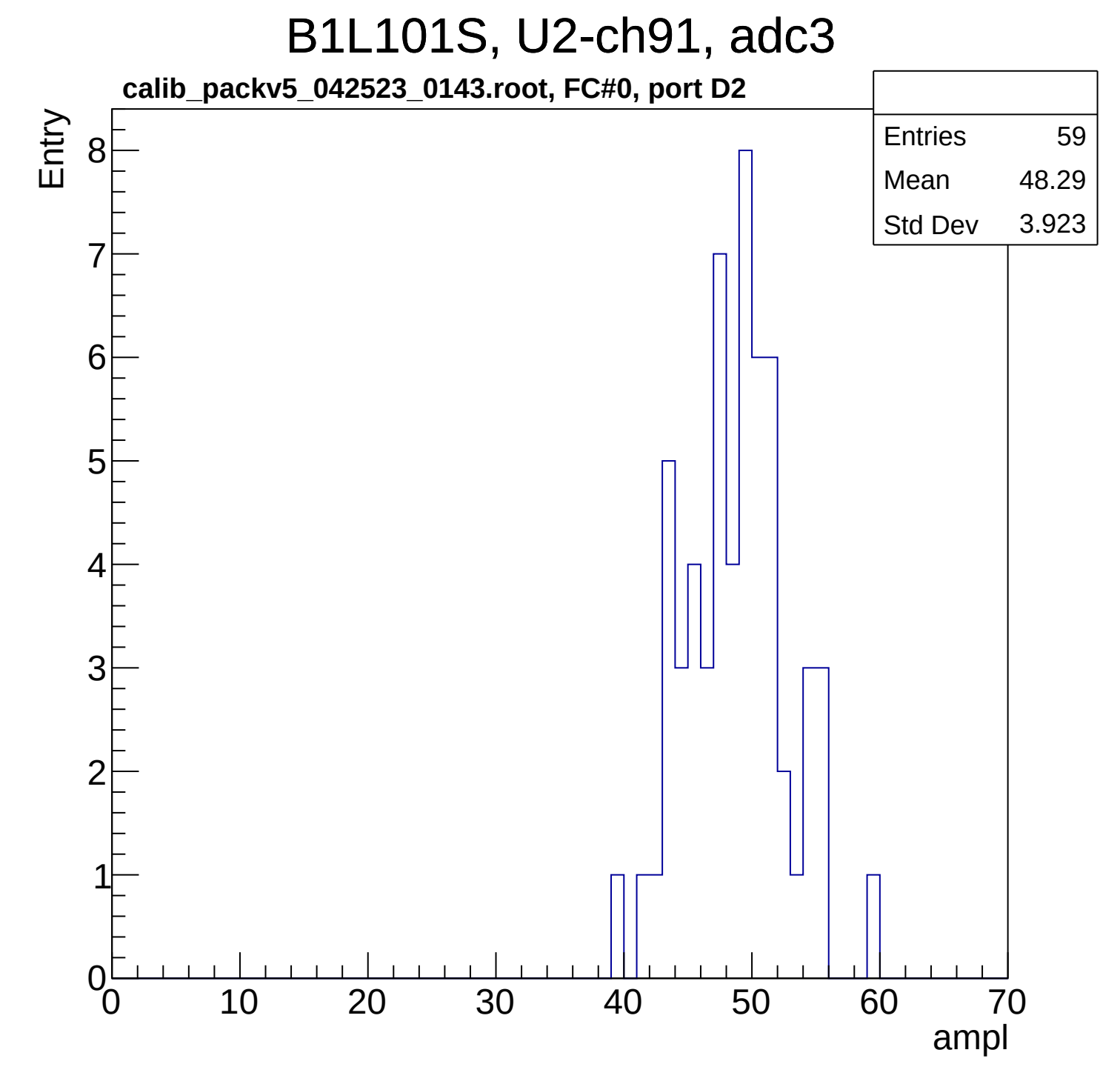

B1L101S, U2-ch90, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 16
Mean 61.12
Std Dev 1.409
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

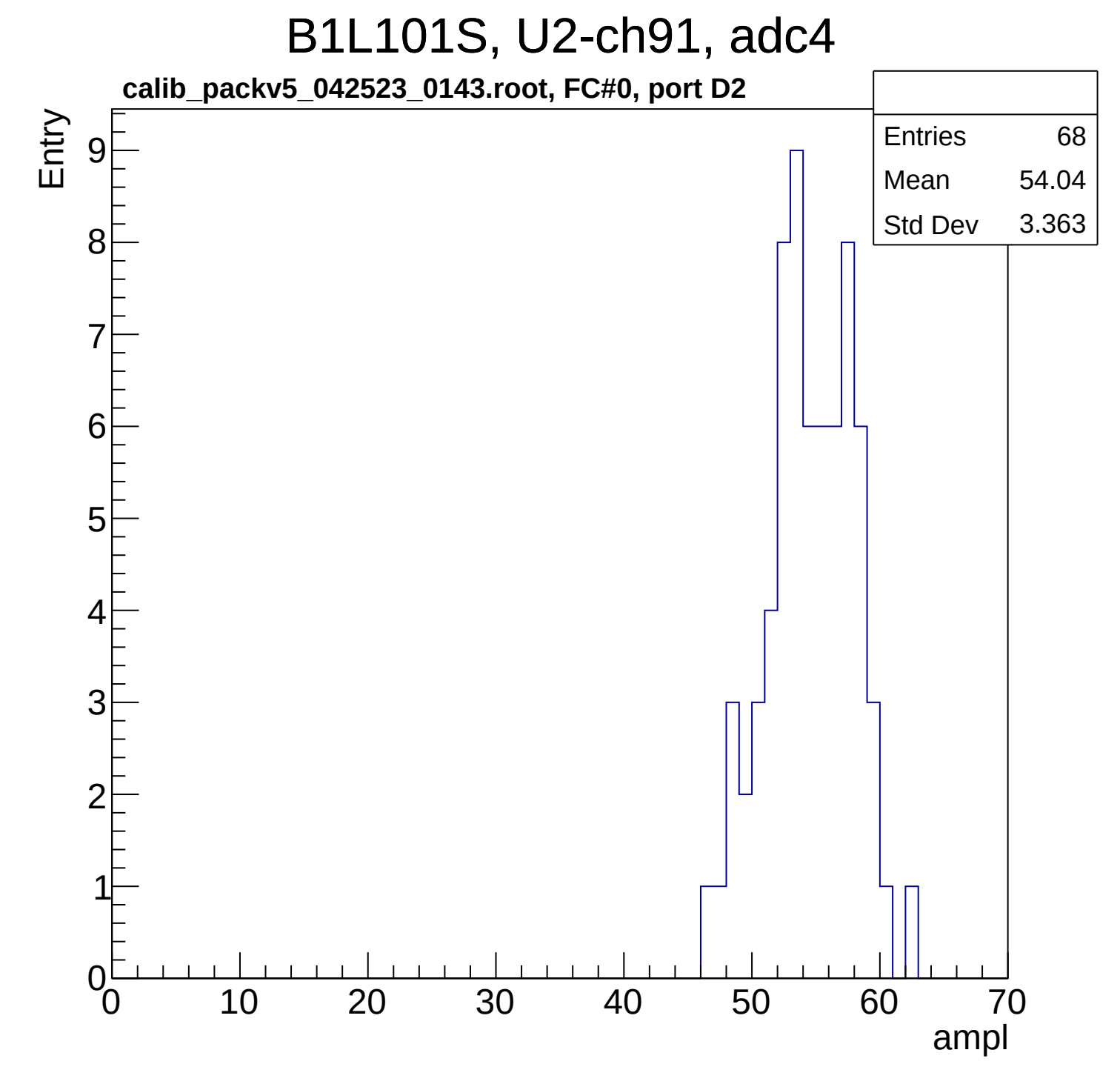

B1L101S, U2-ch90, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

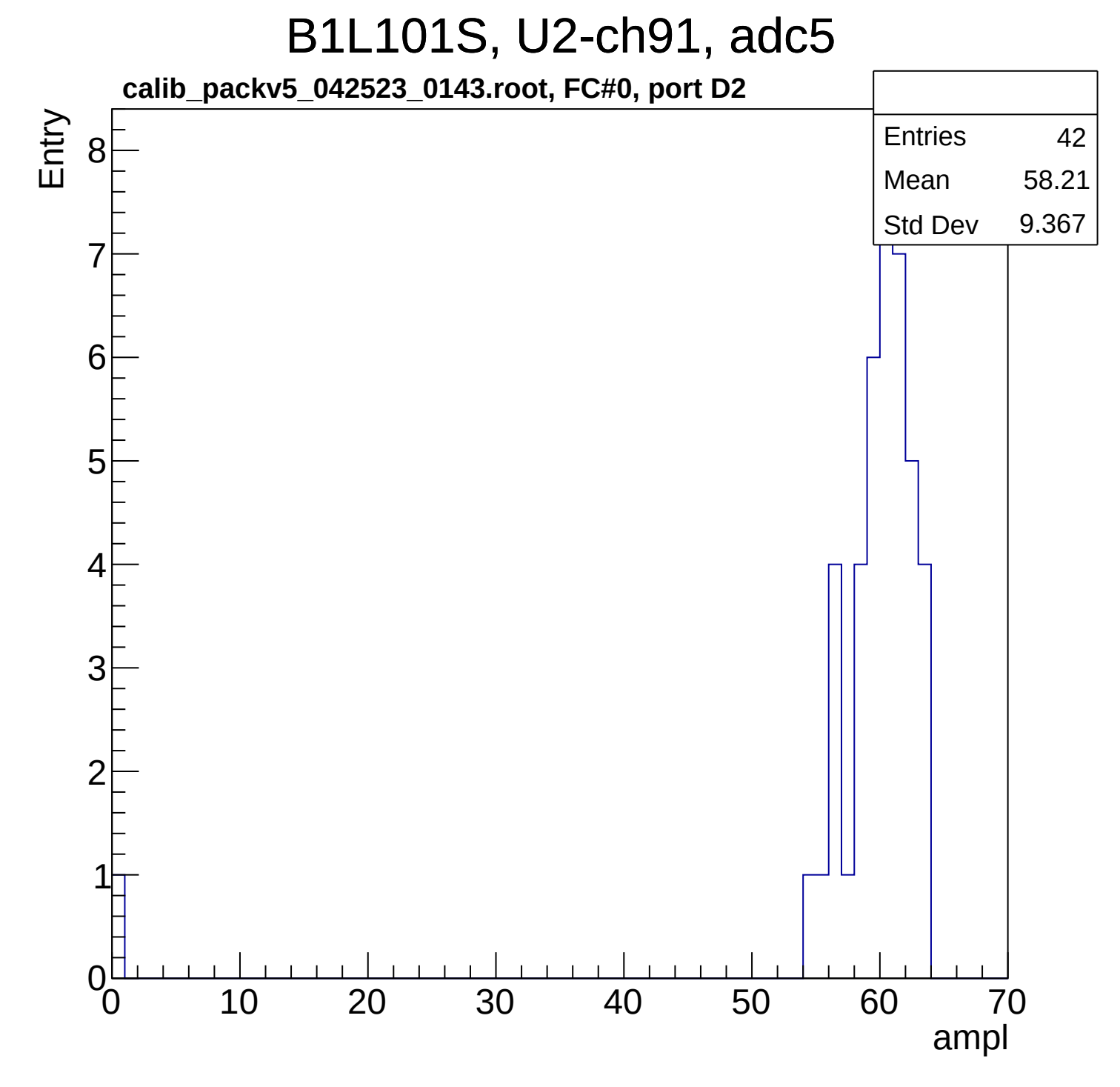

B1L101S, U2-ch91, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 27.46
Std Dev 4.914
Gaus mean : 29.6038
Gaus Width: 4.3216
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

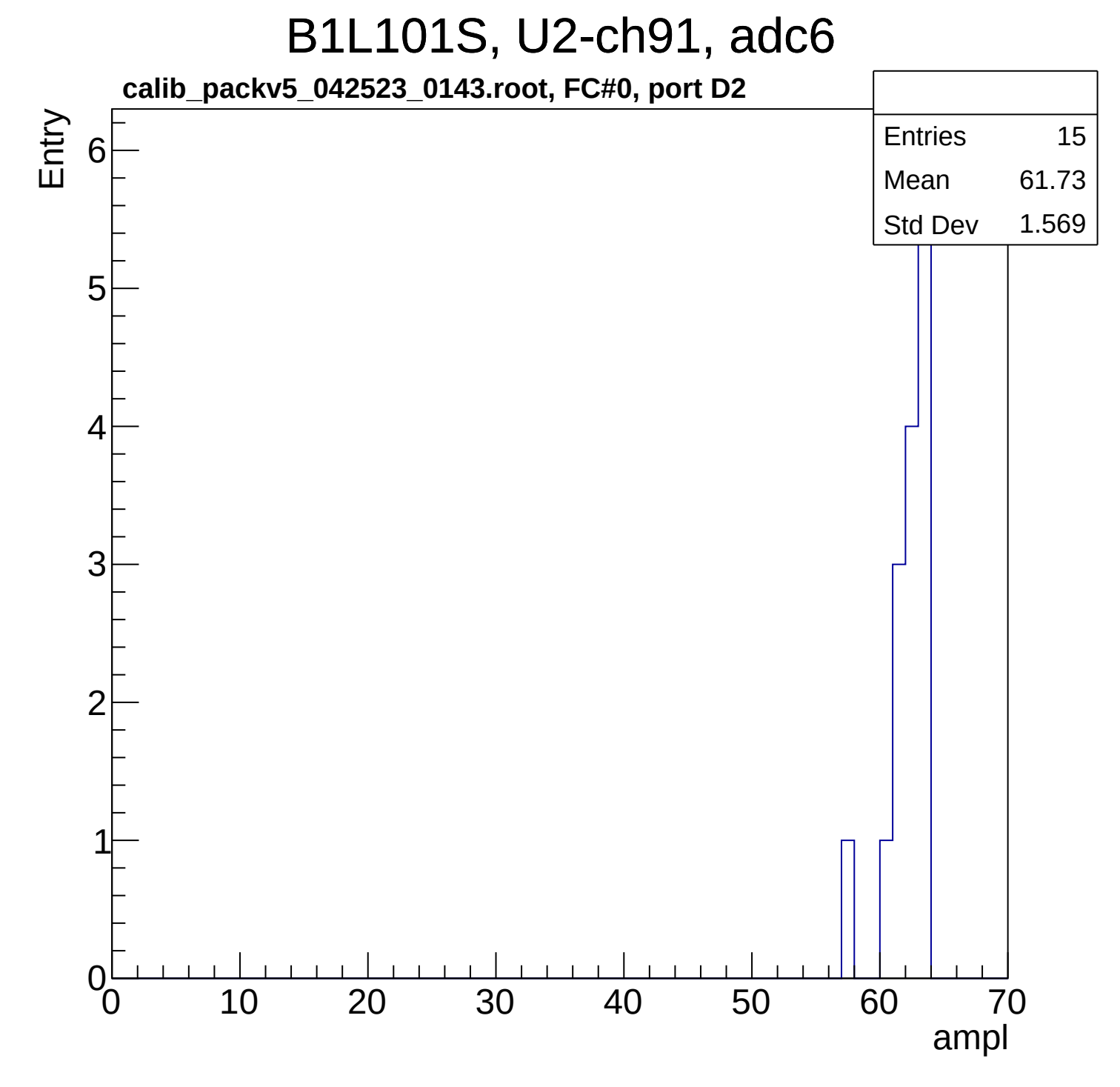

B1L101S, U2-ch91, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 34.59
Std Dev 3.789
Gaus mean : 35.6961
Gaus Width: 3.2468
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

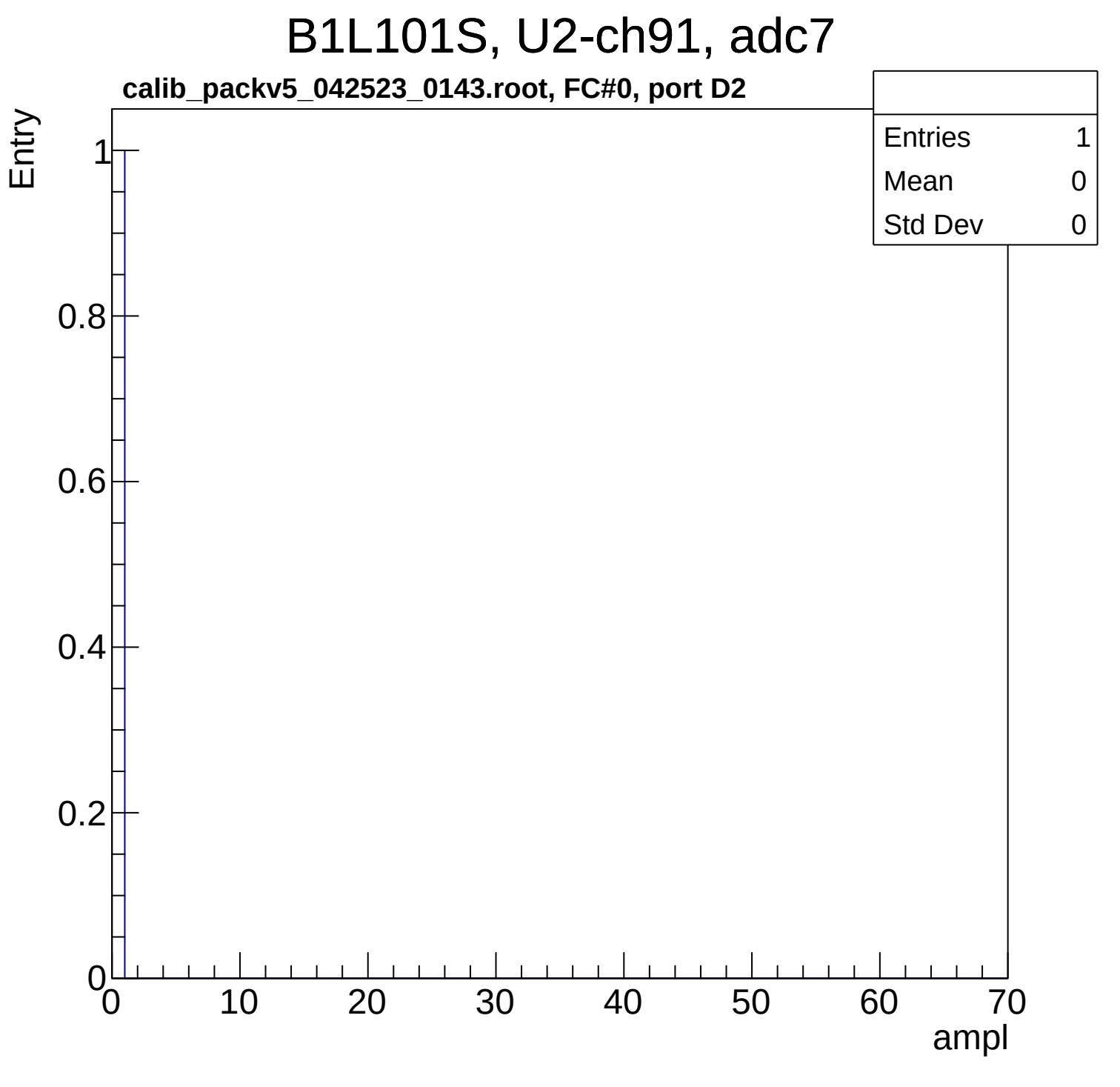

B1L101S, U2-ch91, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 41.45
Std Dev 3.99
Gaus mean : 42.7520
Gaus Width: 3.9789
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

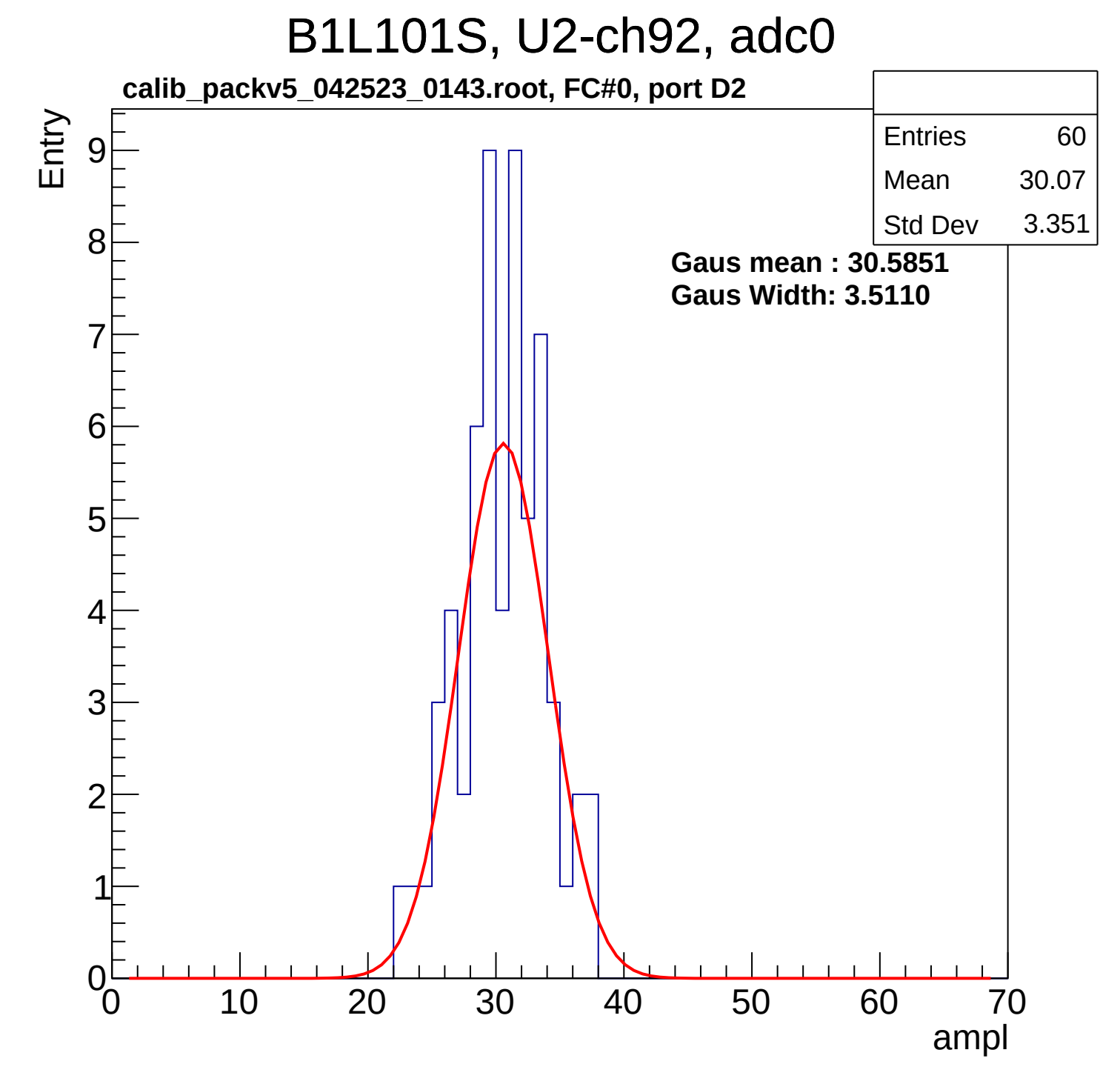

B1L101S, U2-ch91, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 48.29
Std Dev 3.923
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

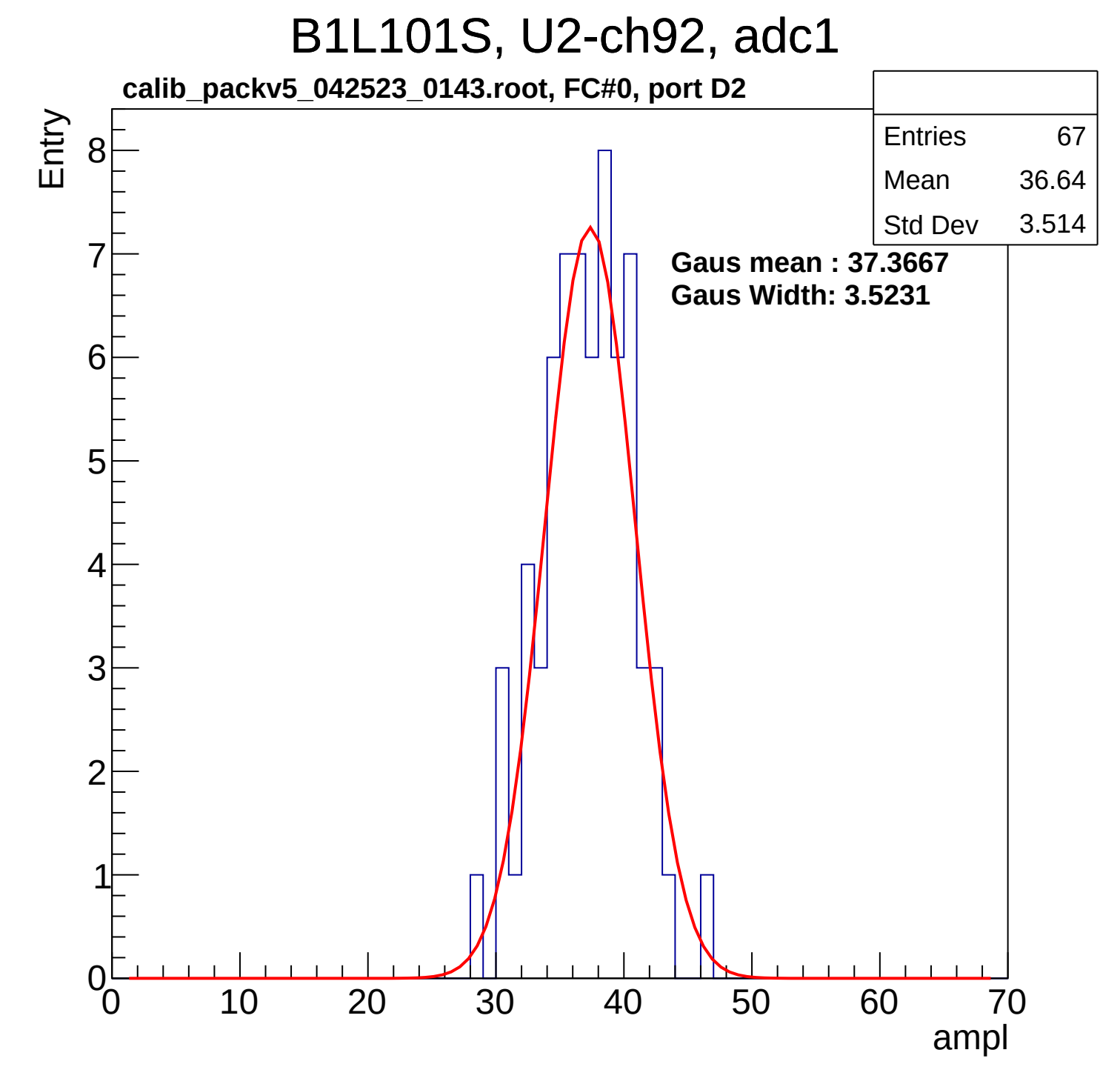

B1L101S, U2-ch91, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 54.04
Std Dev 3.363
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

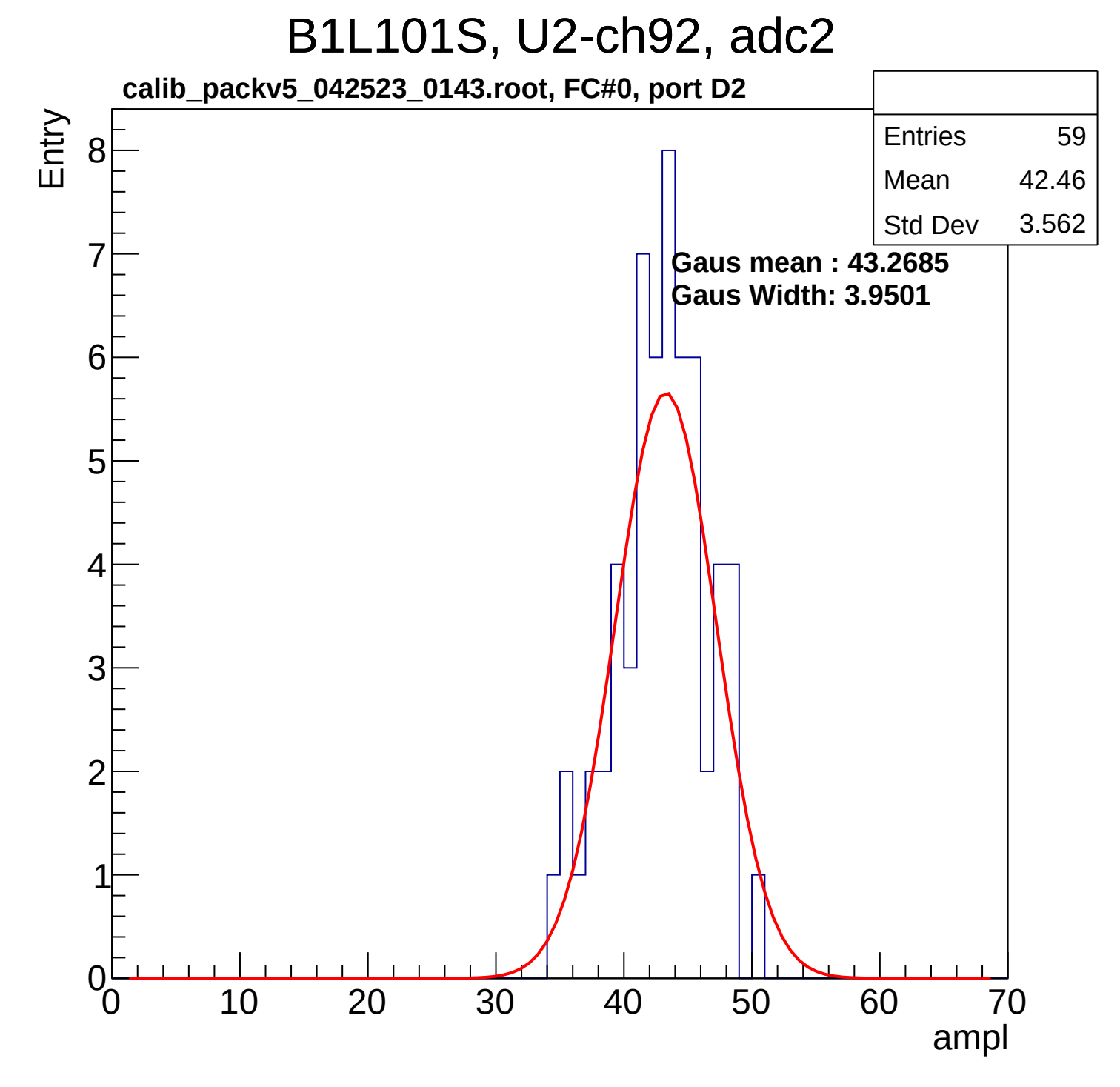

B1L101S, U2-ch91, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 58.21
Std Dev 9.367
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

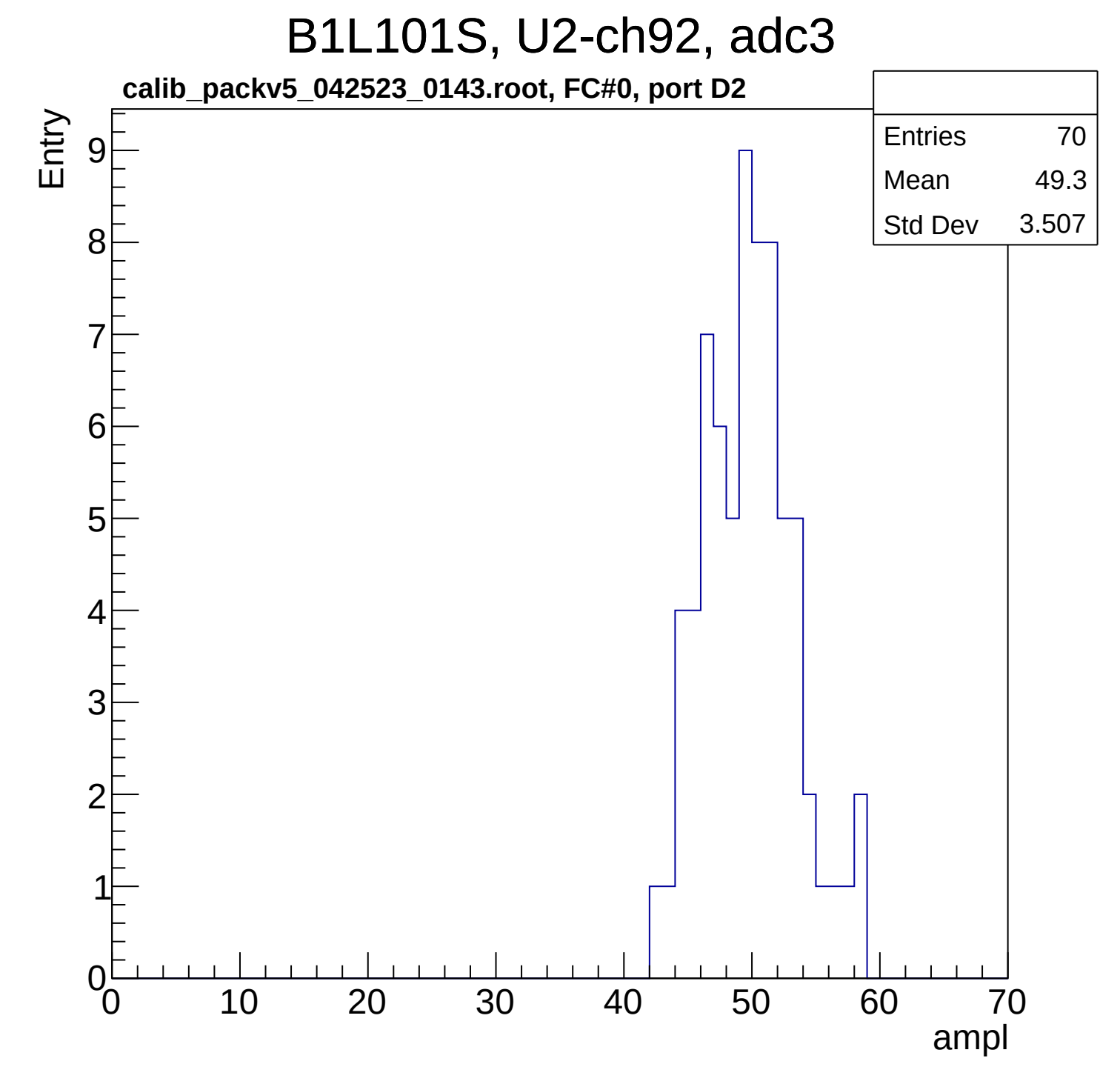

B1L101S, U2-ch91, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 15
Mean 61.73
Std Dev 1.569
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

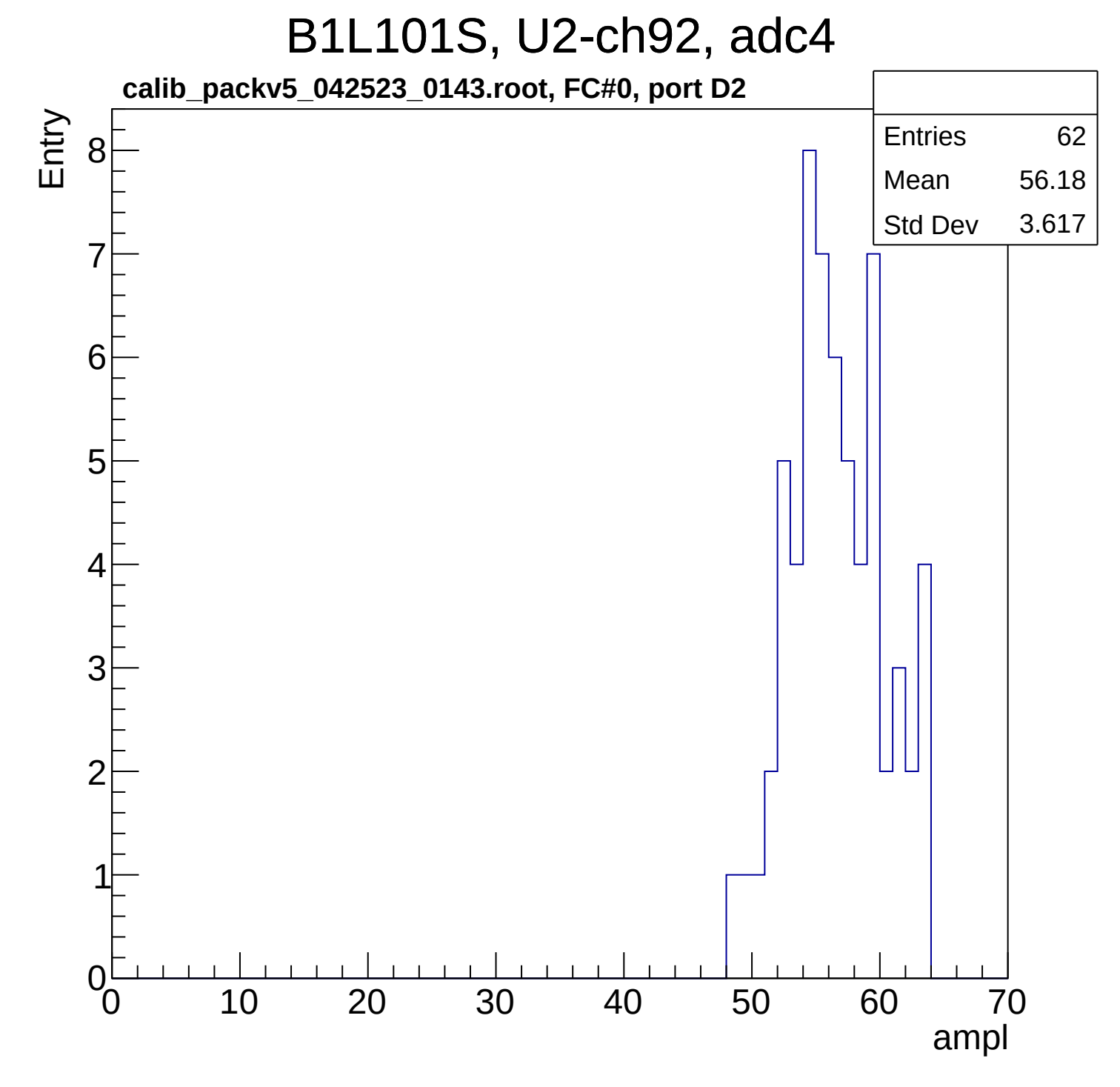

B1L101S, U2-ch91, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

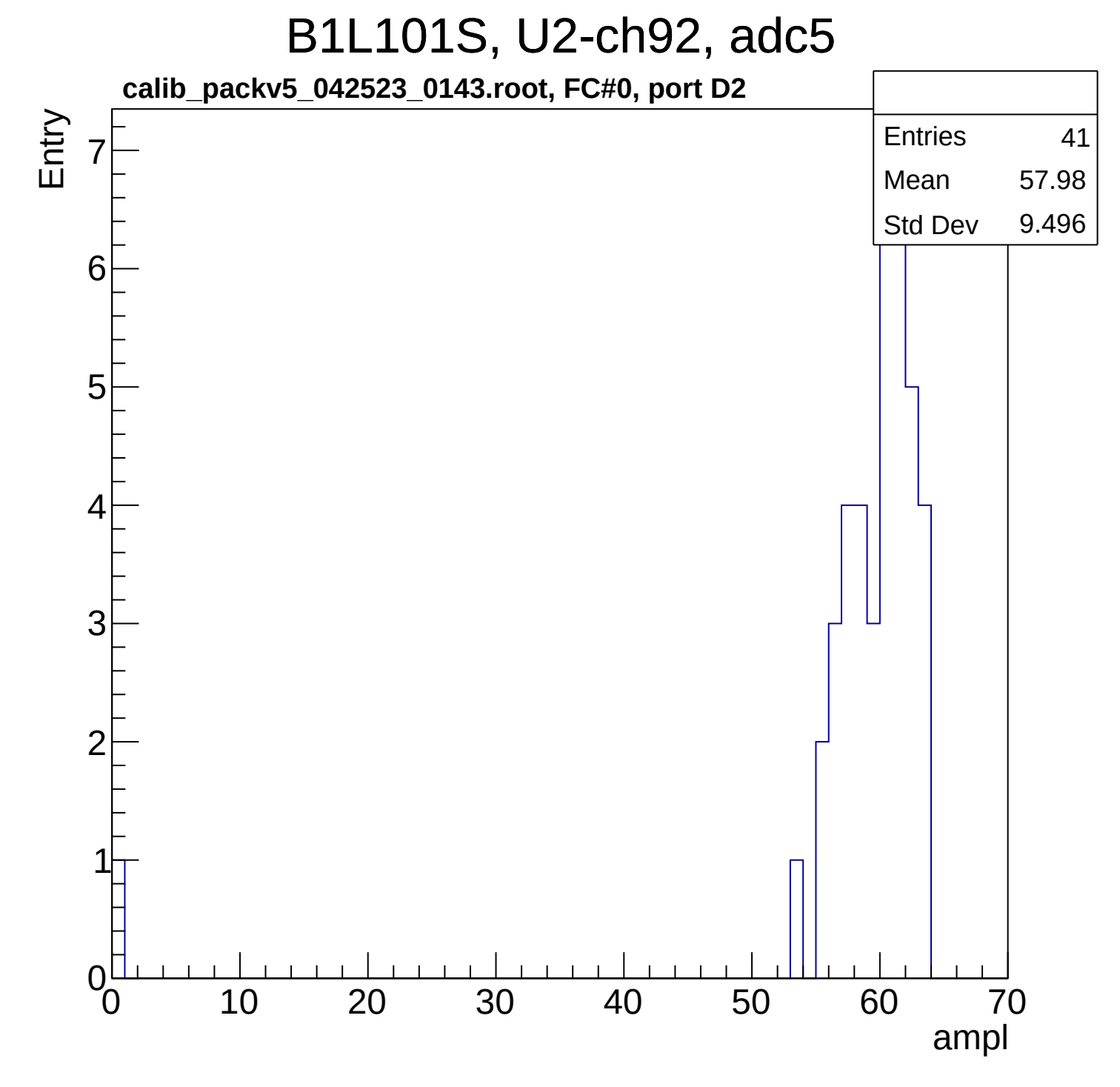

B1L101S, U2-ch92, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 30.07
Std Dev 3.351
Gaus mean : 30.5851
Gaus Width: 3.5110
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

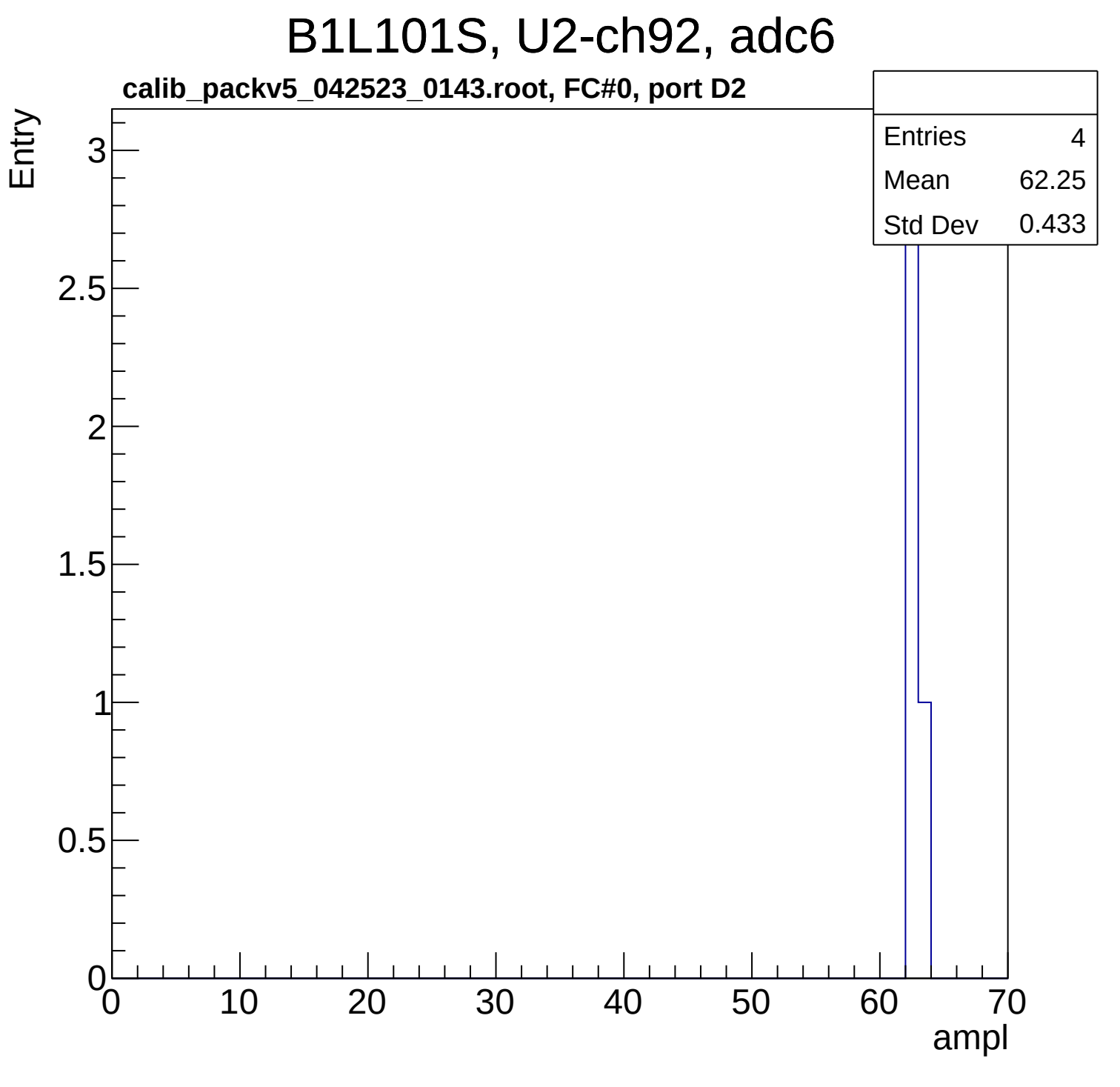

B1L101S, U2-ch92, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 36.64
Std Dev 3.514
Gaus mean : 37.3667
Gaus Width: 3.5231
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

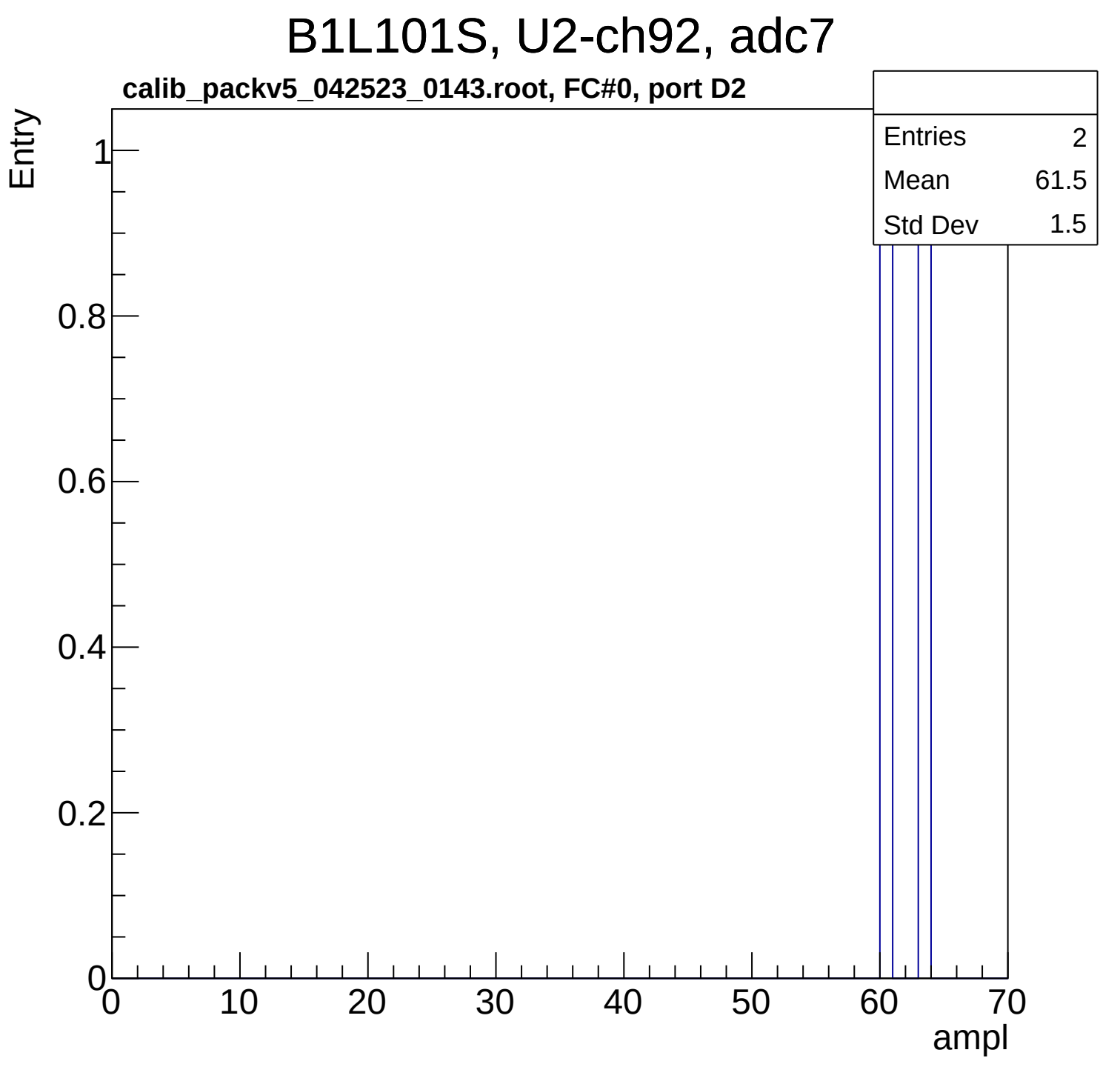

B1L101S, U2-ch92, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 42.46
Std Dev 3.562
Gaus mean : 43.2685
Gaus Width: 3.9501
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

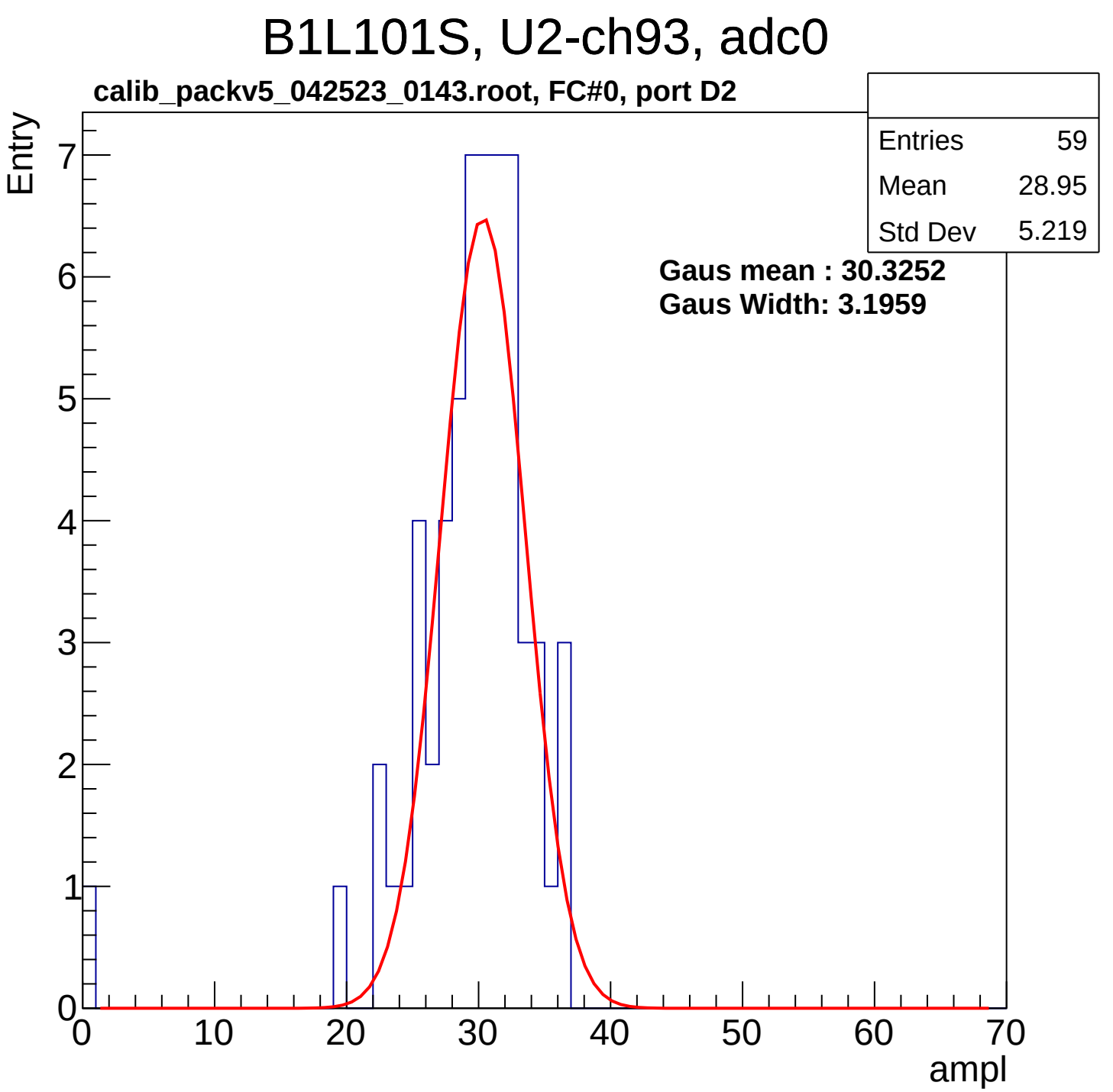

B1L101S, U2-ch92, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 49.3
Std Dev 3.507
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

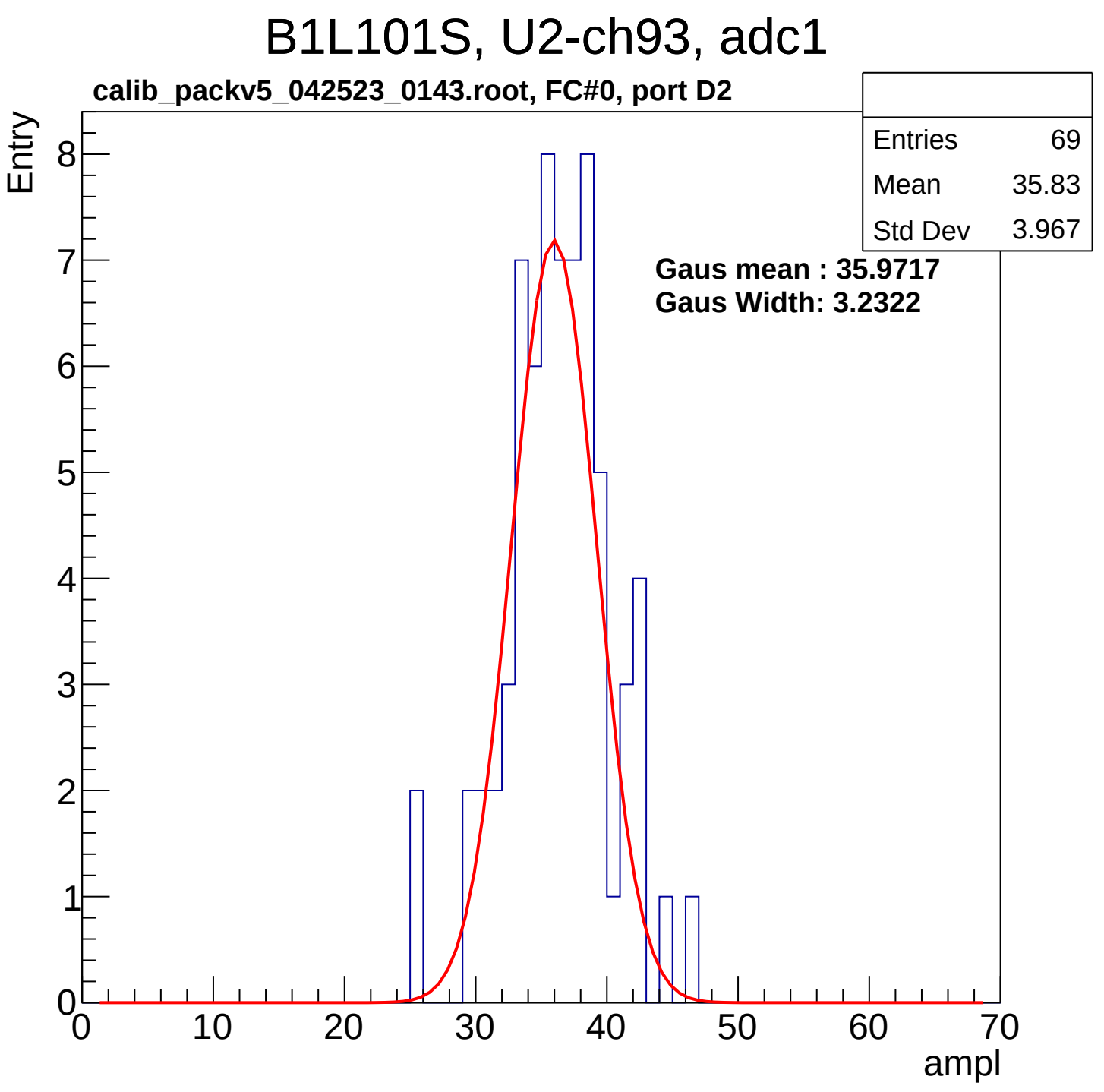

B1L101S, U2-ch92, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 56.18
Std Dev 3.617
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

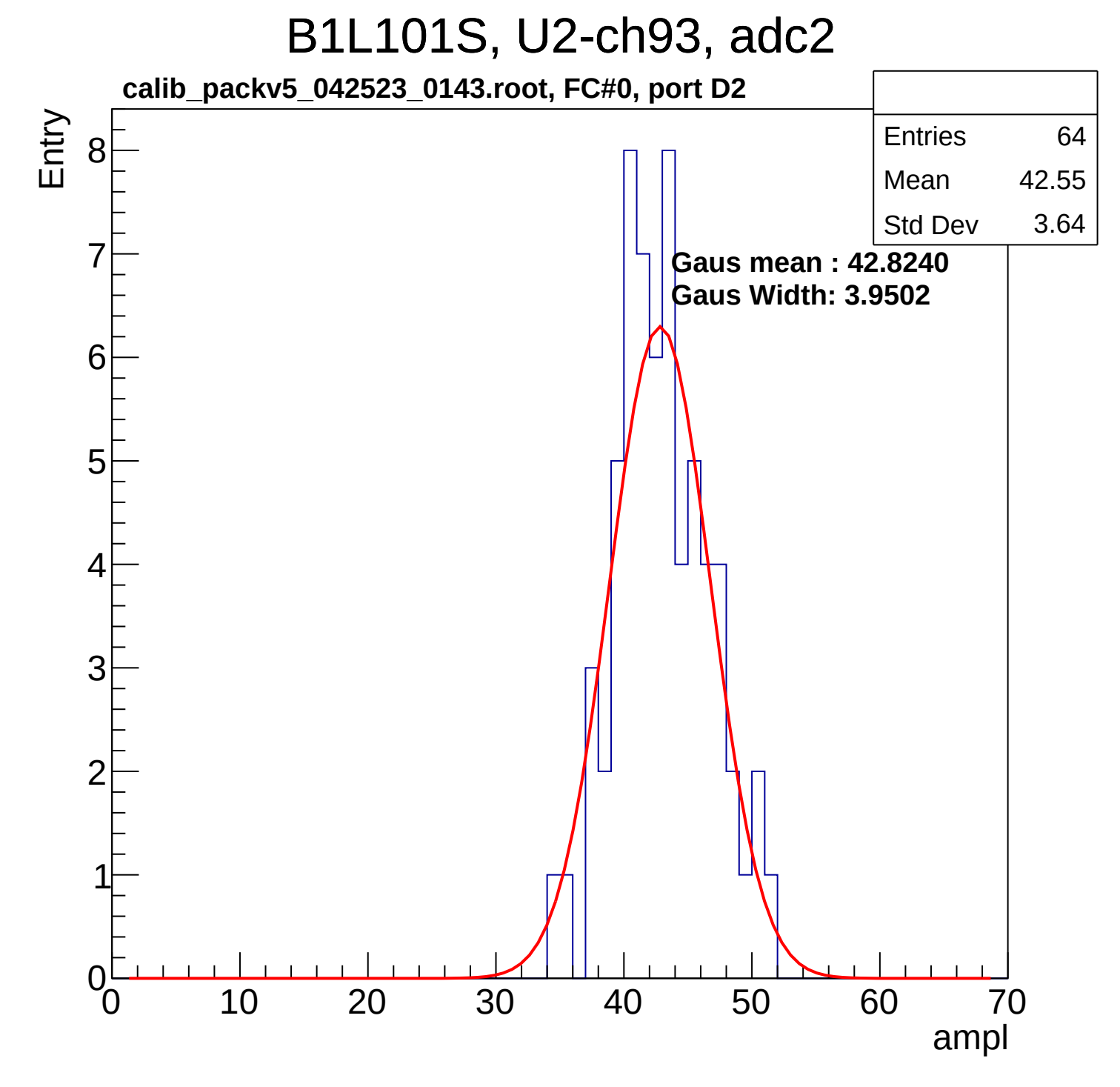

B1L101S, U2-ch92, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 41
Mean 57.98
Std Dev 9.496
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

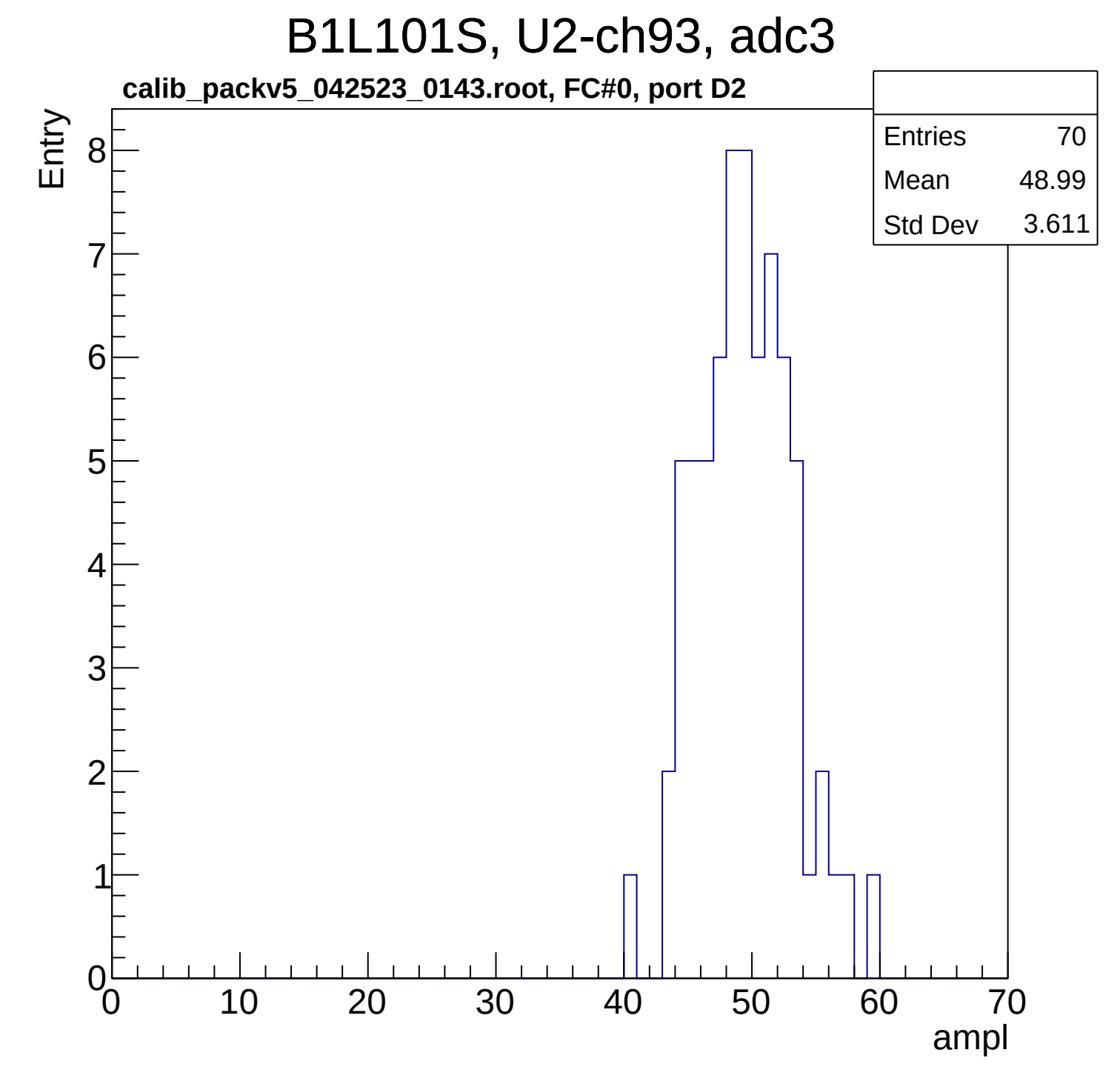

B1L101S, U2-ch92, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 62.25
Std Dev 0.433
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

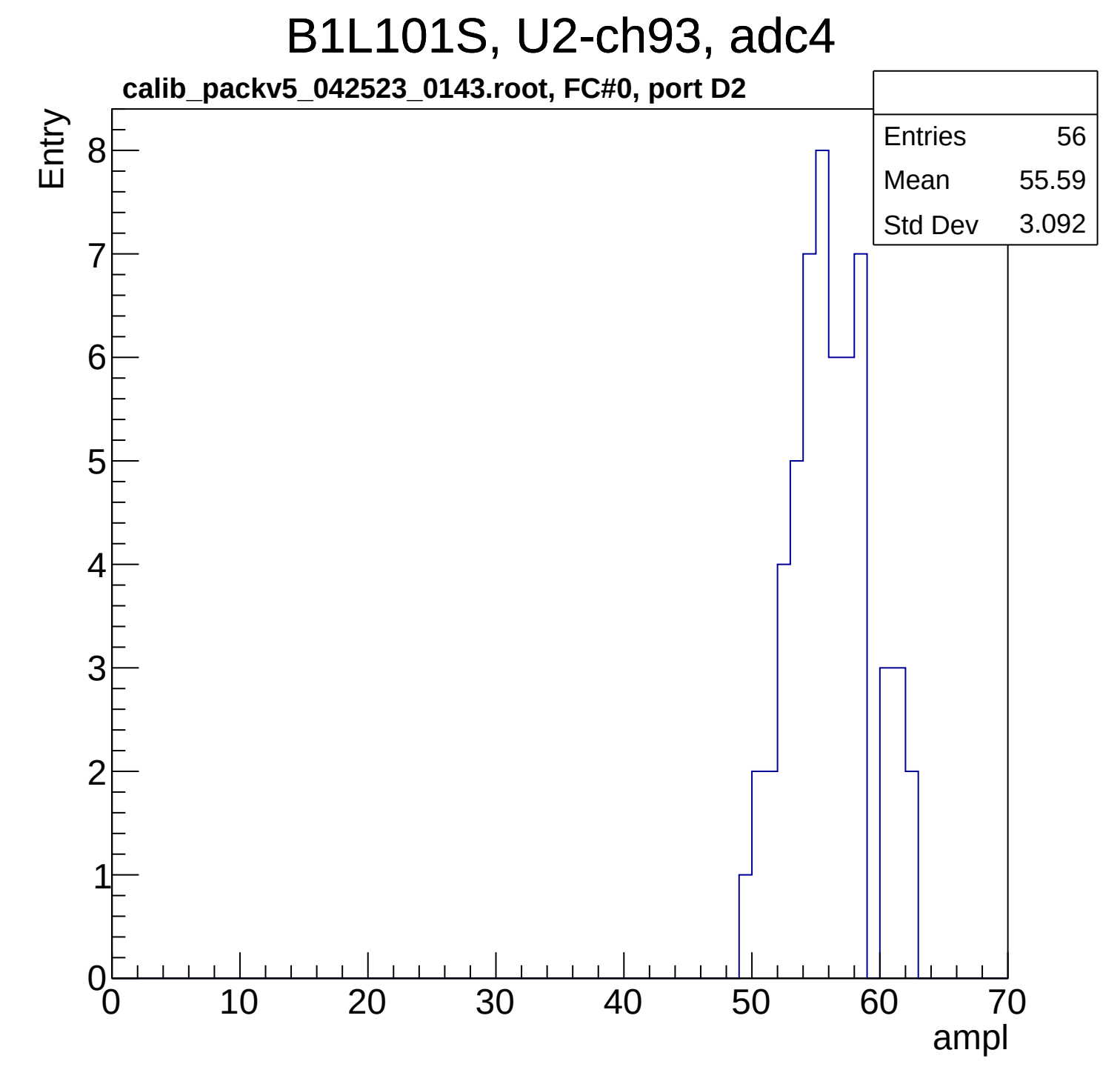

B1L101S, U2-ch92, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 61.5
Std Dev 1.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

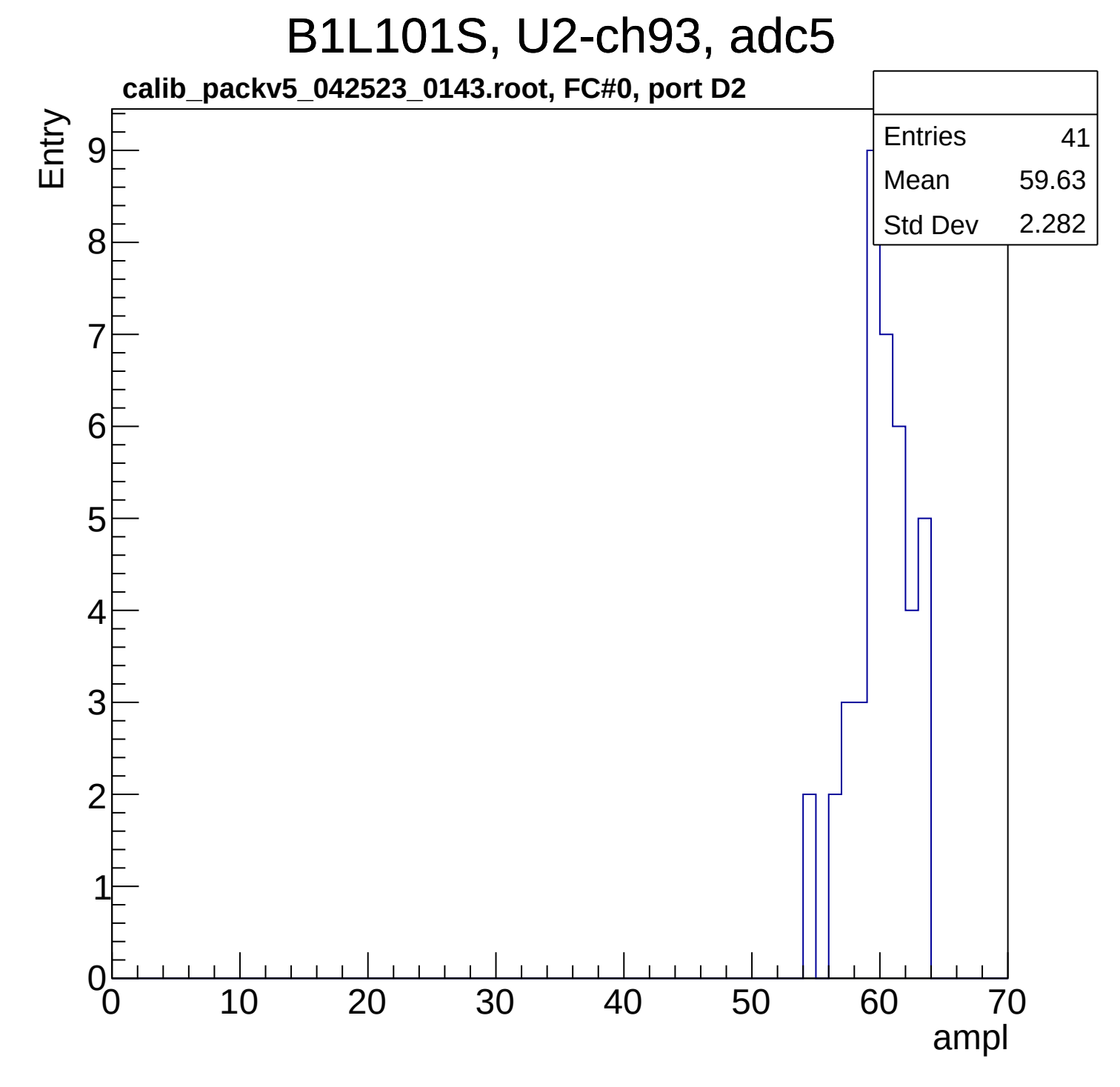

B1L101S, U2-ch93, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 28.95
Std Dev 5.219
Gaus mean : 30.3252
Gaus Width: 3.1959
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

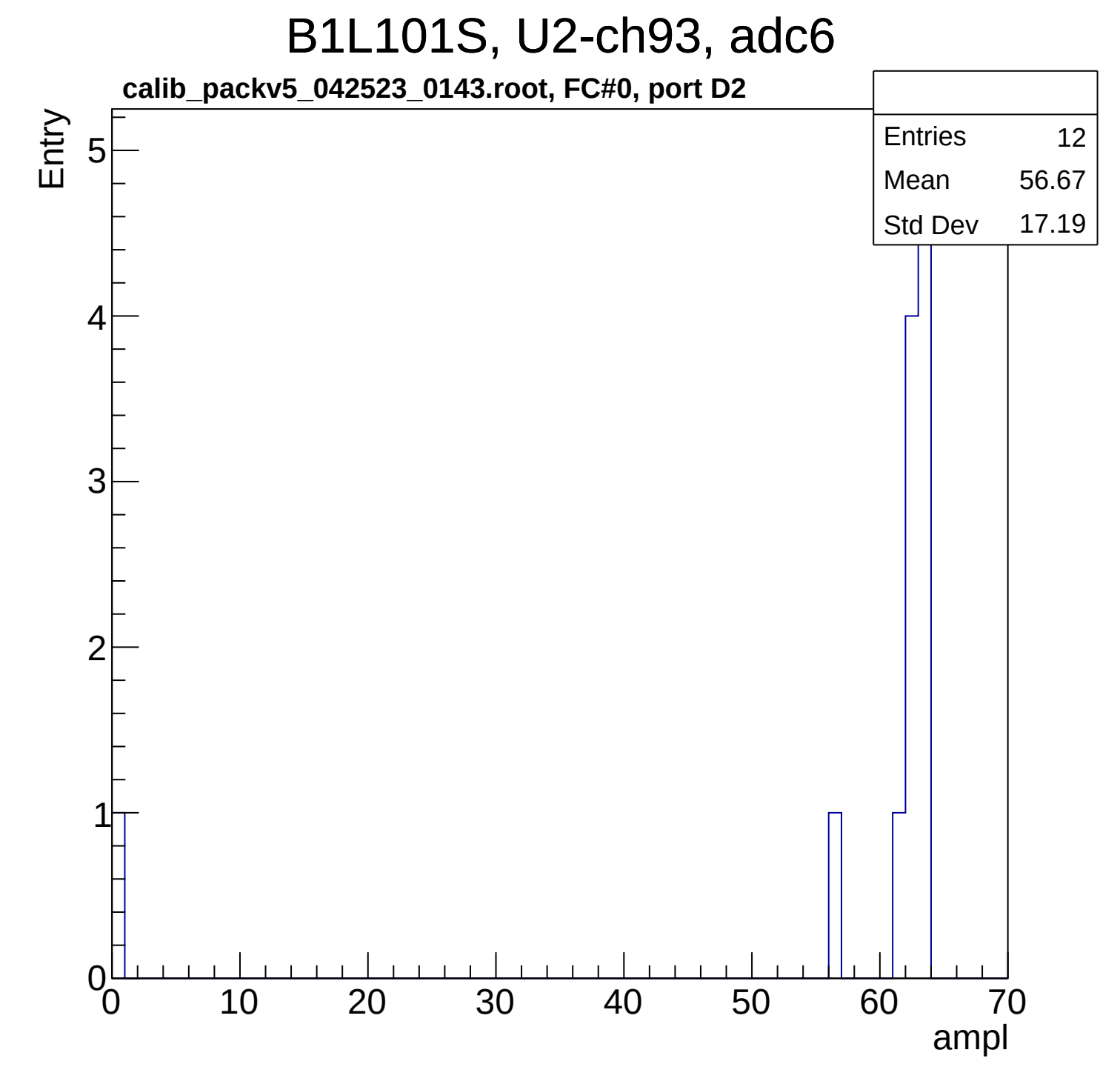

B1L101S, U2-ch93, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 35.83
Std Dev 3.967
Gaus mean : 35.9717
Gaus Width: 3.2322
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

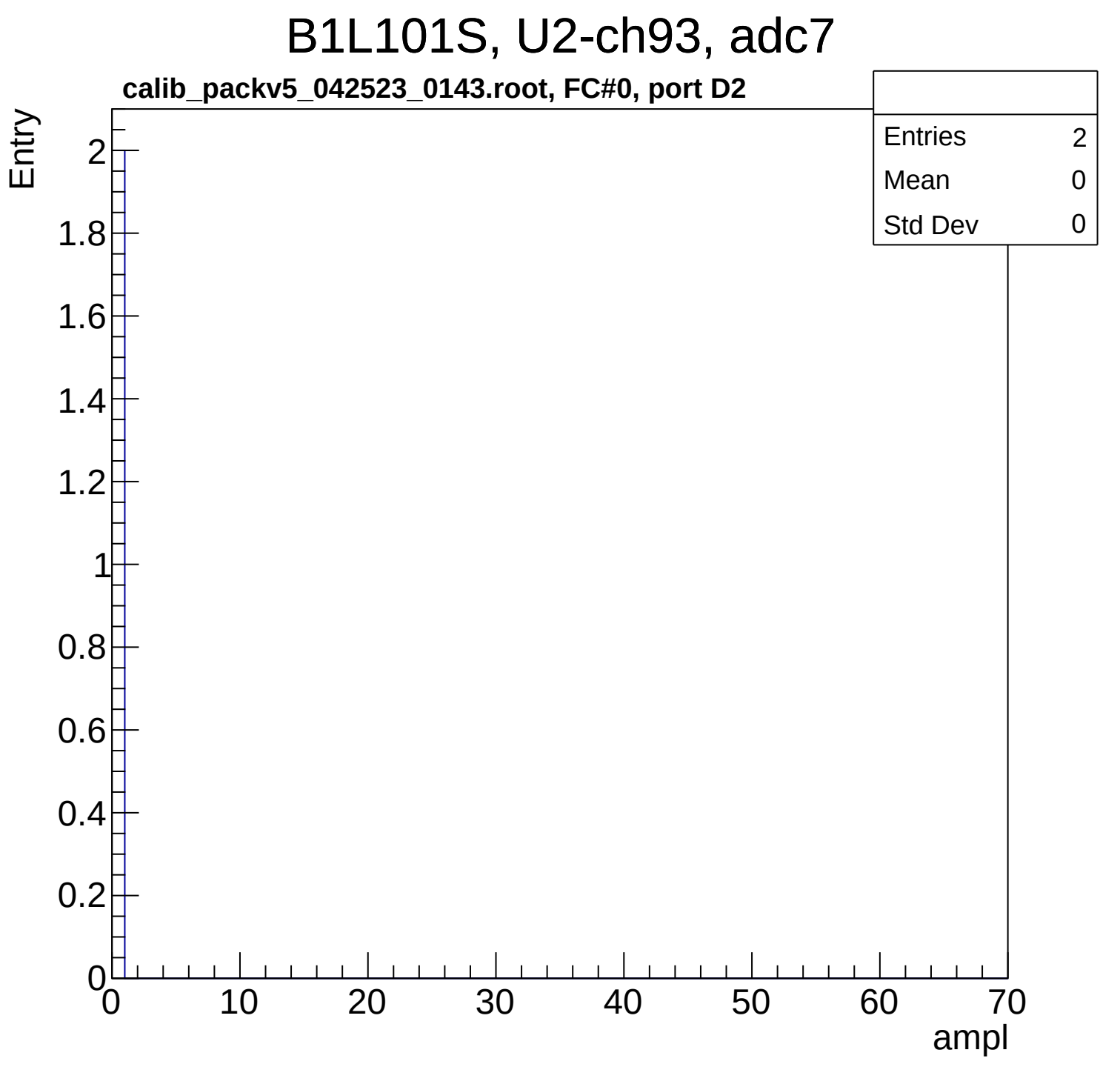

B1L101S, U2-ch93, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 42.55
Std Dev 3.64
Gaus mean : 42.8240
Gaus Width: 3.9502
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

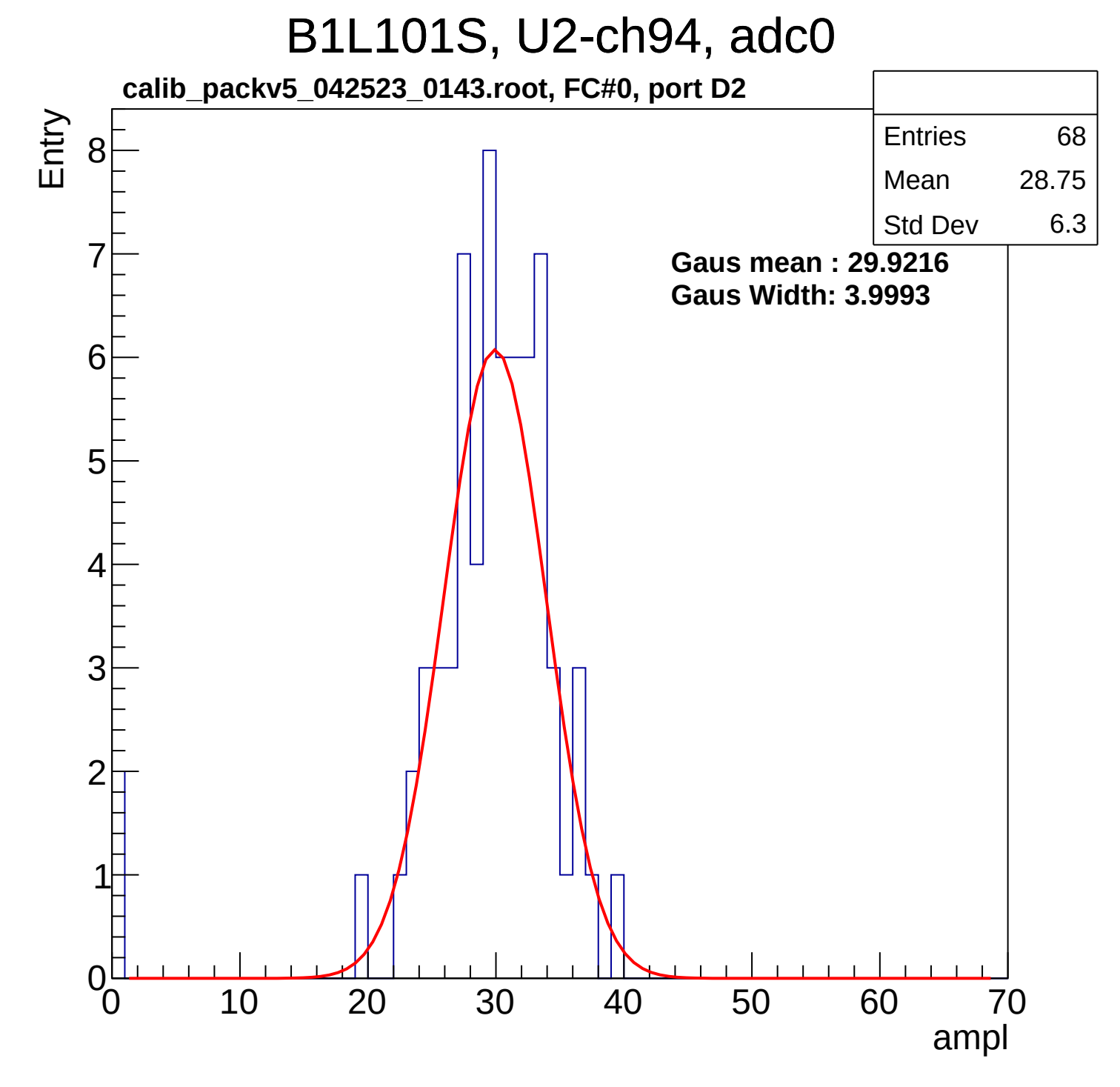

B1L101S, U2-ch93, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 48.99
Std Dev 3.611
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

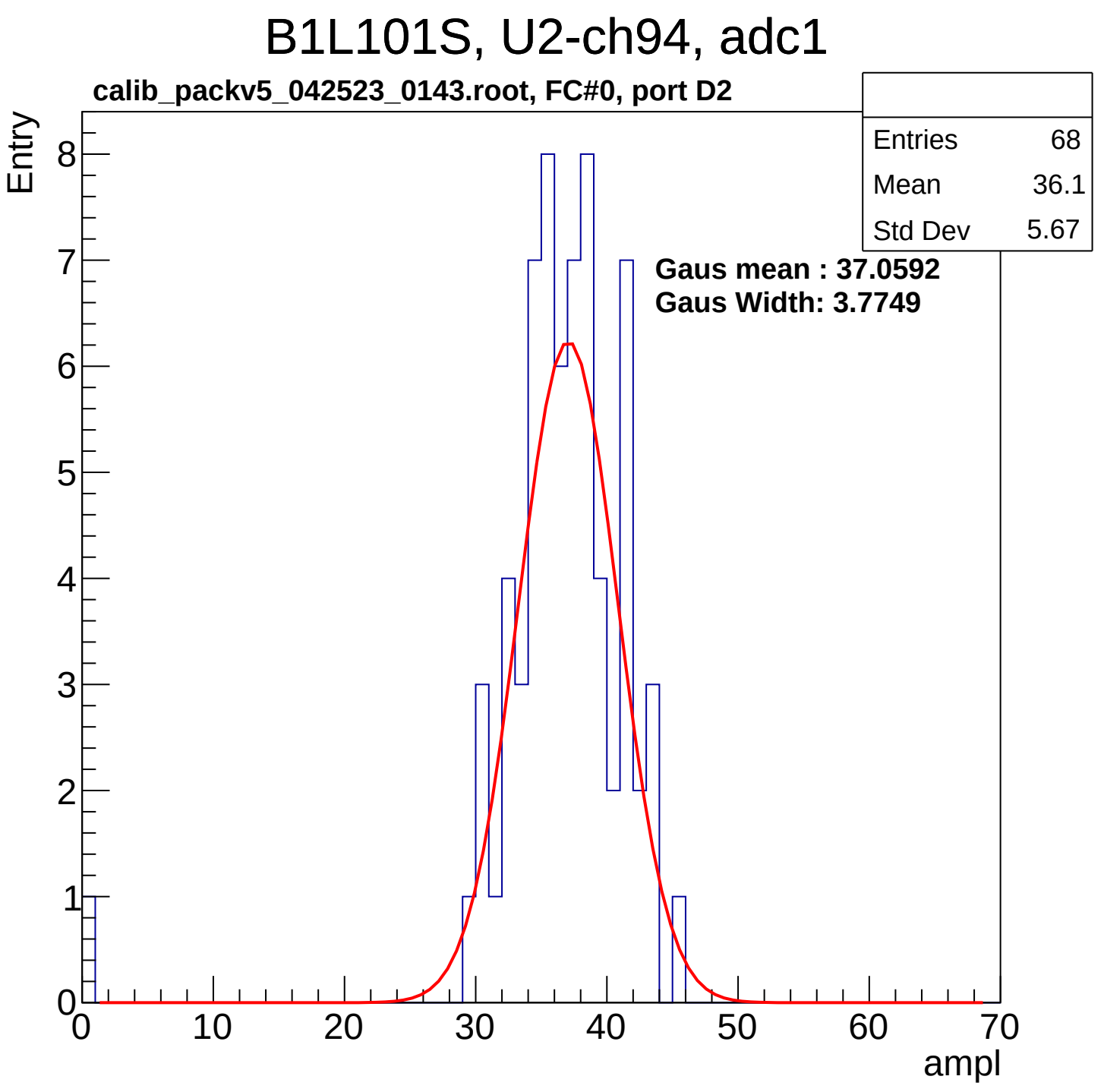

B1L101S, U2-ch93, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 55.59
Std Dev 3.092
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

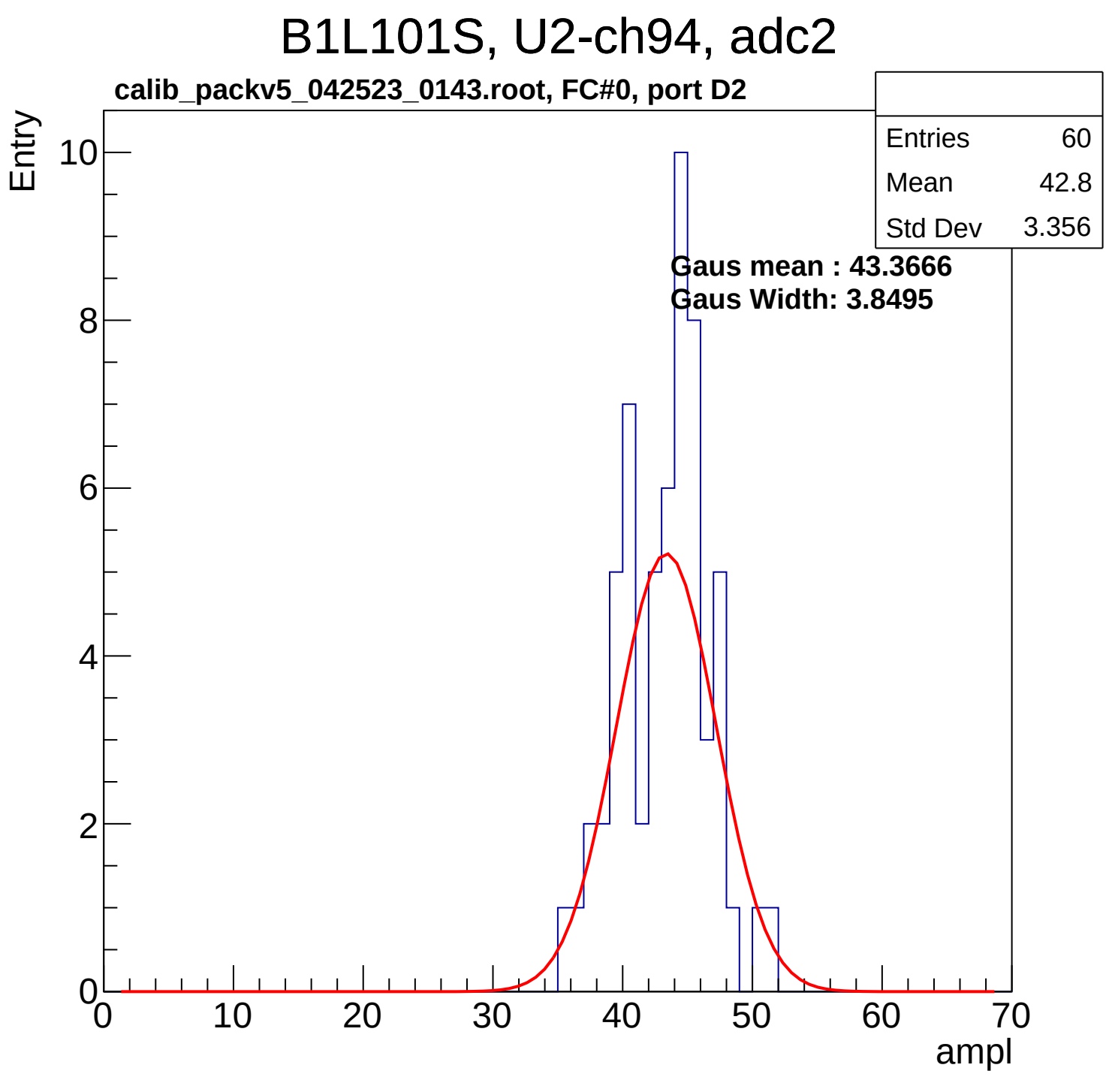

B1L101S, U2-ch93, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 41
Mean 59.63
Std Dev 2.282
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

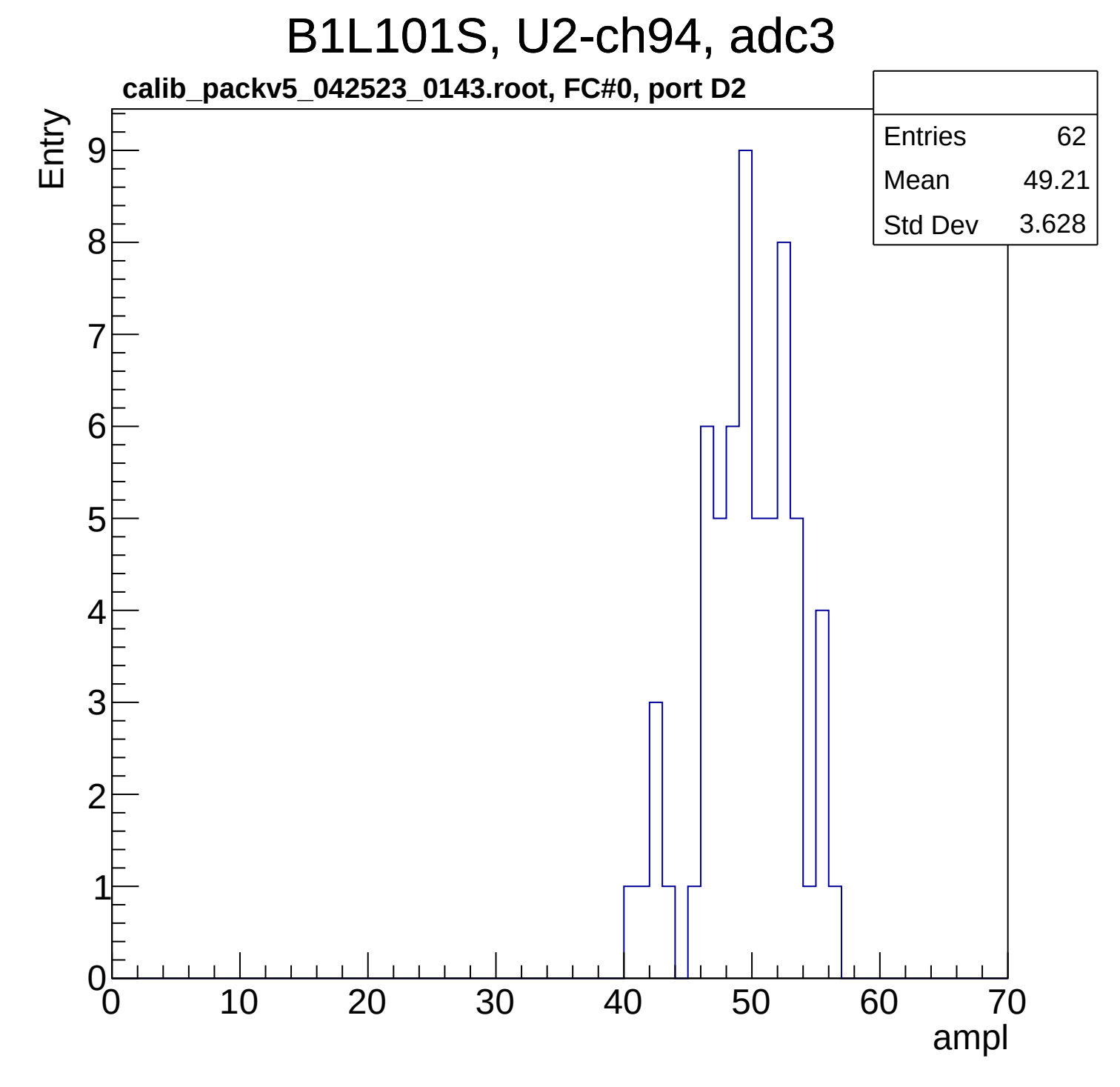

B1L101S, U2-ch93, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 12
Mean 56.67
Std Dev 17.19
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

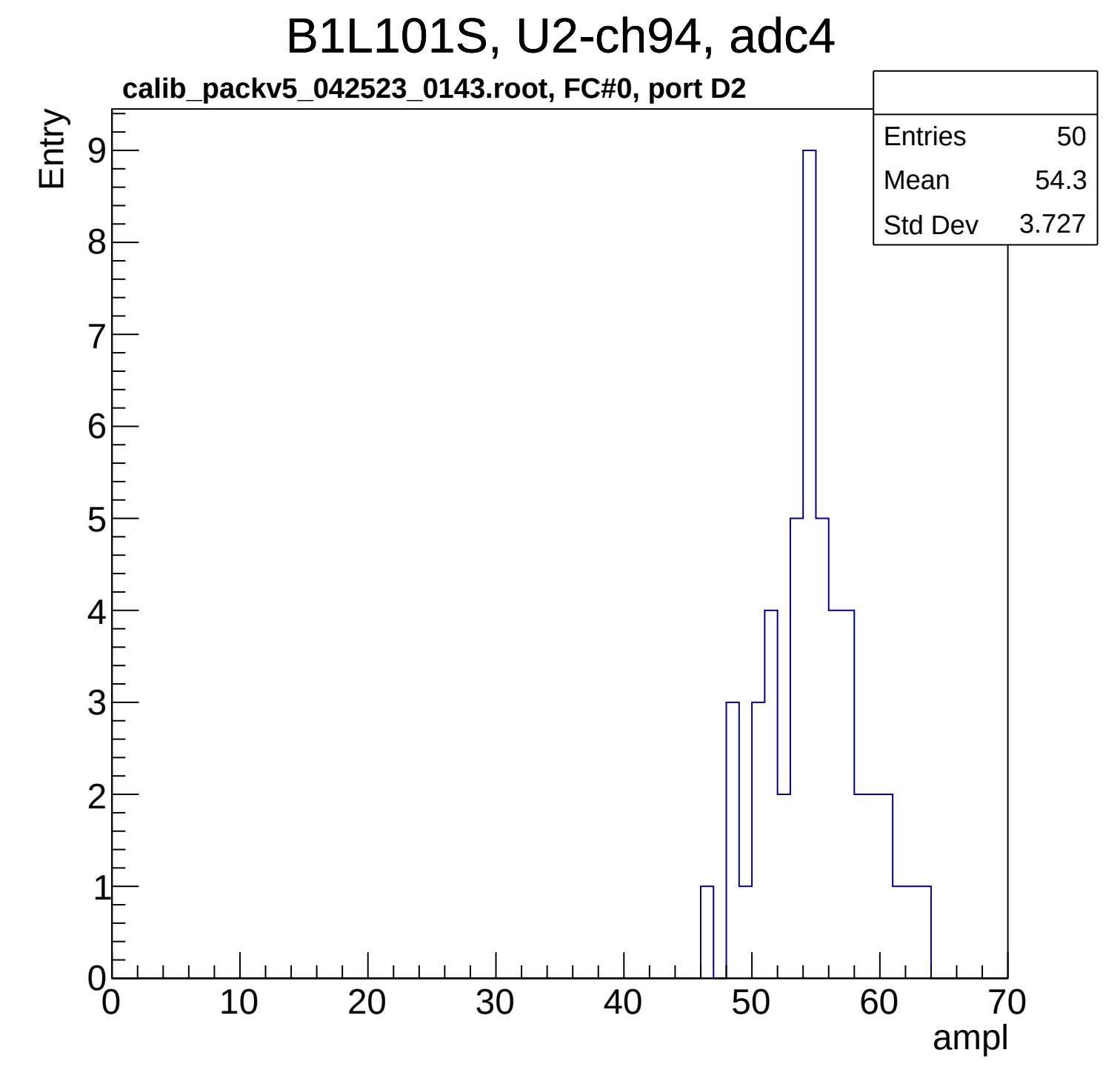

B1L101S, U2-ch93, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

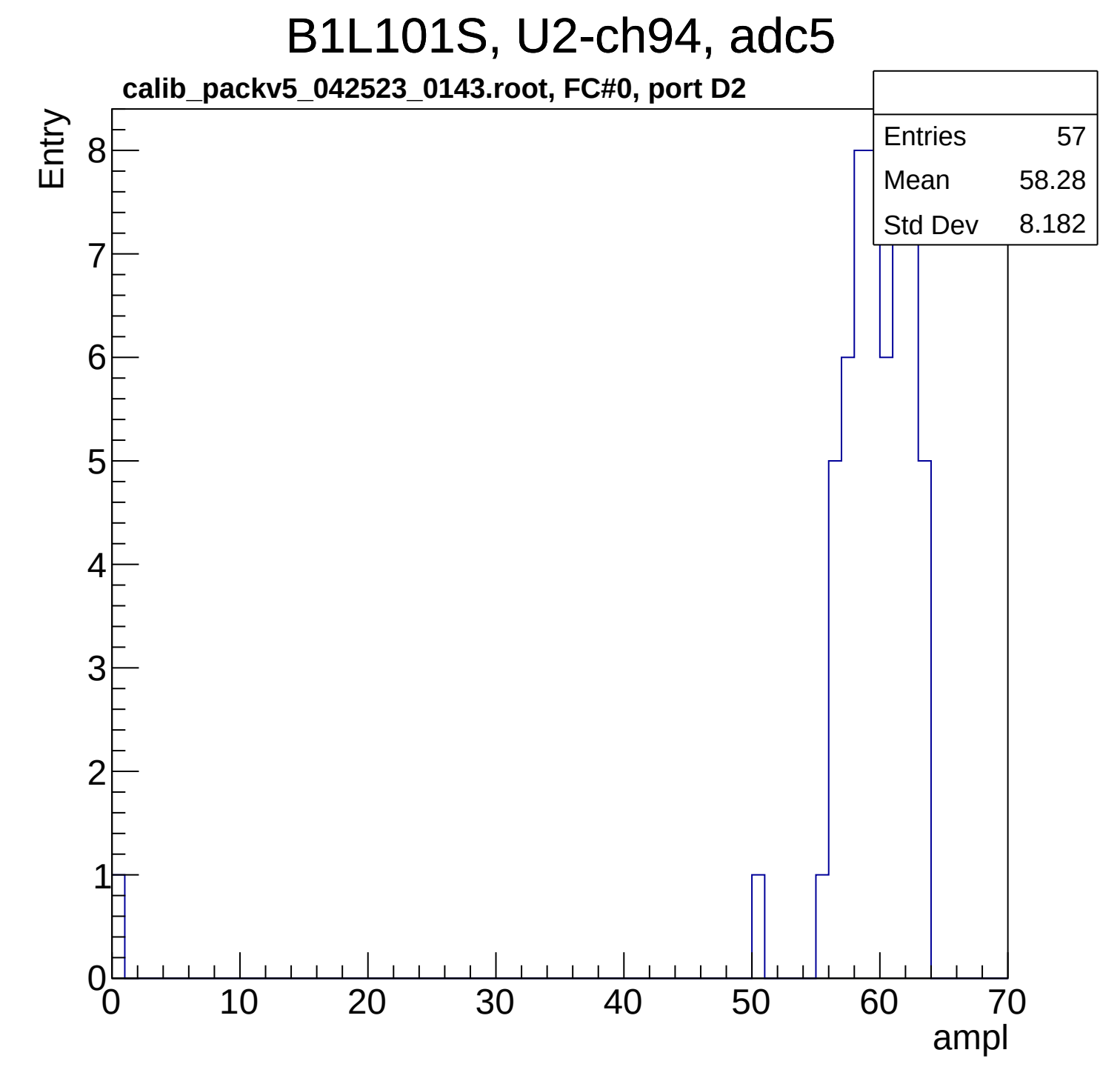

B1L101S, U2-ch94, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 28.75
Std Dev 6.3
Gaus mean : 29.9216
Gaus Width: 3.9993
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

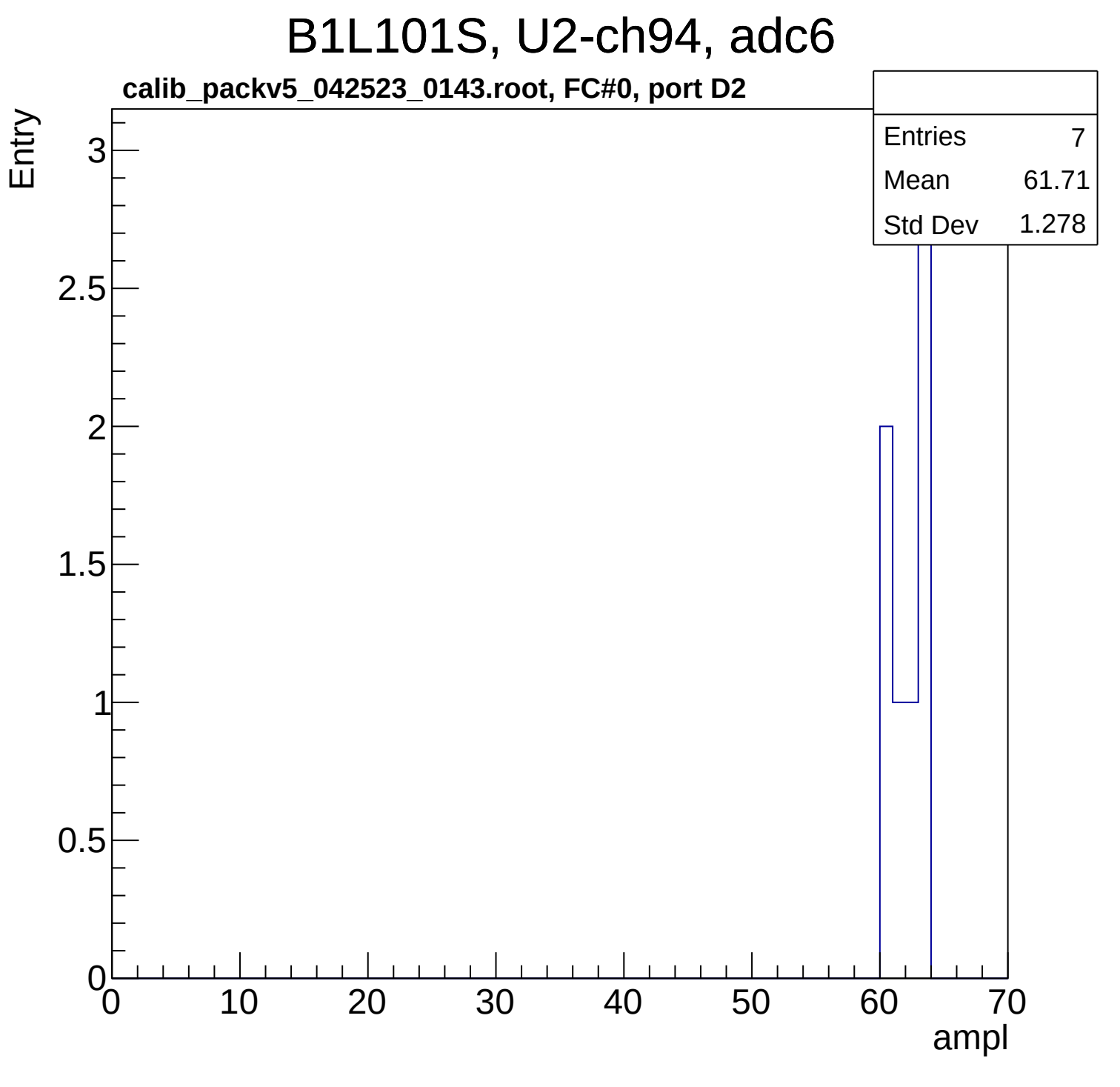

B1L101S, U2-ch94, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 36.1
Std Dev 5.67
Gaus mean : 37.0592
Gaus Width: 3.7749
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

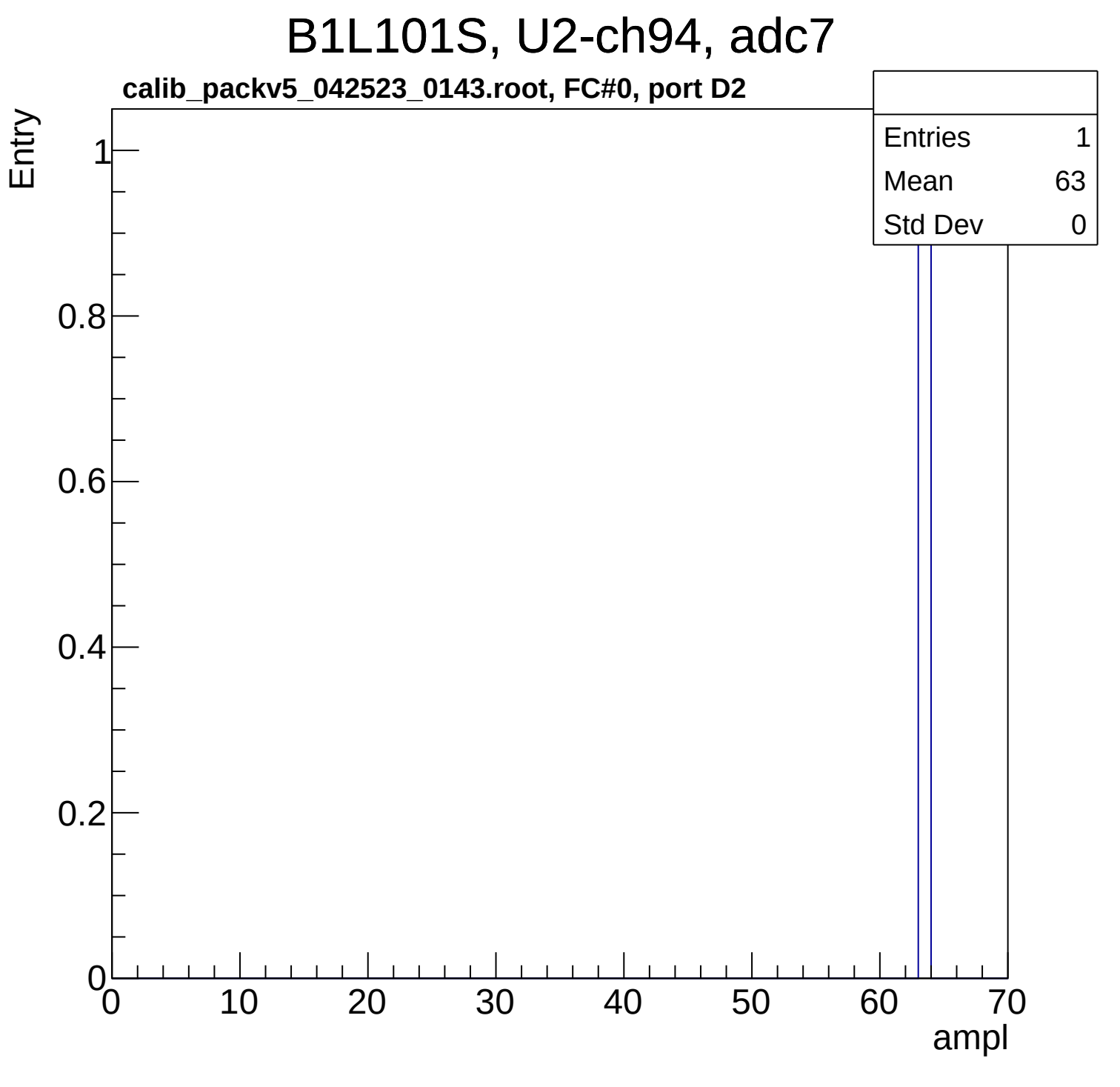

B1L101S, U2-ch94, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 42.8
Std Dev 3.356
Gaus mean : 43.3666
Gaus Width: 3.8495
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

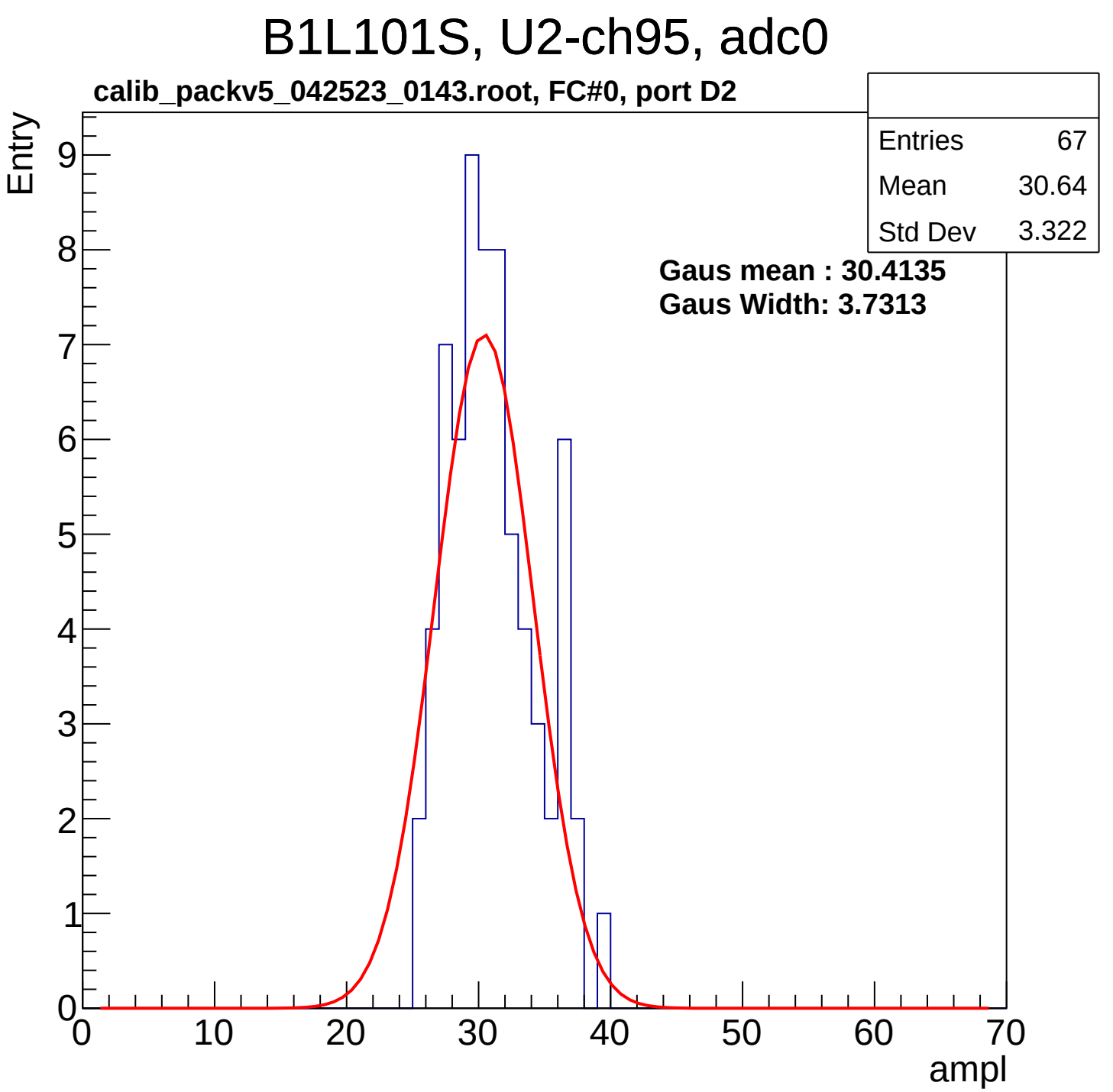

B1L101S, U2-ch94, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 49.21
Std Dev 3.628
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

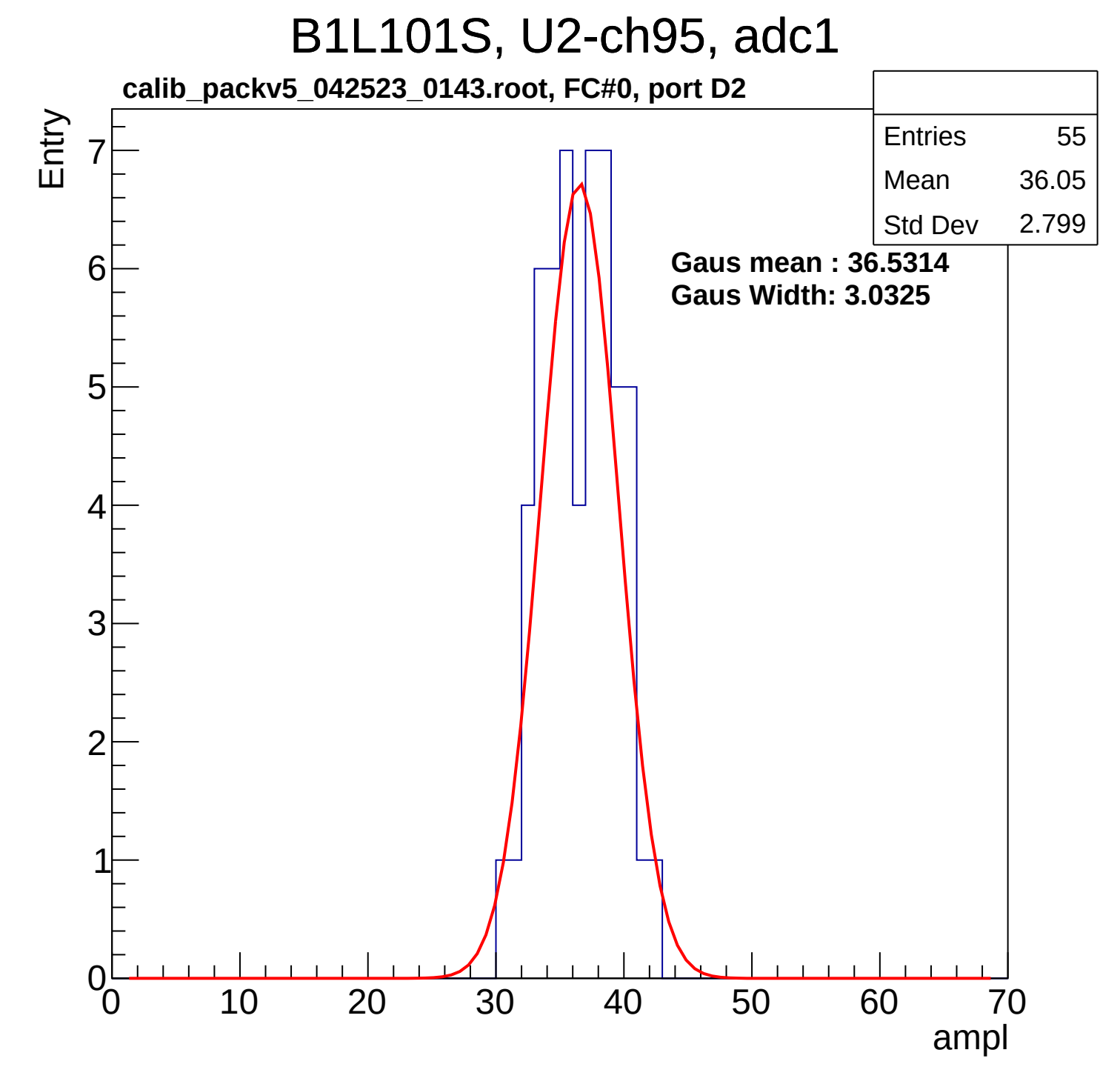

B1L101S, U2-ch94, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 54.3
Std Dev 3.727
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

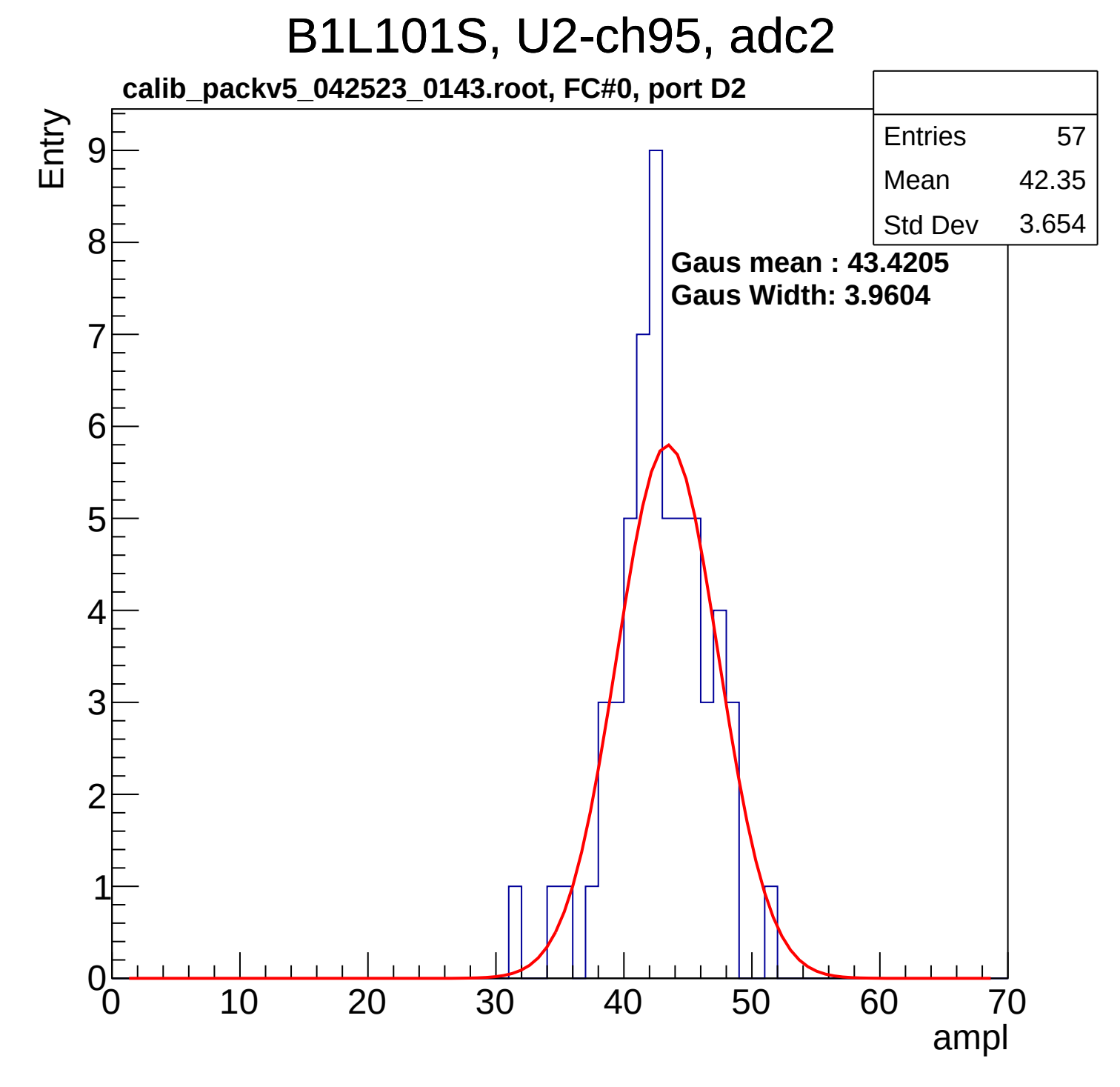

B1L101S, U2-ch94, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 58.28
Std Dev 8.182
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

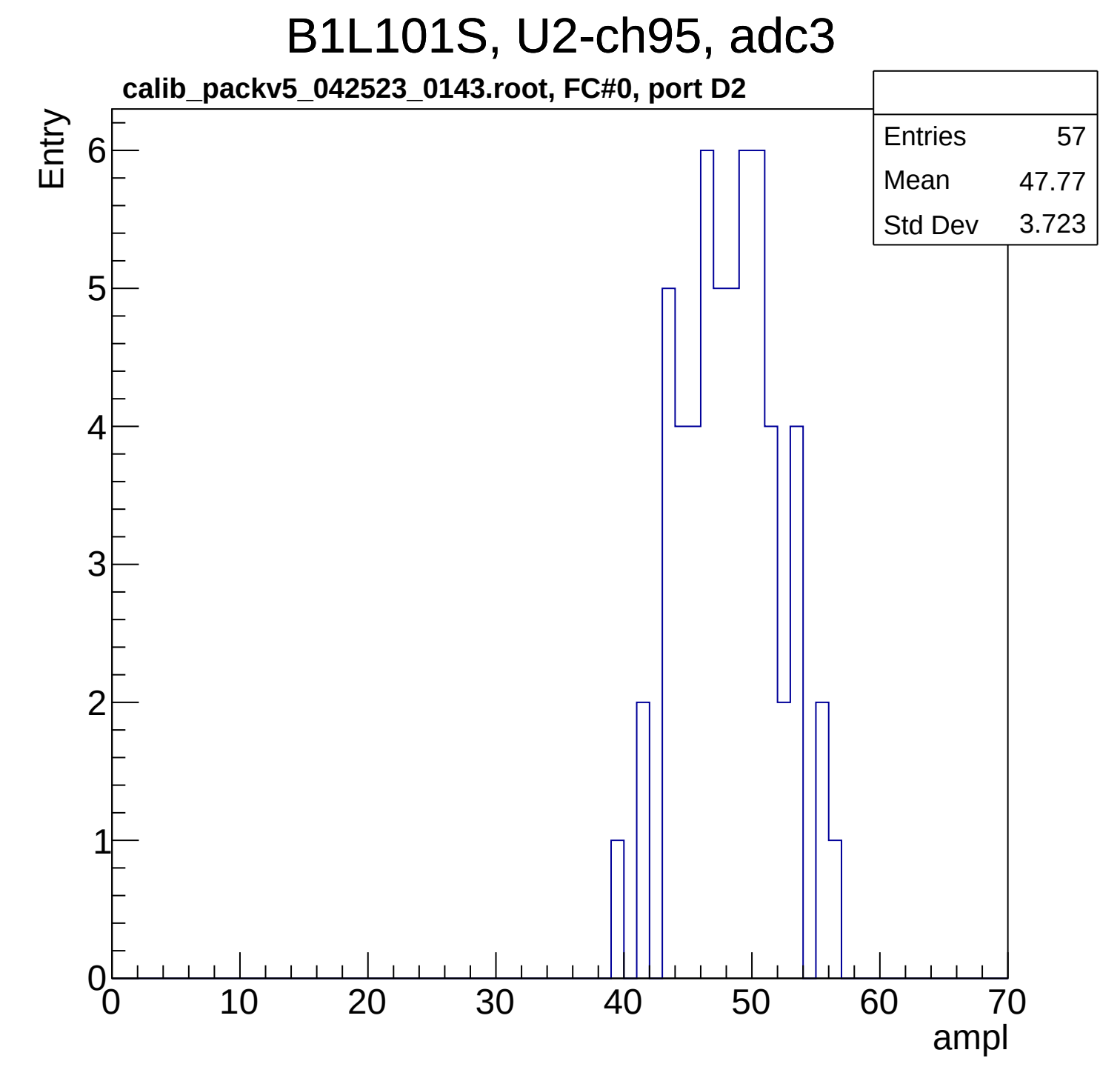

B1L101S, U2-ch94, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 61.71
Std Dev 1.278
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

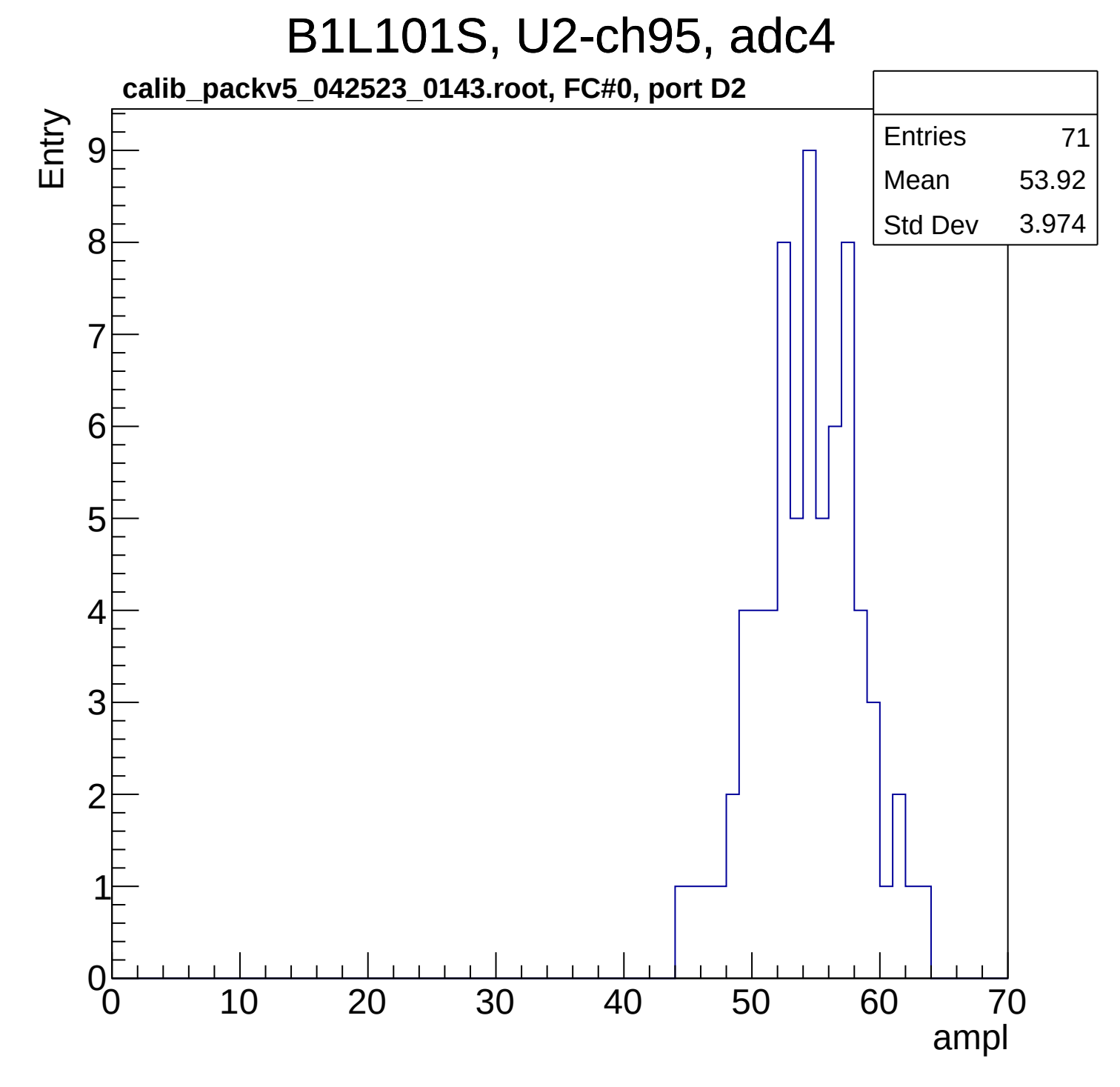

B1L101S, U2-ch94, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

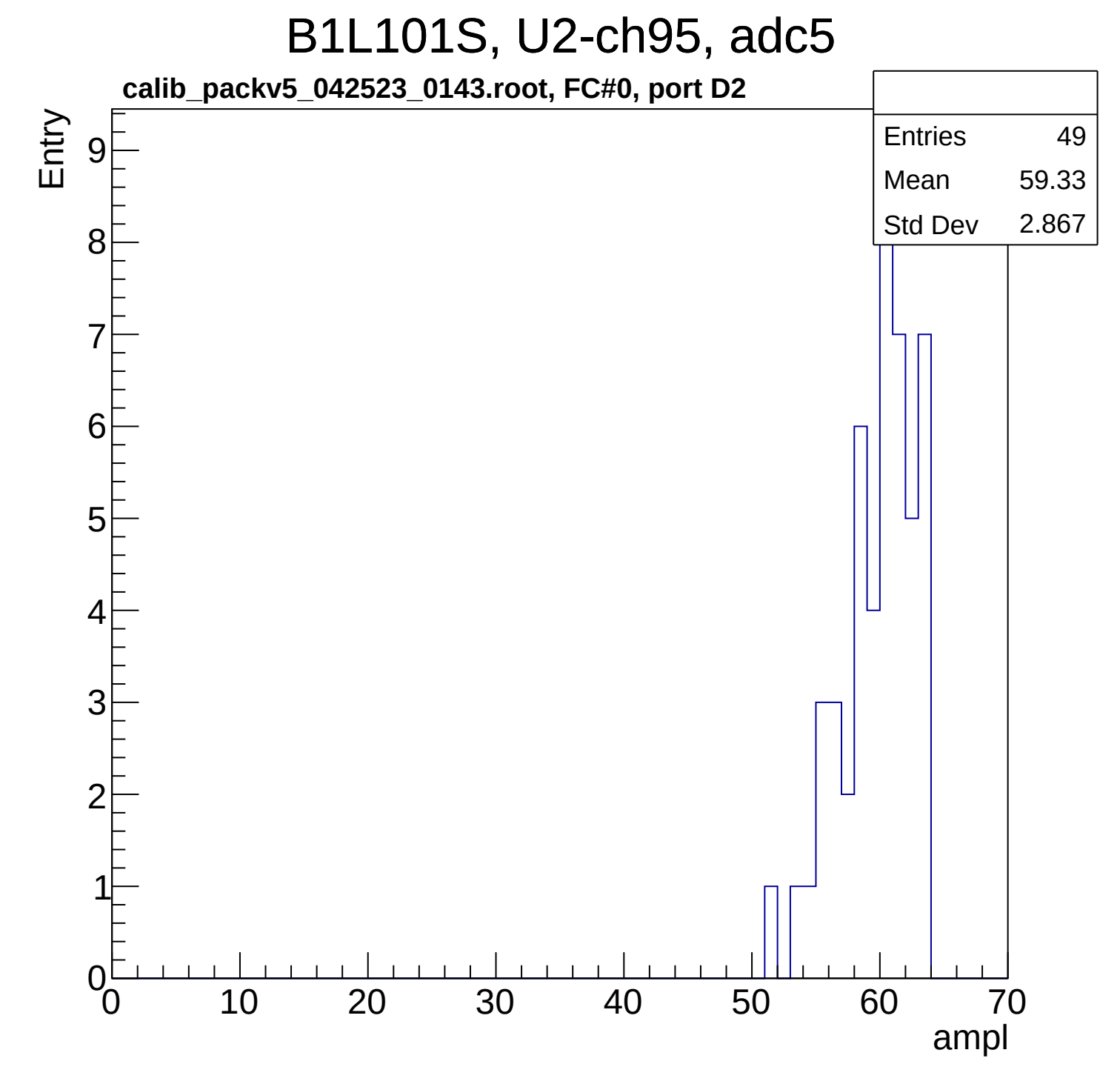

B1L101S, U2-ch95, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 30.64
Std Dev 3.322
Gaus mean : 30.4135
Gaus Width: 3.7313
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

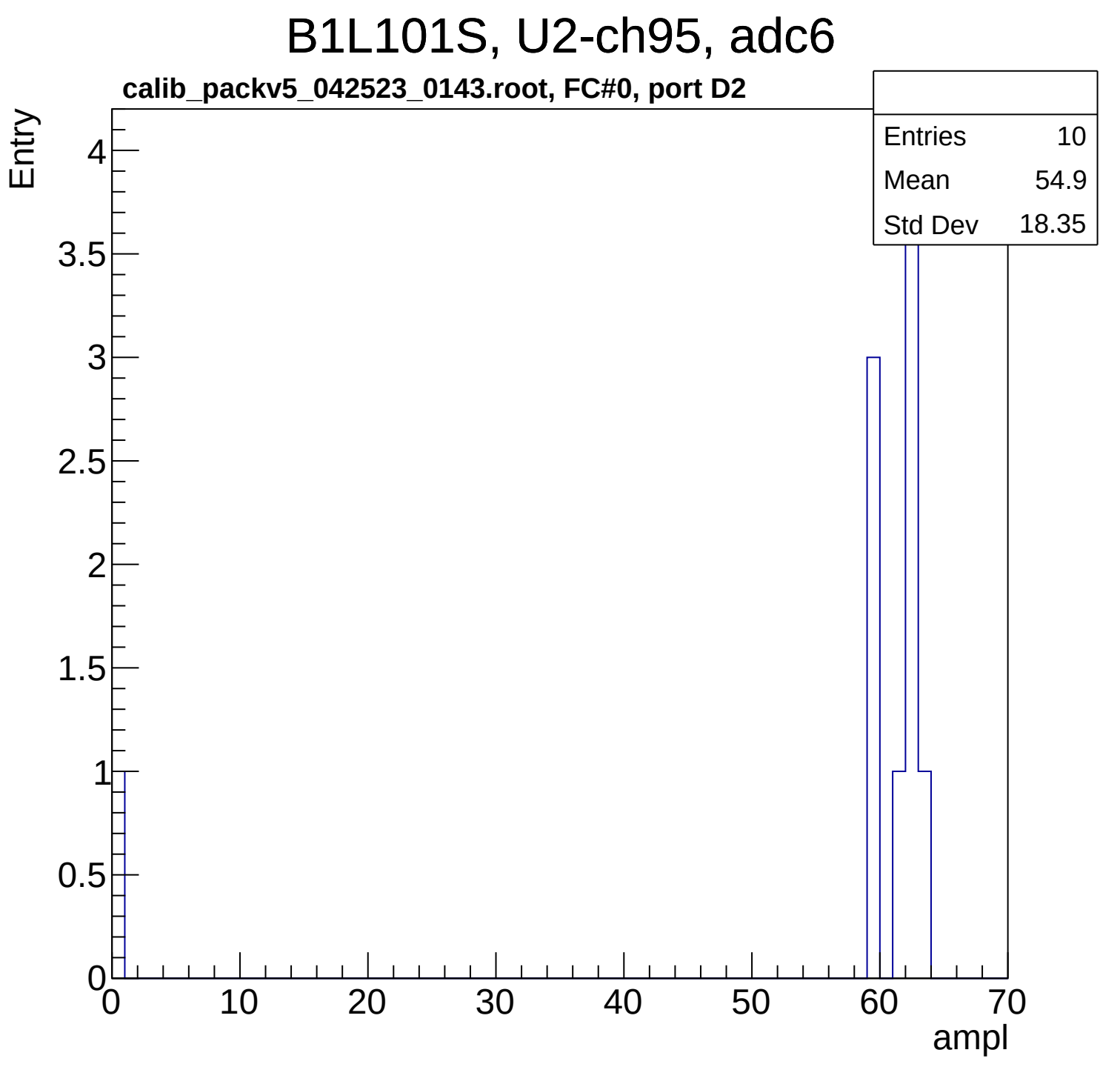

B1L101S, U2-ch95, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 36.05
Std Dev 2.799
Gaus mean : 36.5314
Gaus Width: 3.0325
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

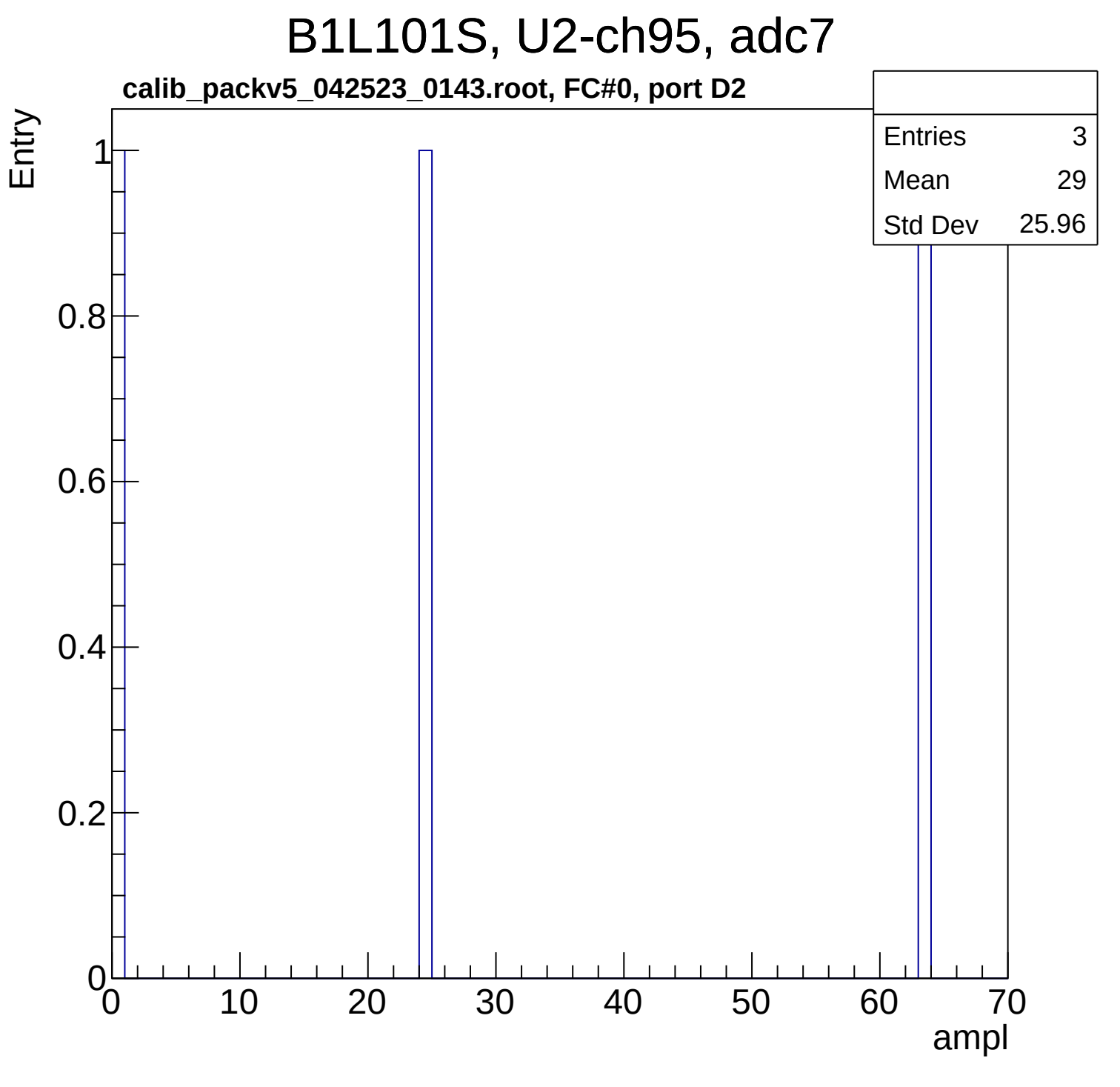

B1L101S, U2-ch95, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 42.35
Std Dev 3.654
Gaus mean : 43.4205
Gaus Width: 3.9604
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

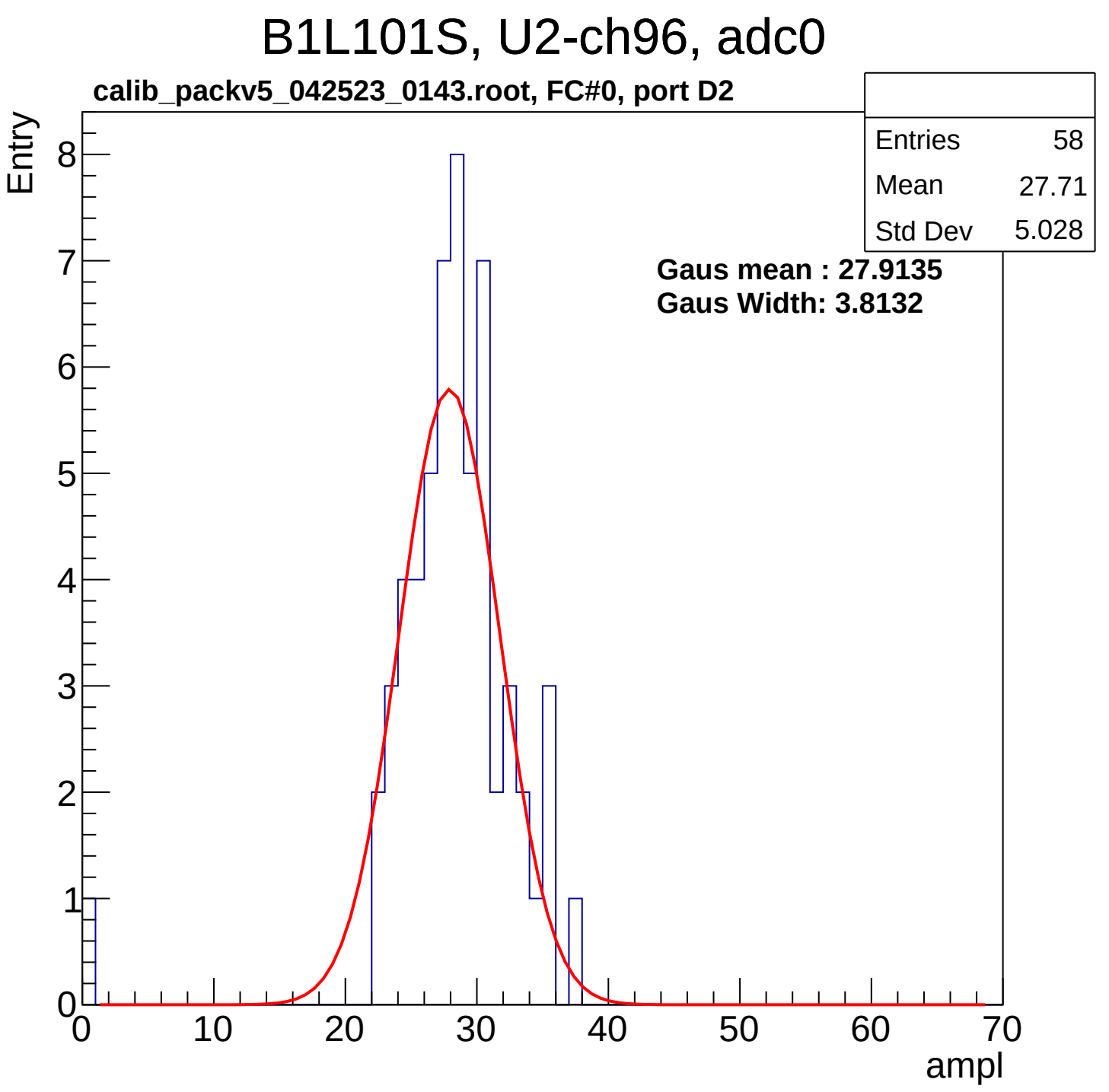

B1L101S, U2-ch95, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 47.77
Std Dev 3.723
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

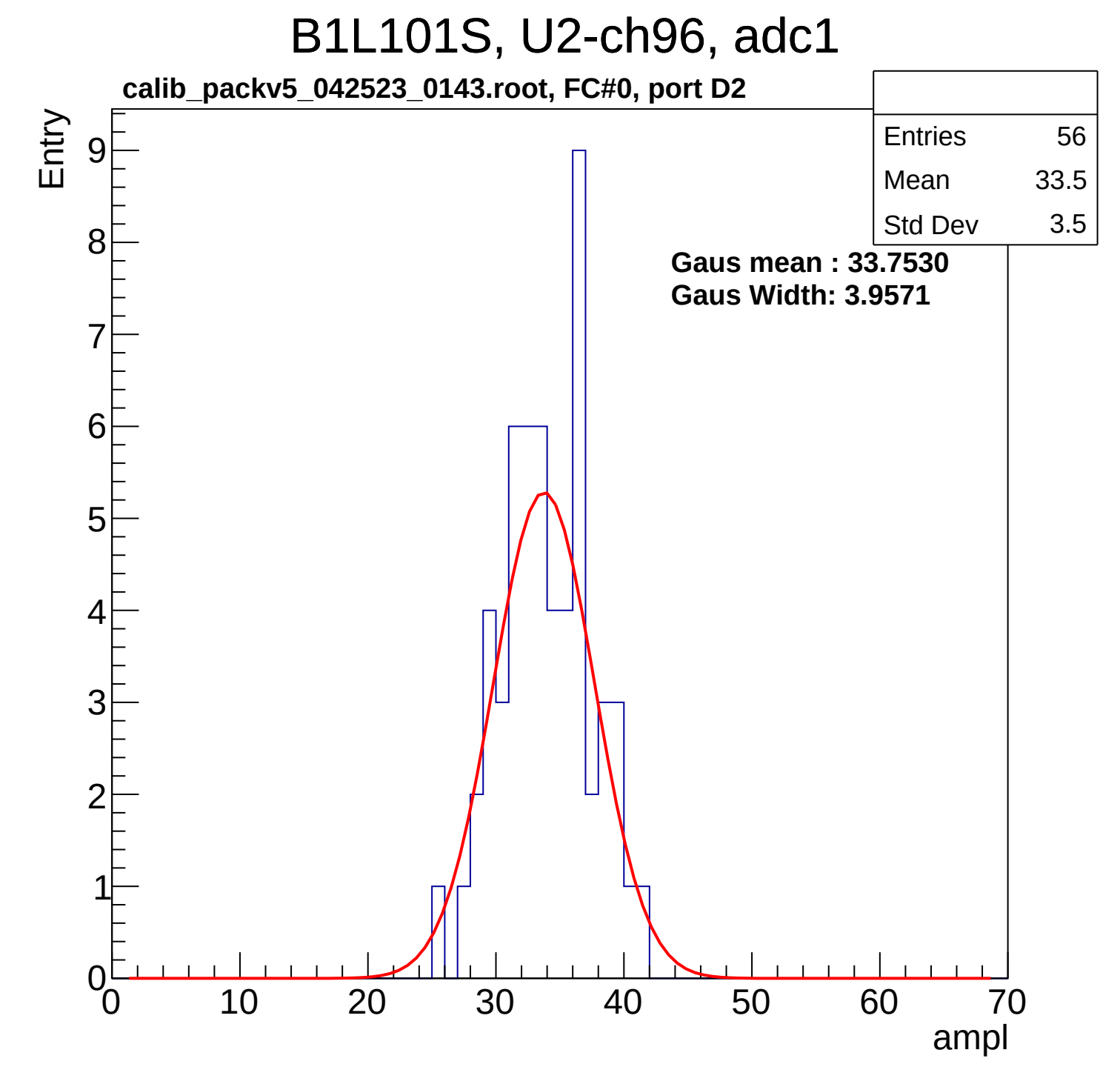

B1L101S, U2-ch95, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 53.92
Std Dev 3.974
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

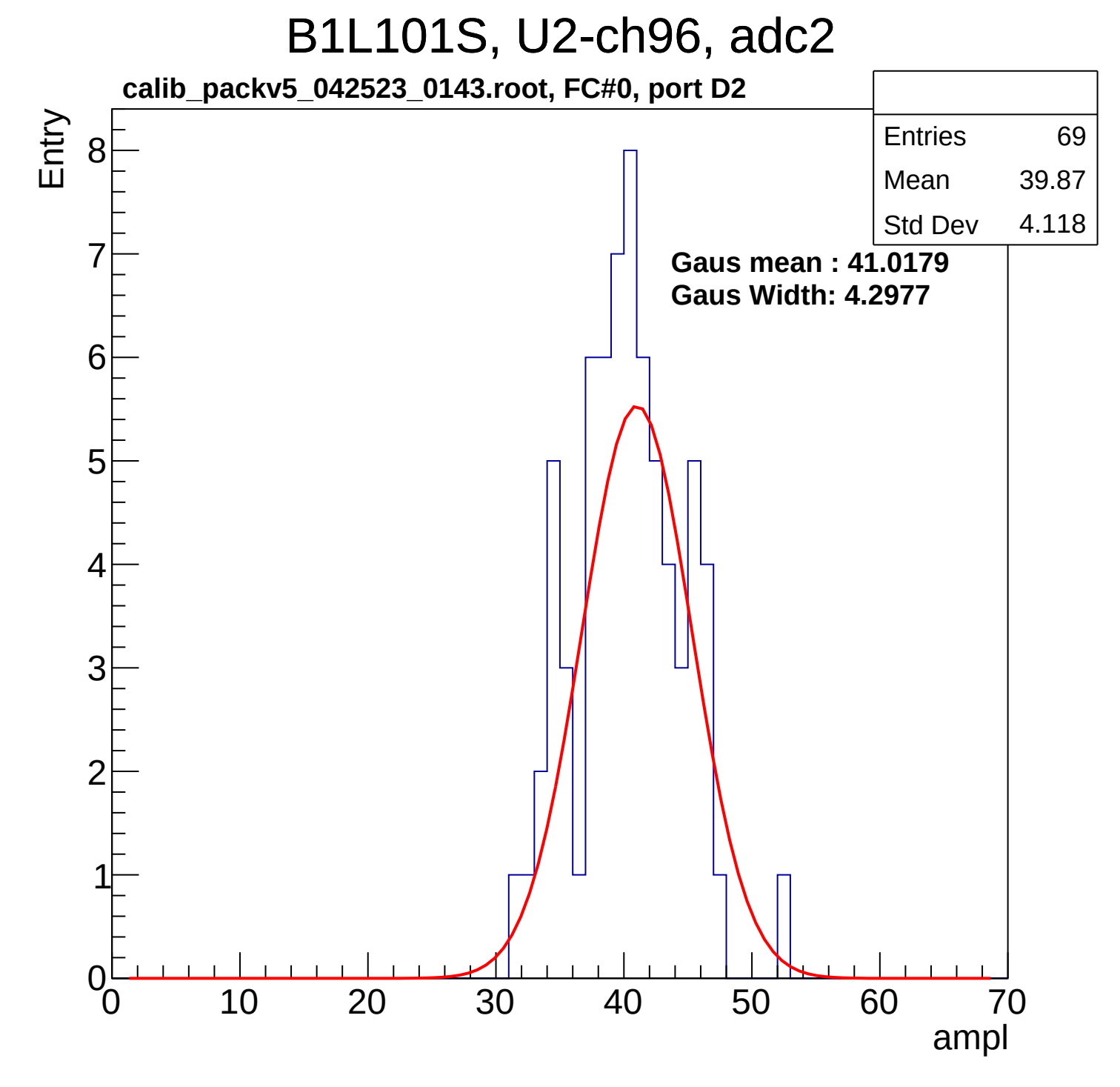

B1L101S, U2-ch95, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 59.33
Std Dev 2.867
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

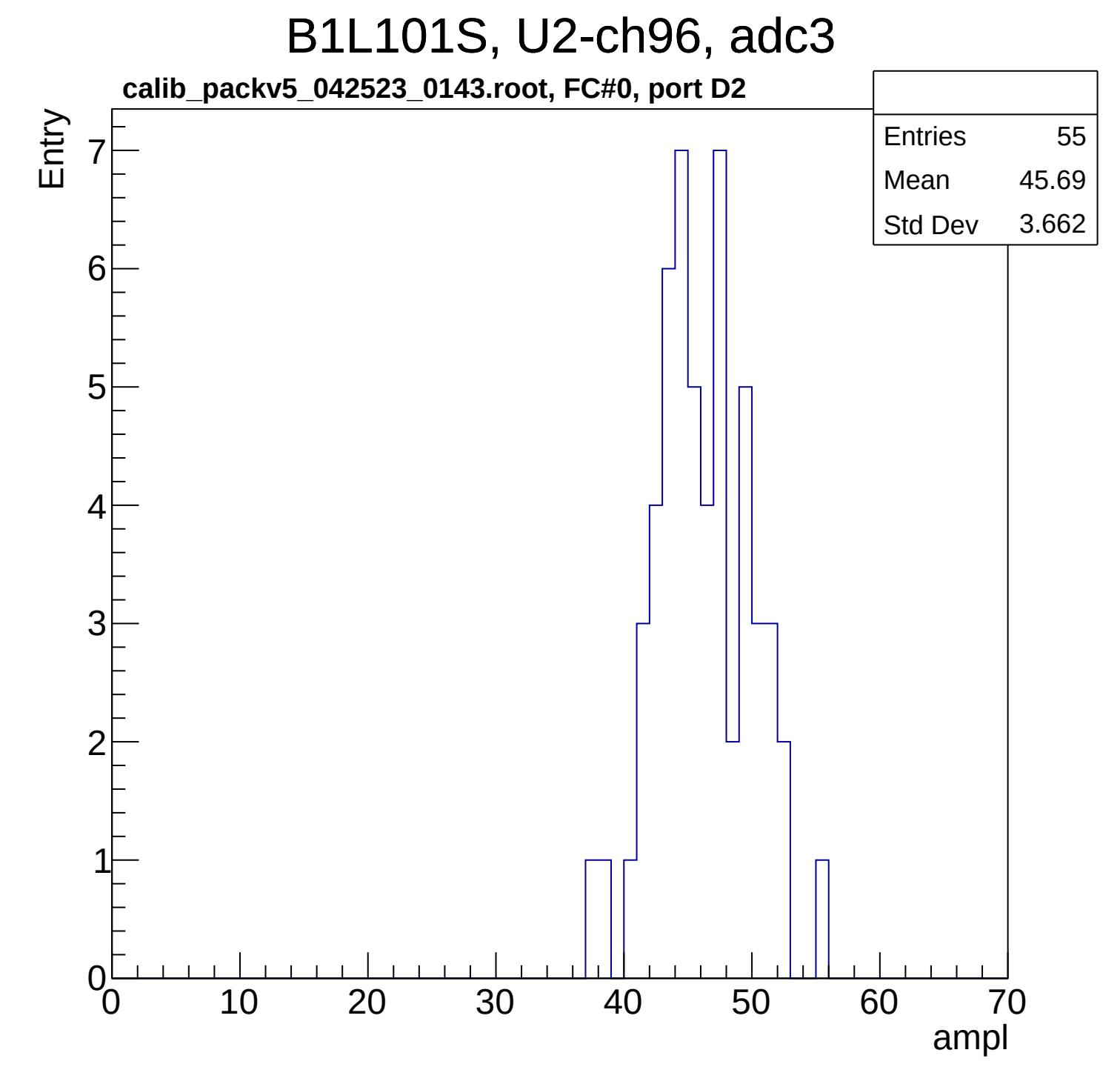

B1L101S, U2-ch95, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 54.9
Std Dev 18.35
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

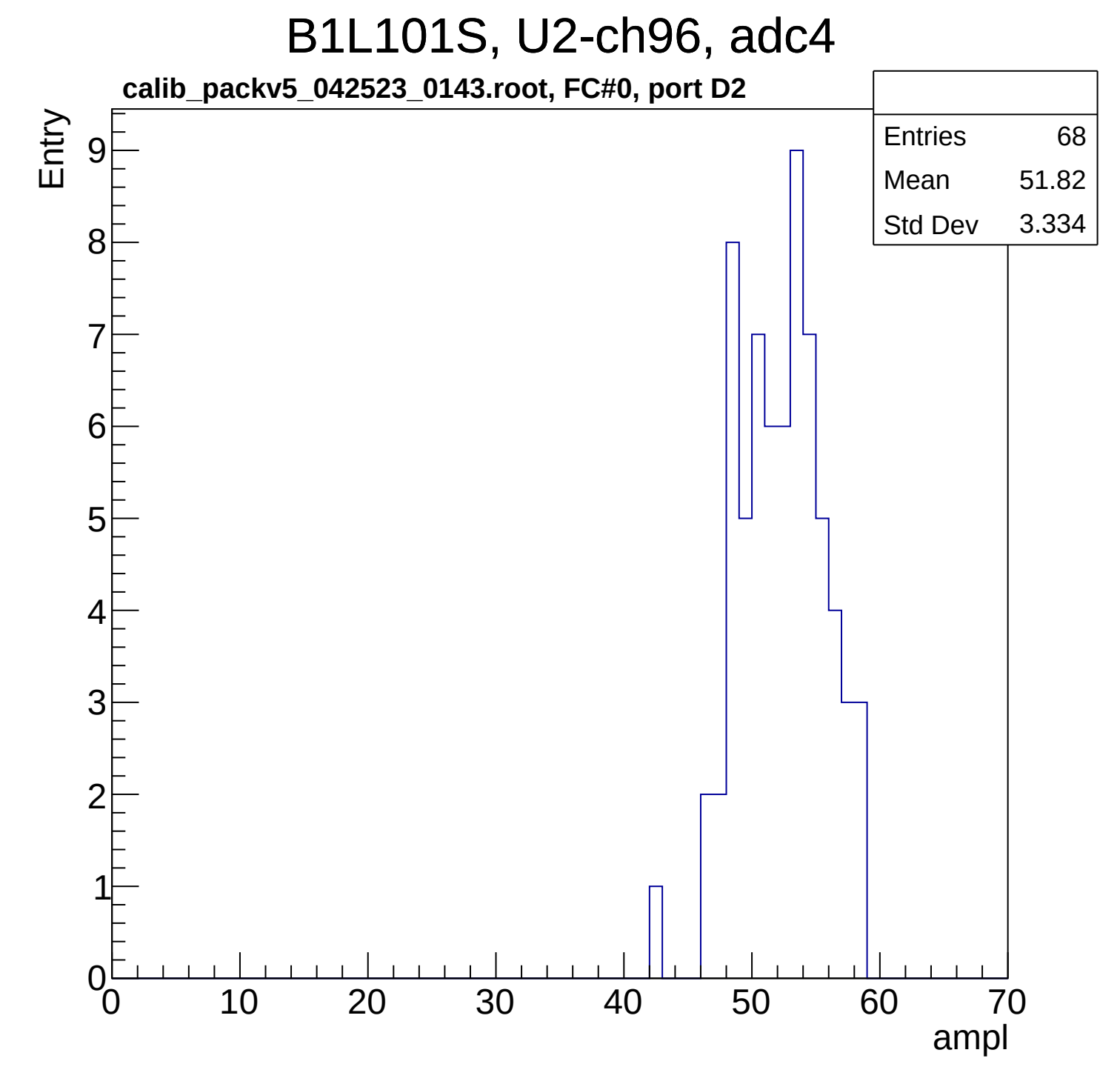

B1L101S, U2-ch95, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 29
Std Dev 25.96
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

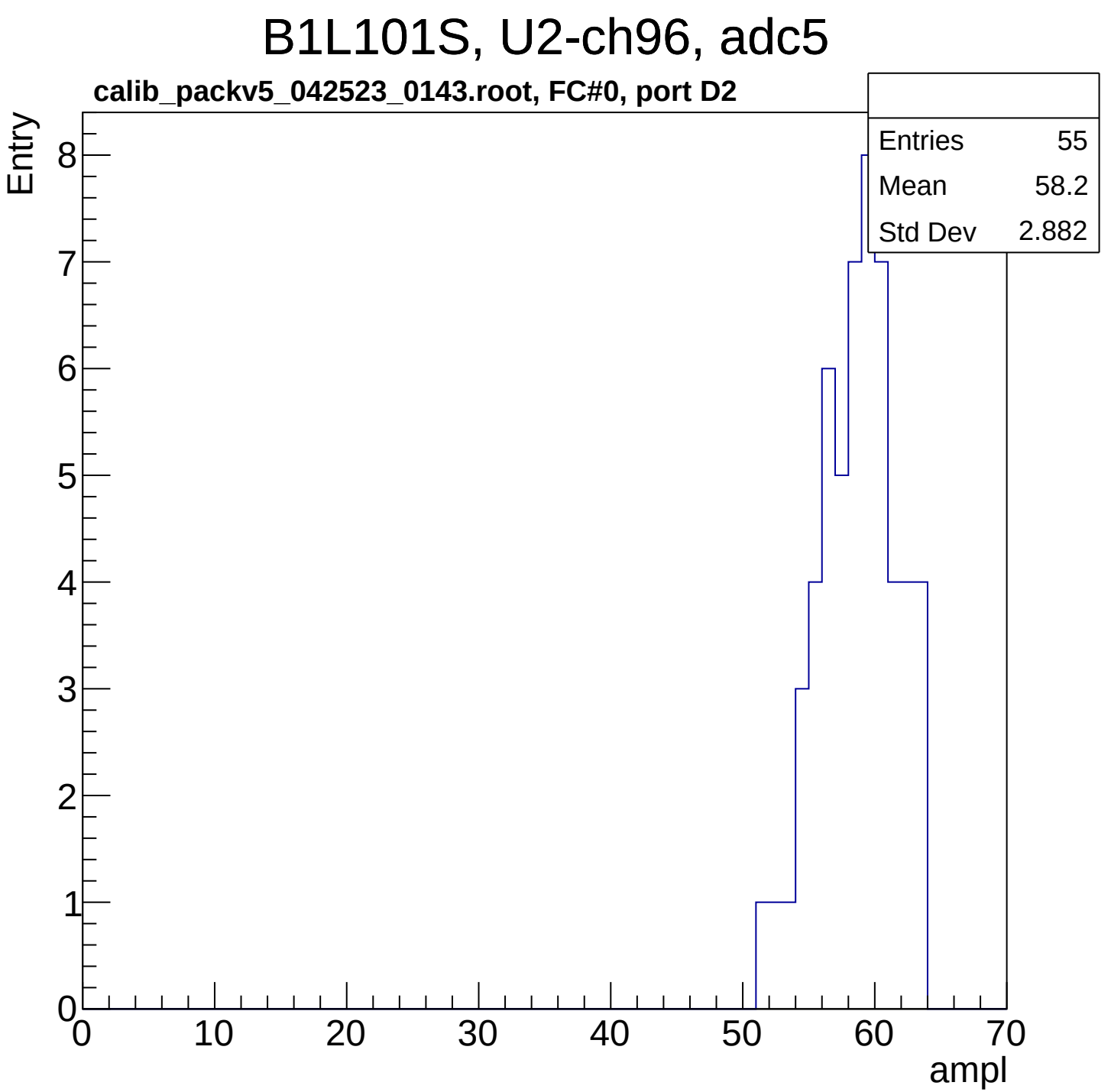

B1L101S, U2-ch96, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 27.71
Std Dev 5.028
Gaus mean : 27.9135
Gaus Width: 3.8132
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

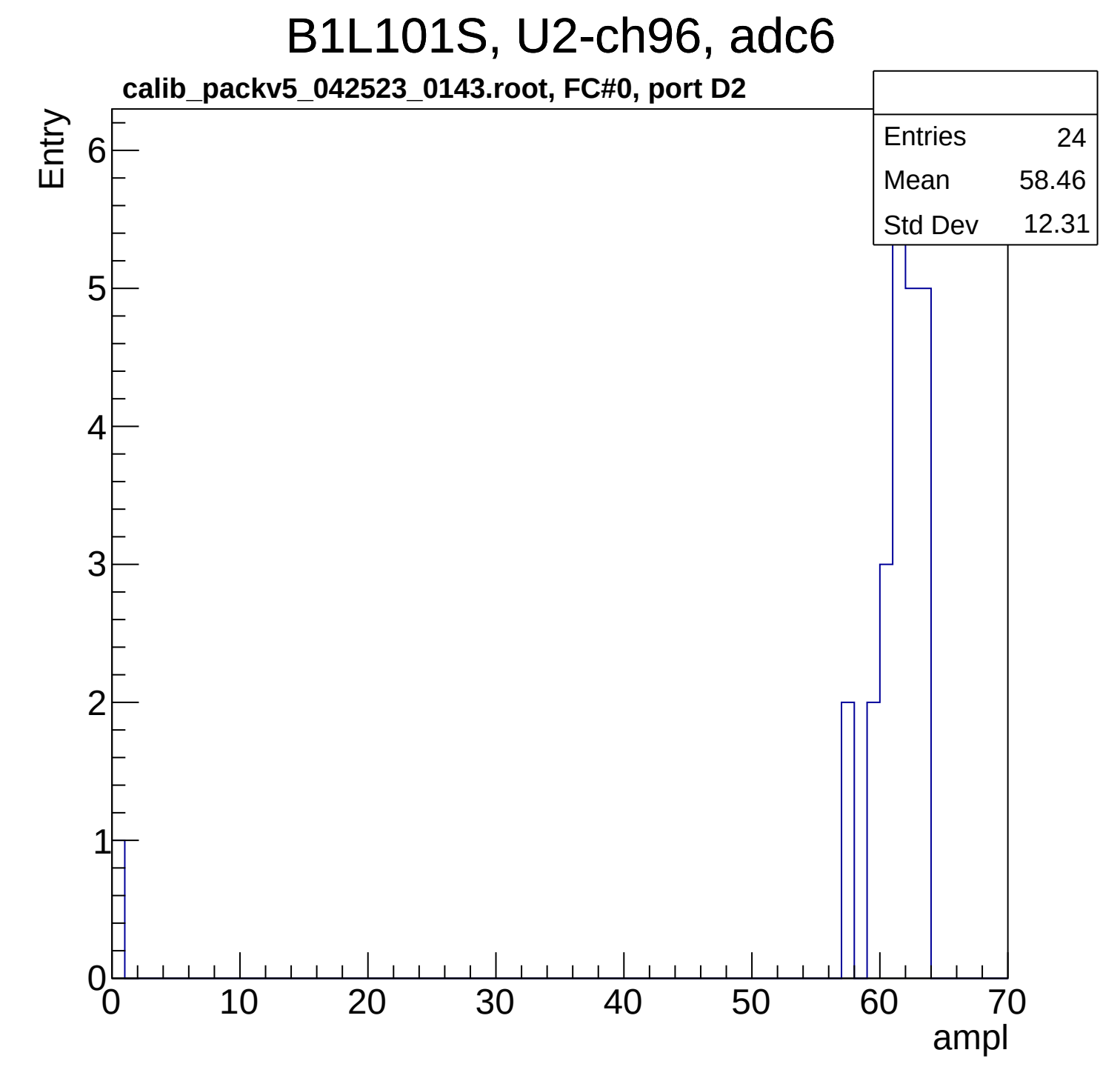

B1L101S, U2-ch96, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 33.5
Std Dev 3.5
Gaus mean : 33.7530
Gaus Width: 3.9571
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

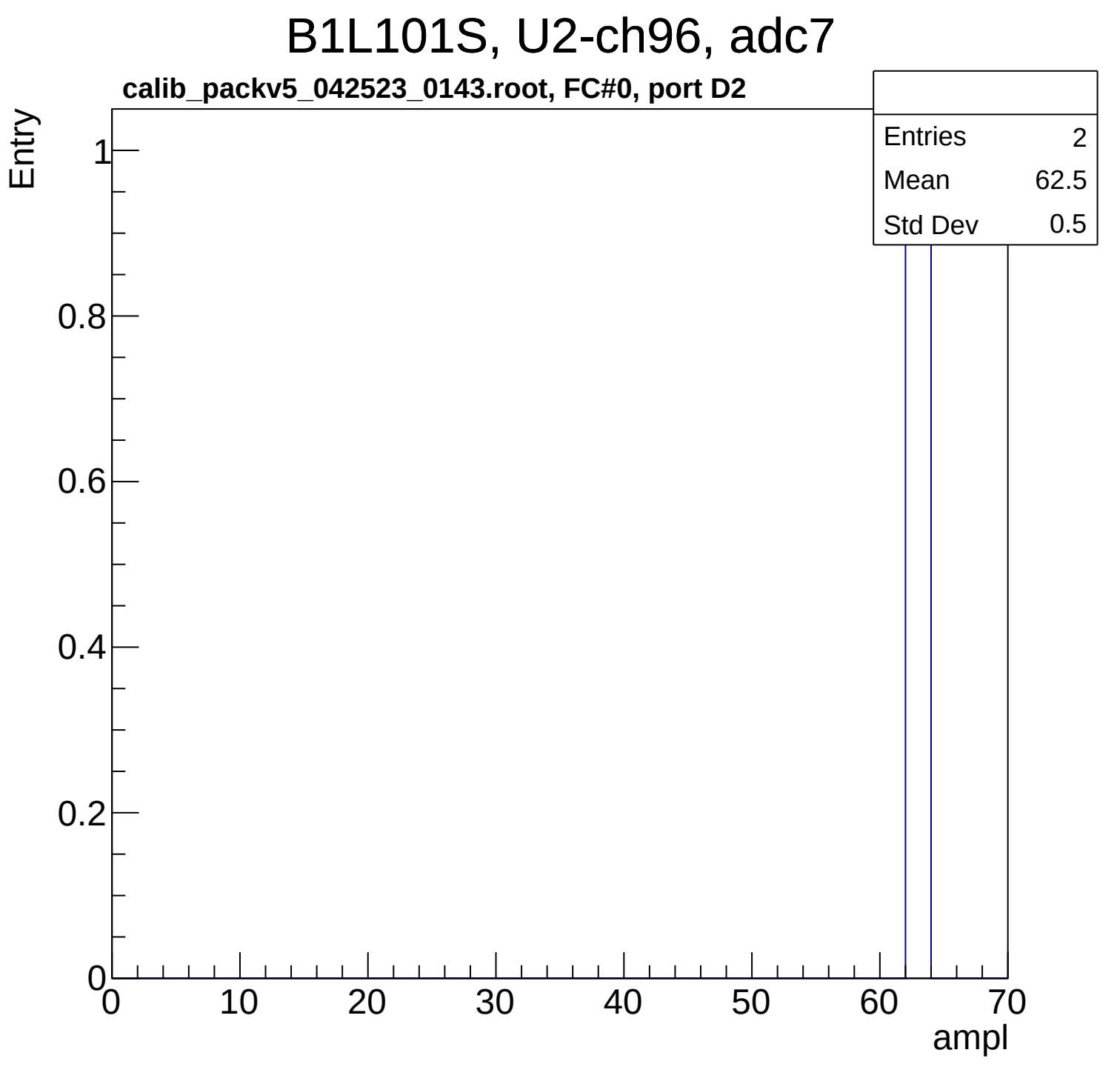

B1L101S, U2-ch96, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 39.87
Std Dev 4.118
Gaus mean : 41.0179
Gaus Width: 4.2977
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

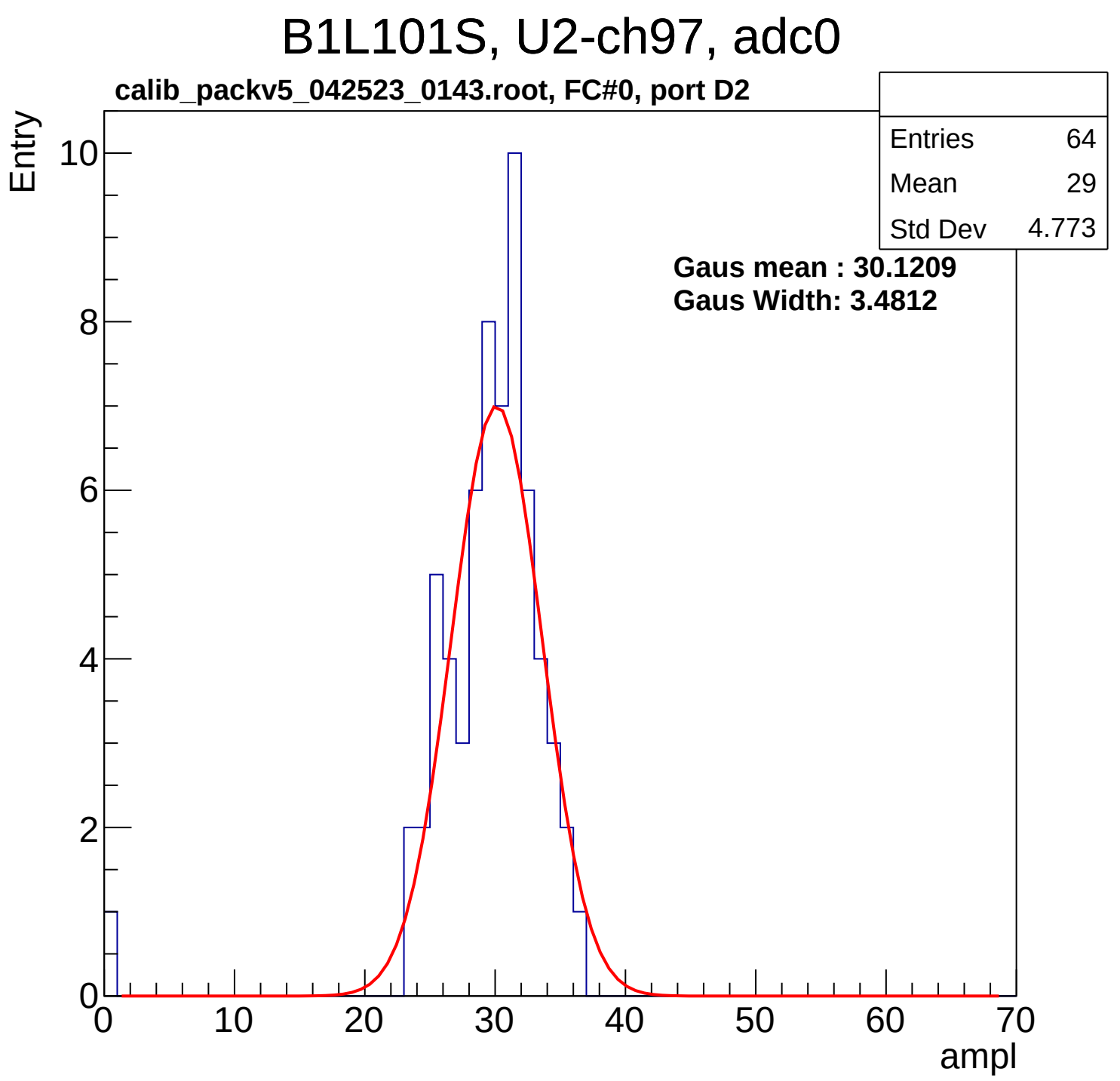

B1L101S, U2-ch96, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 45.69
Std Dev 3.662
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

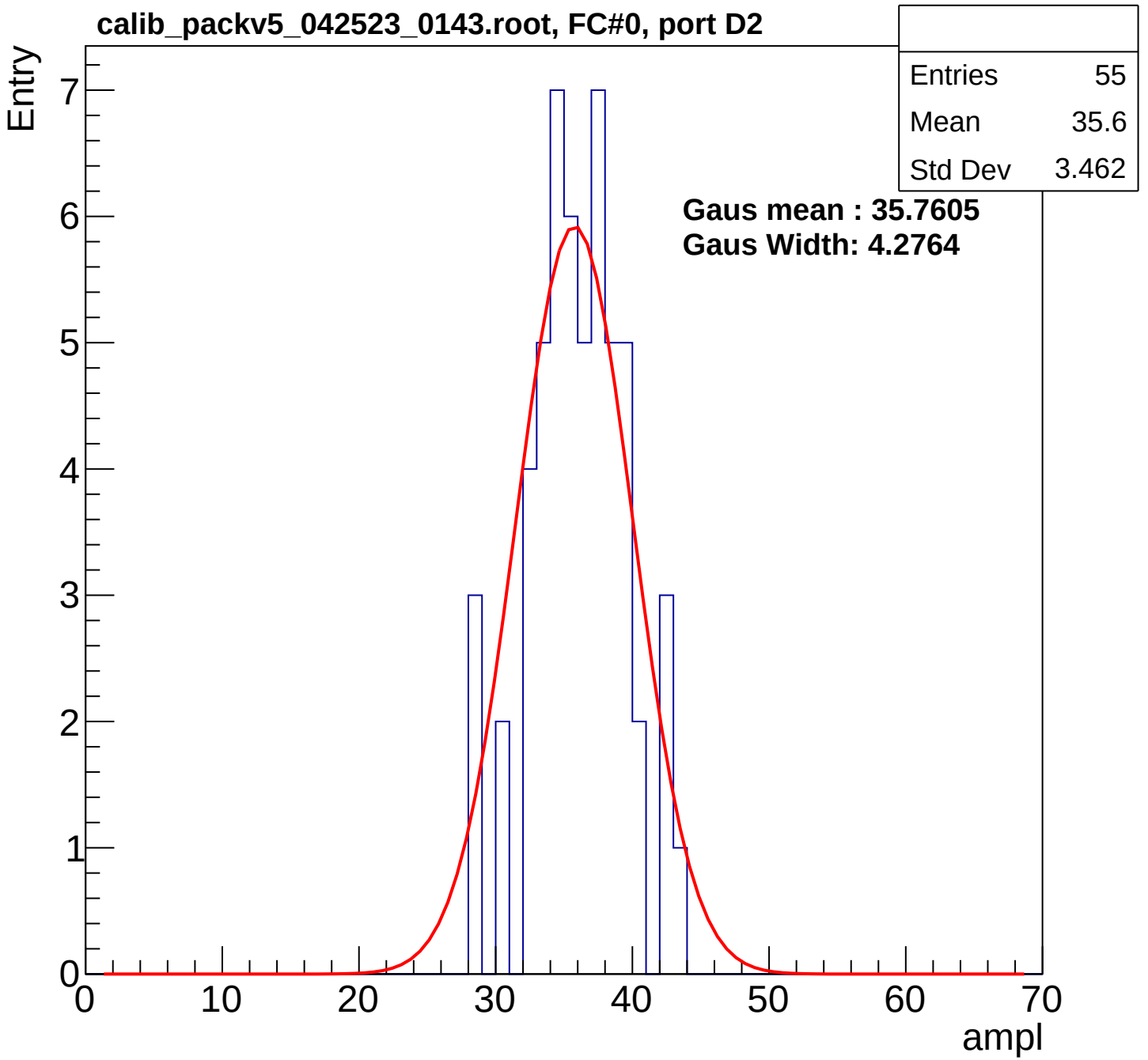

B1L101S, U2-ch96, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 51.82
Std Dev 3.334
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

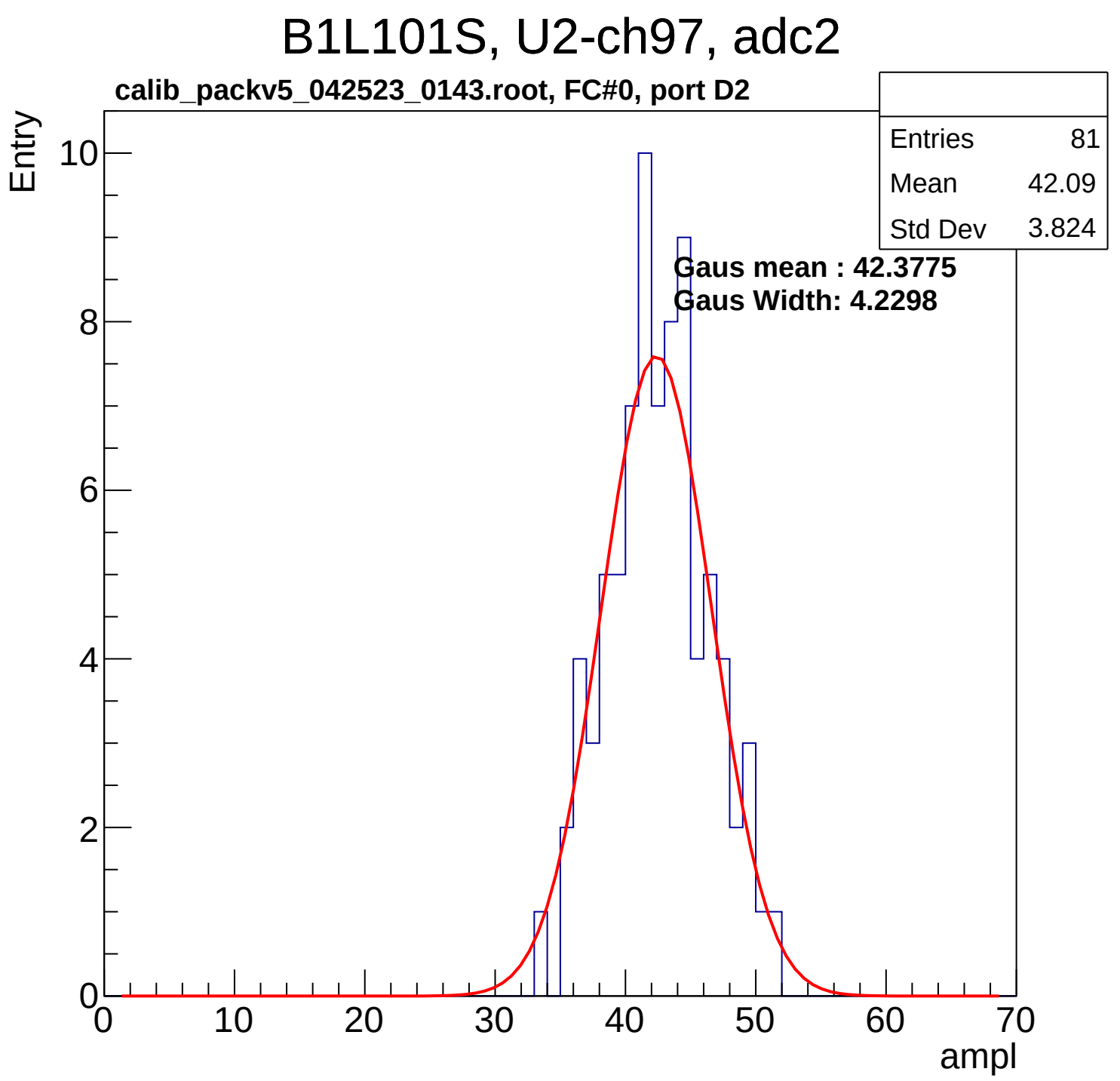

B1L101S, U2-ch96, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 58.2
Std Dev 2.882
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

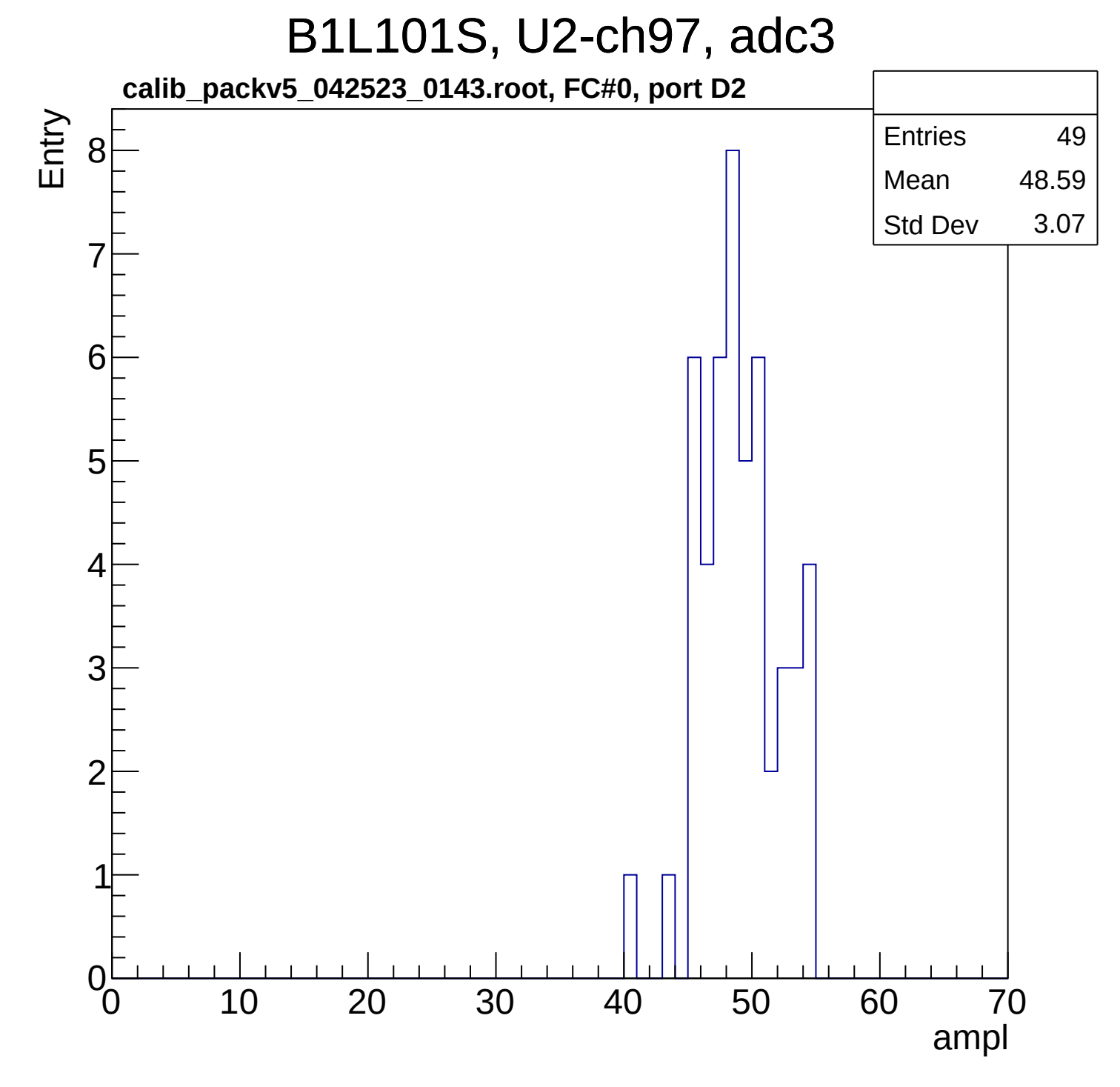

B1L101S, U2-ch96, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 24
Mean 58.46
Std Dev 12.31
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

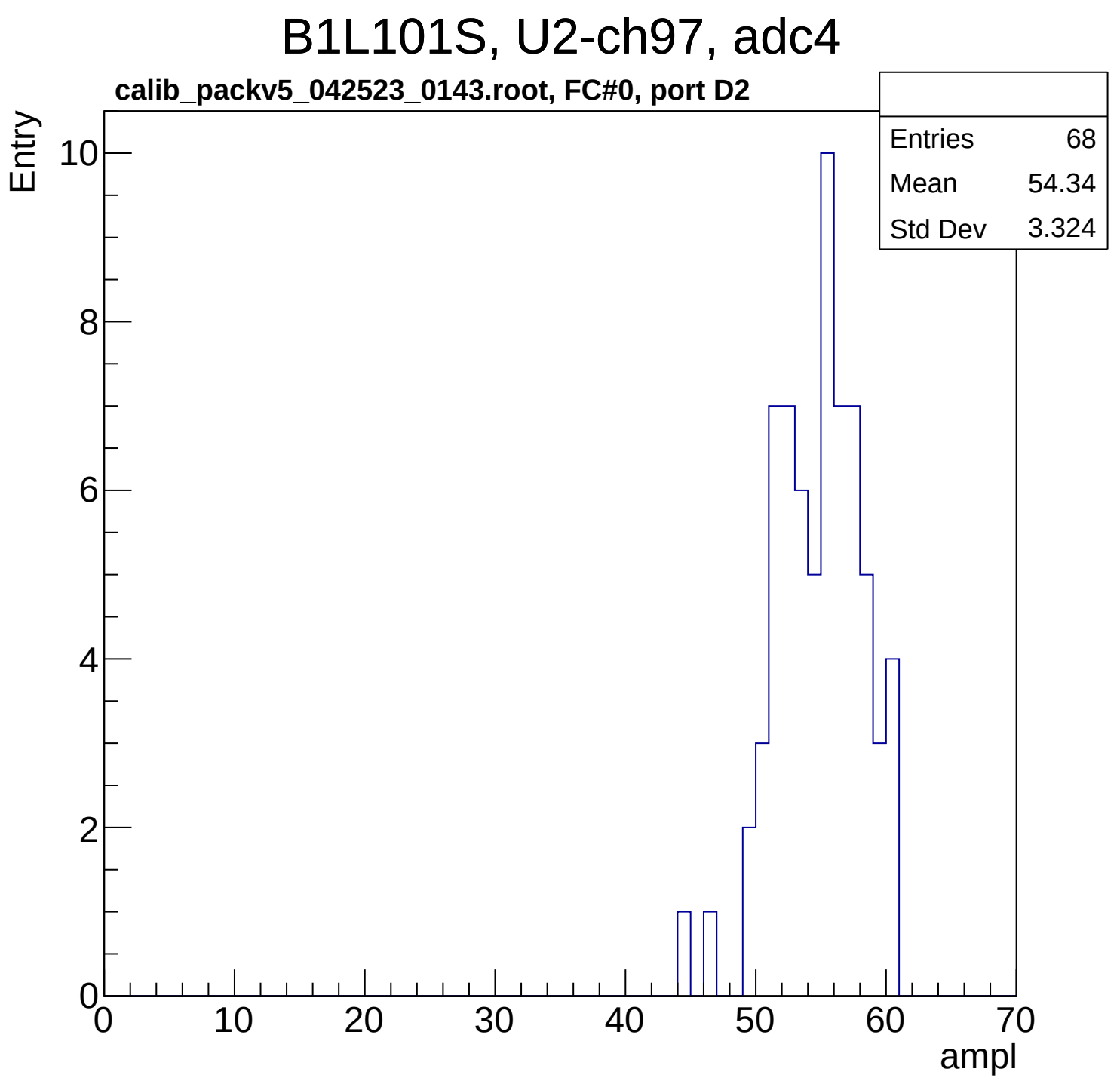

B1L101S, U2-ch96, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

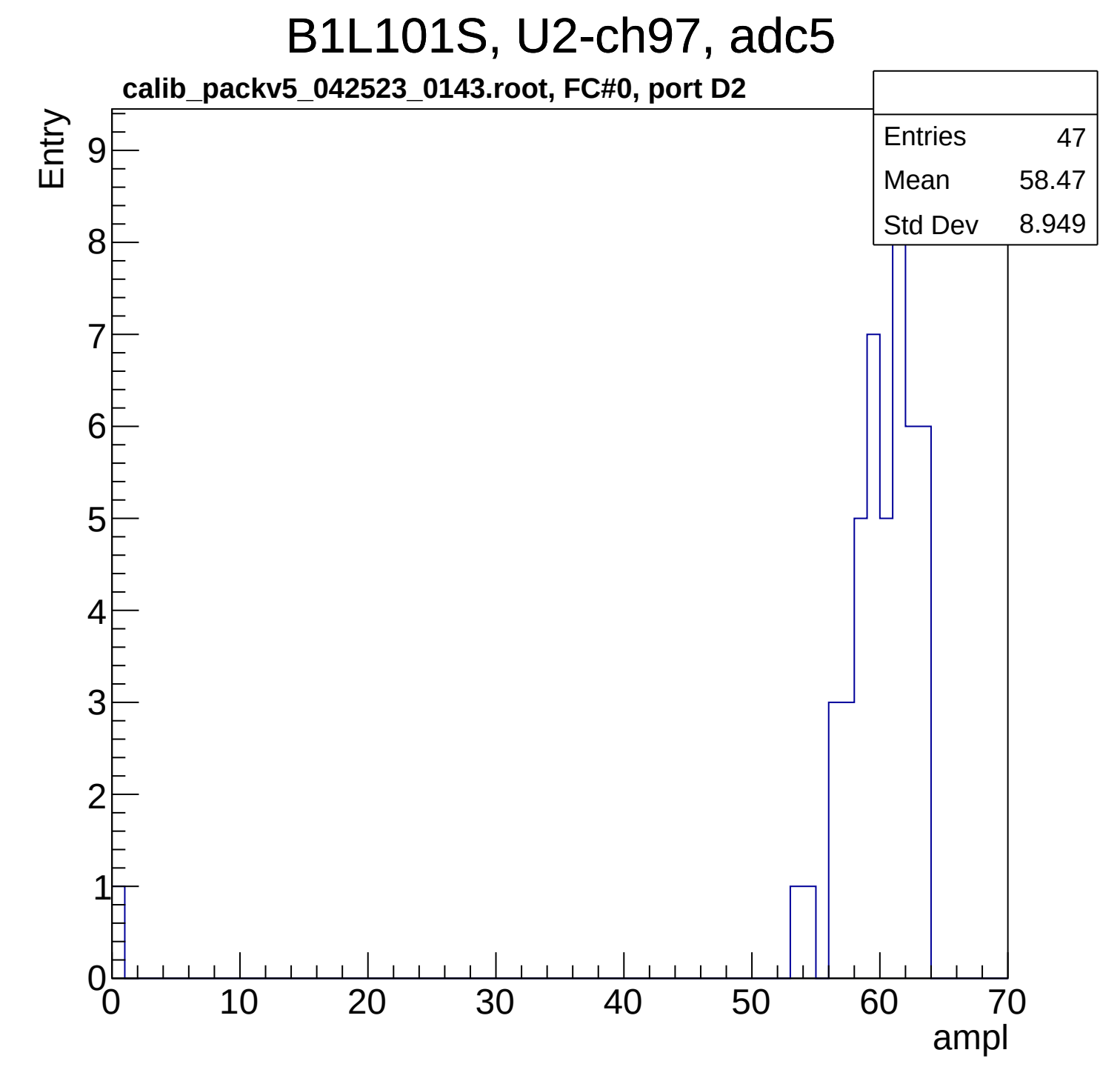

B1L101S, U2-ch97, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 29
Std Dev 4.773
Gaus mean : 30.1209
Gaus Width: 3.4812
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

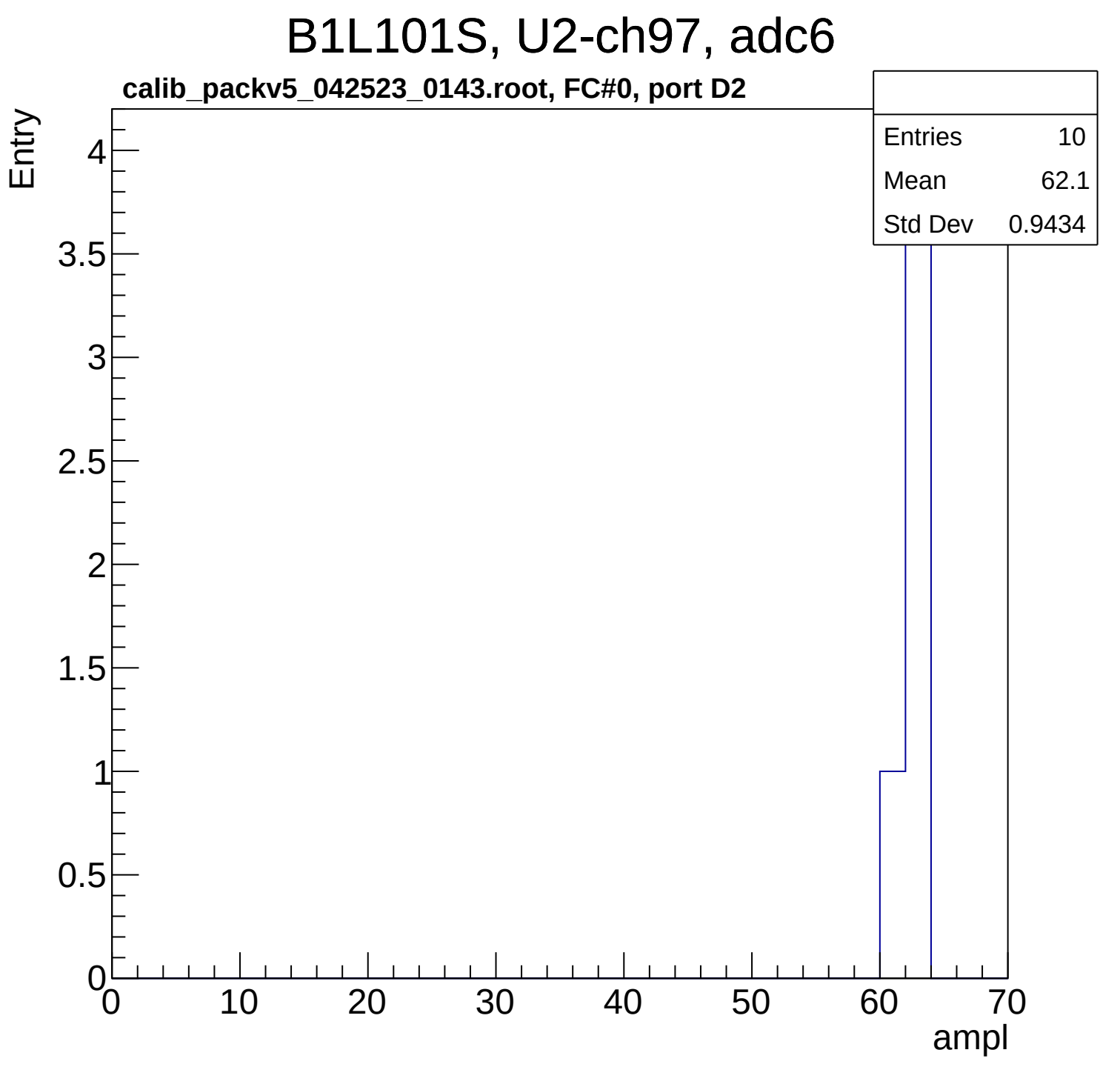

B1L101S, U2-ch97, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 35.6
Std Dev 3.462
Gaus mean : 35.7605
Gaus Width: 4.2764
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

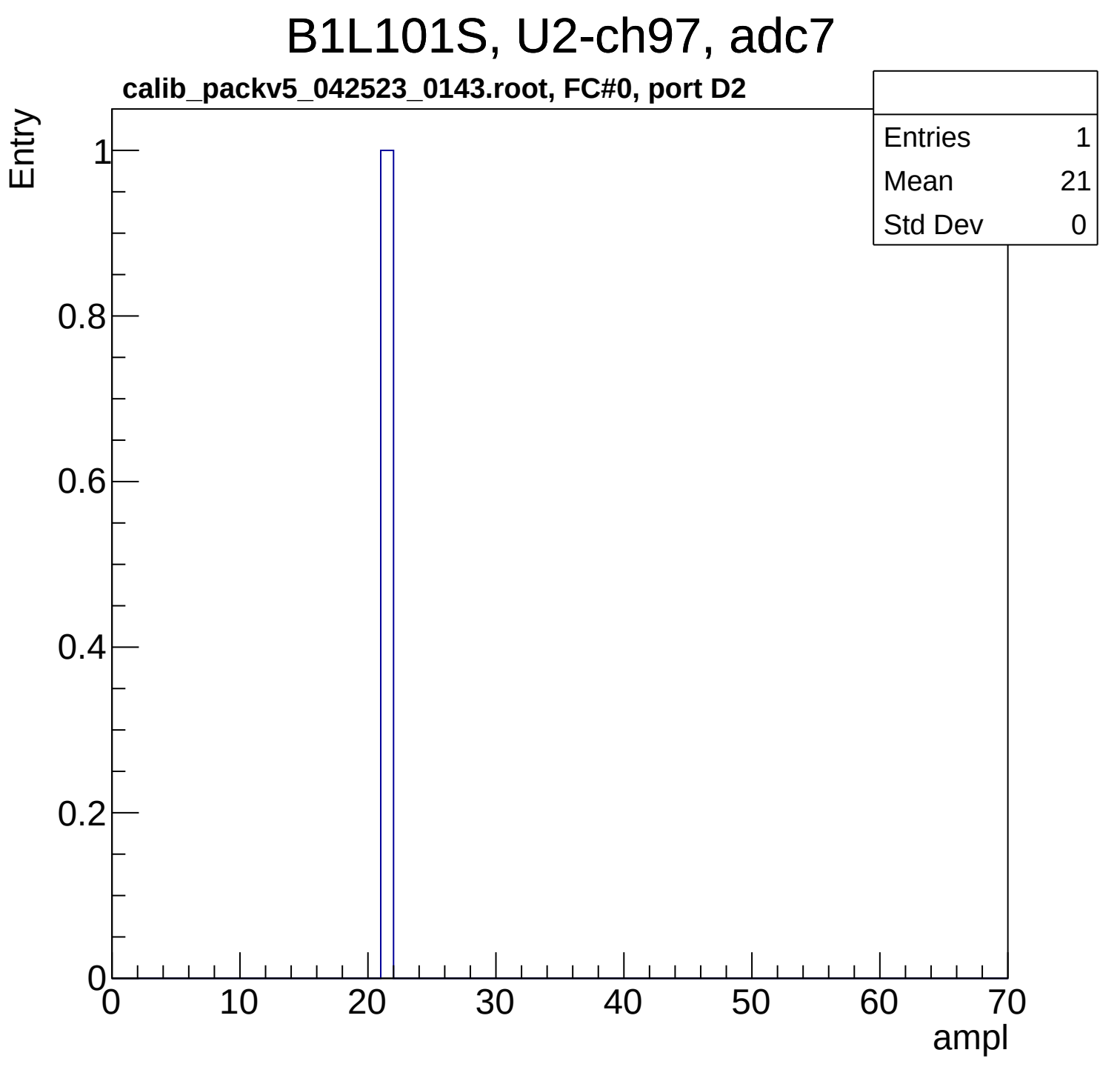

B1L101S, U2-ch97, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 81
Mean 42.09
Std Dev 3.824
Gaus mean : 42.3775
Gaus Width: 4.2298
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

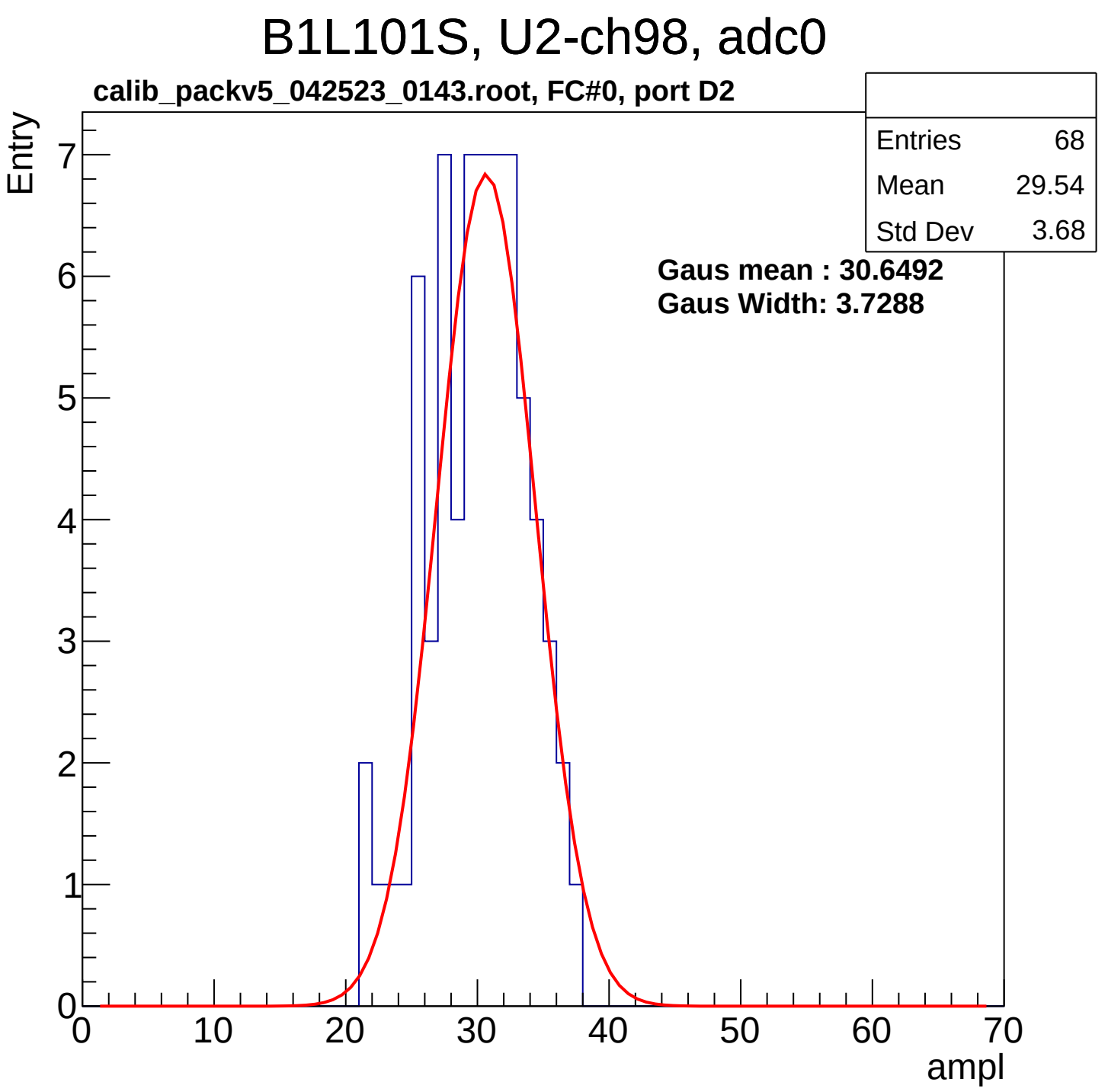

B1L101S, U2-ch97, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 48.59
Std Dev 3.07
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

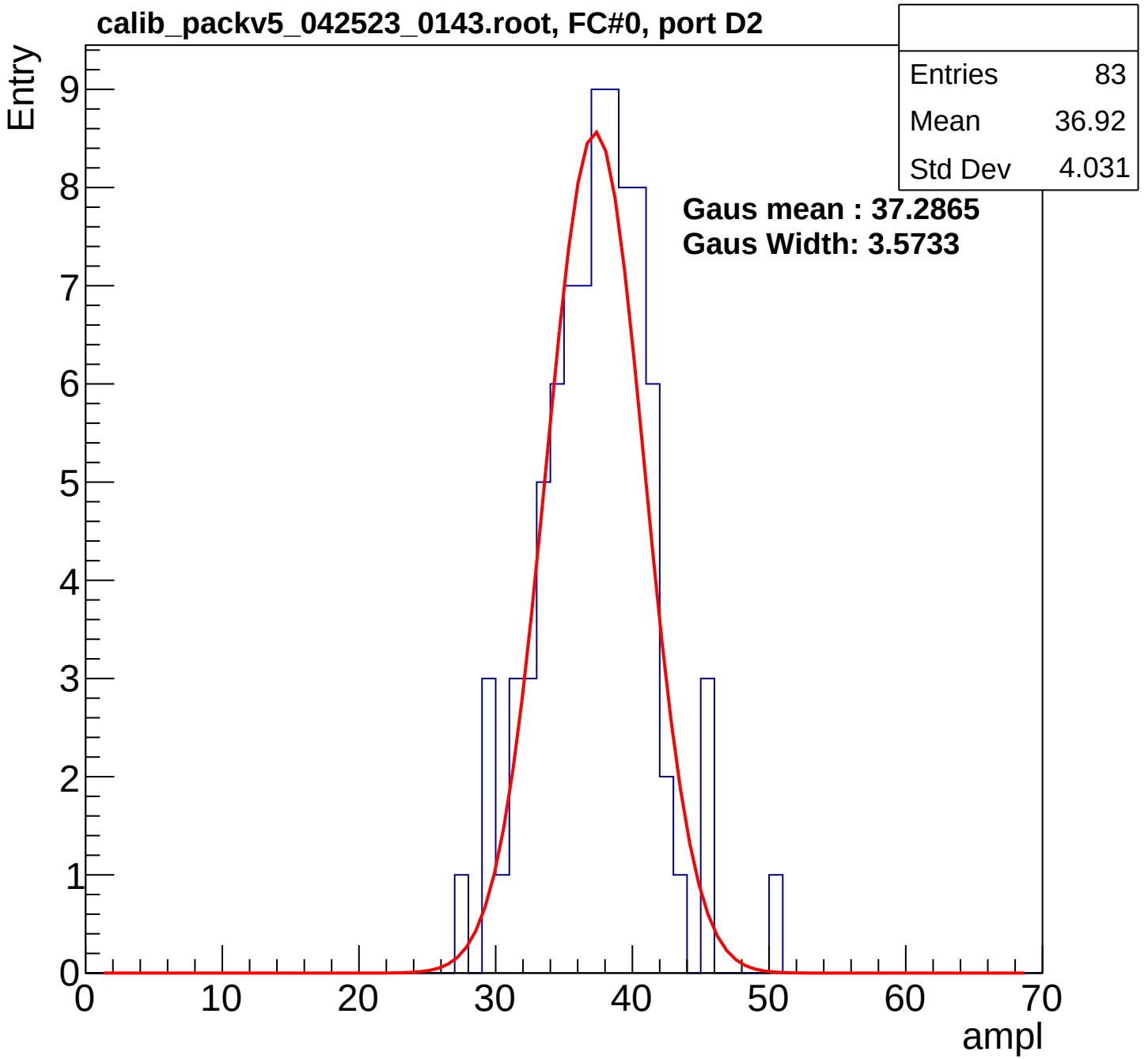

B1L101S, U2-ch97, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 54.34
Std Dev 3.324
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

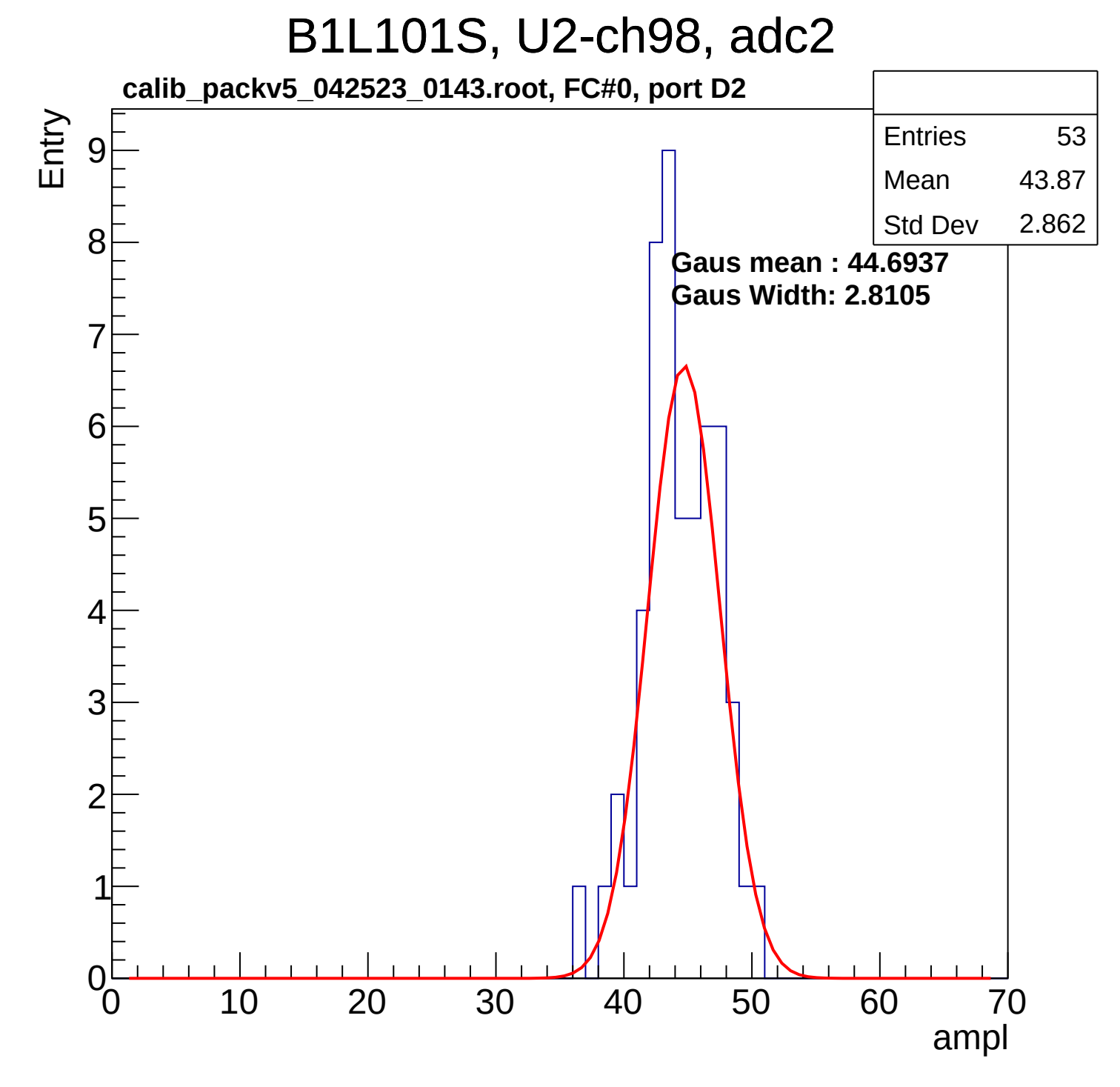

B1L101S, U2-ch97, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 58.47
Std Dev 8.949
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

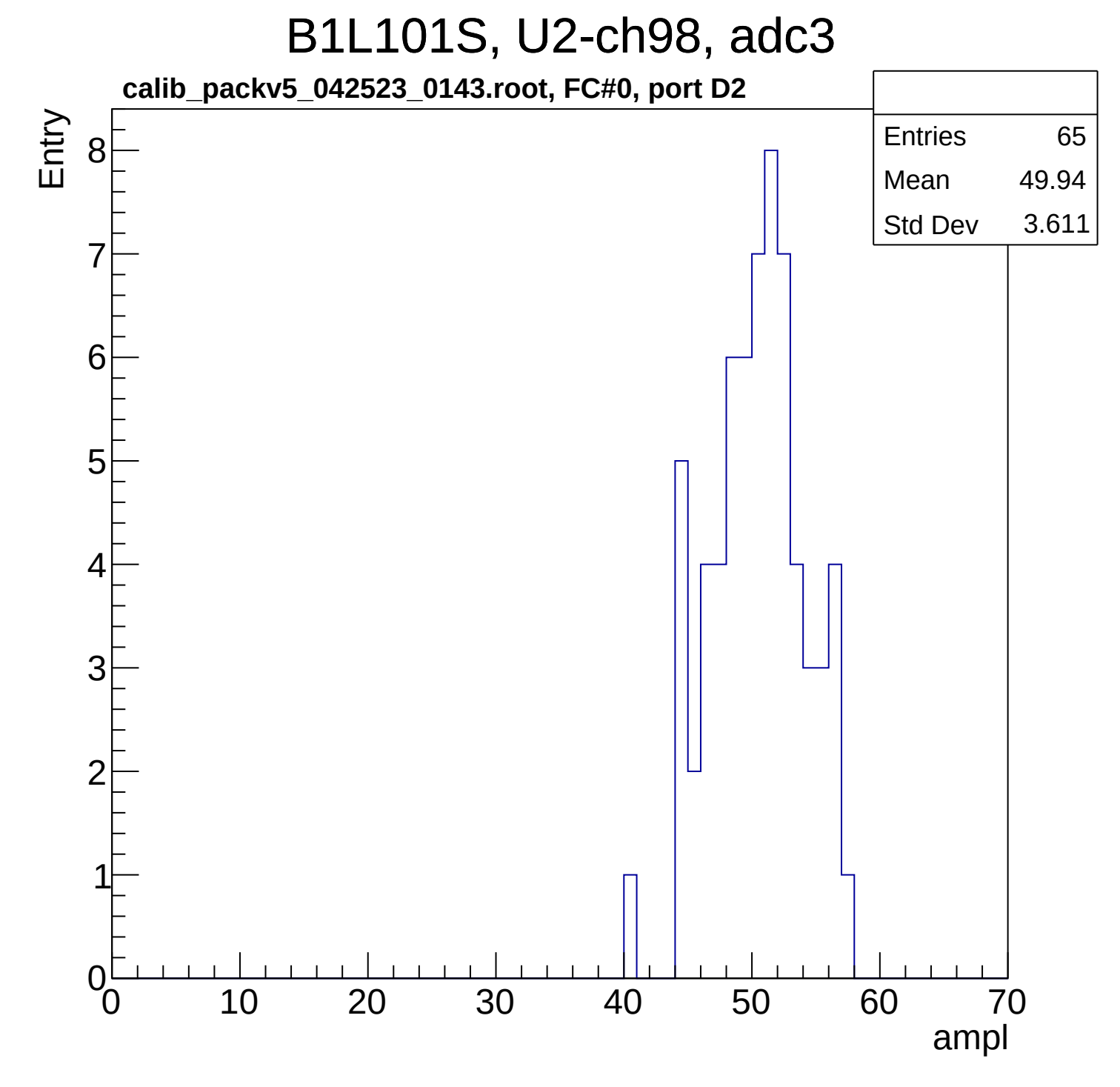

B1L101S, U2-ch97, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 62.1
Std Dev 0.9434
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

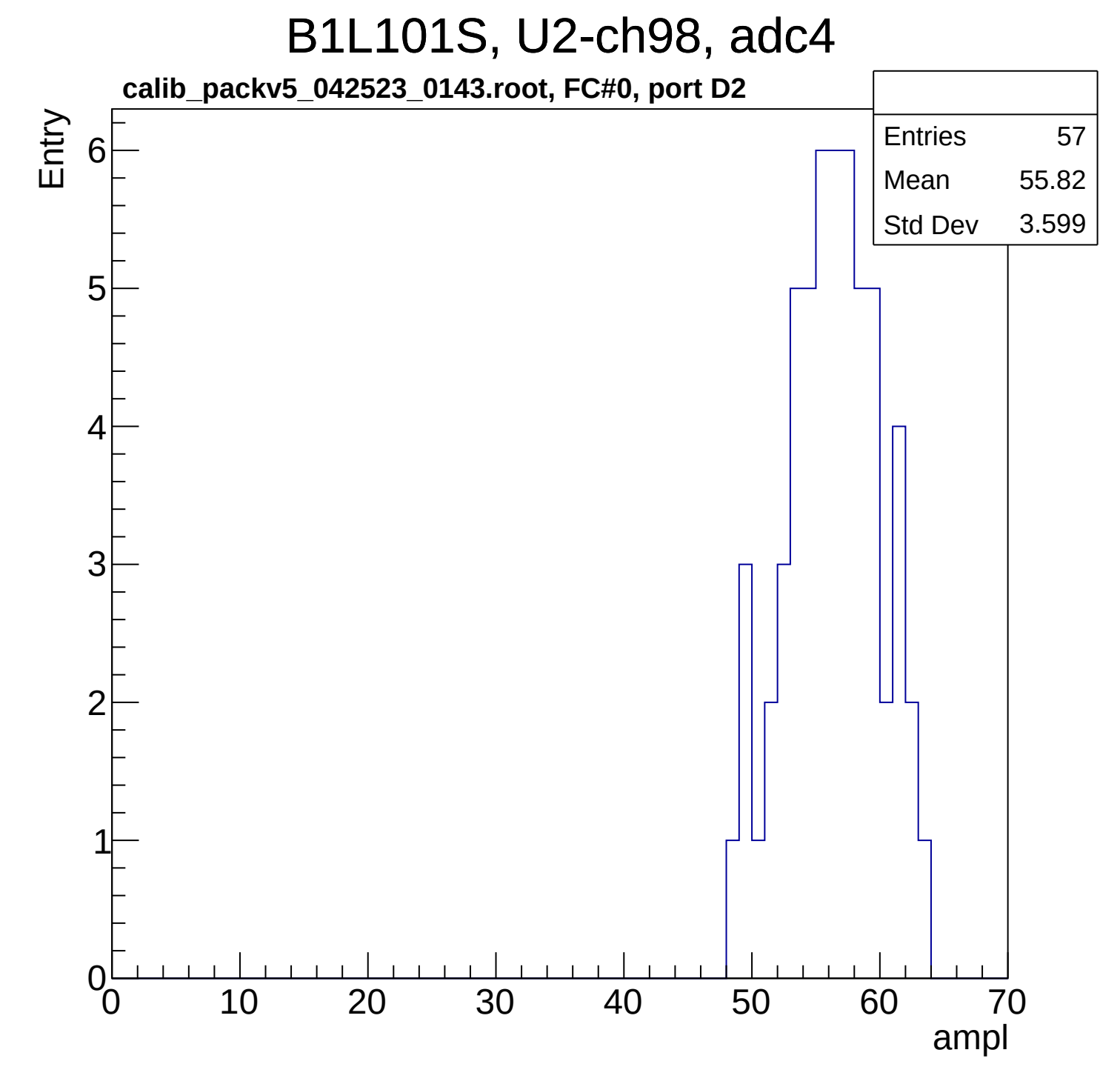

B1L101S, U2-ch97, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 21
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

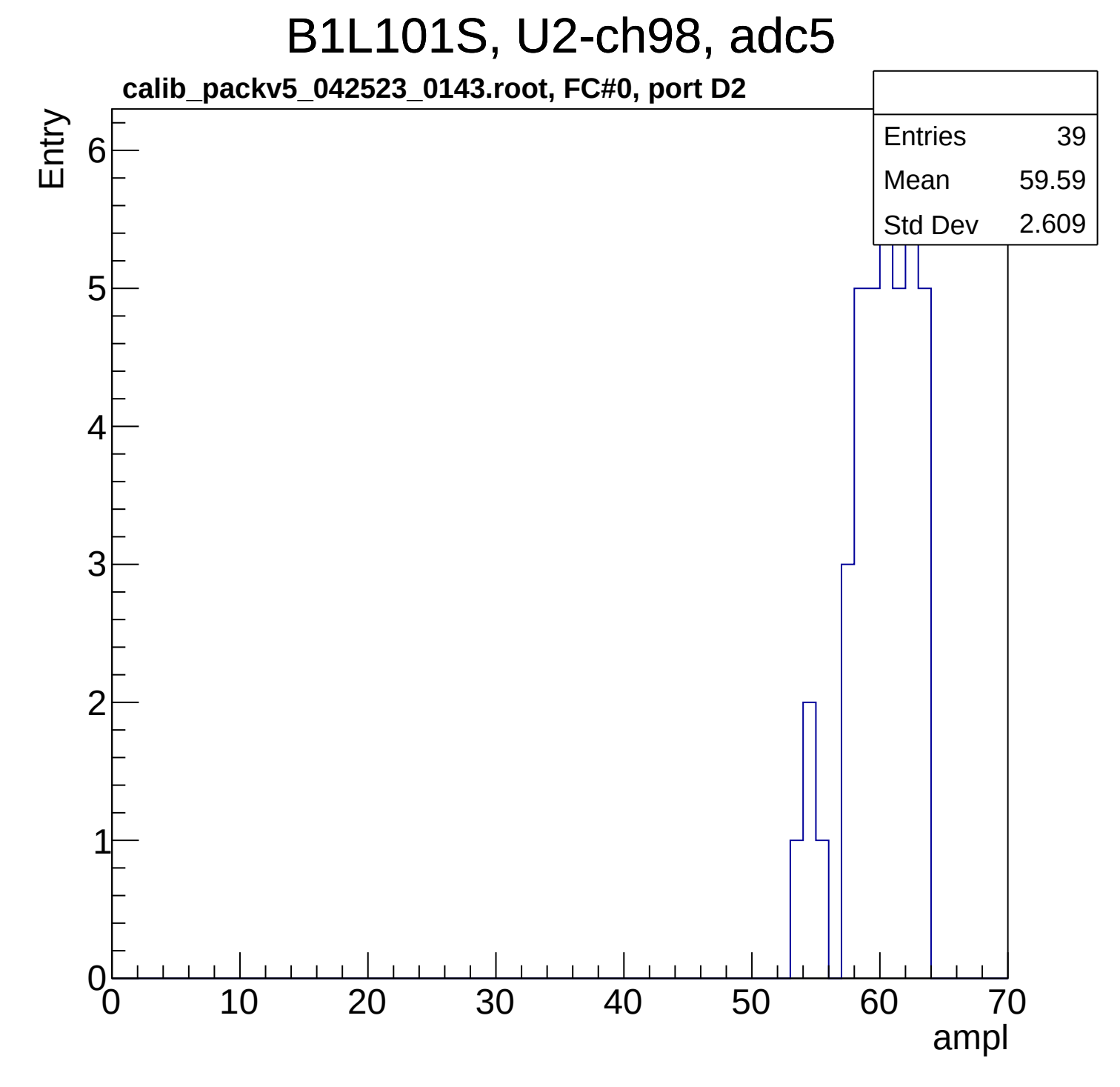

B1L101S, U2-ch98, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 29.54
Std Dev 3.68
Gaus mean : 30.6492
Gaus Width: 3.7288
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

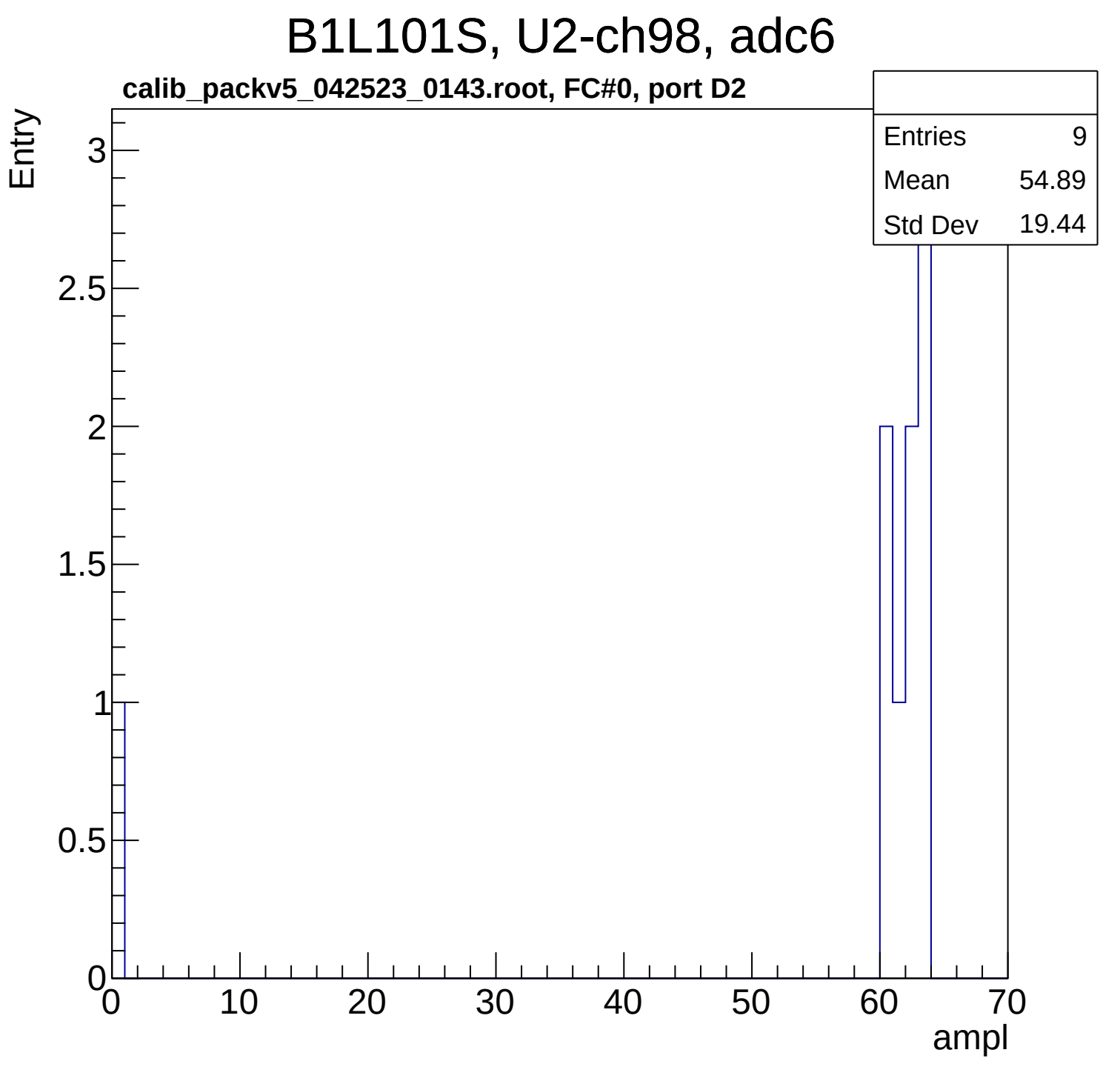

B1L101S, U2-ch98, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 83
Mean 36.92
Std Dev 4.031
Gaus mean : 37.2865
Gaus Width: 3.5733
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

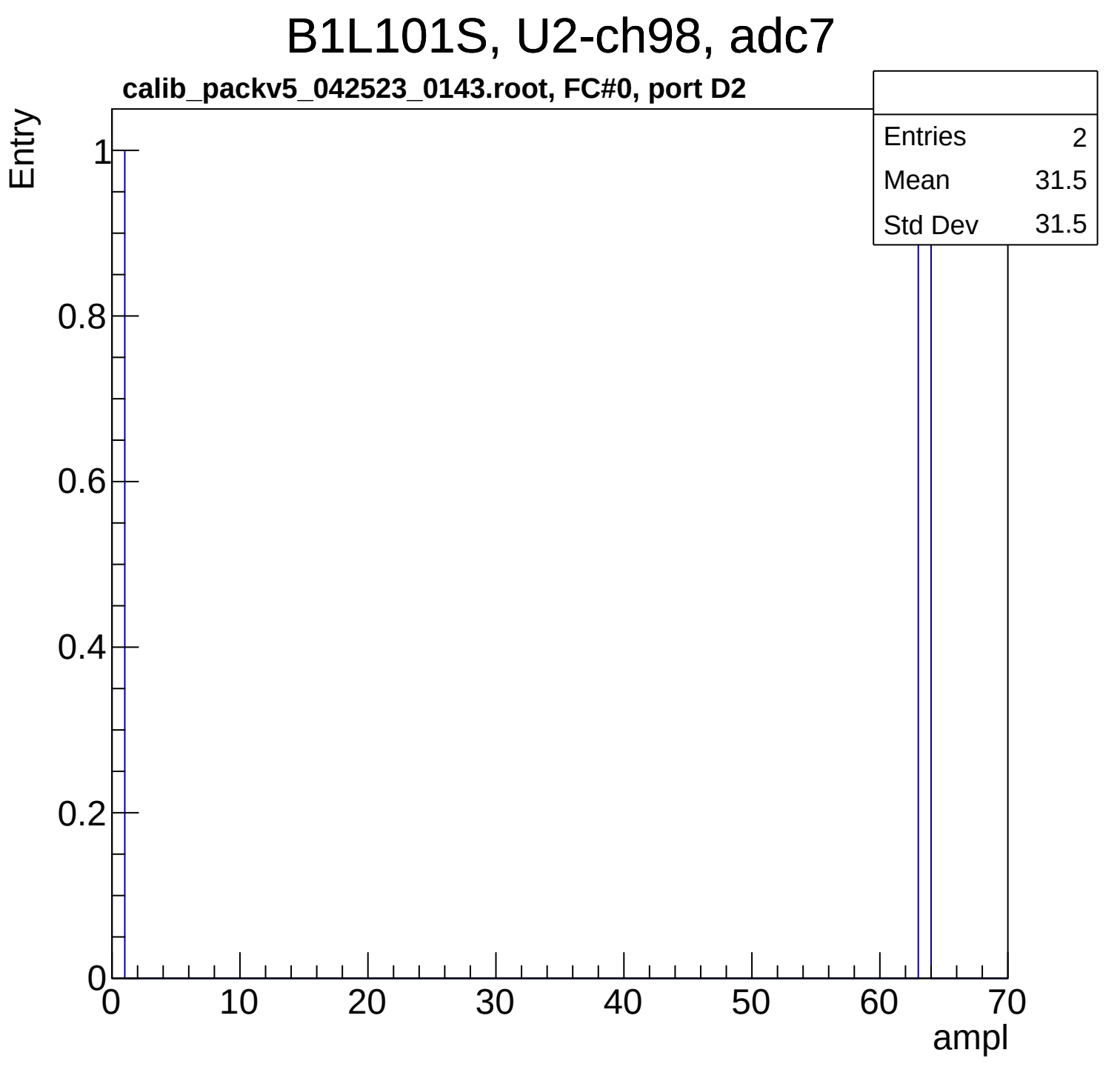

B1L101S, U2-ch98, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 43.87
Std Dev 2.862
Gaus mean : 44.6937
Gaus Width: 2.8105
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

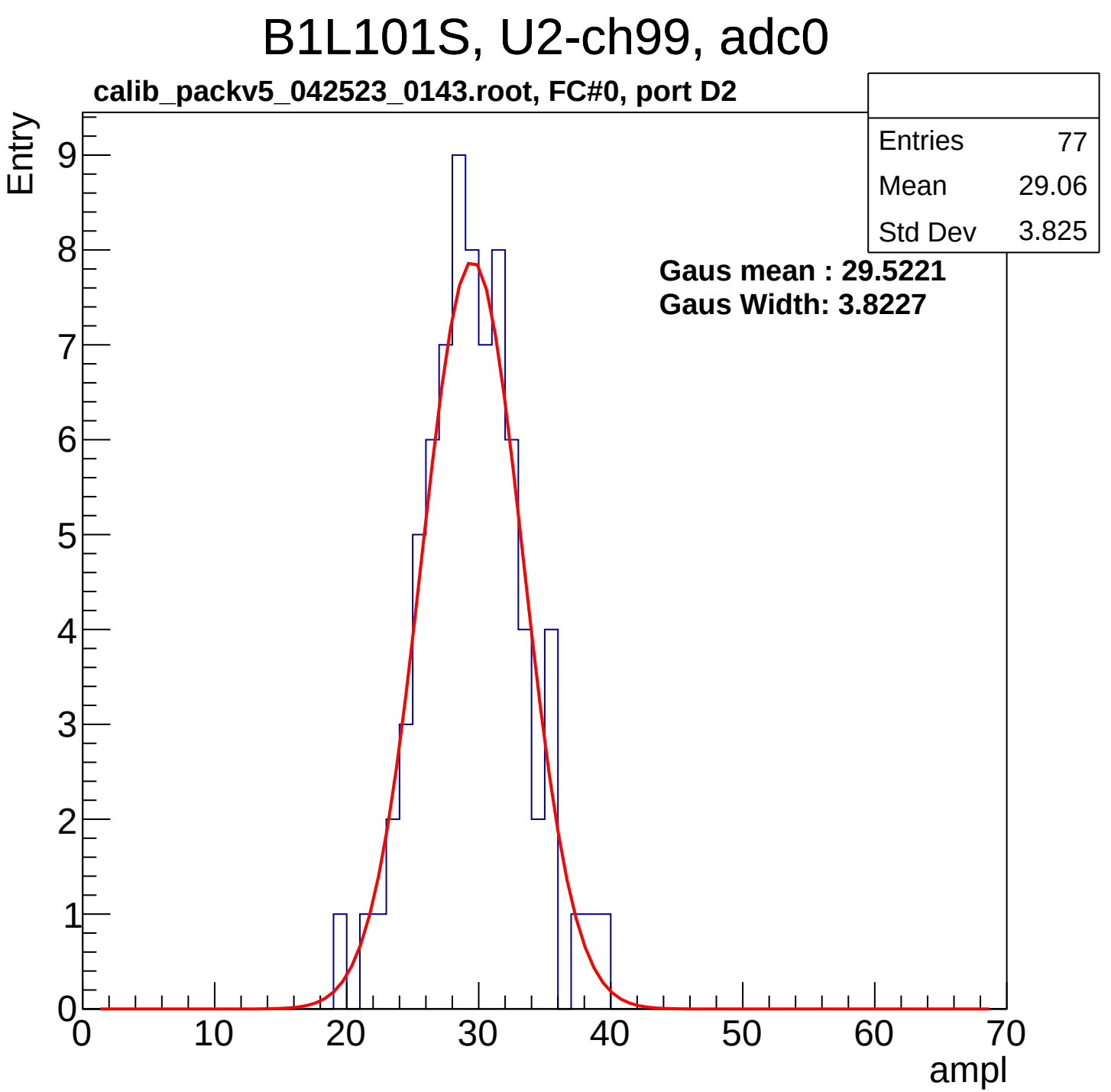

B1L101S, U2-ch98, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 49.94
Std Dev 3.611
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

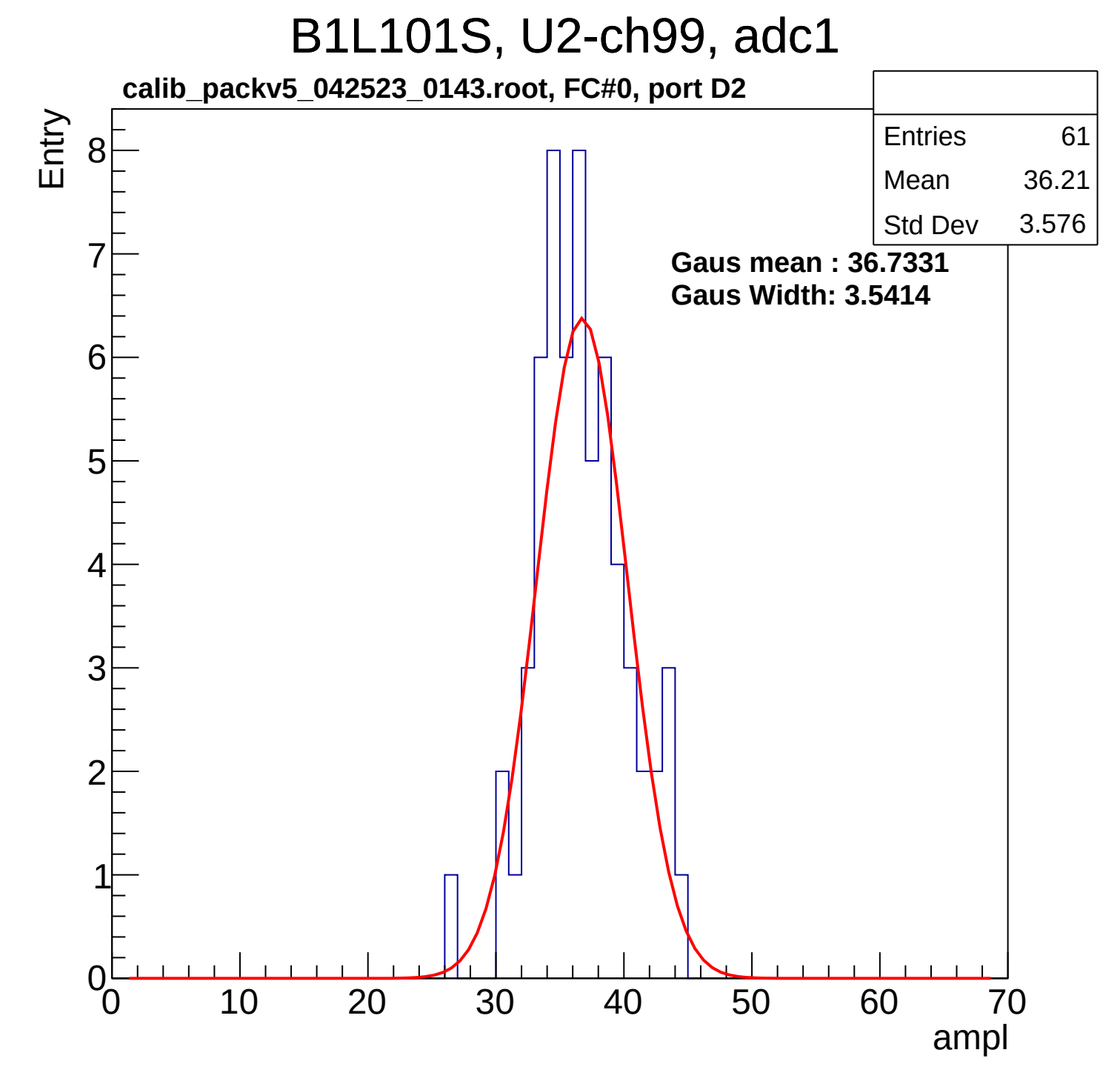

B1L101S, U2-ch98, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 55.82
Std Dev 3.599
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

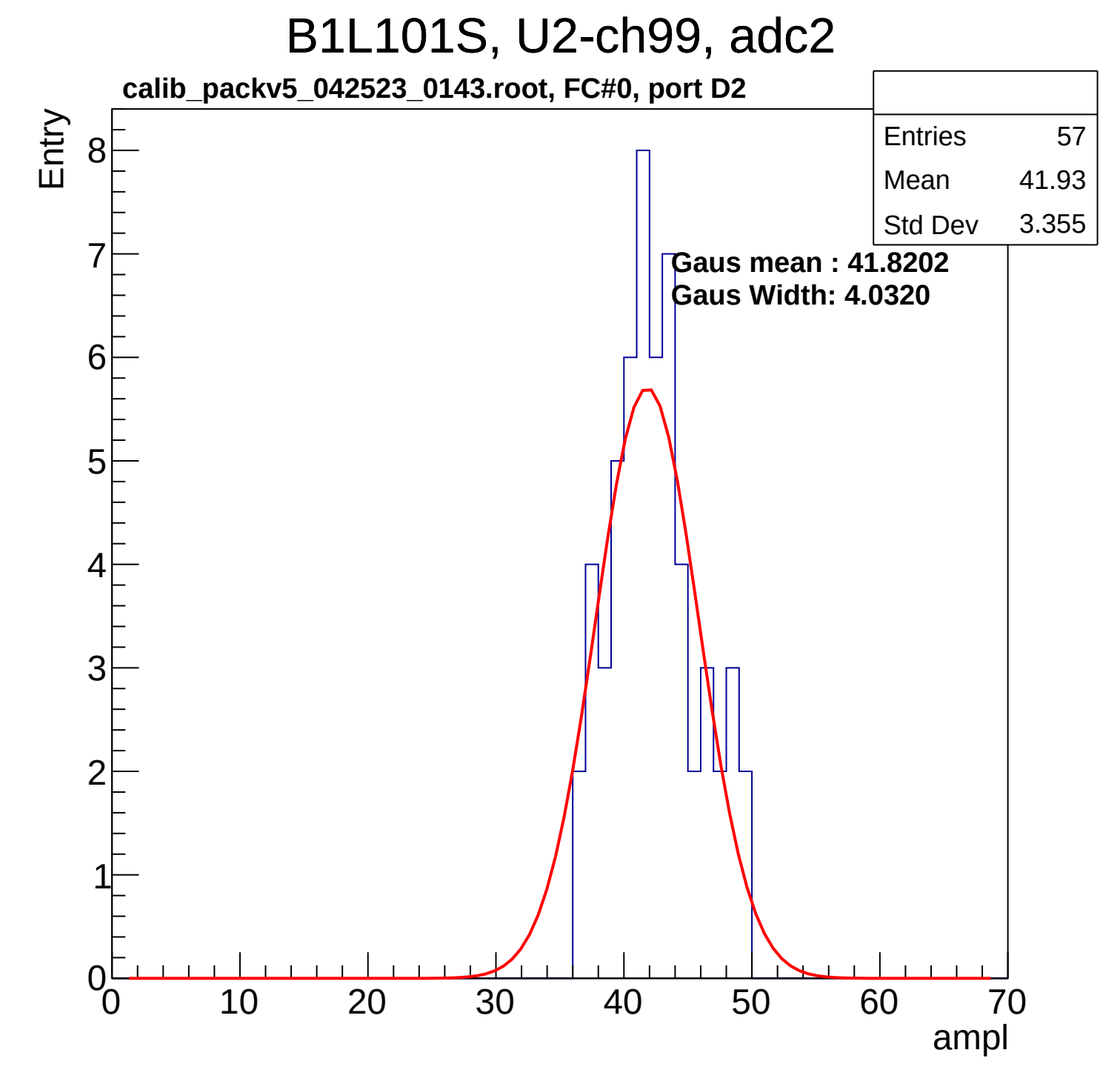

B1L101S, U2-ch98, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 39
Mean 59.59
Std Dev 2.609
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

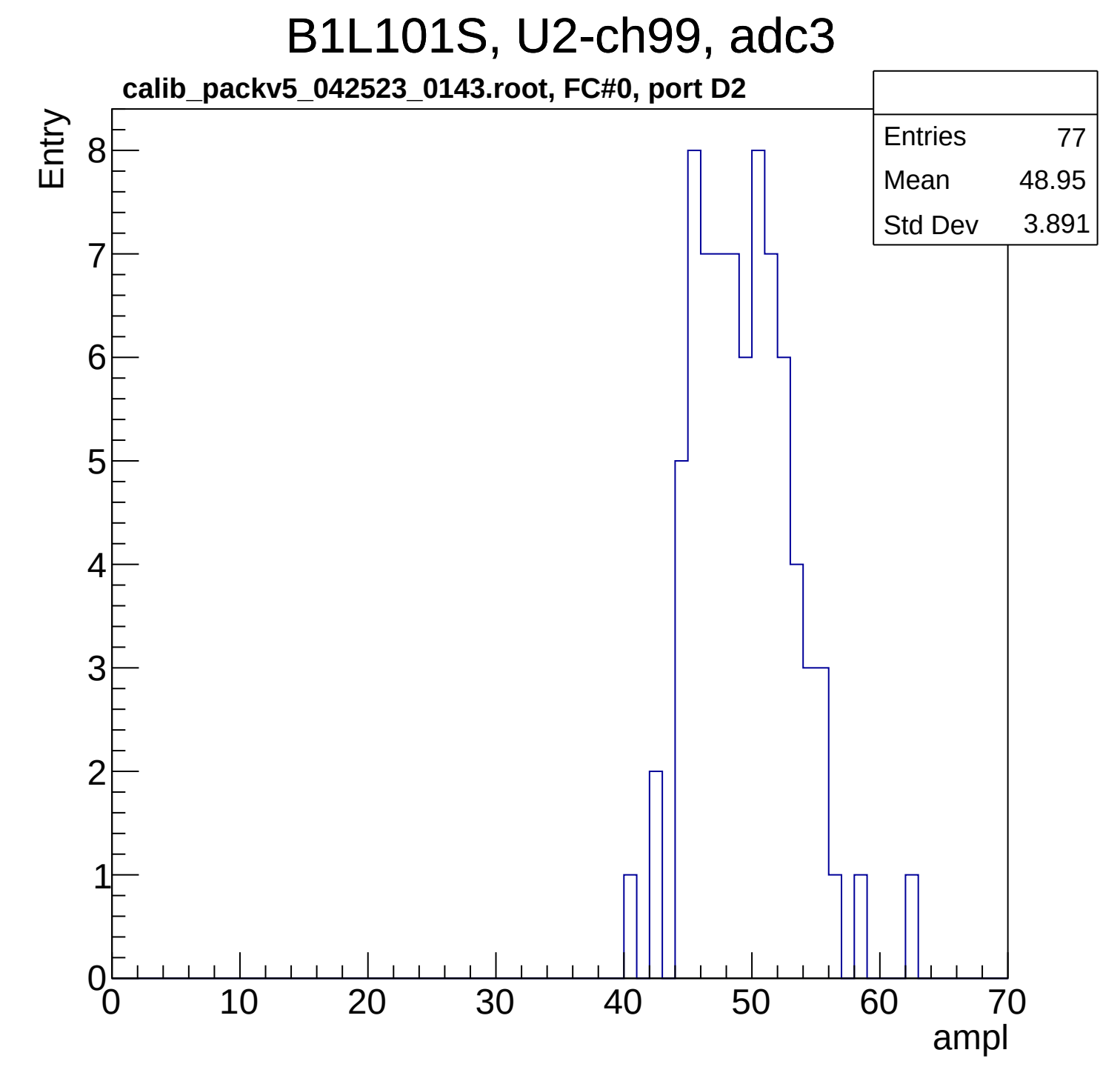

B1L101S, U2-ch98, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 54.89
Std Dev 19.44
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

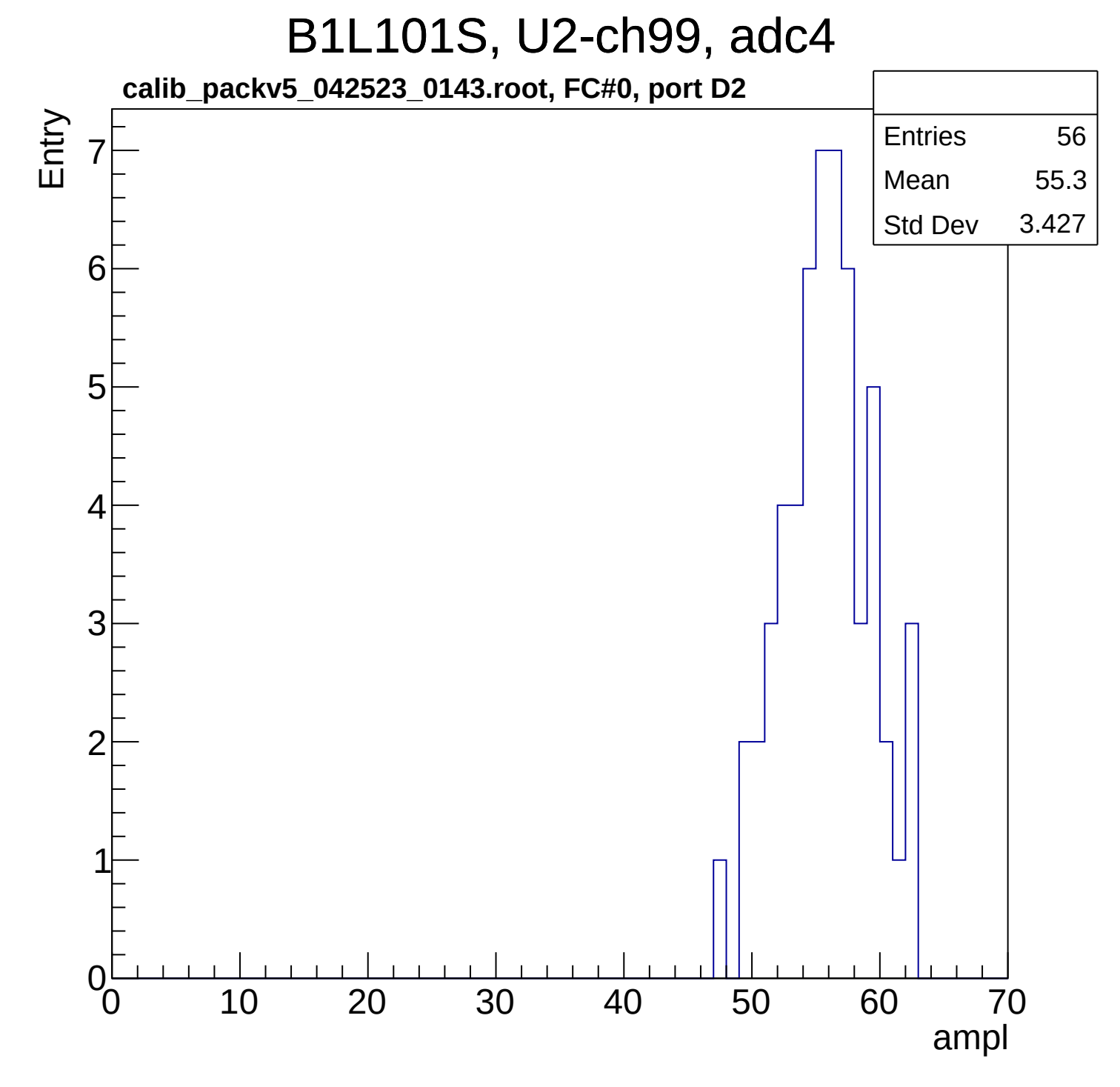

B1L101S, U2-ch98, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

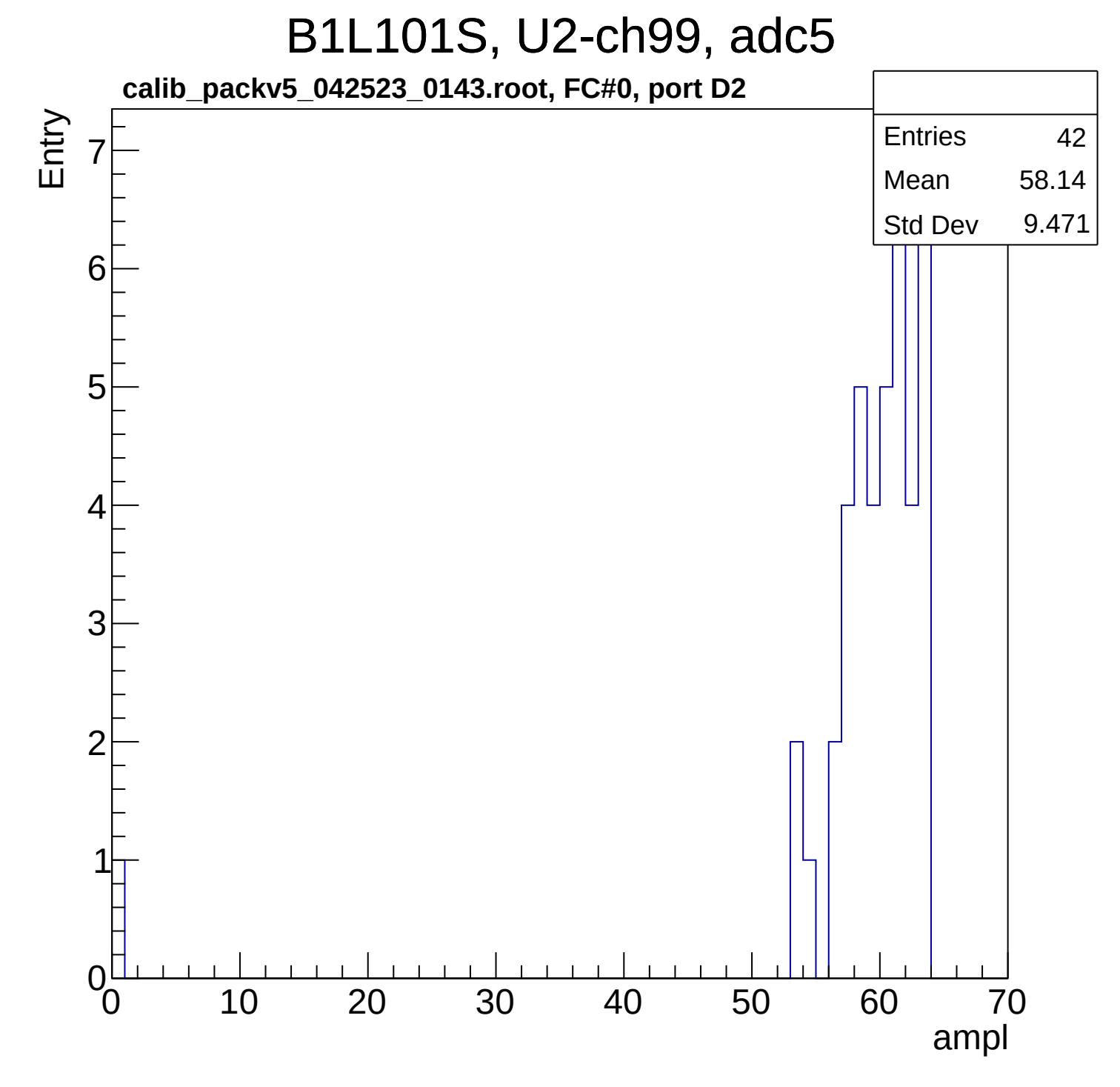

B1L101S, U2-ch99, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 29.06
Std Dev 3.825
Gaus mean : 29.5221
Gaus Width: 3.8227
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

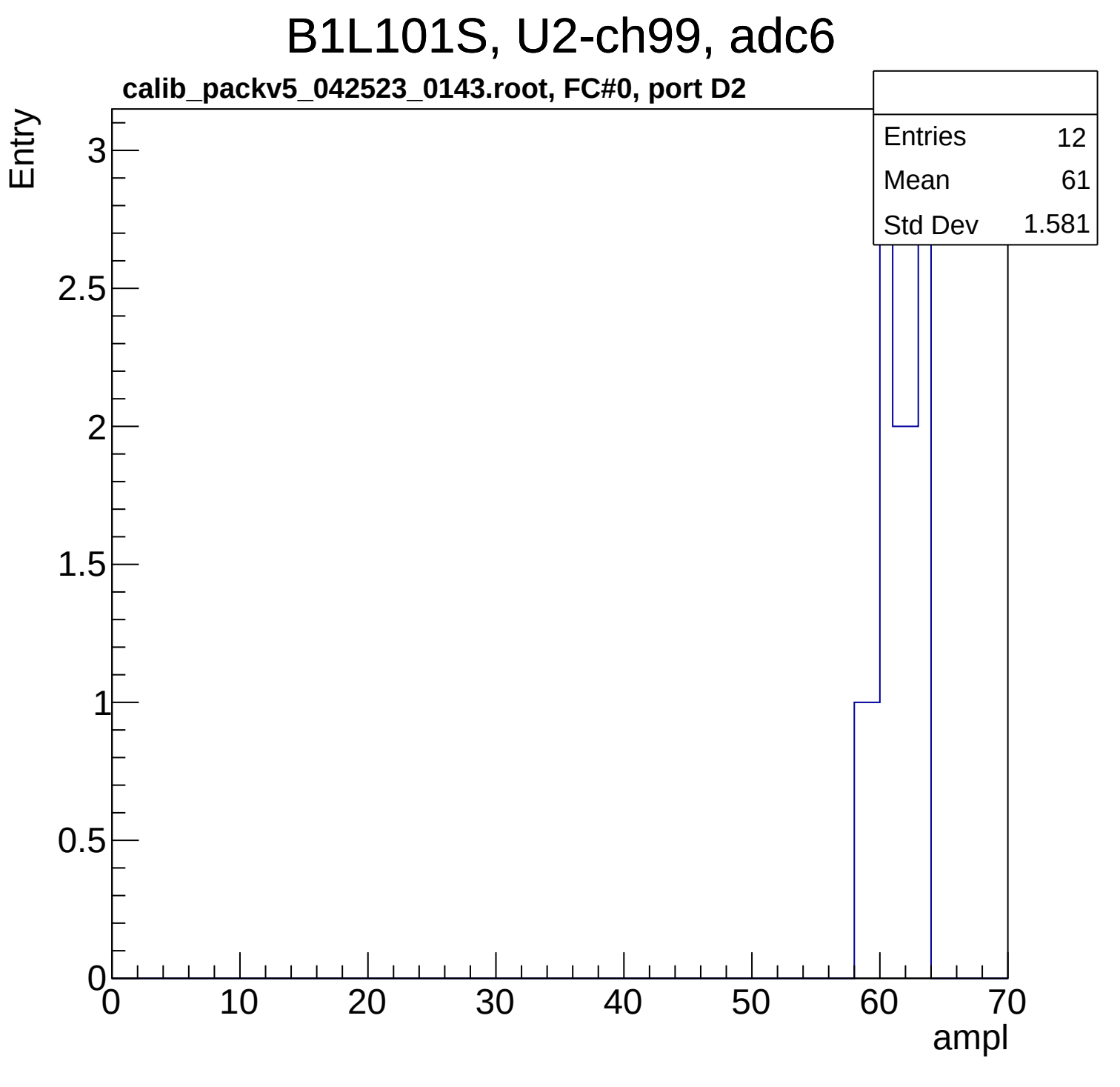

B1L101S, U2-ch99, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 36.21
Std Dev 3.576
Gaus mean : 36.7331
Gaus Width: 3.5414
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

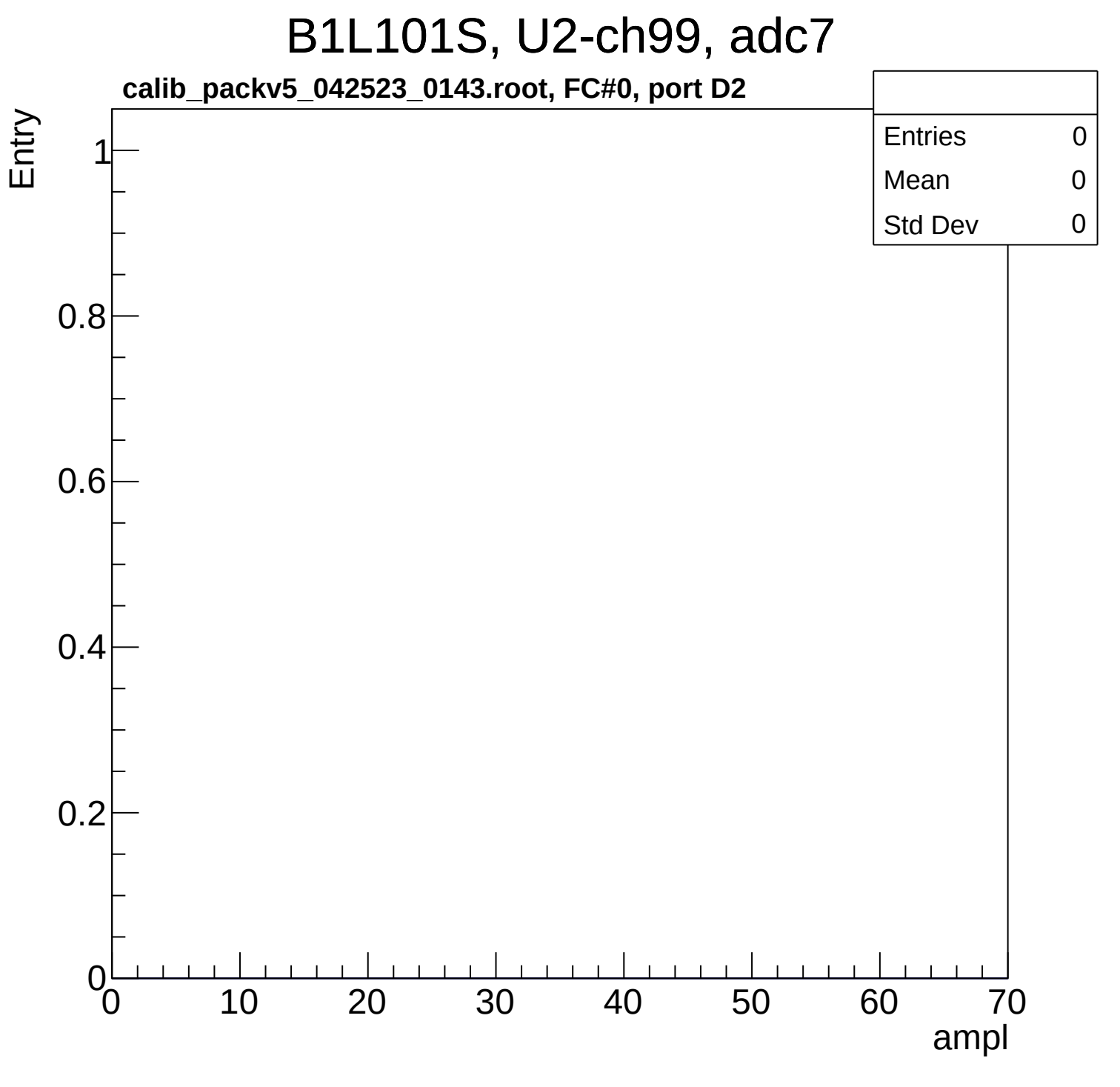

B1L101S, U2-ch99, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 41.93
Std Dev 3.355
Gaus mean : 41.8202
Gaus Width: 4.0320
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

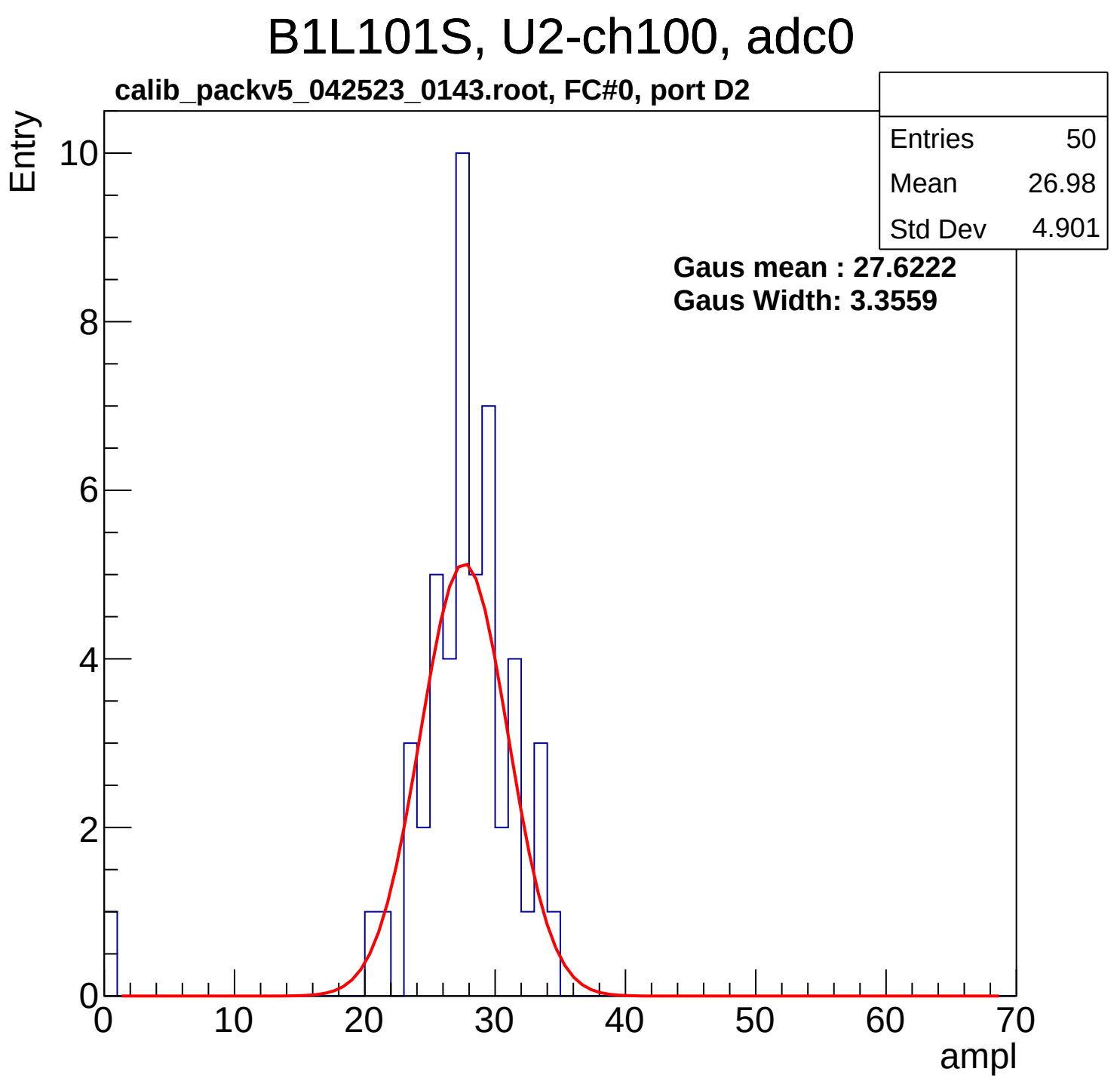

B1L101S, U2-ch99, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 48.95
Std Dev 3.891
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

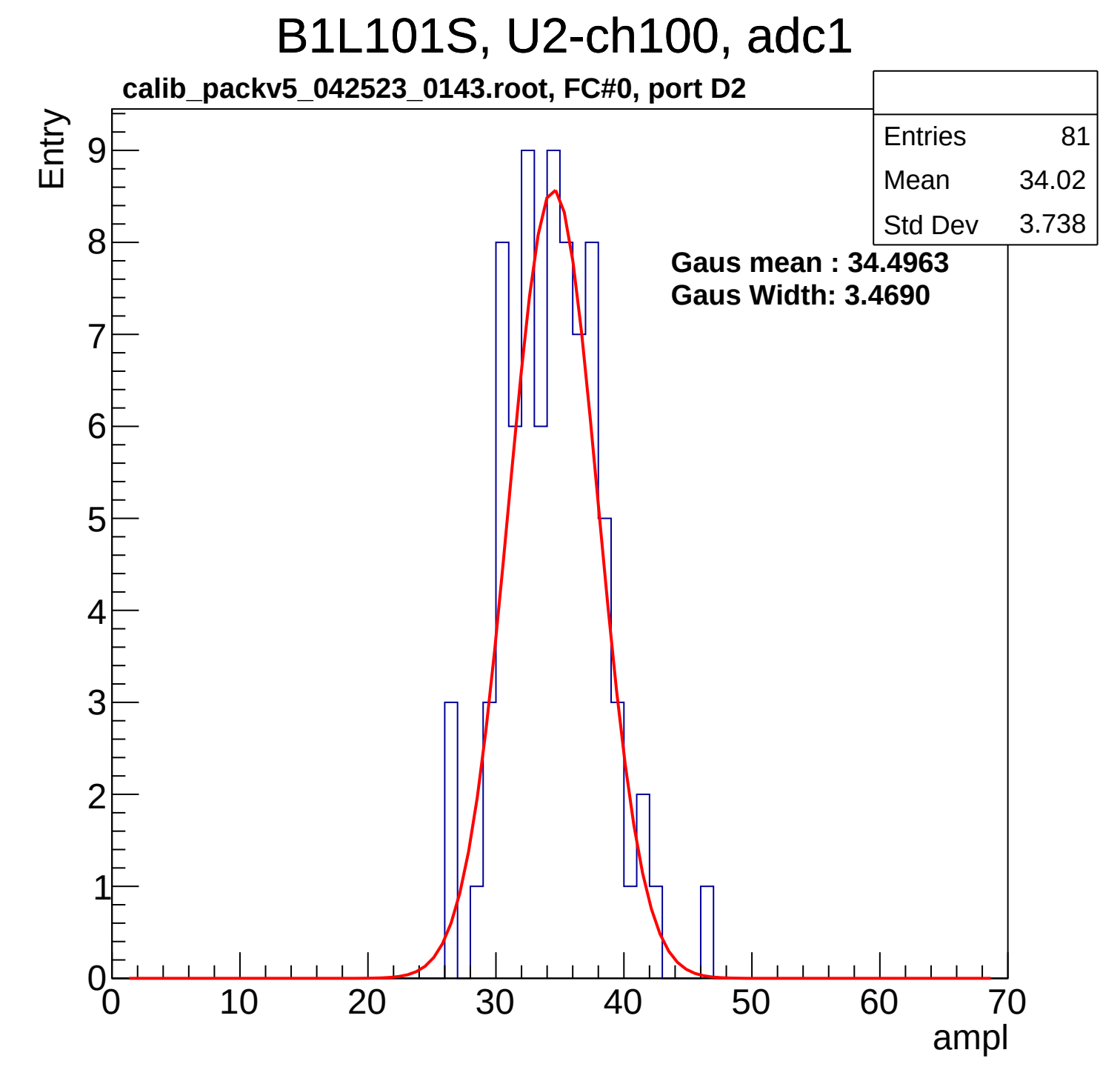

B1L101S, U2-ch99, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 55.3
Std Dev 3.427
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

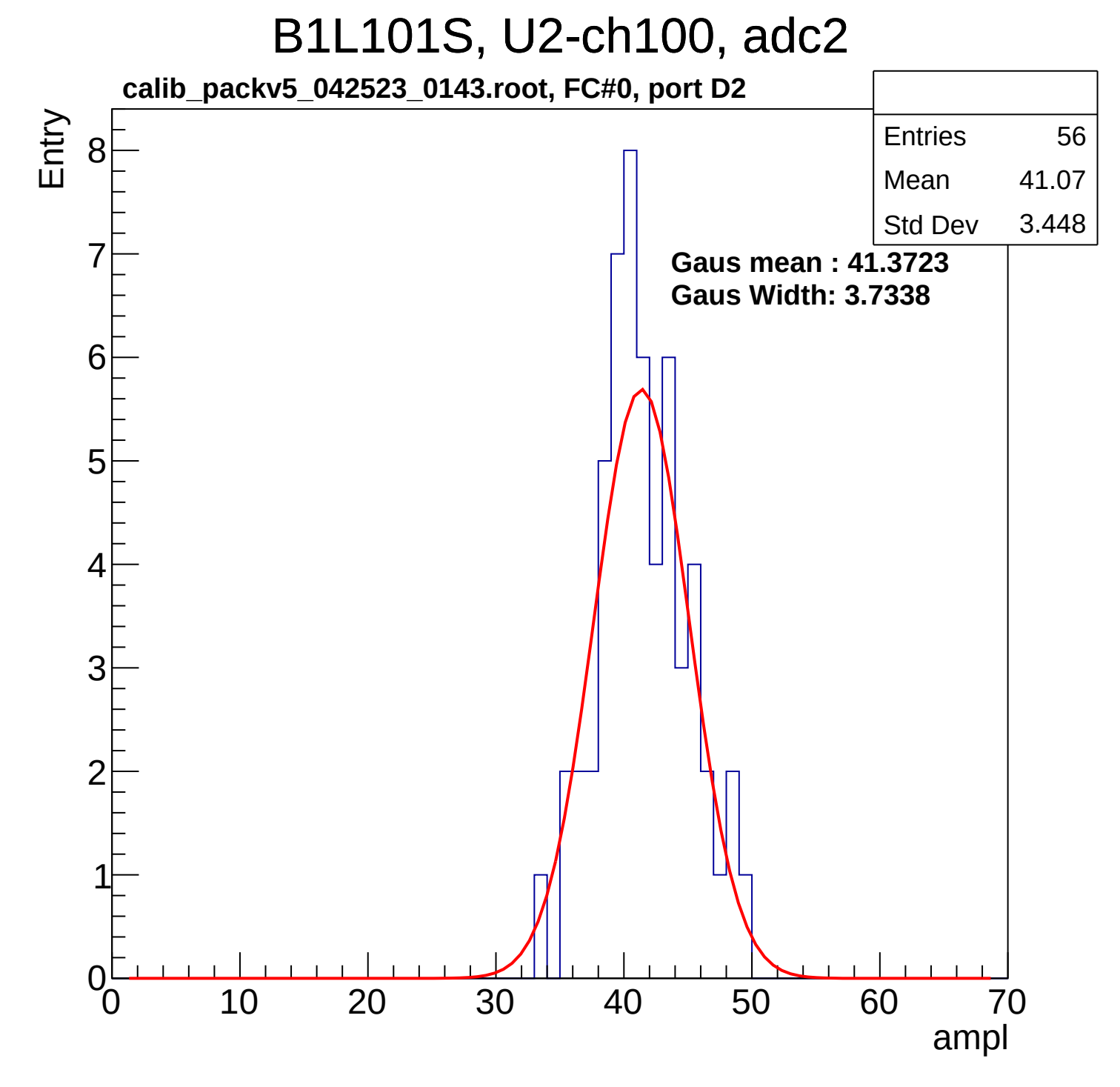

B1L101S, U2-ch99, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 58.14
Std Dev 9.471
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

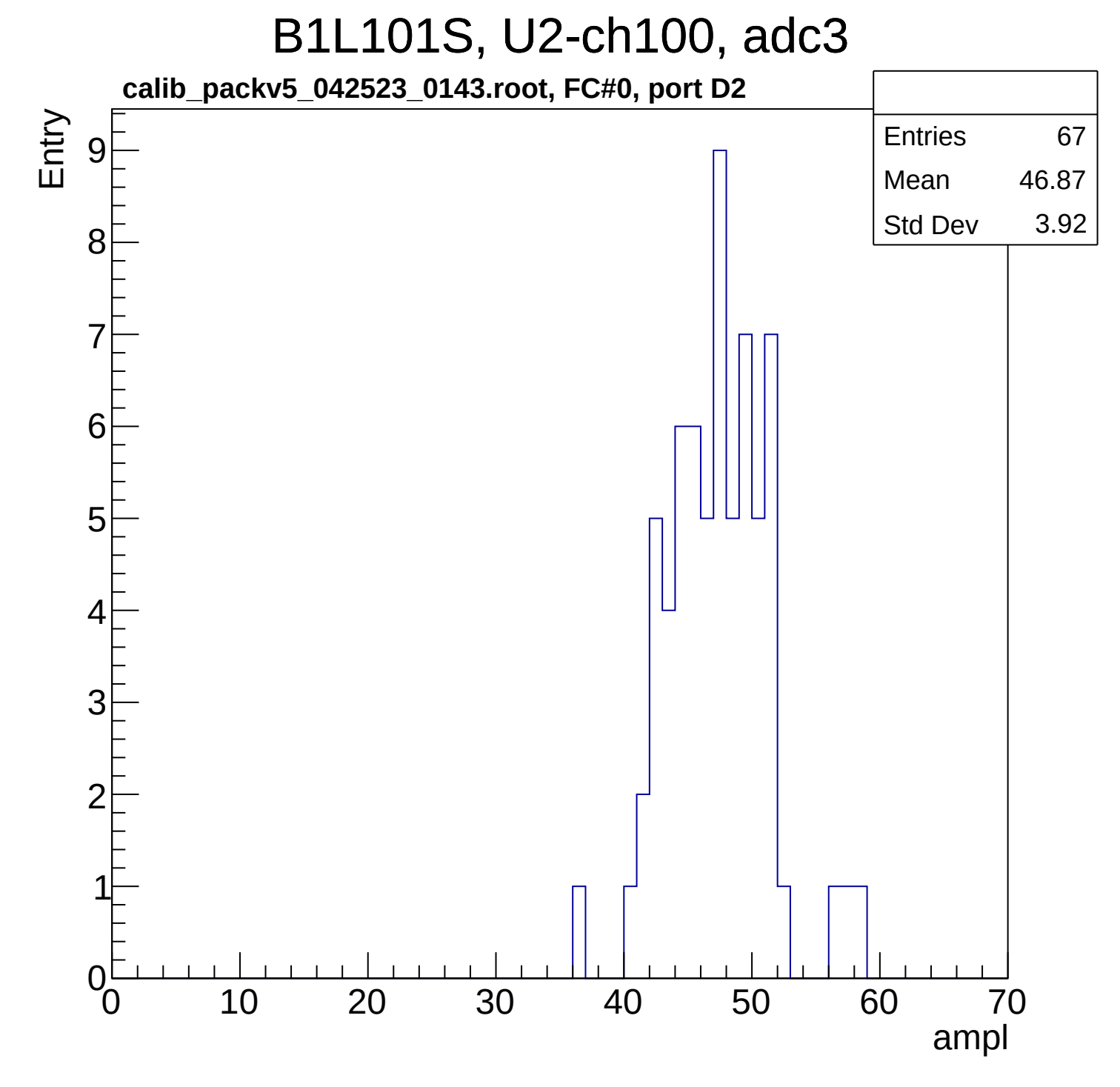

B1L101S, U2-ch99, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 12
Mean 61
Std Dev 1.581
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

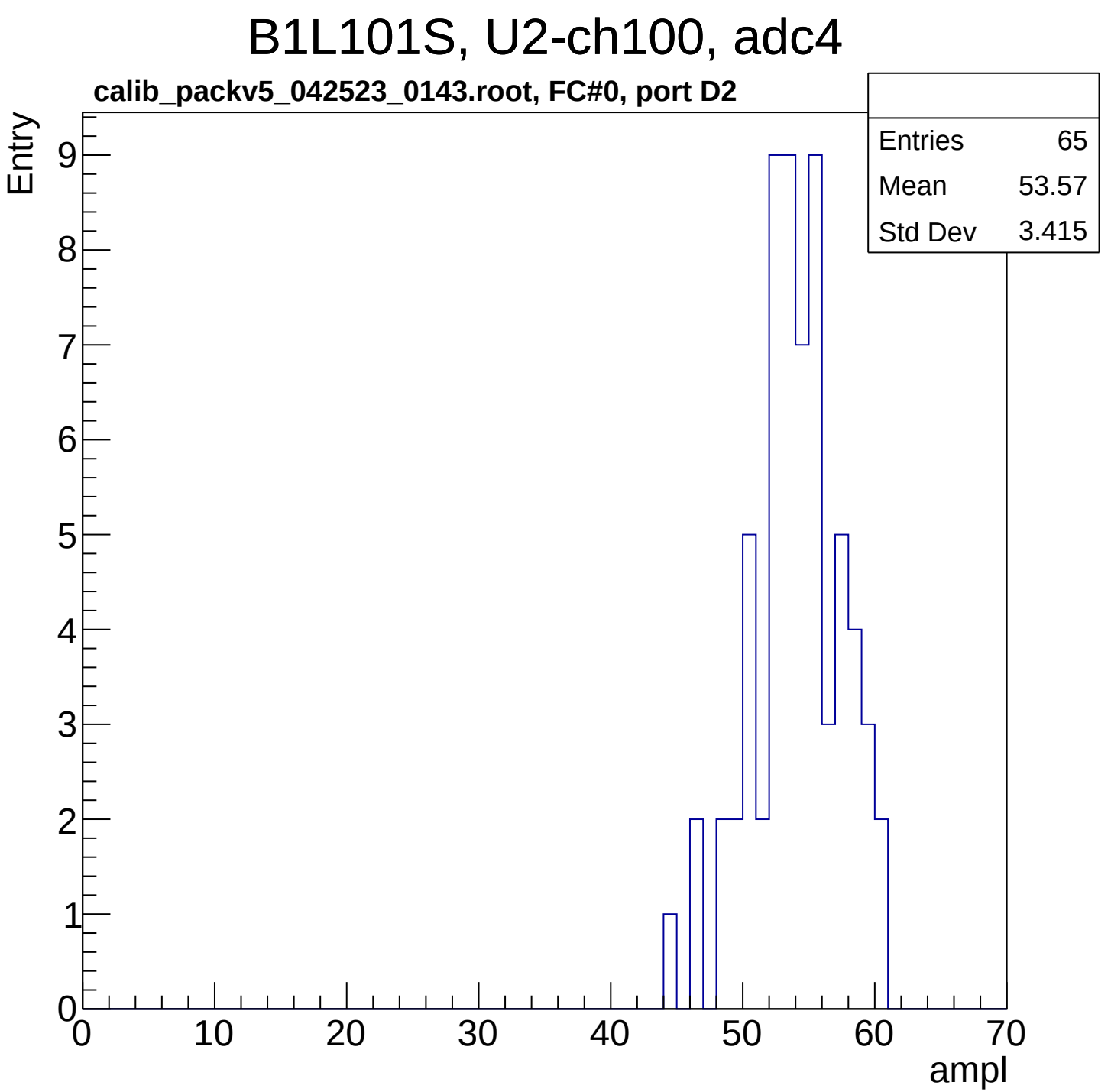

B1L101S, U2-ch99, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

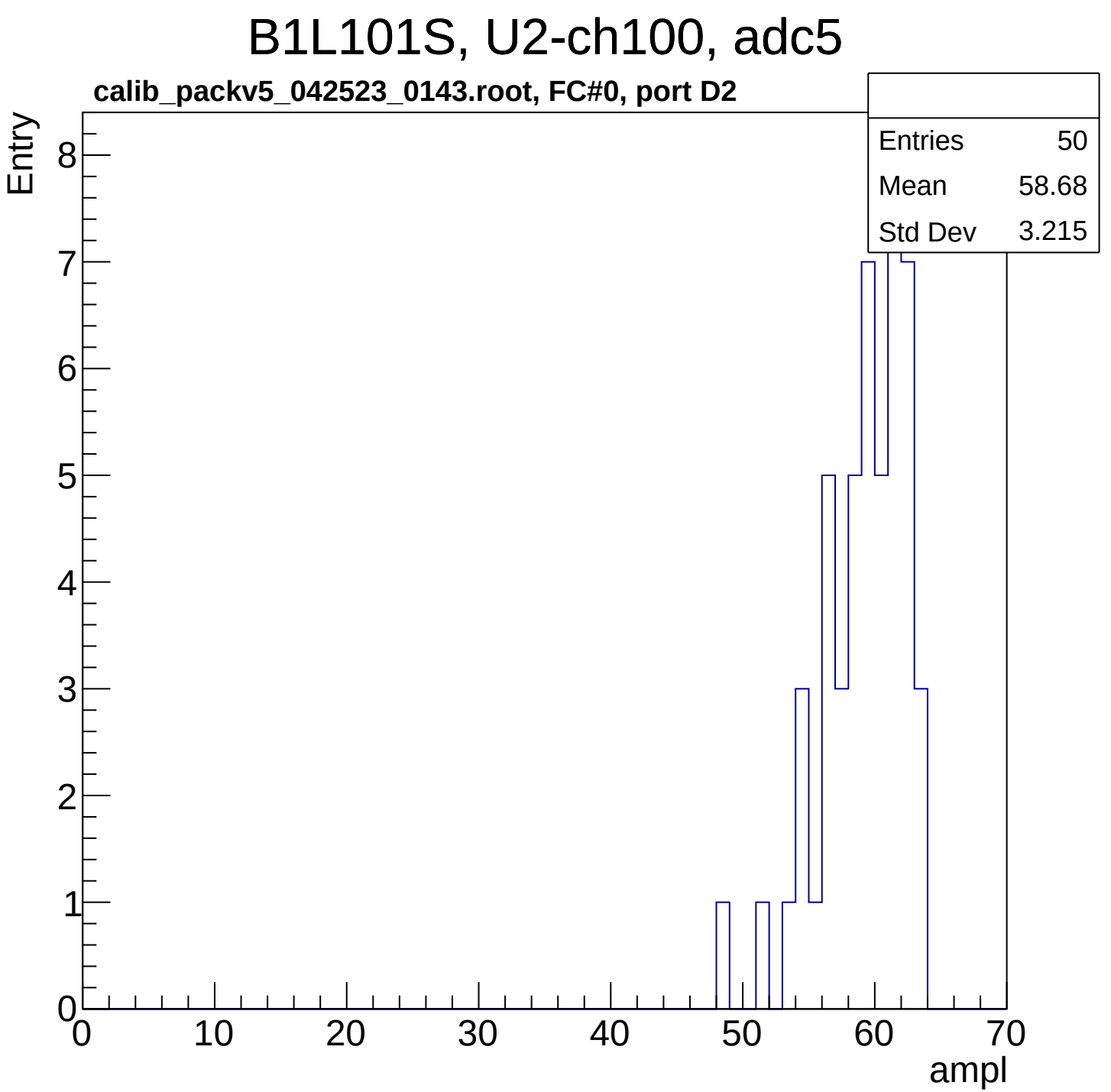

B1L101S, U2-ch100, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 26.98
Std Dev 4.901
Gaus mean : 27.6222
Gaus Width: 3.3559
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

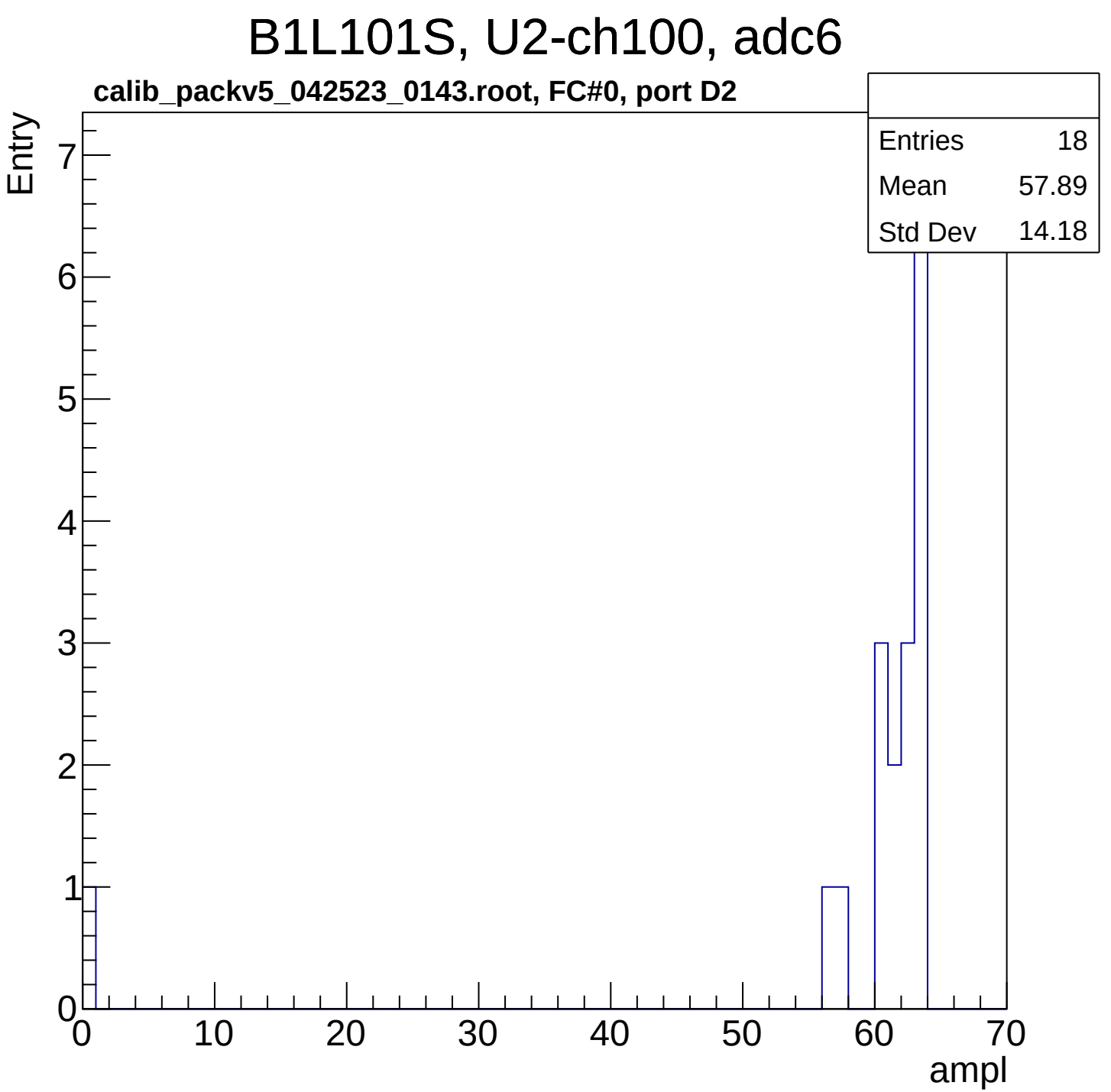

B1L101S, U2-ch100, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 81
Mean 34.02
Std Dev 3.738
Gaus mean : 34.4963
Gaus Width: 3.4690
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

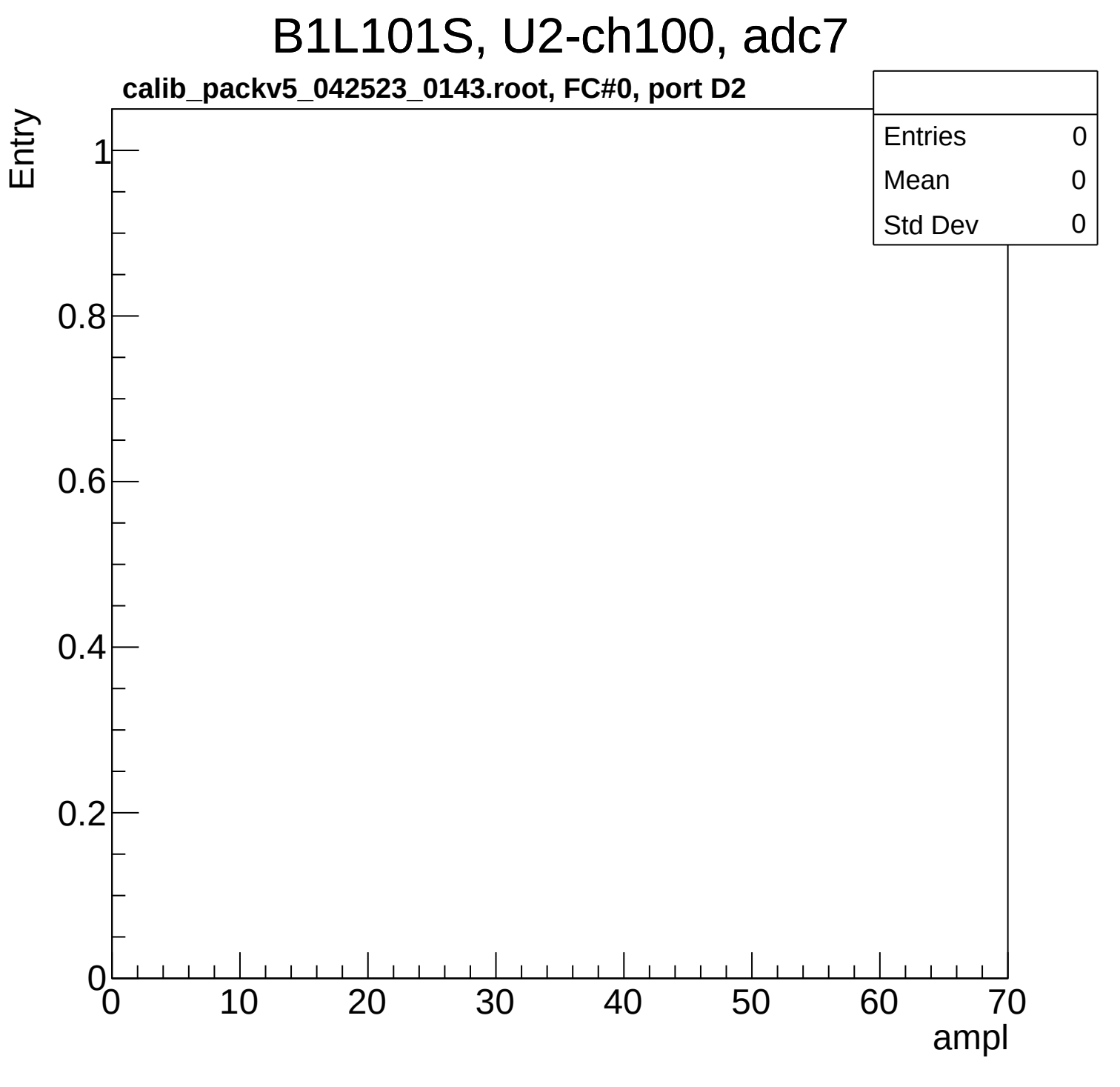

B1L101S, U2-ch100, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 41.07
Std Dev 3.448
Gaus mean : 41.3723
Gaus Width: 3.7338
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

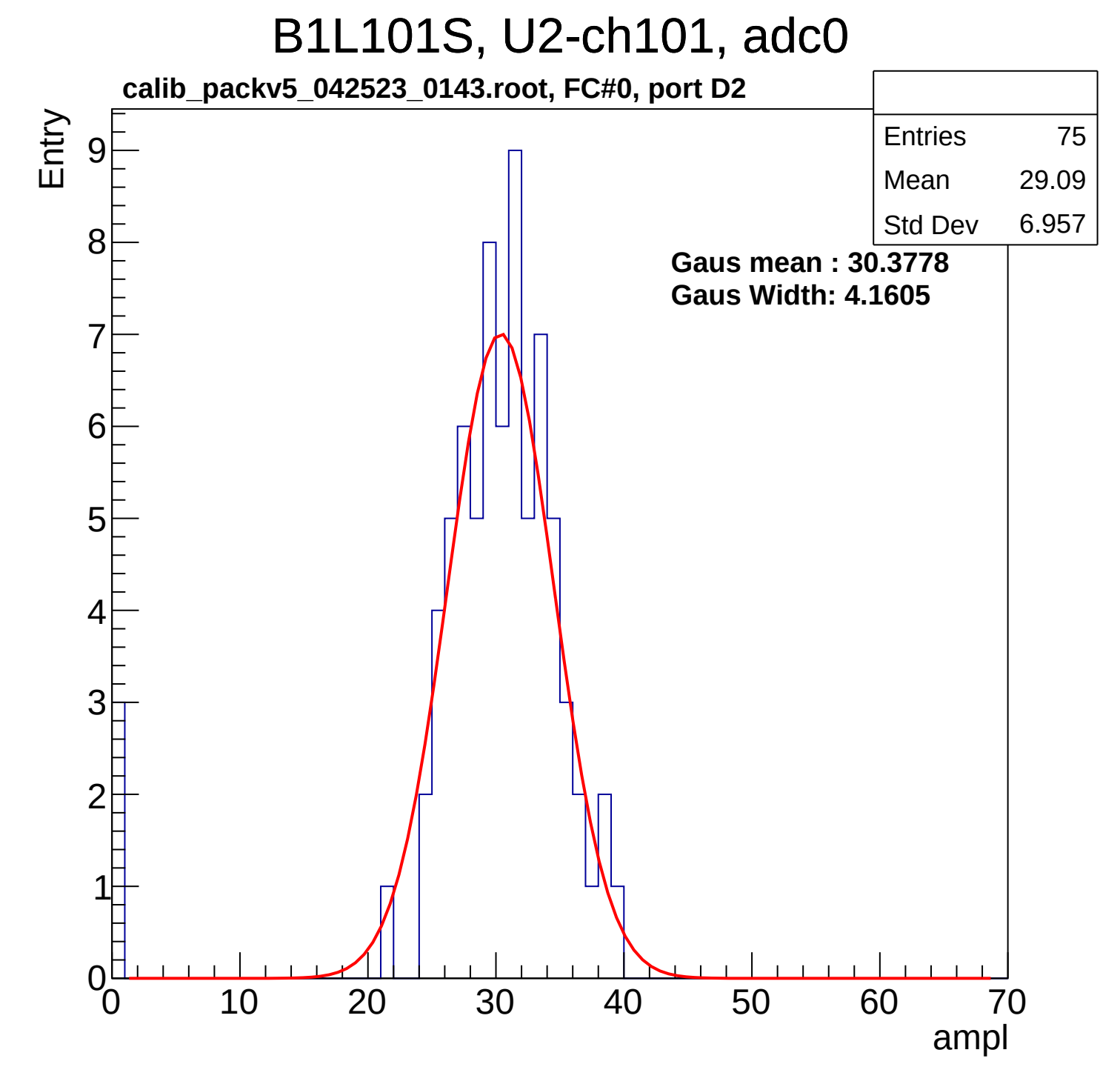

B1L101S, U2-ch100, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 46.87
Std Dev 3.92
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

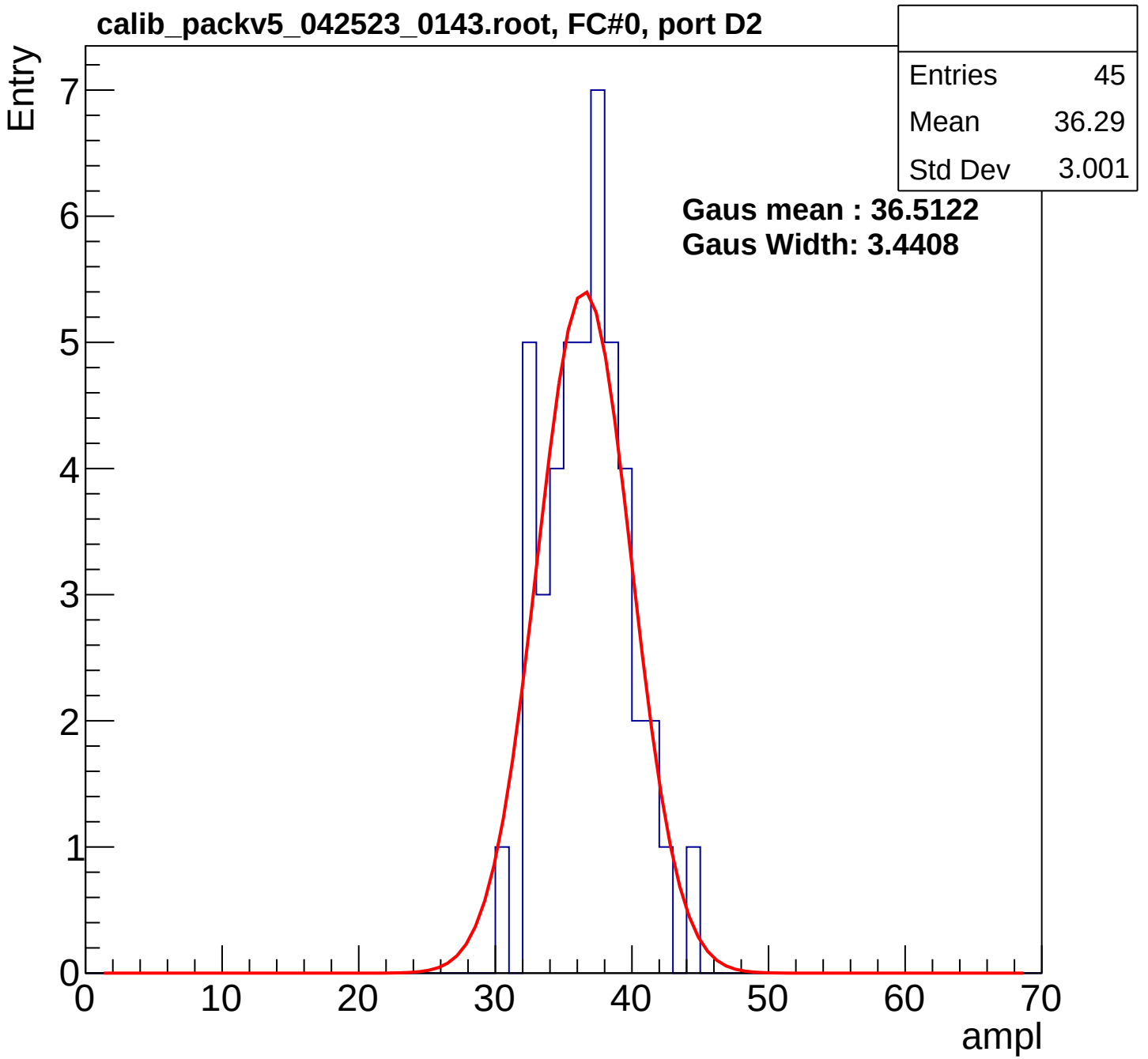

B1L101S, U2-ch100, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 53.57
Std Dev 3.415
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

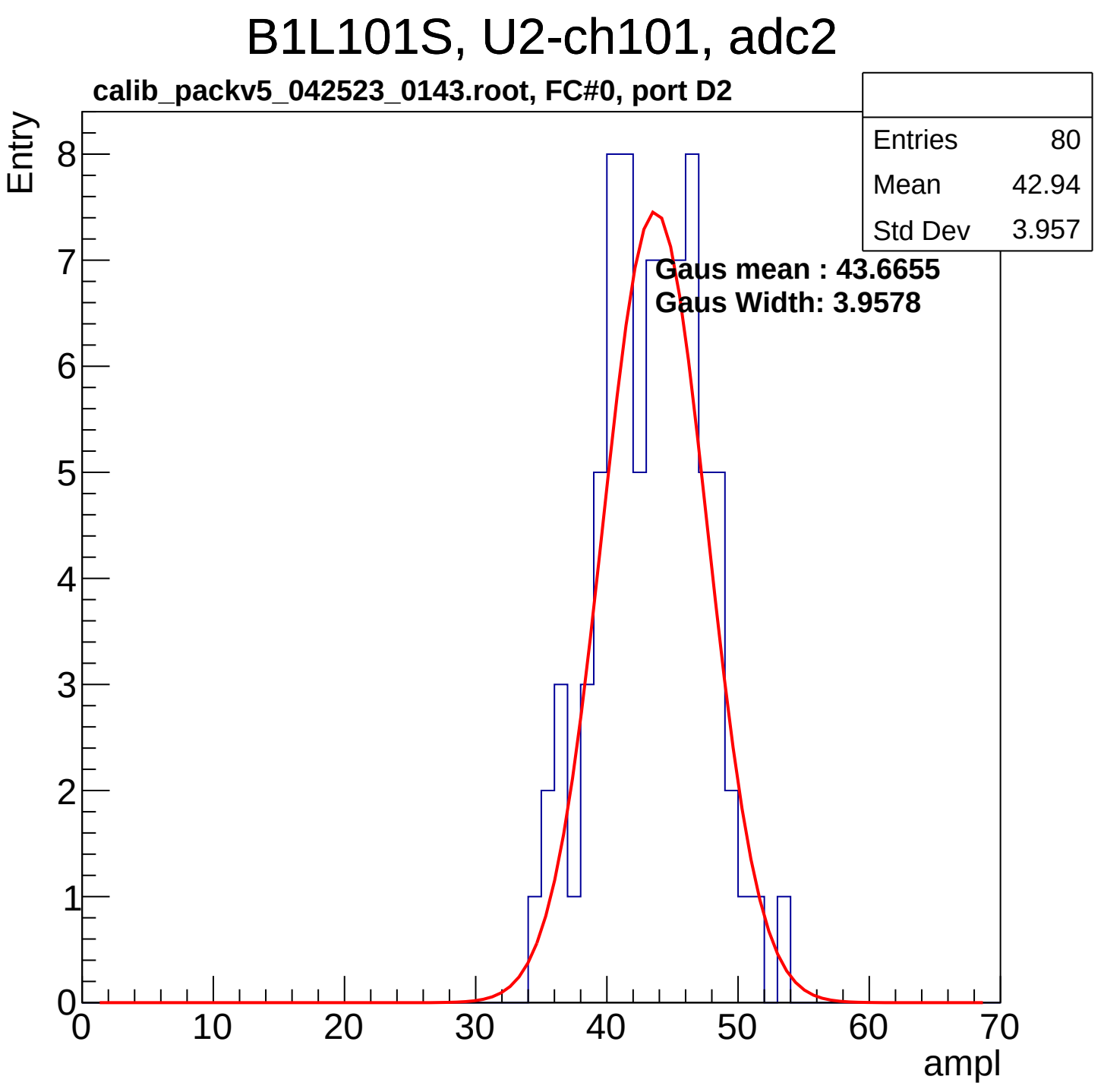

B1L101S, U2-ch100, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 58.68
Std Dev 3.215
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

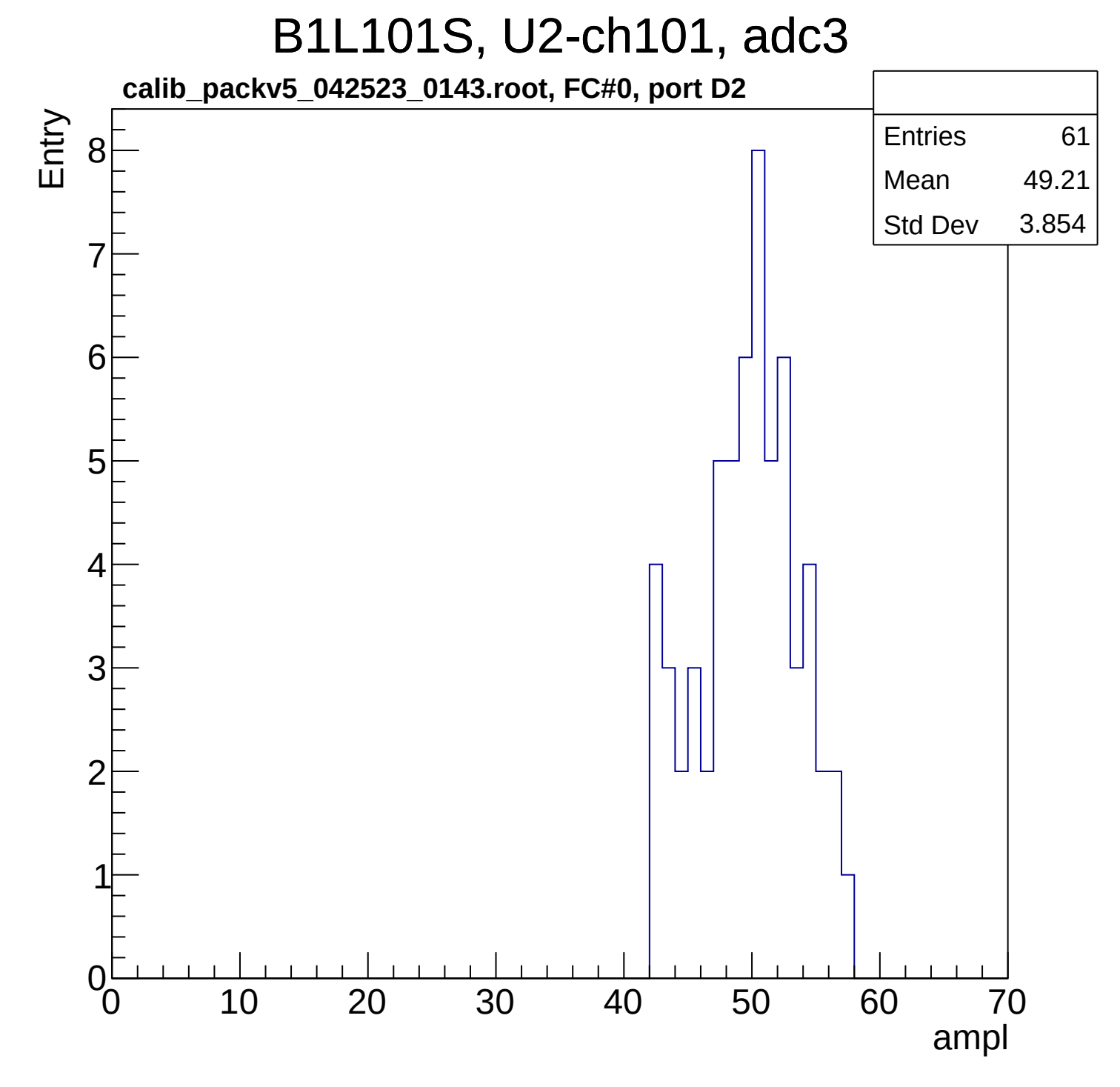

B1L101S, U2-ch100, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 18
Mean 57.89
Std Dev 14.18
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

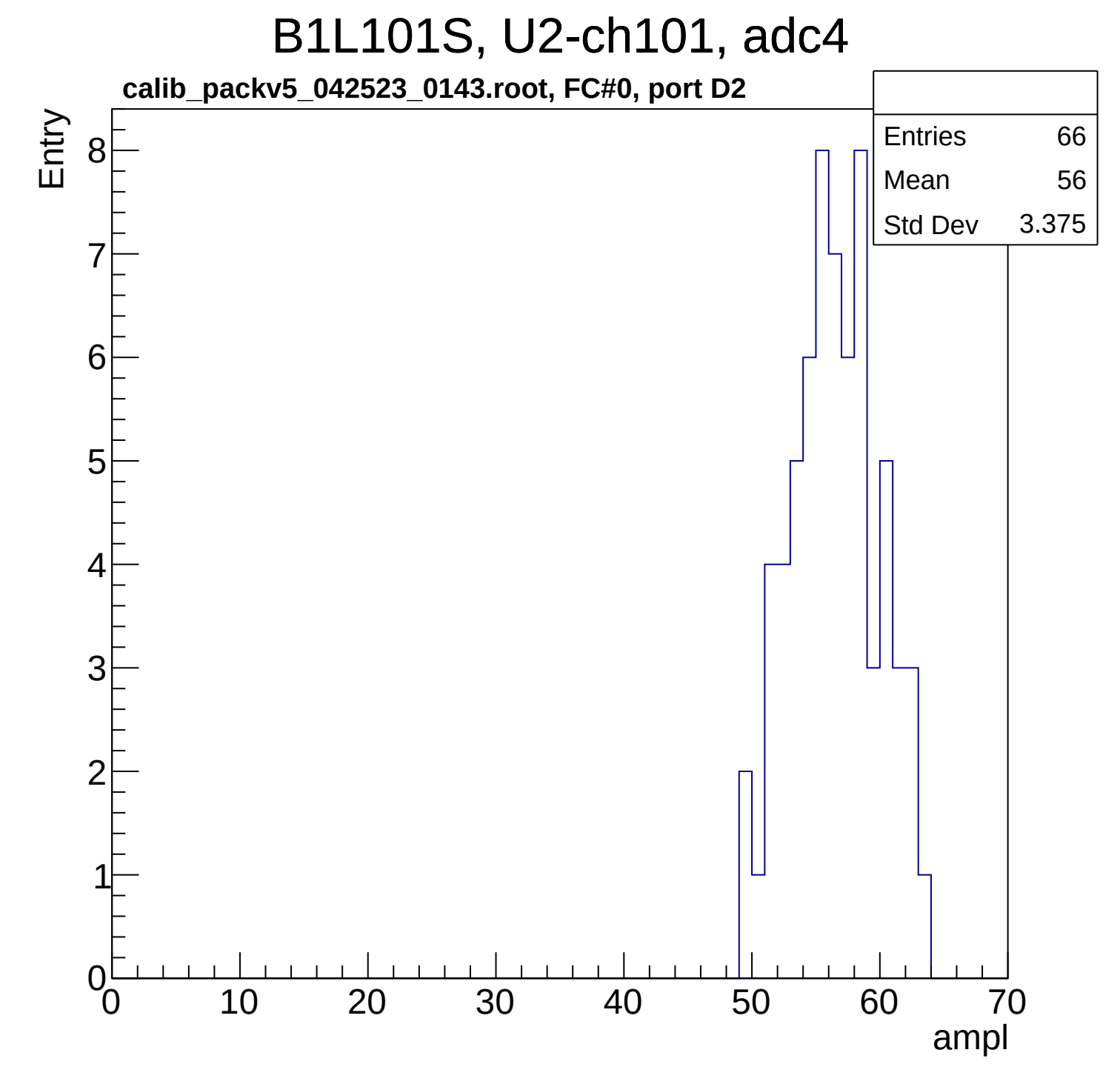

B1L101S, U2-ch100, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

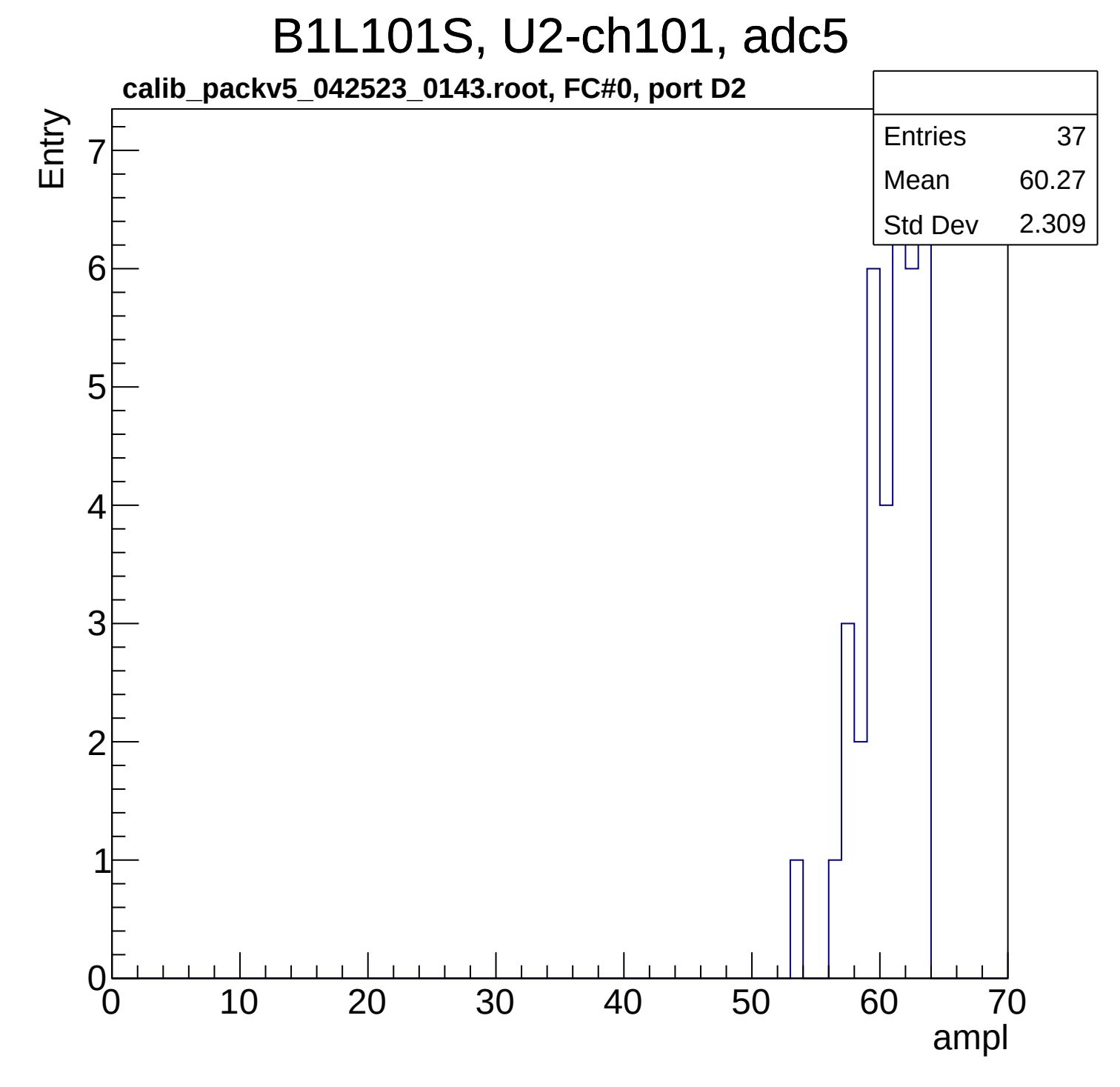

B1L101S, U2-ch101, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 29.09
Std Dev 6.957
Gaus mean : 30.3778
Gaus Width: 4.1605
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

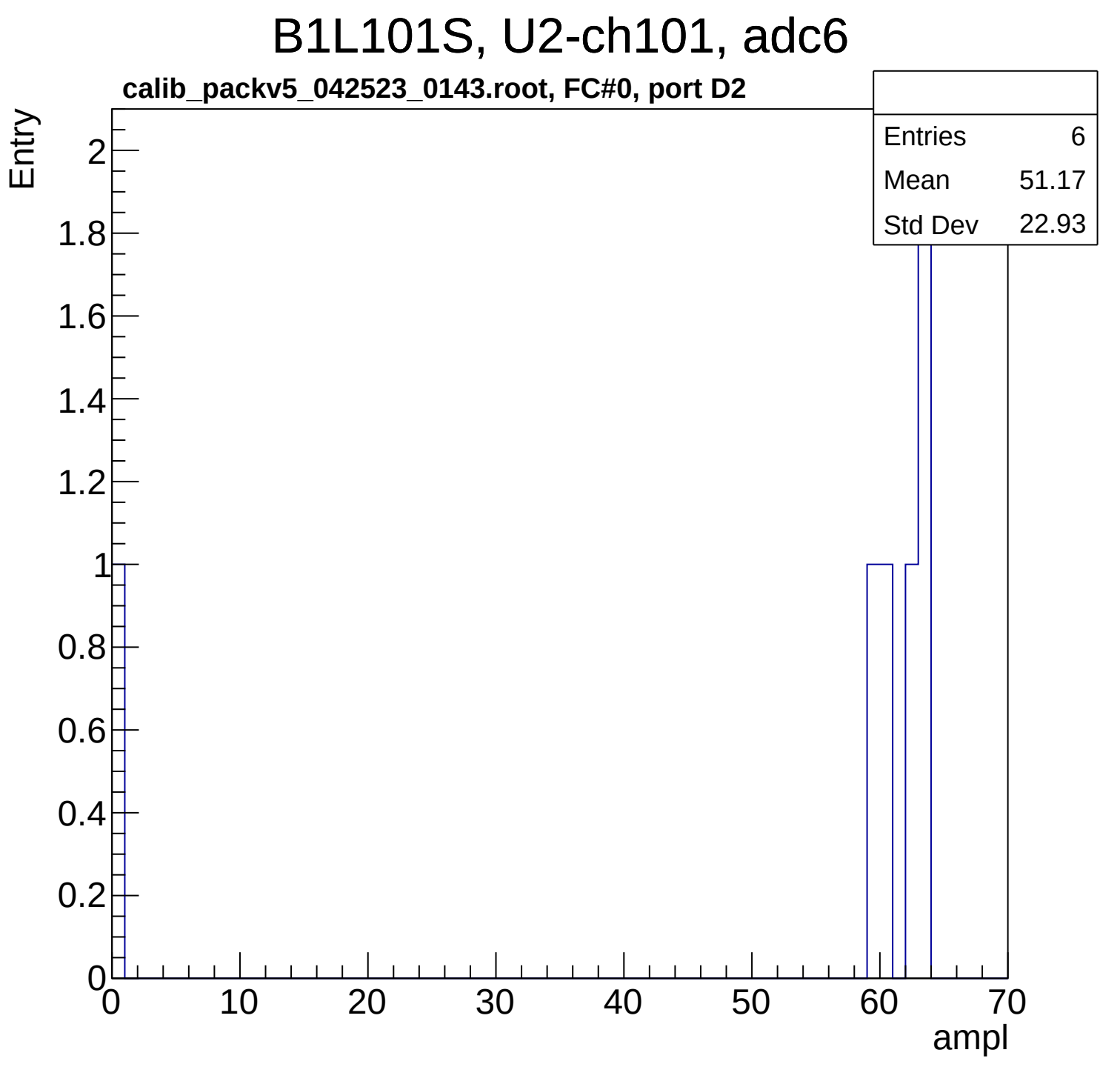

B1L101S, U2-ch101, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 36.29
Std Dev 3.001
Gaus mean : 36.5122
Gaus Width: 3.4408
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

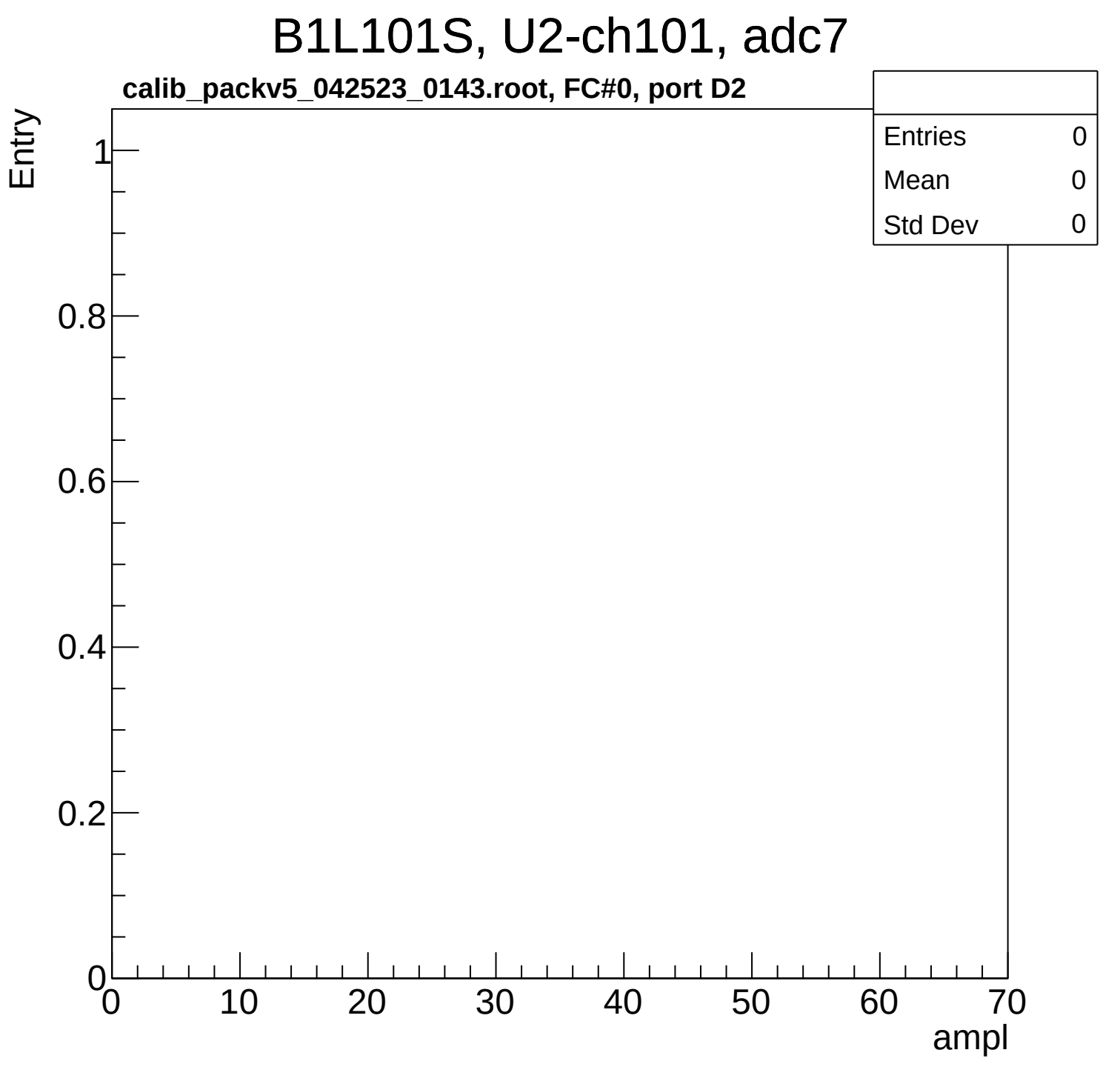

B1L101S, U2-ch101, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 80
Mean 42.94
Std Dev 3.957
Gaus mean : 43.6655
Gaus Width: 3.9578
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

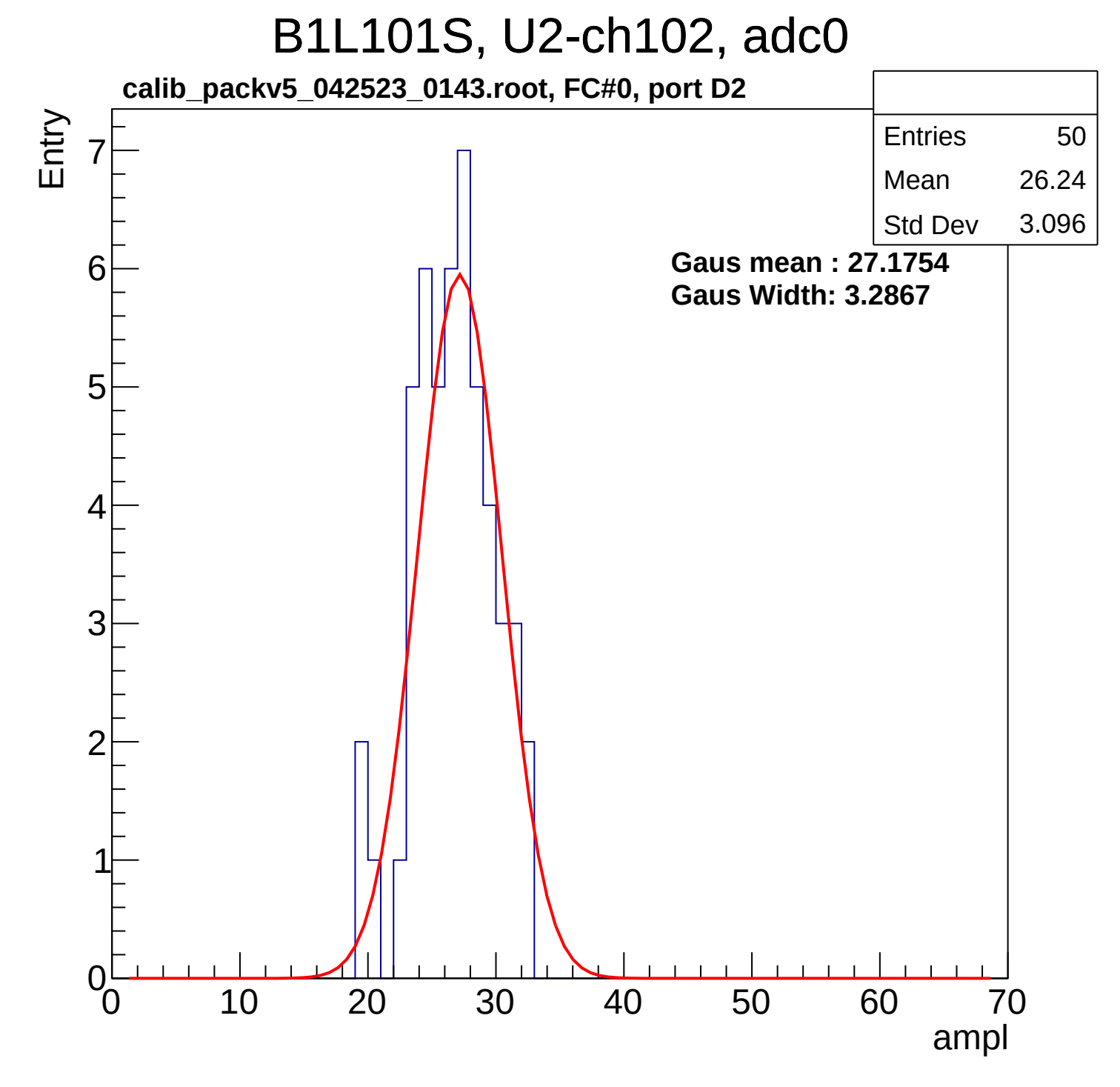

B1L101S, U2-ch101, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 49.21
Std Dev 3.854
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

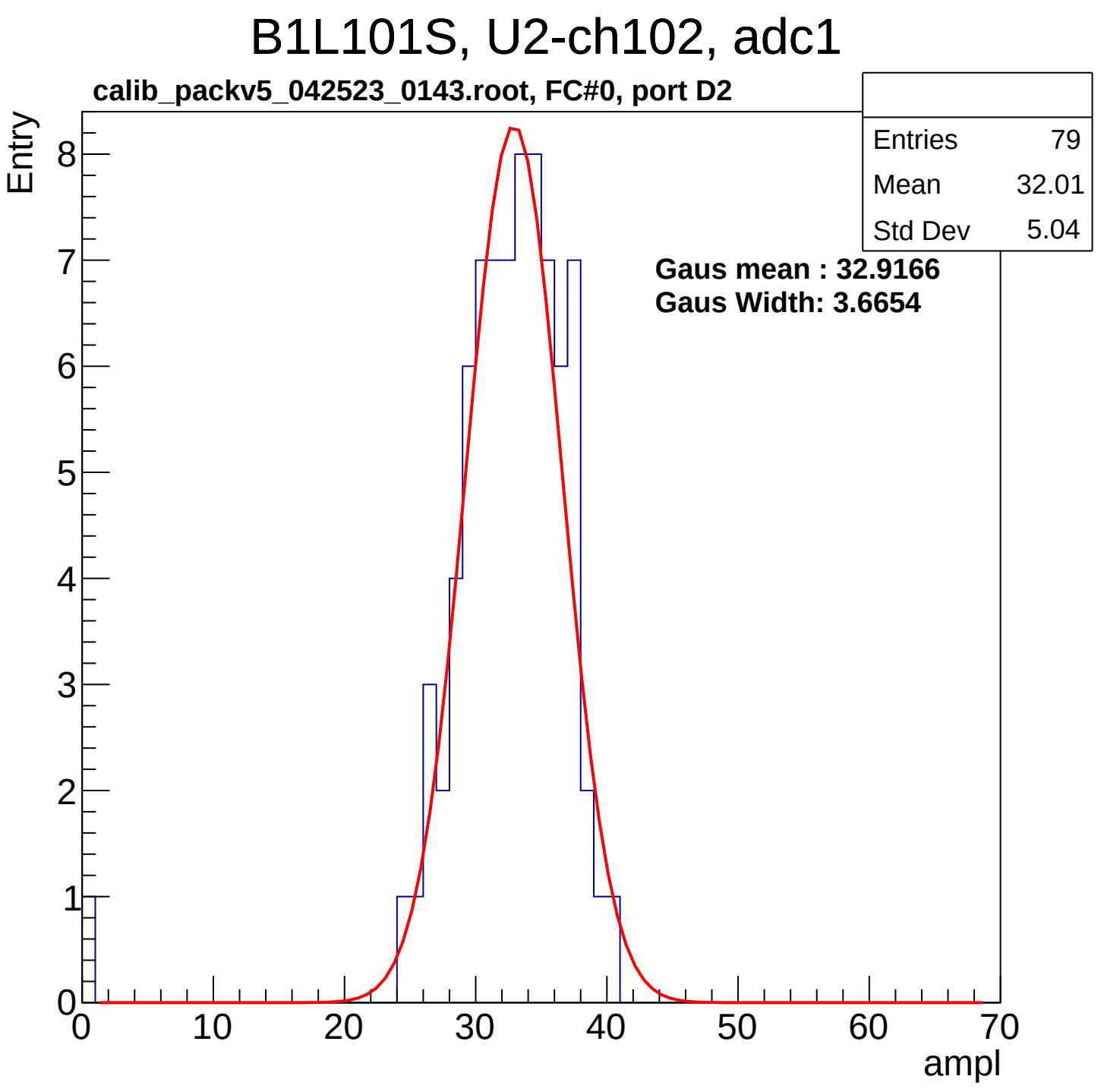

B1L101S, U2-ch101, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 56
Std Dev 3.375
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

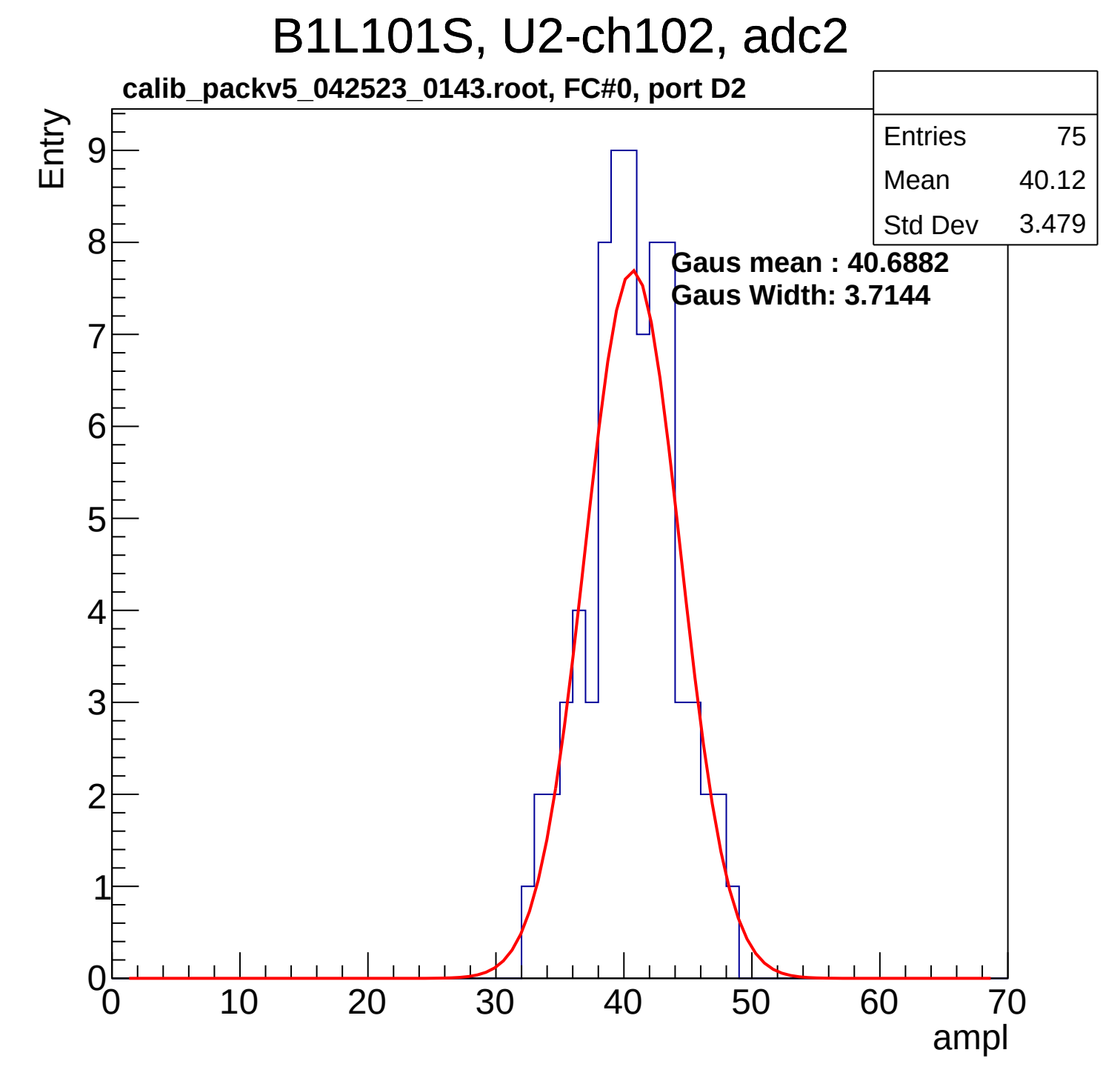

B1L101S, U2-ch101, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 37
Mean 60.27
Std Dev 2.309
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

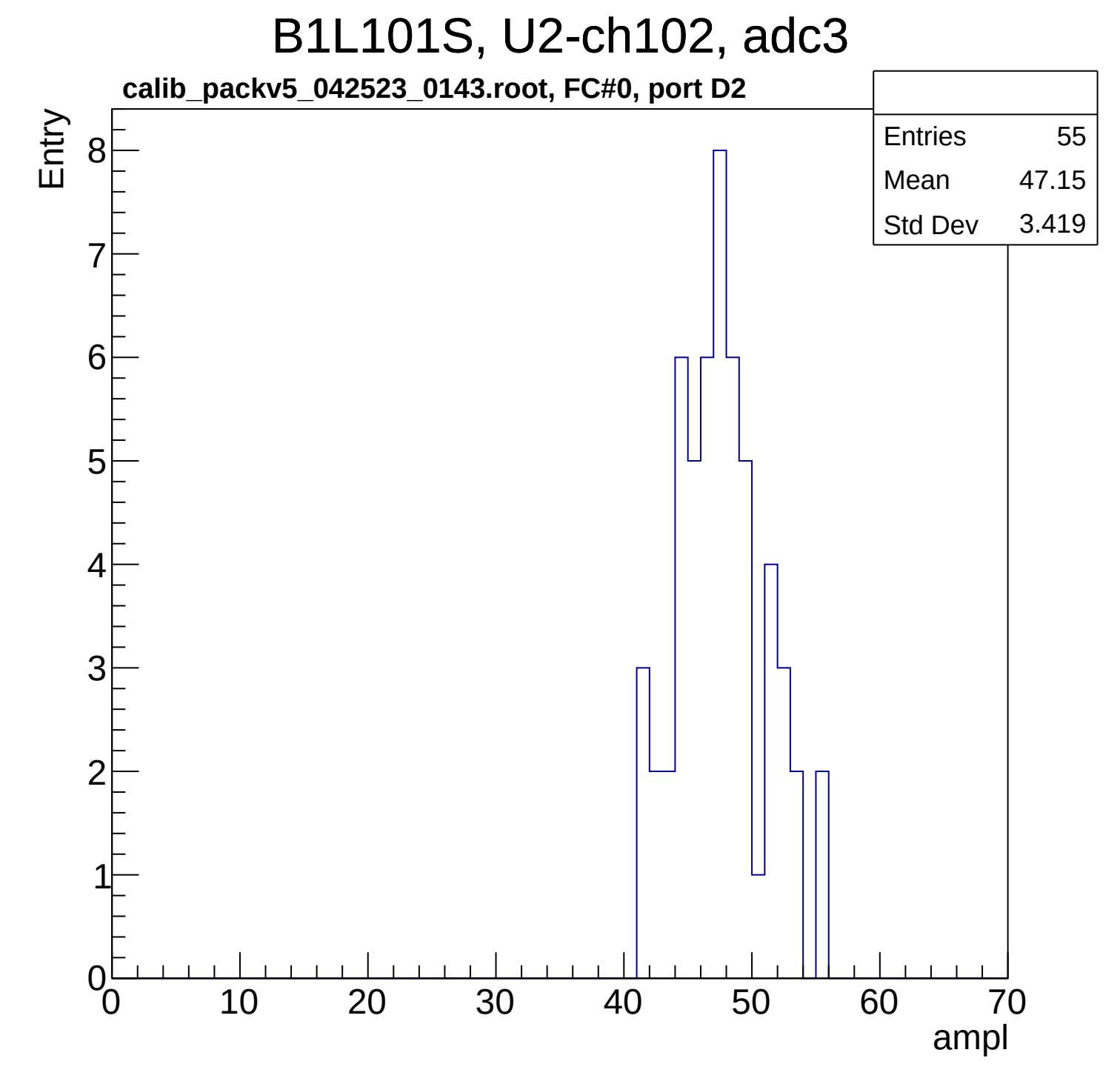

B1L101S, U2-ch101, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 51.17
Std Dev 22.93
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

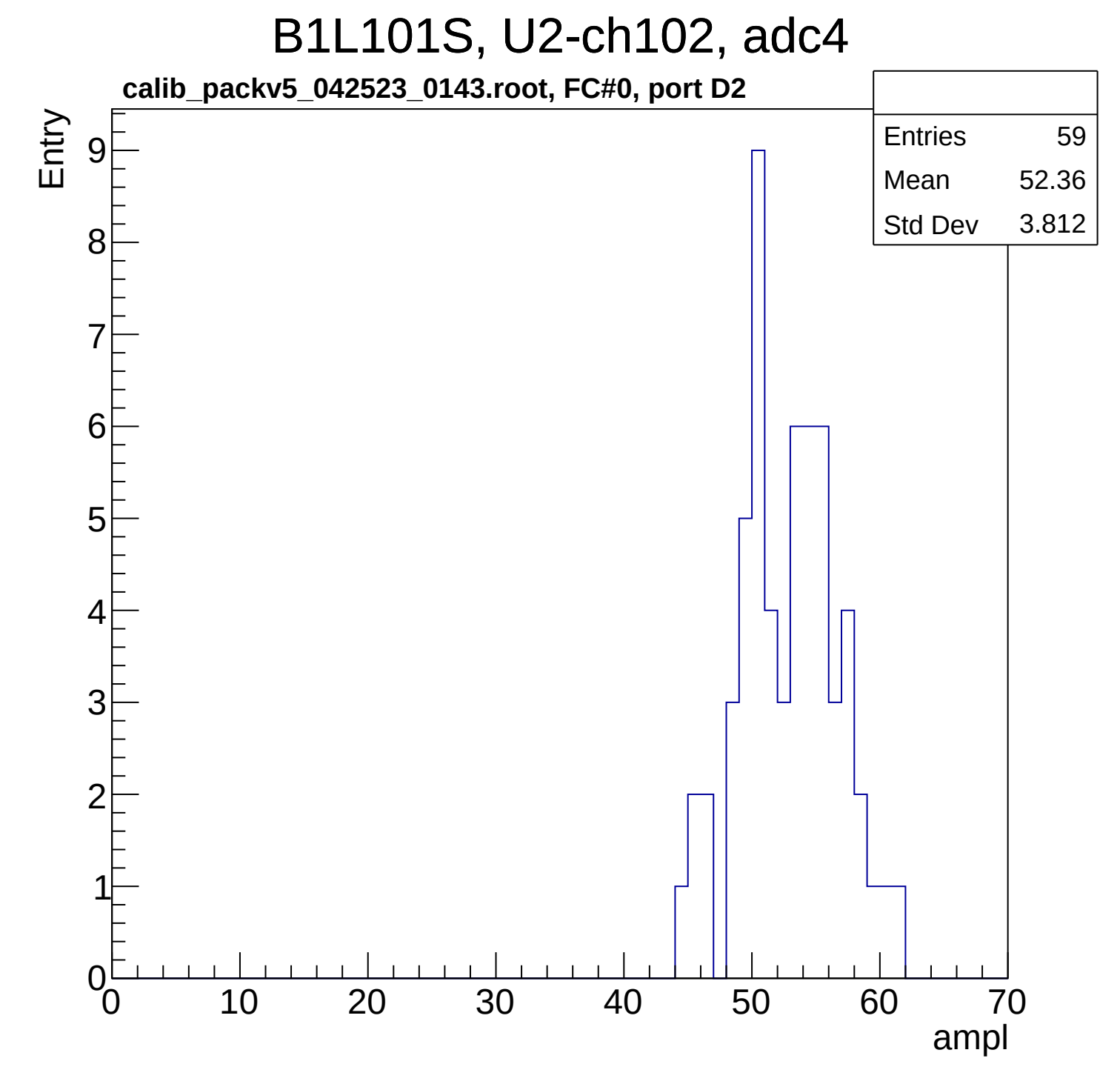

B1L101S, U2-ch101, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

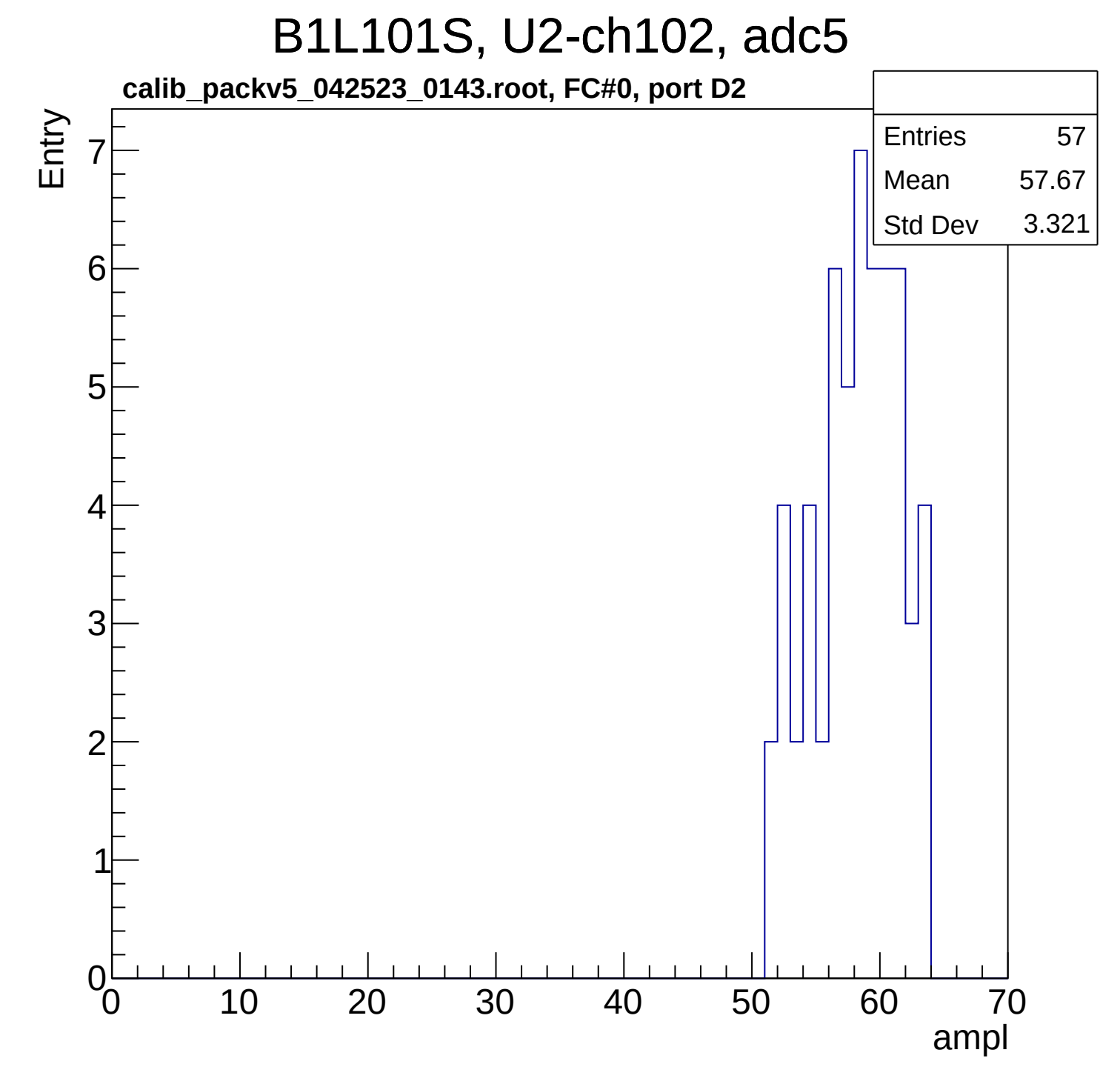

B1L101S, U2-ch102, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 26.24
Std Dev 3.096
Gaus mean : 27.1754
Gaus Width: 3.2867
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

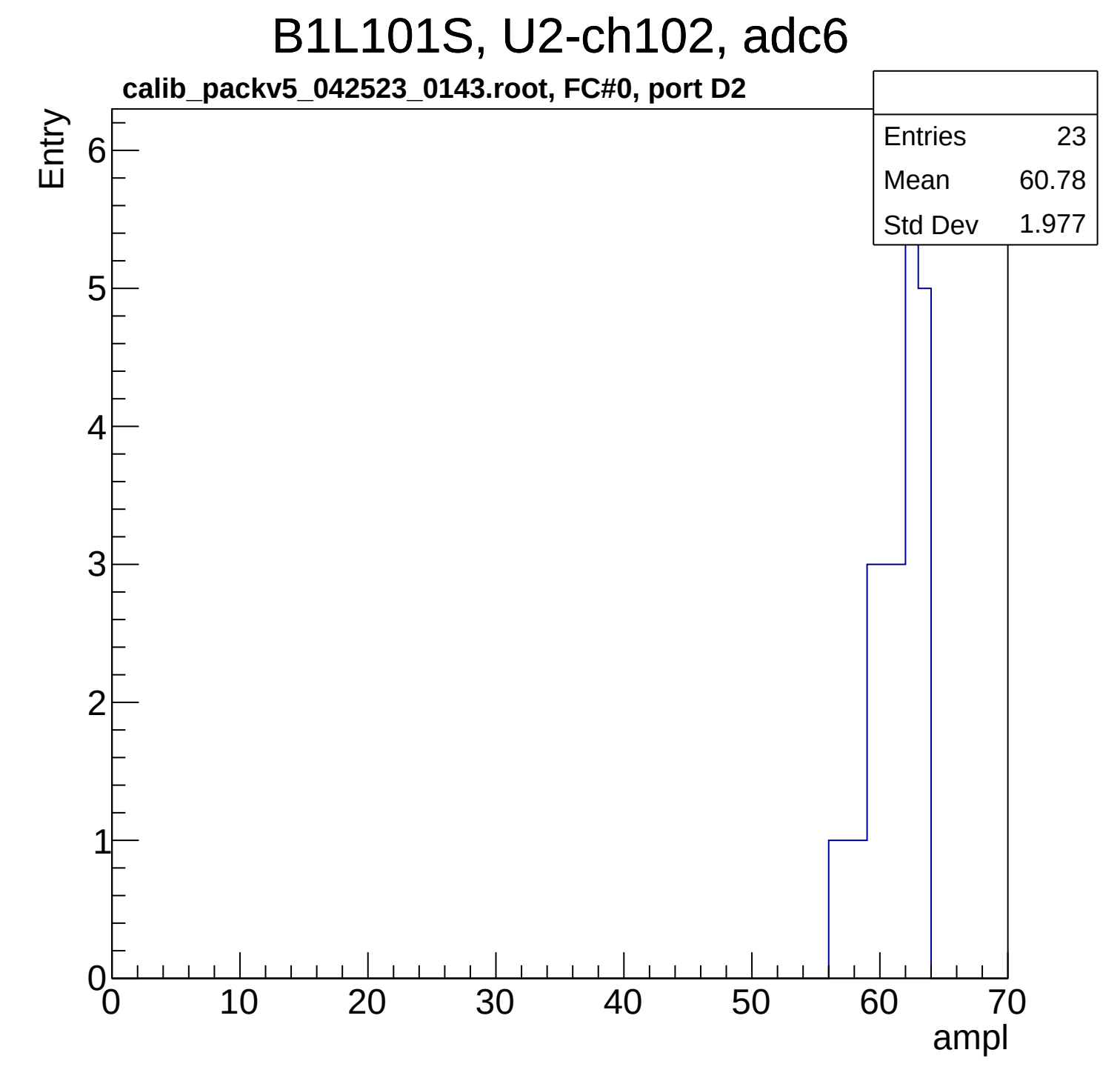

B1L101S, U2-ch102, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 32.01
Std Dev 5.04
Gaus mean : 32.9166
Gaus Width: 3.6654
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

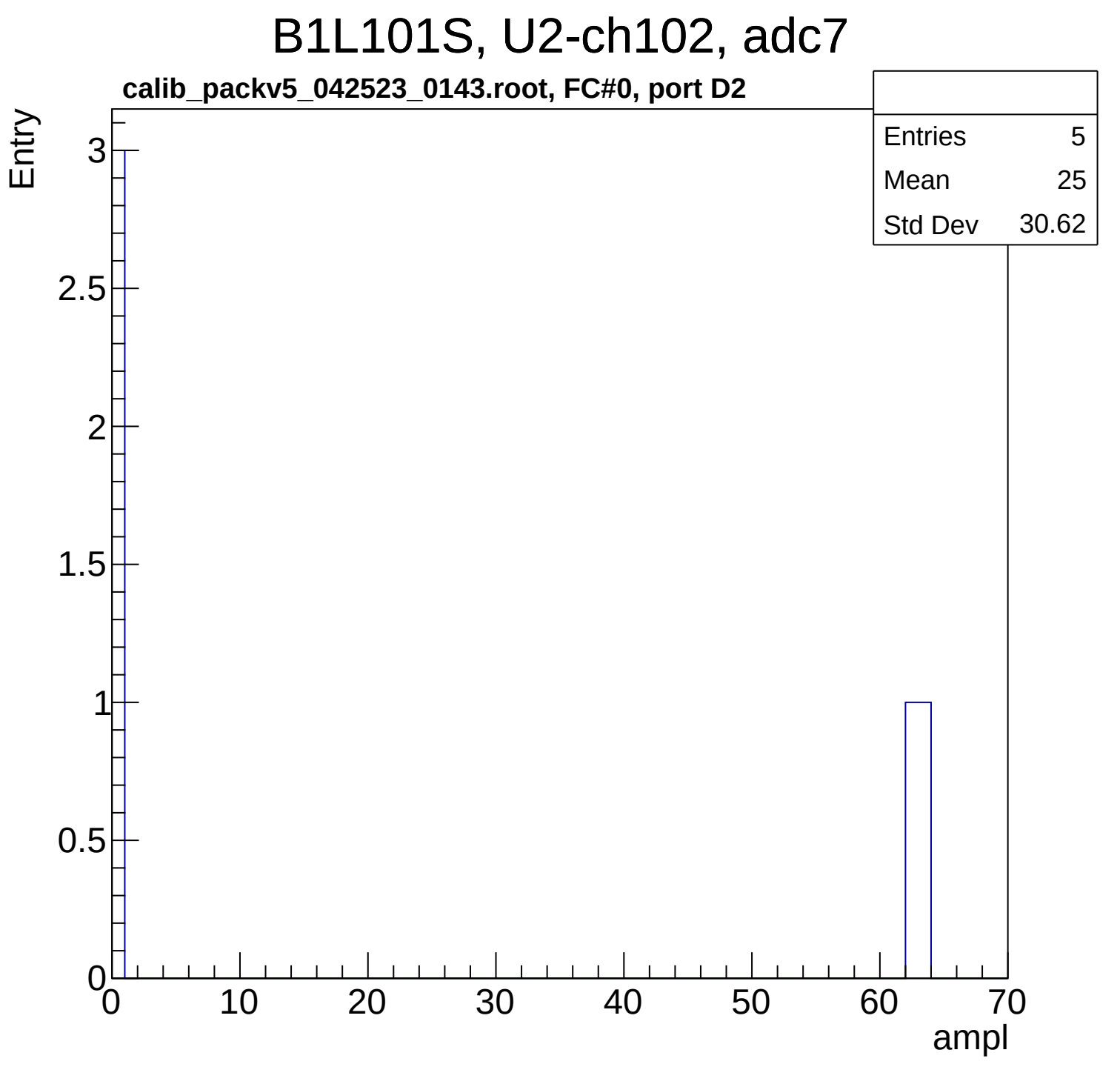

B1L101S, U2-ch102, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 40.12
Std Dev 3.479
Gaus mean : 40.6882
Gaus Width: 3.7144
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

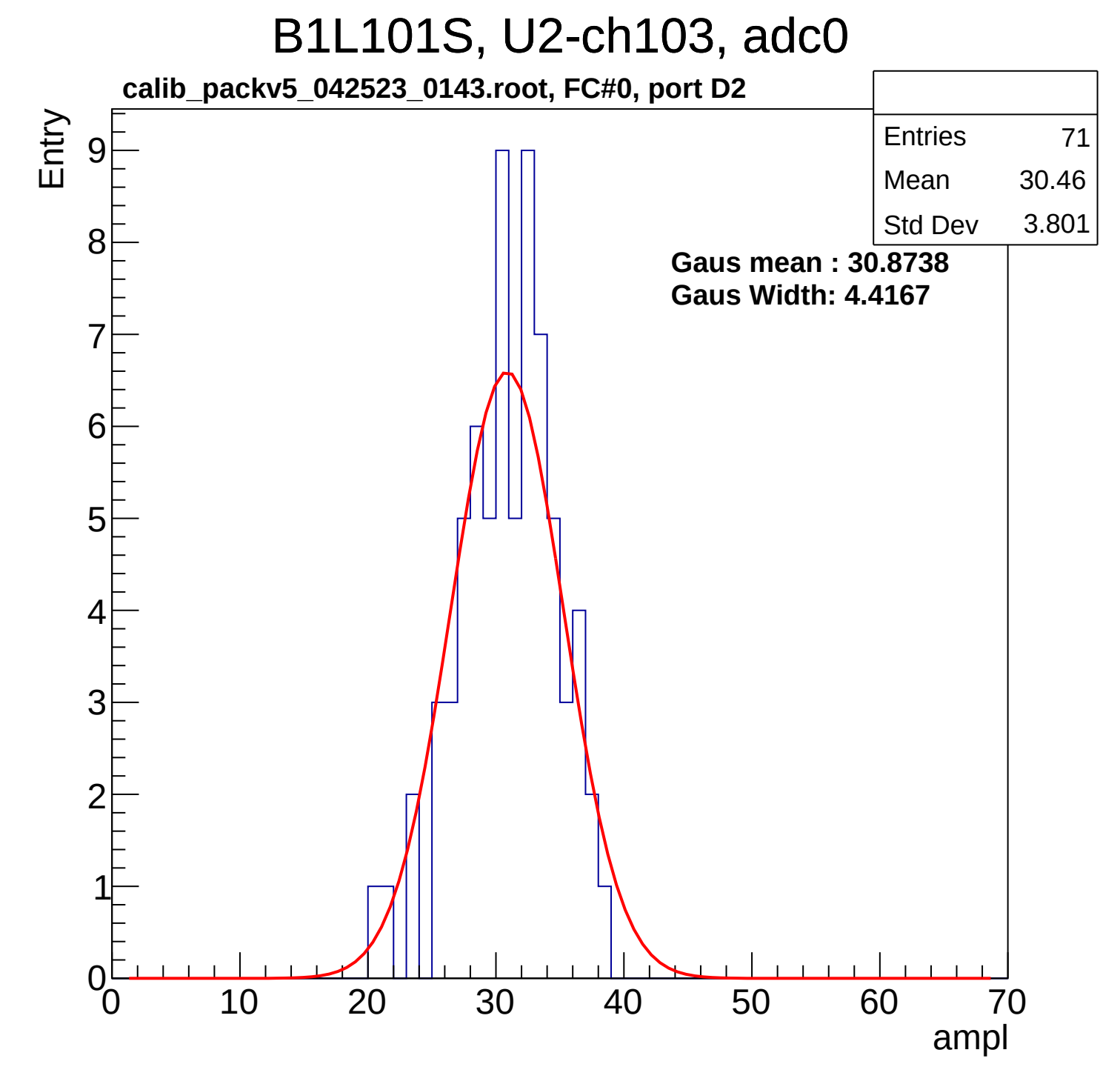

B1L101S, U2-ch102, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 47.15
Std Dev 3.419
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

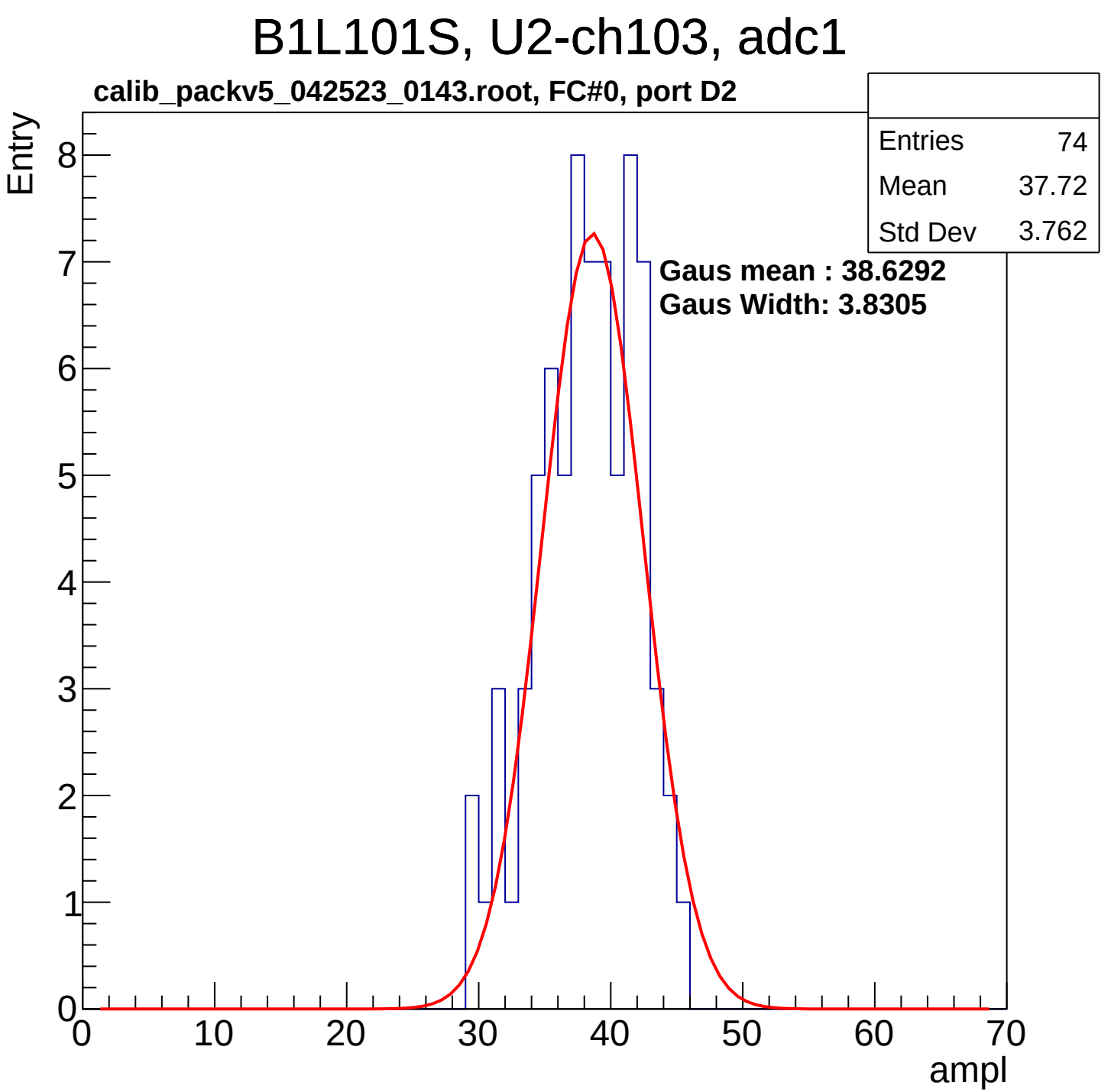

B1L101S, U2-ch102, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 52.36
Std Dev 3.812
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

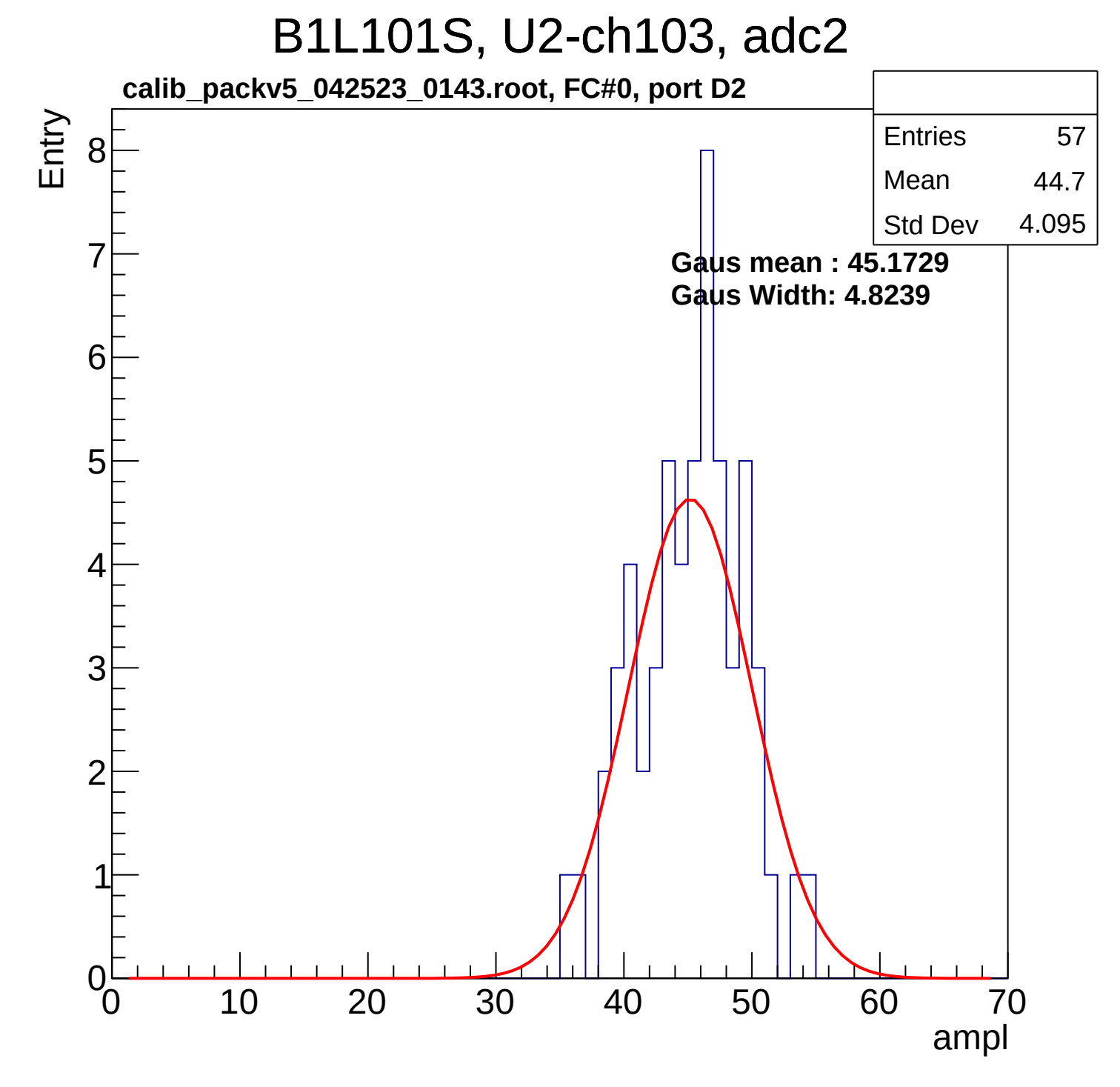

B1L101S, U2-ch102, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 57.67
Std Dev 3.321
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

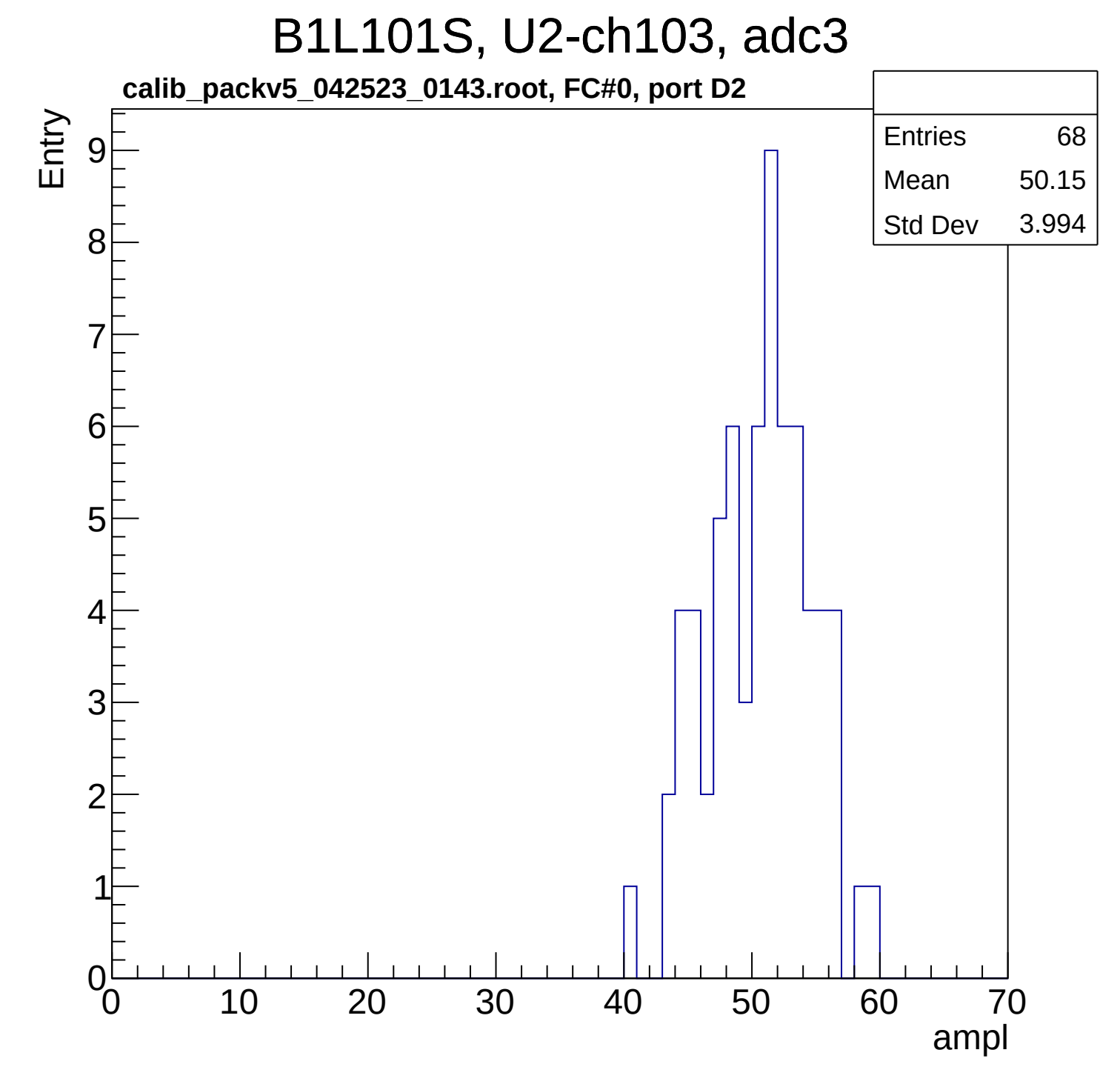

B1L101S, U2-ch102, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 23
Mean 60.78
Std Dev 1.977
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

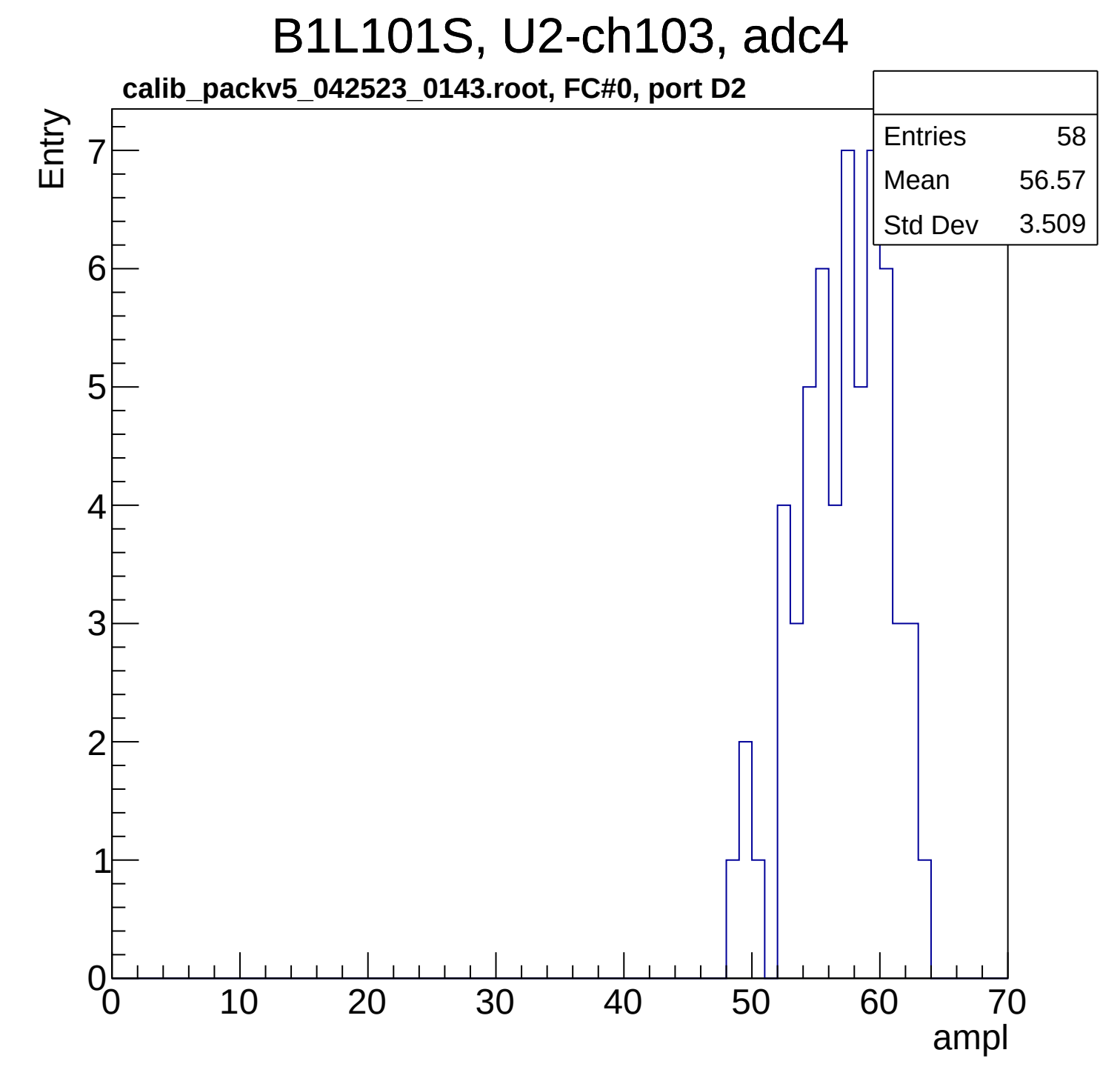

B1L101S, U2-ch102, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 25
Std Dev 30.62
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

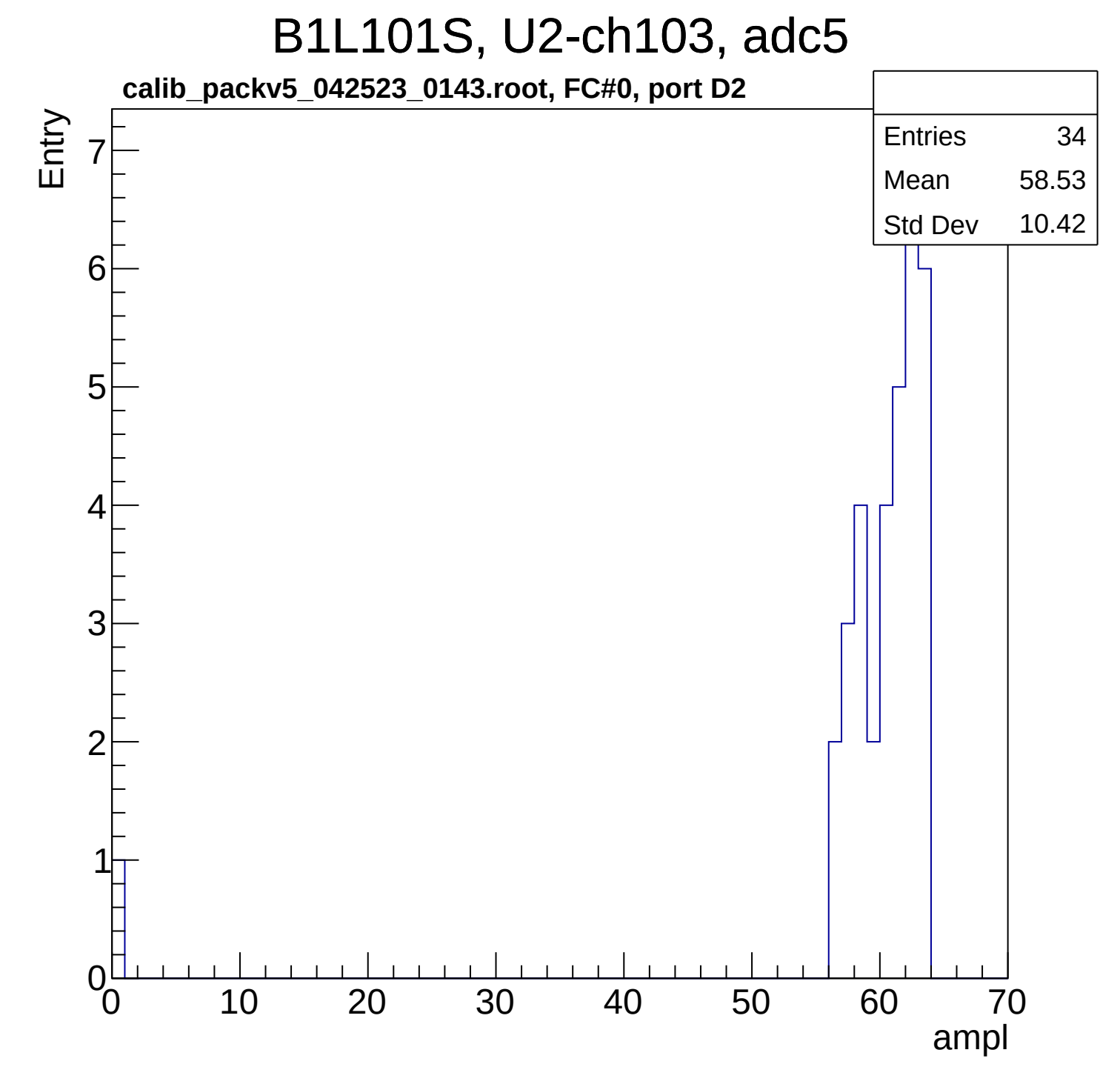

B1L101S, U2-ch103, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 30.46
Std Dev 3.801
Gaus mean : 30.8738
Gaus Width: 4.4167
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

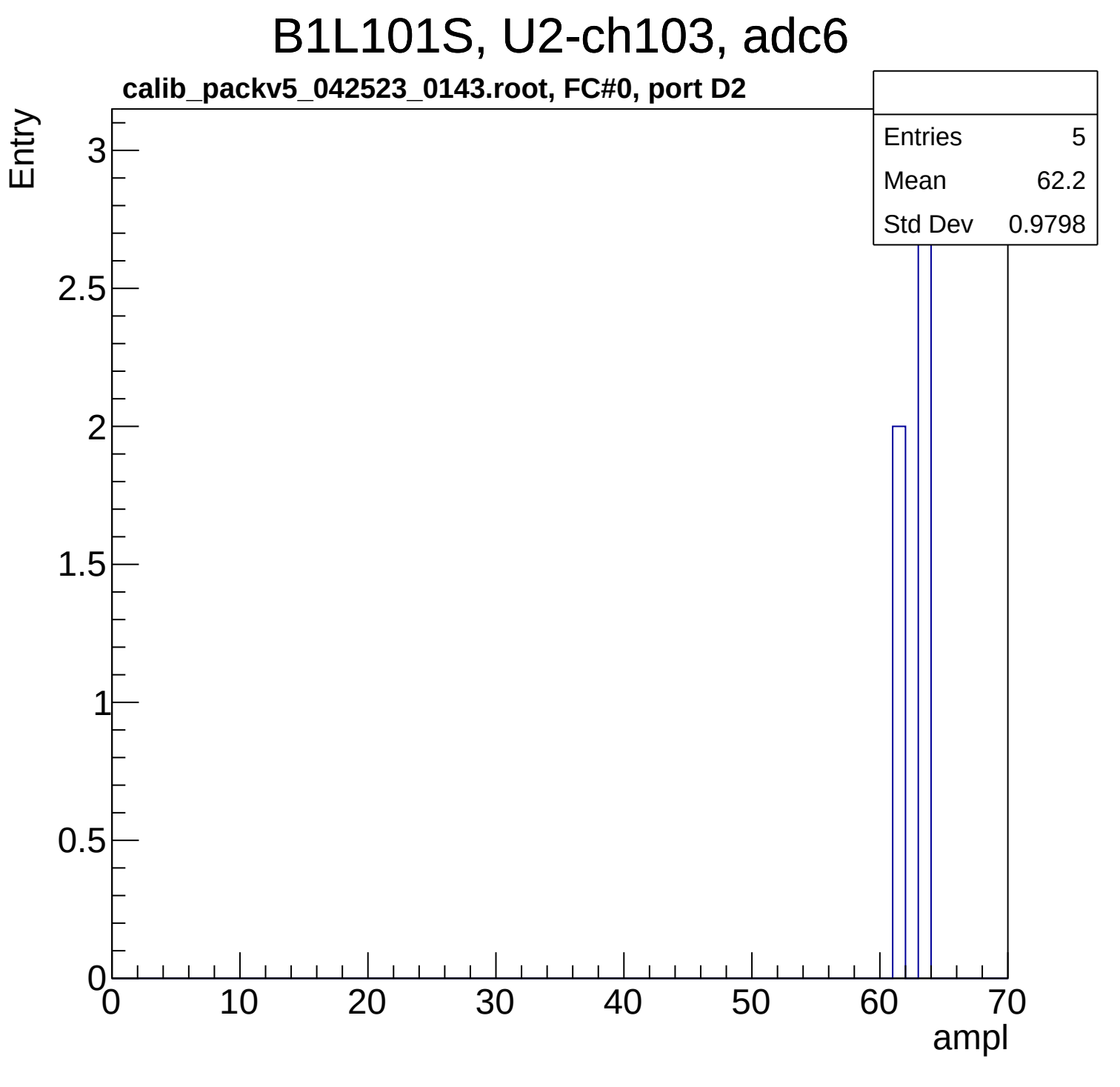

B1L101S, U2-ch103, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 37.72
Std Dev 3.762
Gaus mean : 38.6292
Gaus Width: 3.8305
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

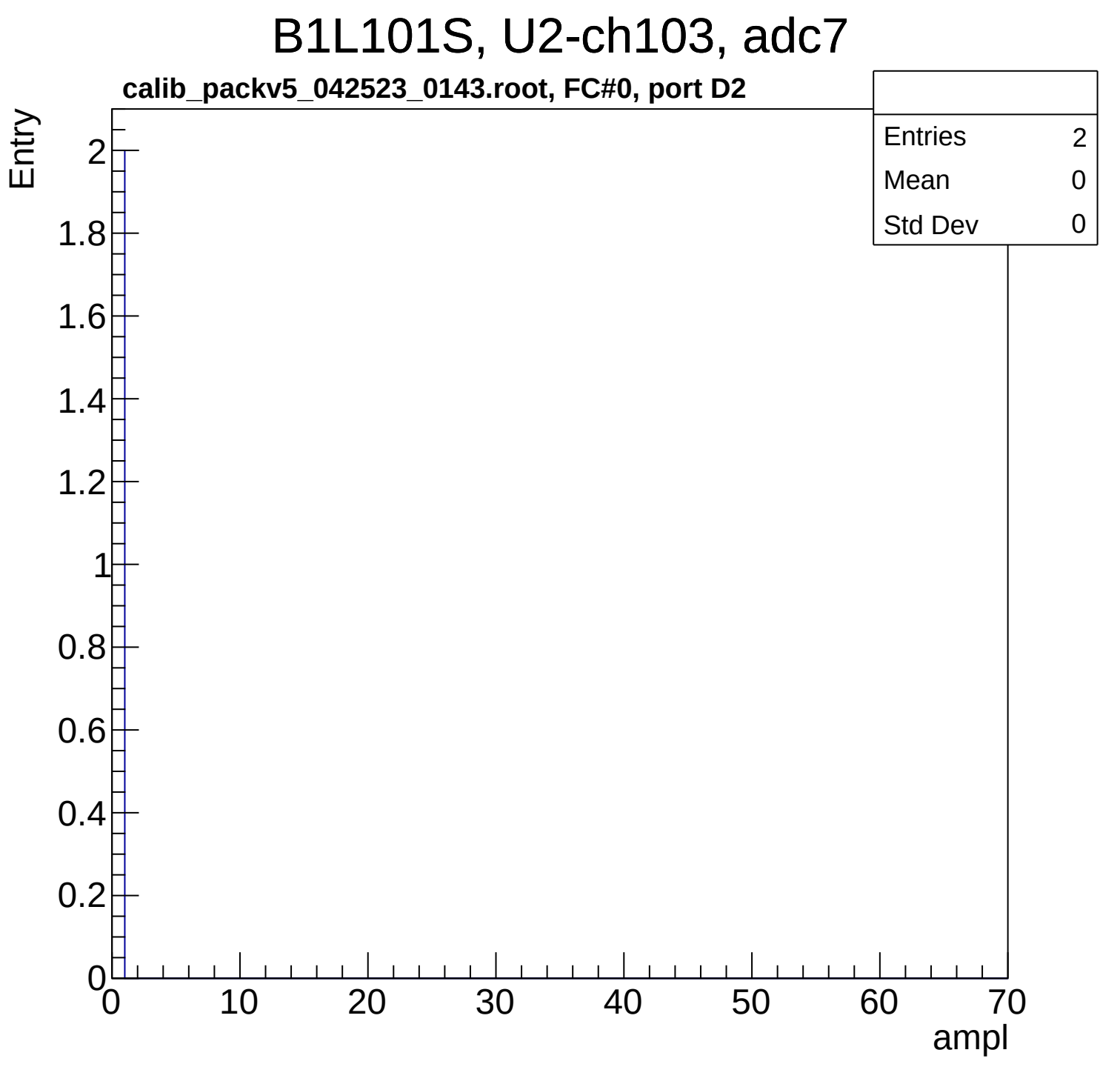

B1L101S, U2-ch103, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 44.7
Std Dev 4.095
Gaus mean : 45.1729
Gaus Width: 4.8239
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

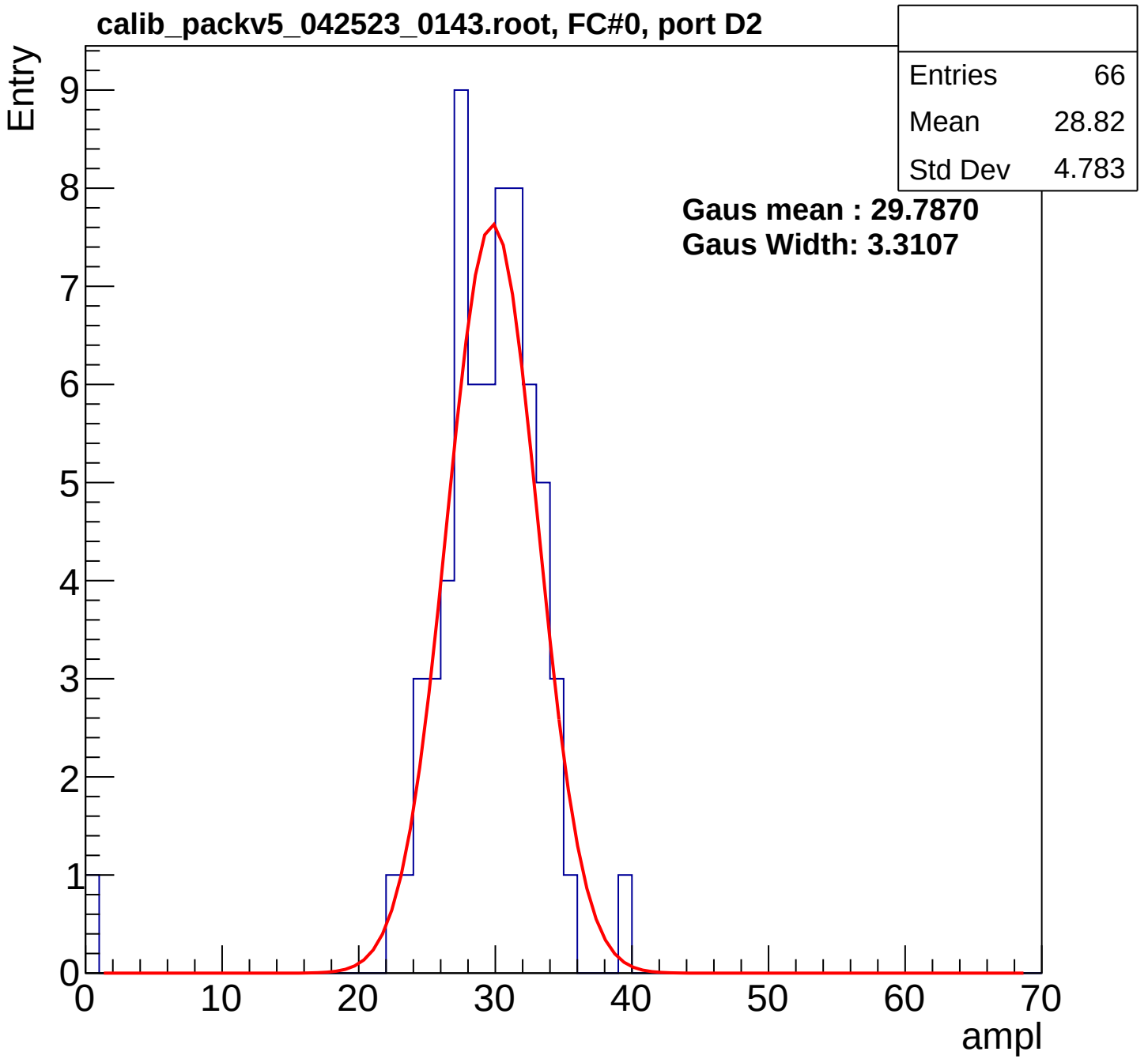

B1L101S, U2-ch103, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 50.15
Std Dev 3.994
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

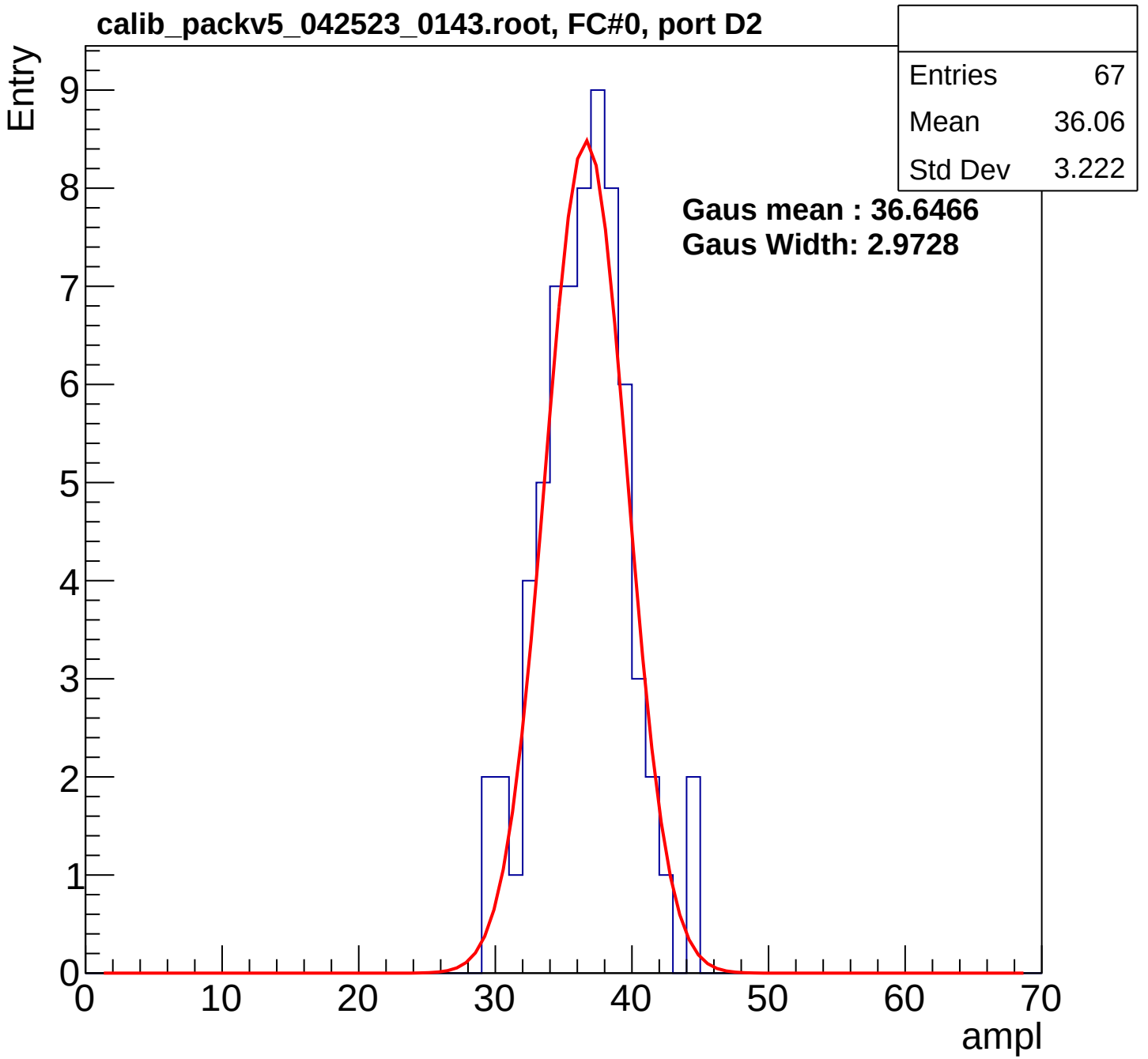

B1L101S, U2-ch103, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 56.57
Std Dev 3.509
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

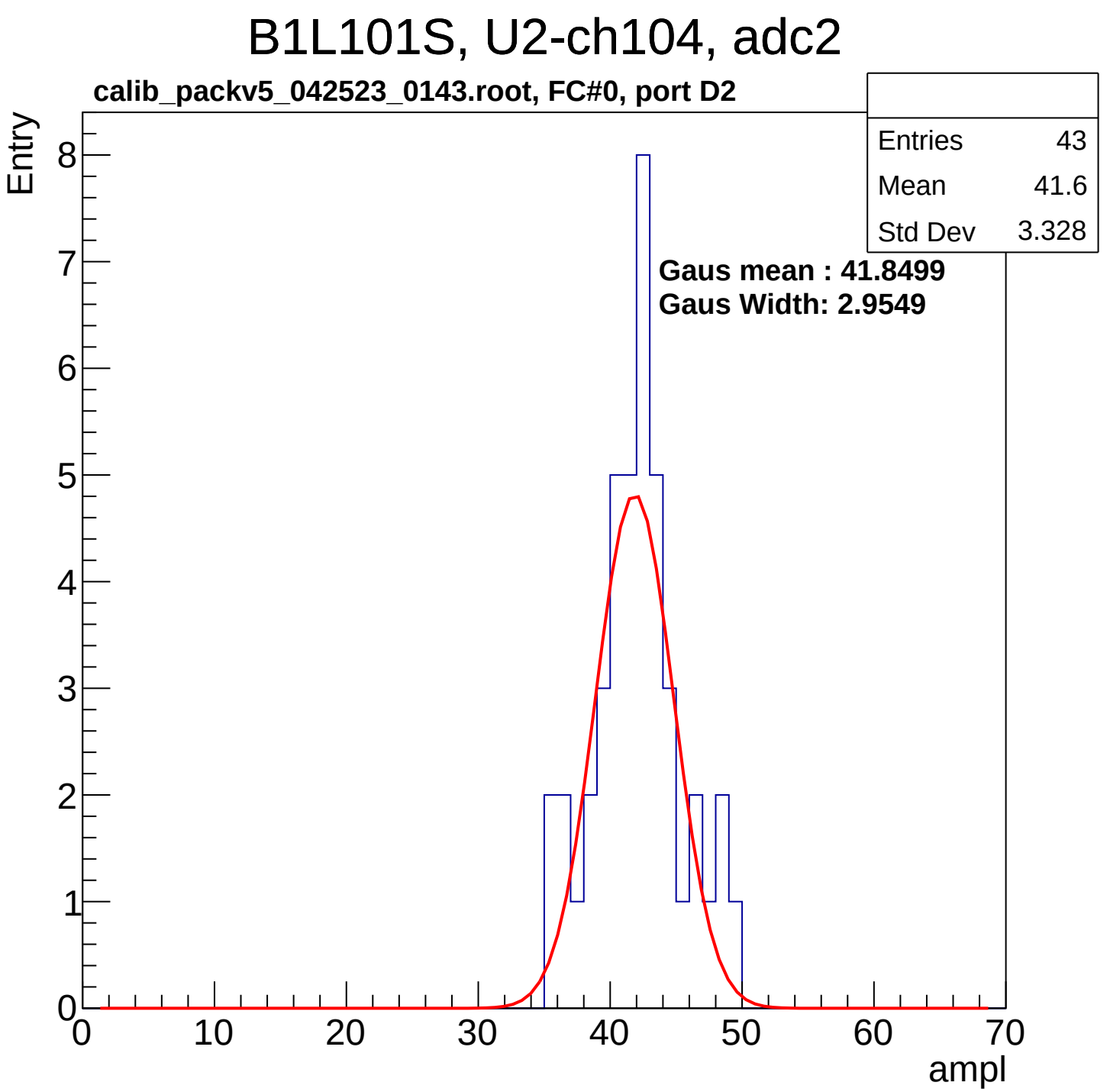

B1L101S, U2-ch103, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 34
Mean 58.53
Std Dev 10.42
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

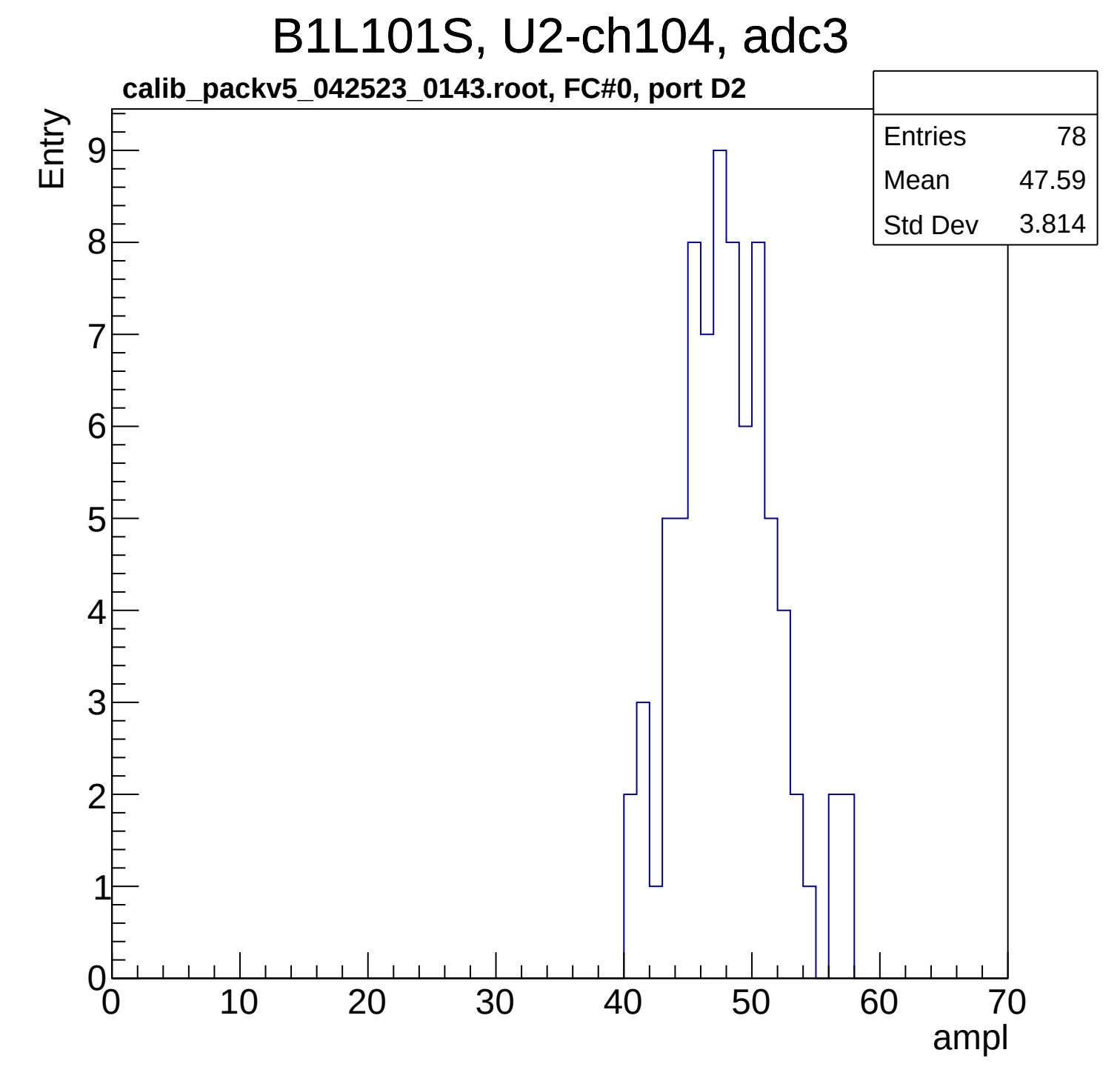

B1L101S, U2-ch103, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 62.2
Std Dev 0.9798
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

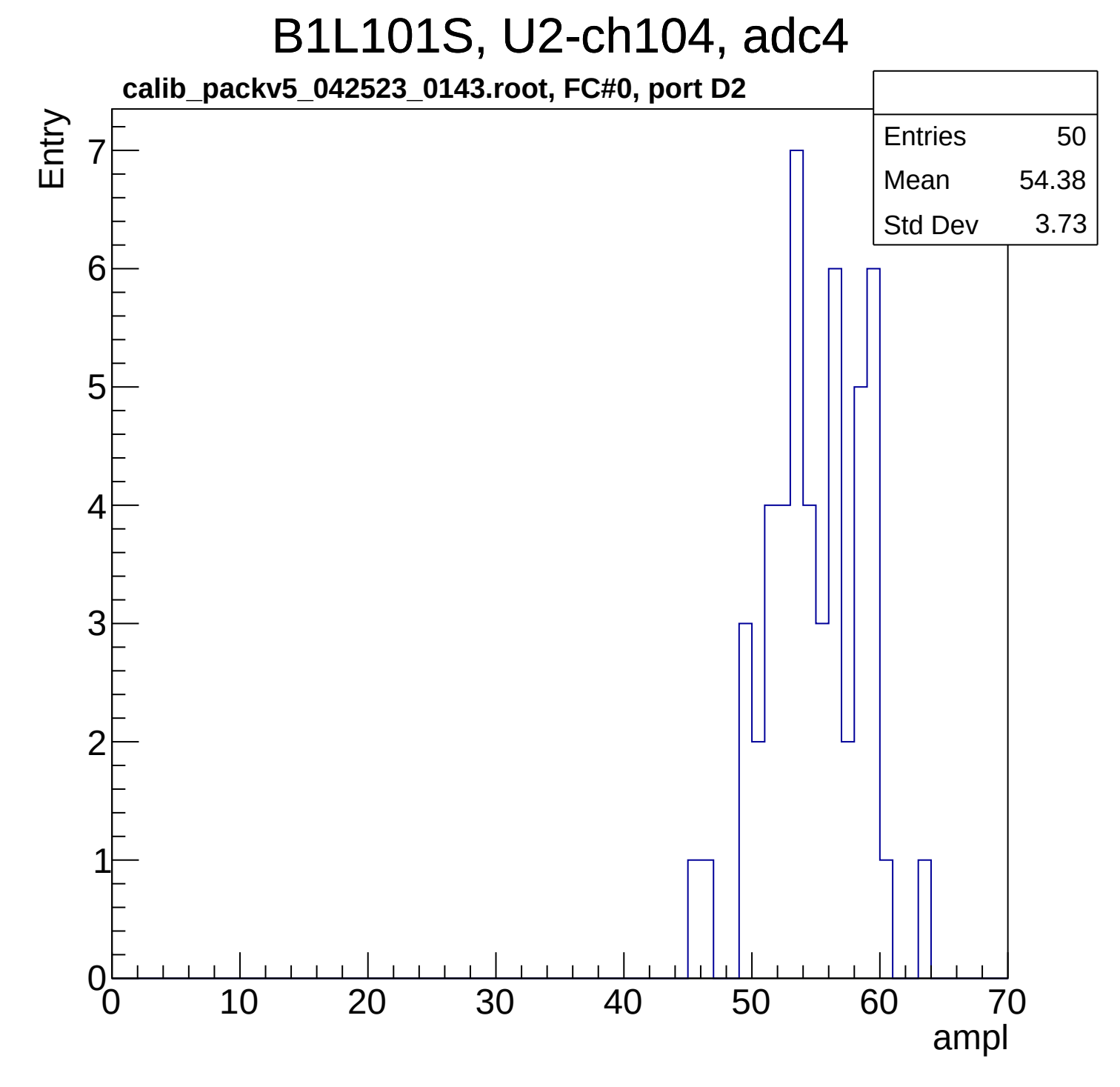

B1L101S, U2-ch103, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

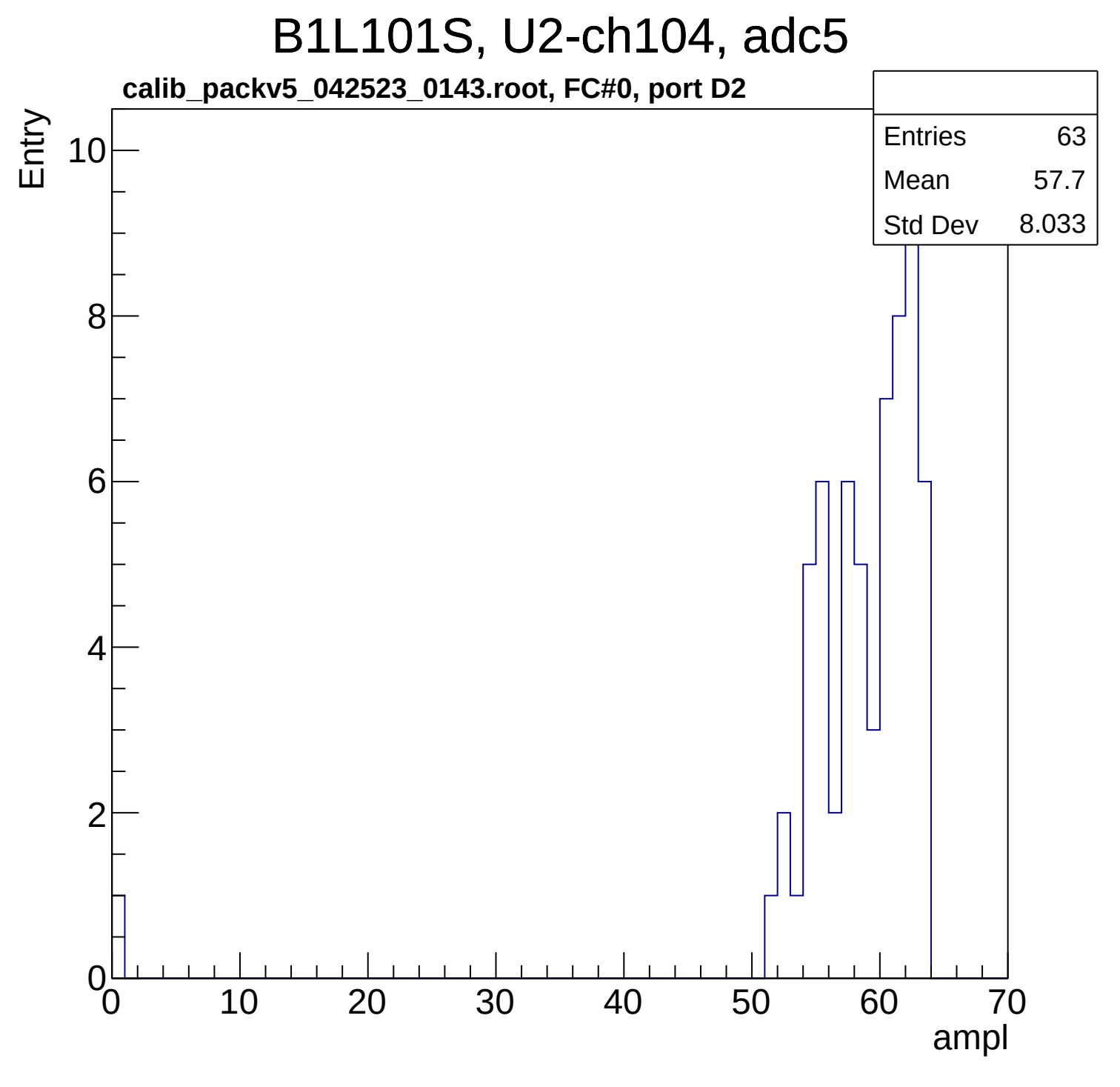

B1L101S, U2-ch104, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 28.82
Std Dev 4.783
Gaus mean : 29.7870
Gaus Width: 3.3107
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

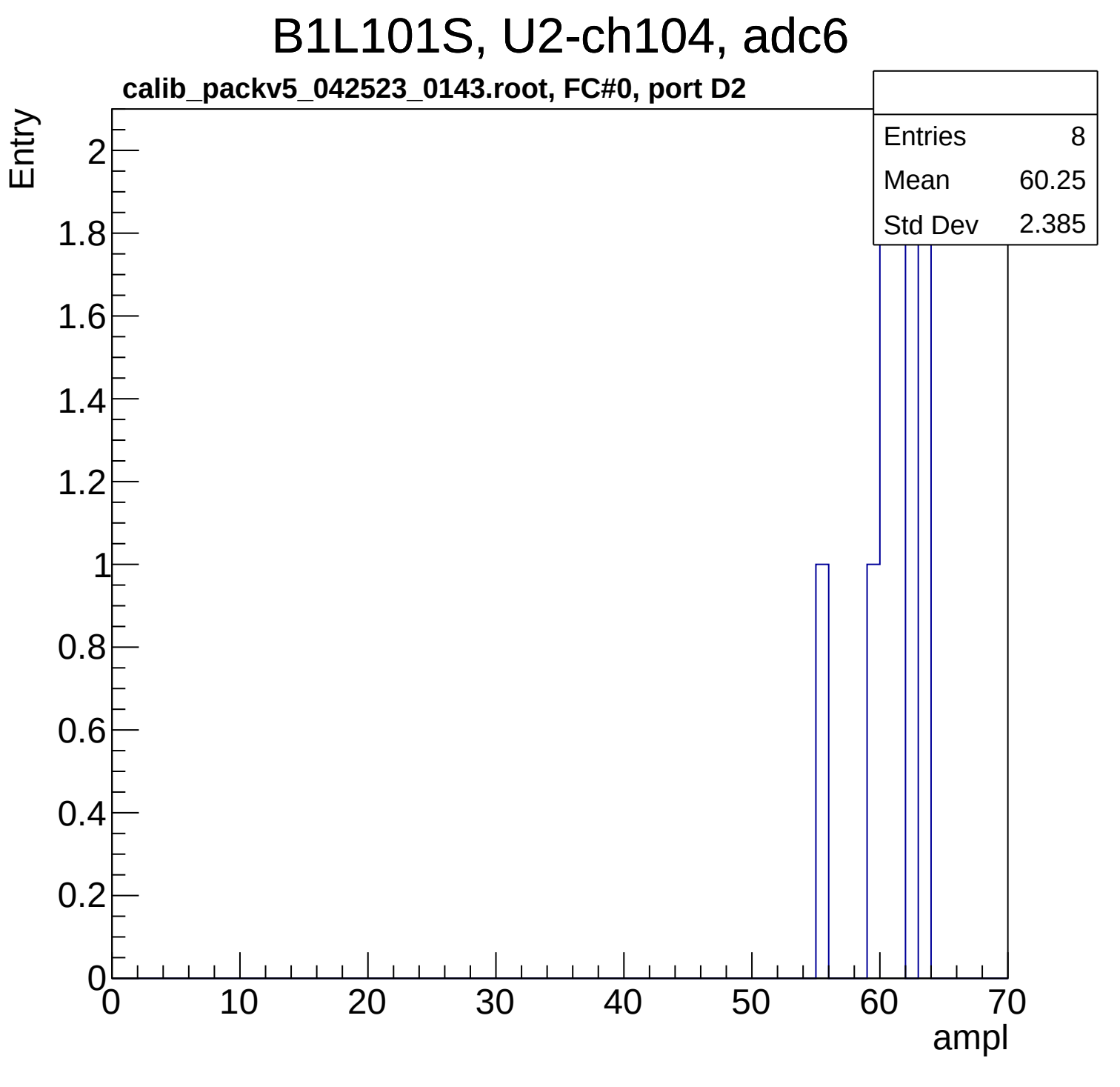

B1L101S, U2-ch104, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 36.06
Std Dev 3.222
Gaus mean : 36.6466
Gaus Width: 2.9728
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

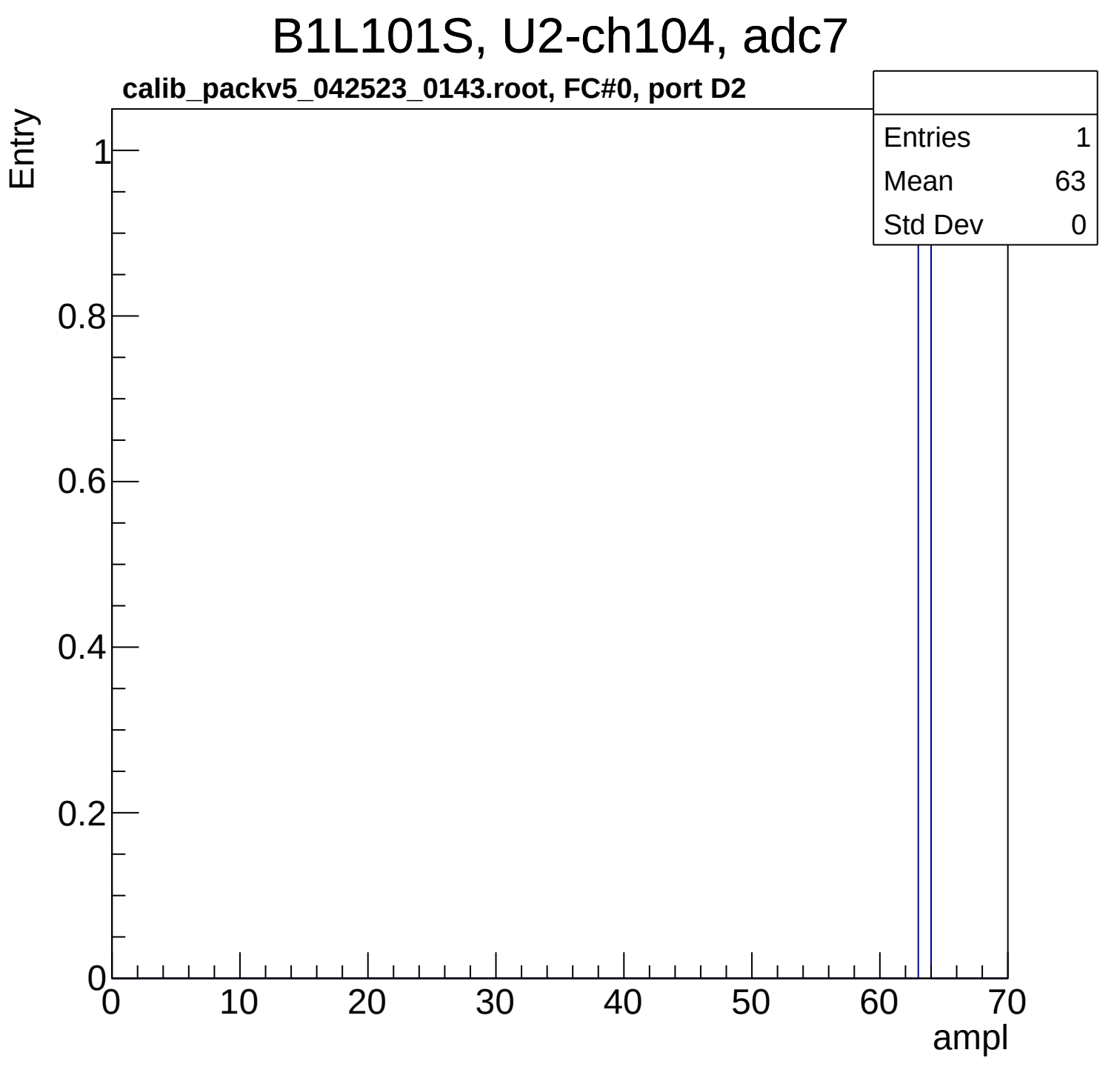

B1L101S, U2-ch104, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 43
Mean 41.6
Std Dev 3.328
Gaus mean : 41.8499
Gaus Width: 2.9549
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

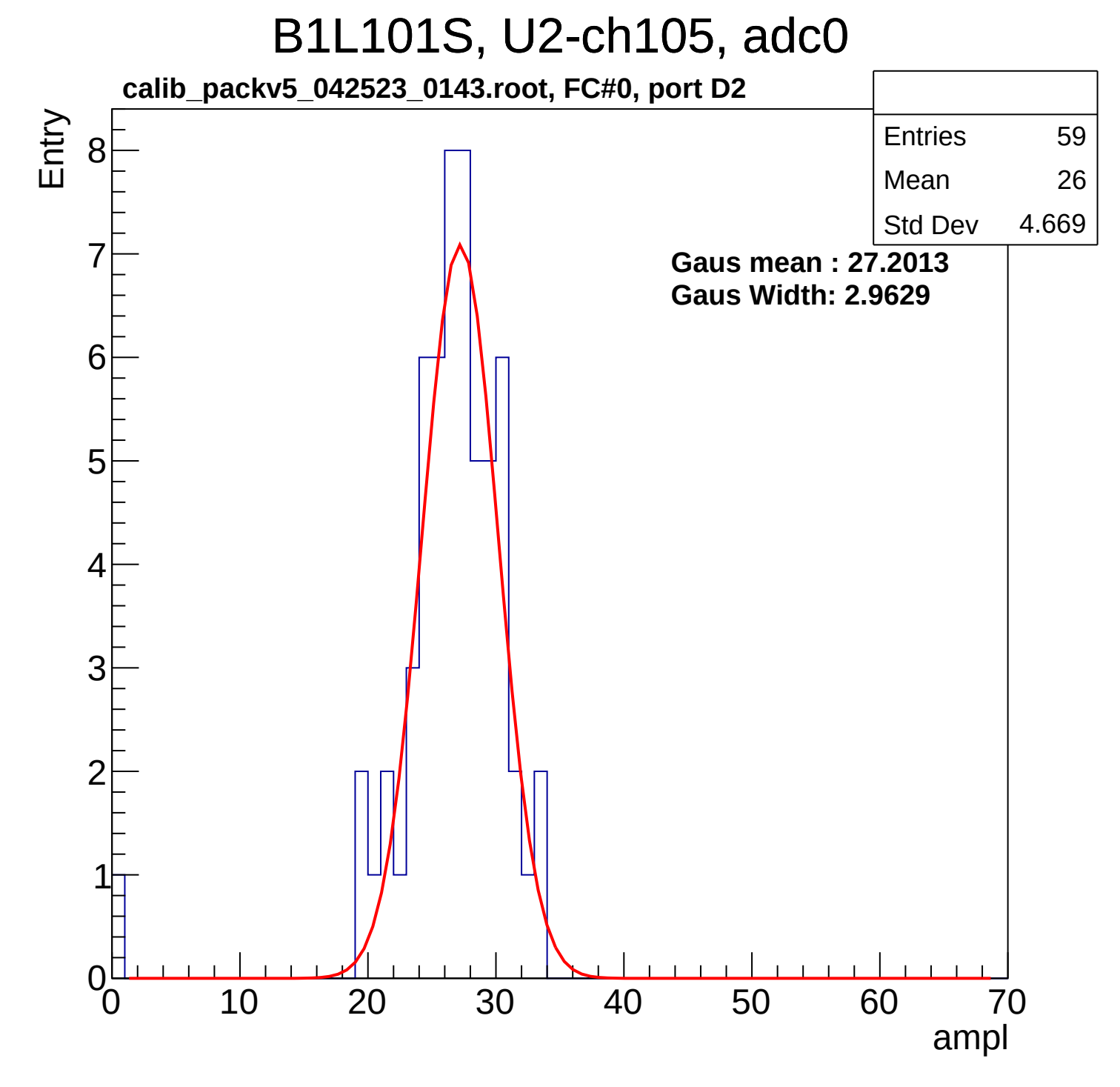

B1L101S, U2-ch104, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 47.59
Std Dev 3.814
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

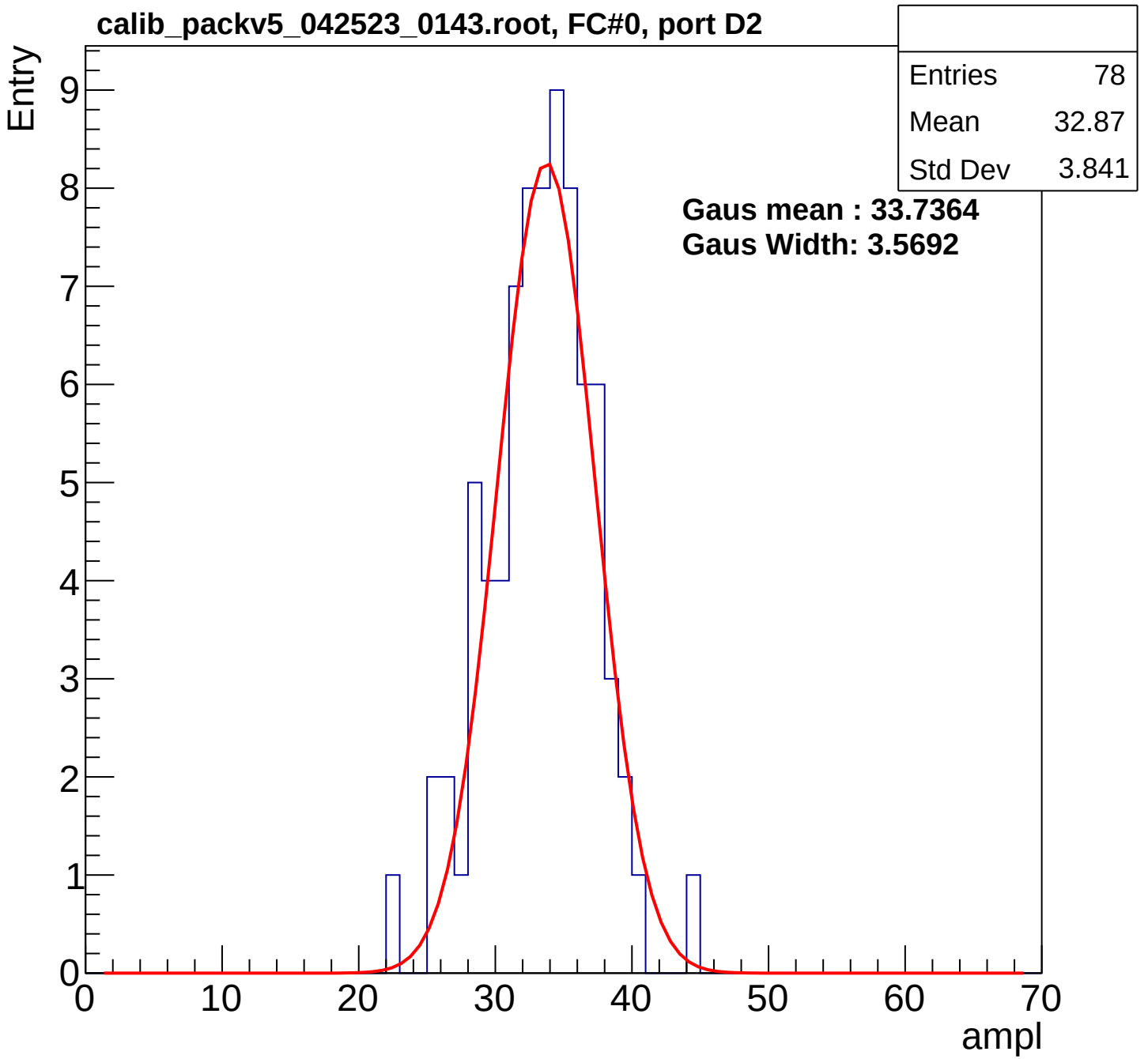

B1L101S, U2-ch104, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 54.38
Std Dev 3.73
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

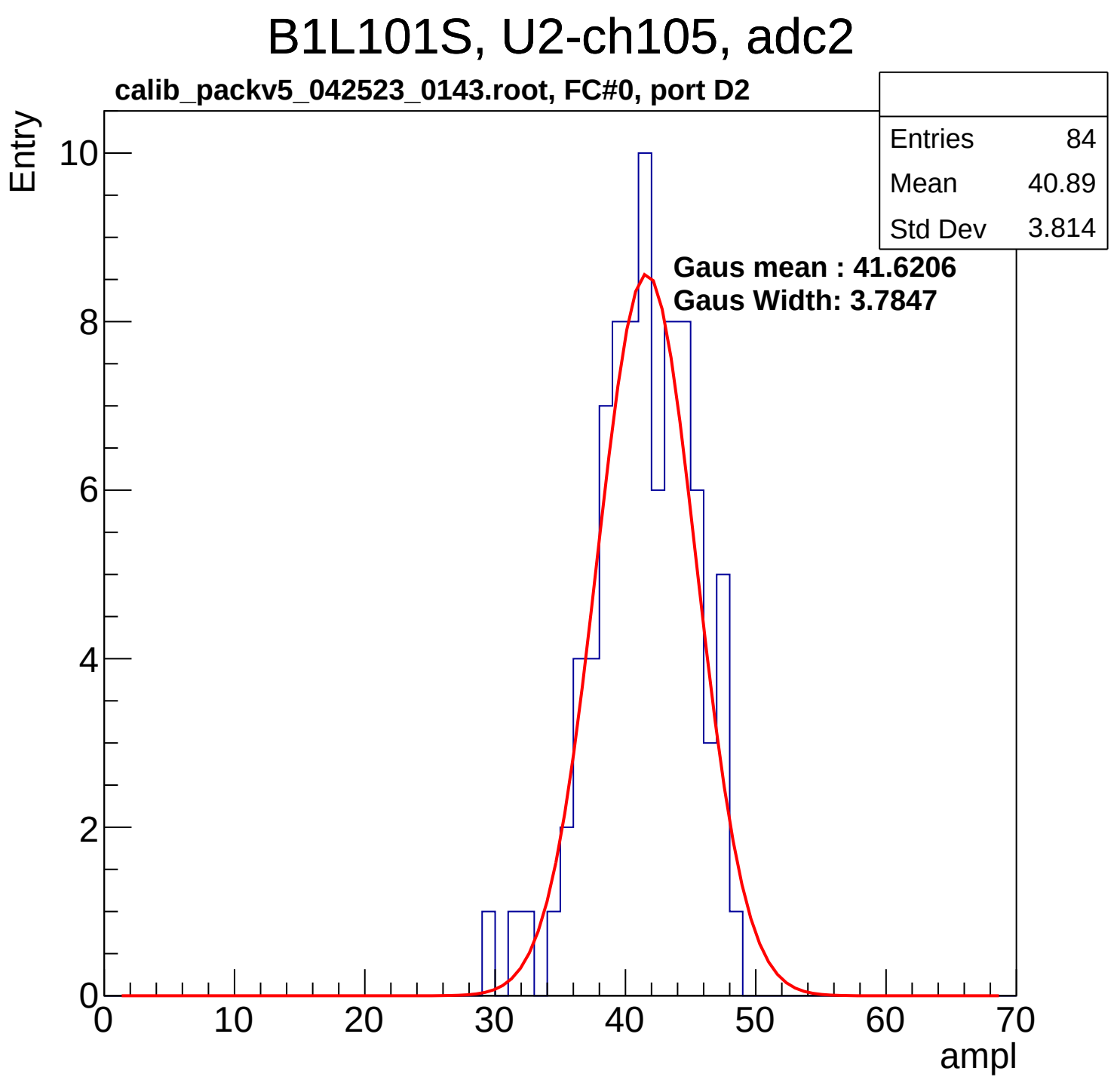

B1L101S, U2-ch104, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 57.7
Std Dev 8.033
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

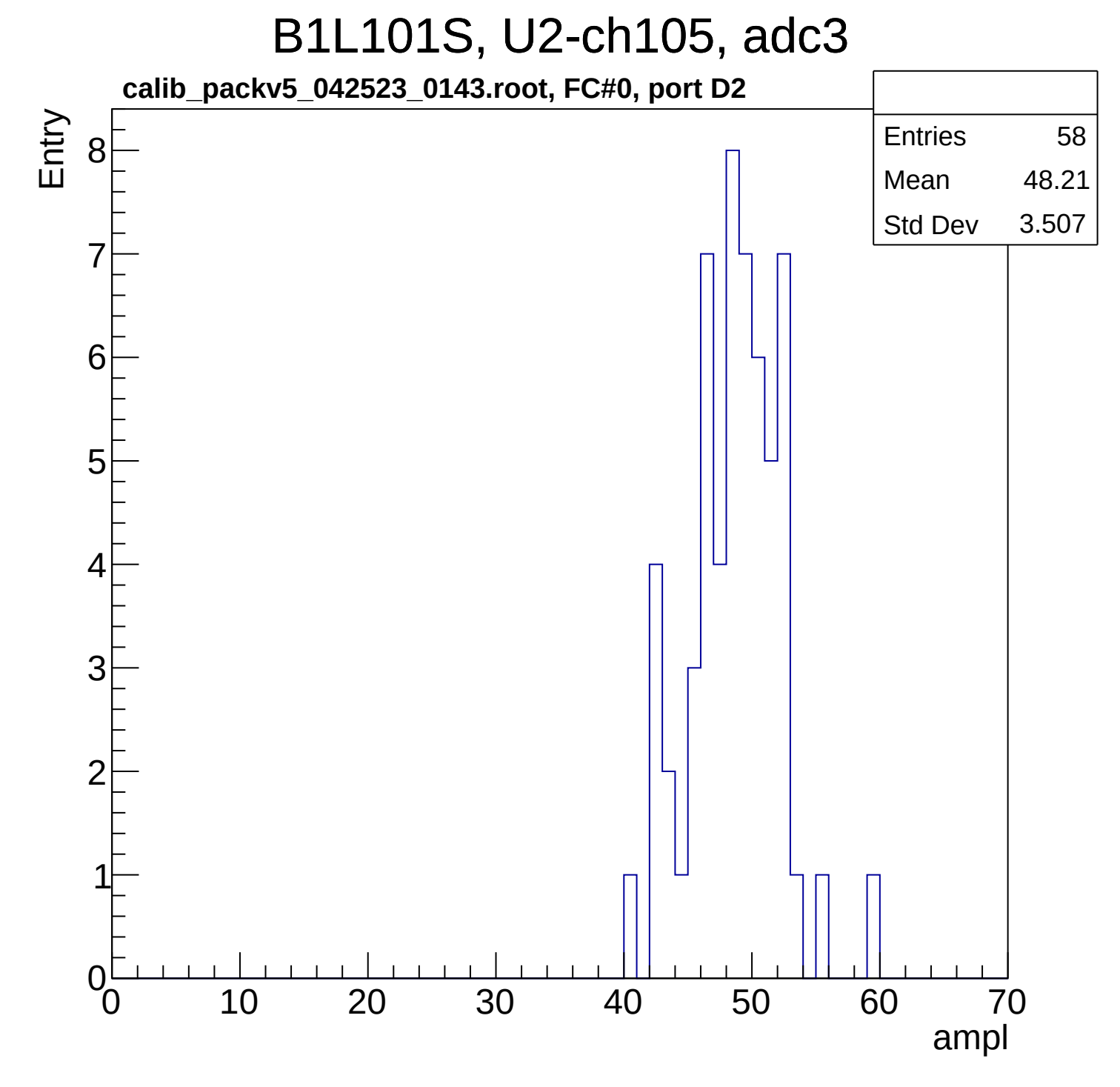

B1L101S, U2-ch104, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 8
Mean 60.25
Std Dev 2.385
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

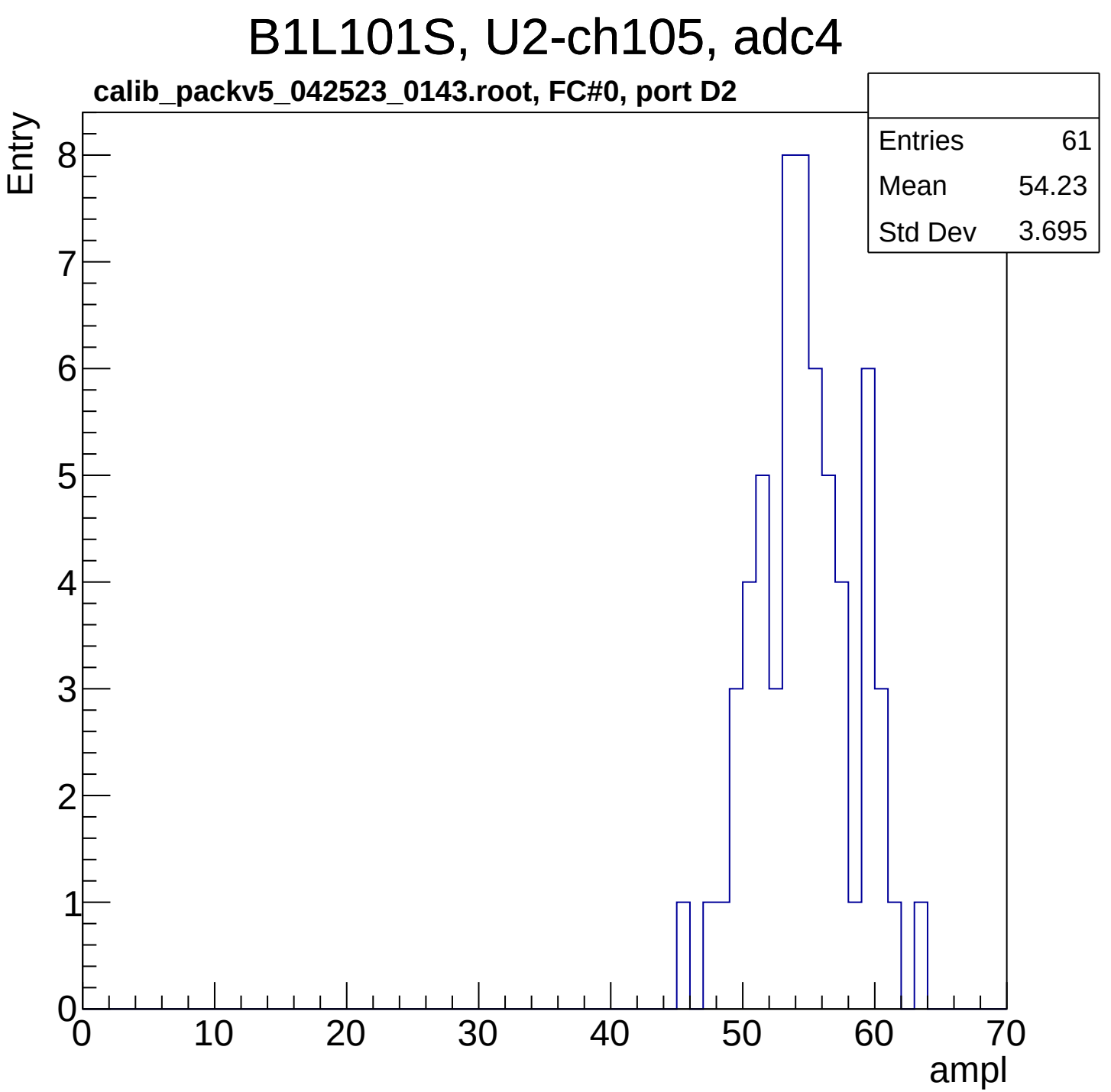

B1L101S, U2-ch104, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

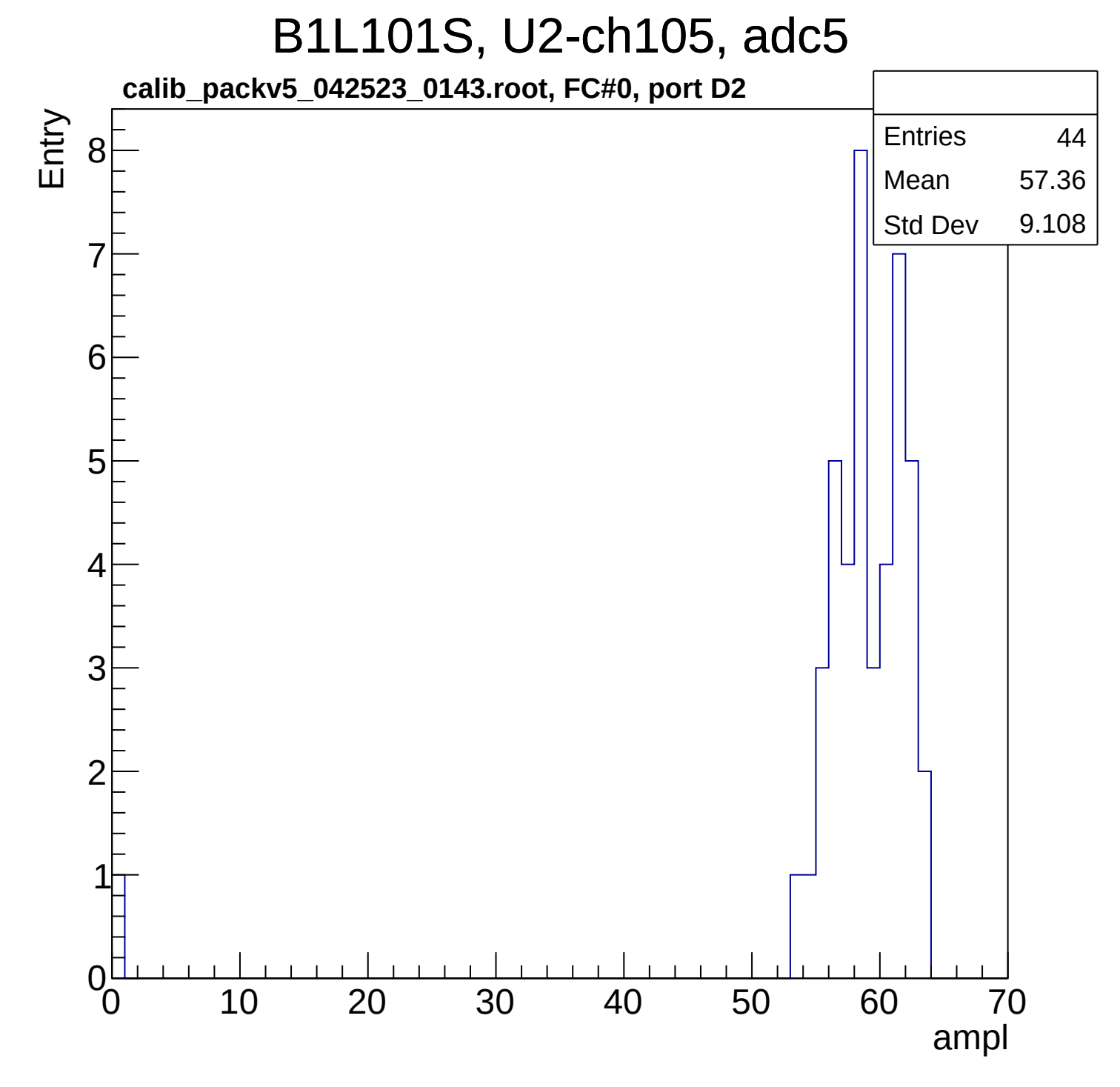

B1L101S, U2-ch105, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 26
Std Dev 4.669
Gaus mean : 27.2013
Gaus Width: 2.9629
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

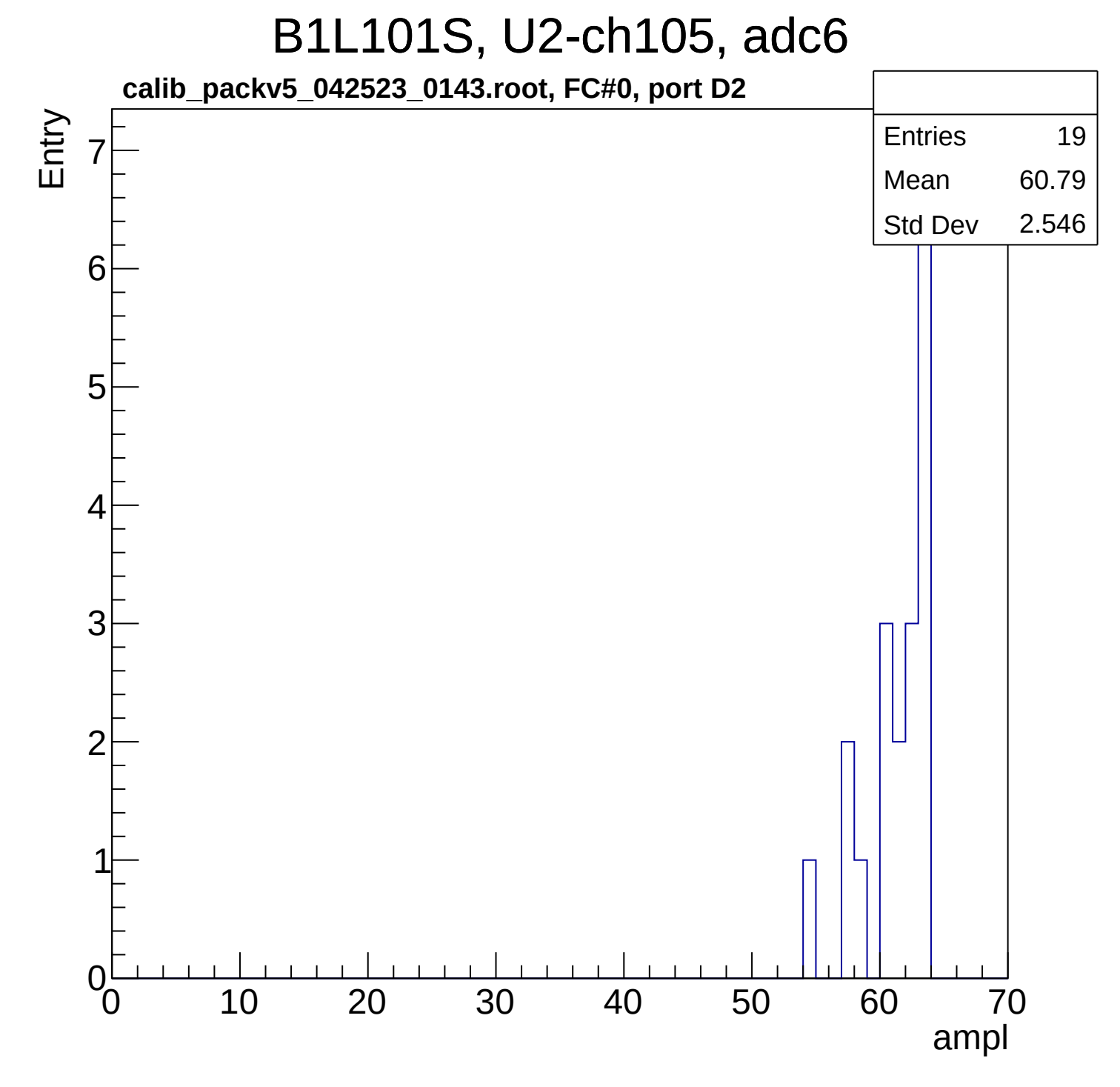

B1L101S, U2-ch105, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 32.87
Std Dev 3.841
Gaus mean : 33.7364
Gaus Width: 3.5692
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

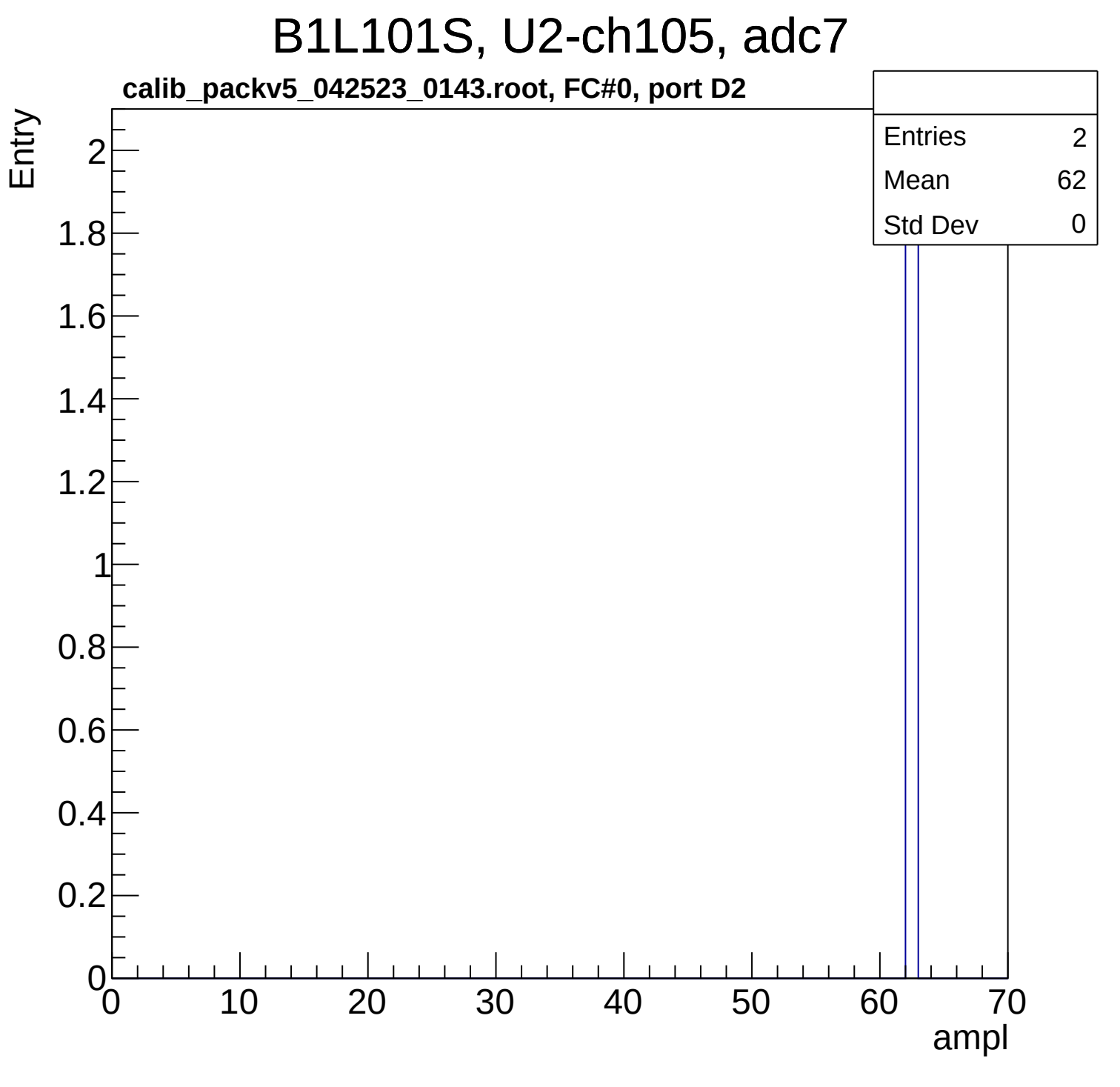

B1L101S, U2-ch105, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 84
Mean 40.89
Std Dev 3.814
Gaus mean : 41.6206
Gaus Width: 3.7847
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

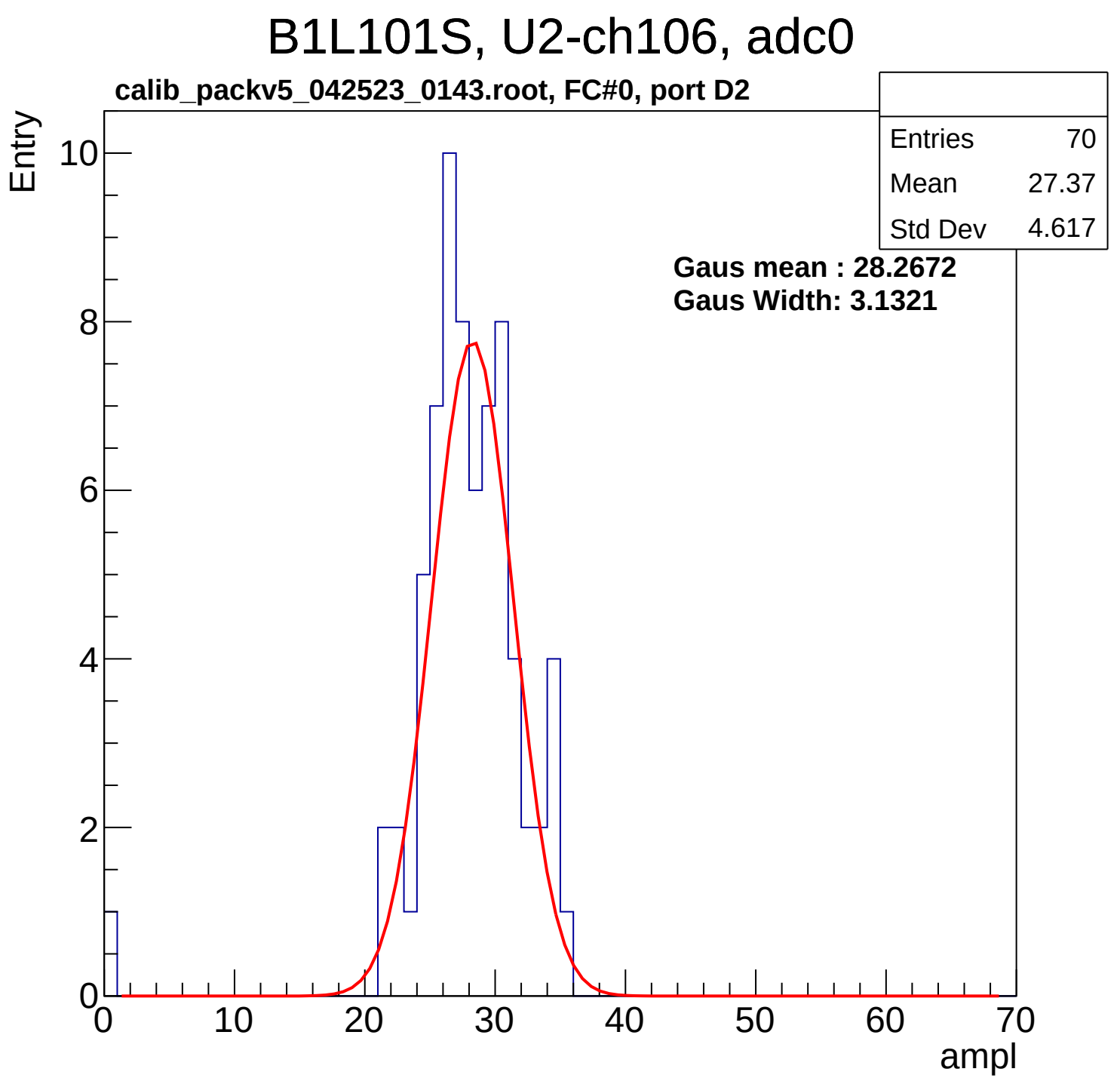

B1L101S, U2-ch105, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 48.21
Std Dev 3.507
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

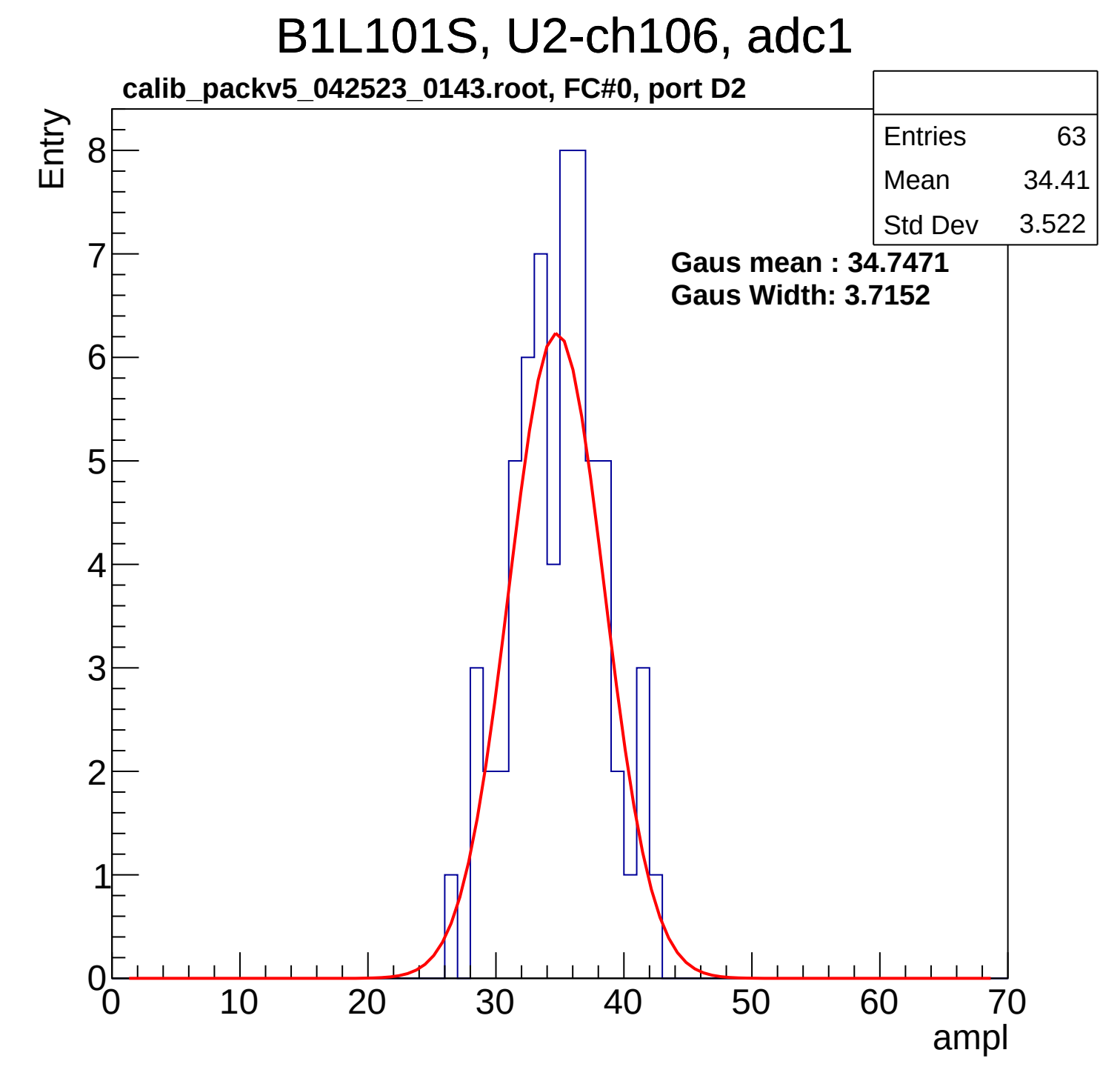

B1L101S, U2-ch105, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 54.23
Std Dev 3.695
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

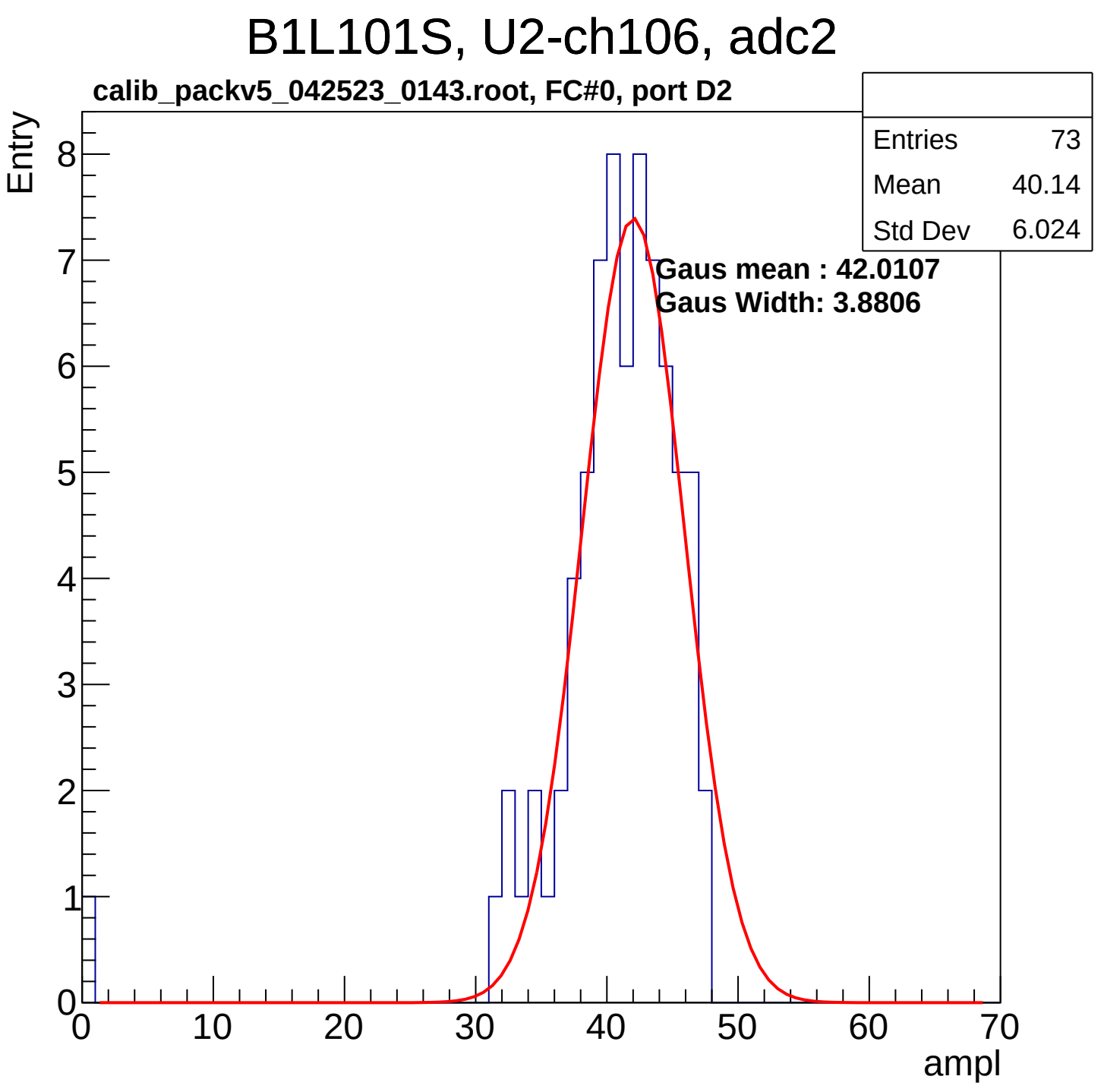

B1L101S, U2-ch105, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 44
Mean 57.36
Std Dev 9.108
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

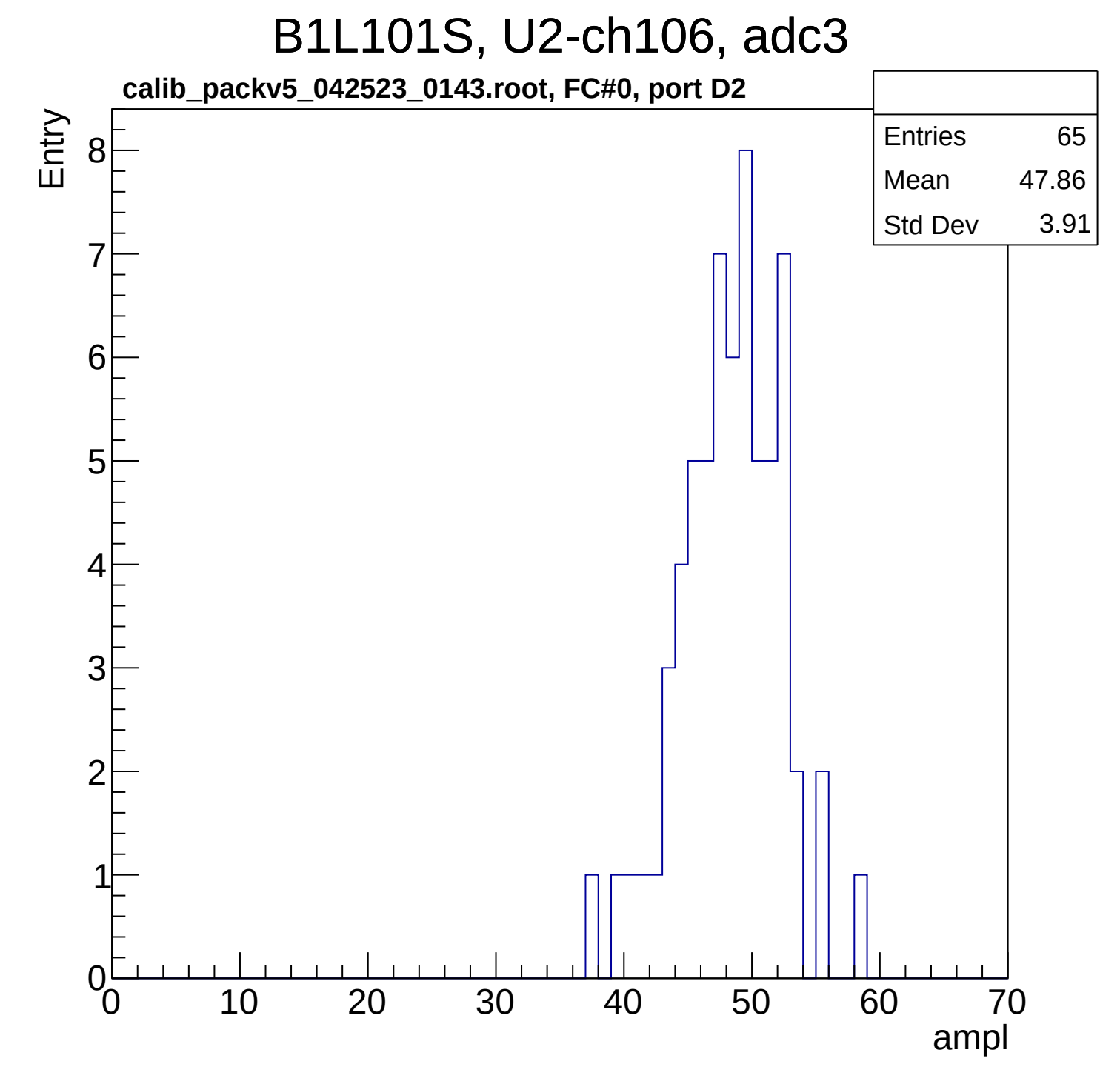

B1L101S, U2-ch105, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 19
Mean 60.79
Std Dev 2.546
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

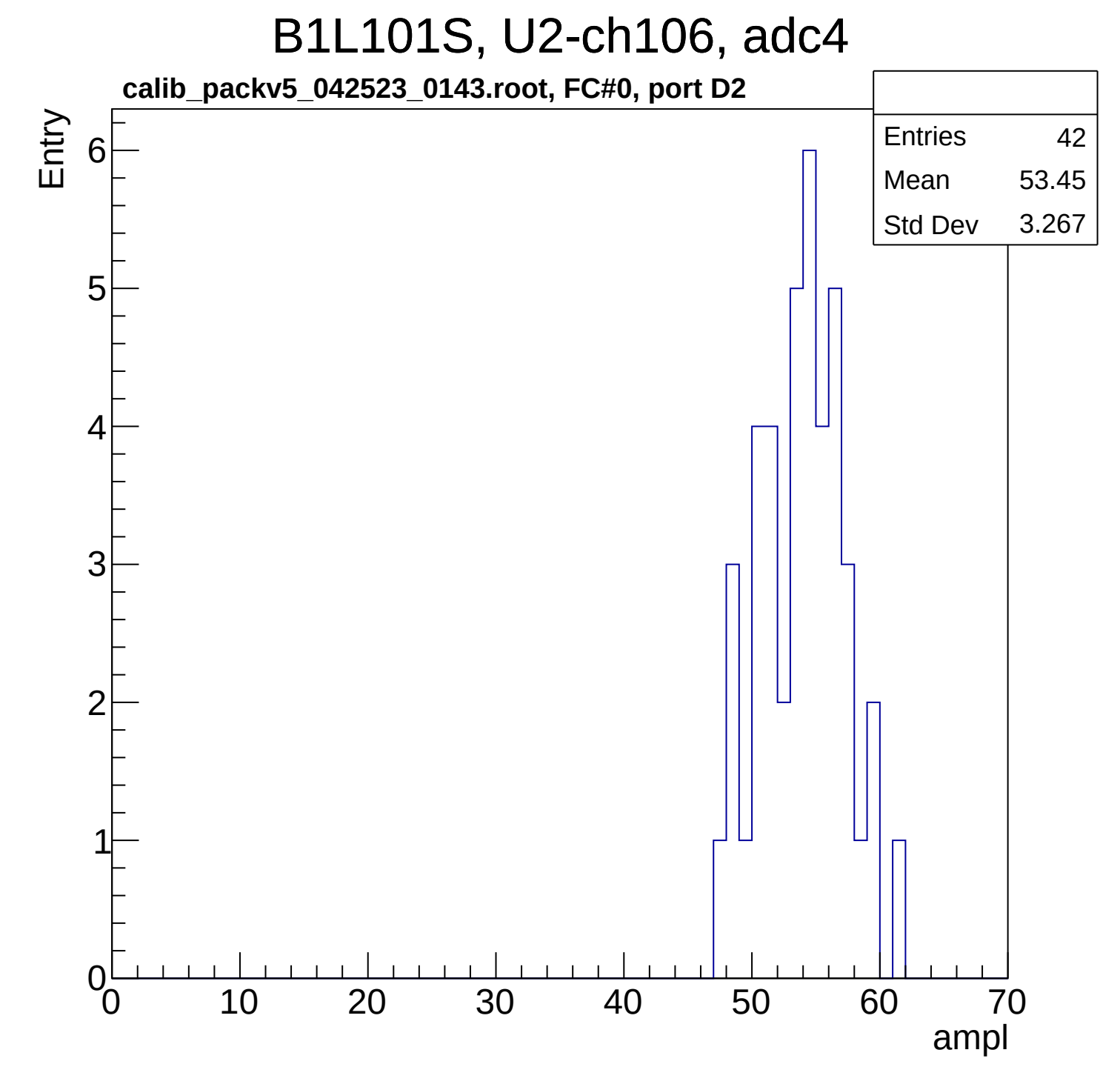

B1L101S, U2-ch105, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 62
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

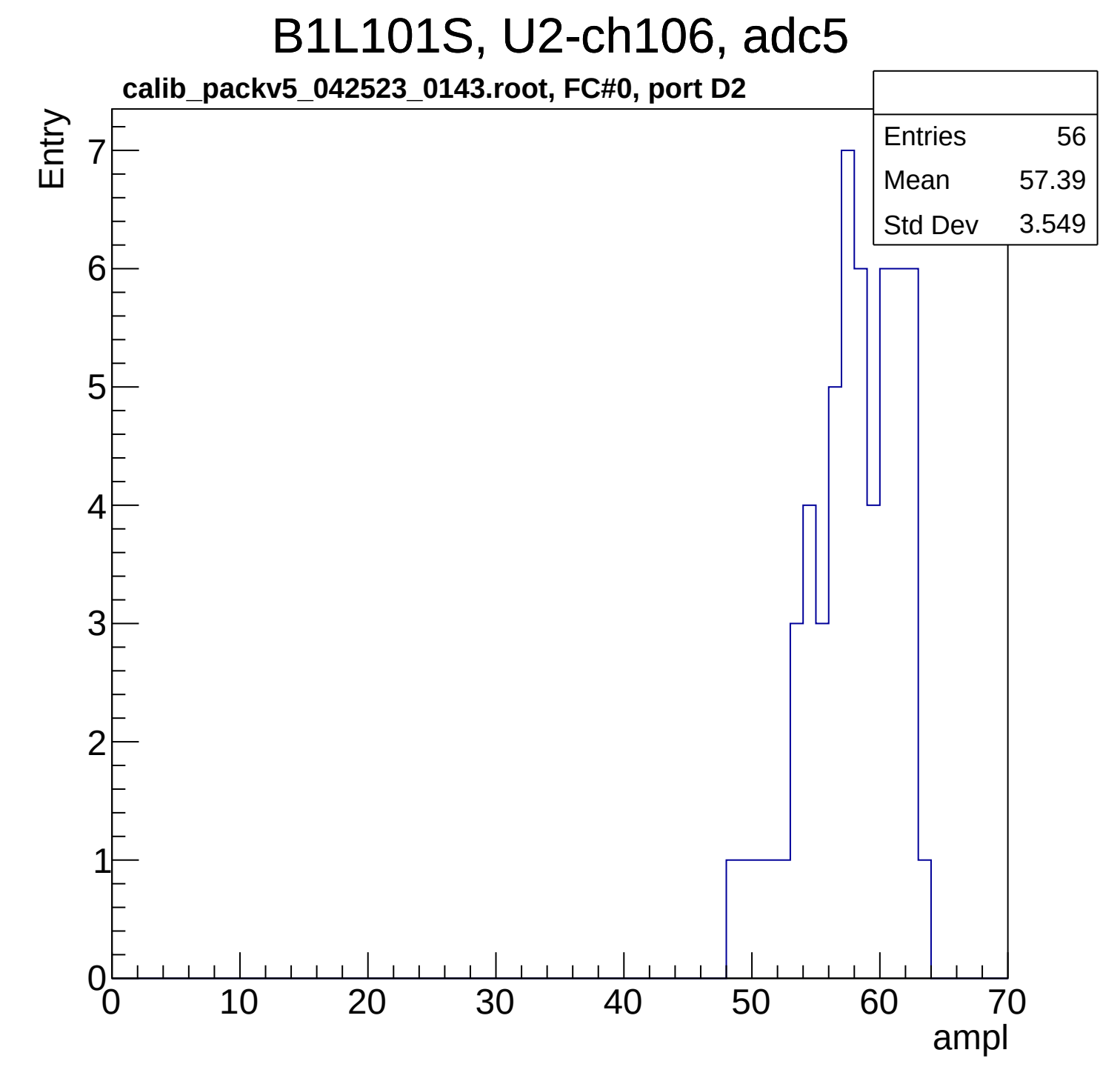

B1L101S, U2-ch106, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 27.37
Std Dev 4.617
Gaus mean : 28.2672
Gaus Width: 3.1321
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

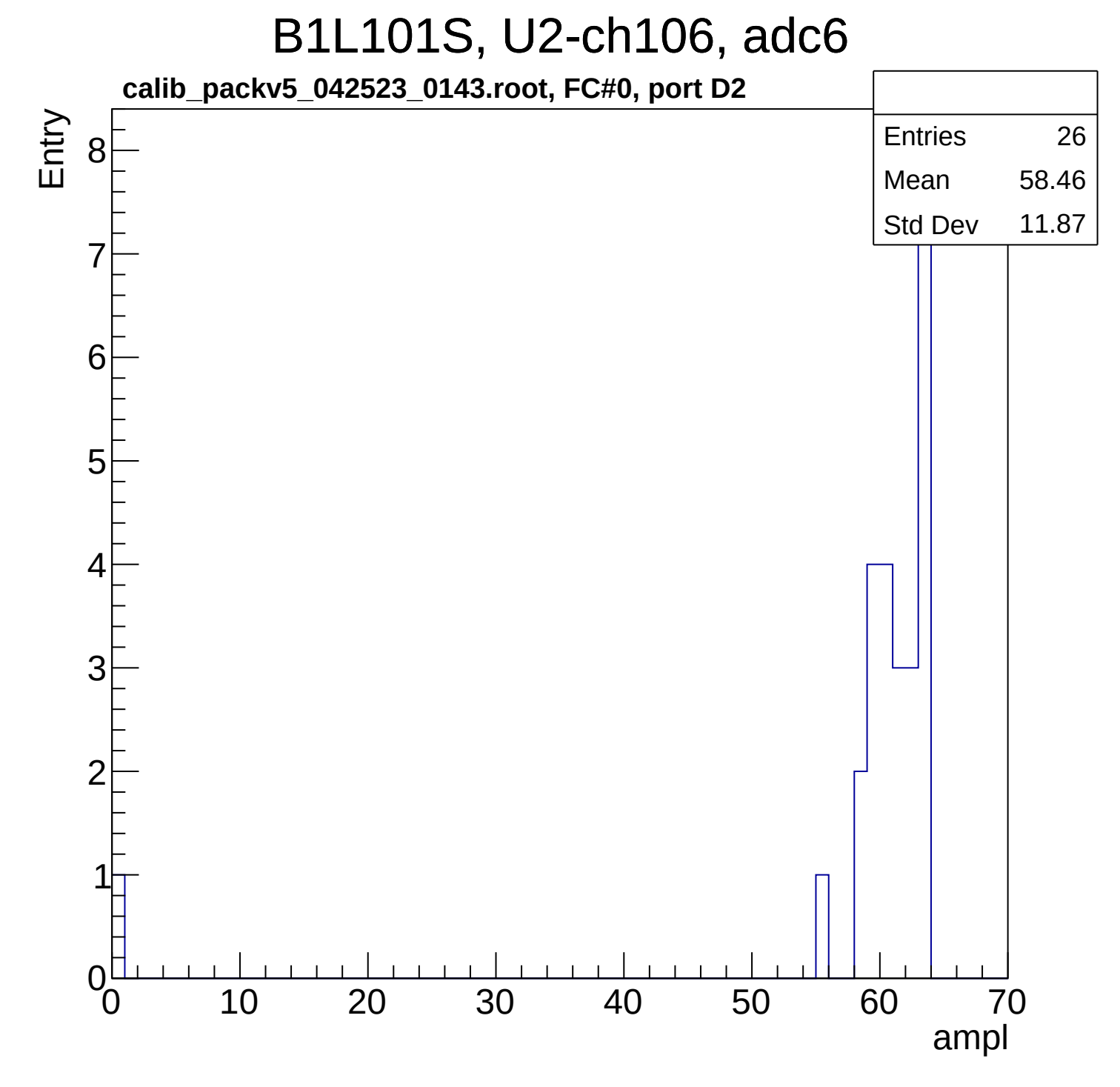

B1L101S, U2-ch106, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 34.41
Std Dev 3.522
Gaus mean : 34.7471
Gaus Width: 3.7152
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

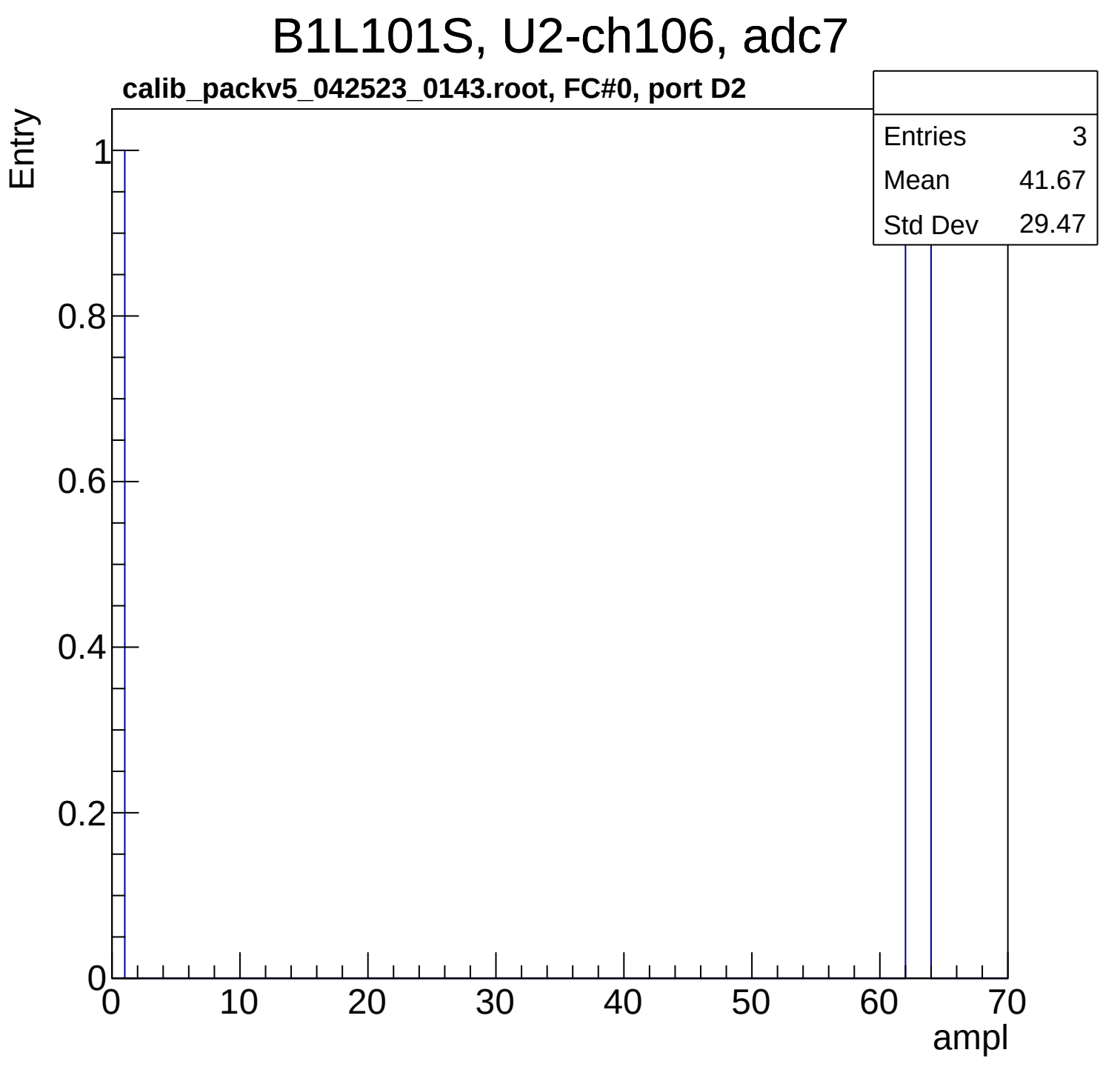

B1L101S, U2-ch106, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 40.14
Std Dev 6.024
Gaus mean : 42.0107
Gaus Width: 3.8806
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

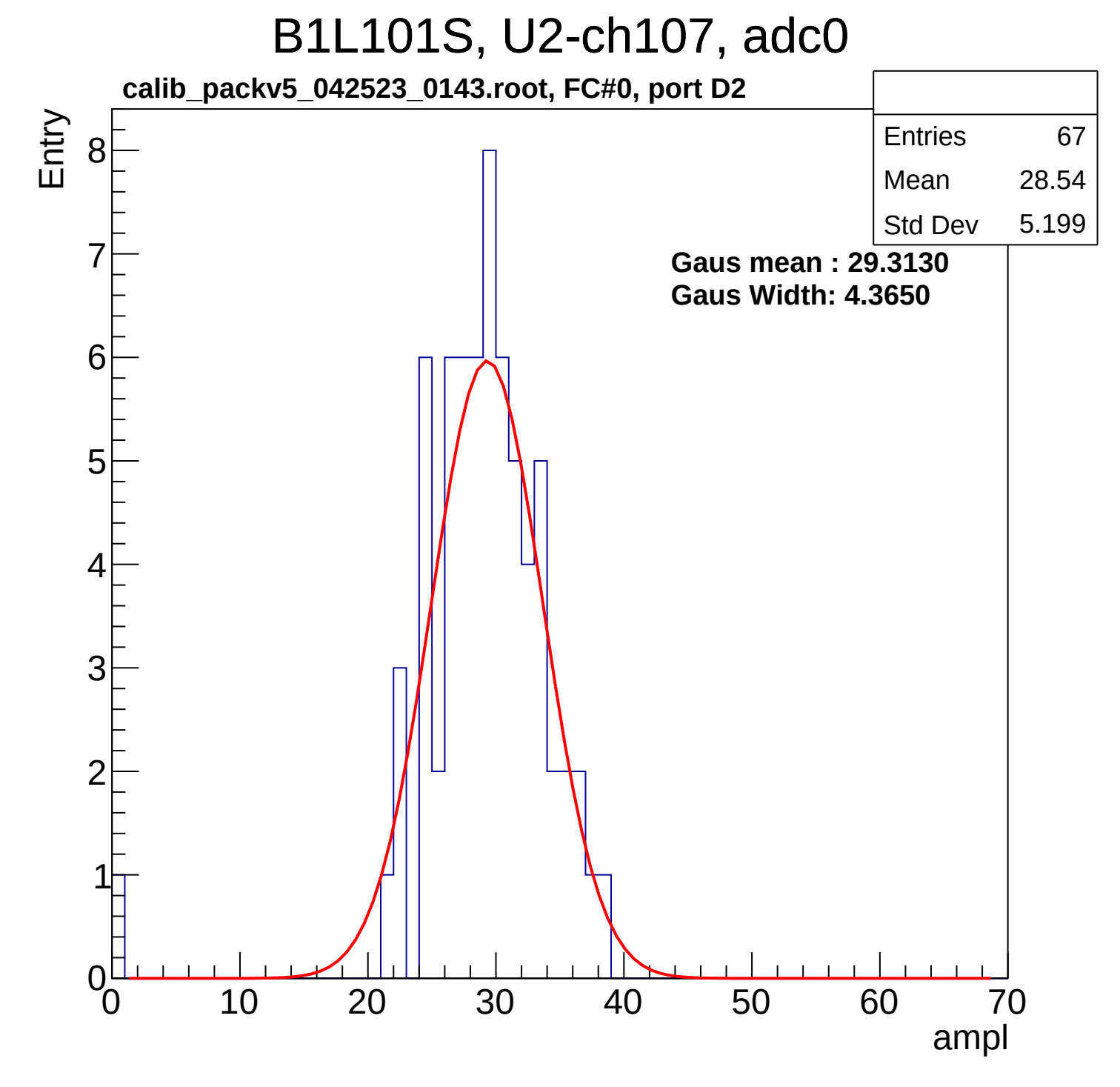

B1L101S, U2-ch106, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 65
Mean 47.86
Std Dev 3.91
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

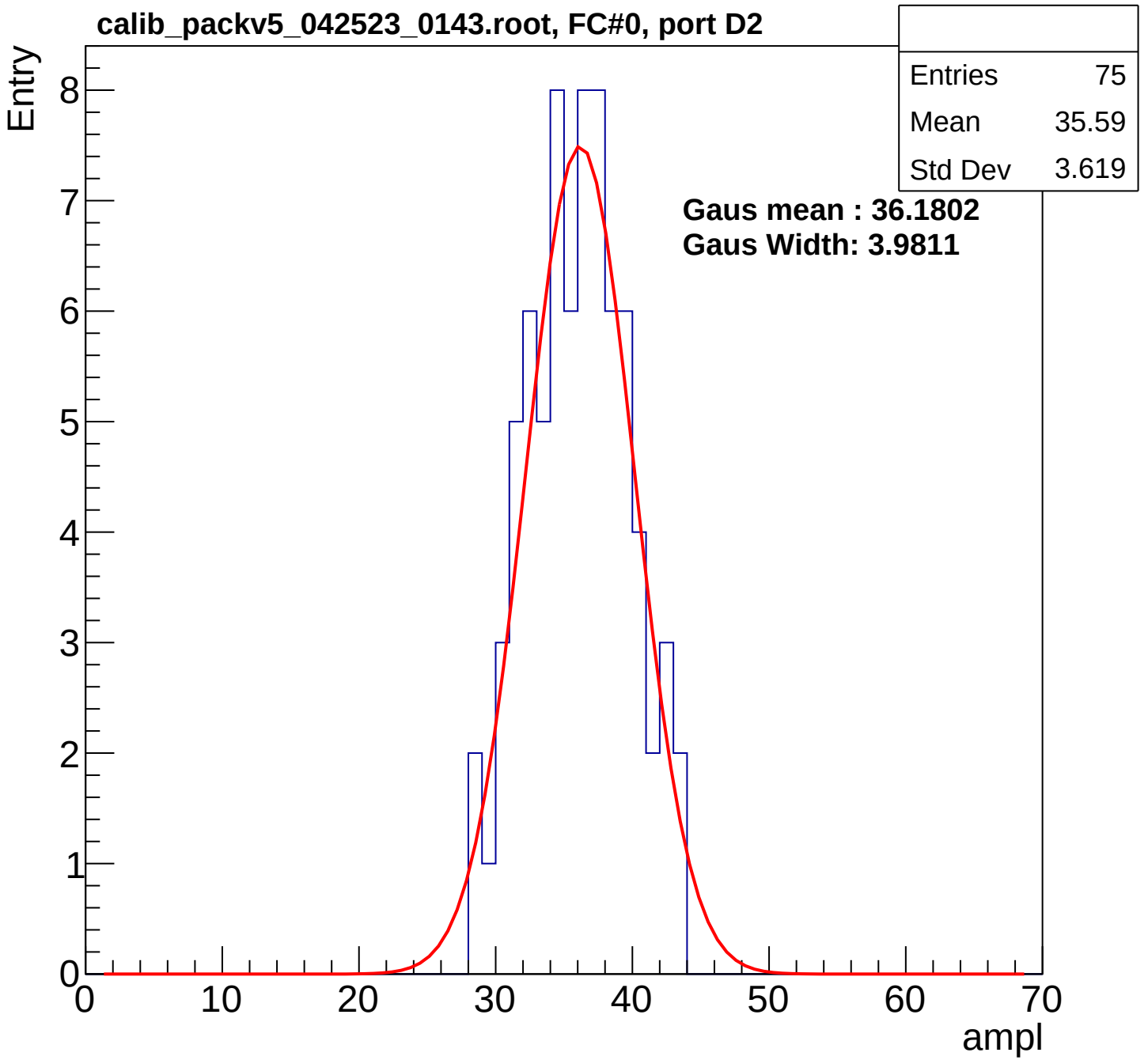

B1L101S, U2-ch106, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 42
Mean 53.45
Std Dev 3.267
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

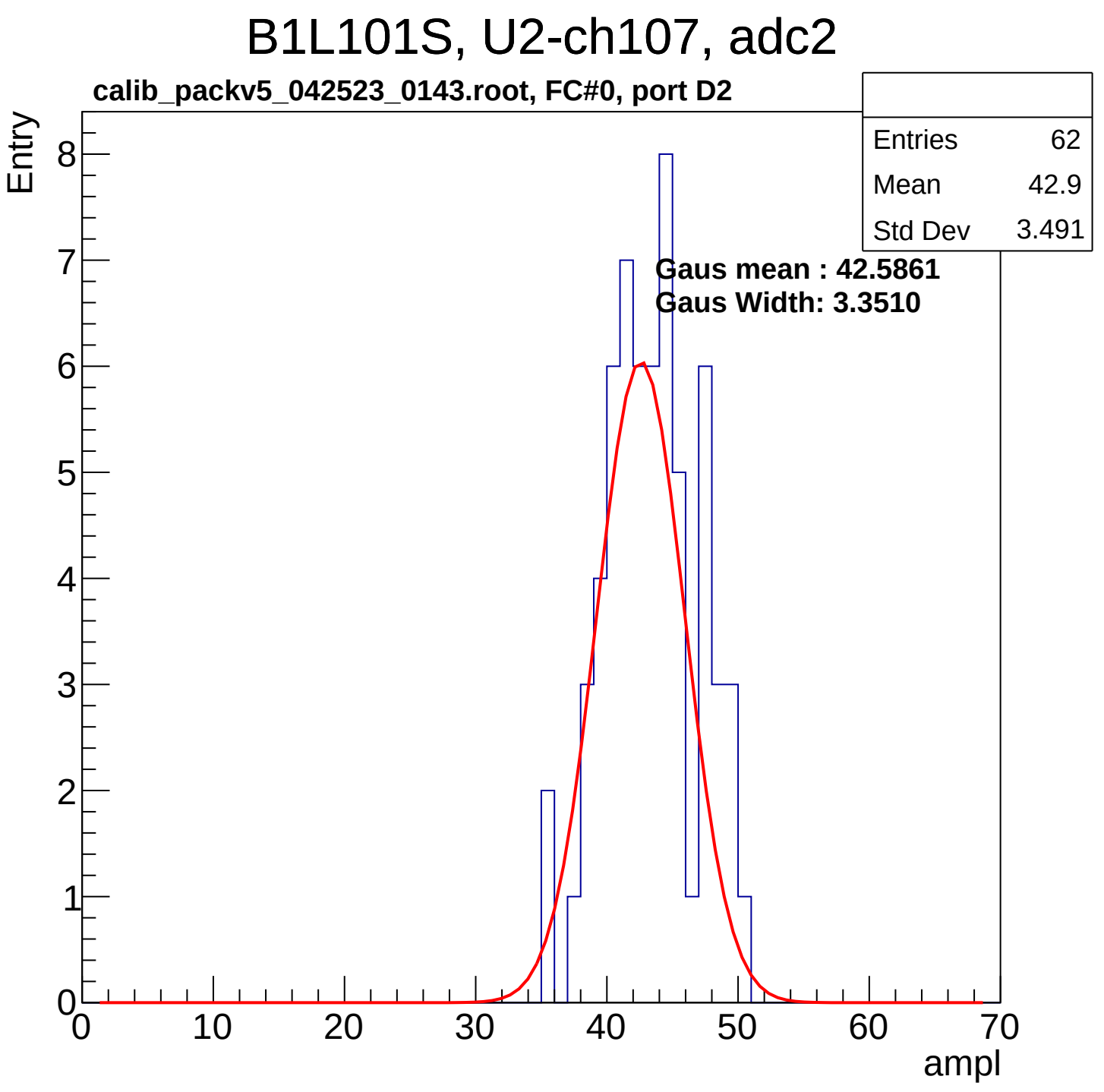

B1L101S, U2-ch106, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 57.39
Std Dev 3.549
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

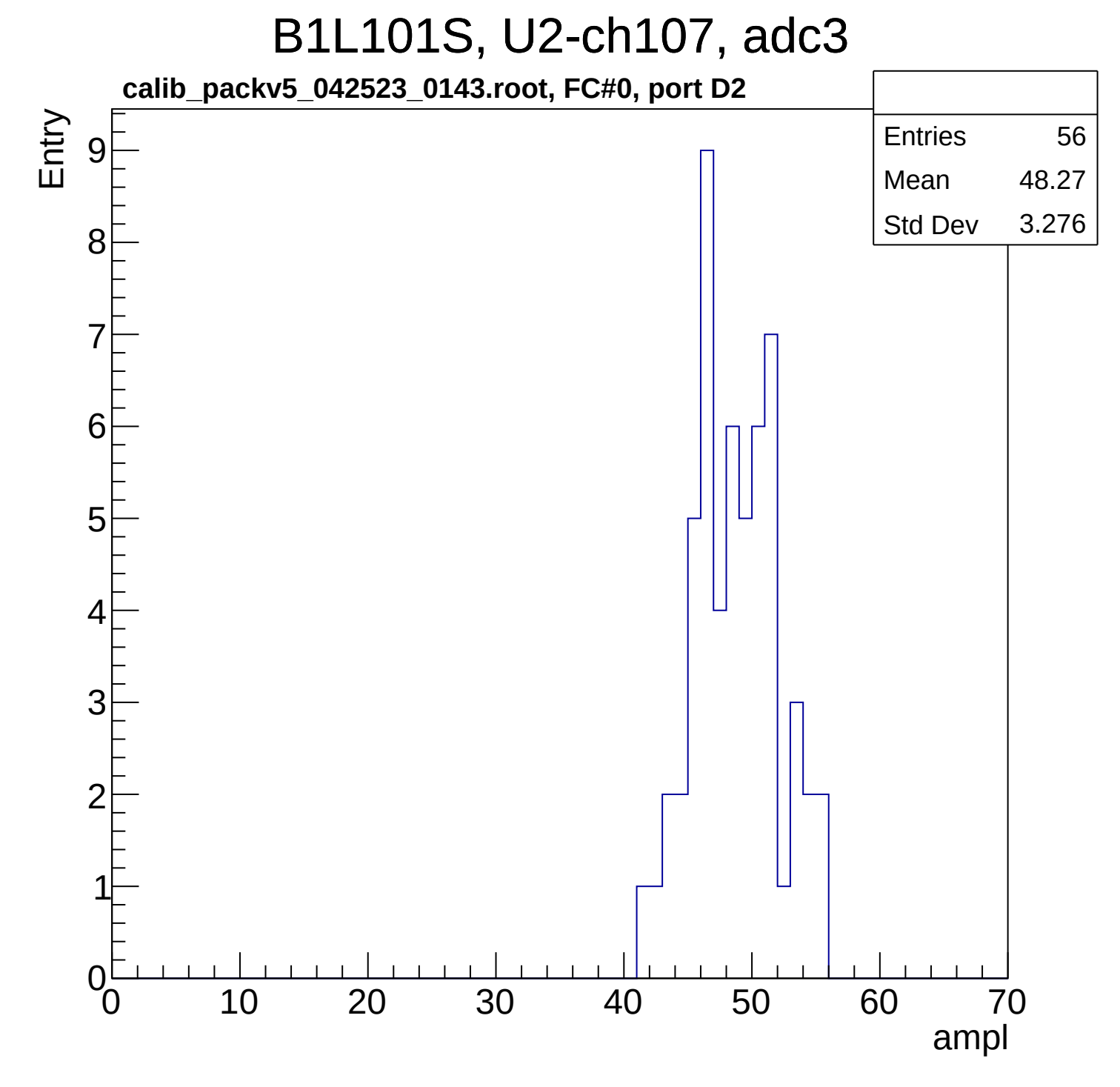

B1L101S, U2-ch106, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 26
Mean 58.46
Std Dev 11.87
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

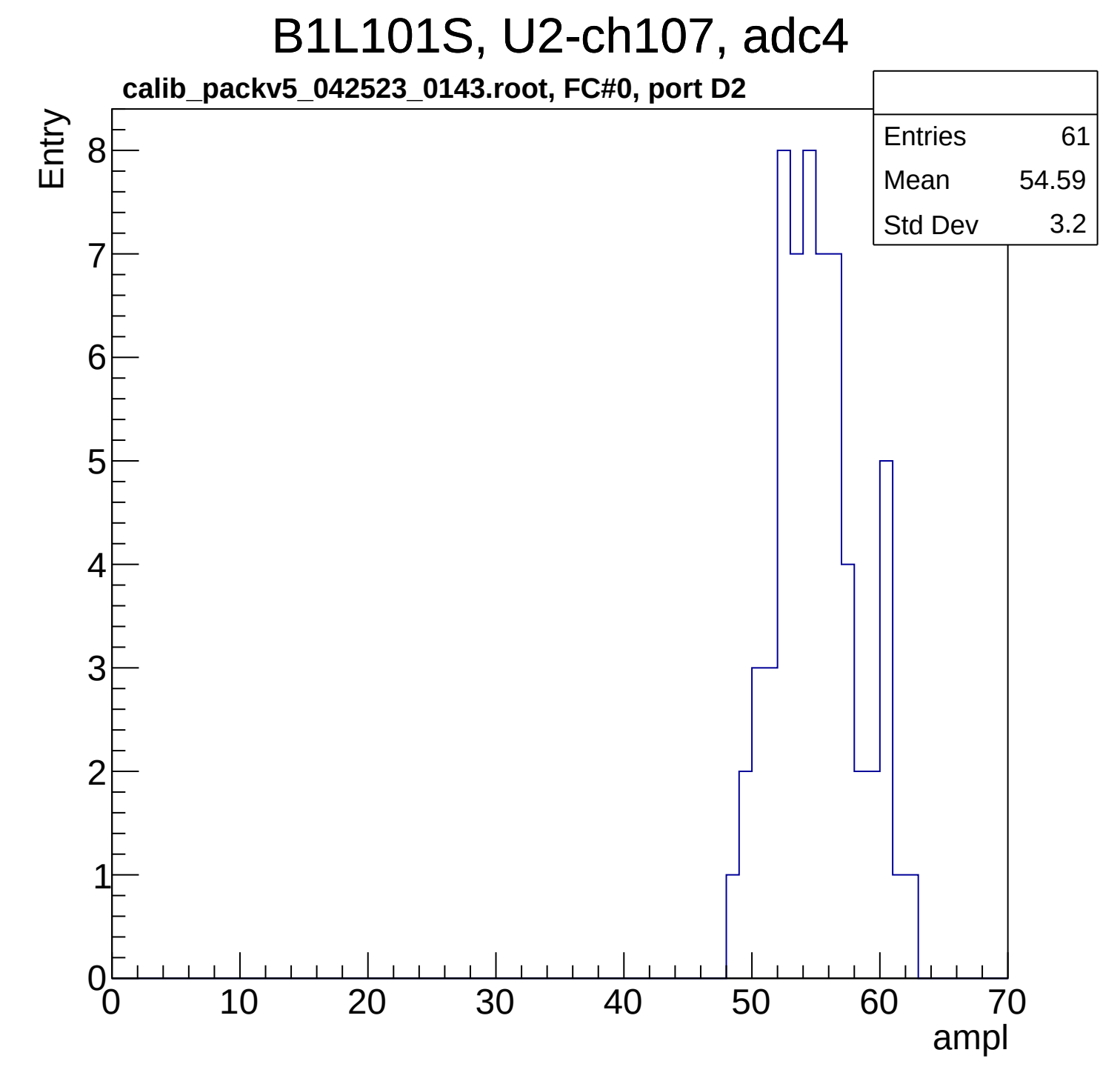

B1L101S, U2-ch106, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 41.67
Std Dev 29.47
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

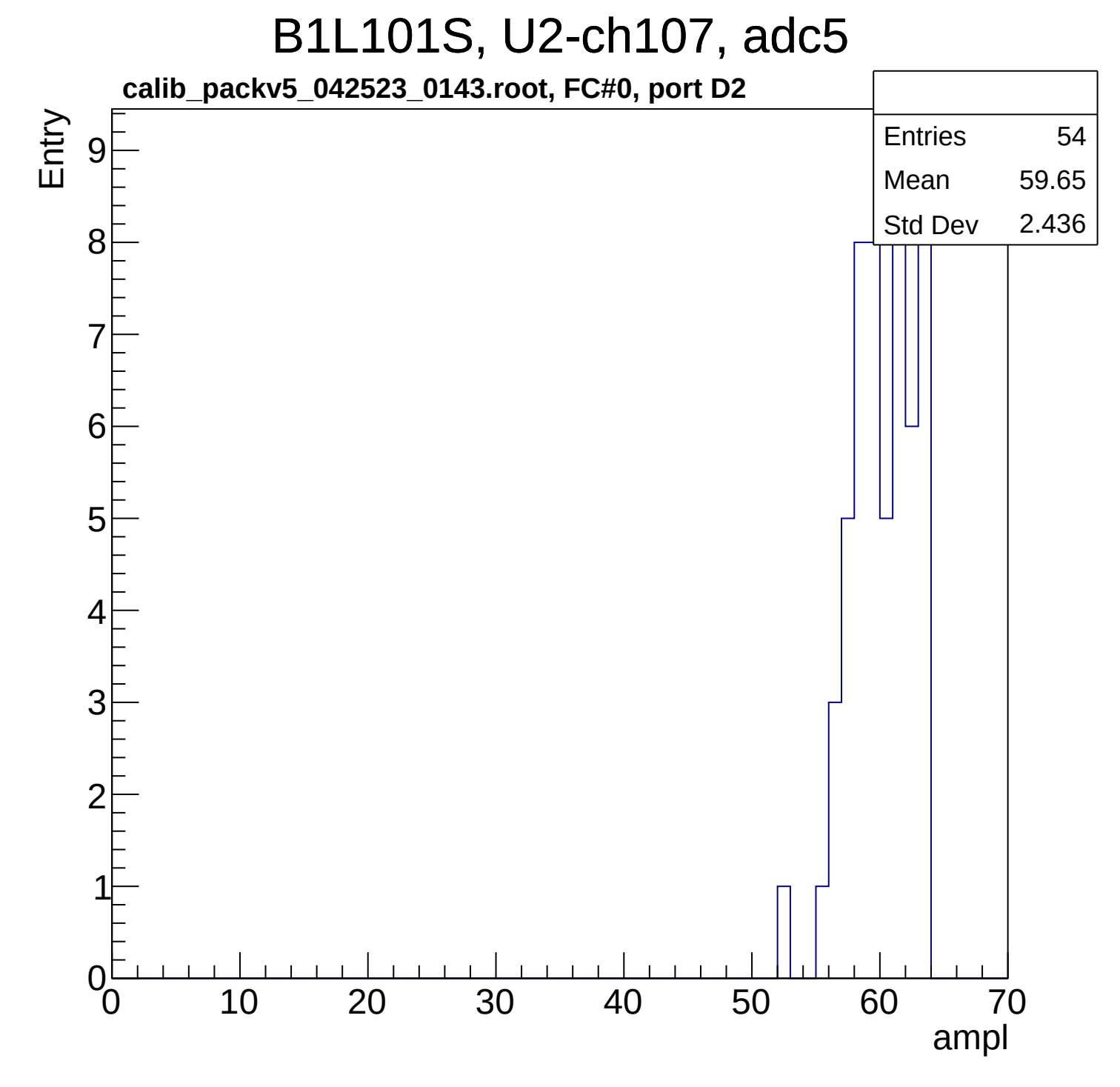

B1L101S, U2-ch107, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 28.54
Std Dev 5.199
Gaus mean : 29.3130
Gaus Width: 4.3650
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

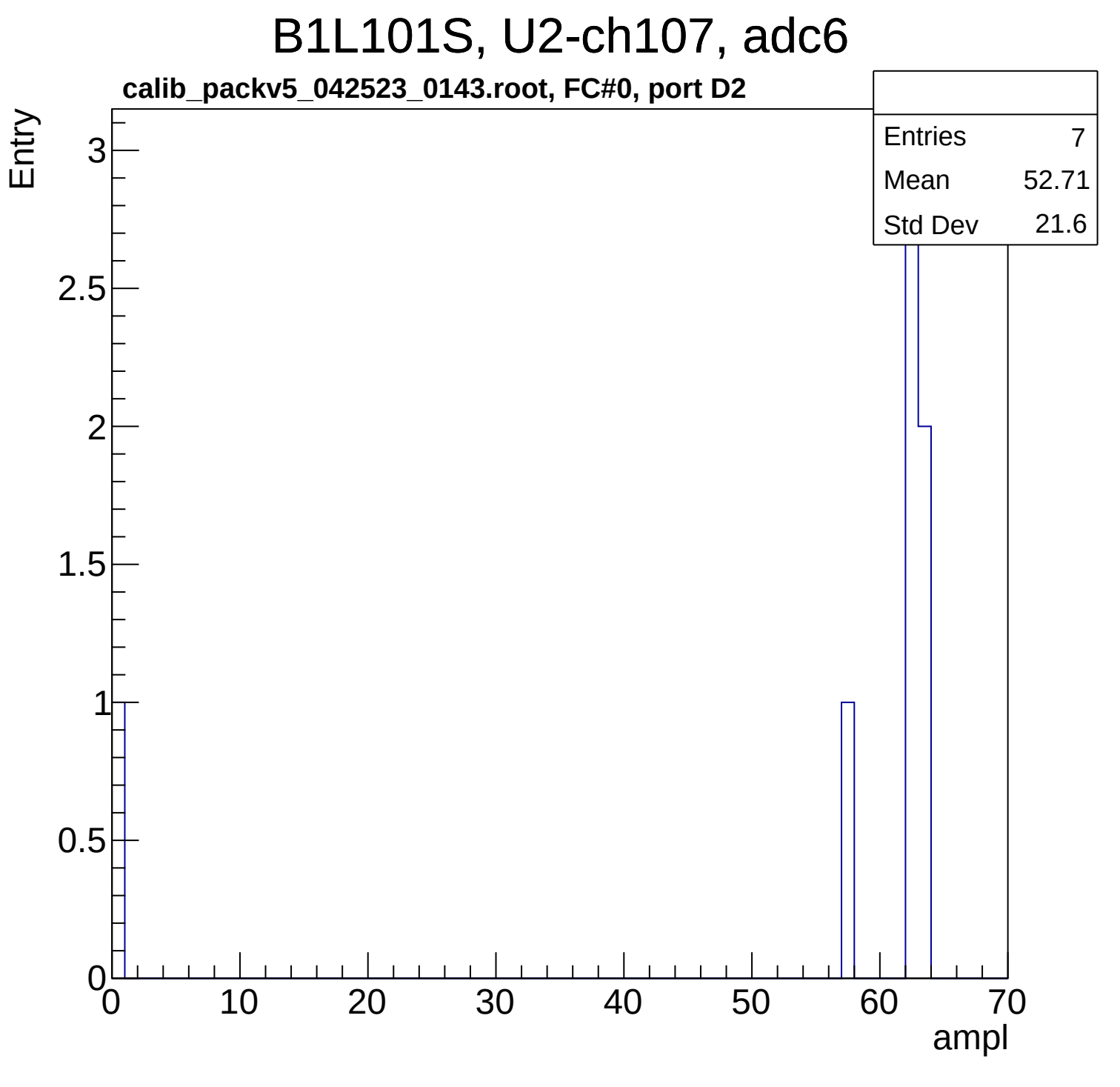

B1L101S, U2-ch107, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 35.59
Std Dev 3.619
Gaus mean : 36.1802
Gaus Width: 3.9811
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

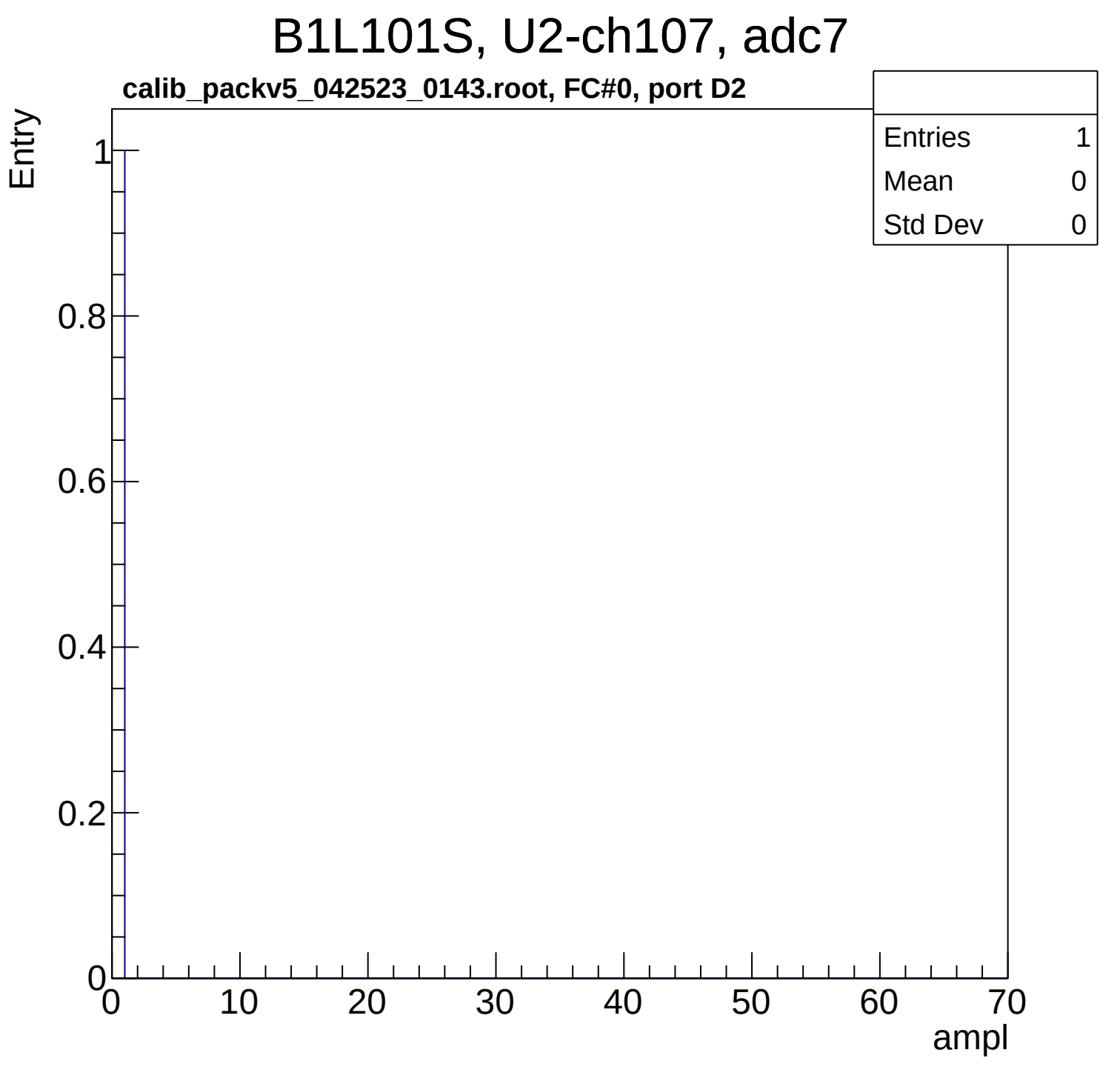

B1L101S, U2-ch107, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 42.9
Std Dev 3.491
Gaus mean : 42.5861
Gaus Width: 3.3510
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

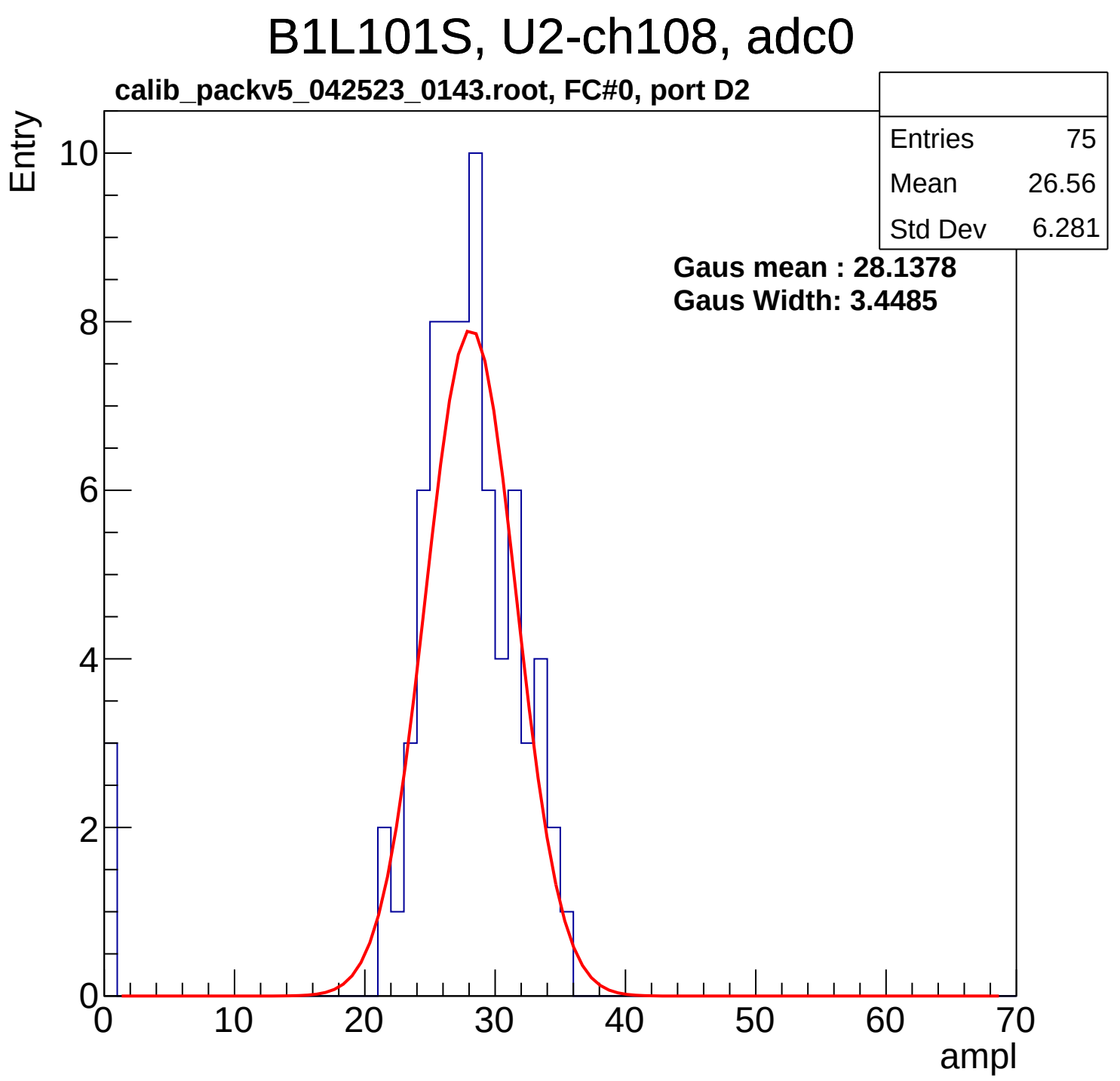

B1L101S, U2-ch107, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 48.27
Std Dev 3.276
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

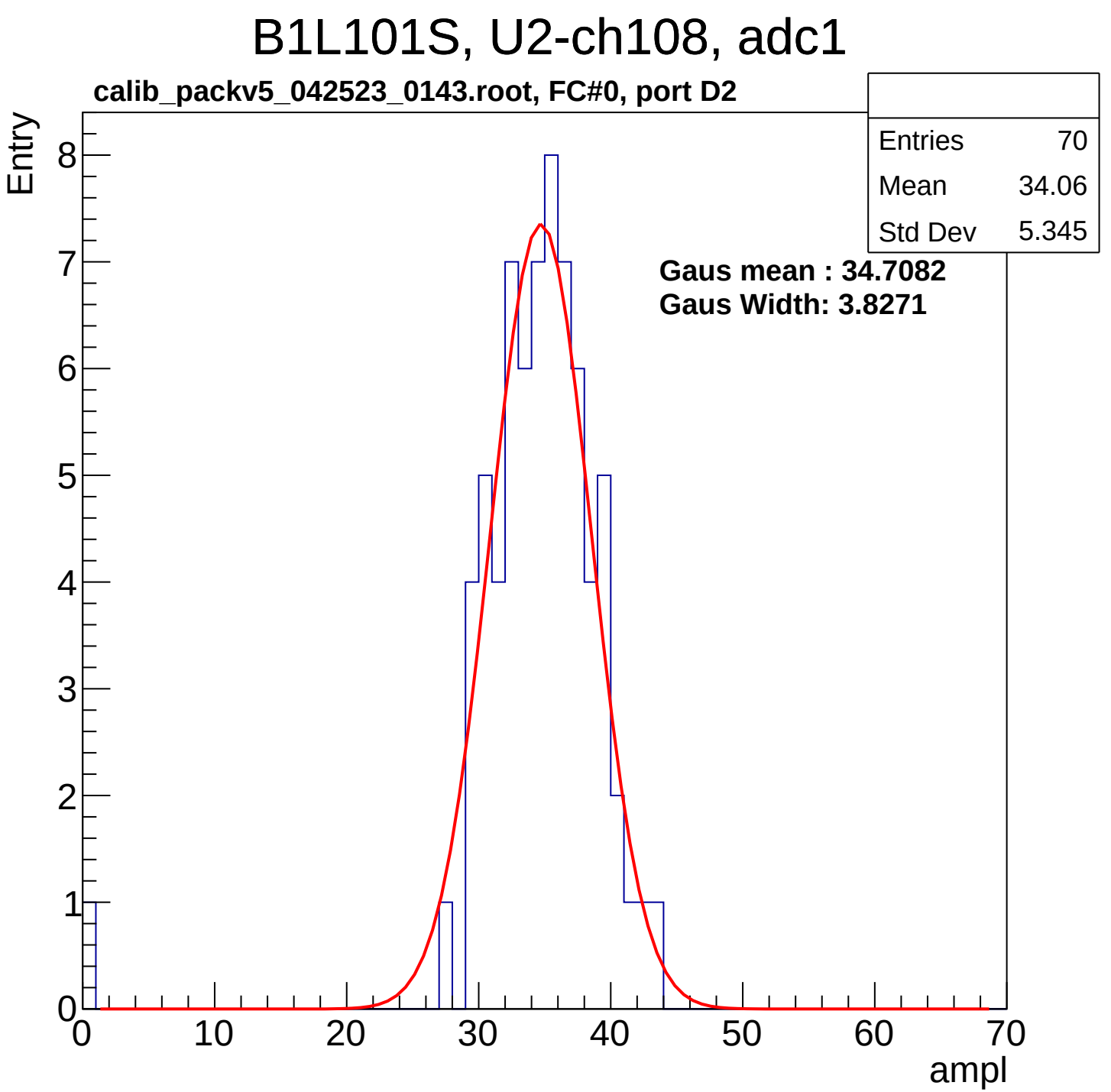

B1L101S, U2-ch107, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 54.59
Std Dev 3.2
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

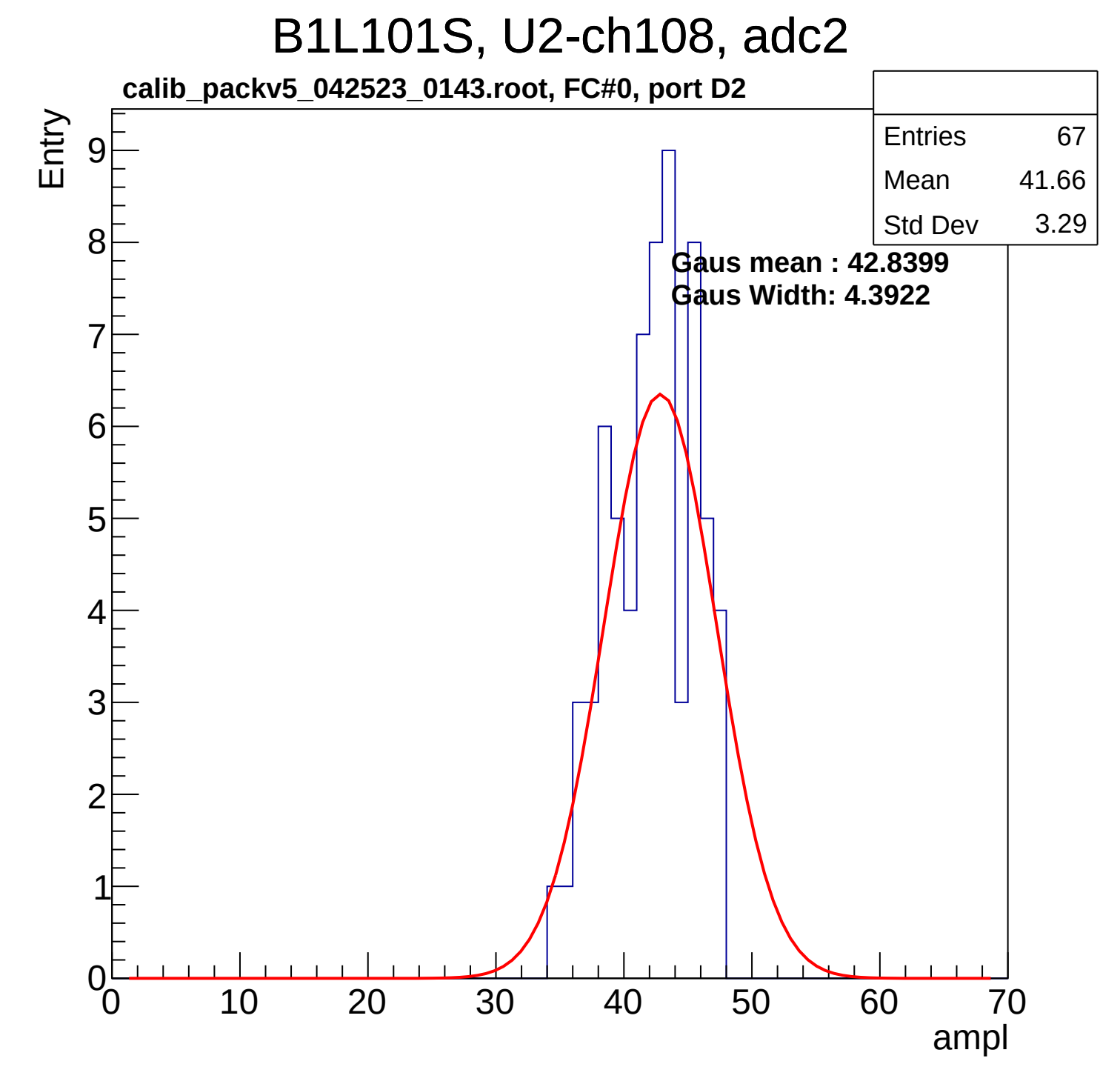

B1L101S, U2-ch107, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 59.65
Std Dev 2.436
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

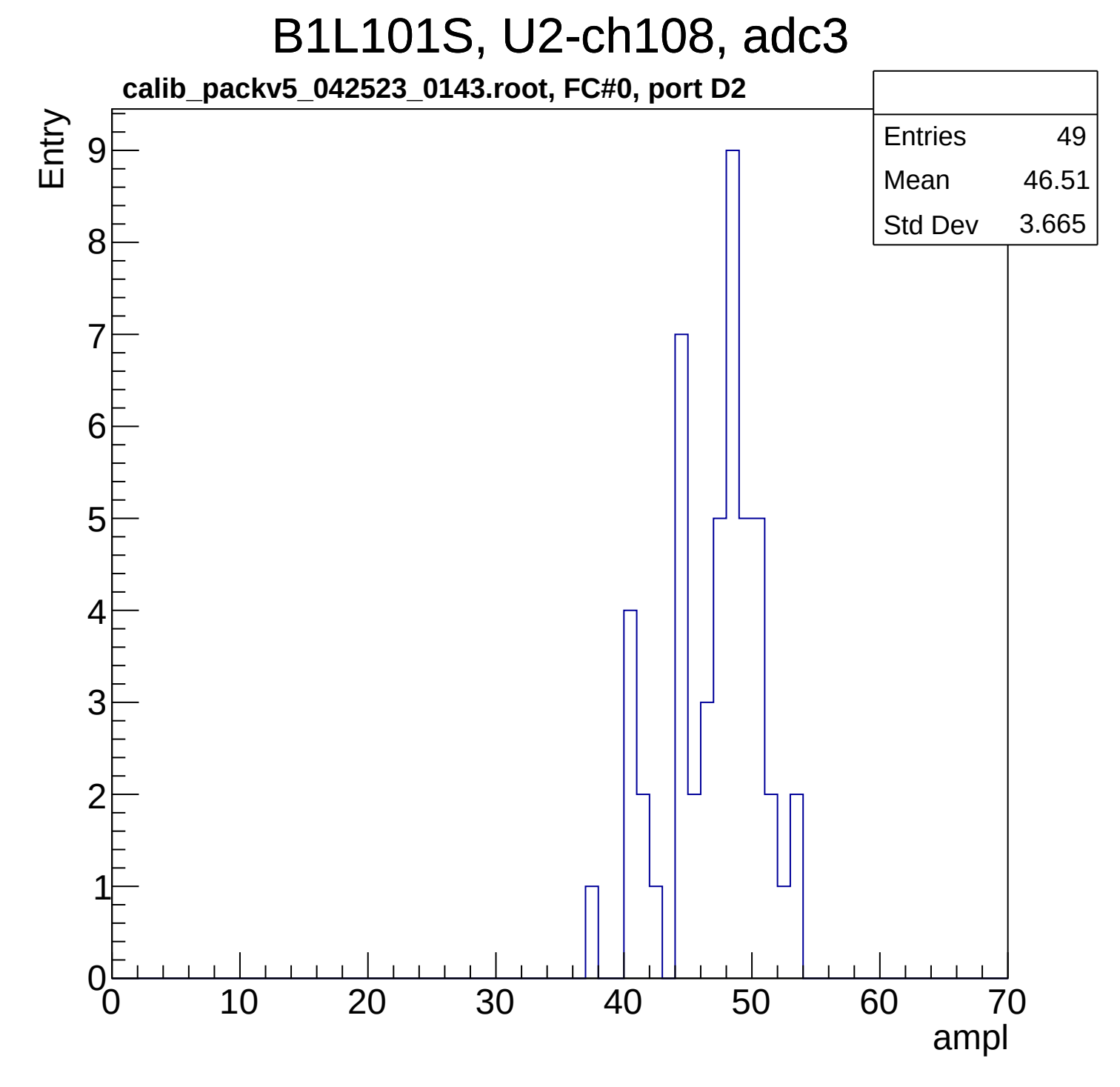

B1L101S, U2-ch107, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 52.71
Std Dev 21.6
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

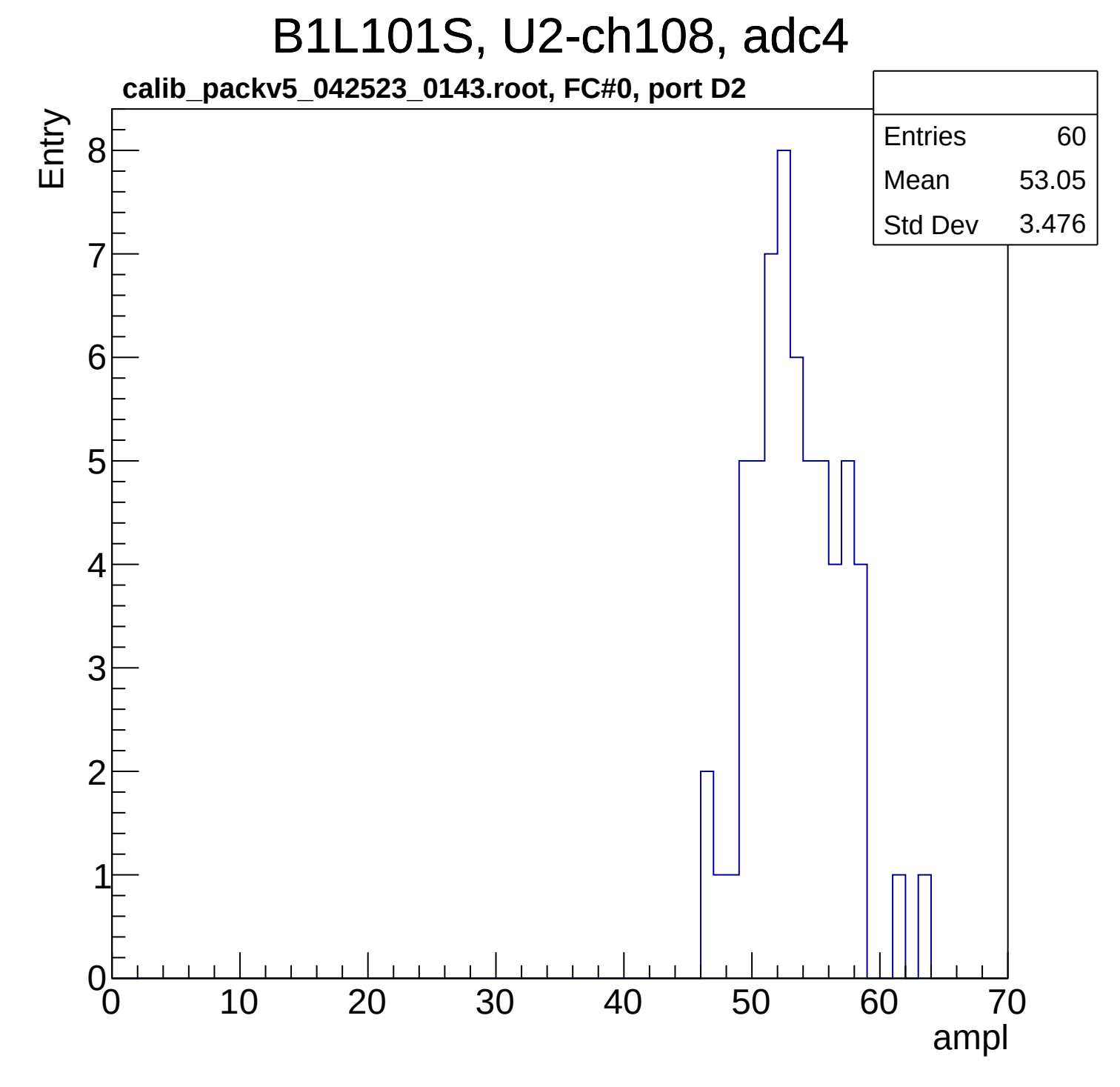

B1L101S, U2-ch107, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

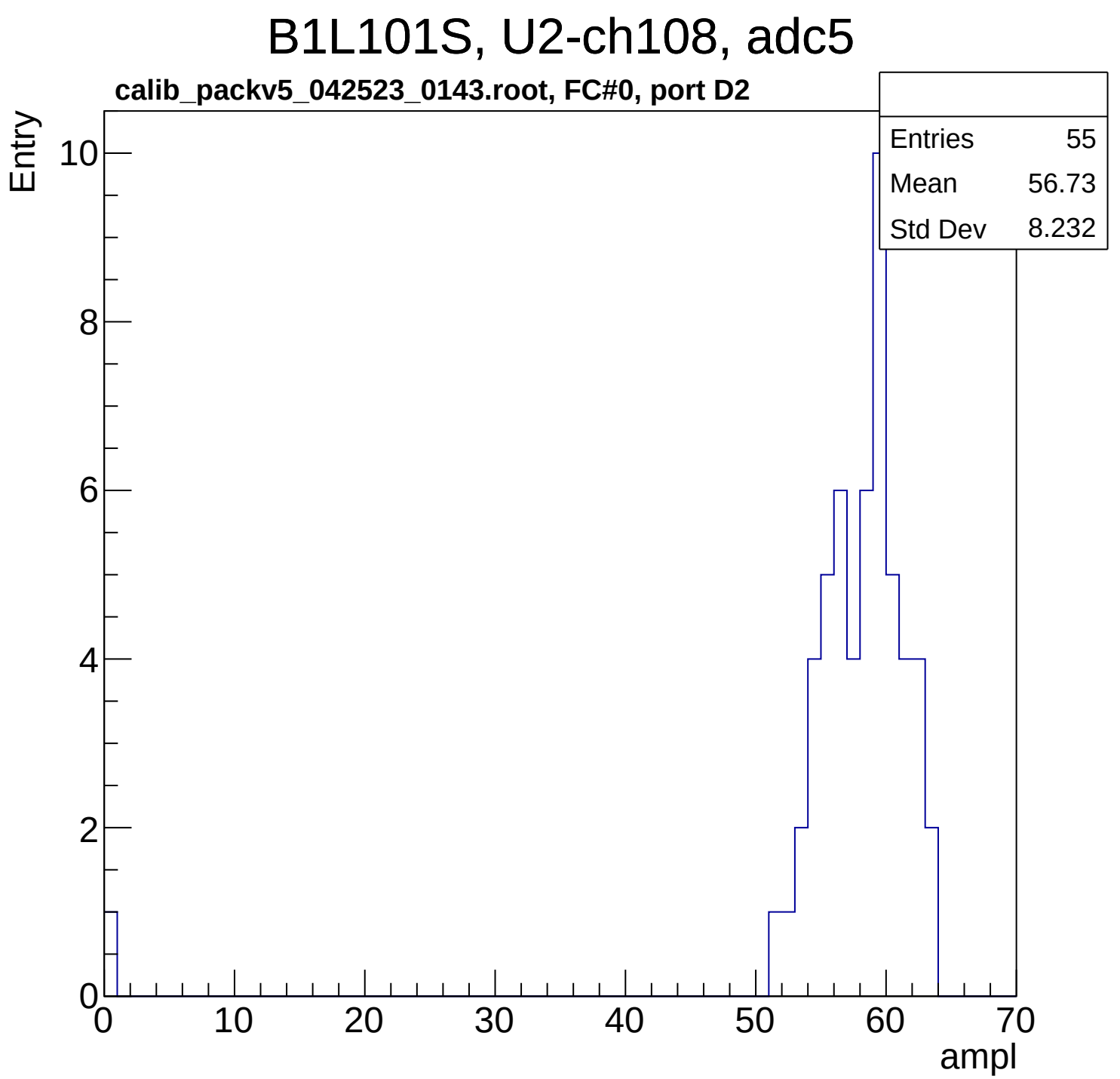

B1L101S, U2-ch108, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 26.56
Std Dev 6.281
Gaus mean : 28.1378
Gaus Width: 3.4485
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

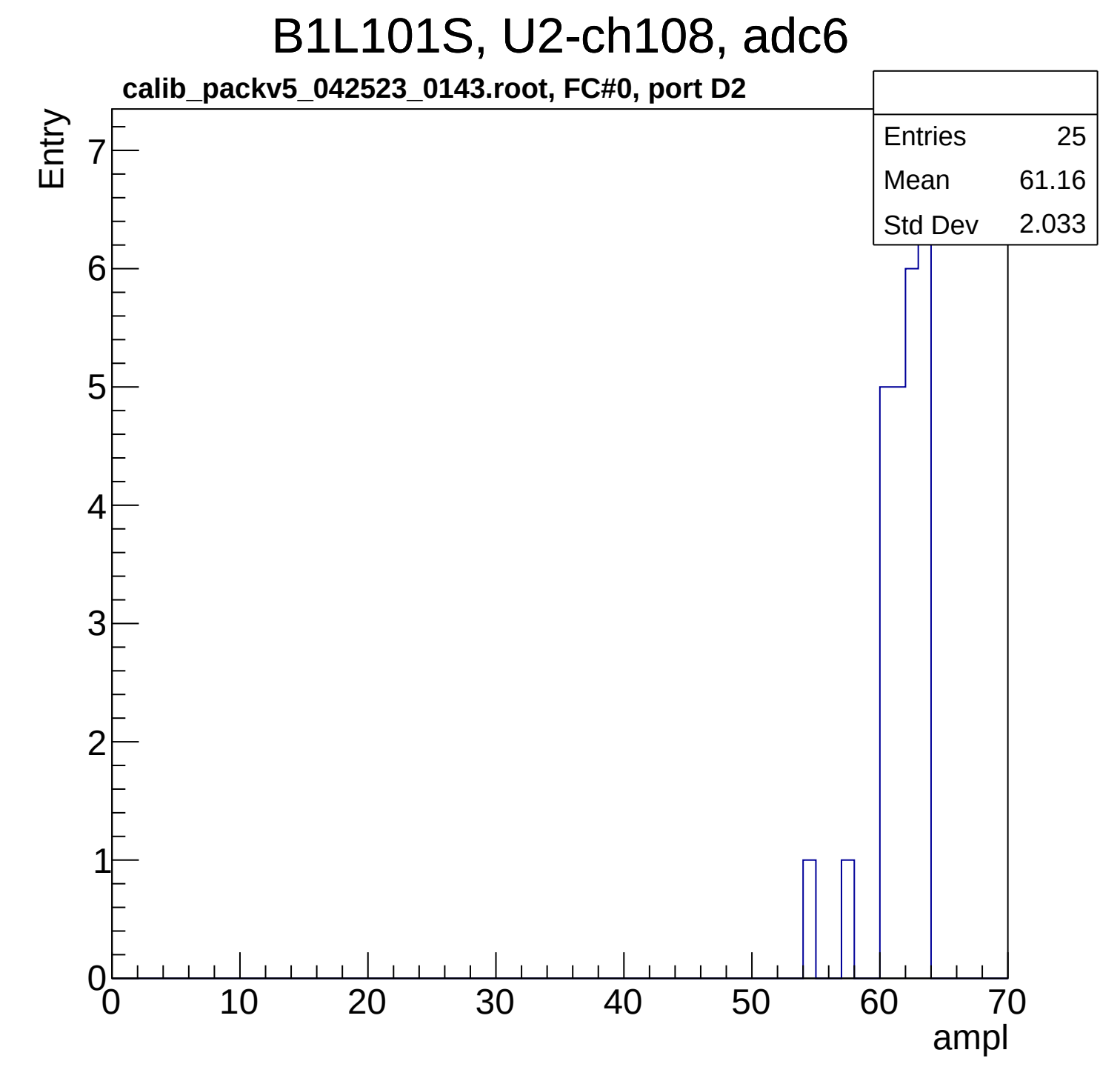

B1L101S, U2-ch108, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 34.06
Std Dev 5.345
Gaus mean : 34.7082
Gaus Width: 3.8271
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

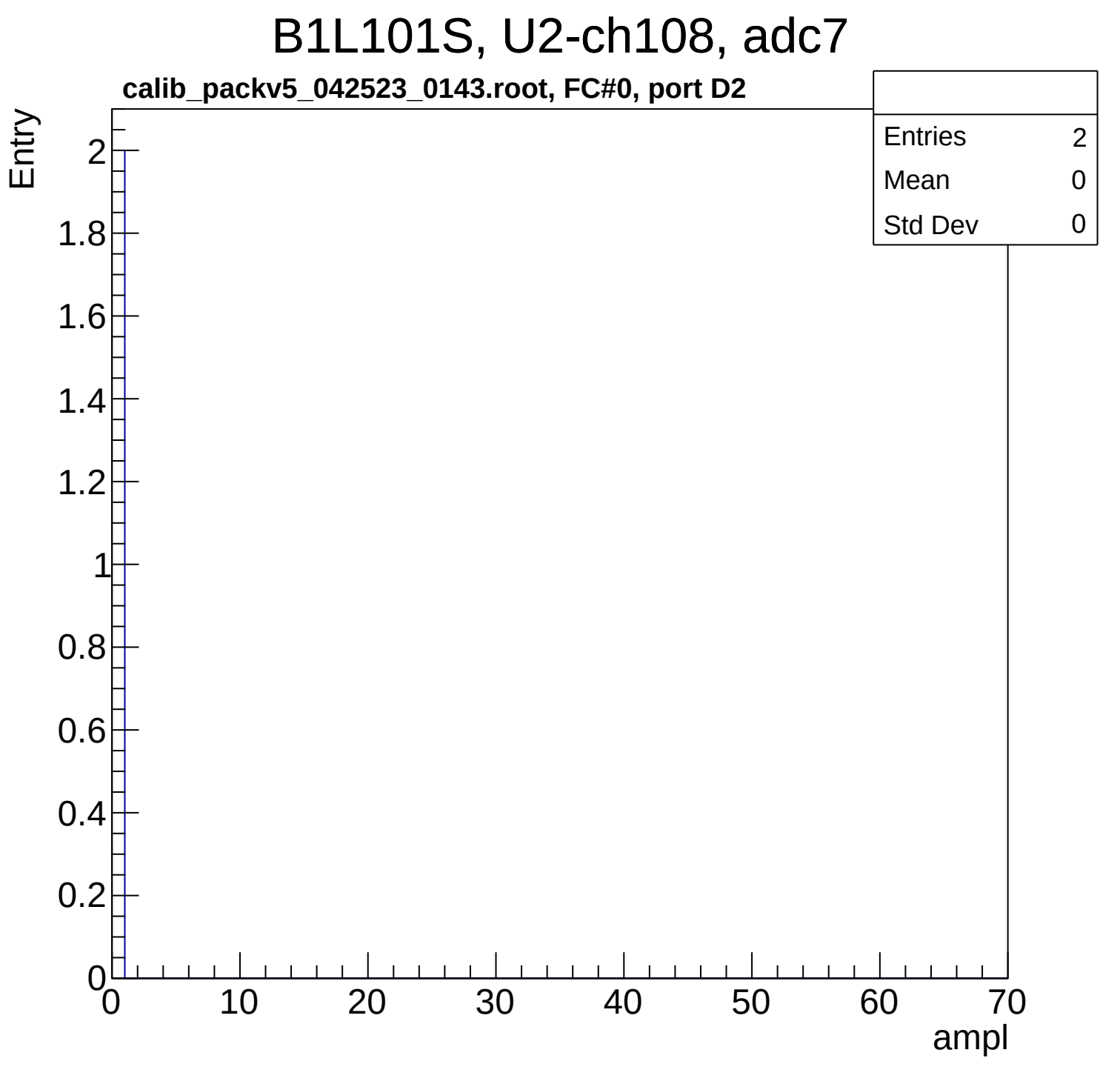

B1L101S, U2-ch108, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 41.66
Std Dev 3.29
Gaus mean : 42.8399
Gaus Width: 4.3922
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

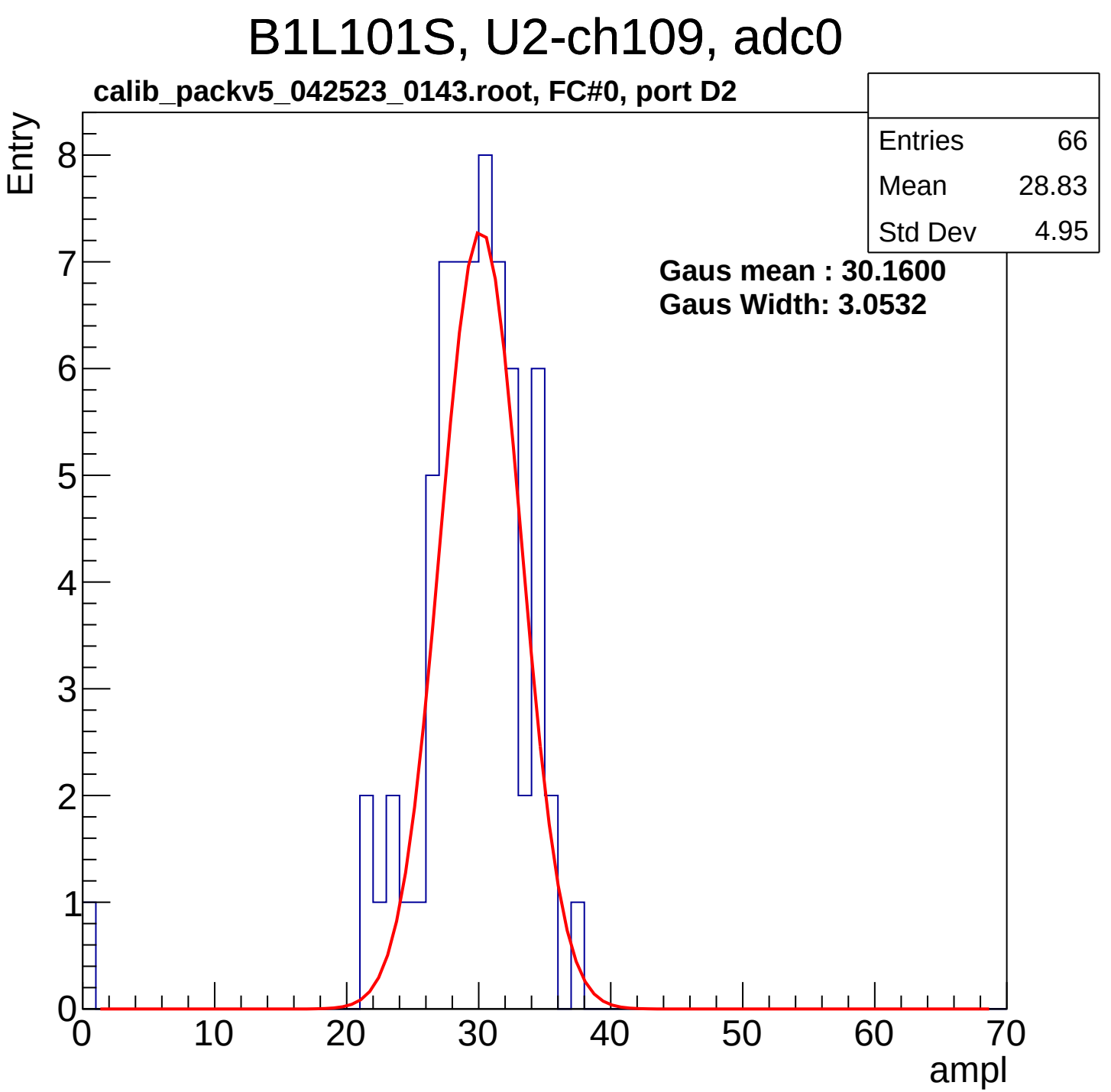

B1L101S, U2-ch108, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 46.51
Std Dev 3.665
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

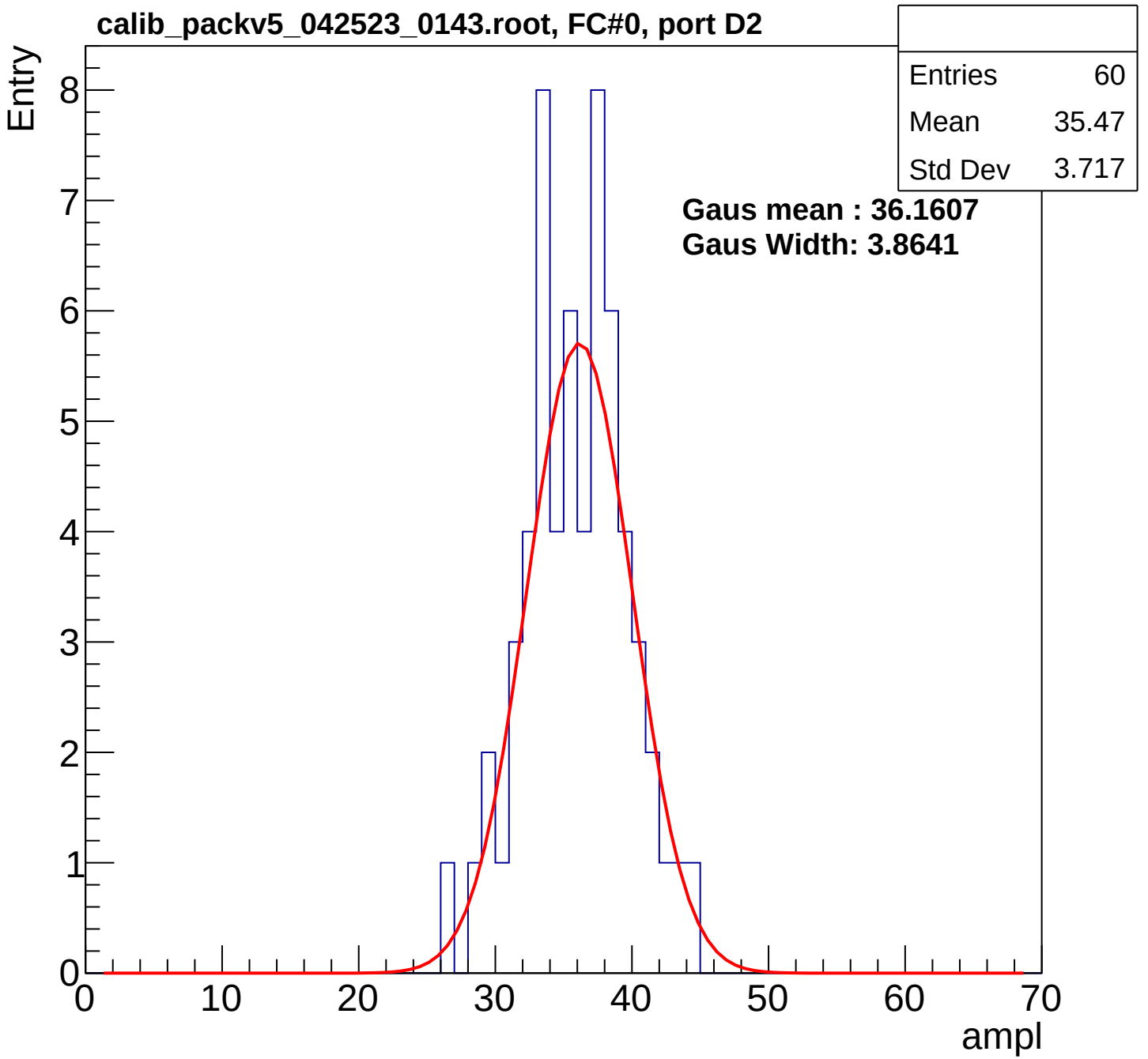

B1L101S, U2-ch108, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 53.05
Std Dev 3.476
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

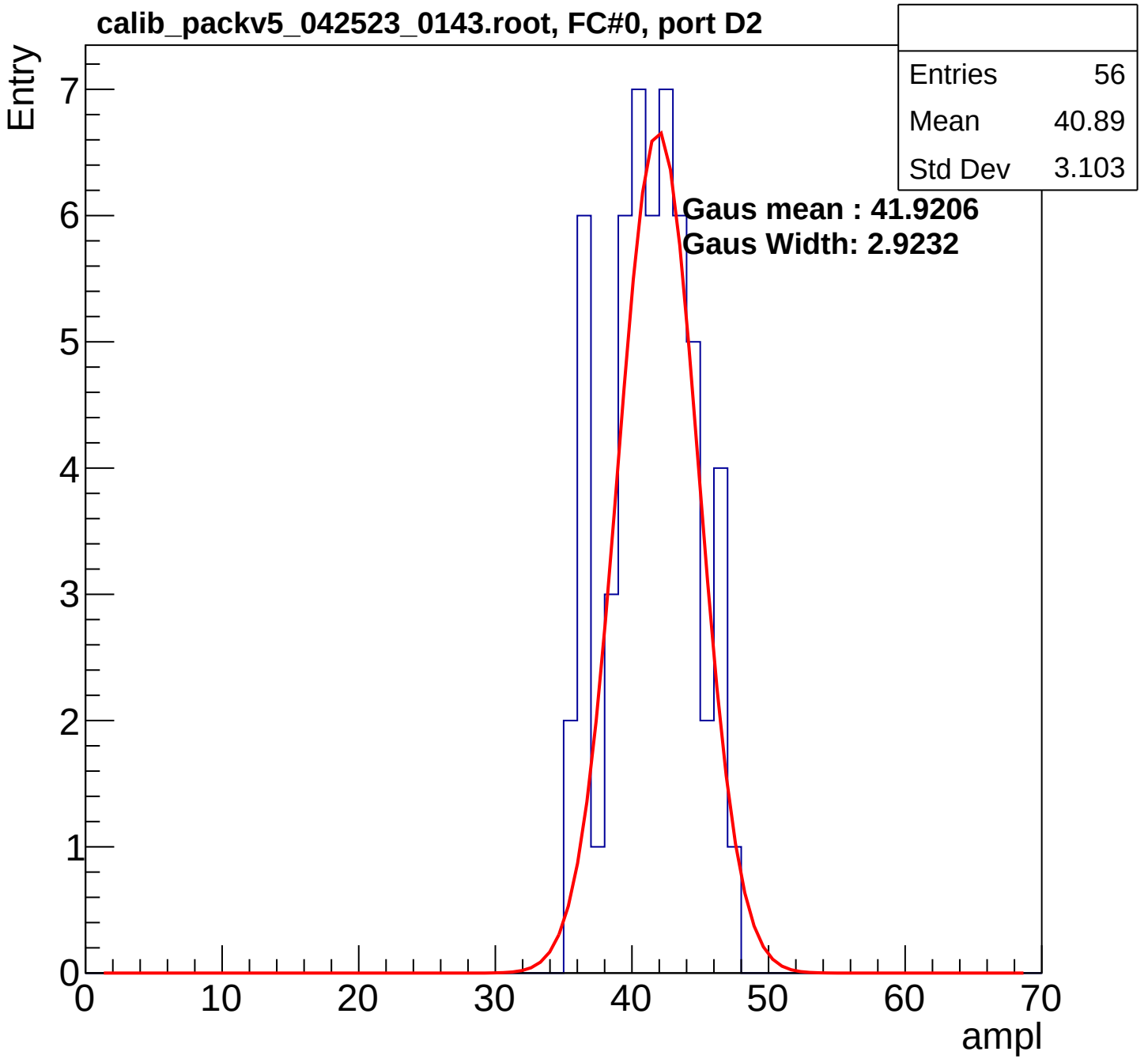

B1L101S, U2-ch108, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 56.73
Std Dev 8.232
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

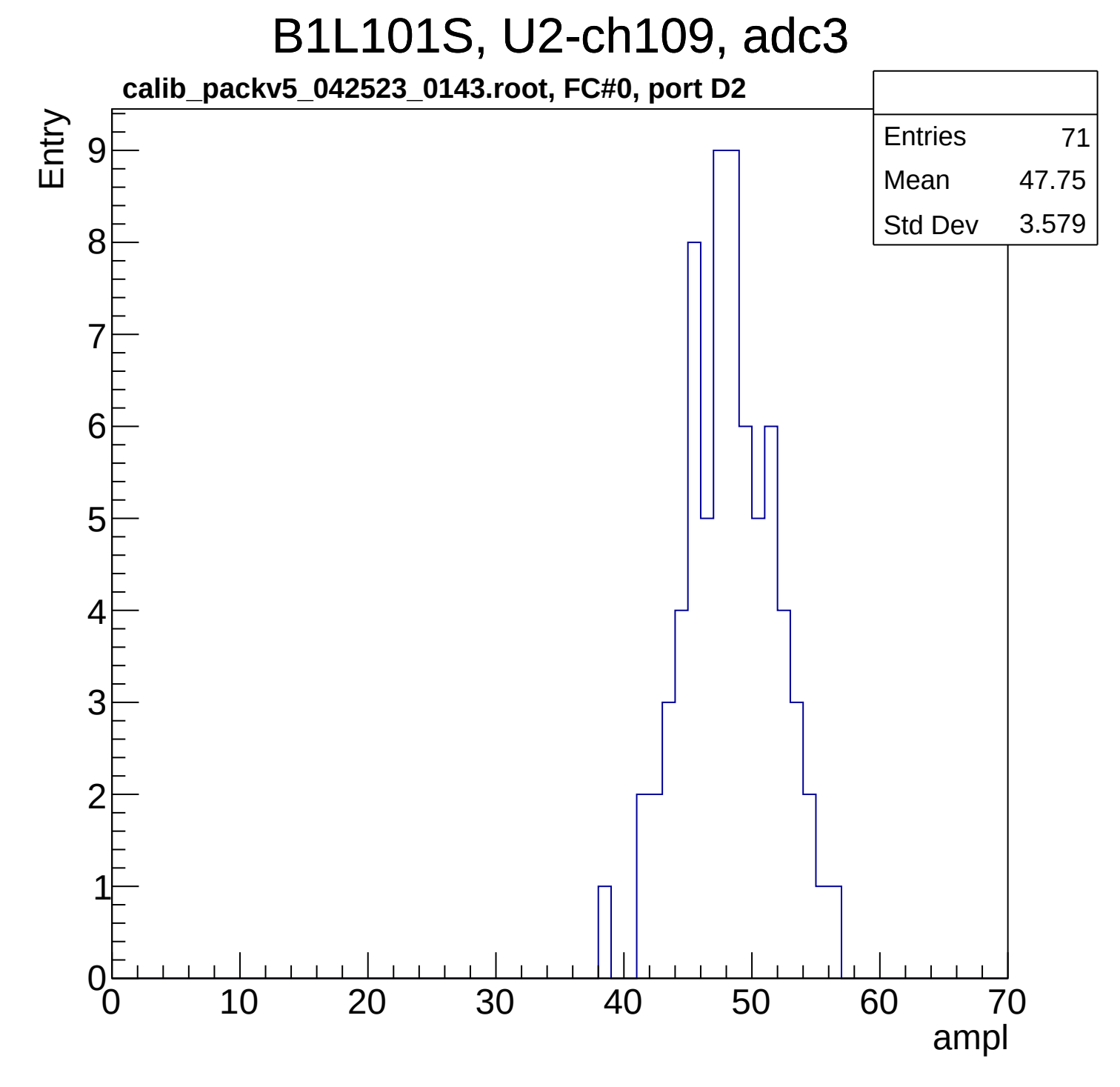

B1L101S, U2-ch108, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 25
Mean 61.16
Std Dev 2.033
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

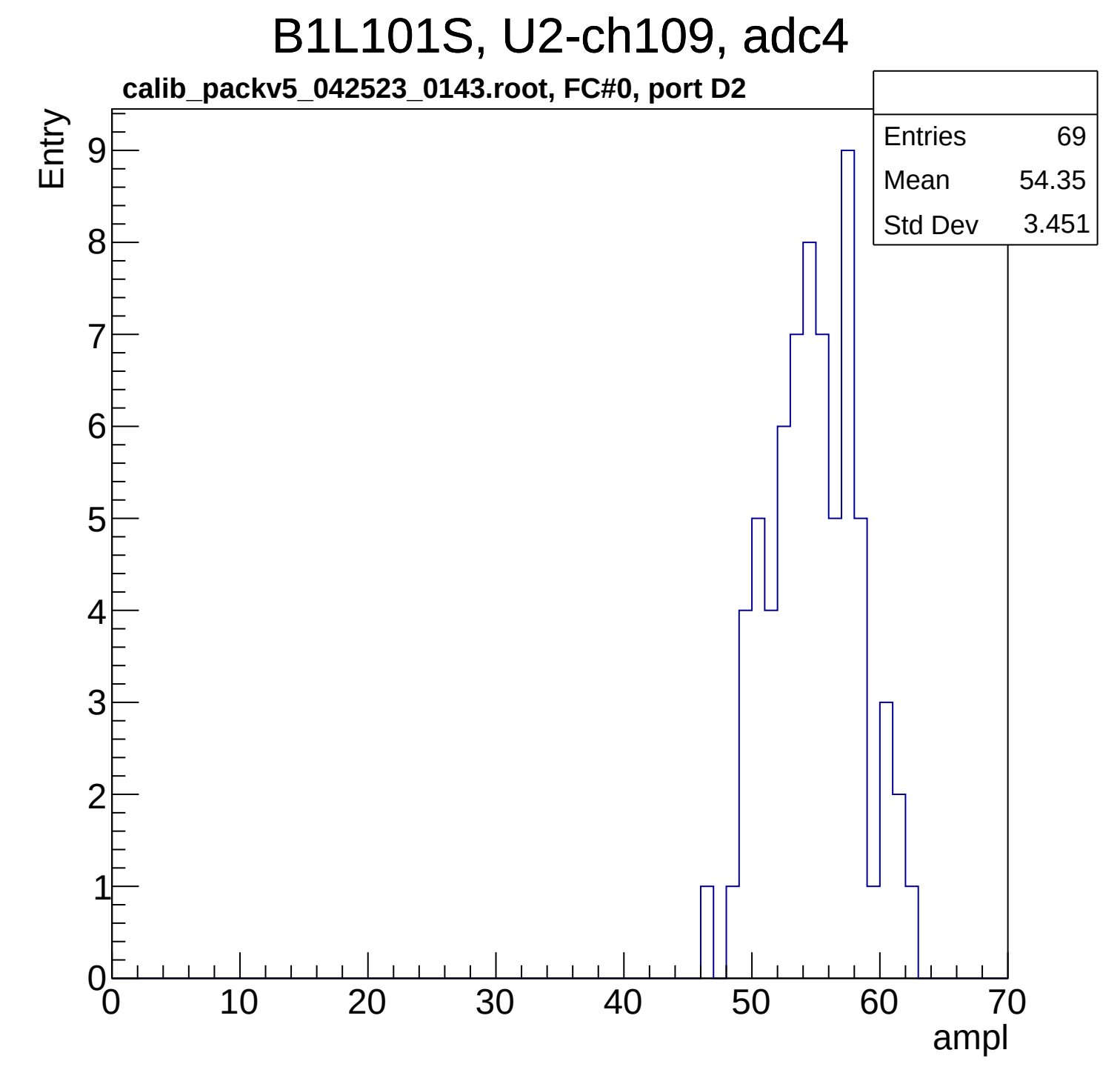

B1L101S, U2-ch108, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

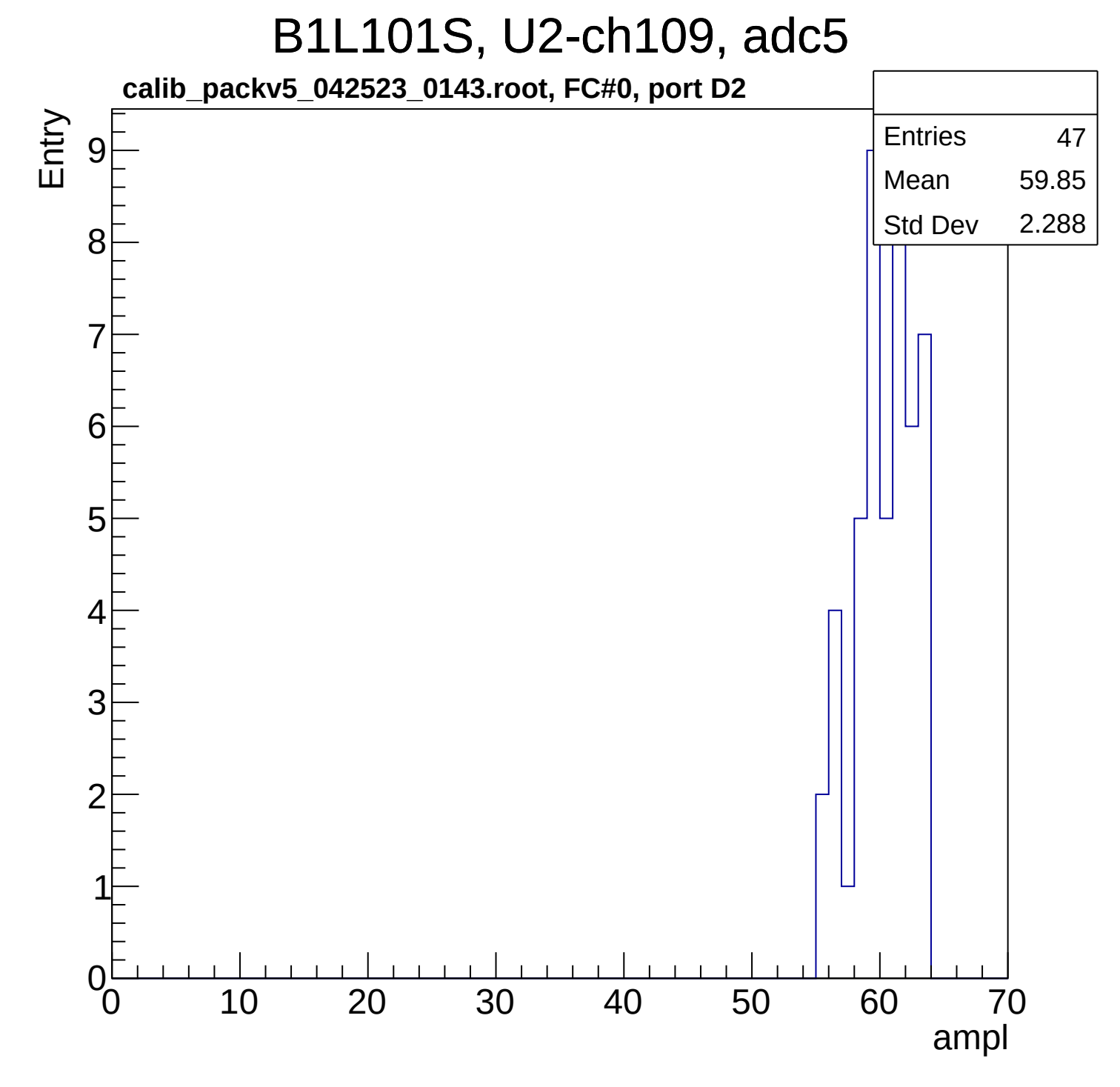

B1L101S, U2-ch109, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 28.83
Std Dev 4.95
Gaus mean : 30.1600
Gaus Width: 3.0532
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

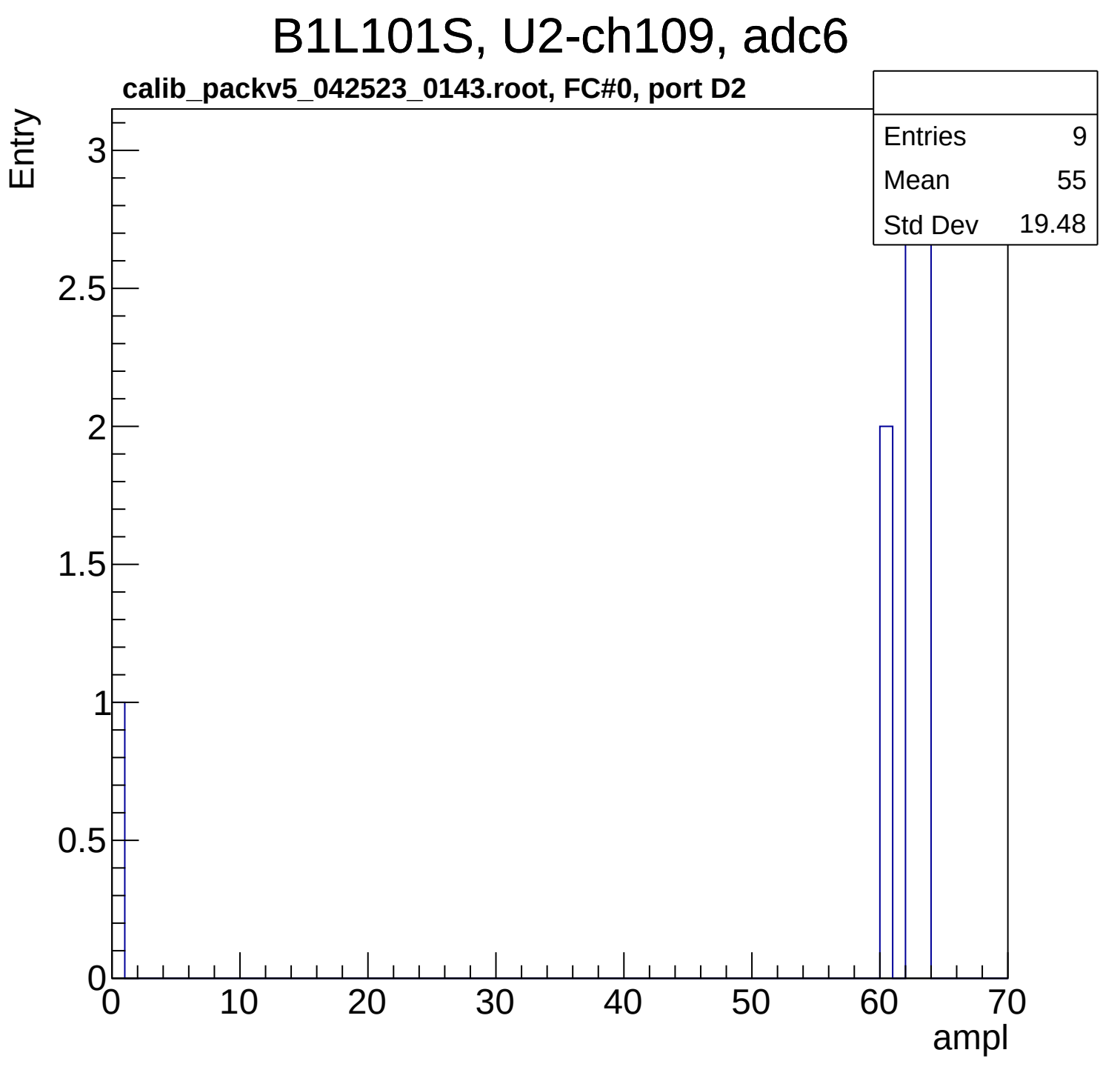

B1L101S, U2-ch109, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 35.47
Std Dev 3.717
Gaus mean : 36.1607
Gaus Width: 3.8641
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

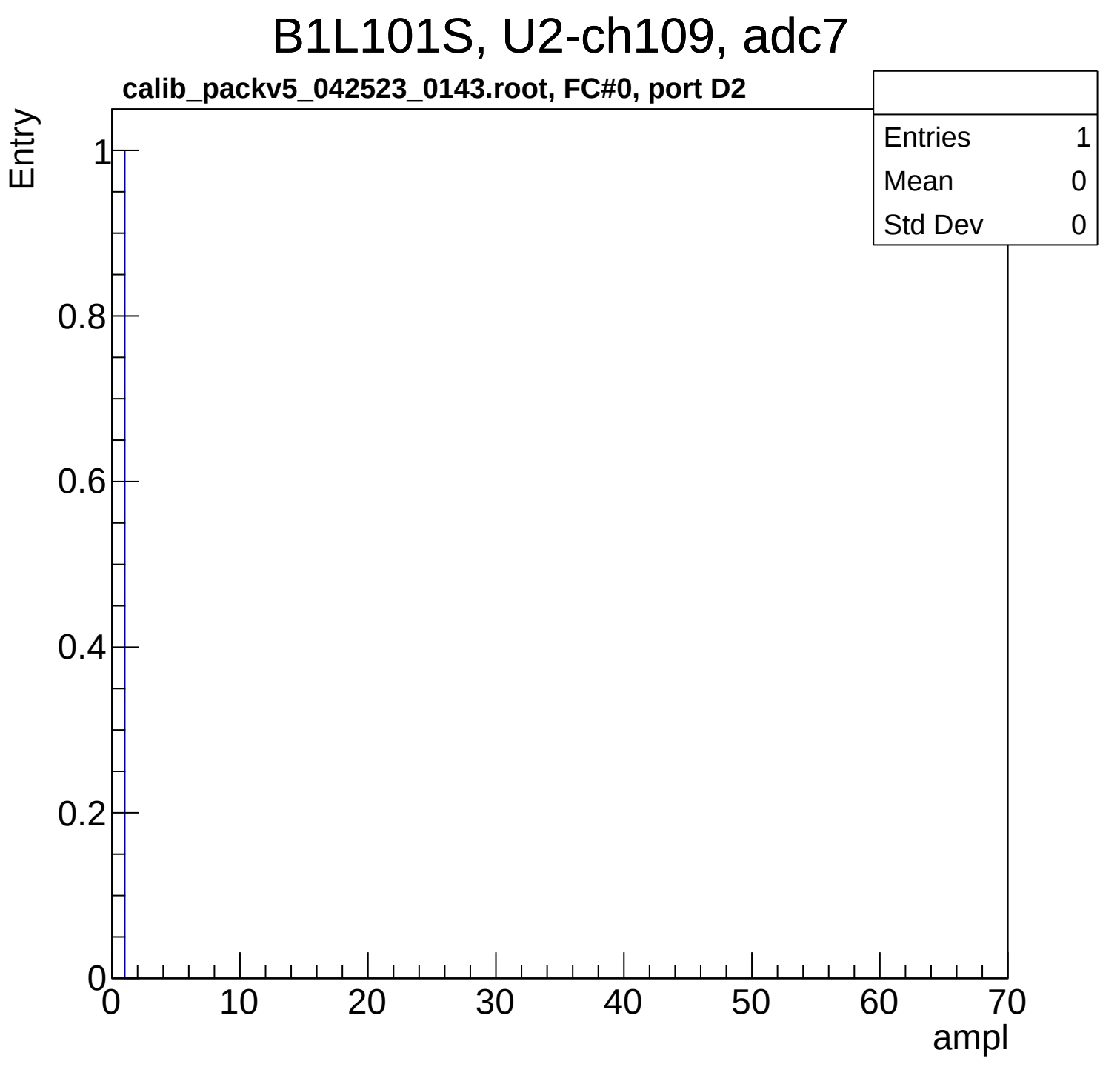

B1L101S, U2-ch109, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 40.89
Std Dev 3.103
Gaus mean : 41.9206
Gaus Width: 2.9232
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

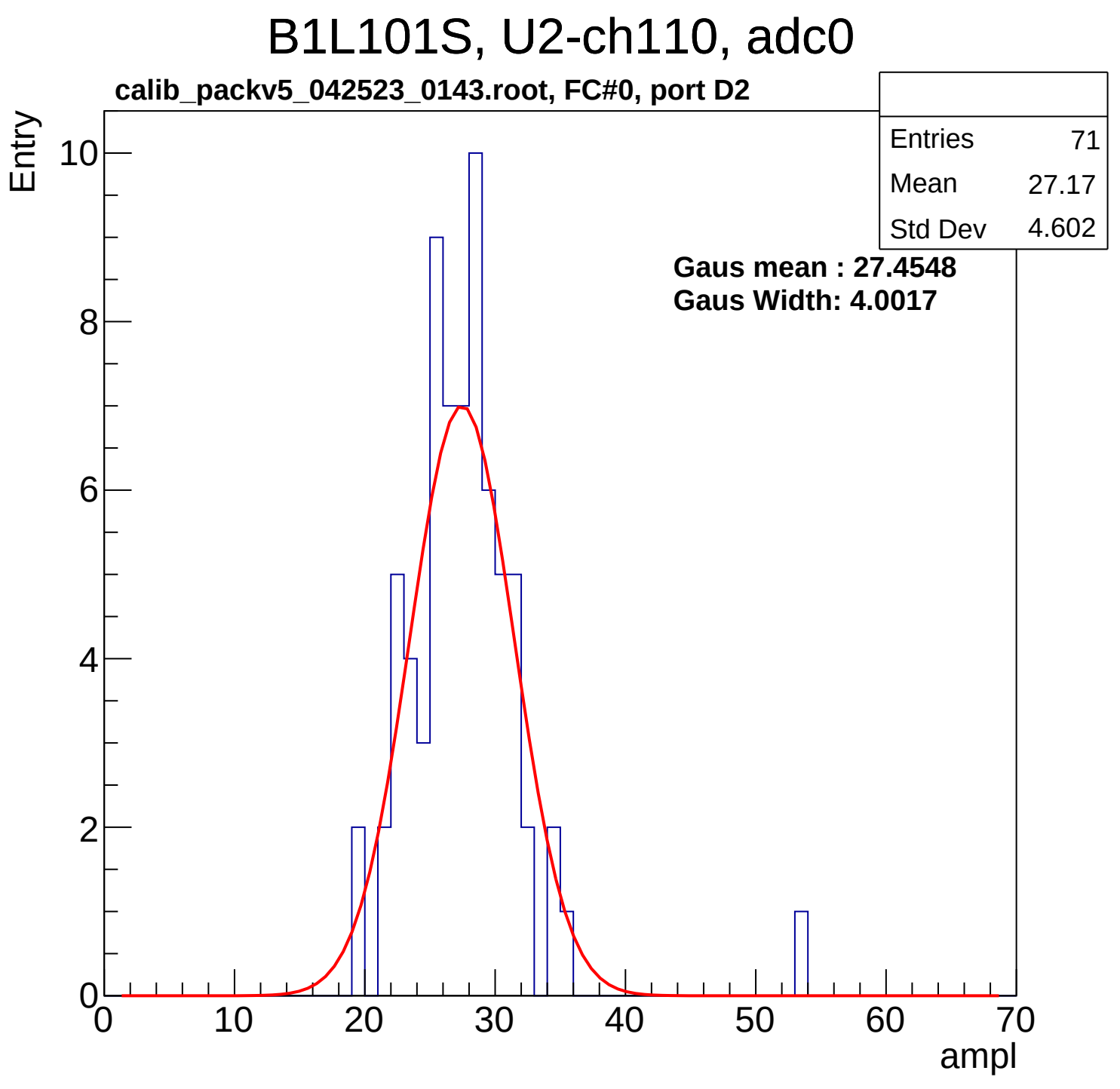

B1L101S, U2-ch109, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 47.75
Std Dev 3.579
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

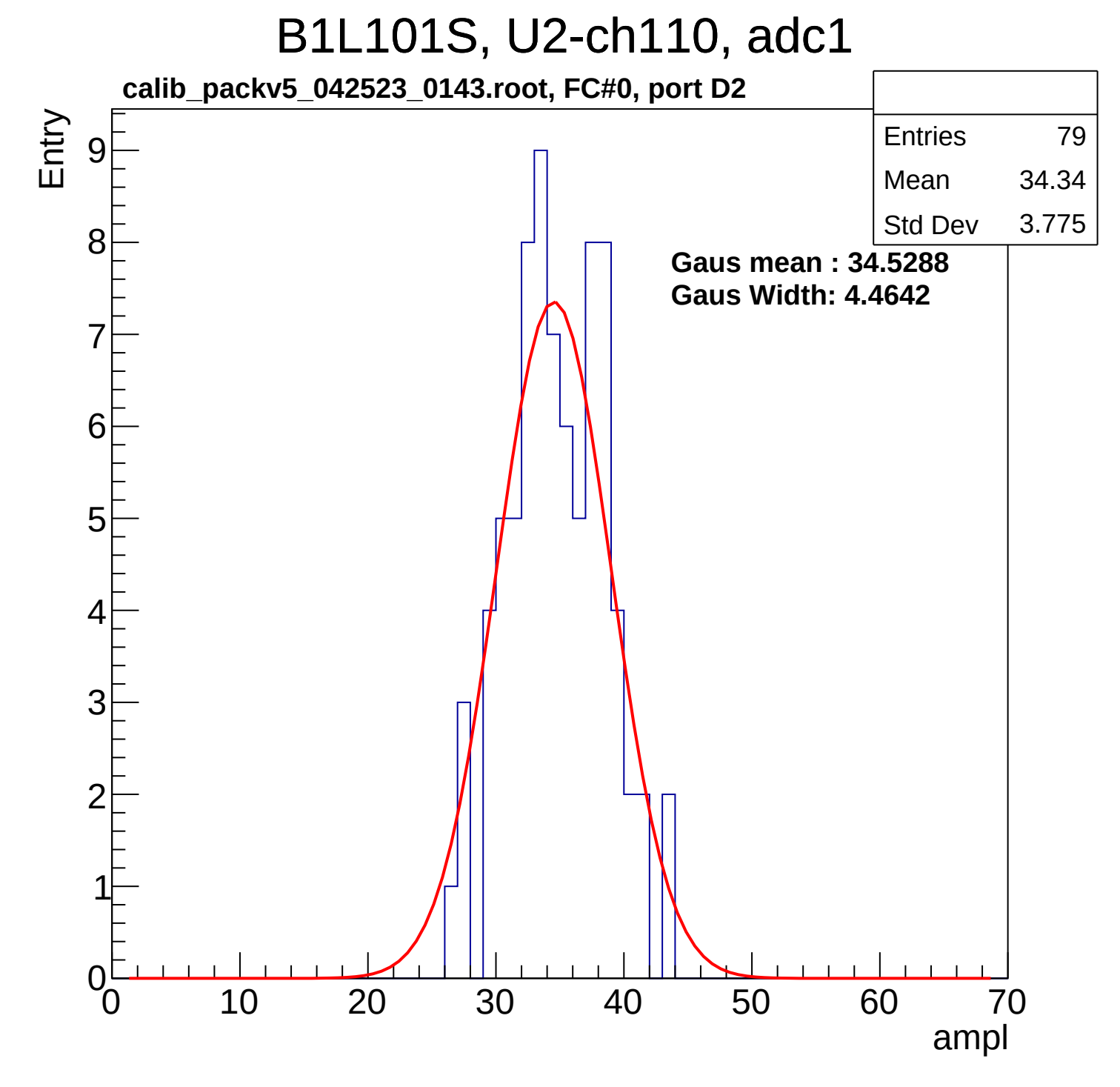

B1L101S, U2-ch109, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 54.35
Std Dev 3.451
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

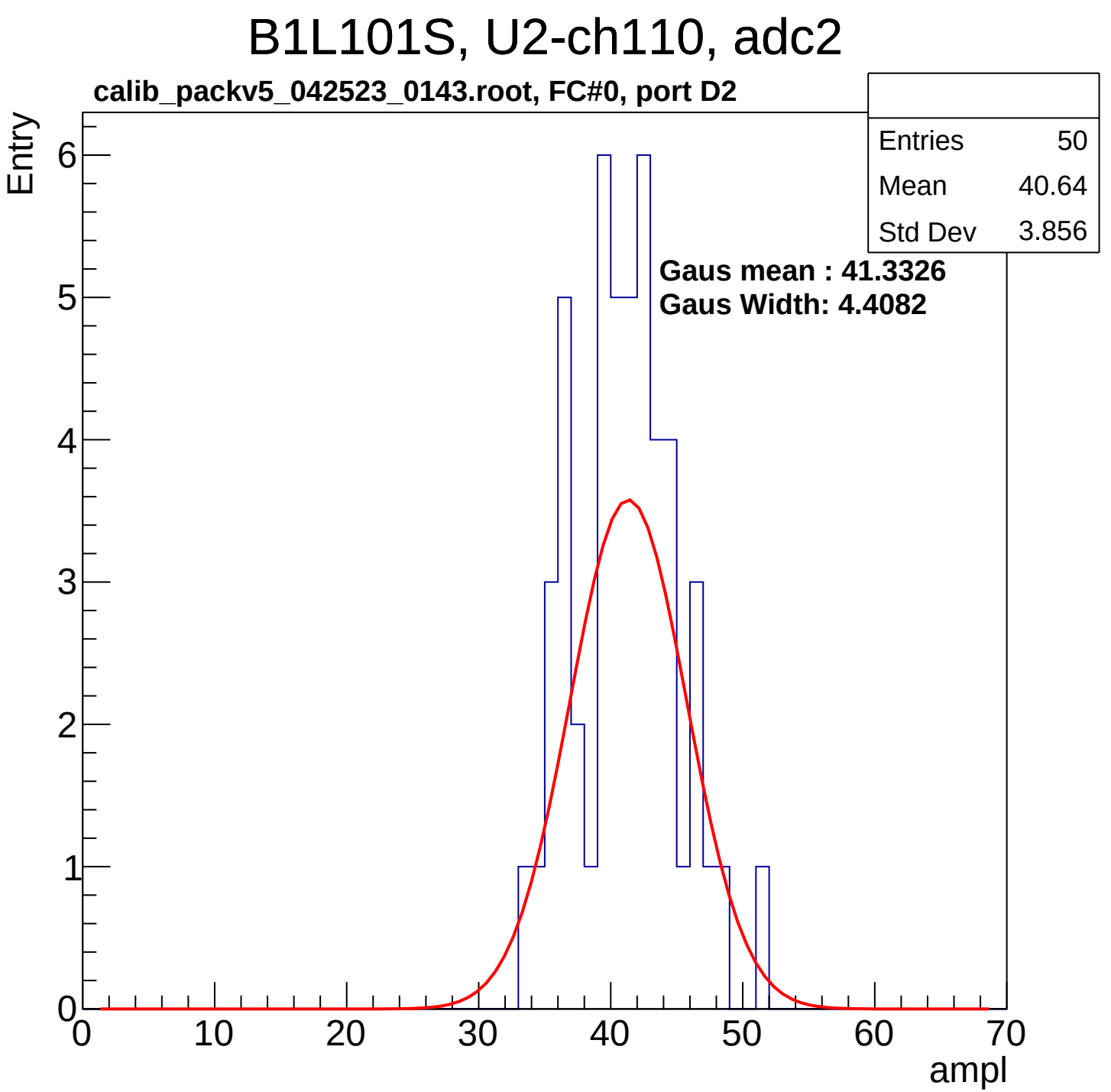

B1L101S, U2-ch109, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 59.85
Std Dev 2.288
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

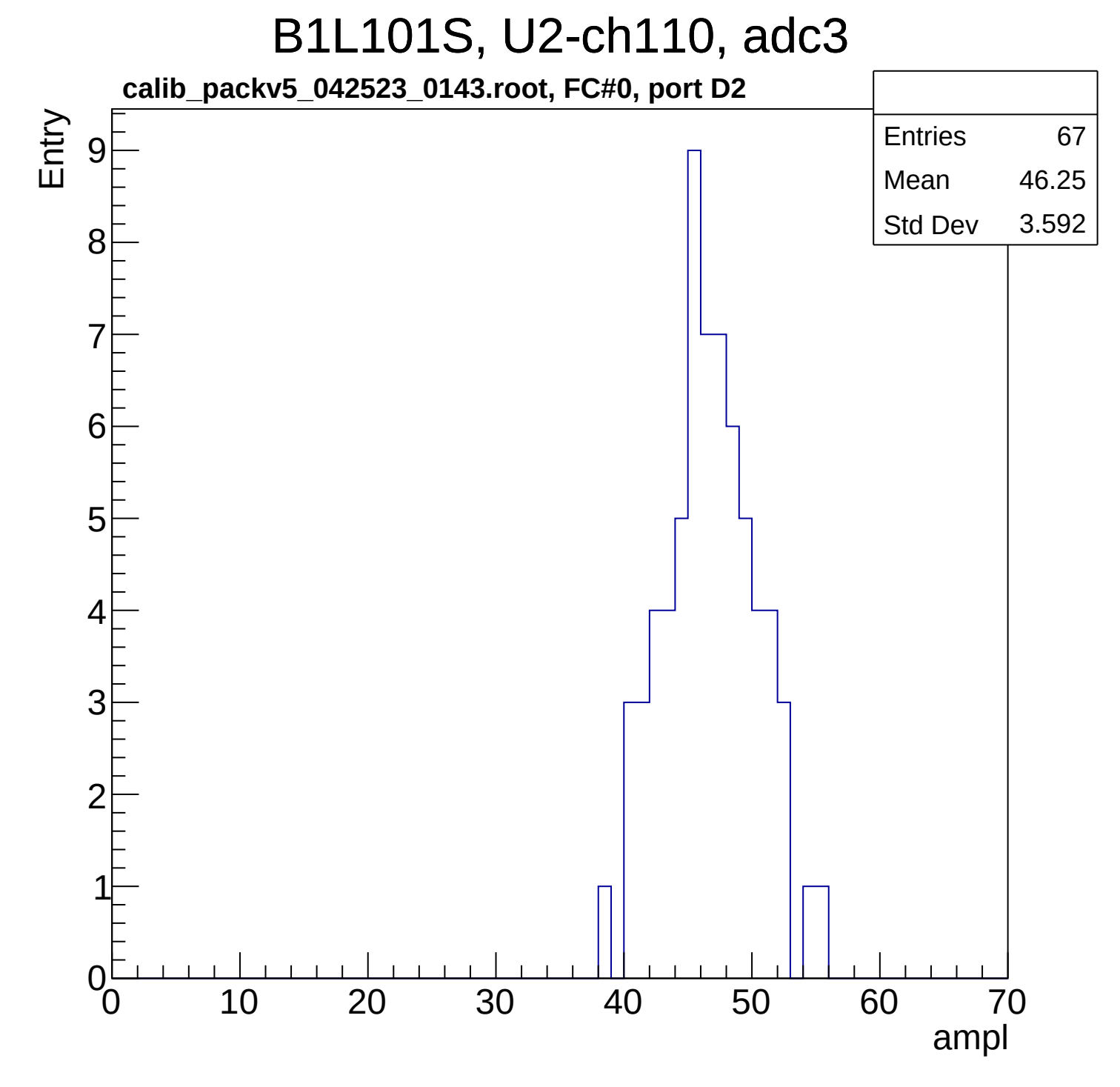

B1L101S, U2-ch109, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 55
Std Dev 19.48
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

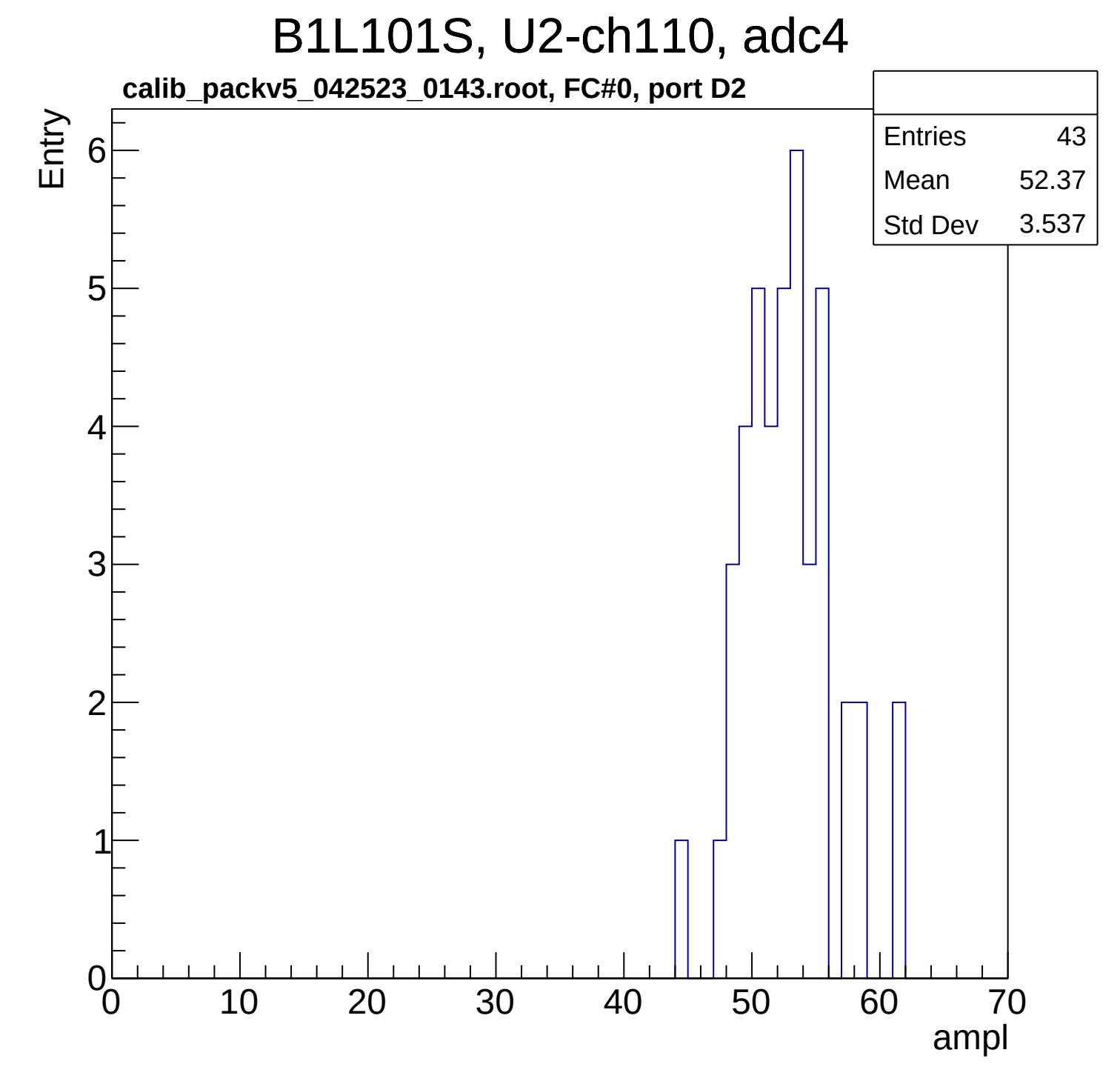

B1L101S, U2-ch109, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

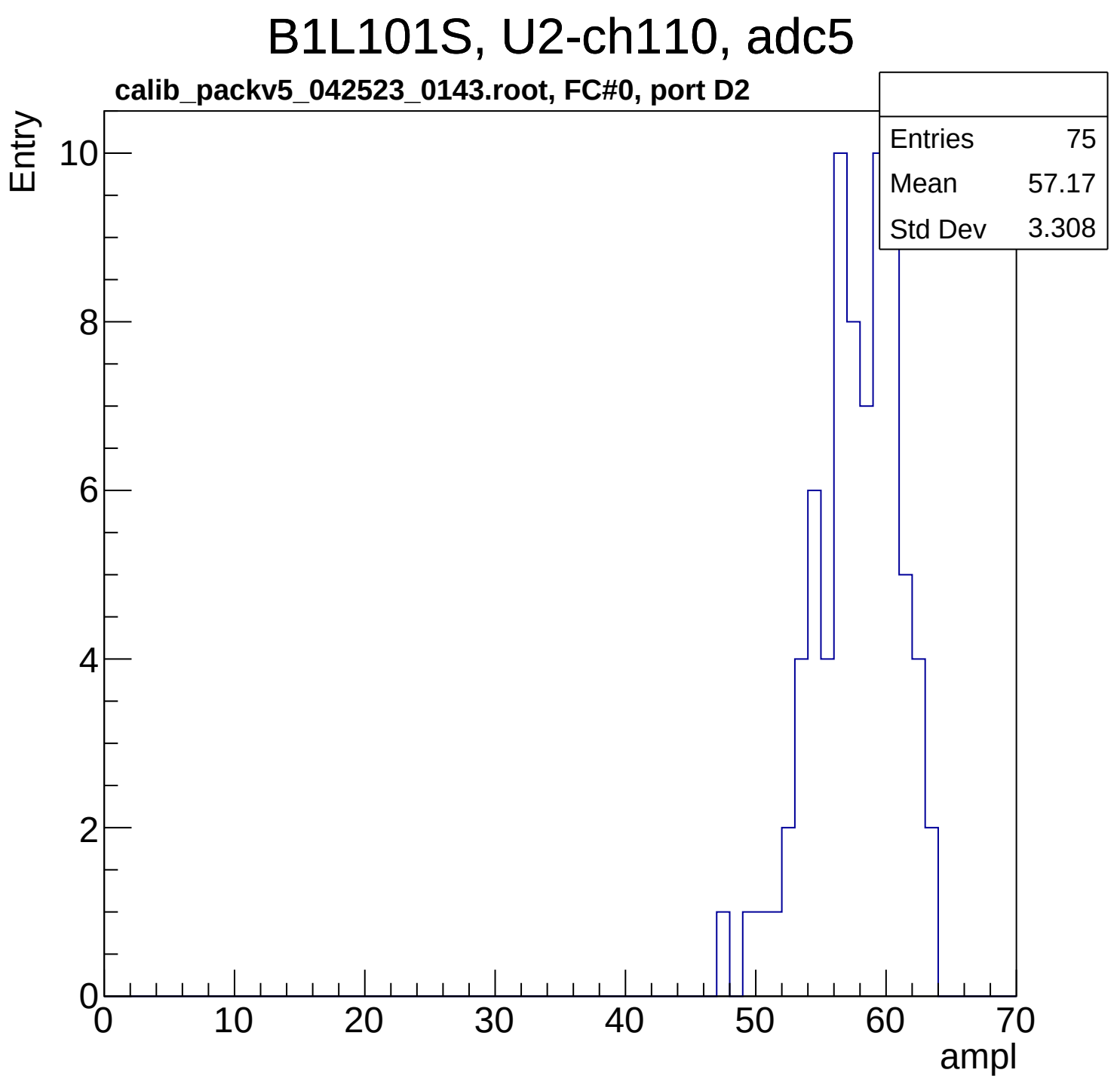

B1L101S, U2-ch110, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 27.17
Std Dev 4.602
Gaus mean : 27.4548
Gaus Width: 4.0017
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

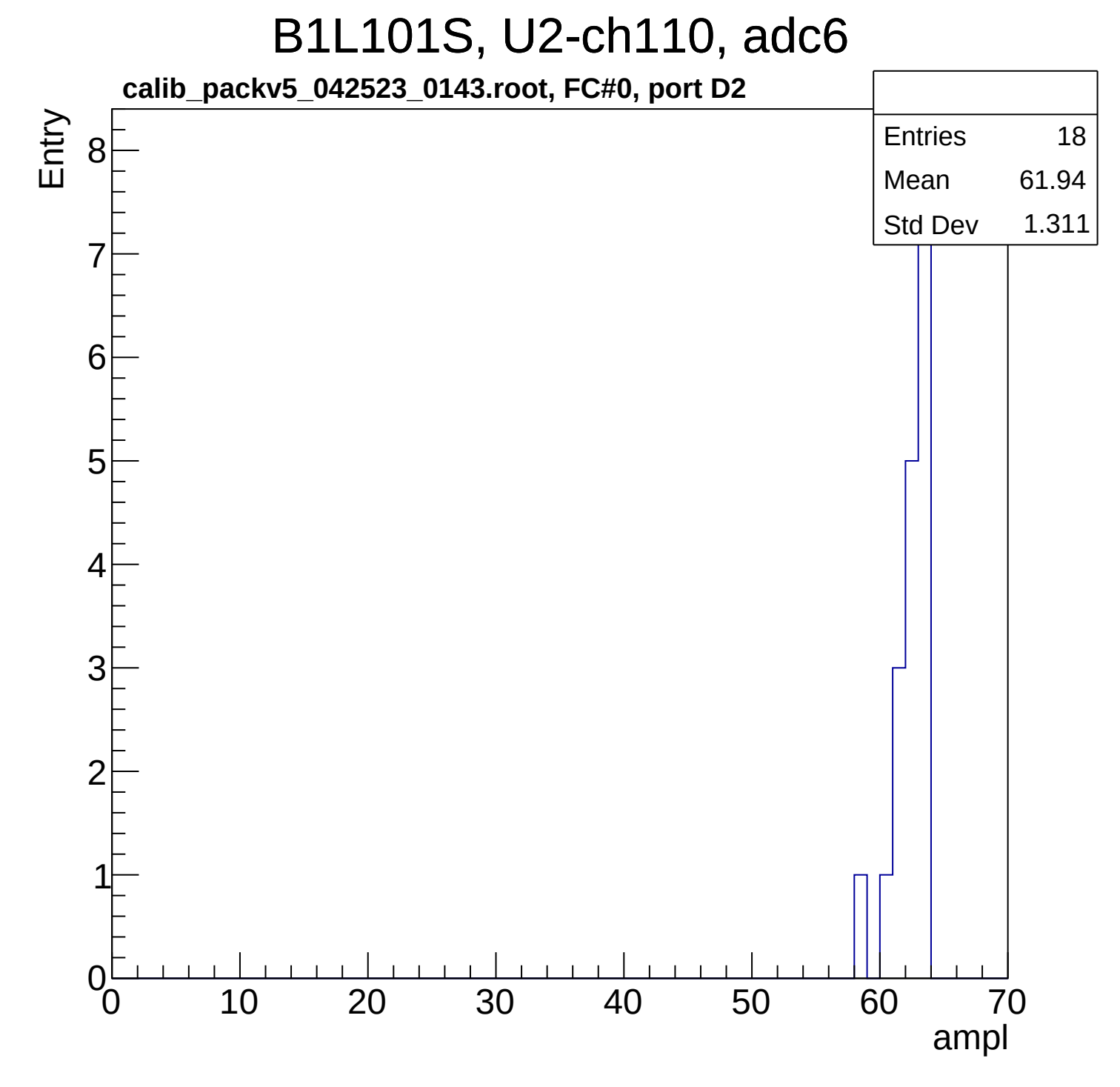

B1L101S, U2-ch110, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 34.34
Std Dev 3.775
Gaus mean : 34.5288
Gaus Width: 4.4642
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

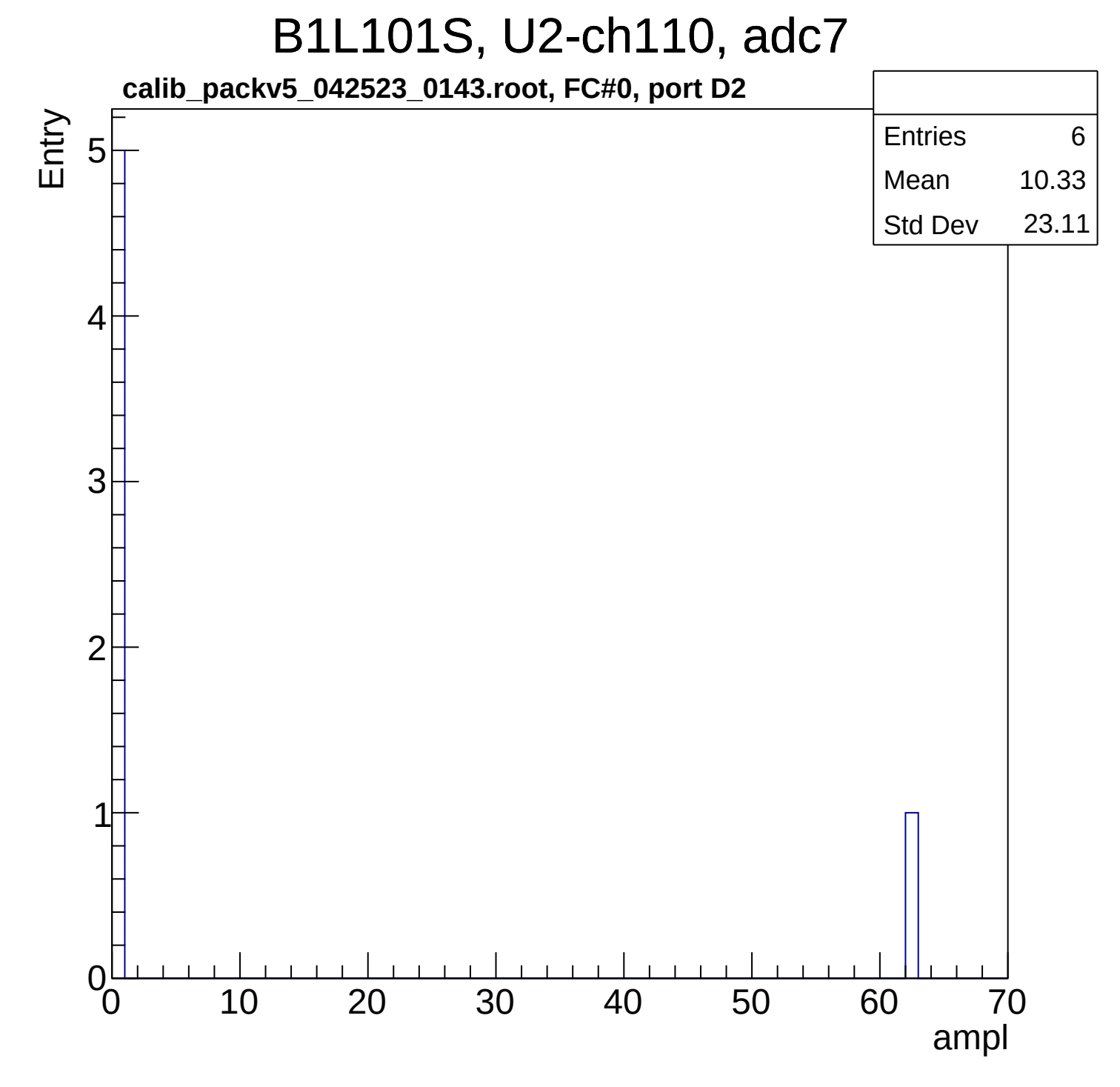

B1L101S, U2-ch110, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 50
Mean 40.64
Std Dev 3.856
Gaus mean : 41.3326
Gaus Width: 4.4082
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

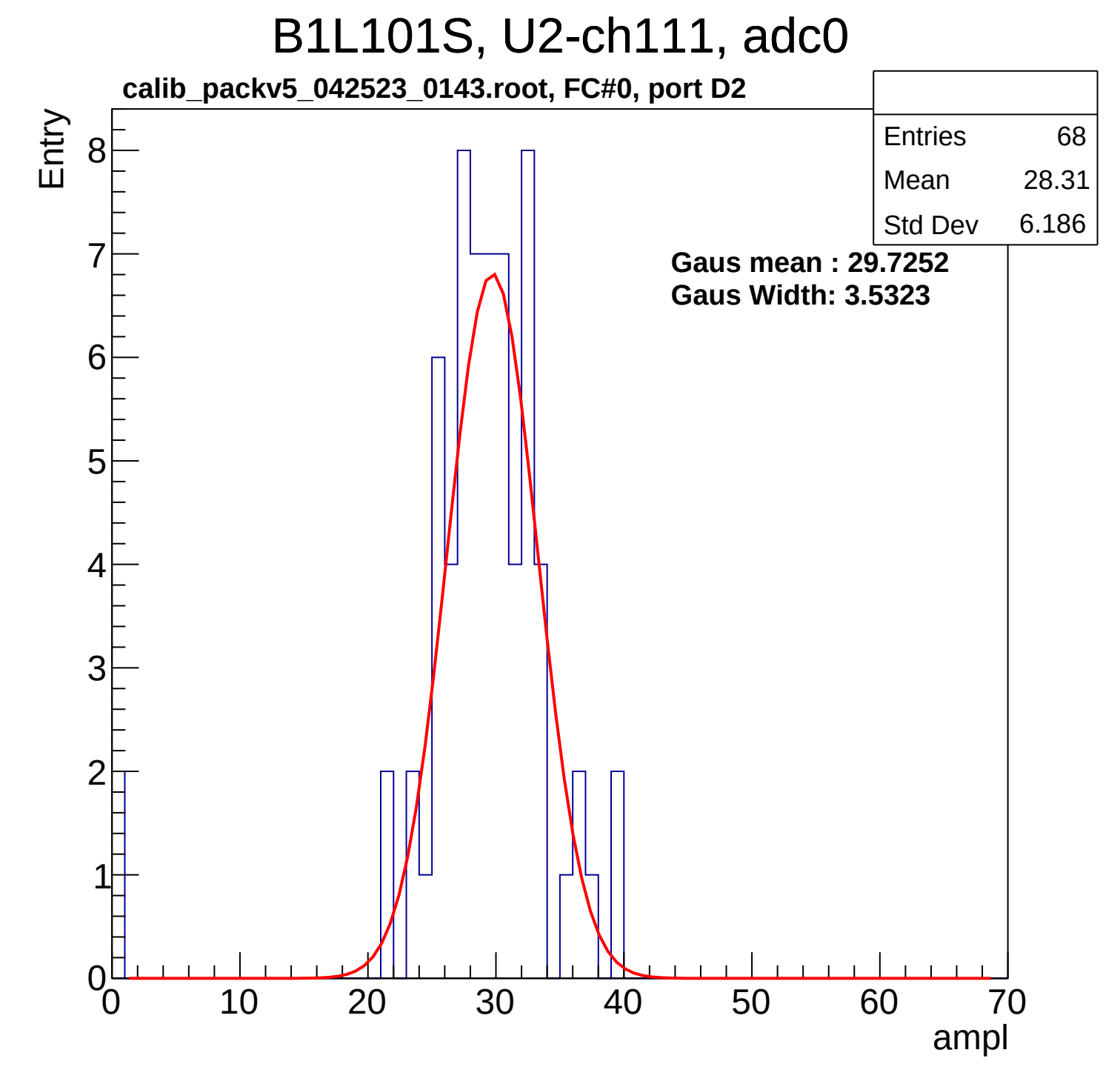

B1L101S, U2-ch110, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 46.25
Std Dev 3.592
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

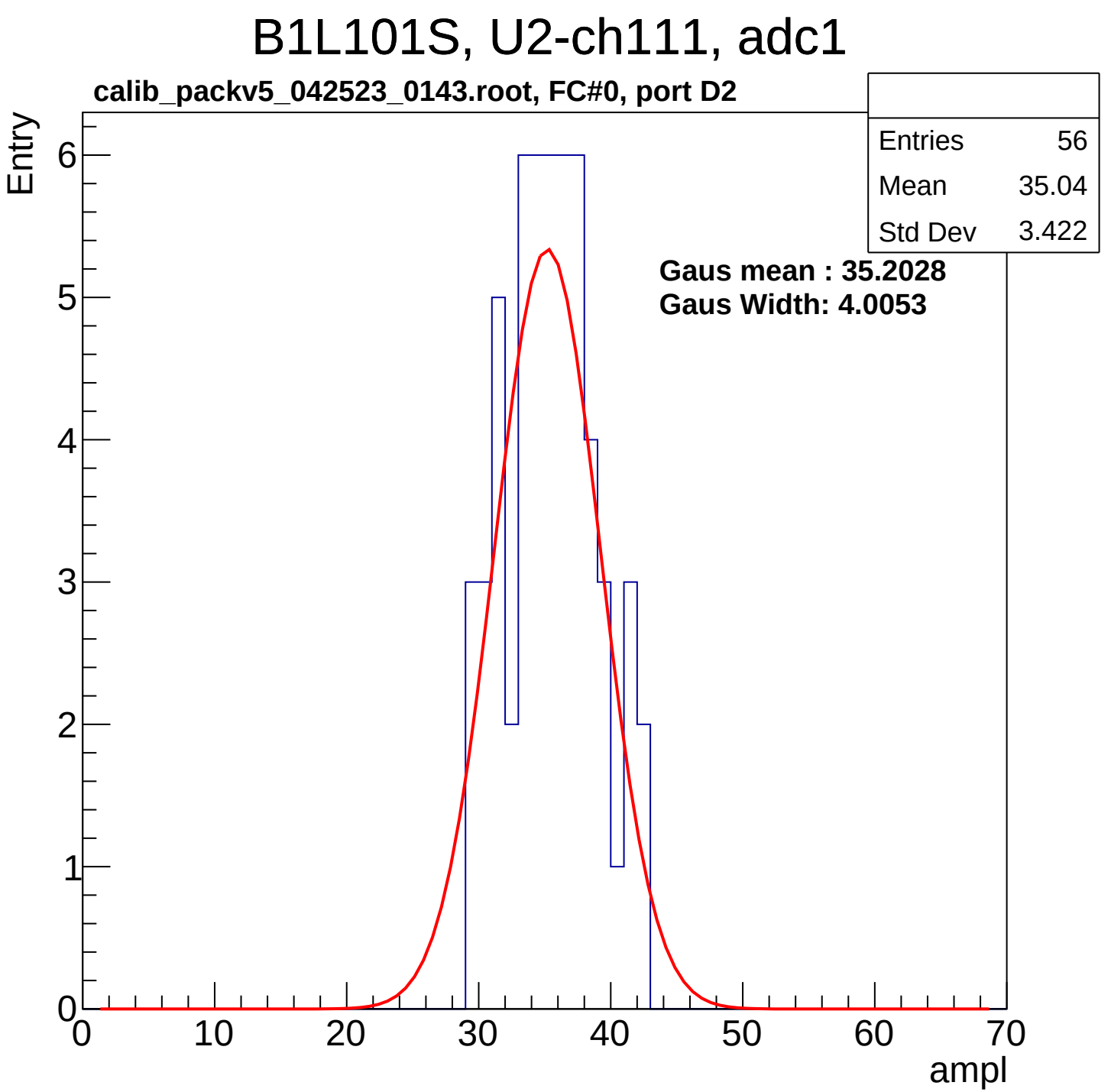

B1L101S, U2-ch110, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 43
Mean 52.37
Std Dev 3.537
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

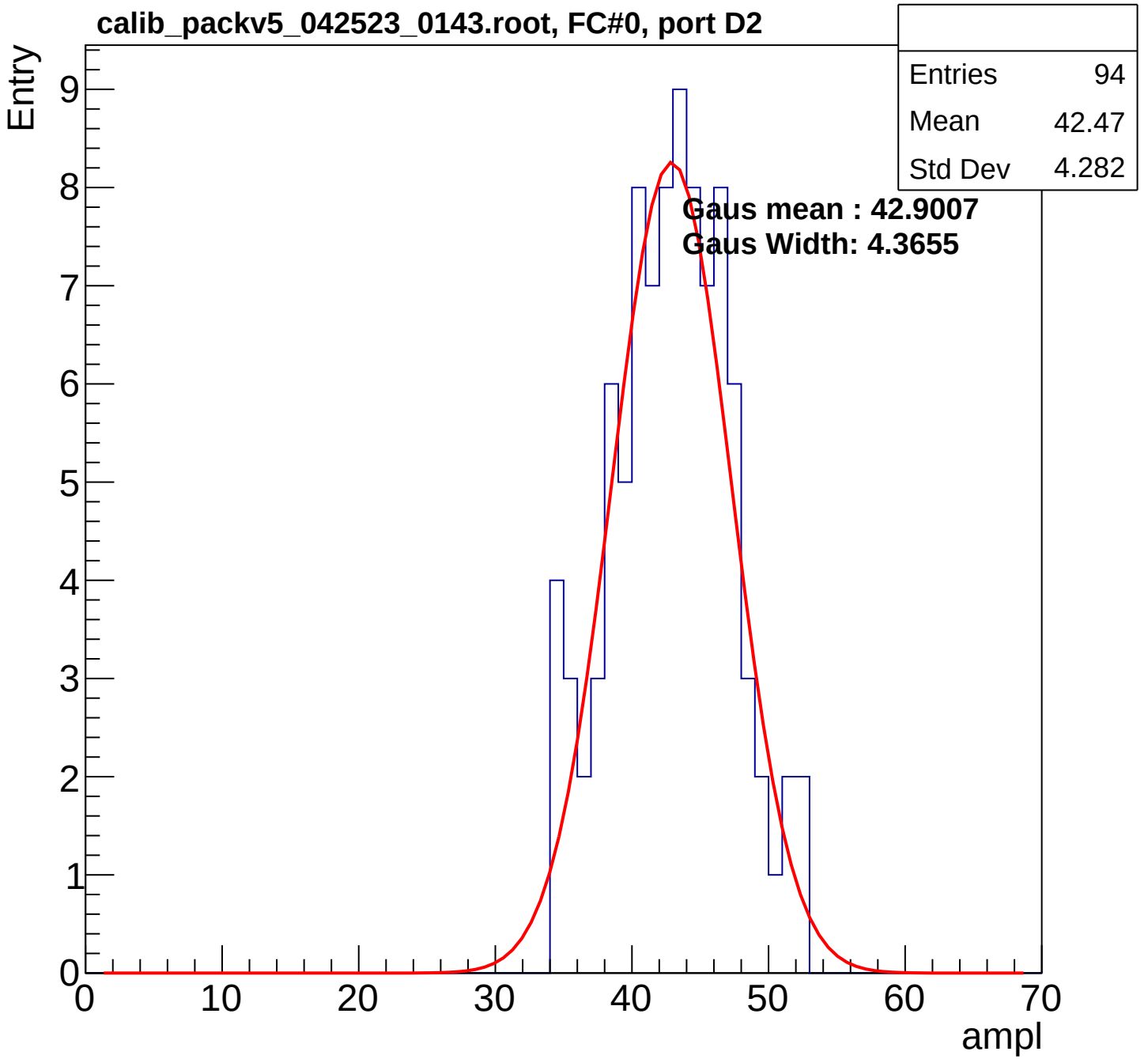

B1L101S, U2-ch110, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 75
Mean 57.17
Std Dev 3.308
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

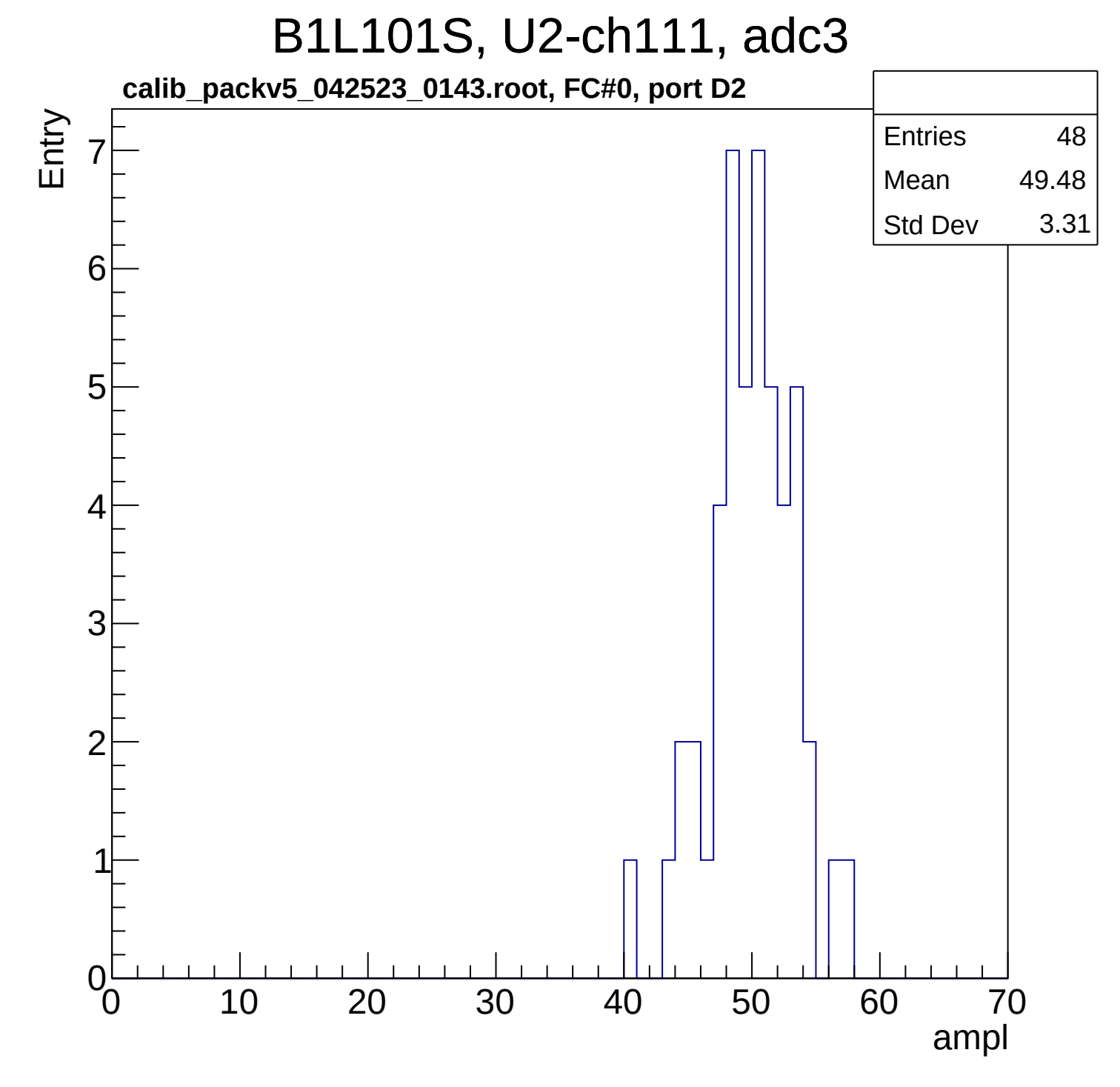

B1L101S, U2-ch110, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 18
Mean 61.94
Std Dev 1.311
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

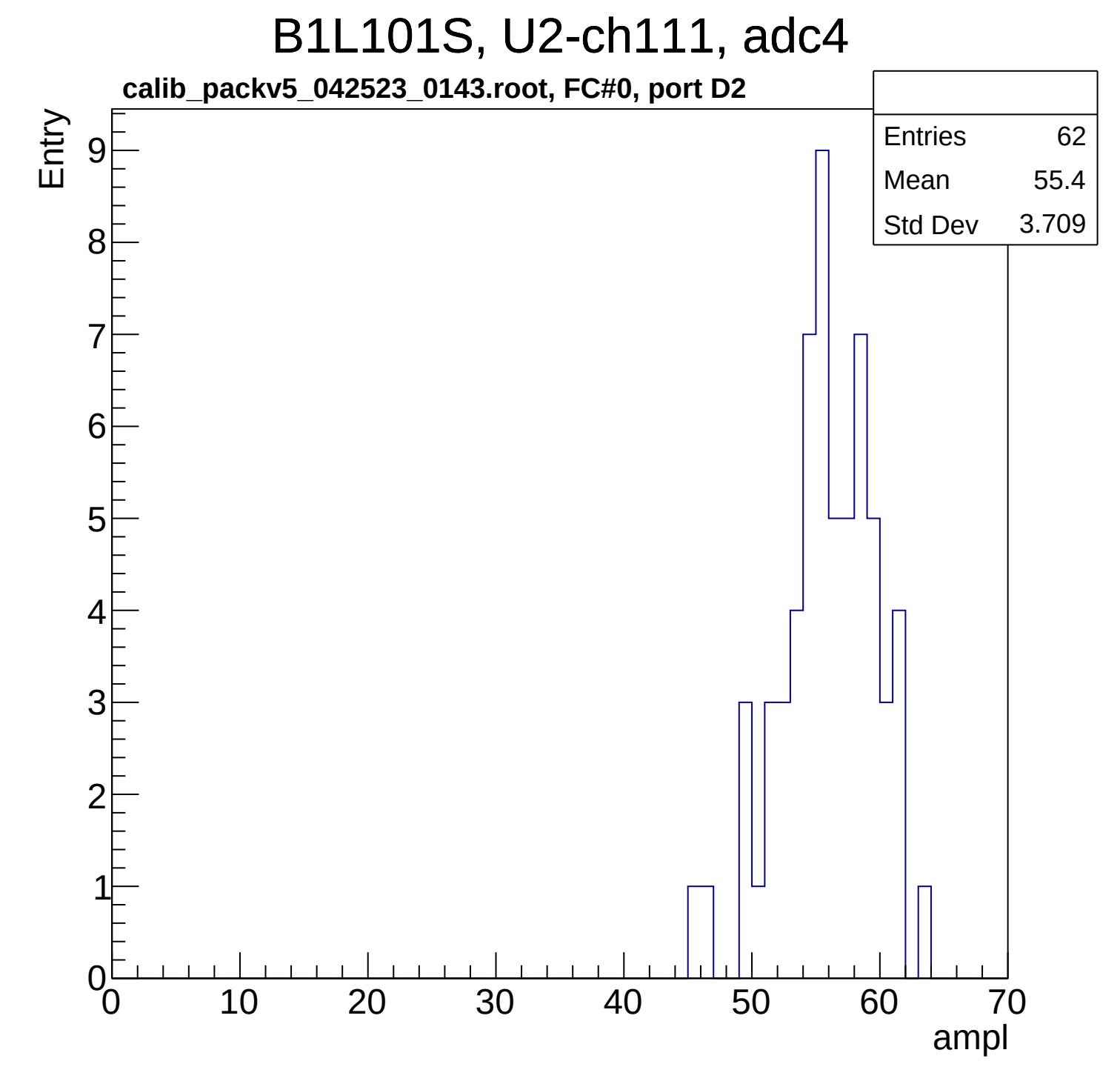

B1L101S, U2-ch110, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 10.33
Std Dev 23.11
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

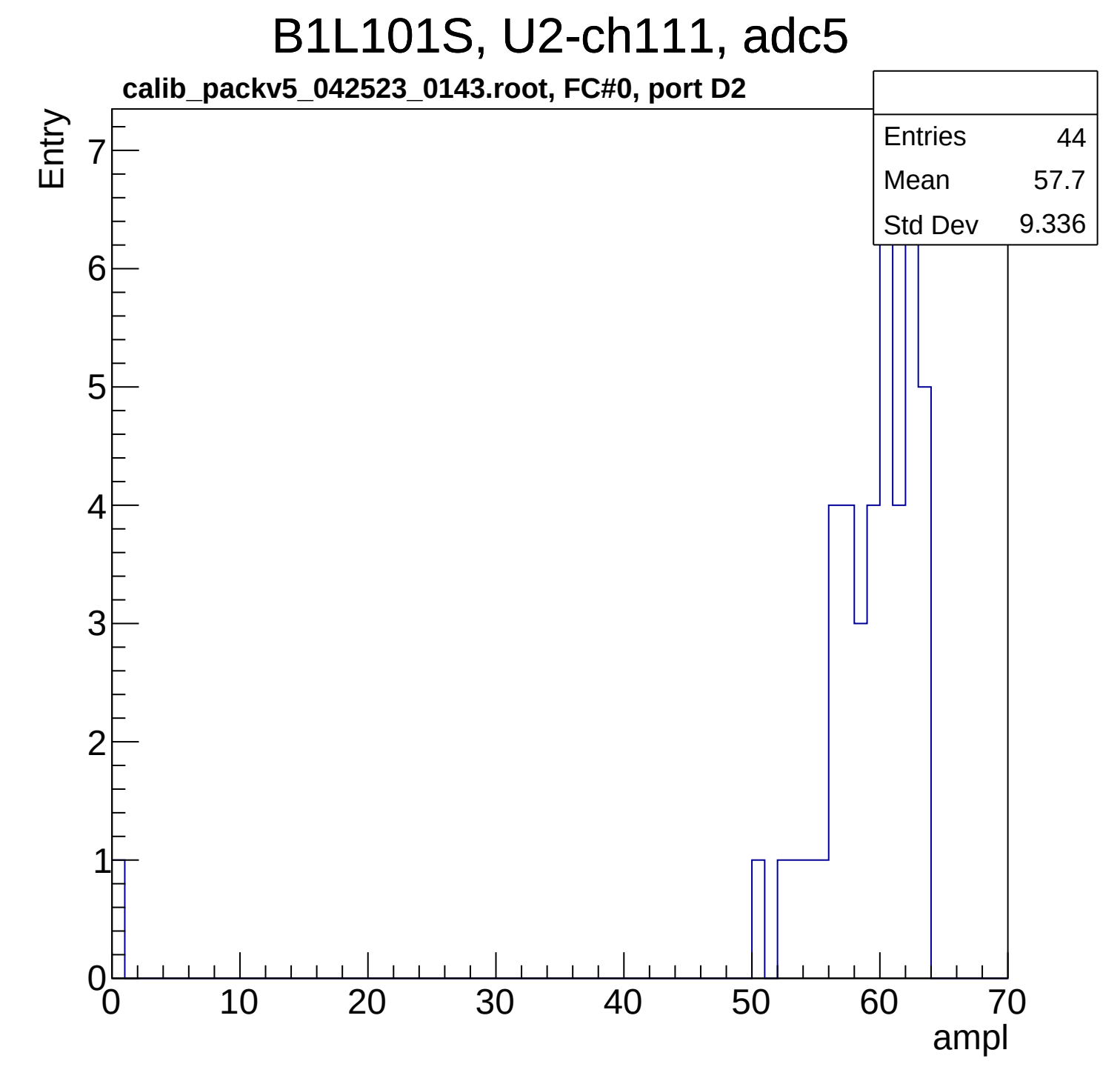

B1L101S, U2-ch111, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 28.31
Std Dev 6.186
Gaus mean : 29.7252
Gaus Width: 3.5323
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

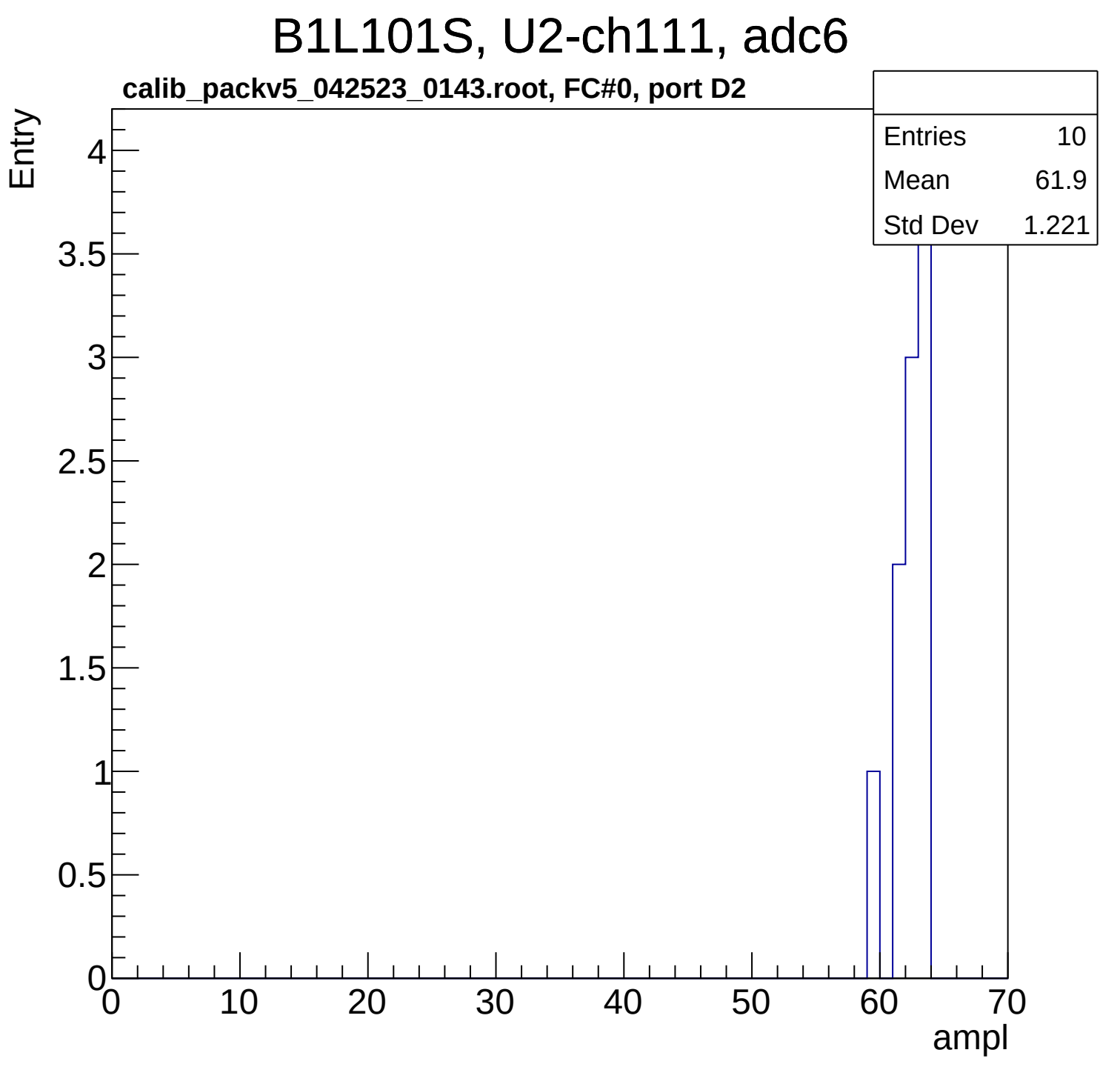

B1L101S, U2-ch111, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 35.04
Std Dev 3.422
Gaus mean : 35.2028
Gaus Width: 4.0053
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

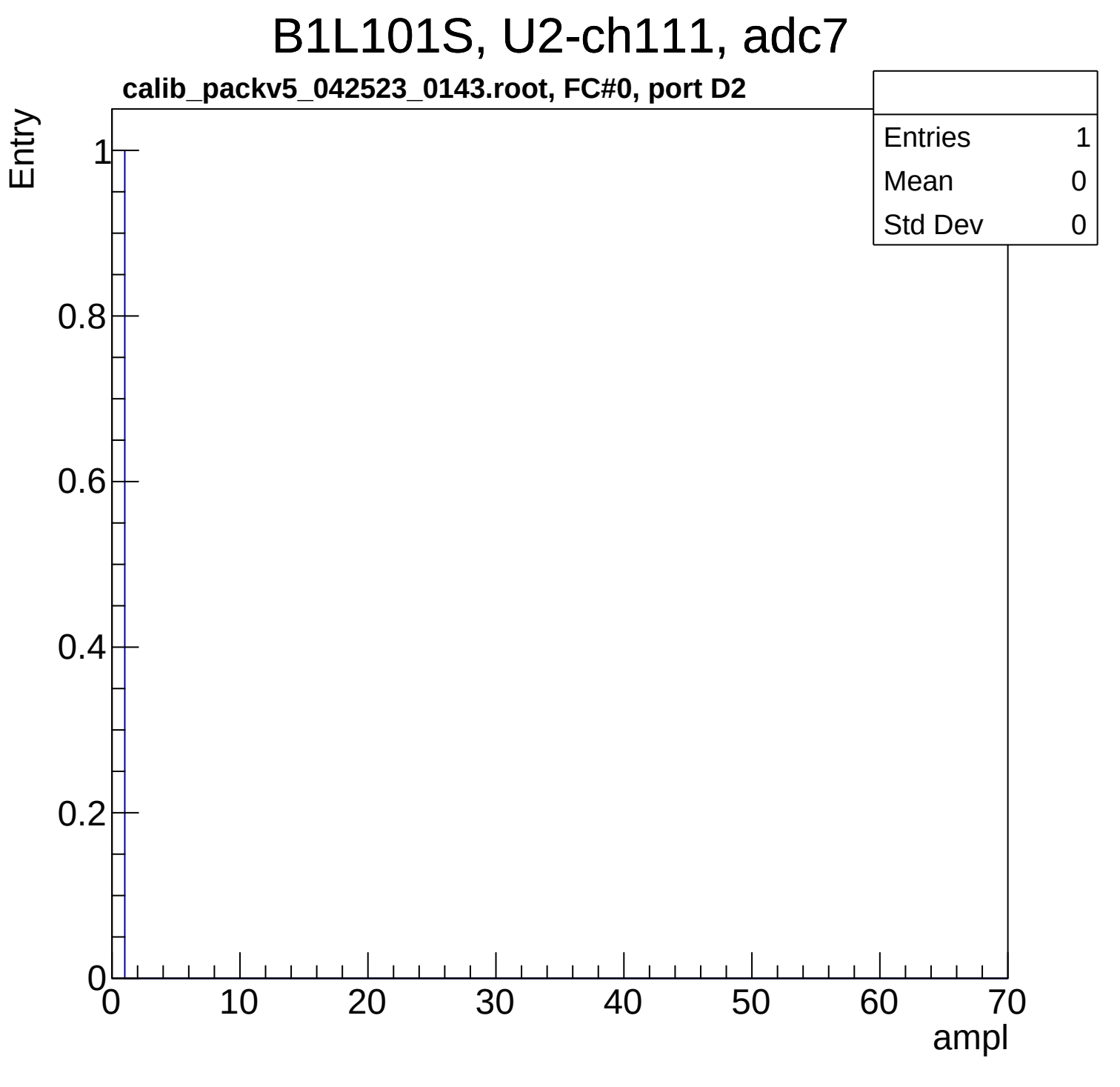

B1L101S, U2-ch111, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 94
Mean 42.47
Std Dev 4.282
Gaus mean : 42.9007
Gaus Width: 4.3655
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

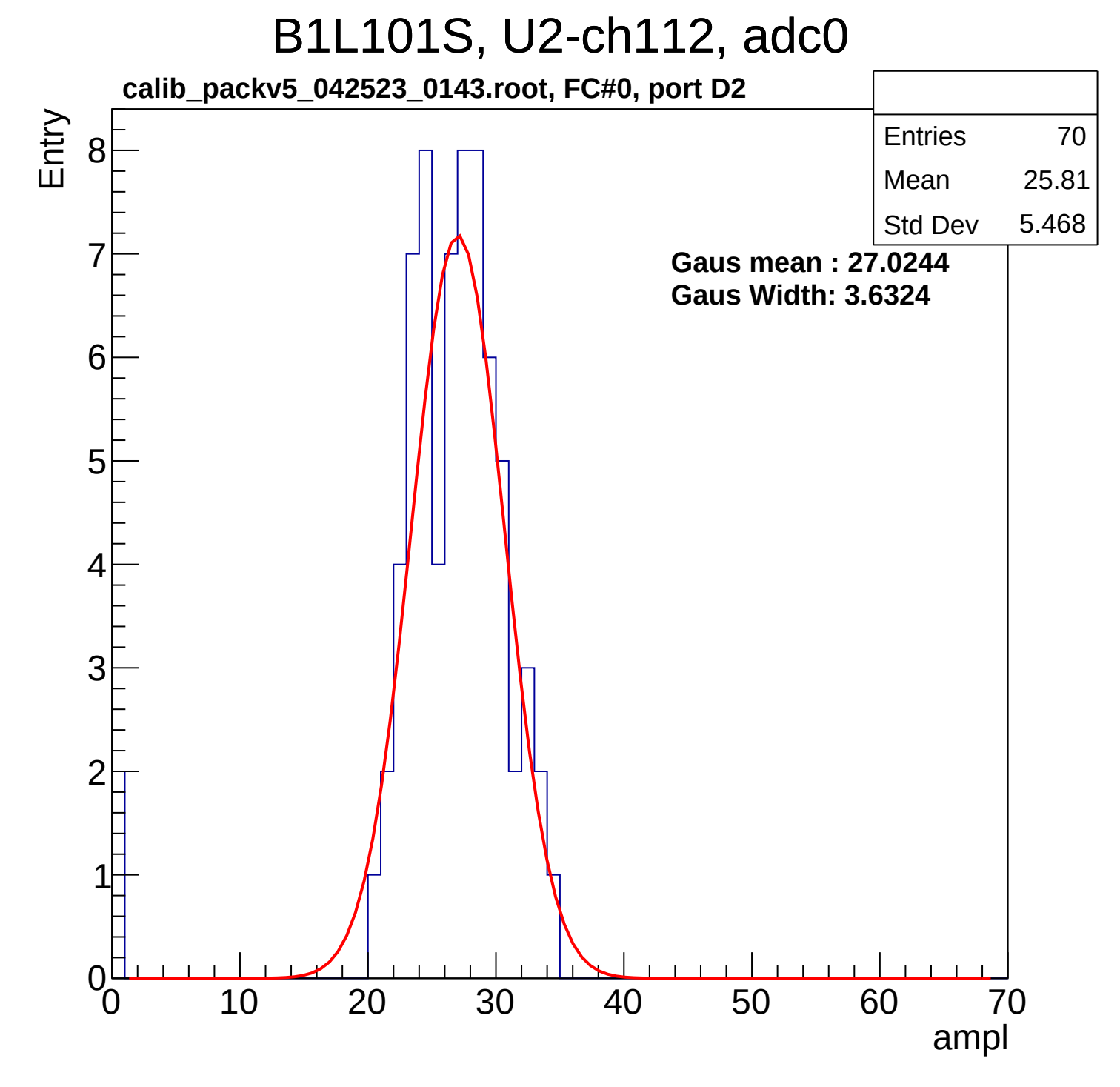

B1L101S, U2-ch111, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 49.48
Std Dev 3.31
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

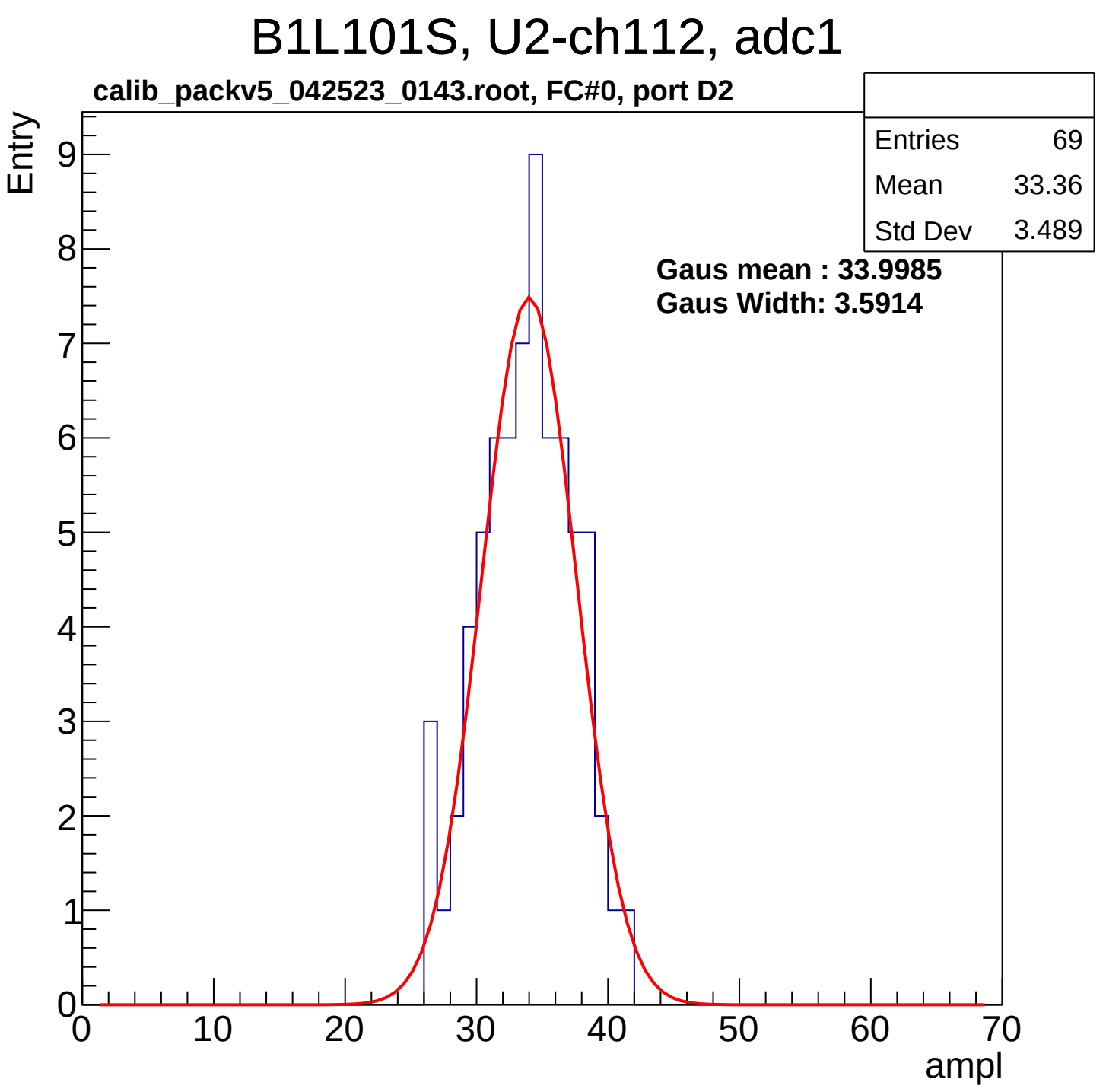

B1L101S, U2-ch111, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 55.4
Std Dev 3.709
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

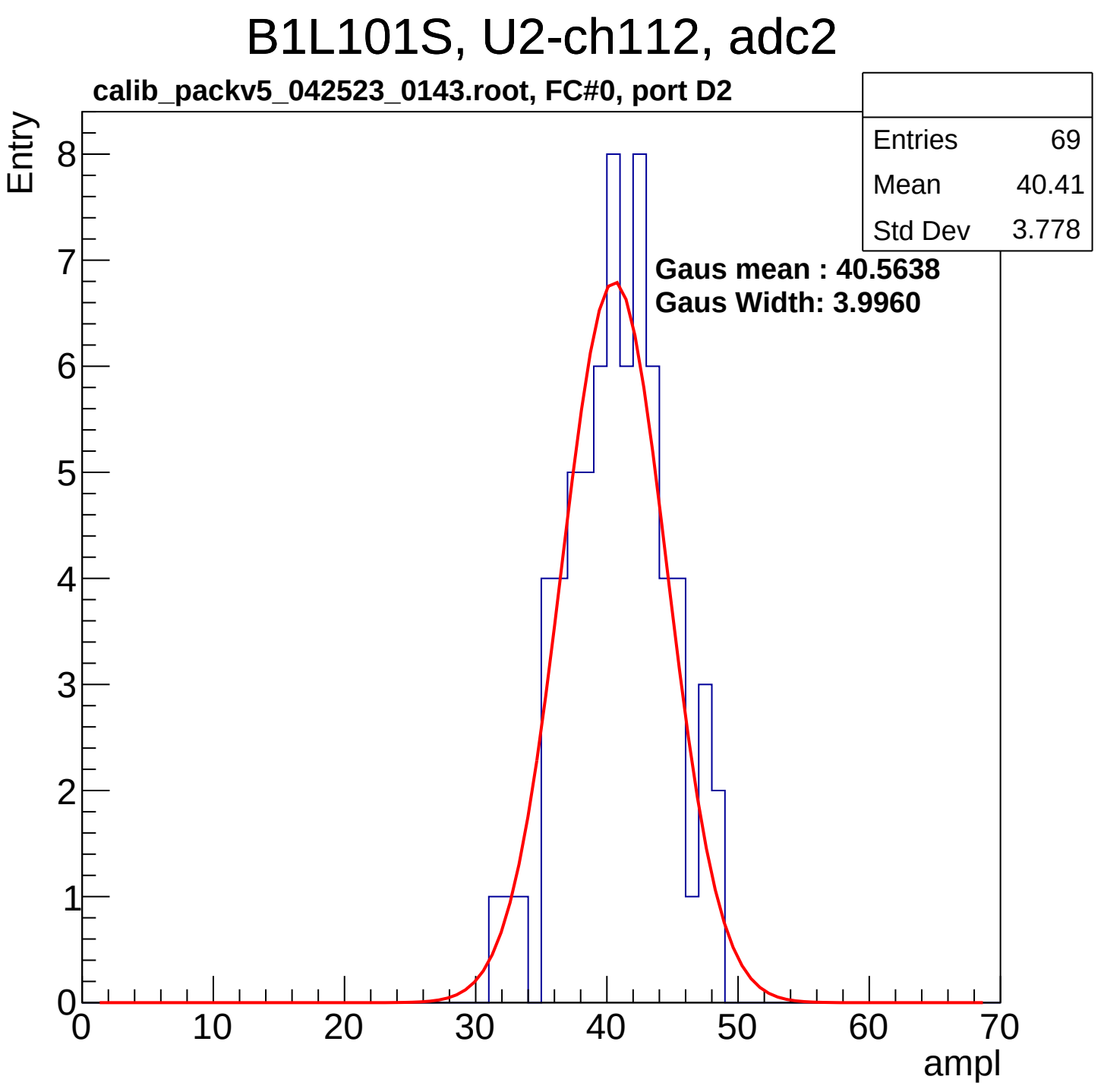

B1L101S, U2-ch111, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 44
Mean 57.7
Std Dev 9.336
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

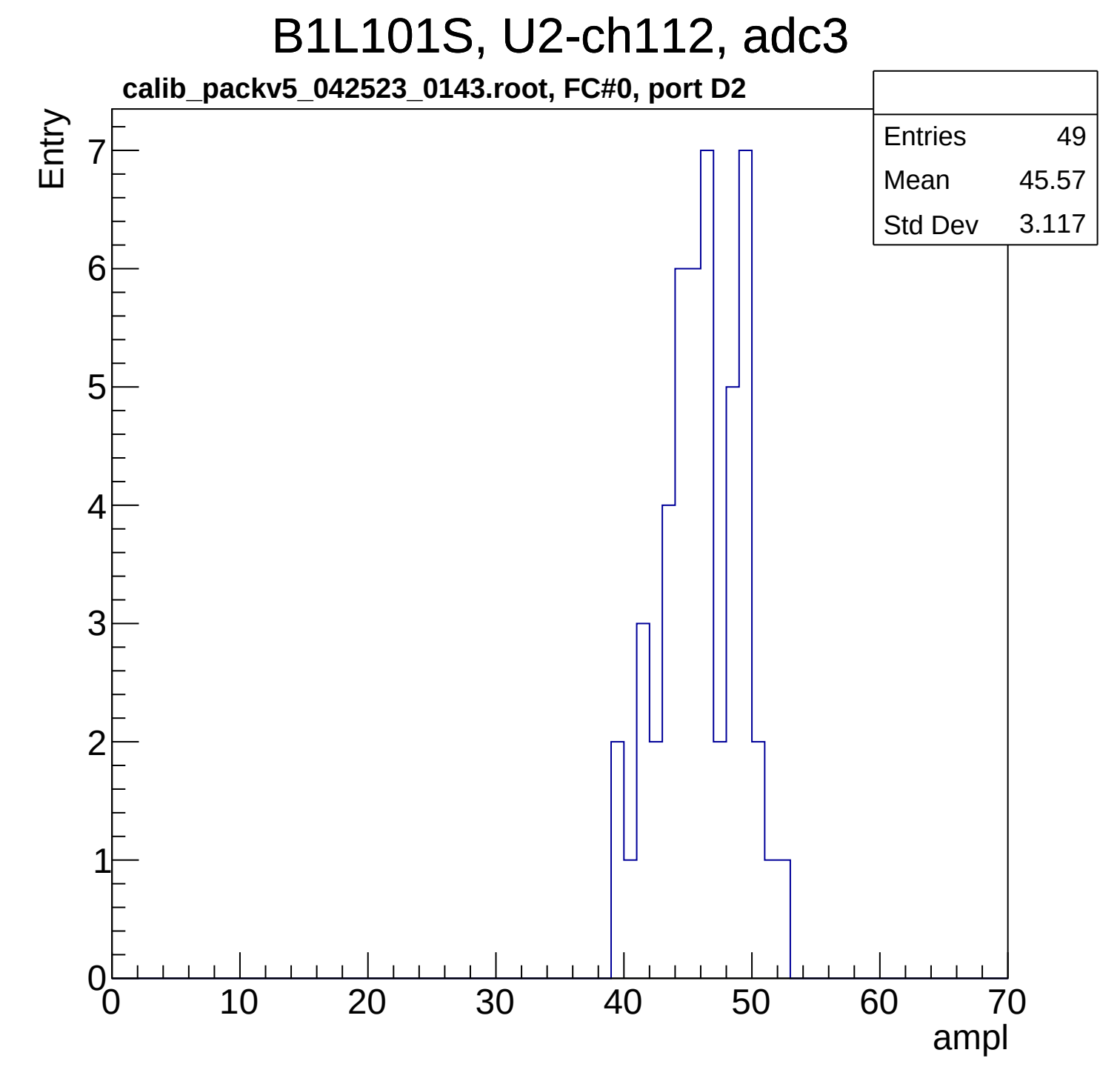

B1L101S, U2-ch111, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 61.9
Std Dev 1.221
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

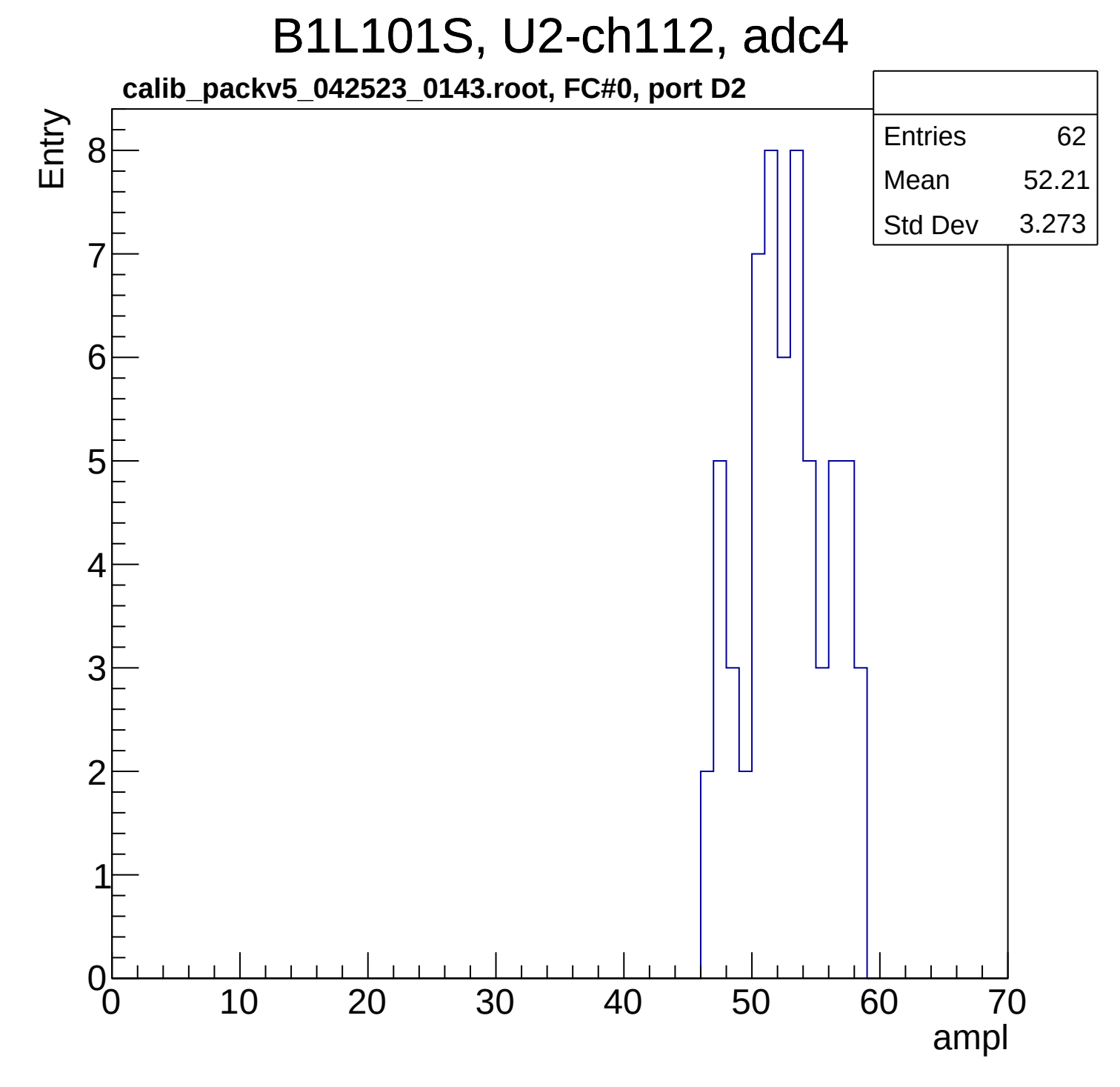

B1L101S, U2-ch111, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

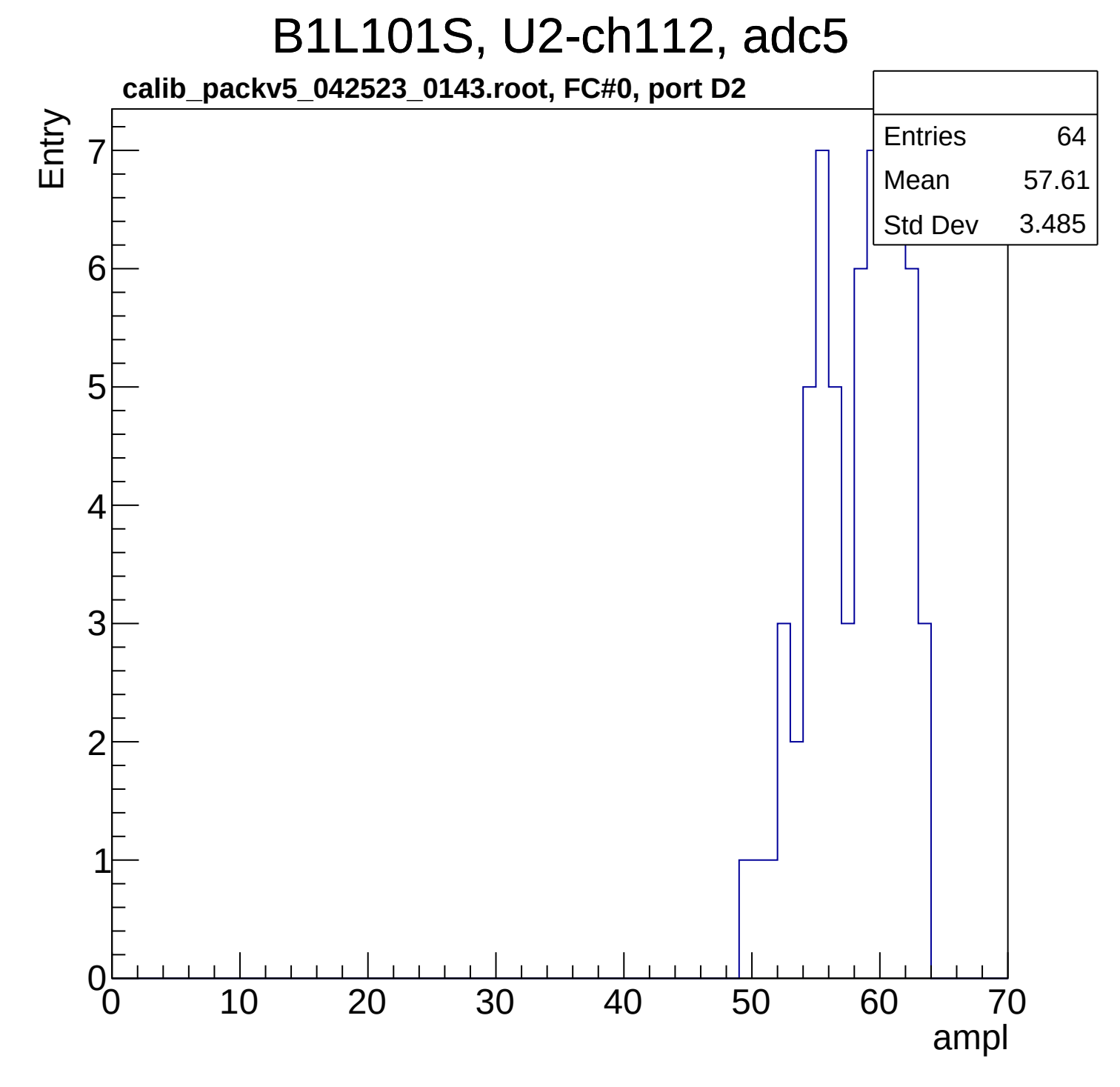

B1L101S, U2-ch112, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 25.81
Std Dev 5.468
Gaus mean : 27.0244
Gaus Width: 3.6324
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

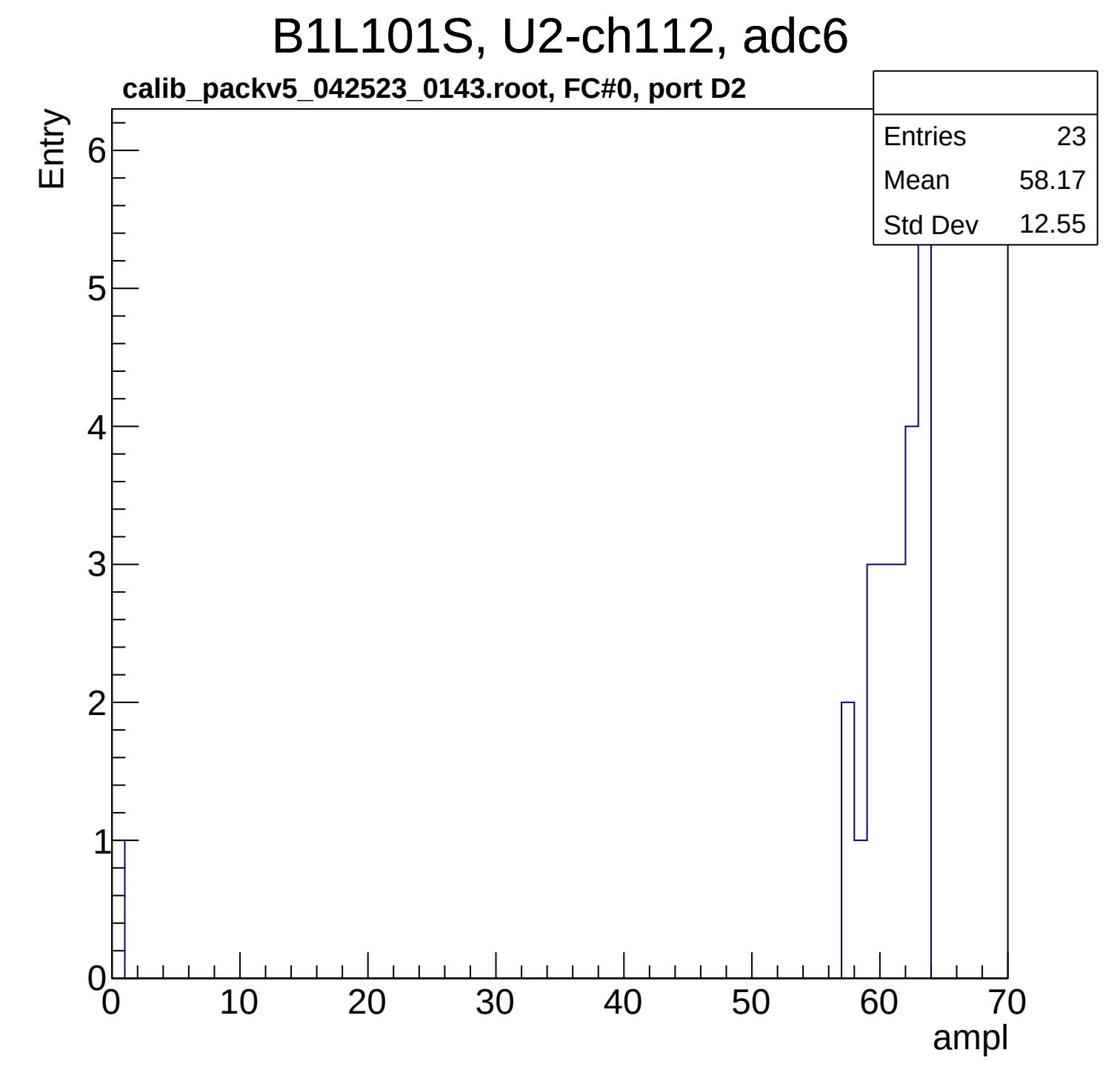

B1L101S, U2-ch112, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 33.36
Std Dev 3.489
Gaus mean : 33.9985
Gaus Width: 3.5914
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

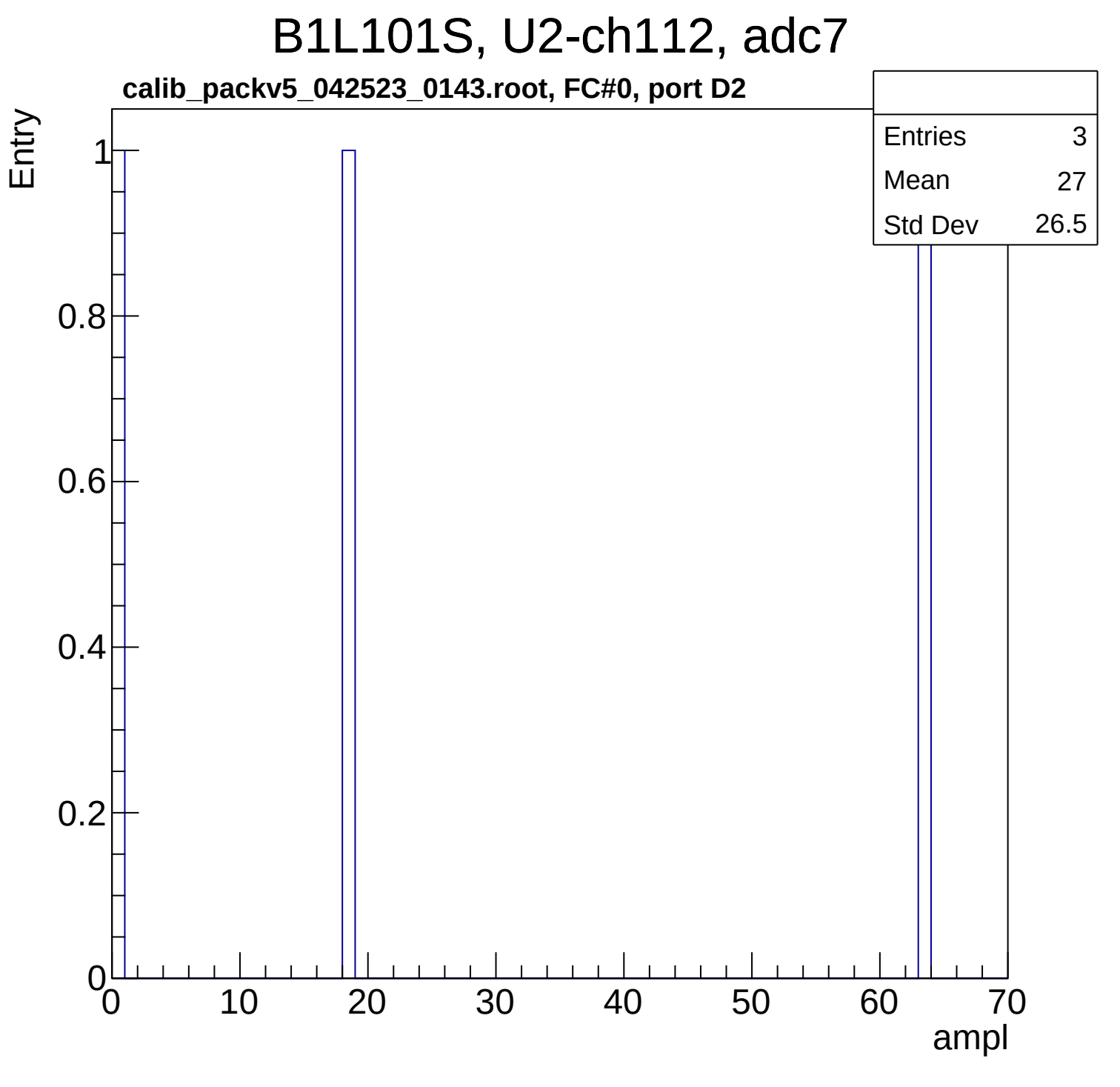

B1L101S, U2-ch112, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 40.41
Std Dev 3.778
Gaus mean : 40.5638
Gaus Width: 3.9960
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

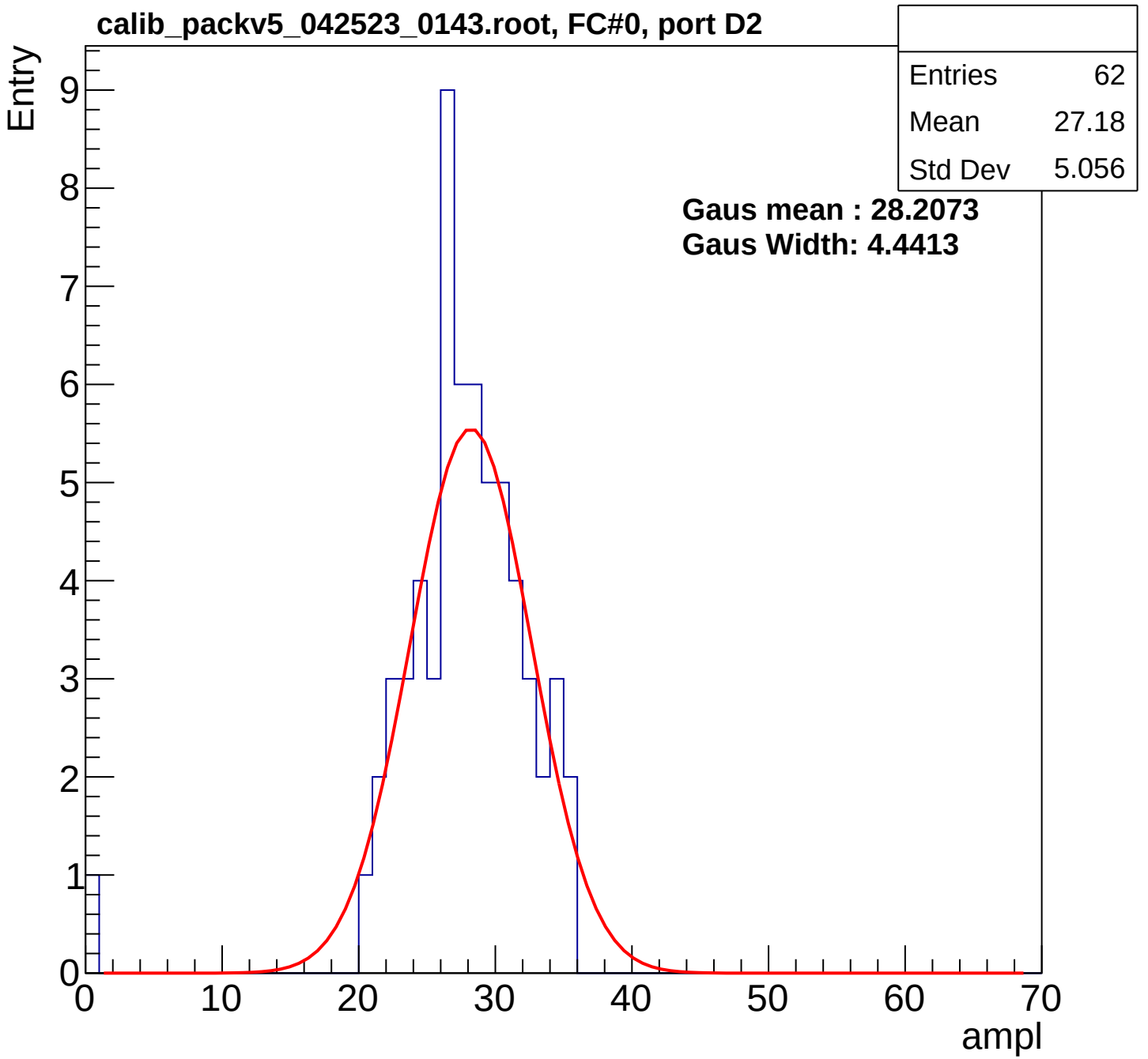

B1L101S, U2-ch112, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 45.57
Std Dev 3.117
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

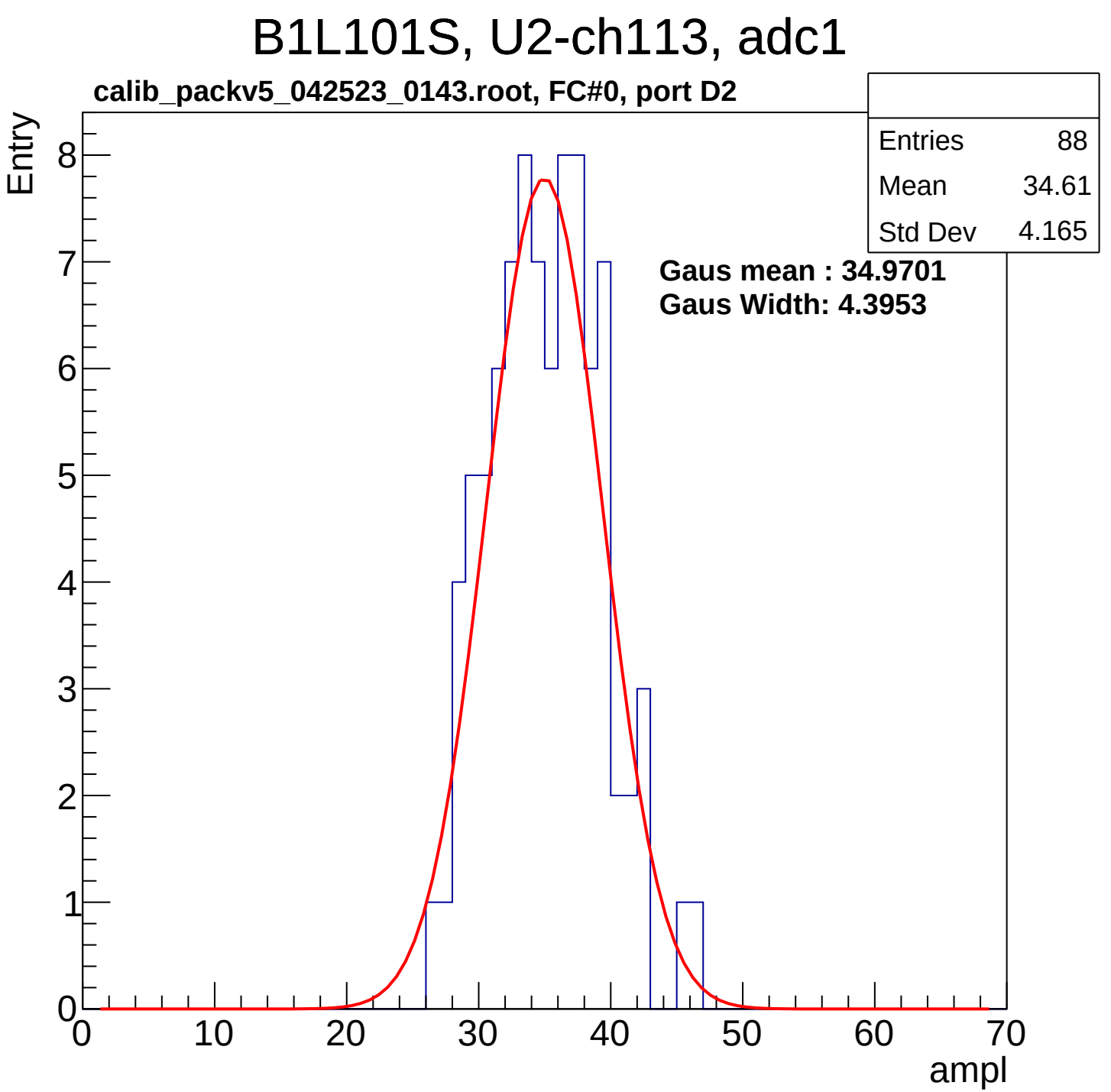

B1L101S, U2-ch112, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 52.21
Std Dev 3.273
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

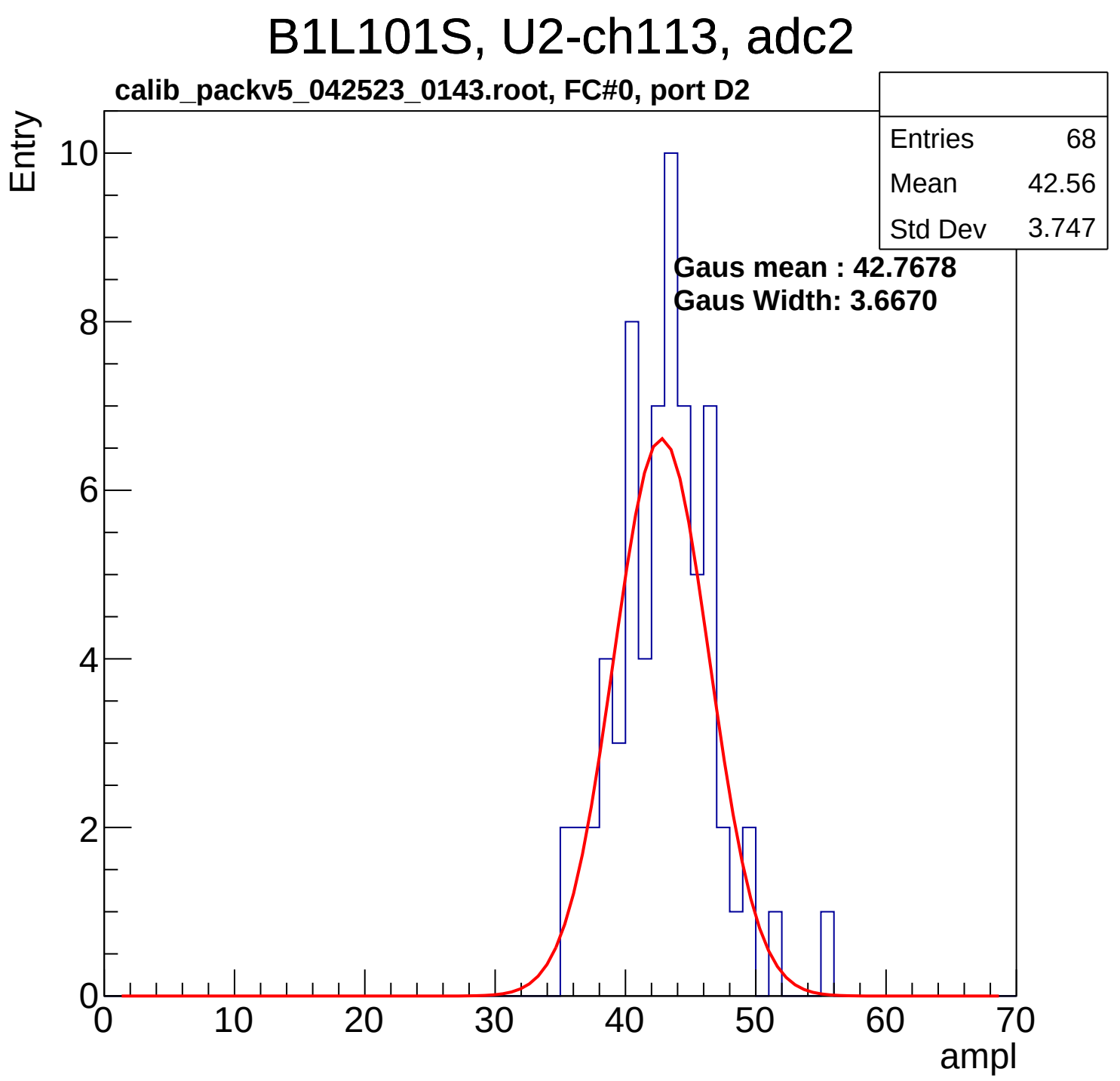

B1L101S, U2-ch112, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 57.61
Std Dev 3.485
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

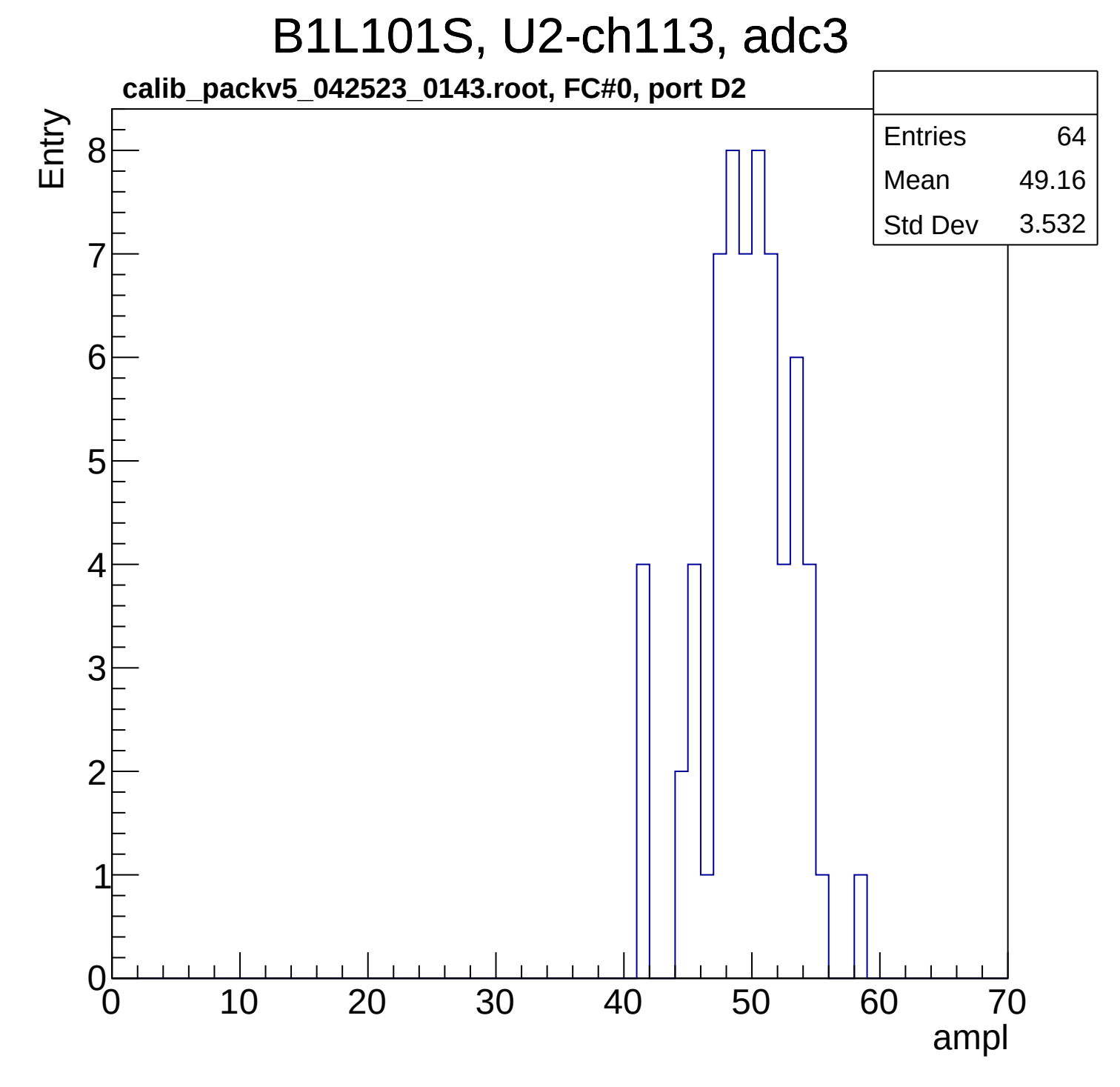

B1L101S, U2-ch112, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 23
Mean 58.17
Std Dev 12.55
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

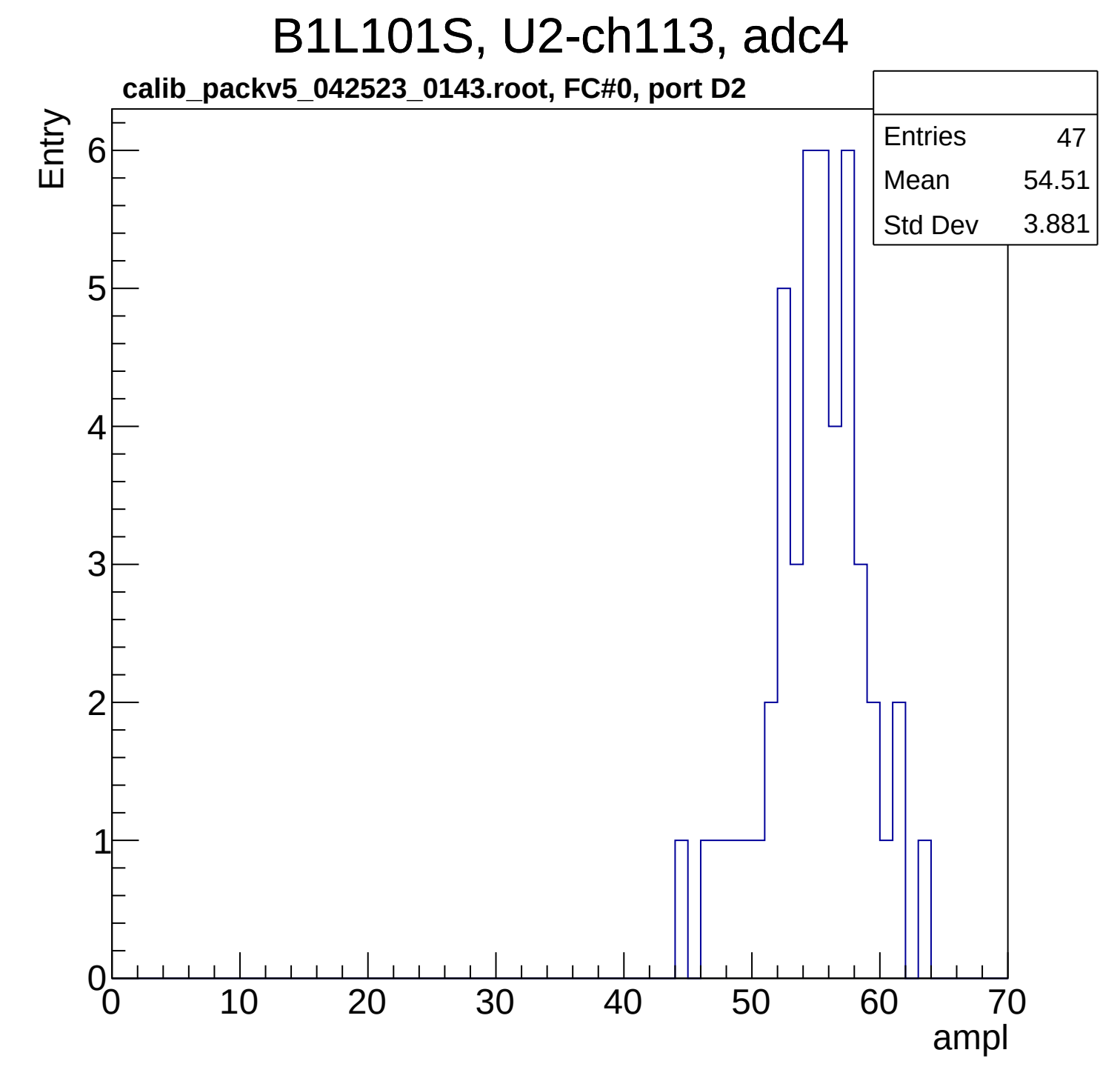

B1L101S, U2-ch112, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 27
Std Dev 26.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

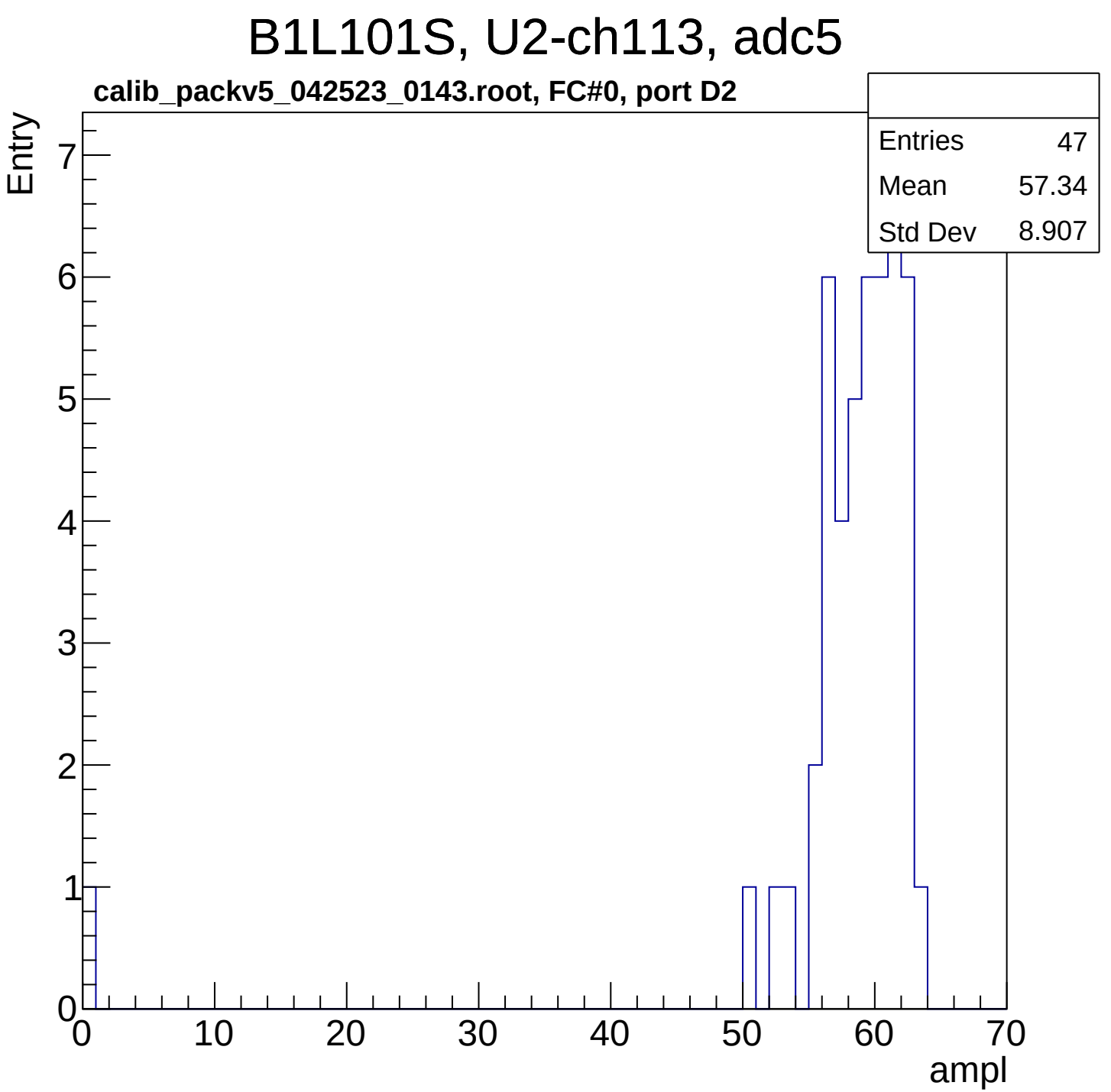

B1L101S, U2-ch113, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 27.18
Std Dev 5.056
Gaus mean : 28.2073
Gaus Width: 4.4413
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

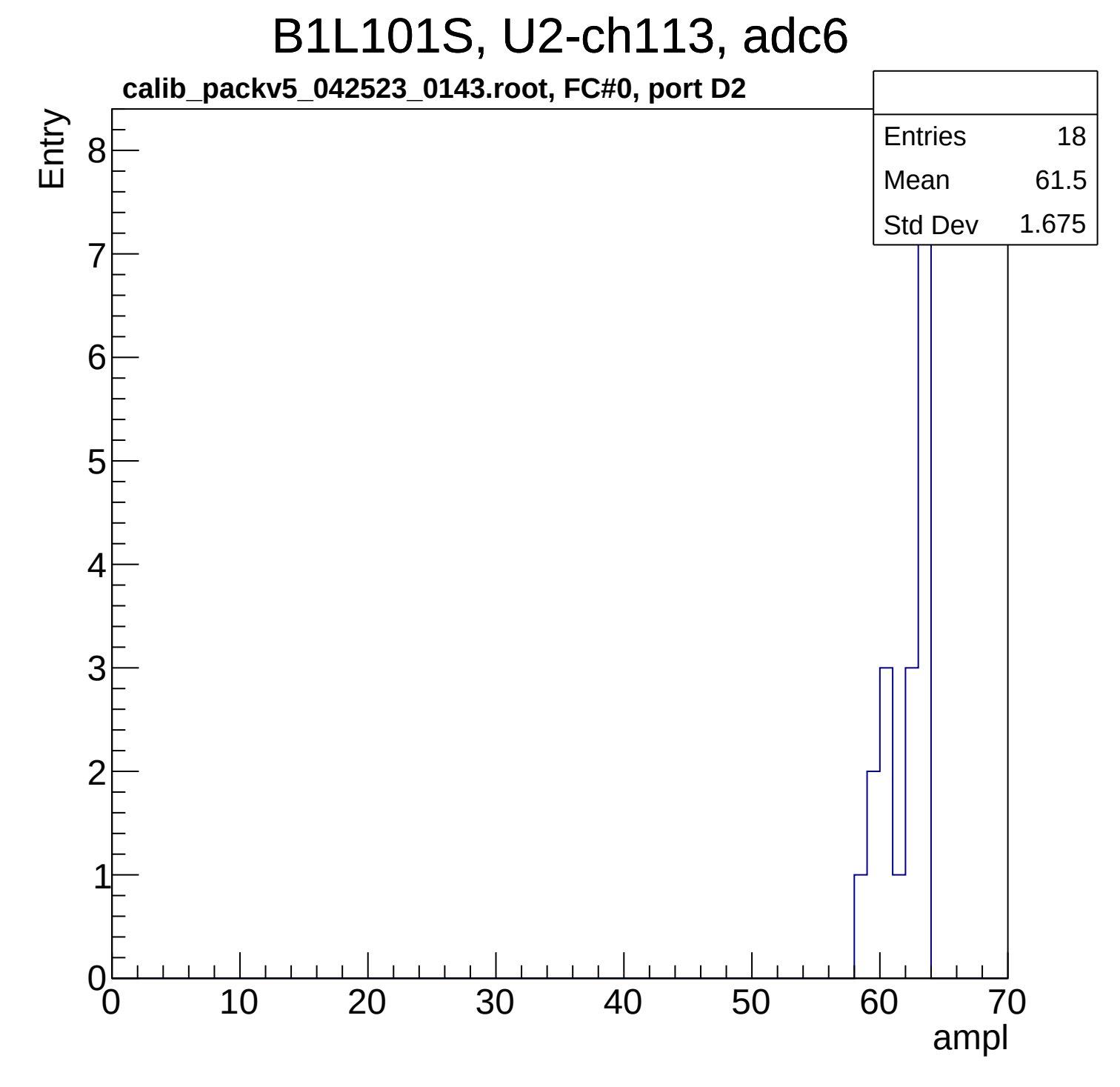

B1L101S, U2-ch113, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 88
Mean 34.61
Std Dev 4.165
Gaus mean : 34.9701
Gaus Width: 4.3953
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

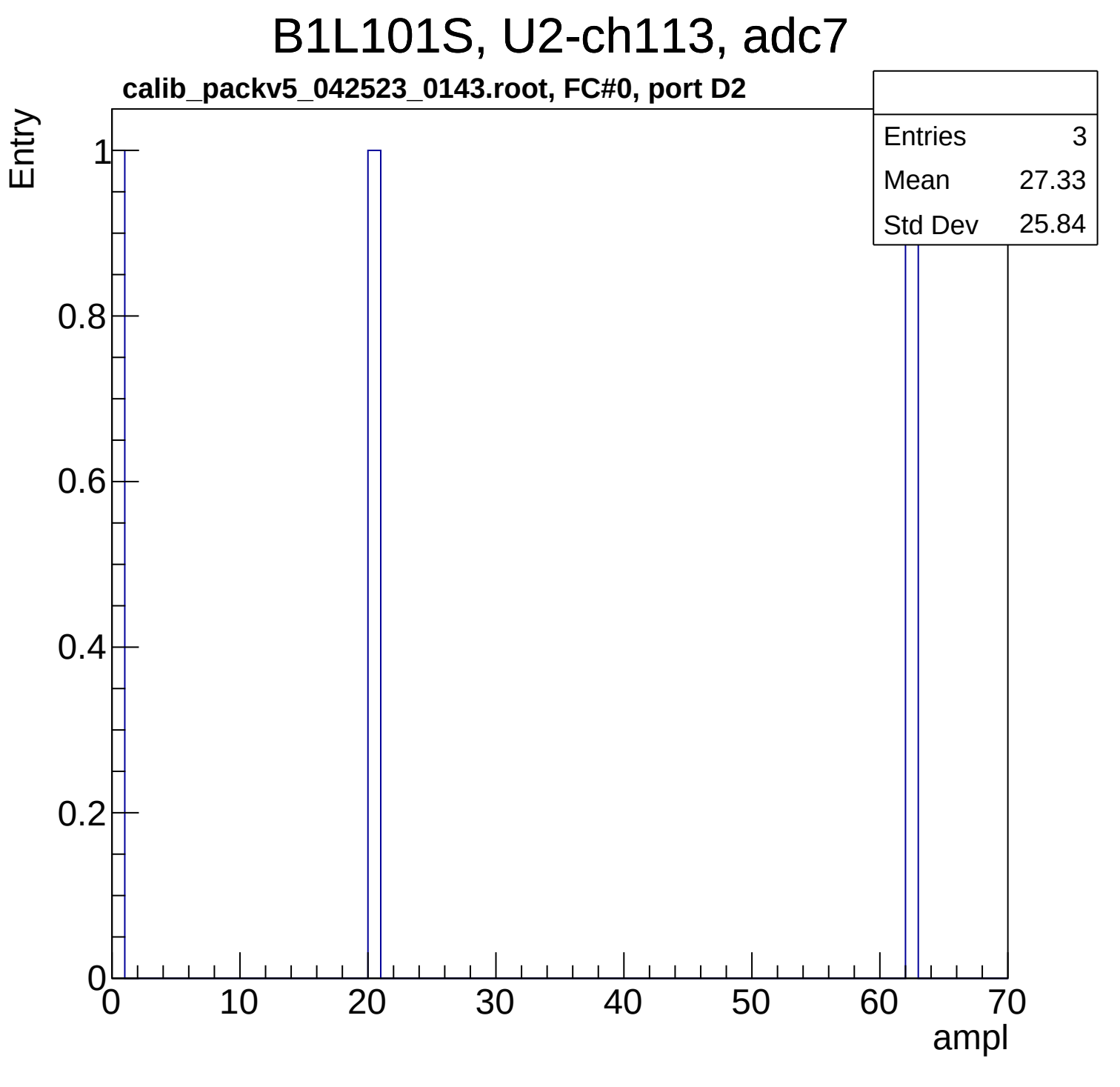

B1L101S, U2-ch113, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 42.56
Std Dev 3.747
Gaus mean : 42.7678
Gaus Width: 3.6670
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

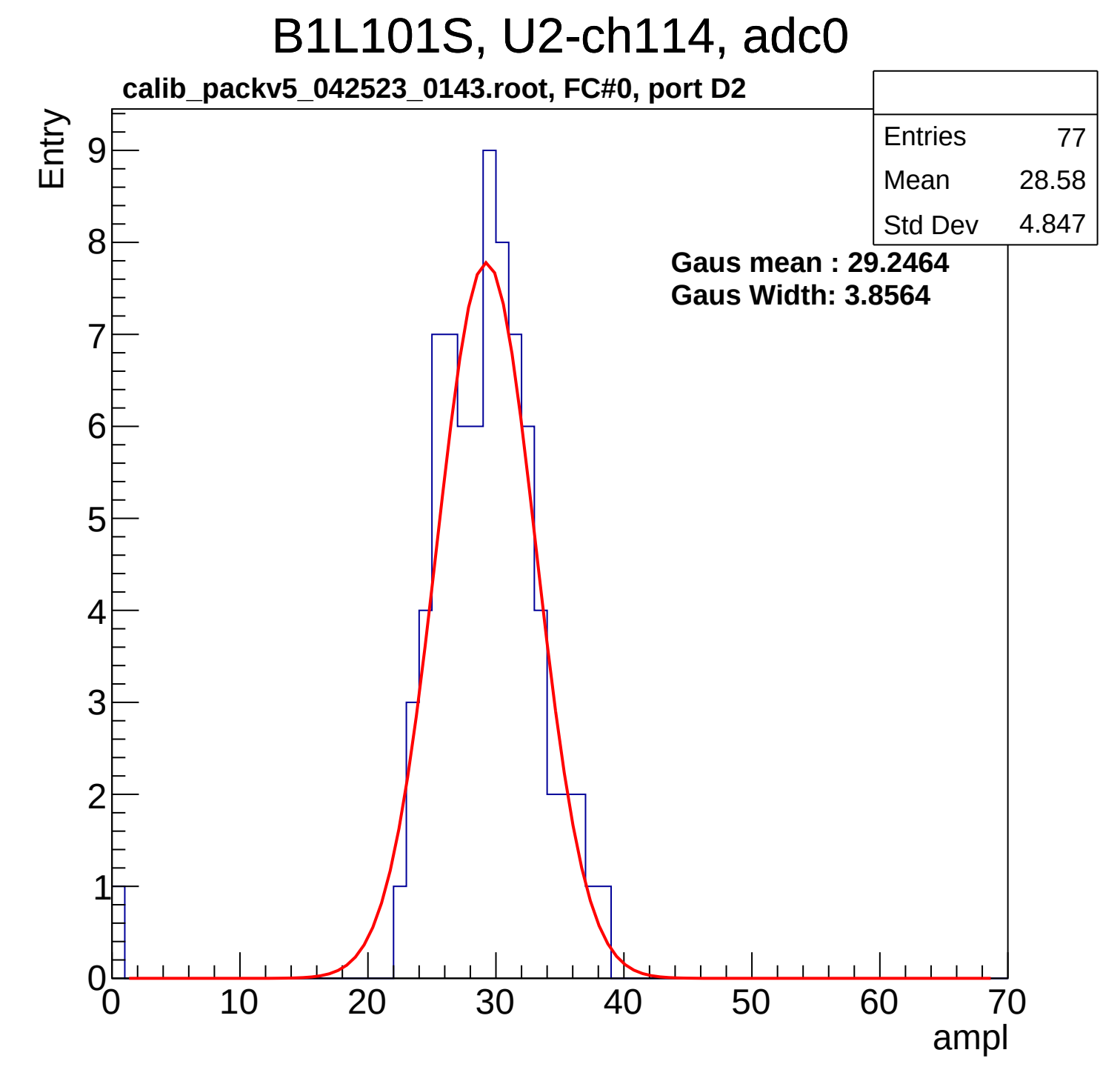

B1L101S, U2-ch113, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 49.16
Std Dev 3.532
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

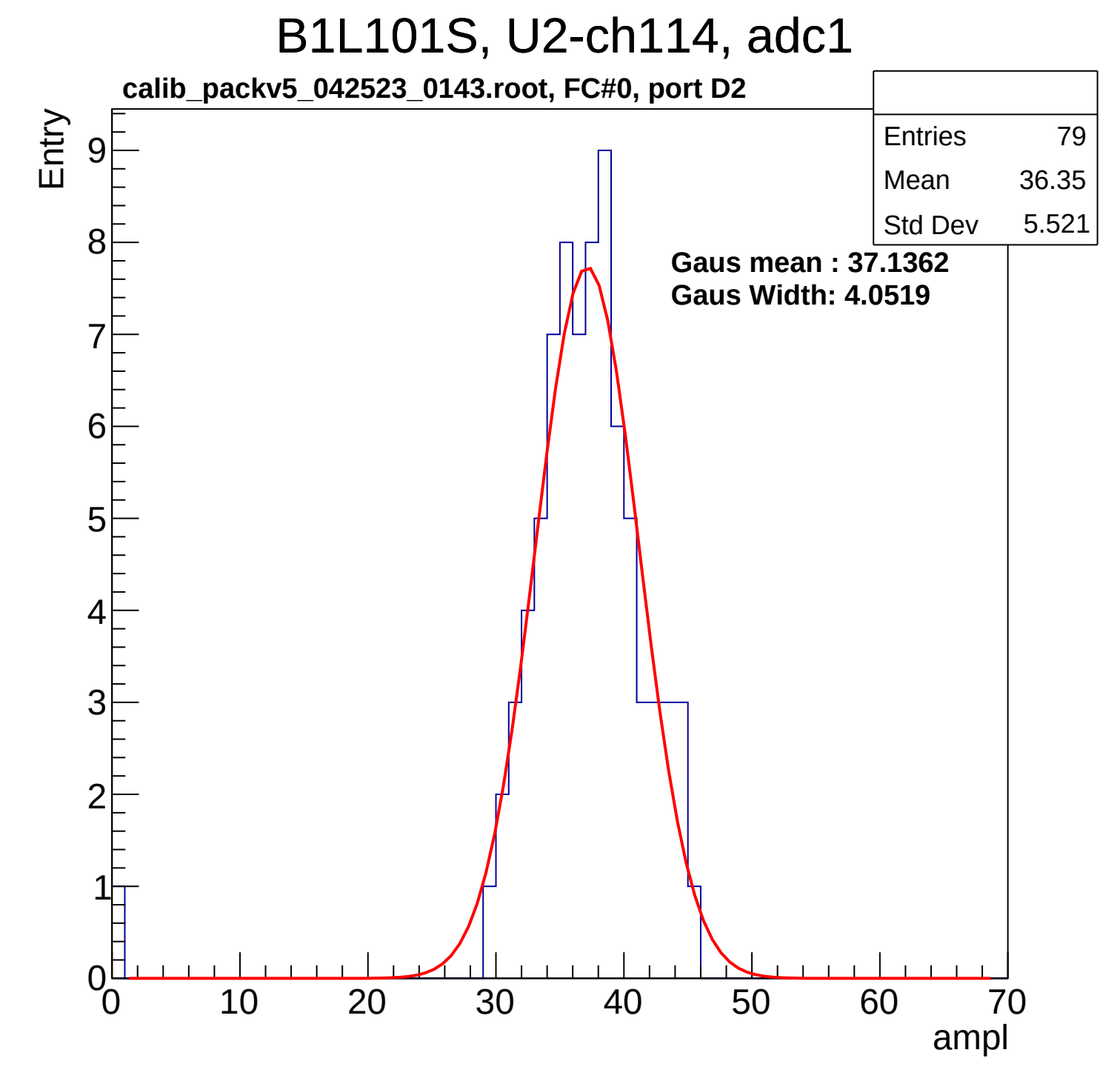

B1L101S, U2-ch113, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 54.51
Std Dev 3.881
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

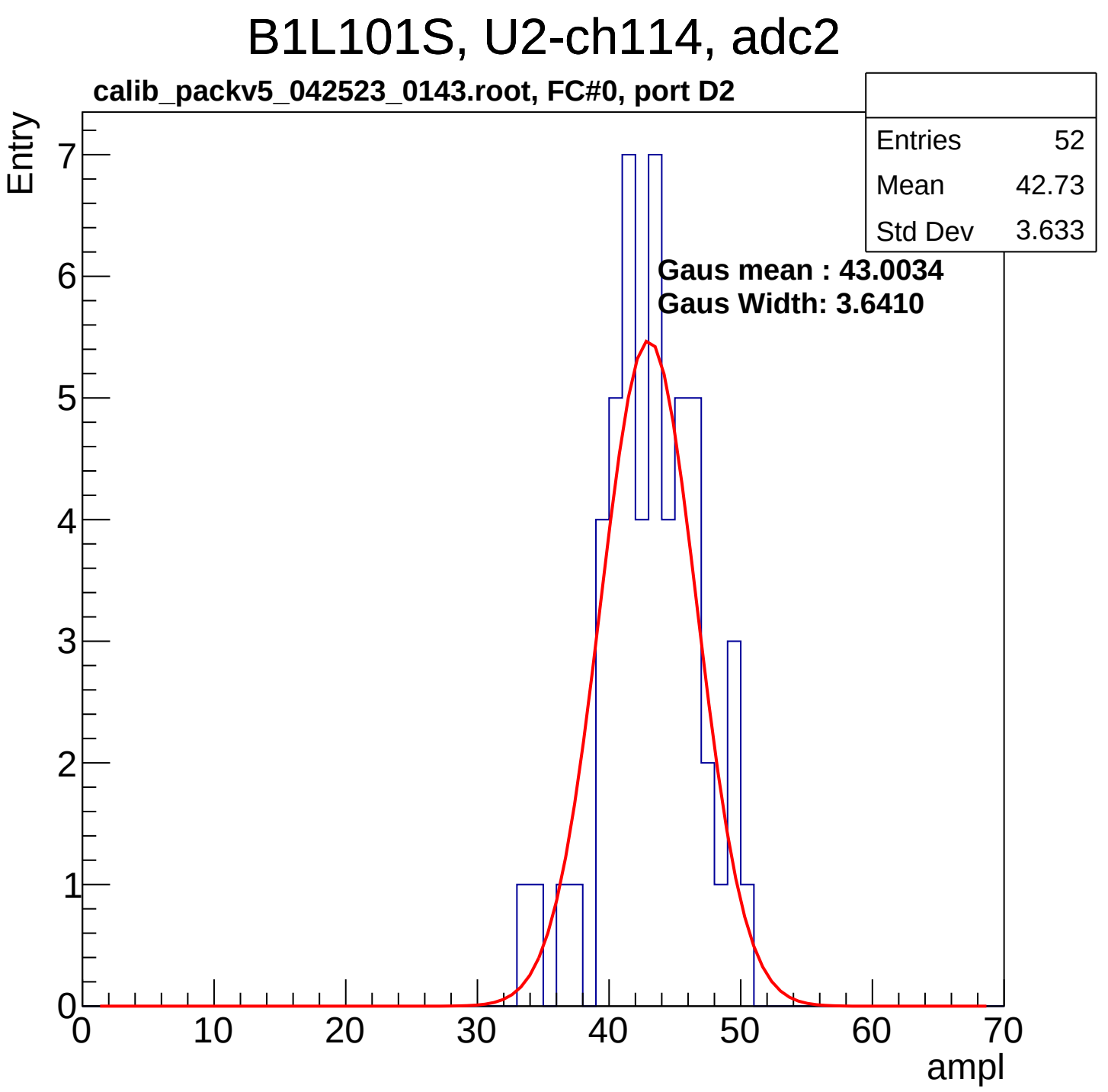

B1L101S, U2-ch113, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 57.34
Std Dev 8.907
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

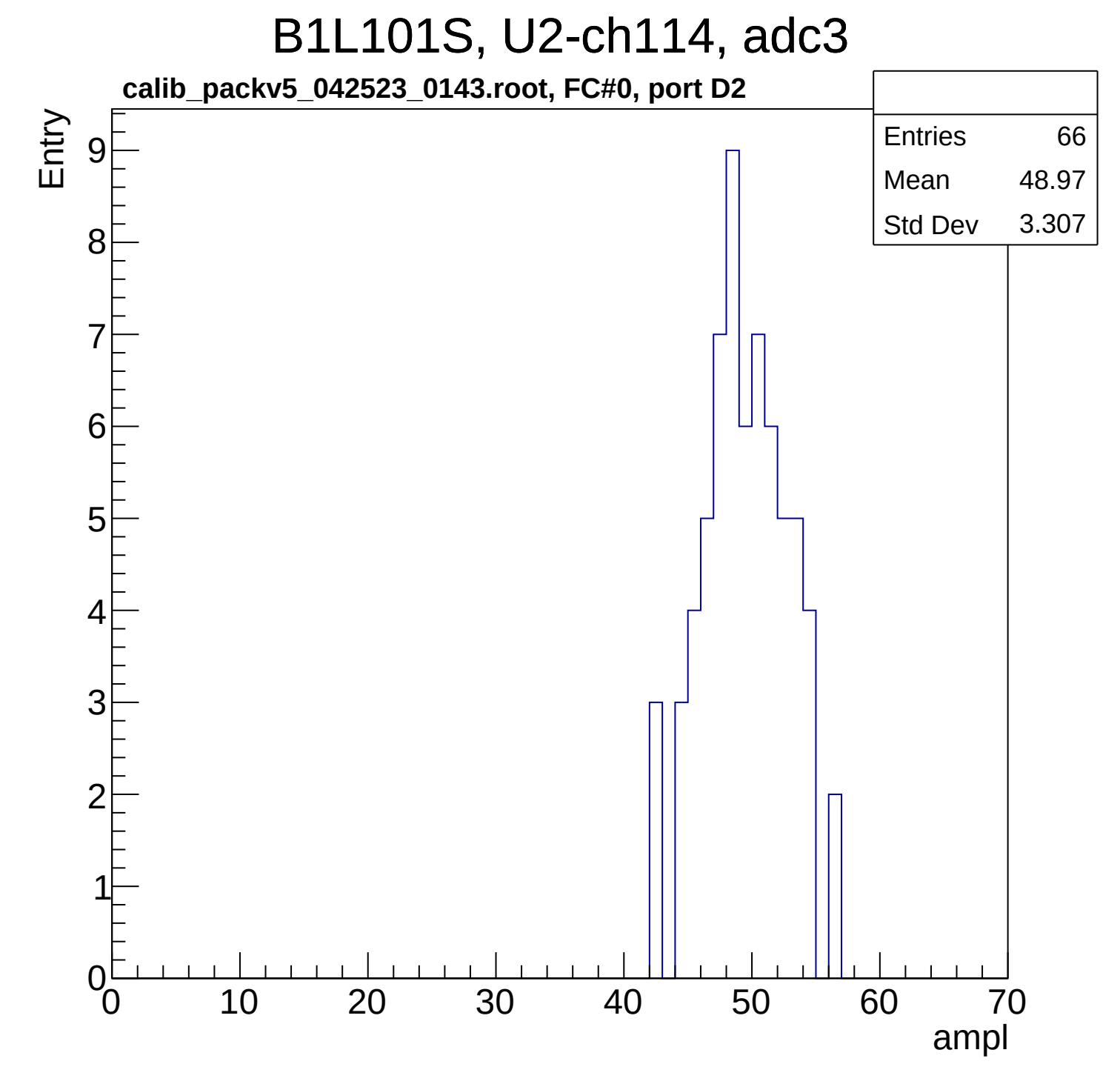

B1L101S, U2-ch113, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 18
Mean 61.5
Std Dev 1.675
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

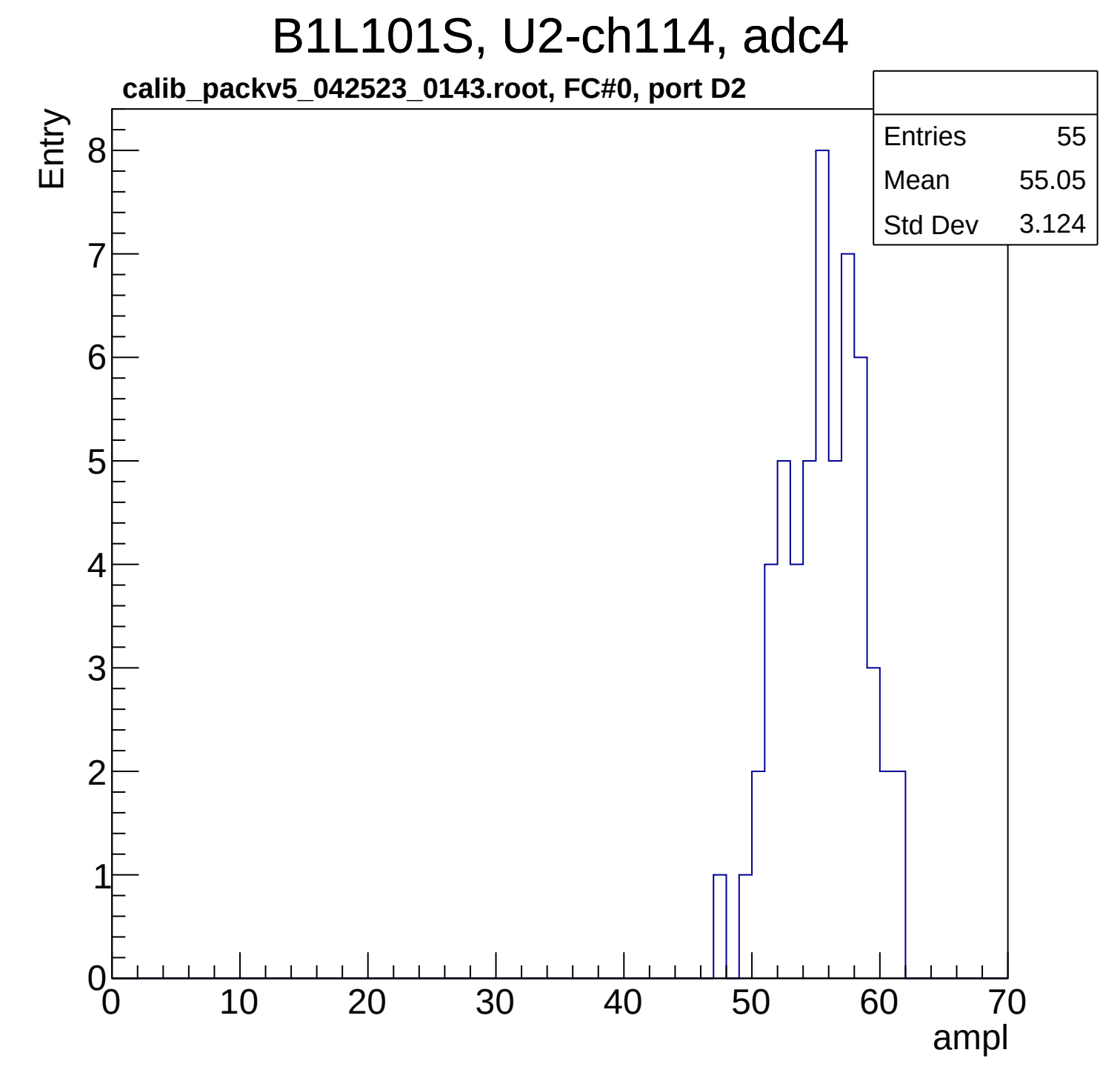

B1L101S, U2-ch113, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 27.33
Std Dev 25.84
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

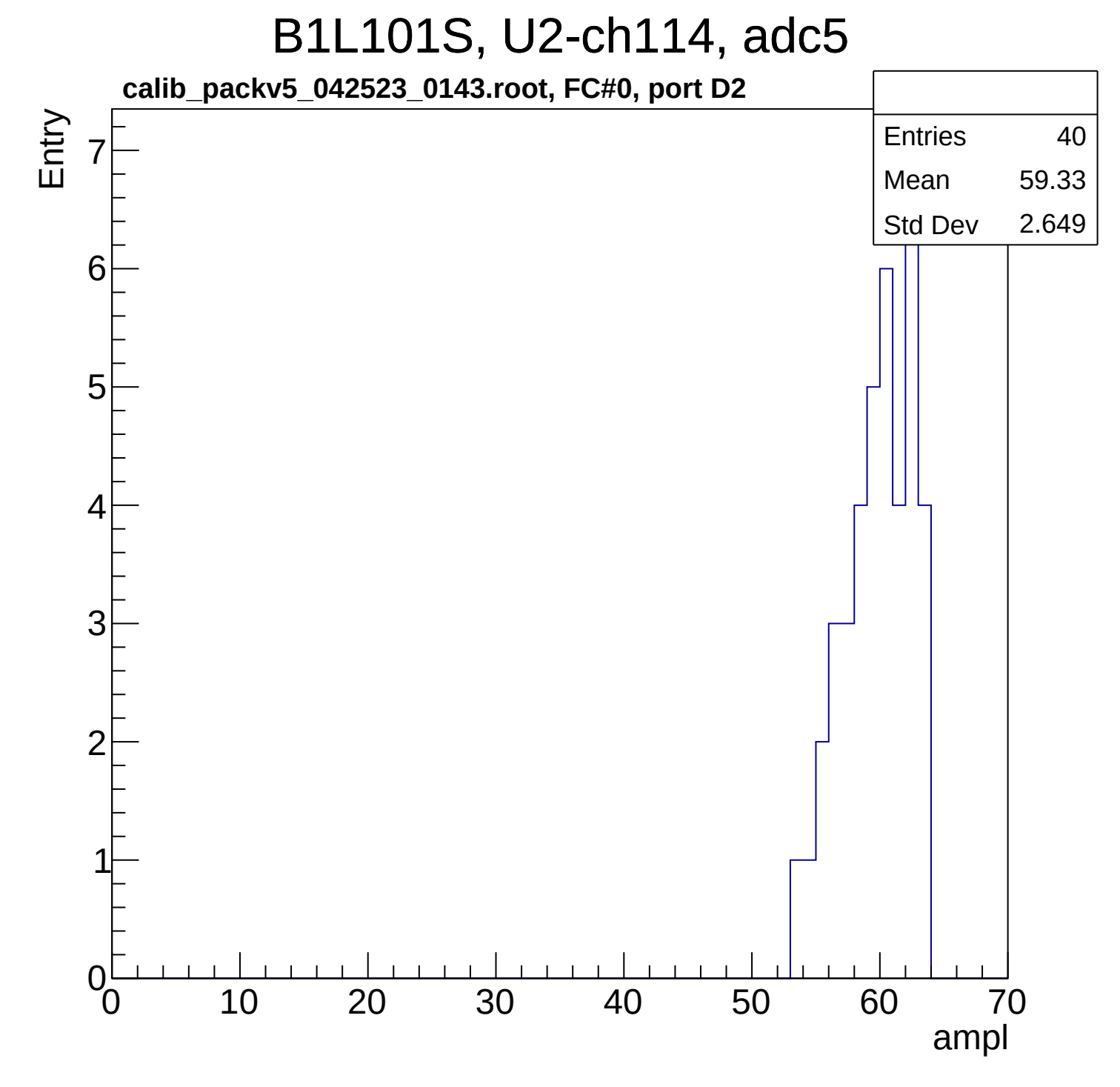

B1L101S, U2-ch114, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 28.58
Std Dev 4.847
Gaus mean : 29.2464
Gaus Width: 3.8564
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

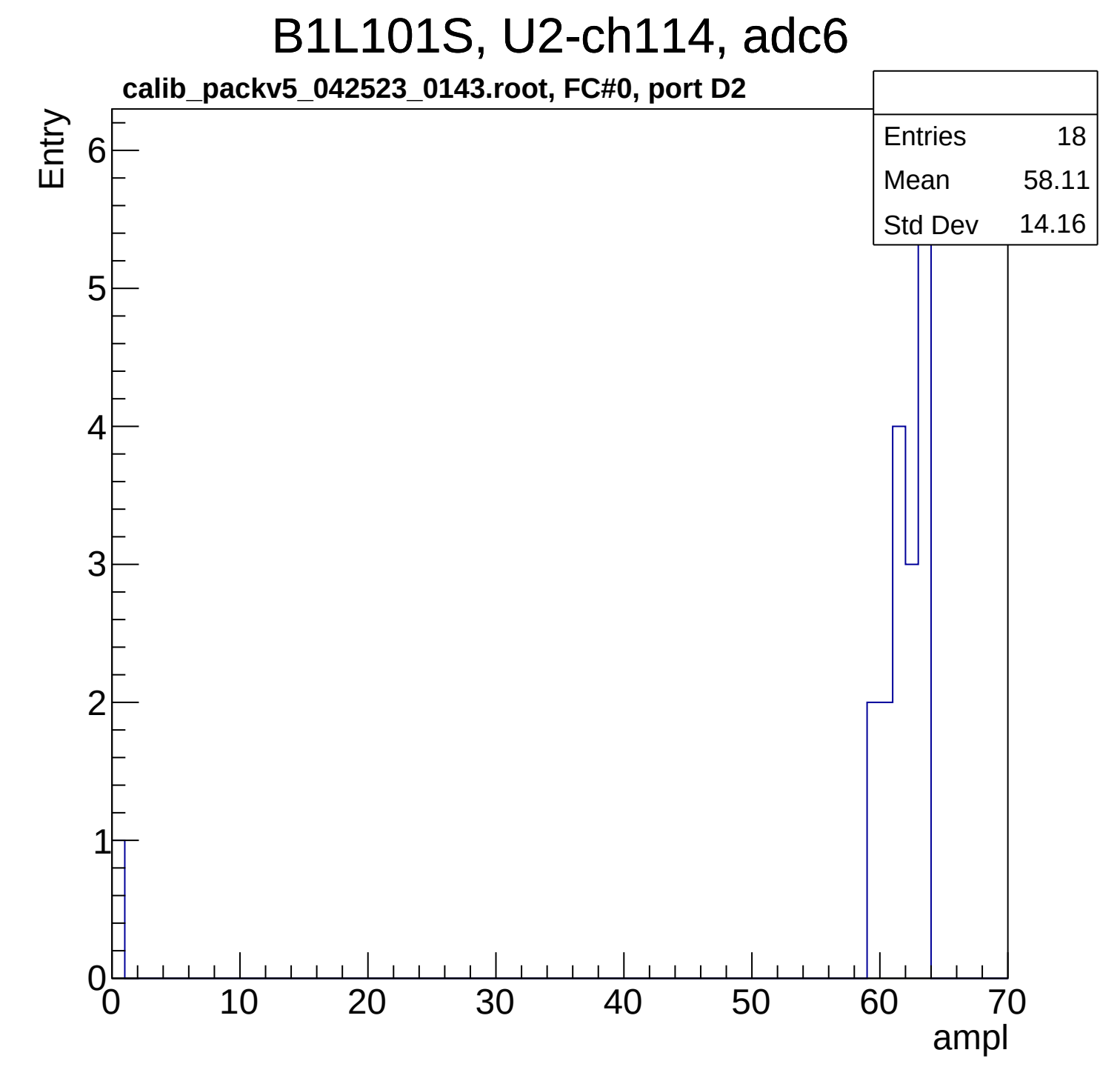

B1L101S, U2-ch114, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 79
Mean 36.35
Std Dev 5.521
Gaus mean : 37.1362
Gaus Width: 4.0519
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

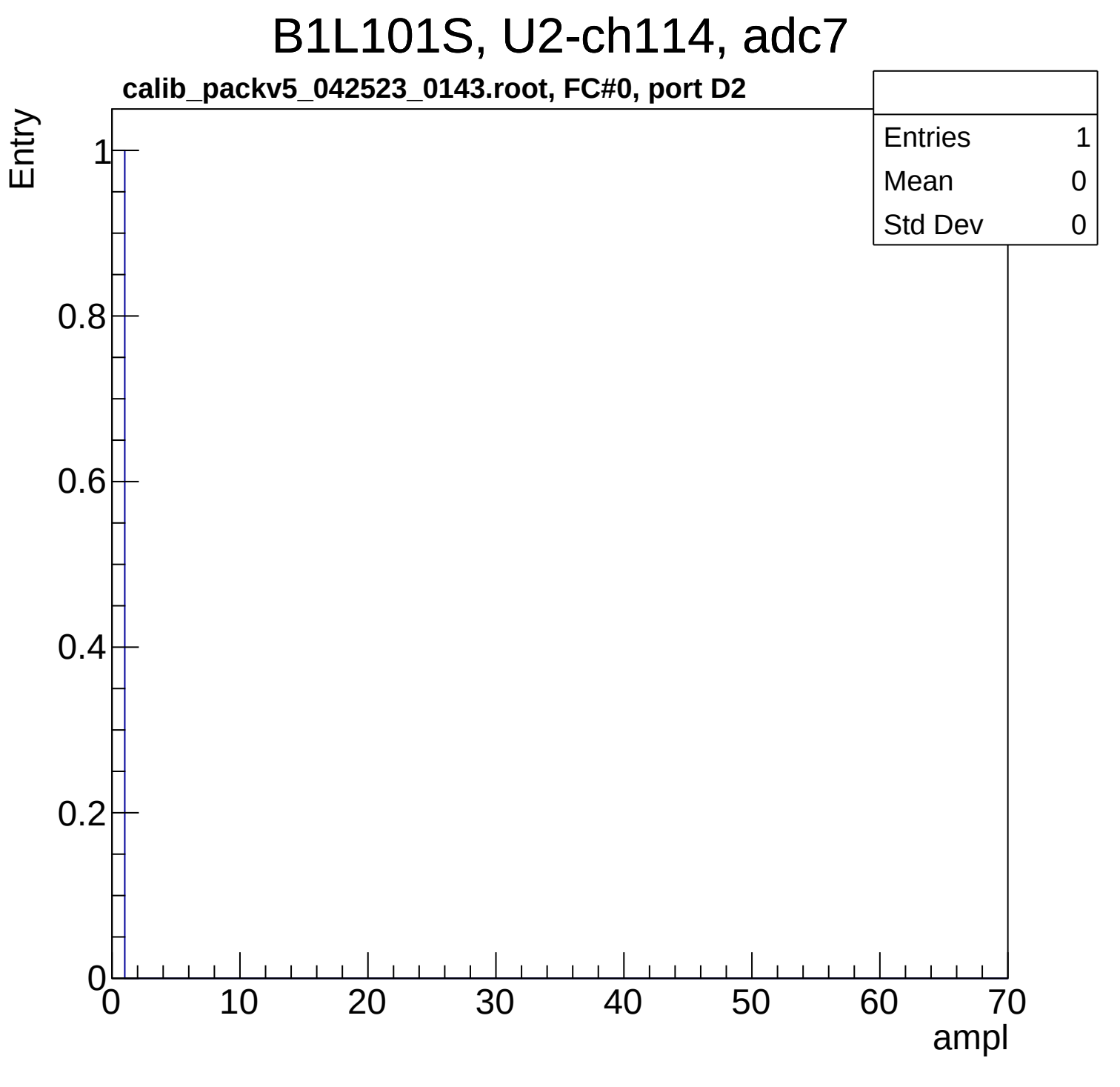

B1L101S, U2-ch114, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 42.73
Std Dev 3.633
Gaus mean : 43.0034
Gaus Width: 3.6410
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

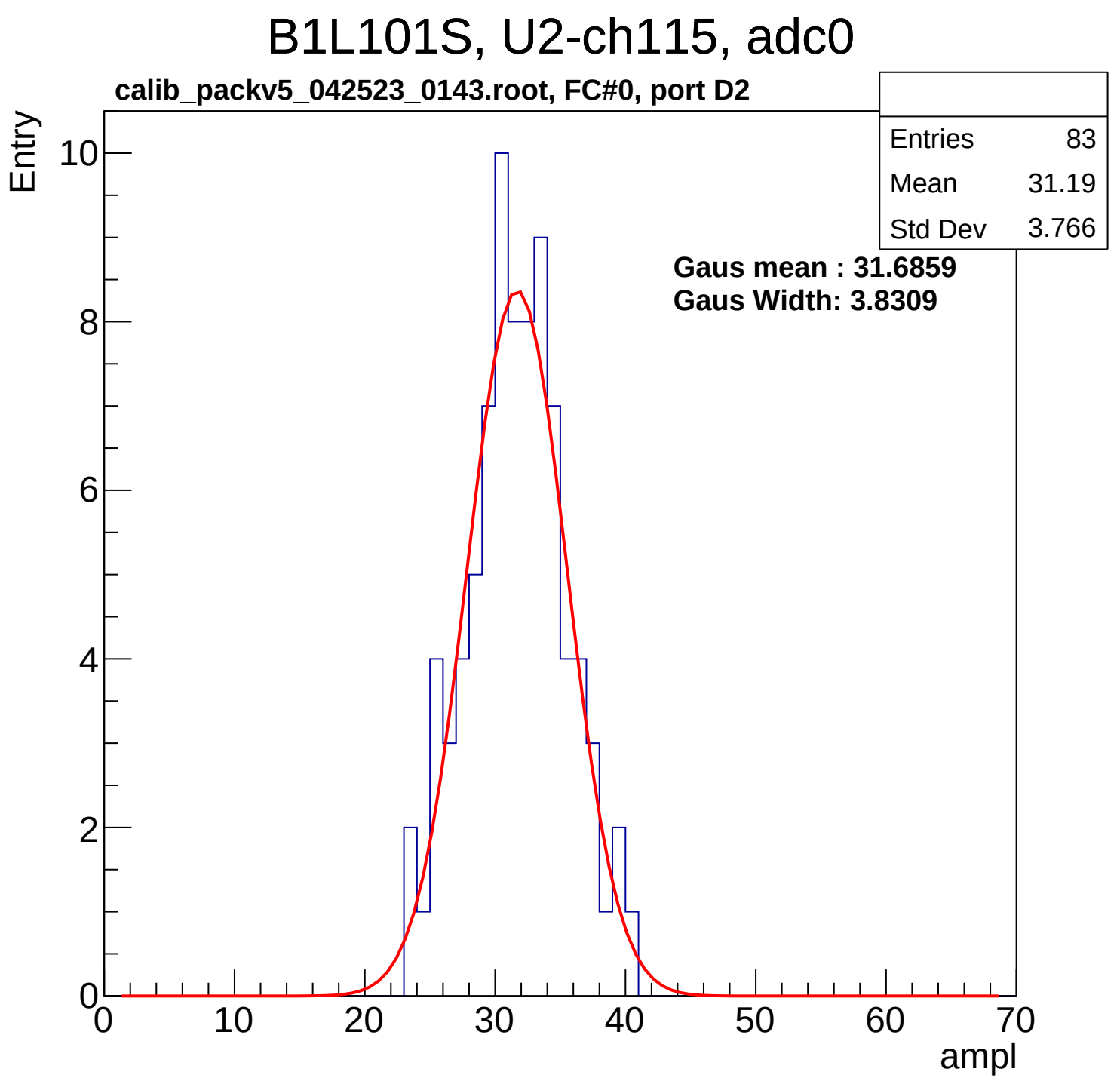

B1L101S, U2-ch114, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 48.97
Std Dev 3.307
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

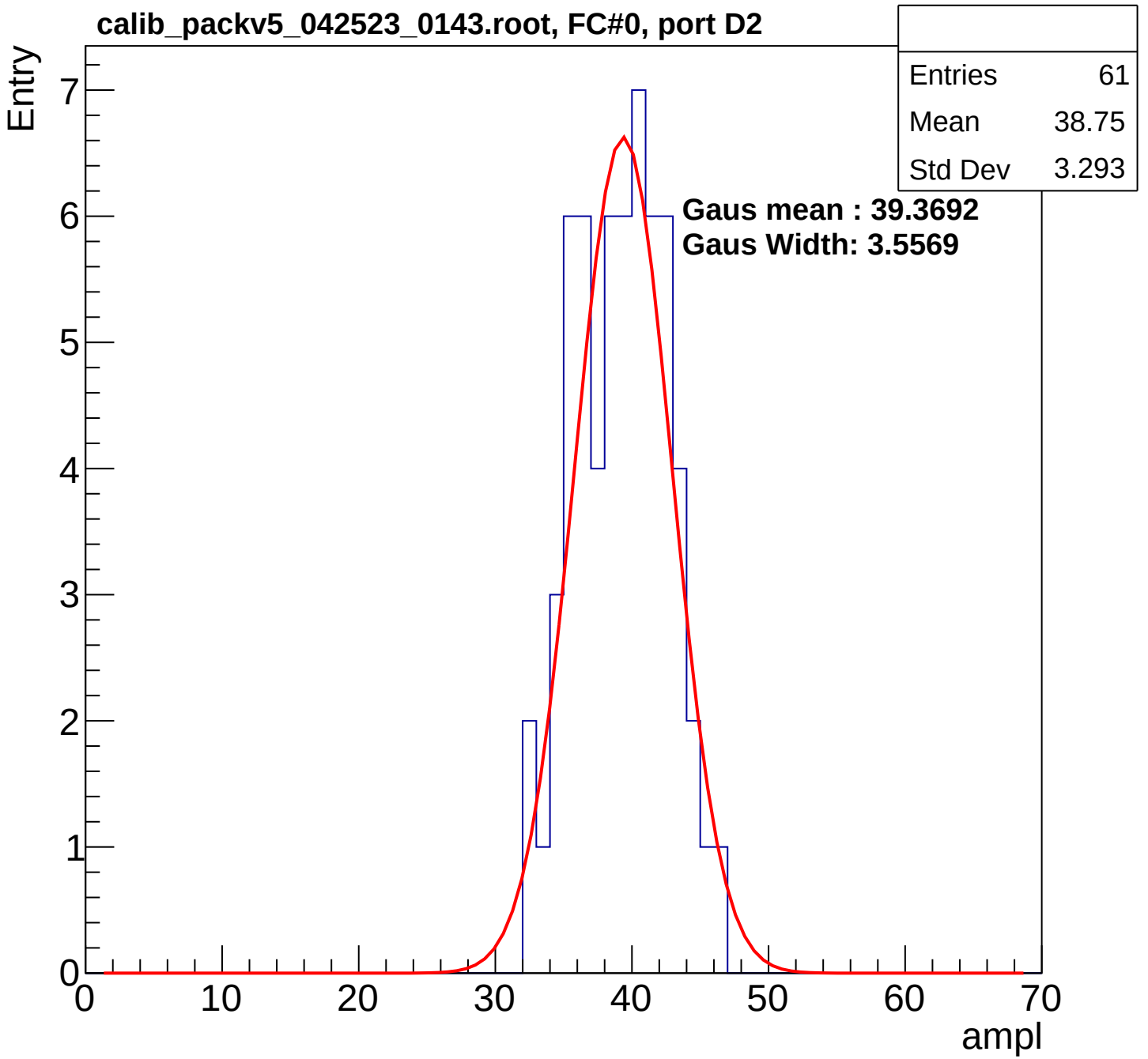

B1L101S, U2-ch114, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 55
Mean 55.05
Std Dev 3.124
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

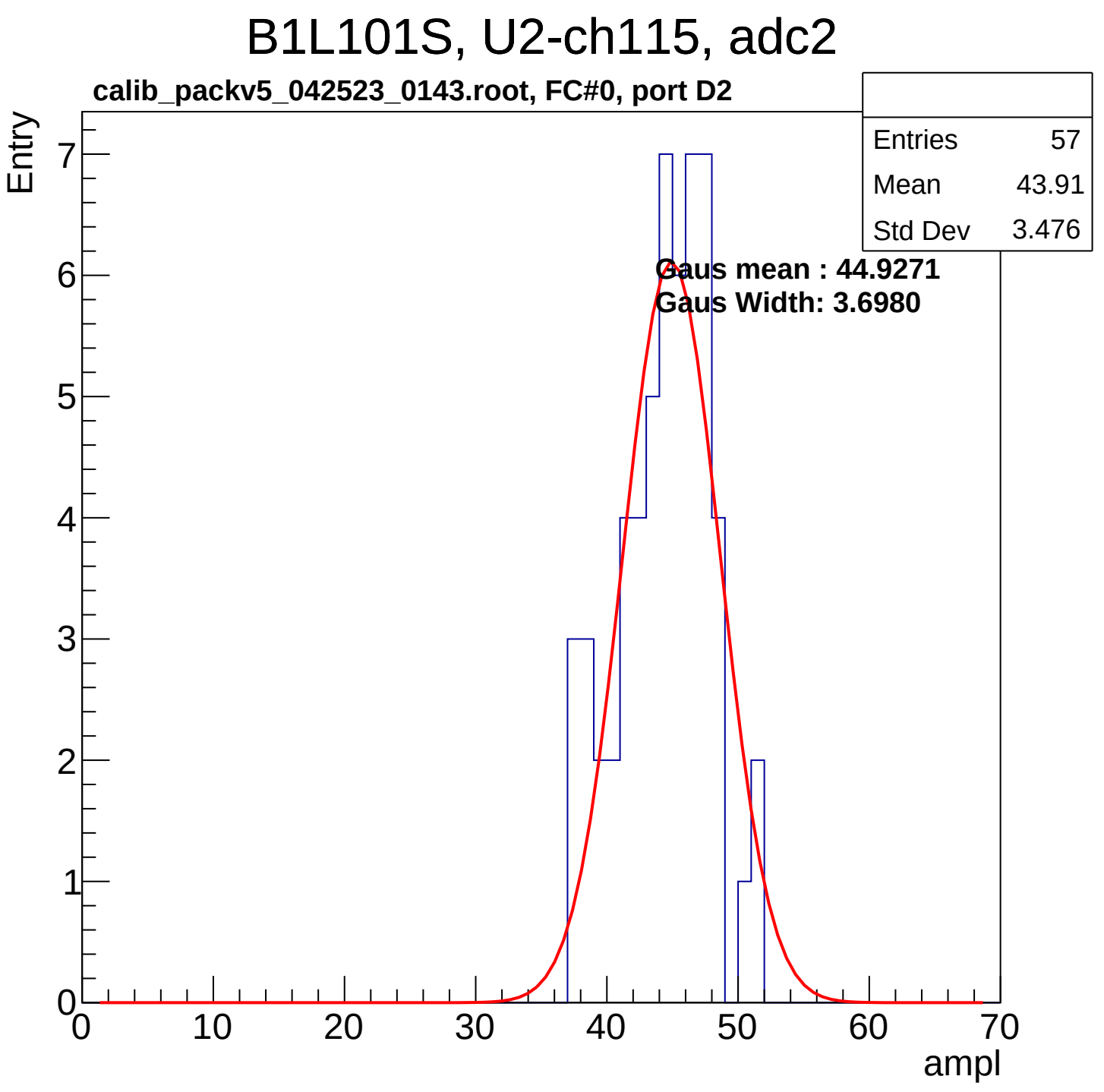

B1L101S, U2-ch114, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 40
Mean 59.33
Std Dev 2.649
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

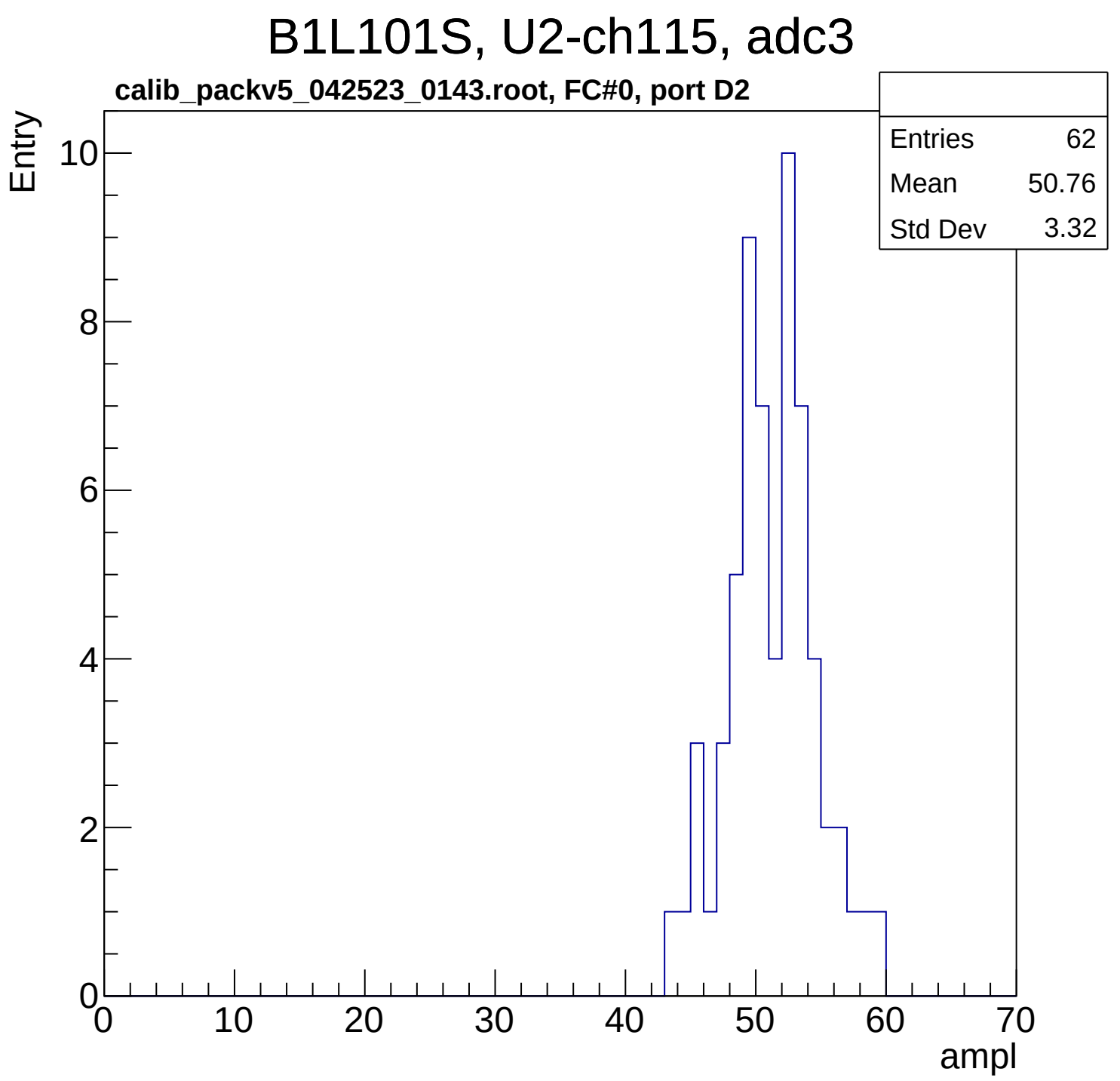

B1L101S, U2-ch114, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 18
Mean 58.11
Std Dev 14.16
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

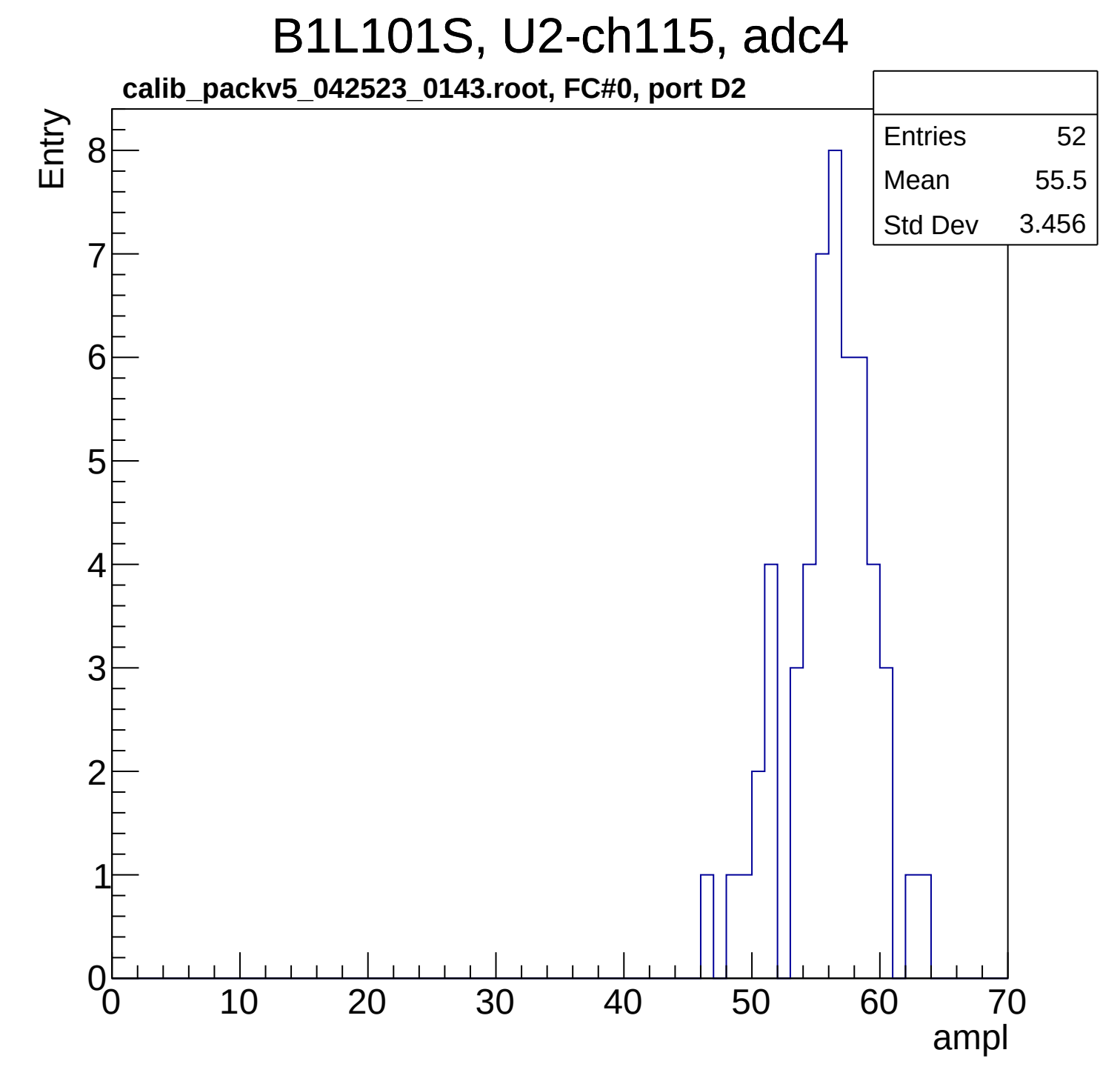

B1L101S, U2-ch114, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

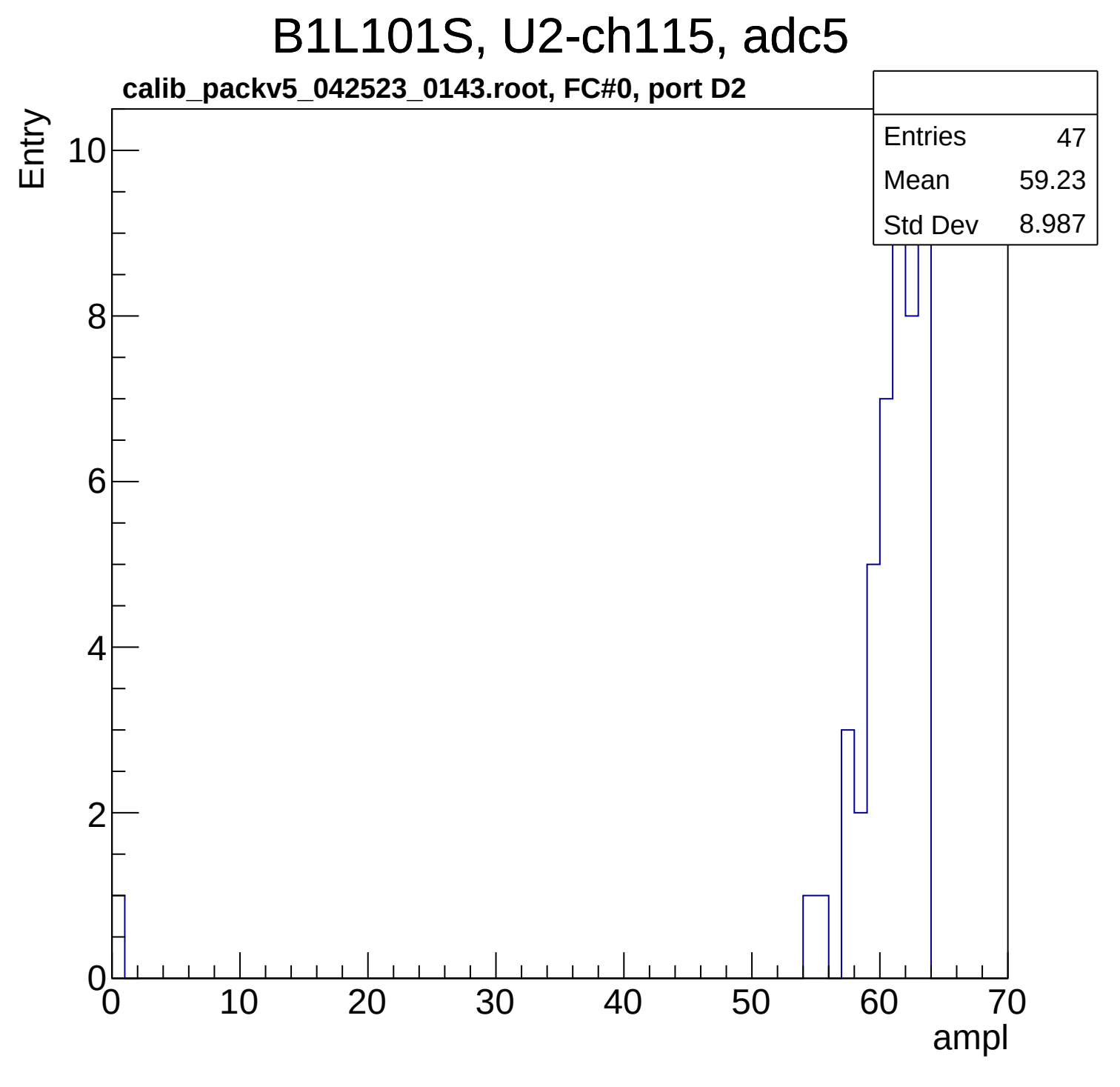

B1L101S, U2-ch115, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 83
Mean 31.19
Std Dev 3.766
Gaus mean : 31.6859
Gaus Width: 3.8309
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

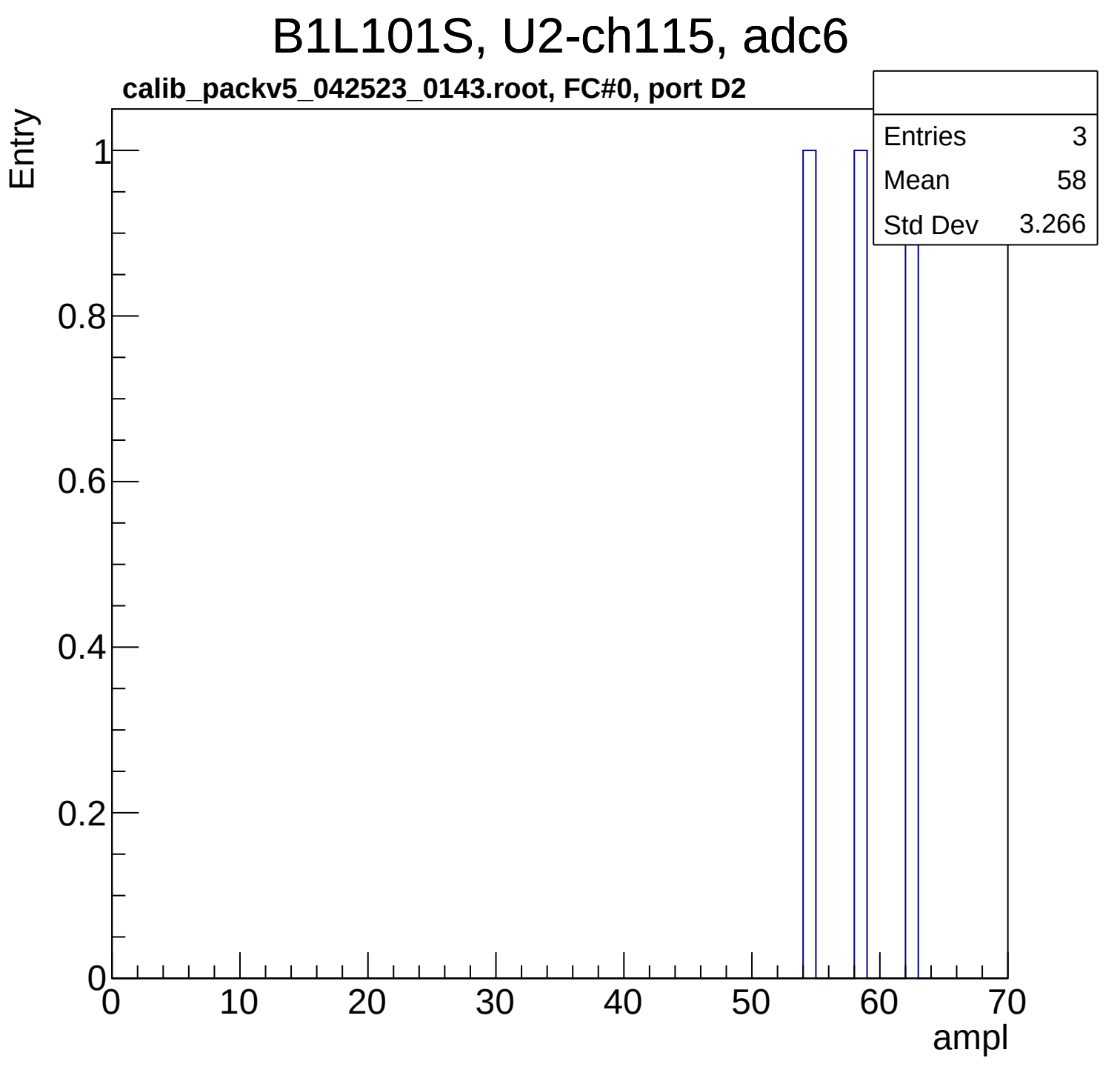

B1L101S, U2-ch115, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 38.75
Std Dev 3.293
Gaus mean : 39.3692
Gaus Width: 3.5569
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

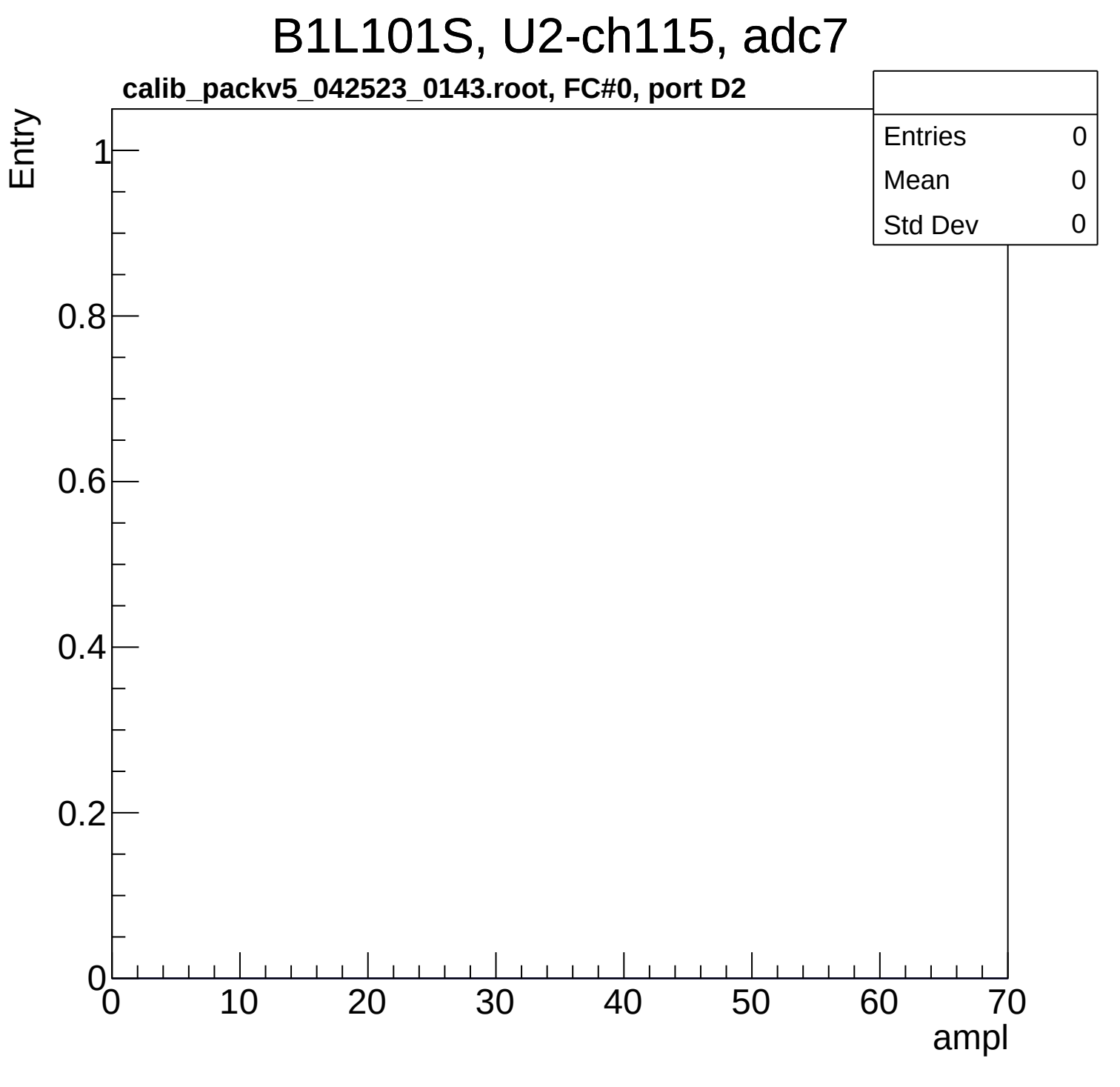

B1L101S, U2-ch115, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 43.91
Std Dev 3.476
Gaus mean : 44.9271
Gaus Width: 3.6980
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

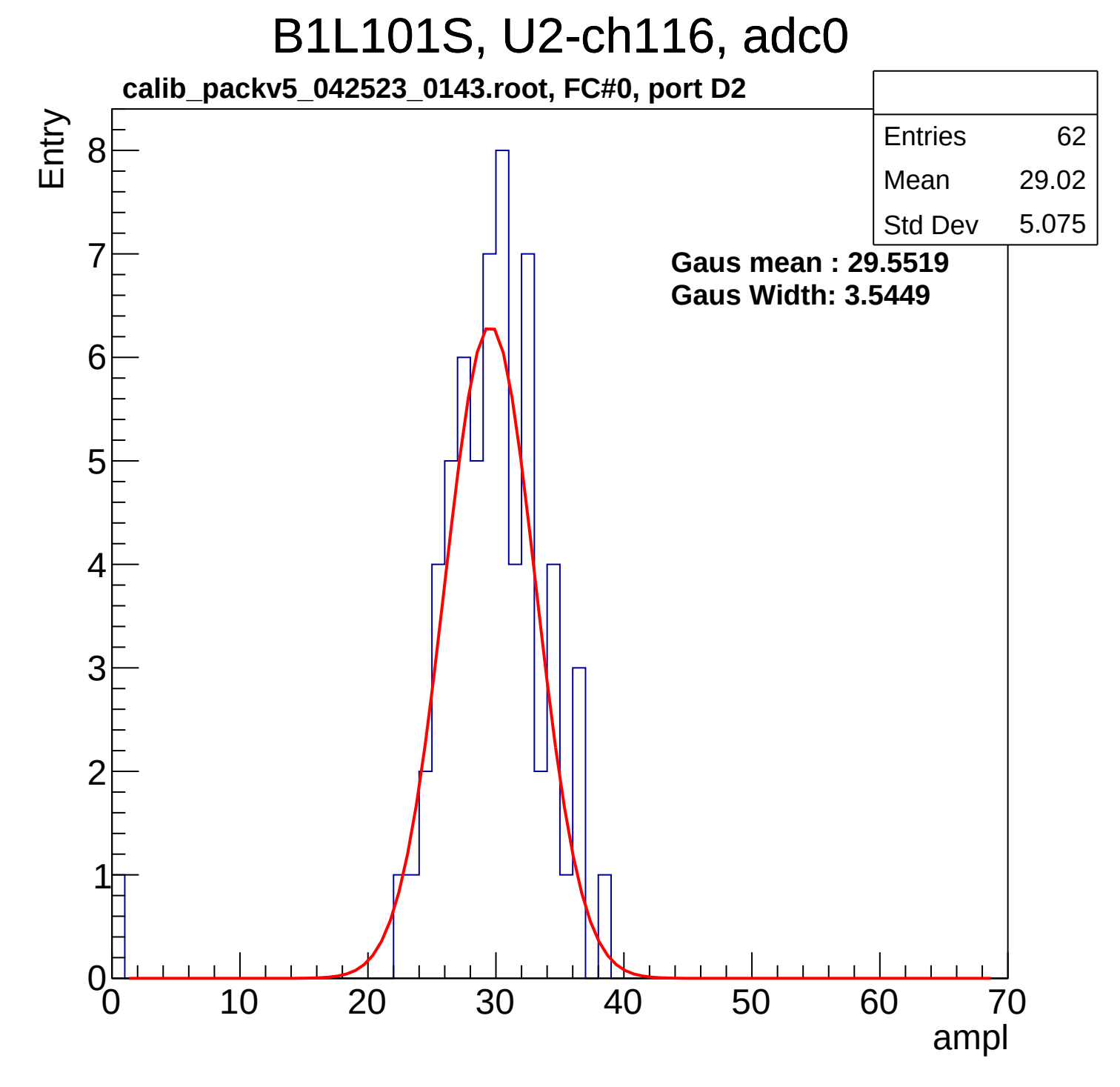

B1L101S, U2-ch115, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 50.76
Std Dev 3.32
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

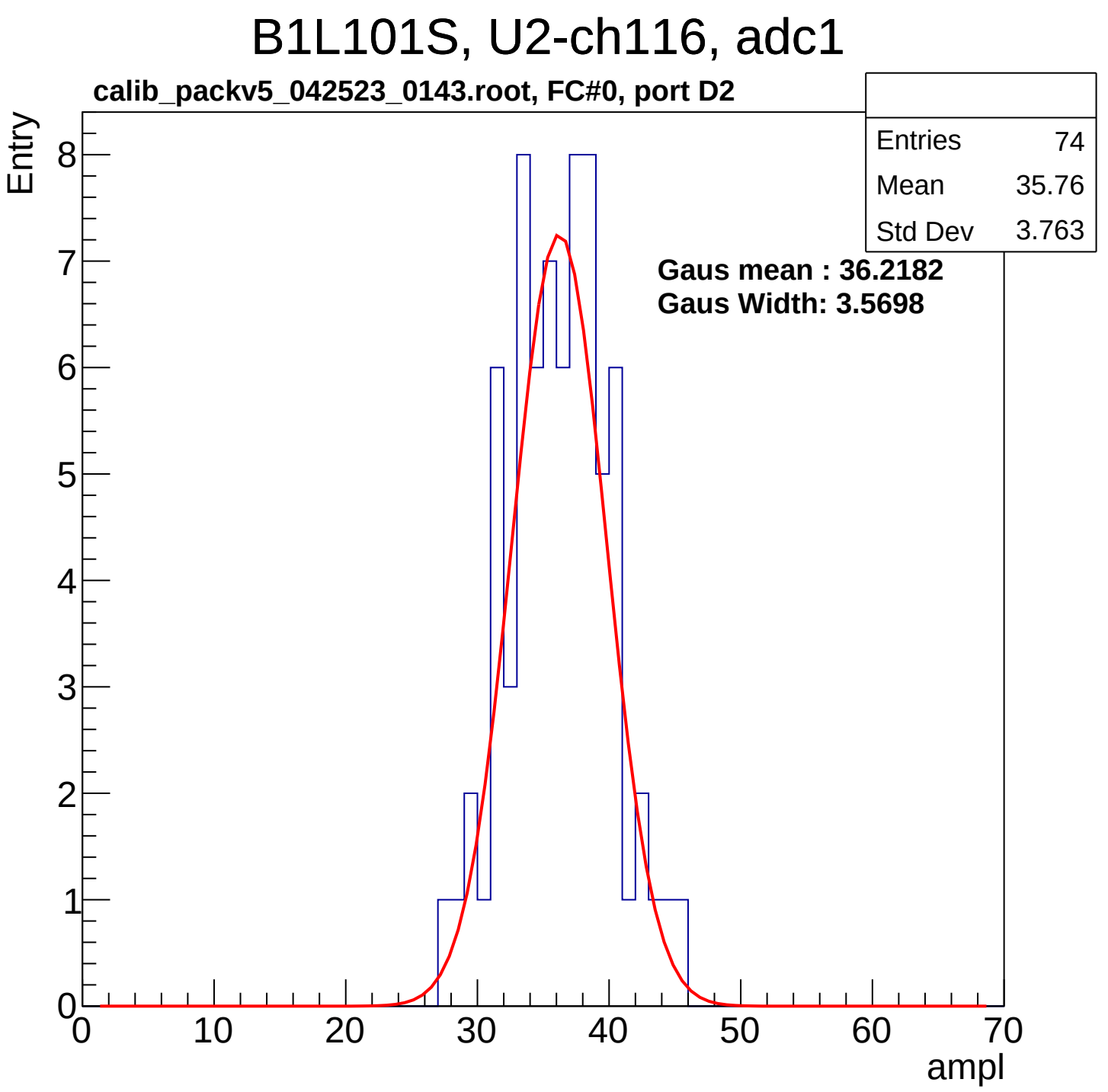

B1L101S, U2-ch115, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 55.5
Std Dev 3.456
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

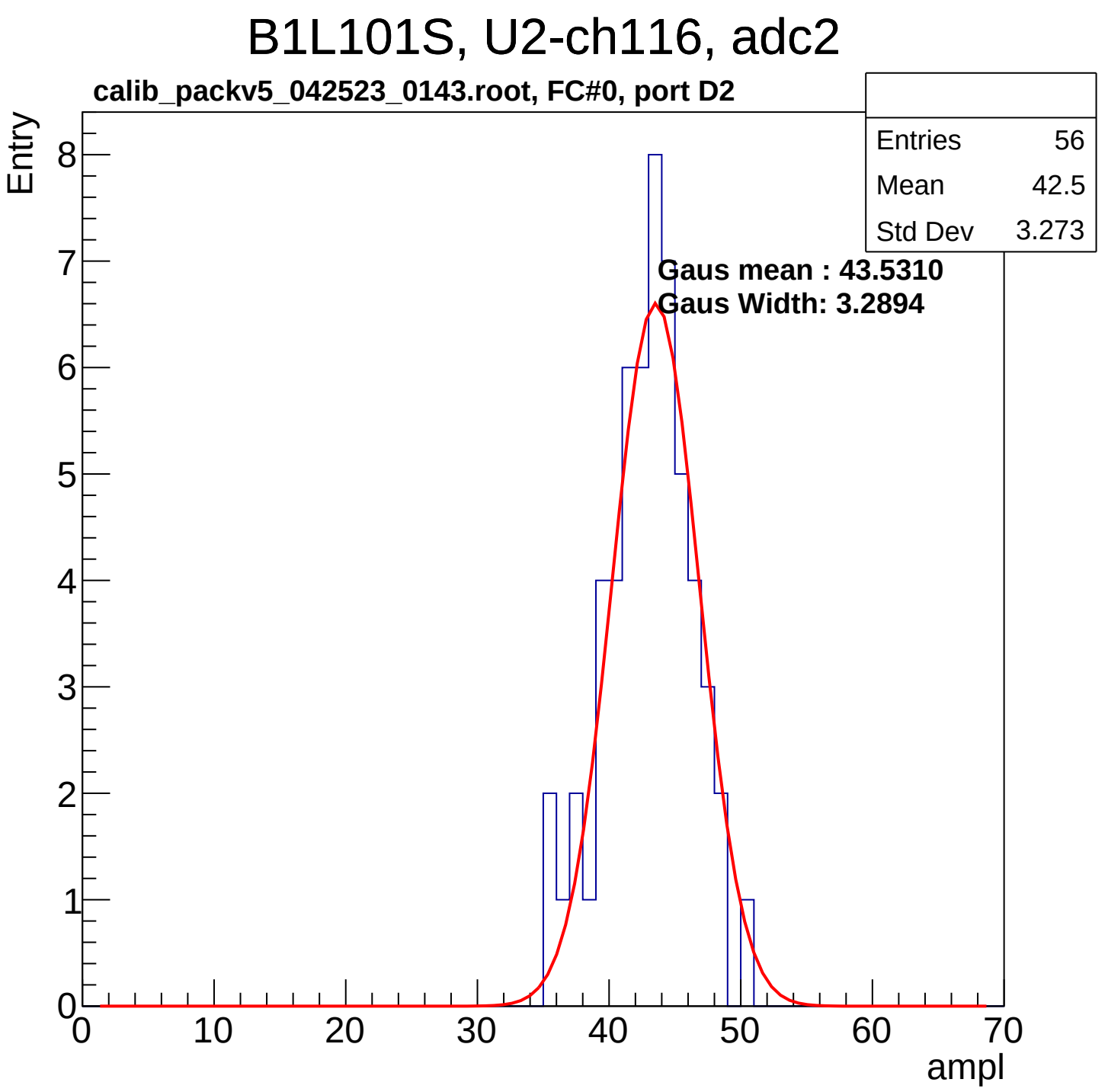

B1L101S, U2-ch115, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 47
Mean 59.23
Std Dev 8.987
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

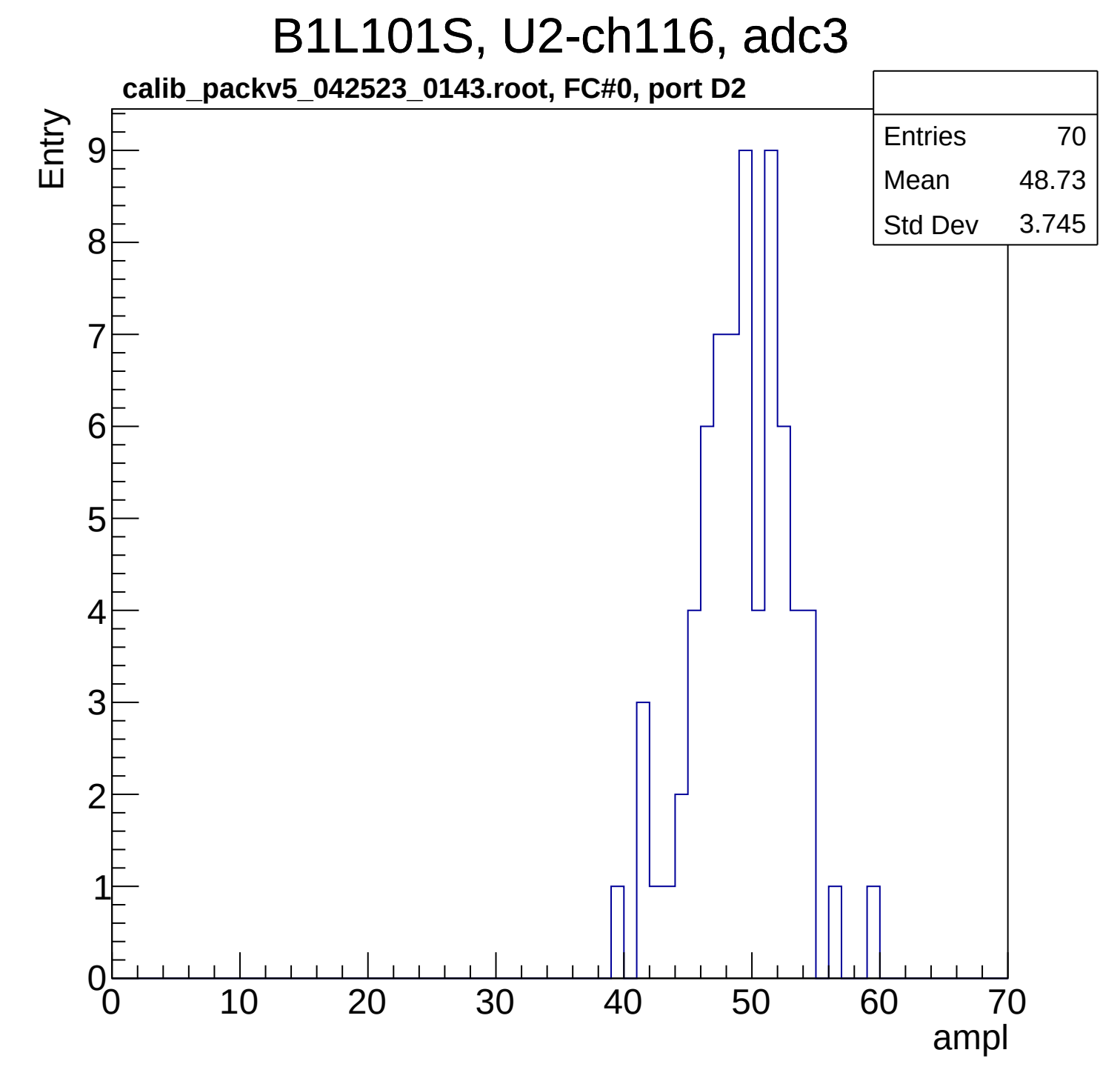

B1L101S, U2-ch115, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 3
Mean 58
Std Dev 3.266
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

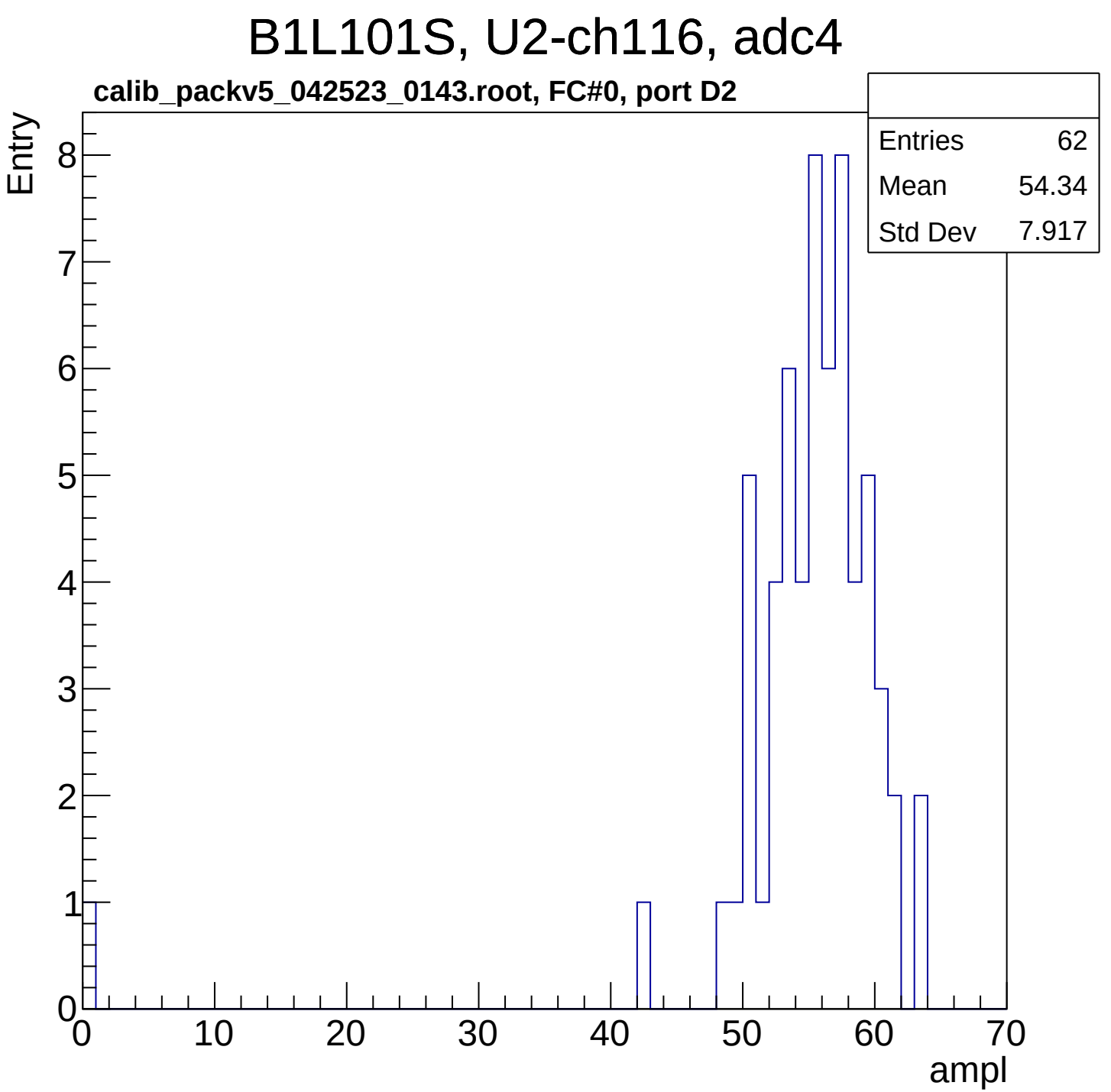

B1L101S, U2-ch115, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

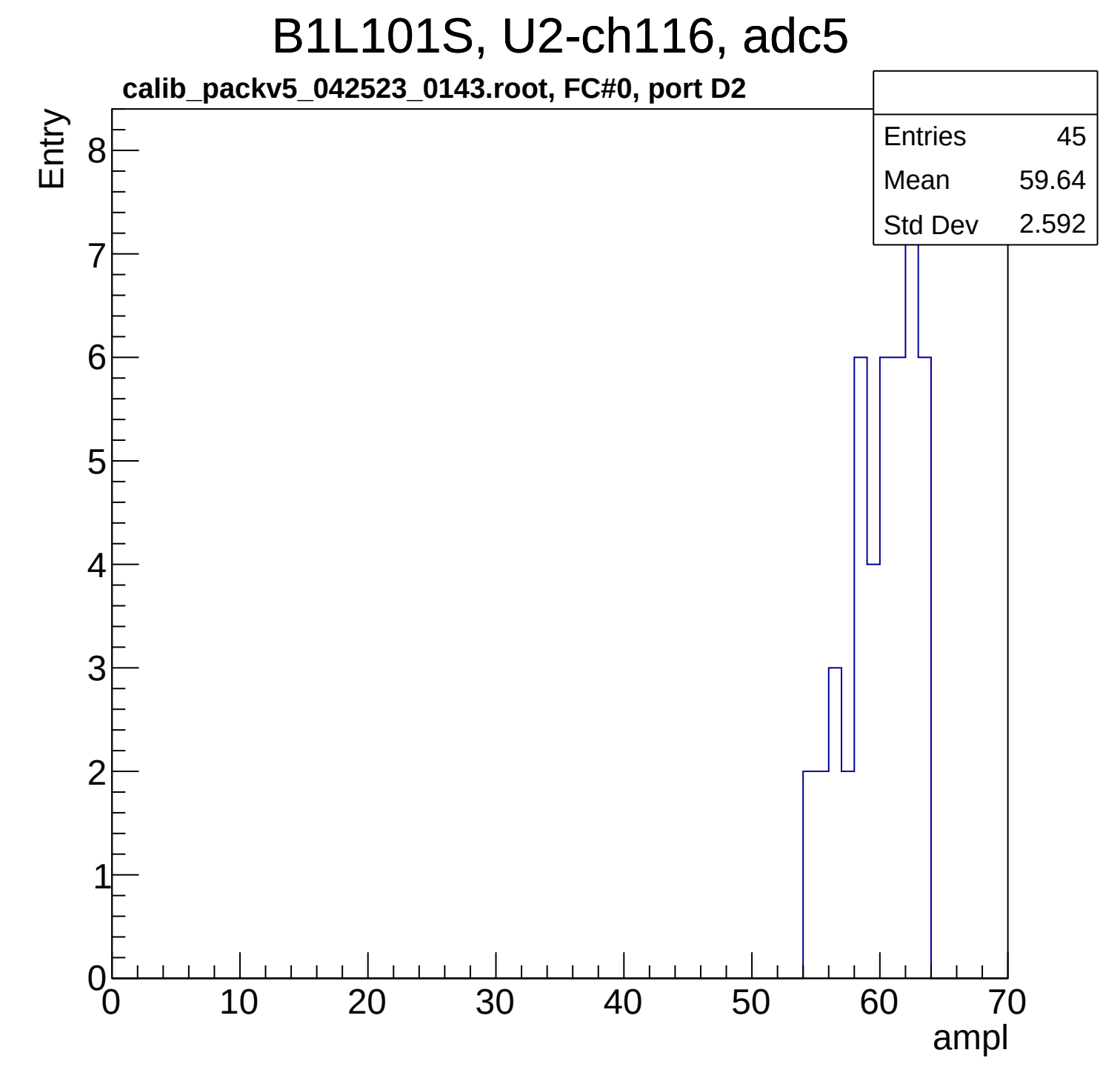

B1L101S, U2-ch116, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 29.02
Std Dev 5.075
Gaus mean : 29.5519
Gaus Width: 3.5449
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

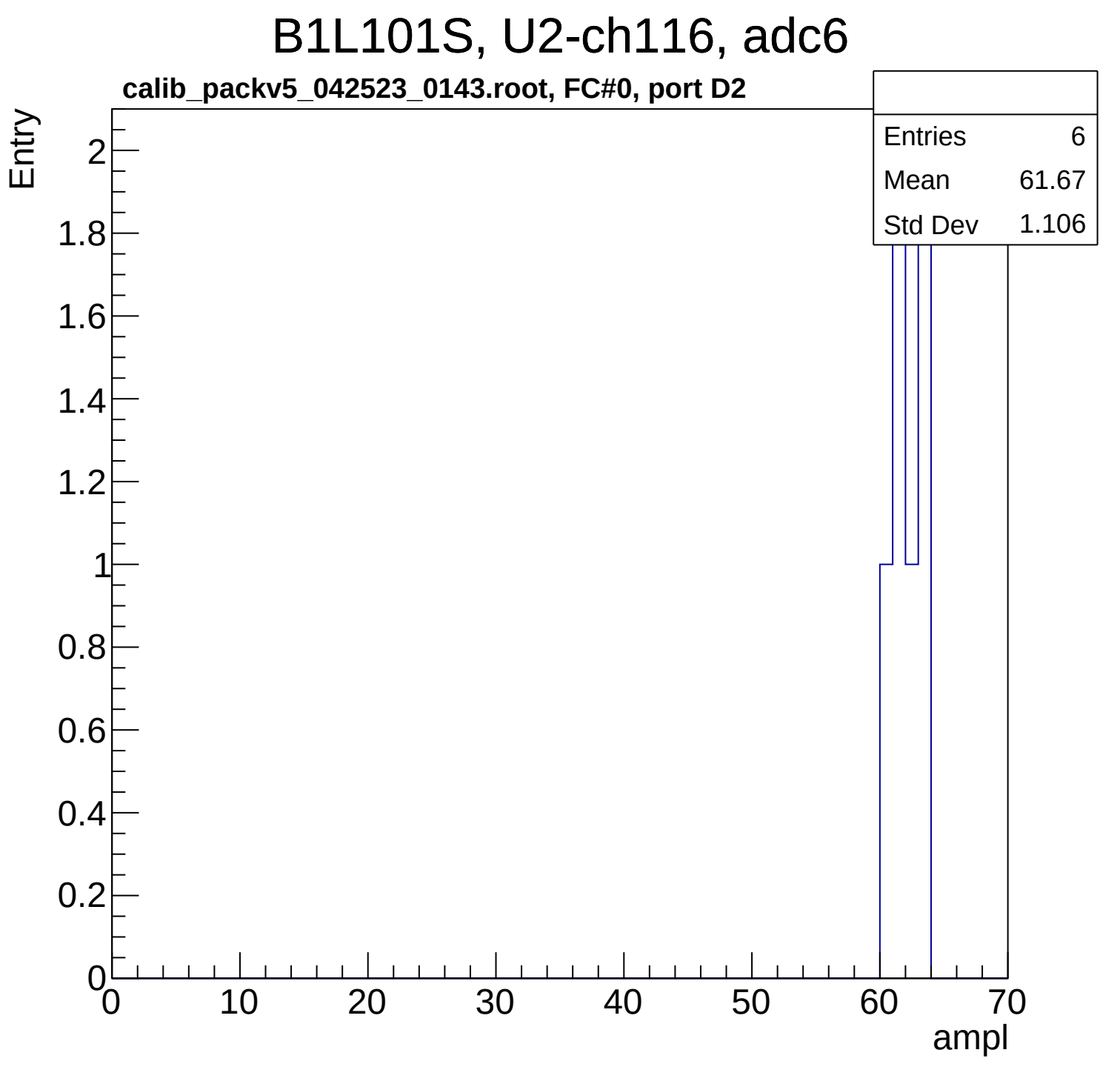

B1L101S, U2-ch116, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 74
Mean 35.76
Std Dev 3.763
Gaus mean : 36.2182
Gaus Width: 3.5698
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

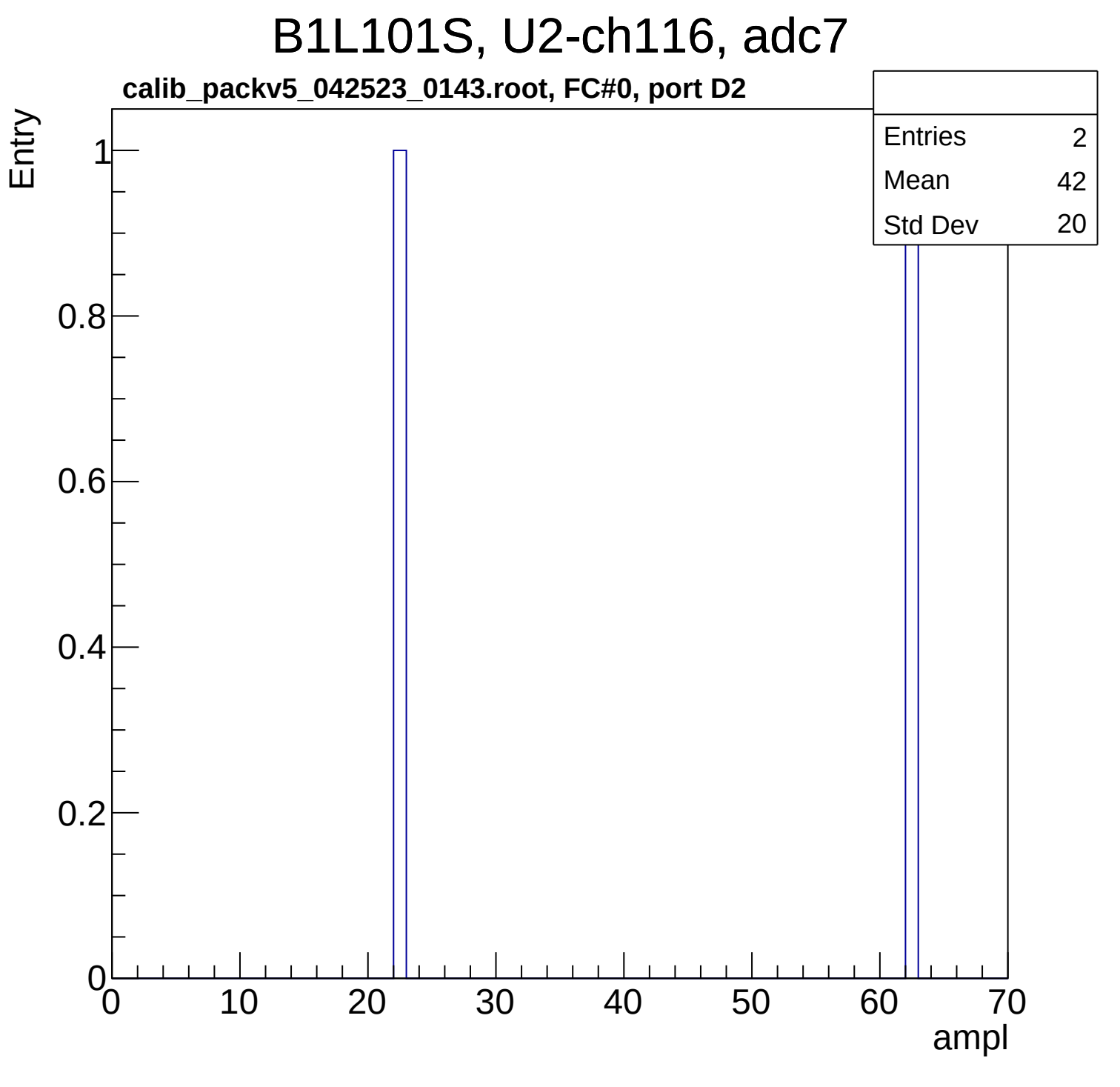

B1L101S, U2-ch116, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 42.5
Std Dev 3.273
Gaus mean : 43.5310
Gaus Width: 3.2894
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

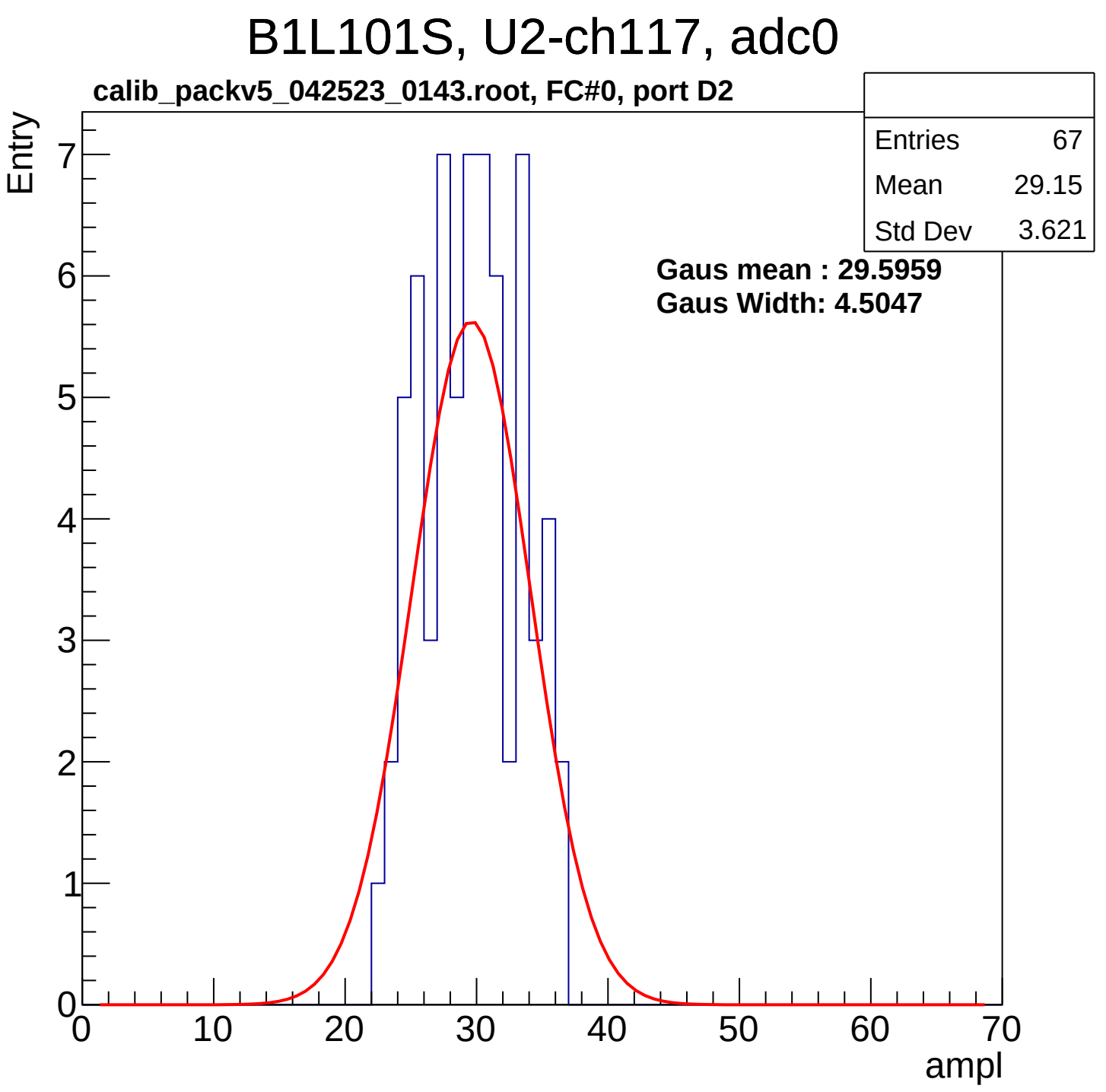

B1L101S, U2-ch116, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 48.73
Std Dev 3.745
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

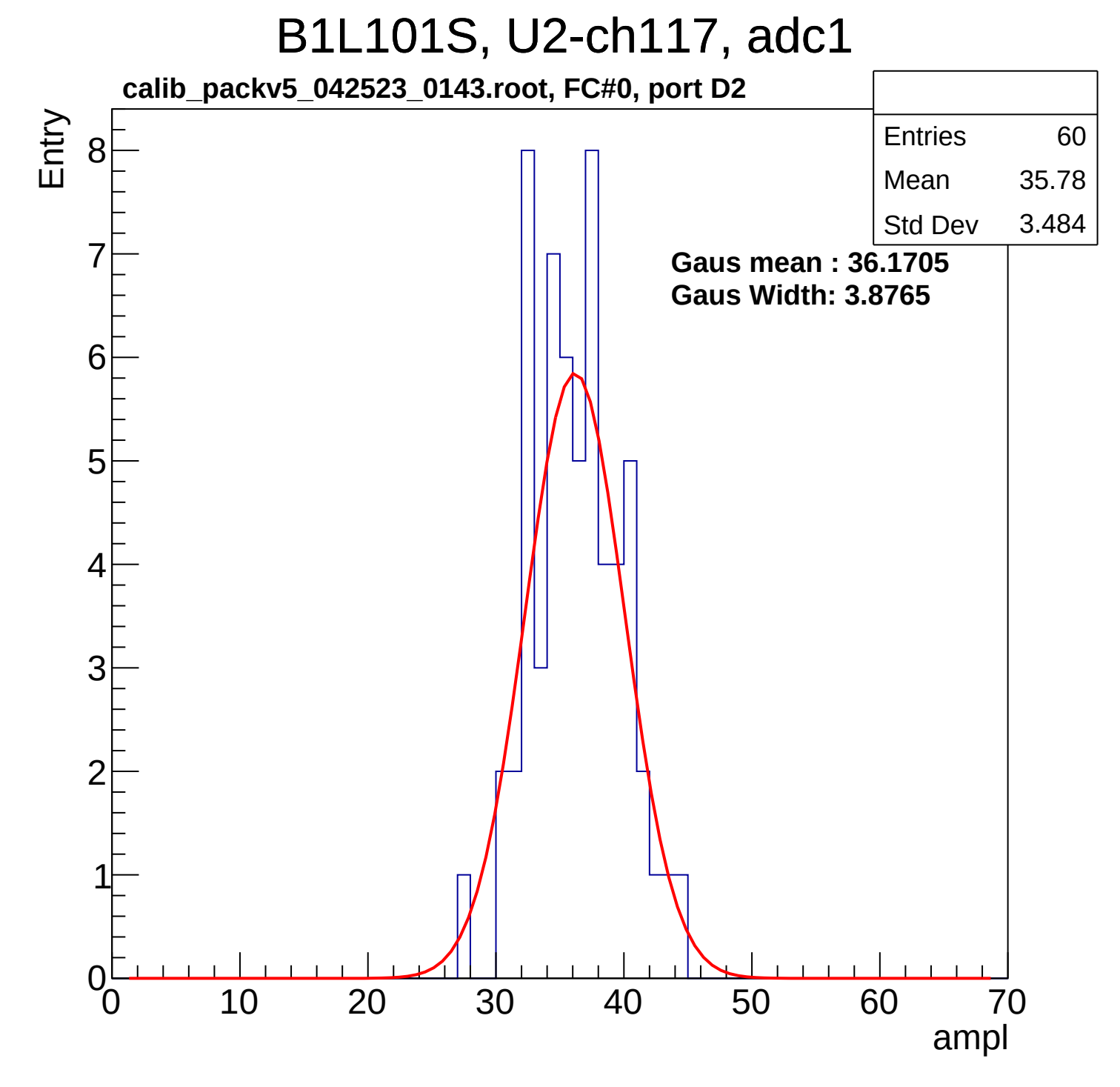

B1L101S, U2-ch116, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 54.34
Std Dev 7.917
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

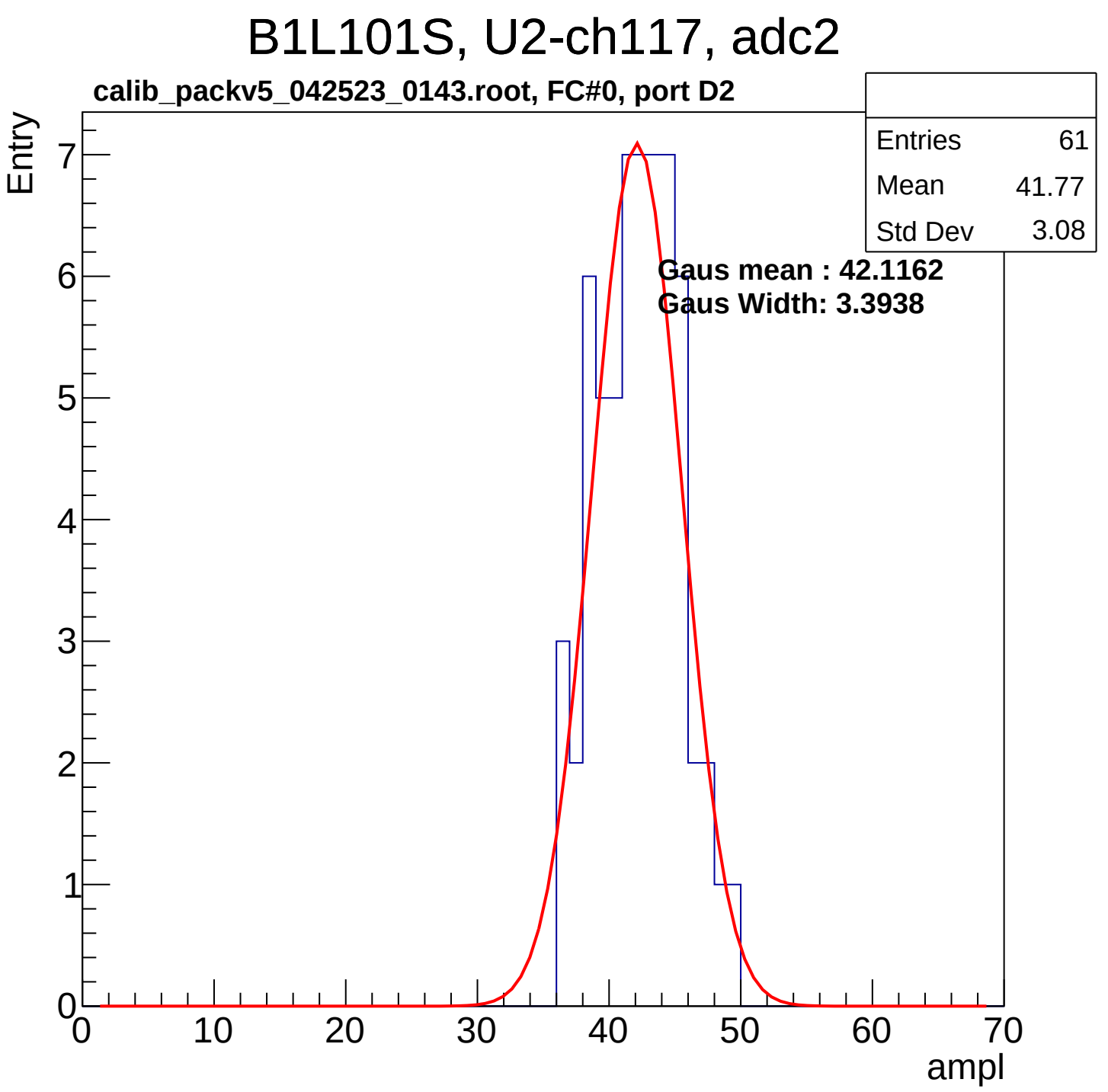

B1L101S, U2-ch116, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 59.64
Std Dev 2.592
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

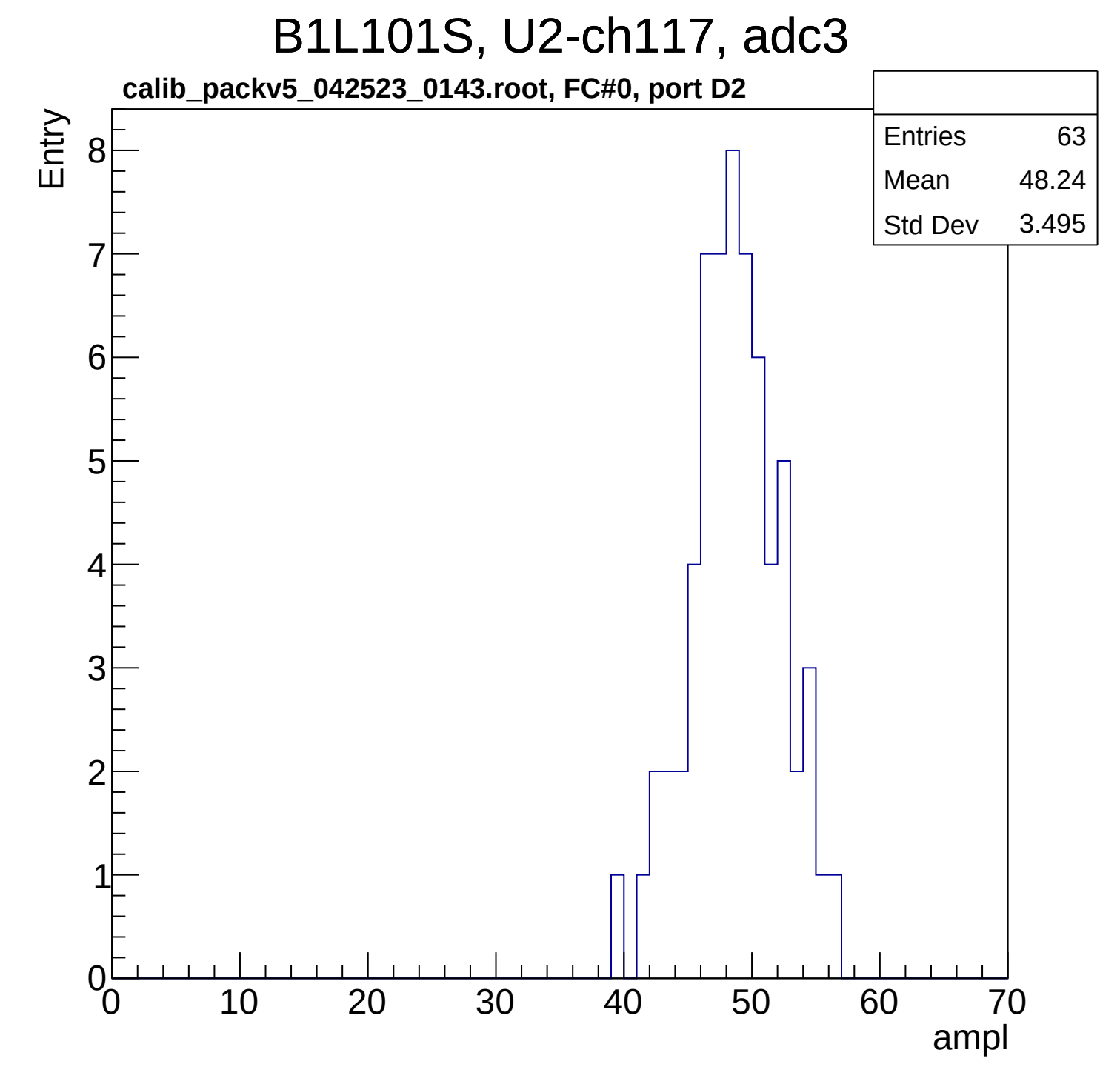

B1L101S, U2-ch116, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 6
Mean 61.67
Std Dev 1.106
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

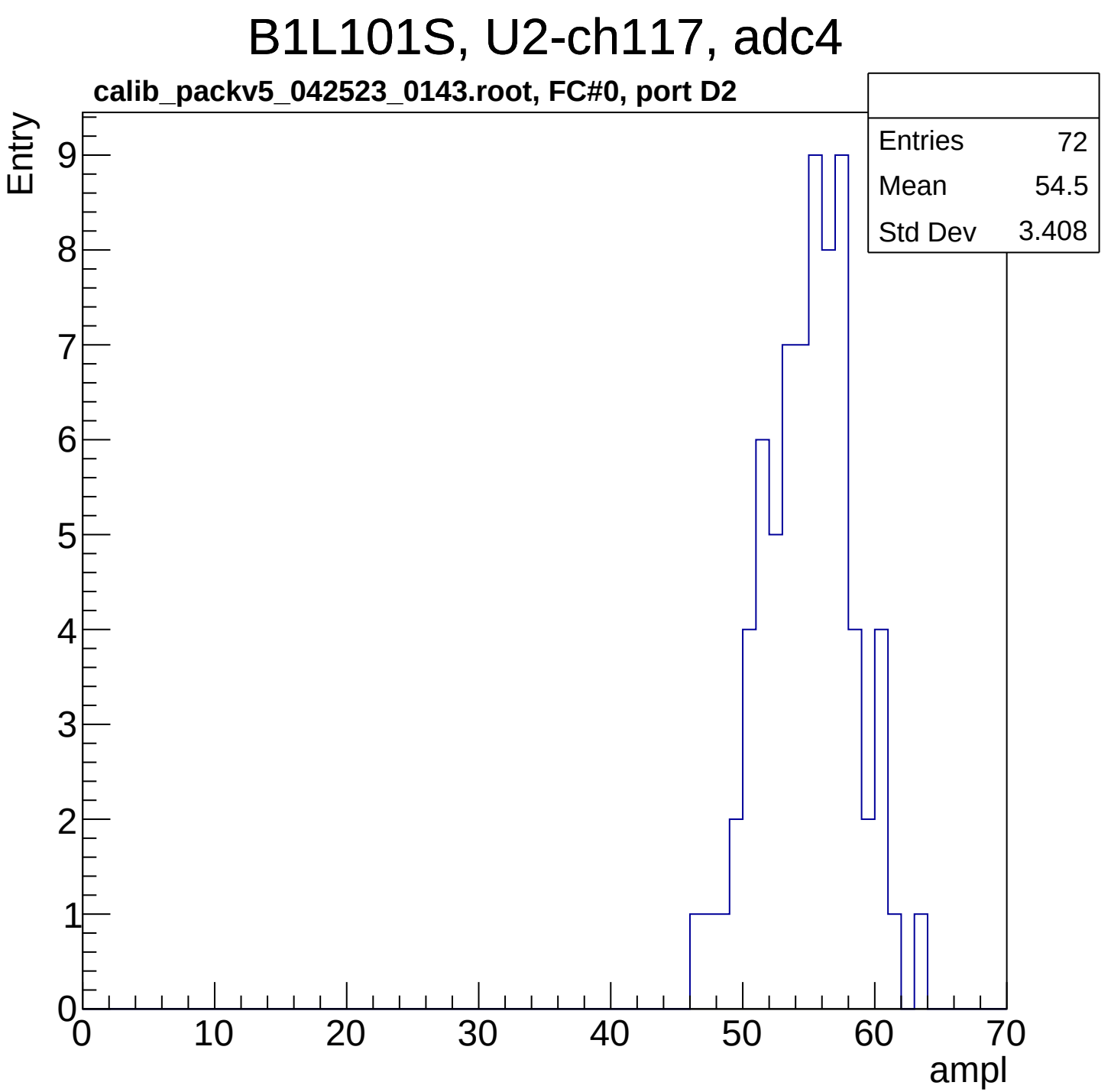

B1L101S, U2-ch116, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 42
Std Dev 20
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

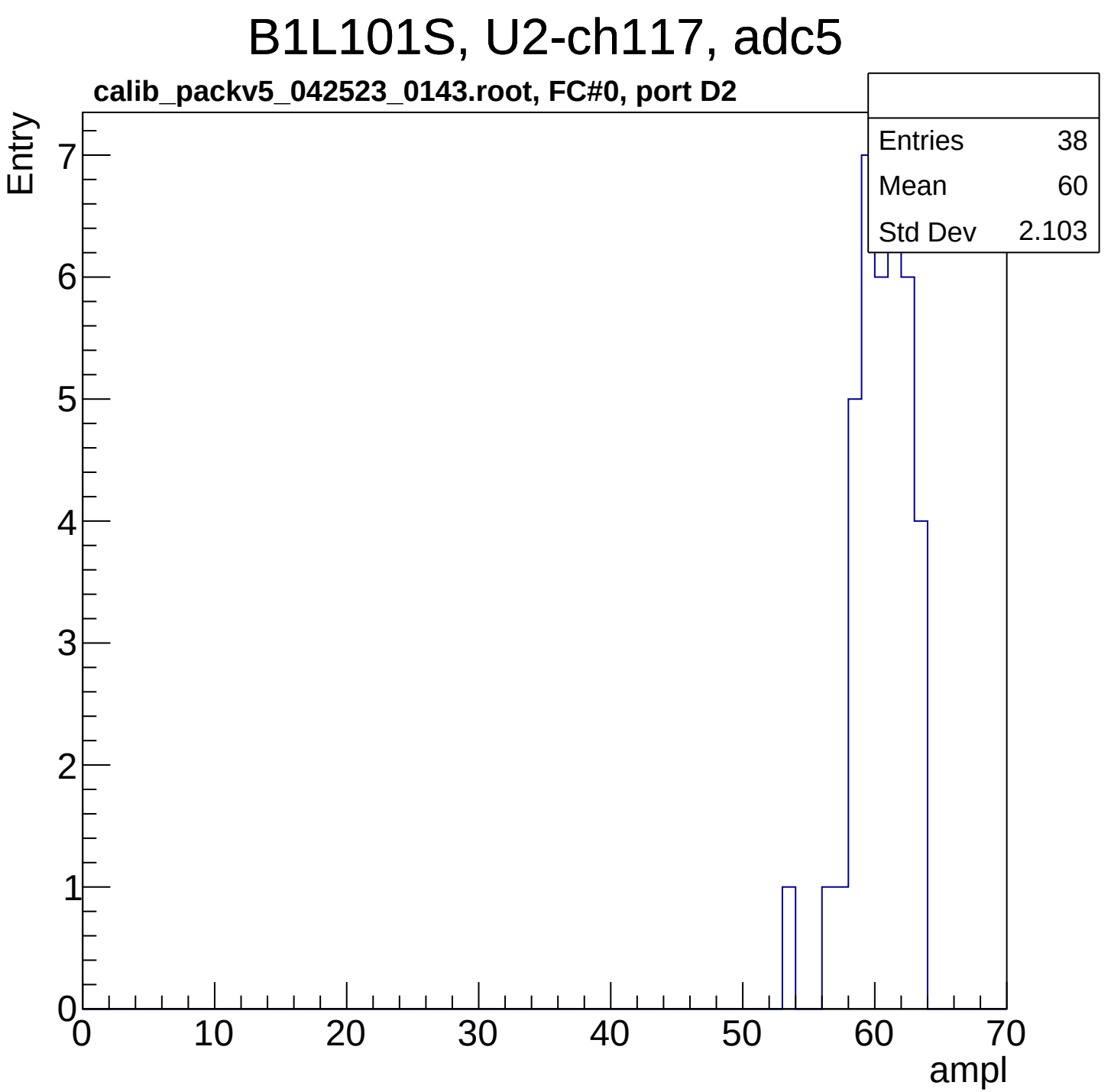

B1L101S, U2-ch117, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 29.15
Std Dev 3.621
Gaus mean : 29.5959
Gaus Width: 4.5047
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

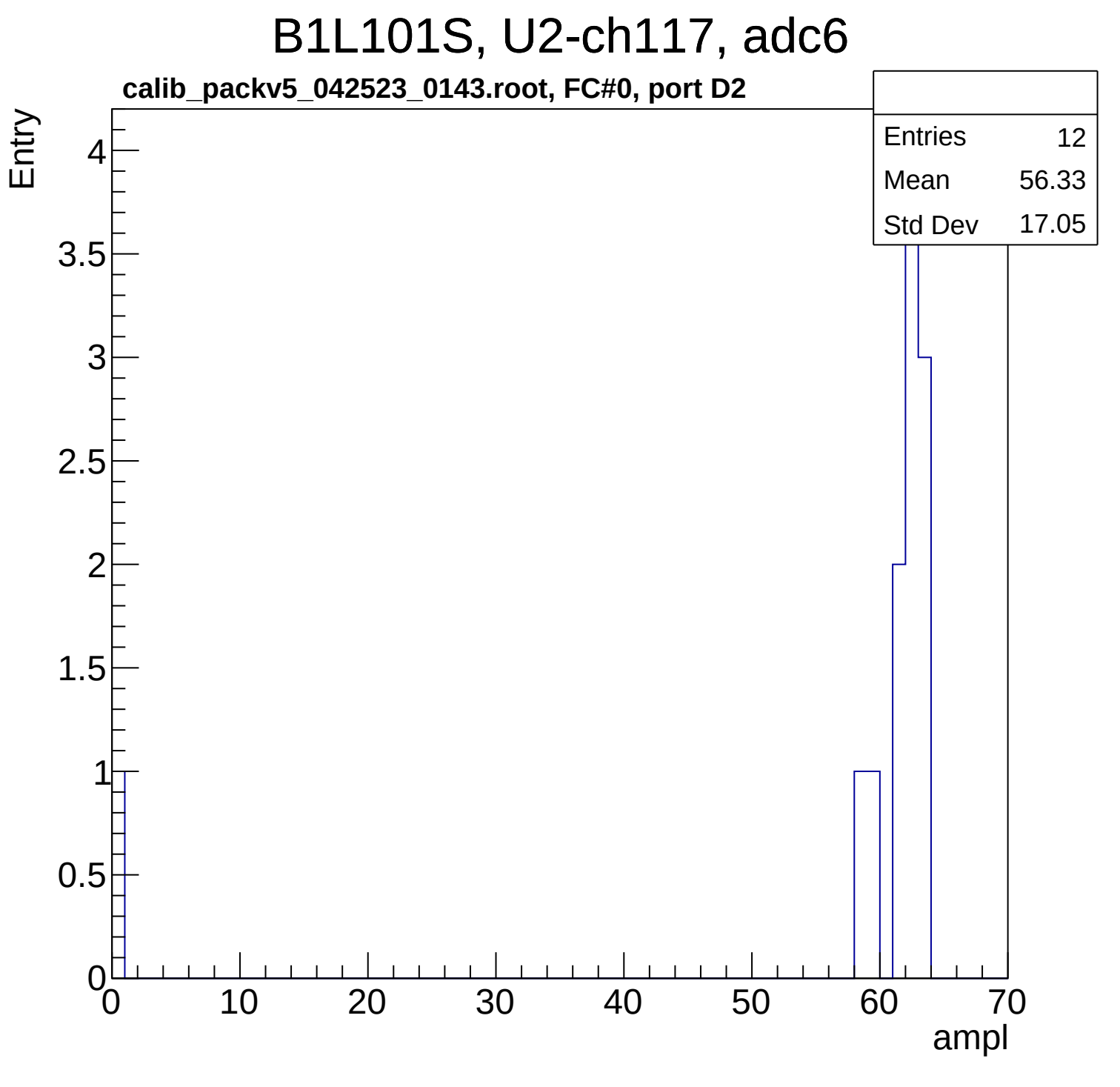

B1L101S, U2-ch117, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 35.78
Std Dev 3.484
Gaus mean : 36.1705
Gaus Width: 3.8765
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

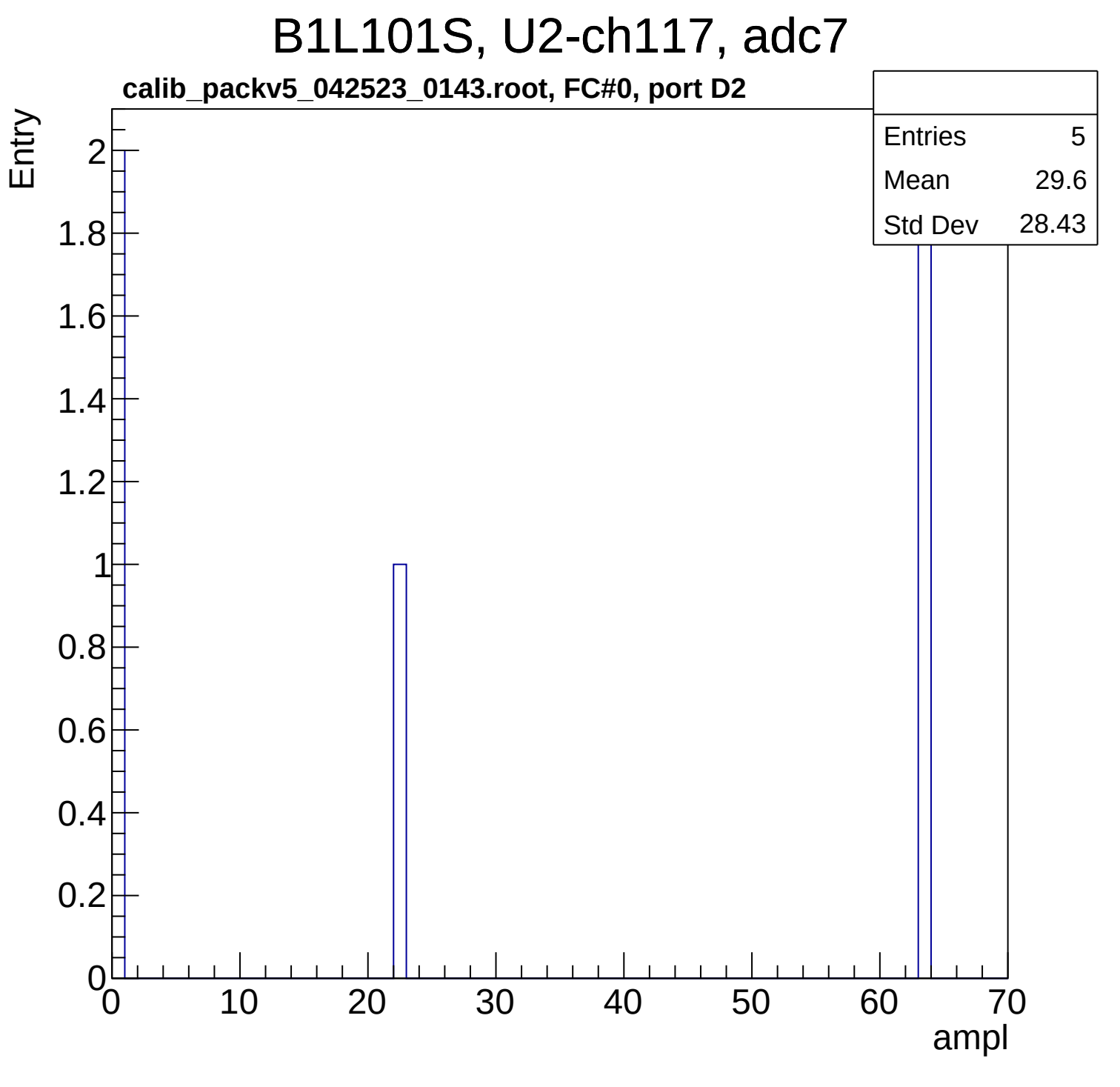

B1L101S, U2-ch117, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 41.77
Std Dev 3.08
Gaus mean : 42.1162
Gaus Width: 3.3938
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

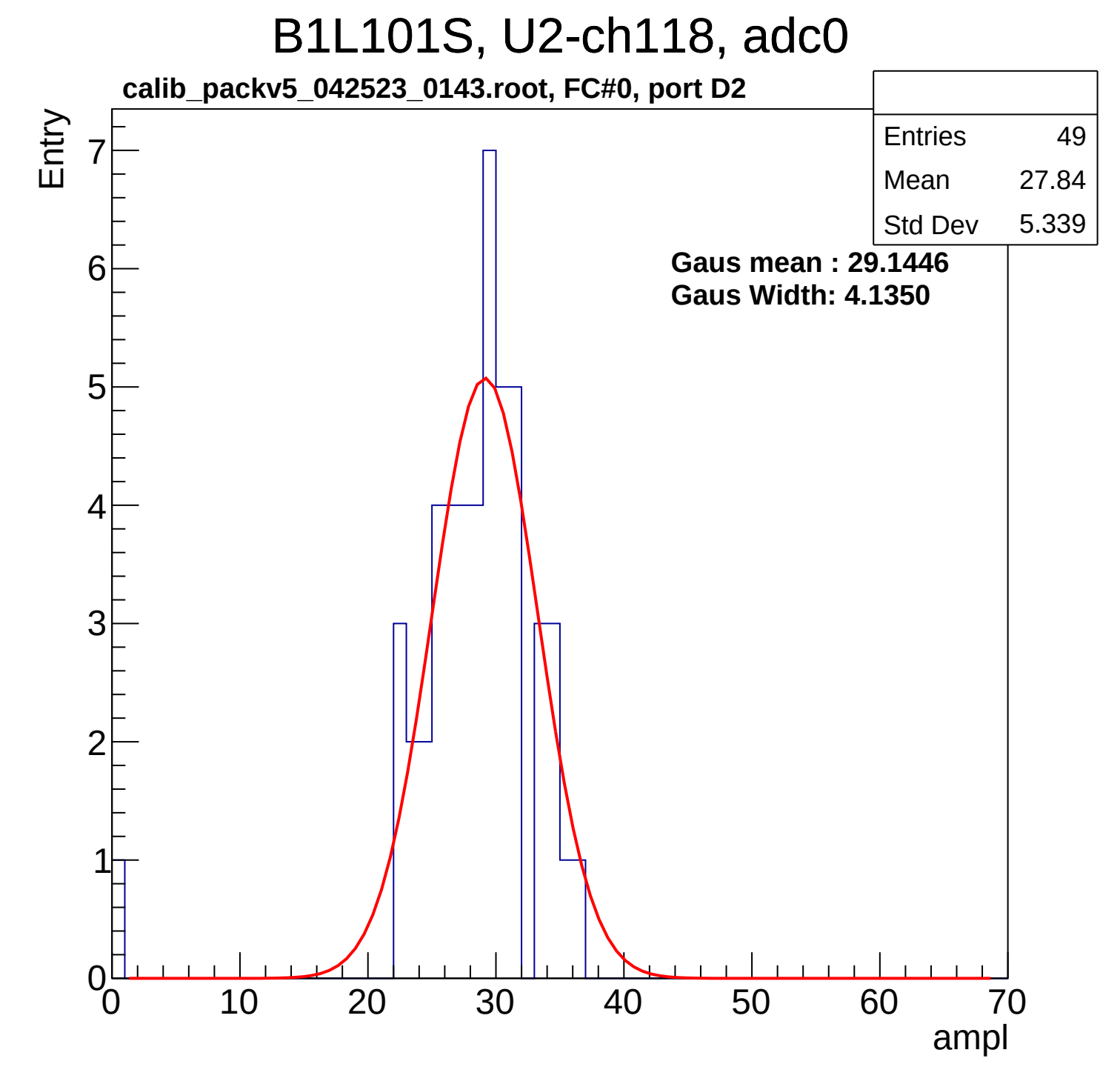

B1L101S, U2-ch117, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 48.24
Std Dev 3.495
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

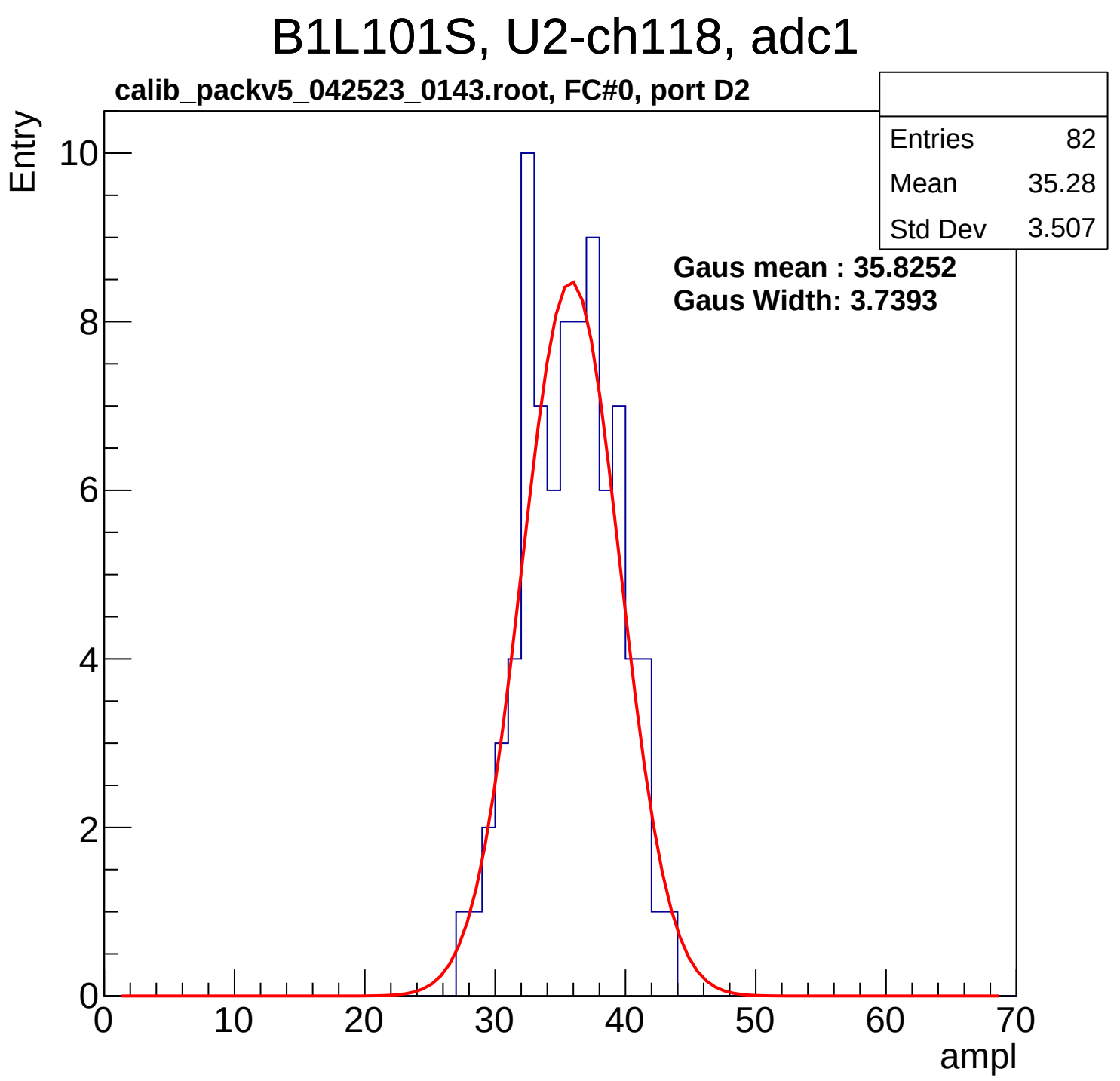

B1L101S, U2-ch117, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 72
Mean 54.5
Std Dev 3.408
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

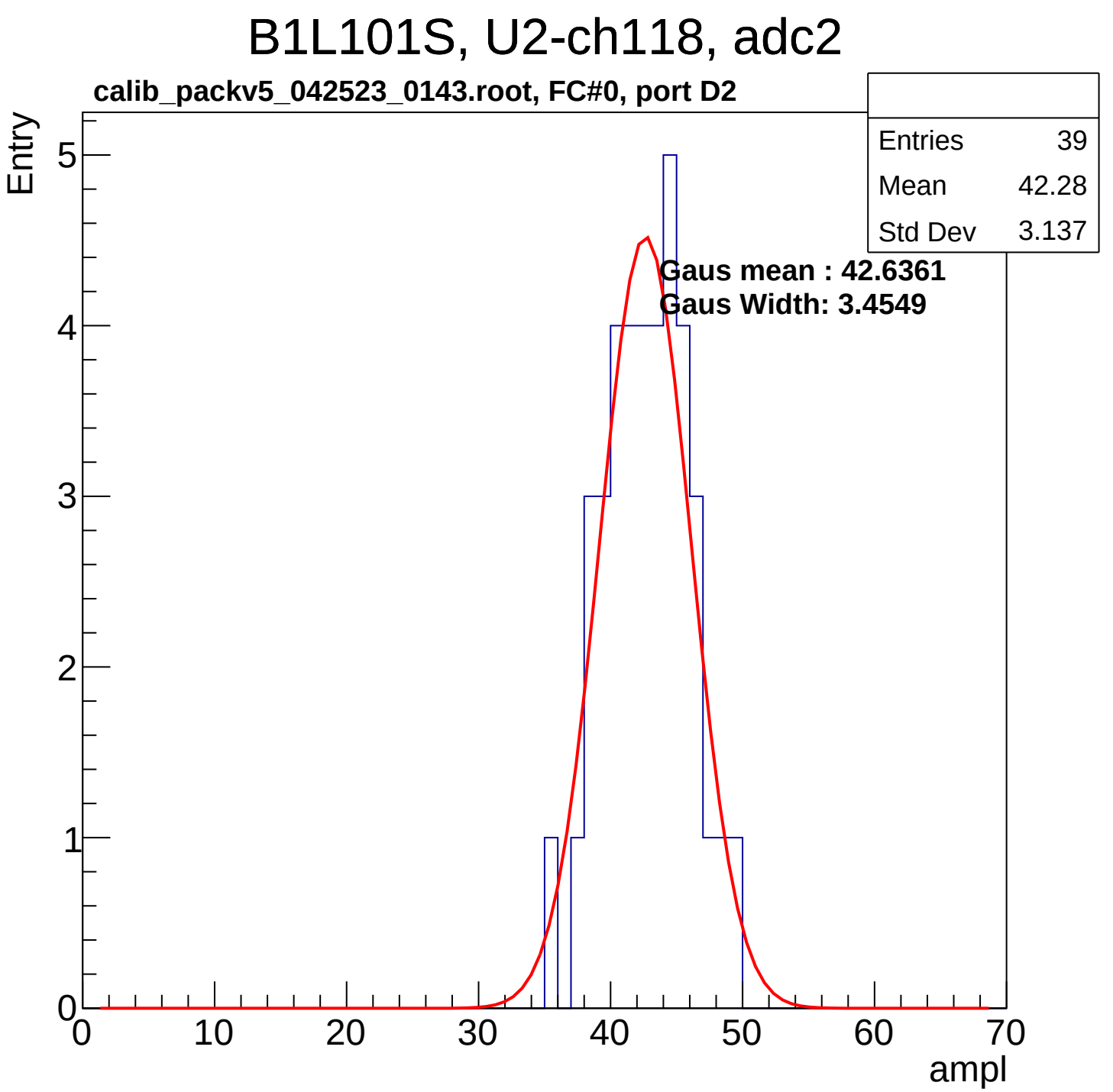

B1L101S, U2-ch117, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 38
Mean 60
Std Dev 2.103
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

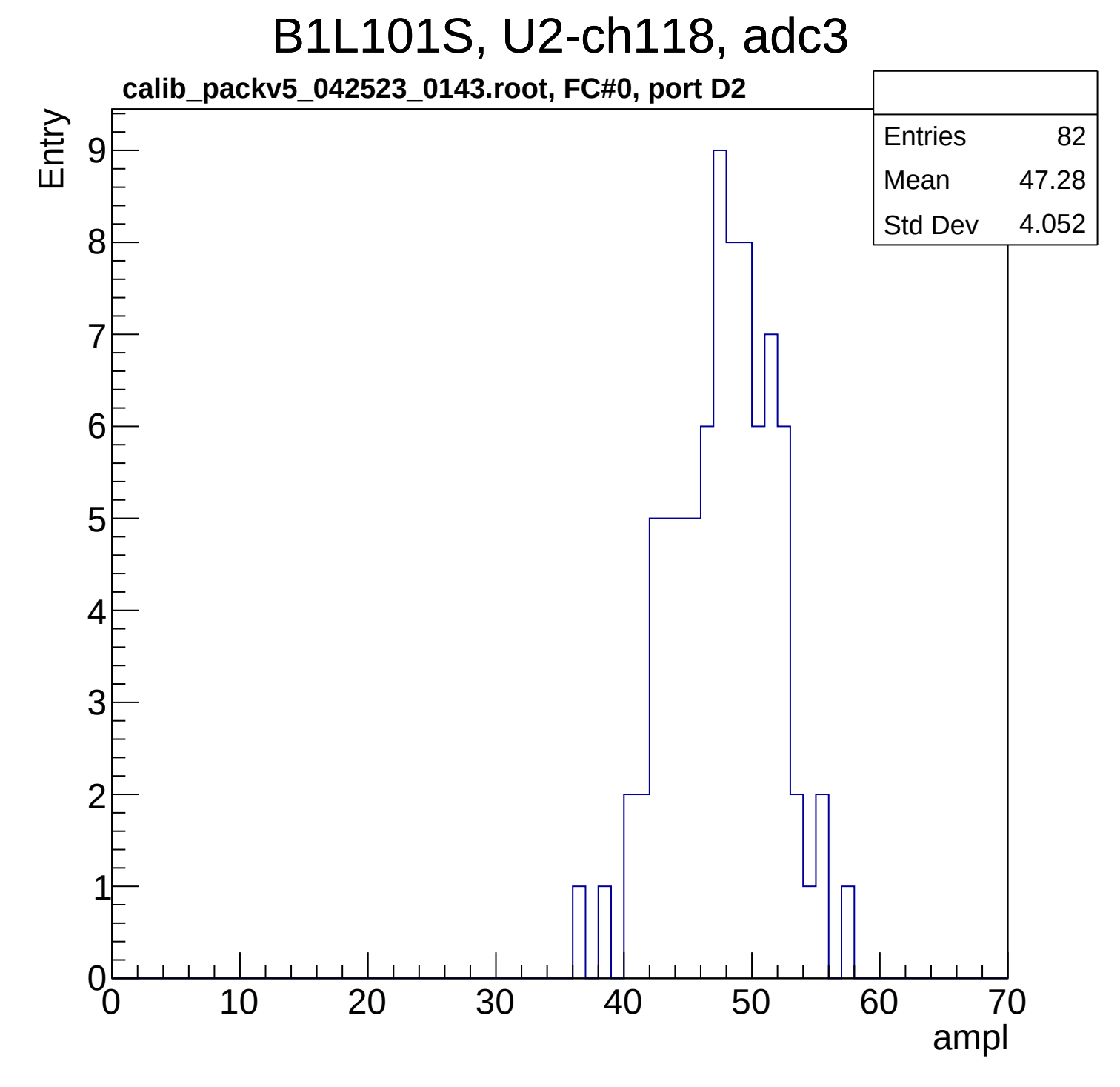

B1L101S, U2-ch117, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 12
Mean 56.33
Std Dev 17.05
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

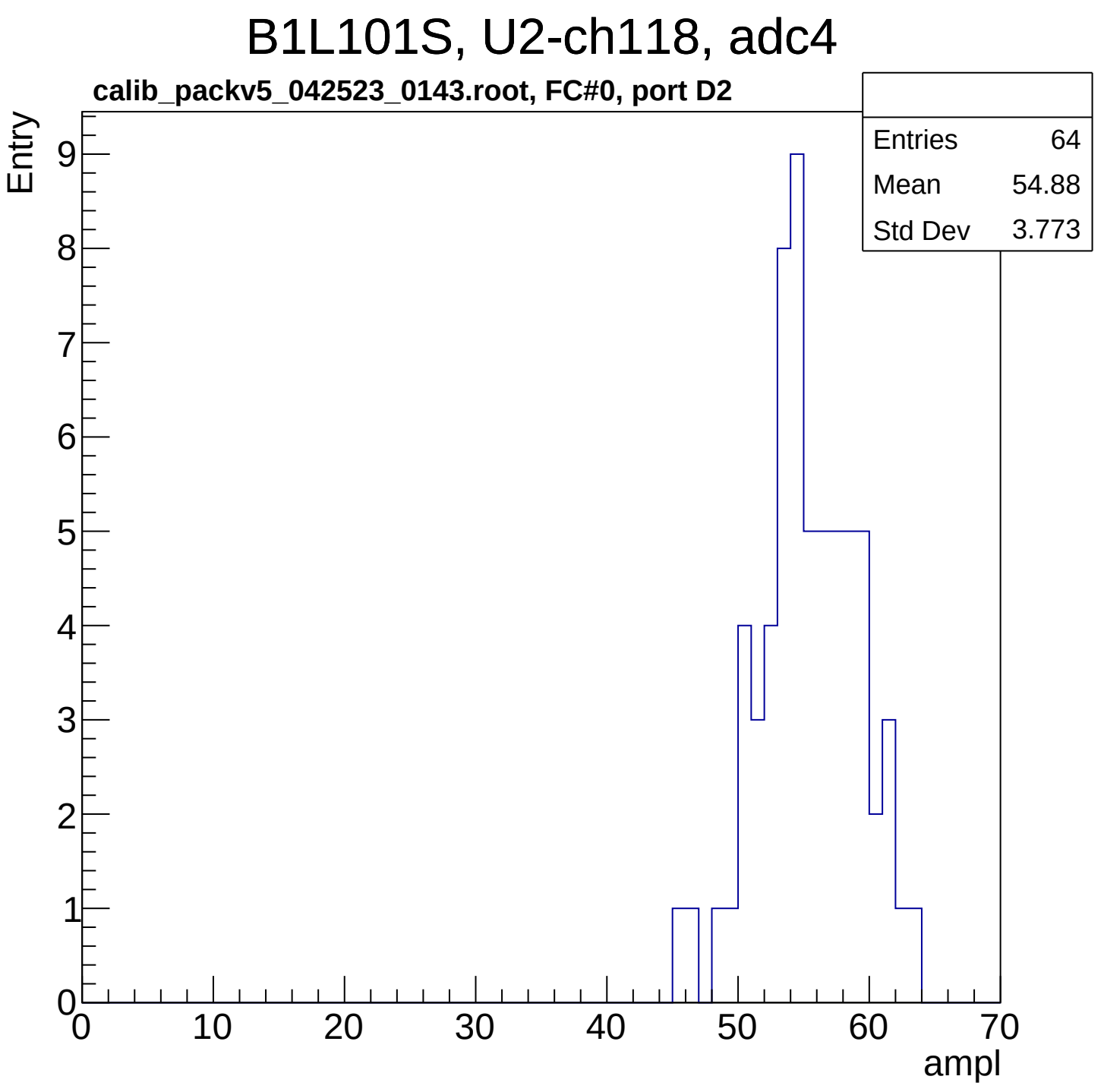

B1L101S, U2-ch117, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 29.6
Std Dev 28.43
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

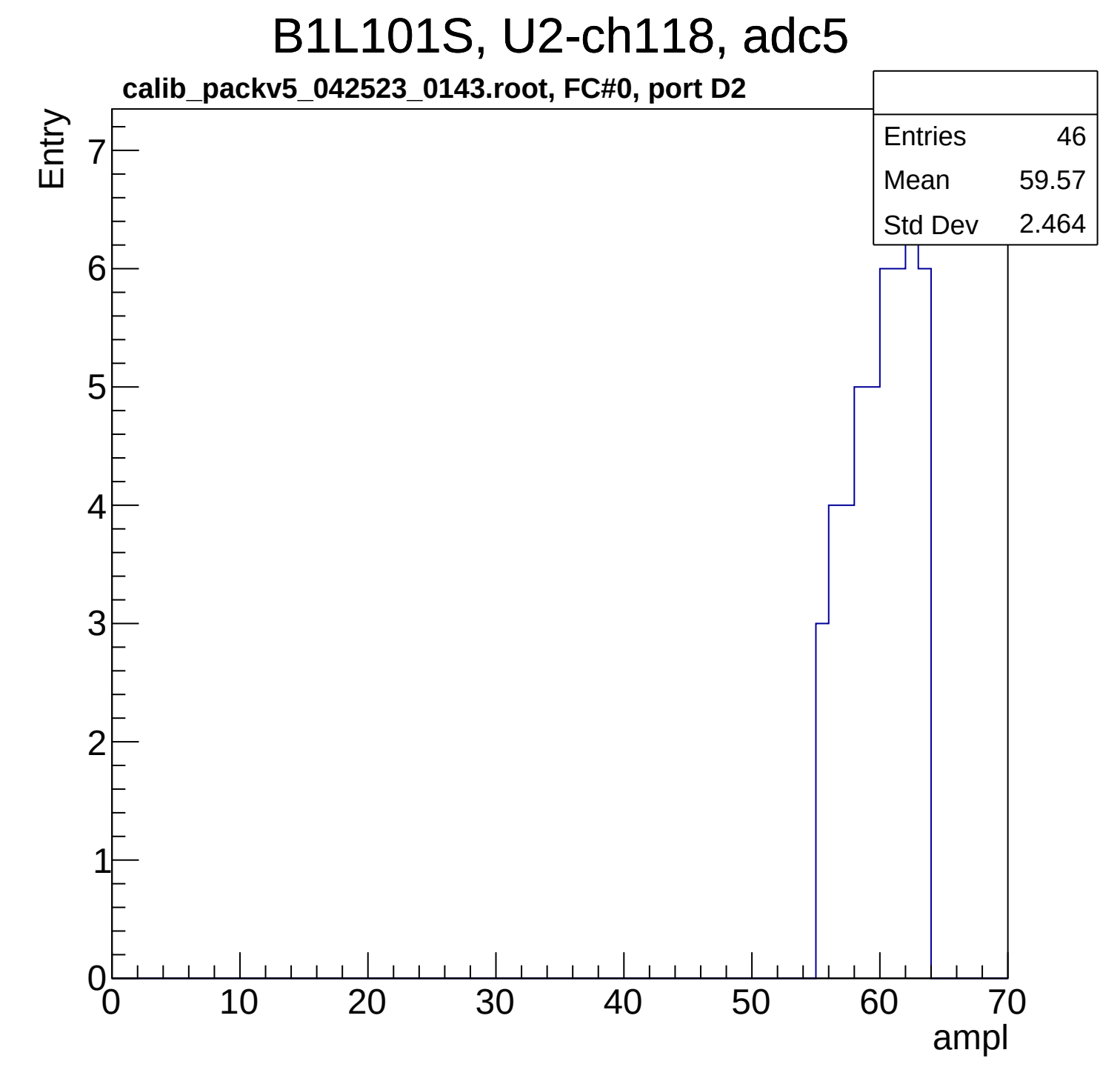

B1L101S, U2-ch118, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 49
Mean 27.84
Std Dev 5.339
Gaus mean : 29.1446
Gaus Width: 4.1350
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

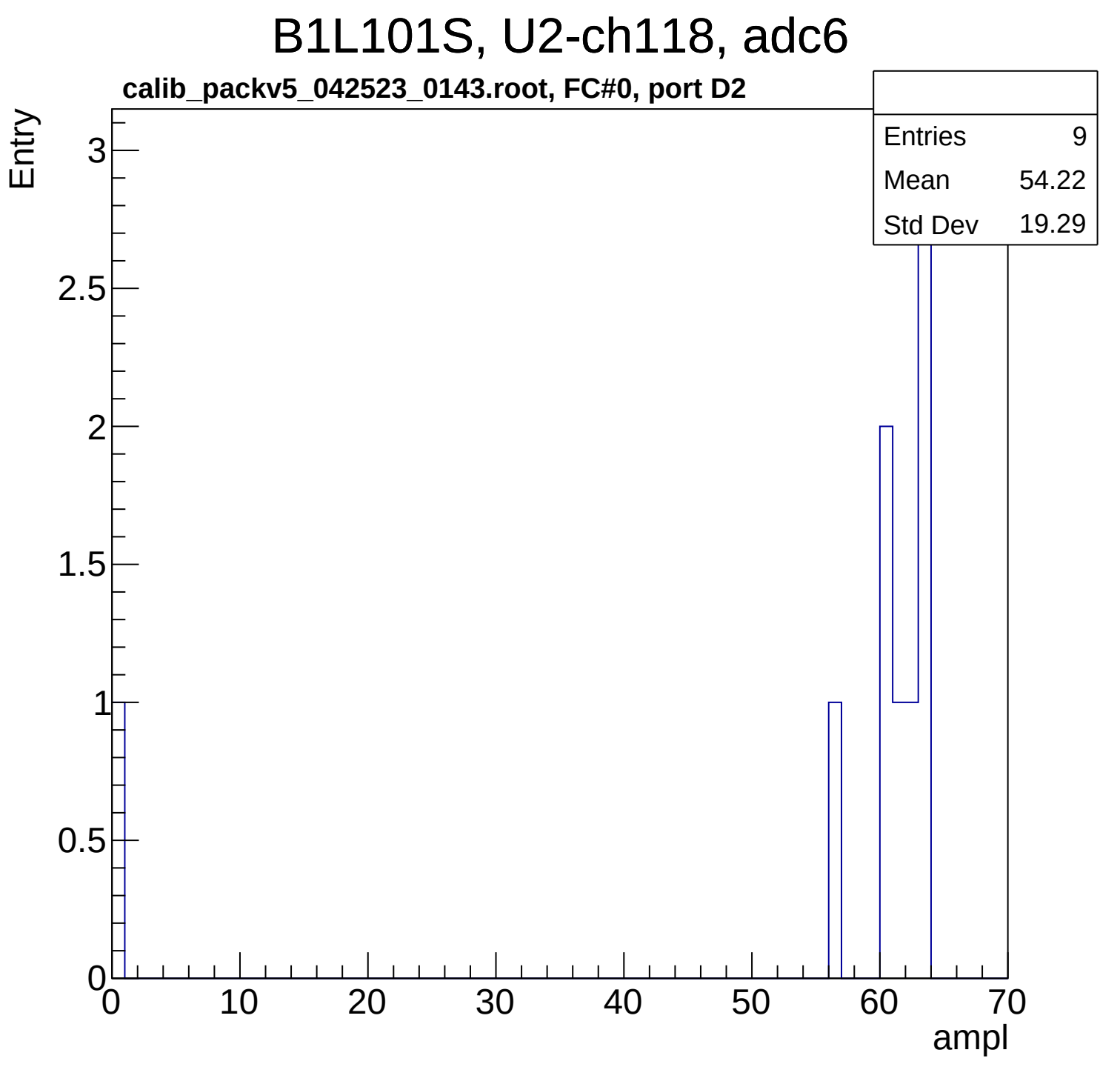

B1L101S, U2-ch118, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 82
Mean 35.28
Std Dev 3.507
Gaus mean : 35.8252
Gaus Width: 3.7393
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

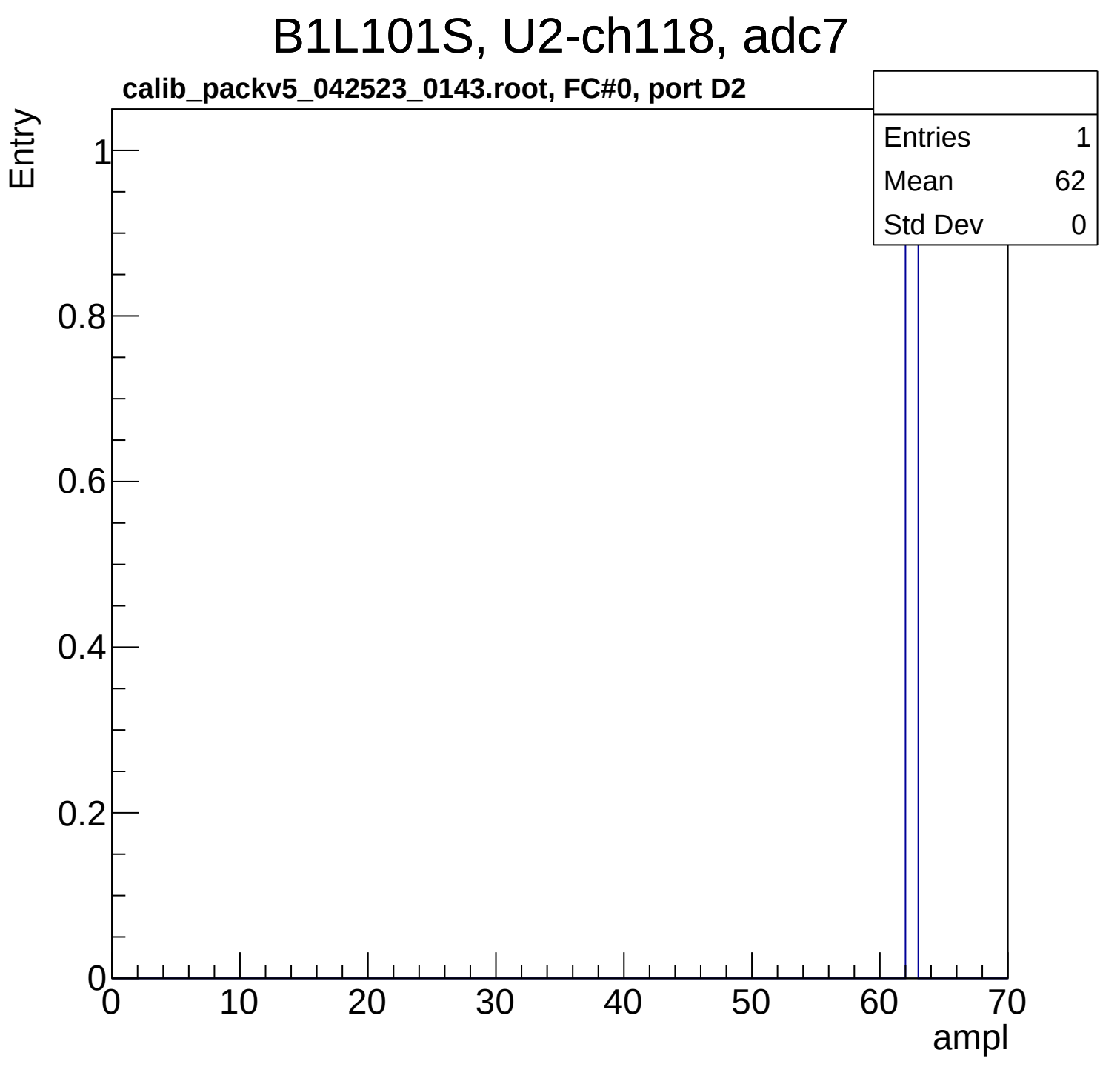

B1L101S, U2-ch118, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 39
Mean 42.28
Std Dev 3.137
Gaus mean : 42.6361
Gaus Width: 3.4549
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

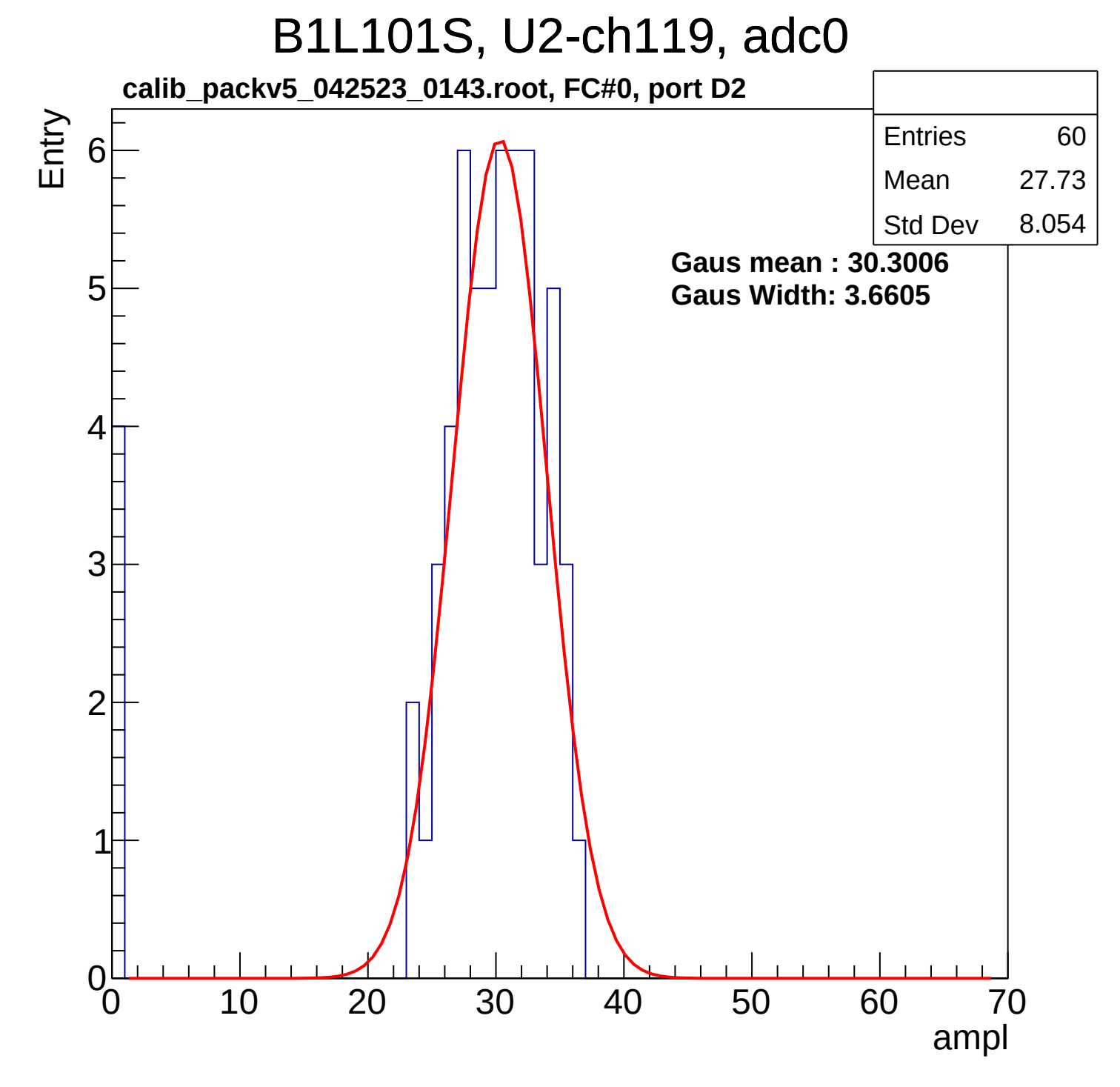

B1L101S, U2-ch118, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 82
Mean 47.28
Std Dev 4.052
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

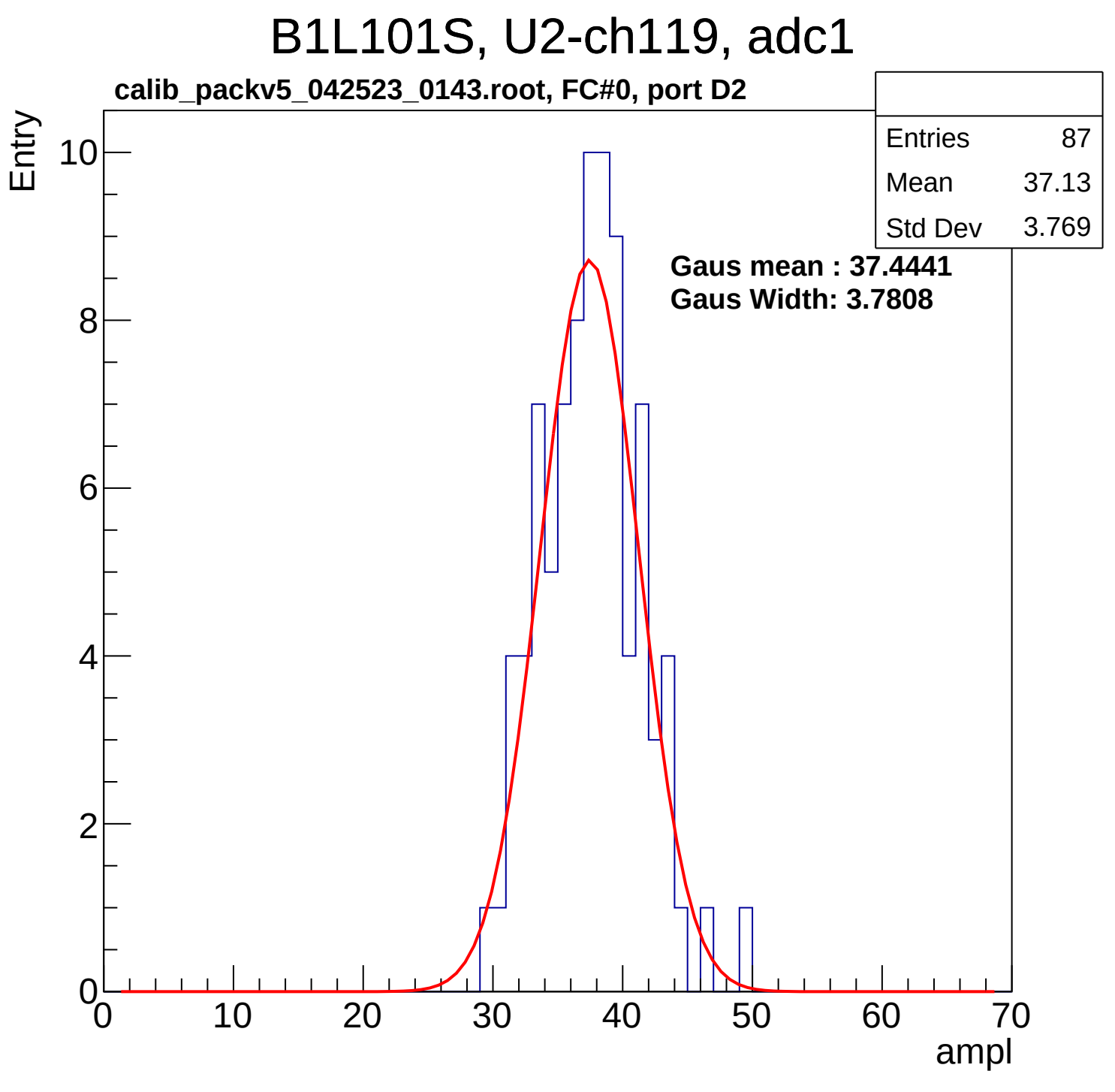

B1L101S, U2-ch118, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 54.88
Std Dev 3.773
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

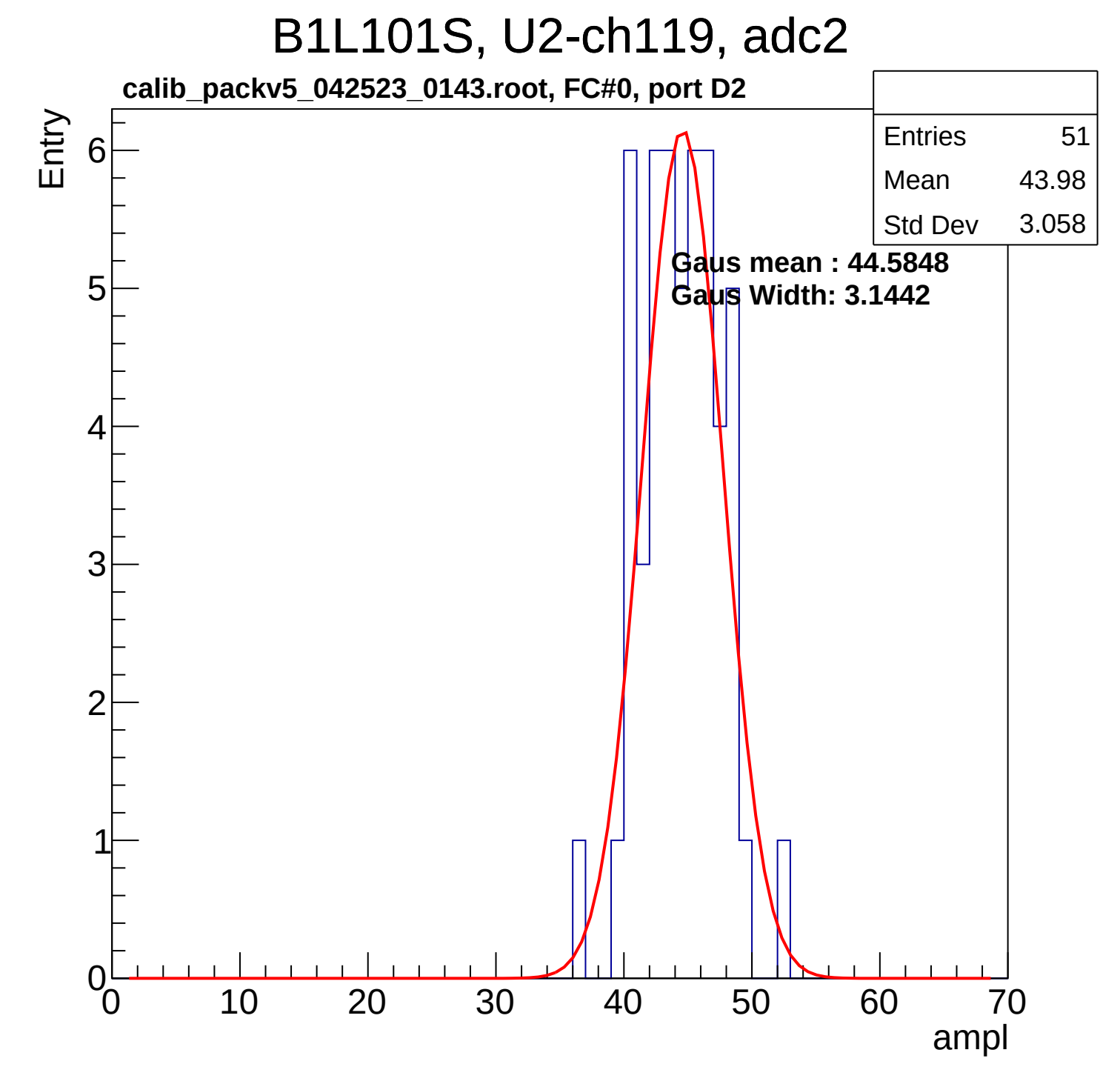

B1L101S, U2-ch118, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 59.57
Std Dev 2.464
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

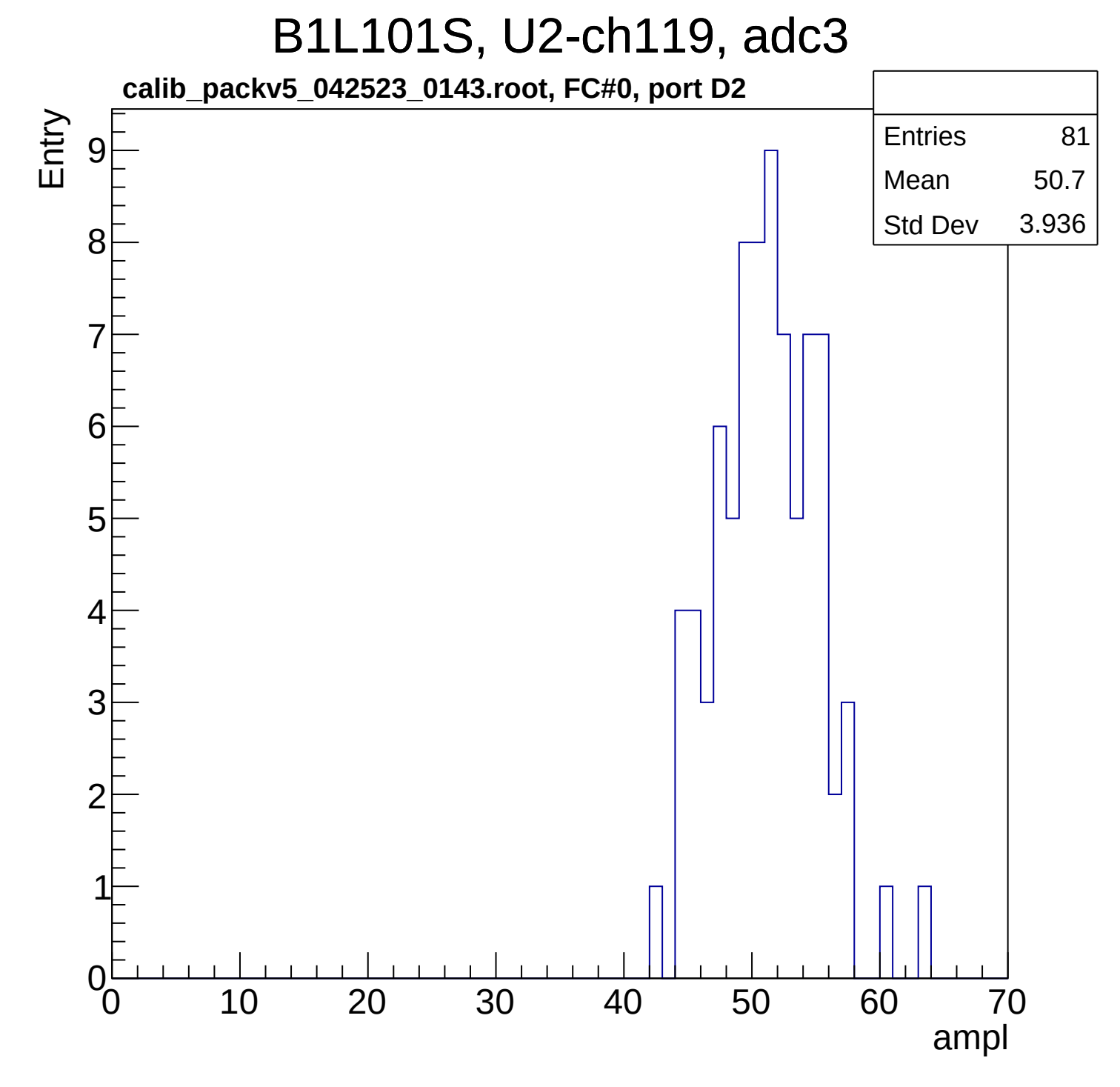

B1L101S, U2-ch118, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 9
Mean 54.22
Std Dev 19.29
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

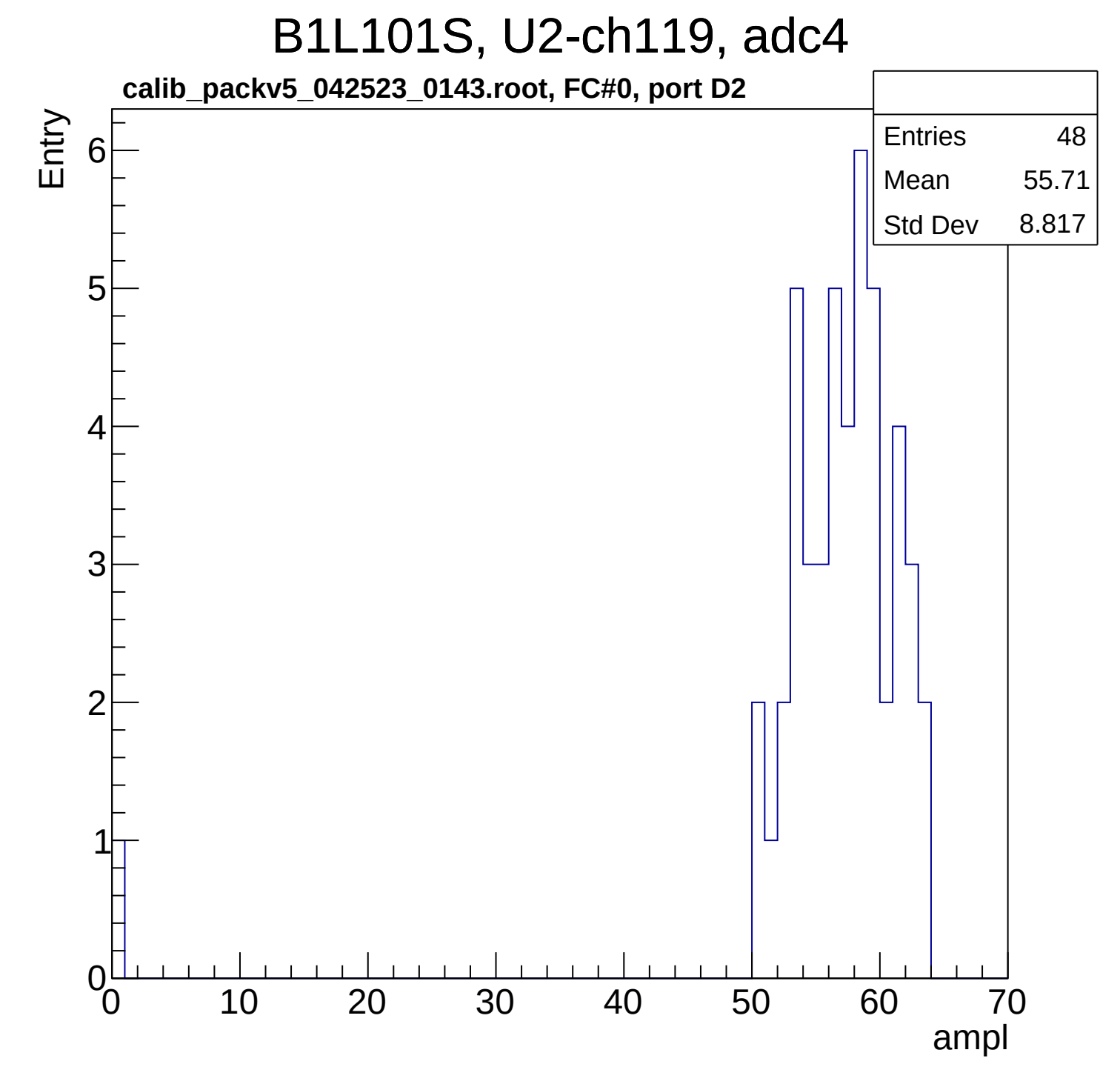

B1L101S, U2-ch118, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

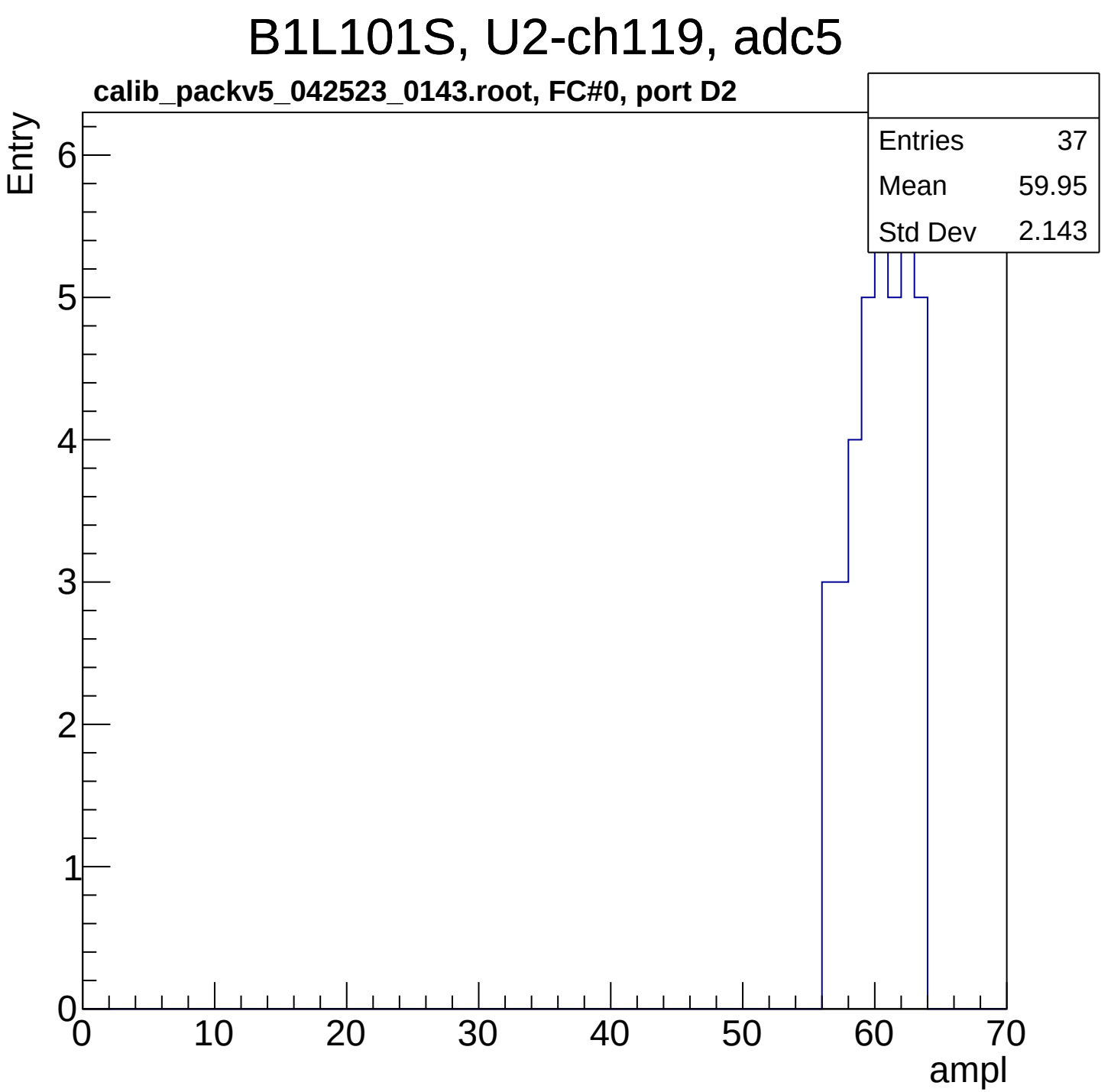

B1L101S, U2-ch119, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 27.73
Std Dev 8.054
Gaus mean : 30.3006
Gaus Width: 3.6605
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

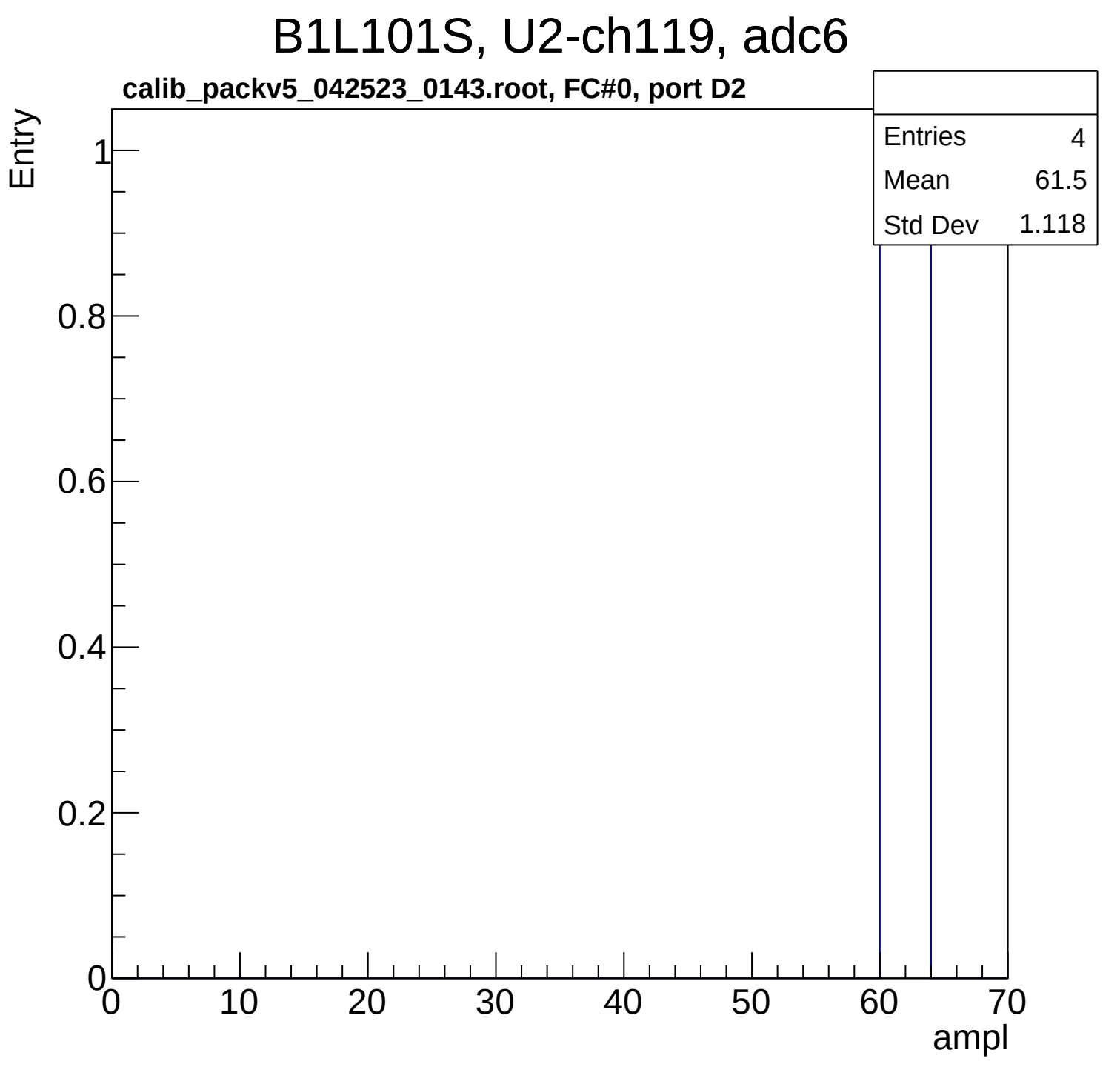

B1L101S, U2-ch119, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 87
Mean 37.13
Std Dev 3.769
Gaus mean : 37.4441
Gaus Width: 3.7808
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

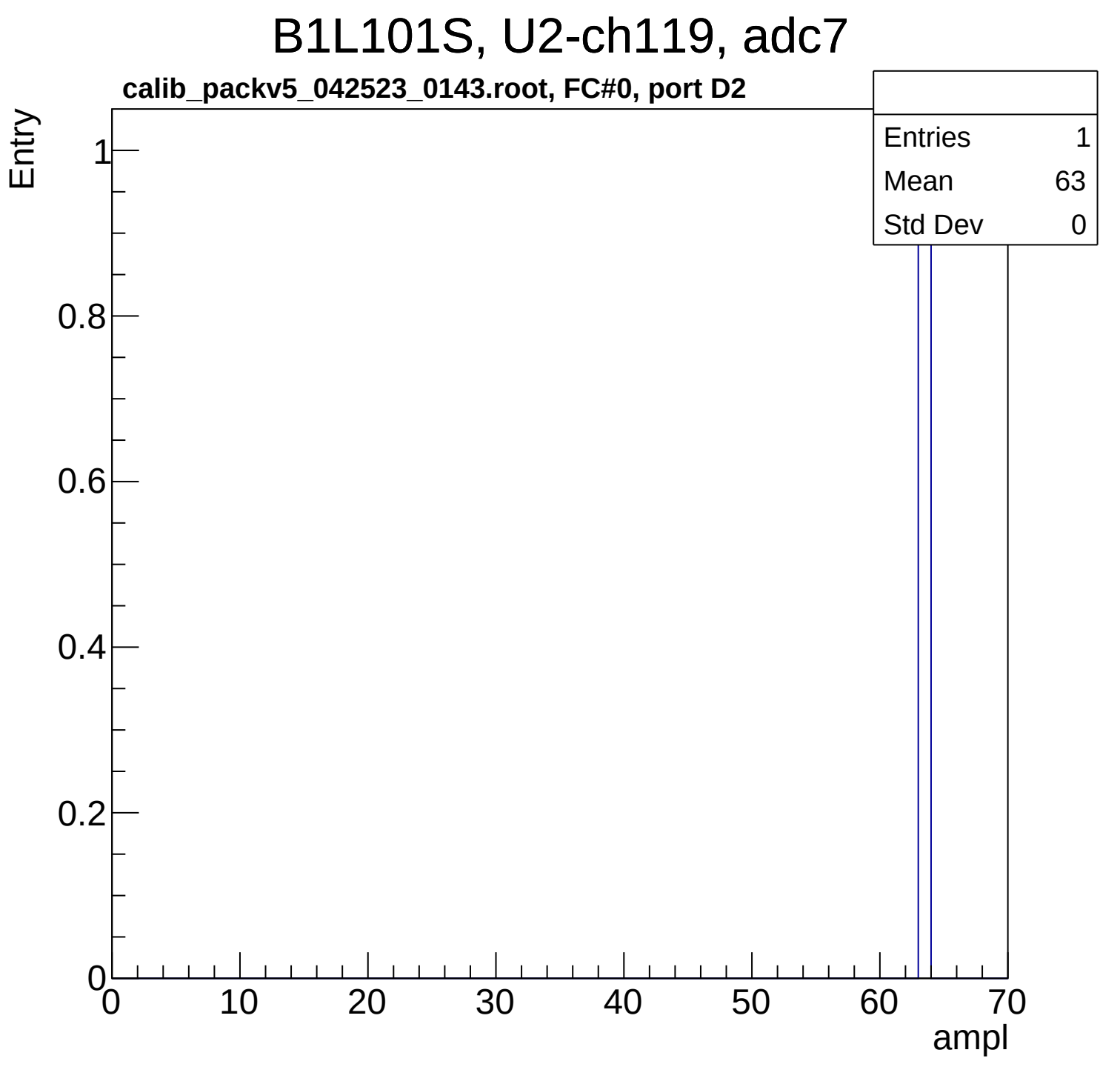

B1L101S, U2-ch119, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 43.98
Std Dev 3.058
Gaus mean : 44.5848
Gaus Width: 3.1442
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

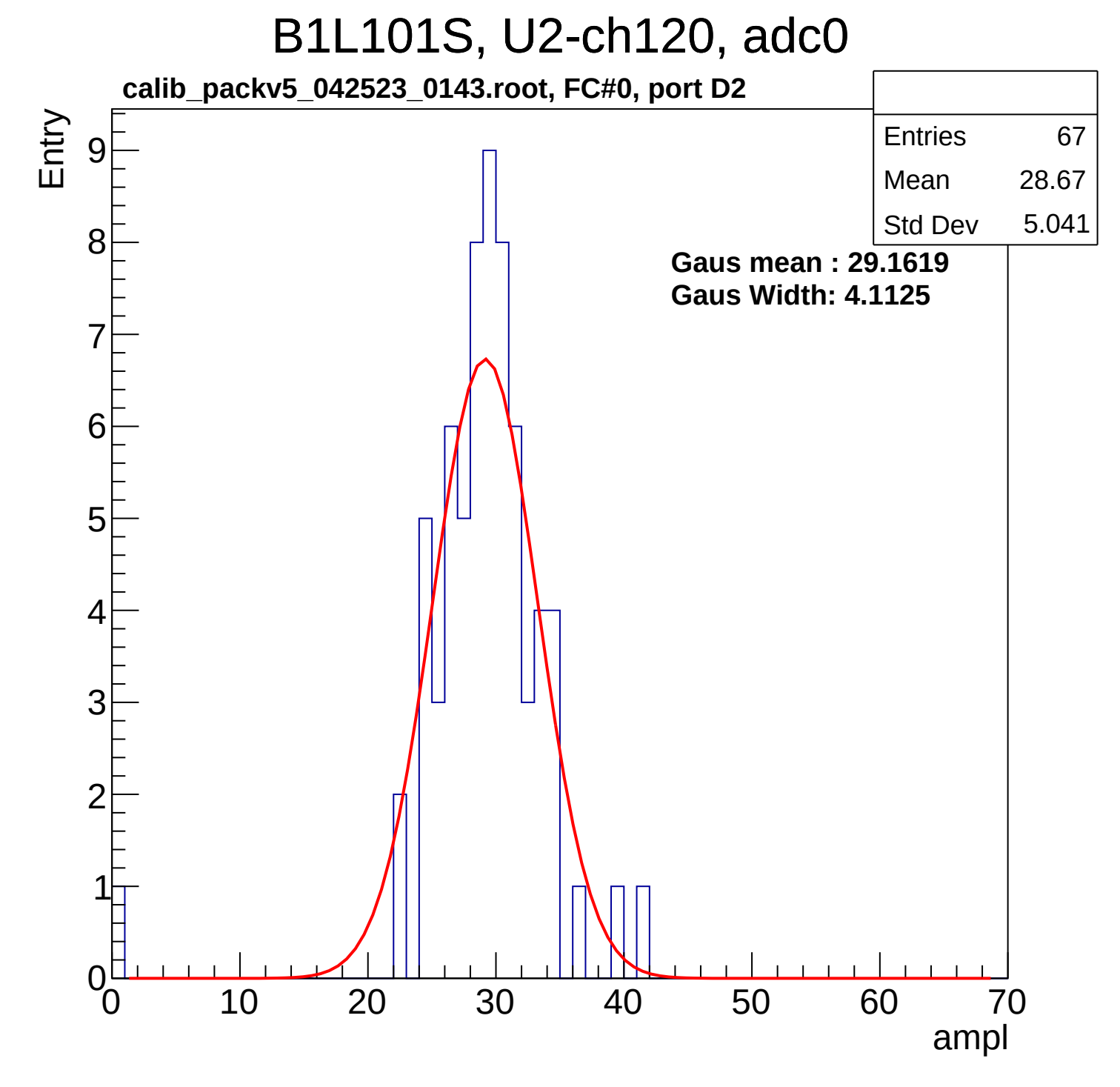

B1L101S, U2-ch119, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 81
Mean 50.7
Std Dev 3.936
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

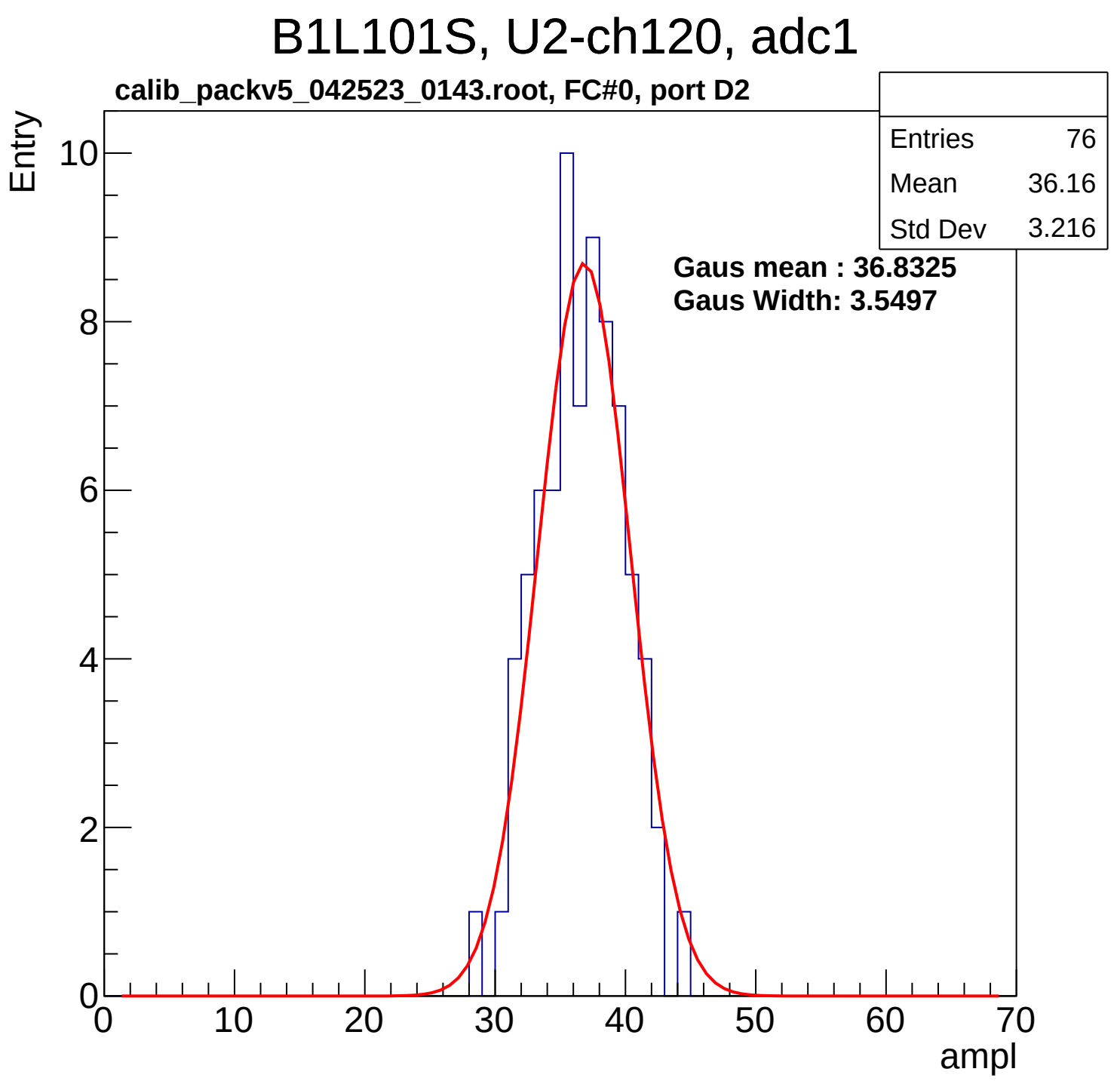

B1L101S, U2-ch119, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 55.71
Std Dev 8.817
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

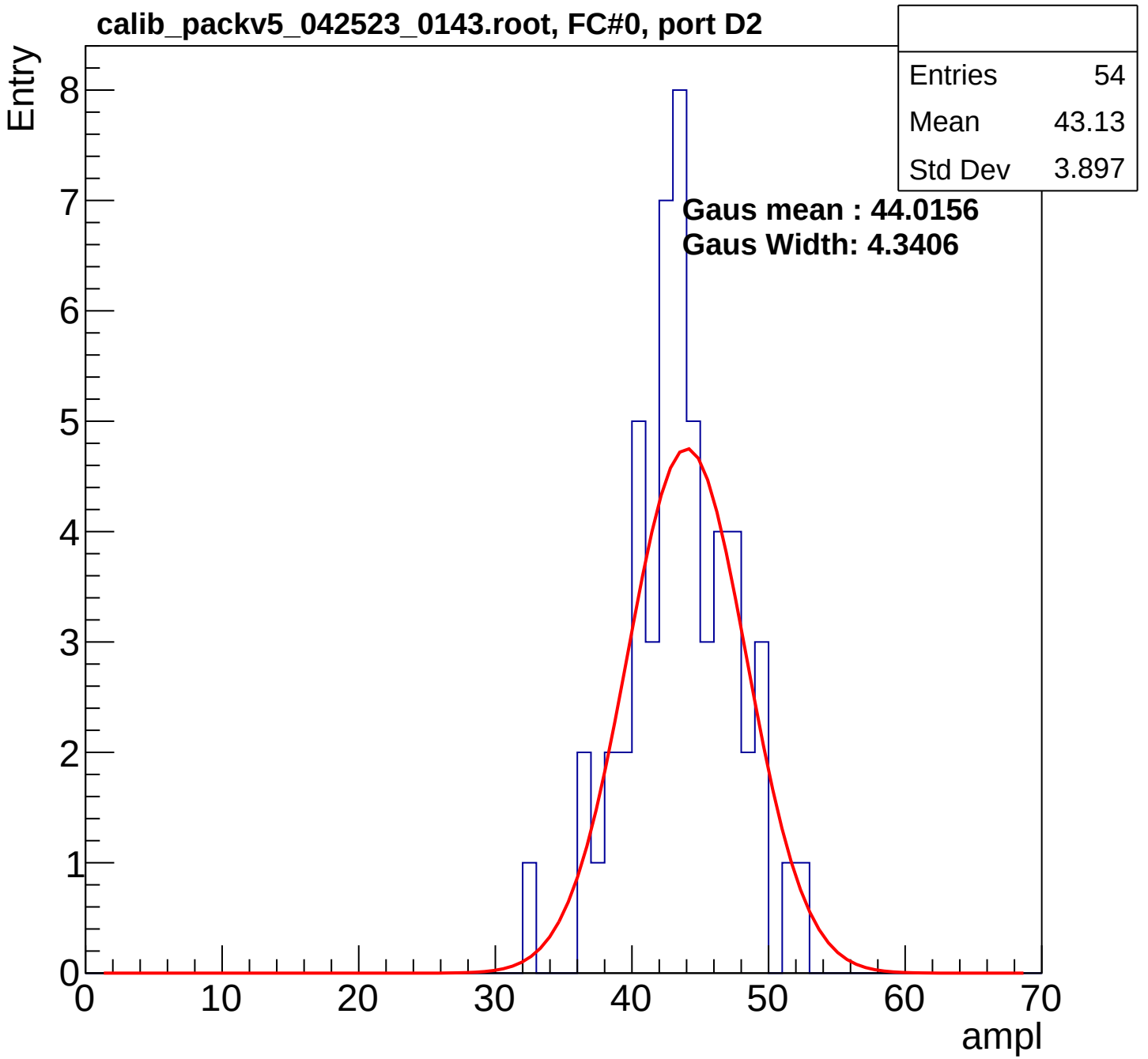

B1L101S, U2-ch119, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 37
Mean 59.95
Std Dev 2.143
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

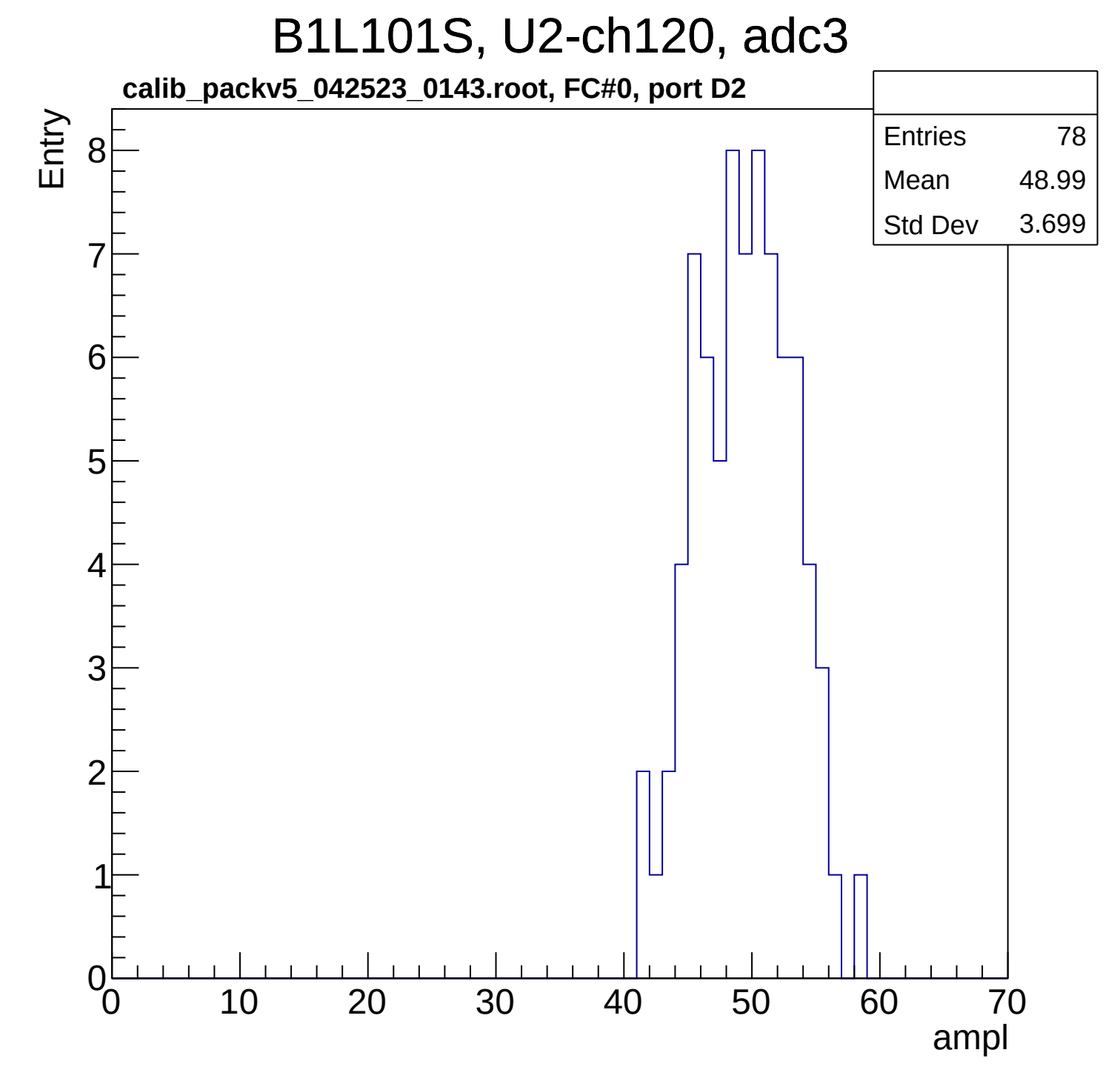

B1L101S, U2-ch119, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 61.5
Std Dev 1.118
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

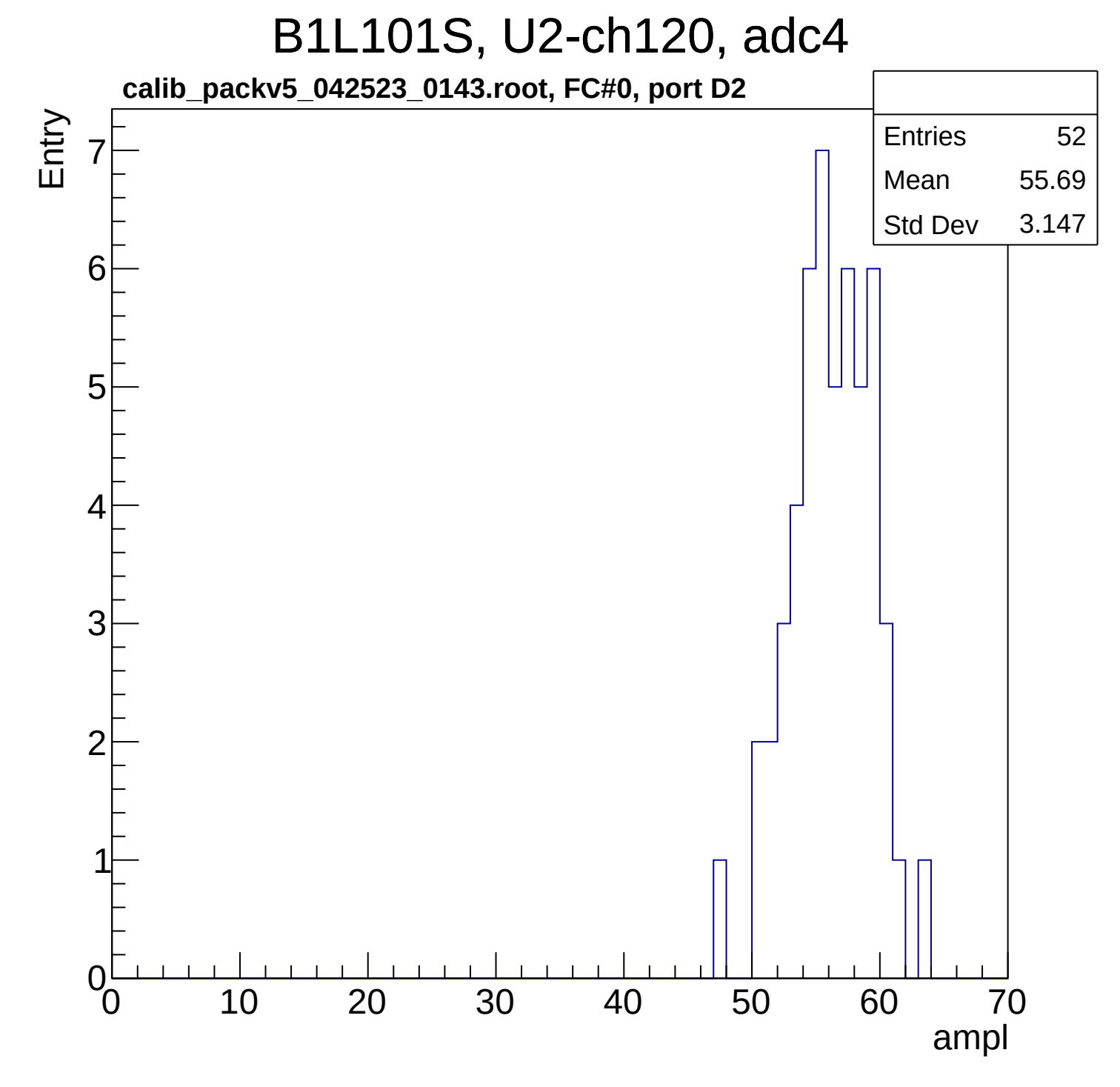

B1L101S, U2-ch119, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

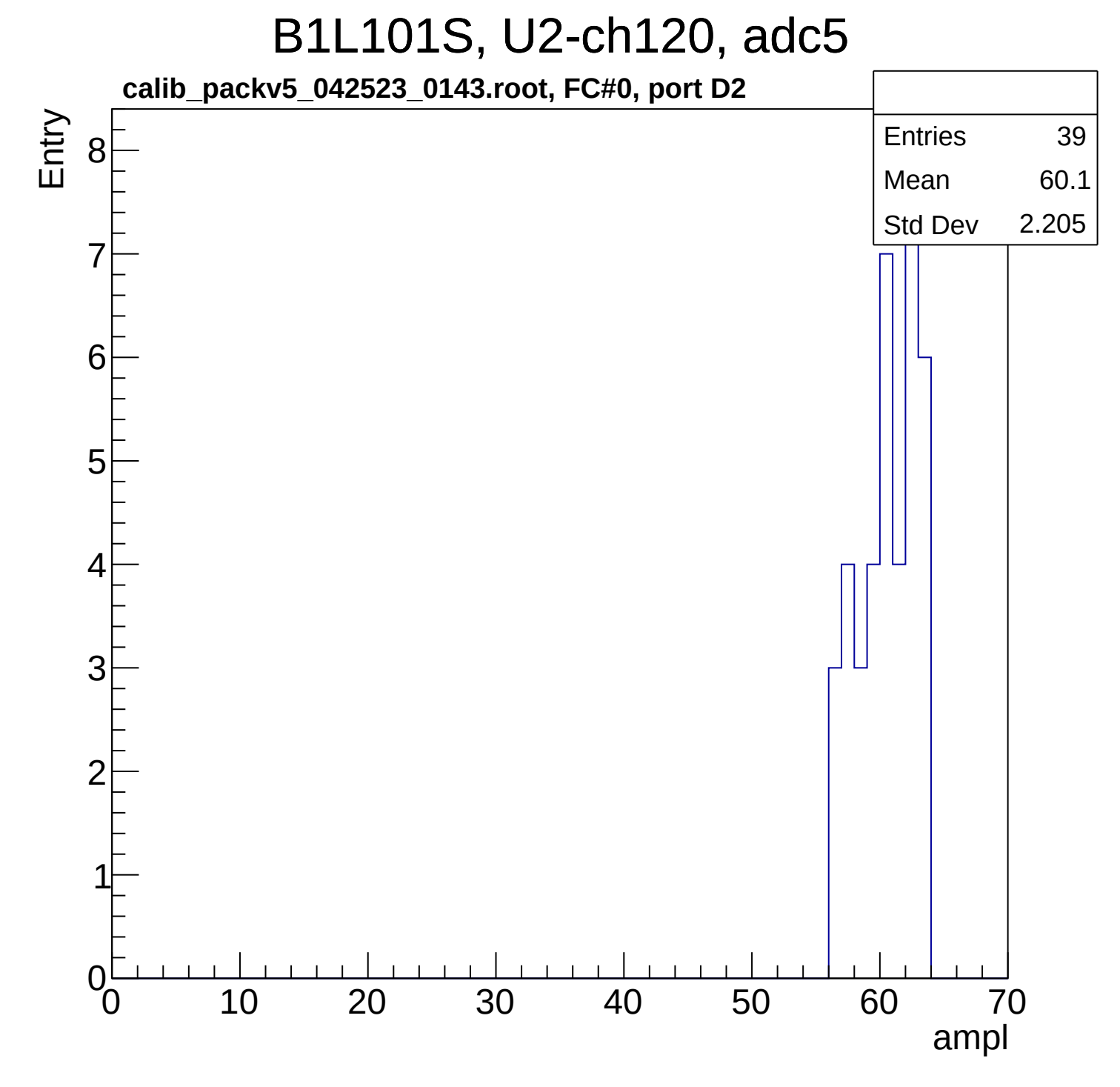

B1L101S, U2-ch120, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 28.67
Std Dev 5.041
Gaus mean : 29.1619
Gaus Width: 4.1125
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

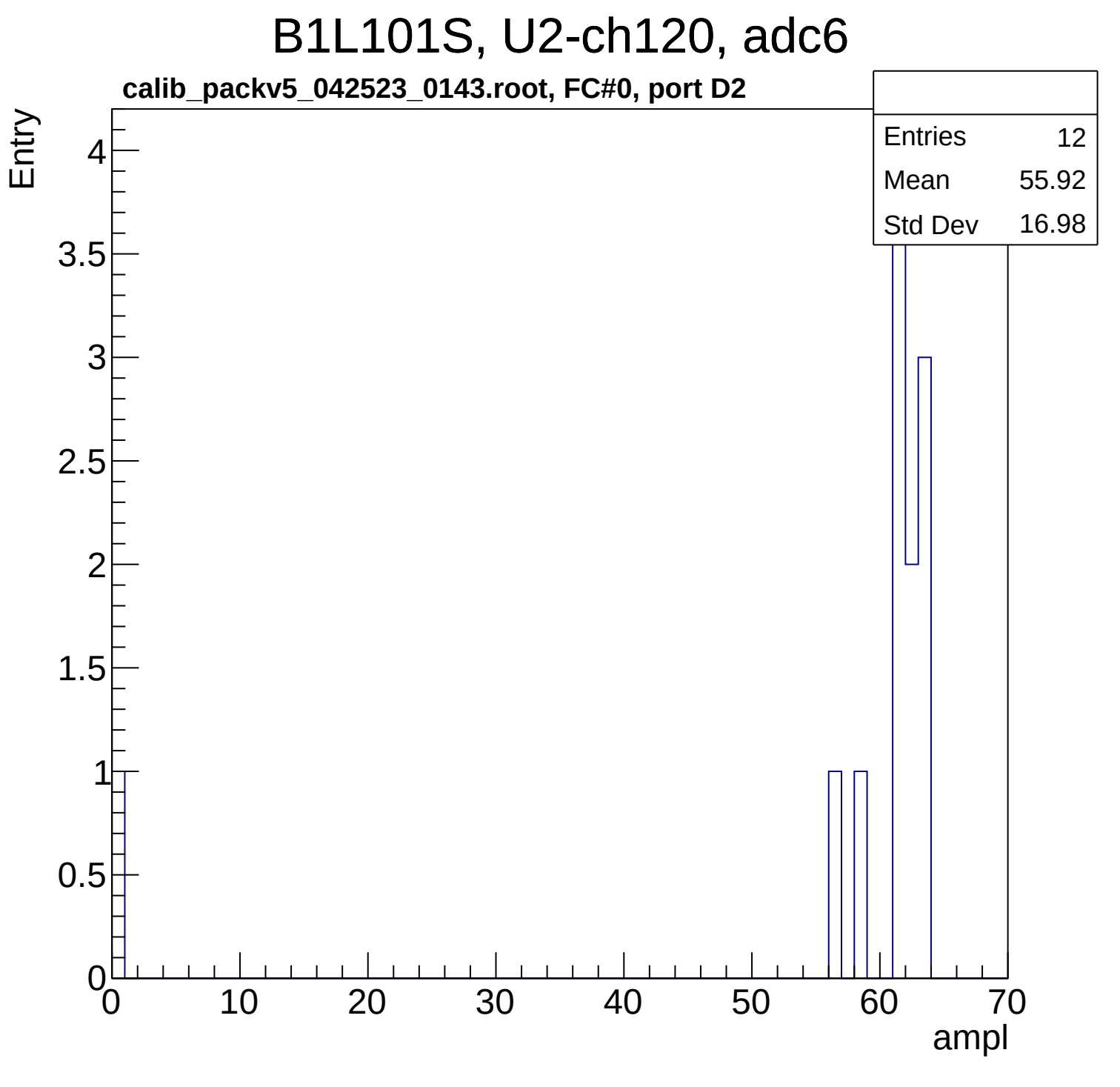

B1L101S, U2-ch120, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 36.16
Std Dev 3.216
Gaus mean : 36.8325
Gaus Width: 3.5497
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

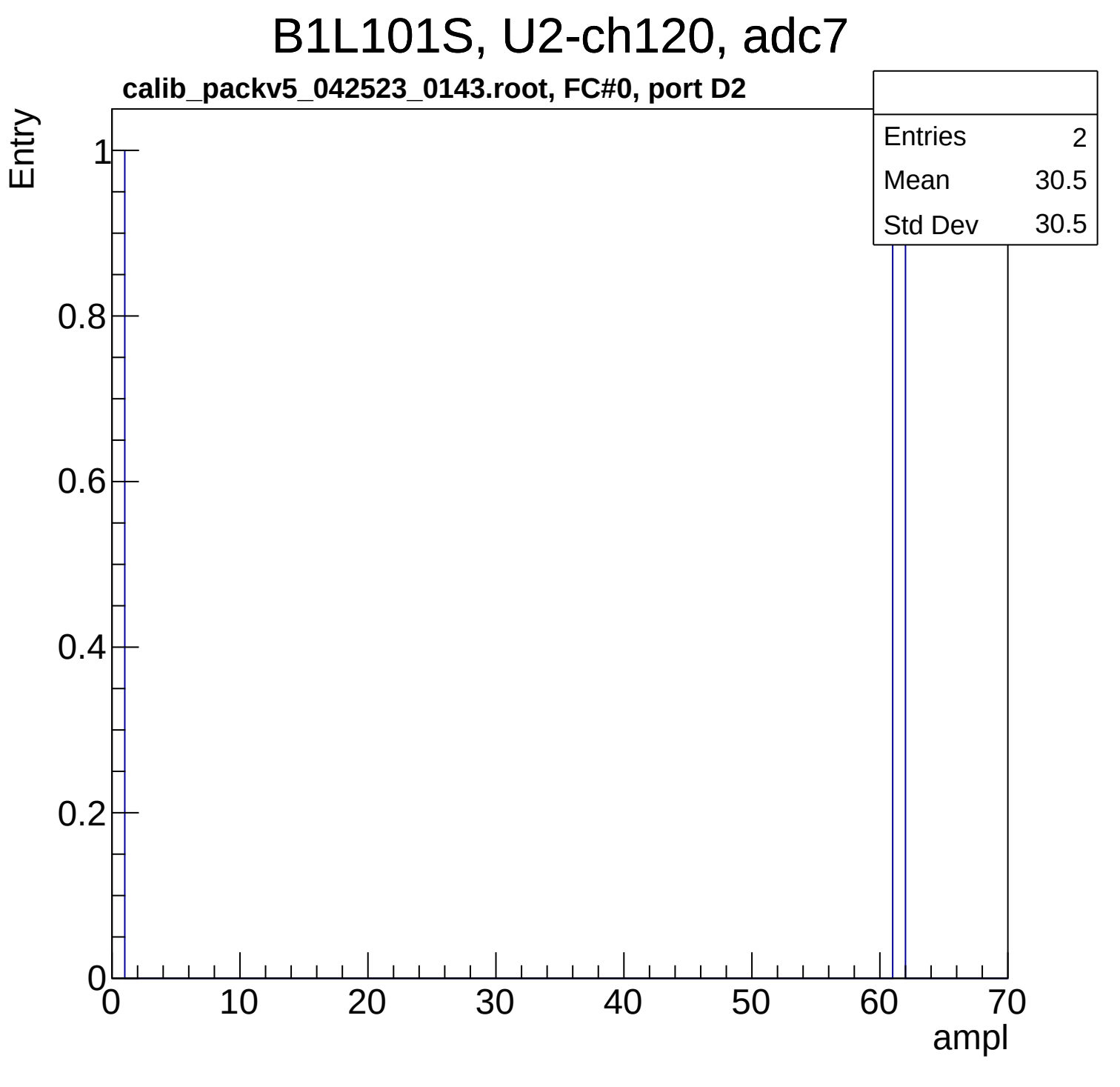

B1L101S, U2-ch120, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 43.13
Std Dev 3.897
Gaus mean : 44.0156
Gaus Width: 4.3406
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

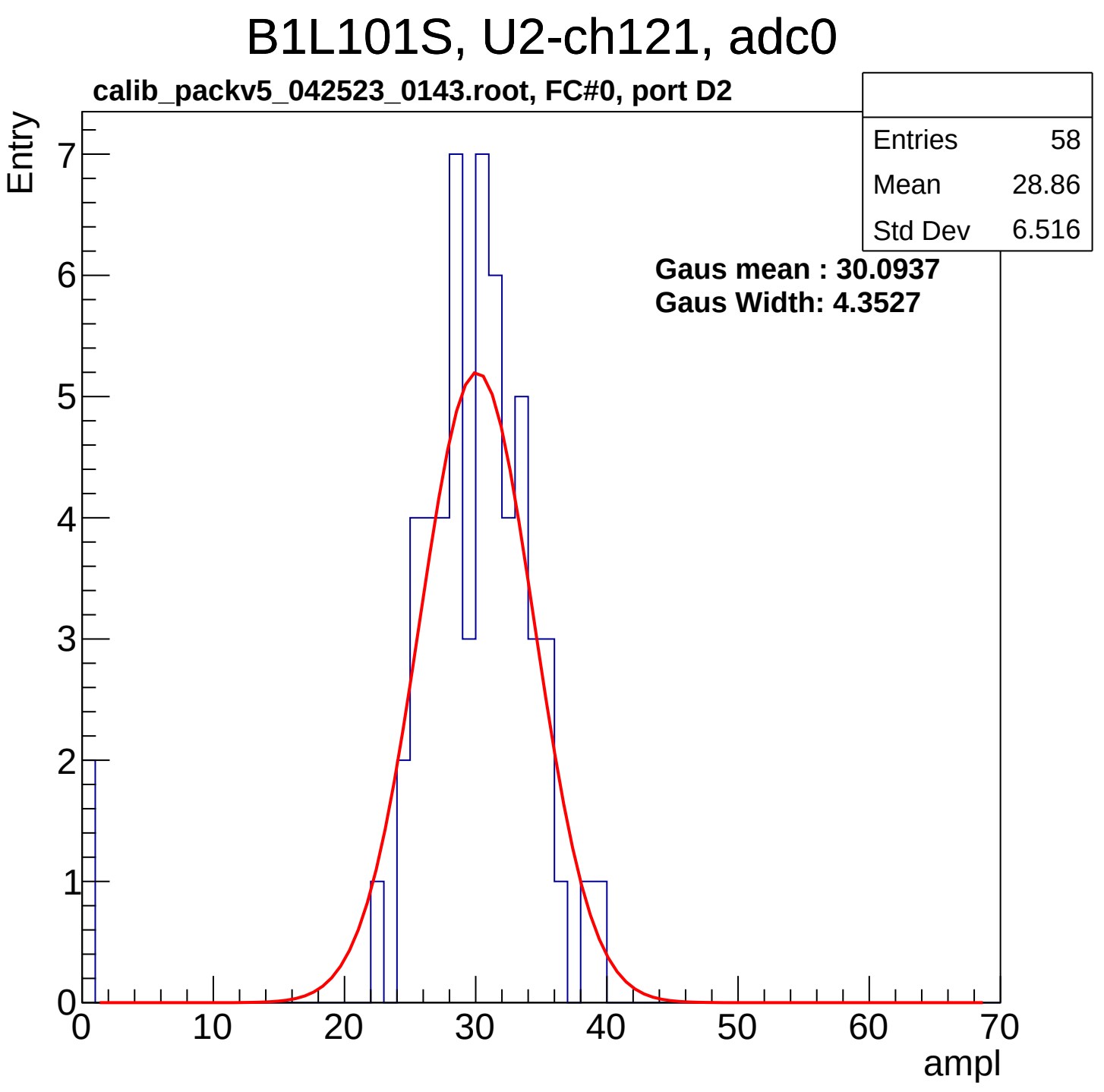

B1L101S, U2-ch120, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 48.99
Std Dev 3.699
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

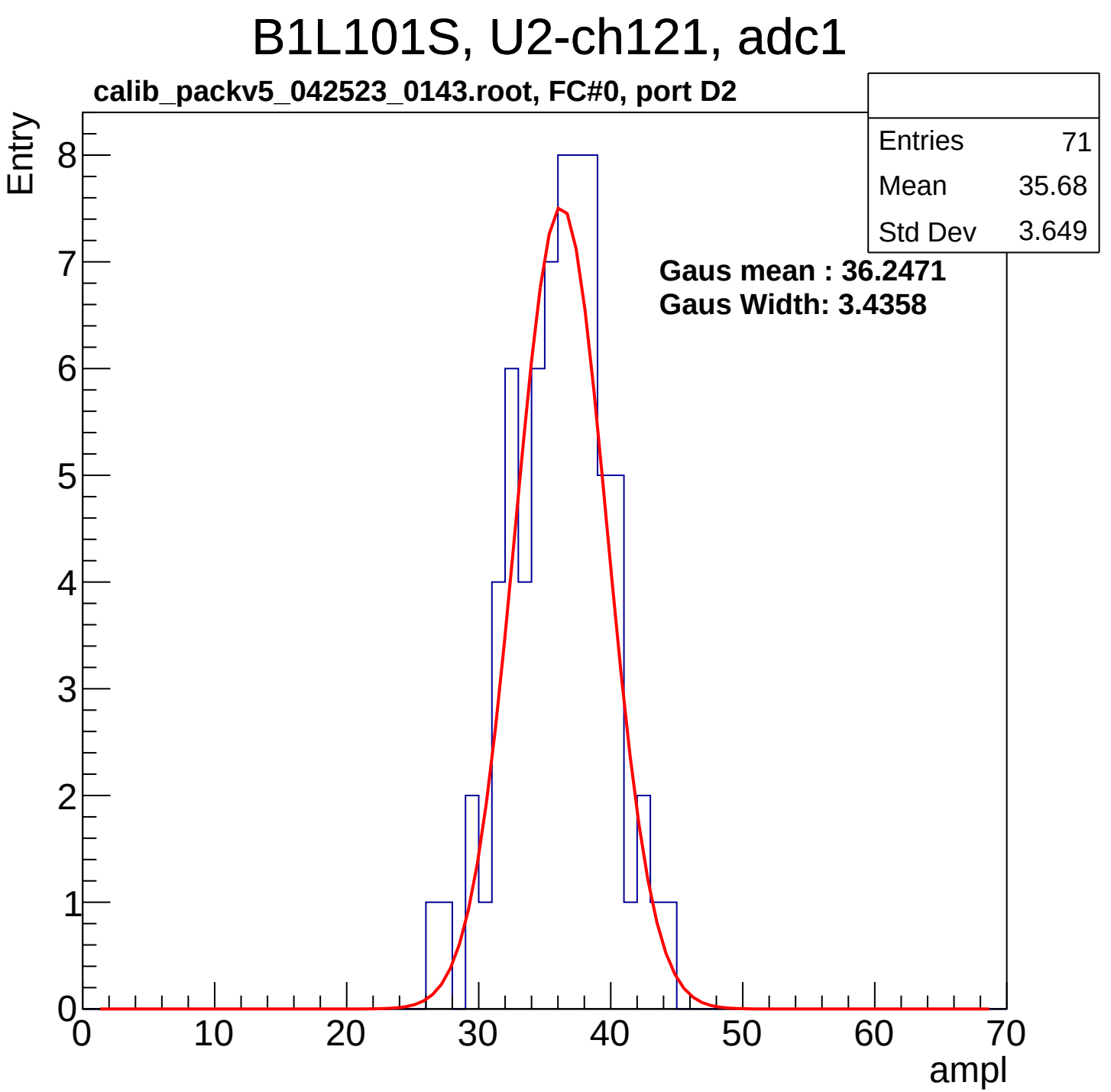

B1L101S, U2-ch120, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 52
Mean 55.69
Std Dev 3.147
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

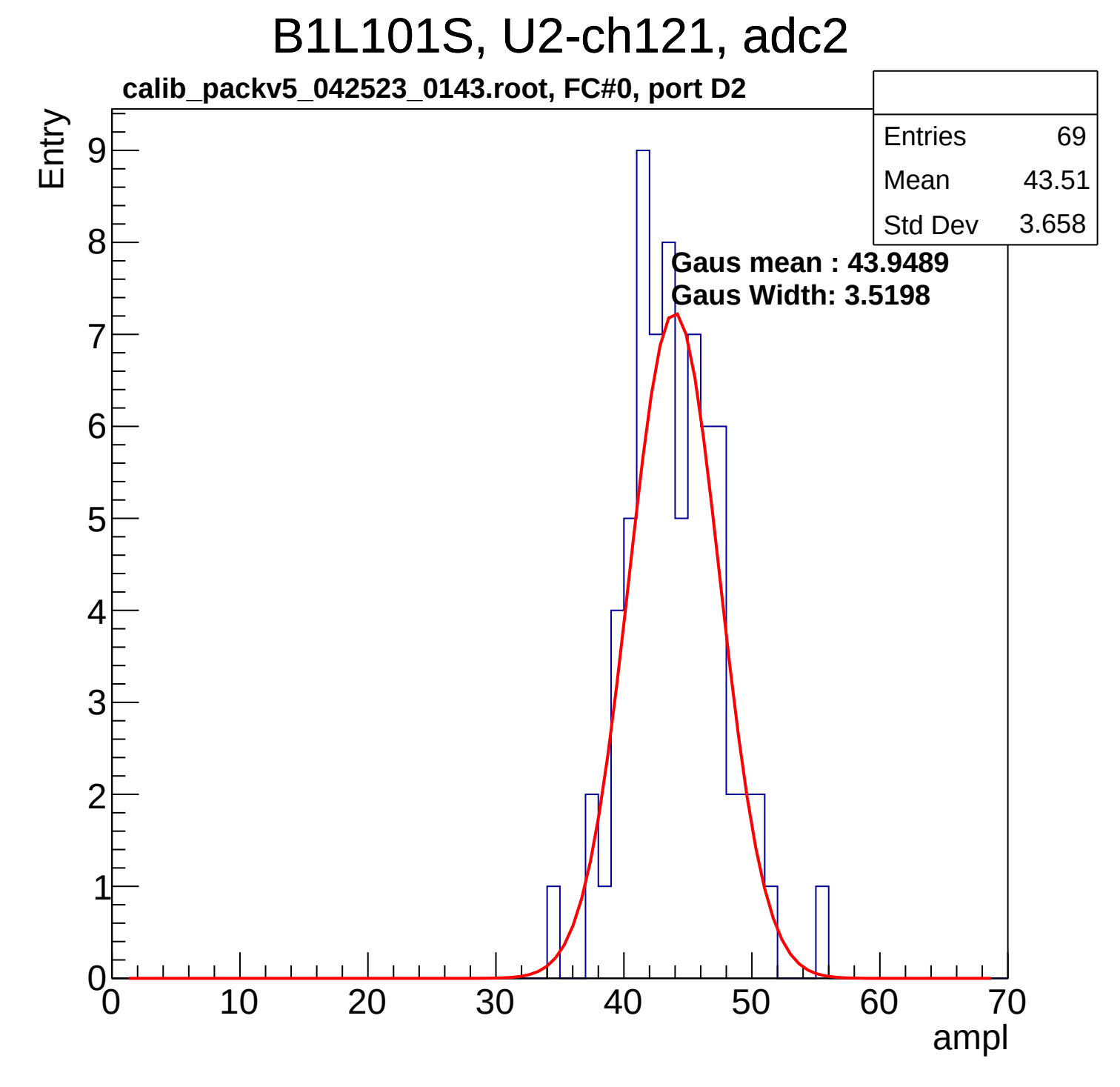

B1L101S, U2-ch120, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 39
Mean 60.1
Std Dev 2.205
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

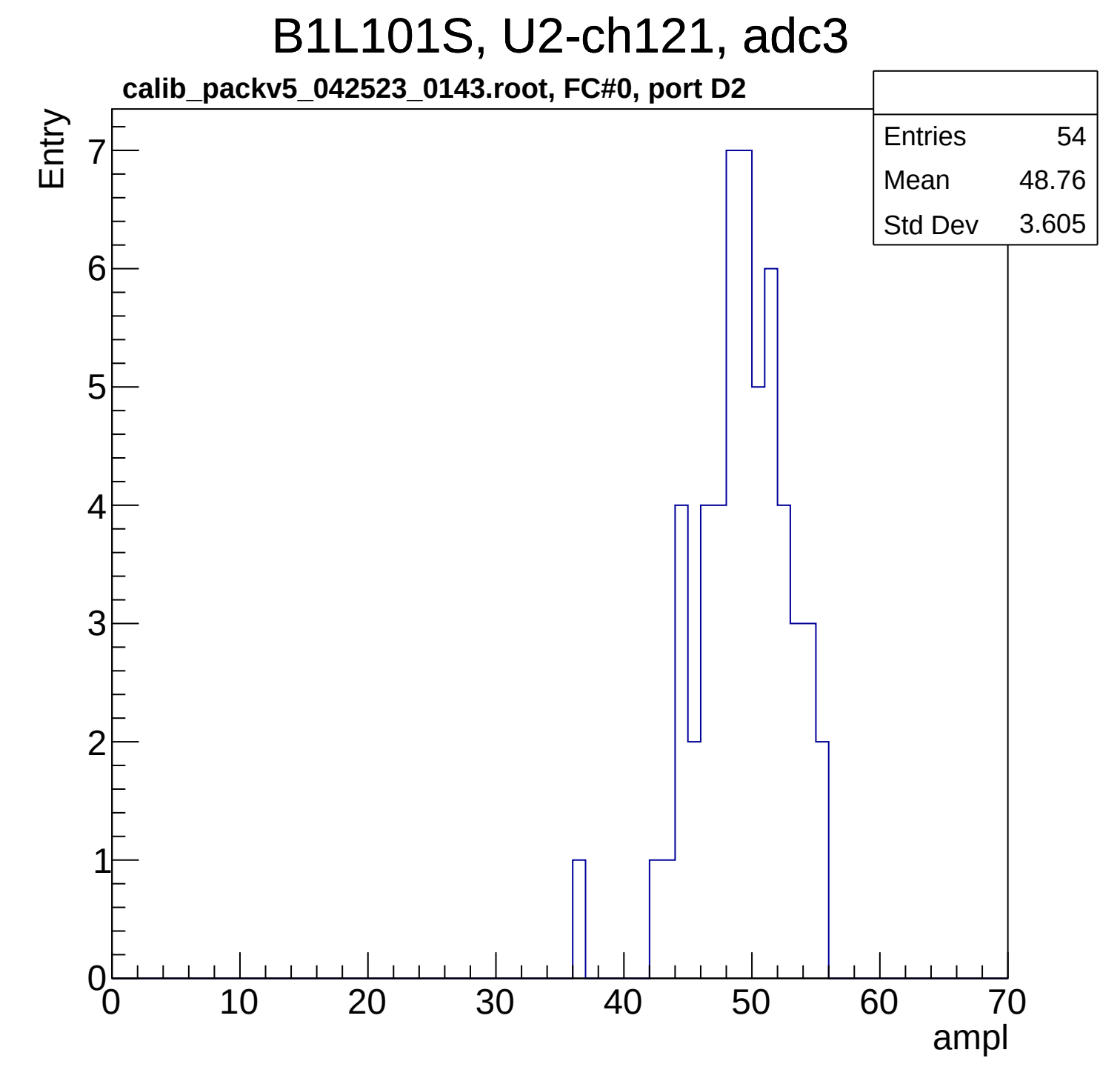

B1L101S, U2-ch120, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 12
Mean 55.92
Std Dev 16.98
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

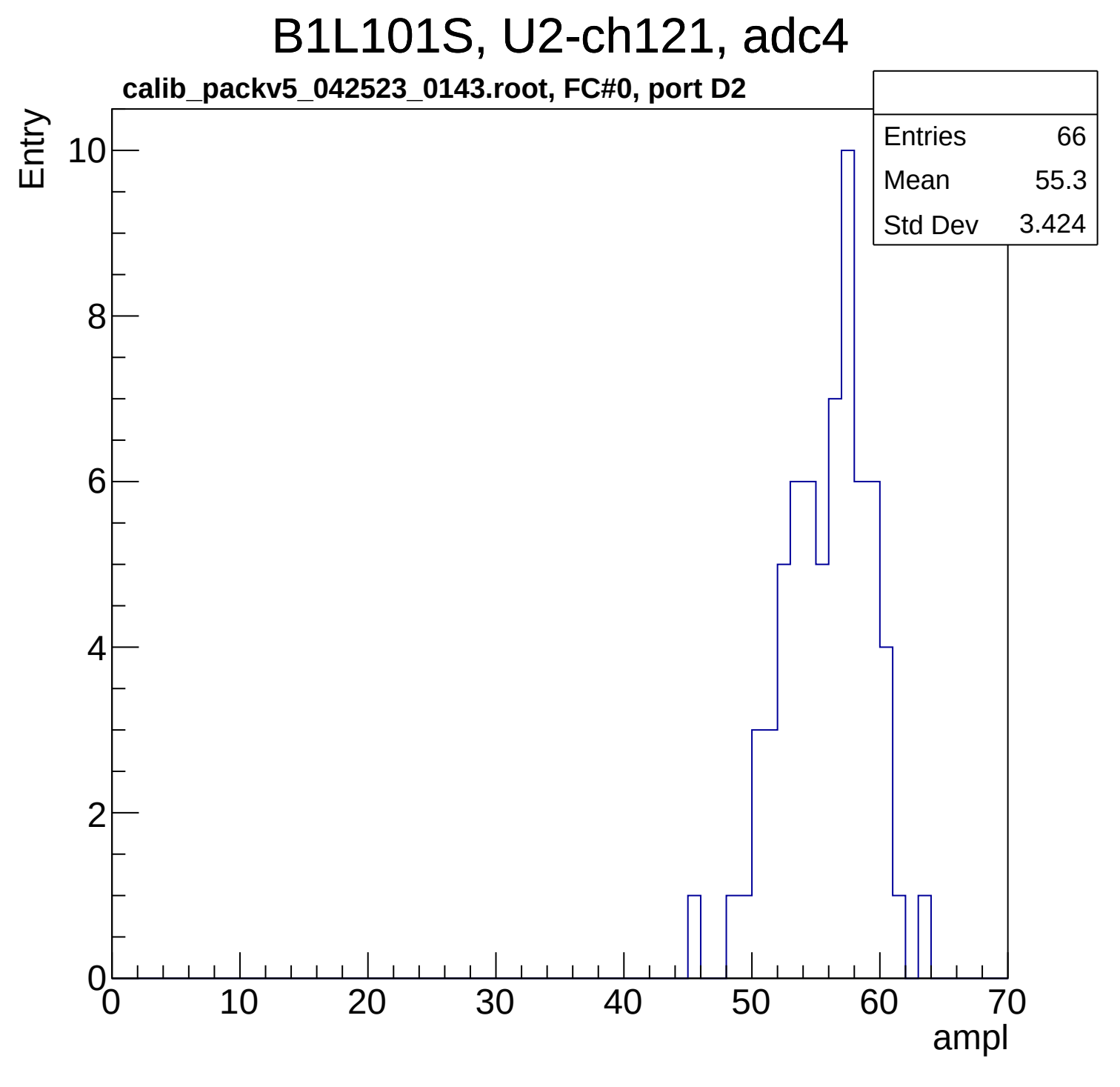

B1L101S, U2-ch120, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 30.5
Std Dev 30.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

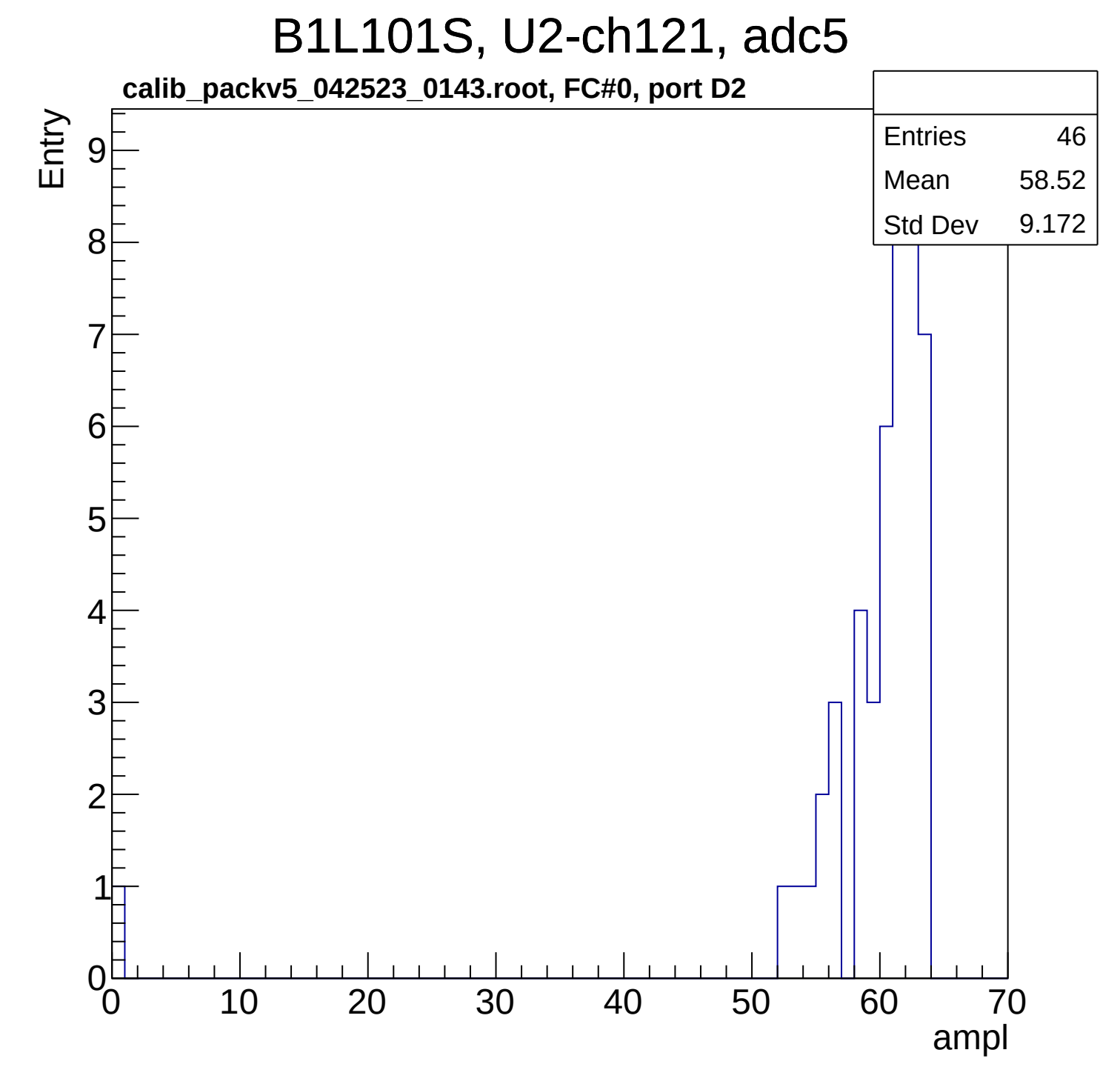

B1L101S, U2-ch121, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 28.86
Std Dev 6.516
Gaus mean : 30.0937
Gaus Width: 4.3527
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

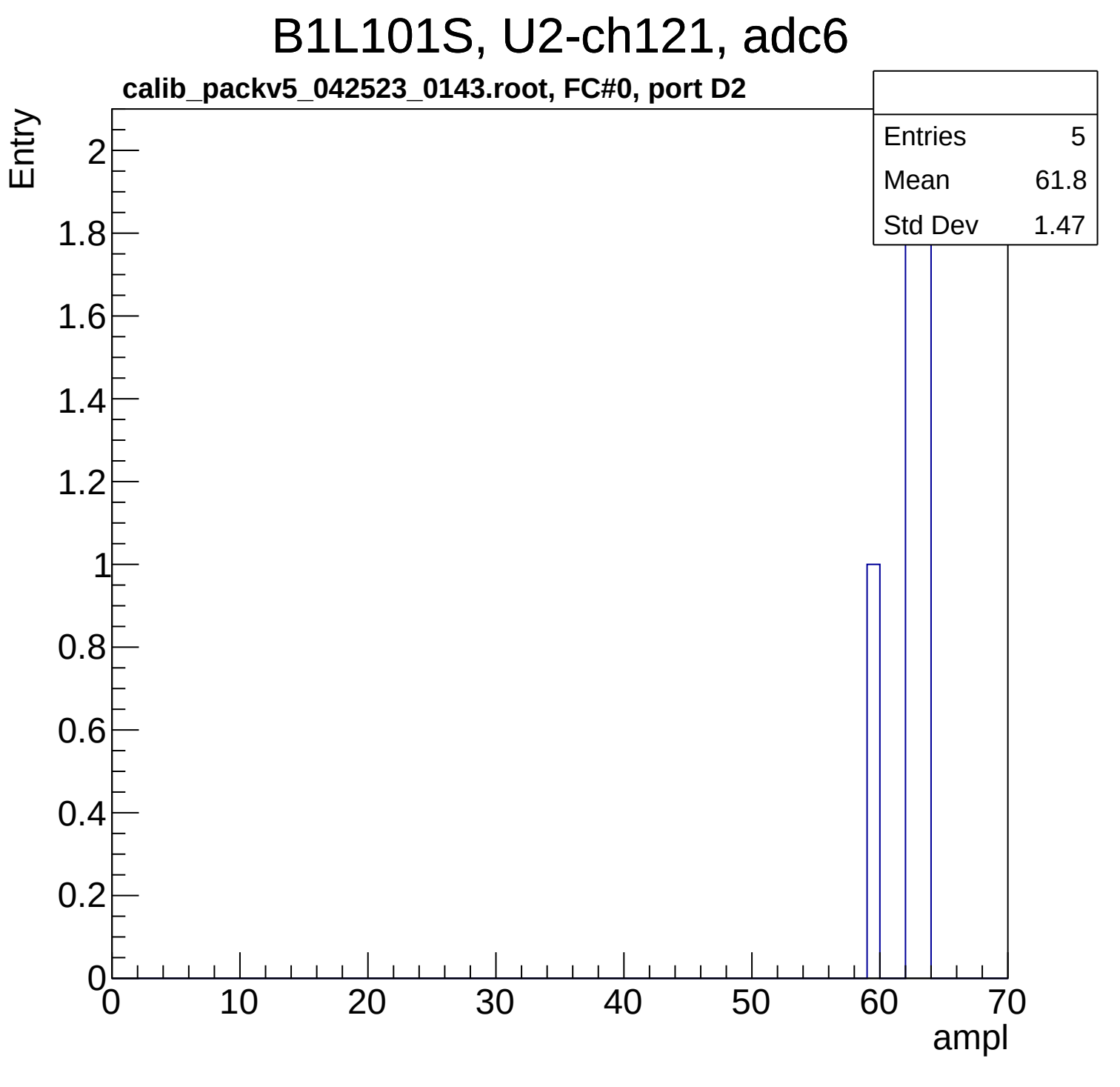

B1L101S, U2-ch121, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 35.68
Std Dev 3.649
Gaus mean : 36.2471
Gaus Width: 3.4358
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

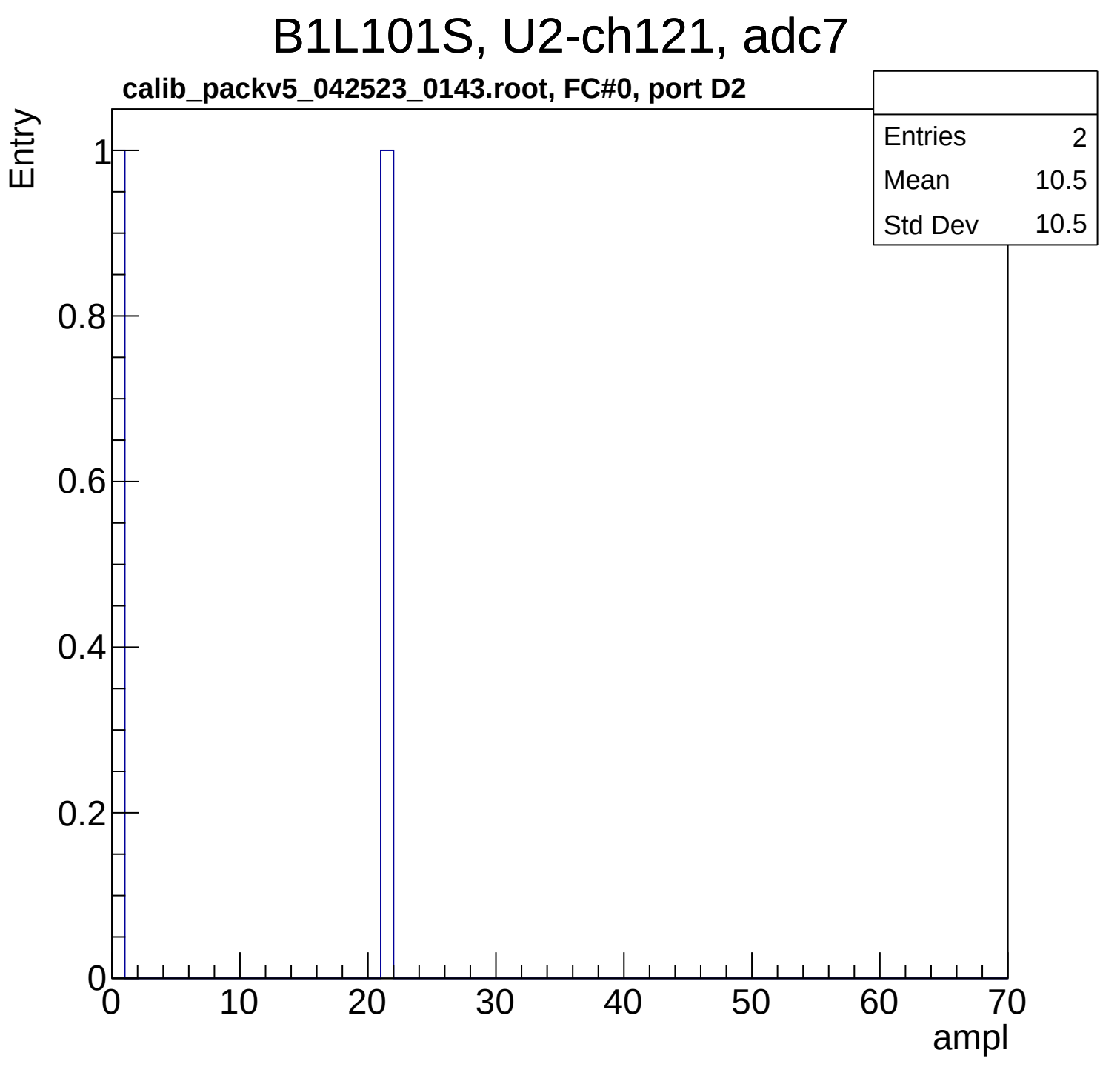

B1L101S, U2-ch121, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 43.51
Std Dev 3.658
Gaus mean : 43.9489
Gaus Width: 3.5198
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

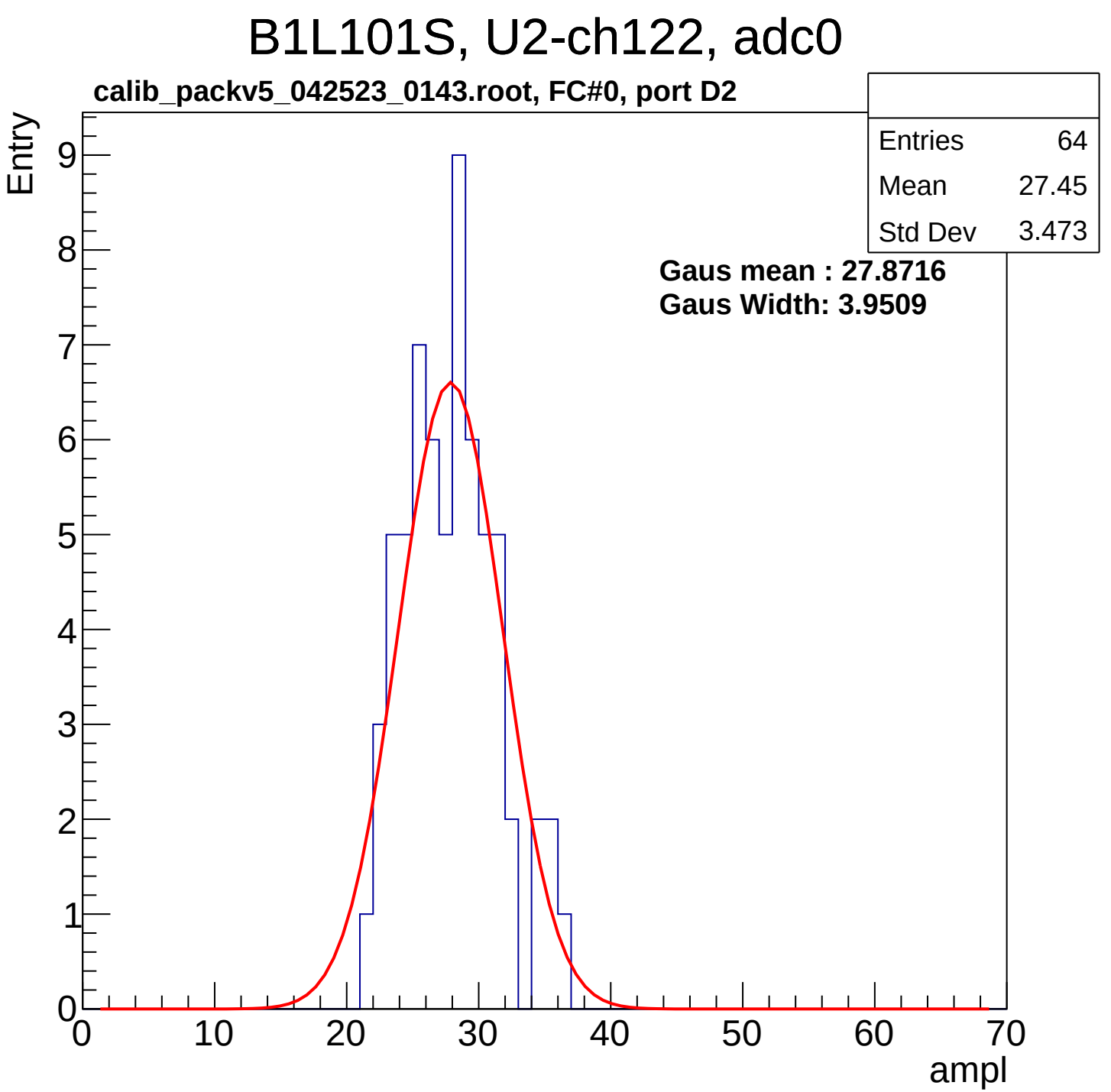

B1L101S, U2-ch121, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 54
Mean 48.76
Std Dev 3.605
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

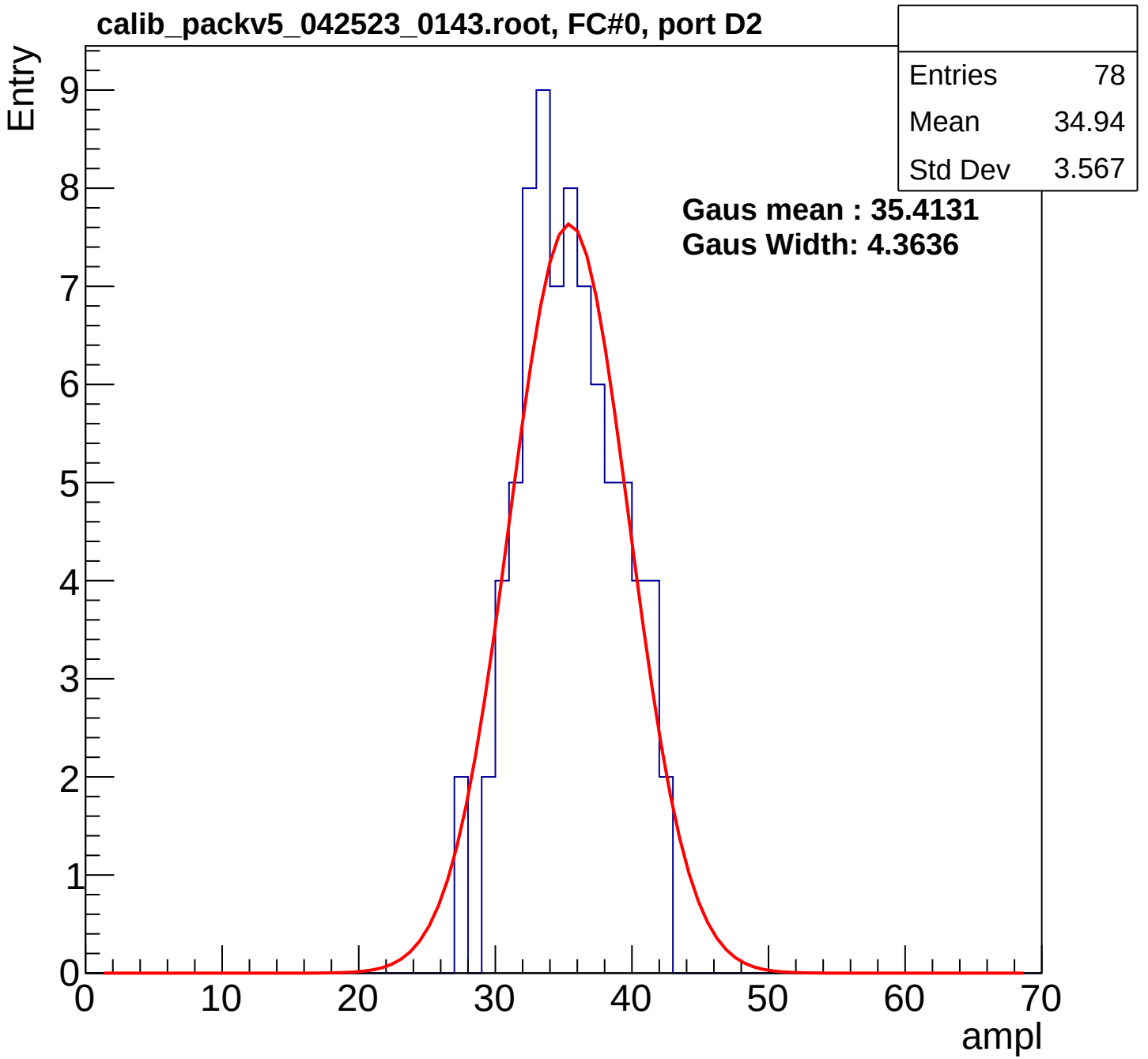

B1L101S, U2-ch121, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 55.3
Std Dev 3.424
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

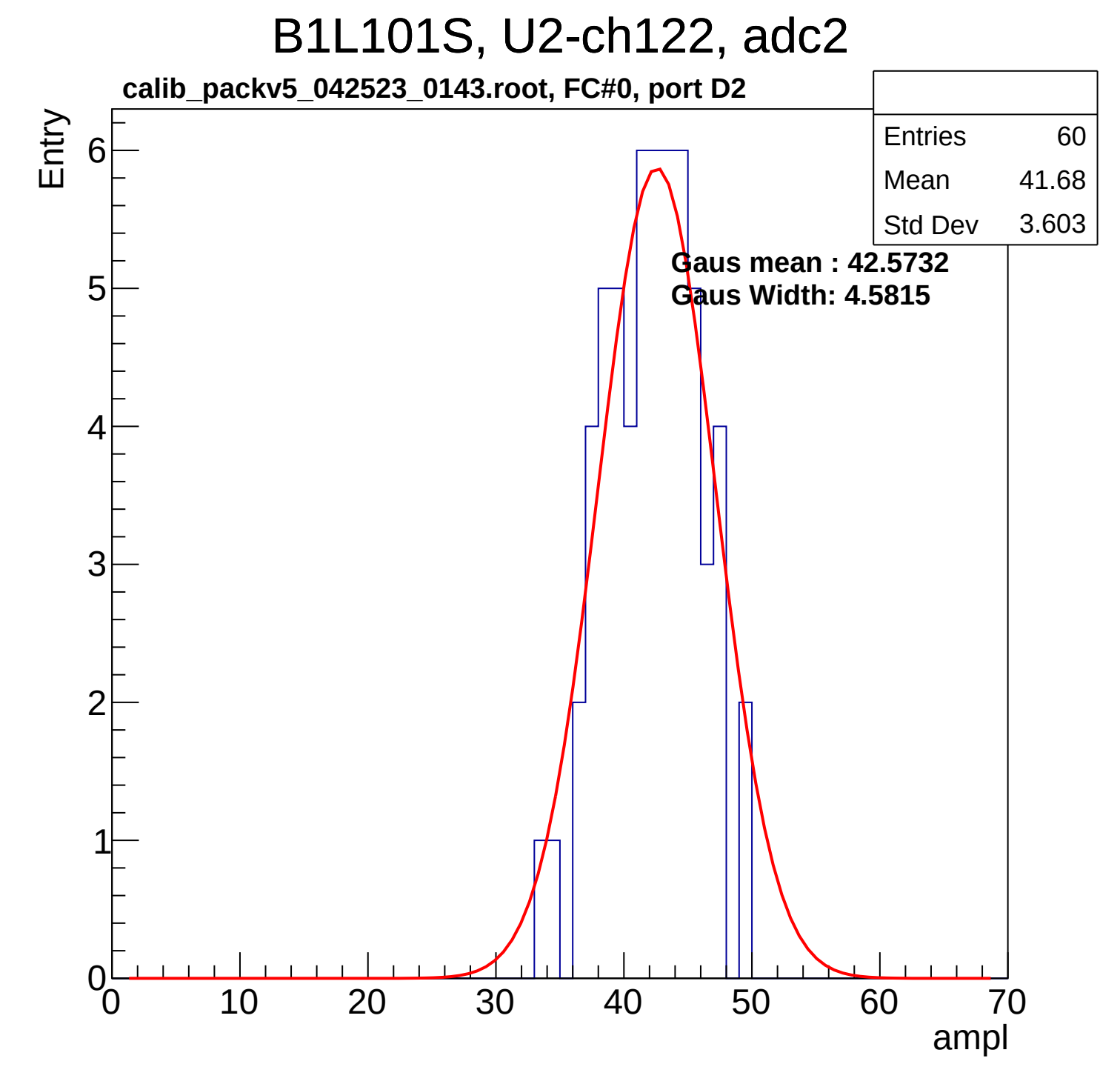

B1L101S, U2-ch121, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 58.52
Std Dev 9.172
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

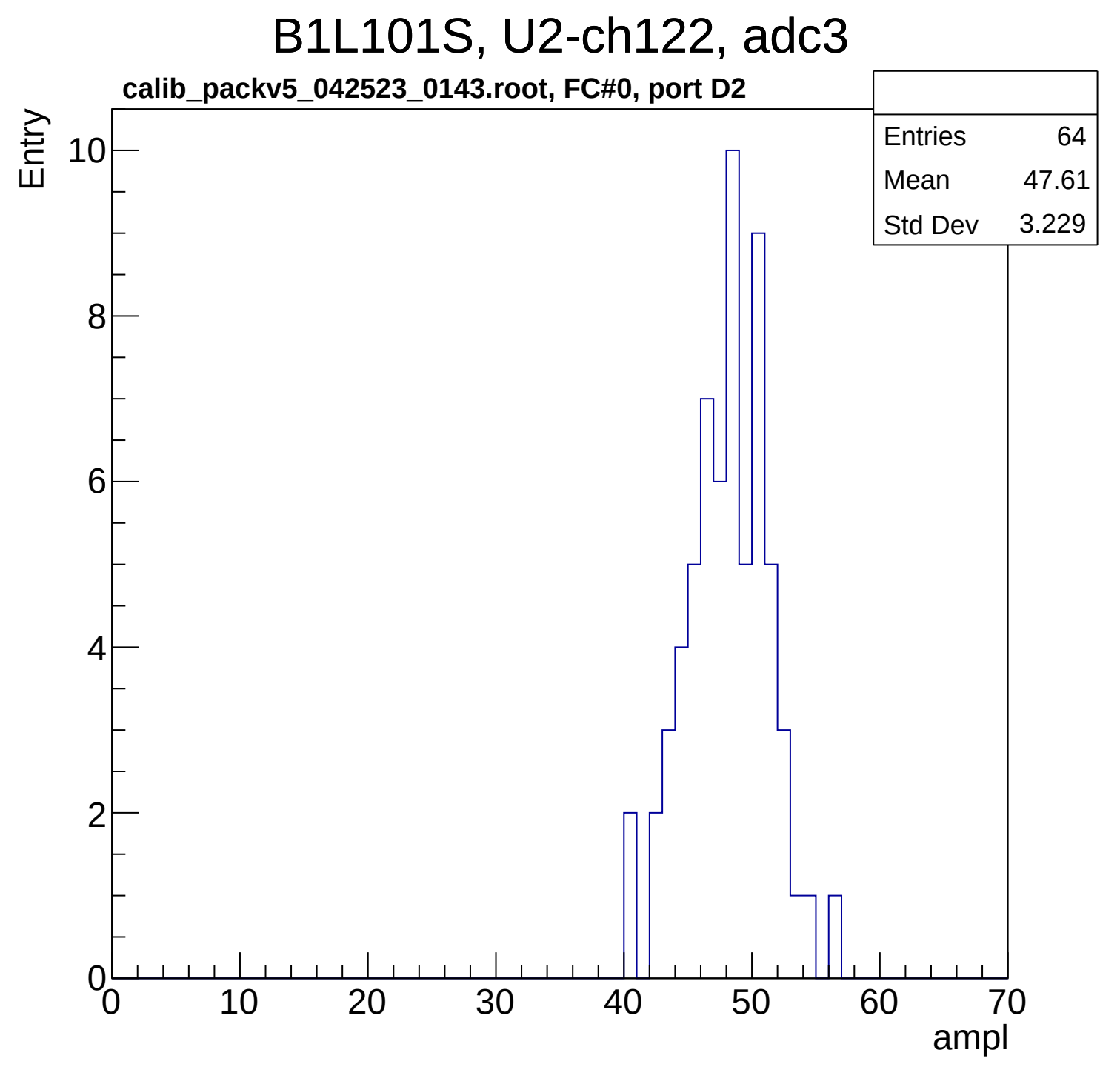

B1L101S, U2-ch121, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 5
Mean 61.8
Std Dev 1.47
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

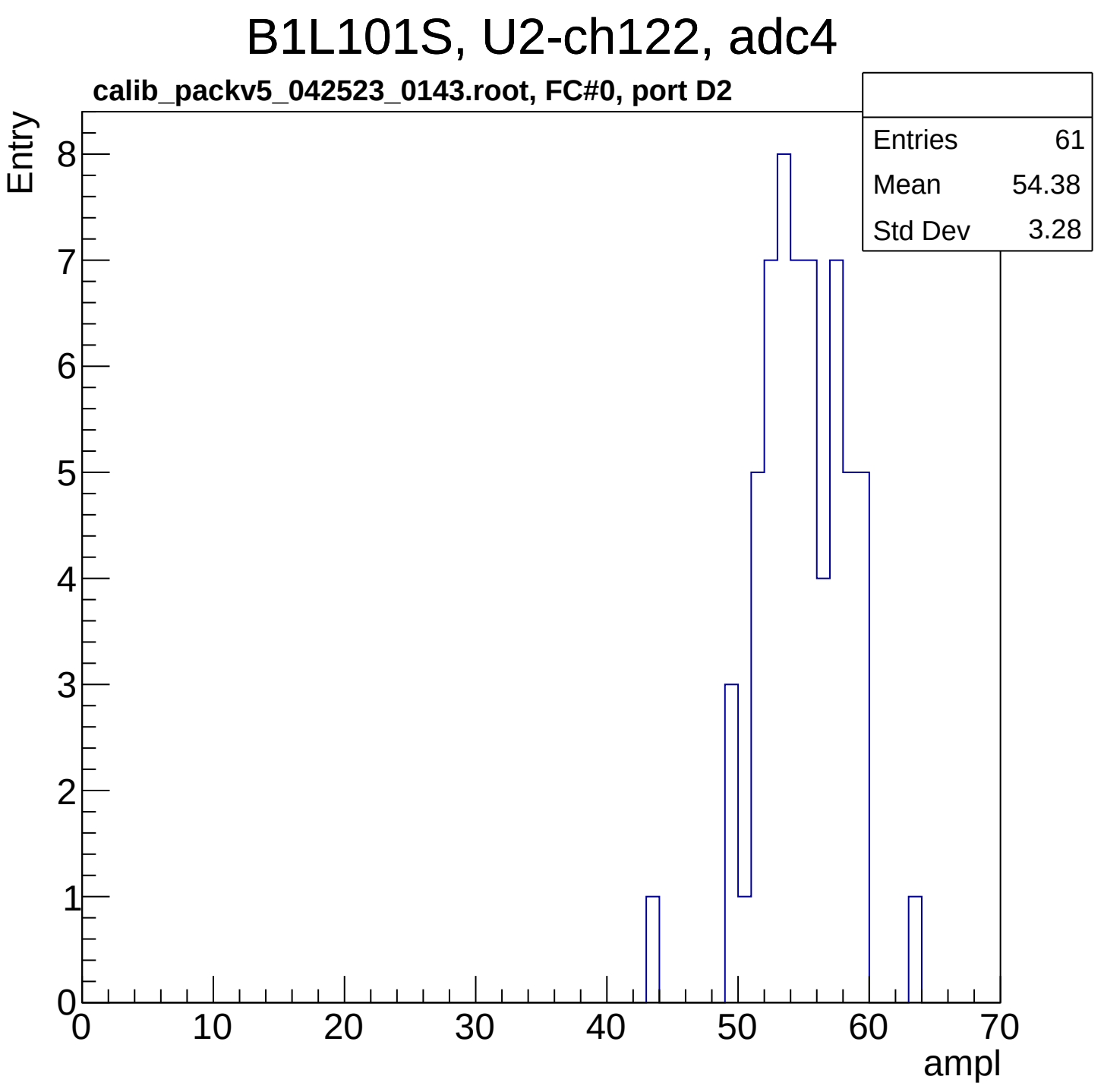

B1L101S, U2-ch121, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 10.5
Std Dev 10.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

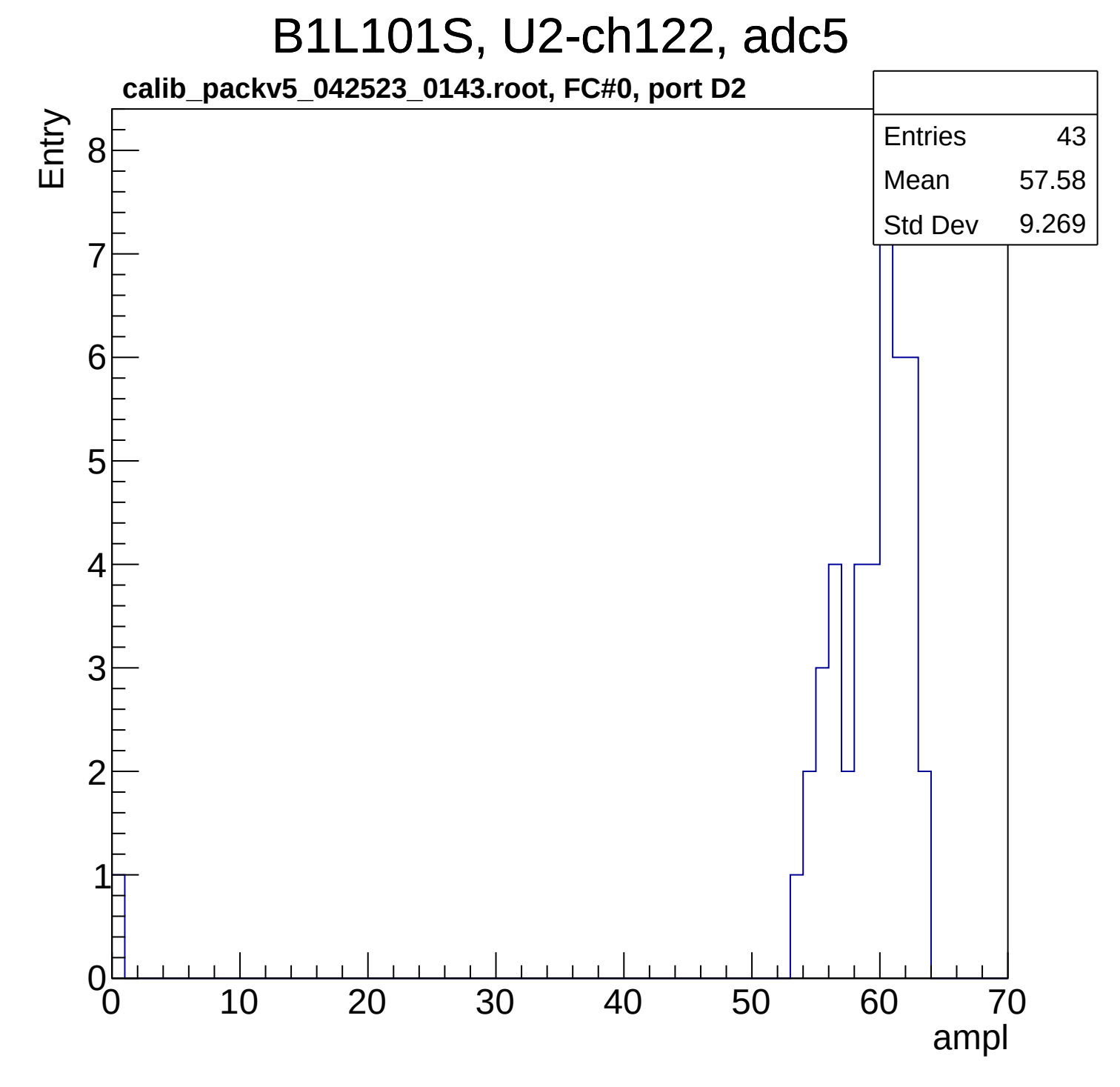

B1L101S, U2-ch122, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 27.45
Std Dev 3.473
Gaus mean : 27.8716
Gaus Width: 3.9509
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

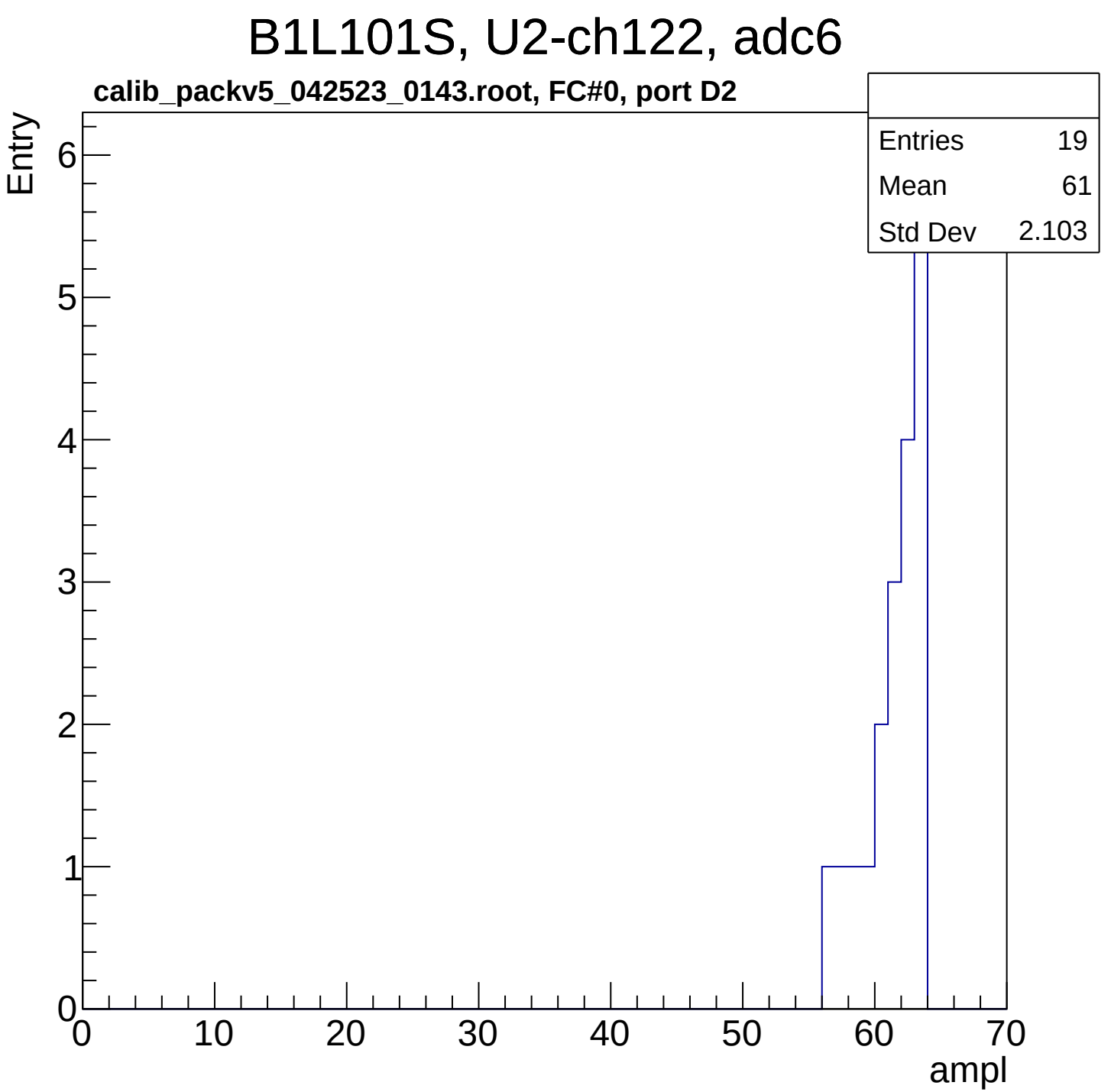

B1L101S, U2-ch122, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 78
Mean 34.94
Std Dev 3.567
Gaus mean : 35.4131
Gaus Width: 4.3636
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

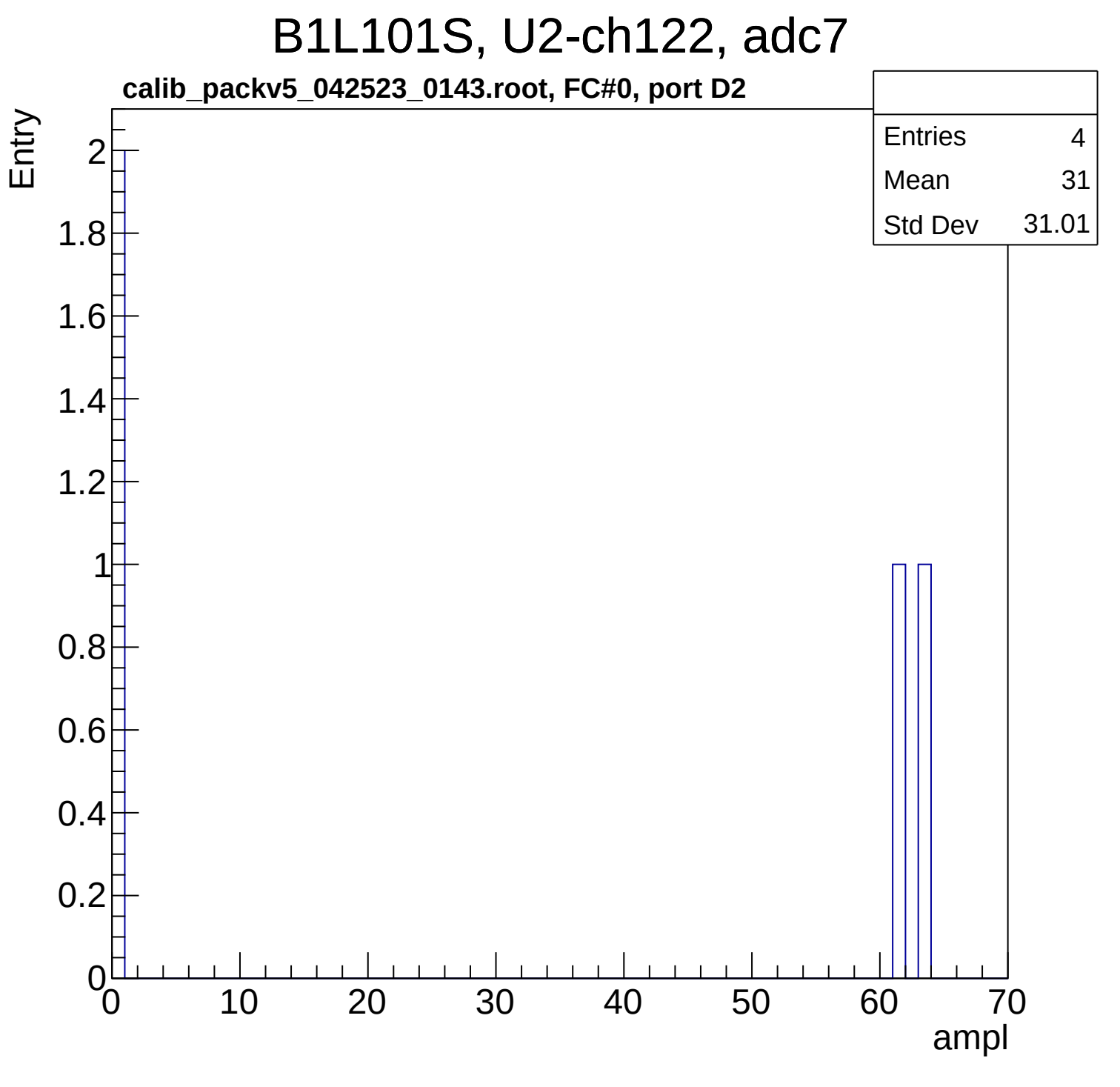

B1L101S, U2-ch122, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 41.68
Std Dev 3.603
Gaus mean : 42.5732
Gaus Width: 4.5815
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

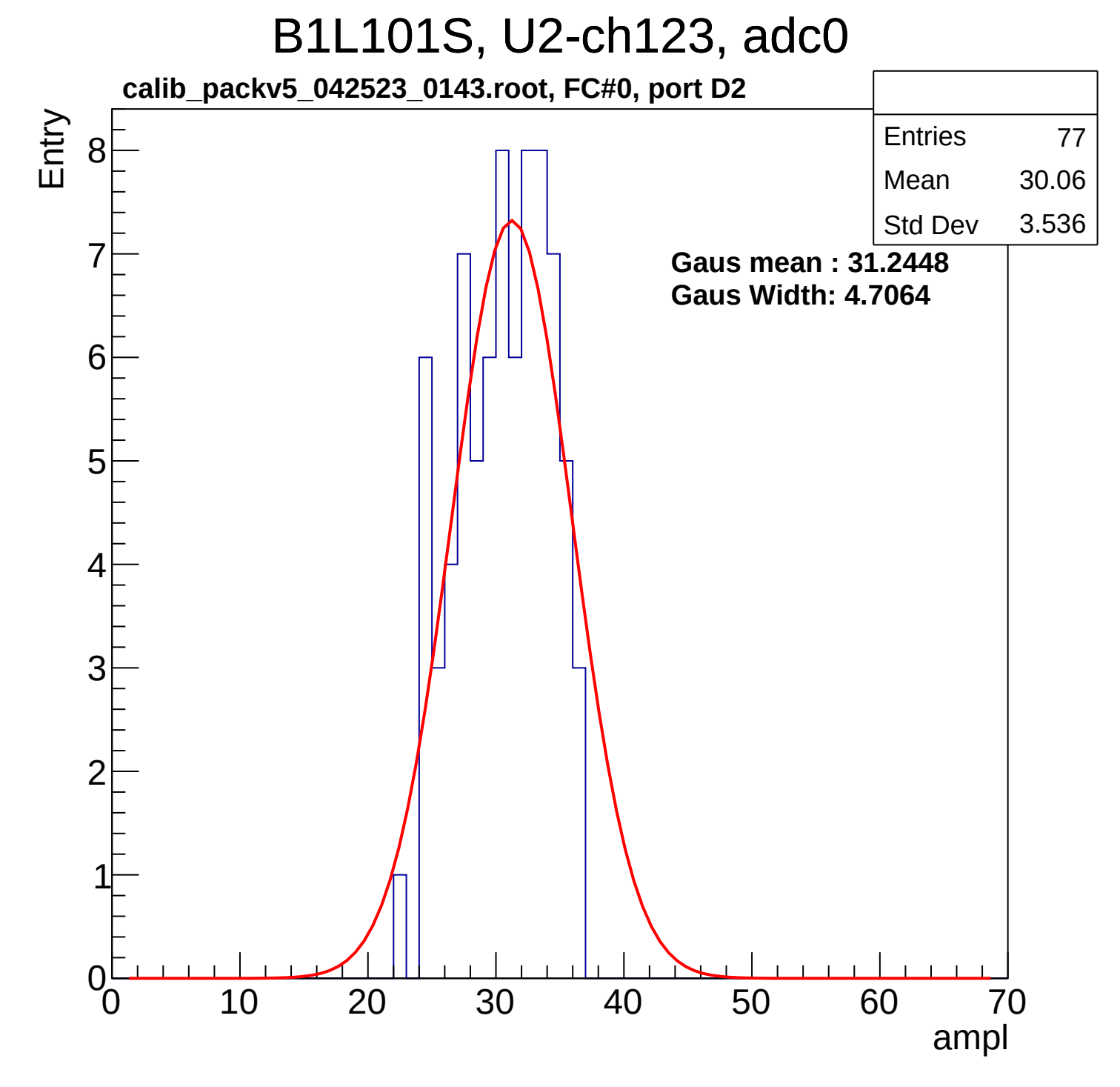

B1L101S, U2-ch122, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 64
Mean 47.61
Std Dev 3.229
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

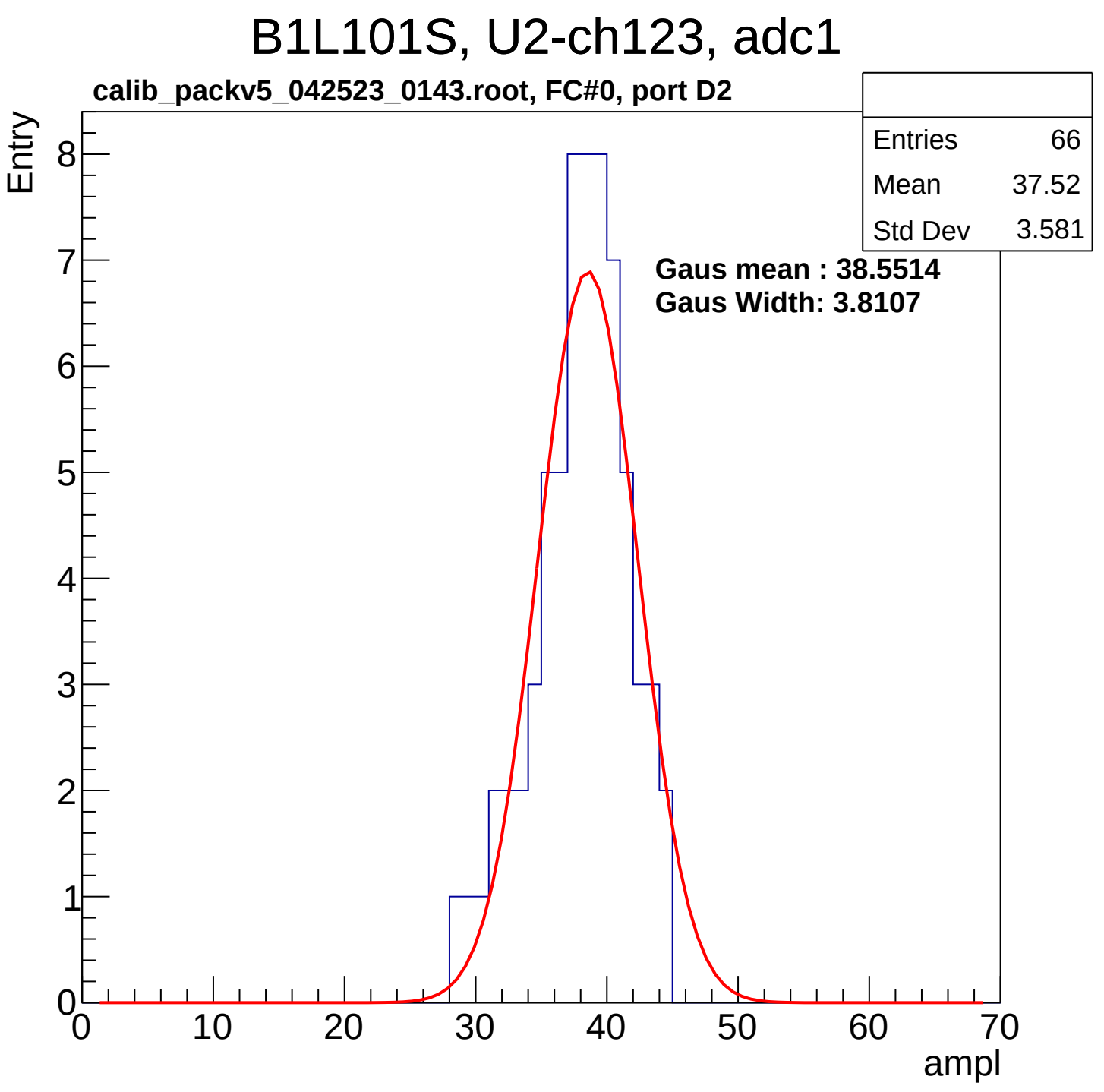

B1L101S, U2-ch122, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 61
Mean 54.38
Std Dev 3.28
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

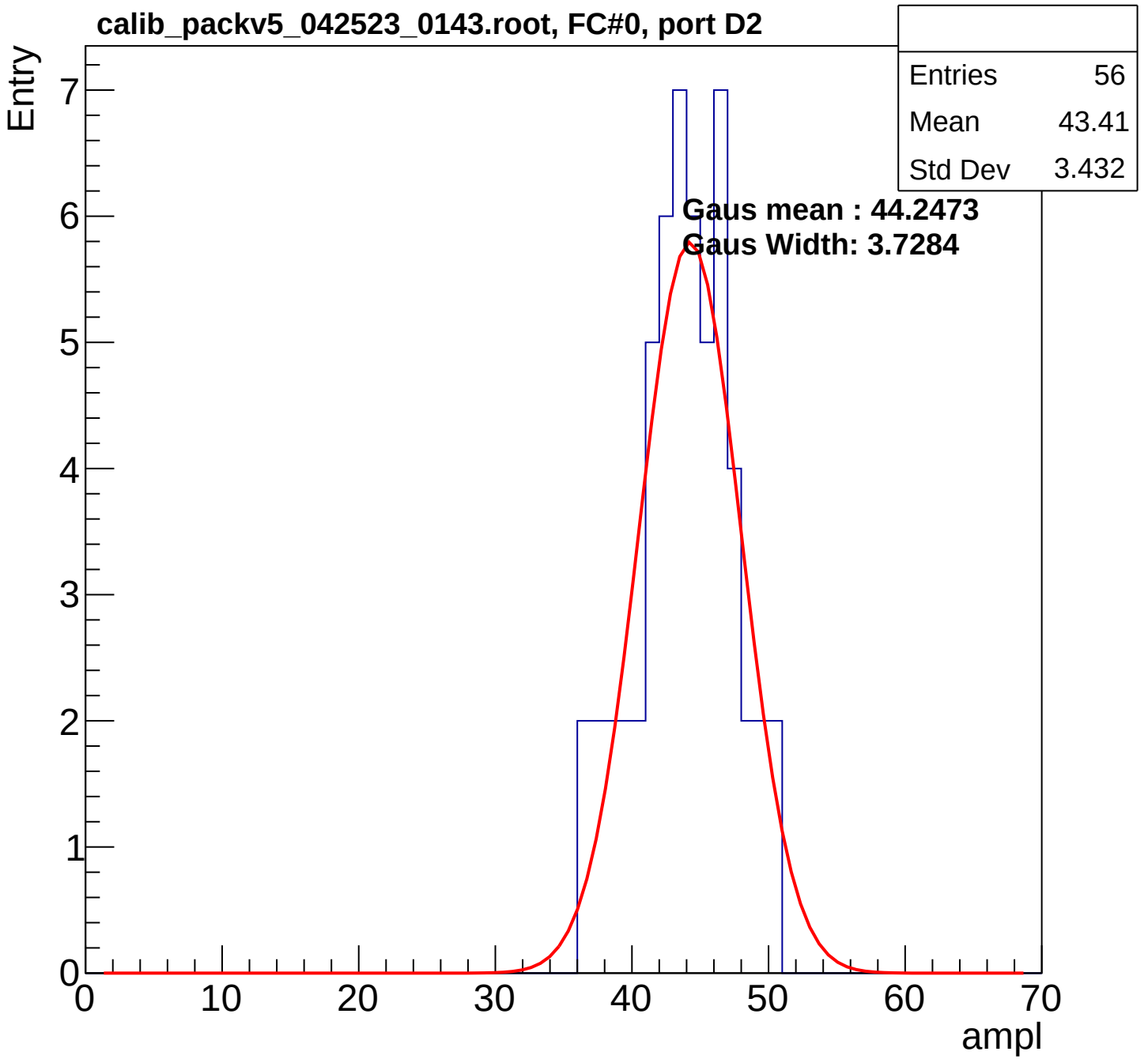

B1L101S, U2-ch122, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 43
Mean 57.58
Std Dev 9.269
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

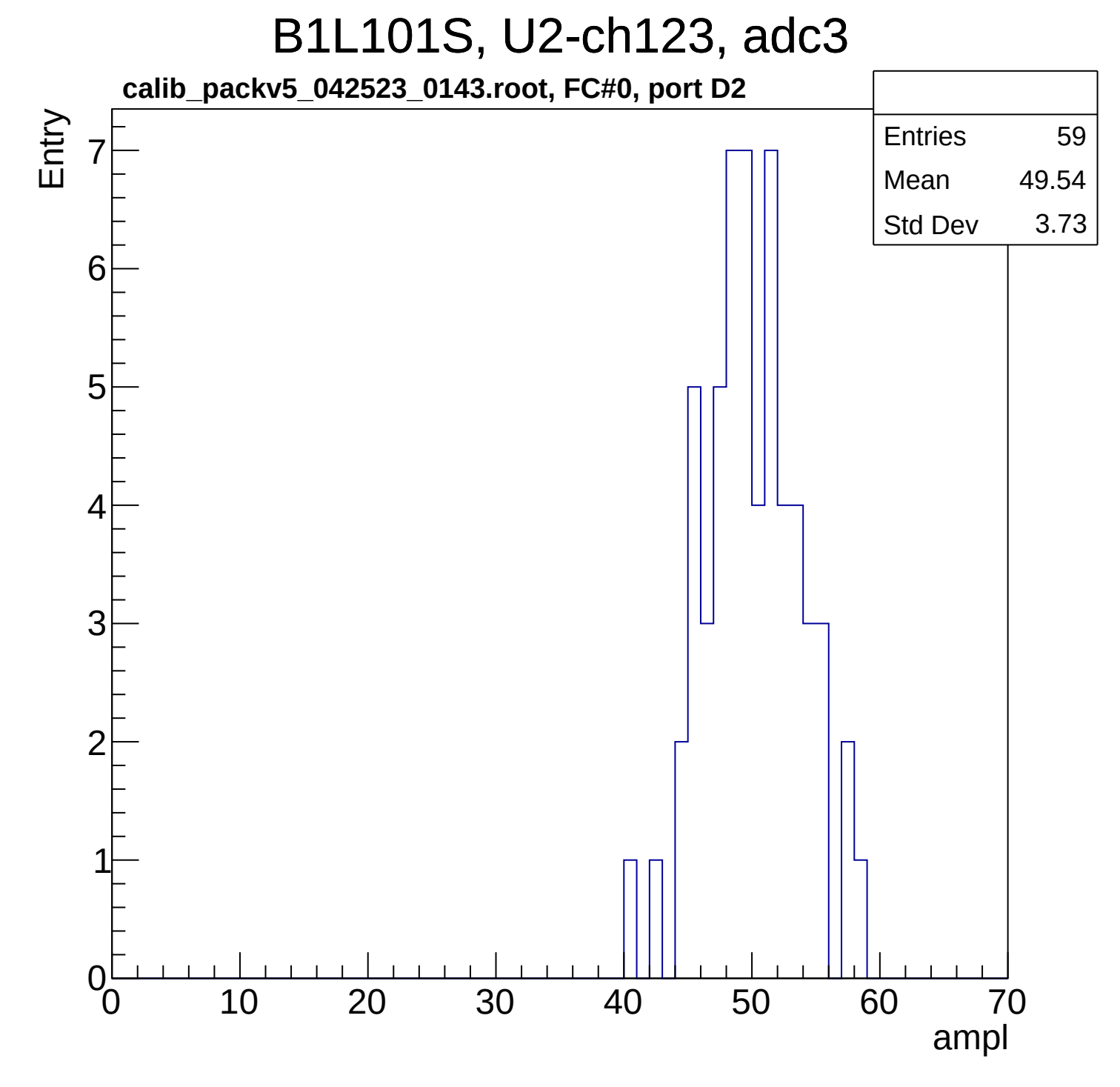

B1L101S, U2-ch122, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 19
Mean 61
Std Dev 2.103
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

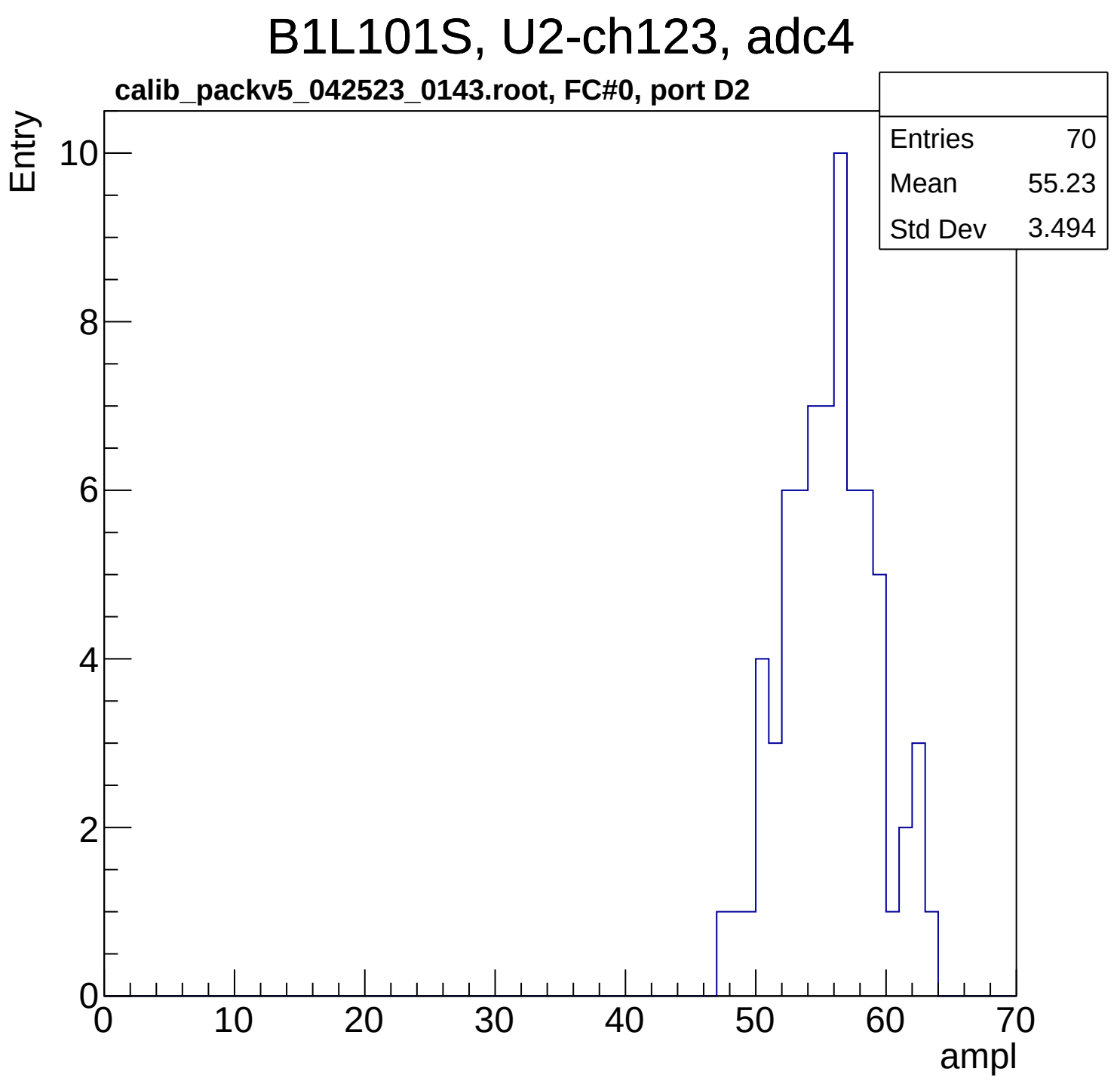

B1L101S, U2-ch122, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 4
Mean 31
Std Dev 31.01
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

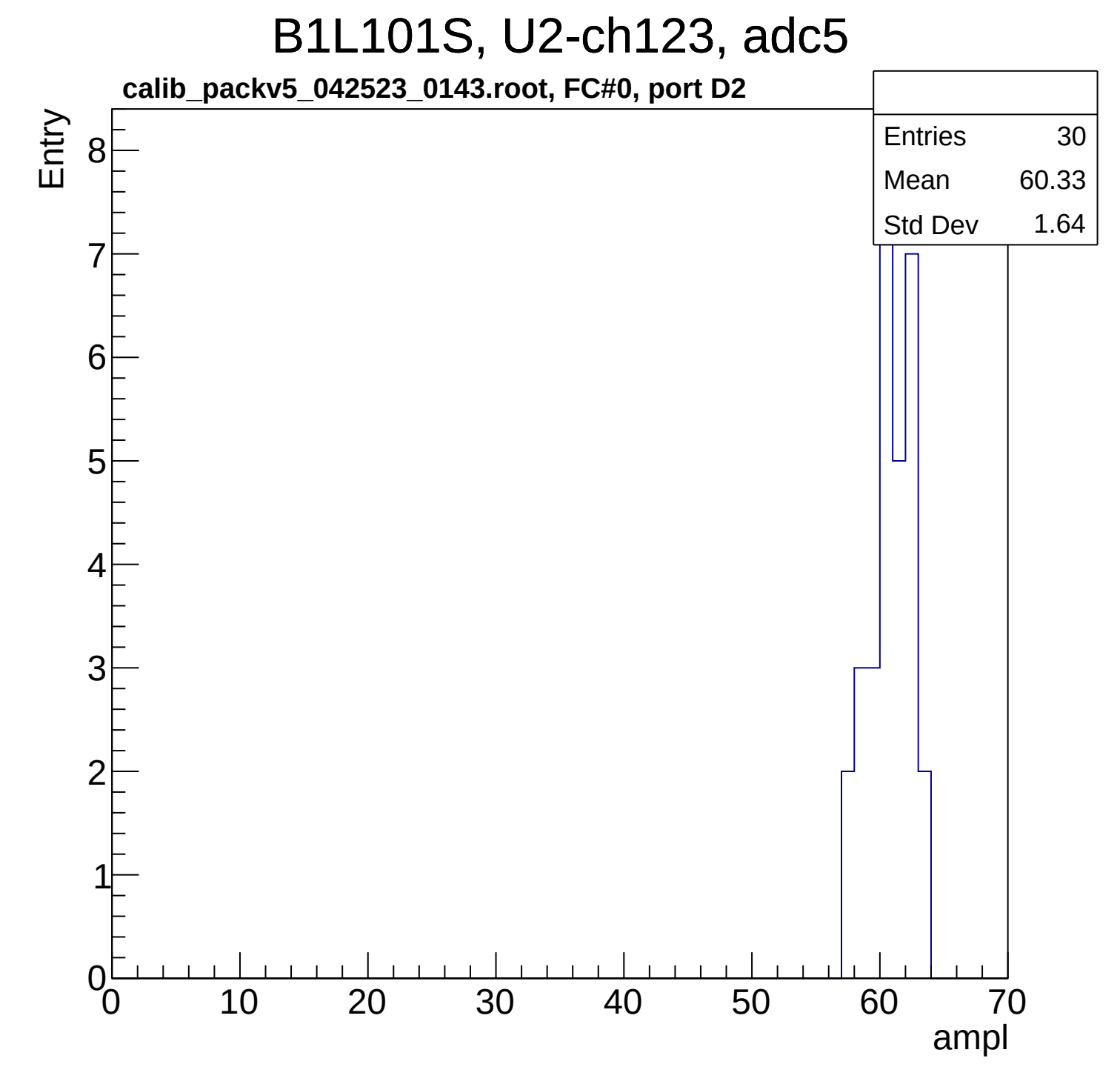

B1L101S, U2-ch123, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 77
Mean 30.06
Std Dev 3.536
Gaus mean : 31.2448
Gaus Width: 4.7064
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

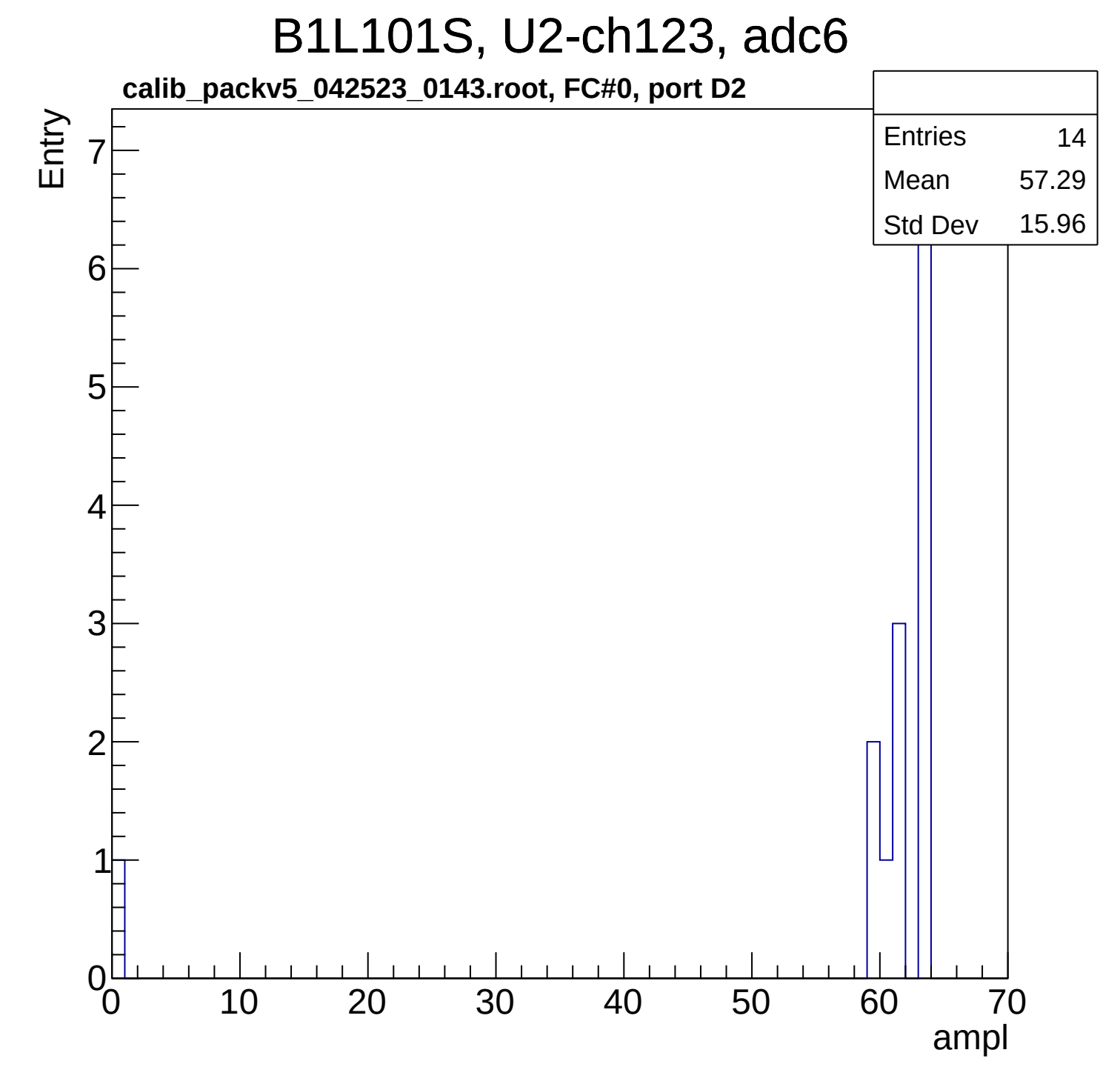

B1L101S, U2-ch123, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 66
Mean 37.52
Std Dev 3.581
Gaus mean : 38.5514
Gaus Width: 3.8107
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

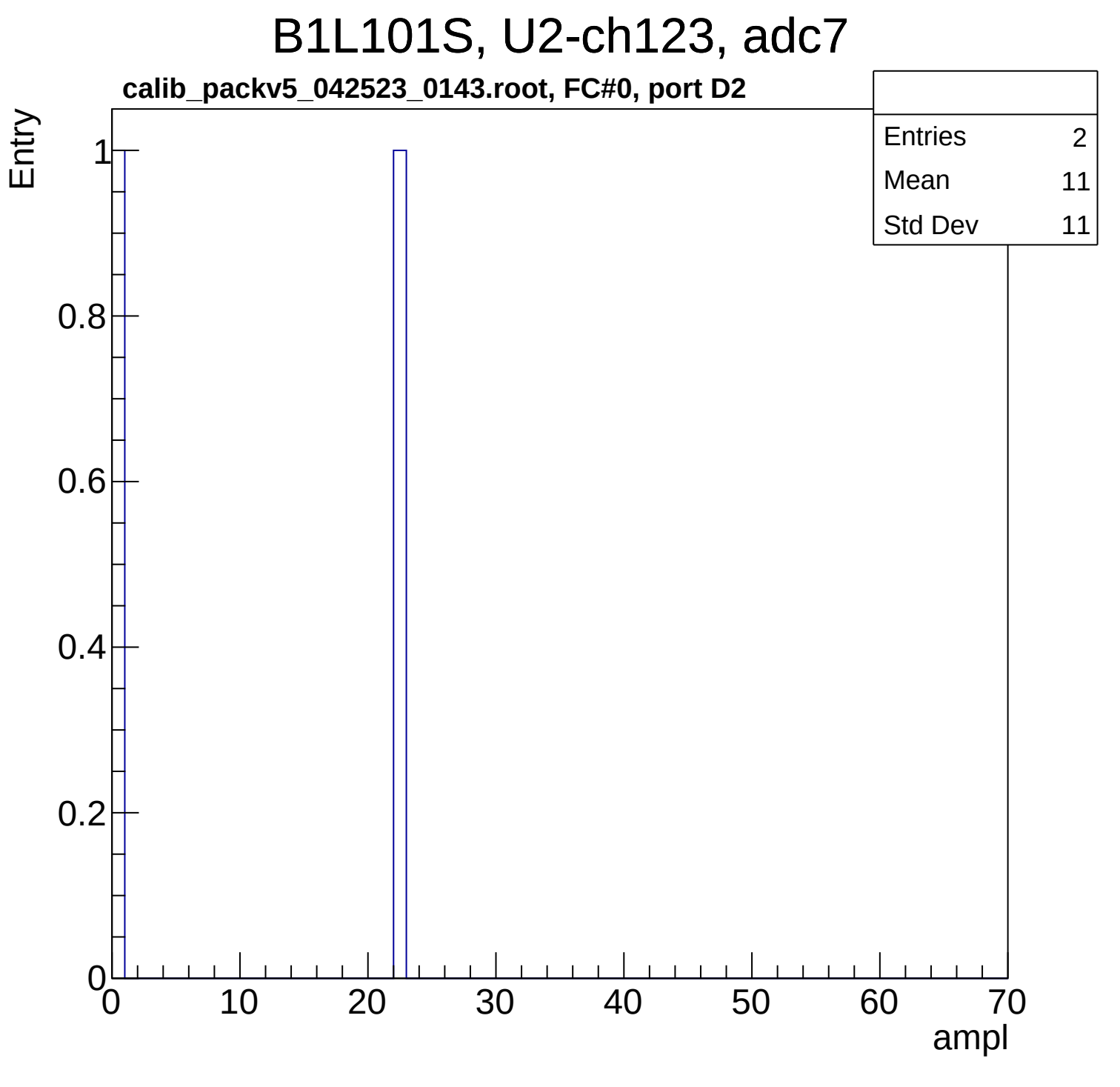

B1L101S, U2-ch123, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 56
Mean 43.41
Std Dev 3.432
Gaus mean : 44.2473
Gaus Width: 3.7284
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

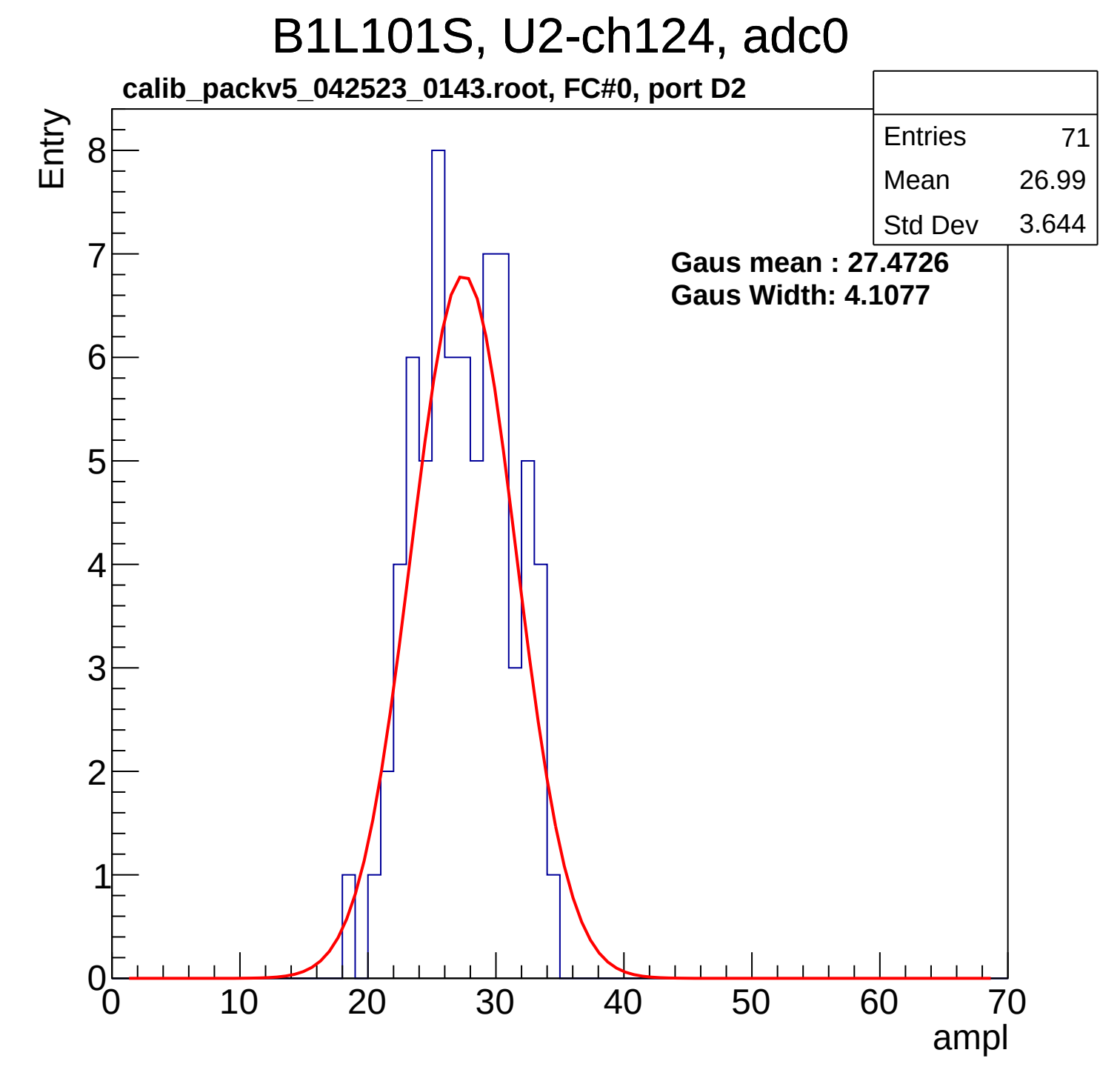

B1L101S, U2-ch123, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 49.54
Std Dev 3.73
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

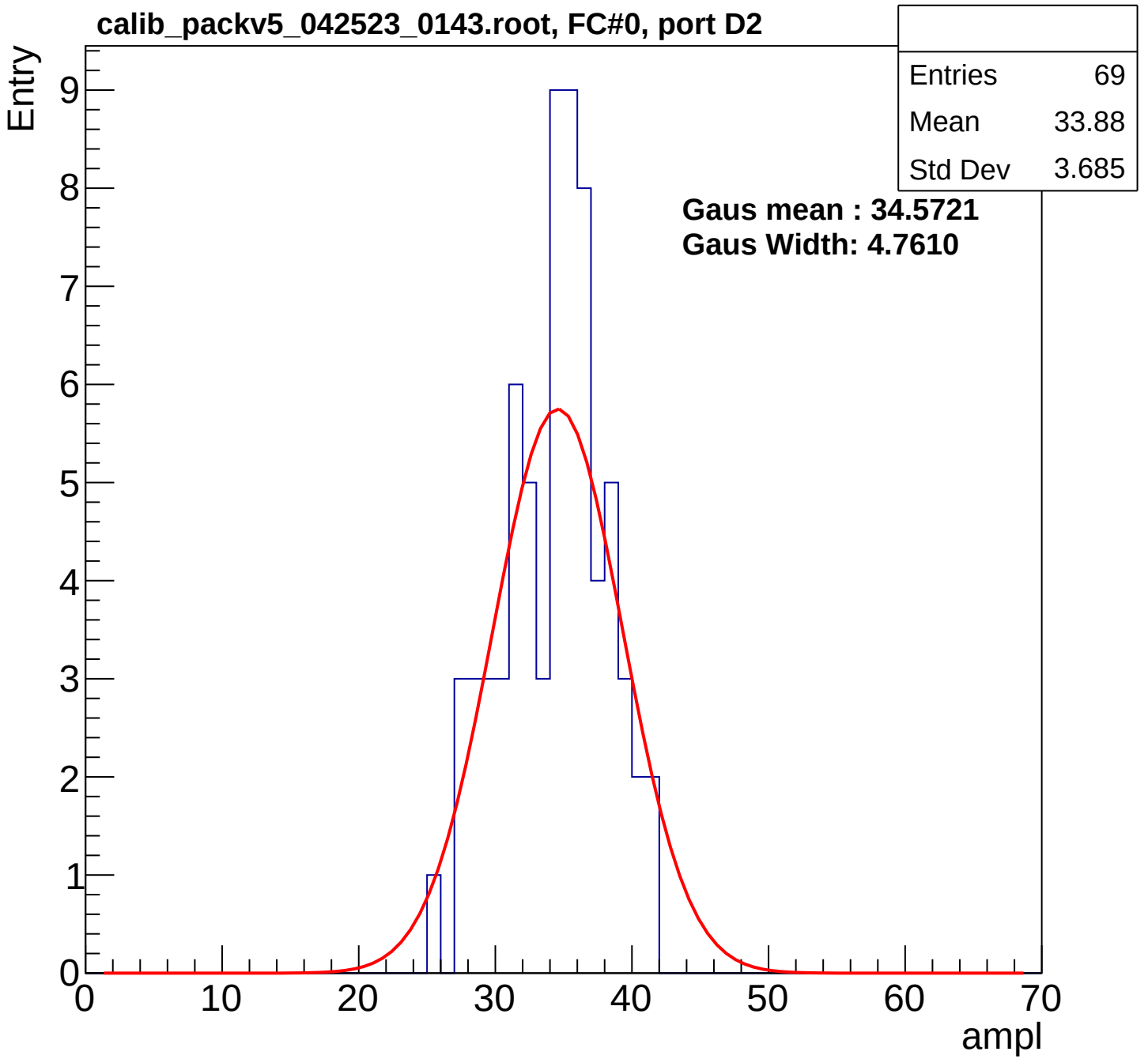

B1L101S, U2-ch123, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 70
Mean 55.23
Std Dev 3.494
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

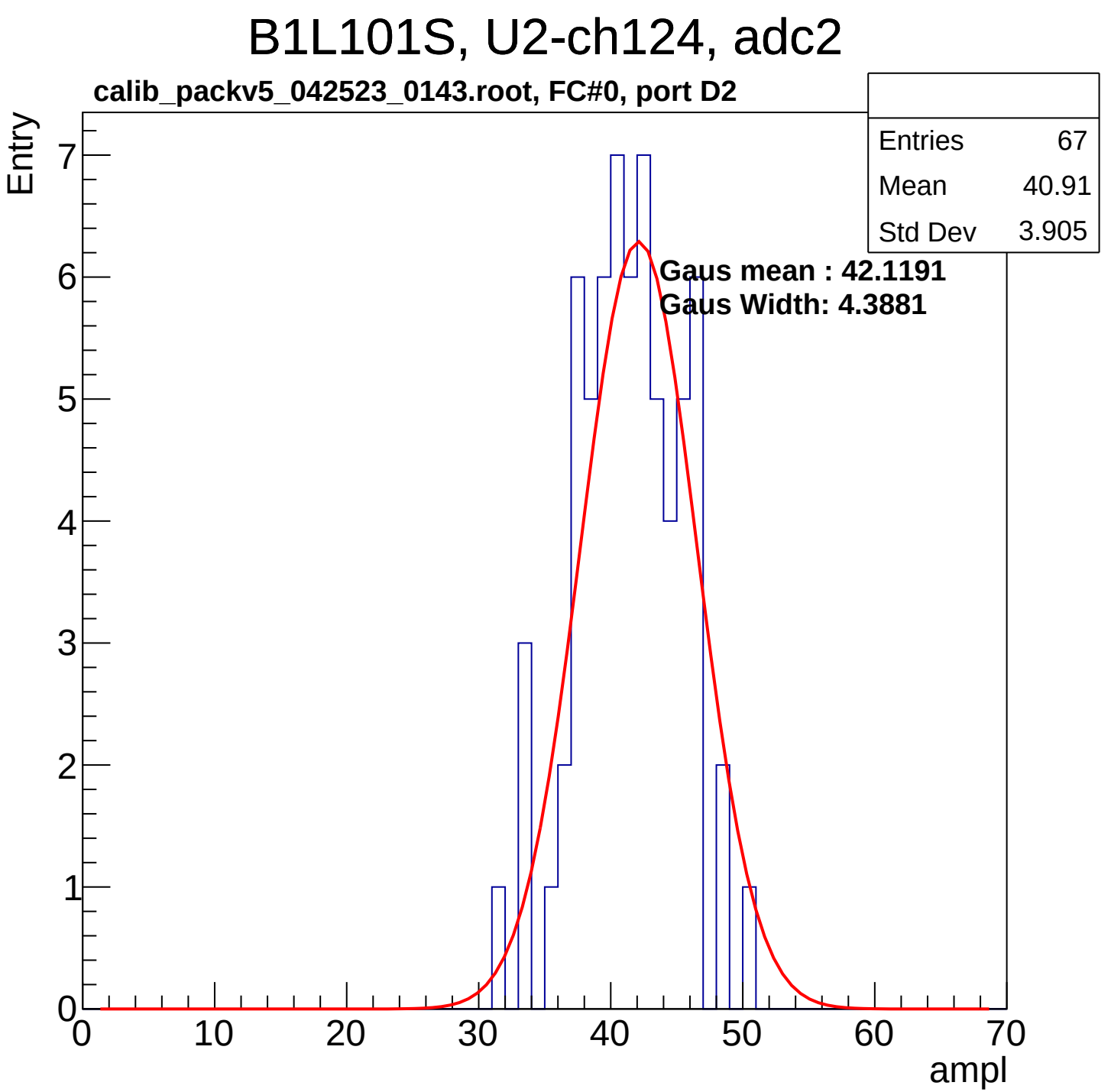

B1L101S, U2-ch123, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 30
Mean 60.33
Std Dev 1.64
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

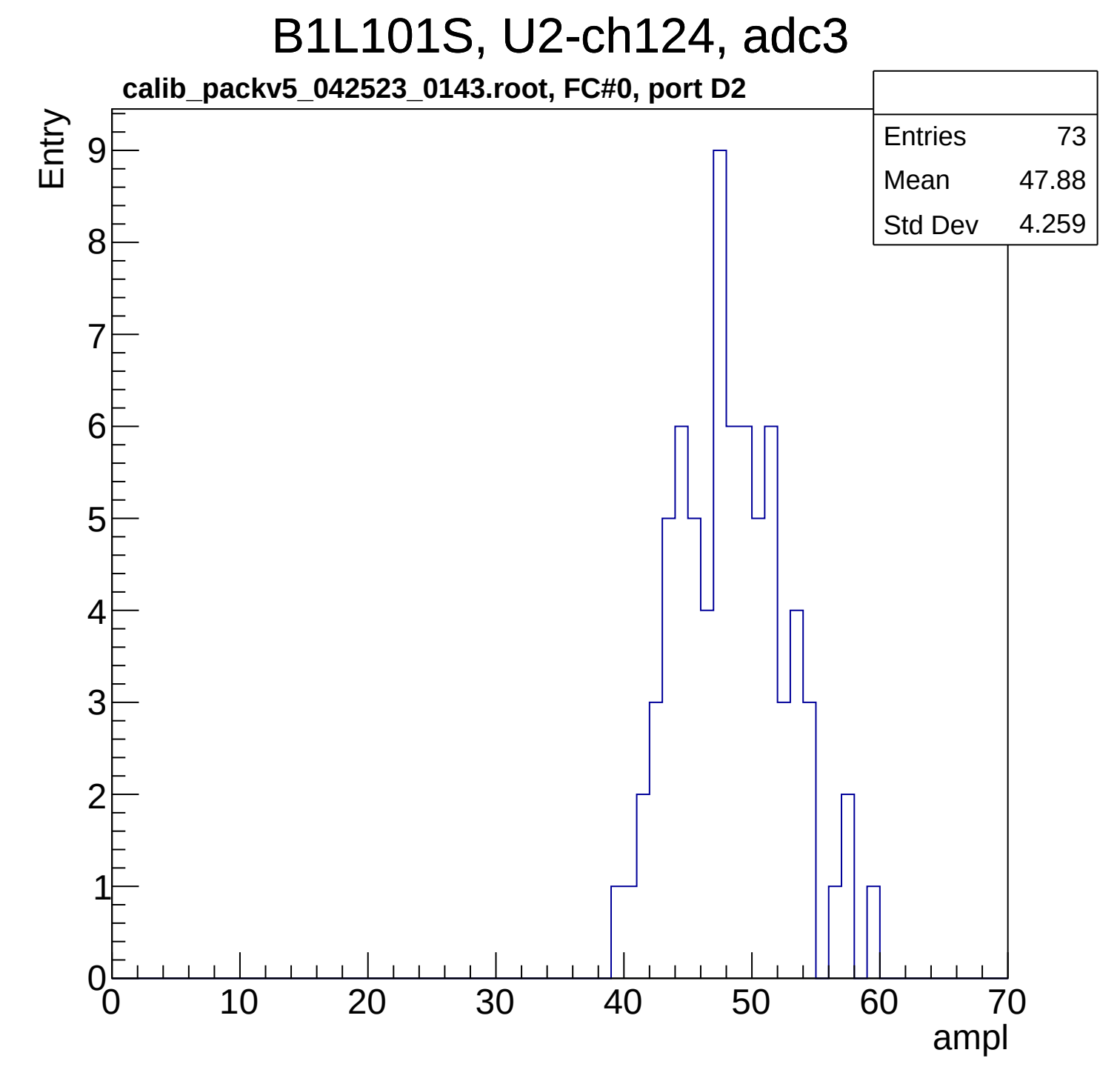

B1L101S, U2-ch123, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 14
Mean 57.29
Std Dev 15.96
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

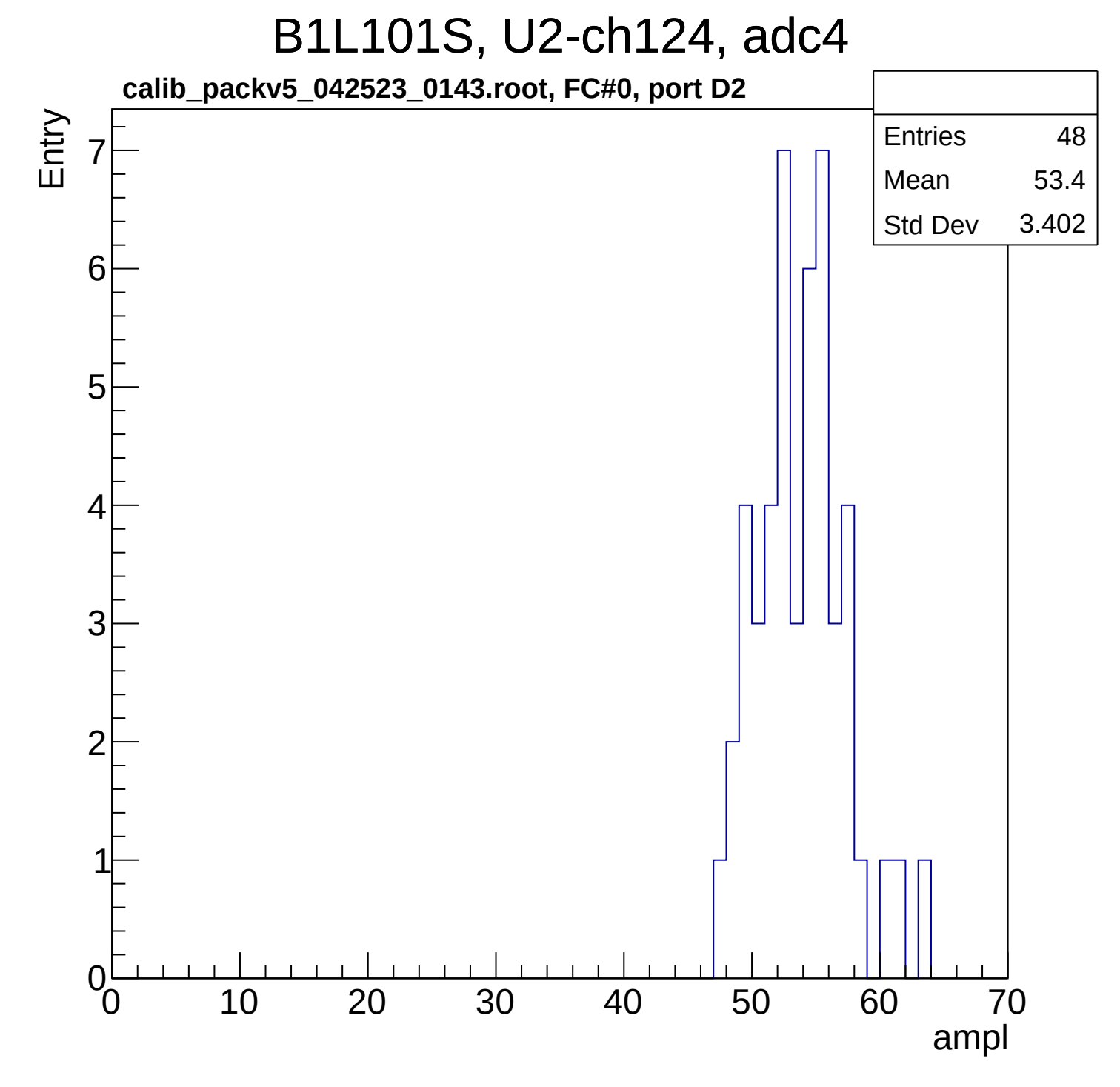

B1L101S, U2-ch123, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 11
Std Dev 11
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

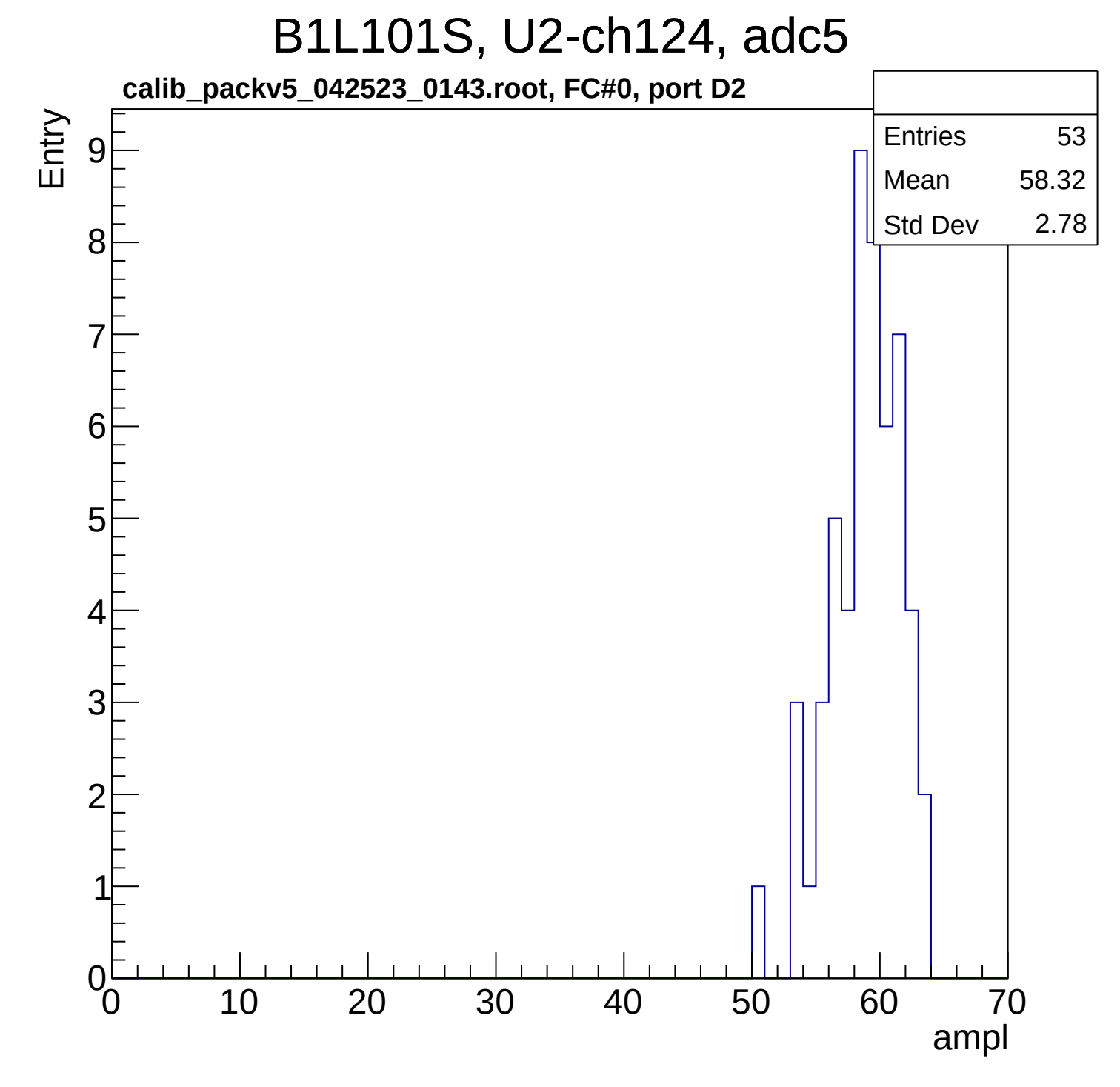

B1L101S, U2-ch124, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 26.99
Std Dev 3.644
Gaus mean : 27.4726
Gaus Width: 4.1077
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

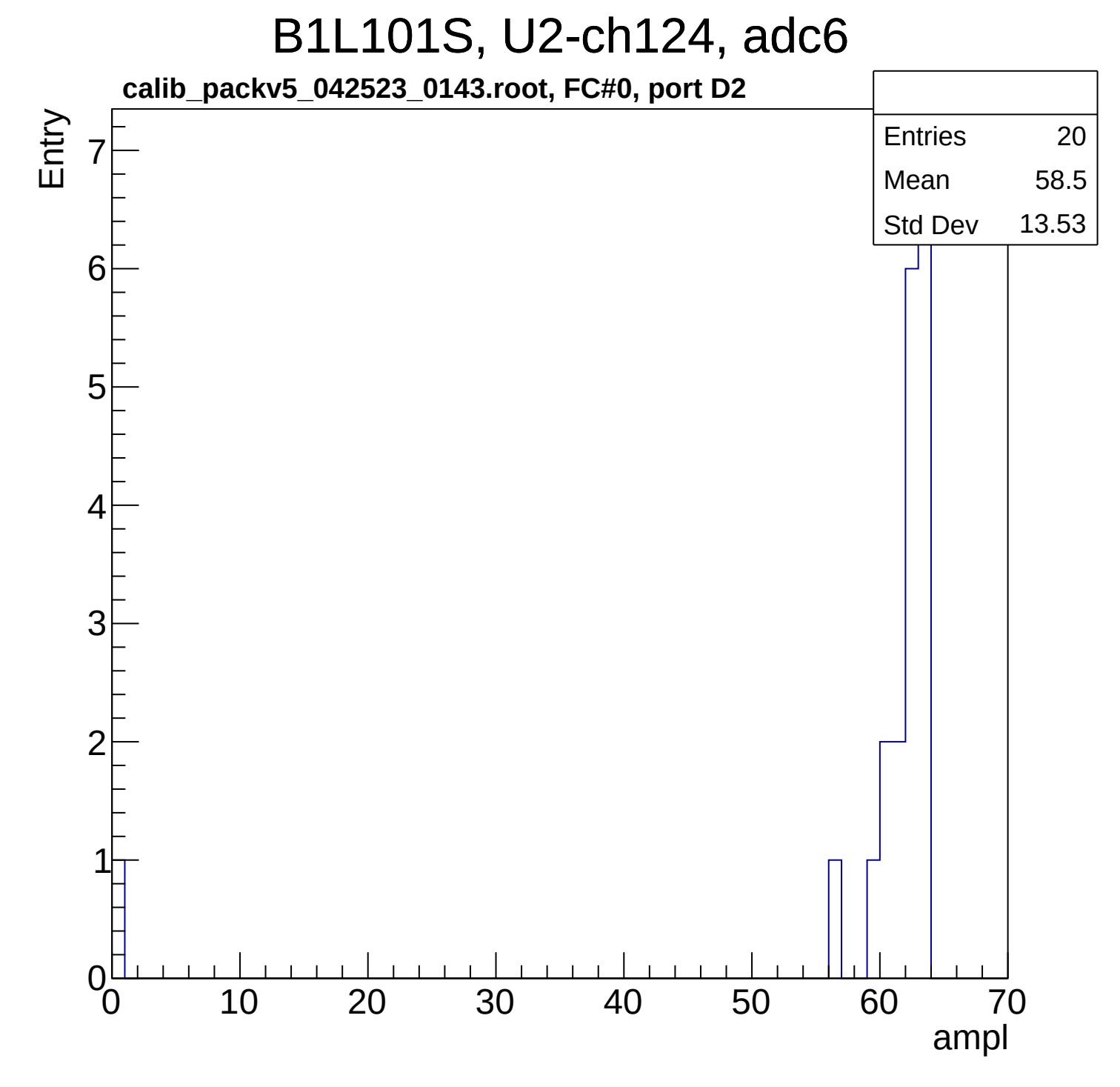

B1L101S, U2-ch124, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 69
Mean 33.88
Std Dev 3.685
Gaus mean : 34.5721
Gaus Width: 4.7610
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

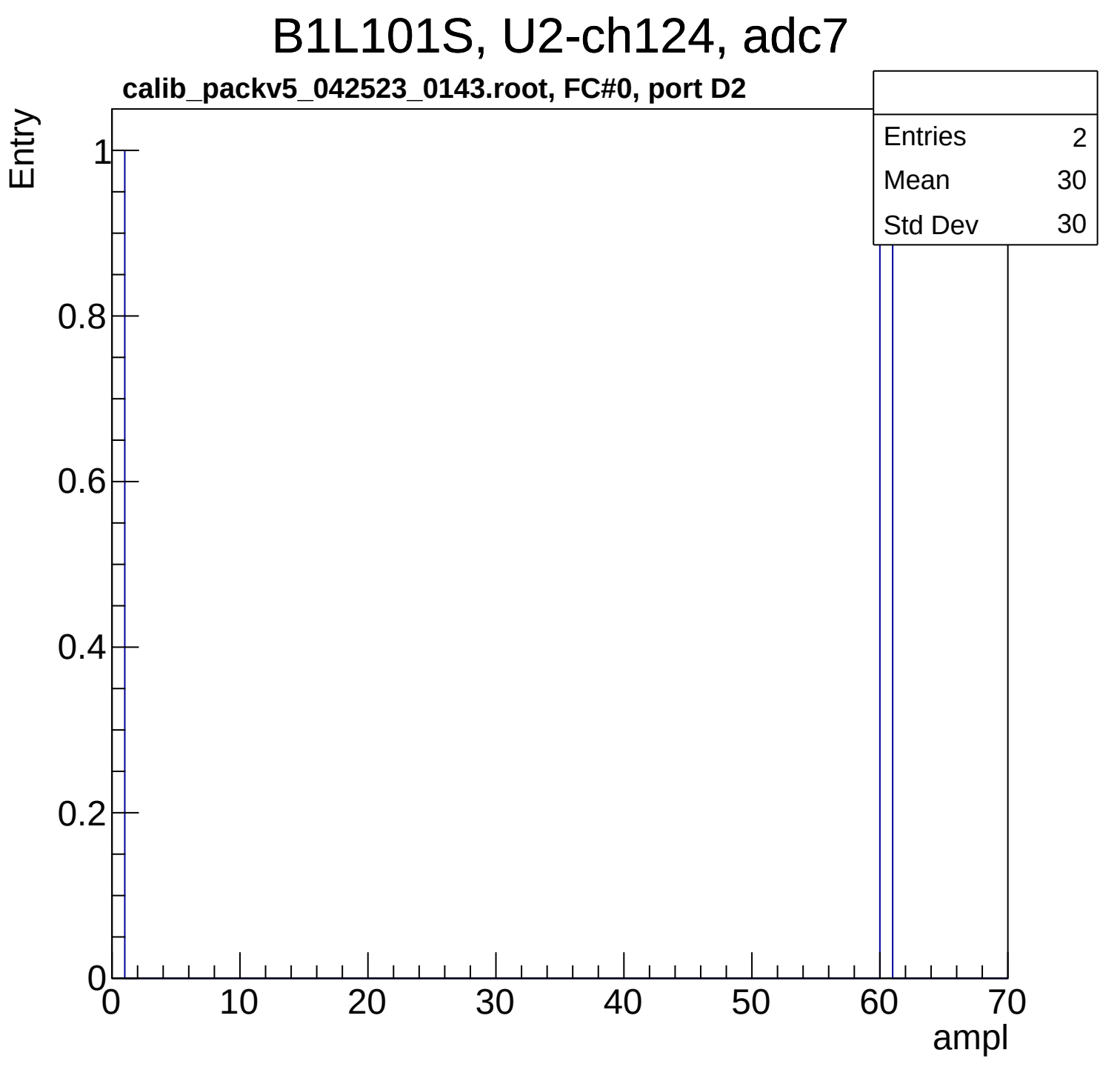

B1L101S, U2-ch124, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 40.91
Std Dev 3.905
Gaus mean : 42.1191
Gaus Width: 4.3881
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

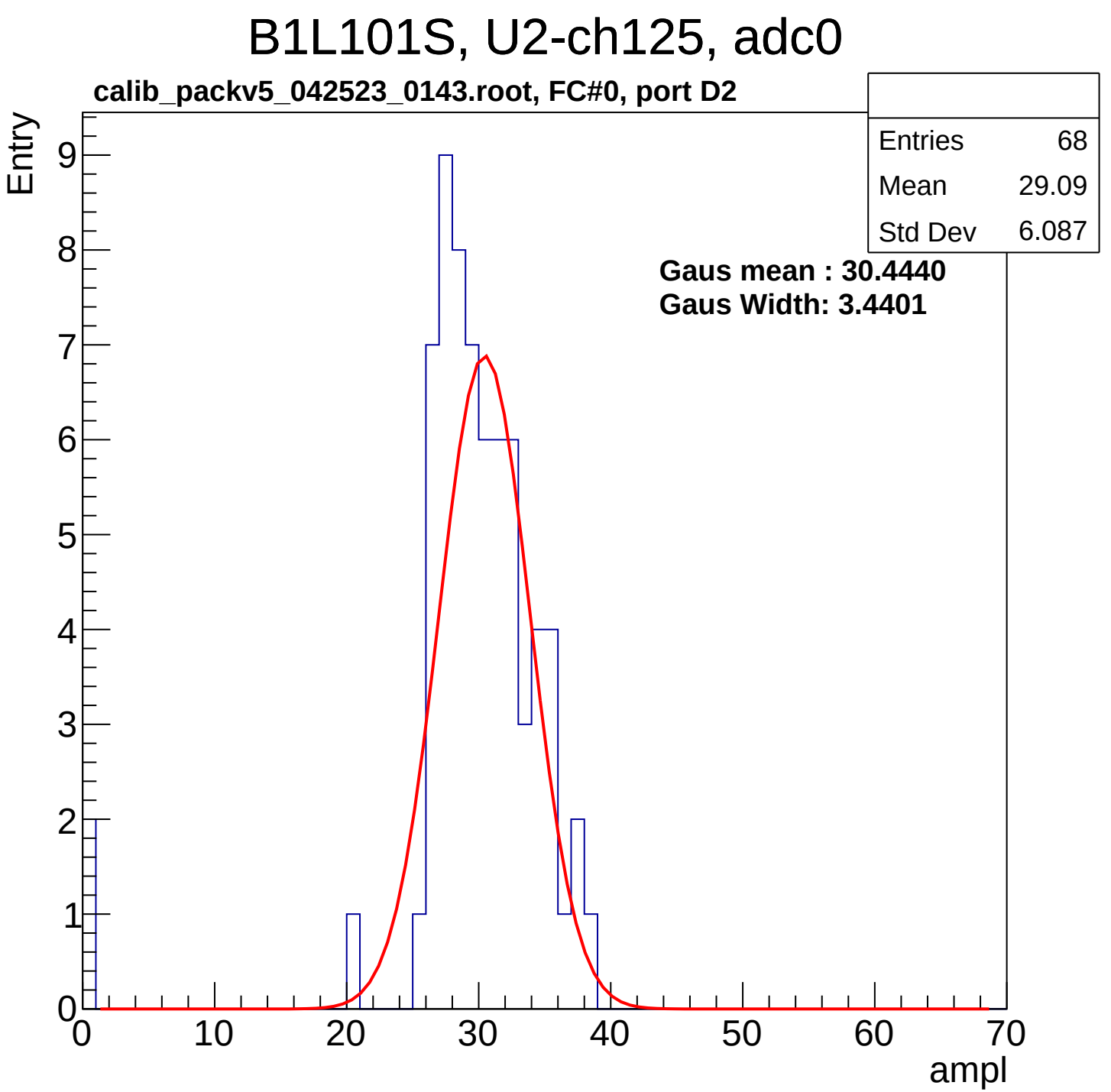

B1L101S, U2-ch124, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 73
Mean 47.88
Std Dev 4.259
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

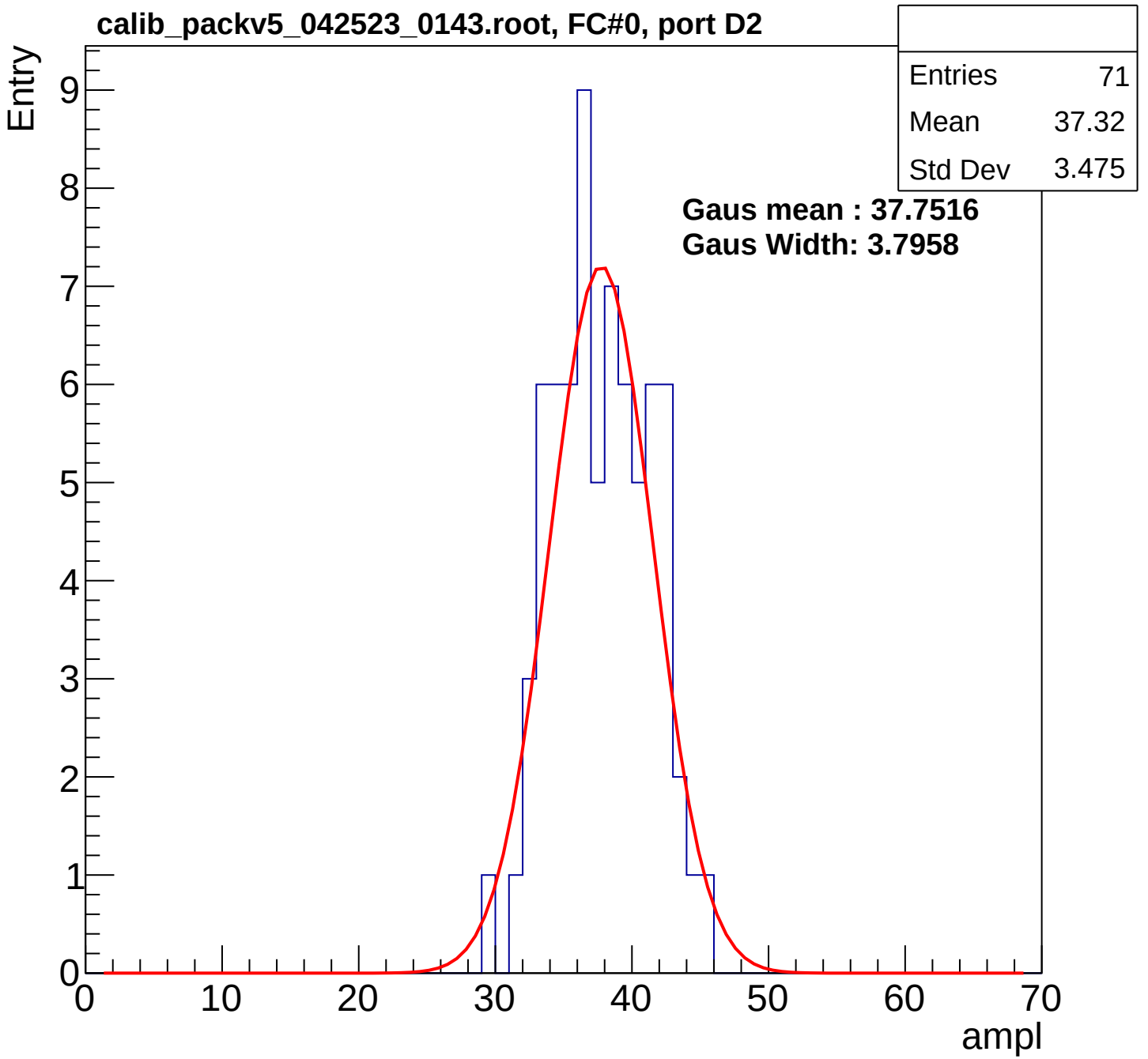

B1L101S, U2-ch124, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 48
Mean 53.4
Std Dev 3.402
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

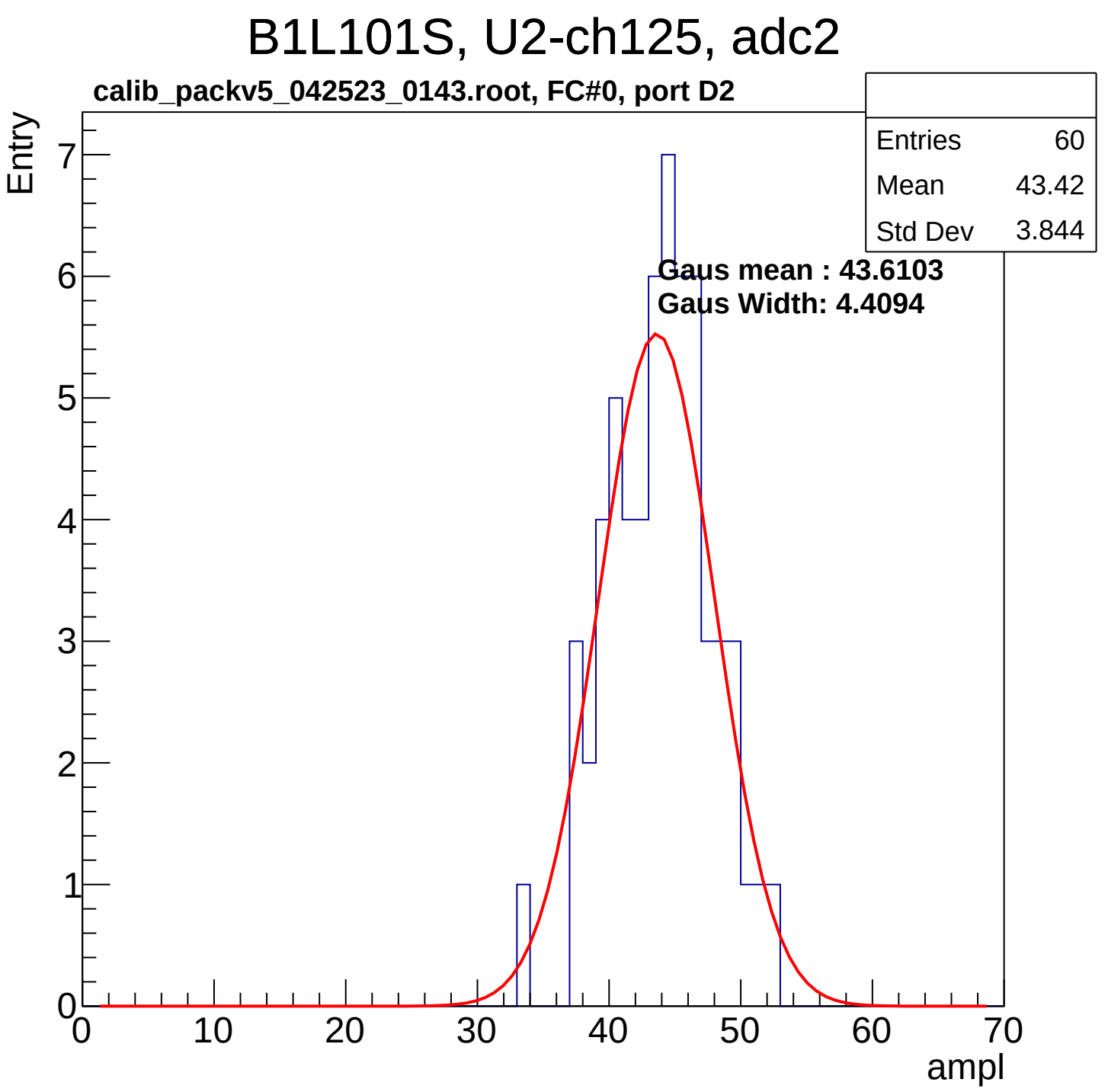

B1L101S, U2-ch124, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 53
Mean 58.32
Std Dev 2.78
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

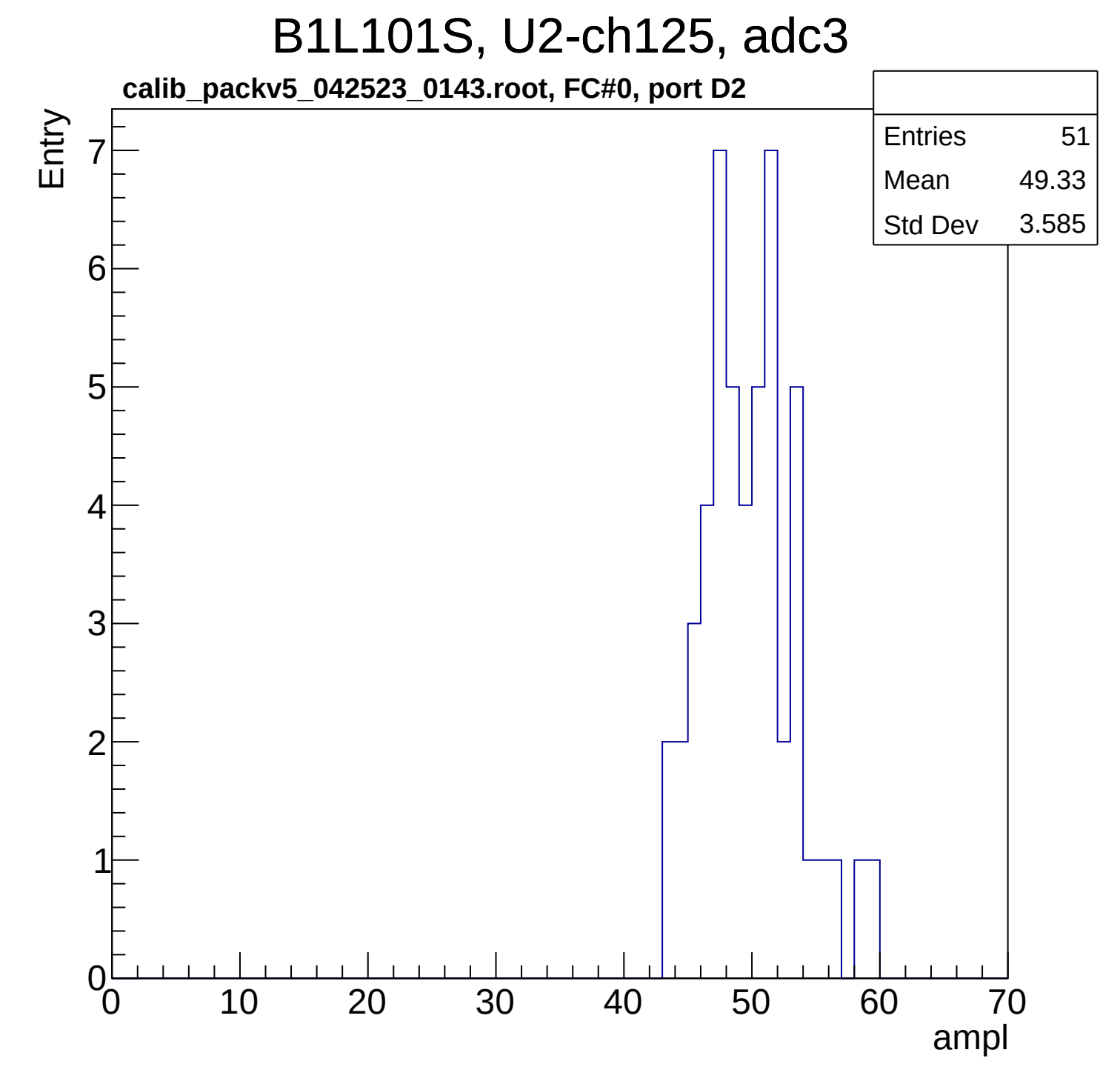

B1L101S, U2-ch124, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 20
Mean 58.5
Std Dev 13.53
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

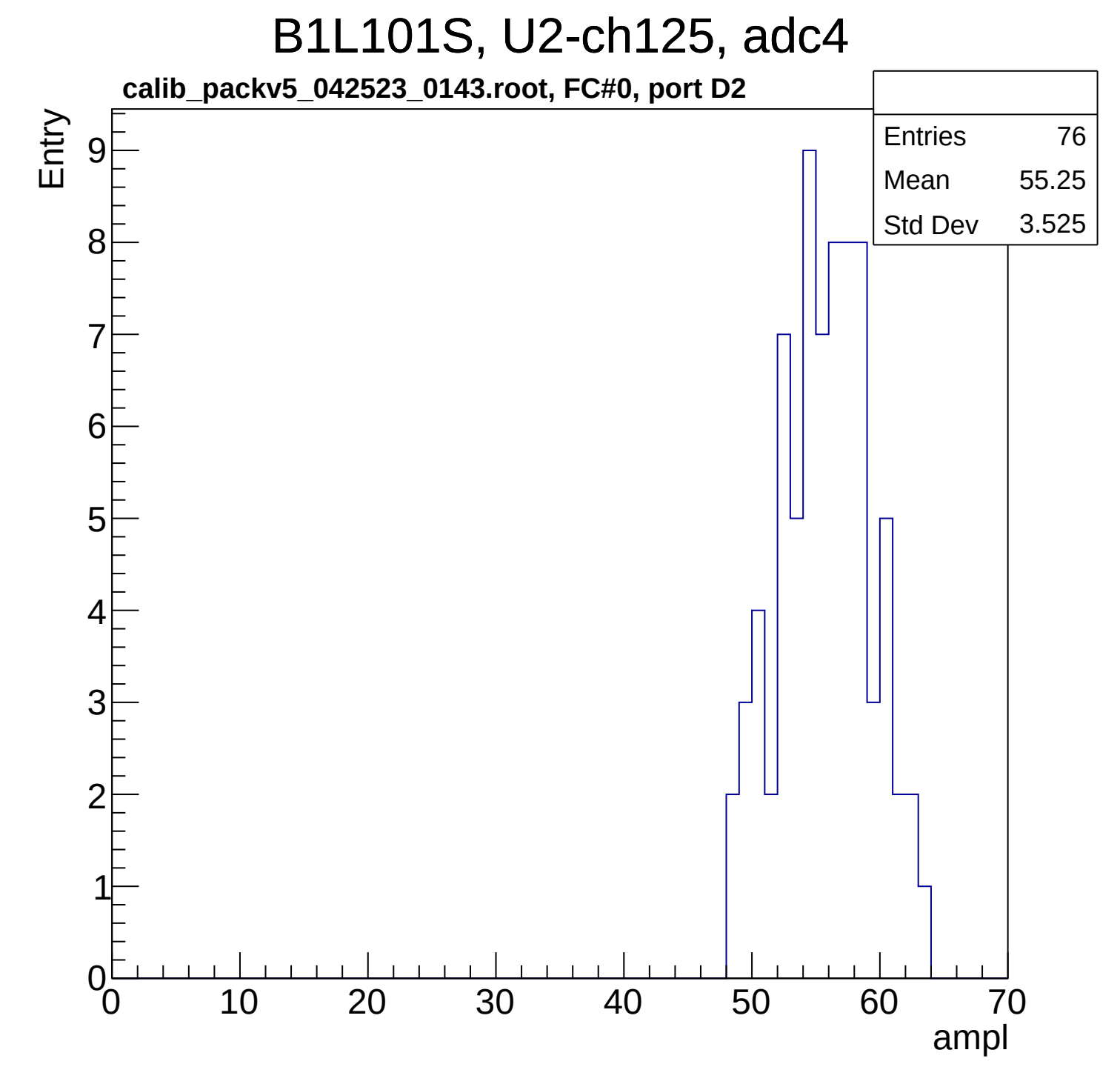

B1L101S, U2-ch124, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 2
Mean 30
Std Dev 30
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

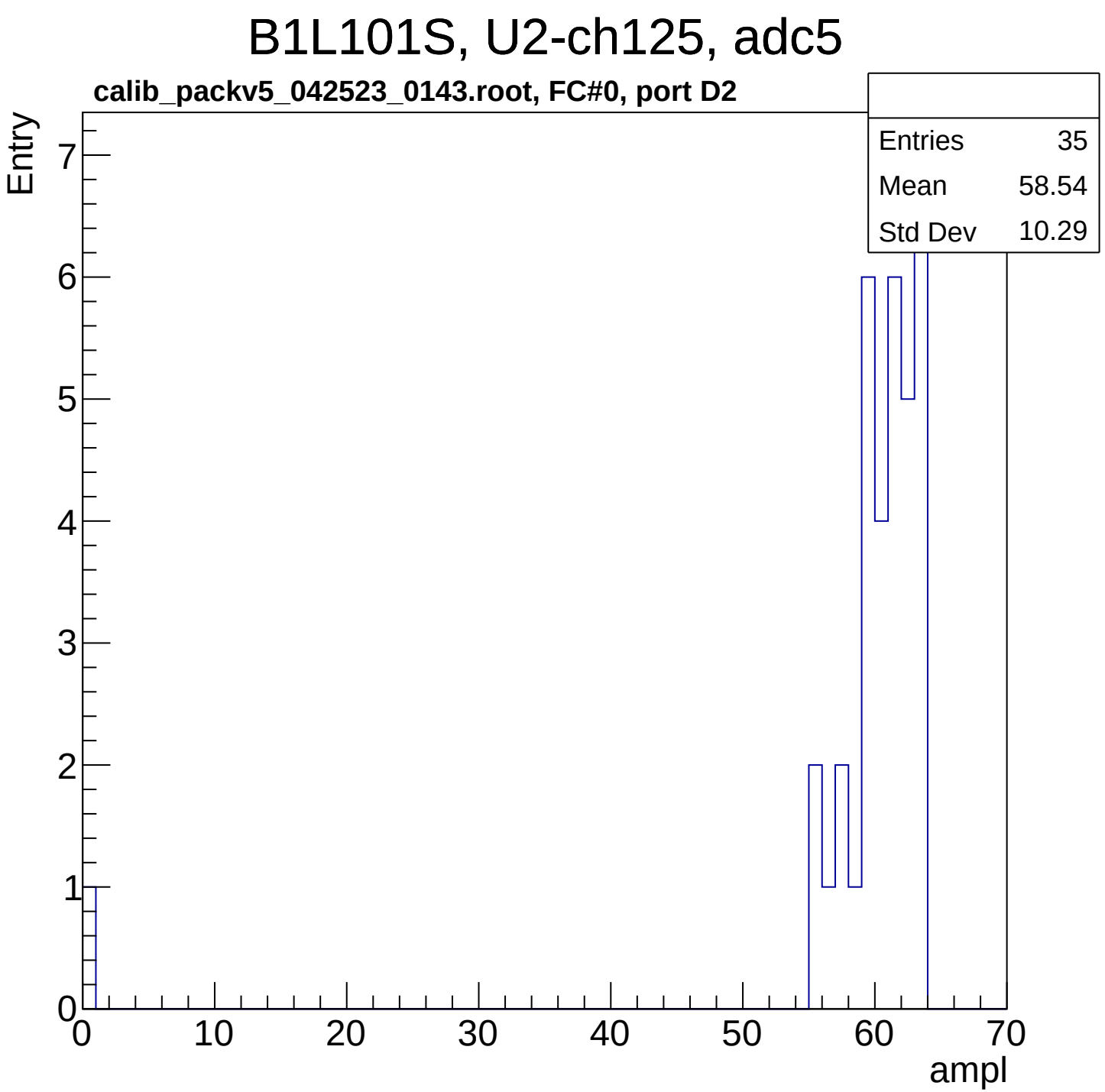

B1L101S, U2-ch125, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 68
Mean 29.09
Std Dev 6.087
Gaus mean : 30.4440
Gaus Width: 3.4401
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

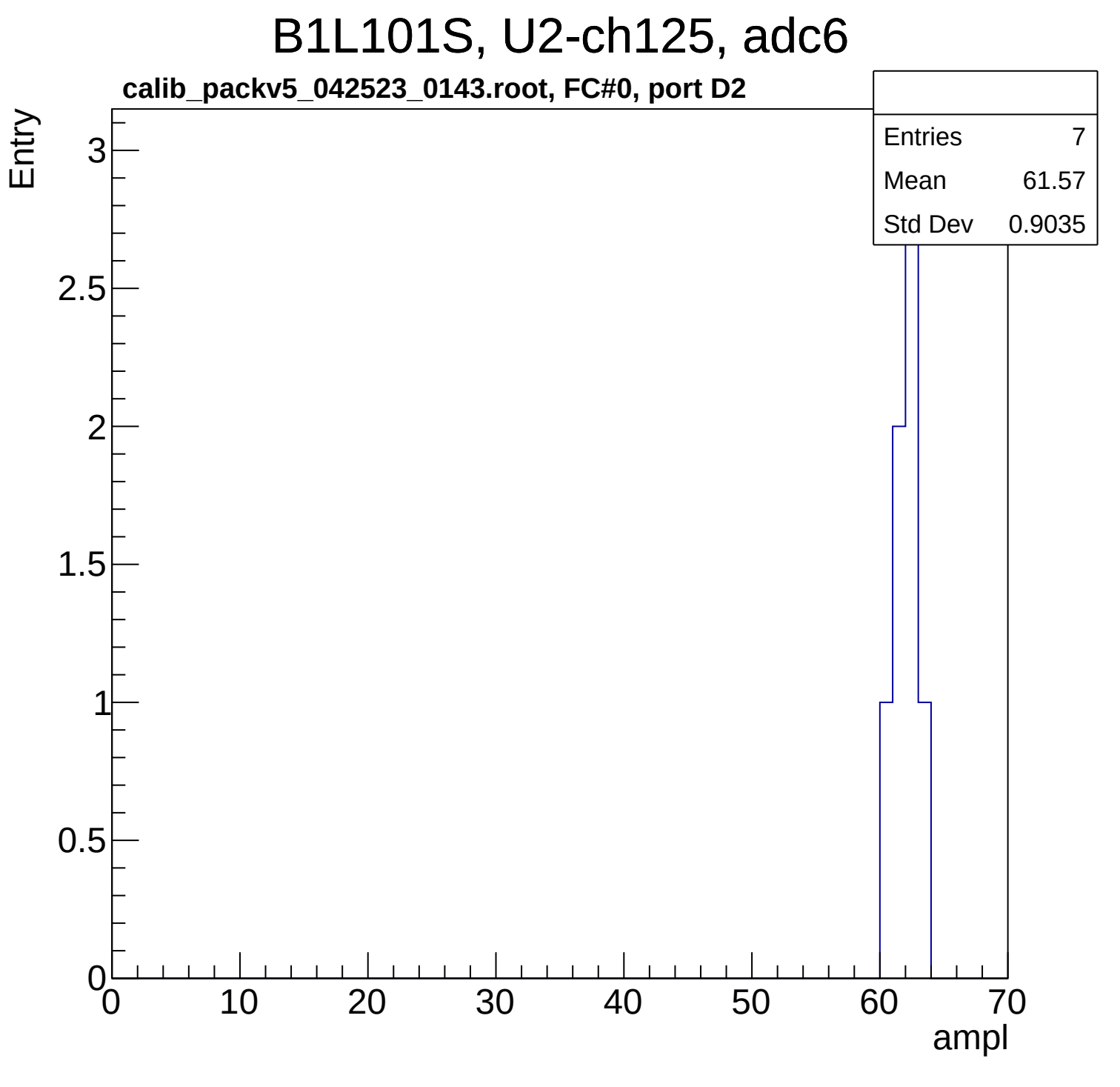

B1L101S, U2-ch125, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 37.32
Std Dev 3.475
Gaus mean : 37.7516
Gaus Width: 3.7958
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

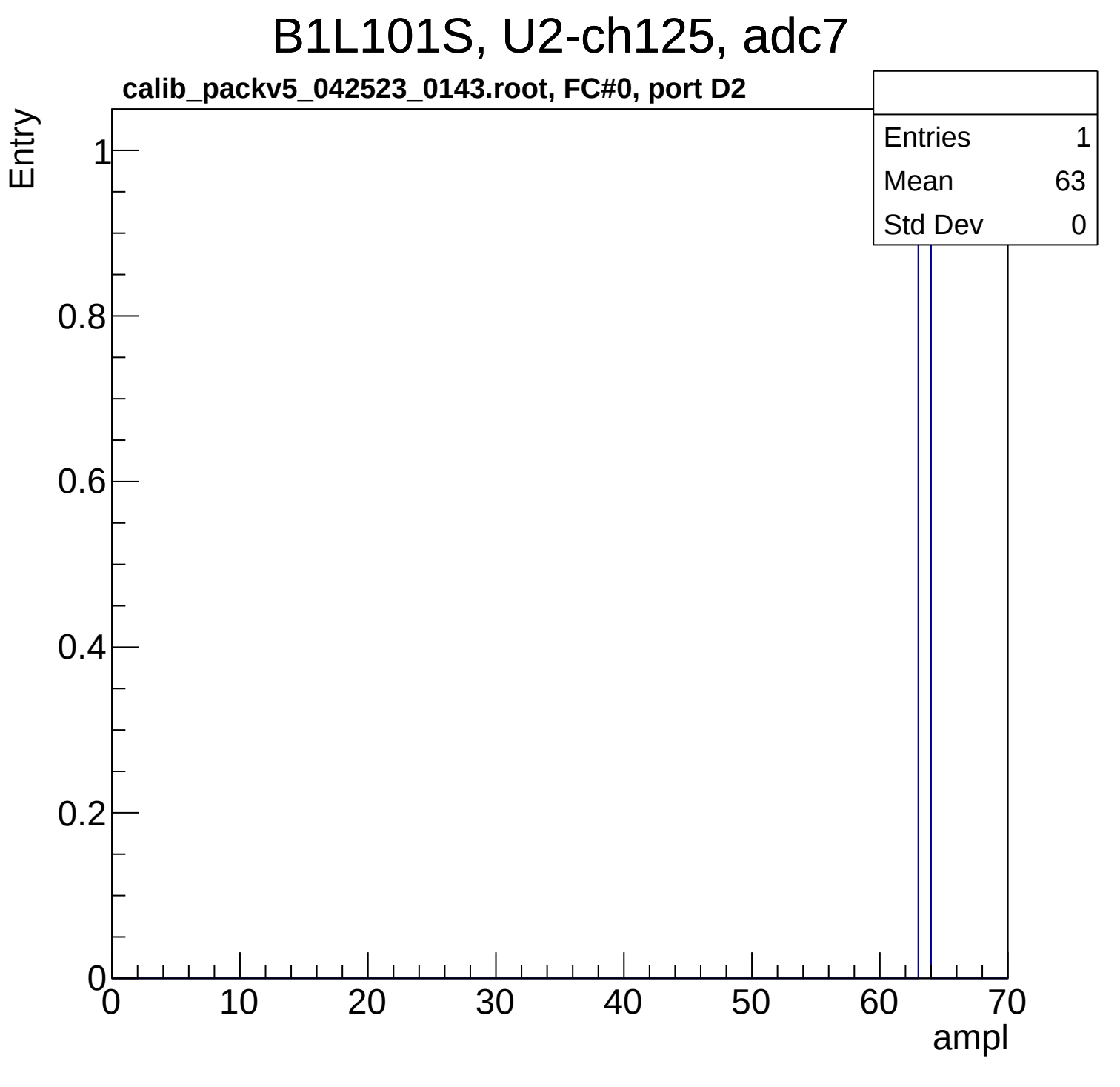

B1L101S, U2-ch125, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 60
Mean 43.42
Std Dev 3.844
Gaus mean : 43.6103
Gaus Width: 4.4094
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

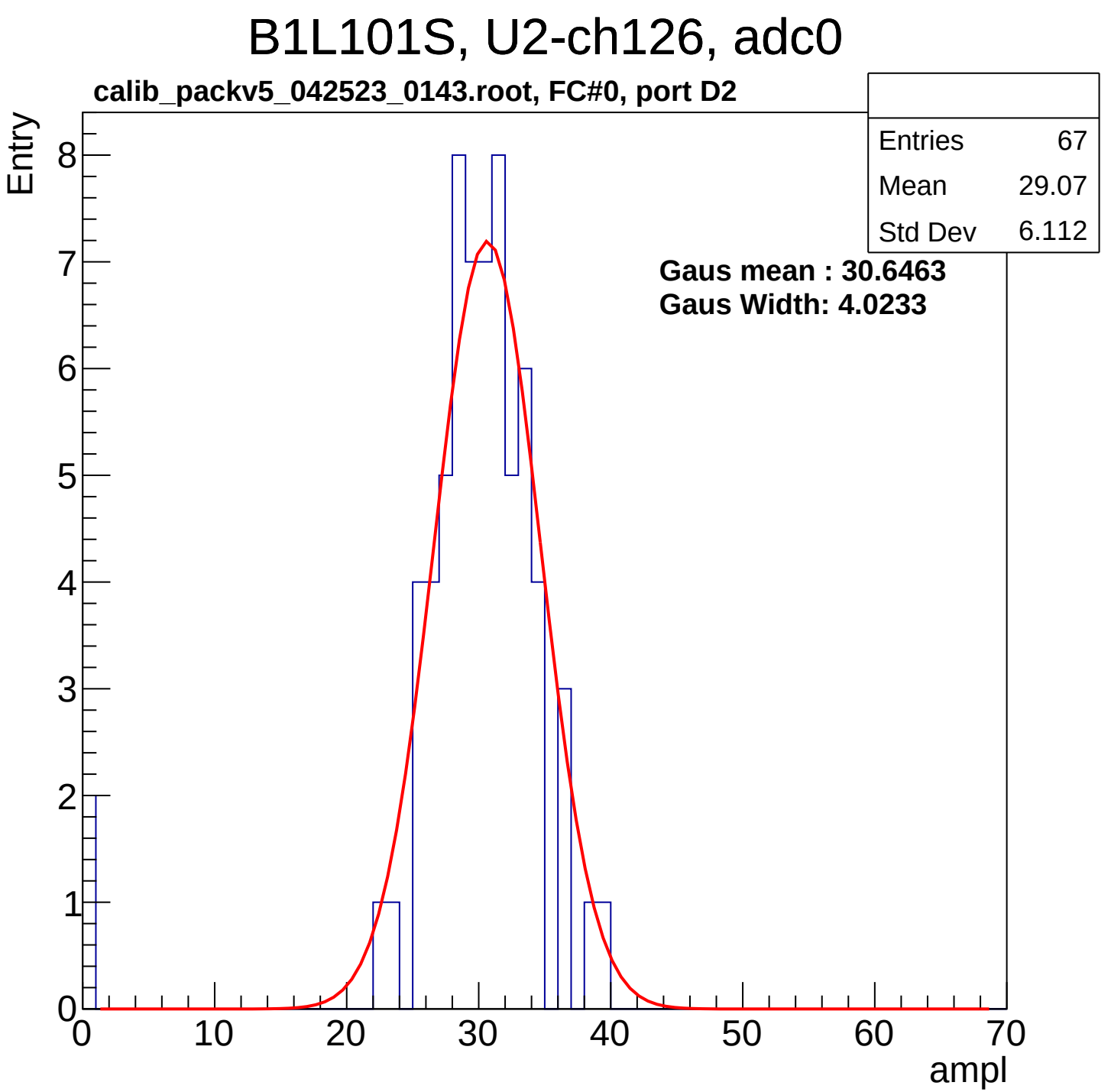

B1L101S, U2-ch125, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 51
Mean 49.33
Std Dev 3.585
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

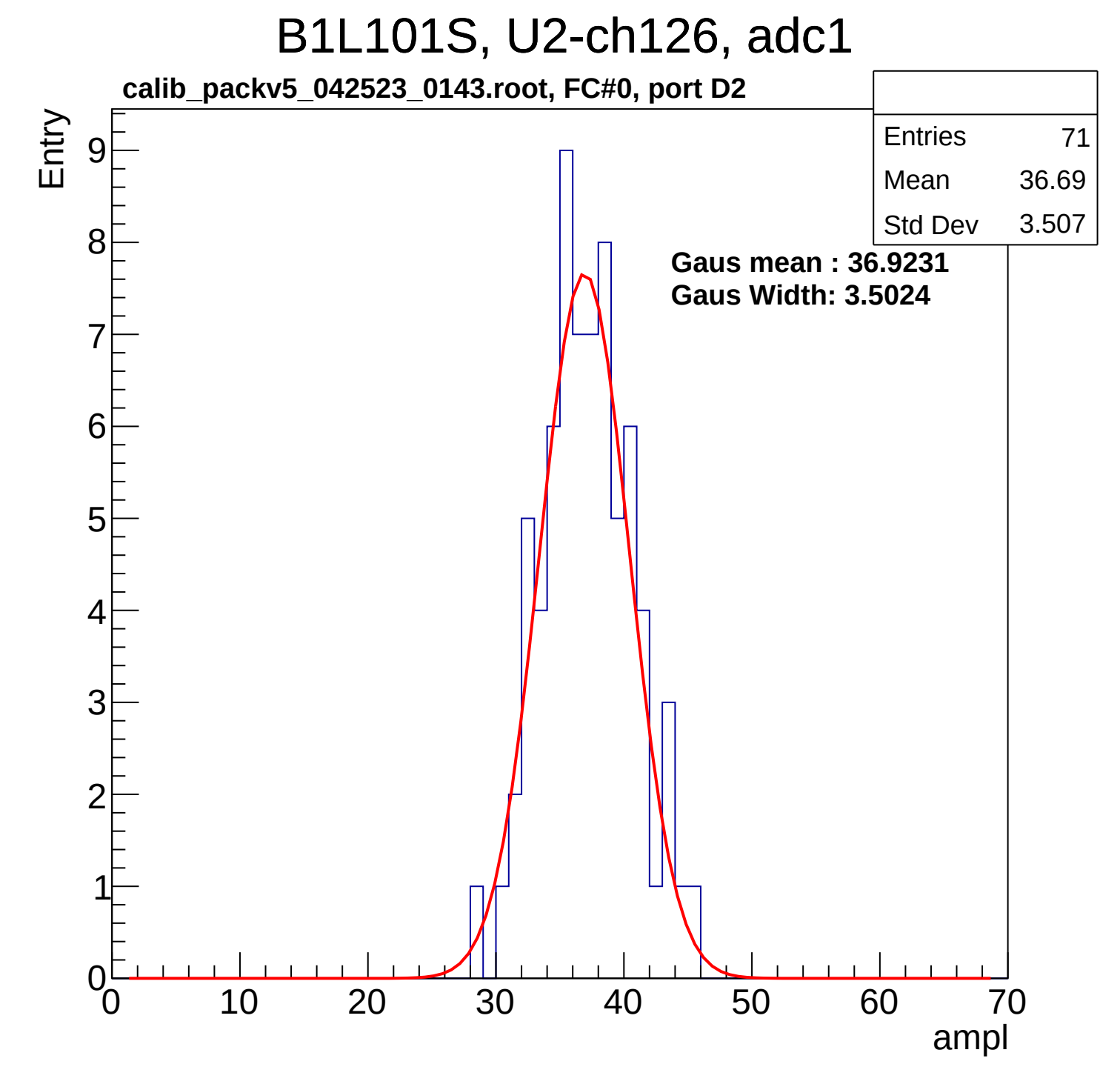

B1L101S, U2-ch125, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 76
Mean 55.25
Std Dev 3.525
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

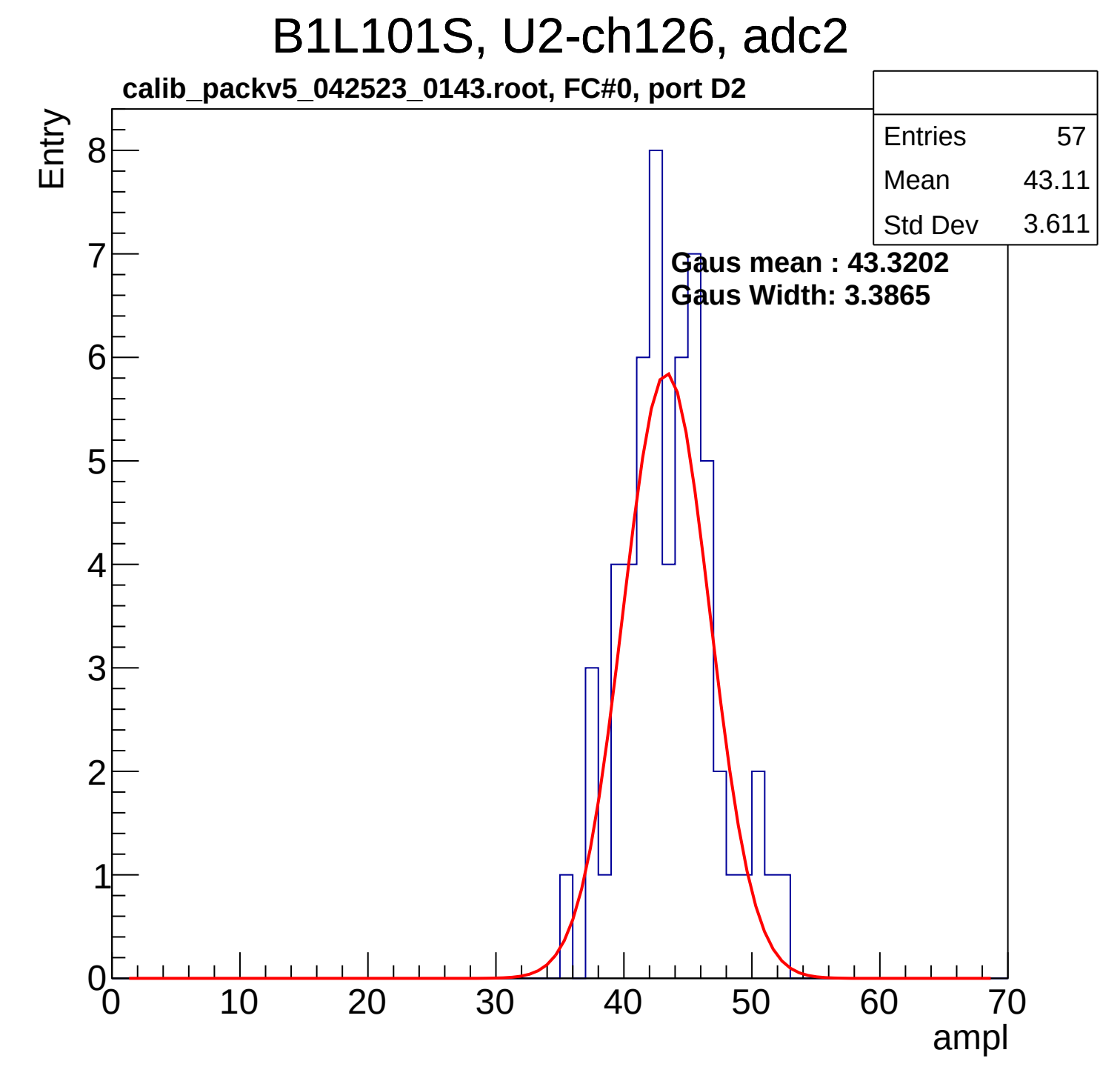

B1L101S, U2-ch125, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 35
Mean 58.54
Std Dev 10.29
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

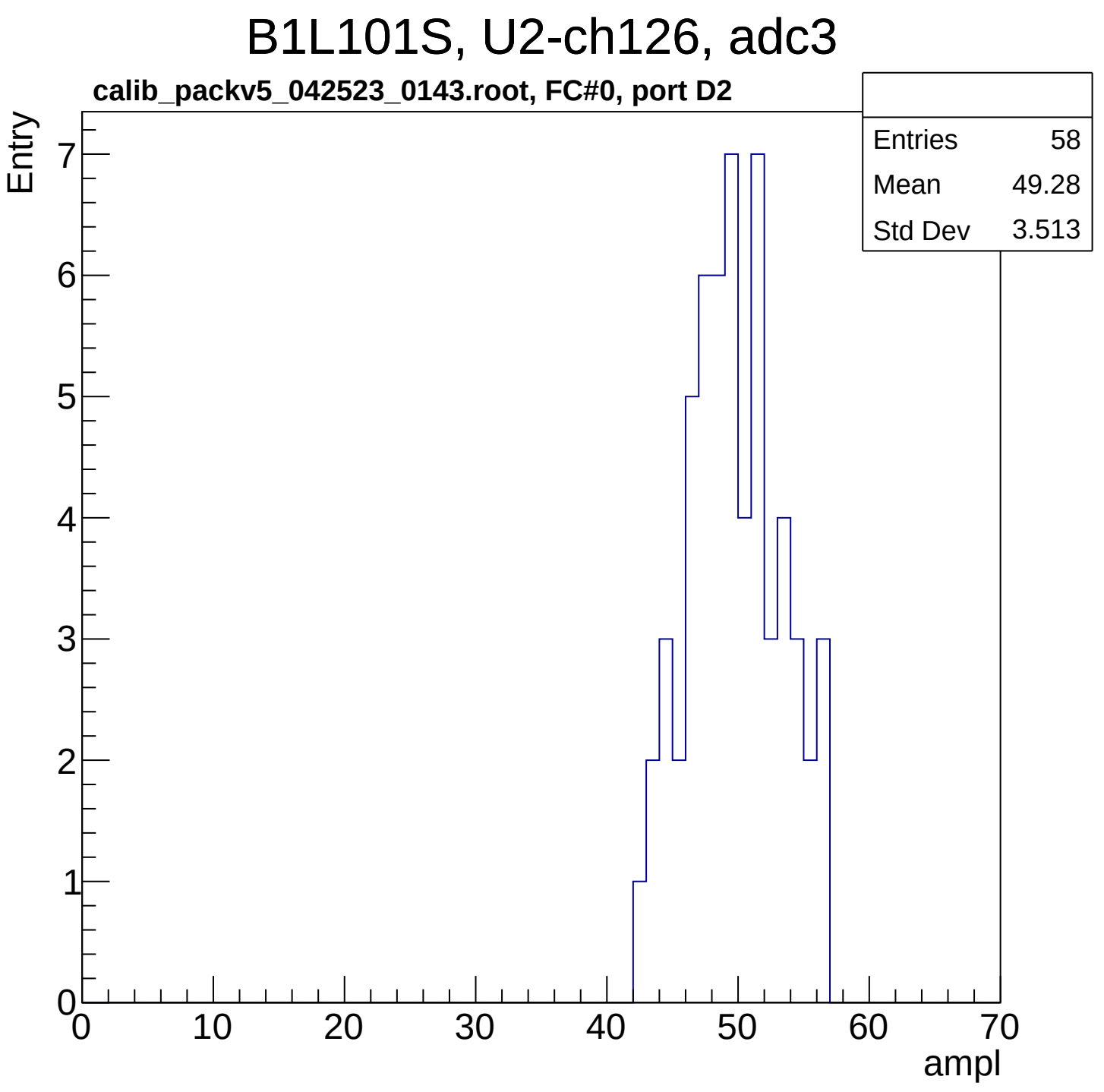

B1L101S, U2-ch125, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 7
Mean 61.57
Std Dev 0.9035
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

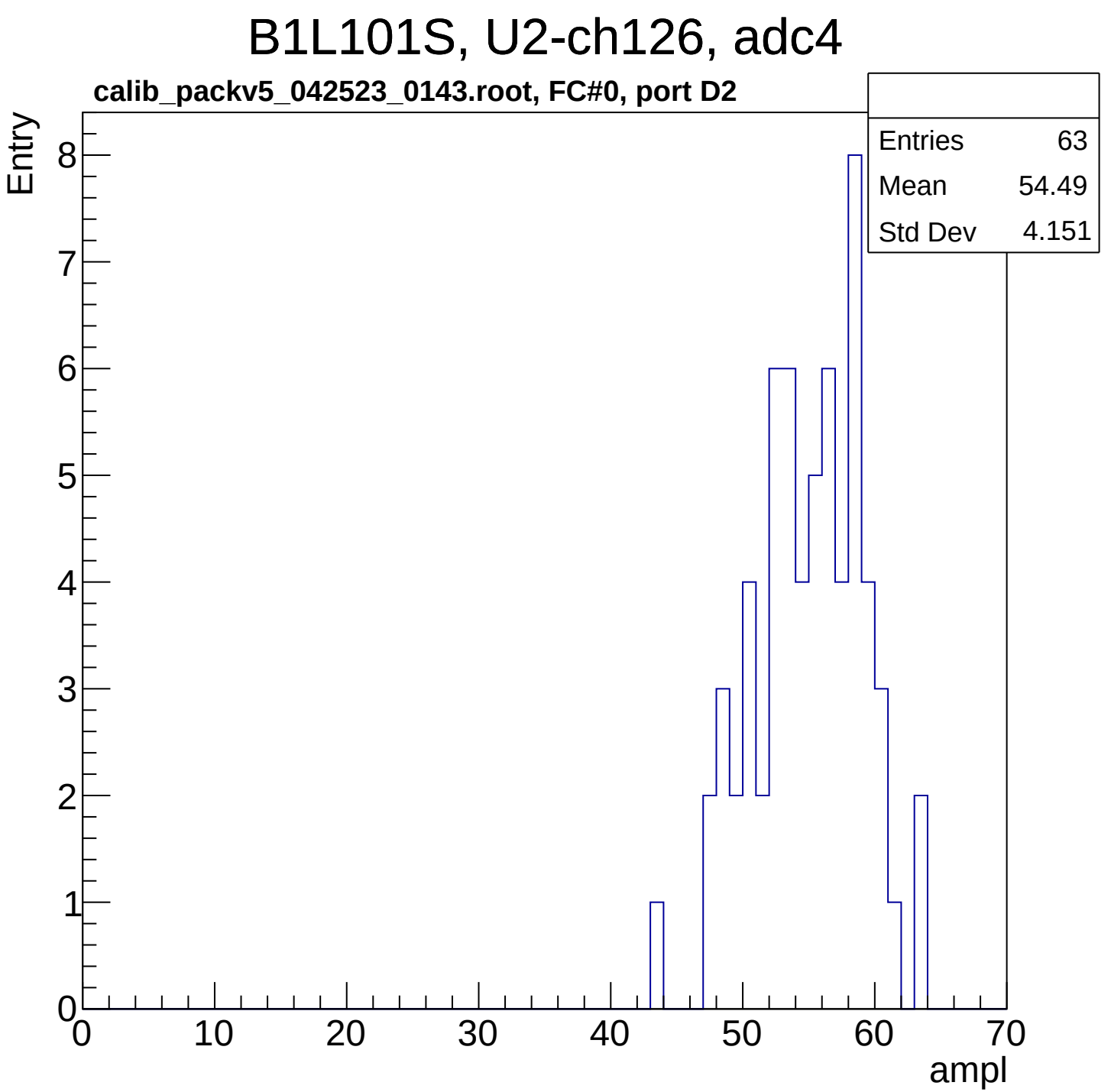

B1L101S, U2-ch125, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

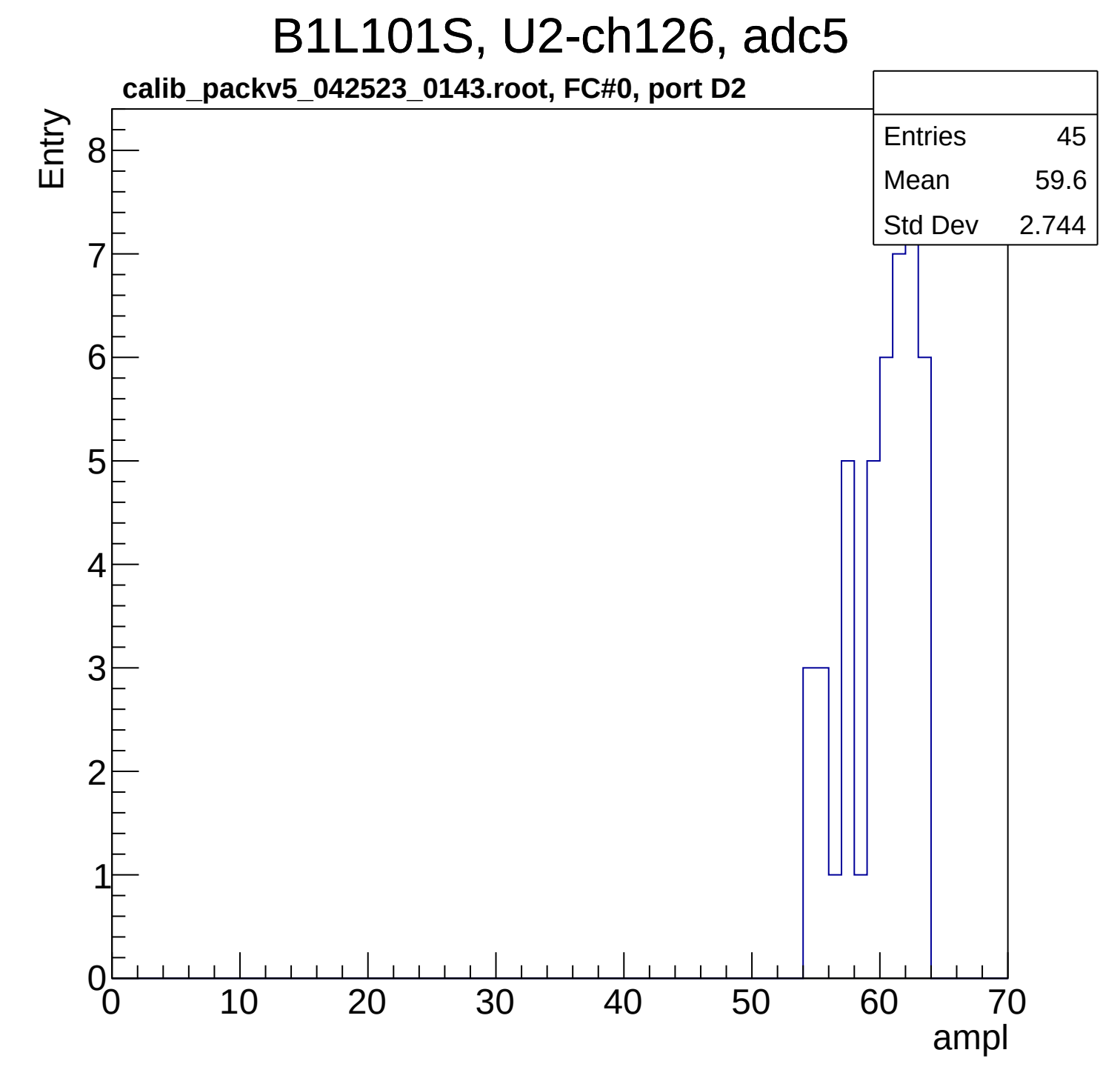

B1L101S, U2-ch126, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 29.07
Std Dev 6.112
Gaus mean : 30.6463
Gaus Width: 4.0233
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

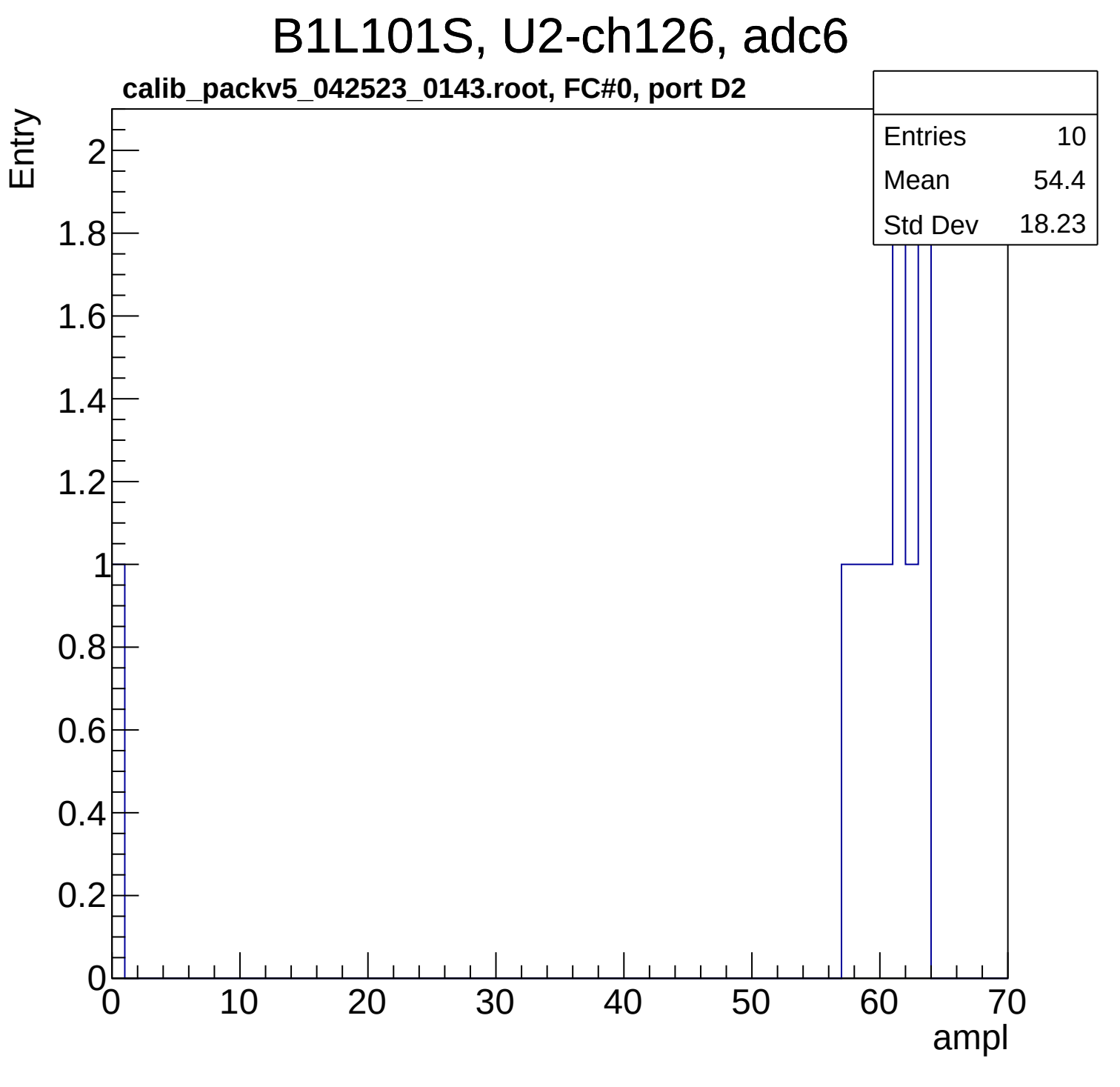

B1L101S, U2-ch126, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 71
Mean 36.69
Std Dev 3.507
Gaus mean : 36.9231
Gaus Width: 3.5024
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

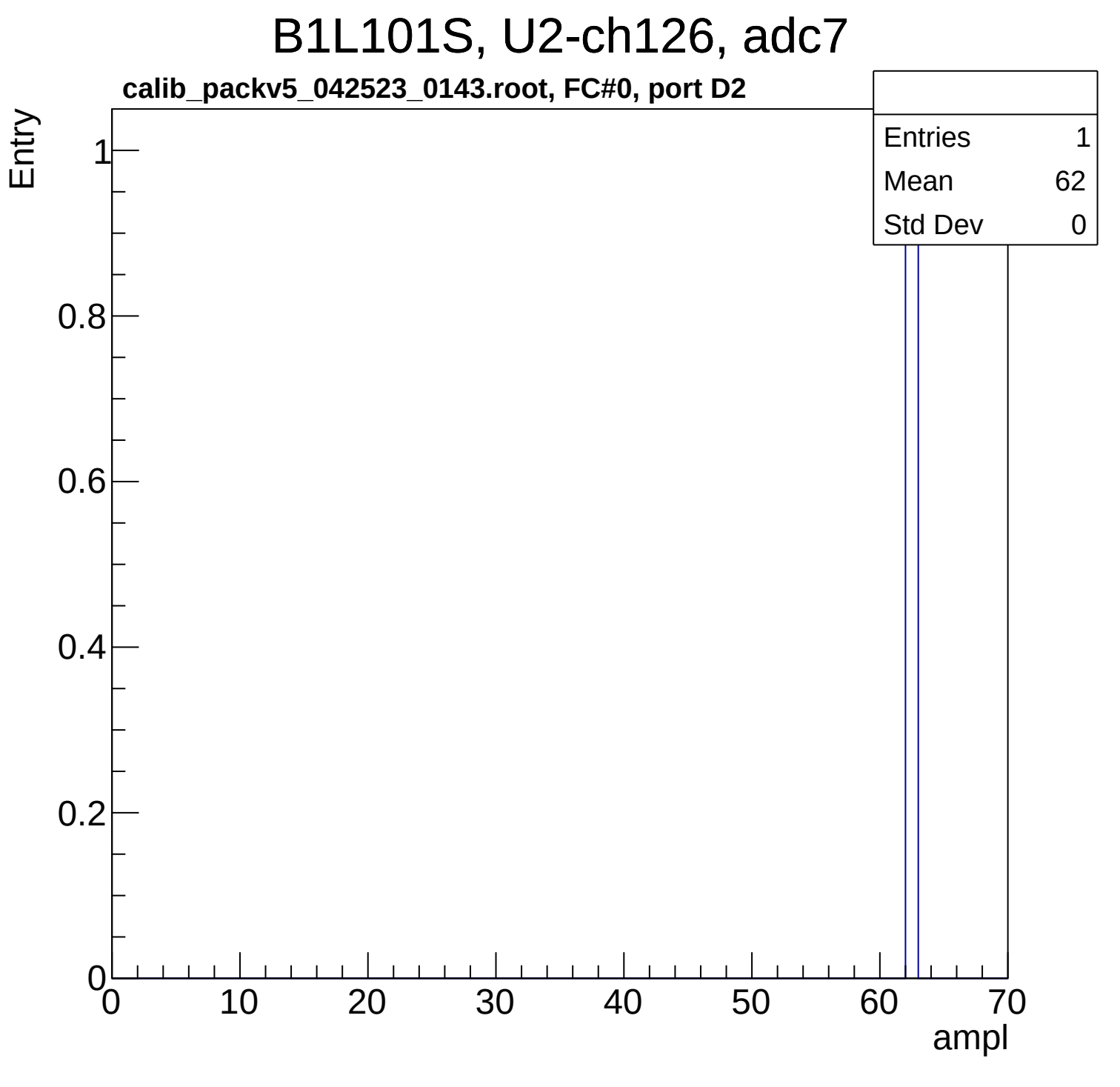

B1L101S, U2-ch126, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 57
Mean 43.11
Std Dev 3.611
Gaus mean : 43.3202
Gaus Width: 3.3865
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

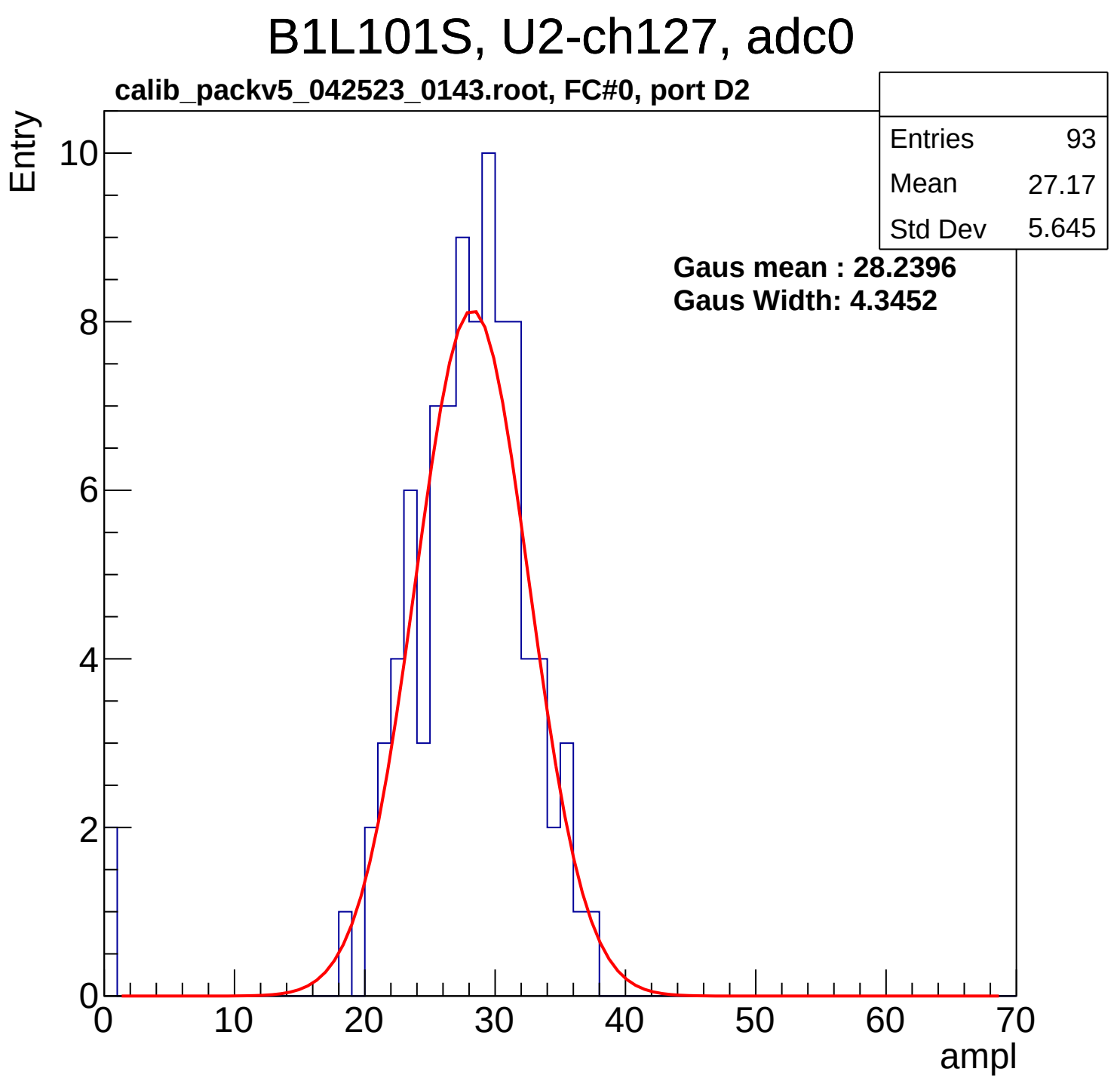

B1L101S, U2-ch126, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 58
Mean 49.28
Std Dev 3.513
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

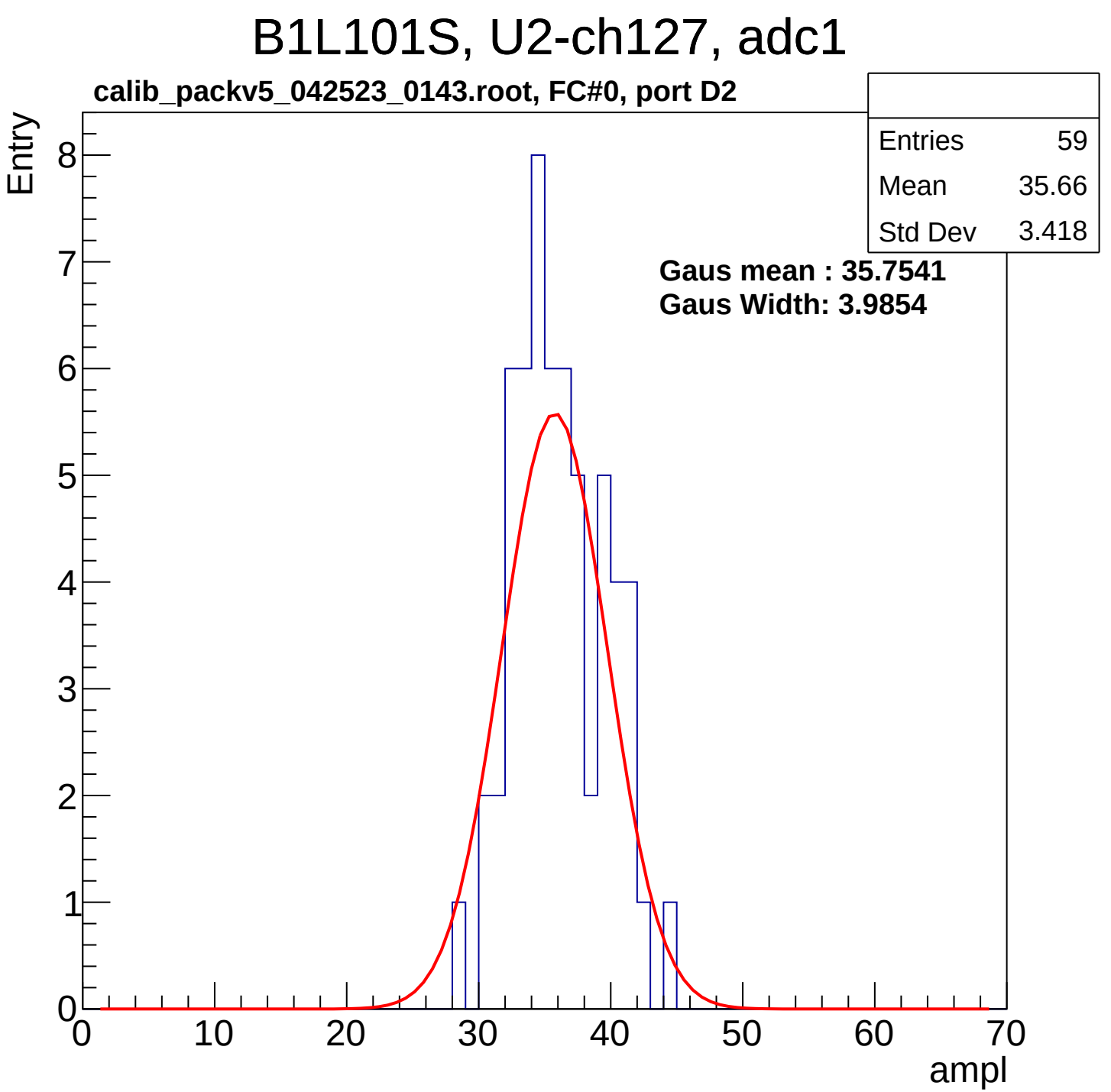

B1L101S, U2-ch126, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 54.49
Std Dev 4.151
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

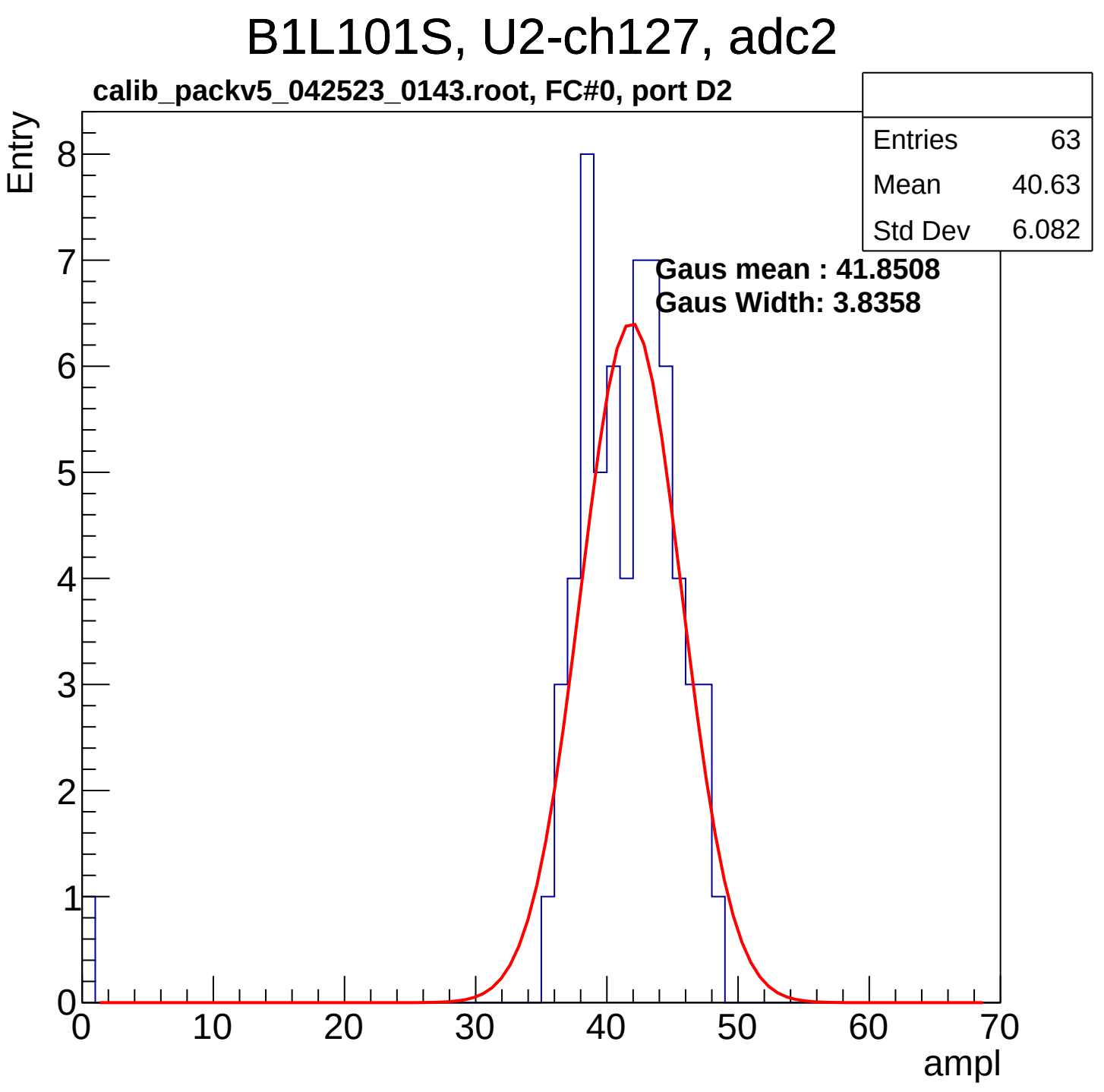

B1L101S, U2-ch126, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 45
Mean 59.6
Std Dev 2.744
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

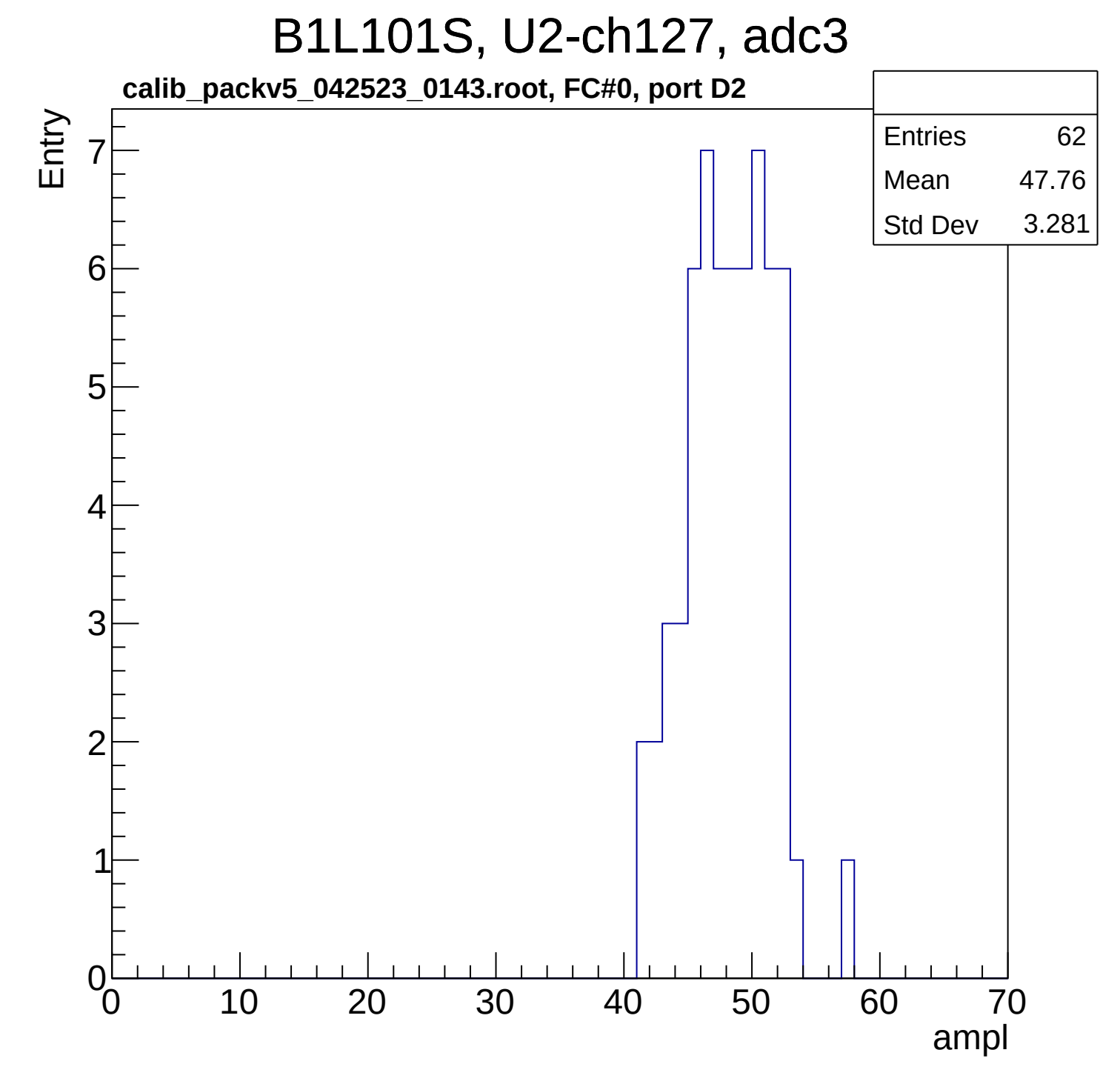

B1L101S, U2-ch126, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 10
Mean 54.4
Std Dev 18.23
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

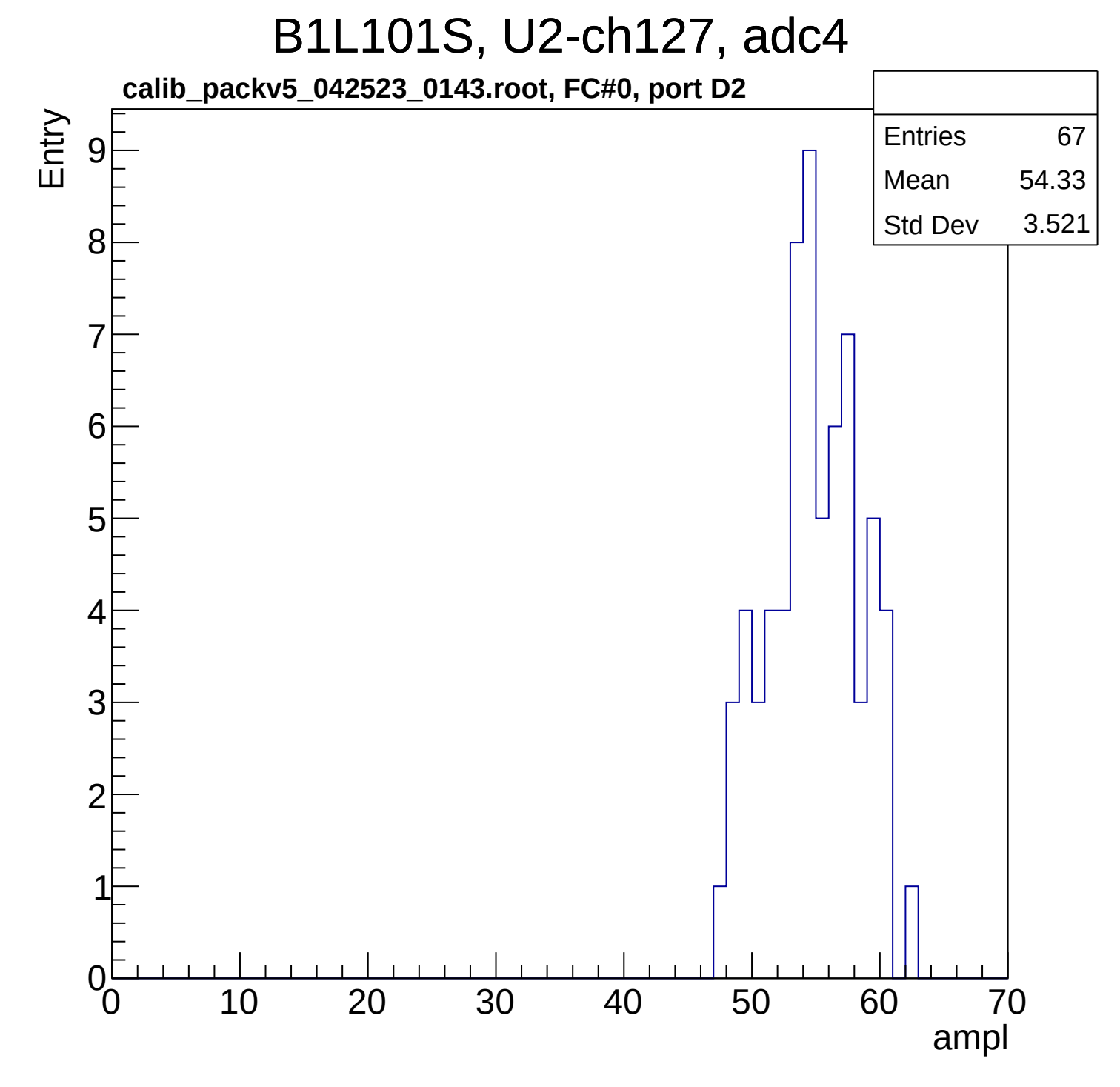

B1L101S, U2-ch126, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

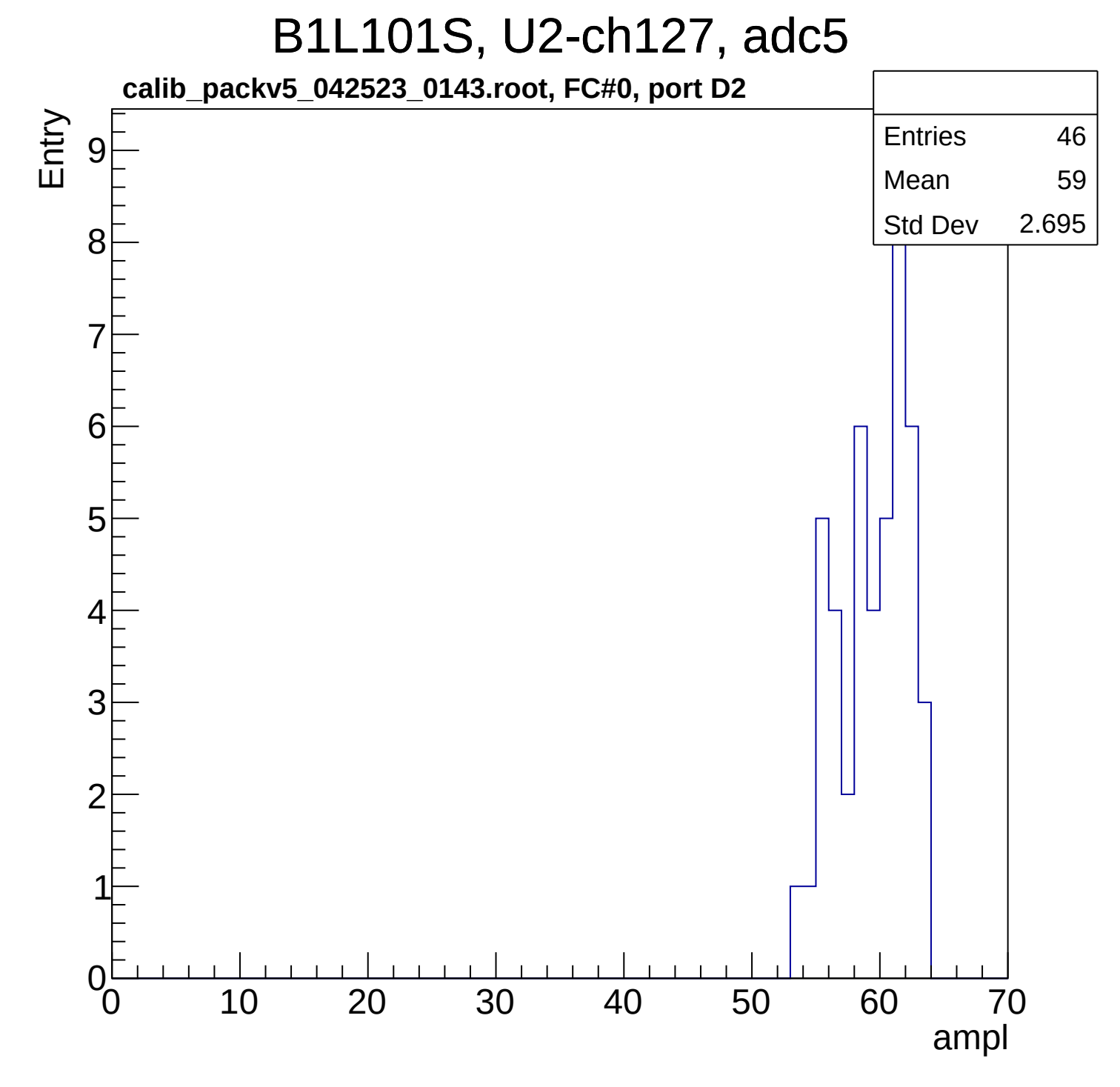

B1L101S, U2-ch127, adc0
calib_packv5_042523_0143.root, FC#0, port D2
Entries 93
Mean 27.17
Std Dev 5.645
Gaus mean : 28.2396
Gaus Width: 4.3452
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

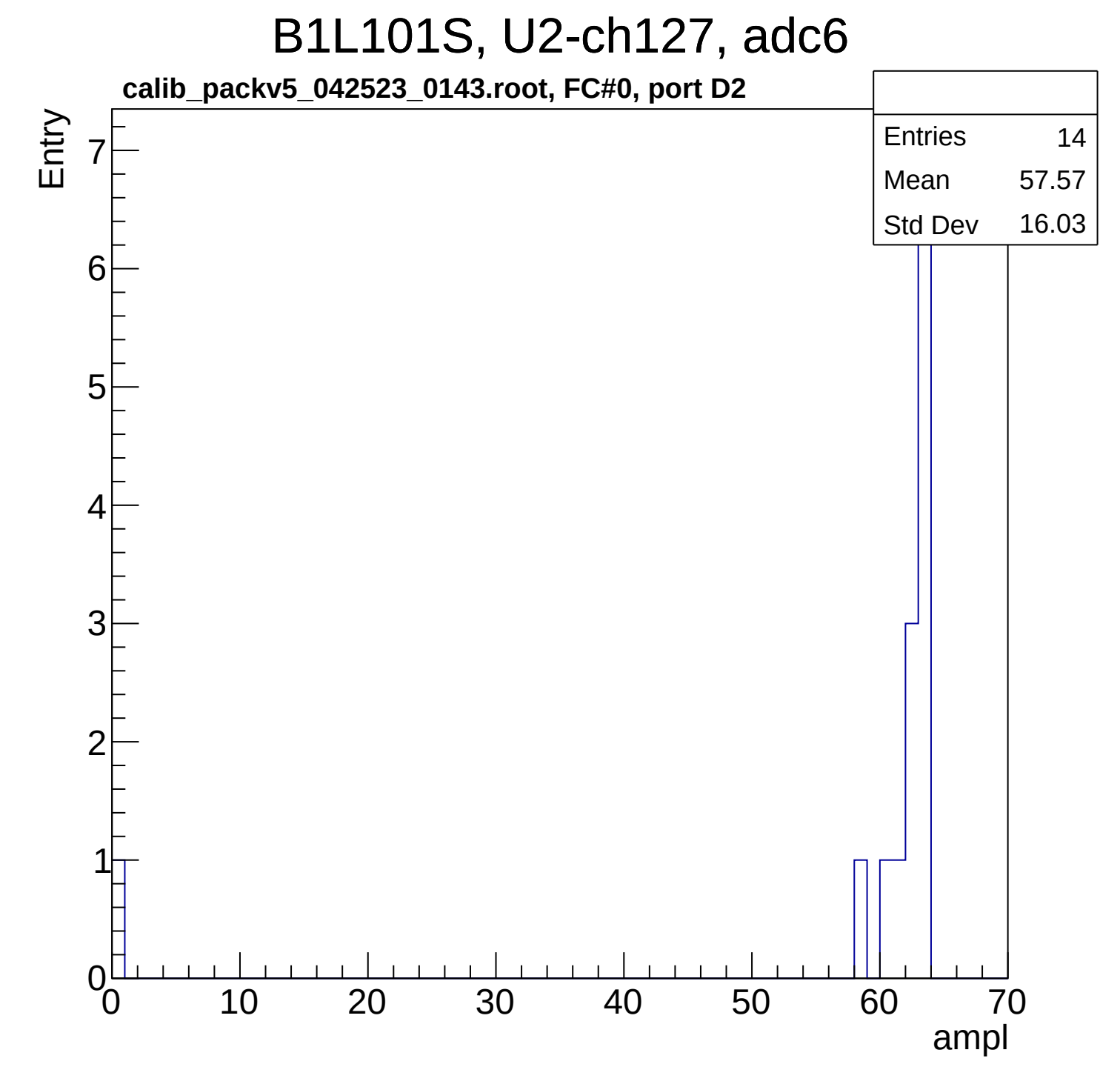

B1L101S, U2-ch127, adc1
calib_packv5_042523_0143.root, FC#0, port D2
Entries 59
Mean 35.66
Std Dev 3.418
Gaus mean : 35.7541
Gaus Width: 3.9854
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

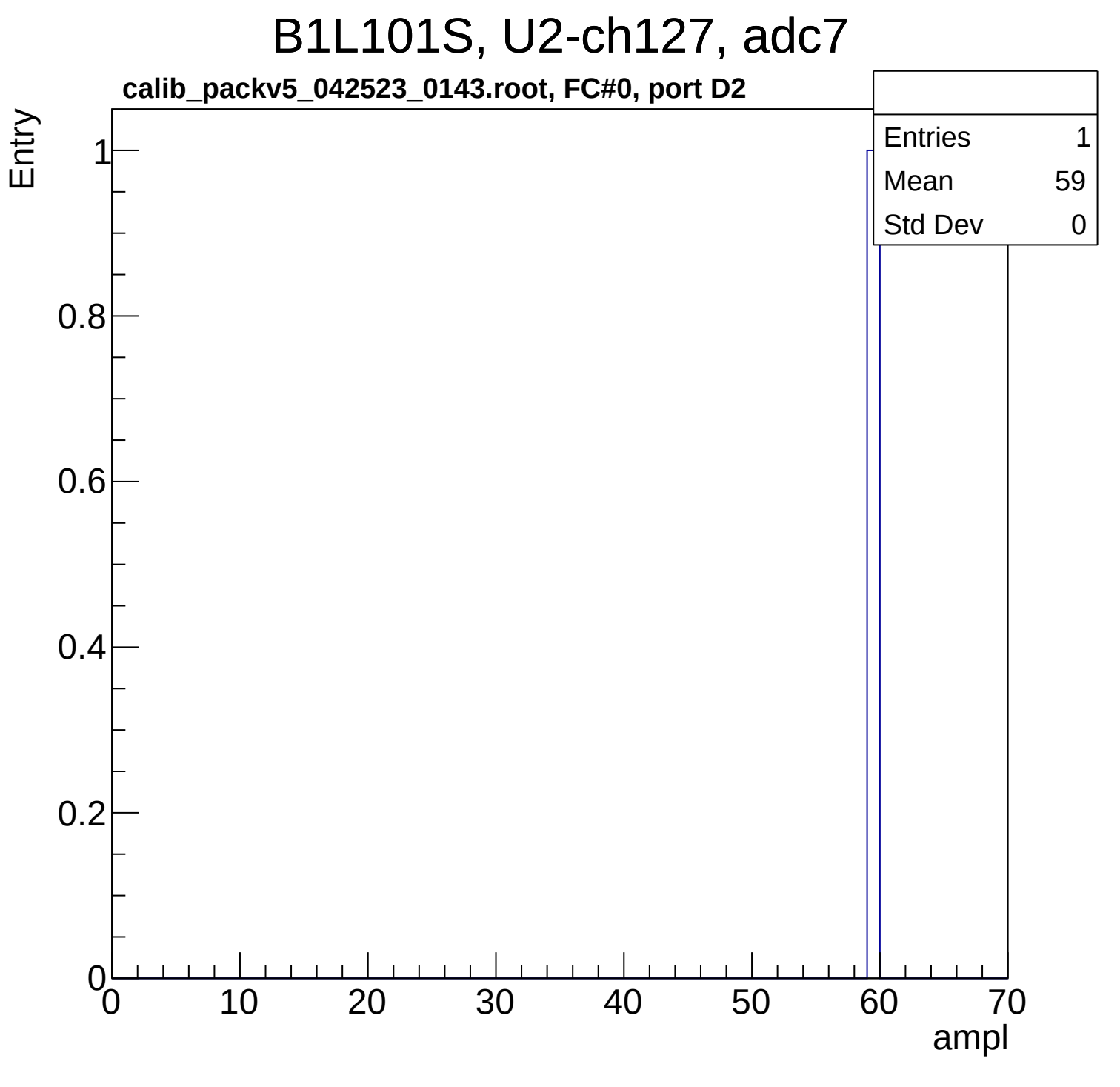

B1L101S, U2-ch127, adc2
calib_packv5_042523_0143.root, FC#0, port D2
Entries 63
Mean 40.63
Std Dev 6.082
Gaus mean : 41.8508
Gaus Width: 3.8358
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

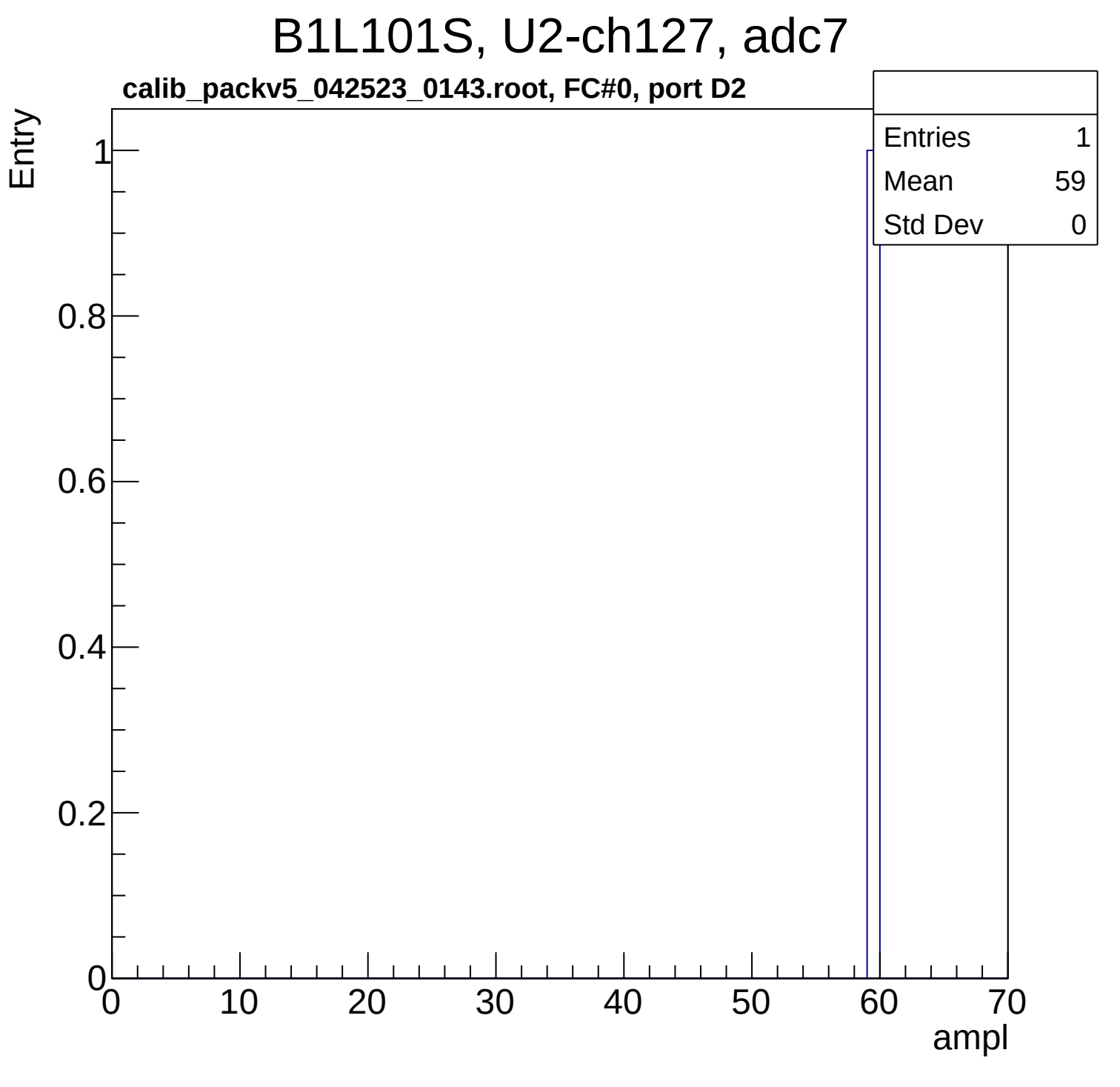

B1L101S, U2-ch127, adc3
calib_packv5_042523_0143.root, FC#0, port D2
Entries 62
Mean 47.76
Std Dev 3.281
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L101S, U2-ch127, adc4
calib_packv5_042523_0143.root, FC#0, port D2
Entries 67
Mean 54.33
Std Dev 3.521
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U2-ch127, adc5
calib_packv5_042523_0143.root, FC#0, port D2
Entries 46
Mean 59
Std Dev 2.695
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L101S, U2-ch127, adc6
calib_packv5_042523_0143.root, FC#0, port D2
Entries 14
Mean 57.57
Std Dev 16.03
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl


B1L101S, U2-ch127, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 59
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70


B1L101S, U2-ch127, adc7
calib_packv5_042523_0143.root, FC#0, port D2
Entries 1
Mean 59
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70