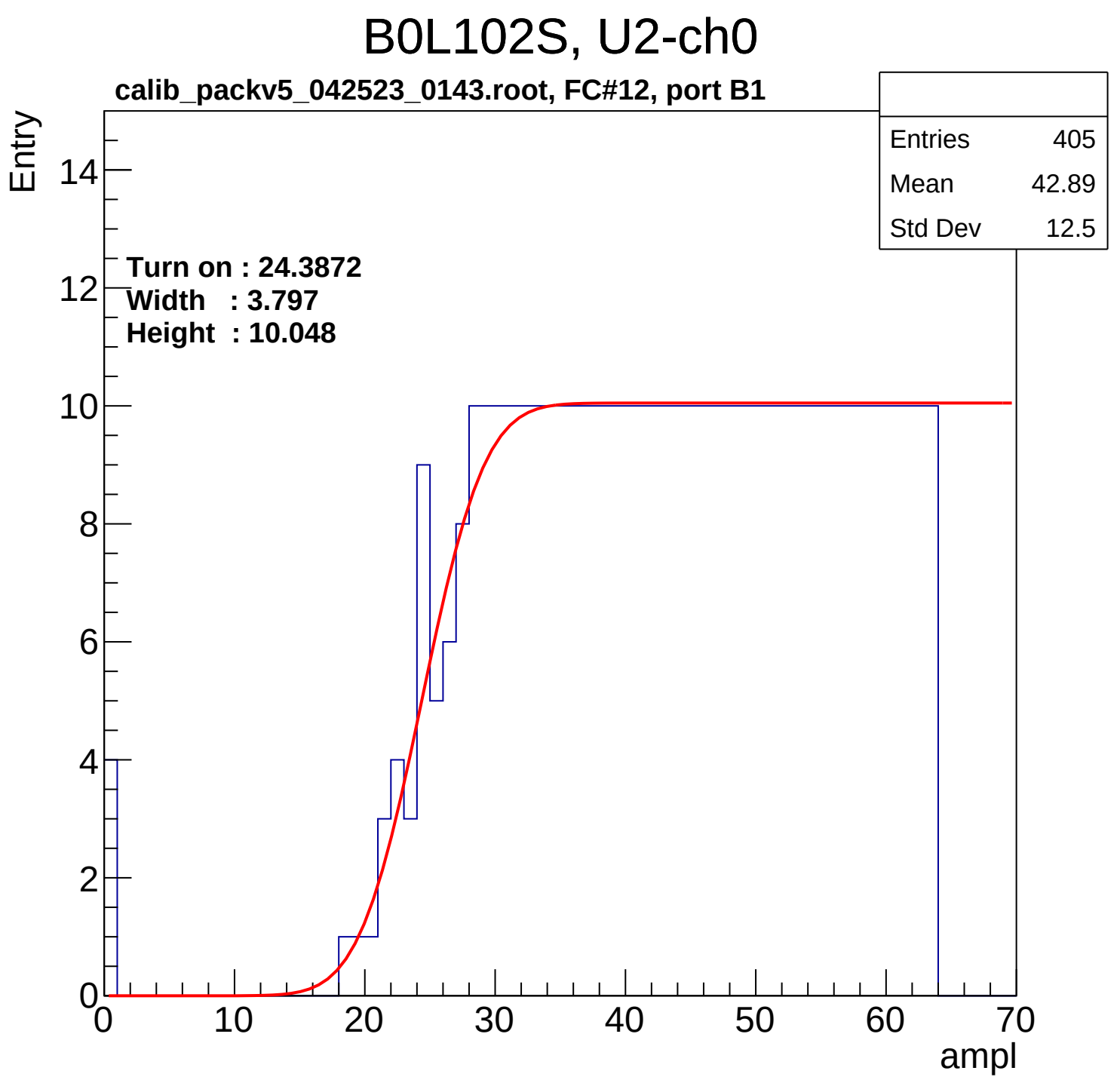
B0L102S, U2-ch0
calib_packv5_042523_0143.root, FC#12, port B1
Entries 405
Mean 42.89
Std Dev 12.5
Turn on : 24.3872
Width : 3.797
Height : 10.048
Entry
ampl
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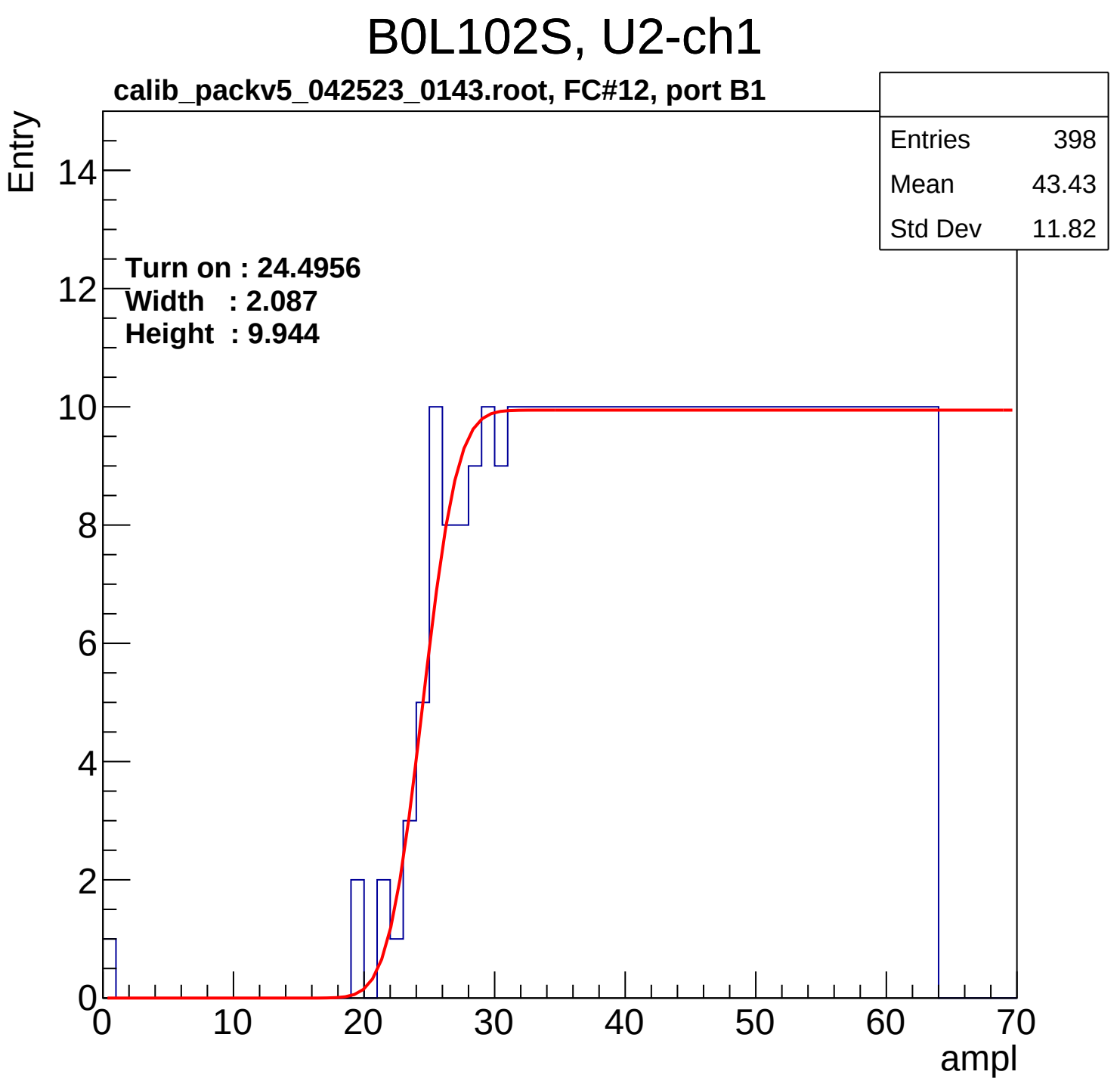
B0L102S, U2-ch1
calib_packv5_042523_0143.root, FC#12, port B1
Entries 398
Mean 43.43
Std Dev 11.82
Turn on : 24.4956
Width : 2.087
Height : 9.944
Entry
ampl
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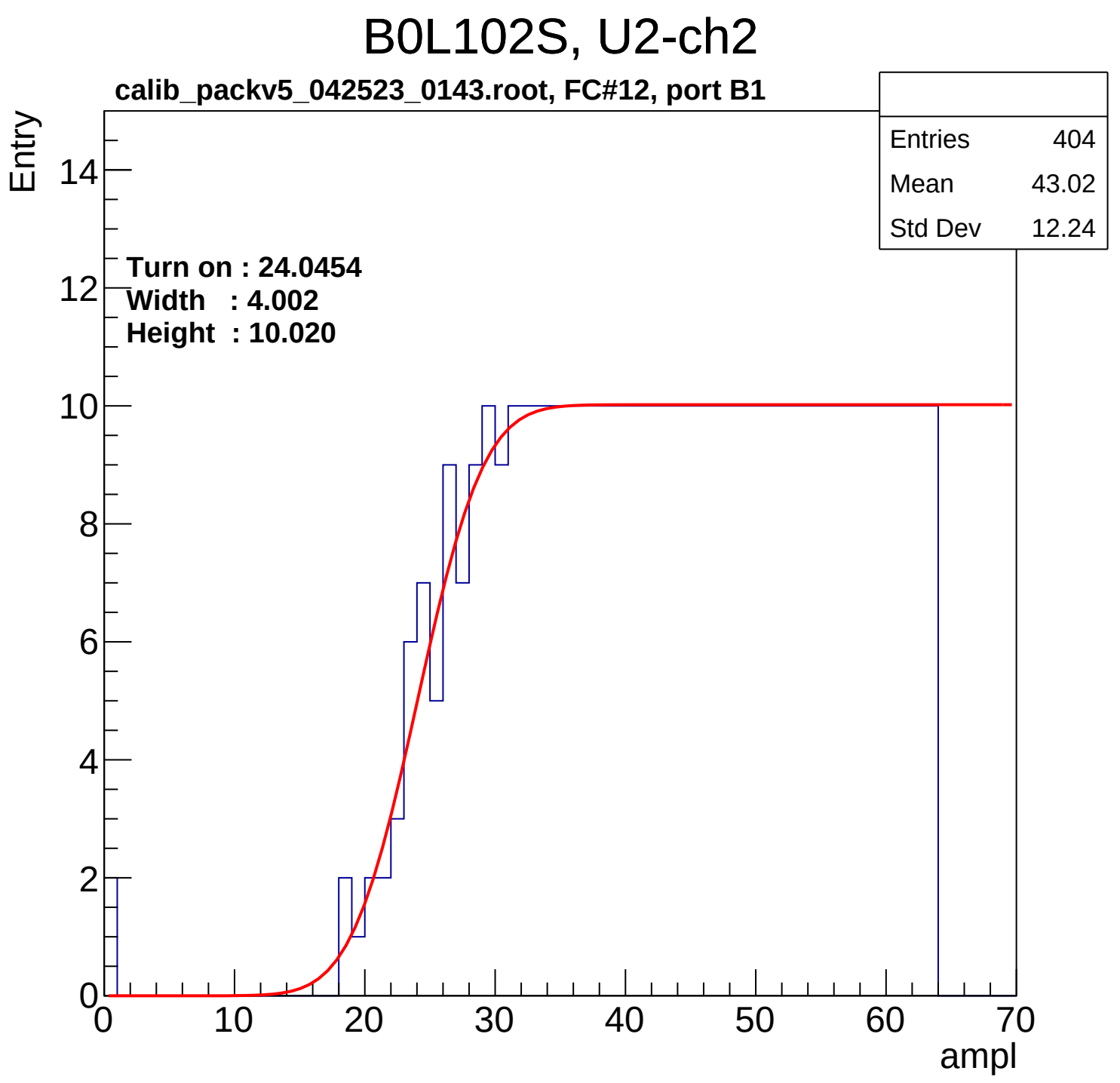
B0L102S, U2-ch2
calib_packv5_042523_0143.root, FC#12, port B1
Entries 404
Mean 43.02
Std Dev 12.24
Turn on : 24.0454
Width : 4.002
Height : 10.020
Entry
ampl
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2
4
6
8
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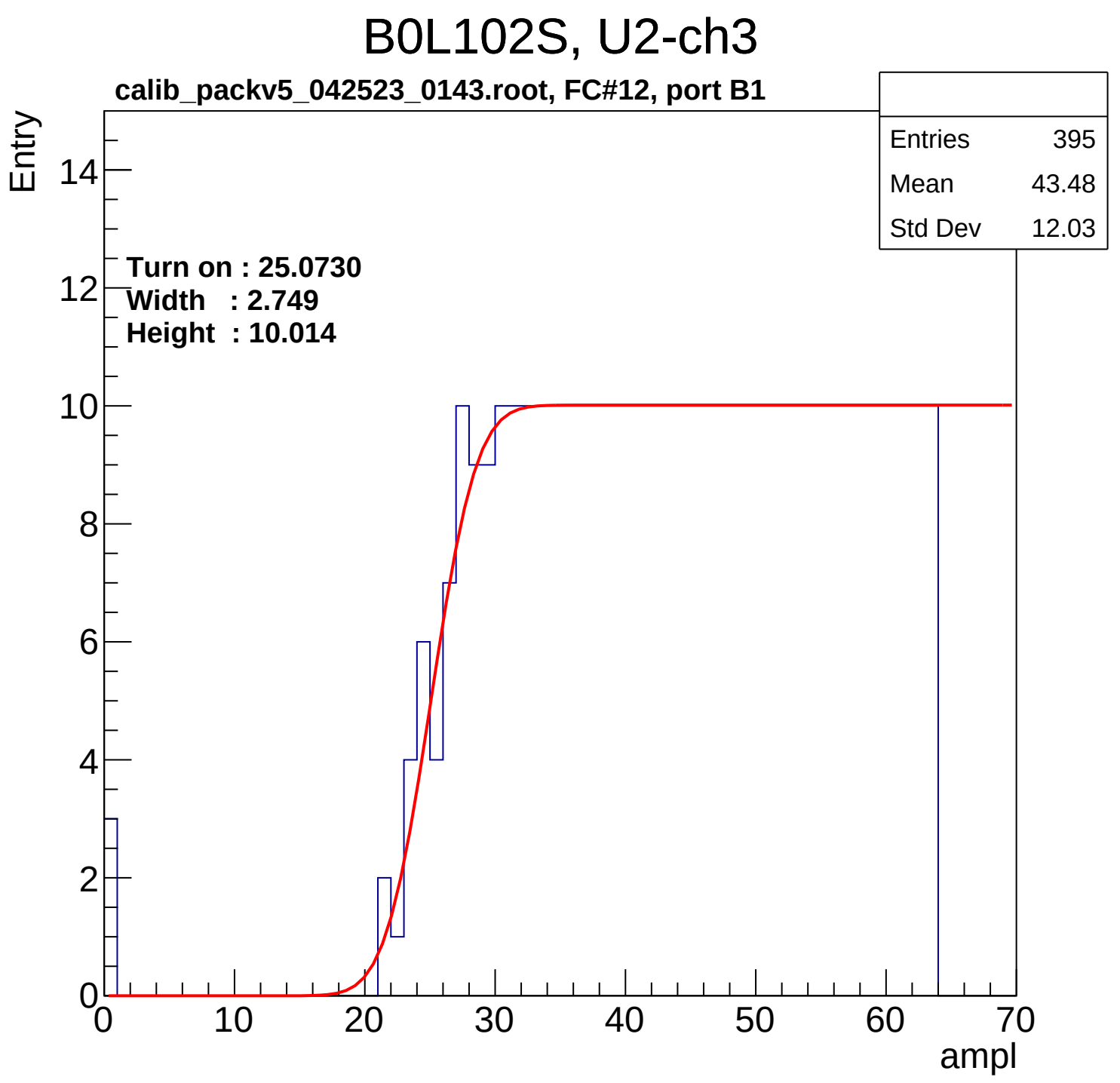
B0L102S, U2-ch3
calib_packv5_042523_0143.root, FC#12, port B1
Entries 395
Mean 43.48
Std Dev 12.03
Turn on : 25.0730
Width : 2.749
Height : 10.014
Entry
ampl
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2
4
6
8
10
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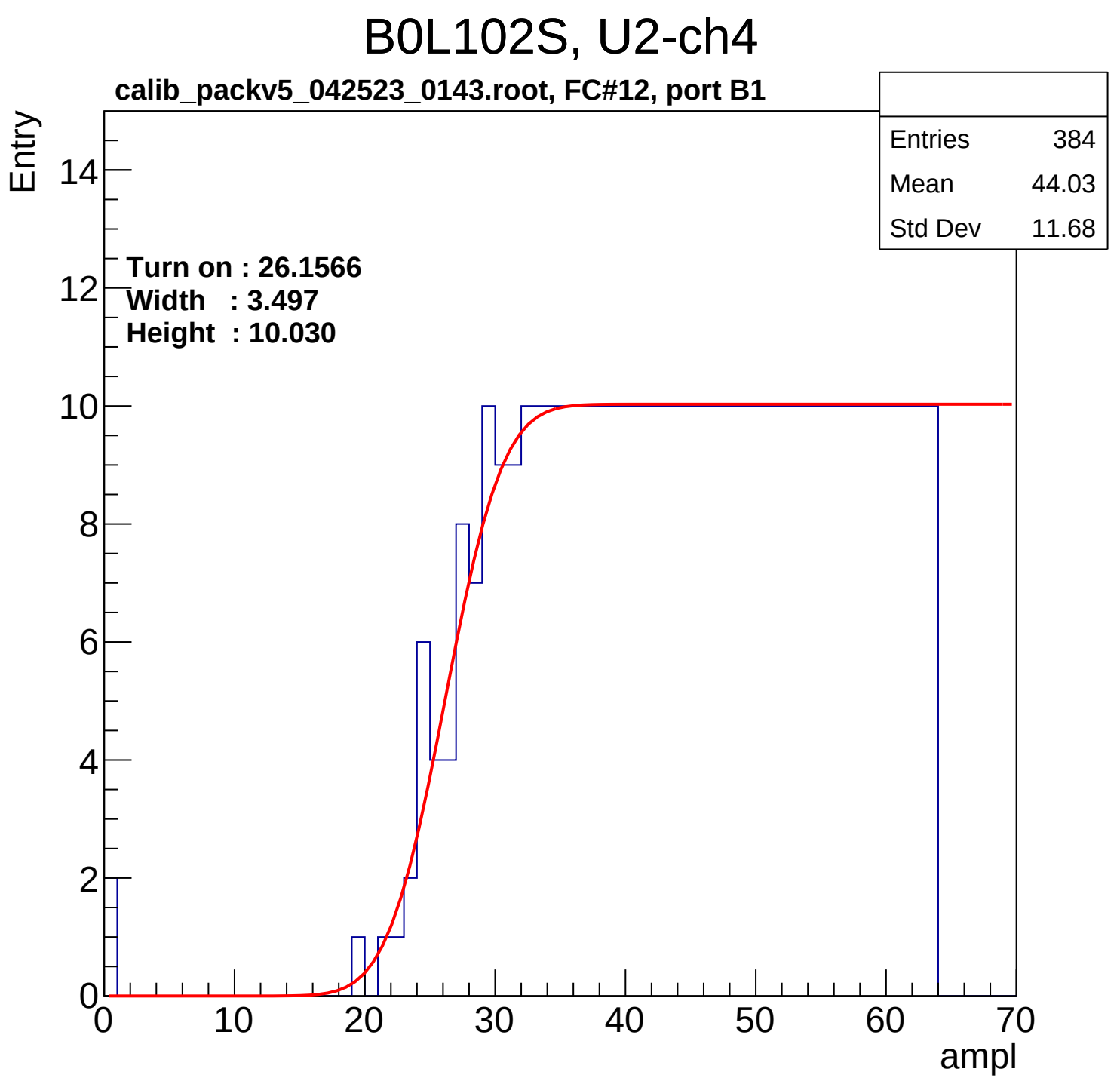
B0L102S, U2-ch4
calib_packv5_042523_0143.root, FC#12, port B1
Entries 384
Mean 44.03
Std Dev 11.68
Turn on : 26.1566
Width : 3.497
Height : 10.030
Entry
ampl
0
2
4
6
8
10
12
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0
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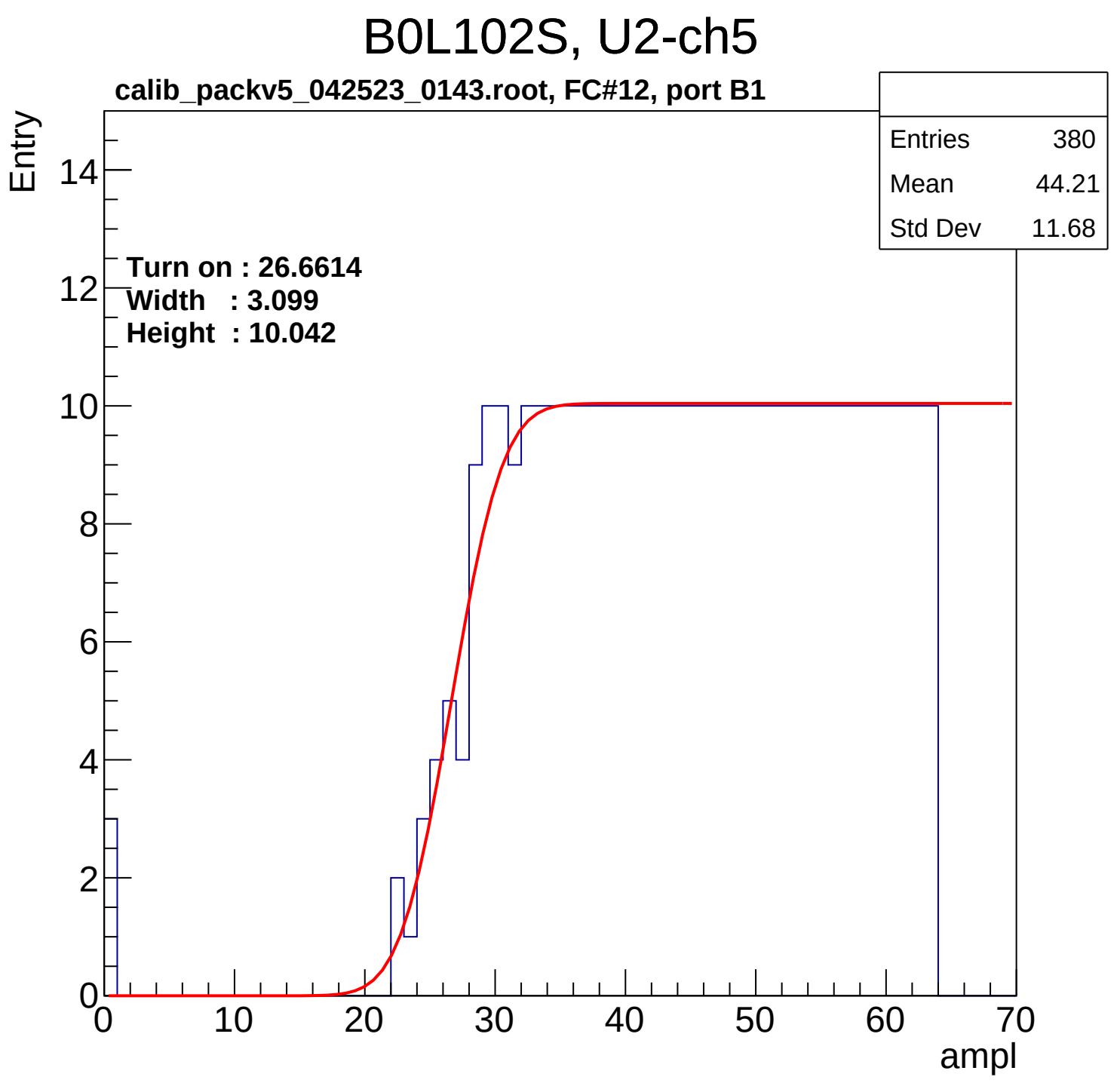
B0L102S, U2-ch5
calib_packv5_042523_0143.root, FC#12, port B1
Entries 380
Mean 44.21
Std Dev 11.68
Turn on : 26.6614
Width : 3.099
Height : 10.042
Entry
ampl
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6
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10
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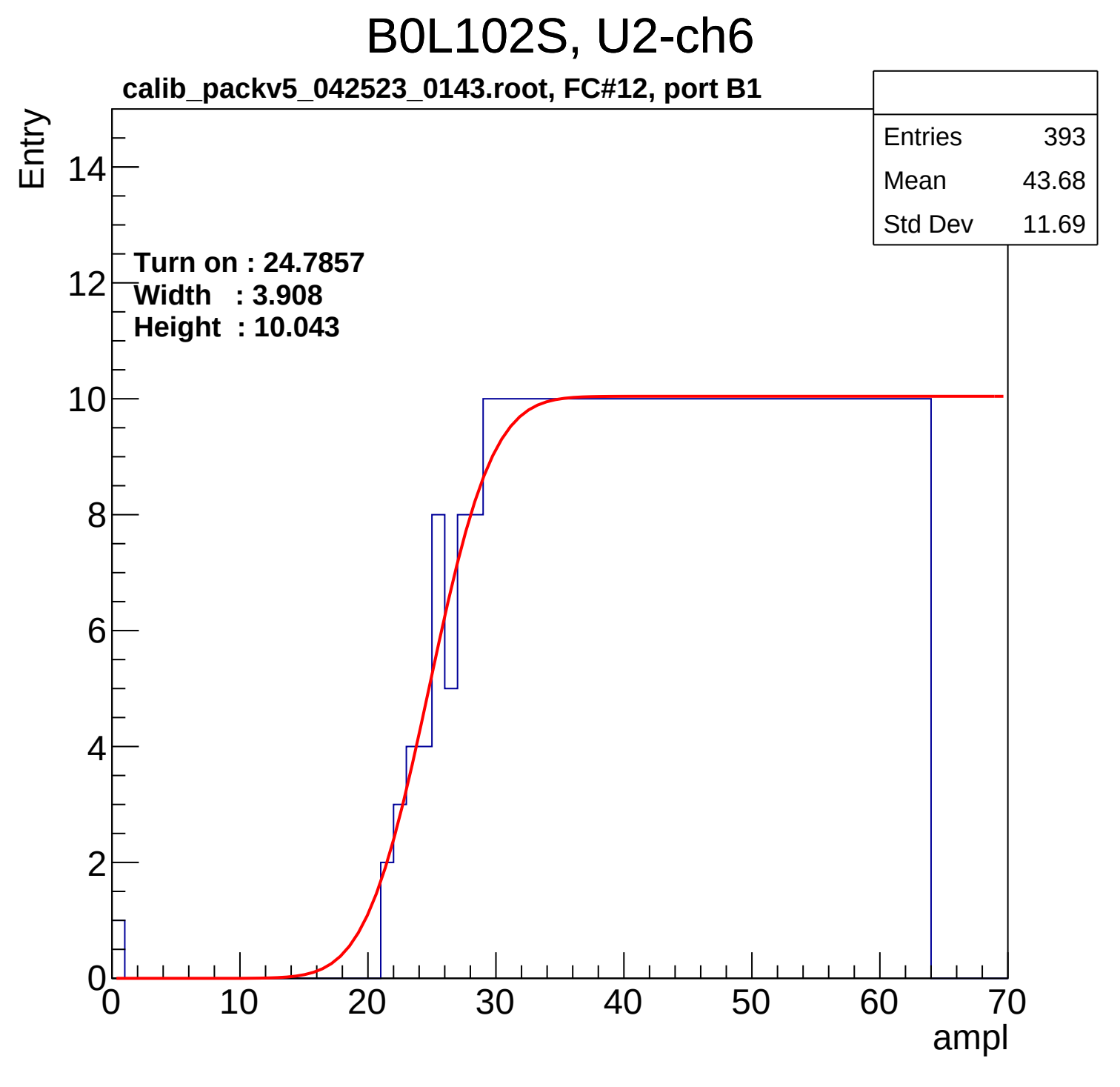
B0L102S, U2-ch6
calib_packv5_042523_0143.root, FC#12, port B1
Entries 393
Mean 43.68
Std Dev 11.69
Turn on : 24.7857
Width : 3.908
Height : 10.043
Entry
ampl
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4
6
8
10
12
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0
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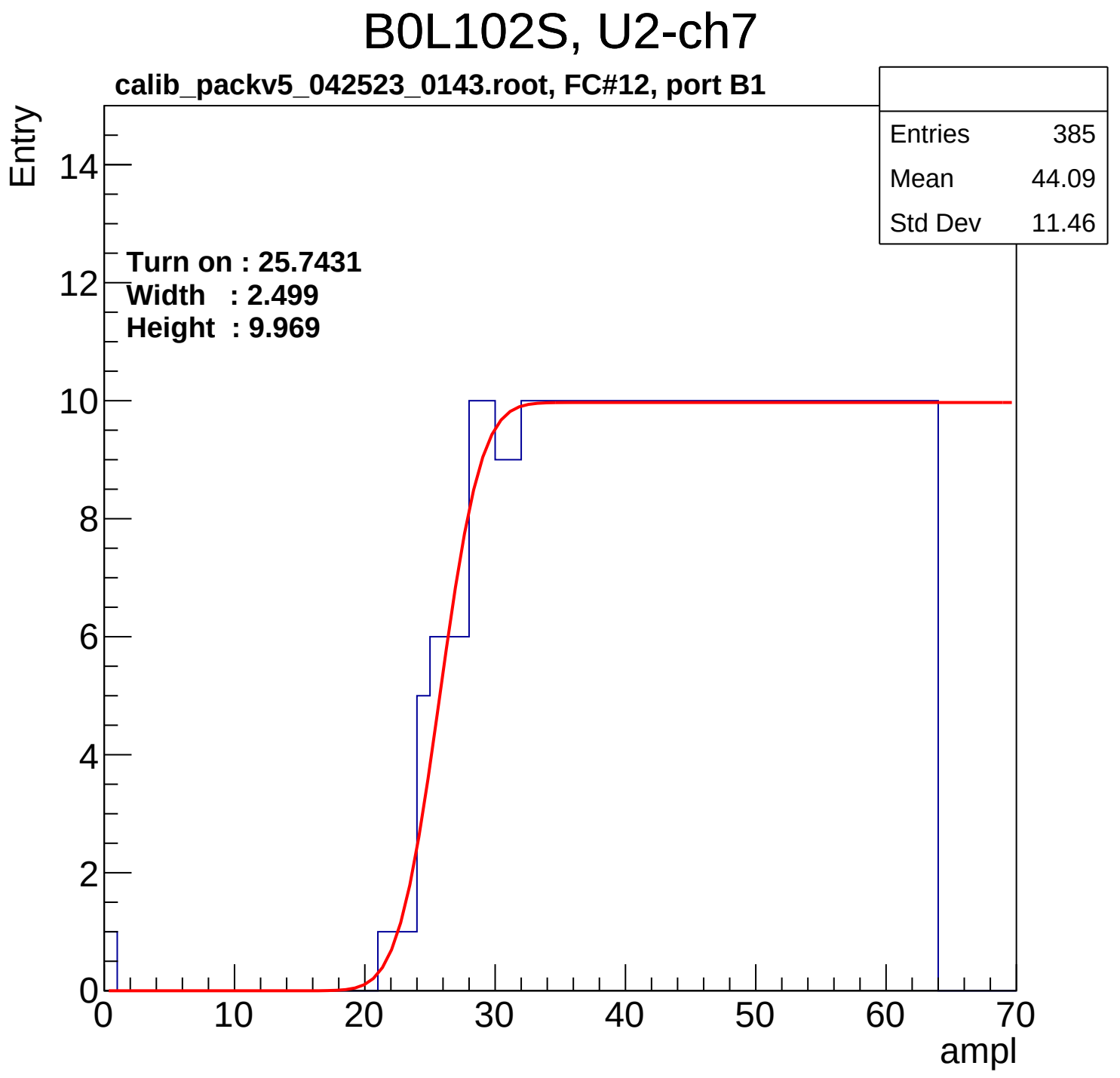
B0L102S, U2-ch7
calib_packv5_042523_0143.root, FC#12, port B1
Entries 385
Mean 44.09
Std Dev 11.46
Turn on : 25.7431
Width : 2.499
Height : 9.969
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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60
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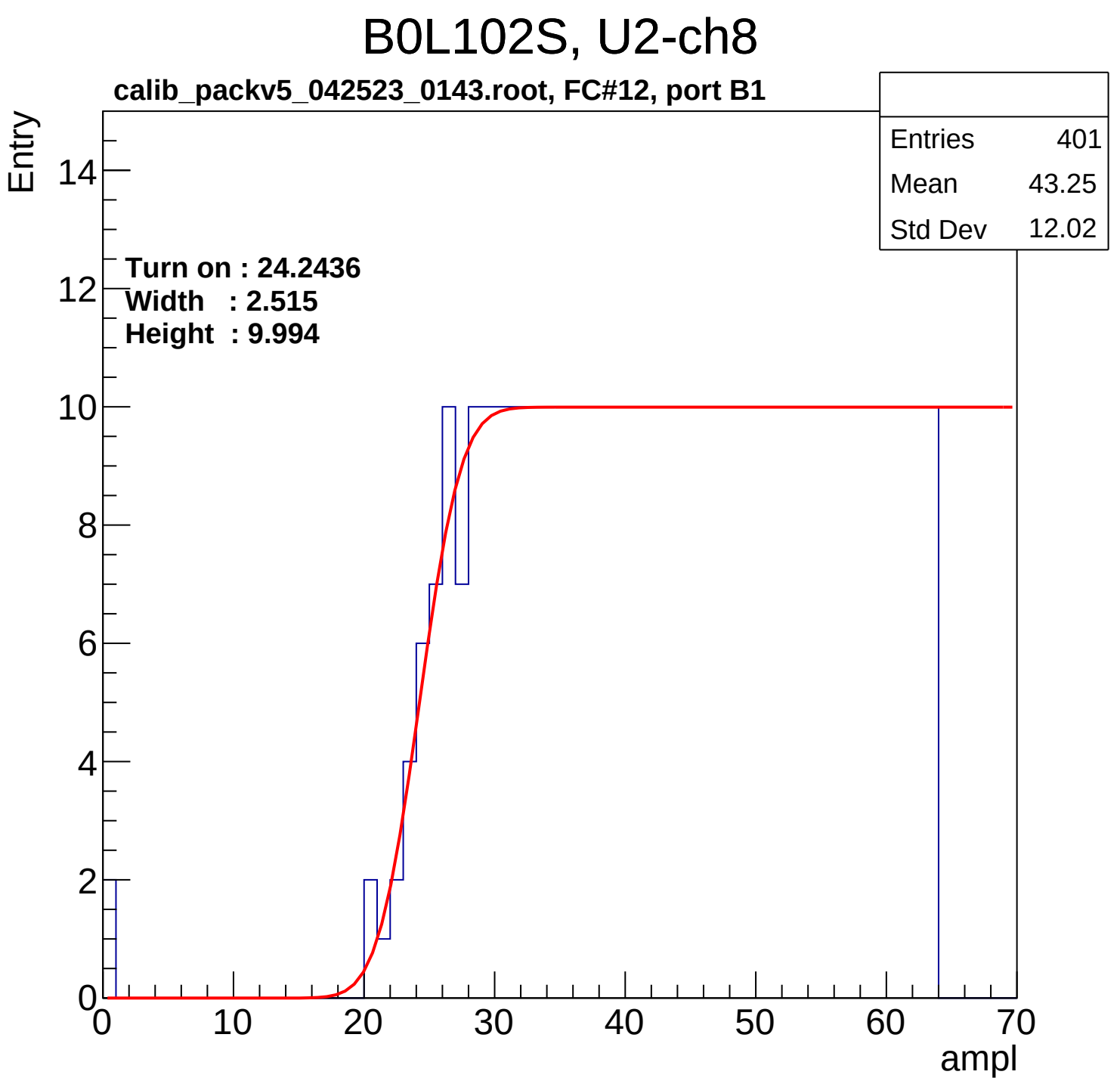
B0L102S, U2-ch8
calib_packv5_042523_0143.root, FC#12, port B1
Entries 401
Mean 43.25
Std Dev 12.02
Turn on : 24.2436
Width : 2.515
Height : 9.994
Entry
ampl
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2
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6
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10
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0
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60
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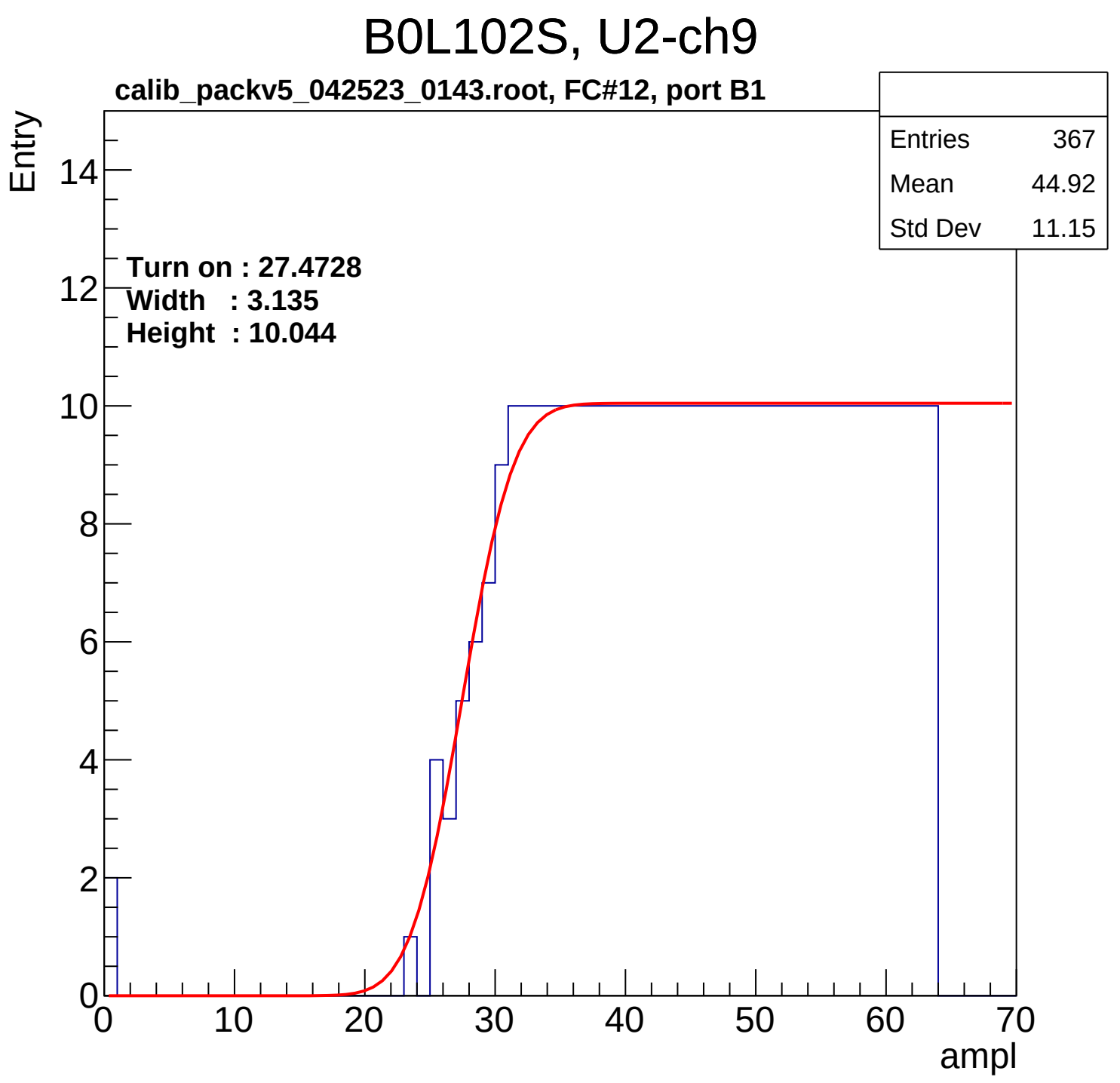
B0L102S, U2-ch9
calib_packv5_042523_0143.root, FC#12, port B1
Entries 367
Mean 44.92
Std Dev 11.15
Turn on : 27.4728
Width : 3.135
Height : 10.044
Entry
ampl
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4
6
8
10
12
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0
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20
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60
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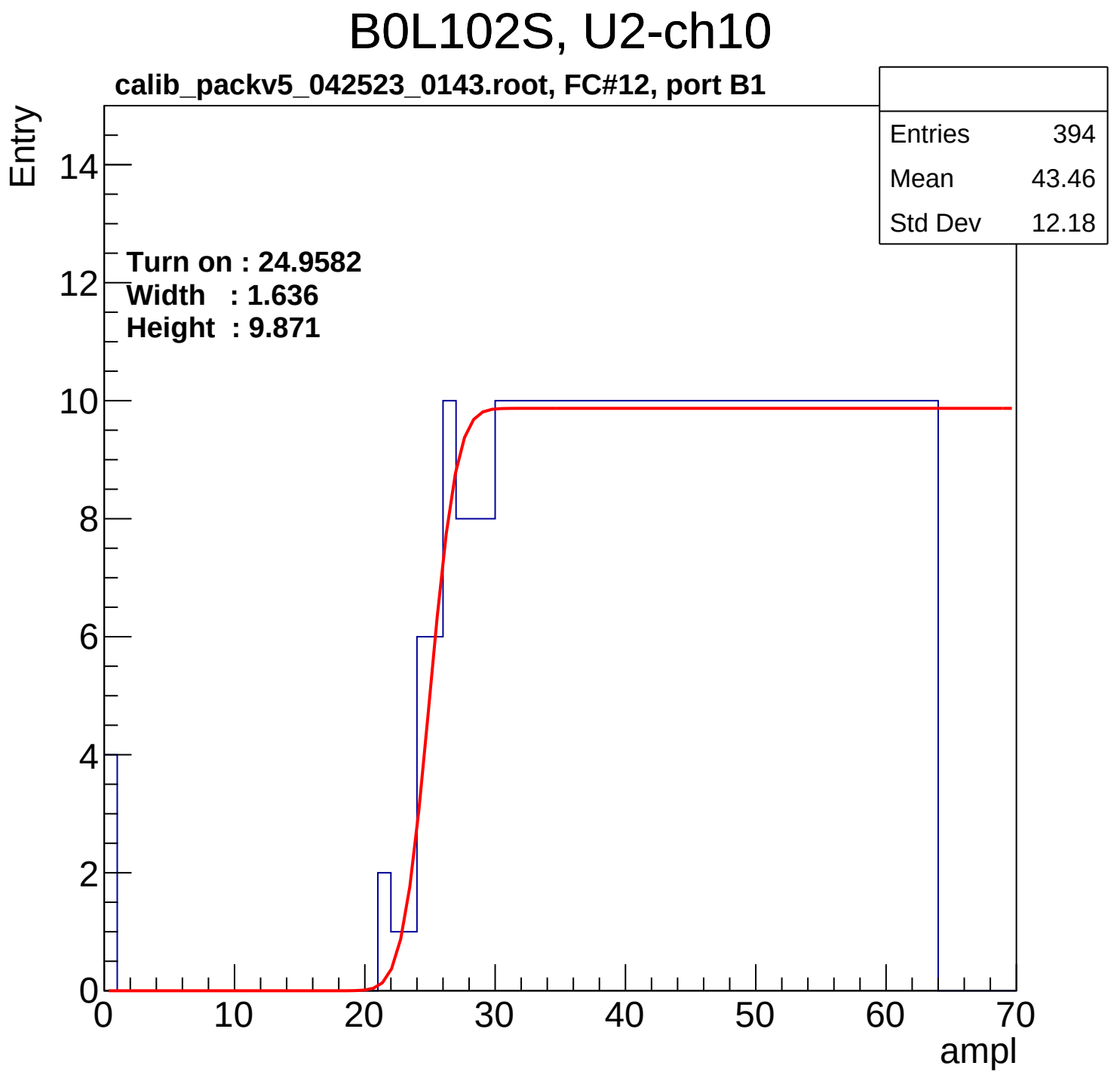
B0L102S, U2-ch10
calib_packv5_042523_0143.root, FC#12, port B1
Entries 394
Mean 43.46
Std Dev 12.18
Turn on : 24.9582
Width : 1.636
Height : 9.871
Entry
ampl
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2
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6
8
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12
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0
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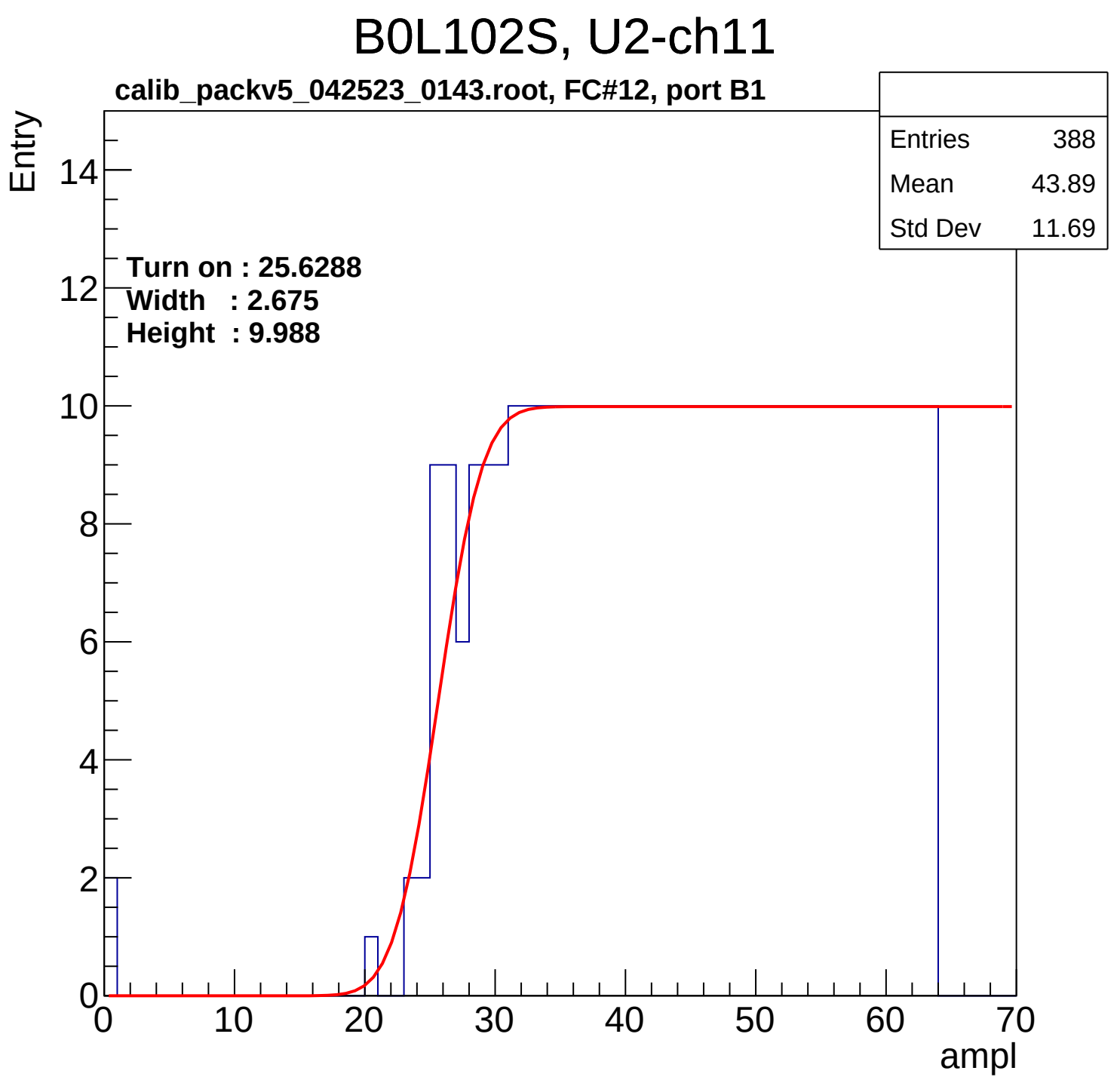
B0L102S, U2-ch11
calib_packv5_042523_0143.root, FC#12, port B1
Entries 388
Mean 43.89
Std Dev 11.69
Turn on : 25.6288
Width : 2.675
Height : 9.988
Entry
ampl
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2
4
6
8
10
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0
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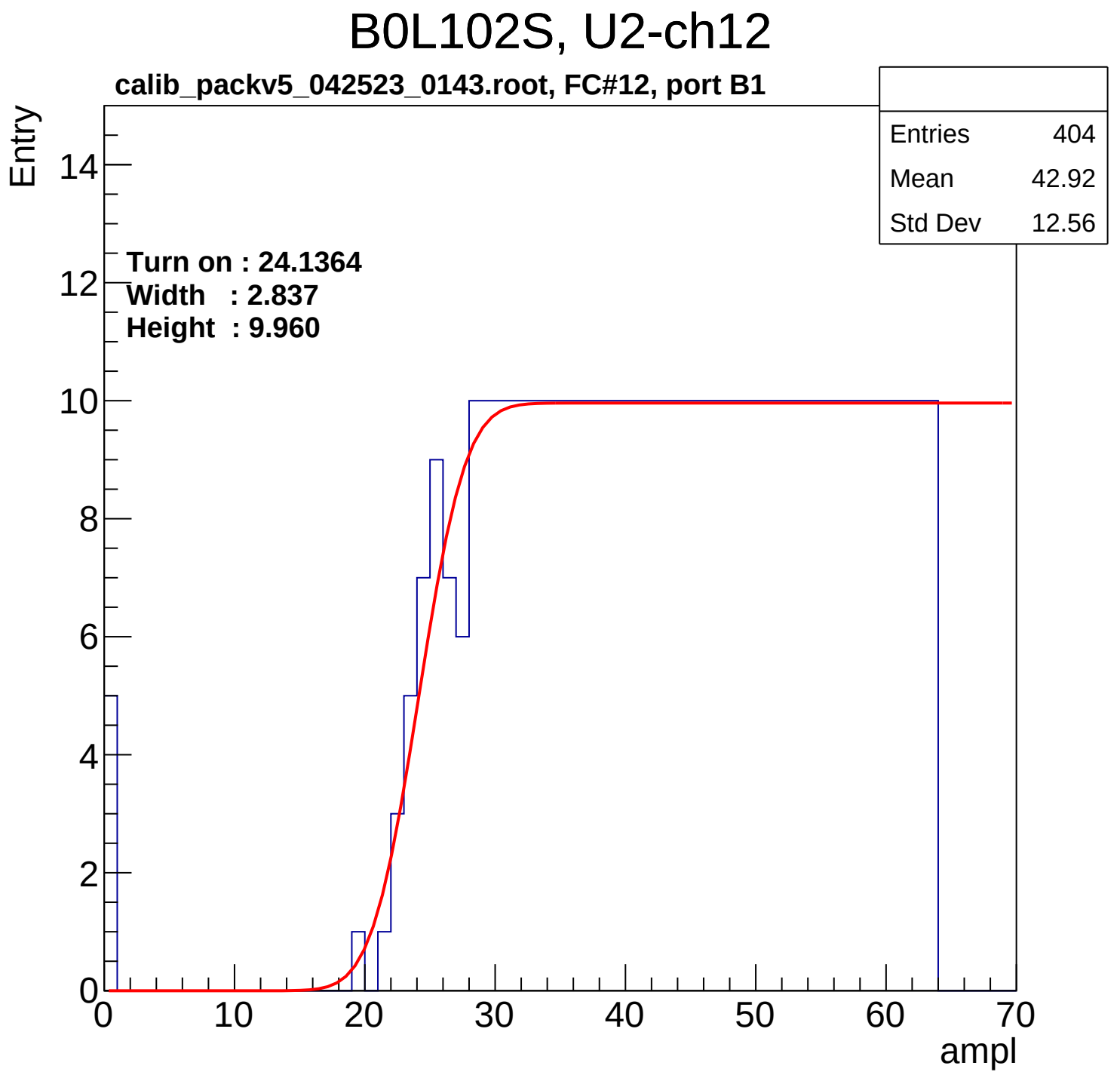
B0L102S, U2-ch12
calib_packv5_042523_0143.root, FC#12, port B1
Entries 404
Mean 42.92
Std Dev 12.56
Turn on : 24.1364
Width : 2.837
Height : 9.960
Entry
ampl
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2
4
6
8
10
12
14
0
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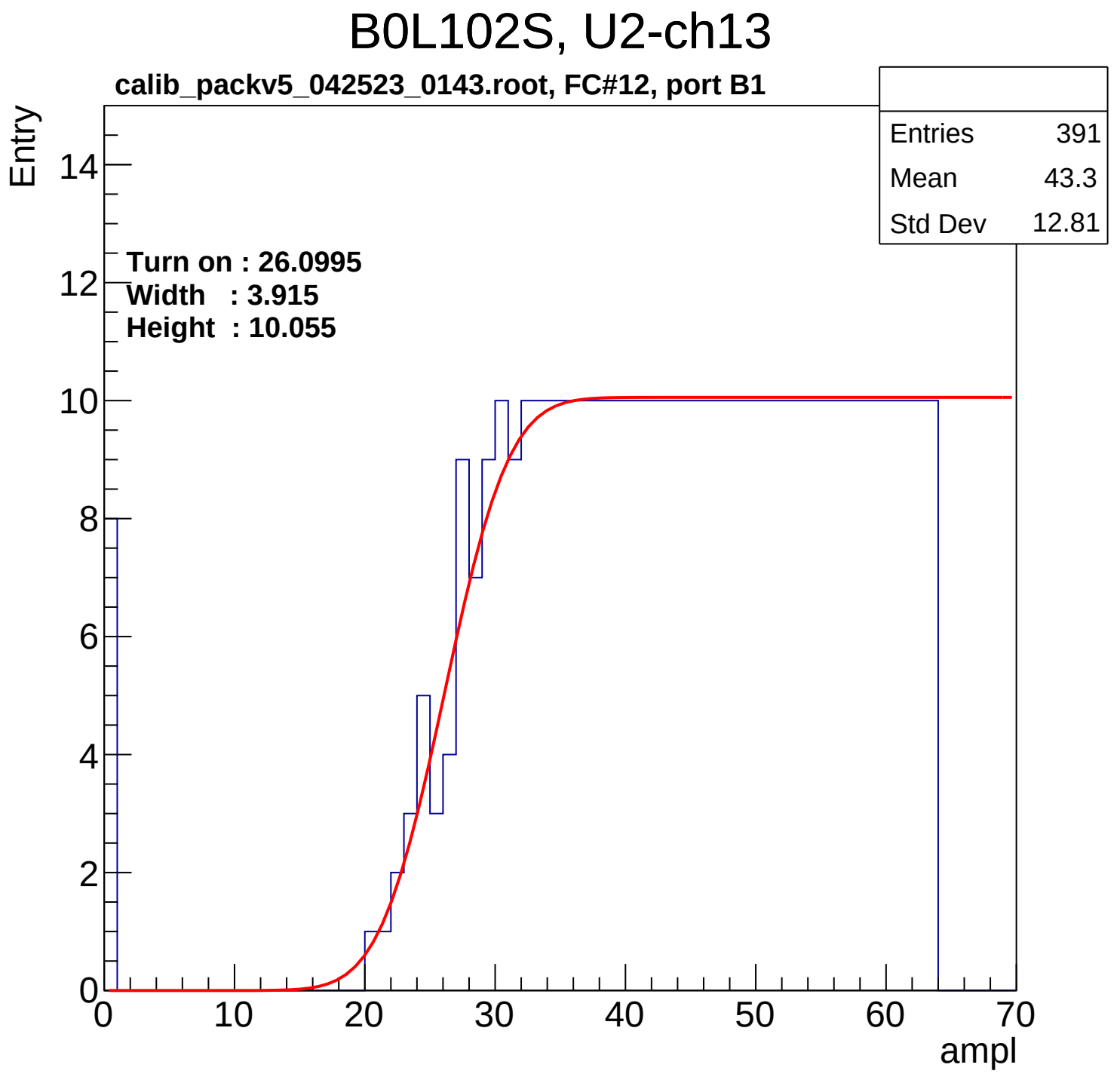
B0L102S, U2-ch13
calib_packv5_042523_0143.root, FC#12, port B1
Entries 391
Mean 43.3
Std Dev 12.81
Turn on : 26.0995
Width : 3.915
Height : 10.055
Entry
ampl
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4
6
8
10
12
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0
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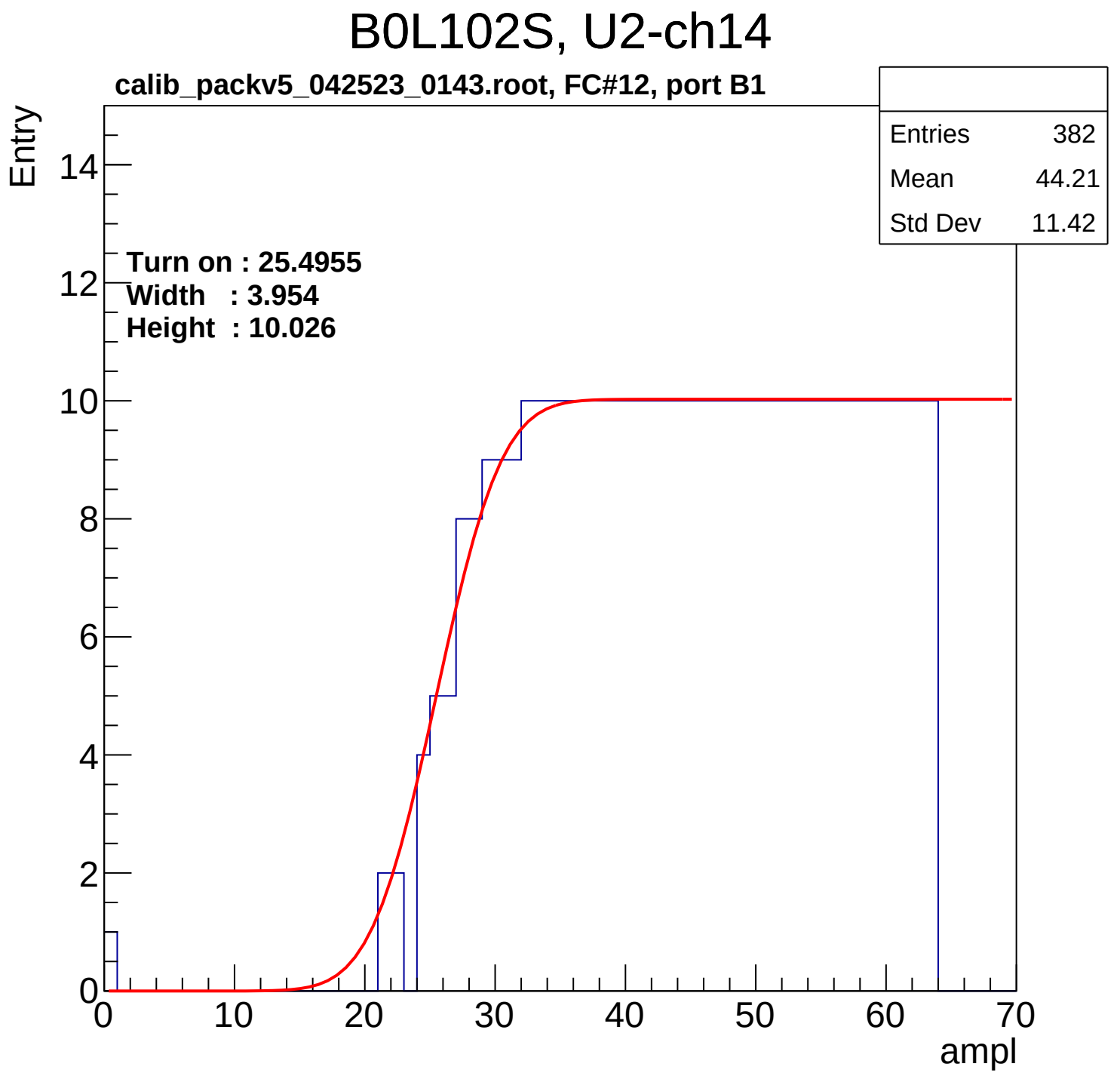
B0L102S, U2-ch14
calib_packv5_042523_0143.root, FC#12, port B1
Entries 382
Mean 44.21
Std Dev 11.42
Turn on : 25.4955
Width : 3.954
Height : 10.026
Entry
ampl
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6
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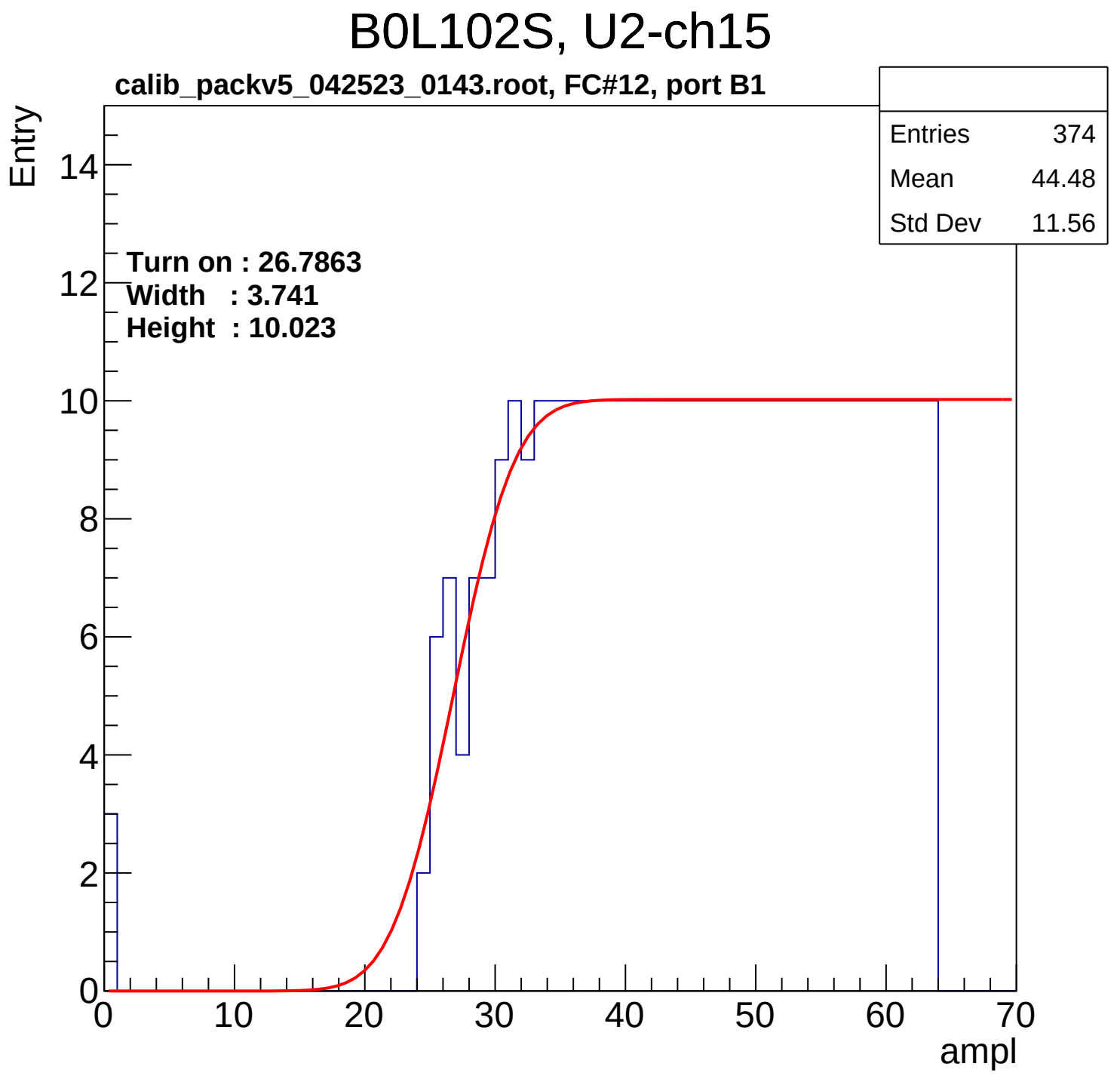
B0L102S, U2-ch15
calib_packv5_042523_0143.root, FC#12, port B1
Entries 374
Mean 44.48
Std Dev 11.56
Turn on : 26.7863
Width : 3.741
Height : 10.023
Entry
ampl
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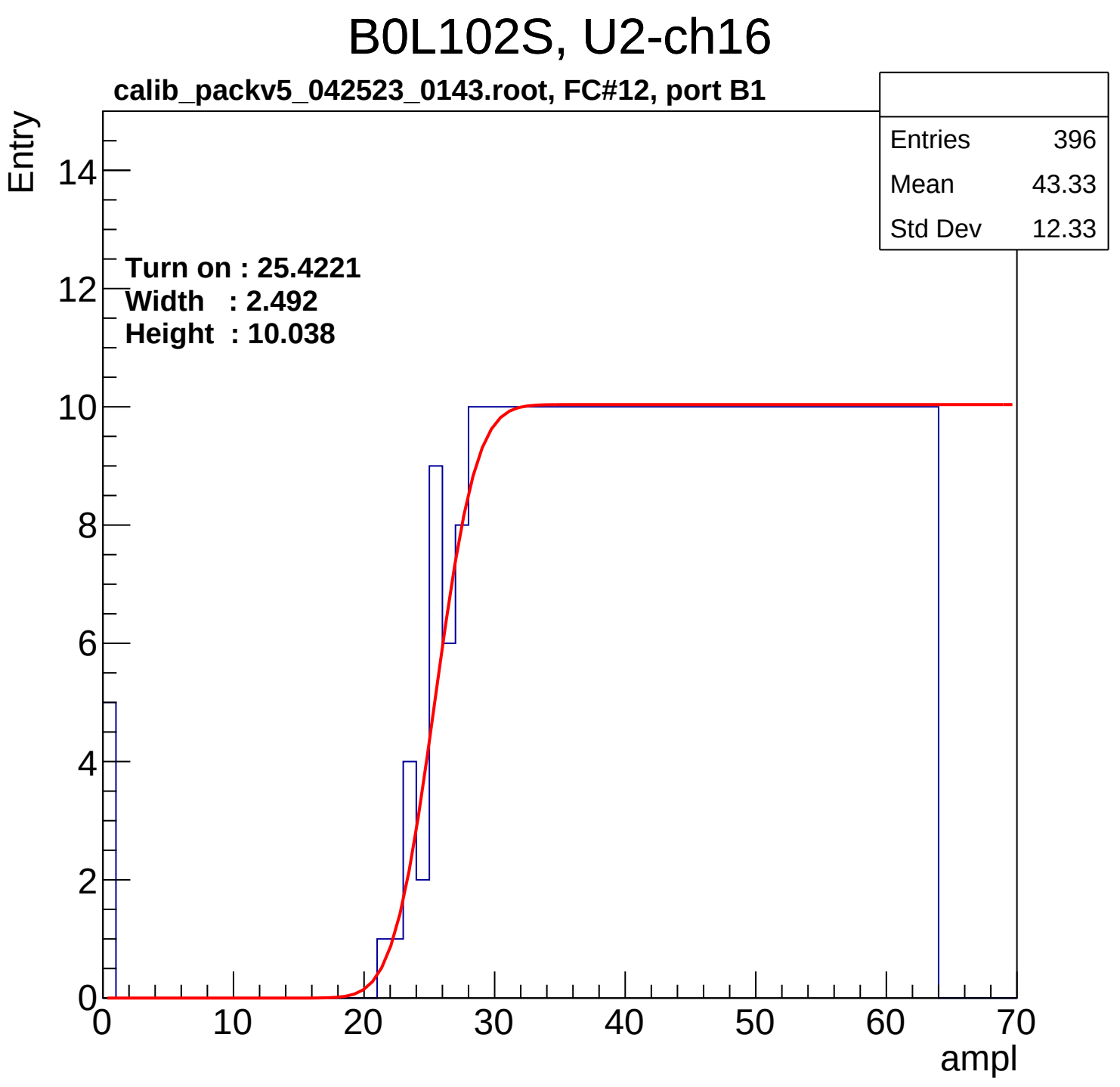
B0L102S, U2-ch16
calib_packv5_042523_0143.root, FC#12, port B1
Entries 396
Mean 43.33
Std Dev 12.33
Turn on : 25.4221
Width : 2.492
Height : 10.038
Entry
ampl
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2
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6
8
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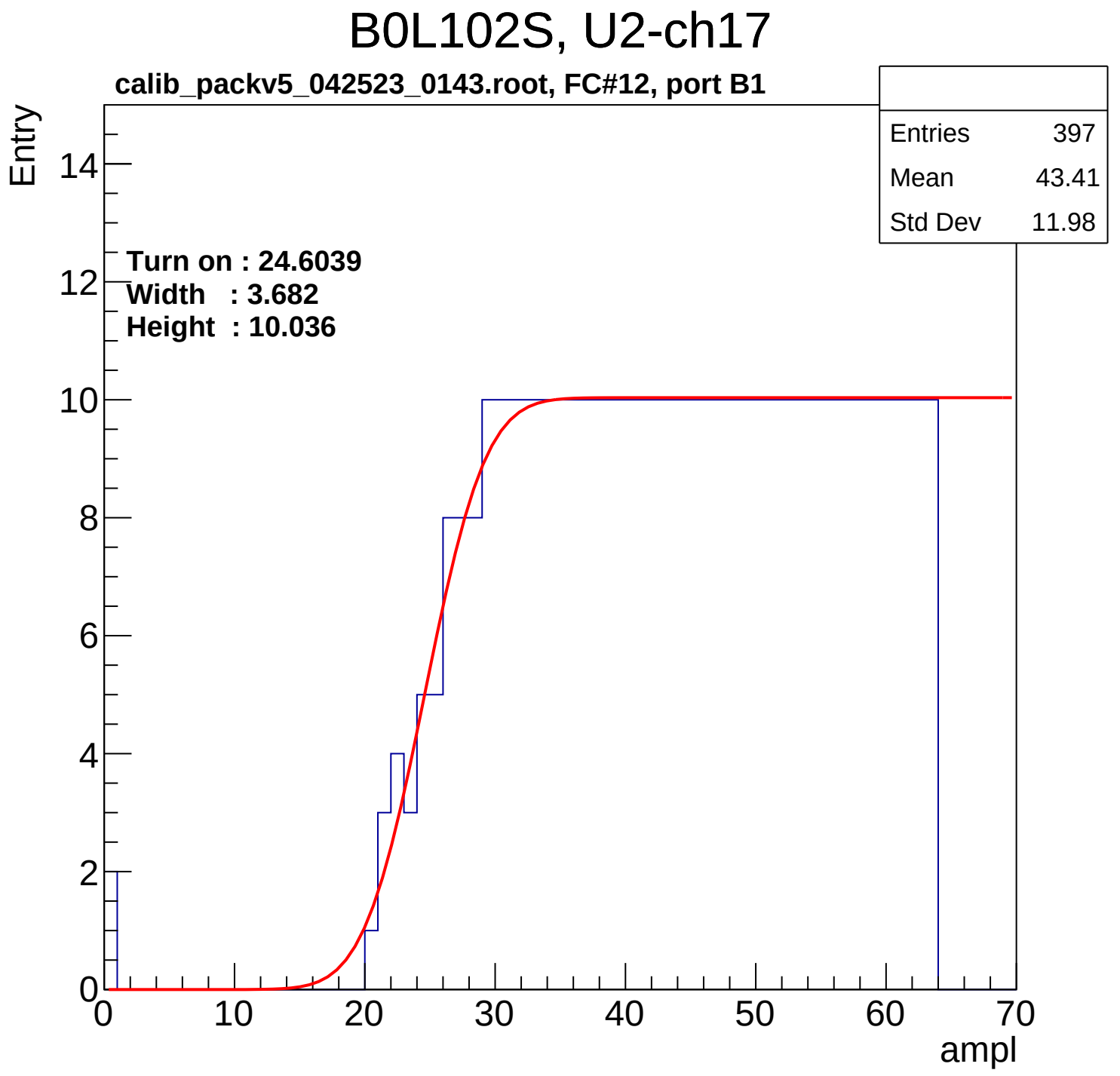
B0L102S, U2-ch17
calib_packv5_042523_0143.root, FC#12, port B1
Entries 397
Mean 43.41
Std Dev 11.98
Turn on : 24.6039
Width : 3.682
Height : 10.036
Entry
ampl
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2
4
6
8
10
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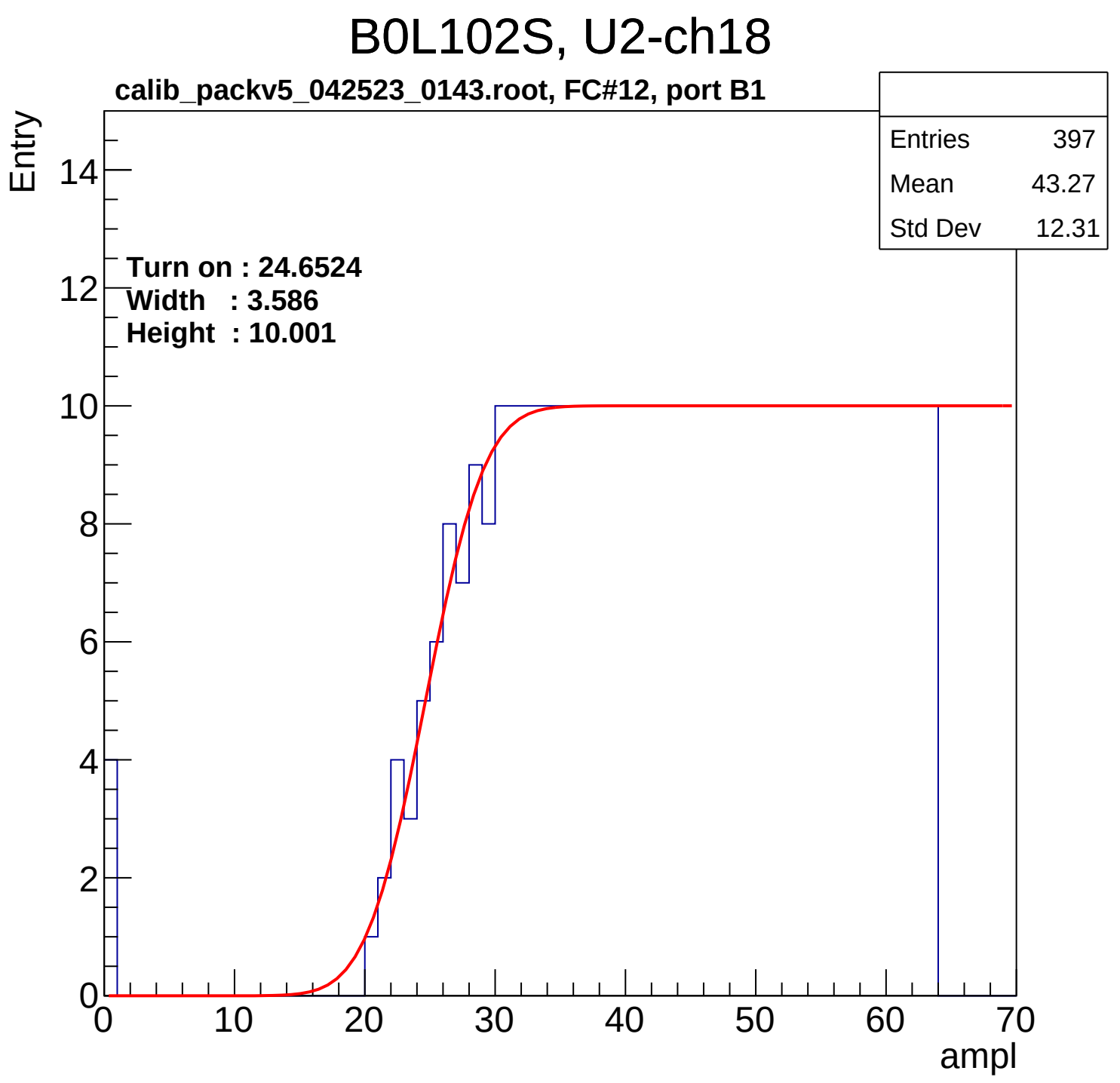
B0L102S, U2-ch18
calib_packv5_042523_0143.root, FC#12, port B1
Entries 397
Mean 43.27
Std Dev 12.31
Turn on : 24.6524
Width : 3.586
Height : 10.001
Entry
ampl
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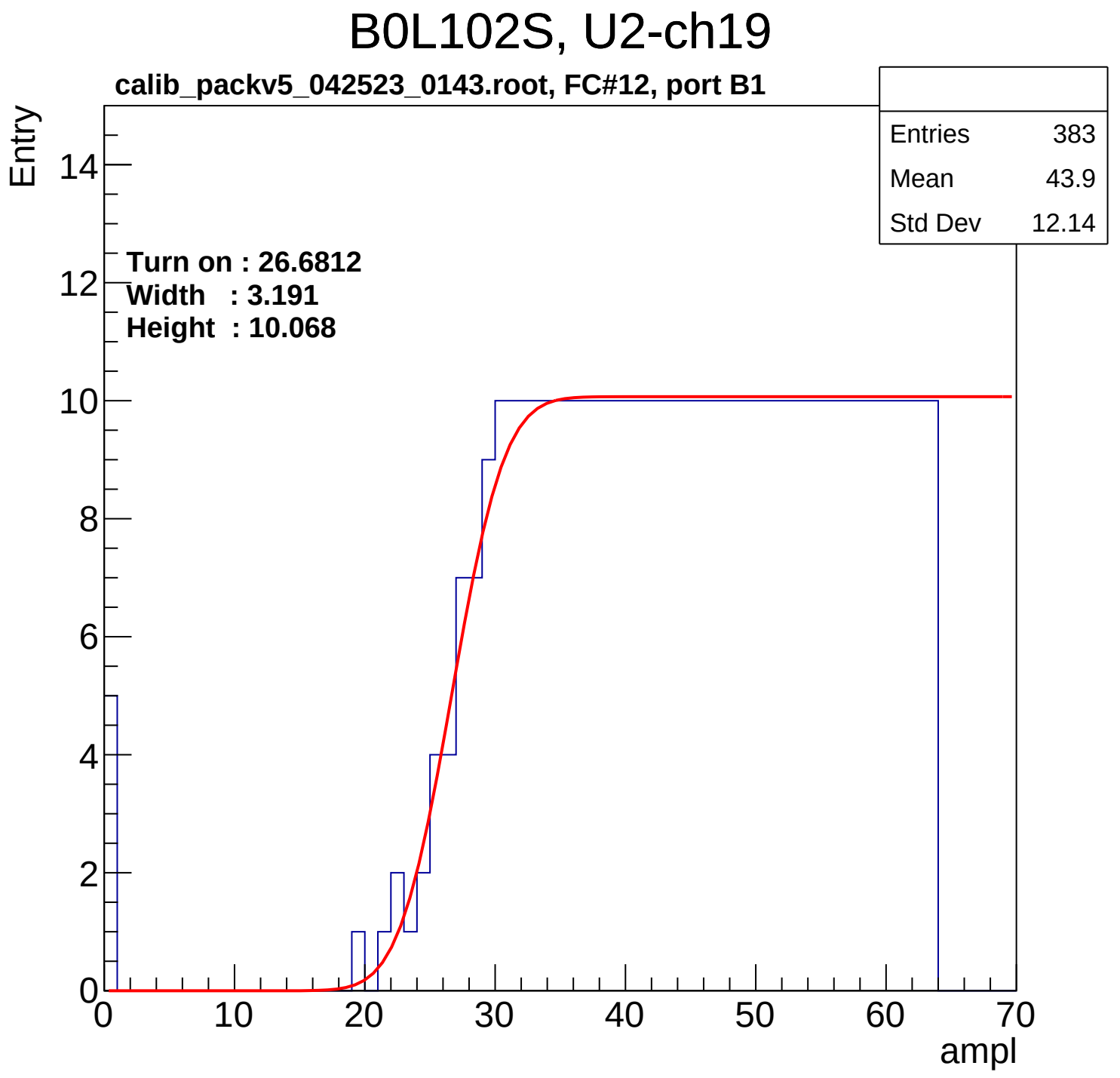
B0L102S, U2-ch19
calib_packv5_042523_0143.root, FC#12, port B1
Entries 383
Mean 43.9
Std Dev 12.14
Turn on : 26.6812
Width : 3.191
Height : 10.068
Entry
ampl
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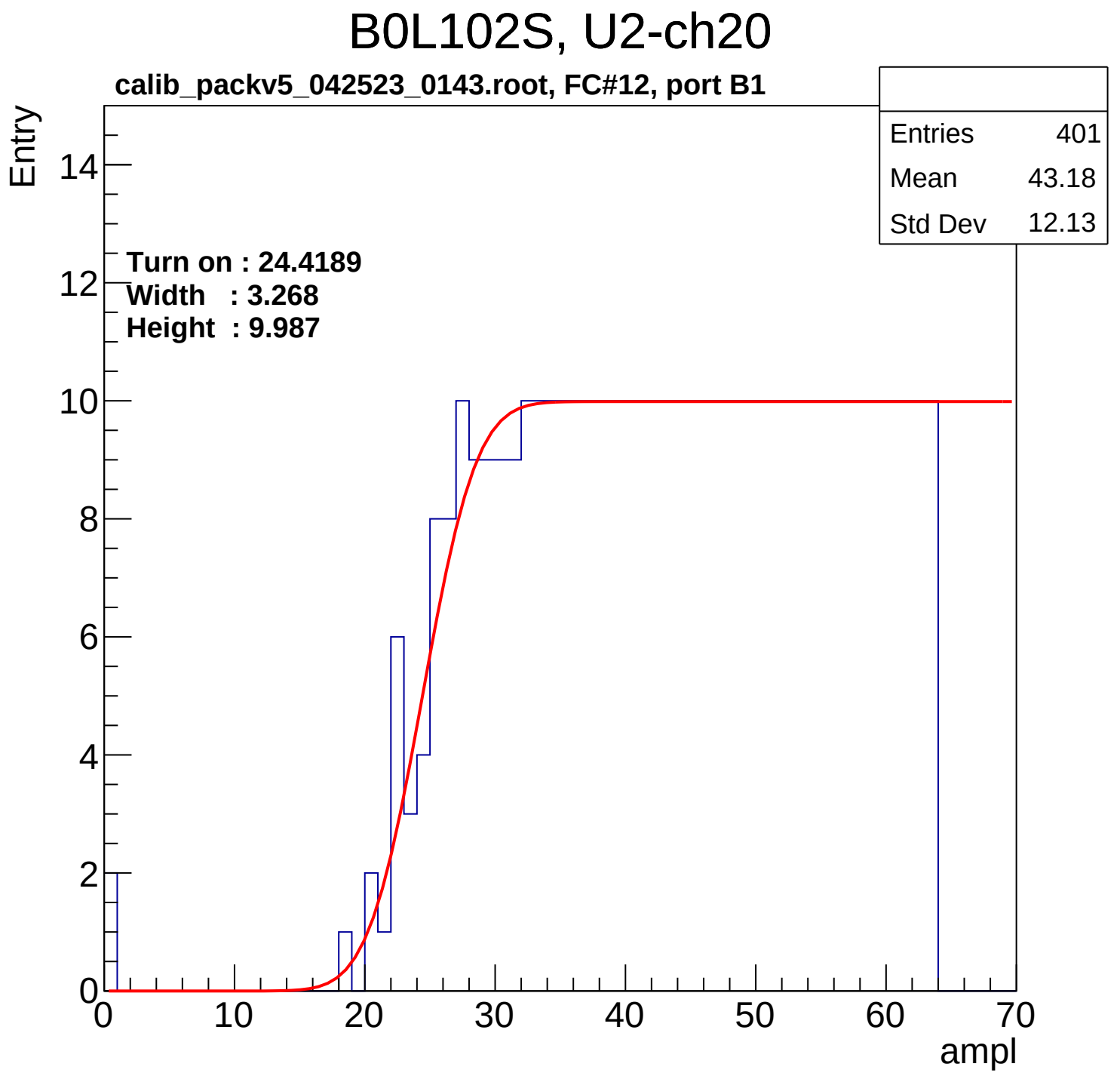
B0L102S, U2-ch20
calib_packv5_042523_0143.root, FC#12, port B1
Entries 401
Mean 43.18
Std Dev 12.13
Turn on : 24.4189
Width : 3.268
Height : 9.987
Entry
ampl
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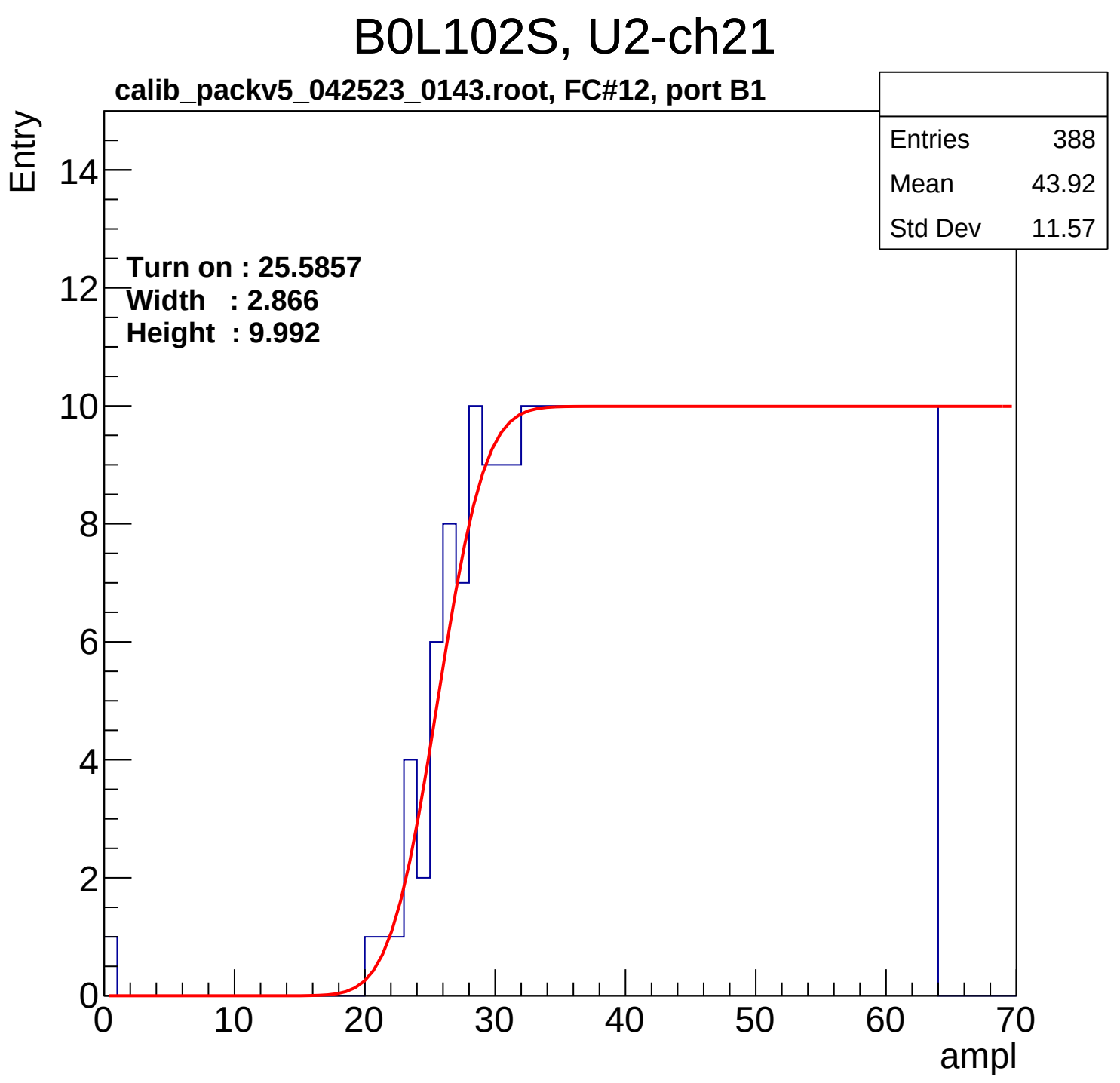
B0L102S, U2-ch21
calib_packv5_042523_0143.root, FC#12, port B1
Entries 388
Mean 43.92
Std Dev 11.57
Turn on : 25.5857
Width : 2.866
Height : 9.992
Entry
ampl
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10
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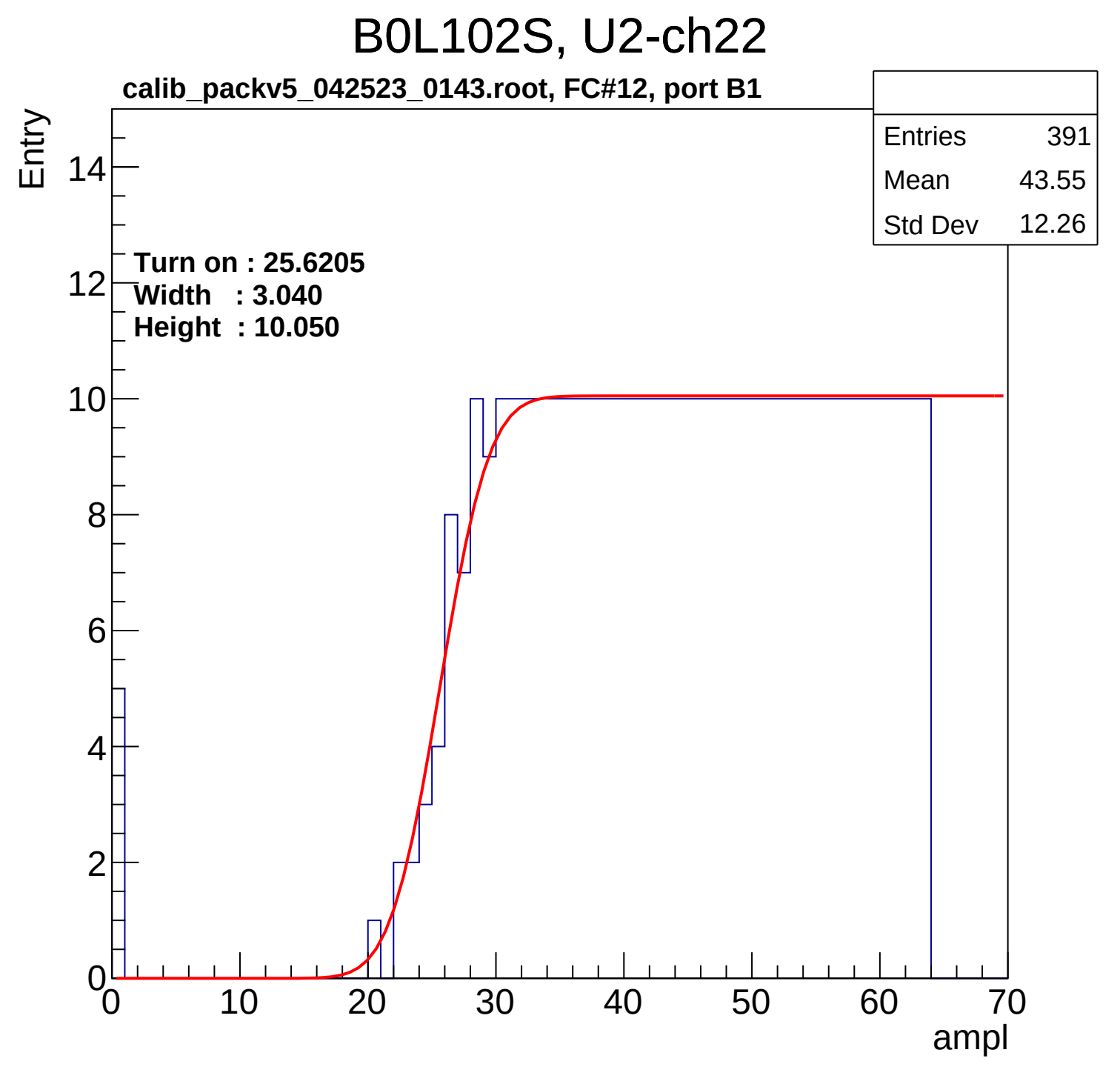
B0L102S, U2-ch22
calib_packv5_042523_0143.root, FC#12, port B1
Entries 391
Mean 43.55
Std Dev 12.26
Turn on : 25.6205
Width : 3.040
Height : 10.050
Entry
ampl
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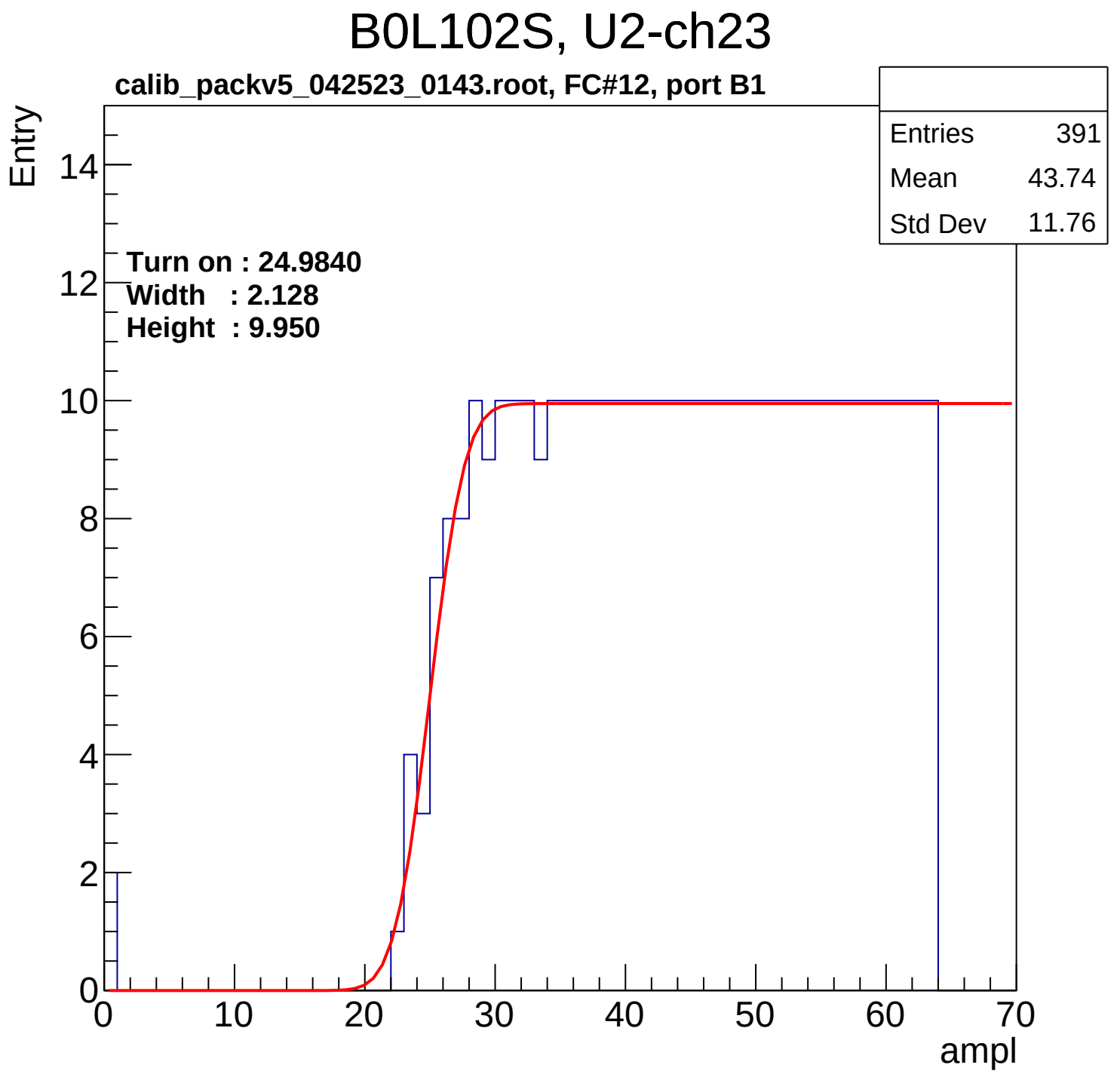
B0L102S, U2-ch23
calib_packv5_042523_0143.root, FC#12, port B1
Entries 391
Mean 43.74
Std Dev 11.76
Turn on : 24.9840
Width : 2.128
Height : 9.950
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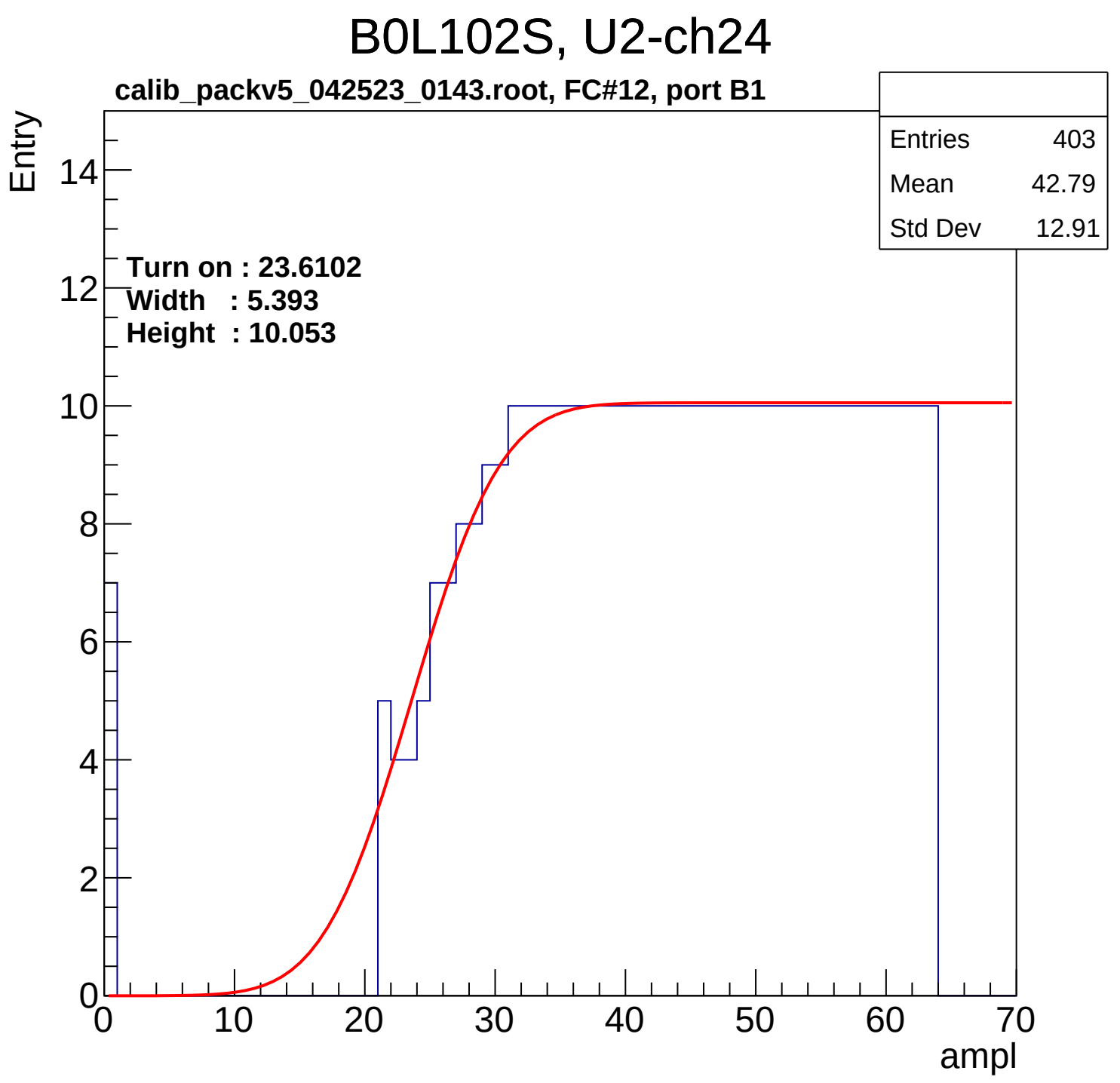
B0L102S, U2-ch24
calib_packv5_042523_0143.root, FC#12, port B1
Entries 403
Mean 42.79
Std Dev 12.91
Turn on : 23.6102
Width : 5.393
Height : 10.053
Entry
ampl
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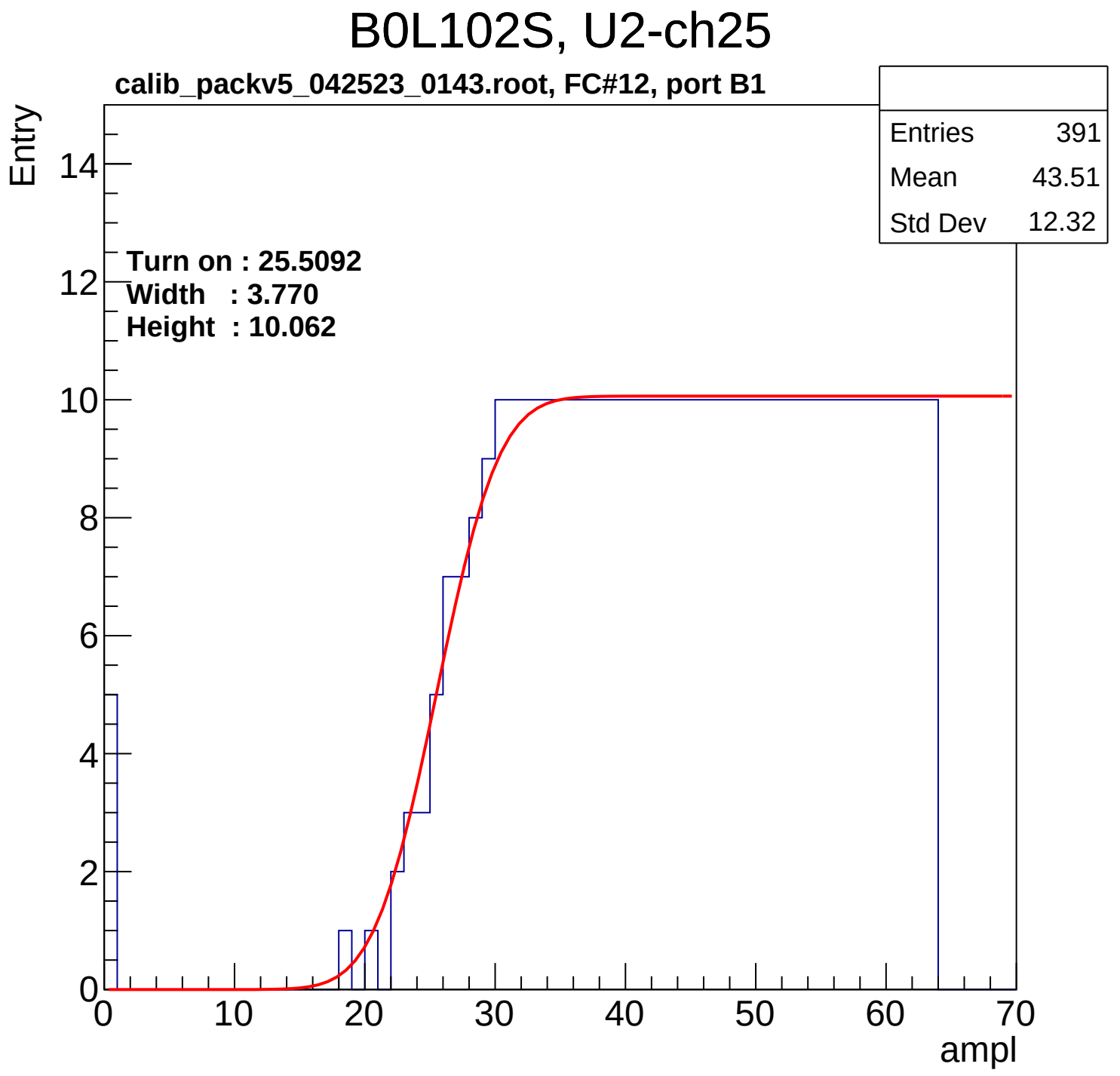
B0L102S, U2-ch25
calib_packv5_042523_0143.root, FC#12, port B1
Entries 391
Mean 43.51
Std Dev 12.32
Turn on : 25.5092
Width : 3.770
Height : 10.062
Entry
ampl
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8
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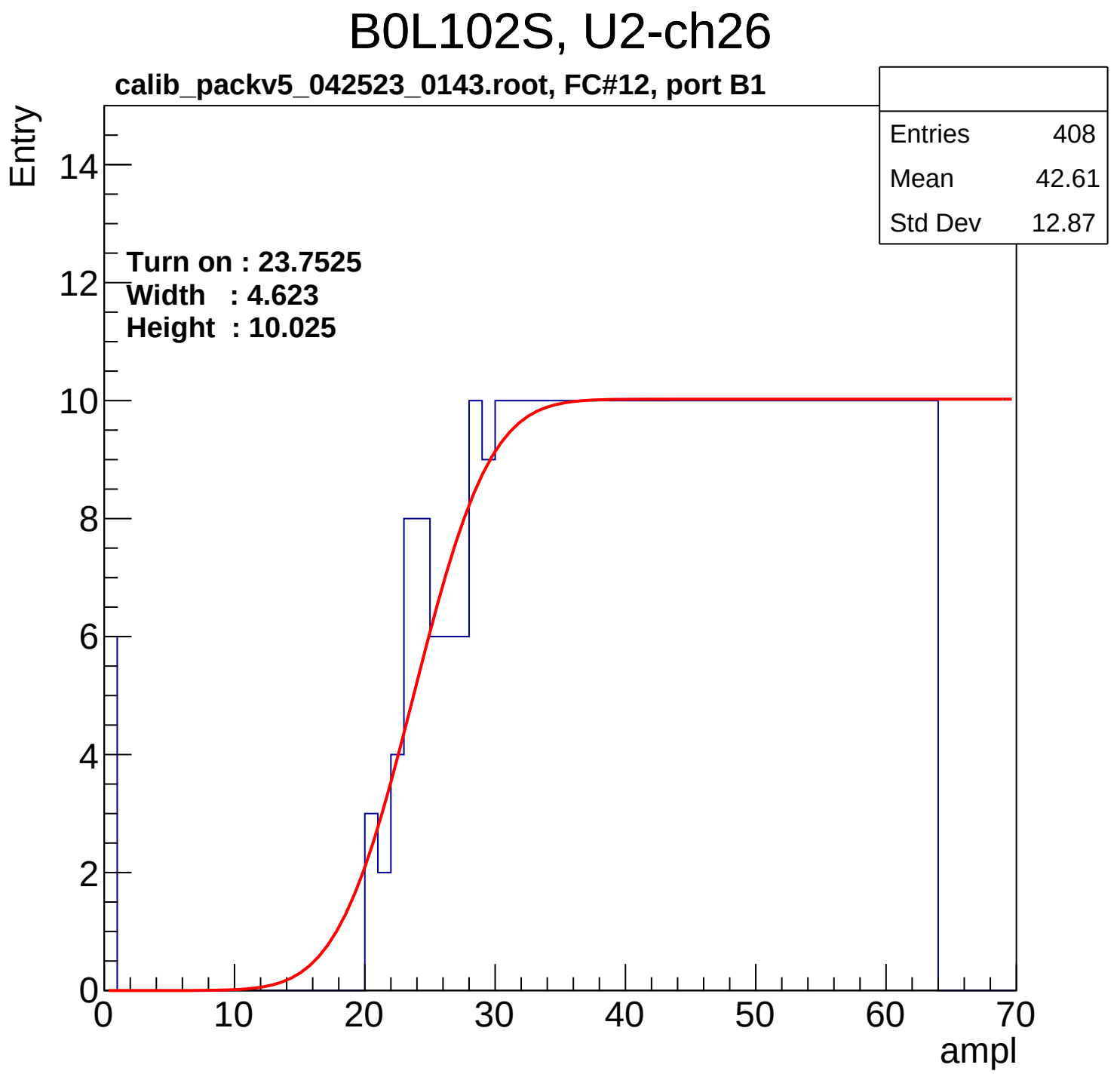
B0L102S, U2-ch26
calib_packv5_042523_0143.root, FC#12, port B1
Entries 408
Mean 42.61
Std Dev 12.87
Turn on : 23.7525
Width : 4.623
Height : 10.025
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ampl
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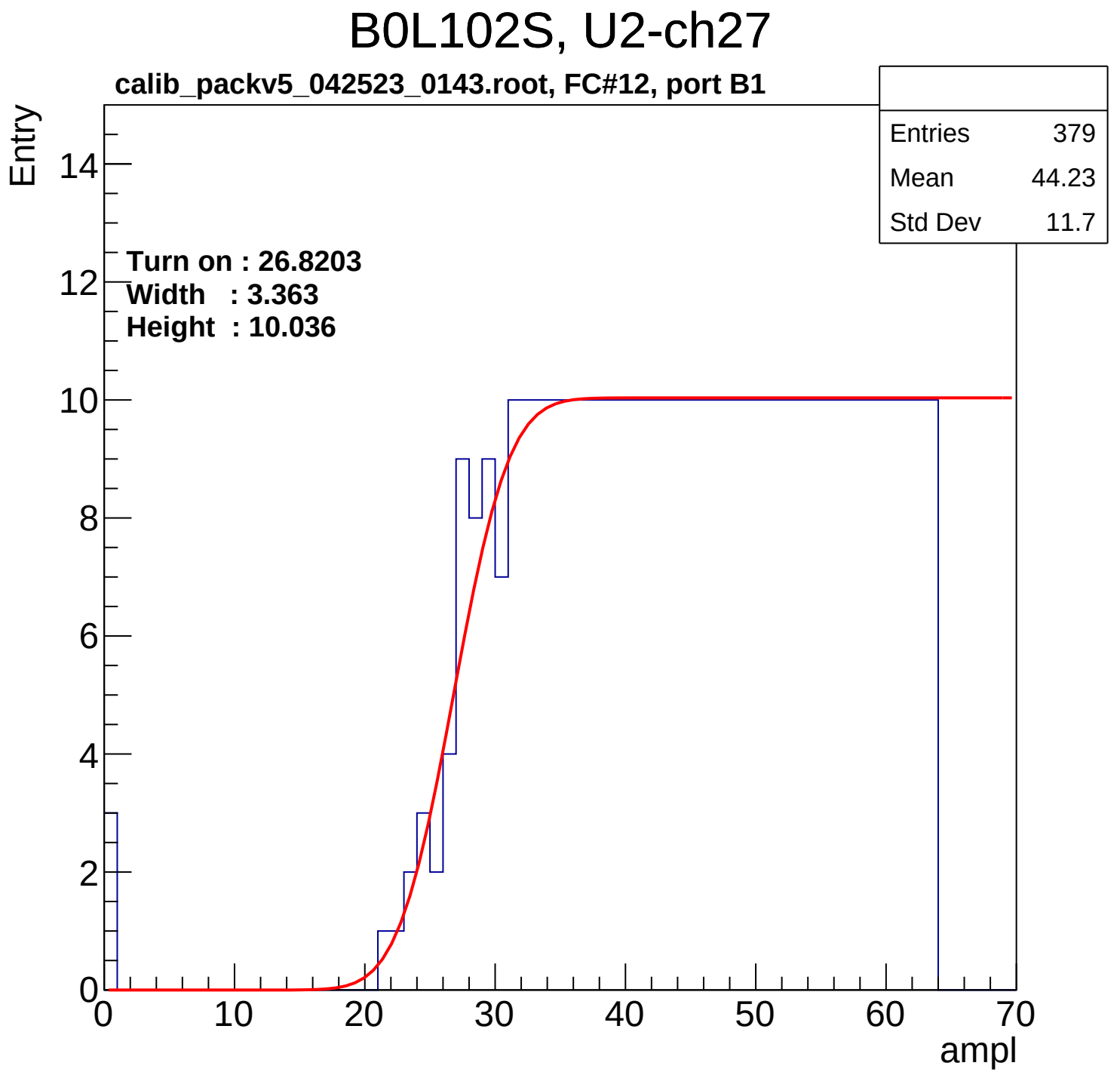
B0L102S, U2-ch27
calib_packv5_042523_0143.root, FC#12, port B1
Entries 379
Mean 44.23
Std Dev 11.7
Turn on : 26.8203
Width : 3.363
Height : 10.036
Entry
ampl
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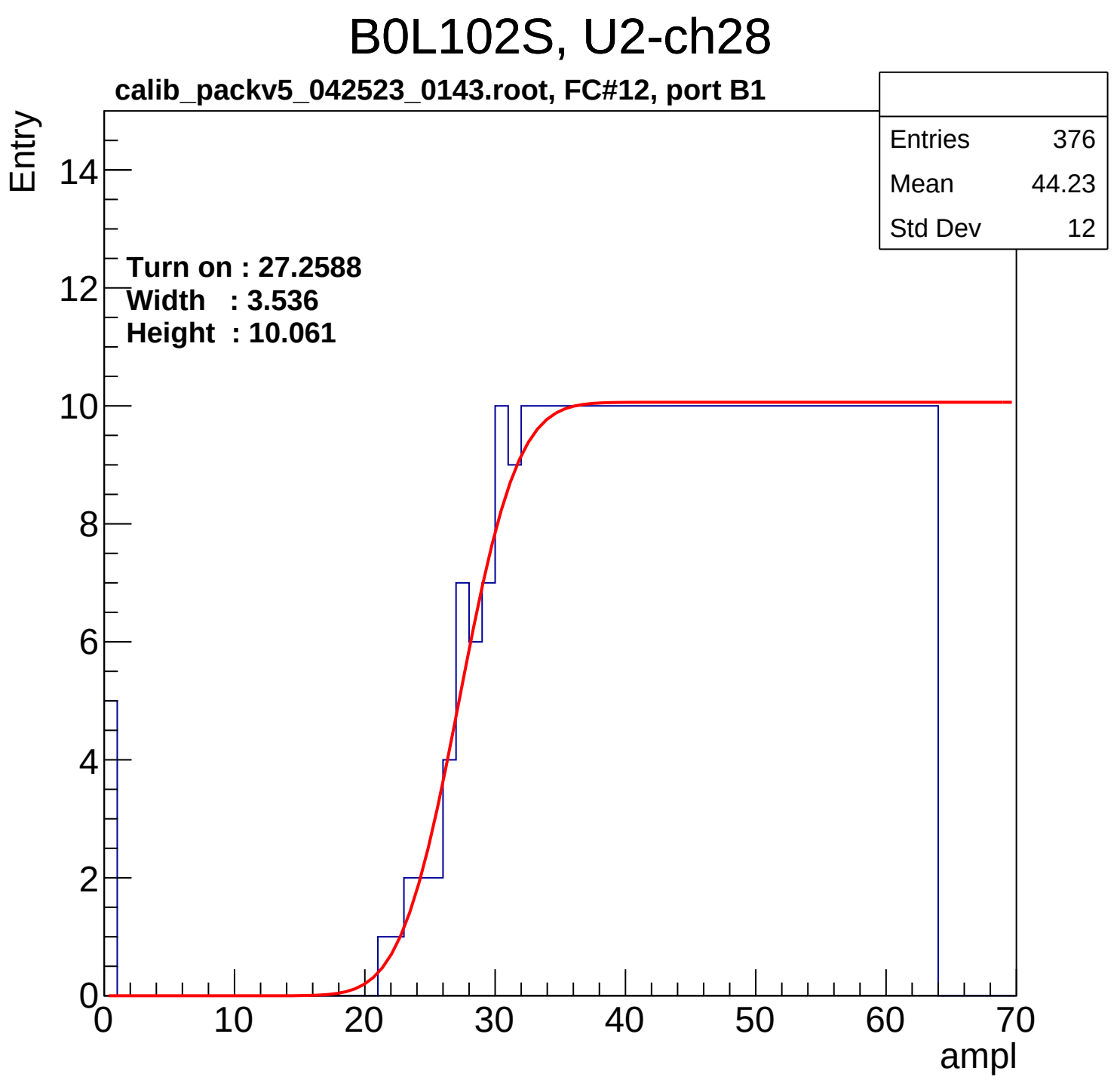
B0L102S, U2-ch28
calib_packv5_042523_0143.root, FC#12, port B1
Entries 376
Mean 44.23
Std Dev 12
Turn on : 27.2588
Width : 3.536
Height : 10.061
Entry
ampl
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4
6
8
10
12
14
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10
20
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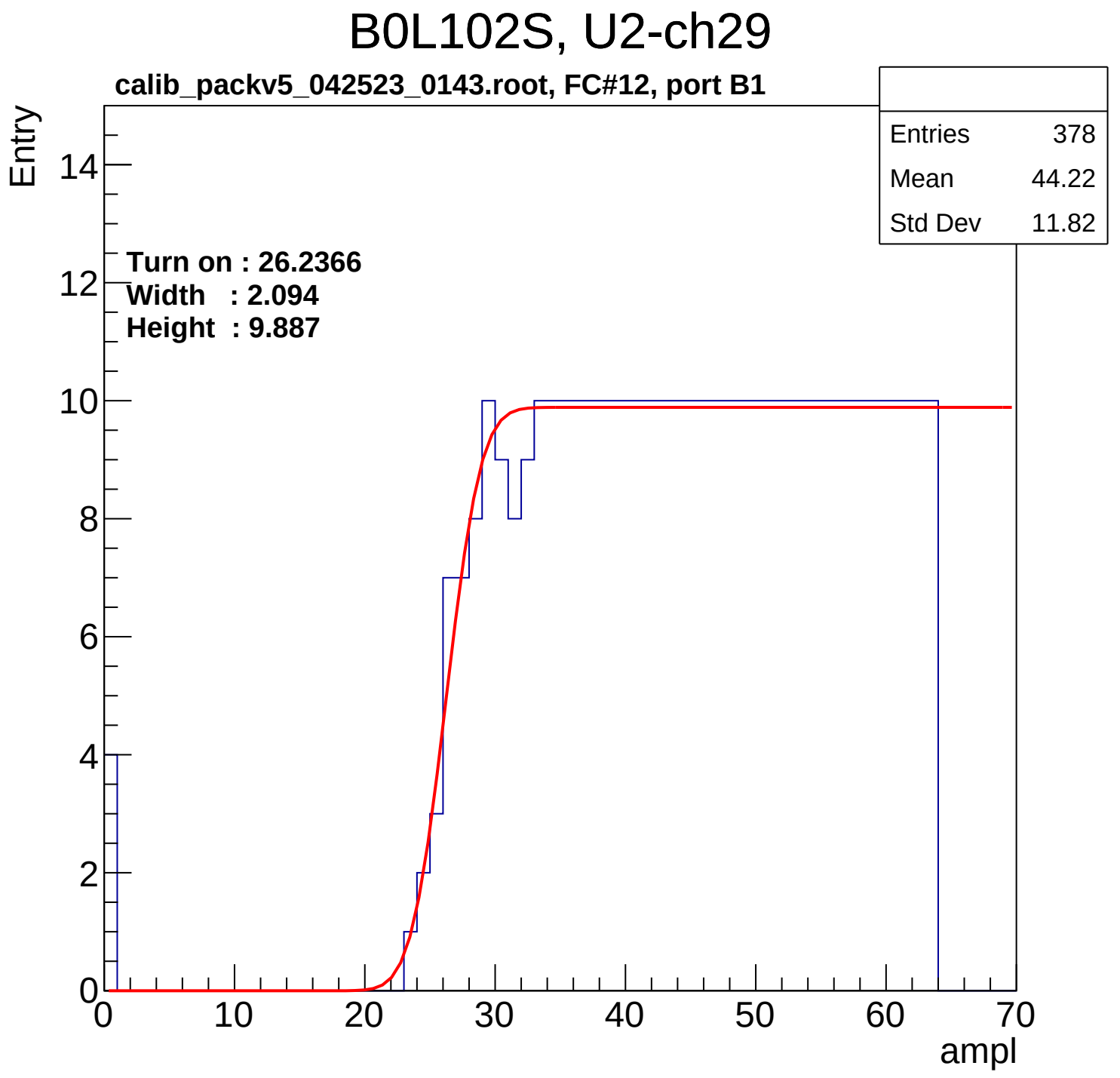
B0L102S, U2-ch29
calib_packv5_042523_0143.root, FC#12, port B1
Entries 378
Mean 44.22
Std Dev 11.82
Turn on : 26.2366
Width : 2.094
Height : 9.887
Entry
ampl
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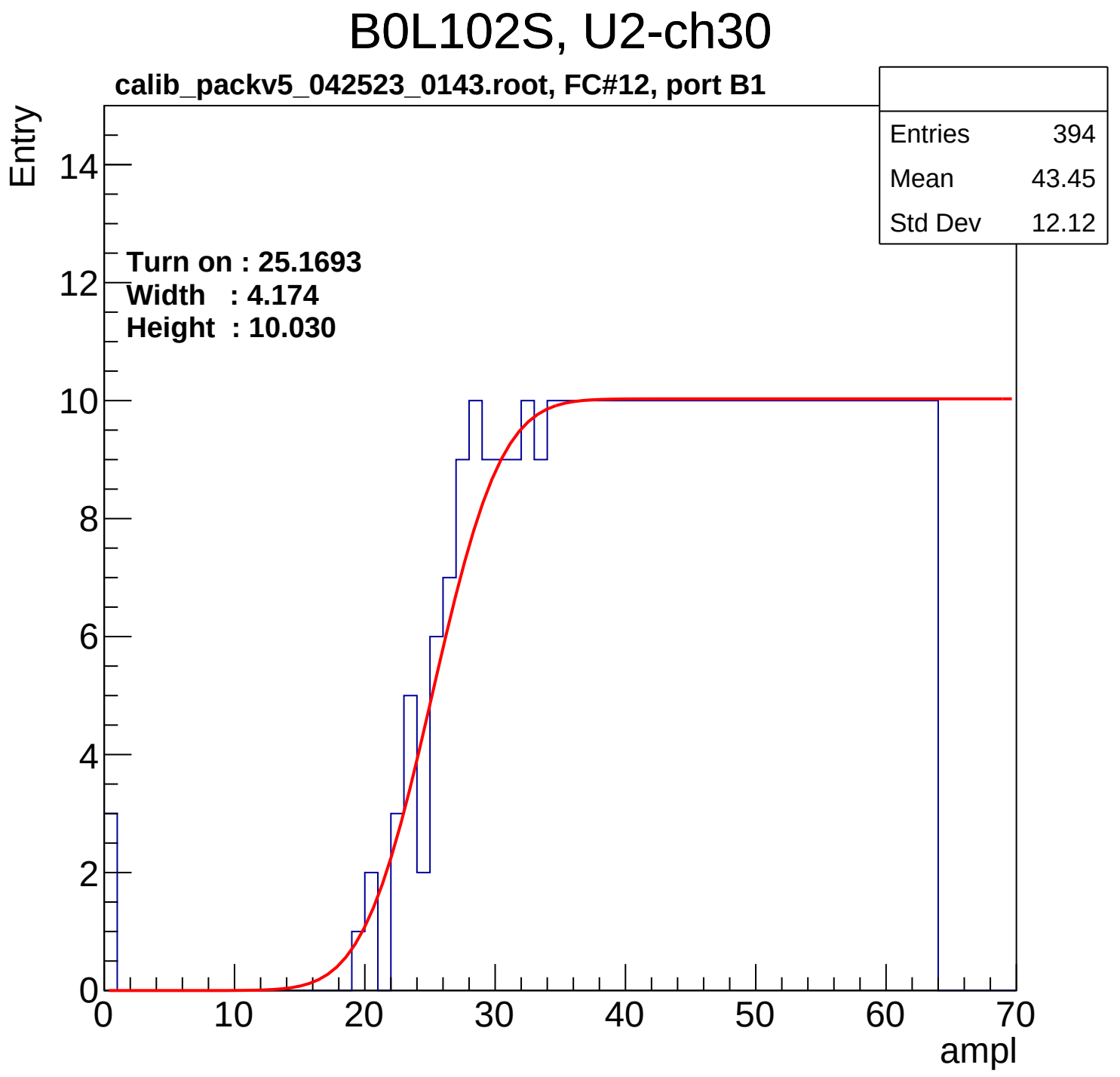
B0L102S, U2-ch30
calib_packv5_042523_0143.root, FC#12, port B1
Entries 394
Mean 43.45
Std Dev 12.12
Turn on : 25.1693
Width : 4.174
Height : 10.030
Entry
ampl
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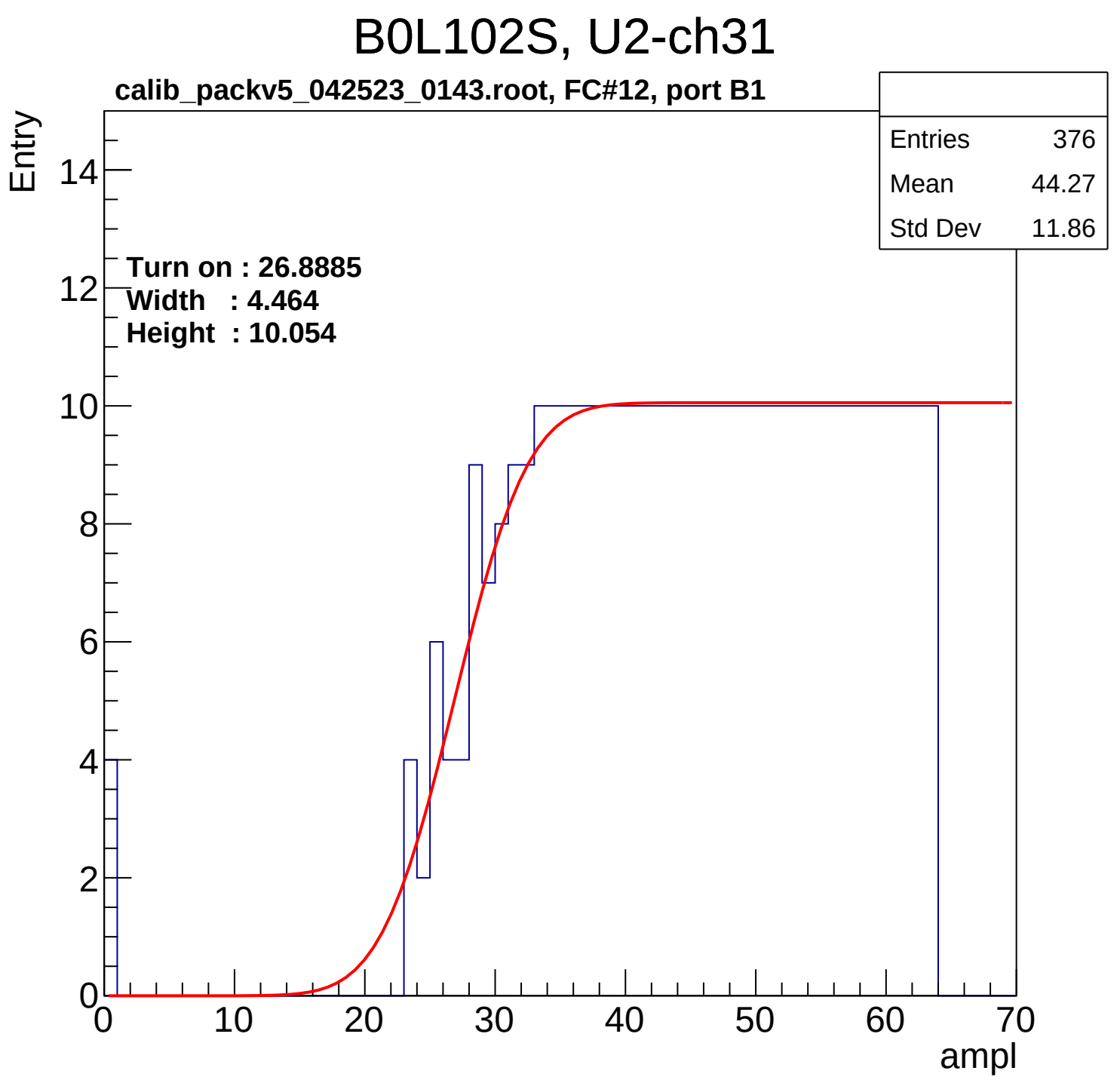
B0L102S, U2-ch31
calib_packv5_042523_0143.root, FC#12, port B1
Entries 376
Mean 44.27
Std Dev 11.86
Turn on : 26.8885
Width : 4.464
Height : 10.054
Entry
ampl
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2
4
6
8
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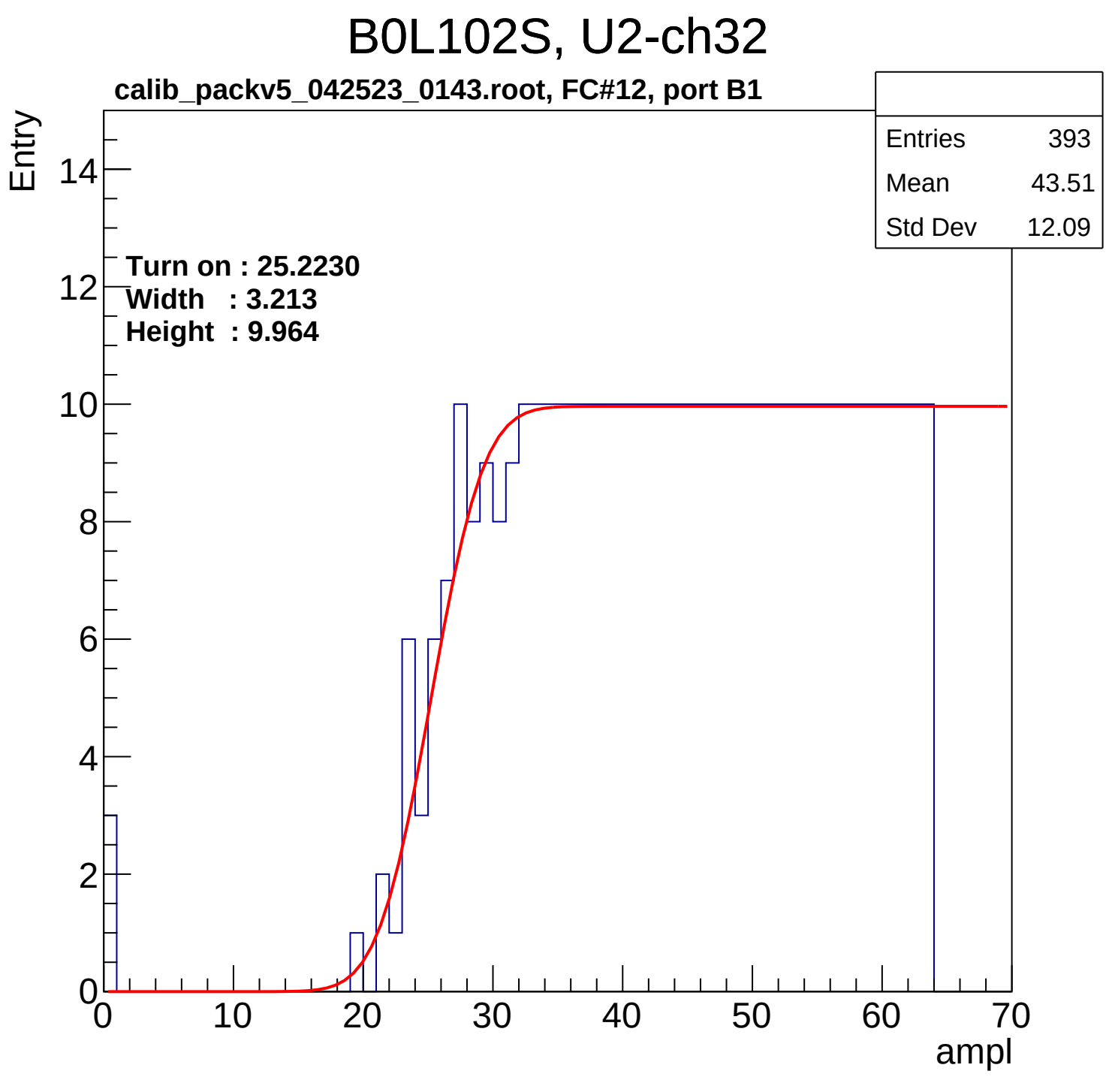
B0L102S, U2-ch32
calib_packv5_042523_0143.root, FC#12, port B1
Entries 393
Mean 43.51
Std Dev 12.09
Turn on : 25.2230
Width : 3.213
Height : 9.964
Entry
ampl
0
2
4
6
8
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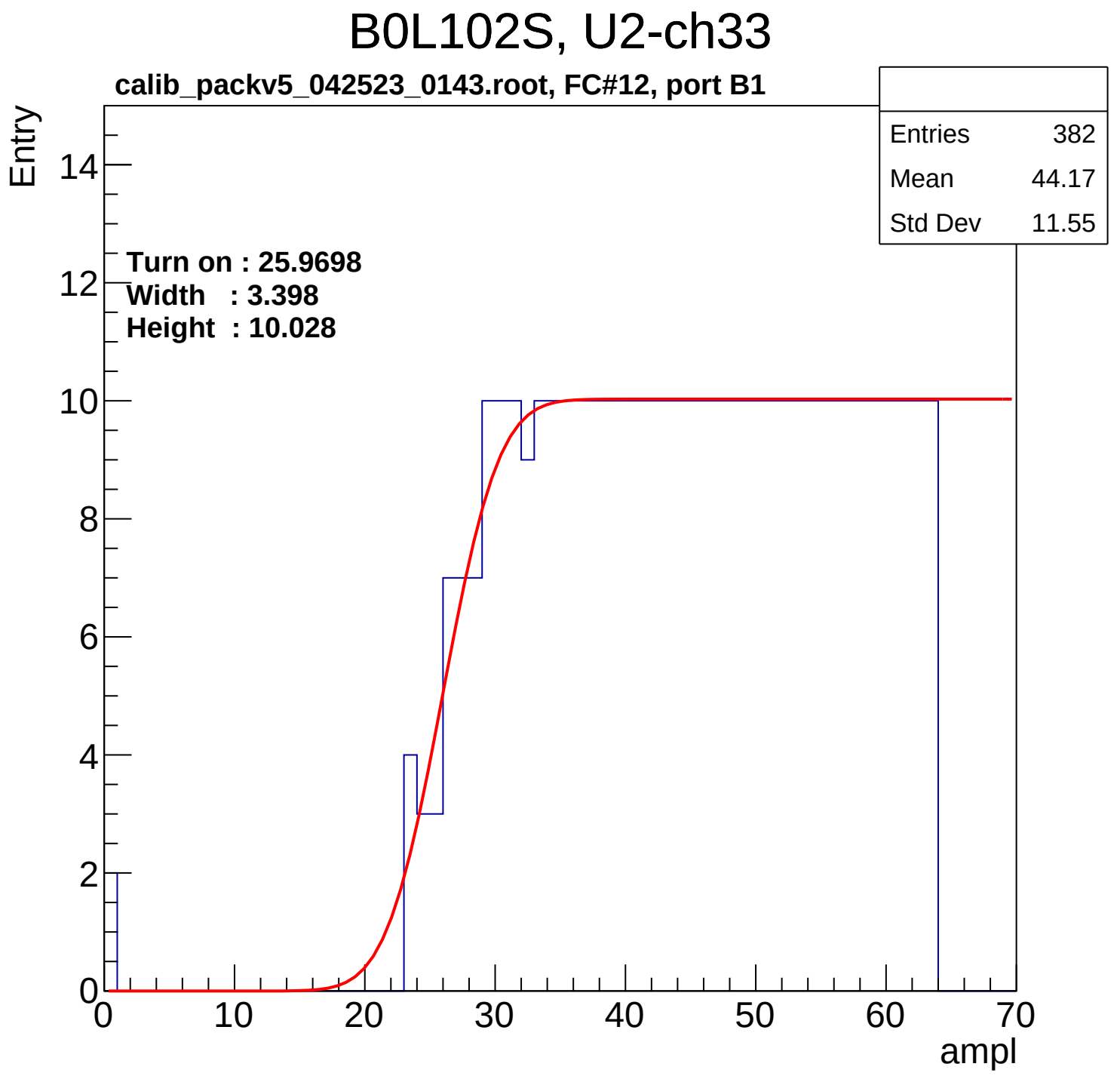
B0L102S, U2-ch33
calib_packv5_042523_0143.root, FC#12, port B1
Entries 382
Mean 44.17
Std Dev 11.55
Turn on : 25.9698
Width : 3.398
Height : 10.028
Entry
ampl
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8
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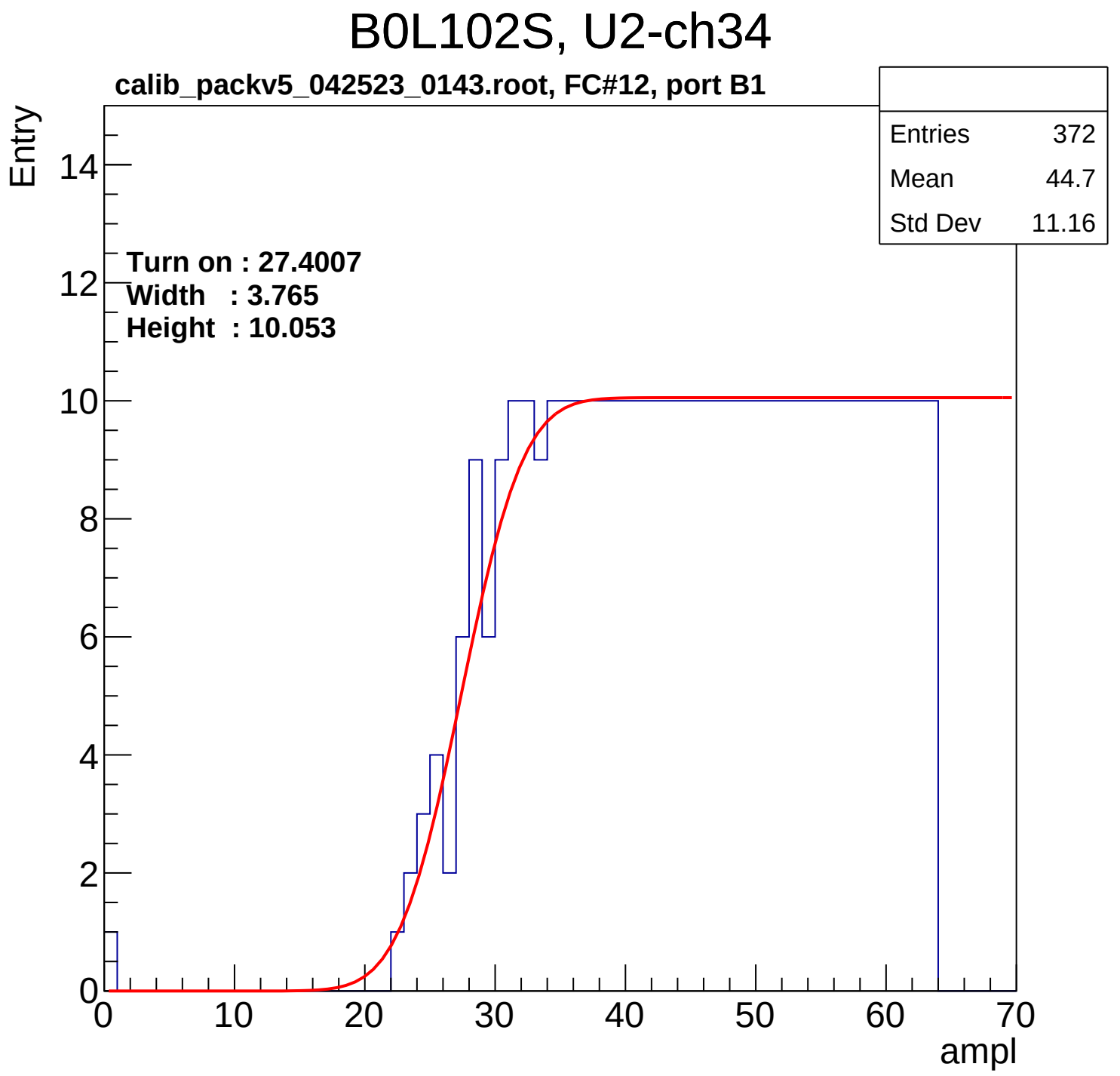
B0L102S, U2-ch34
calib_packv5_042523_0143.root, FC#12, port B1
Entries 372
Mean 44.7
Std Dev 11.16
Turn on : 27.4007
Width : 3.765
Height : 10.053
Entry
ampl
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2
4
6
8
10
12
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0
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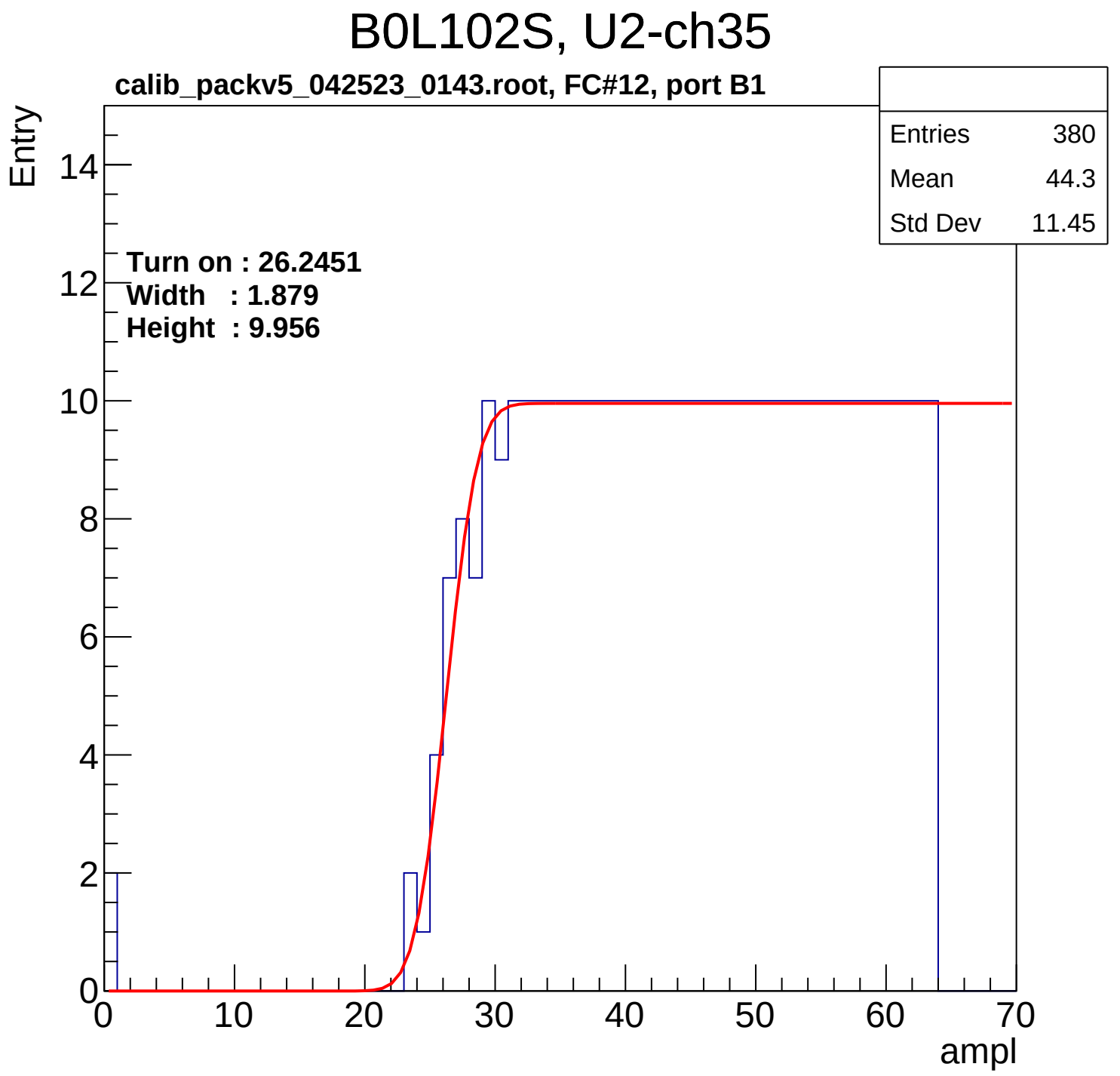
B0L102S, U2-ch35
calib_packv5_042523_0143.root, FC#12, port B1
Entries 380
Mean 44.3
Std Dev 11.45
Turn on : 26.2451
Width : 1.879
Height : 9.956
Entry
ampl
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6
8
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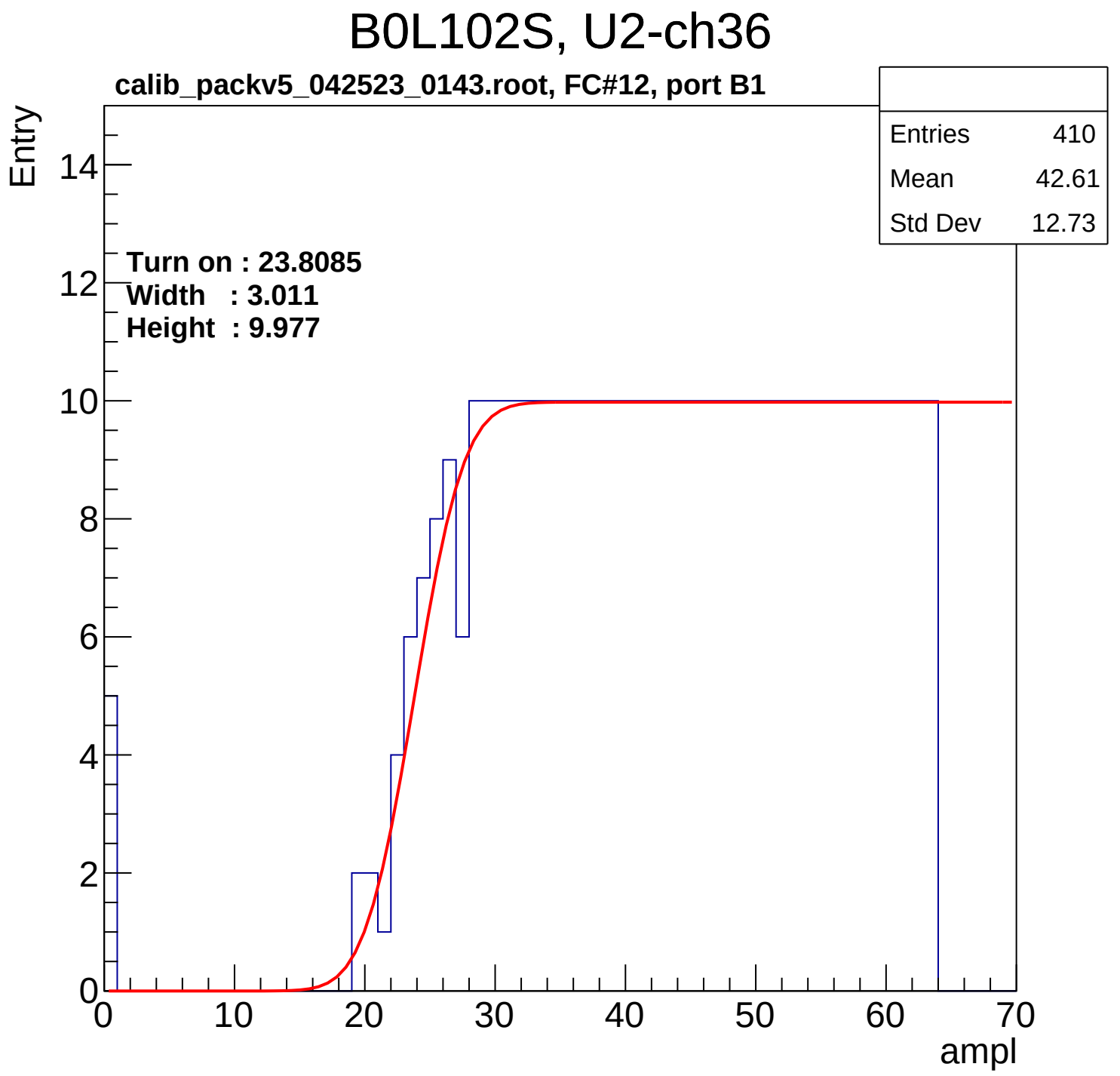
B0L102S, U2-ch36
calib_packv5_042523_0143.root, FC#12, port B1
Entries 410
Mean 42.61
Std Dev 12.73
Turn on : 23.8085
Width : 3.011
Height : 9.977
Entry
ampl
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2
4
6
8
10
12
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40
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60
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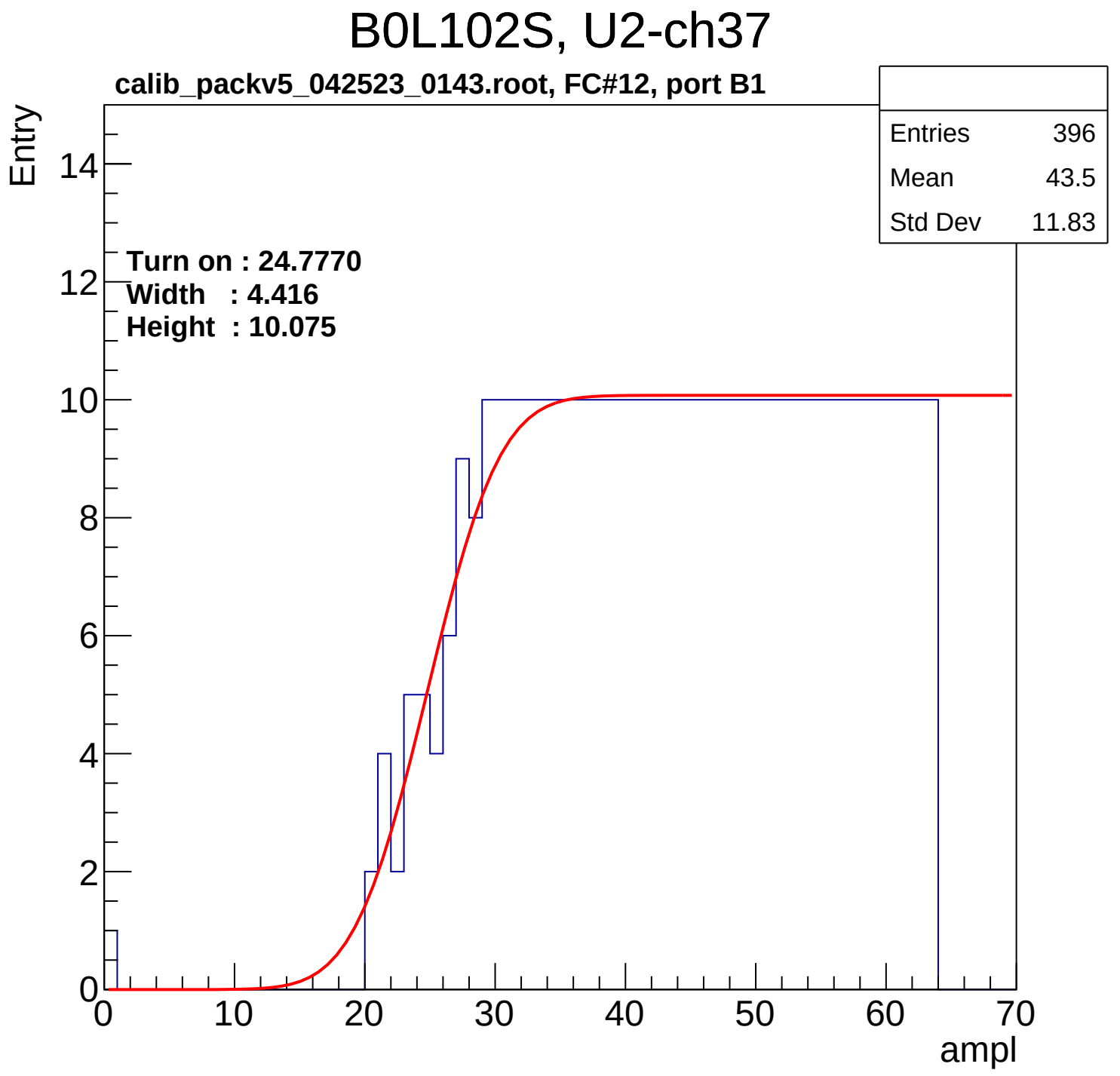
B0L102S, U2-ch37
calib_packv5_042523_0143.root, FC#12, port B1
Entries 396
Mean 43.5
Std Dev 11.83
Turn on : 24.7770
Width : 4.416
Height : 10.075
Entry
ampl
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2
4
6
8
10
12
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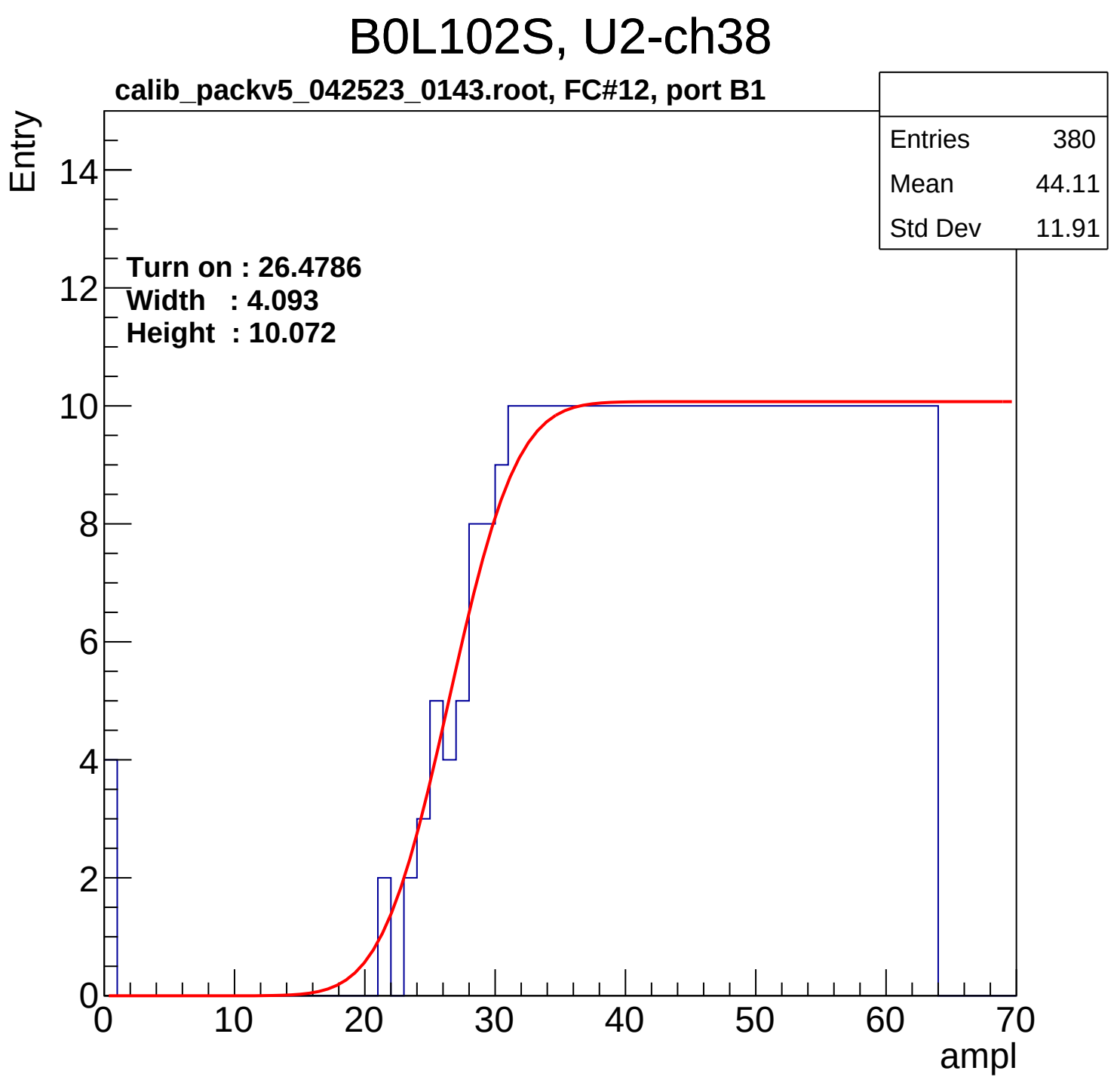
B0L102S, U2-ch38
calib_packv5_042523_0143.root, FC#12, port B1
Entries 380
Mean 44.11
Std Dev 11.91
Turn on : 26.4786
Width : 4.093
Height : 10.072
Entry
ampl
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4
6
8
10
12
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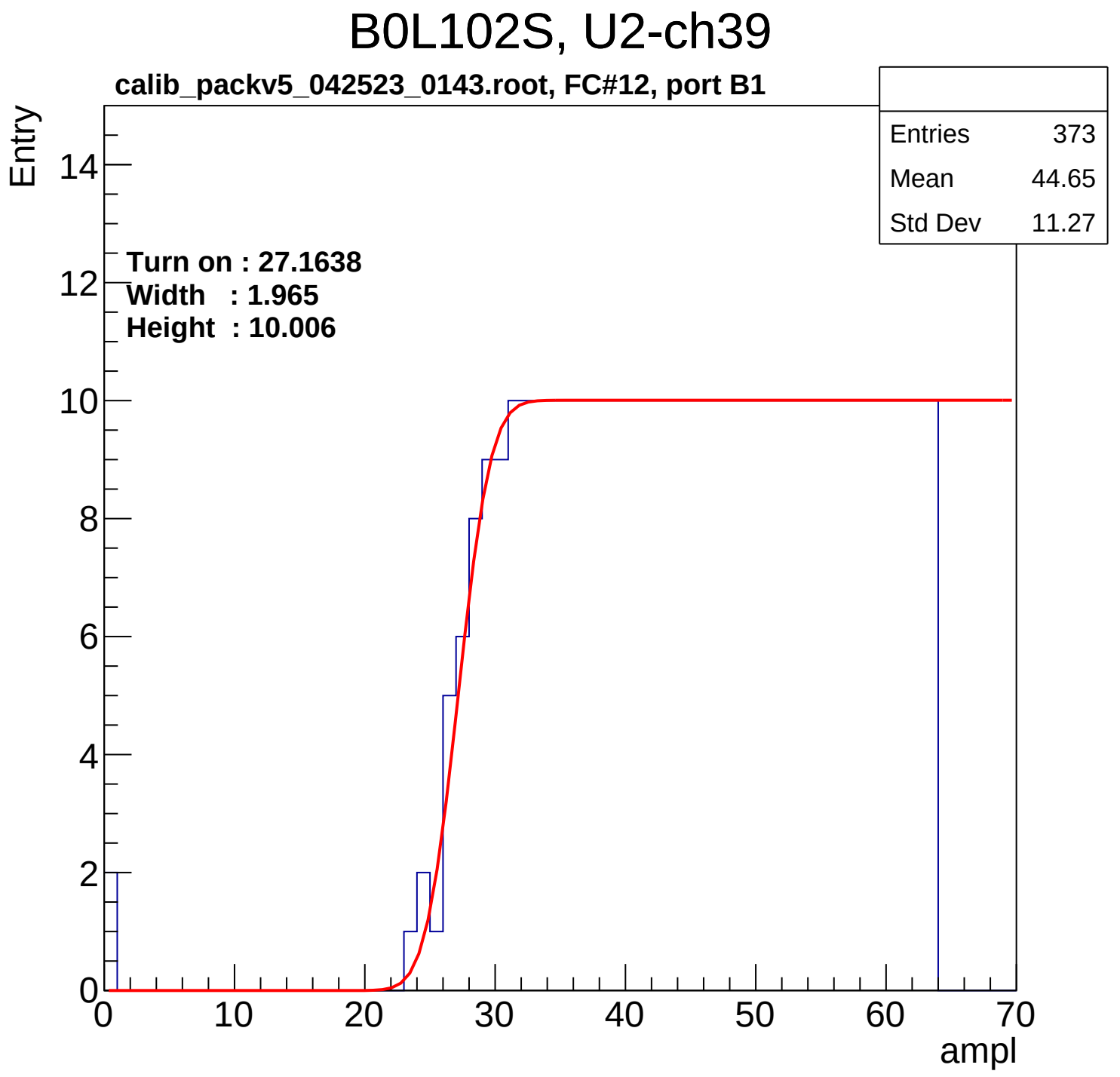
B0L102S, U2-ch39
calib_packv5_042523_0143.root, FC#12, port B1
Entries 373
Mean 44.65
Std Dev 11.27
Turn on : 27.1638
Width : 1.965
Height : 10.006
Entry
ampl
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8
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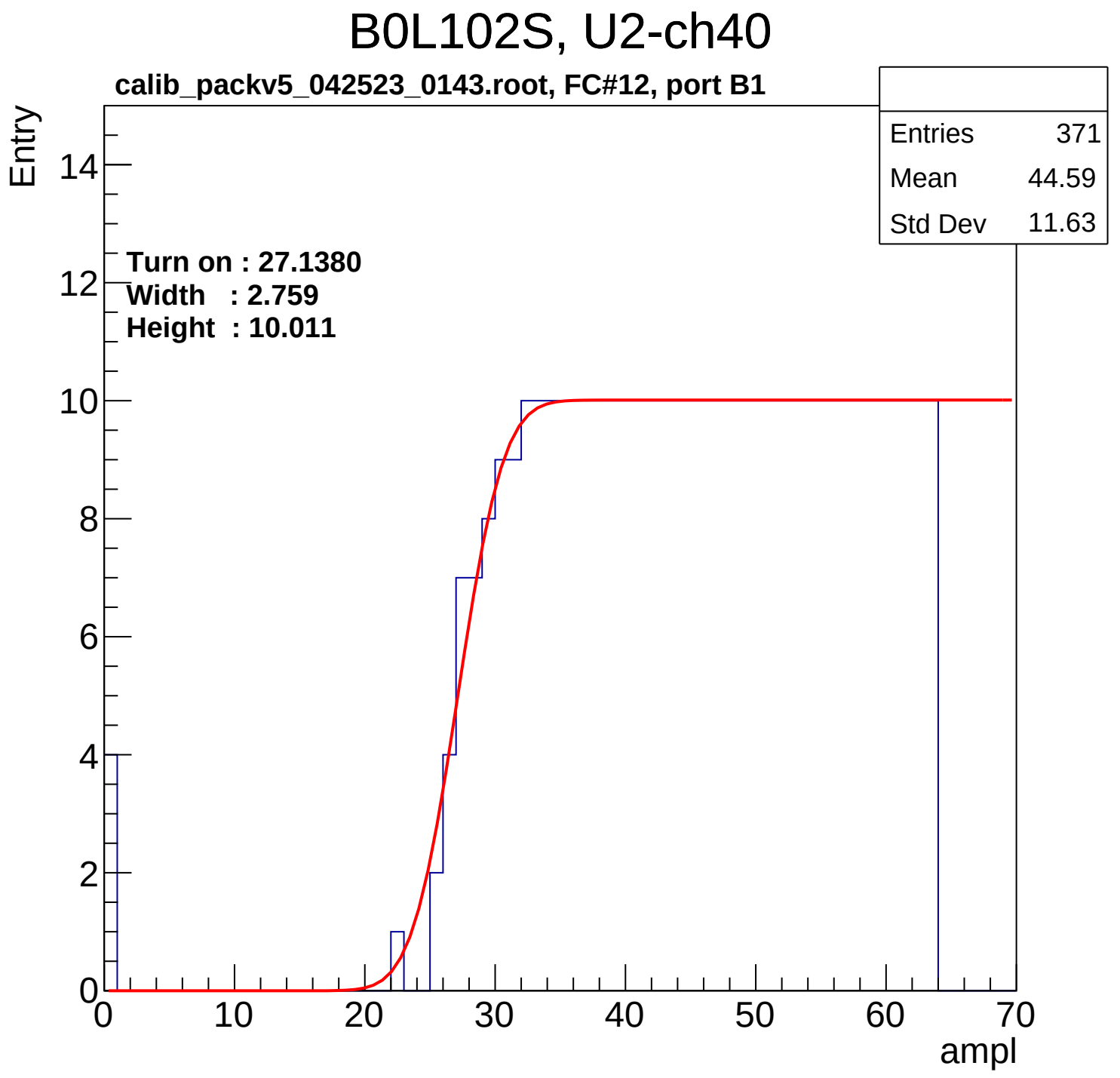
B0L102S, U2-ch40
calib_packv5_042523_0143.root, FC#12, port B1
Entries 371
Mean 44.59
Std Dev 11.63
Turn on : 27.1380
Width : 2.759
Height : 10.011
Entry
ampl
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8
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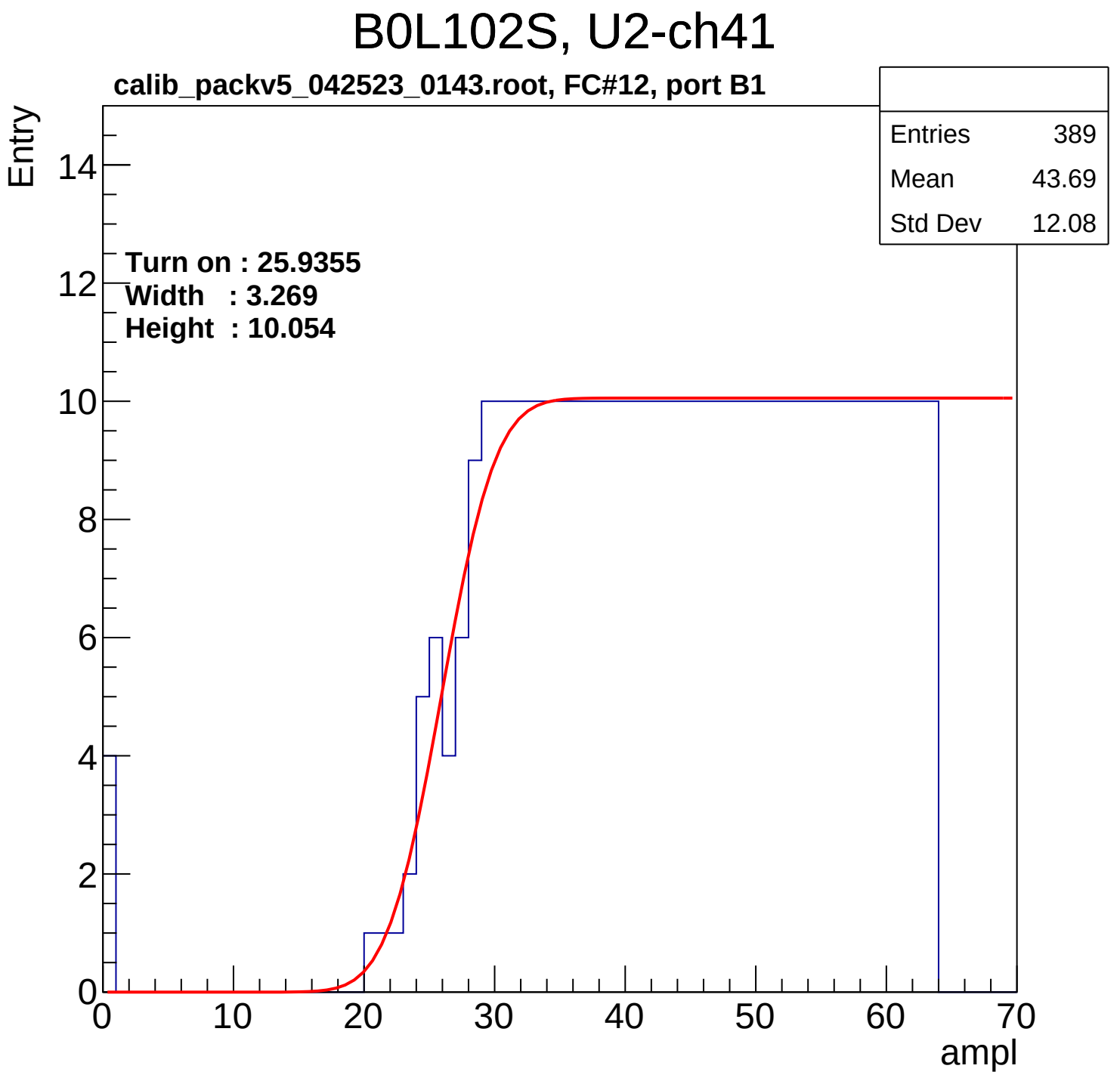
B0L102S, U2-ch41
calib_packv5_042523_0143.root, FC#12, port B1
Entries 389
Mean 43.69
Std Dev 12.08
Turn on : 25.9355
Width : 3.269
Height : 10.054
Entry
ampl
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8
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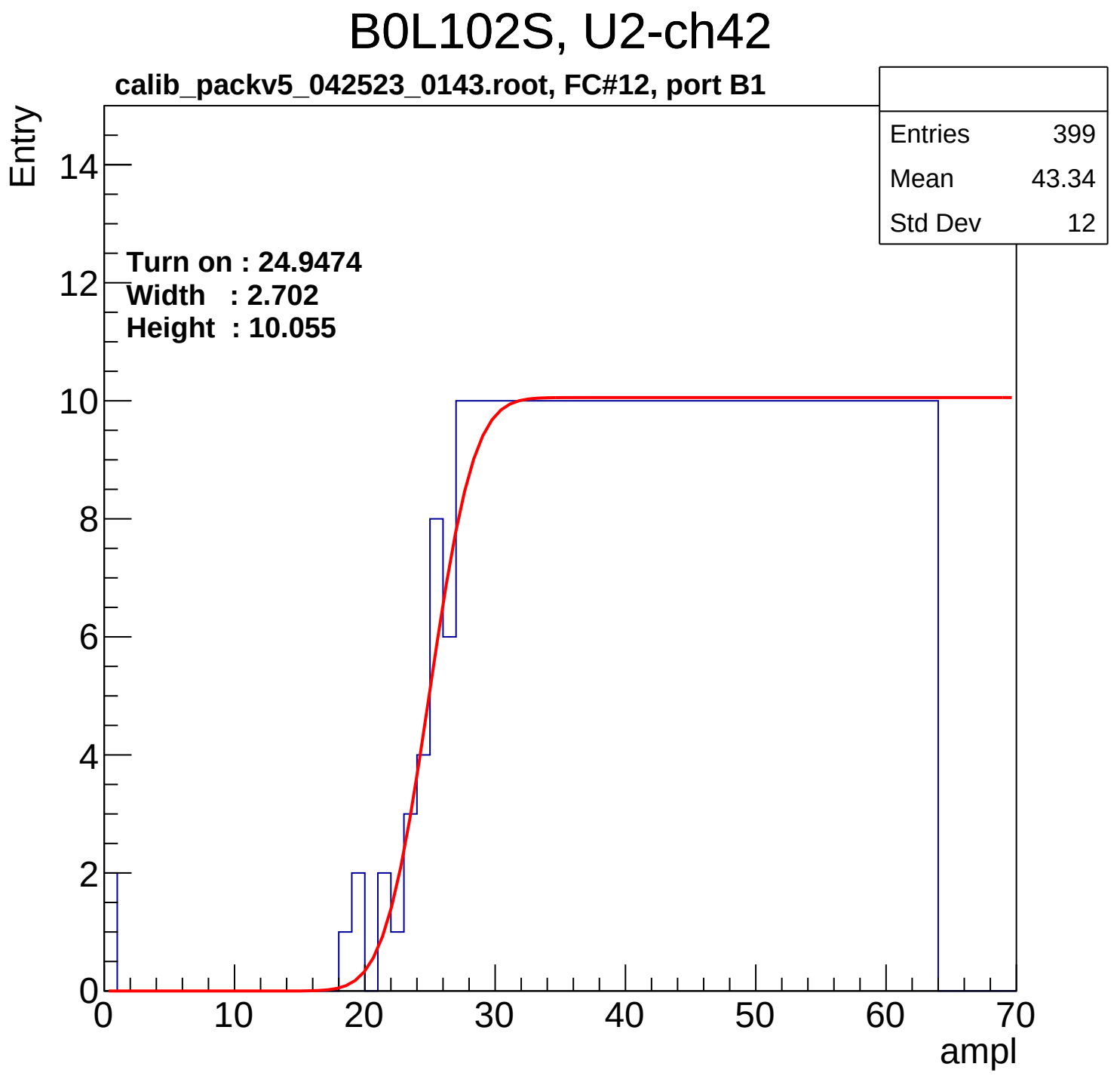
B0L102S, U2-ch42
calib_packv5_042523_0143.root, FC#12, port B1
Entries 399
Mean 43.34
Std Dev 12
Turn on : 24.9474
Width : 2.702
Height : 10.055
Entry
ampl
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6
8
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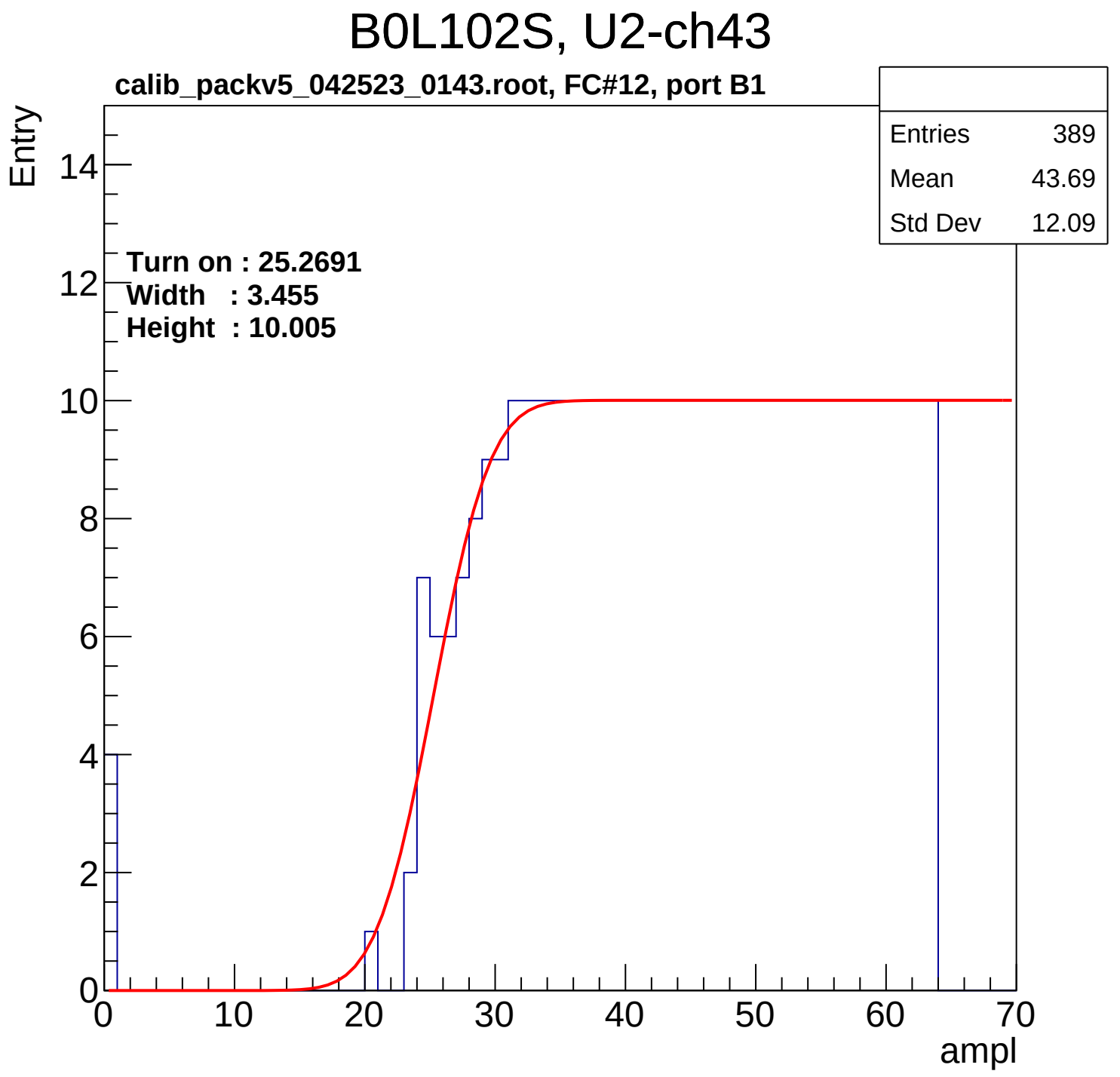
B0L102S, U2-ch43
calib_packv5_042523_0143.root, FC#12, port B1
Entries 389
Mean 43.69
Std Dev 12.09
Turn on : 25.2691
Width : 3.455
Height : 10.005
Entry
ampl
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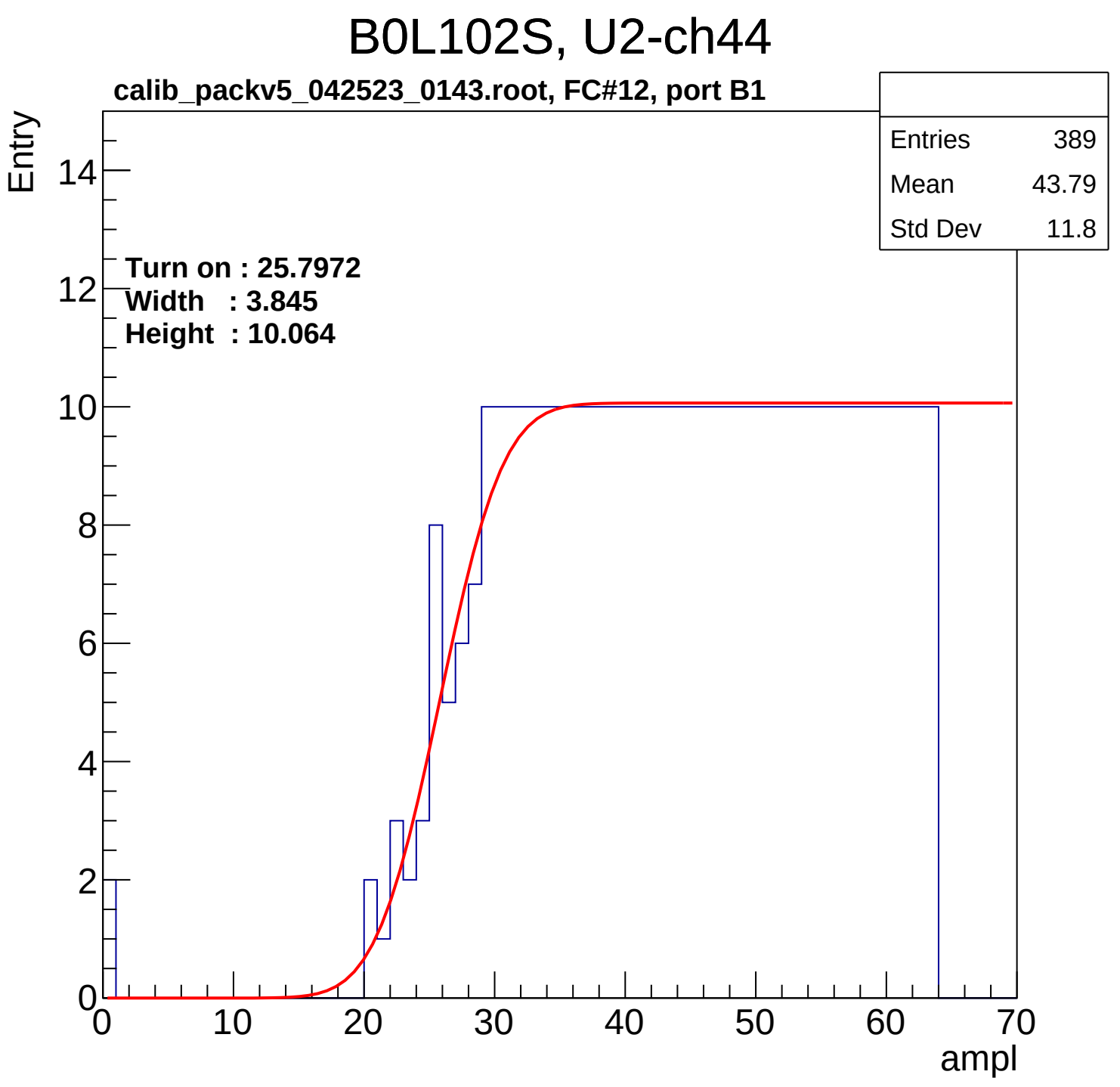
B0L102S, U2-ch44
calib_packv5_042523_0143.root, FC#12, port B1
Entries 389
Mean 43.79
Std Dev 11.8
Turn on : 25.7972
Width : 3.845
Height : 10.064
Entry
ampl
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4
6
8
10
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0
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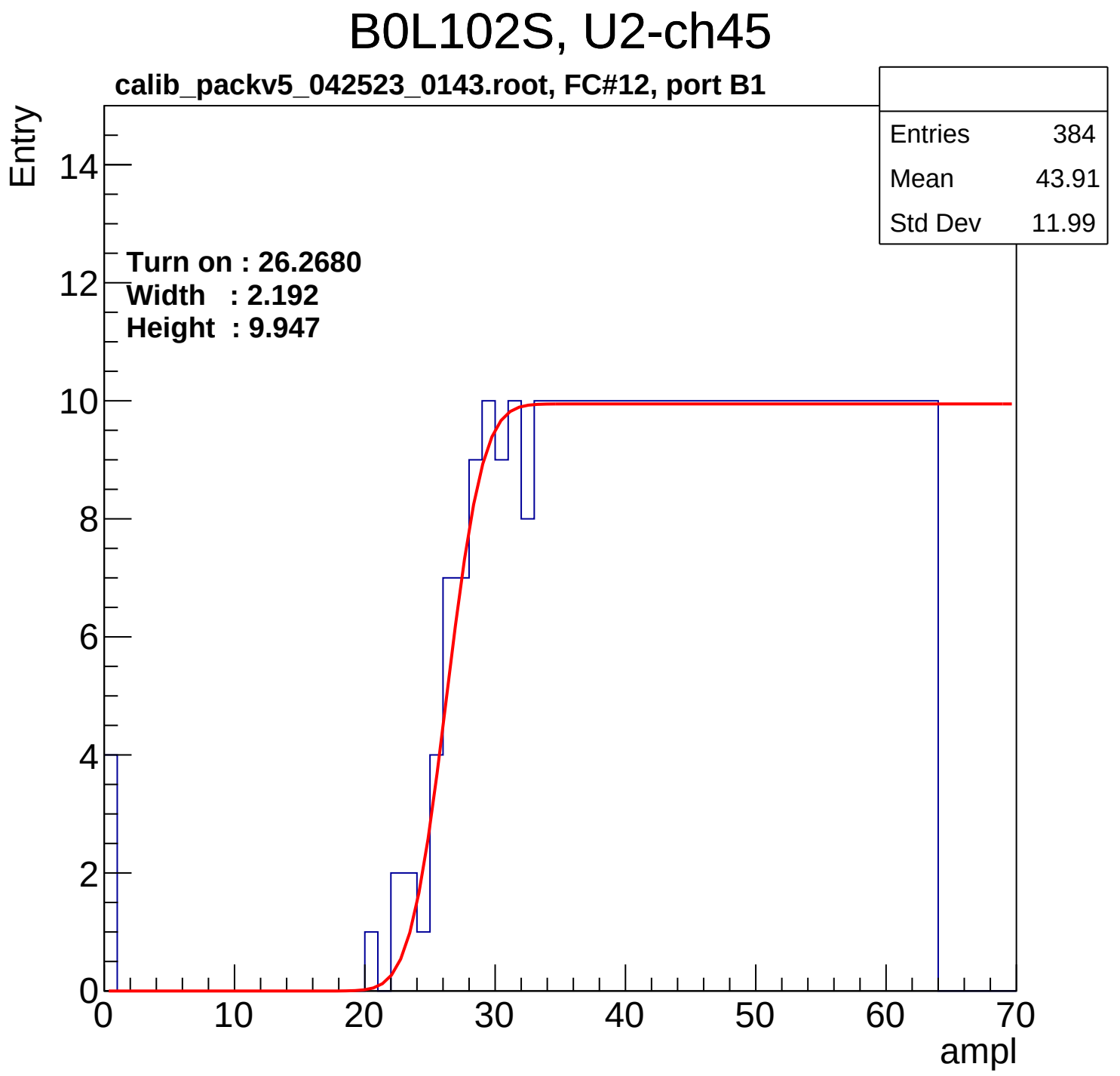
B0L102S, U2-ch45
calib_packv5_042523_0143.root, FC#12, port B1
Entries 384
Mean 43.91
Std Dev 11.99
Turn on : 26.2680
Width : 2.192
Height : 9.947
Entry
ampl
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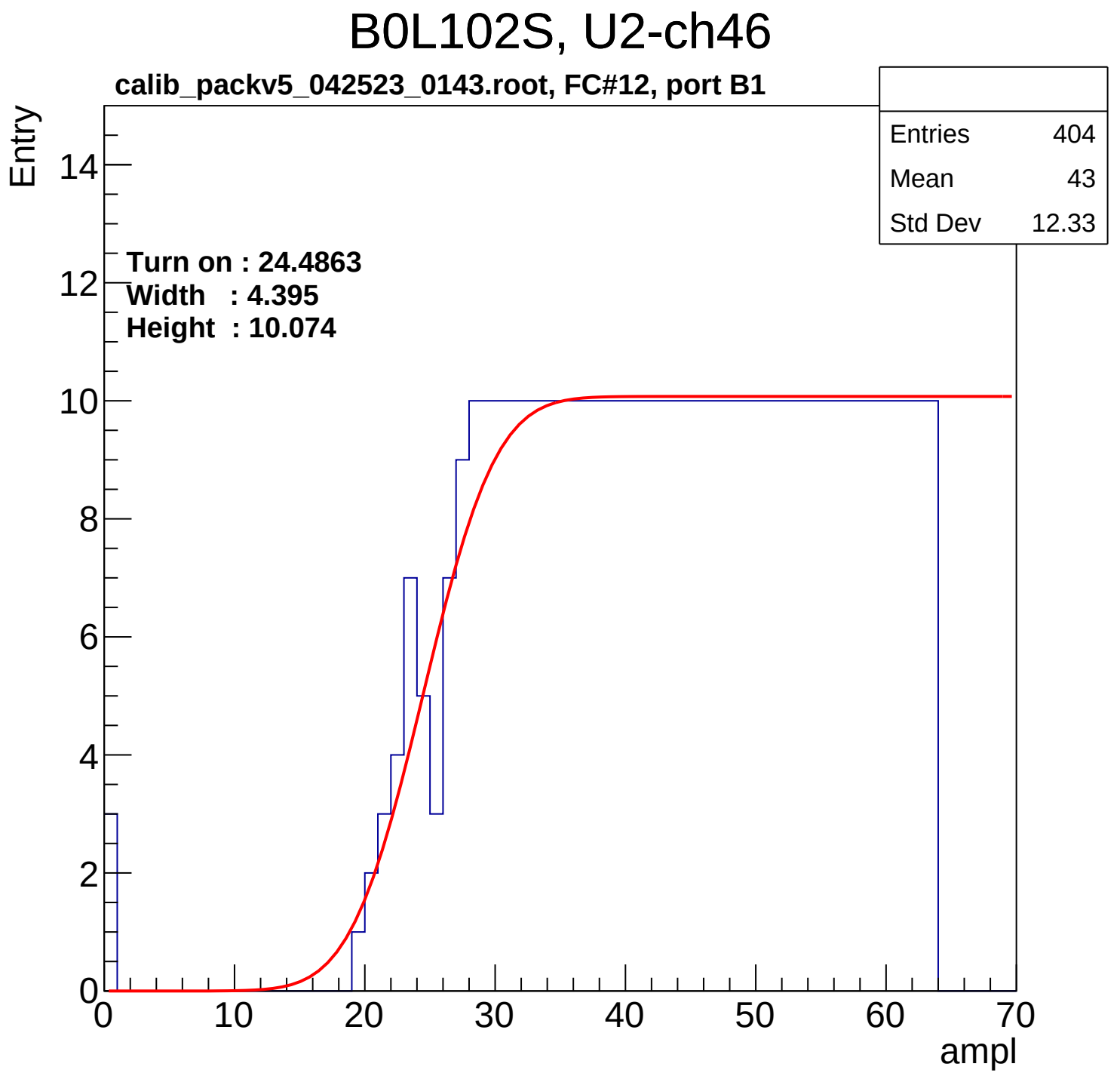
B0L102S, U2-ch46
calib_packv5_042523_0143.root, FC#12, port B1
Entries 404
Mean 43
Std Dev 12.33
Turn on : 24.4863
Width : 4.395
Height : 10.074
Entry
ampl
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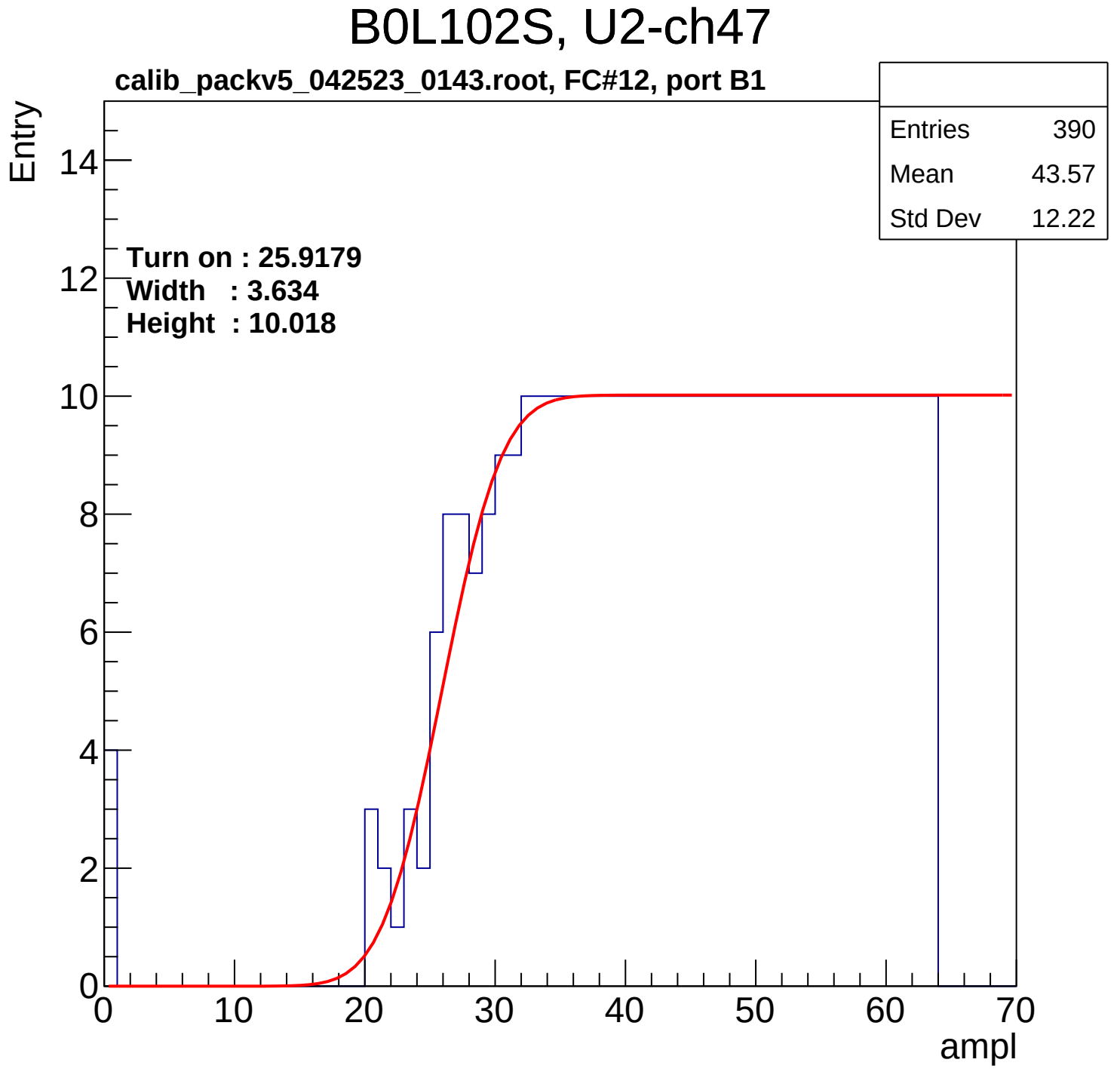
B0L102S, U2-ch47
calib_packv5_042523_0143.root, FC#12, port B1
Entries 390
Mean 43.57
Std Dev 12.22
Turn on : 25.9179
Width : 3.634
Height : 10.018
Entry
ampl
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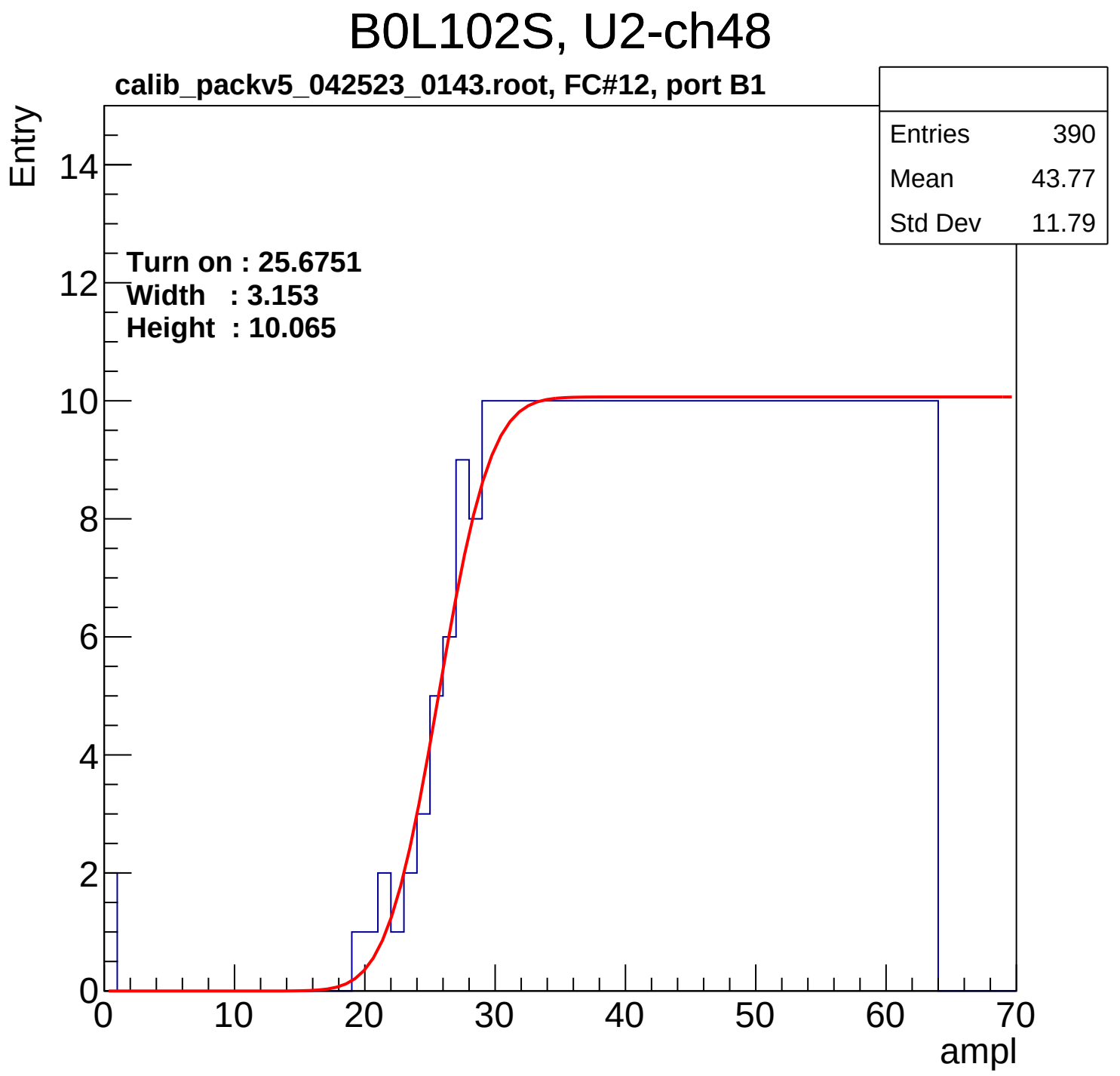
B0L102S, U2-ch48
calib_packv5_042523_0143.root, FC#12, port B1
Entries 390
Mean 43.77
Std Dev 11.79
Turn on : 25.6751
Width : 3.153
Height : 10.065
Entry
ampl
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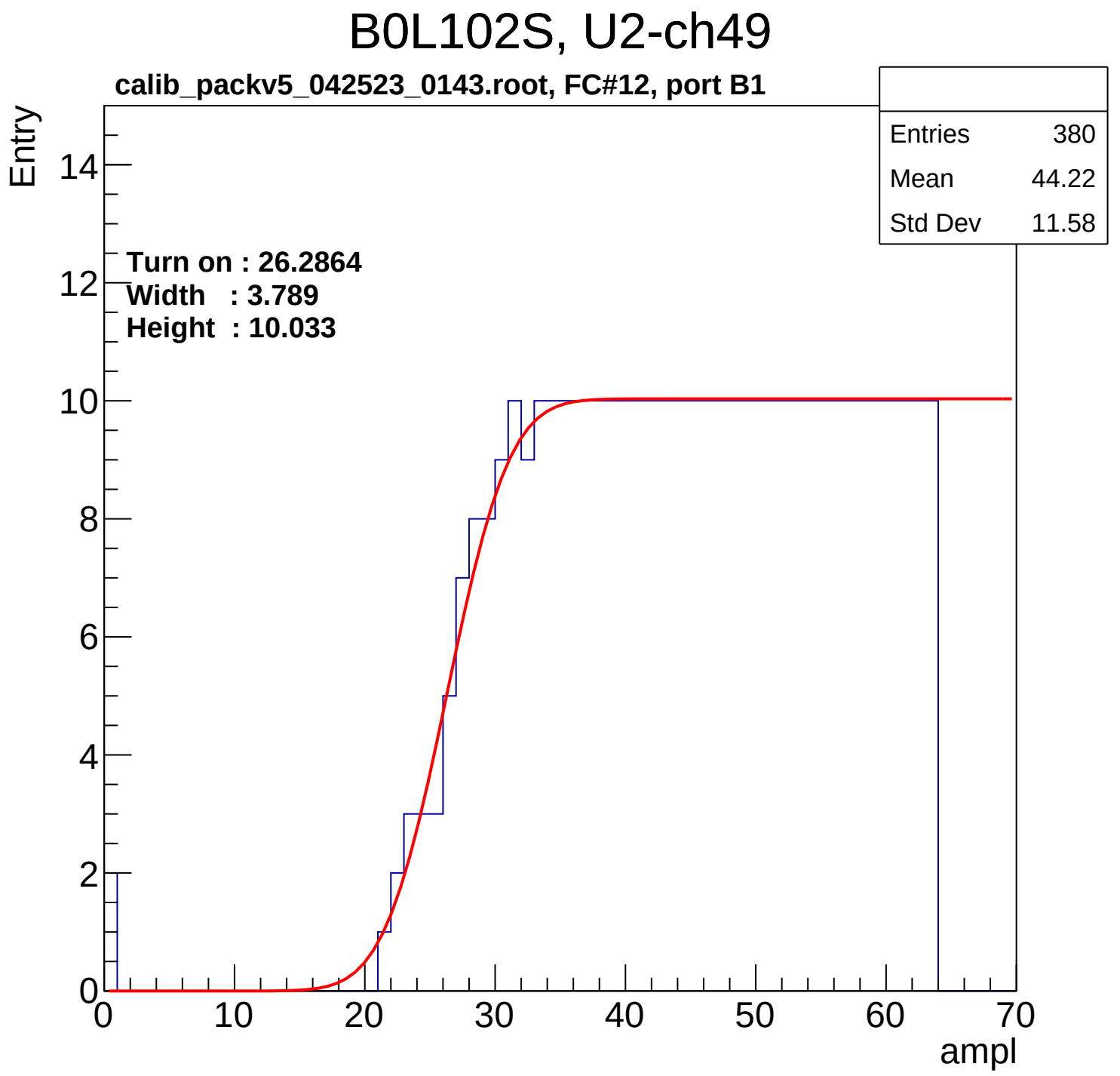
B0L102S, U2-ch49
calib_packv5_042523_0143.root, FC#12, port B1
Entries 380
Mean 44.22
Std Dev 11.58
Turn on : 26.2864
Width : 3.789
Height : 10.033
Entry
ampl
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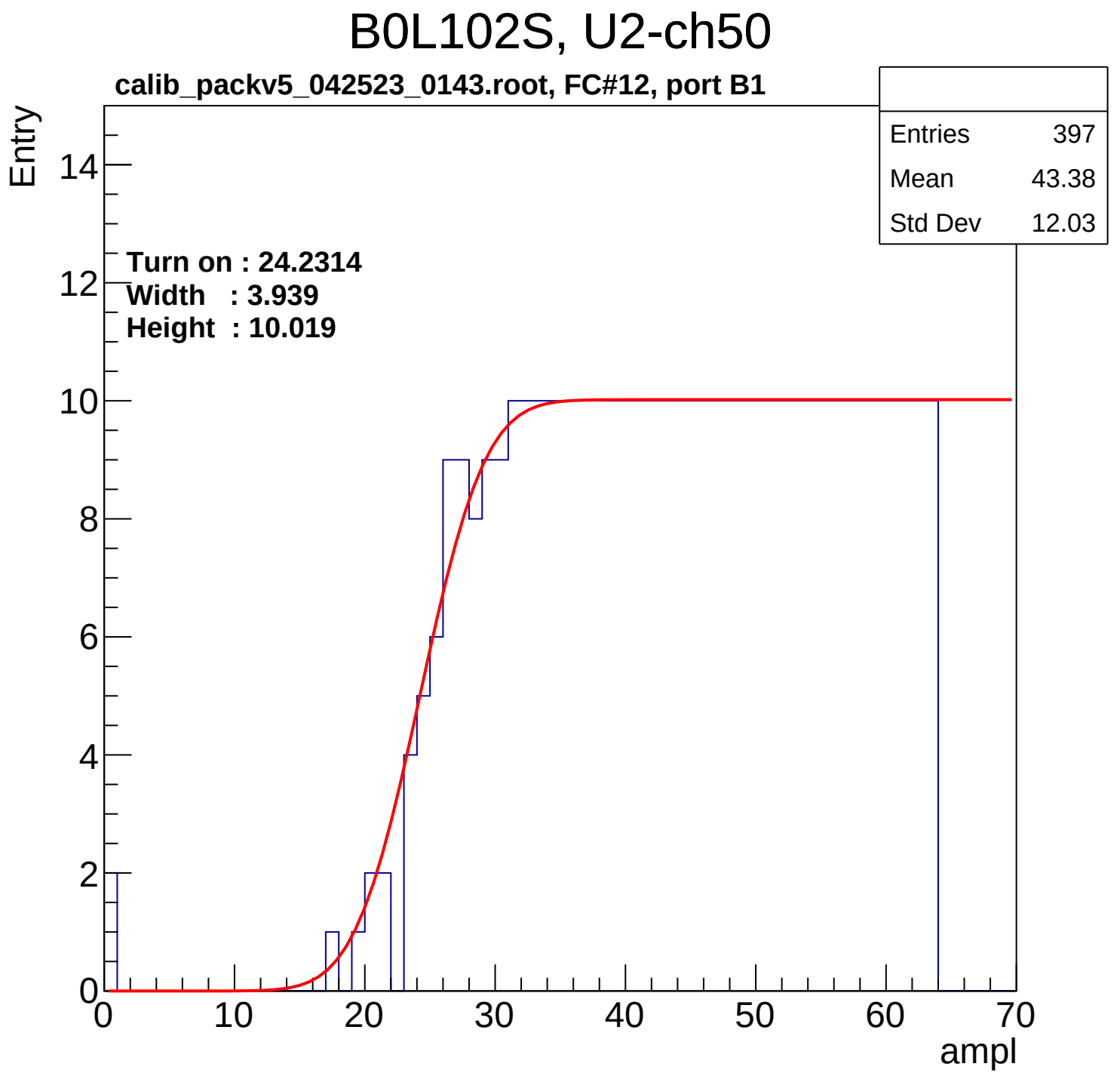
B0L102S, U2-ch50
calib_packv5_042523_0143.root, FC#12, port B1
Entries 397
Mean 43.38
Std Dev 12.03
Turn on : 24.2314
Width : 3.939
Height : 10.019
Entry
ampl
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8
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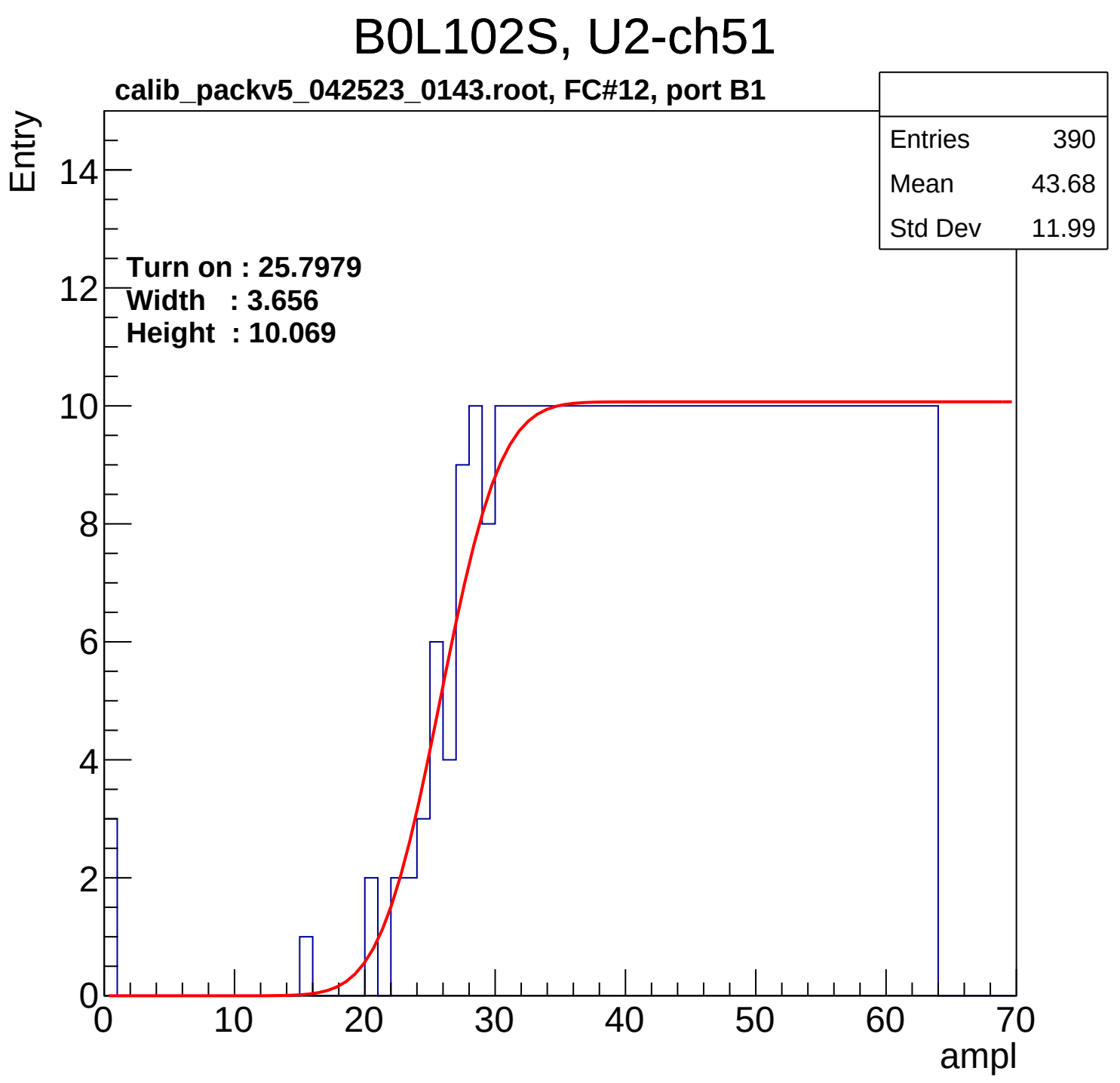
B0L102S, U2-ch51
calib_packv5_042523_0143.root, FC#12, port B1
Entries 390
Mean 43.68
Std Dev 11.99
Turn on : 25.7979
Width : 3.656
Height : 10.069
Entry
ampl
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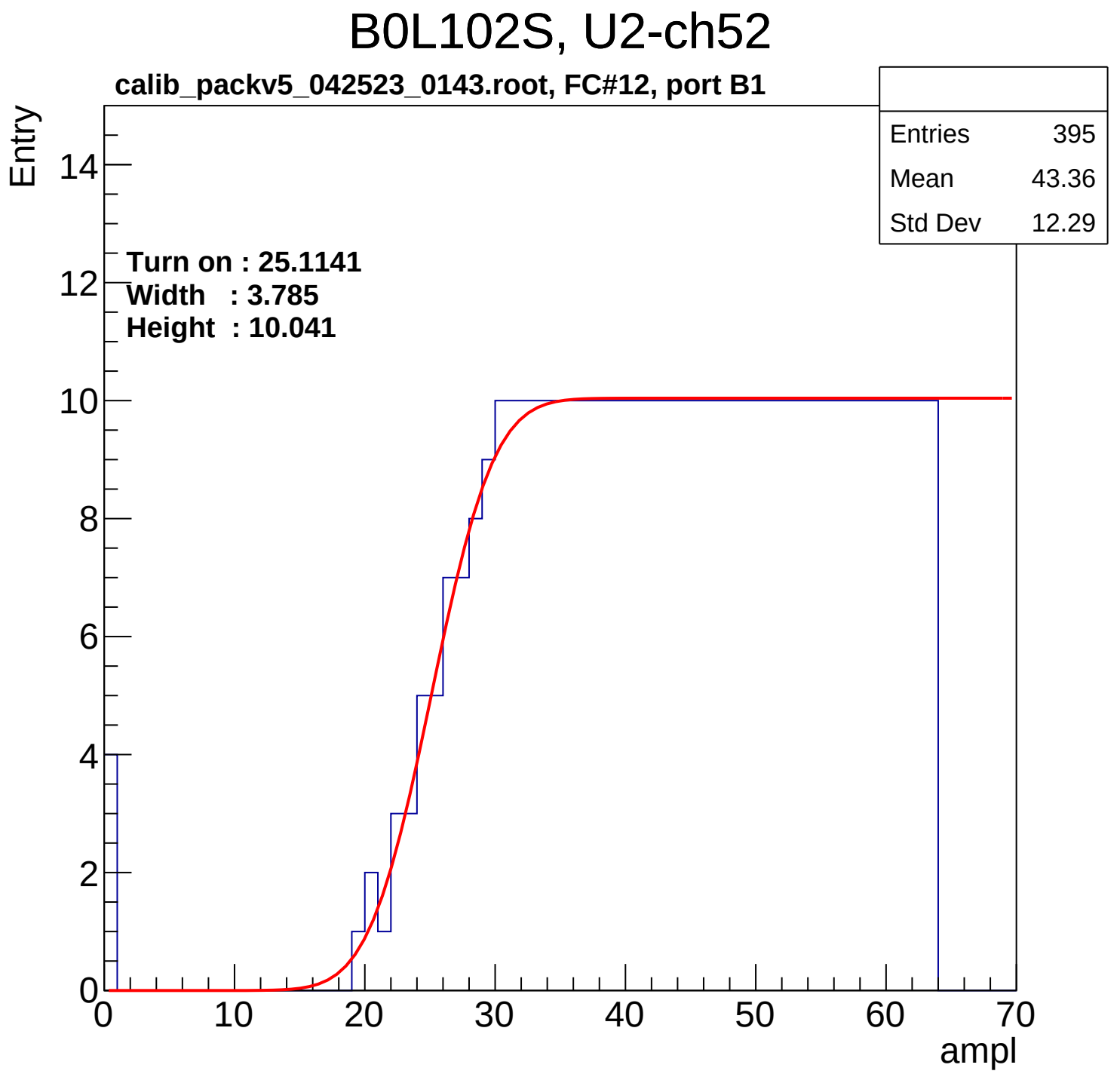
B0L102S, U2-ch52
calib_packv5_042523_0143.root, FC#12, port B1
Entries 395
Mean 43.36
Std Dev 12.29
Turn on : 25.1141
Width : 3.785
Height : 10.041
Entry
ampl
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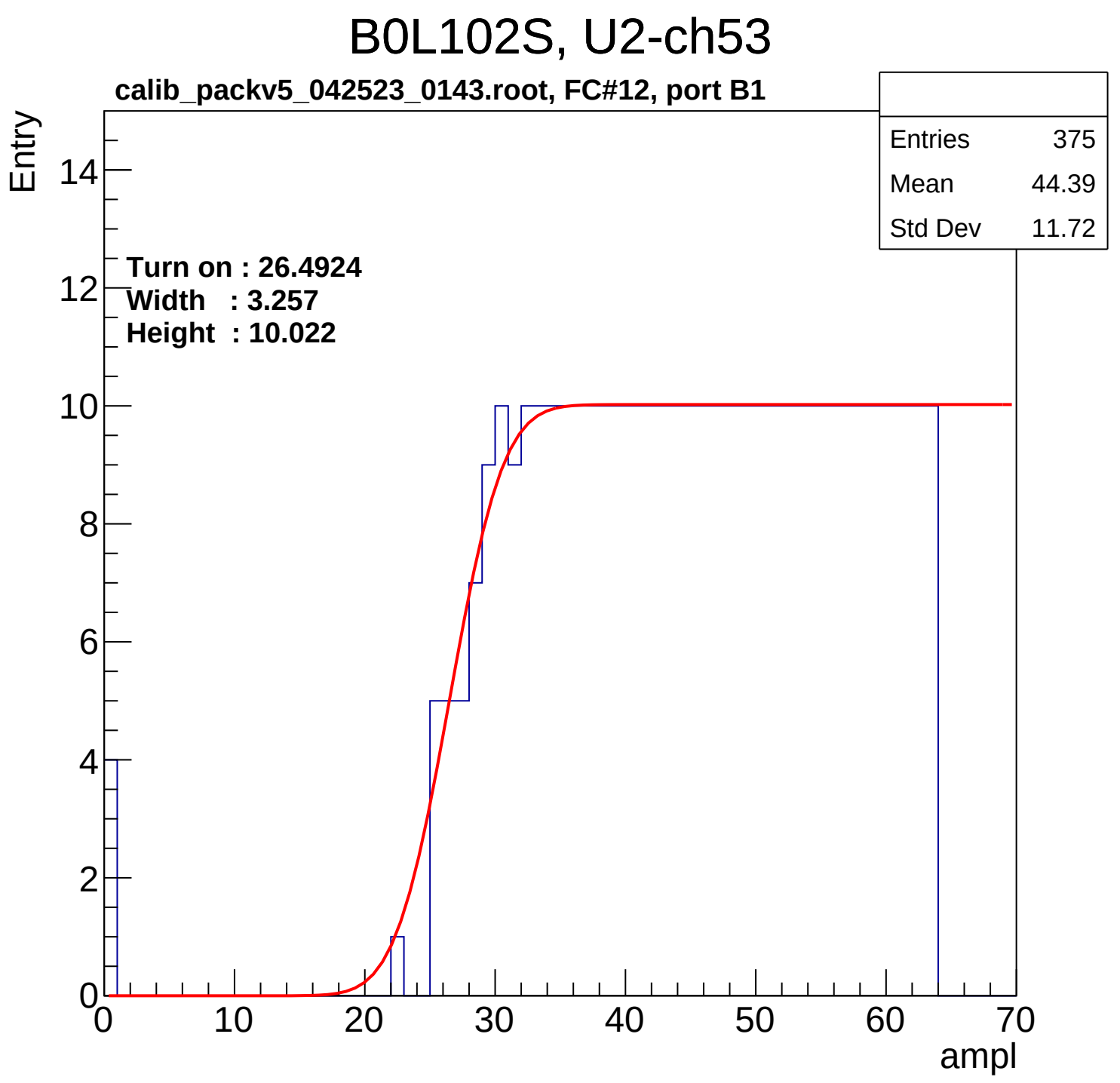
B0L102S, U2-ch53
calib_packv5_042523_0143.root, FC#12, port B1
Entries 375
Mean 44.39
Std Dev 11.72
Turn on : 26.4924
Width : 3.257
Height : 10.022
Entry
ampl
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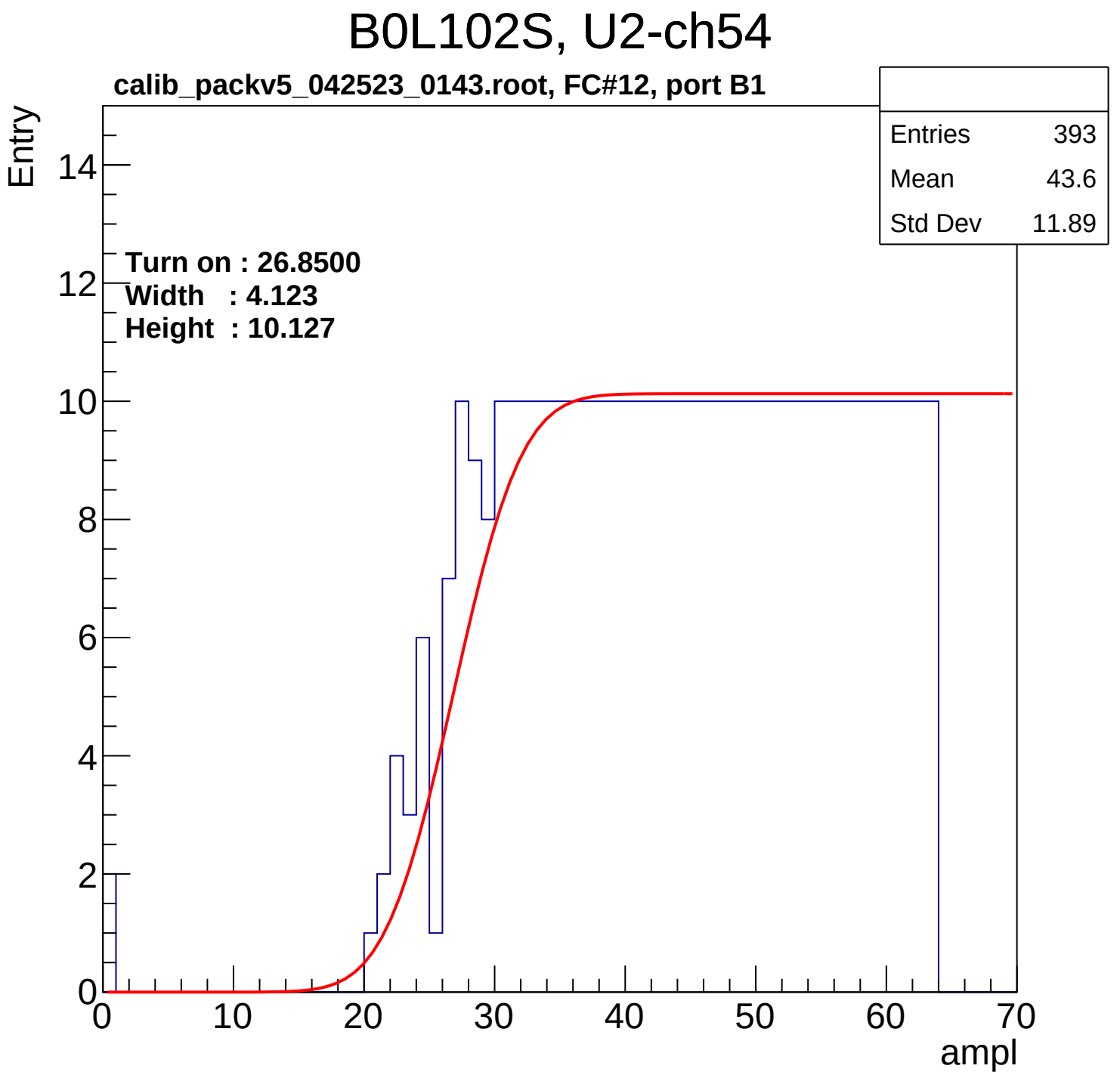
B0L102S, U2-ch54
calib_packv5_042523_0143.root, FC#12, port B1
Entries 393
Mean 43.6
Std Dev 11.89
Turn on : 26.8500
Width : 4.123
Height : 10.127
Entry
ampl
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6
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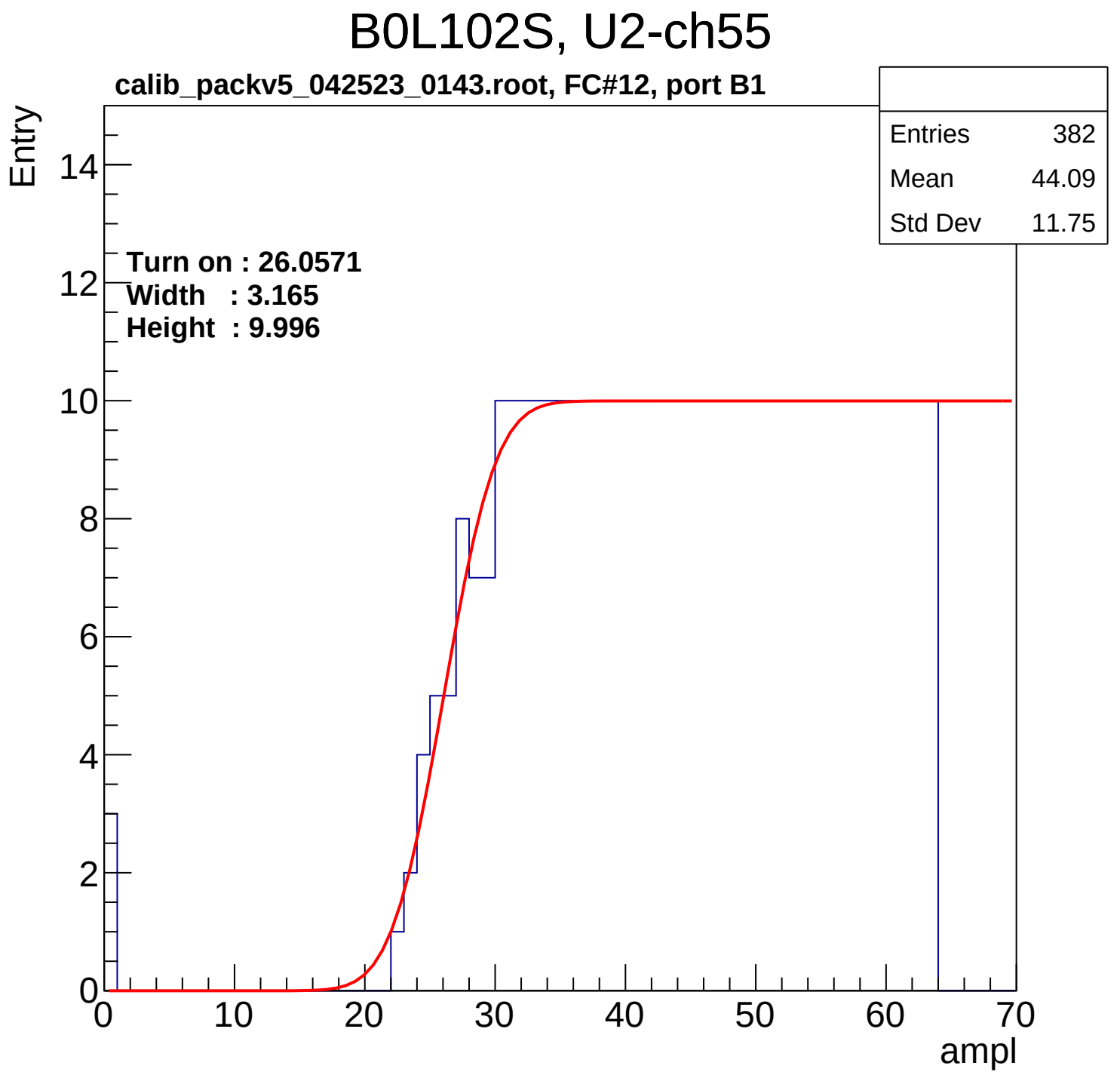
B0L102S, U2-ch55
calib_packv5_042523_0143.root, FC#12, port B1
Entries 382
Mean 44.09
Std Dev 11.75
Turn on : 26.0571
Width : 3.165
Height : 9.996
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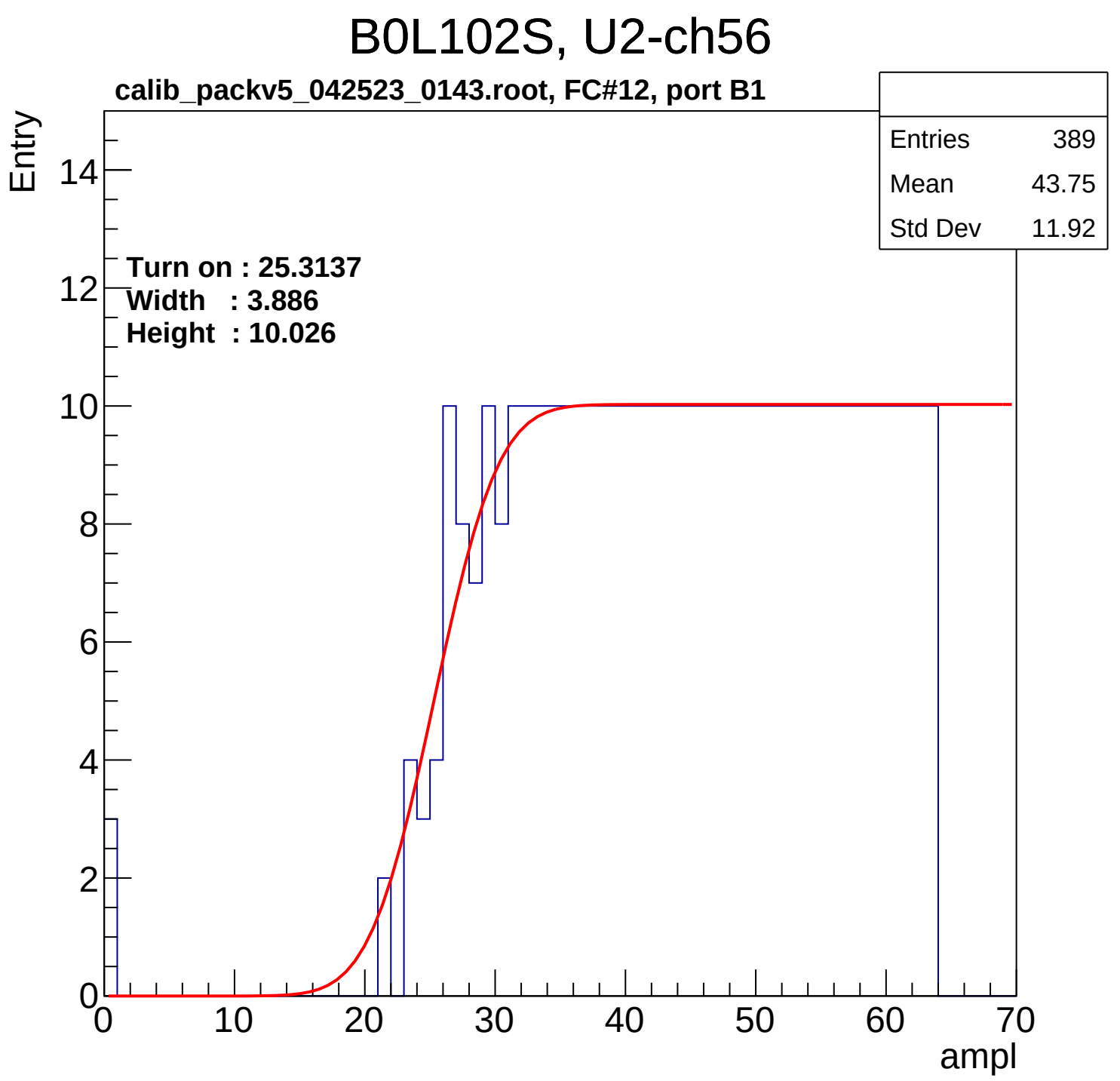
B0L102S, U2-ch56
calib_packv5_042523_0143.root, FC#12, port B1
Entries 389
Mean 43.75
Std Dev 11.92
Turn on : 25.3137
Width : 3.886
Height : 10.026
Entry
ampl
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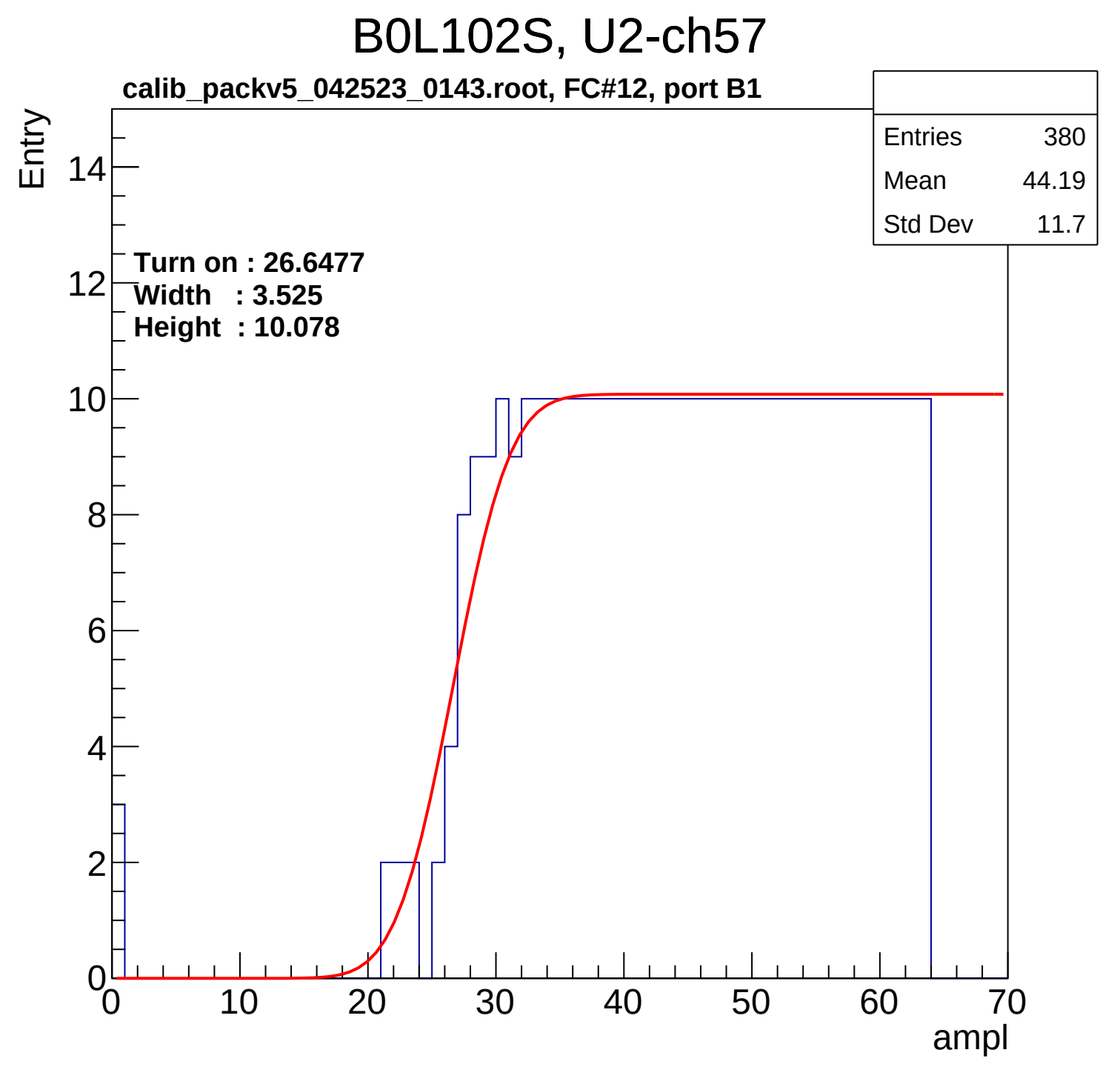
B0L102S, U2-ch57
calib_packv5_042523_0143.root, FC#12, port B1
Entries 380
Mean 44.19
Std Dev 11.7
Turn on : 26.6477
Width : 3.525
Height : 10.078
Entry
ampl
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6
8
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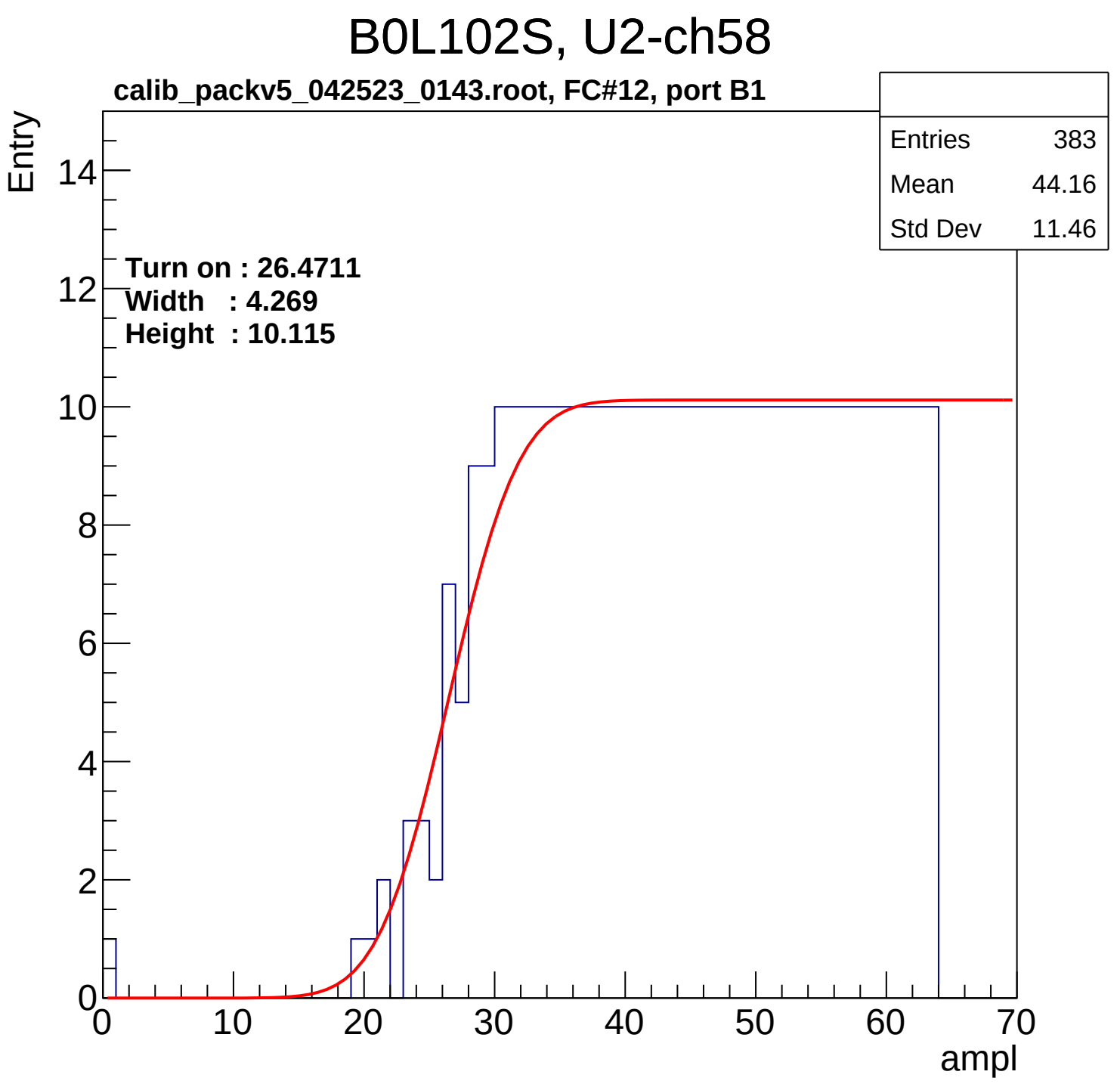
B0L102S, U2-ch58
calib_packv5_042523_0143.root, FC#12, port B1
Entries 383
Mean 44.16
Std Dev 11.46
Turn on : 26.4711
Width : 4.269
Height : 10.115
Entry
ampl
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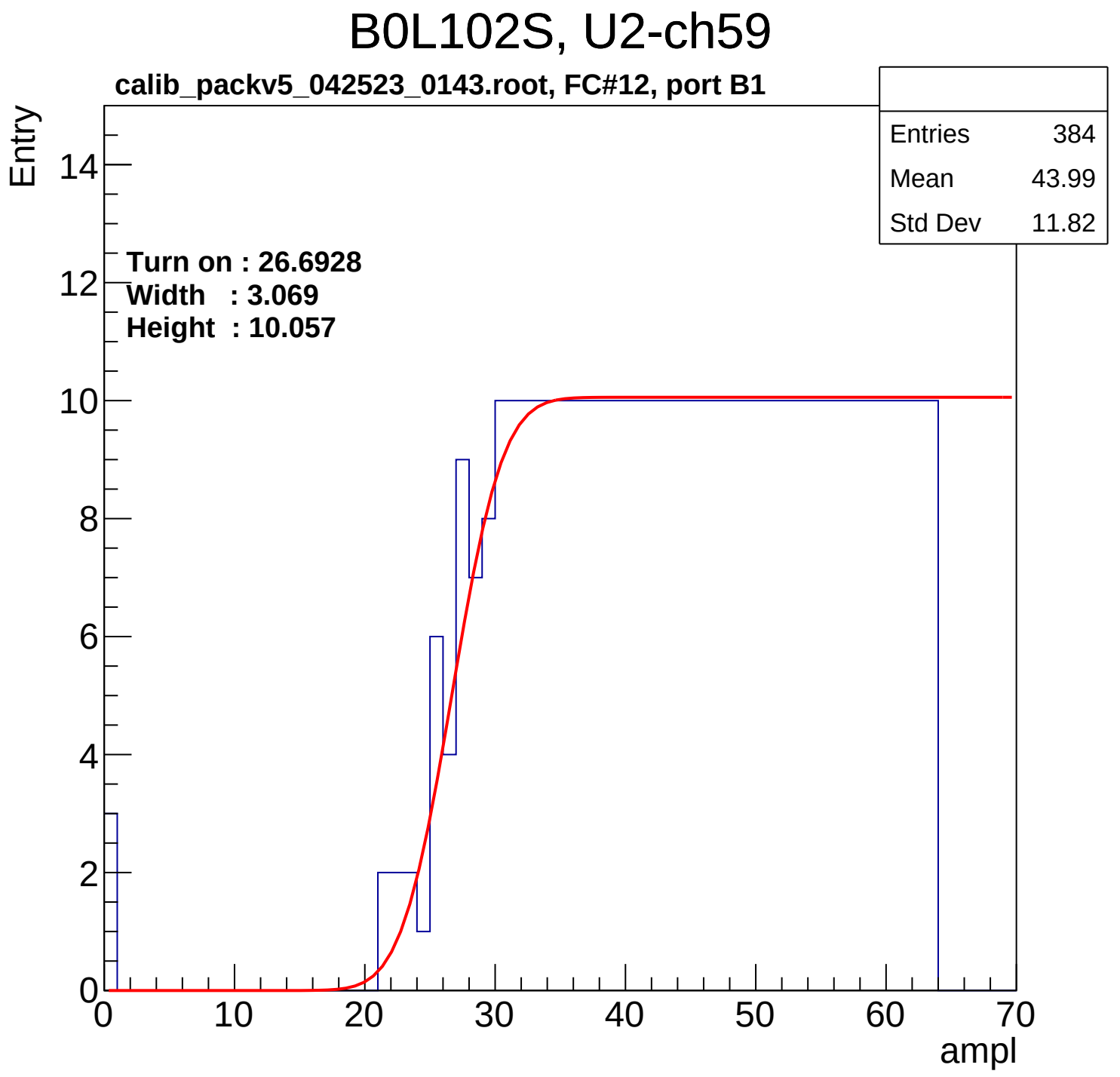
B0L102S, U2-ch59
calib_packv5_042523_0143.root, FC#12, port B1
Entries 384
Mean 43.99
Std Dev 11.82
Turn on : 26.6928
Width : 3.069
Height : 10.057
Entry
ampl
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2
4
6
8
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0
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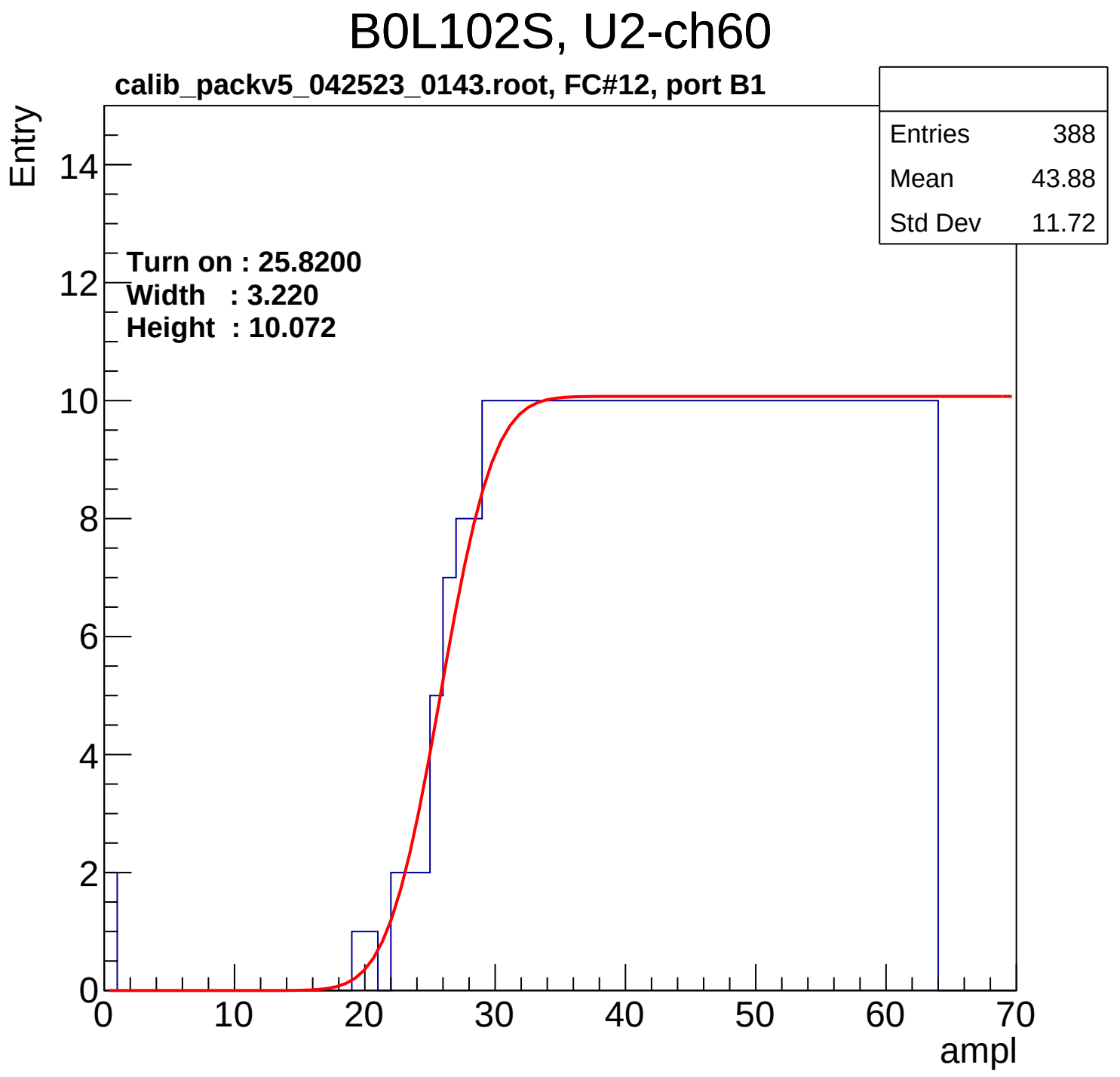
B0L102S, U2-ch60
calib_packv5_042523_0143.root, FC#12, port B1
Entries 388
Mean 43.88
Std Dev 11.72
Turn on : 25.8200
Width : 3.220
Height : 10.072
Entry
ampl
0
2
4
6
8
10
12
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0
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40
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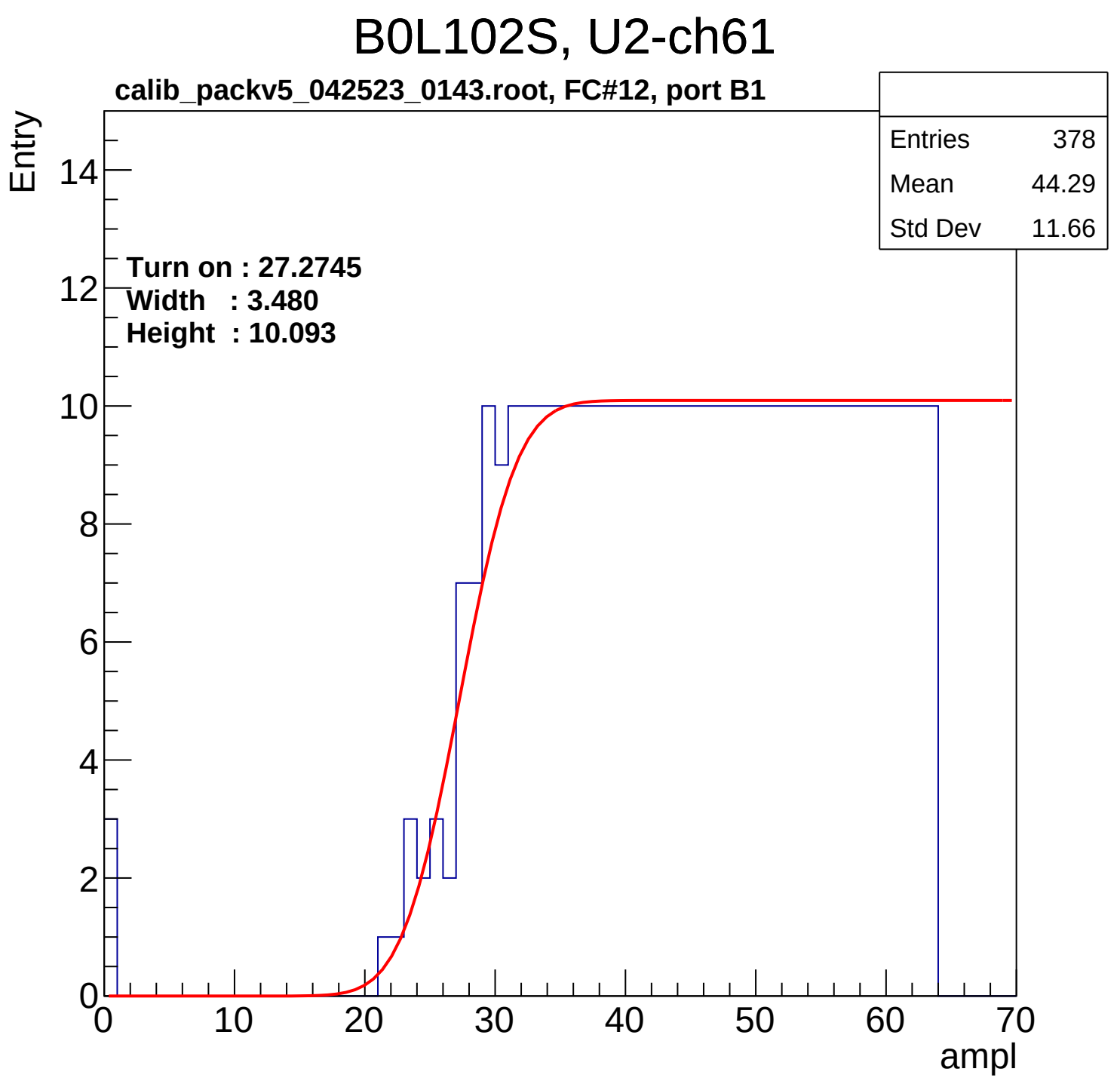
B0L102S, U2-ch61
calib_packv5_042523_0143.root, FC#12, port B1
Entries 378
Mean 44.29
Std Dev 11.66
Turn on : 27.2745
Width : 3.480
Height : 10.093
Entry
ampl
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2
4
6
8
10
12
14
0
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60
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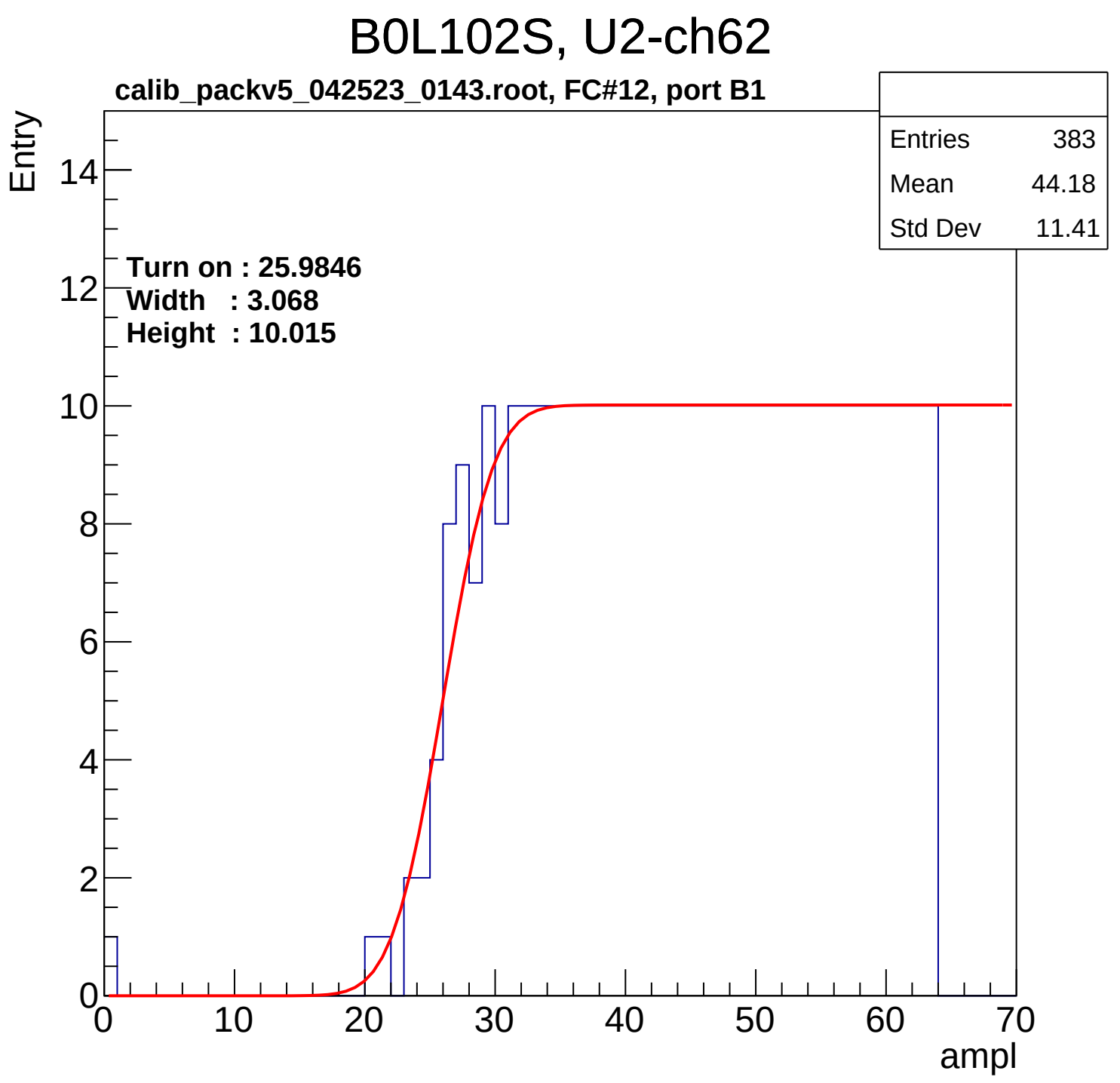
B0L102S, U2-ch62
calib_packv5_042523_0143.root, FC#12, port B1
Entries 383
Mean 44.18
Std Dev 11.41
Turn on : 25.9846
Width : 3.068
Height : 10.015
Entry
ampl
0
2
4
6
8
10
12
14
0
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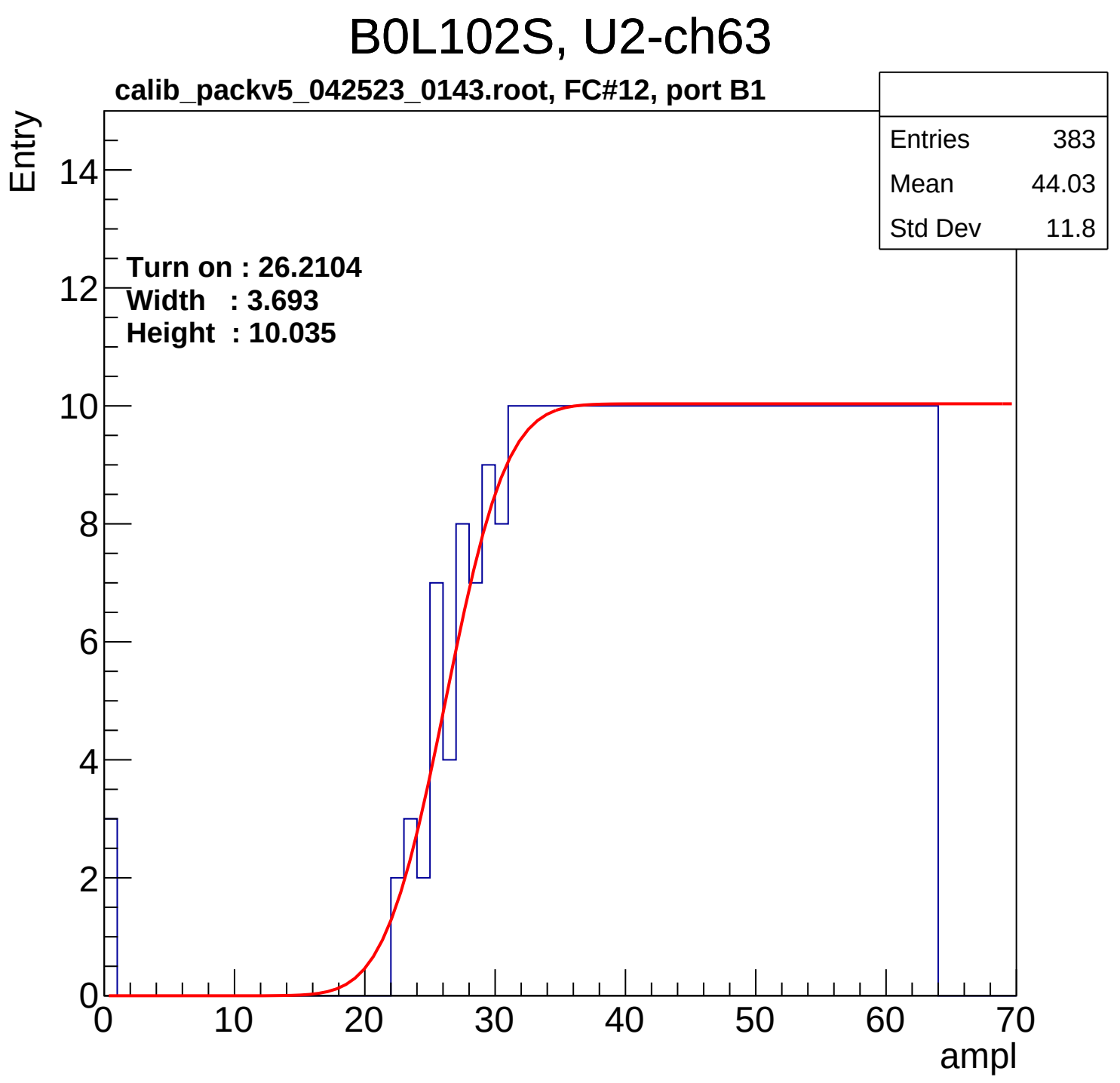
B0L102S, U2-ch63
calib_packv5_042523_0143.root, FC#12, port B1
Entries 383
Mean 44.03
Std Dev 11.8
Turn on : 26.2104
Width : 3.693
Height : 10.035
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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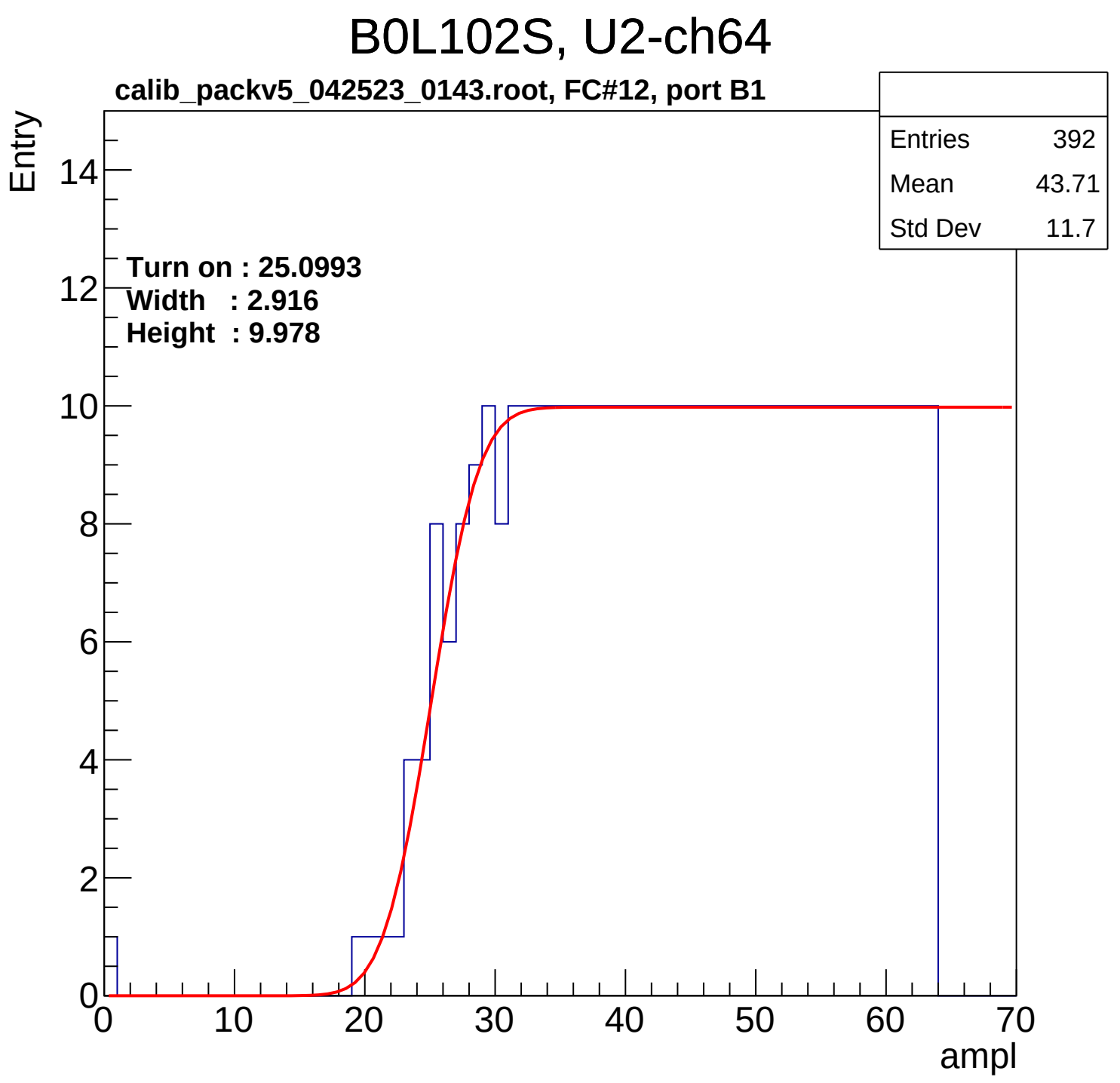
B0L102S, U2-ch64
calib_packv5_042523_0143.root, FC#12, port B1
Entries 392
Mean 43.71
Std Dev 11.7
Turn on : 25.0993
Width : 2.916
Height : 9.978
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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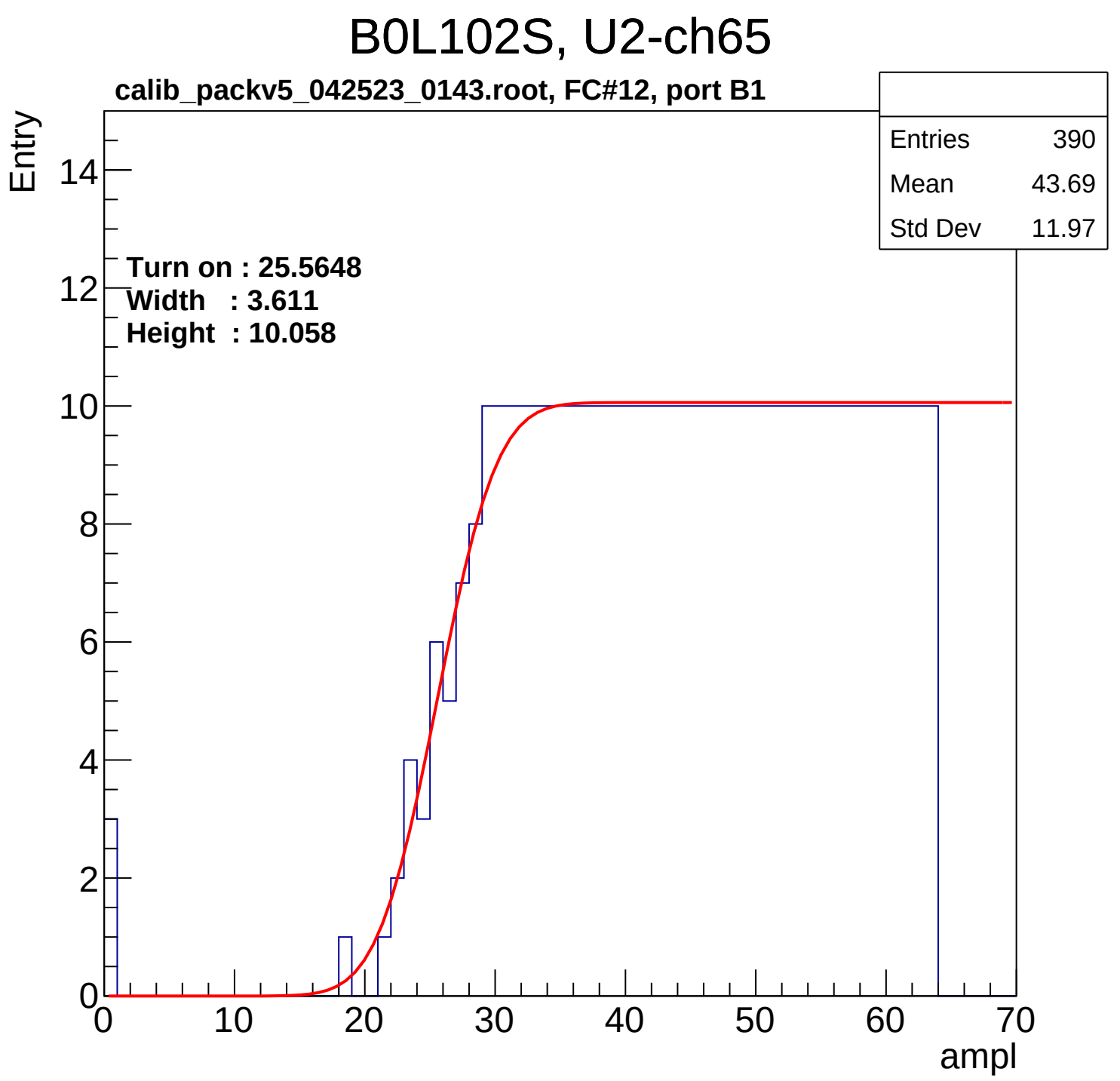
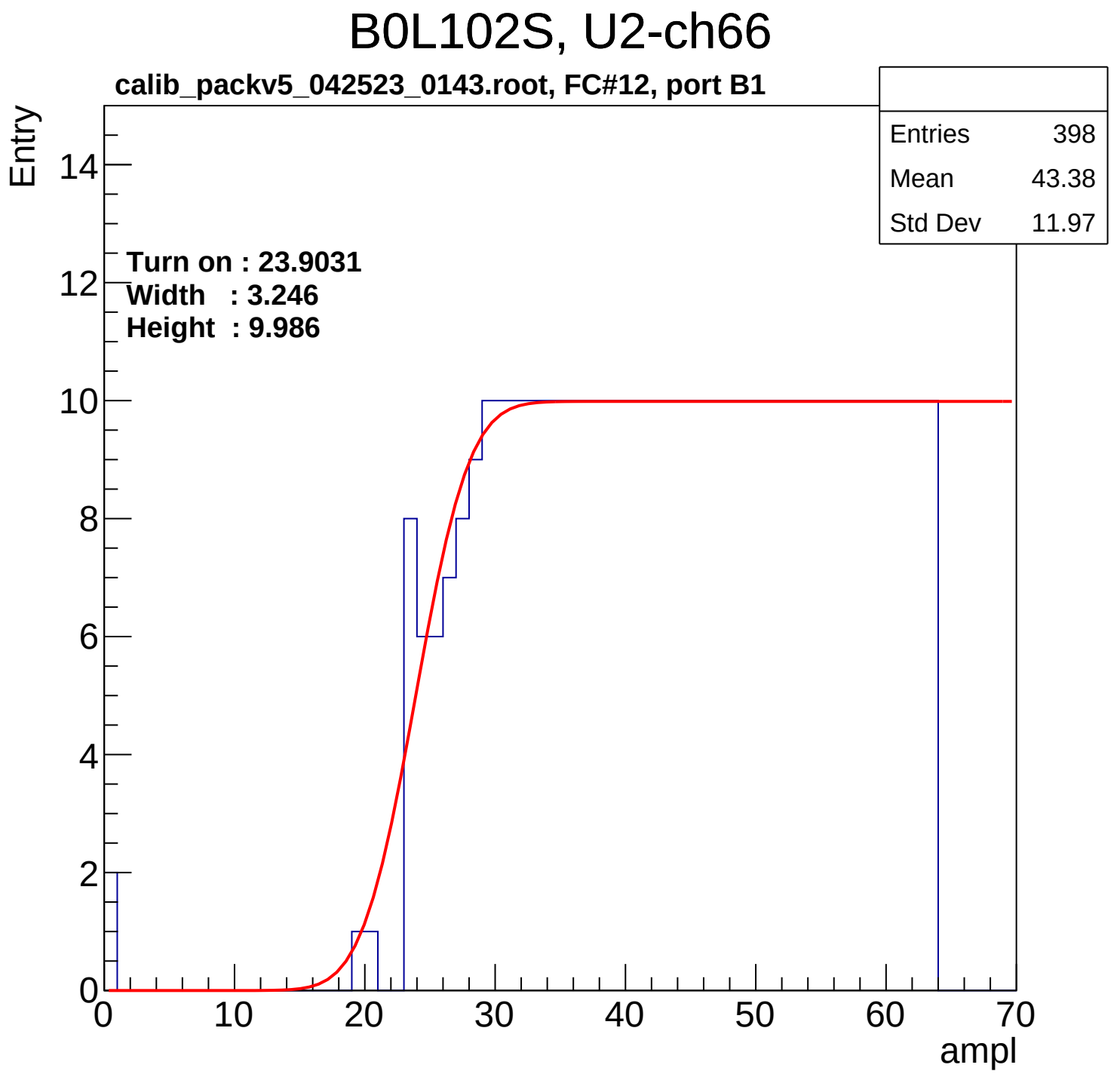

B0L102S, U2-ch65
calib_packv5_042523_0143.root, FC#12, port B1
Entries 390
Mean 43.69
Std Dev 11.97
Turn on : 25.5648
Width : 3.611
Height : 10.058
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L102S, U2-ch66
calib_packv5_042523_0143.root, FC#12, port B1
Entries 398
Mean 43.38
Std Dev 11.97
Turn on : 23.9031
Width : 3.246
Height : 9.986
Entry
ampl
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2
4
6
8
10
12
14
0
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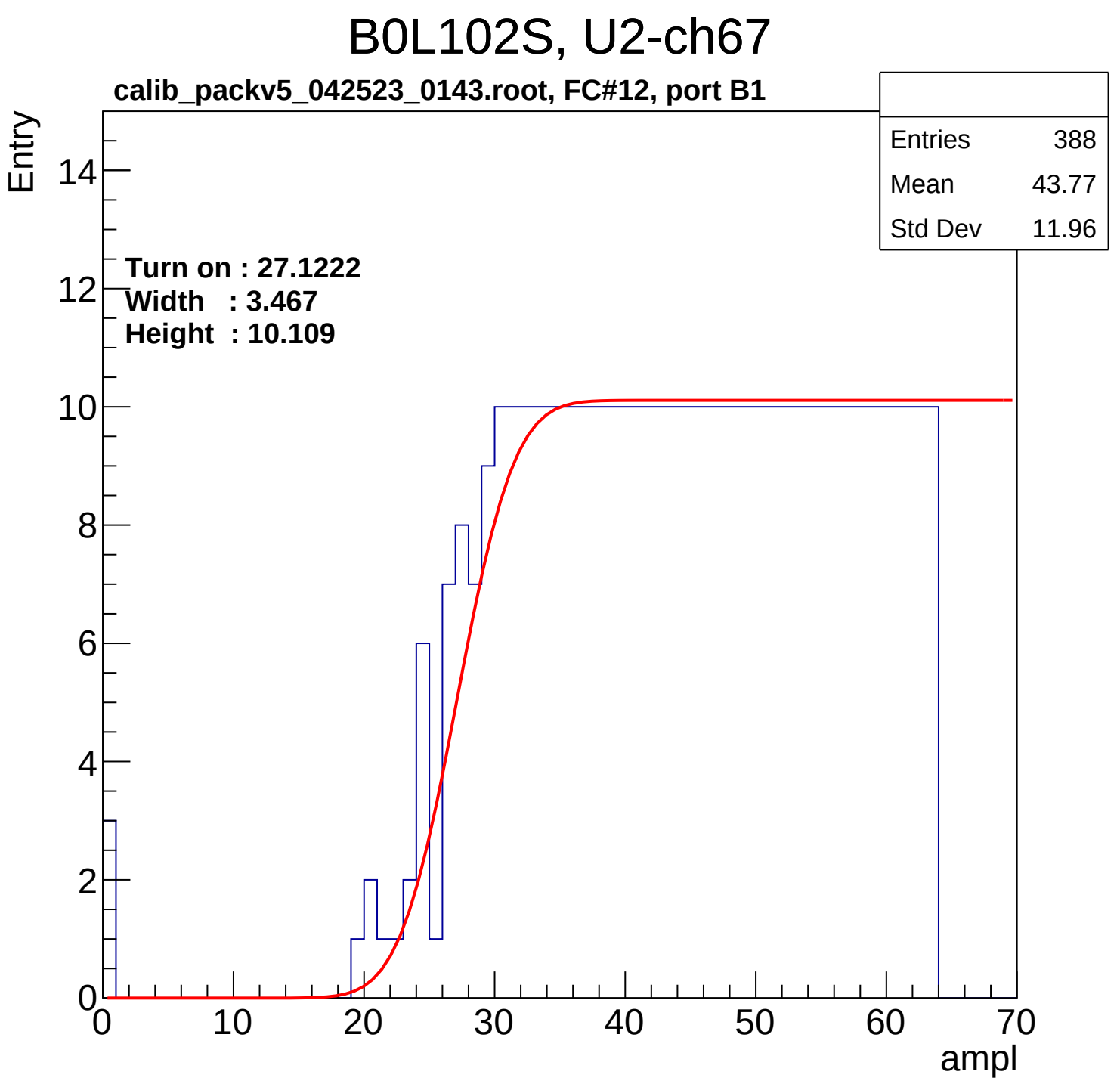
B0L102S, U2-ch67
calib_packv5_042523_0143.root, FC#12, port B1
Entries 388
Mean 43.77
Std Dev 11.96
Turn on : 27.1222
Width : 3.467
Height : 10.109
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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60
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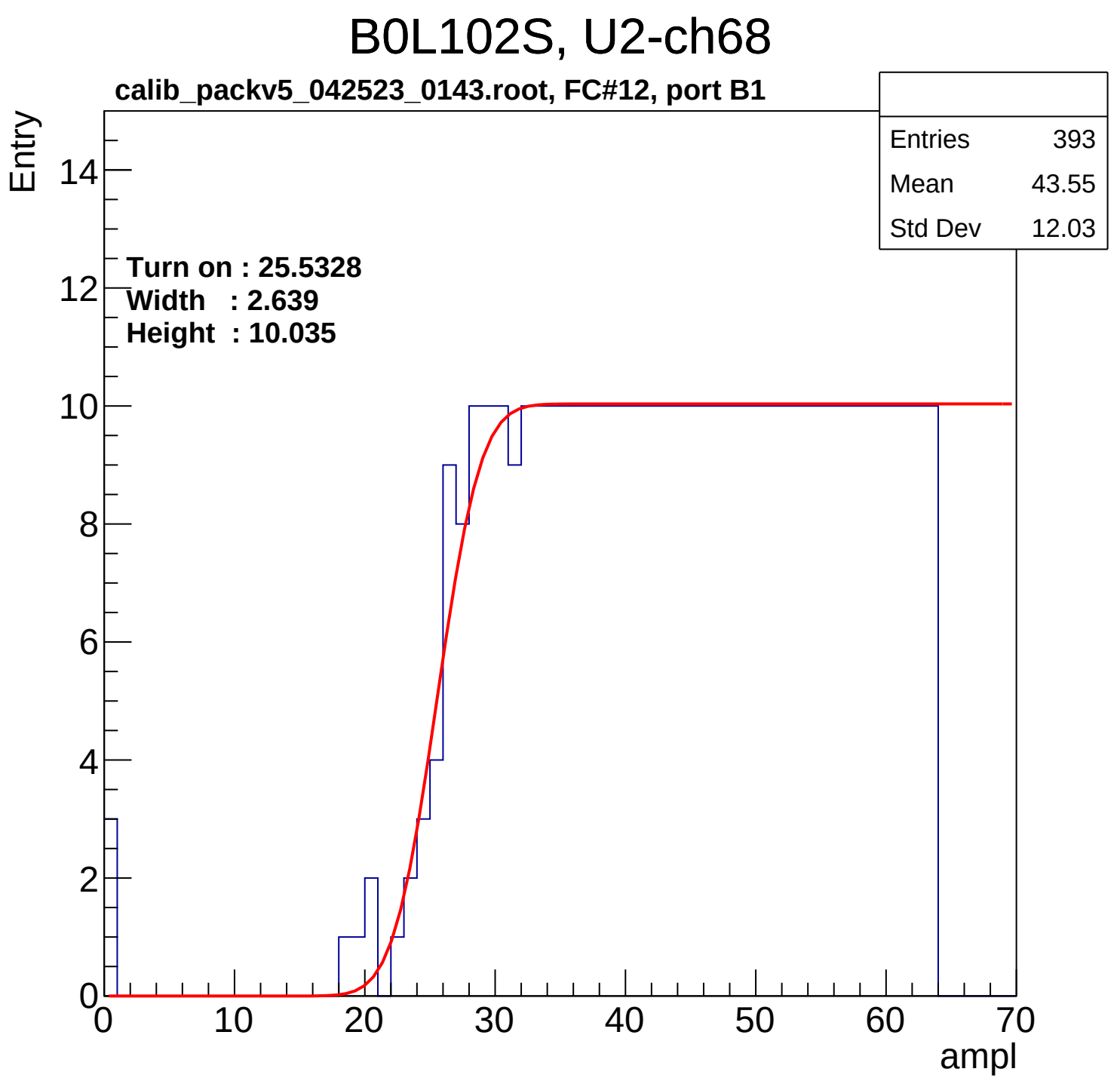
B0L102S, U2-ch68
calib_packv5_042523_0143.root, FC#12, port B1
Entries 393
Mean 43.55
Std Dev 12.03
Turn on : 25.5328
Width : 2.639
Height : 10.035
Entry
ampl
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2
4
6
8
10
12
14
0
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60
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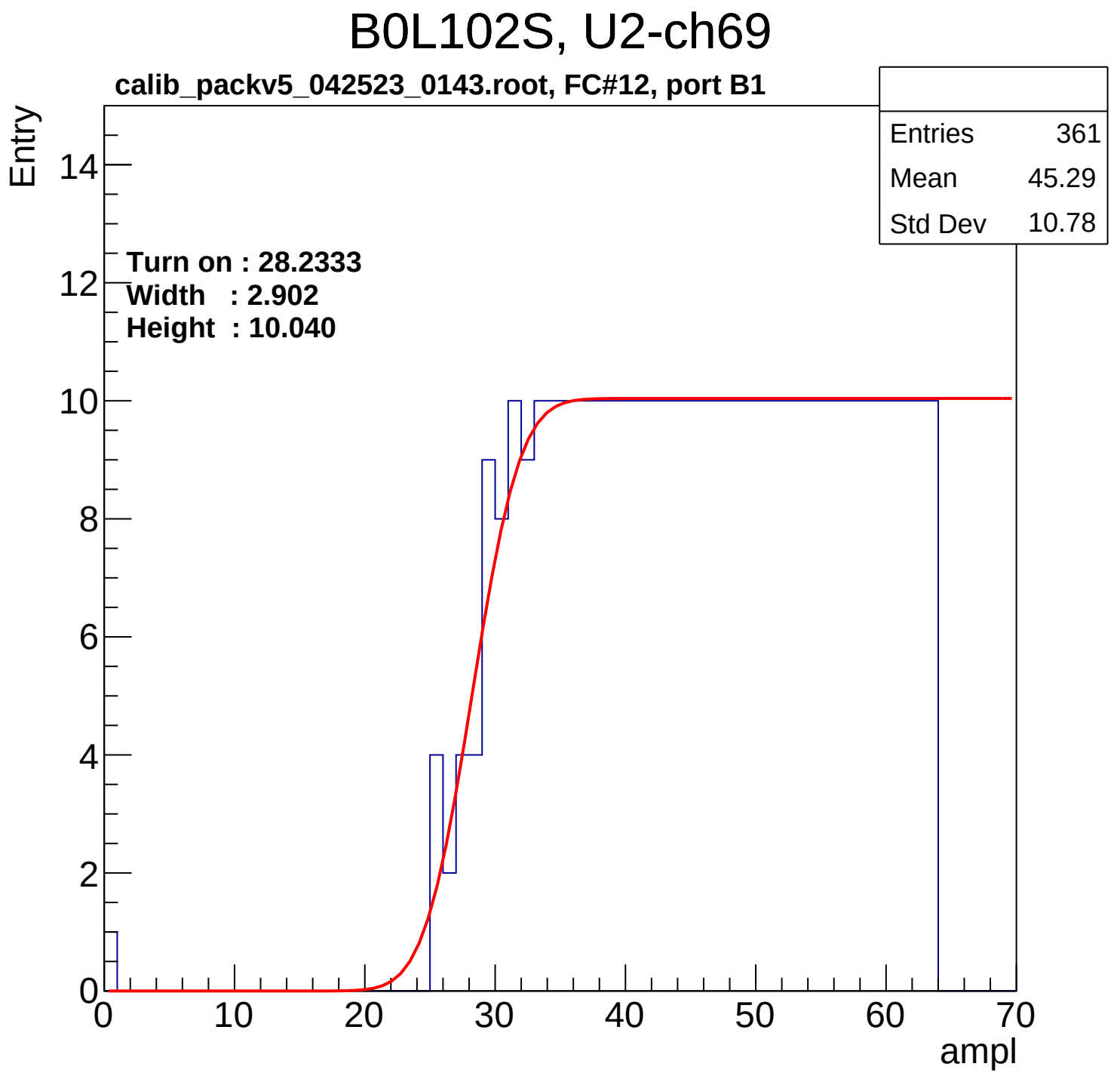
B0L102S, U2-ch69
calib_packv5_042523_0143.root, FC#12, port B1
Entries 361
Mean 45.29
Std Dev 10.78
Turn on : 28.2333
Width : 2.902
Height : 10.040
Entry
ampl
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2
4
6
8
10
12
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20
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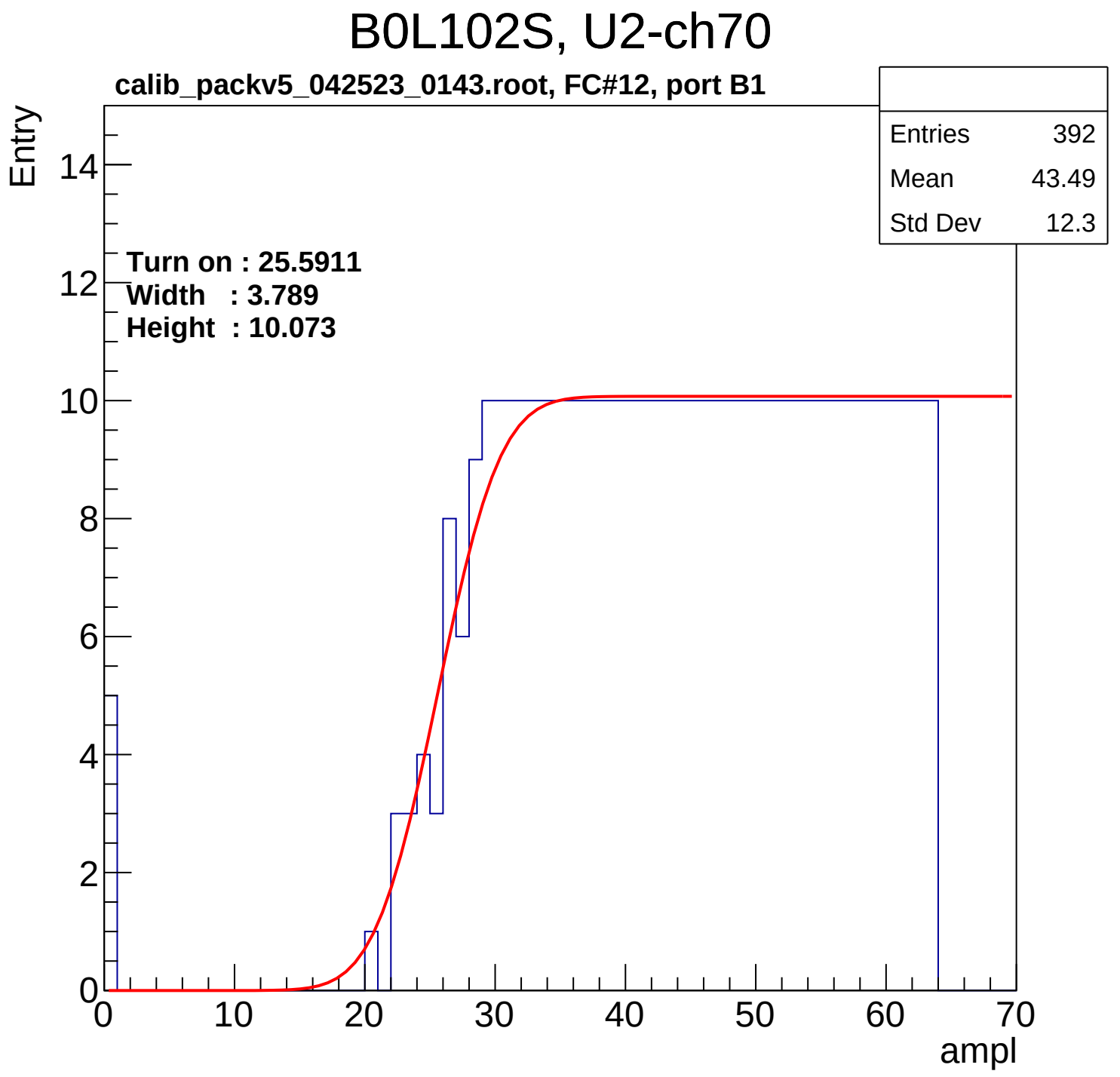
B0L102S, U2-ch70
calib_packv5_042523_0143.root, FC#12, port B1
Entries 392
Mean 43.49
Std Dev 12.3
Turn on : 25.5911
Width : 3.789
Height : 10.073
Entry
ampl
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4
6
8
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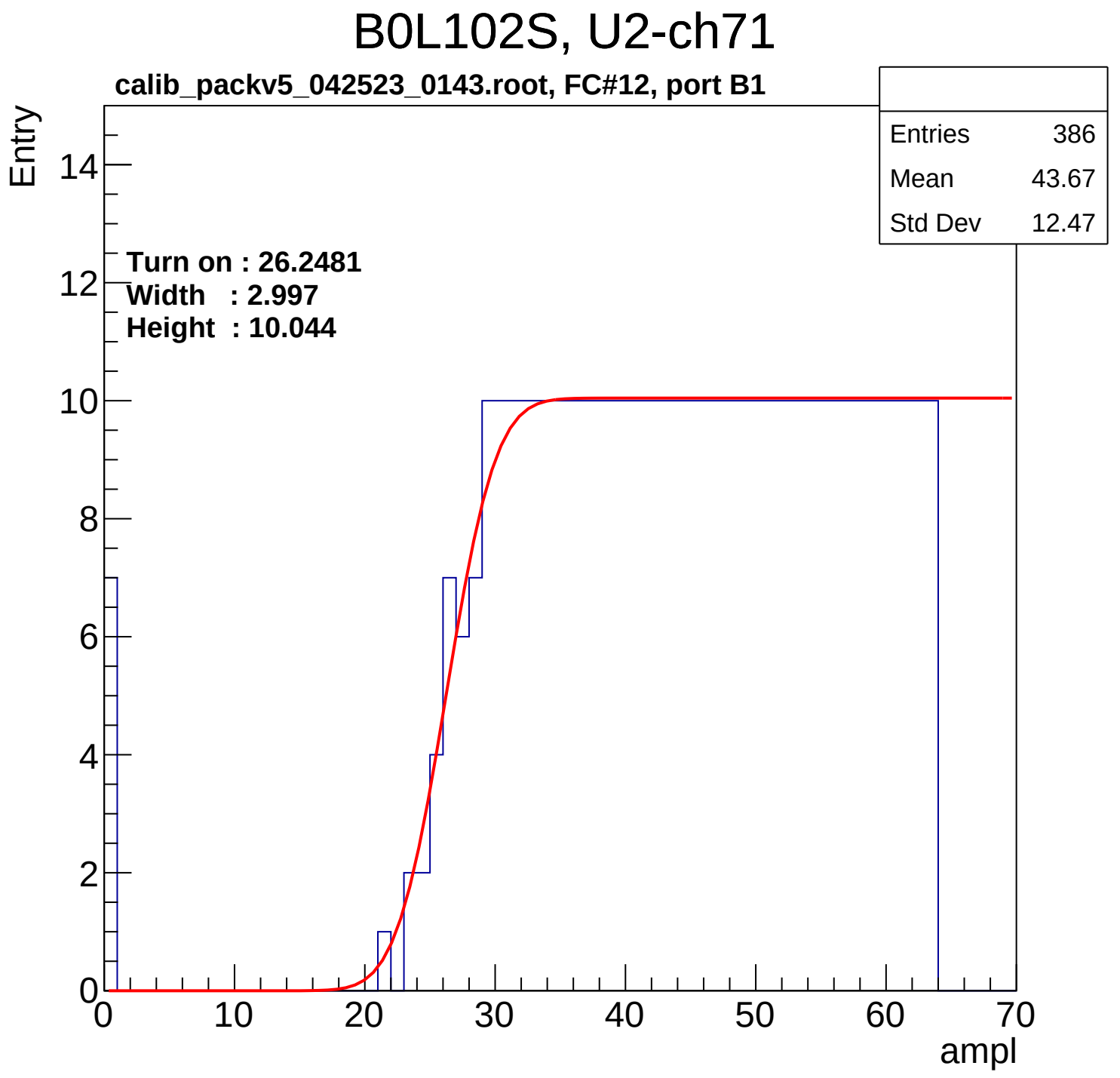
B0L102S, U2-ch71
calib_packv5_042523_0143.root, FC#12, port B1
Entries 386
Mean 43.67
Std Dev 12.47
Turn on : 26.2481
Width : 2.997
Height : 10.044
Entry
ampl
0
2
4
6
8
10
12
14
0
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20
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60
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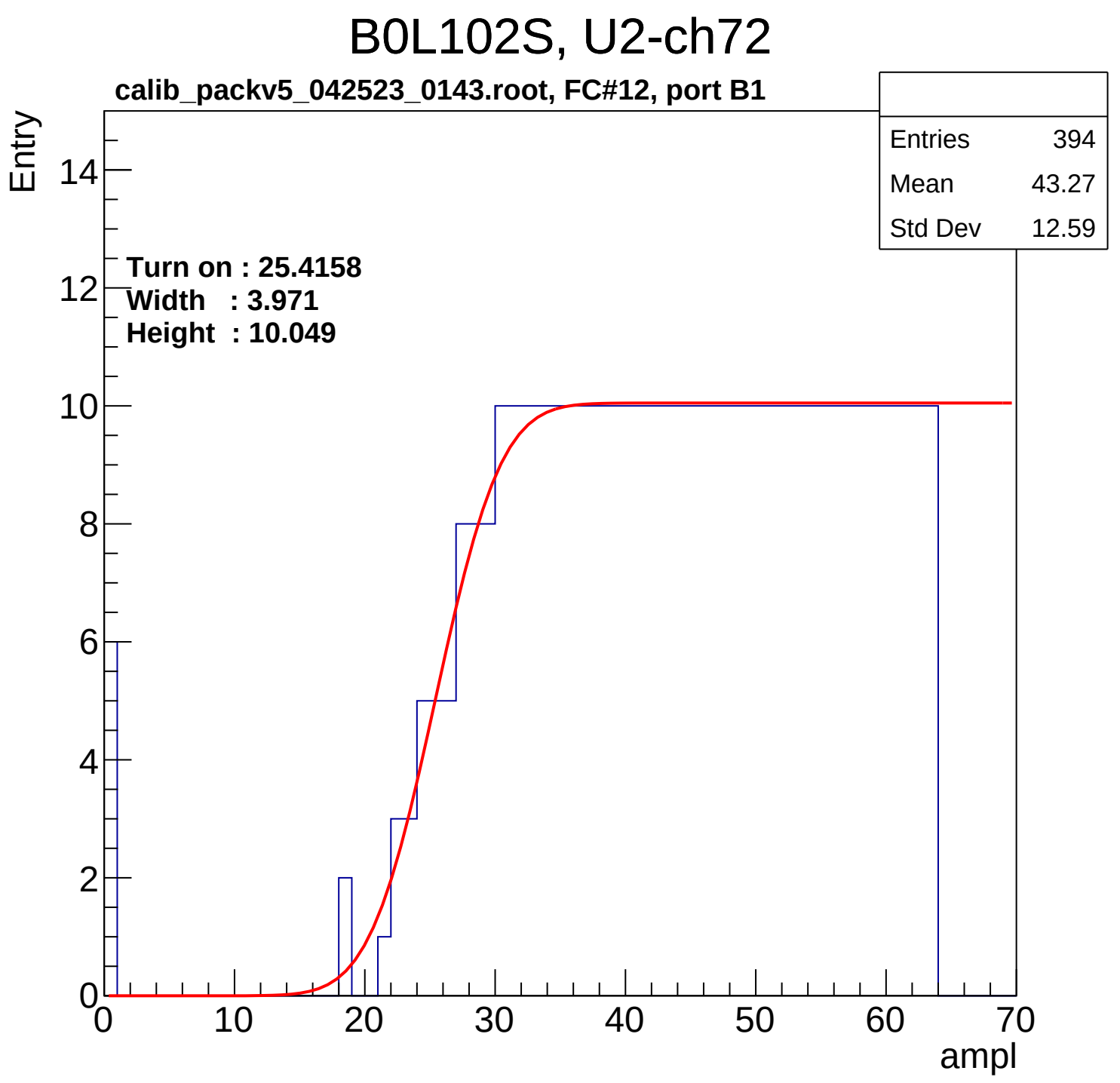
B0L102S, U2-ch72
calib_packv5_042523_0143.root, FC#12, port B1
Entries 394
Mean 43.27
Std Dev 12.59
Turn on : 25.4158
Width : 3.971
Height : 10.049
Entry
ampl
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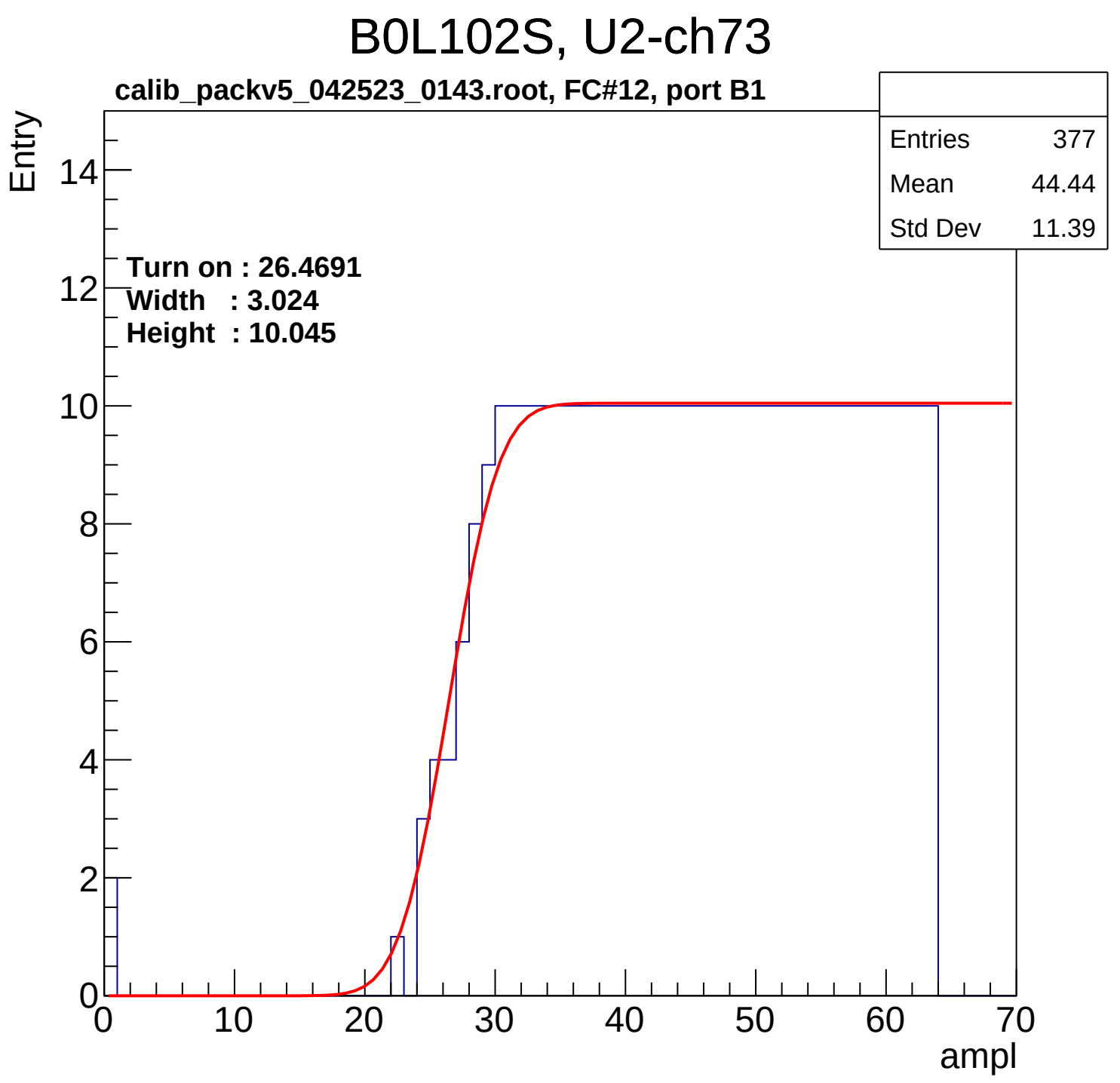
B0L102S, U2-ch73
calib_packv5_042523_0143.root, FC#12, port B1
Entries 377
Mean 44.44
Std Dev 11.39
Turn on : 26.4691
Width : 3.024
Height : 10.045
Entry
ampl
0
2
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6
8
10
12
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0
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60
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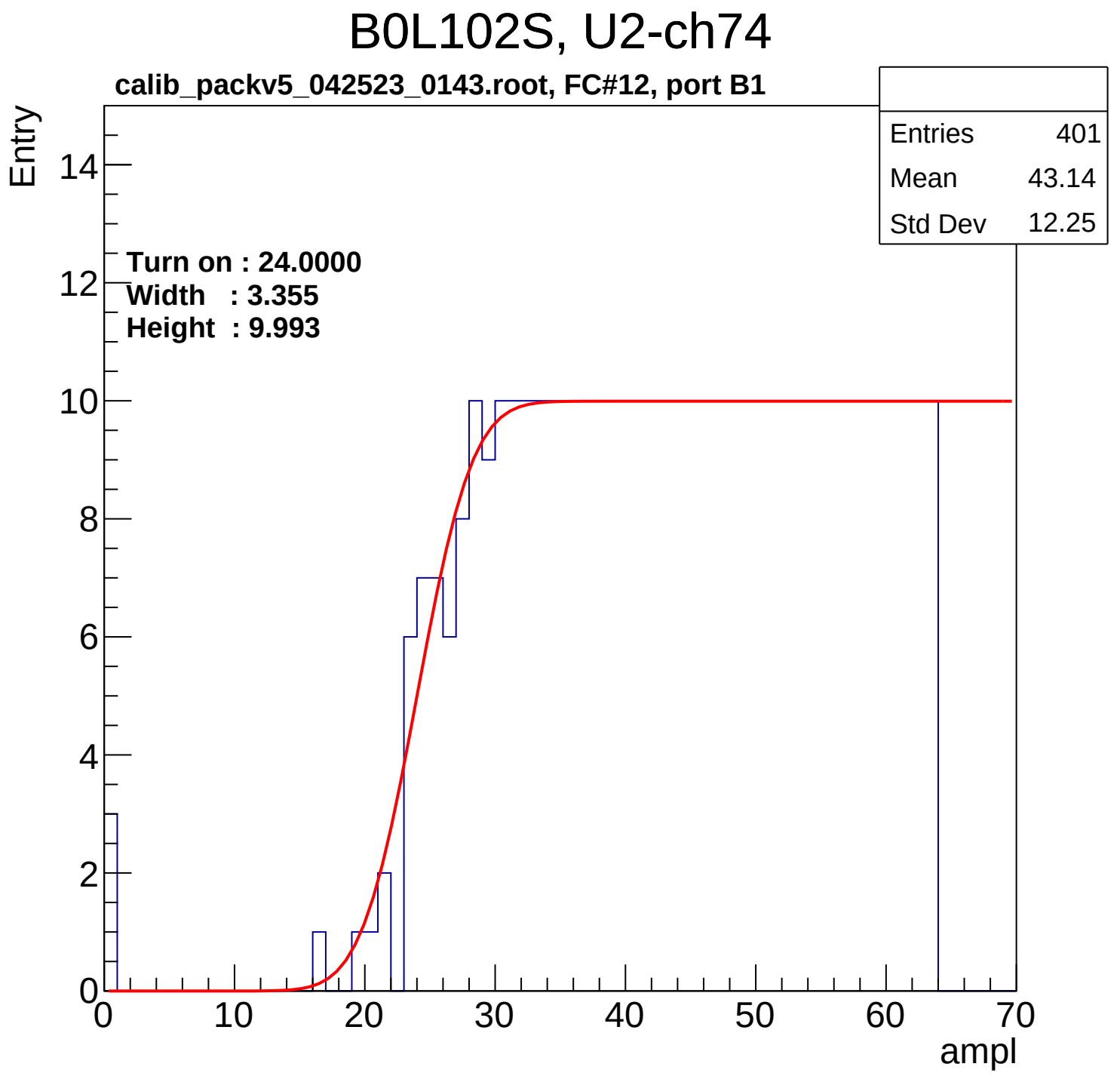
B0L102S, U2-ch74
calib_packv5_042523_0143.root, FC#12, port B1
Entries 401
Mean 43.14
Std Dev 12.25
Turn on : 24.0000
Width : 3.355
Height : 9.993
Entry
ampl
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4
6
8
10
12
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0
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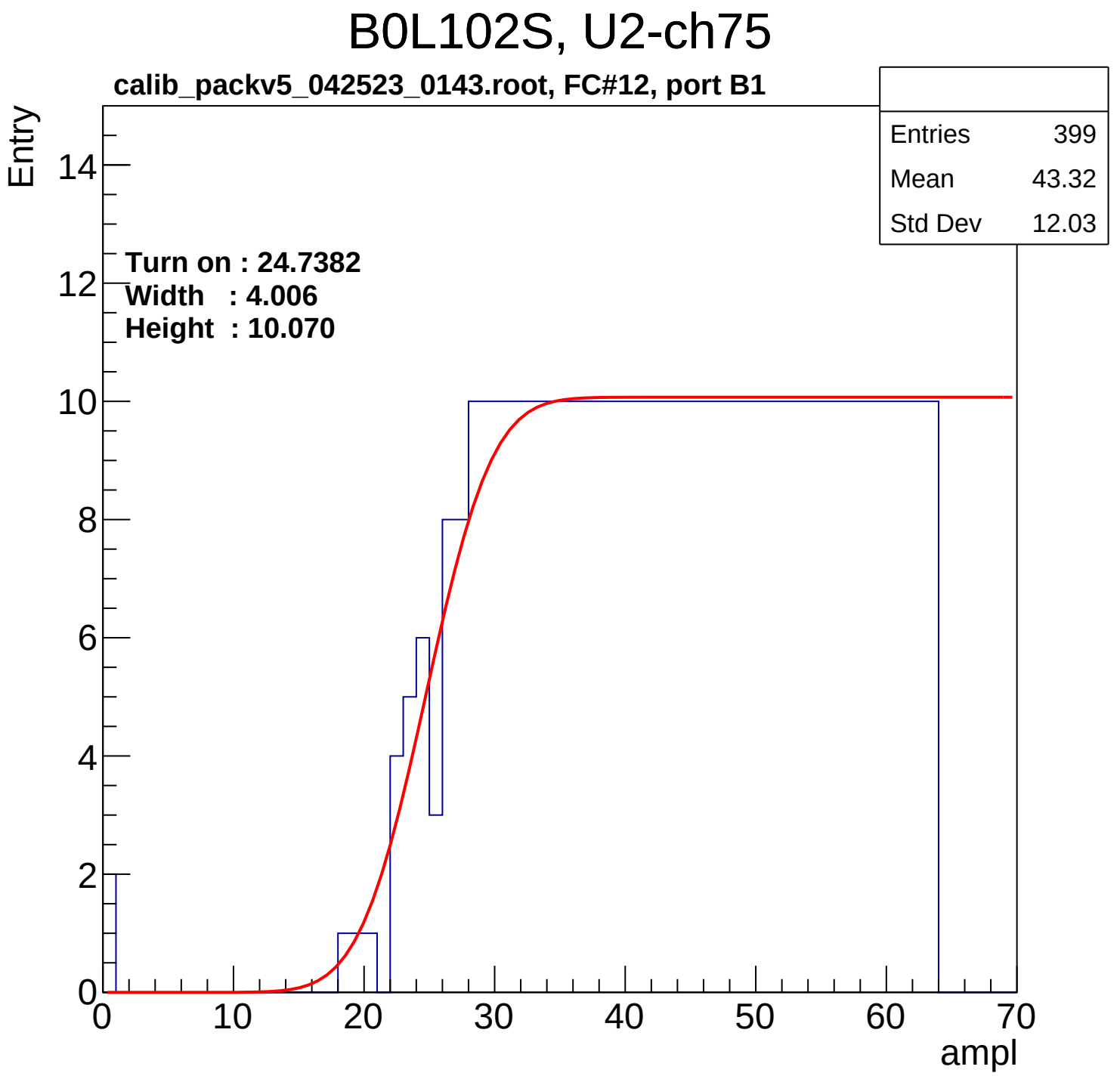
B0L102S, U2-ch75
calib_packv5_042523_0143.root, FC#12, port B1
Entries 399
Mean 43.32
Std Dev 12.03
Turn on : 24.7382
Width : 4.006
Height : 10.070
Entry
ampl
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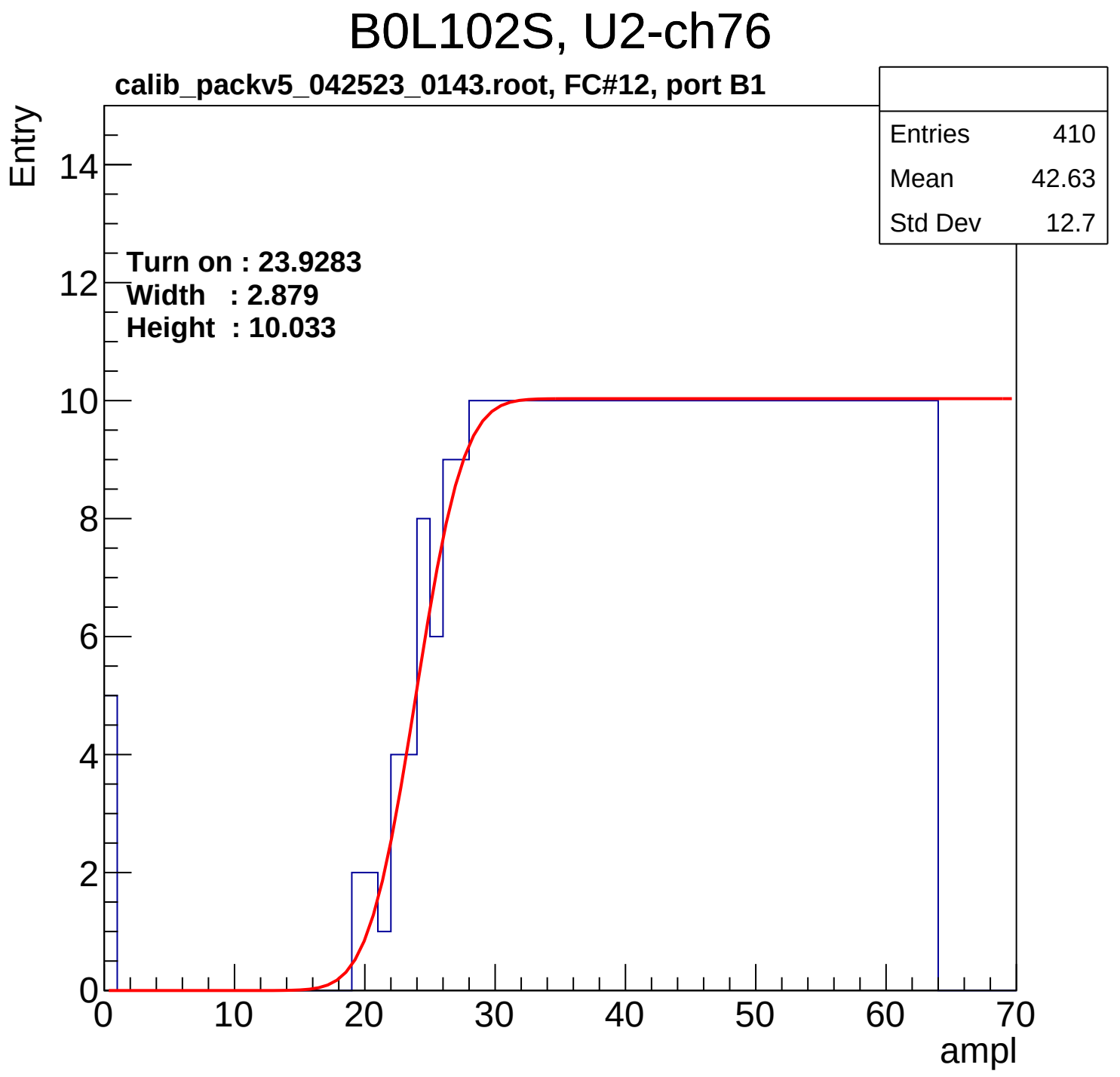
B0L102S, U2-ch76
calib_packv5_042523_0143.root, FC#12, port B1
Entries 410
Mean 42.63
Std Dev 12.7
Turn on : 23.9283
Width : 2.879
Height : 10.033
Entry
ampl
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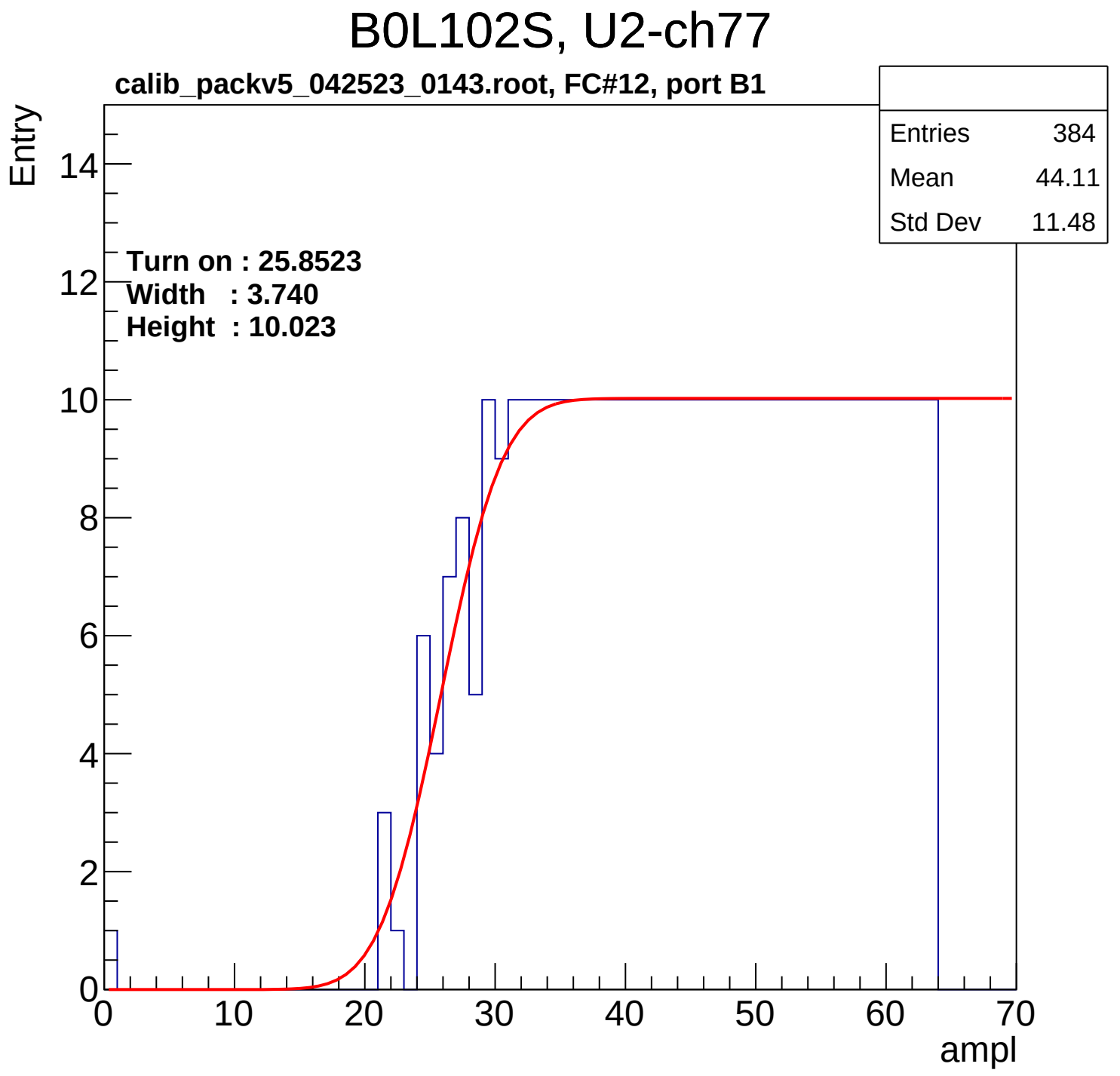
B0L102S, U2-ch77
calib_packv5_042523_0143.root, FC#12, port B1
Entries 384
Mean 44.11
Std Dev 11.48
Turn on : 25.8523
Width : 3.740
Height : 10.023
Entry
ampl
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8
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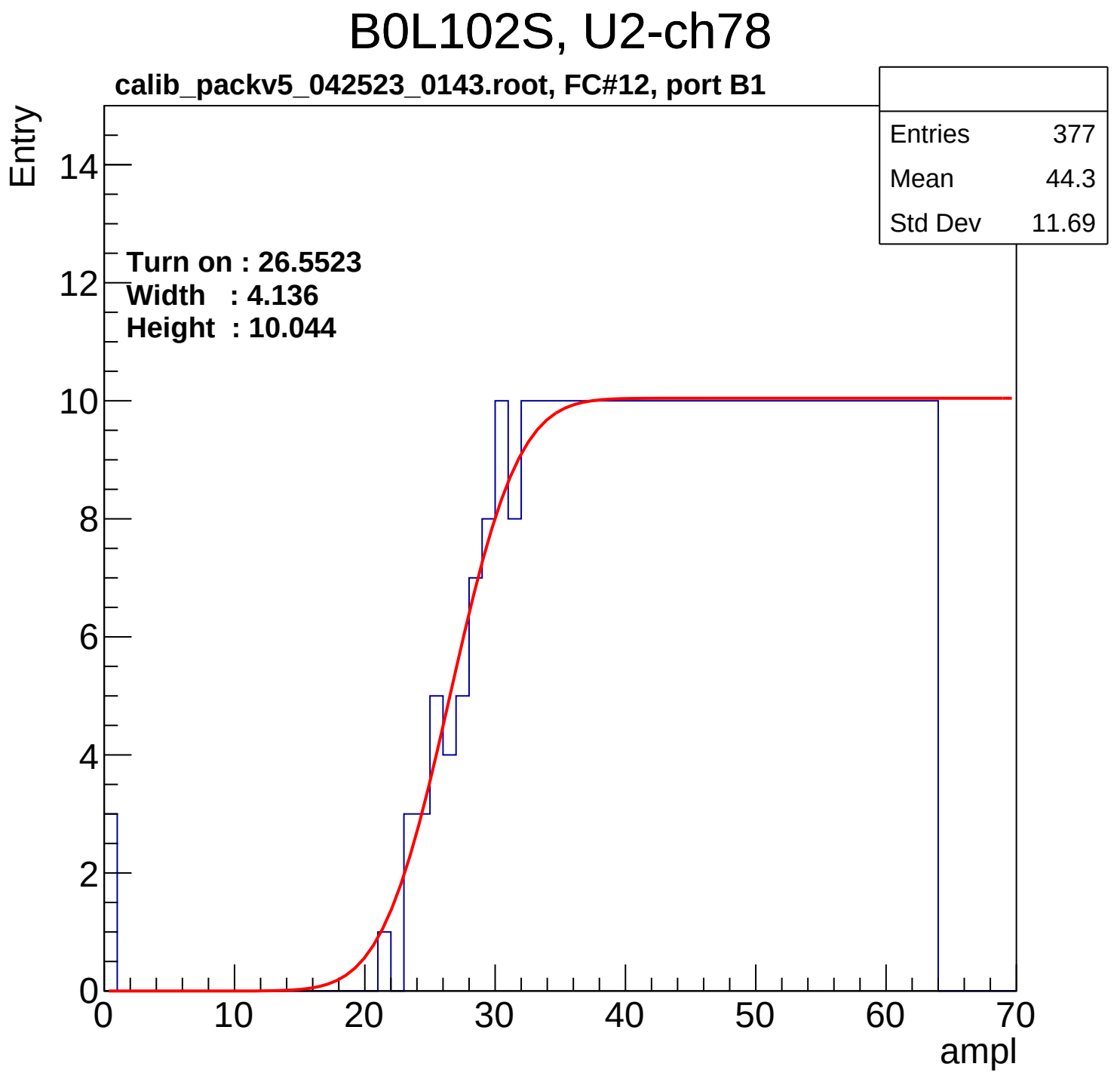
B0L102S, U2-ch78
calib_packv5_042523_0143.root, FC#12, port B1
Entries 377
Mean 44.3
Std Dev 11.69
Turn on : 26.5523
Width : 4.136
Height : 10.044
Entry
ampl
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4
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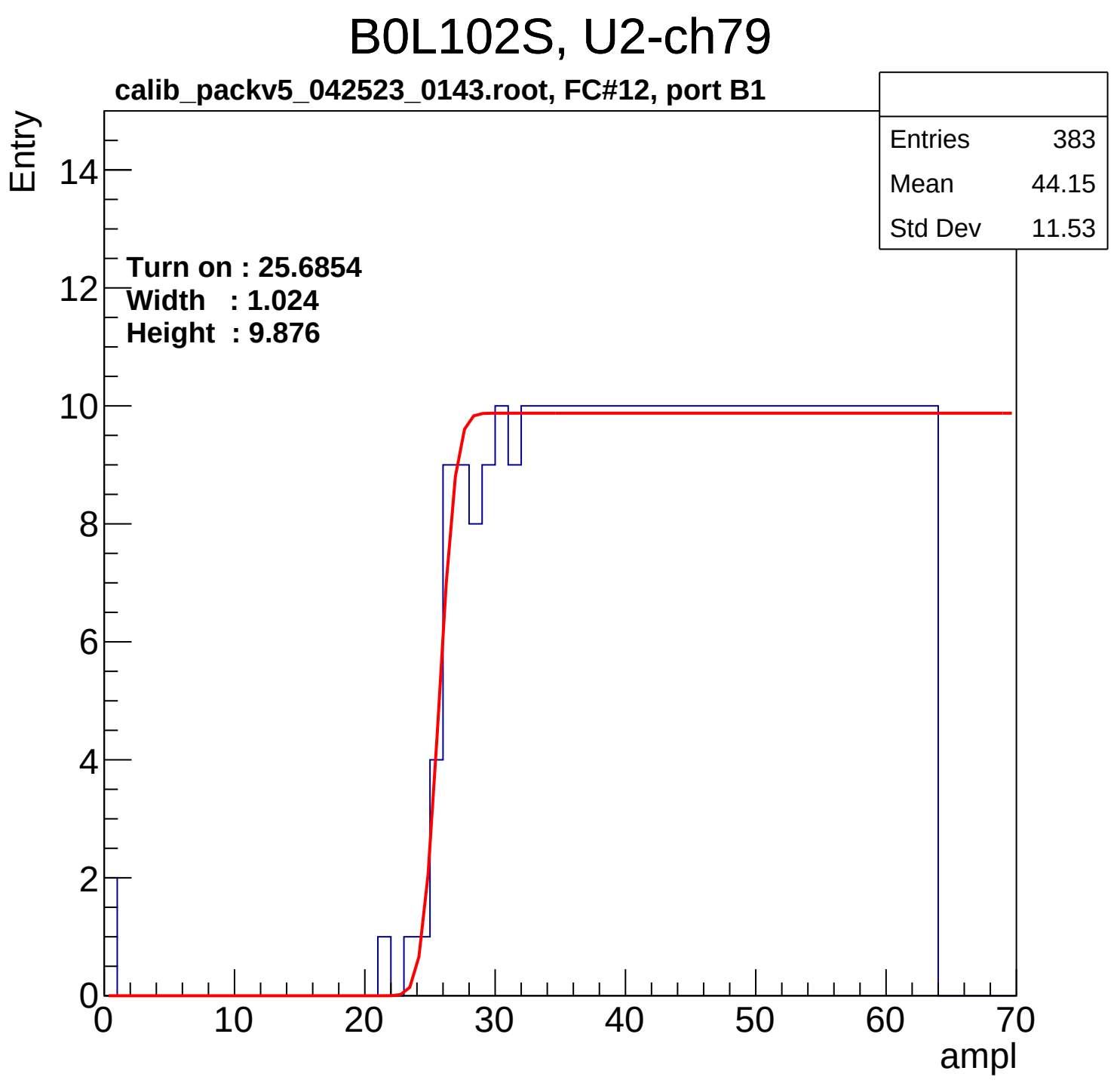
B0L102S, U2-ch79
calib_packv5_042523_0143.root, FC#12, port B1
Entries 383
Mean 44.15
Std Dev 11.53
Turn on : 25.6854
Width : 1.024
Height : 9.876
Entry
ampl
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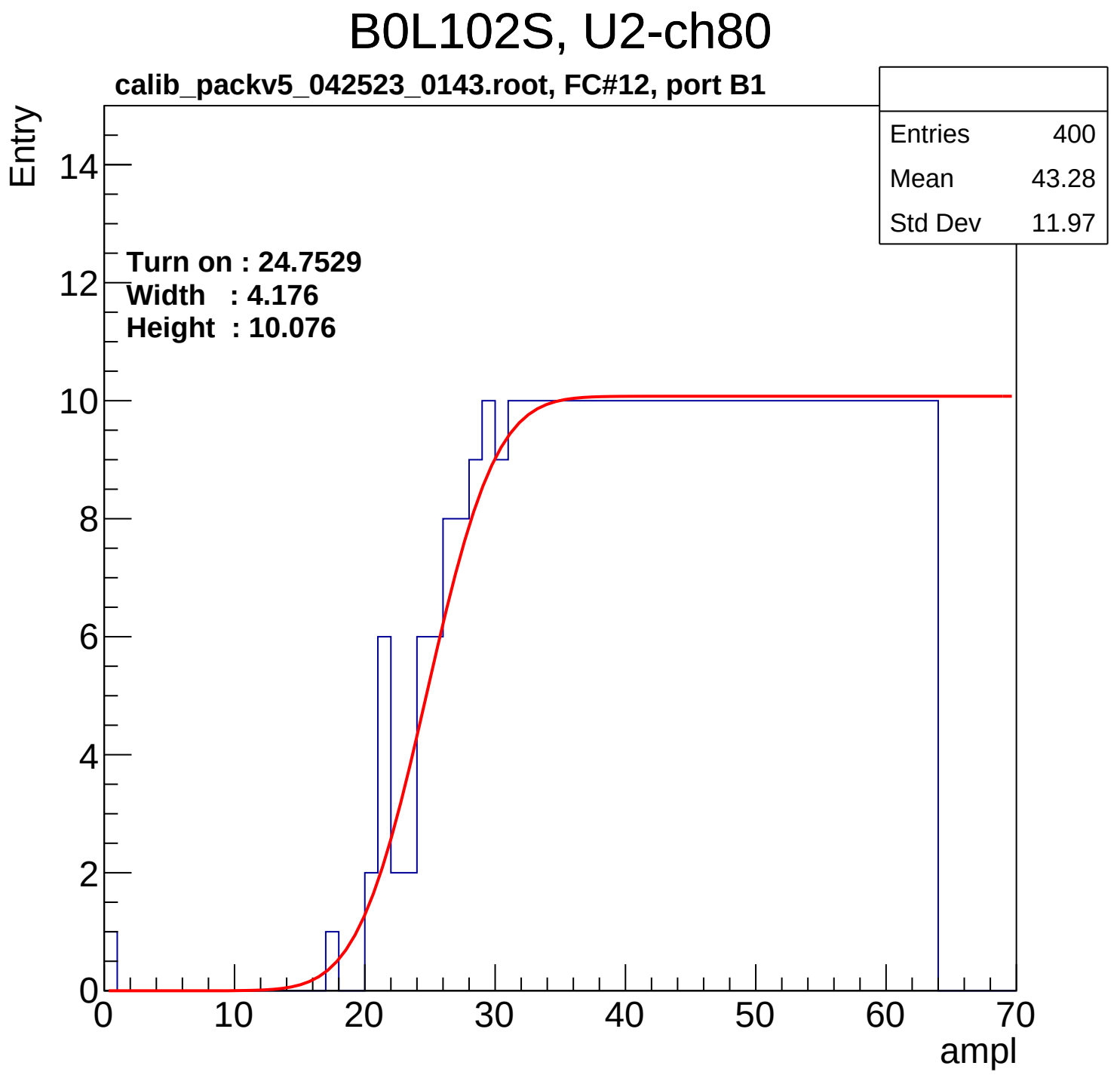
B0L102S, U2-ch80
calib_packv5_042523_0143.root, FC#12, port B1
Entries 400
Mean 43.28
Std Dev 11.97
Turn on : 24.7529
Width : 4.176
Height : 10.076
Entry
ampl
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8
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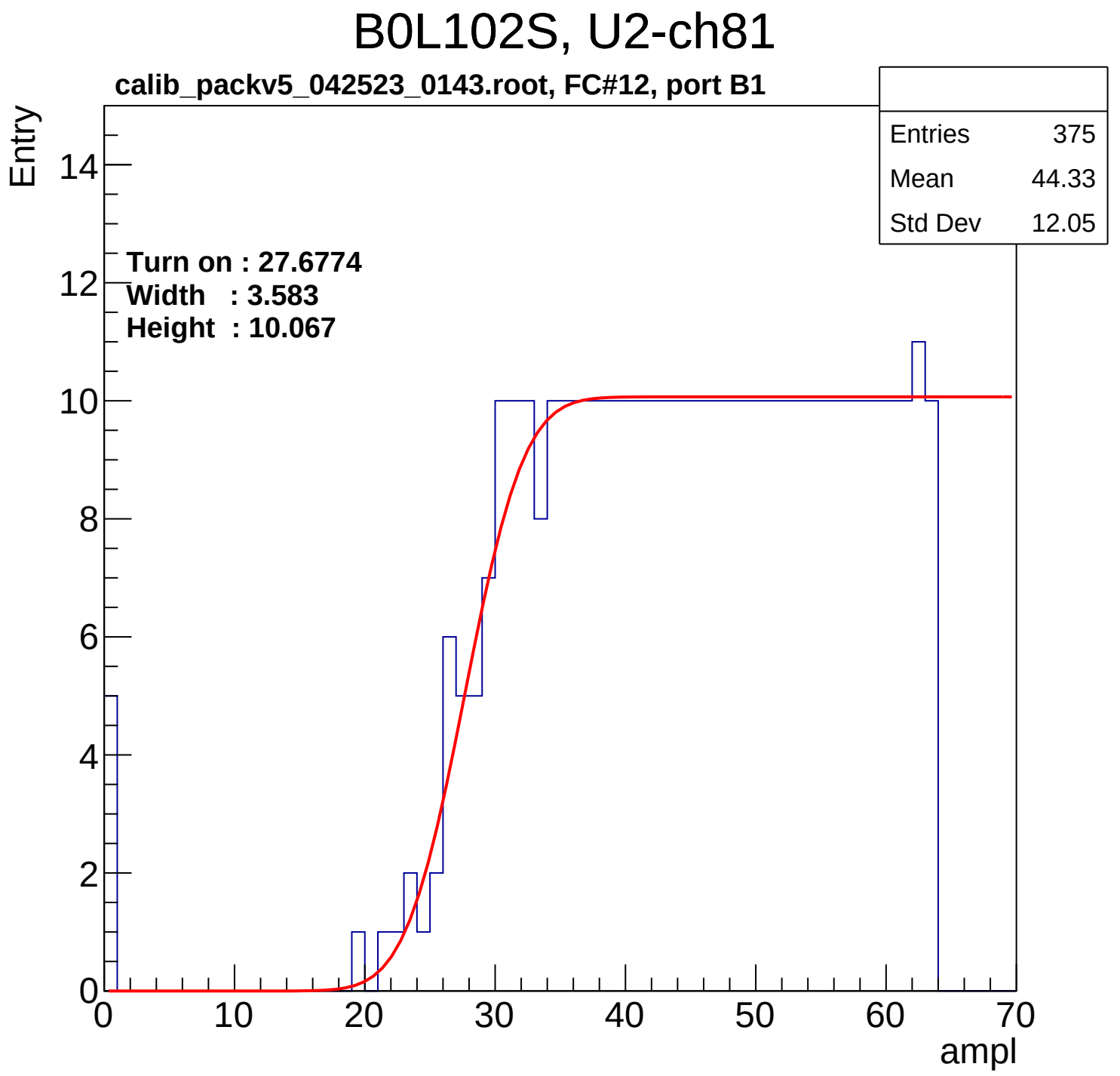
B0L102S, U2-ch81
calib_packv5_042523_0143.root, FC#12, port B1
Entries 375
Mean 44.33
Std Dev 12.05
Turn on : 27.6774
Width : 3.583
Height : 10.067
Entry
ampl
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2
4
6
8
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0
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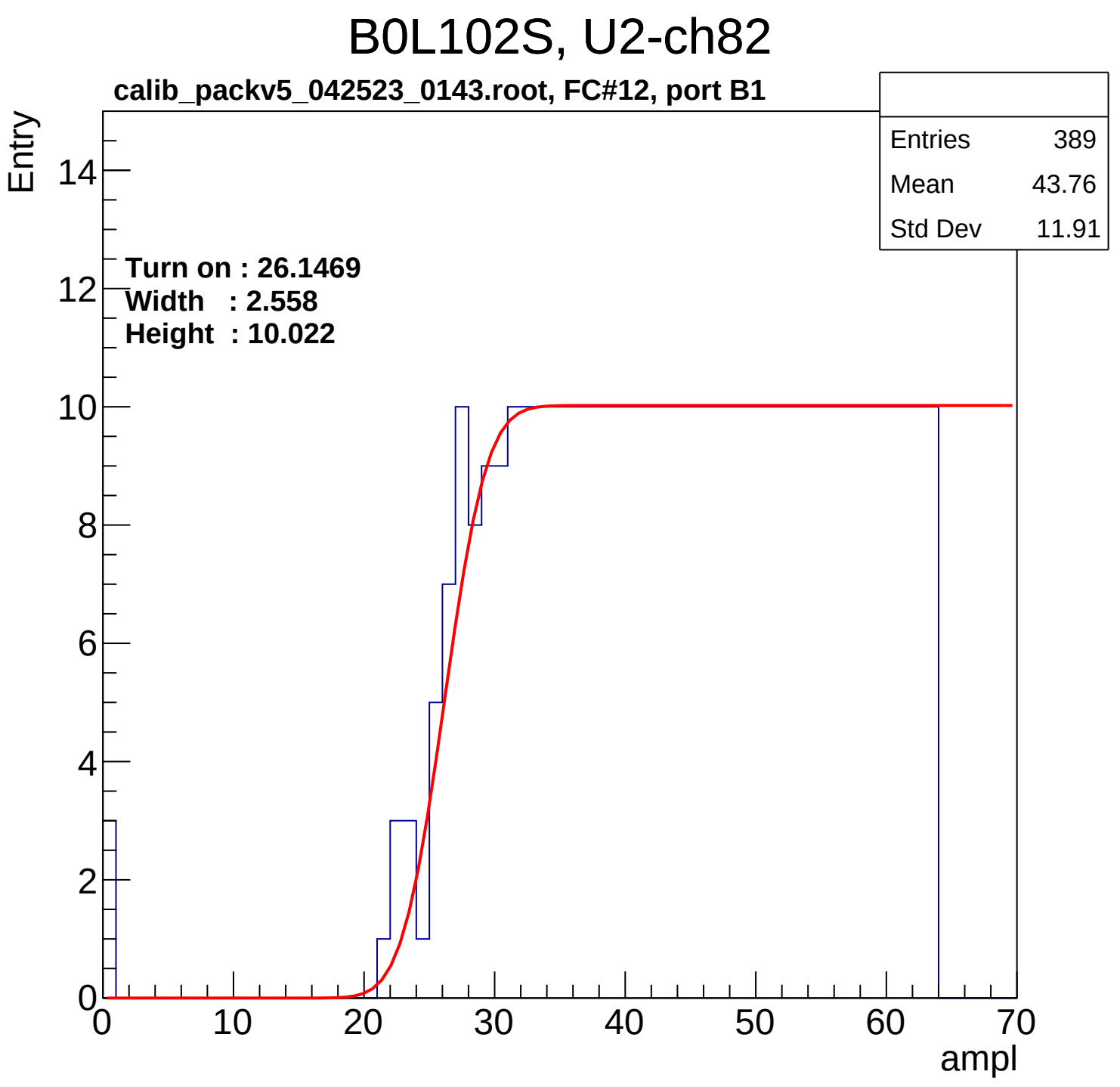
B0L102S, U2-ch82
calib_packv5_042523_0143.root, FC#12, port B1
Entries 389
Mean 43.76
Std Dev 11.91
Turn on : 26.1469
Width : 2.558
Height : 10.022
Entry
ampl
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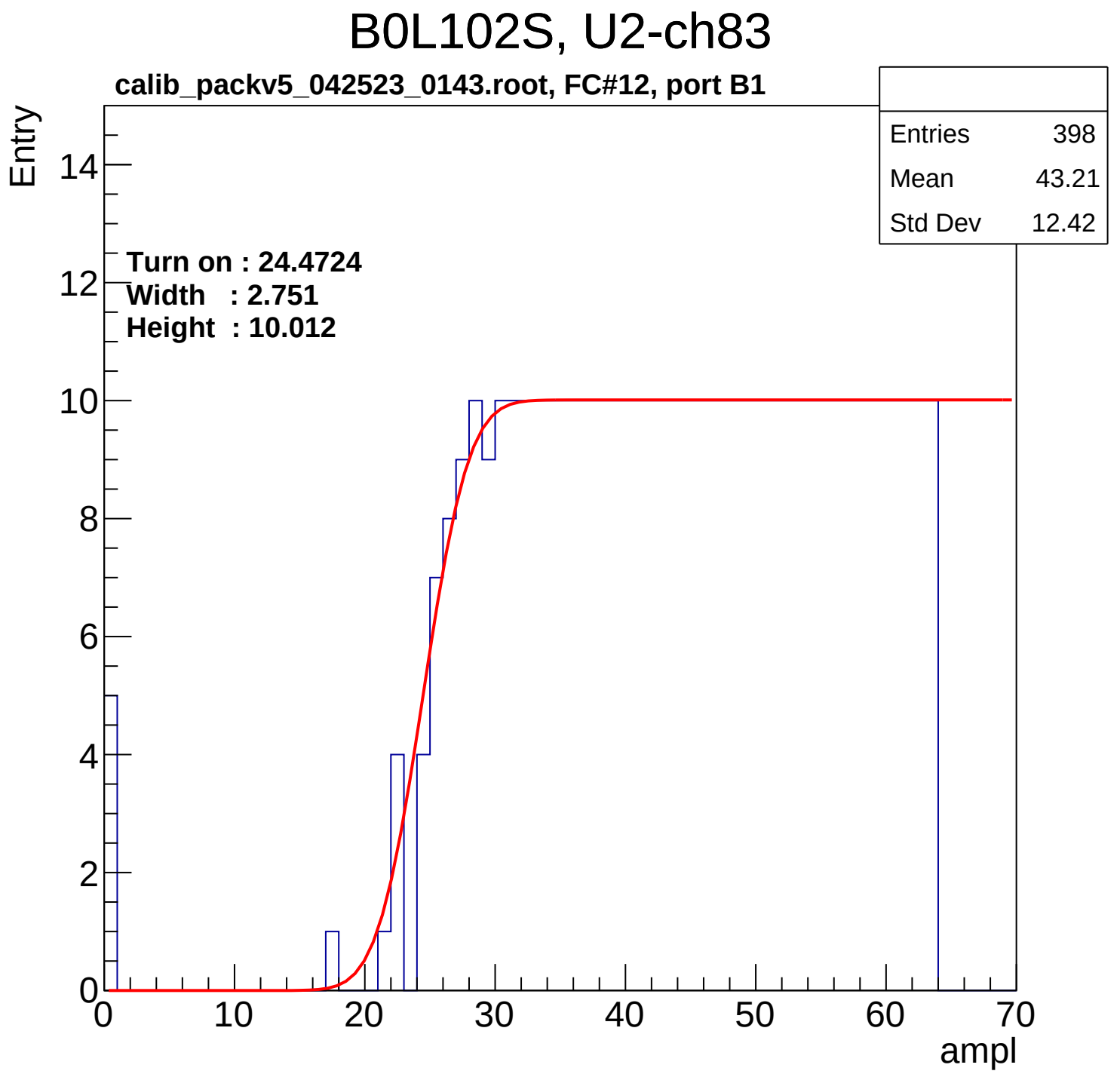
B0L102S, U2-ch83
calib_packv5_042523_0143.root, FC#12, port B1
Entries 398
Mean 43.21
Std Dev 12.42
Turn on : 24.4724
Width : 2.751
Height : 10.012
Entry
ampl
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4
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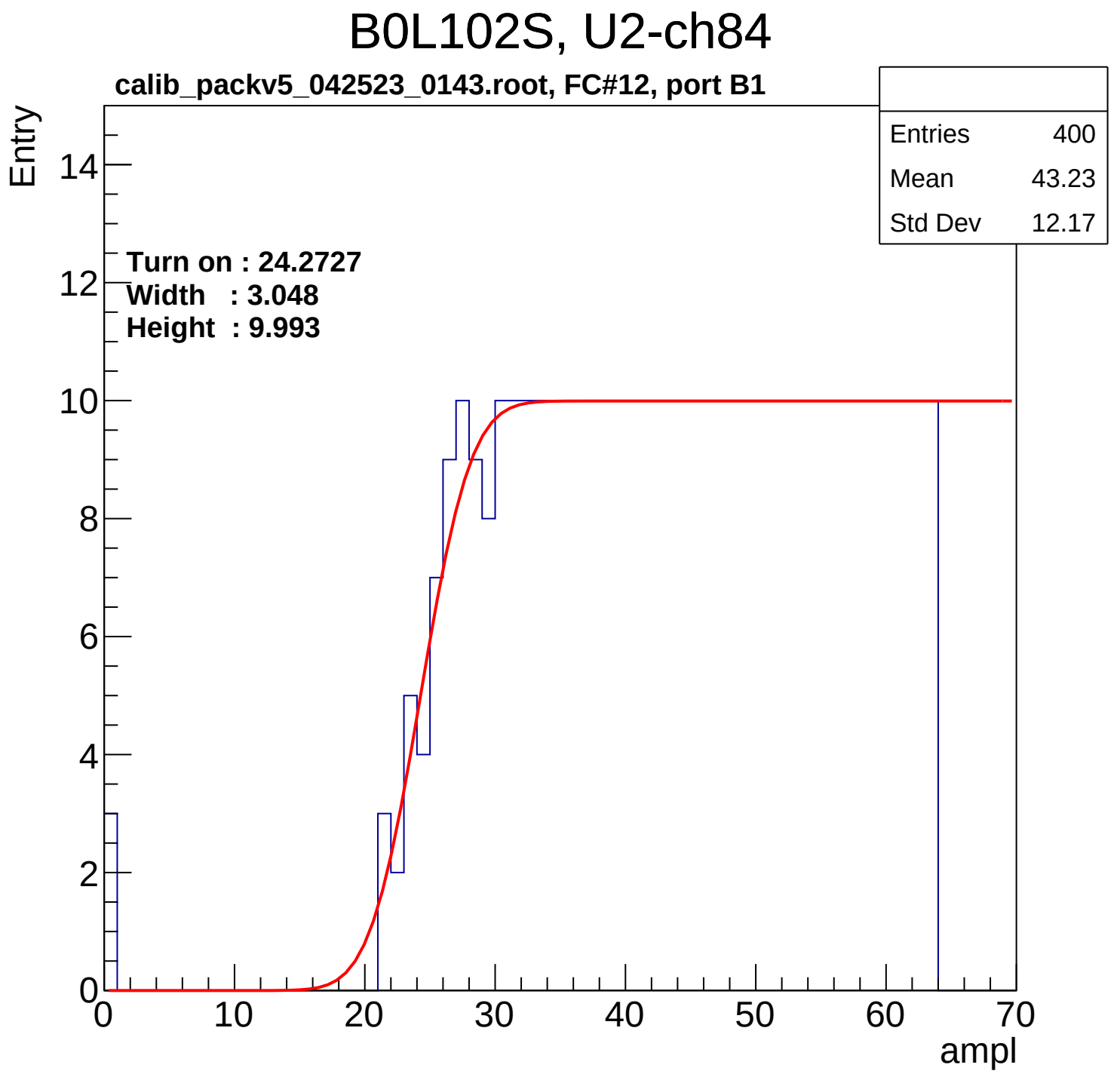
B0L102S, U2-ch84
calib_packv5_042523_0143.root, FC#12, port B1
Entries 400
Mean 43.23
Std Dev 12.17
Turn on : 24.2727
Width : 3.048
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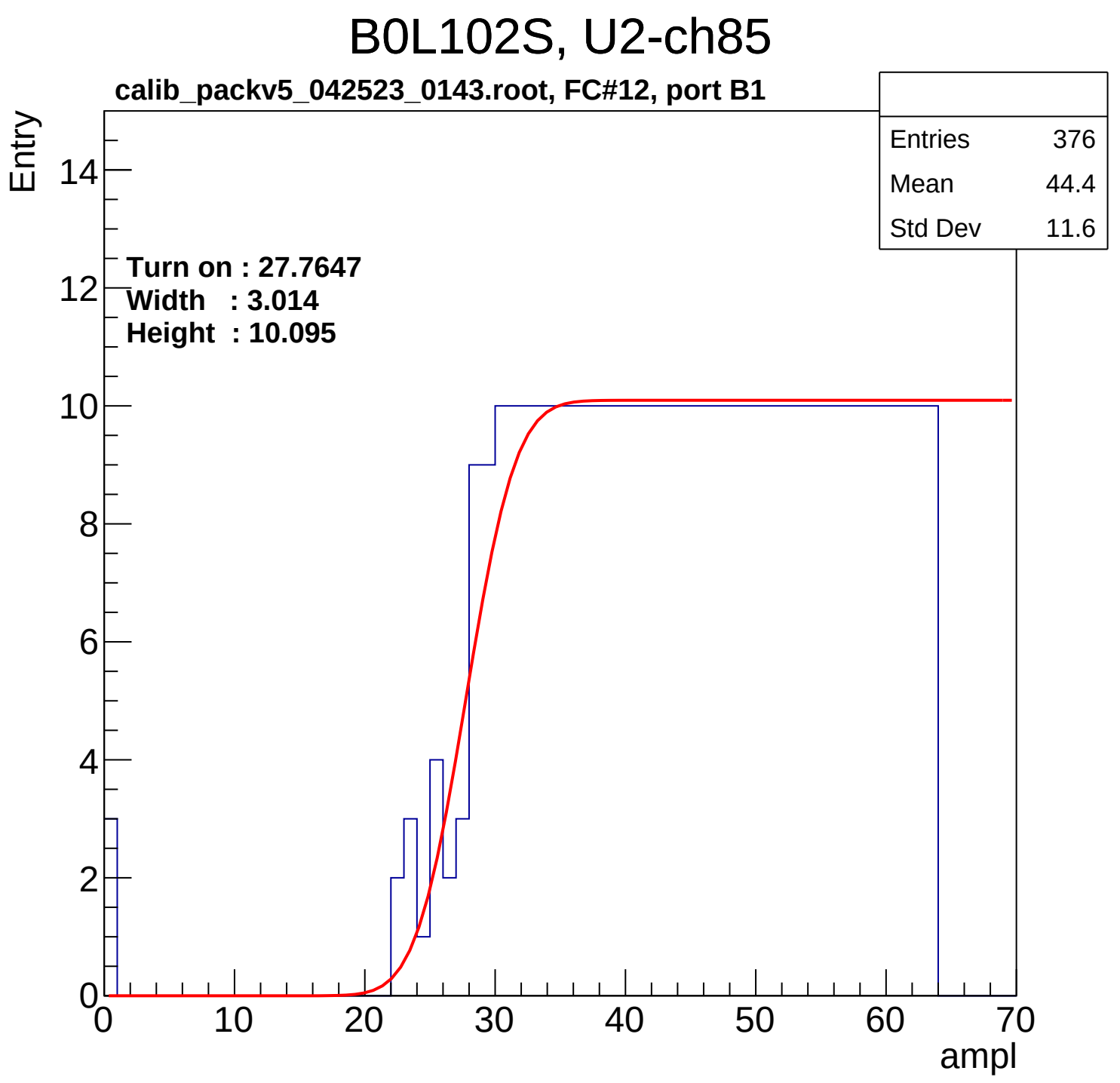
B0L102S, U2-ch85
calib_packv5_042523_0143.root, FC#12, port B1
Entries 376
Mean 44.4
Std Dev 11.6
Turn on : 27.7647
Width : 3.014
Height : 10.095
Entry
ampl
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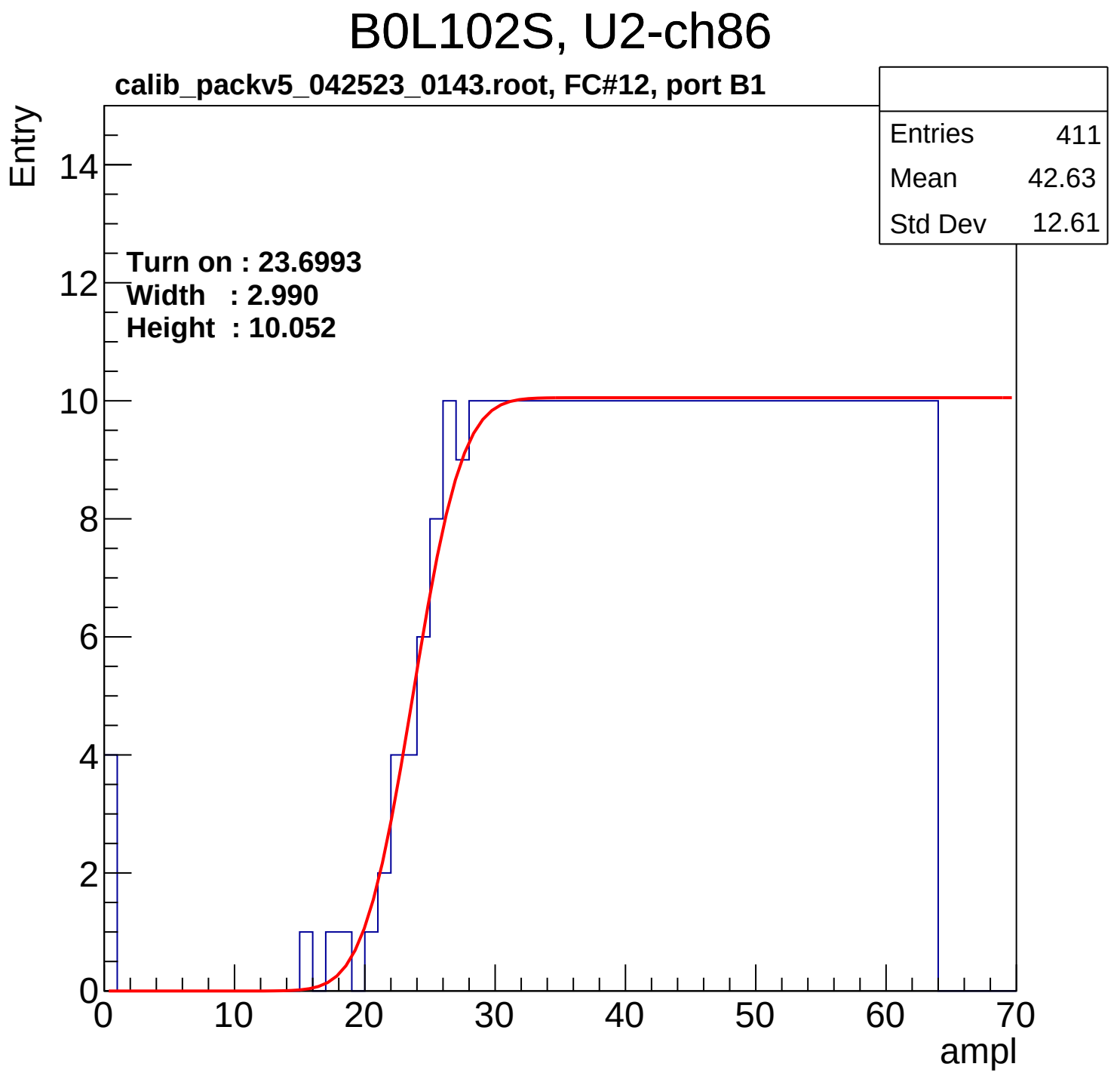
B0L102S, U2-ch86
calib_packv5_042523_0143.root, FC#12, port B1
Entries 411
Mean 42.63
Std Dev 12.61
Turn on : 23.6993
Width : 2.990
Height : 10.052
Entry
ampl
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4
6
8
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12
14
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20
30
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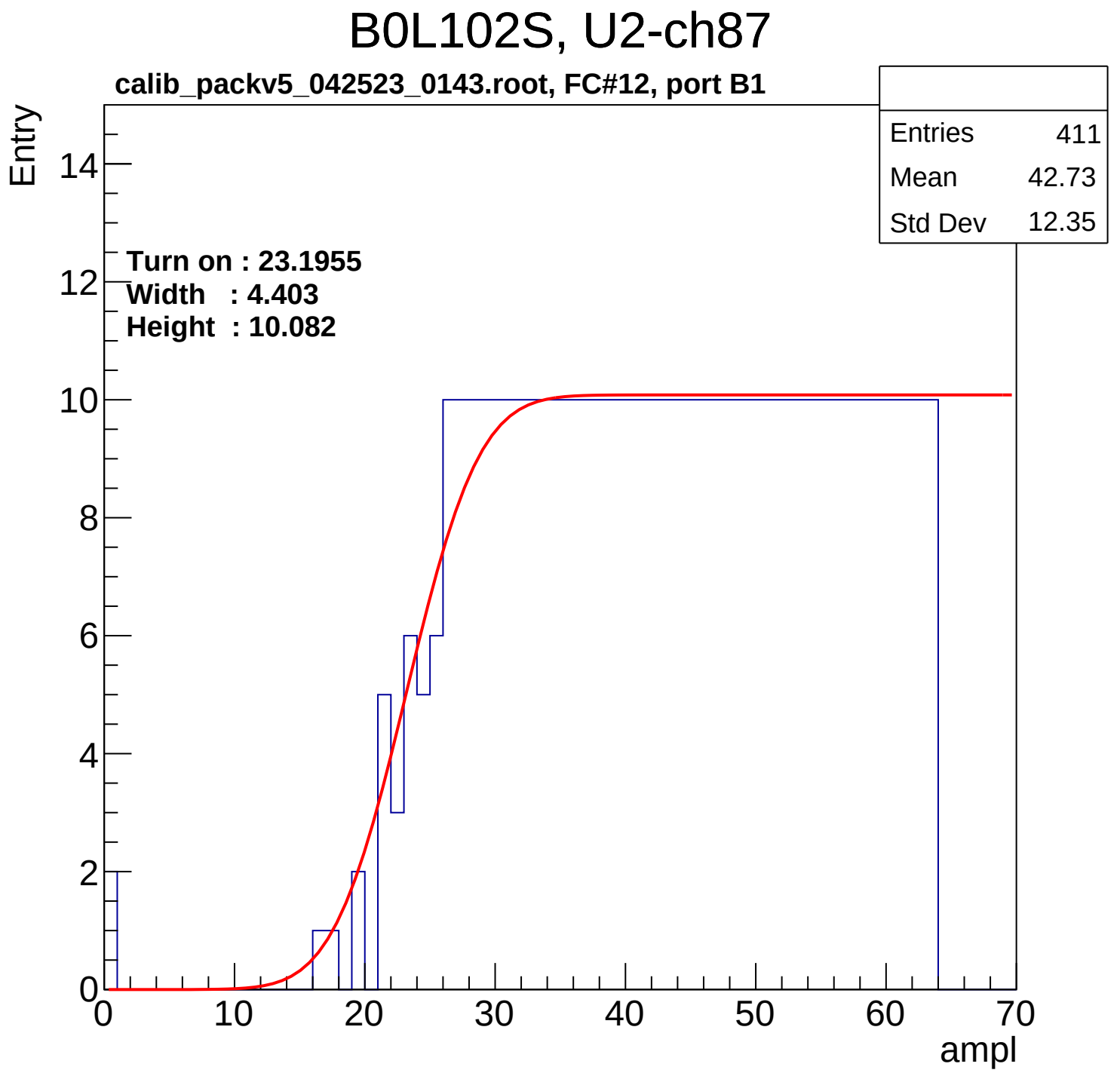
B0L102S, U2-ch87
calib_packv5_042523_0143.root, FC#12, port B1
Entries 411
Mean 42.73
Std Dev 12.35
Turn on : 23.1955
Width : 4.403
Height : 10.082
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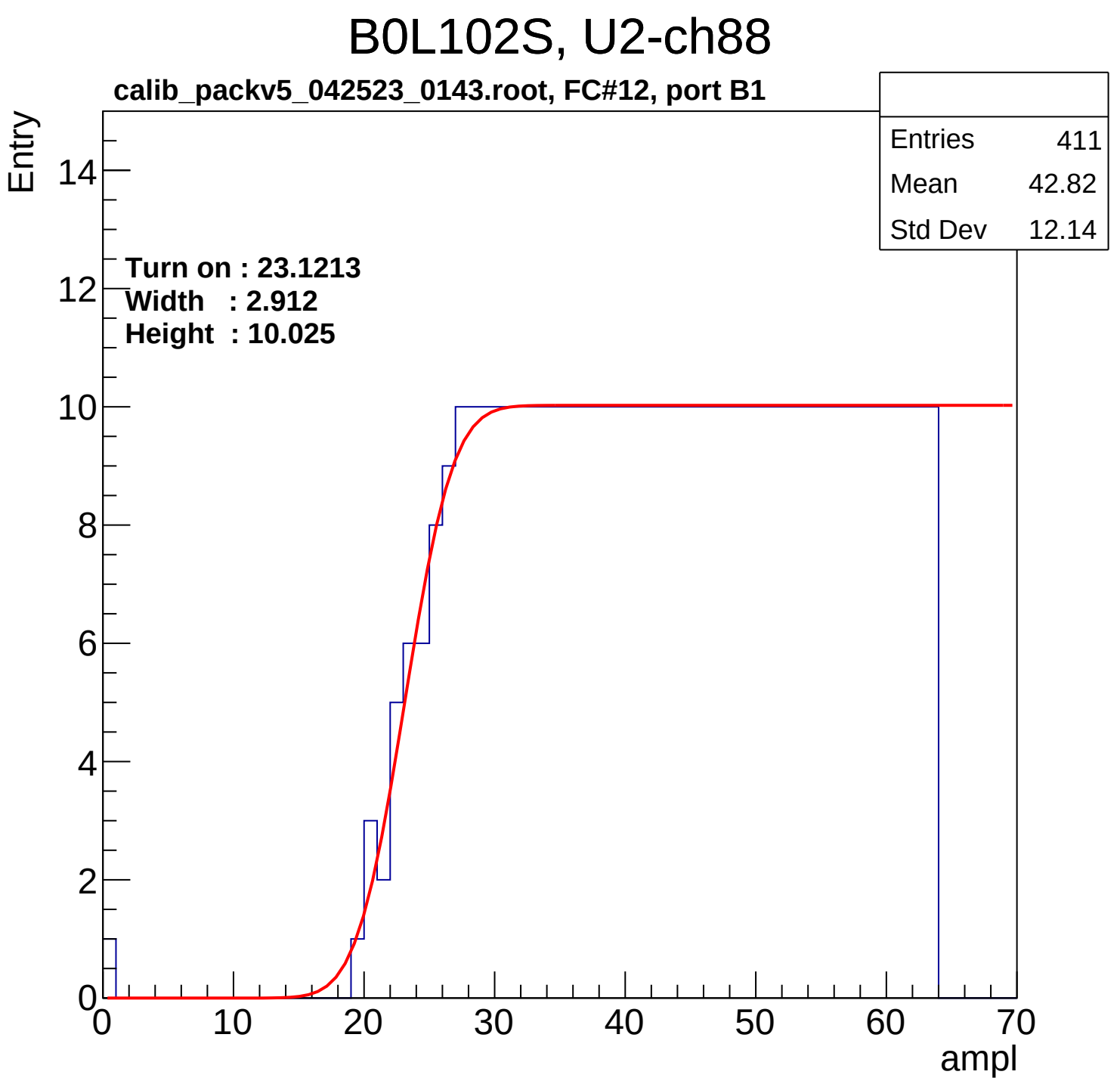
B0L102S, U2-ch88
calib_packv5_042523_0143.root, FC#12, port B1
Entries 411
Mean 42.82
Std Dev 12.14
Turn on : 23.1213
Width : 2.912
Height : 10.025
Entry
ampl
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4
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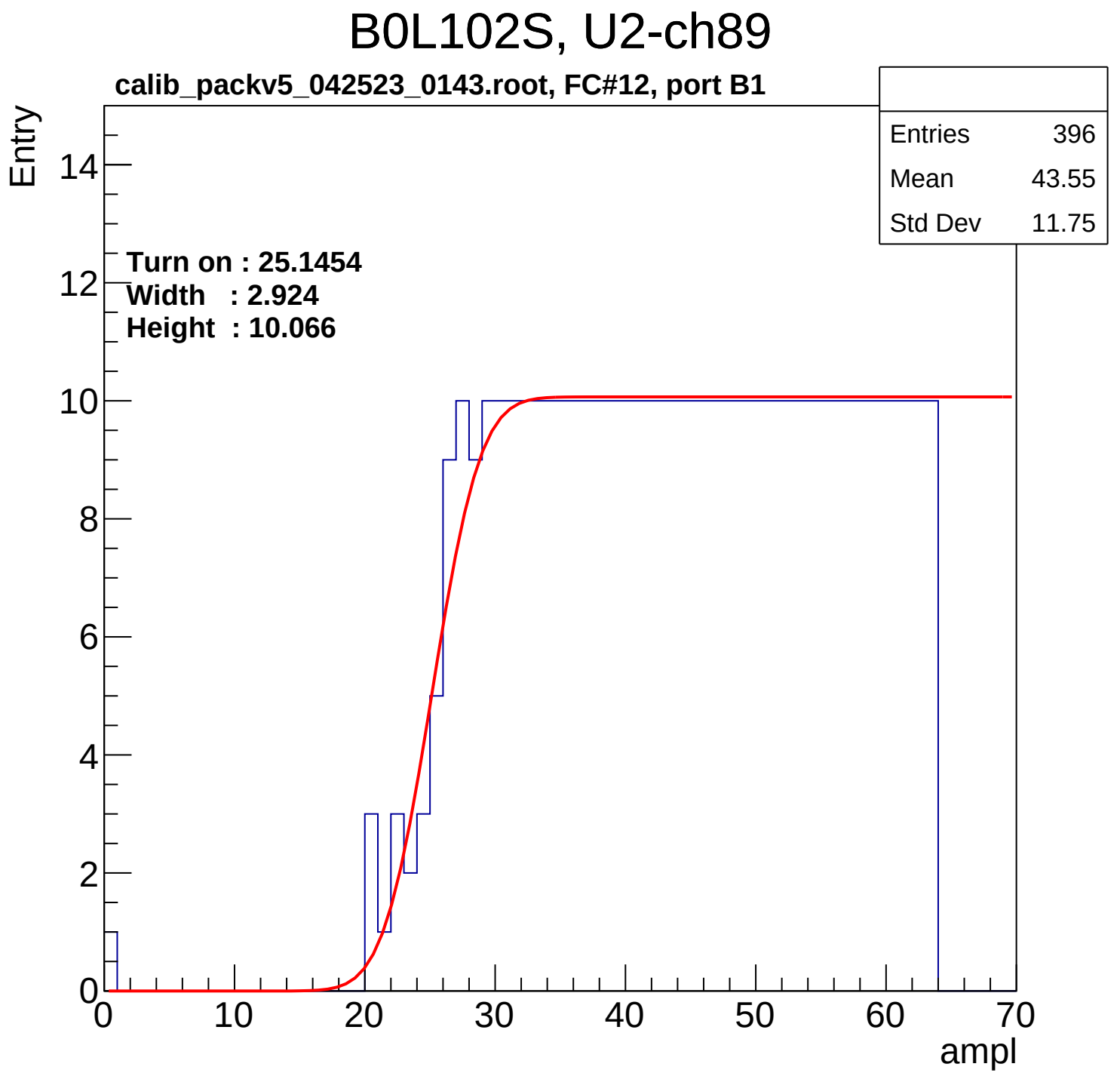
B0L102S, U2-ch89
calib_packv5_042523_0143.root, FC#12, port B1
Entries 396
Mean 43.55
Std Dev 11.75
Turn on : 25.1454
Width : 2.924
Height : 10.066
Entry
ampl
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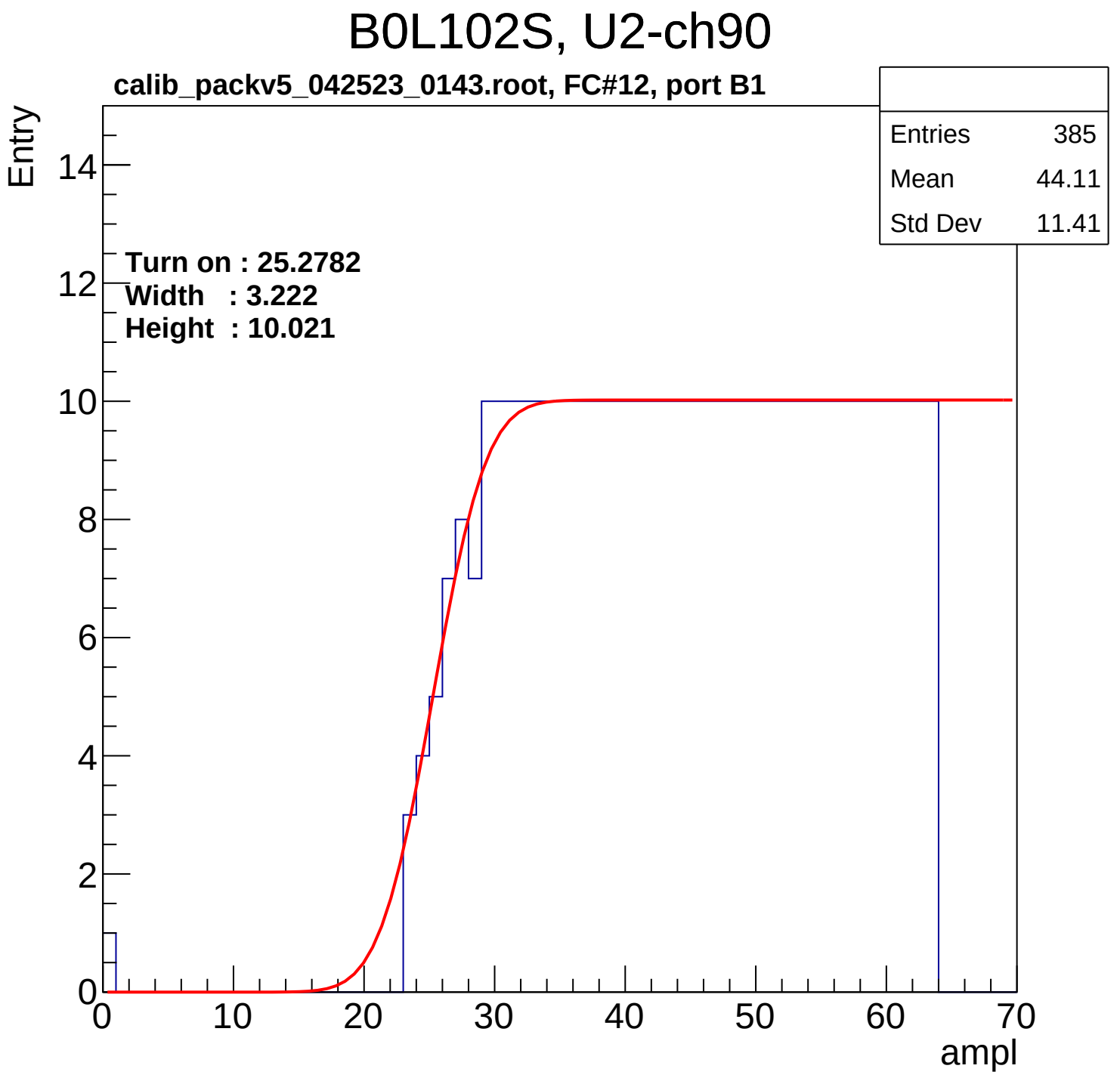
B0L102S, U2-ch90
calib_packv5_042523_0143.root, FC#12, port B1
Entries 385
Mean 44.11
Std Dev 11.41
Turn on : 25.2782
Width : 3.222
Height : 10.021
Entry
ampl
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2
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6
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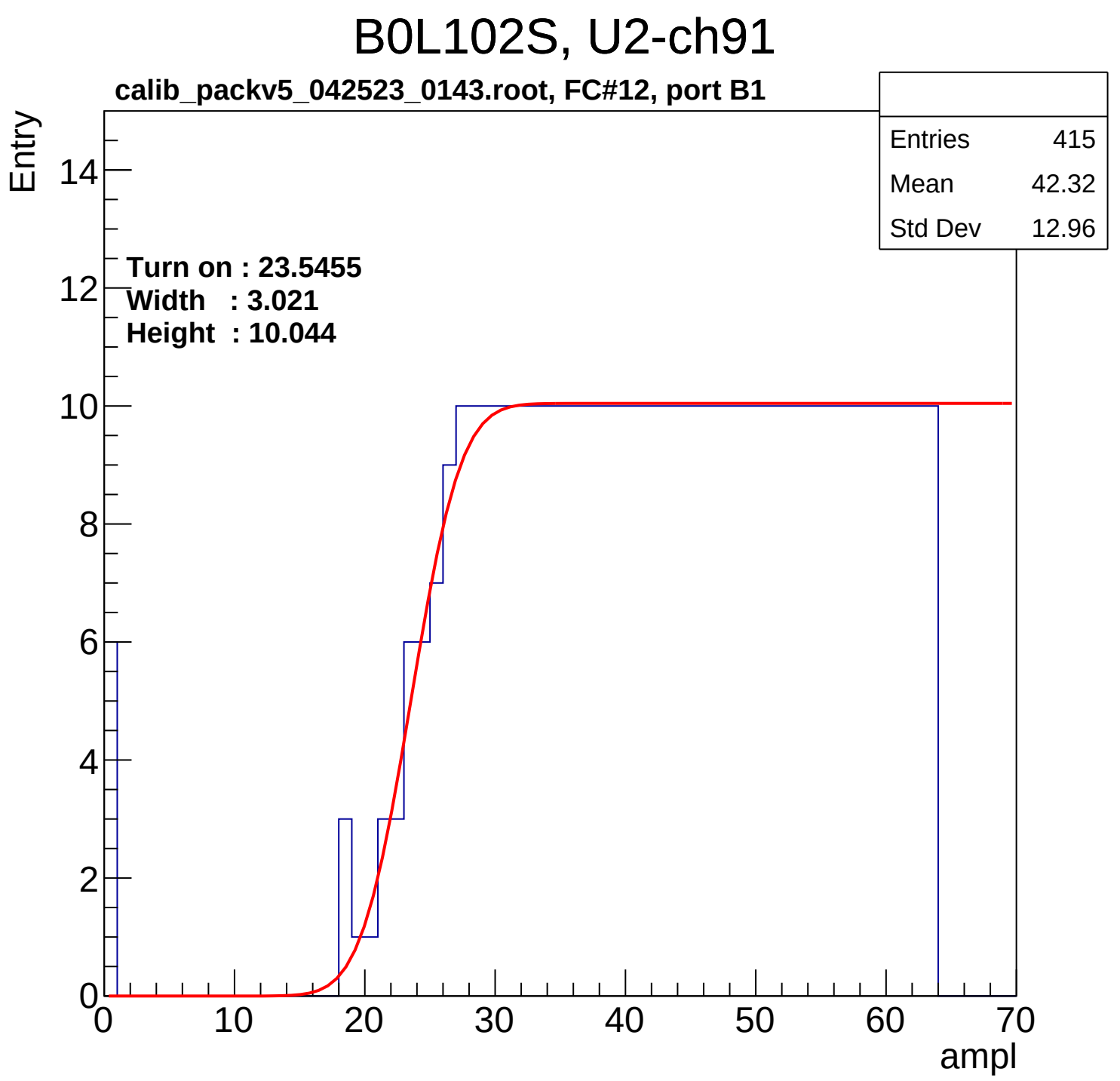
B0L102S, U2-ch91
calib_packv5_042523_0143.root, FC#12, port B1
Entries 415
Mean 42.32
Std Dev 12.96
Turn on : 23.5455
Width : 3.021
Height : 10.044
Entry
ampl
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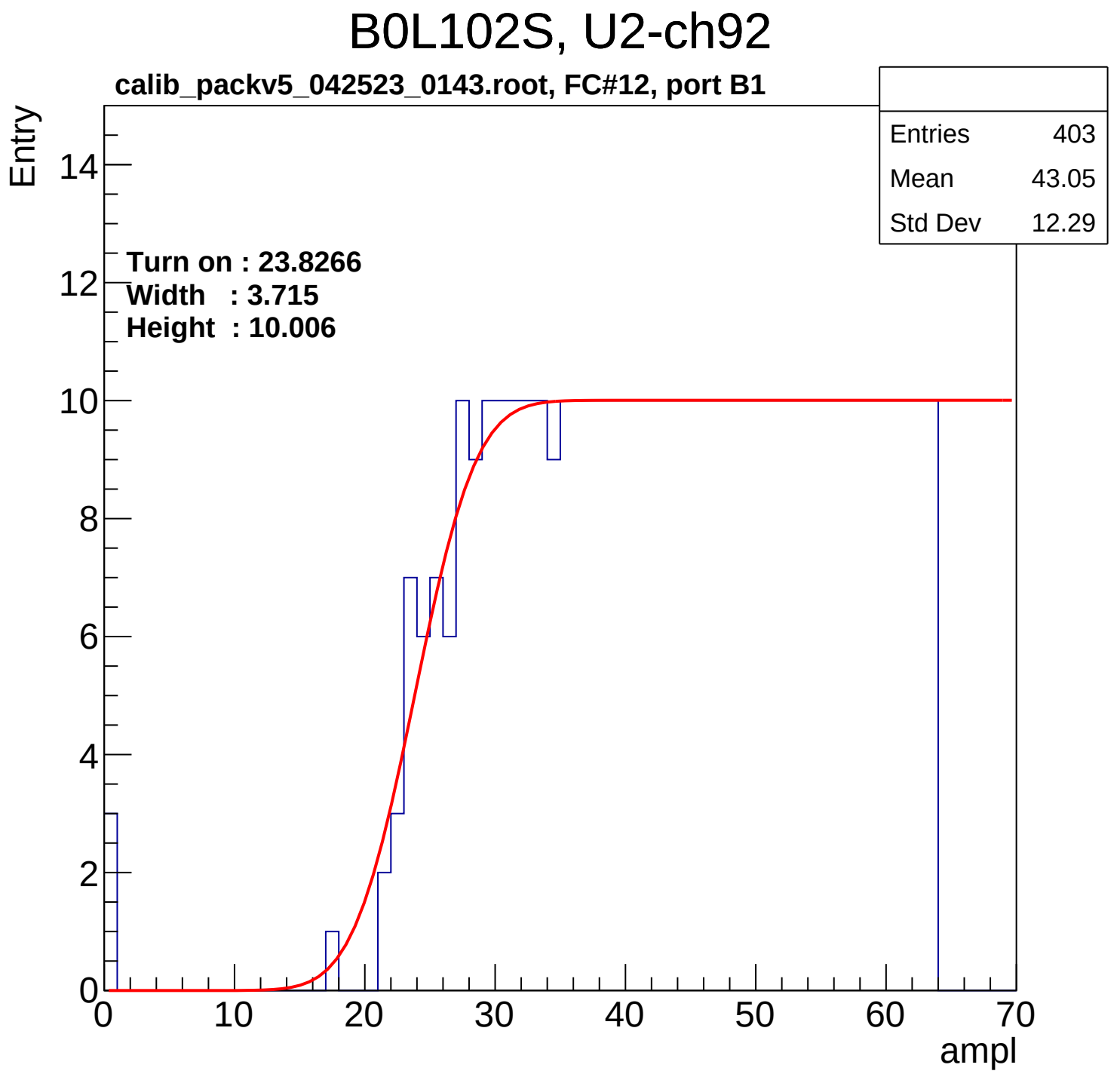
B0L102S, U2-ch92
calib_packv5_042523_0143.root, FC#12, port B1
Entries 403
Mean 43.05
Std Dev 12.29
Turn on : 23.8266
Width : 3.715
Height : 10.006
Entry
ampl
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6
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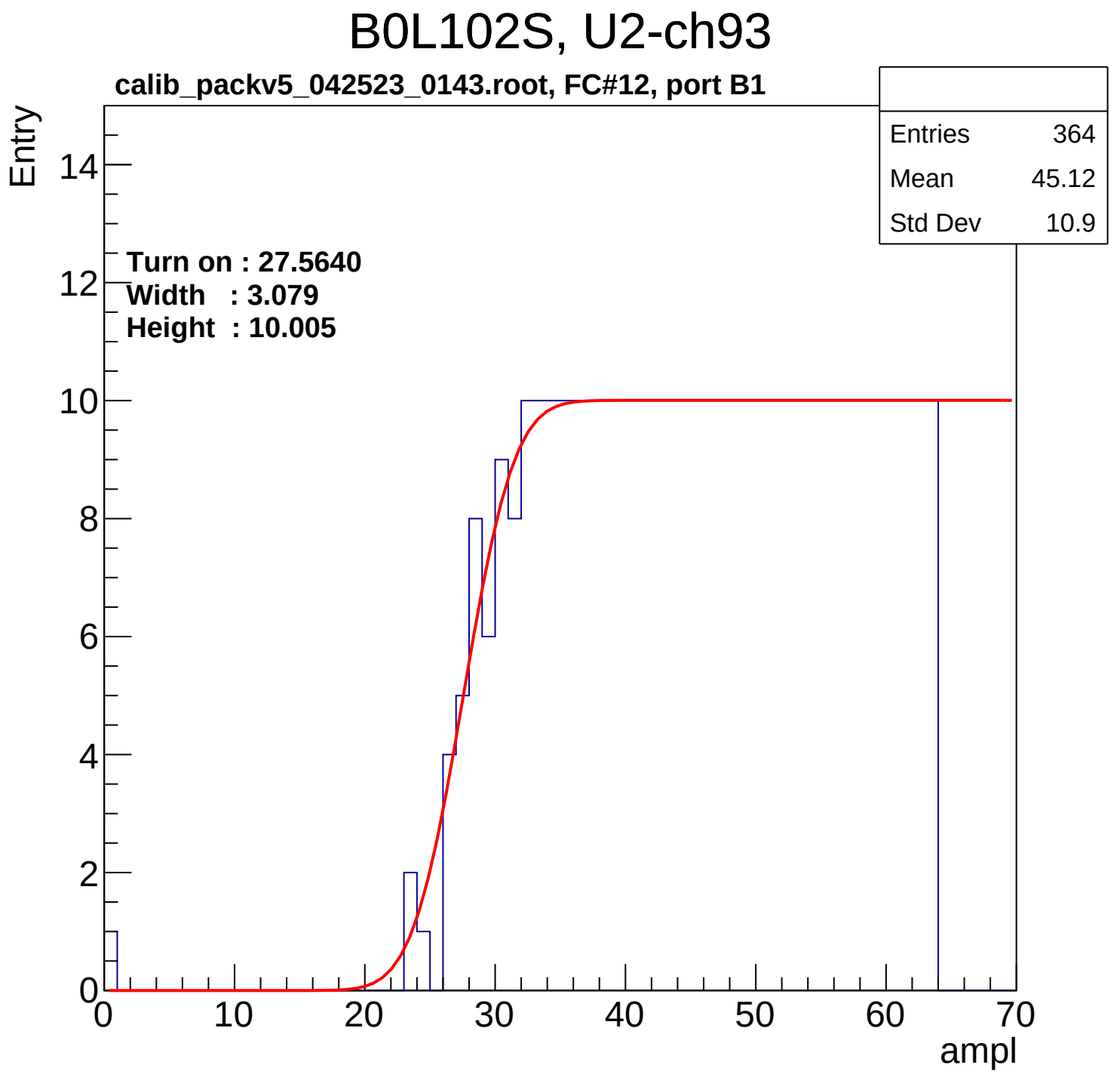
B0L102S, U2-ch93
calib_packv5_042523_0143.root, FC#12, port B1
Entries 364
Mean 45.12
Std Dev 10.9
Turn on : 27.5640
Width : 3.079
Height : 10.005
Entry
ampl
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2
4
6
8
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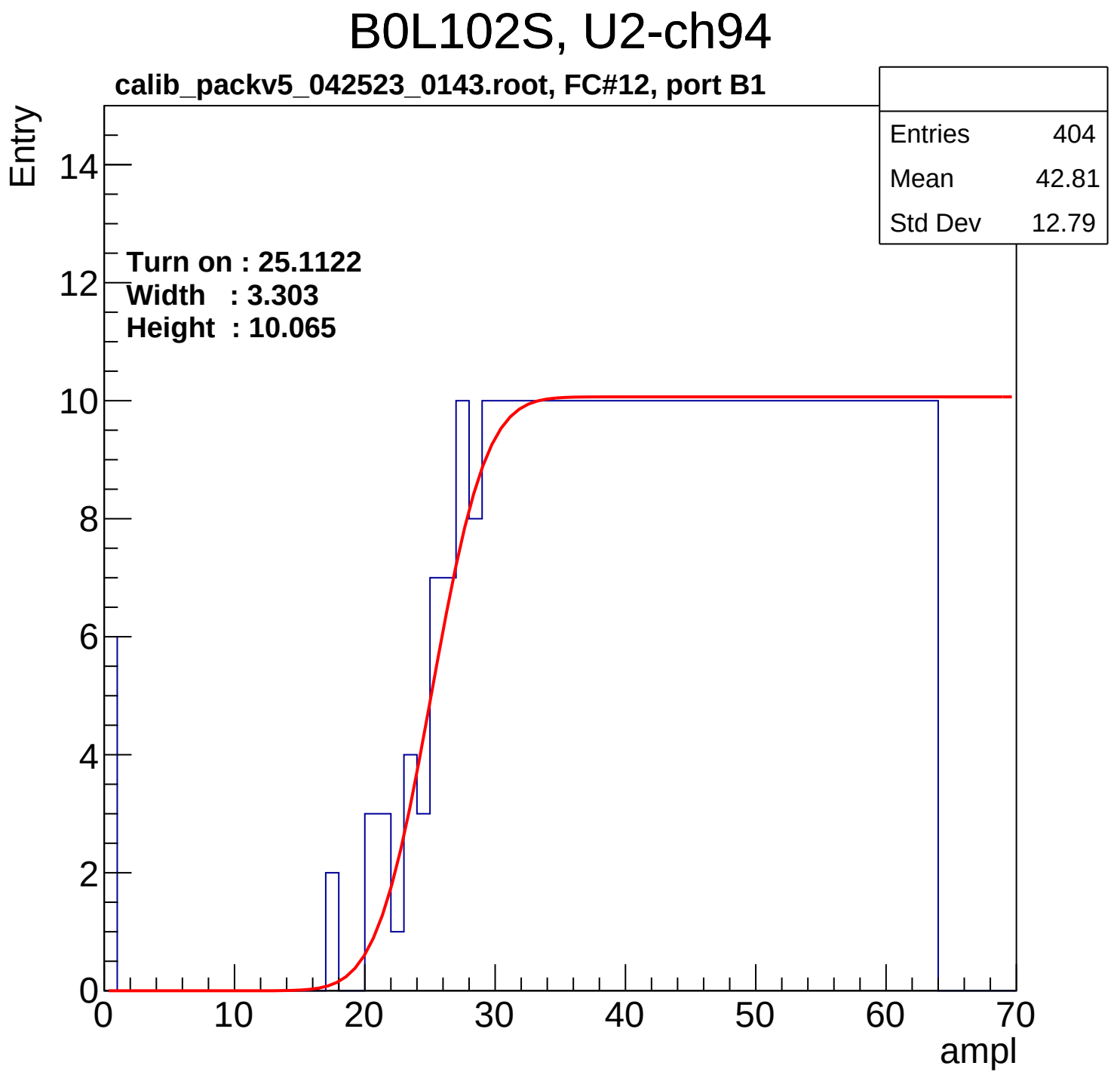
B0L102S, U2-ch94
calib_packv5_042523_0143.root, FC#12, port B1
Entries 404
Mean 42.81
Std Dev 12.79
Turn on : 25.1122
Width : 3.303
Height : 10.065
Entry
ampl
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2
4
6
8
10
12
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0
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60
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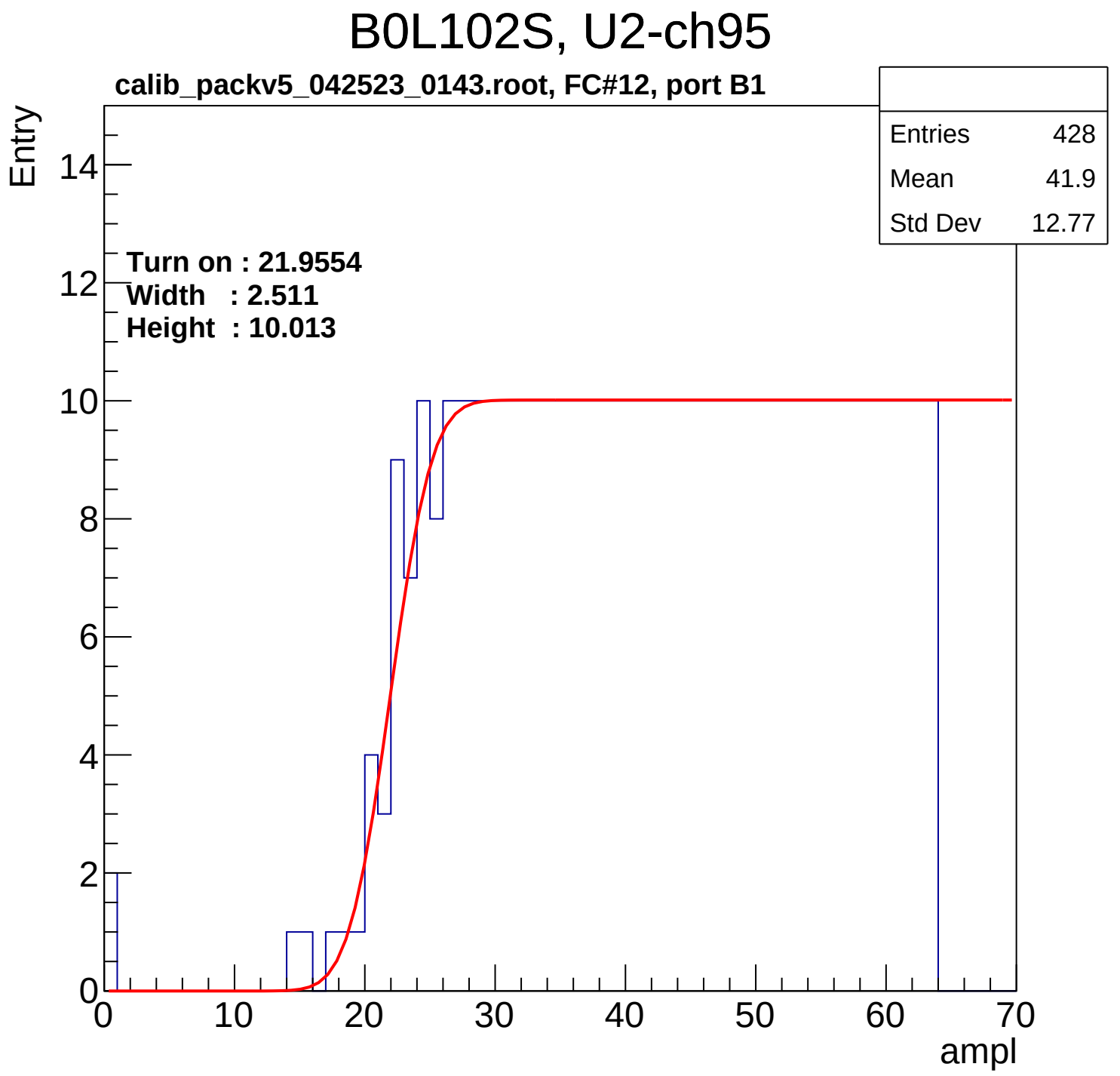
B0L102S, U2-ch95
calib_packv5_042523_0143.root, FC#12, port B1
Entries 428
Mean 41.9
Std Dev 12.77
Turn on : 21.9554
Width : 2.511
Height : 10.013
Entry
ampl
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2
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6
8
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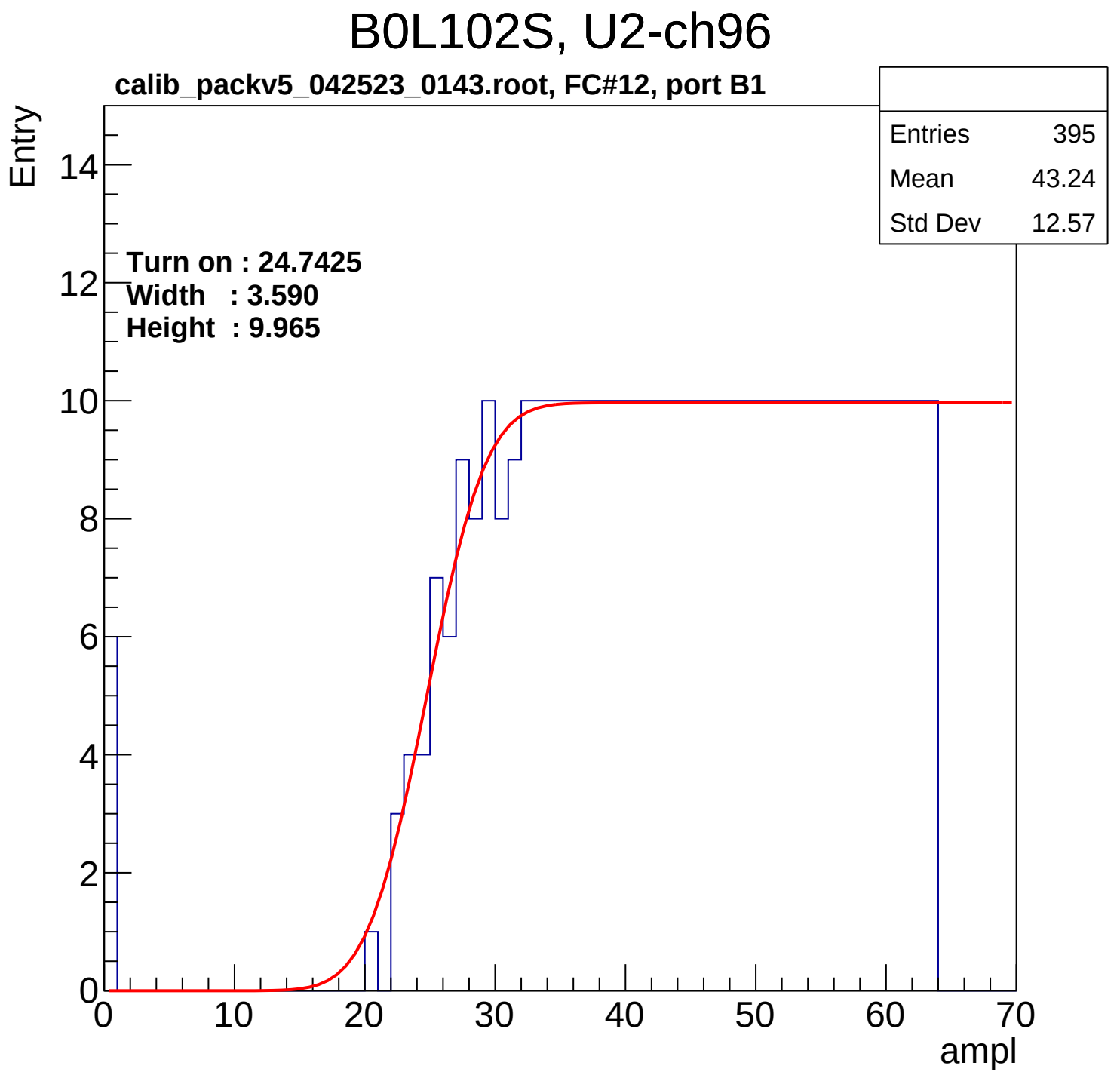
B0L102S, U2-ch96
calib_packv5_042523_0143.root, FC#12, port B1
Entries 395
Mean 43.24
Std Dev 12.57
Turn on : 24.7425
Width : 3.590
Height : 9.965
Entry
ampl
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6
8
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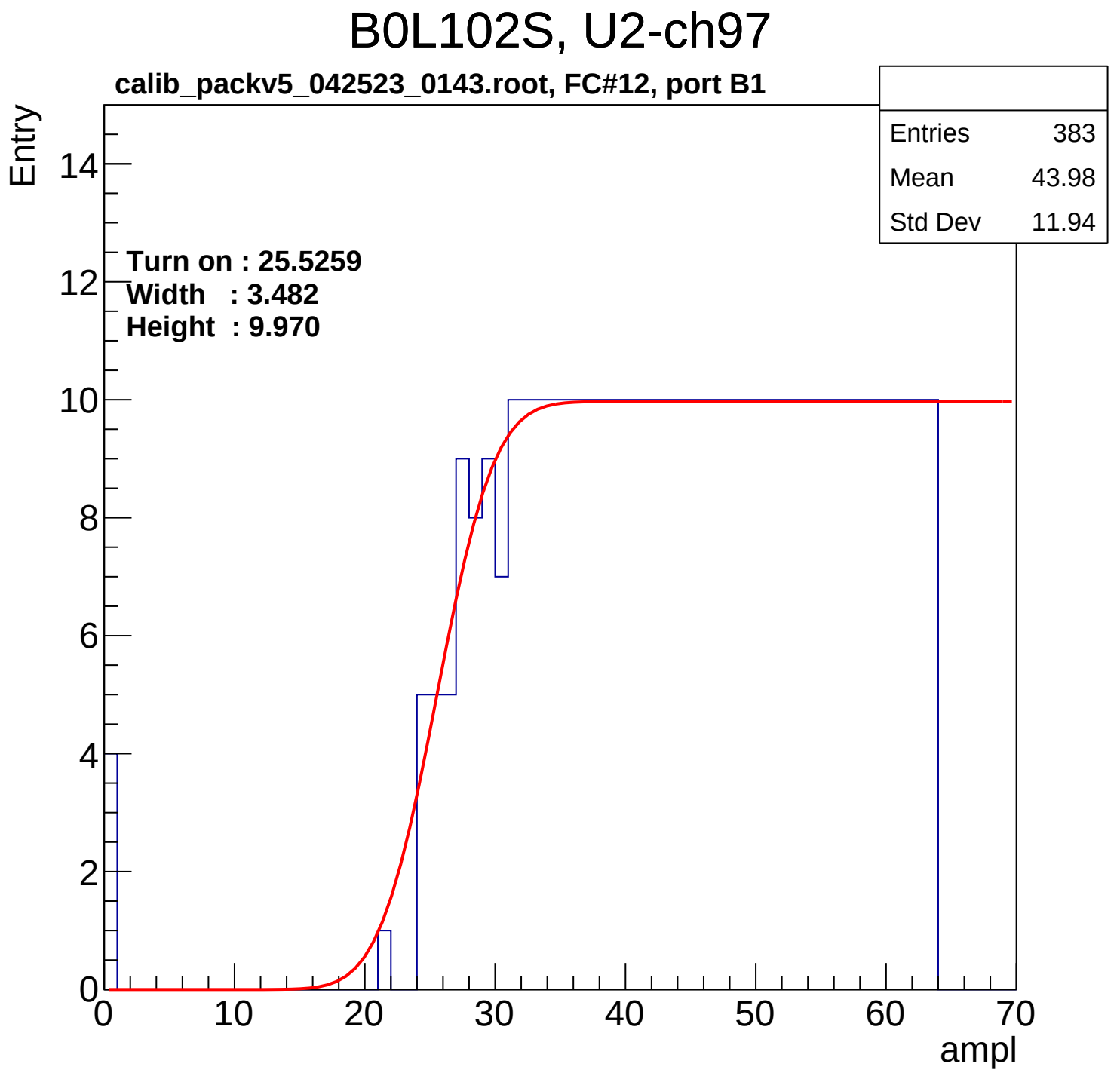
B0L102S, U2-ch97
calib_packv5_042523_0143.root, FC#12, port B1
Entries 383
Mean 43.98
Std Dev 11.94
Turn on : 25.5259
Width : 3.482
Height : 9.970
Entry
ampl
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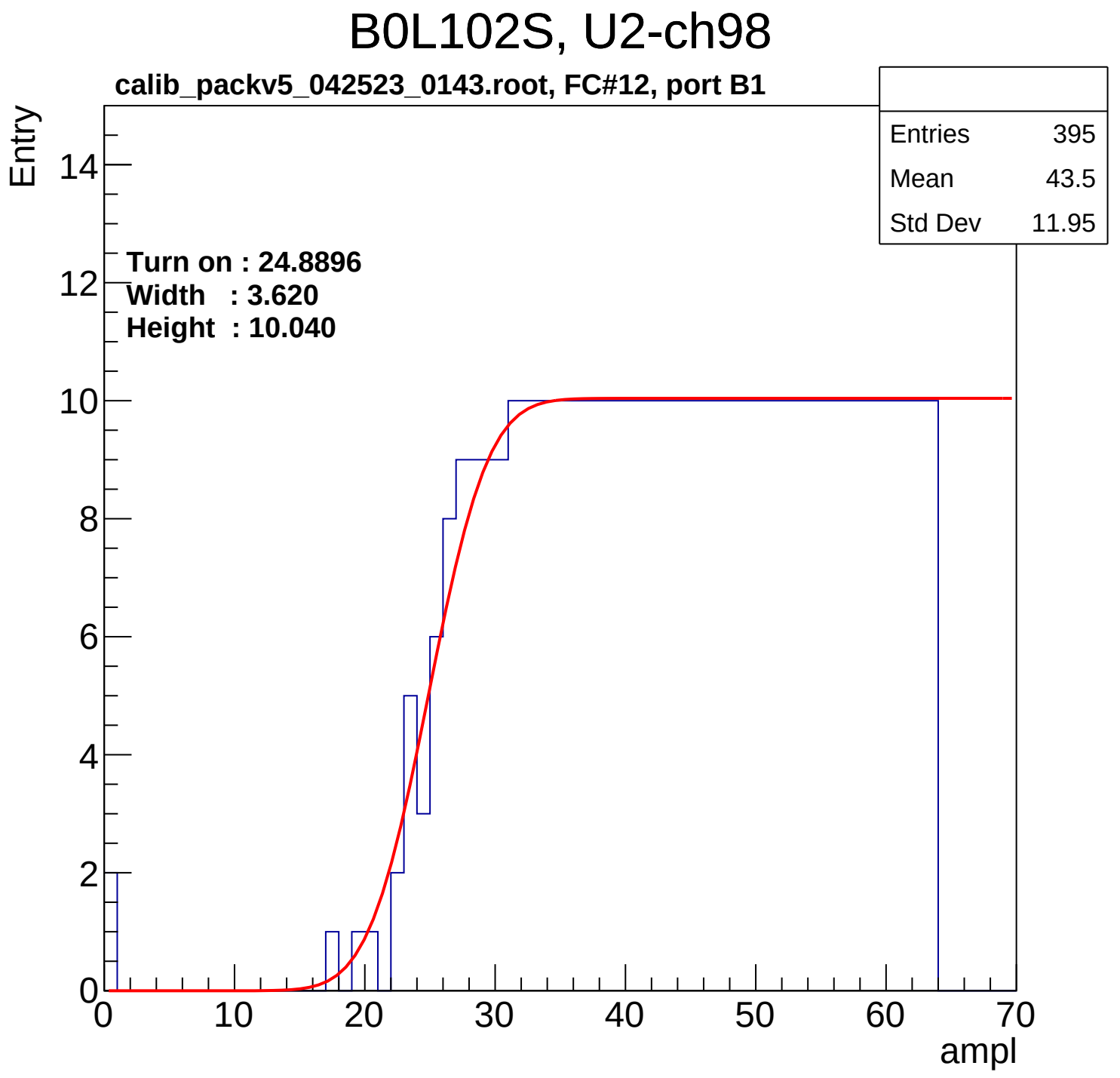
B0L102S, U2-ch98
calib_packv5_042523_0143.root, FC#12, port B1
Entries 395
Mean 43.5
Std Dev 11.95
Turn on : 24.8896
Width : 3.620
Height : 10.040
Entry
ampl
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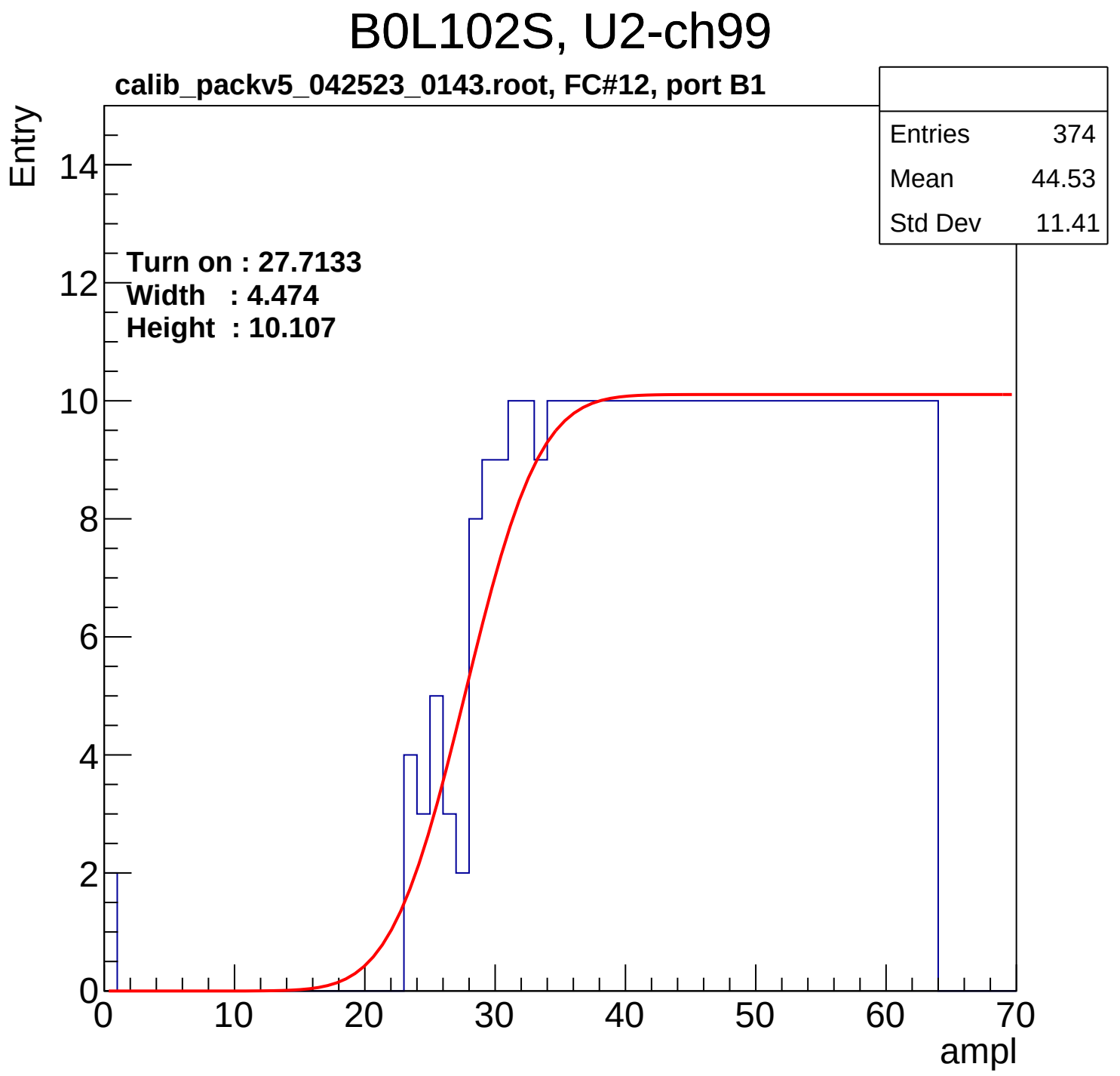
B0L102S, U2-ch99
calib_packv5_042523_0143.root, FC#12, port B1
Entries 374
Mean 44.53
Std Dev 11.41
Turn on : 27.7133
Width : 4.474
Height : 10.107
Entry
ampl
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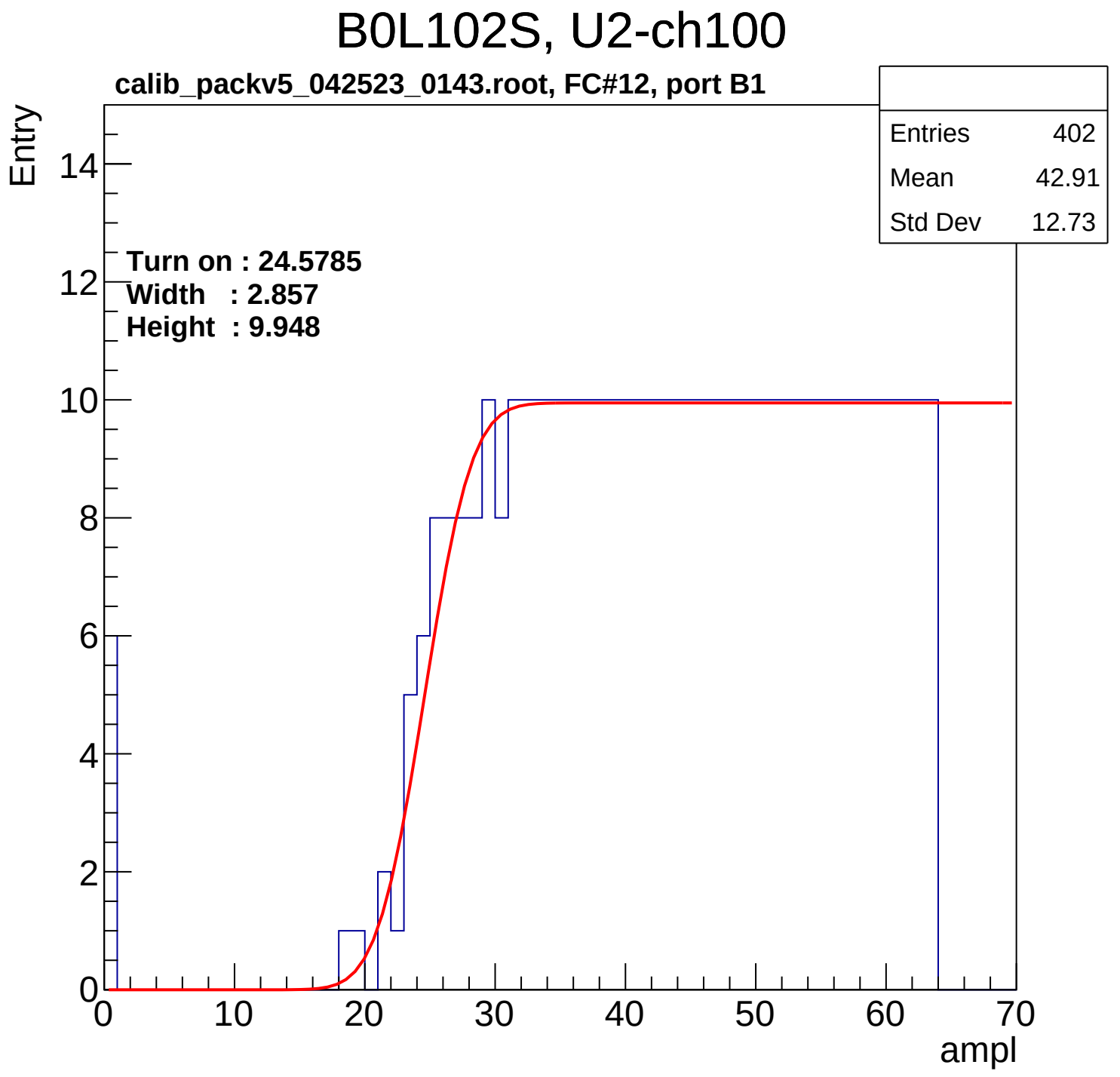
B0L102S, U2-ch100
calib_packv5_042523_0143.root, FC#12, port B1
Entries 402
Mean 42.91
Std Dev 12.73
Turn on : 24.5785
Width : 2.857
Height : 9.948
Entry
ampl
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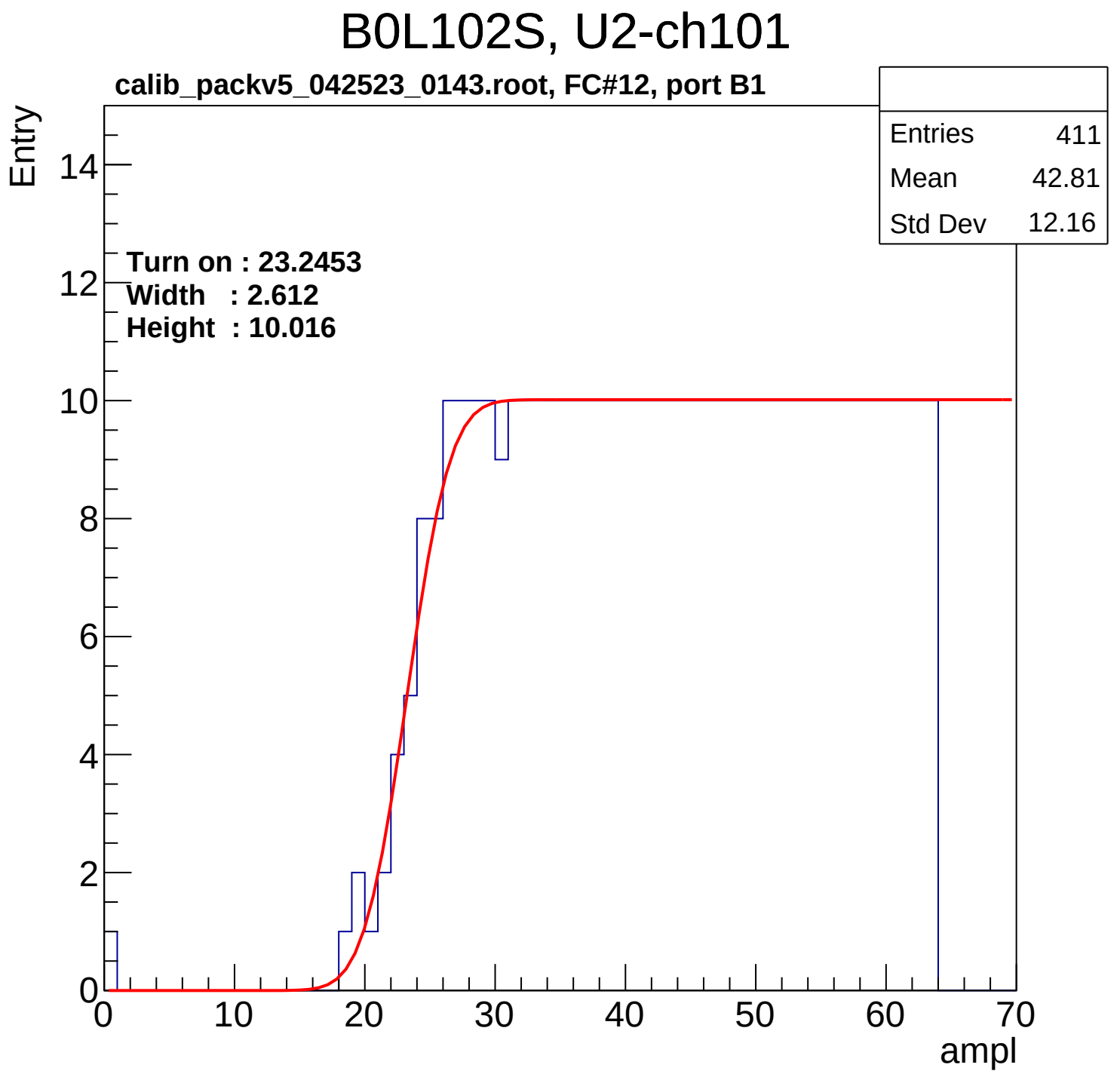
B0L102S, U2-ch101
calib_packv5_042523_0143.root, FC#12, port B1
Entries 411
Mean 42.81
Std Dev 12.16
Turn on : 23.2453
Width : 2.612
Height : 10.016
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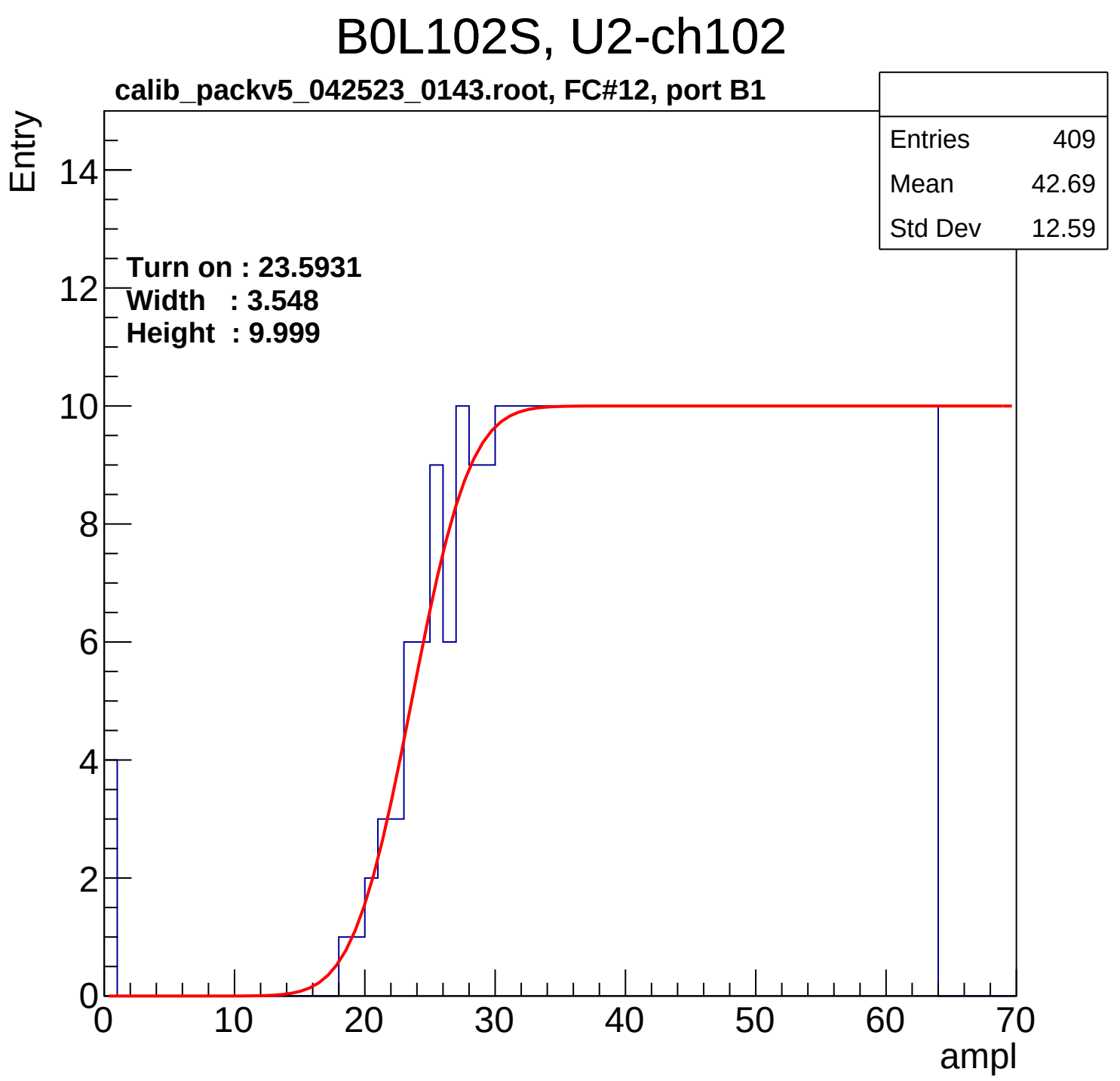
B0L102S, U2-ch102
calib_packv5_042523_0143.root, FC#12, port B1
Entries 409
Mean 42.69
Std Dev 12.59
Turn on : 23.5931
Width : 3.548
Height : 9.999
Entry
ampl
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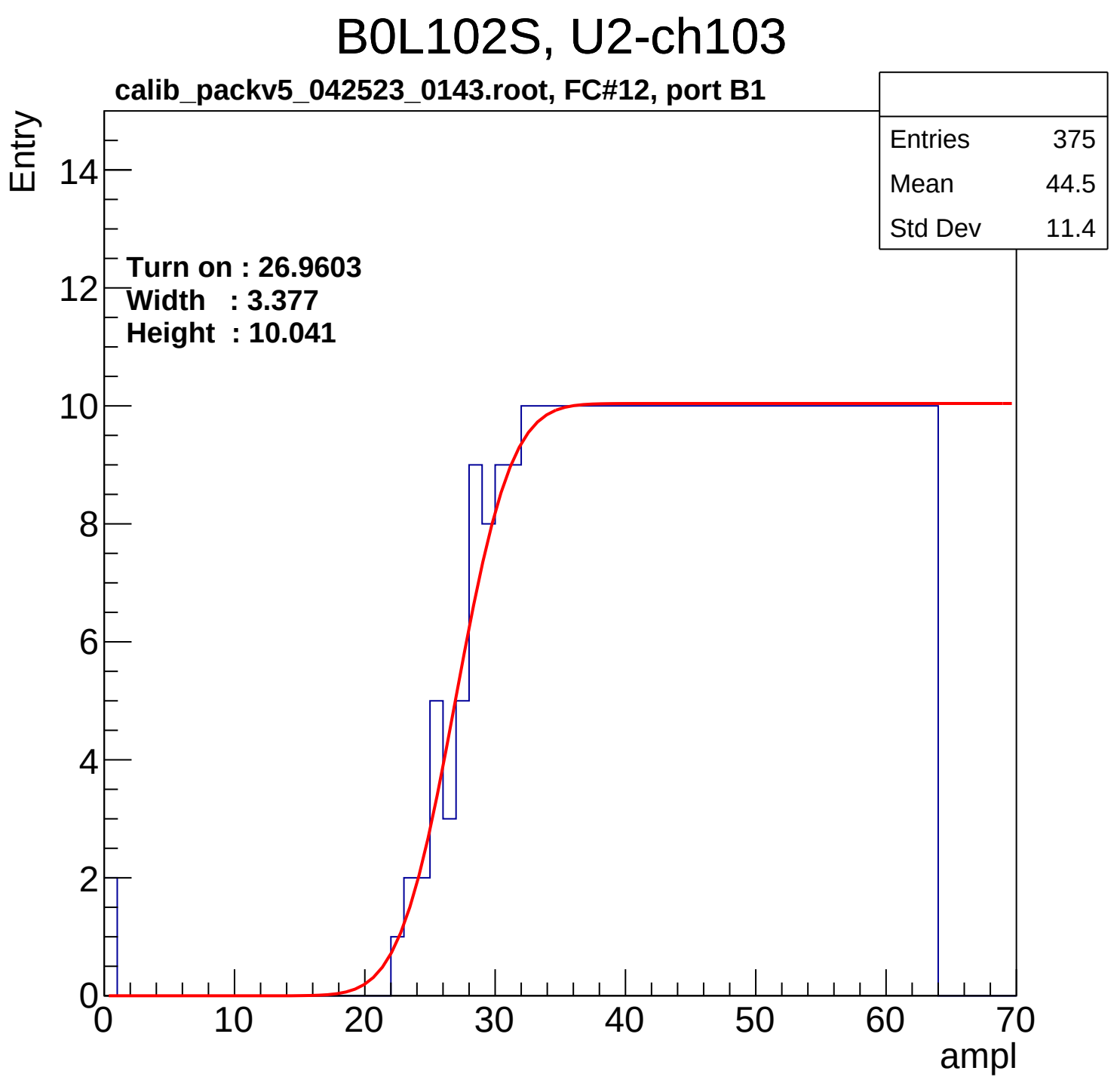
B0L102S, U2-ch103
calib_packv5_042523_0143.root, FC#12, port B1
Entries 375
Mean 44.5
Std Dev 11.4
Turn on : 26.9603
Width : 3.377
Height : 10.041
Entry
ampl
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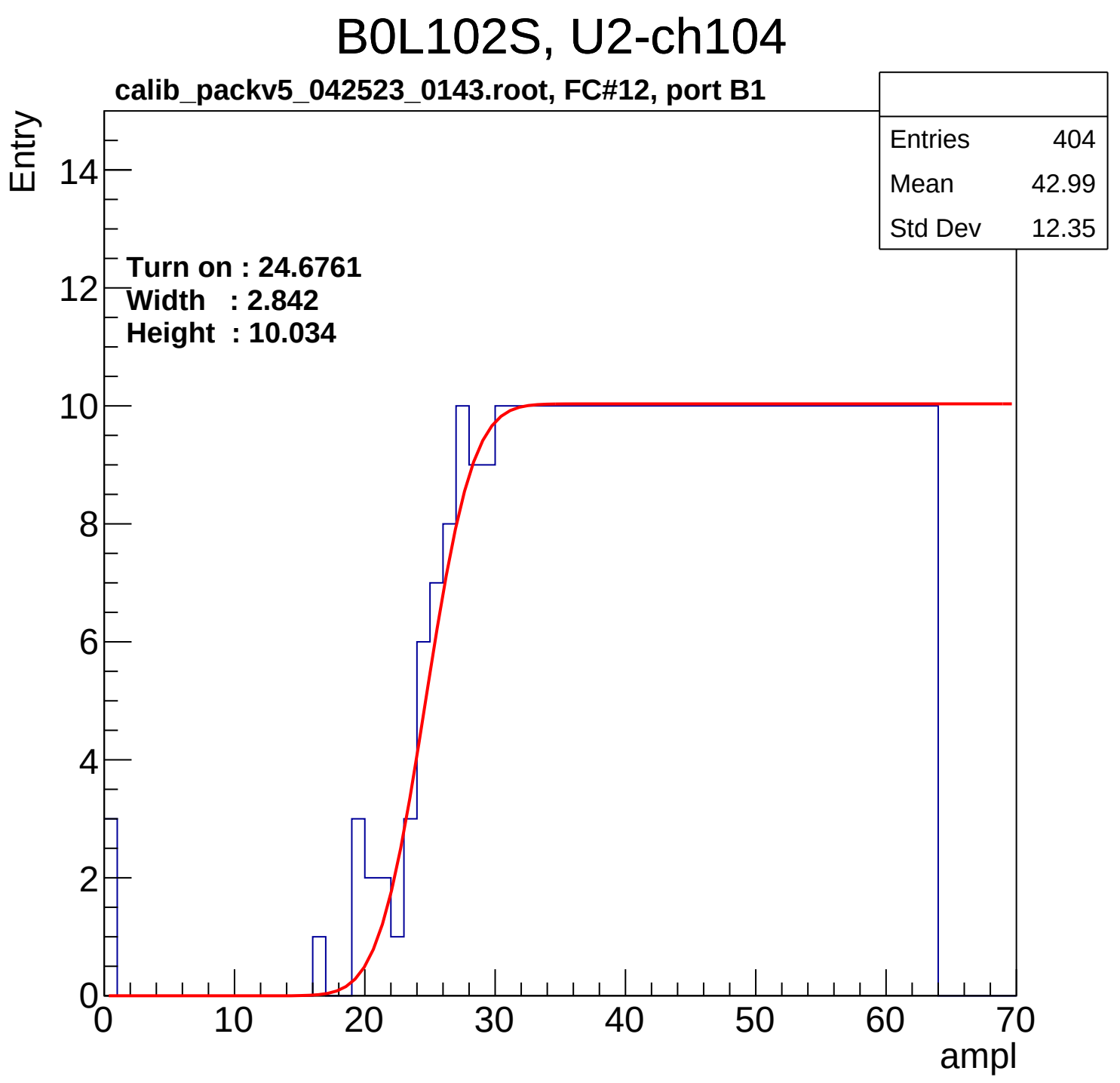
B0L102S, U2-ch104
calib_packv5_042523_0143.root, FC#12, port B1
Entries 404
Mean 42.99
Std Dev 12.35
Turn on : 24.6761
Width : 2.842
Height : 10.034
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ampl
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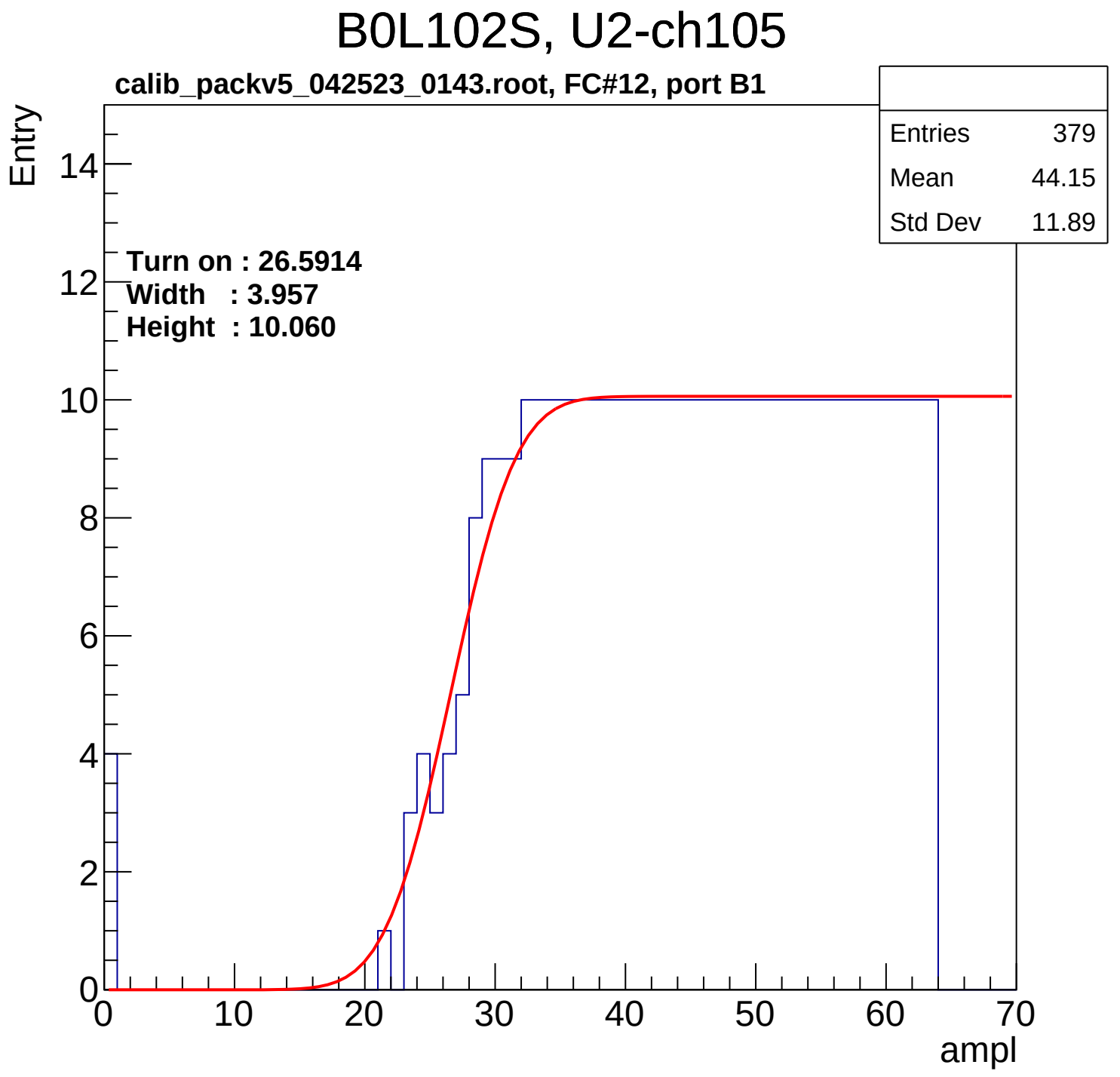
B0L102S, U2-ch105
calib_packv5_042523_0143.root, FC#12, port B1
Entries 379
Mean 44.15
Std Dev 11.89
Turn on : 26.5914
Width : 3.957
Height : 10.060
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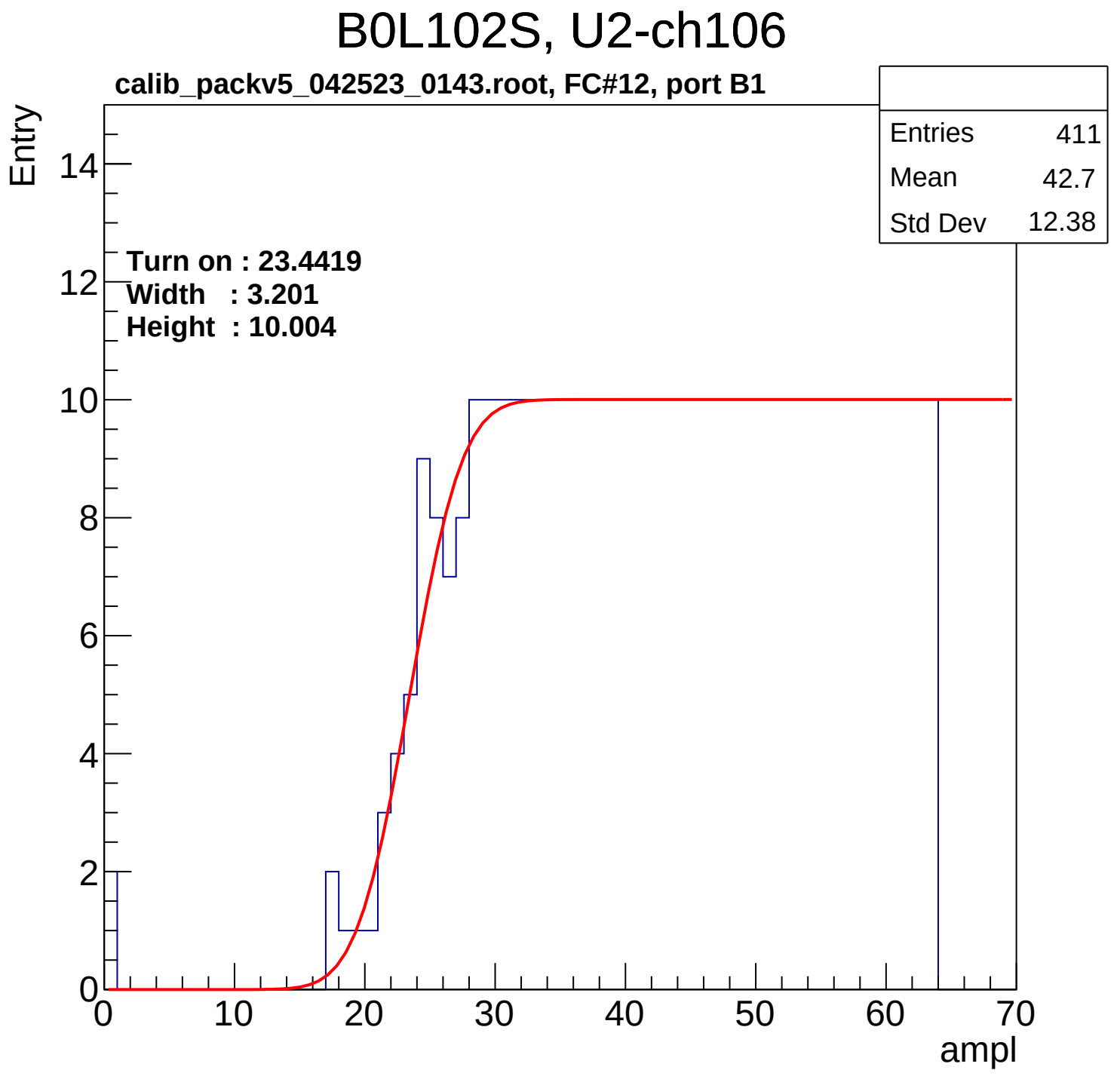
B0L102S, U2-ch106
calib_packv5_042523_0143.root, FC#12, port B1
Entries 411
Mean 42.7
Std Dev 12.38
Turn on : 23.4419
Width : 3.201
Height : 10.004
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ampl
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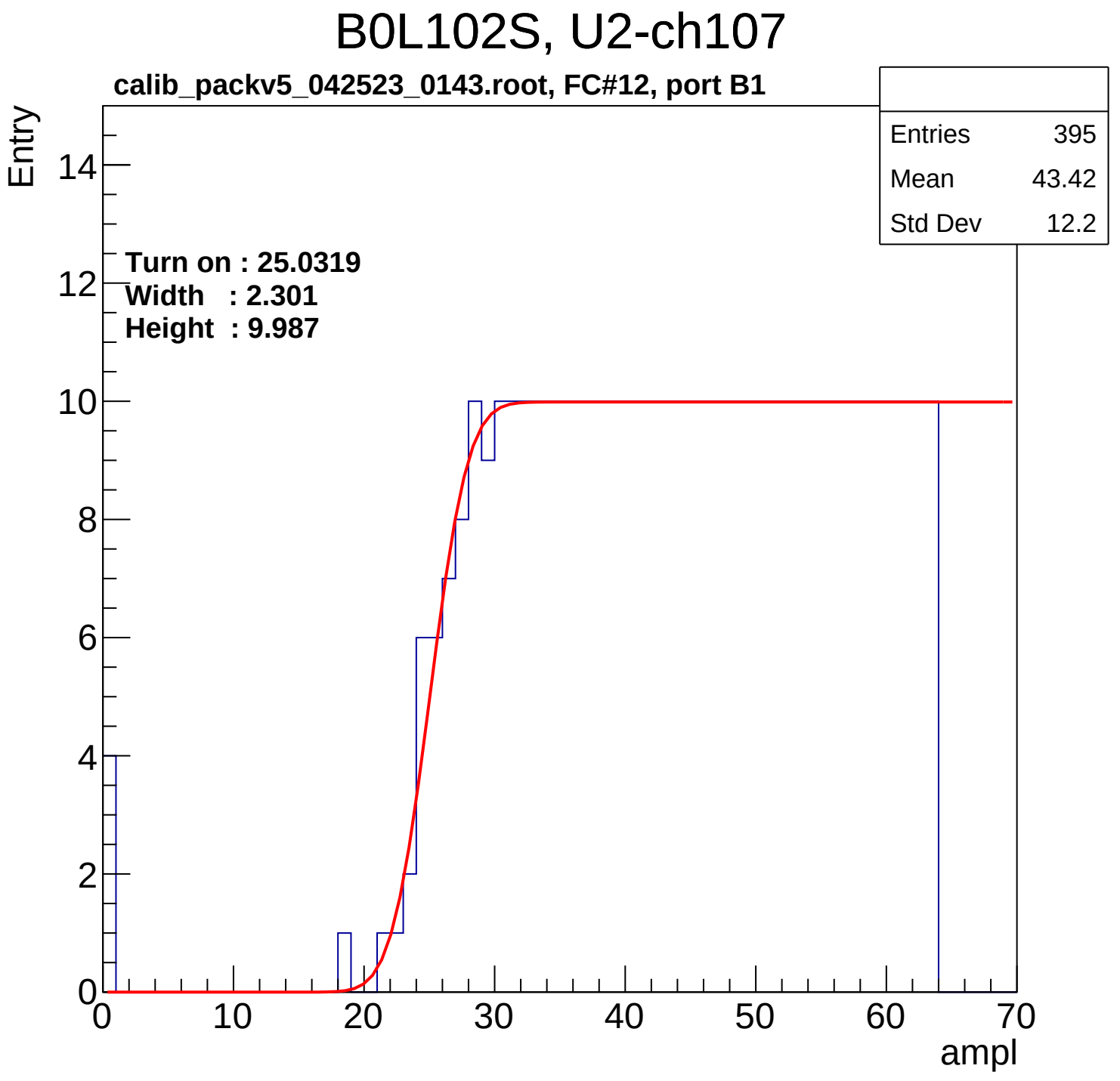
B0L102S, U2-ch107
calib_packv5_042523_0143.root, FC#12, port B1
Entries 395
Mean 43.42
Std Dev 12.2
Turn on : 25.0319
Width : 2.301
Height : 9.987
Entry
ampl
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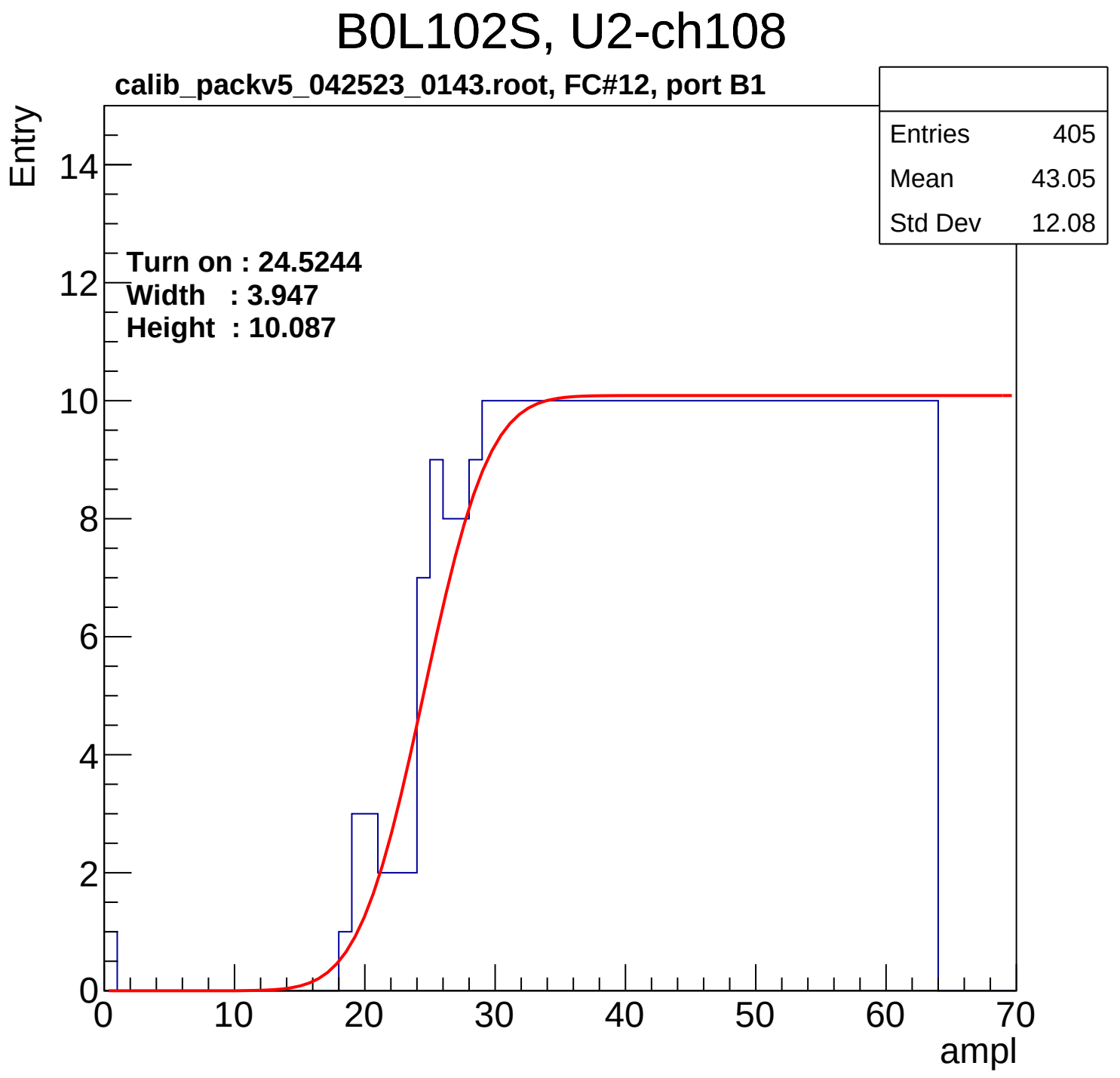
B0L102S, U2-ch108
calib_packv5_042523_0143.root, FC#12, port B1
Entries 405
Mean 43.05
Std Dev 12.08
Turn on : 24.5244
Width : 3.947
Height : 10.087
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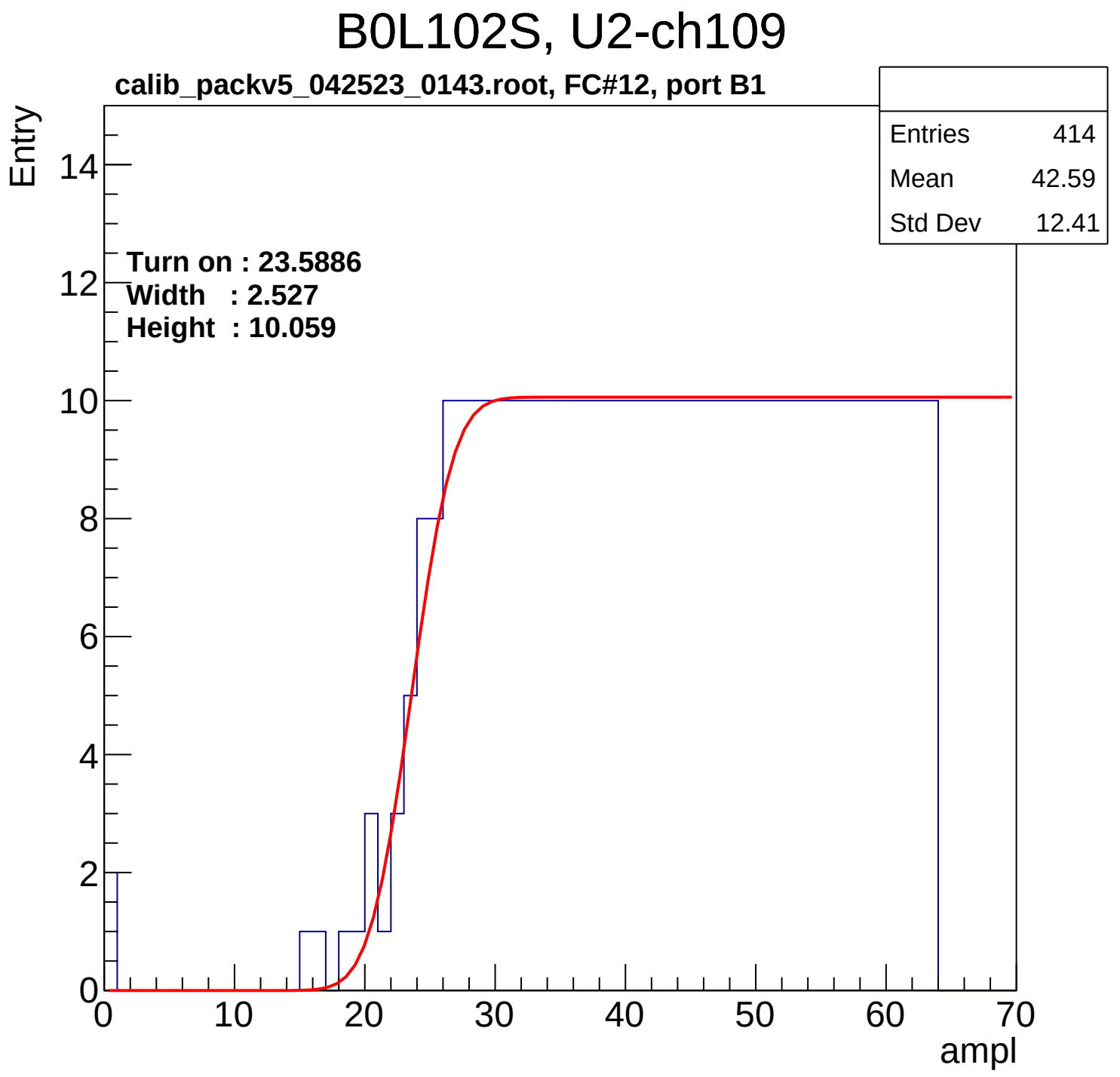
B0L102S, U2-ch109
calib_packv5_042523_0143.root, FC#12, port B1
Entries 414
Mean 42.59
Std Dev 12.41
Turn on : 23.5886
Width : 2.527
Height : 10.059
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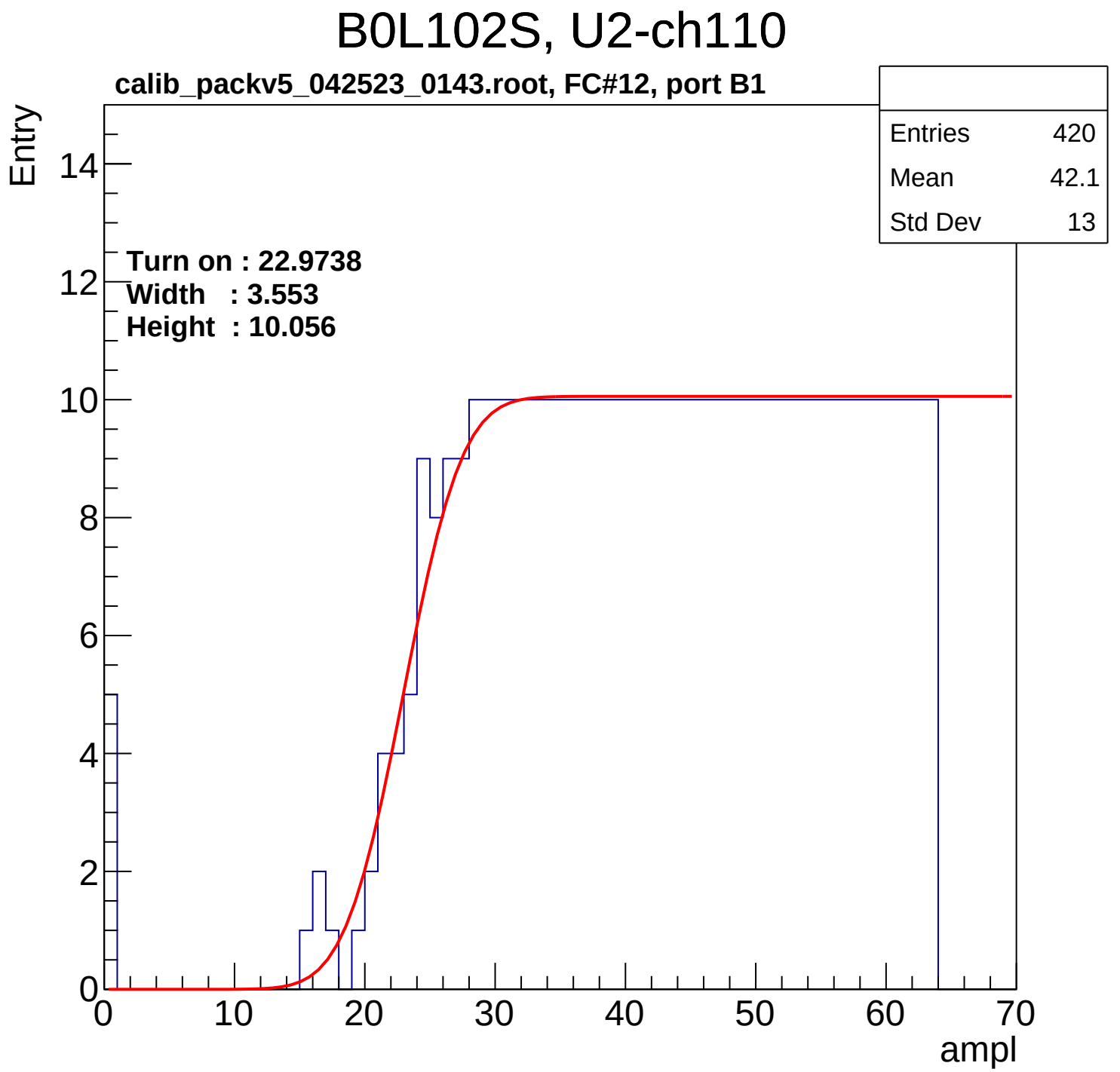
B0L102S, U2-ch110
calib_packv5_042523_0143.root, FC#12, port B1
Entries 420
Mean 42.1
Std Dev 13
Turn on : 22.9738
Width : 3.553
Height : 10.056
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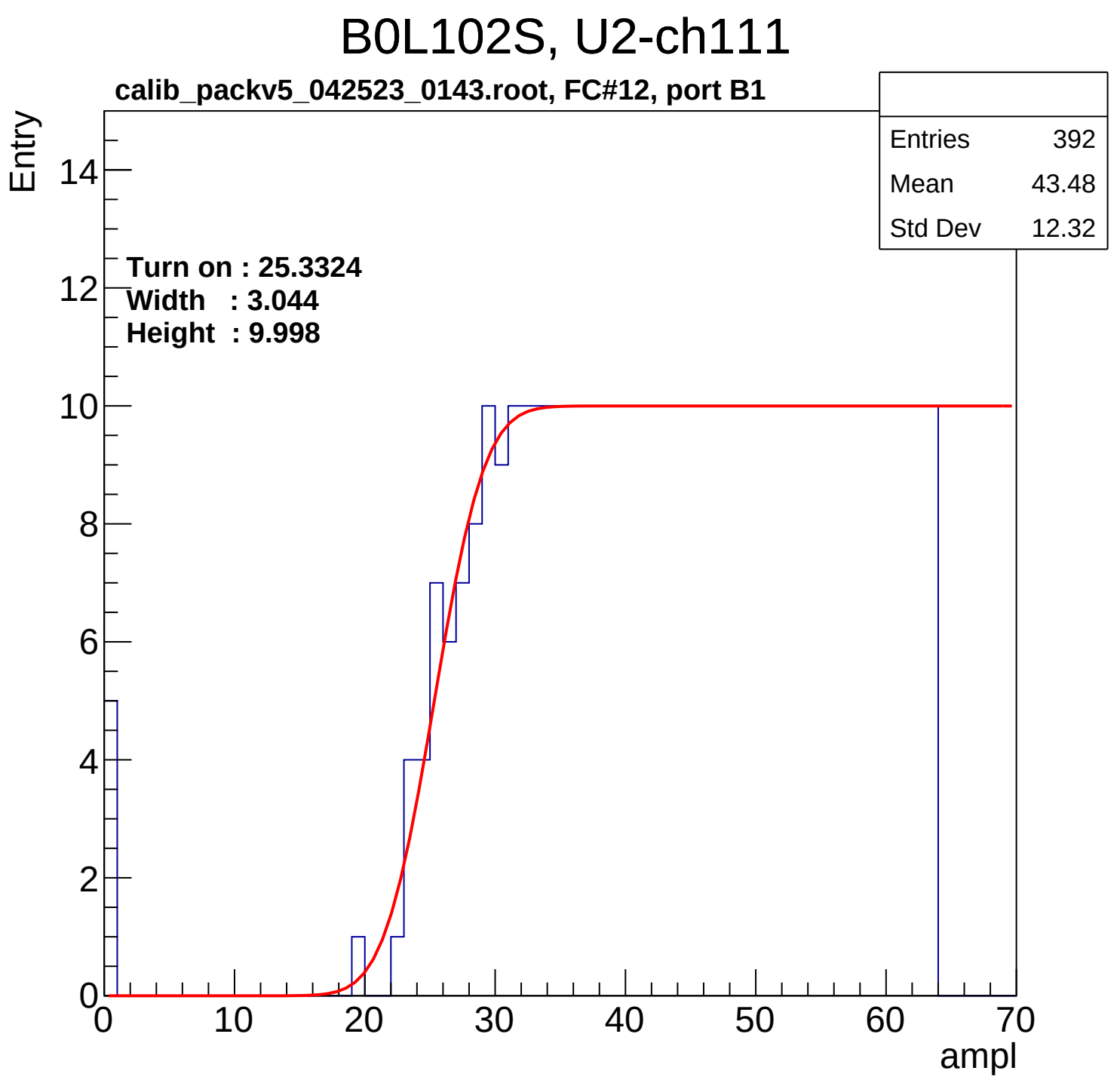
B0L102S, U2-ch111
calib_packv5_042523_0143.root, FC#12, port B1
Entries 392
Mean 43.48
Std Dev 12.32
Turn on : 25.3324
Width : 3.044
Height : 9.998
Entry
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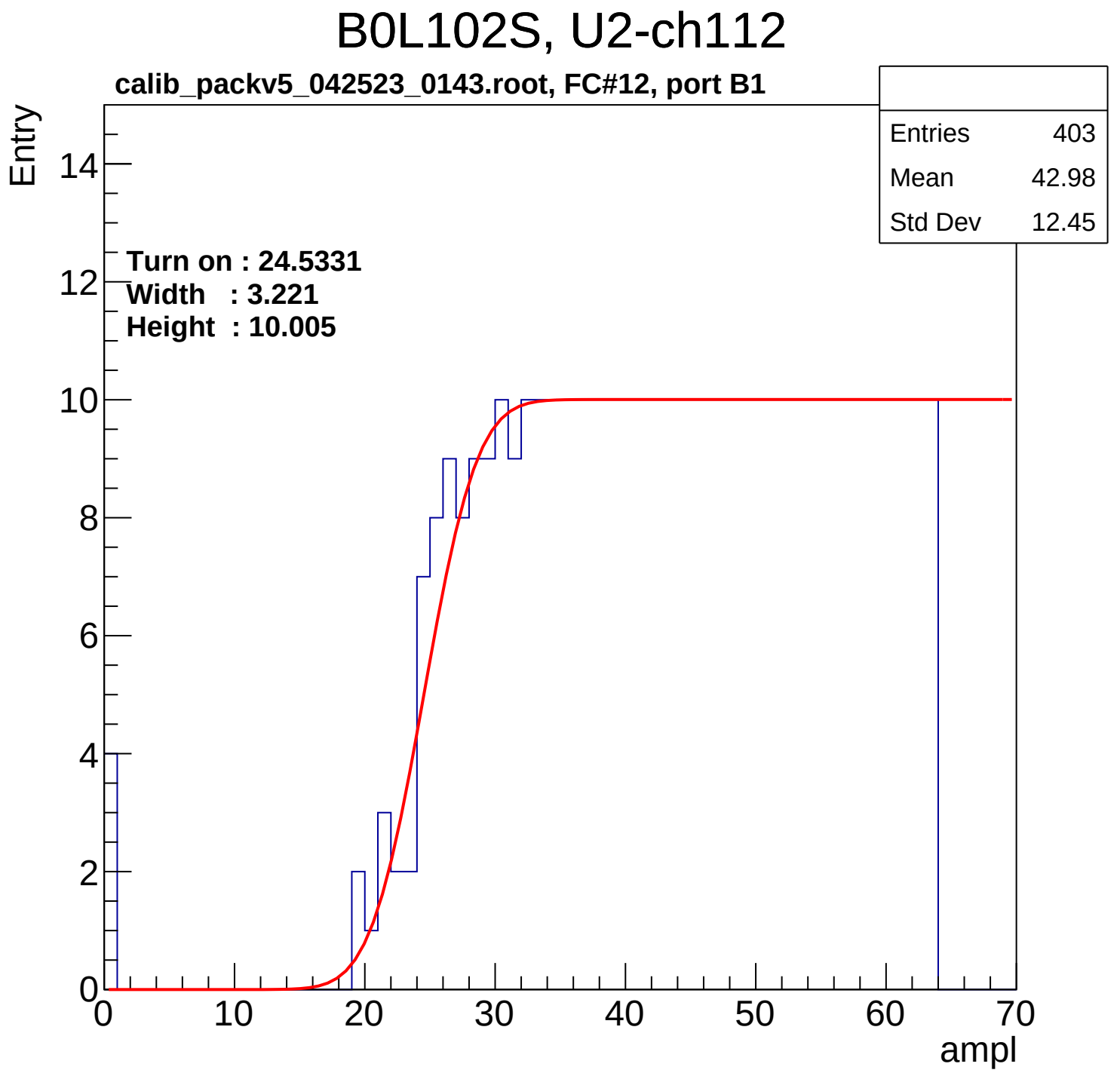
B0L102S, U2-ch112
calib_packv5_042523_0143.root, FC#12, port B1
Entries 403
Mean 42.98
Std Dev 12.45
Turn on : 24.5331
Width : 3.221
Height : 10.005
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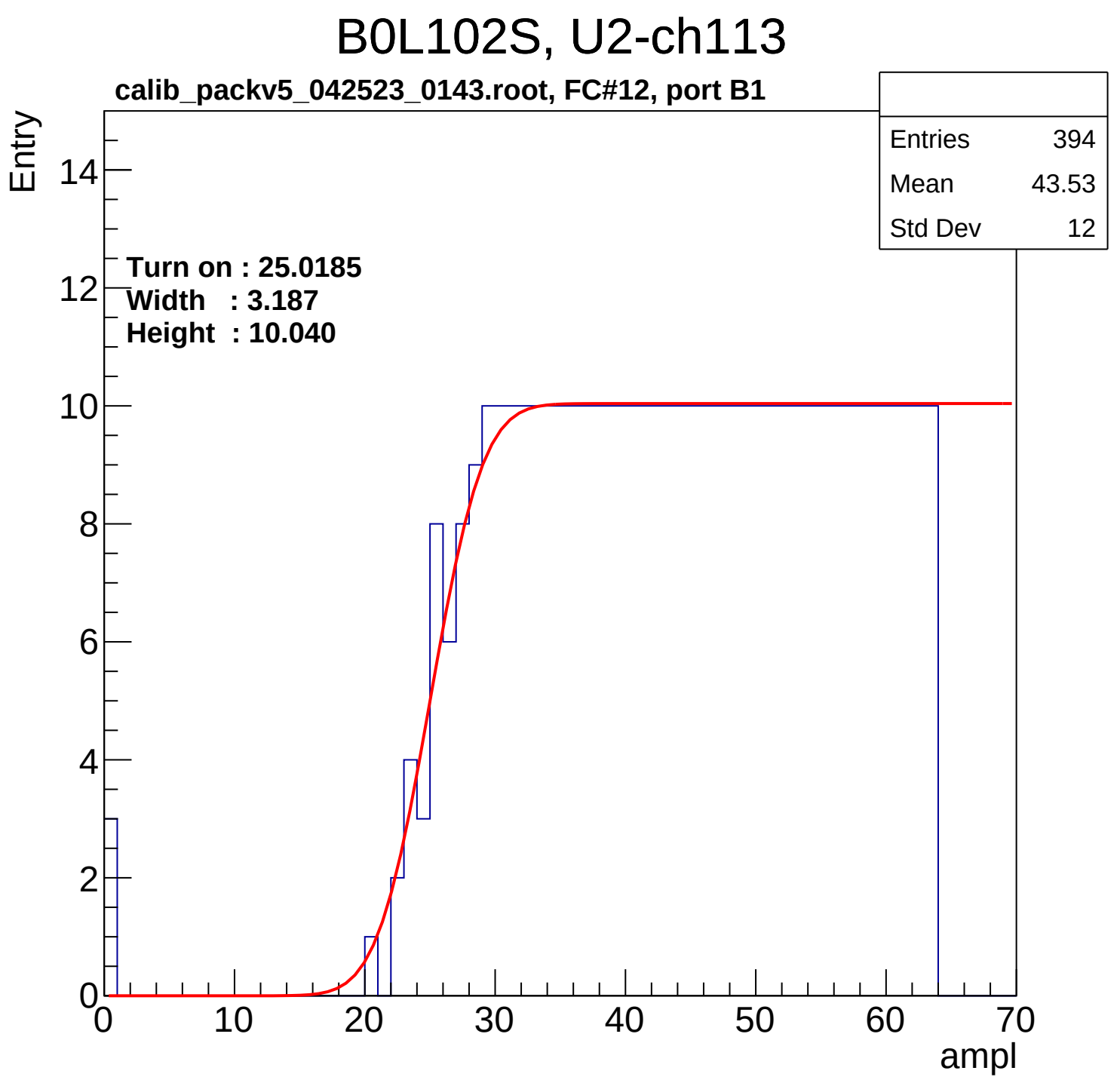
B0L102S, U2-ch113
calib_packv5_042523_0143.root, FC#12, port B1
Entries 394
Mean 43.53
Std Dev 12
Turn on : 25.0185
Width : 3.187
Height : 10.040
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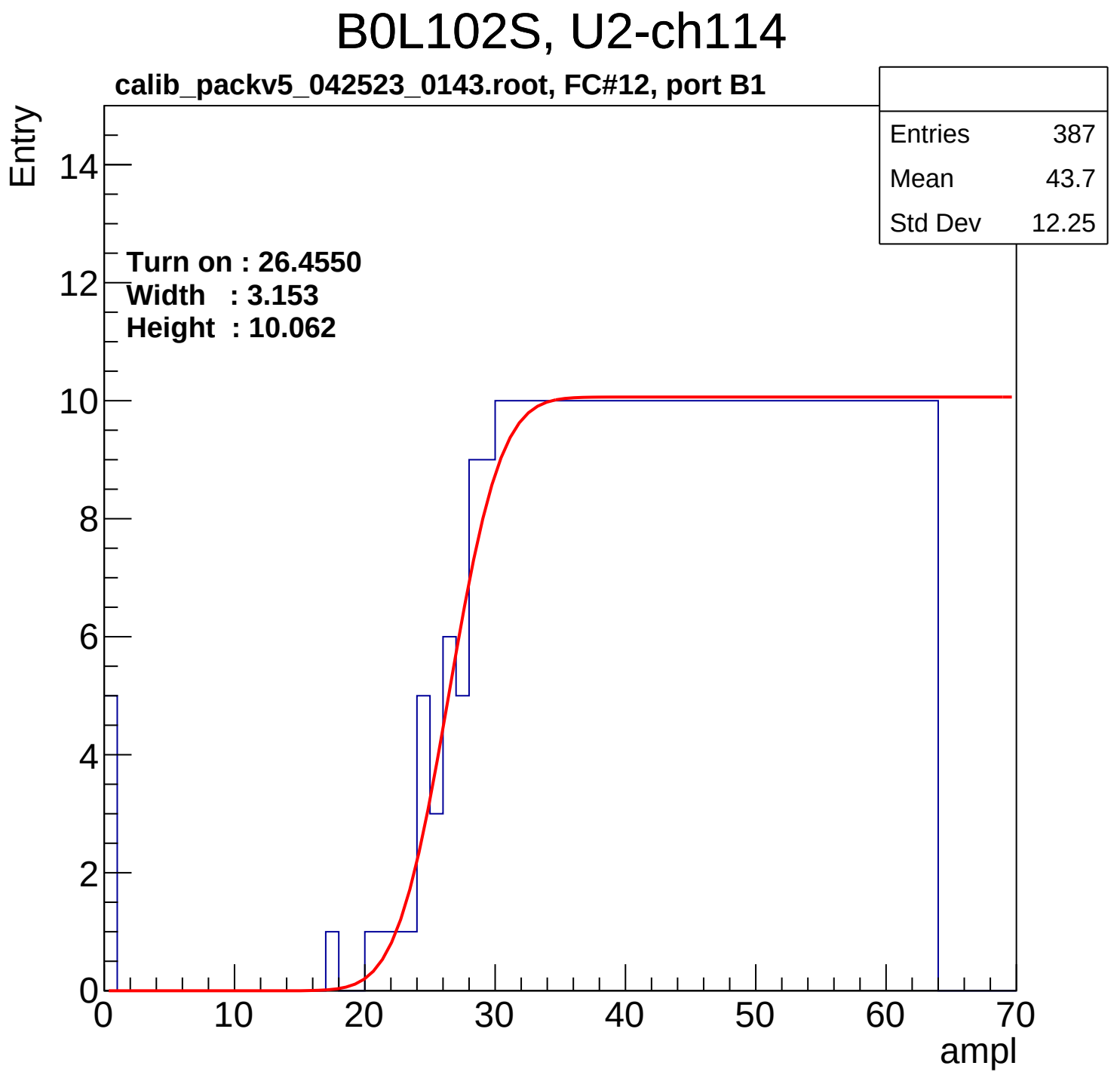
B0L102S, U2-ch114
calib_packv5_042523_0143.root, FC#12, port B1
Entries 387
Mean 43.7
Std Dev 12.25
Turn on : 26.4550
Width : 3.153
Height : 10.062
Entry
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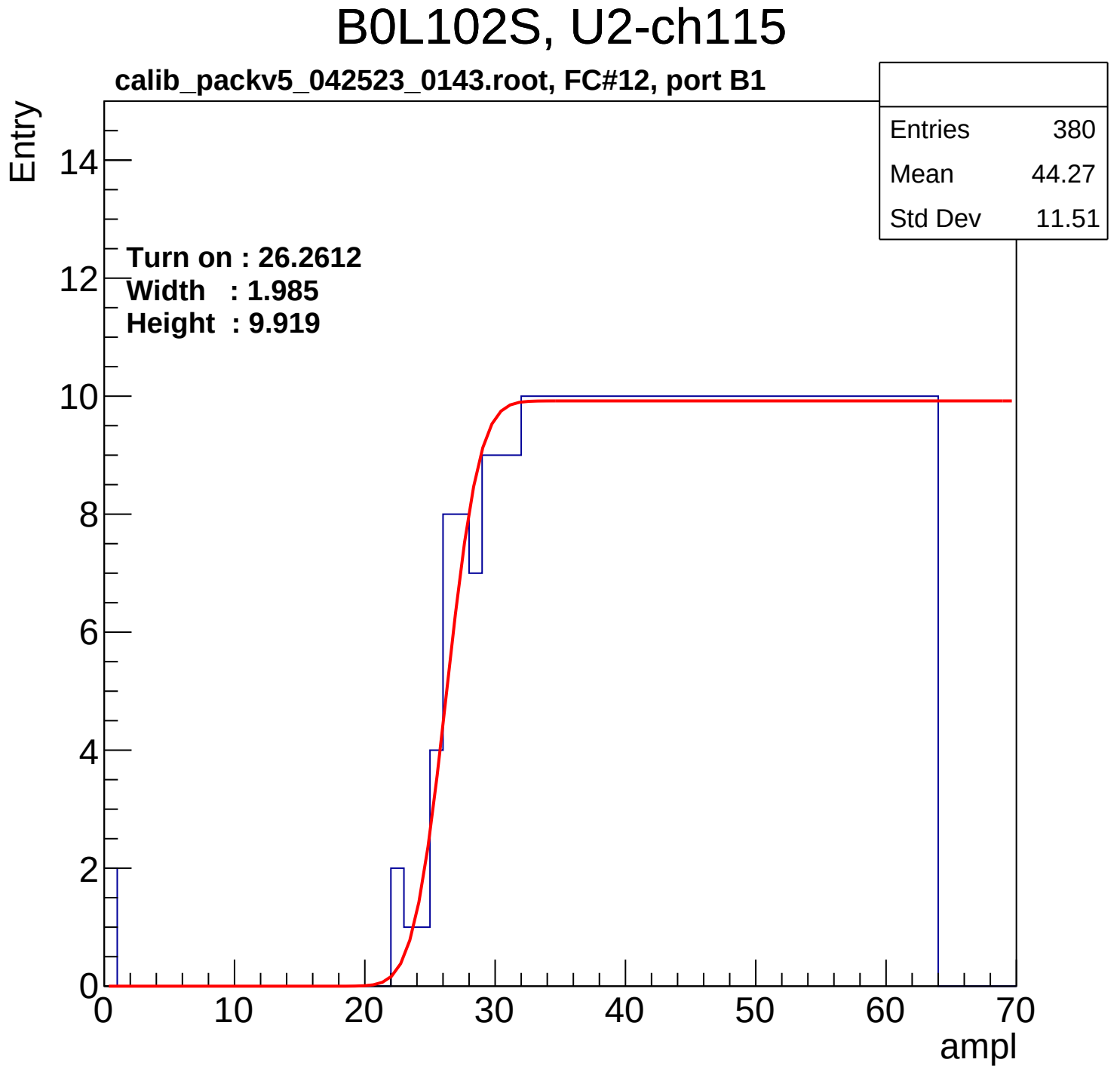
B0L102S, U2-ch115
calib_packv5_042523_0143.root, FC#12, port B1
Entries 380
Mean 44.27
Std Dev 11.51
Turn on : 26.2612
Width : 1.985
Height : 9.919
Entry
ampl
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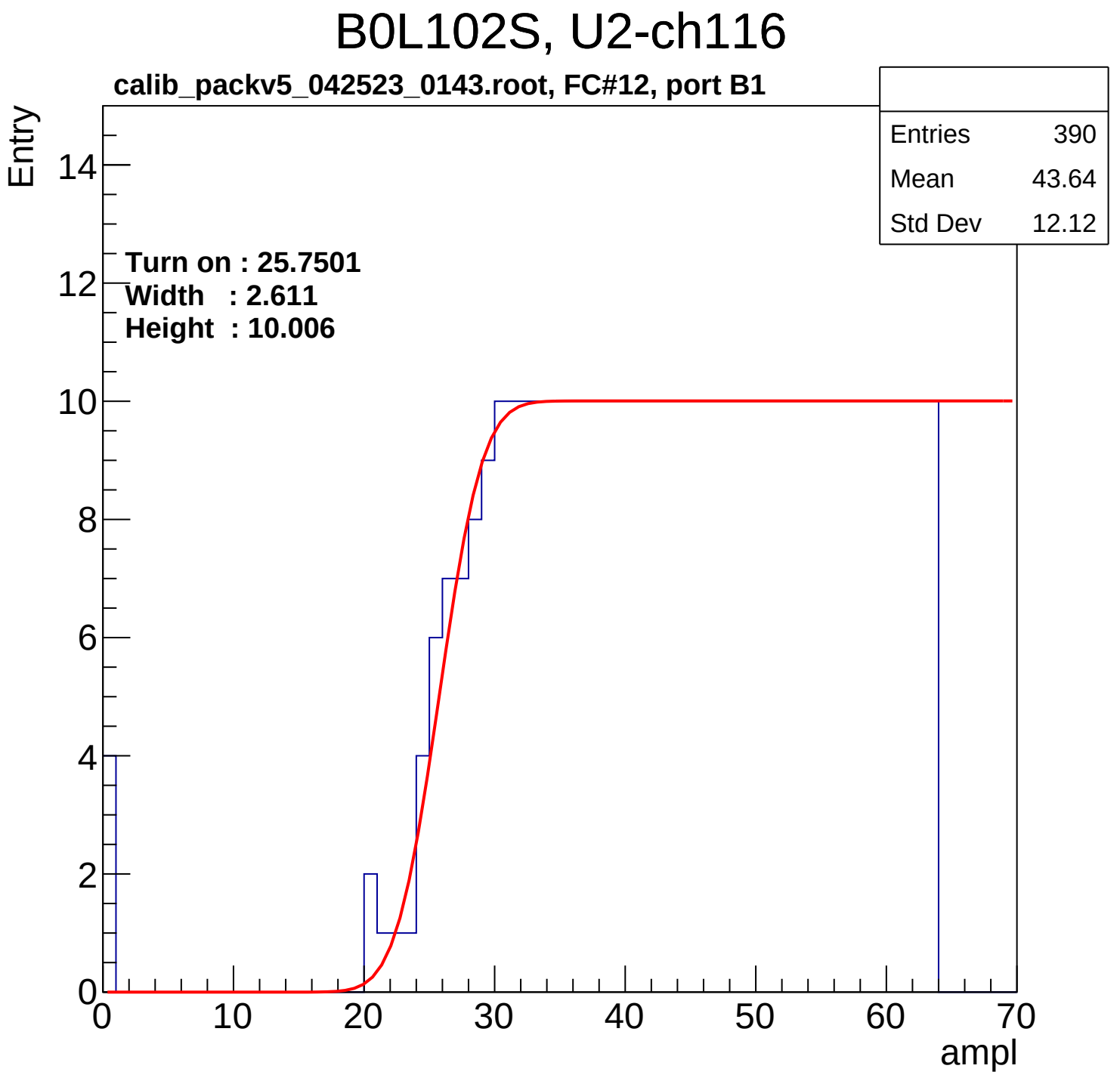
B0L102S, U2-ch116
calib_packv5_042523_0143.root, FC#12, port B1
Entries 390
Mean 43.64
Std Dev 12.12
Turn on : 25.7501
Width : 2.611
Height : 10.006
Entry
ampl
0
2
4
6
8
10
12
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0
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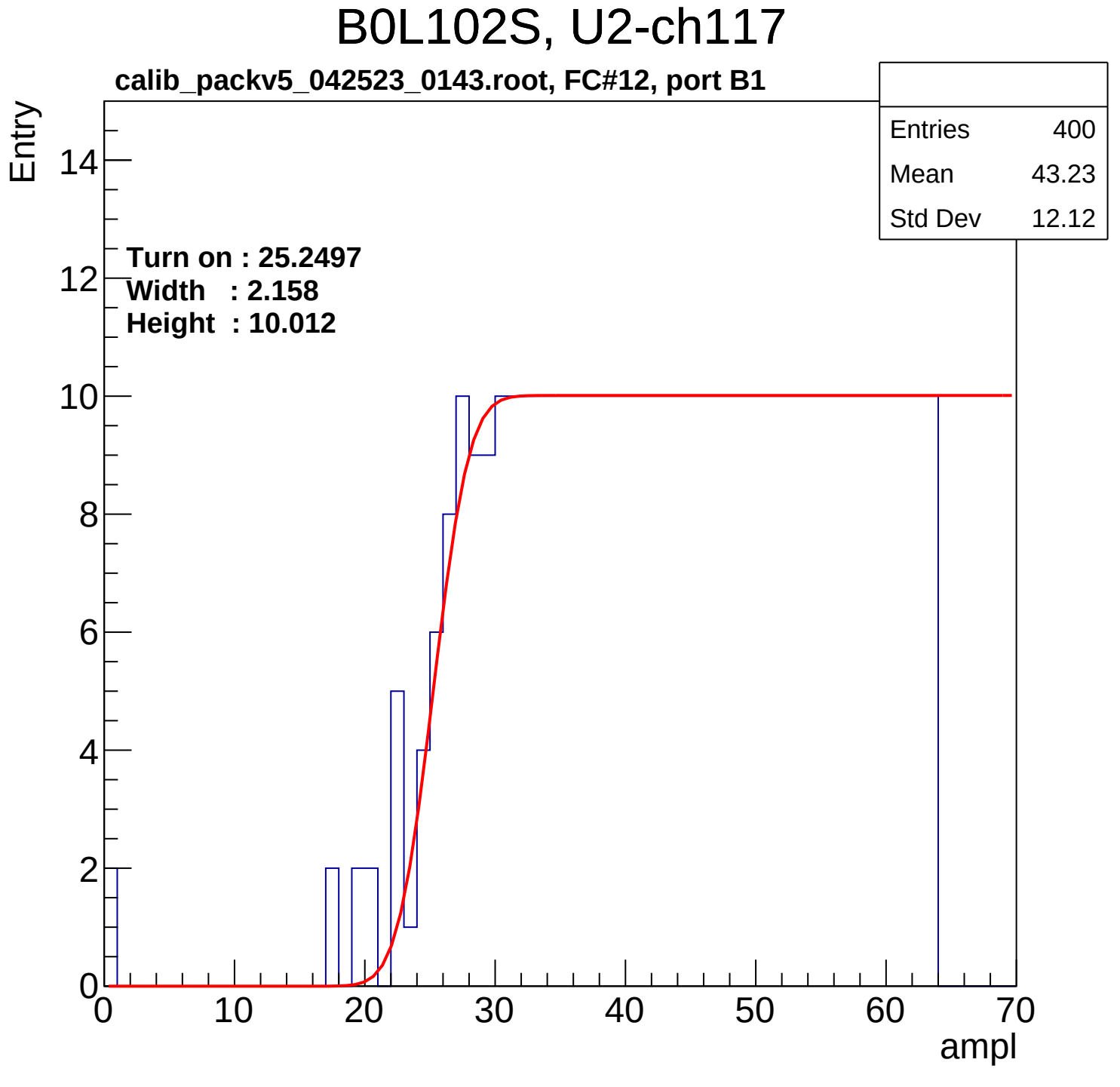
B0L102S, U2-ch117
calib_packv5_042523_0143.root, FC#12, port B1
Entries 400
Mean 43.23
Std Dev 12.12
Turn on : 25.2497
Width : 2.158
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
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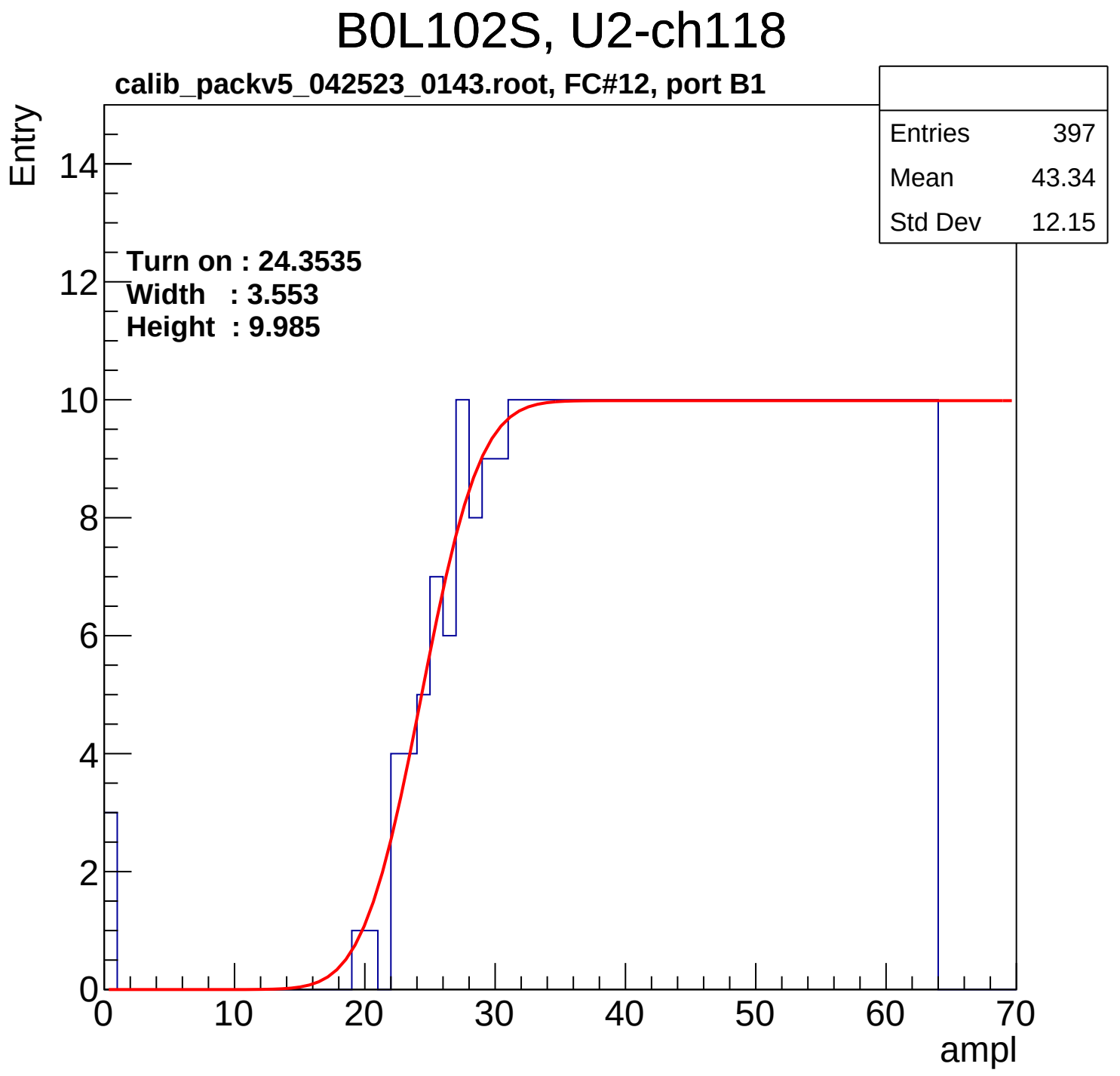
B0L102S, U2-ch118
calib_packv5_042523_0143.root, FC#12, port B1
Entries 397
Mean 43.34
Std Dev 12.15
Turn on : 24.3535
Width : 3.553
Height : 9.985
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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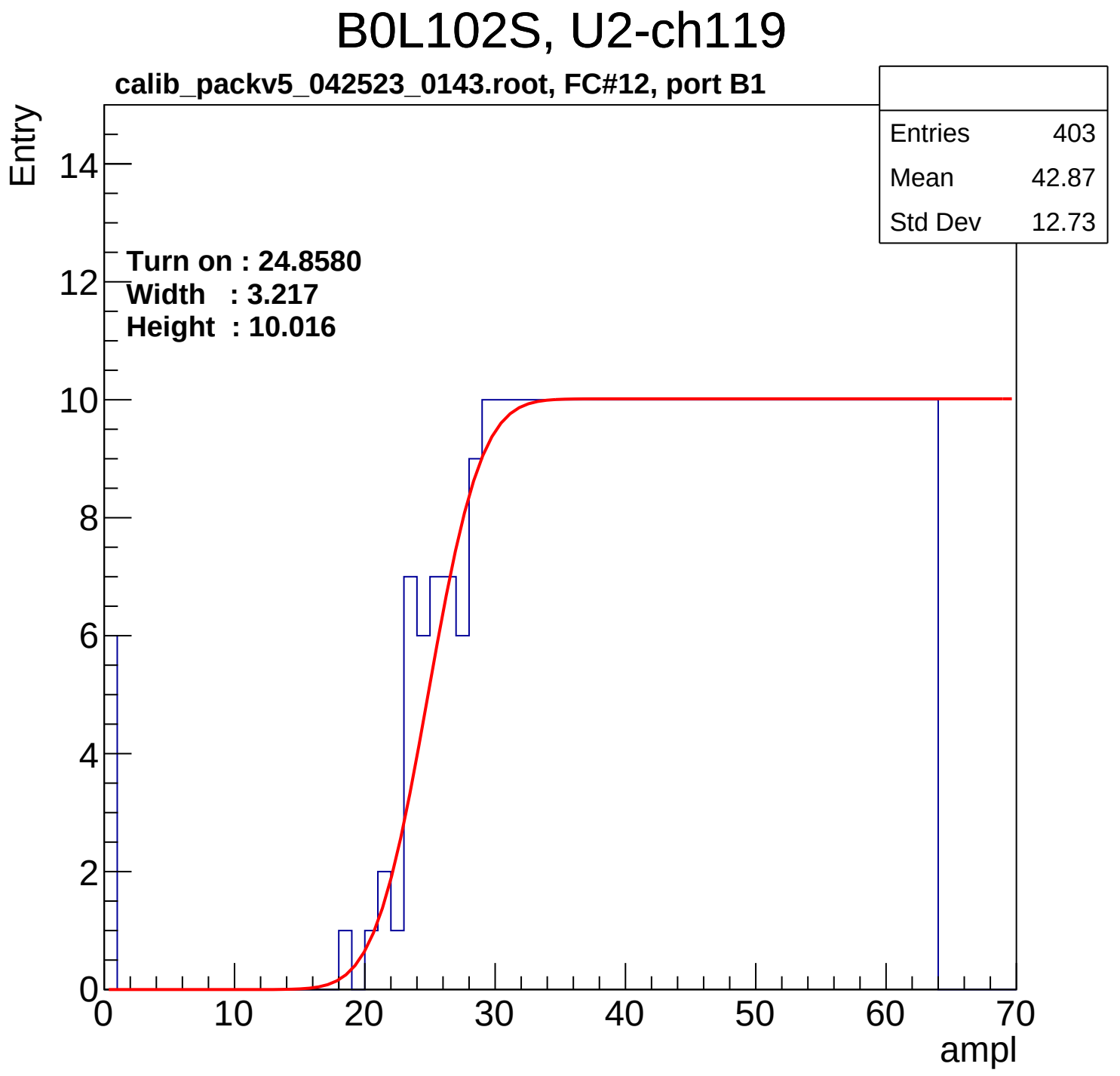
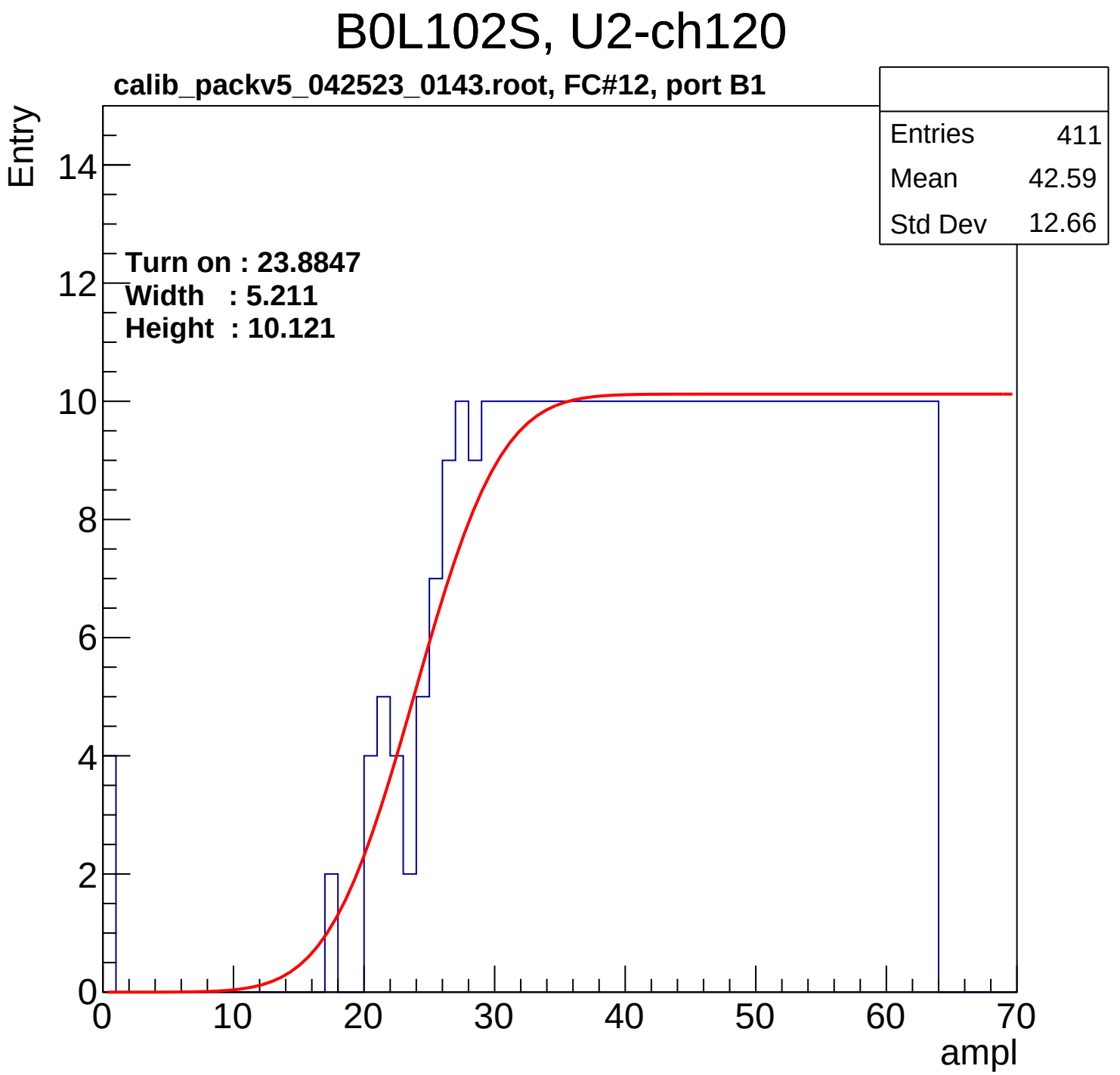

B0L102S, U2-ch119
calib_packv5_042523_0143.root, FC#12, port B1
Entries 403
Mean 42.87
Std Dev 12.73
Turn on : 24.8580
Width : 3.217
Height : 10.016
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L102S, U2-ch120
calib_packv5_042523_0143.root, FC#12, port B1
Entries 411
Mean 42.59
Std Dev 12.66
Turn on : 23.8847
Width : 5.211
Height : 10.121
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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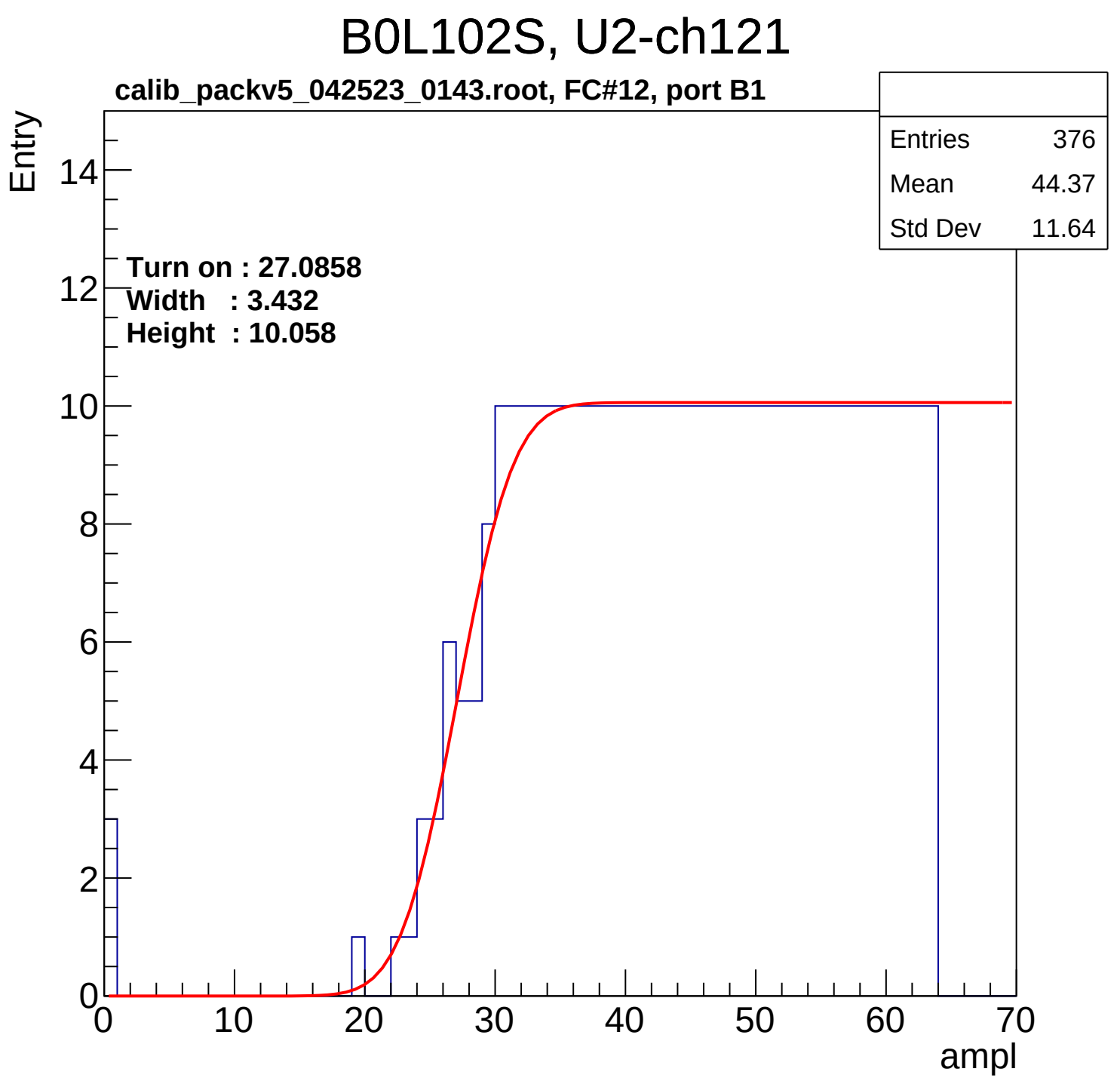
B0L102S, U2-ch121
calib_packv5_042523_0143.root, FC#12, port B1
Entries 376
Mean 44.37
Std Dev 11.64
Turn on : 27.0858
Width : 3.432
Height : 10.058
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
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60
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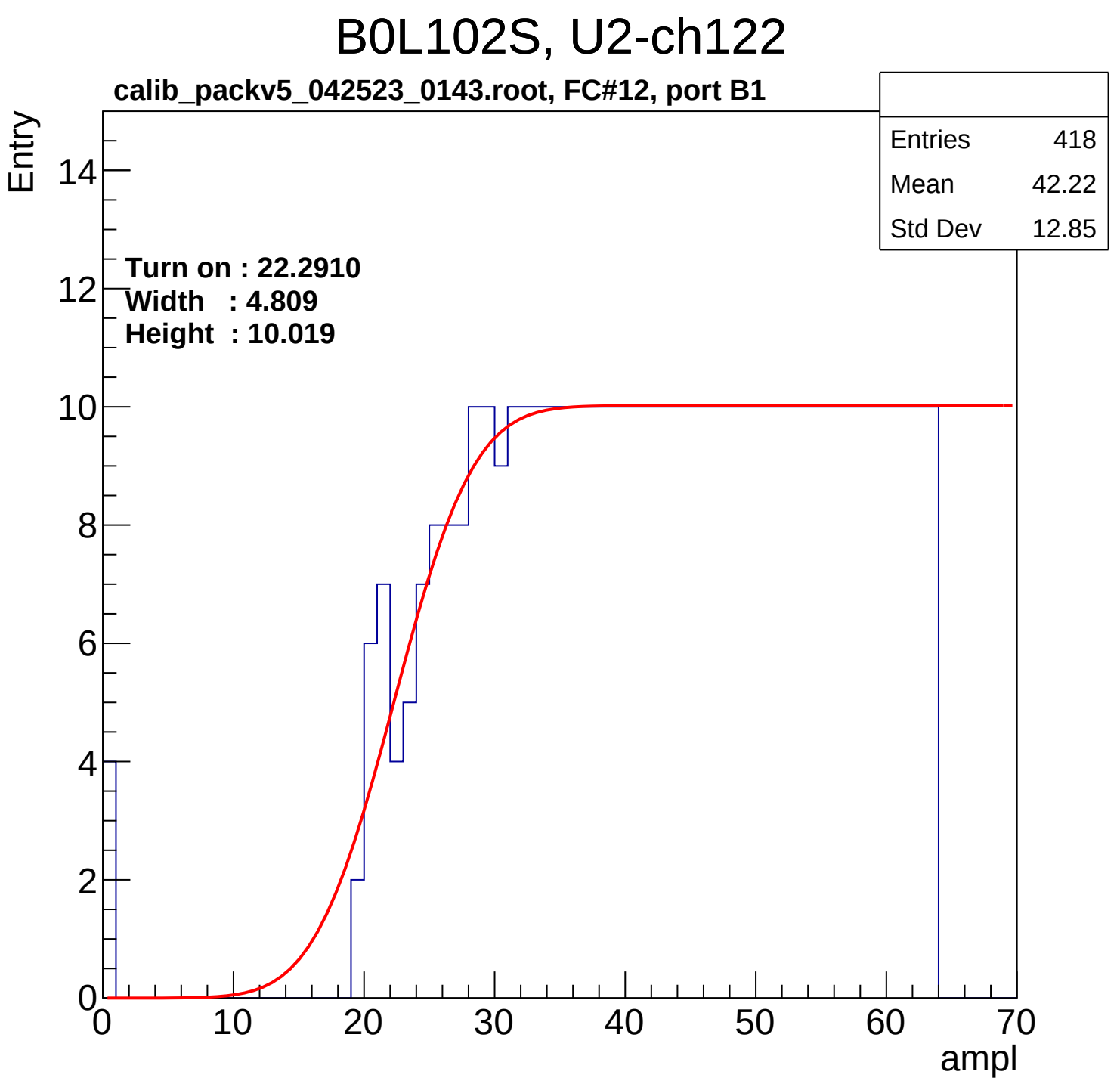
B0L102S, U2-ch122
calib_packv5_042523_0143.root, FC#12, port B1
Entries 418
Mean 42.22
Std Dev 12.85
Turn on : 22.2910
Width : 4.809
Height : 10.019
Entry
ampl
0
2
4
6
8
10
12
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0
10
20
30
40
50
60
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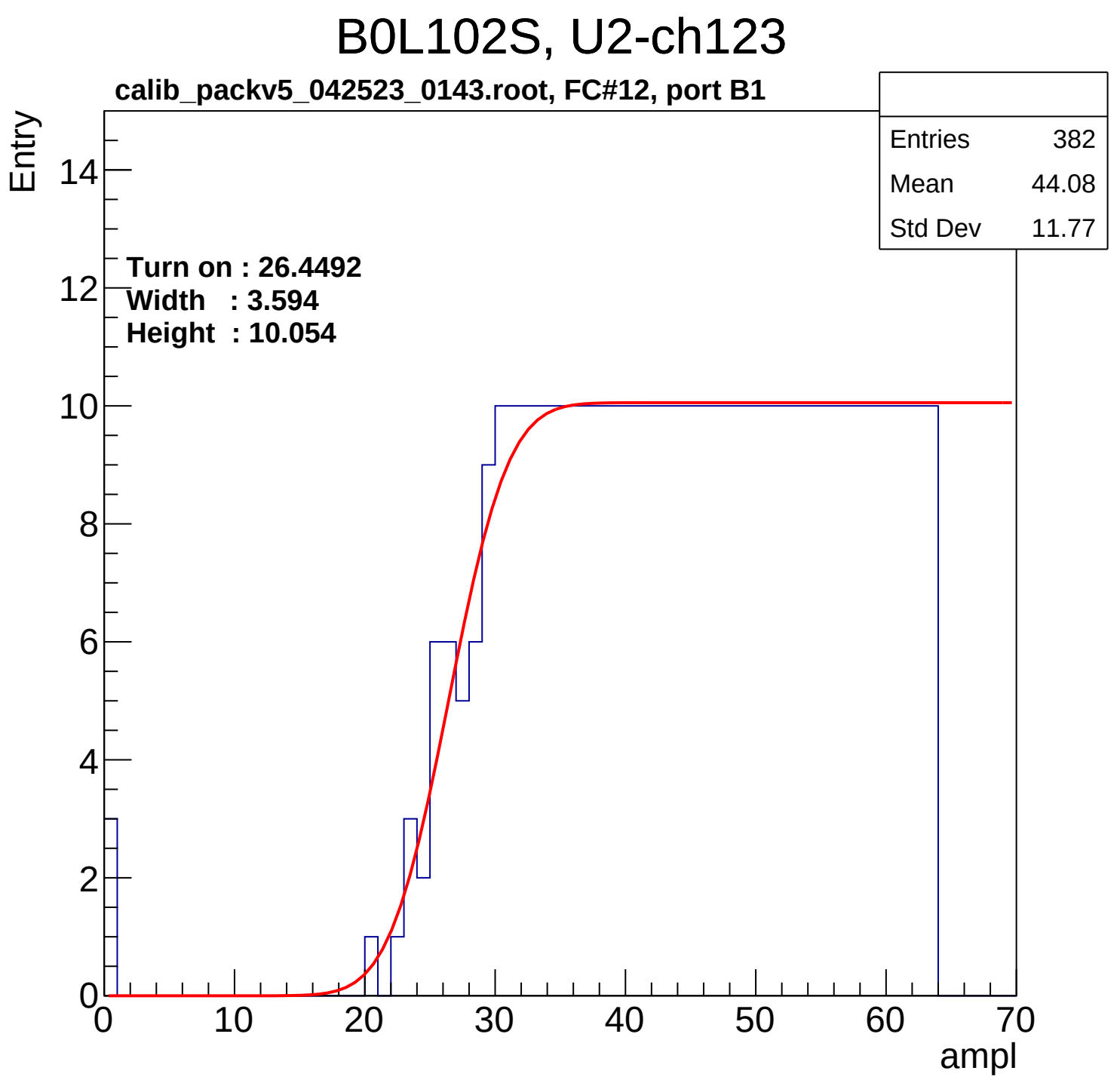
B0L102S, U2-ch123
calib_packv5_042523_0143.root, FC#12, port B1
Entries 382
Mean 44.08
Std Dev 11.77
Turn on : 26.4492
Width : 3.594
Height : 10.054
Entry
ampl
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2
4
6
8
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12
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0
10
20
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40
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60
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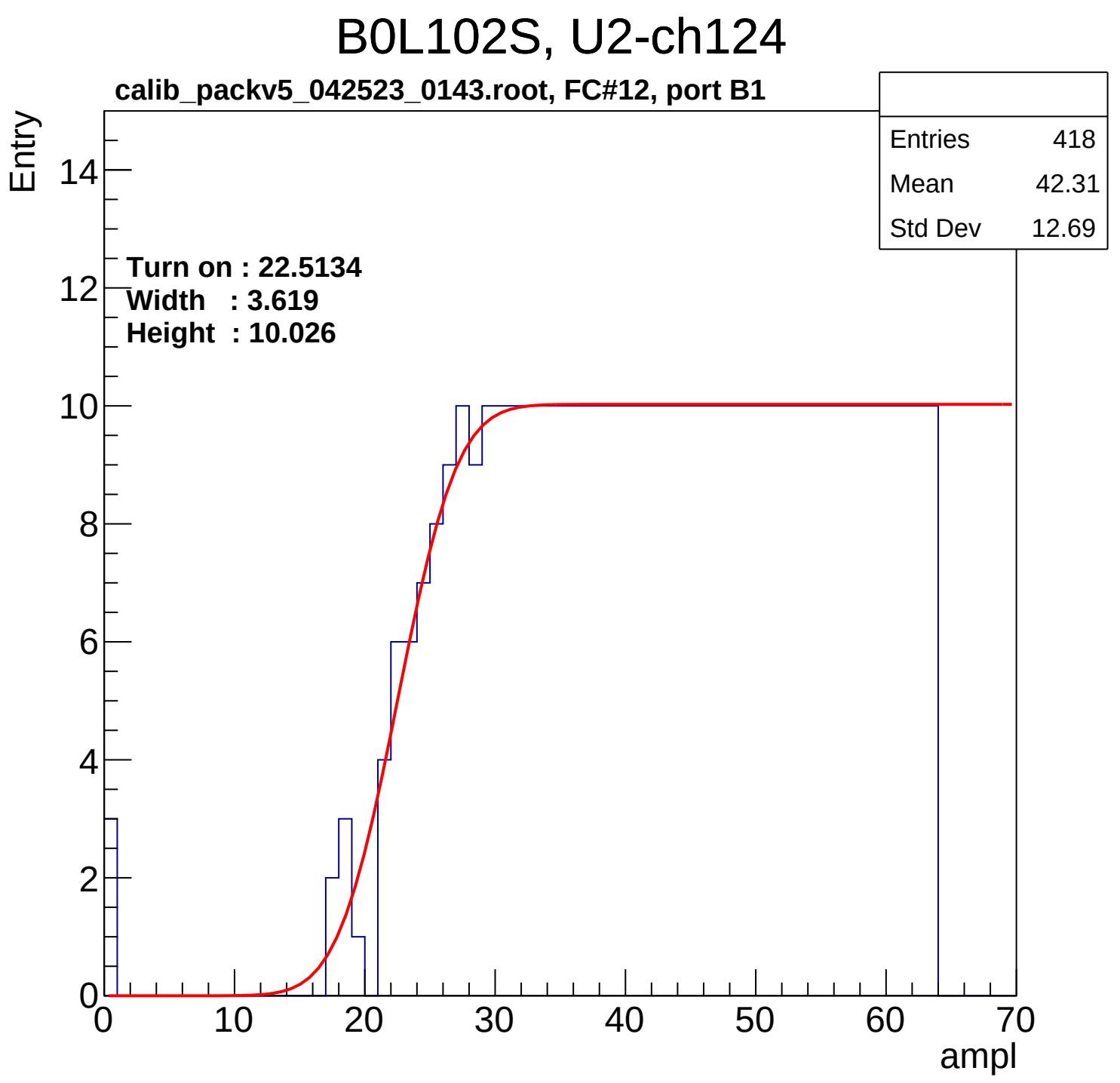
B0L102S, U2-ch124
calib_packv5_042523_0143.root, FC#12, port B1
Entries 418
Mean 42.31
Std Dev 12.69
Turn on : 22.5134
Width : 3.619
Height : 10.026
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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40
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60
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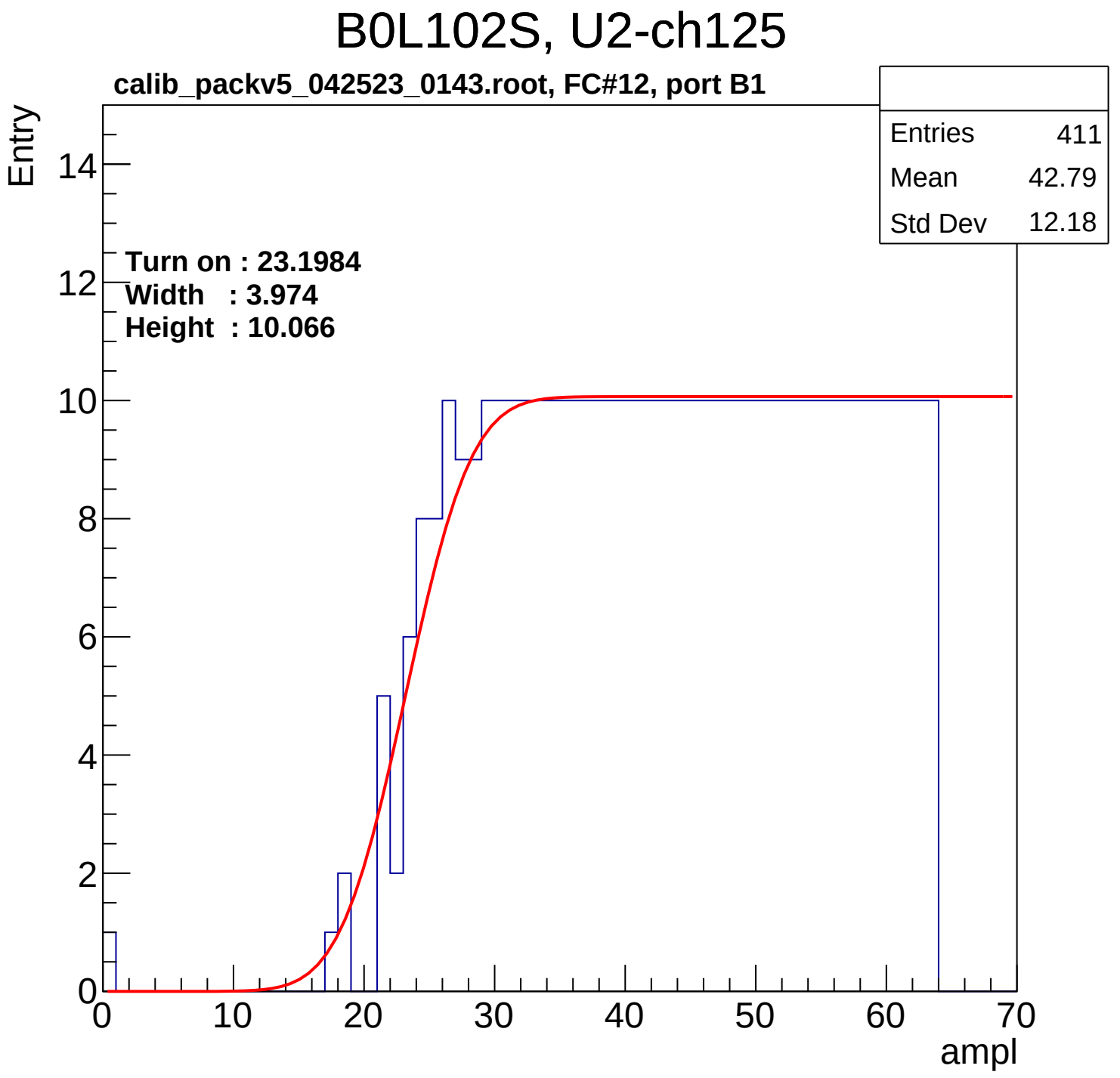
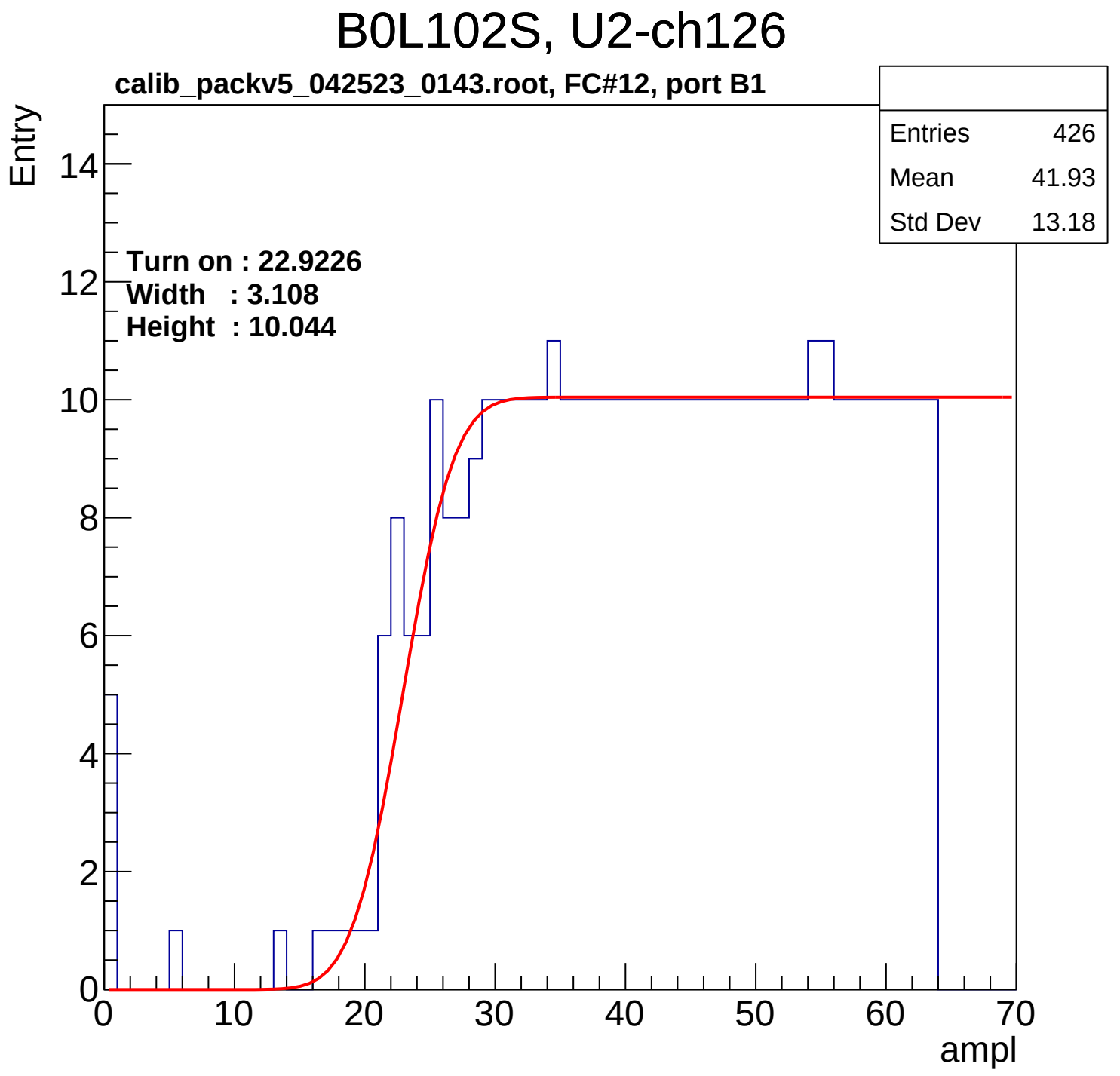

B0L102S, U2-ch125
calib_packv5_042523_0143.root, FC#12, port B1
Entries 411
Mean 42.79
Std Dev 12.18
Turn on : 23.1984
Width : 3.974
Height : 10.066
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L102S, U2-ch126
calib_packv5_042523_0143.root, FC#12, port B1
Entries 426
Mean 41.93
Std Dev 13.18
Turn on : 22.9226
Width : 3.108
Height : 10.044
Entry
ampl
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2
4
6
8
10
12
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0
10
20
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40
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60
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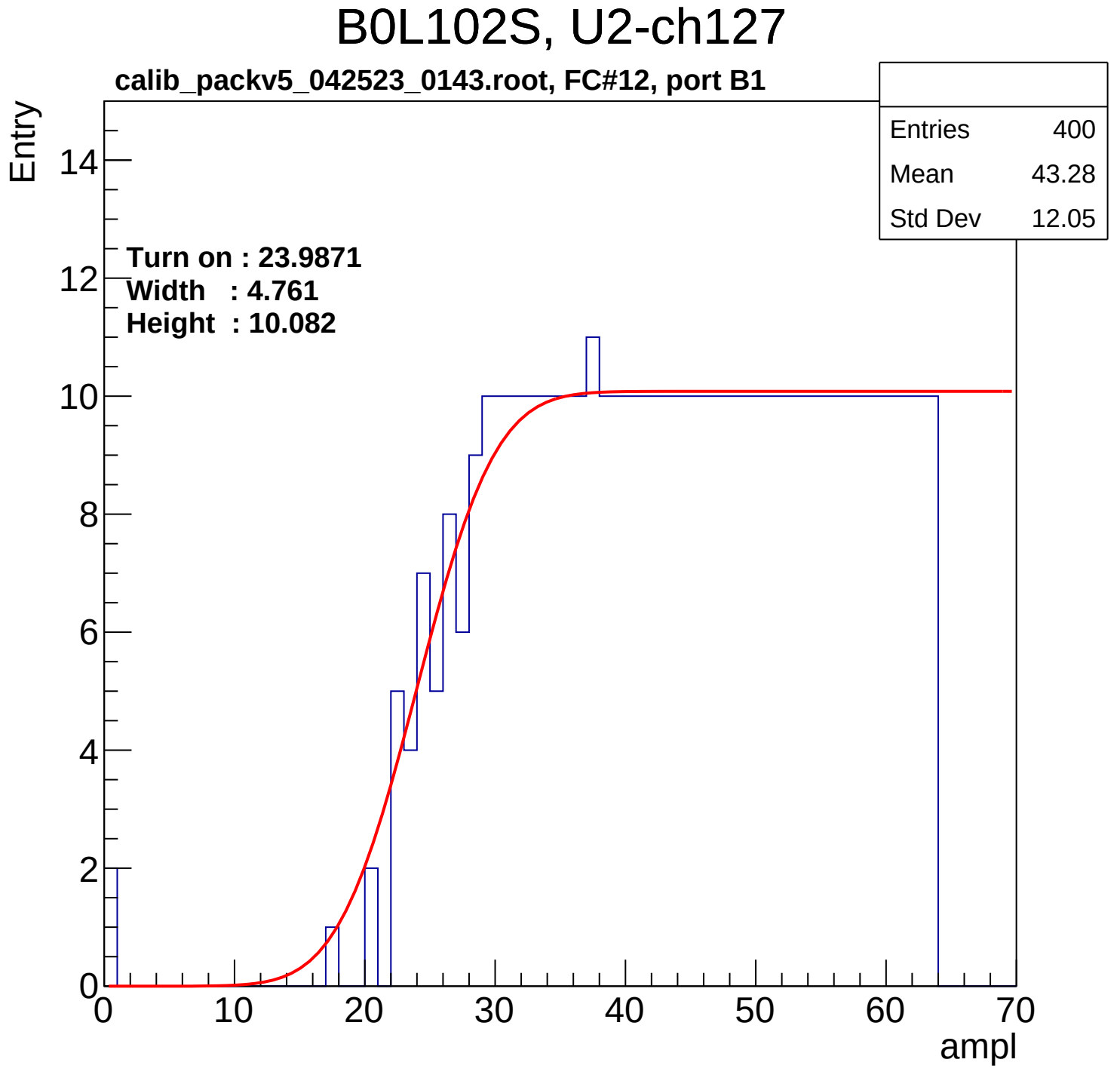
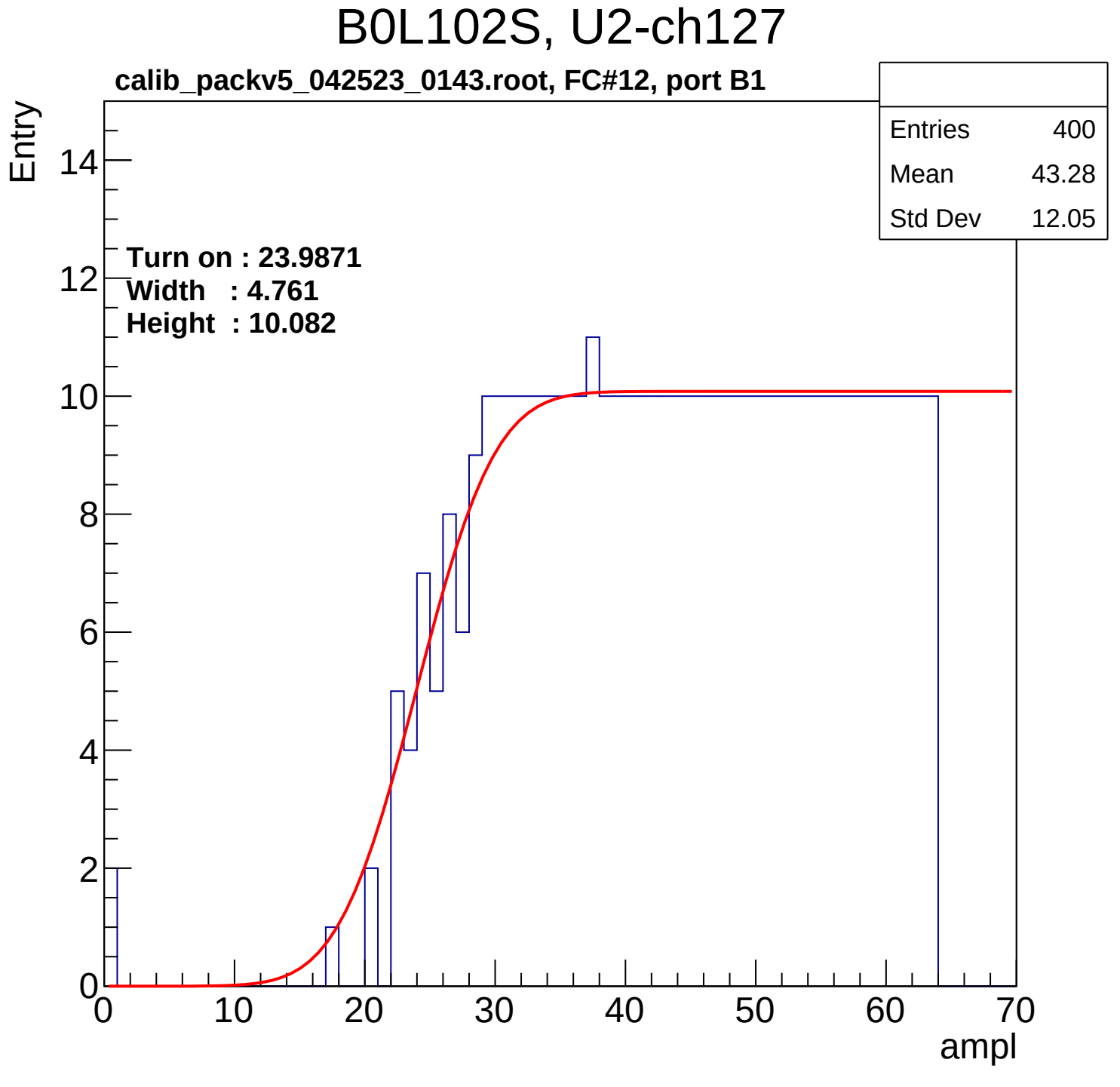

B0L102S, U2-ch127
calib_packv5_042523_0143.root, FC#12, port B1
Entries 400
Mean 43.28
Std Dev 12.05
Turn on : 23.9871
Width : 4.761
Height : 10.082
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B0L102S, U2-ch127
calib_packv5_042523_0143.root, FC#12, port B1
Entries 400
Mean 43.28
Std Dev 12.05
Turn on : 23.9871
Width : 4.761
Height : 10.082
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70