



# B1L103S, U26-ch0, adc0

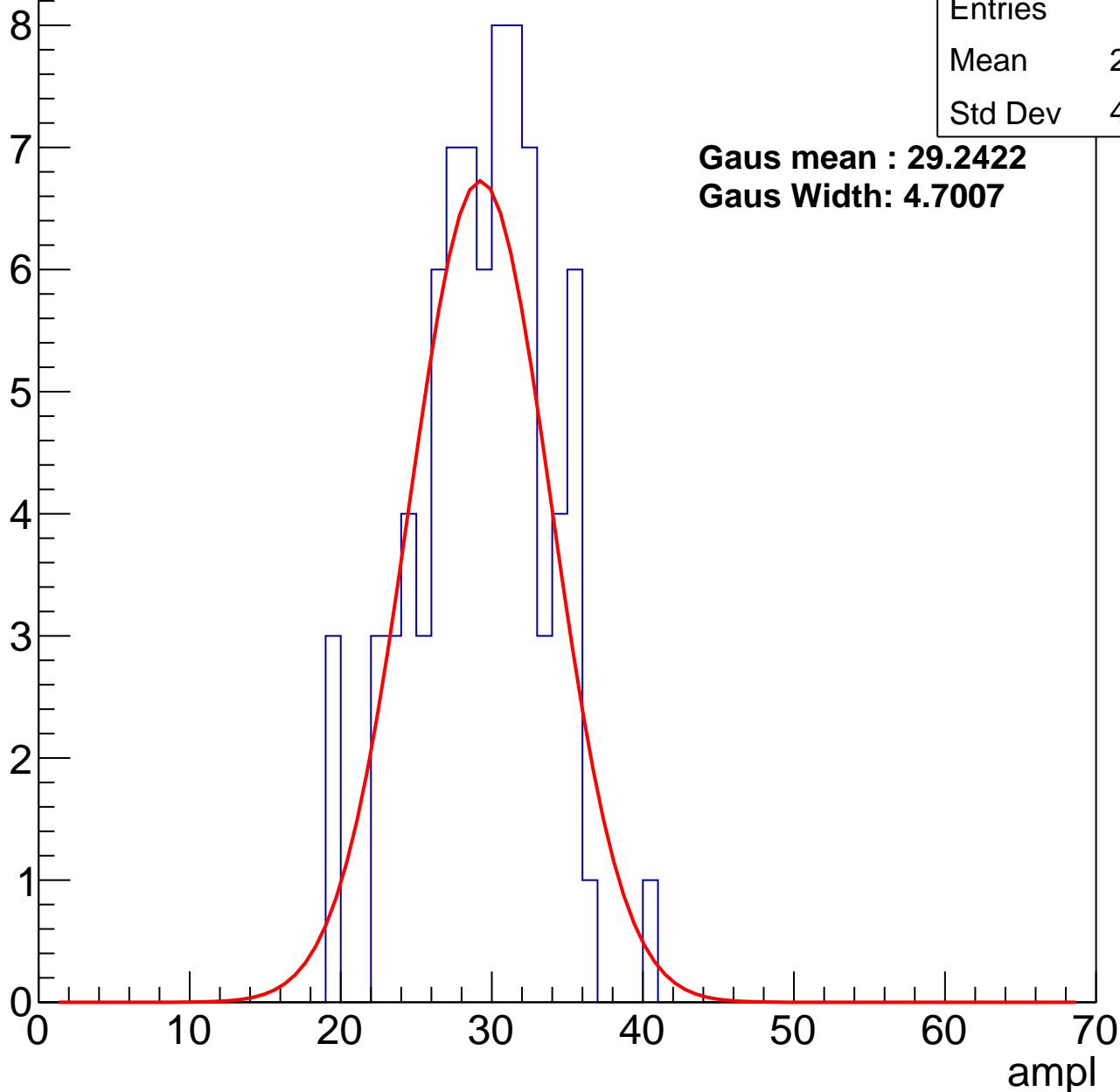
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	28.89
Std Dev	4.225

**Gaus mean : 29.2422**

**Gaus Width: 4.7007**



# B1L103S, U26-ch0, adc1

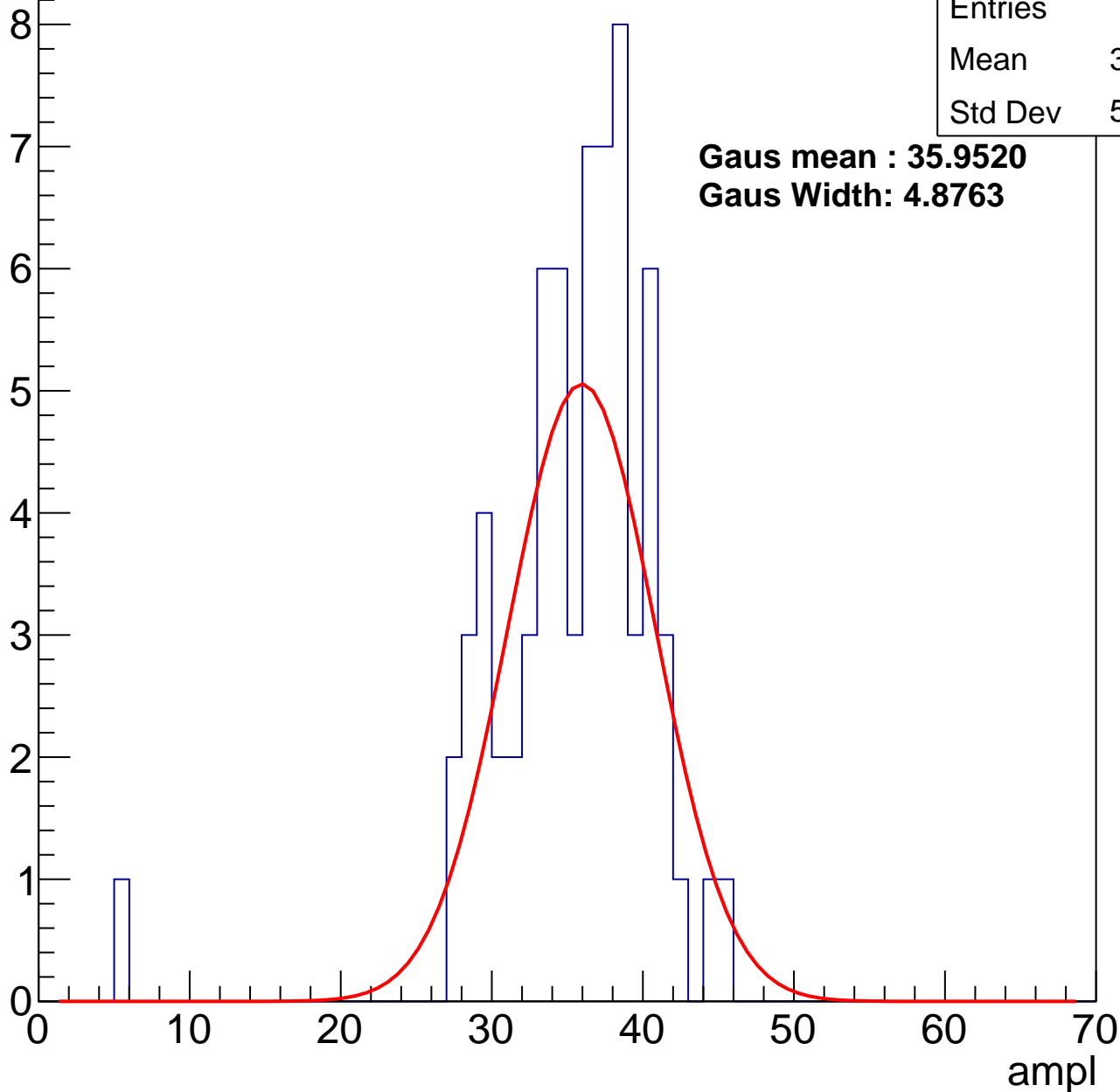
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	34.93
Std Dev	5.518

**Gaus mean : 35.9520**

**Gaus Width: 4.8763**



# B1L103S, U26-ch0, adc2

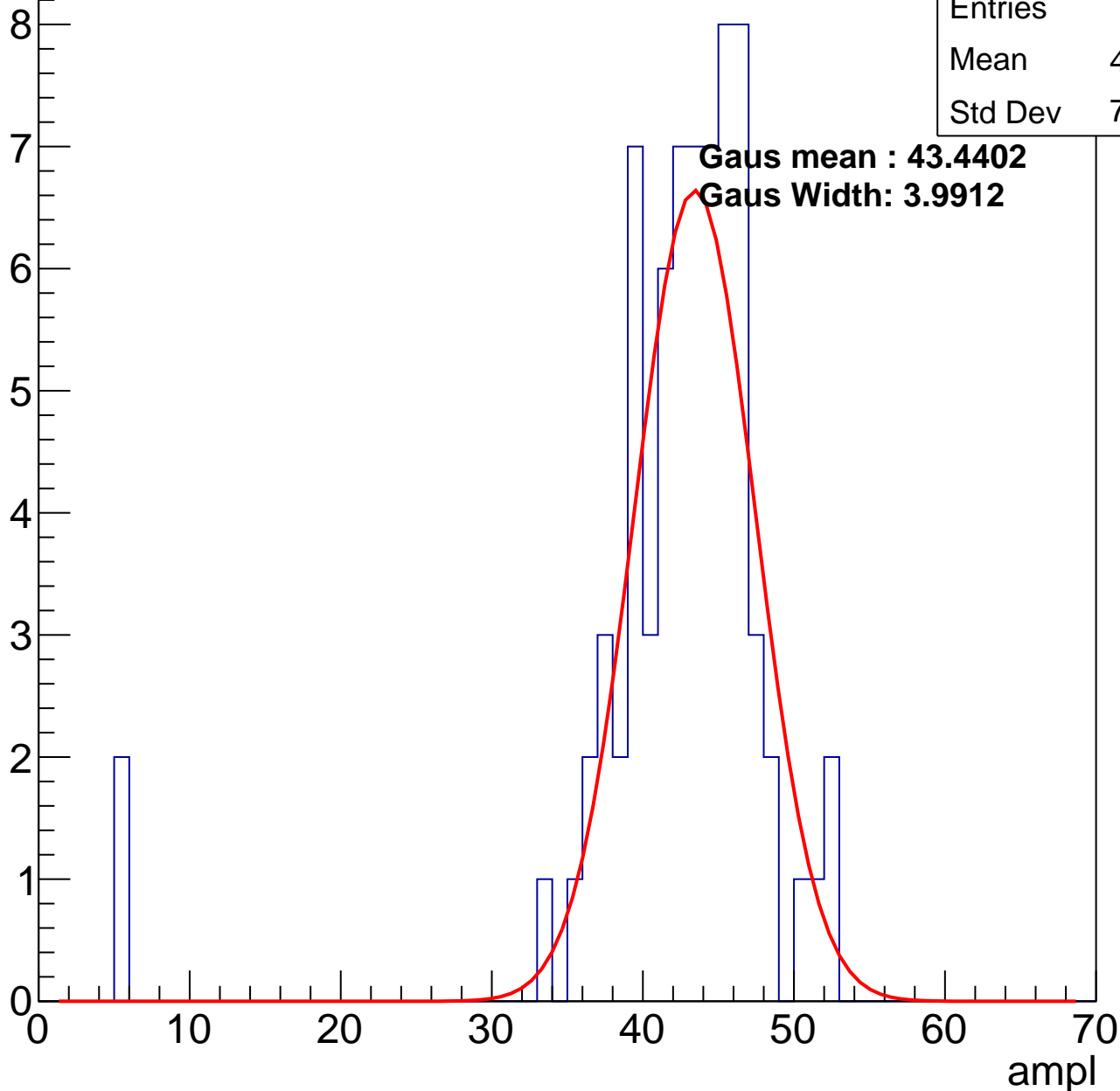
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	41.77
Std Dev	7.263

**Gaus mean : 43.4402**

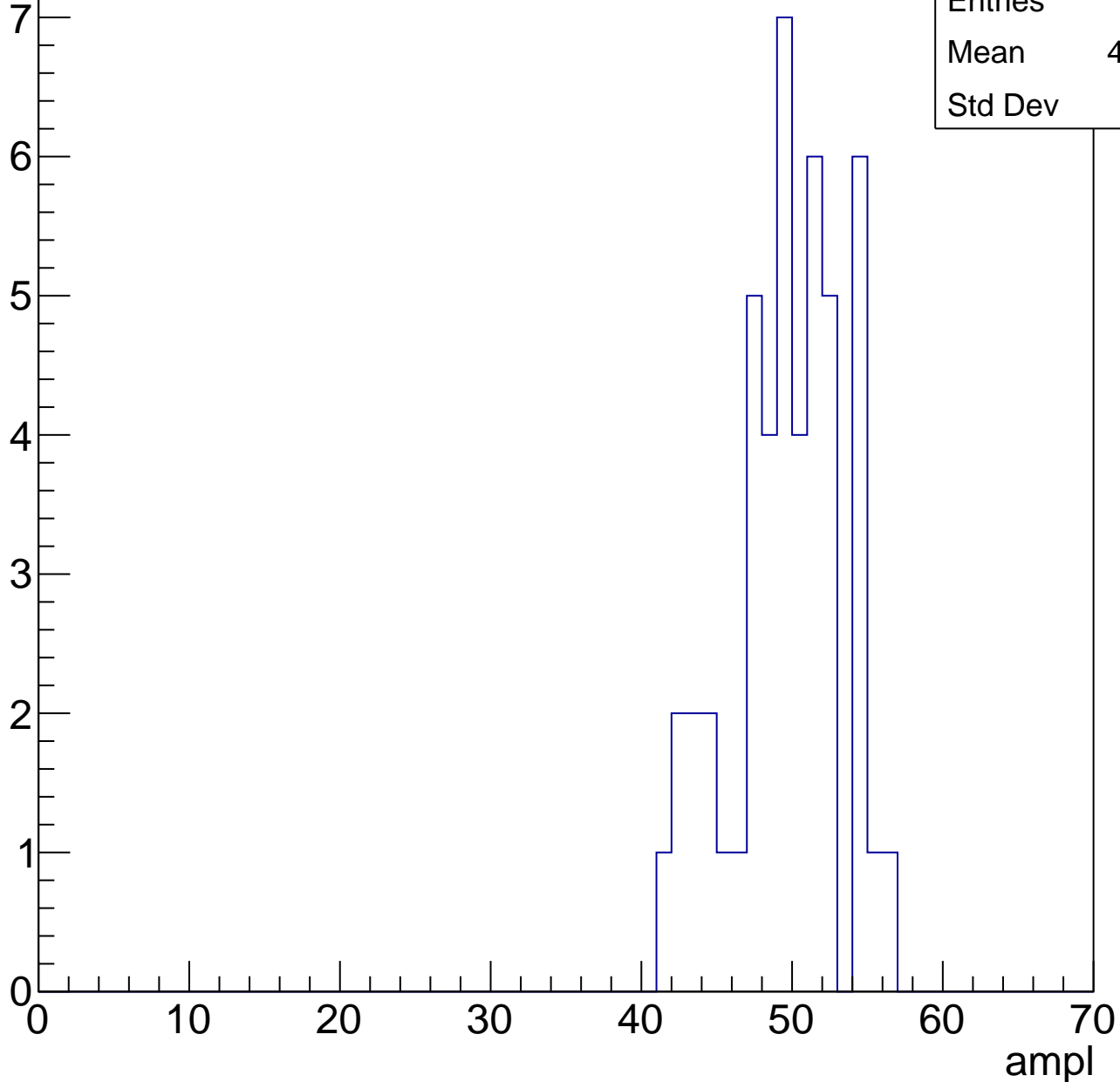
**Gaus Width: 3.9912**



# B1L103S, U26-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

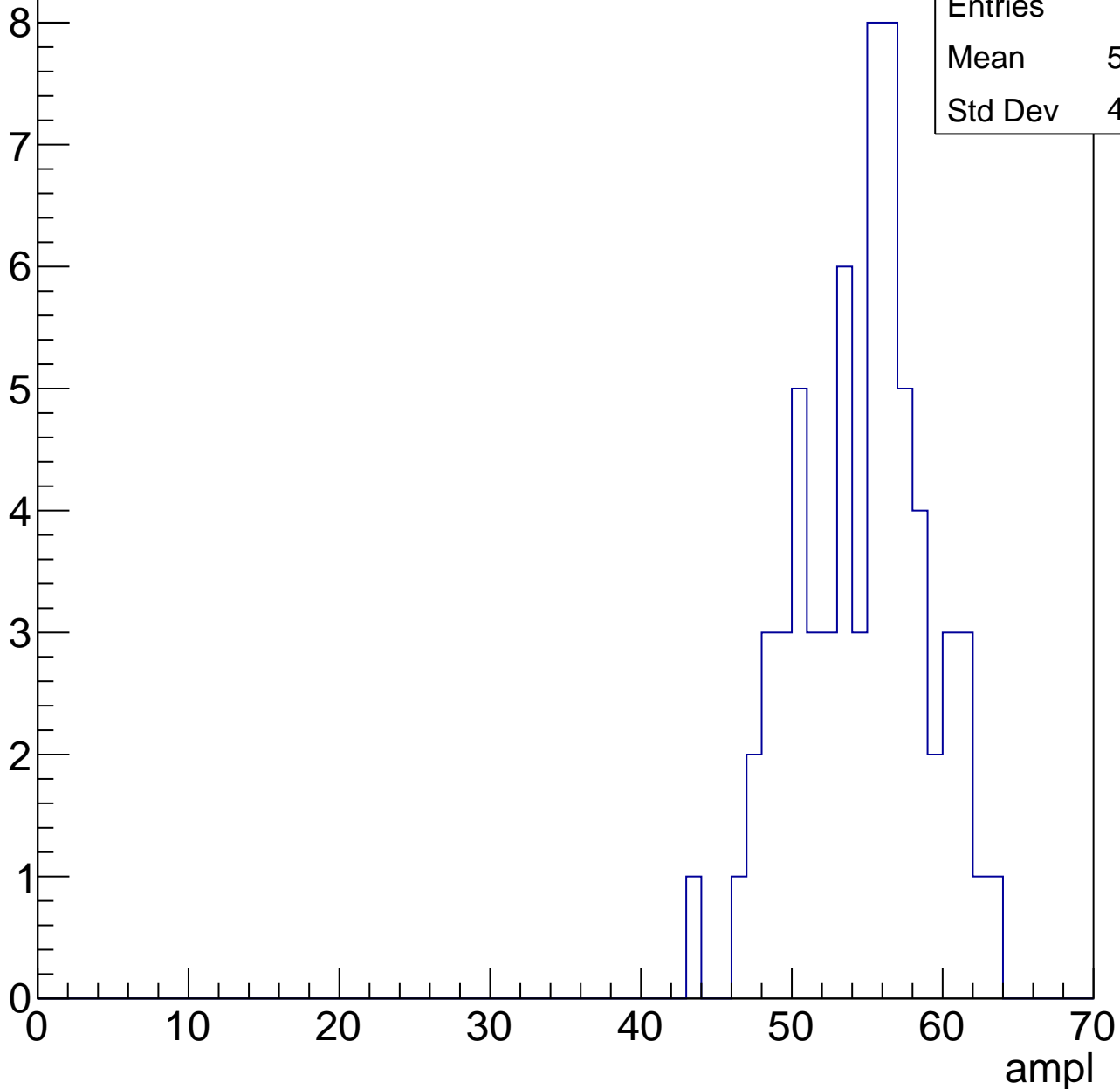


# B1L103S, U26-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	54.22
Std Dev	4.273

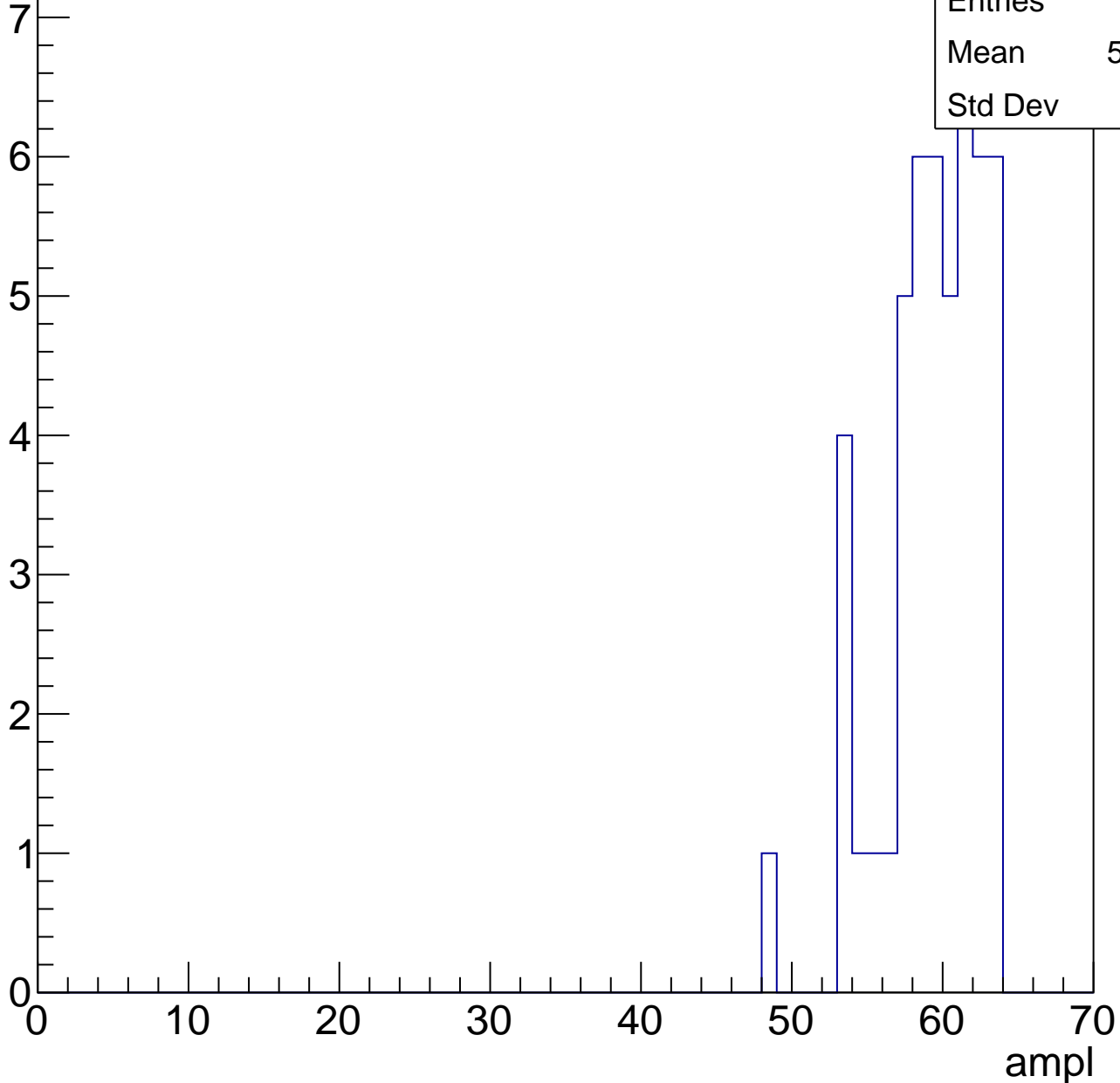


# B1L103S, U26-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	58.96
Std Dev	3.27



# B1L103S, U26-ch0, adc6

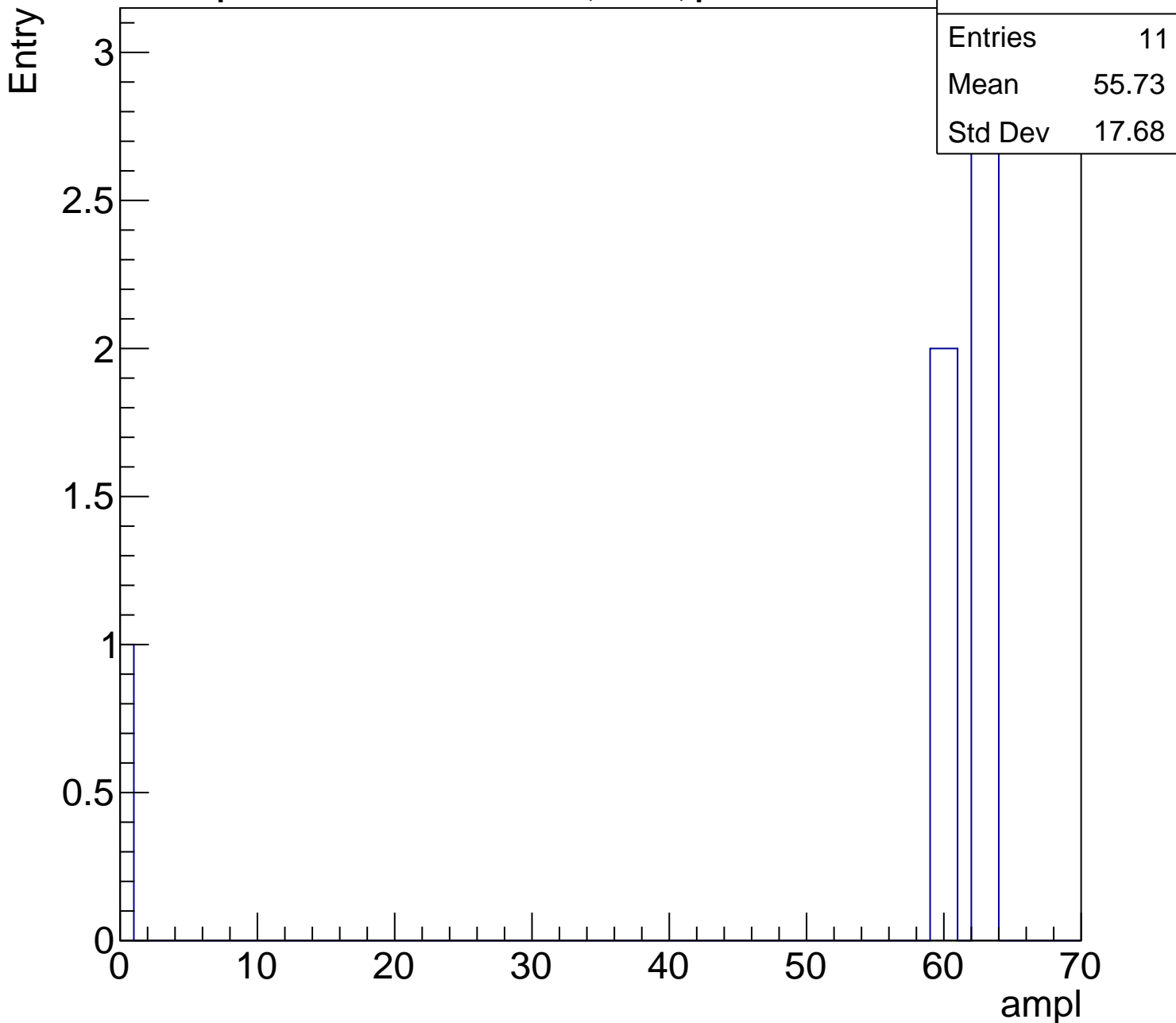
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	11
Mean	55.73
Std Dev	17.68

ampl





# B1L103S, U26-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch1, adc0

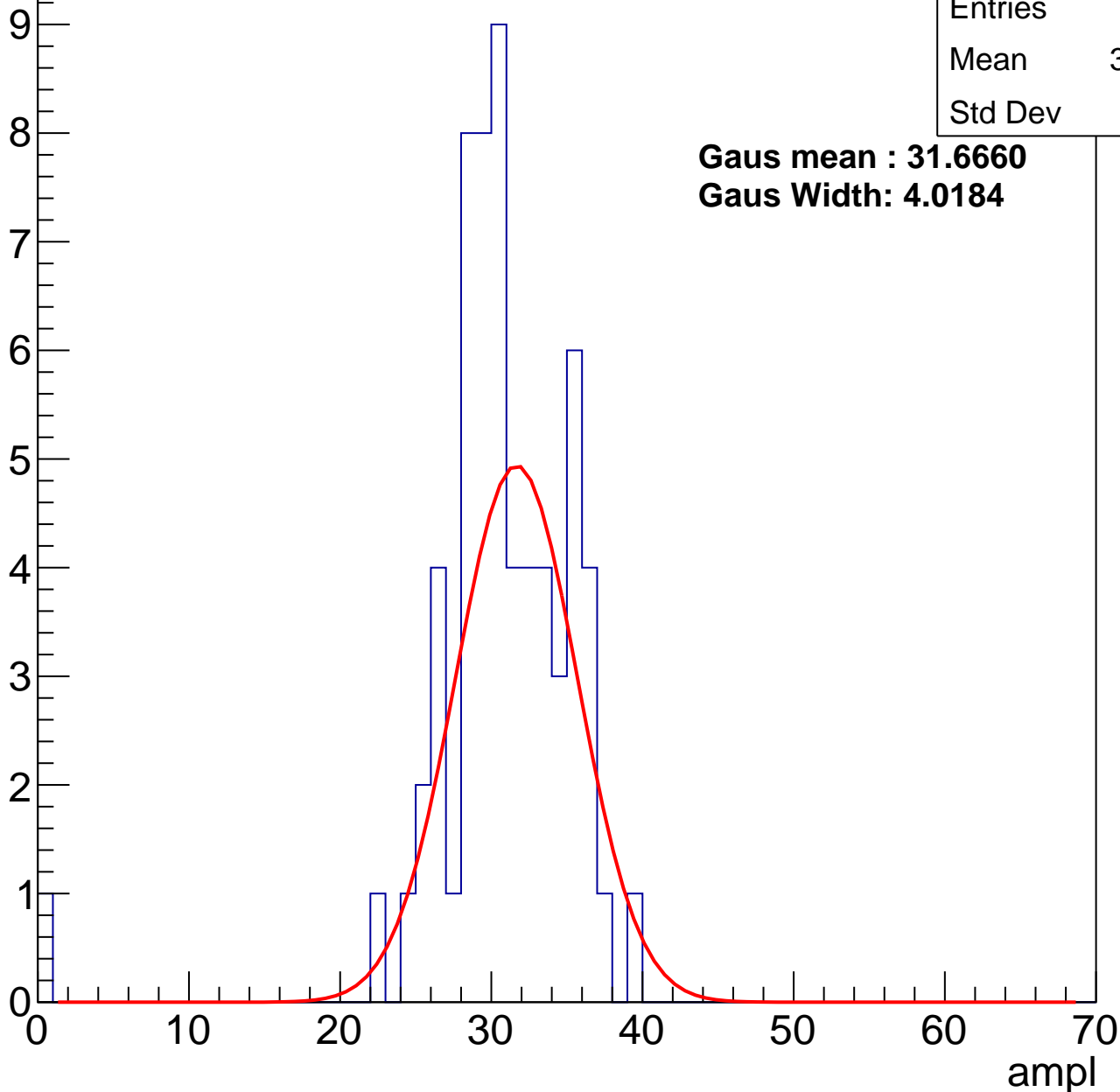
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	30.15
Std Dev	5.22

**Gaus mean : 31.6660**

**Gaus Width: 4.0184**



# B1L103S, U26-ch1, adc1

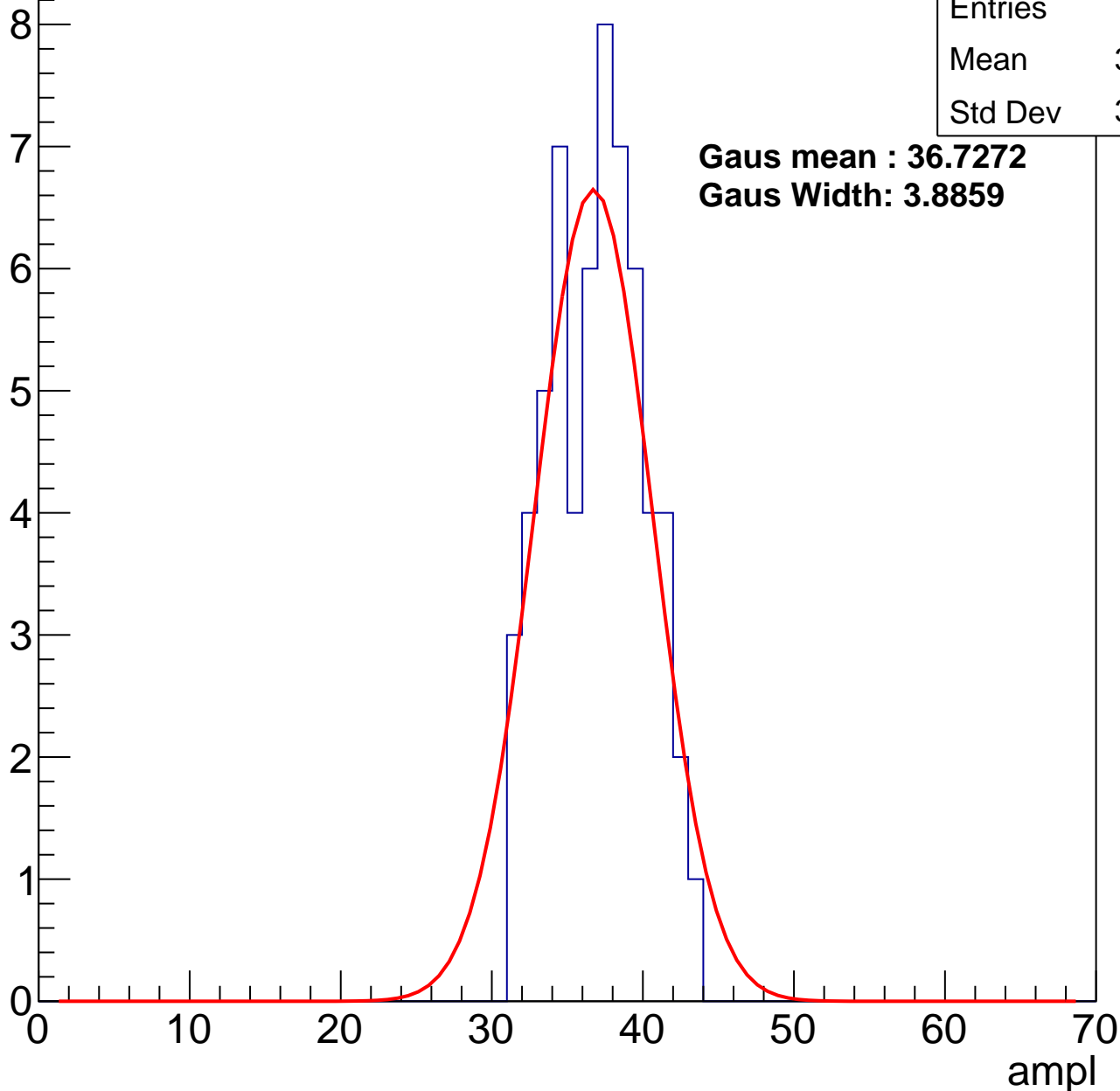
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	36.51
Std Dev	3.071

**Gaus mean : 36.7272**

**Gaus Width: 3.8859**



# B1L103S, U26-ch1, adc2

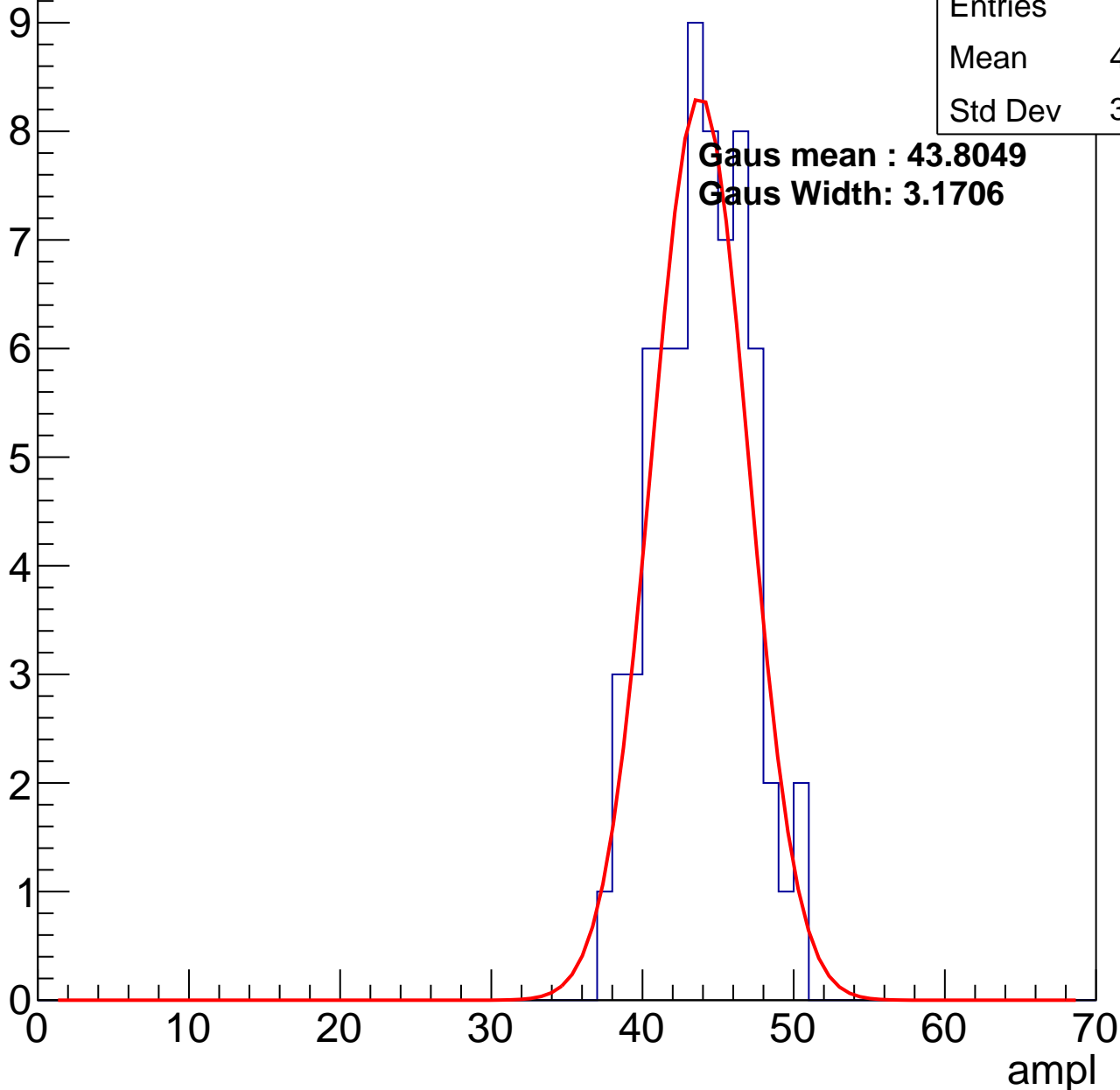
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	43.46
Std Dev	3.012

**Gaus mean : 43.8049**

**Gaus Width: 3.1706**

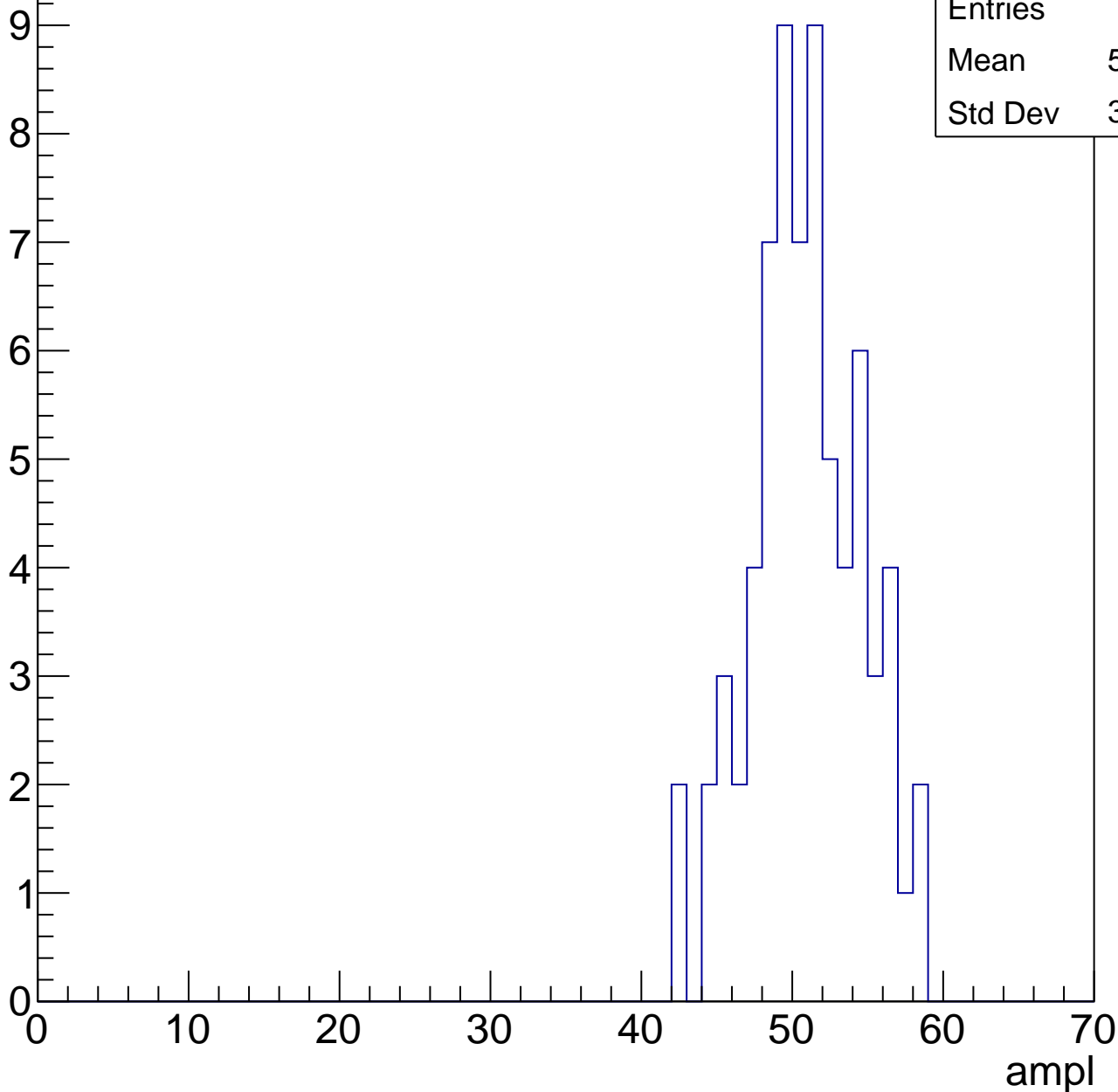


# B1L103S, U26-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	50.44
Std Dev	3.632

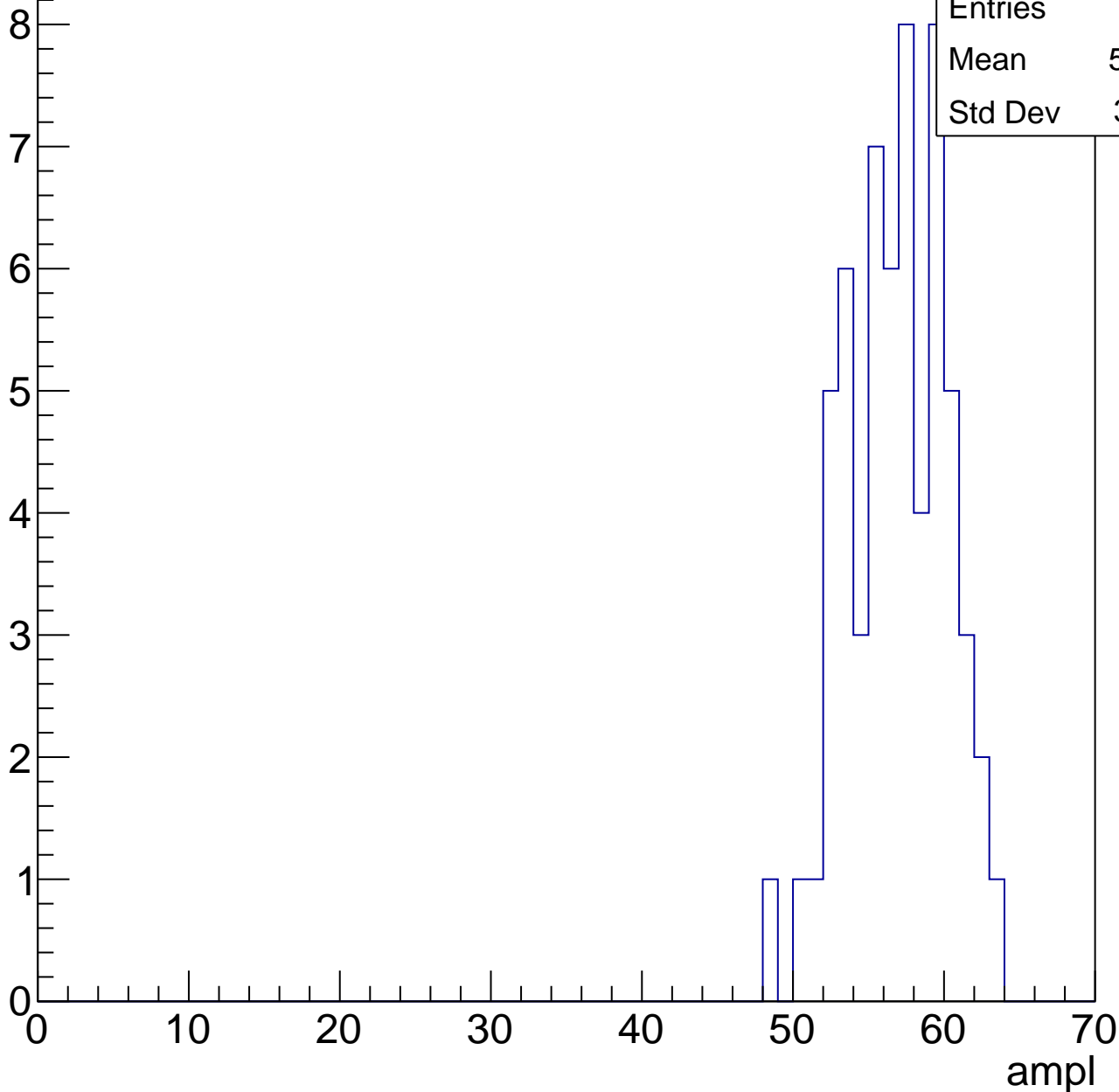


# B1L103S, U26-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	56.39
Std Dev	3.241

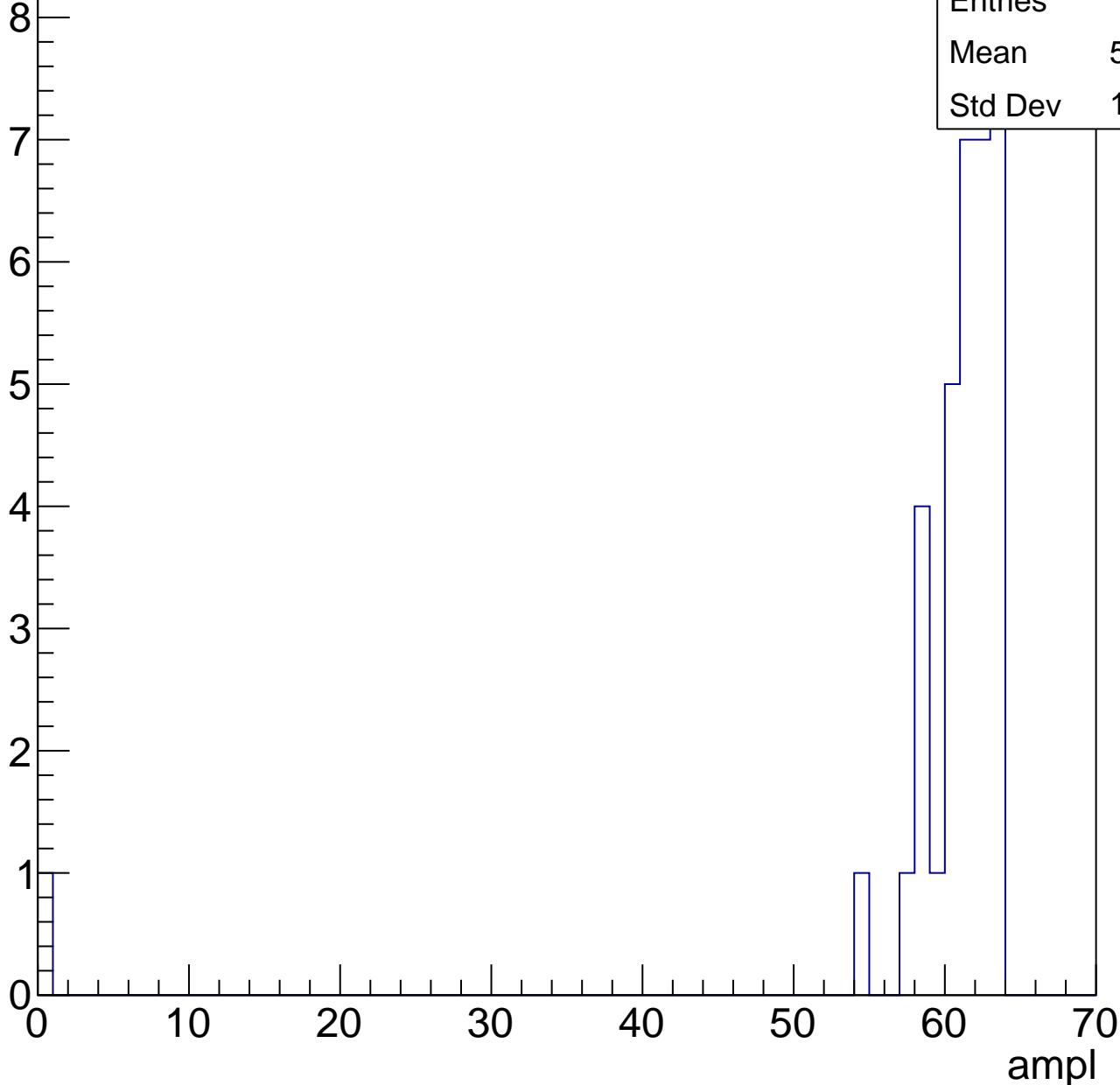


# B1L103S, U26-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	35
Mean	59.06
Std Dev	10.33



# B1L103S, U26-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U26-ch2, adc0

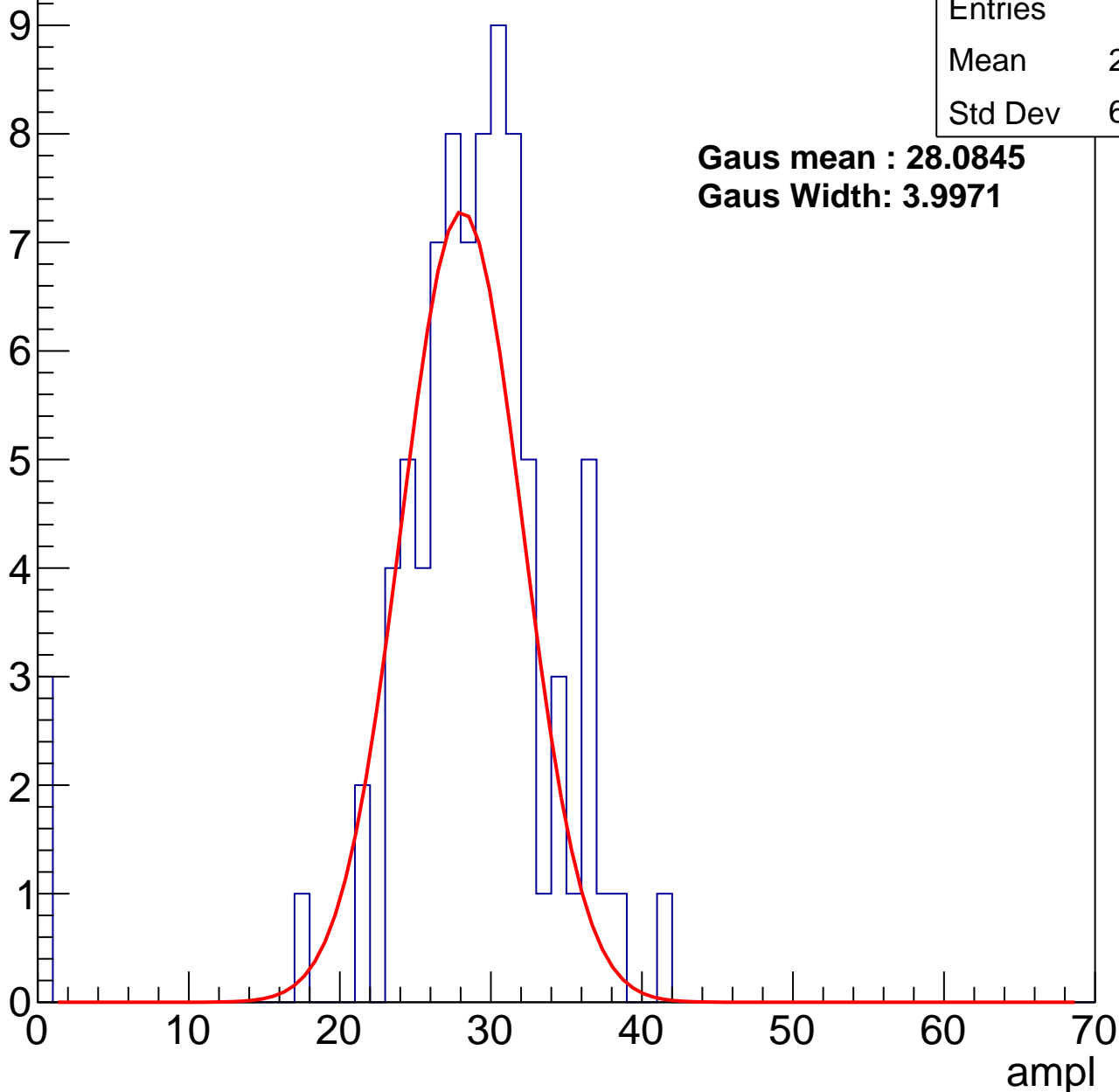
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	84
Mean	27.87
Std Dev	6.787

**Gaus mean : 28.0845**

**Gaus Width: 3.9971**



# B1L103S, U26-ch2, adc1

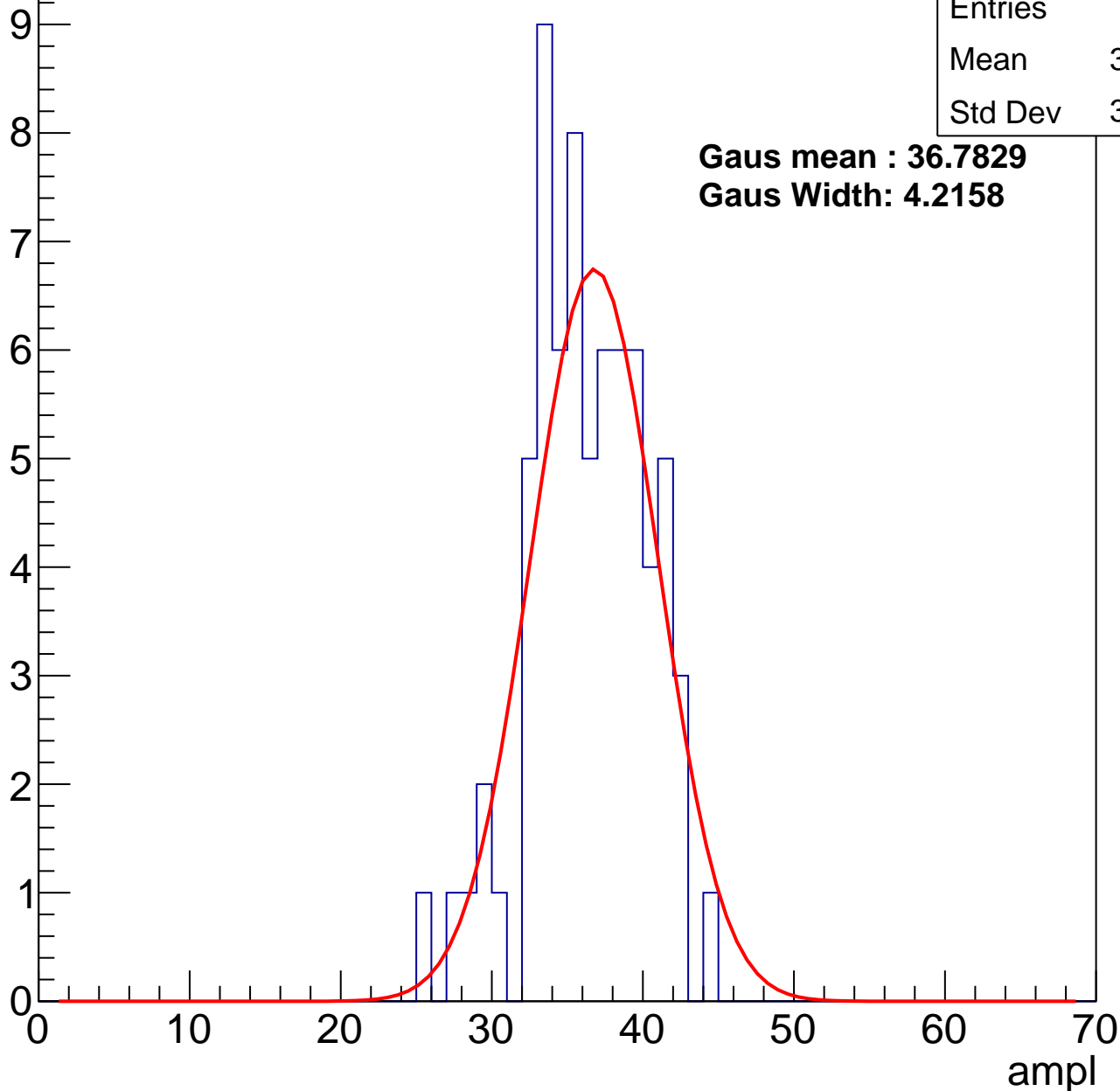
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	35.83
Std Dev	3.847

**Gaus mean : 36.7829**

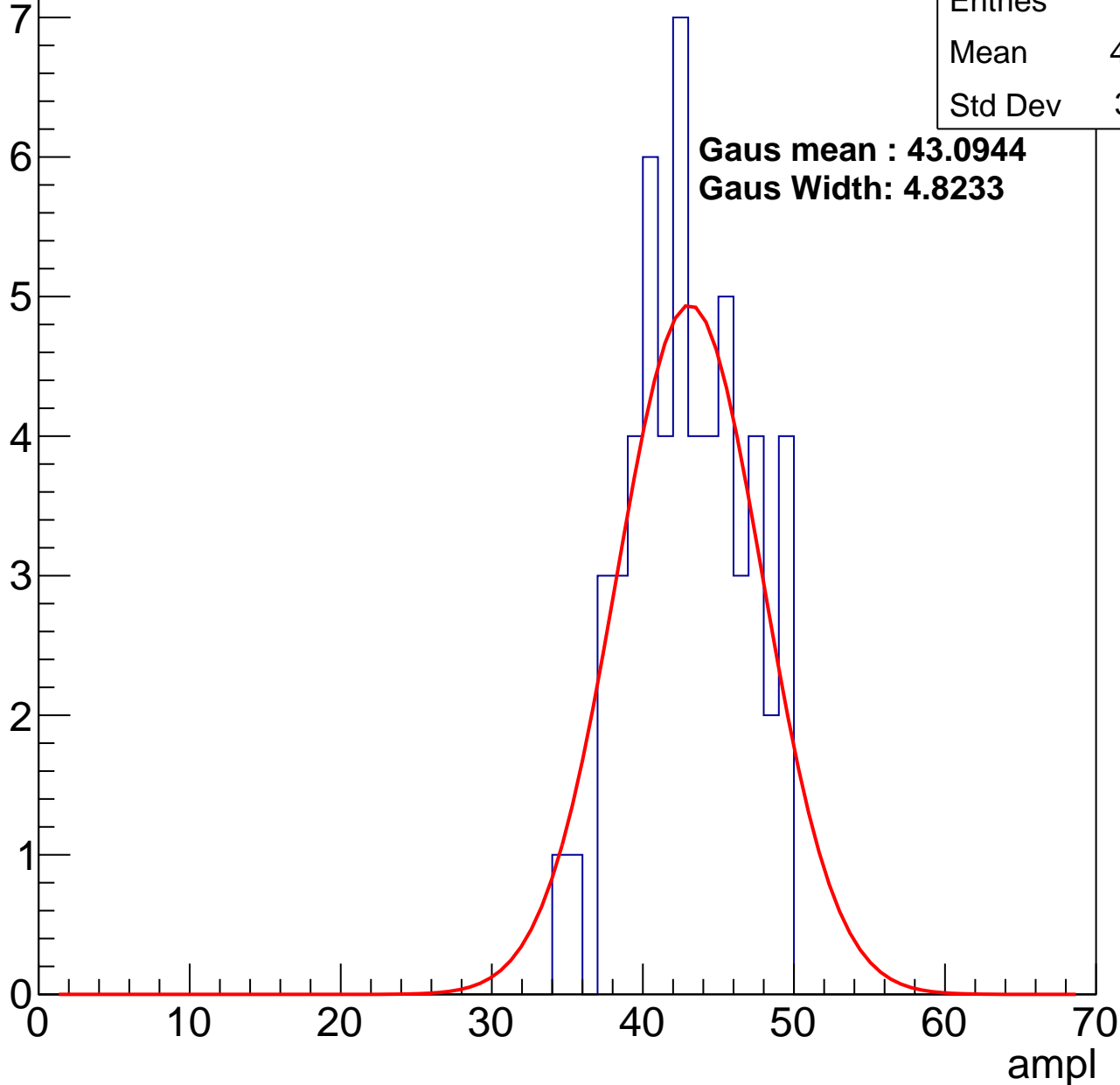
**Gaus Width: 4.2158**



# B1L103S, U26-ch2, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

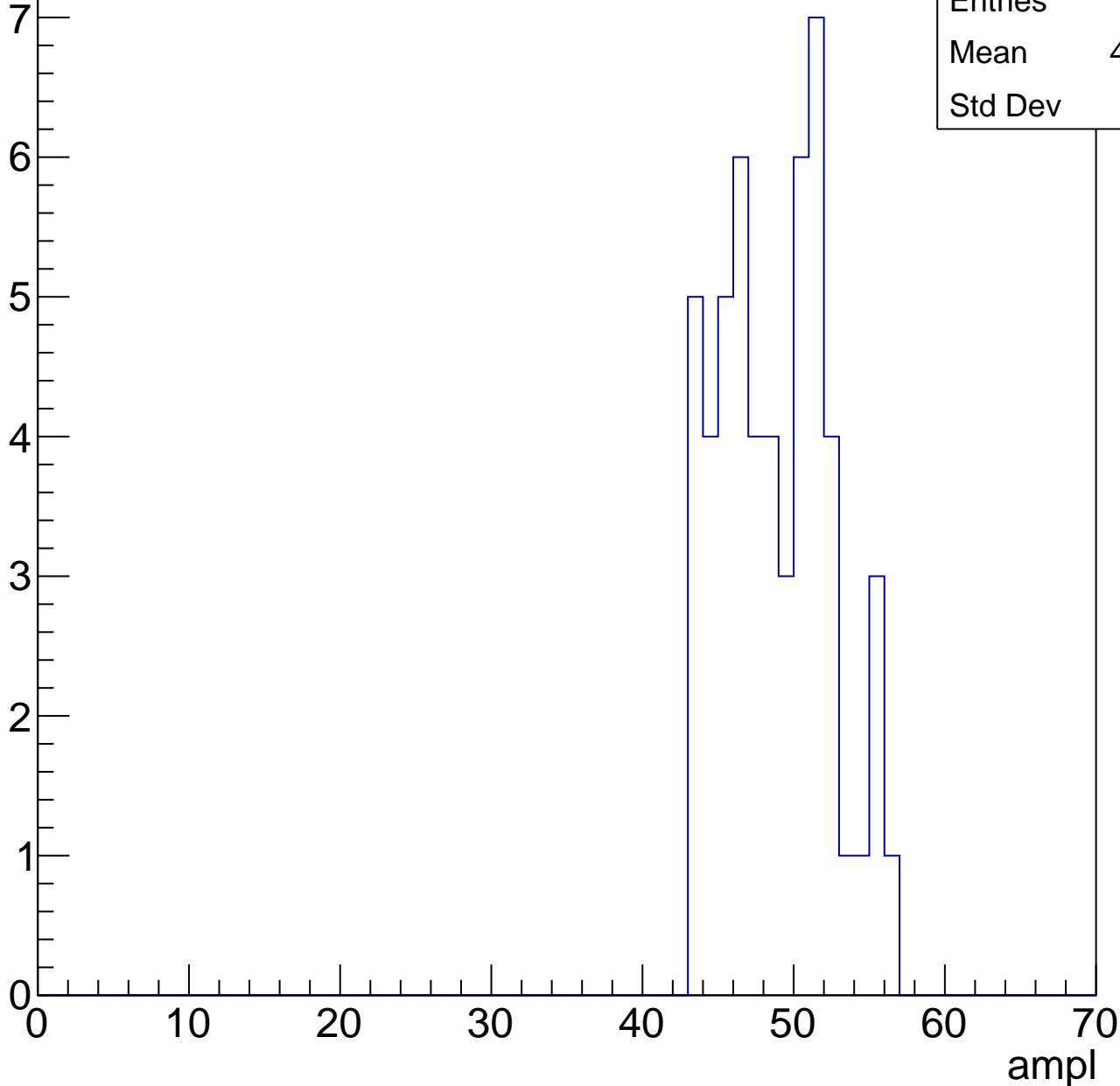


# B1L103S, U26-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	48.37
Std Dev	3.55

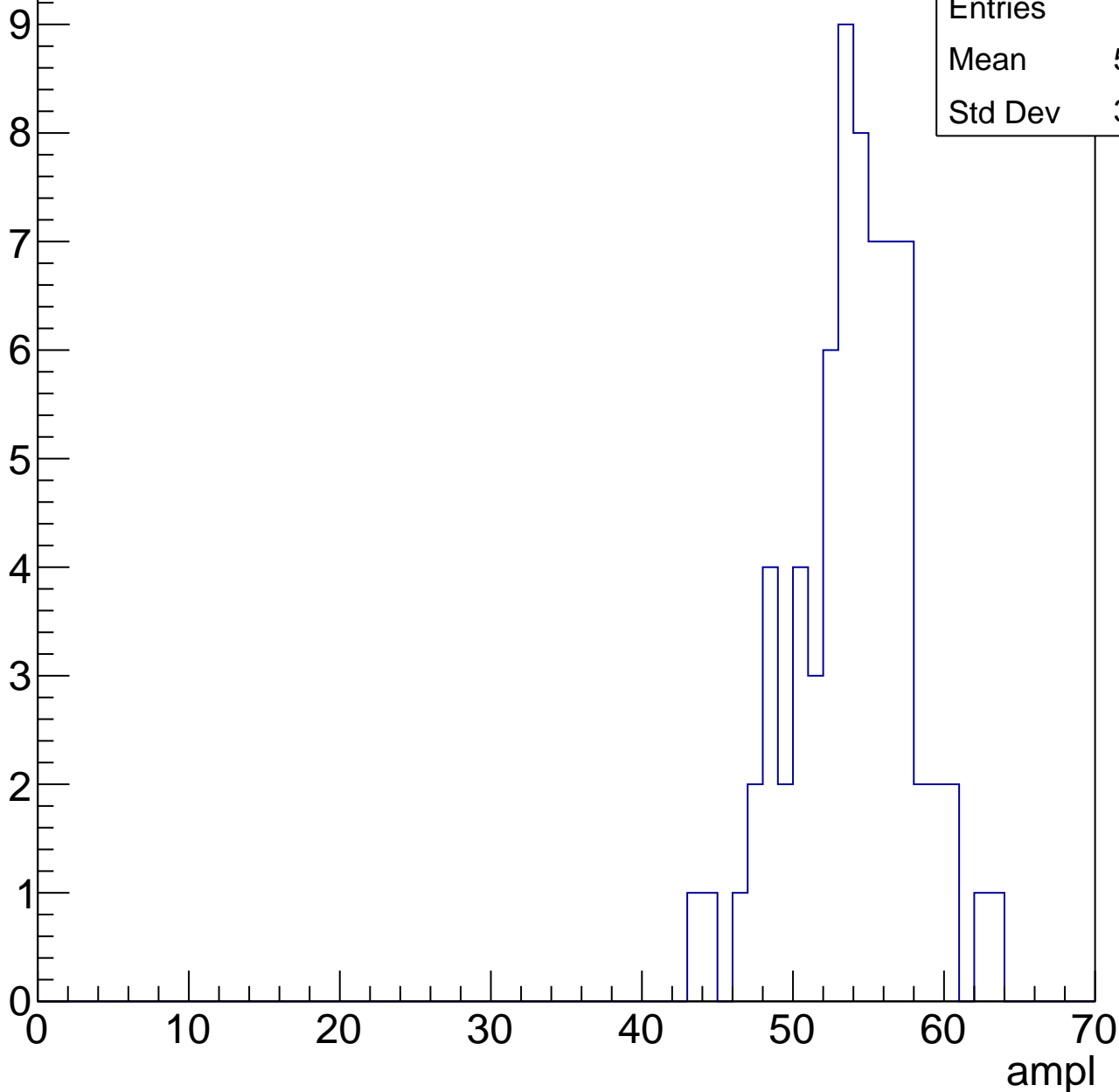


# B1L103S, U26-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	53.51
Std Dev	3.931

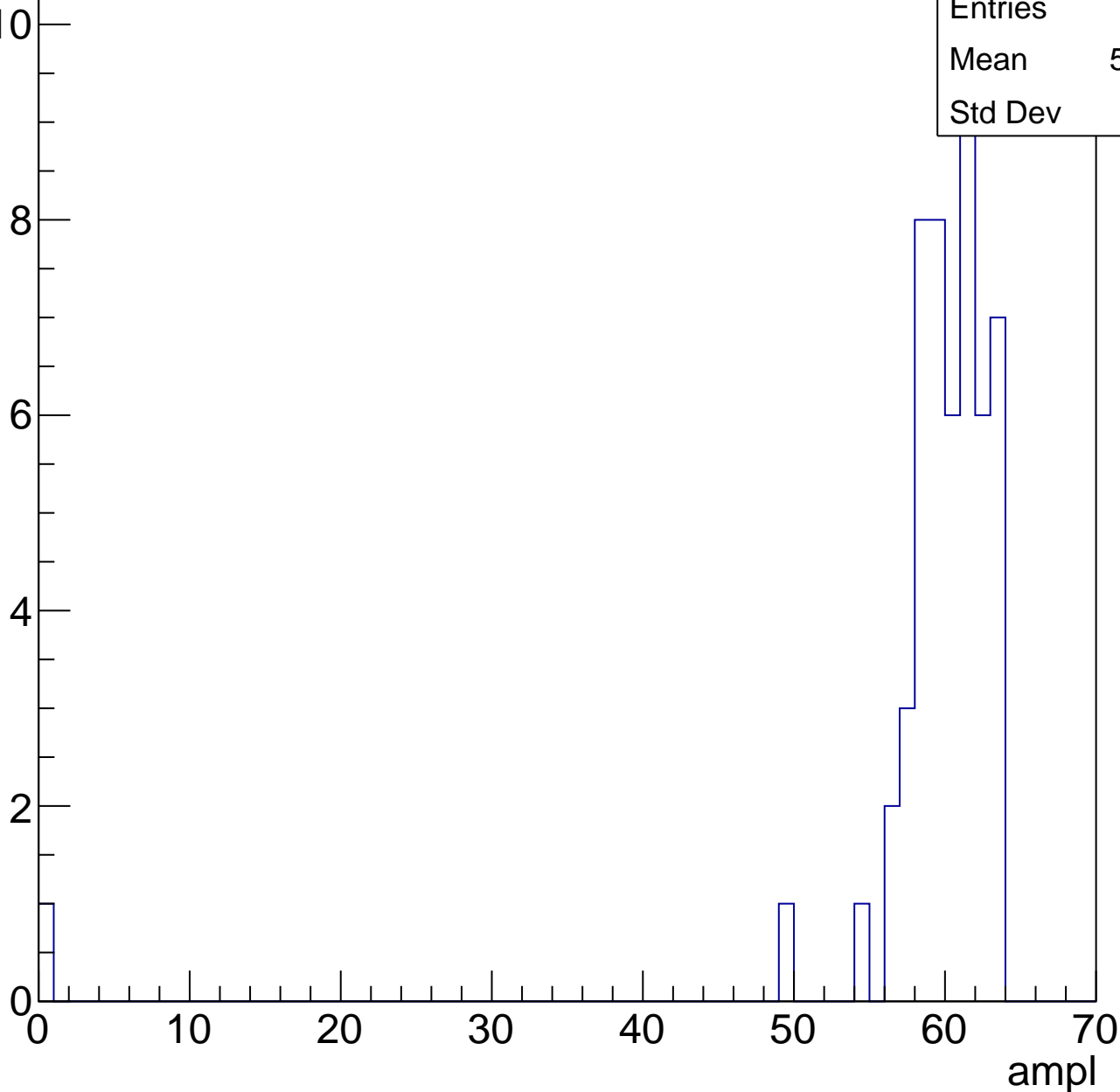


# B1L103S, U26-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

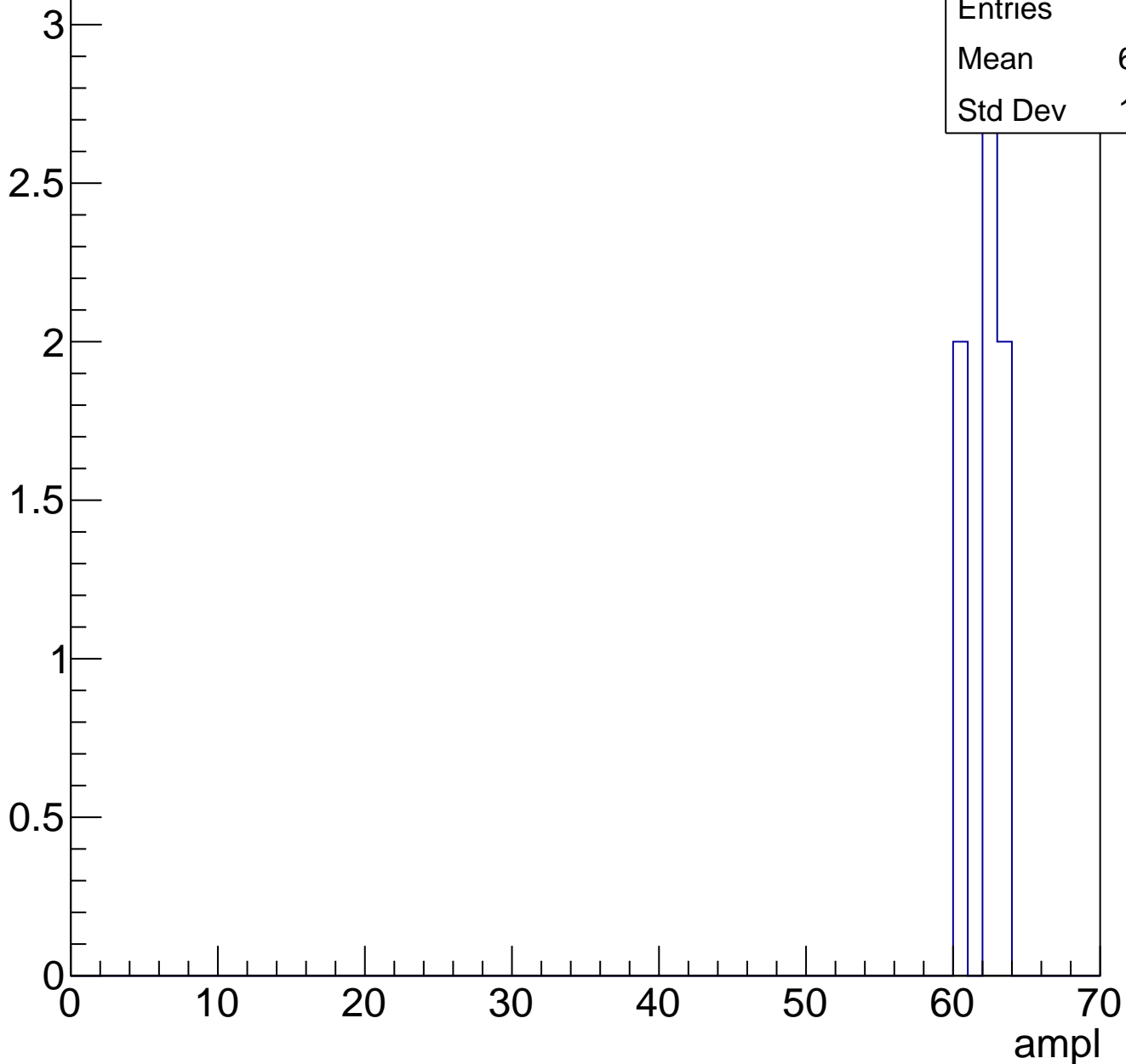
Entries	53
Mean	58.58
Std Dev	8.52



# B1L103S, U26-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U26-ch3, adc0

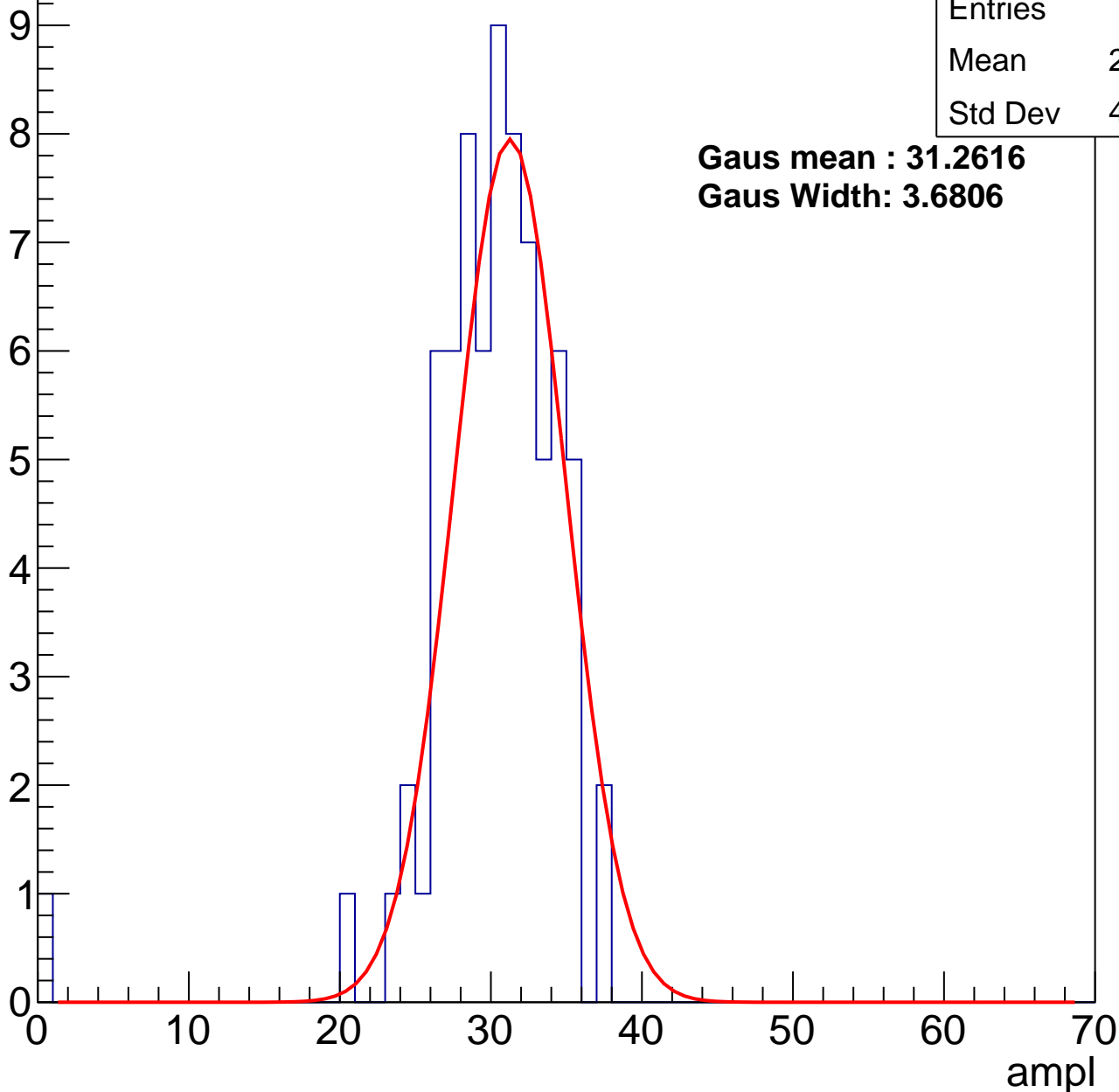
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	29.62
Std Dev	4.826

**Gaus mean : 31.2616**

**Gaus Width: 3.6806**



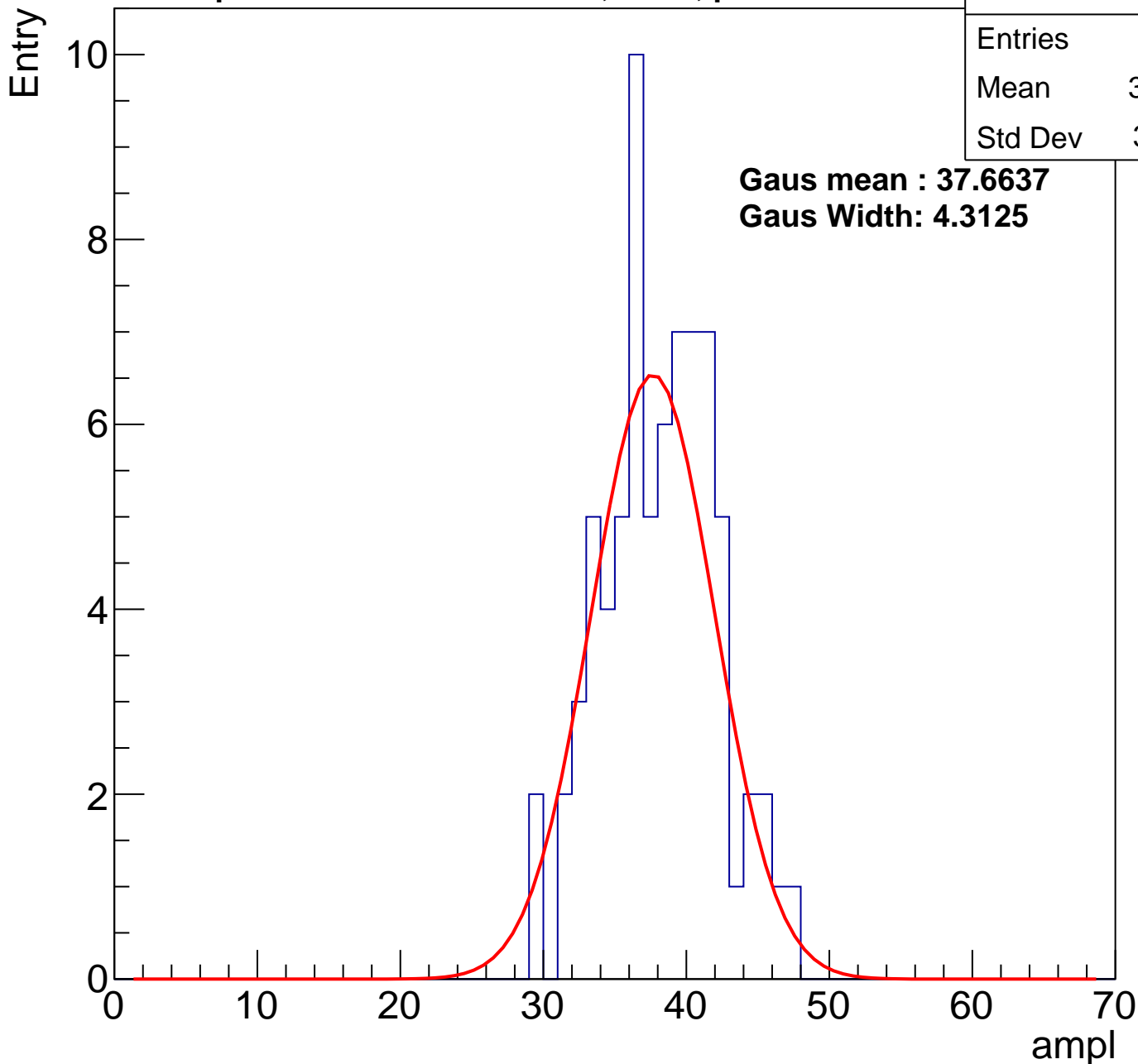
# B1L103S, U26-ch3, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	75
Mean	37.72
Std Dev	3.931

**Gaus mean : 37.6637**

**Gaus Width: 4.3125**



# B1L103S, U26-ch3, adc2

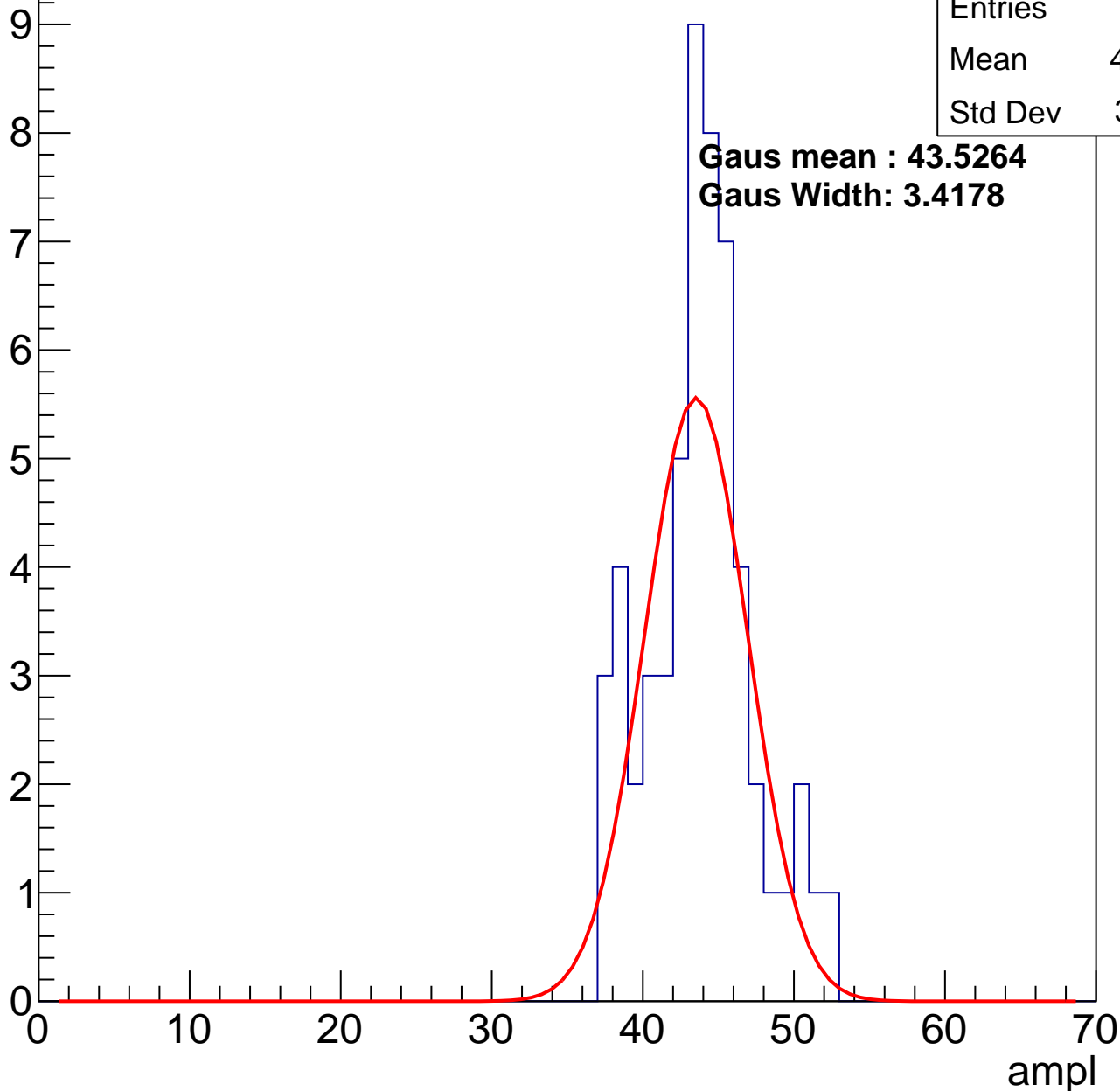
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	43.32
Std Dev	3.501

**Gaus mean : 43.5264**

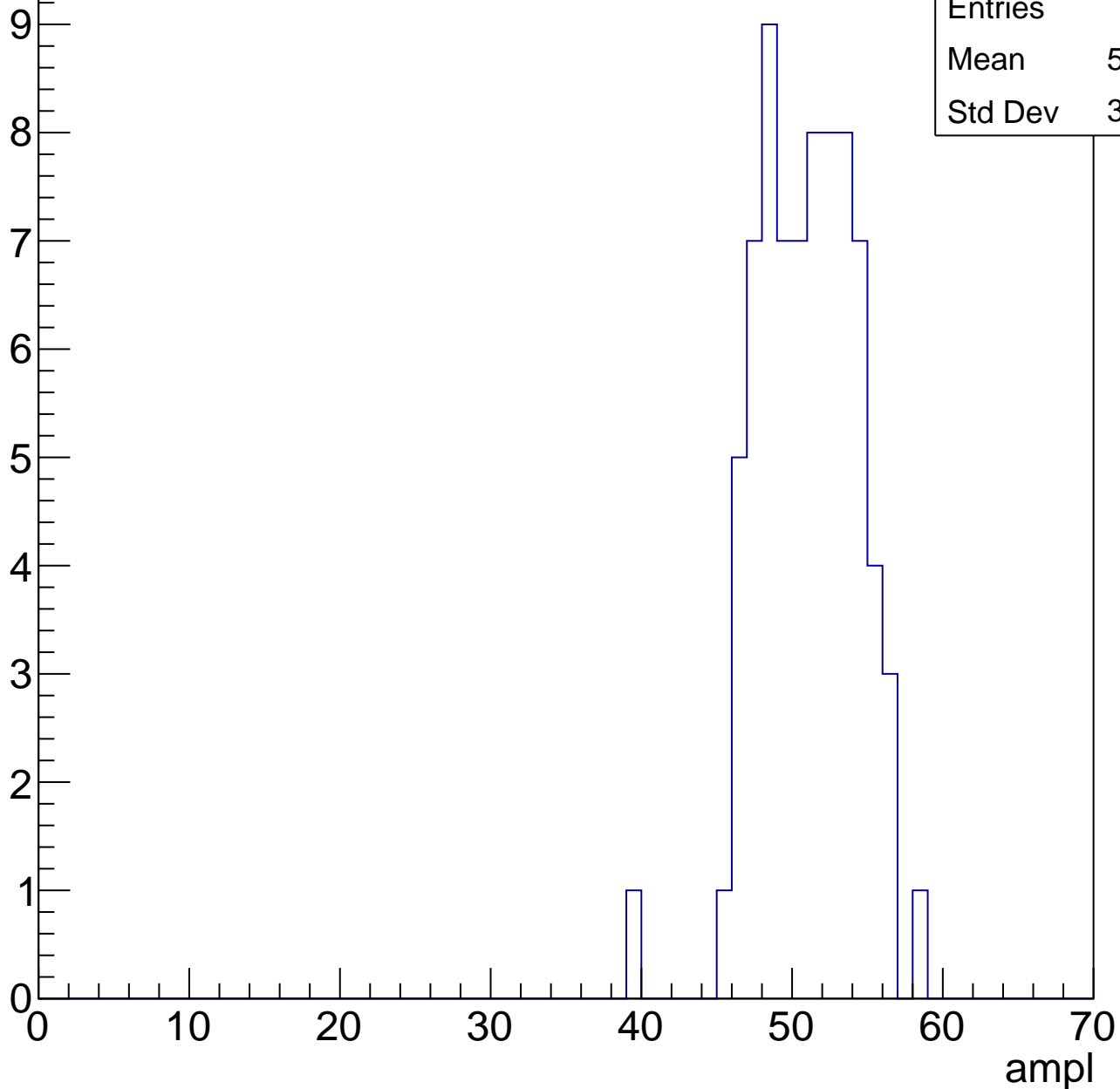
**Gaus Width: 3.4178**



# B1L103S, U26-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

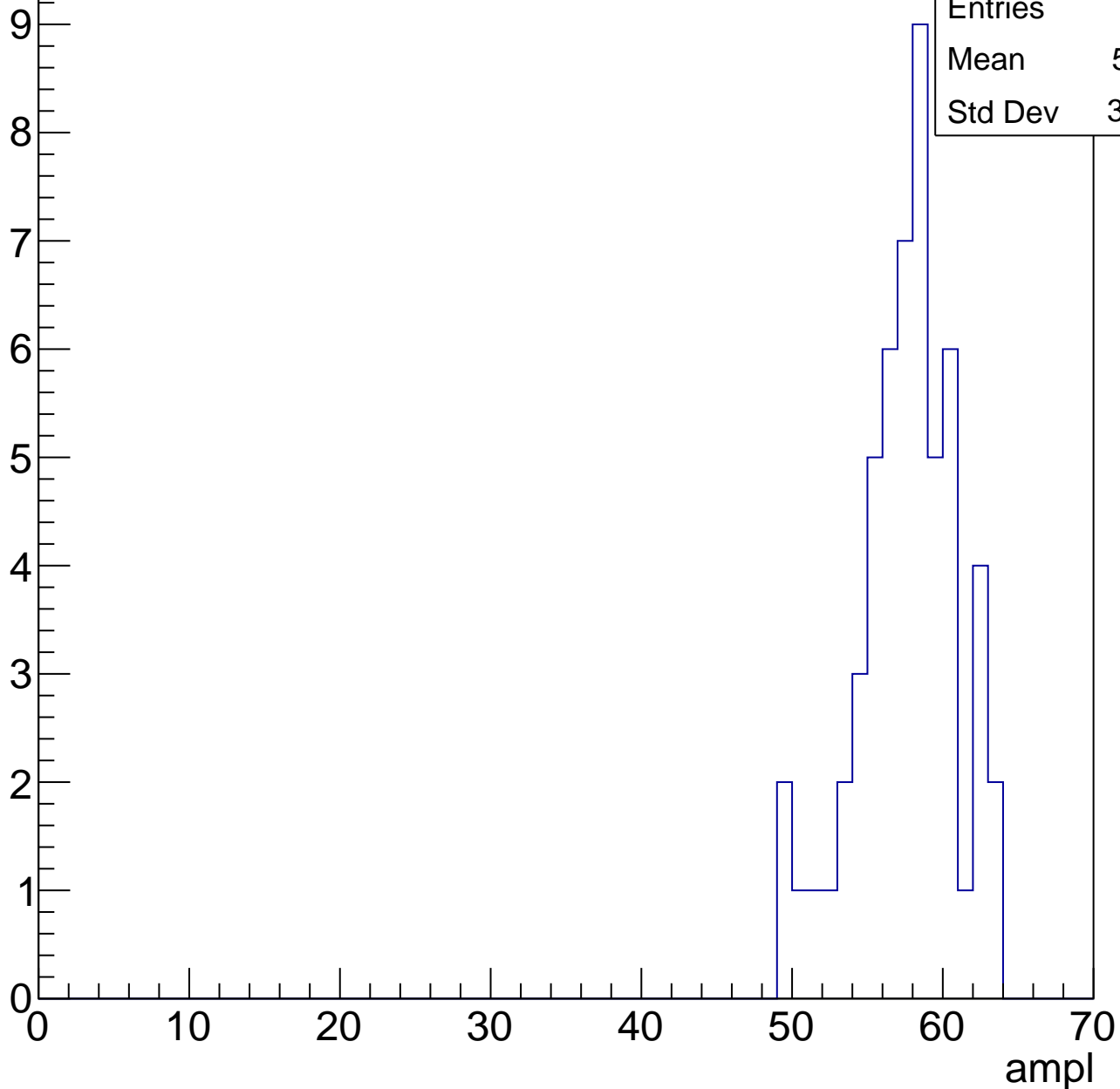
Entry



# B1L103S, U26-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

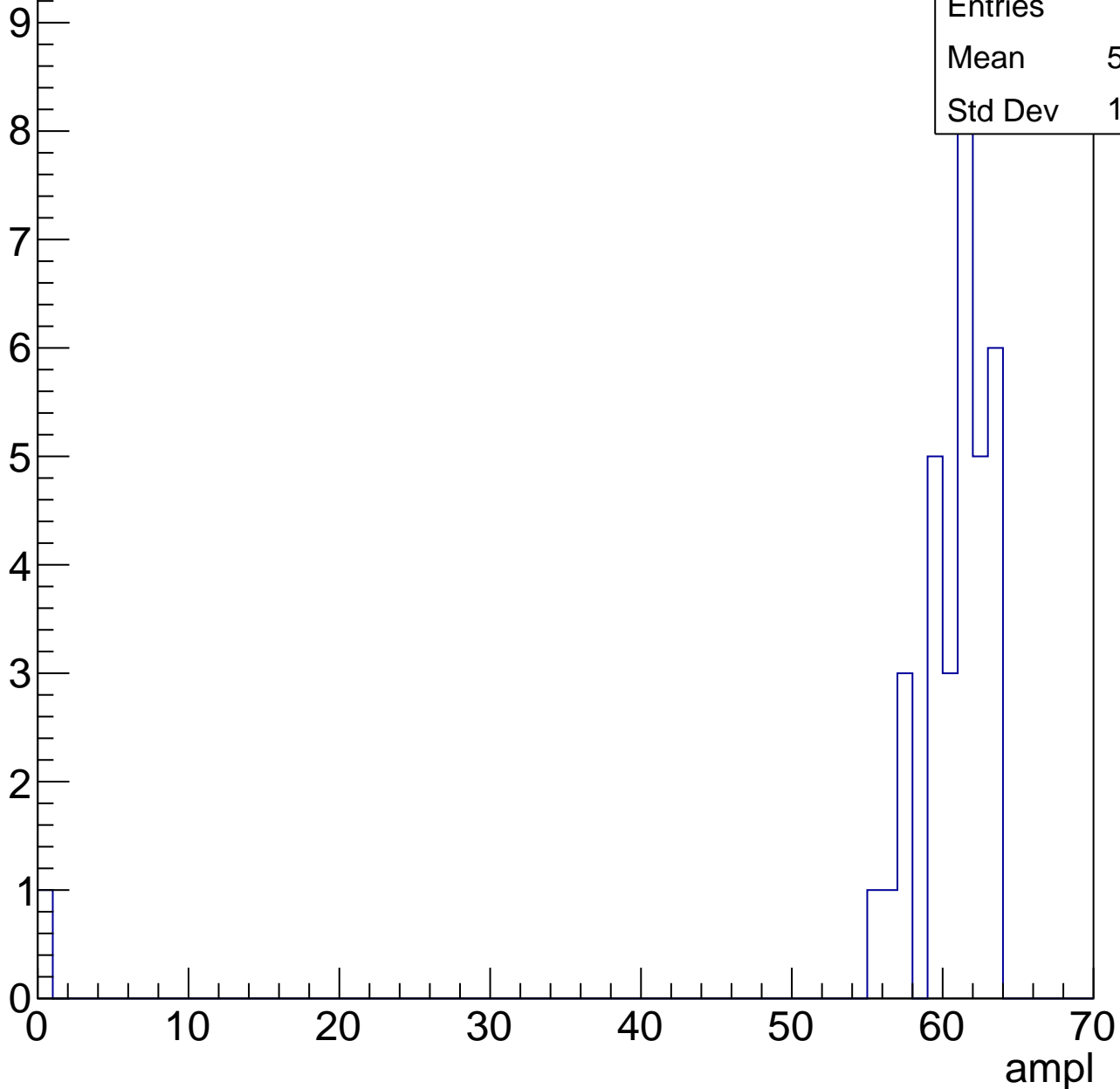


# B1L103S, U26-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	34
Mean	58.65
Std Dev	10.42



# B1L103S, U26-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

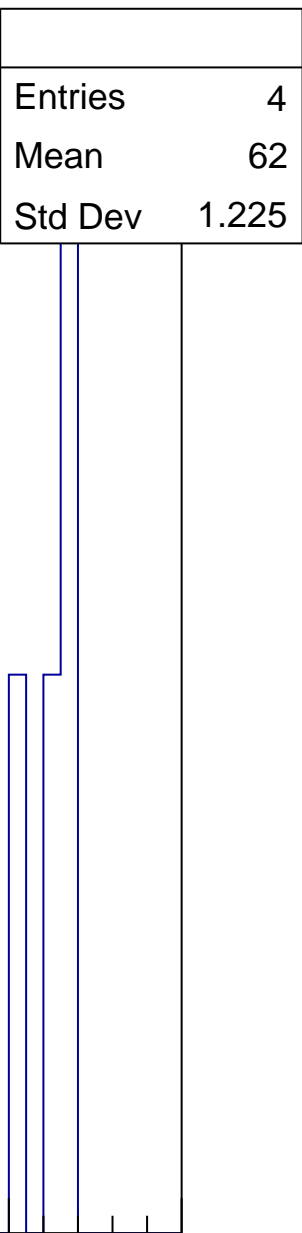
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	62
Std Dev	1.225

0 10 20 30 40 50 60 70

ampl





# B1L103S, U26-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U26-ch4, adc0

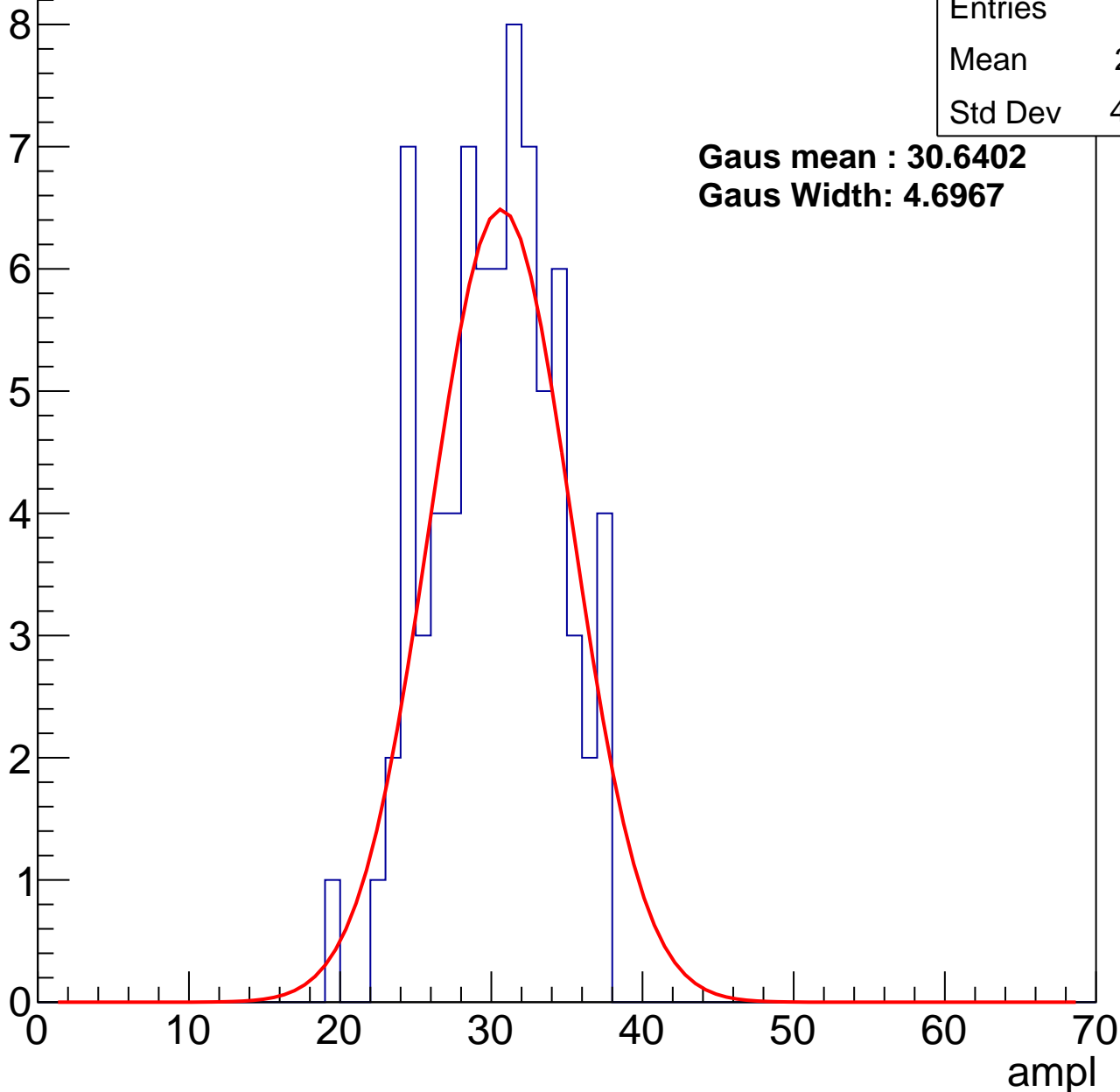
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	29.71
Std Dev	4.068

**Gaus mean : 30.6402**

**Gaus Width: 4.6967**



# B1L103S, U26-ch4, adc1

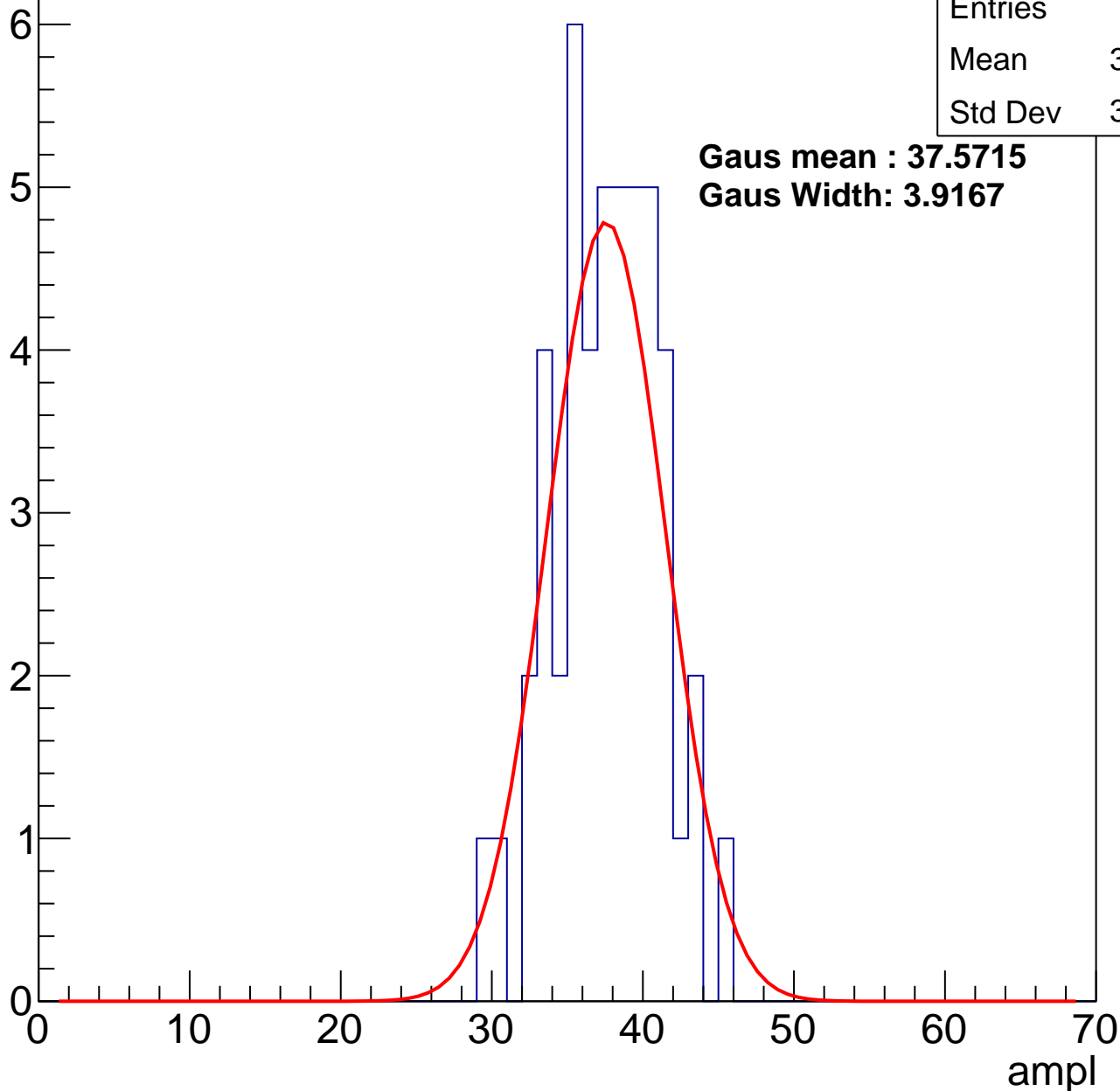
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	37.17
Std Dev	3.436

**Gaus mean : 37.5715**

**Gaus Width: 3.9167**



# B1L103S, U26-ch4, adc2

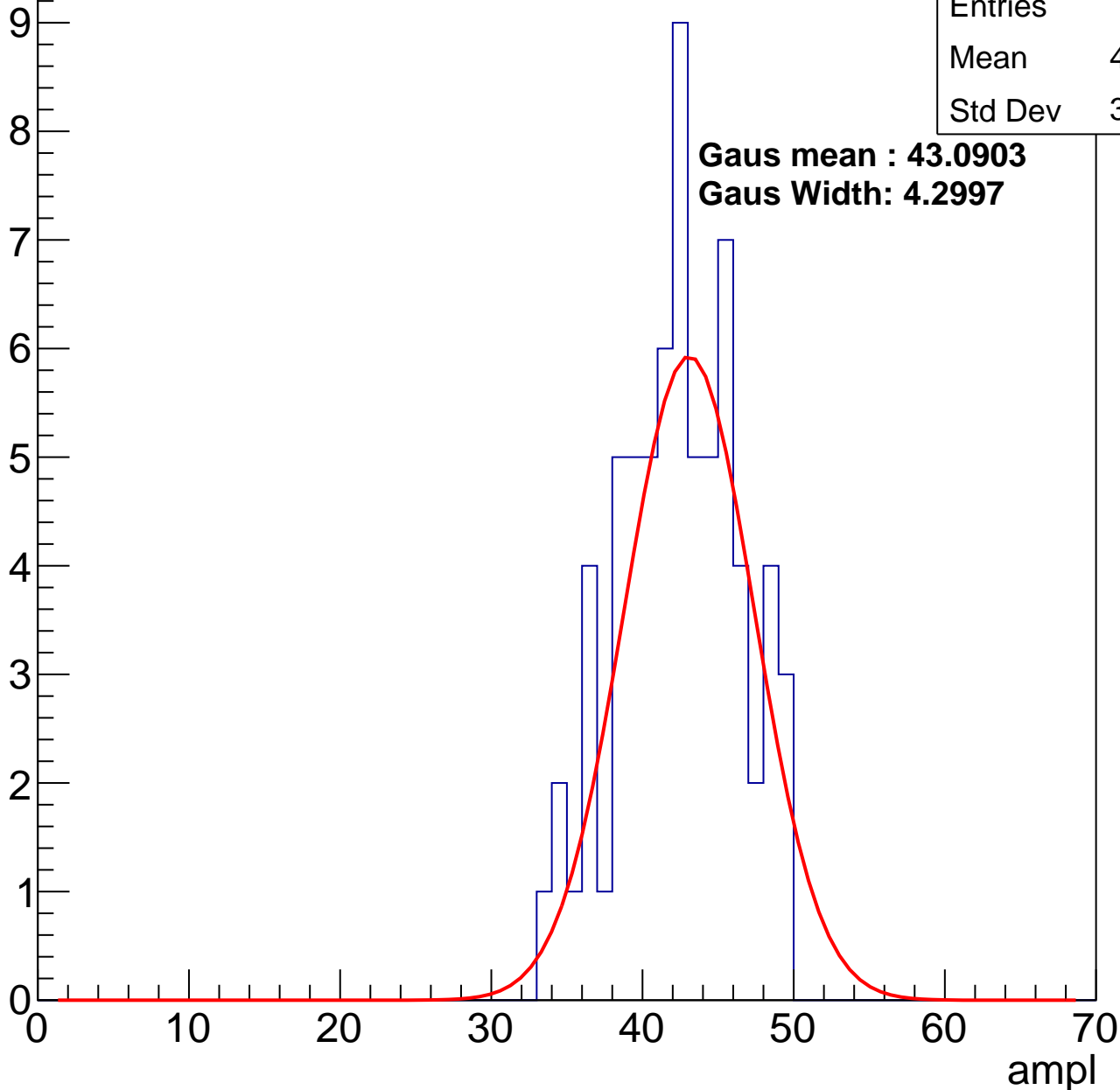
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	41.93
Std Dev	3.939

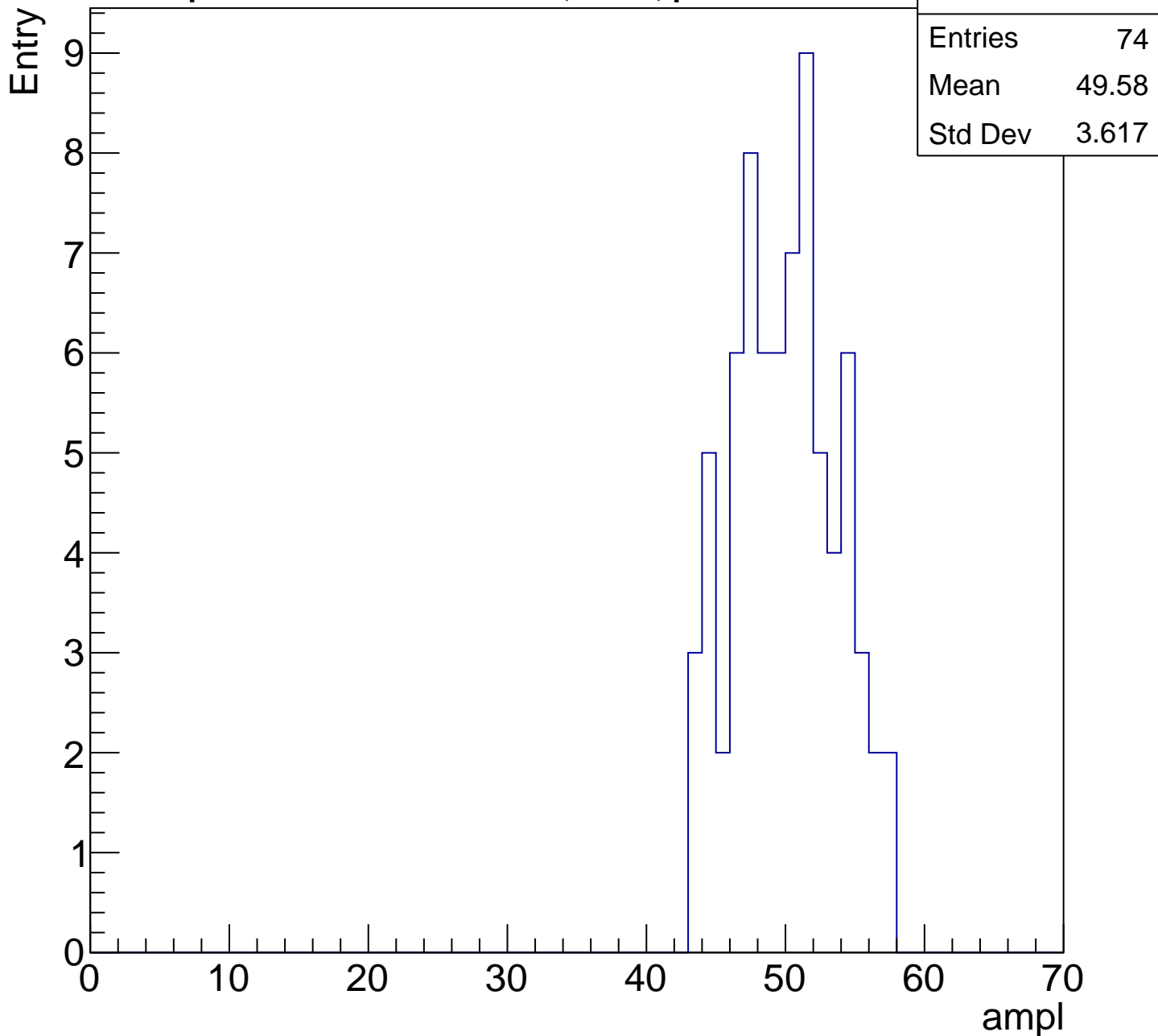
**Gaus mean : 43.0903**

**Gaus Width: 4.2997**



# B1L103S, U26-ch4, adc3

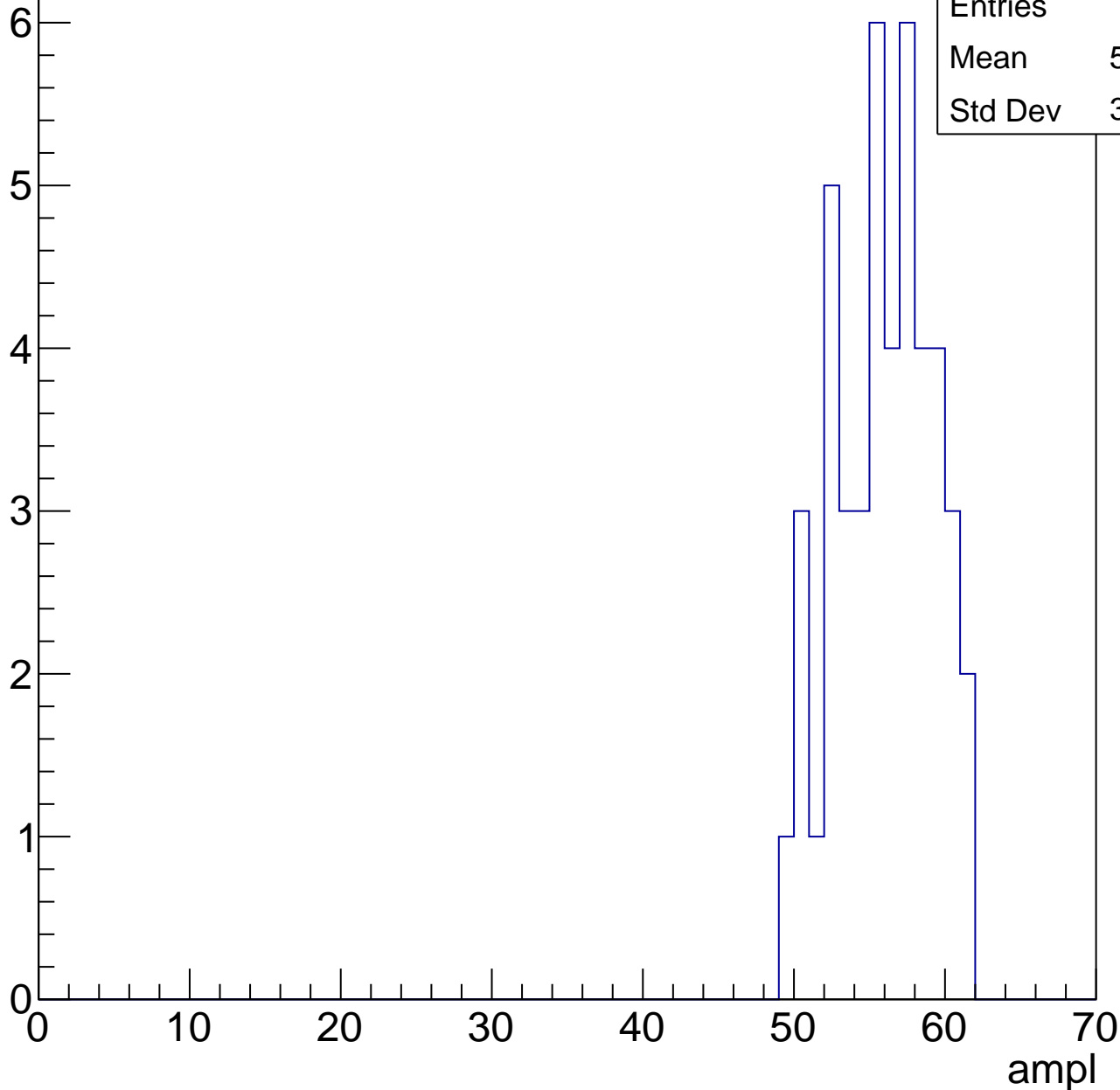
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U26-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



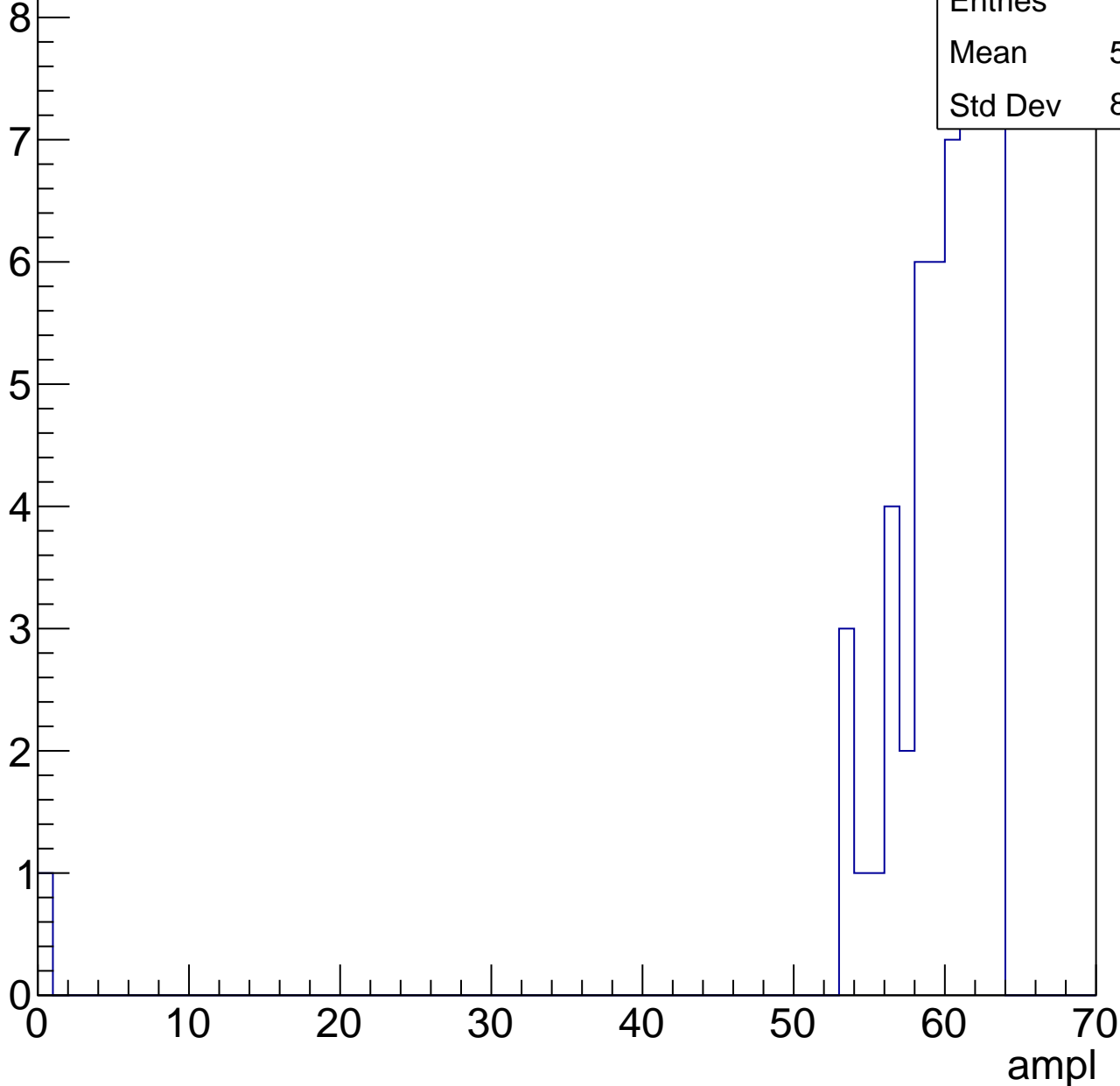
Entries	45
Mean	55.49
Std Dev	3.167

# B1L103S, U26-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	58.47
Std Dev	8.425



# B1L103S, U26-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U26-ch5, adc0

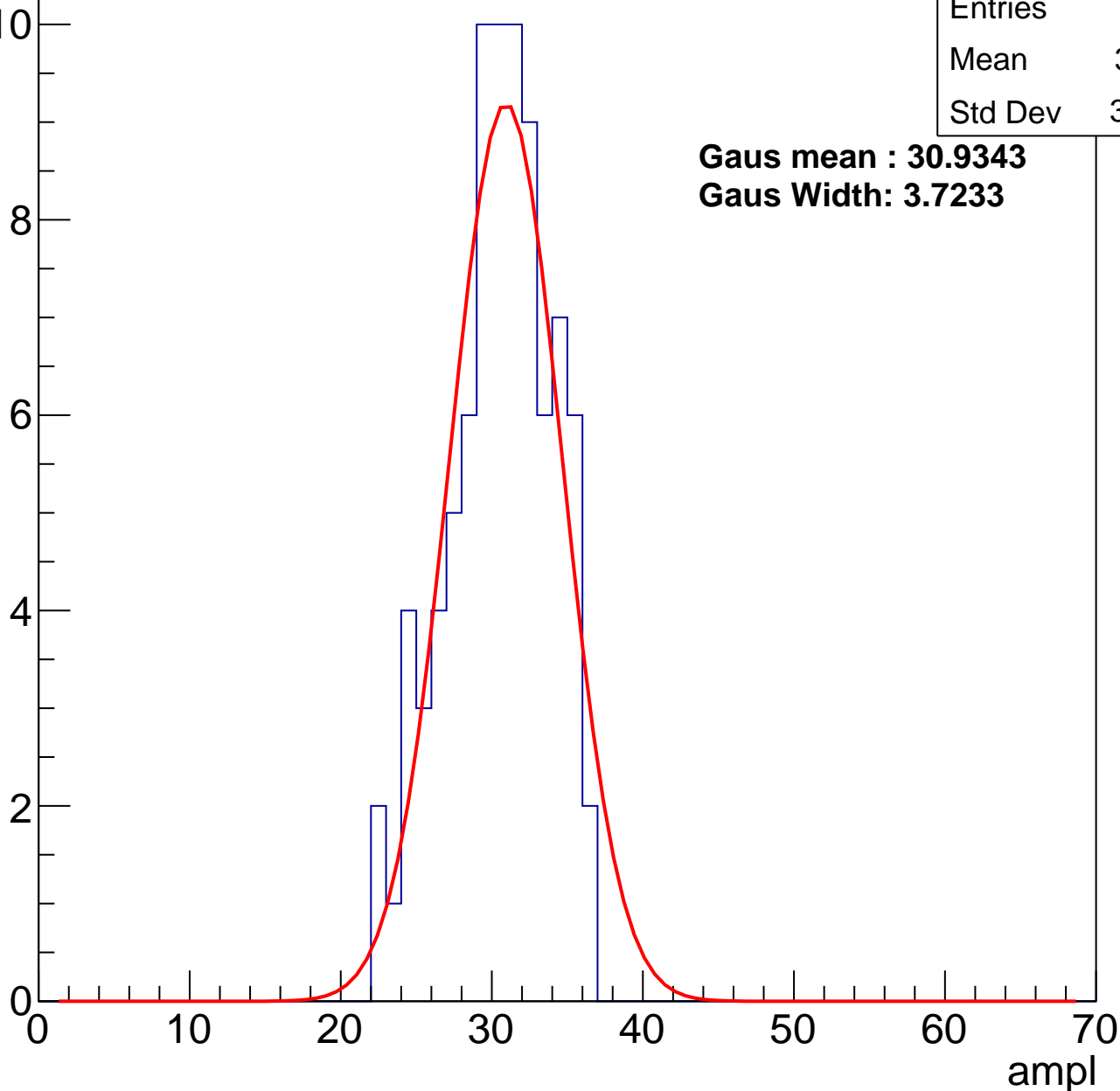
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	85
Mean	30.01
Std Dev	3.383

**Gaus mean : 30.9343**

**Gaus Width: 3.7233**



# B1L103S, U26-ch5, adc1

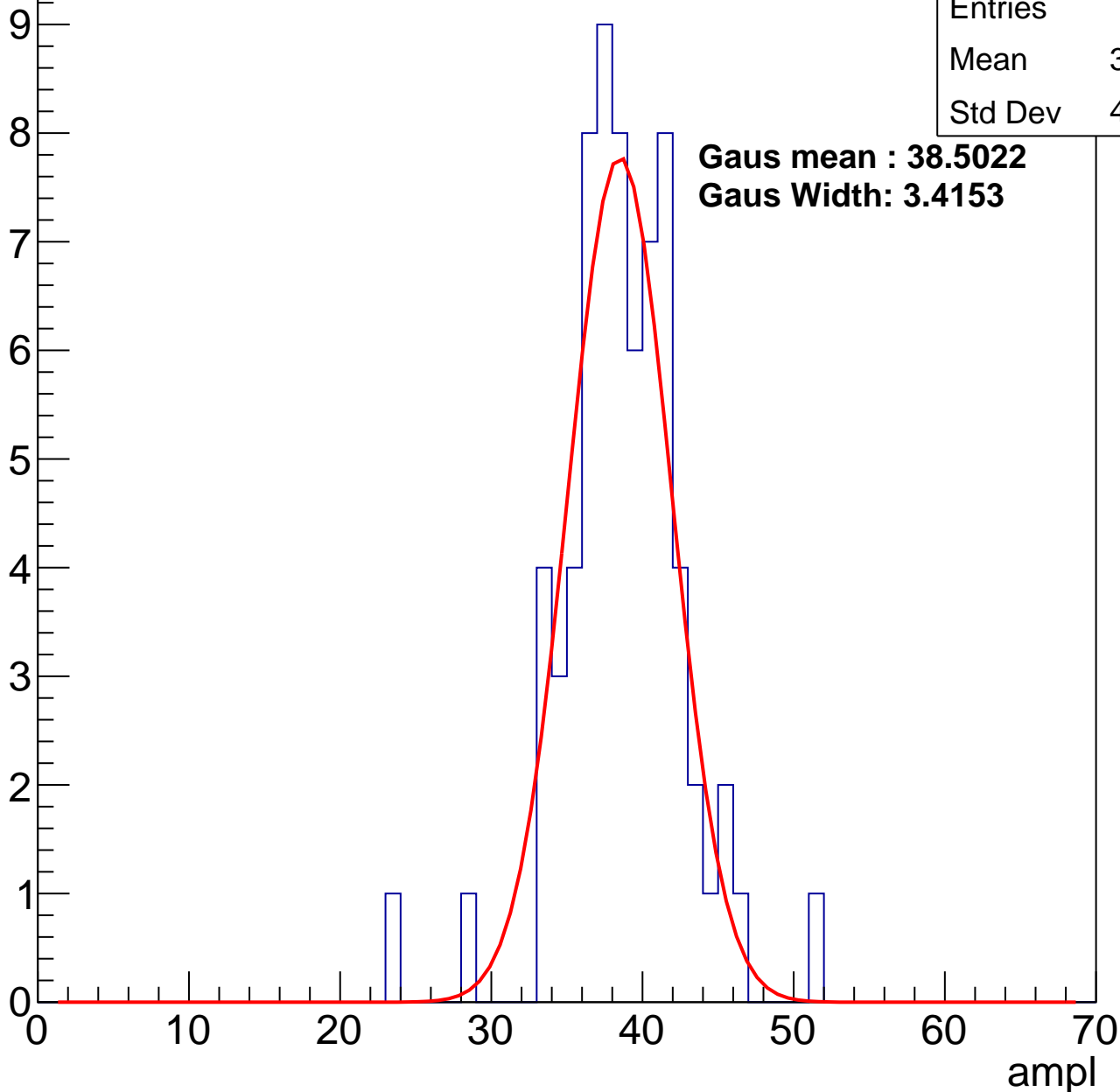
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	38.24
Std Dev	4.023

**Gaus mean : 38.5022**

**Gaus Width: 3.4153**



# B1L103S, U26-ch5, adc2

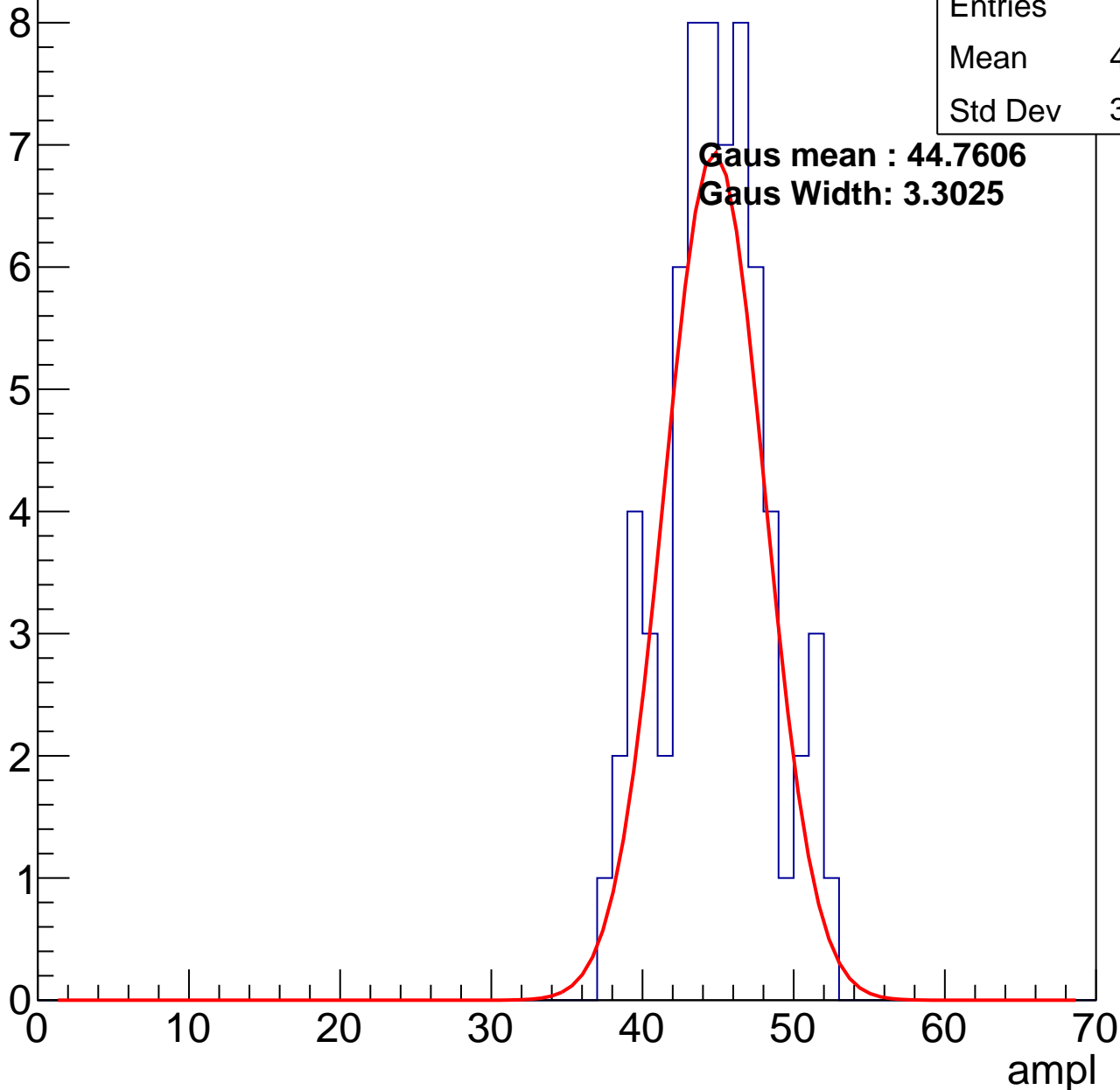
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	44.39
Std Dev	3.424

**Gaus mean : 44.7606**

**Gaus Width: 3.3025**

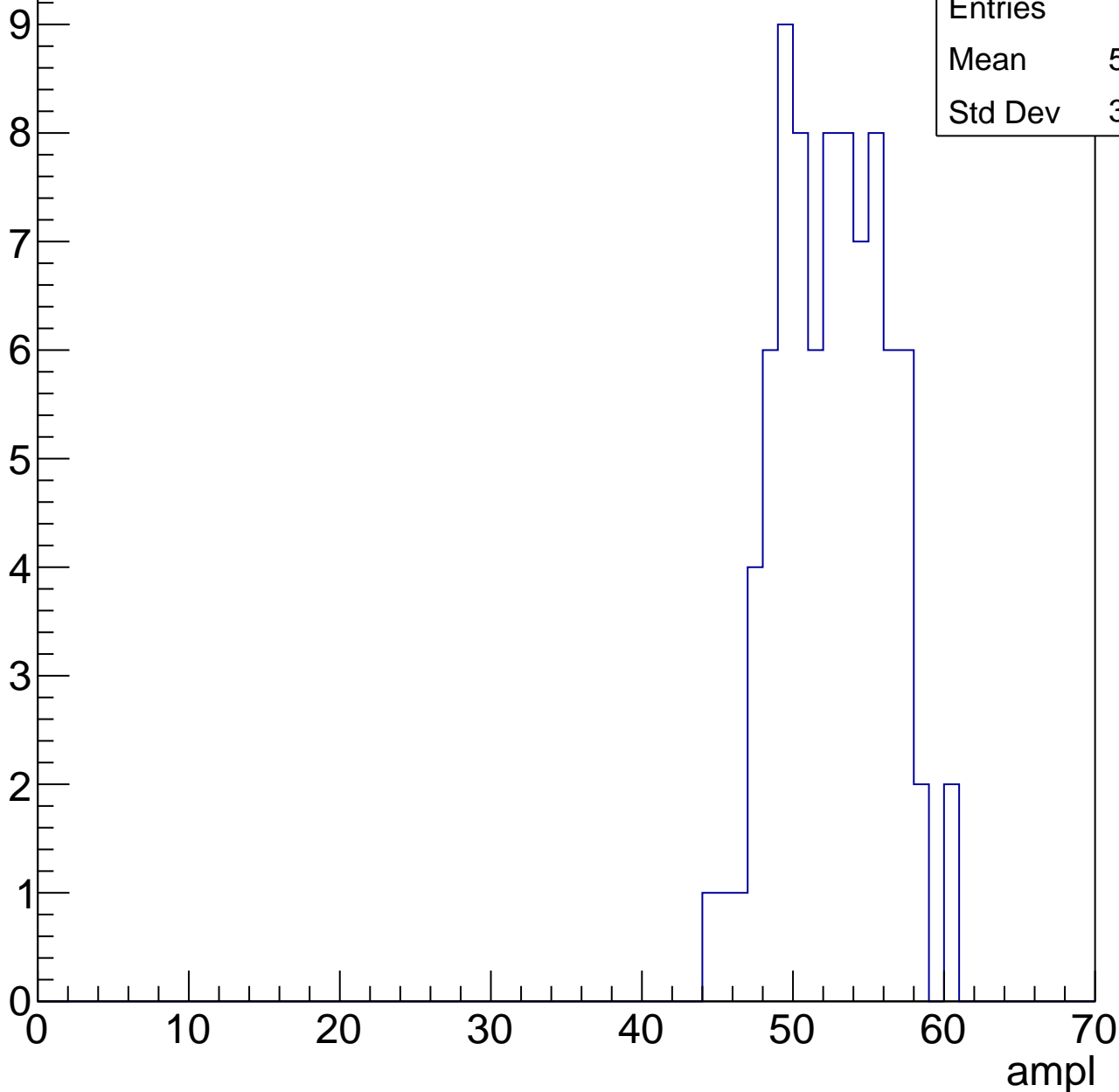


# B1L103S, U26-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	52.17
Std Dev	3.498



# B1L103S, U26-ch5, adc4

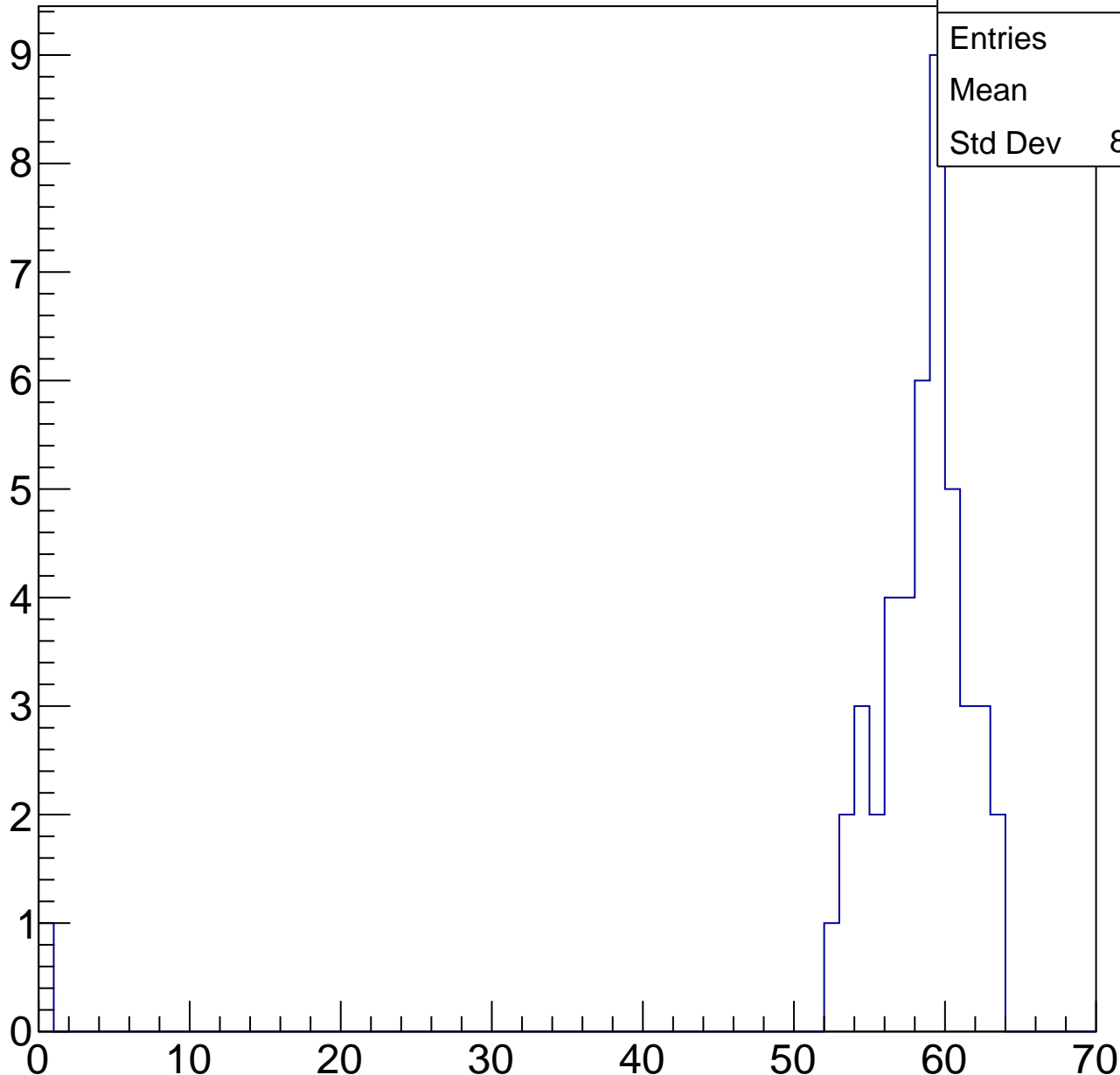
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	45
Mean	56.8
Std Dev	8.976

ampl



# B1L103S, U26-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

7

6

5

4

3

2

1

0

Entries

27

Mean

61.37

Std Dev

1.444

ampl

0

10

20

30

40

50

60

70

# B1L103S, U26-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U26-ch6, adc0

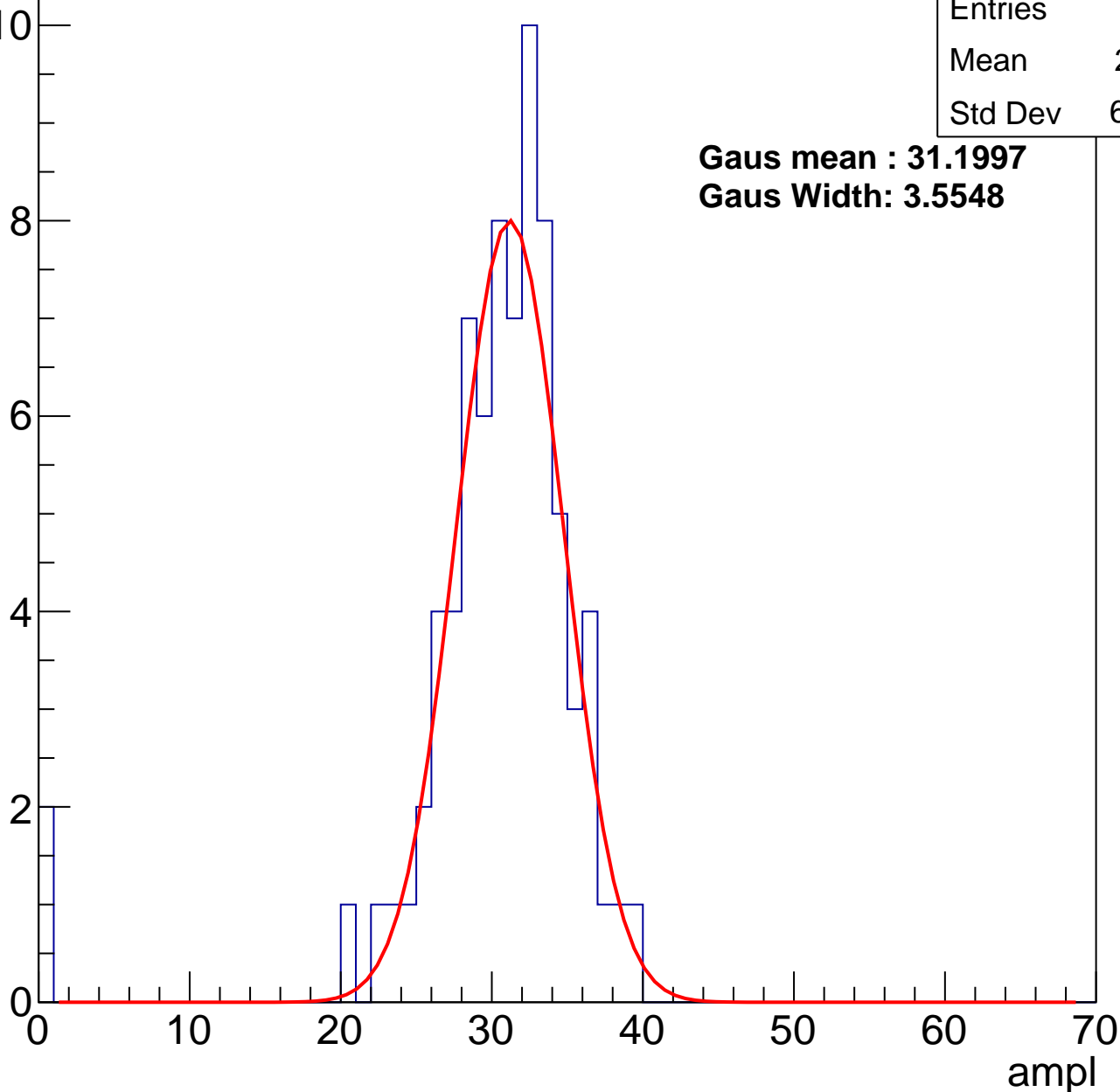
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	29.81
Std Dev	6.075

**Gaus mean : 31.1997**

**Gaus Width: 3.5548**



# B1L103S, U26-ch6, adc1

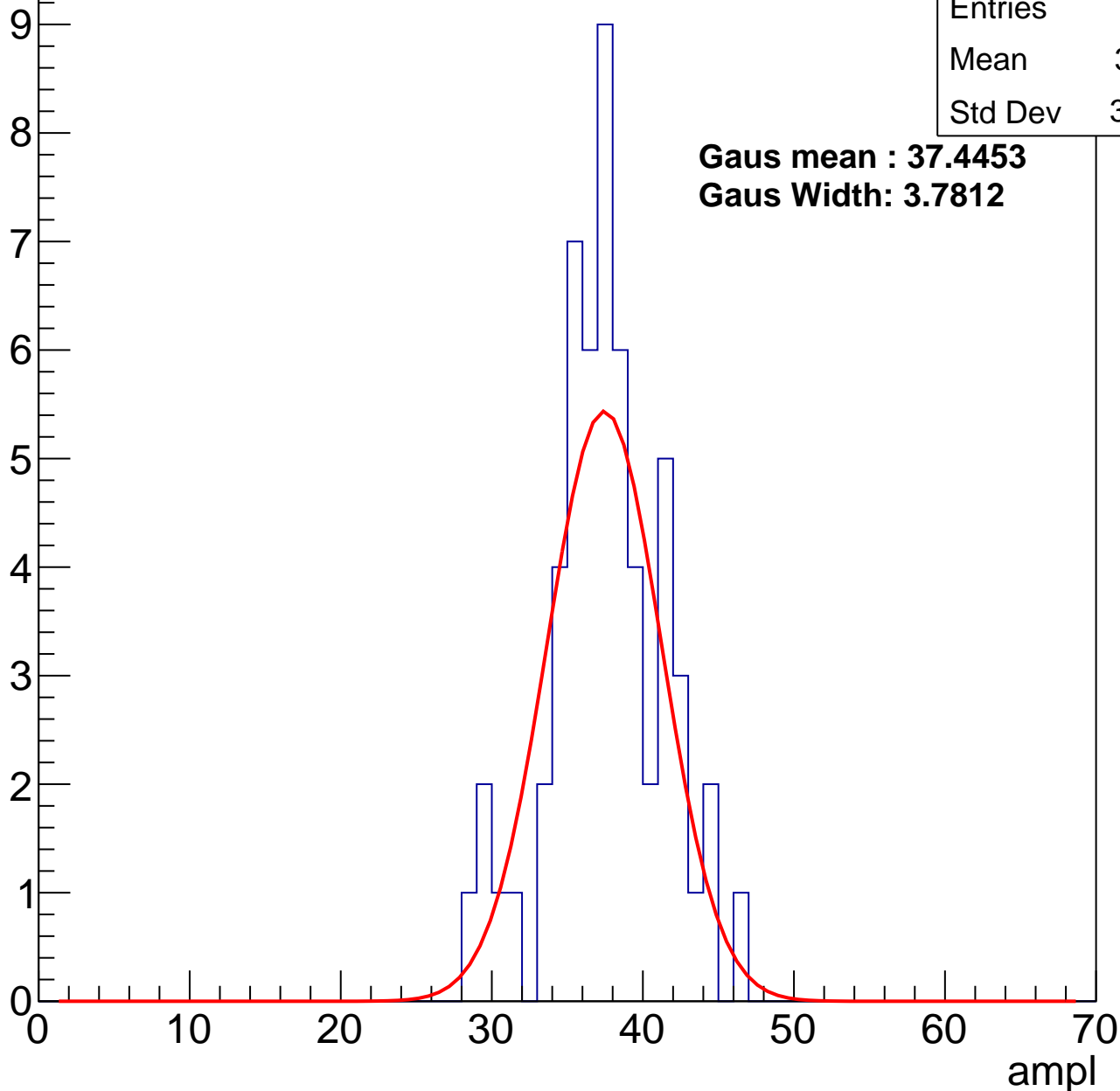
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	37.11
Std Dev	3.759

**Gaus mean : 37.4453**

**Gaus Width: 3.7812**



# B1L103S, U26-ch6, adc2

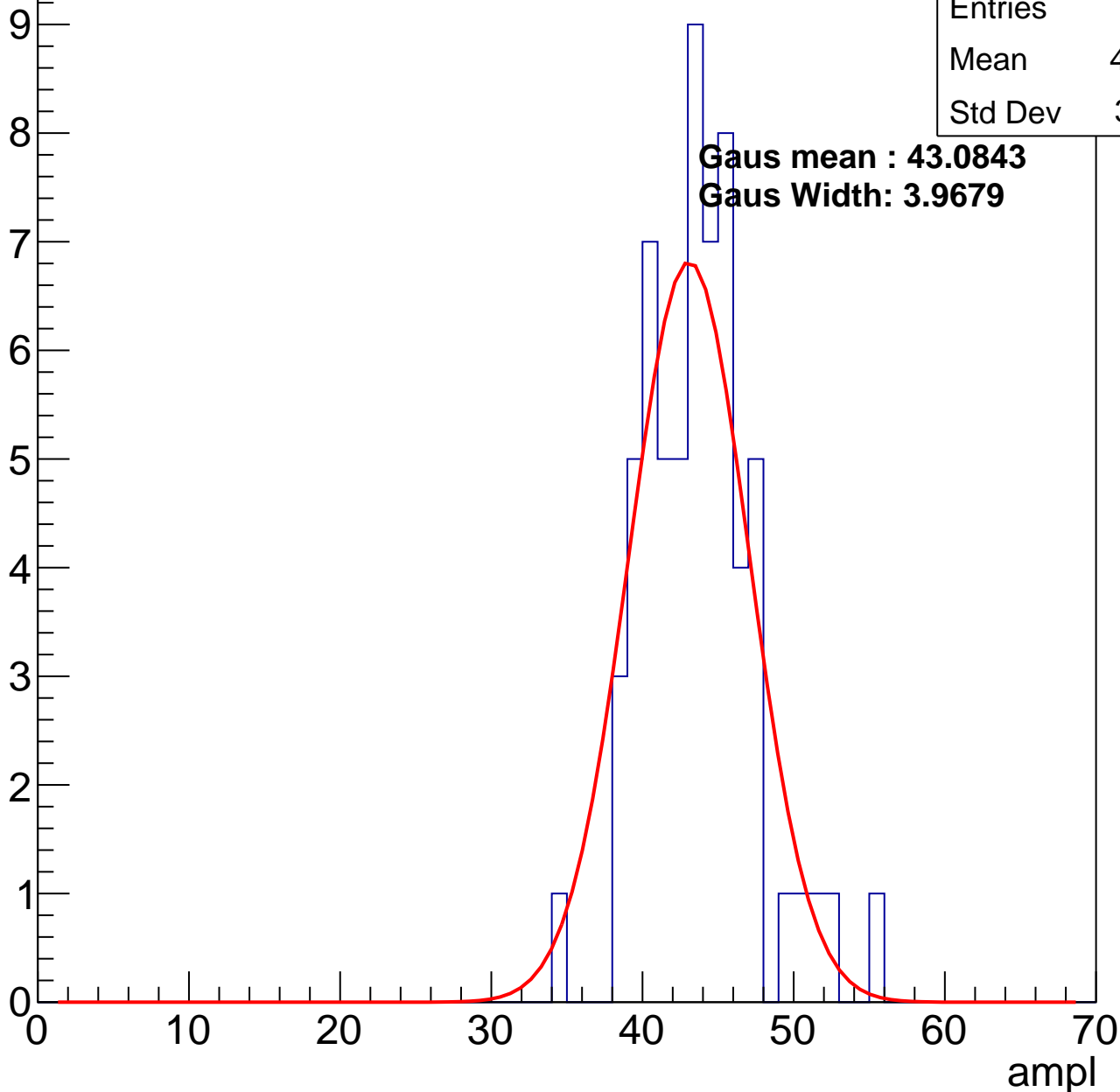
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	43.27
Std Dev	3.641

**Gaus mean : 43.0843**

**Gaus Width: 3.9679**

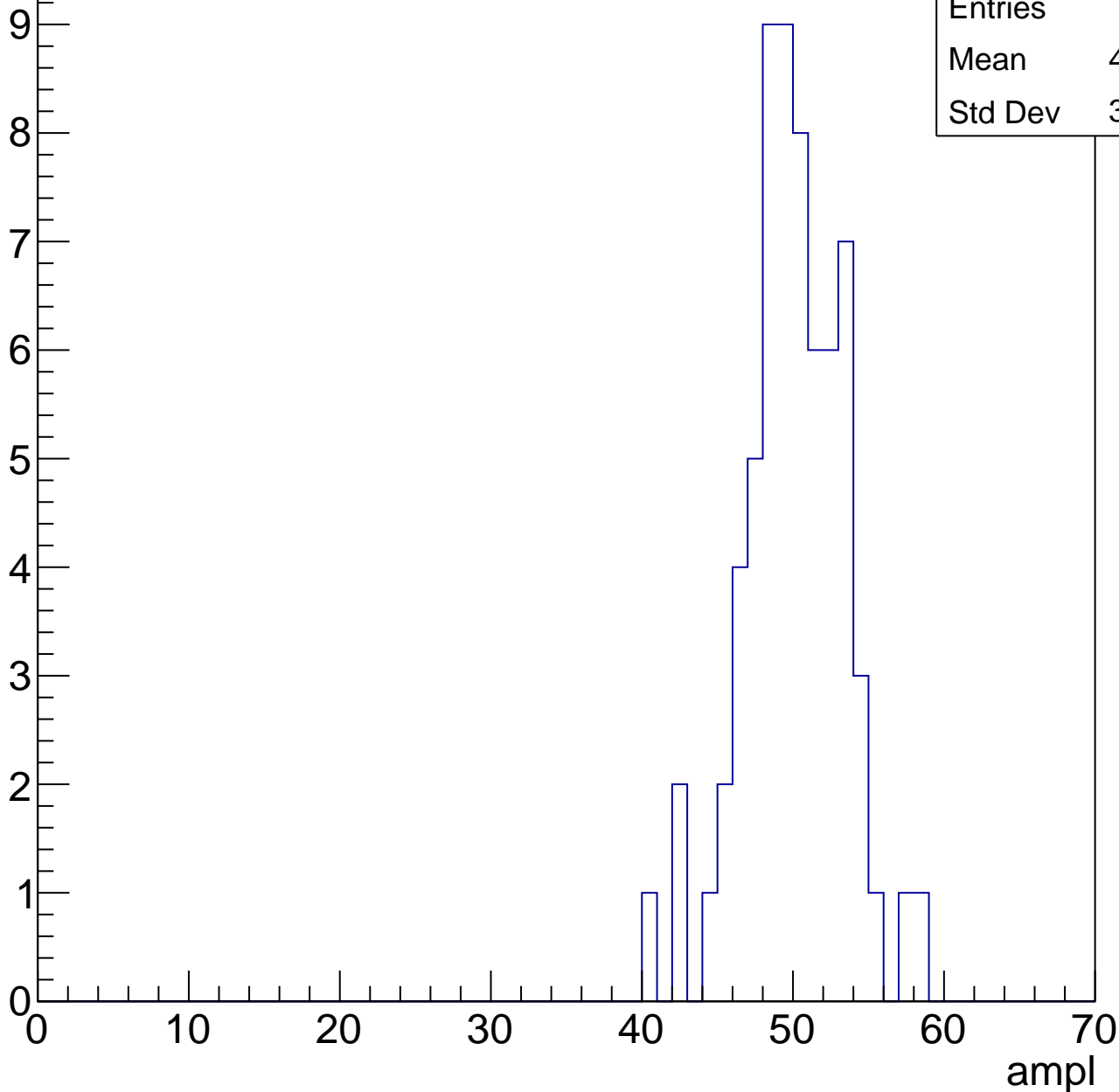


# B1L103S, U26-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	49.56
Std Dev	3.335

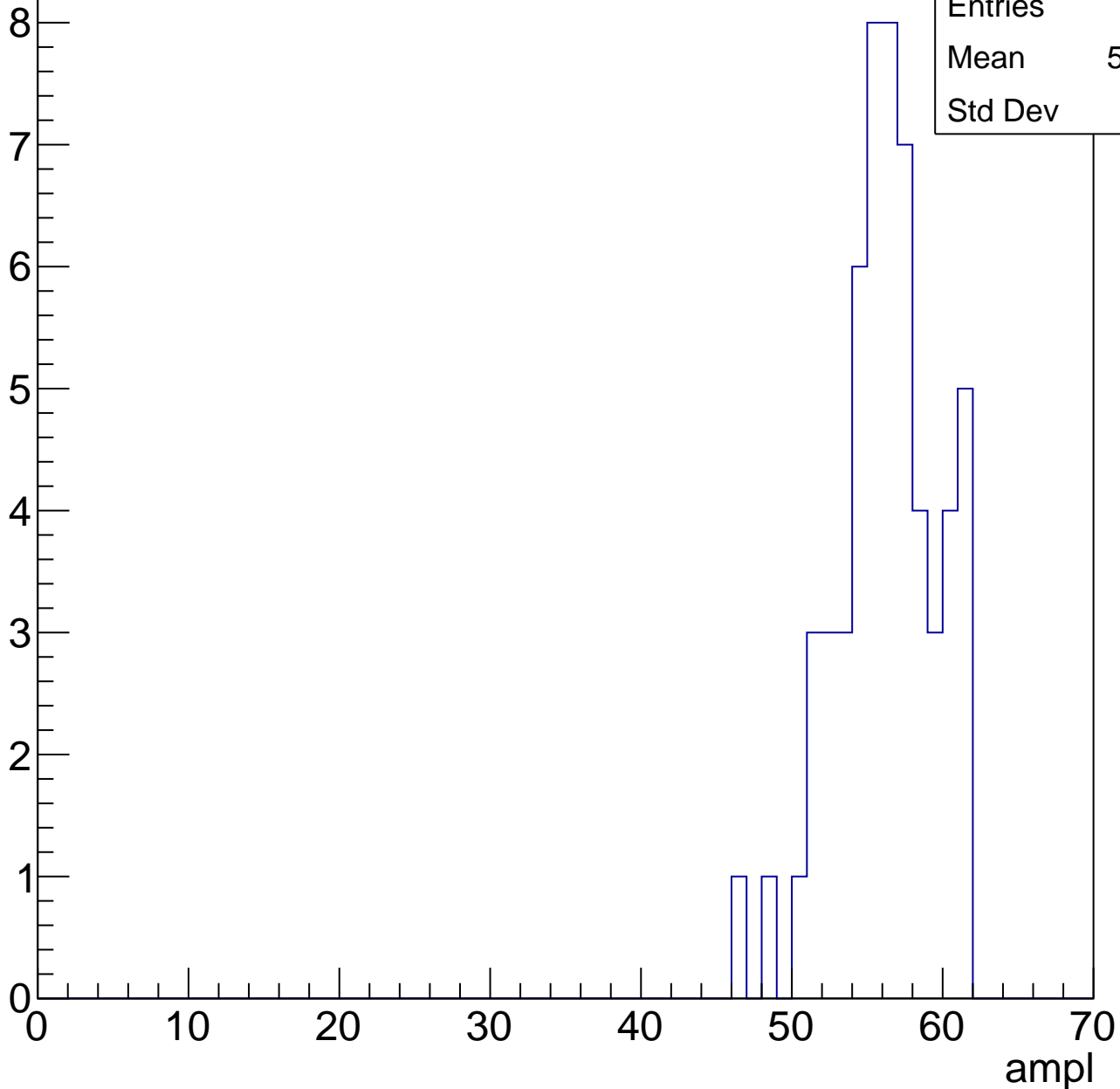


# B1L103S, U26-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	55.74
Std Dev	3.29

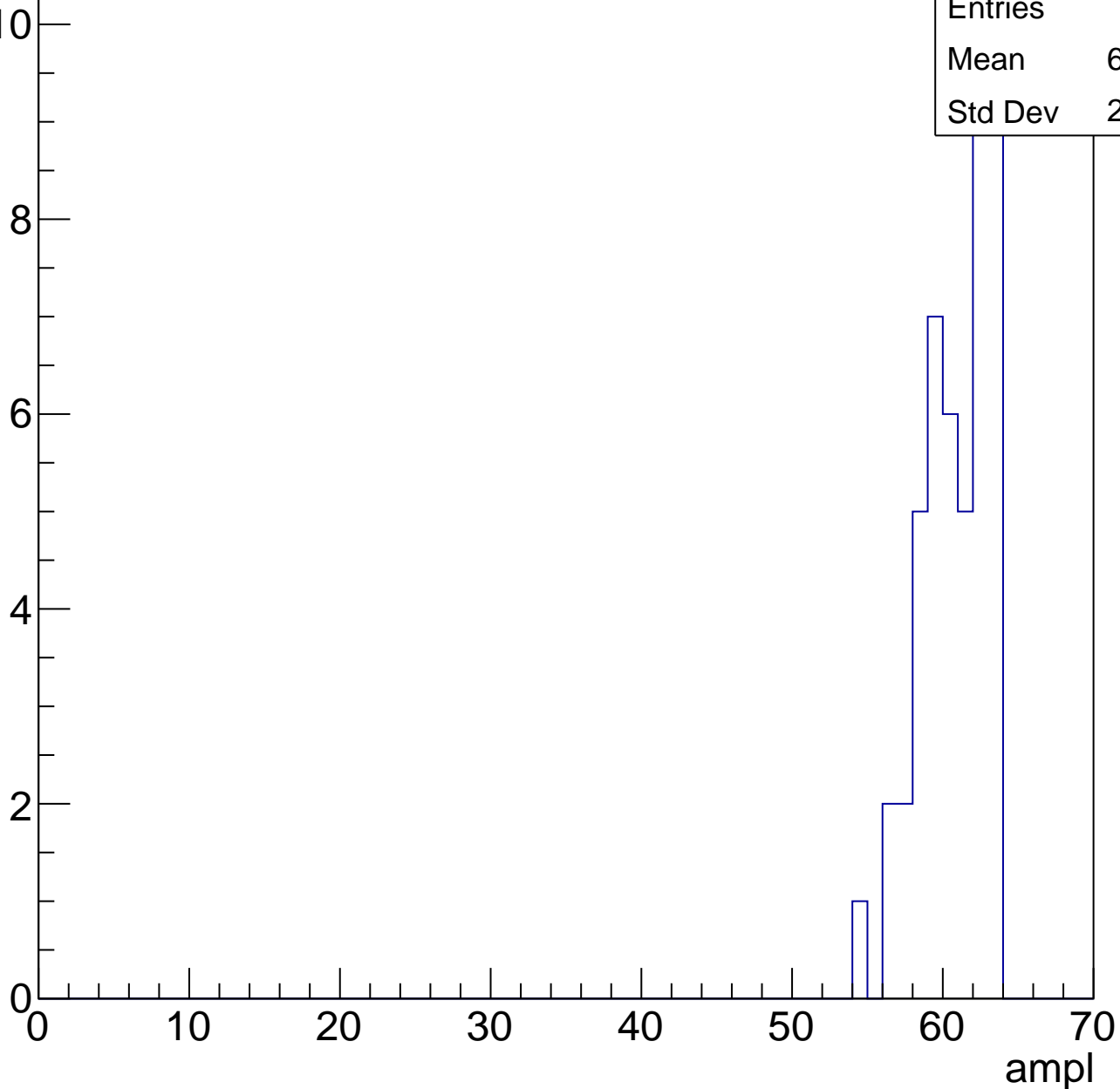


# B1L103S, U26-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

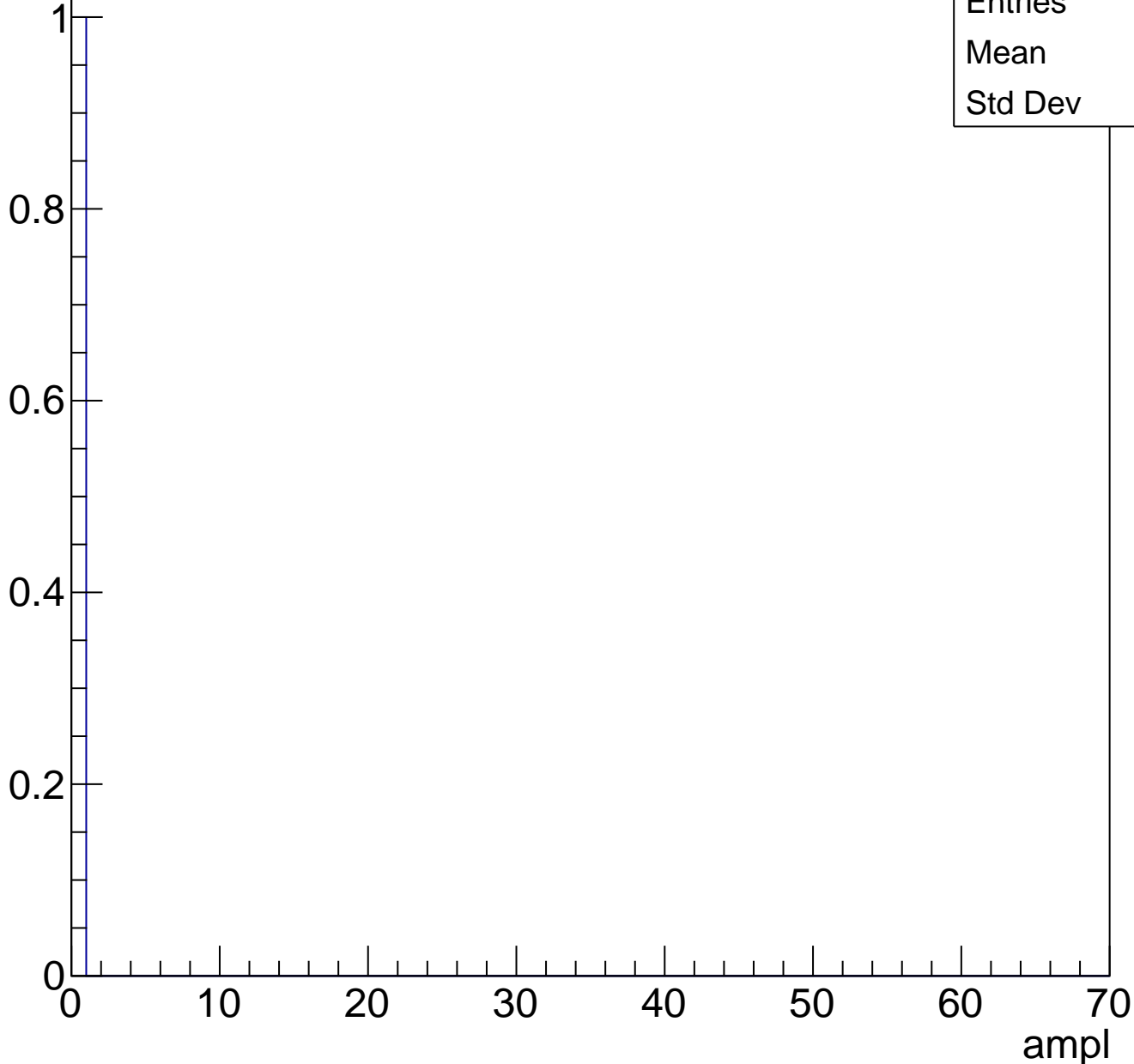
Entries	47
Mean	60.32
Std Dev	2.232



# B1L103S, U26-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch7, adc0

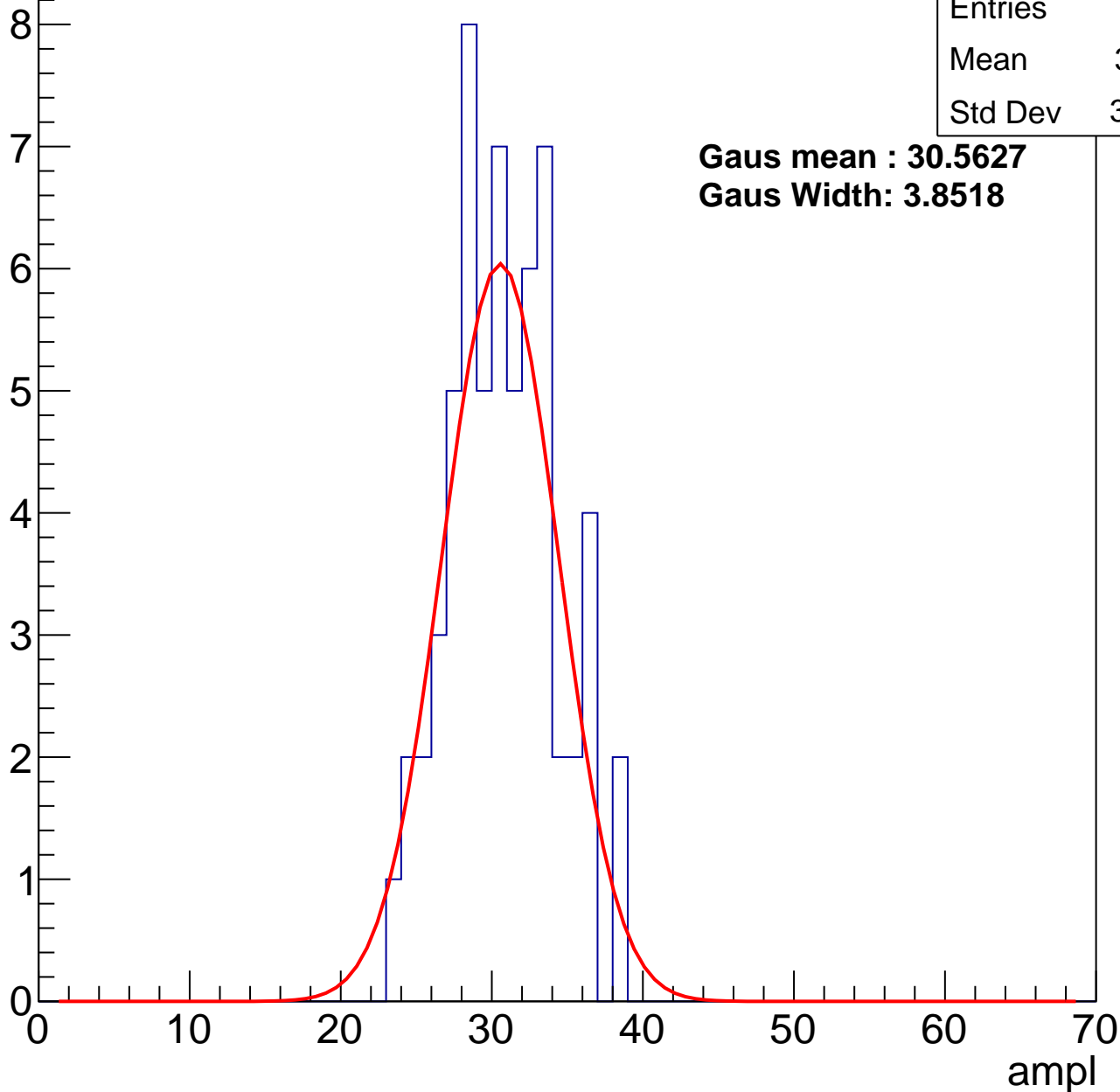
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	30.31
Std Dev	3.486

**Gaus mean : 30.5627**

**Gaus Width: 3.8518**



# B1L103S, U26-ch7, adc1

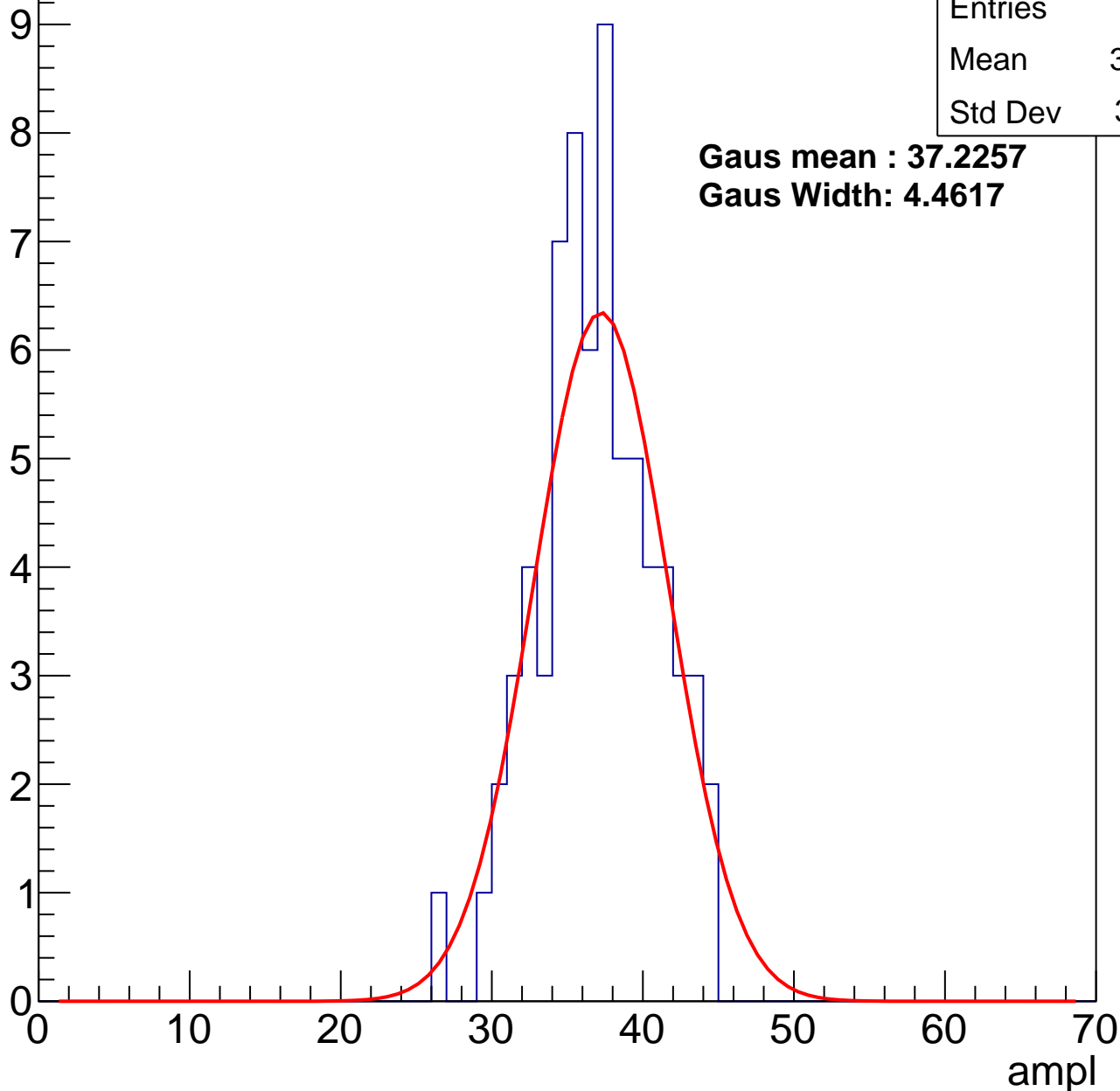
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	36.49
Std Dev	3.831

**Gaus mean : 37.2257**

**Gaus Width: 4.4617**



# B1L103S, U26-ch7, adc2

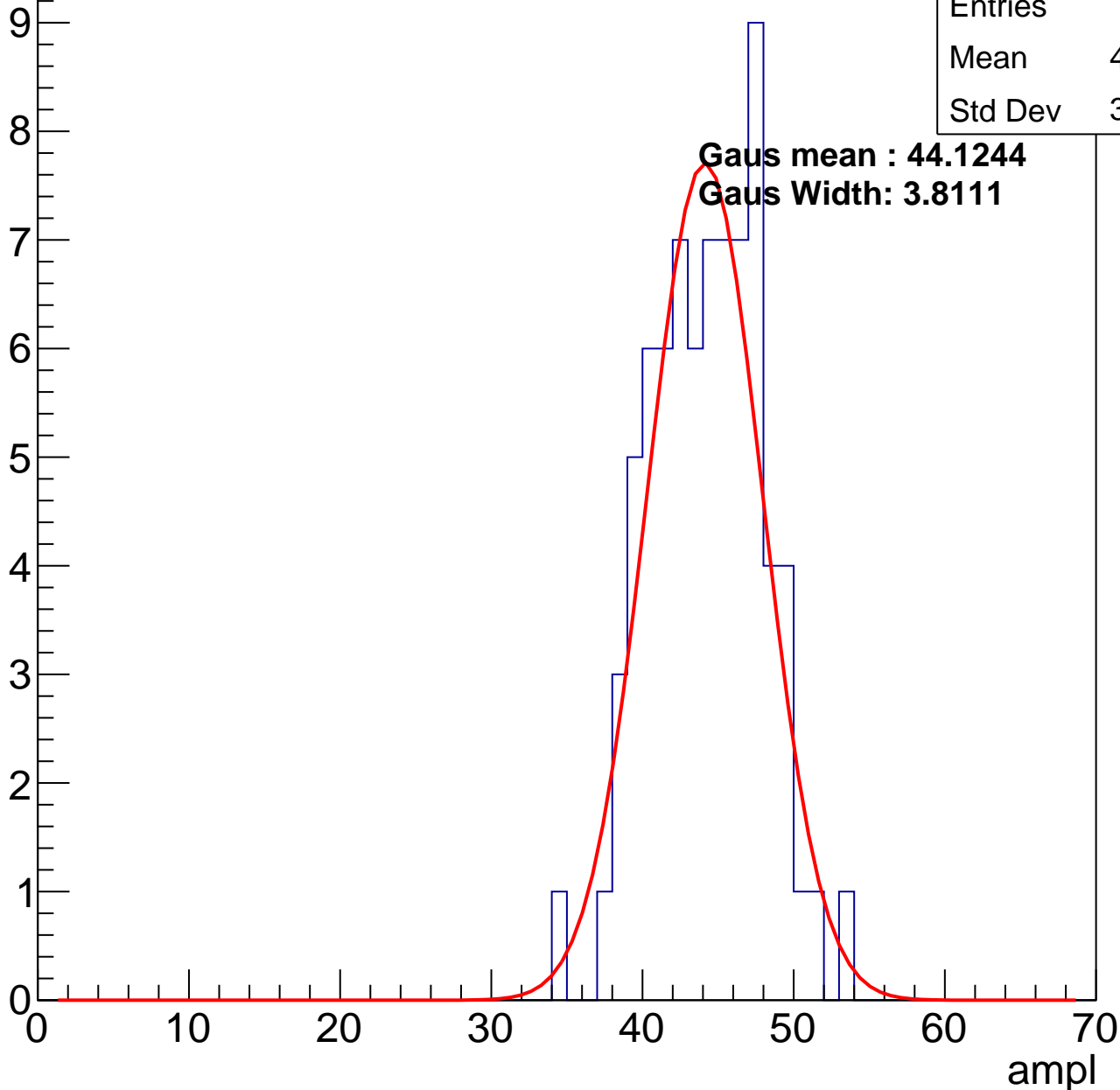
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	43.79
Std Dev	3.643

**Gaus mean : 44.1244**

**Gaus Width: 3.8111**

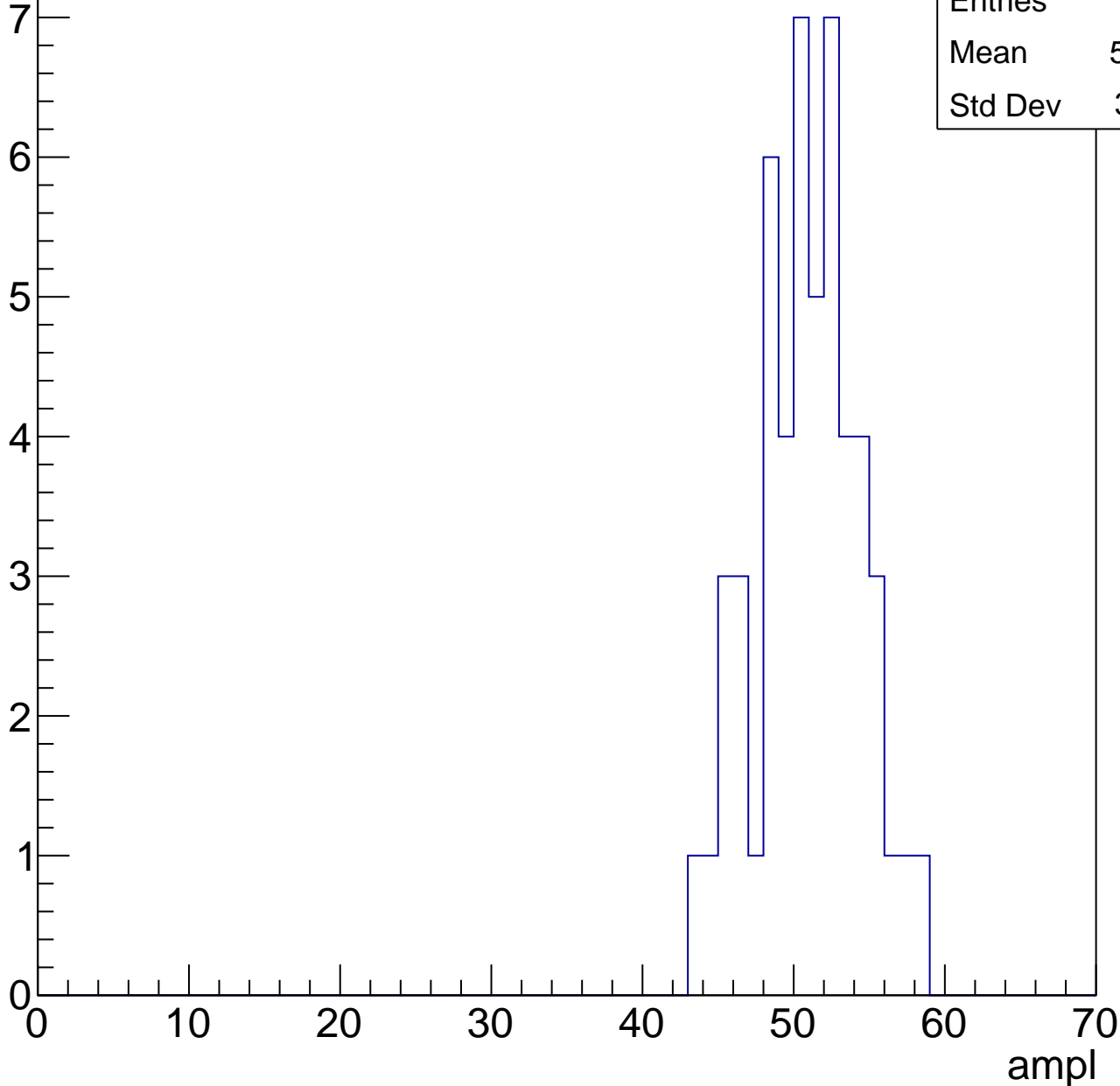


# B1L103S, U26-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	50.46
Std Dev	3.371

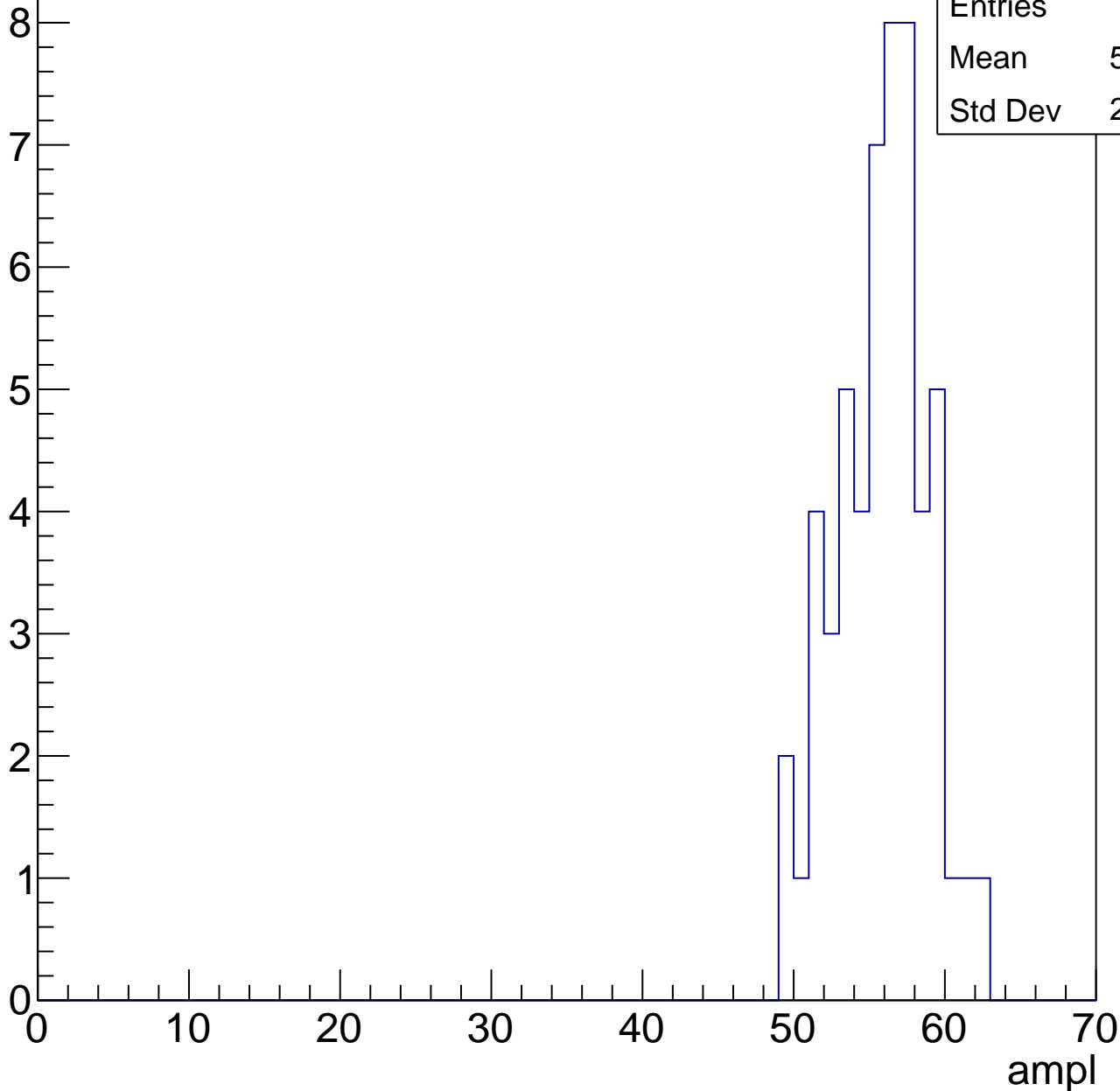


# B1L103S, U26-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	55.33
Std Dev	2.956

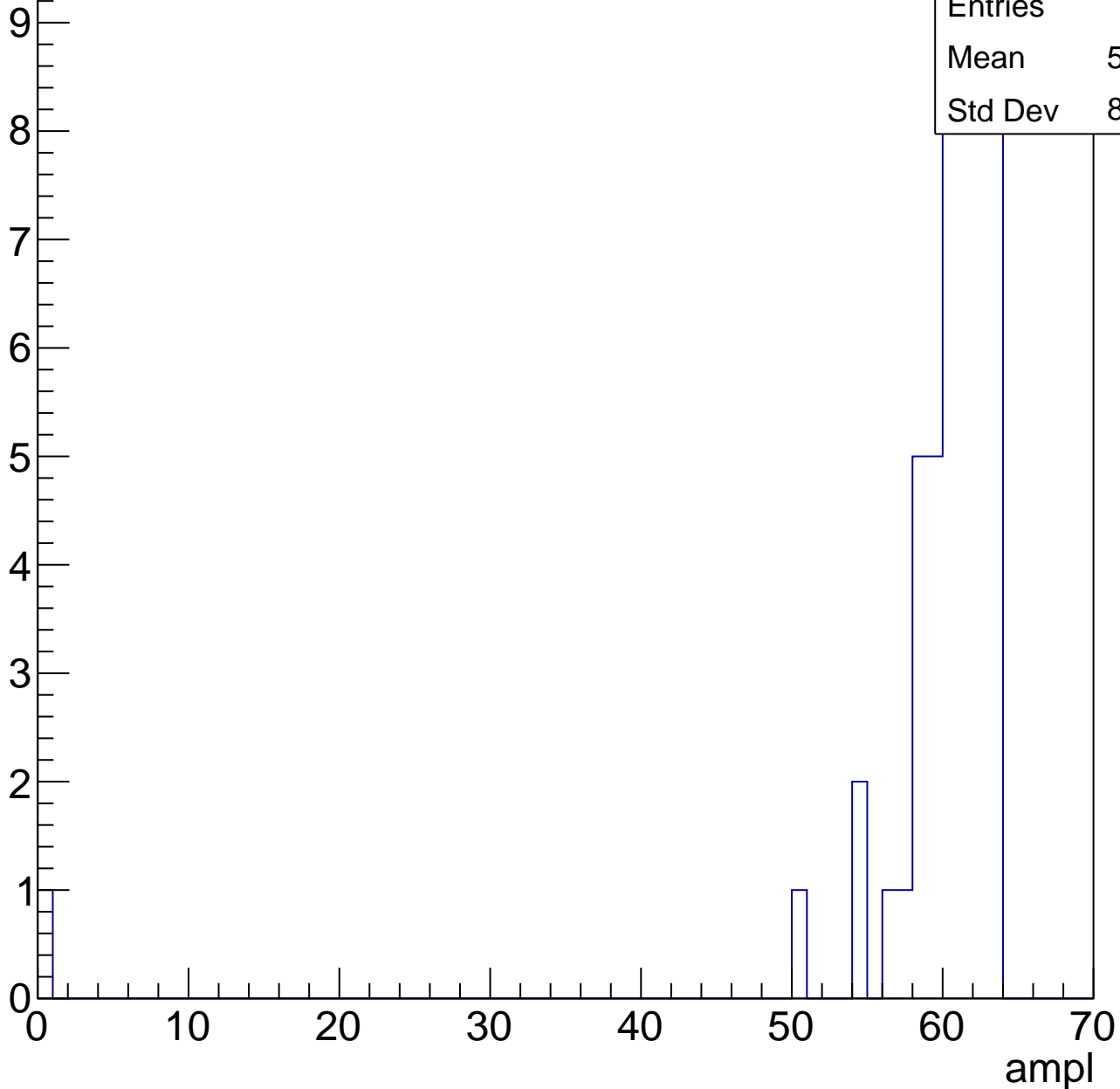


# B1L103S, U26-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	58.98
Std Dev	8.826



# B1L103S, U26-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

3

Mean

61.33

Std Dev

1.247



# B1L103S, U26-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	19
Std Dev	0

ampl

# B1L103S, U26-ch8, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	74
Mean	28.77
Std Dev	3.733

**Gaus mean : 28.9720**

**Gaus Width: 3.2528**

Entry

10  
8  
6  
4  
2  
0

ampl

0

10

20

30

40

50

60

70

# B1L103S, U26-ch8, adc1

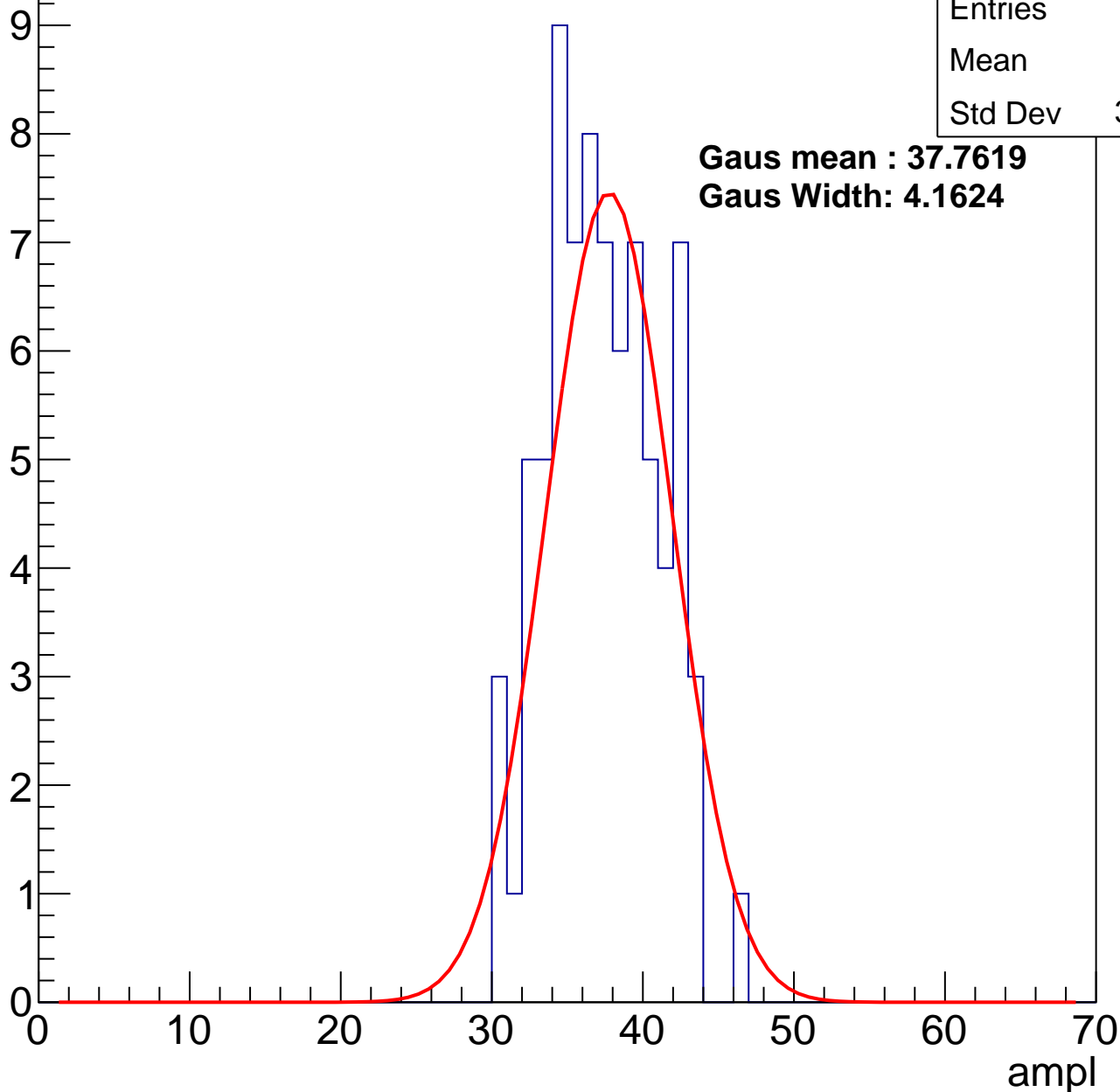
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	36.9
Std Dev	3.601

**Gaus mean : 37.7619**

**Gaus Width: 4.1624**



# B1L103S, U26-ch8, adc2

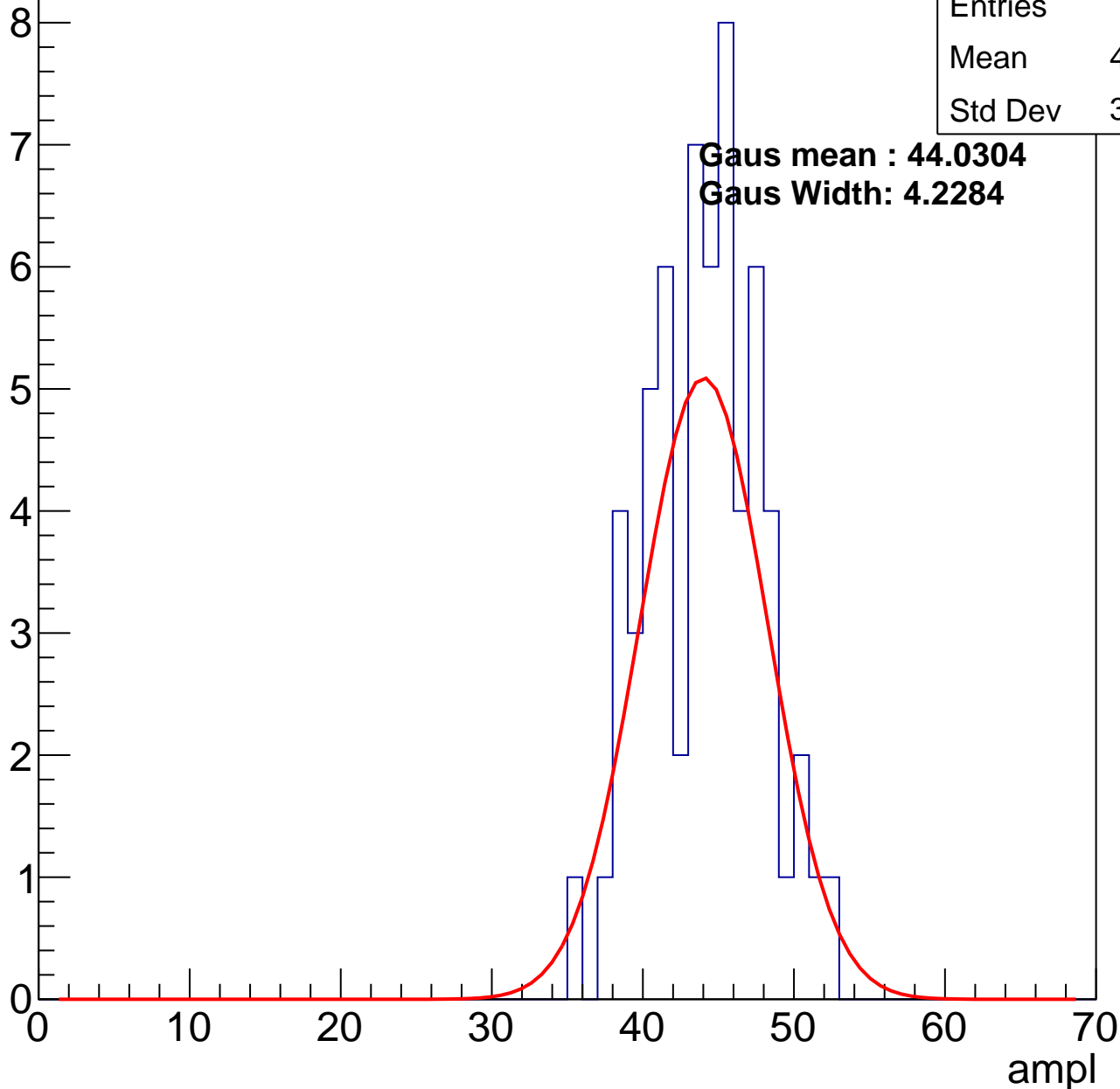
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	43.65
Std Dev	3.686

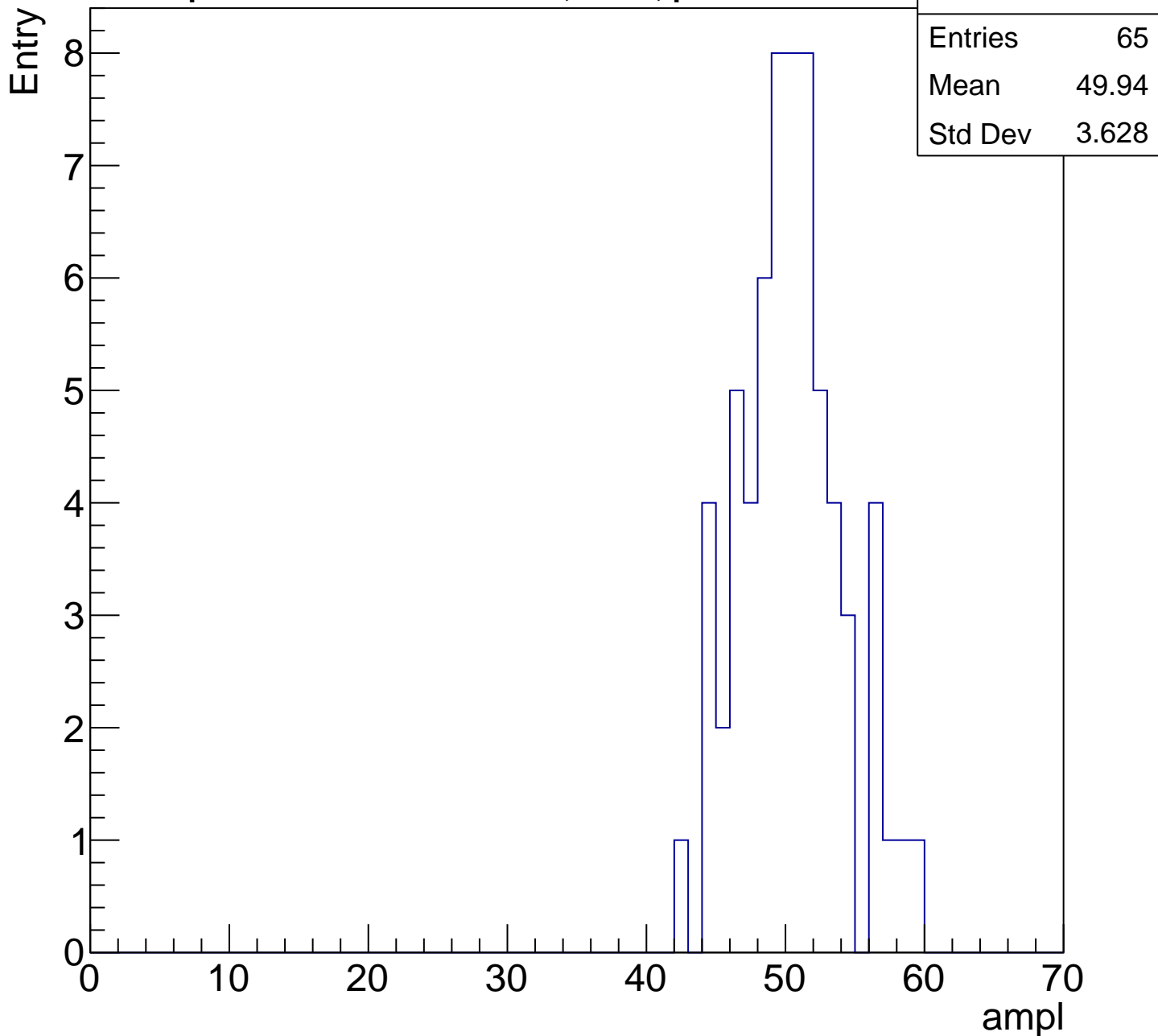
**Gaus mean : 44.0304**

**Gaus Width: 4.2284**



# B1L103S, U26-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

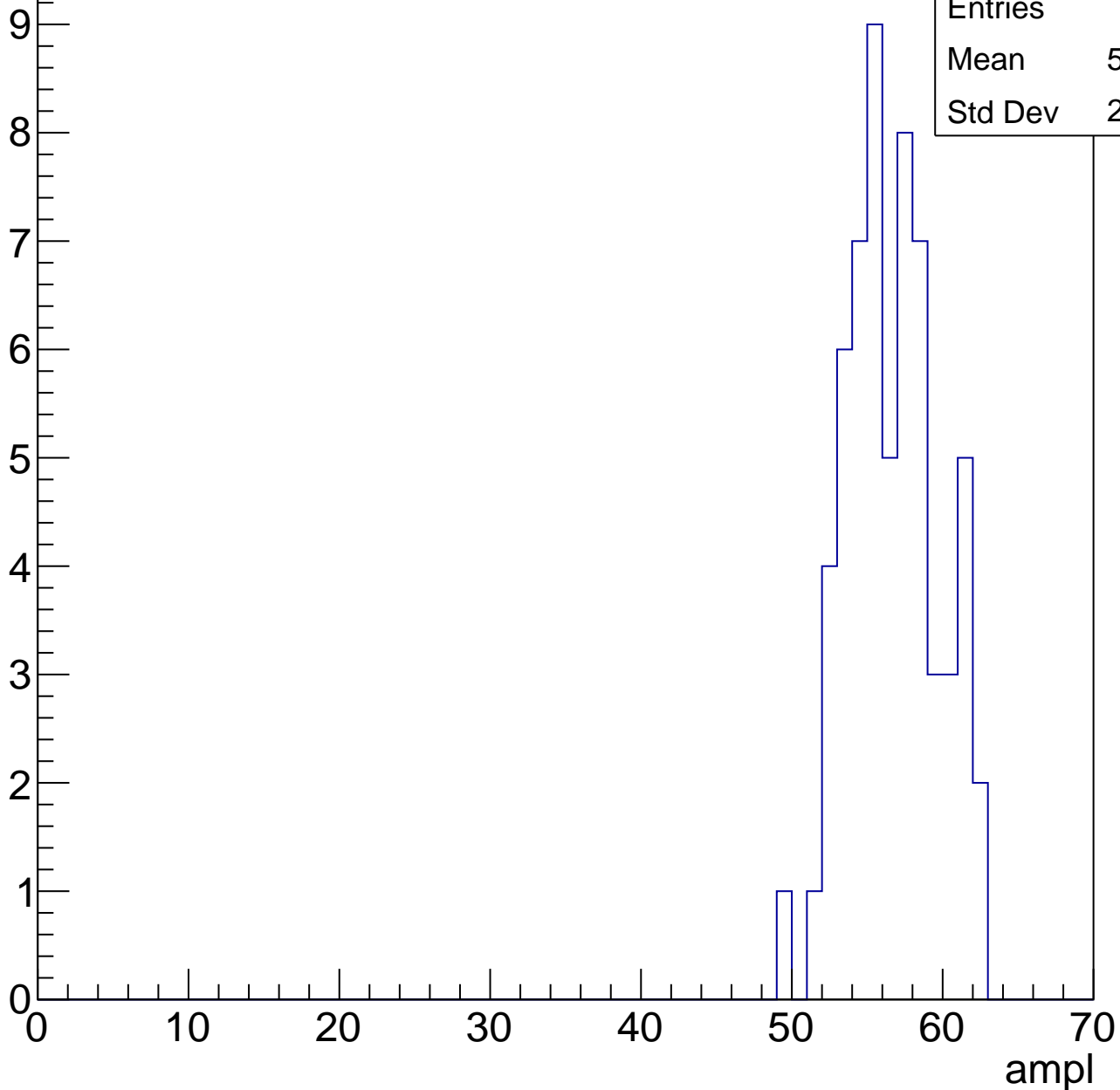


# B1L103S, U26-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	56.18
Std Dev	2.962

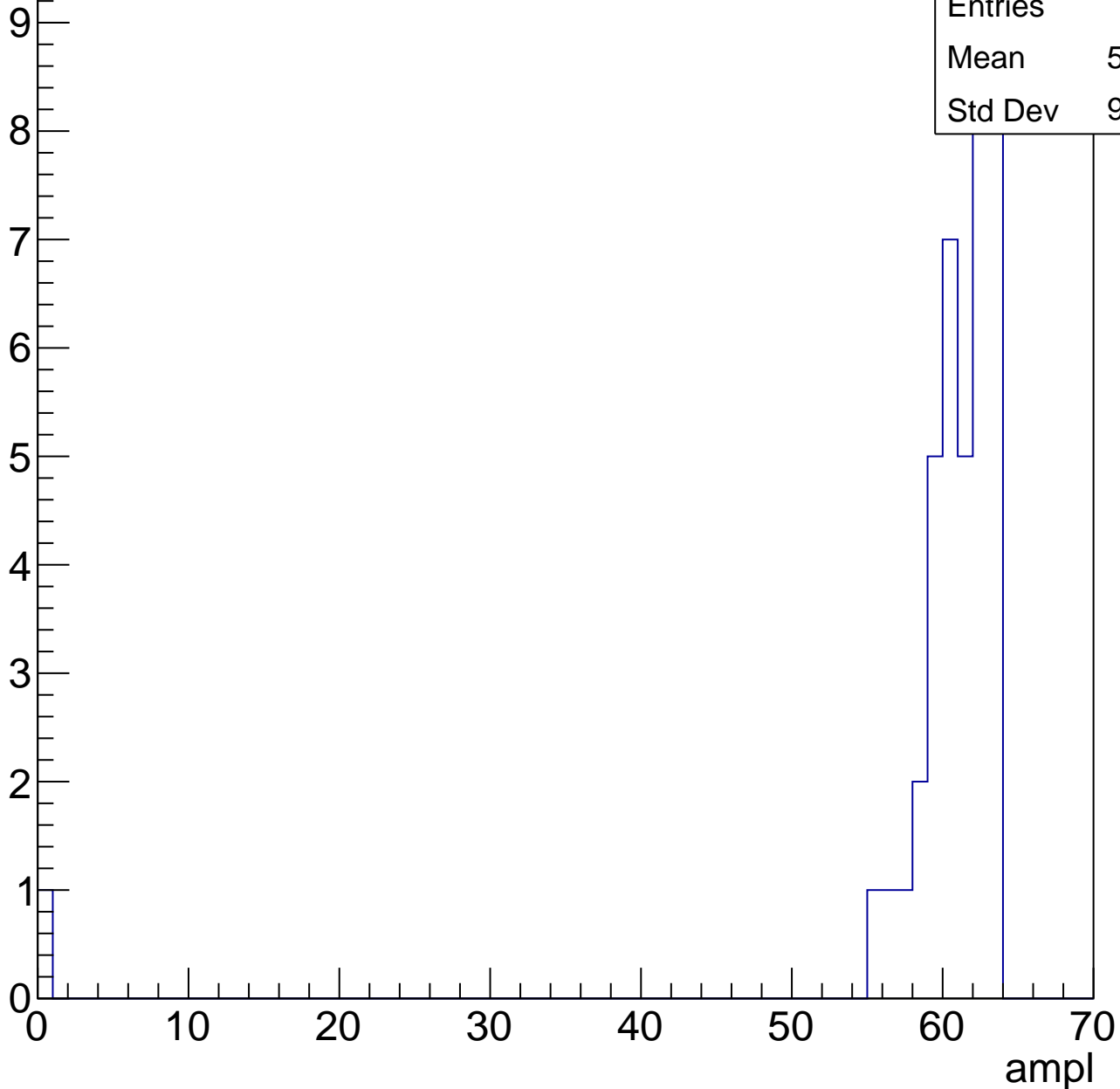


# B1L103S, U26-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	40
Mean	59.17
Std Dev	9.687



# B1L103S, U26-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

2

Mean

61

Std Dev

2



# B1L103S, U26-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U26-ch9, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	86
Mean	27.45
Std Dev	5.627

**Gaus mean : 28.1813**

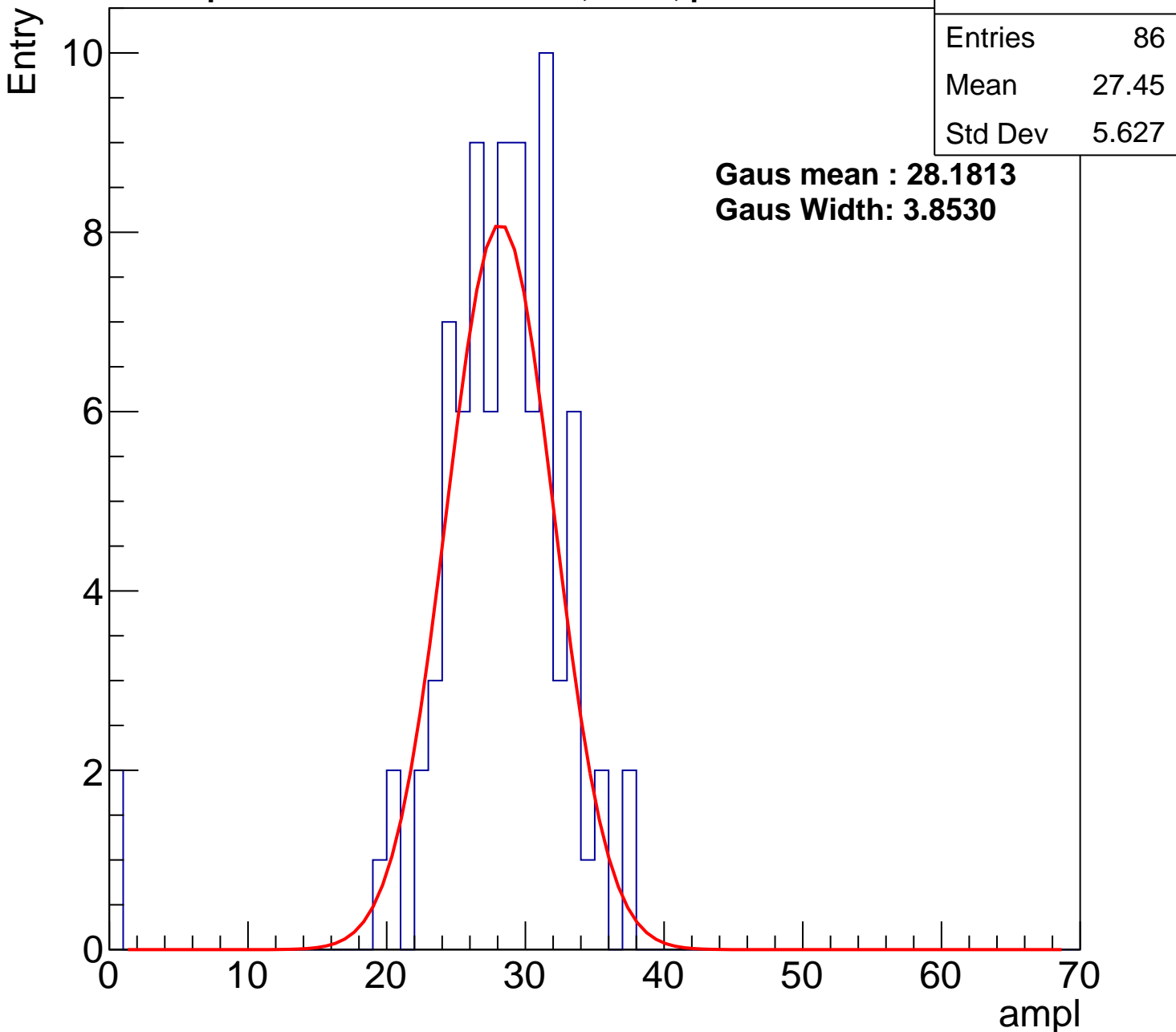
**Gaus Width: 3.8530**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch9, adc1

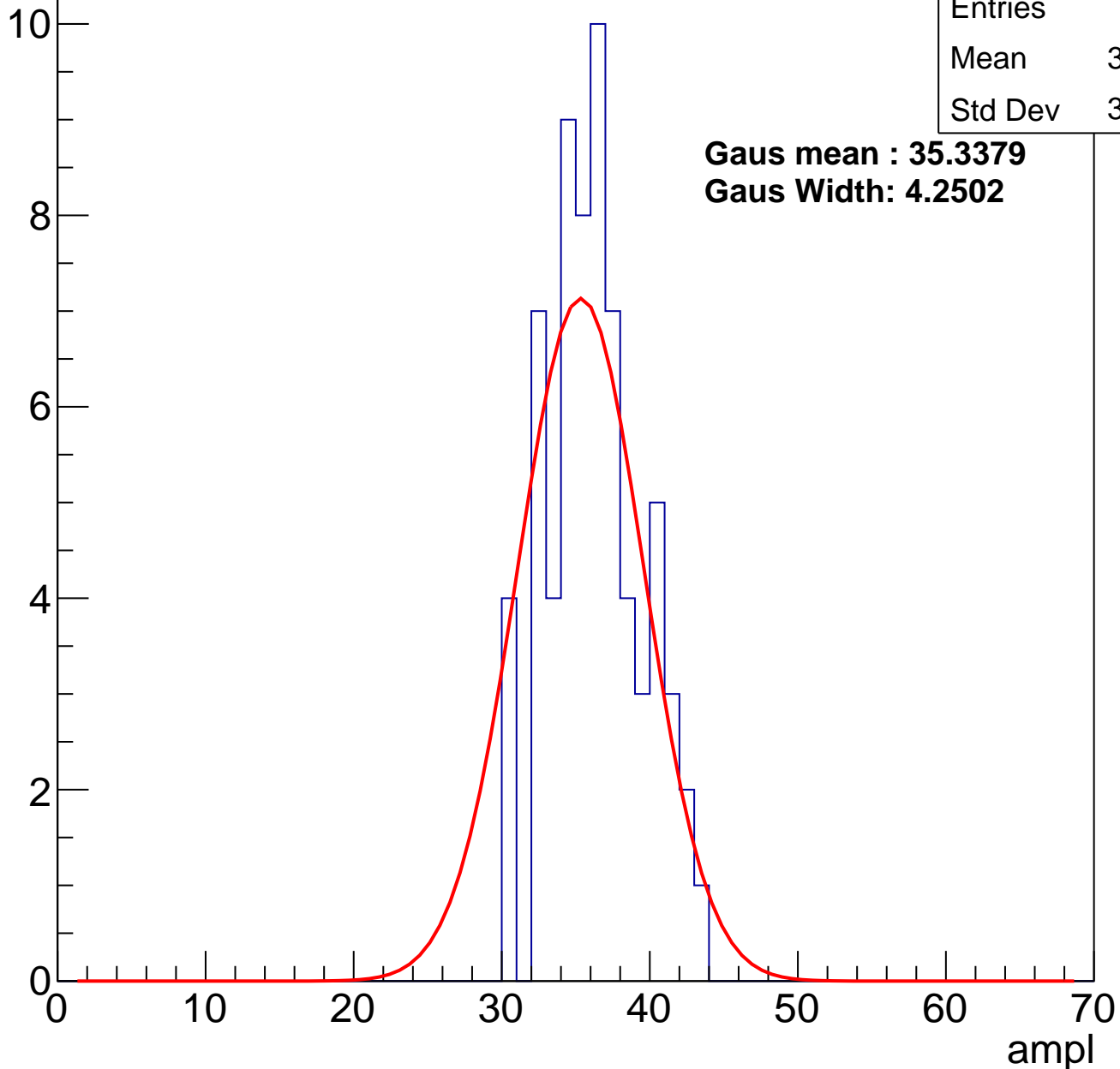
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	67
Mean	35.82
Std Dev	3.138

**Gaus mean : 35.3379**

**Gaus Width: 4.2502**

Entry



# B1L103S, U26-ch9, adc2

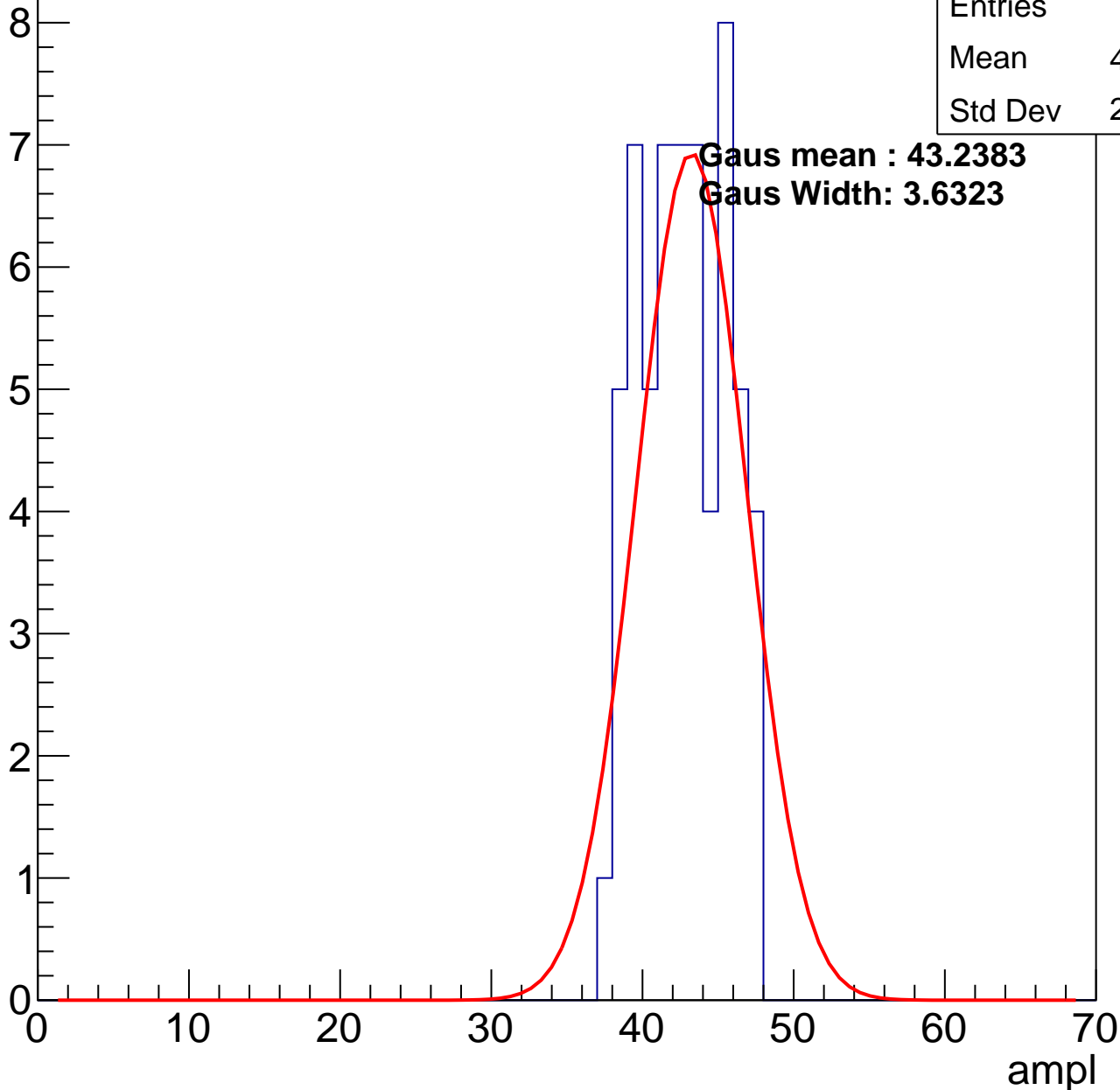
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	42.27
Std Dev	2.786

**Gaus mean : 43.2383**

**Gaus Width: 3.6323**

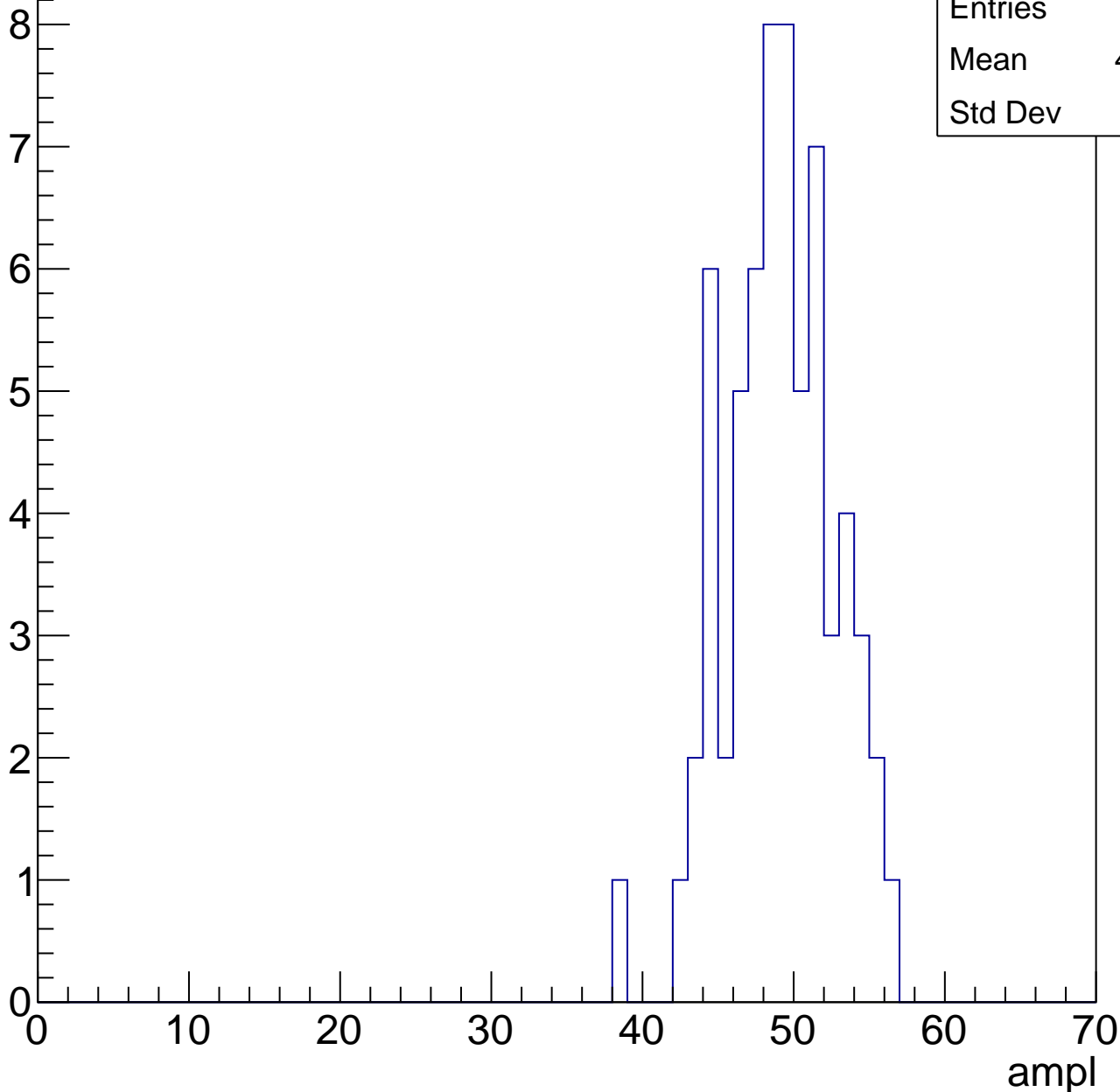


# B1L103S, U26-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

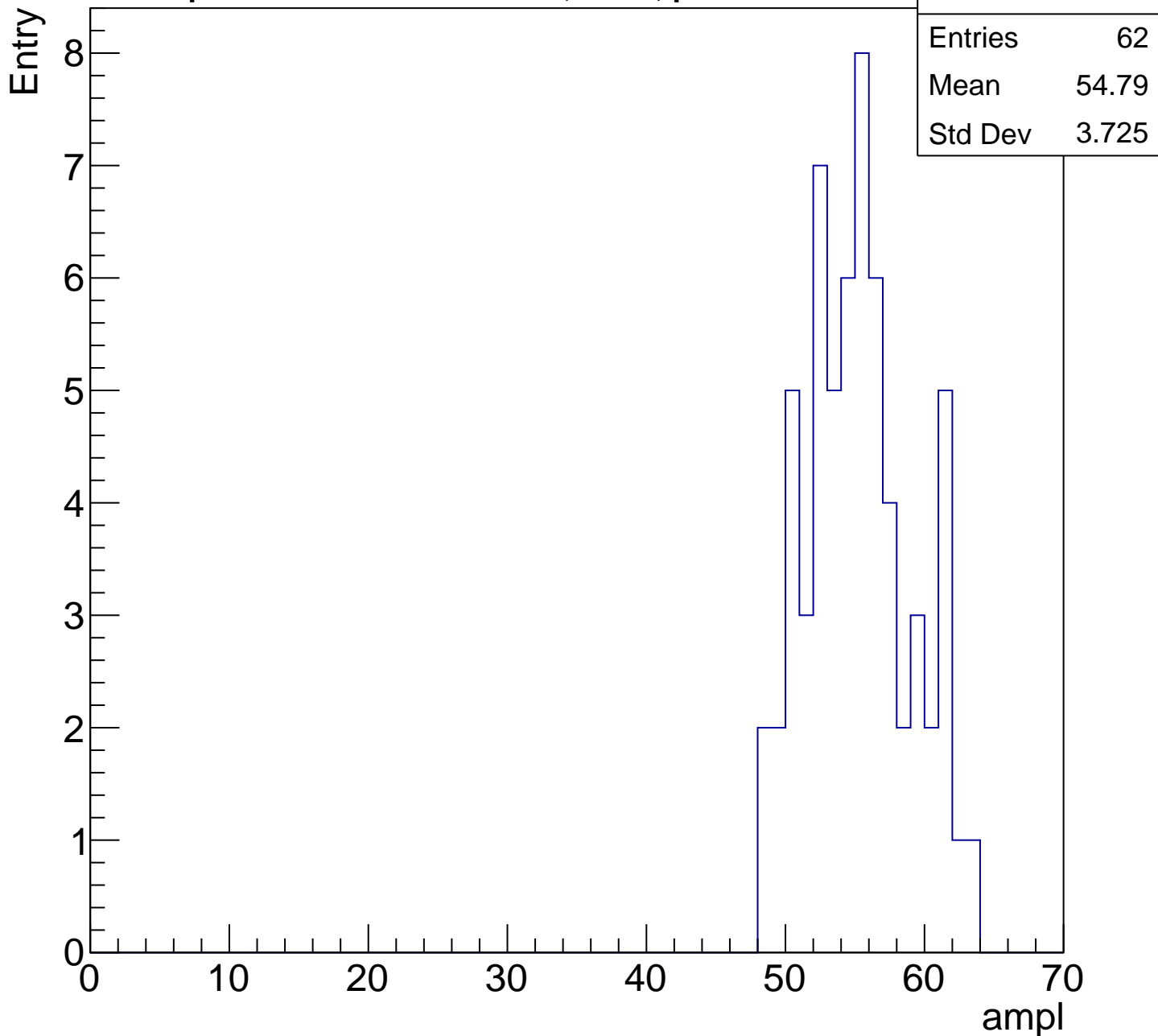
Entry

Entries	64
Mean	48.61
Std Dev	3.56



# B1L103S, U26-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

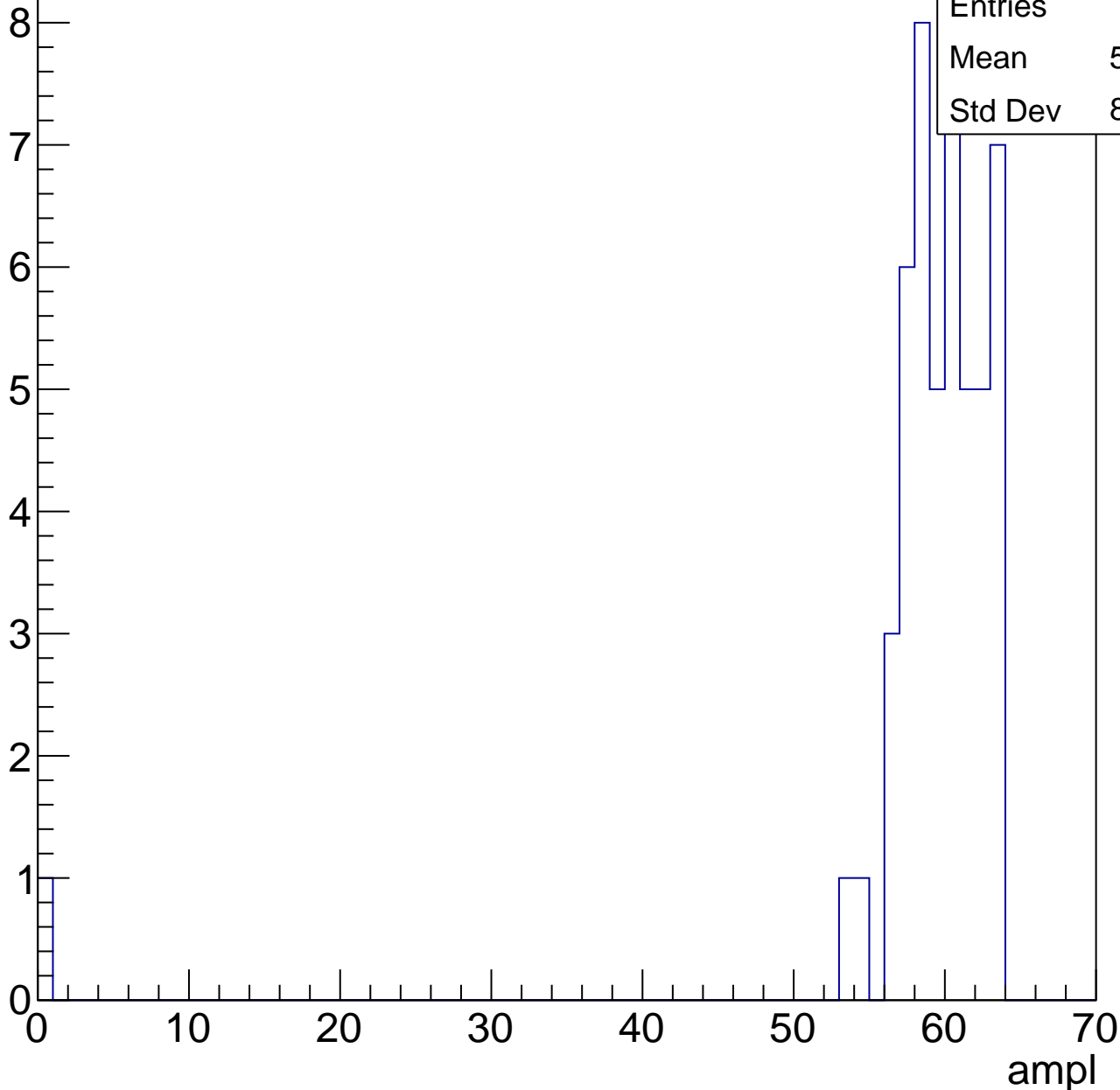


# B1L103S, U26-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

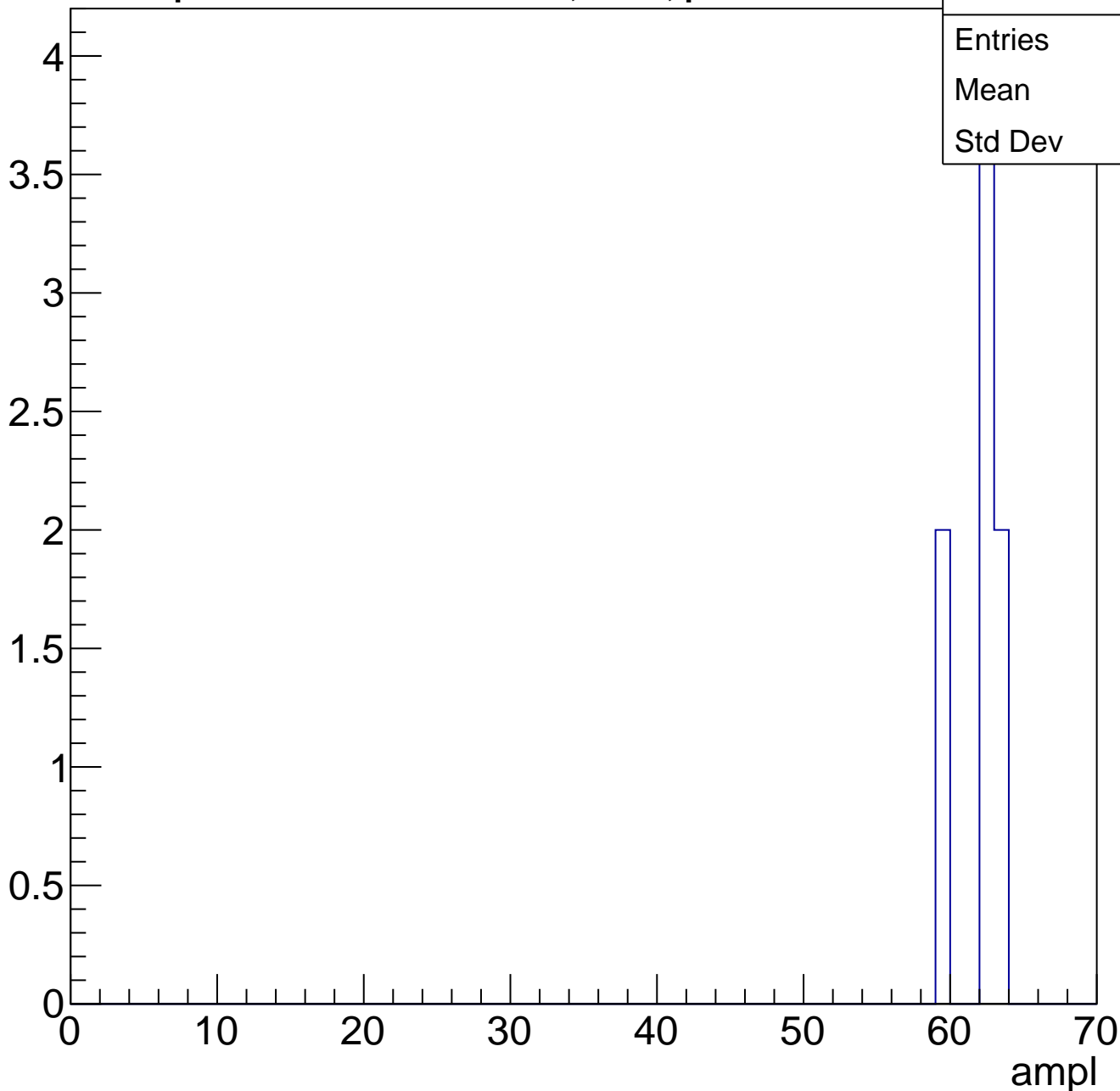
Entries	50
Mean	58.24
Std Dev	8.668



# B1L103S, U26-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U26-ch10, adc0

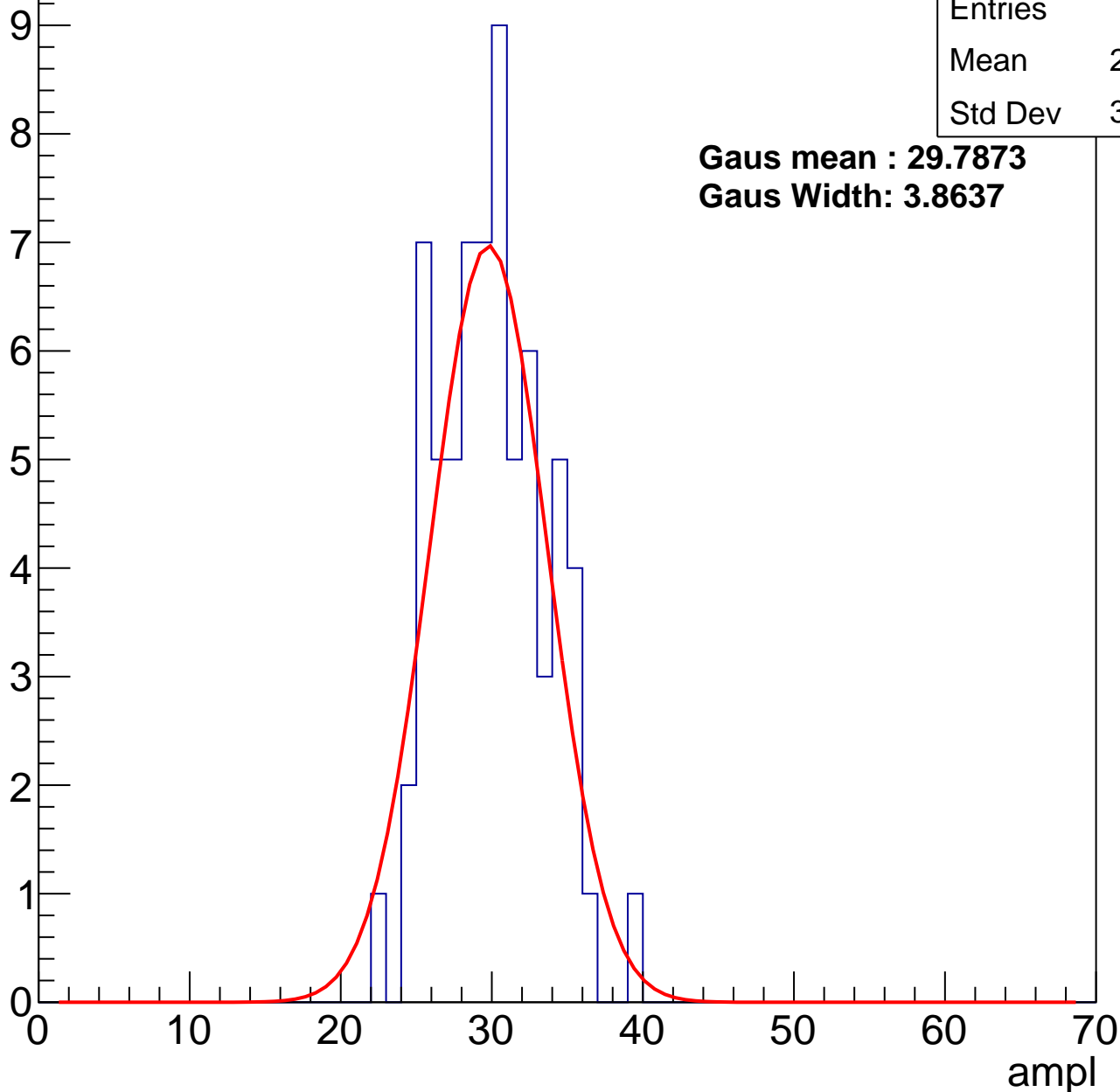
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	29.56
Std Dev	3.453

**Gaus mean : 29.7873**

**Gaus Width: 3.8637**



# B1L103S, U26-ch10, adc1

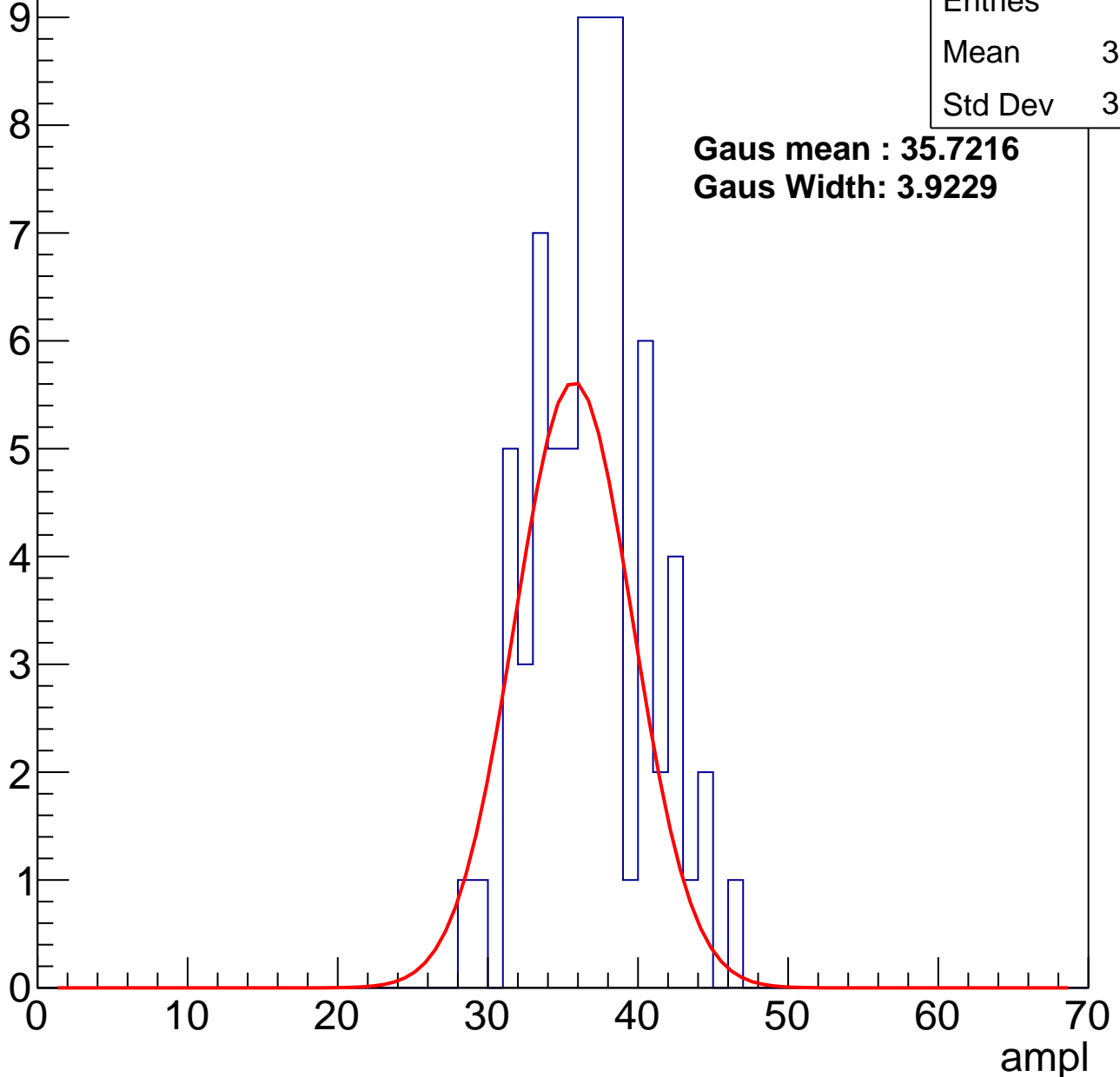
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	36.46
Std Dev	3.715

**Gaus mean : 35.7216**

**Gaus Width: 3.9229**



# B1L103S, U26-ch10, adc2

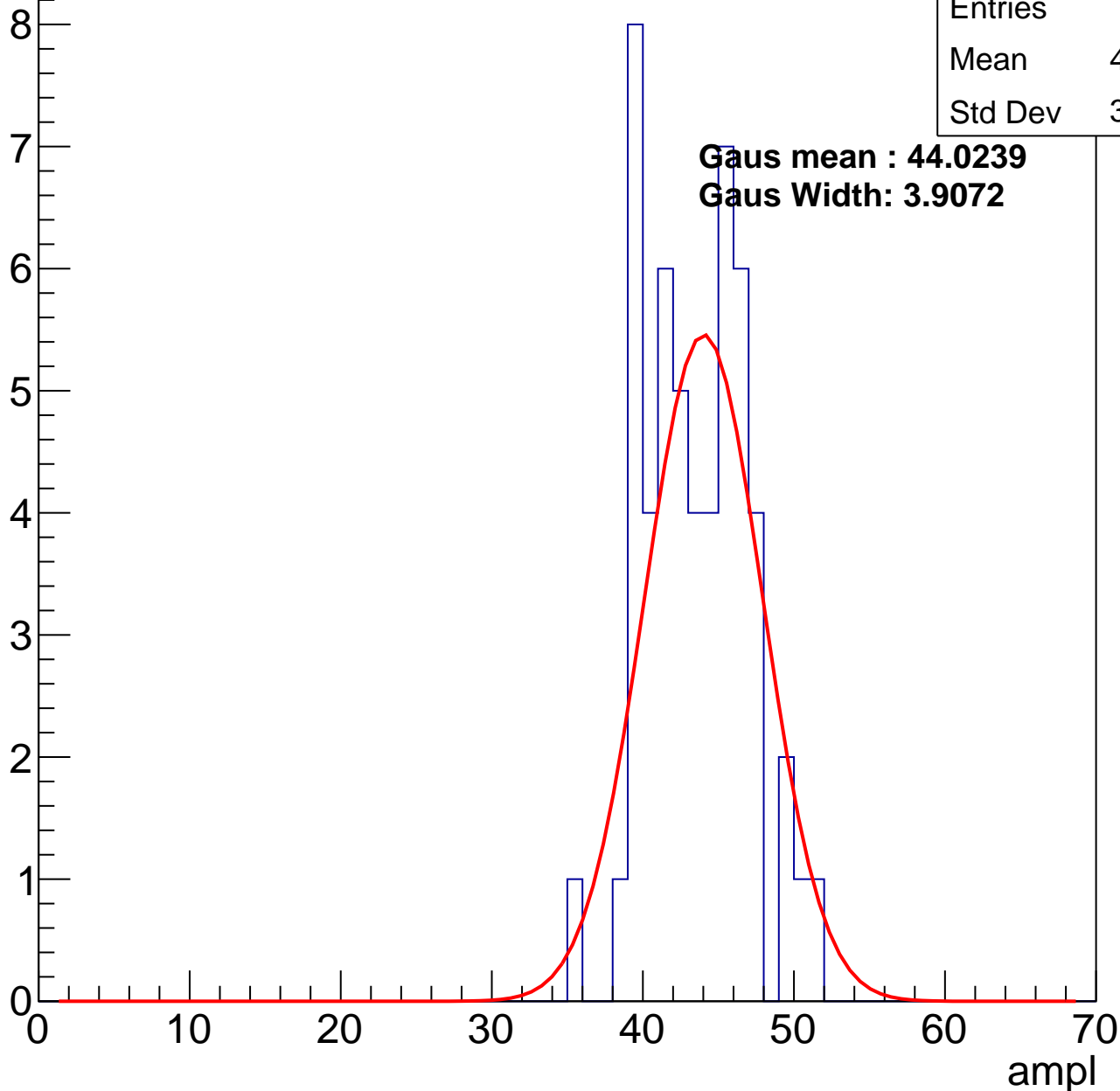
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	43.09
Std Dev	3.379

**Gaus mean : 44.0239**

**Gaus Width: 3.9072**

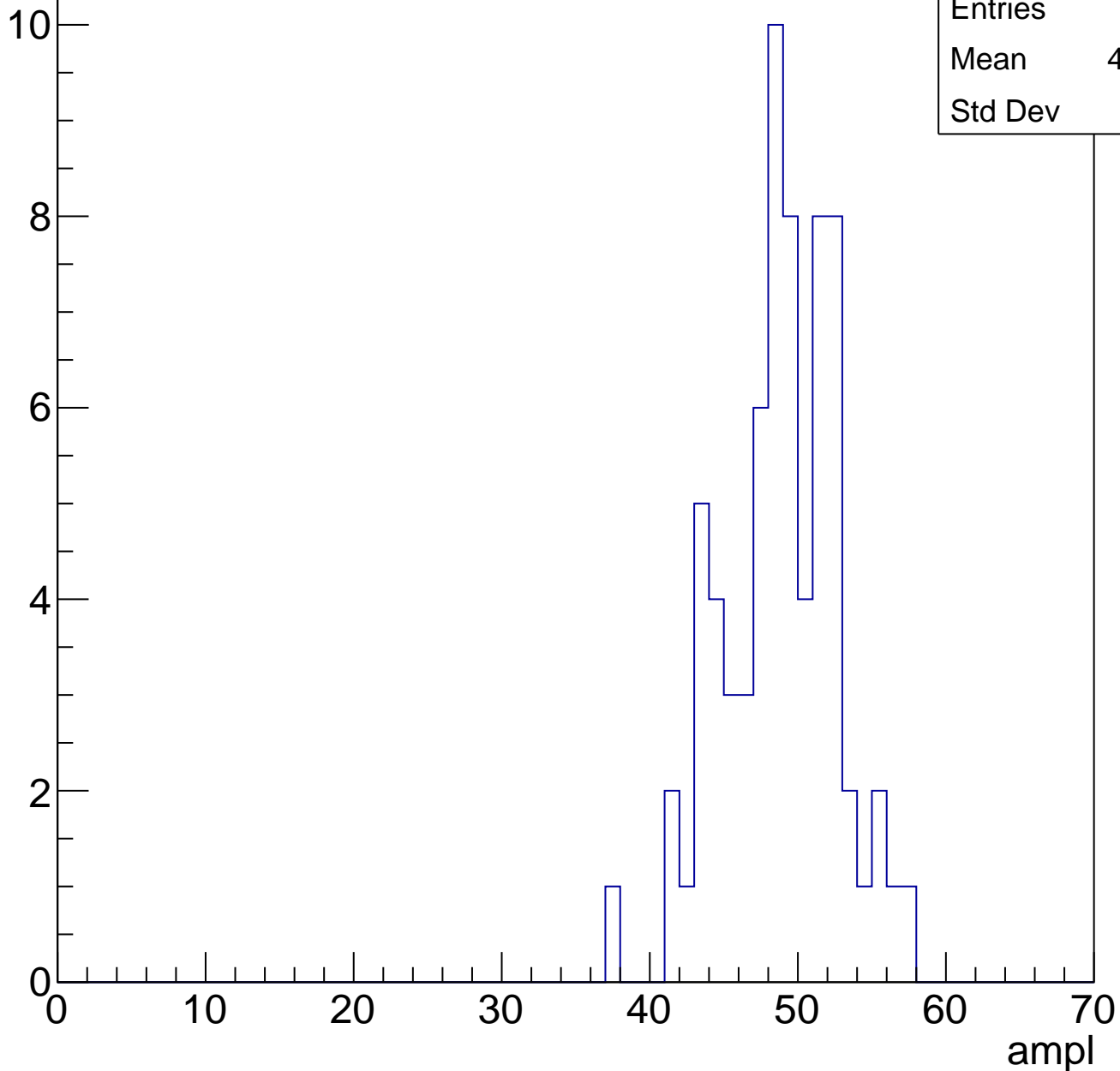


# B1L103S, U26-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

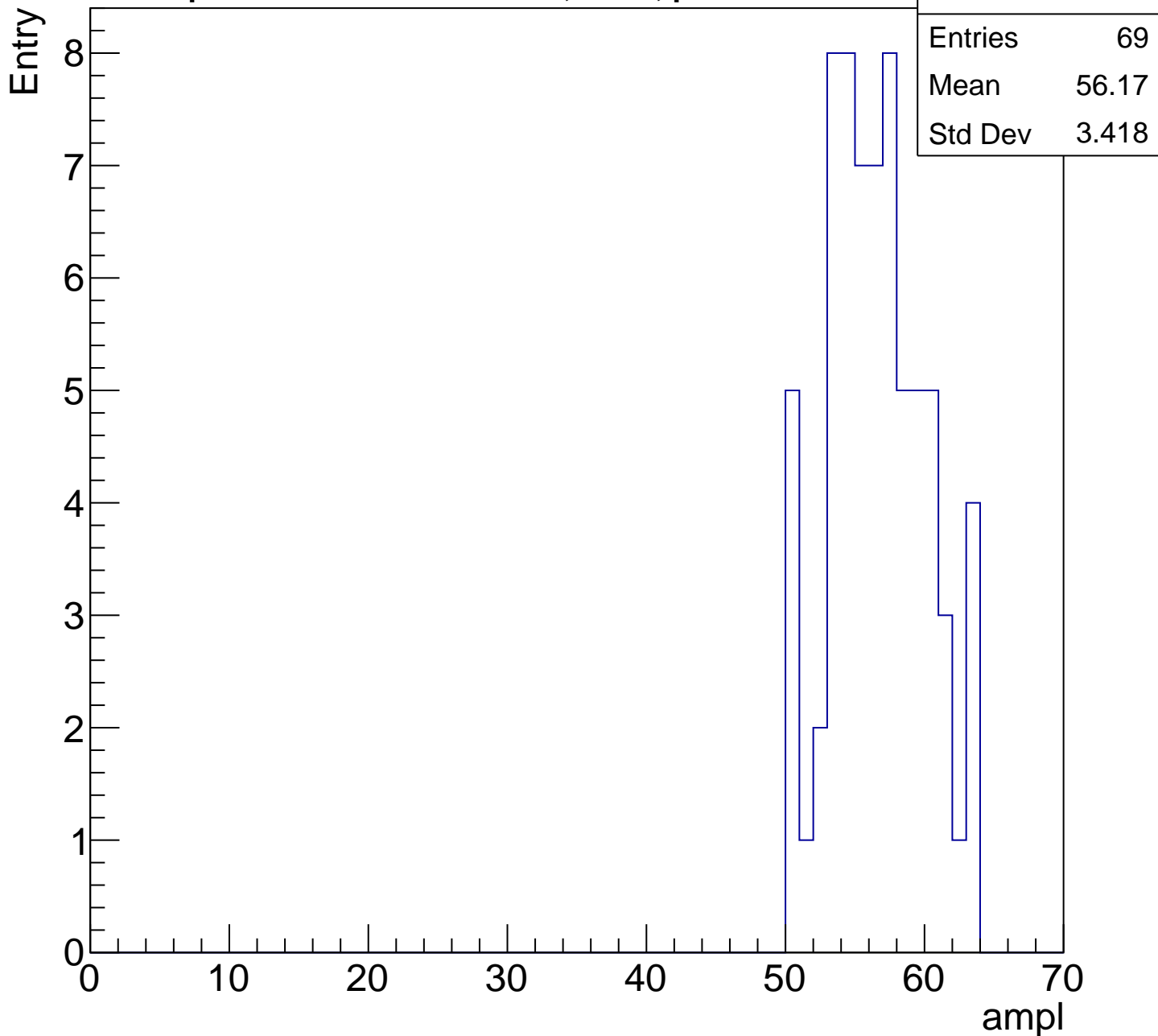
Entries	70
Mean	48.37
Std Dev	3.84

Entry



# B1L103S, U26-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

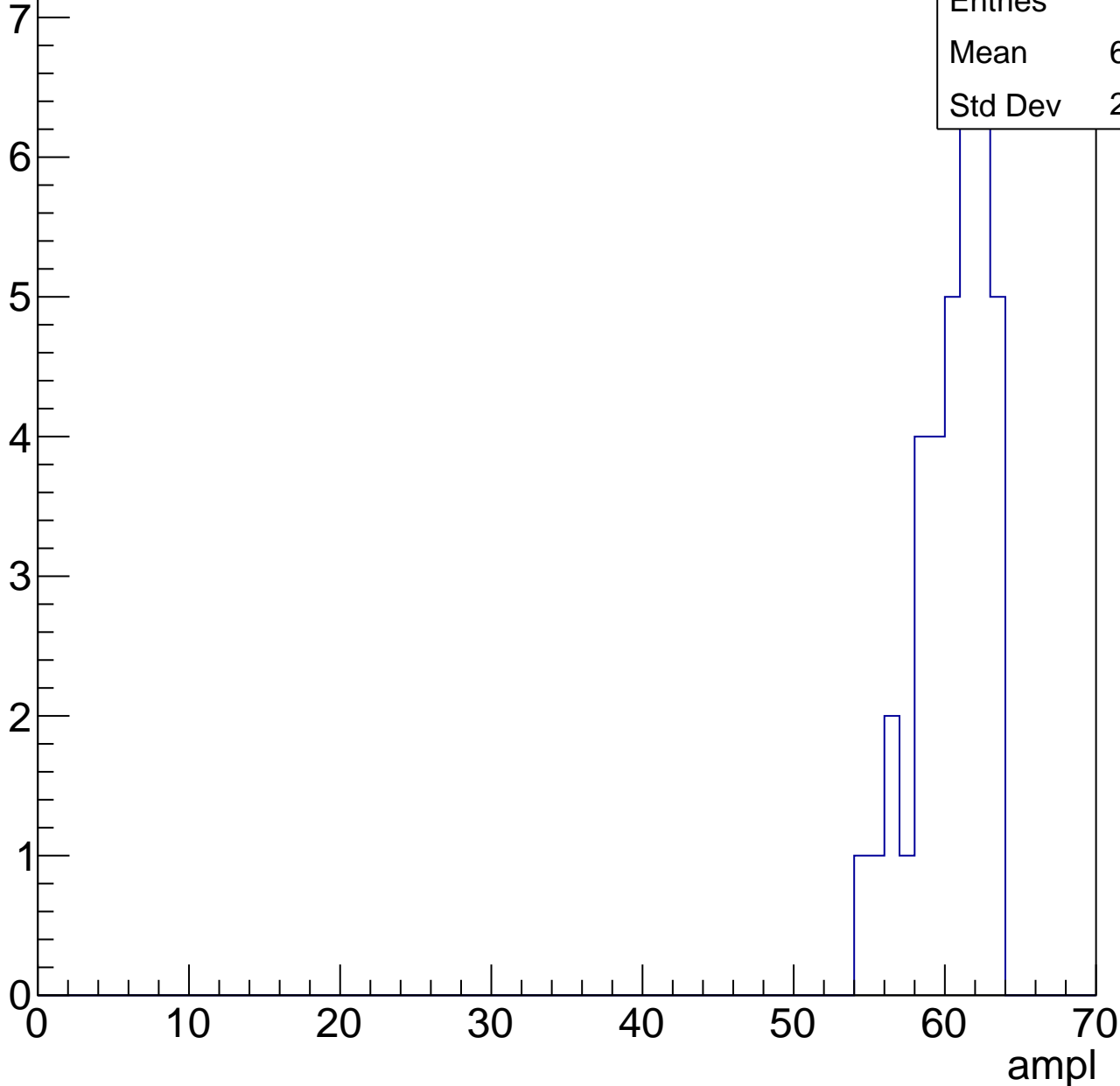


# B1L103S, U26-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	37
Mean	60.05
Std Dev	2.336



# B1L103S, U26-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

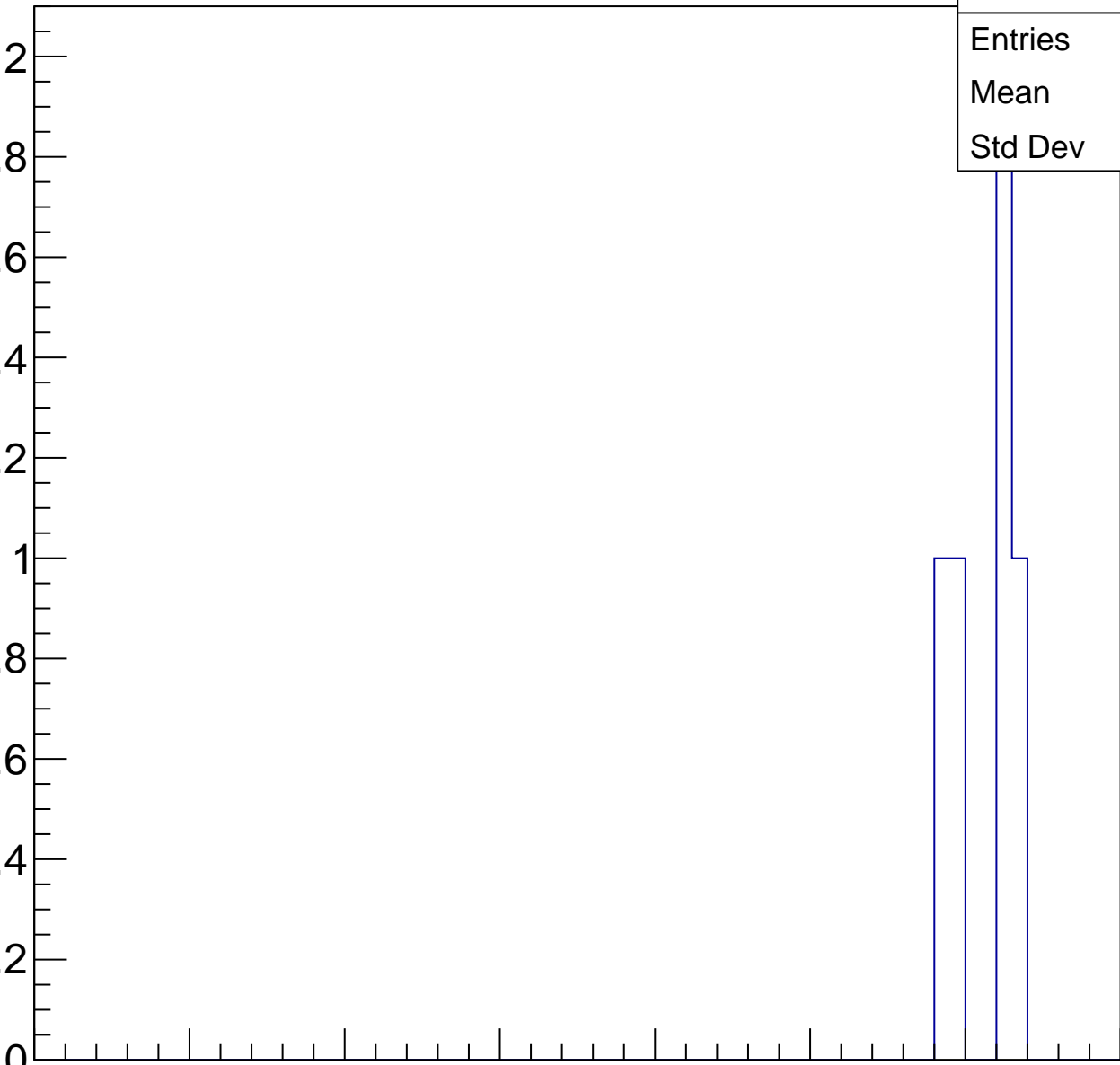
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	60.8
Std Dev	1.939

0 10 20 30 40 50 60 70

ampl





# B1L103S, U26-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch11, adc0

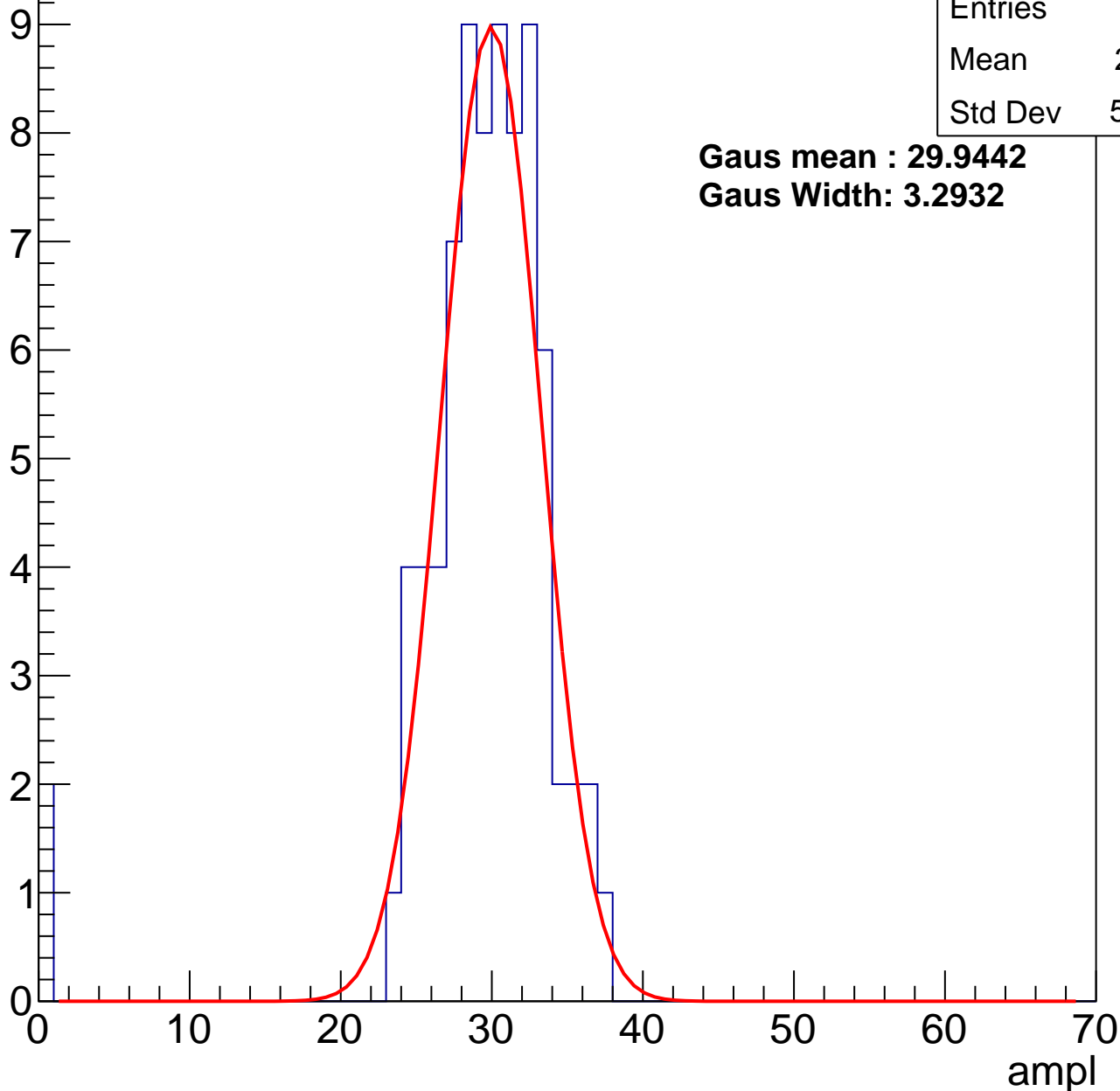
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	28.81
Std Dev	5.609

**Gaus mean : 29.9442**

**Gaus Width: 3.2932**



# B1L103S, U26-ch11, adc1

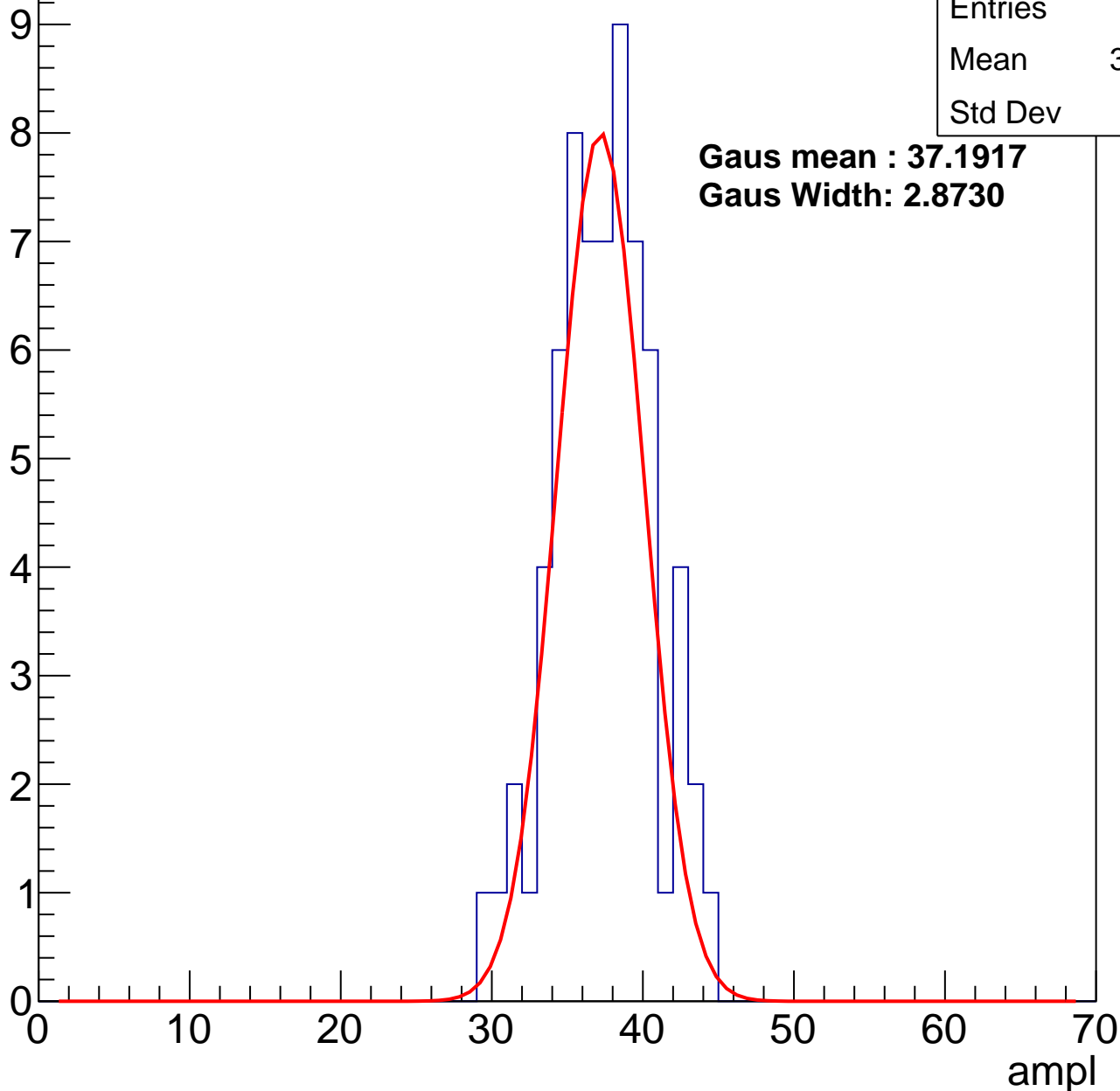
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	36.93
Std Dev	3.22

**Gaus mean : 37.1917**

**Gaus Width: 2.8730**



# B1L103S, U26-ch11, adc2

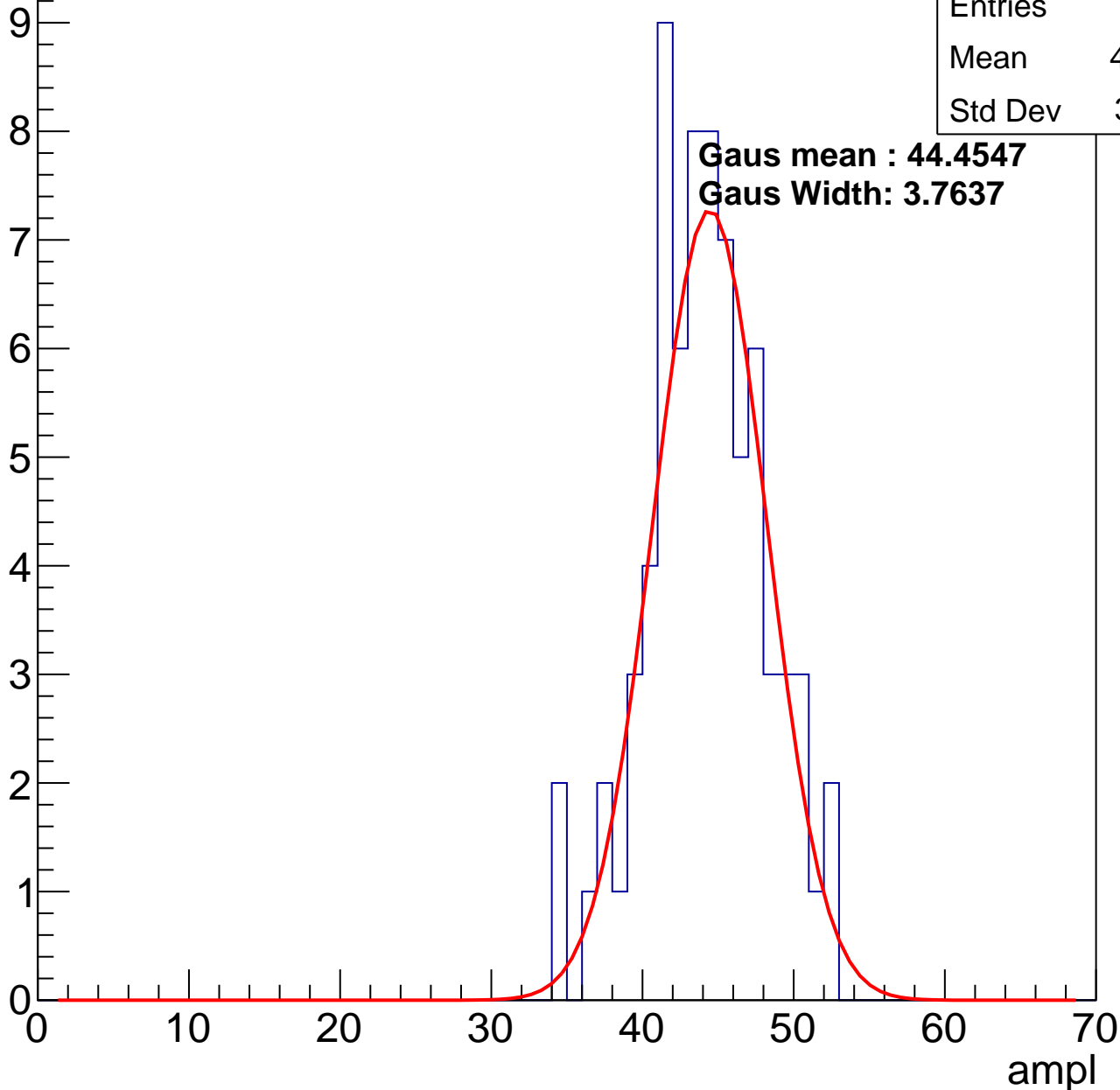
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	43.69
Std Dev	3.911

**Gaus mean : 44.4547**

**Gaus Width: 3.7637**

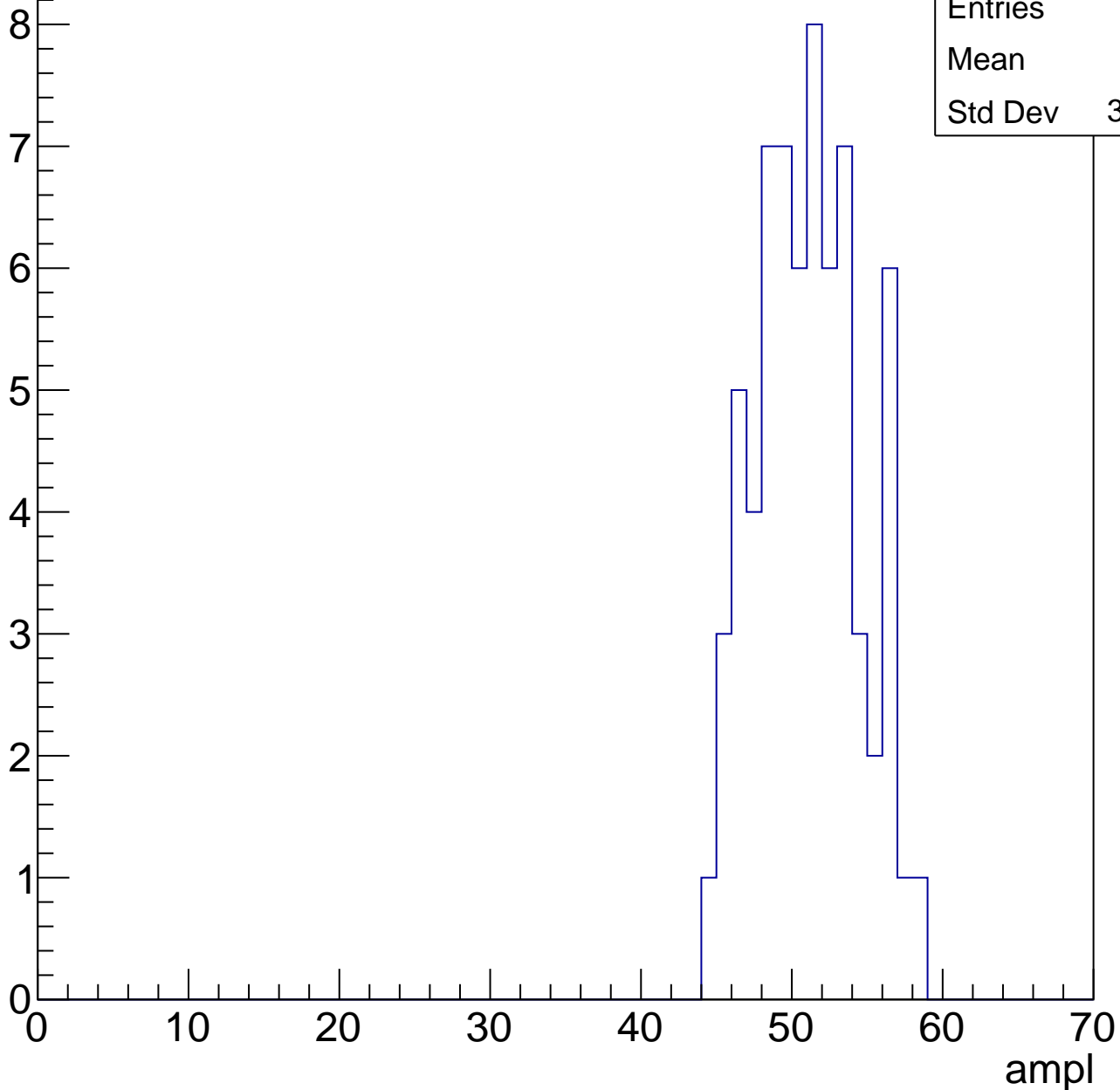


# B1L103S, U26-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	50.6
Std Dev	3.368

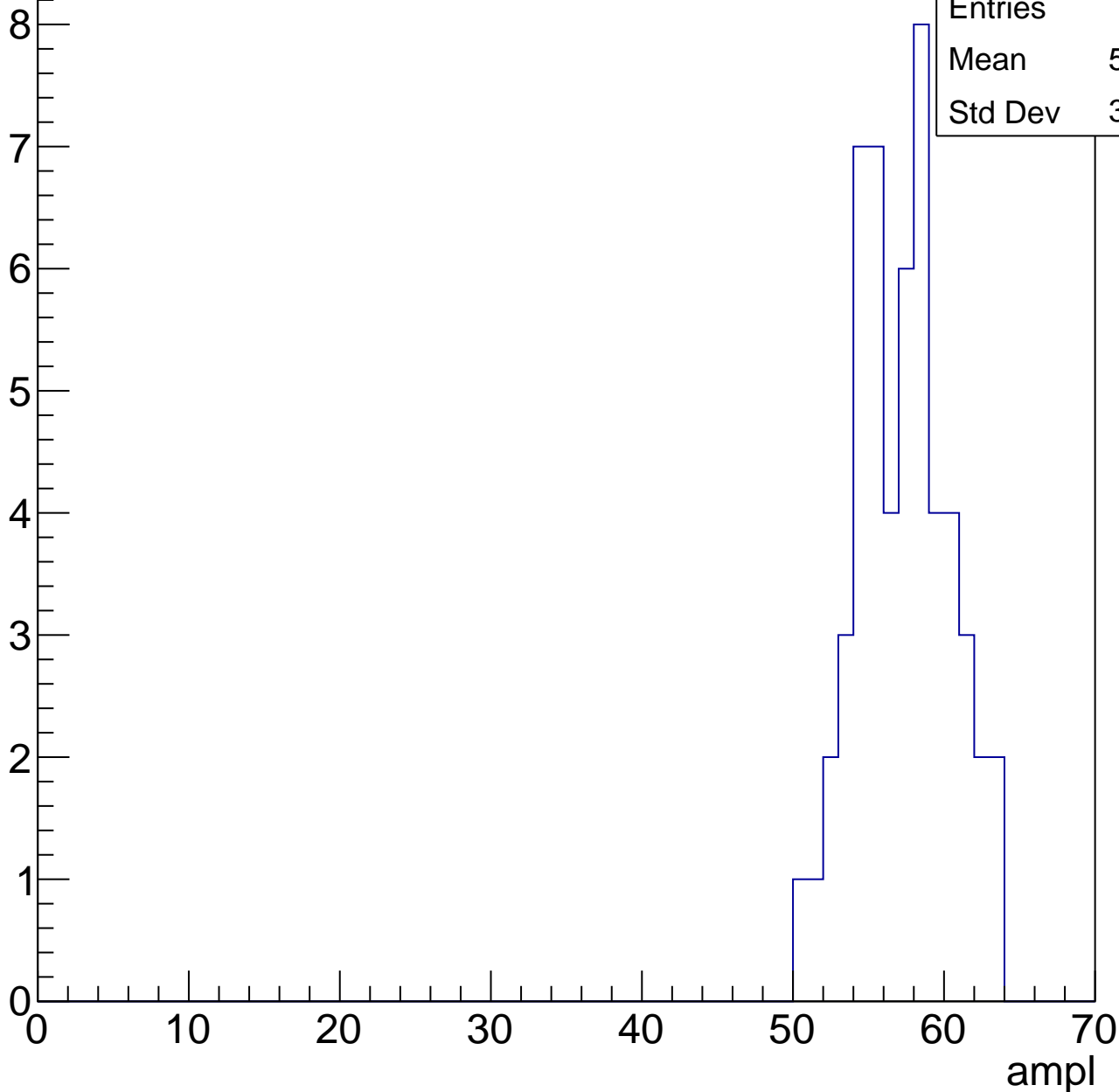


# B1L103S, U26-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	56.78
Std Dev	3.059

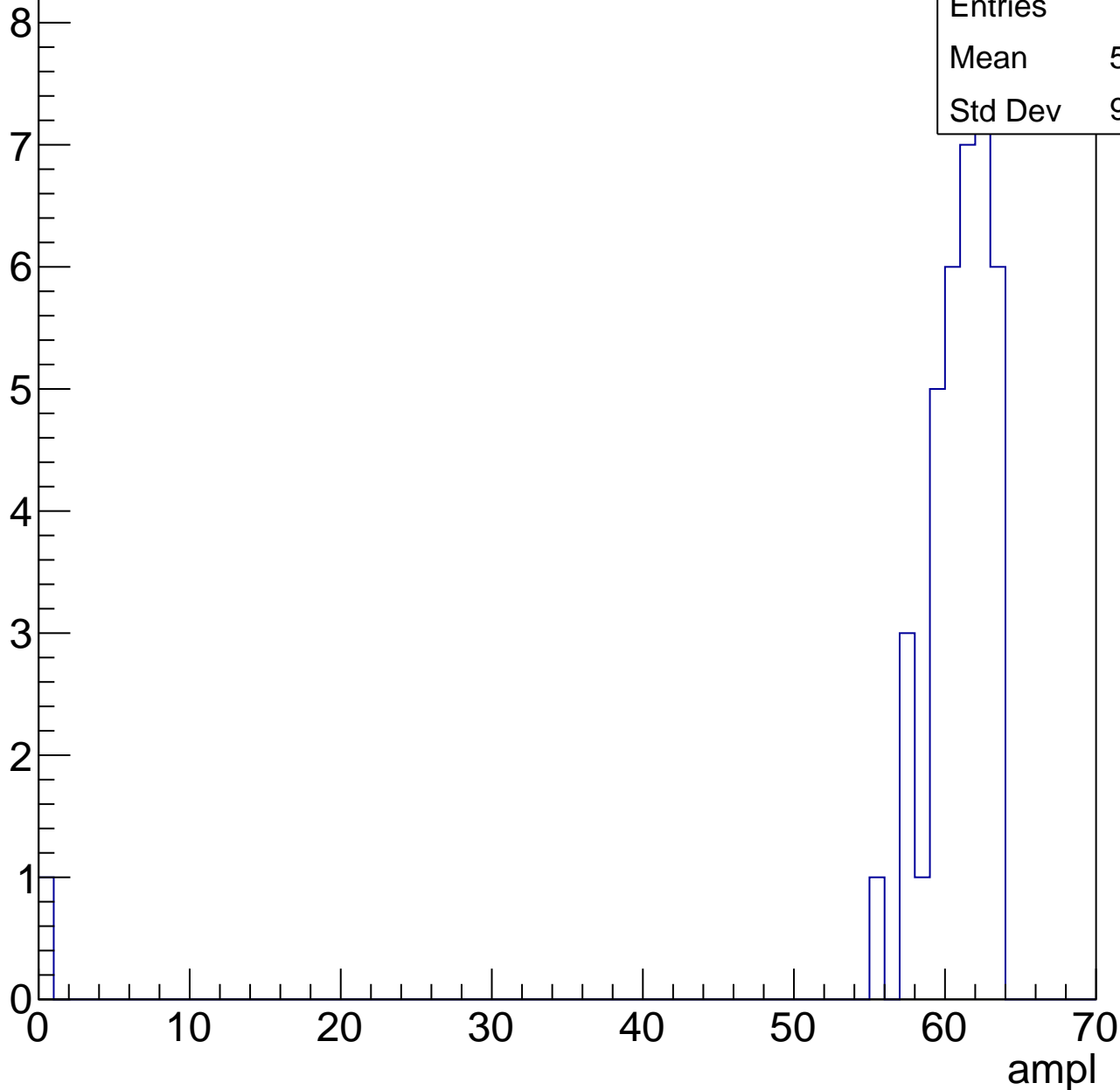


# B1L103S, U26-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	38
Mean	58.95
Std Dev	9.883



# B1L103S, U26-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L103S, U26-ch12, adc0

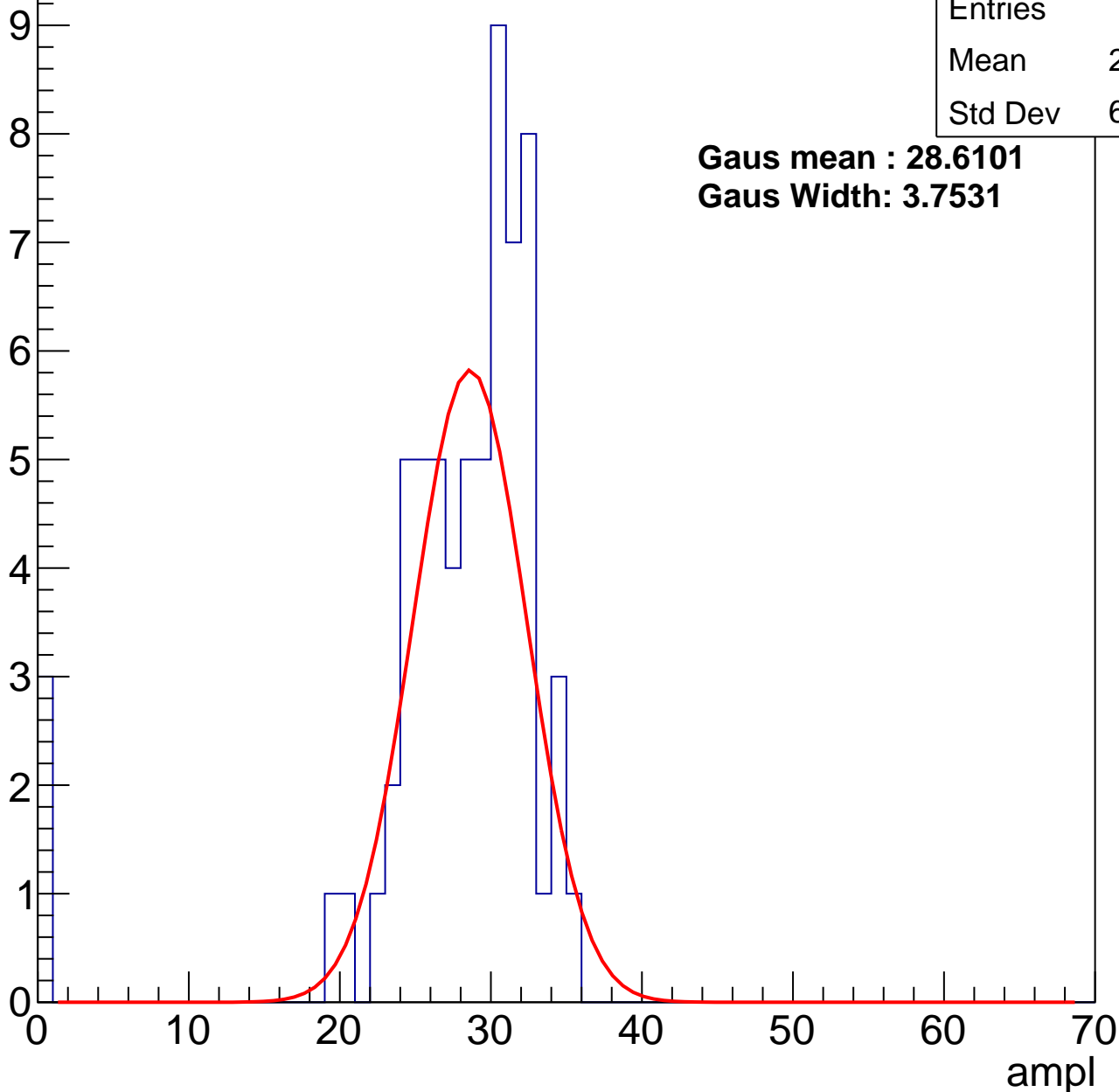
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	27.09
Std Dev	6.844

**Gaus mean : 28.6101**

**Gaus Width: 3.7531**



# B1L103S, U26-ch12, adc1

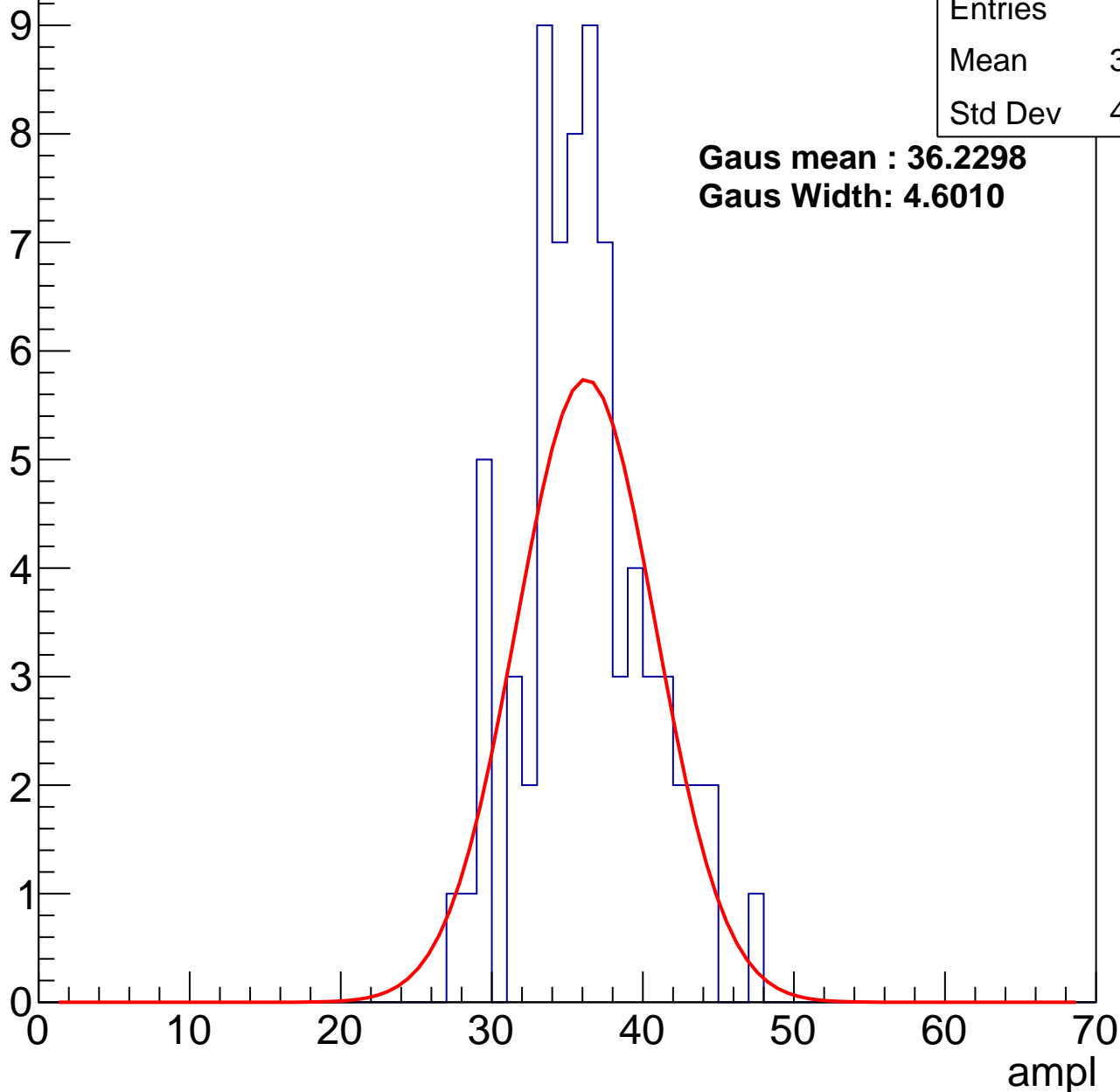
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	35.74
Std Dev	4.093

**Gaus mean : 36.2298**

**Gaus Width: 4.6010**



# B1L103S, U26-ch12, adc2

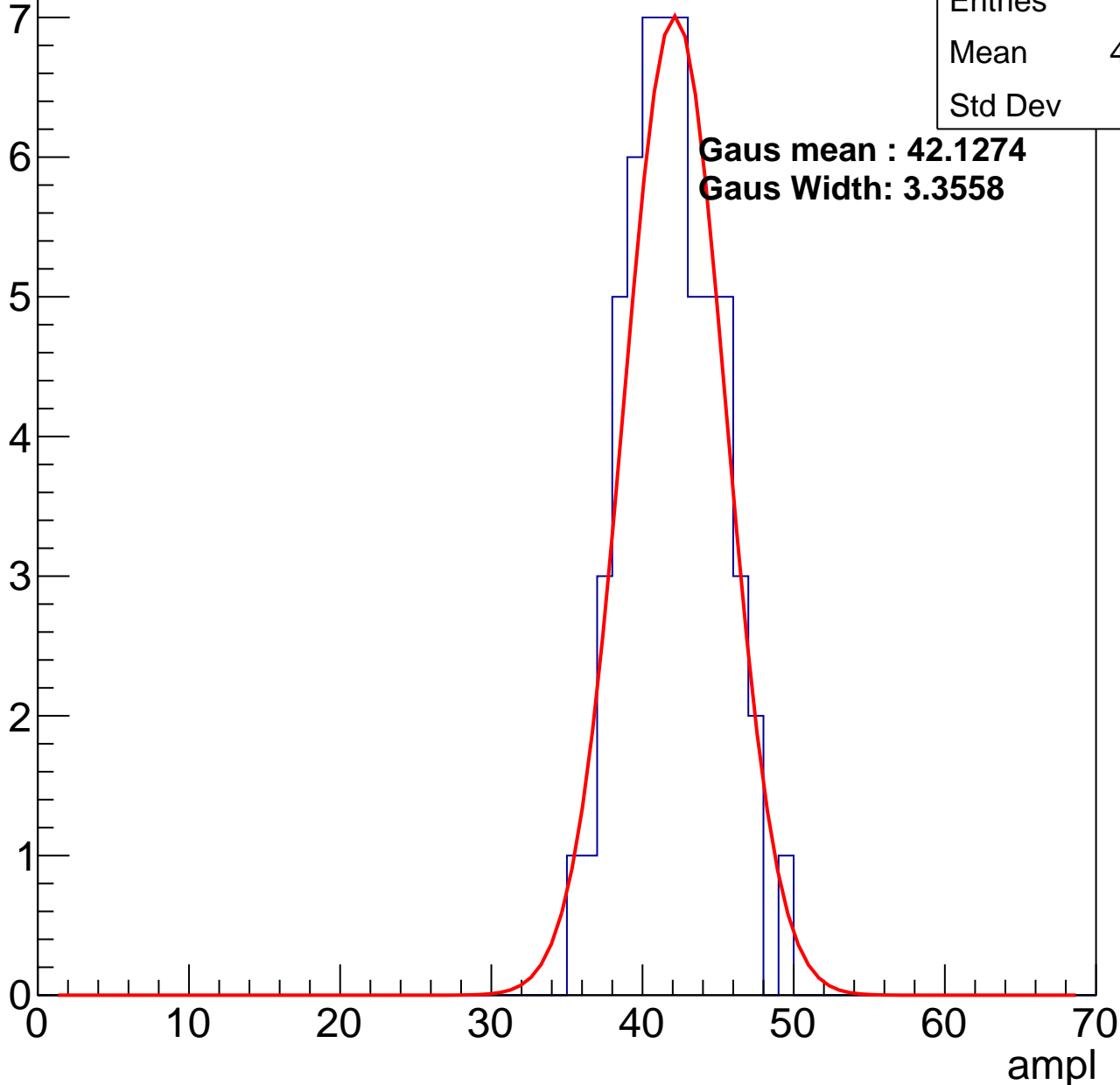
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	41.52
Std Dev	3.03

**Gaus mean : 42.1274**

**Gaus Width: 3.3558**

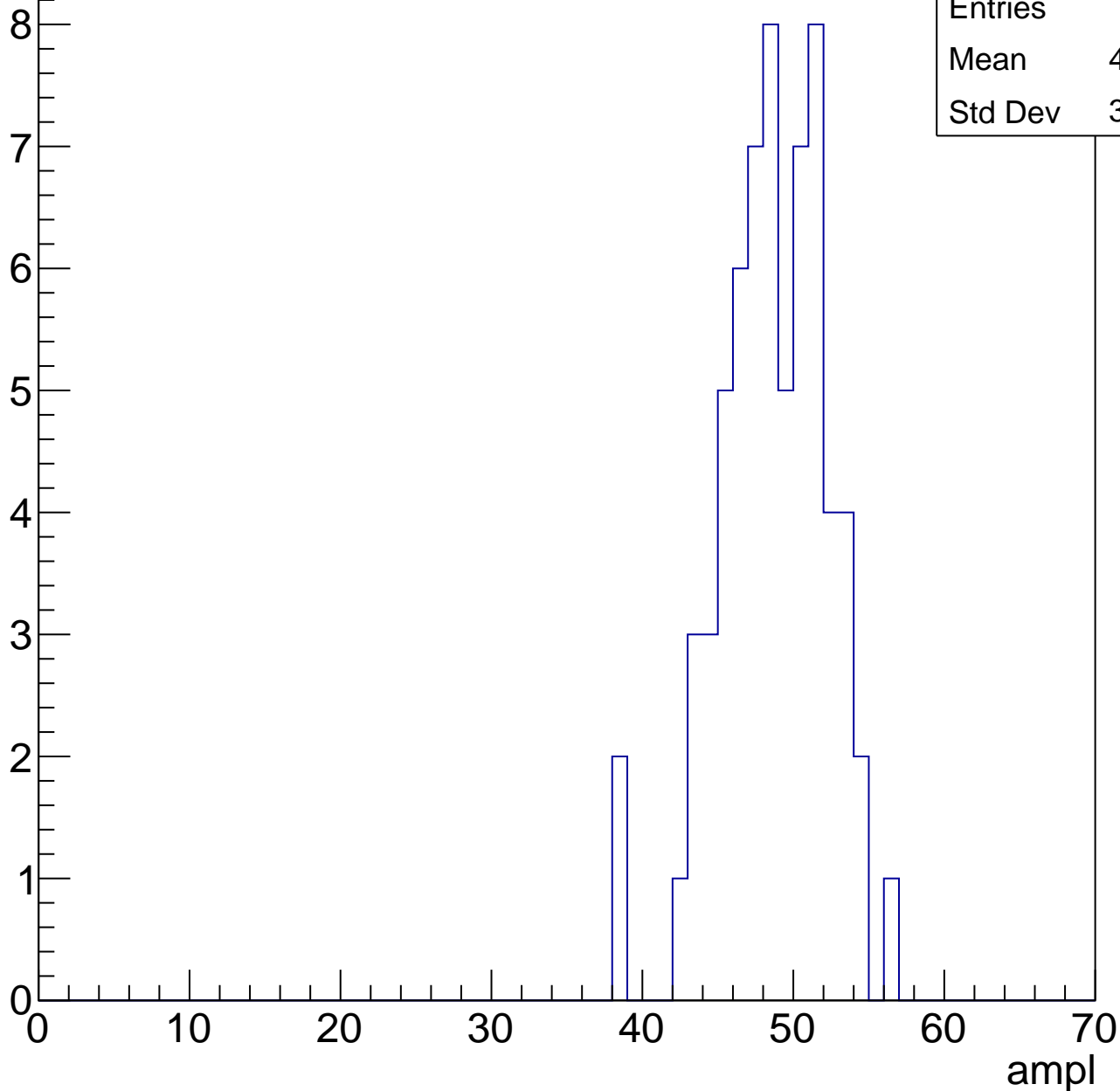


# B1L103S, U26-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	48.18
Std Dev	3.563

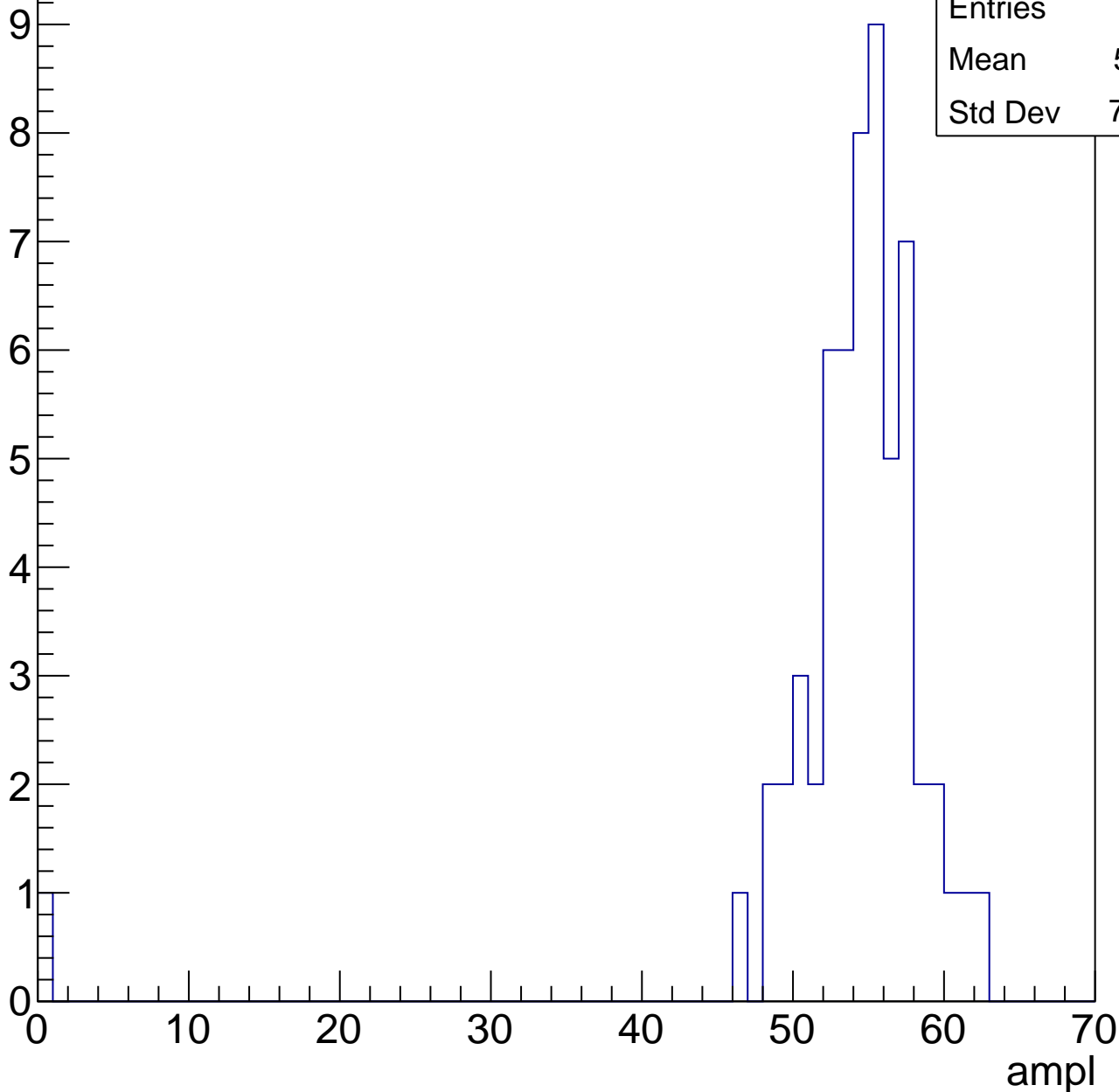


# B1L103S, U26-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	53.31
Std Dev	7.694

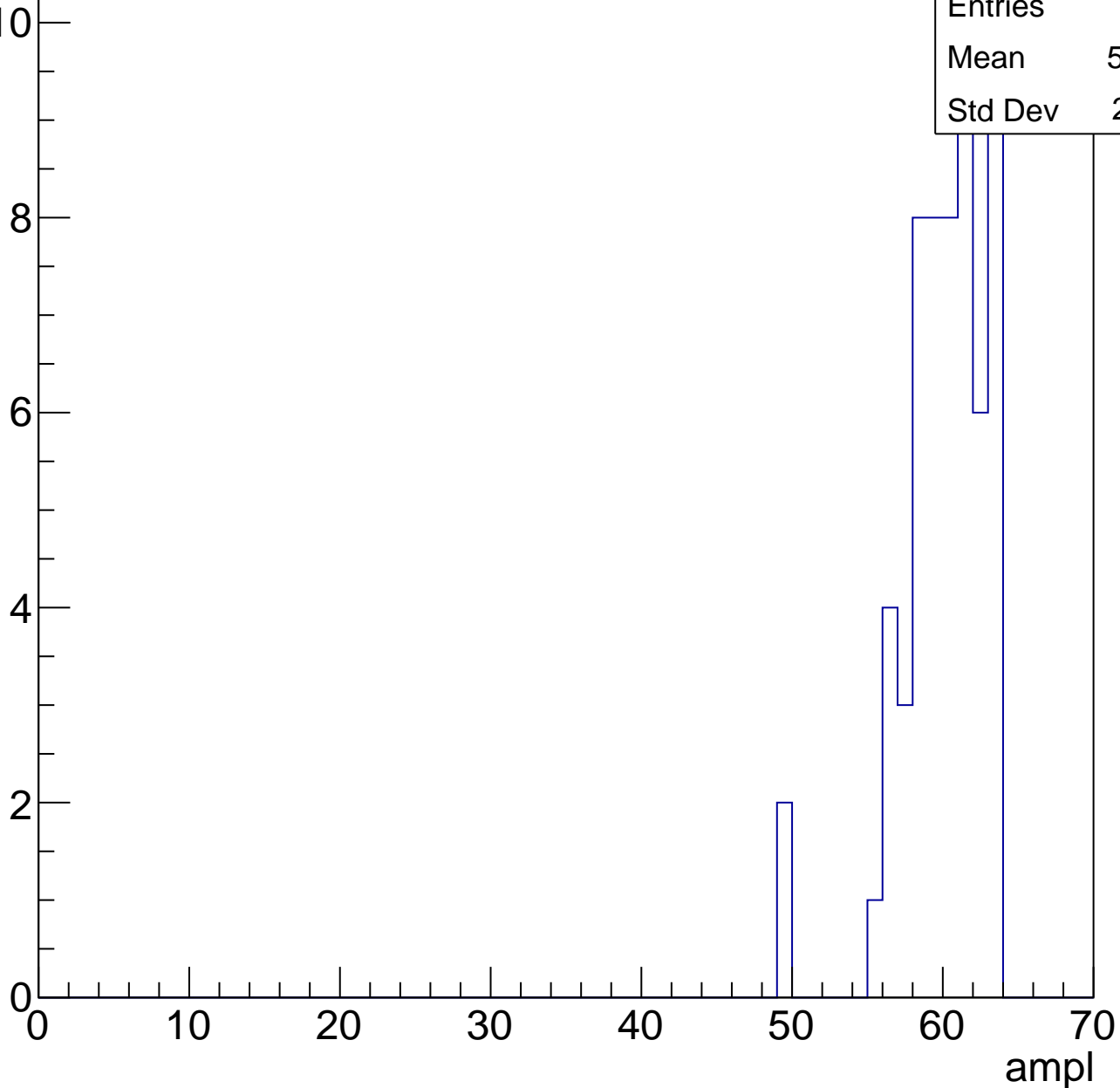


# B1L103S, U26-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

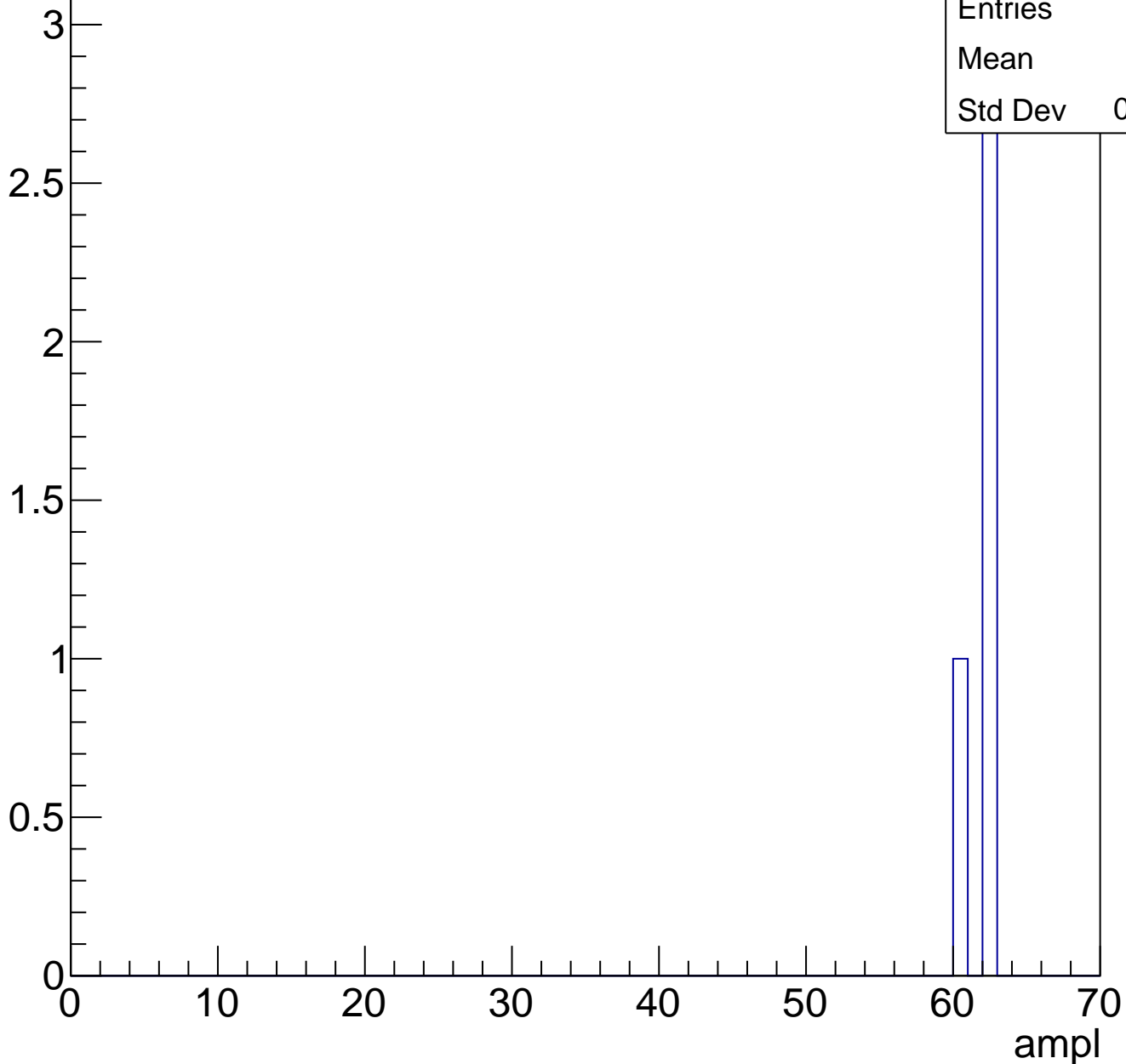
Entries	59
Mean	59.58
Std Dev	2.941



# B1L103S, U26-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U26-ch13, adc0

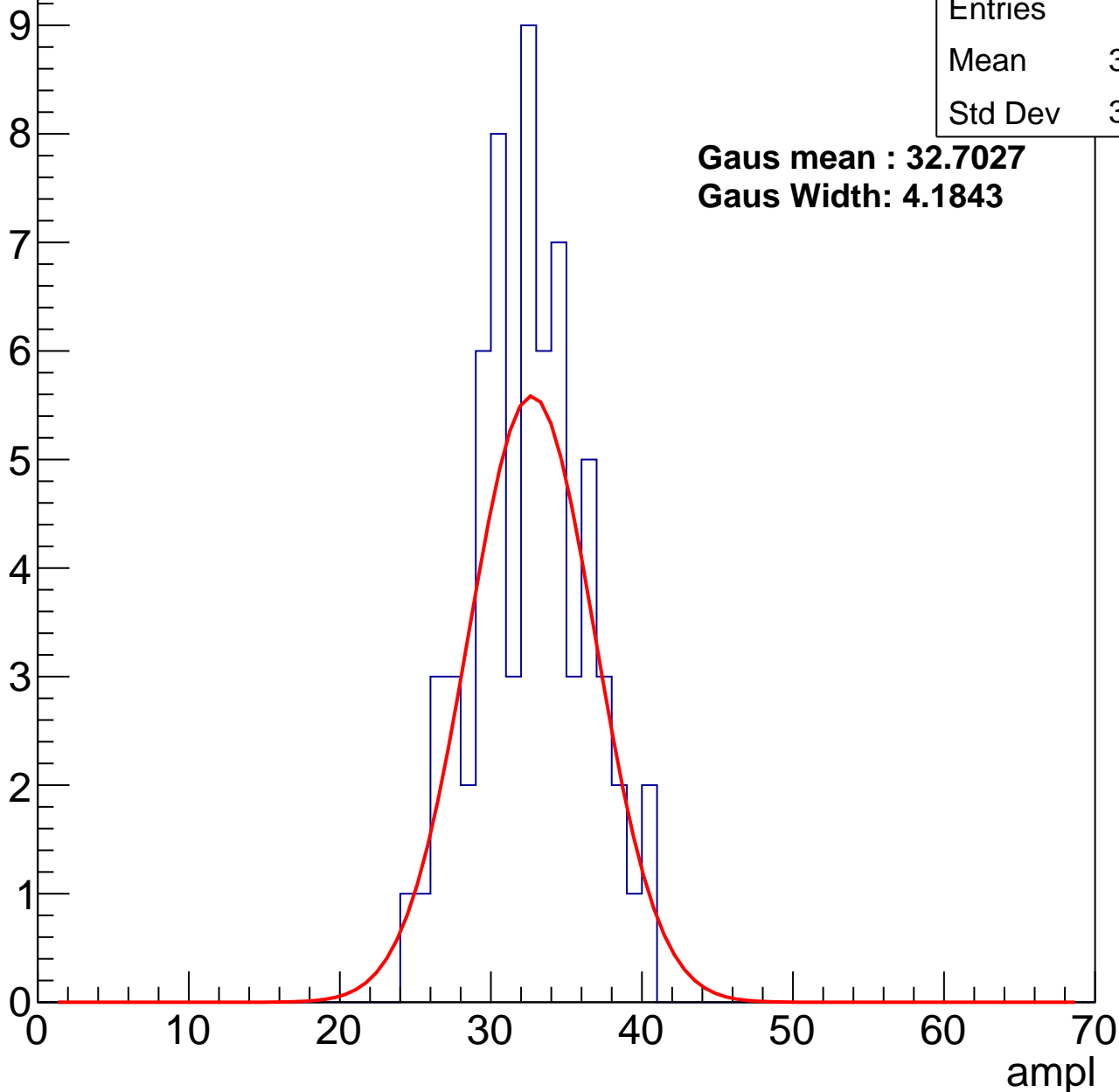
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	32.09
Std Dev	3.682

**Gaus mean : 32.7027**

**Gaus Width: 4.1843**



# B1L103S, U26-ch13, adc1

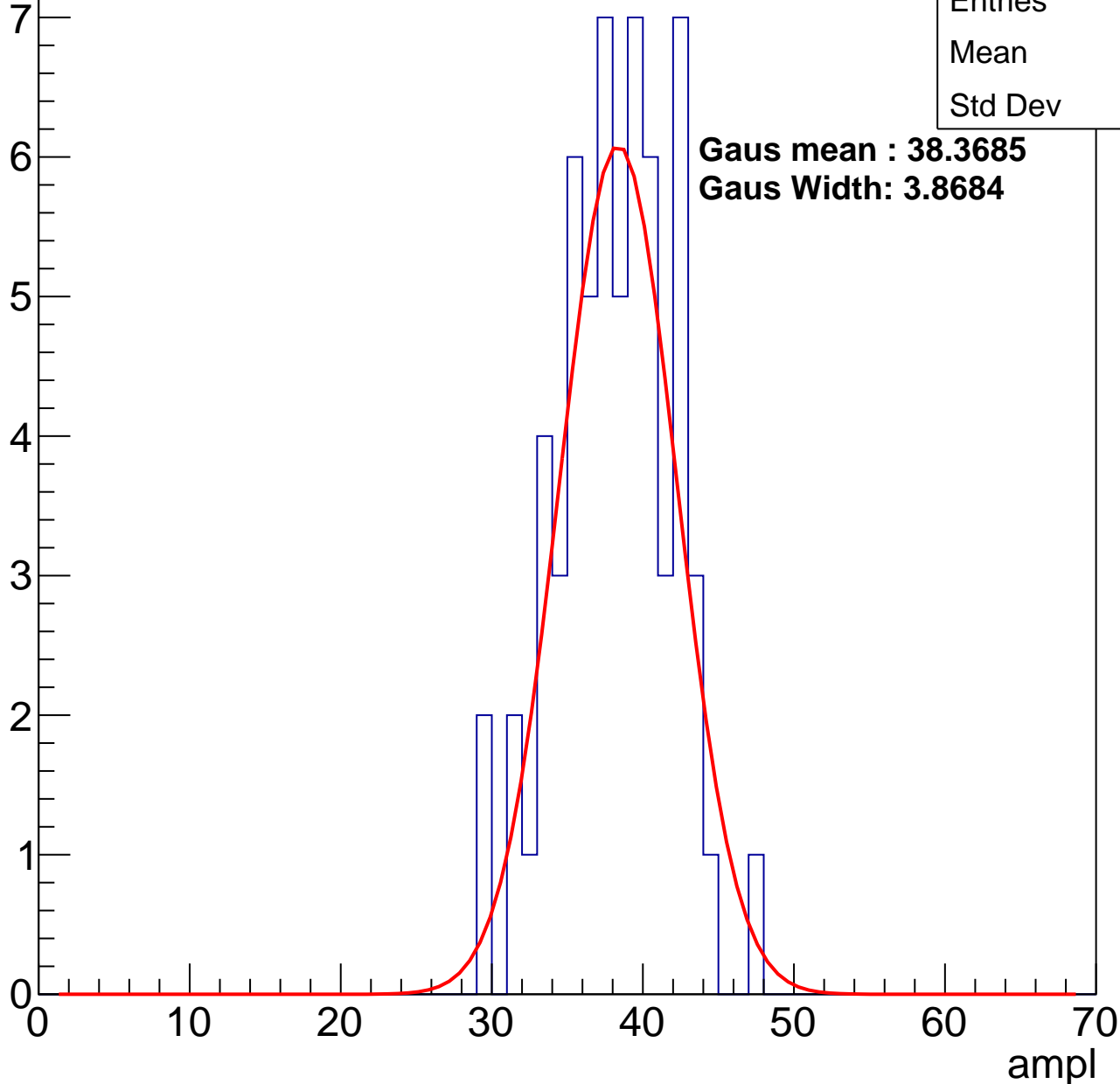
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	37.7
Std Dev	3.74

**Gaus mean : 38.3685**

**Gaus Width: 3.8684**



# B1L103S, U26-ch13, adc2

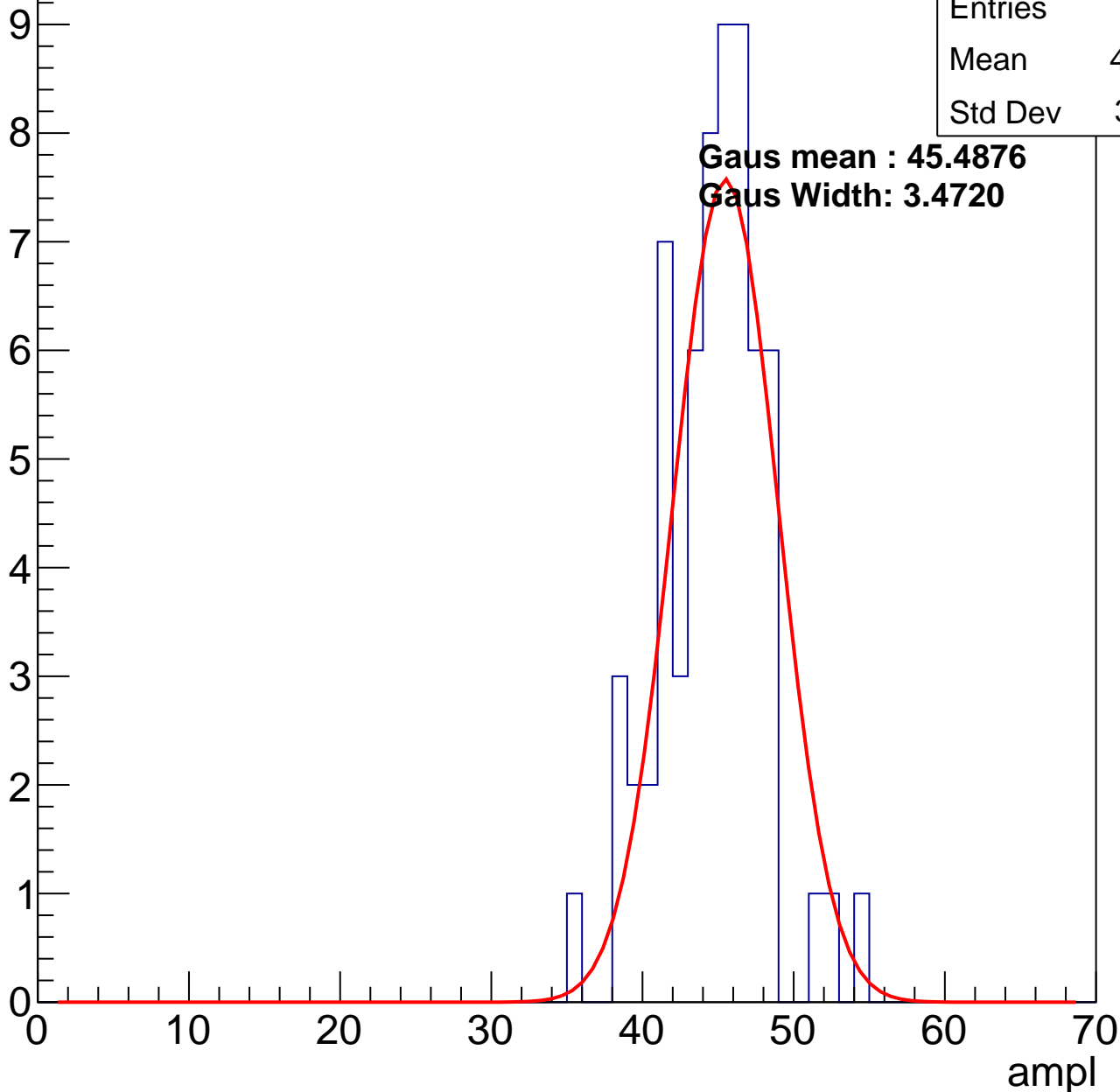
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	44.25
Std Dev	3.411

**Gaus mean : 45.4876**

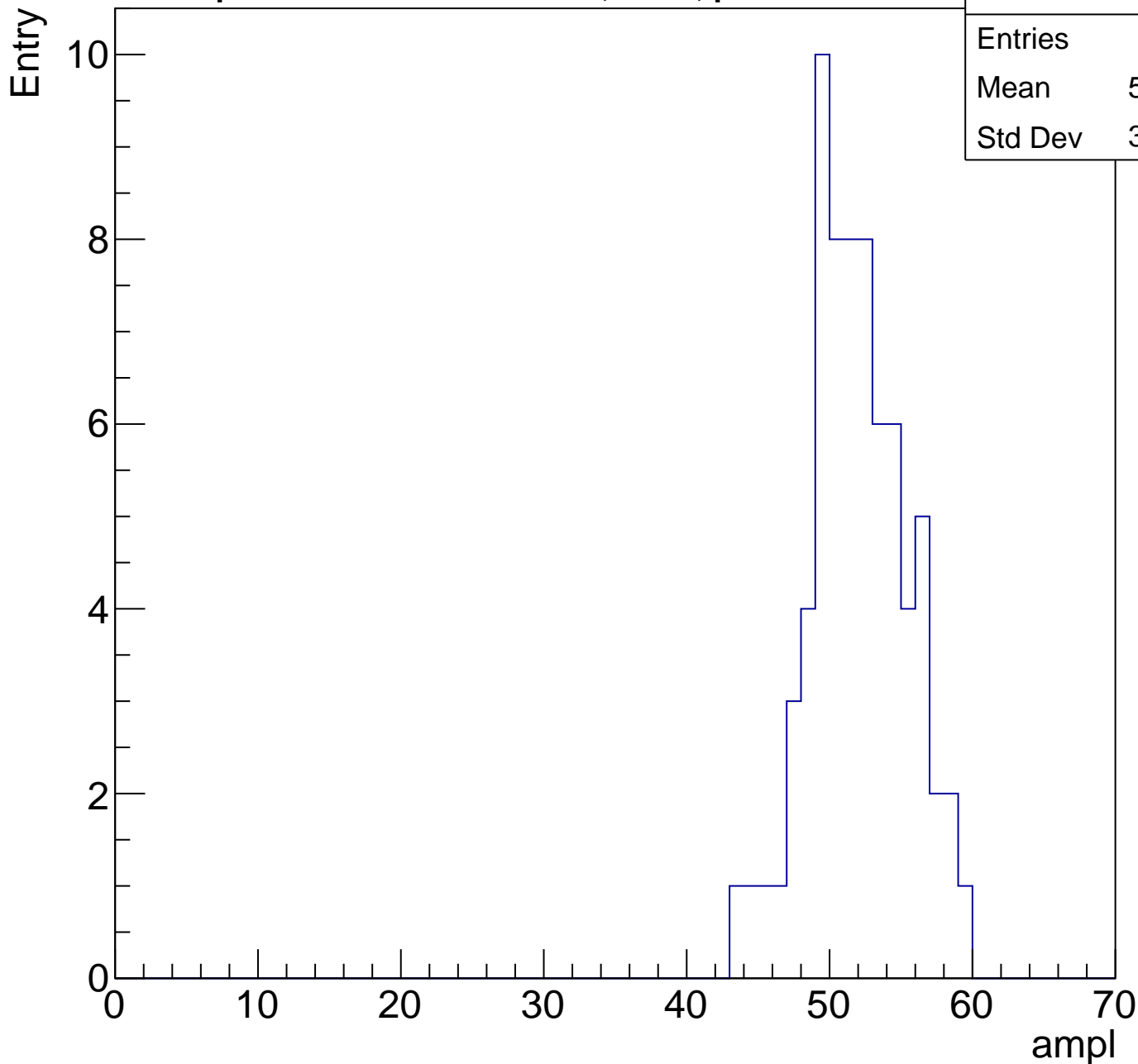
**Gaus Width: 3.4720**



# B1L103S, U26-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	71
Mean	51.49
Std Dev	3.352

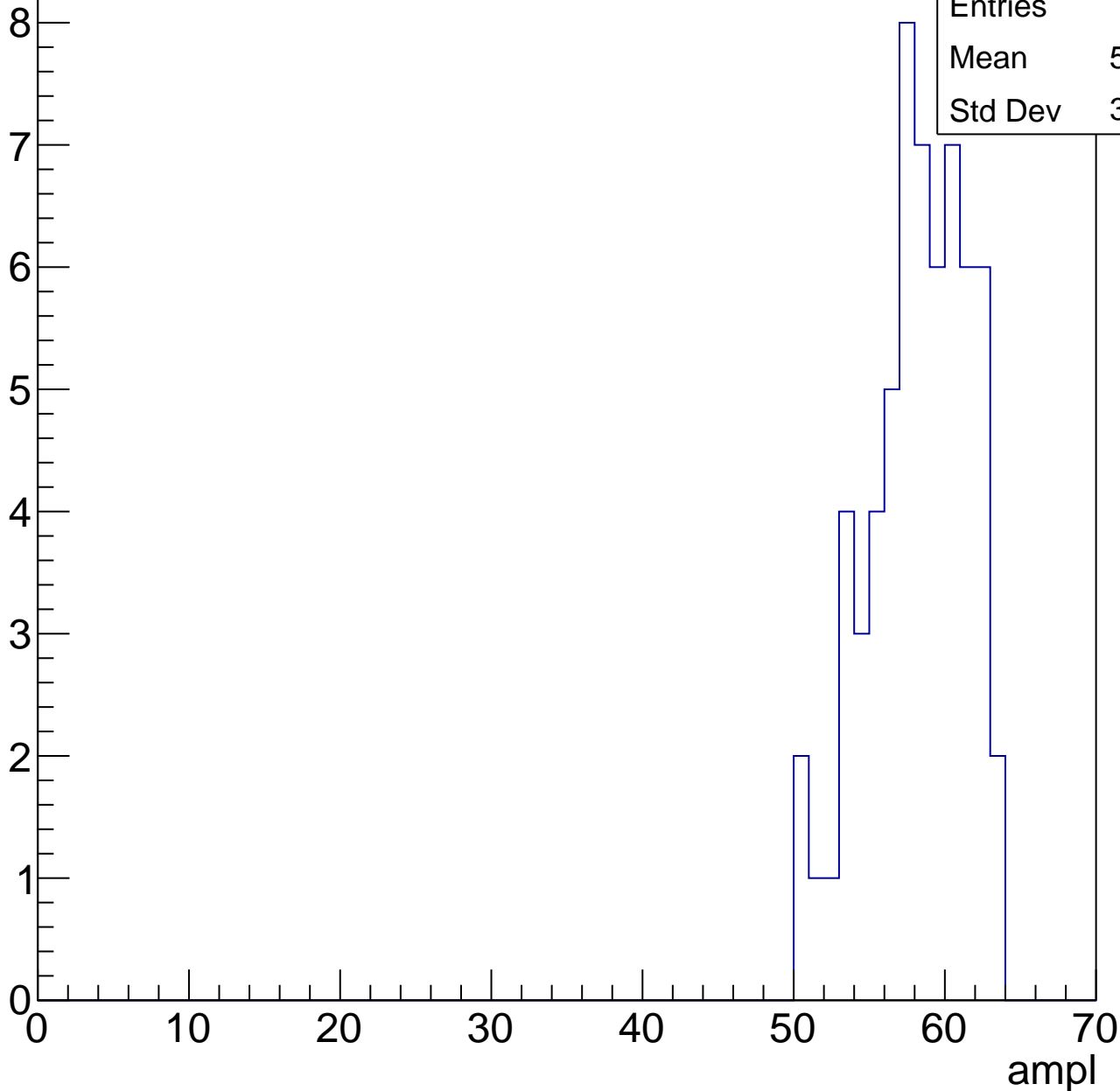


# B1L103S, U26-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	57.69
Std Dev	3.246

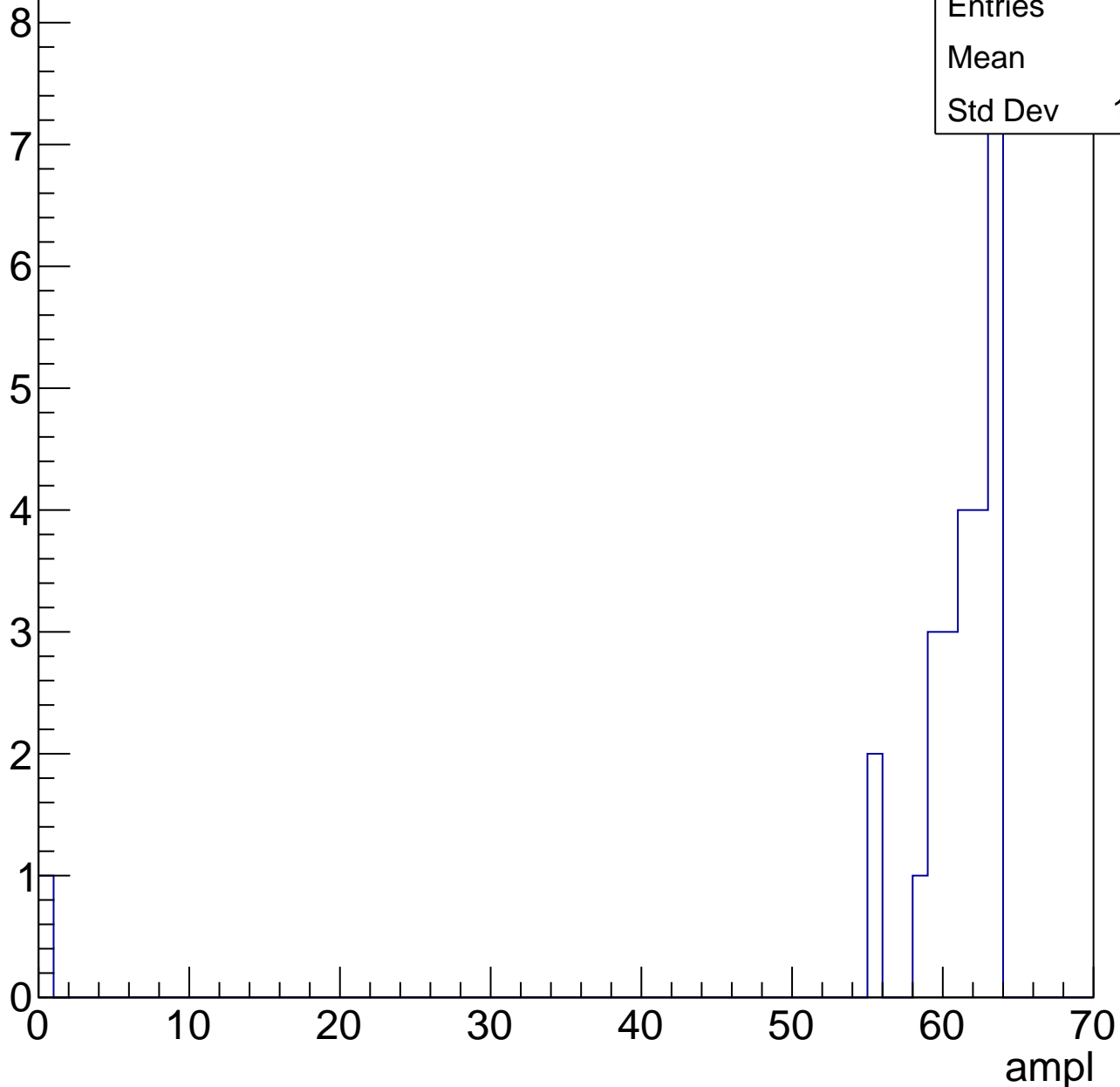


# B1L103S, U26-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	26
Mean	58.5
Std Dev	11.91



# B1L103S, U26-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L103S, U26-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch14, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	88
Mean	30.2
Std Dev	3.888

**Gaus mean : 30.3026**

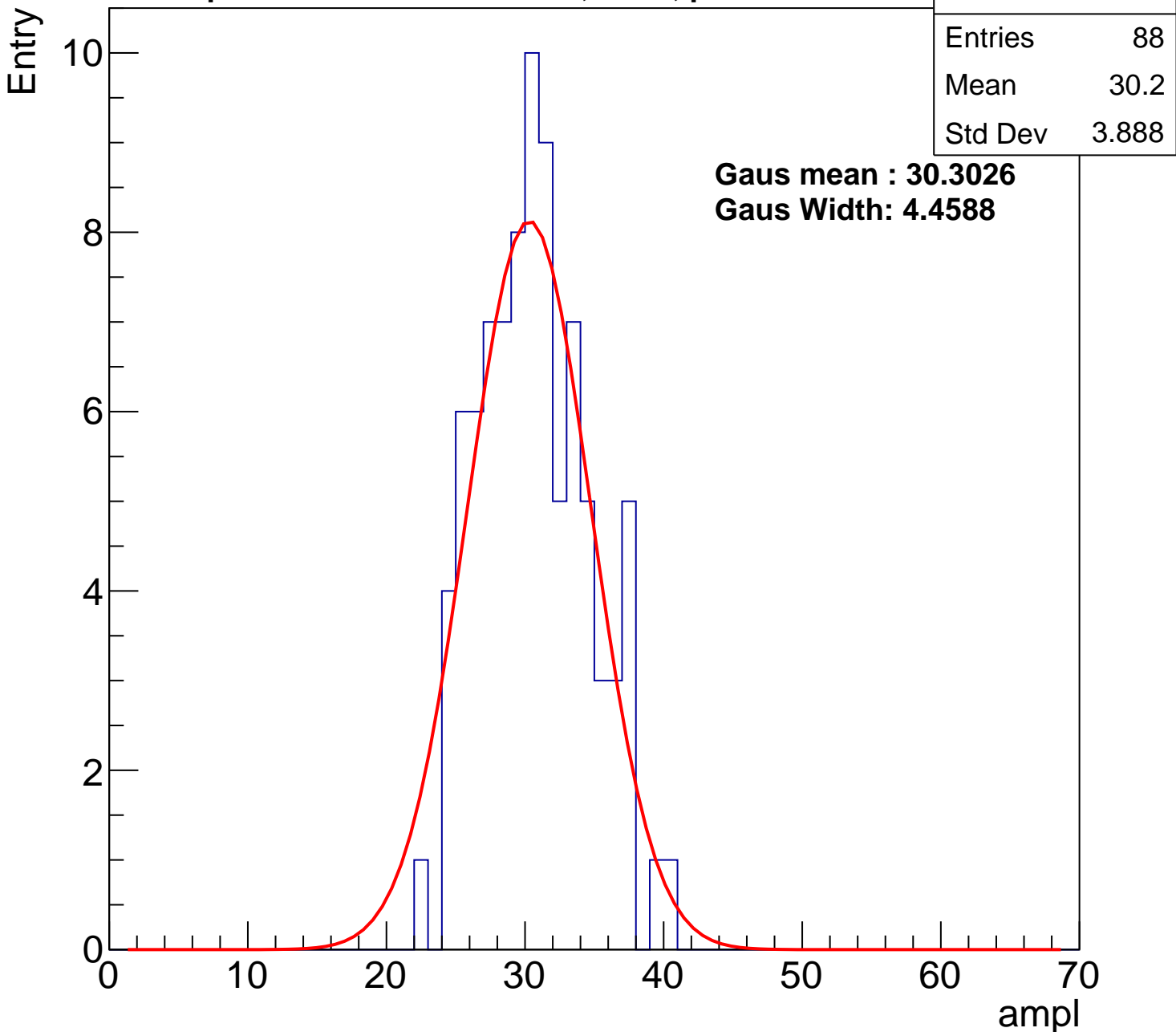
**Gaus Width: 4.4588**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



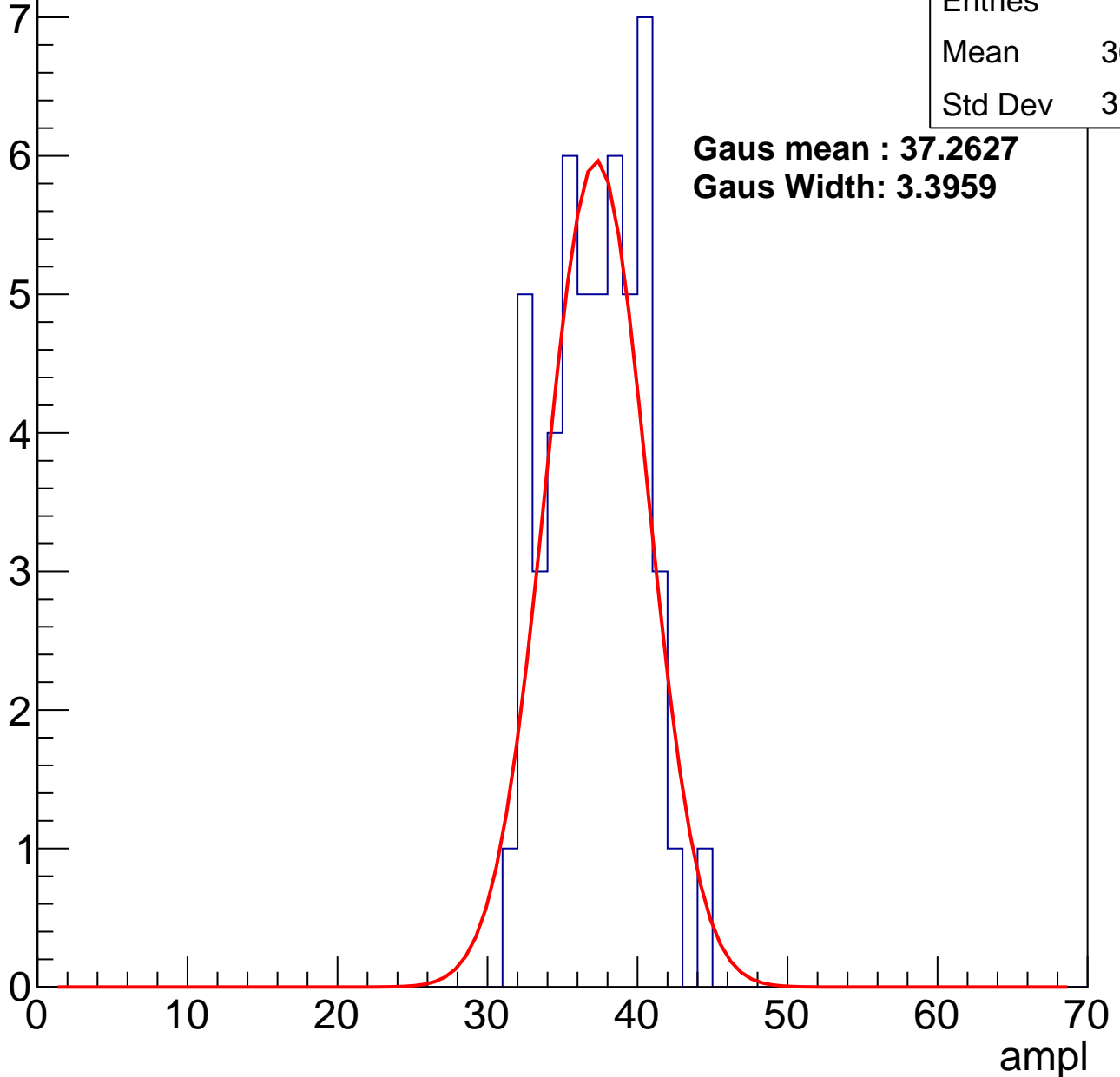
# B1L103S, U26-ch14, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	36.79
Std Dev	3.047

**Gaus mean : 37.2627**  
**Gaus Width: 3.3959**



# B1L103S, U26-ch14, adc2

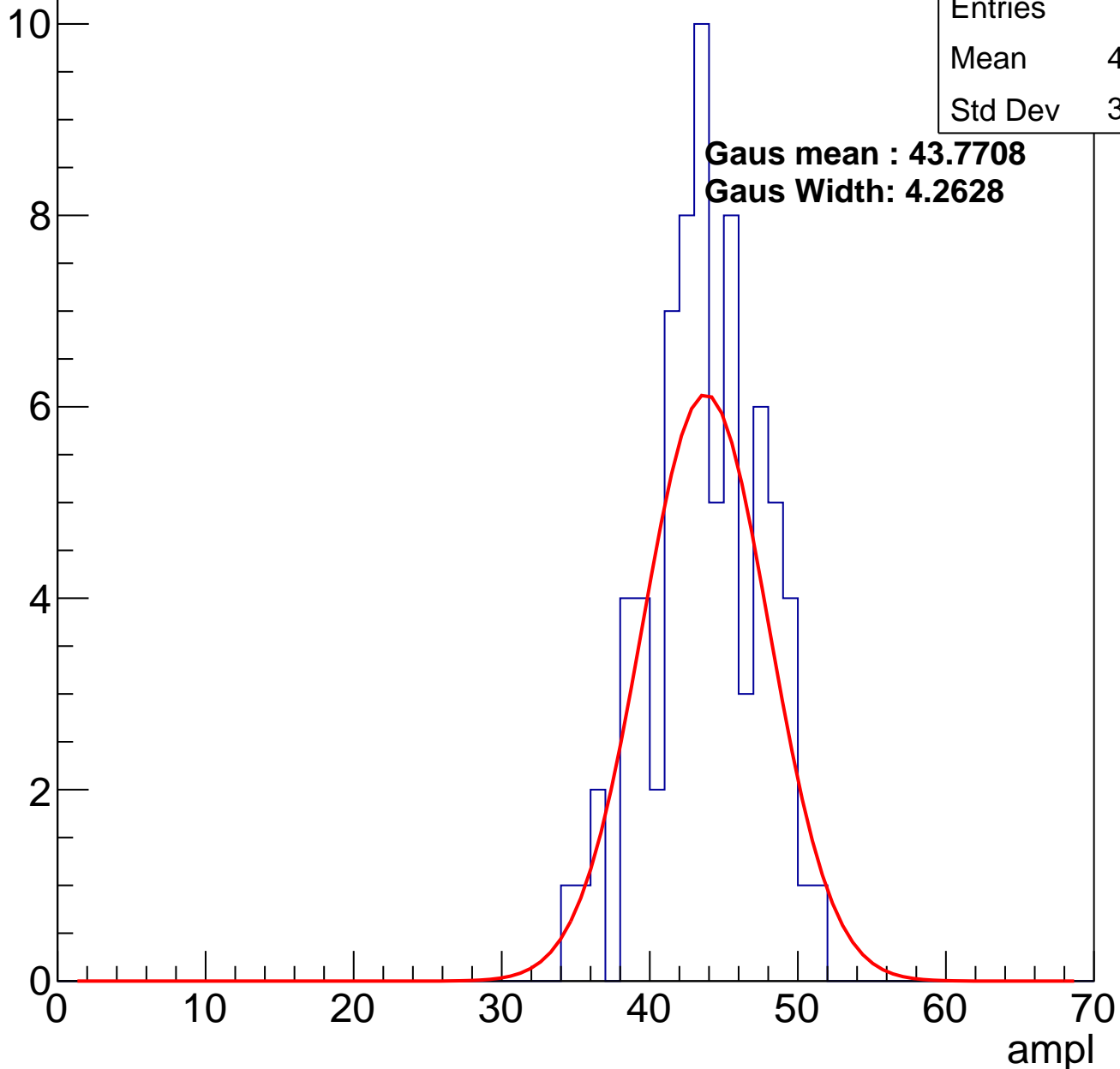
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	72
Mean	43.32
Std Dev	3.719

**Gaus mean : 43.7708**

**Gaus Width: 4.2628**

Entry

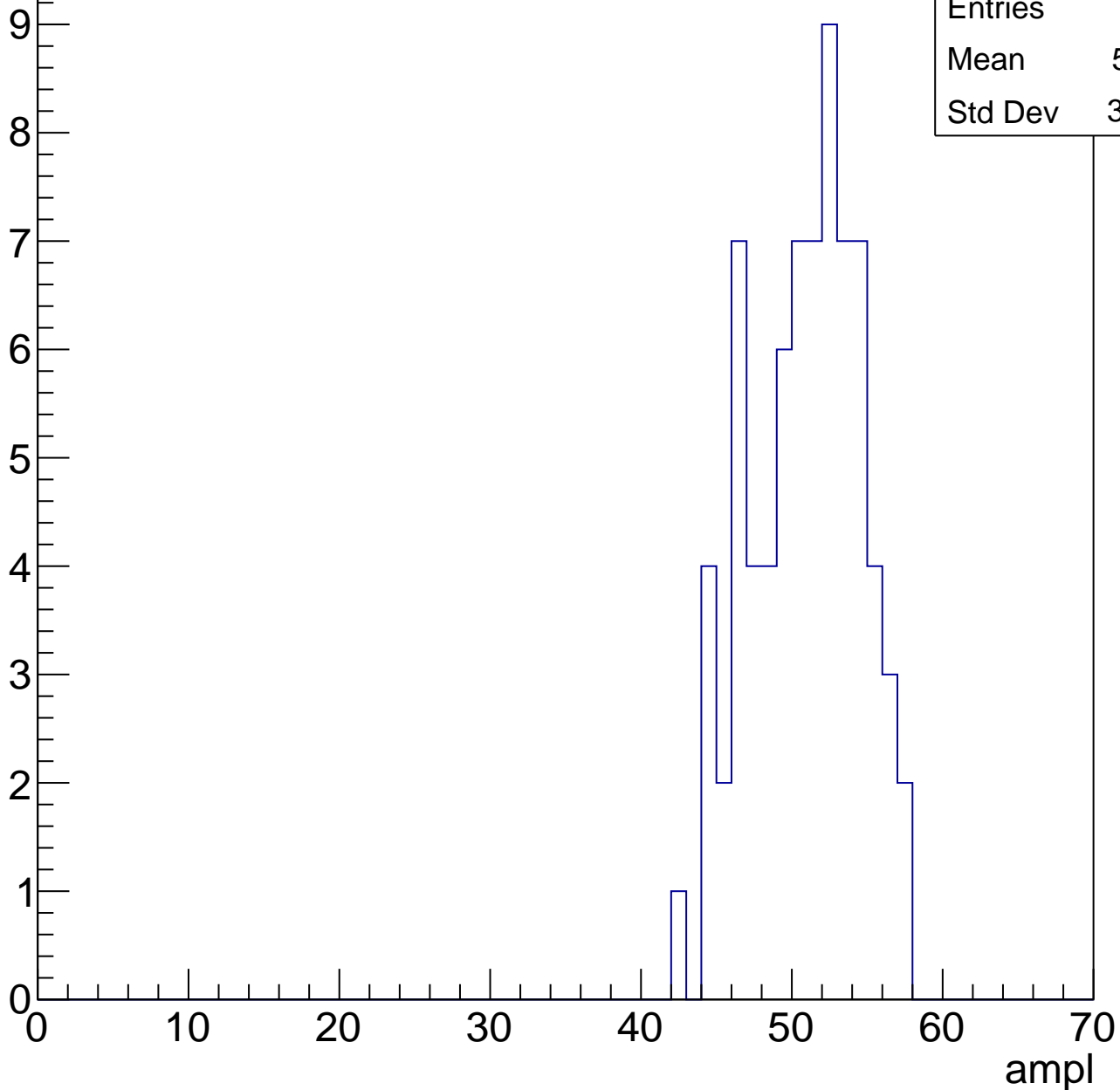


# B1L103S, U26-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	50.41
Std Dev	3.564

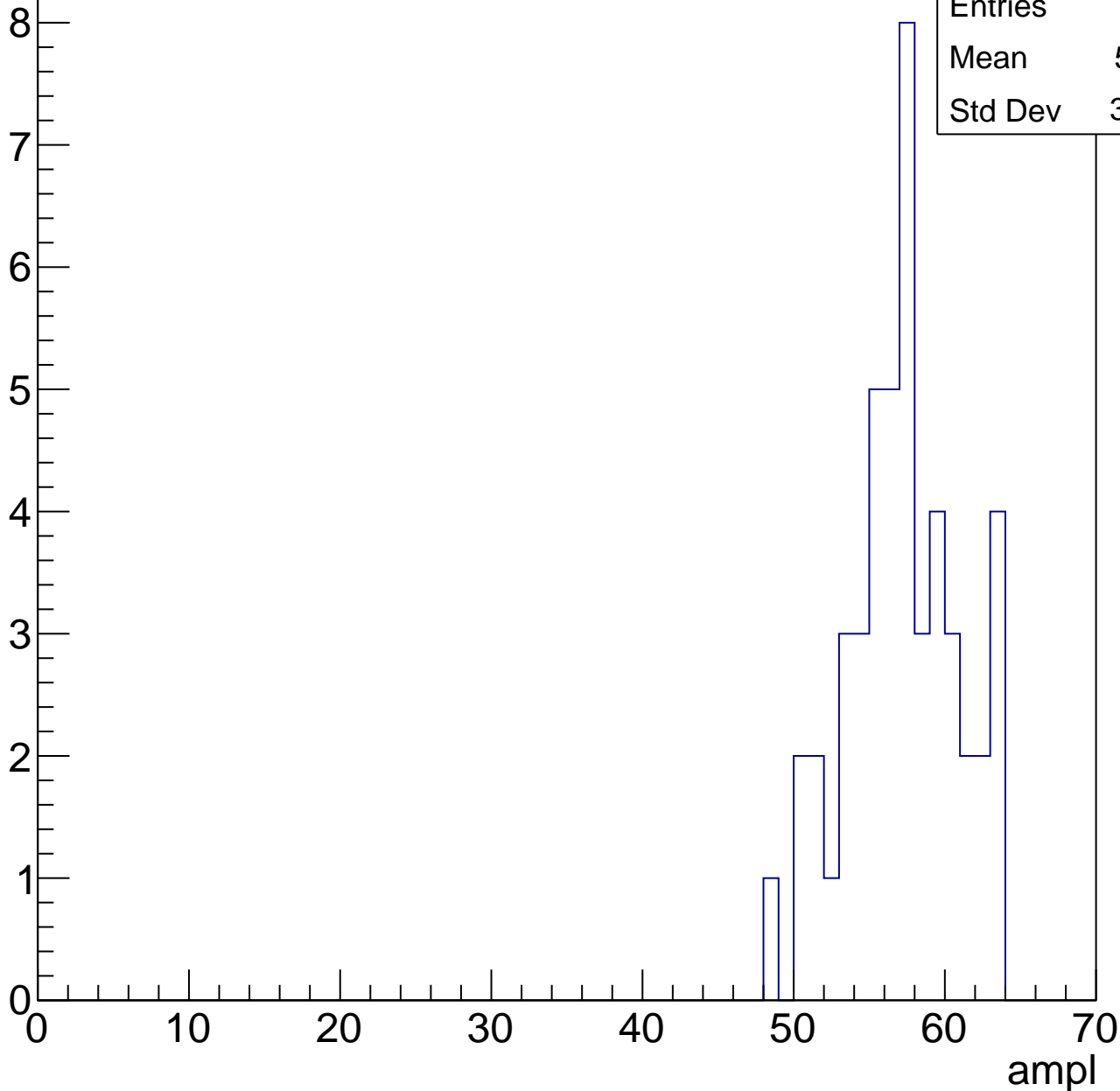


# B1L103S, U26-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	56.71
Std Dev	3.663

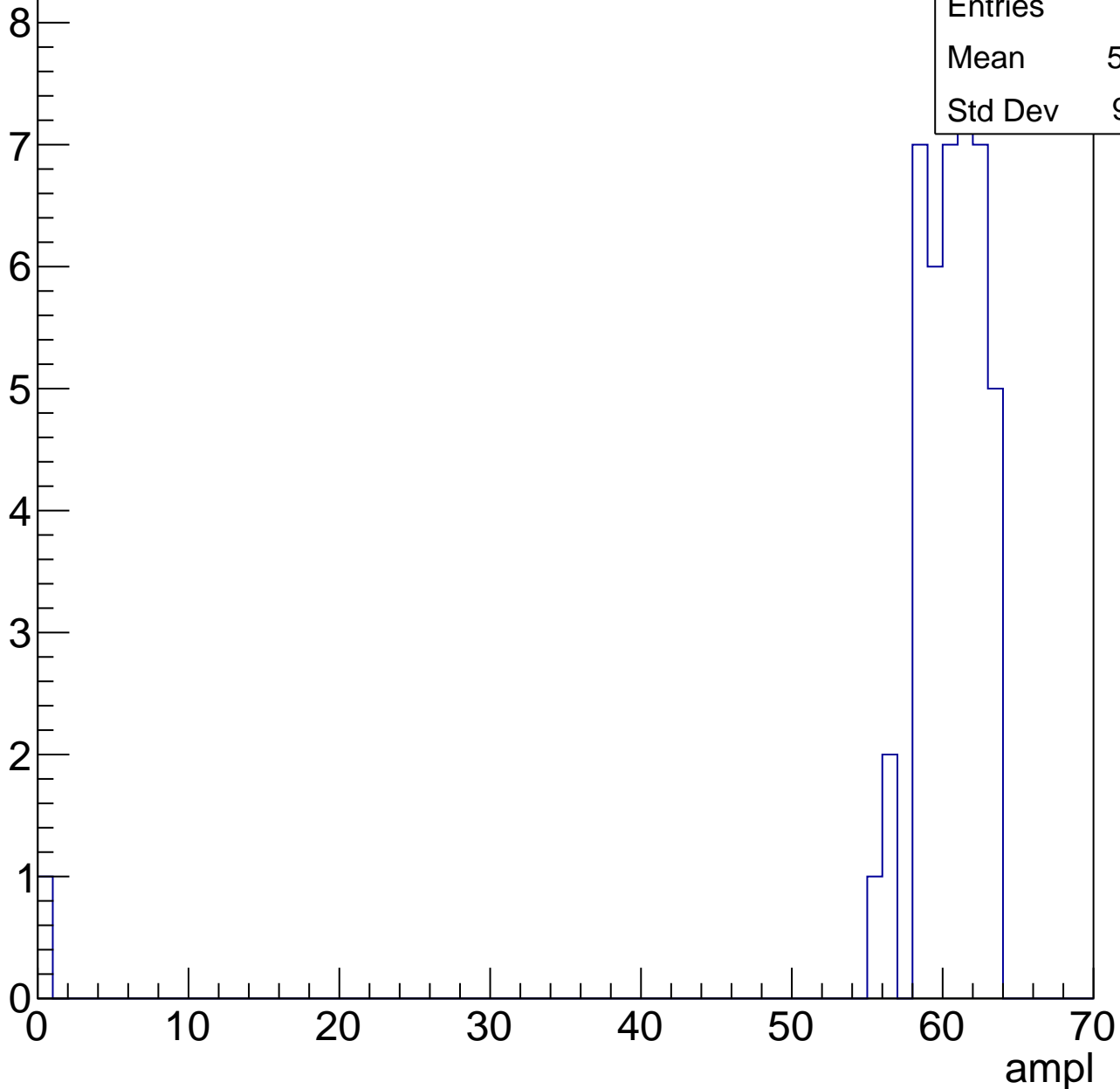


# B1L103S, U26-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	58.73
Std Dev	9.171



# B1L103S, U26-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U26-ch15, adc0

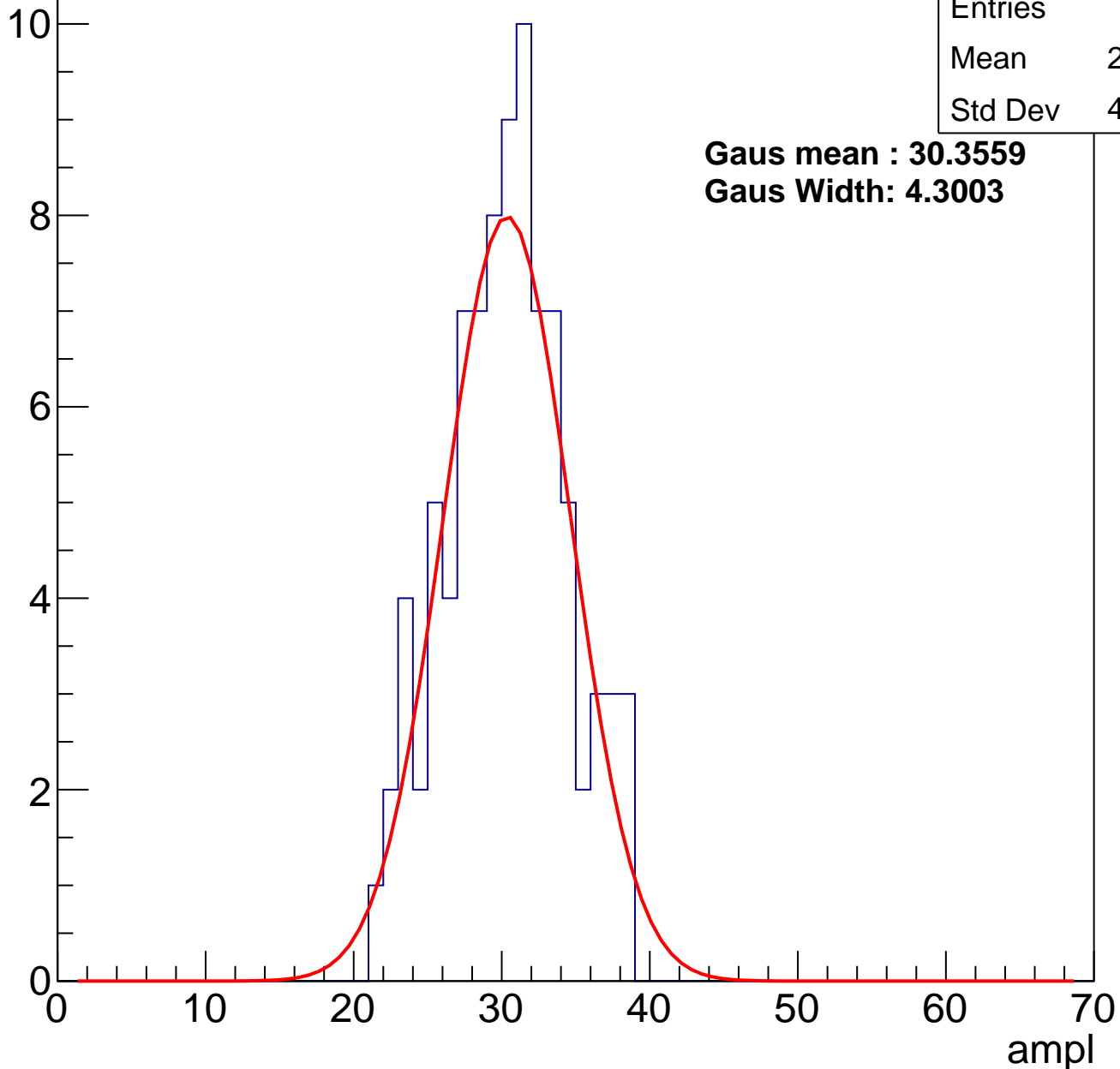
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	89
Mean	29.88
Std Dev	4.025

**Gaus mean : 30.3559**

**Gaus Width: 4.3003**

Entry



# B1L103S, U26-ch15, adc1

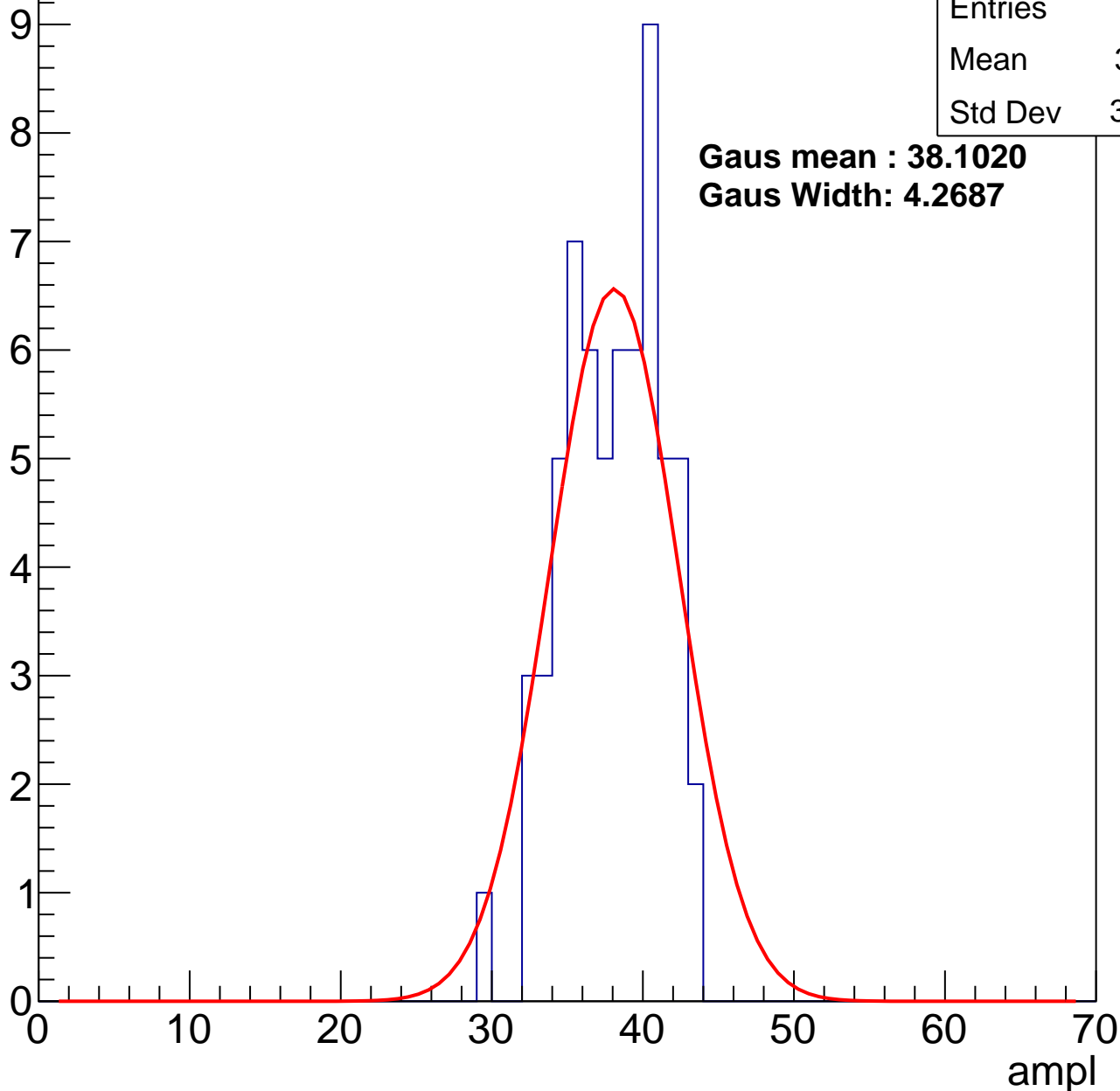
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	37.51
Std Dev	3.182

**Gaus mean : 38.1020**

**Gaus Width: 4.2687**



# B1L103S, U26-ch15, adc2

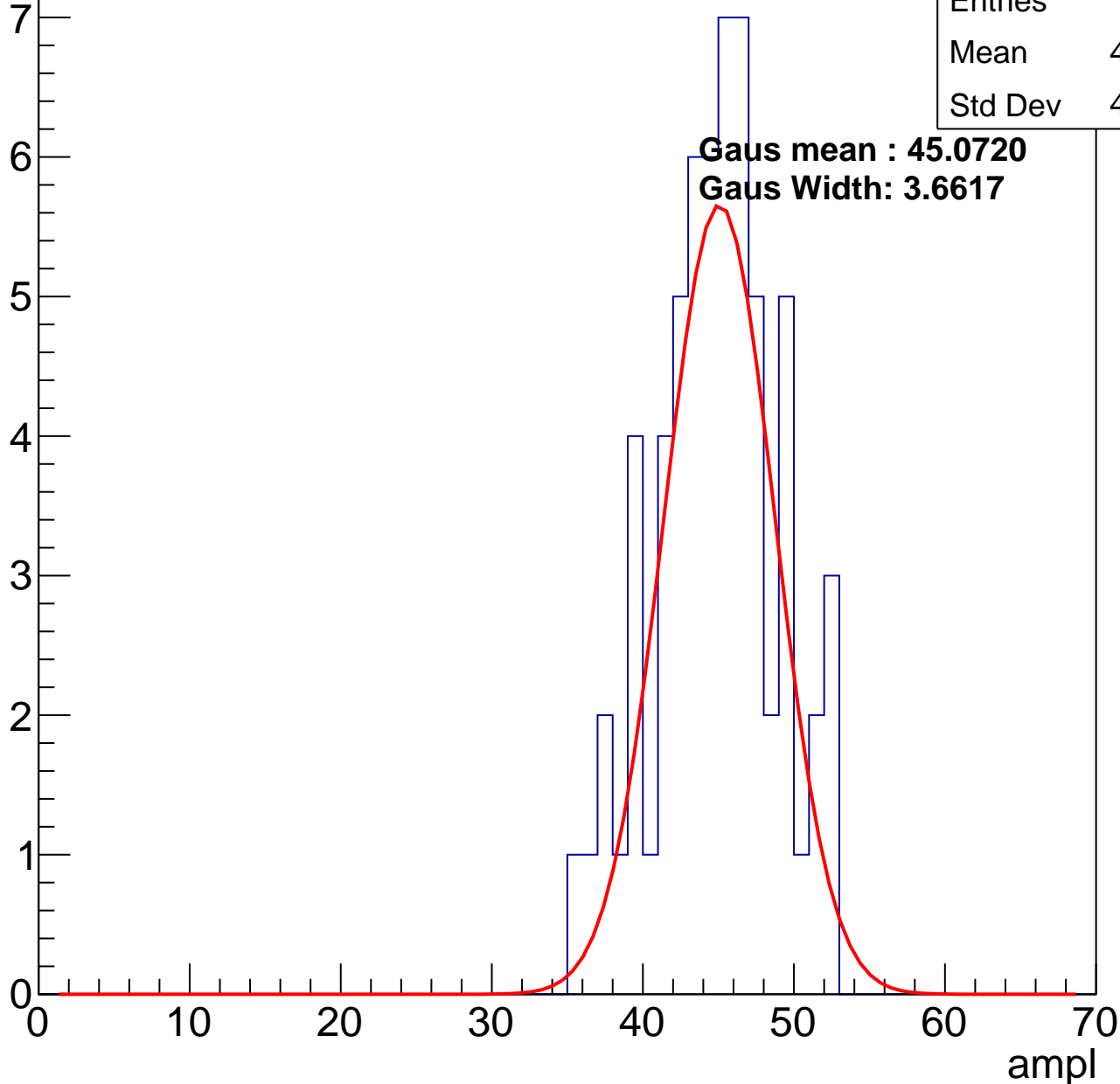
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	44.38
Std Dev	4.006

**Gaus mean : 45.0720**

**Gaus Width: 3.6617**

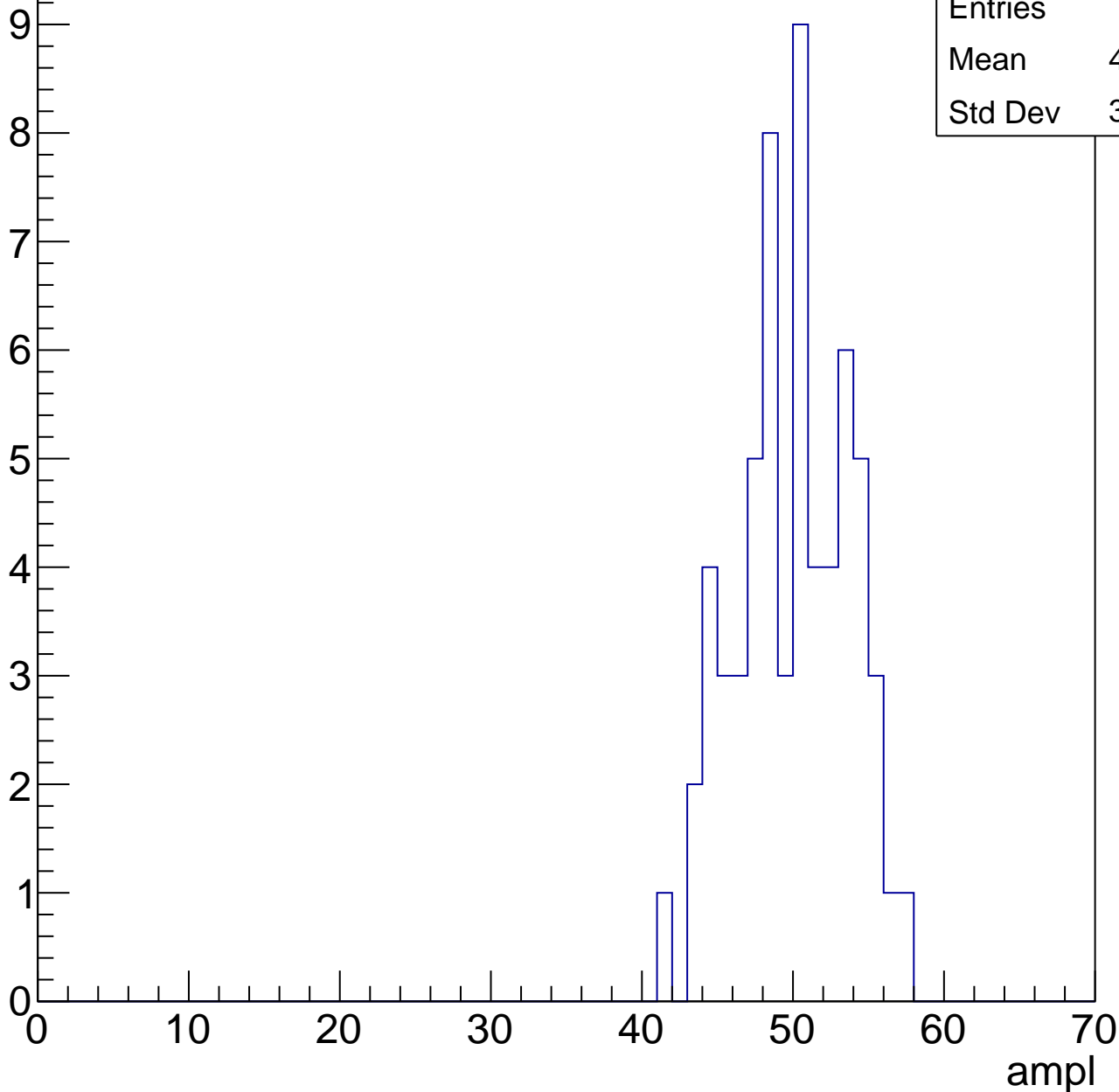


# B1L103S, U26-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

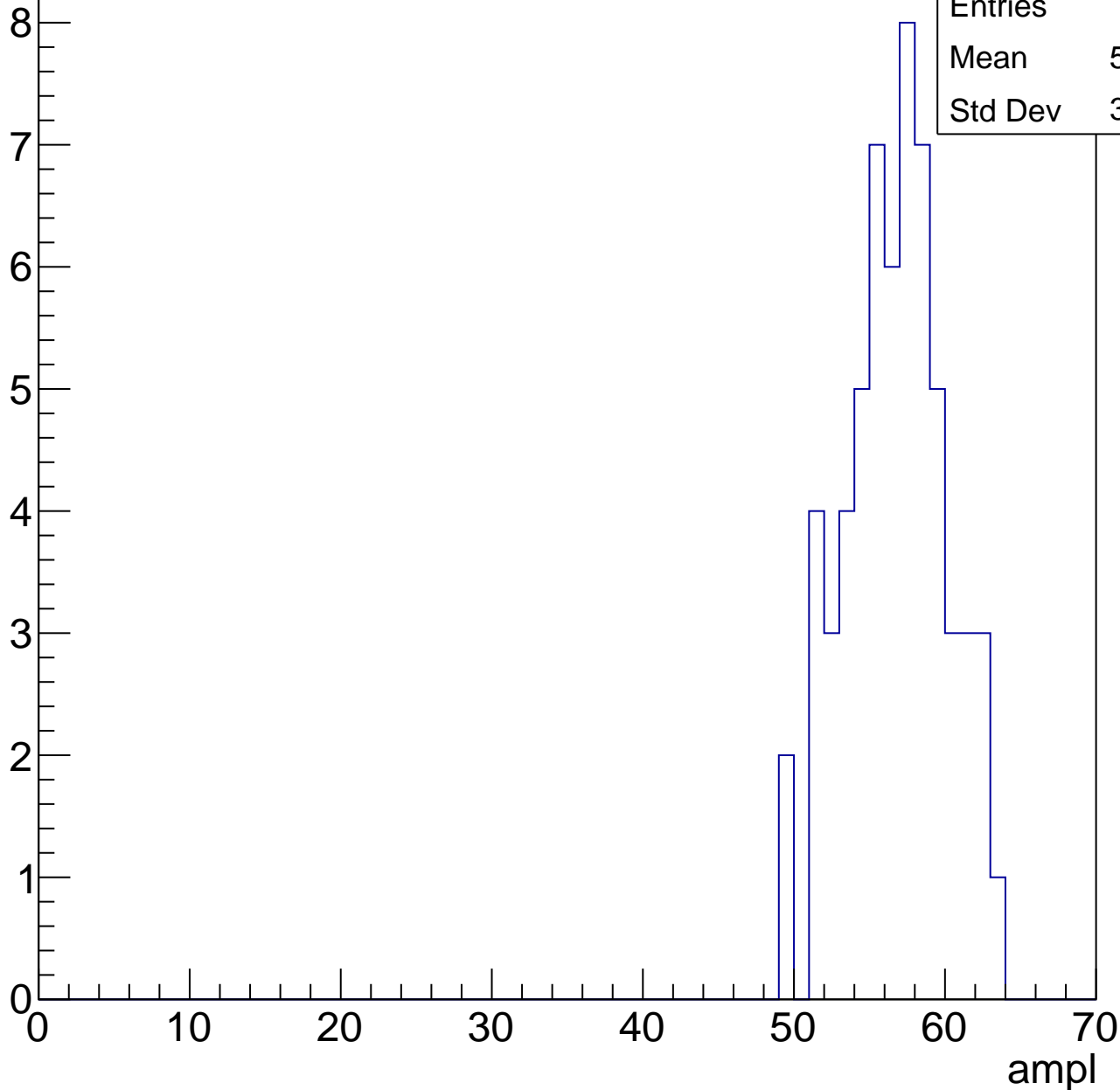
Entries	62
Mean	49.52
Std Dev	3.649



# B1L103S, U26-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

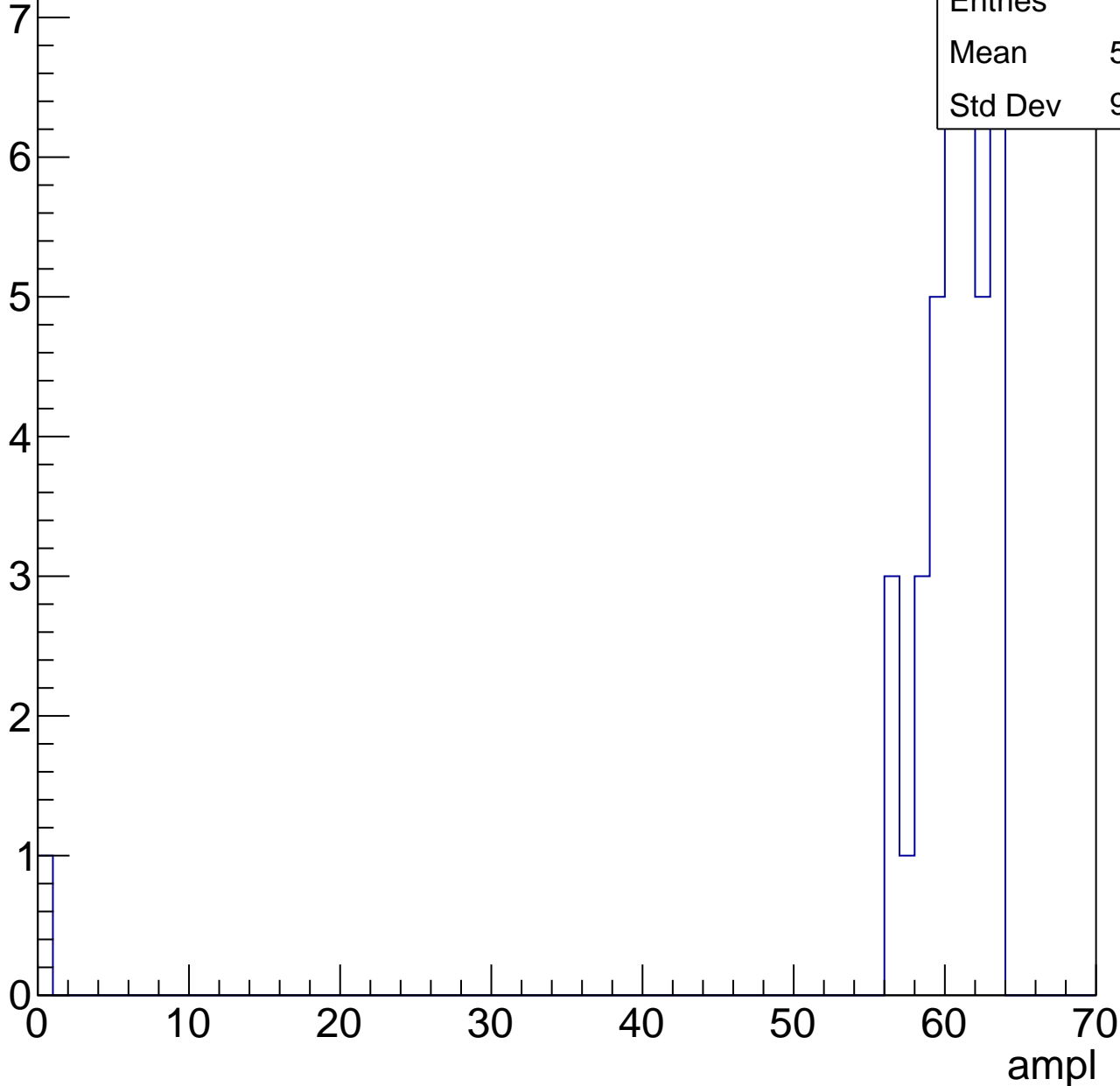


# B1L103S, U26-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	39
Mean	58.77
Std Dev	9.747



# B1L103S, U26-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U26-ch16, adc0

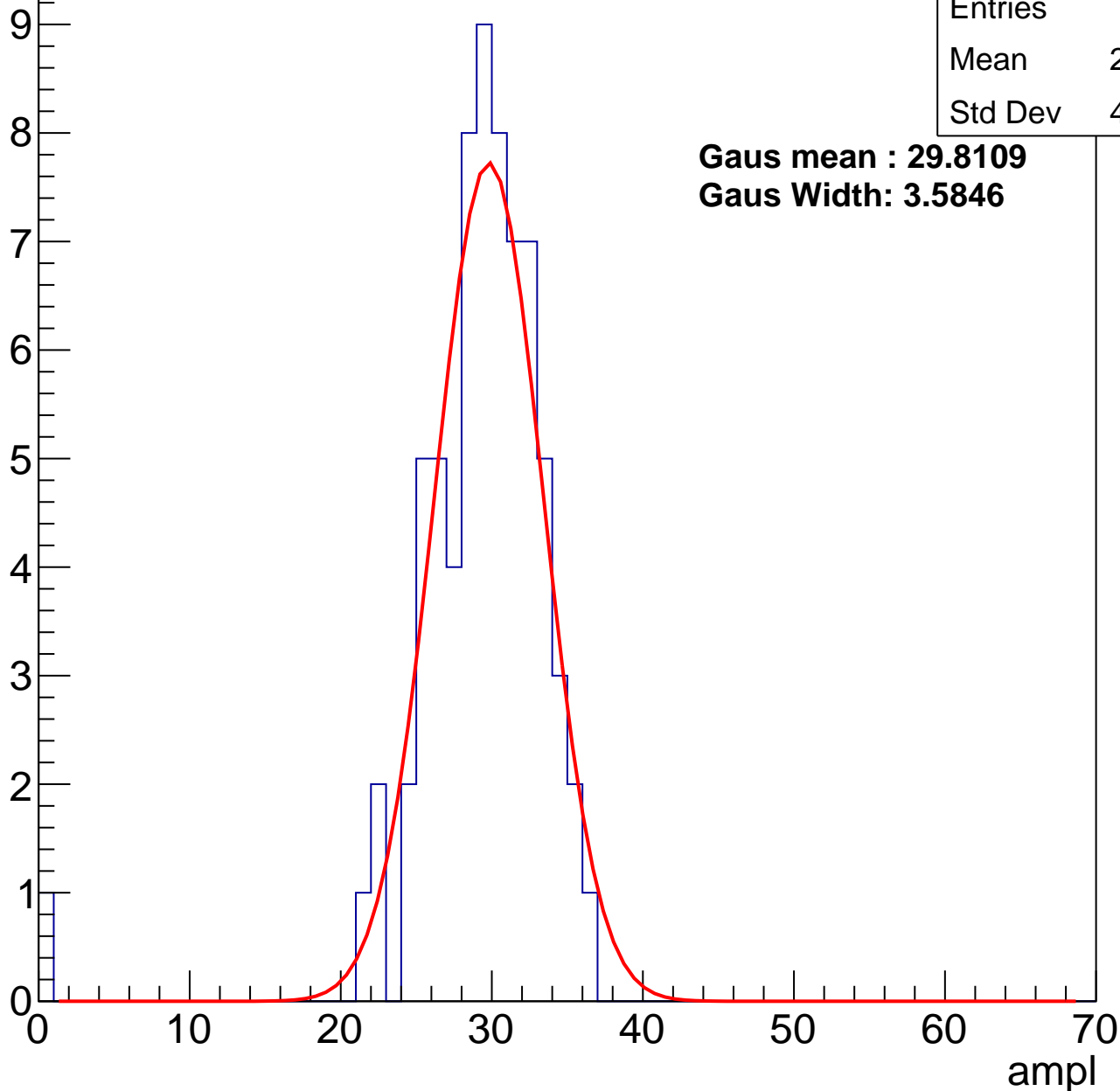
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	28.79
Std Dev	4.742

**Gaus mean : 29.8109**

**Gaus Width: 3.5846**



# B1L103S, U26-ch16, adc1

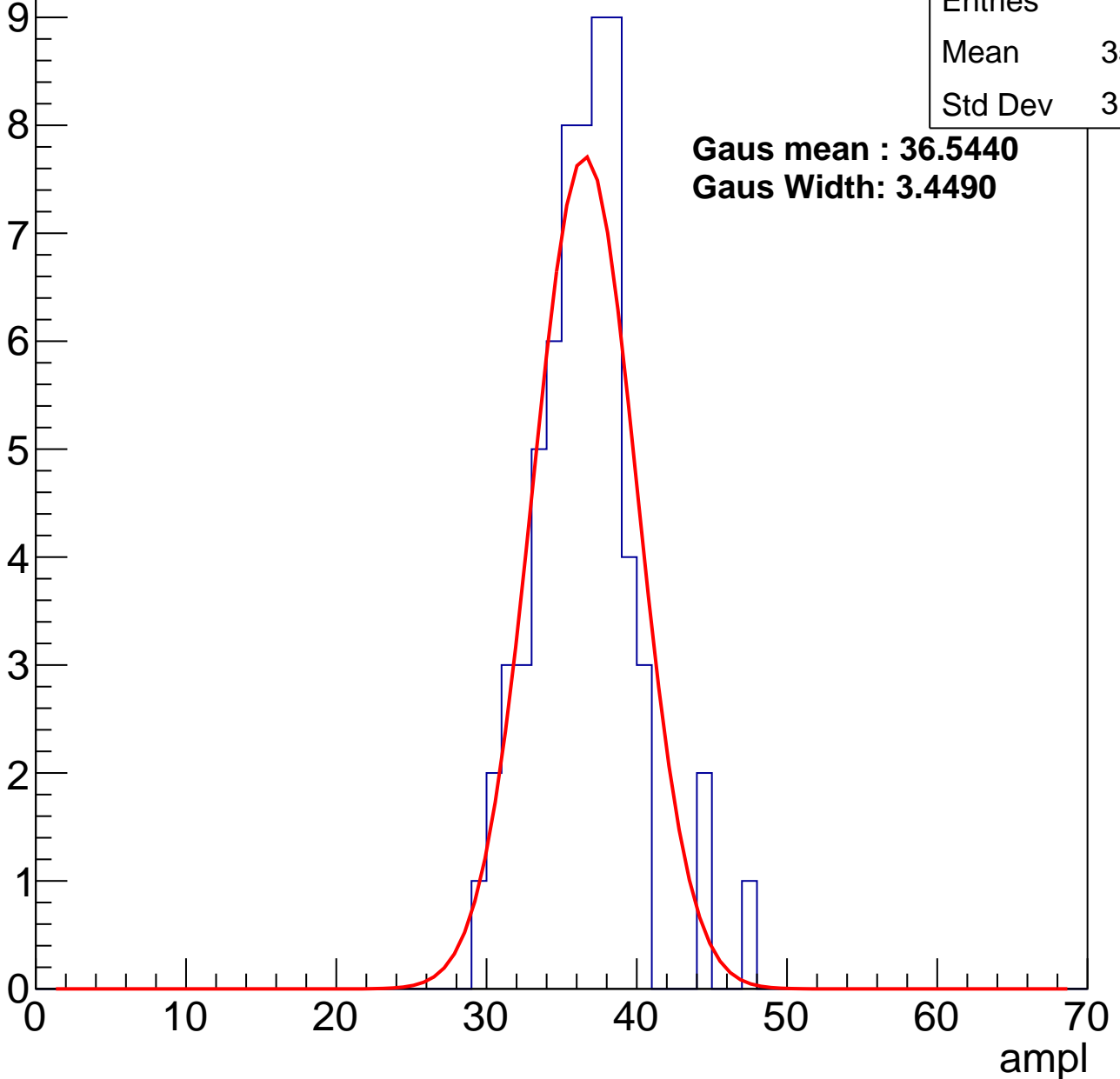
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	35.95
Std Dev	3.304

**Gaus mean : 36.5440**

**Gaus Width: 3.4490**



# B1L103S, U26-ch16, adc2

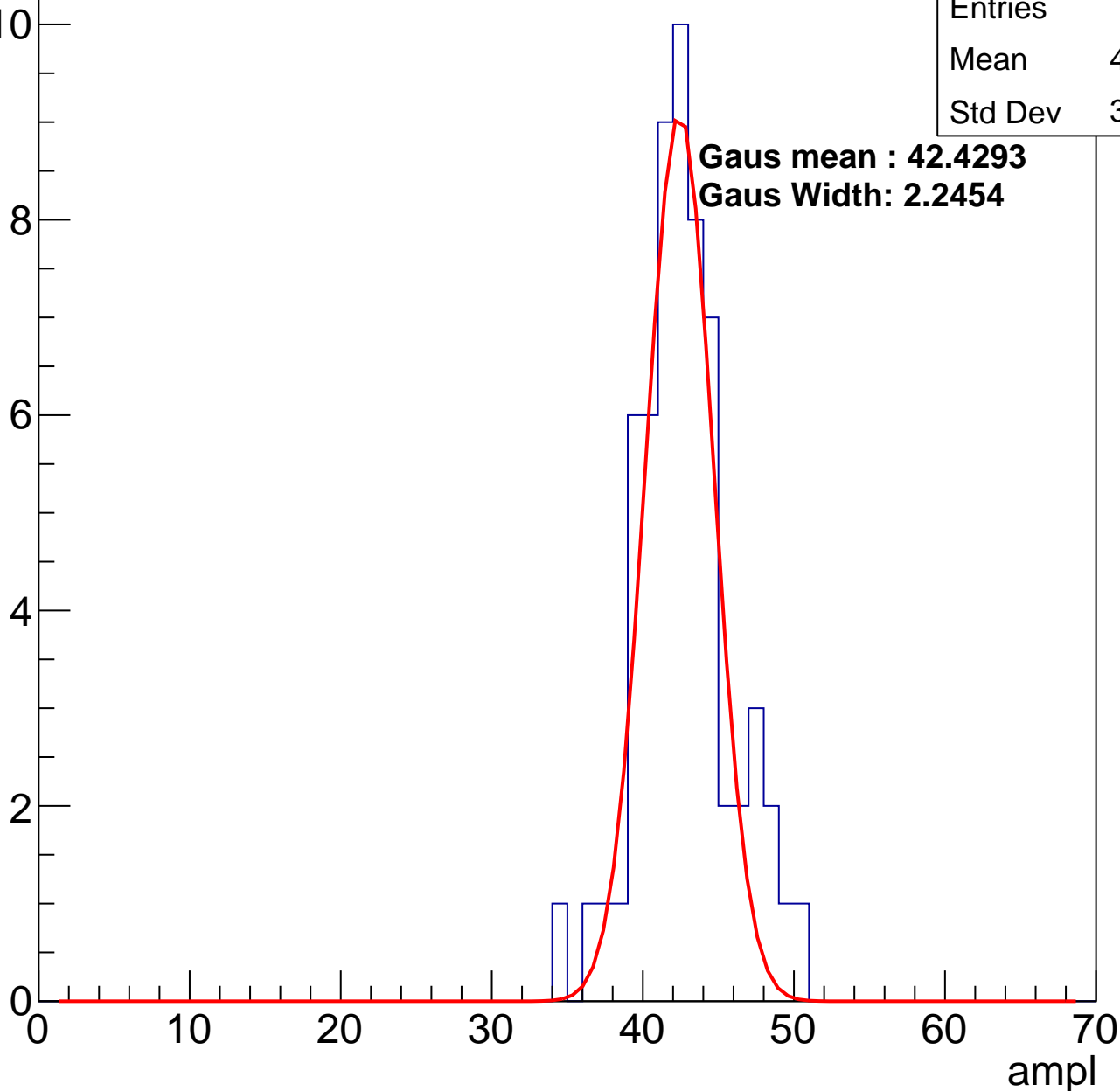
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	42.26
Std Dev	3.056

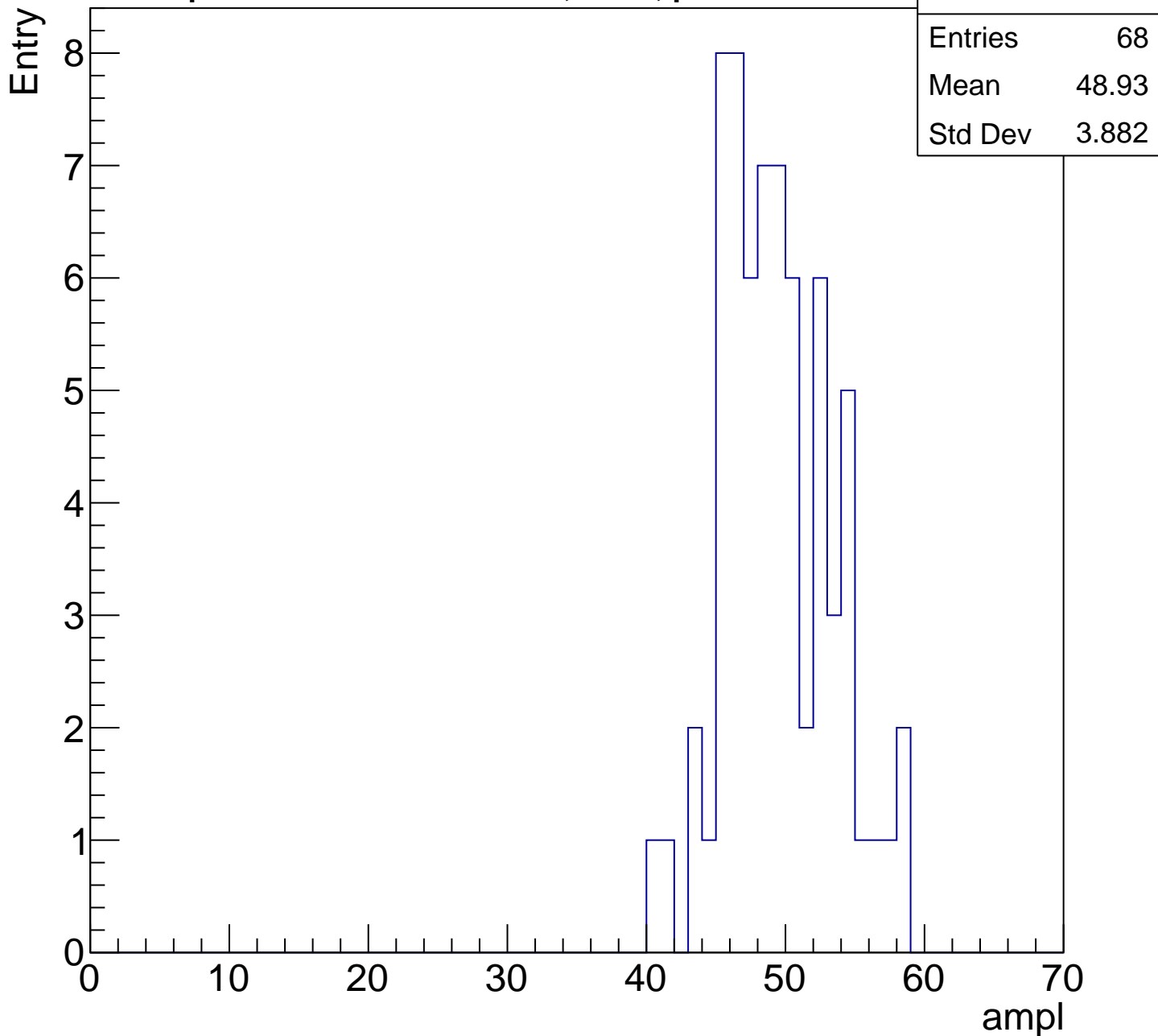
**Gaus mean : 42.4293**

**Gaus Width: 2.2454**



# B1L103S, U26-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

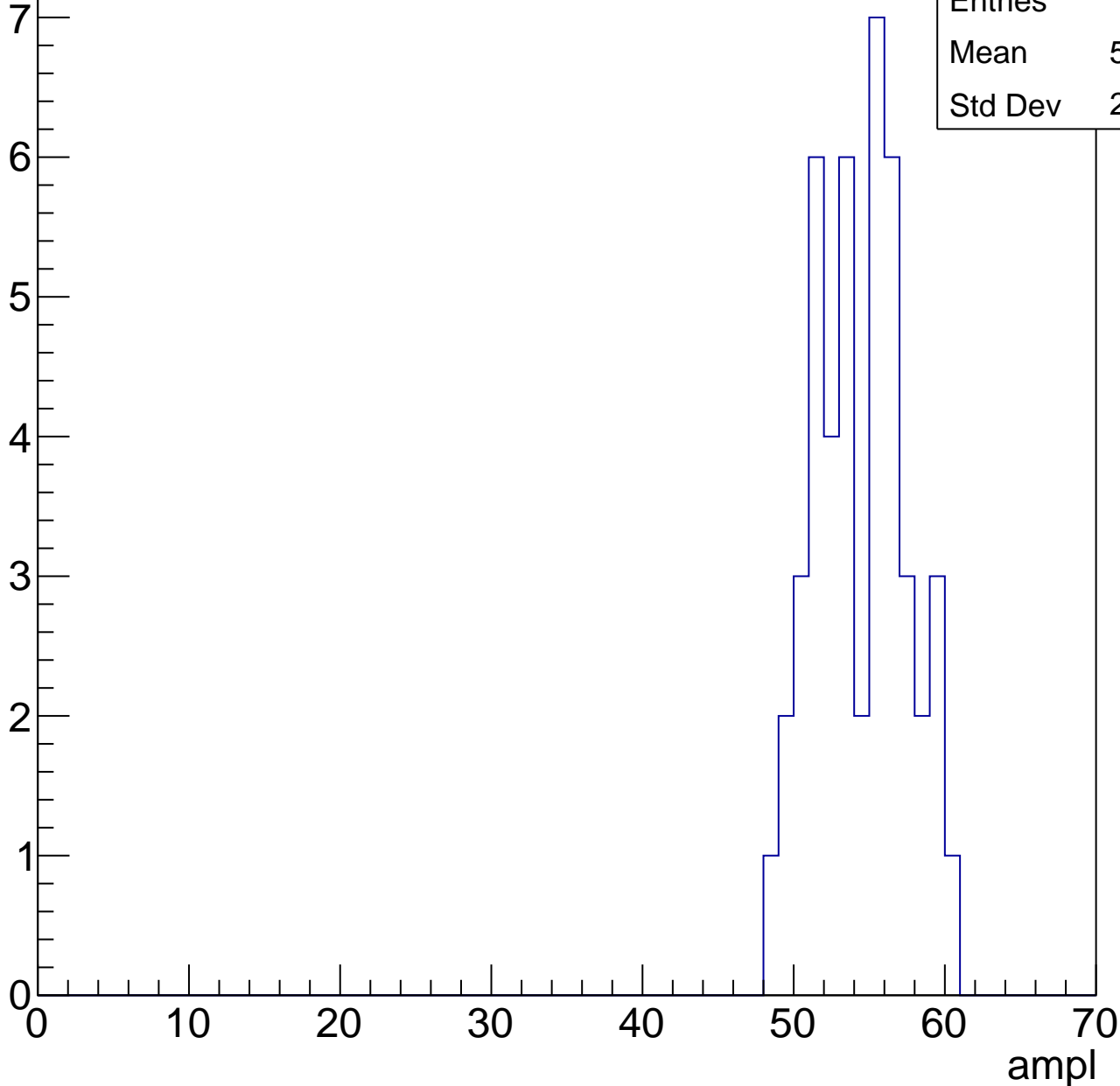


# B1L103S, U26-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	53.93
Std Dev	2.988

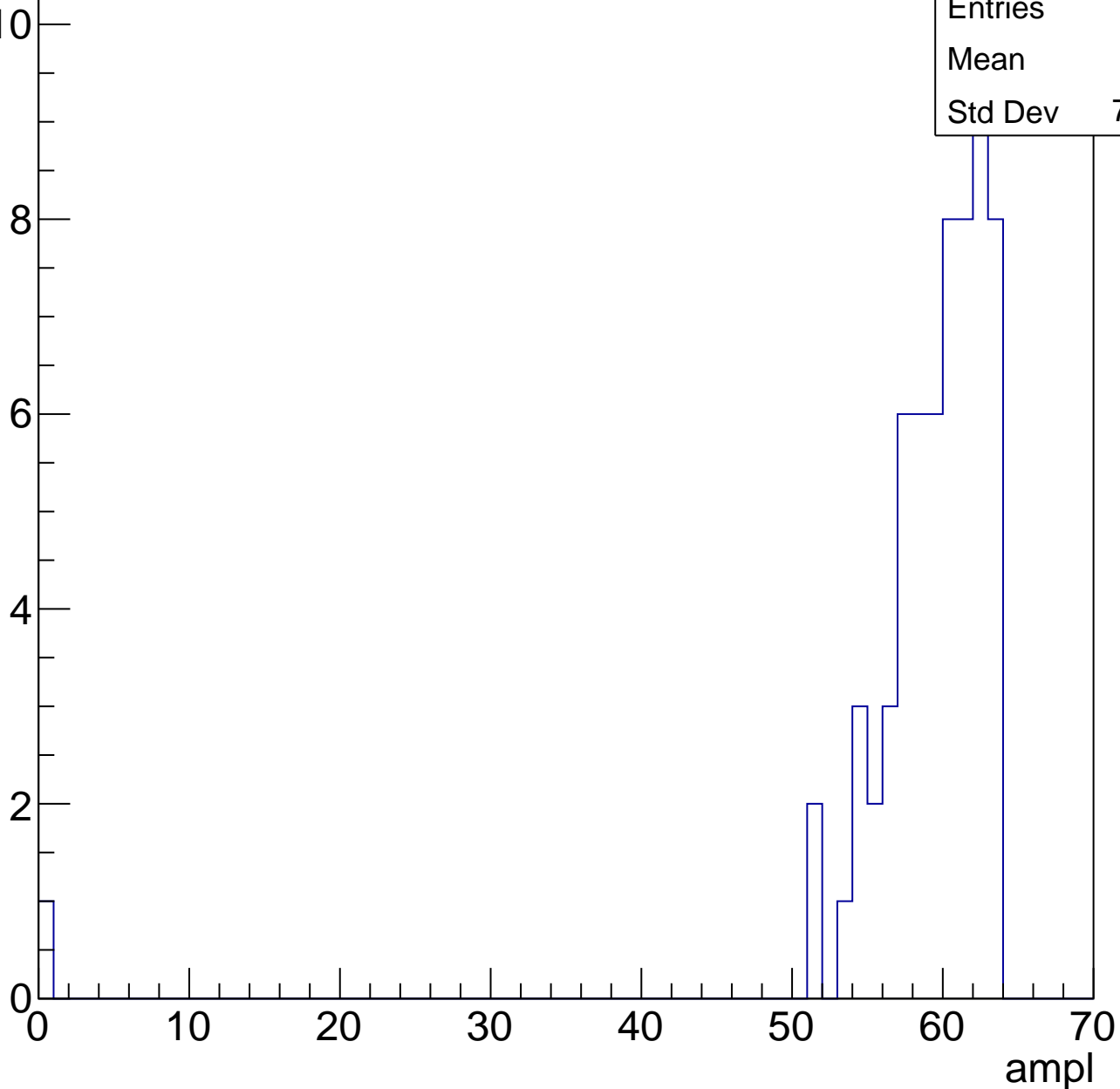


# B1L103S, U26-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	58.3
Std Dev	7.941



# B1L103S, U26-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

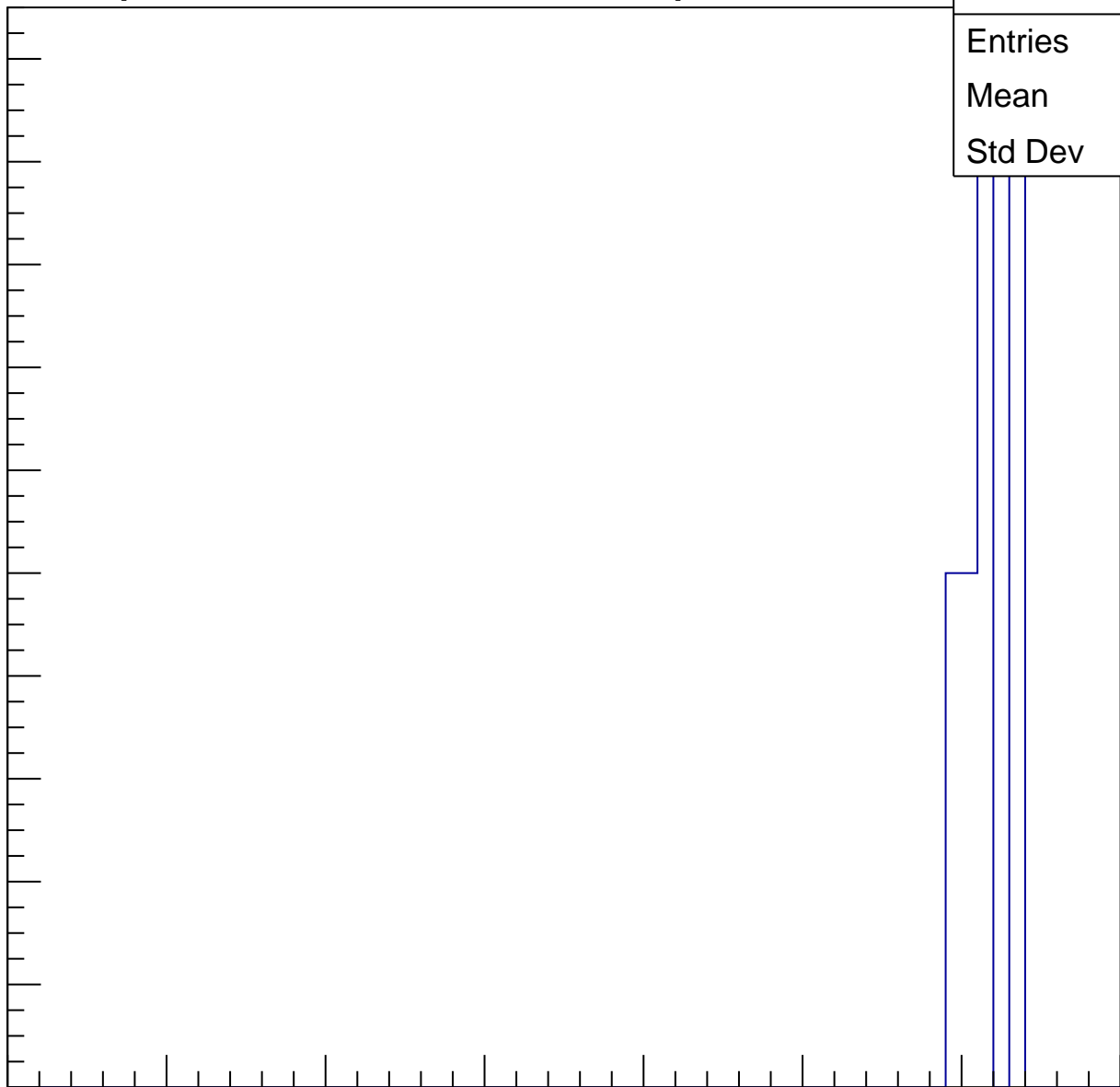
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.17
Std Dev	1.462

0 10 20 30 40 50 60 70

ampl

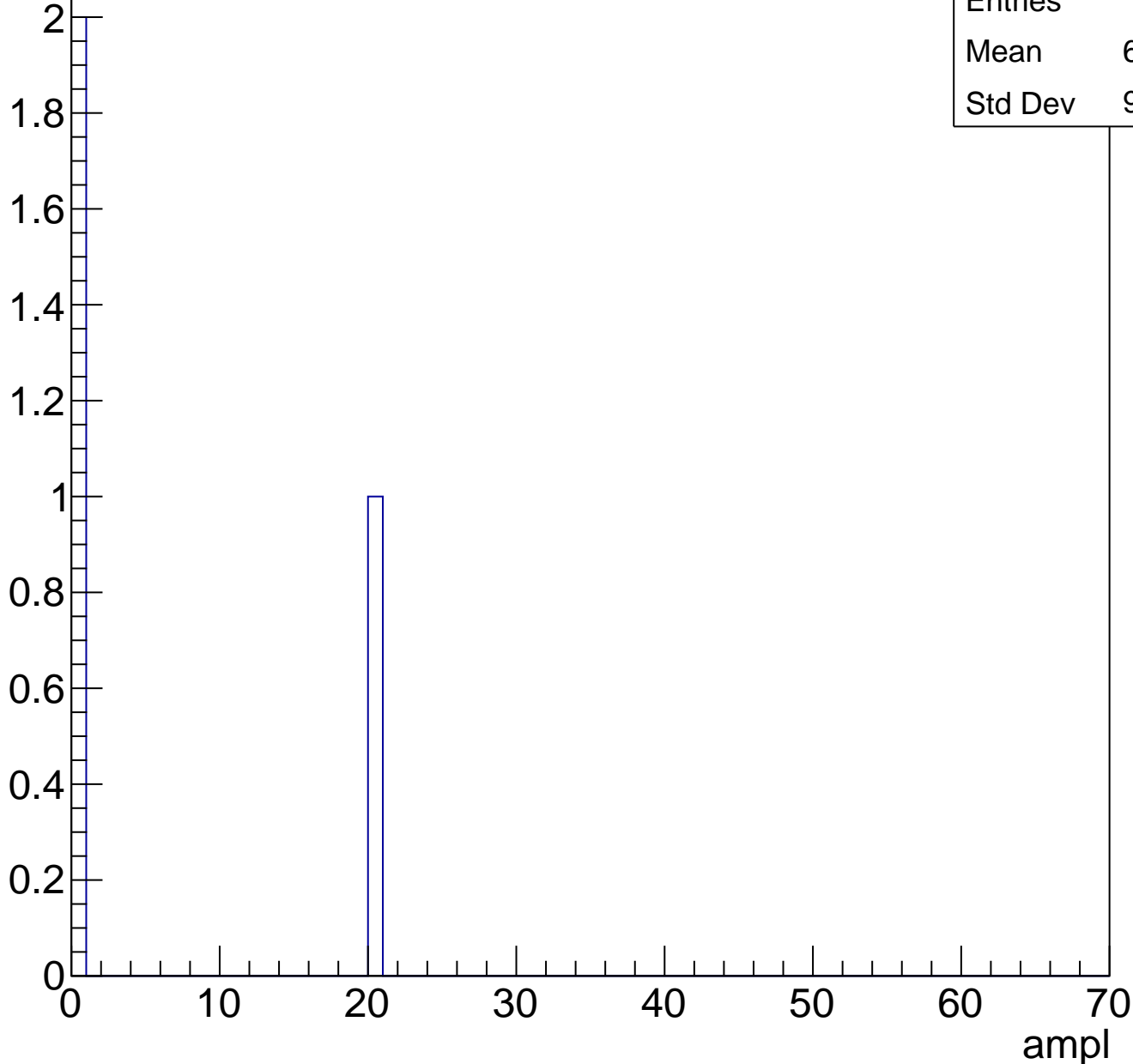




# B1L103S, U26-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	6.667
Std Dev	9.428

# B1L103S, U26-ch17, adc0

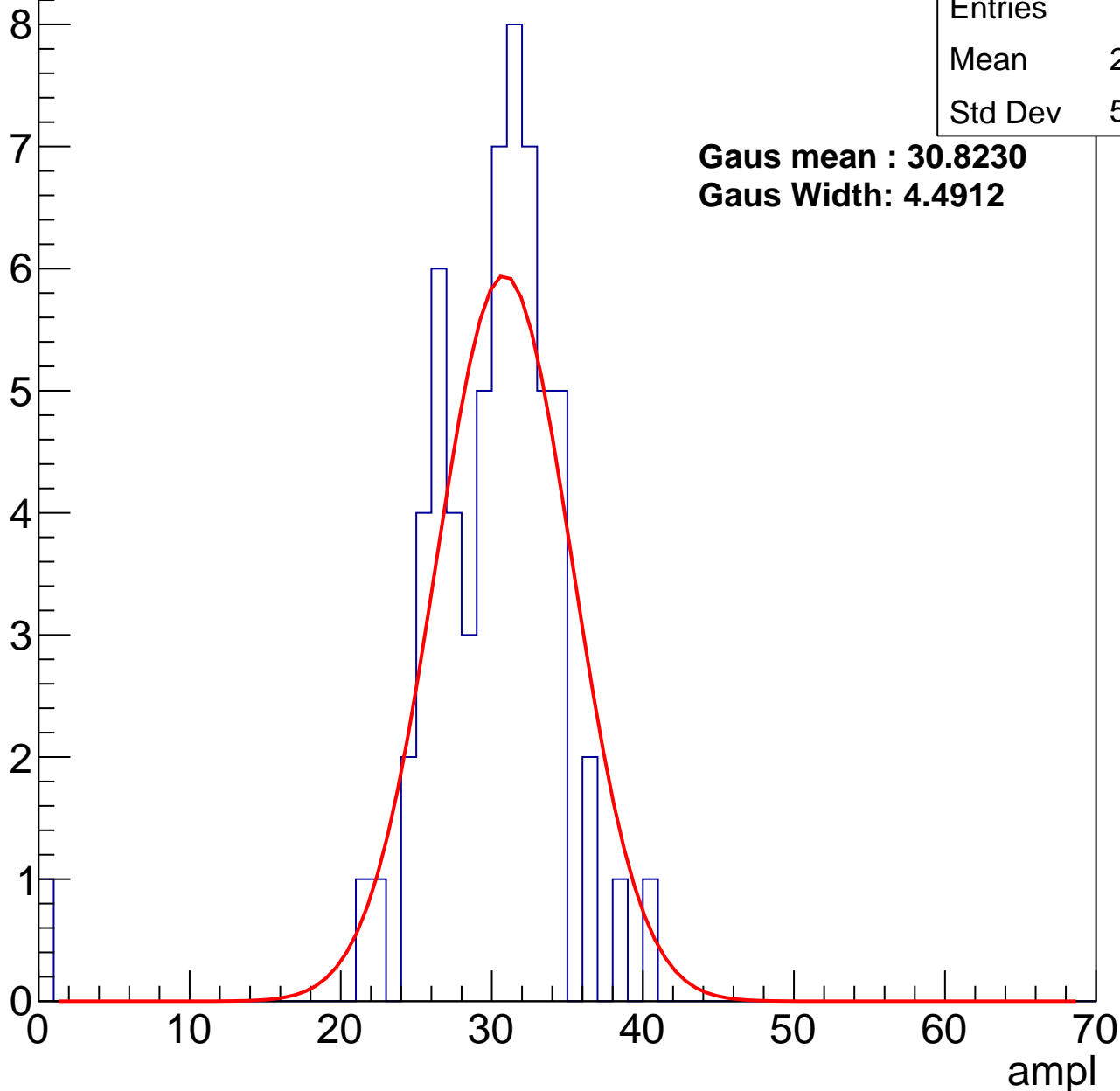
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	29.38
Std Dev	5.254

**Gaus mean : 30.8230**

**Gaus Width: 4.4912**



# B1L103S, U26-ch17, adc1

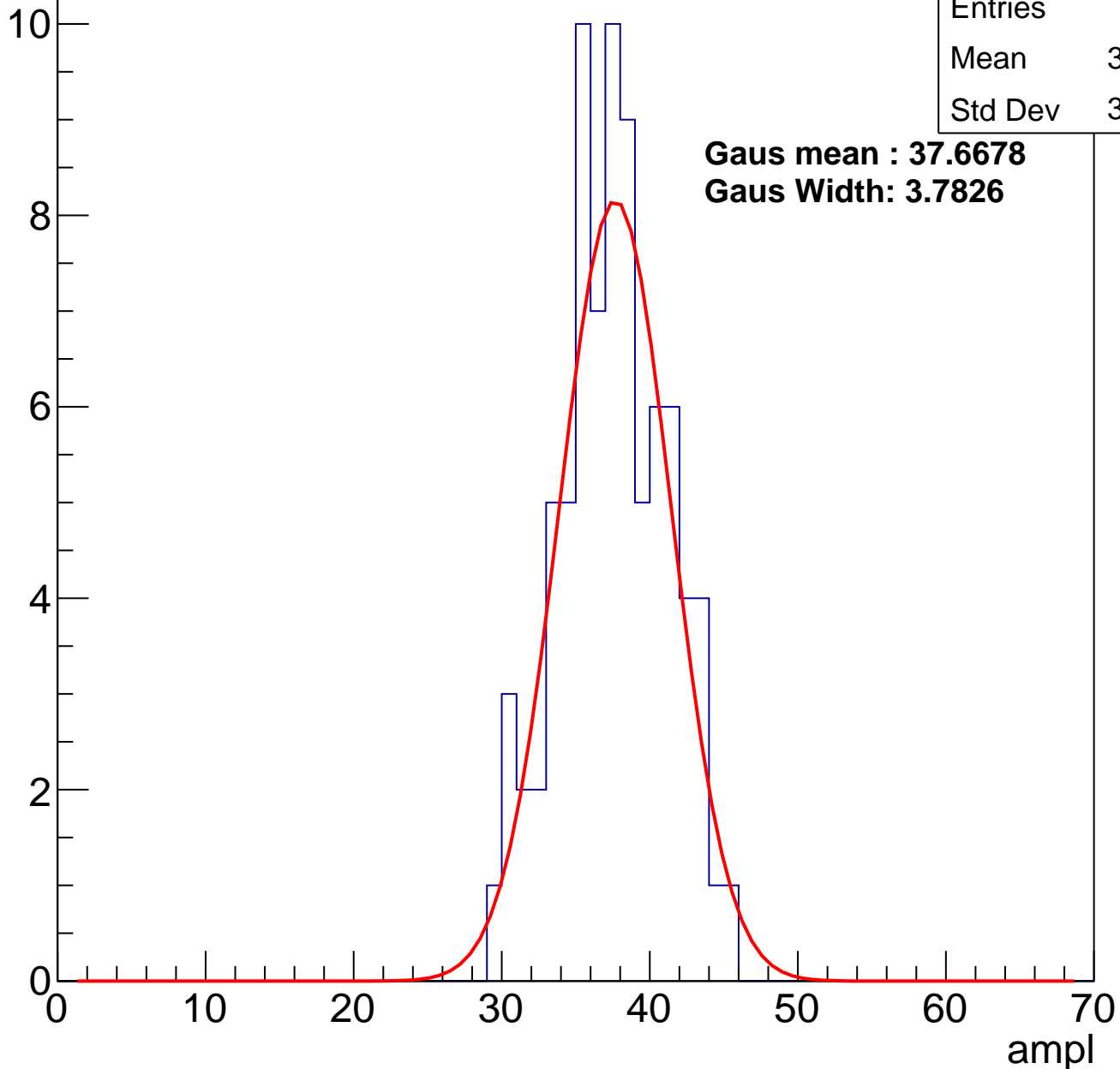
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	81
Mean	37.09
Std Dev	3.584

**Gaus mean : 37.6678**

**Gaus Width: 3.7826**

Entry



# B1L103S, U26-ch17, adc2

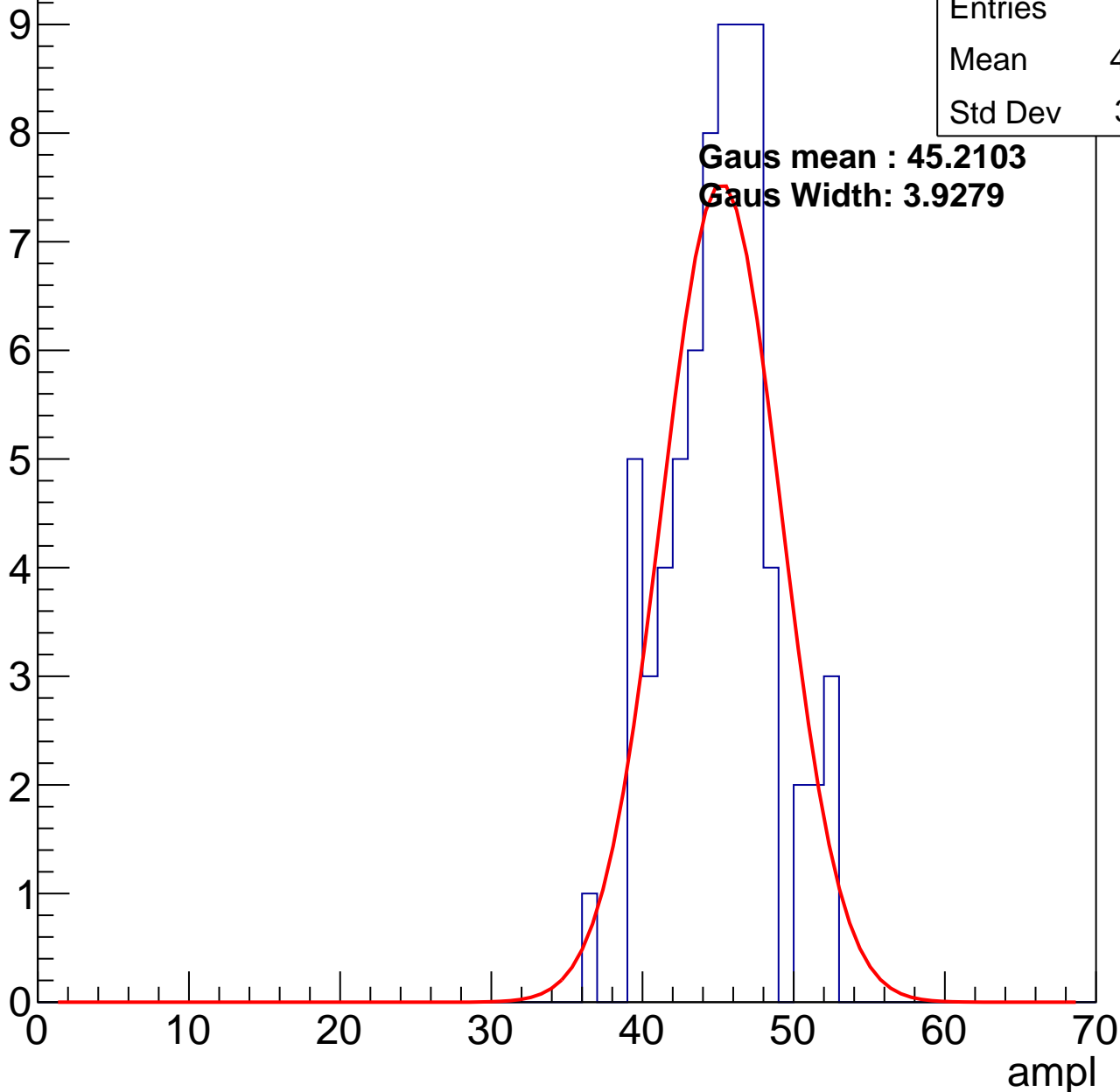
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	44.67
Std Dev	3.421

**Gaus mean : 45.2103**

**Gaus Width: 3.9279**

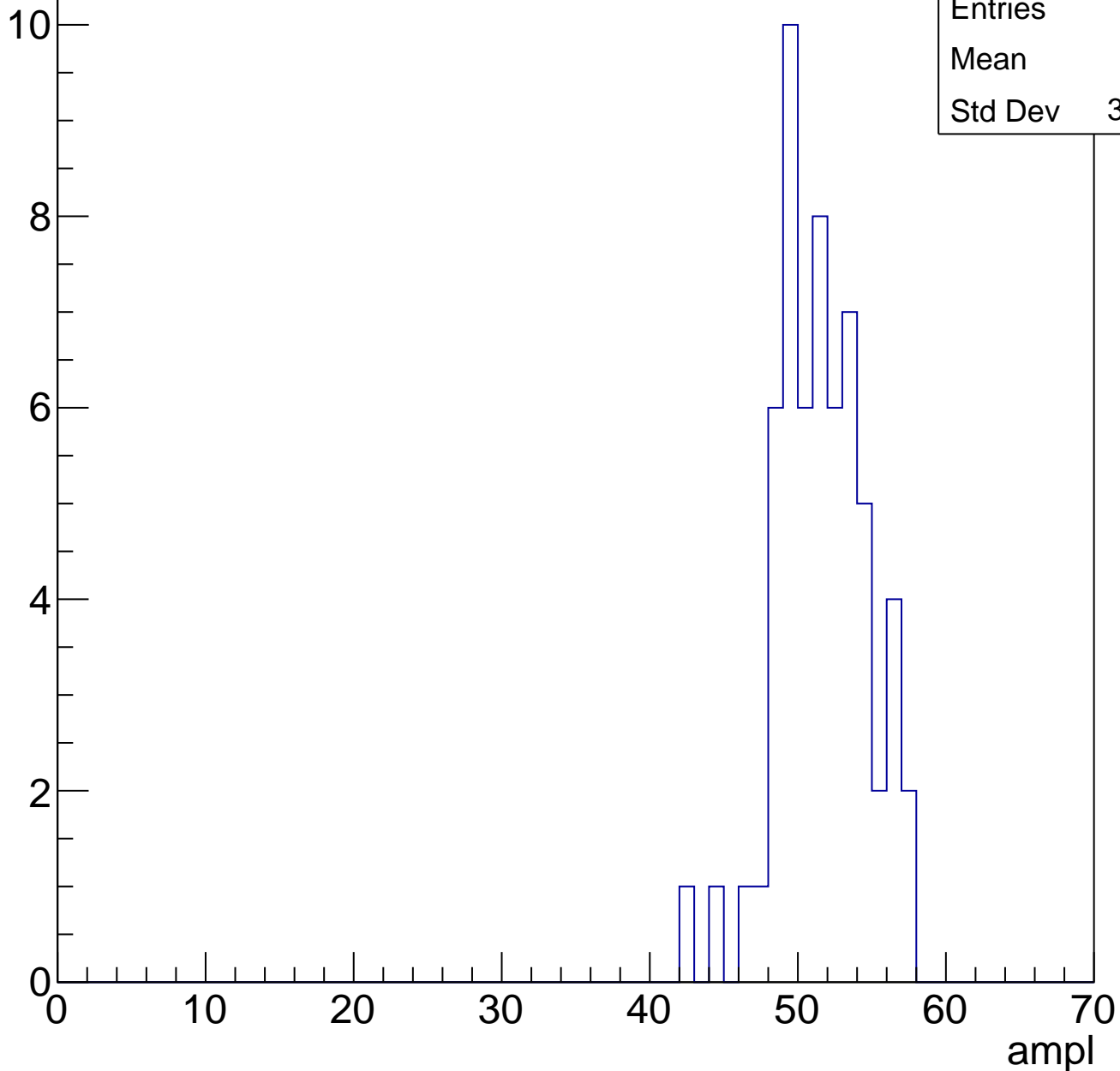


# B1L103S, U26-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	60
Mean	51.1
Std Dev	3.037

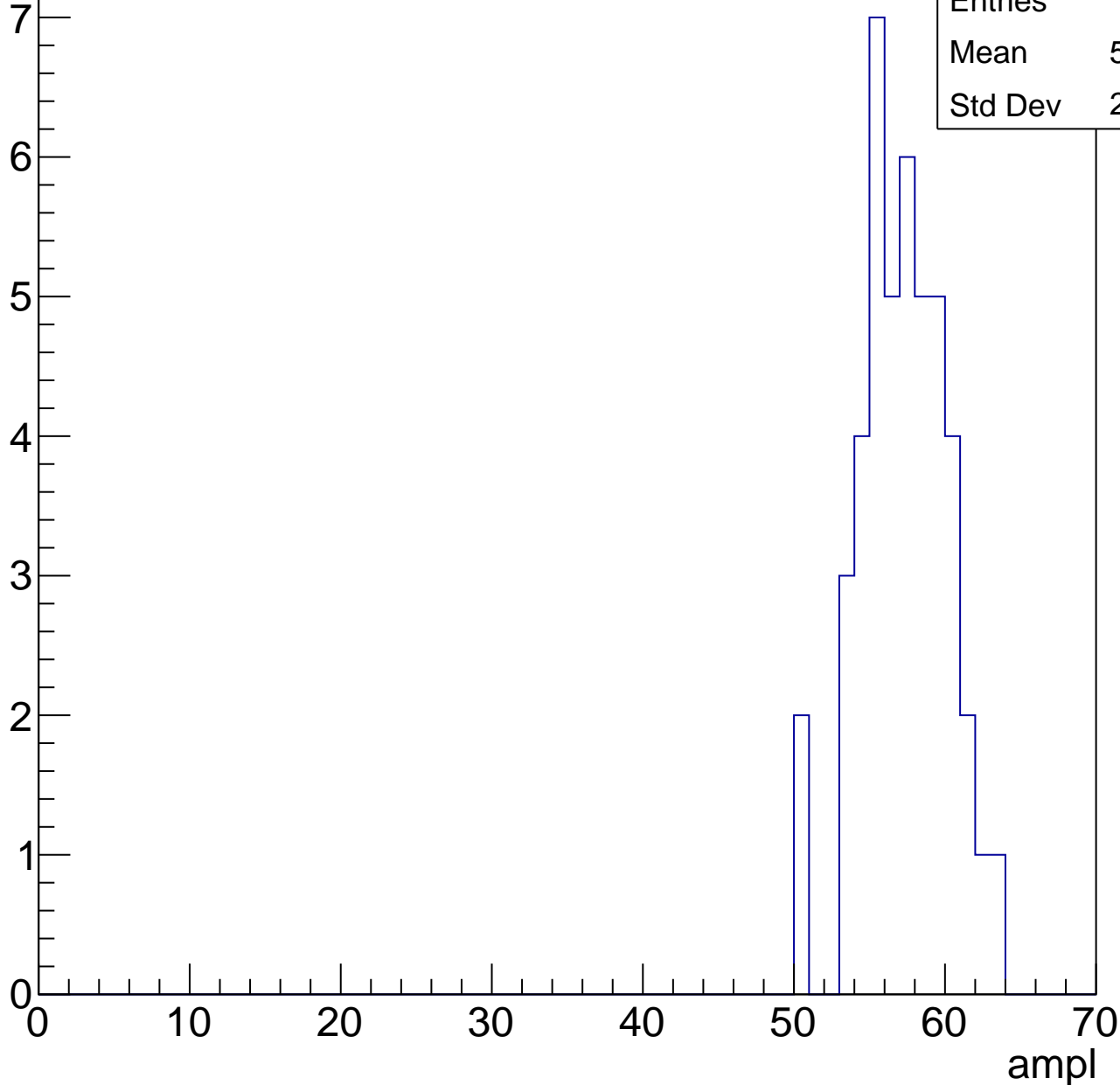
Entry



# B1L103S, U26-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

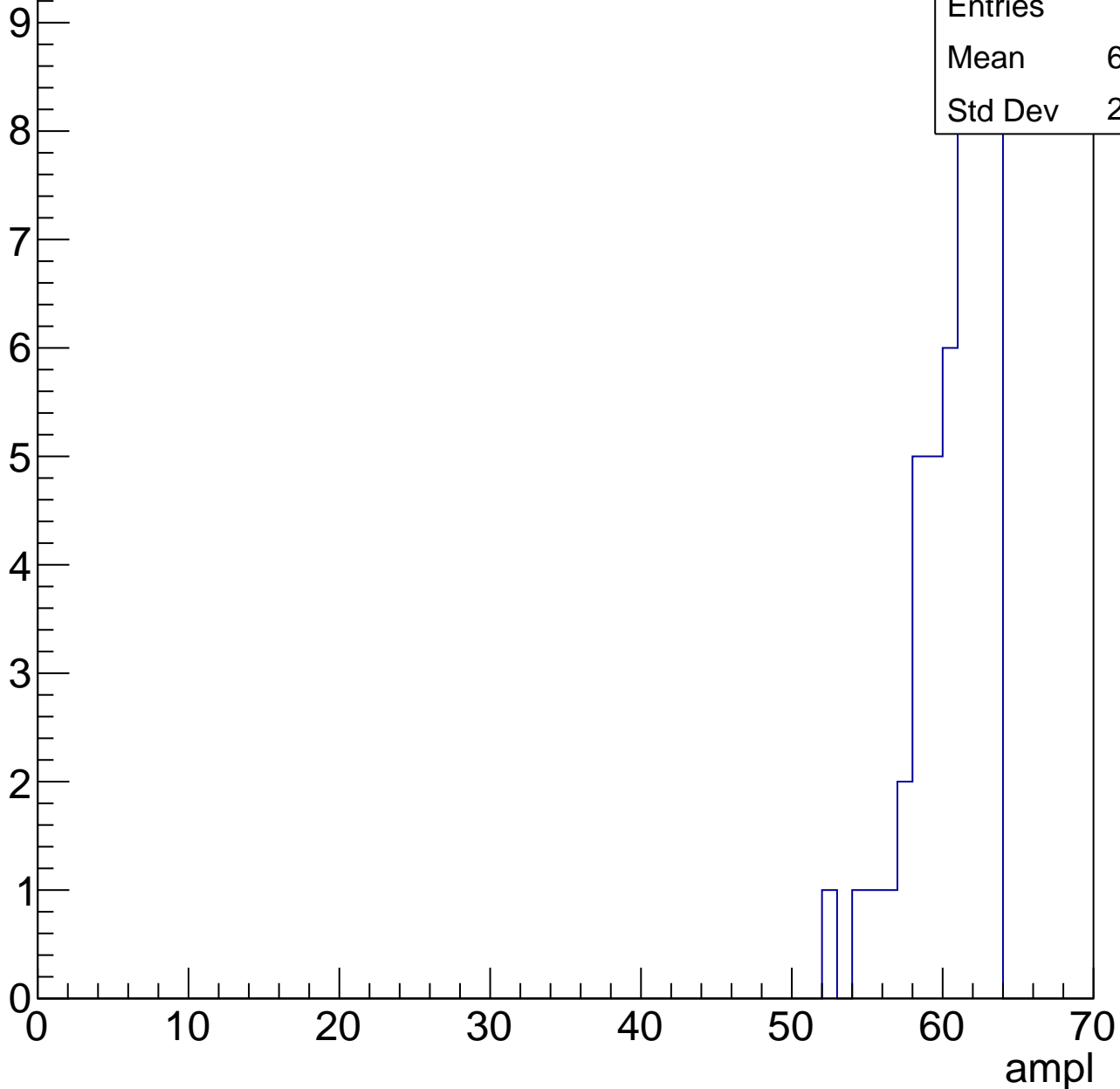


Entries	45
Mean	56.76
Std Dev	2.853

# B1L103S, U26-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	47
Mean	60.13
Std Dev	2.523

# B1L103S, U26-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U26-ch18, adc0

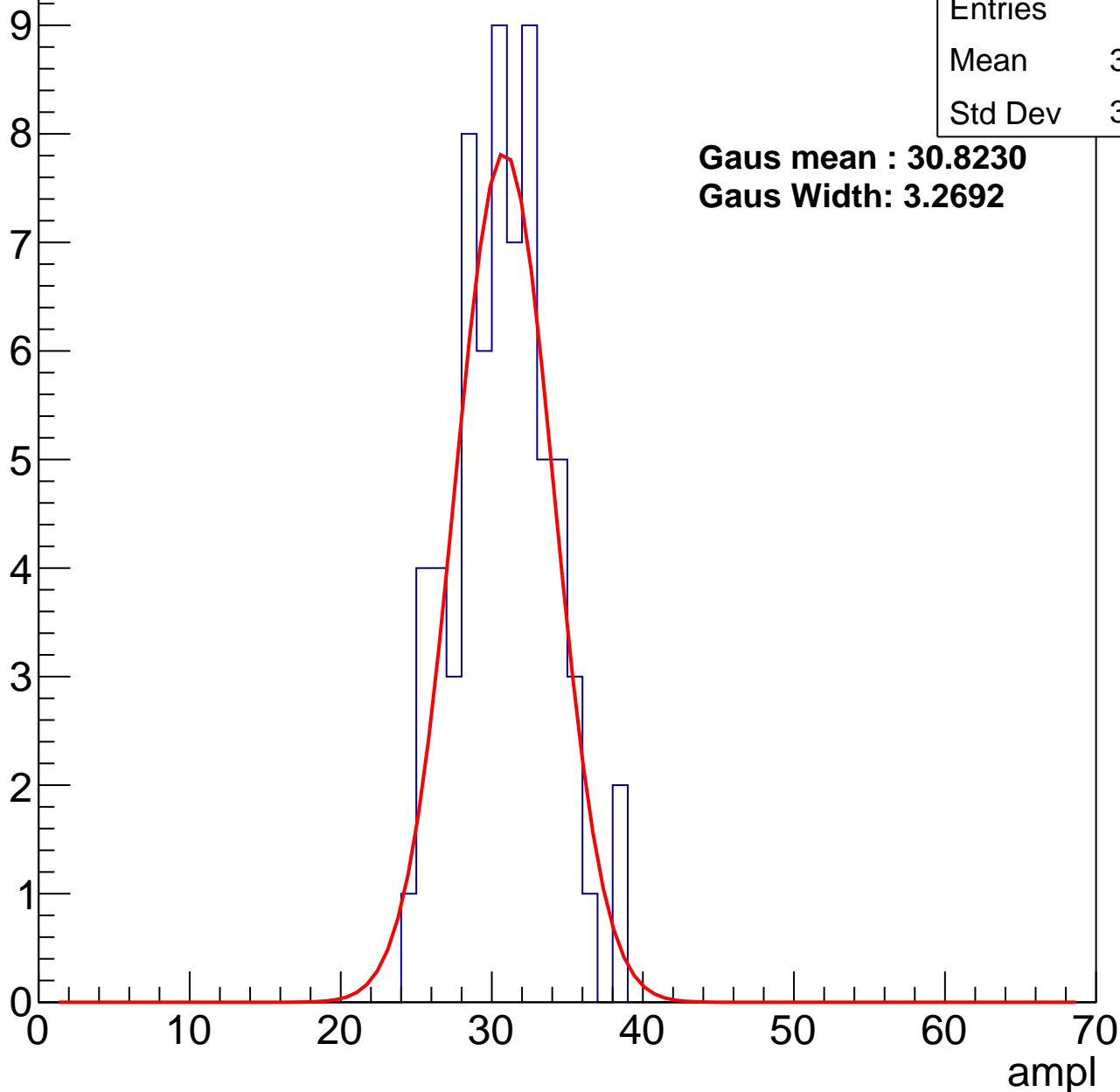
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	30.36
Std Dev	3.147

**Gaus mean : 30.8230**

**Gaus Width: 3.2692**



# B1L103S, U26-ch18, adc1

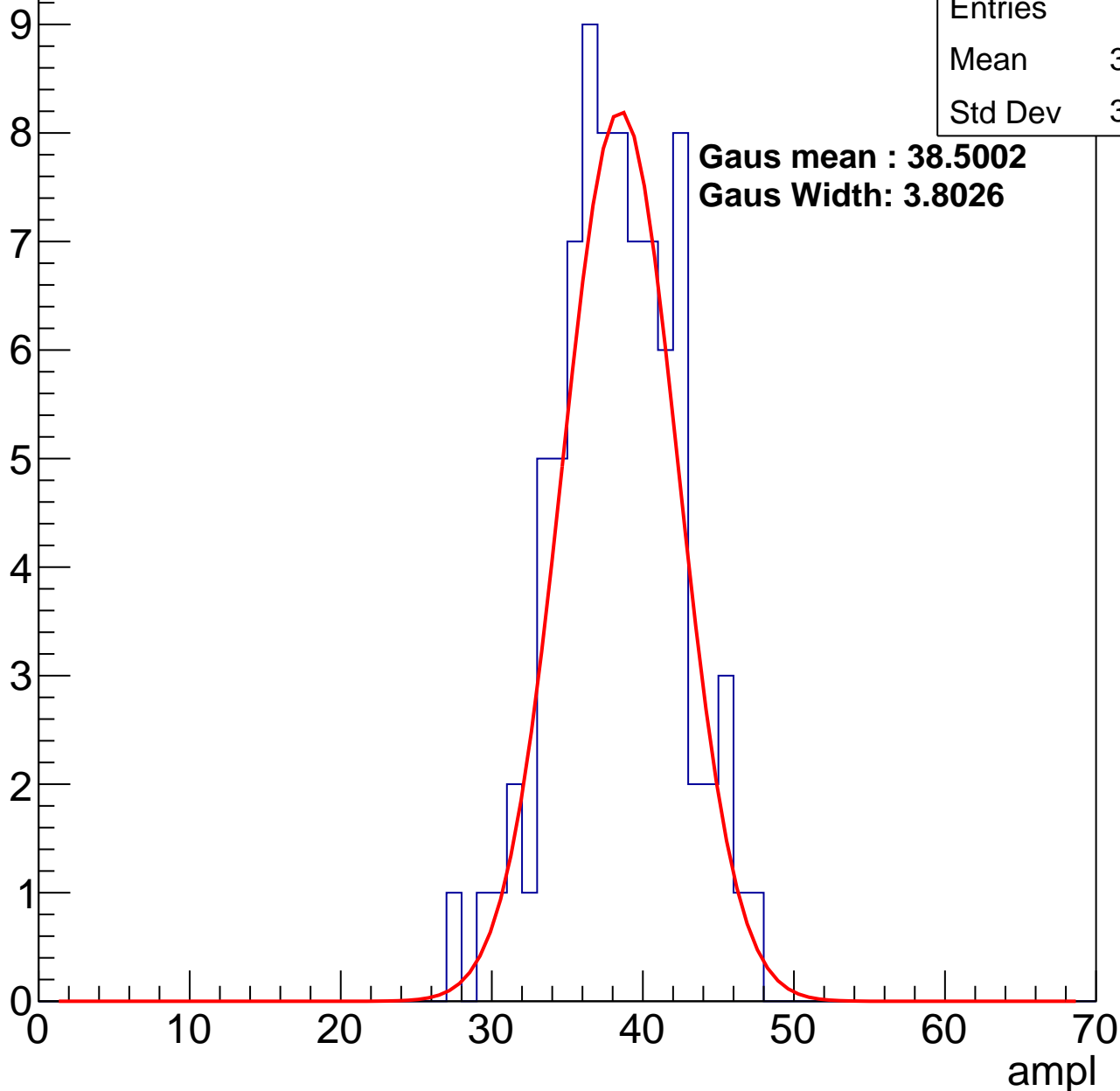
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	85
Mean	37.89
Std Dev	3.974

**Gaus mean : 38.5002**

**Gaus Width: 3.8026**



# B1L103S, U26-ch18, adc2

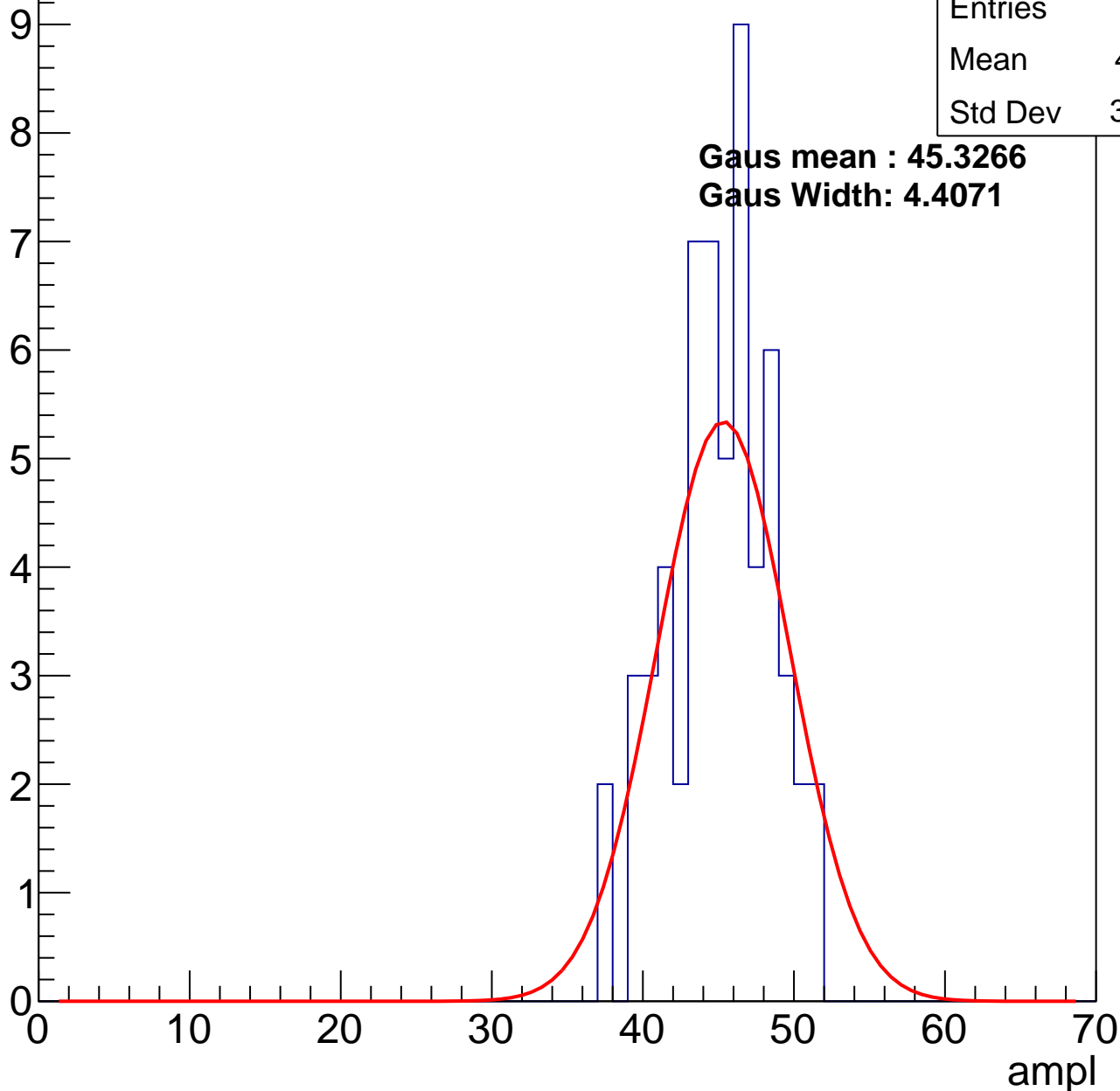
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	44.61
Std Dev	3.365

**Gaus mean : 45.3266**

**Gaus Width: 4.4071**

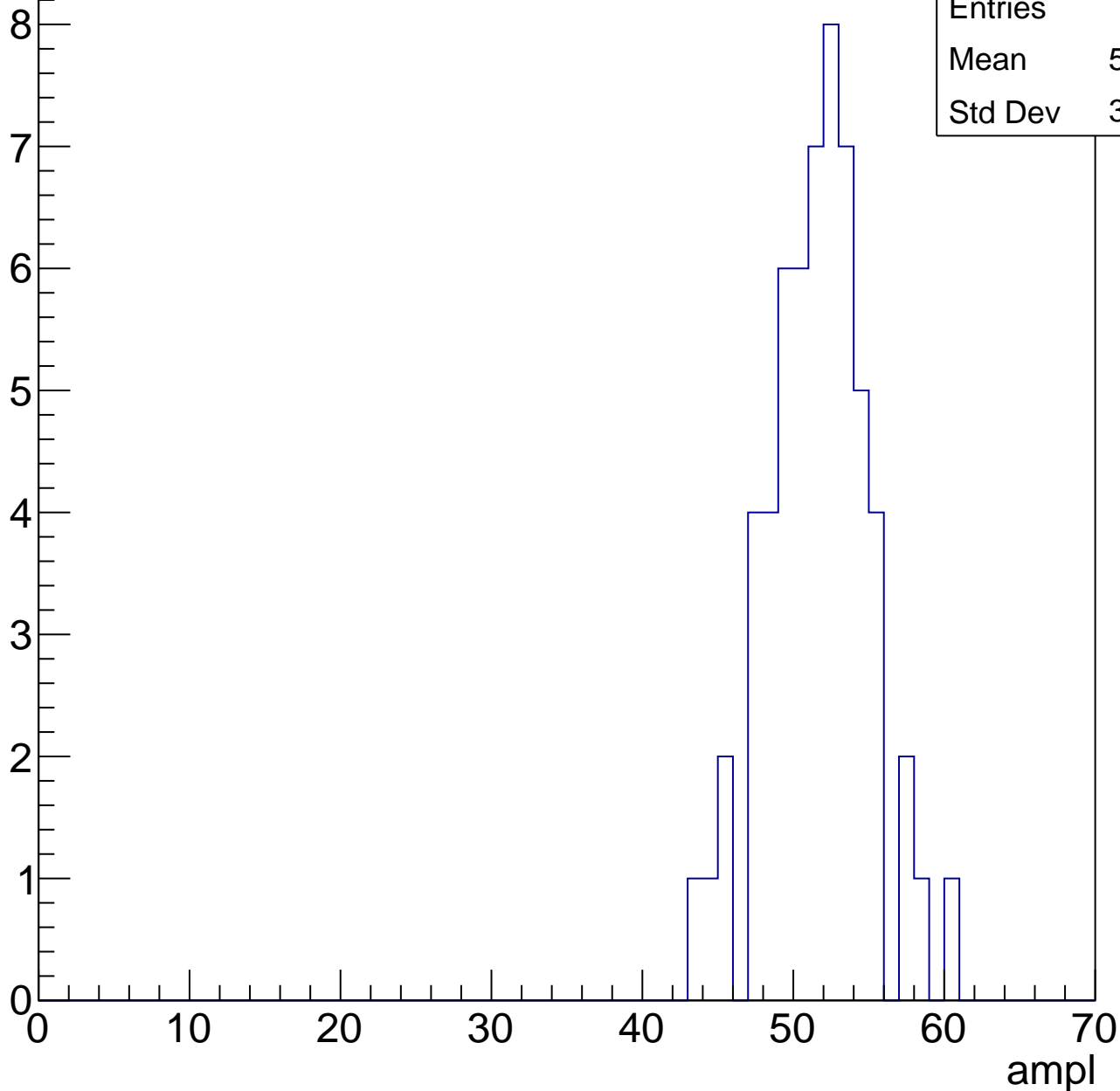


# B1L103S, U26-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	51.14
Std Dev	3.347



# B1L103S, U26-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	60
Mean	56.53
Std Dev	3.344

Entry

10

8

6

4

2

0

0

10

20

30

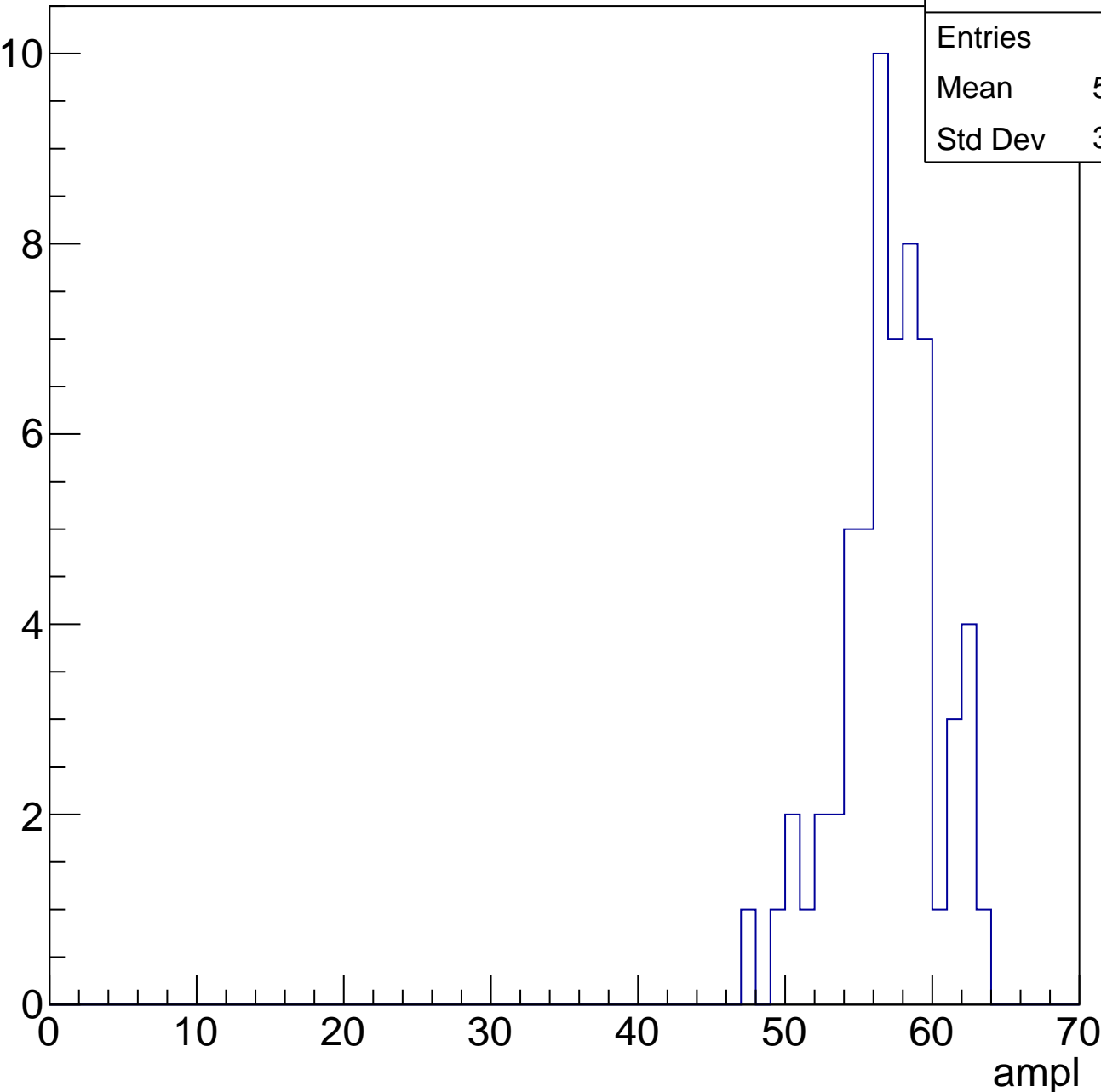
40

50

60

70

ampl



# B1L103S, U26-ch18, adc5

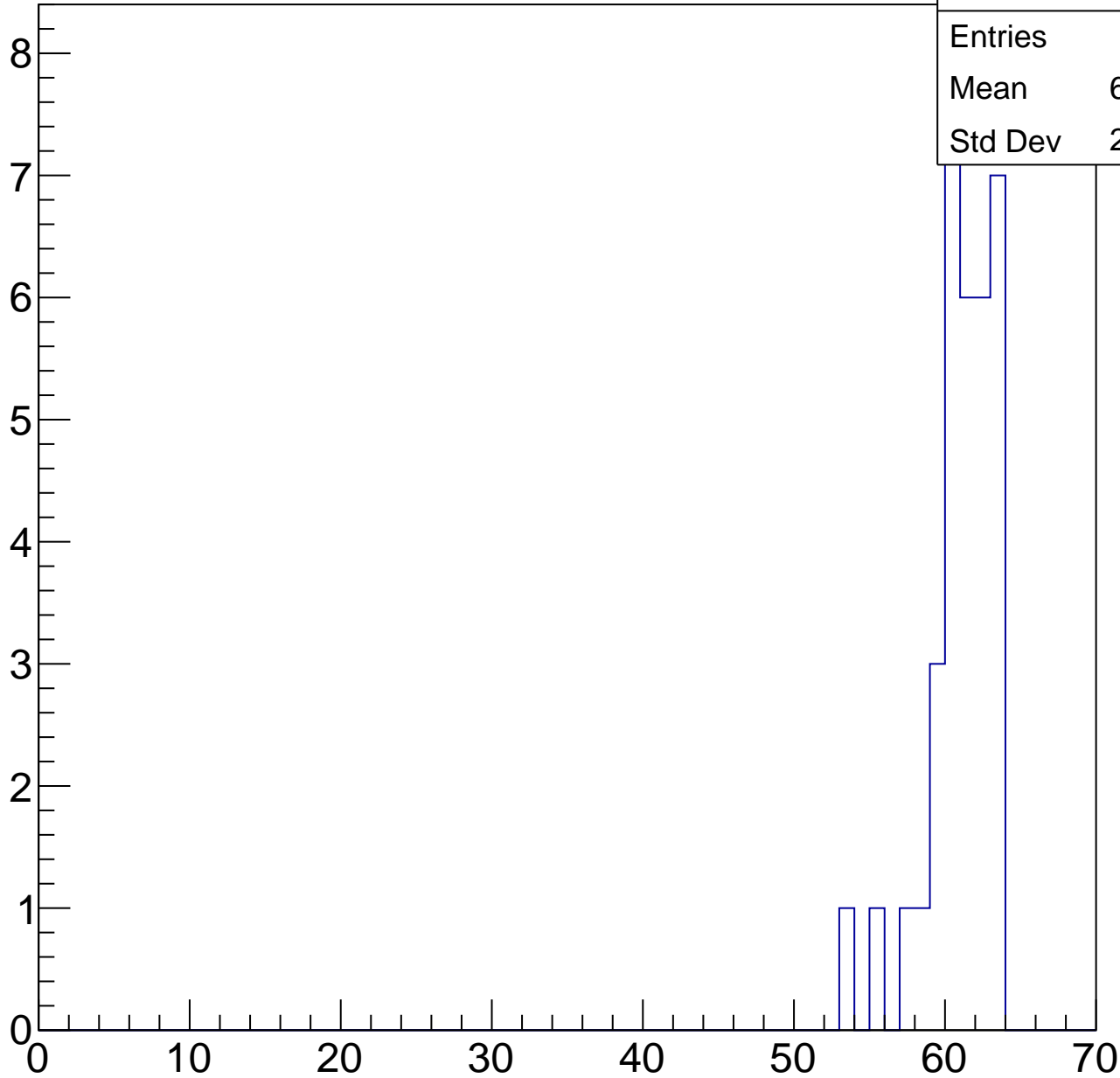
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	34
Mean	60.56
Std Dev	2.252

ampl



# B1L103S, U26-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

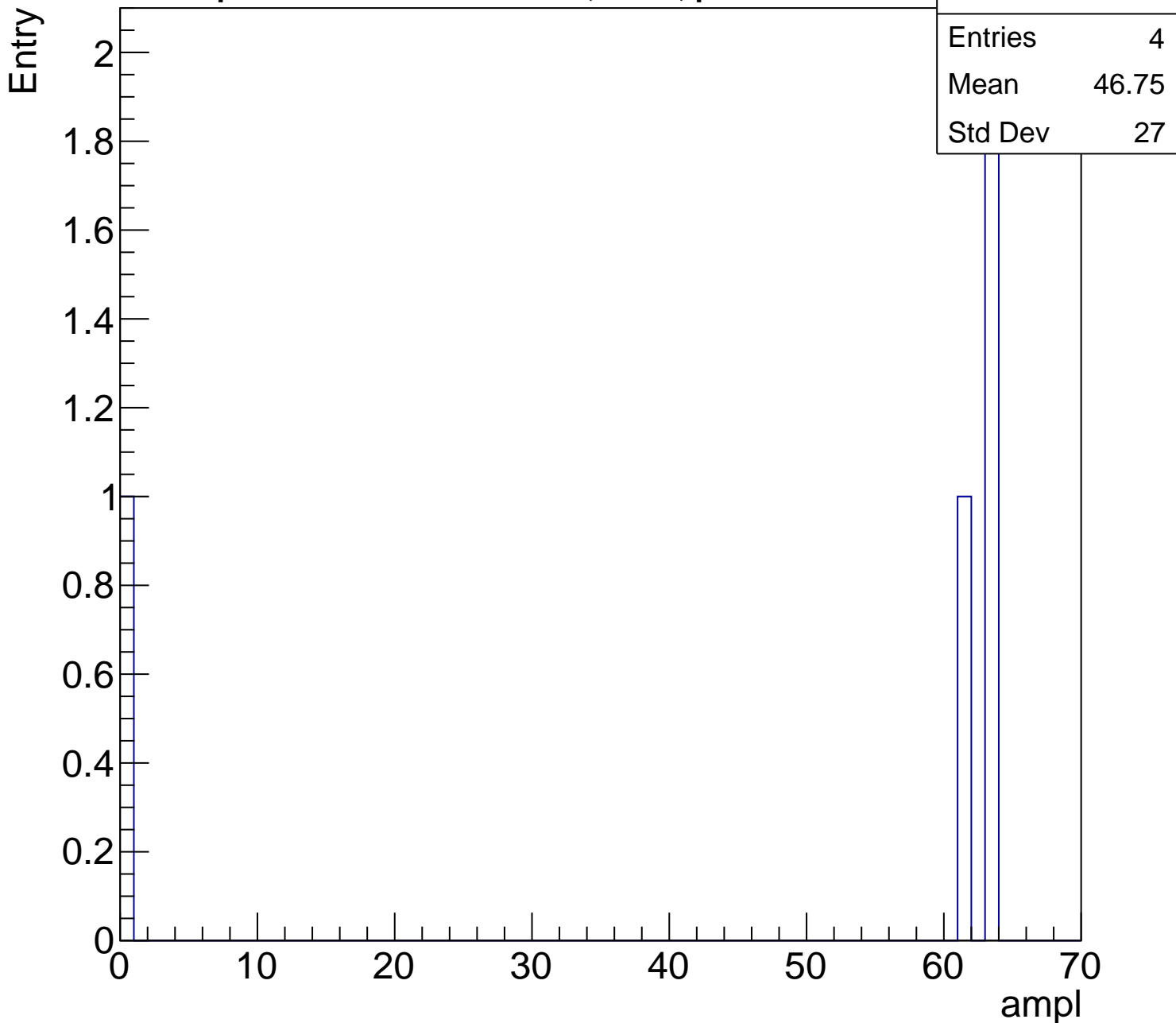
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	46.75
Std Dev	27

0 10 20 30 40 50 60 70

ampl





# B1L103S, U26-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch19, adc0

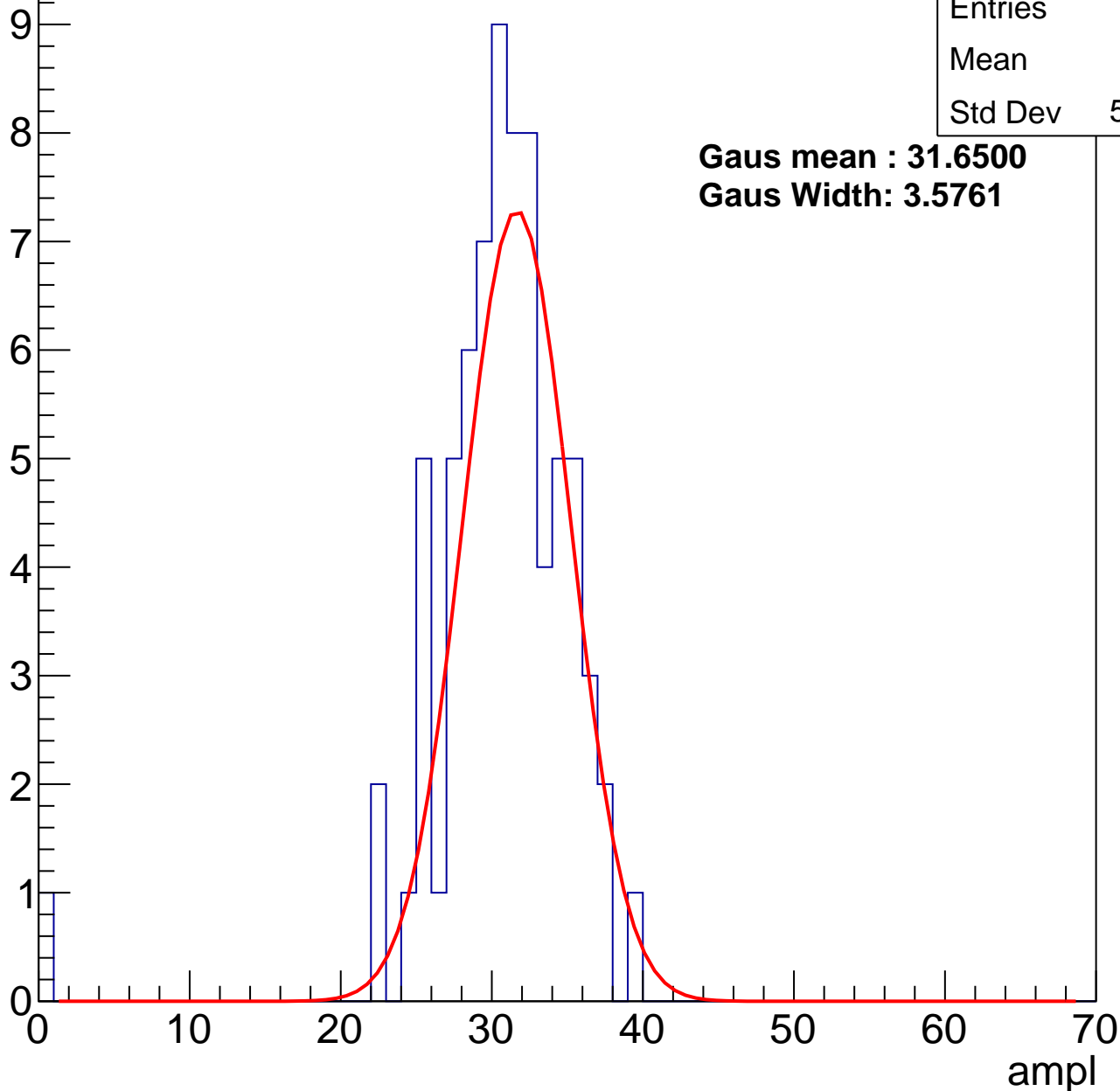
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	30.1
Std Dev	5.032

**Gaus mean : 31.6500**

**Gaus Width: 3.5761**



# B1L103S, U26-ch19, adc1

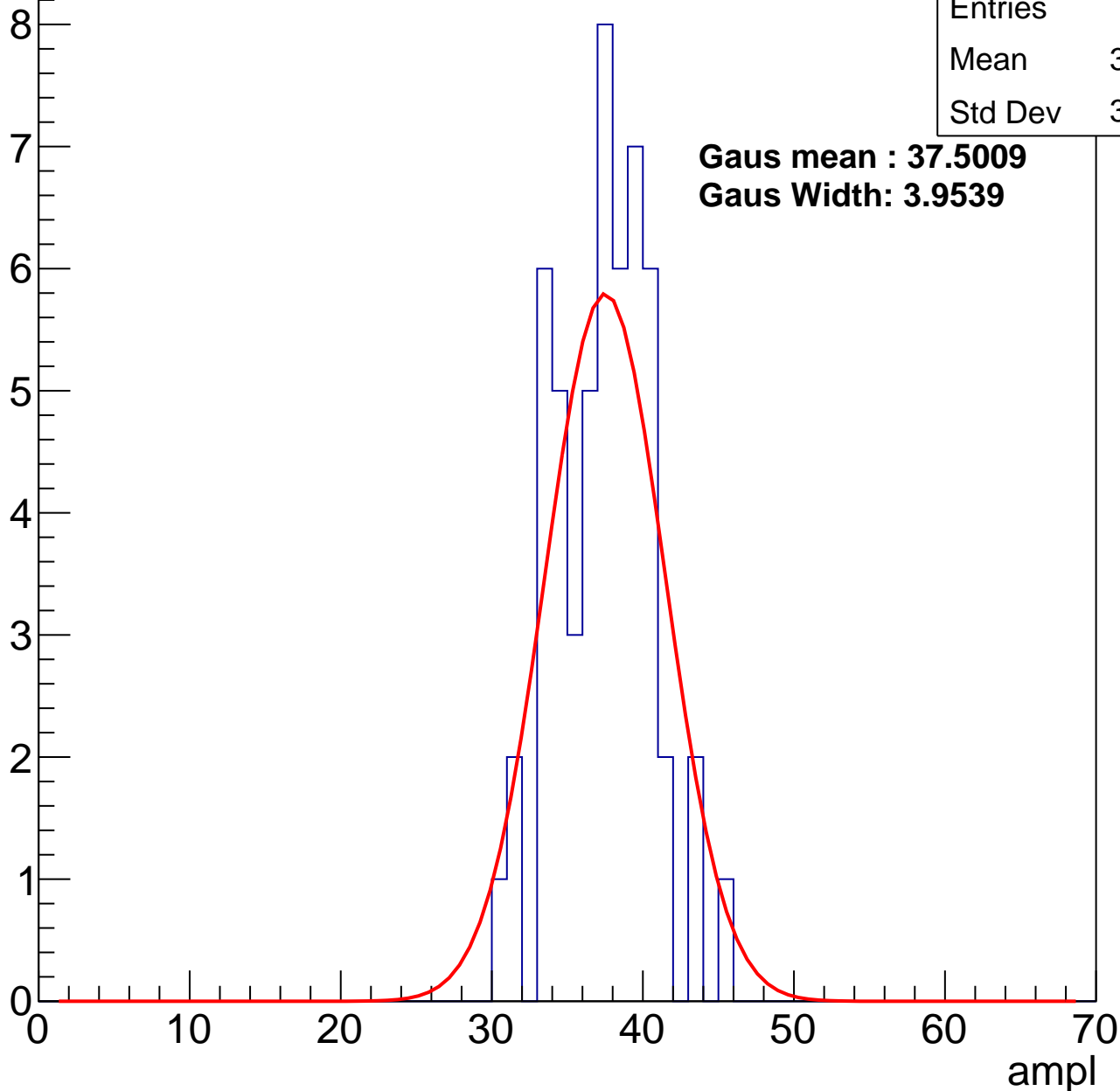
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	36.94
Std Dev	3.147

**Gaus mean : 37.5009**

**Gaus Width: 3.9539**



# B1L103S, U26-ch19, adc2

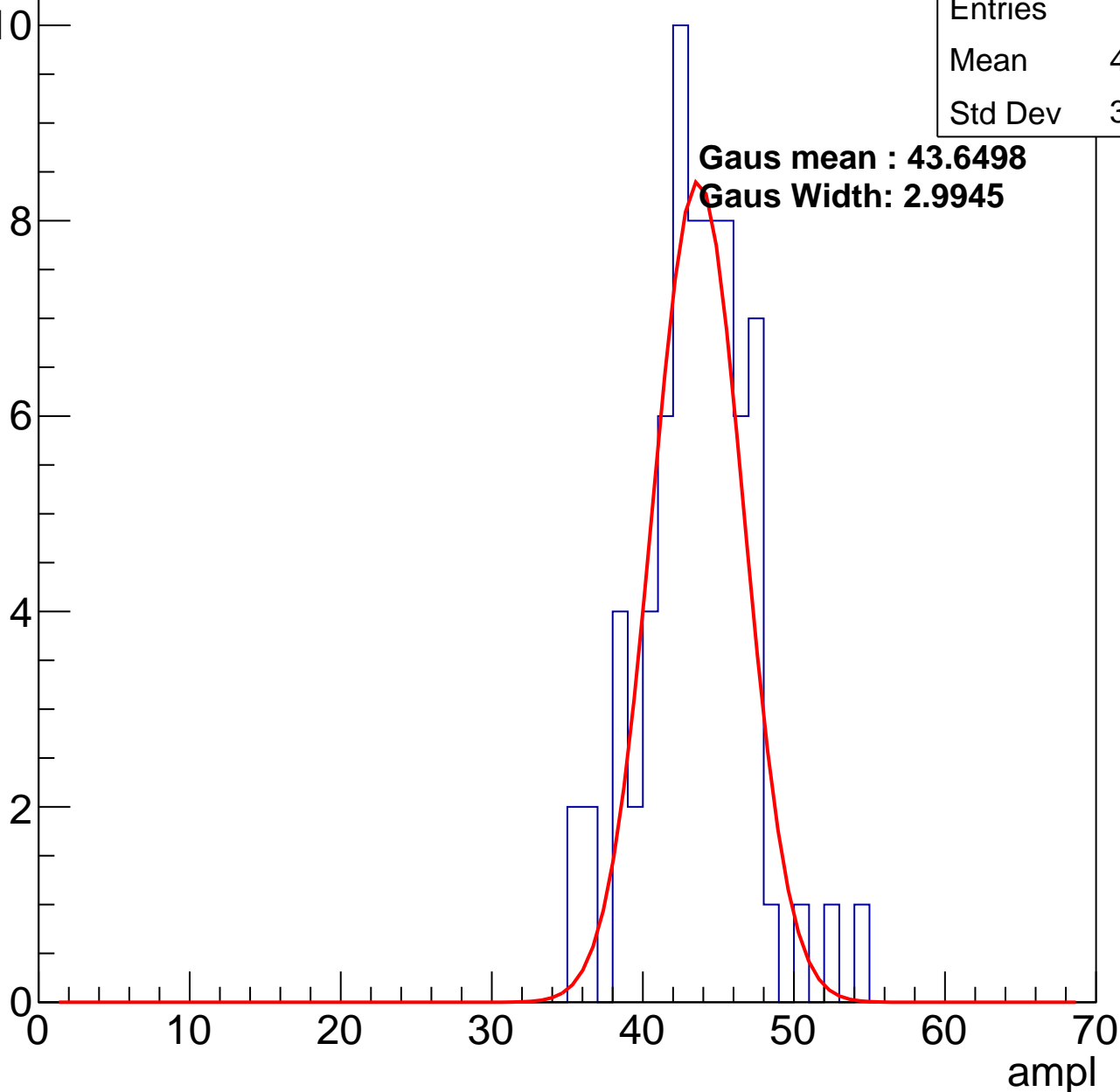
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	43.14
Std Dev	3.577

**Gaus mean : 43.6498**

**Gaus Width: 2.9945**

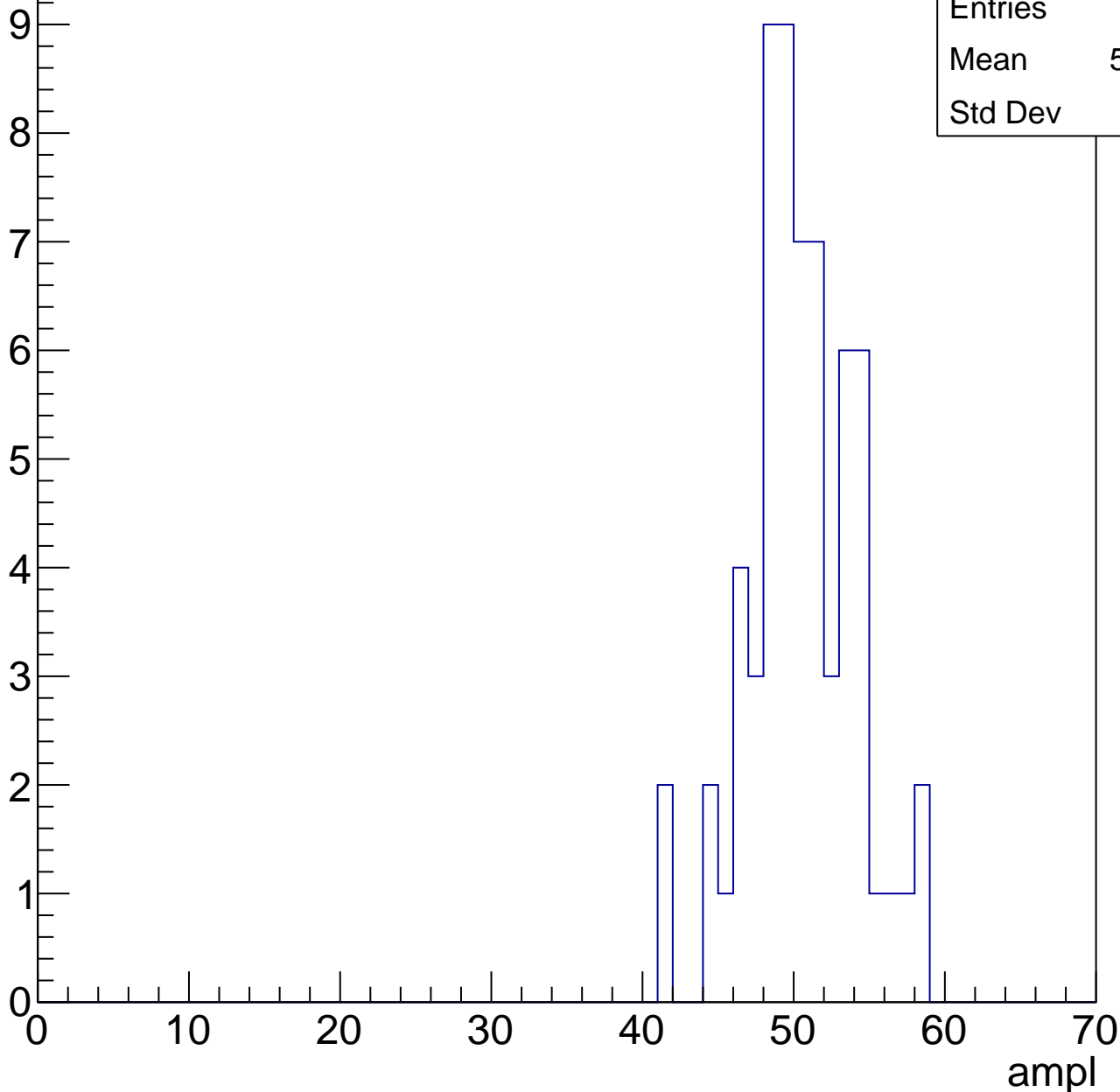


# B1L103S, U26-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

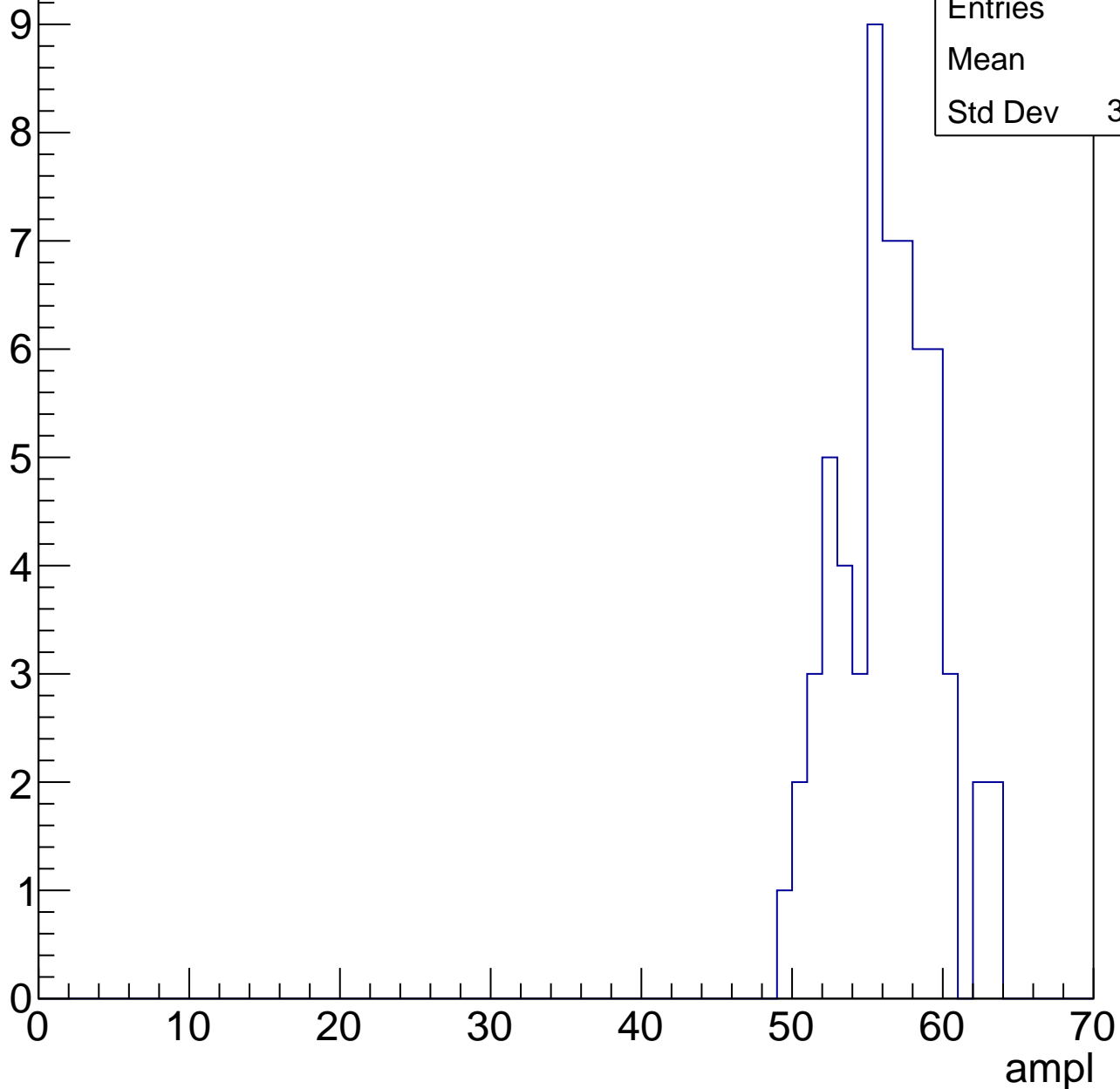
Entries	64
Mean	50.03
Std Dev	3.54



# B1L103S, U26-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



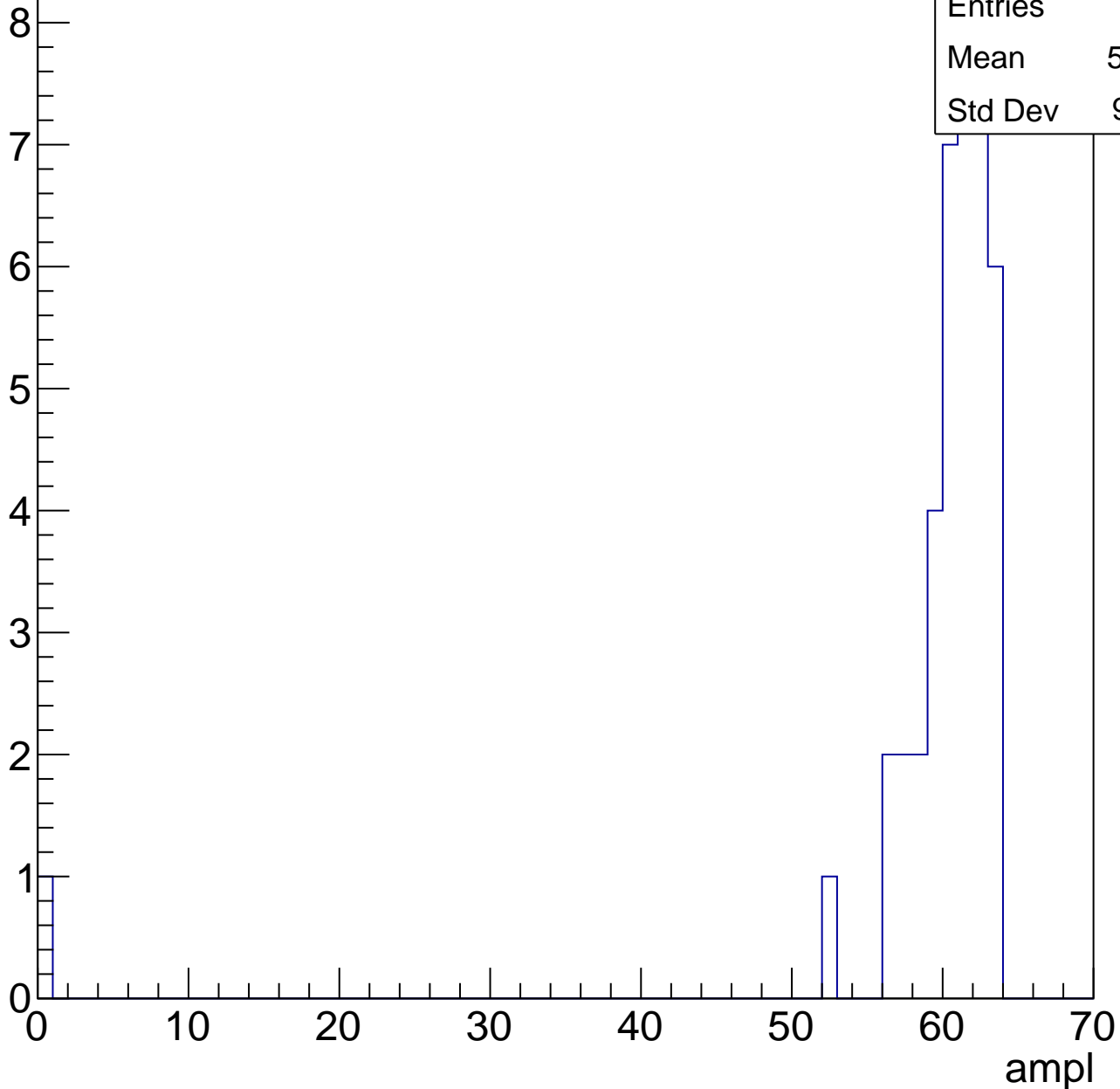
Entries	60
Mean	55.9
Std Dev	3.254

# B1L103S, U26-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	41
Mean	58.83
Std Dev	9.581



# B1L103S, U26-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L103S, U26-ch20, adc0

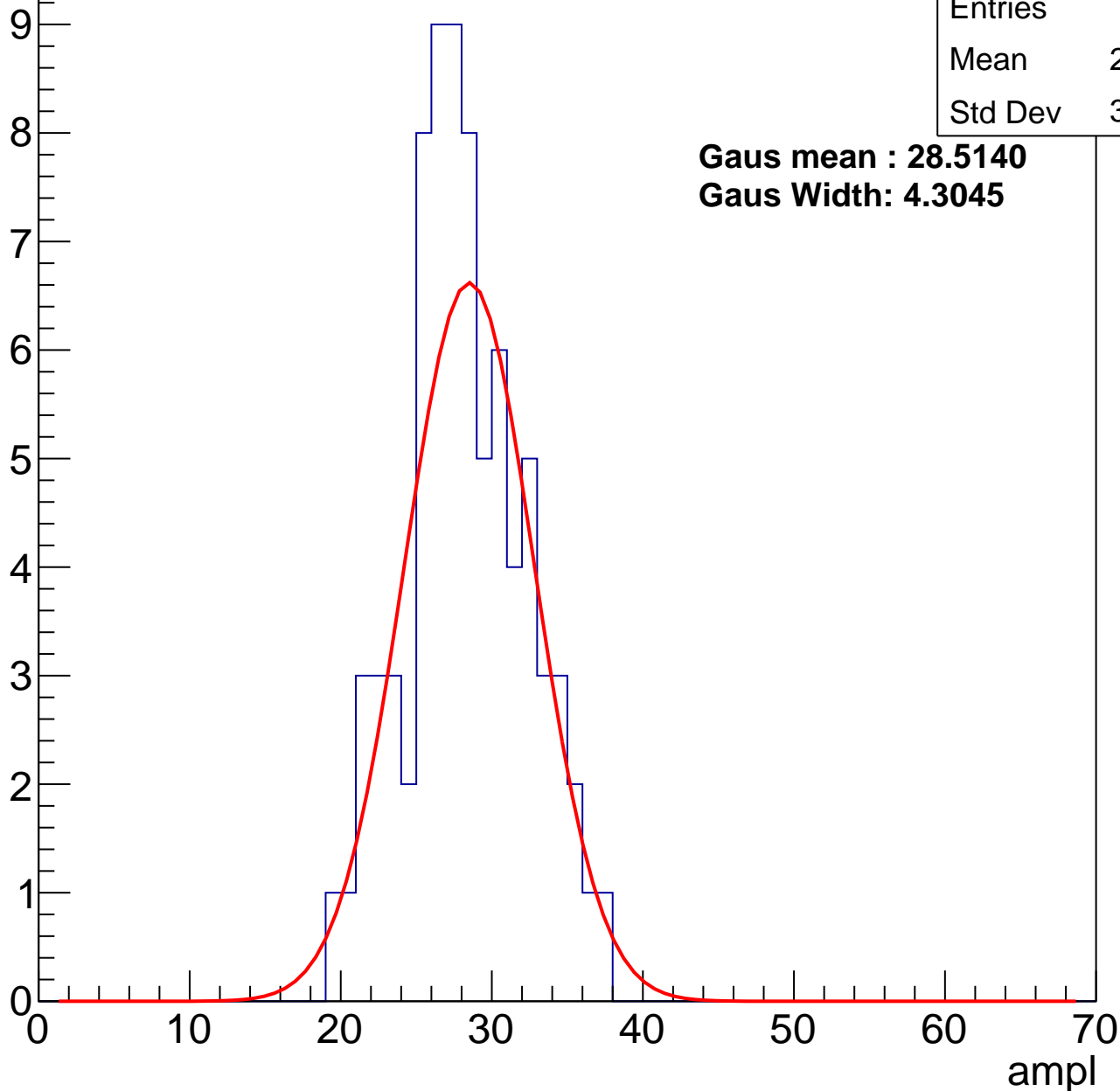
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	27.78
Std Dev	3.933

**Gaus mean : 28.5140**

**Gaus Width: 4.3045**



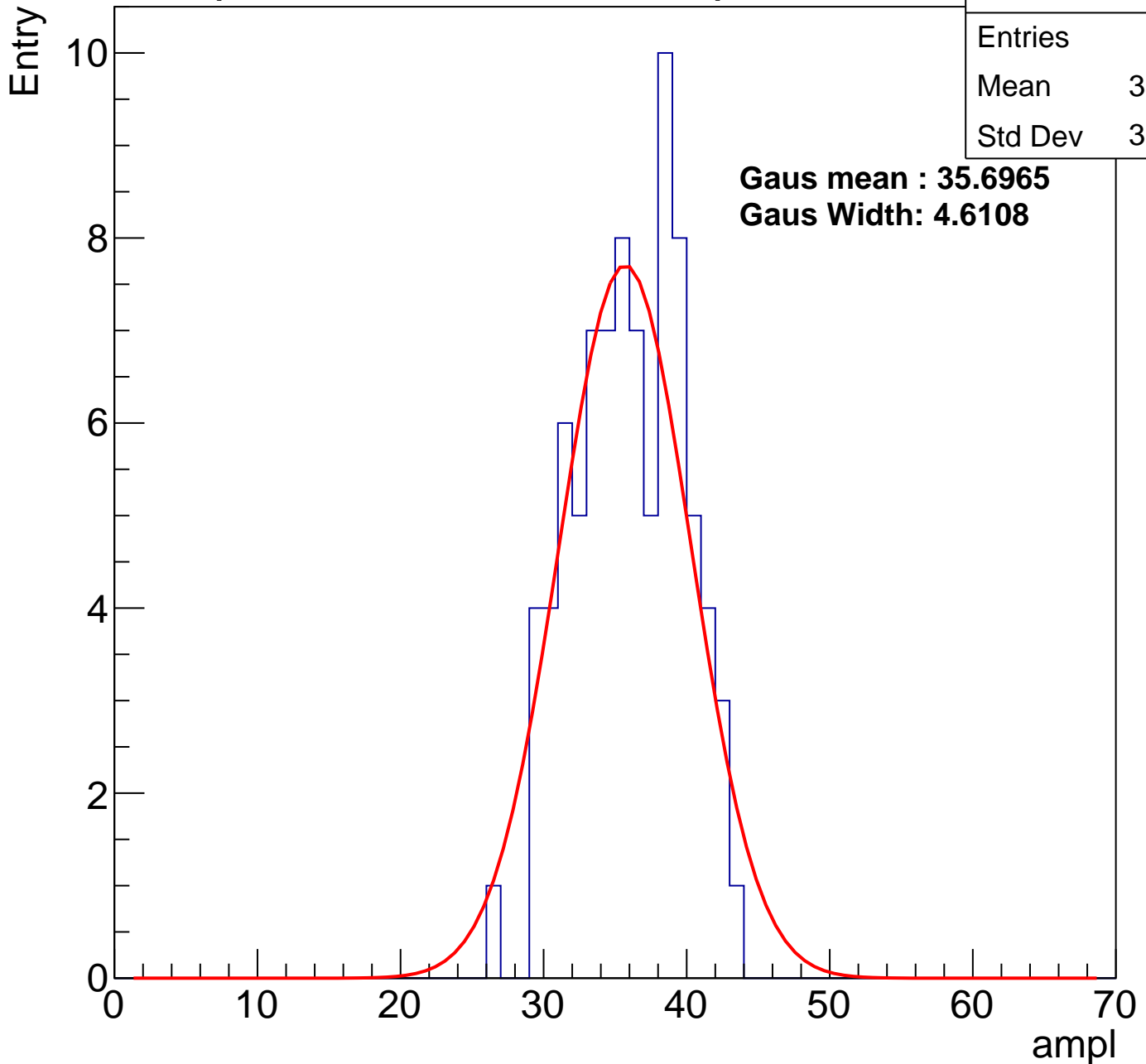
# B1L103S, U26-ch20, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	85
Mean	35.52
Std Dev	3.762

**Gaus mean : 35.6965**

**Gaus Width: 4.6108**



# B1L103S, U26-ch20, adc2

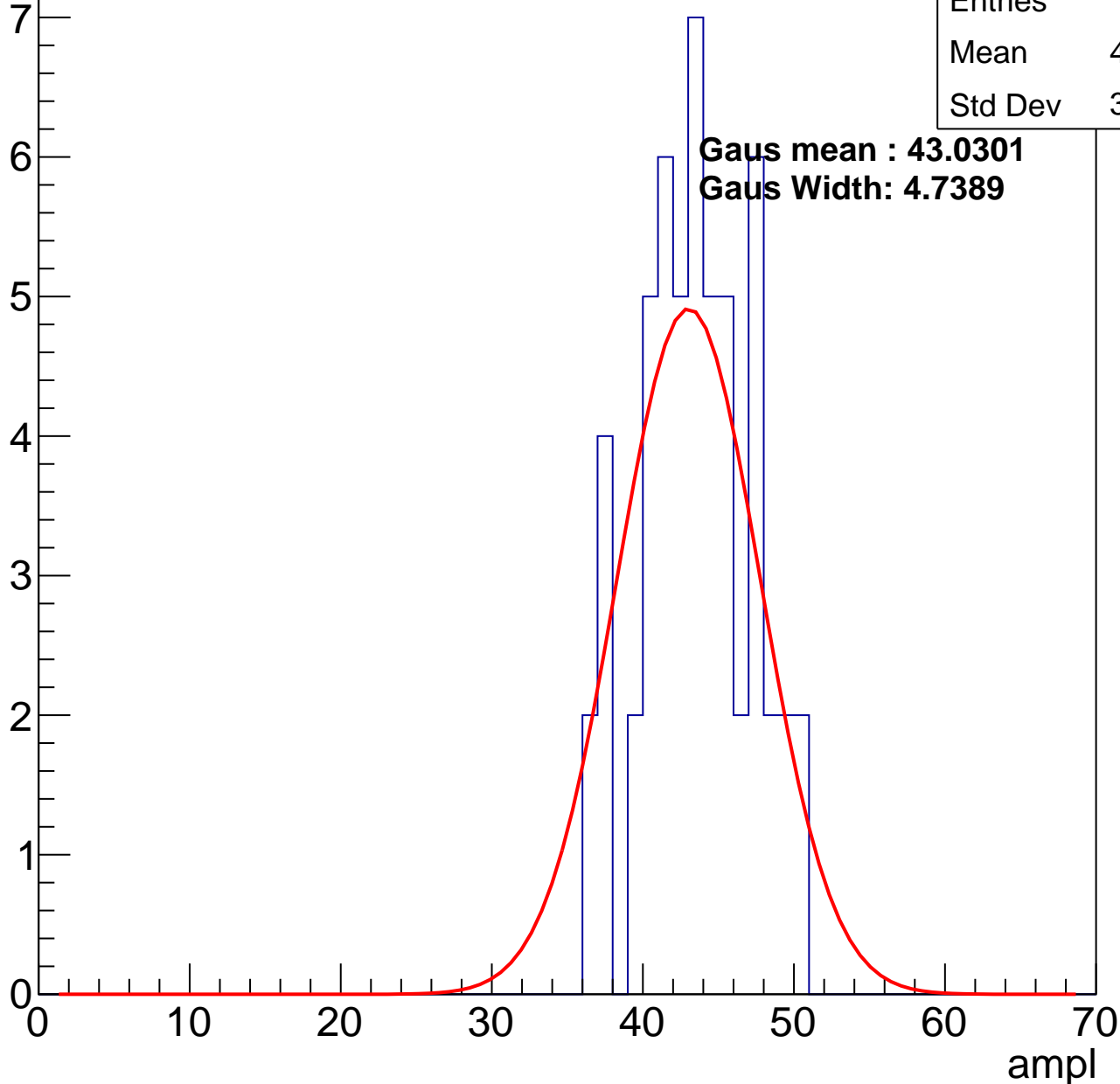
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	43.05
Std Dev	3.585

**Gaus mean : 43.0301**

**Gaus Width: 4.7389**

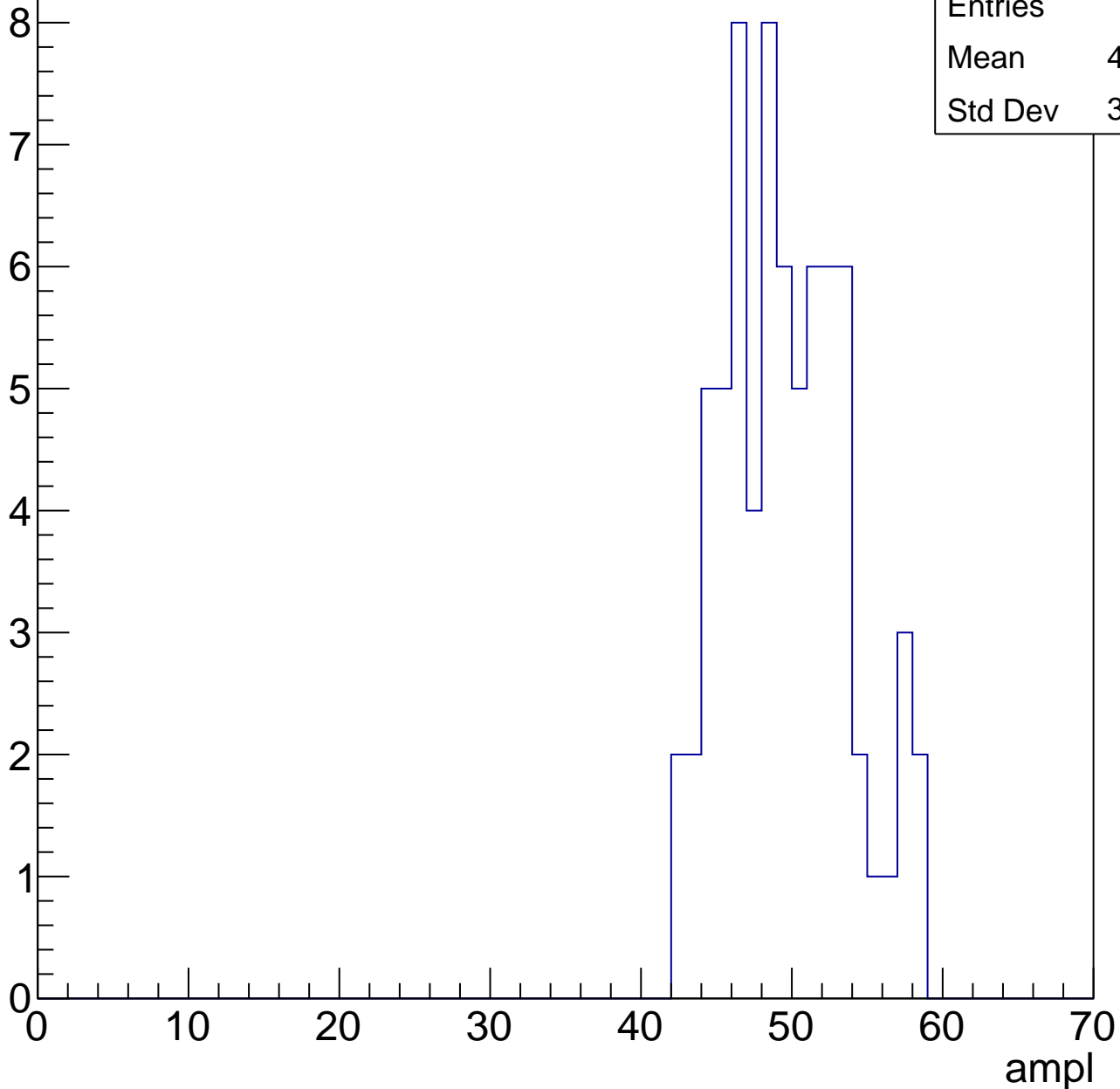


# B1L103S, U26-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

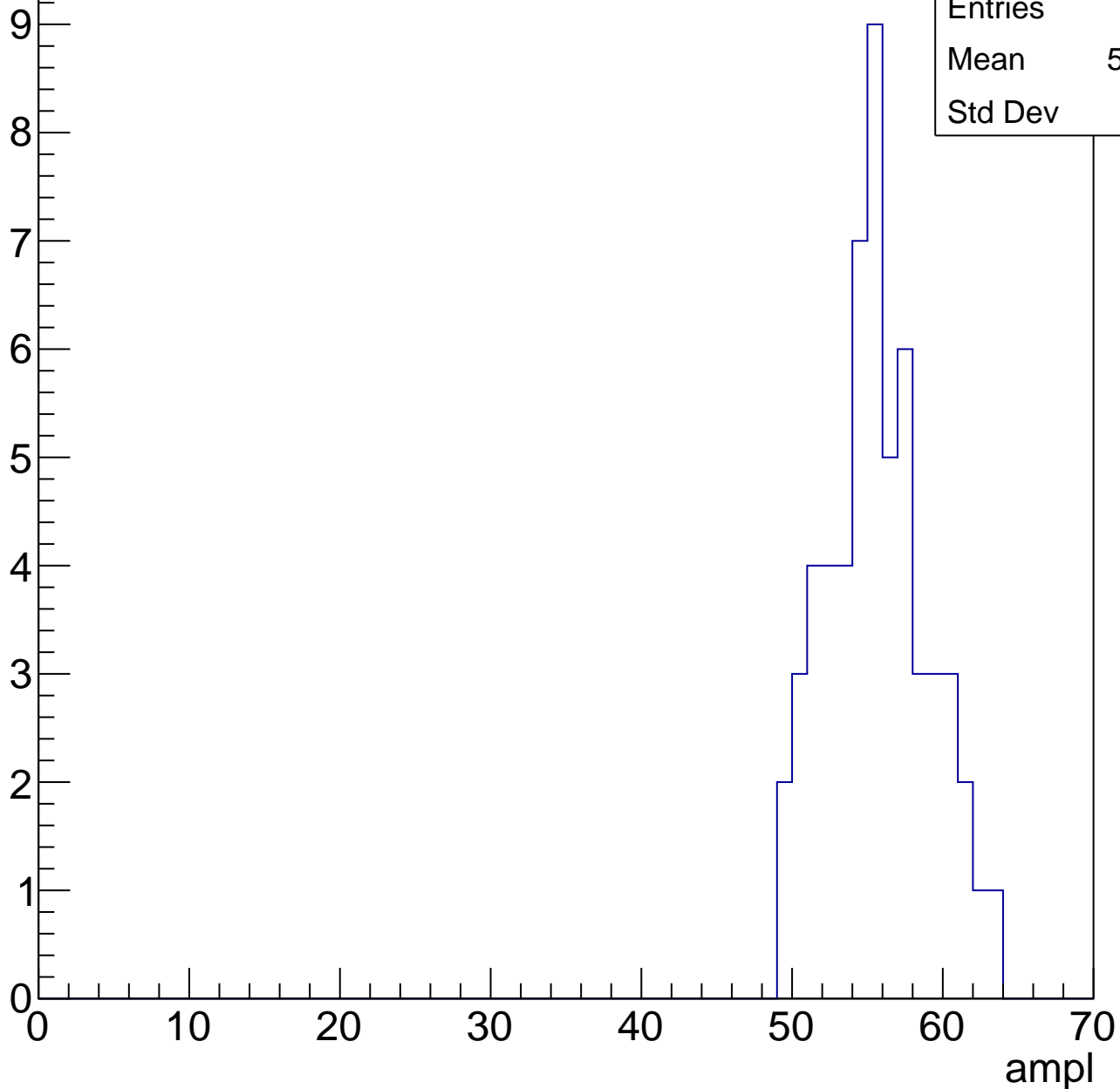
Entries	72
Mean	49.18
Std Dev	3.973



# B1L103S, U26-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

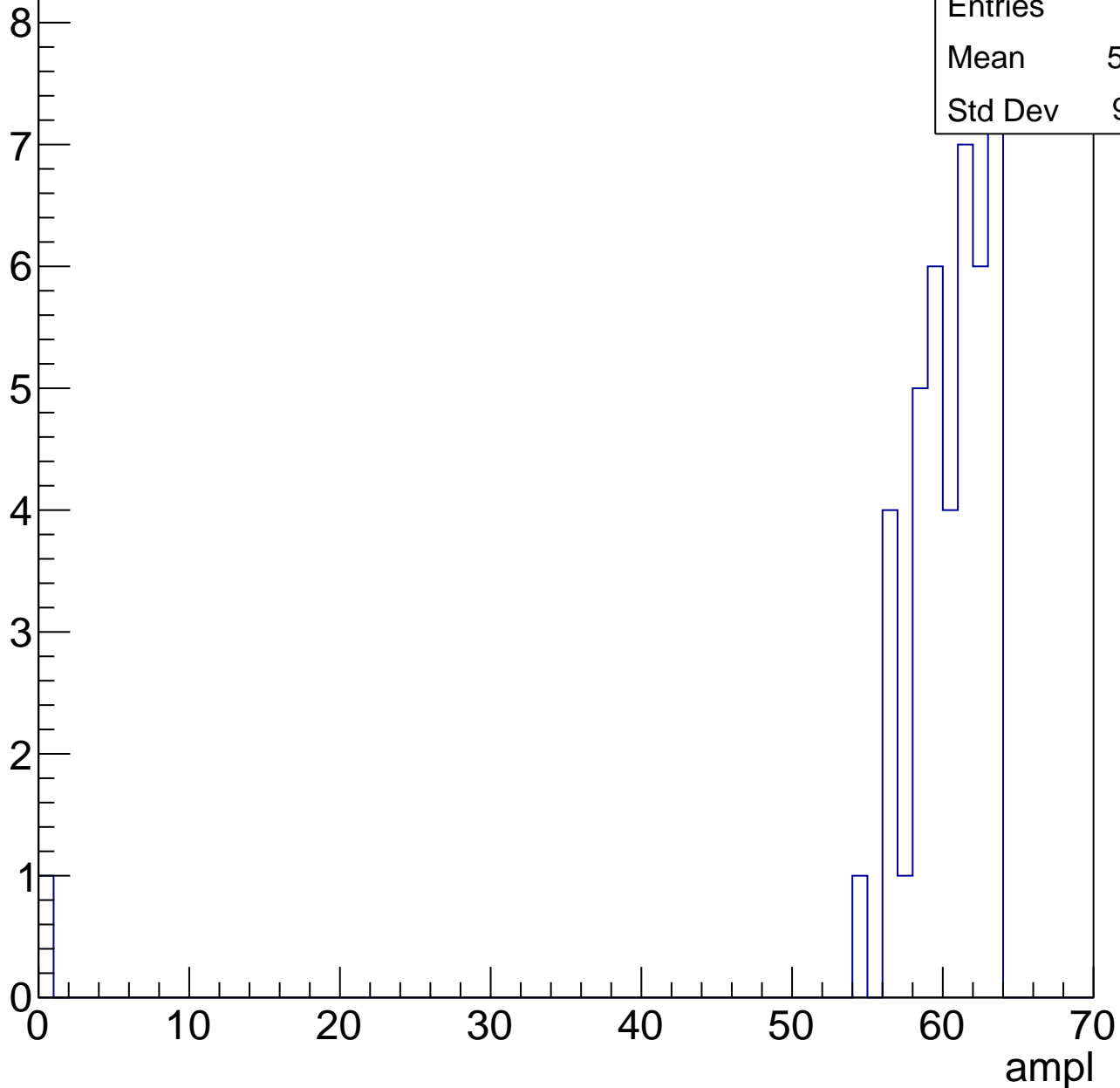


# B1L103S, U26-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

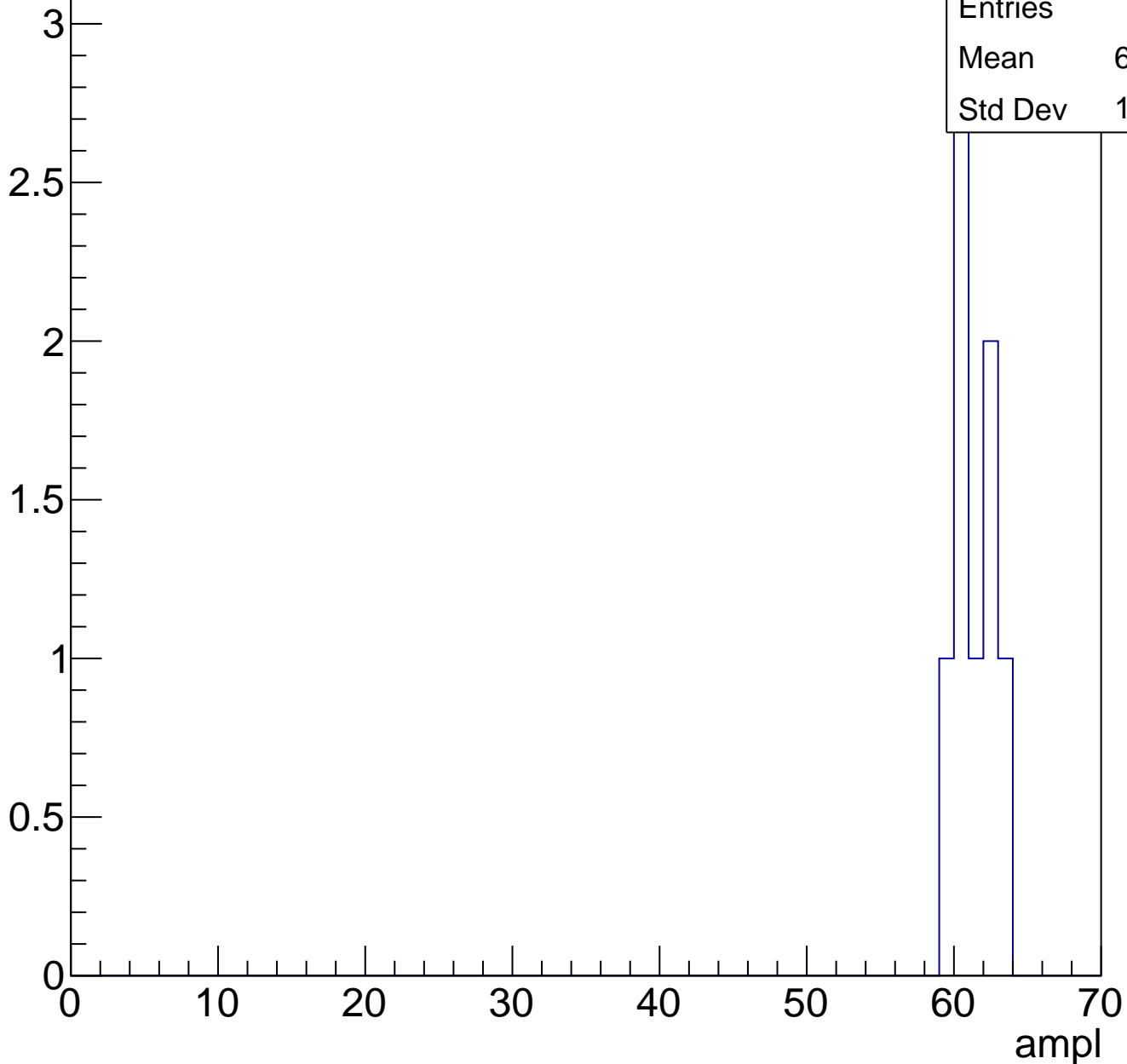
Entries	43
Mean	58.65
Std Dev	9.351



# B1L103S, U26-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch21, adc0

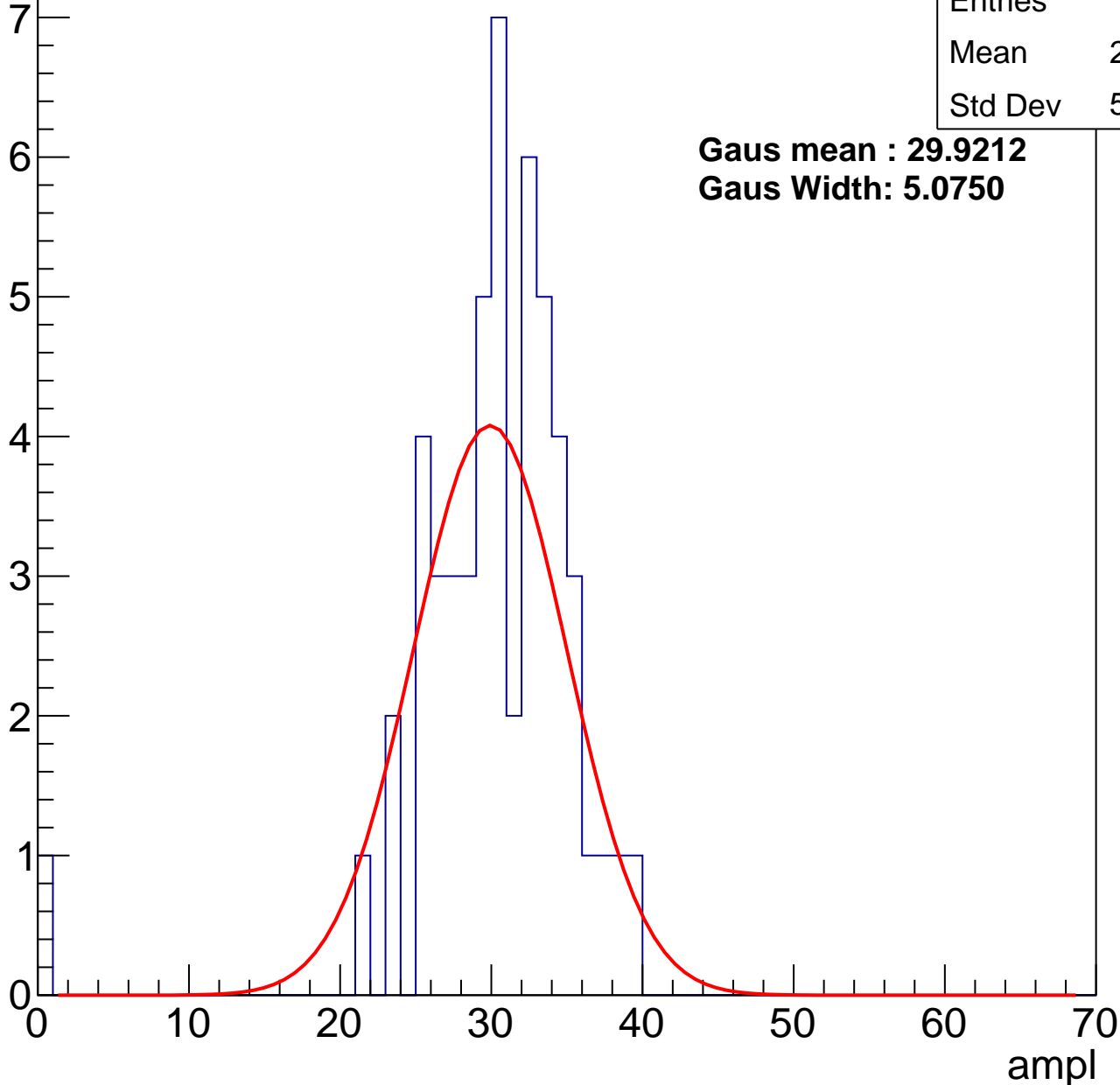
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	29.72
Std Dev	5.675

**Gaus mean : 29.9212**

**Gaus Width: 5.0750**



# B1L103S, U26-ch21, adc1

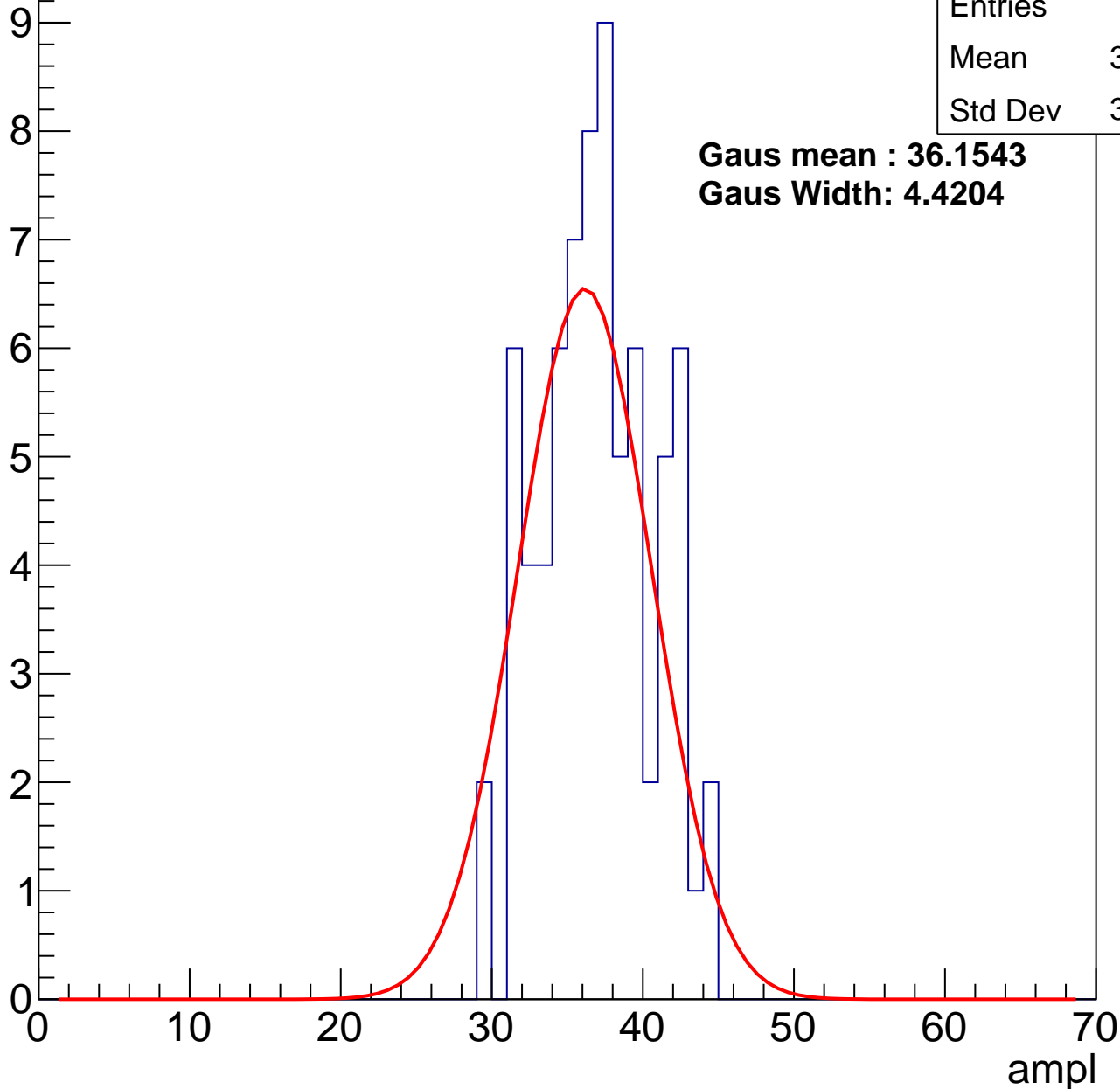
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	36.52
Std Dev	3.687

**Gaus mean : 36.1543**

**Gaus Width: 4.4204**



# B1L103S, U26-ch21, adc2

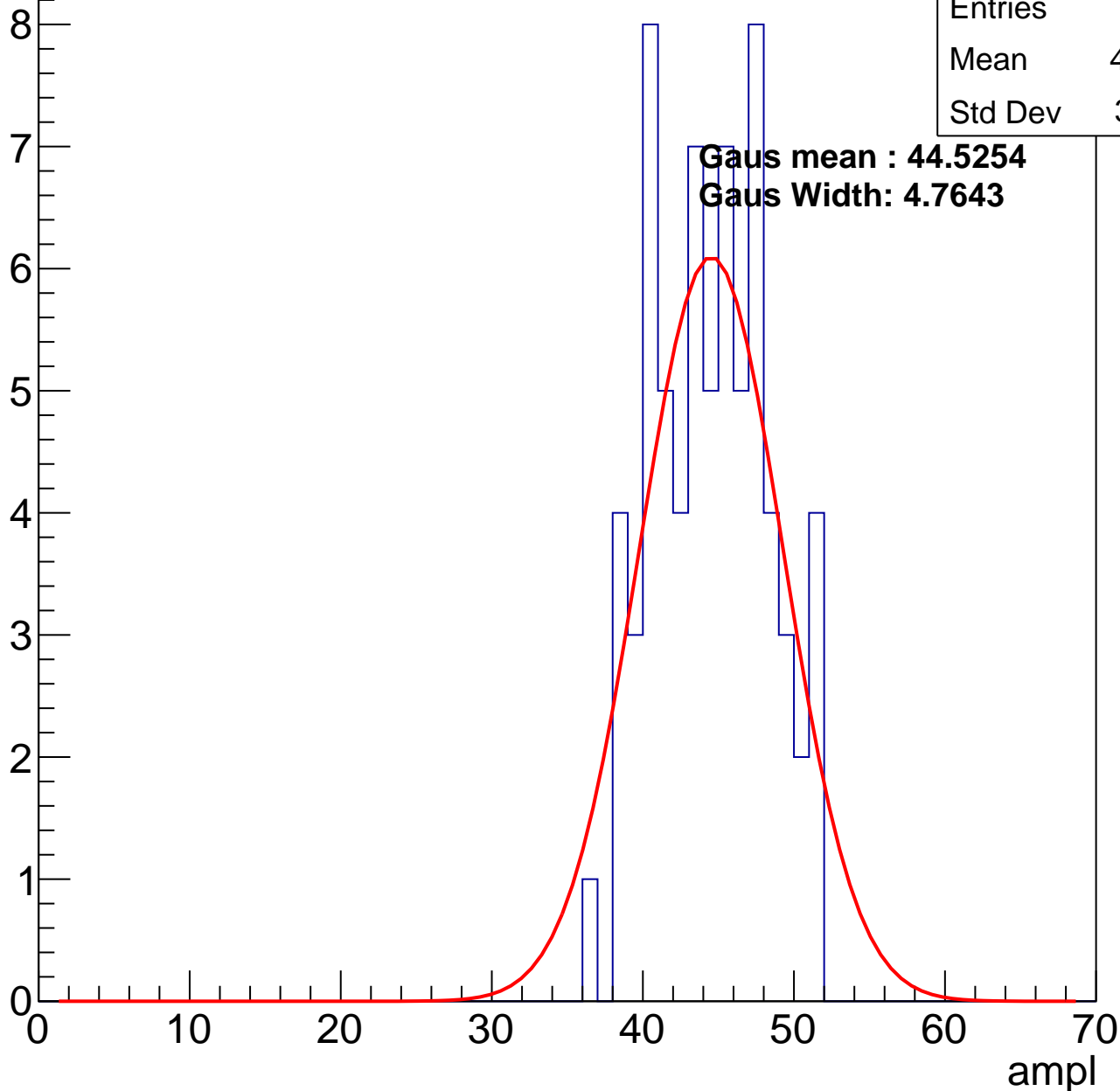
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	44.04
Std Dev	3.751

**Gaus mean : 44.5254**

**Gaus Width: 4.7643**



# B1L103S, U26-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	76
Mean	50.74
Std Dev	3.788

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

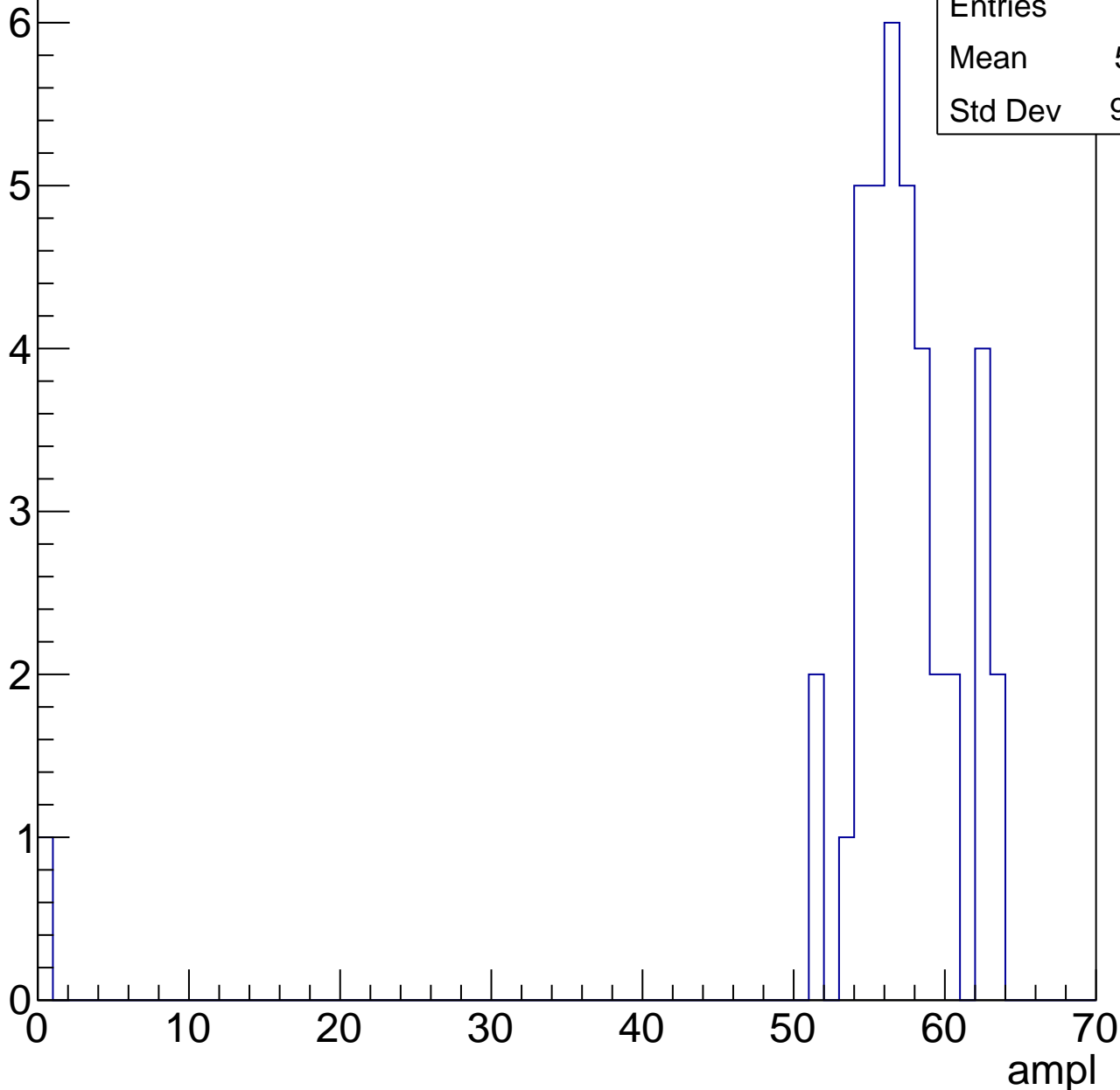
70

# B1L103S, U26-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	39
Mean	55.51
Std Dev	9.505

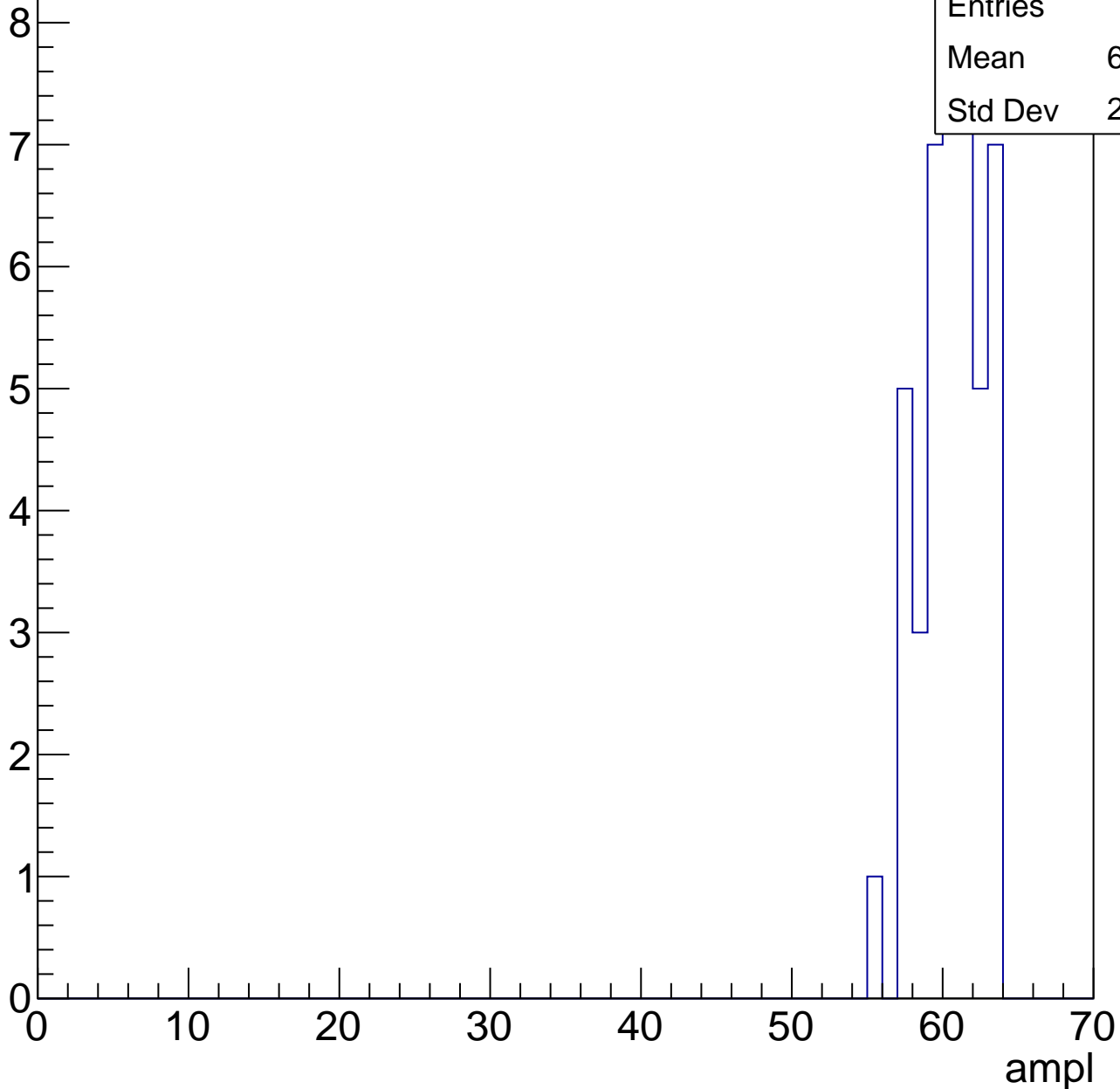


# B1L103S, U26-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	60.14
Std Dev	2.018



# B1L103S, U26-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

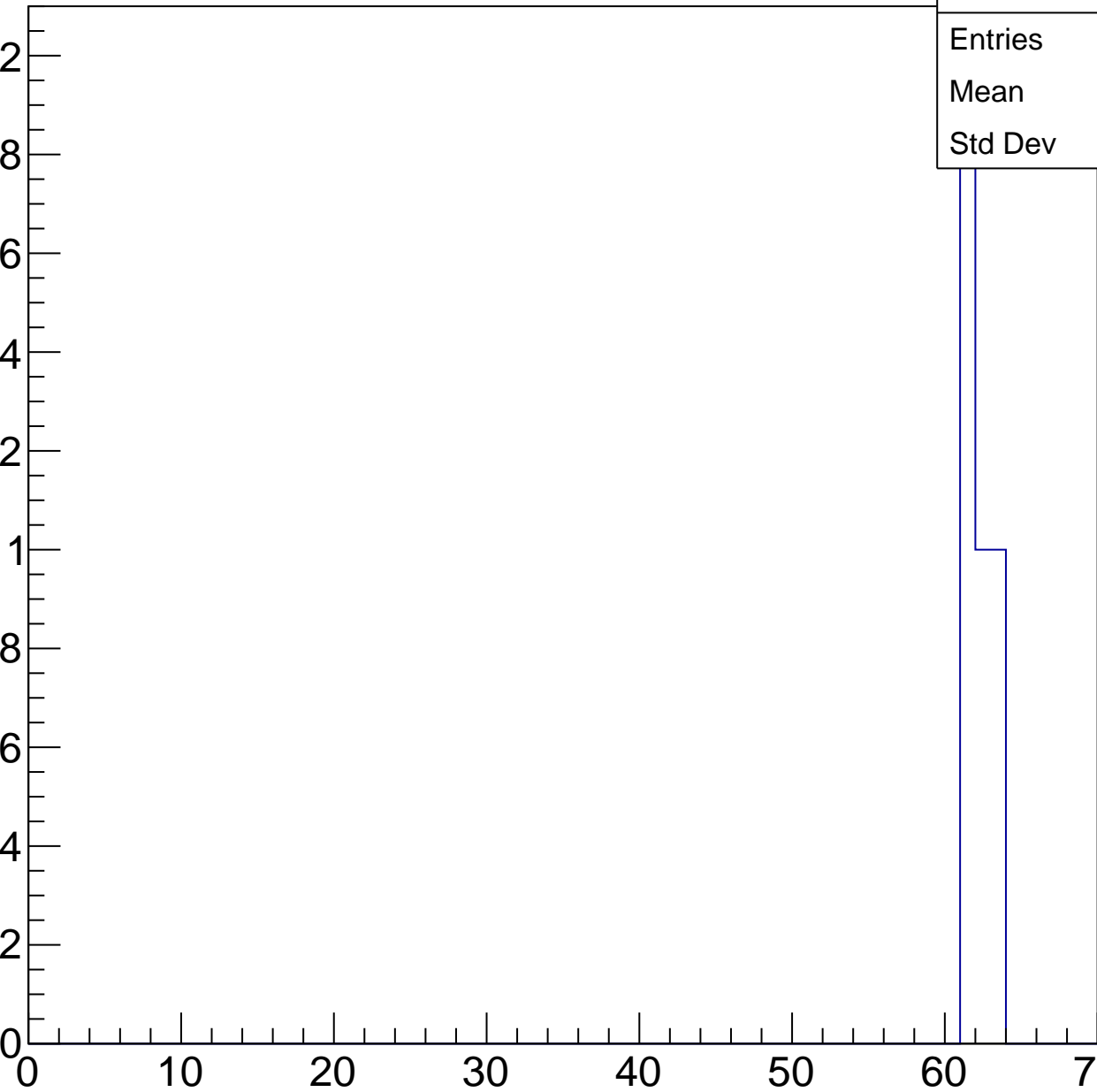
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	61.75
Std Dev	0.8292

0 10 20 30 40 50 60 70

ampl





# B1L103S, U26-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L103S, U26-ch22, adc0

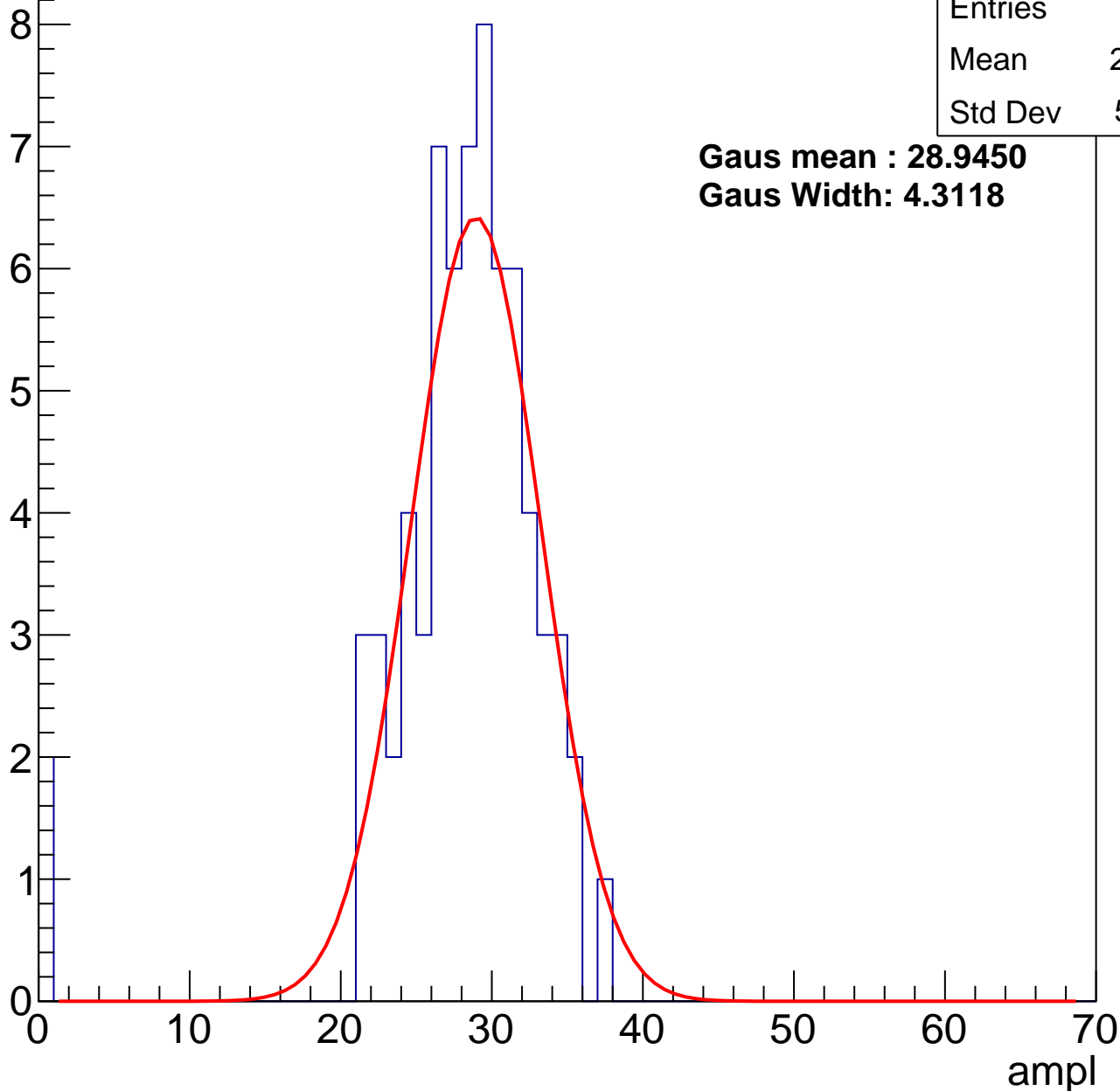
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	27.43
Std Dev	5.961

**Gaus mean : 28.9450**

**Gaus Width: 4.3118**



# B1L103S, U26-ch22, adc1

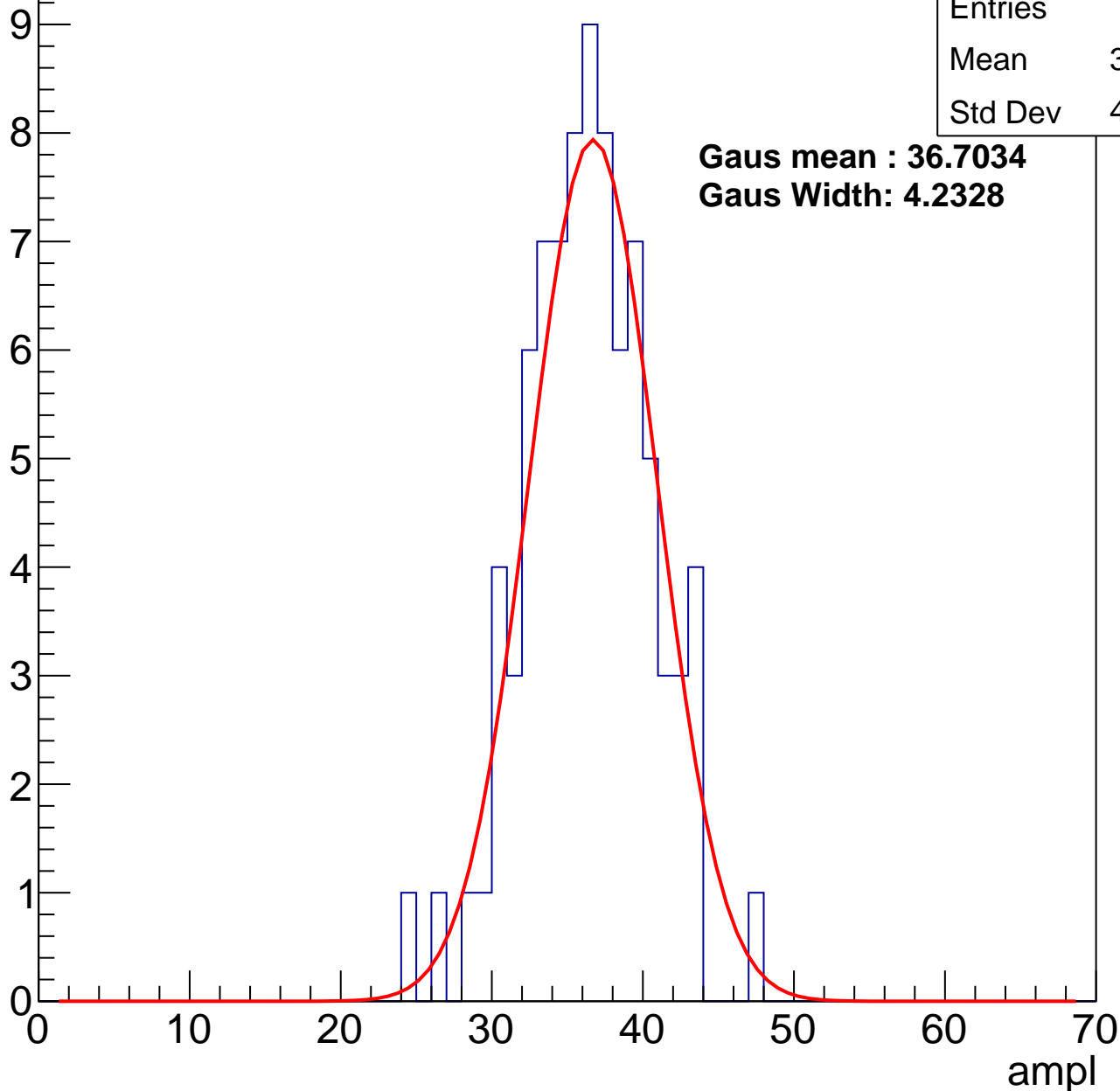
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	85
Mean	35.88
Std Dev	4.123

**Gaus mean : 36.7034**

**Gaus Width: 4.2328**



# B1L103S, U26-ch22, adc2

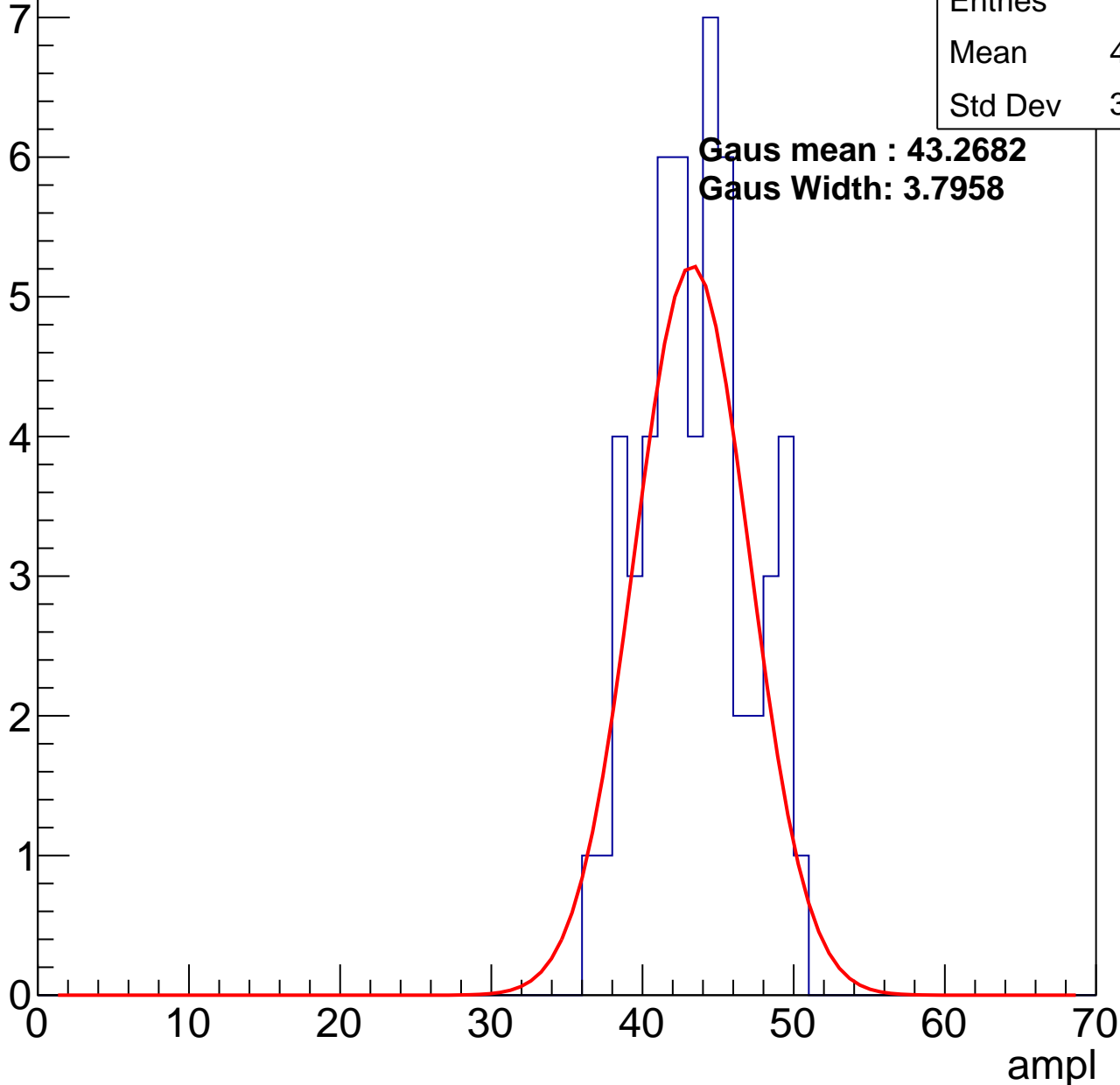
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	43.07
Std Dev	3.463

**Gaus mean : 43.2682**

**Gaus Width: 3.7958**

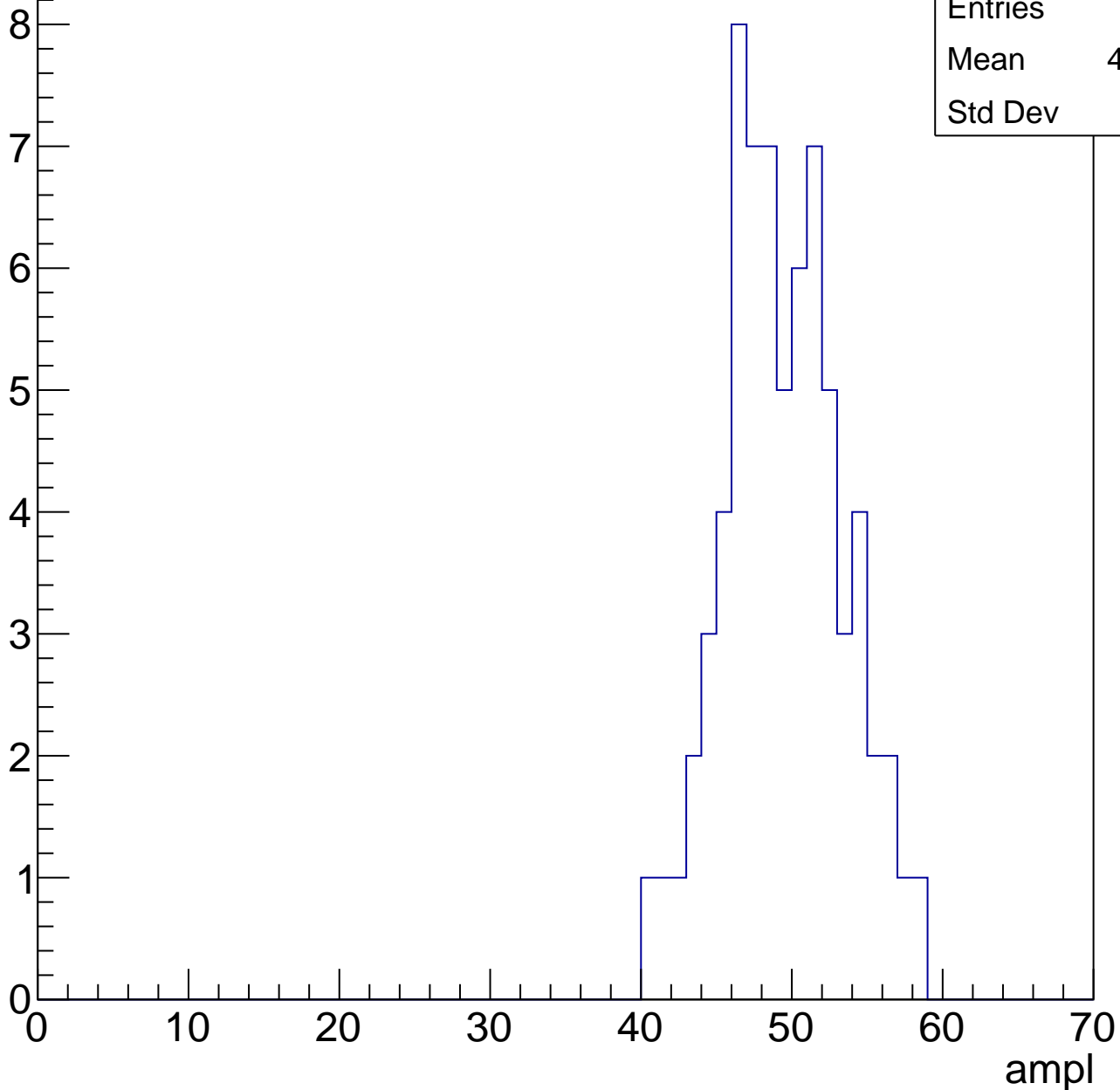


# B1L103S, U26-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	48.97
Std Dev	3.88

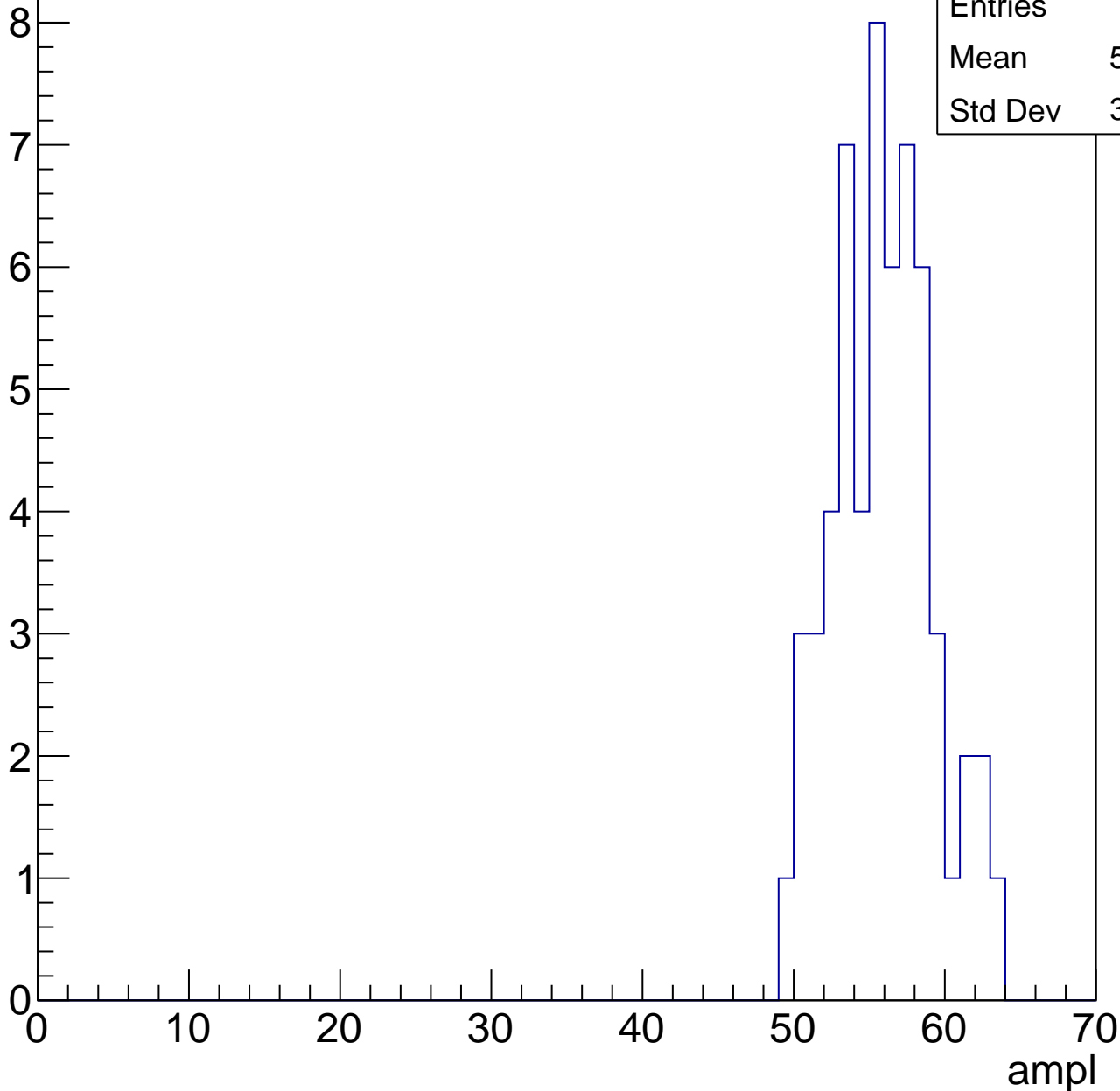


# B1L103S, U26-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	55.45
Std Dev	3.244

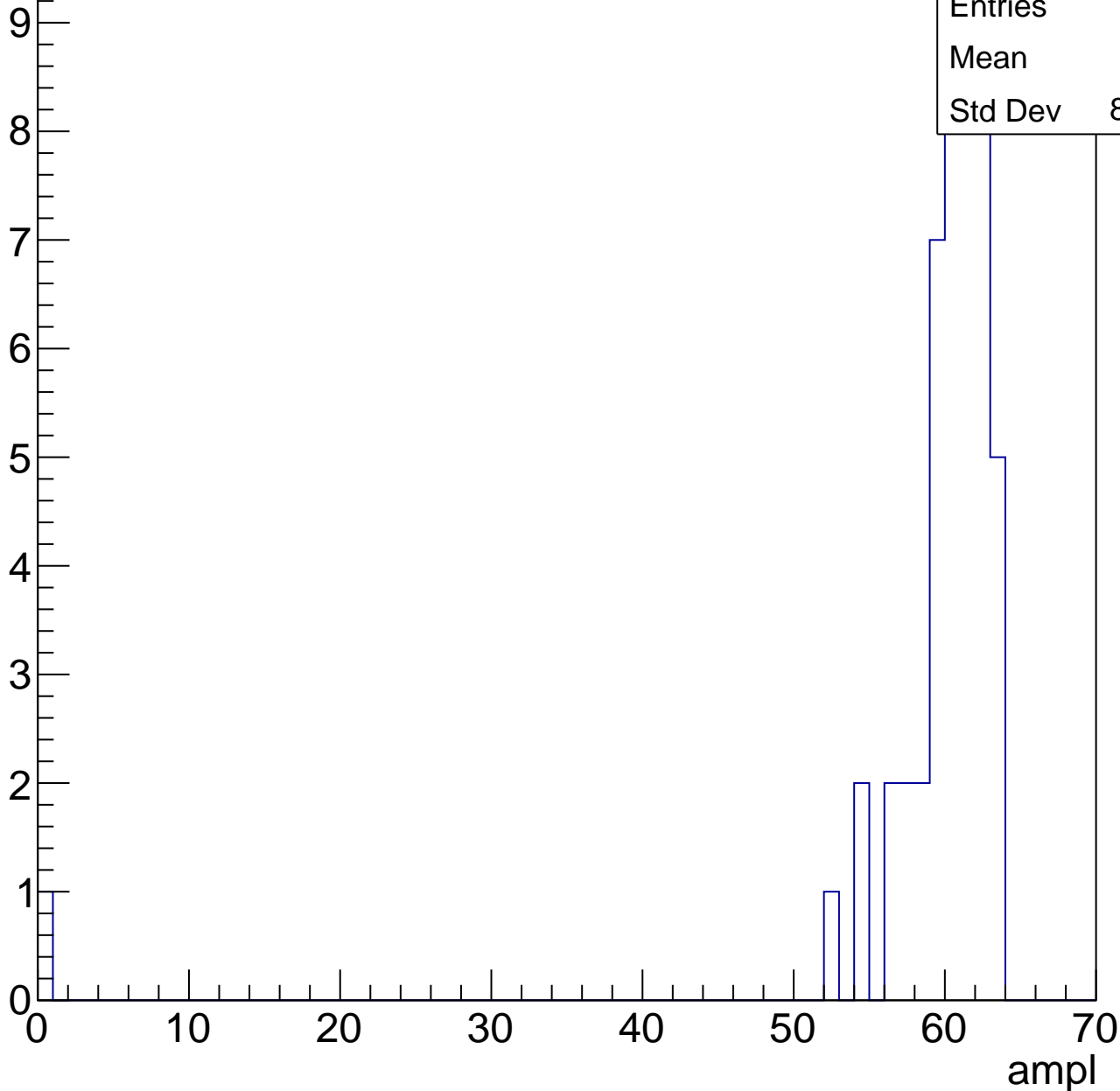


# B1L103S, U26-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

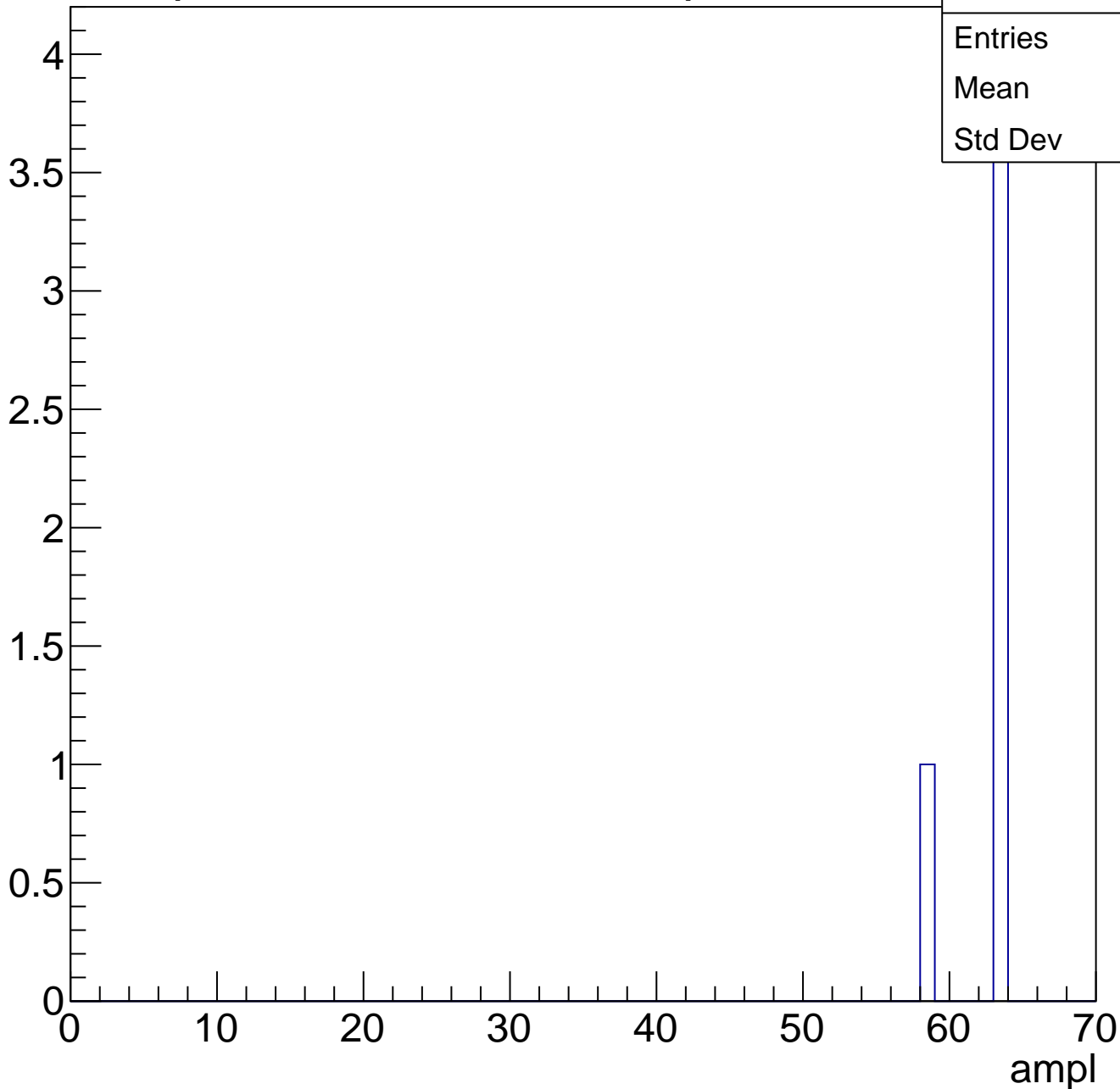
Entries	47
Mean	58.6
Std Dev	8.984



# B1L103S, U26-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U26-ch23, adc0

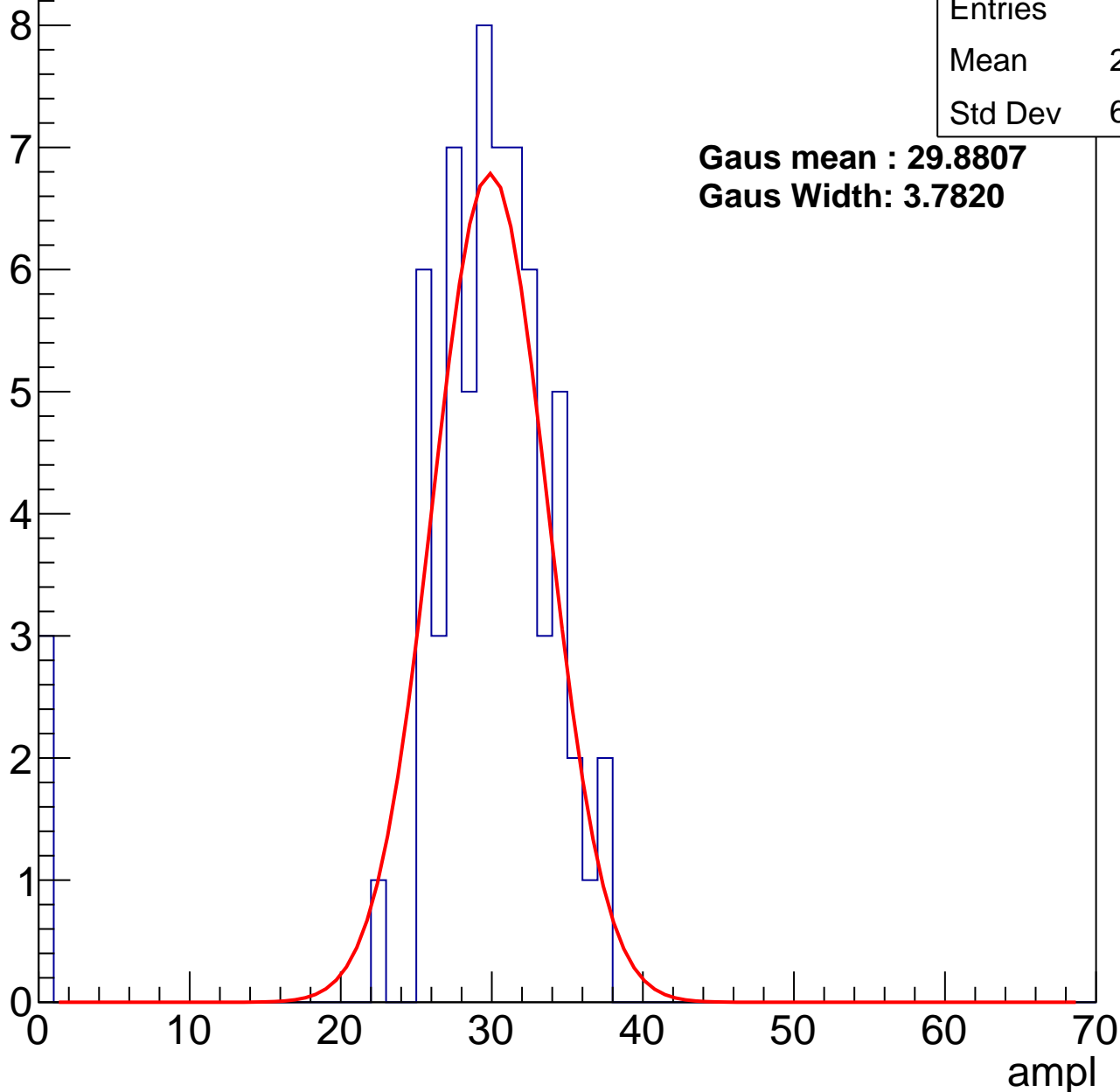
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	28.47
Std Dev	6.985

**Gaus mean : 29.8807**

**Gaus Width: 3.7820**



# B1L103S, U26-ch23, adc1

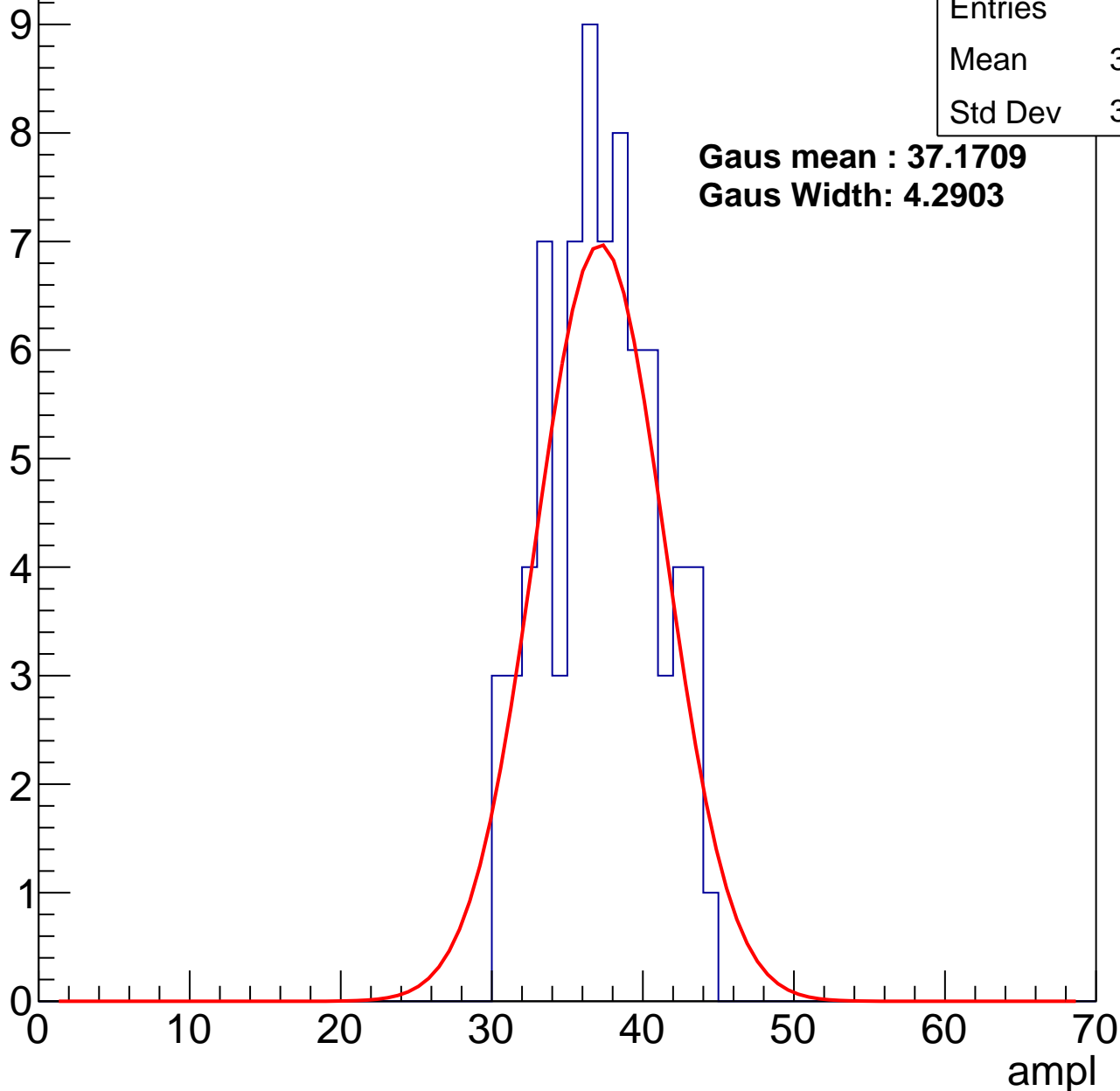
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	36.76
Std Dev	3.566

**Gaus mean : 37.1709**

**Gaus Width: 4.2903**



# B1L103S, U26-ch23, adc2

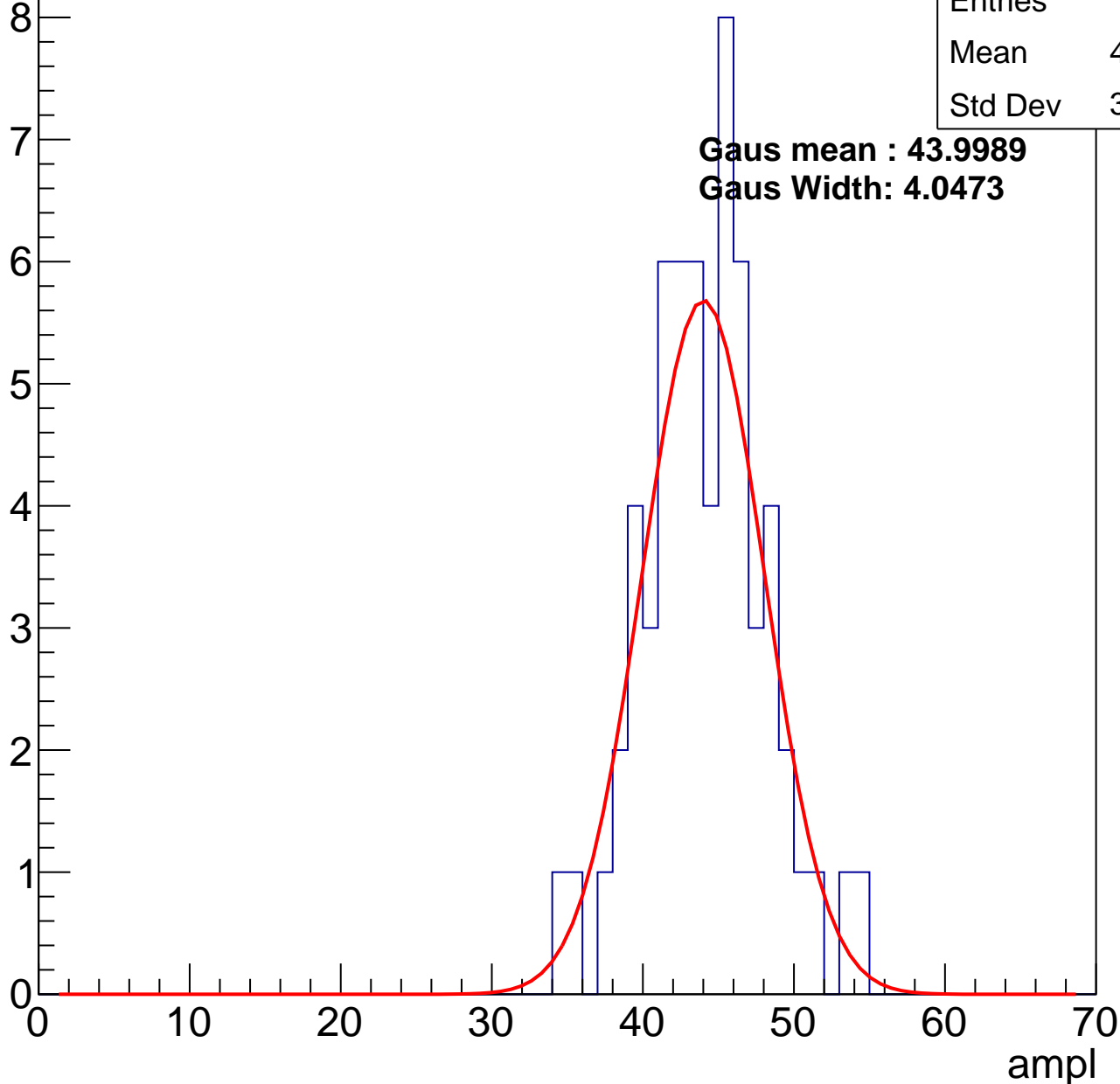
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	43.69
Std Dev	3.982

**Gaus mean : 43.9989**

**Gaus Width: 4.0473**

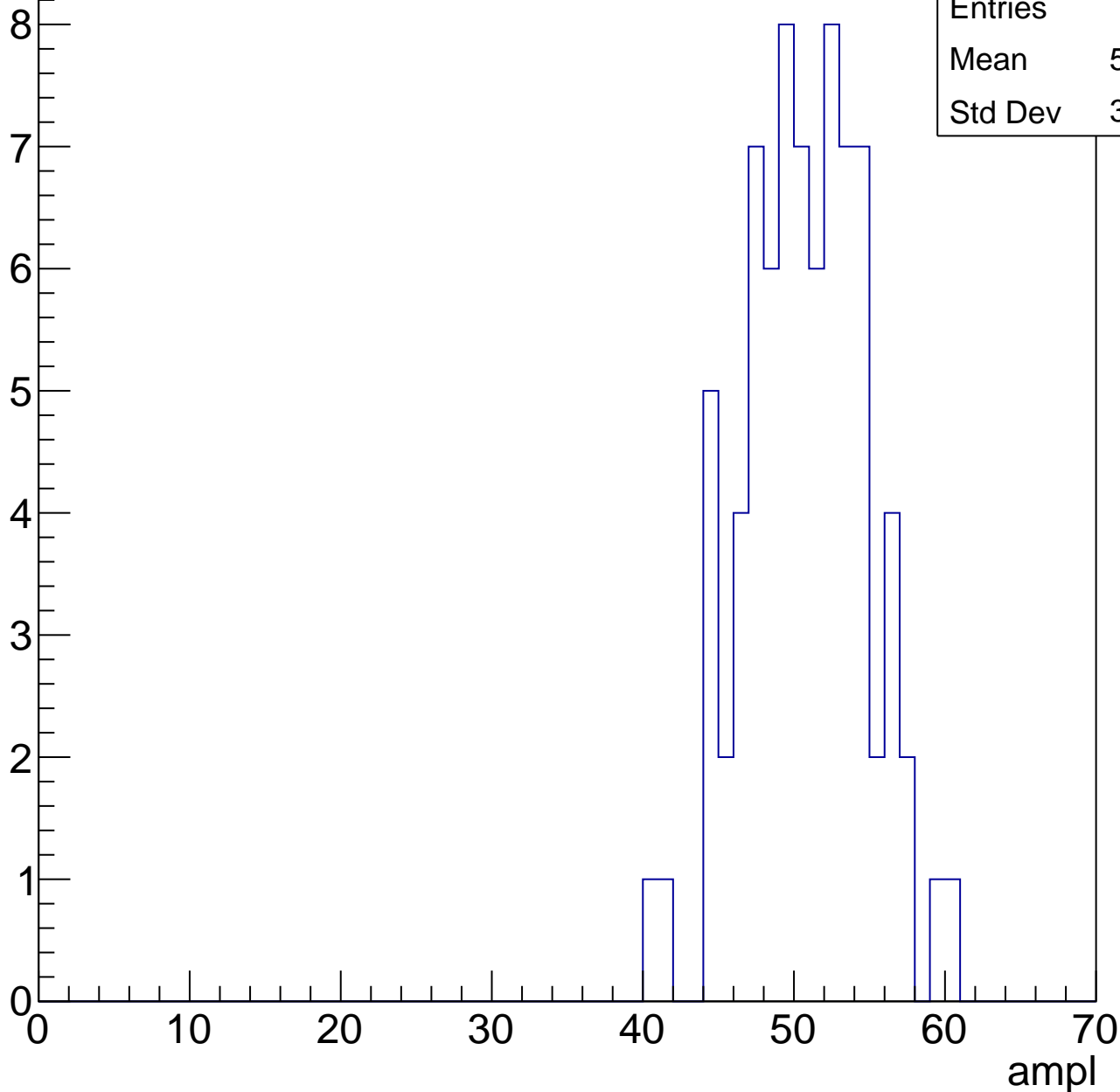


# B1L103S, U26-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	50.28
Std Dev	3.978

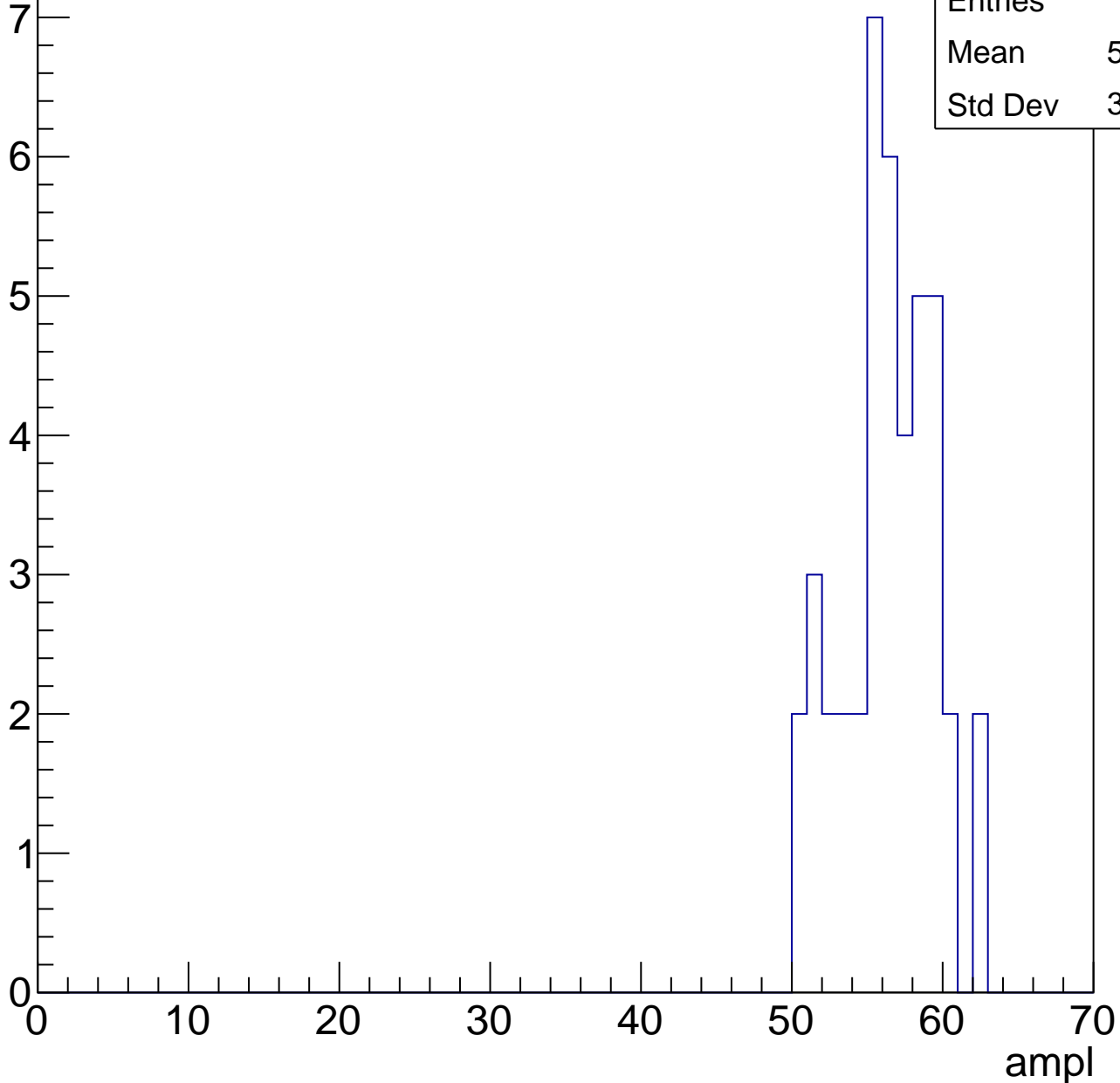


# B1L103S, U26-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	42
Mean	55.93
Std Dev	3.027

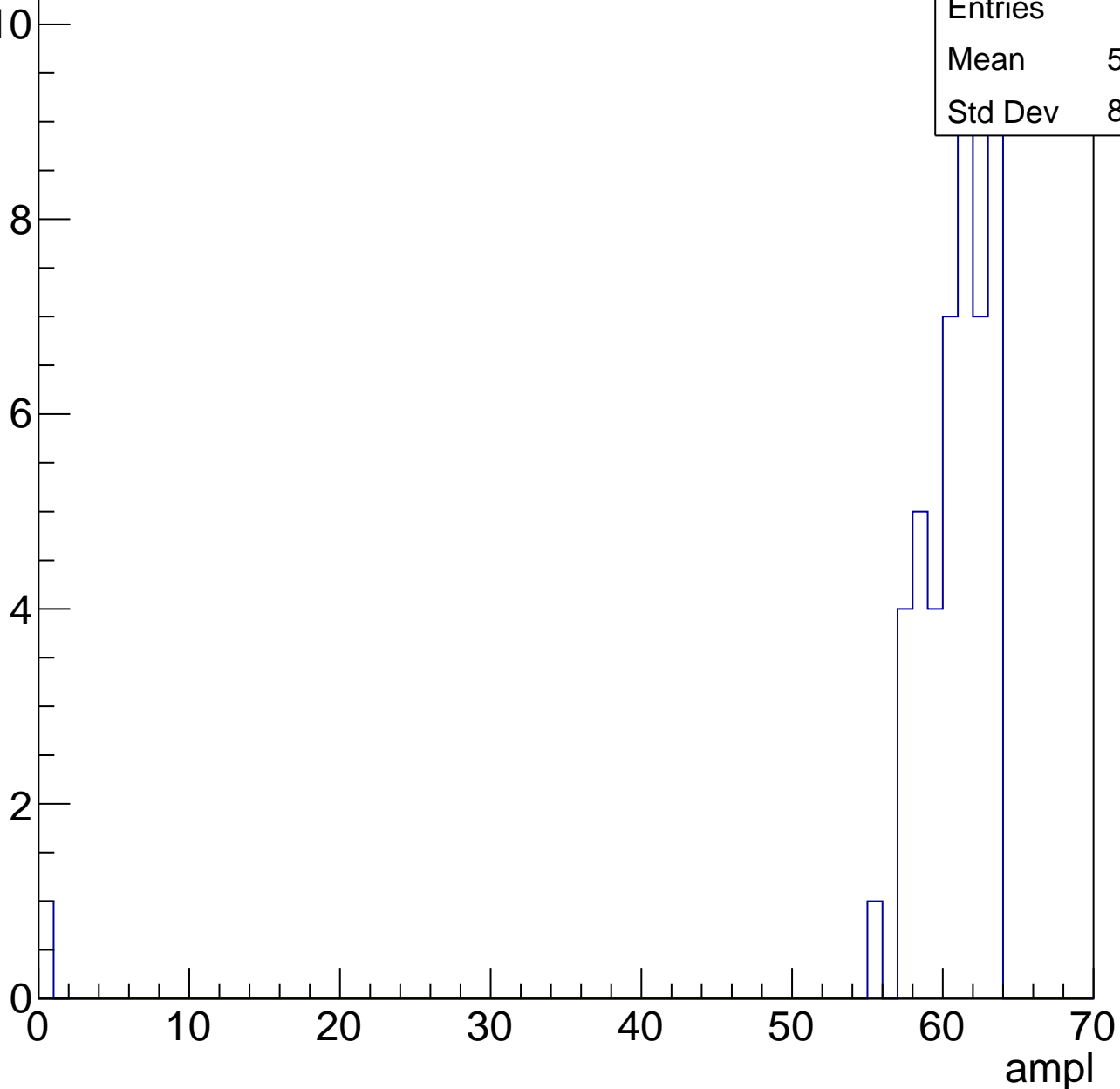


# B1L103S, U26-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	59.24
Std Dev	8.789



# B1L103S, U26-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

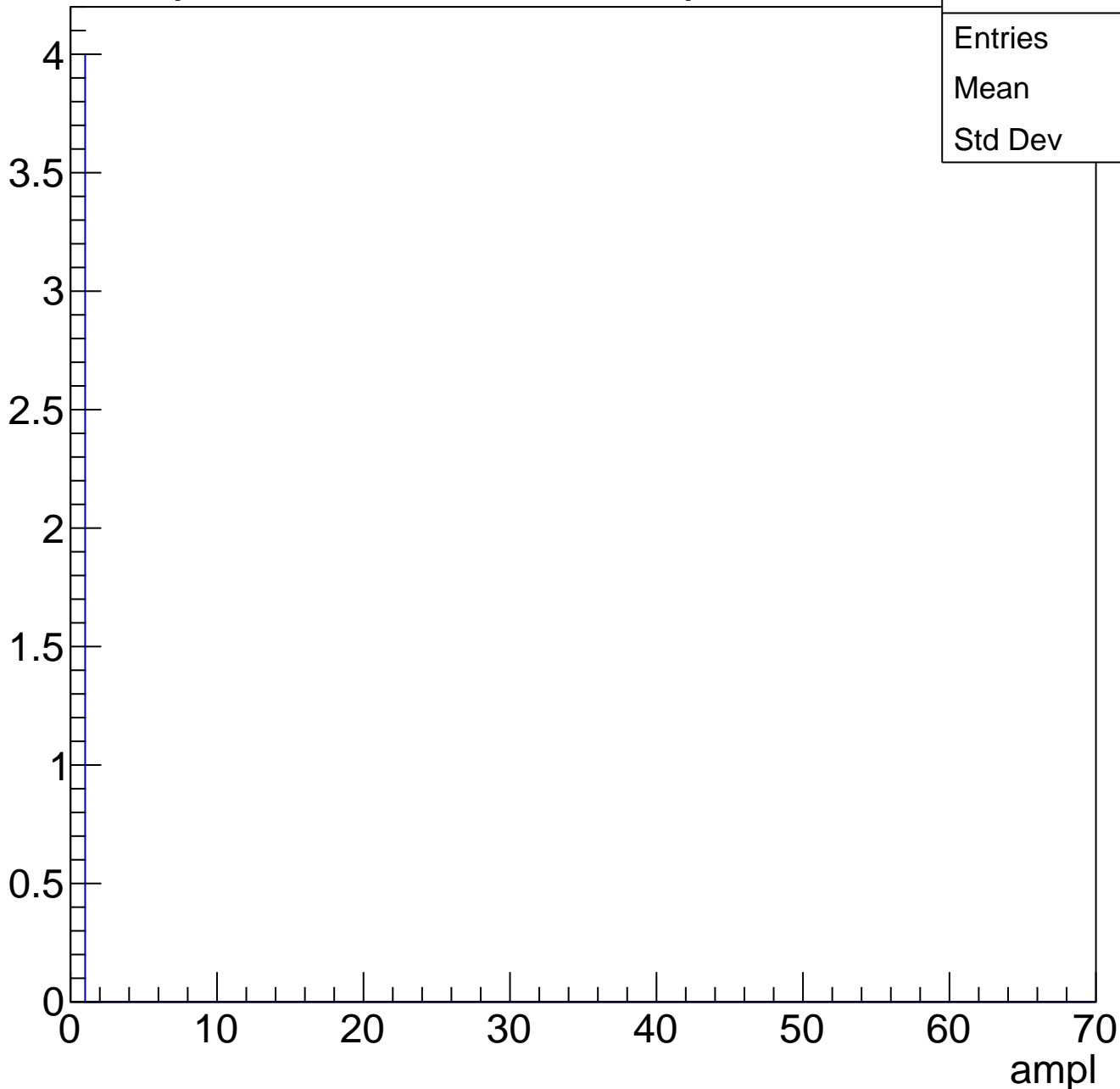




# B1L103S, U26-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	4
Mean	0
Std Dev	0

# B1L103S, U26-ch24, adc0

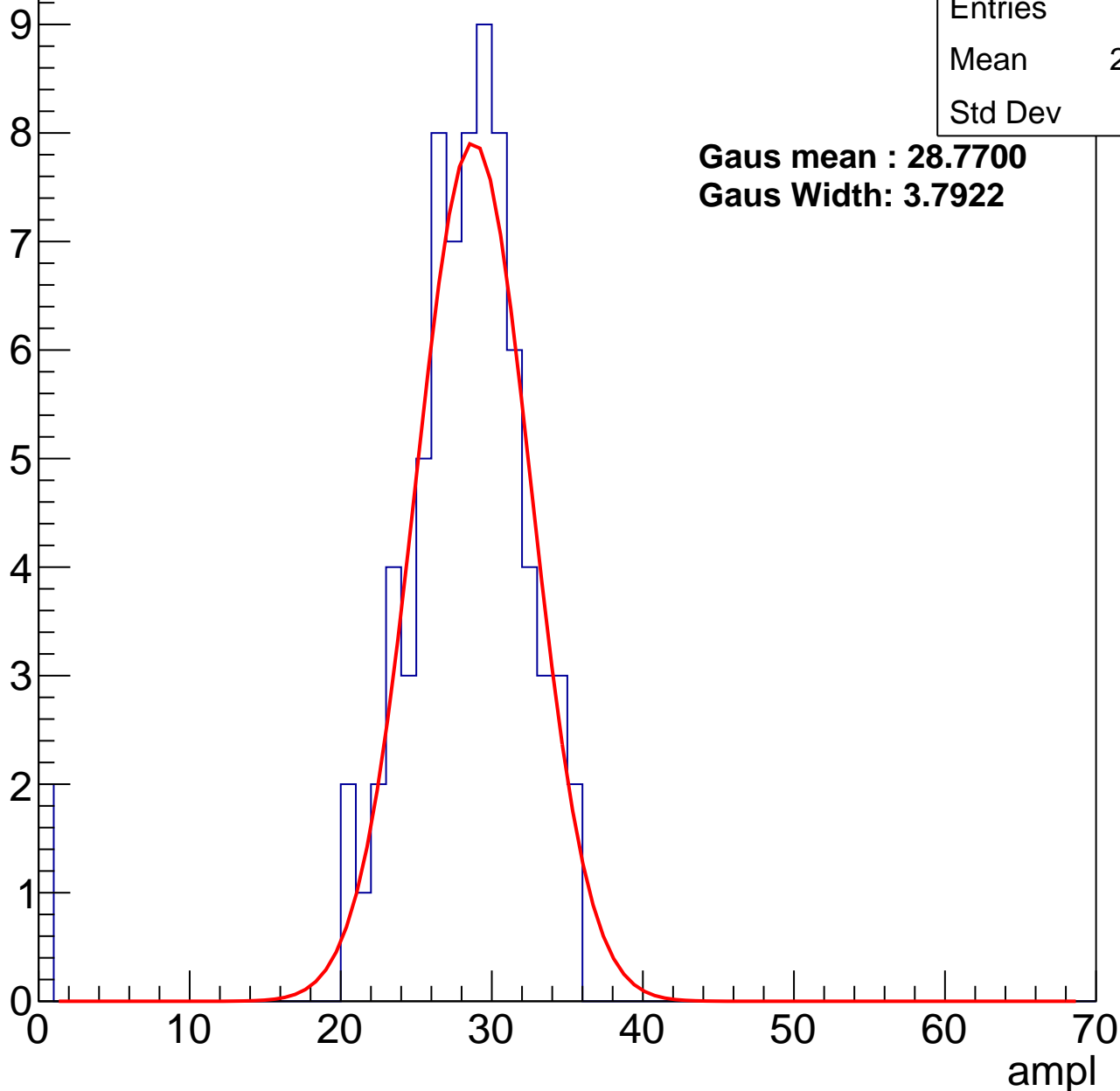
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	27.29
Std Dev	5.64

**Gaus mean : 28.7700**

**Gaus Width: 3.7922**



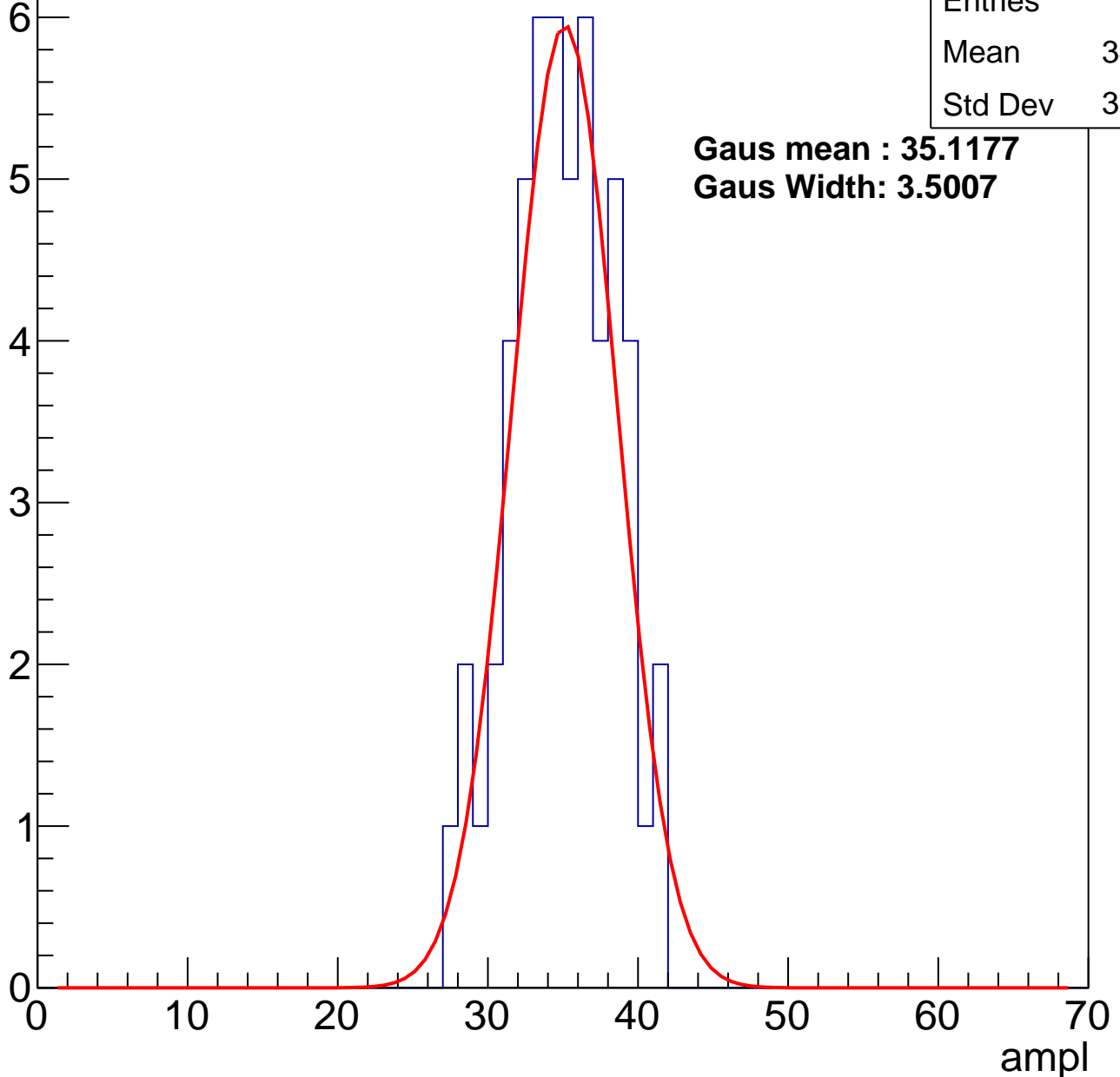
# B1L103S, U26-ch24, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	34.54
Std Dev	3.343

**Gaus mean : 35.1177**  
**Gaus Width: 3.5007**



# B1L103S, U26-ch24, adc2

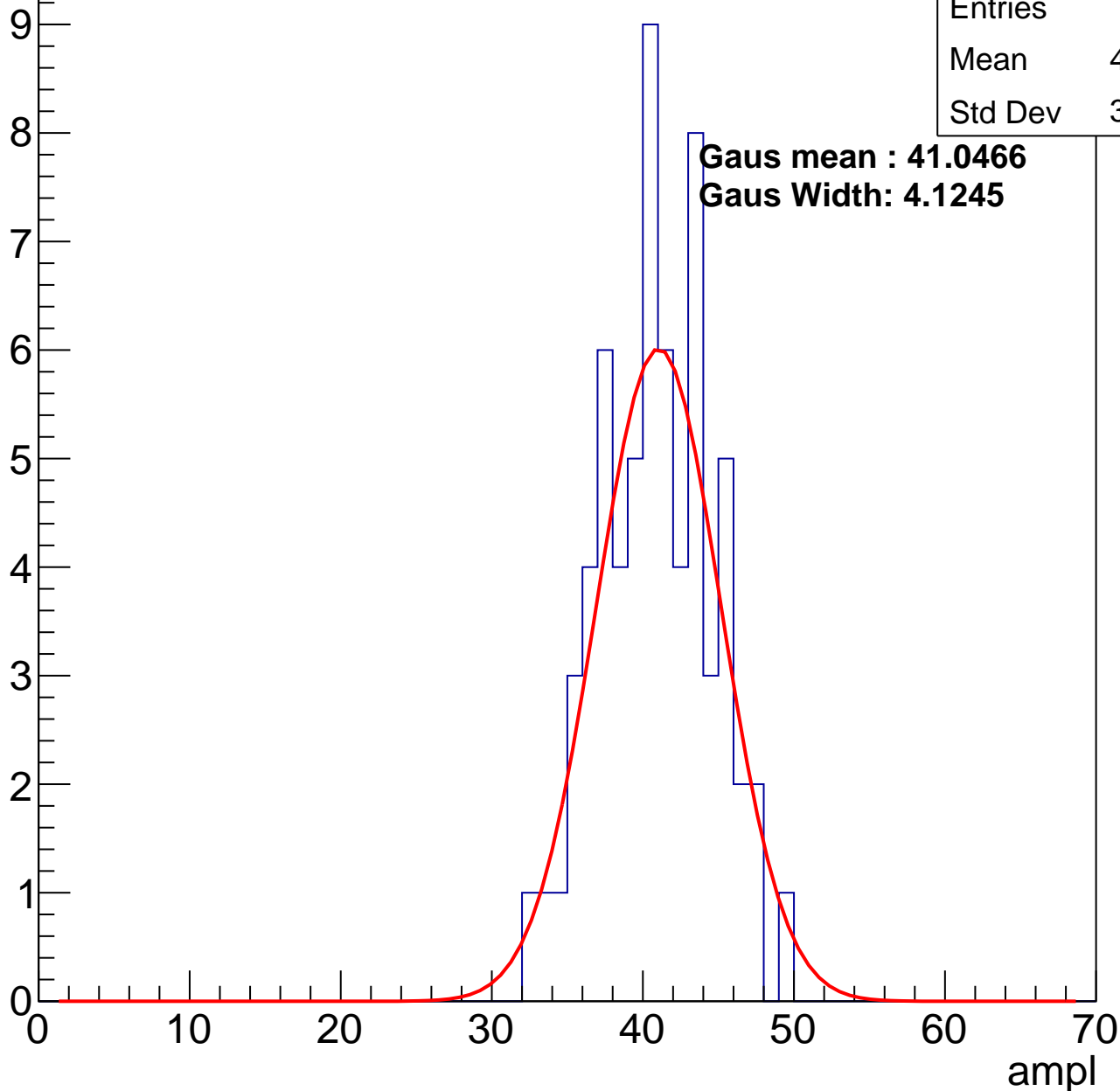
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	40.42
Std Dev	3.658

**Gaus mean : 41.0466**

**Gaus Width: 4.1245**



# B1L103S, U26-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

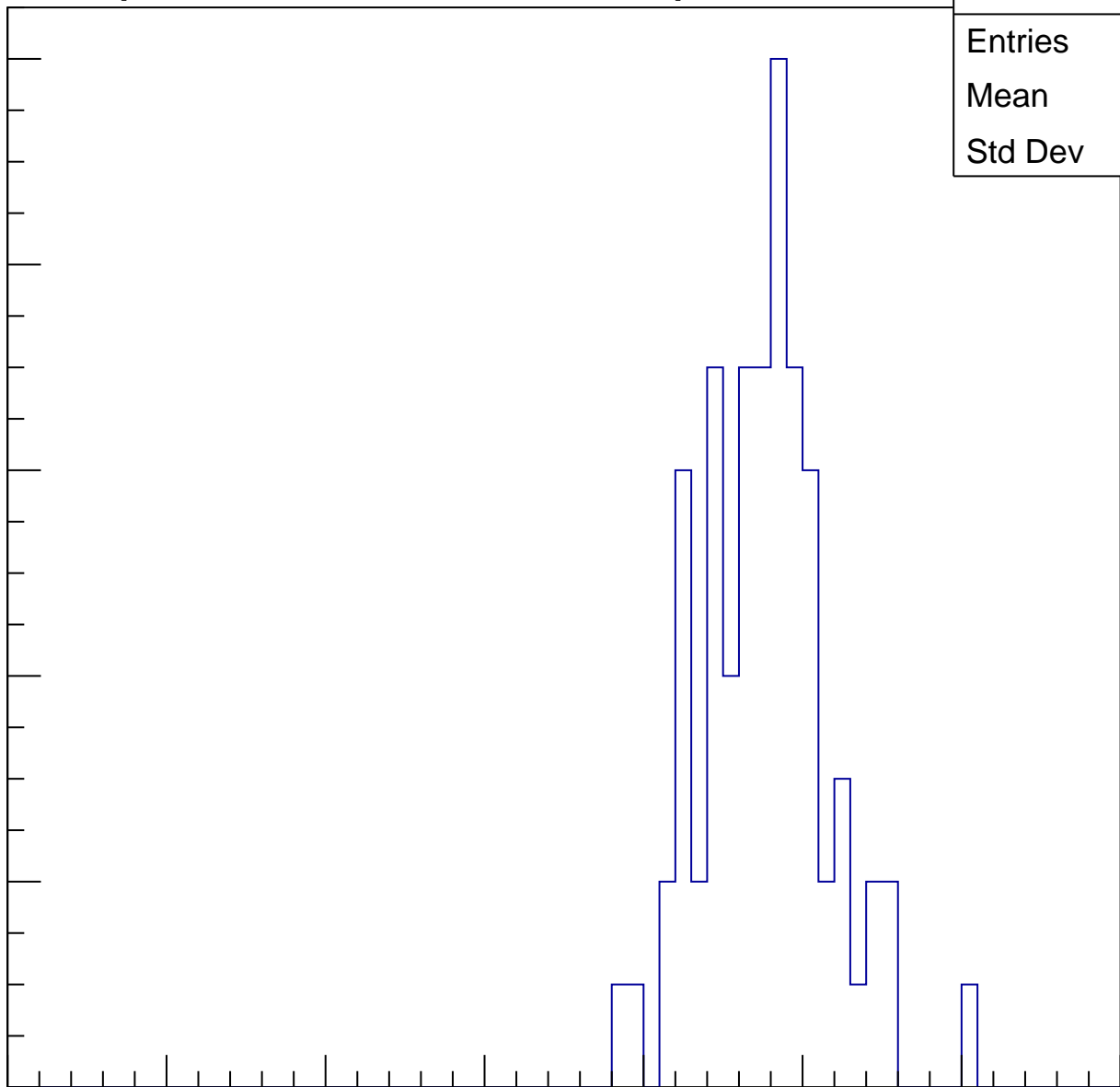
Entries	71
Mean	47.15
Std Dev	3.96

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

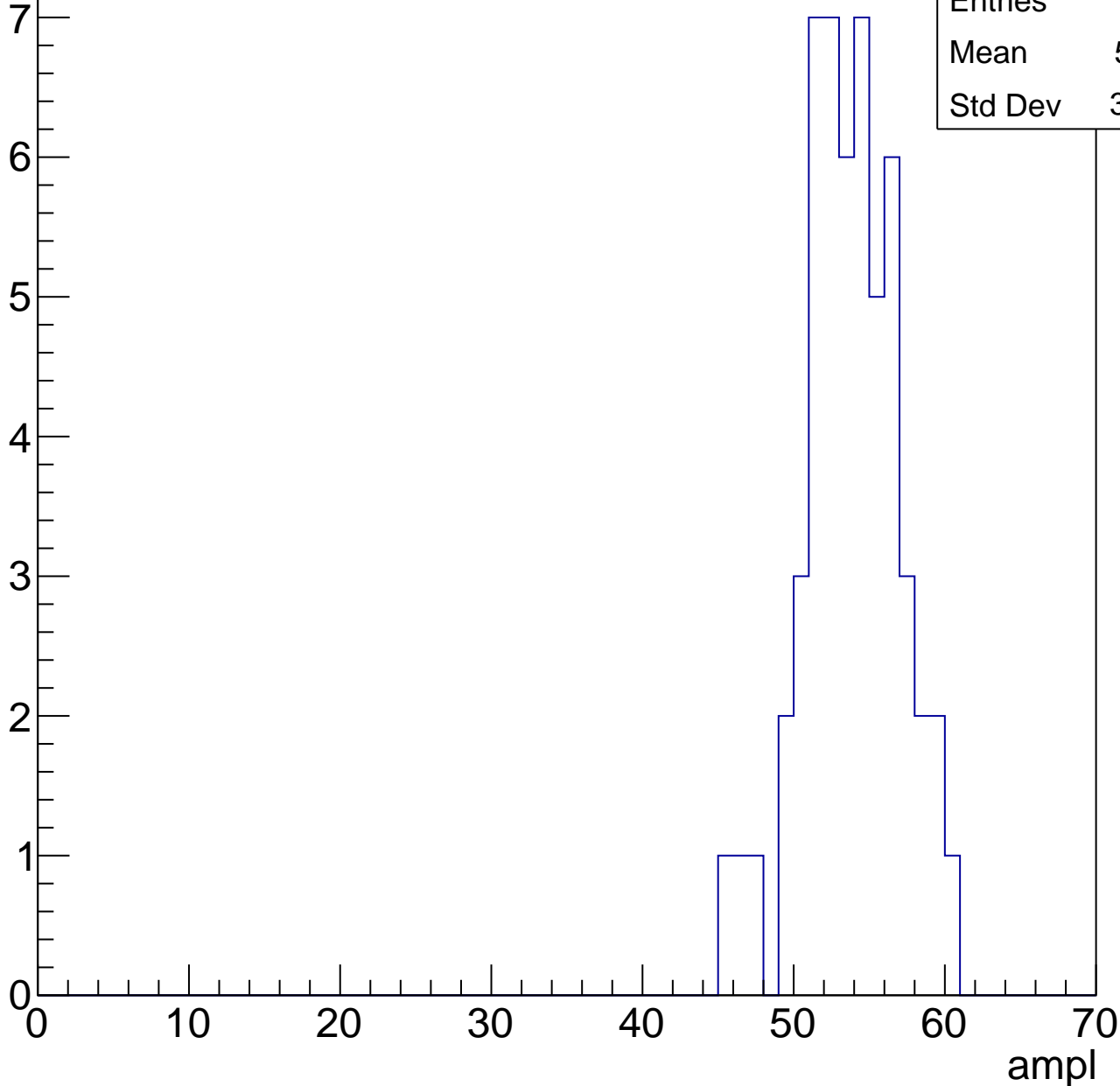


# B1L103S, U26-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	53.31
Std Dev	3.155

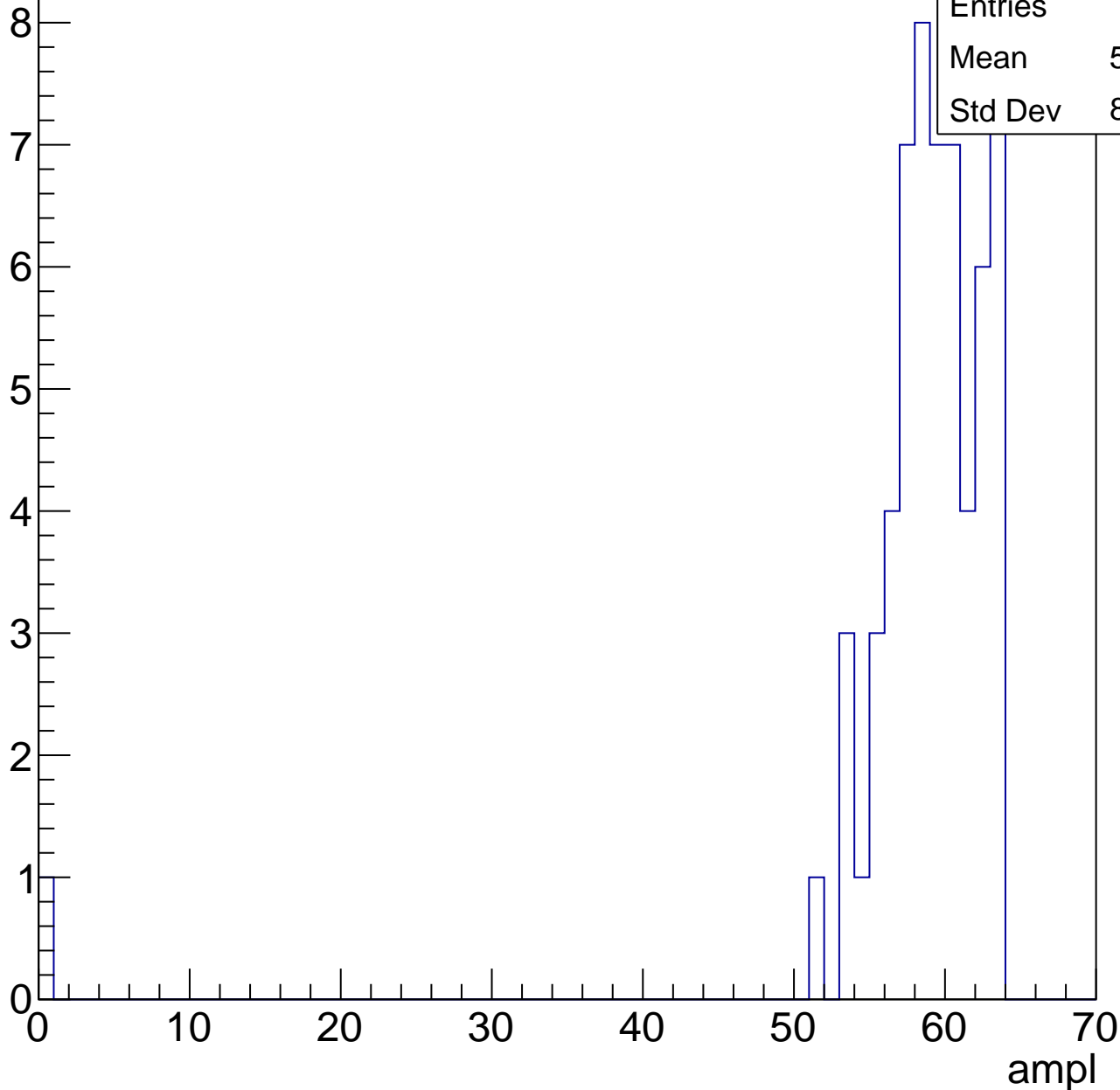


# B1L103S, U26-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	57.82
Std Dev	8.082

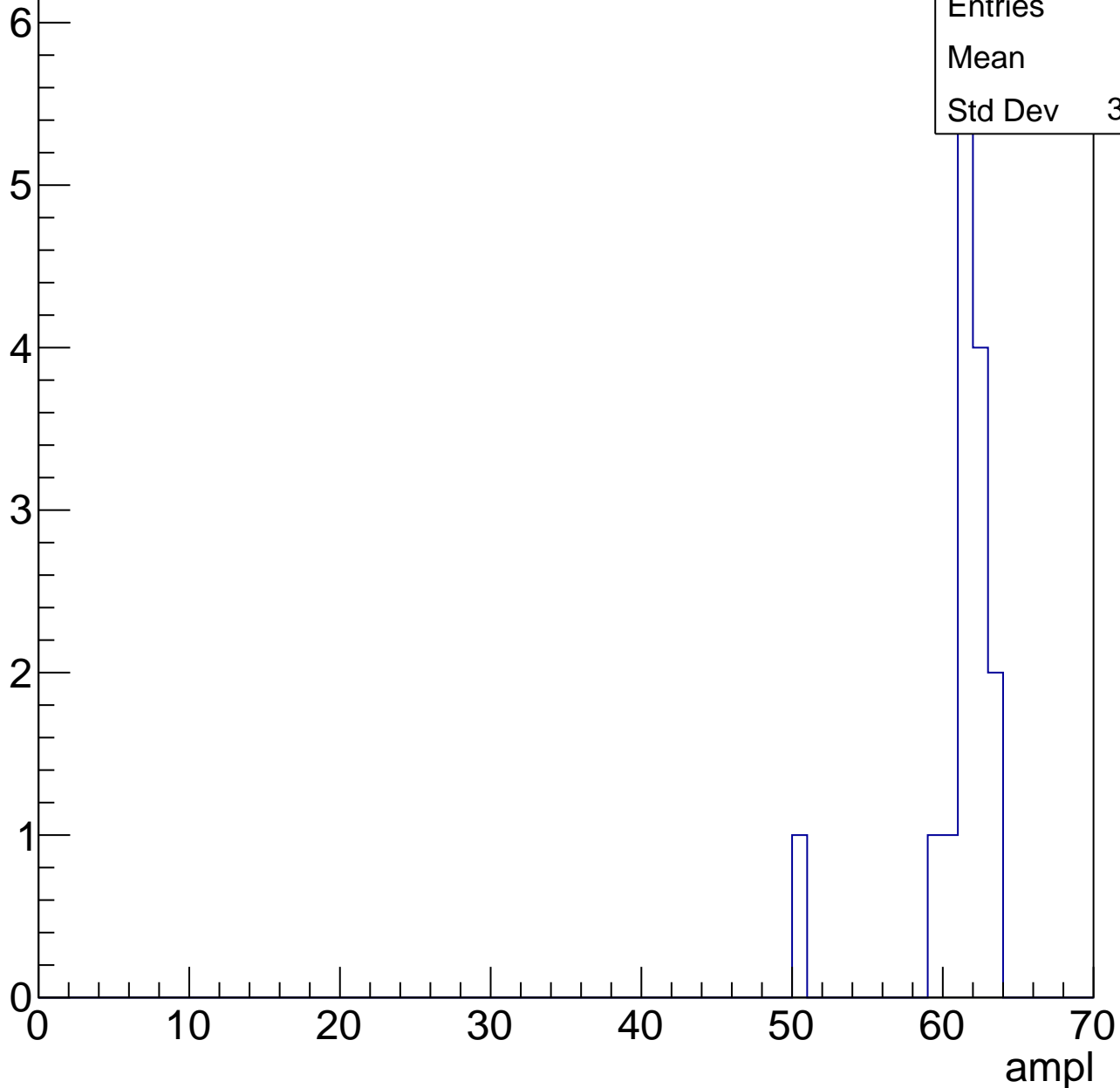


# B1L103S, U26-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	15
Mean	60.6
Std Dev	3.007





# B1L103S, U26-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U26-ch25, adc0

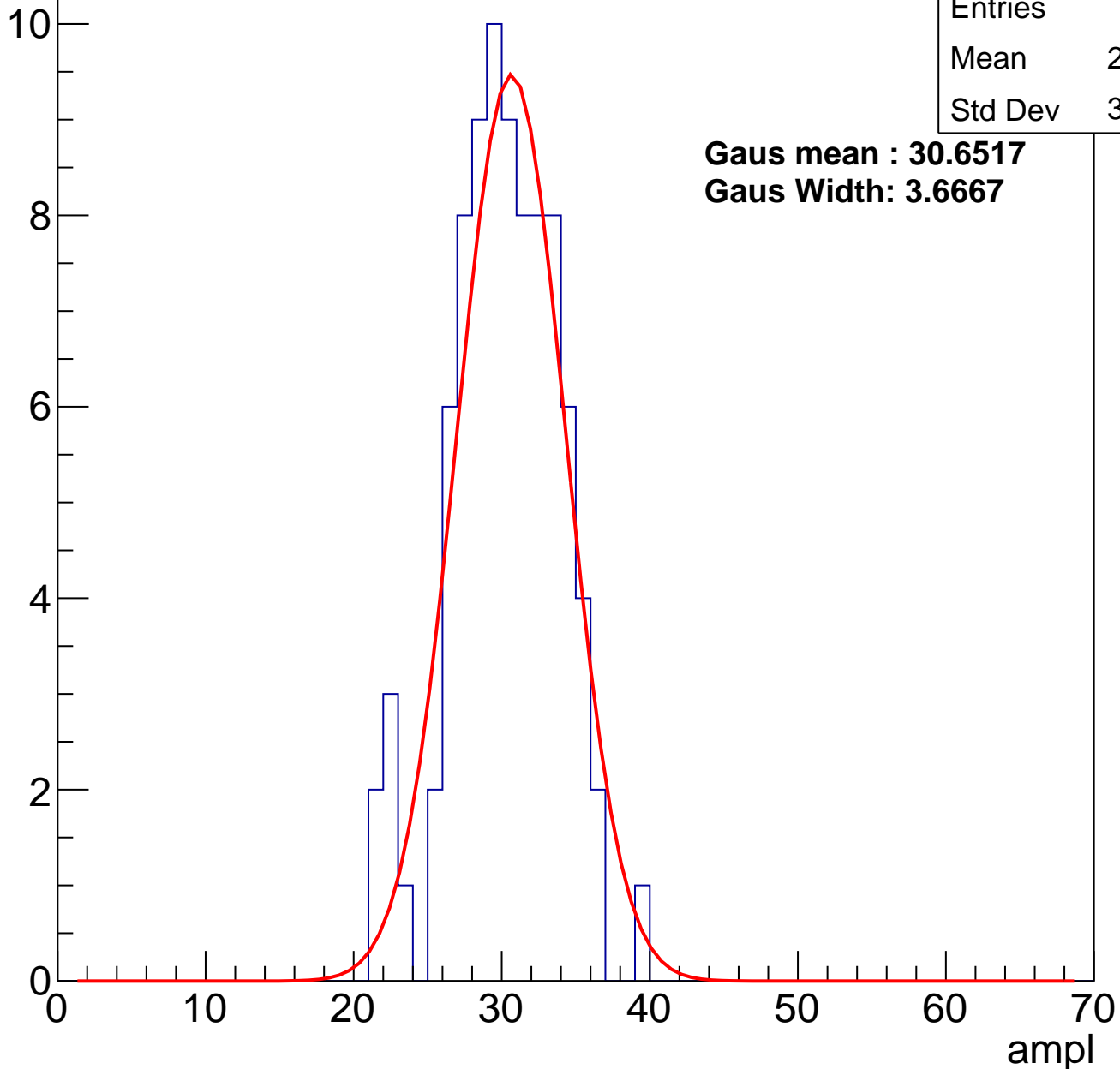
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	87
Mean	29.75
Std Dev	3.592

**Gaus mean : 30.6517**

**Gaus Width: 3.6667**

Entry



# B1L103S, U26-ch25, adc1

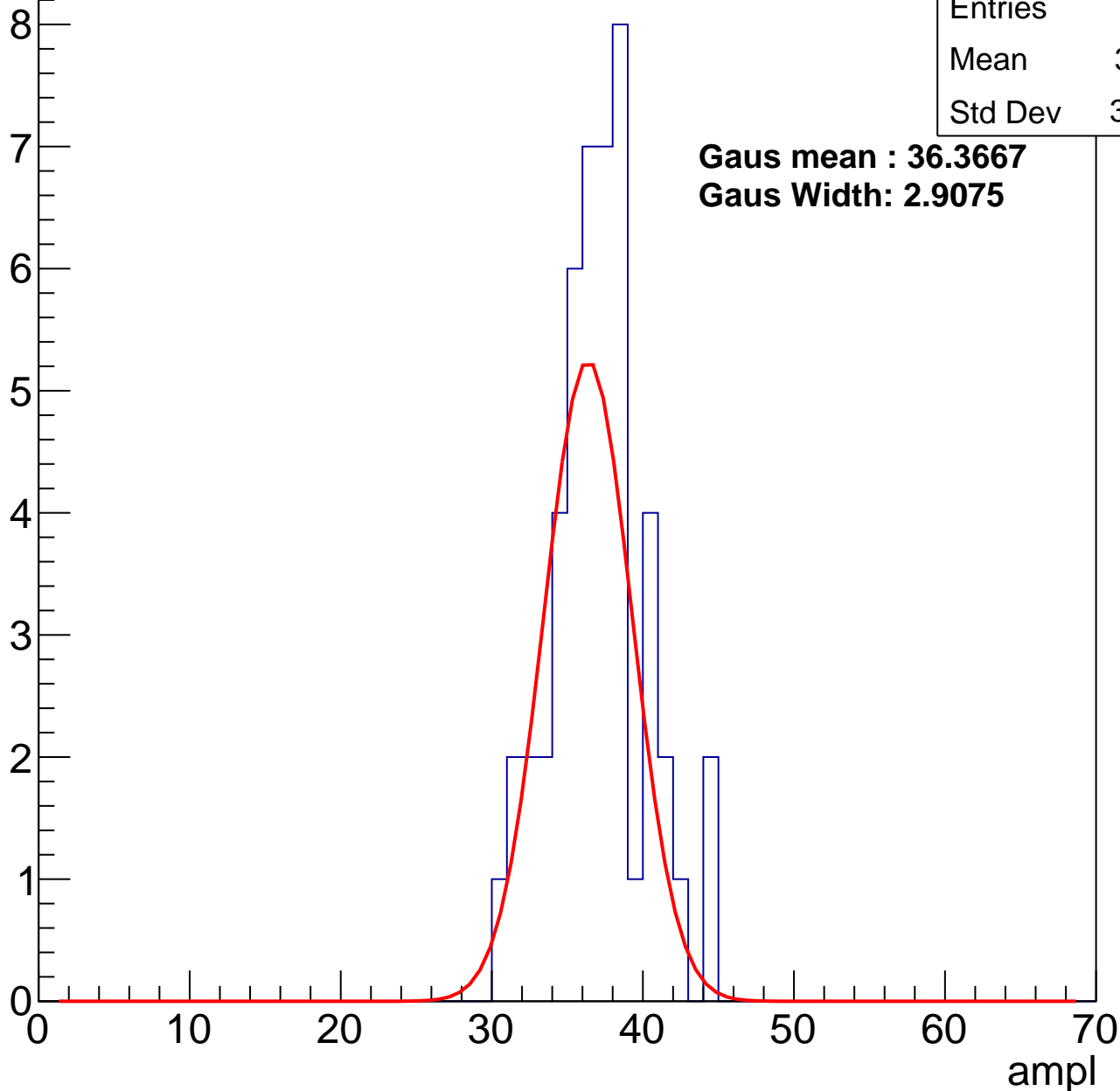
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	36.61
Std Dev	3.083

**Gaus mean : 36.3667**

**Gaus Width: 2.9075**



# B1L103S, U26-ch25, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	91
Mean	43.51
Std Dev	3.528

**Gaus mean : 44.0286**

**Gaus Width: 3.7529**

10

8

6

4

2

0

0

10

20

30

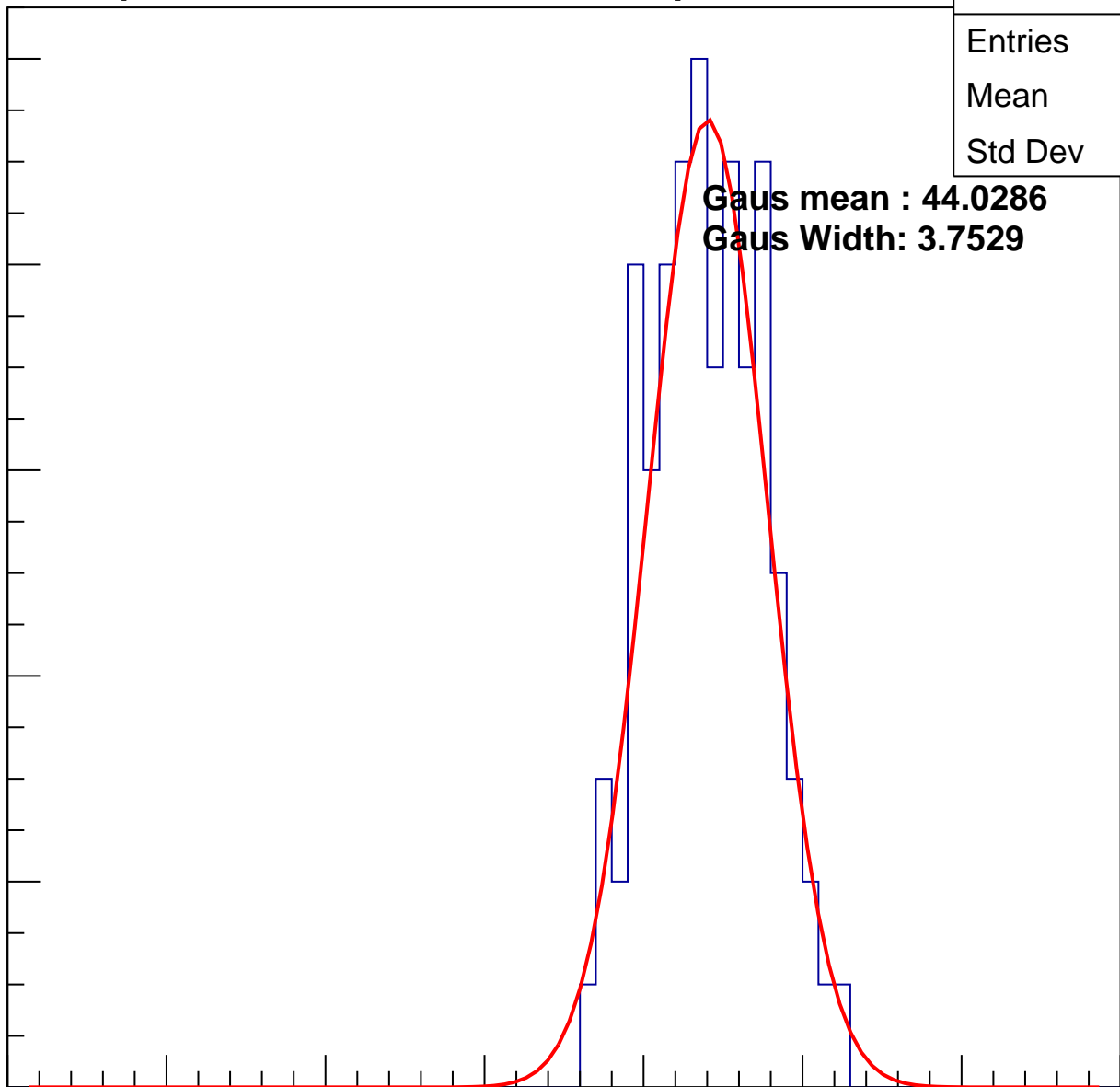
40

50

60

70

ampl

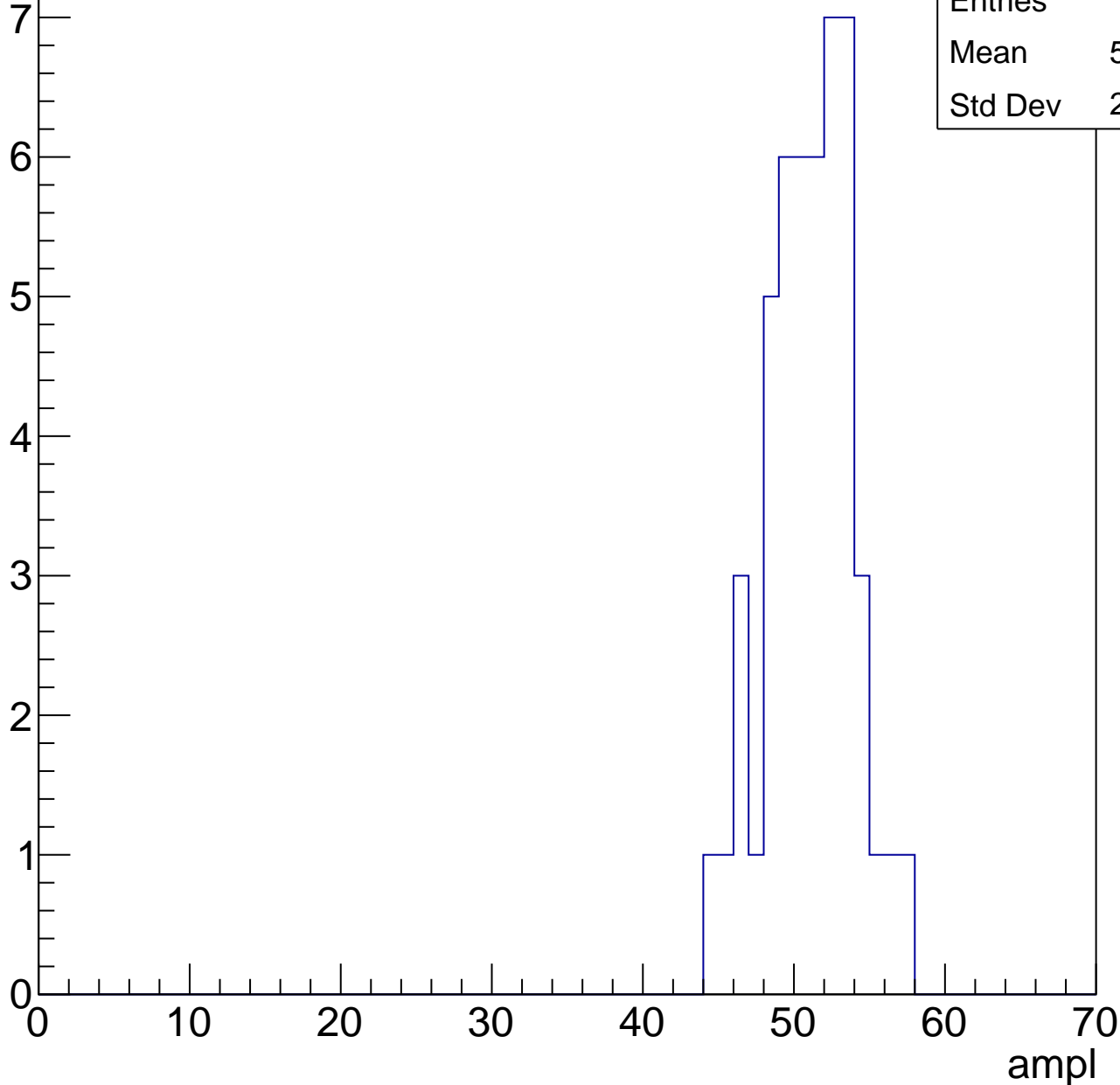


# B1L103S, U26-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

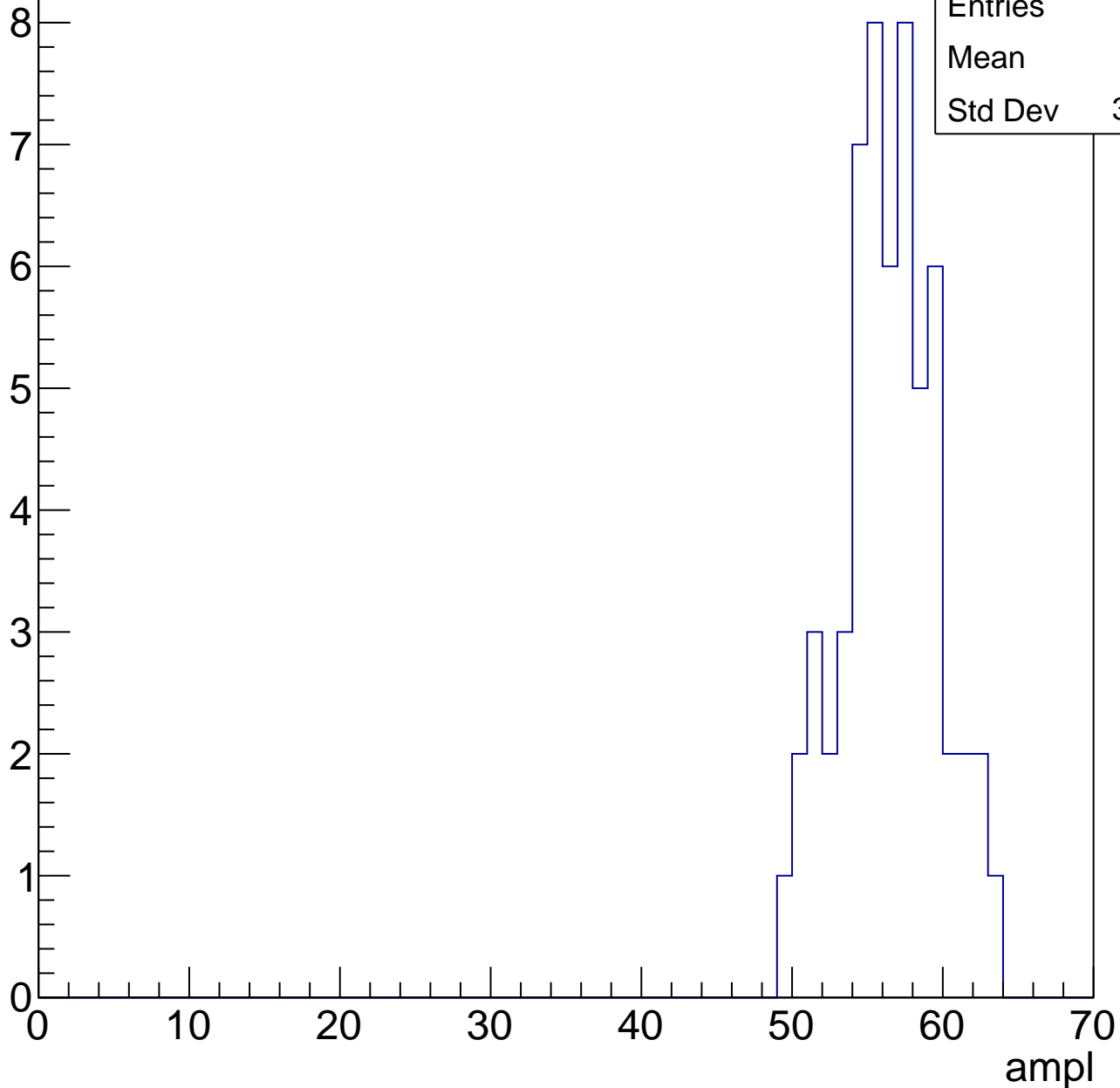
Entries	49
Mean	50.59
Std Dev	2.792



# B1L103S, U26-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

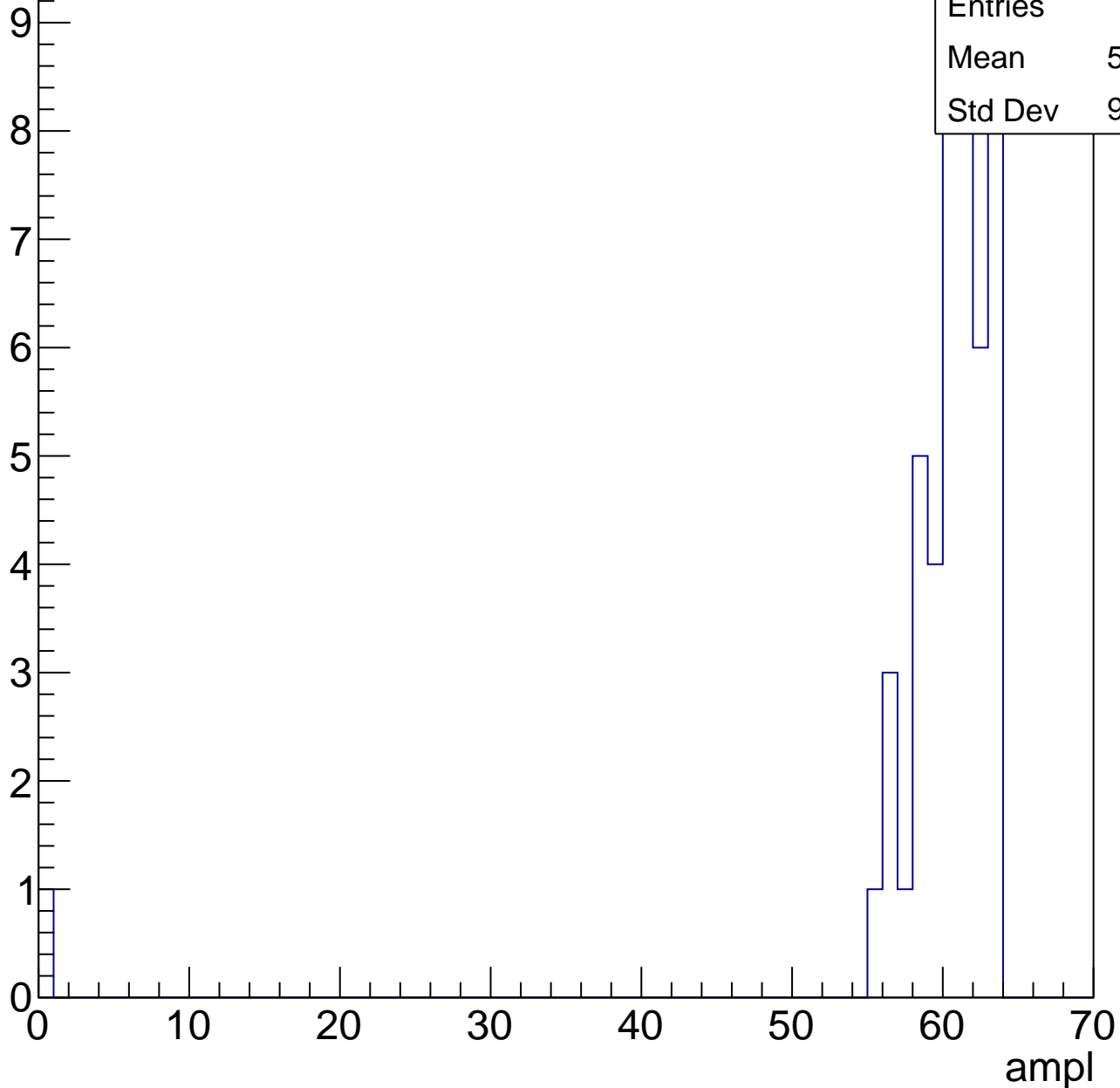
Entry



# B1L103S, U26-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U26-ch26, adc0

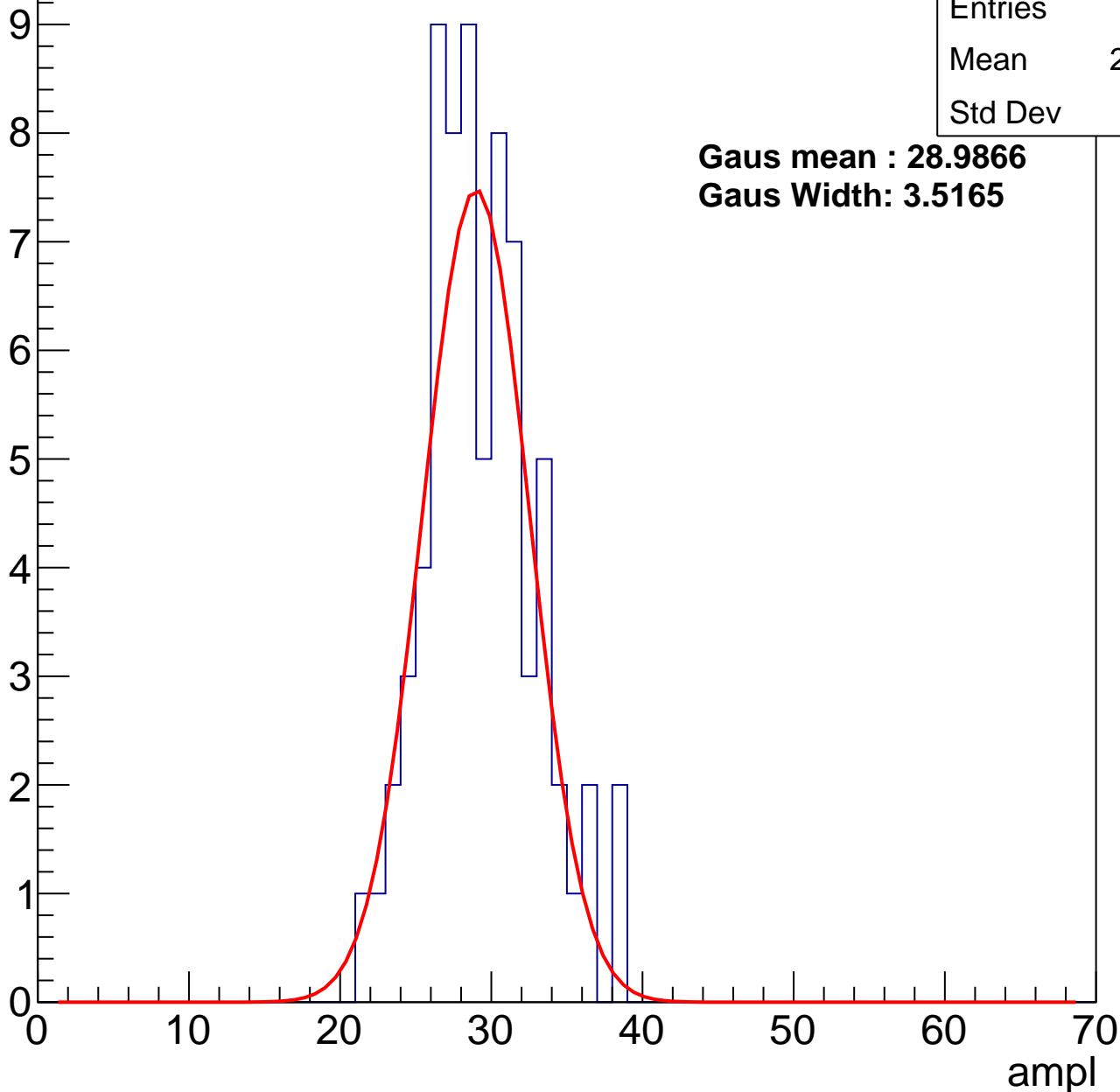
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	28.85
Std Dev	3.6

**Gaus mean : 28.9866**

**Gaus Width: 3.5165**



# B1L103S, U26-ch26, adc1

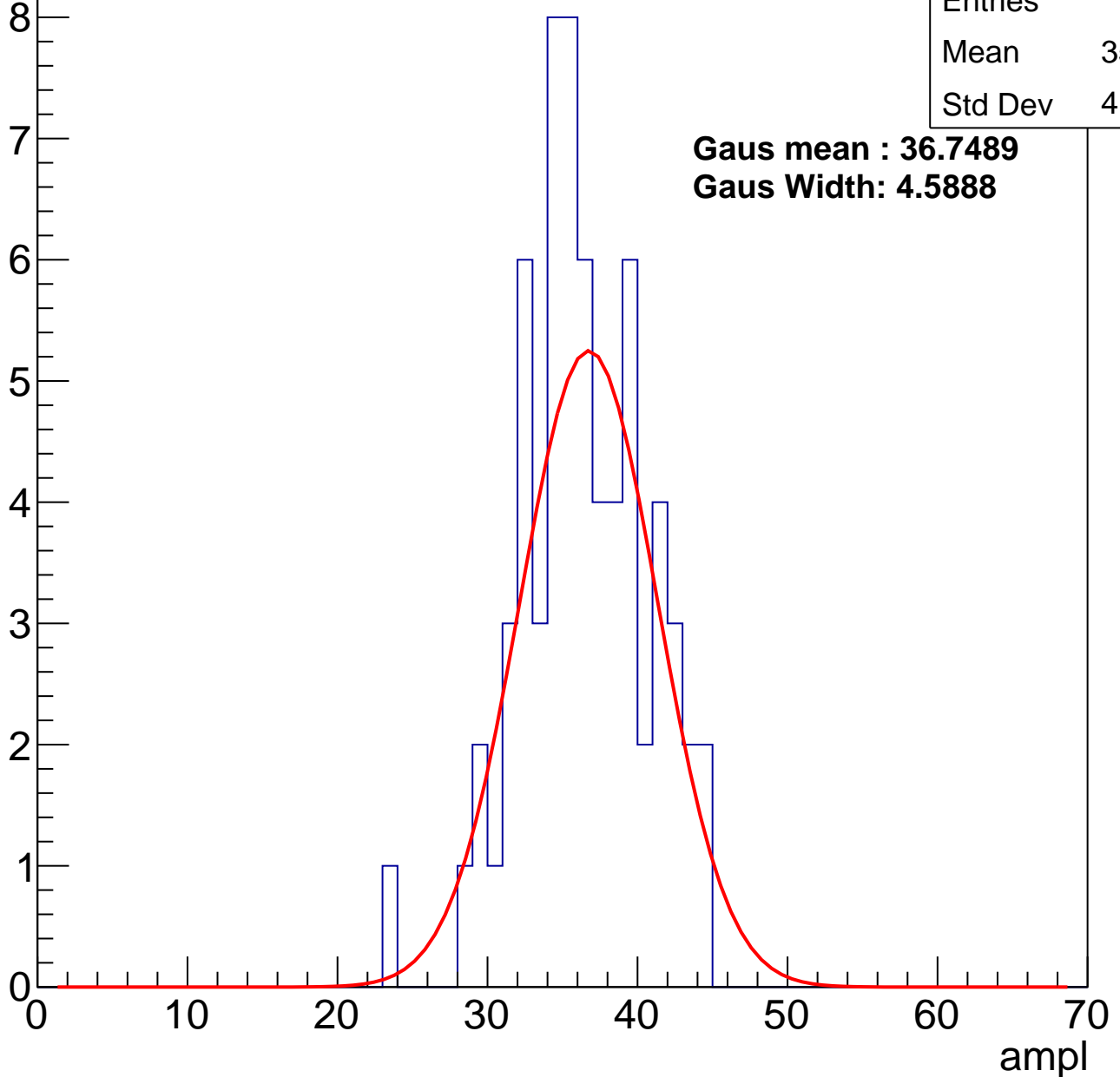
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	35.89
Std Dev	4.164

**Gaus mean : 36.7489**

**Gaus Width: 4.5888**



# B1L103S, U26-ch26, adc2

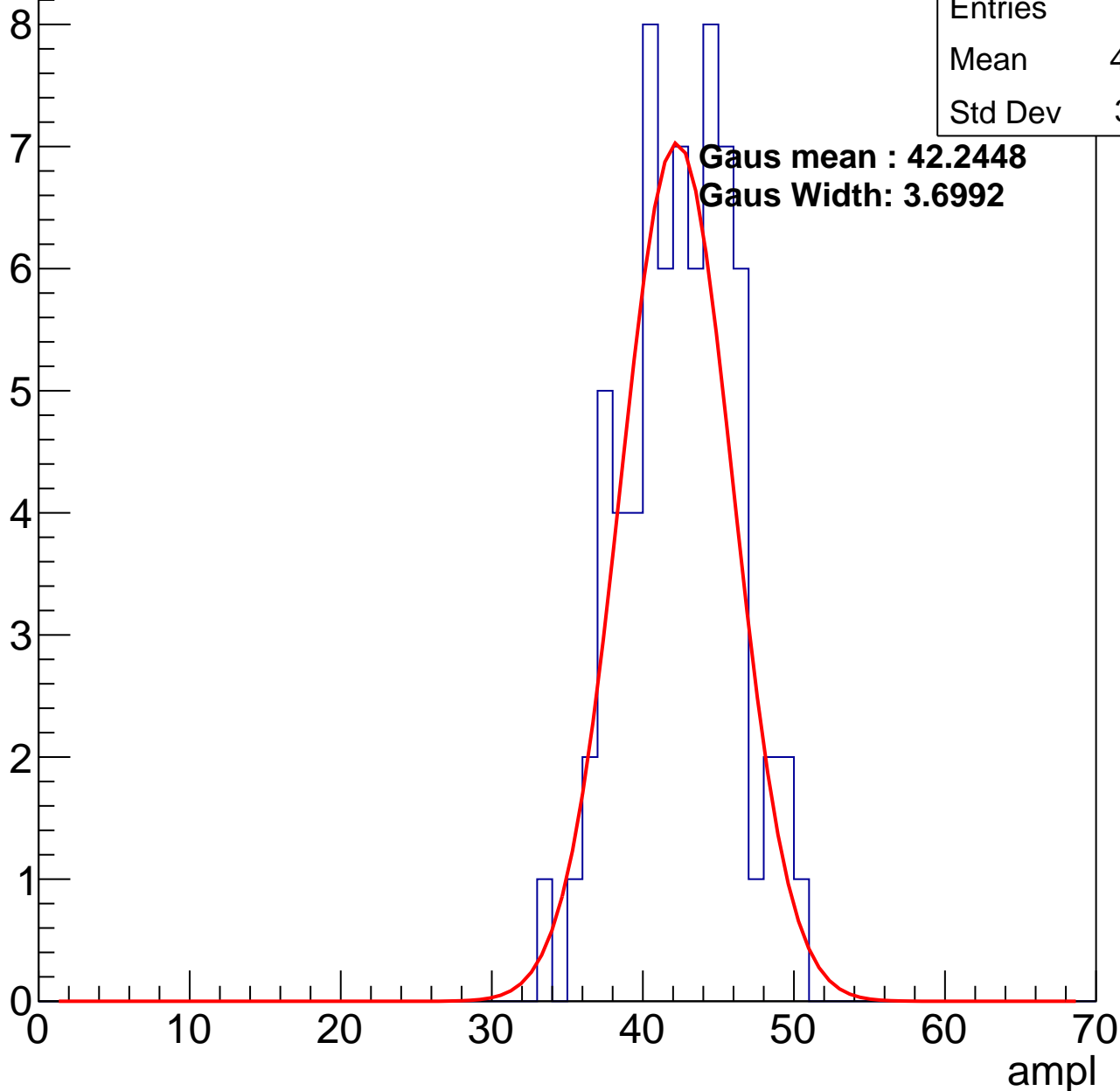
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	42.04
Std Dev	3.601

**Gaus mean : 42.2448**

**Gaus Width: 3.6992**

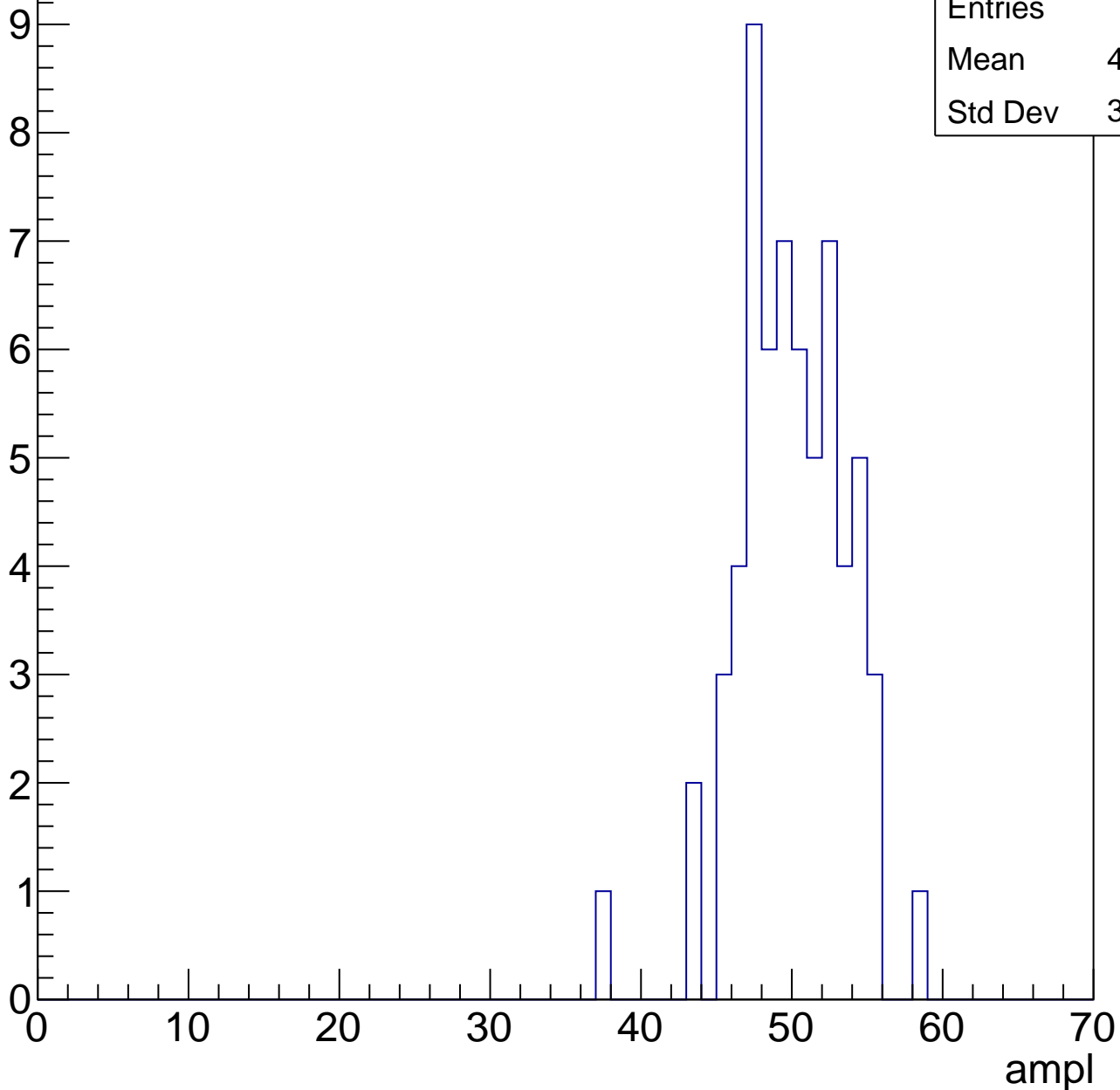


# B1L103S, U26-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	49.52
Std Dev	3.545

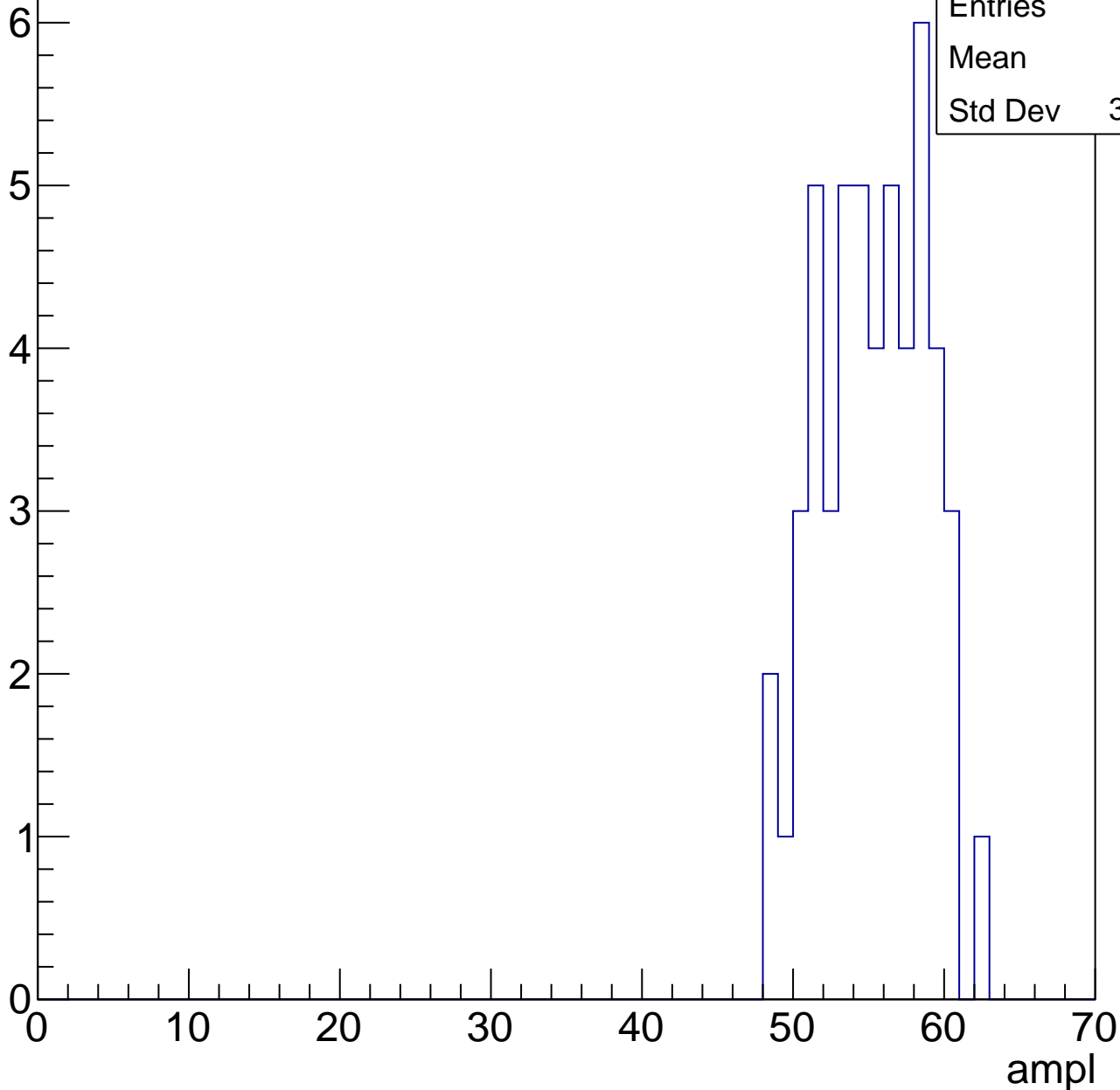


# B1L103S, U26-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	54.8
Std Dev	3.436



# B1L103S, U26-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

6

5

4

3

2

1

0

Entries 45

Mean 57.96

Std Dev 9.09

0

10

20

30

40

50

60

ampl

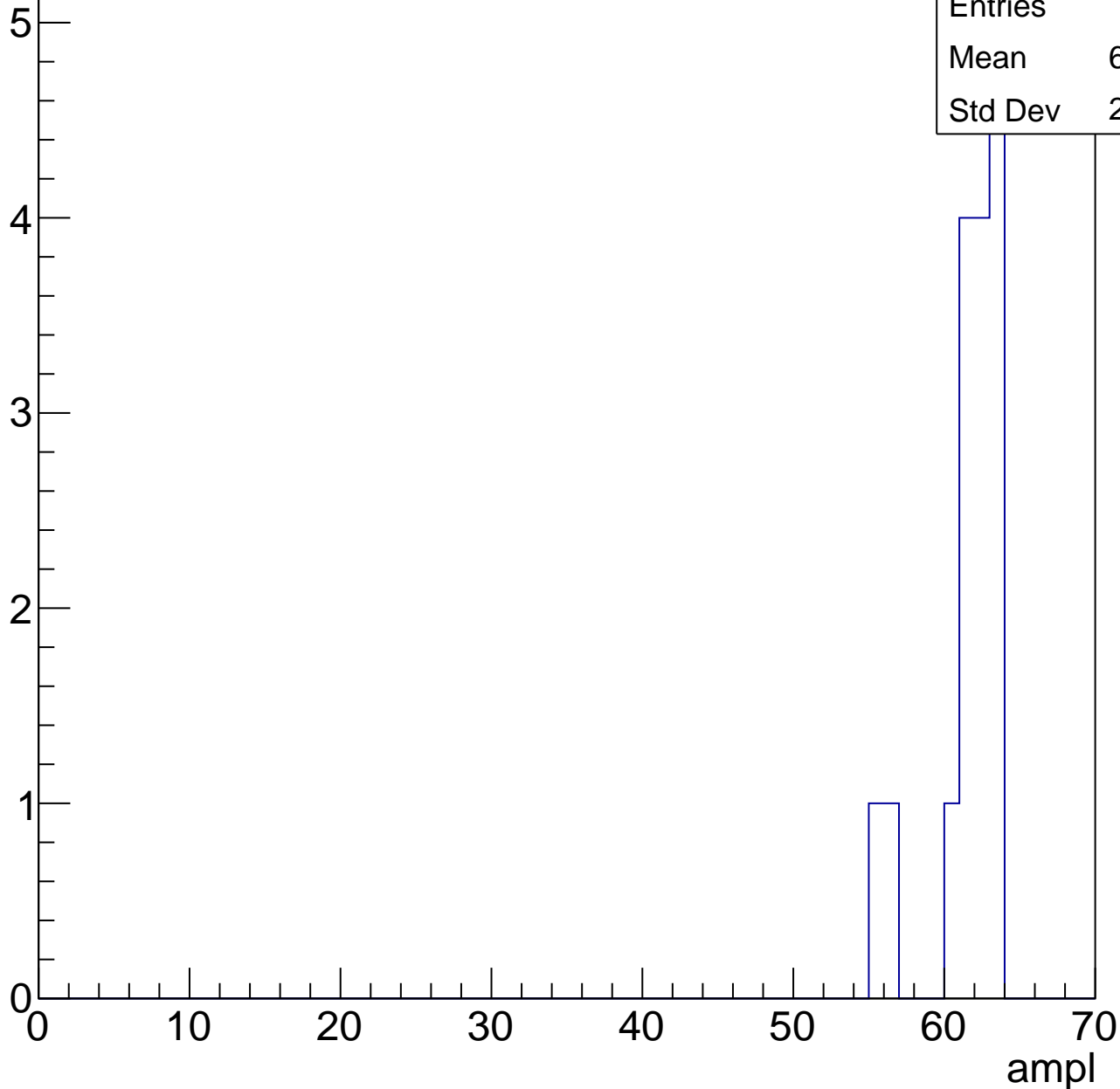
0

# B1L103S, U26-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	16
Mean	61.12
Std Dev	2.315





# B1L103S, U26-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch27, adc0

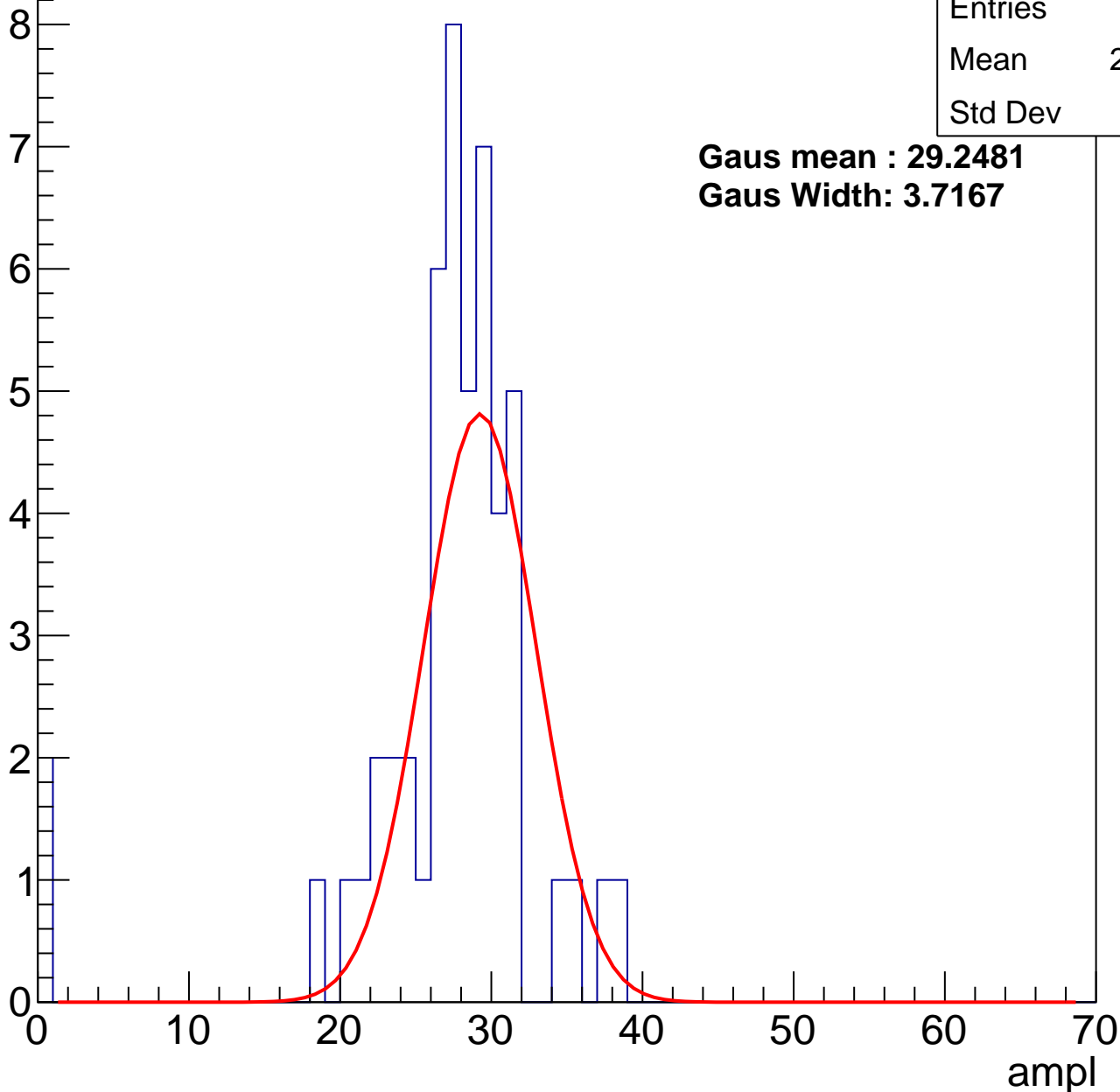
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	26.59
Std Dev	6.58

**Gaus mean : 29.2481**

**Gaus Width: 3.7167**



# B1L103S, U26-ch27, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	96
Mean	34.73
Std Dev	4.045

**Gaus mean : 34.9120**

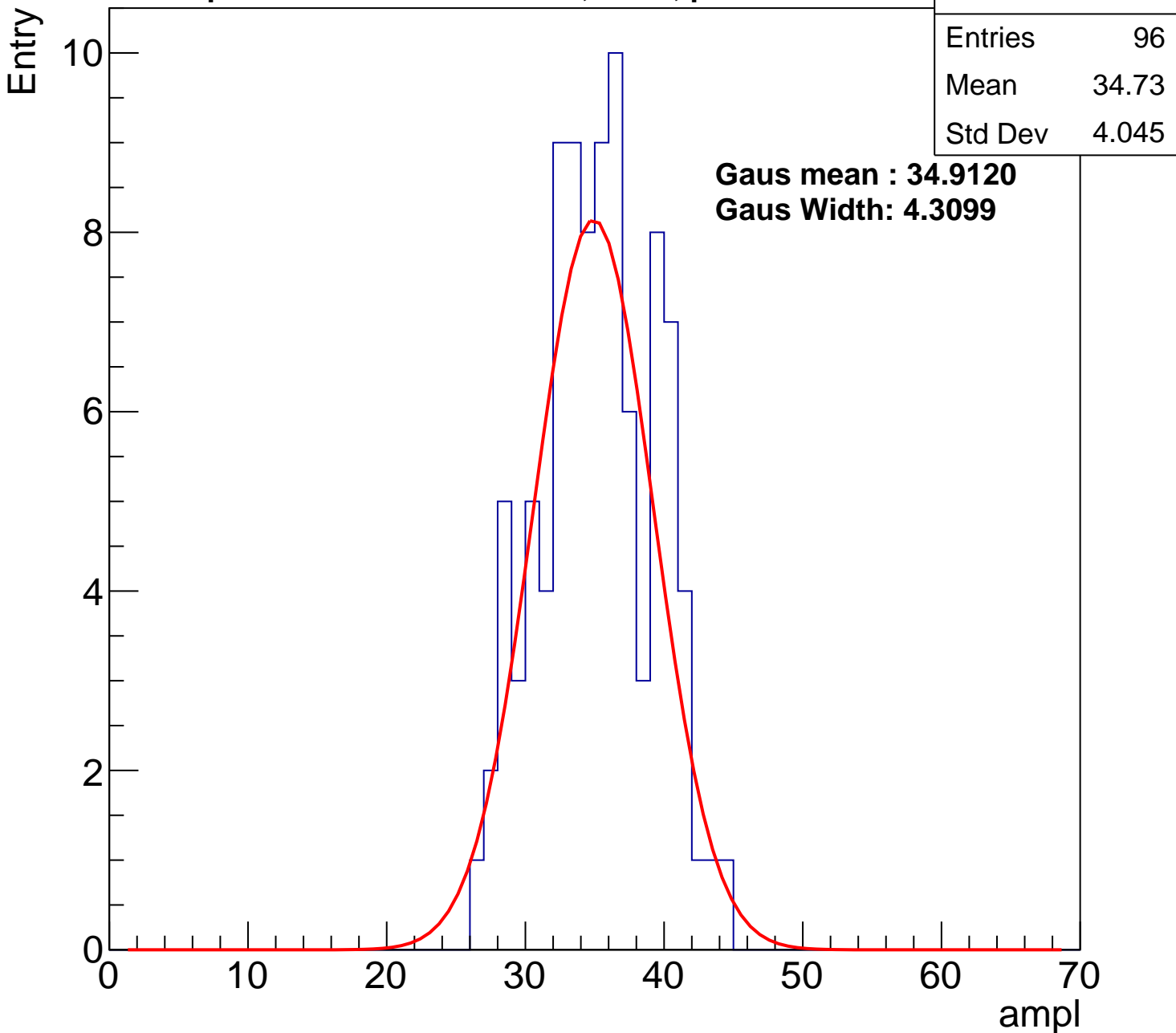
**Gaus Width: 4.3099**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch27, adc2

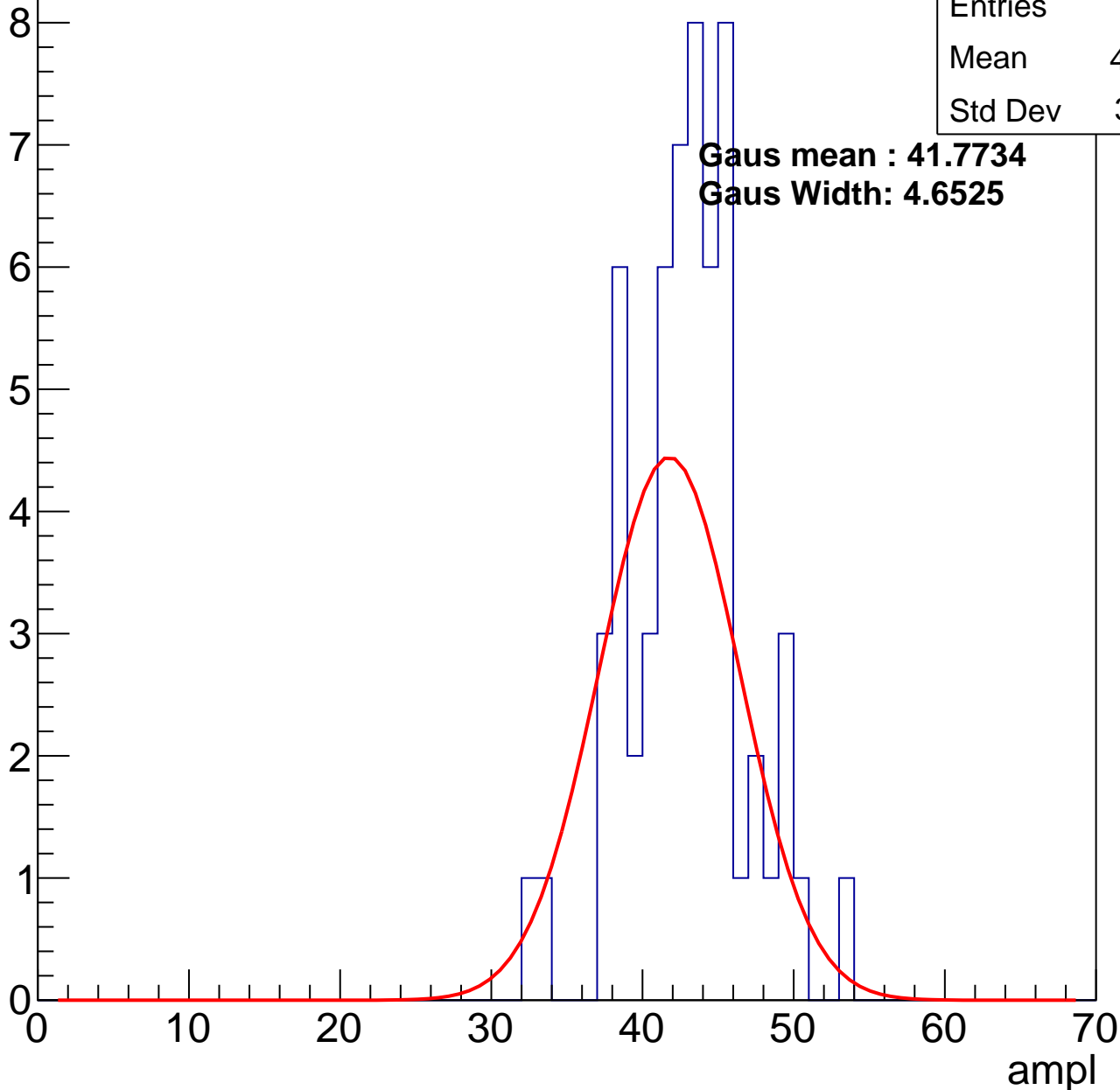
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	42.47
Std Dev	3.901

**Gaus mean : 41.7734**

**Gaus Width: 4.6525**

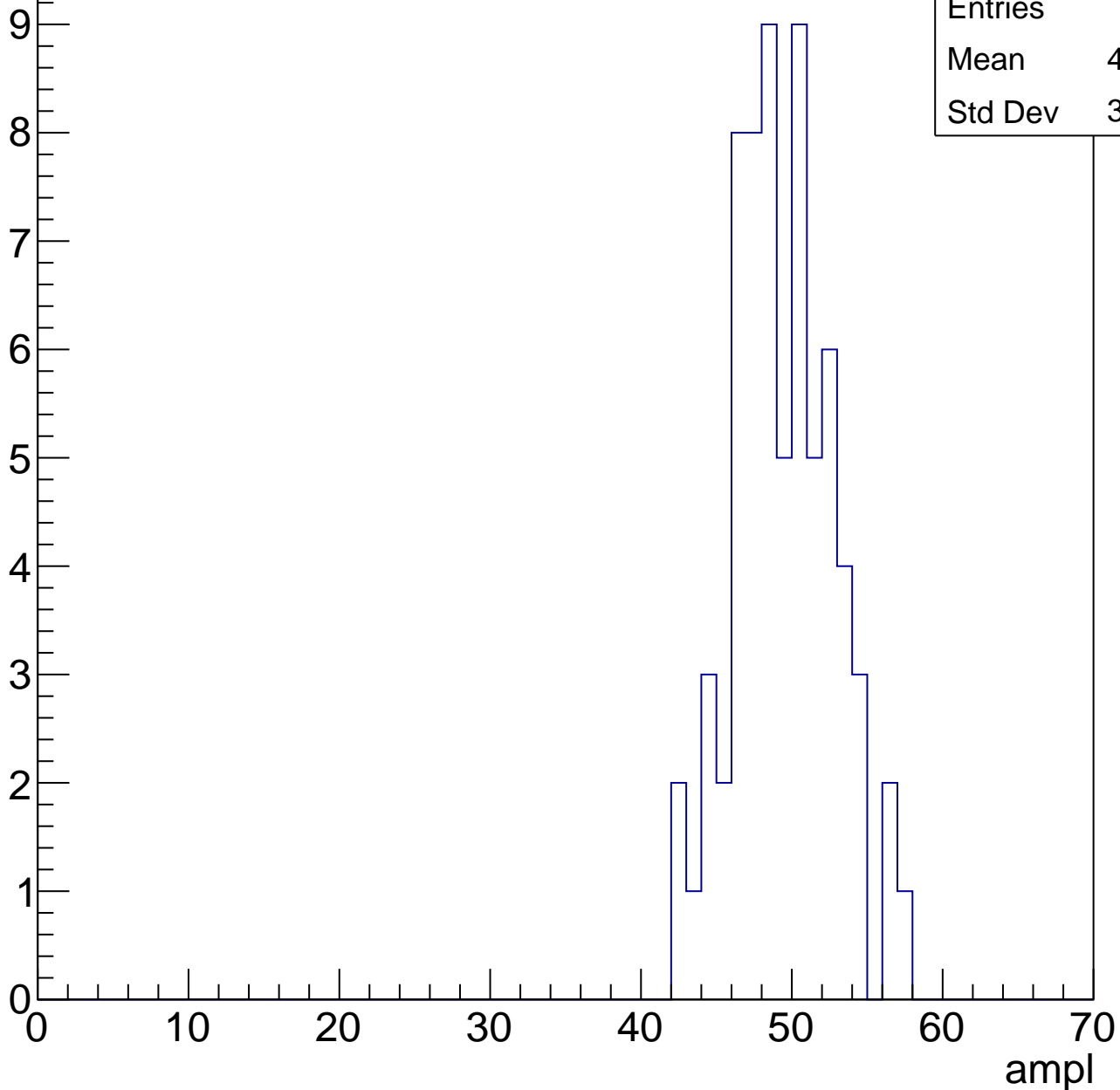


# B1L103S, U26-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

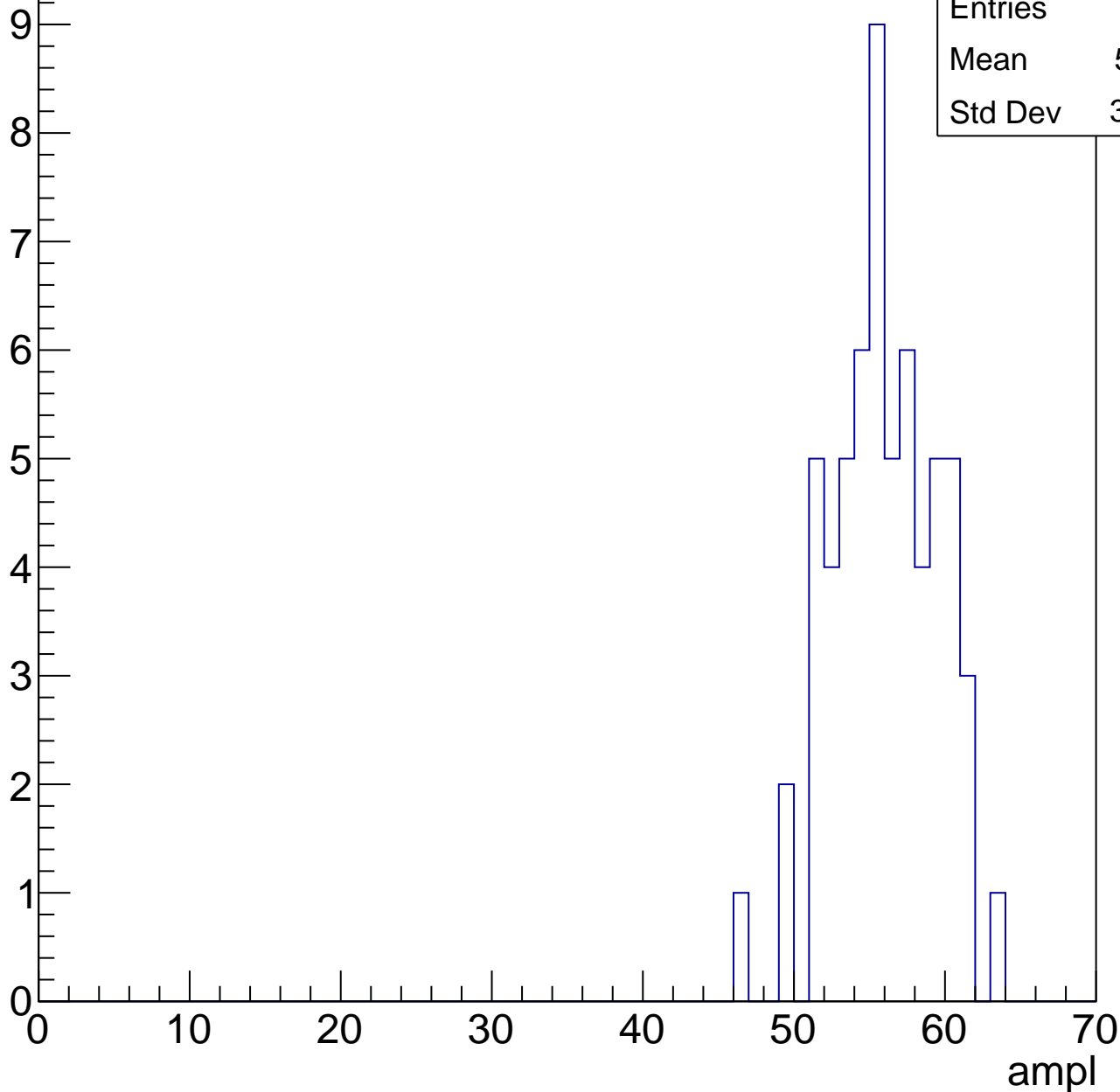
Entries	68
Mean	48.97
Std Dev	3.294



# B1L103S, U26-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

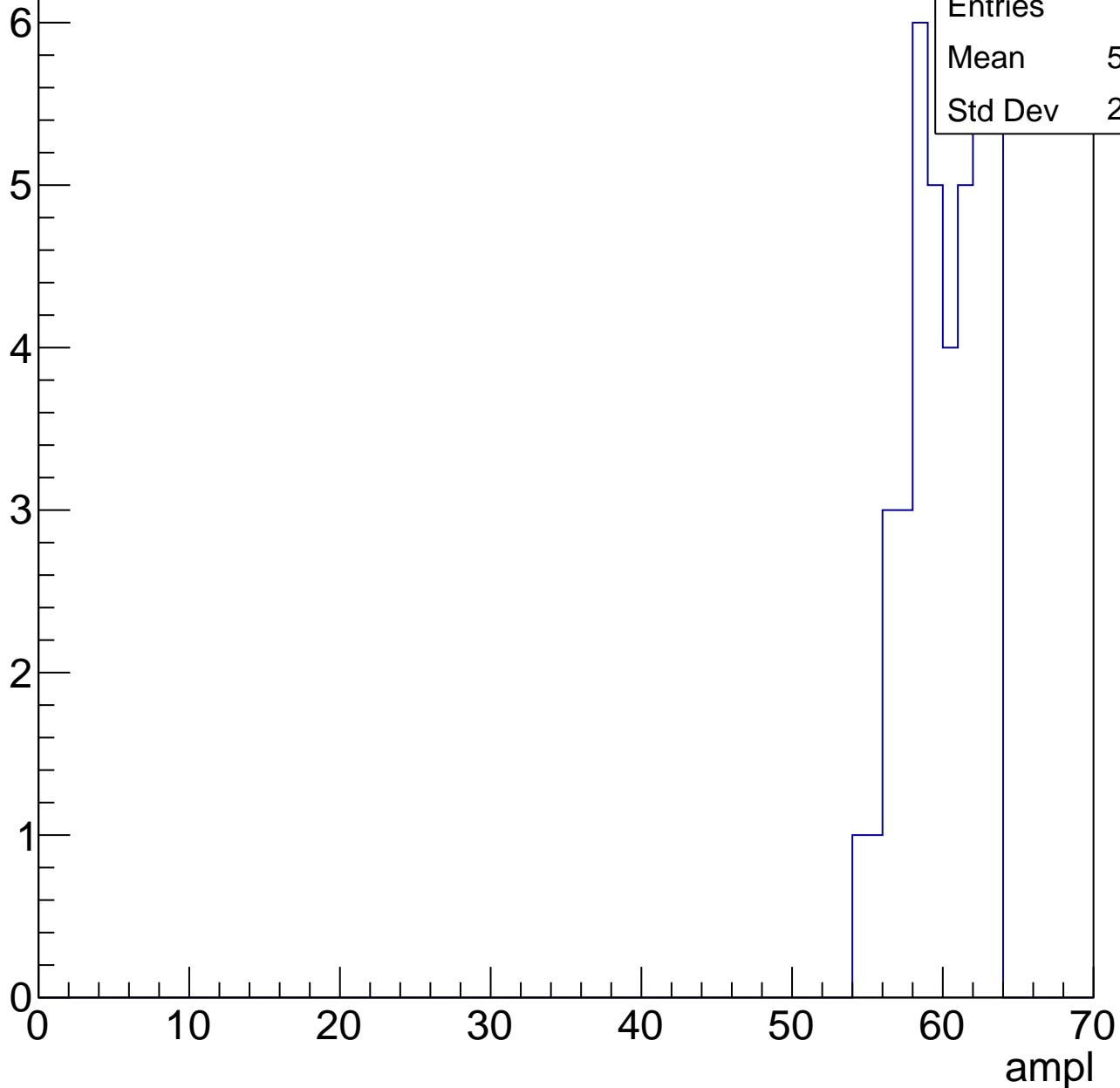
Entry



# B1L103S, U26-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

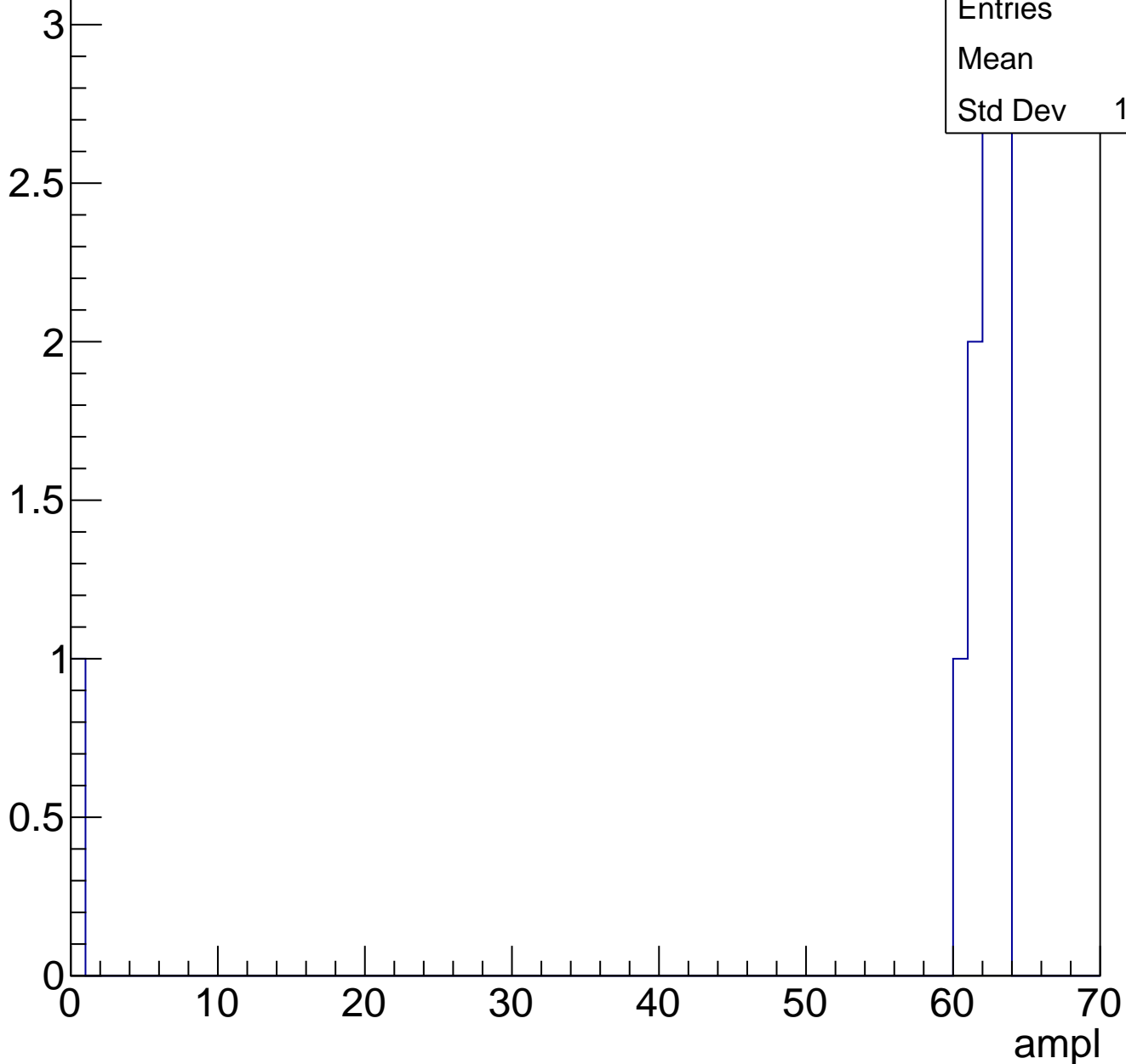
Entry



# B1L103S, U26-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch28, adc0

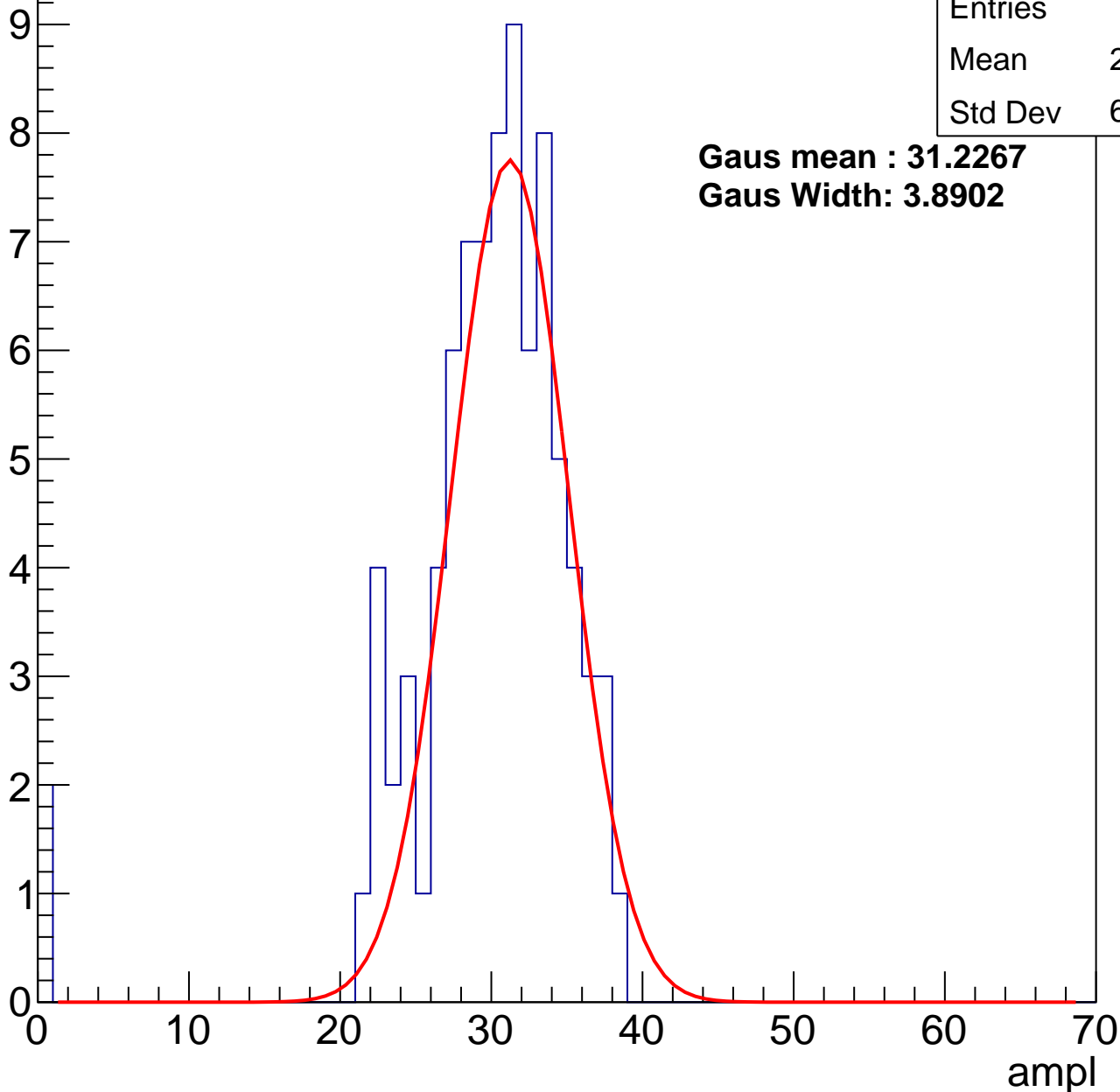
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	84
Mean	29.27
Std Dev	6.056

**Gaus mean : 31.2267**

**Gaus Width: 3.8902**



# B1L103S, U26-ch28, adc1

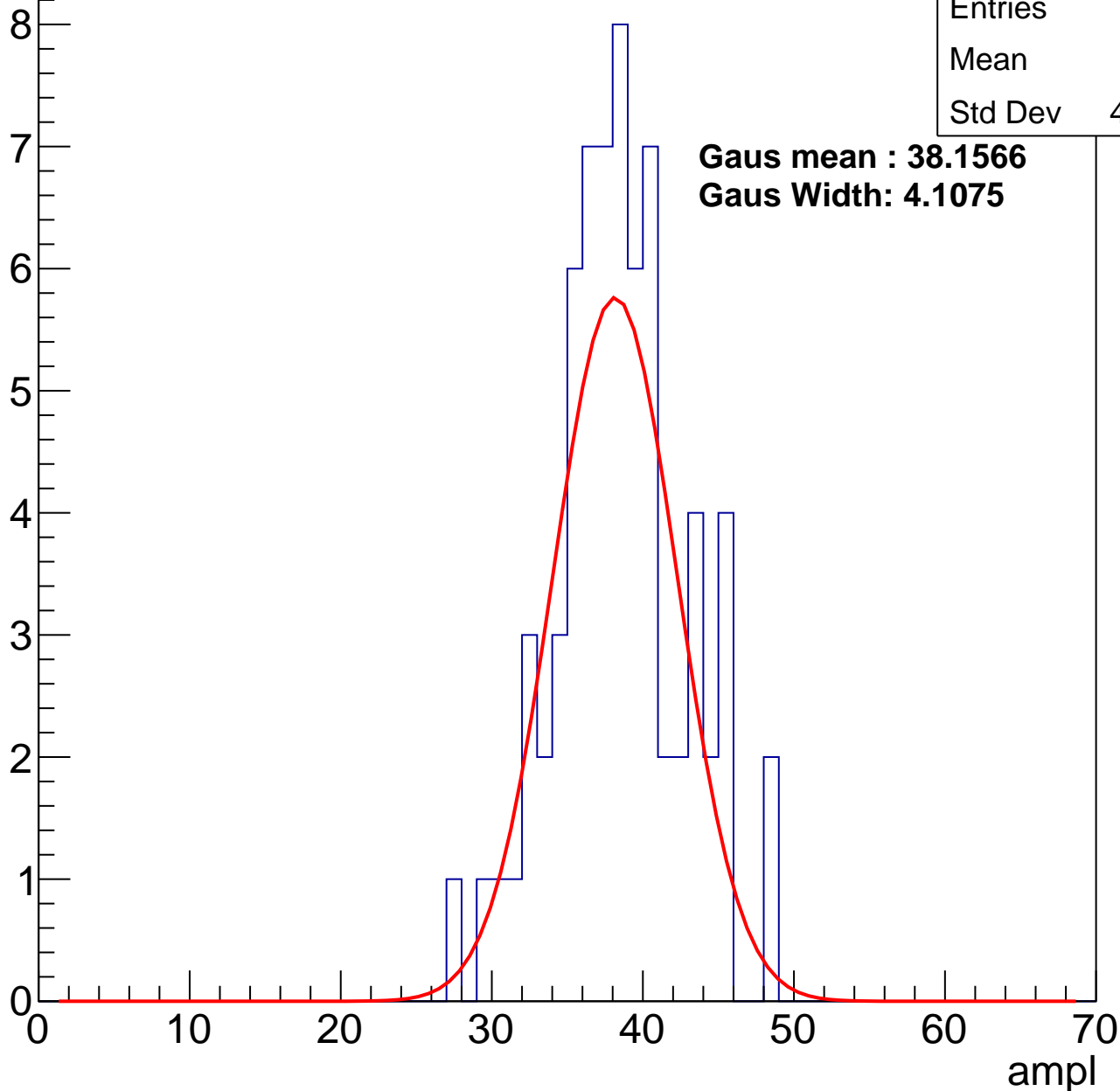
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	38
Std Dev	4.277

**Gaus mean : 38.1566**

**Gaus Width: 4.1075**



# B1L103S, U26-ch28, adc2

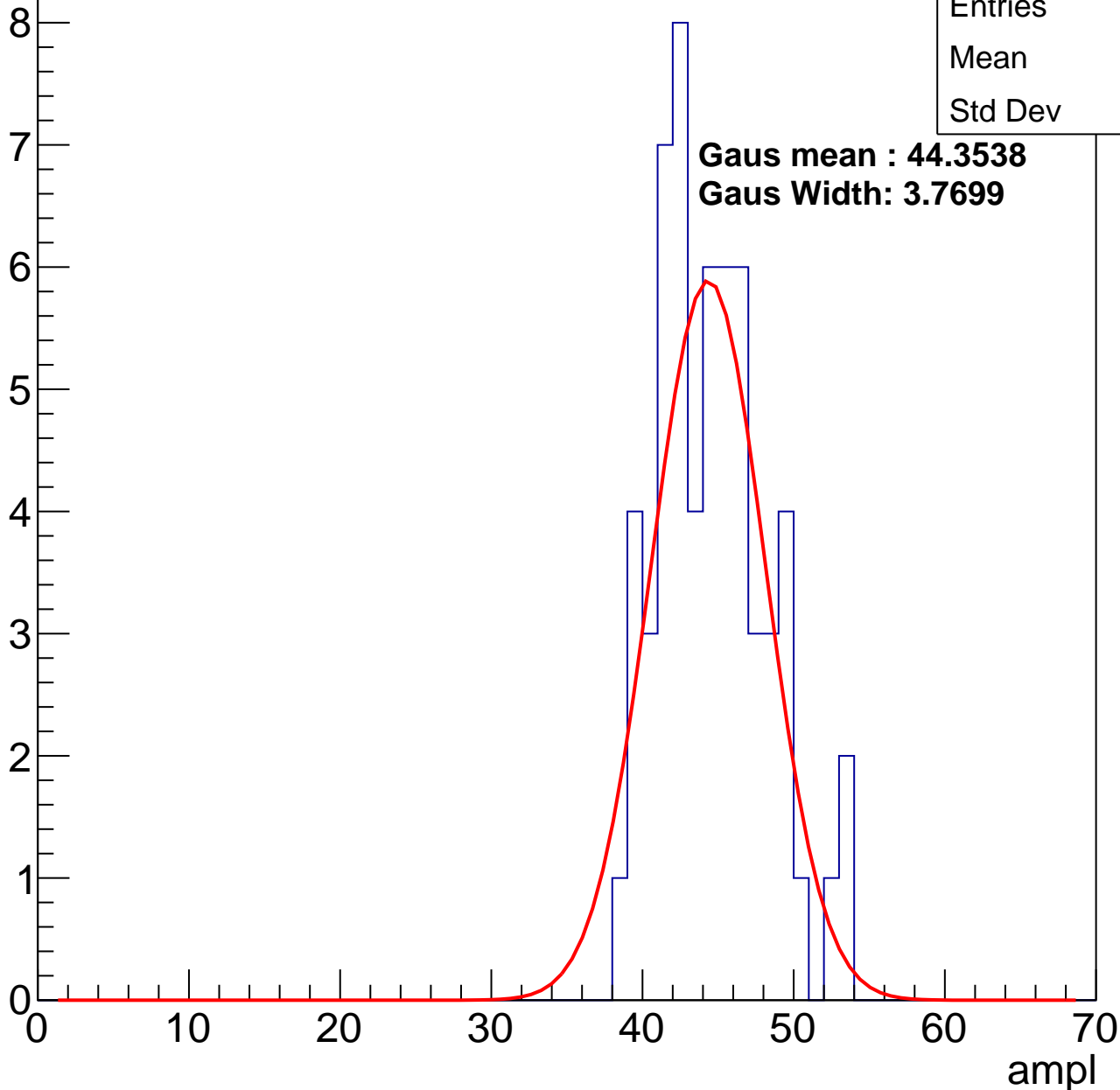
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	44.2
Std Dev	3.56

**Gaus mean : 44.3538**

**Gaus Width: 3.7699**



# B1L103S, U26-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	70
Mean	50.53
Std Dev	3.718

Entry

10

8

6

4

2

0

0

10

20

30

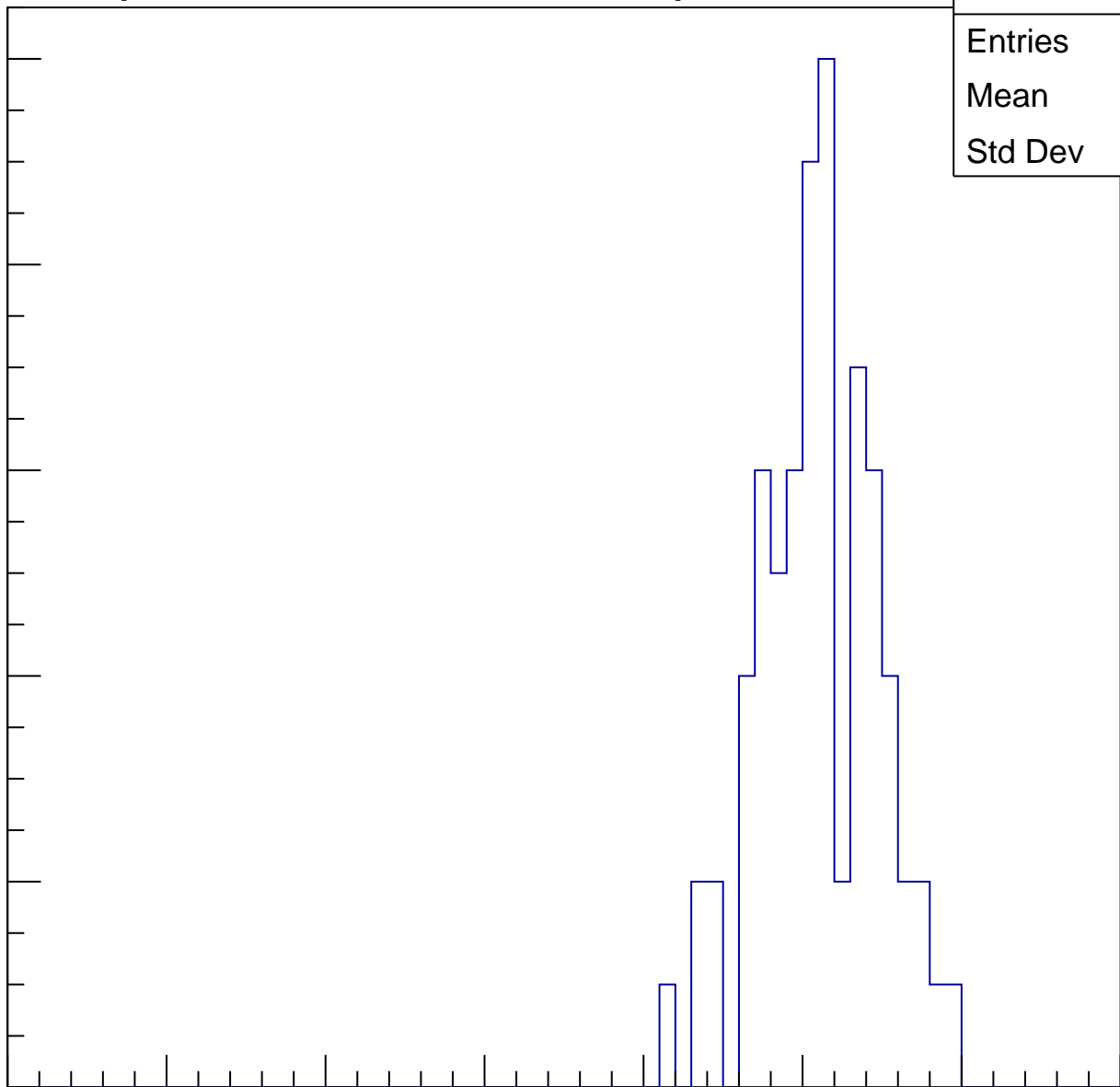
40

50

60

70

ampl

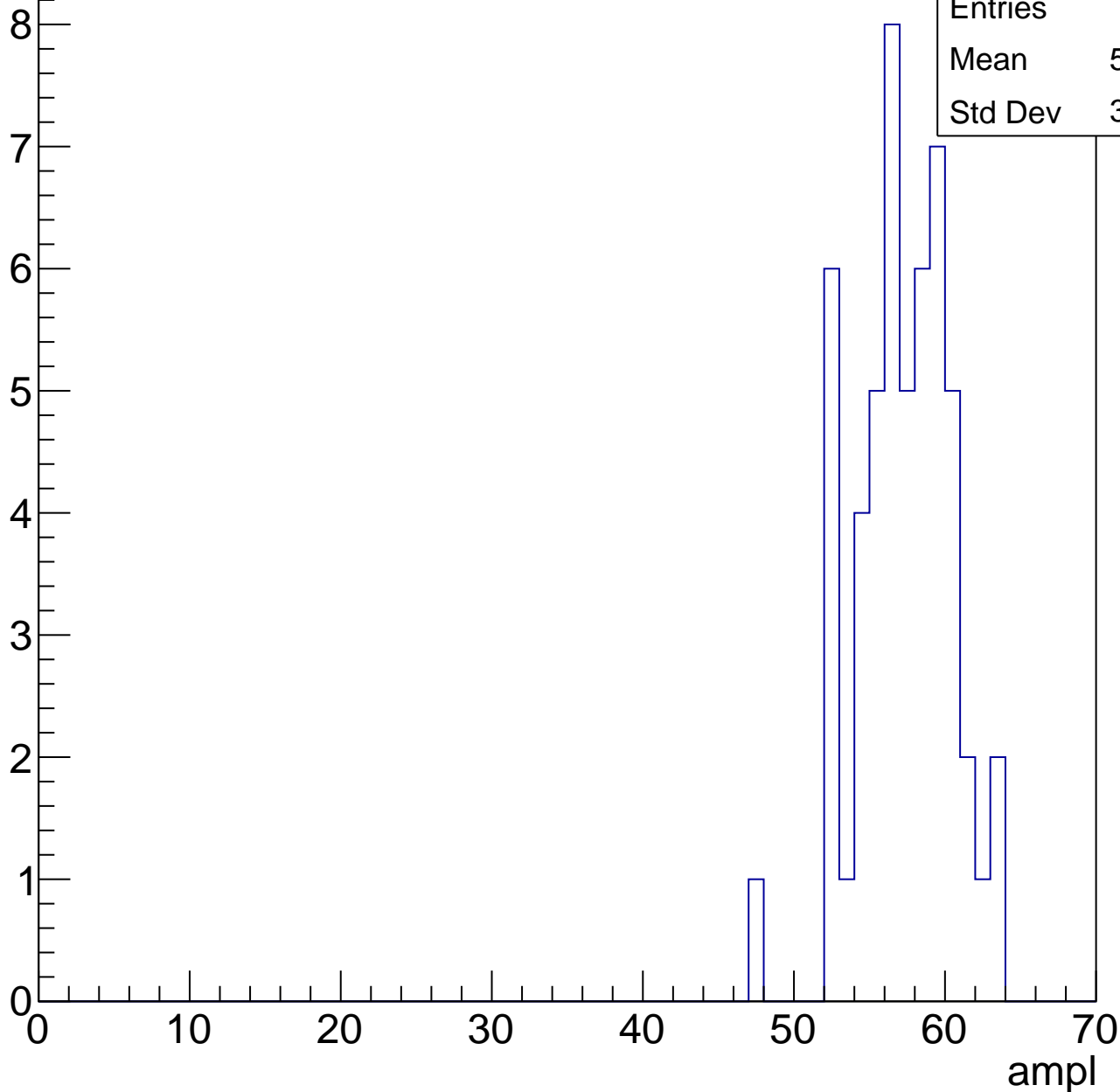


# B1L103S, U26-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	56.74
Std Dev	3.175

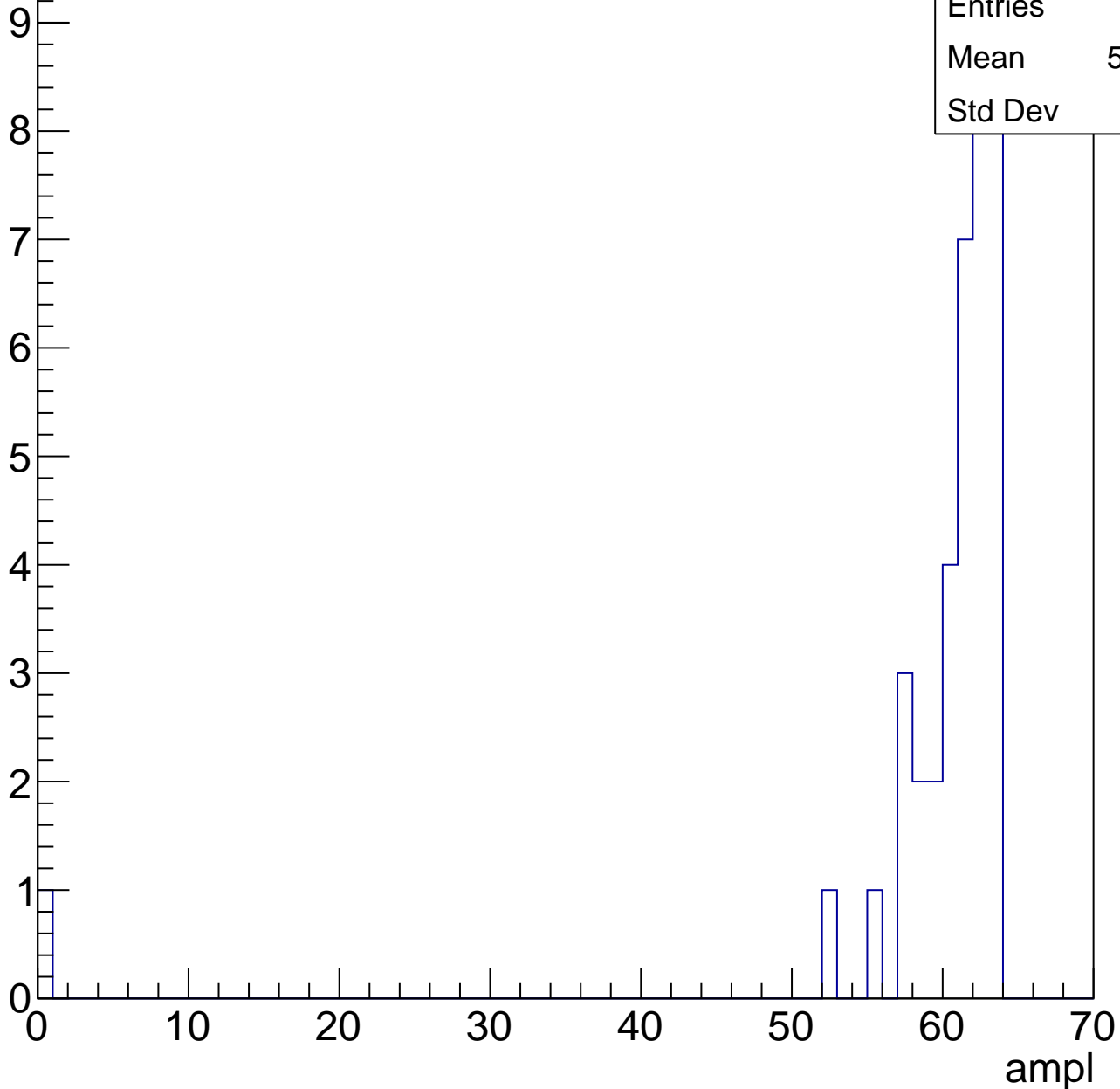


# B1L103S, U26-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	38
Mean	58.97
Std Dev	10



# B1L103S, U26-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries	3
Mean	59.67
Std Dev	1.247



# B1L103S, U26-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch29, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	83
Mean	26.39
Std Dev	5.488

**Gaus mean : 27.3890**

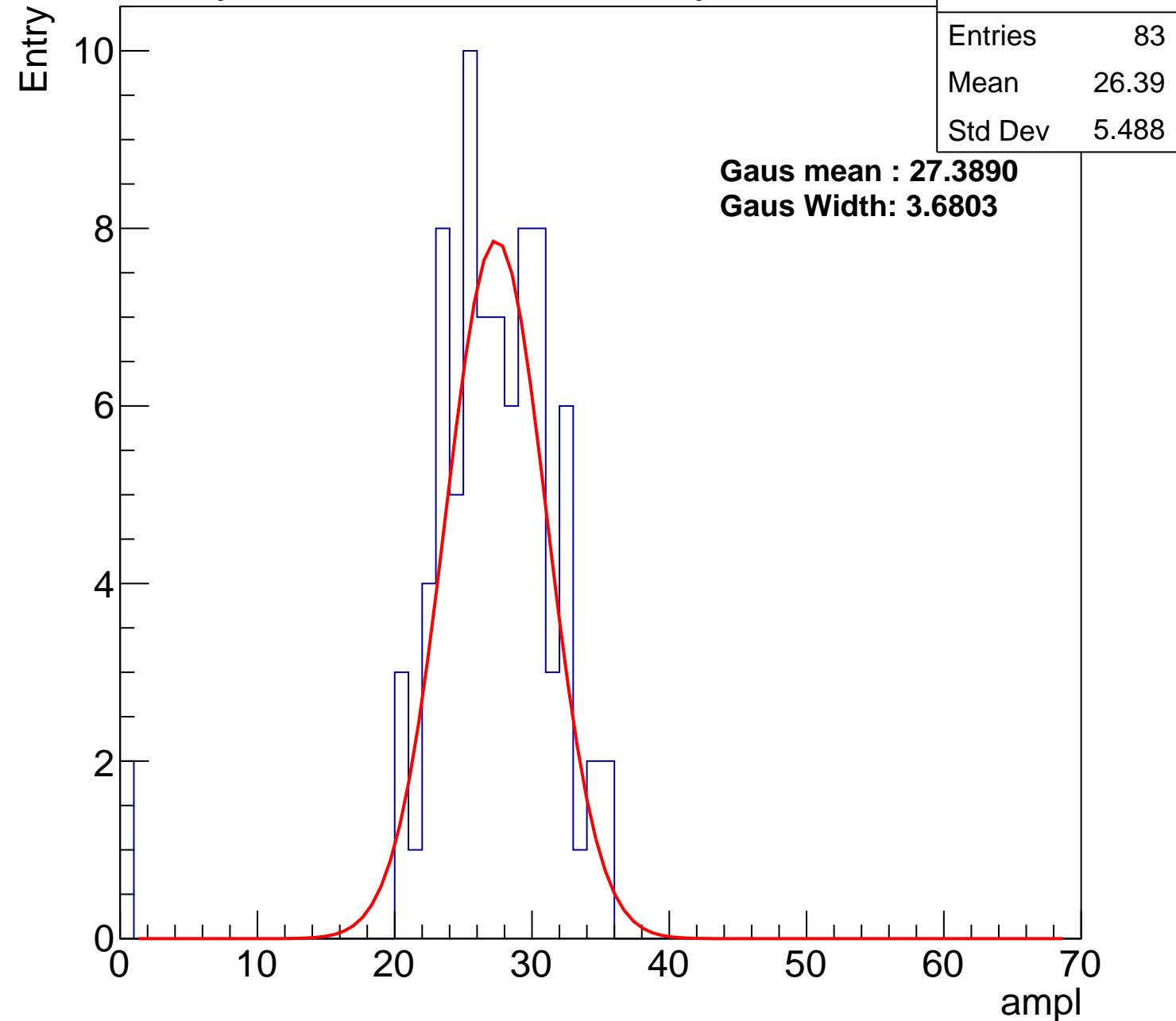
**Gaus Width: 3.6803**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch29, adc1

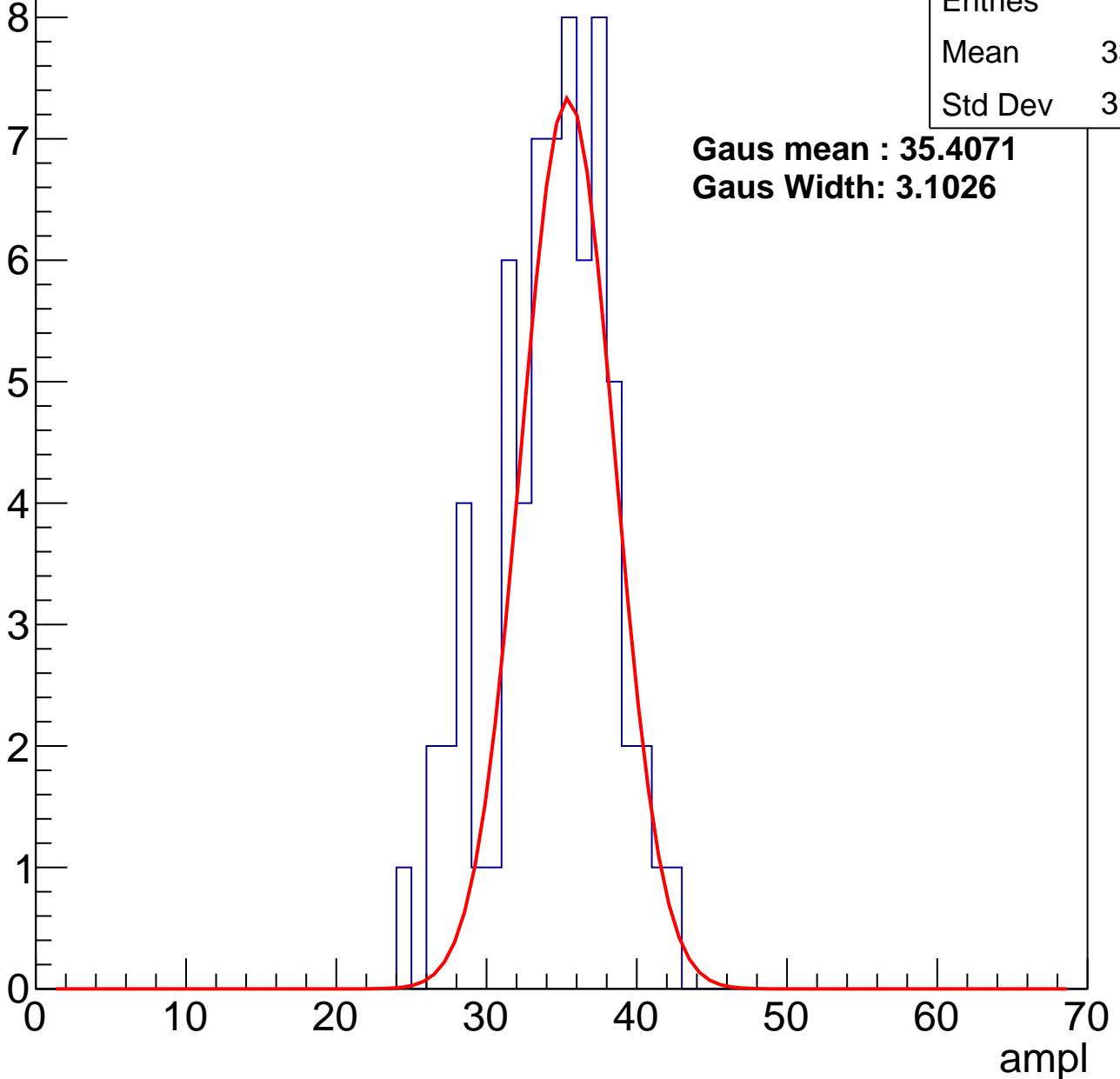
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	33.93
Std Dev	3.848

**Gaus mean : 35.4071**

**Gaus Width: 3.1026**



# B1L103S, U26-ch29, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	40.97
Std Dev	3.516

**Gaus mean : 41.8433**

**Gaus Width: 3.6501**

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

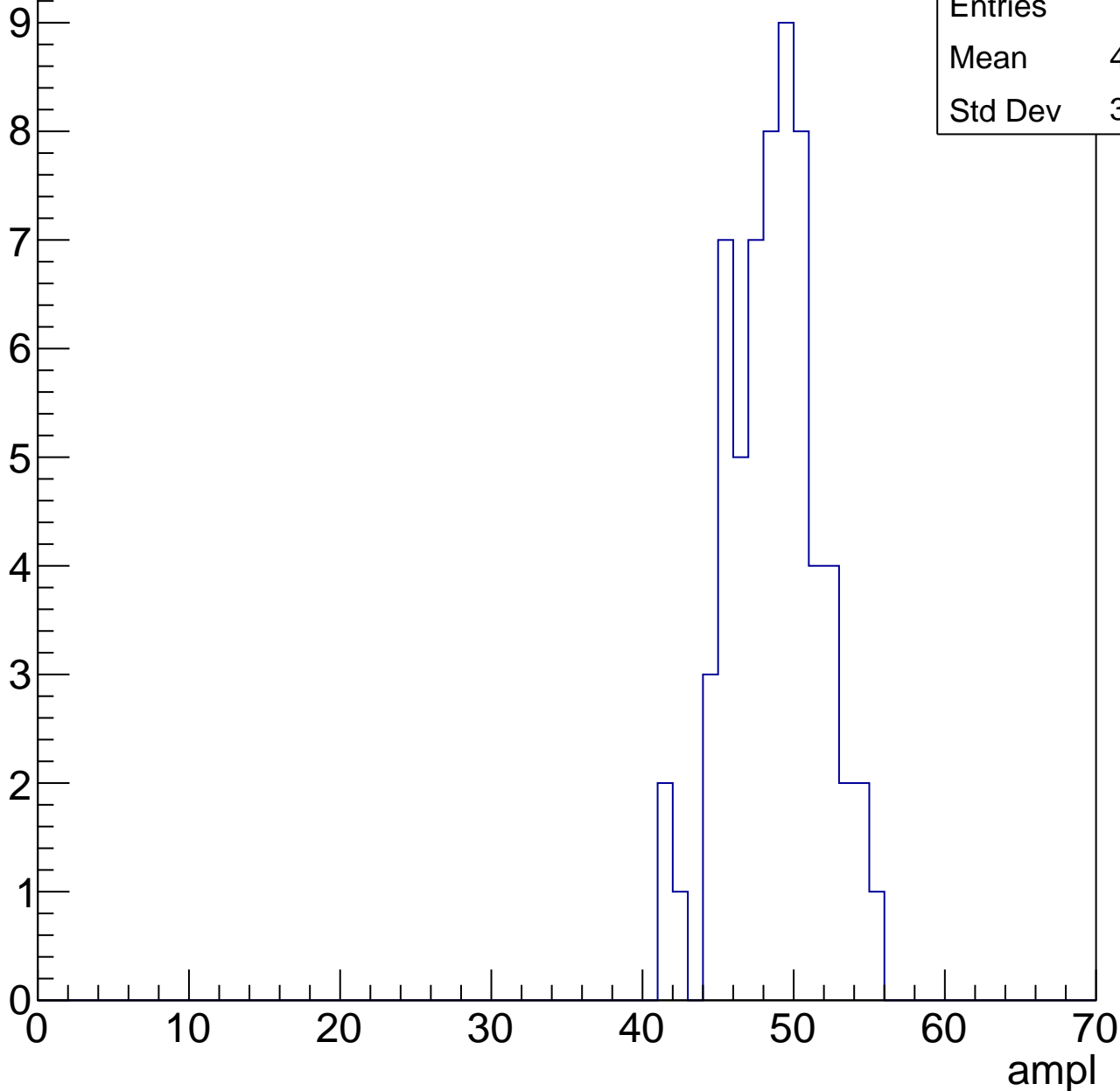


# B1L103S, U26-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	48.19
Std Dev	3.039

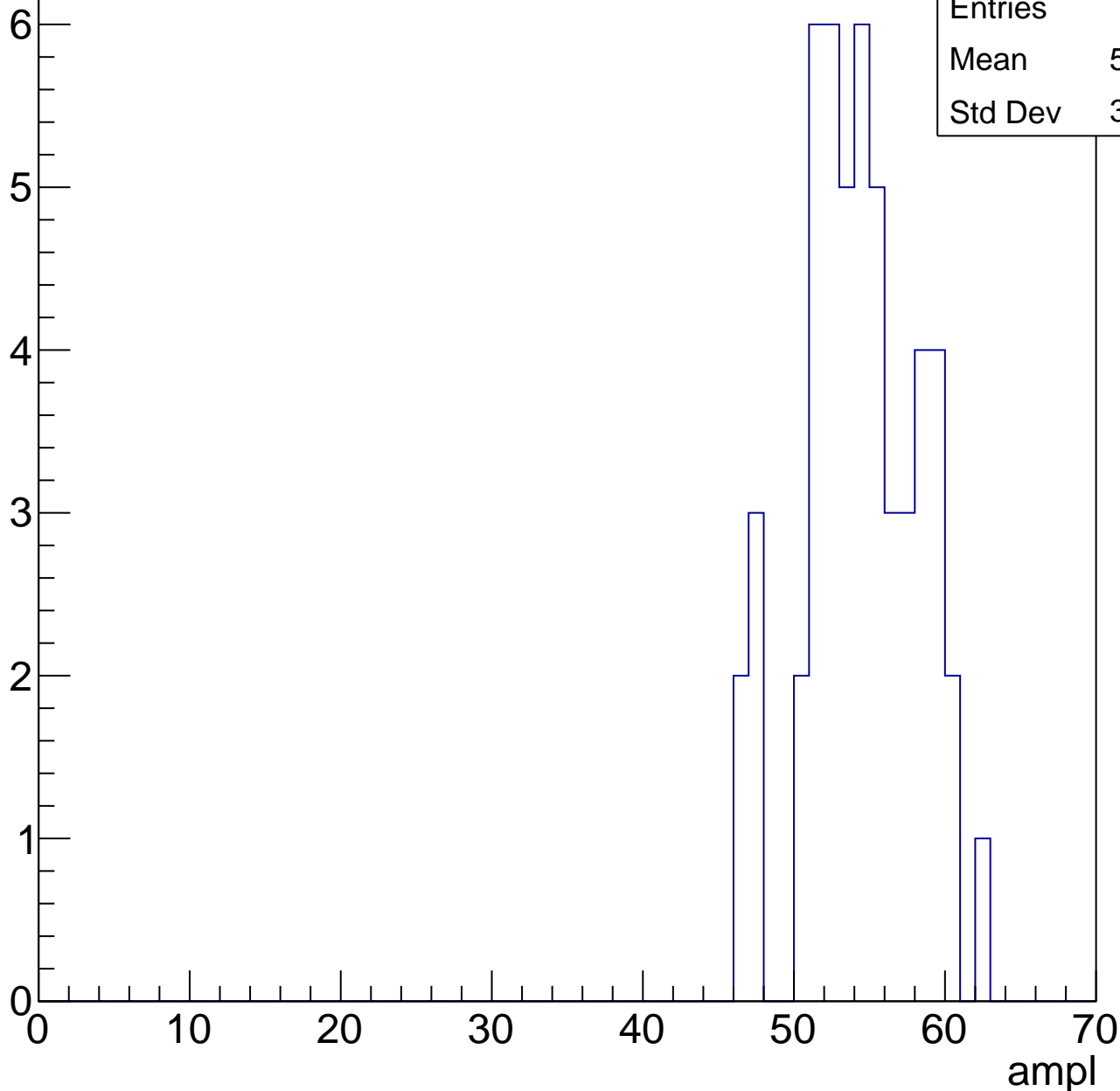


# B1L103S, U26-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	53.92
Std Dev	3.756

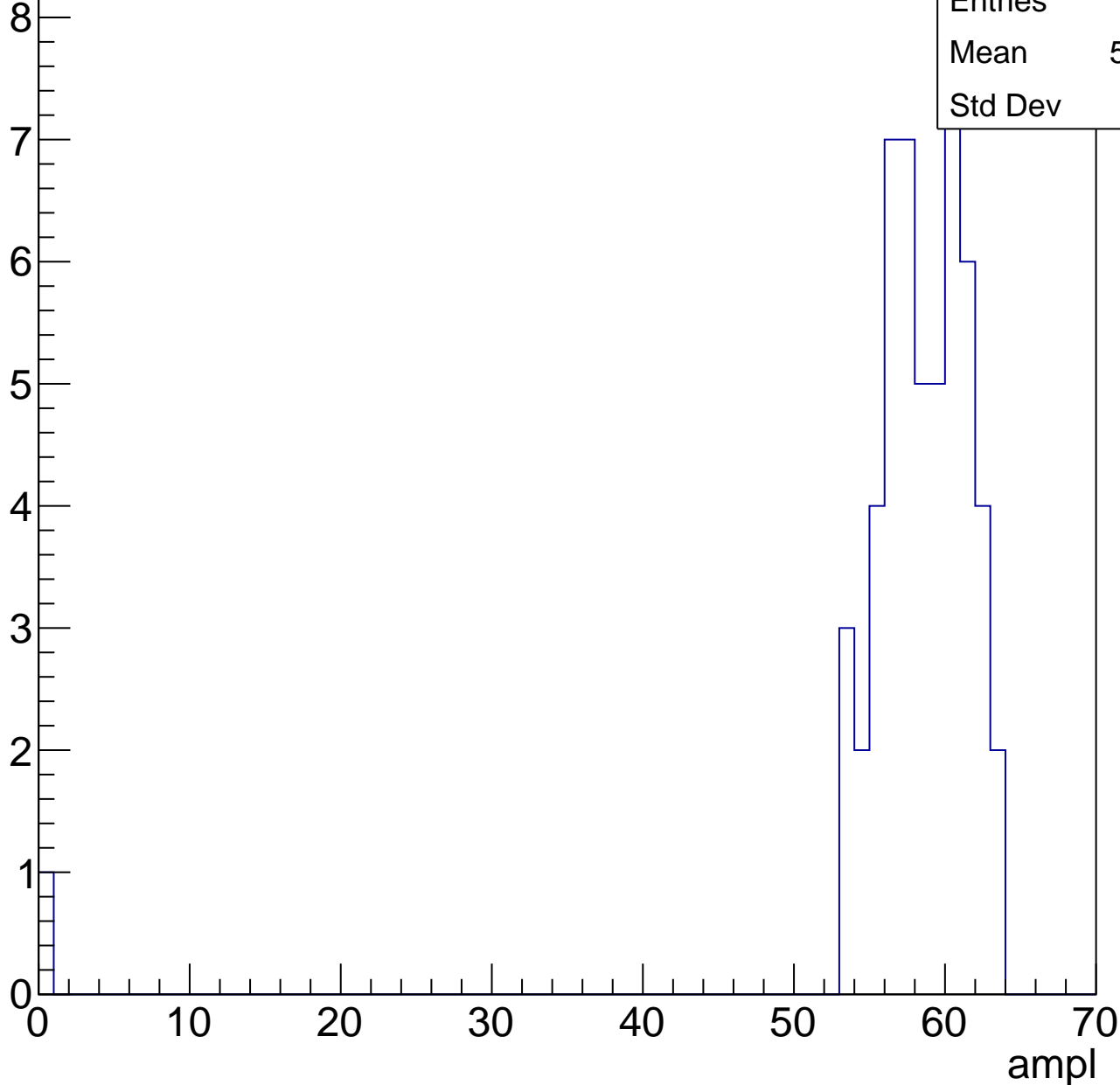


# B1L103S, U26-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	57.09
Std Dev	8.28

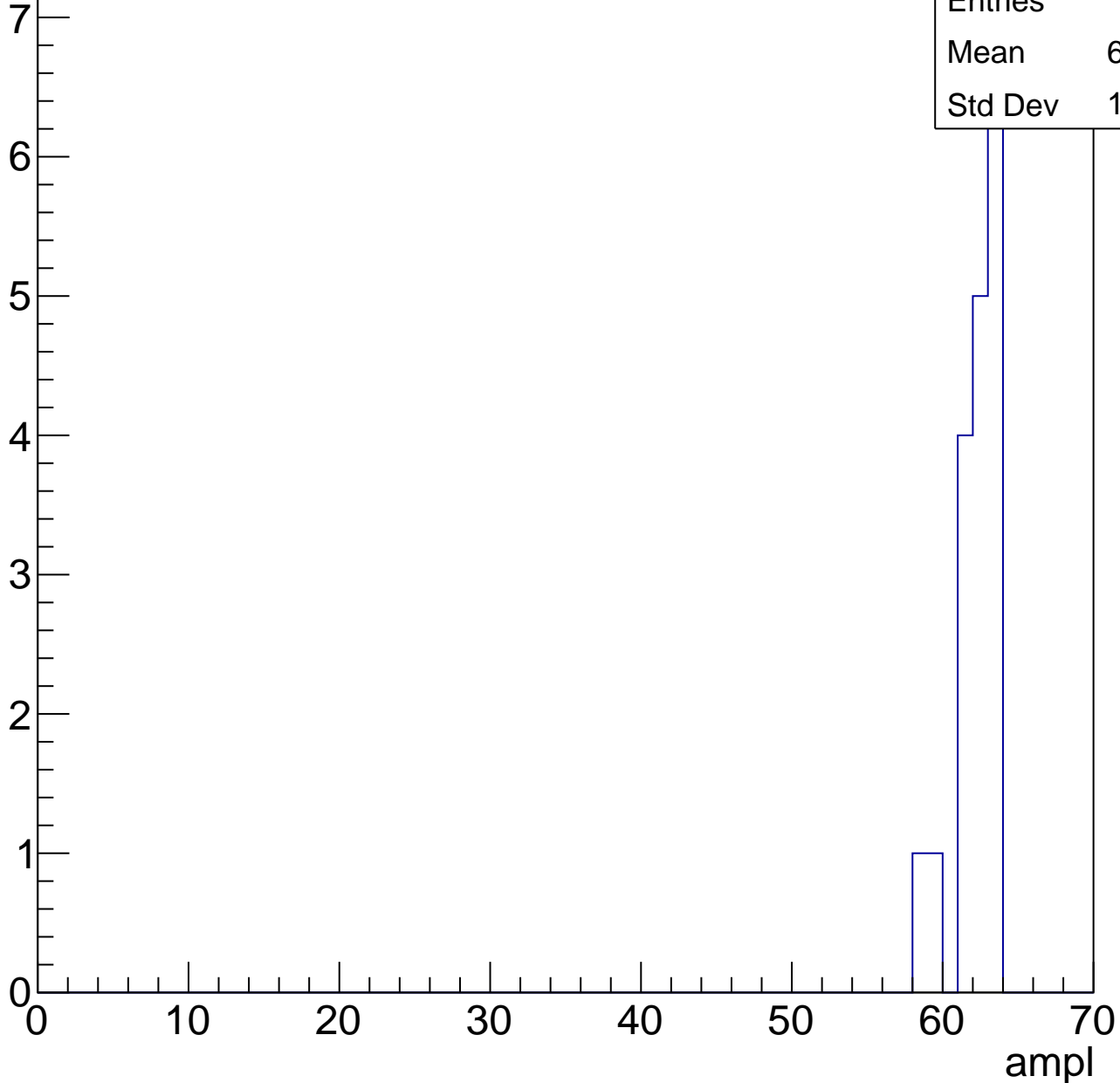


# B1L103S, U26-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	18
Mean	61.78
Std Dev	1.397

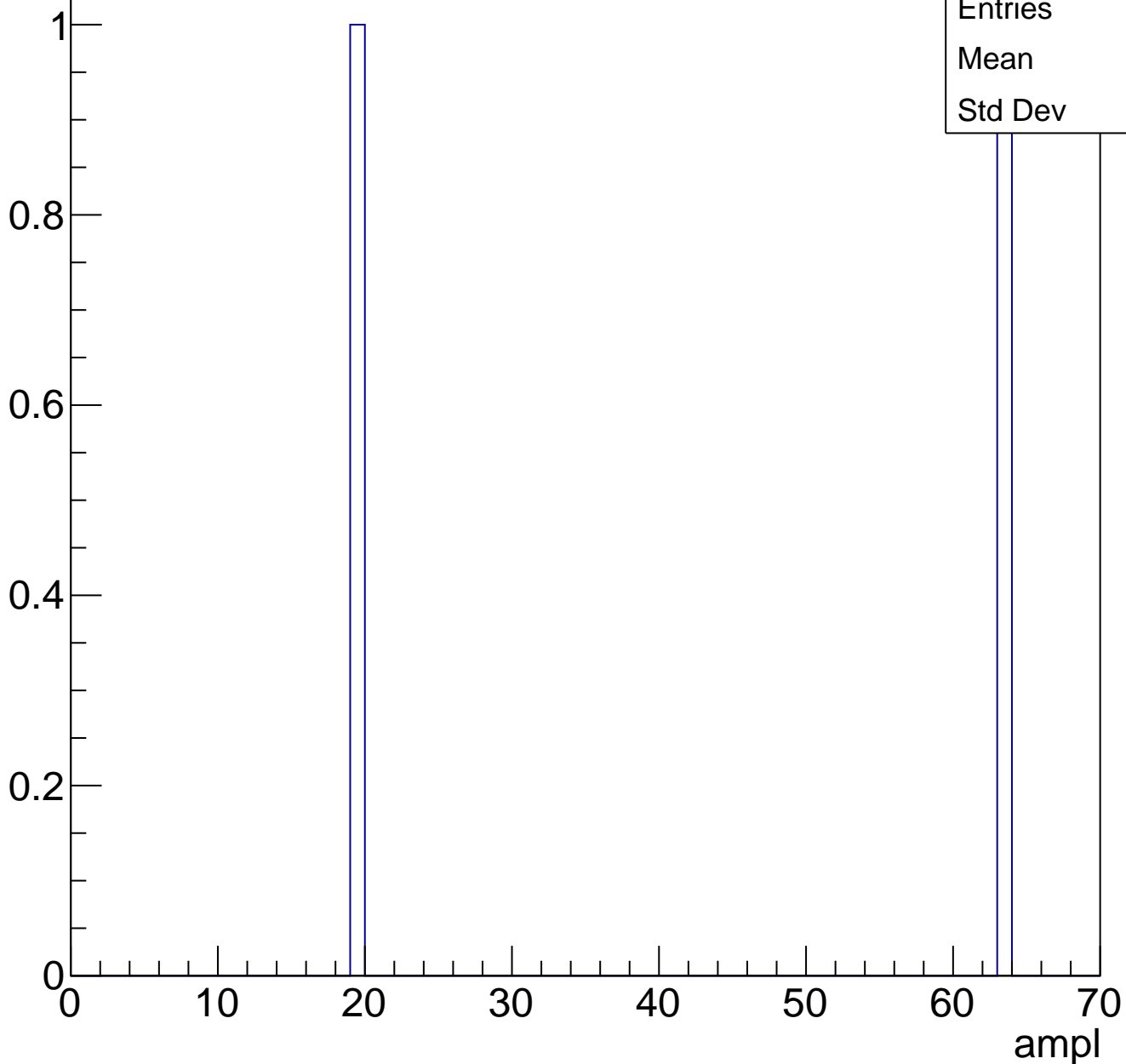




# B1L103S, U26-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch30, adc0

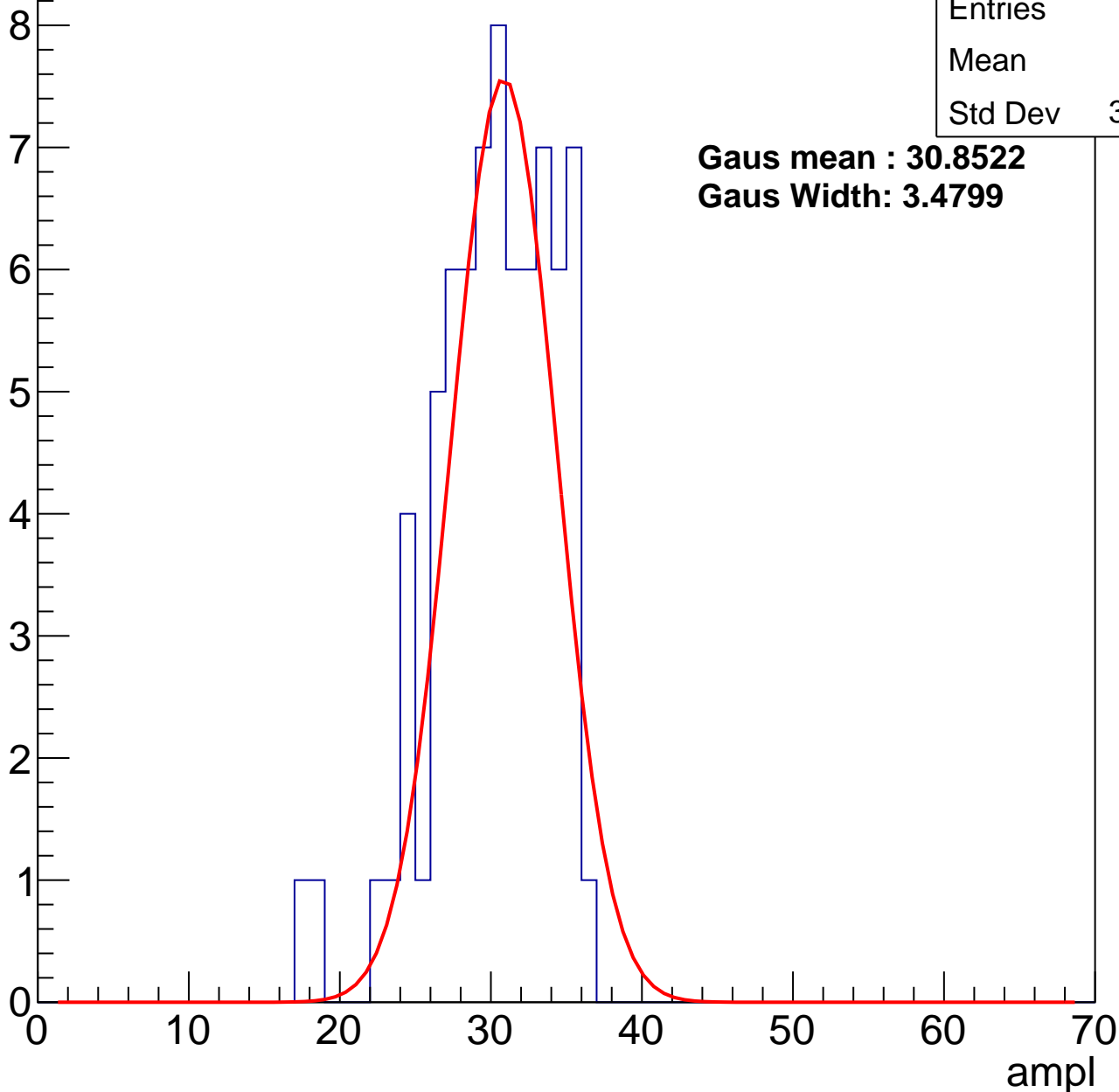
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	29.7
Std Dev	3.948

**Gaus mean : 30.8522**

**Gaus Width: 3.4799**



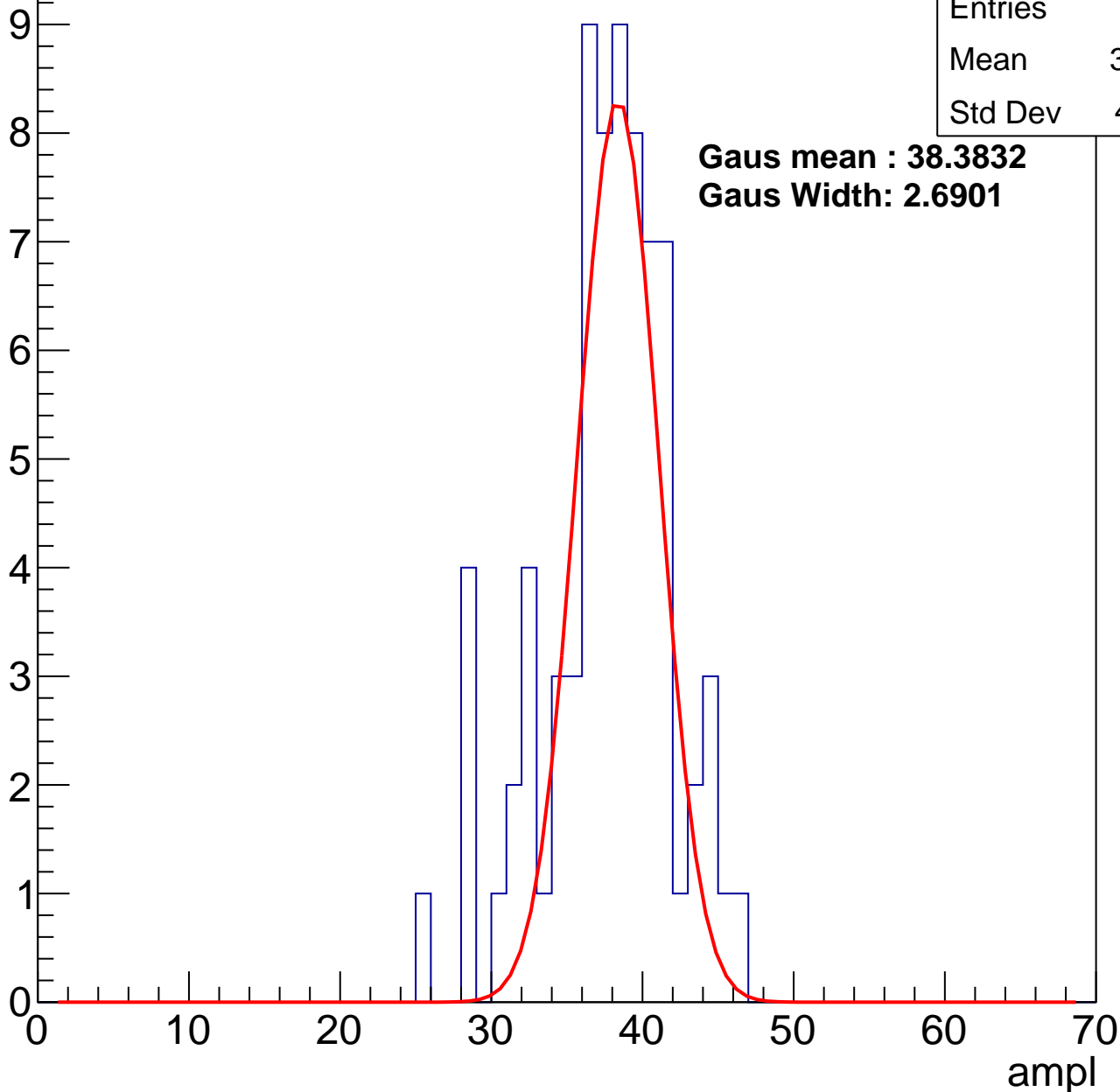
# B1L103S, U26-ch30, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	37.19
Std Dev	4.251

**Gaus mean : 38.3832**  
**Gaus Width: 2.6901**



# B1L103S, U26-ch30, adc2

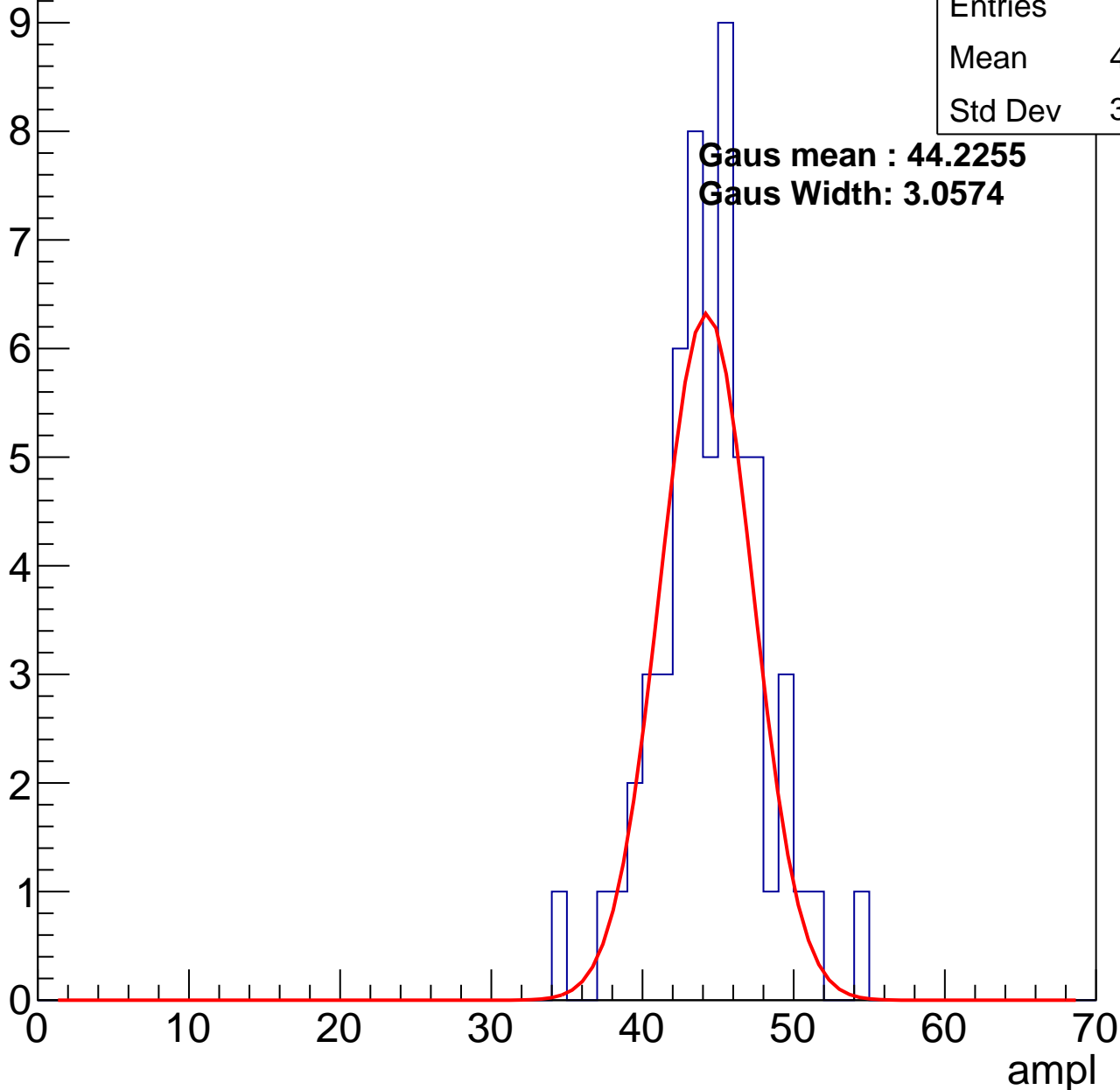
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	44.04
Std Dev	3.515

**Gaus mean : 44.2255**

**Gaus Width: 3.0574**

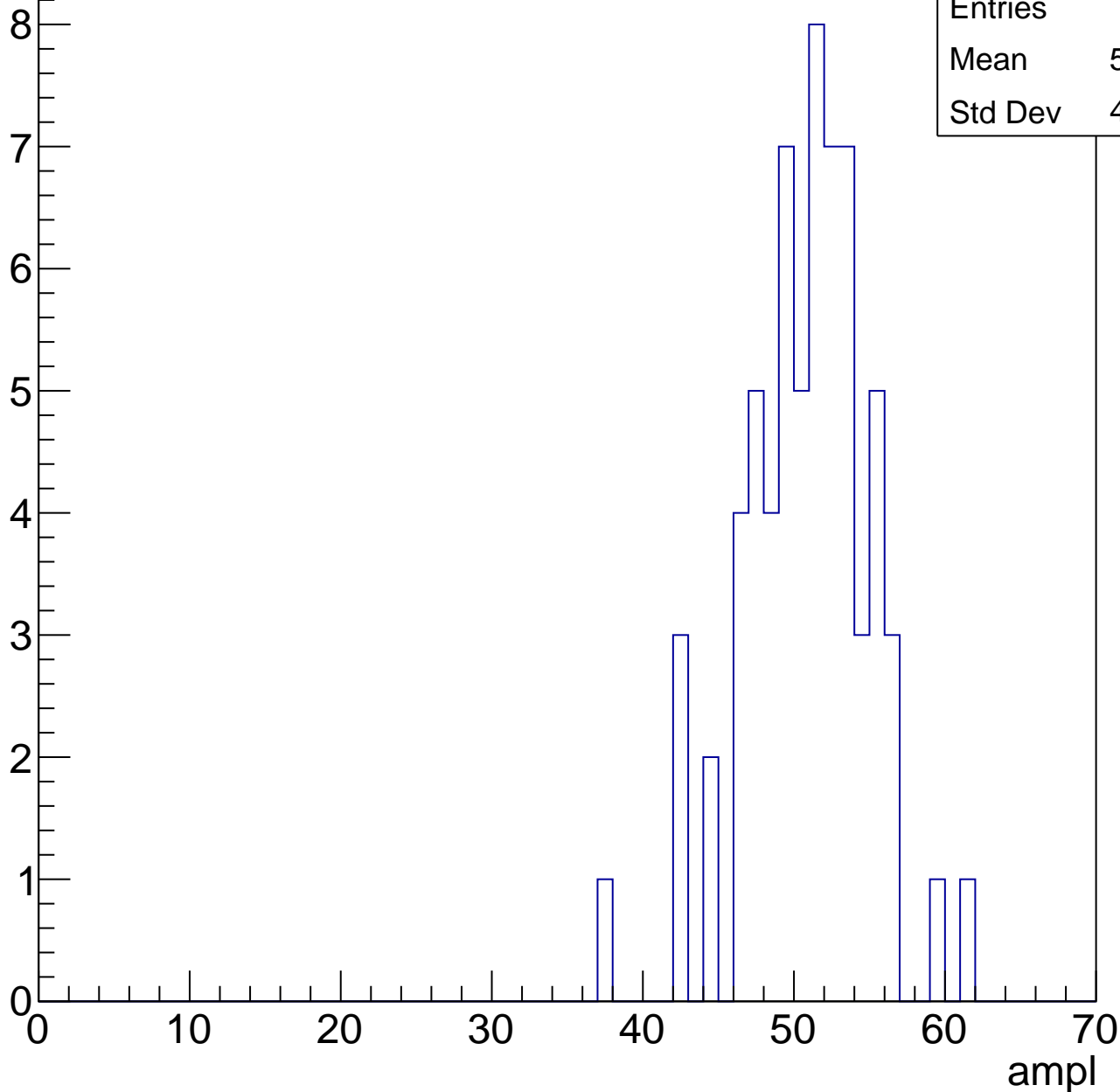


# B1L103S, U26-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	50.35
Std Dev	4.154

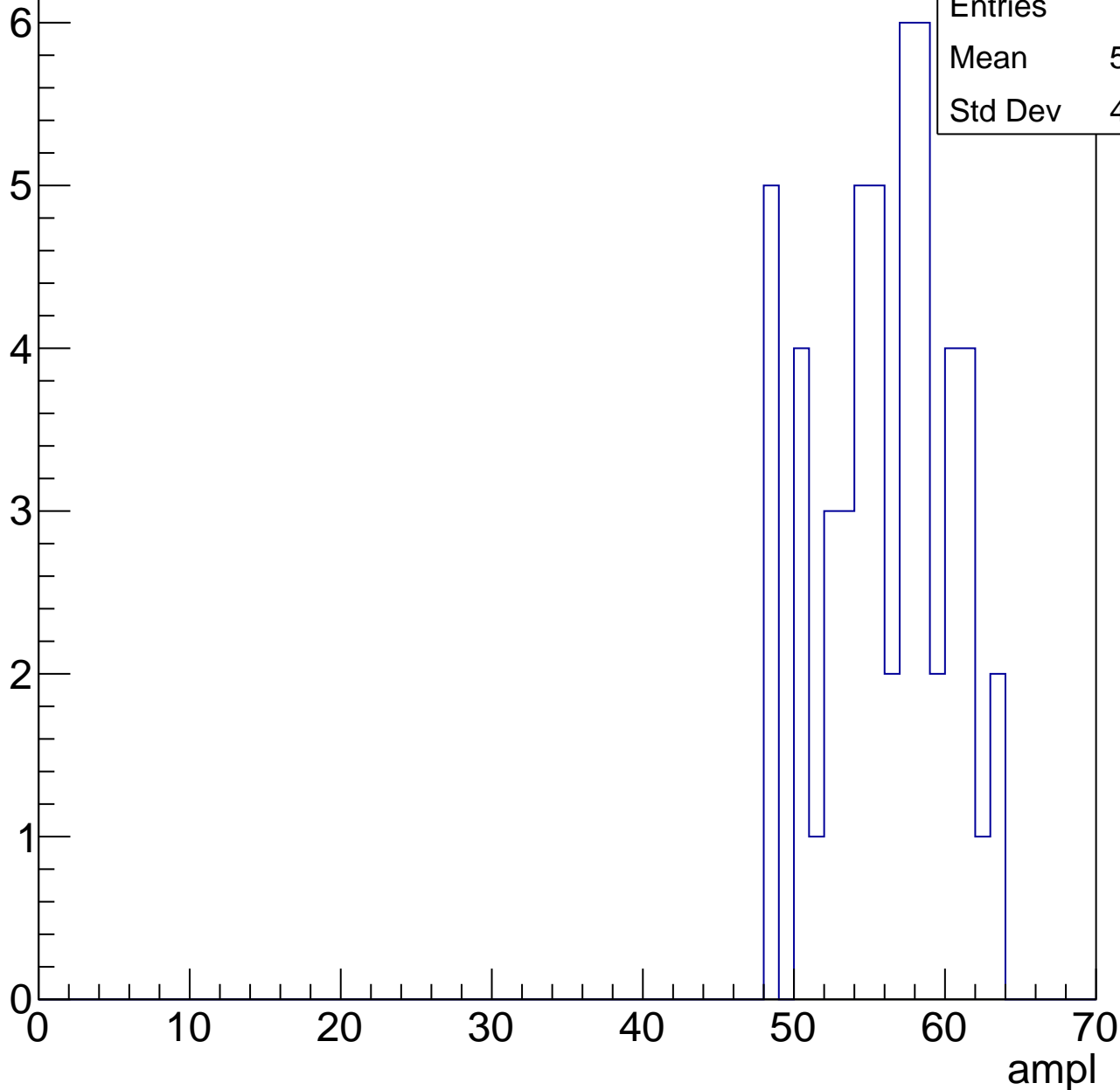


# B1L103S, U26-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	55.53
Std Dev	4.174

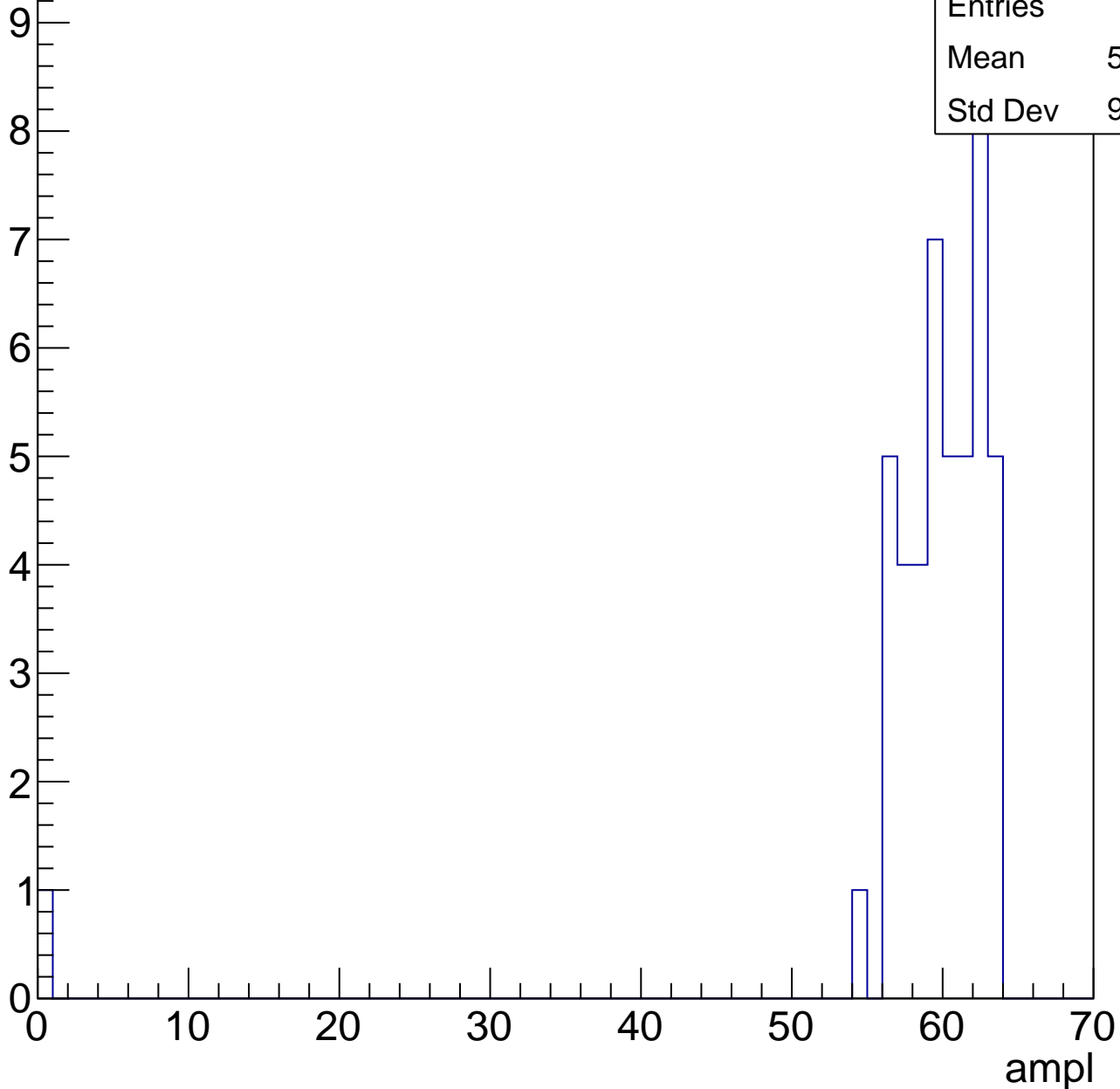


# B1L103S, U26-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	58.37
Std Dev	9.015



# B1L103S, U26-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L103S, U26-ch31, adc0

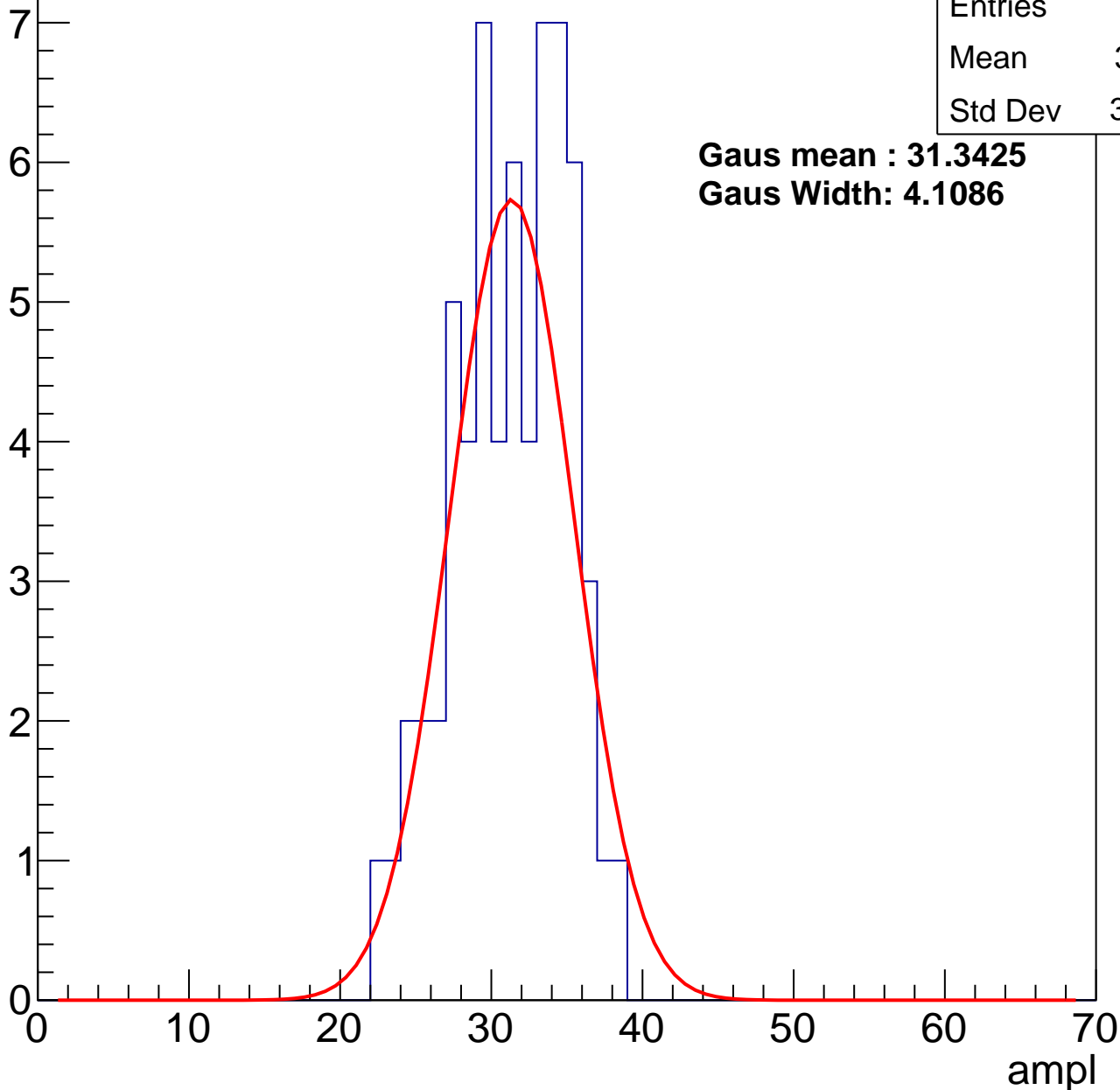
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	30.81
Std Dev	3.698

**Gaus mean : 31.3425**

**Gaus Width: 4.1086**



# B1L103S, U26-ch31, adc1

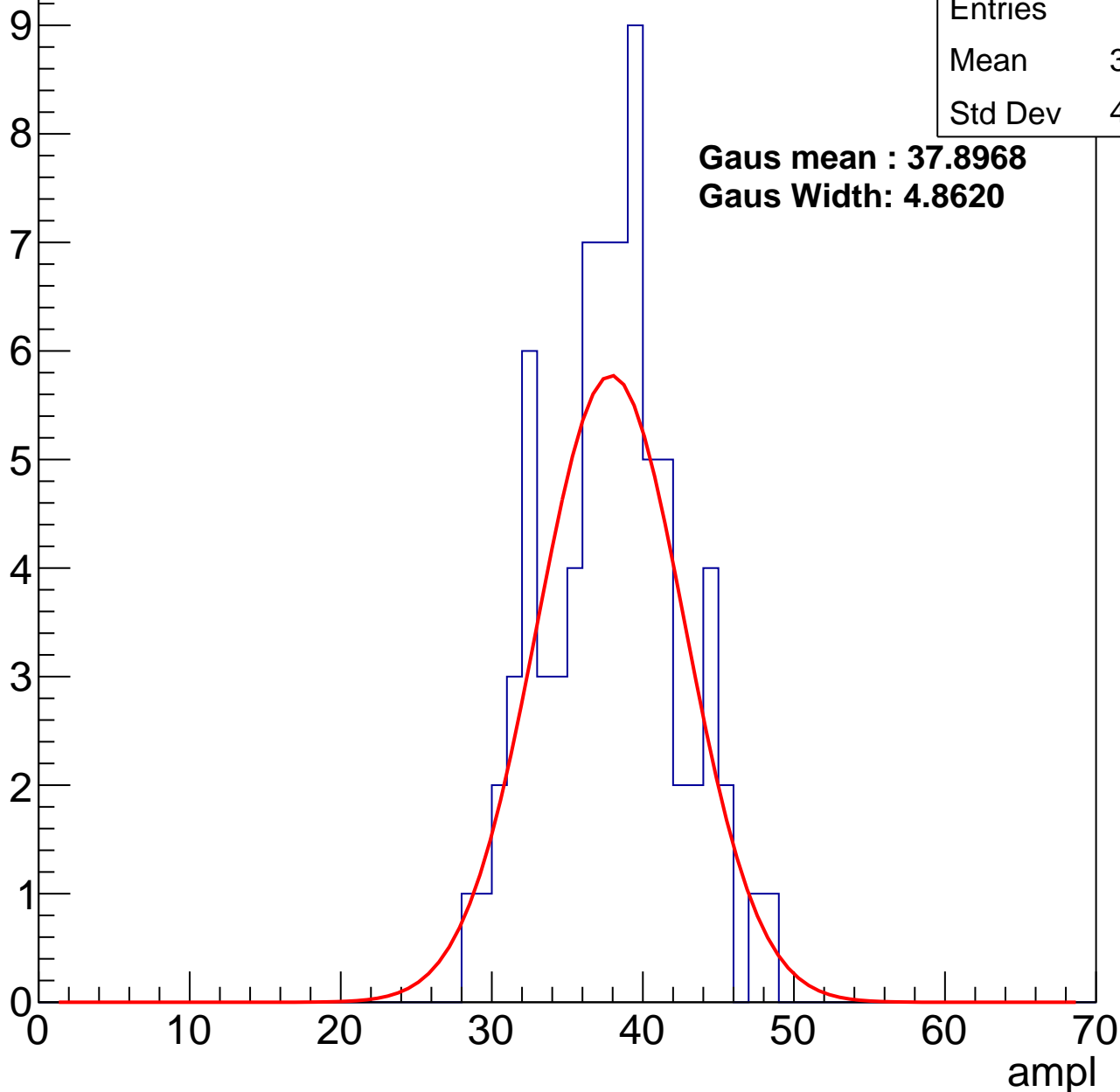
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	37.43
Std Dev	4.352

**Gaus mean : 37.8968**

**Gaus Width: 4.8620**



# B1L103S, U26-ch31, adc2

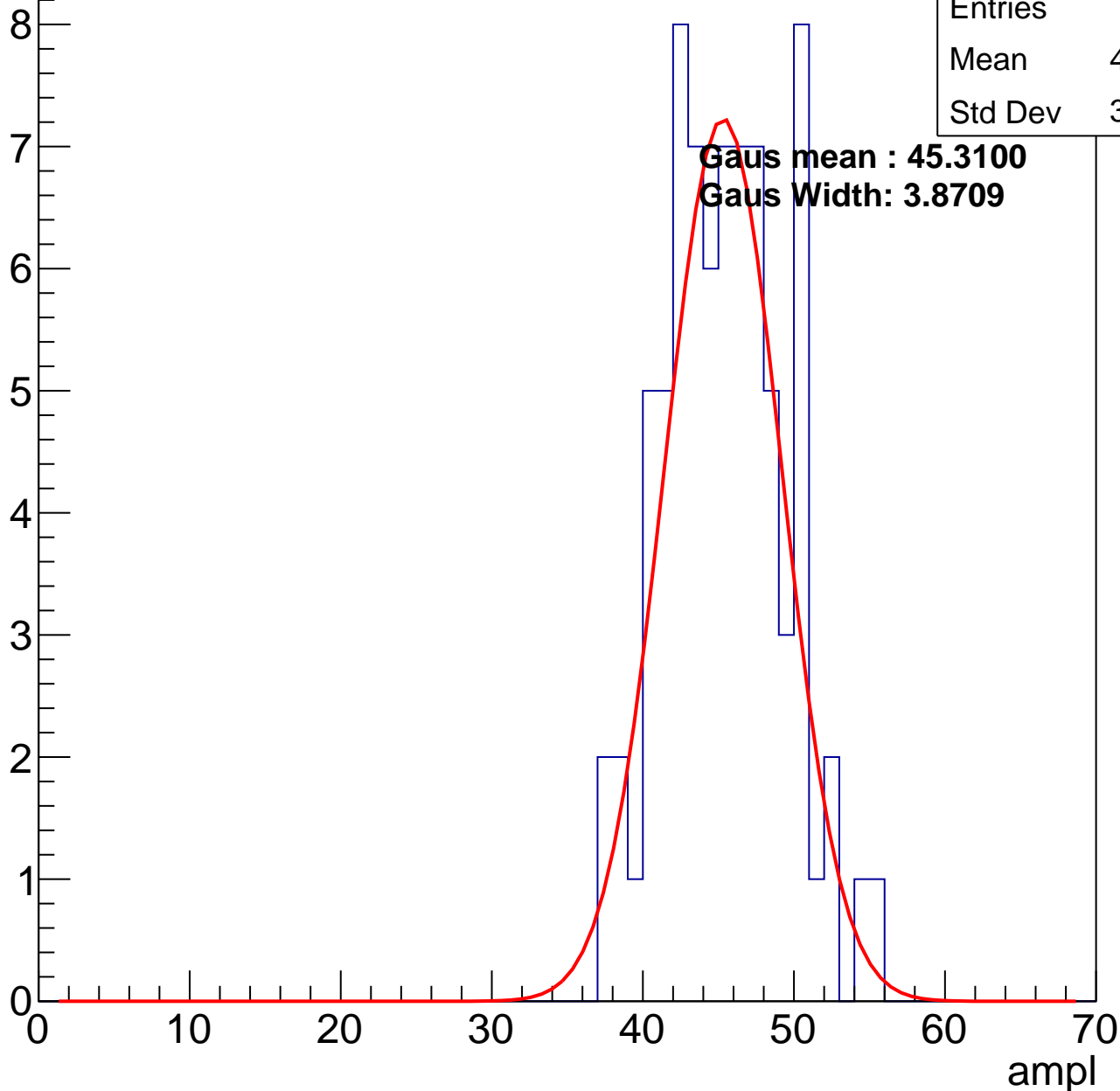
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	45.03
Std Dev	3.948

**Gaus mean : 45.3100**

**Gaus Width: 3.8709**

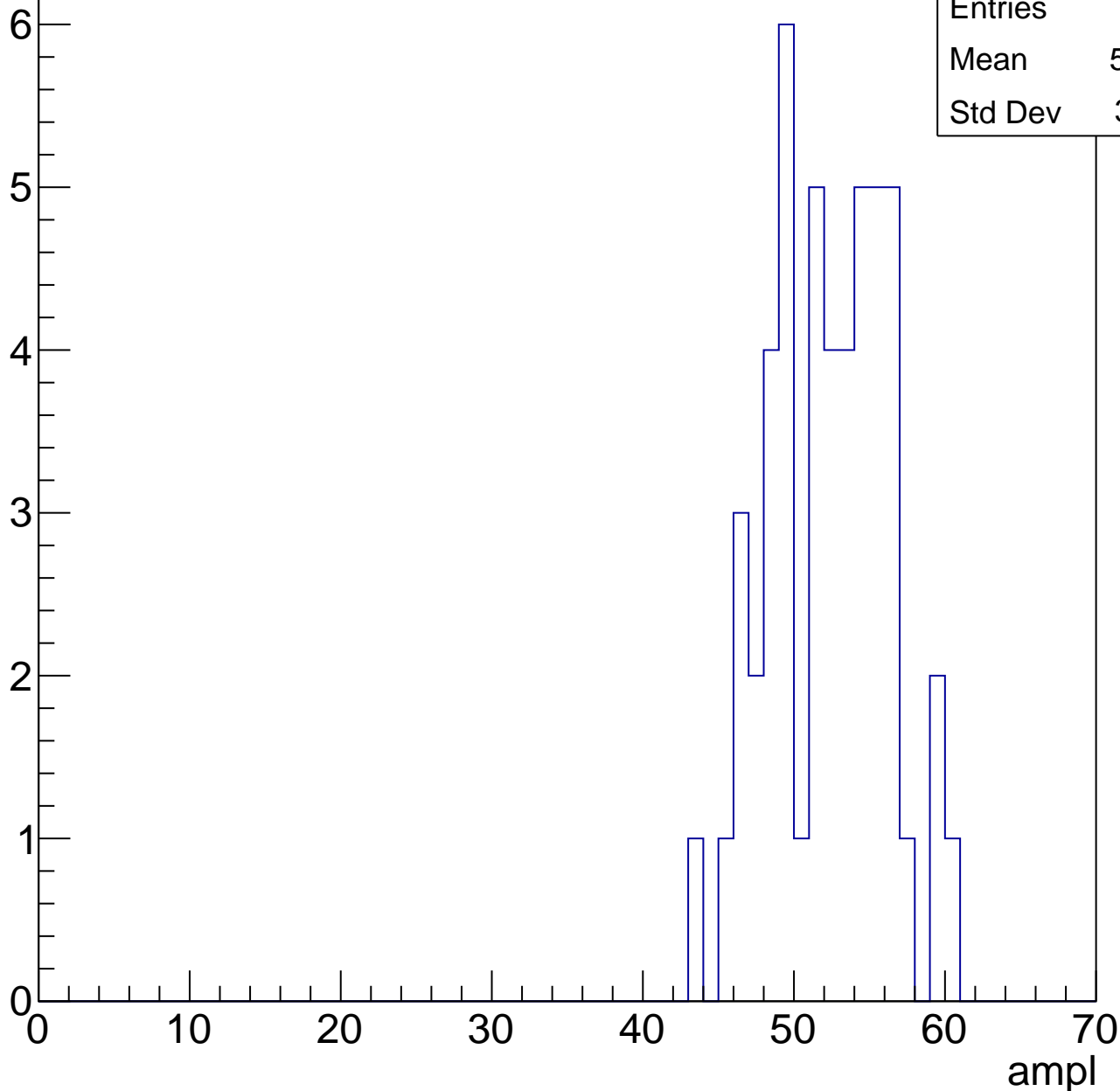


# B1L103S, U26-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	51.82
Std Dev	3.871

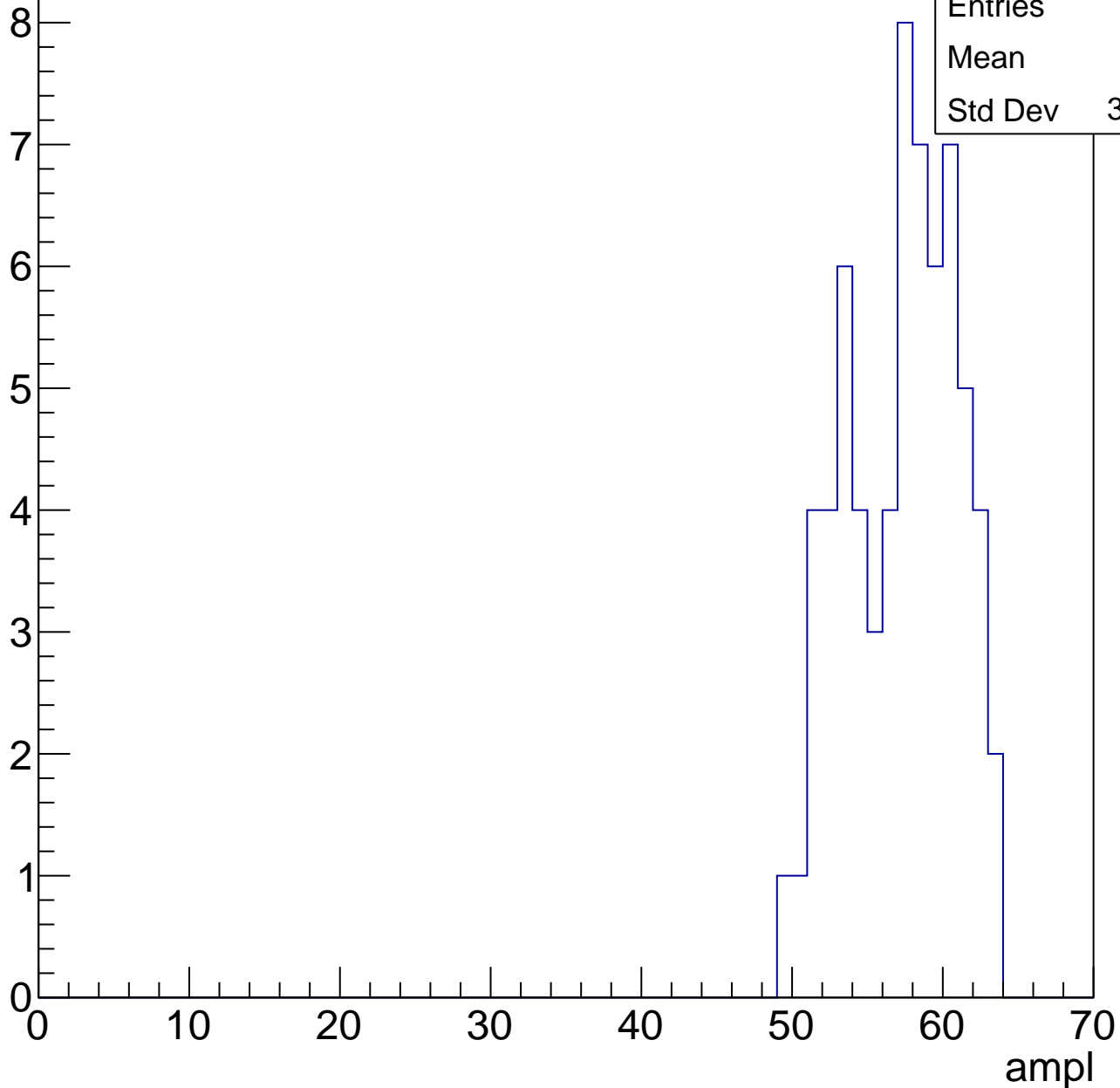


# B1L103S, U26-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	56.8
Std Dev	3.585

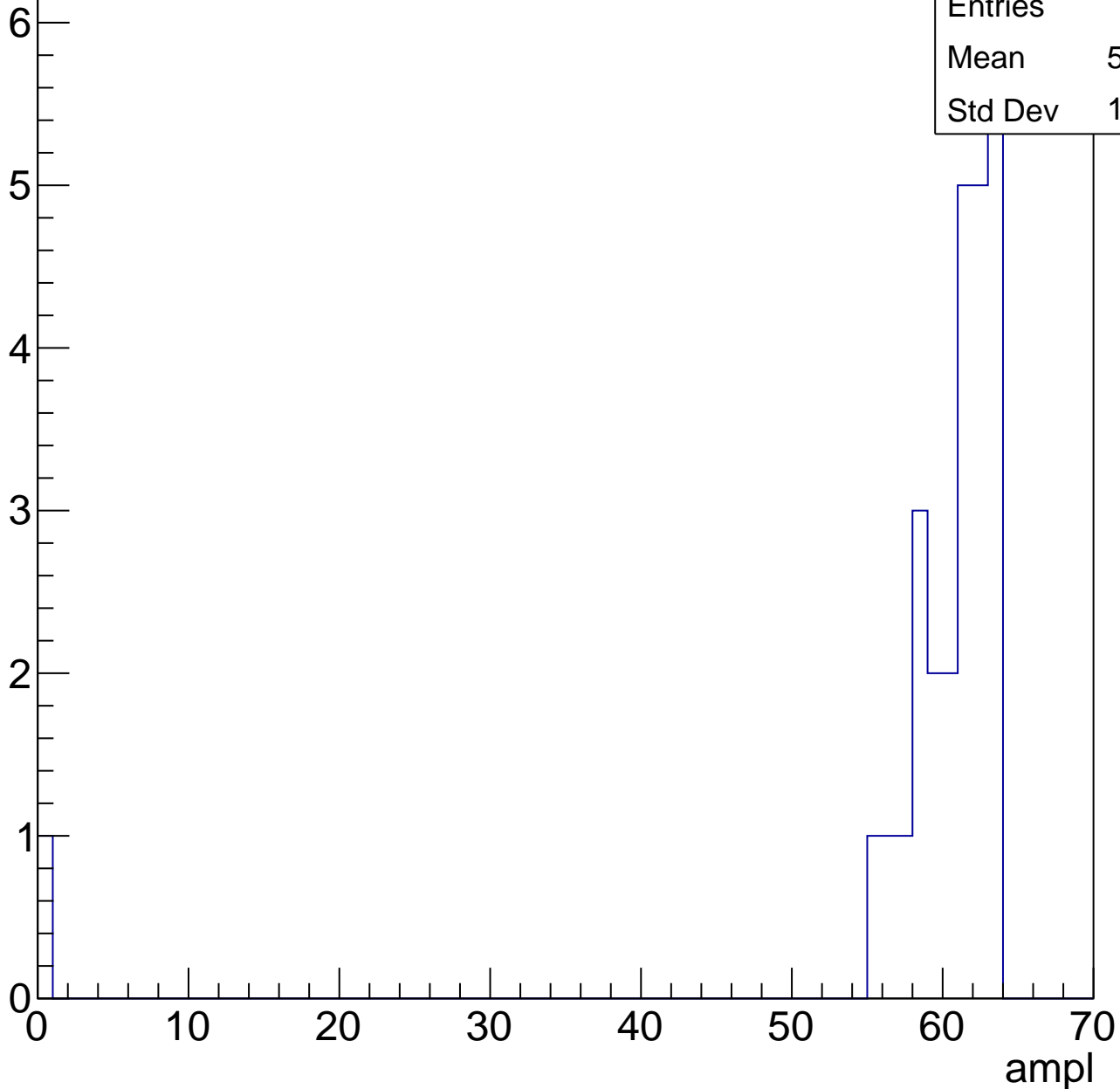


# B1L103S, U26-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	27
Mean	58.26
Std Dev	11.64



# B1L103S, U26-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U26-ch32, adc0

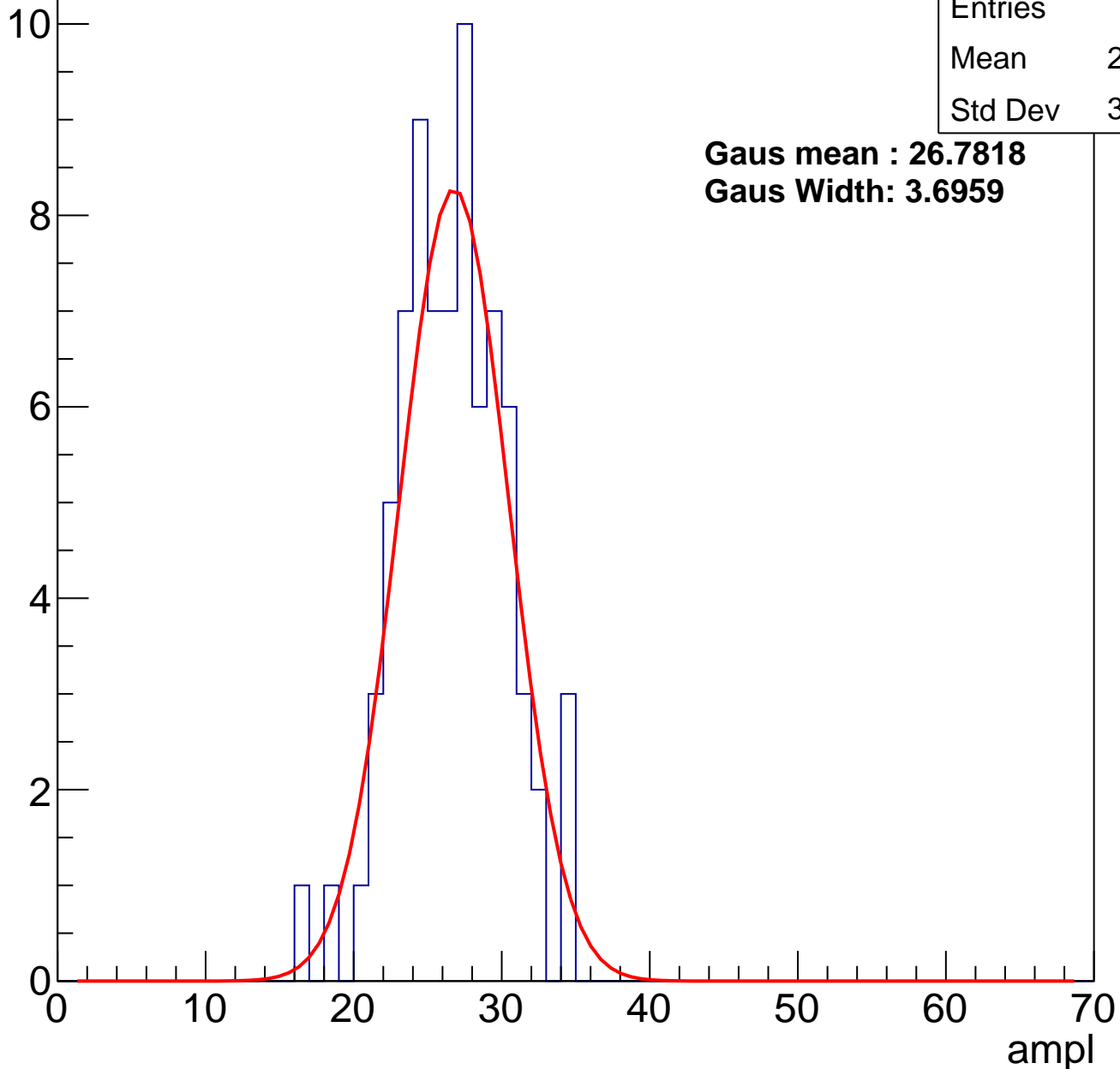
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	78
Mean	26.17
Std Dev	3.564

**Gaus mean : 26.7818**

**Gaus Width: 3.6959**

Entry



# B1L103S, U26-ch32, adc1

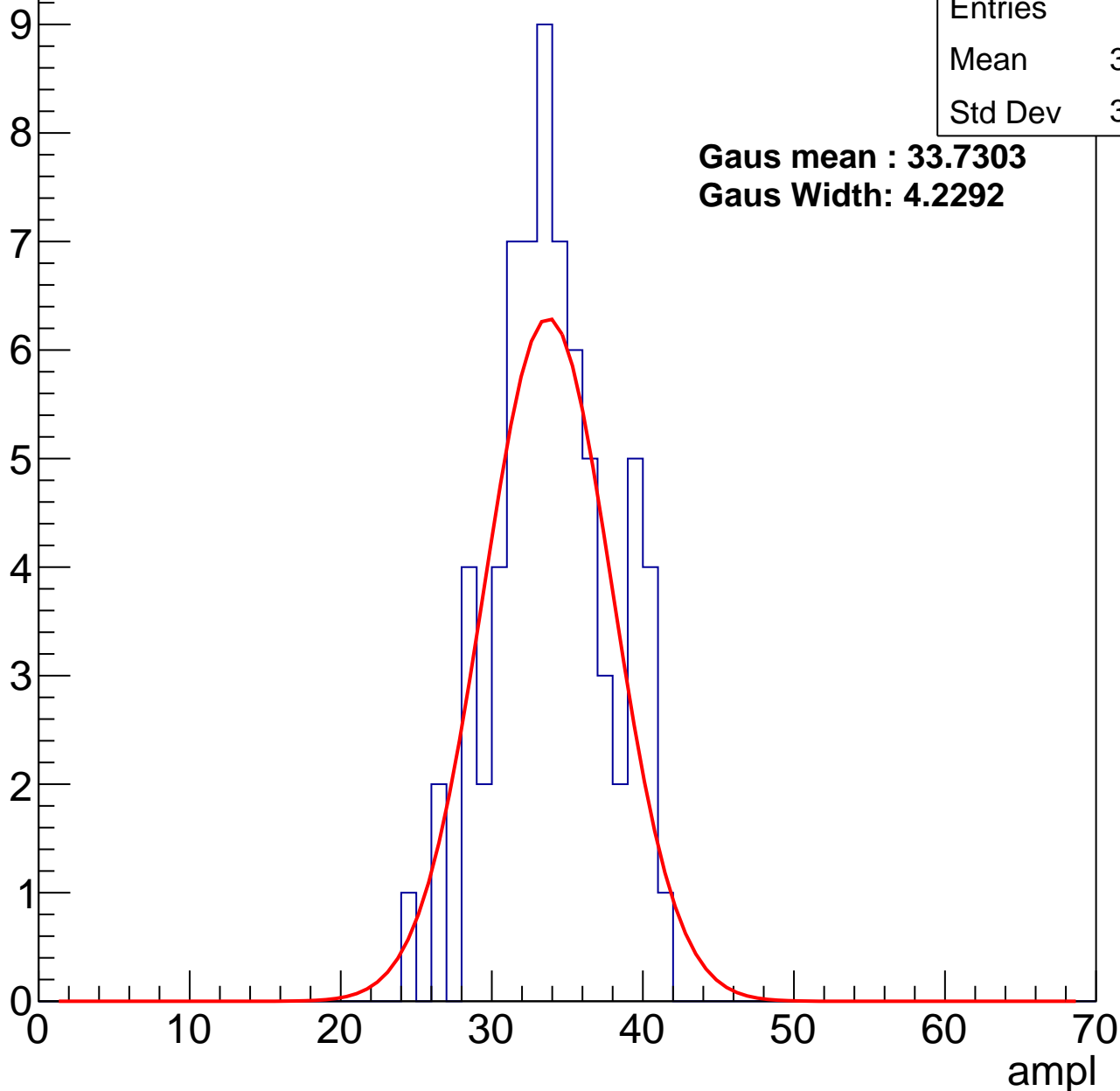
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	33.55
Std Dev	3.759

**Gaus mean : 33.7303**

**Gaus Width: 4.2292**



# B1L103S, U26-ch32, adc2

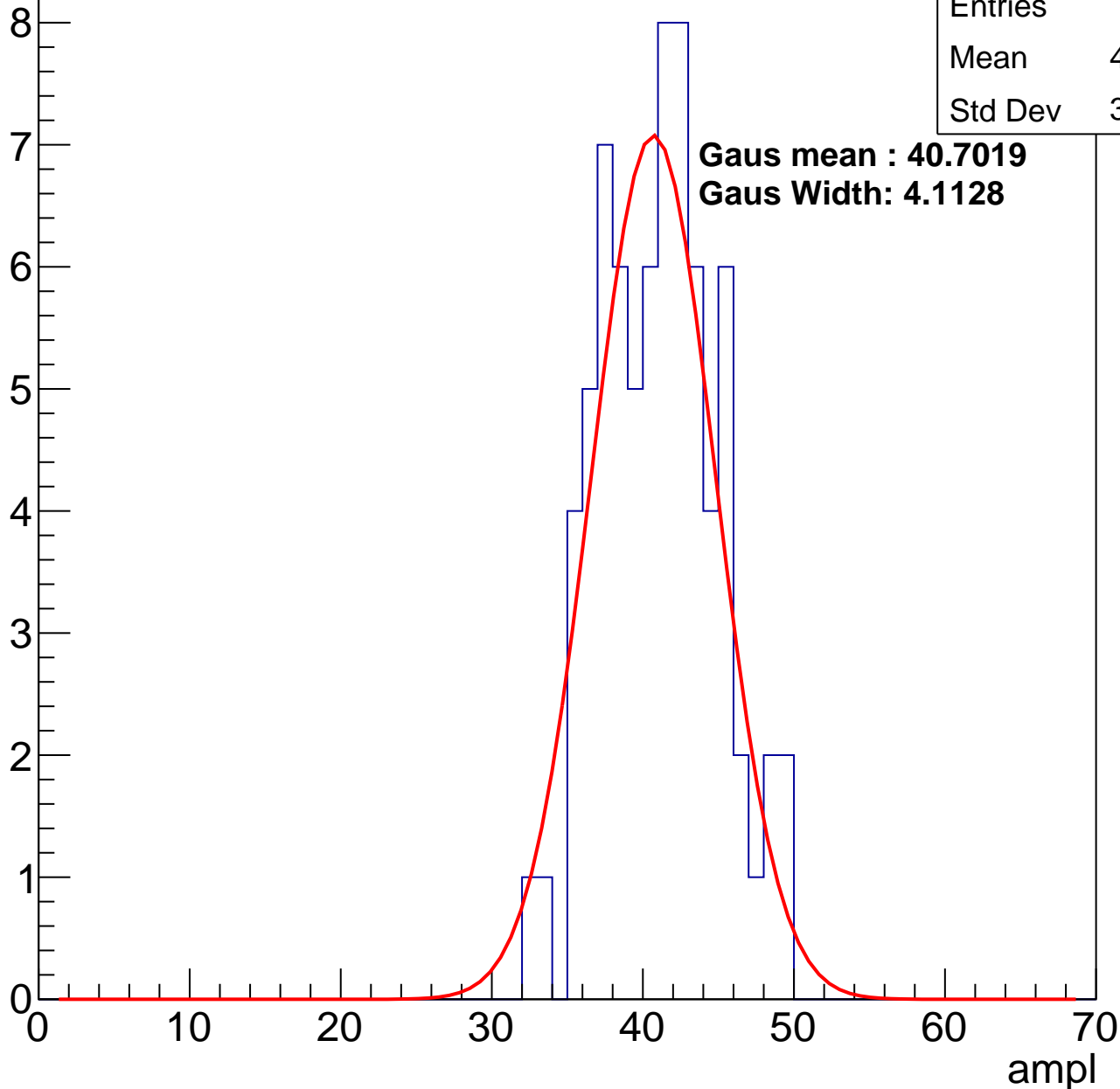
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	40.65
Std Dev	3.808

**Gaus mean : 40.7019**

**Gaus Width: 4.1128**

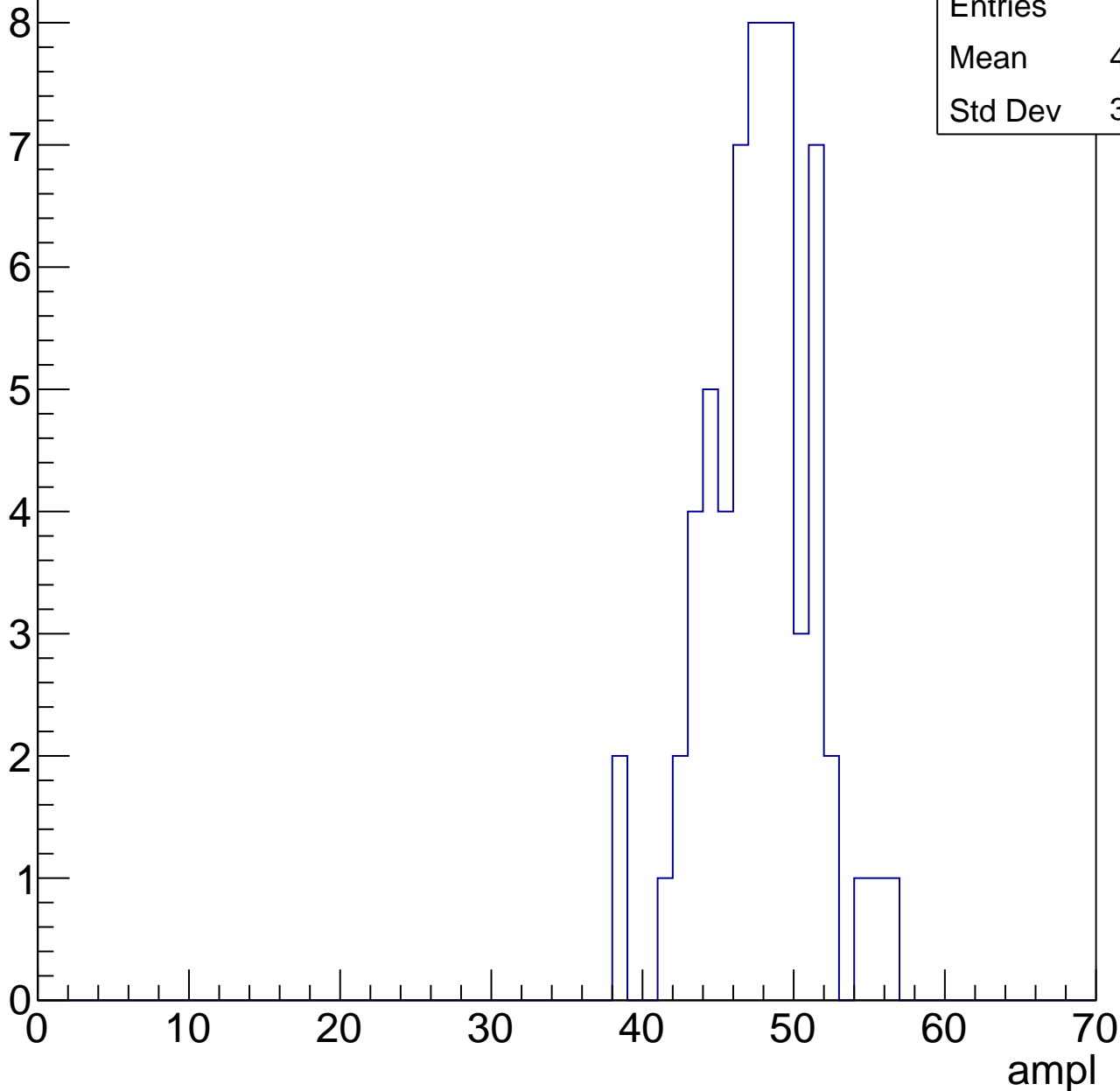


# B1L103S, U26-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

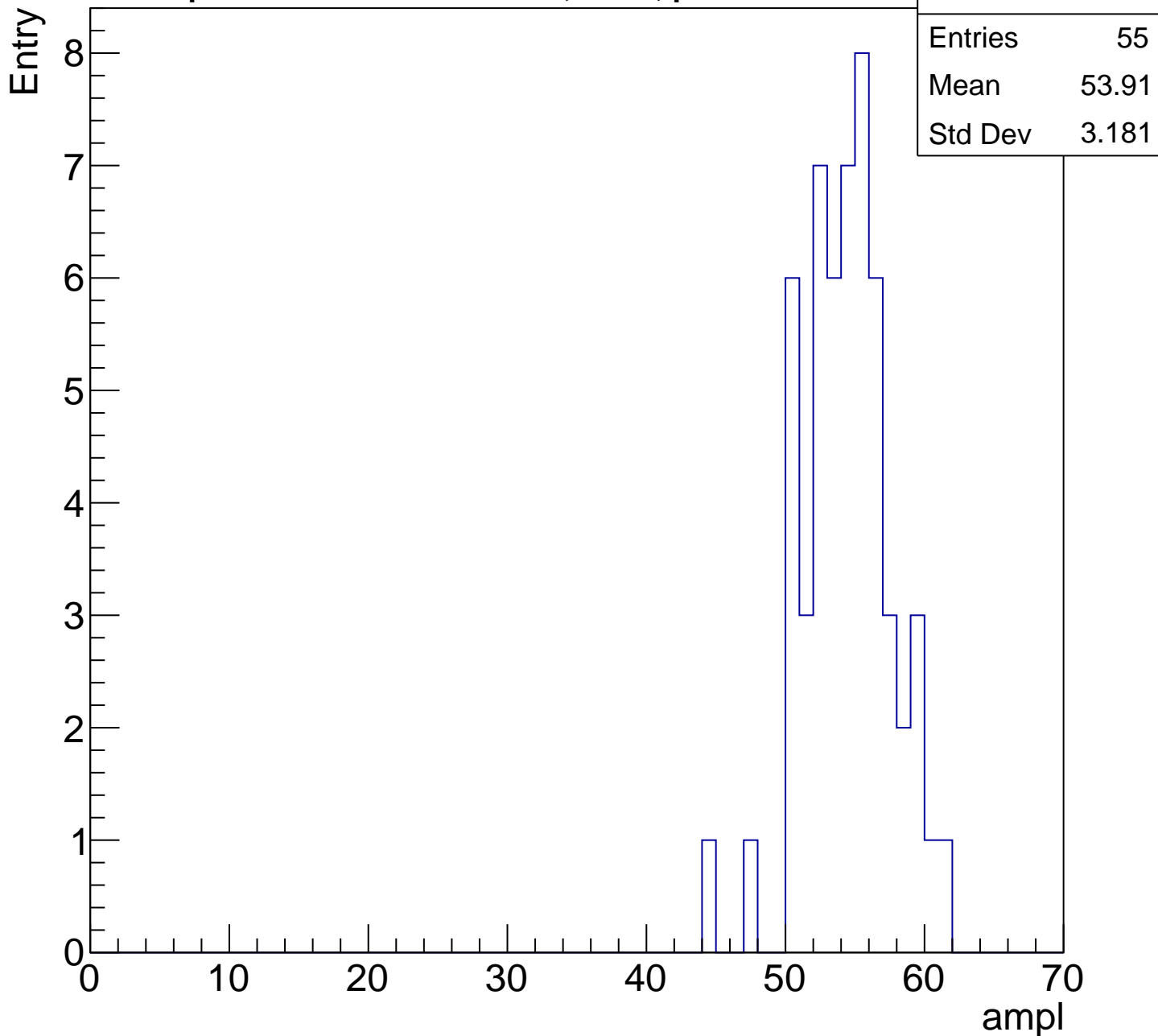
Entry

Entries	64
Mean	47.23
Std Dev	3.534



# B1L103S, U26-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

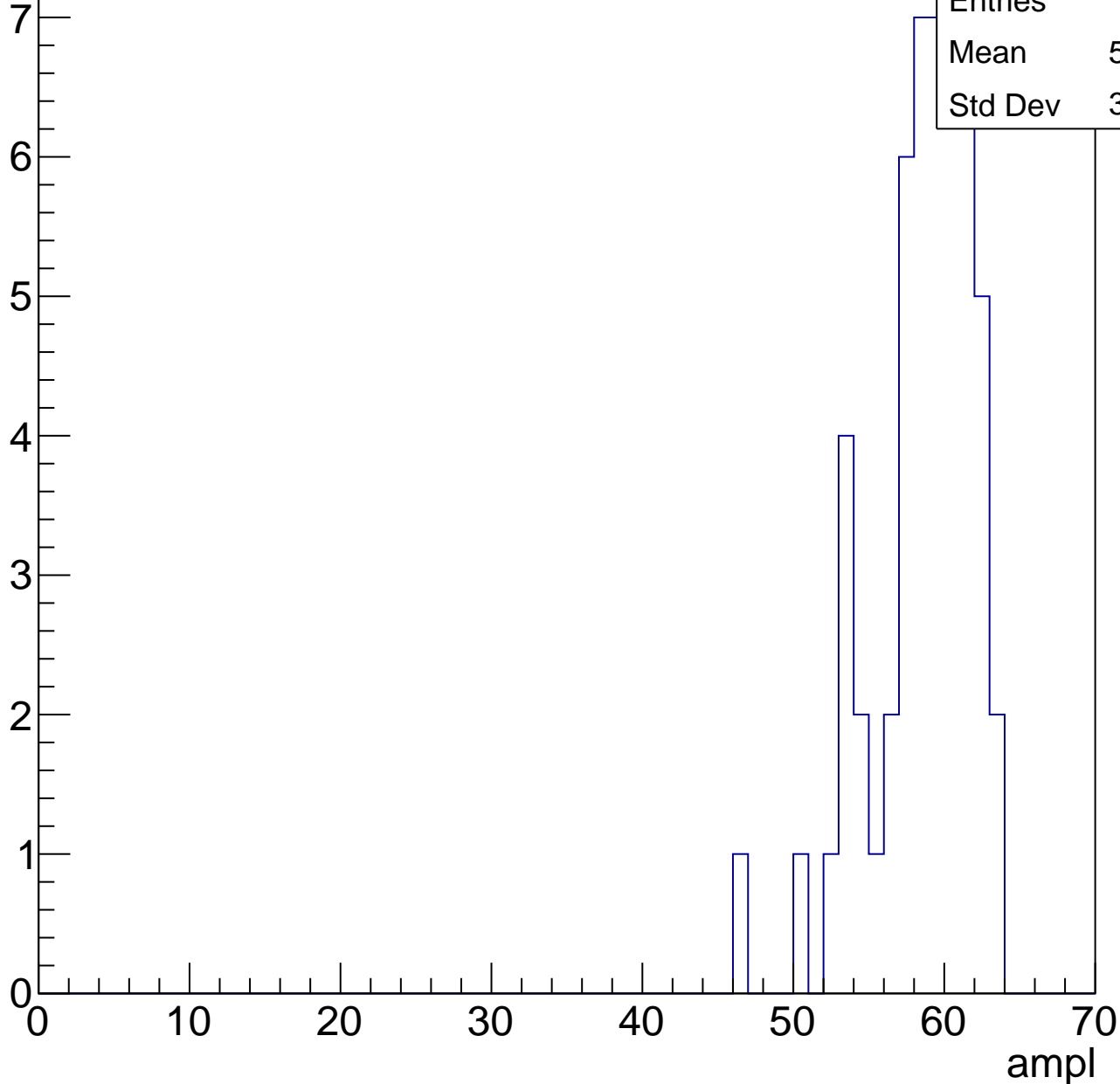


# B1L103S, U26-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	58.09
Std Dev	3.438

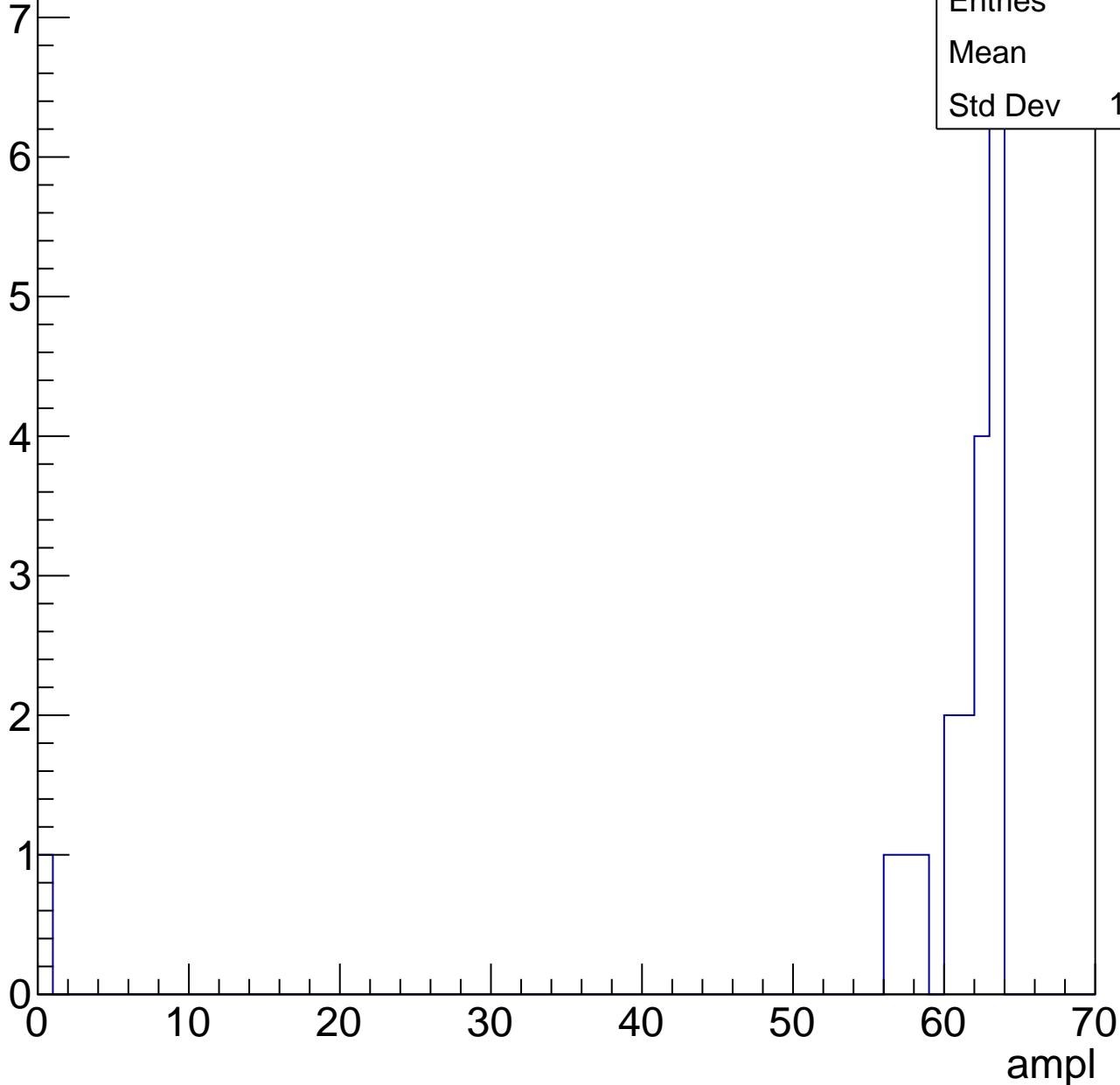


# B1L103S, U26-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	19
Mean	58
Std Dev	13.83





# B1L103S, U26-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch33, adc0

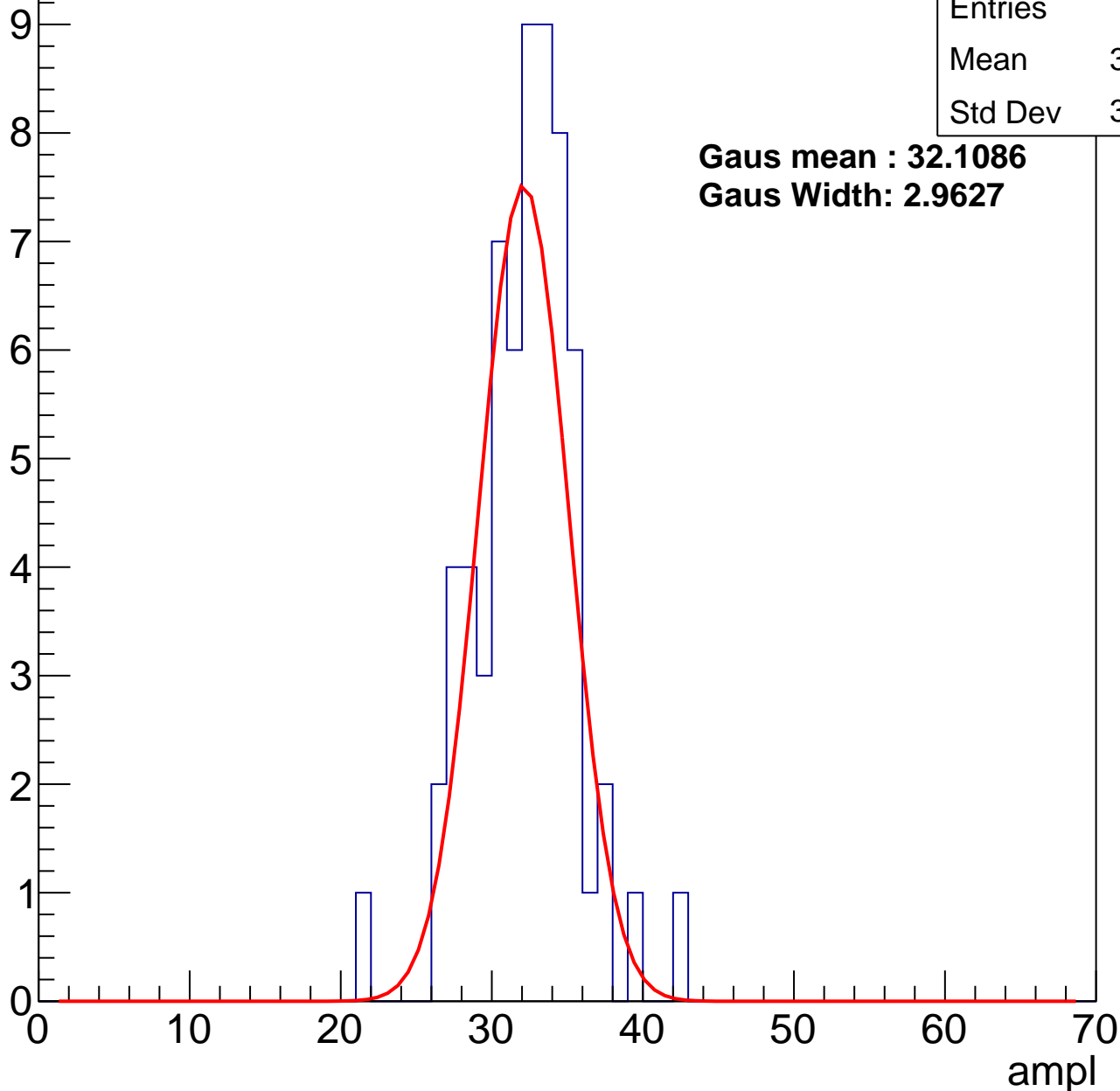
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	31.78
Std Dev	3.366

**Gaus mean : 32.1086**

**Gaus Width: 2.9627**



# B1L103S, U26-ch33, adc1

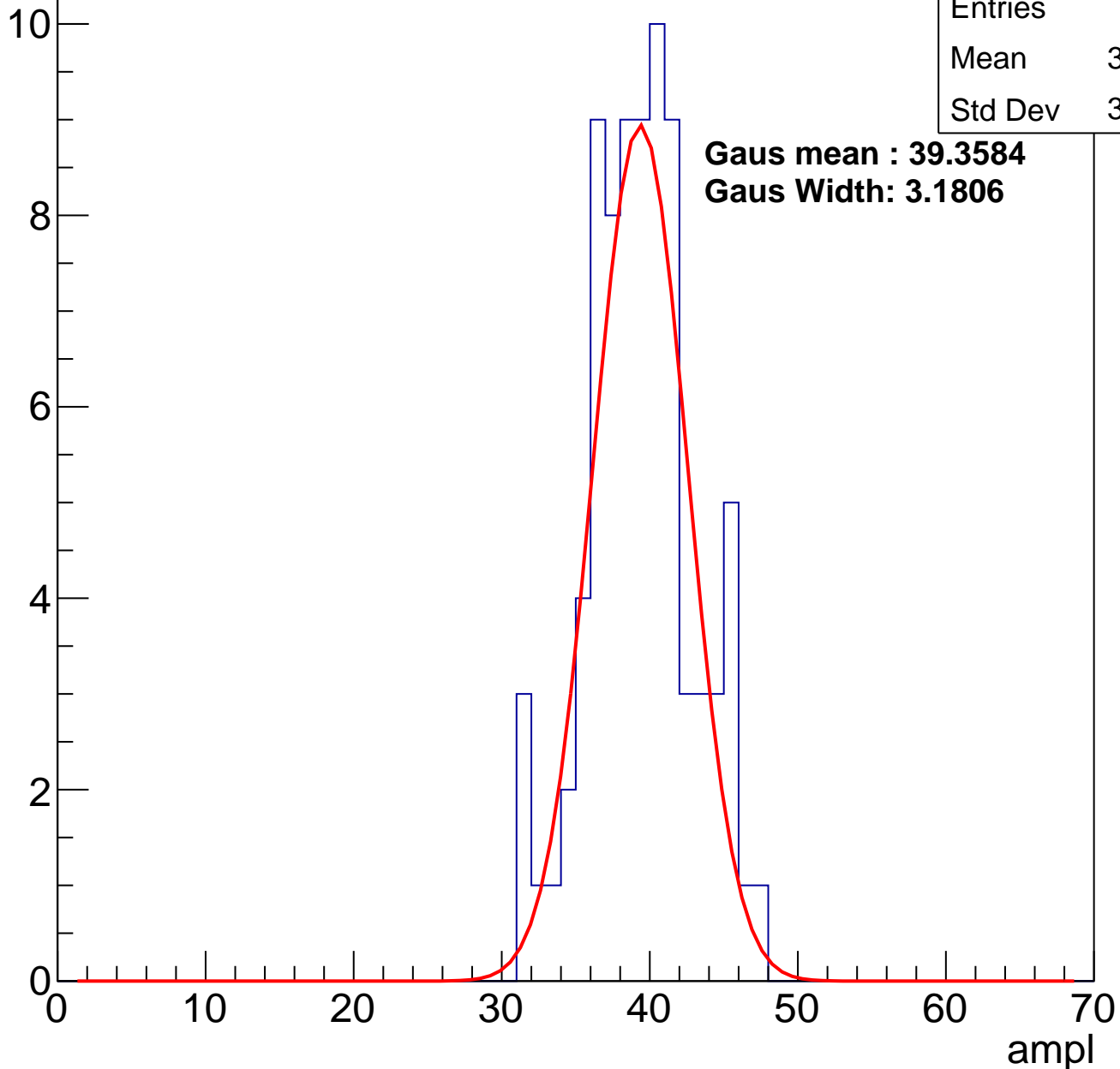
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	81
Mean	38.93
Std Dev	3.516

**Gaus mean : 39.3584**

**Gaus Width: 3.1806**

Entry

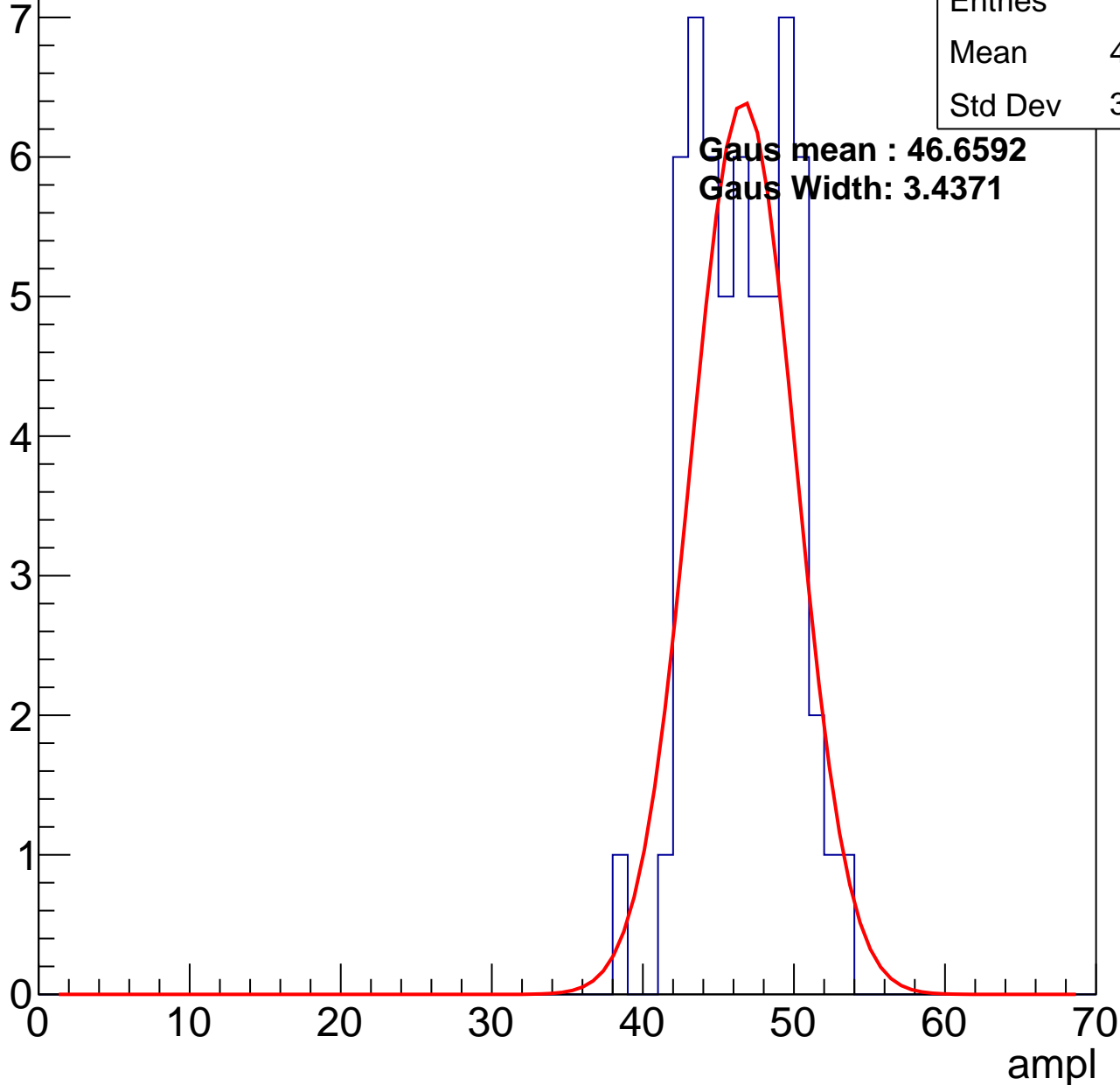


# B1L103S, U26-ch33, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	46.14
Std Dev	3.175

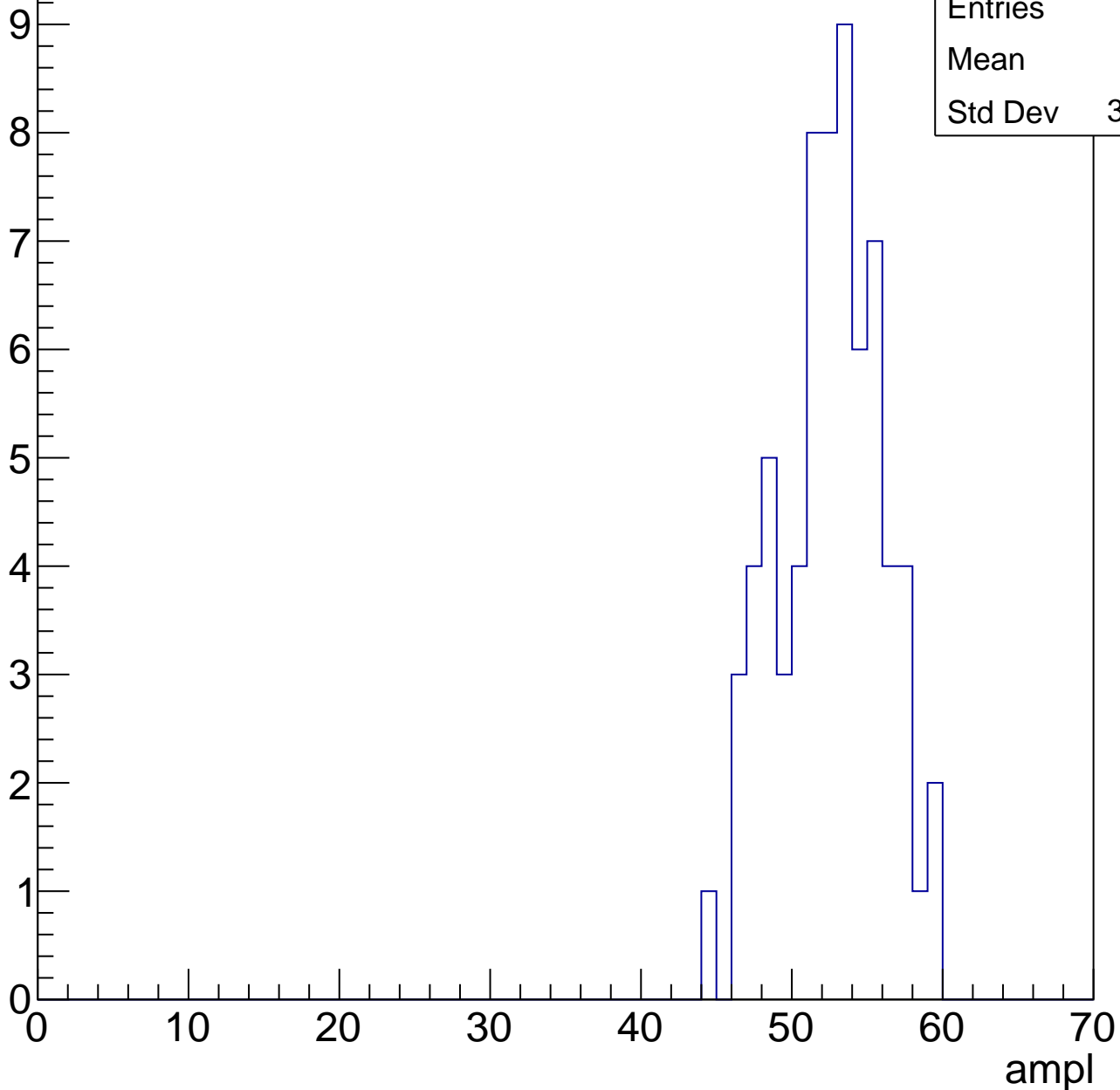


# B1L103S, U26-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

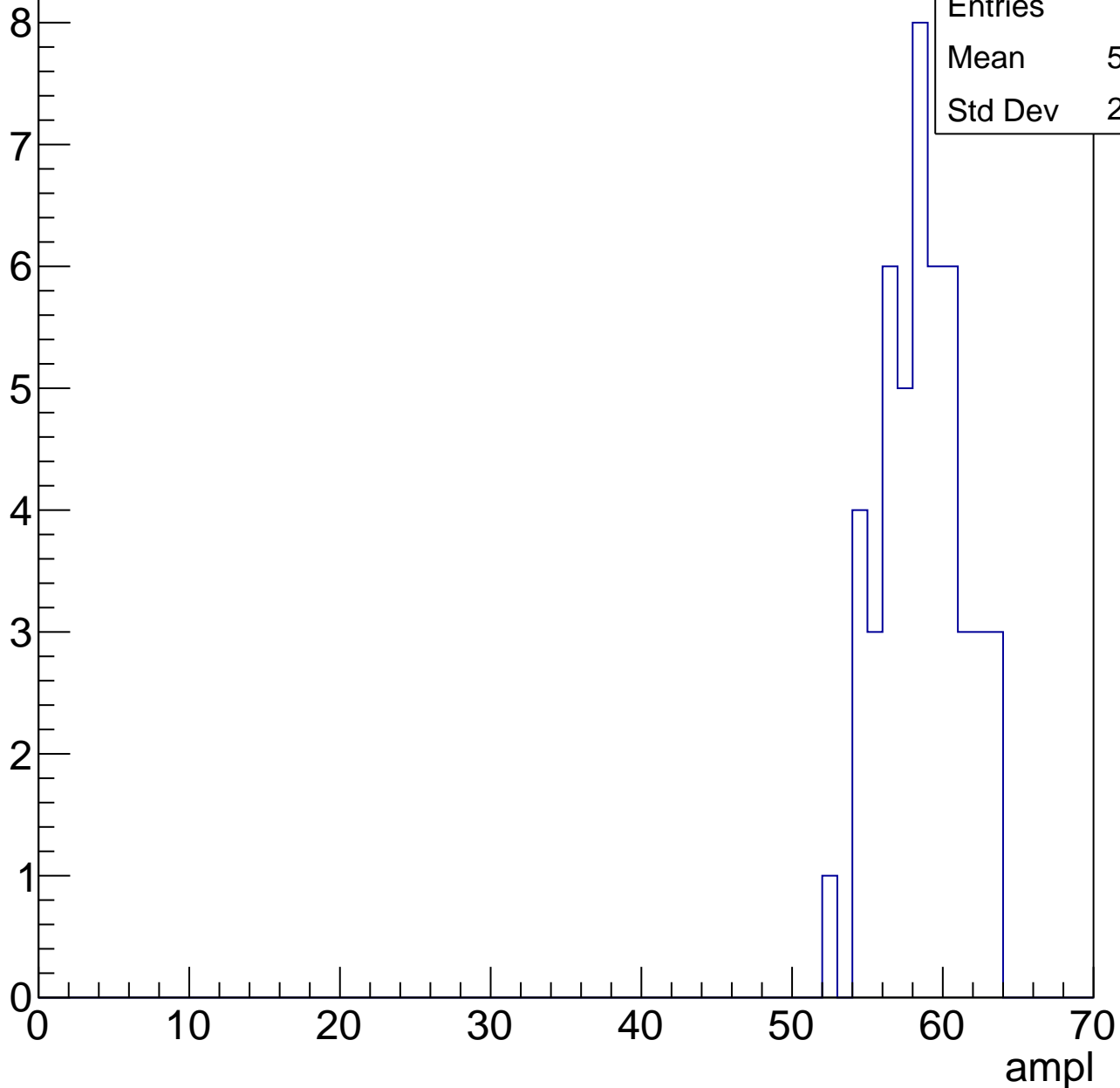
Entries	69
Mean	52.1
Std Dev	3.397



# B1L103S, U26-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

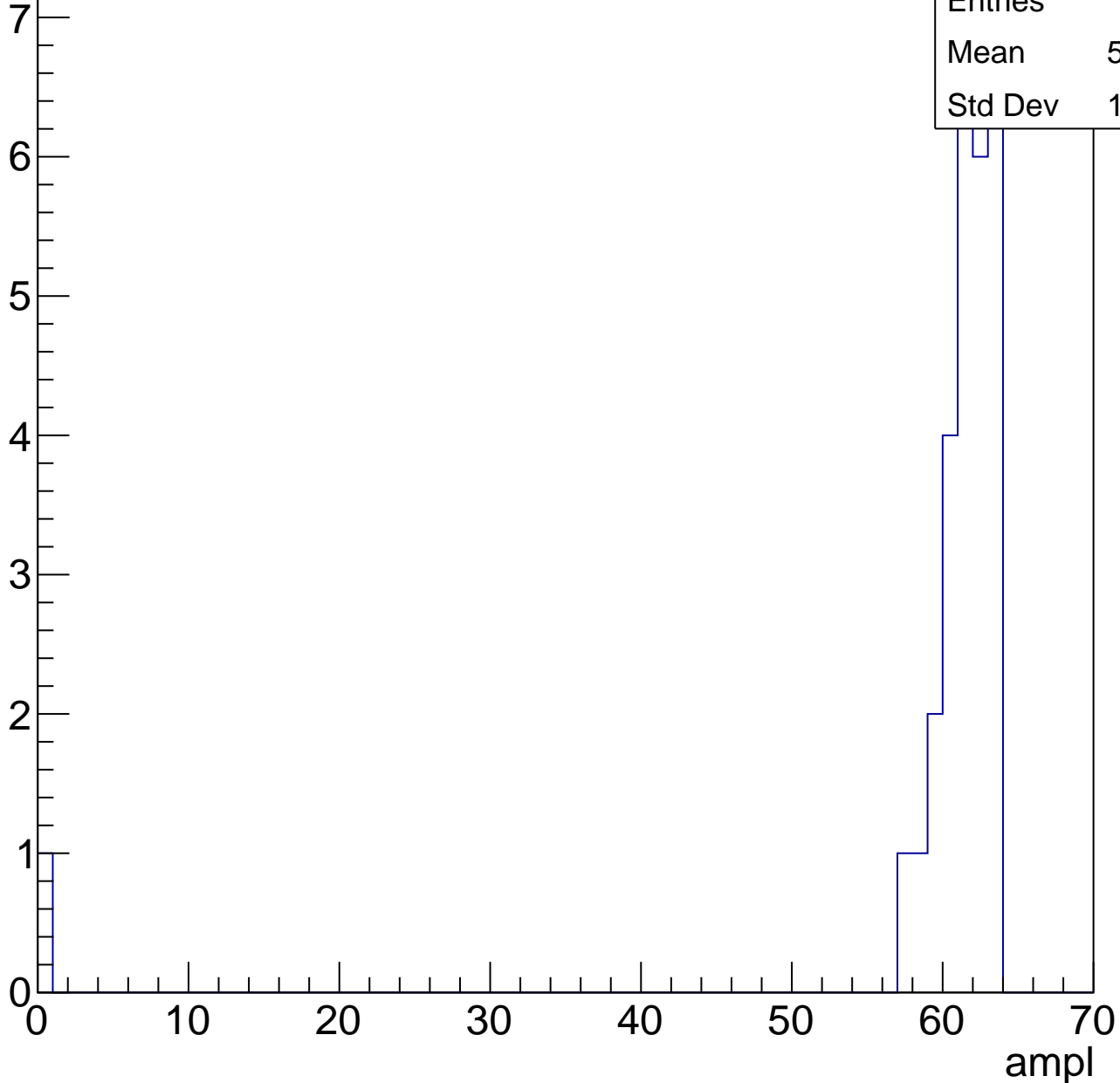


# B1L103S, U26-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	29
Mean	59.07
Std Dev	11.27



# B1L103S, U26-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U26-ch34, adc0

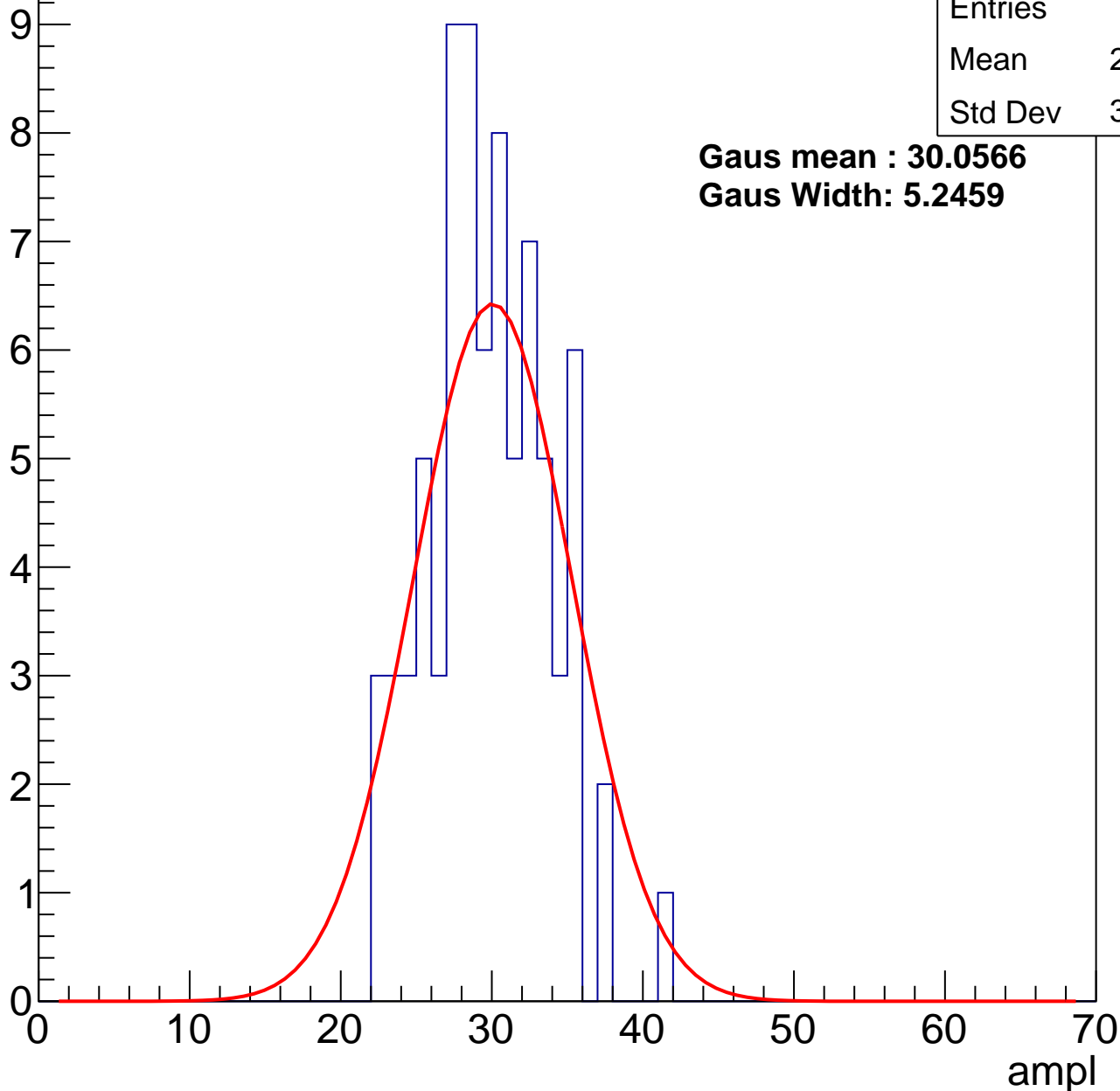
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	29.36
Std Dev	3.932

**Gaus mean : 30.0566**

**Gaus Width: 5.2459**

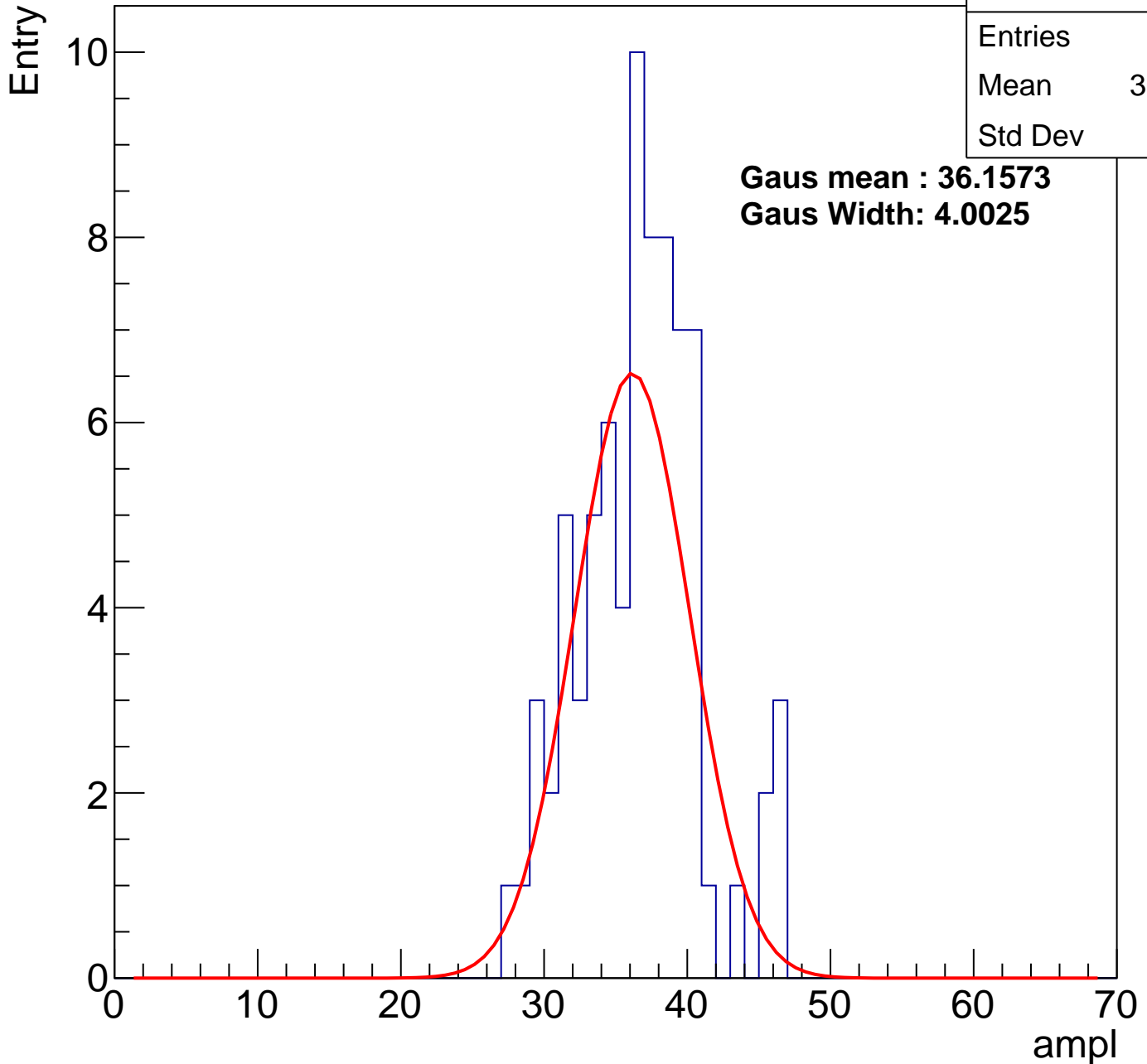


# B1L103S, U26-ch34, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	77
Mean	36.19
Std Dev	4.2

**Gaus mean : 36.1573**  
**Gaus Width: 4.0025**



# B1L103S, U26-ch34, adc2

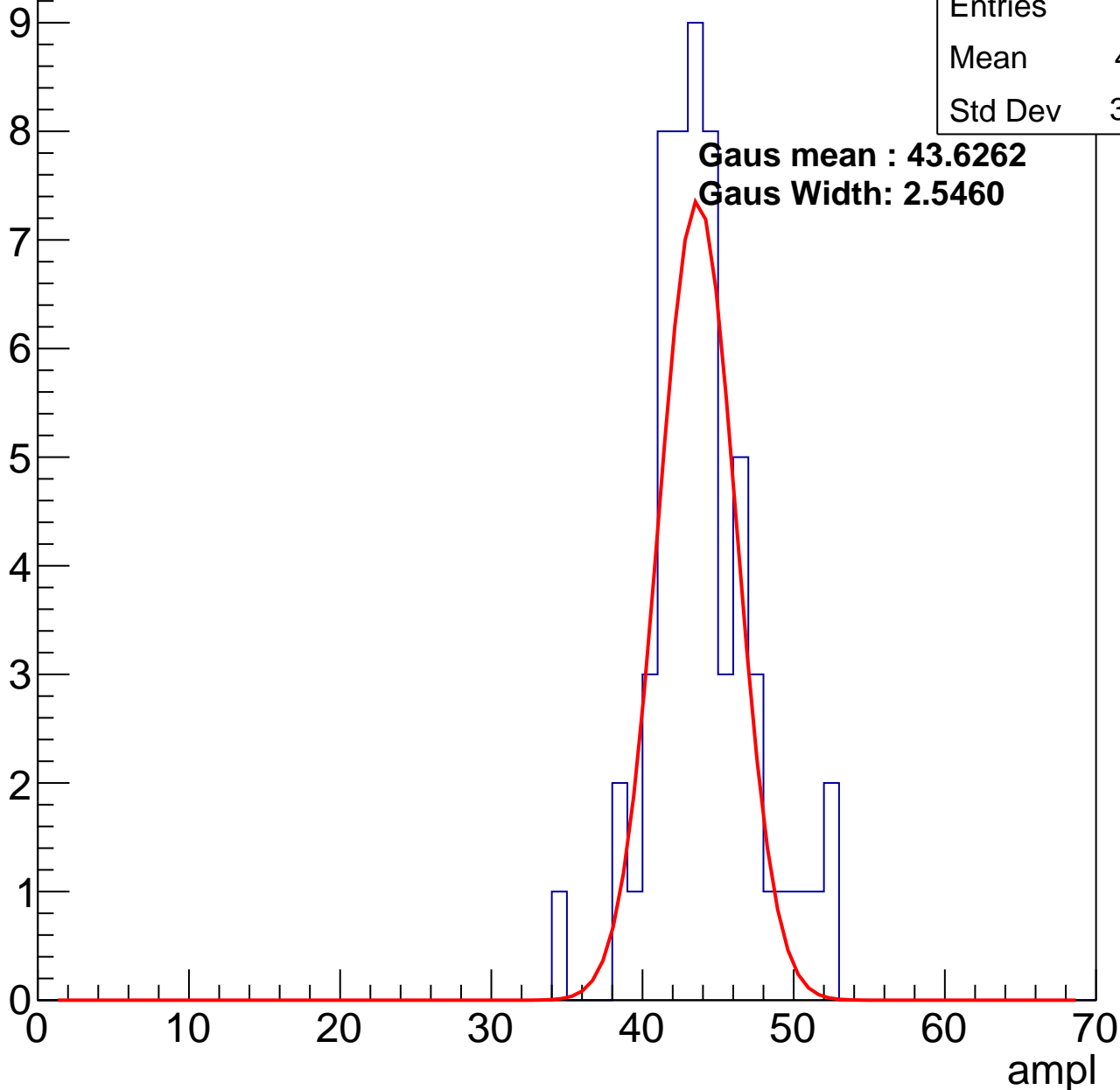
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	43.51
Std Dev	3.372

**Gaus mean : 43.6262**

**Gaus Width: 2.5460**

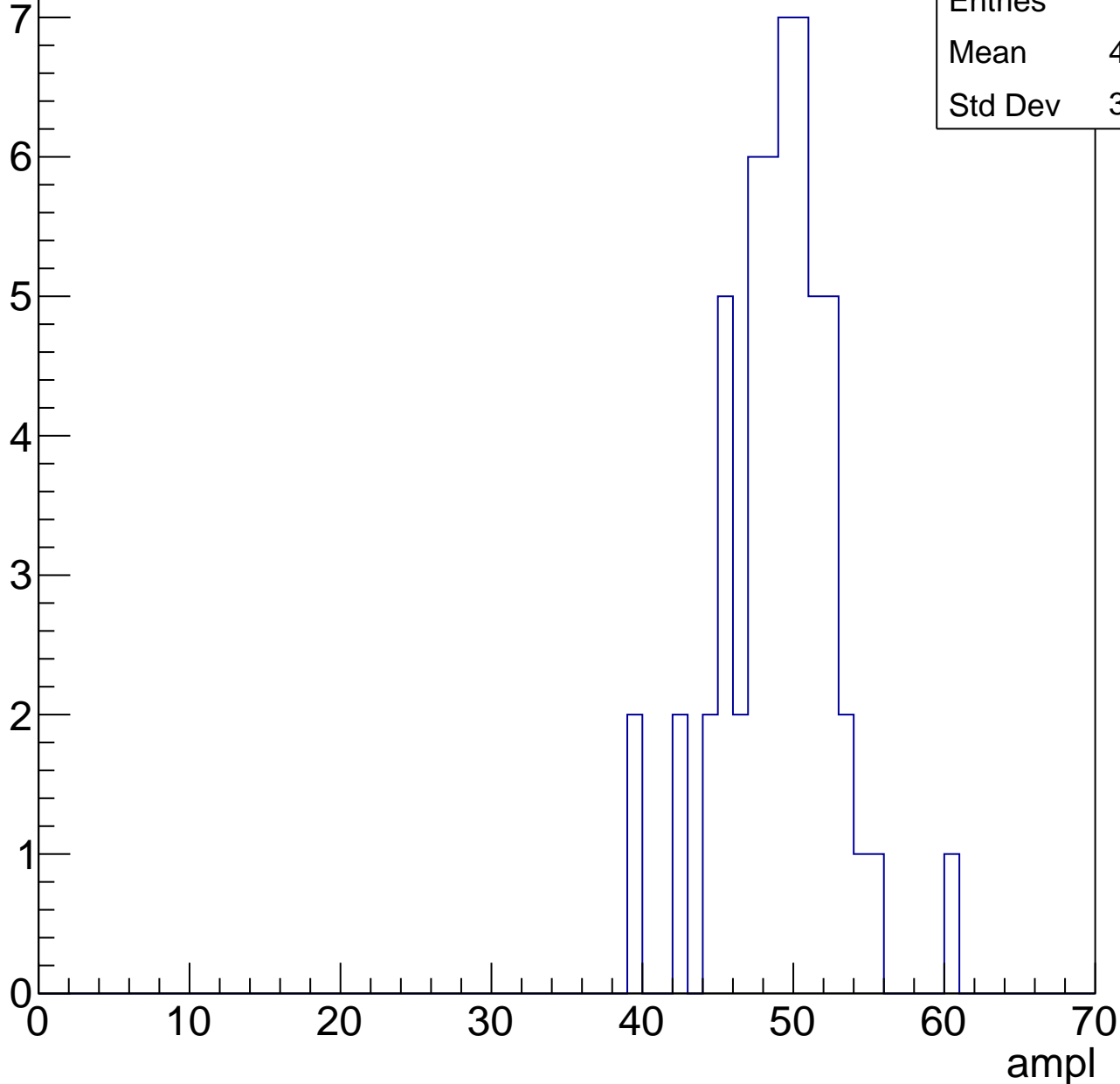


# B1L103S, U26-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	48.52
Std Dev	3.725

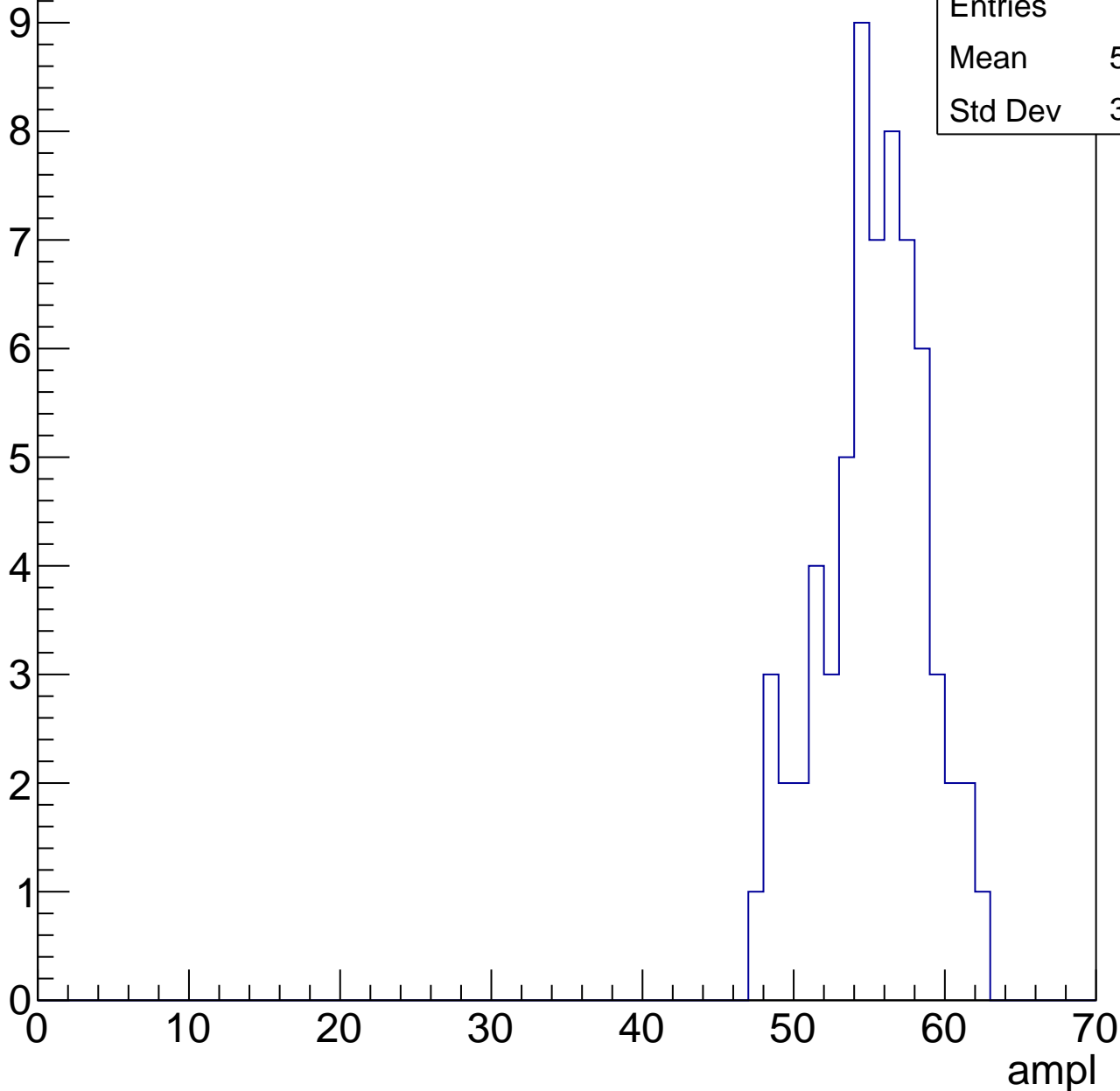


# B1L103S, U26-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	54.78
Std Dev	3.417

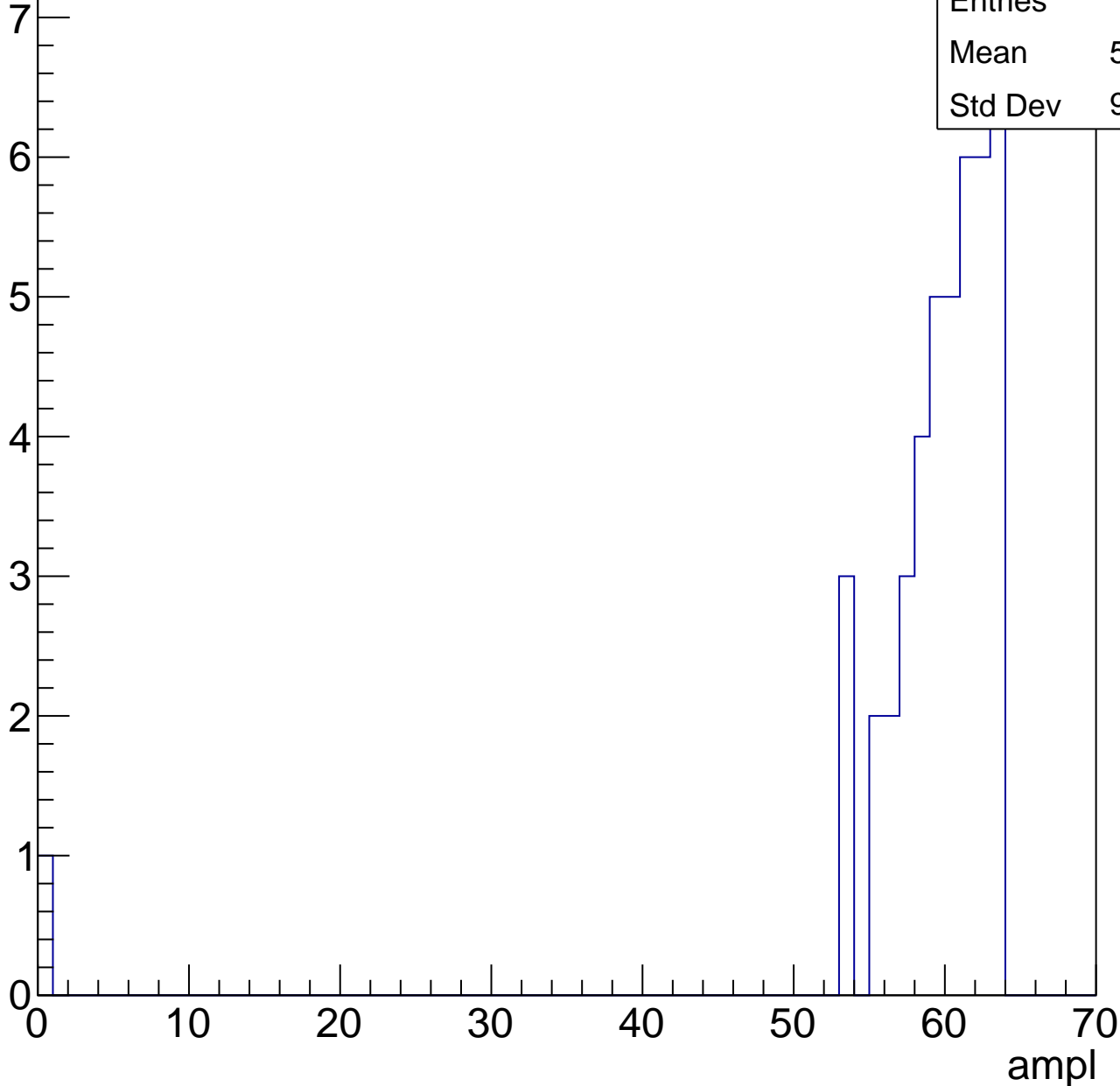


# B1L103S, U26-ch34, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

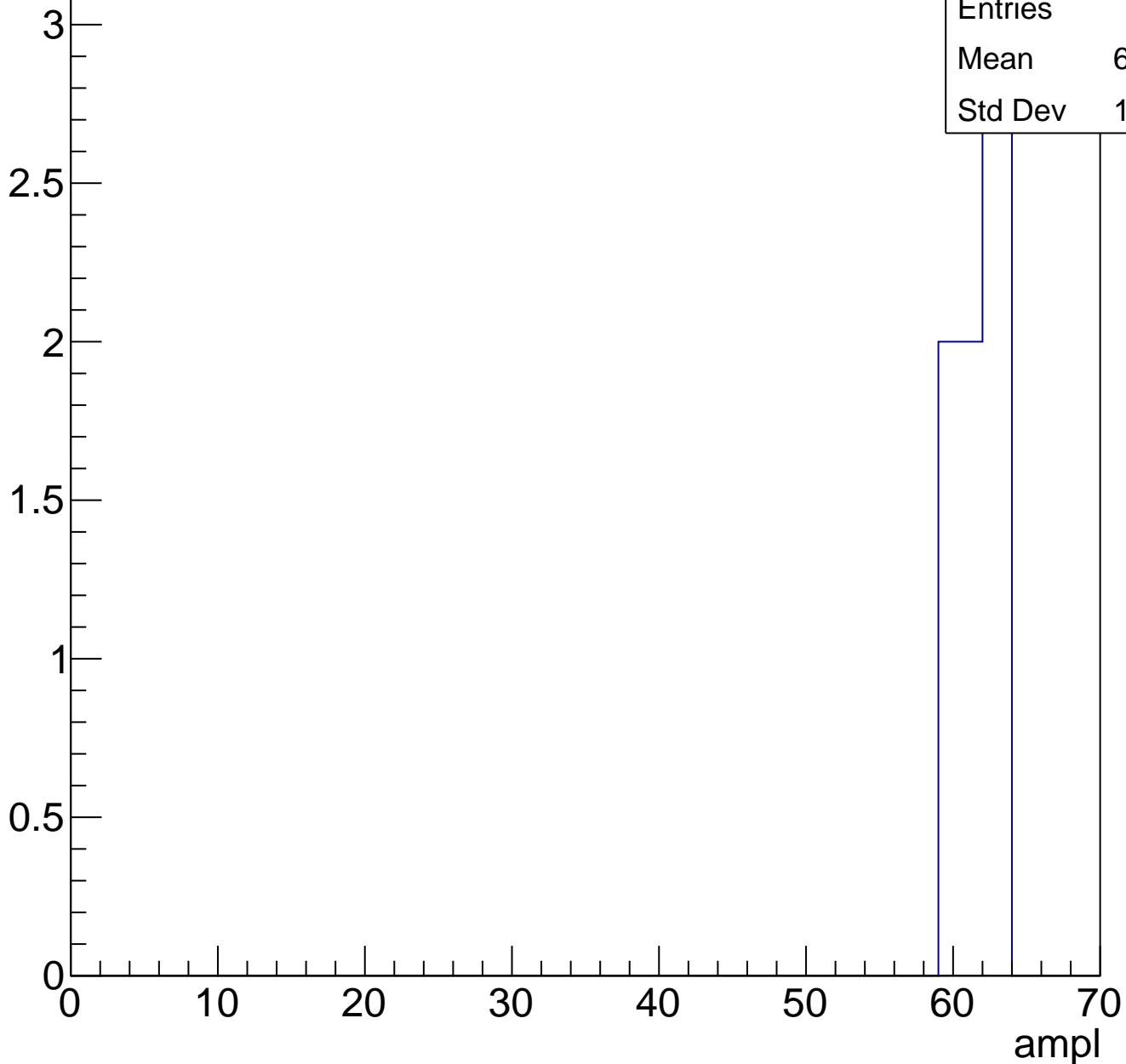
Entries	44
Mean	58.14
Std Dev	9.314



# B1L103S, U26-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U26-ch35, adc0

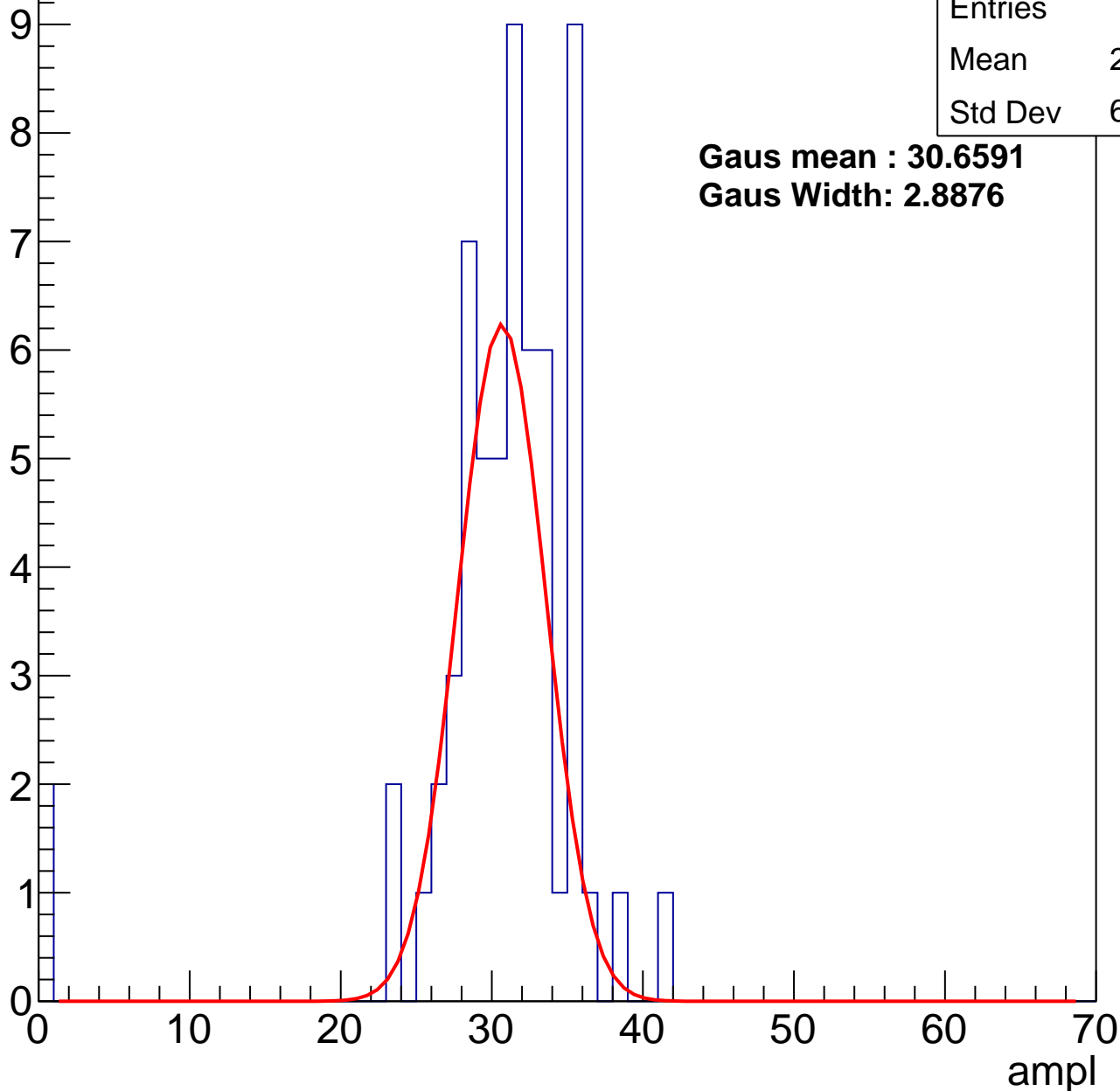
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	29.97
Std Dev	6.483

**Gaus mean : 30.6591**

**Gaus Width: 2.8876**



# B1L103S, U26-ch35, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	72
Mean	37.71
Std Dev	3.446

**Gaus mean : 38.8031**

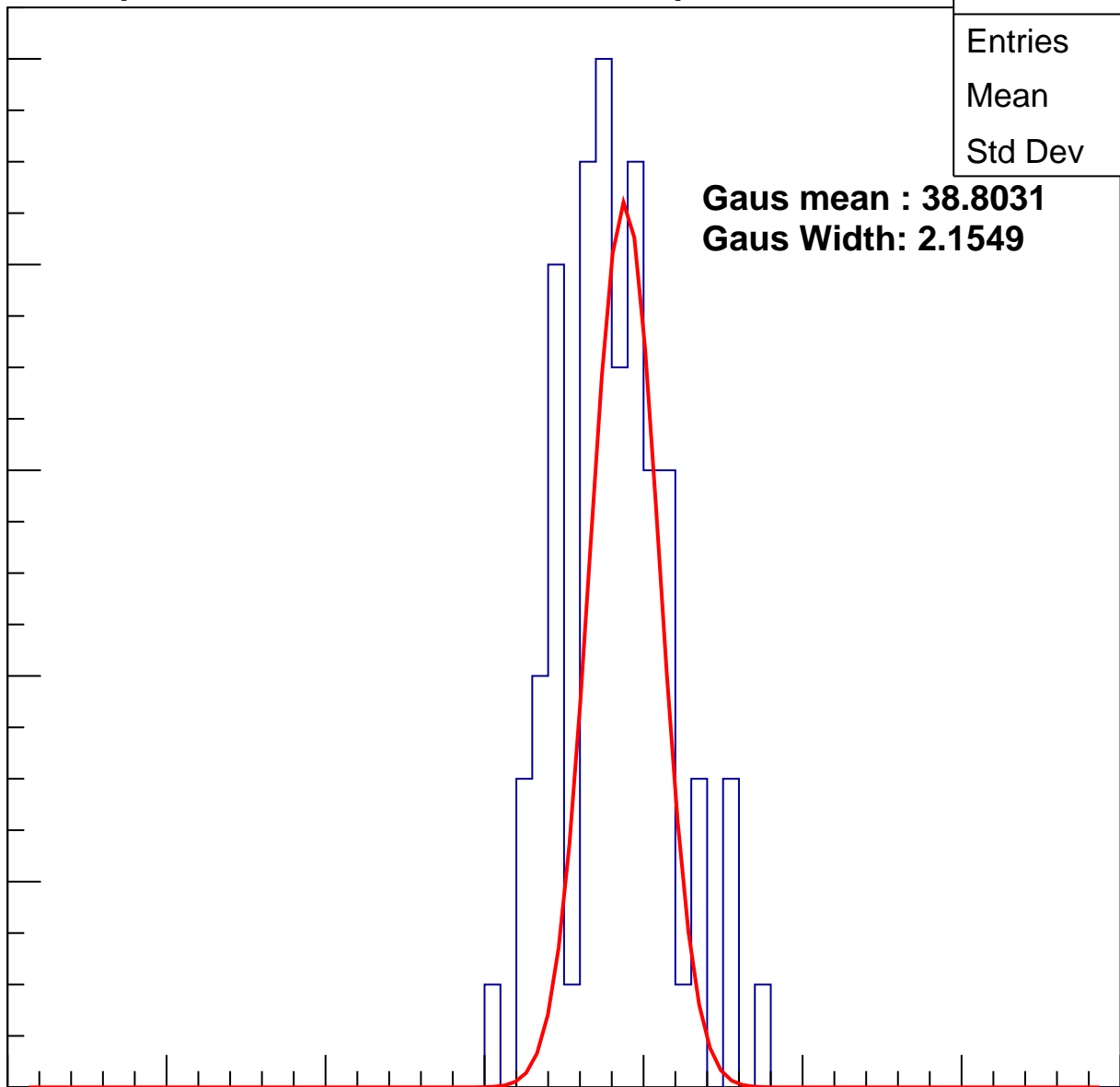
**Gaus Width: 2.1549**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch35, adc2

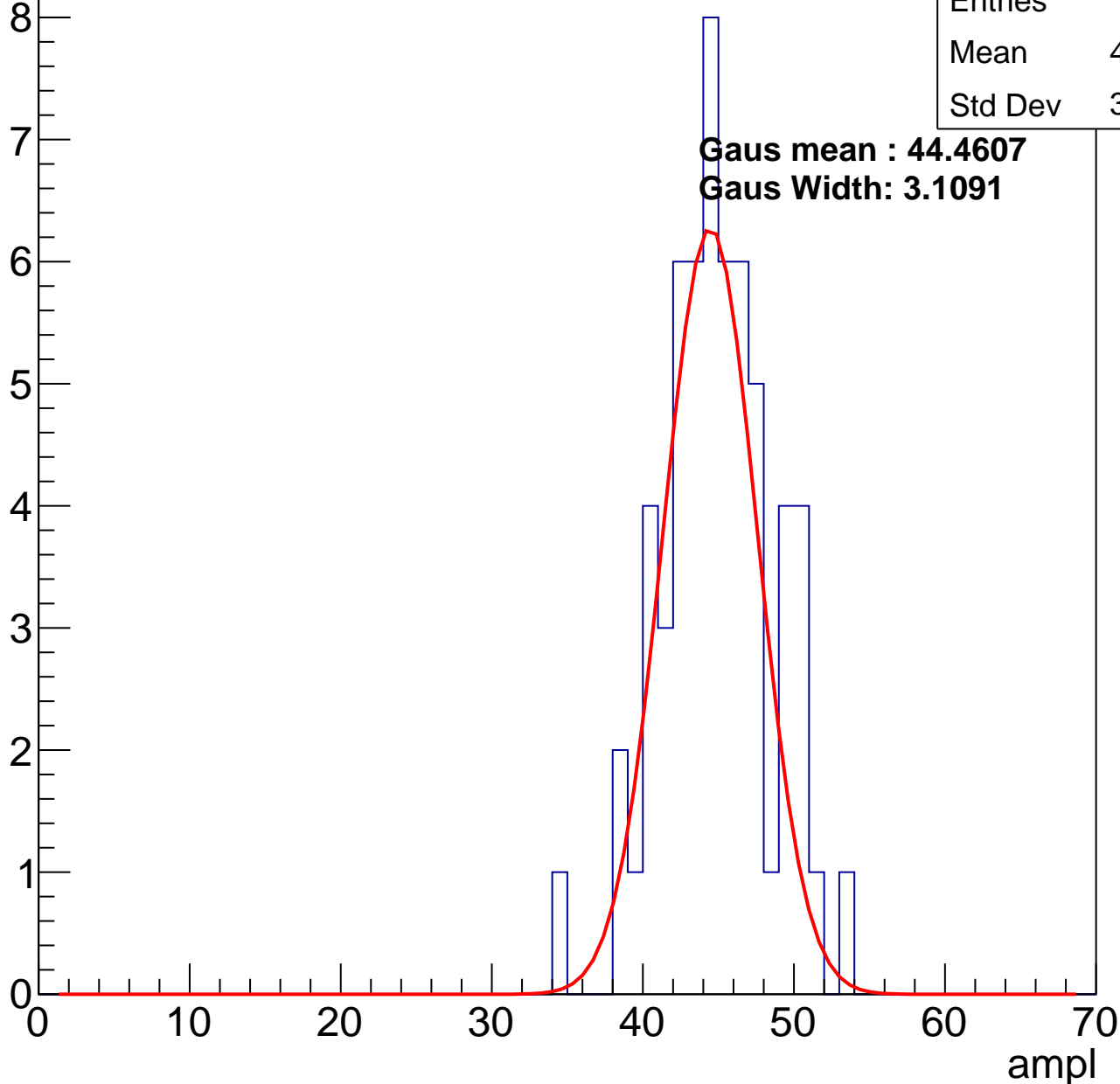
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	44.46
Std Dev	3.614

**Gaus mean : 44.4607**

**Gaus Width: 3.1091**

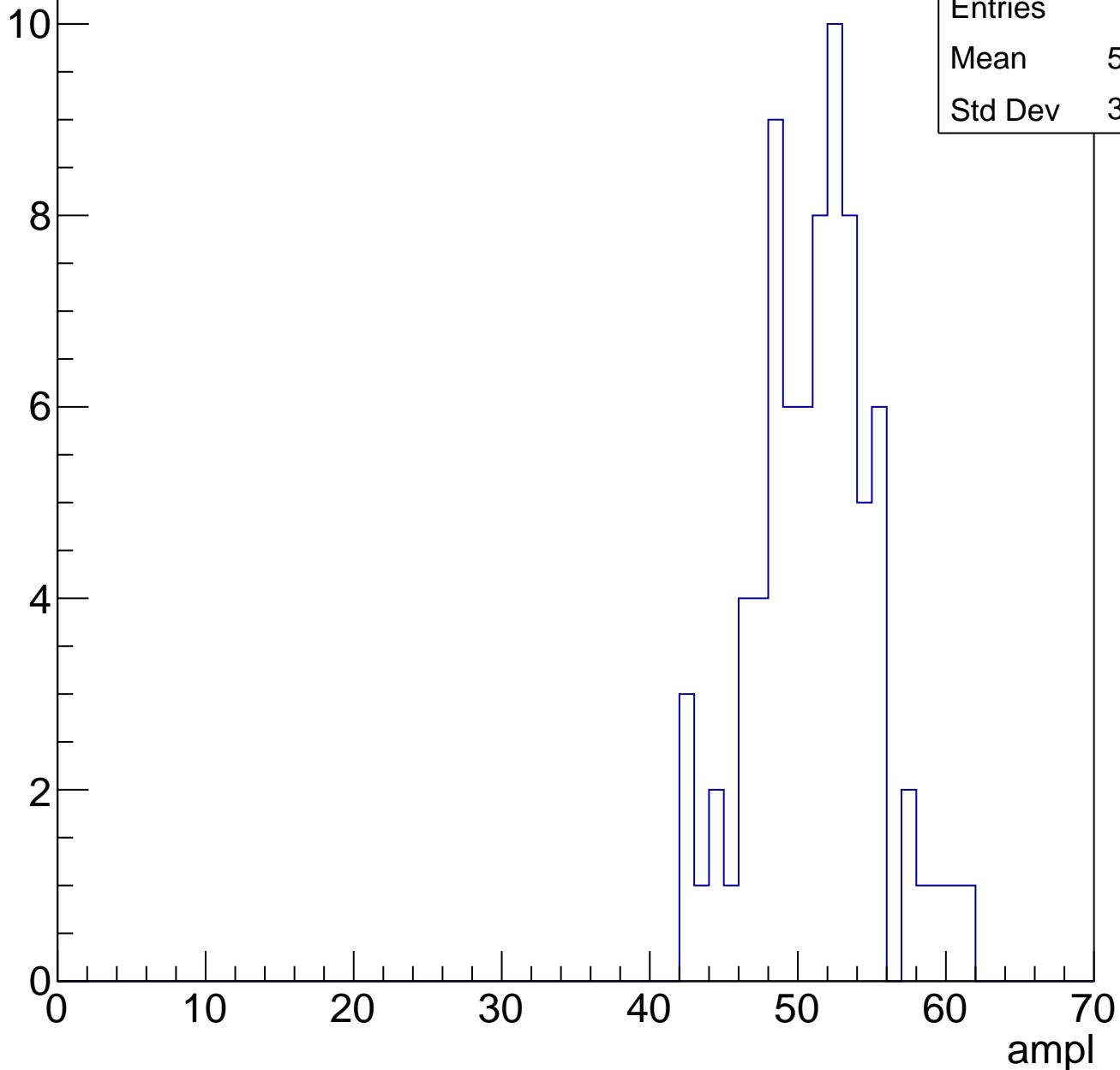


# B1L103S, U26-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	79
Mean	50.68
Std Dev	3.989

Entry

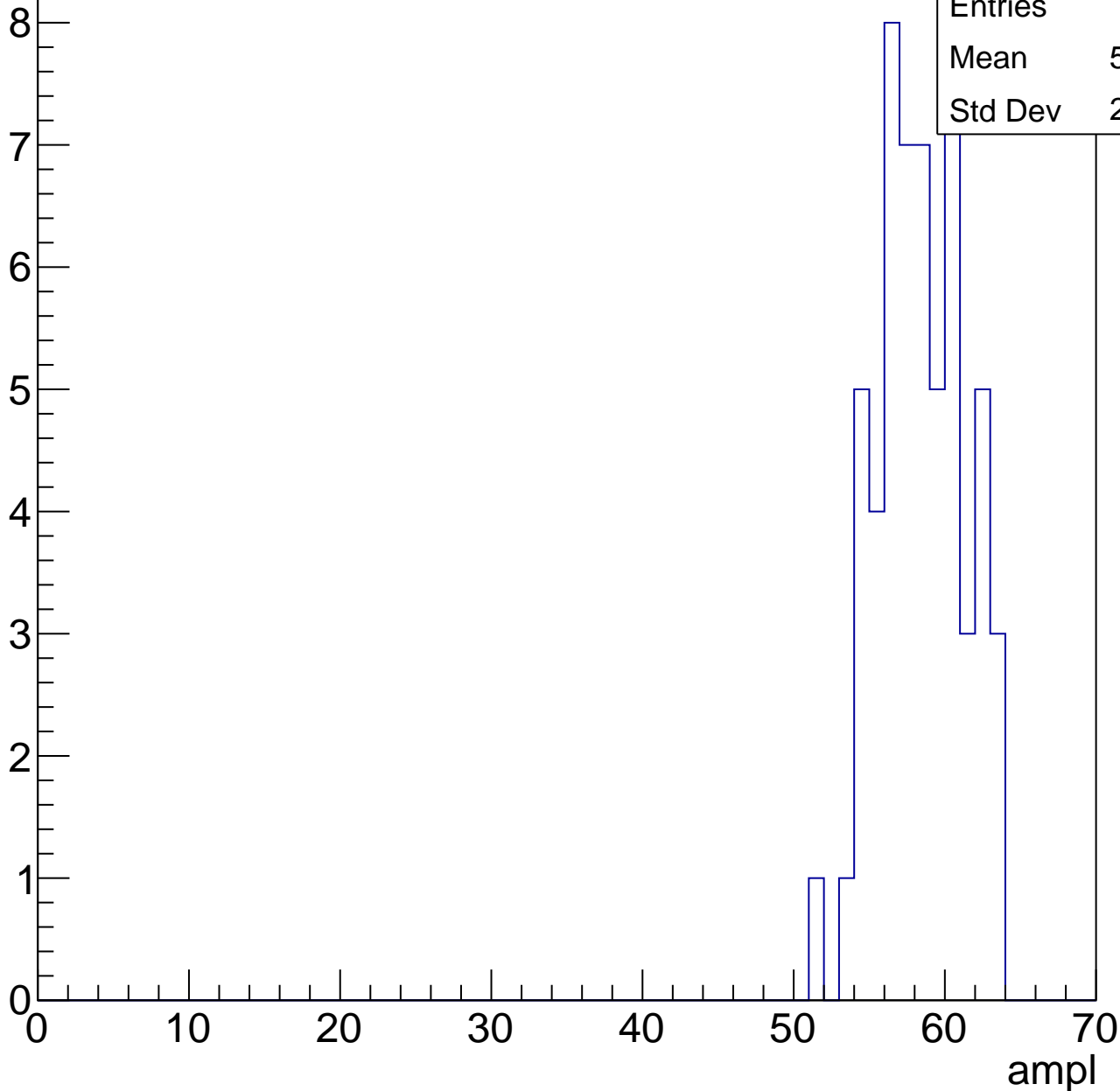


# B1L103S, U26-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

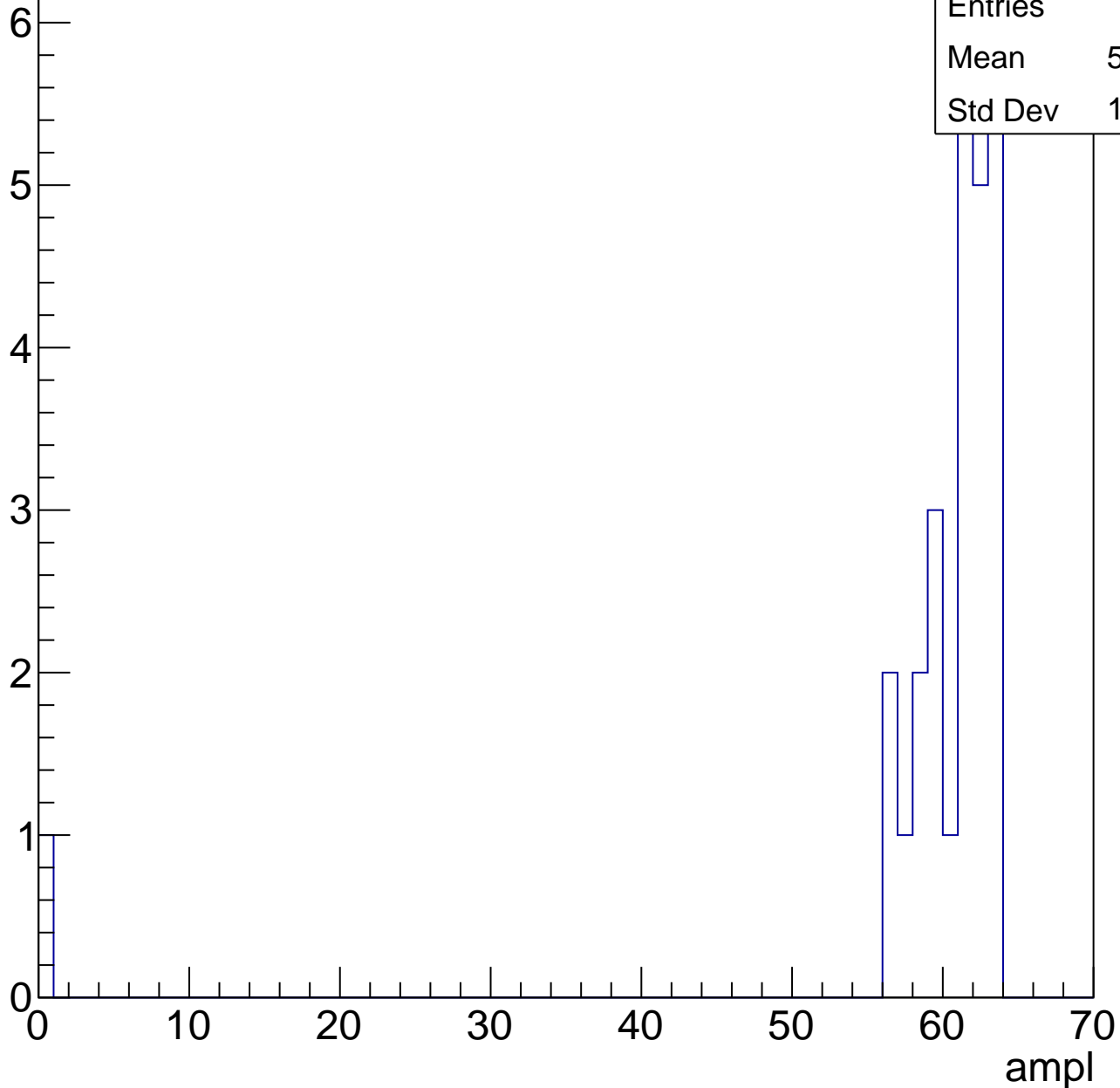
Entries	57
Mean	57.96
Std Dev	2.803



# B1L103S, U26-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U26-ch36, adc0

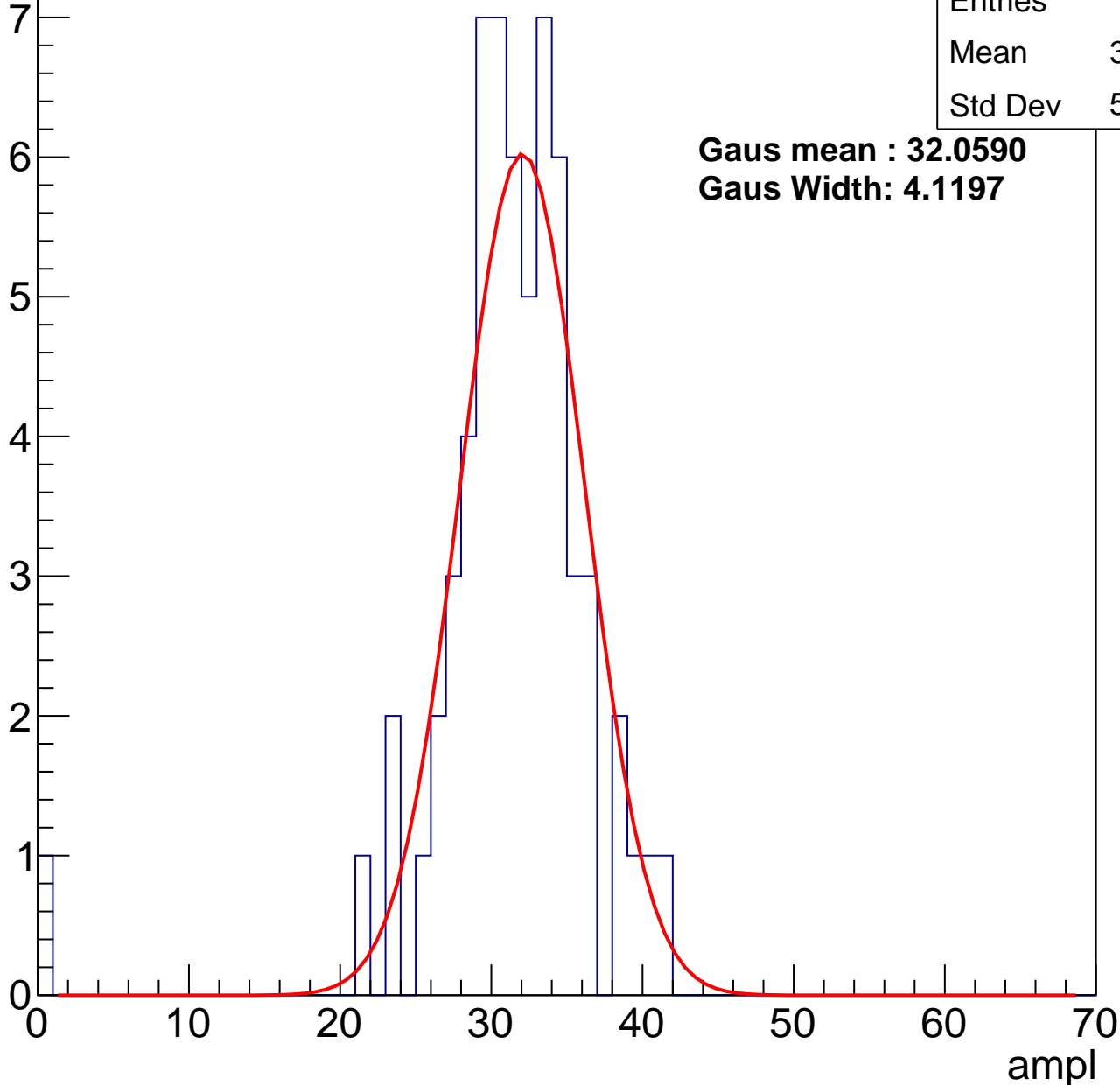
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	30.79
Std Dev	5.555

**Gaus mean : 32.0590**

**Gaus Width: 4.1197**



# B1L103S, U26-ch36, adc1

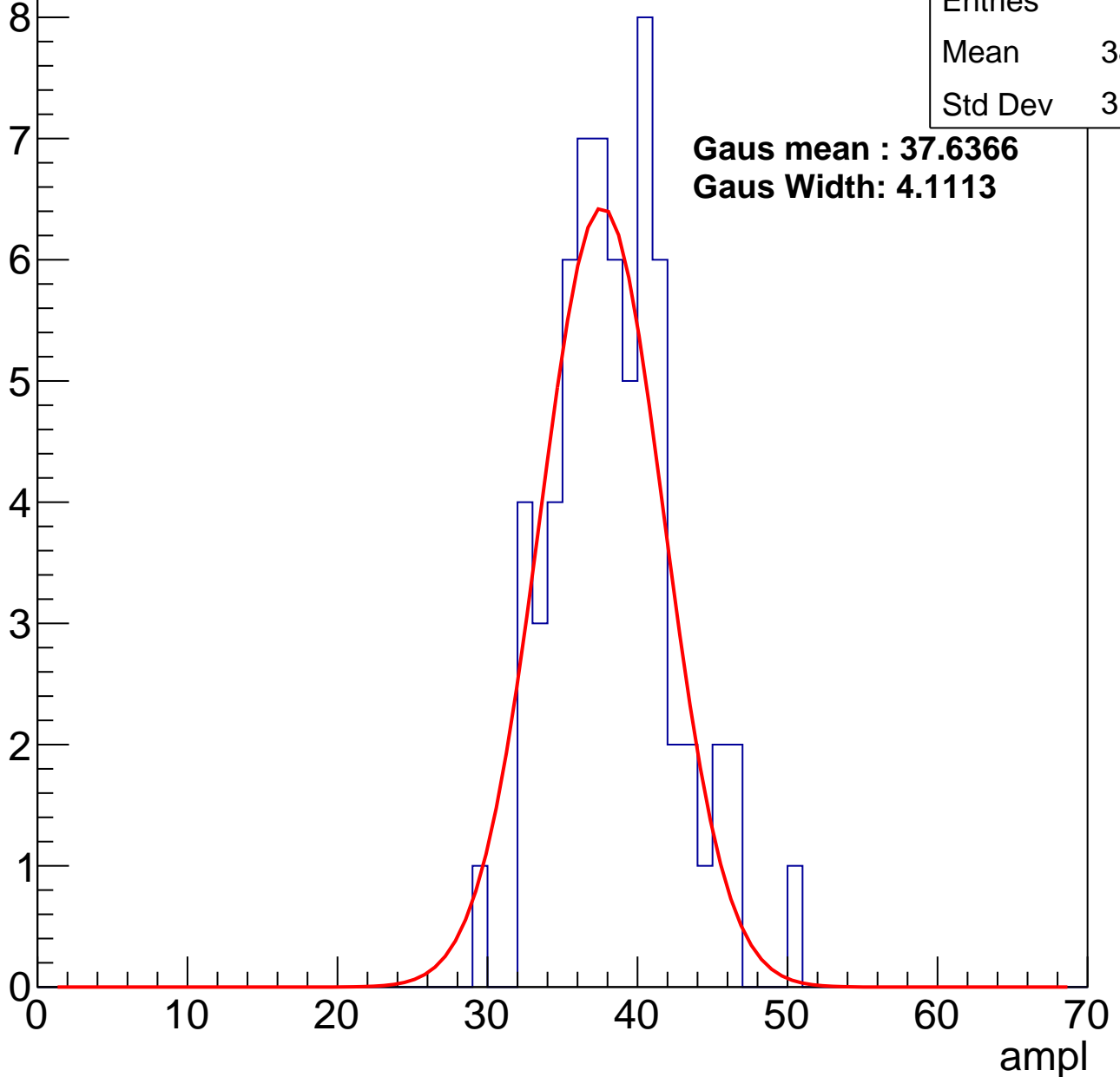
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	38.03
Std Dev	3.925

**Gaus mean : 37.6366**

**Gaus Width: 4.1113**



# B1L103S, U26-ch36, adc2

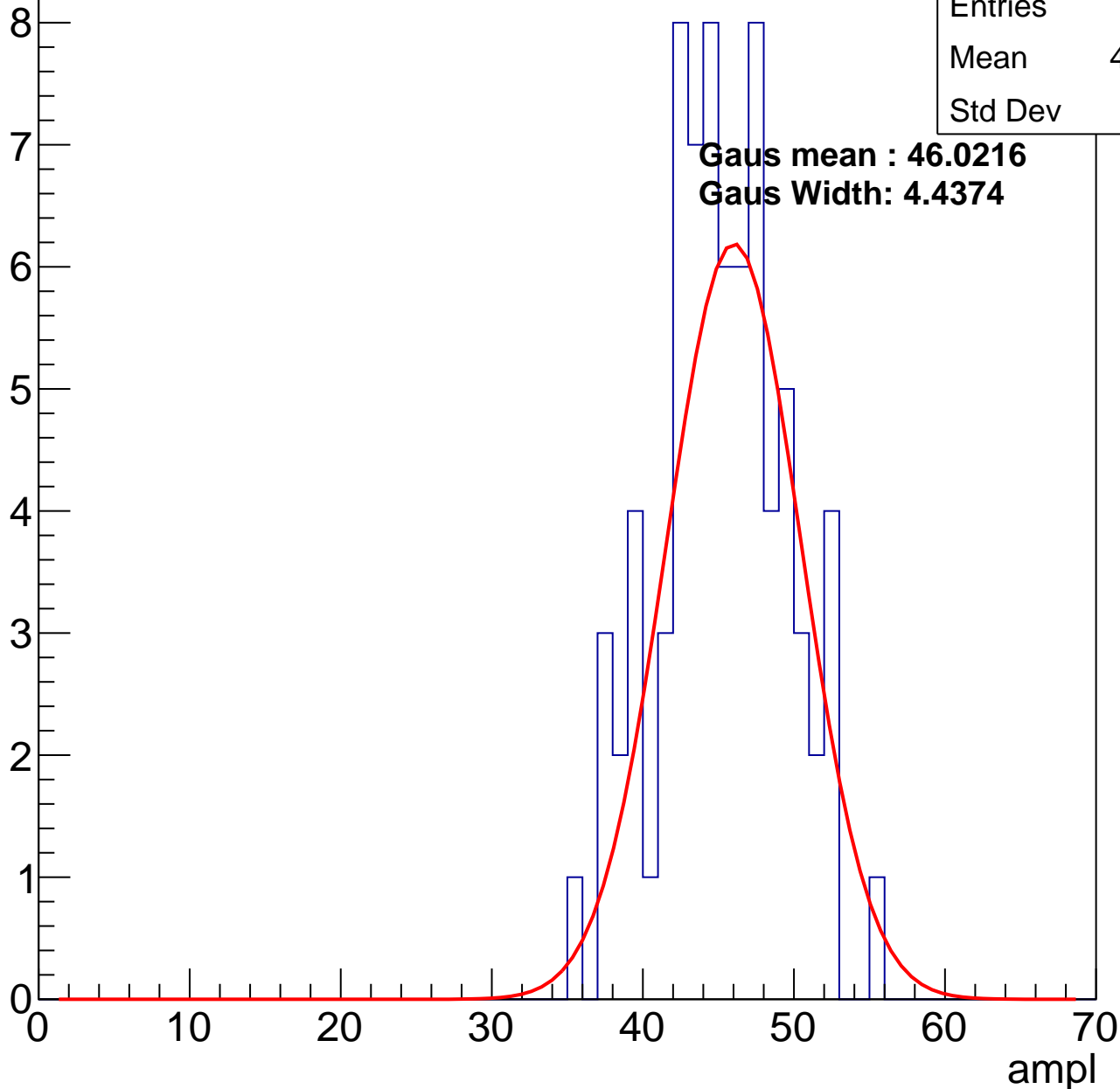
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	44.79
Std Dev	4.15

**Gaus mean : 46.0216**

**Gaus Width: 4.4374**

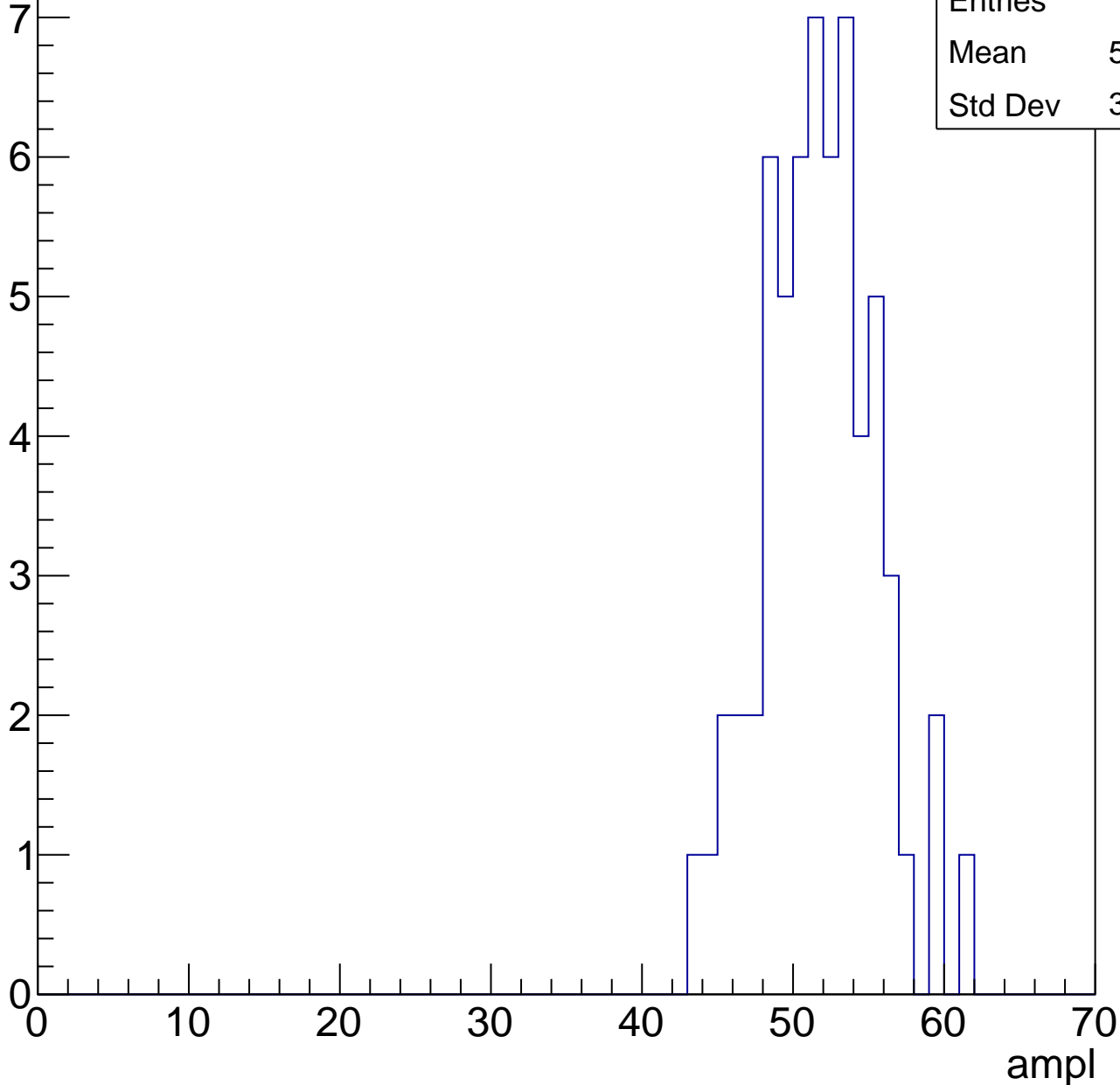


# B1L103S, U26-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	51.33
Std Dev	3.687

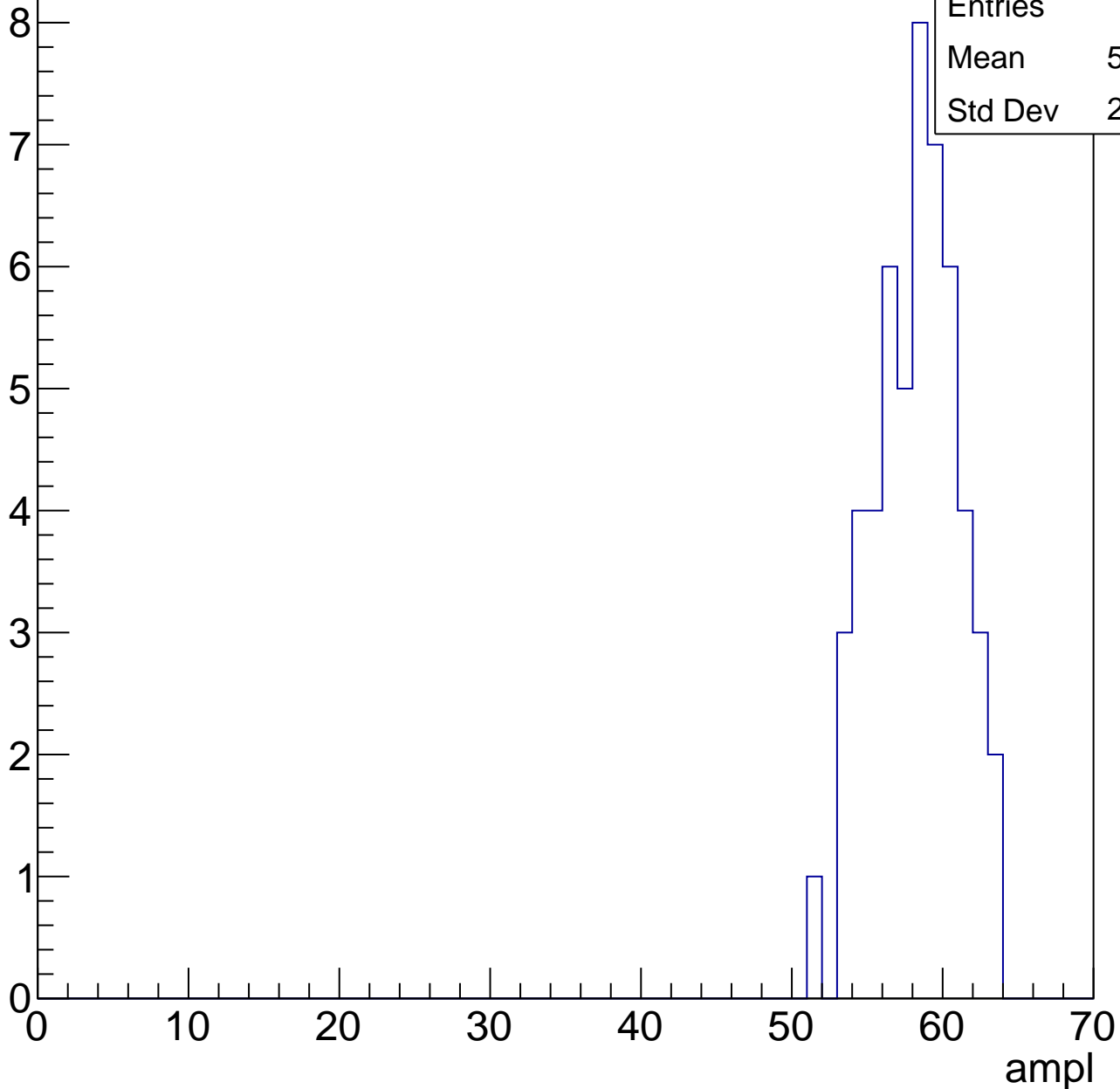


# B1L103S, U26-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	57.74
Std Dev	2.796

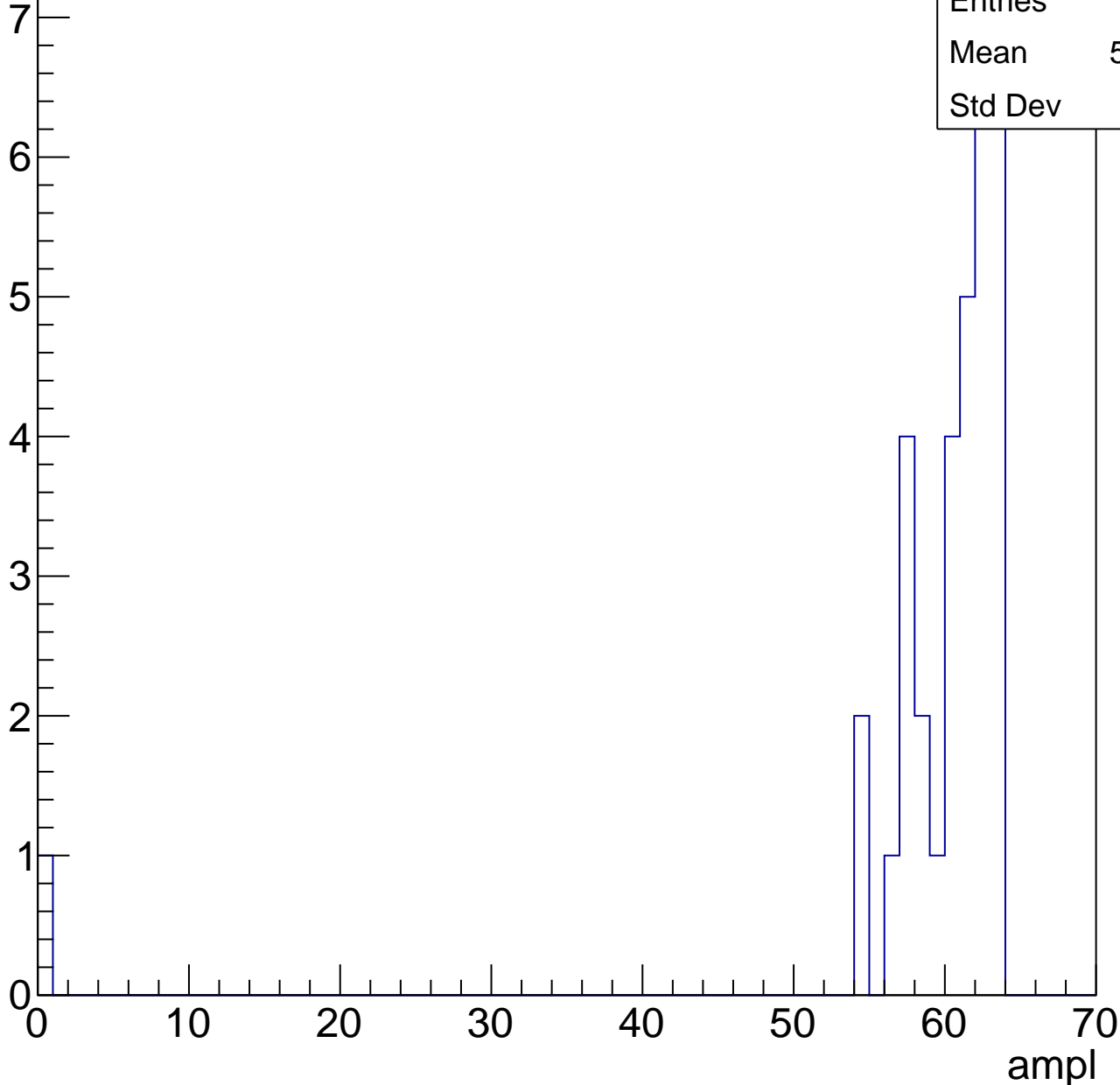


# B1L103S, U26-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	34
Mean	58.44
Std Dev	10.5



# B1L103S, U26-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U26-ch37, adc0

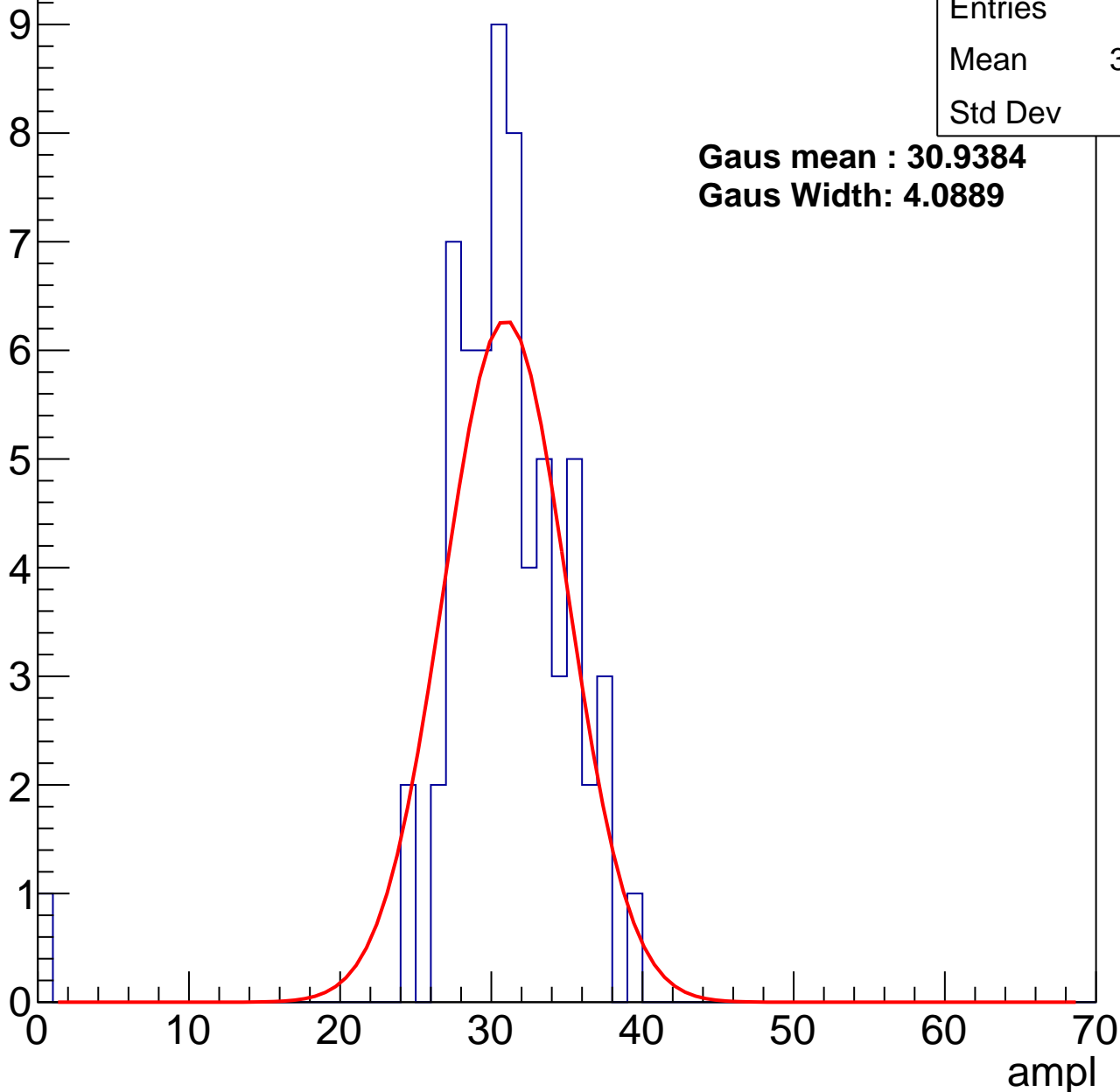
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	30.33
Std Dev	5.05

**Gaus mean : 30.9384**

**Gaus Width: 4.0889**



# B1L103S, U26-ch37, adc1

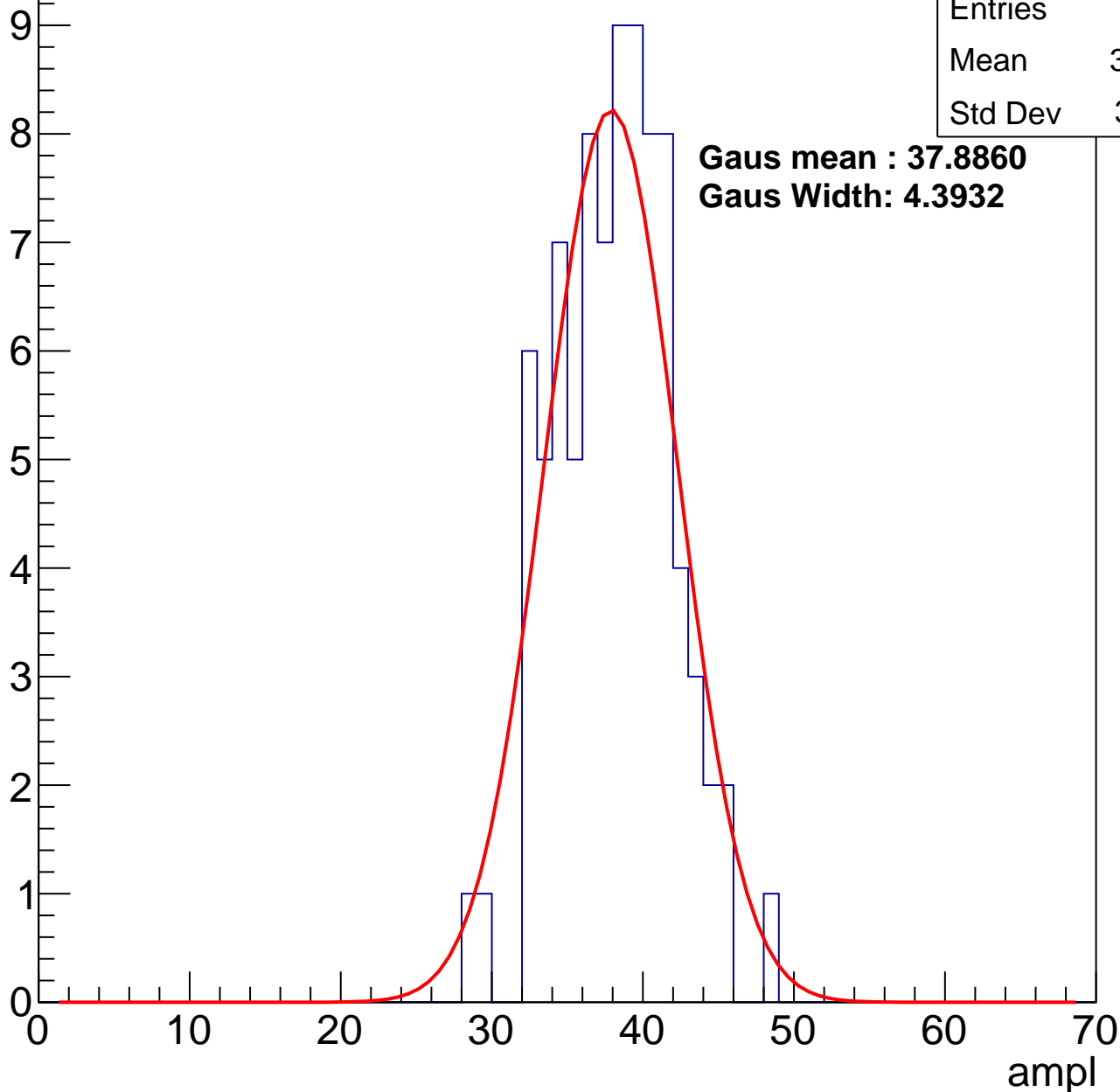
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	86
Mean	37.65
Std Dev	3.781

**Gaus mean : 37.8860**

**Gaus Width: 4.3932**



# B1L103S, U26-ch37, adc2

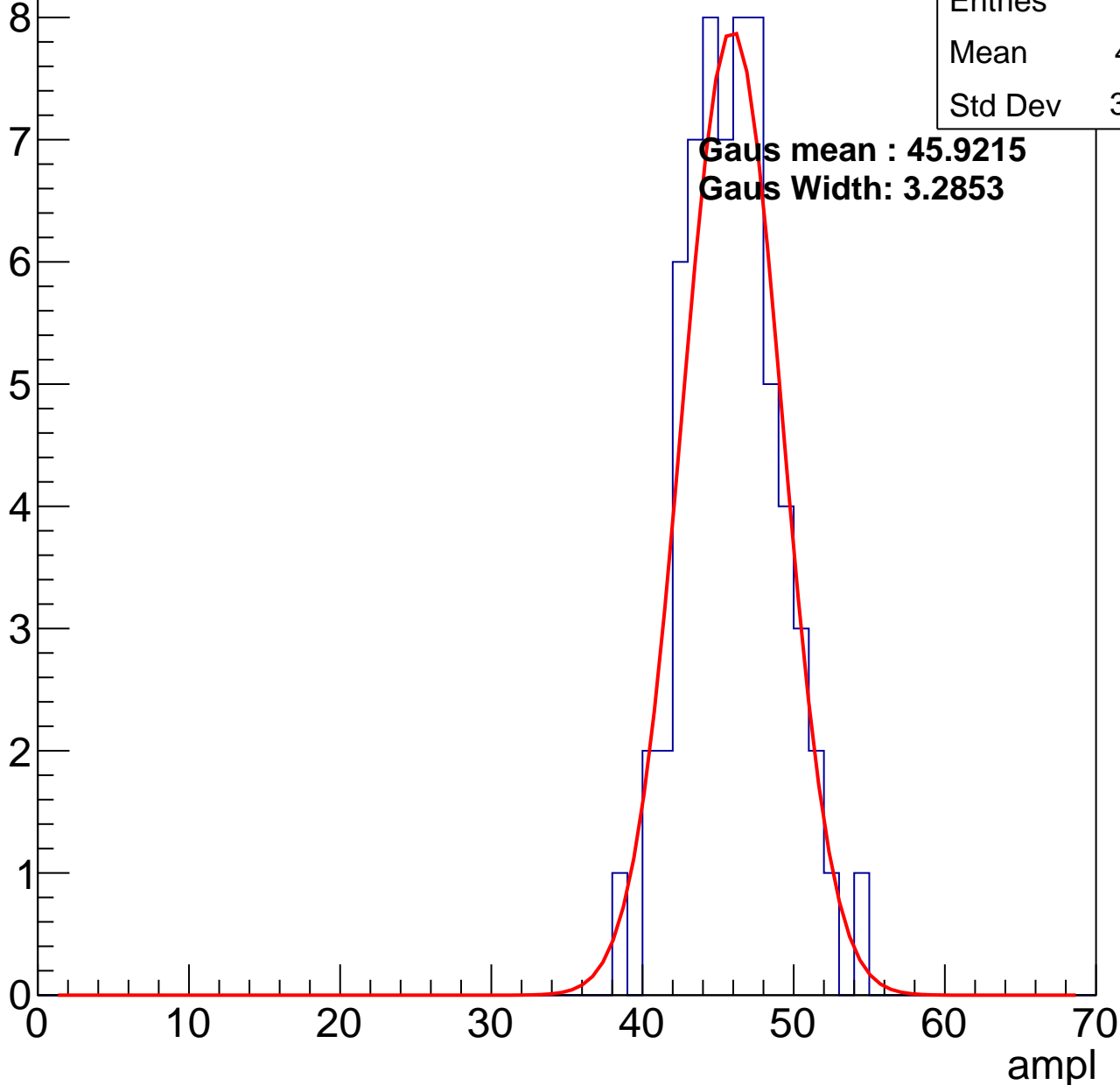
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	45.51
Std Dev	3.114

**Gaus mean : 45.9215**

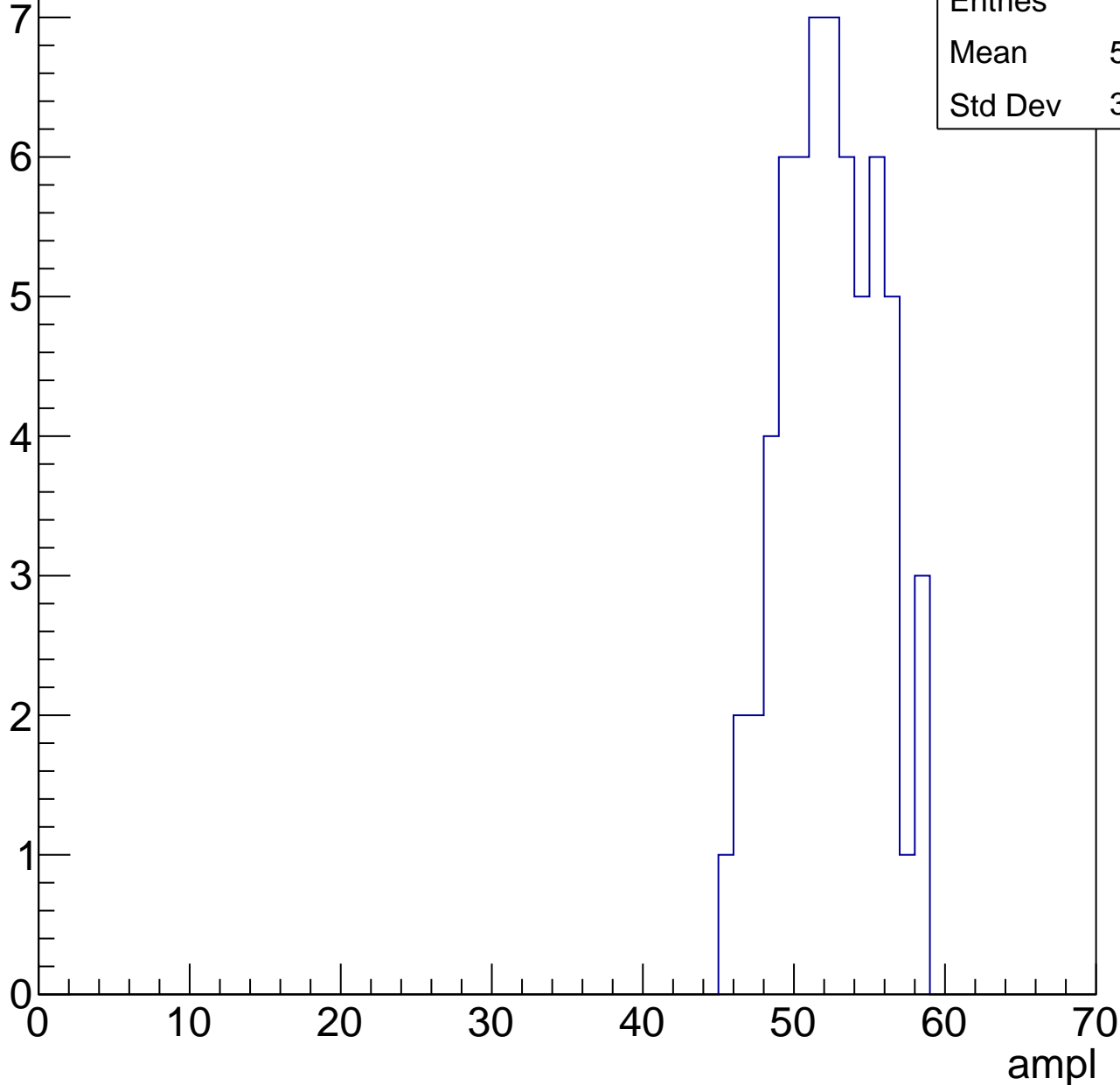
**Gaus Width: 3.2853**



# B1L103S, U26-ch37, adc3

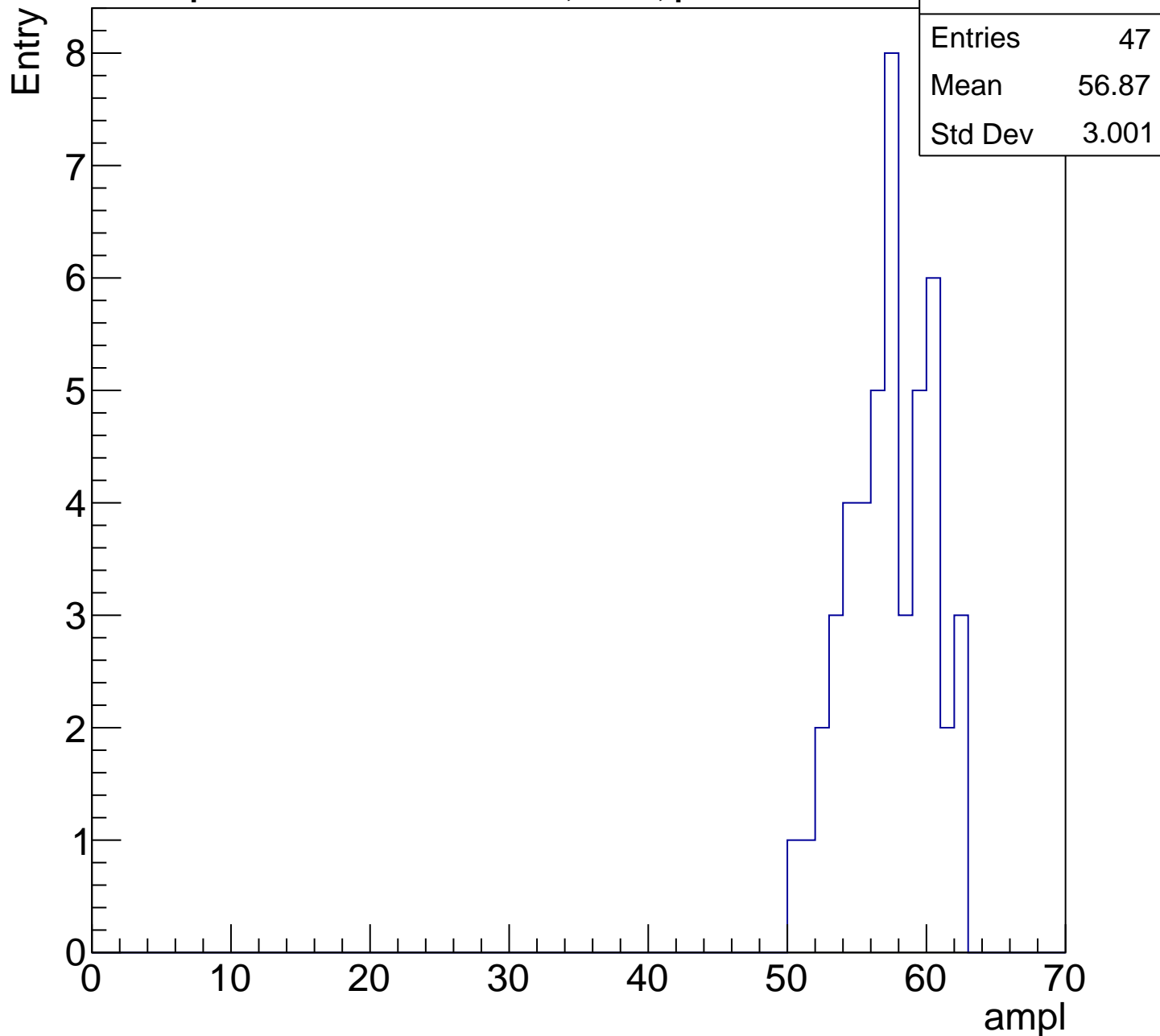
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

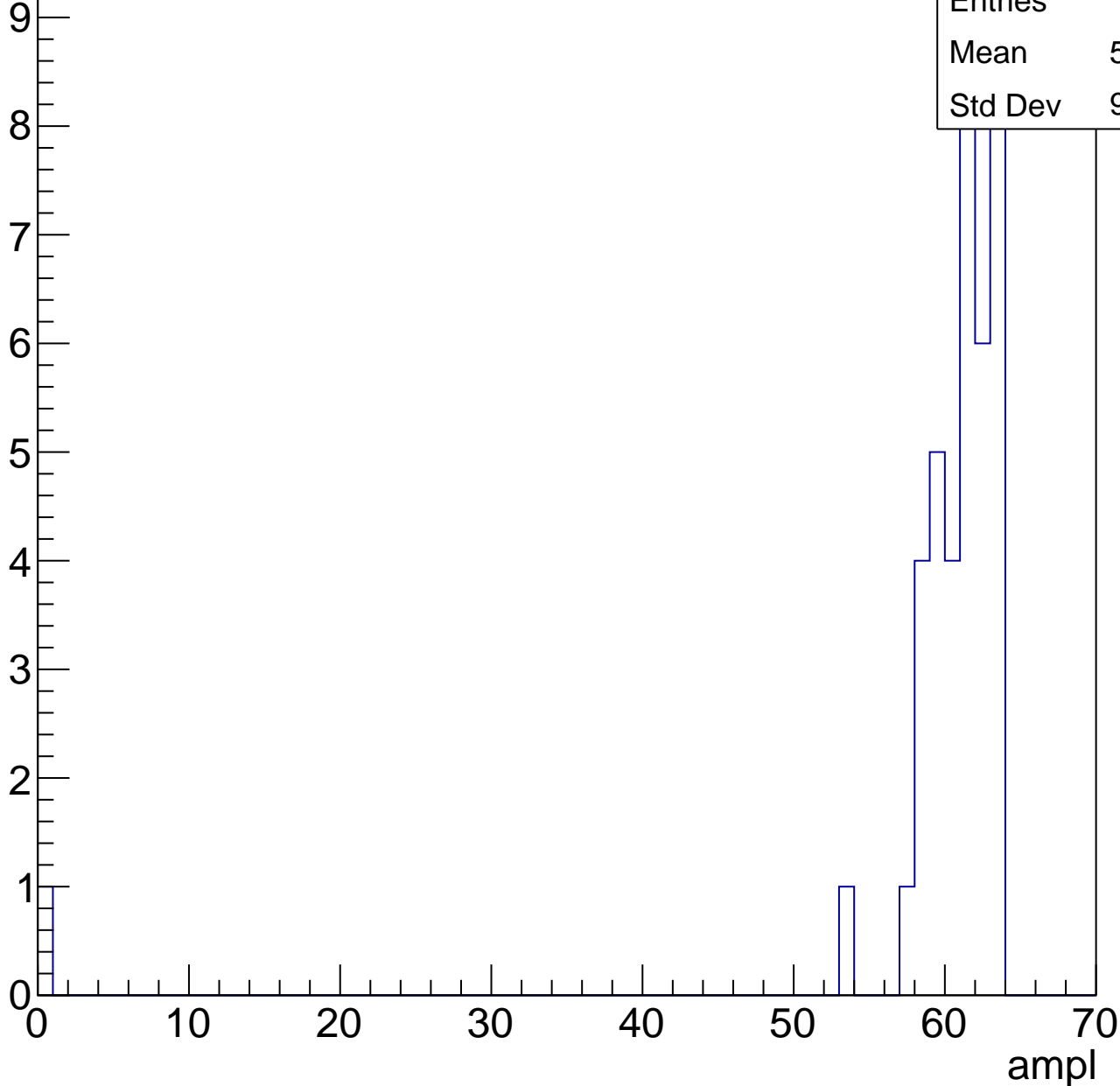


# B1L103S, U26-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	39
Mean	59.08
Std Dev	9.817



# B1L103S, U26-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U26-ch38, adc0

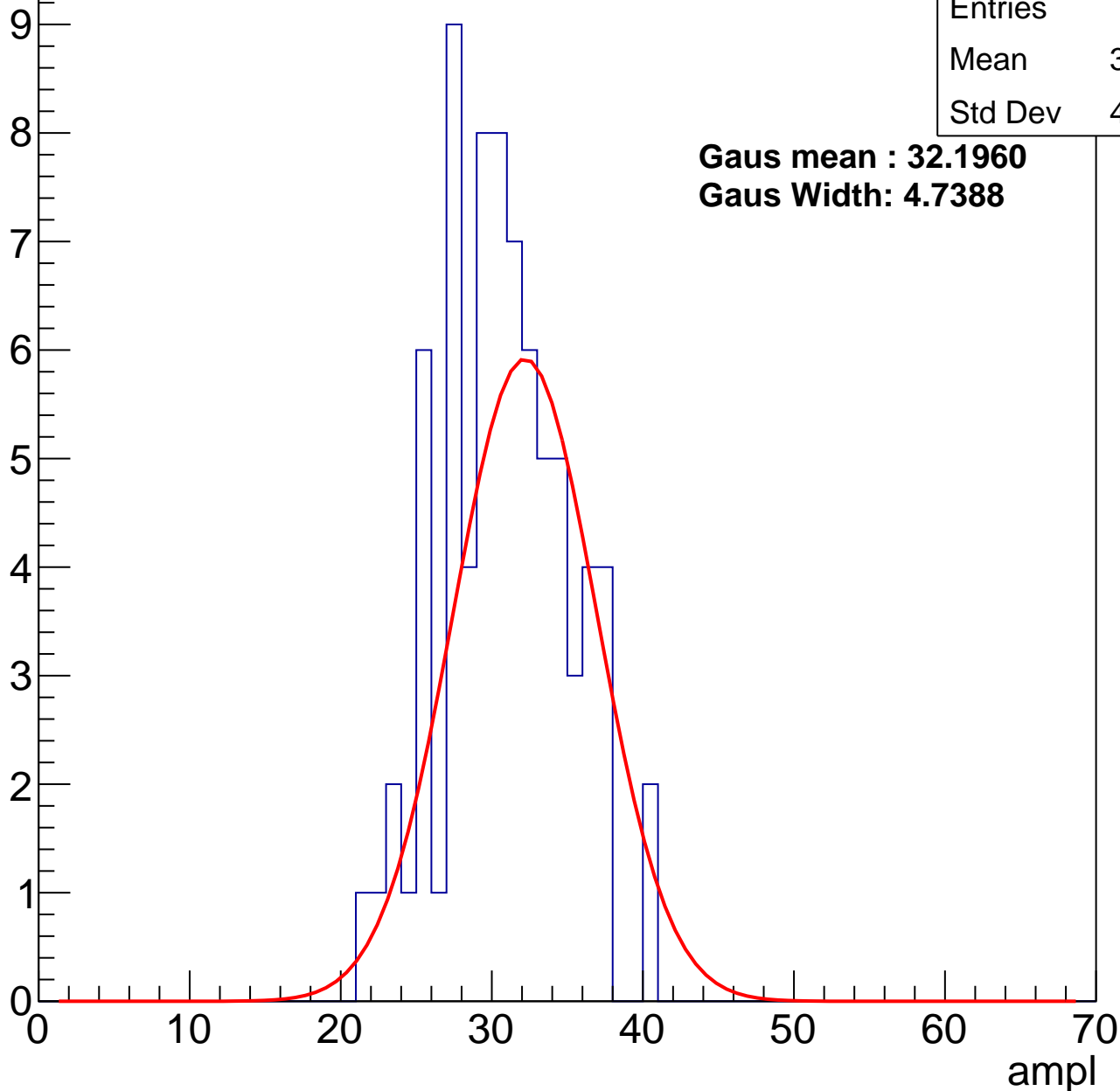
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	30.35
Std Dev	4.127

**Gaus mean : 32.1960**

**Gaus Width: 4.7388**



# B1L103S, U26-ch38, adc1

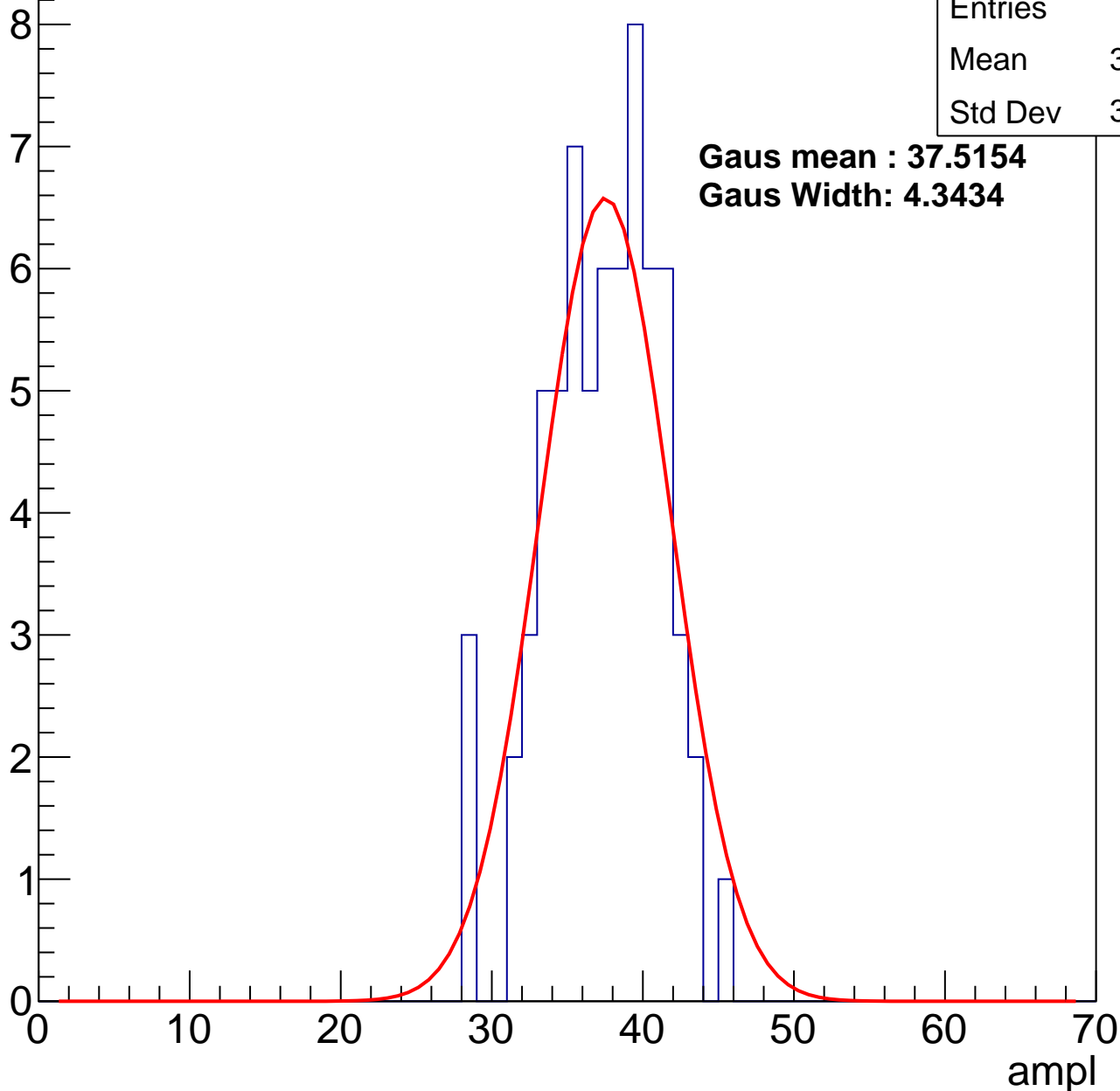
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	36.87
Std Dev	3.729

**Gaus mean : 37.5154**

**Gaus Width: 4.3434**



# B1L103S, U26-ch38, adc2

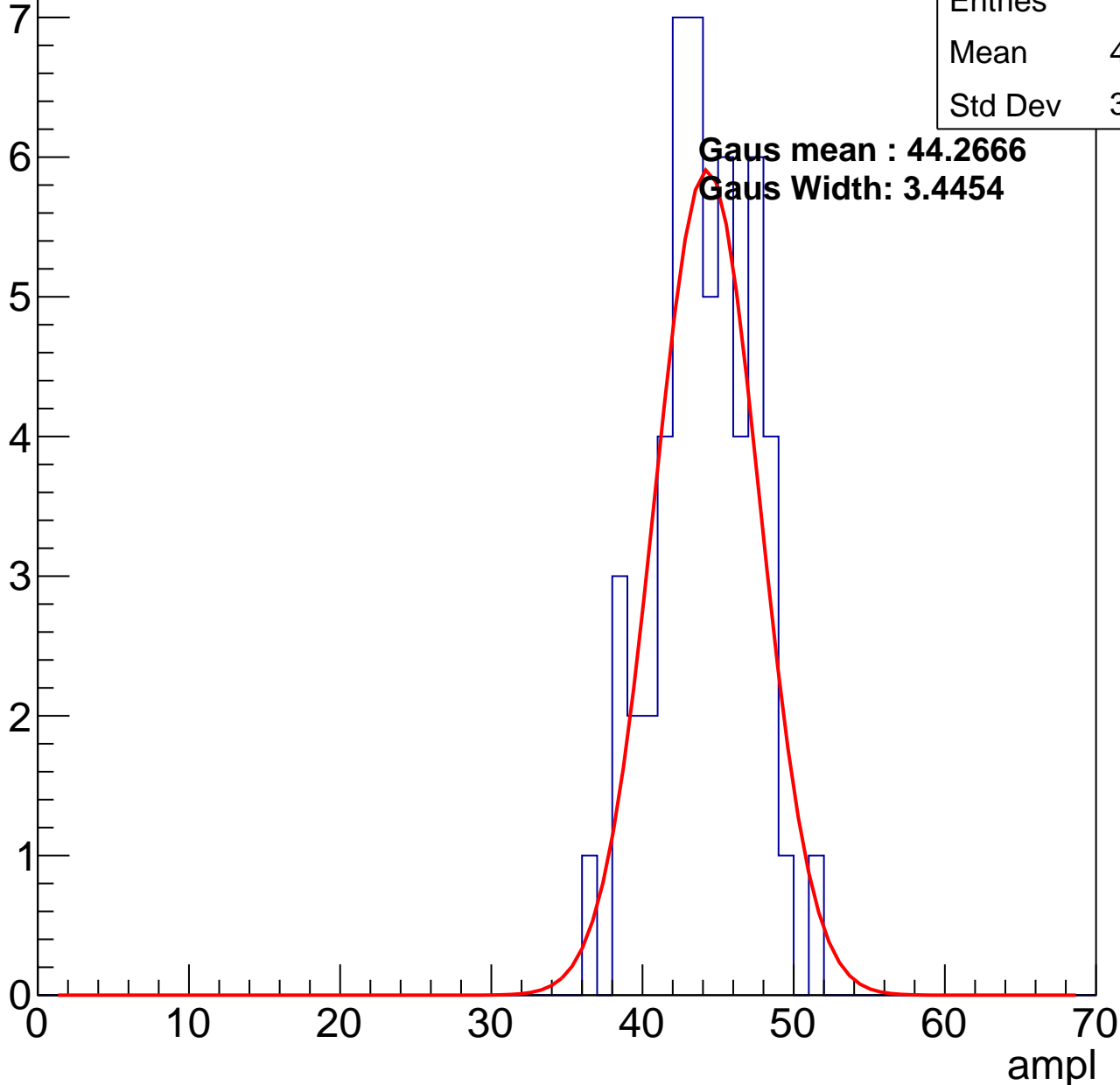
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	43.68
Std Dev	3.173

**Gaus mean : 44.2666**

**Gaus Width: 3.4454**

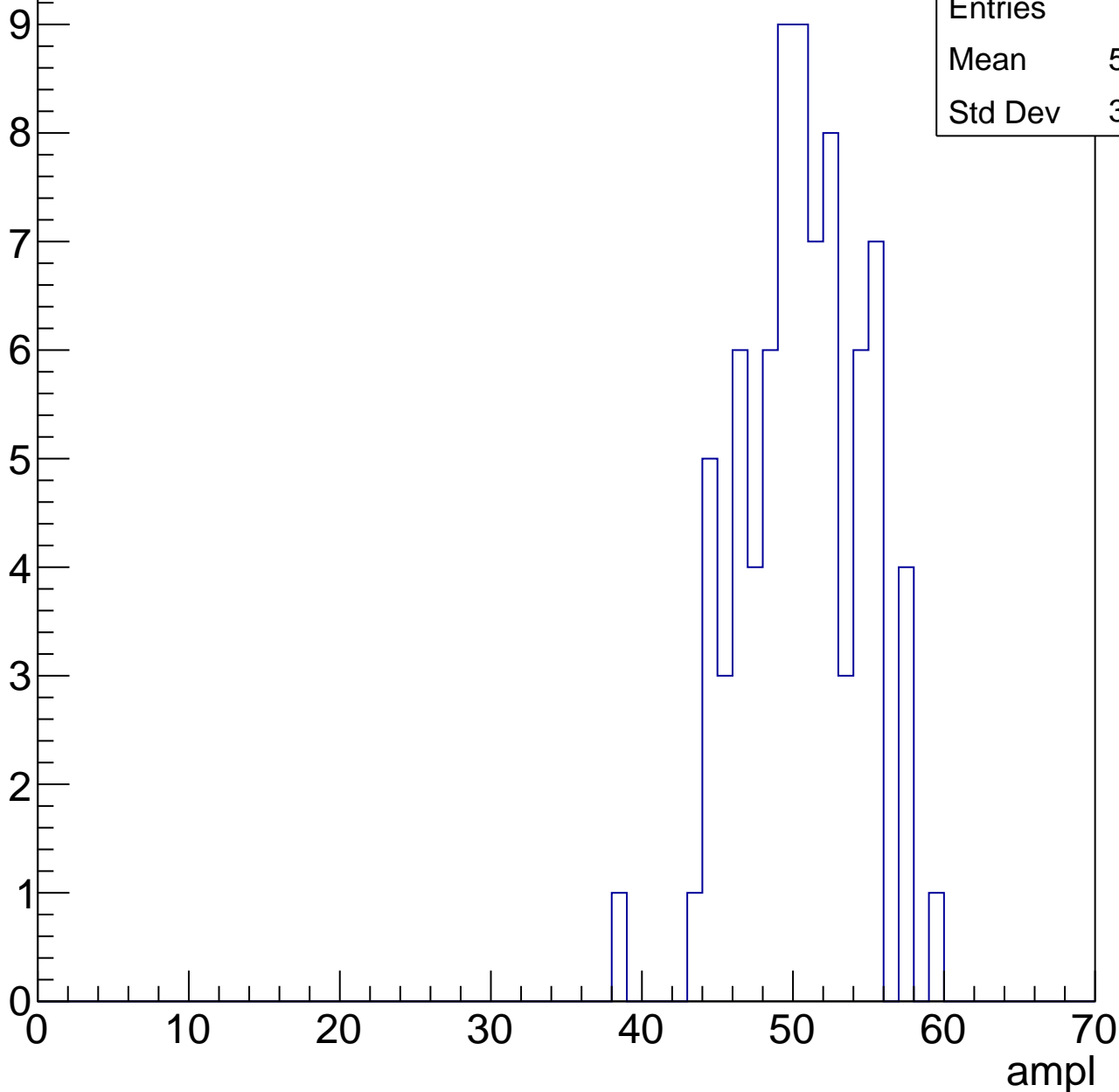


# B1L103S, U26-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	50.09
Std Dev	3.915

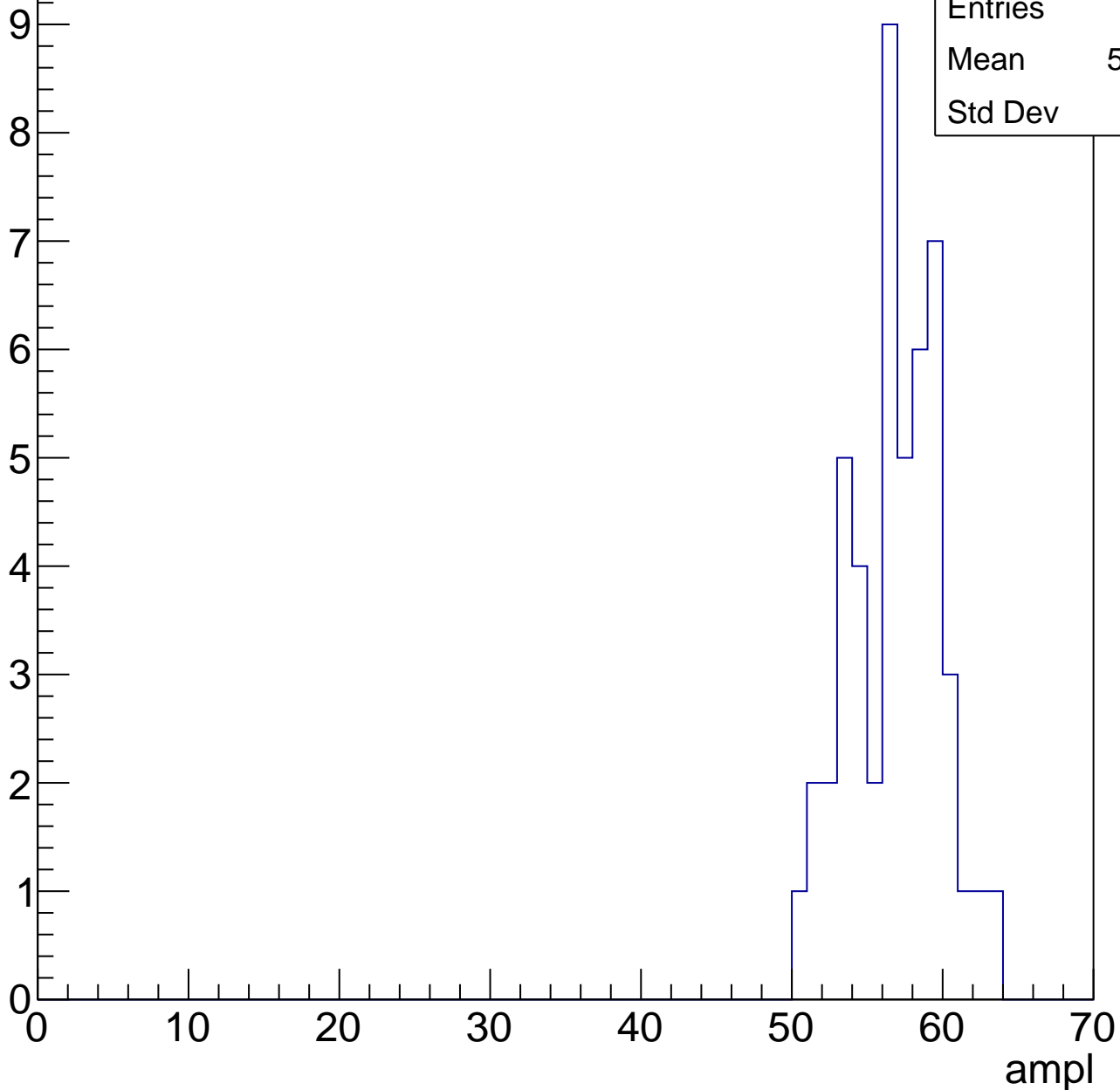


# B1L103S, U26-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	56.39
Std Dev	2.94

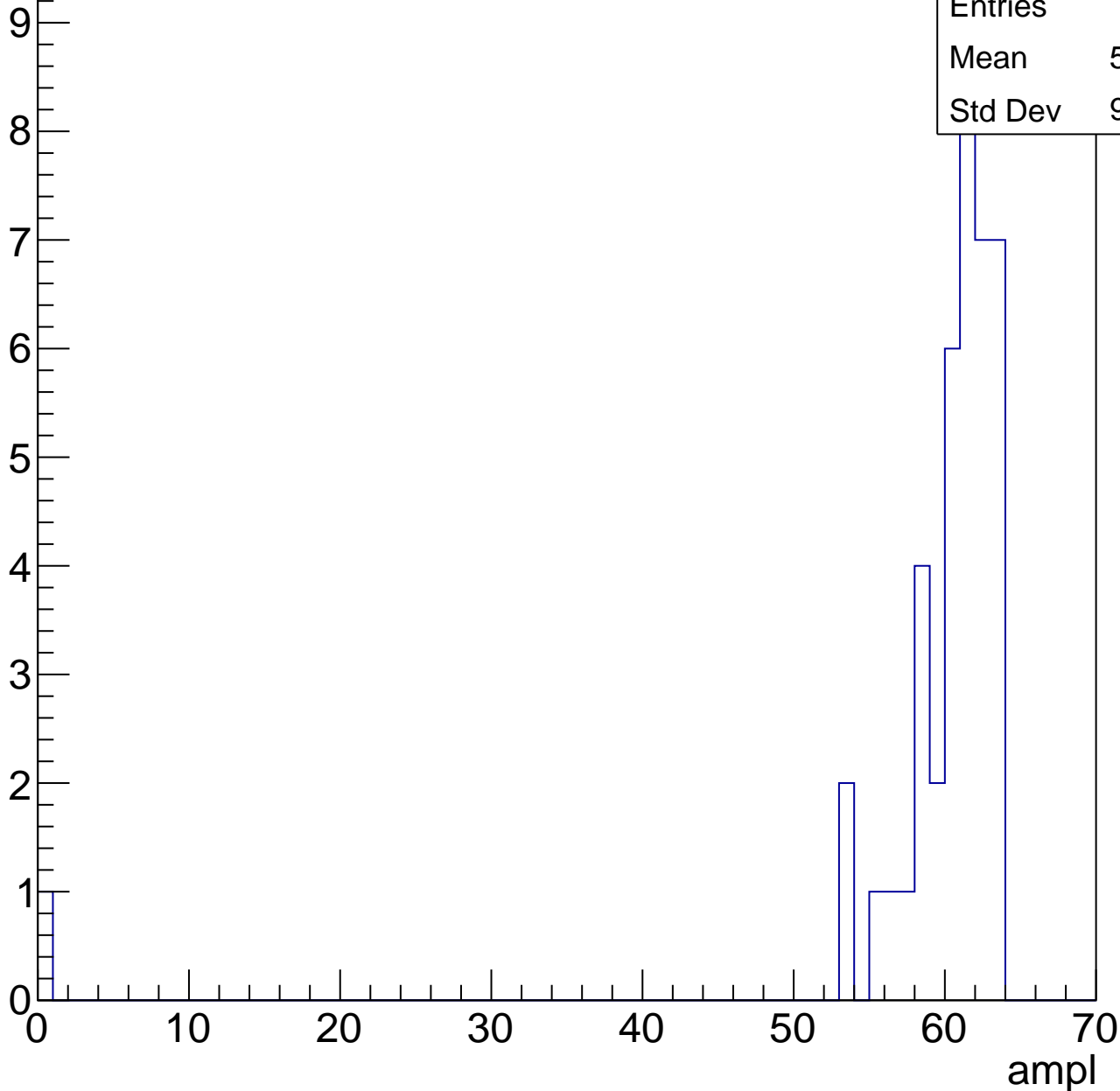


# B1L103S, U26-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	41
Mean	58.73
Std Dev	9.627



# B1L103S, U26-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch39, adc0

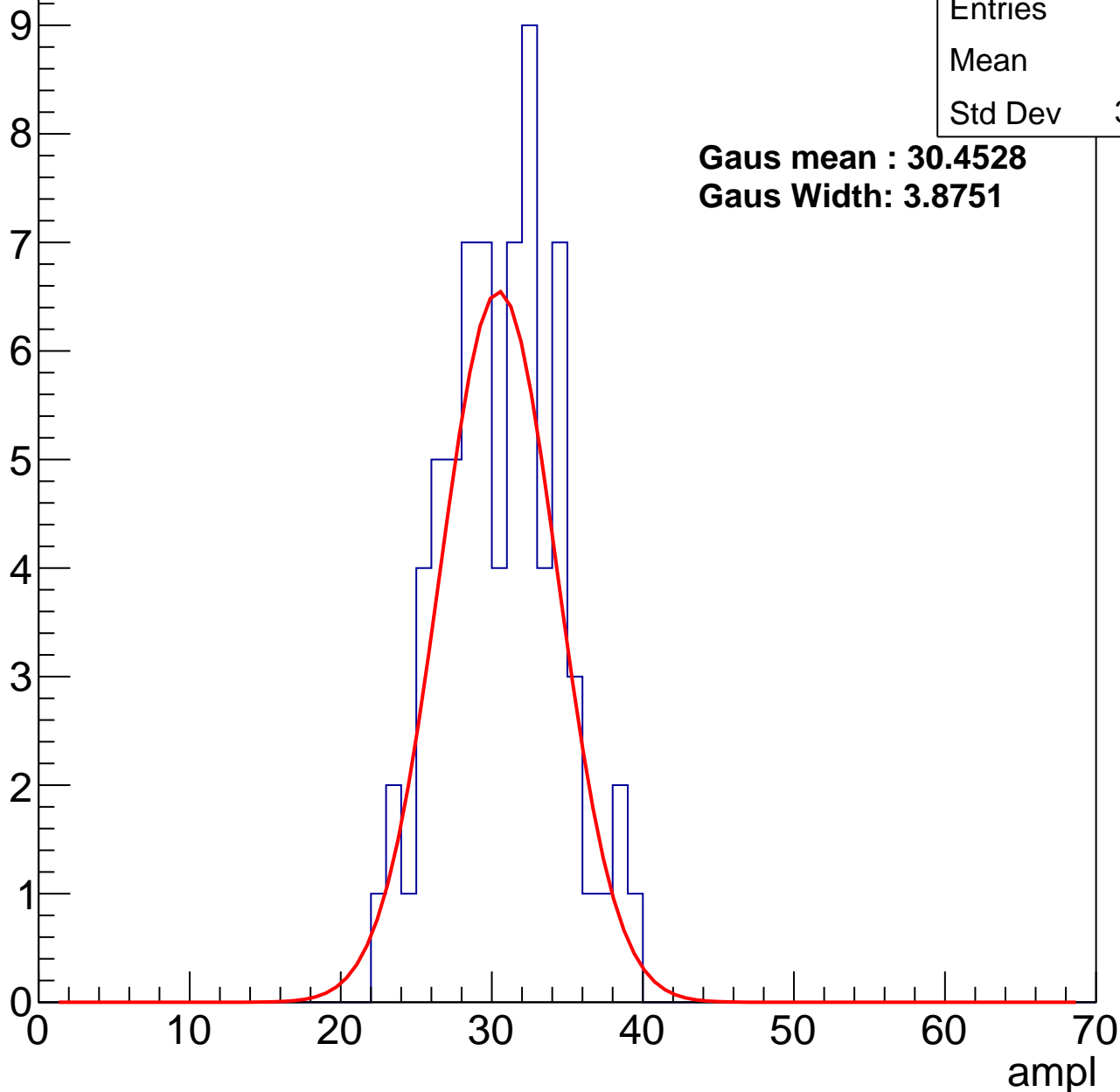
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	30.2
Std Dev	3.781

**Gaus mean : 30.4528**

**Gaus Width: 3.8751**



# B1L103S, U26-ch39, adc1

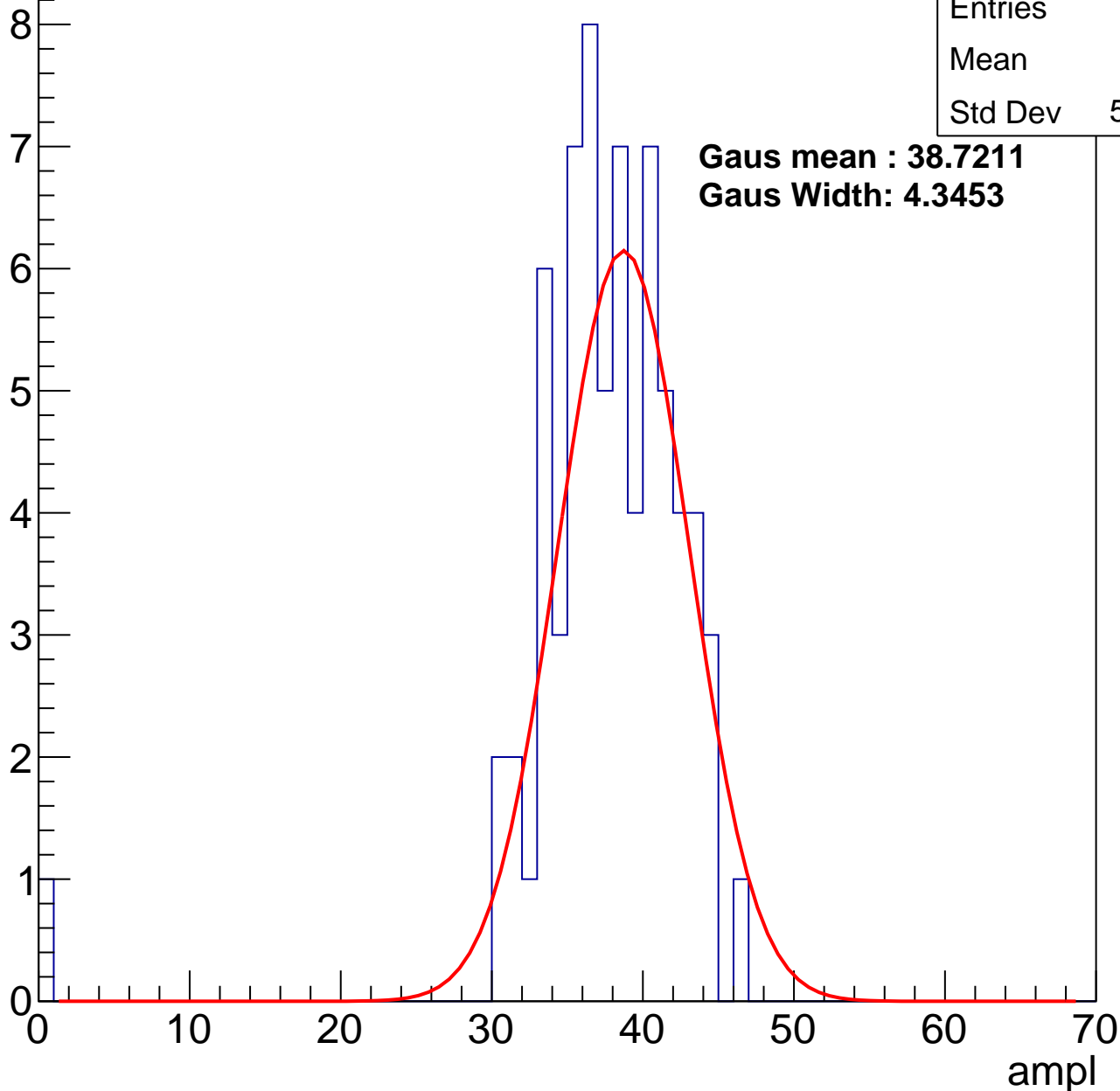
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	37.1
Std Dev	5.807

**Gaus mean : 38.7211**

**Gaus Width: 4.3453**



# B1L103S, U26-ch39, adc2

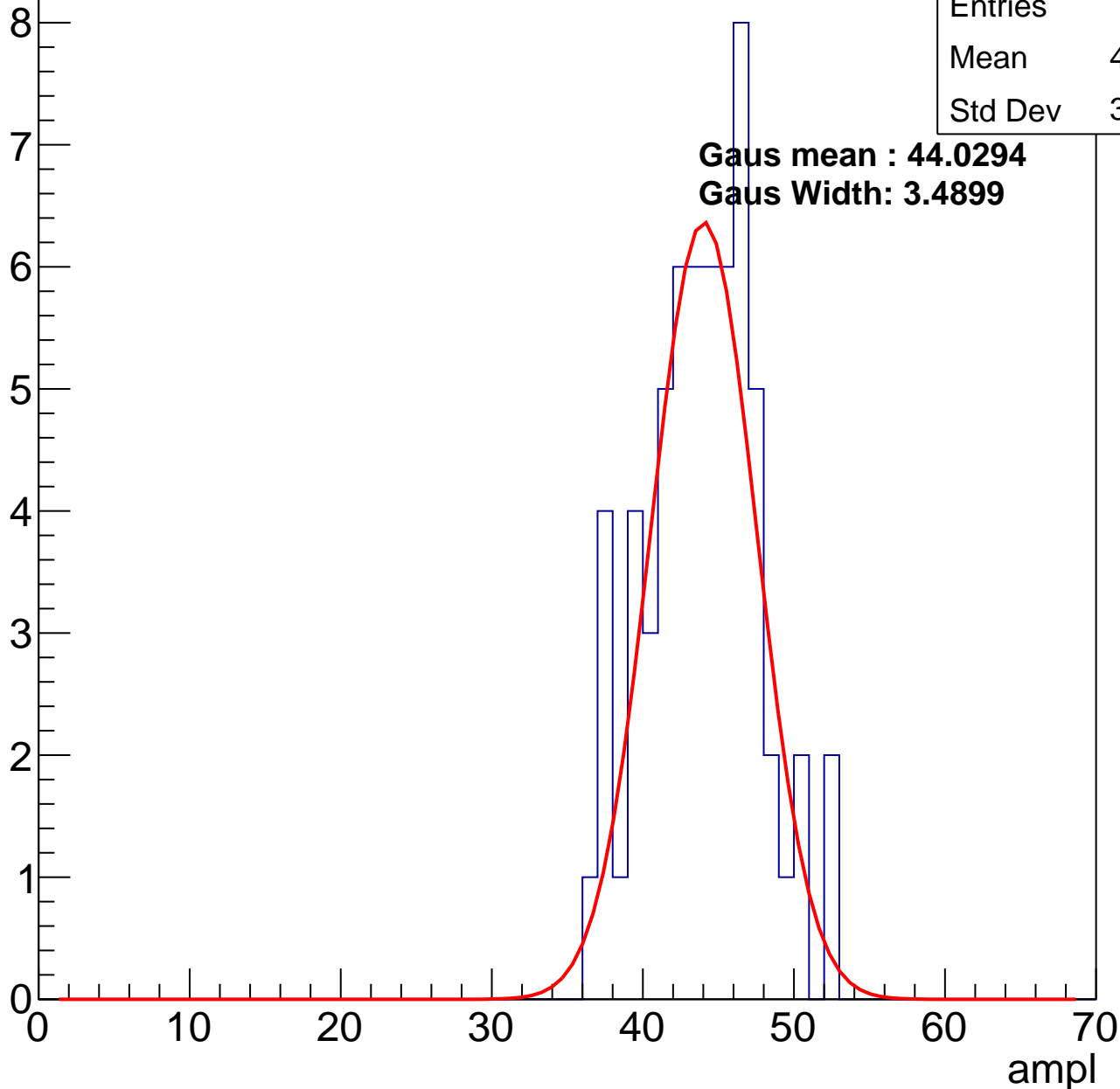
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	43.53
Std Dev	3.693

**Gaus mean : 44.0294**

**Gaus Width: 3.4899**

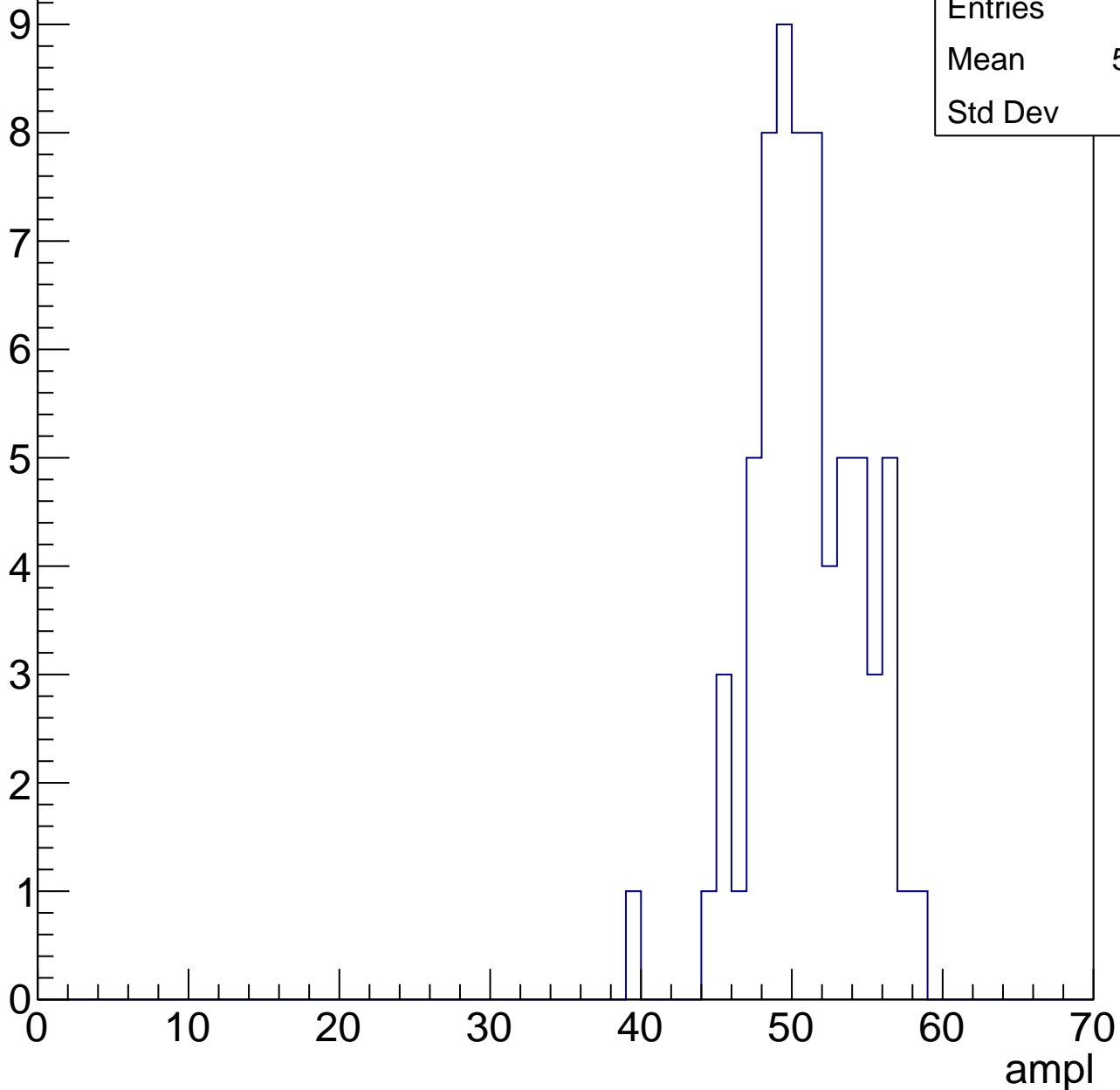


# B1L103S, U26-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	50.51
Std Dev	3.5

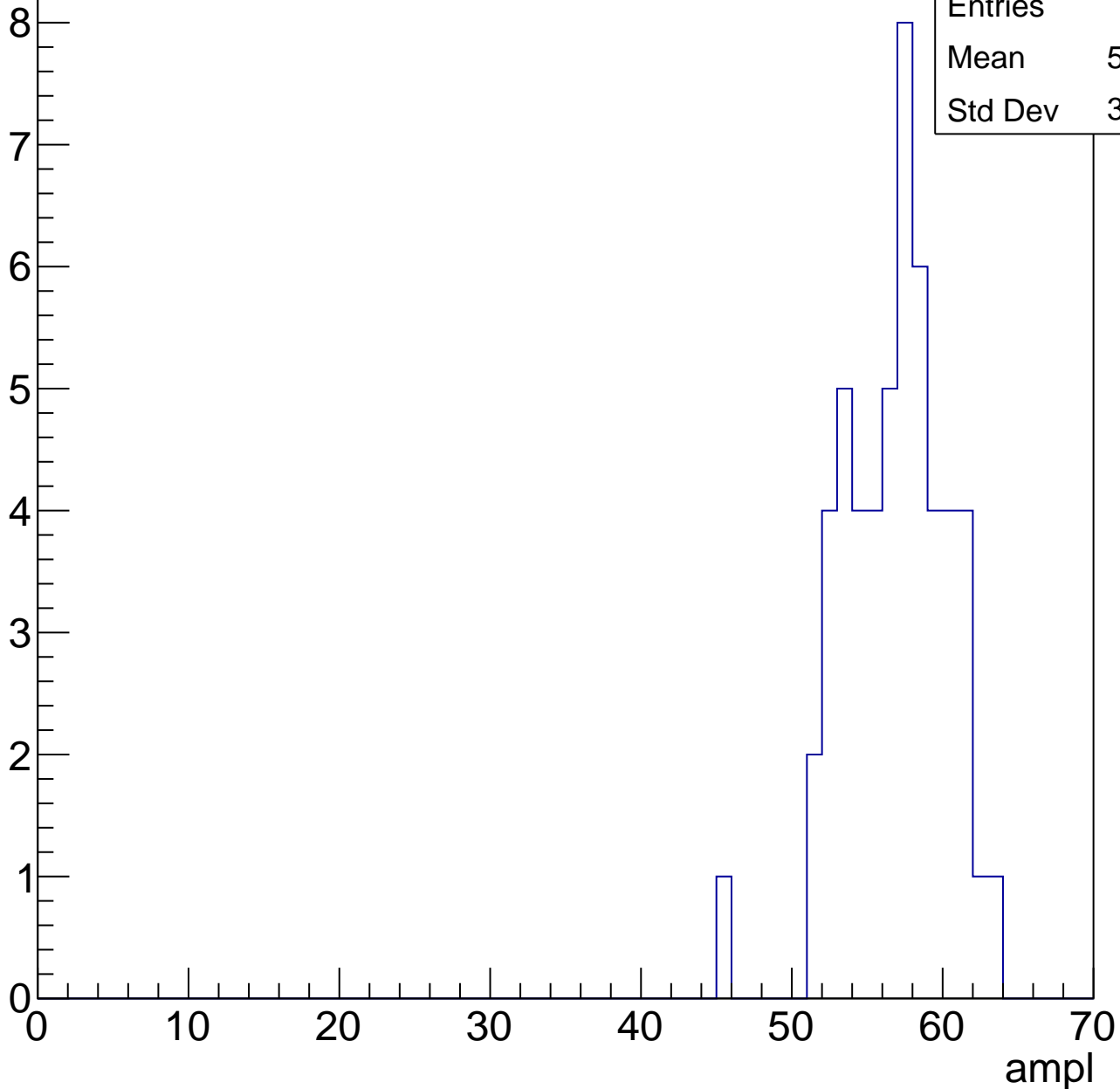


# B1L103S, U26-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	56.32
Std Dev	3.397

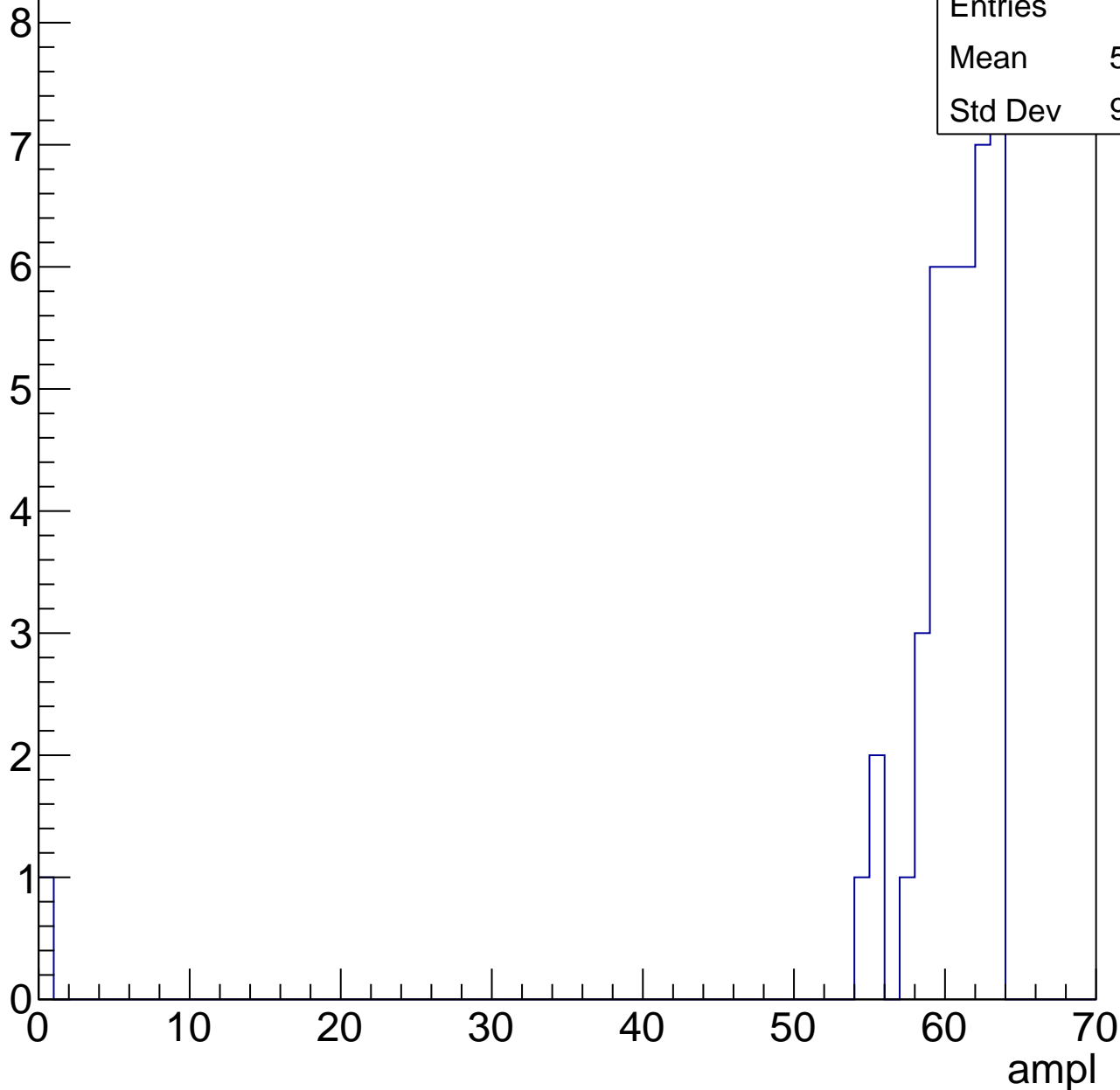


# B1L103S, U26-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

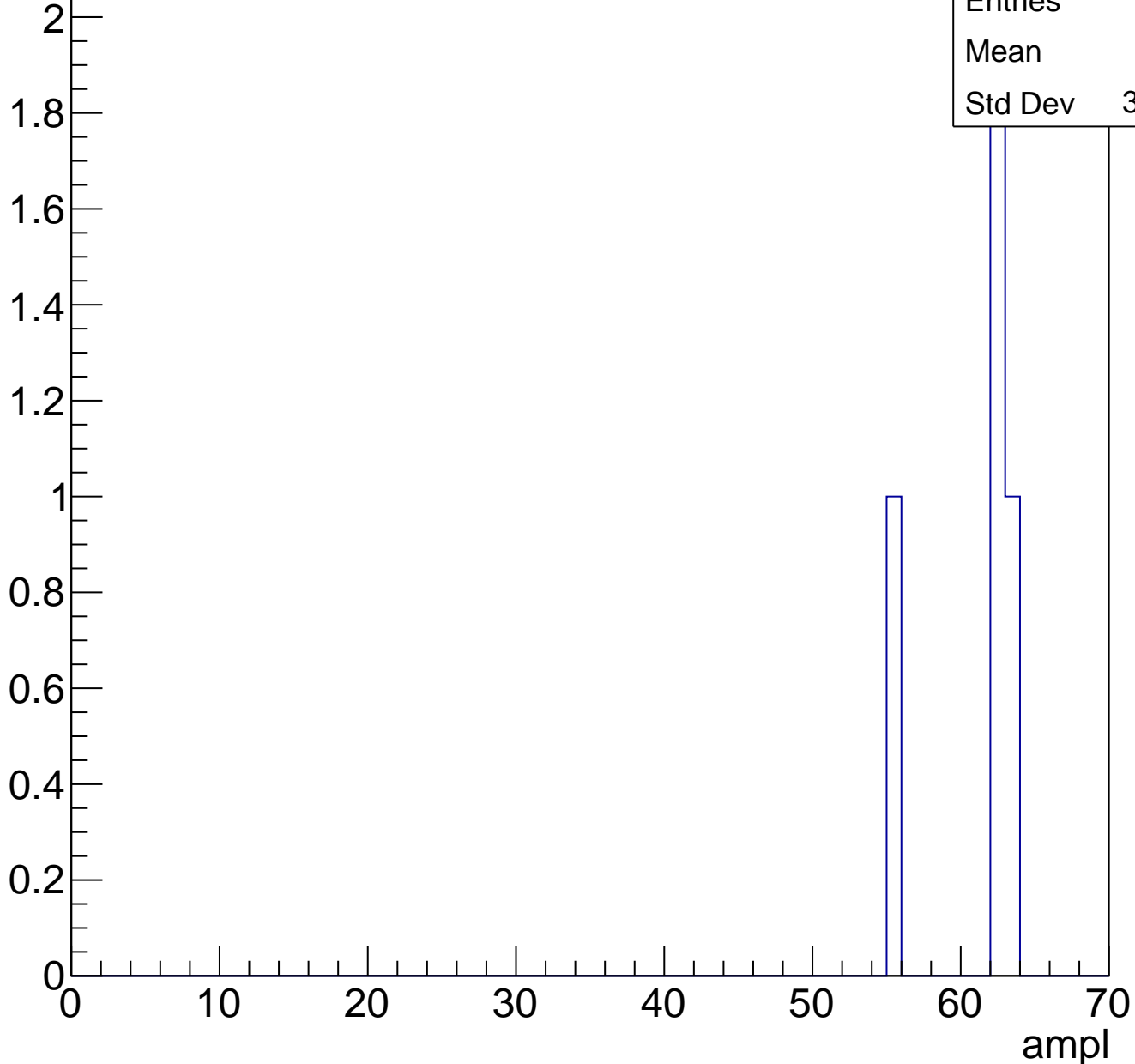
Entries	41
Mean	58.85
Std Dev	9.583



# B1L103S, U26-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch40, adc0

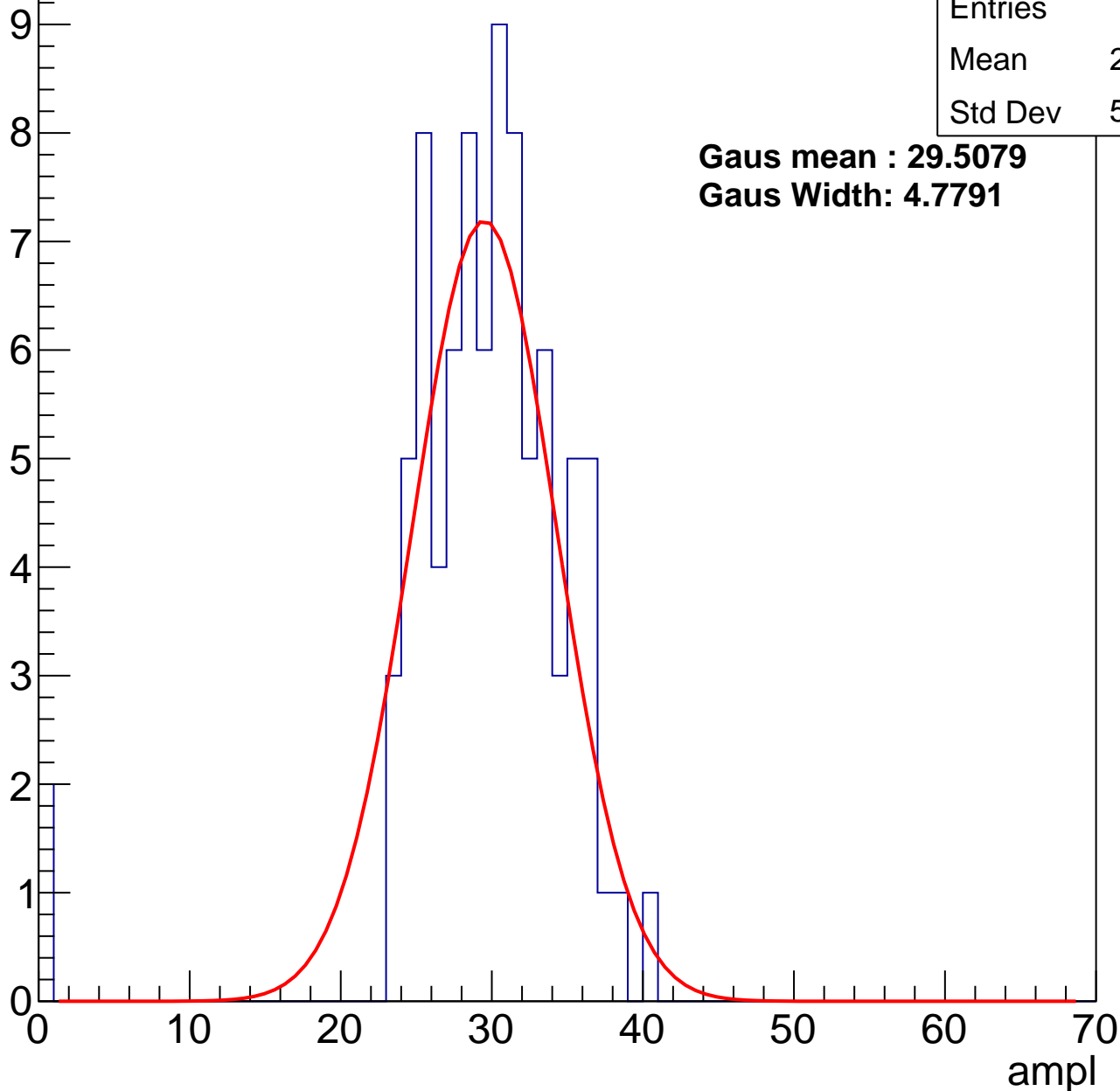
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	86
Mean	29.08
Std Dev	5.963

**Gaus mean : 29.5079**

**Gaus Width: 4.7791**



# B1L103S, U26-ch40, adc1

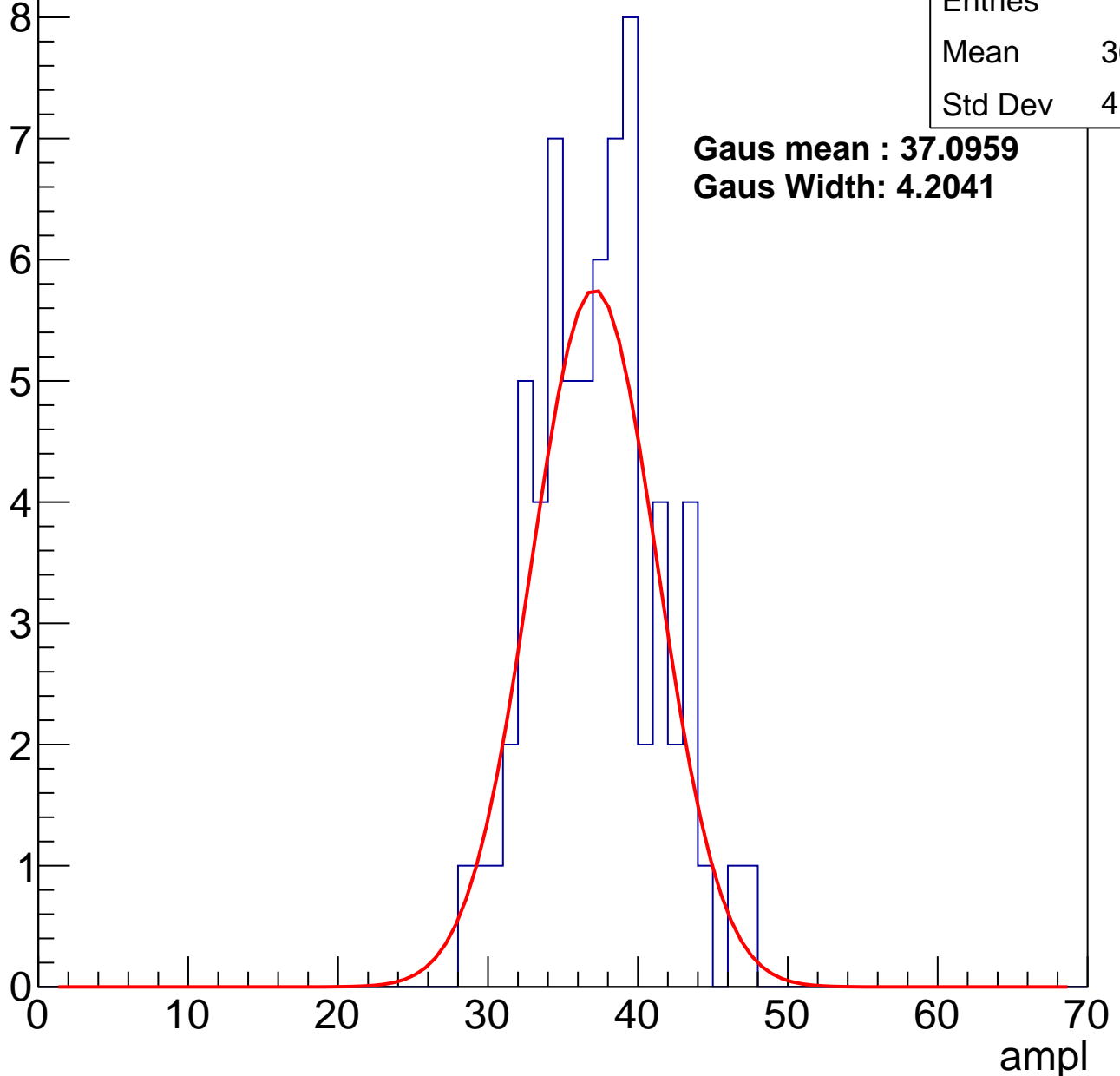
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	36.88
Std Dev	4.028

**Gaus mean : 37.0959**

**Gaus Width: 4.2041**



# B1L103S, U26-ch40, adc2

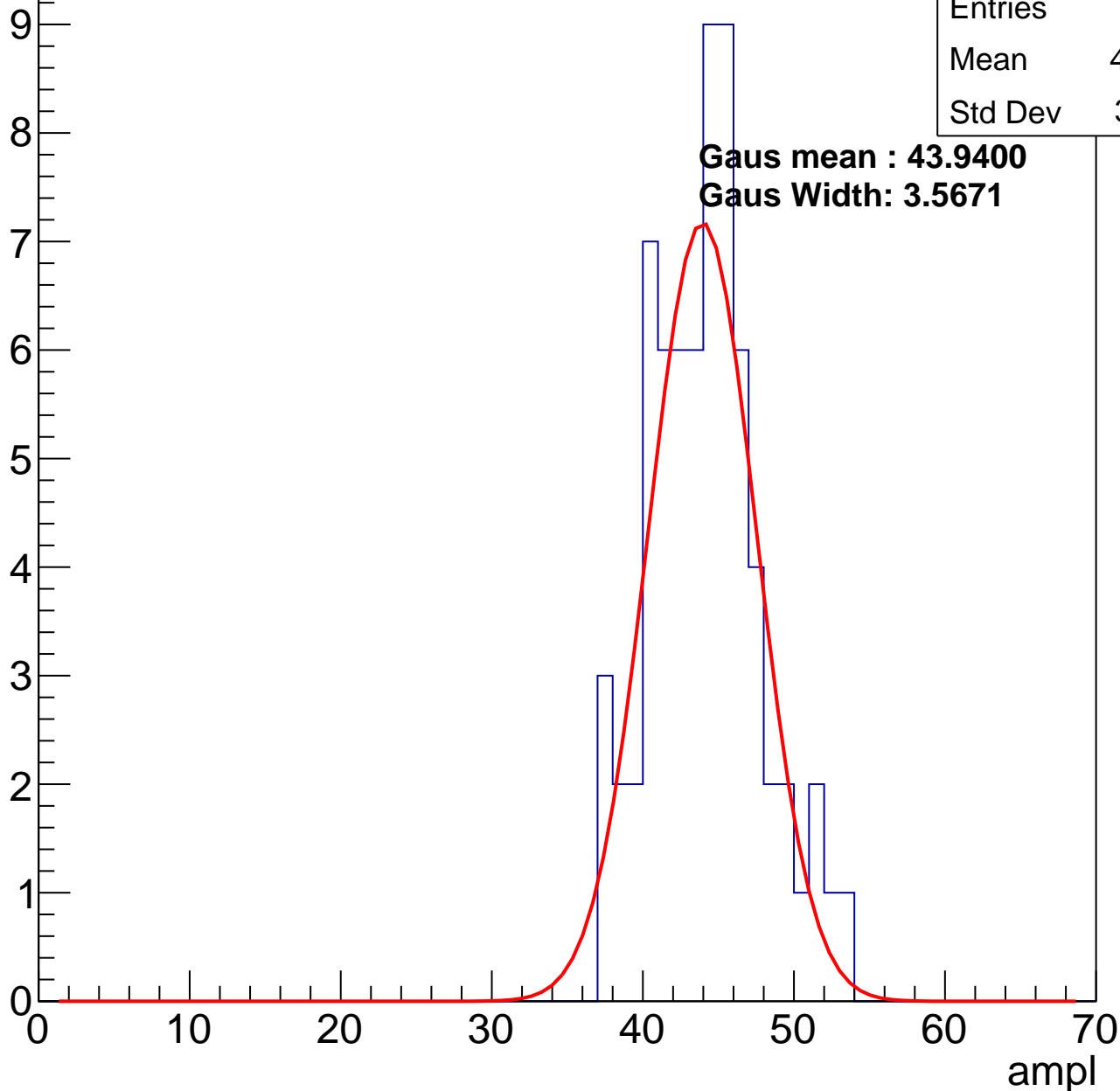
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	43.72
Std Dev	3.591

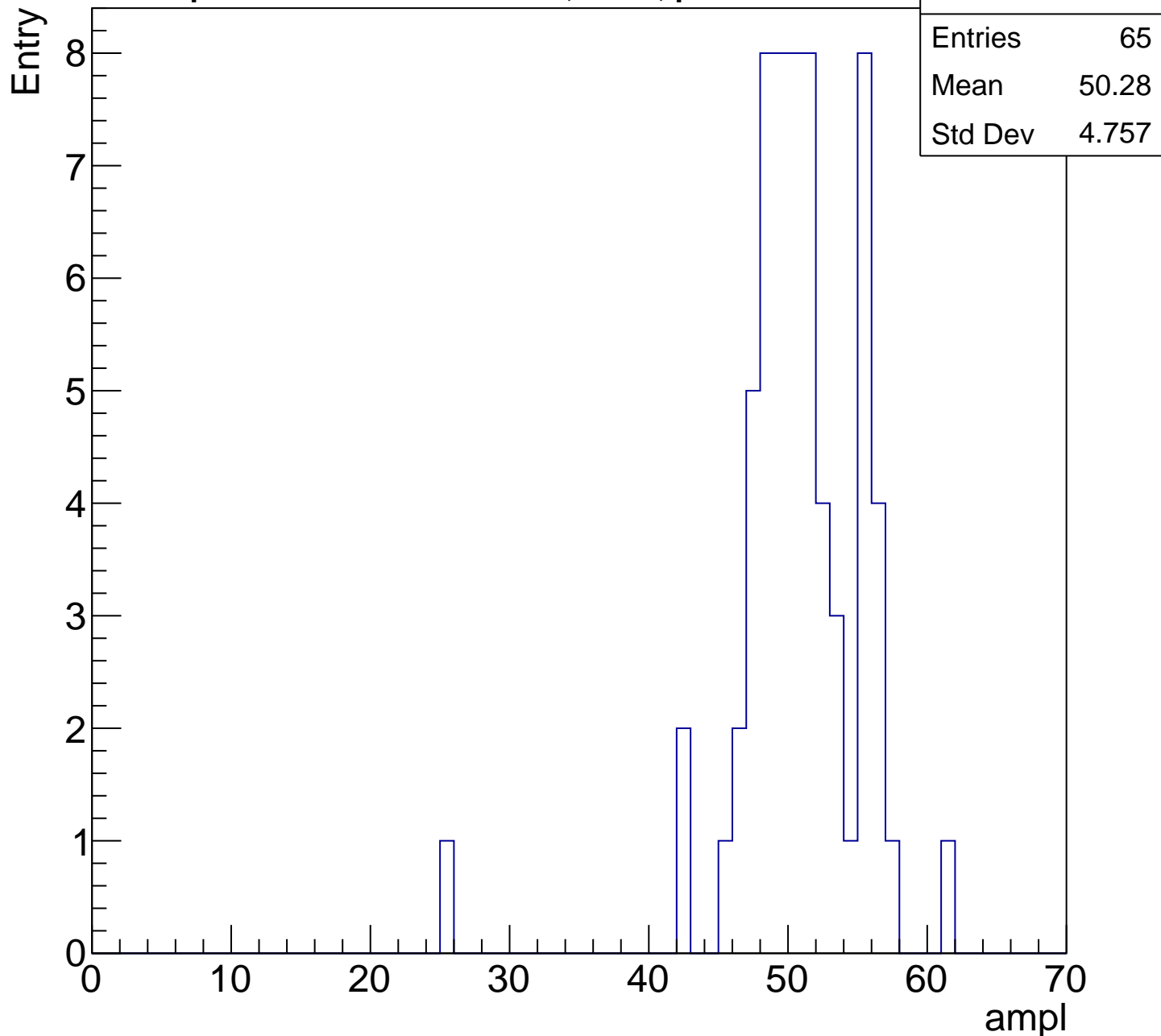
**Gaus mean : 43.9400**

**Gaus Width: 3.5671**



# B1L103S, U26-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

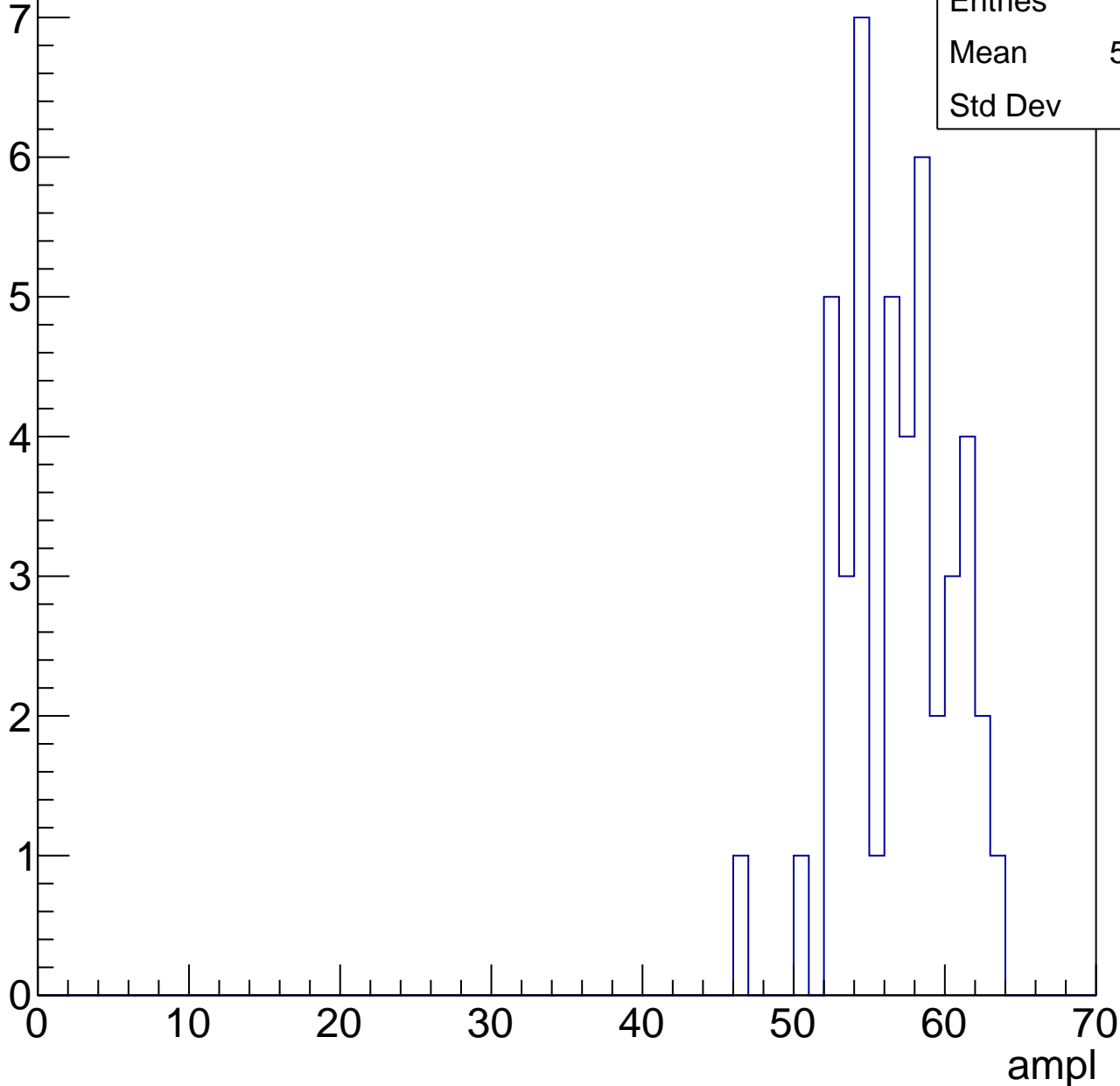


# B1L103S, U26-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	56.29
Std Dev	3.6

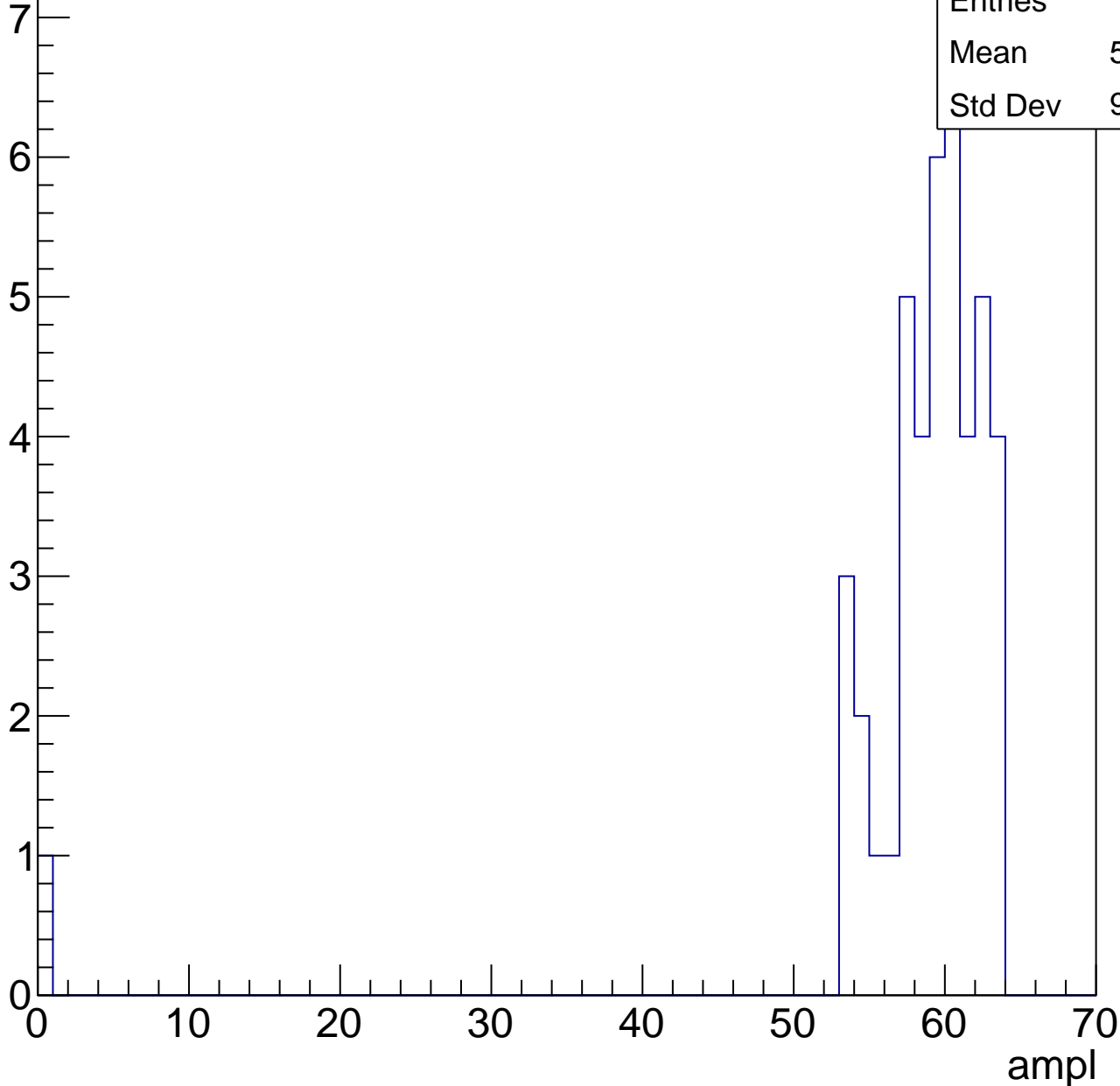


# B1L103S, U26-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	43
Mean	57.56
Std Dev	9.314

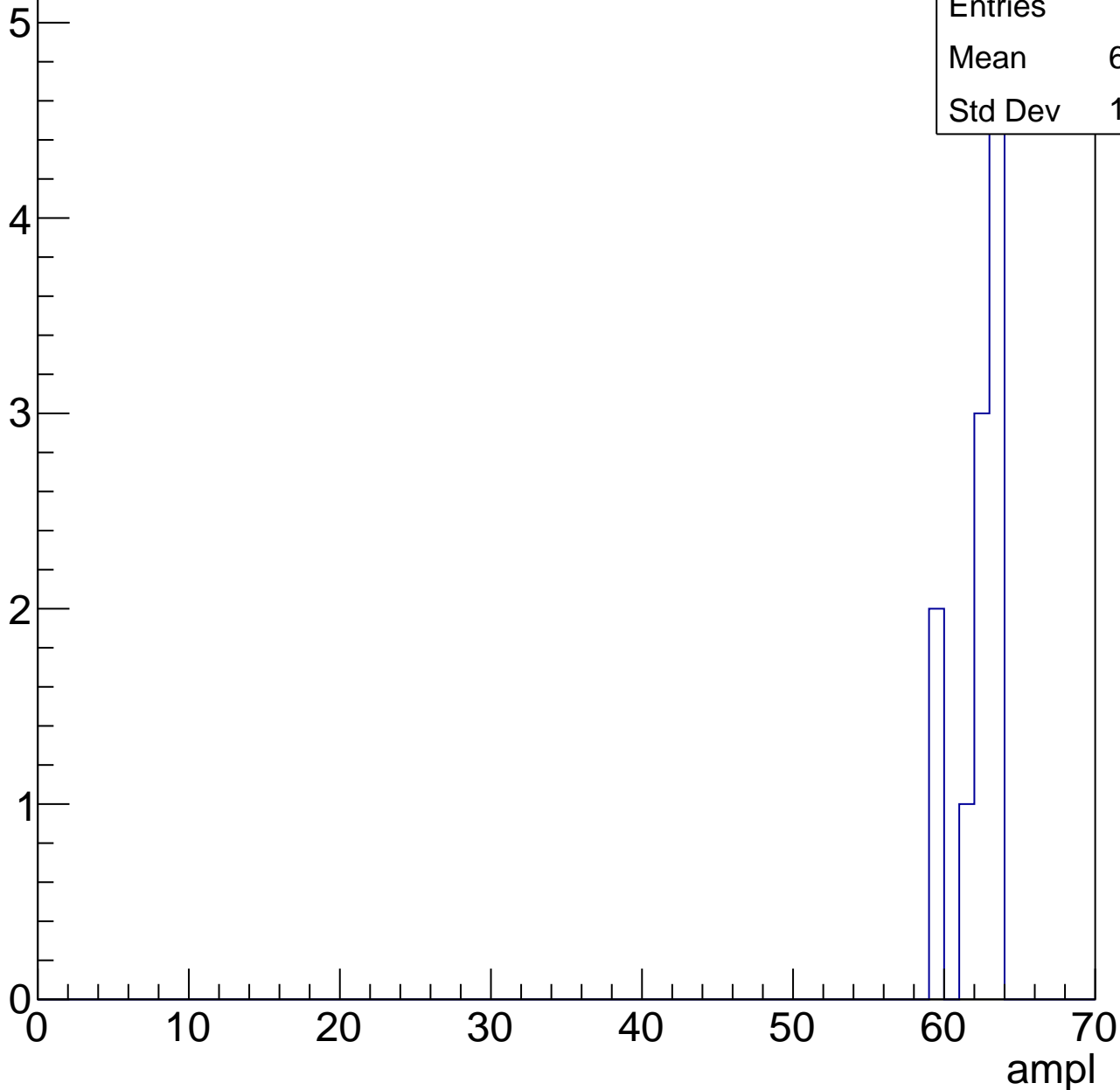


# B1L103S, U26-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	11
Mean	61.82
Std Dev	1.466





# B1L103S, U26-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U26-ch41, adc0

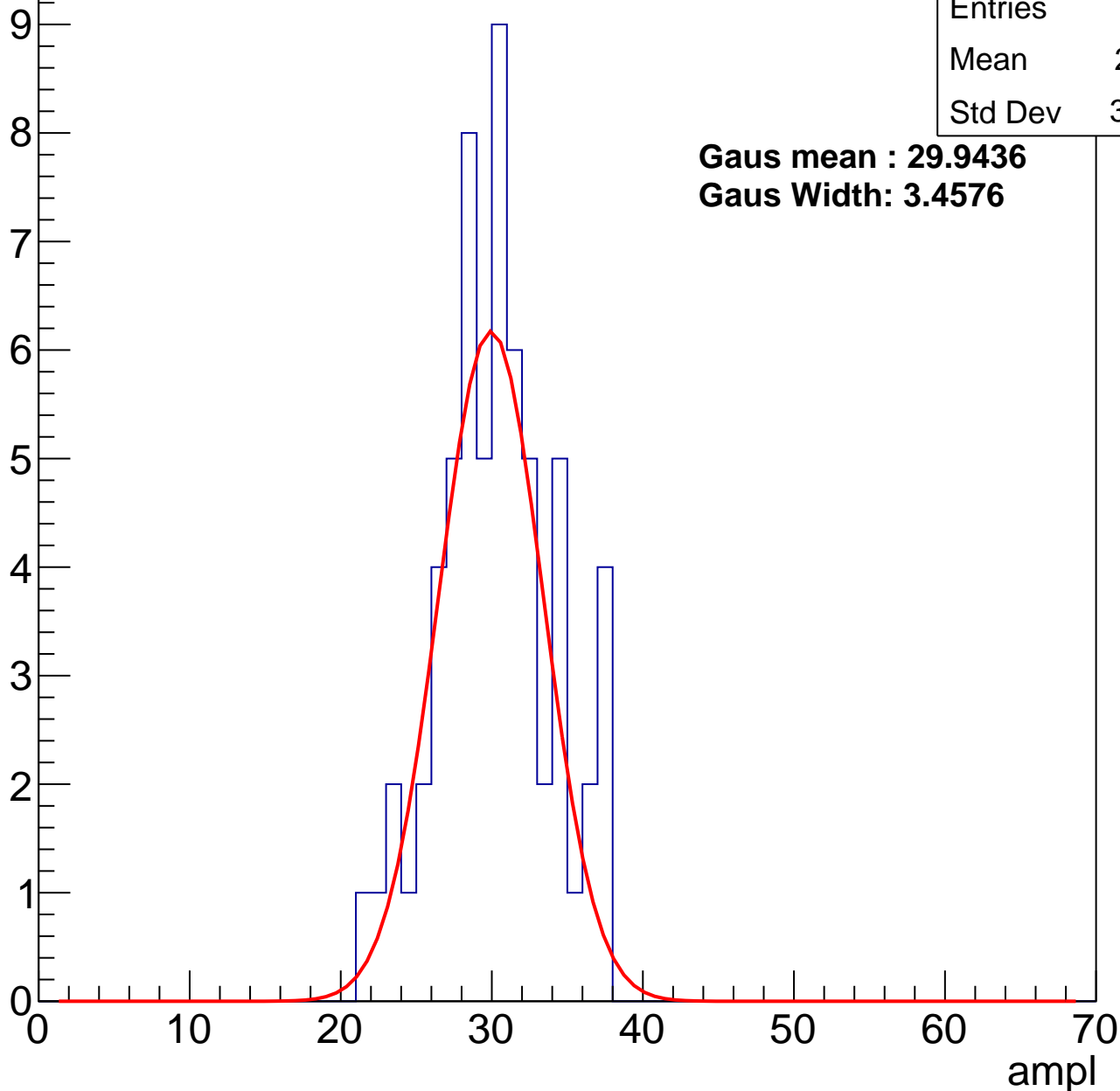
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	29.81
Std Dev	3.758

**Gaus mean : 29.9436**

**Gaus Width: 3.4576**



# B1L103S, U26-ch41, adc1

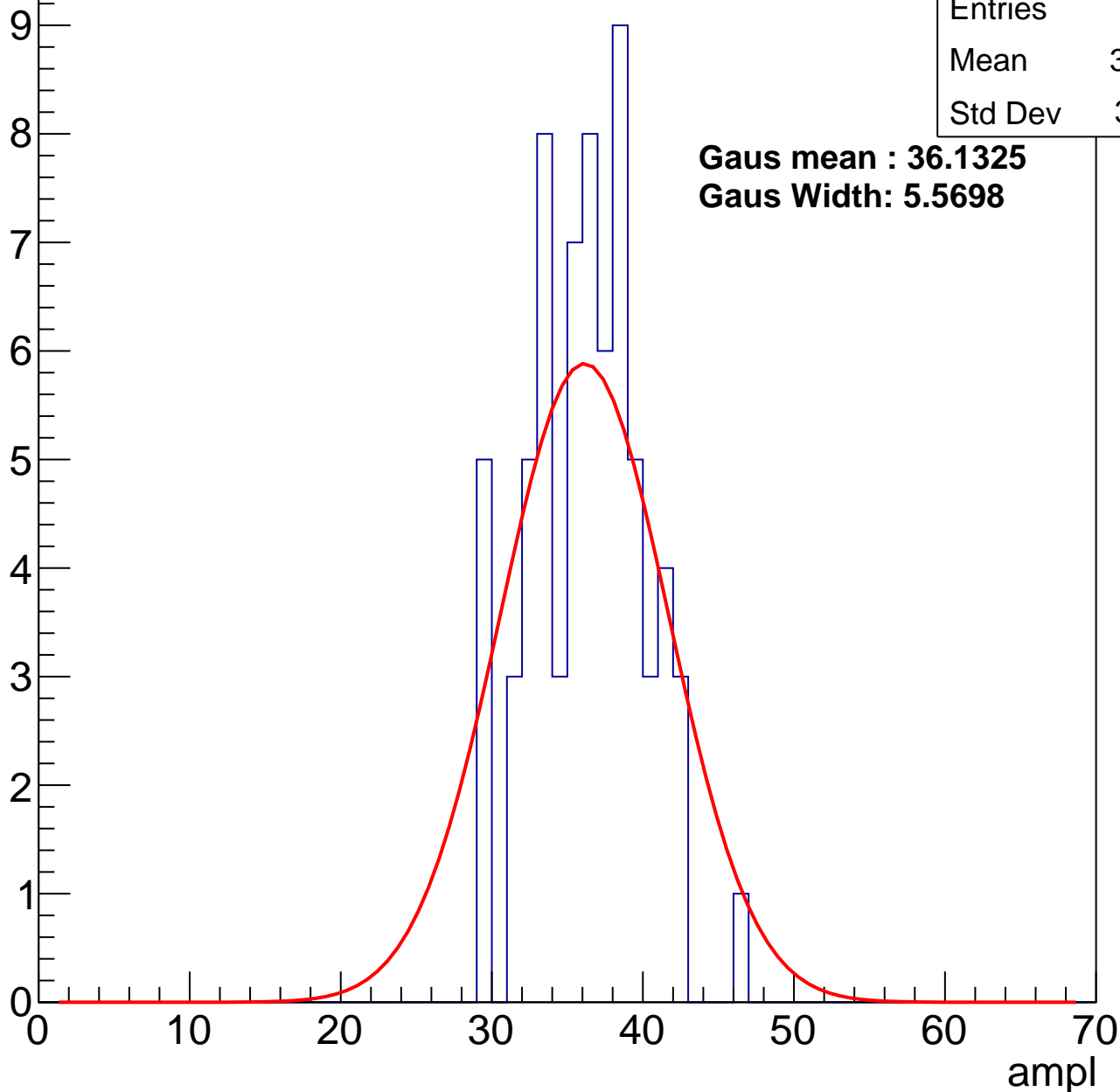
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	35.89
Std Dev	3.651

**Gaus mean : 36.1325**

**Gaus Width: 5.5698**



# B1L103S, U26-ch41, adc2

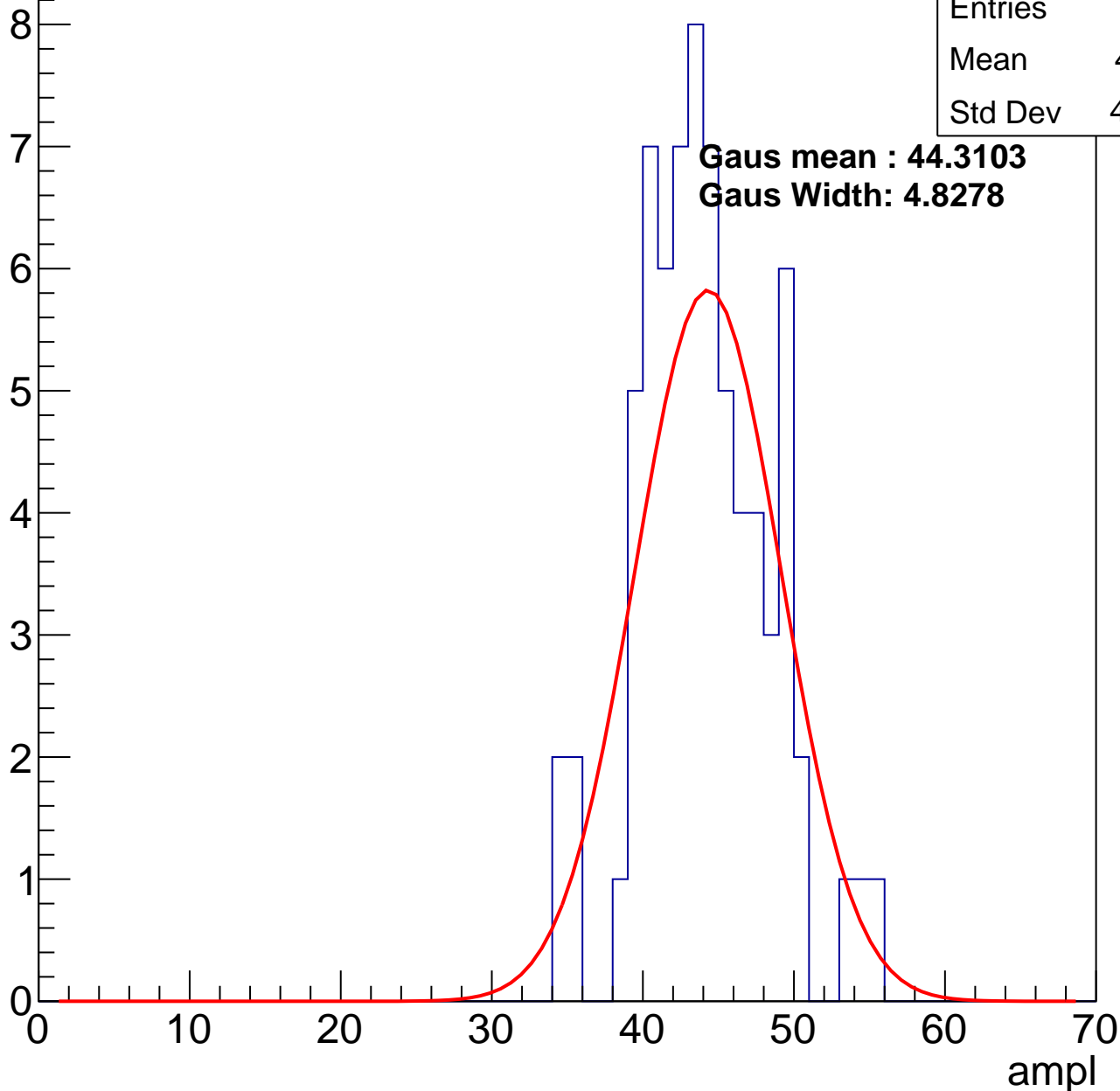
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	43.61
Std Dev	4.319

**Gaus mean : 44.3103**

**Gaus Width: 4.8278**

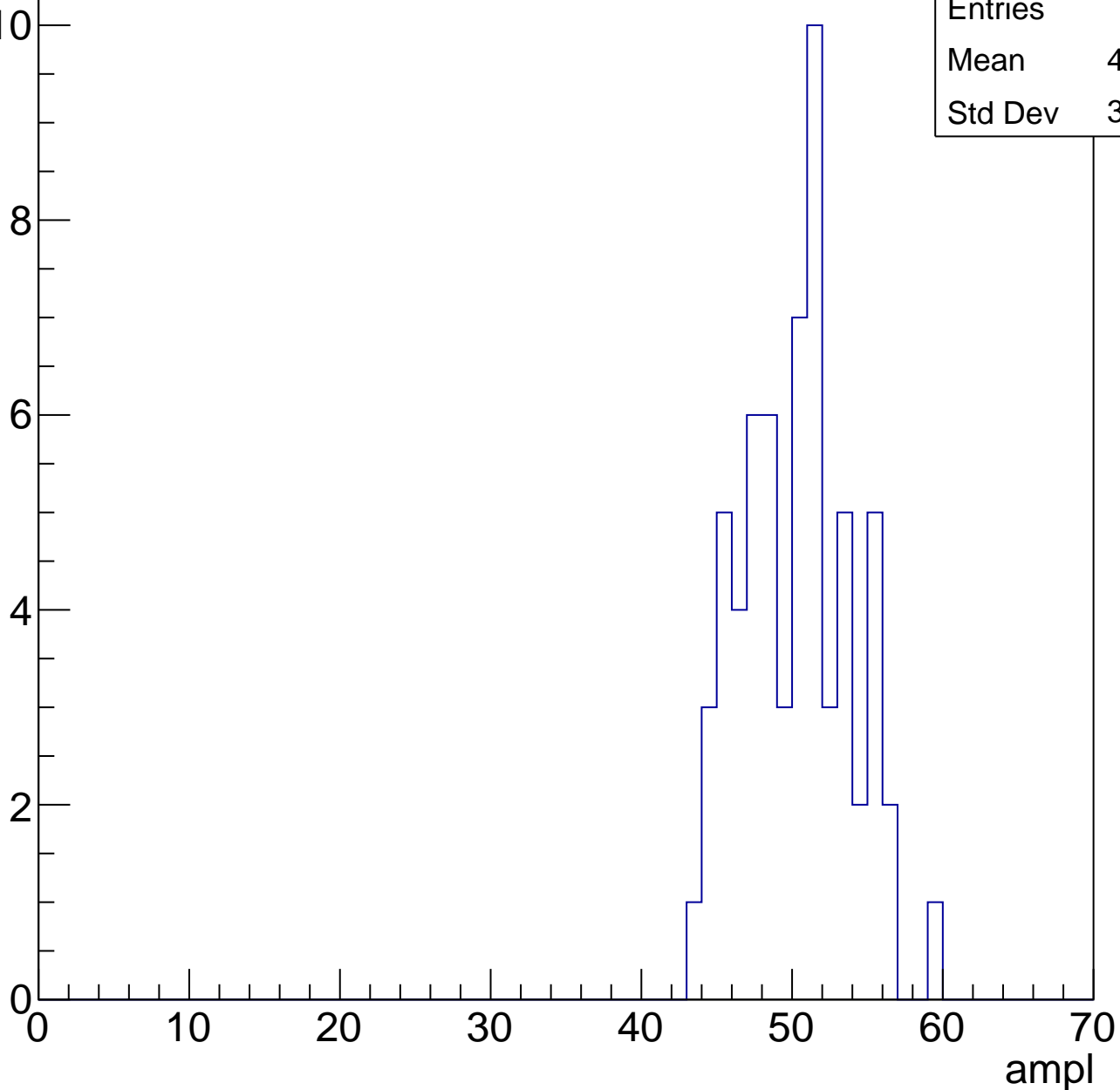


# B1L103S, U26-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	49.78
Std Dev	3.565

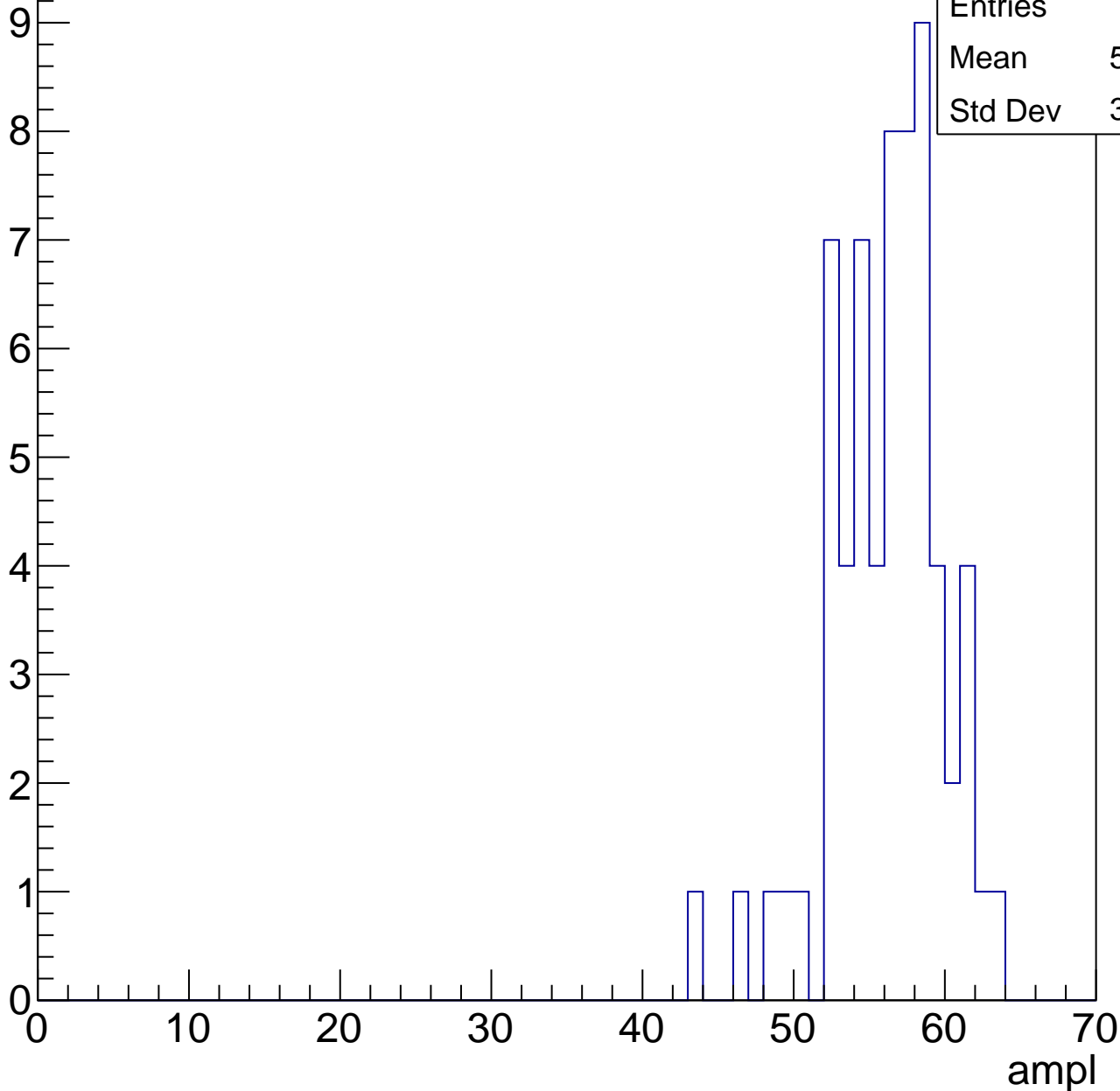


# B1L103S, U26-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	55.64
Std Dev	3.722

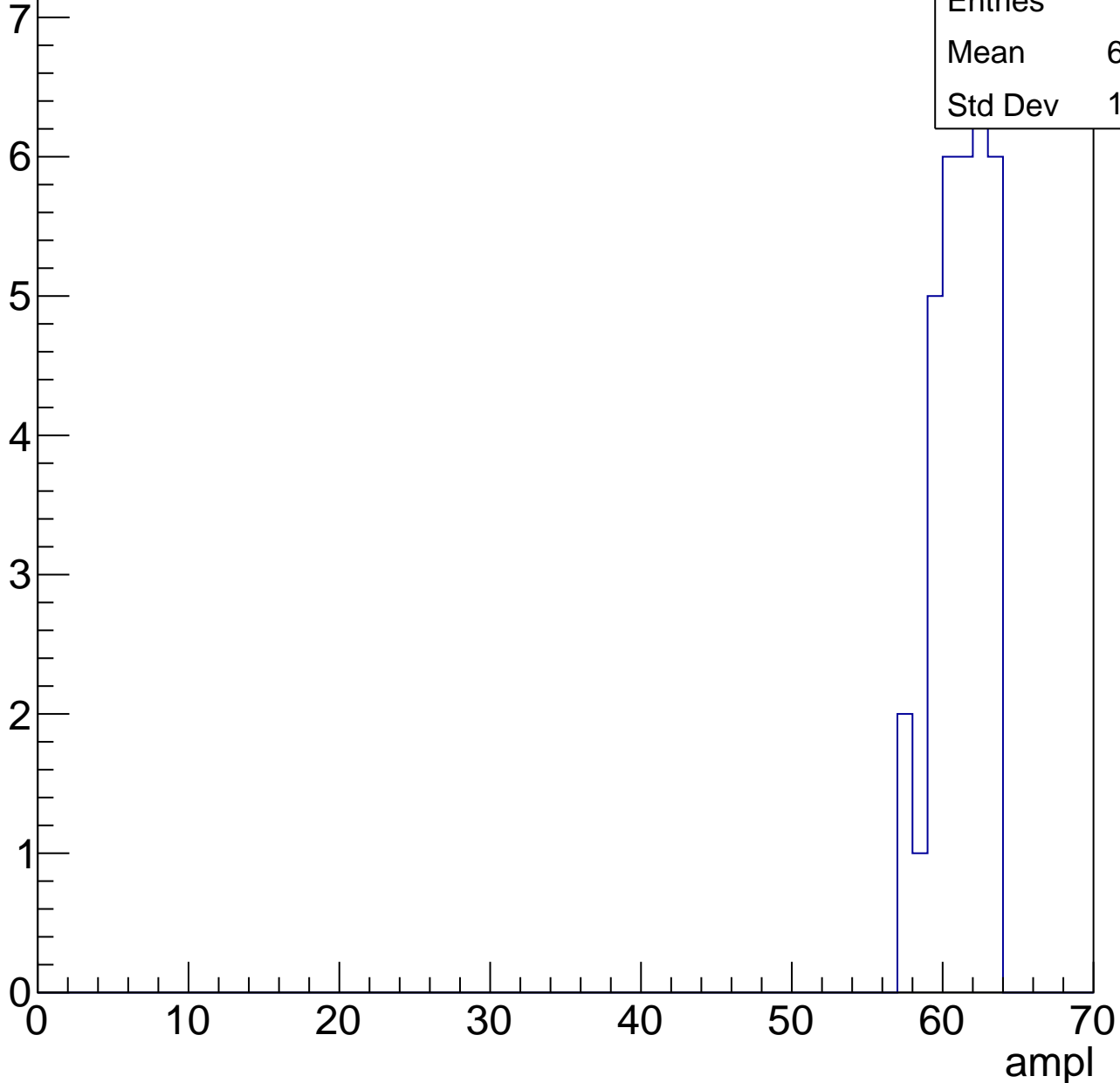


# B1L103S, U26-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

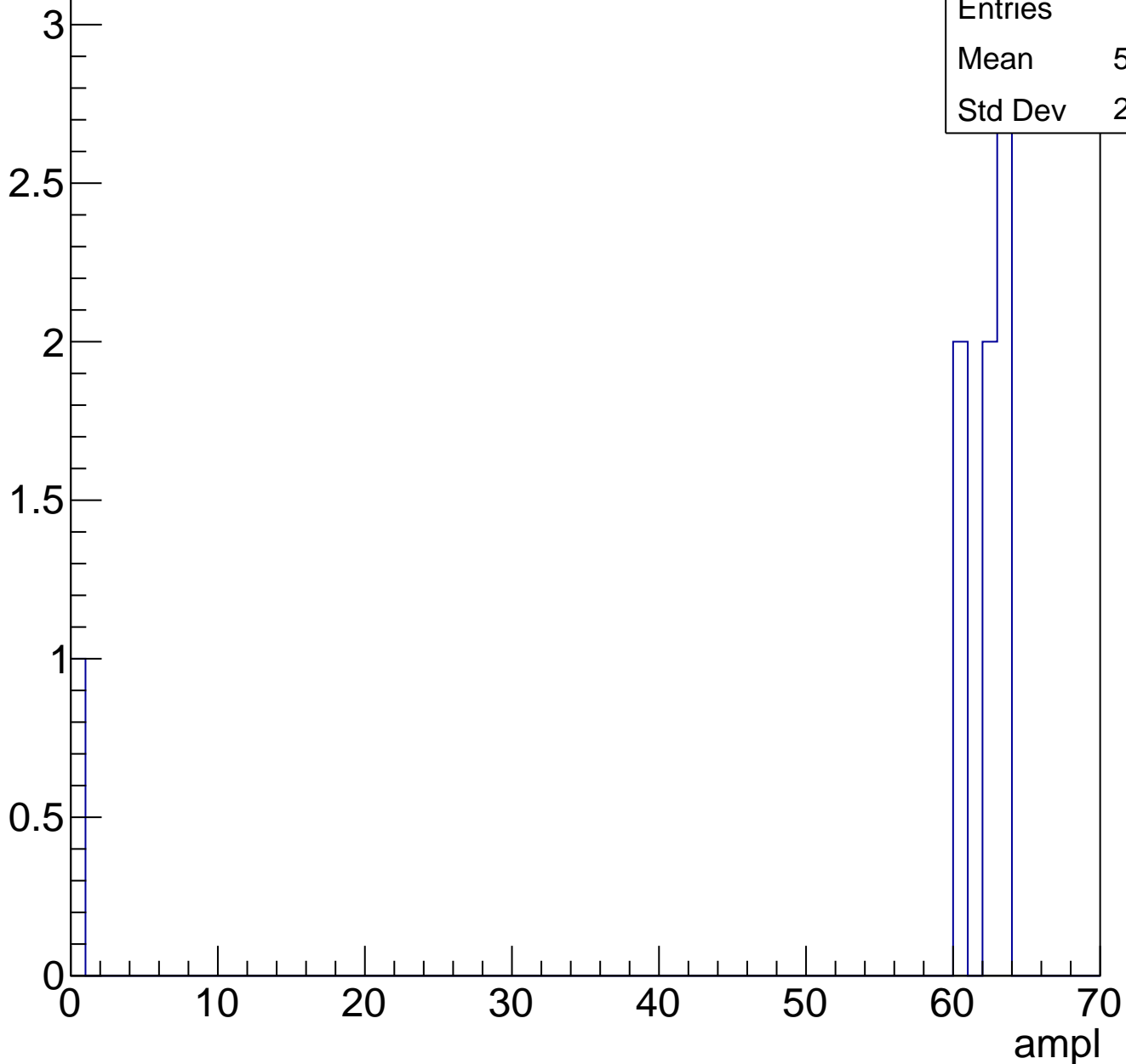
Entries	33
Mean	60.76
Std Dev	1.706



# B1L103S, U26-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U26-ch42, adc0

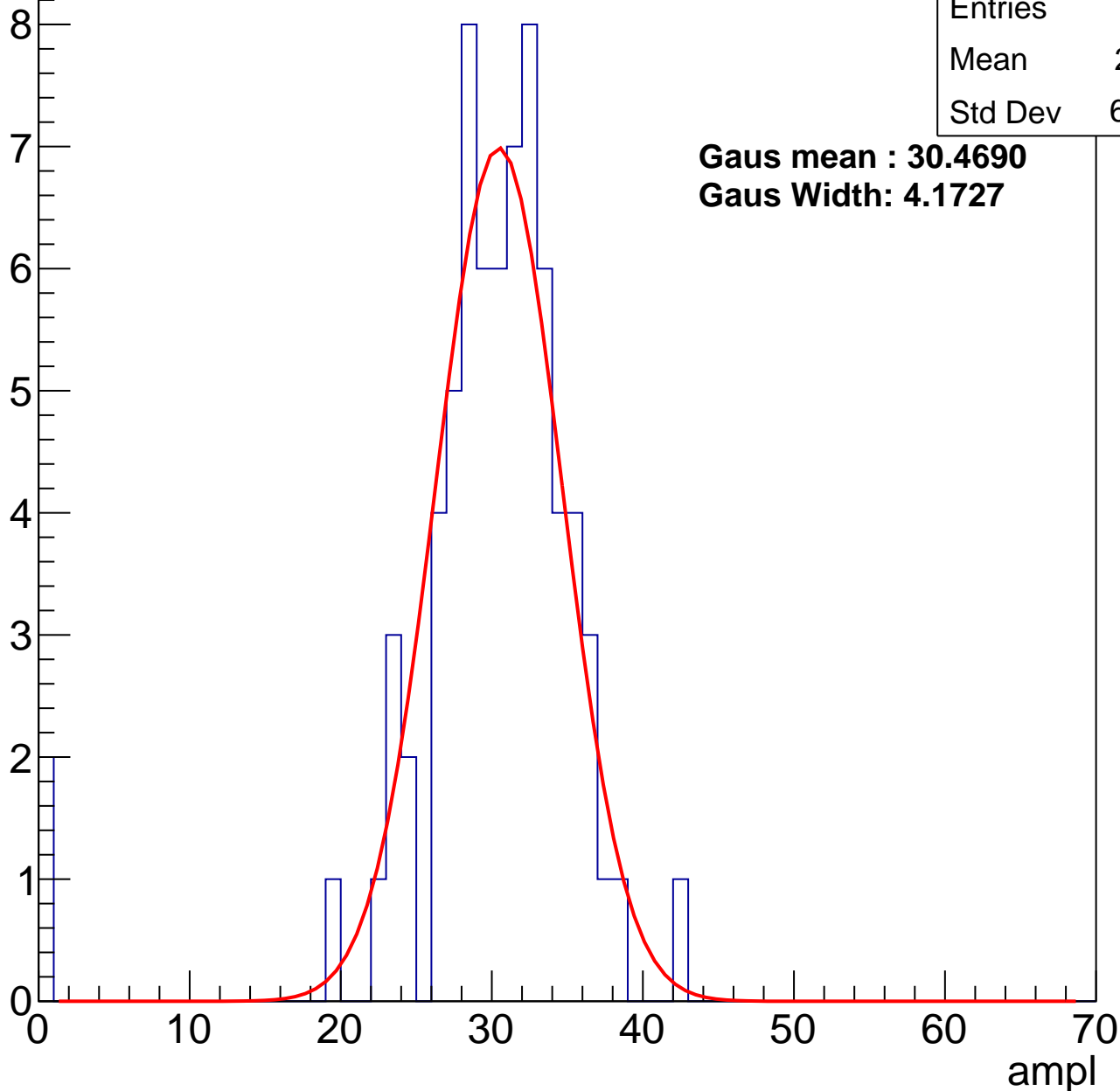
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	29.41
Std Dev	6.354

**Gaus mean : 30.4690**

**Gaus Width: 4.1727**



# B1L103S, U26-ch42, adc1

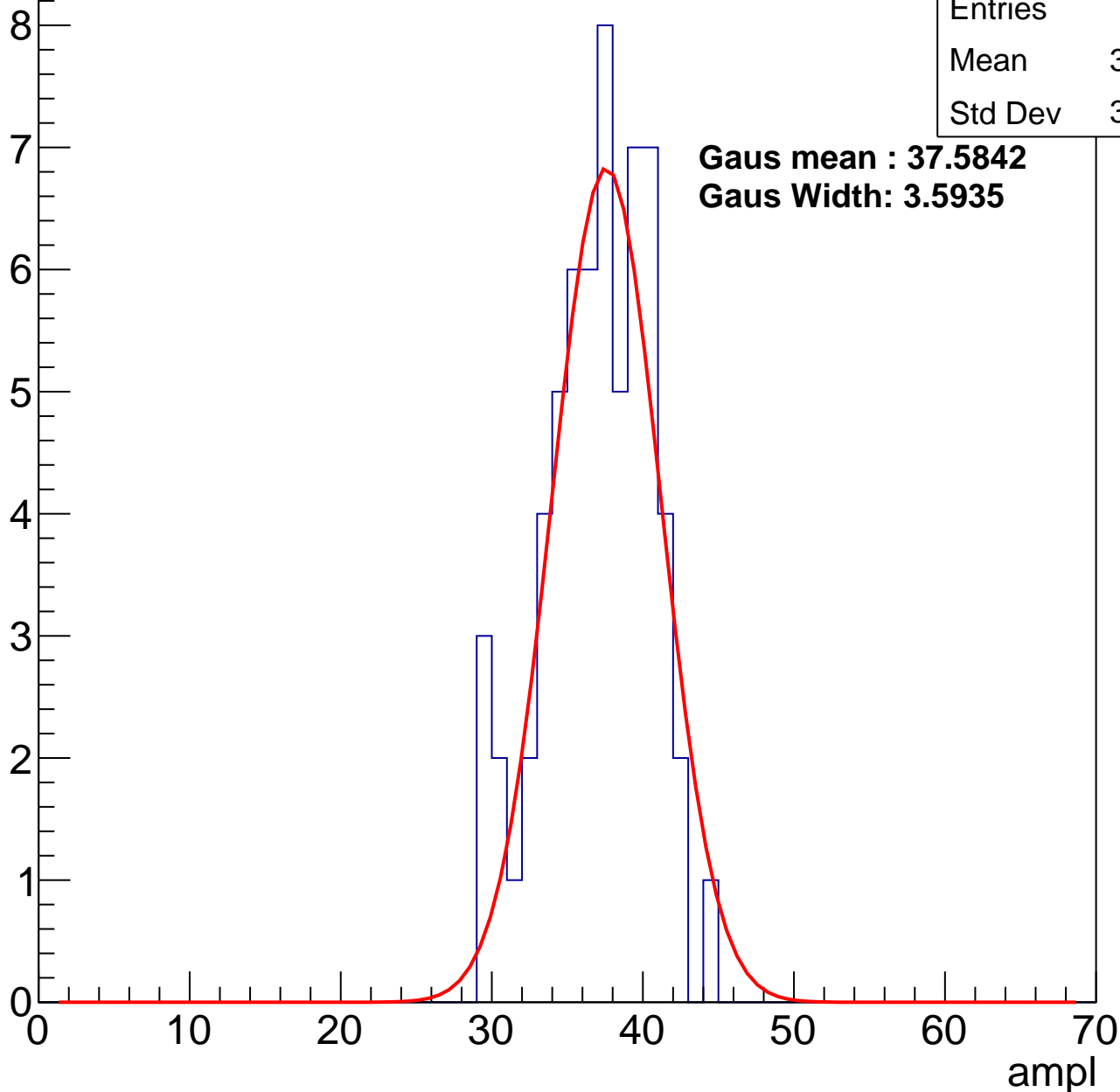
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	36.52
Std Dev	3.473

**Gaus mean : 37.5842**

**Gaus Width: 3.5935**



# B1L103S, U26-ch42, adc2

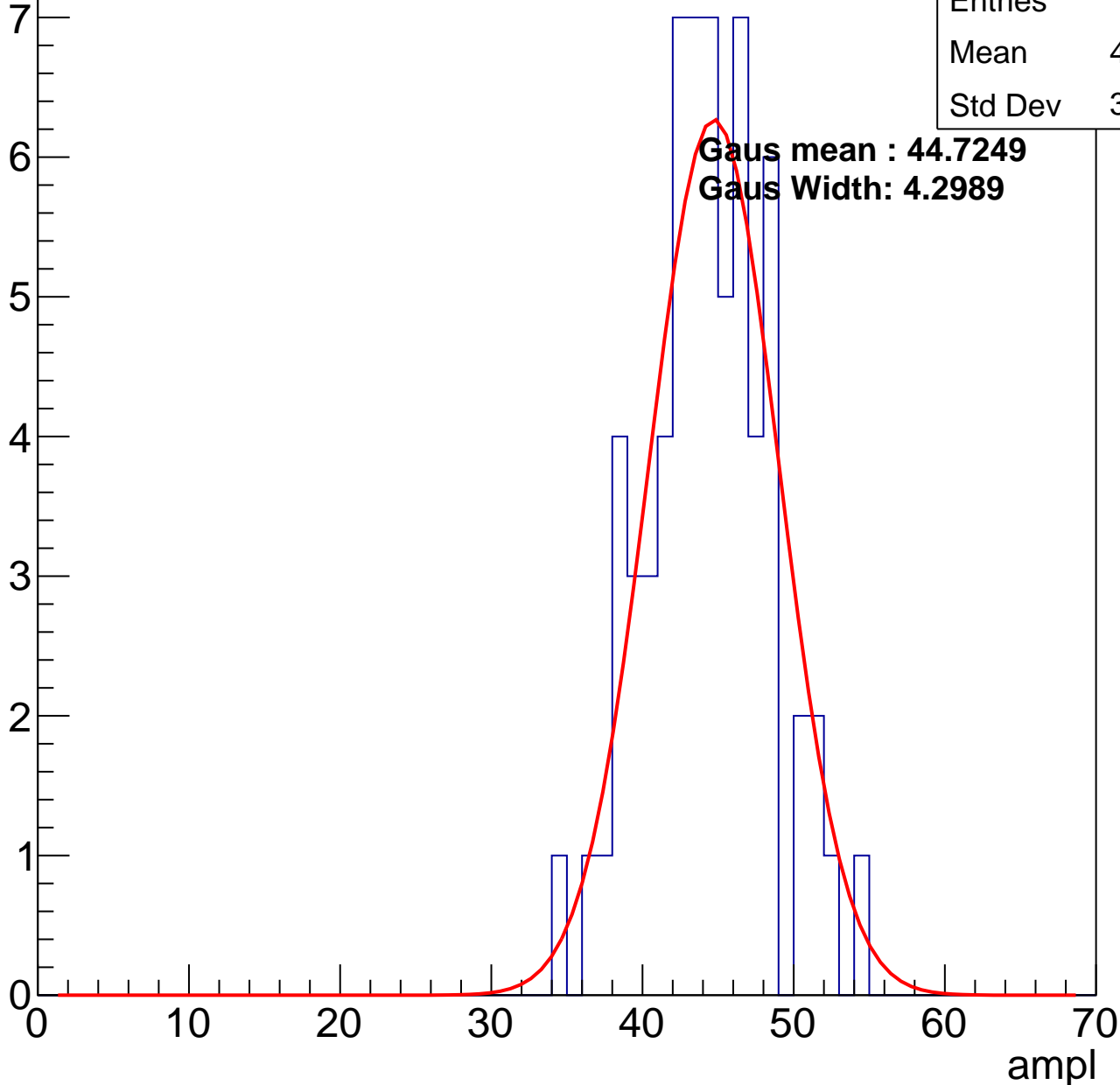
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	43.85
Std Dev	3.986

**Gaus mean : 44.7249**

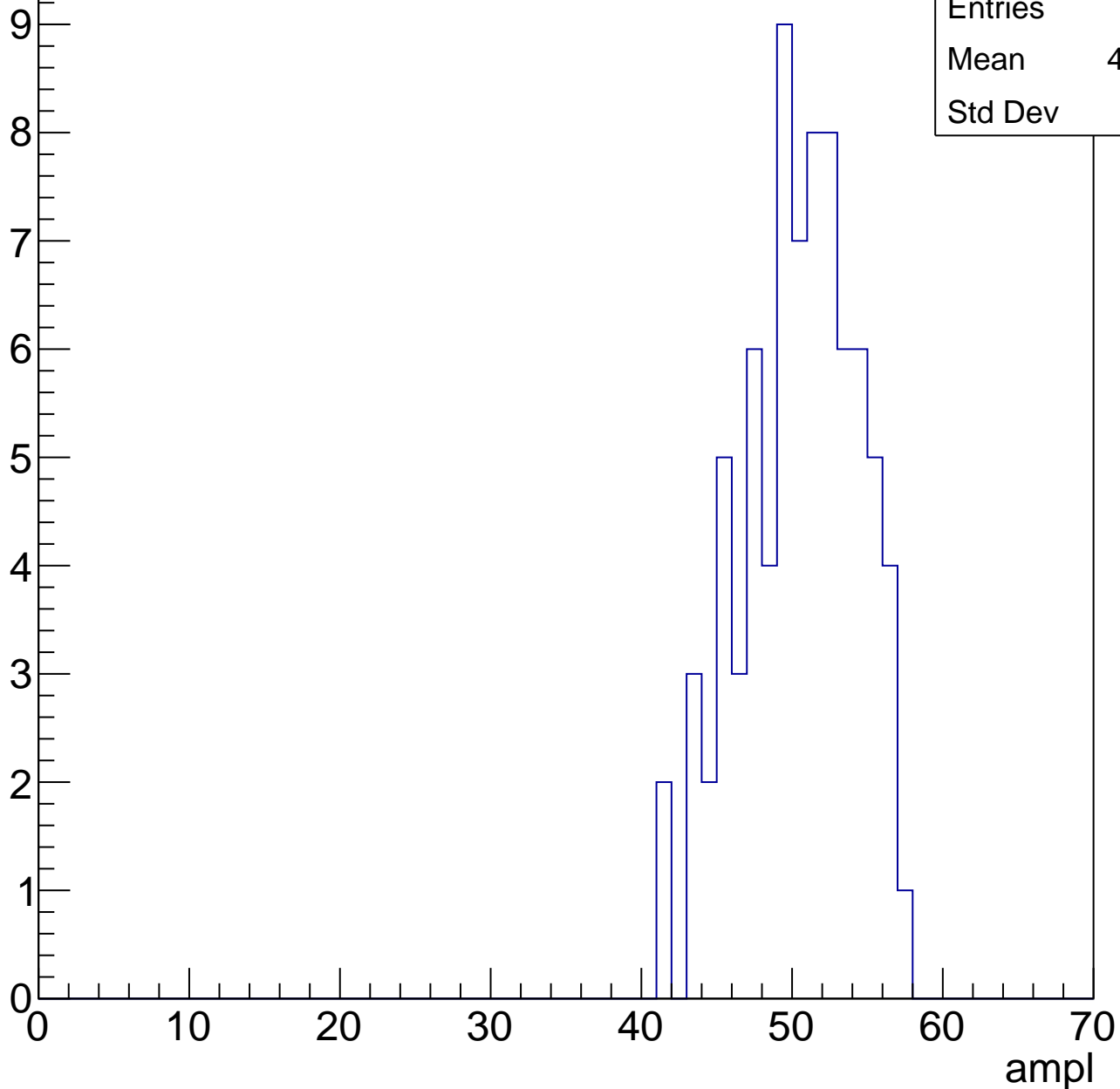
**Gaus Width: 4.2989**



# B1L103S, U26-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

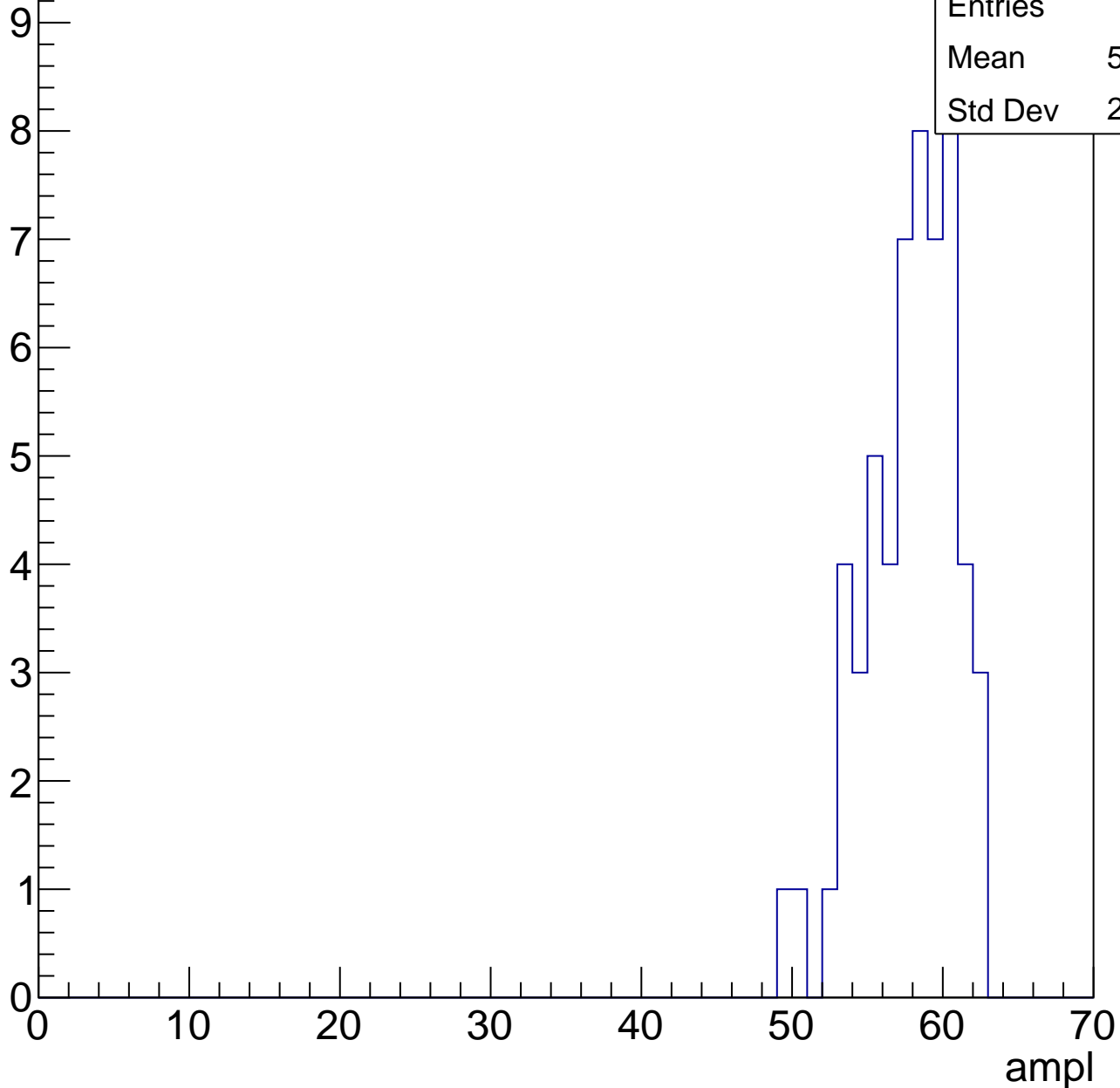
Entry



# B1L103S, U26-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

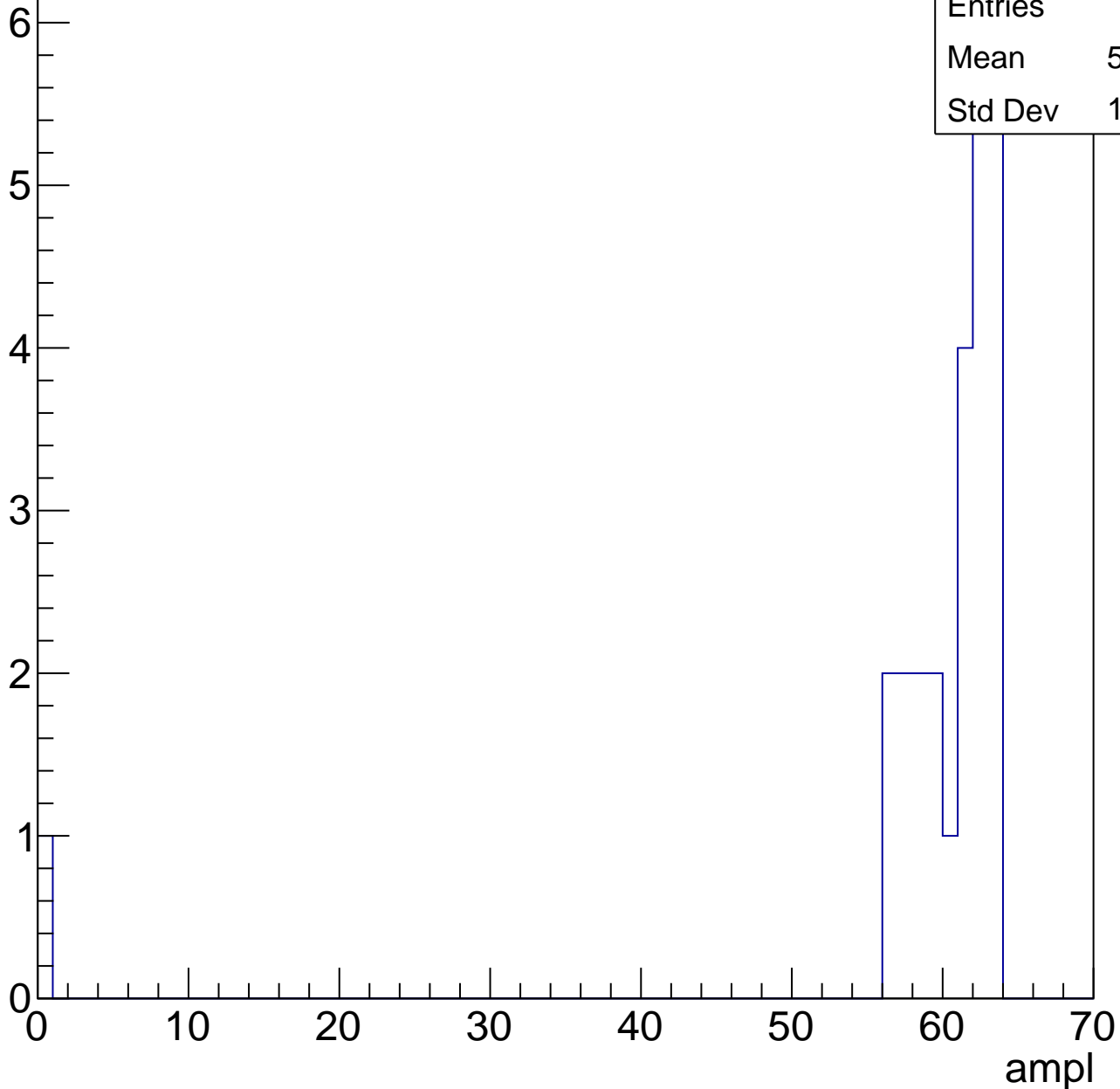


# B1L103S, U26-ch42, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

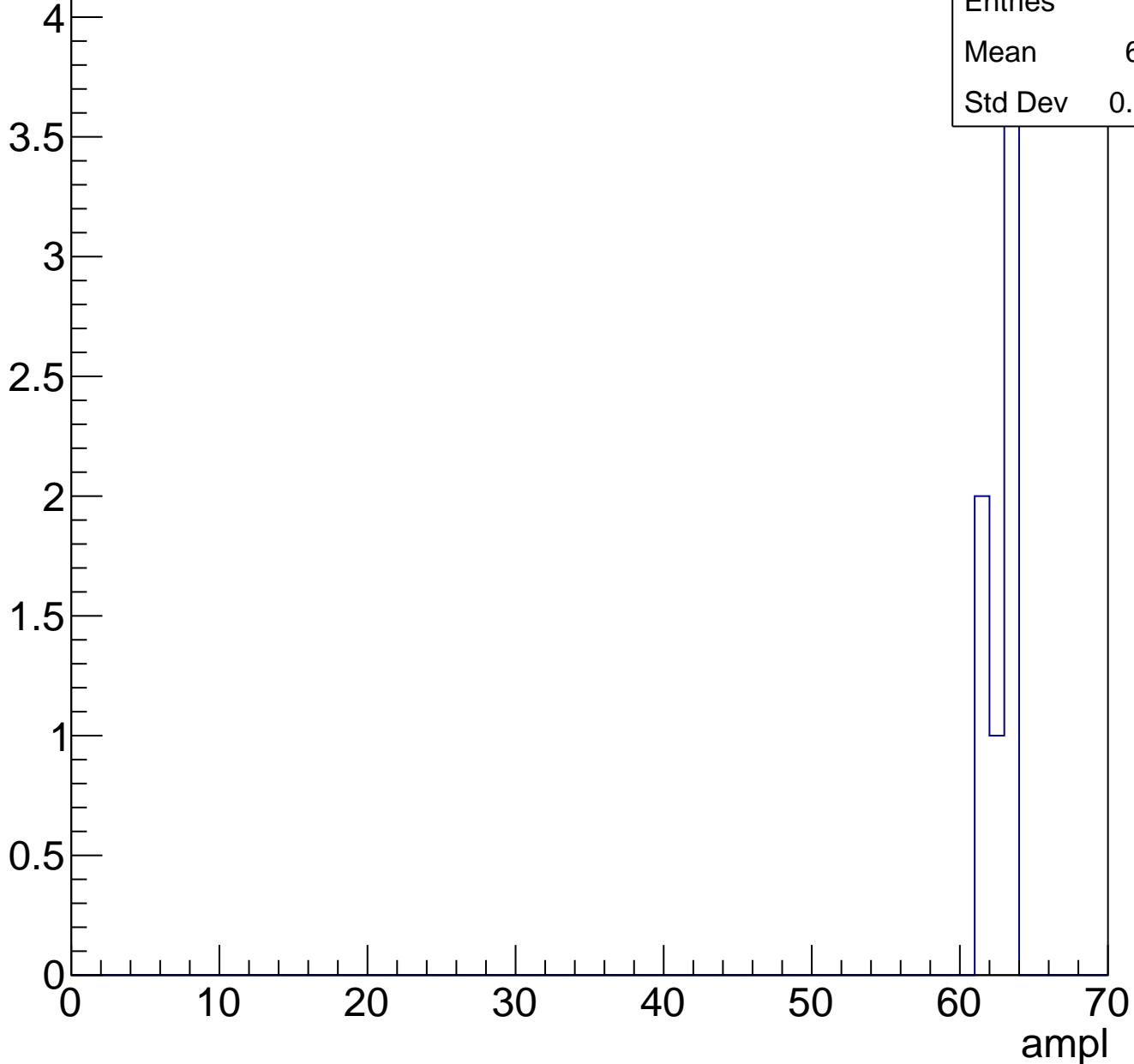
Entries	26
Mean	58.23
Std Dev	11.87



# B1L103S, U26-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

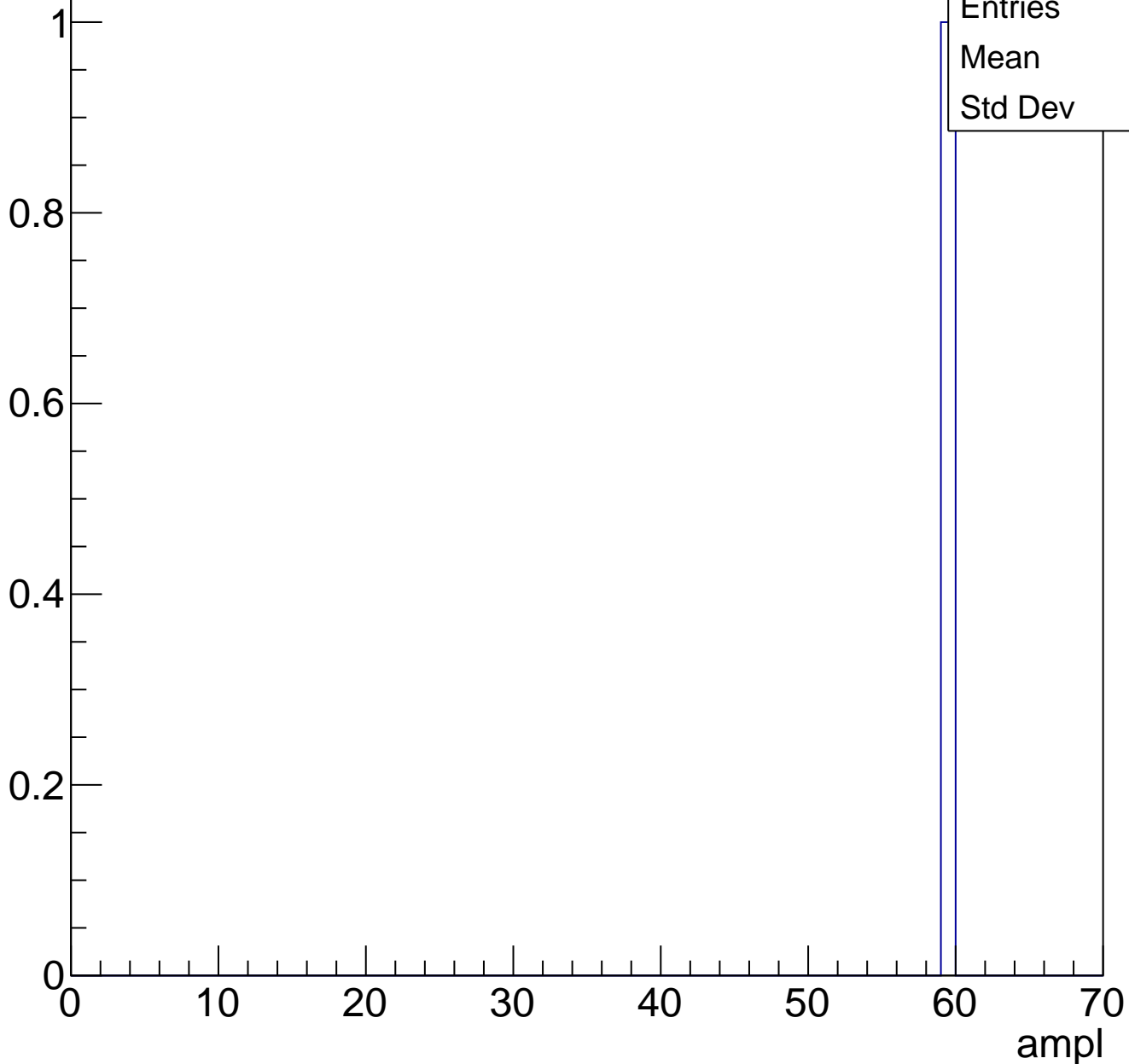




# B1L103S, U26-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	59
Std Dev	0

# B1L103S, U26-ch43, adc0

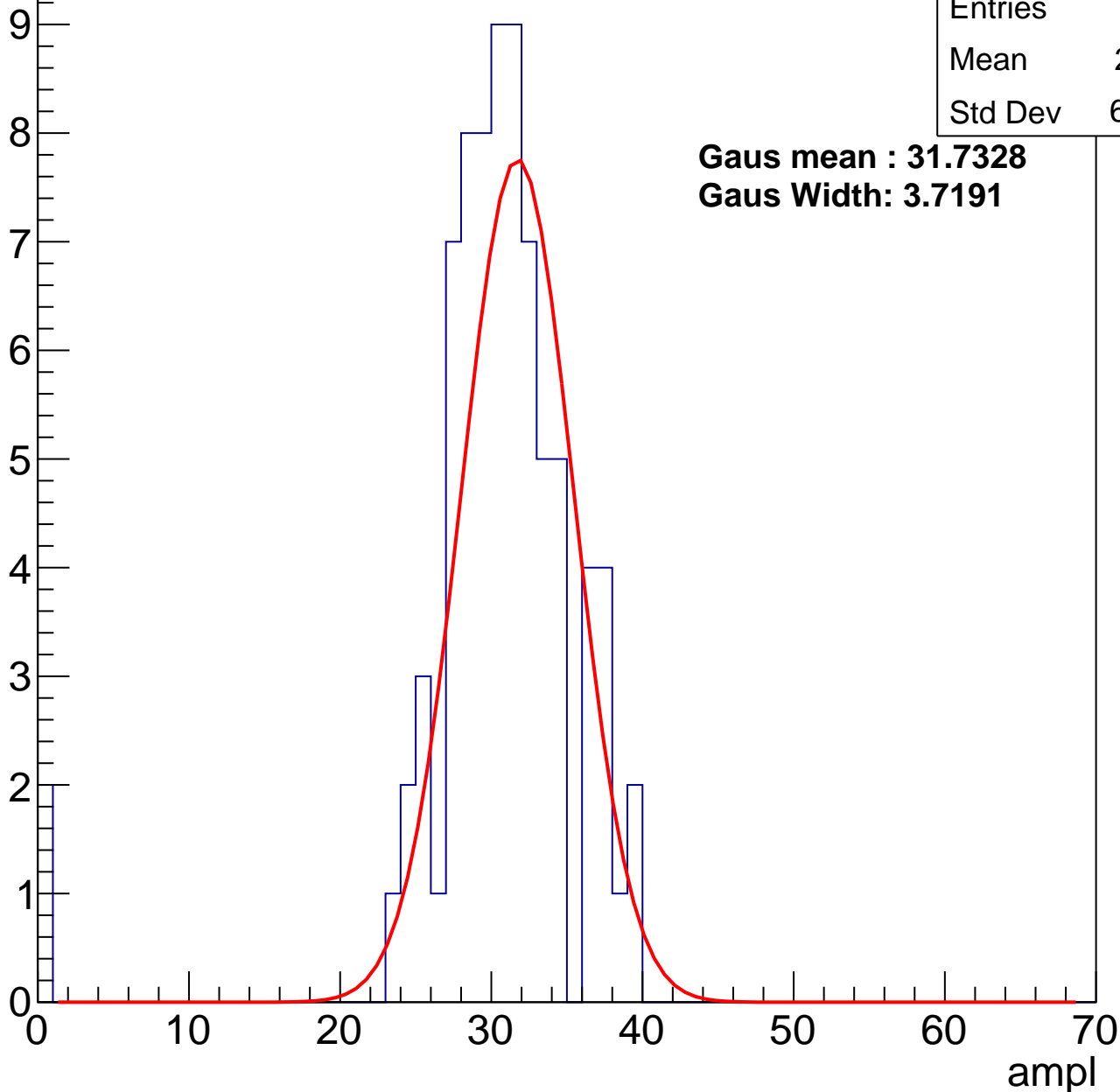
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	29.91
Std Dev	6.037

**Gaus mean : 31.7328**

**Gaus Width: 3.7191**



# B1L103S, U26-ch43, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	74
Mean	37.64
Std Dev	3.78

**Gaus mean : 37.6297**

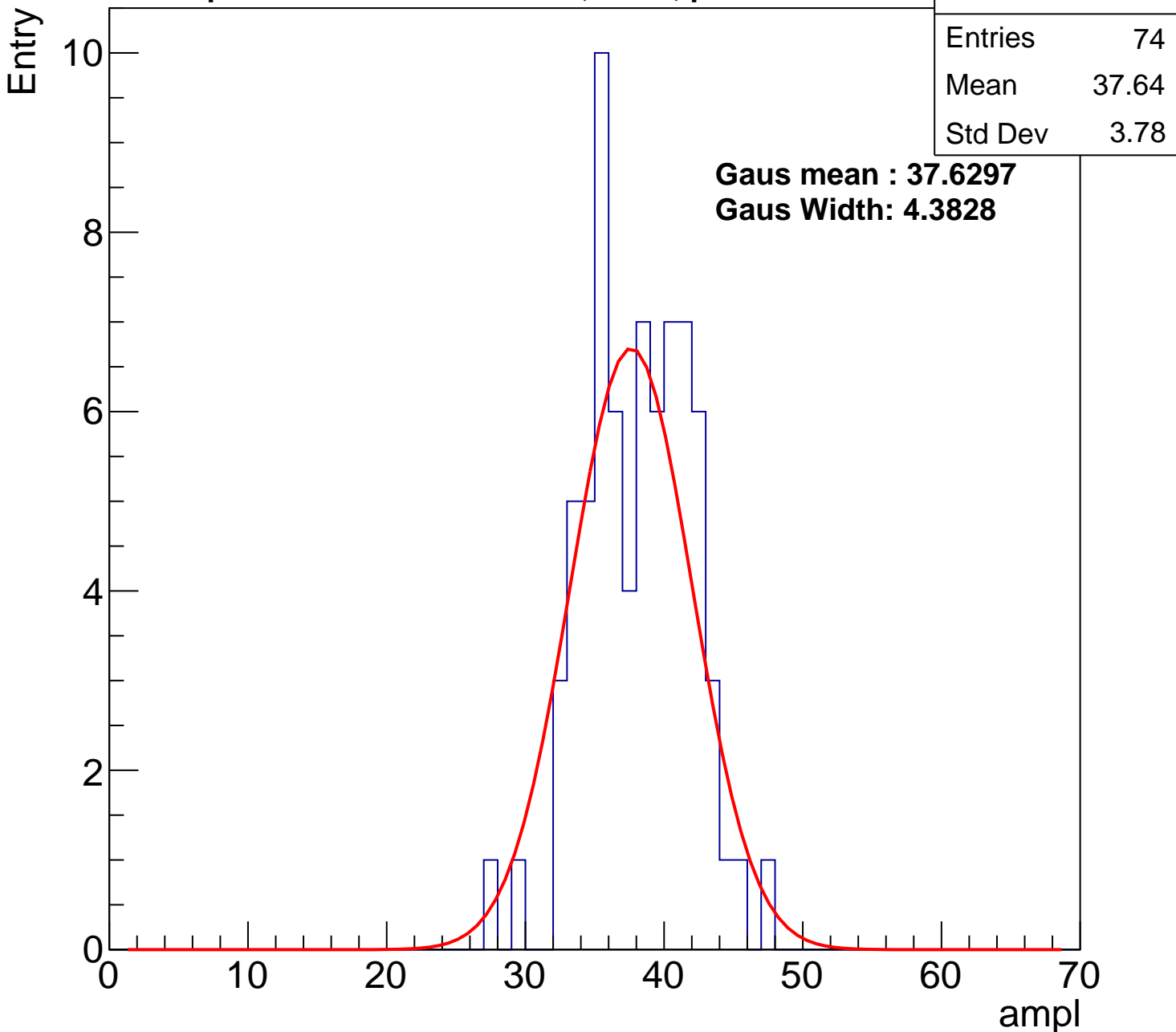
**Gaus Width: 4.3828**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch43, adc2

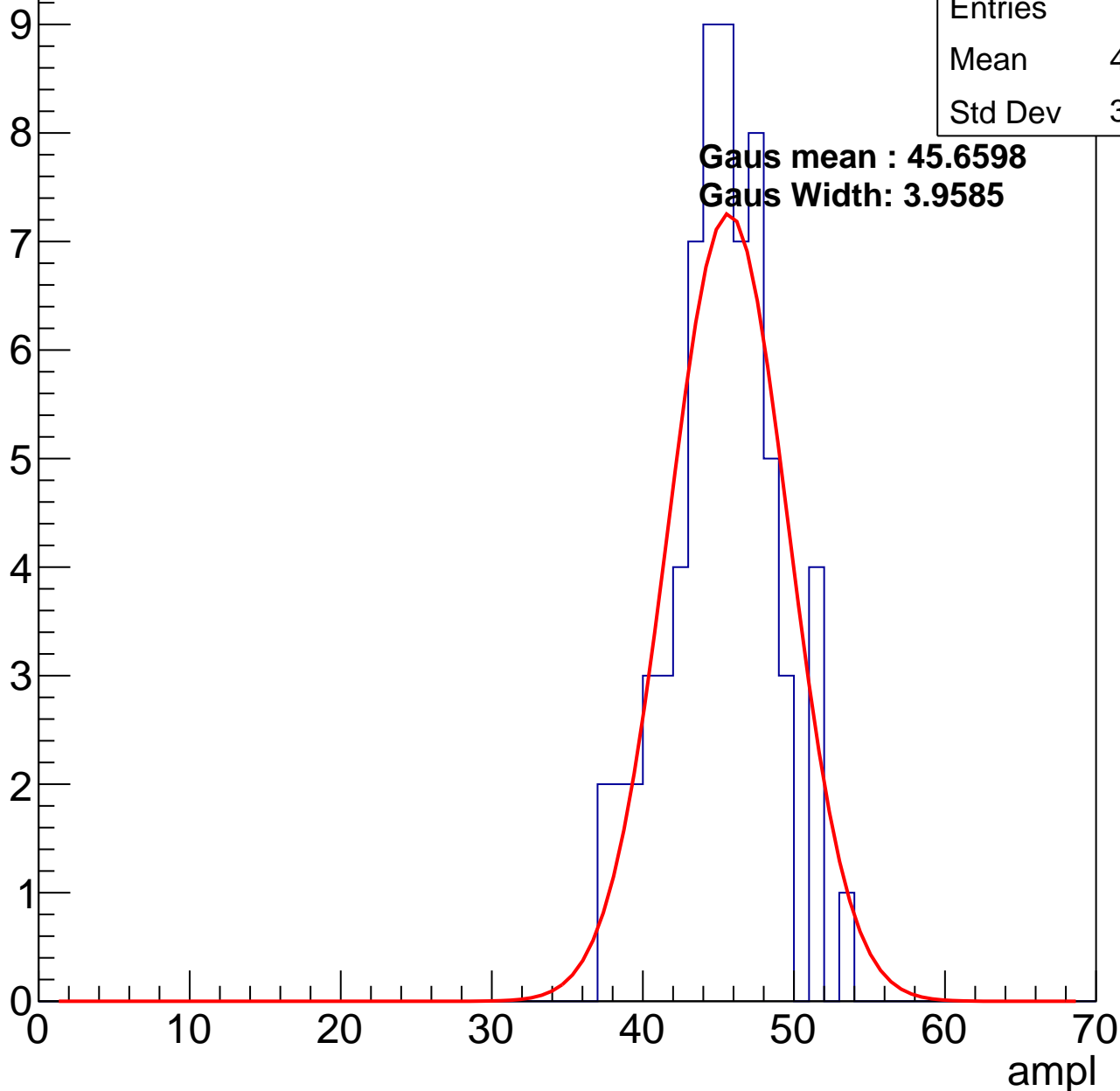
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	44.68
Std Dev	3.462

**Gaus mean : 45.6598**

**Gaus Width: 3.9585**

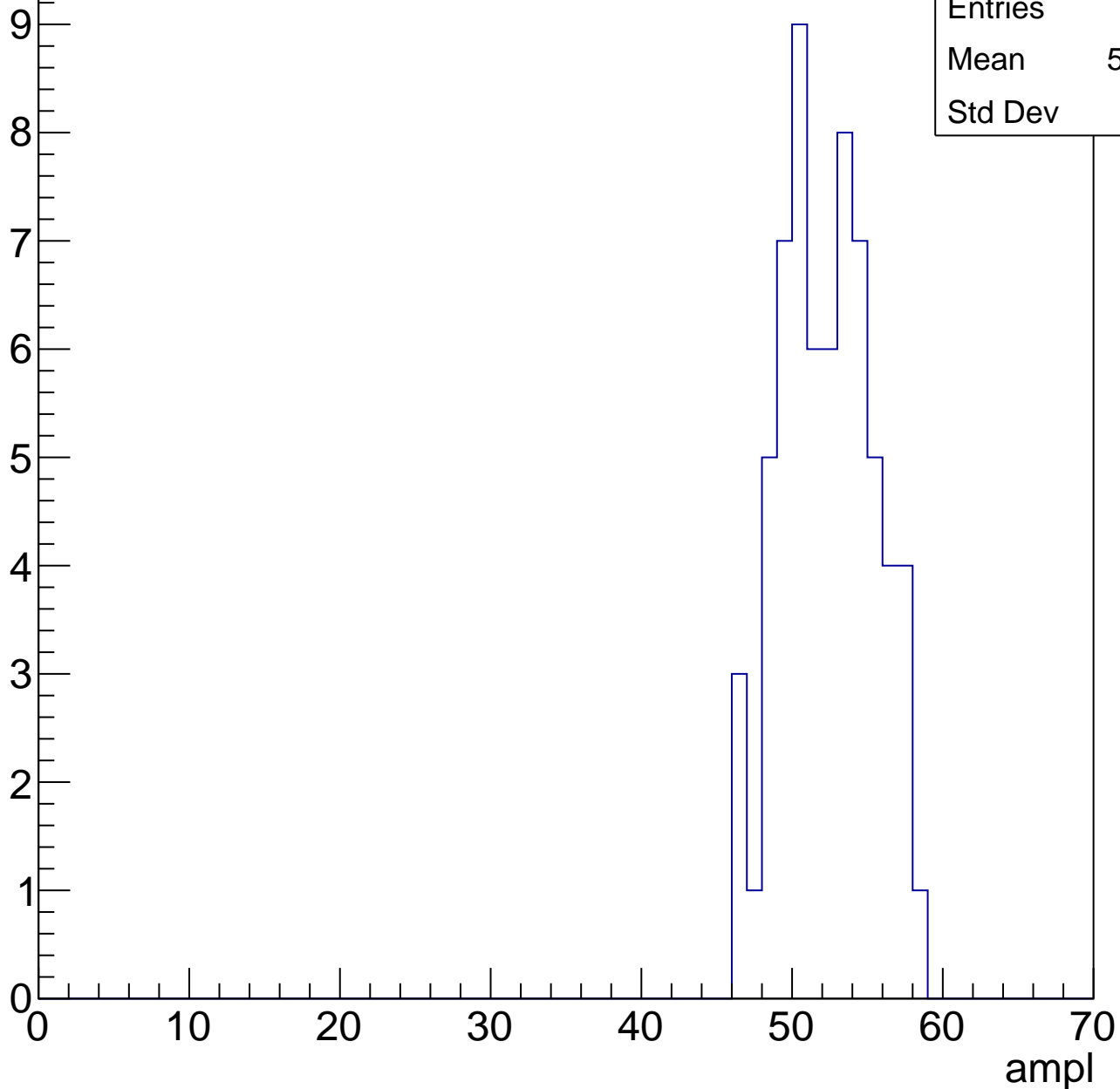


# B1L103S, U26-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	51.86
Std Dev	3.01

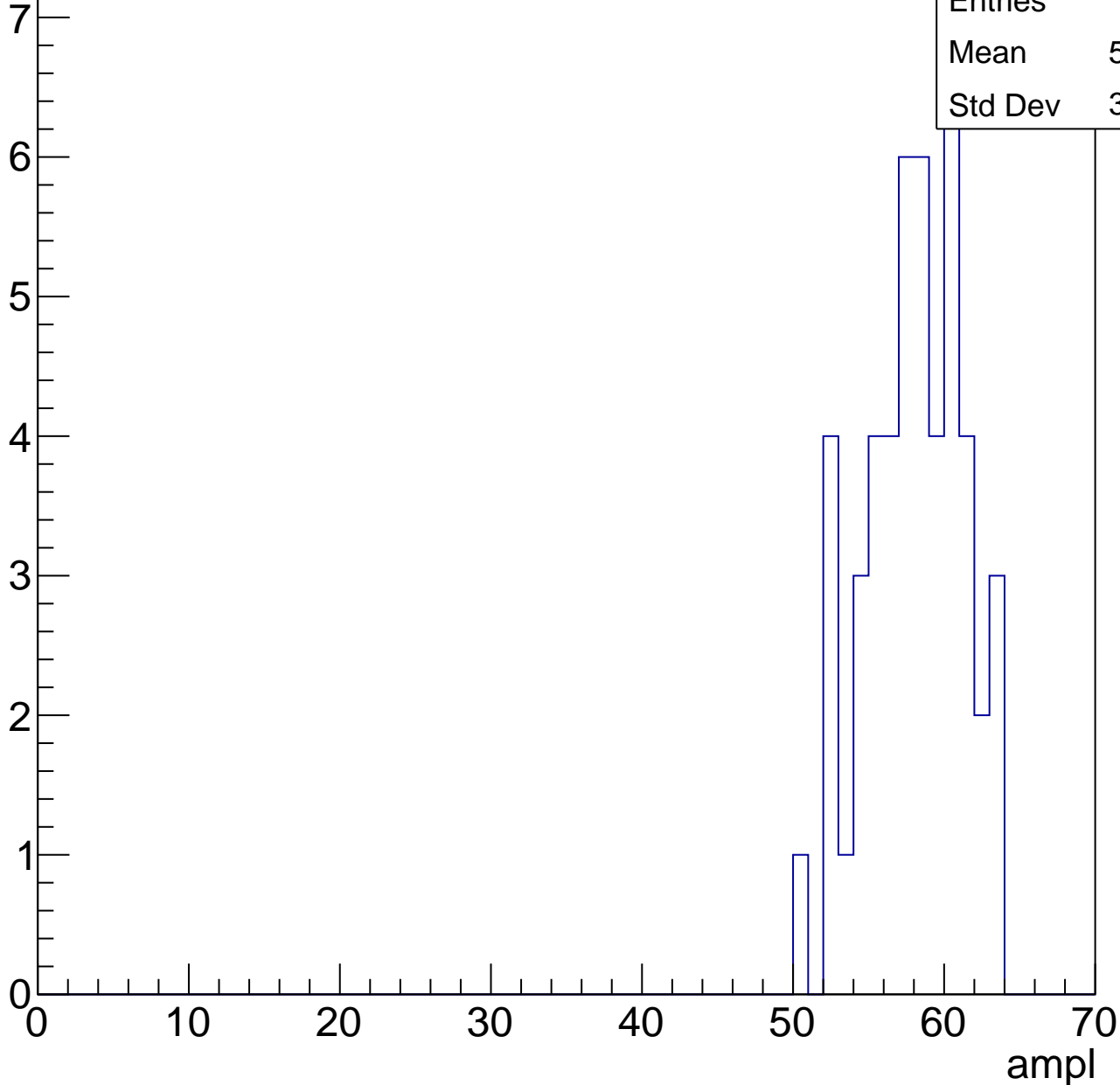


# B1L103S, U26-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	57.55
Std Dev	3.208

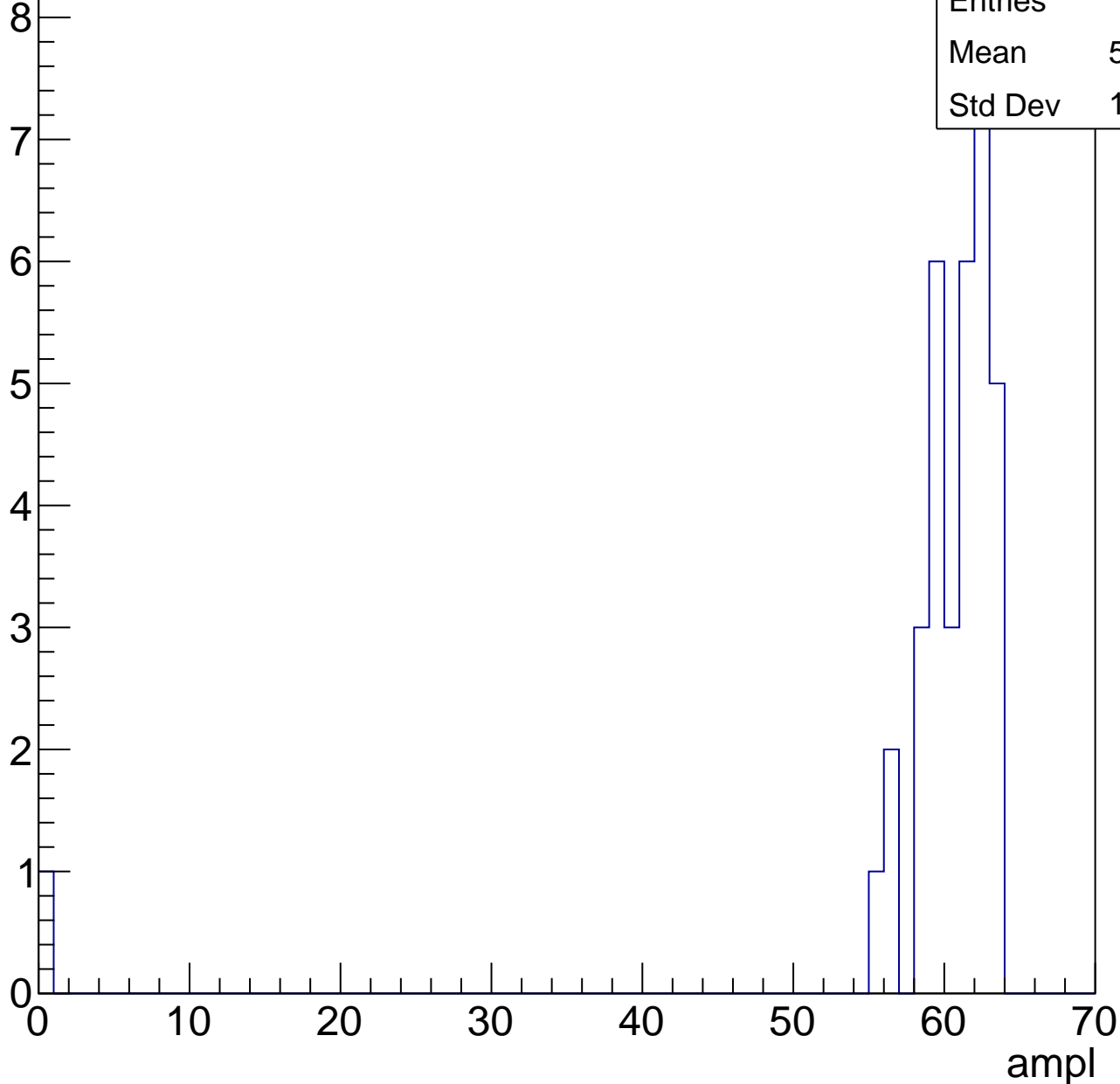


# B1L103S, U26-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	35
Mean	58.63
Std Dev	10.27



# B1L103S, U26-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U26-ch44, adc0

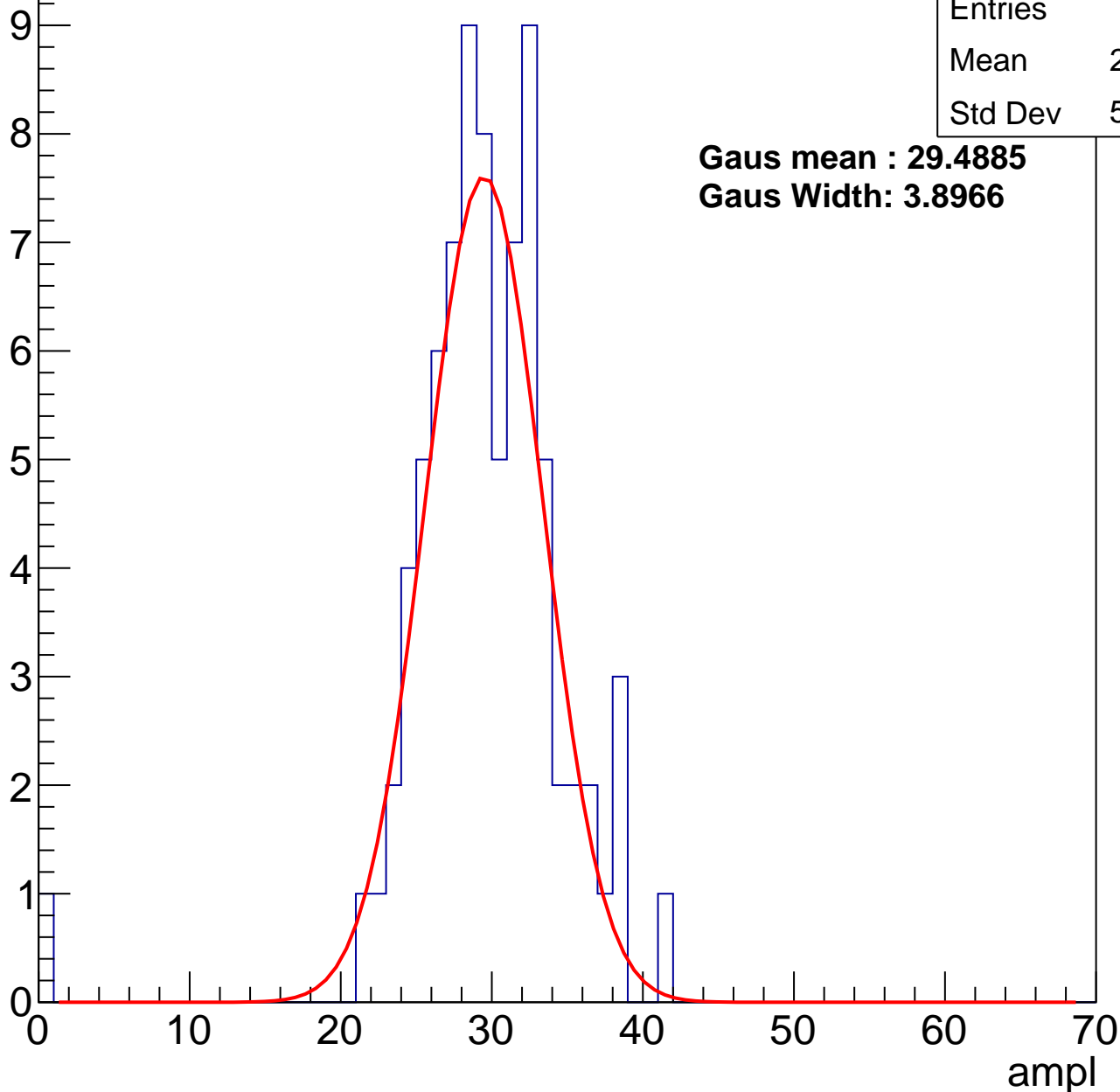
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	81
Mean	29.15
Std Dev	5.164

**Gaus mean : 29.4885**

**Gaus Width: 3.8966**



# B1L103S, U26-ch44, adc1

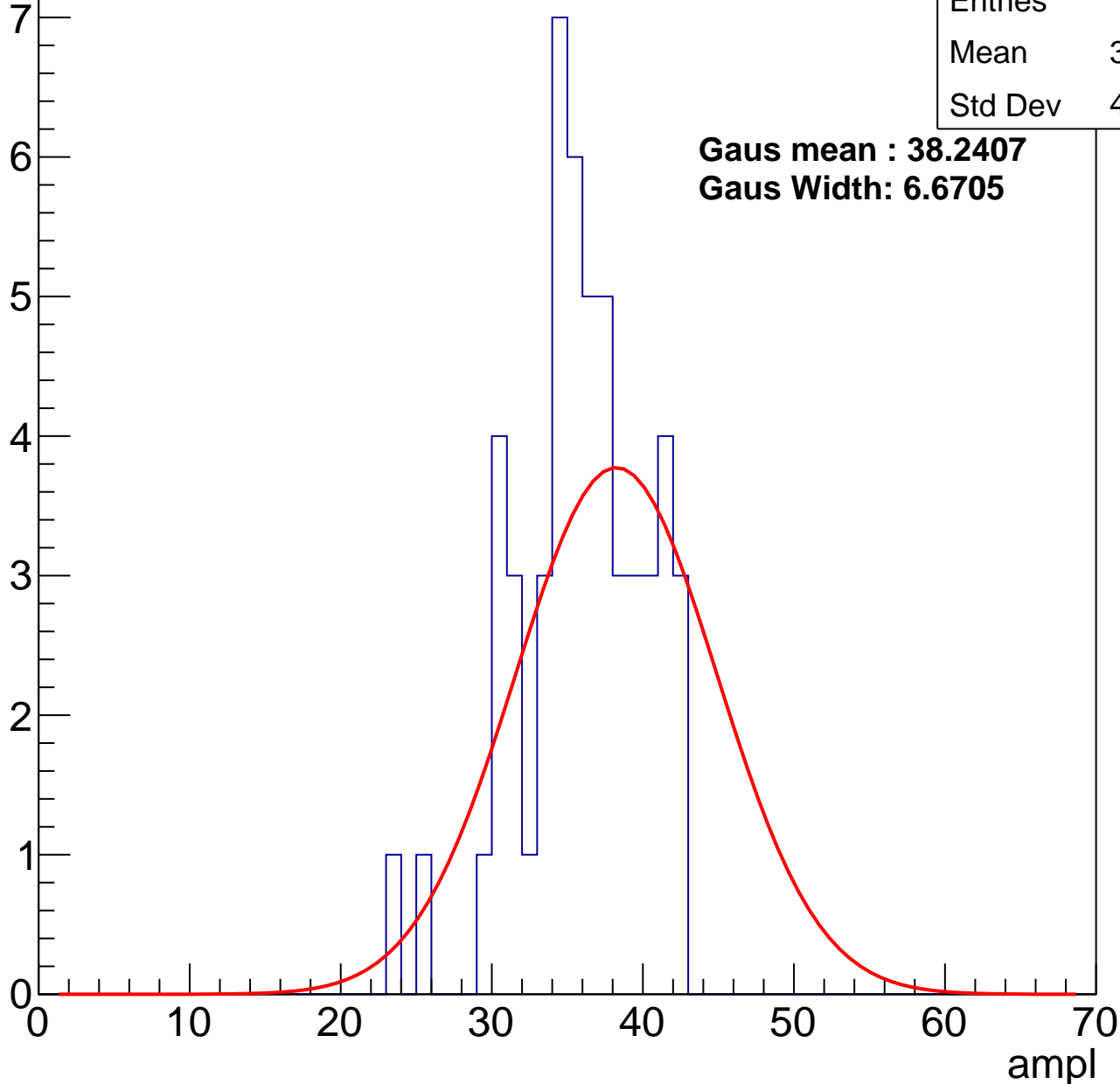
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	35.38
Std Dev	4.154

**Gaus mean : 38.2407**

**Gaus Width: 6.6705**



# B1L103S, U26-ch44, adc2

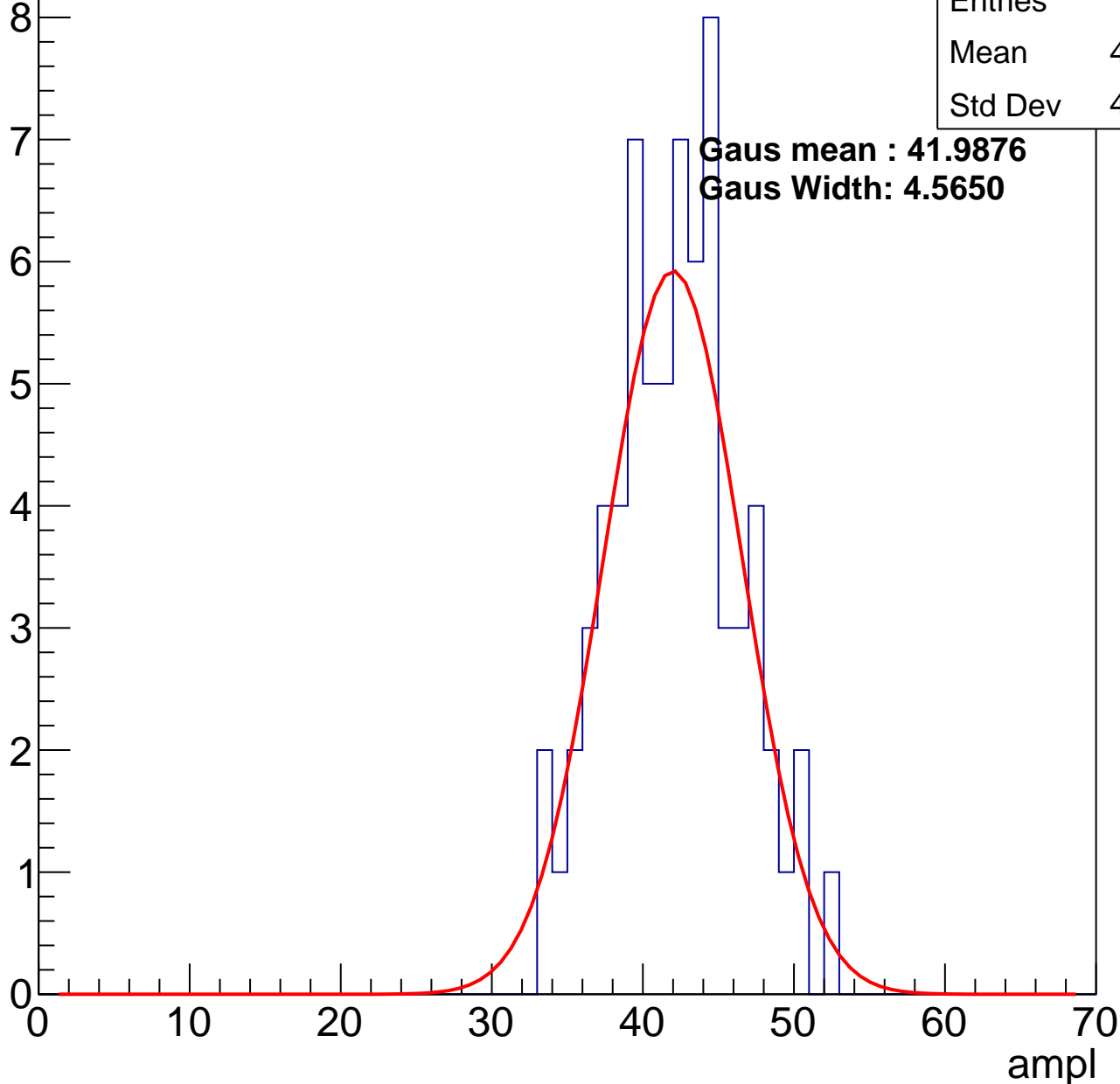
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	41.69
Std Dev	4.207

**Gaus mean : 41.9876**

**Gaus Width: 4.5650**

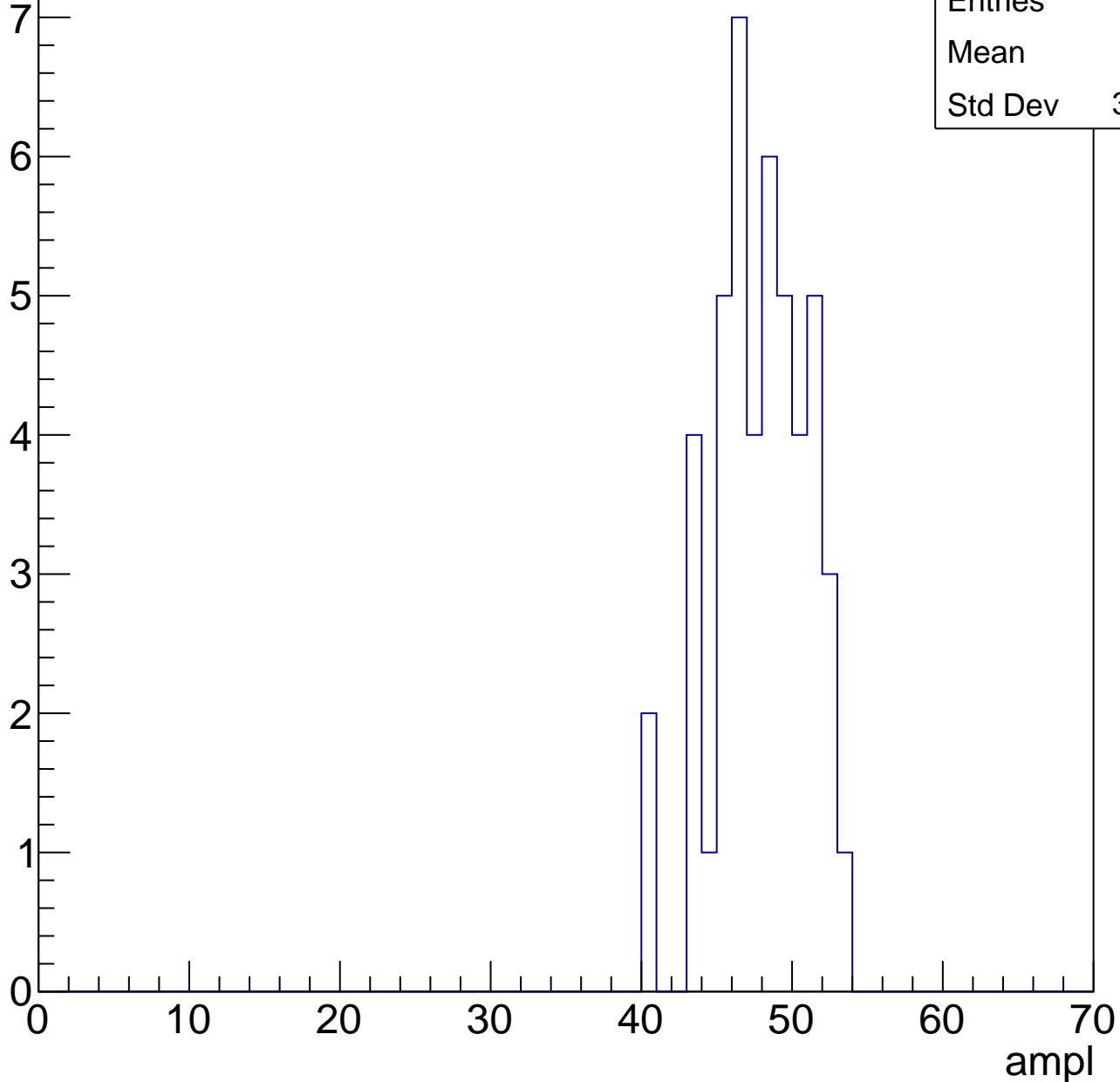


# B1L103S, U26-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	47.4
Std Dev	3.071

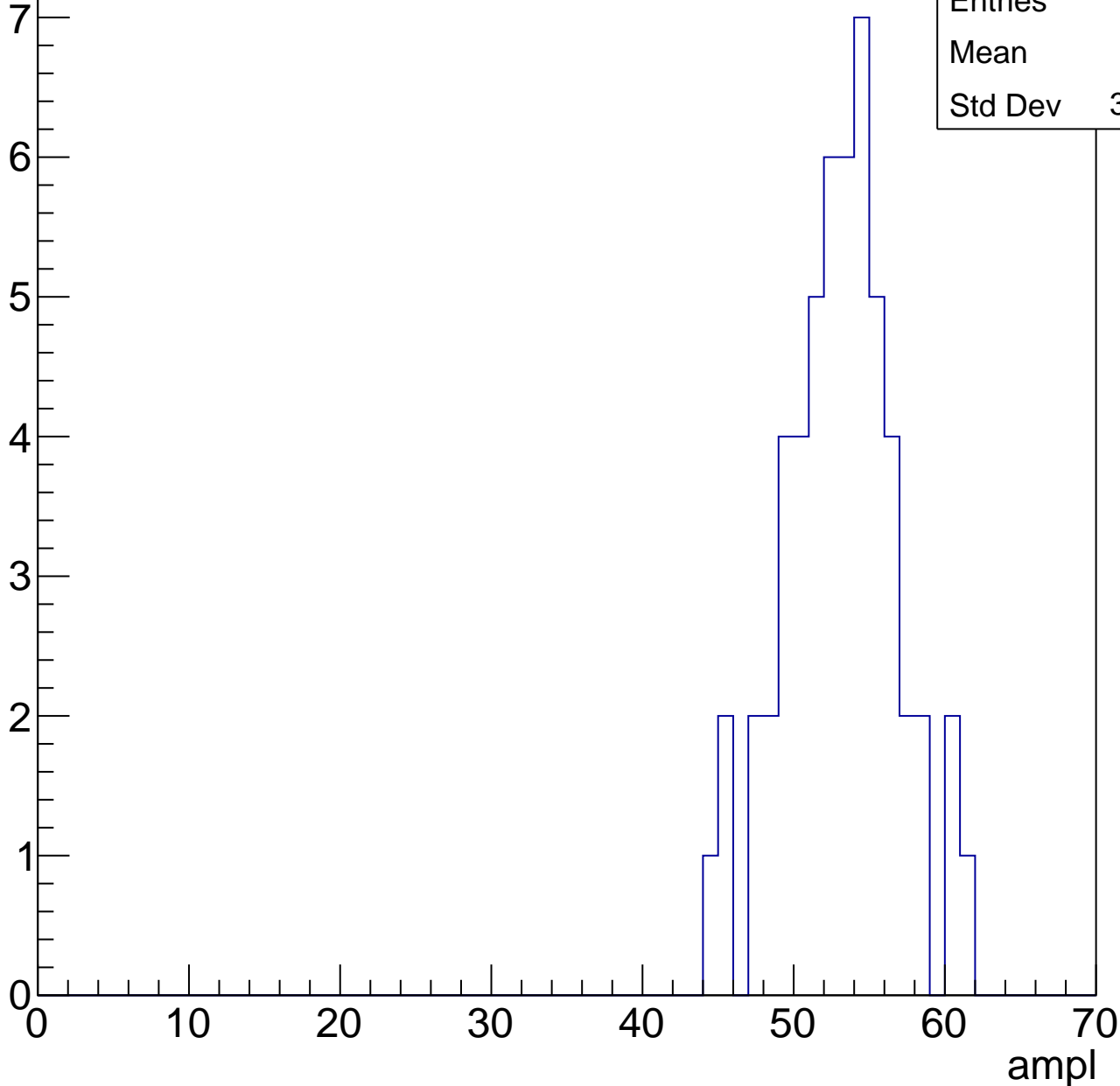


# B1L103S, U26-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

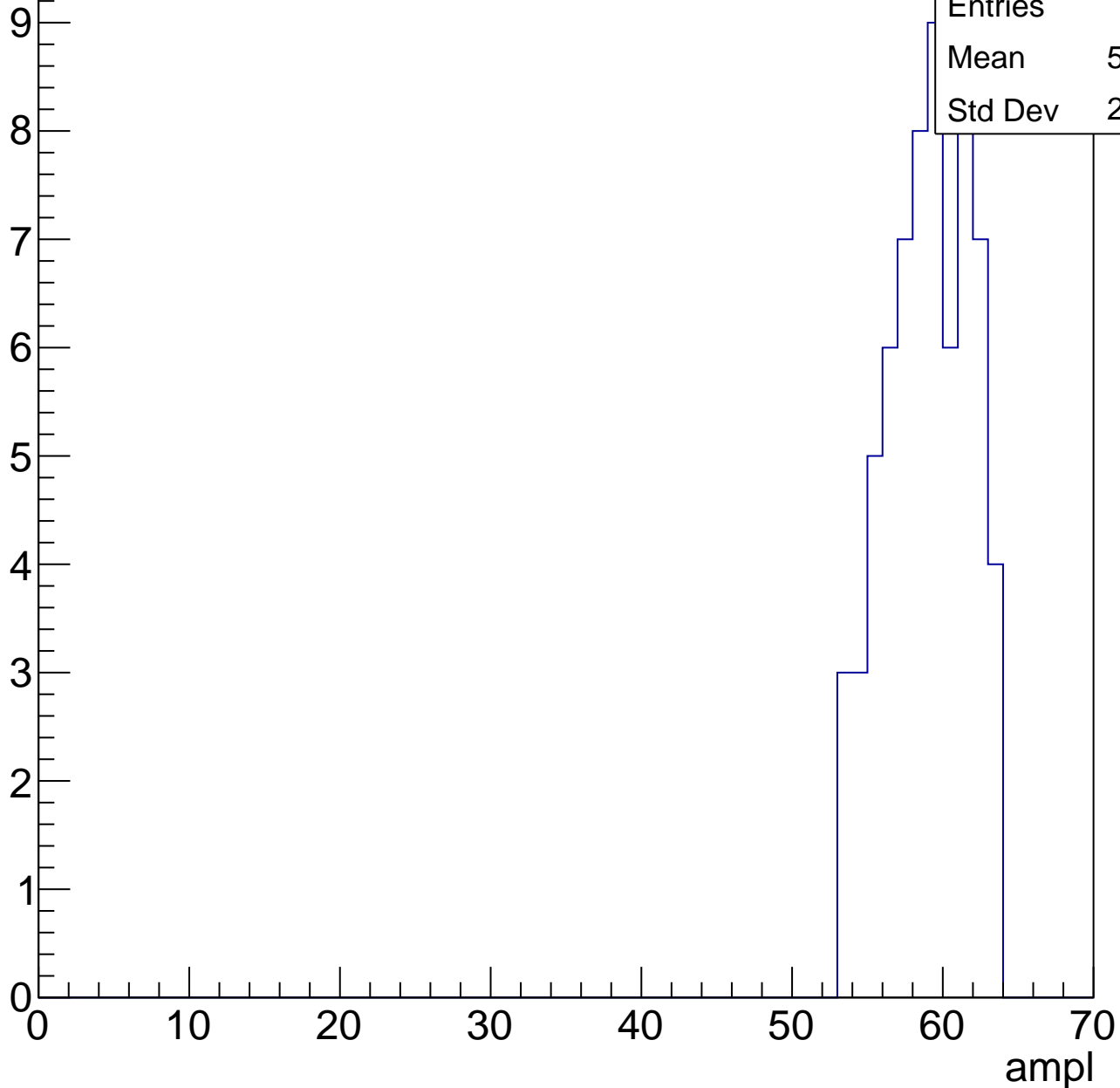
Entries	55
Mean	52.6
Std Dev	3.706



# B1L103S, U26-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



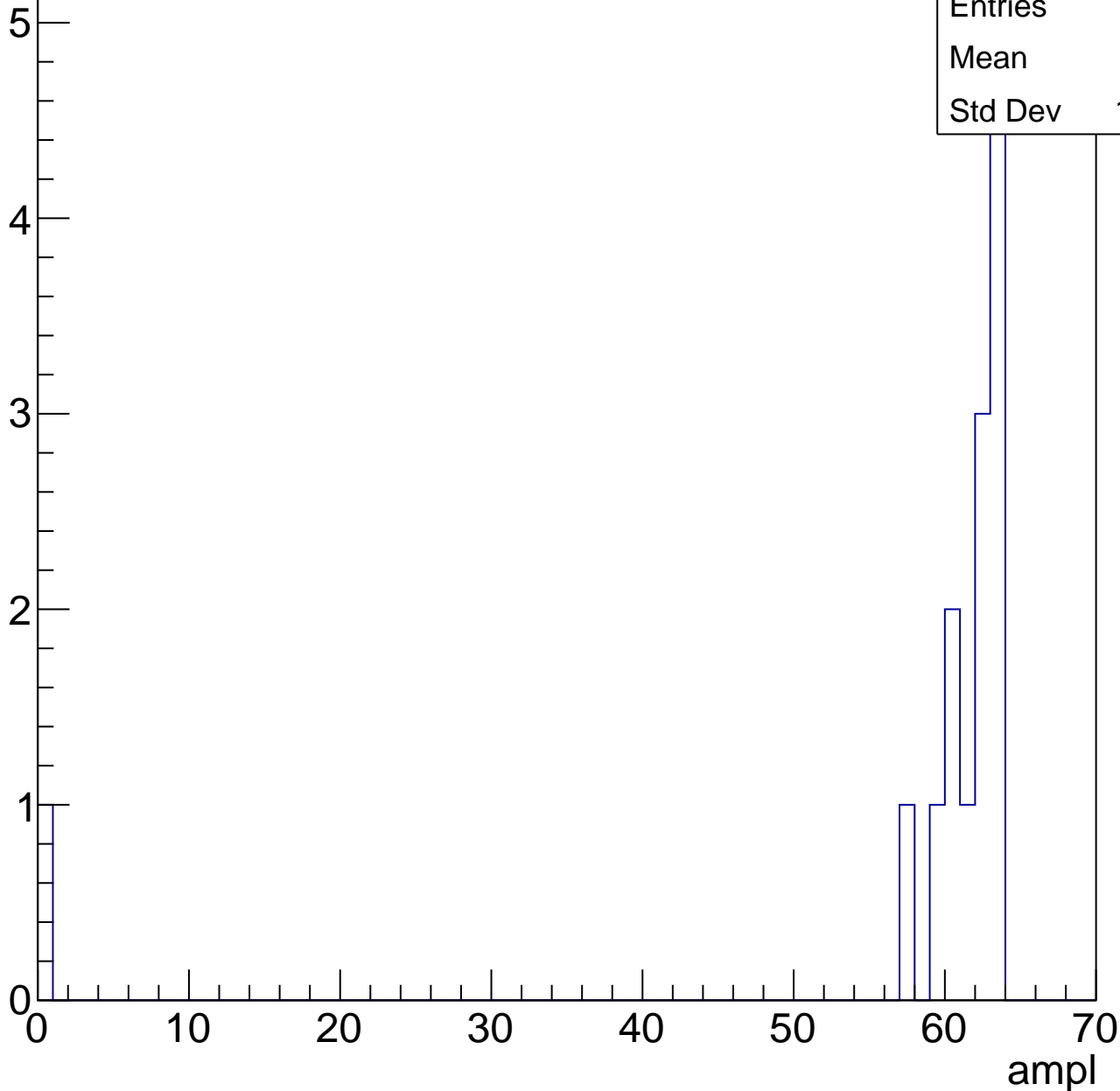
Entries	66
Mean	58.48
Std Dev	2.754

# B1L103S, U26-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	14
Mean	57
Std Dev	15.91





# B1L103S, U26-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	63
Std Dev	0

# B1L103S, U26-ch45, adc0

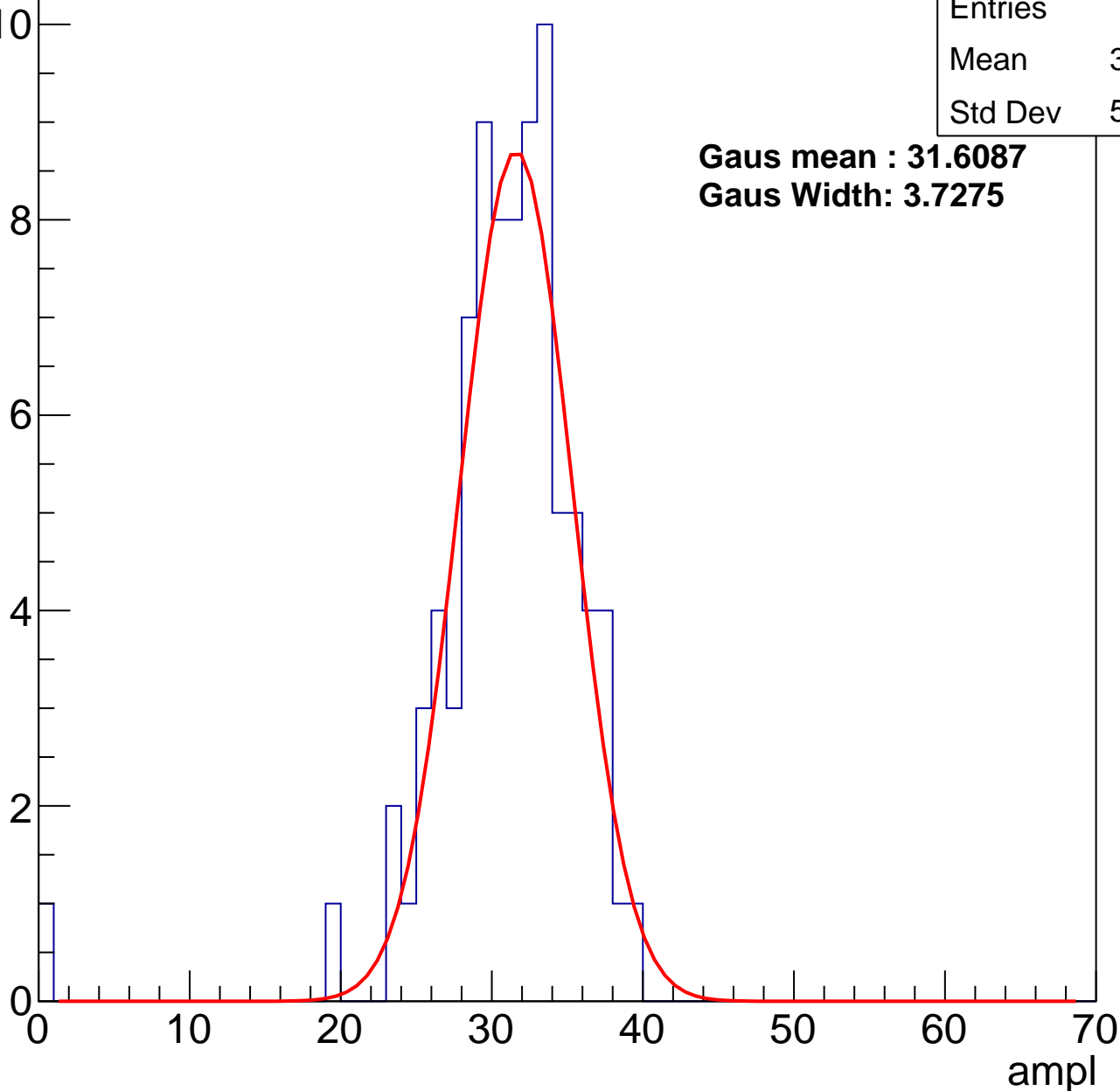
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	86
Mean	30.53
Std Dev	5.009

**Gaus mean : 31.6087**

**Gaus Width: 3.7275**



# B1L103S, U26-ch45, adc1

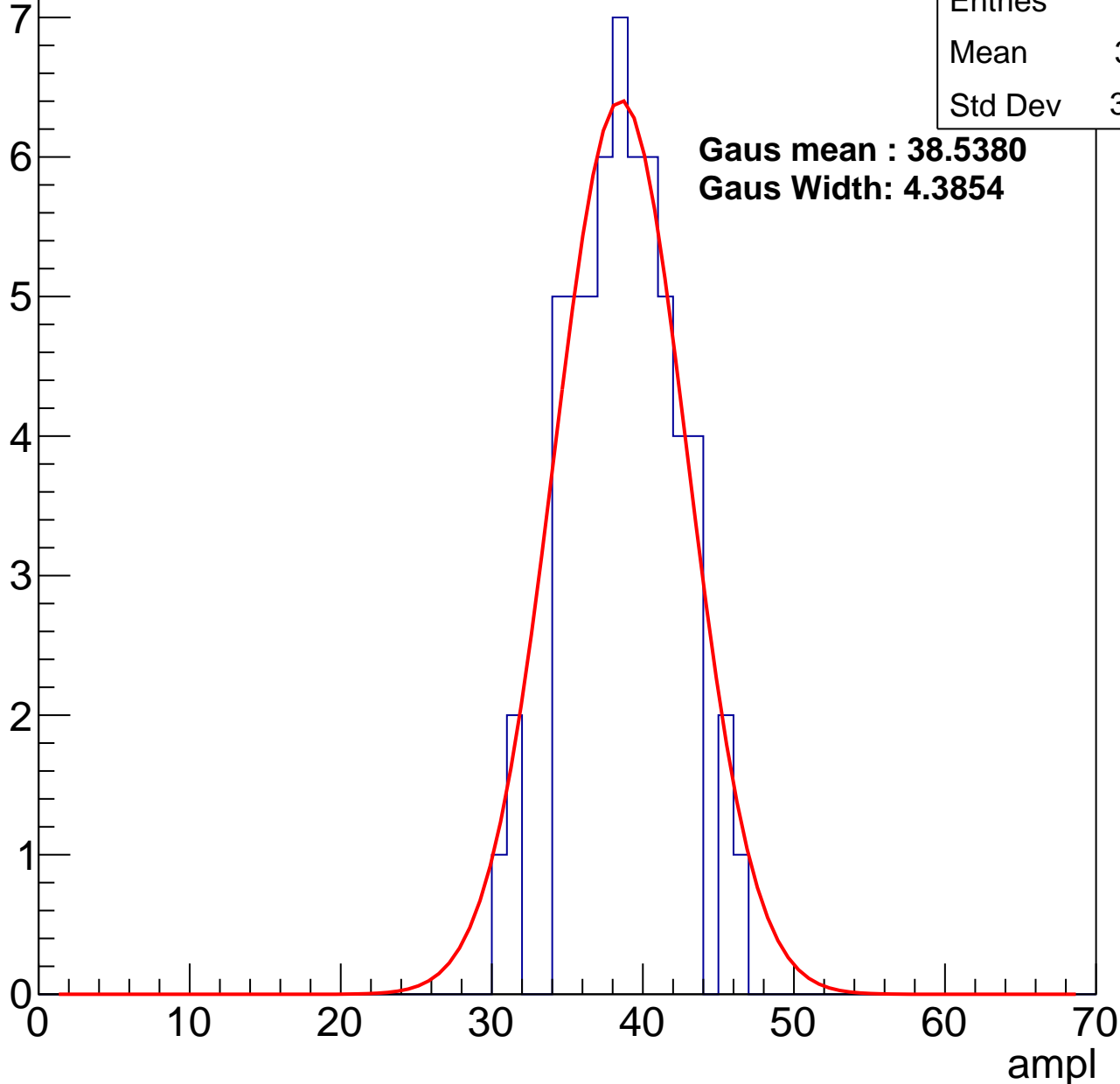
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	38.31
Std Dev	3.465

**Gaus mean : 38.5380**

**Gaus Width: 4.3854**



# B1L103S, U26-ch45, adc2

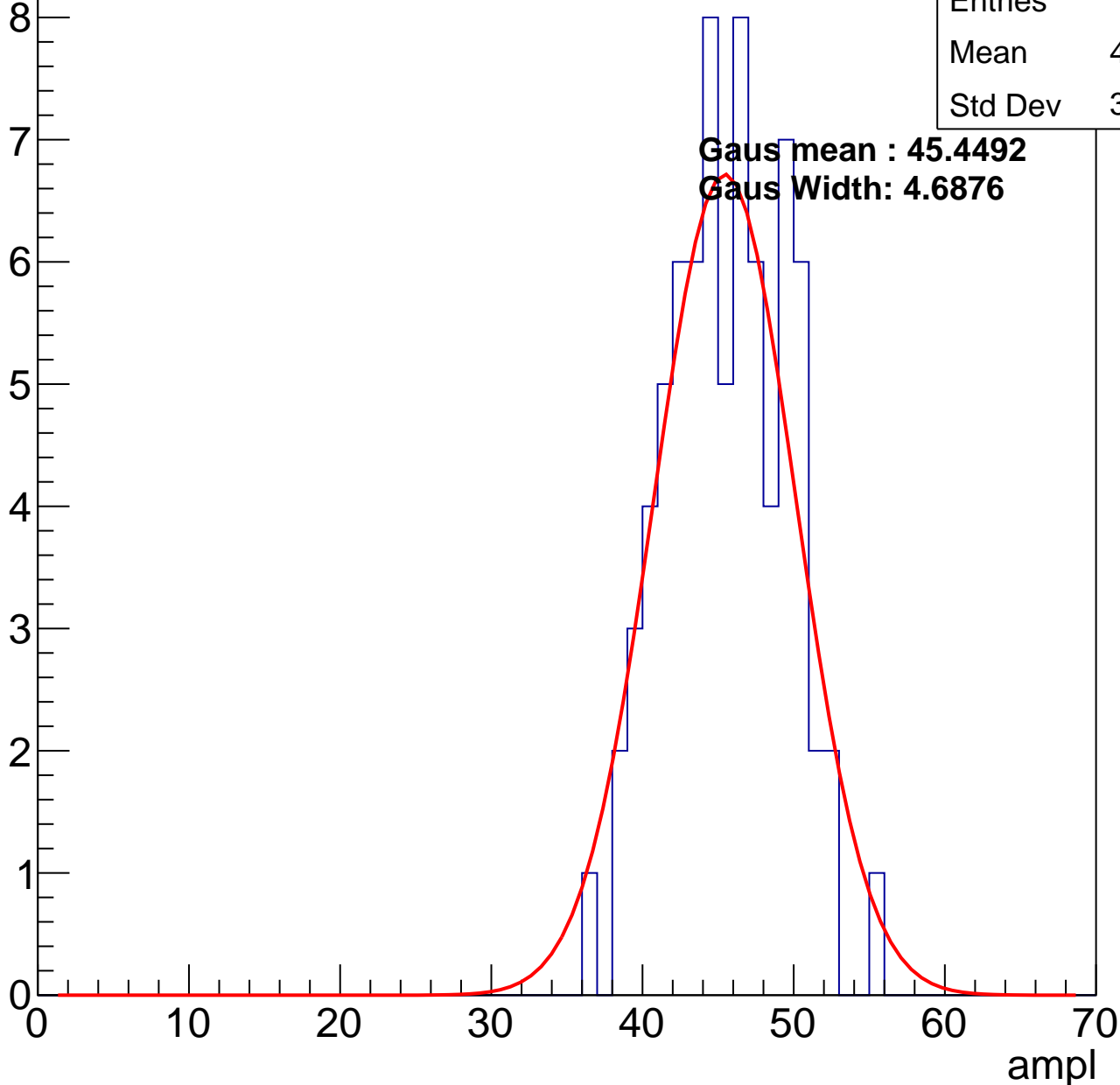
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	45.09
Std Dev	3.894

Gaus mean : 45.4492

Gaus Width: 4.6876

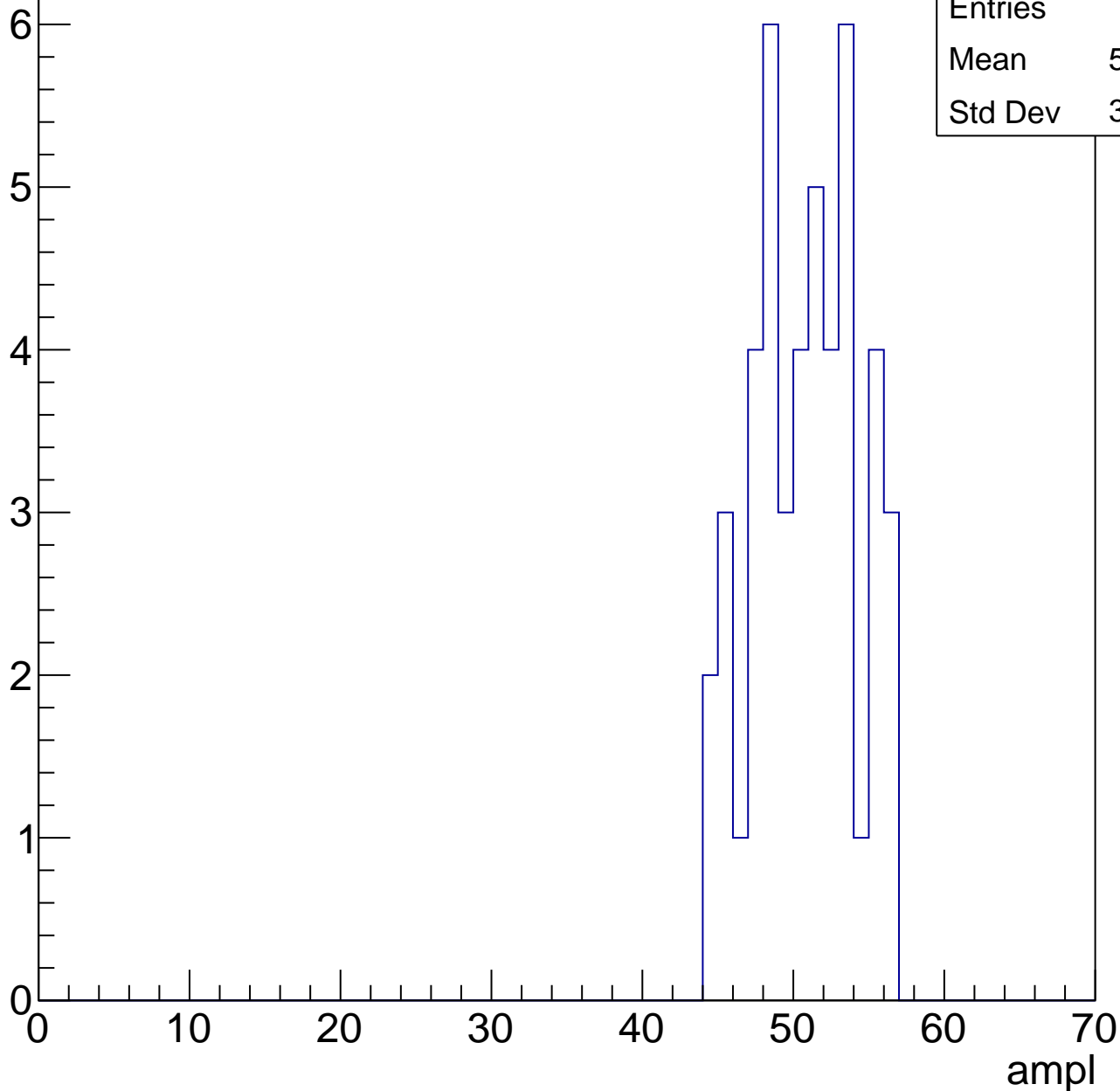


# B1L103S, U26-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	50.33
Std Dev	3.363

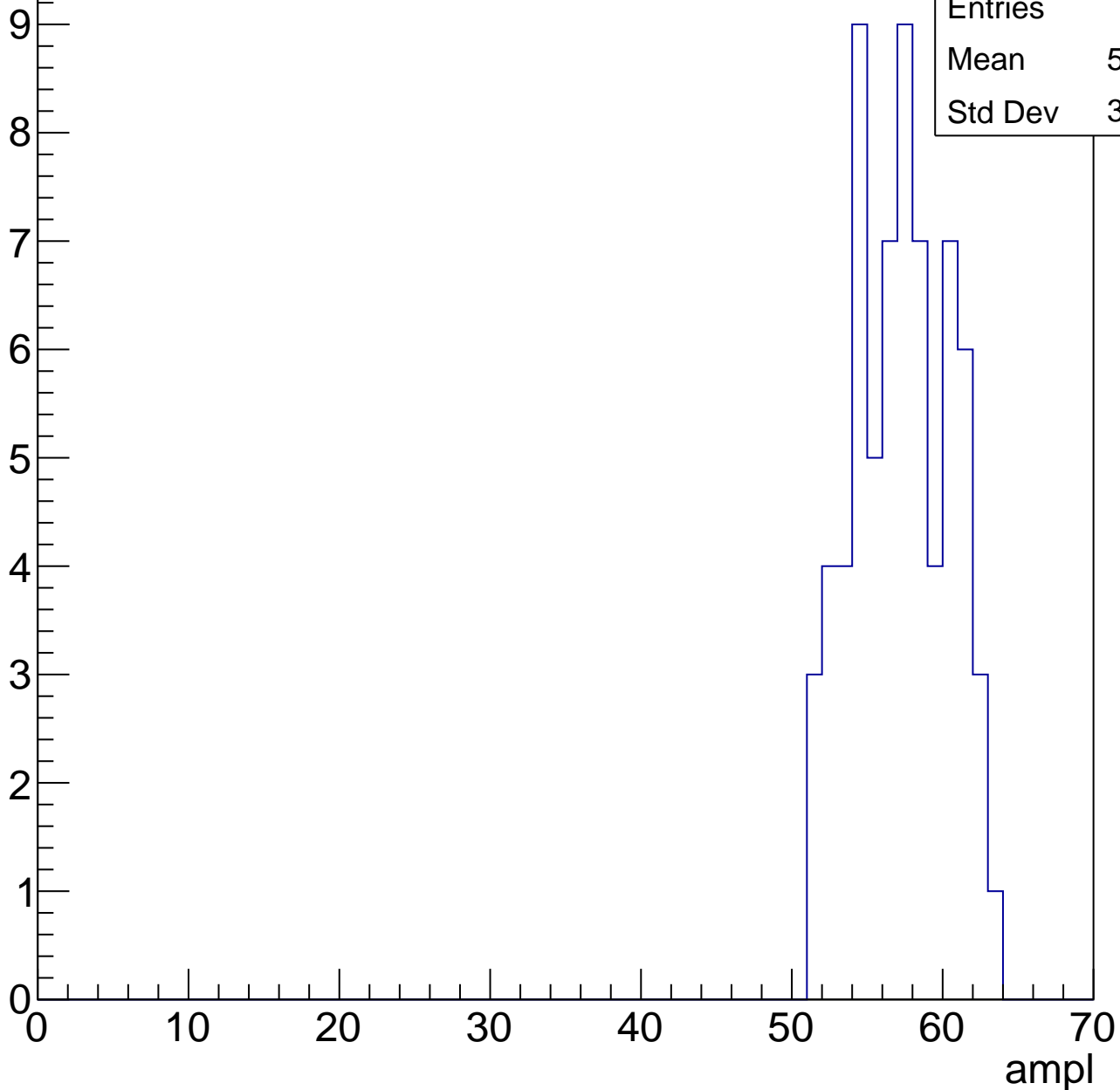


# B1L103S, U26-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	56.75
Std Dev	3.113

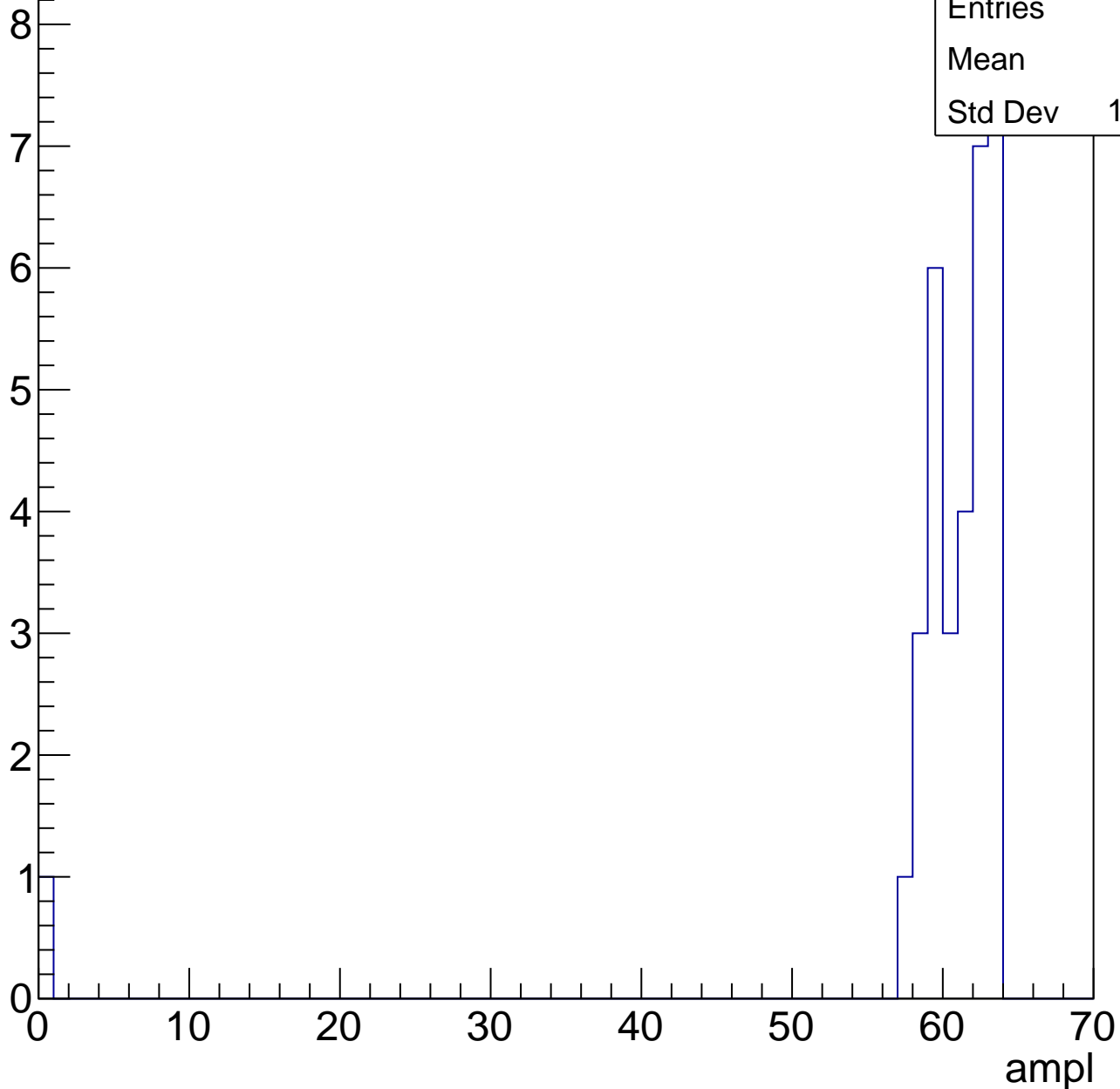


# B1L103S, U26-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	33
Mean	59
Std Dev	10.59



# B1L103S, U26-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U26-ch46, adc0

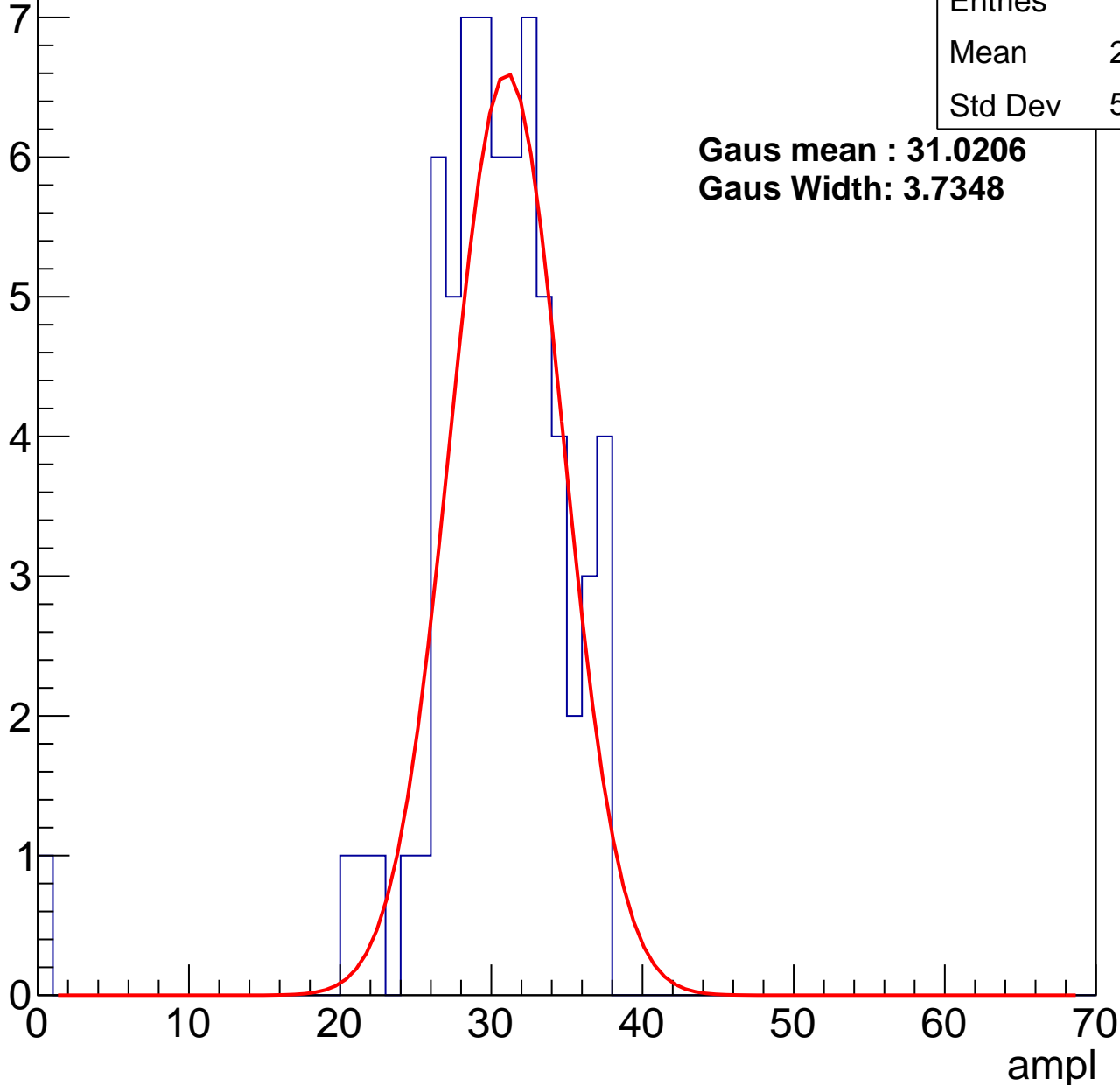
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	29.69
Std Dev	5.248

**Gaus mean : 31.0206**

**Gaus Width: 3.7348**



# B1L103S, U26-ch46, adc1

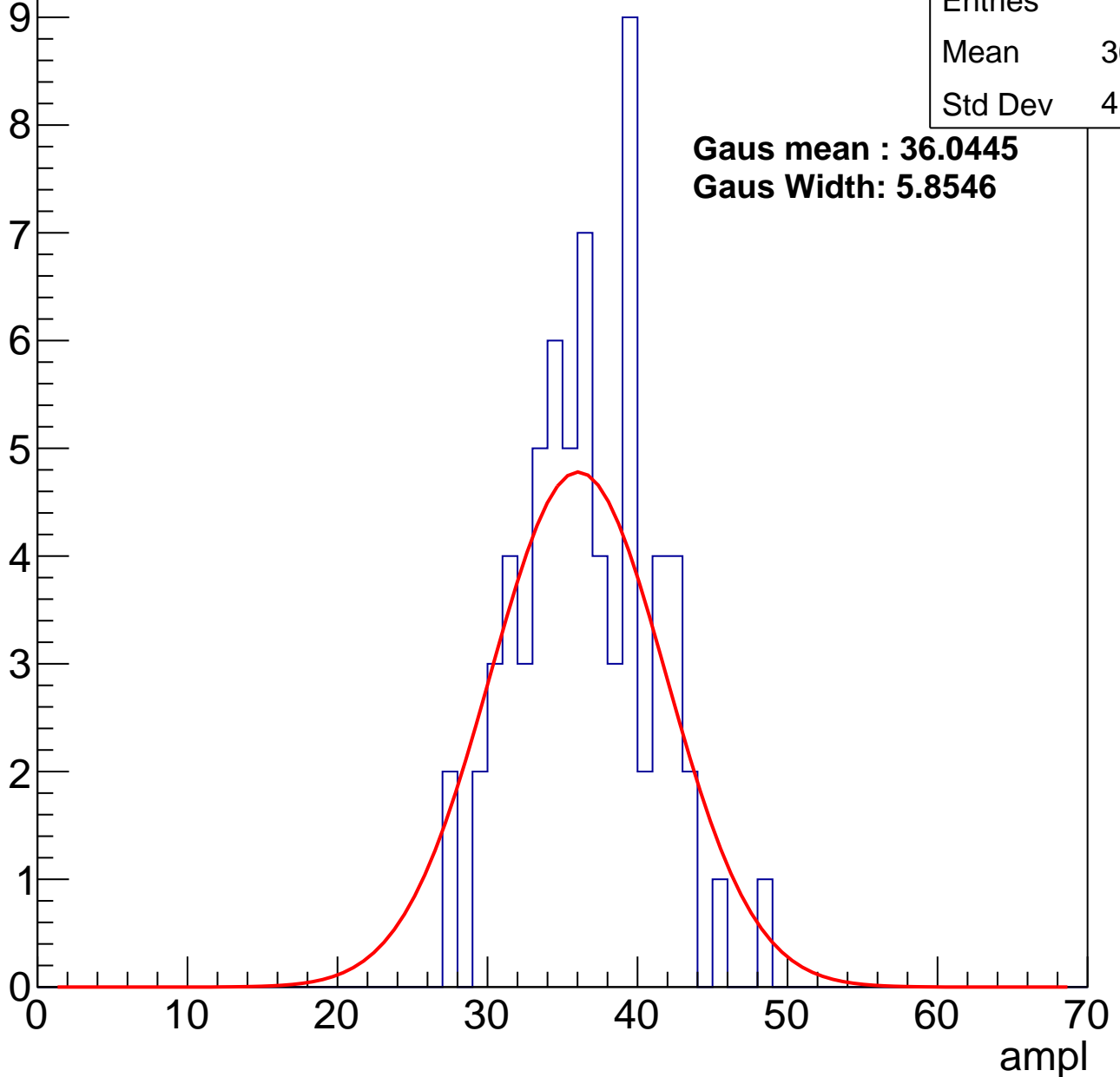
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	36.15
Std Dev	4.379

**Gaus mean : 36.0445**

**Gaus Width: 5.8546**



# B1L103S, U26-ch46, adc2

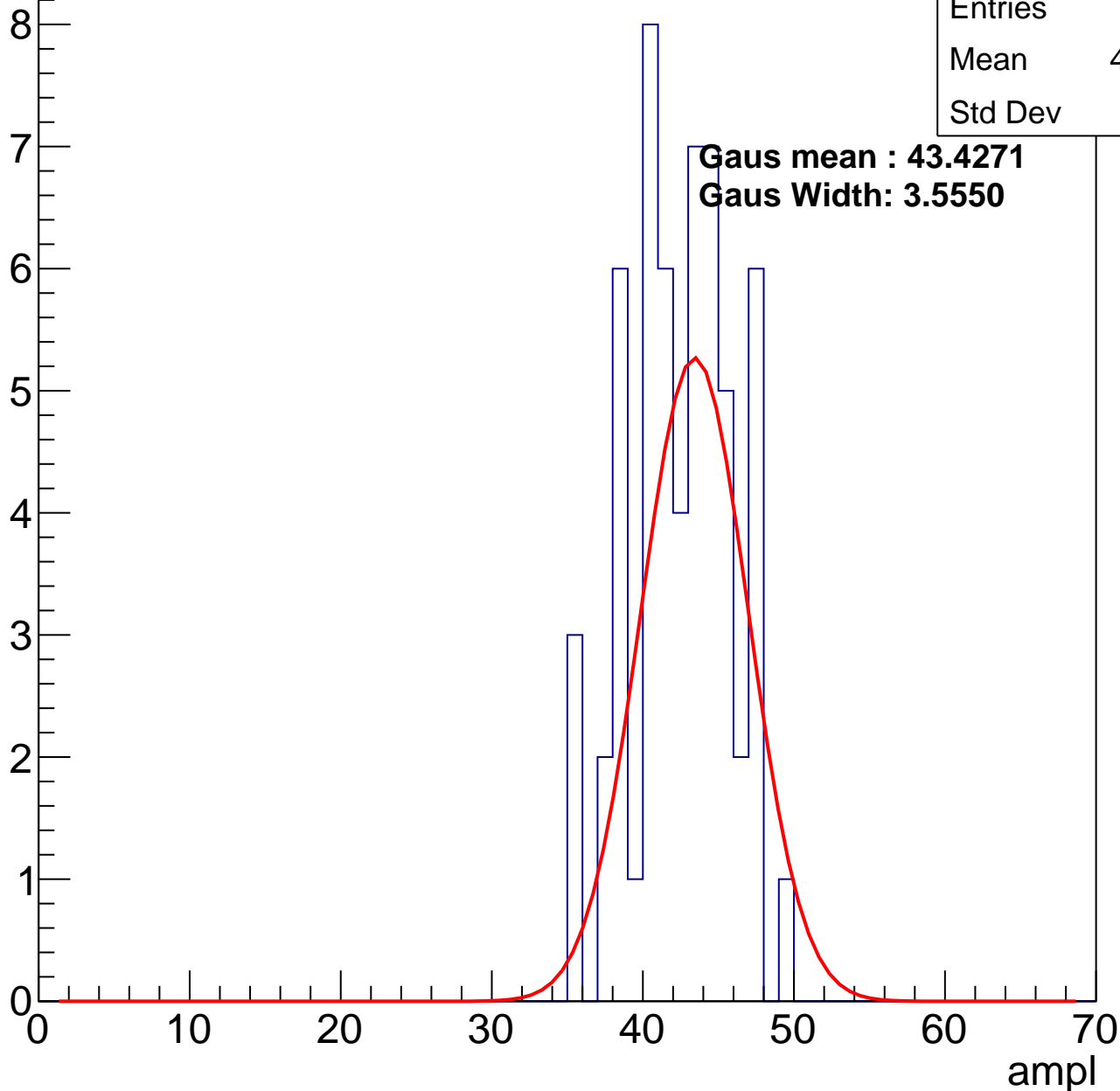
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	42.02
Std Dev	3.35

**Gaus mean : 43.4271**

**Gaus Width: 3.5550**

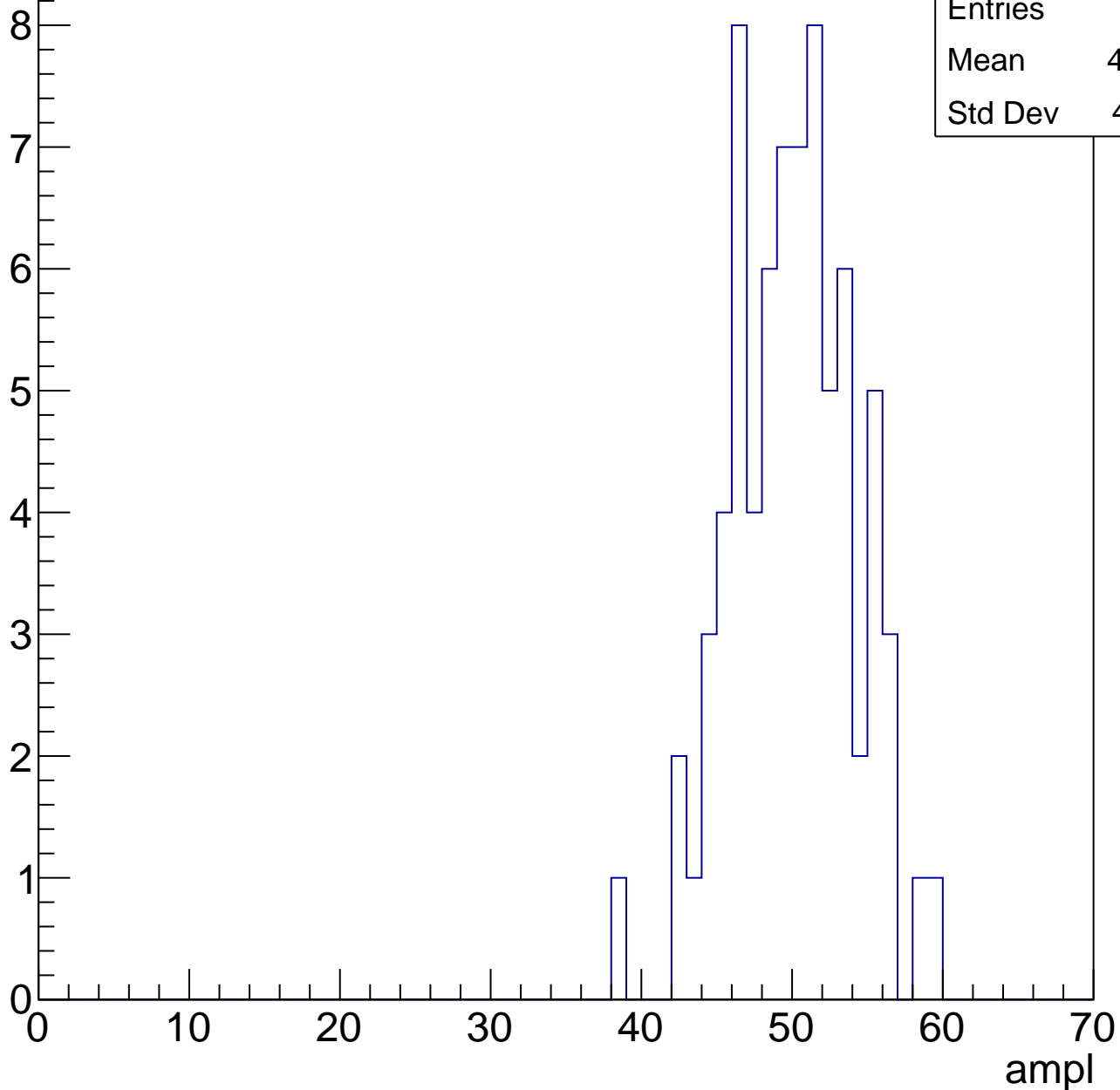


# B1L103S, U26-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

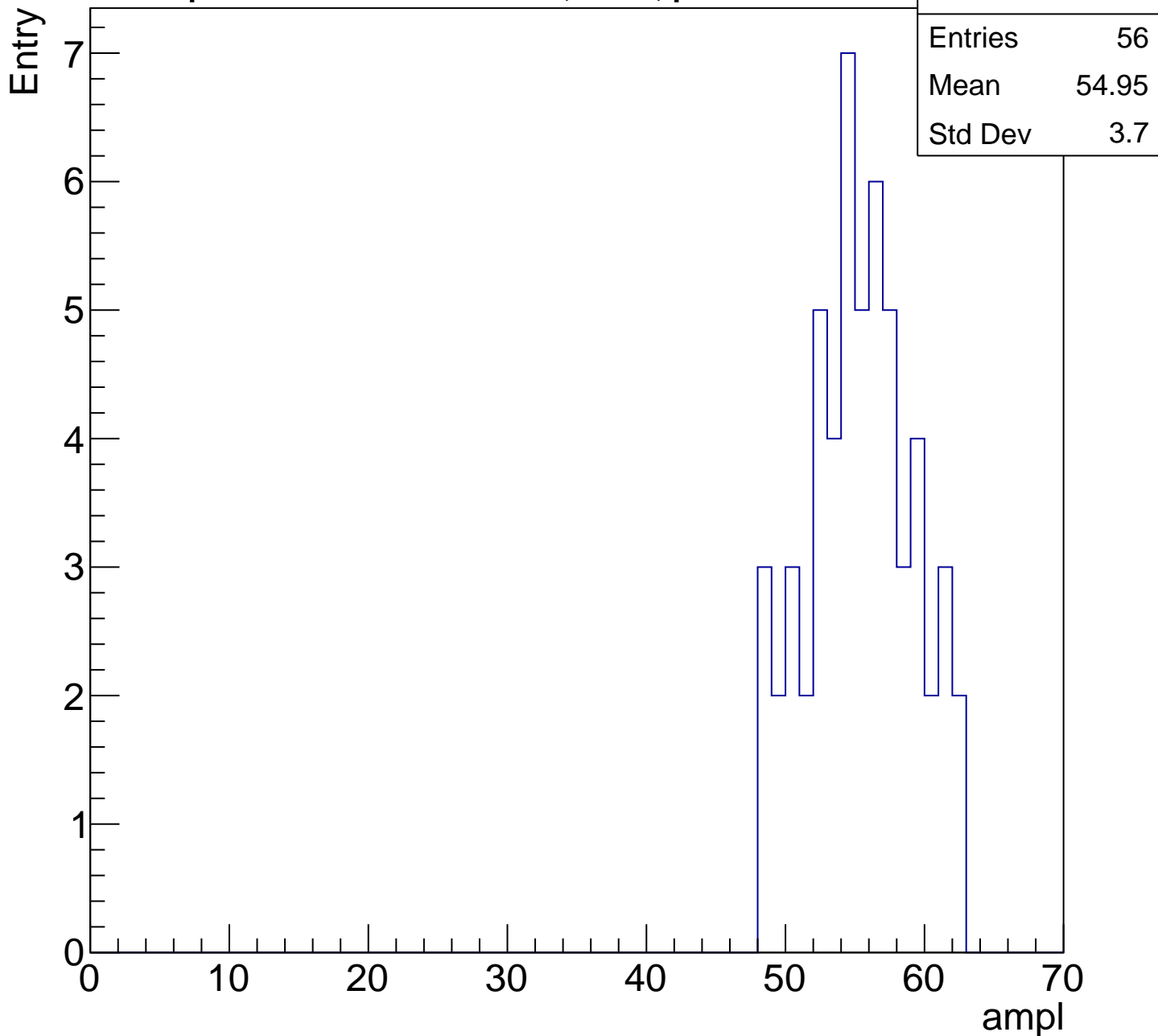
Entry

Entries	74
Mean	49.57
Std Dev	4.031



# B1L103S, U26-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

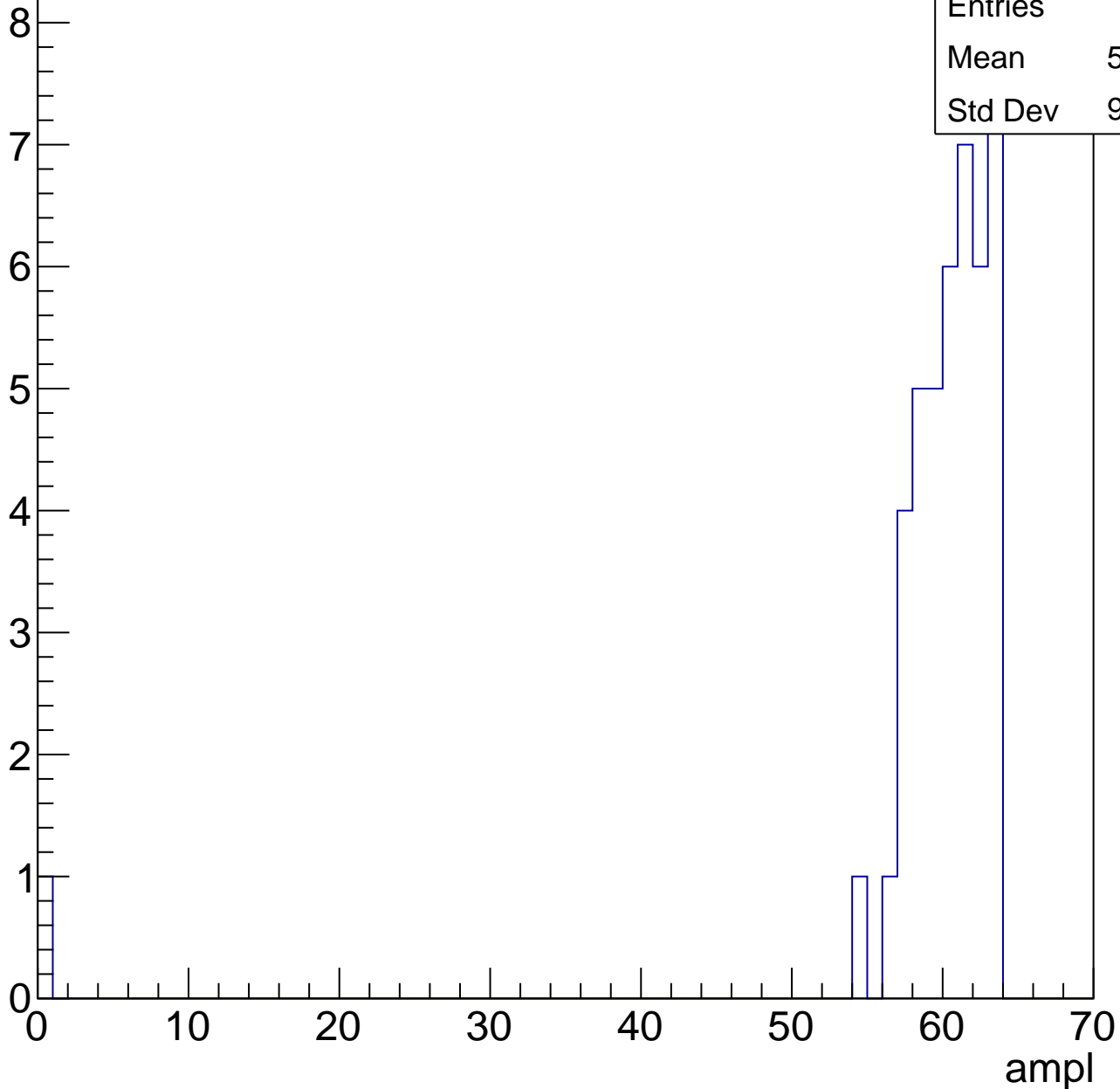


# B1L103S, U26-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	58.77
Std Dev	9.232



# B1L103S, U26-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

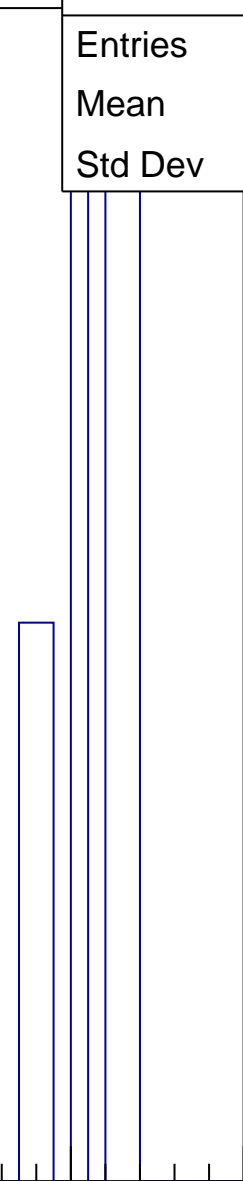
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	8
Mean	60.62
Std Dev	2.118

0 10 20 30 40 50 60 70

ampl





# B1L103S, U26-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U26-ch47, adc0

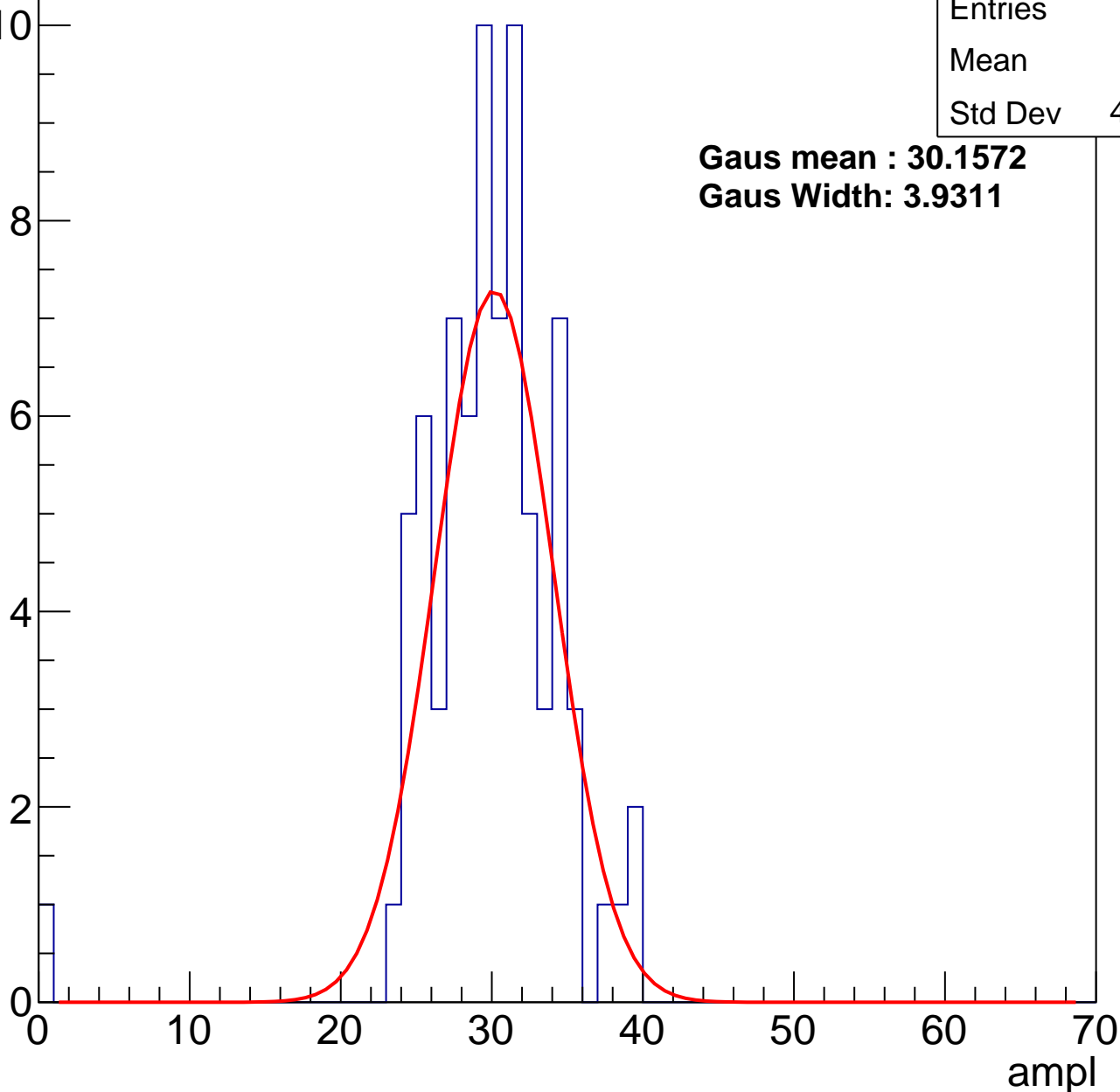
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	29.4
Std Dev	4.955

**Gaus mean : 30.1572**

**Gaus Width: 3.9311**



# B1L103S, U26-ch47, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	73
Mean	36.84
Std Dev	3.569

**Gaus mean : 37.0945**

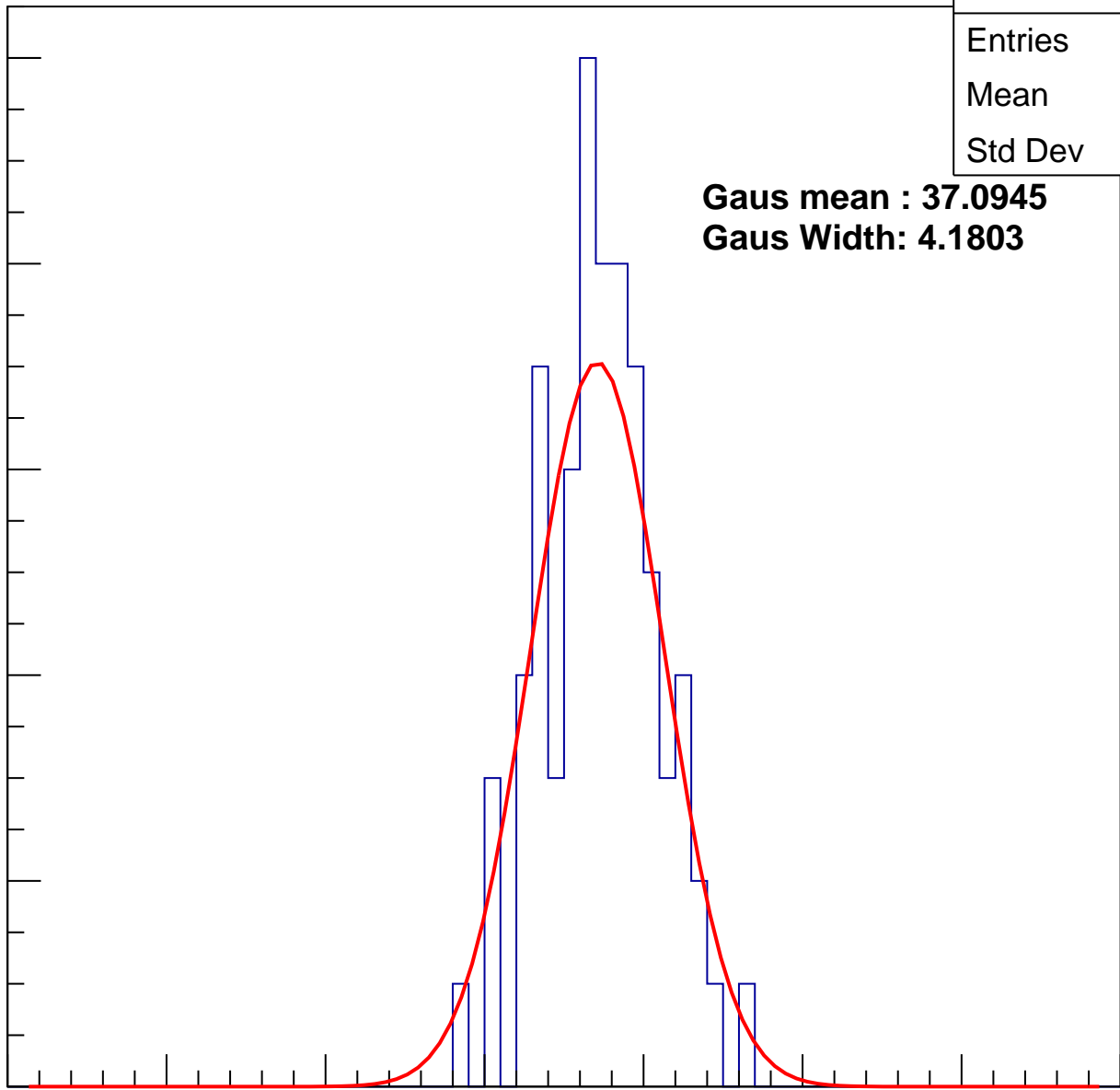
**Gaus Width: 4.1803**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch47, adc2

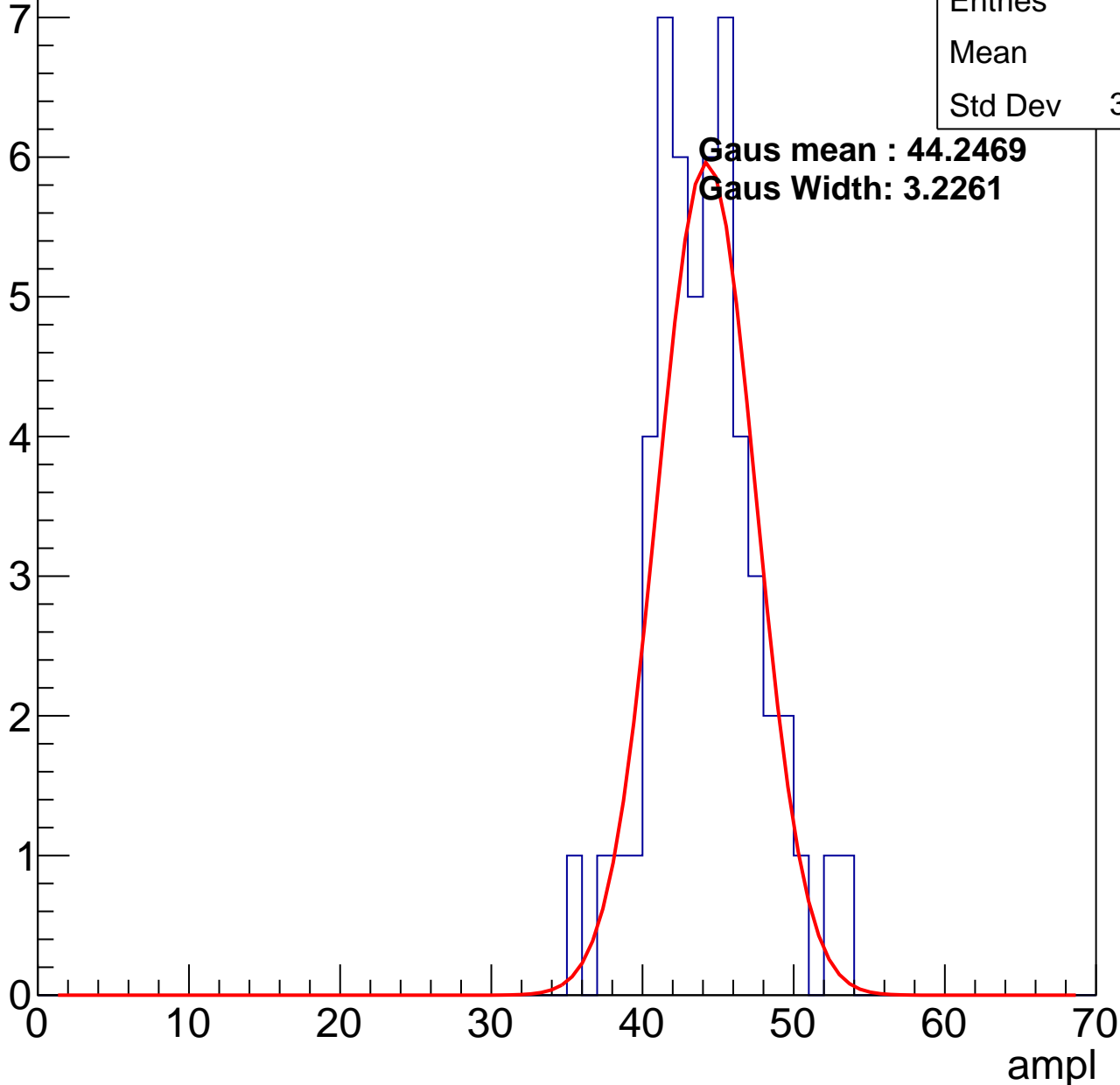
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	43.7
Std Dev	3.516

**Gaus mean : 44.2469**

**Gaus Width: 3.2261**

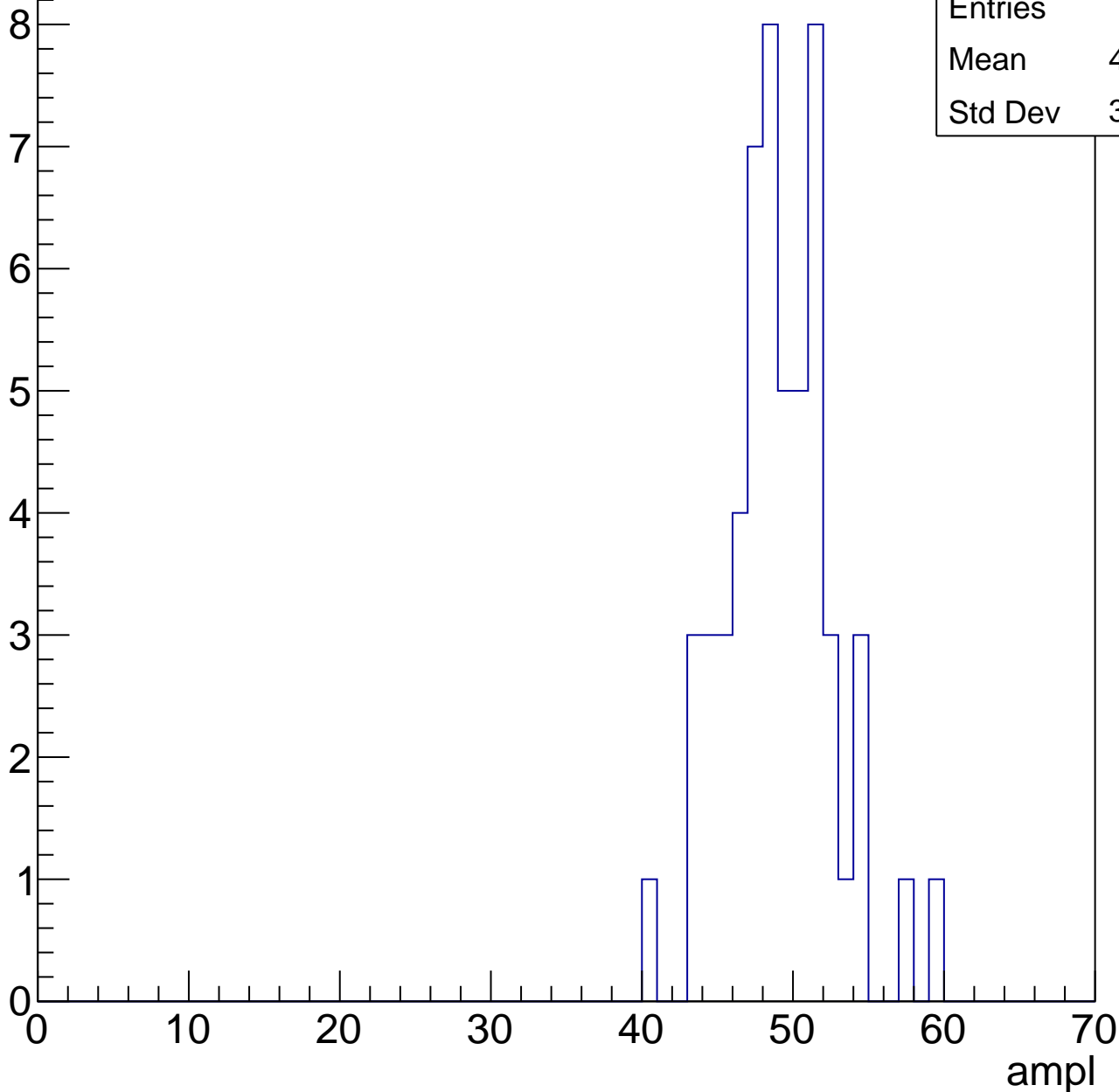


# B1L103S, U26-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	48.62
Std Dev	3.523

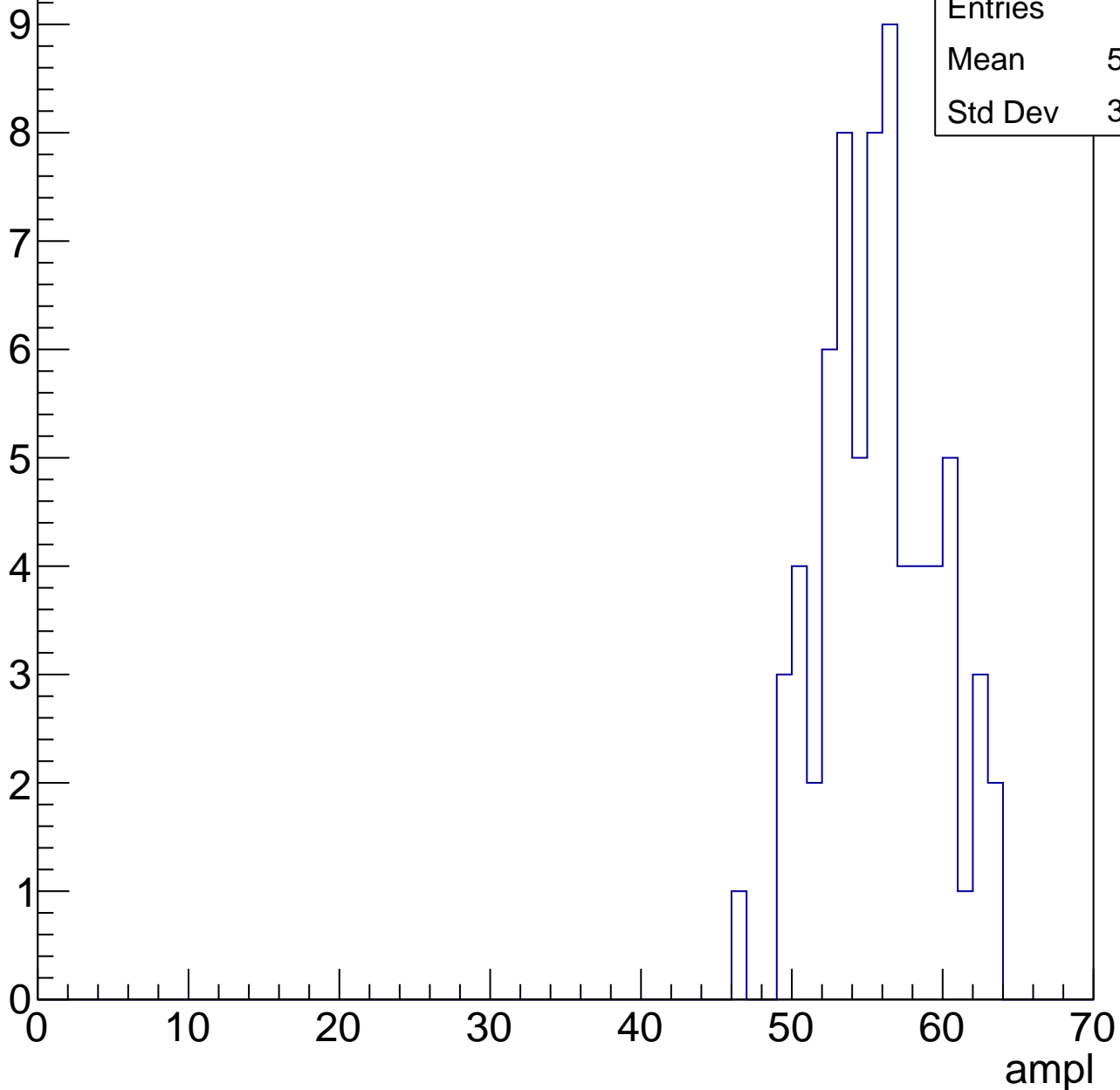


# B1L103S, U26-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	55.28
Std Dev	3.745

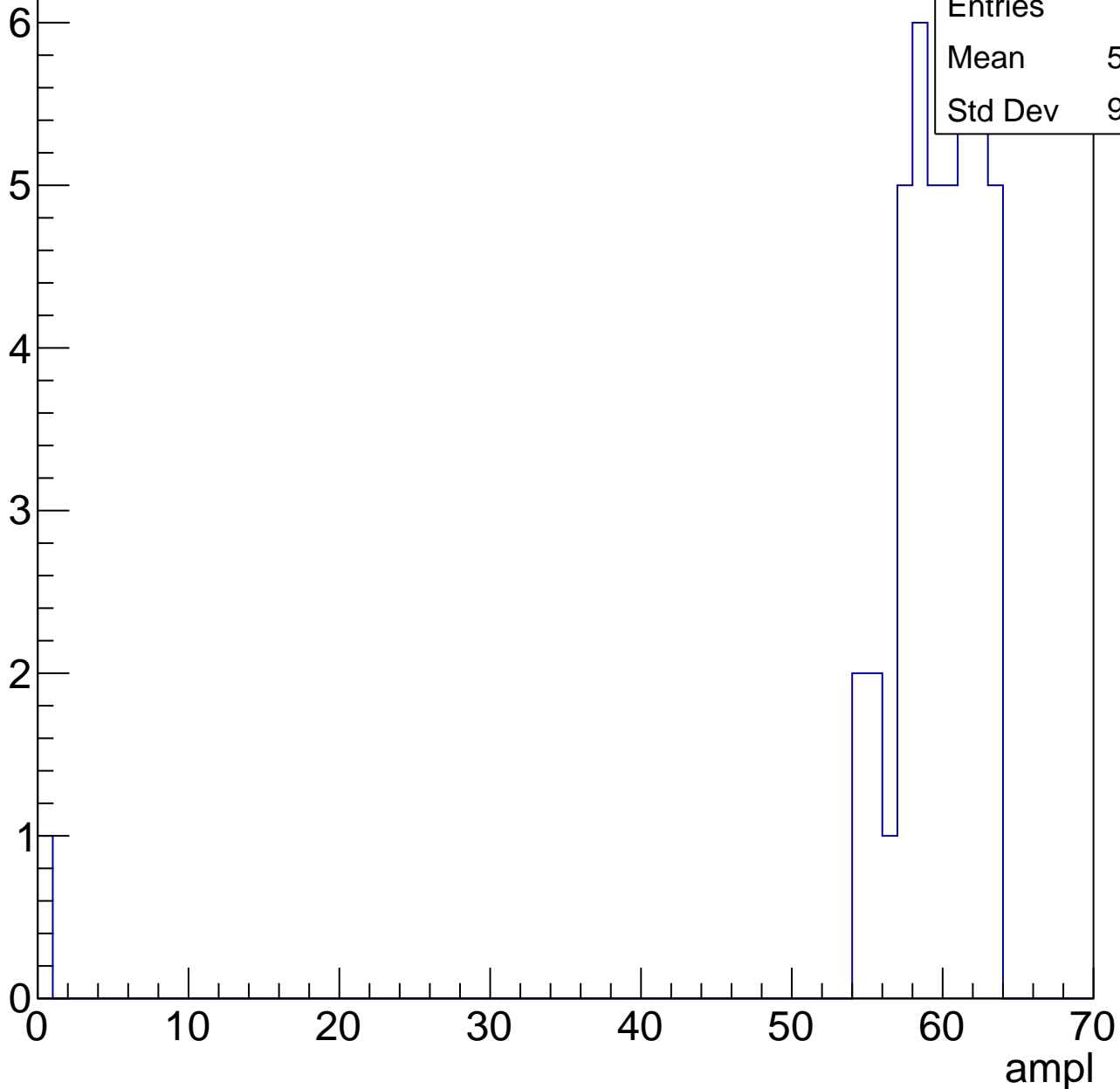


# B1L103S, U26-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	58.07
Std Dev	9.198



# B1L103S, U26-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

6

Mean

61.83

Std Dev

0.8975



# B1L103S, U26-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch48, adc0

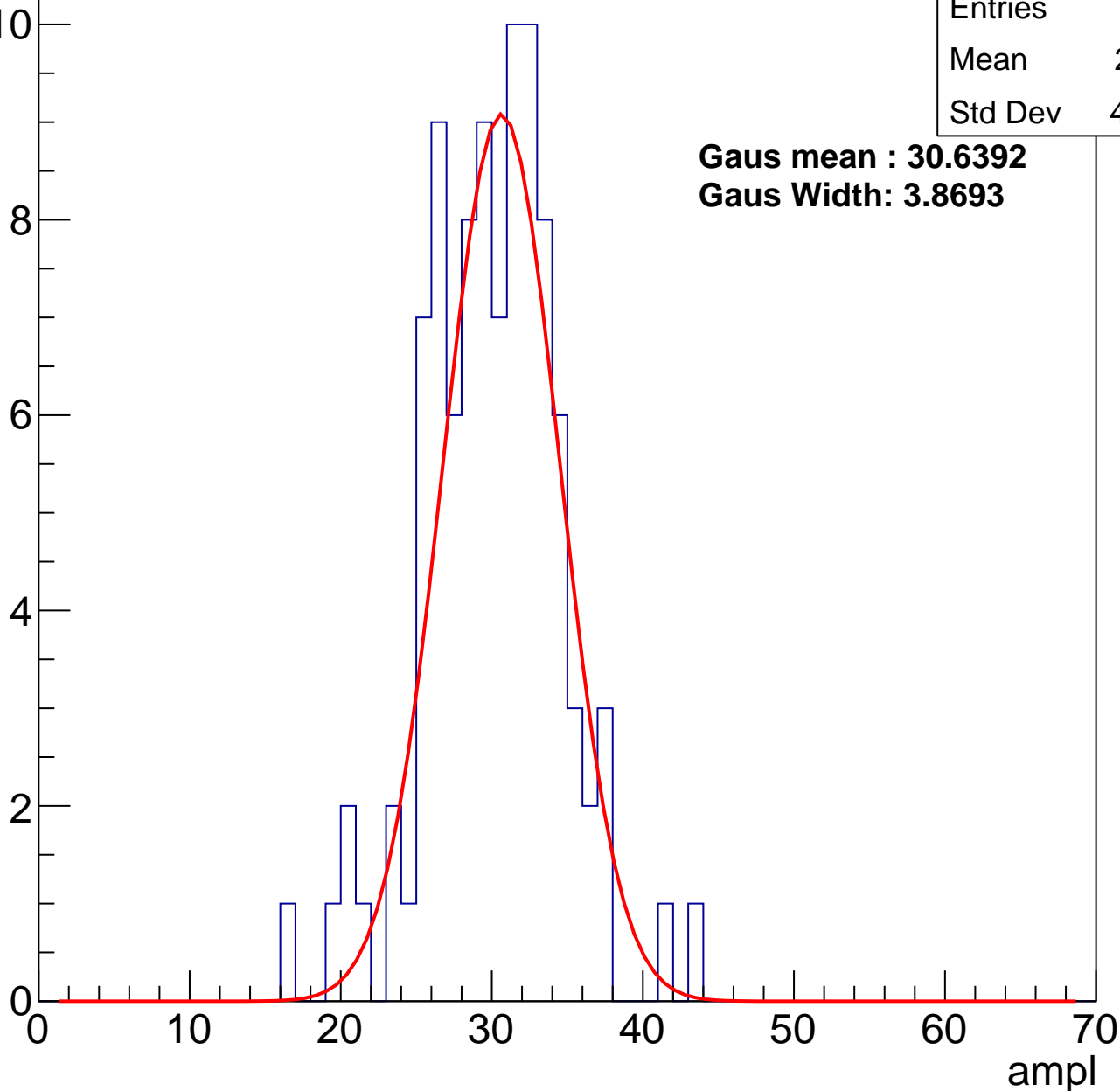
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	98
Mean	29.61
Std Dev	4.442

**Gaus mean : 30.6392**

**Gaus Width: 3.8693**



# B1L103S, U26-ch48, adc1

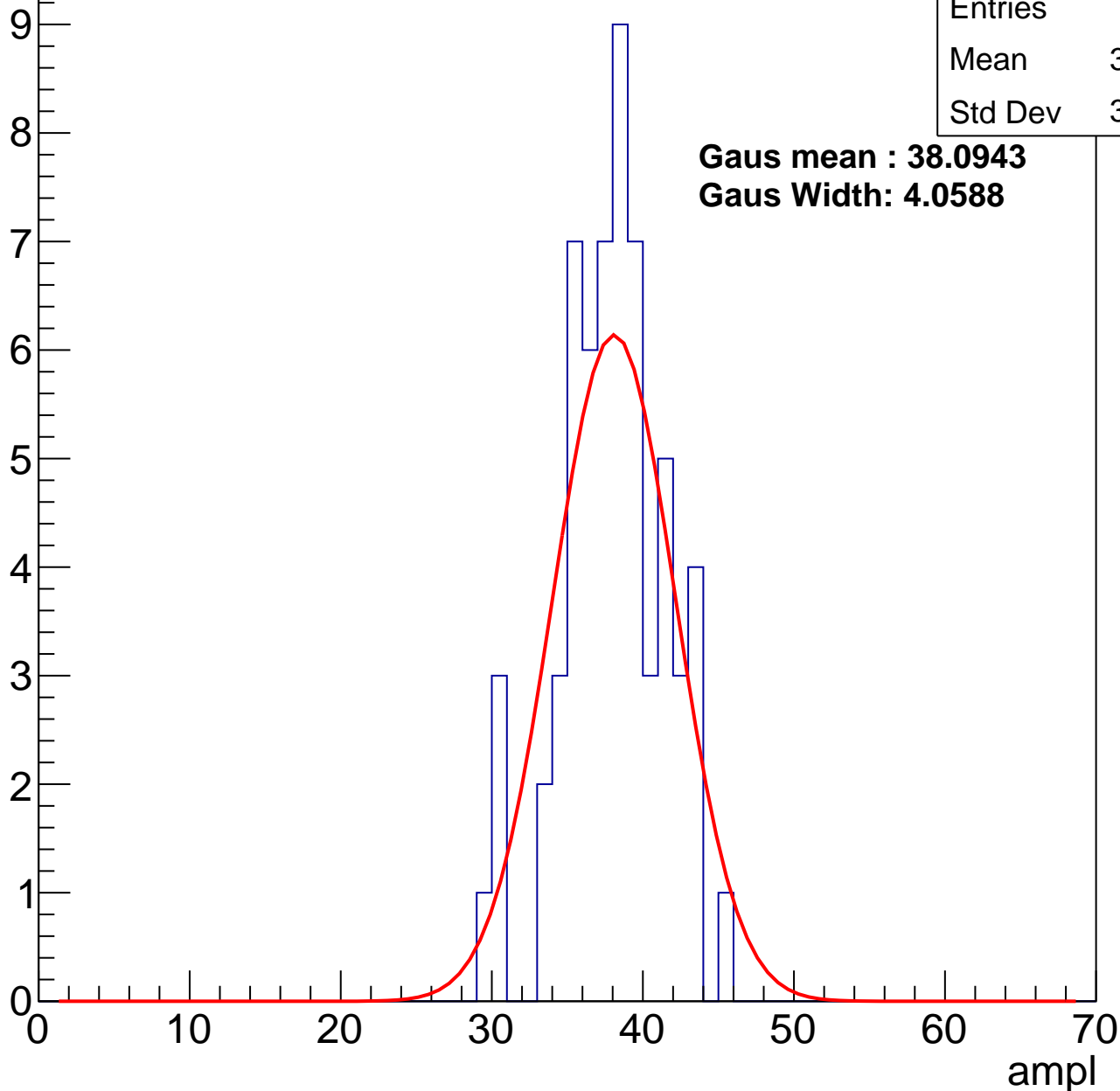
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	37.54
Std Dev	3.419

**Gaus mean : 38.0943**

**Gaus Width: 4.0588**



# B1L103S, U26-ch48, adc2

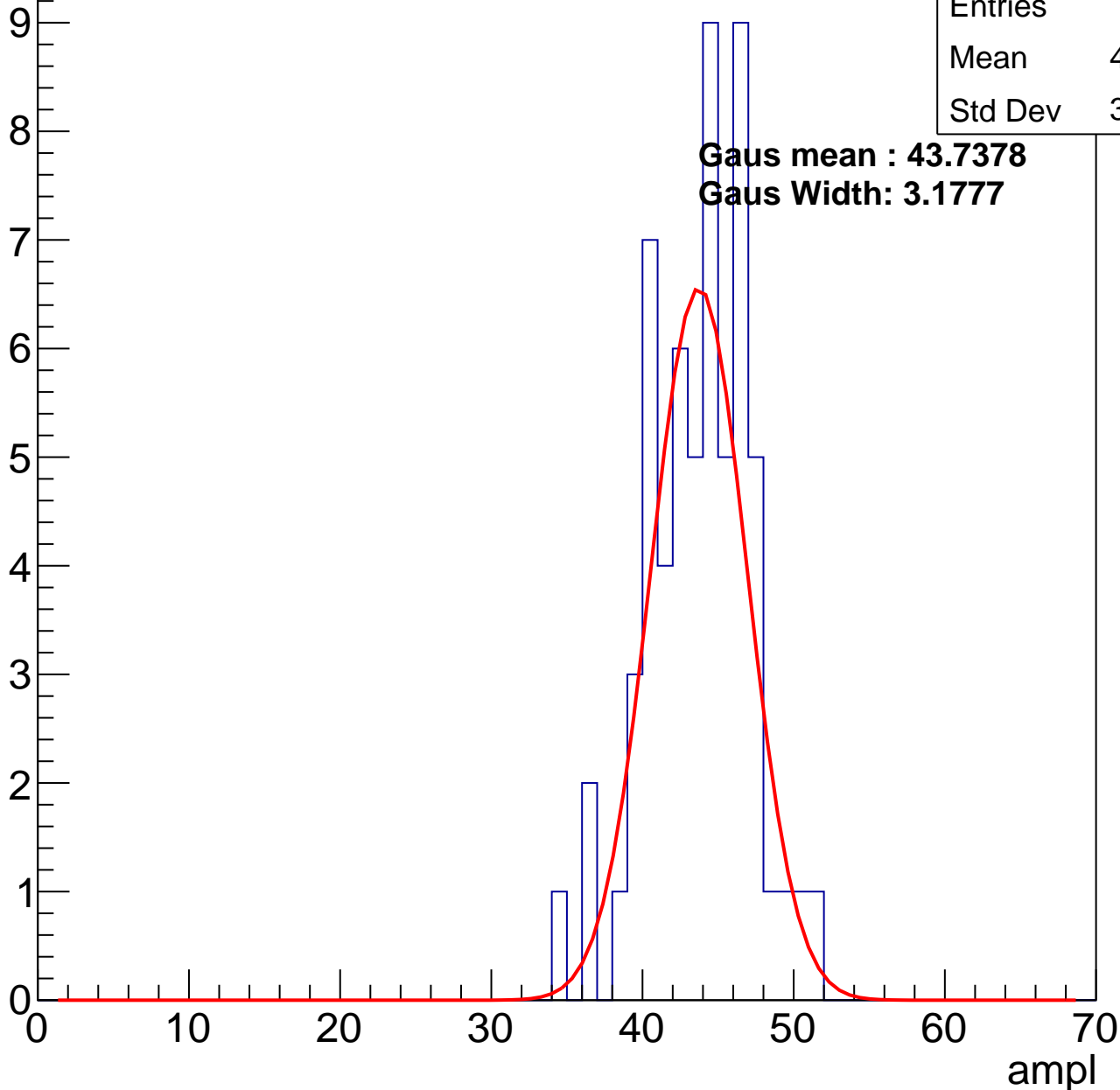
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	43.28
Std Dev	3.378

**Gaus mean : 43.7378**

**Gaus Width: 3.1777**

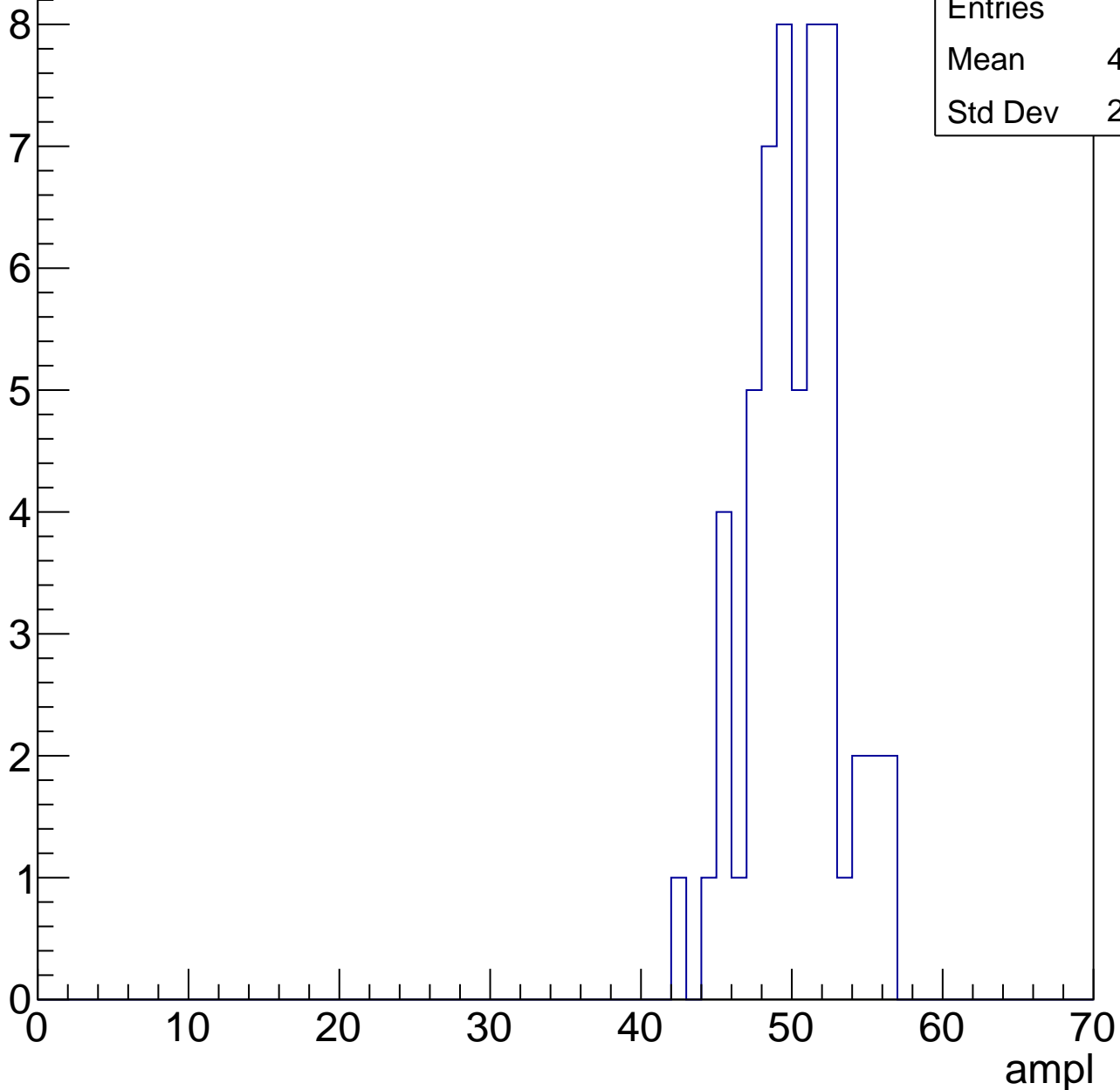


# B1L103S, U26-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	49.67
Std Dev	2.997

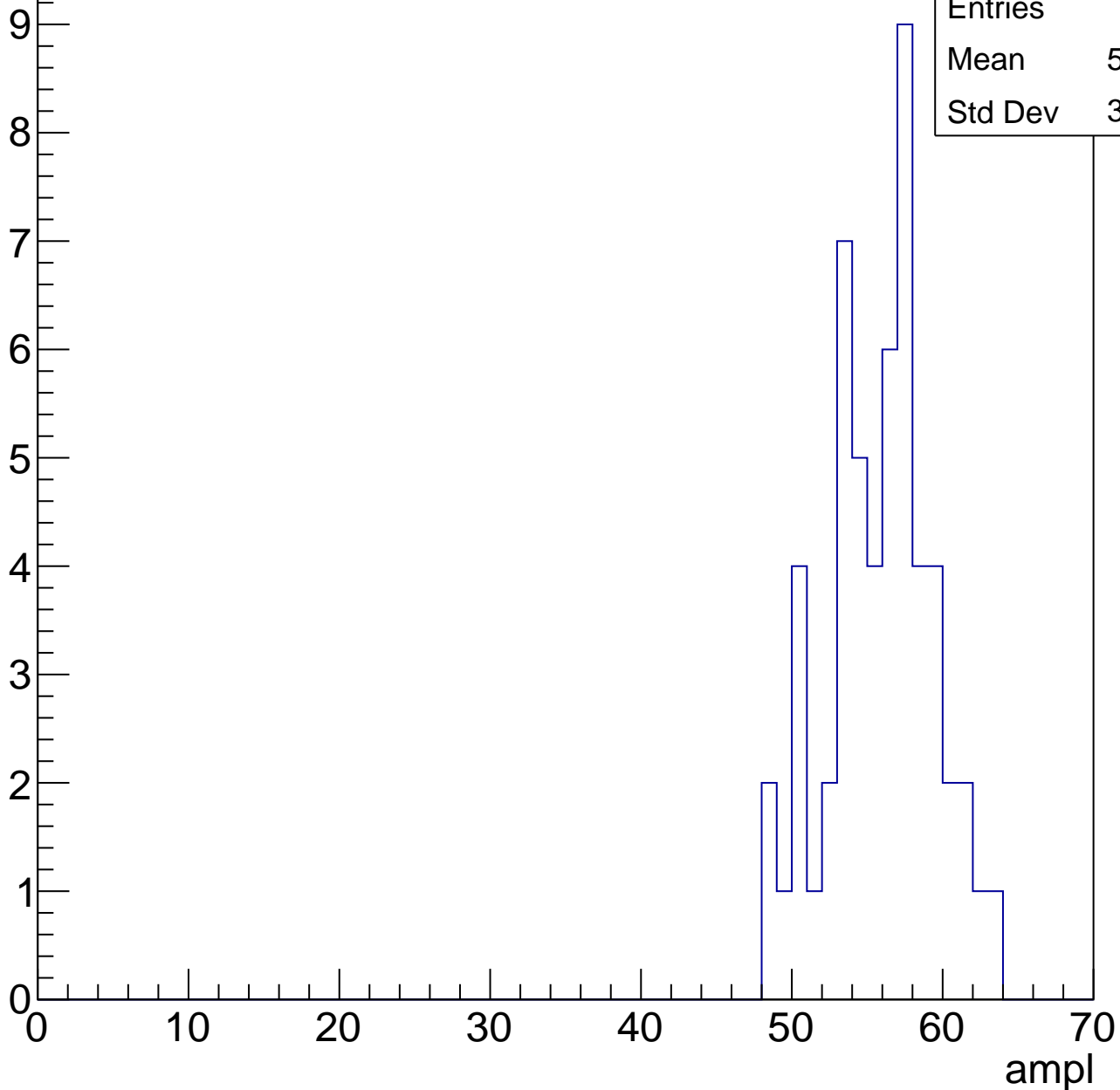


# B1L103S, U26-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	55.36
Std Dev	3.492

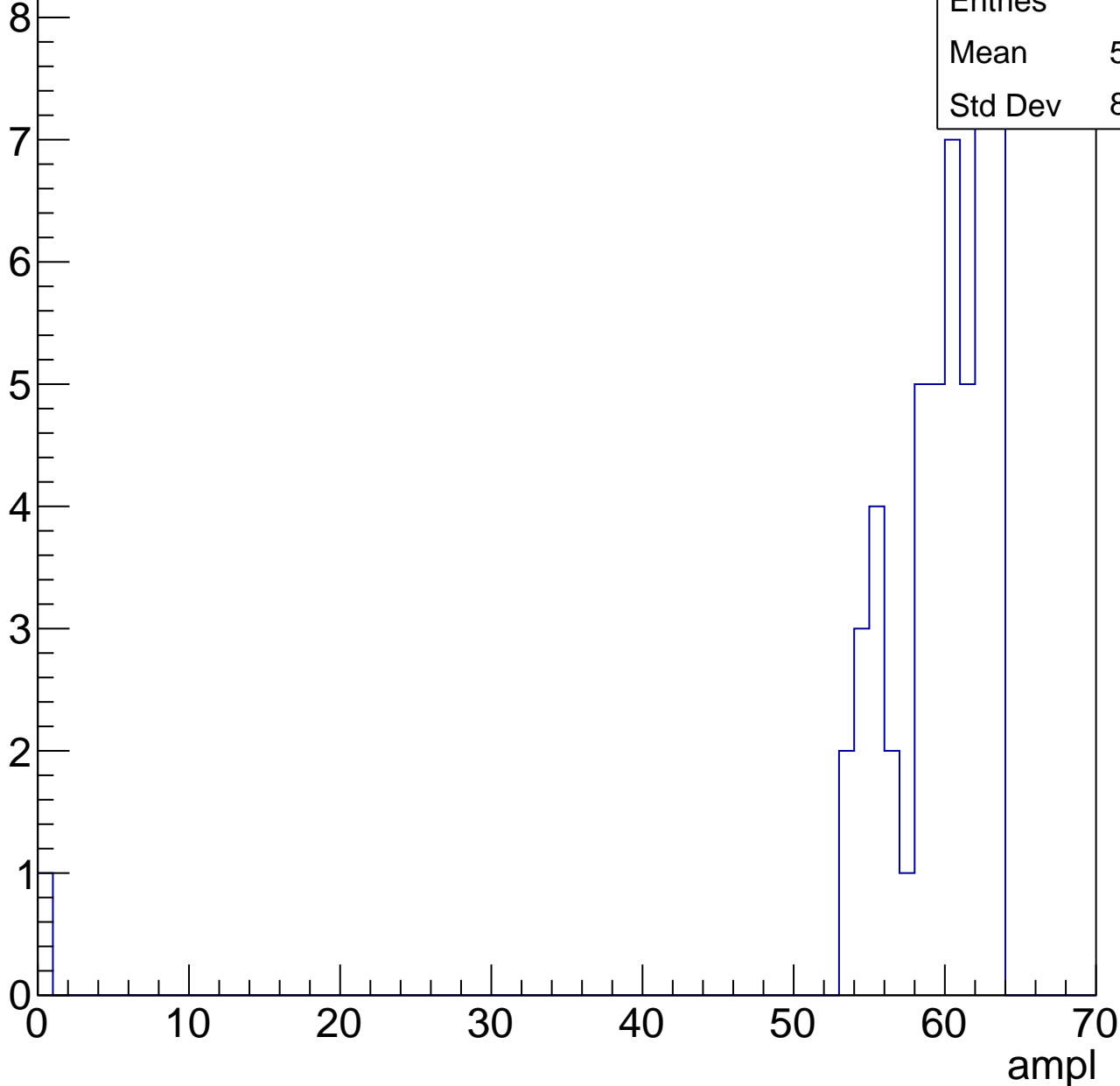


# B1L103S, U26-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

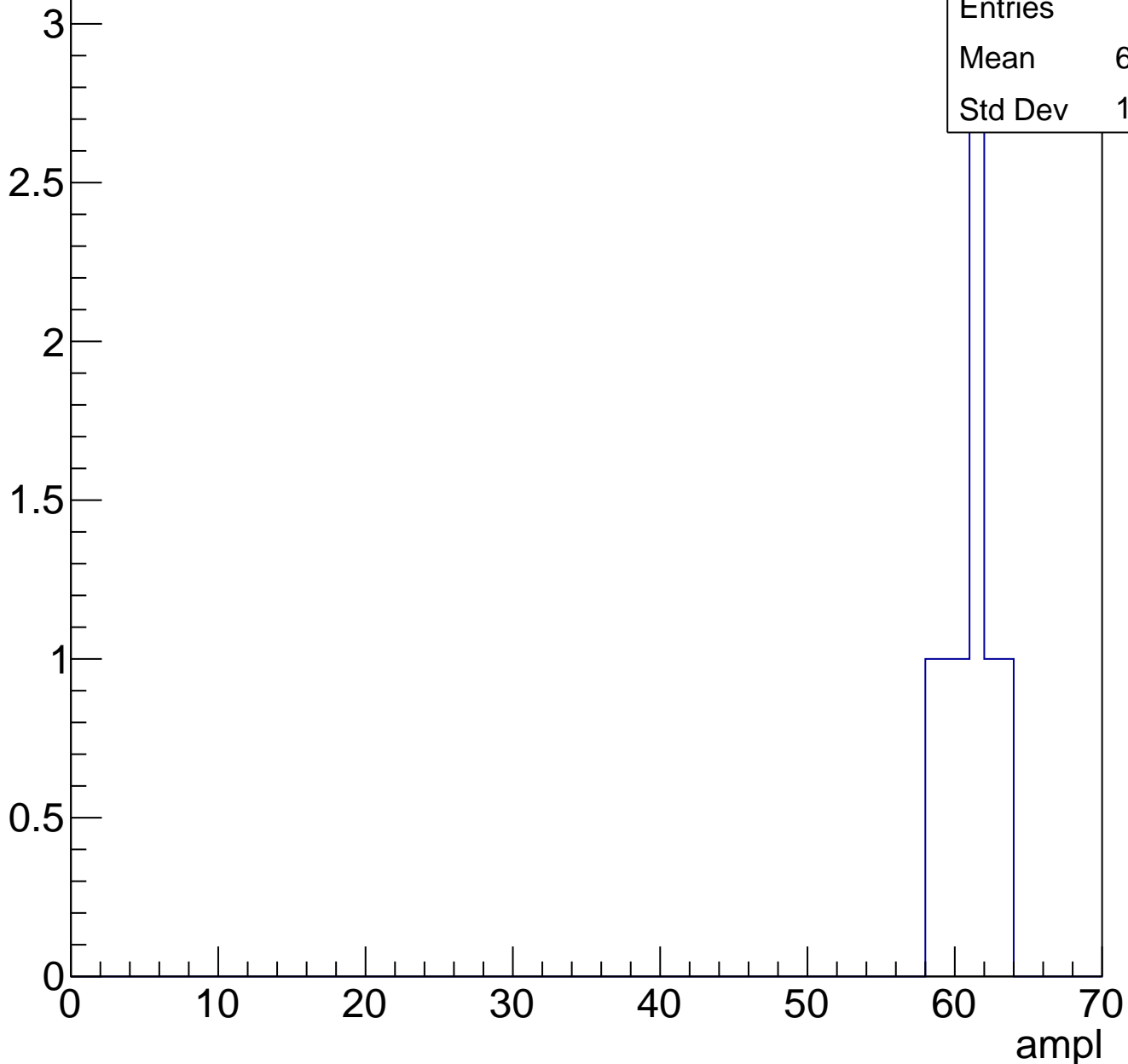
Entries	51
Mean	58.18
Std Dev	8.758



# B1L103S, U26-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U26-ch49, adc0

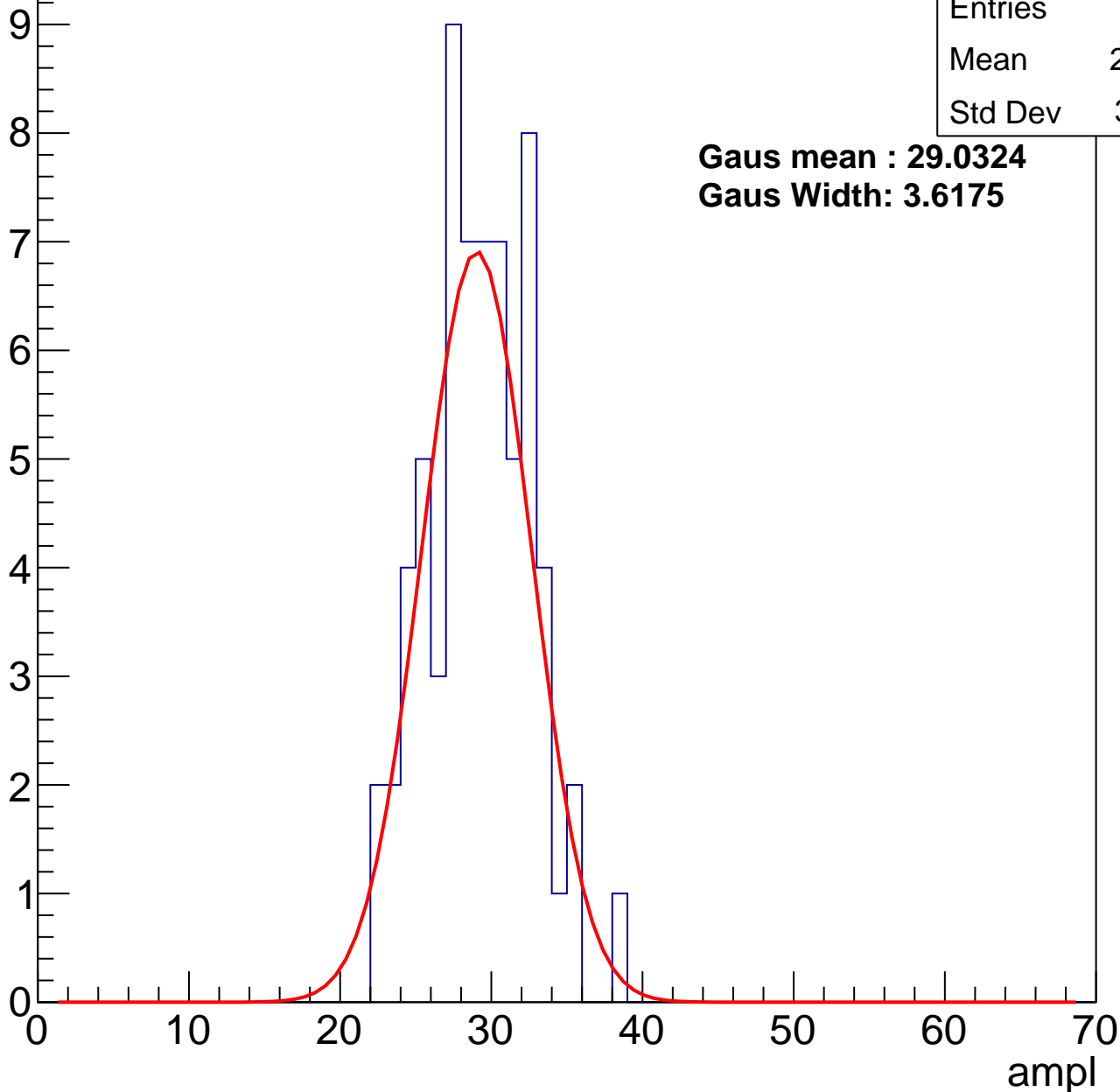
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	28.75
Std Dev	3.361

**Gaus mean : 29.0324**

**Gaus Width: 3.6175**



# B1L103S, U26-ch49, adc1

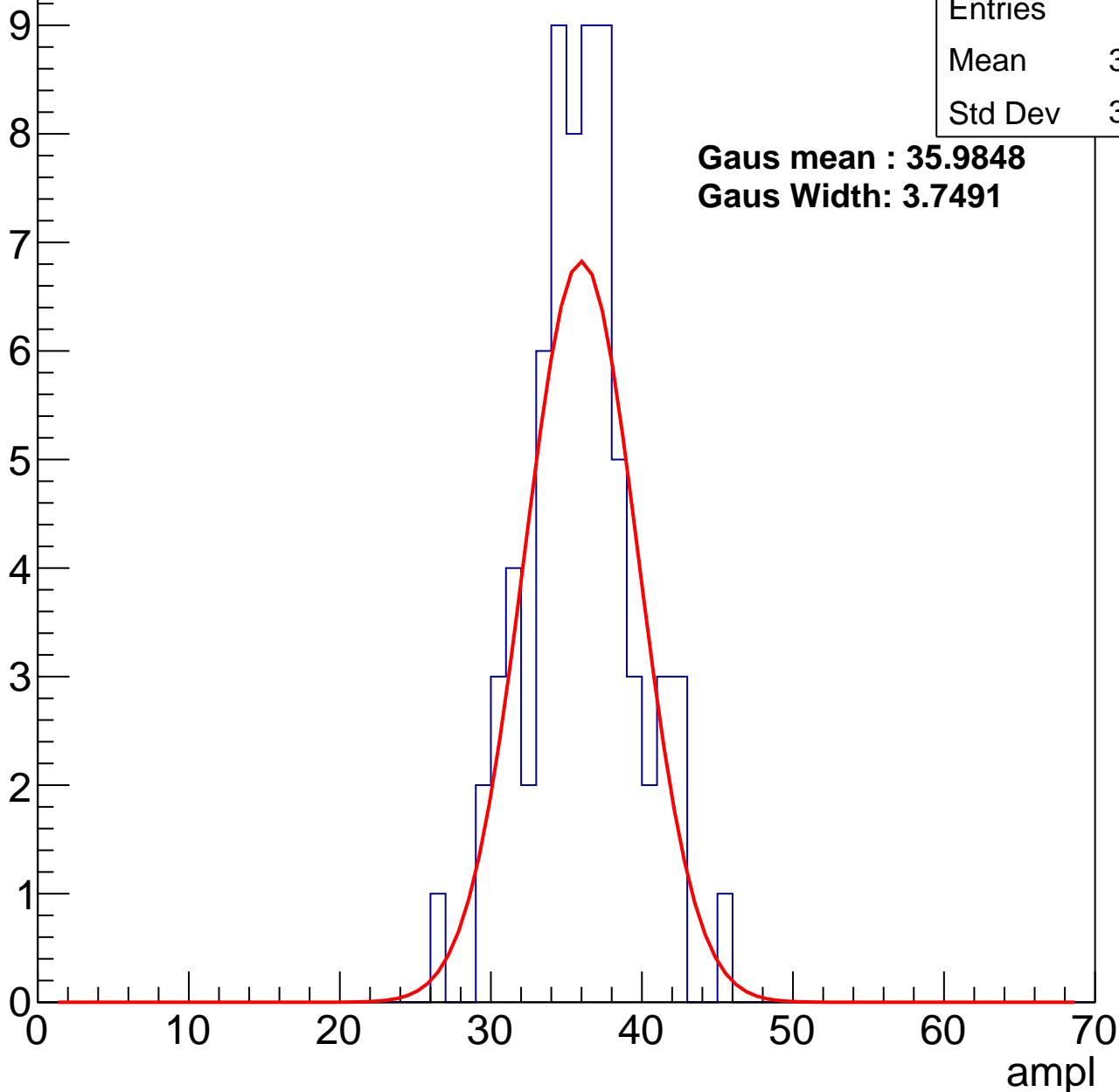
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	35.49
Std Dev	3.524

**Gaus mean : 35.9848**

**Gaus Width: 3.7491**



# B1L103S, U26-ch49, adc2

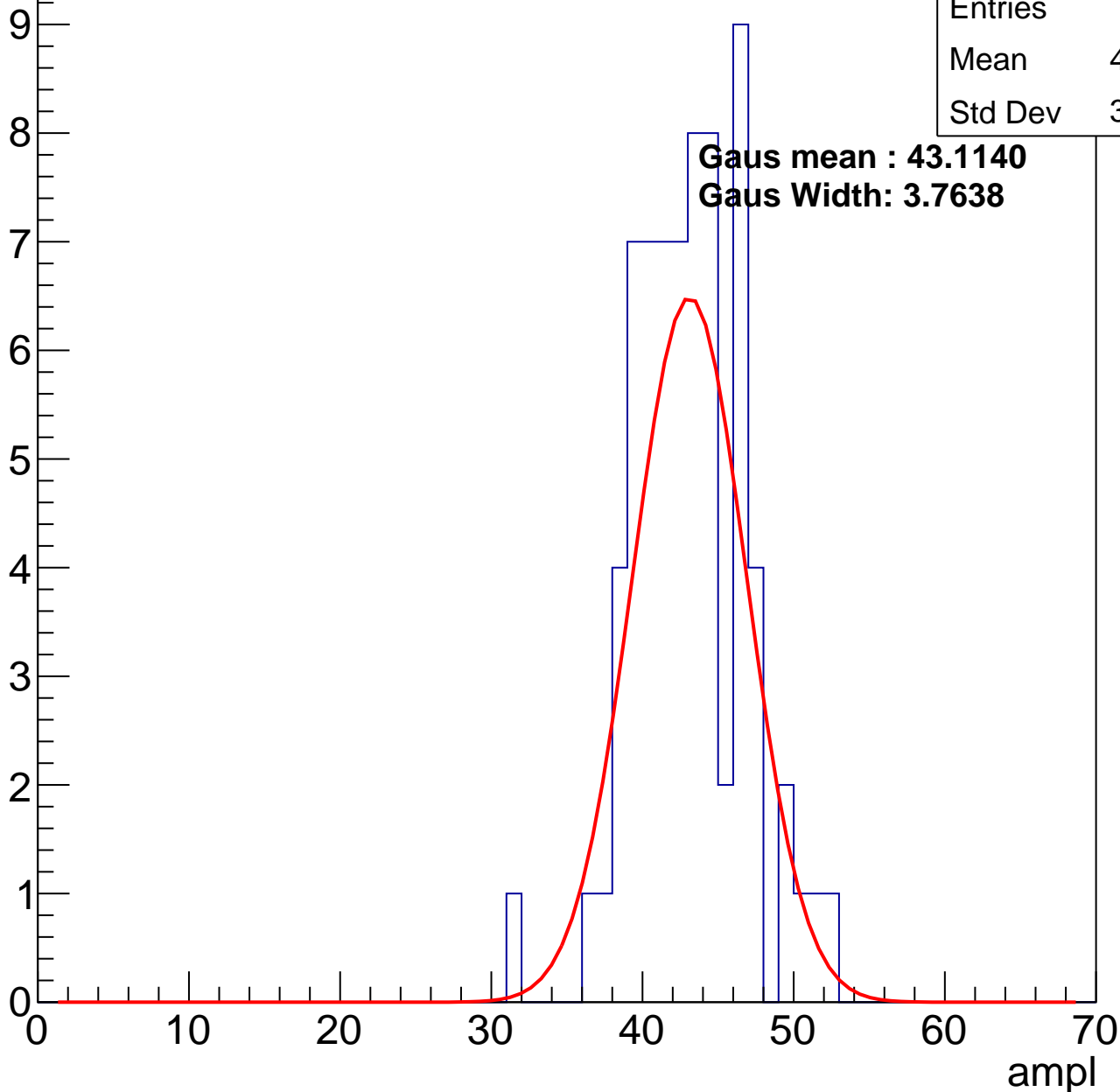
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	42.66
Std Dev	3.673

**Gaus mean : 43.1140**

**Gaus Width: 3.7638**

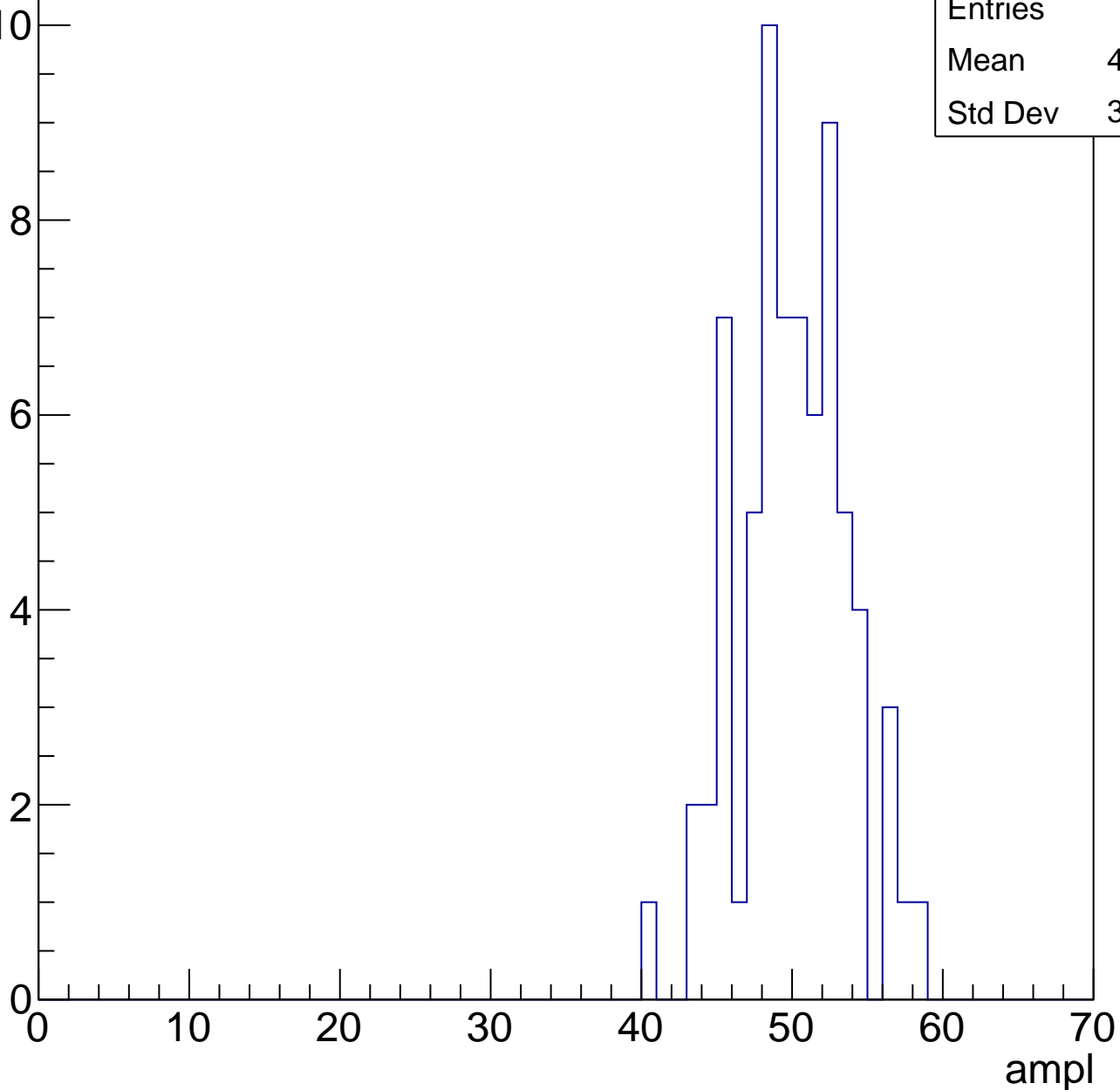


# B1L103S, U26-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	49.59
Std Dev	3.586

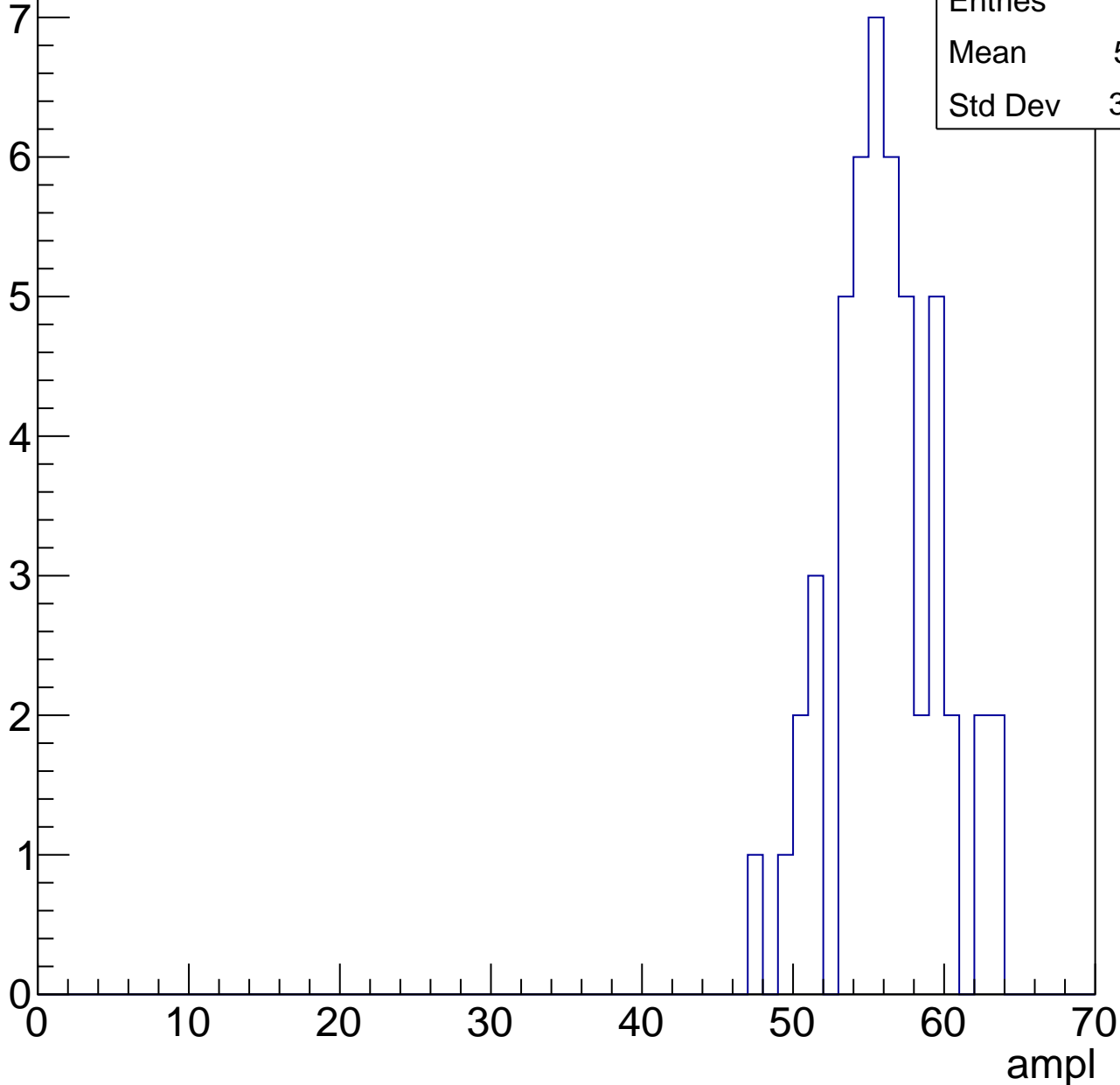


# B1L103S, U26-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	55.61
Std Dev	3.516

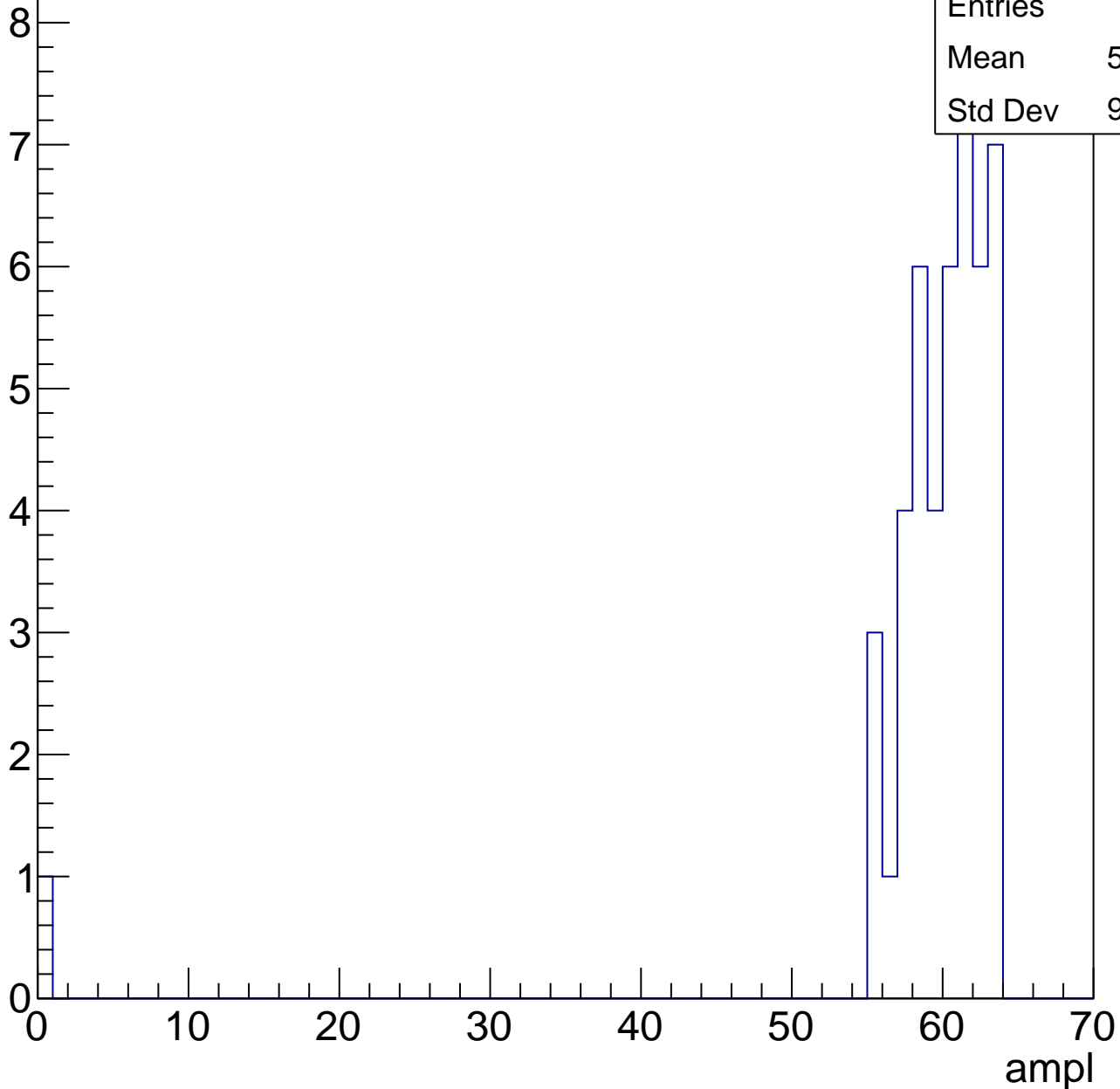


# B1L103S, U26-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	58.57
Std Dev	9.035



# B1L103S, U26-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

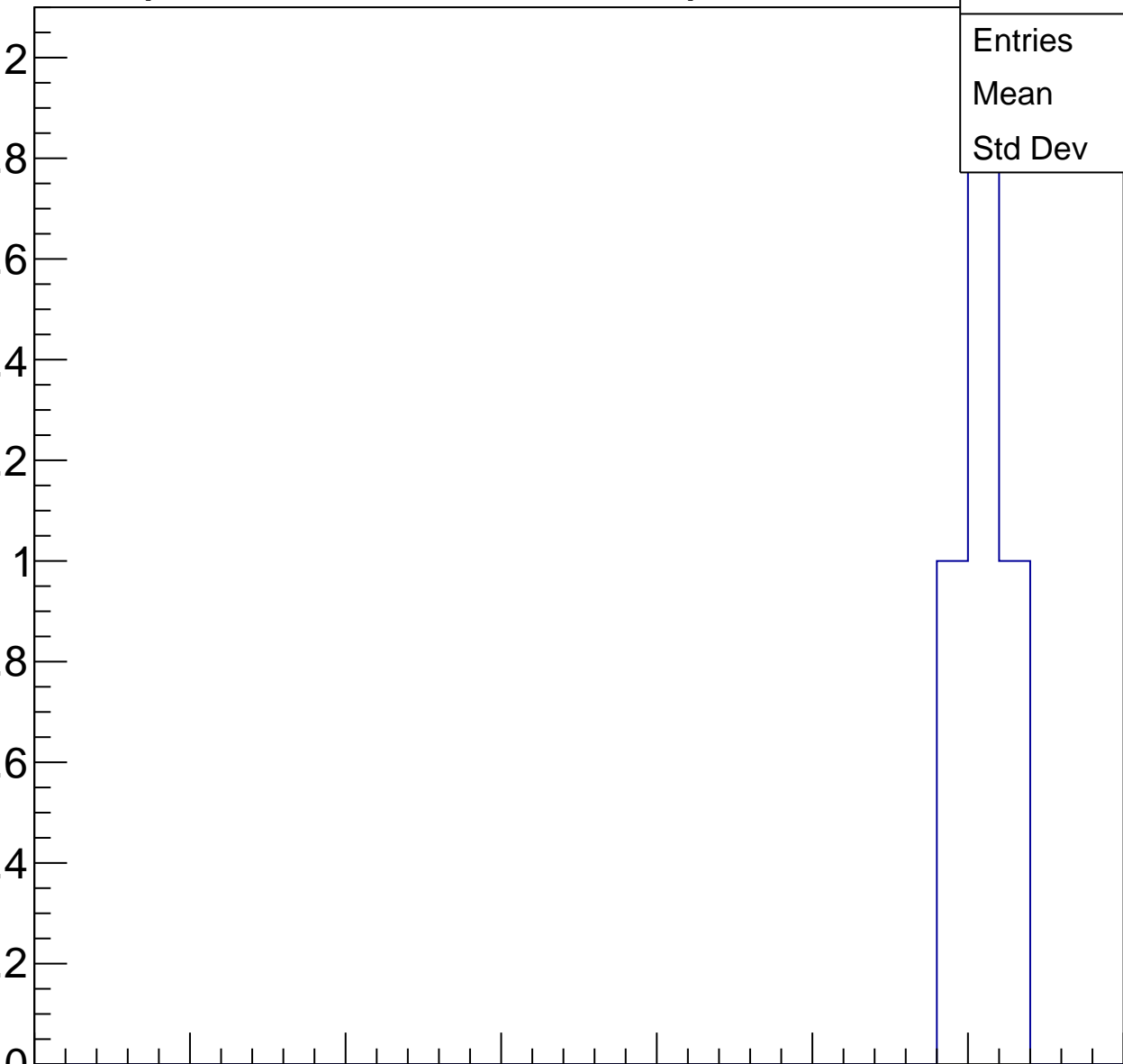
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	8
Mean	60.5
Std Dev	1.5

0 10 20 30 40 50 60 70

ampl





# B1L103S, U26-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch50, adc0

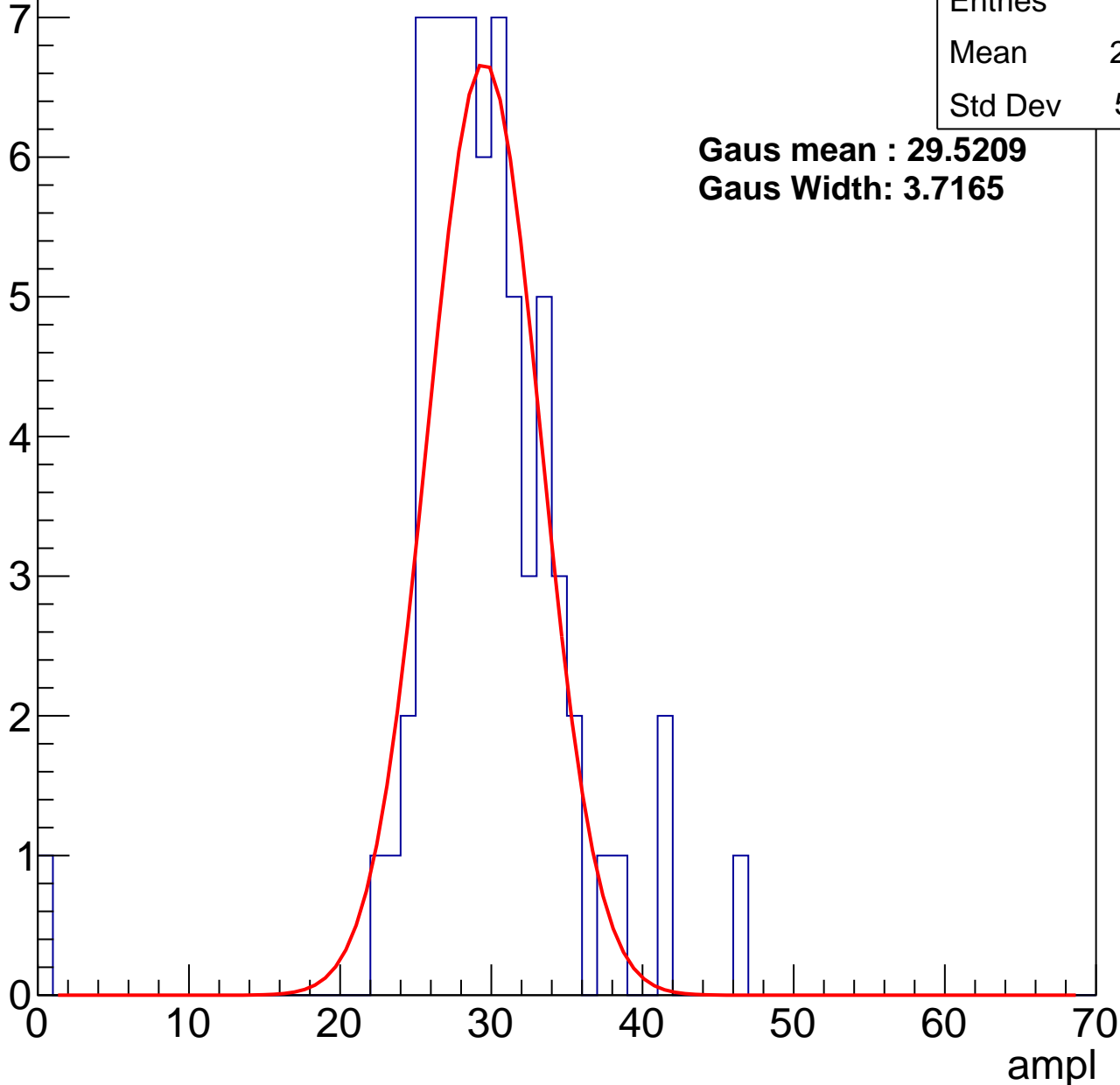
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	29.13
Std Dev	5.631

**Gaus mean : 29.5209**

**Gaus Width: 3.7165**



# B1L103S, U26-ch50, adc1

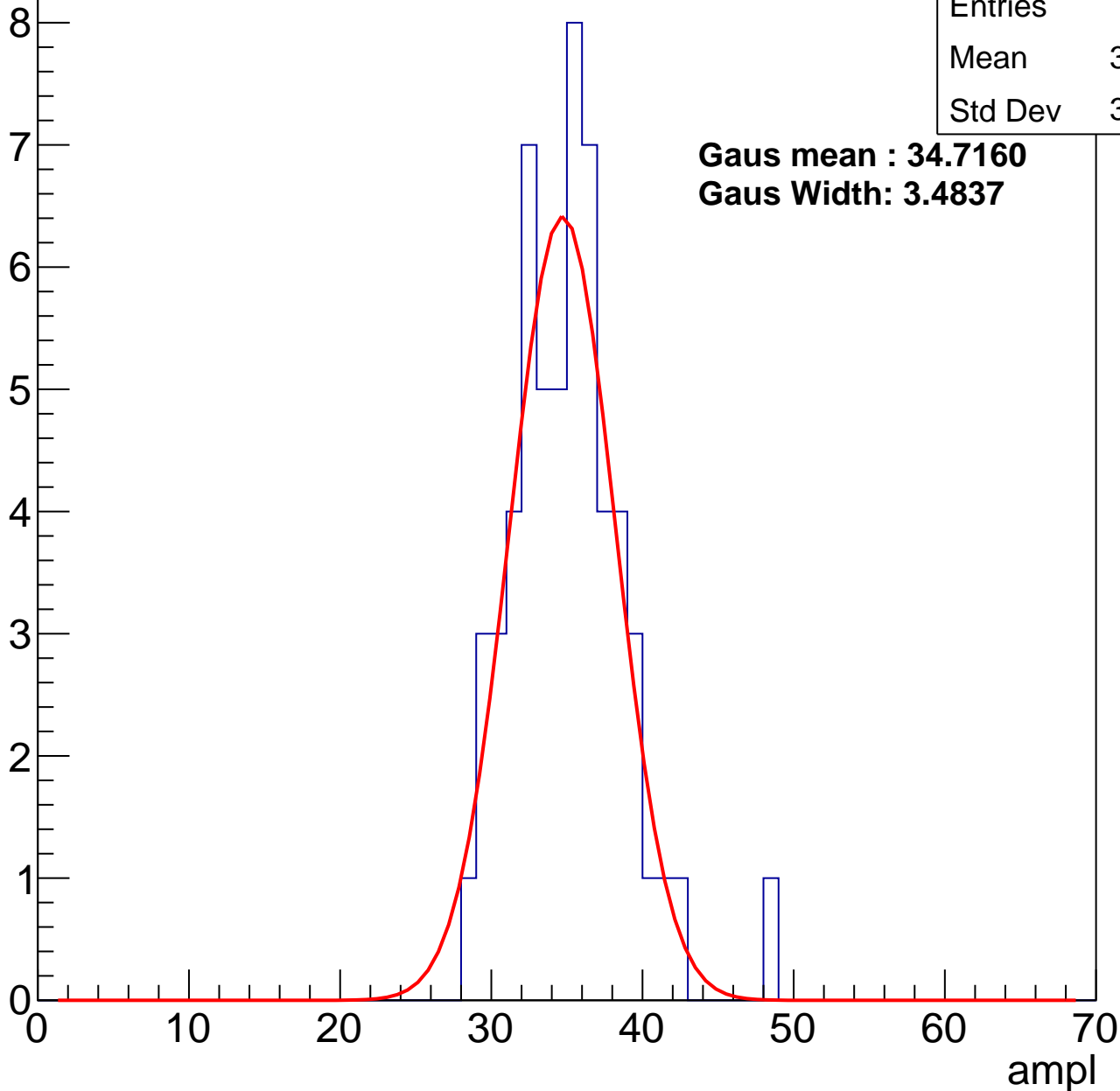
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	34.62
Std Dev	3.624

**Gaus mean : 34.7160**

**Gaus Width: 3.4837**



# B1L103S, U26-ch50, adc2

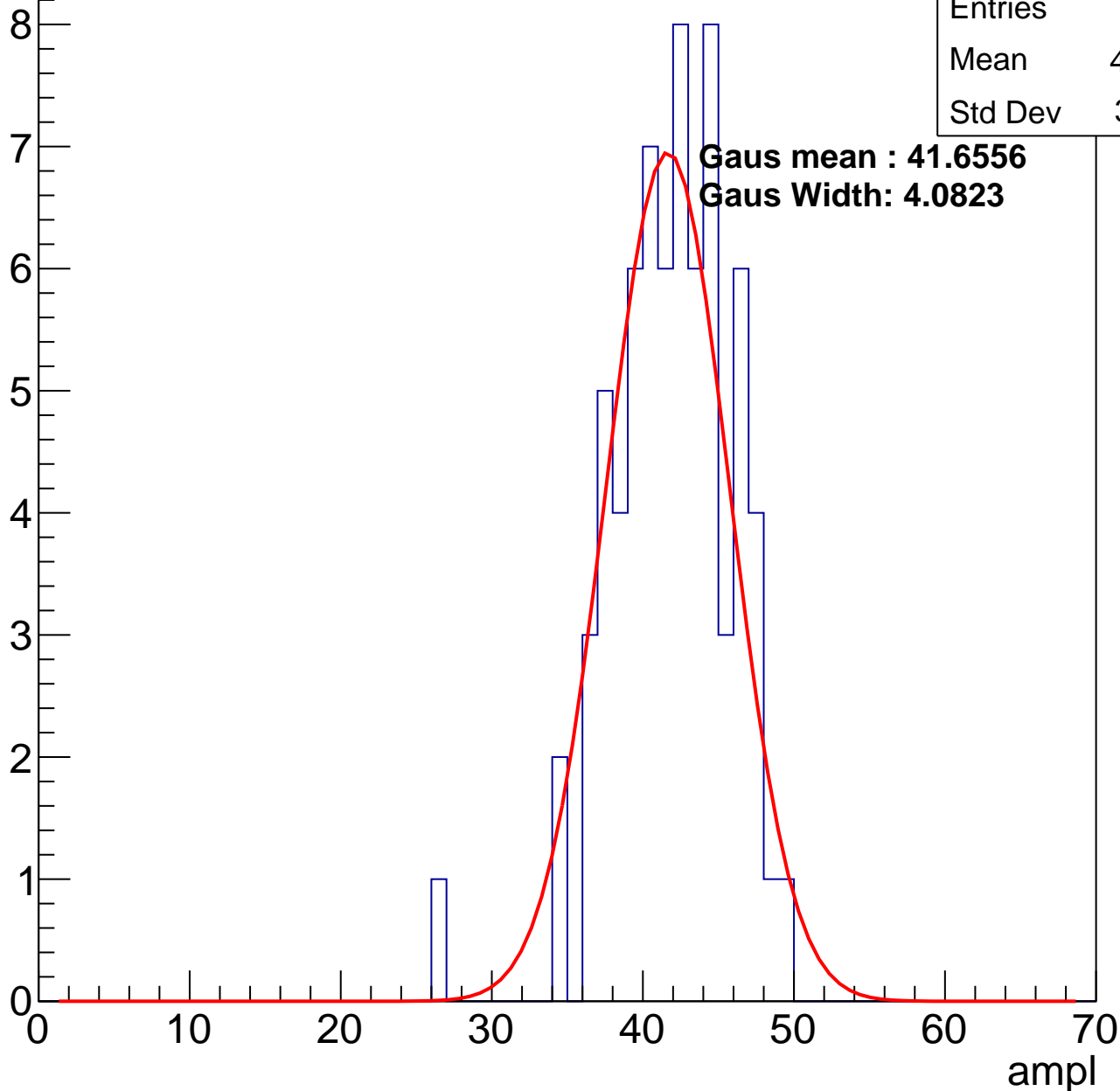
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	41.42
Std Dev	3.921

**Gaus mean : 41.6556**

**Gaus Width: 4.0823**

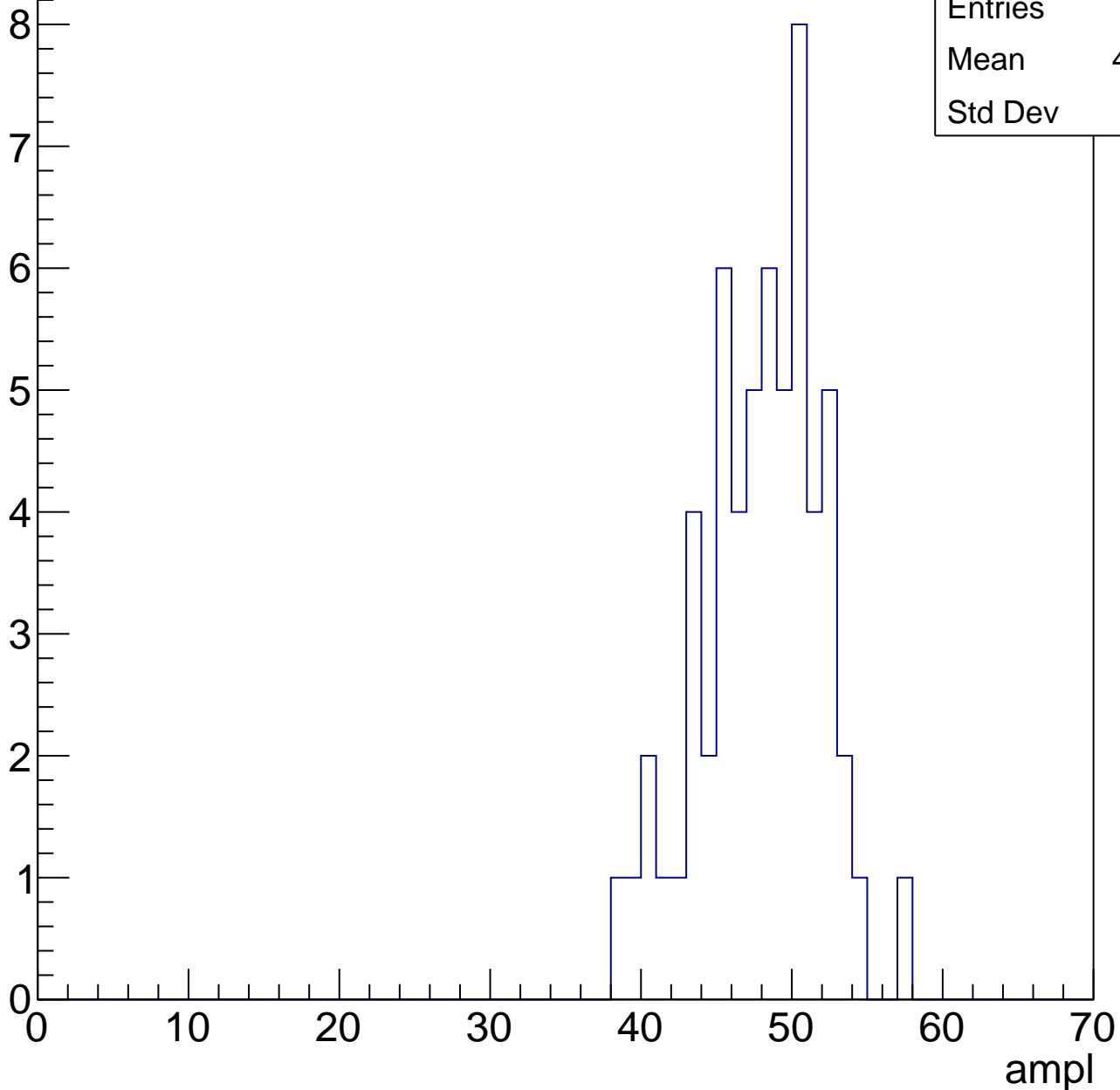


# B1L103S, U26-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

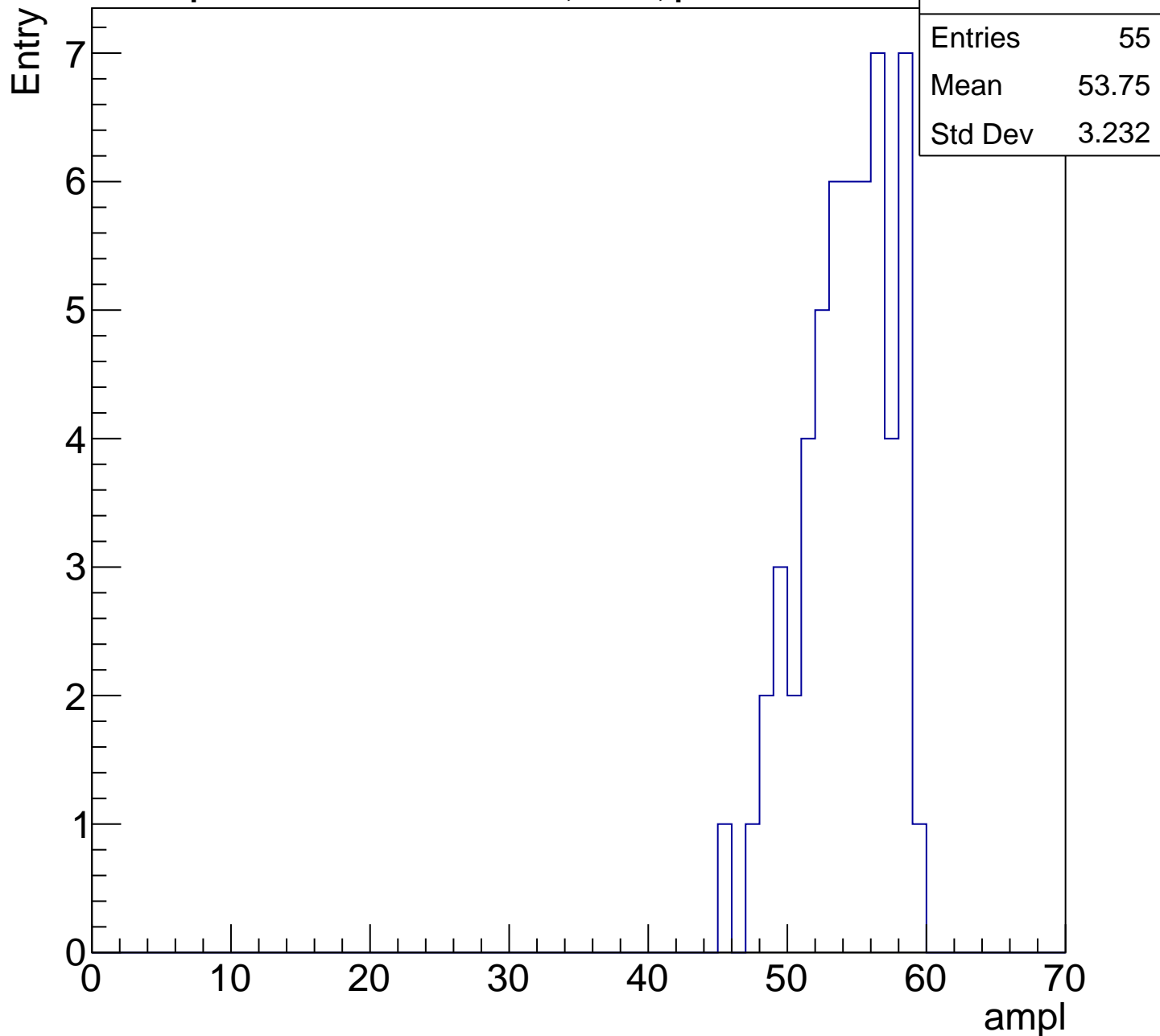
Entry

Entries	59
Mean	47.51
Std Dev	3.92



# B1L103S, U26-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U26-ch50, adc5

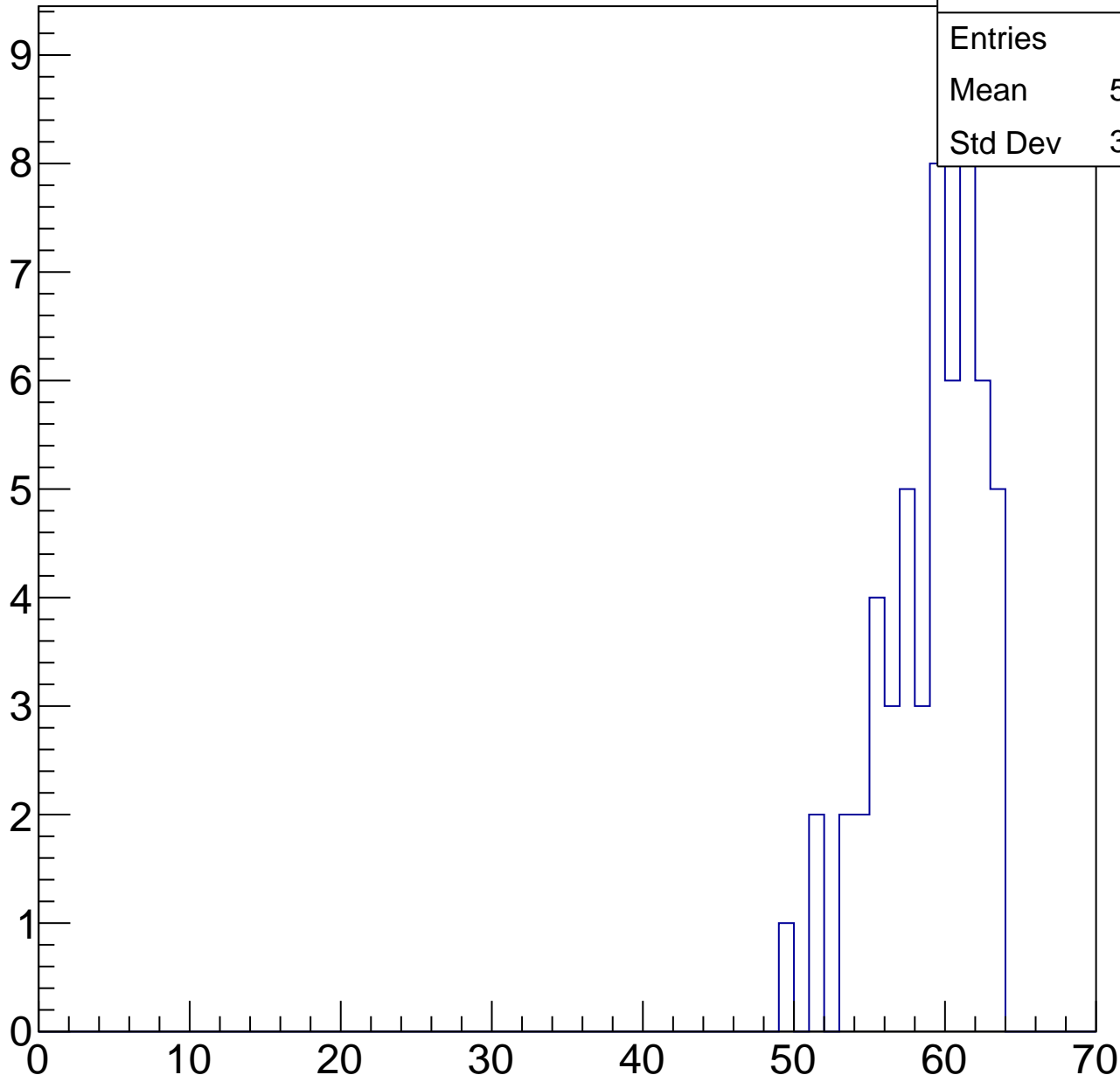
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	56
Mean	58.57
Std Dev	3.353

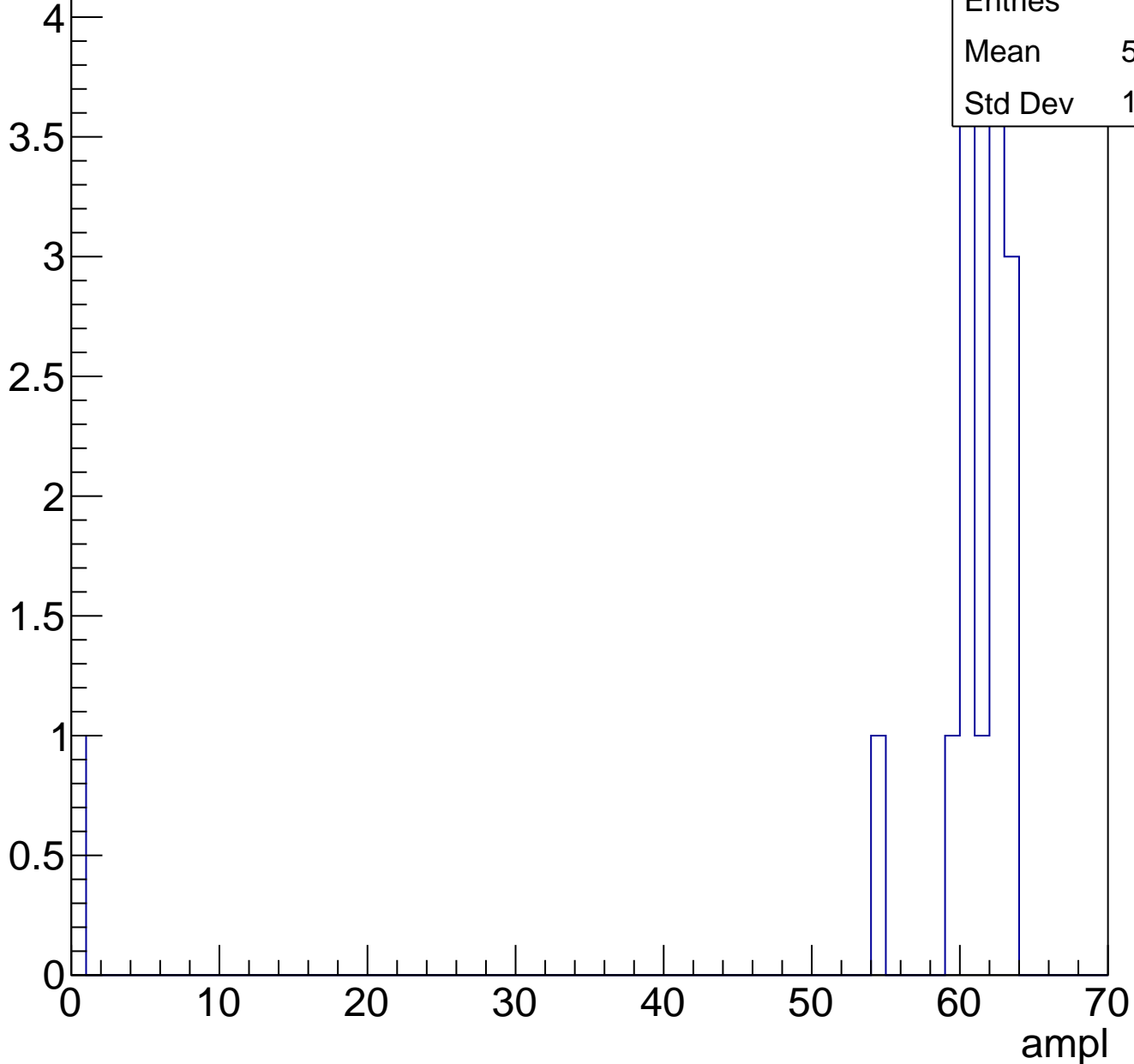
ampl



# B1L103S, U26-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

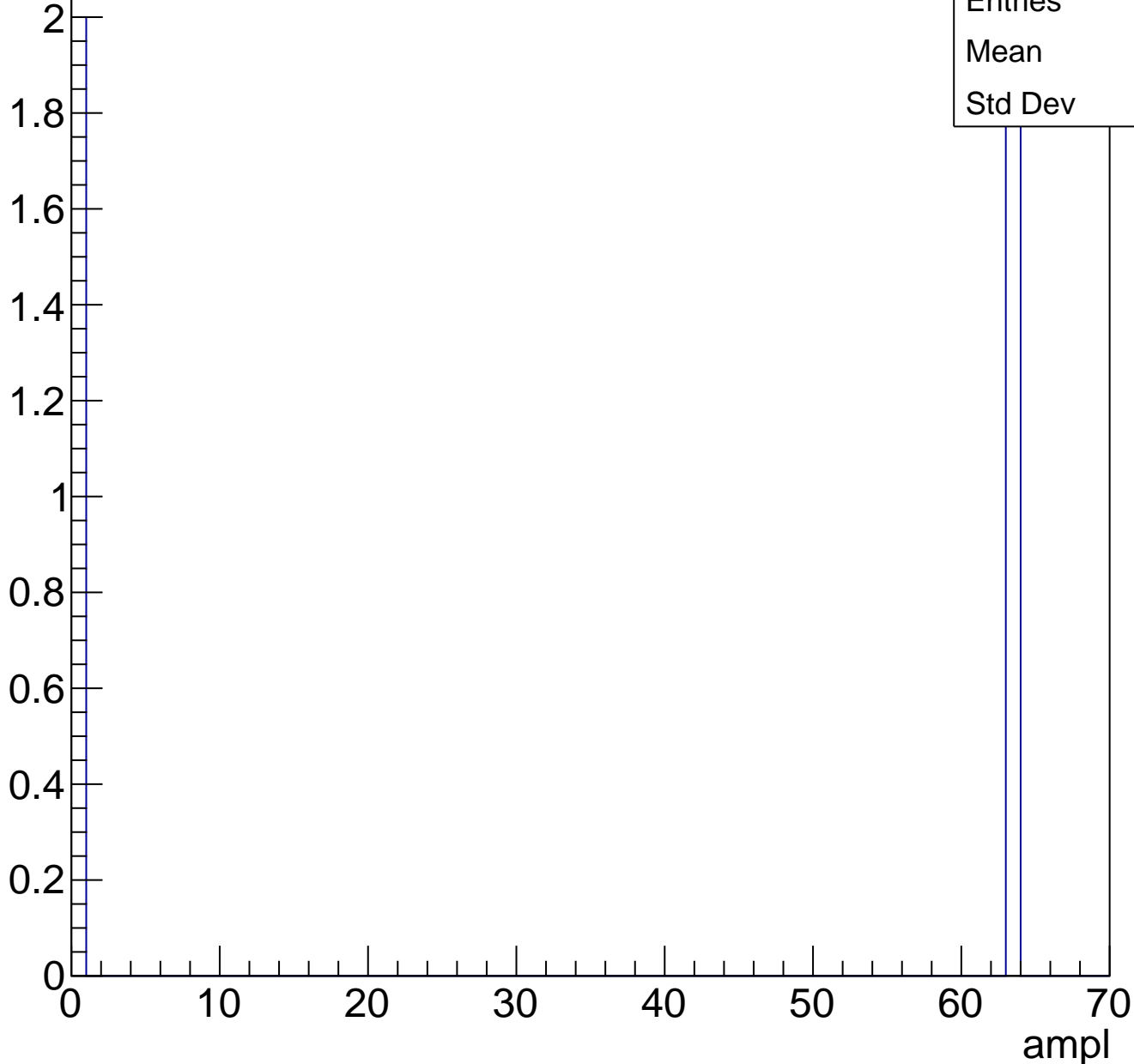




# B1L103S, U26-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch51, adc0

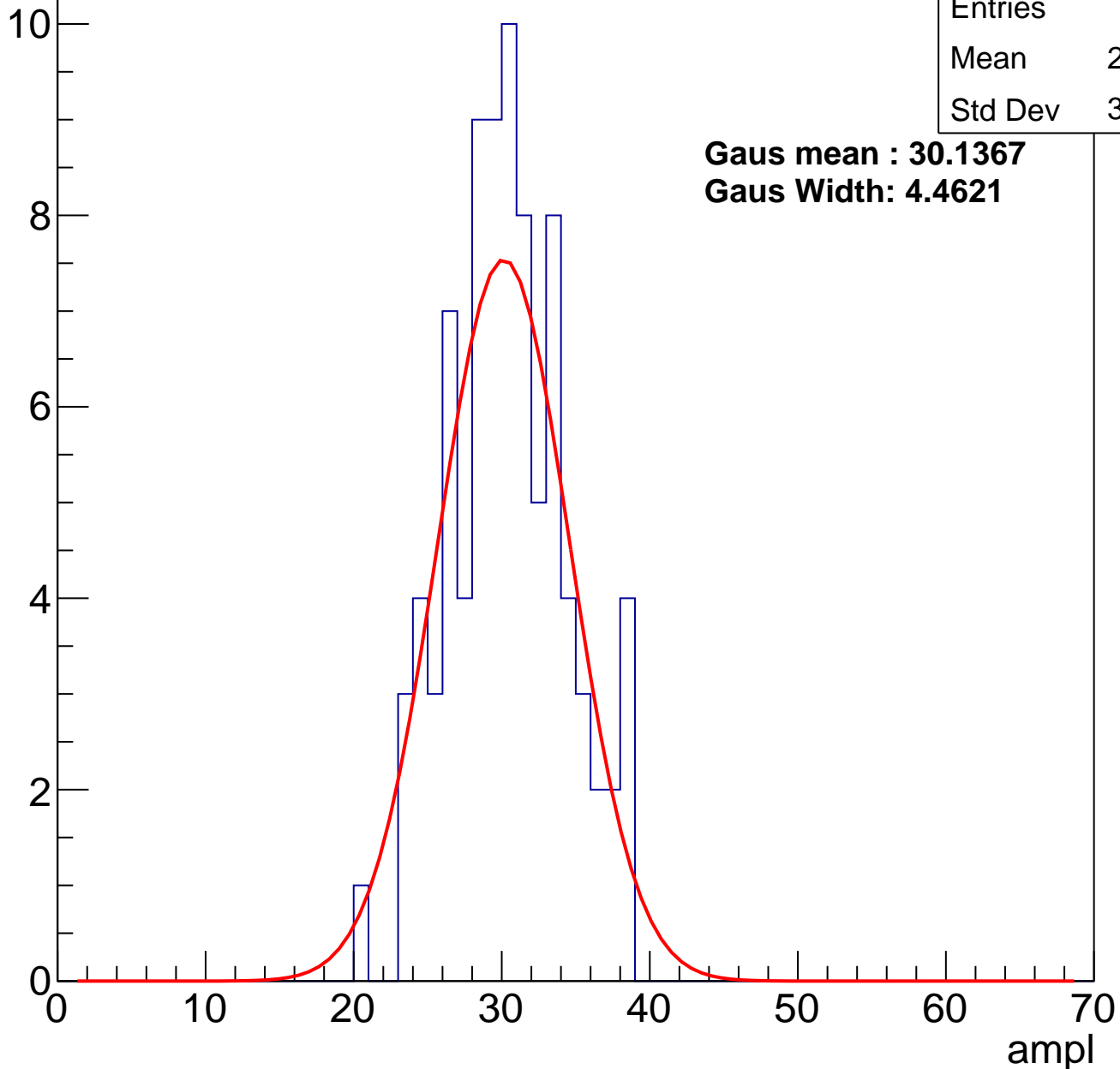
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	86
Mean	29.93
Std Dev	3.923

**Gaus mean : 30.1367**

**Gaus Width: 4.4621**

Entry



# B1L103S, U26-ch51, adc1

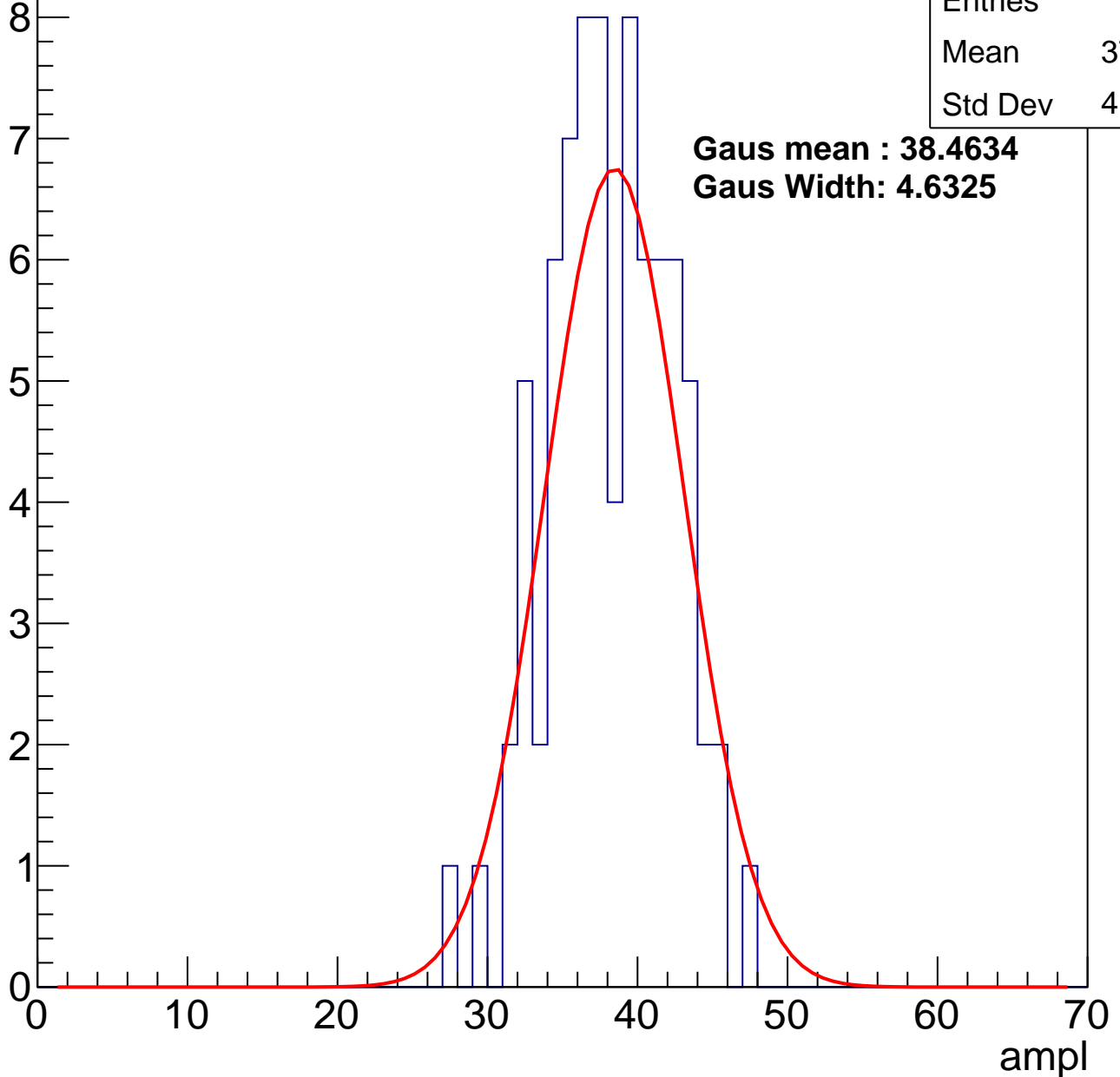
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	37.74
Std Dev	4.002

**Gaus mean : 38.4634**

**Gaus Width: 4.6325**



# B1L103S, U26-ch51, adc2

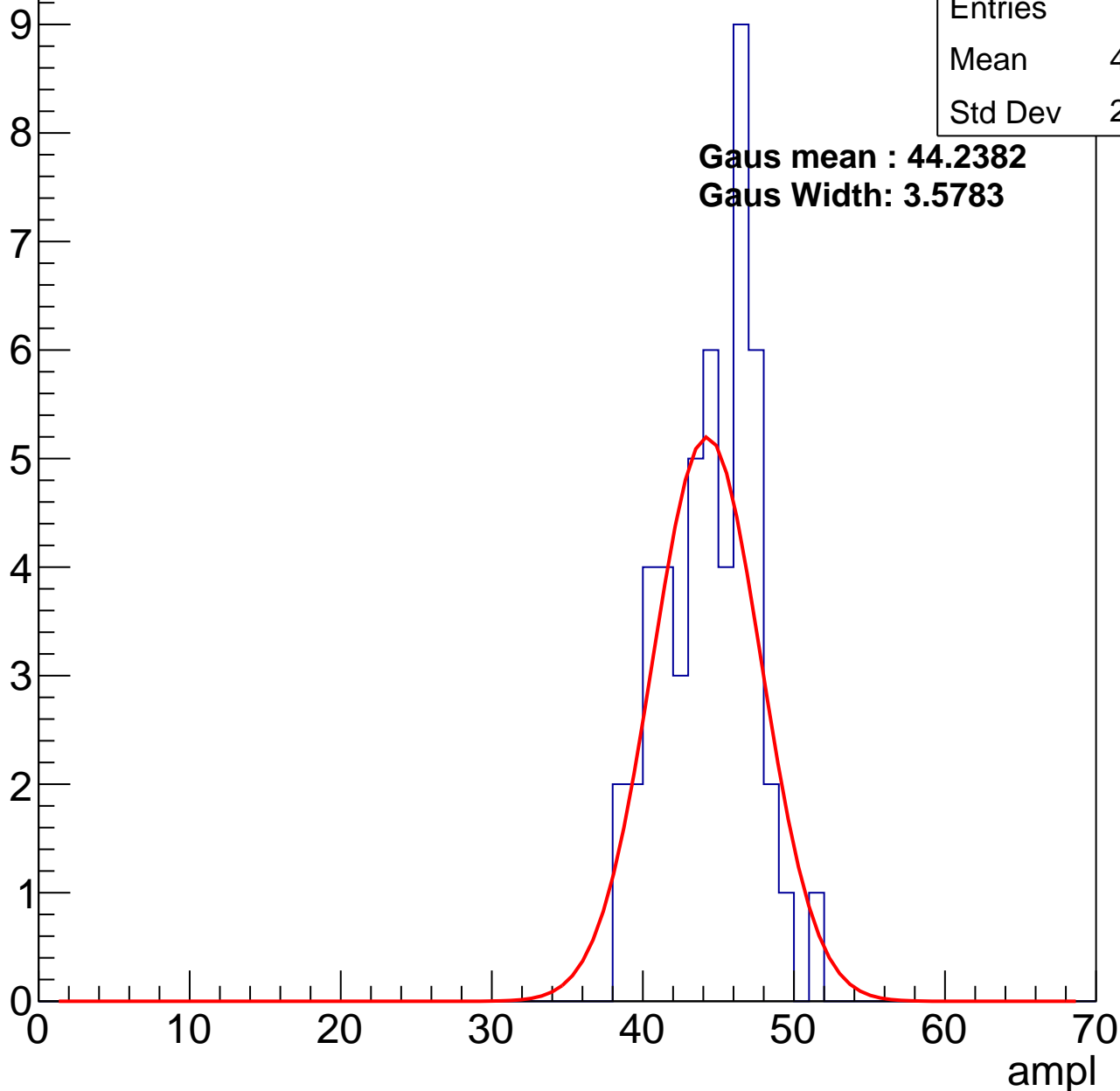
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	43.98
Std Dev	2.993

**Gaus mean : 44.2382**

**Gaus Width: 3.5783**

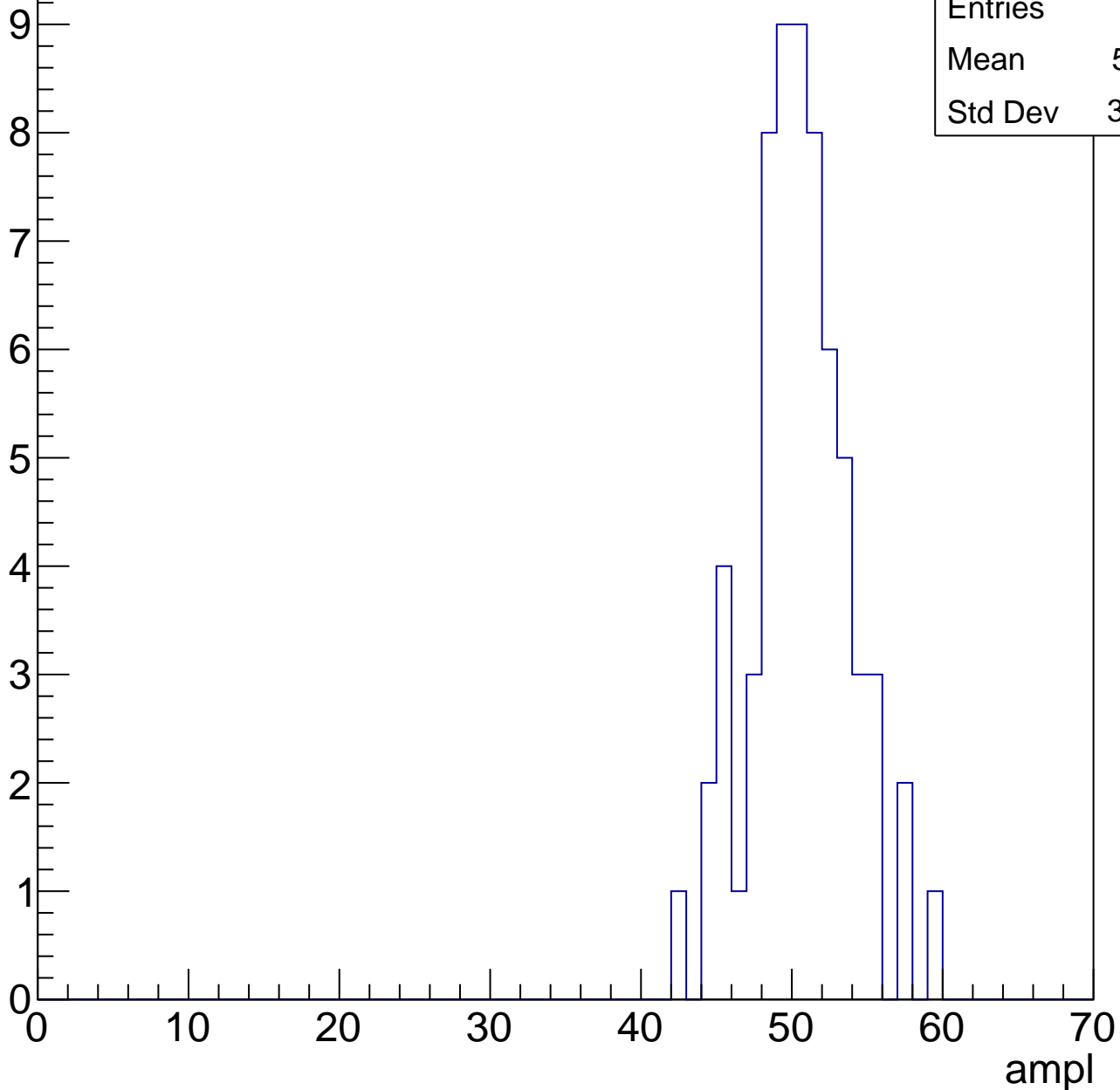


# B1L103S, U26-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	50.11
Std Dev	3.278

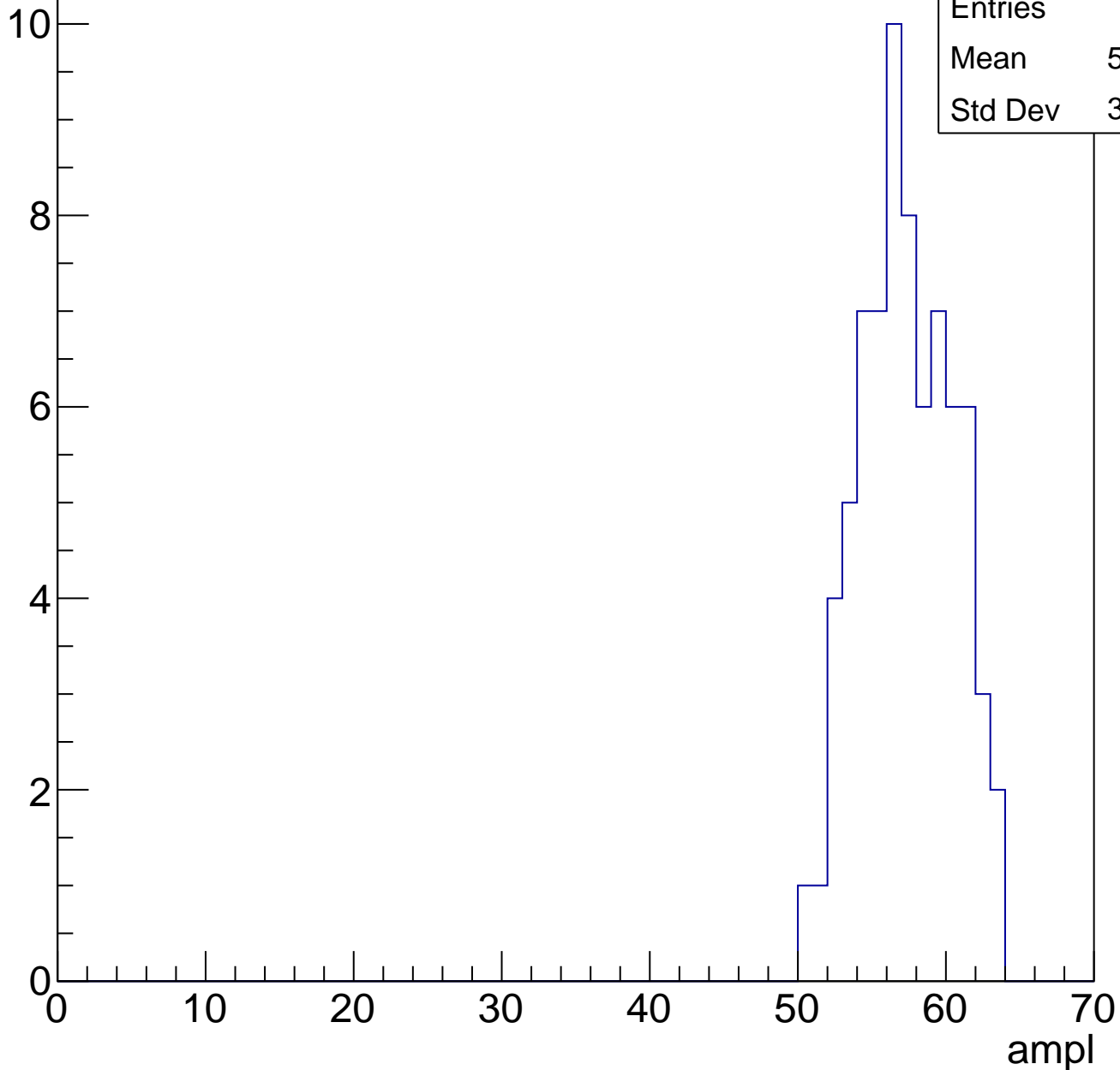


# B1L103S, U26-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	73
Mean	56.88
Std Dev	3.088

Entry

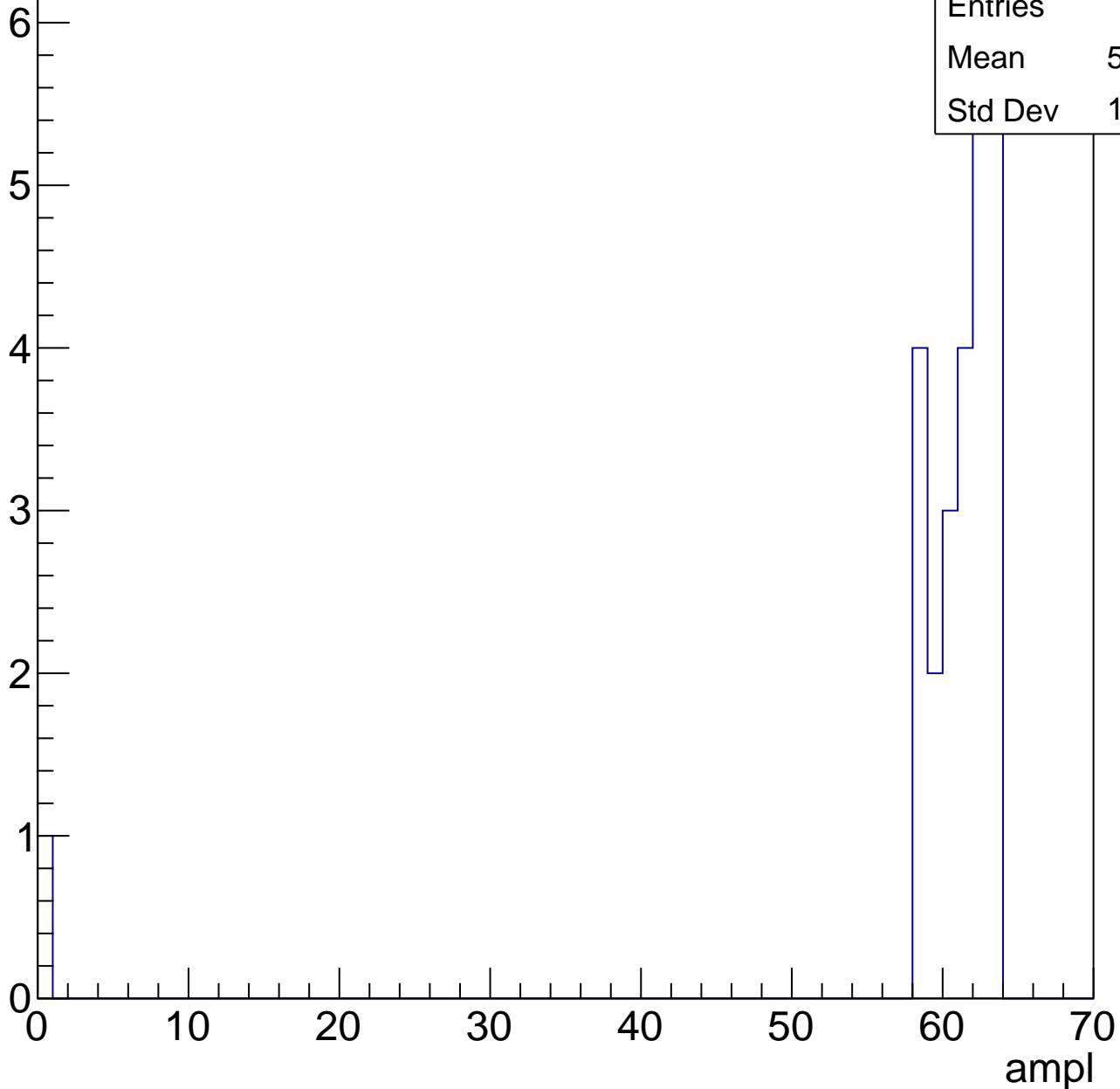


# B1L103S, U26-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	26
Mean	58.62
Std Dev	11.85



# B1L103S, U26-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	4
Mean	62
Std Dev	1.225



# B1L103S, U26-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U26-ch52, adc0

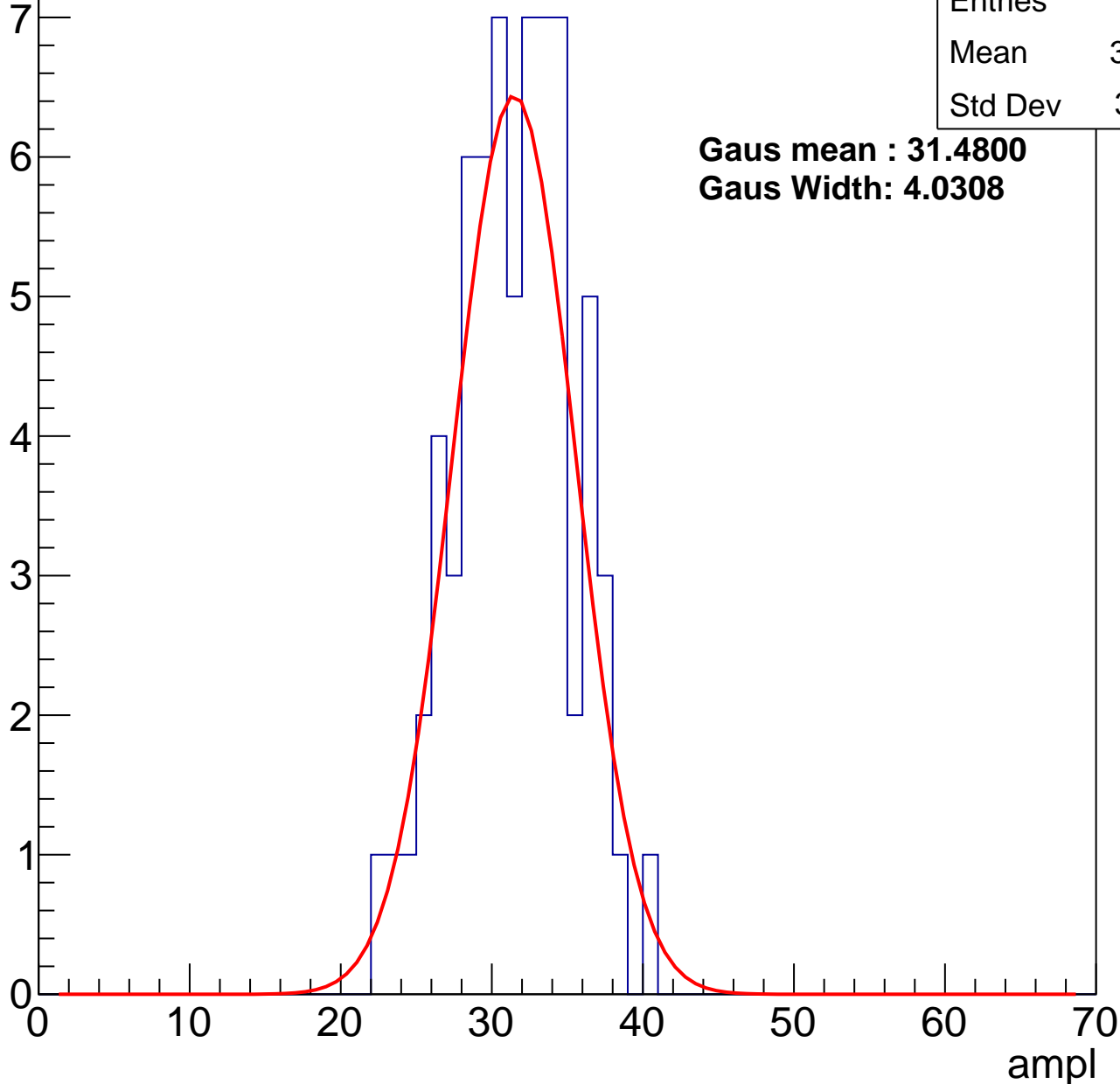
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	31.06
Std Dev	3.791

**Gaus mean : 31.4800**

**Gaus Width: 4.0308**



# B1L103S, U26-ch52, adc1

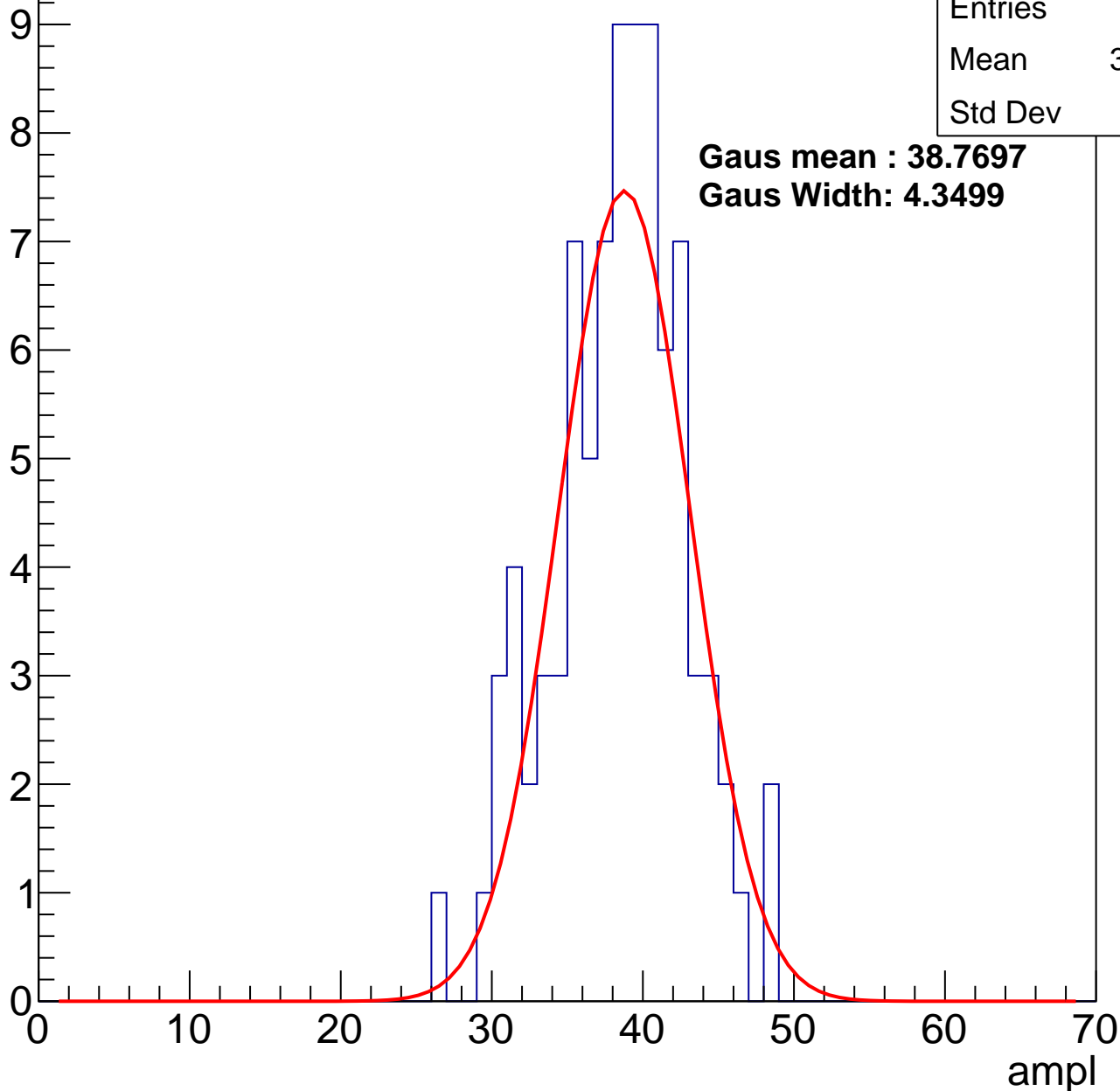
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	87
Mean	37.98
Std Dev	4.36

**Gaus mean : 38.7697**

**Gaus Width: 4.3499**



# B1L103S, U26-ch52, adc2

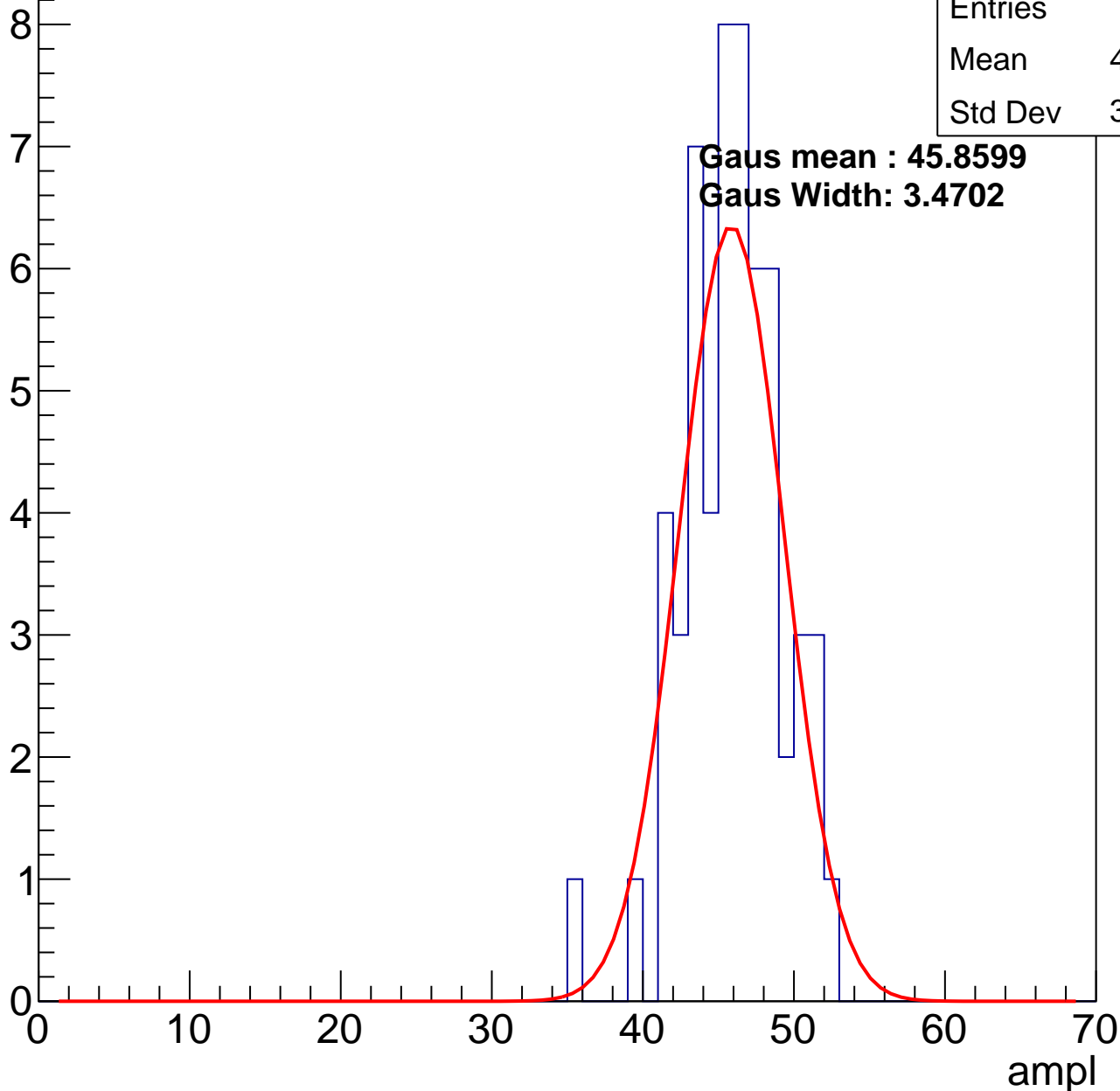
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	45.47
Std Dev	3.234

**Gaus mean : 45.8599**

**Gaus Width: 3.4702**

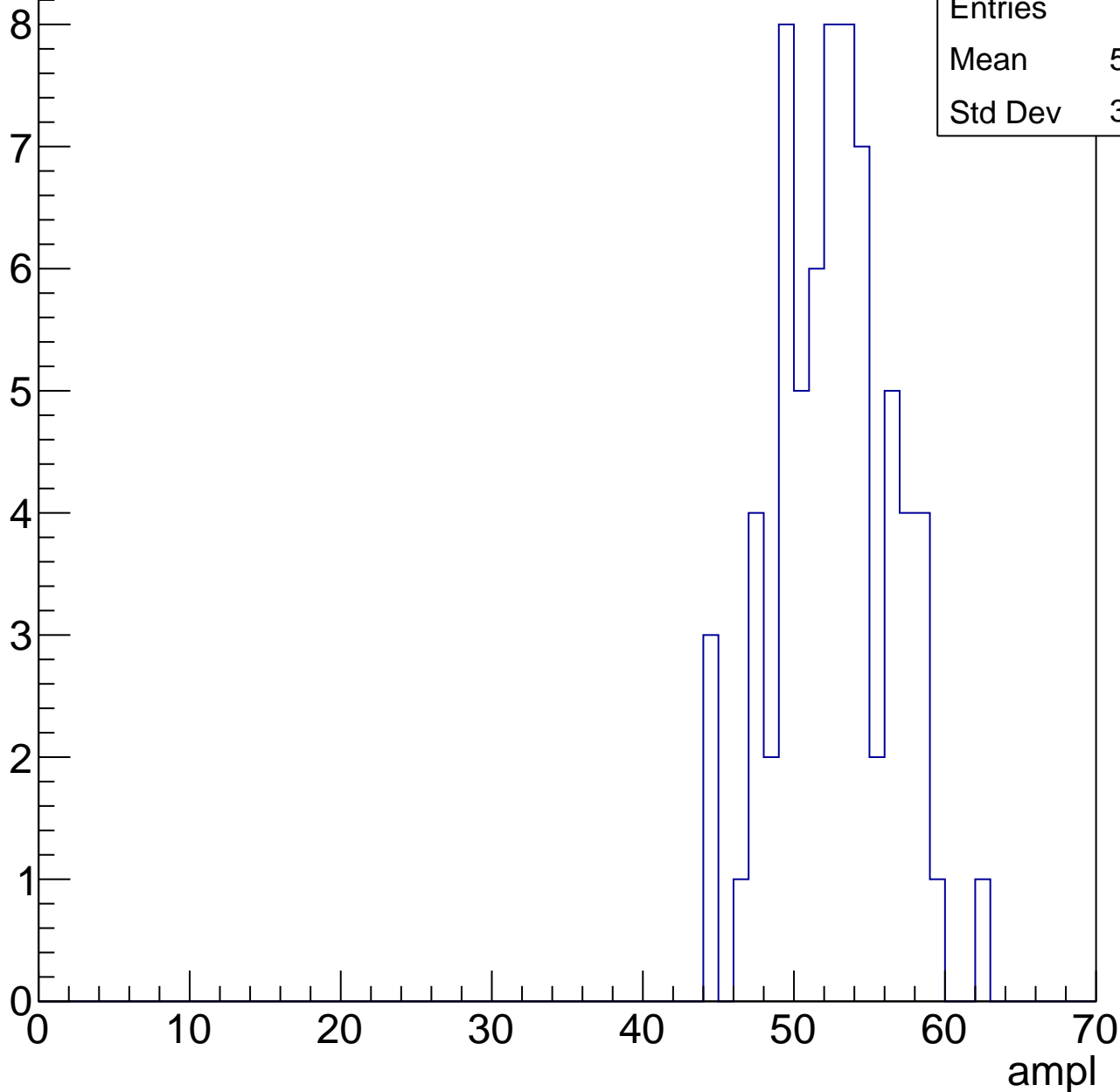


# B1L103S, U26-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

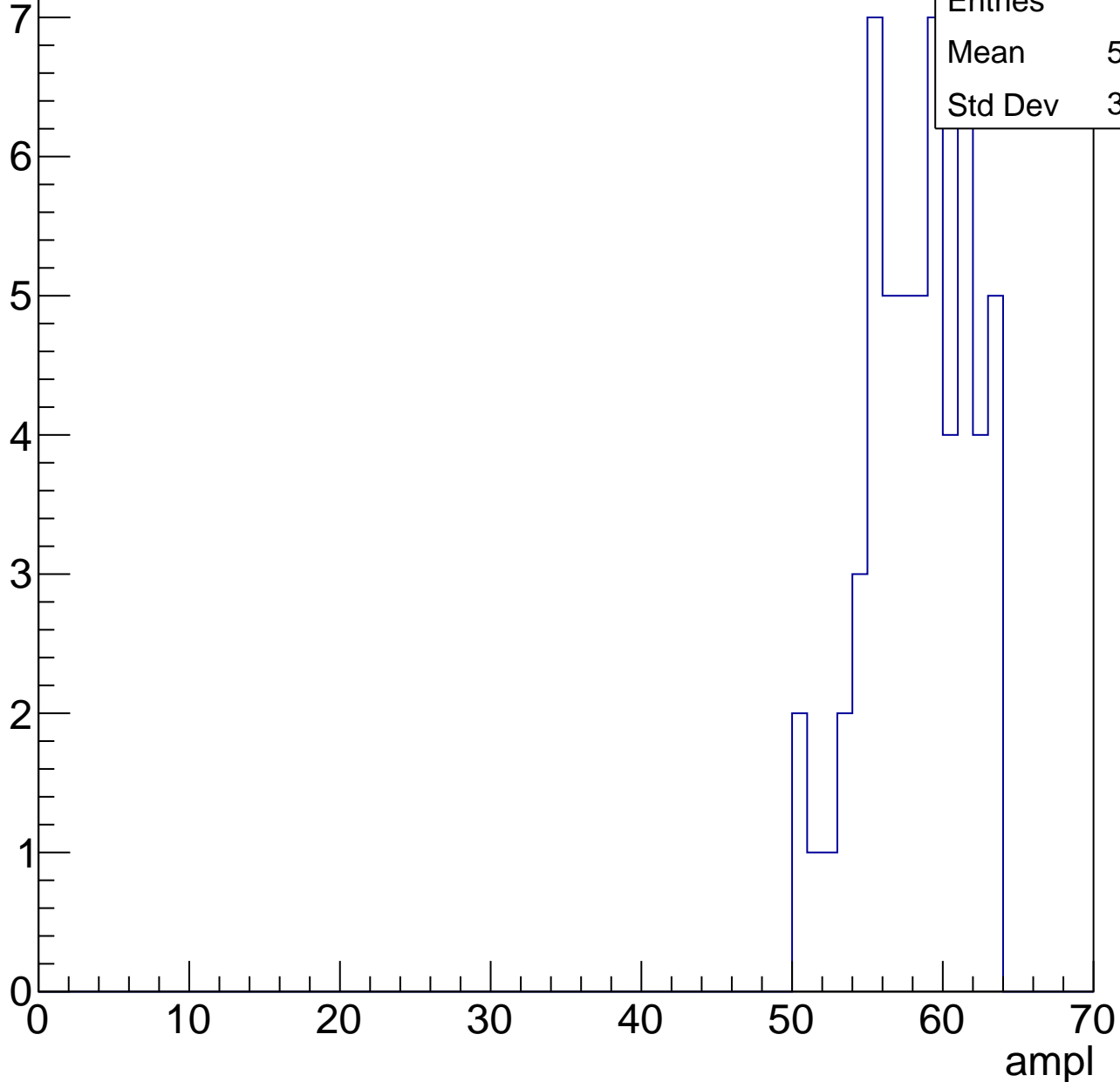
Entries	69
Mean	52.16
Std Dev	3.775



# B1L103S, U26-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

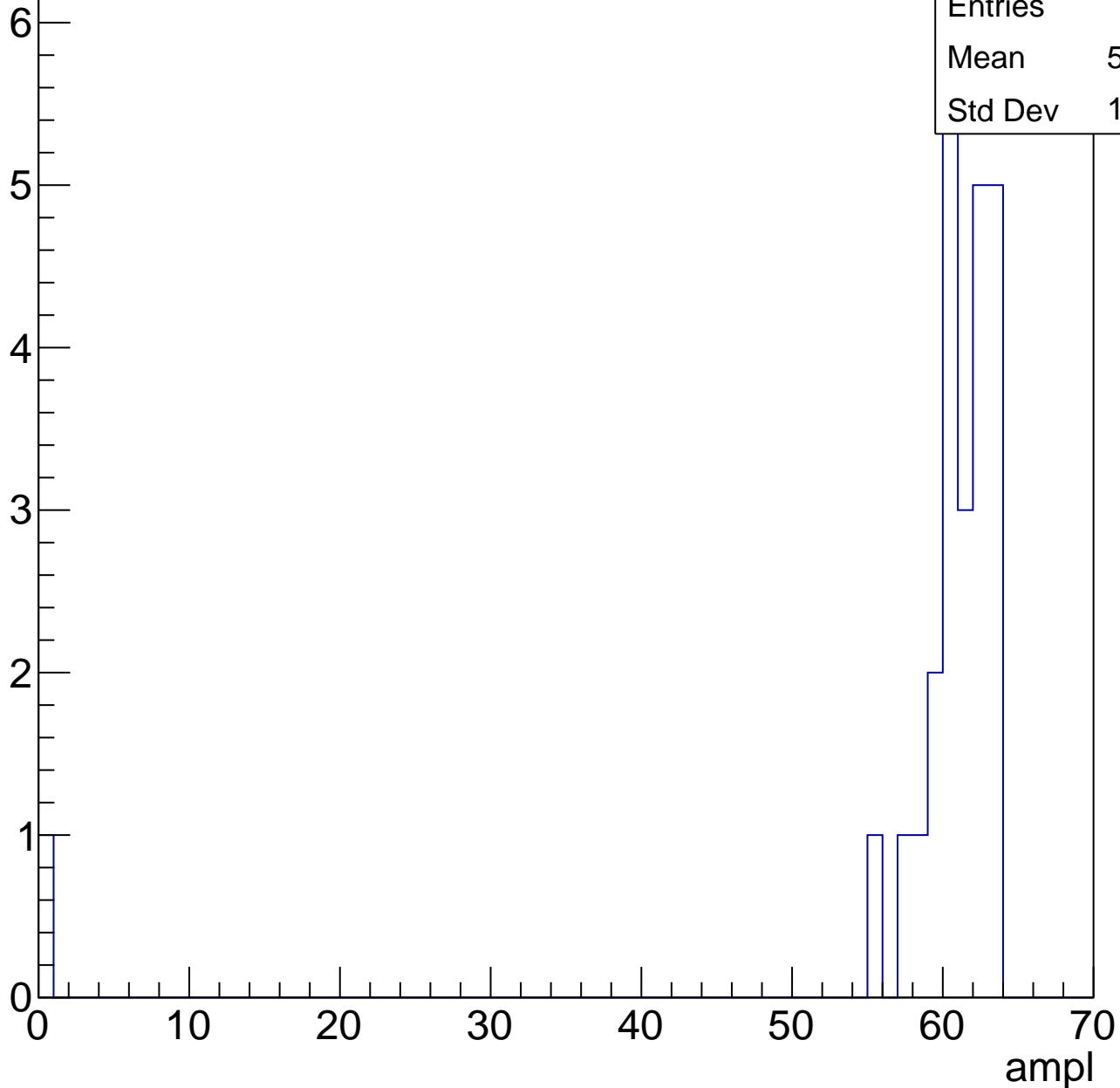


Entries	58
Mean	57.83
Std Dev	3.405

# B1L103S, U26-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L103S, U26-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch53, adc0

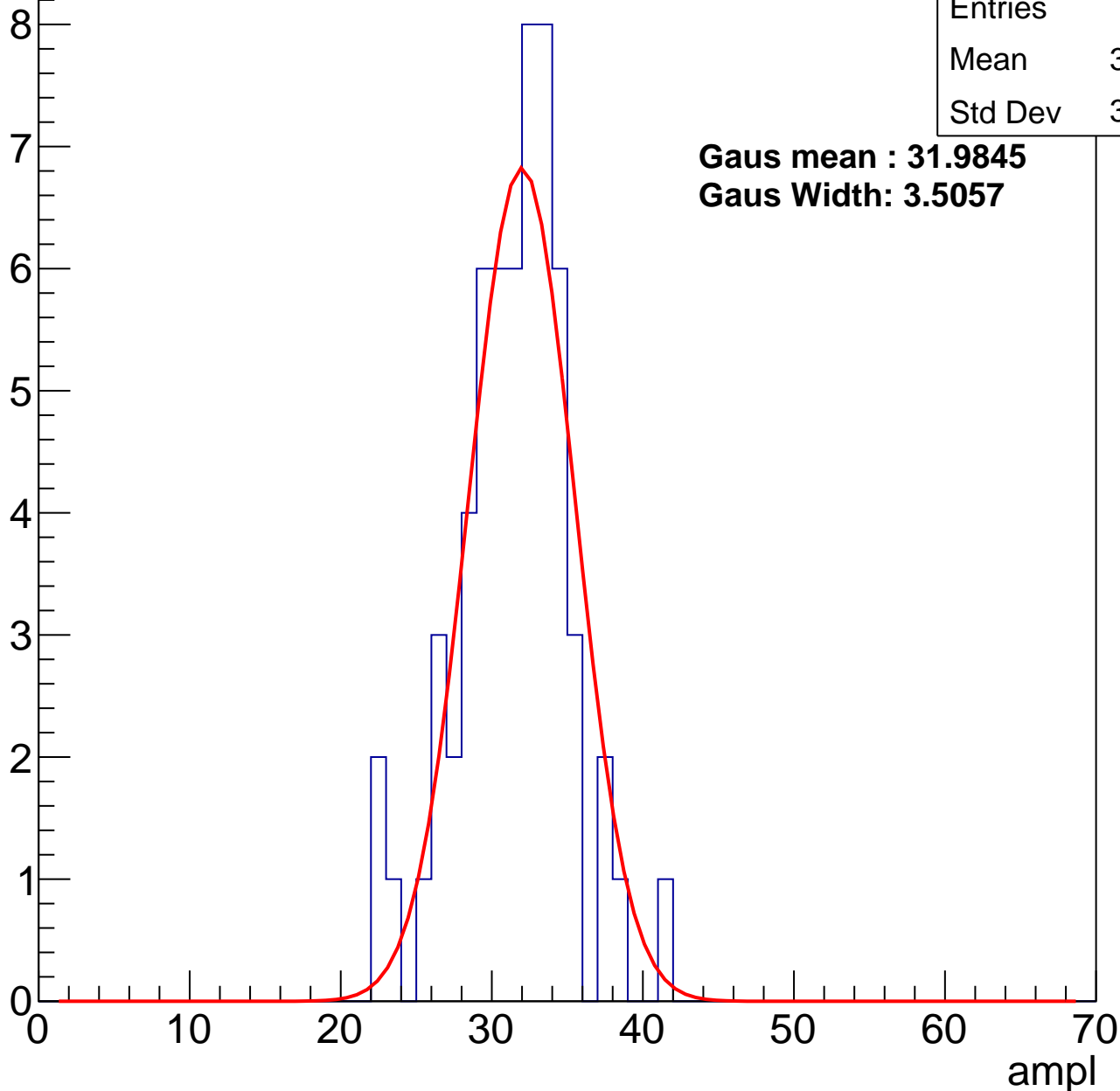
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	30.97
Std Dev	3.647

**Gaus mean : 31.9845**

**Gaus Width: 3.5057**



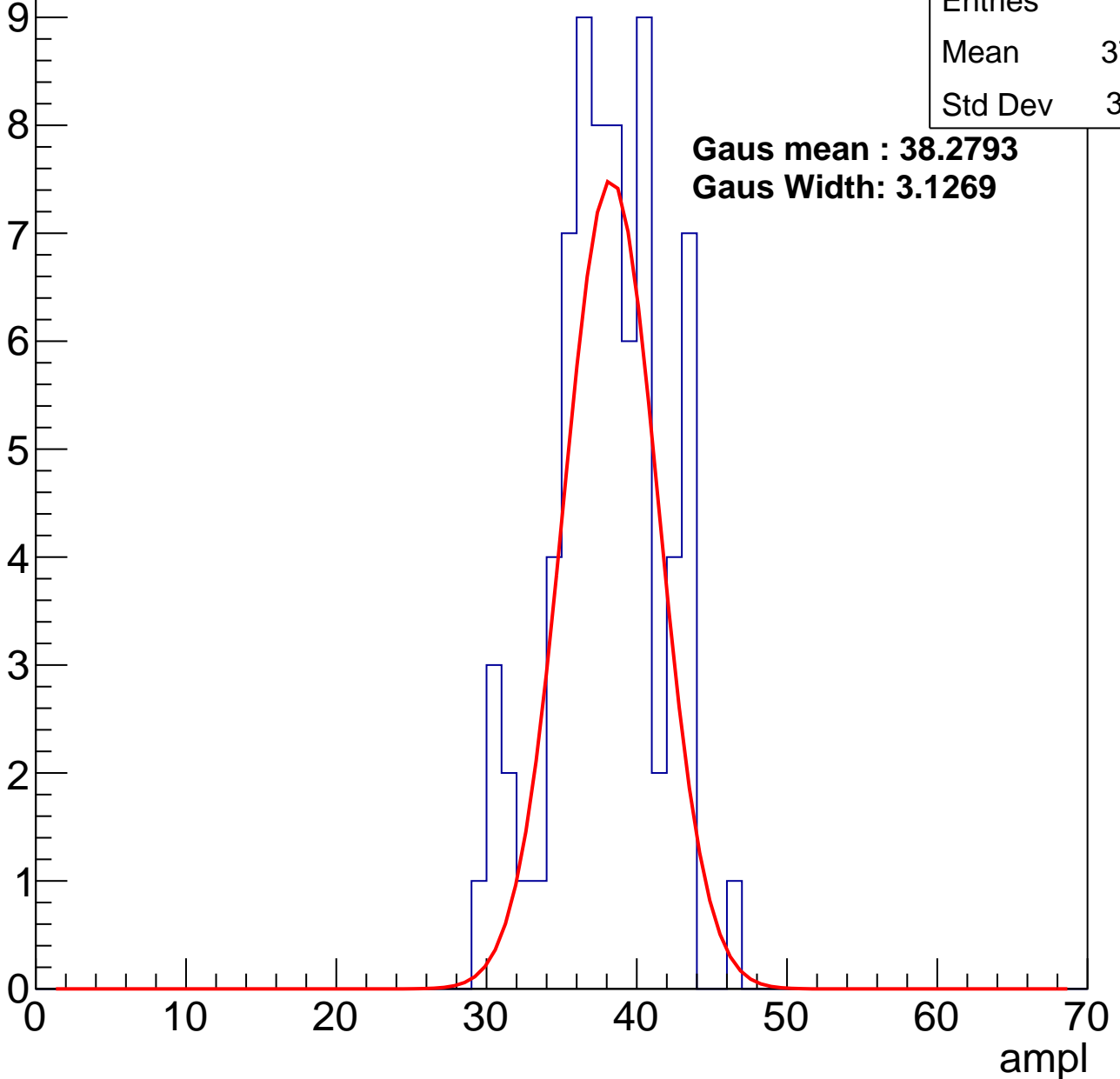
# B1L103S, U26-ch53, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	37.56
Std Dev	3.611

**Gaus mean : 38.2793**  
**Gaus Width: 3.1269**



# B1L103S, U26-ch53, adc2

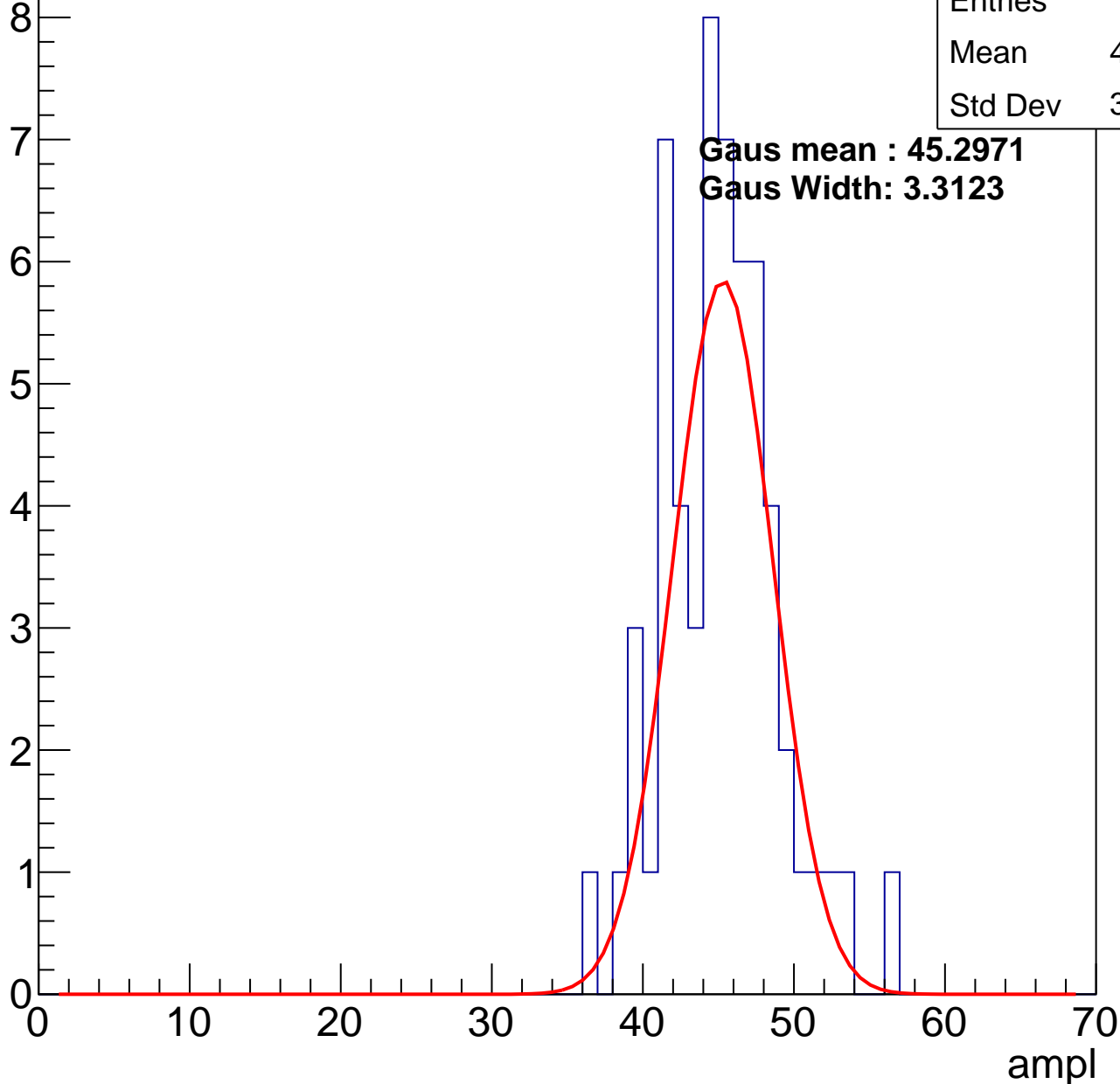
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	44.69
Std Dev	3.756

**Gaus mean : 45.2971**

**Gaus Width: 3.3123**

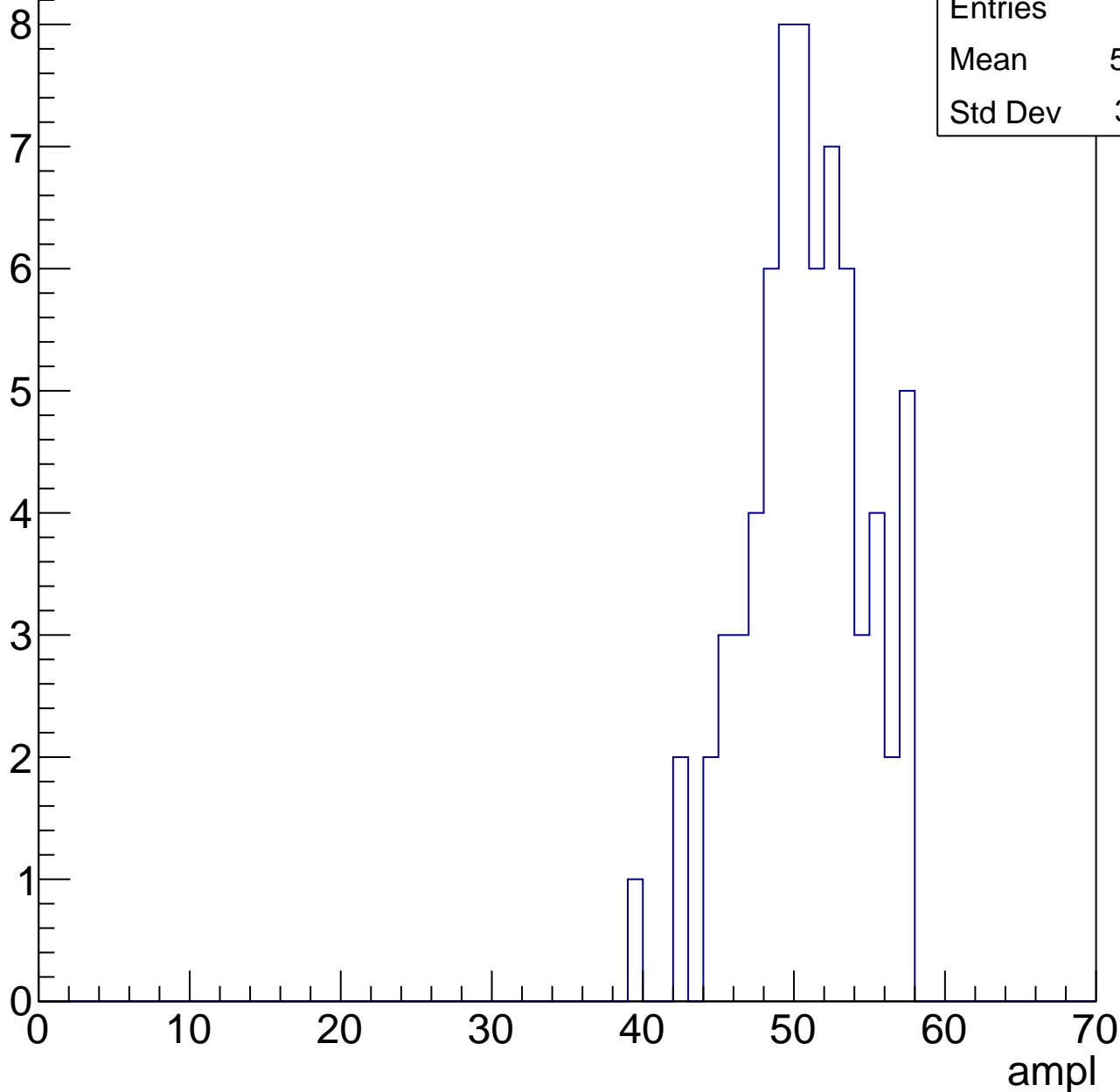


# B1L103S, U26-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

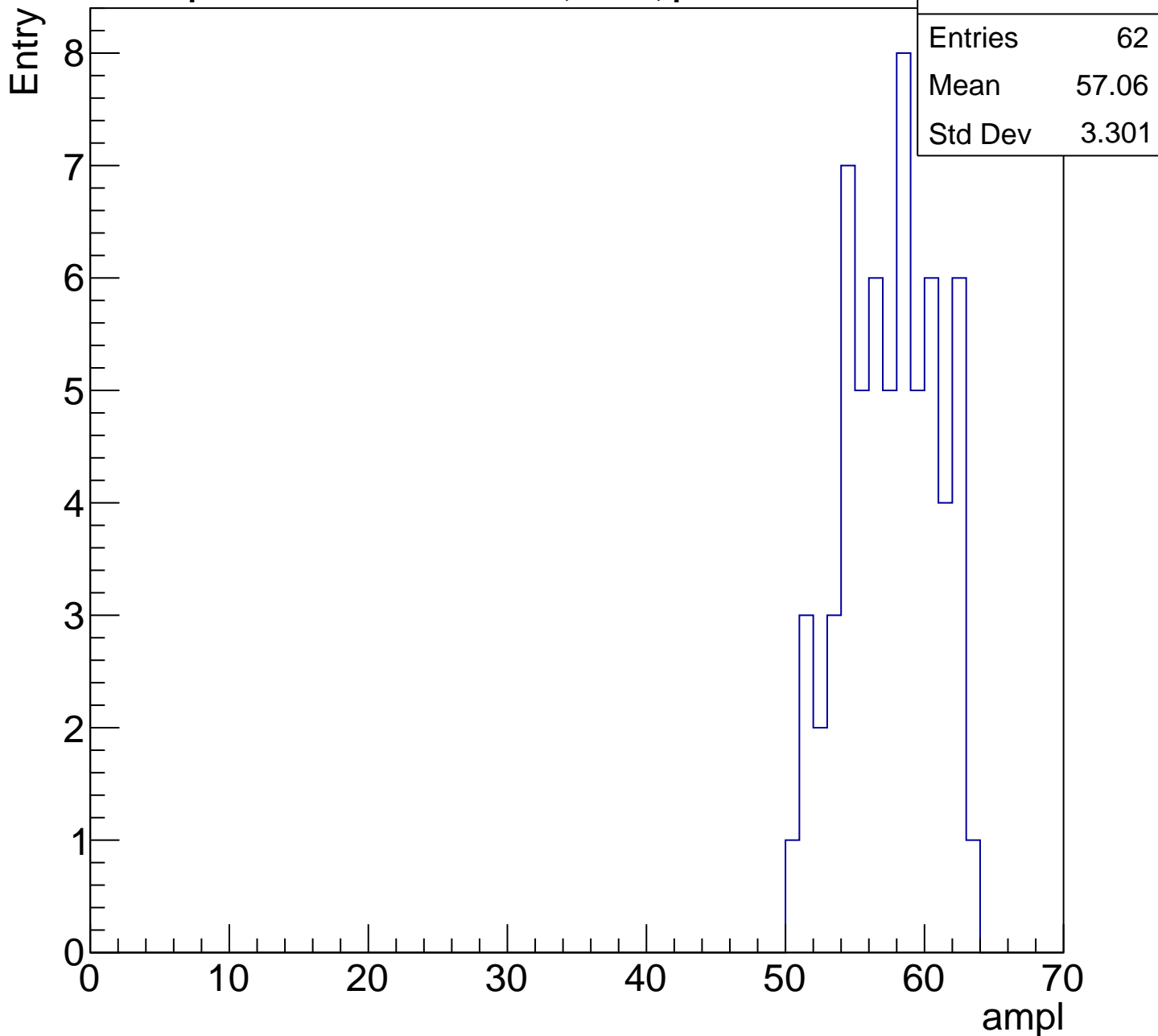
Entry

Entries	70
Mean	50.27
Std Dev	3.891



# B1L103S, U26-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

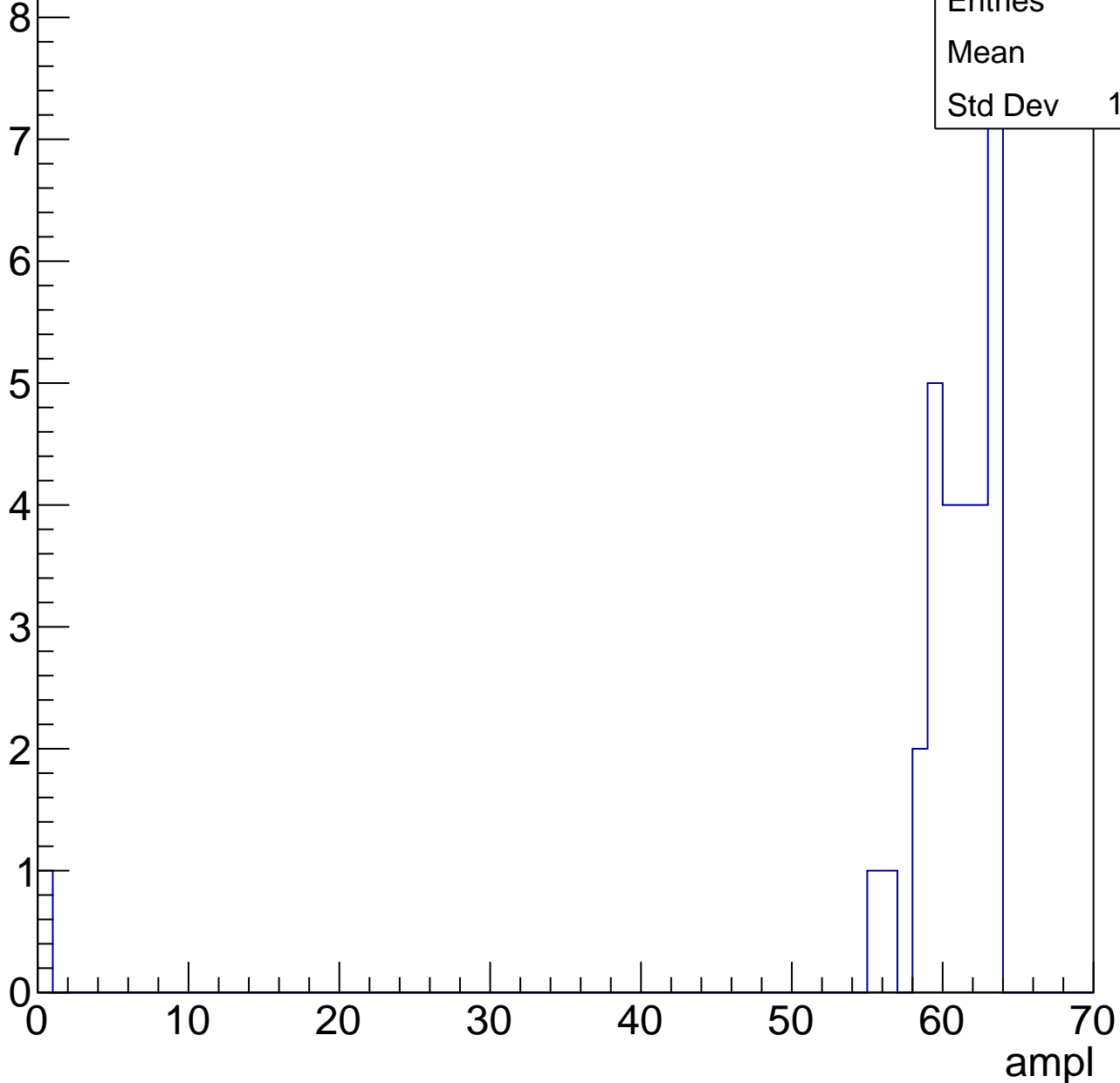


# B1L103S, U26-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	30
Mean	58.6
Std Dev	11.09



# B1L103S, U26-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	61.67
Std Dev	0.9428



# B1L103S, U26-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch54, adc0

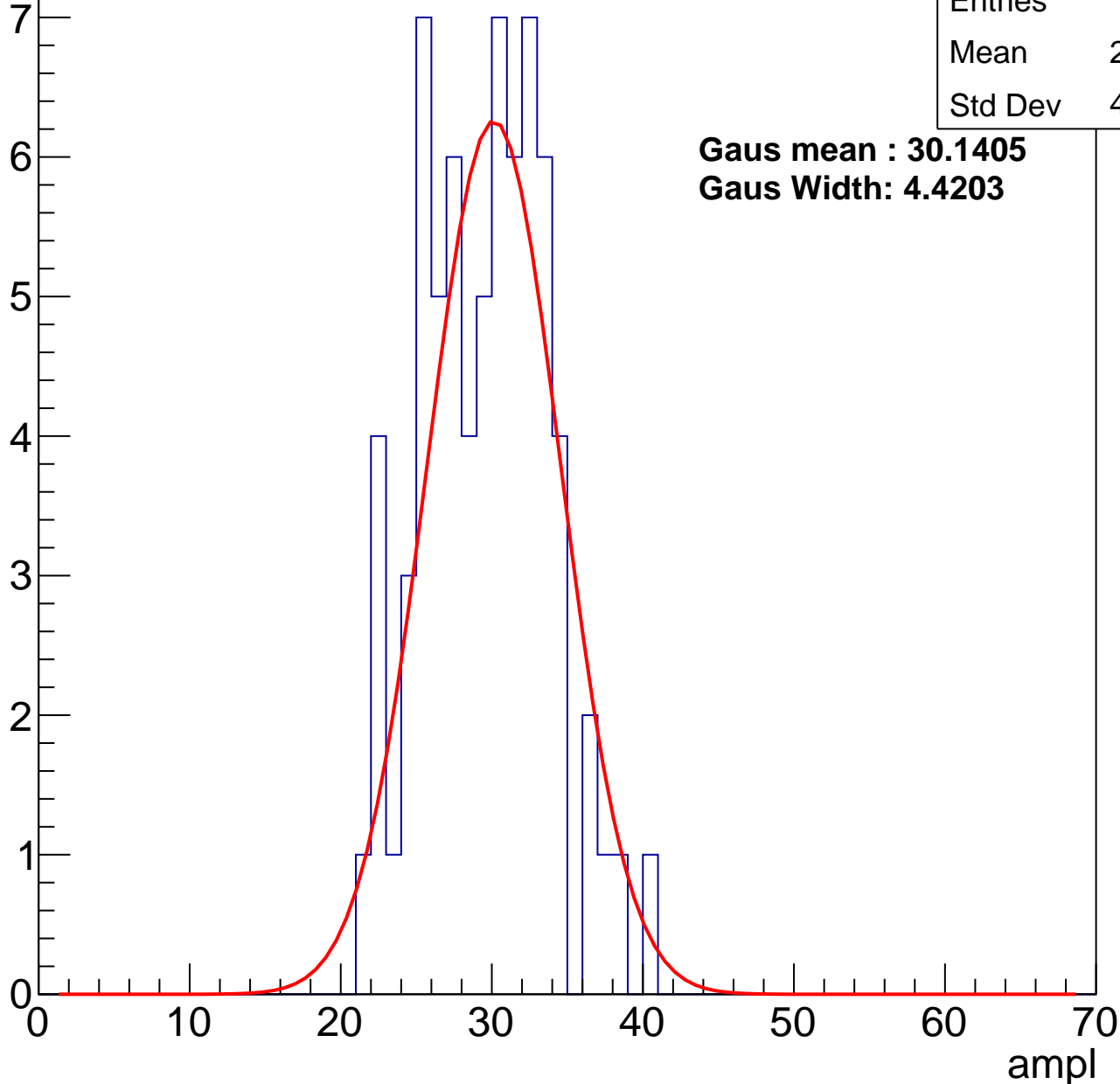
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	29.14
Std Dev	4.126

**Gaus mean : 30.1405**

**Gaus Width: 4.4203**



# B1L103S, U26-ch54, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	70
Mean	35.91
Std Dev	3.872

**Gaus mean : 37.1157**

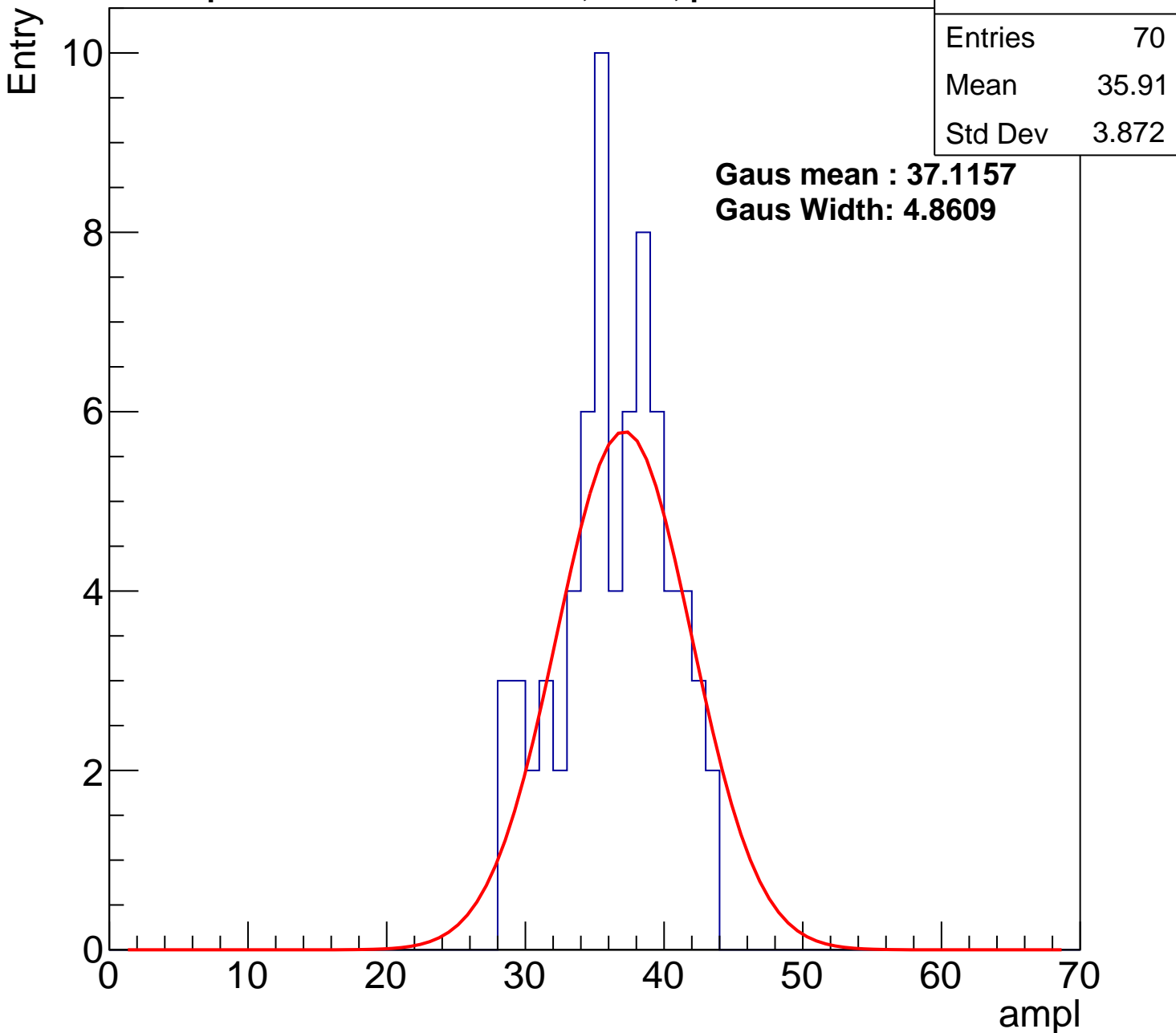
**Gaus Width: 4.8609**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

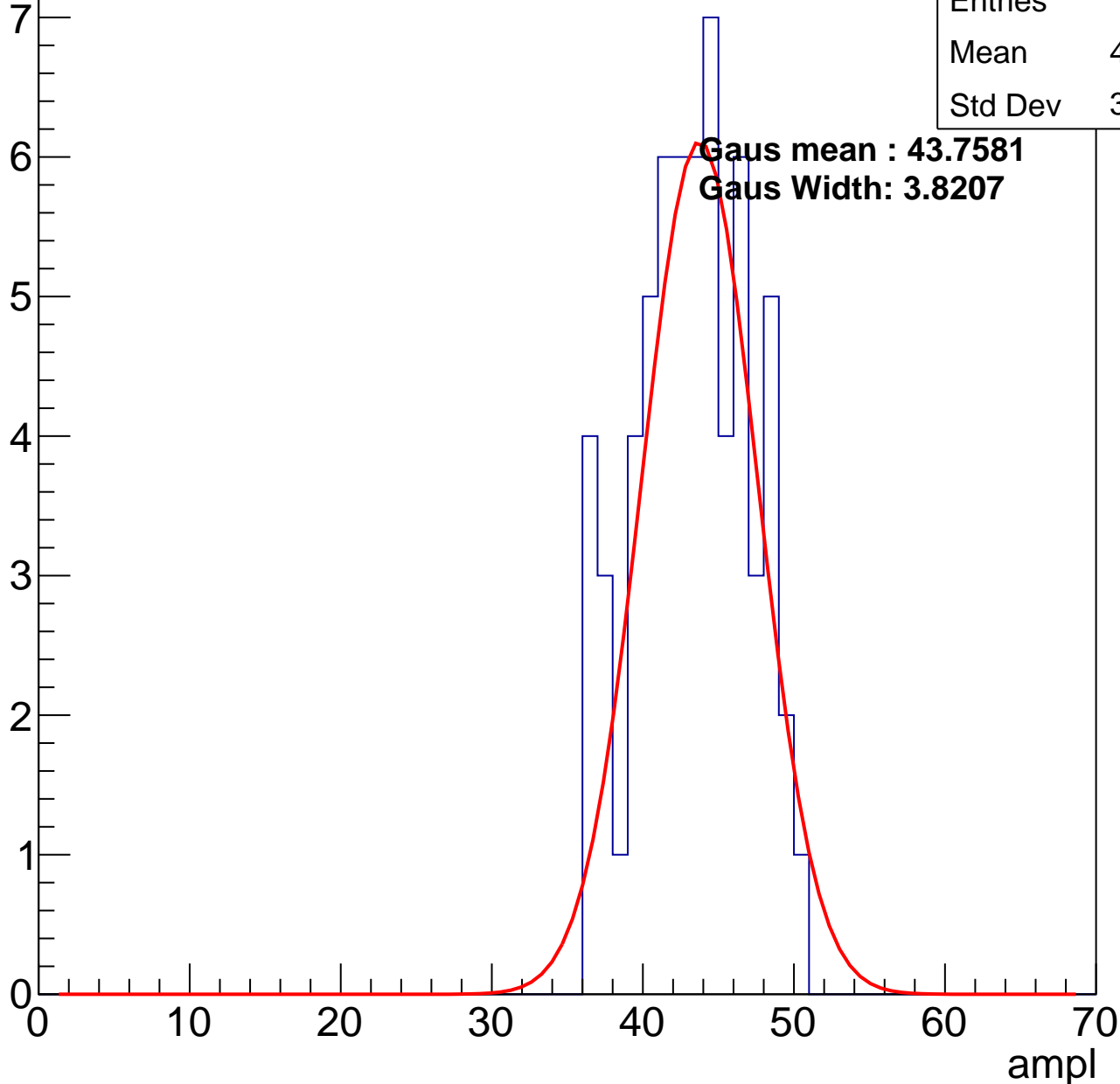


# B1L103S, U26-ch54, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	42.83
Std Dev	3.645

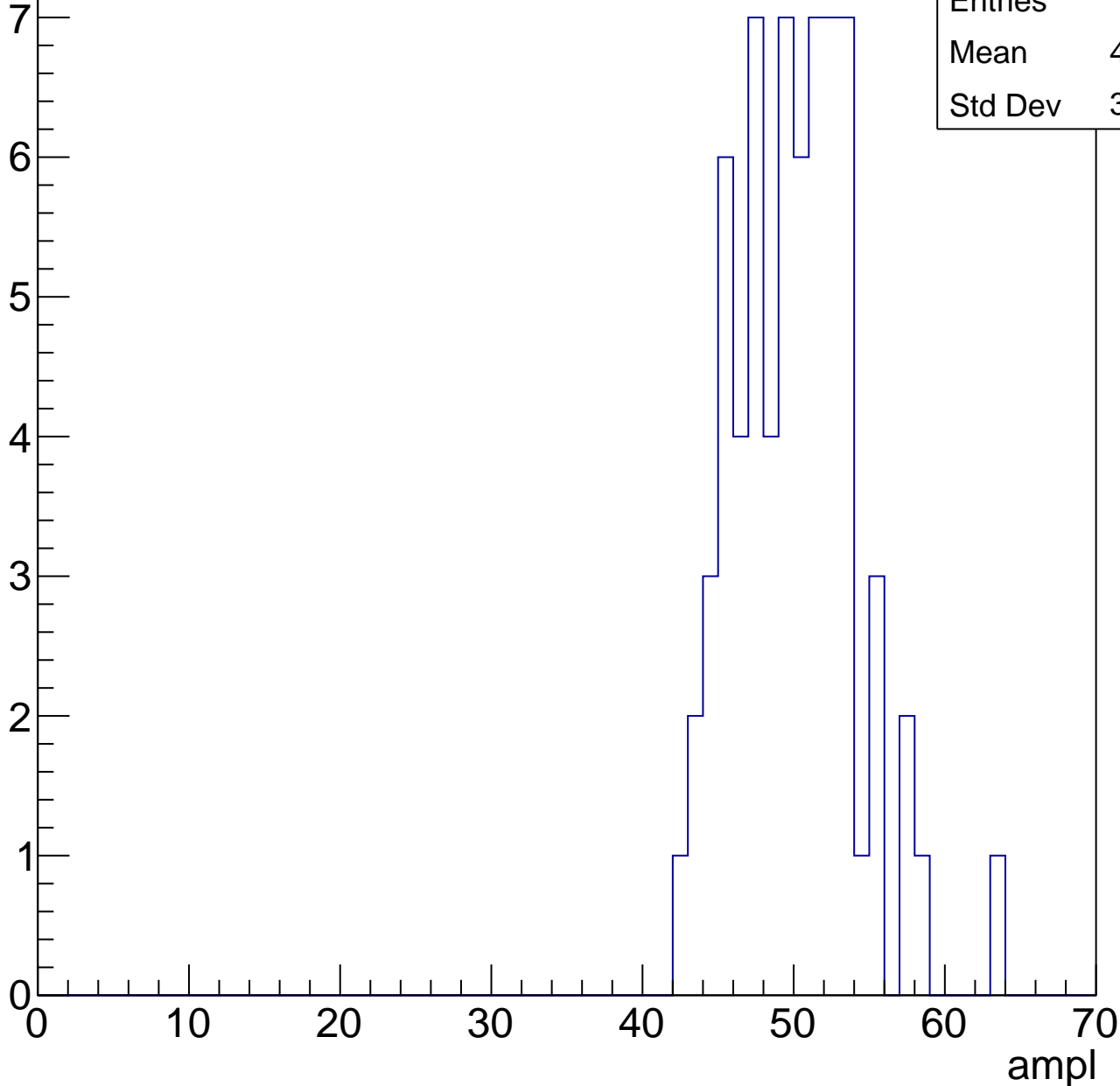


# B1L103S, U26-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	49.62
Std Dev	3.957

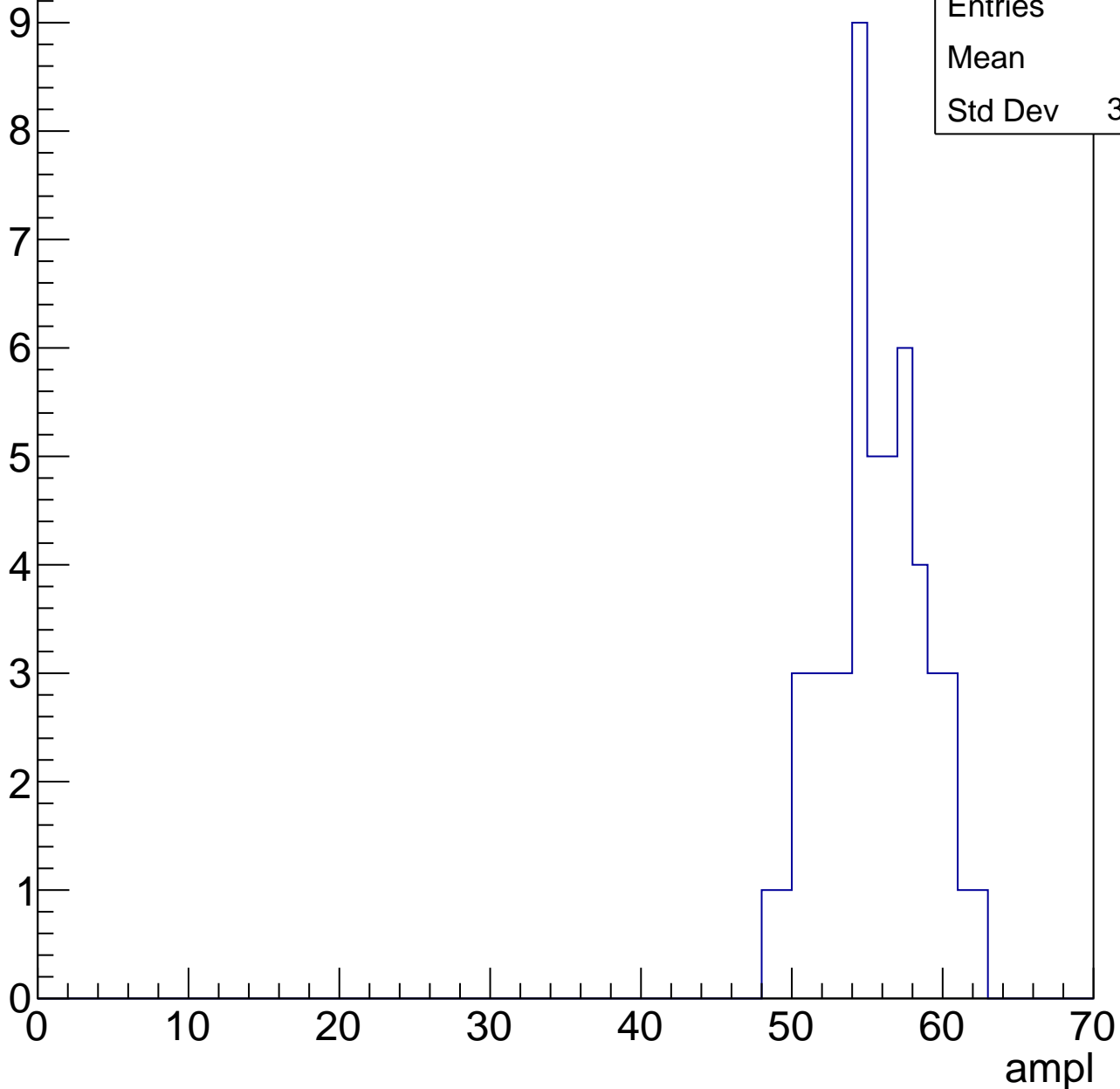


# B1L103S, U26-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	55.1
Std Dev	3.219

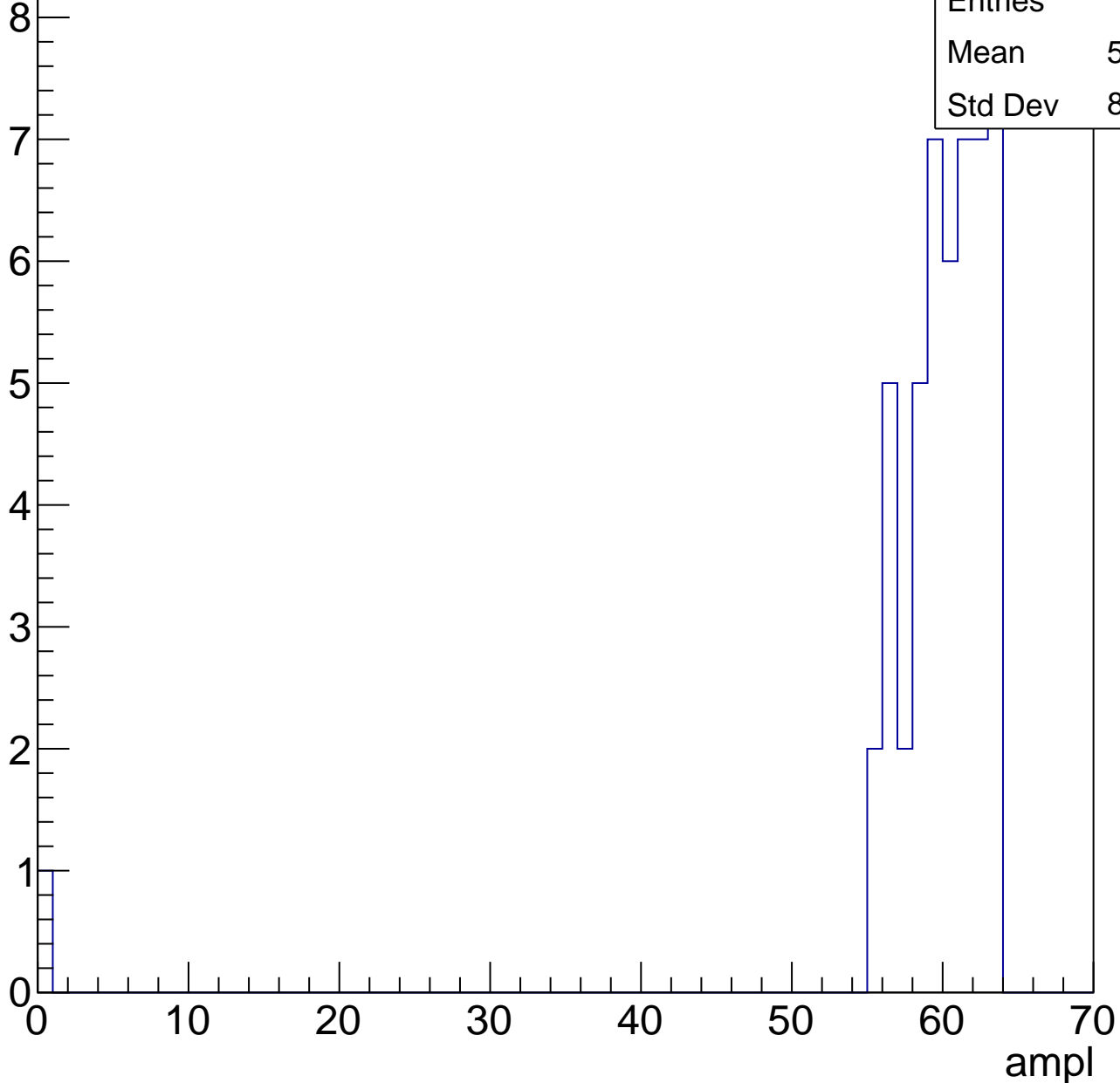


# B1L103S, U26-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	58.64
Std Dev	8.706



# B1L103S, U26-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.5
Std Dev	0.9574

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U26-ch55, adc0

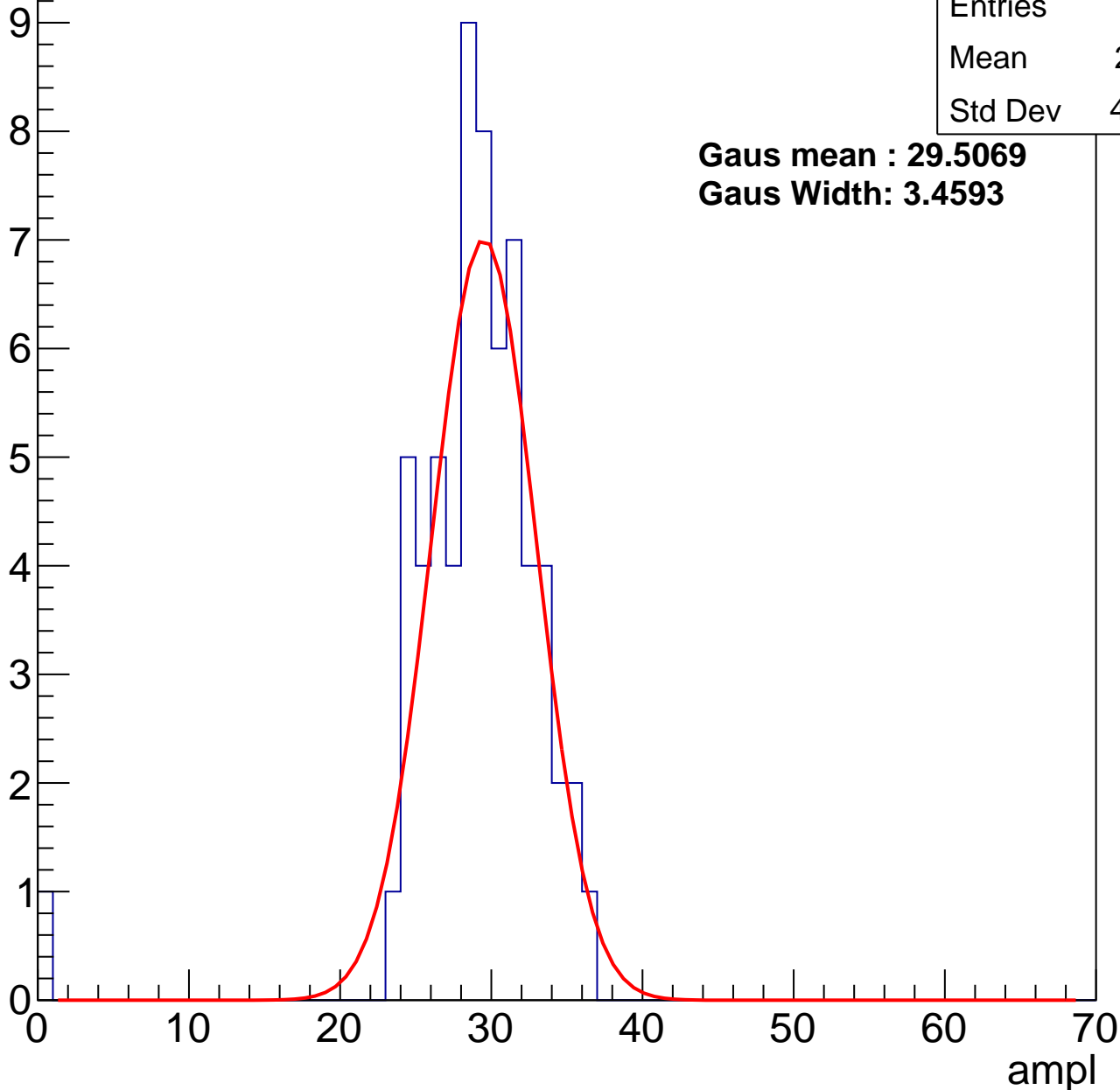
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	28.51
Std Dev	4.757

**Gaus mean : 29.5069**

**Gaus Width: 3.4593**



# B1L103S, U26-ch55, adc1

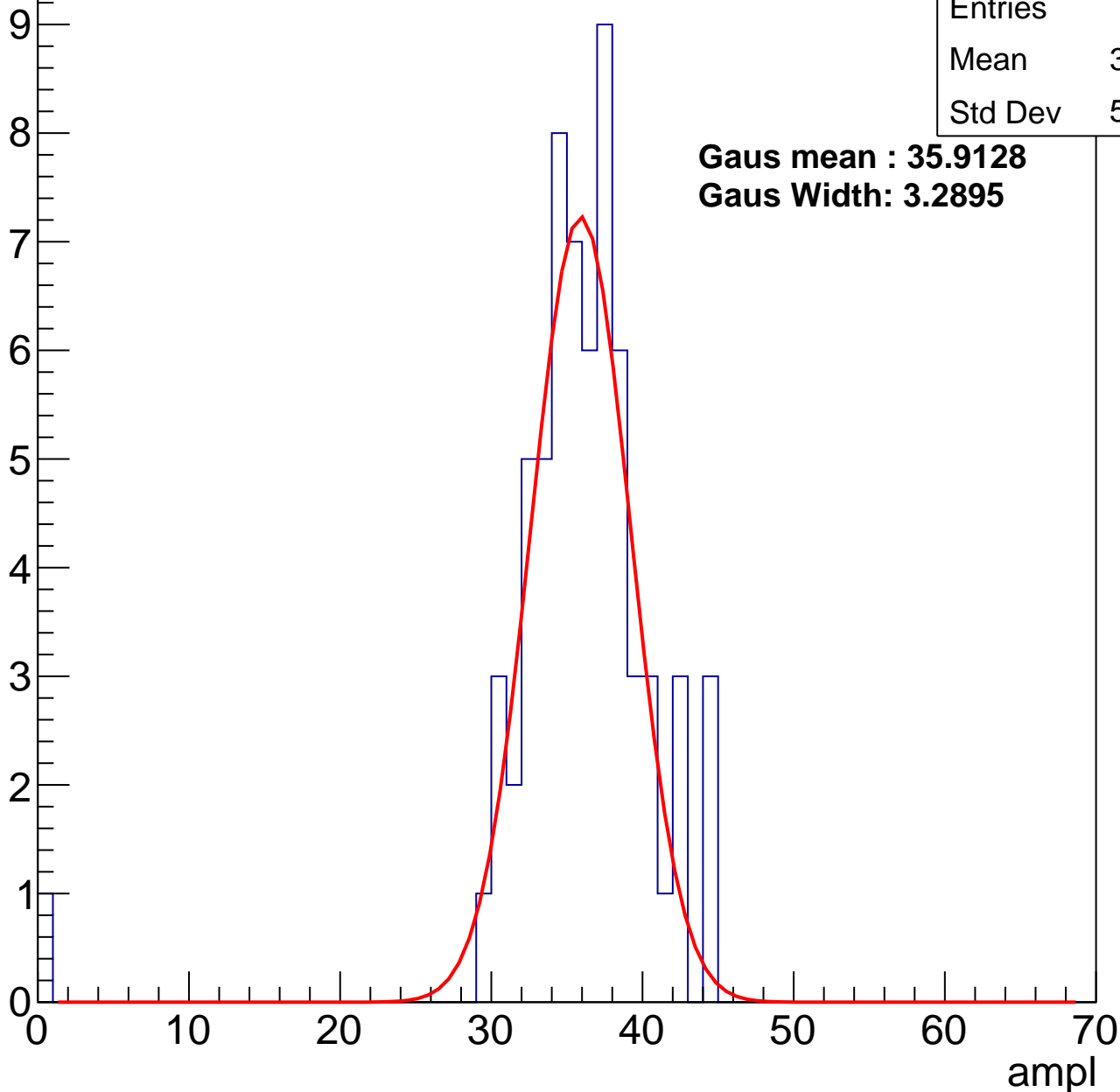
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	35.39
Std Dev	5.608

**Gaus mean : 35.9128**

**Gaus Width: 3.2895**



# B1L103S, U26-ch55, adc2

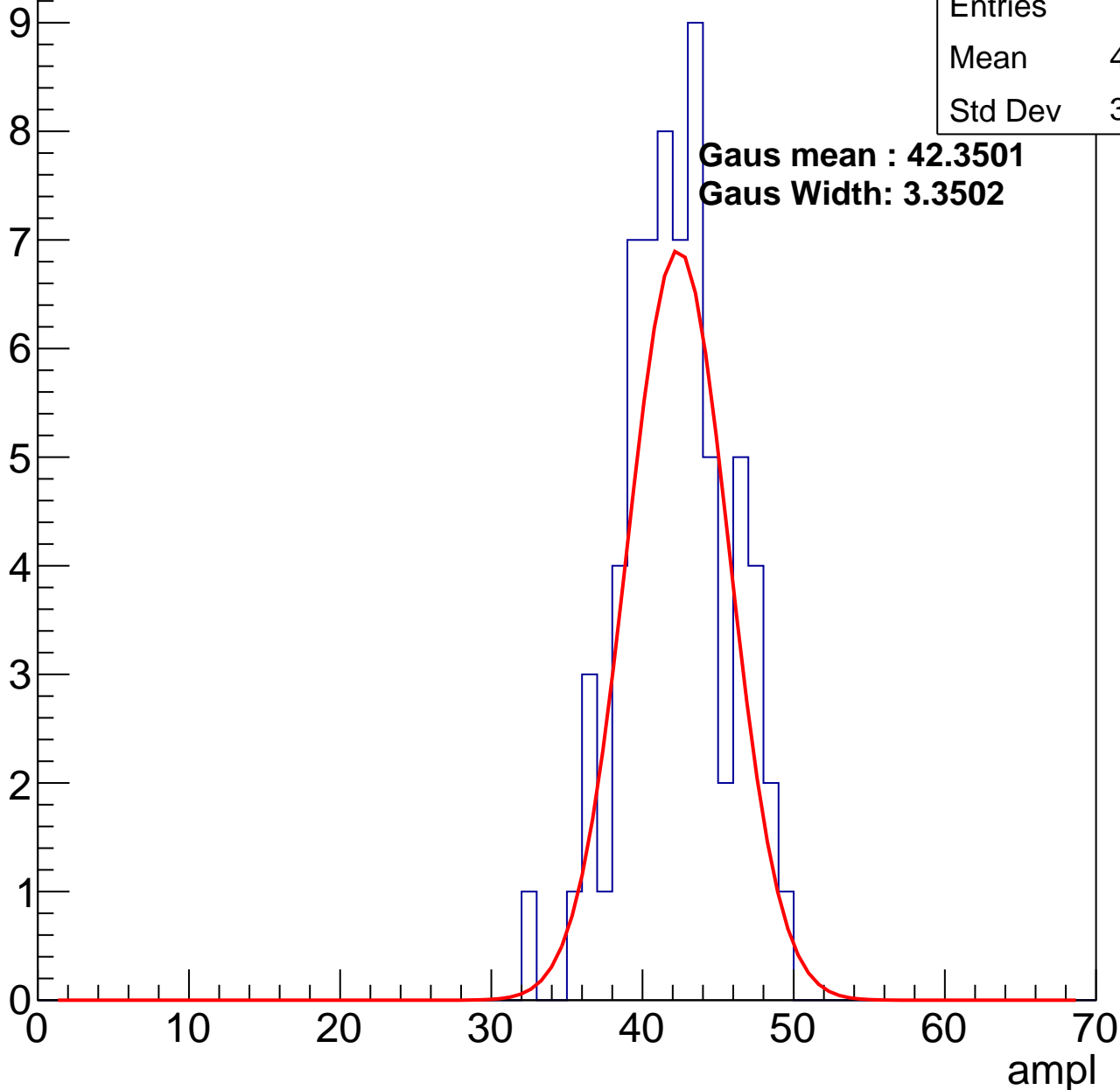
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	41.78
Std Dev	3.433

**Gaus mean : 42.3501**

**Gaus Width: 3.3502**

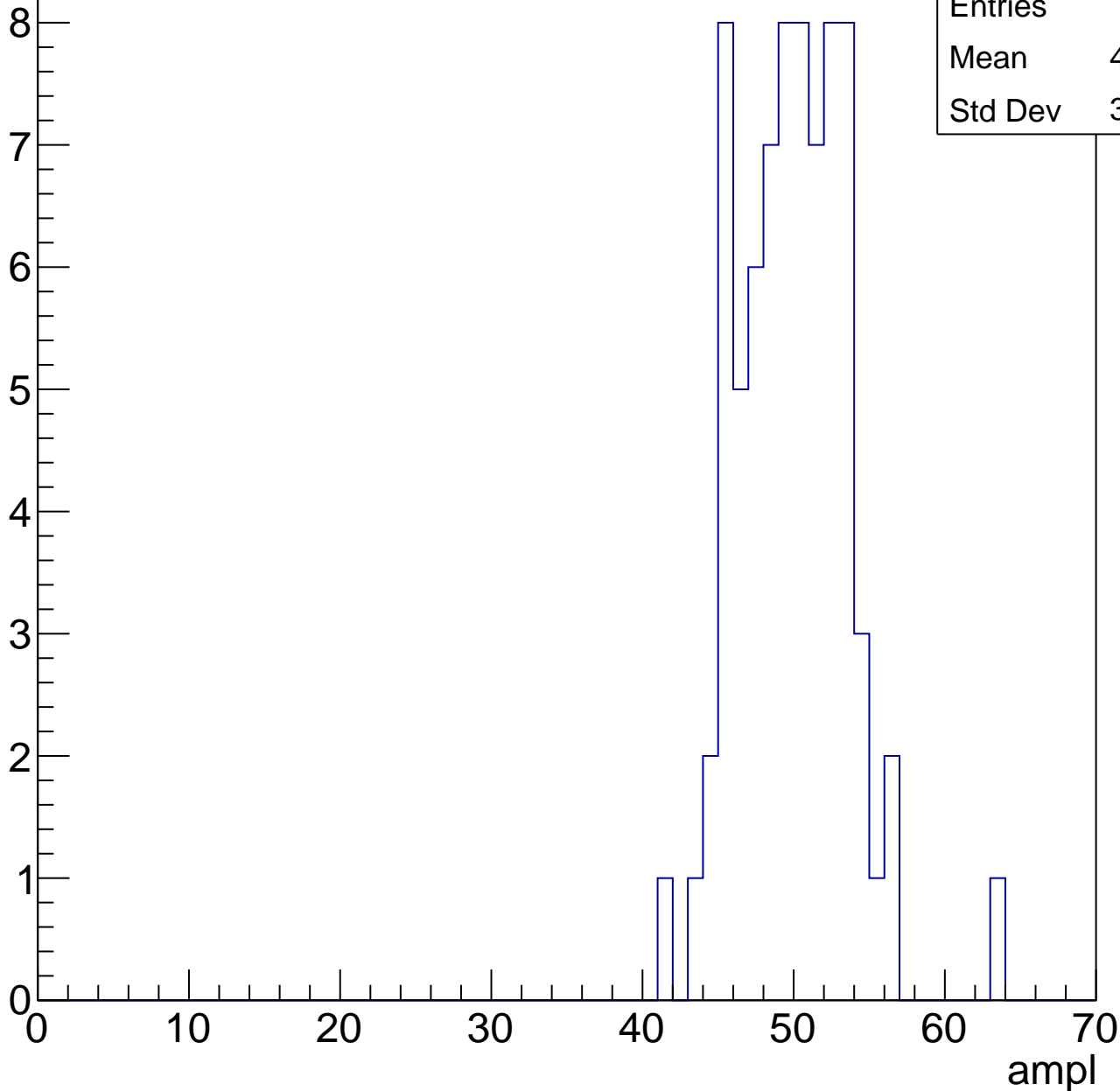


# B1L103S, U26-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

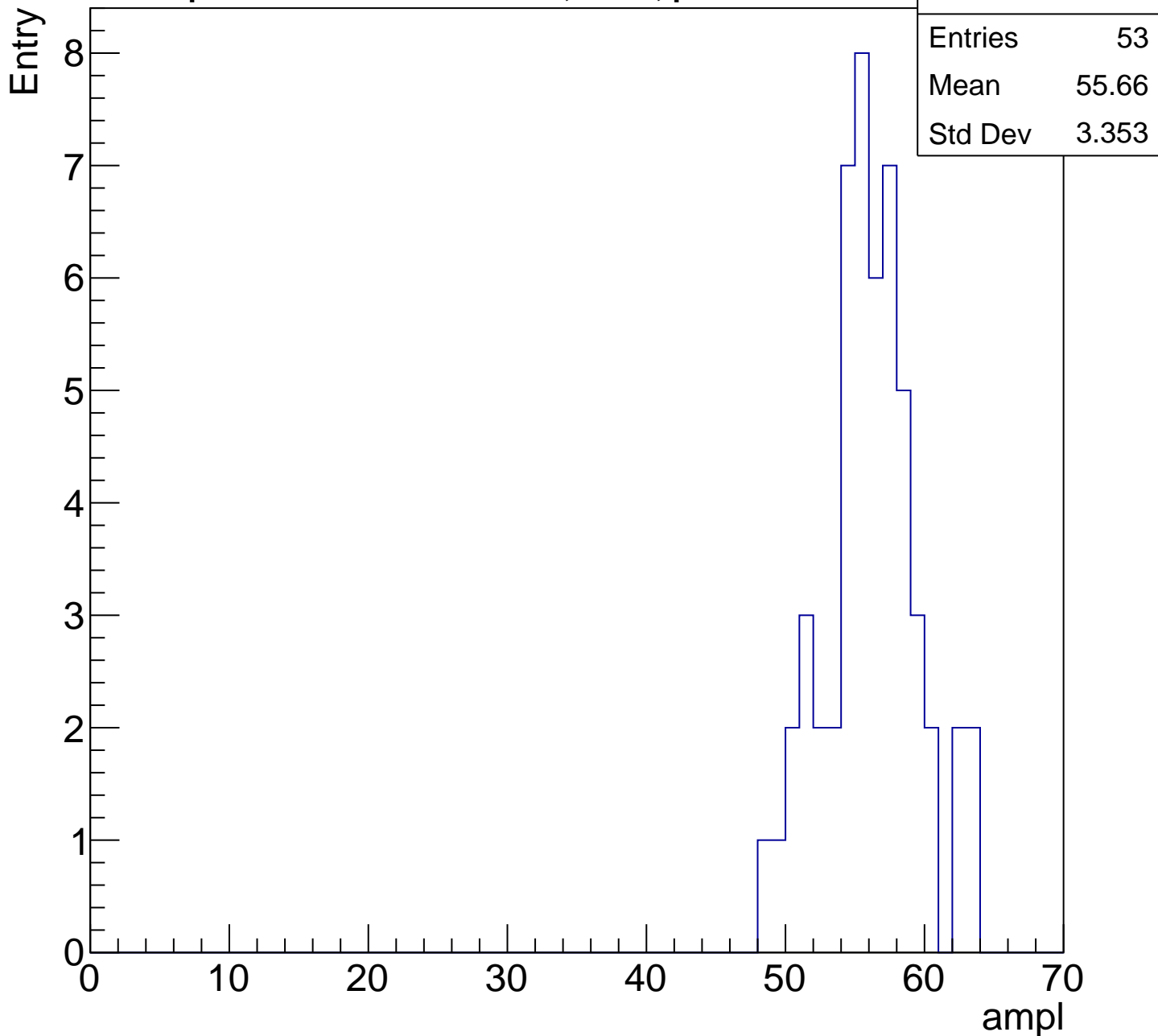
Entry

Entries	76
Mean	49.49
Std Dev	3.585



# B1L103S, U26-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

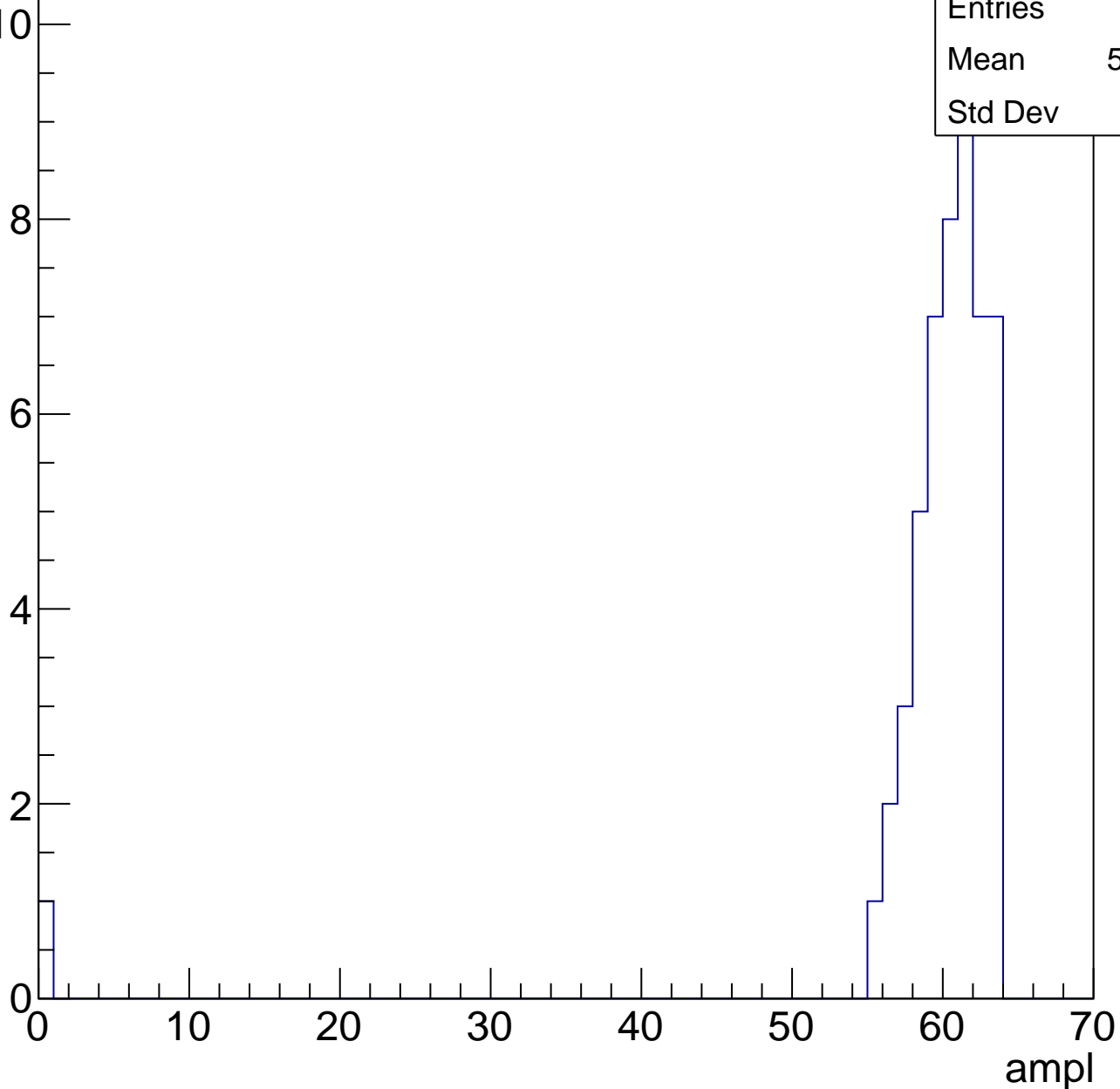


# B1L103S, U26-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	58.94
Std Dev	8.58



# B1L103S, U26-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U26-ch56, adc0

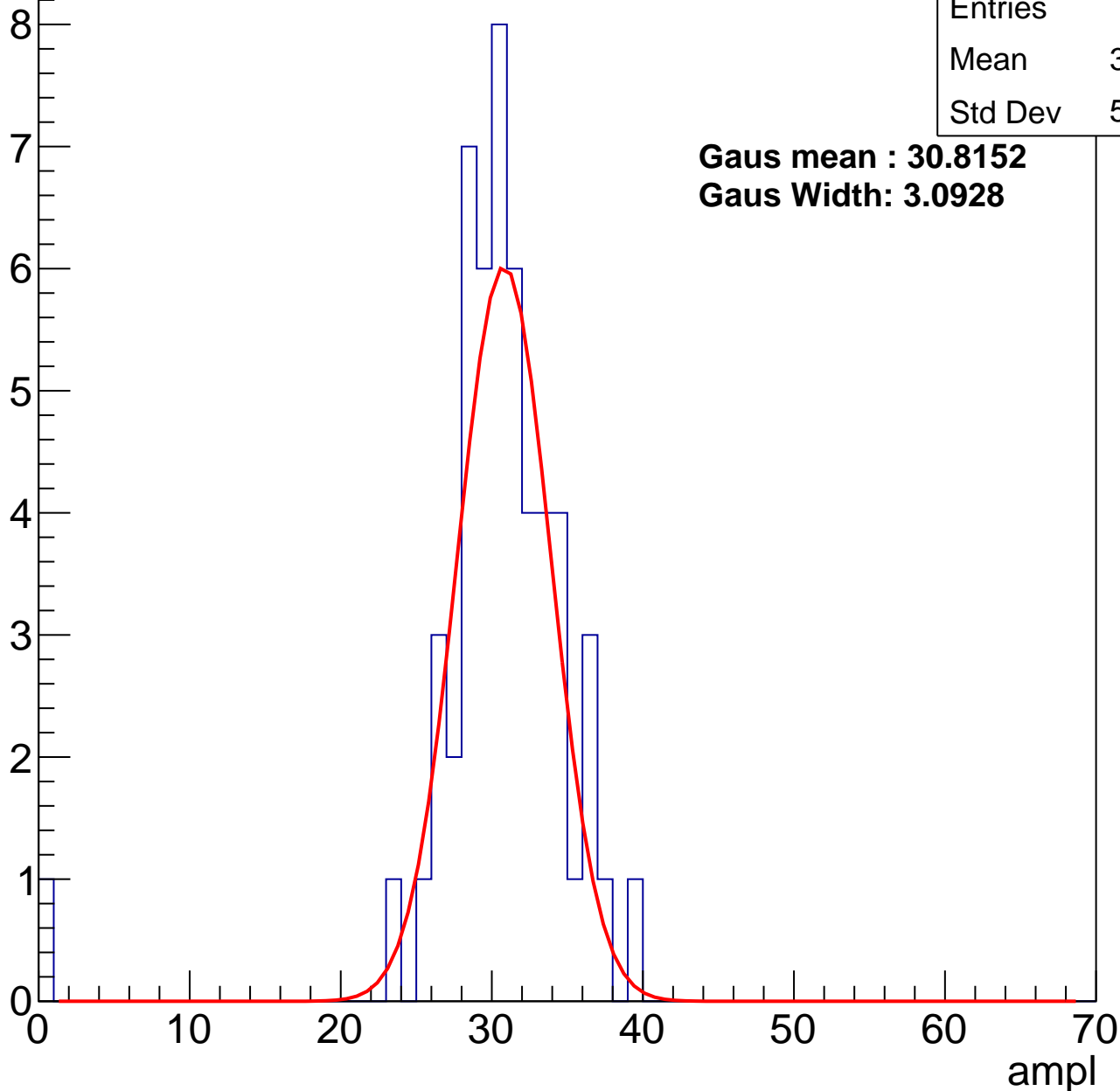
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	30.02
Std Dev	5.247

**Gaus mean : 30.8152**

**Gaus Width: 3.0928**



# B1L103S, U26-ch56, adc1

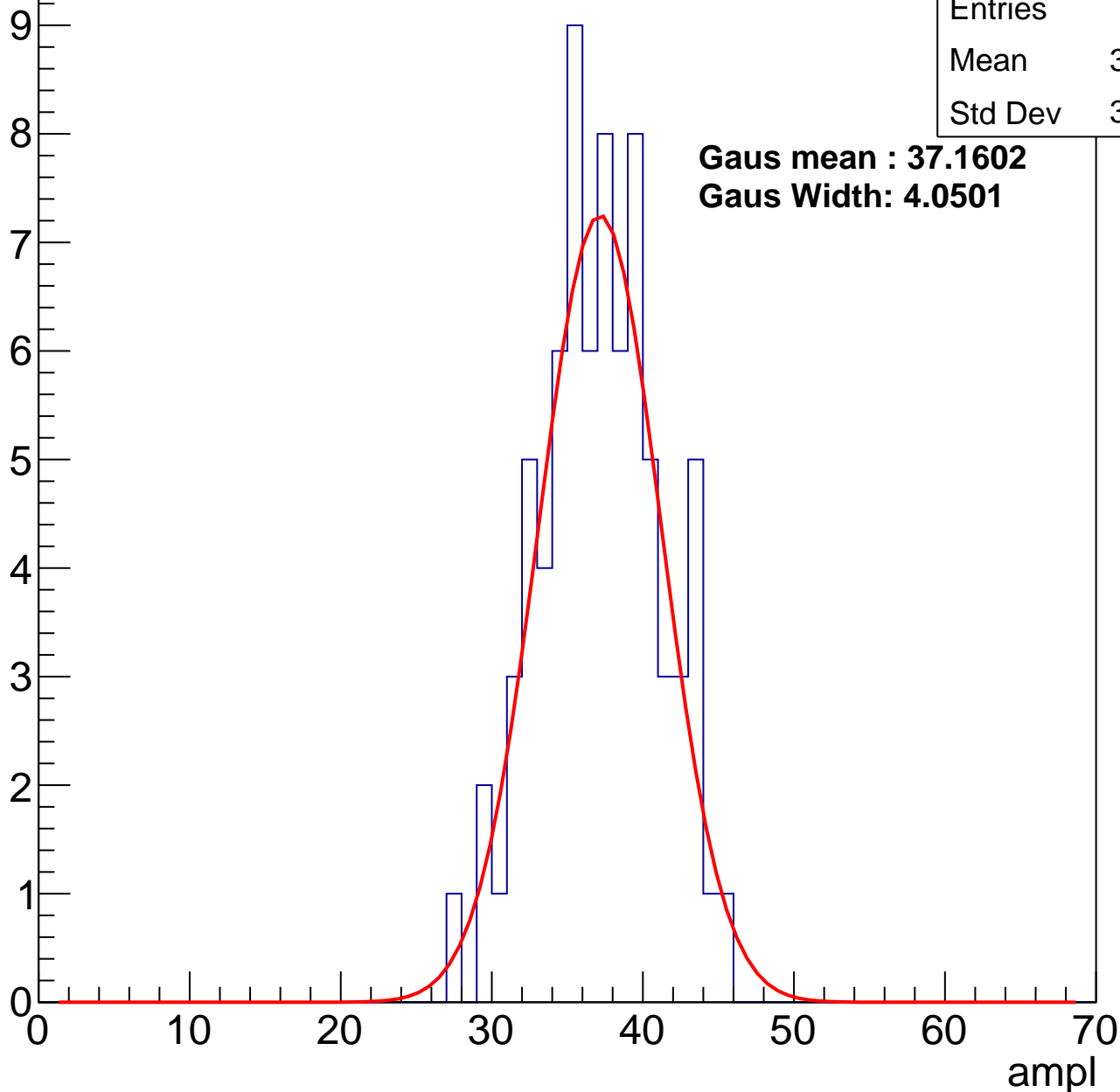
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	36.68
Std Dev	3.883

**Gaus mean : 37.1602**

**Gaus Width: 4.0501**



# B1L103S, U26-ch56, adc2

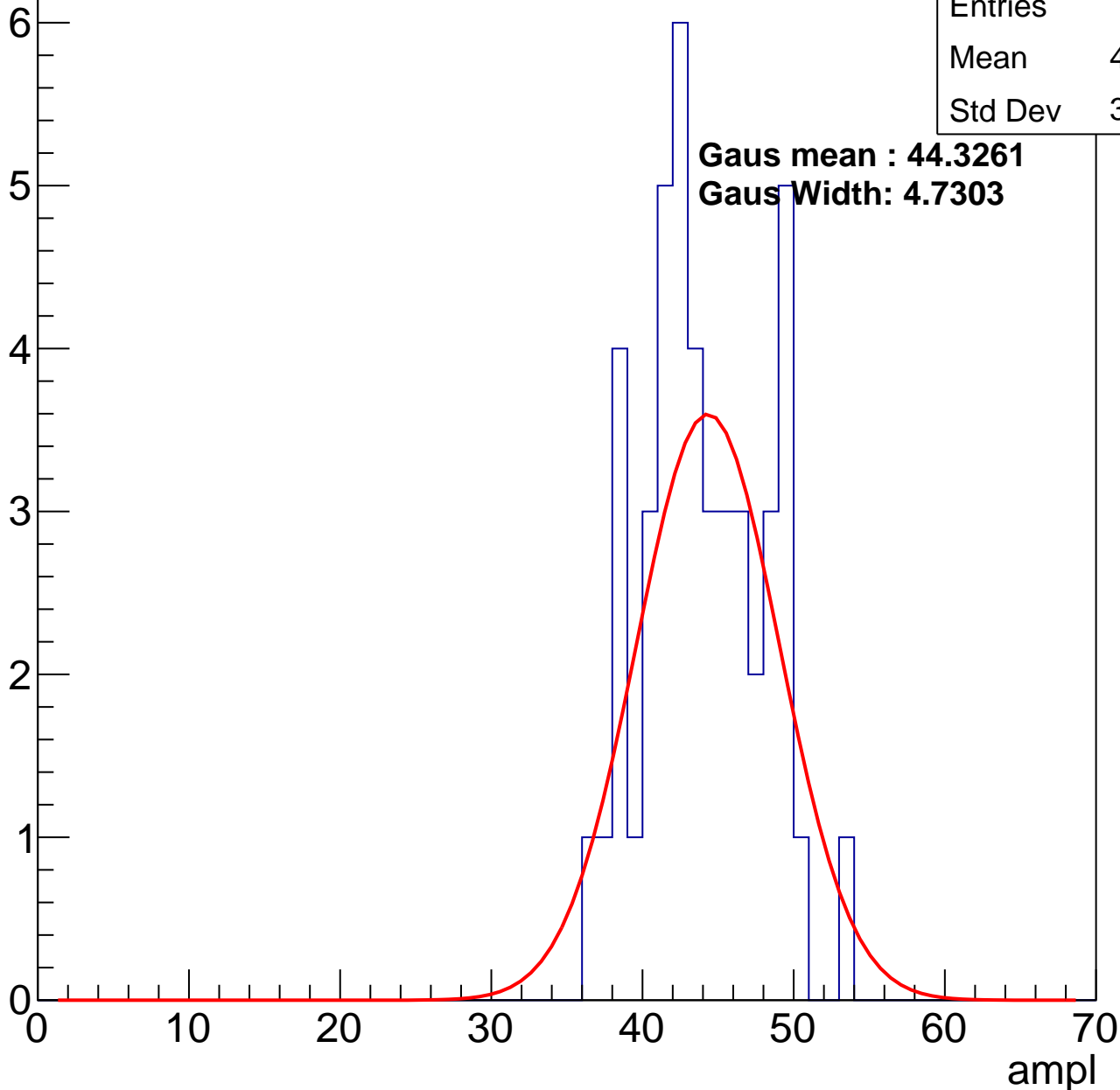
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	43.57
Std Dev	3.949

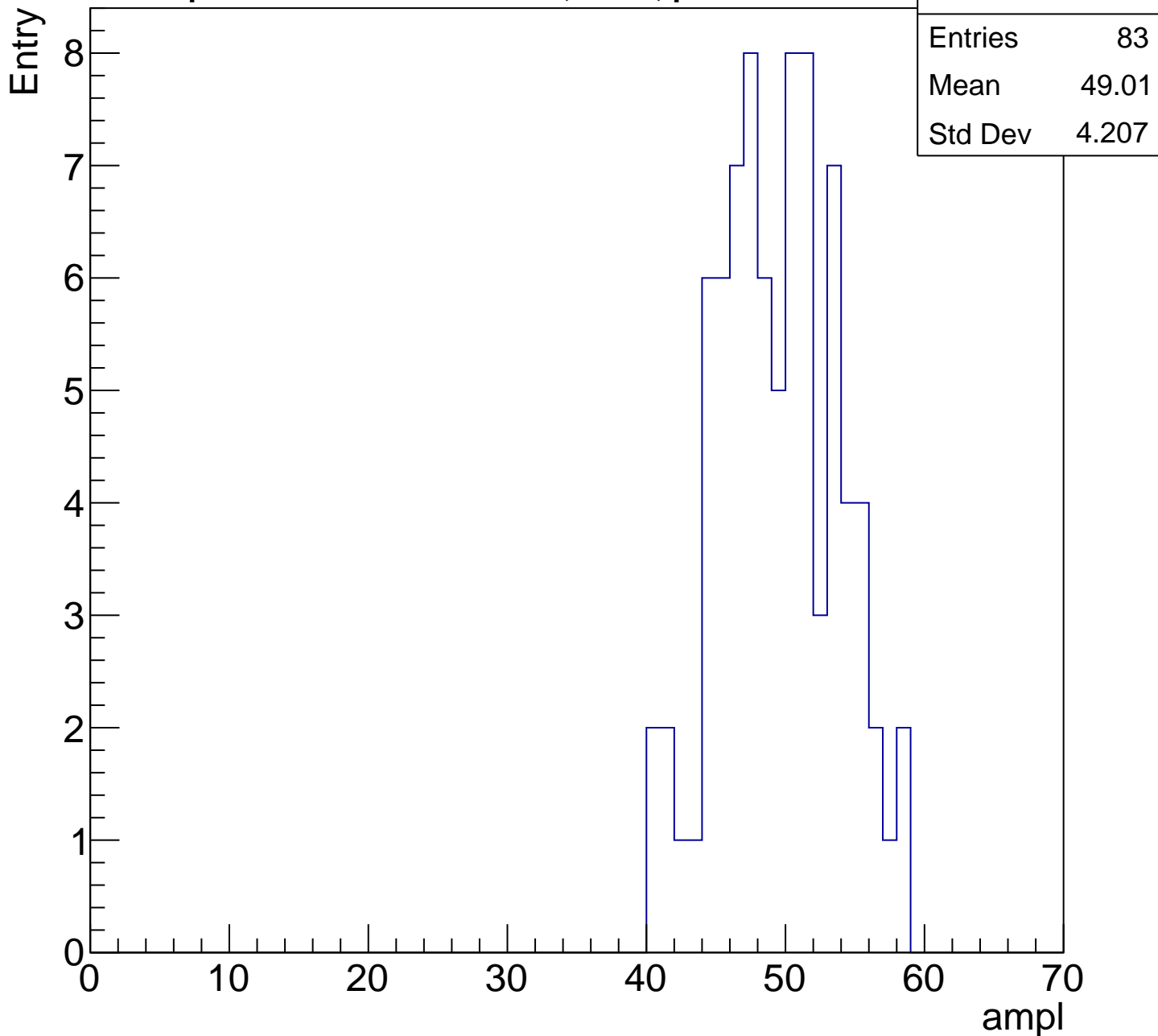
**Gaus mean : 44.3261**

**Gaus Width: 4.7303**



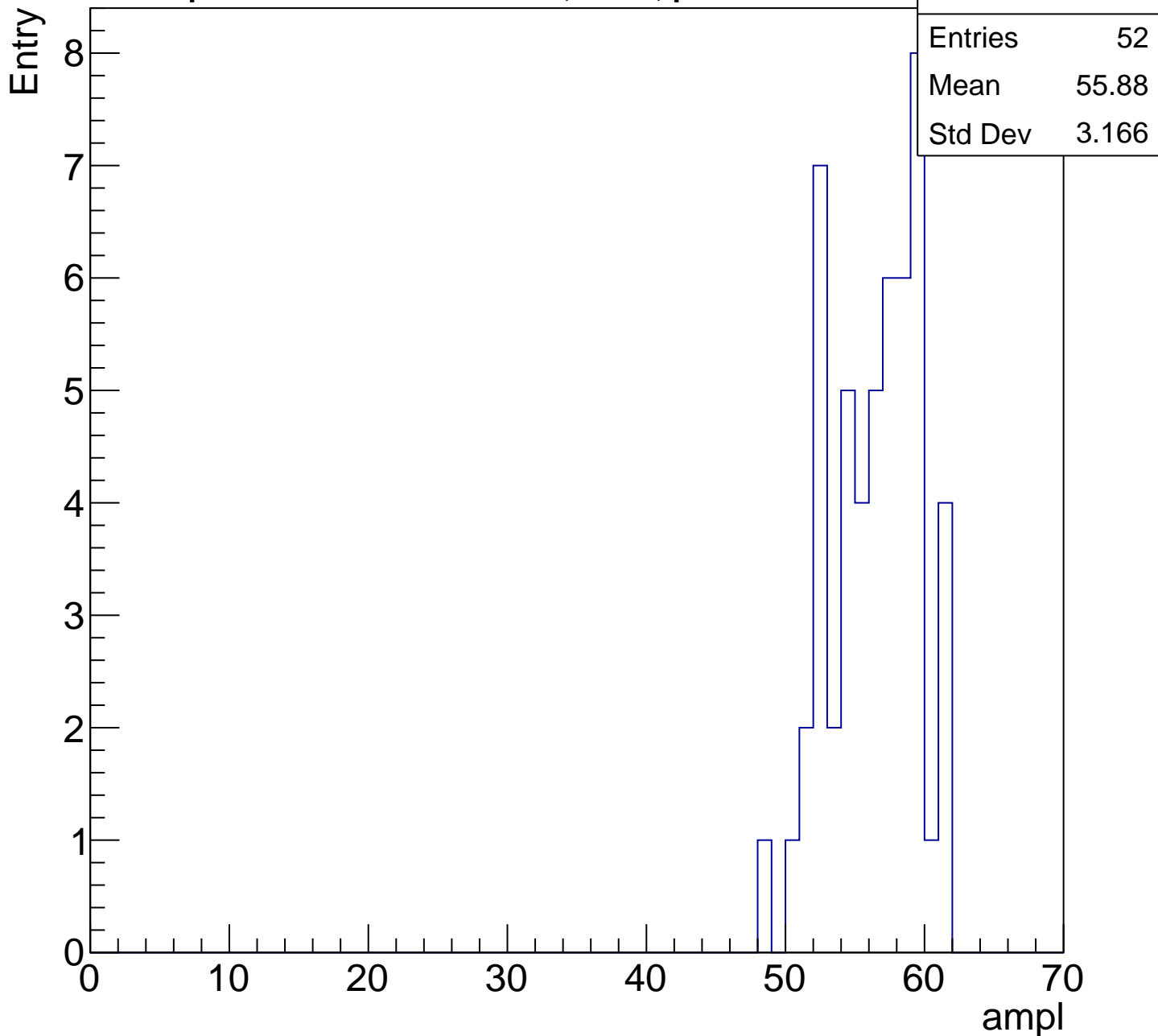
# B1L103S, U26-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U26-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U26-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

Entries	47
Mean	58.87
Std Dev	9.026

# B1L103S, U26-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U26-ch57, adc0

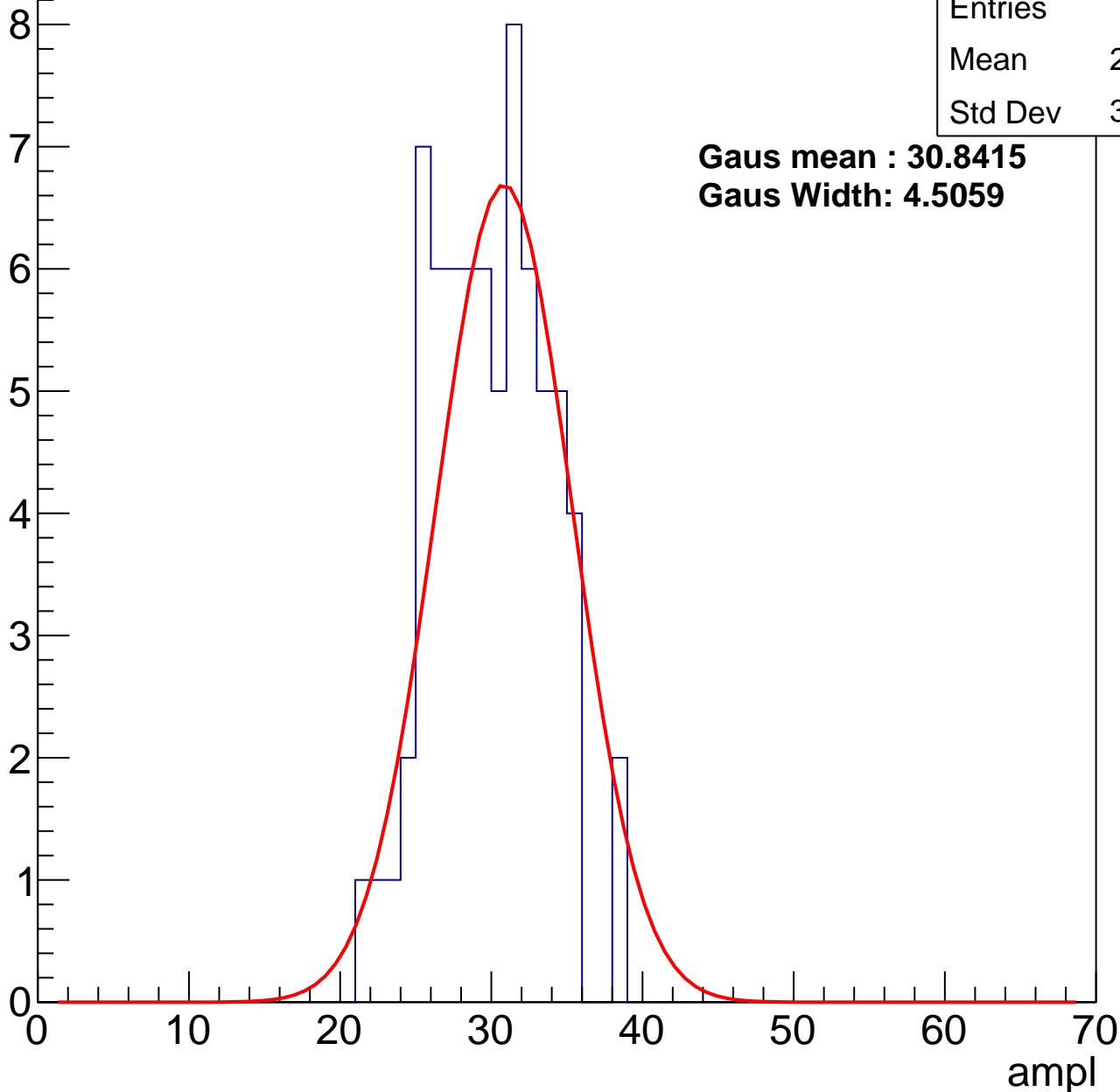
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	29.44
Std Dev	3.722

**Gaus mean : 30.8415**

**Gaus Width: 4.5059**



# B1L103S, U26-ch57, adc1

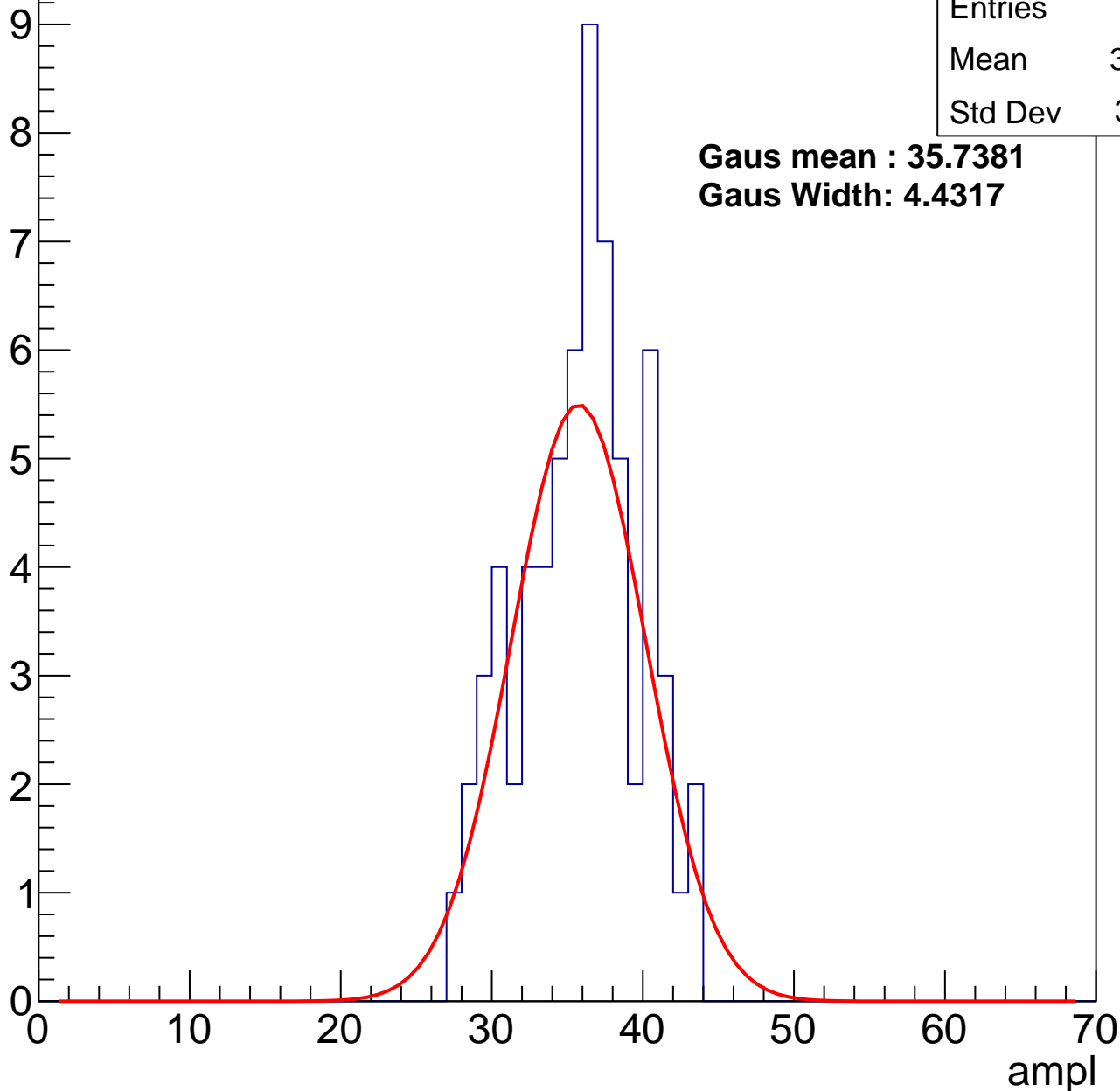
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	35.36
Std Dev	3.891

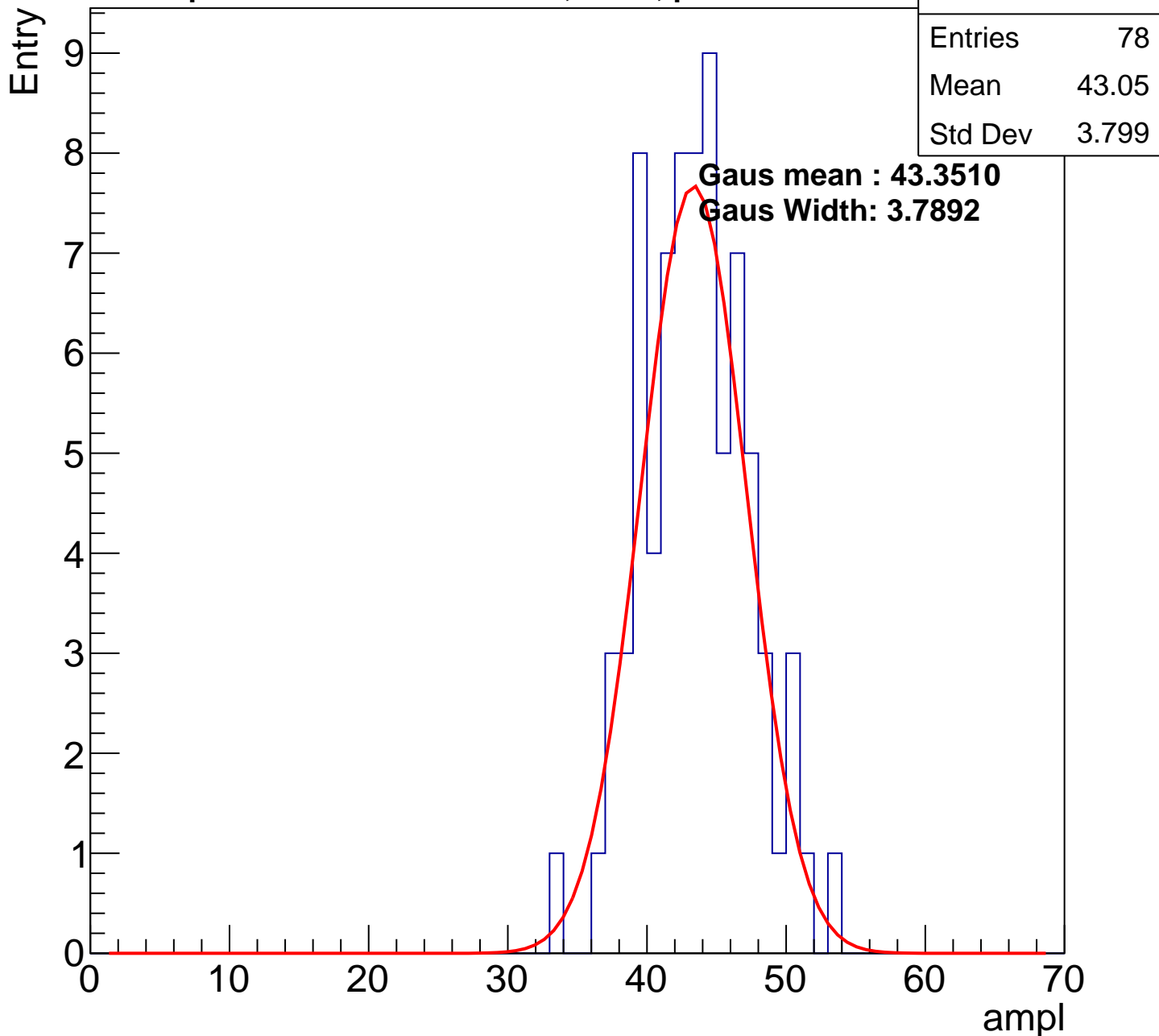
**Gaus mean : 35.7381**

**Gaus Width: 4.4317**



# B1L103S, U26-ch57, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

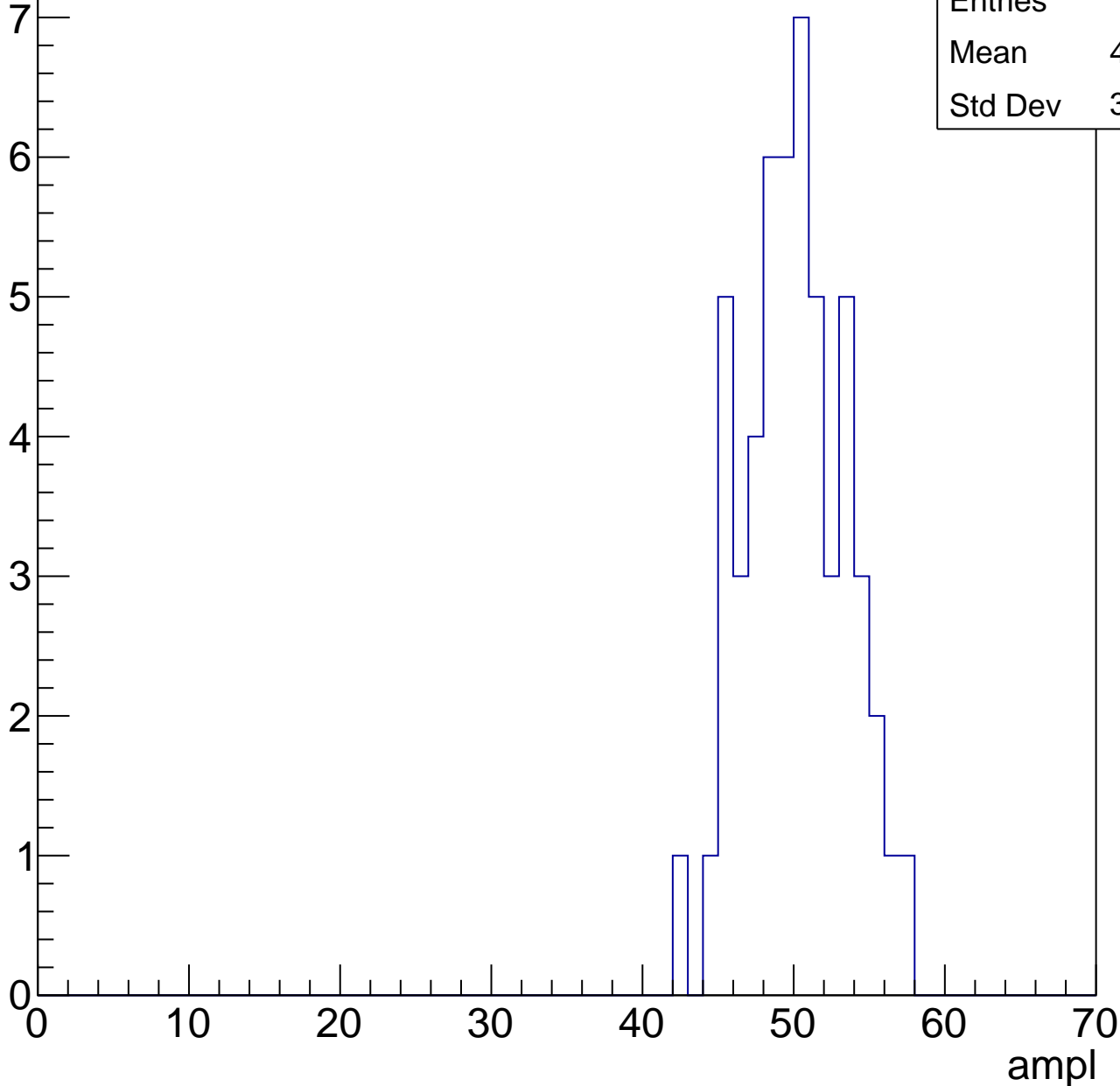


# B1L103S, U26-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

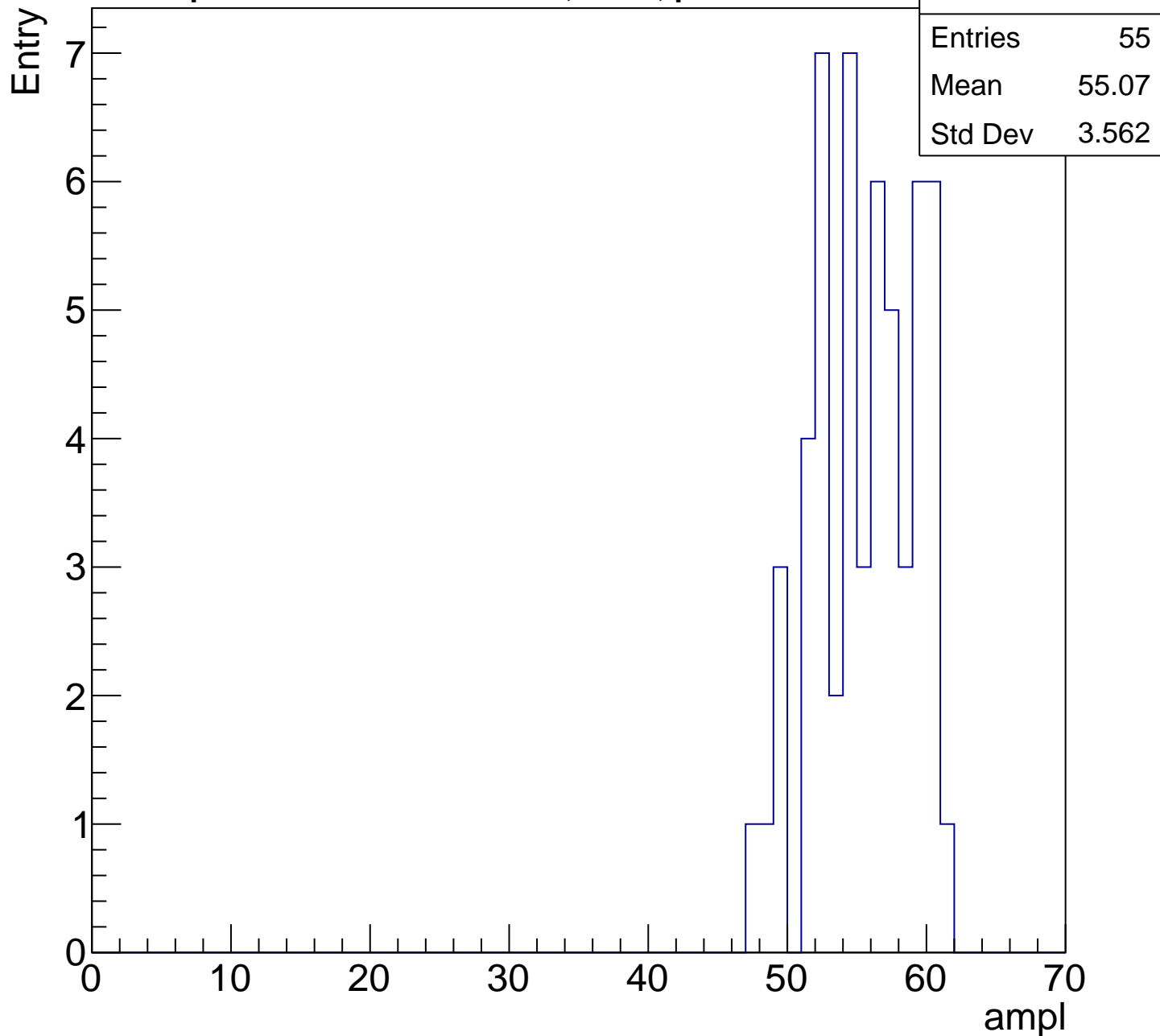
Entry

Entries	53
Mean	49.62
Std Dev	3.298



# B1L103S, U26-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U26-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

Entries	56
Mean	59.54
Std Dev	2.853

0

2

4

6

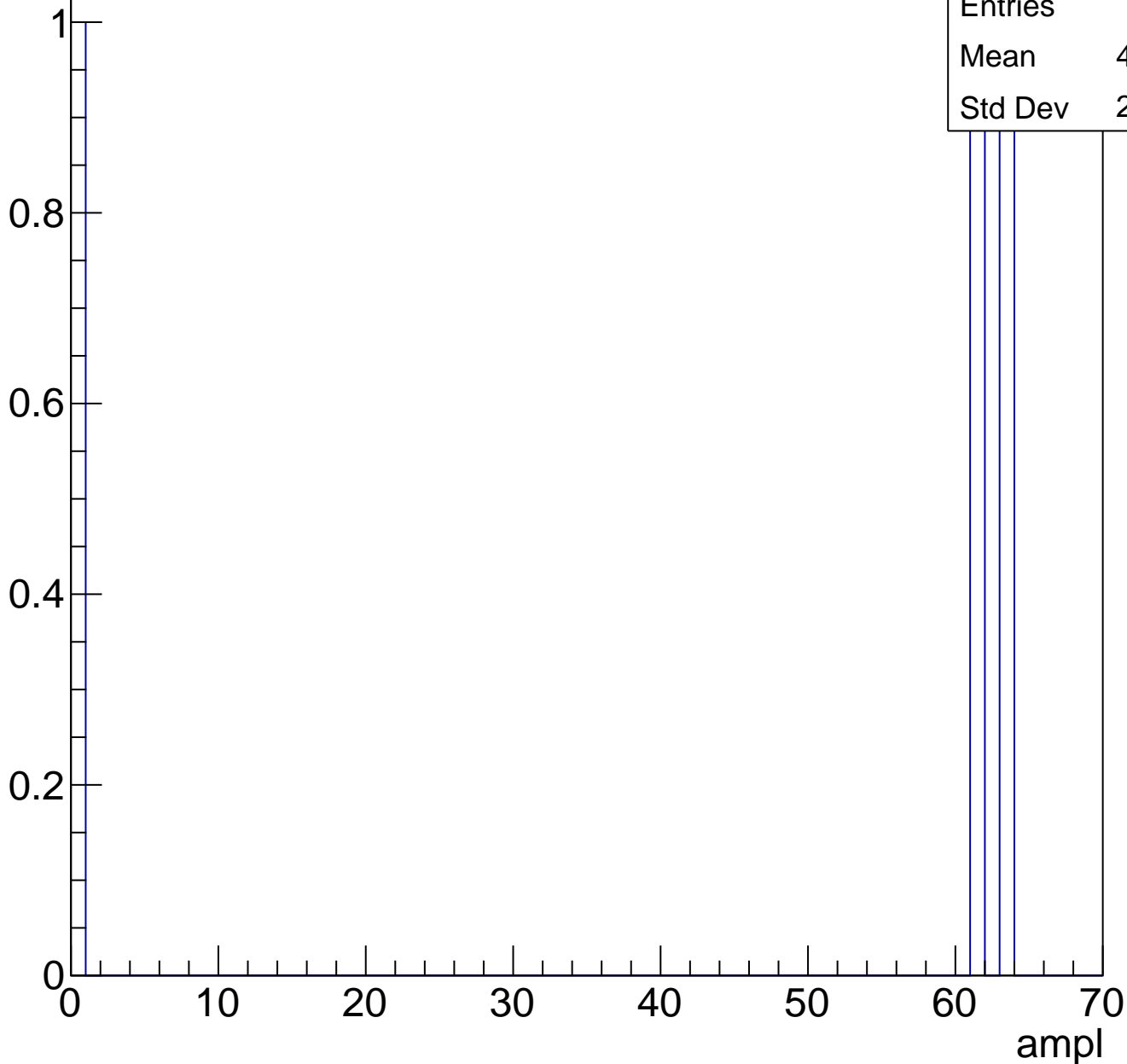
8

10

# B1L103S, U26-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U26-ch58, adc0

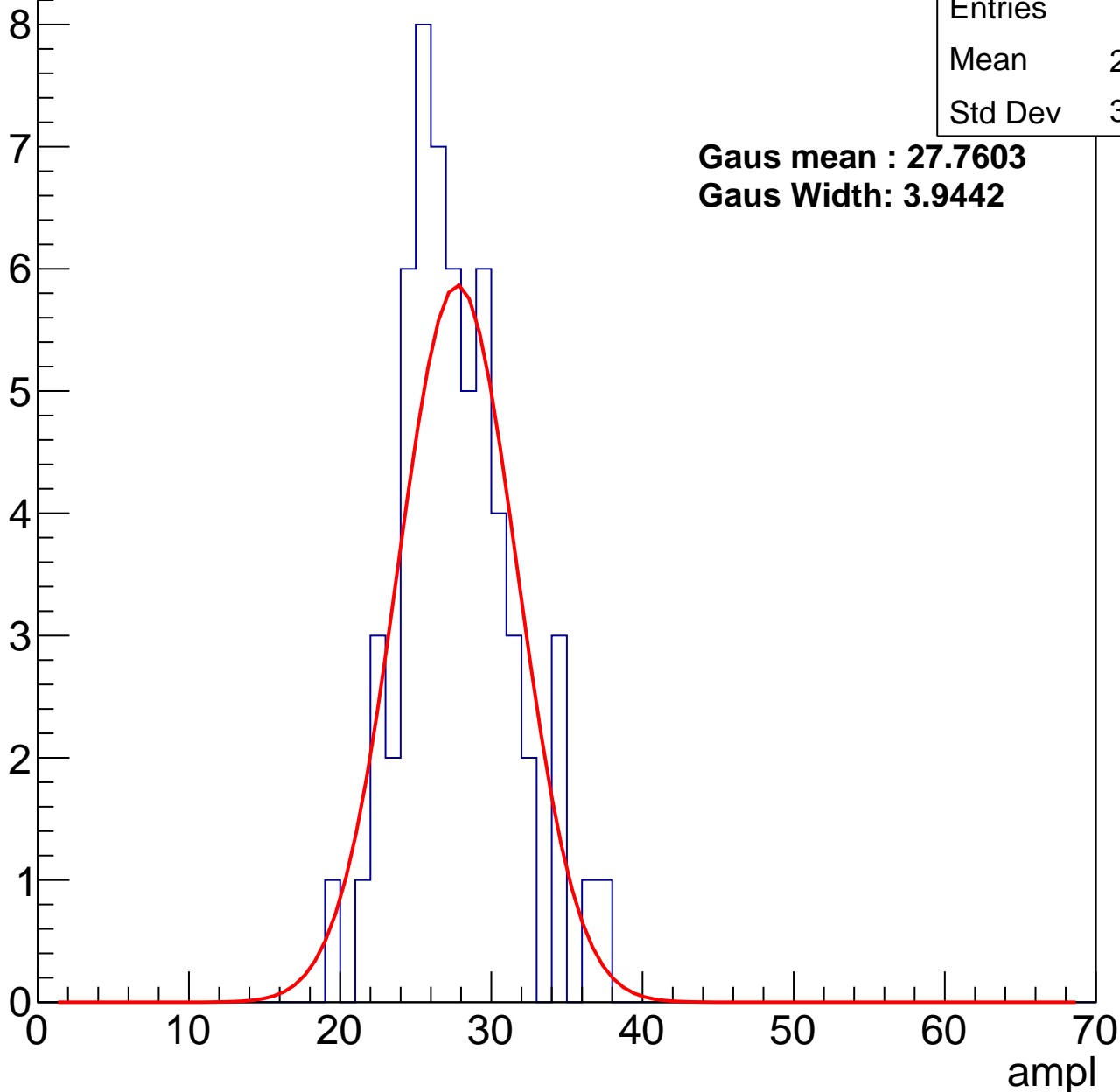
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	27.22
Std Dev	3.655

**Gaus mean : 27.7603**

**Gaus Width: 3.9442**



# B1L103S, U26-ch58, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	85
Mean	34.19
Std Dev	4.216

**Gaus mean : 34.4157**

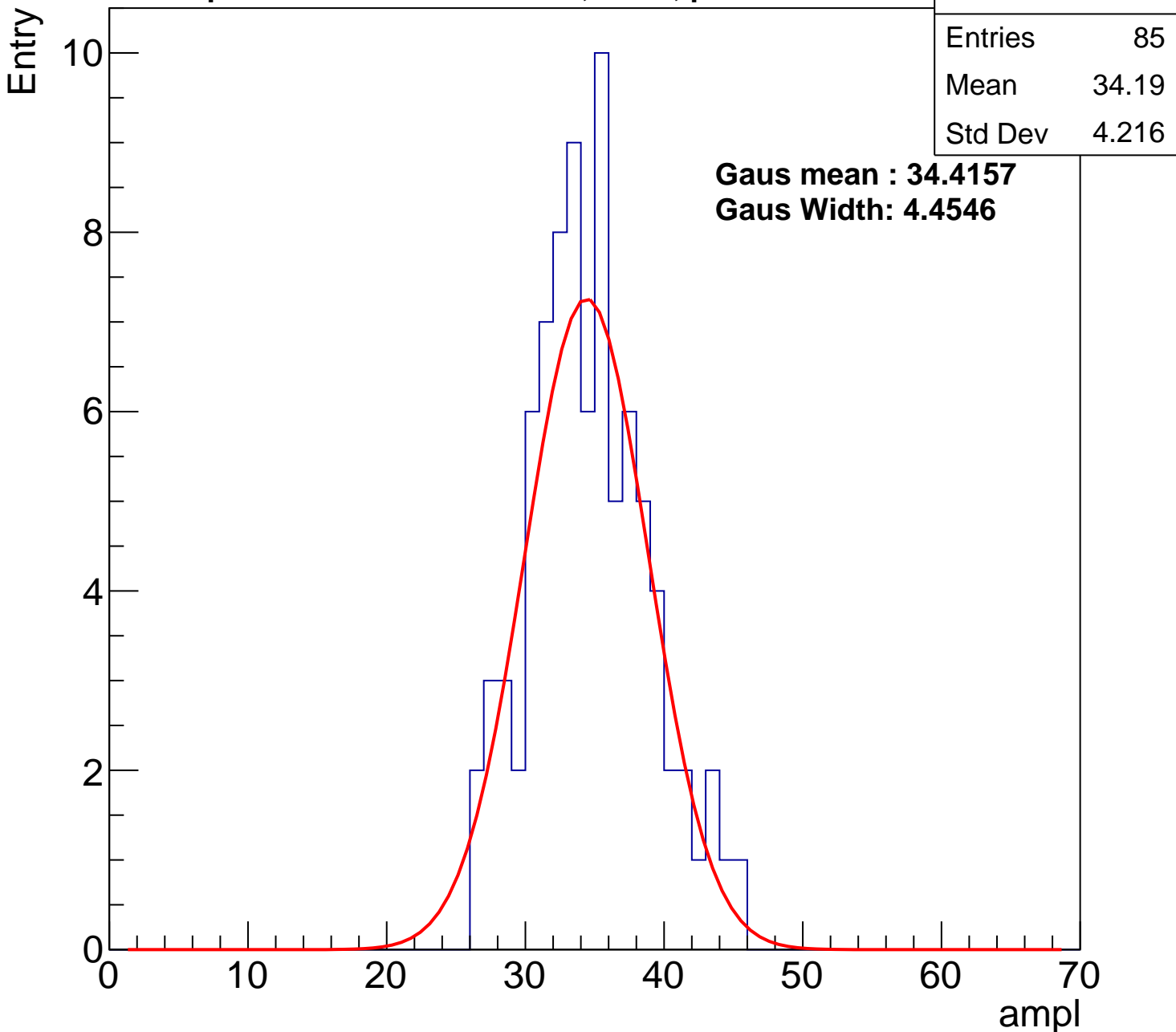
**Gaus Width: 4.4546**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch58, adc2

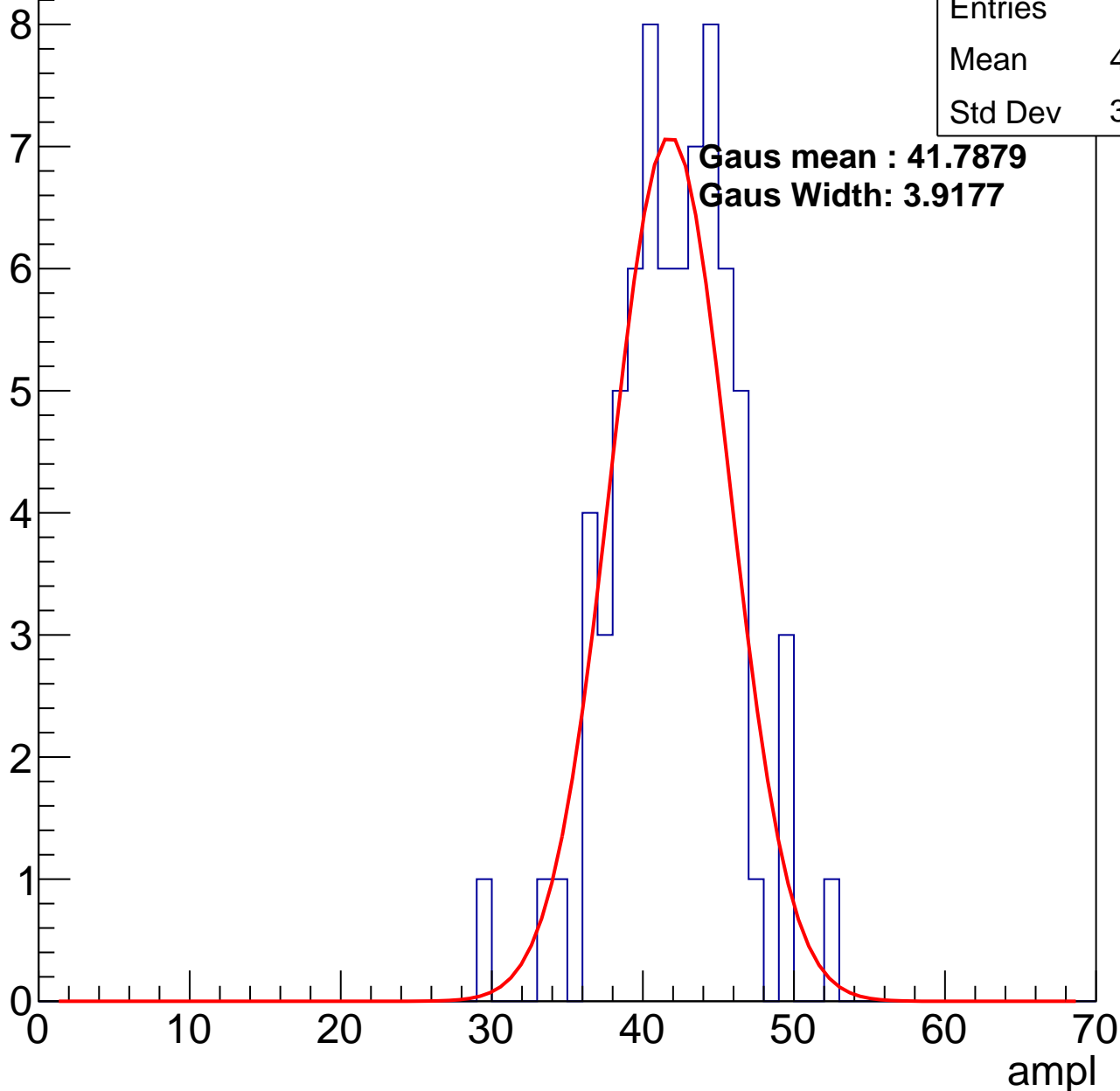
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	41.56
Std Dev	3.972

**Gaus mean : 41.7879**

**Gaus Width: 3.9177**

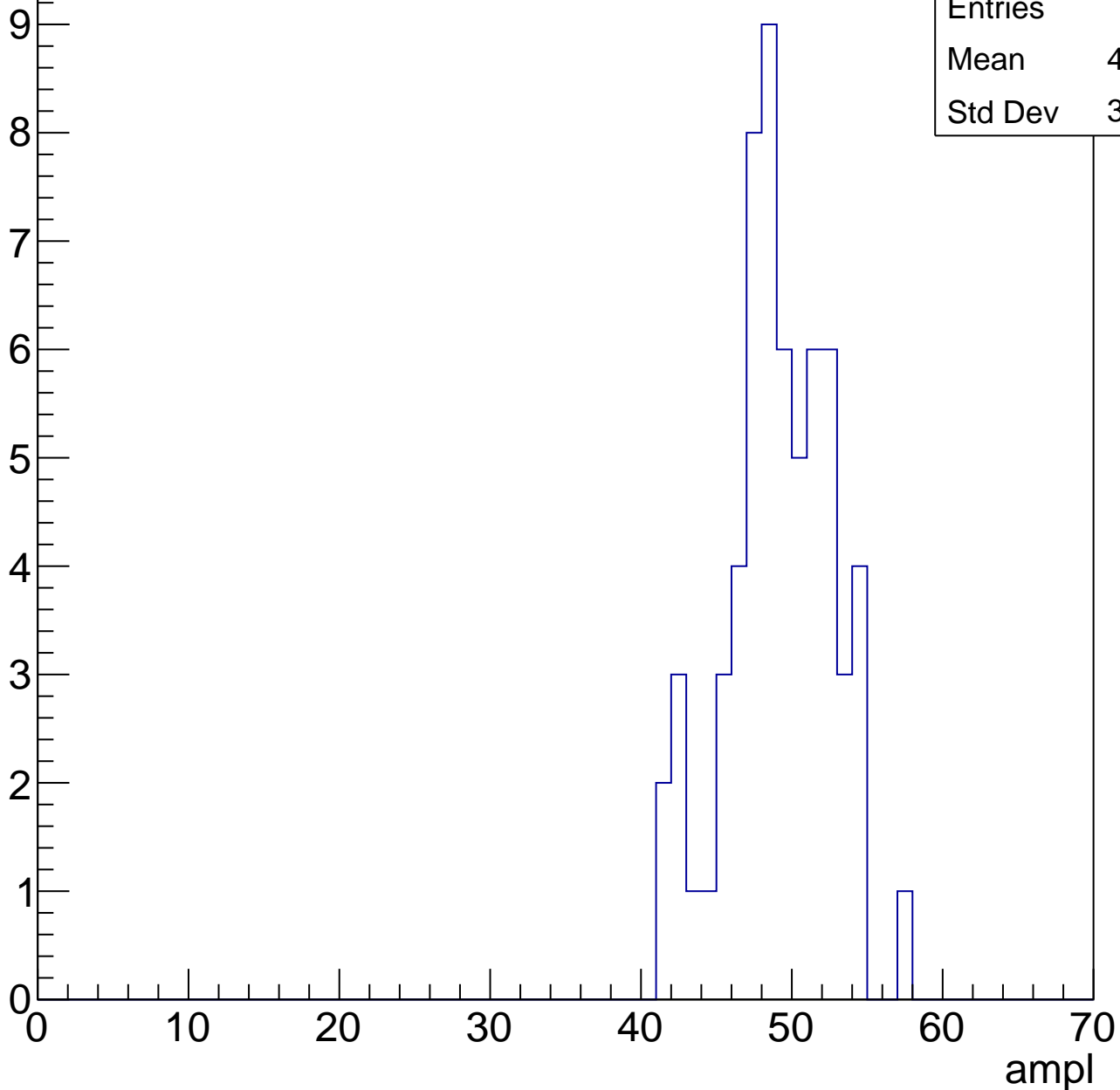


# B1L103S, U26-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

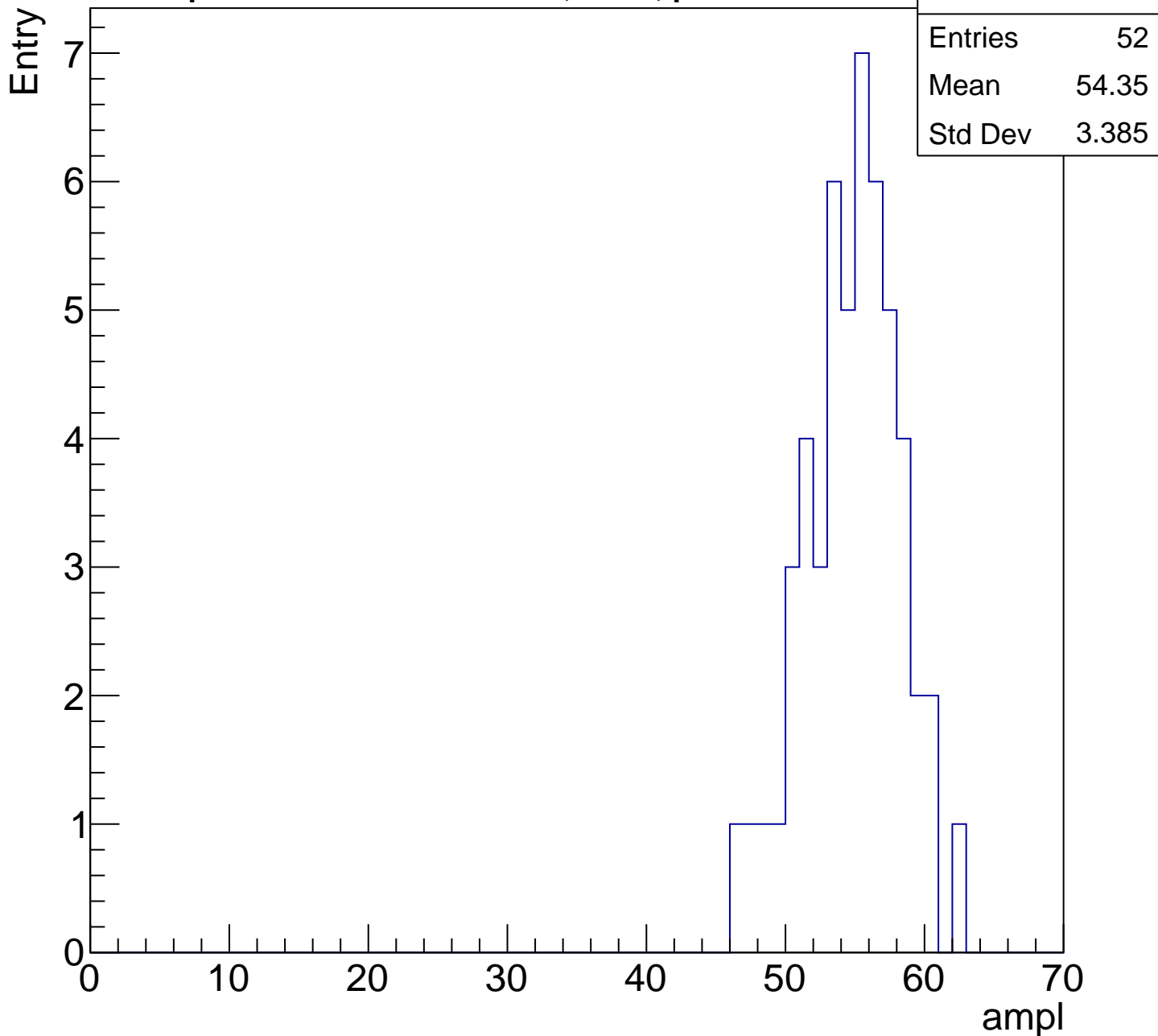
Entry

Entries	62
Mean	48.65
Std Dev	3.474



# B1L103S, U26-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

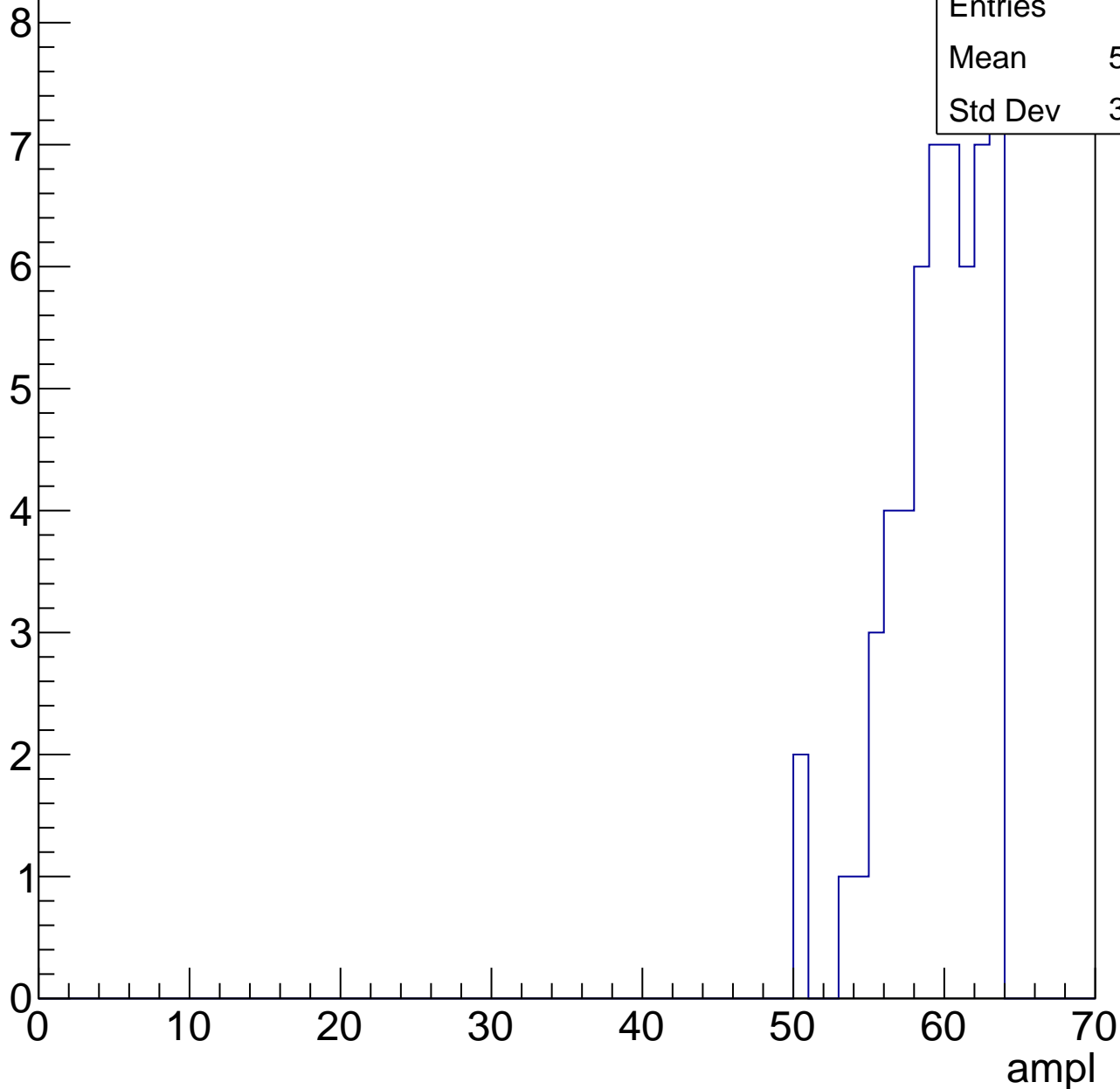


# B1L103S, U26-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

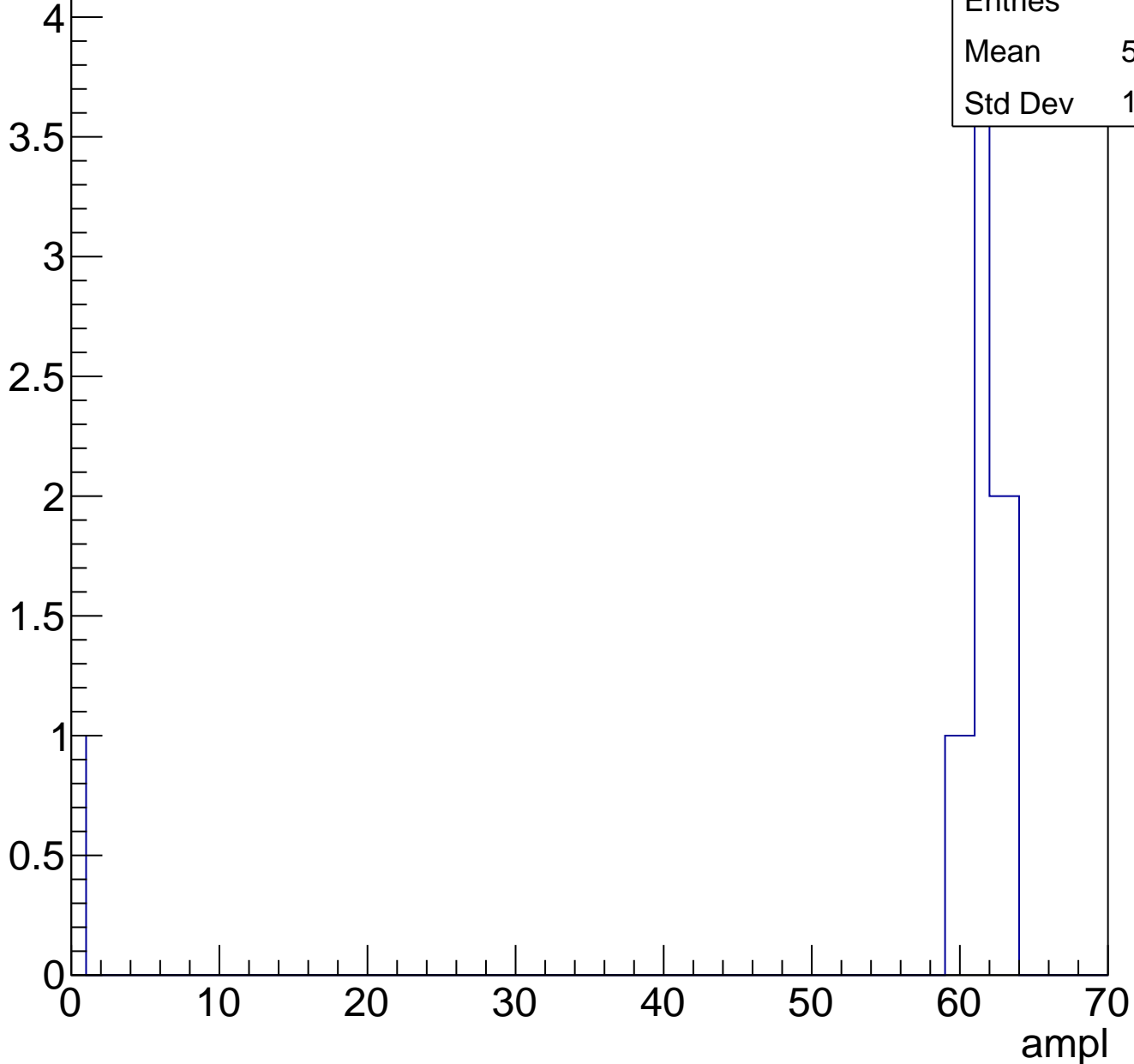
Entries	56
Mean	59.09
Std Dev	3.135



# B1L103S, U26-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U26-ch59, adc0

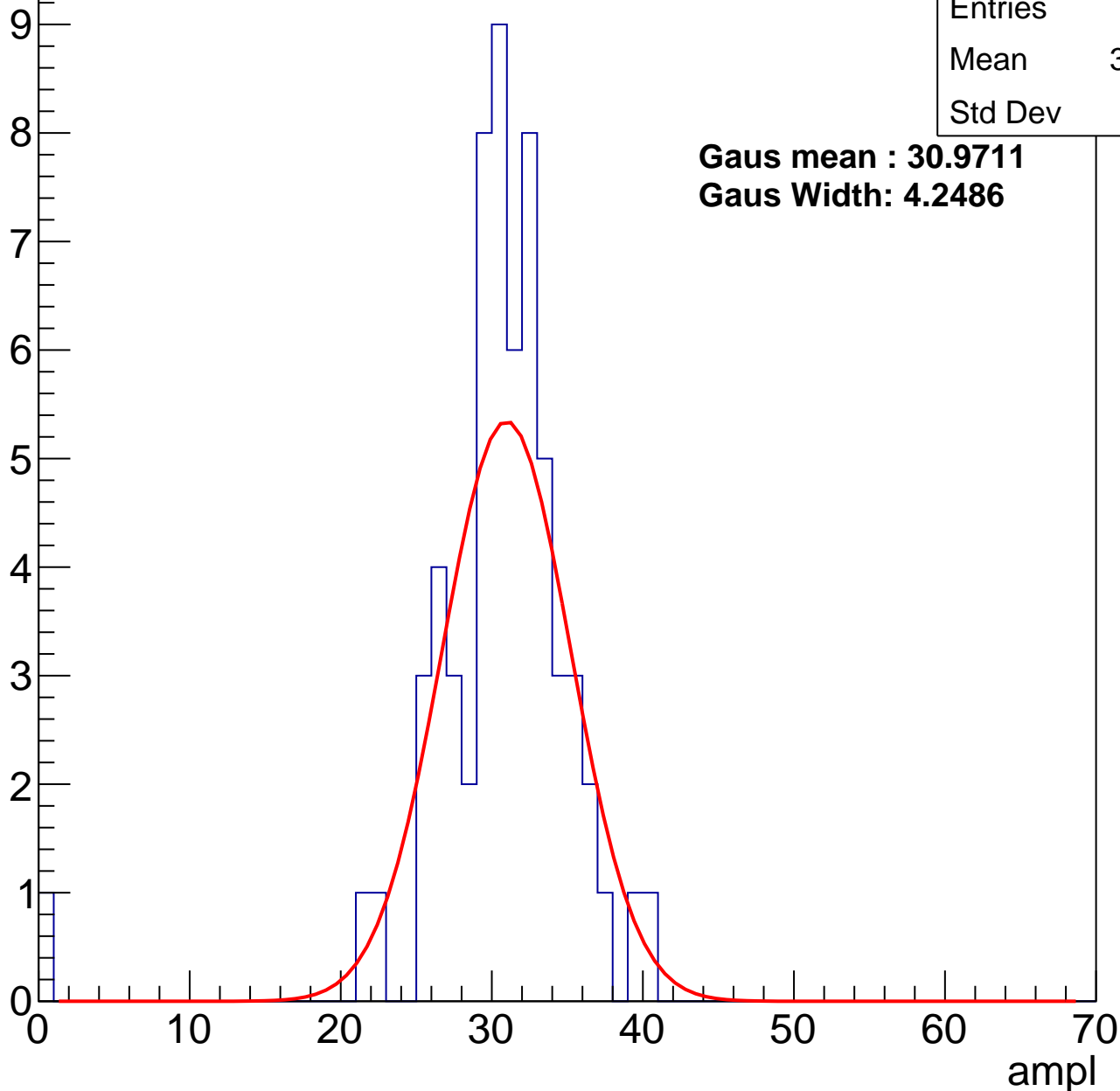
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	30.05
Std Dev	5.29

**Gaus mean : 30.9711**

**Gaus Width: 4.2486**



# B1L103S, U26-ch59, adc1

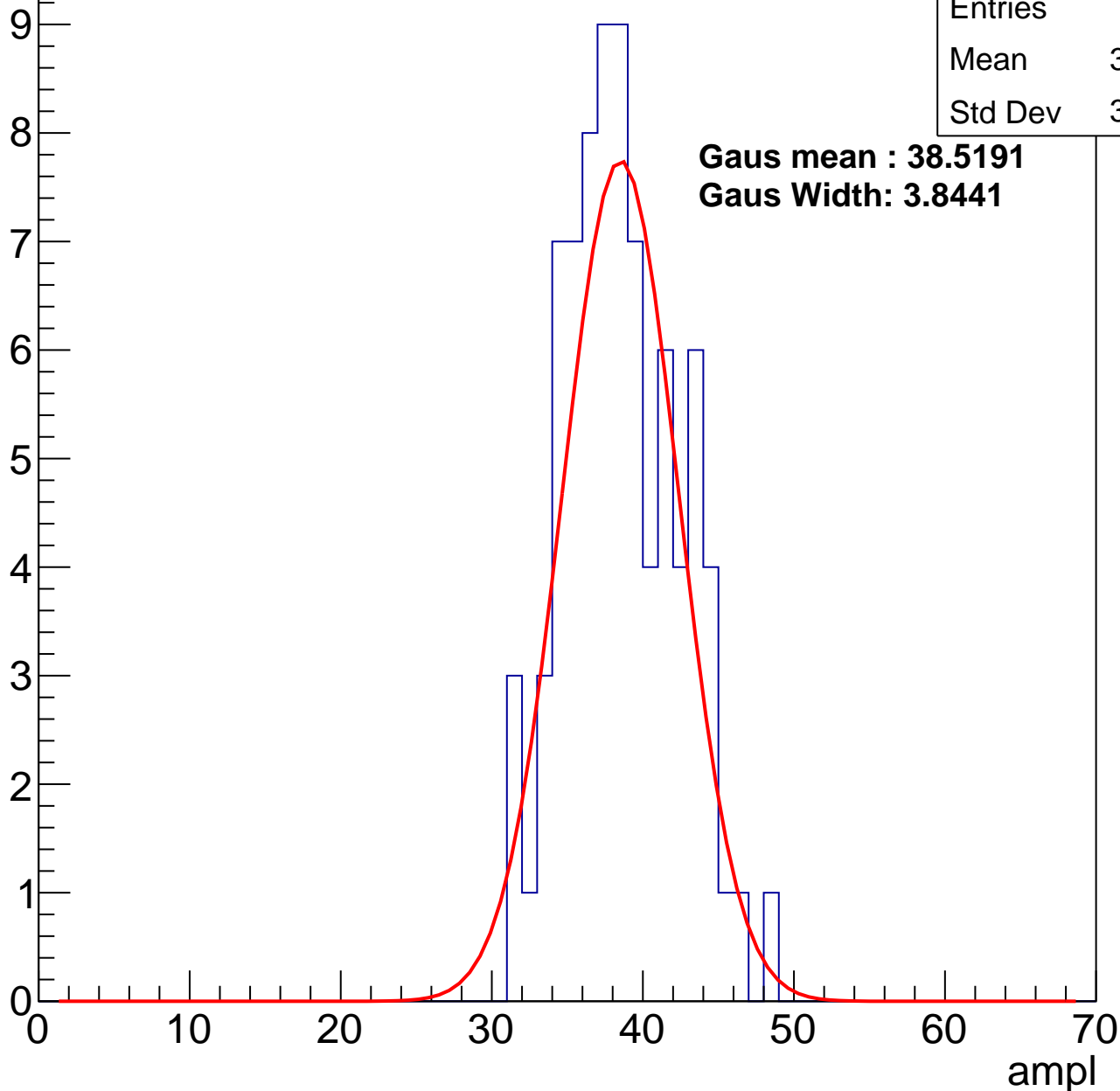
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	81
Mean	38.15
Std Dev	3.719

**Gaus mean : 38.5191**

**Gaus Width: 3.8441**



# B1L103S, U26-ch59, adc2

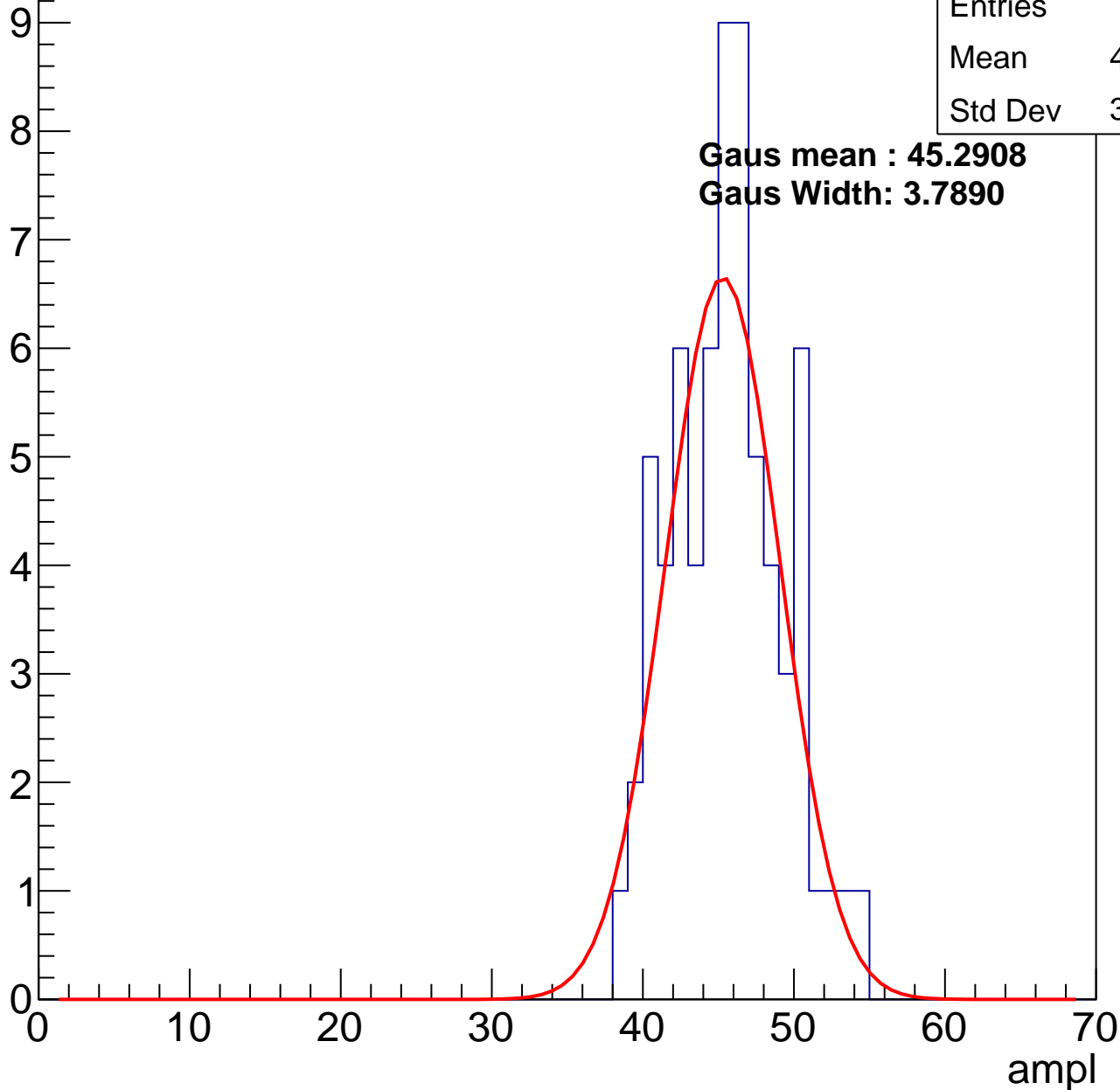
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	45.16
Std Dev	3.592

**Gaus mean : 45.2908**

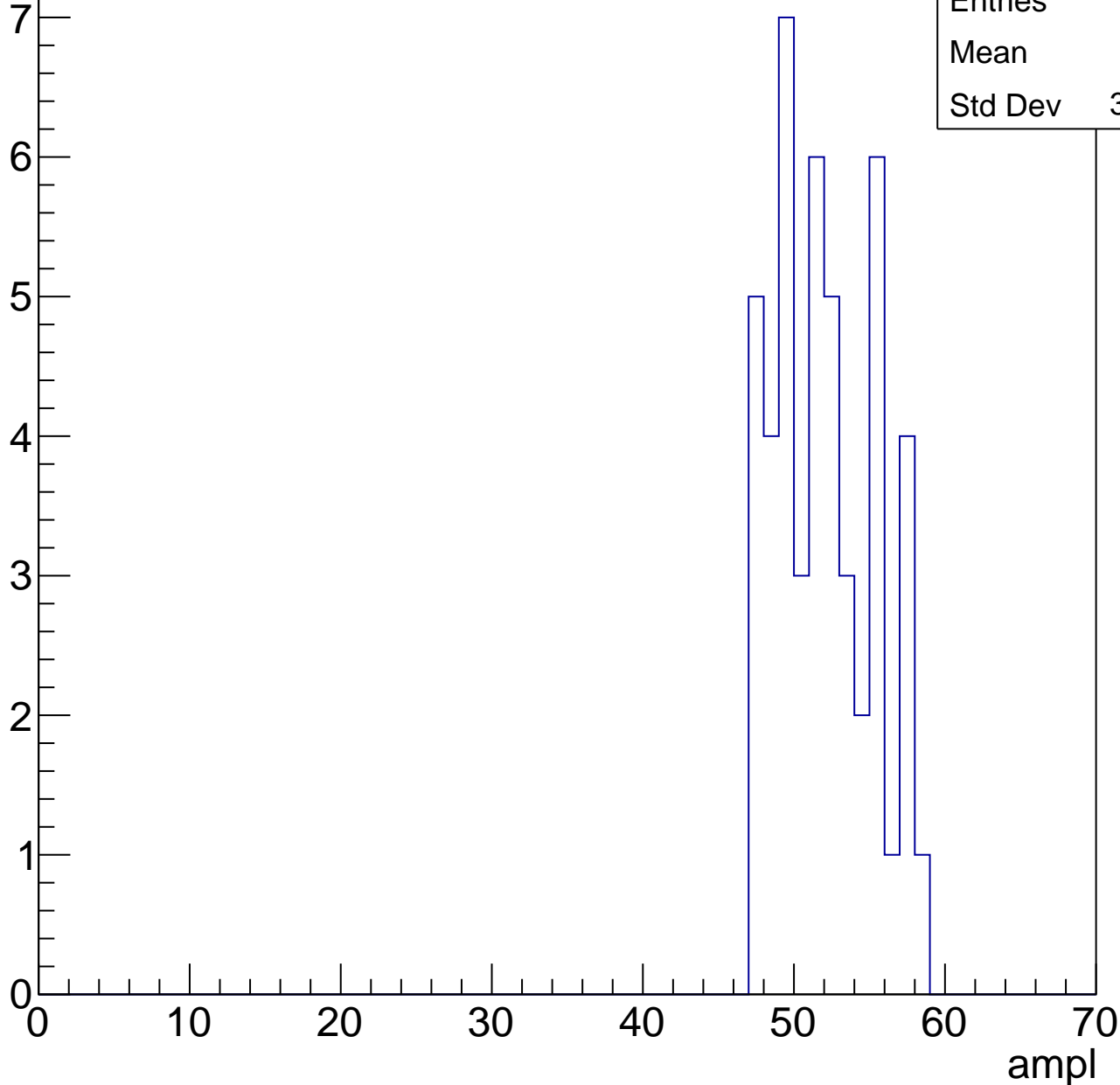
**Gaus Width: 3.7890**



# B1L103S, U26-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

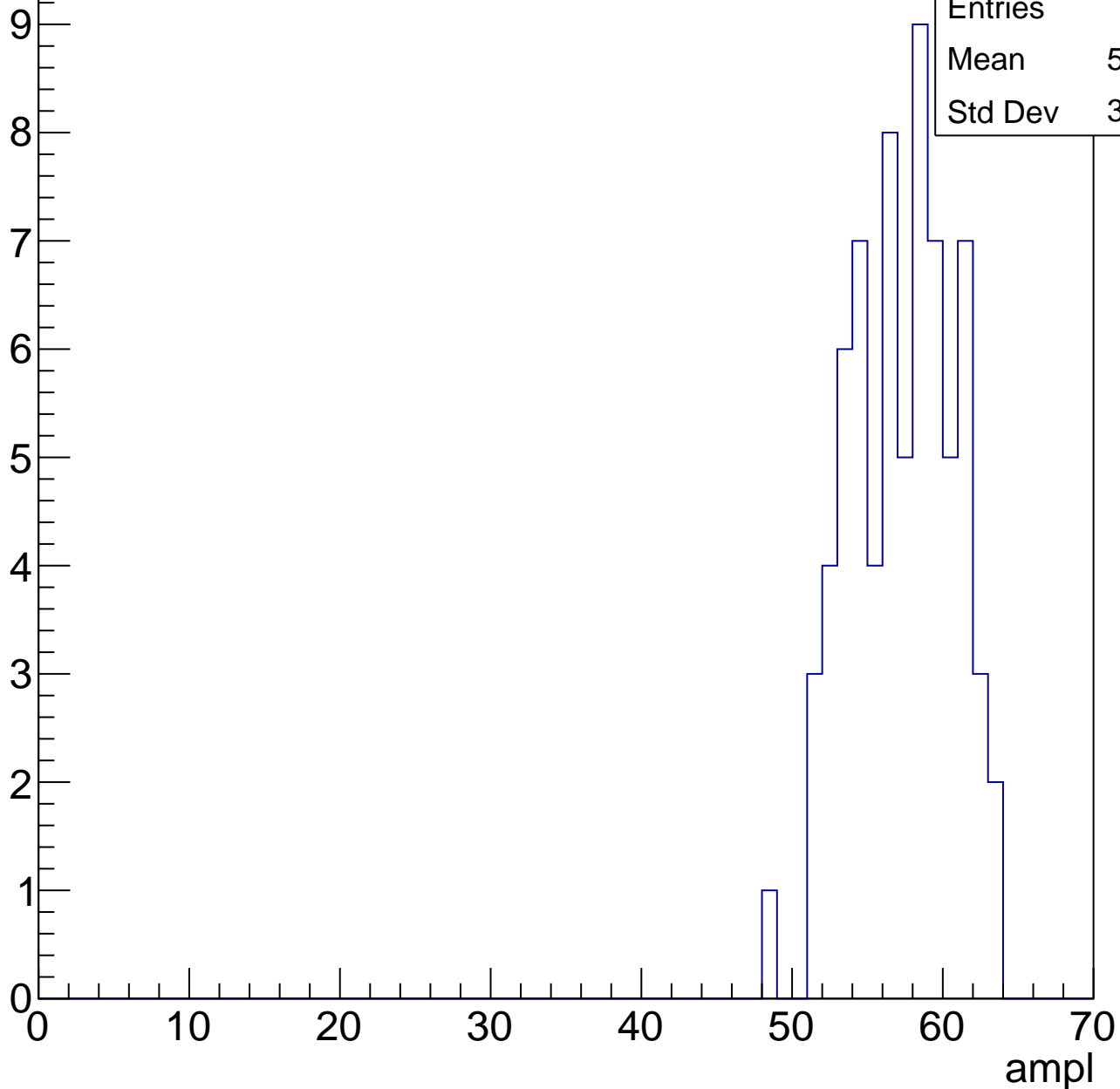


# B1L103S, U26-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	56.79
Std Dev	3.377

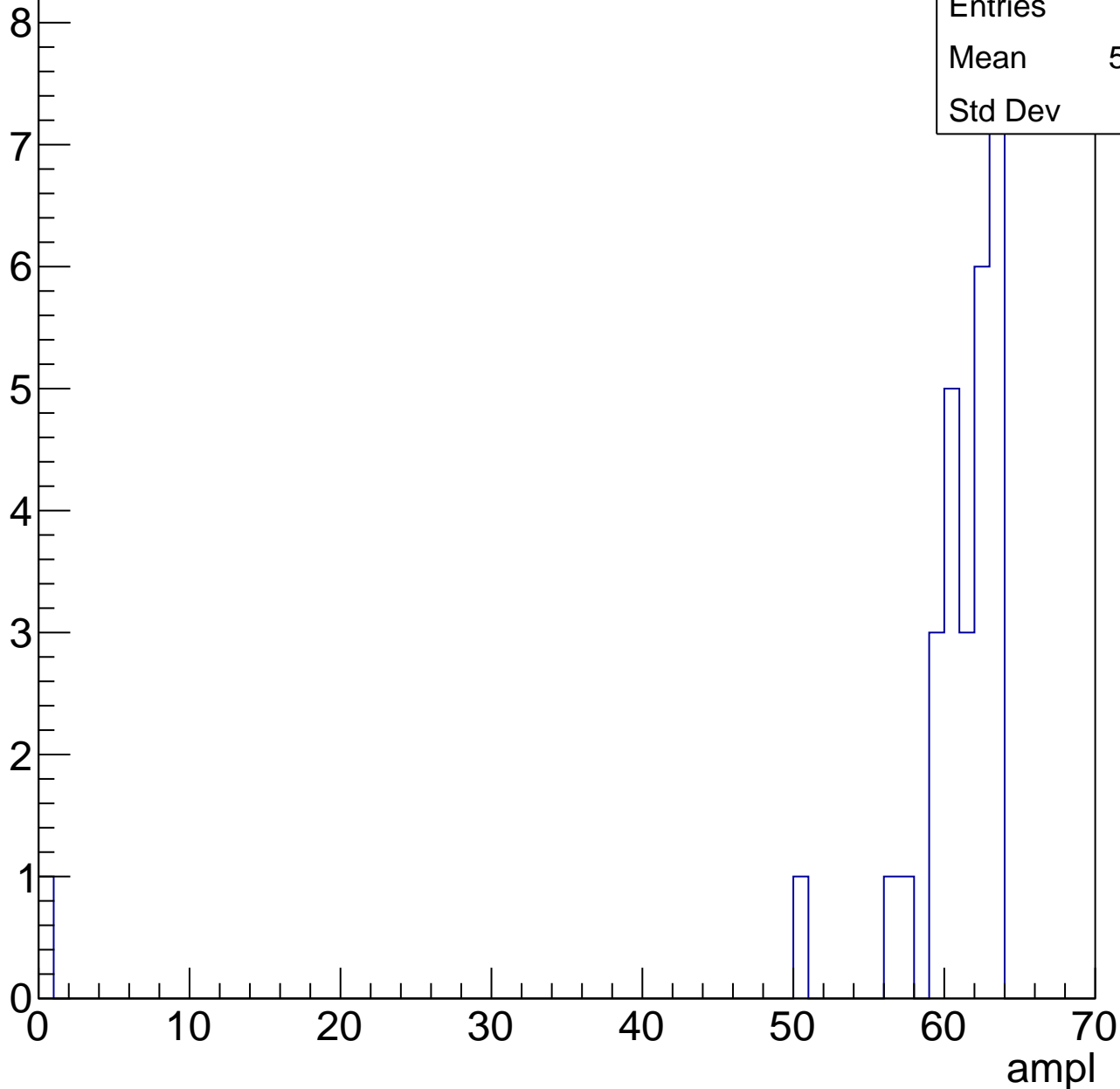


# B1L103S, U26-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	29
Mean	58.59
Std Dev	11.4



# B1L103S, U26-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U26-ch60, adc0

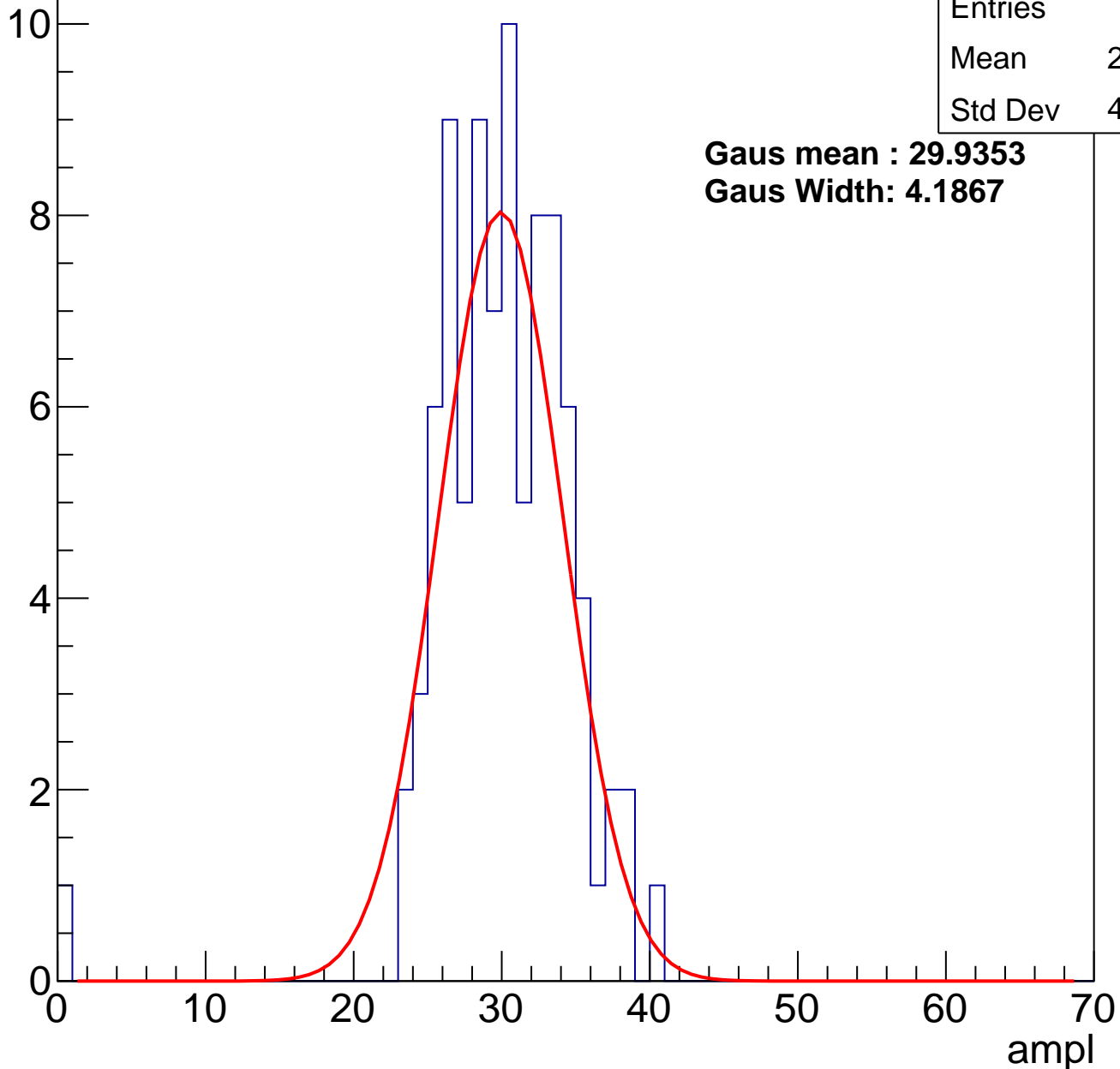
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	89
Mean	29.63
Std Dev	4.907

**Gaus mean : 29.9353**

**Gaus Width: 4.1867**

Entry



# B1L103S, U26-ch60, adc1

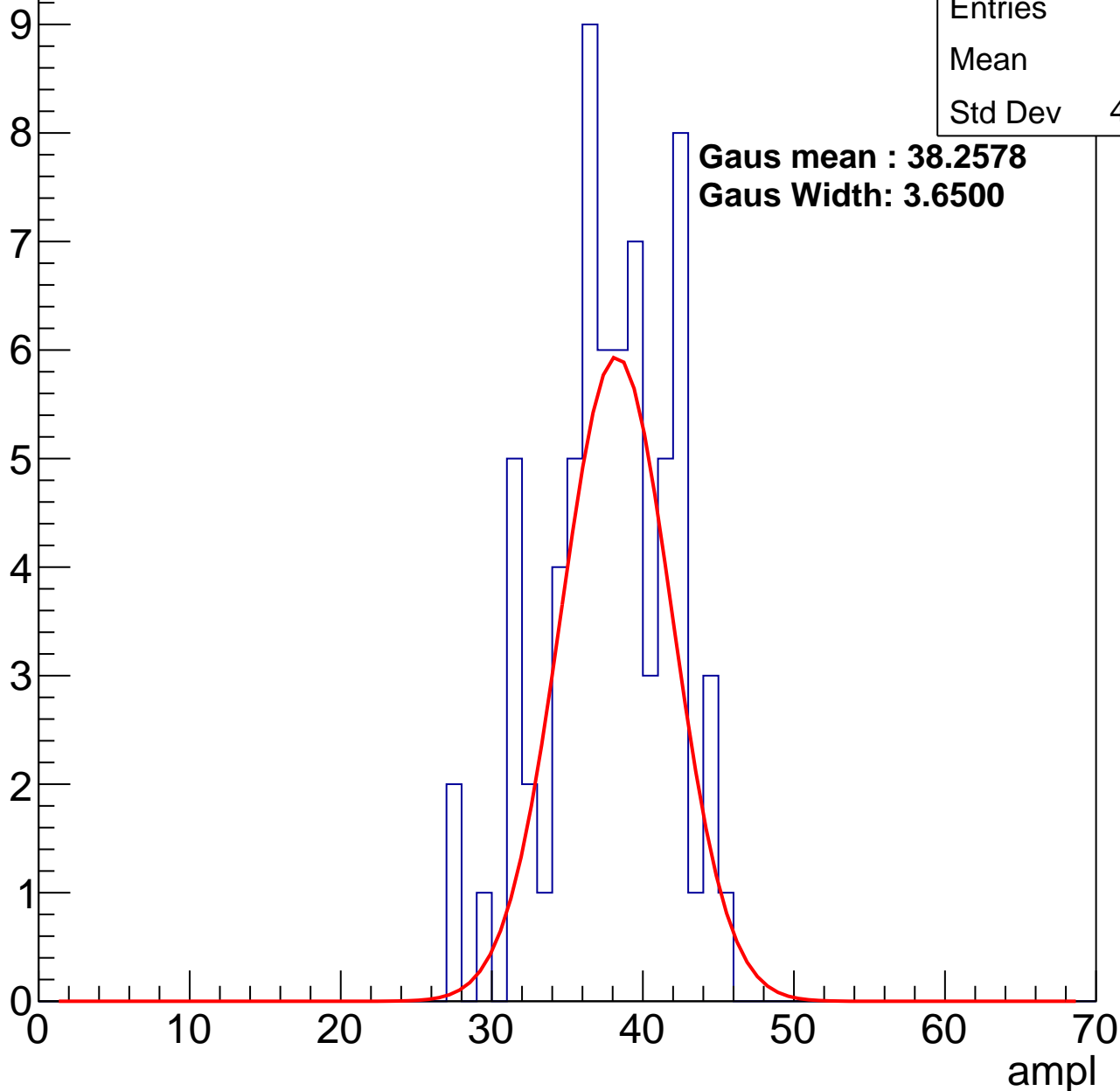
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	37.3
Std Dev	4.094

**Gaus mean : 38.2578**

**Gaus Width: 3.6500**



# B1L103S, U26-ch60, adc2

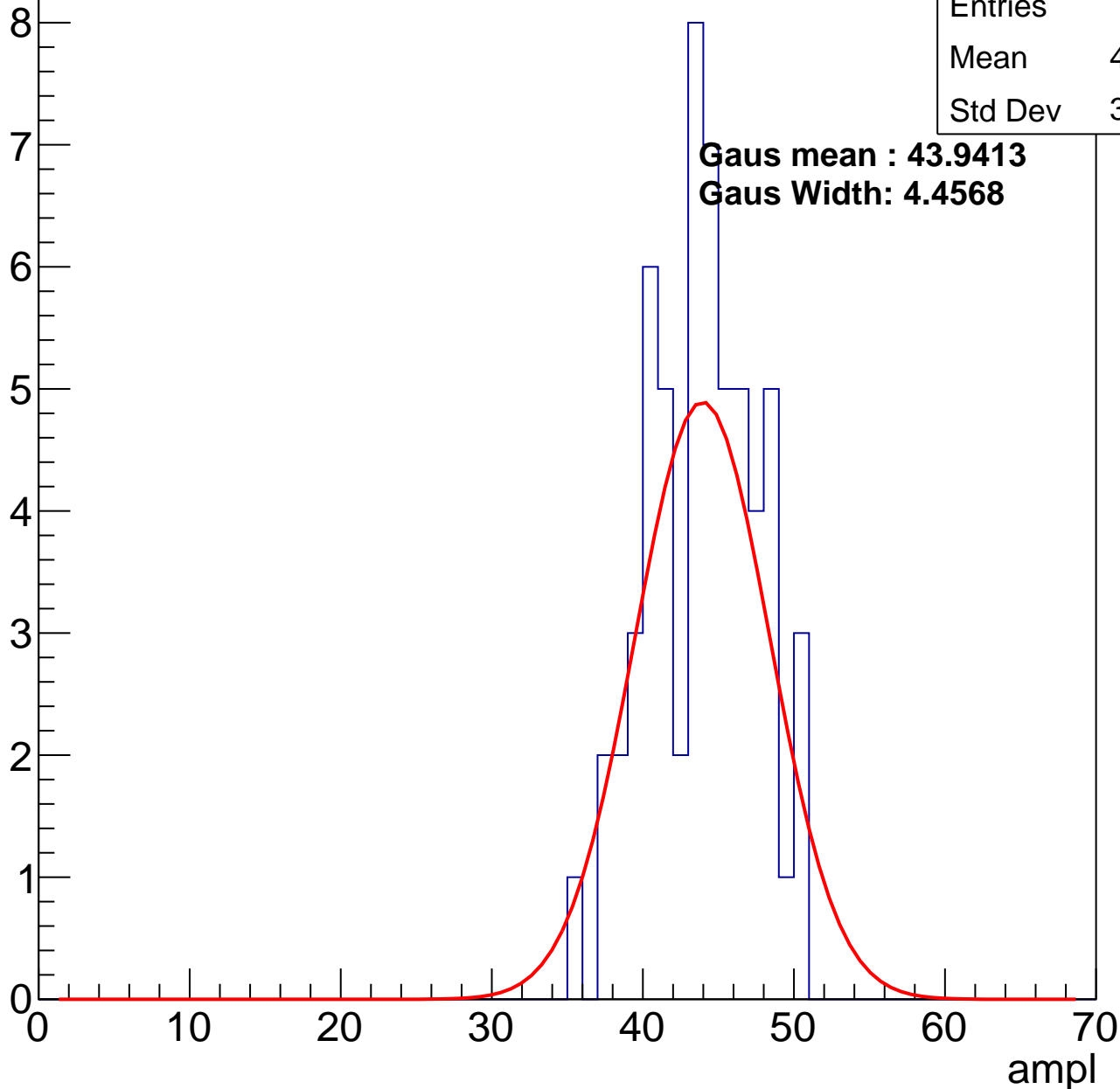
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	43.47
Std Dev	3.543

**Gaus mean : 43.9413**

**Gaus Width: 4.4568**

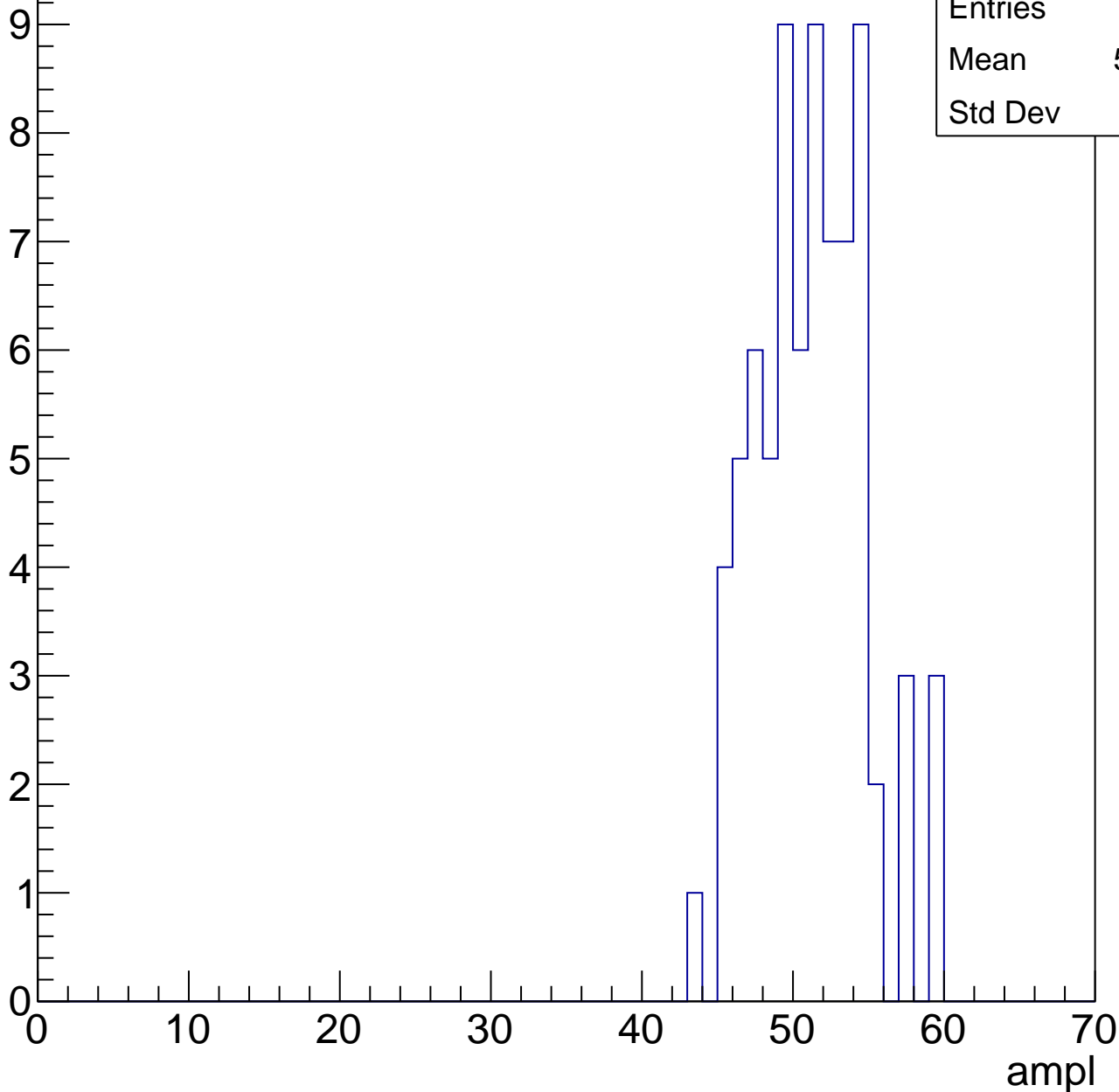


# B1L103S, U26-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	50.71
Std Dev	3.55

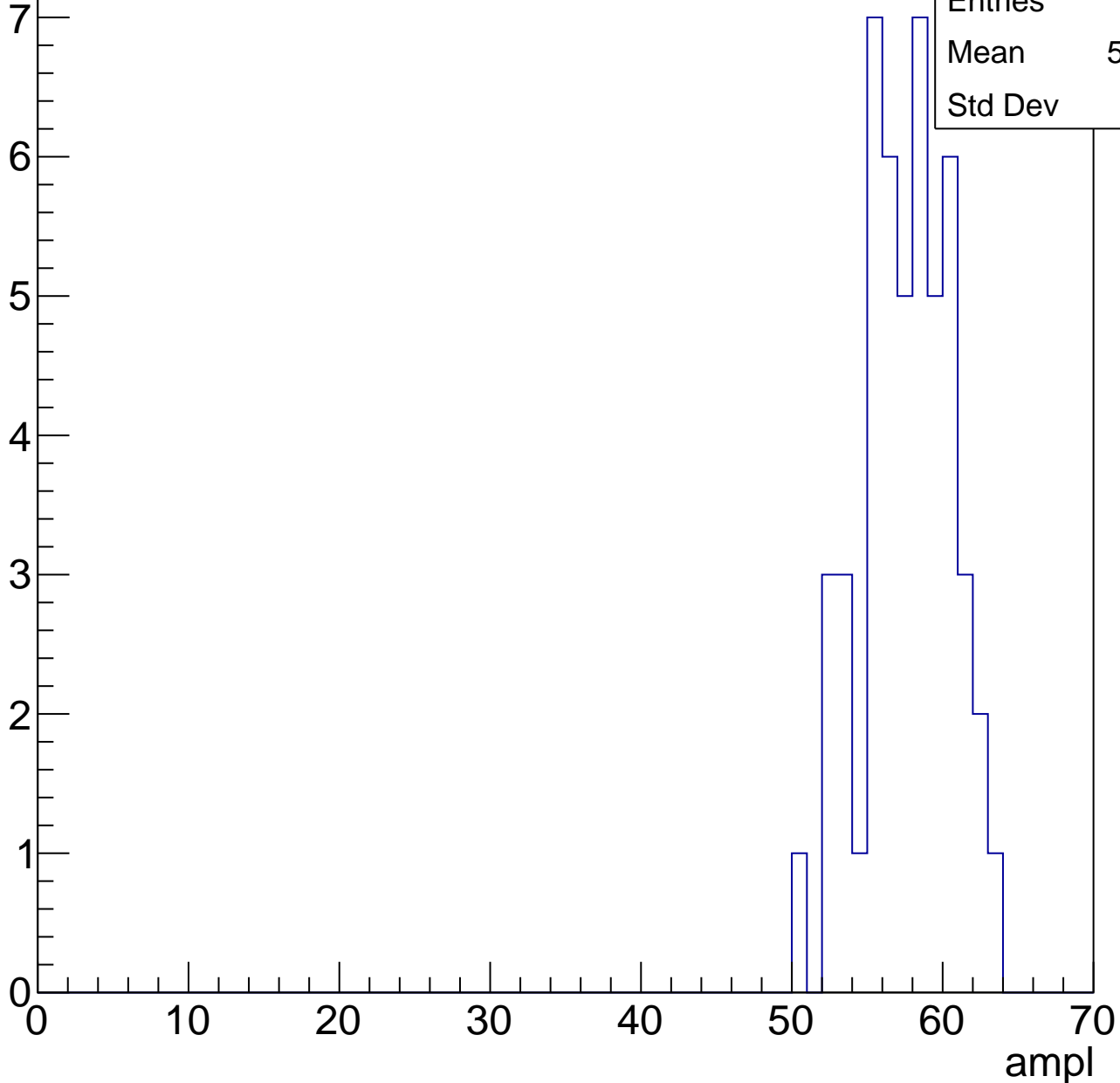


# B1L103S, U26-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	57.12
Std Dev	2.93

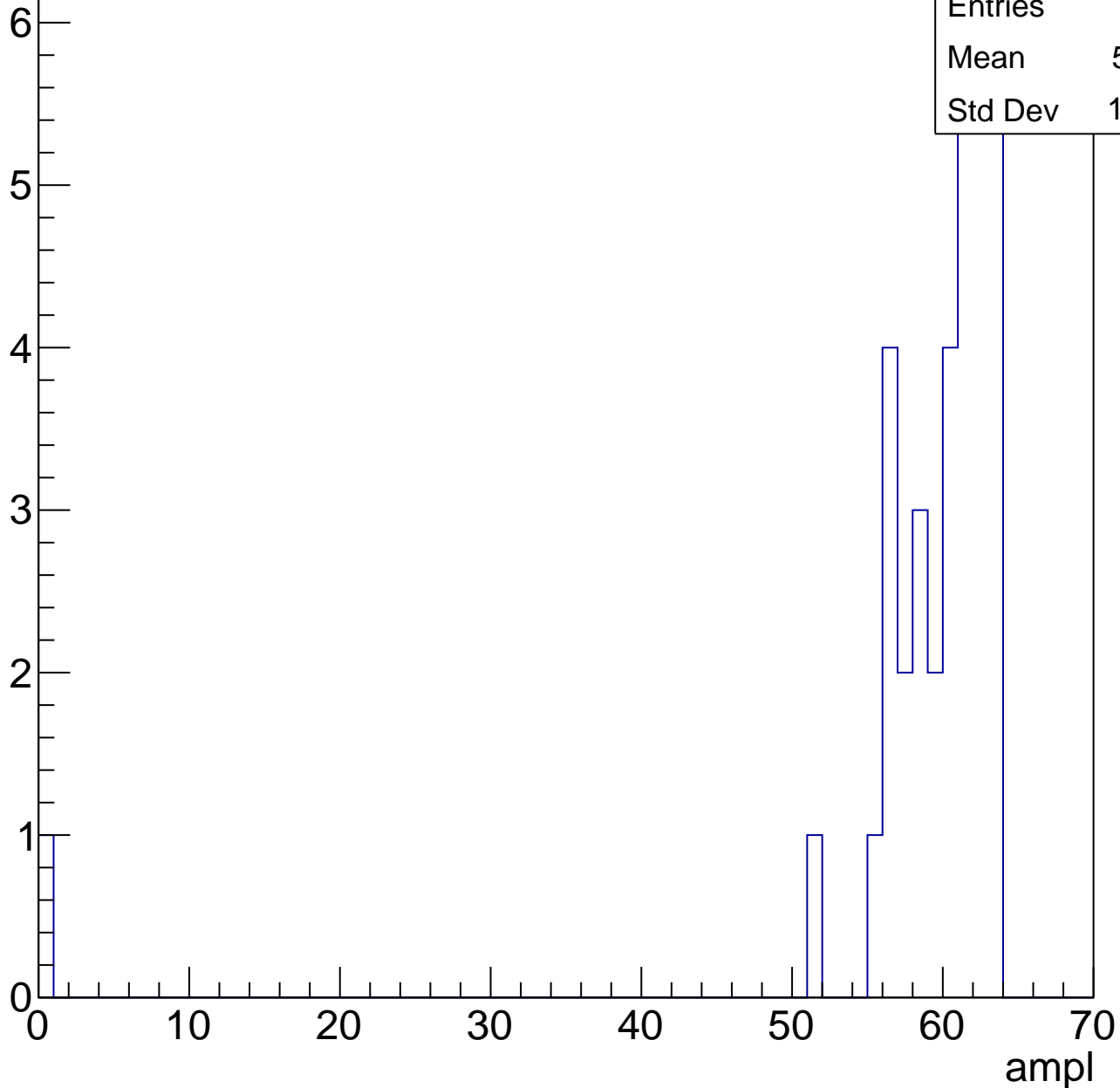


# B1L103S, U26-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	36
Mean	58.11
Std Dev	10.22



# B1L103S, U26-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

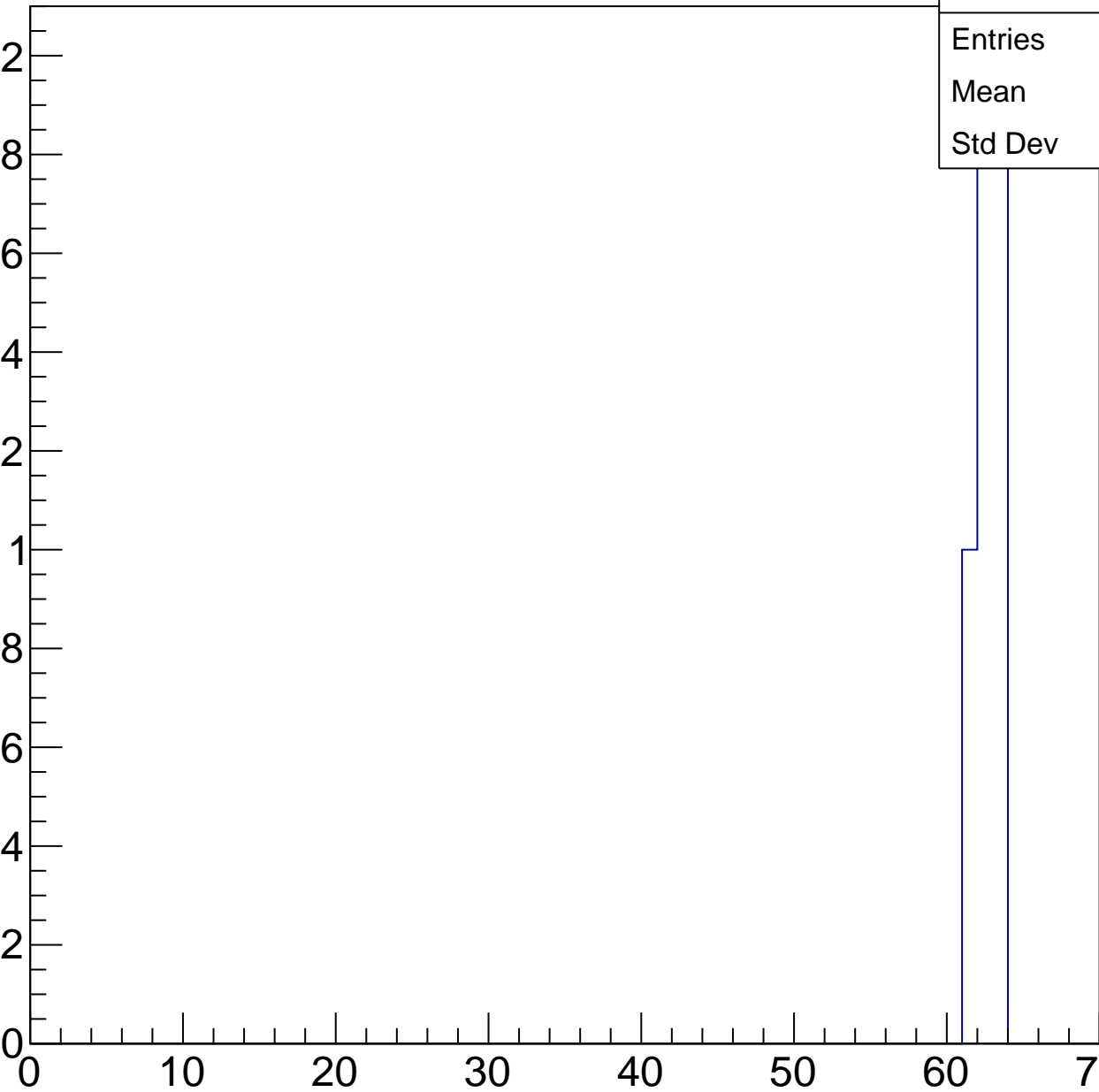
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	62.2
Std Dev	0.7483

0 10 20 30 40 50 60 70

ampl

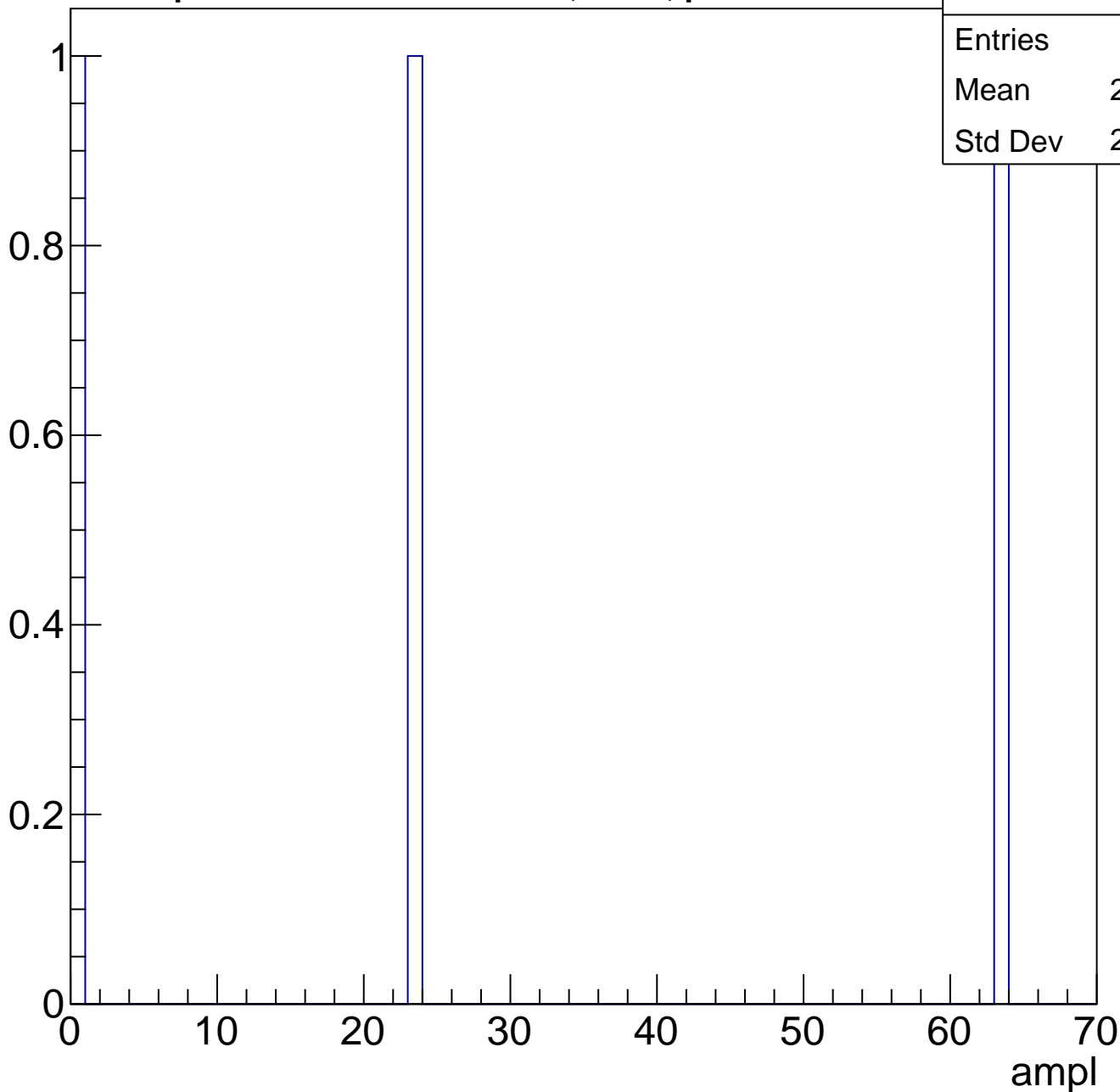




# B1L103S, U26-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	28.67
Std Dev	26.03

# B1L103S, U26-ch61, adc0

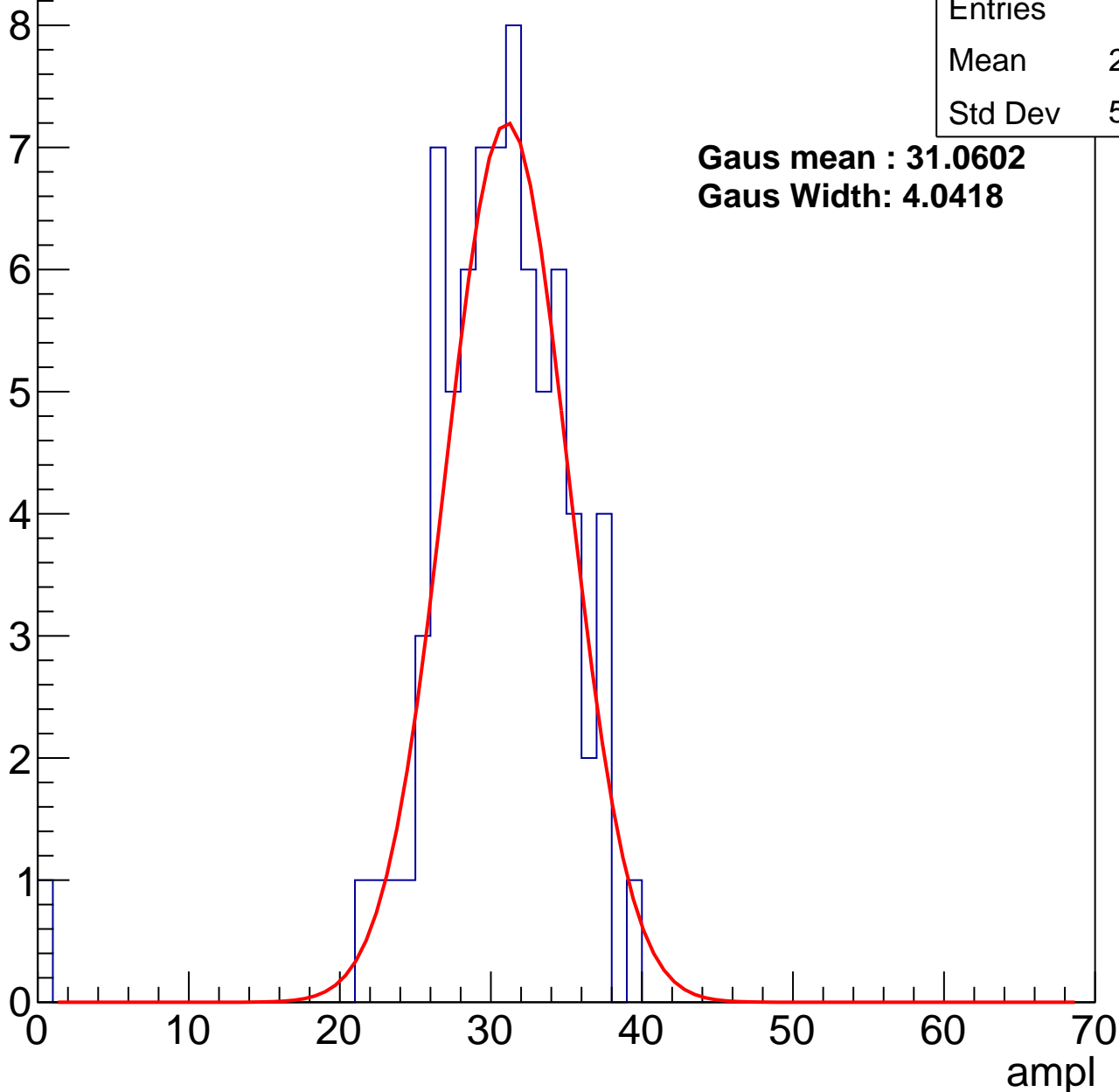
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	29.88
Std Dev	5.148

**Gaus mean : 31.0602**

**Gaus Width: 4.0418**



# B1L103S, U26-ch61, adc1

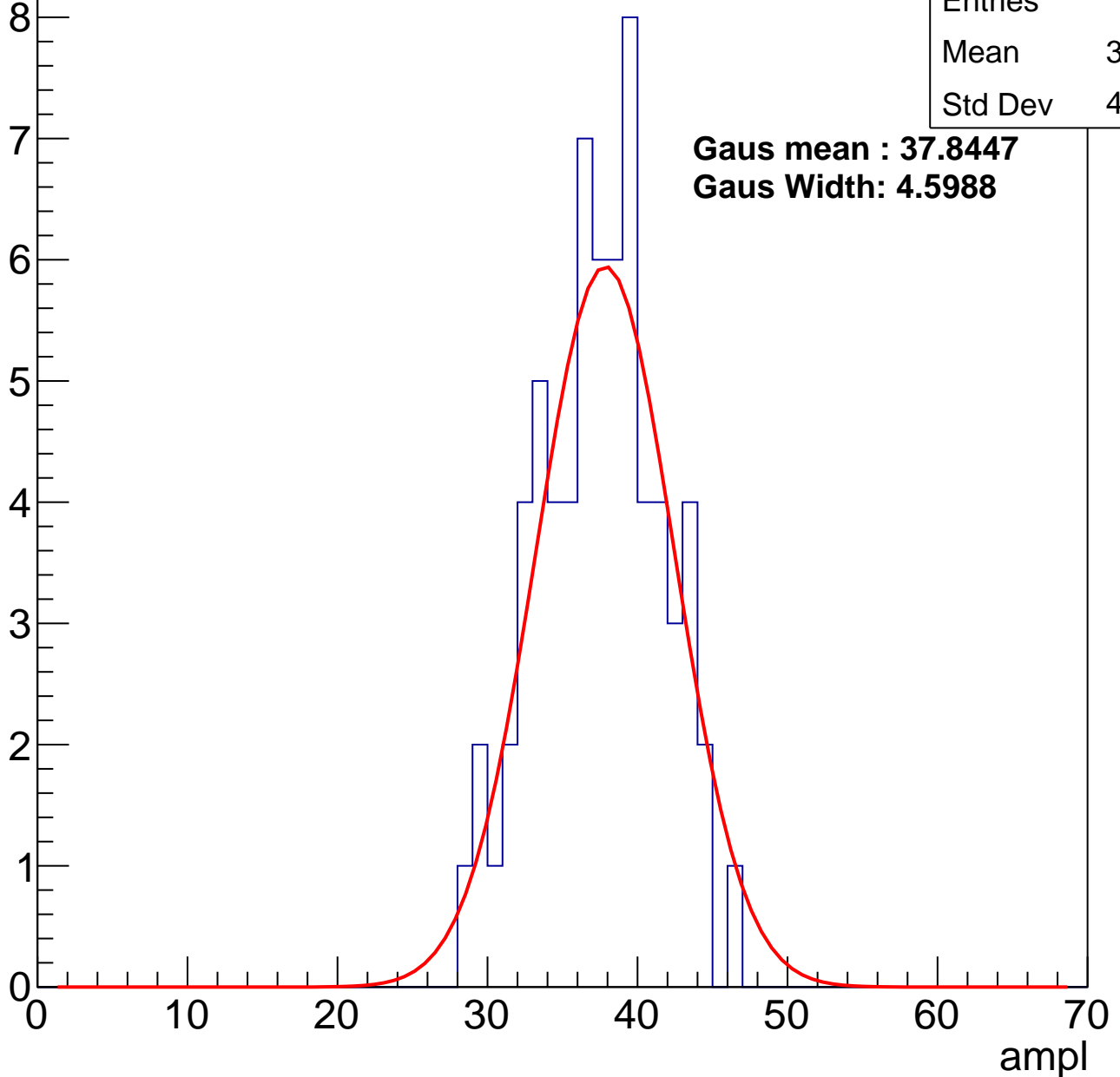
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	37.01
Std Dev	4.031

**Gaus mean : 37.8447**

**Gaus Width: 4.5988**

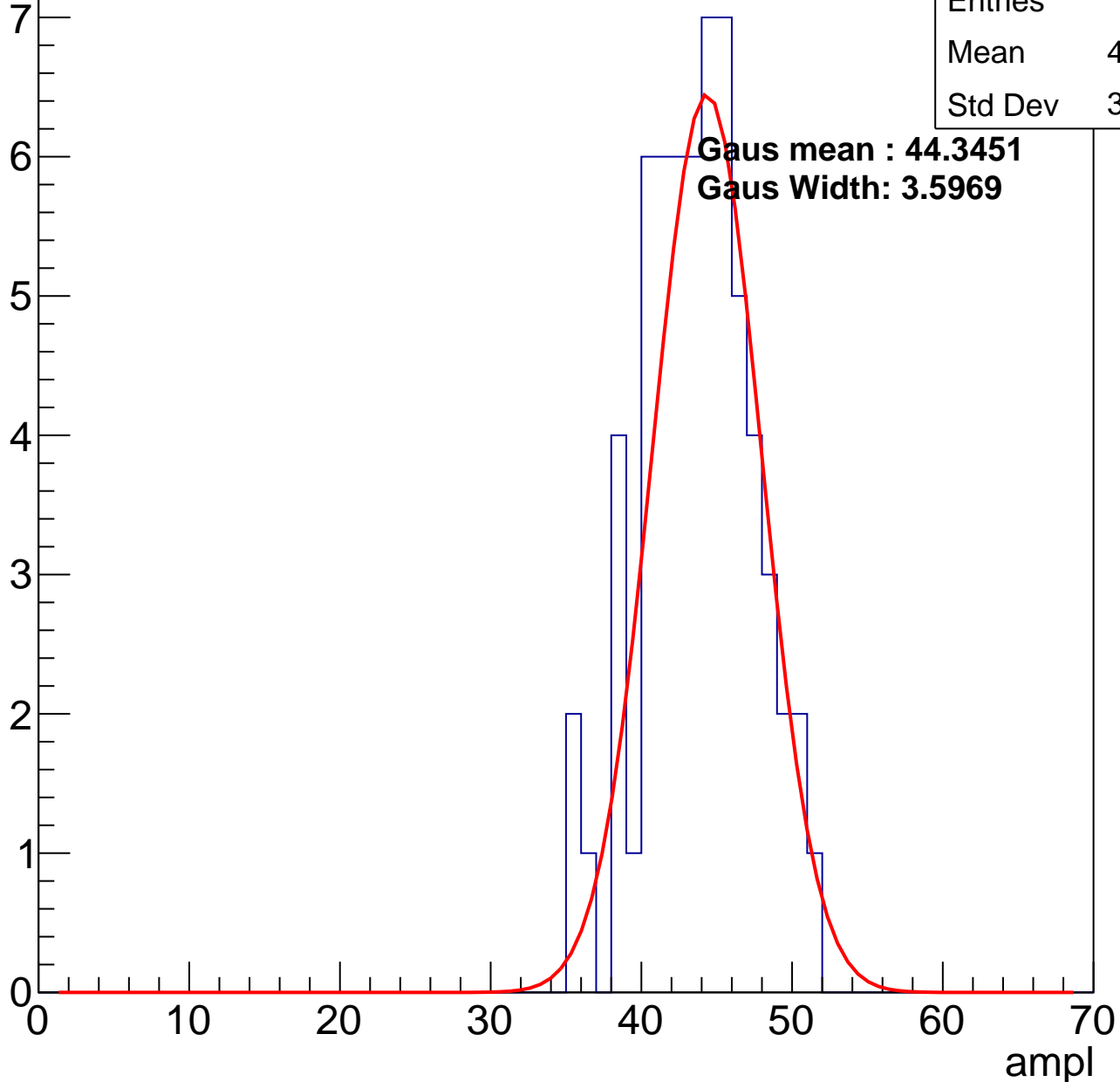


# B1L103S, U26-ch61, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	43.29
Std Dev	3.618

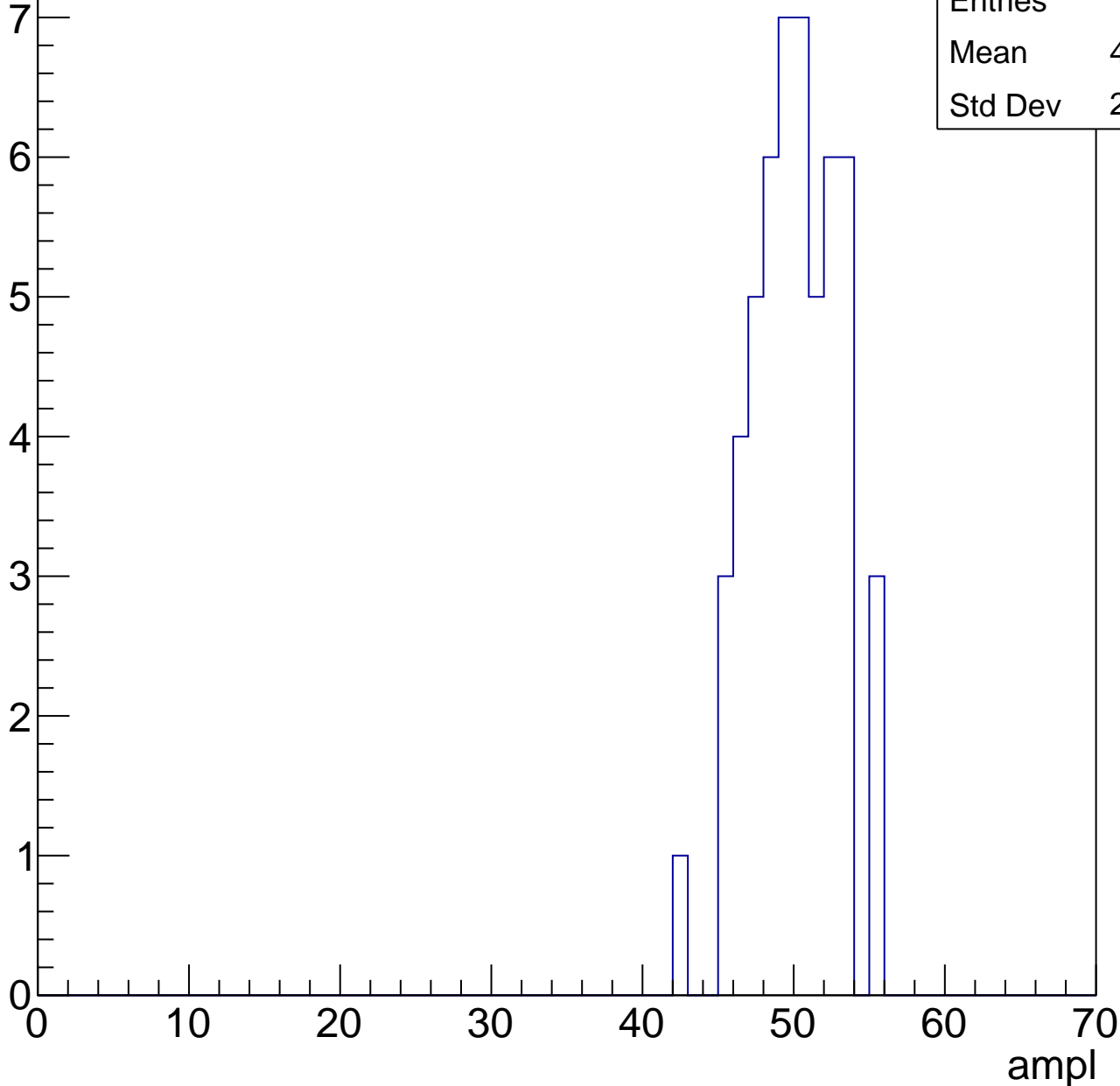


# B1L103S, U26-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	49.57
Std Dev	2.838

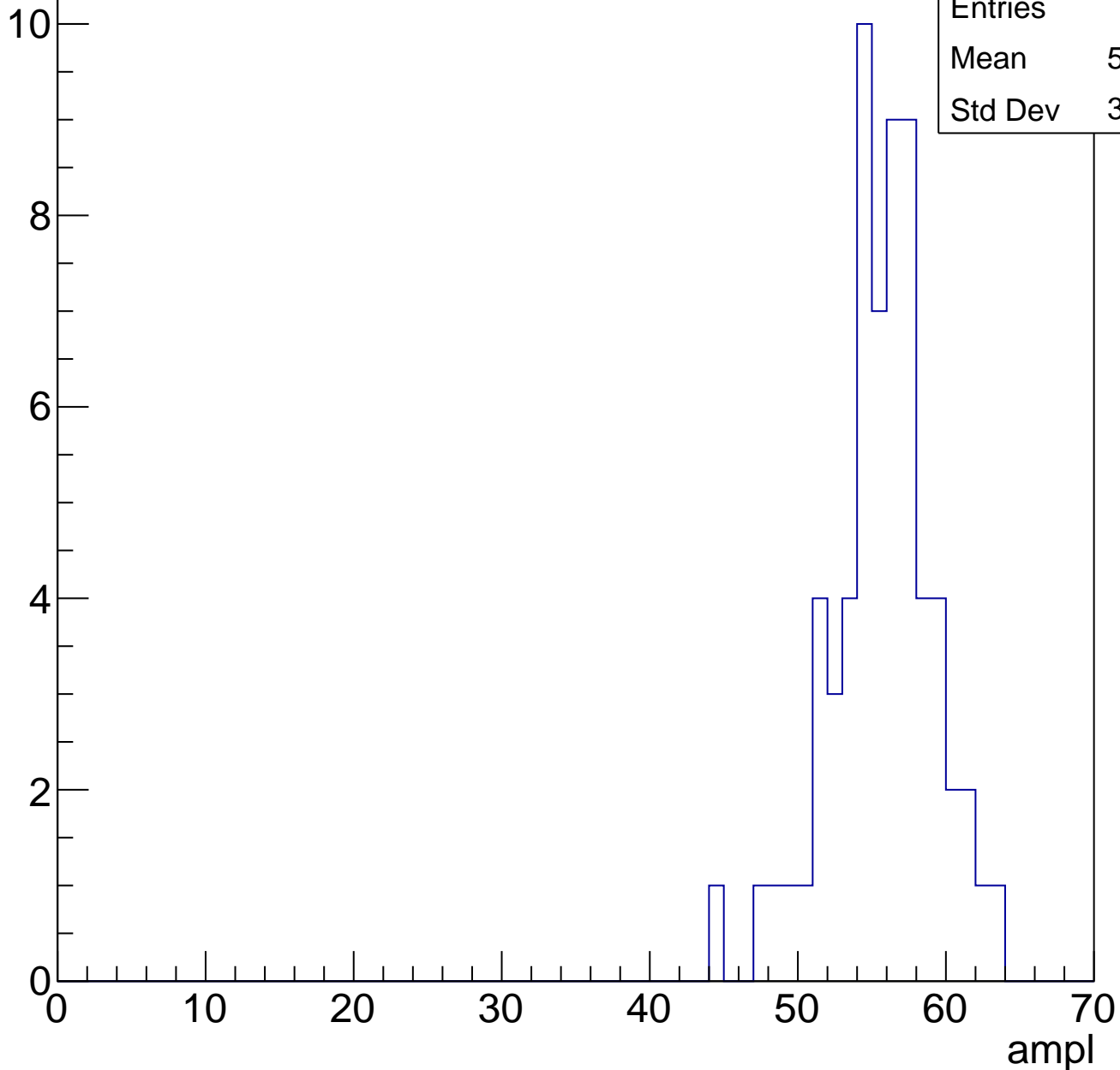


# B1L103S, U26-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	65
Mean	55.18
Std Dev	3.486

Entry

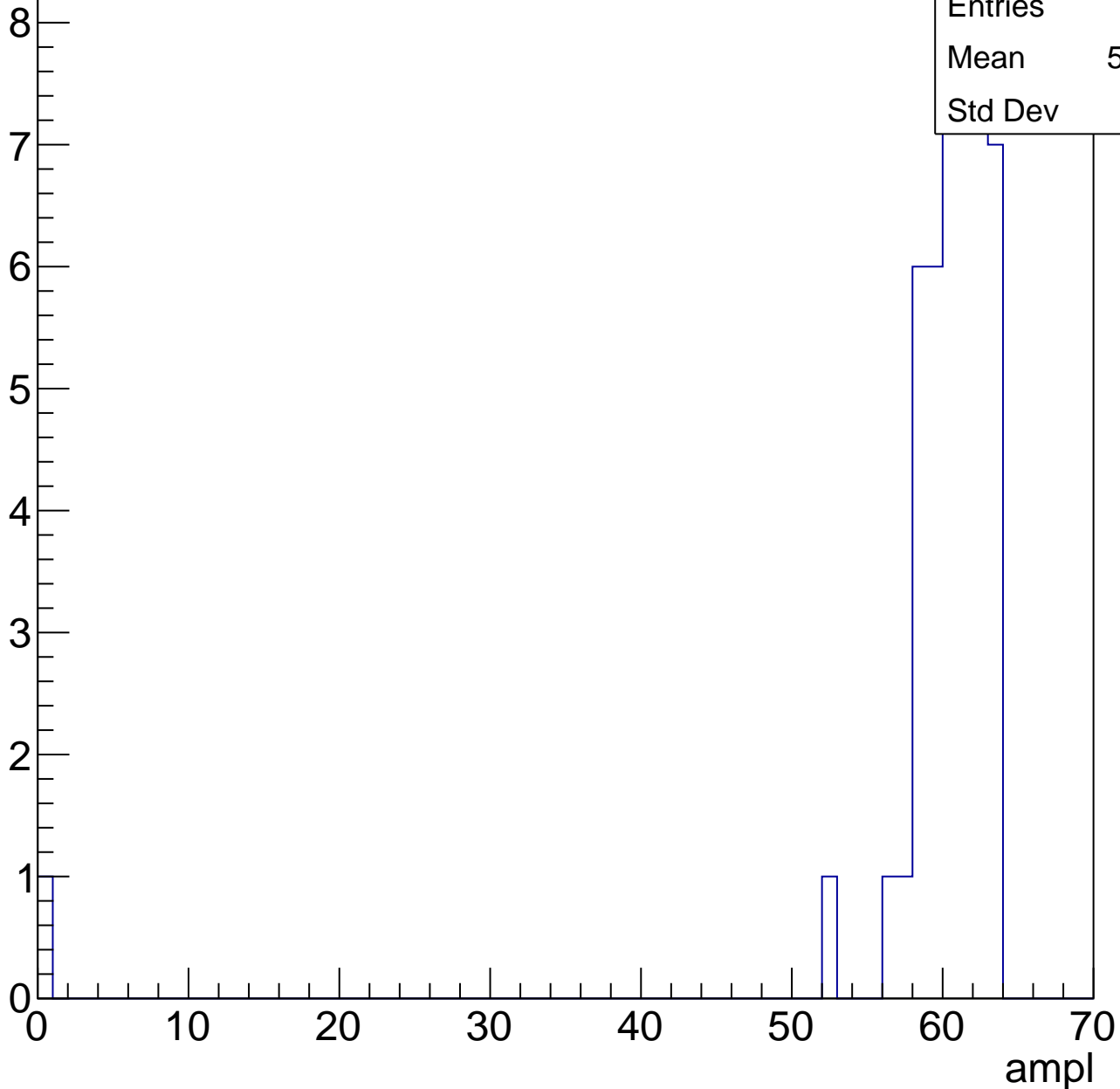


# B1L103S, U26-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	58.98
Std Dev	8.96



# B1L103S, U26-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

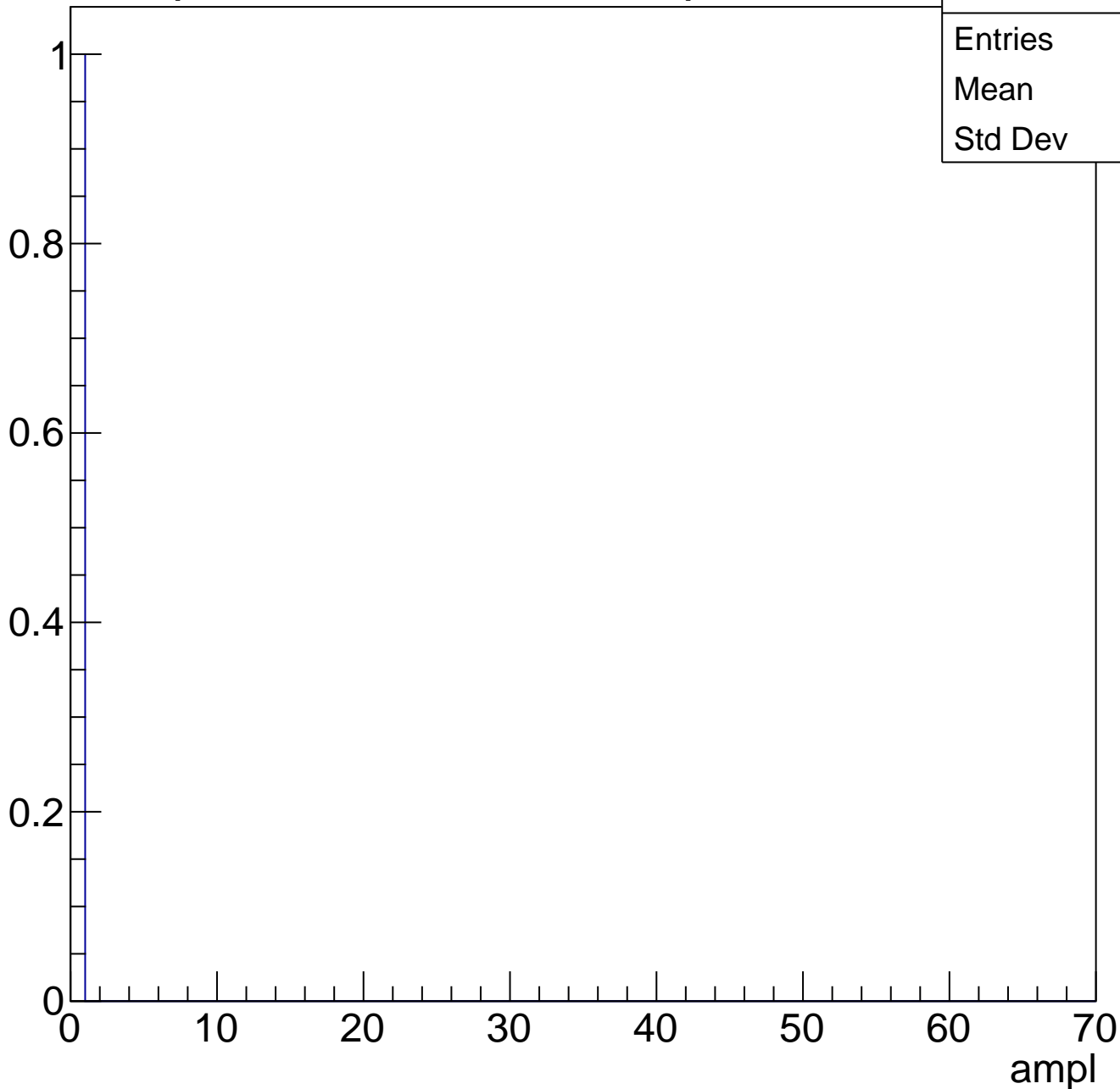
0 10 20 30 40 50 60 70



# B1L103S, U26-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch62, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	61
Mean	27.13
Std Dev	6.045

**Gaus mean : 28.3446**

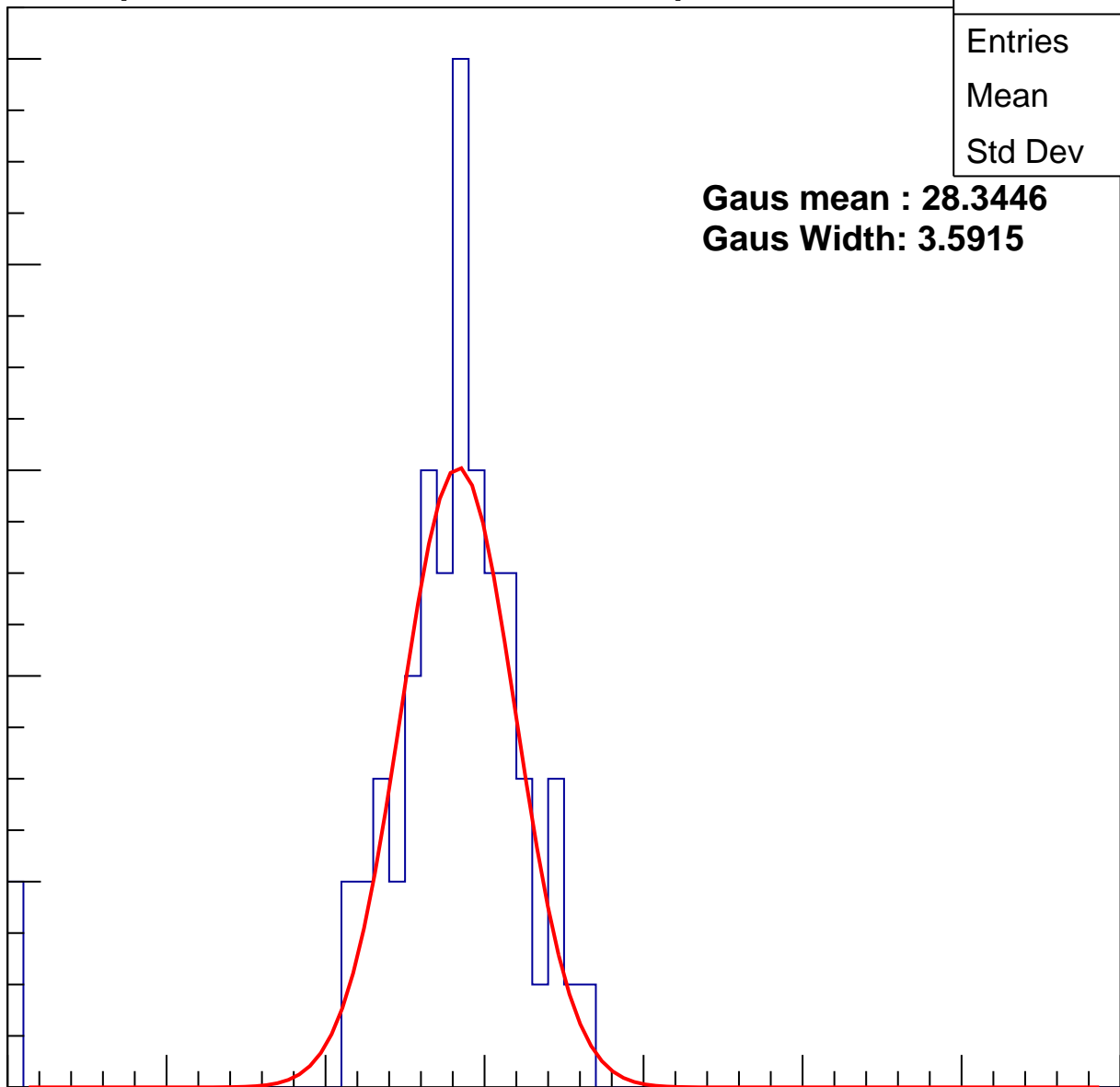
**Gaus Width: 3.5915**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



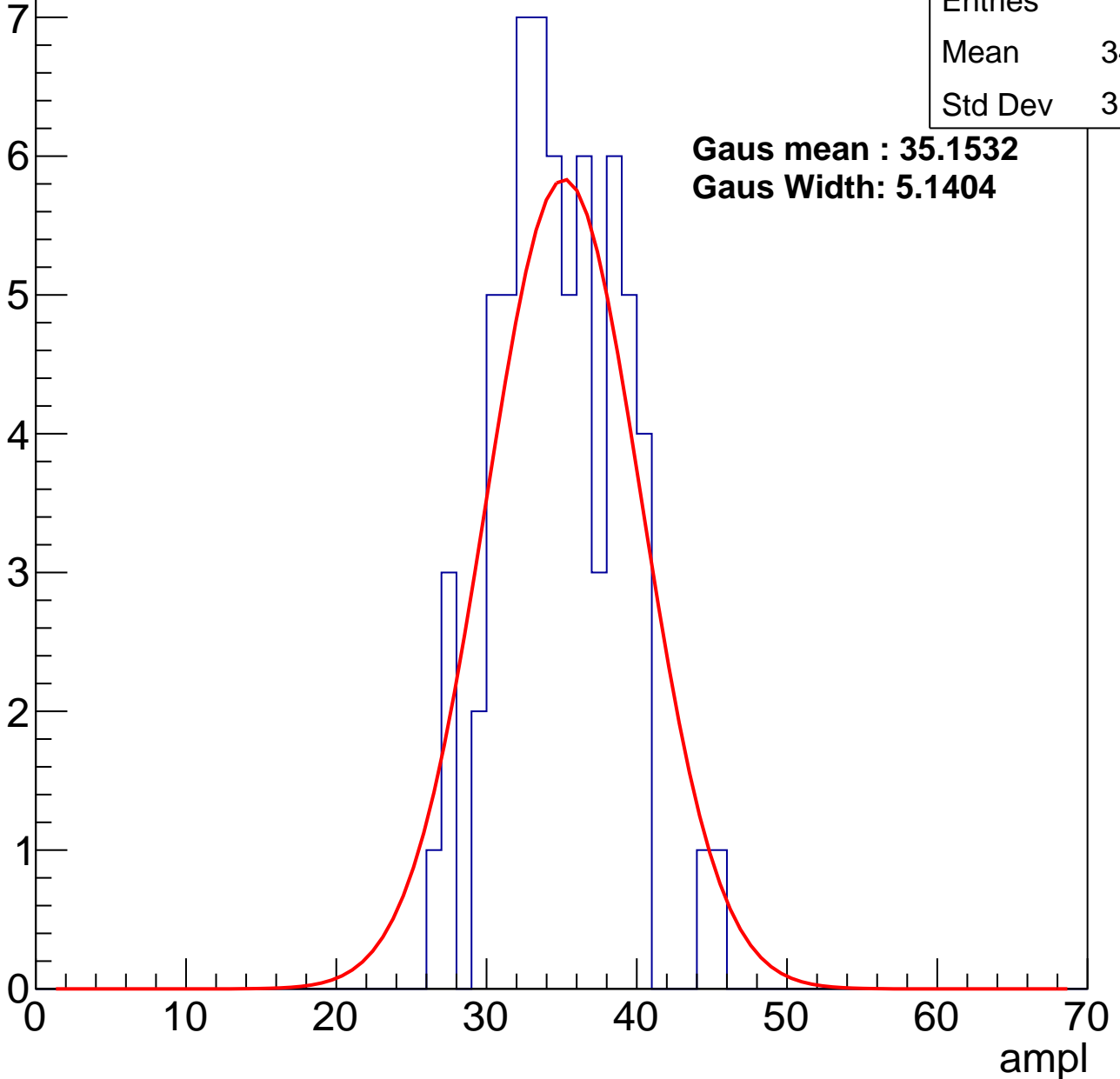
# B1L103S, U26-ch62, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	34.37
Std Dev	3.966

**Gaus mean : 35.1532**  
**Gaus Width: 5.1404**



# B1L103S, U26-ch62, adc2

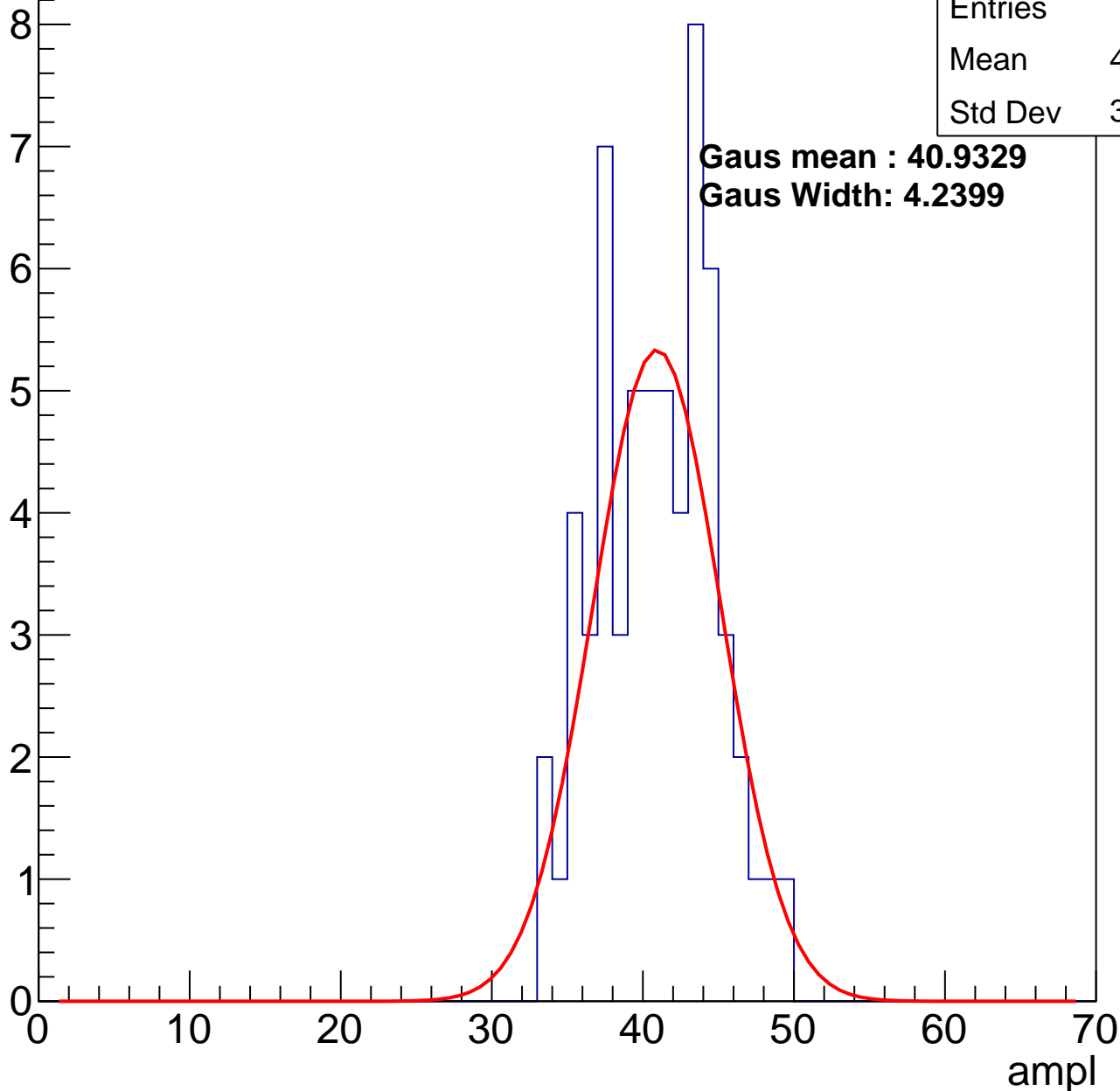
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	40.46
Std Dev	3.796

**Gaus mean : 40.9329**

**Gaus Width: 4.2399**

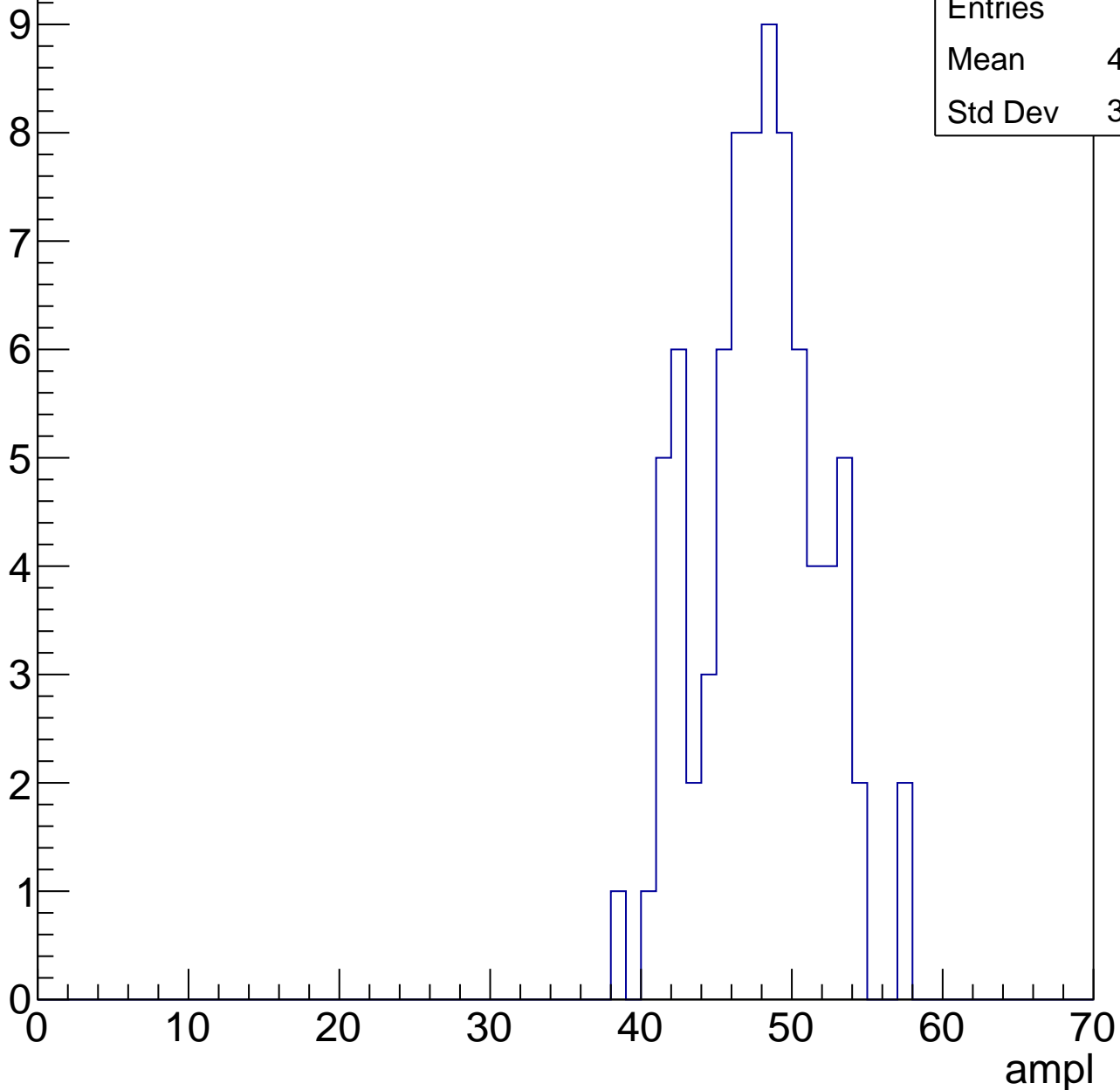


# B1L103S, U26-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	47.38
Std Dev	3.995

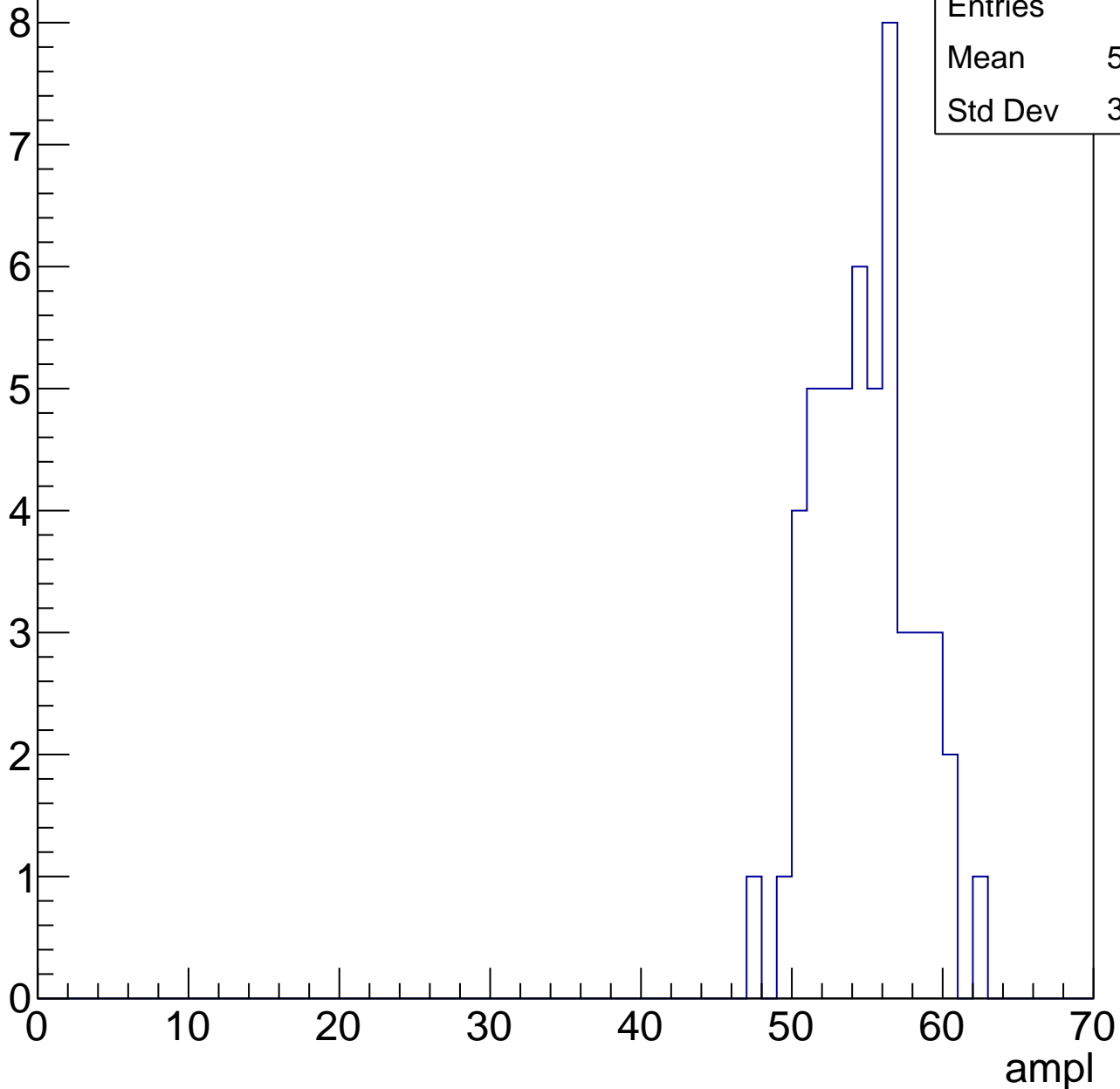


# B1L103S, U26-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	54.37
Std Dev	3.175

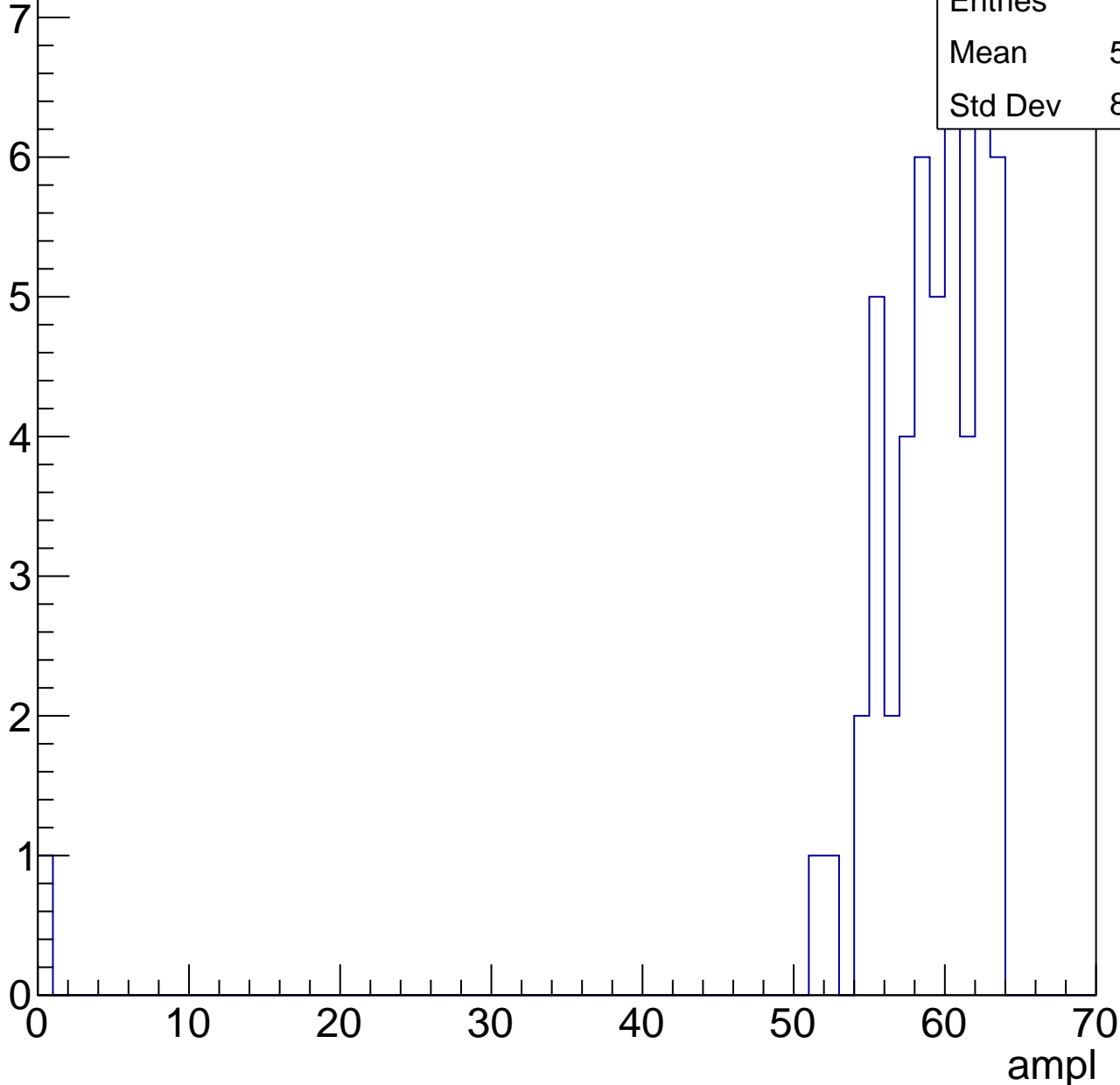


# B1L103S, U26-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

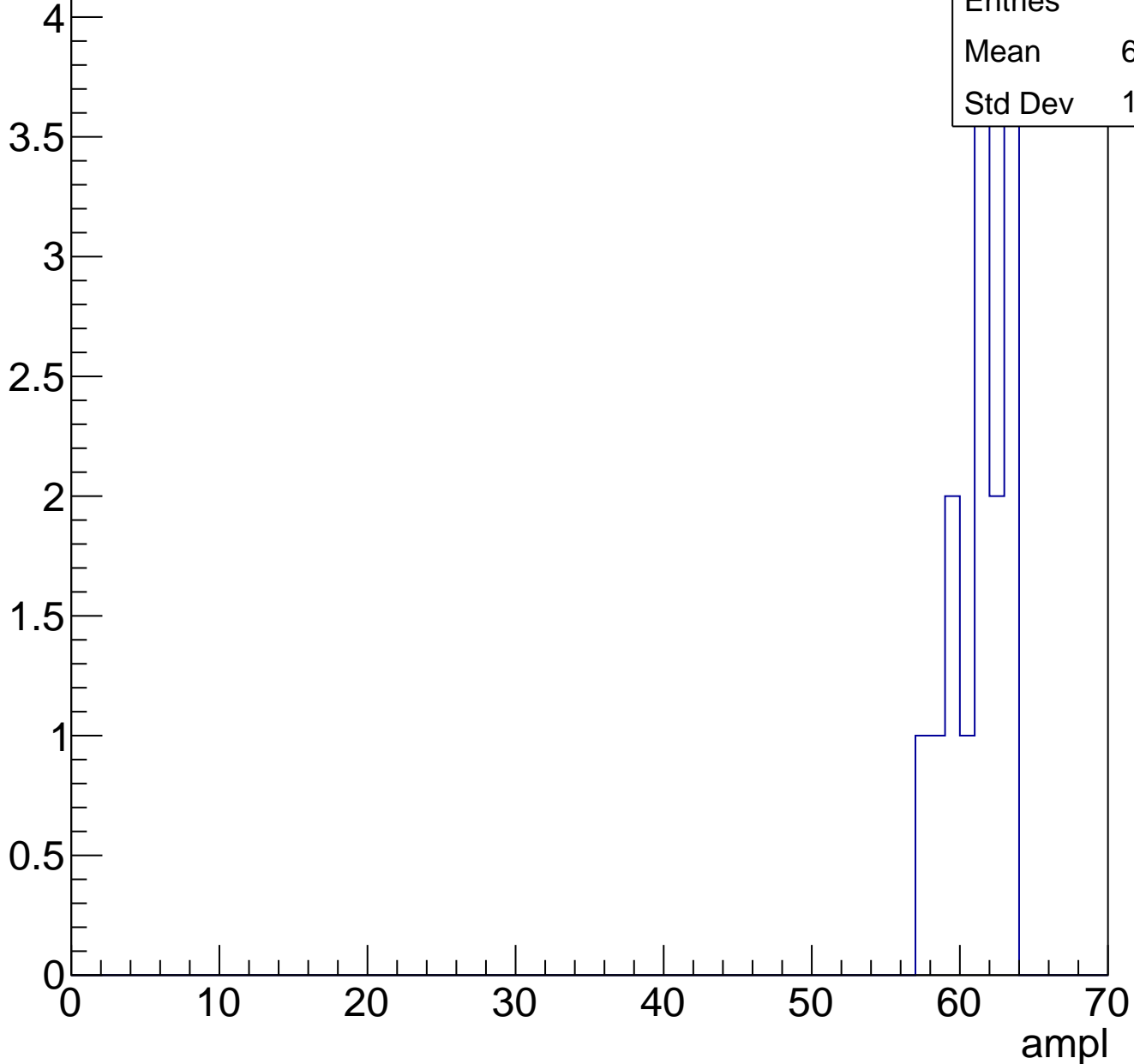
Entries	51
Mean	57.75
Std Dev	8.706



# B1L103S, U26-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	61
Std Dev	0

ampl

# B1L103S, U26-ch63, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	71
Mean	30.41
Std Dev	3.372

**Gaus mean : 29.9999**

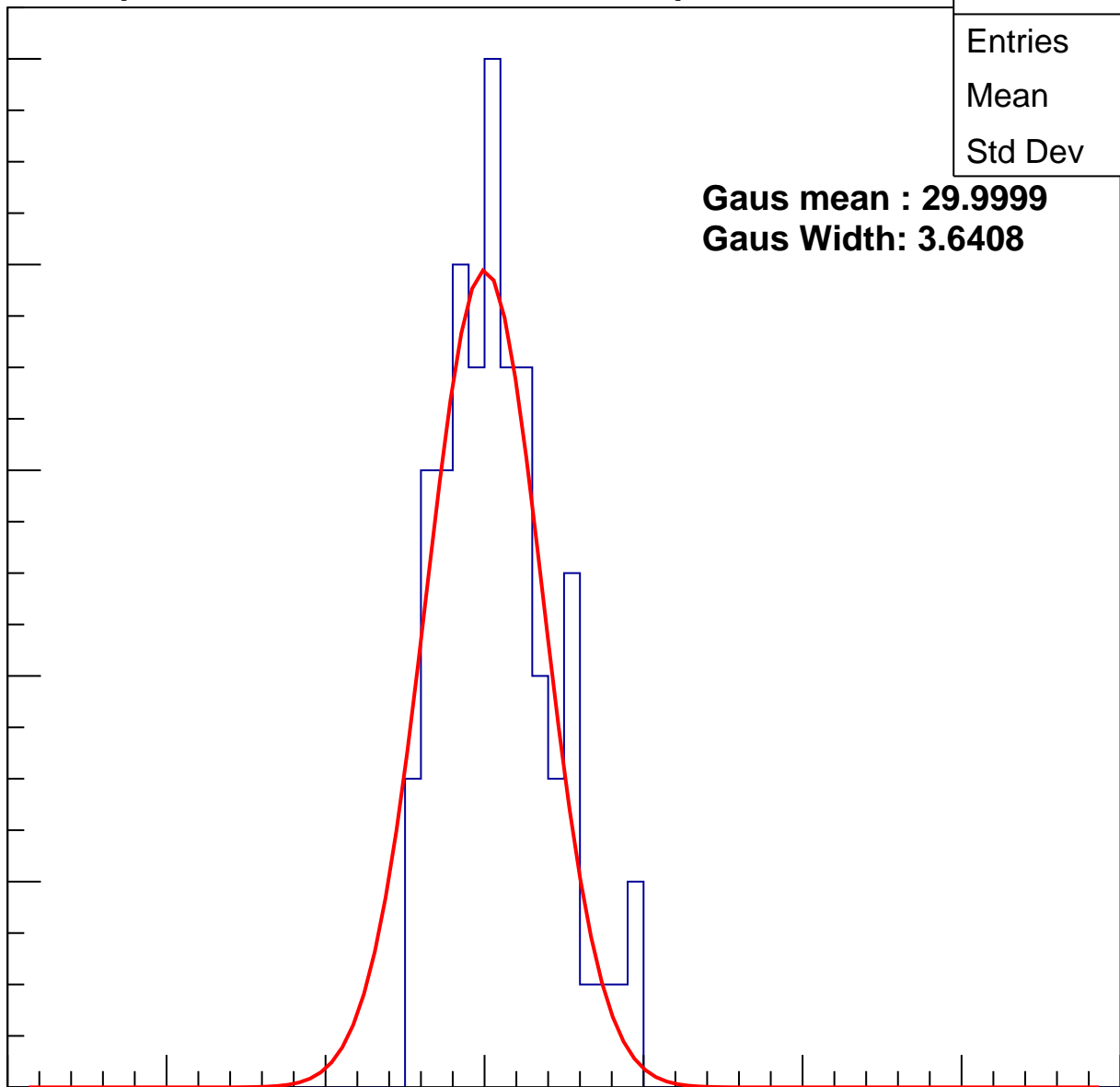
**Gaus Width: 3.6408**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch63, adc1

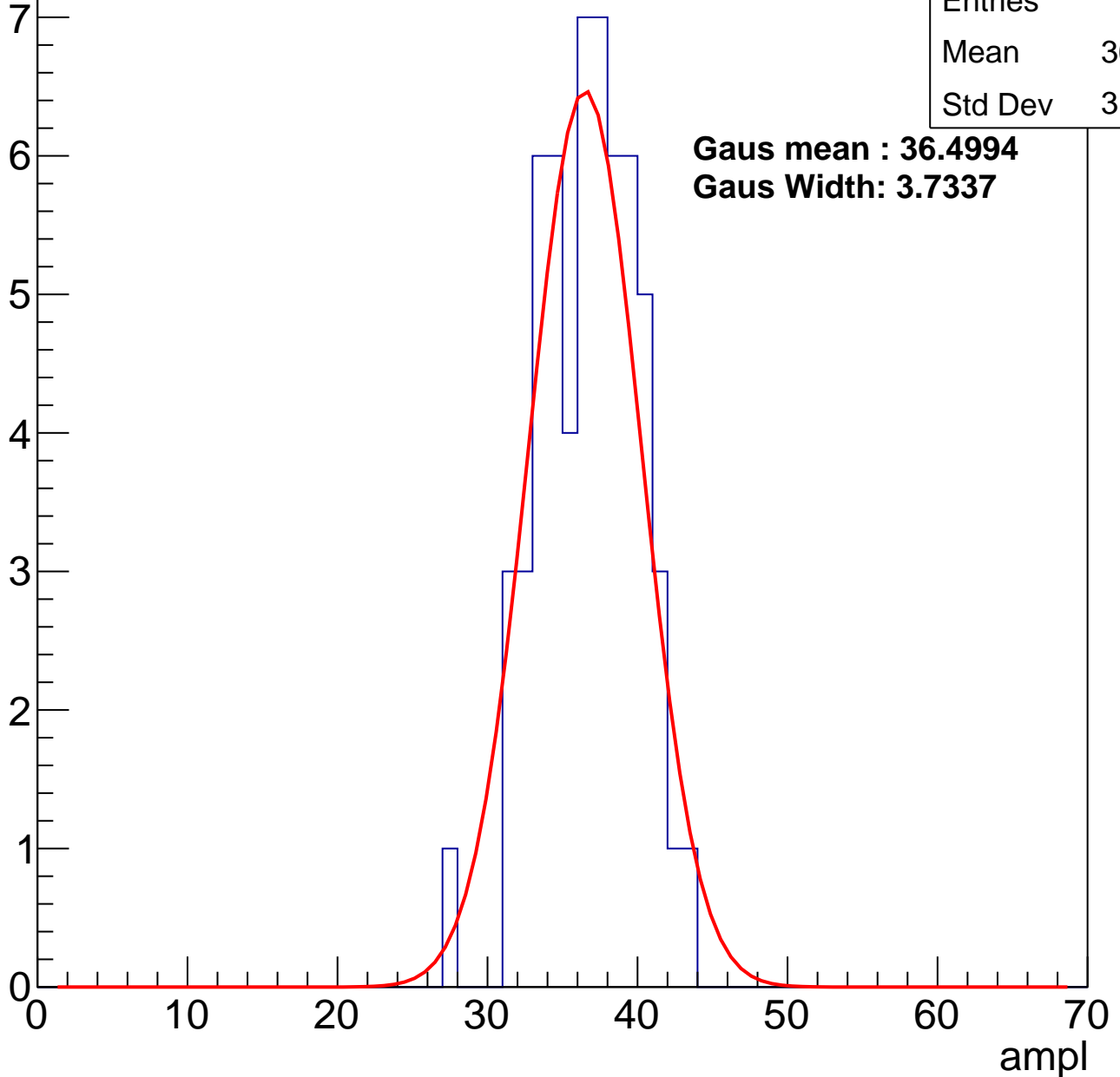
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	36.25
Std Dev	3.208

**Gaus mean : 36.4994**

**Gaus Width: 3.7337**



# B1L103S, U26-ch63, adc2

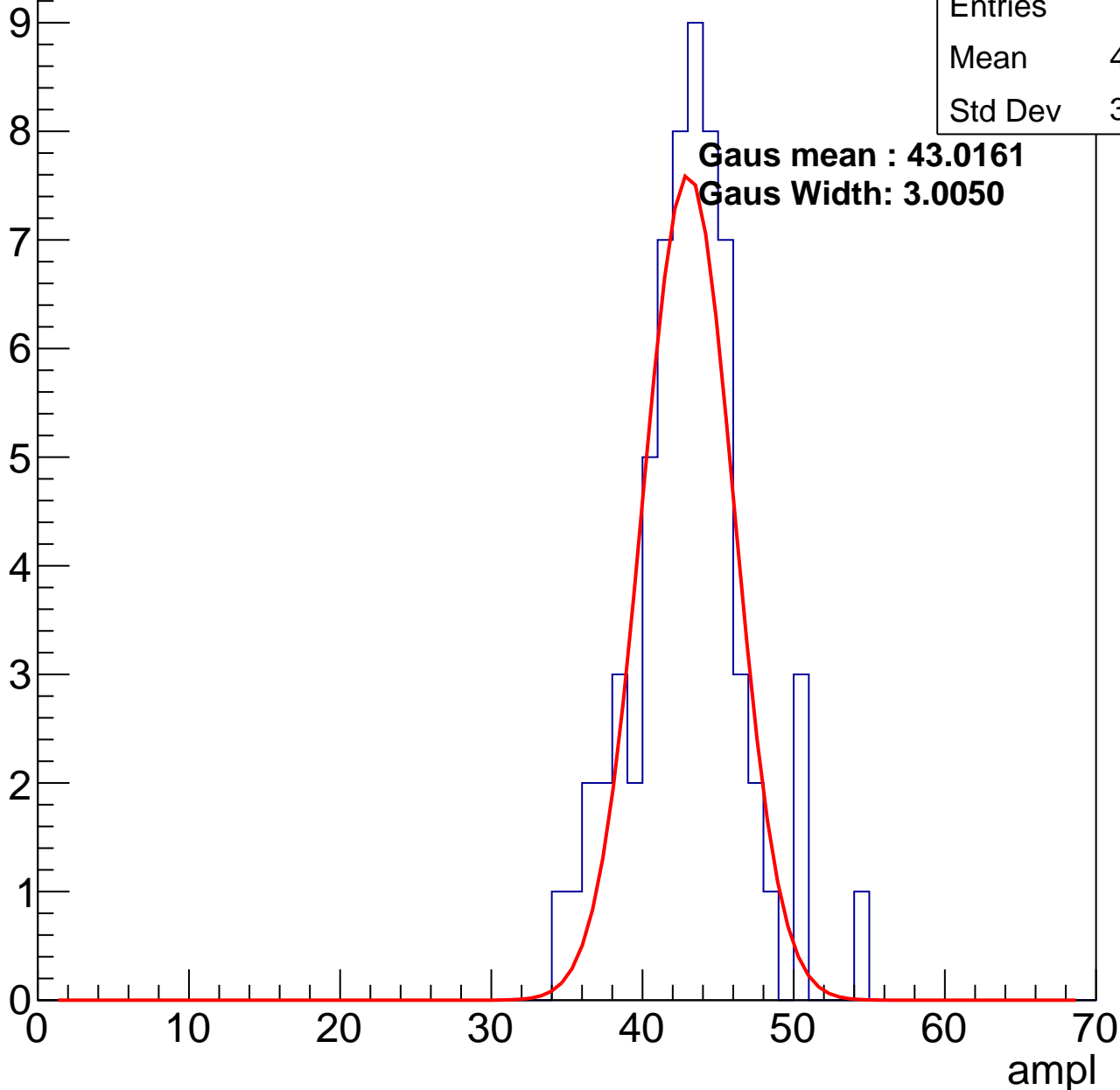
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	42.58
Std Dev	3.679

**Gaus mean : 43.0161**

**Gaus Width: 3.0050**



# B1L103S, U26-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	86
Mean	50.19
Std Dev	3.552

Entry

10

8

6

4

2

0

0

10

20

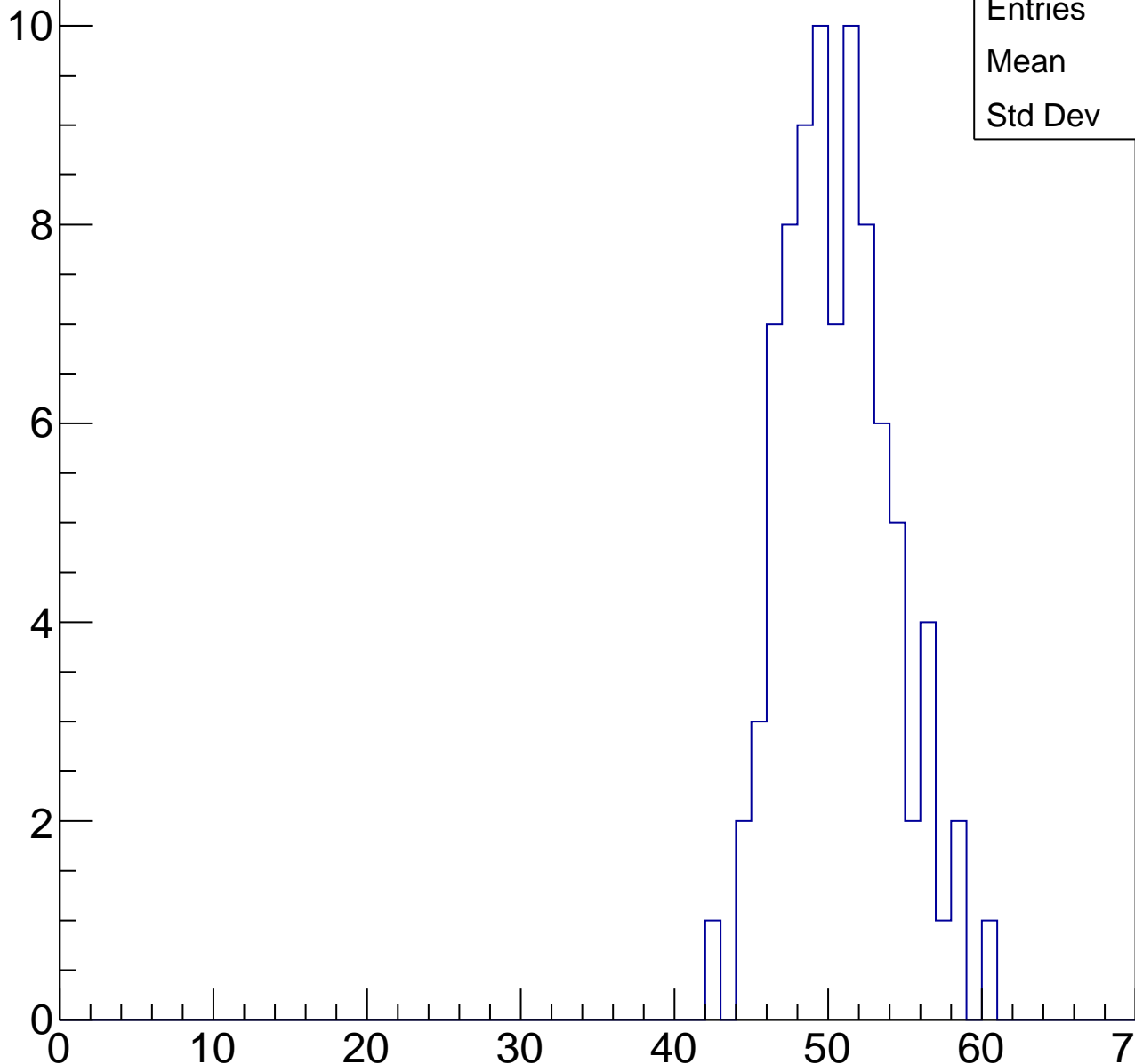
30

40

50

60

ampl

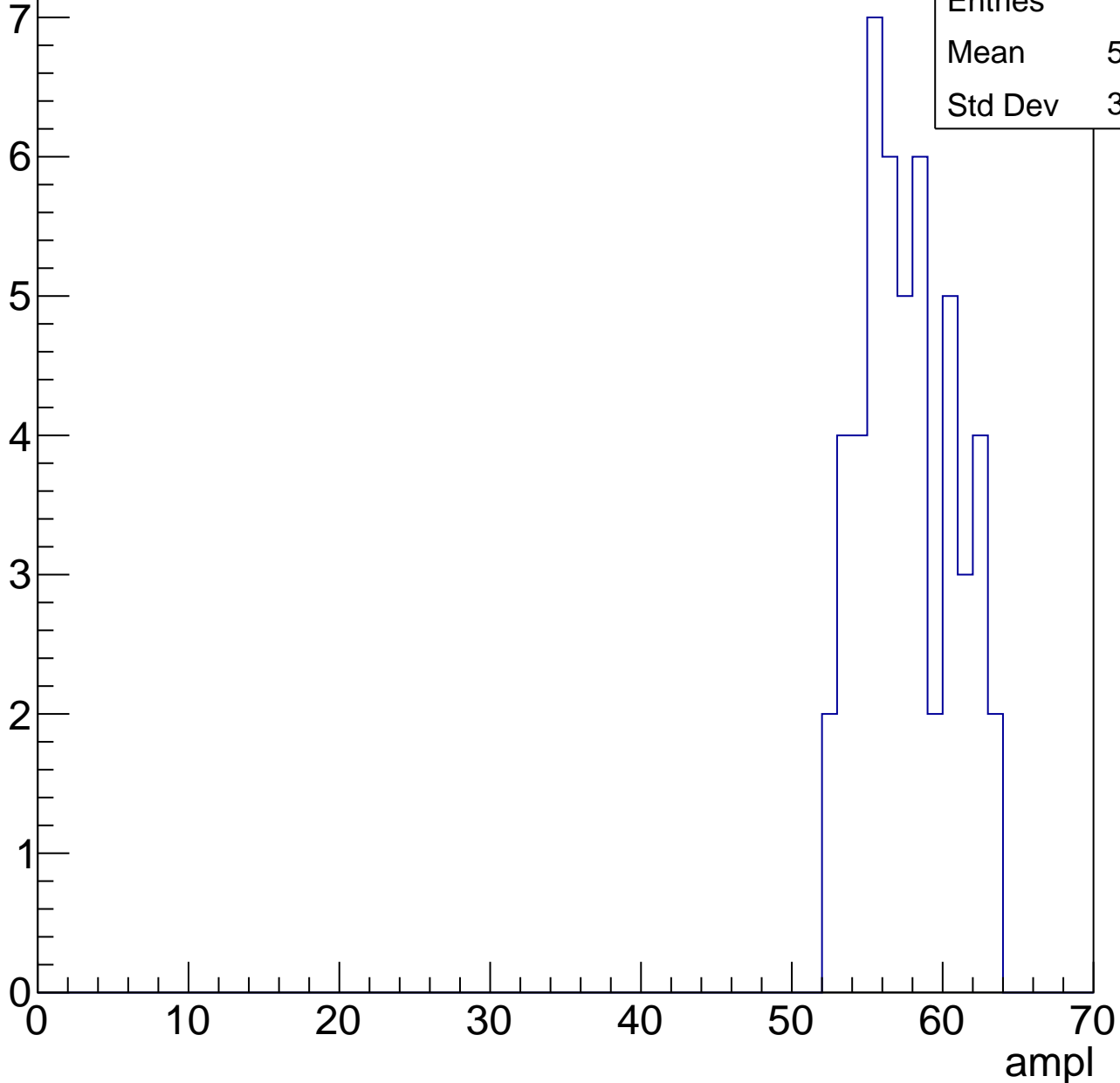


# B1L103S, U26-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	57.22
Std Dev	3.035



# B1L103S, U26-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	36
Mean	58.39
Std Dev	10.08

ampl

0 10 20 30 40 50 60 70

1

2

3

4

5

6

7

8

# B1L103S, U26-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	22
Std Dev	0

# B1L103S, U26-ch64, adc0

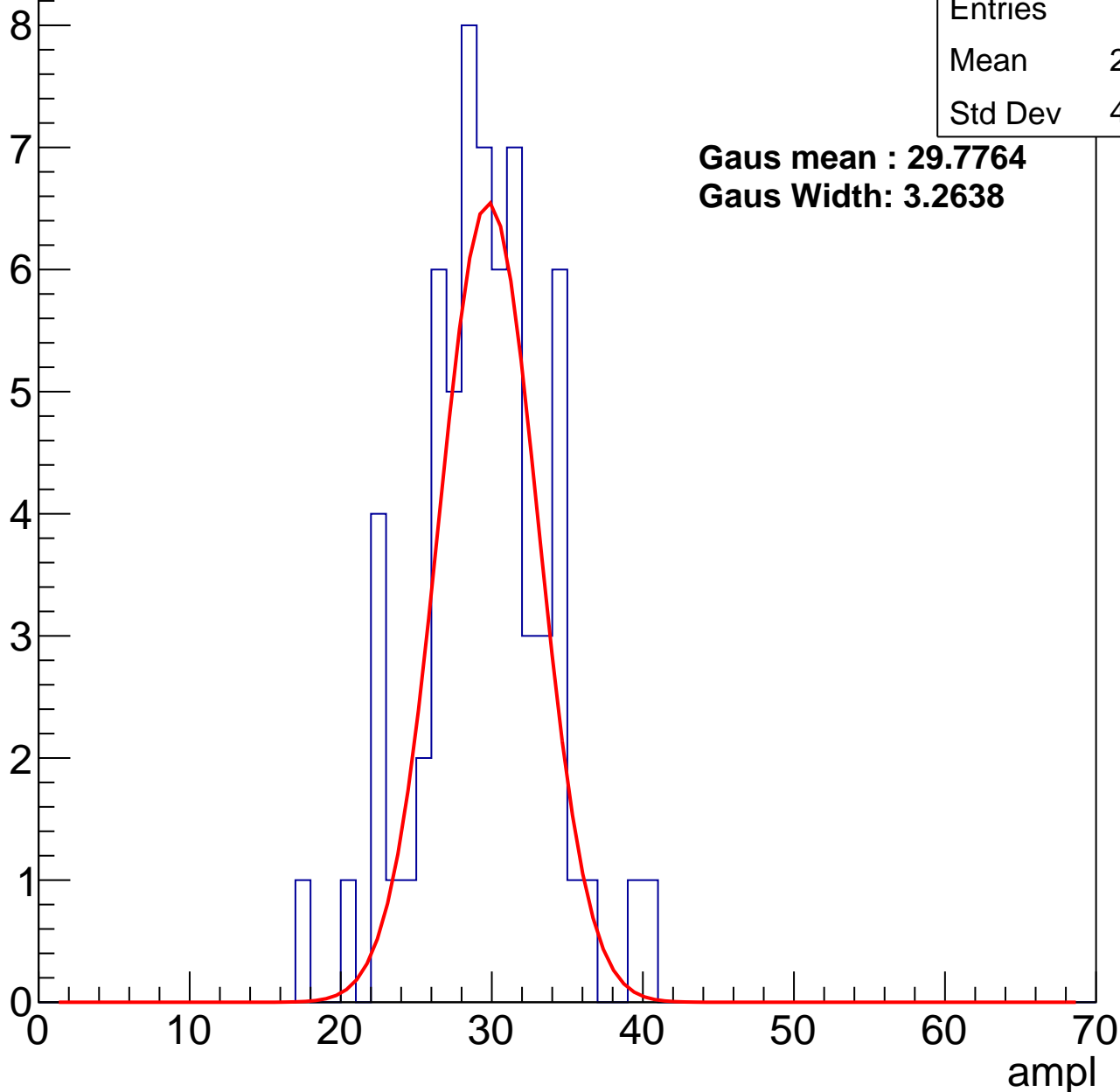
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	29.02
Std Dev	4.226

**Gaus mean : 29.7764**

**Gaus Width: 3.2638**



# B1L103S, U26-ch64, adc1

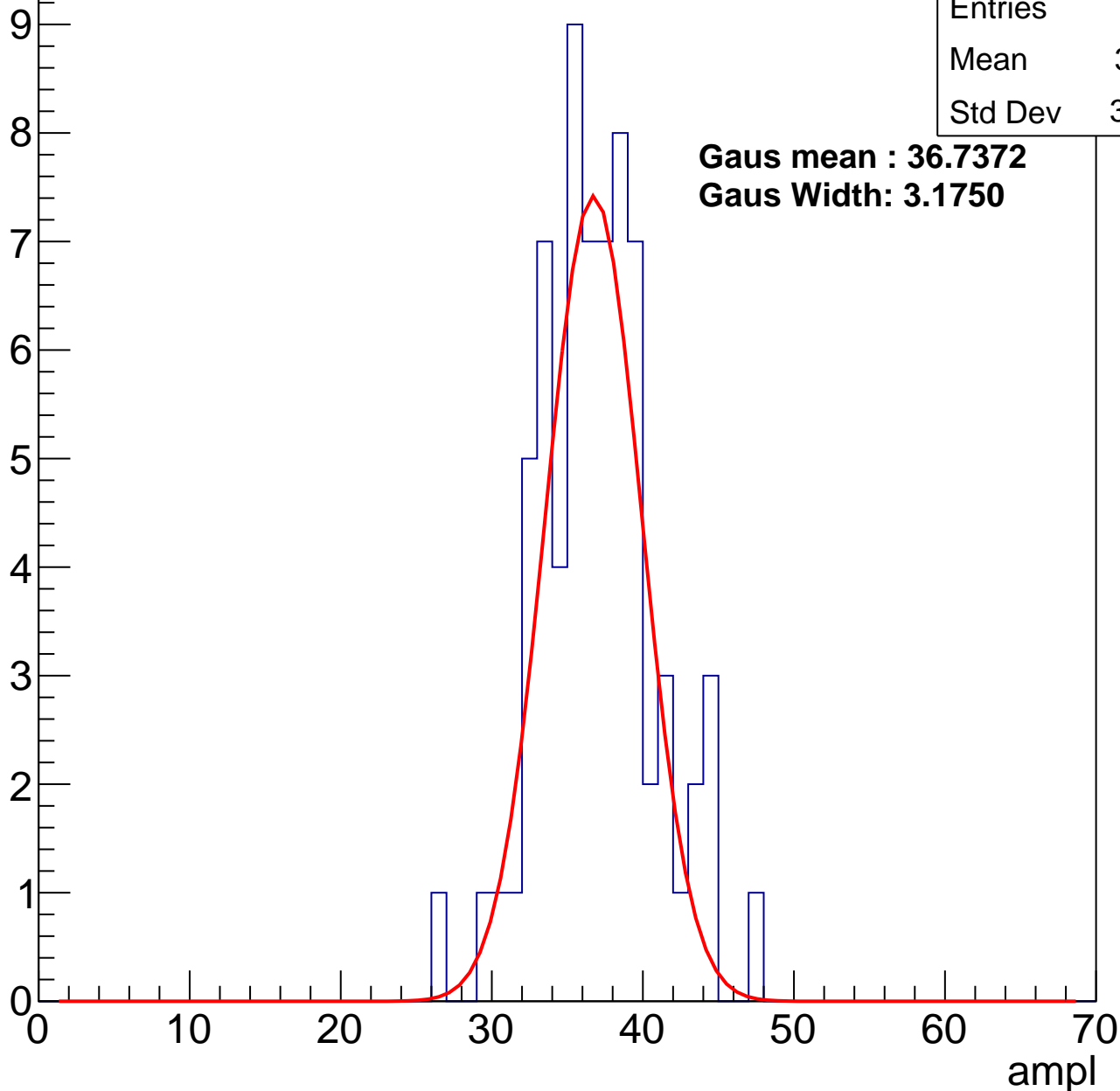
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	36.51
Std Dev	3.809

**Gaus mean : 36.7372**

**Gaus Width: 3.1750**



# B1L103S, U26-ch64, adc2

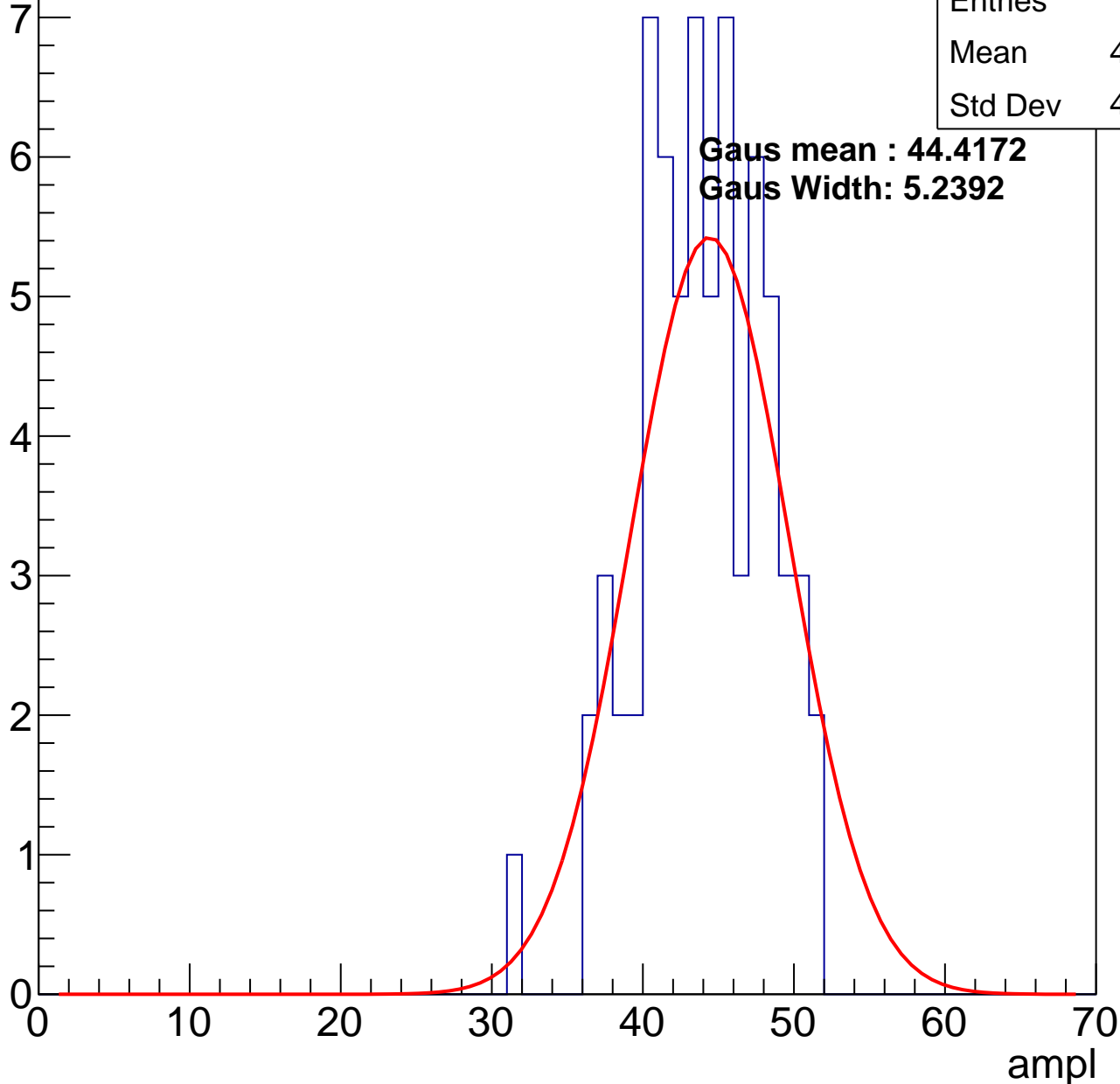
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	43.46
Std Dev	4.123

**Gaus mean : 44.4172**

**Gaus Width: 5.2392**

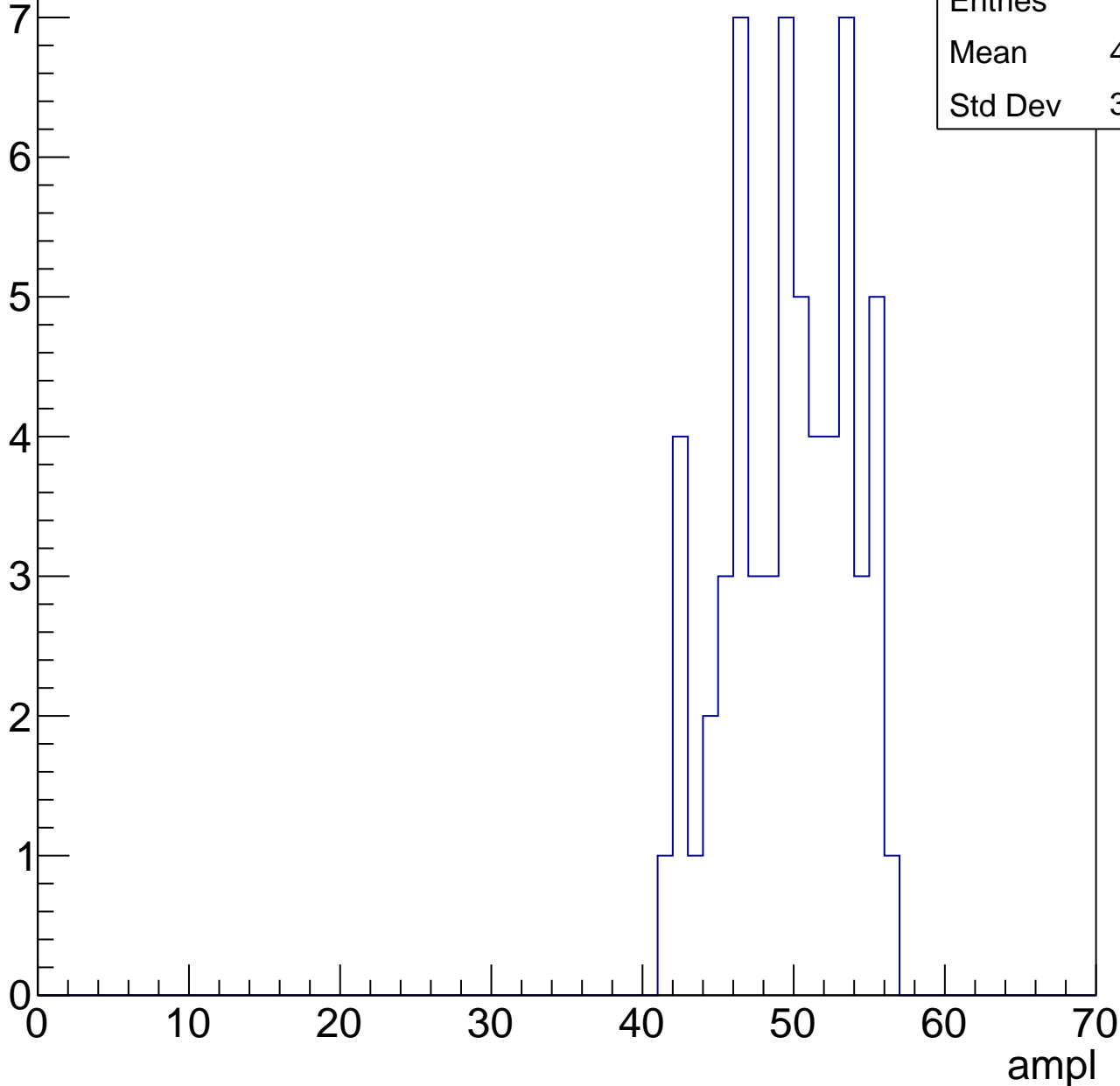


# B1L103S, U26-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	49.18
Std Dev	3.964

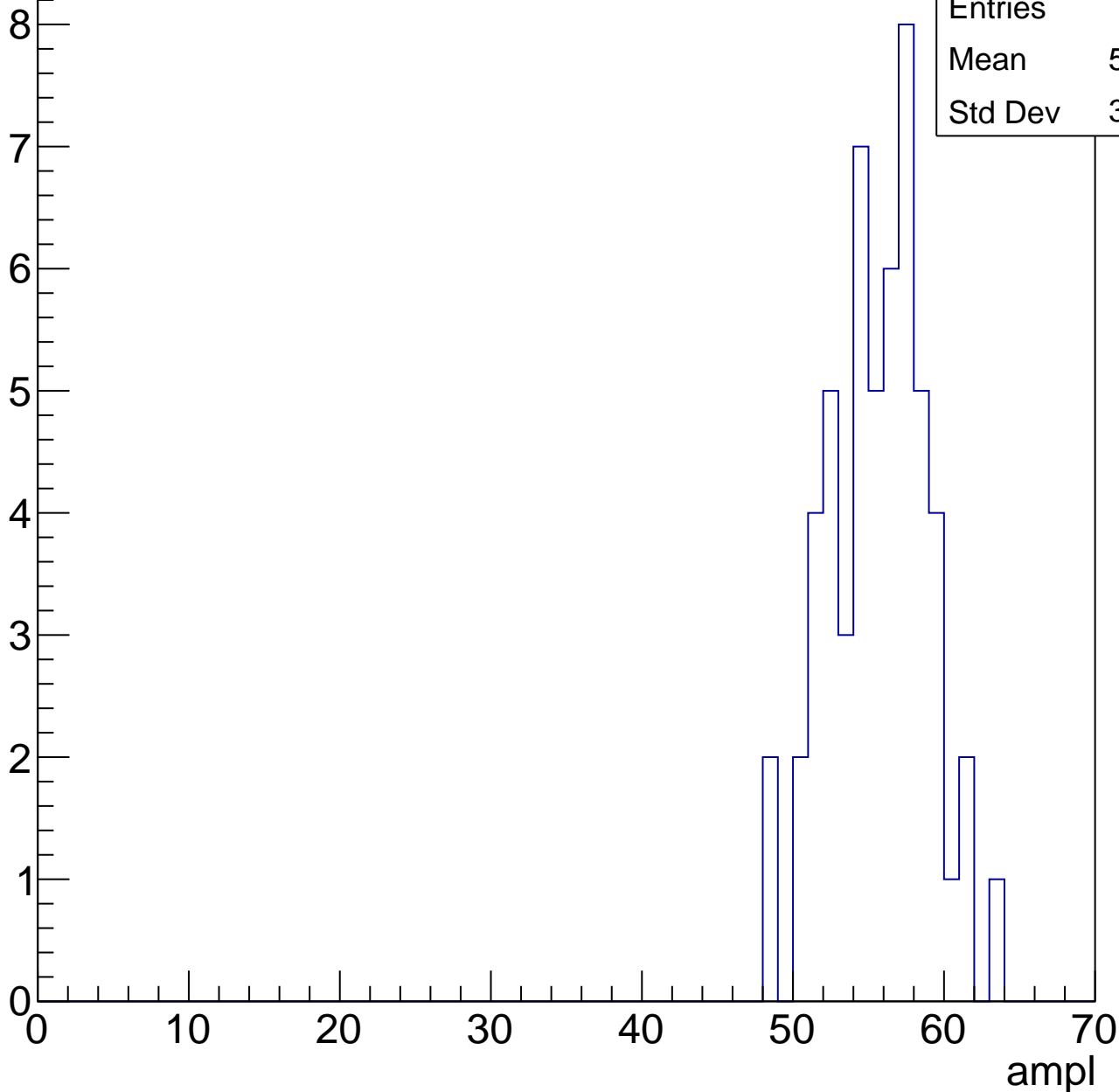


# B1L103S, U26-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

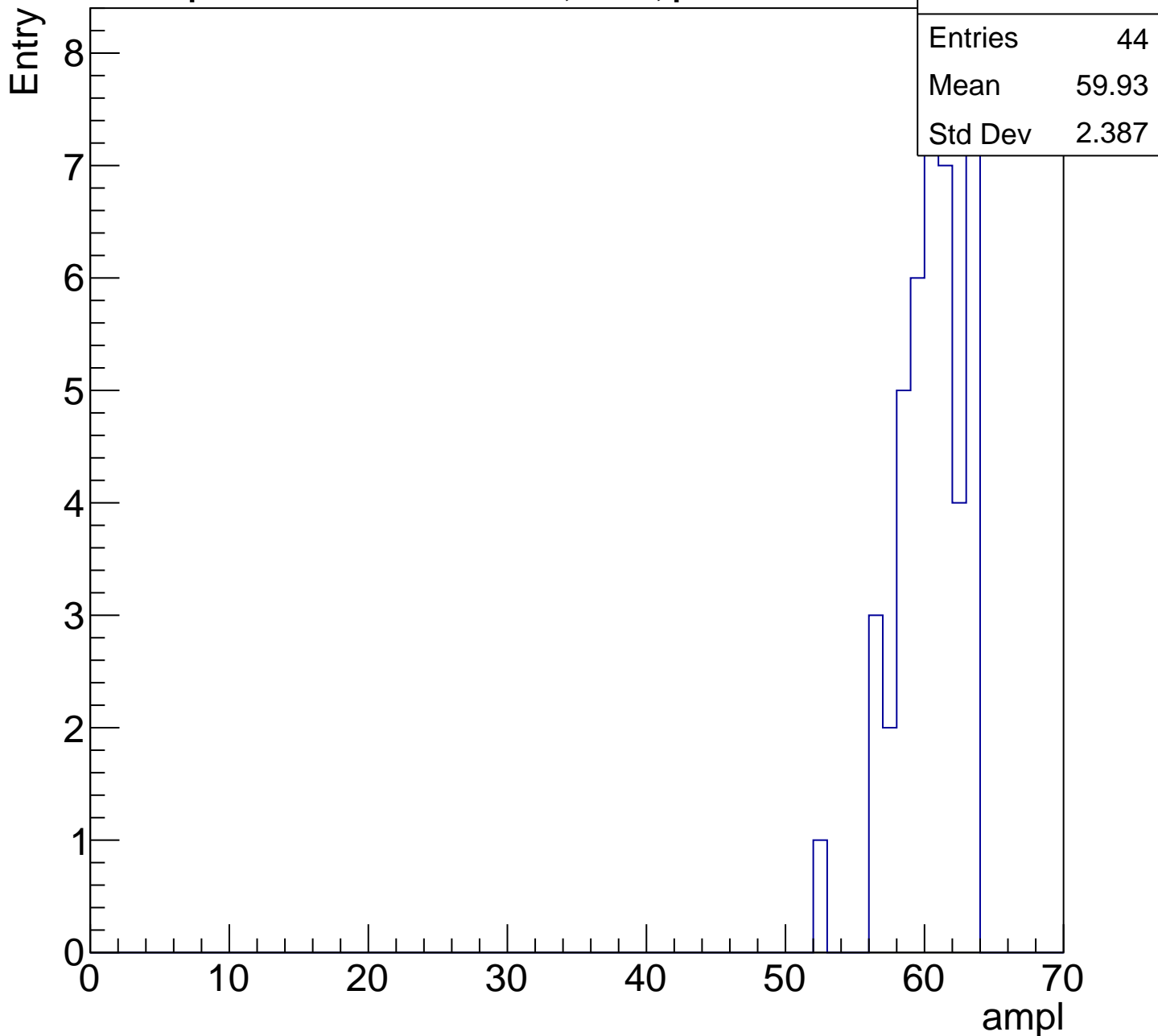
Entry

Entries	55
Mean	55.18
Std Dev	3.253



# B1L103S, U26-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

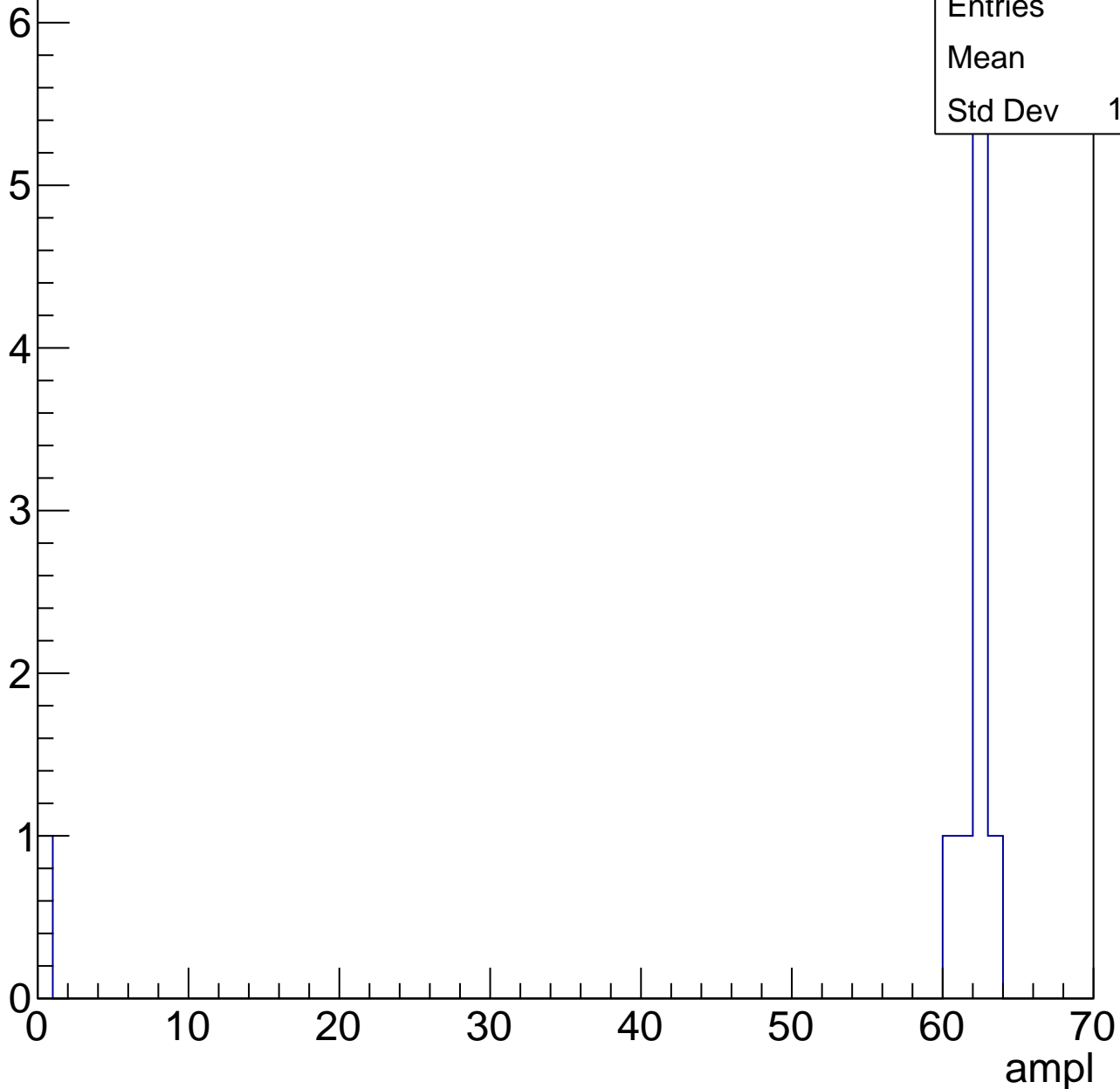


# B1L103S, U26-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	10
Mean	55.6
Std Dev	18.55





# B1L103S, U26-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch65, adc0

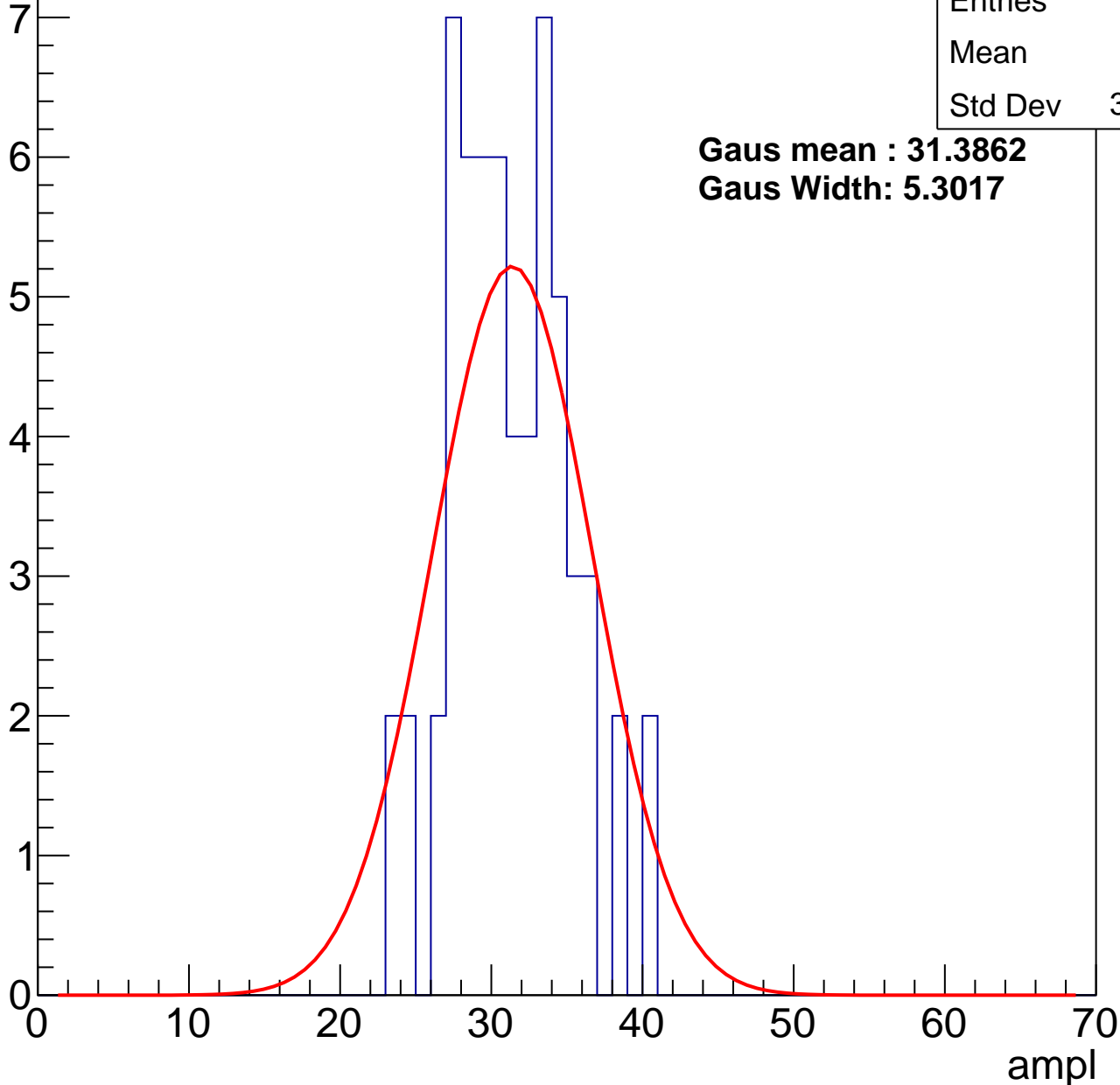
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	30.8
Std Dev	3.904

**Gaus mean : 31.3862**

**Gaus Width: 5.3017**



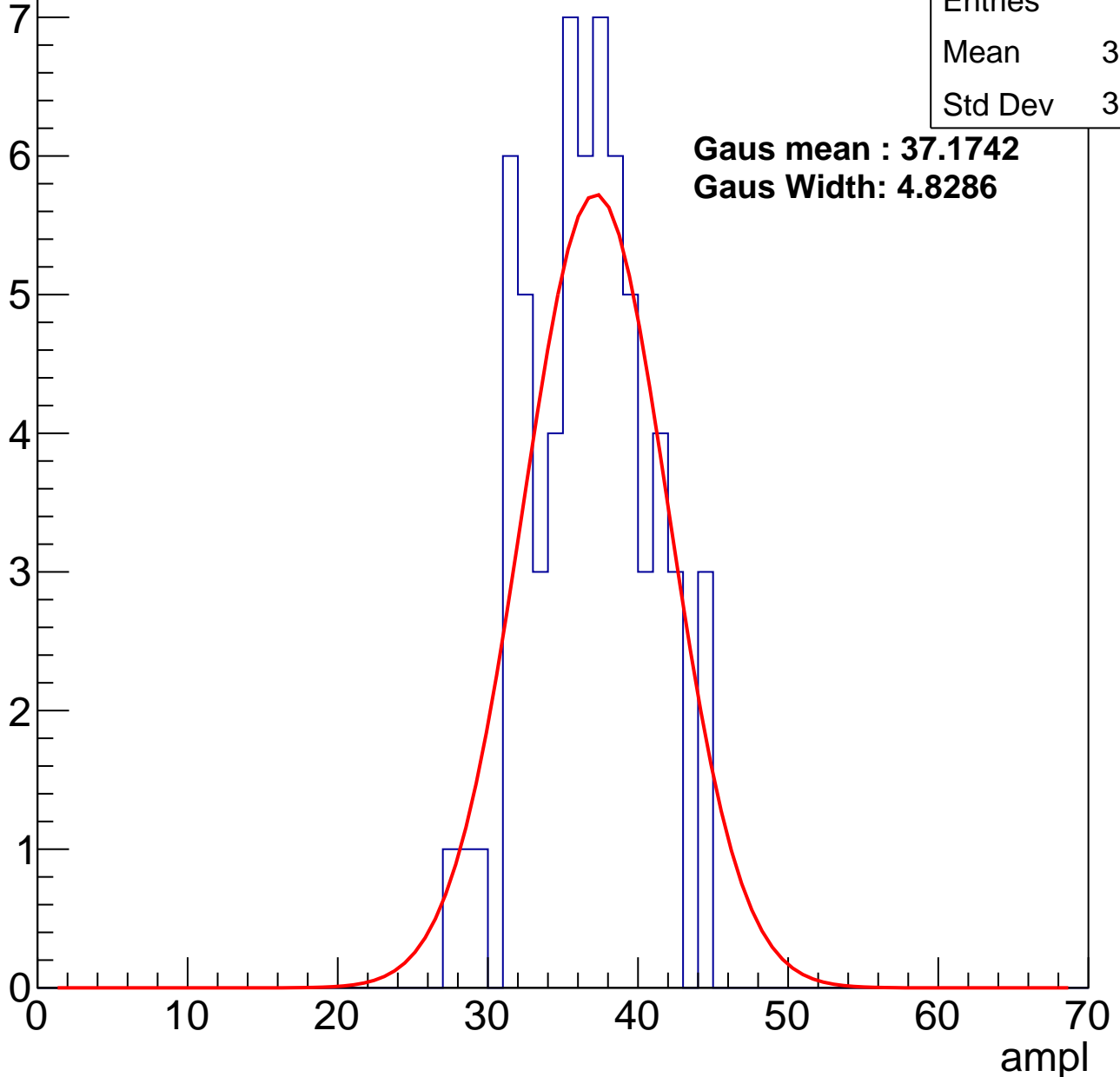
# B1L103S, U26-ch65, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	36.15
Std Dev	3.915

**Gaus mean : 37.1742**  
**Gaus Width: 4.8286**



# B1L103S, U26-ch65, adc2

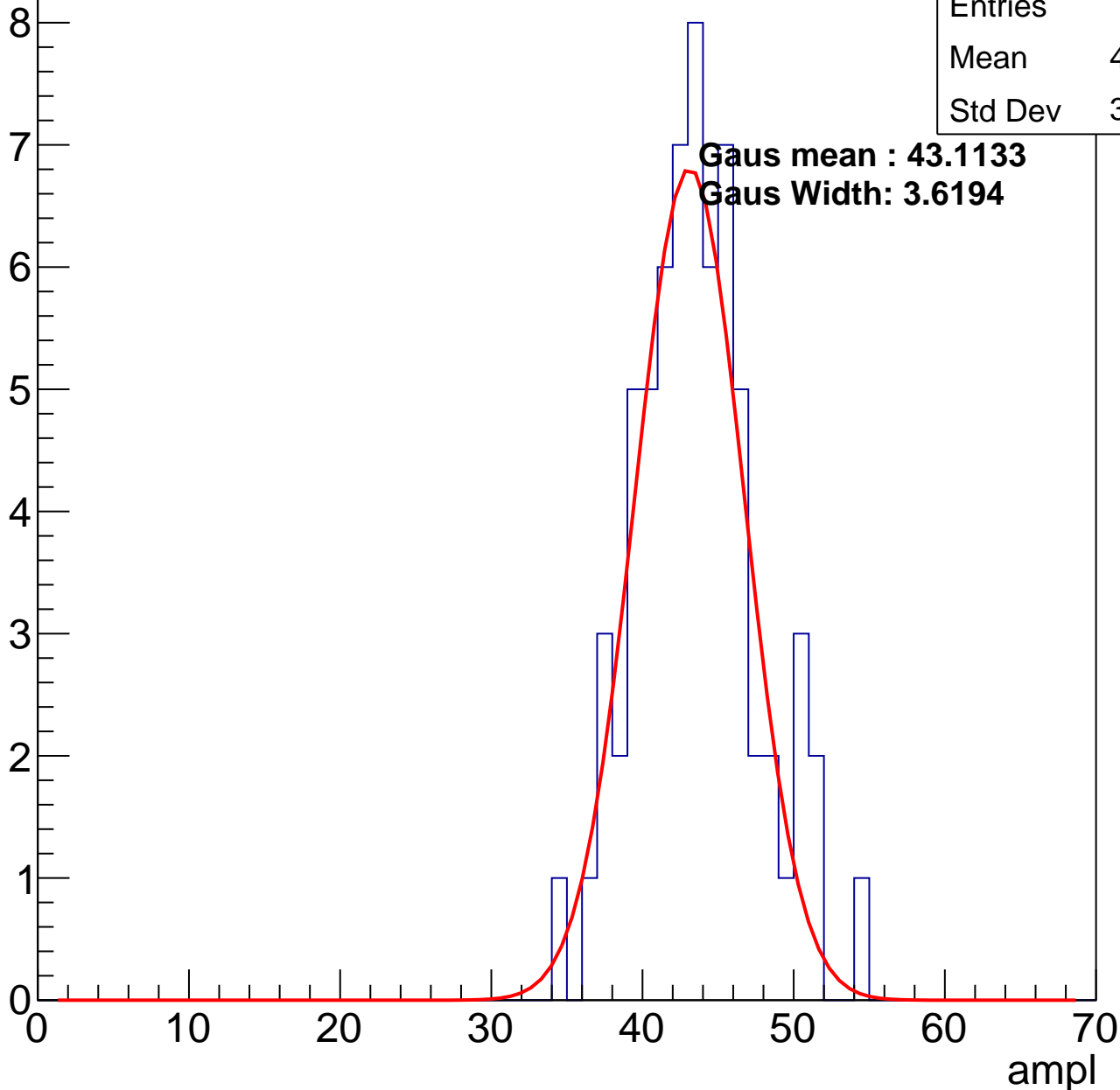
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	43.13
Std Dev	3.932

**Gaus mean : 43.1133**

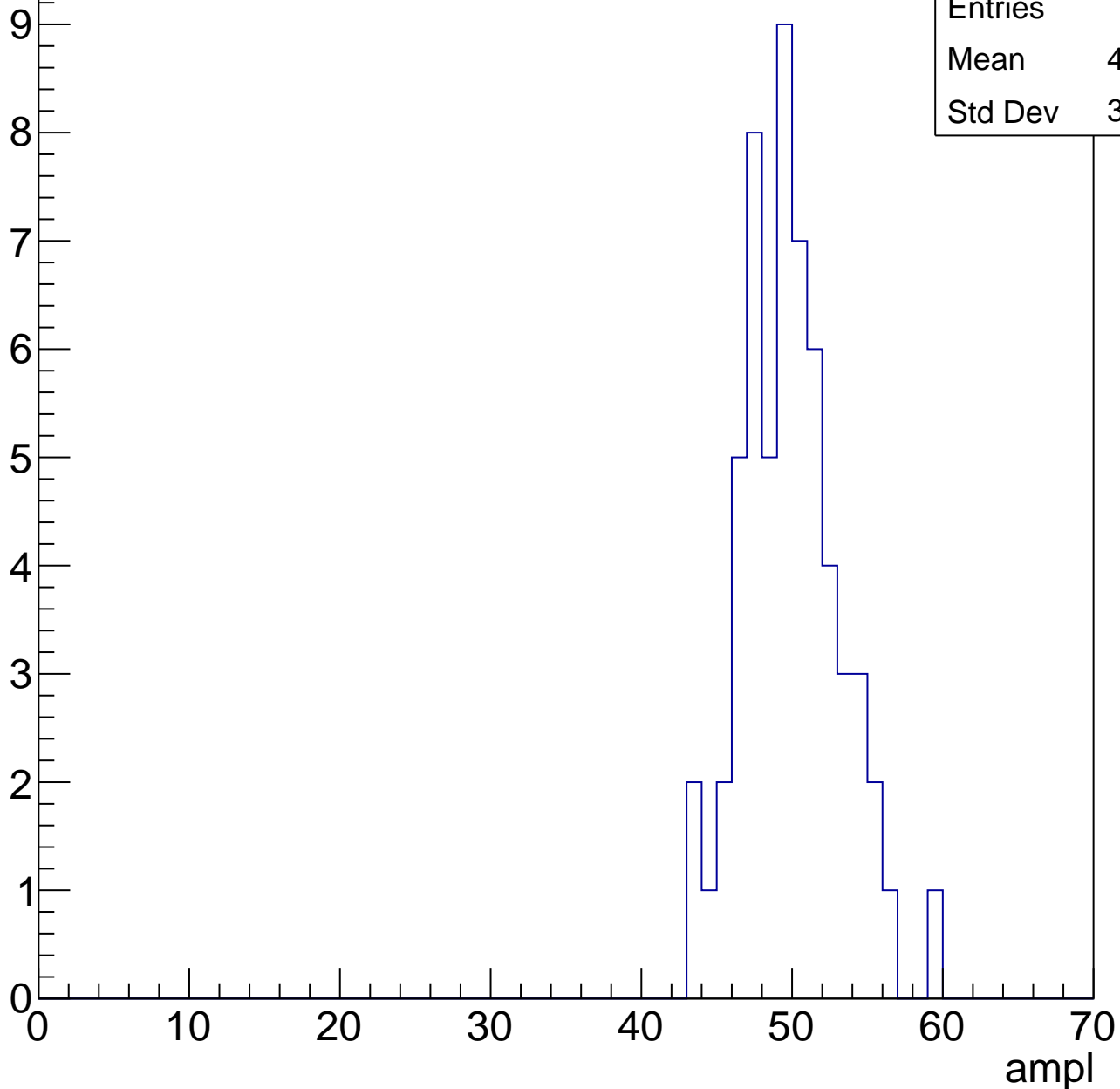
**Gaus Width: 3.6194**



# B1L103S, U26-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



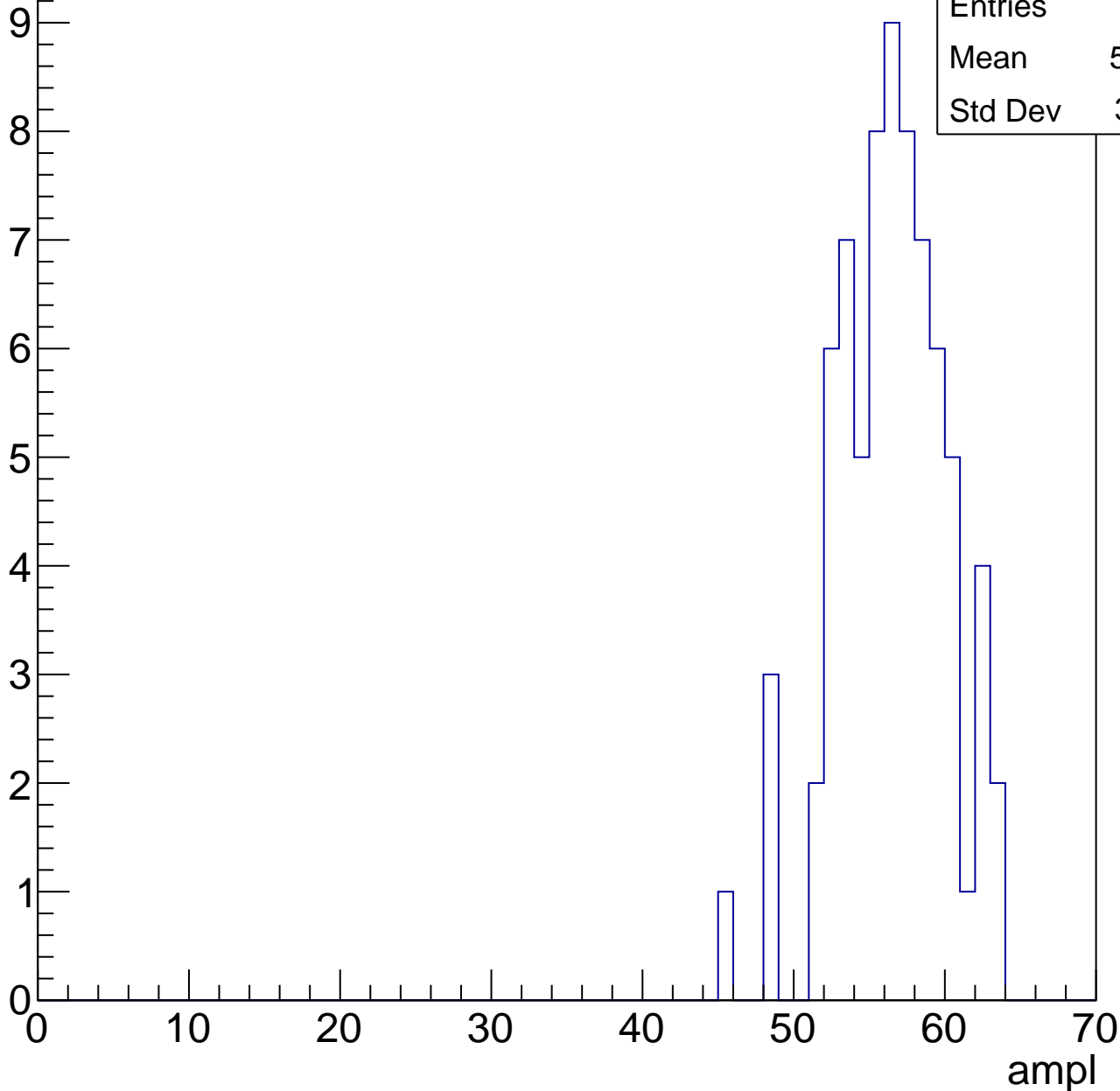
Entries	59
Mean	49.44
Std Dev	3.217

# B1L103S, U26-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	55.93
Std Dev	3.651

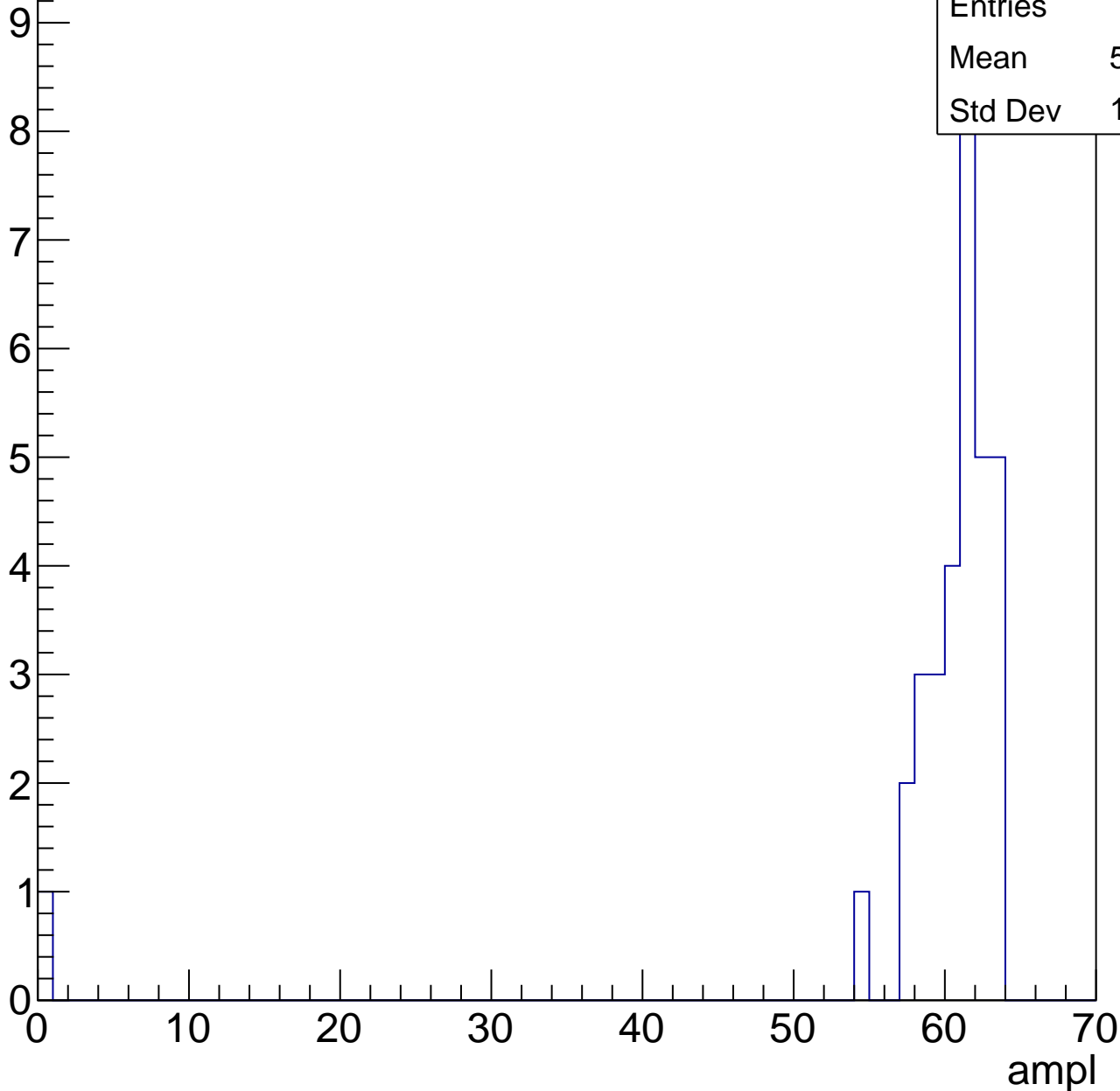


# B1L103S, U26-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	33
Mean	58.58
Std Dev	10.55



# B1L103S, U26-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U26-ch66, adc0

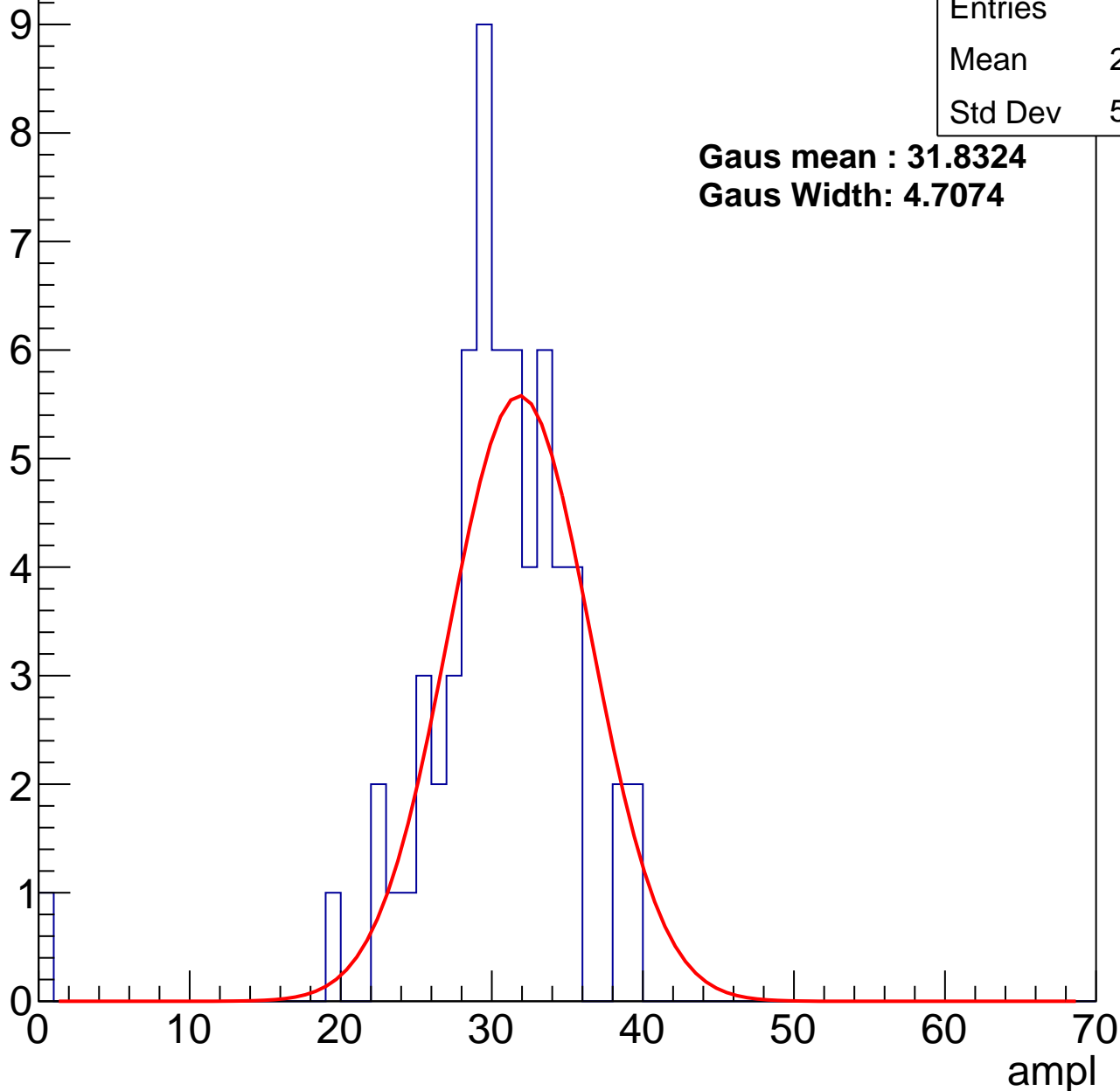
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	29.67
Std Dev	5.526

**Gaus mean : 31.8324**

**Gaus Width: 4.7074**



# B1L103S, U26-ch66, adc1

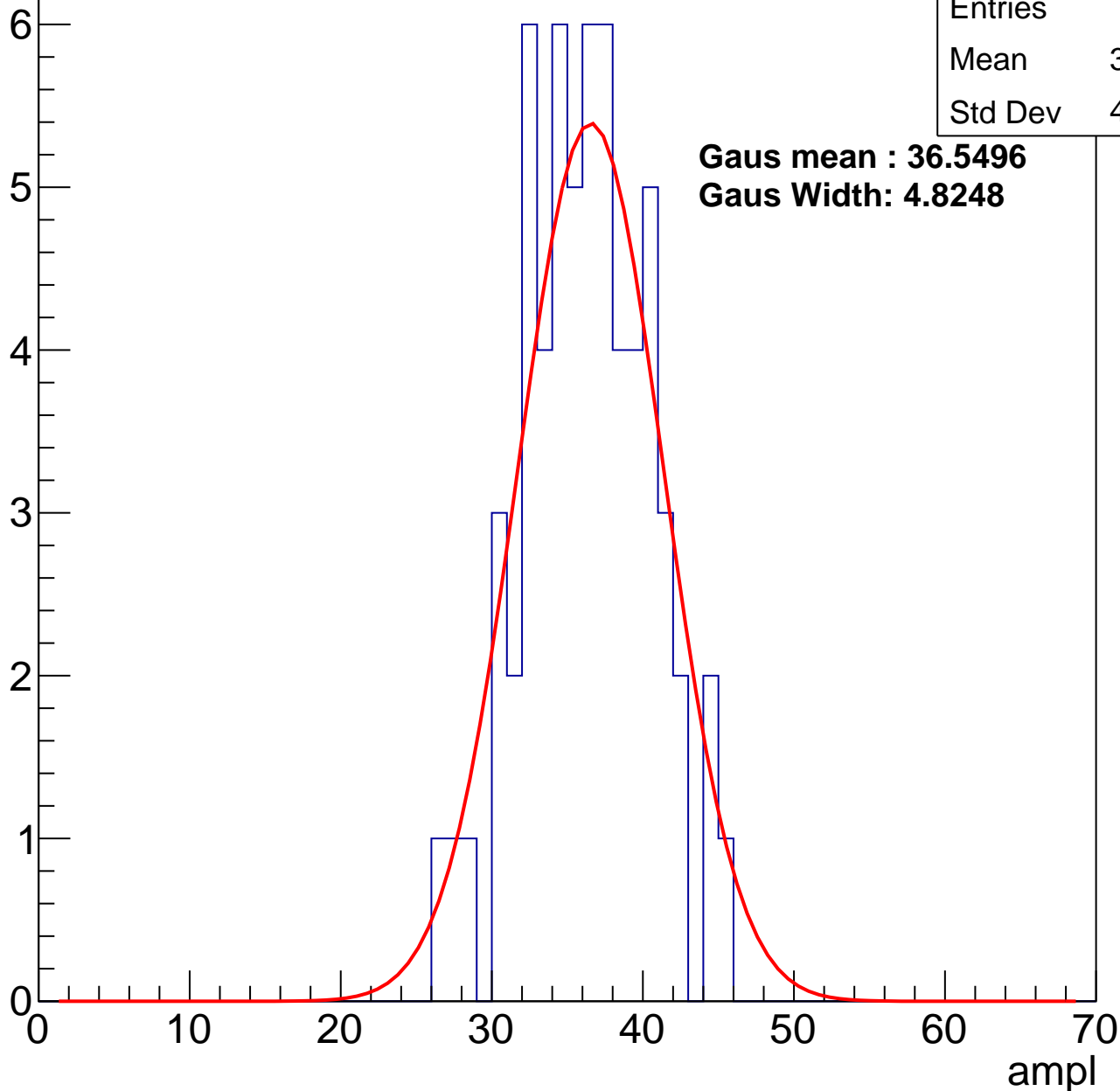
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	35.84
Std Dev	4.128

**Gaus mean : 36.5496**

**Gaus Width: 4.8248**



# B1L103S, U26-ch66, adc2

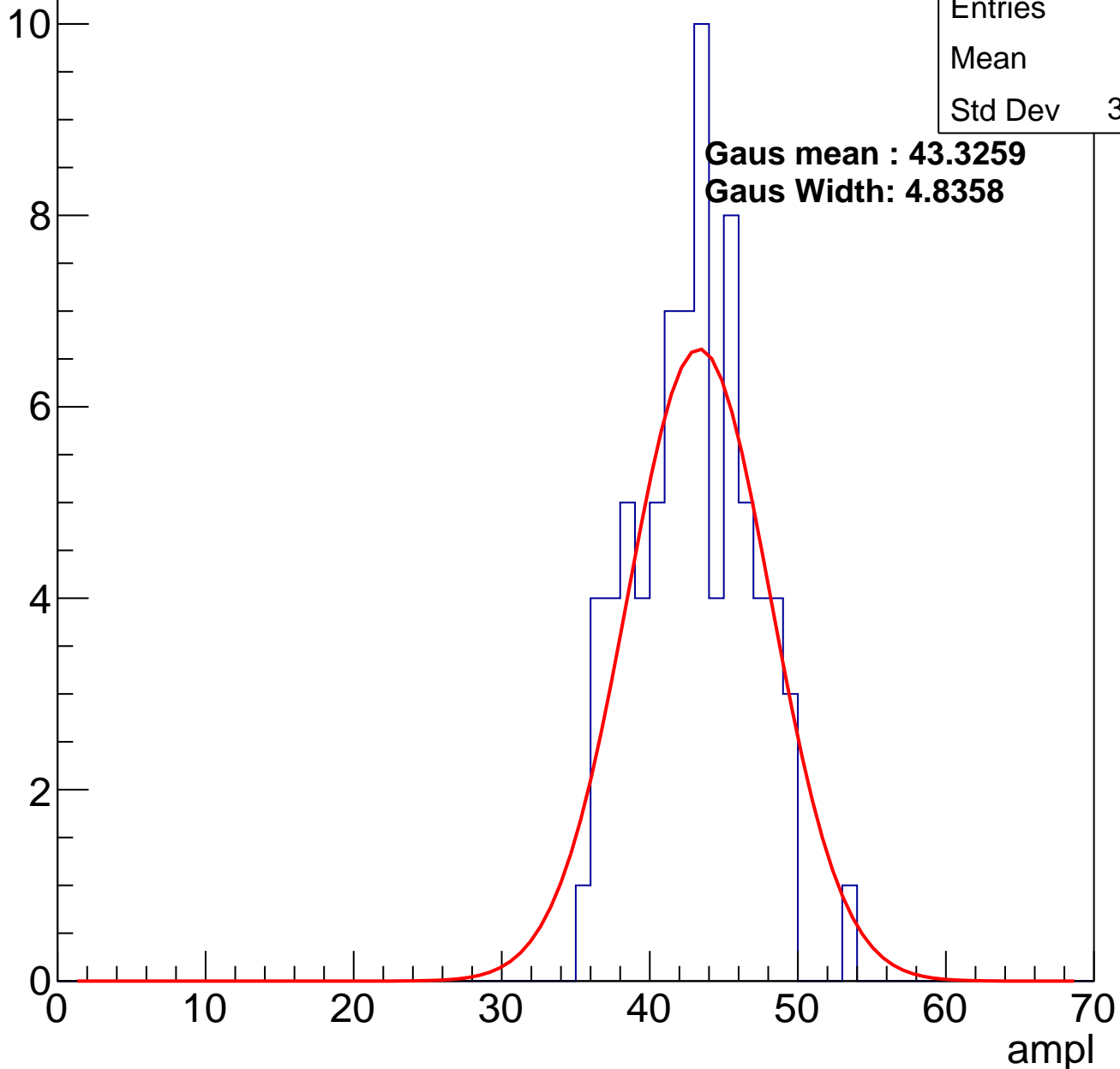
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	76
Mean	42.5
Std Dev	3.817

**Gaus mean : 43.3259**

**Gaus Width: 4.8358**

Entry

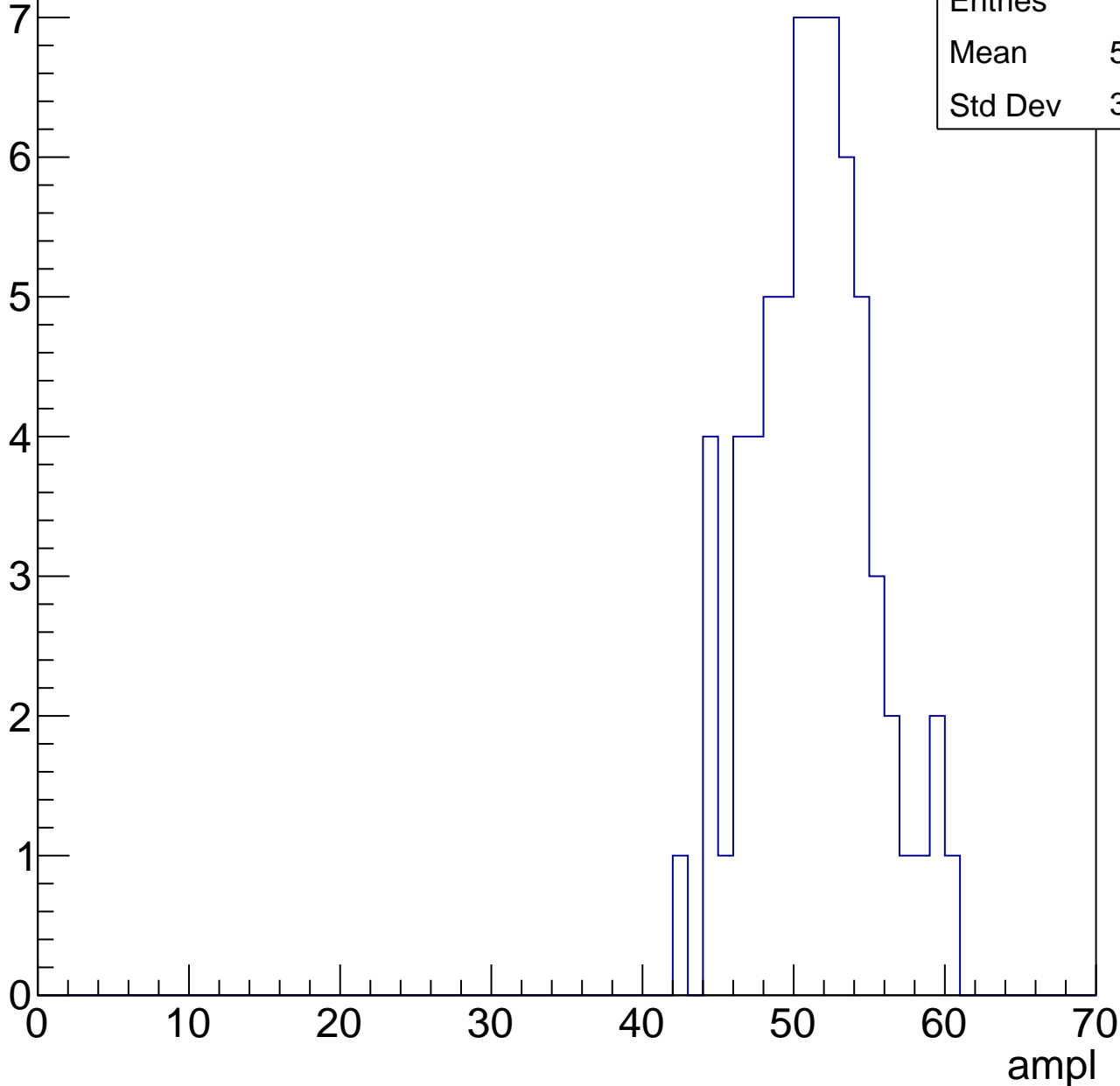


# B1L103S, U26-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	50.74
Std Dev	3.917

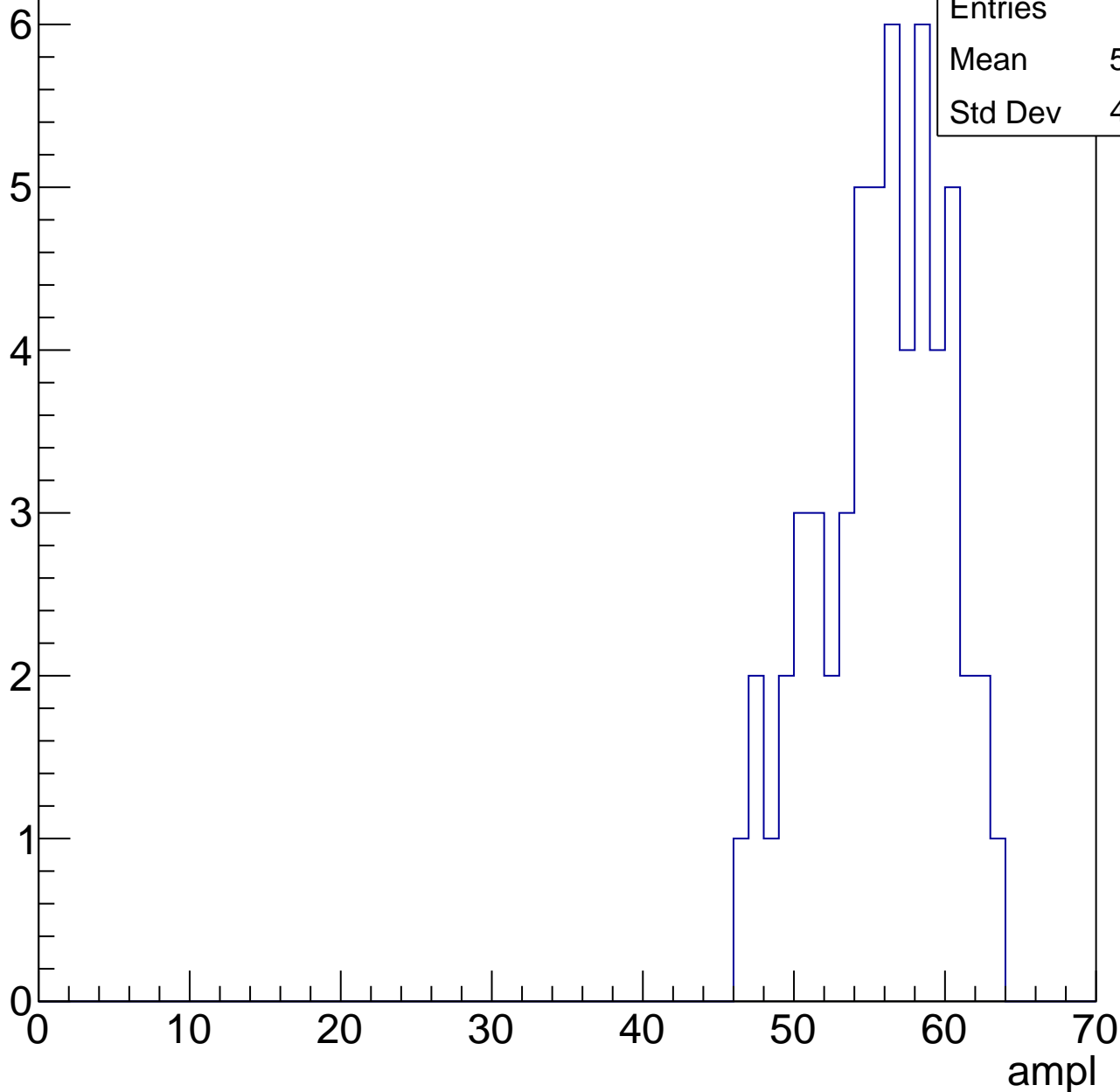


# B1L103S, U26-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	55.33
Std Dev	4.148

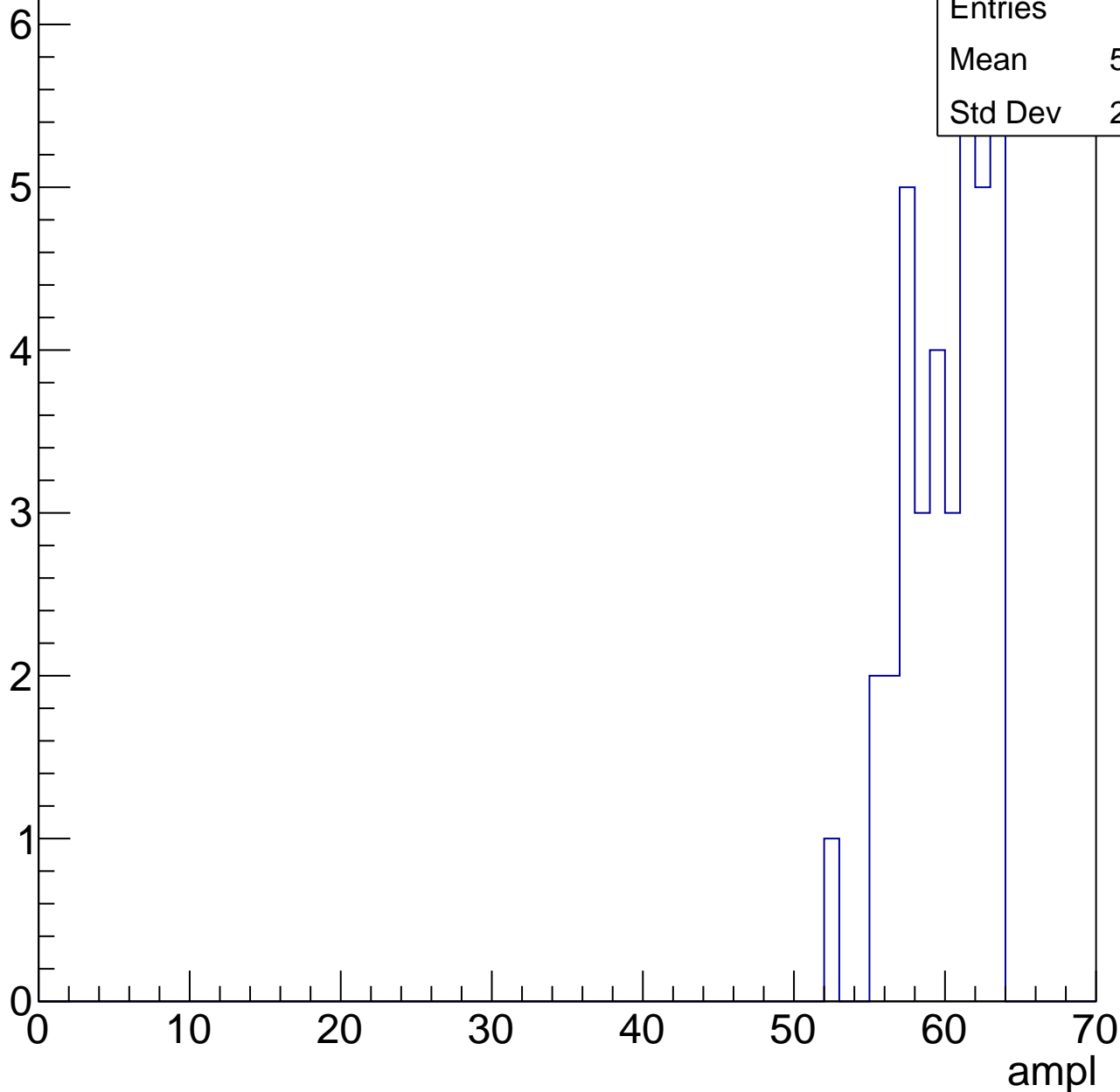


# B1L103S, U26-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

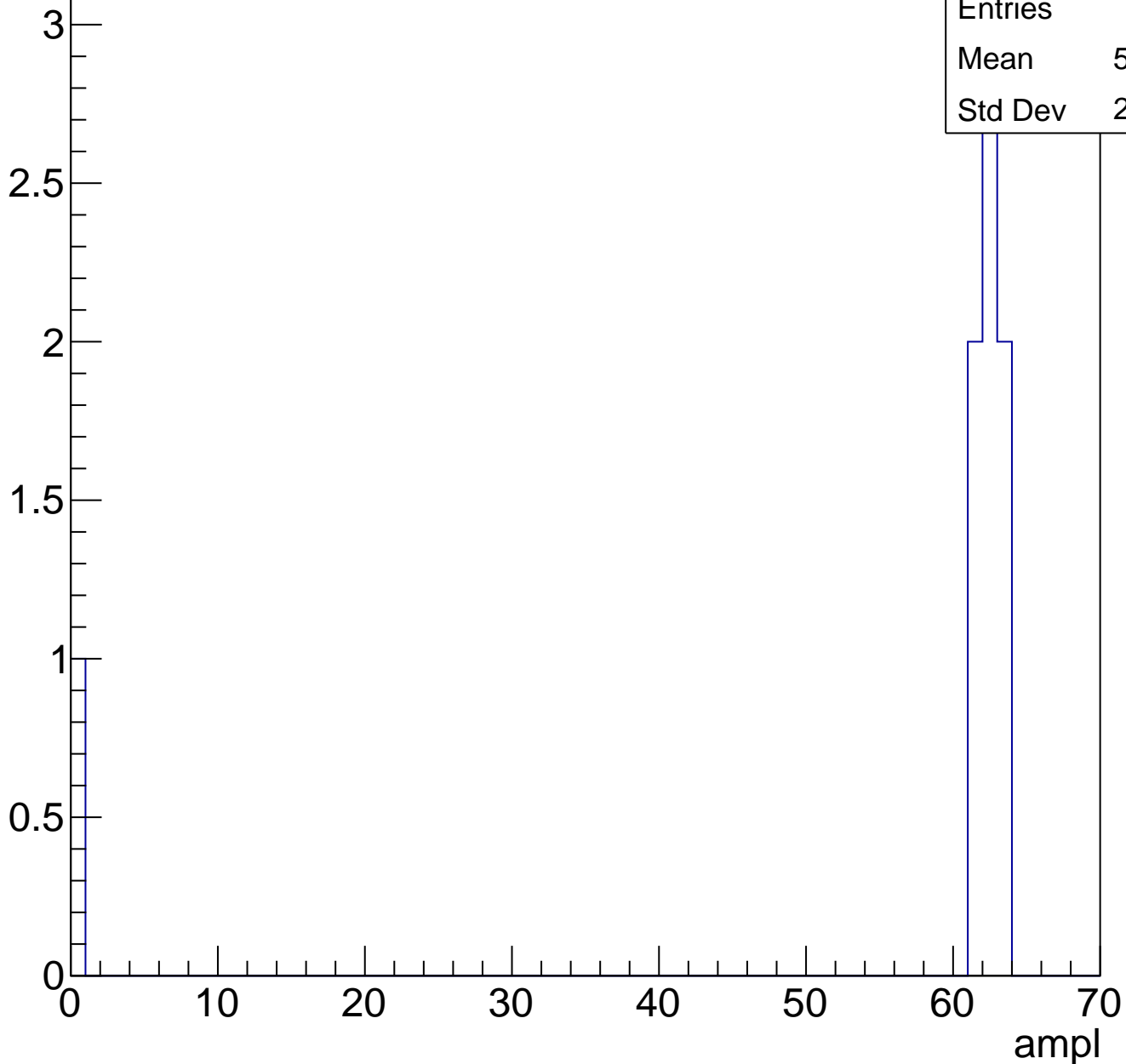
Entries	37
Mean	59.54
Std Dev	2.747



# B1L103S, U26-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



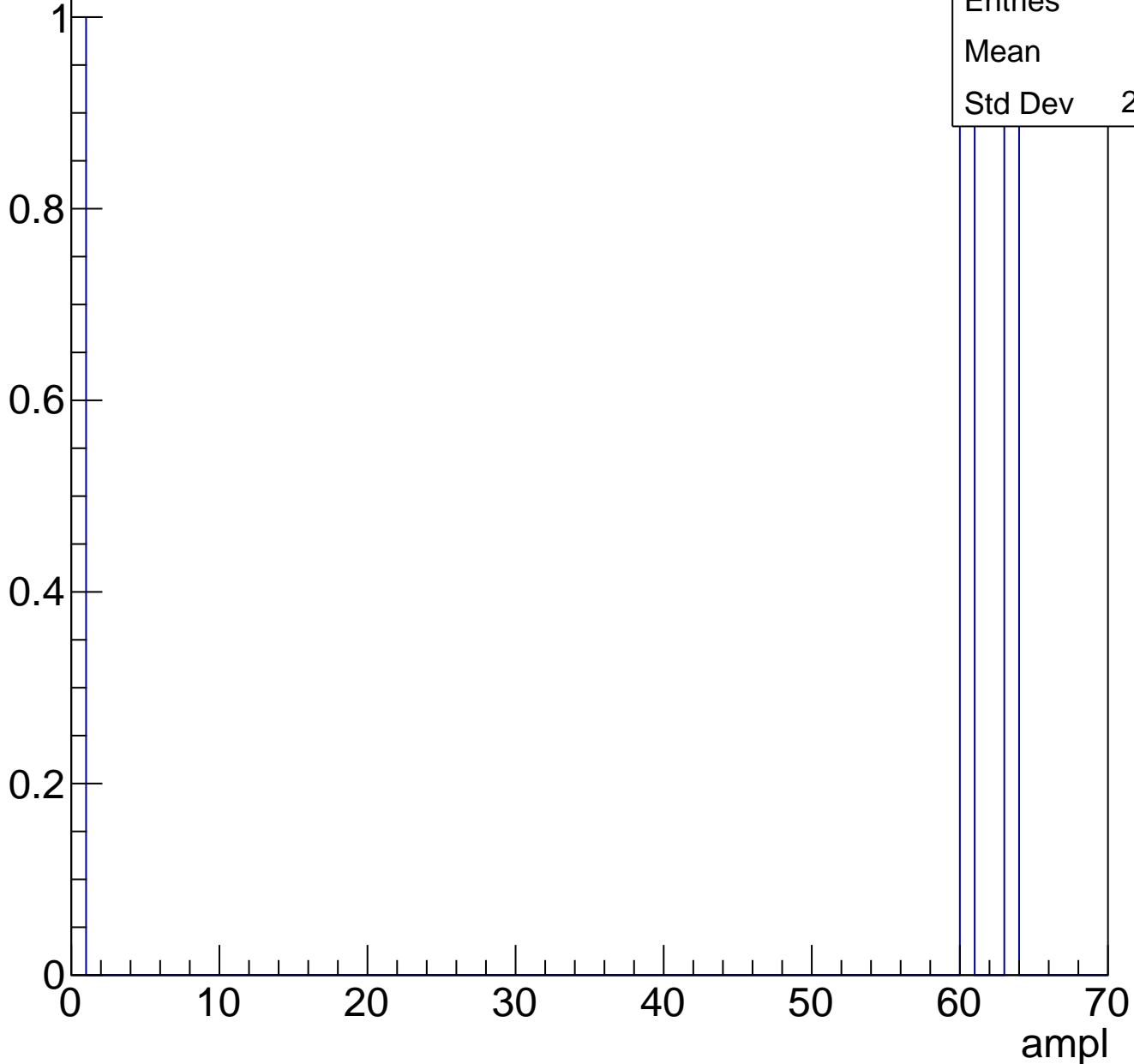
Entries	8
Mean	54.25
Std Dev	20.52



# B1L103S, U26-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch67, adc0

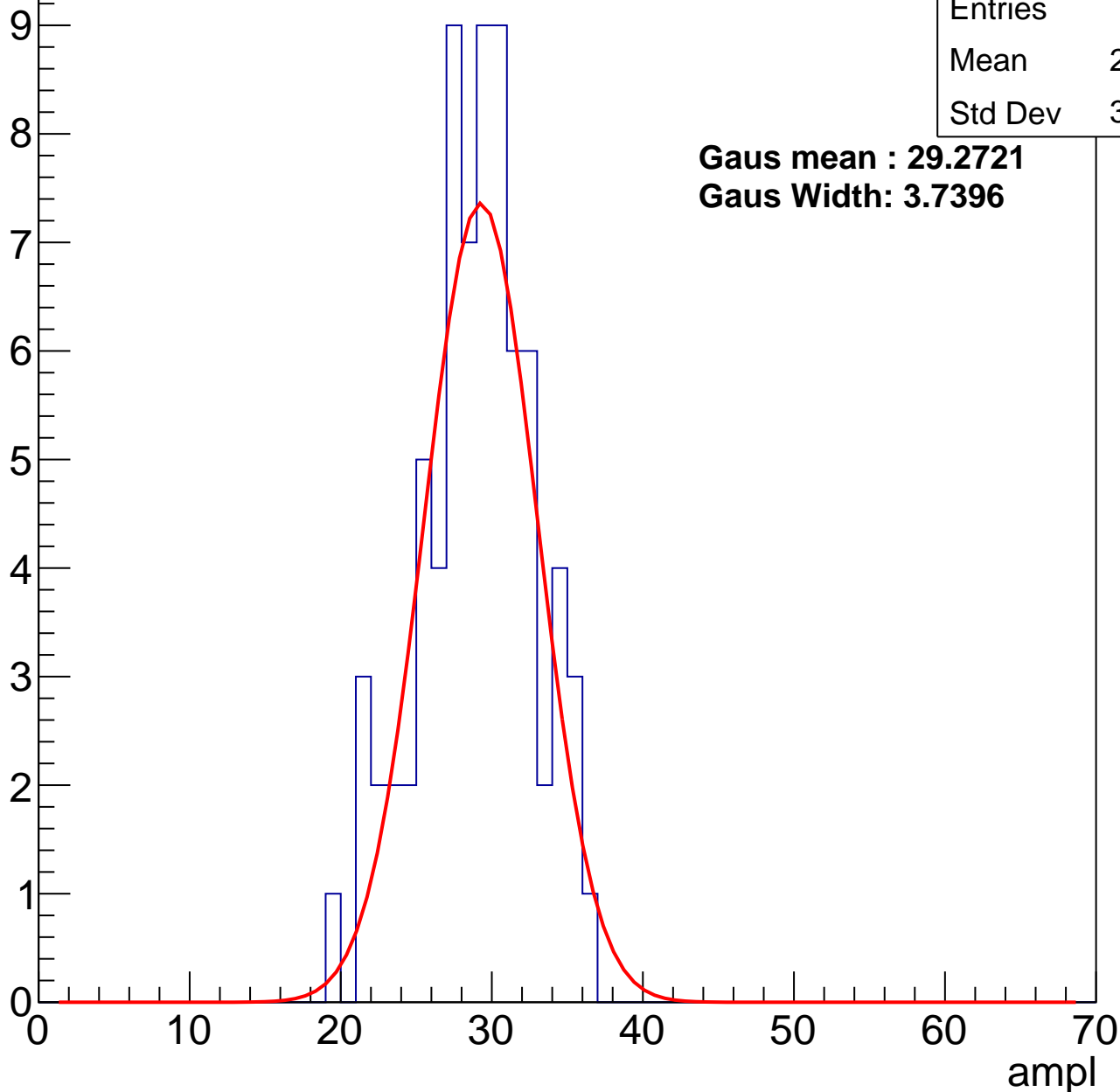
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	28.53
Std Dev	3.707

**Gaus mean : 29.2721**

**Gaus Width: 3.7396**



# B1L103S, U26-ch67, adc1

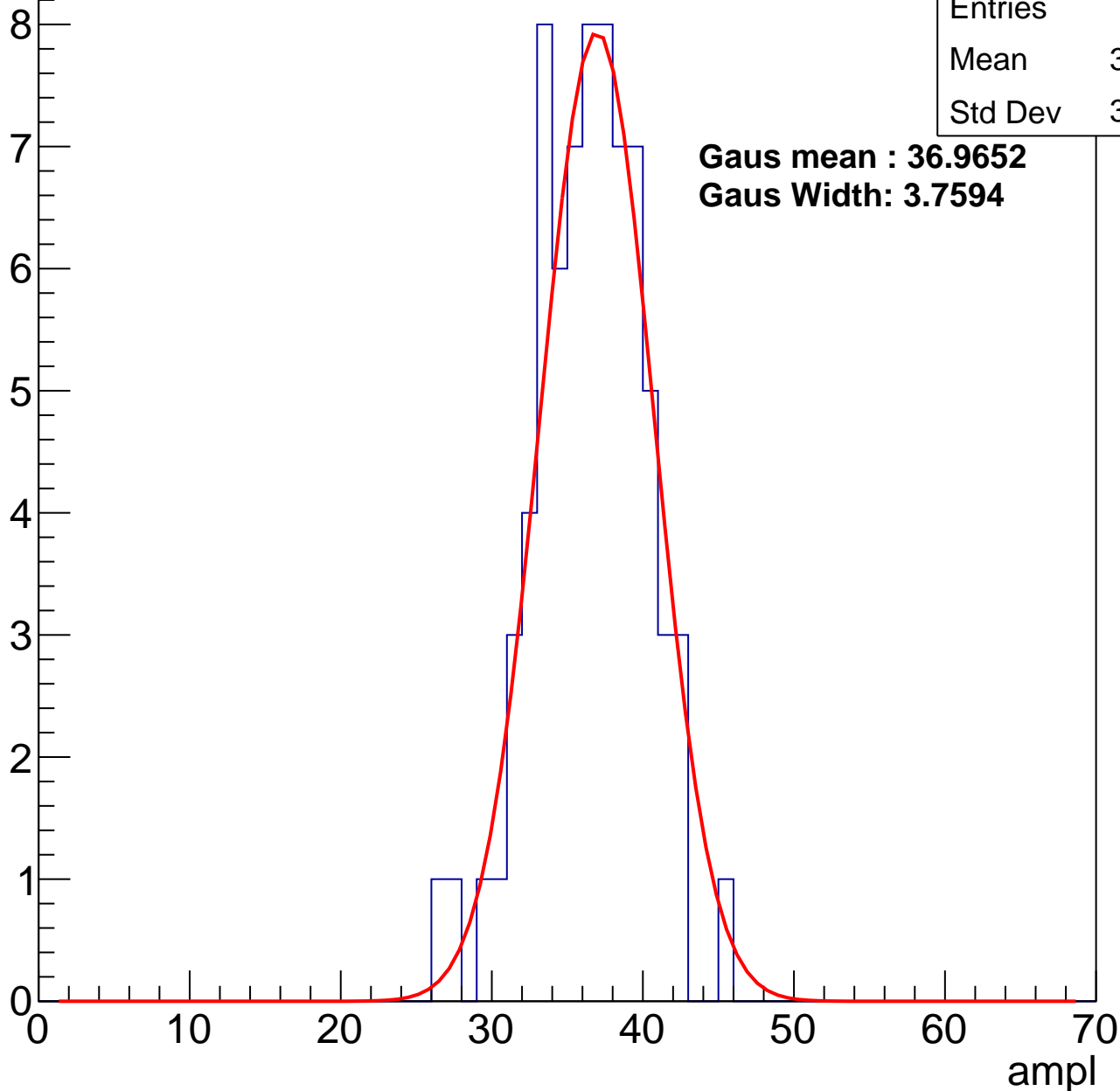
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	35.99
Std Dev	3.585

**Gaus mean : 36.9652**

**Gaus Width: 3.7594**



# B1L103S, U26-ch67, adc2

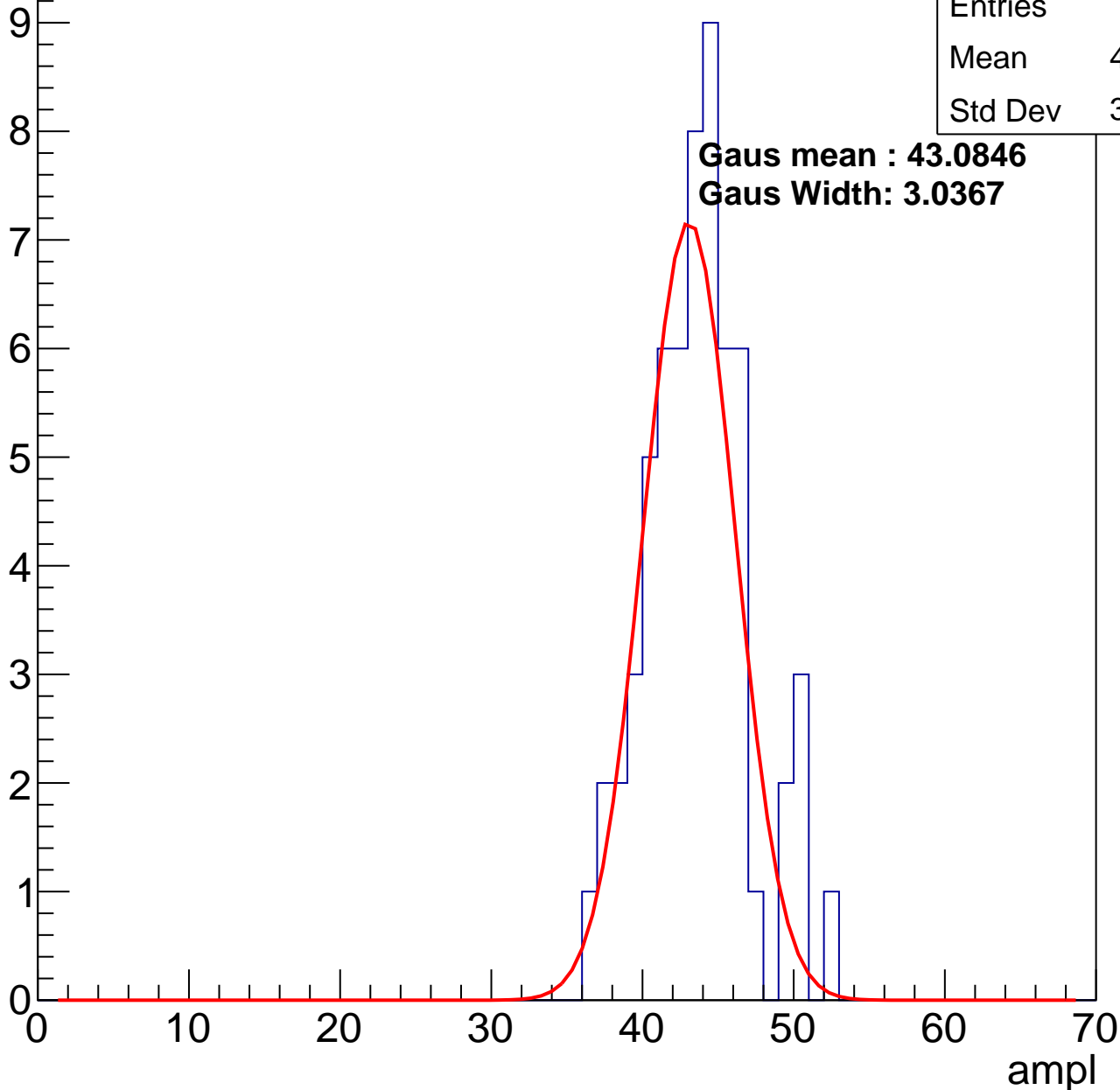
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	43.18
Std Dev	3.375

**Gaus mean : 43.0846**

**Gaus Width: 3.0367**

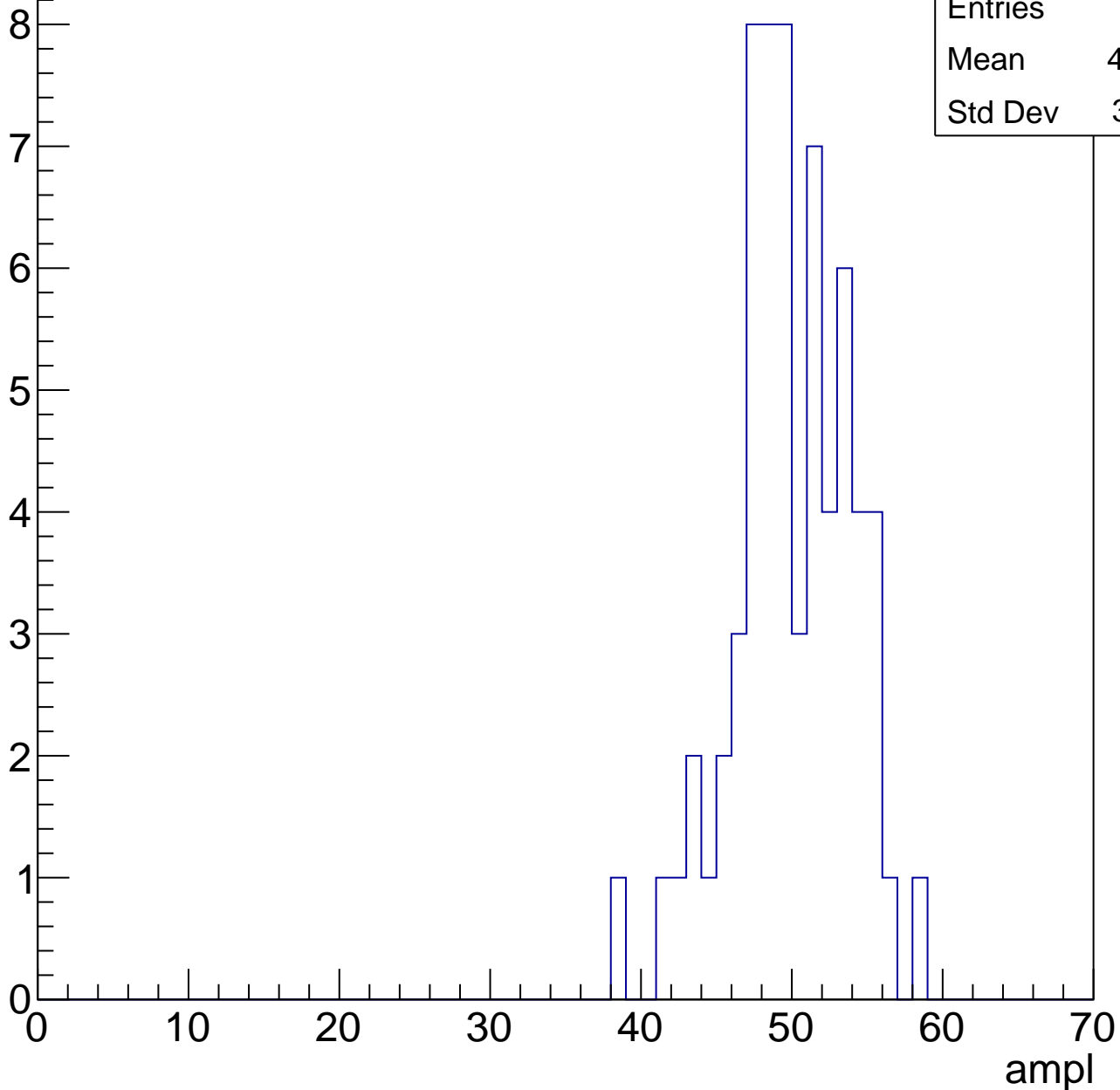


# B1L103S, U26-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	49.45
Std Dev	3.831

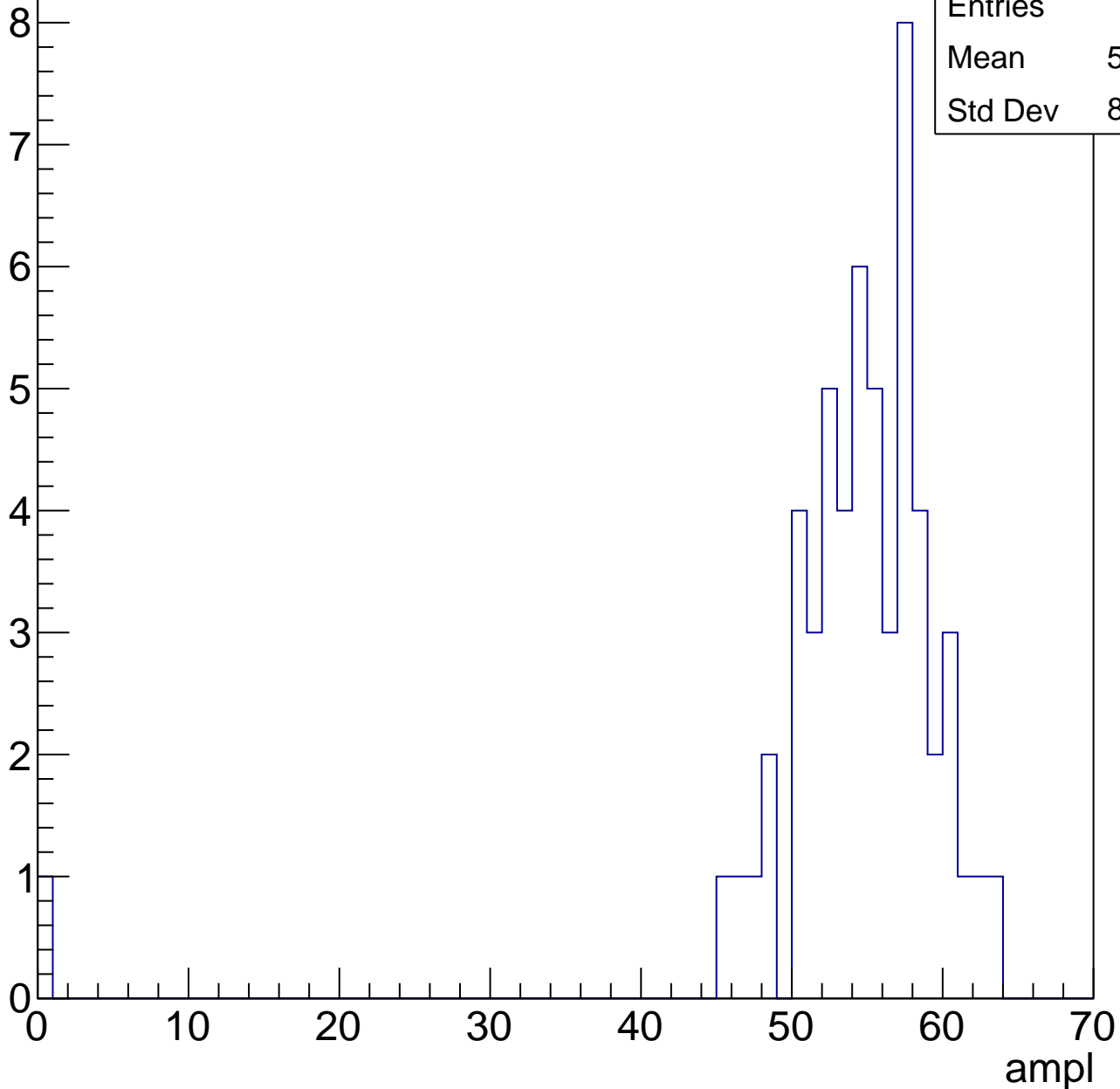


# B1L103S, U26-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

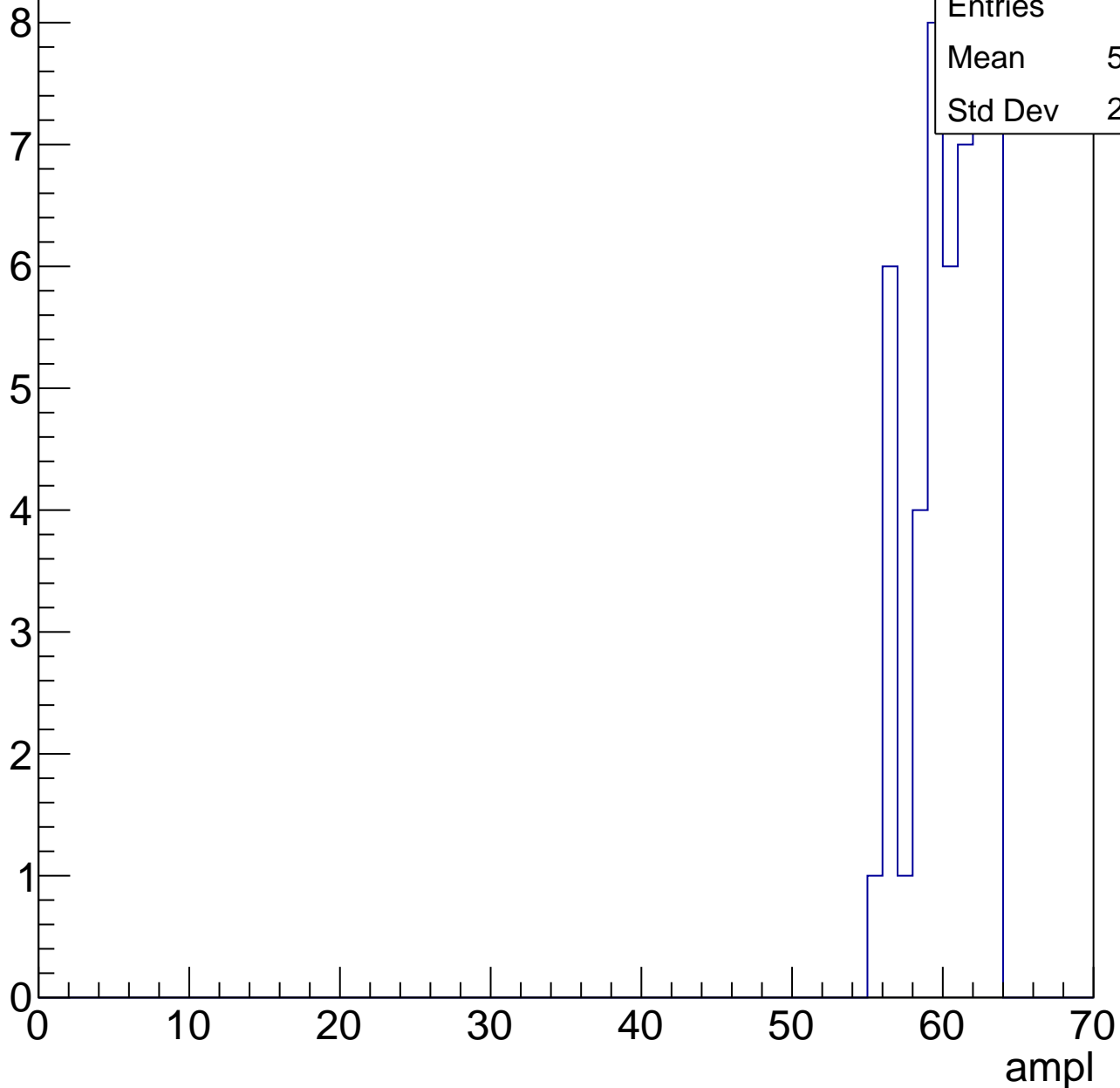
Entries	56
Mean	53.54
Std Dev	8.227



# B1L103S, U26-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	49
Mean	59.98
Std Dev	2.325

# B1L103S, U26-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

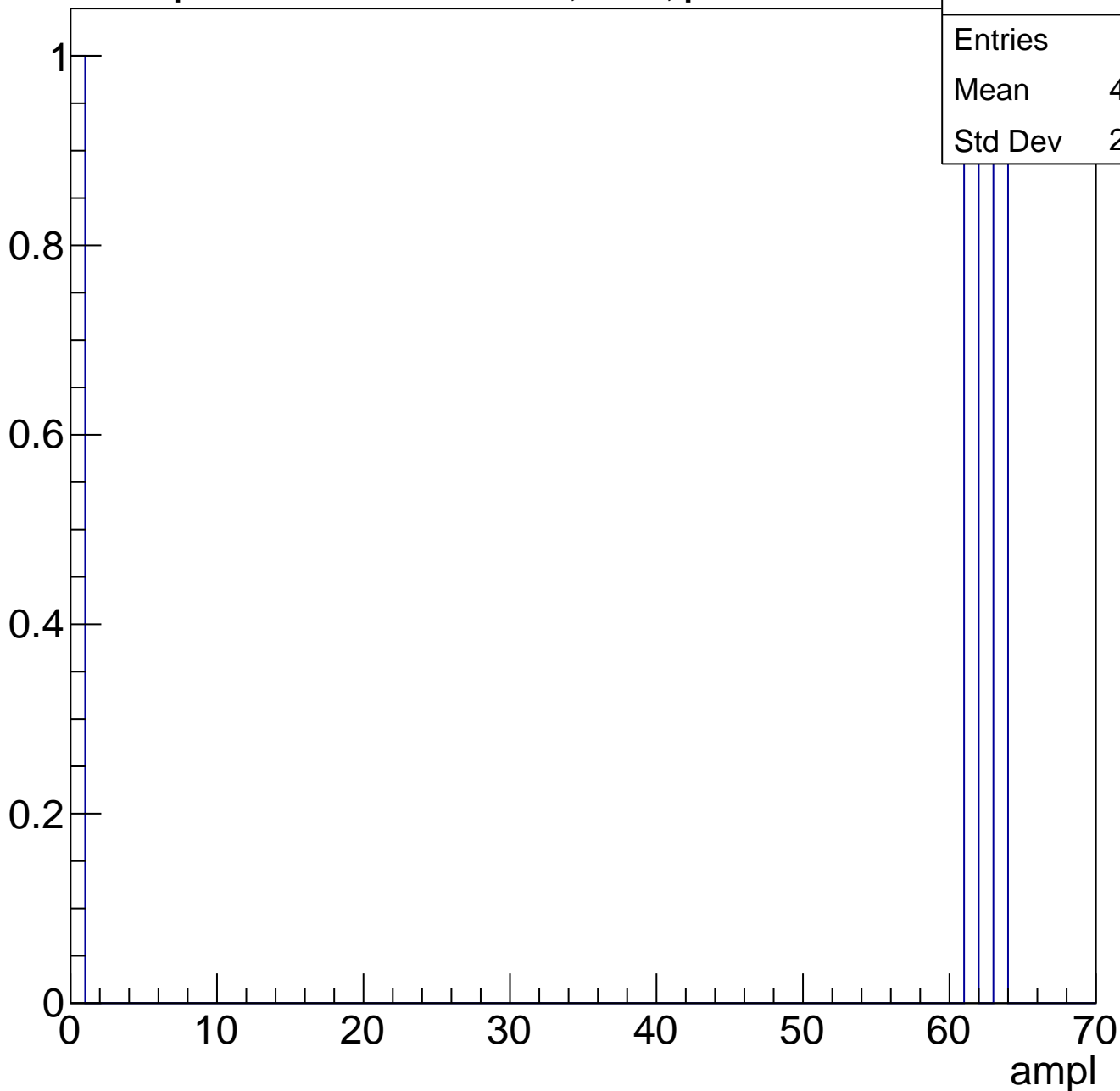
Entries	5
Mean	59.6
Std Dev	1.855



# B1L103S, U26-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch68, adc0

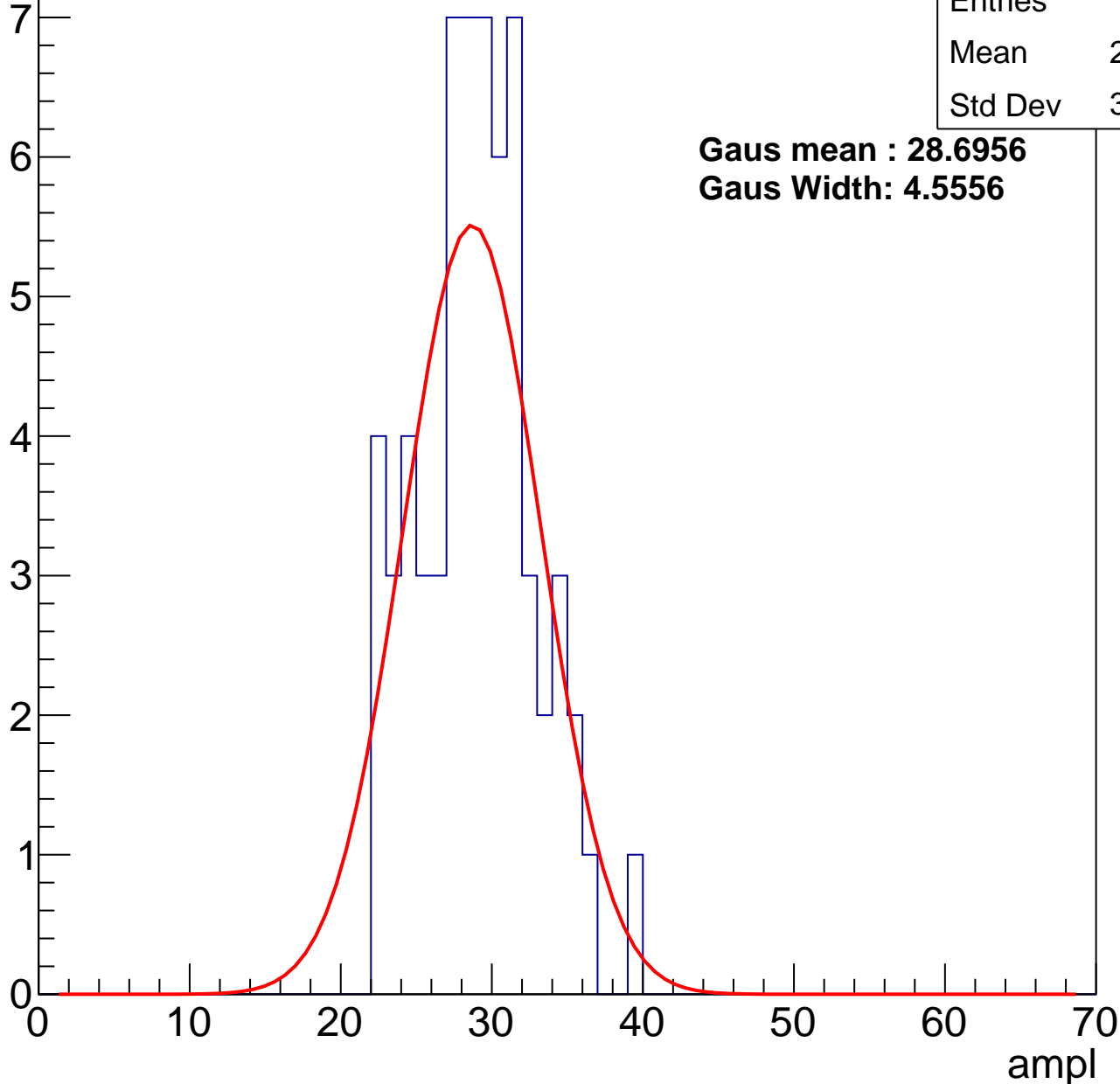
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	28.57
Std Dev	3.762

**Gaus mean : 28.6956**

**Gaus Width: 4.5556**



# B1L103S, U26-ch68, adc1

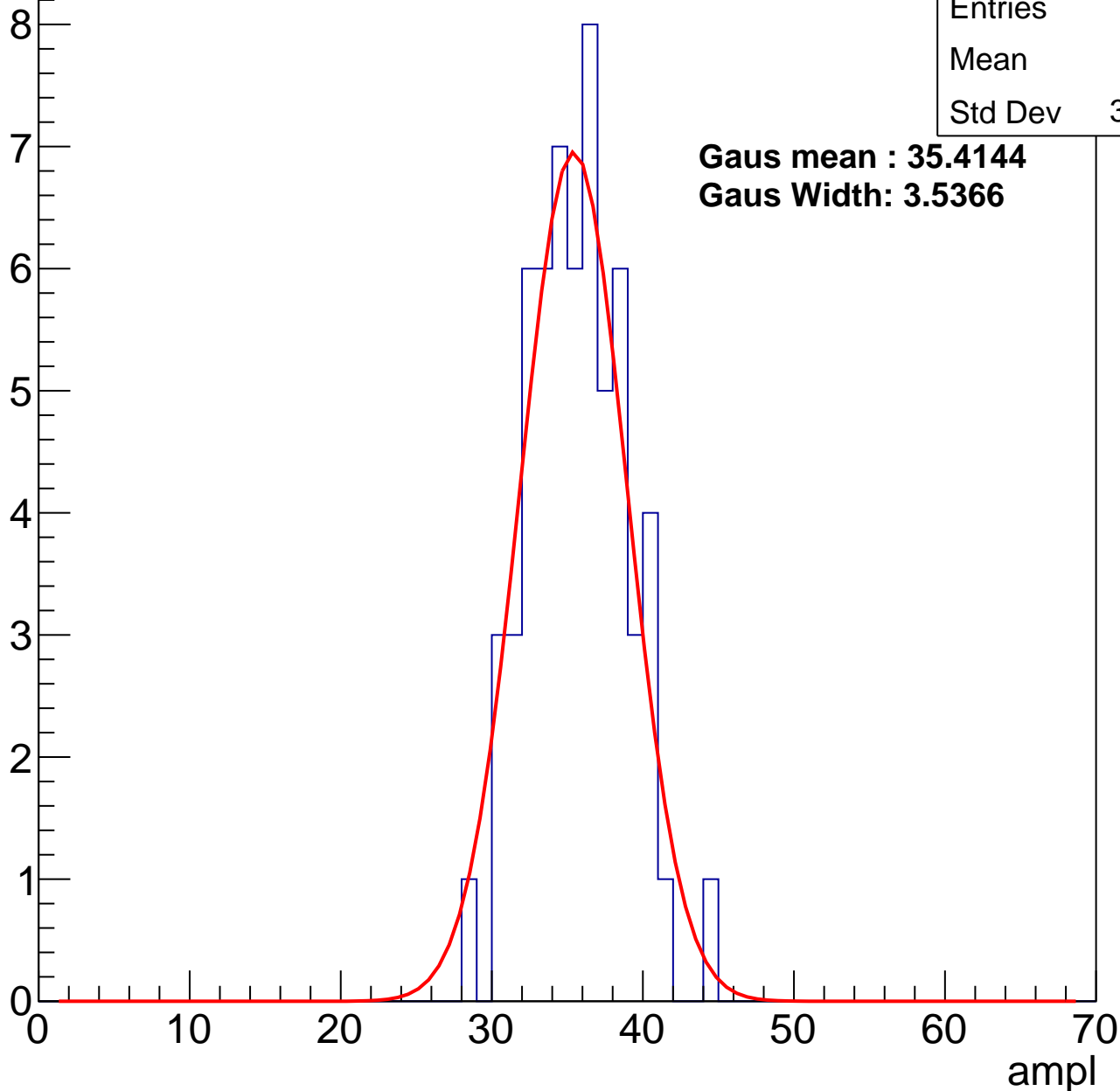
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	35.2
Std Dev	3.166

**Gaus mean : 35.4144**

**Gaus Width: 3.5366**



# B1L103S, U26-ch68, adc2

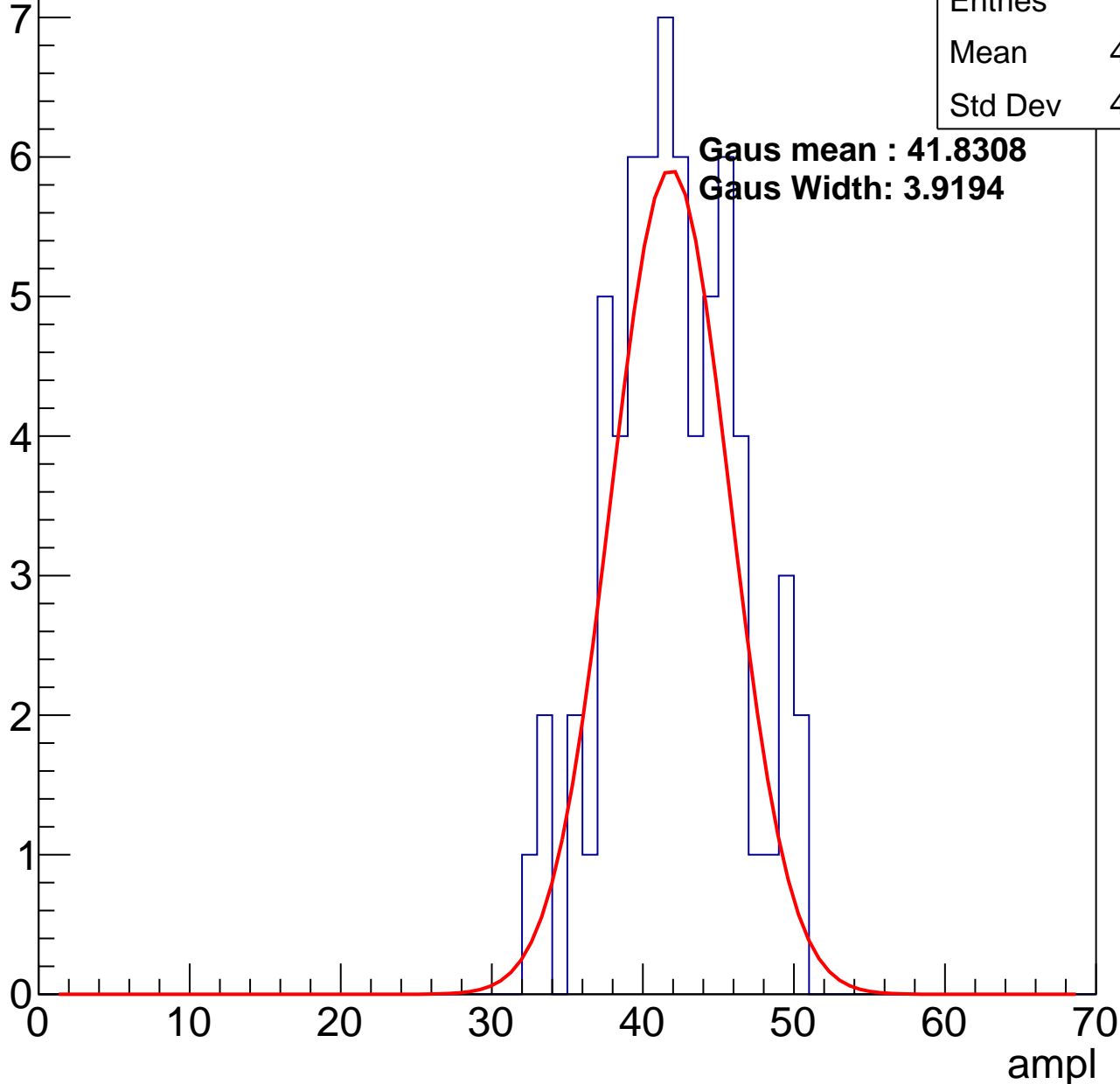
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	41.55
Std Dev	4.146

**Gaus mean : 41.8308**

**Gaus Width: 3.9194**

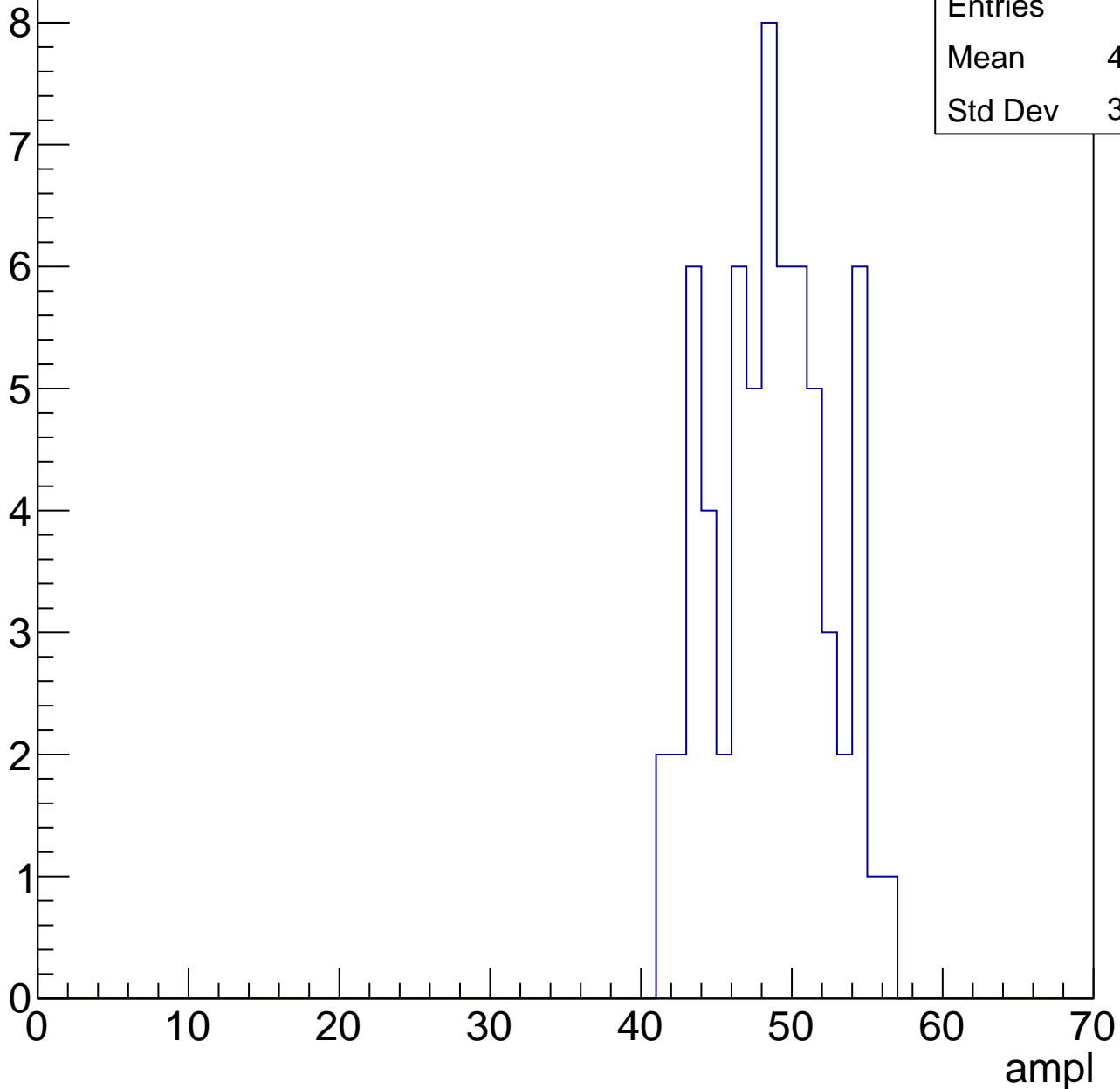


# B1L103S, U26-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	48.17
Std Dev	3.785

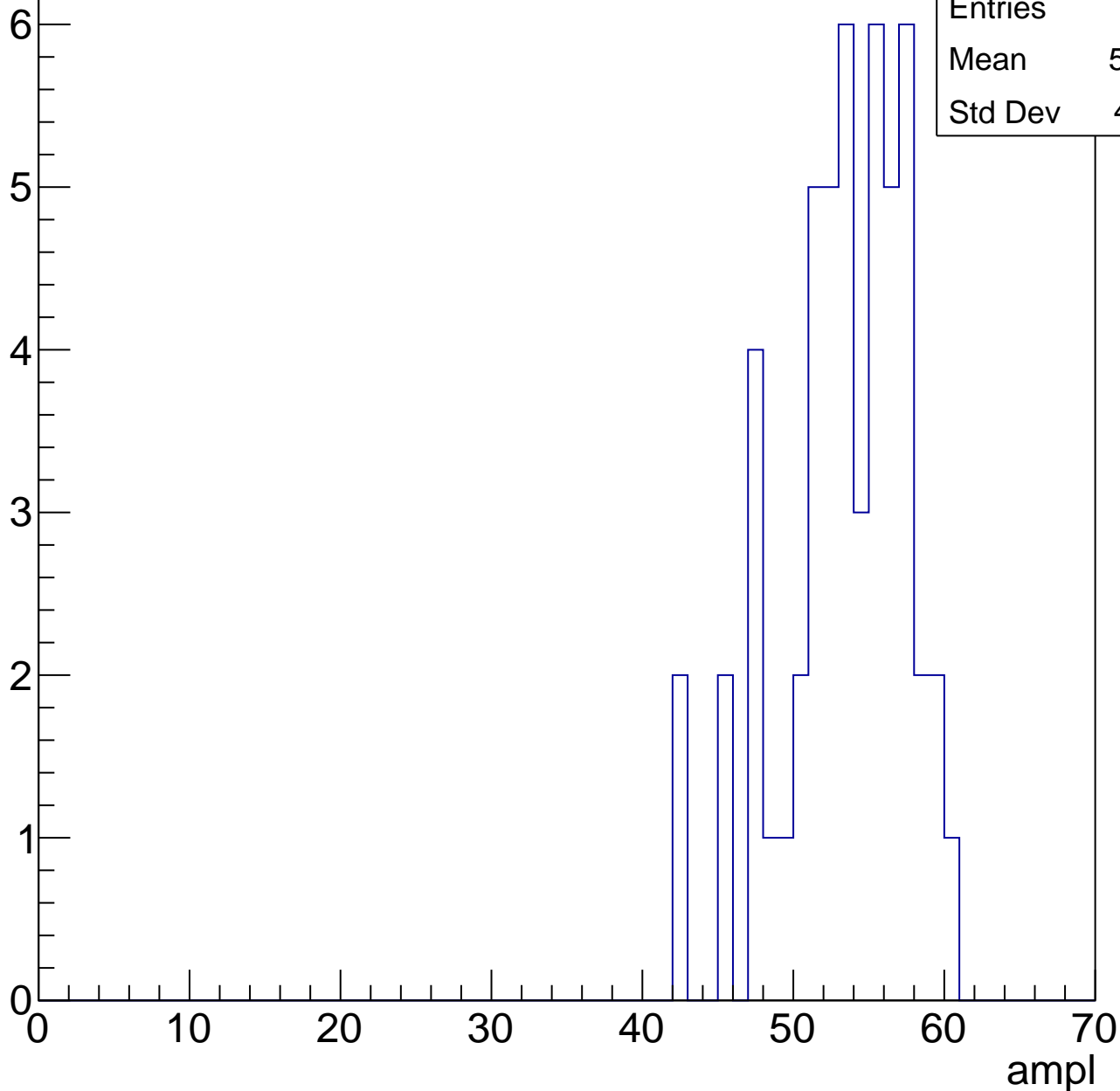


# B1L103S, U26-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

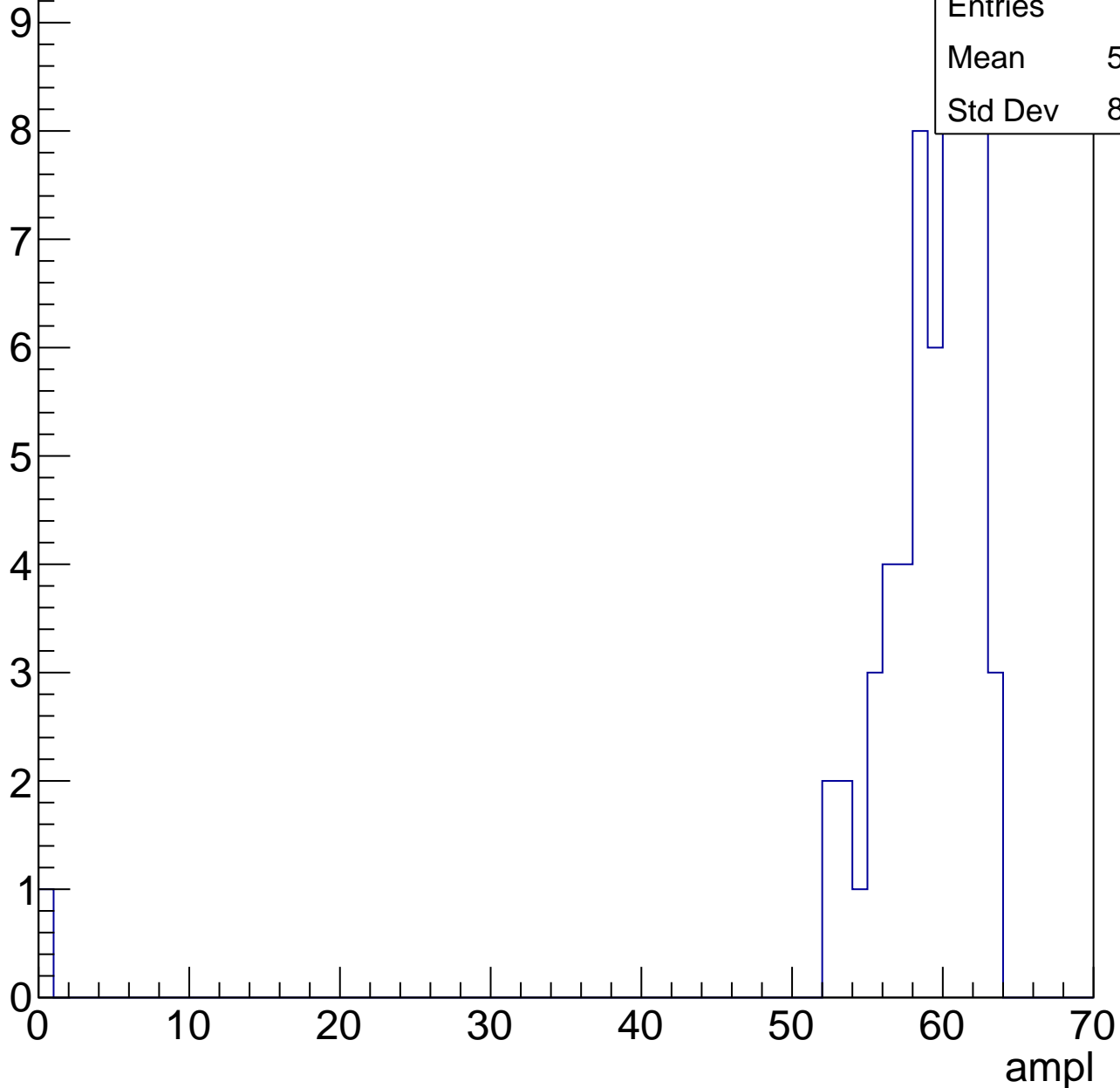
Entries	53
Mean	52.83
Std Dev	4.201



# B1L103S, U26-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

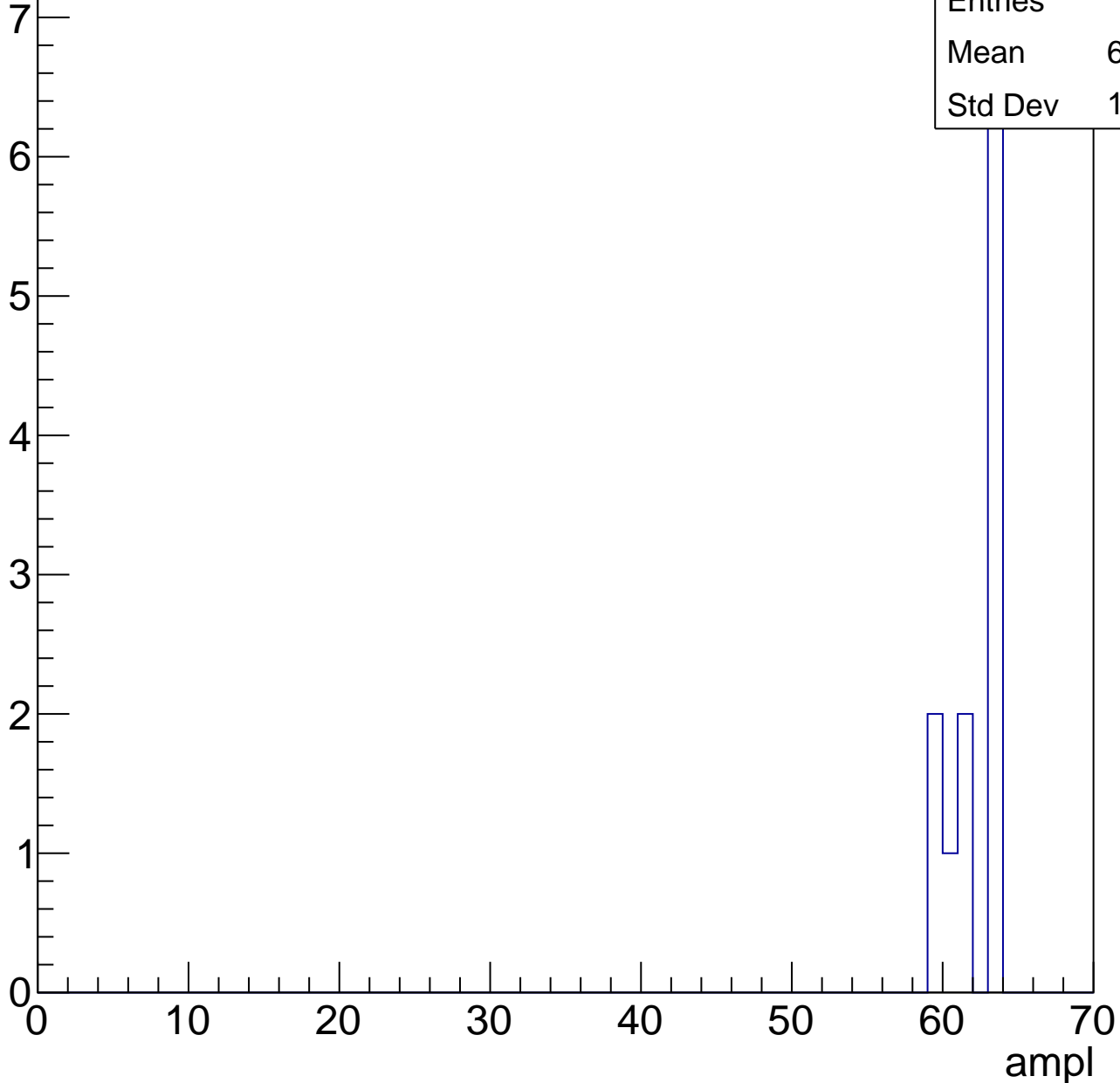


# B1L103S, U26-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	12
Mean	61.75
Std Dev	1.588





# B1L103S, U26-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch69, adc0

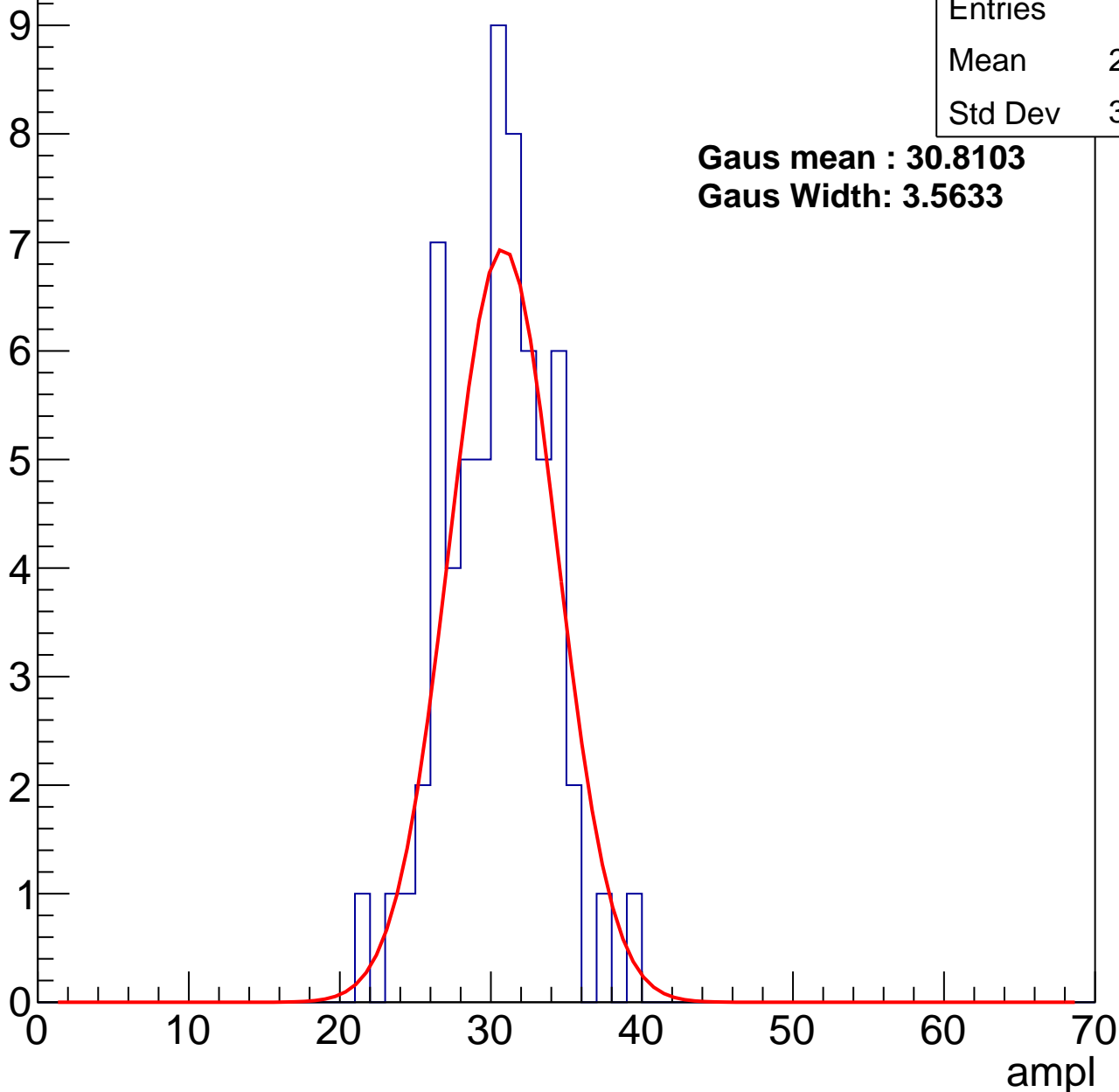
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	29.97
Std Dev	3.405

**Gaus mean : 30.8103**

**Gaus Width: 3.5633**

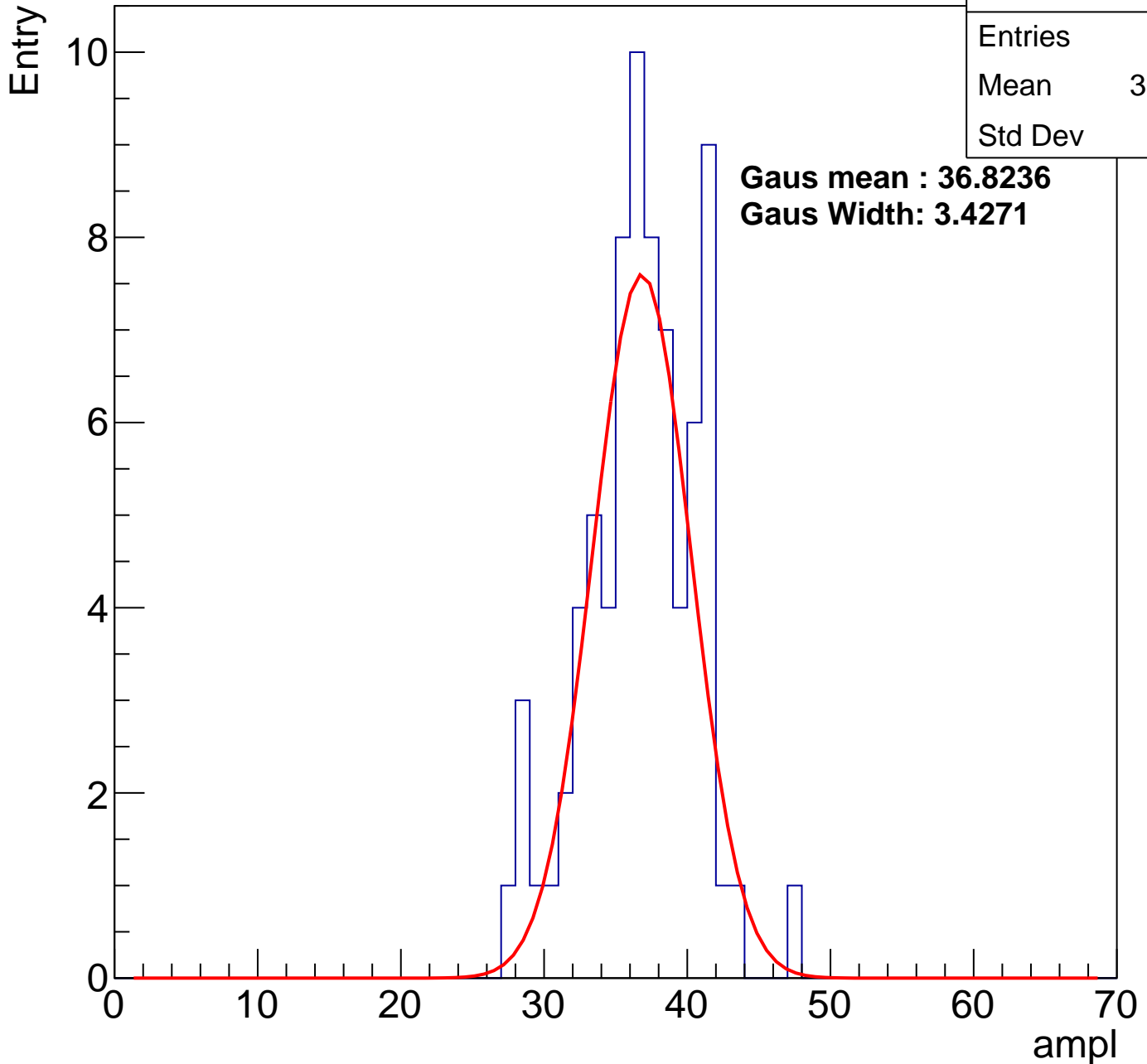


# B1L103S, U26-ch69, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	76
Mean	36.32
Std Dev	3.86

**Gaus mean : 36.8236**  
**Gaus Width: 3.4271**



# B1L103S, U26-ch69, adc2

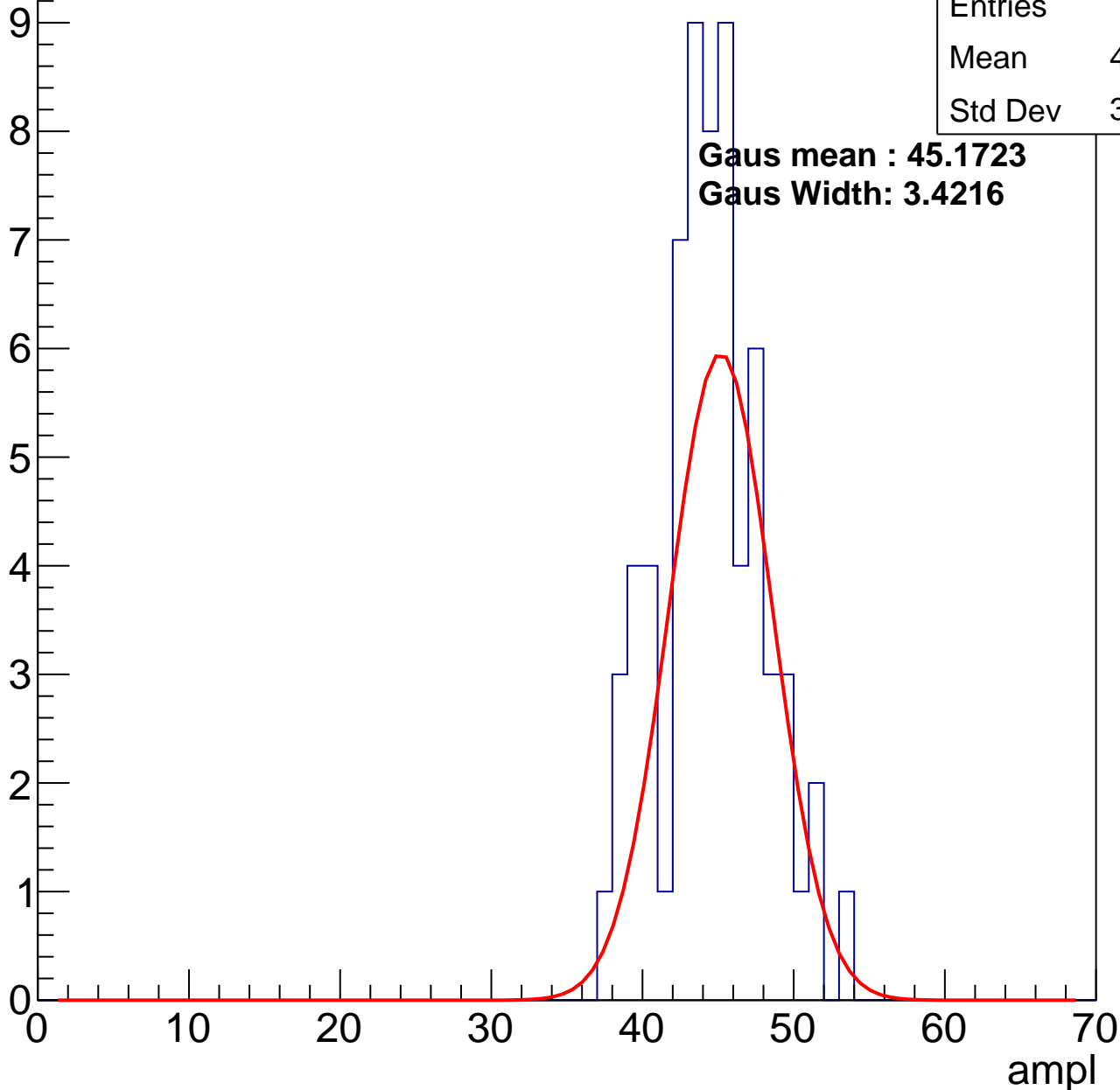
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	44.06
Std Dev	3.446

**Gaus mean : 45.1723**

**Gaus Width: 3.4216**

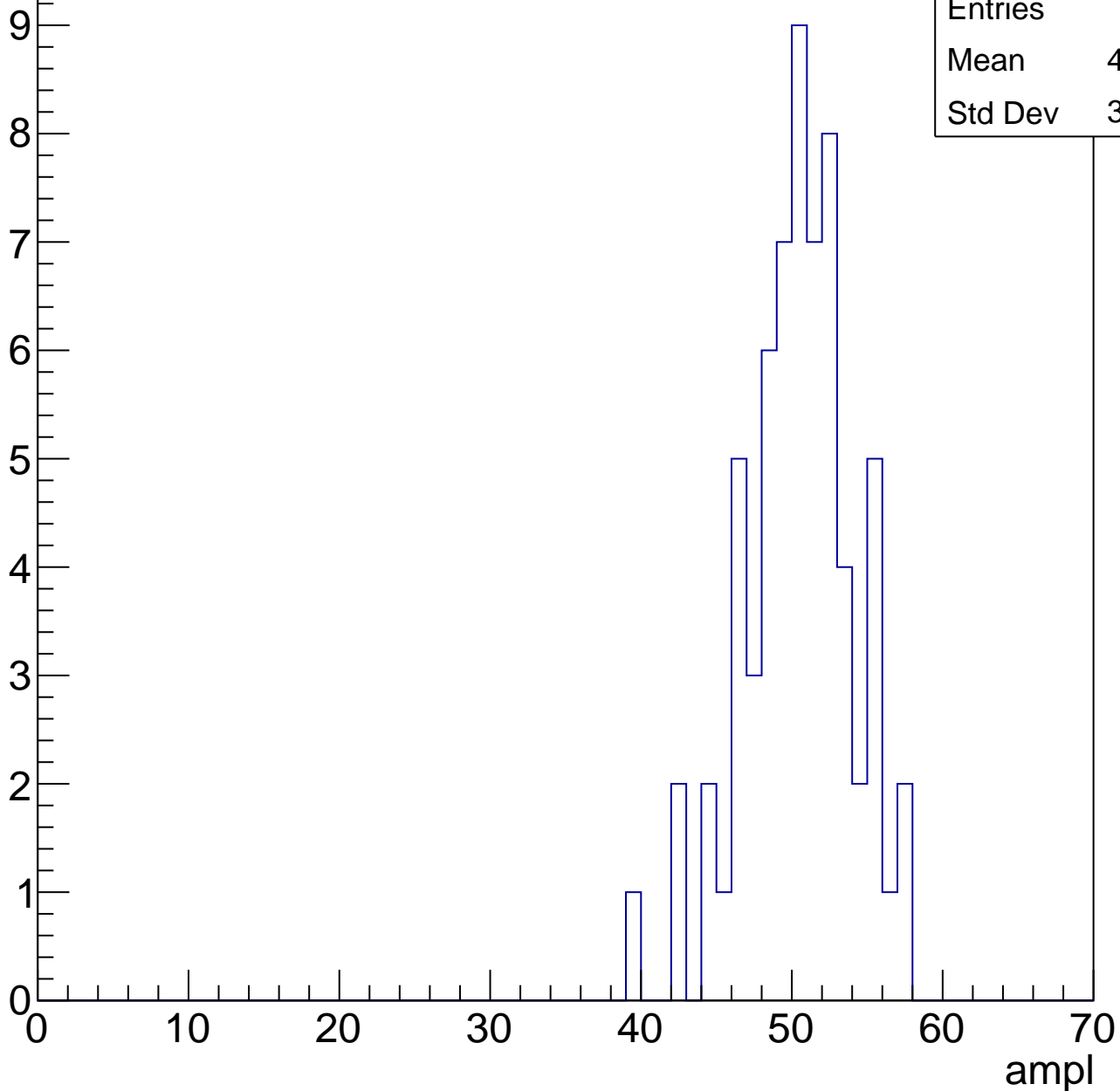


# B1L103S, U26-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	49.94
Std Dev	3.616

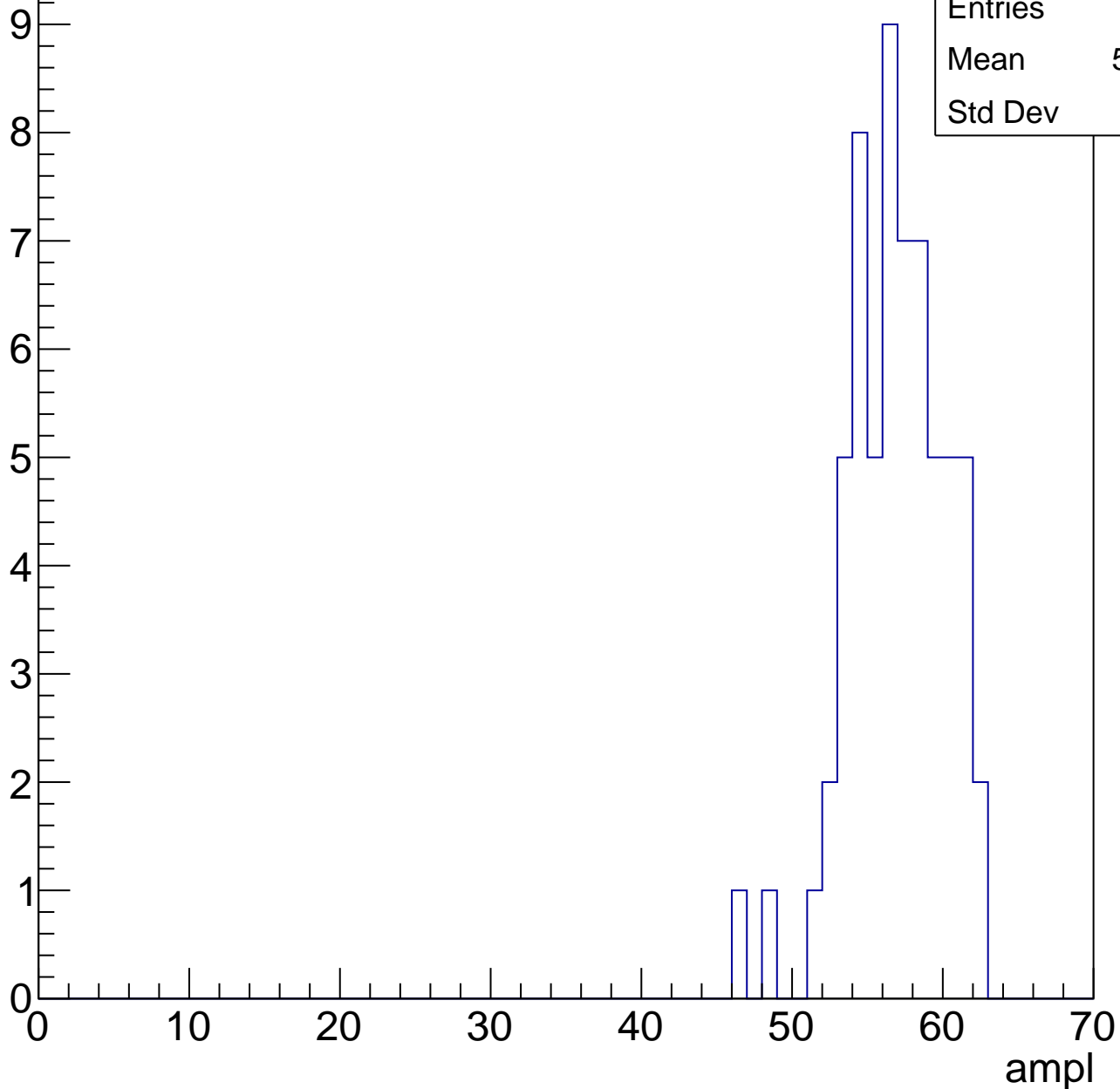


# B1L103S, U26-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	56.41
Std Dev	3.21

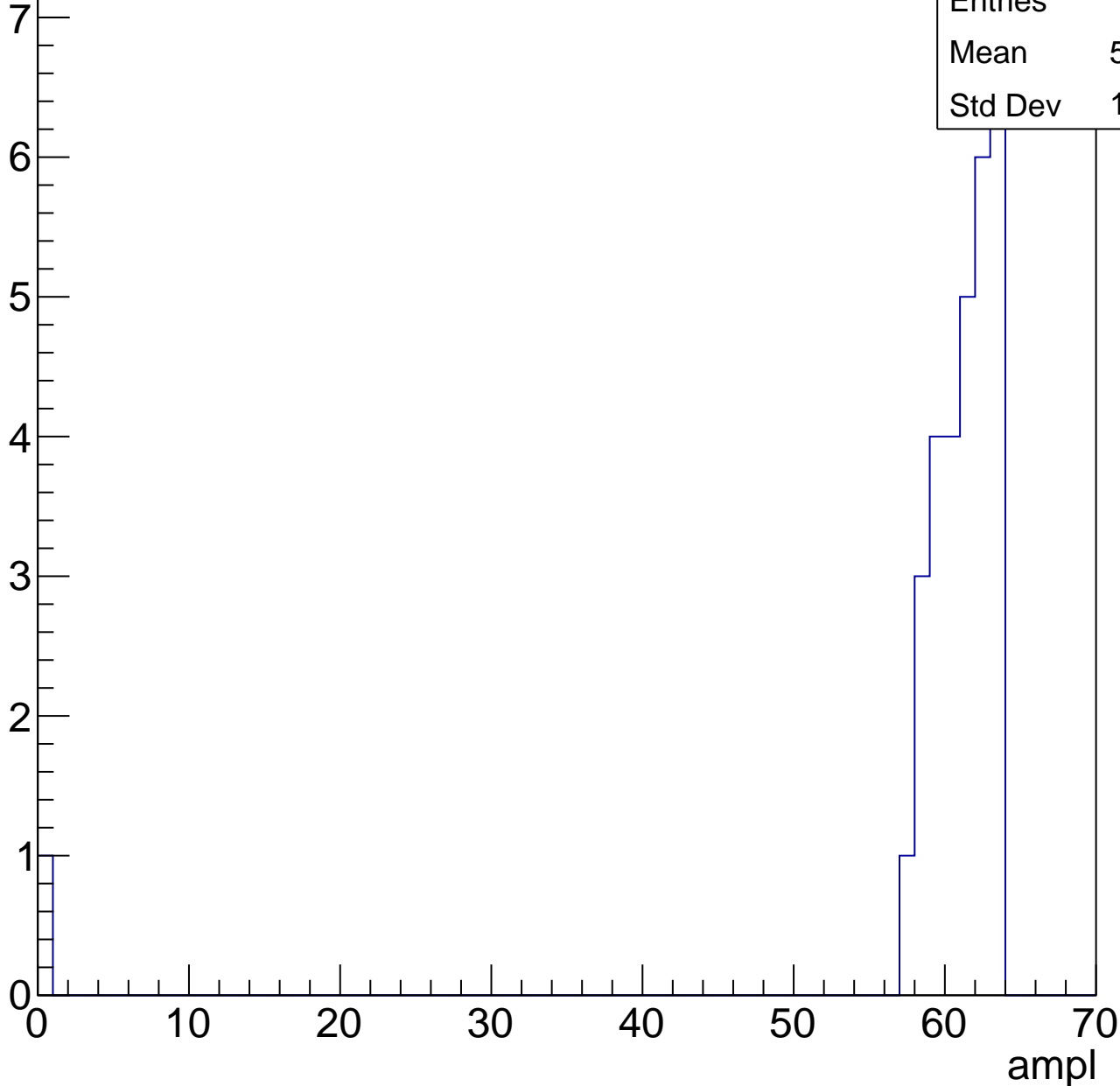


# B1L103S, U26-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

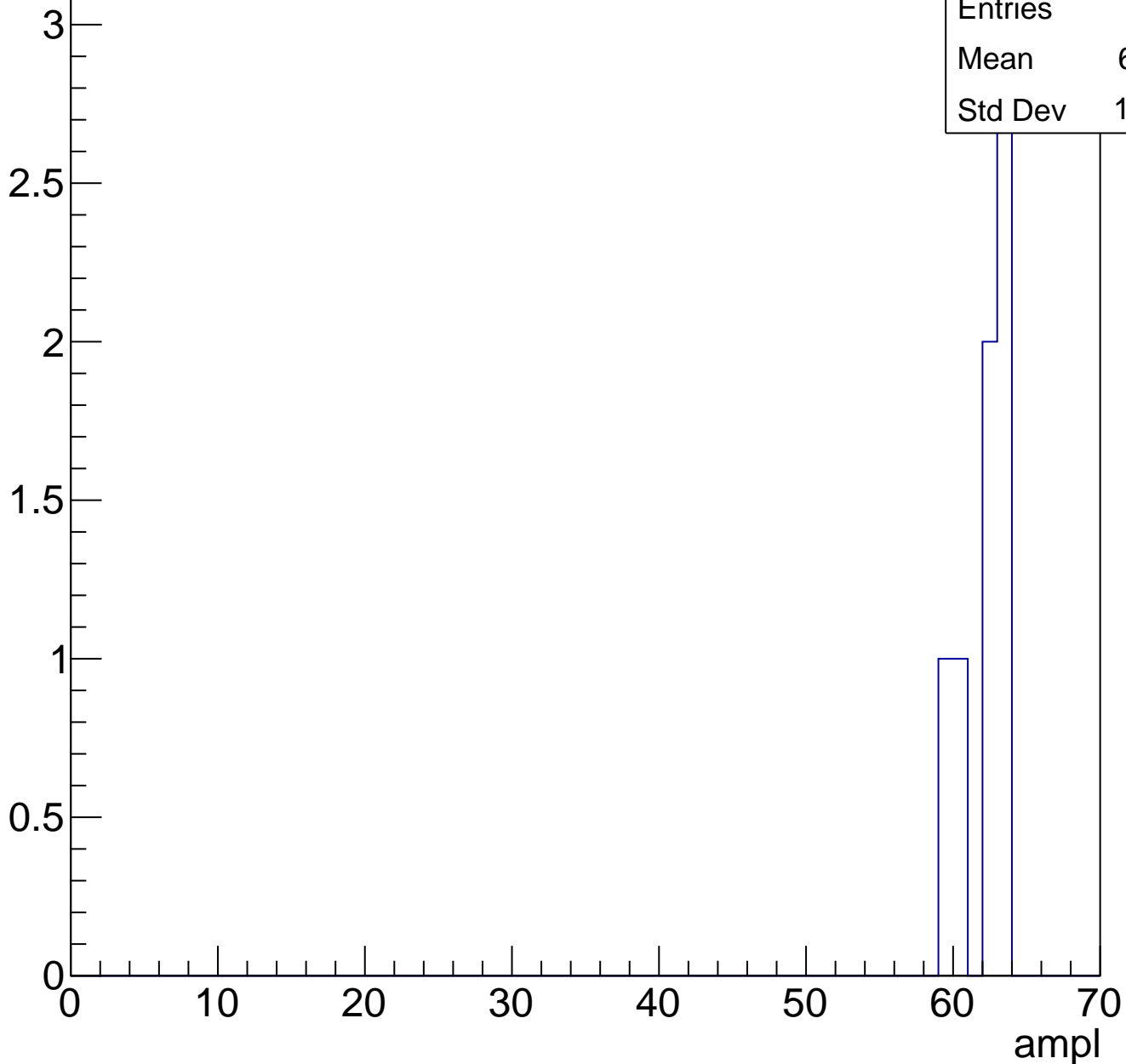
Entries	31
Mean	58.87
Std Dev	10.89



# B1L103S, U26-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U26-ch70, adc0

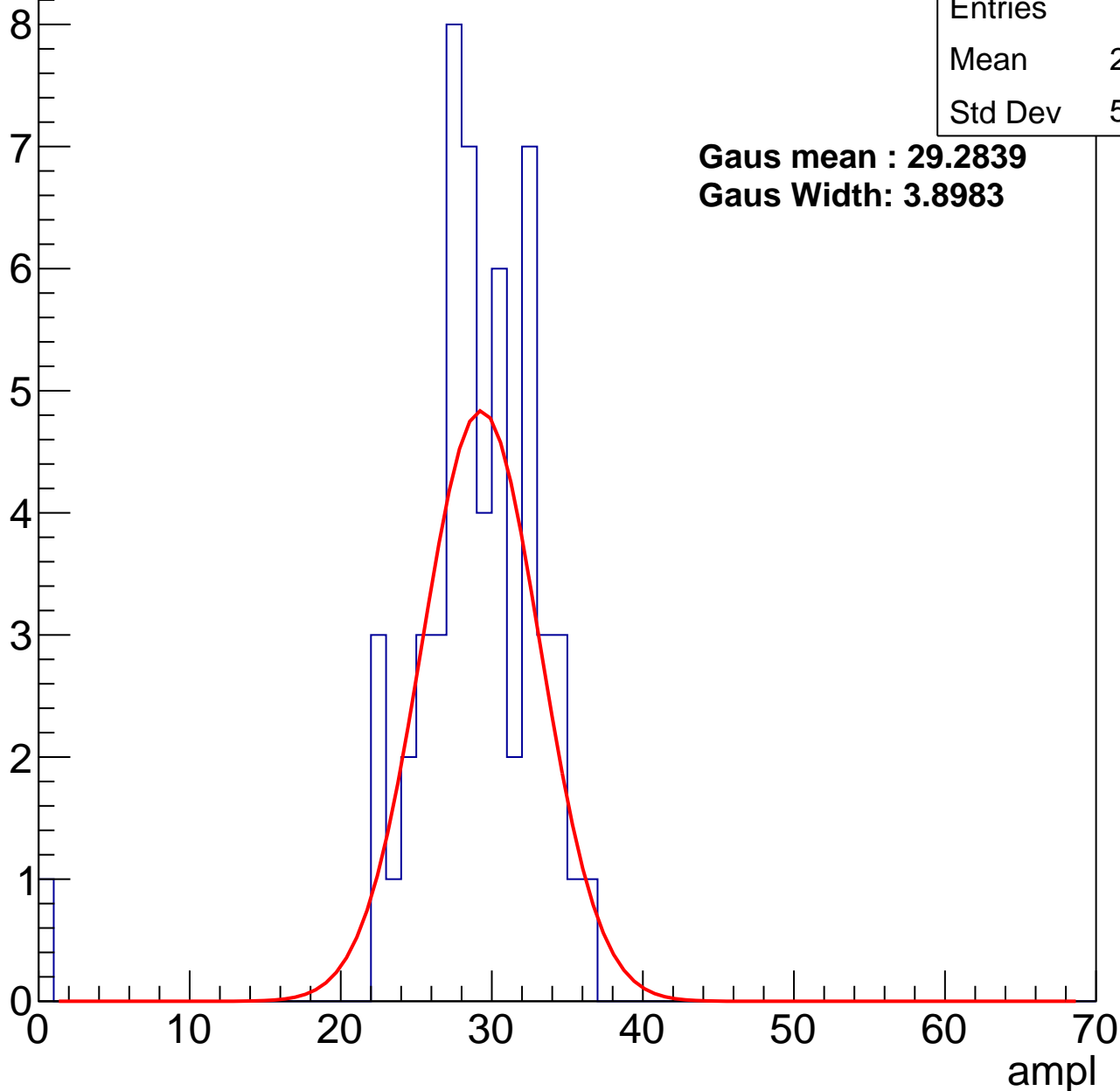
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	28.29
Std Dev	5.126

**Gaus mean : 29.2839**

**Gaus Width: 3.8983**



# B1L103S, U26-ch70, adc1

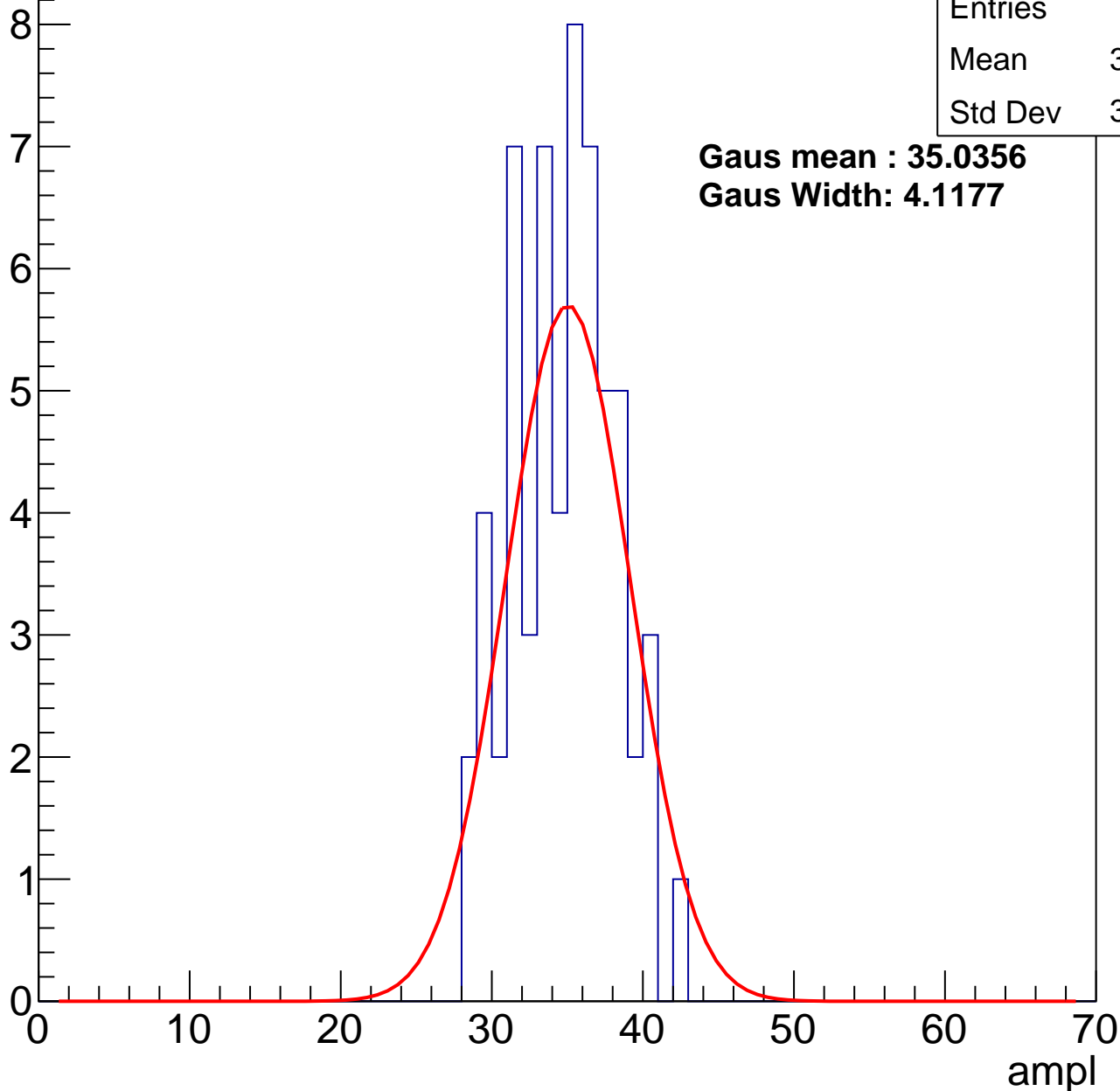
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	34.32
Std Dev	3.324

**Gaus mean : 35.0356**

**Gaus Width: 4.1177**



# B1L103S, U26-ch70, adc2

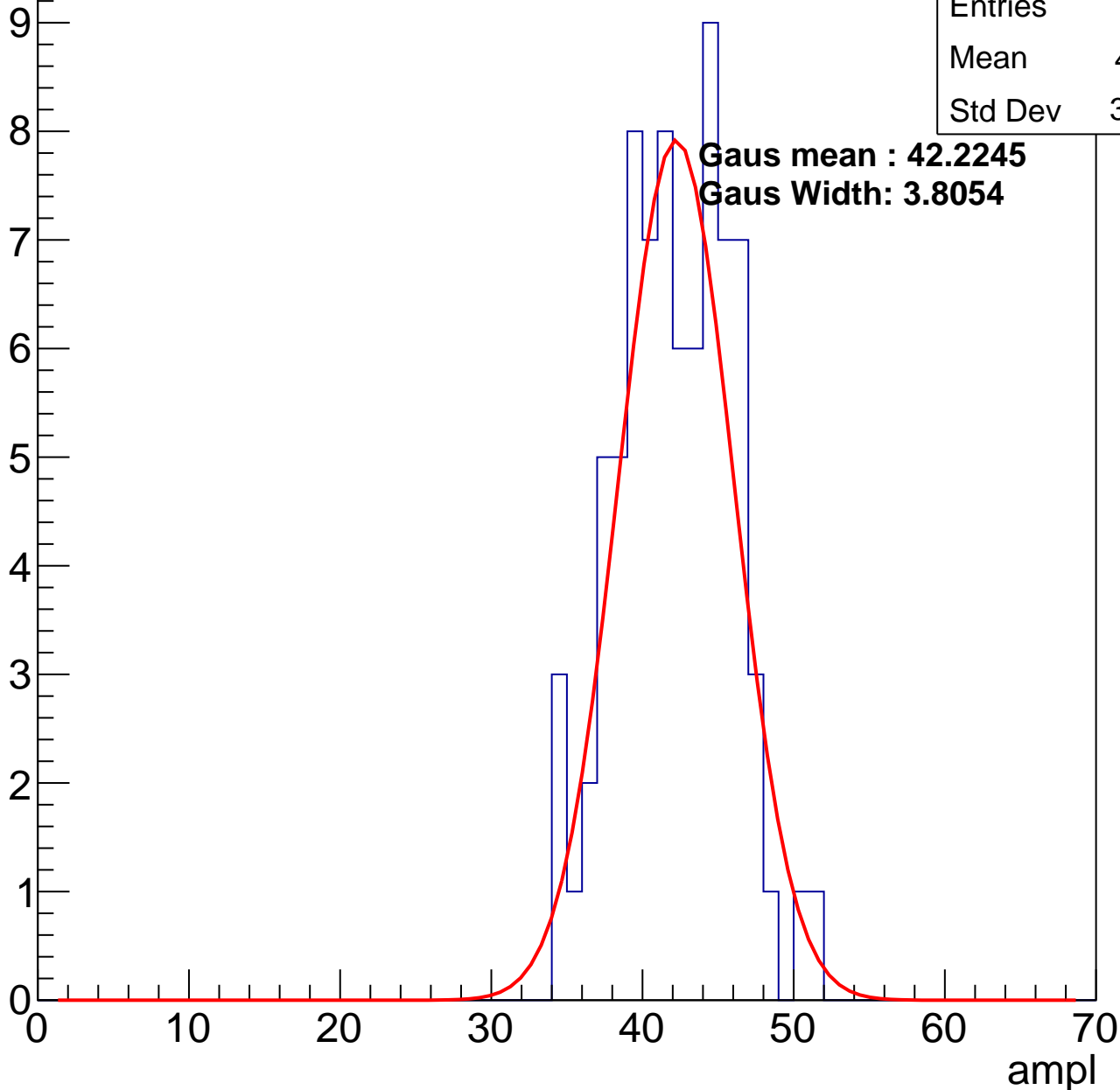
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	41.71
Std Dev	3.695

**Gaus mean : 42.2245**

**Gaus Width: 3.8054**

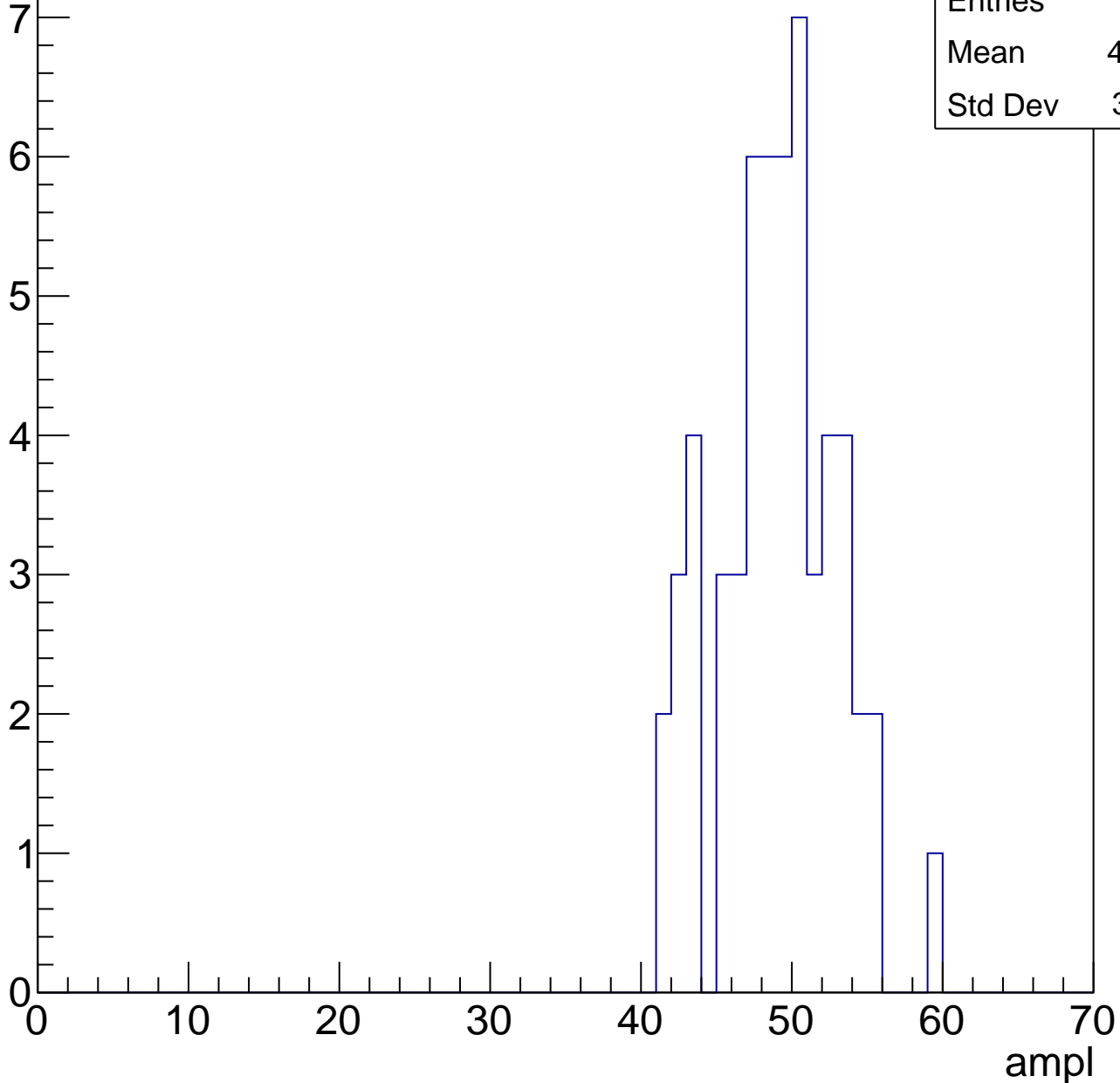


# B1L103S, U26-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	48.52
Std Dev	3.901

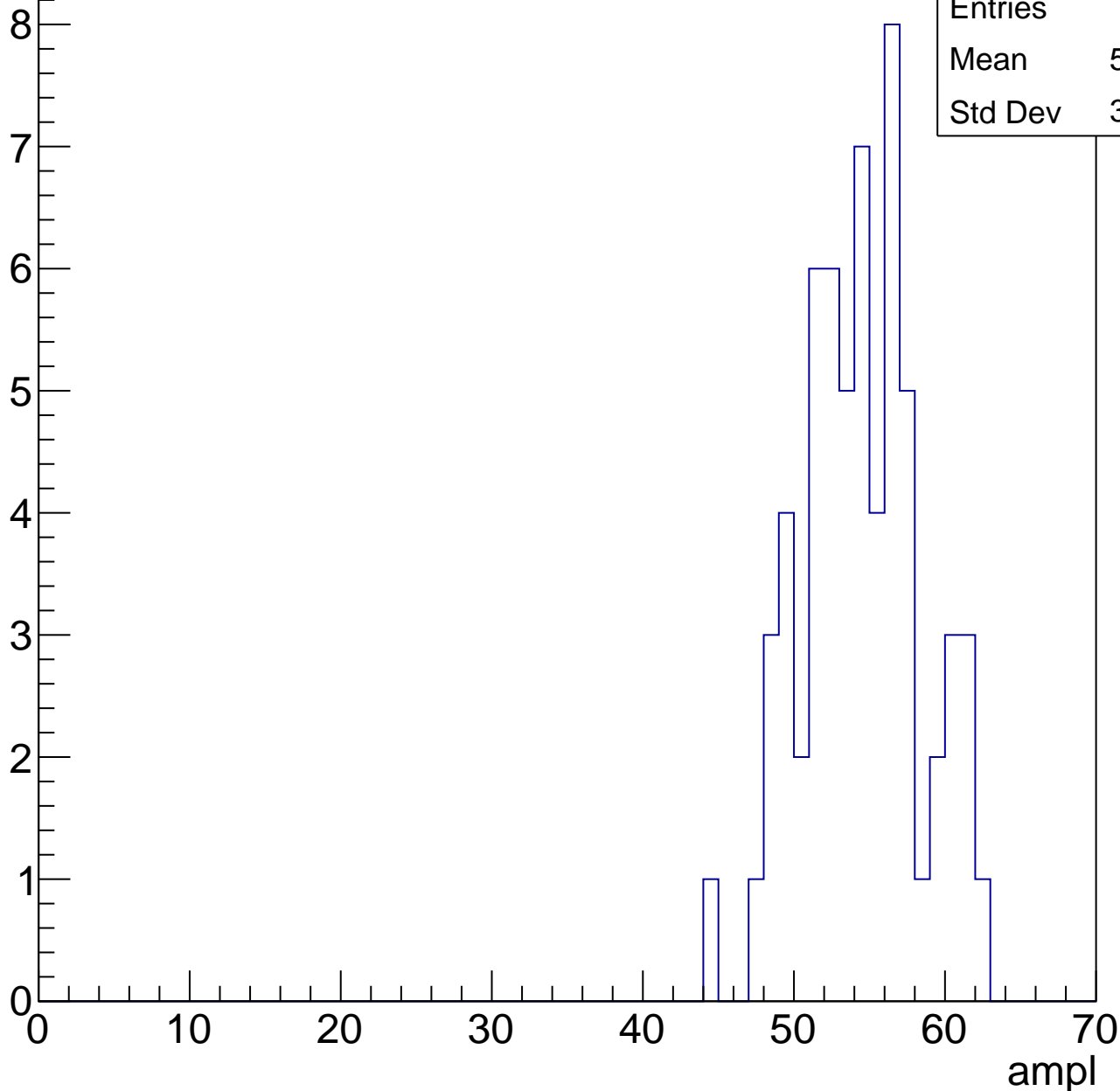


# B1L103S, U26-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	53.97
Std Dev	3.889

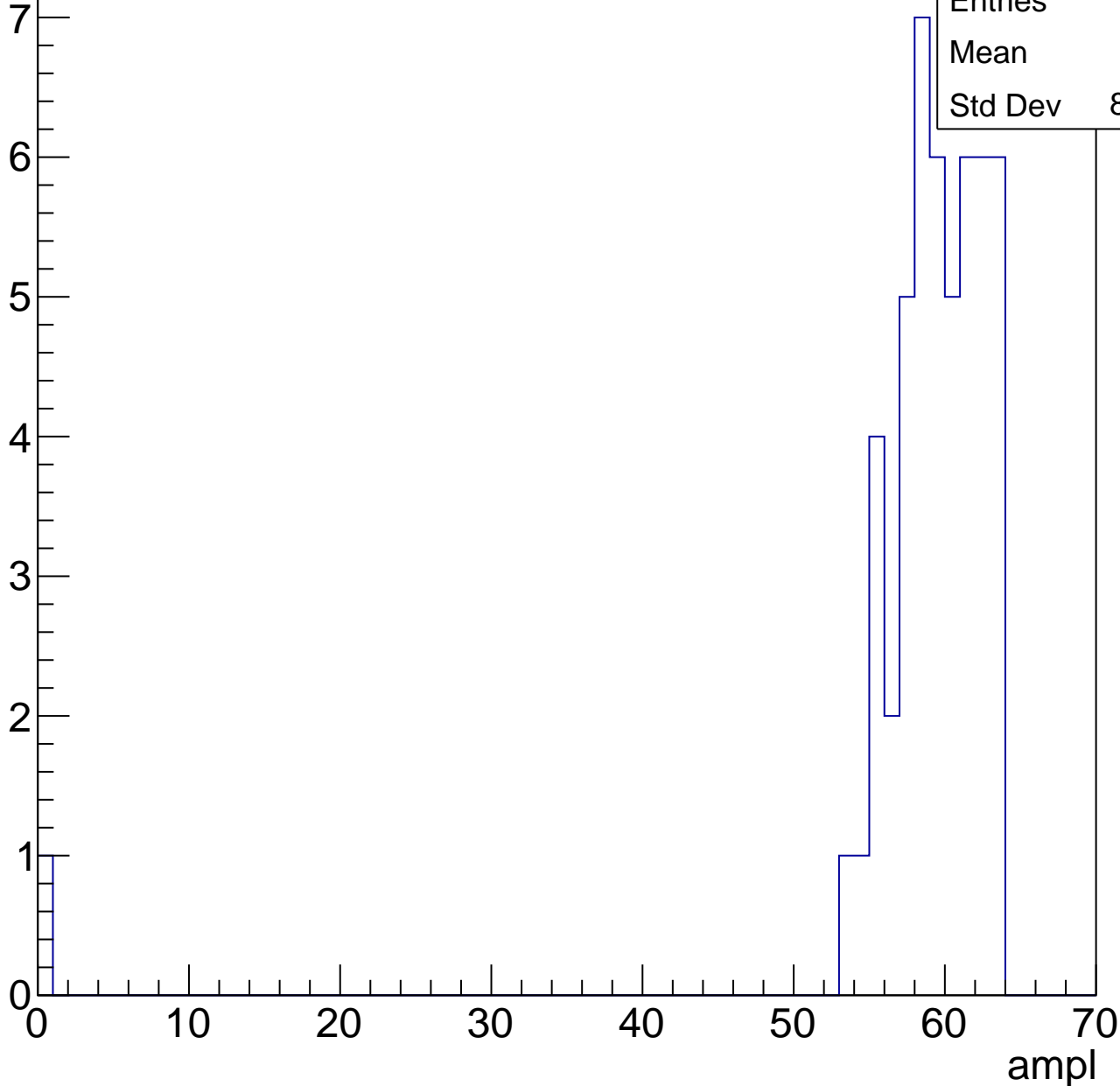


# B1L103S, U26-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

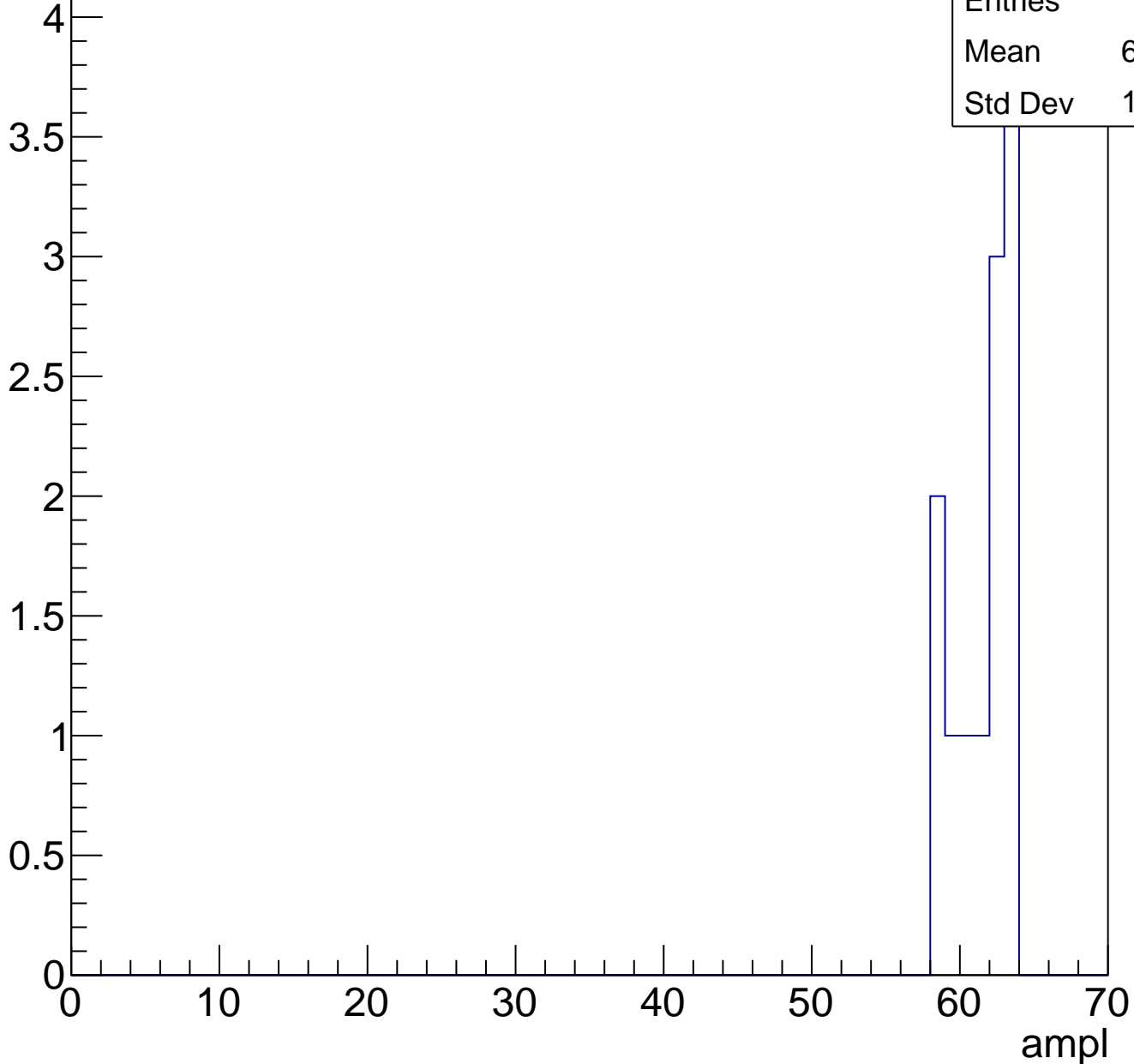
Entries	50
Mean	58
Std Dev	8.695



# B1L103S, U26-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

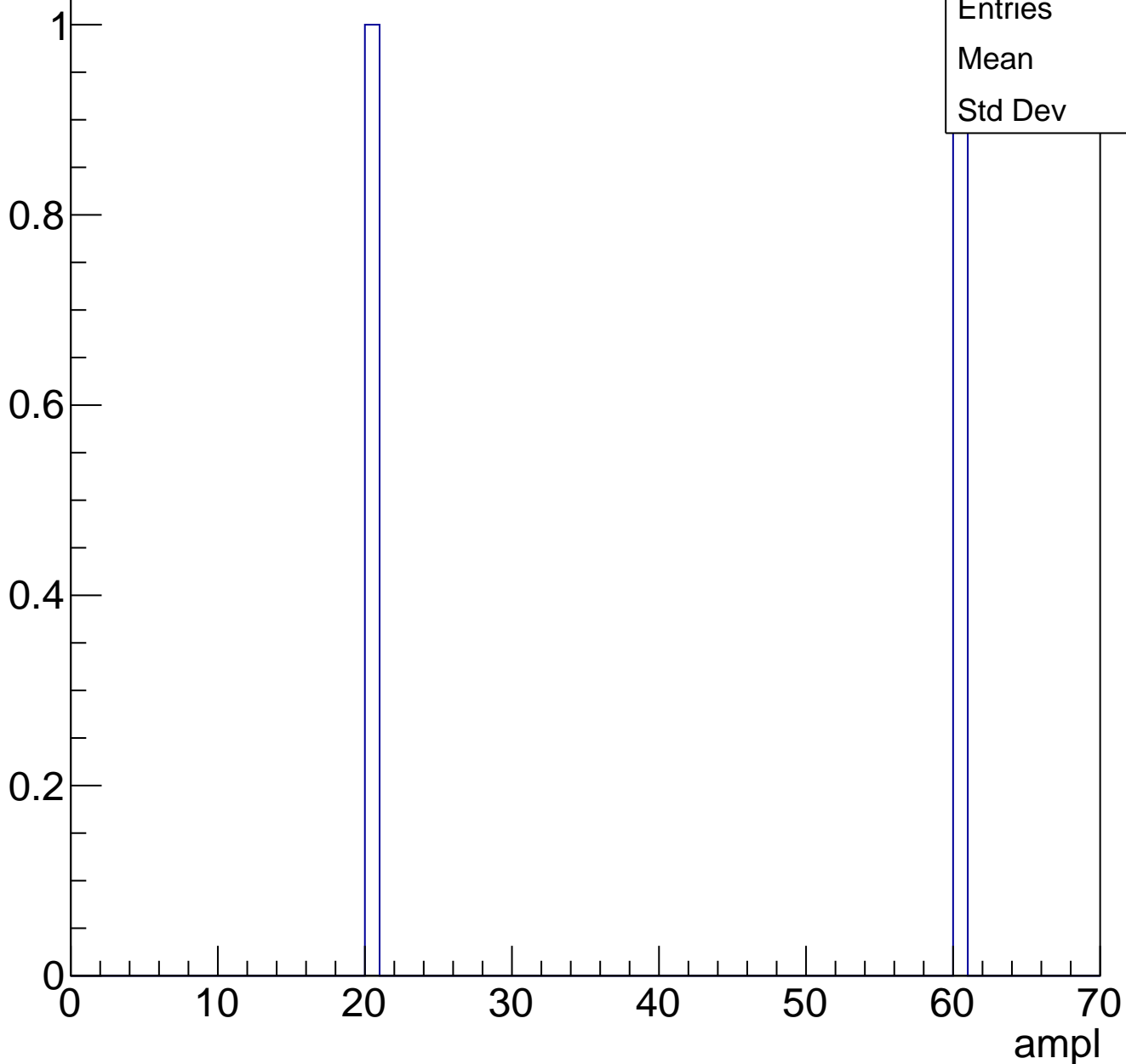




# B1L103S, U26-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	40
Std Dev	20

# B1L103S, U26-ch71, adc0

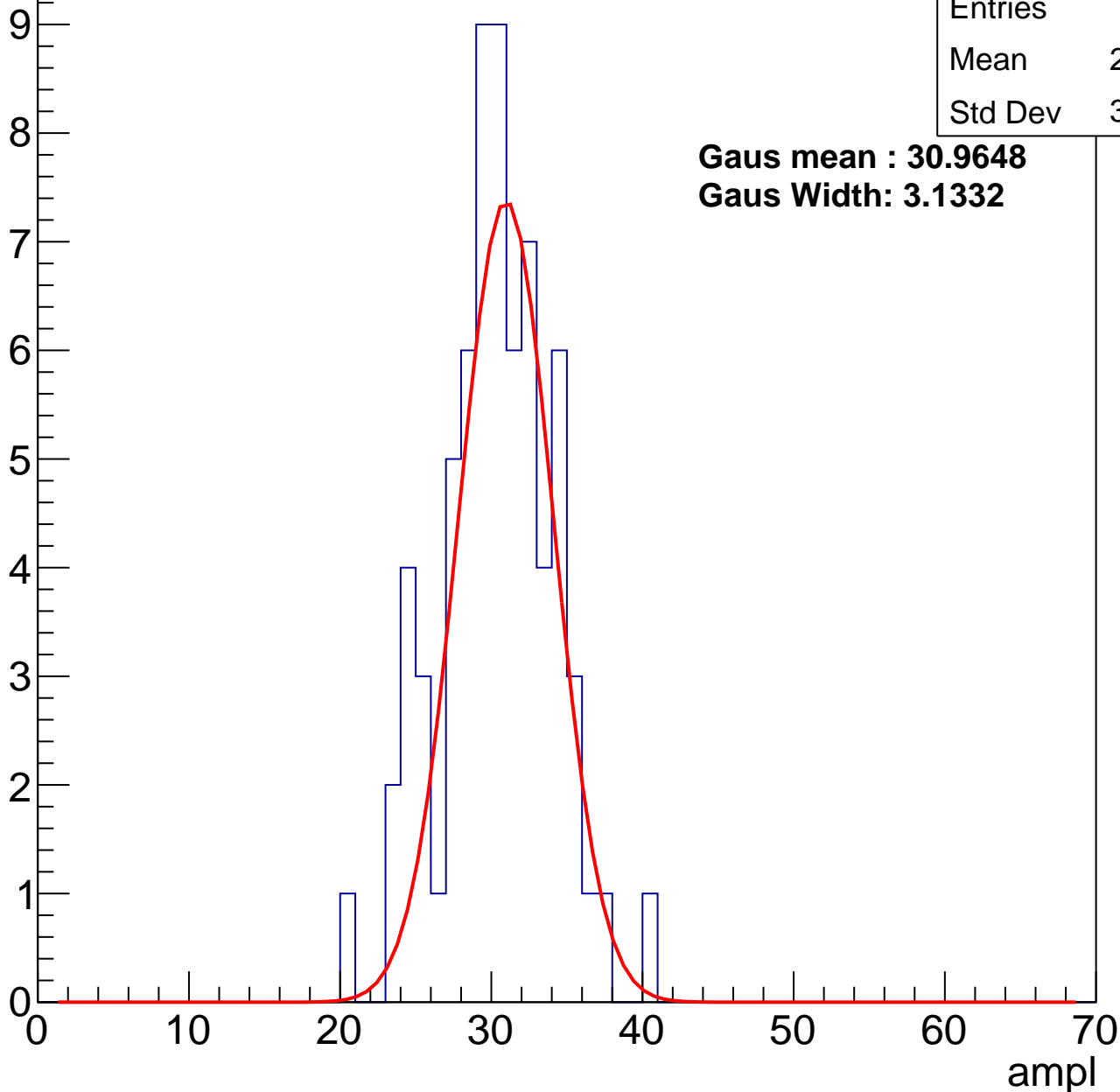
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	29.87
Std Dev	3.683

**Gaus mean : 30.9648**

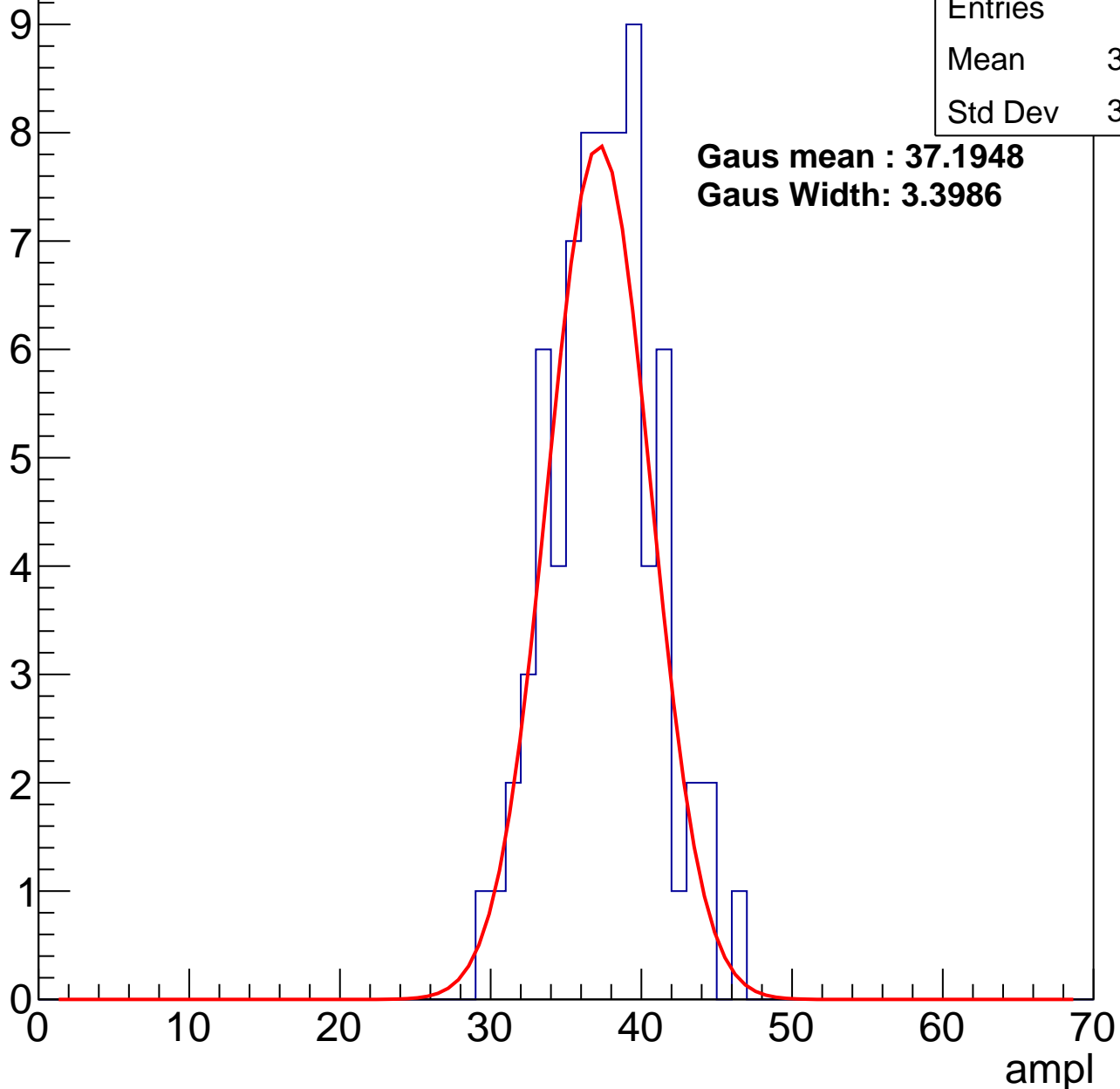
**Gaus Width: 3.1332**



# B1L103S, U26-ch71, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	73
Mean	37.03
Std Dev	3.472

# B1L103S, U26-ch71, adc2

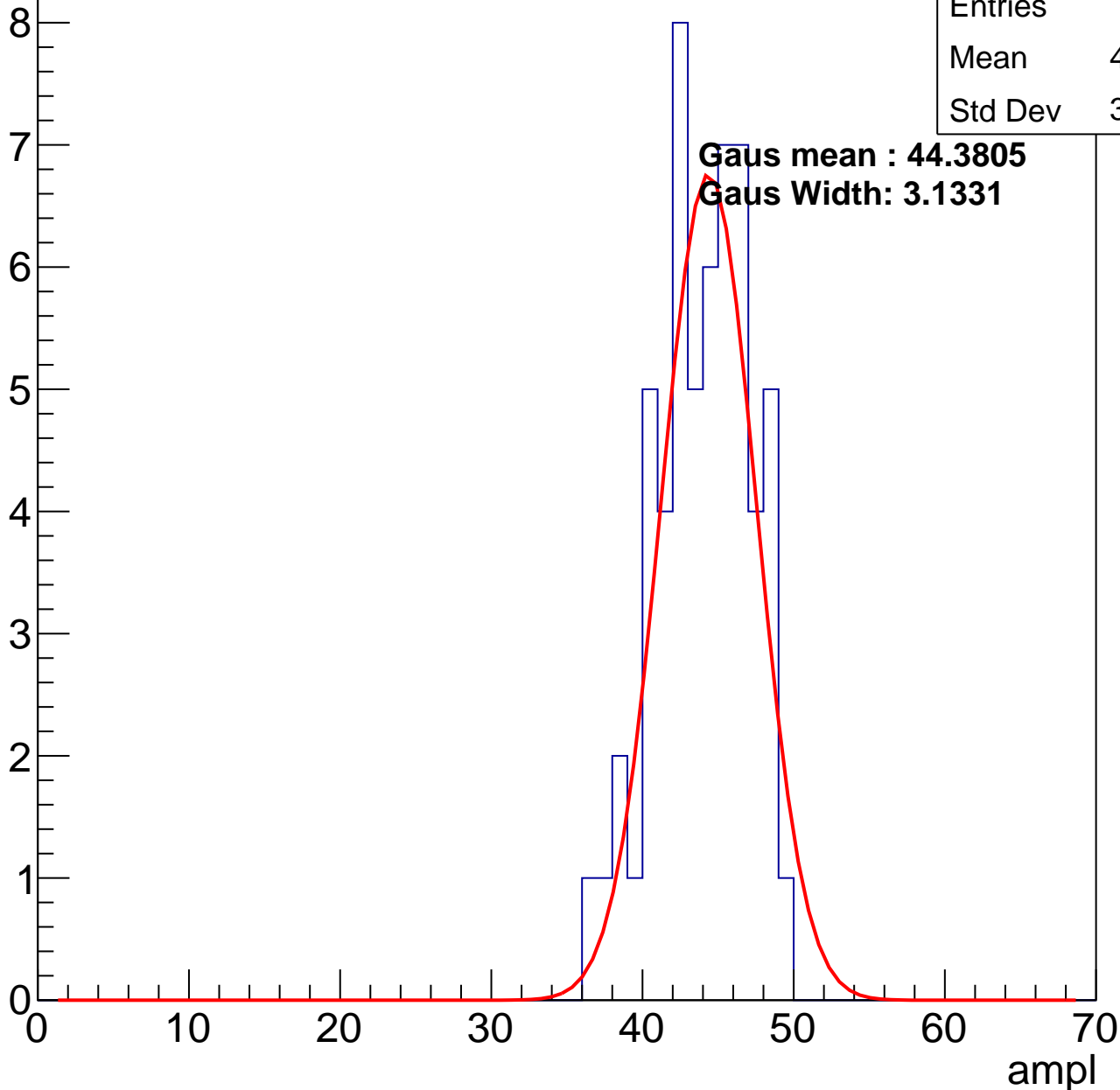
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	43.53
Std Dev	3.038

**Gaus mean : 44.3805**

**Gaus Width: 3.1331**

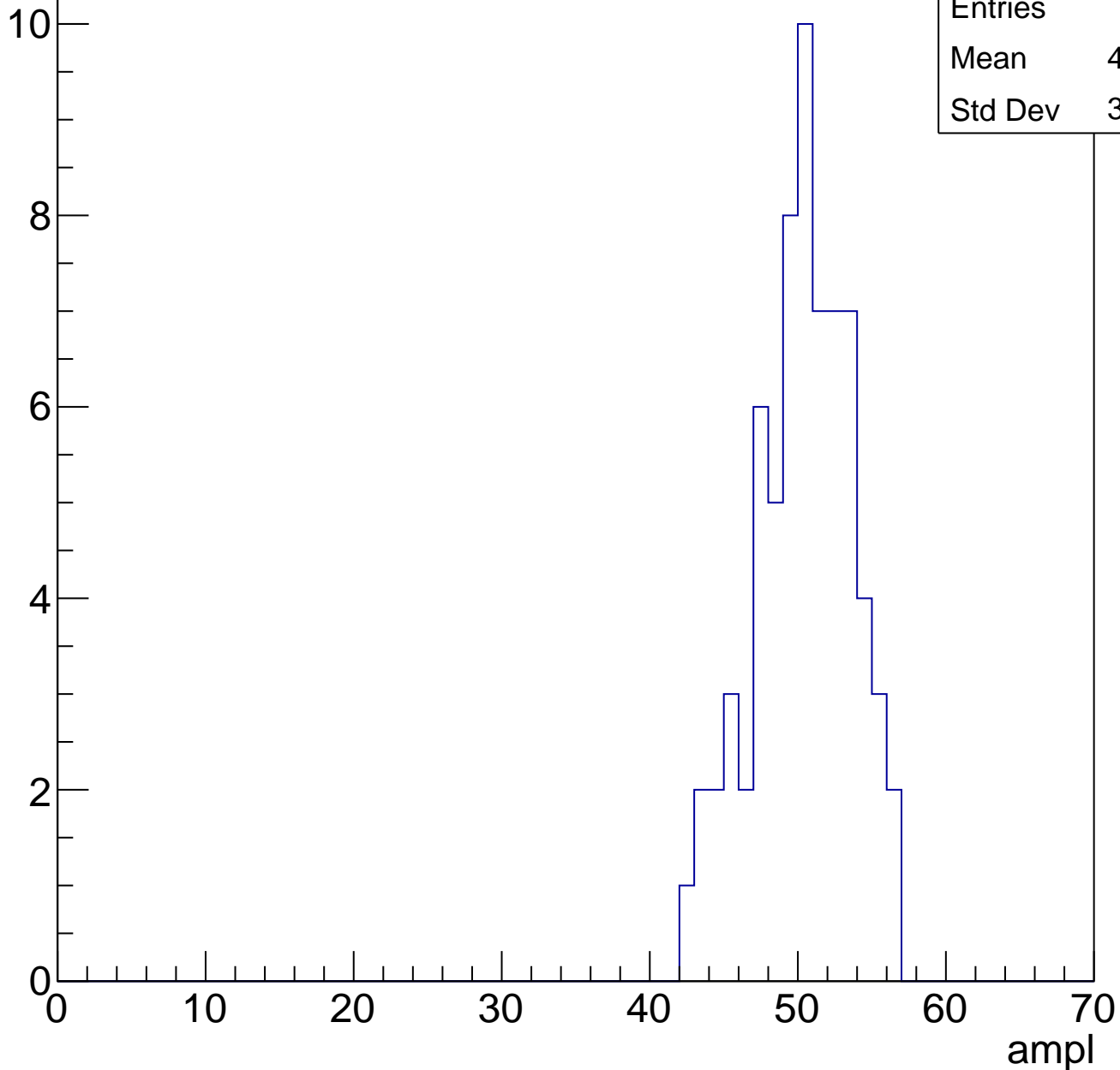


# B1L103S, U26-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	69
Mean	49.88
Std Dev	3.255

Entry

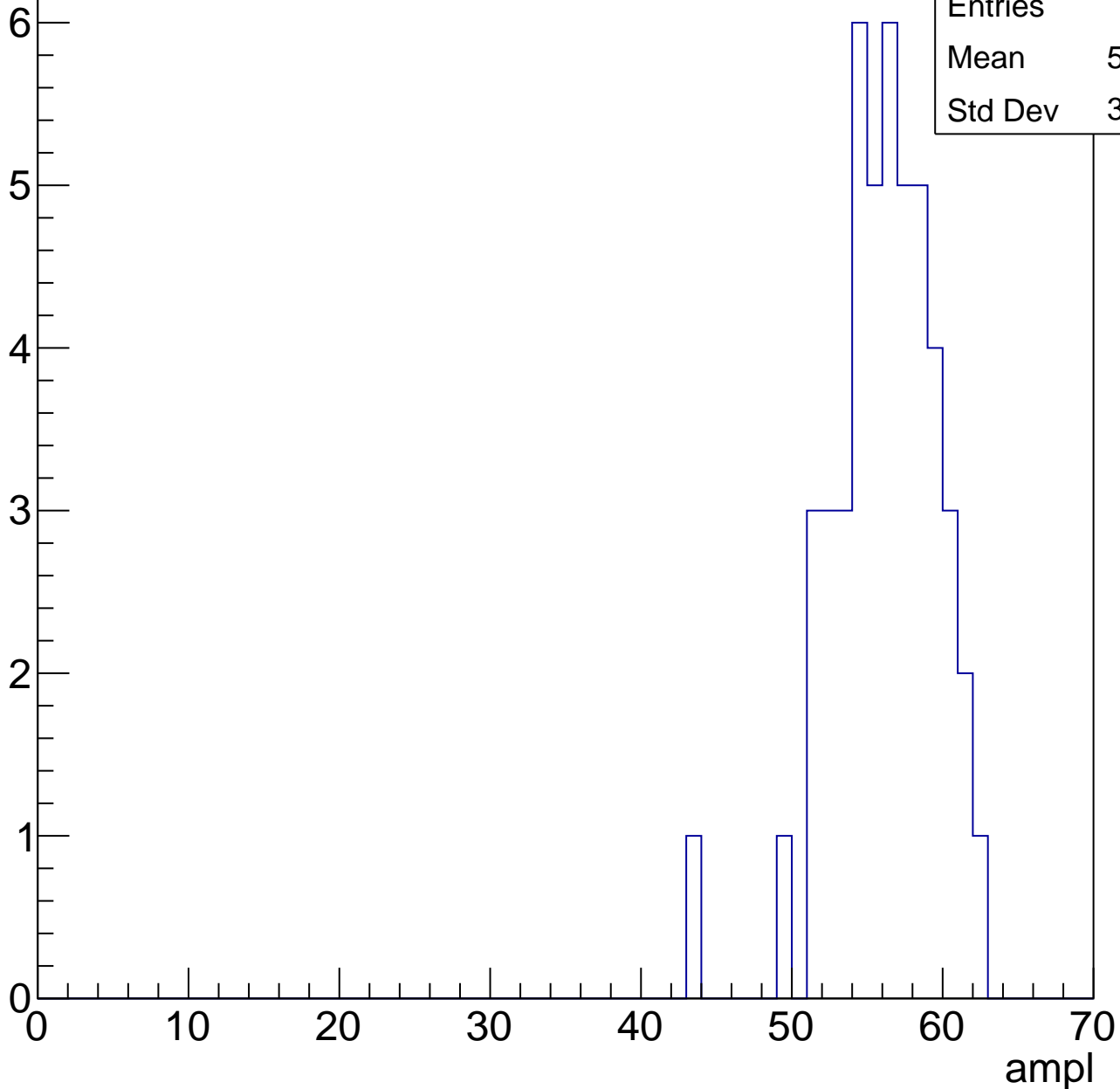


# B1L103S, U26-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	55.62
Std Dev	3.492

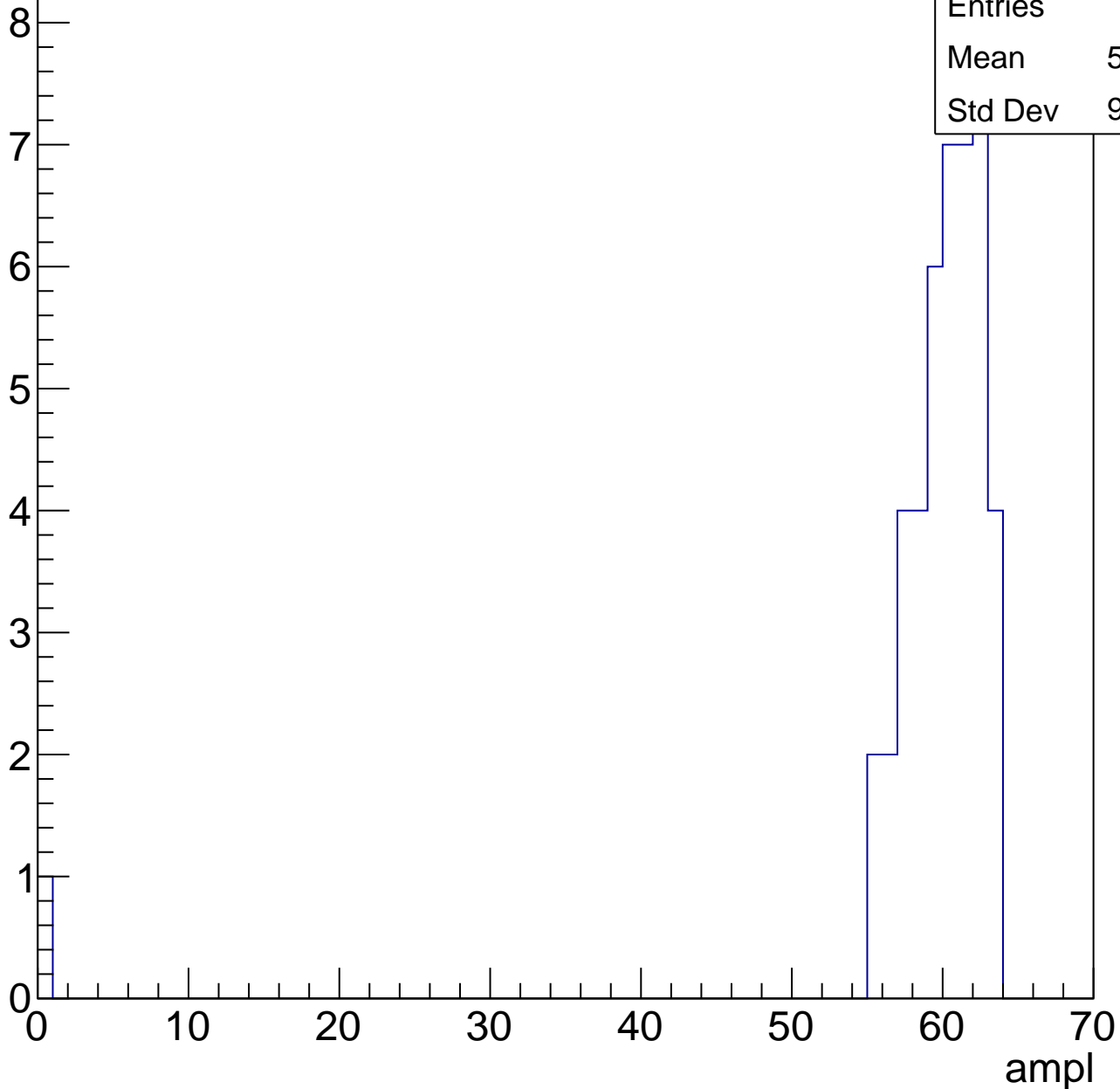


# B1L103S, U26-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	58.47
Std Dev	9.079

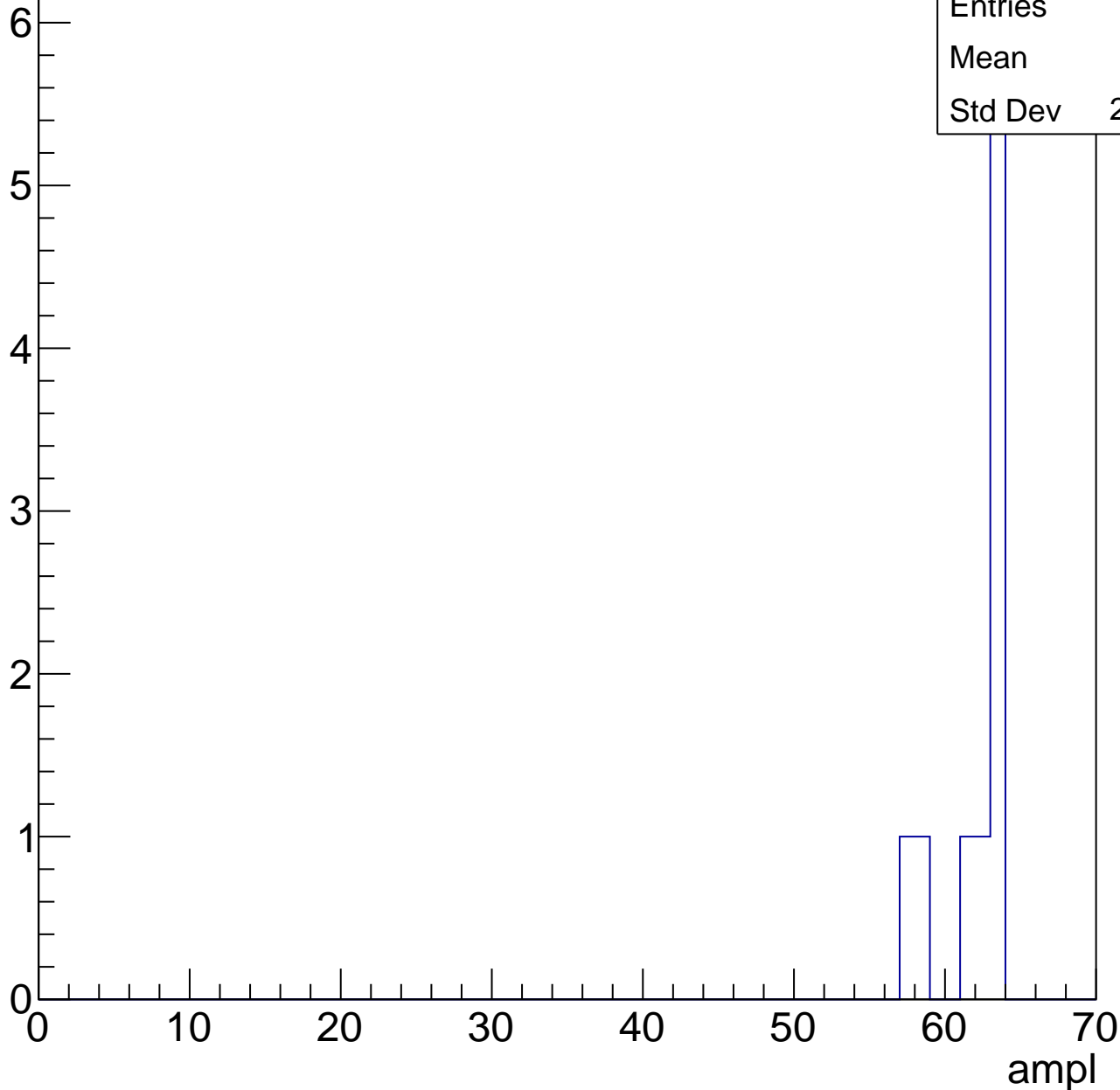


# B1L103S, U26-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	10
Mean	61.6
Std Dev	2.154





# B1L103S, U26-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch72, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	72
Mean	29.31
Std Dev	3.538

**Gaus mean : 29.6715**

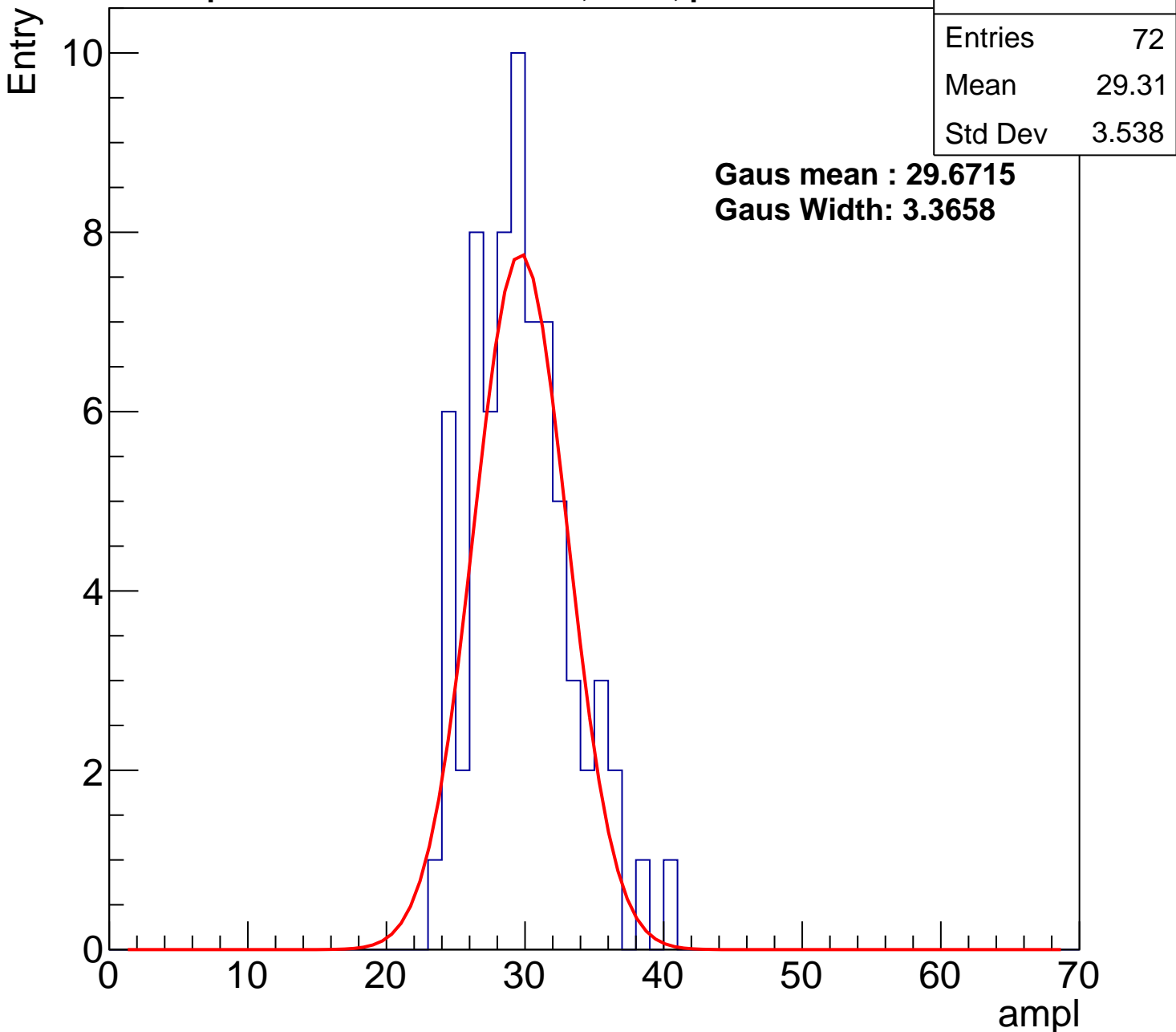
**Gaus Width: 3.3658**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch72, adc1

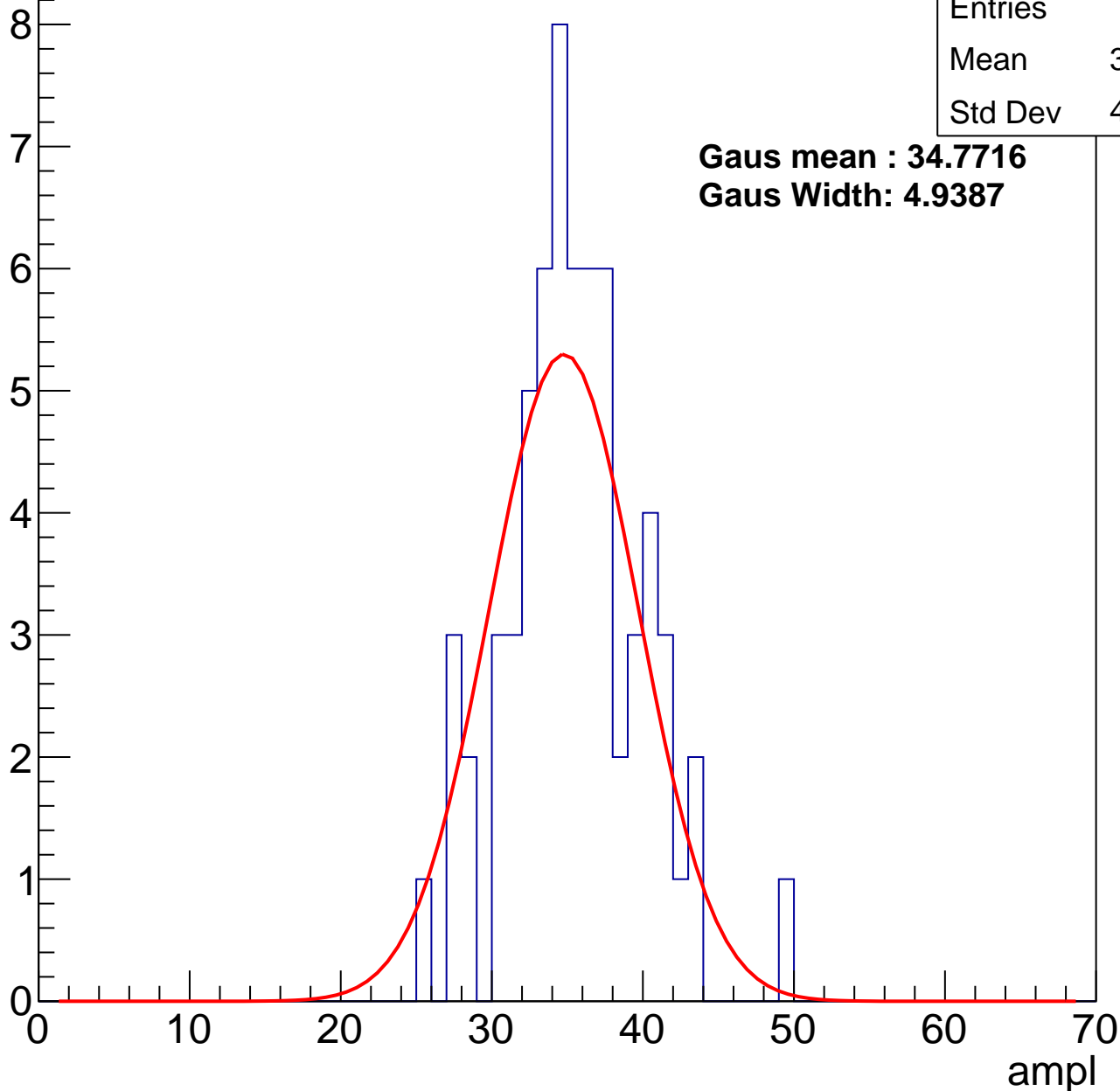
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	35.02
Std Dev	4.415

**Gaus mean : 34.7716**

**Gaus Width: 4.9387**



# B1L103S, U26-ch72, adc2

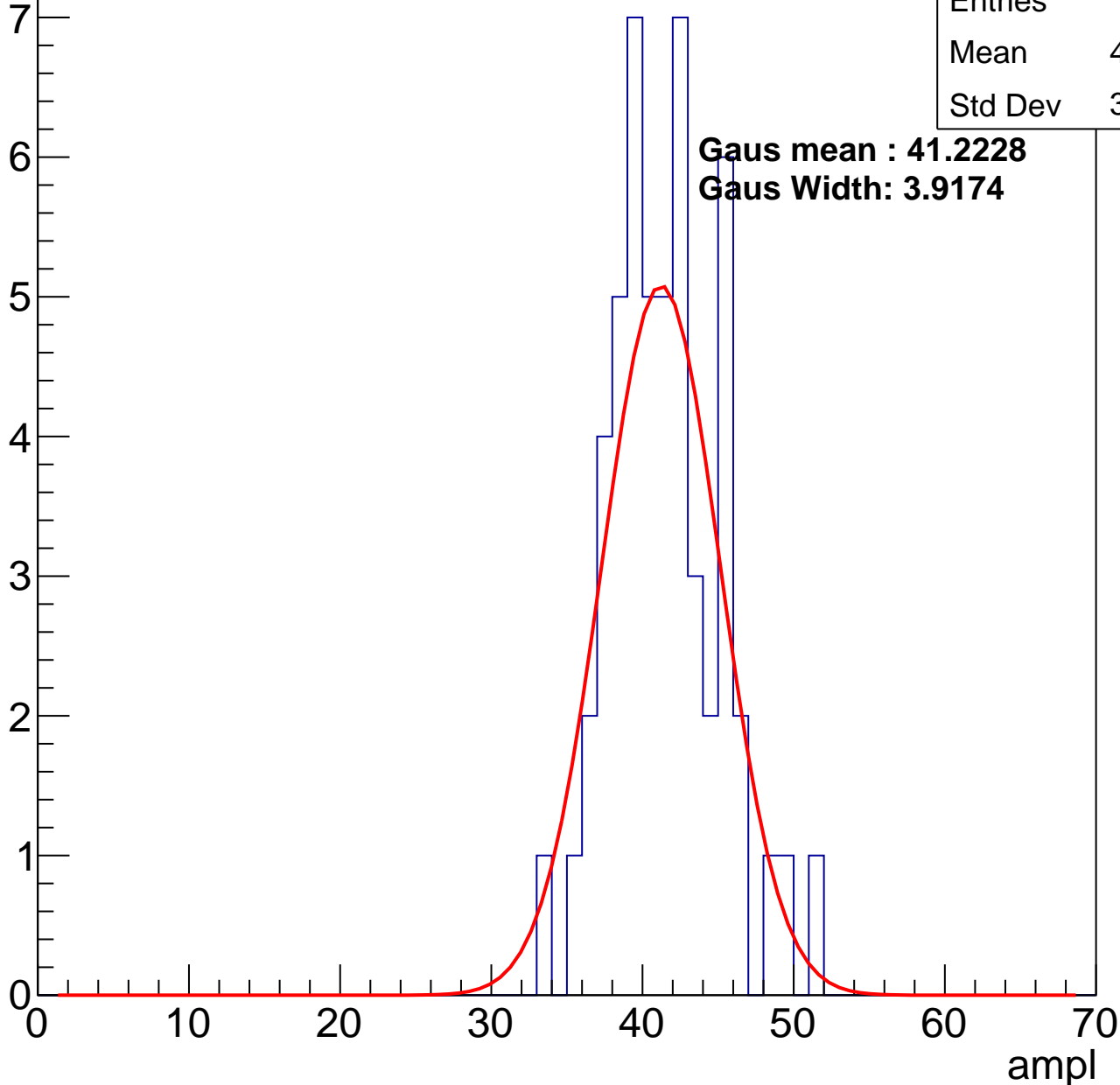
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	41.08
Std Dev	3.602

**Gaus mean : 41.2228**

**Gaus Width: 3.9174**

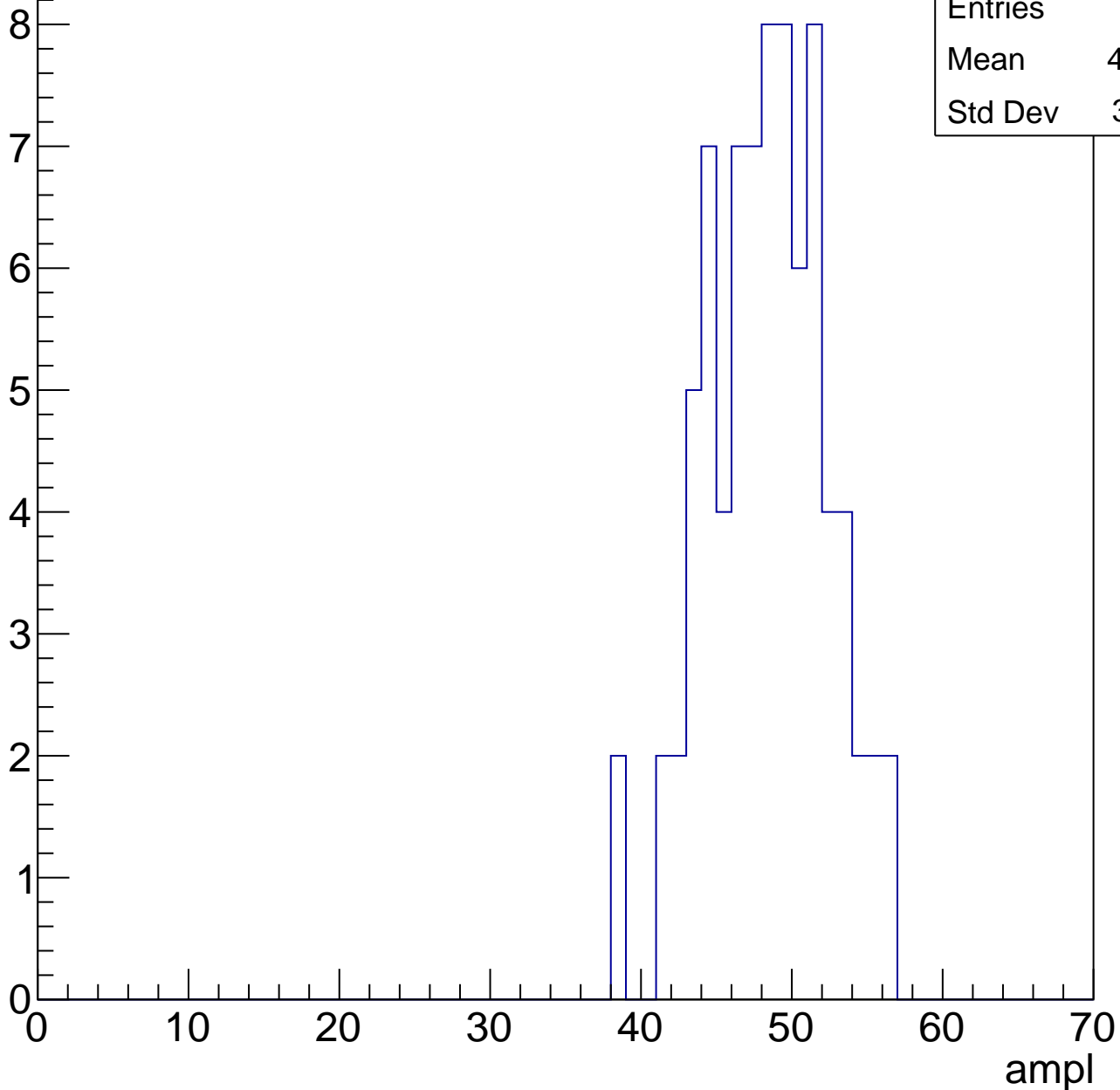


# B1L103S, U26-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

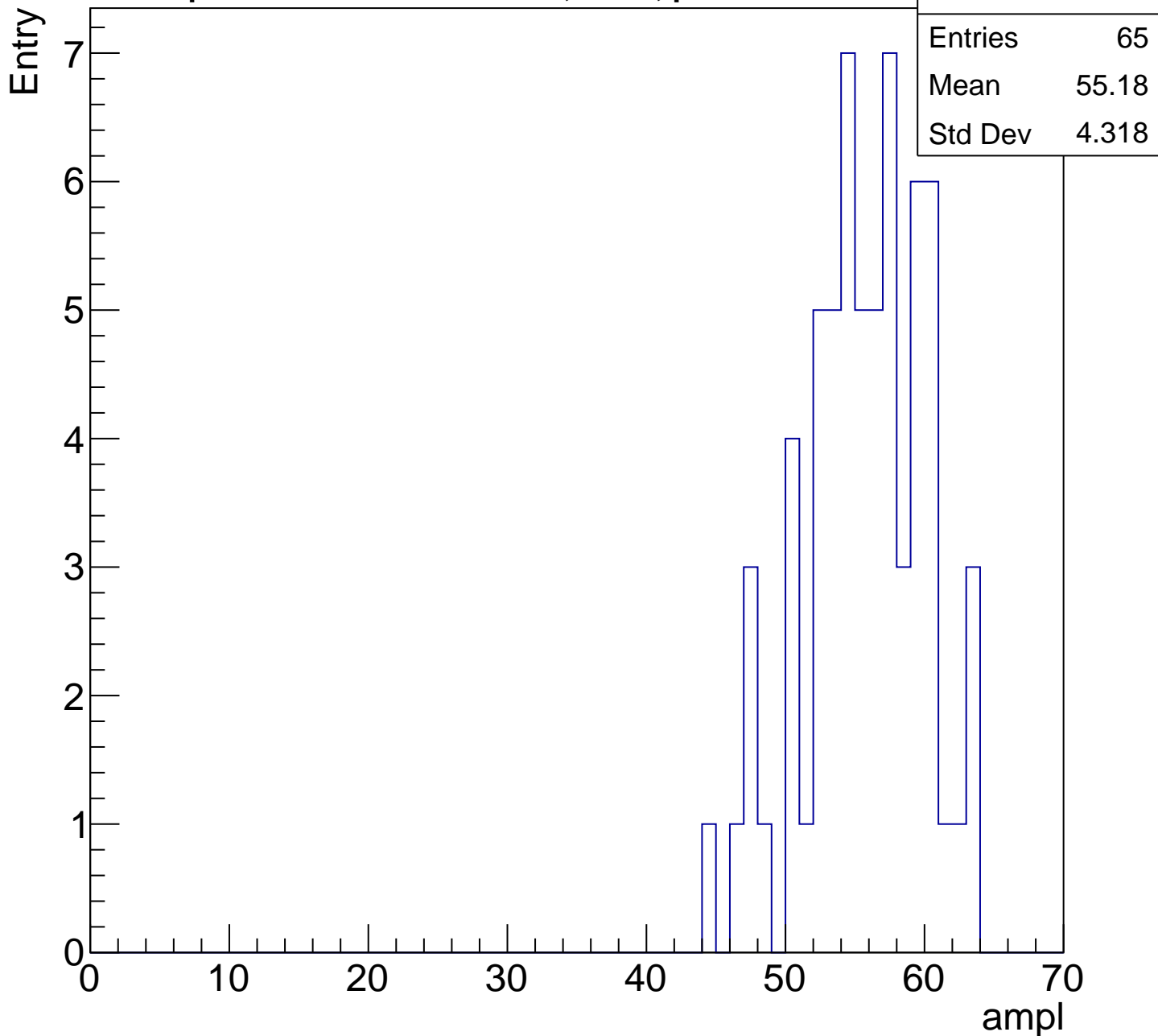
Entry

Entries	80
Mean	47.88
Std Dev	3.941



# B1L103S, U26-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

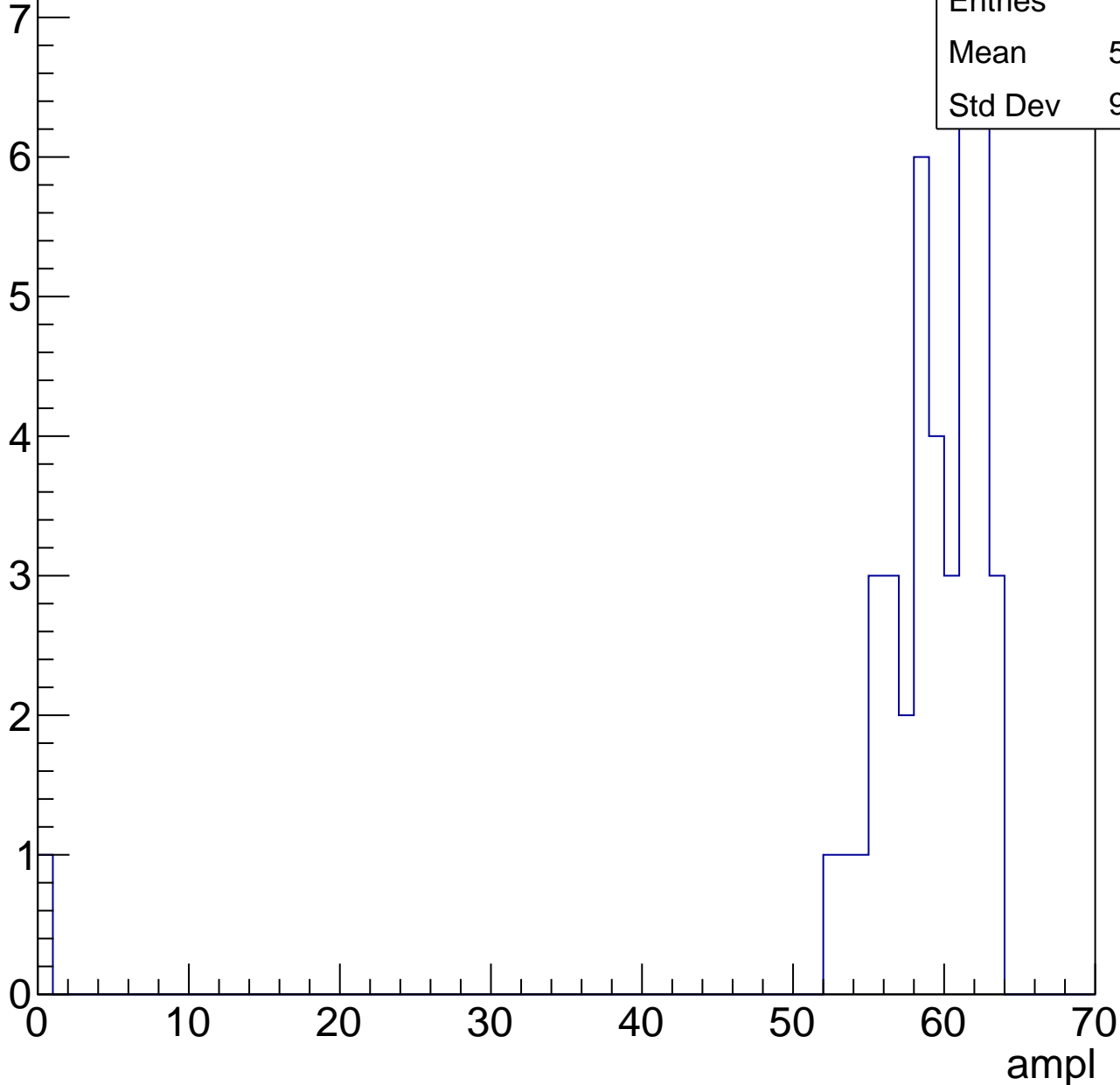


# B1L103S, U26-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

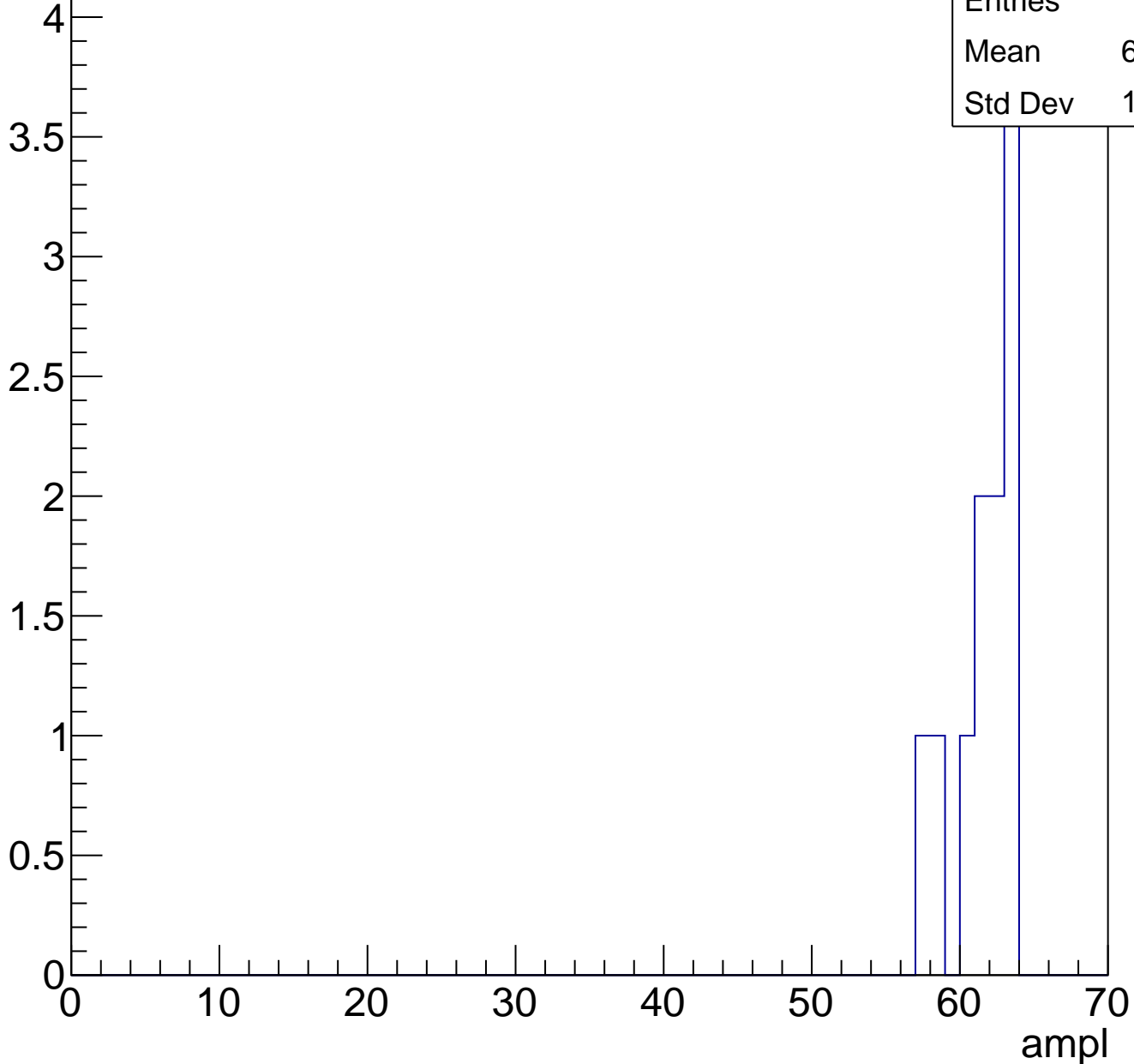
Entries	42
Mean	57.62
Std Dev	9.439



# B1L103S, U26-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U26-ch73, adc0

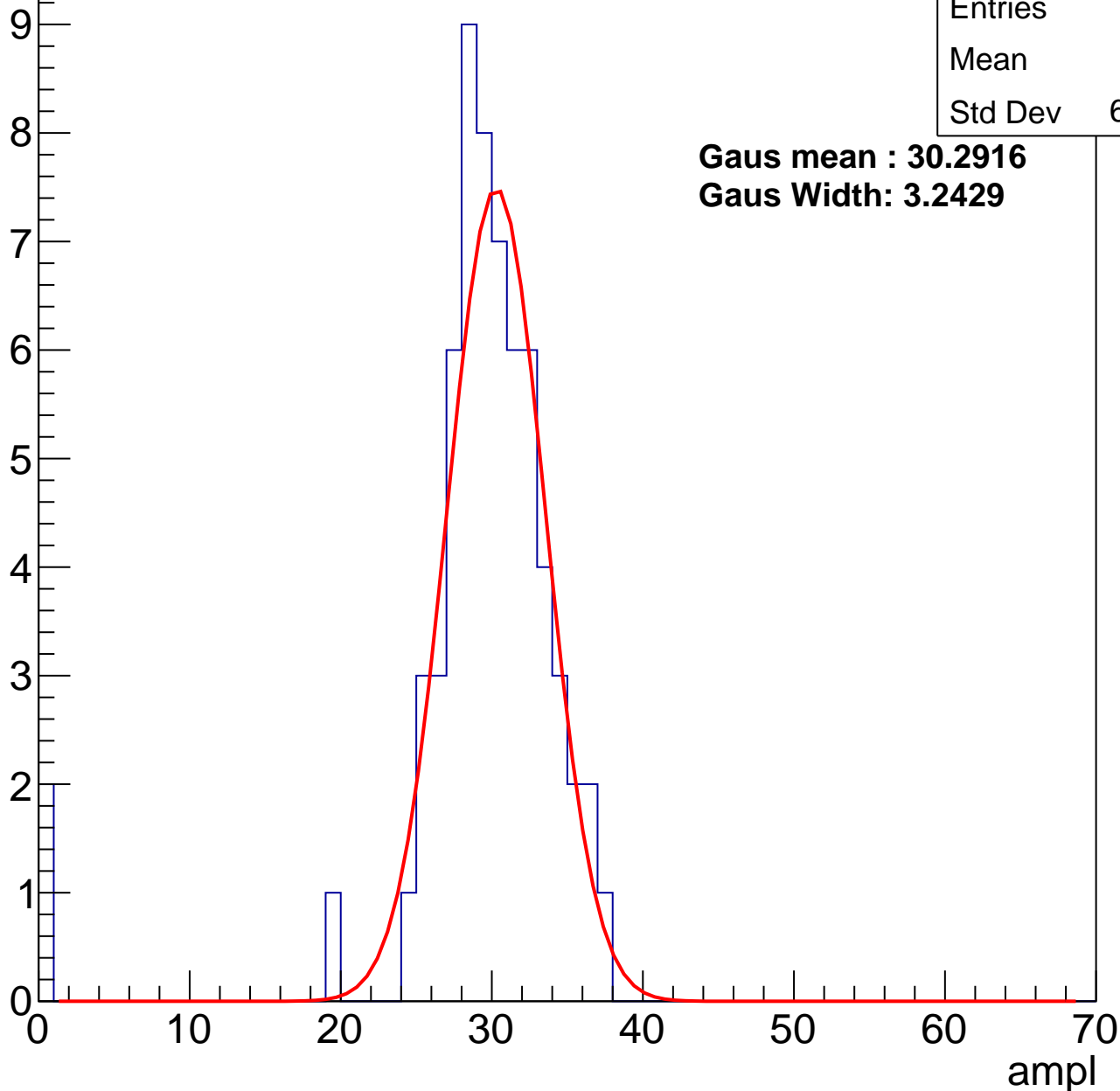
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	28.8
Std Dev	6.086

**Gaus mean : 30.2916**

**Gaus Width: 3.2429**



# B1L103S, U26-ch73, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	78
Mean	36.99
Std Dev	3.632

**Gaus mean : 37.7307**

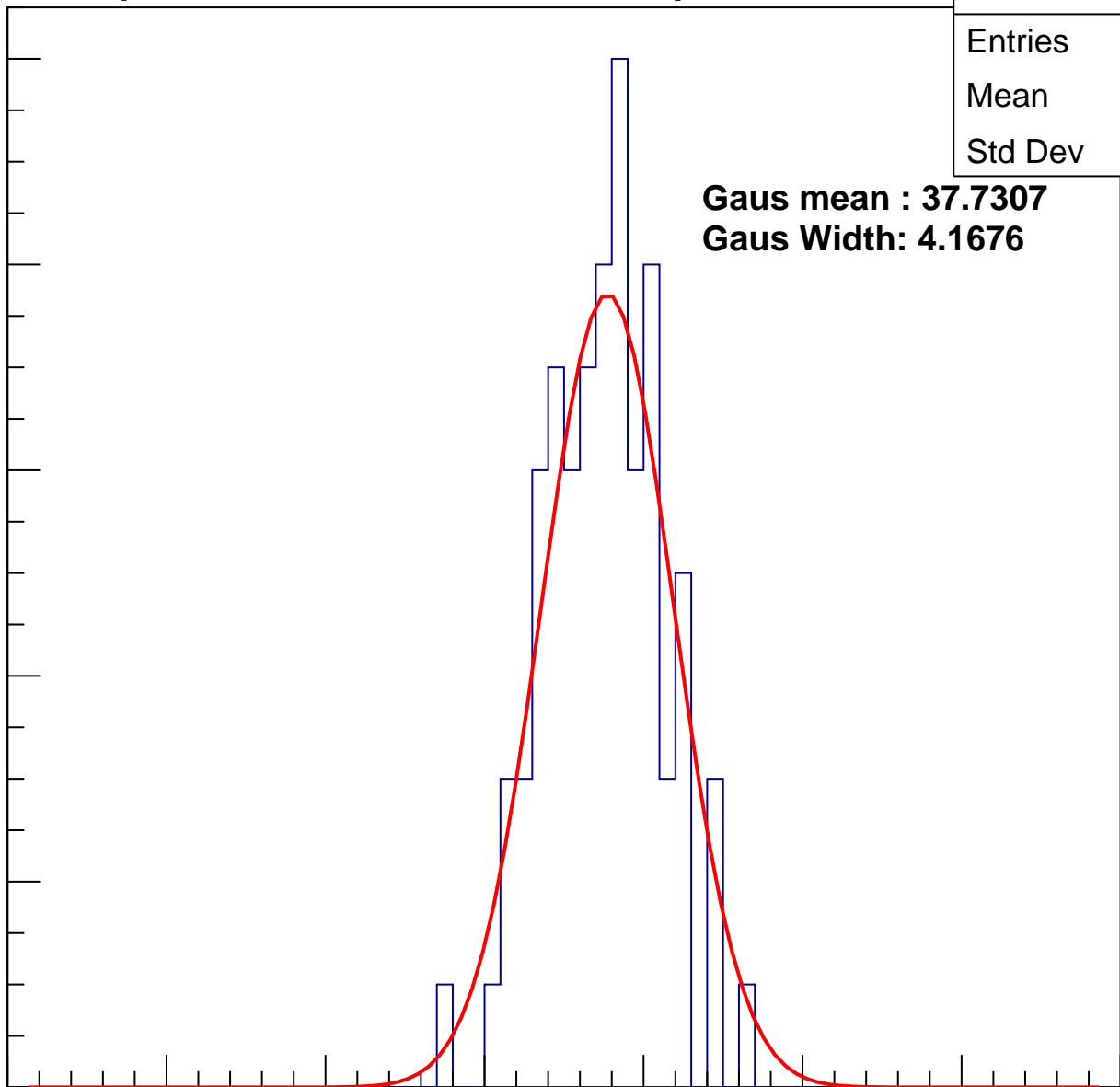
**Gaus Width: 4.1676**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch73, adc2

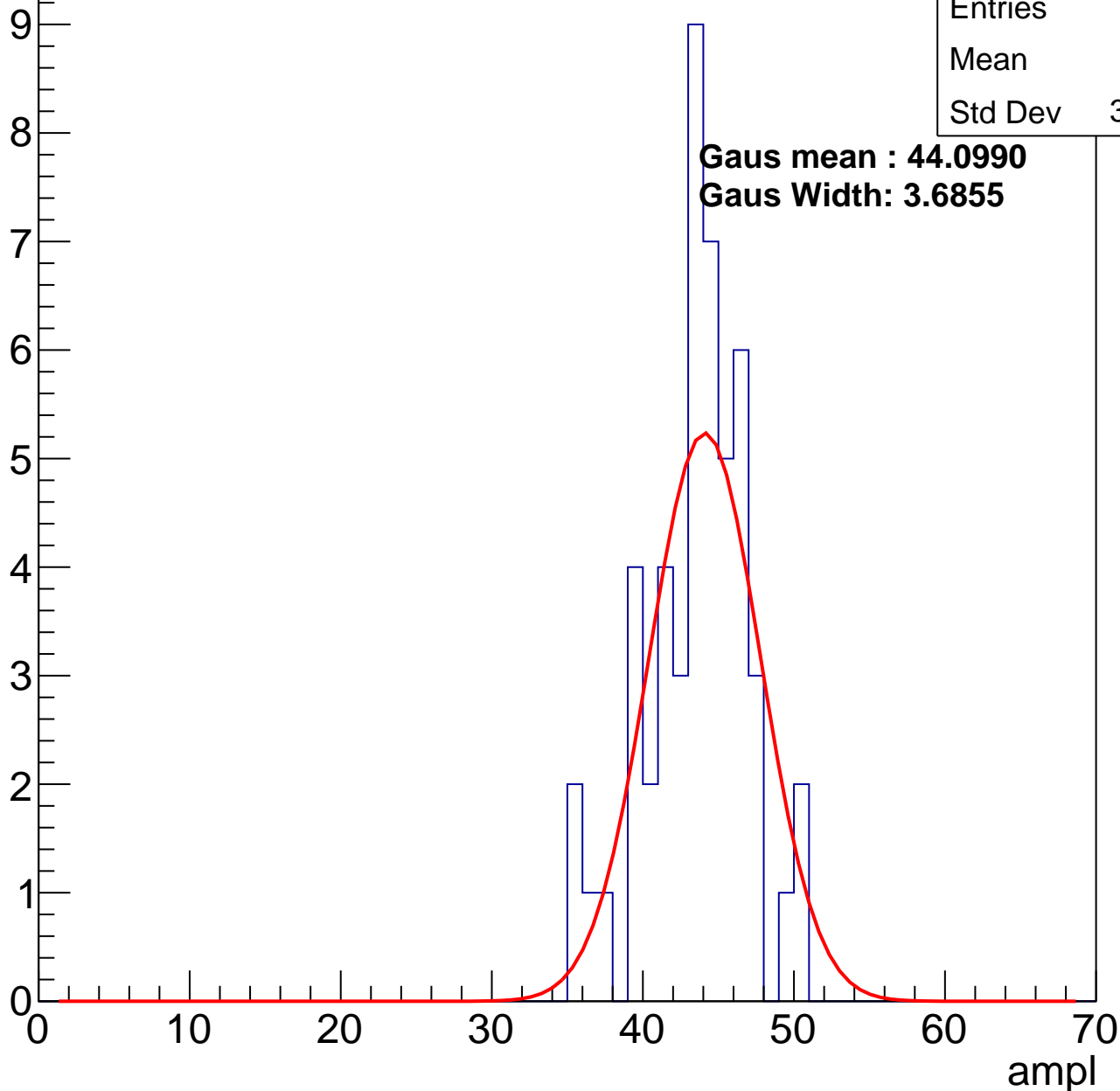
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	43.1
Std Dev	3.396

**Gaus mean : 44.0990**

**Gaus Width: 3.6855**

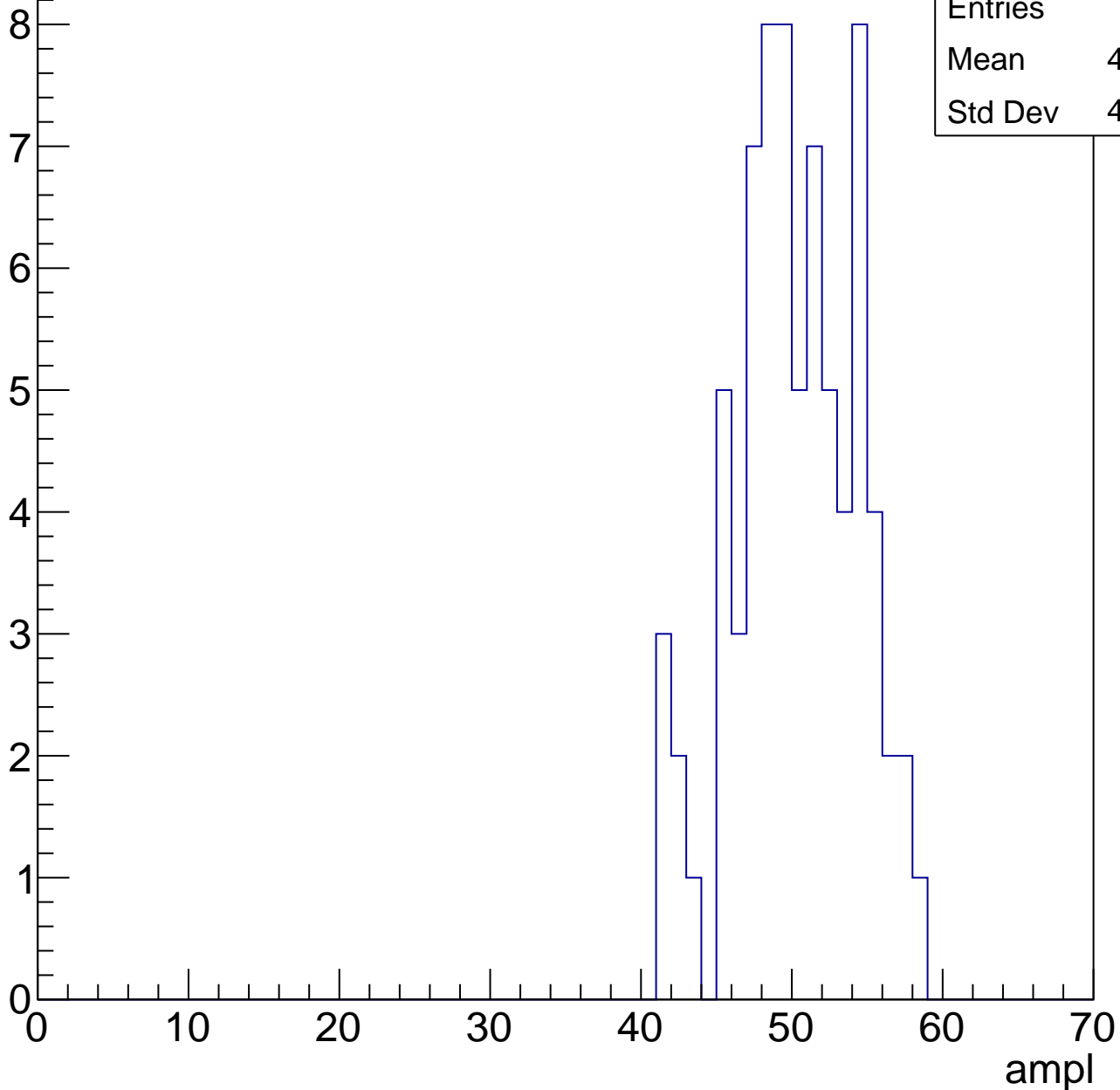


# B1L103S, U26-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	49.77
Std Dev	4.028



# B1L103S, U26-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

7

6

5

4

3

2

1

0

Entries	55
Mean	55.55
Std Dev	3.789

ampl

0

10

20

30

40

50

60

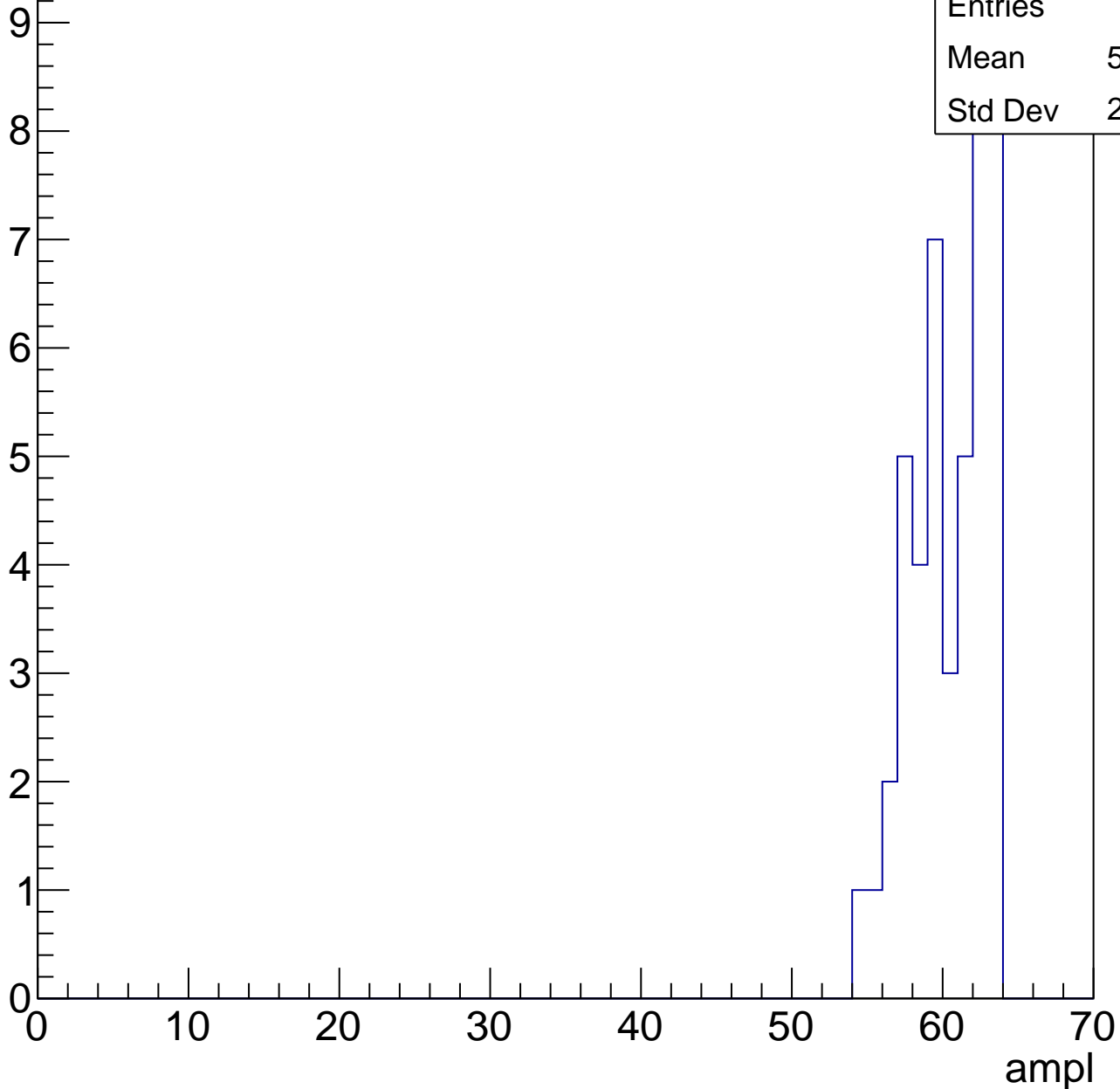
70

# B1L103S, U26-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

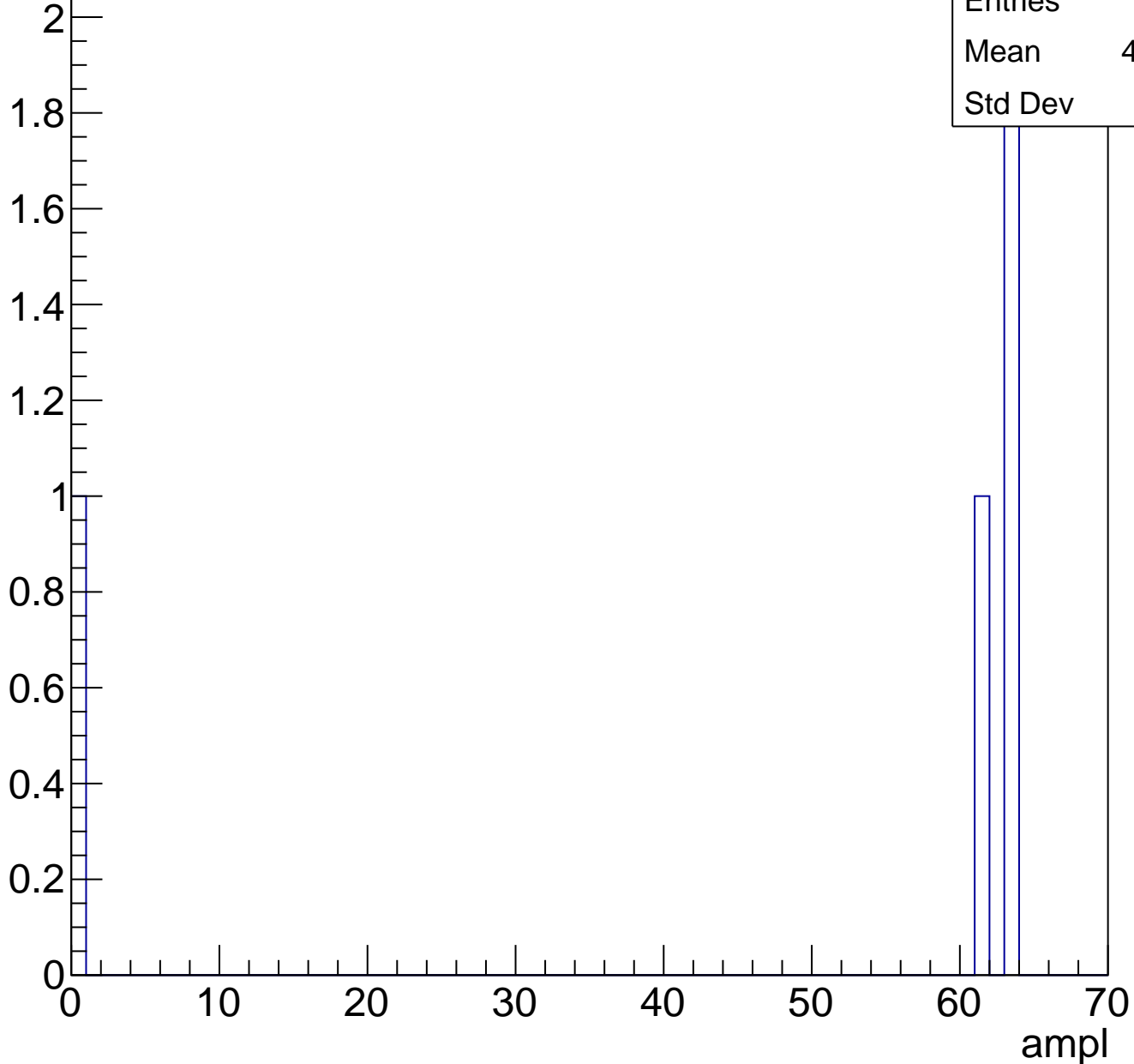
Entries	45
Mean	59.96
Std Dev	2.467



# B1L103S, U26-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U26-ch74, adc0

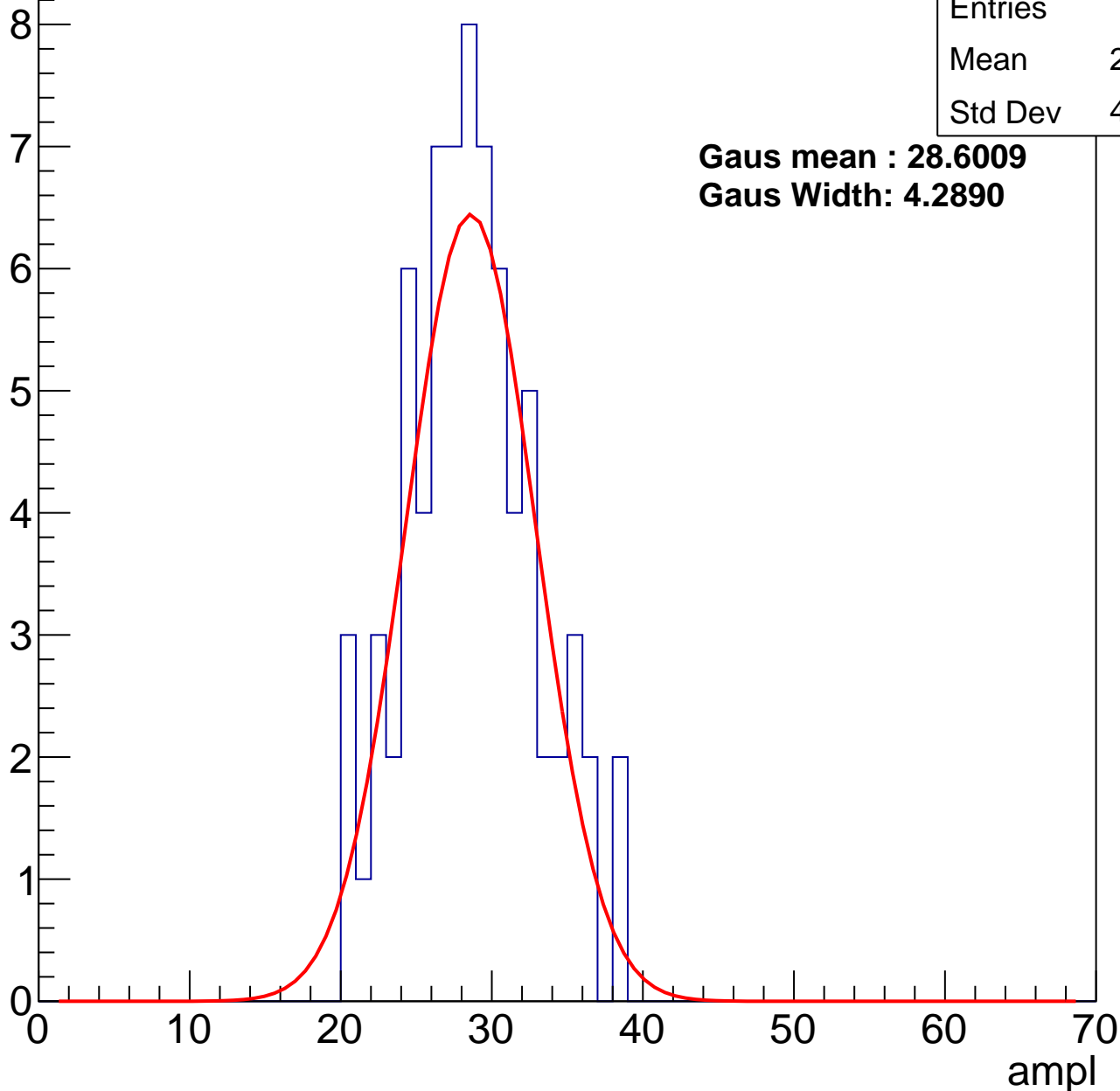
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	28.19
Std Dev	4.203

**Gaus mean : 28.6009**

**Gaus Width: 4.2890**



# B1L103S, U26-ch74, adc1

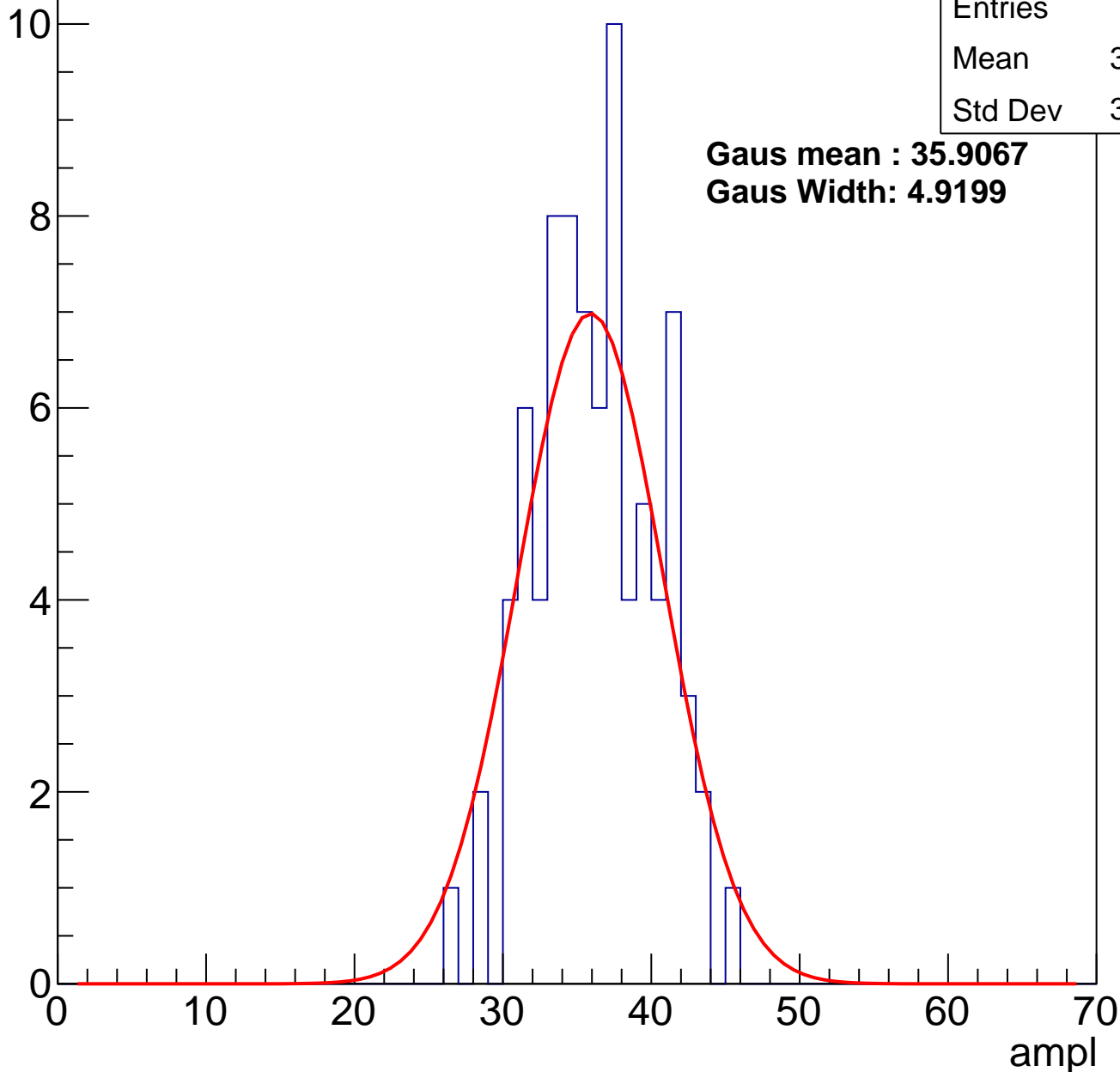
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	82
Mean	35.78
Std Dev	3.966

**Gaus mean : 35.9067**

**Gaus Width: 4.9199**

Entry



# B1L103S, U26-ch74, adc2

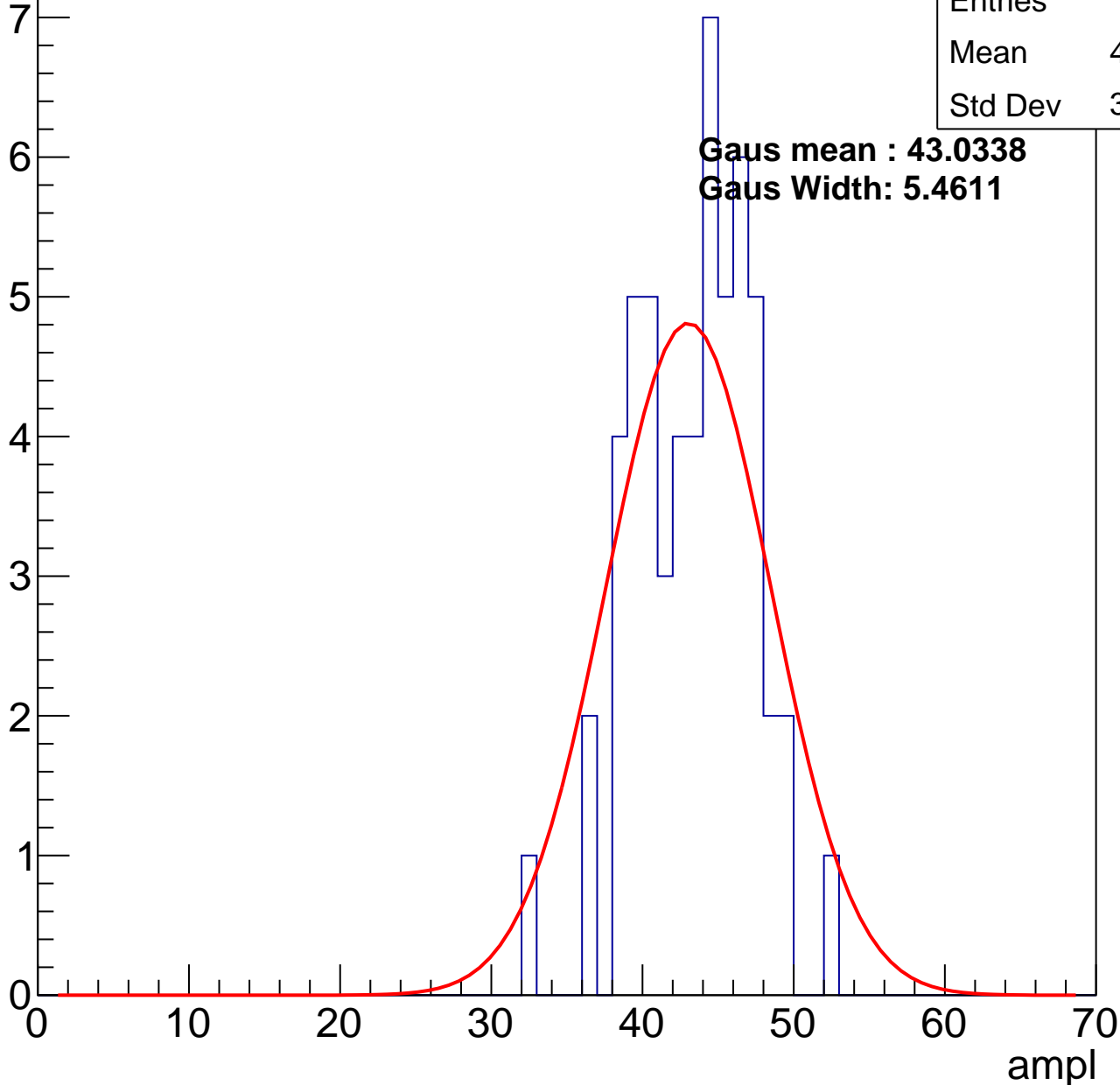
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	42.93
Std Dev	3.835

**Gaus mean : 43.0338**

**Gaus Width: 5.4611**

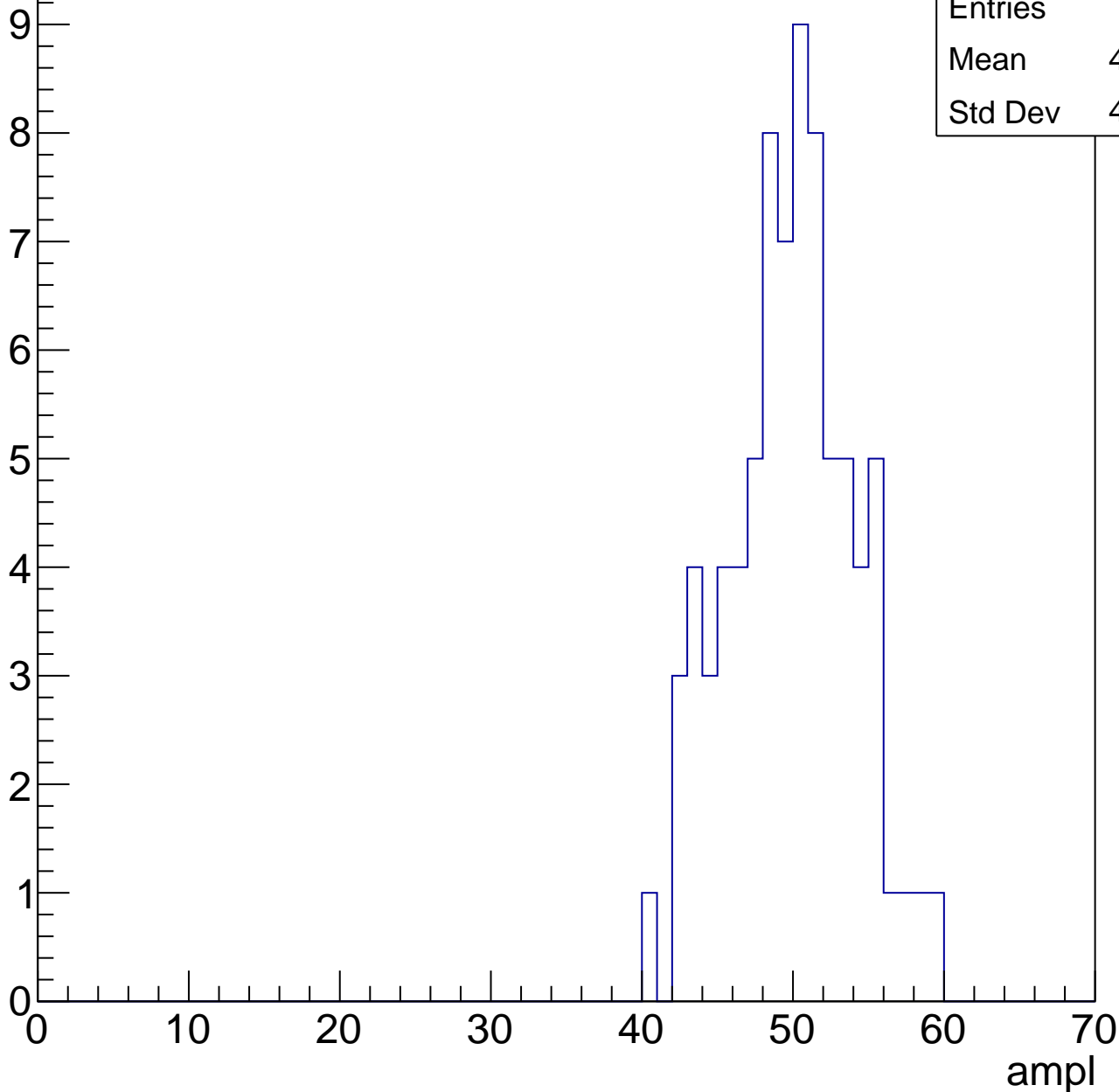


# B1L103S, U26-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	49.37
Std Dev	4.063

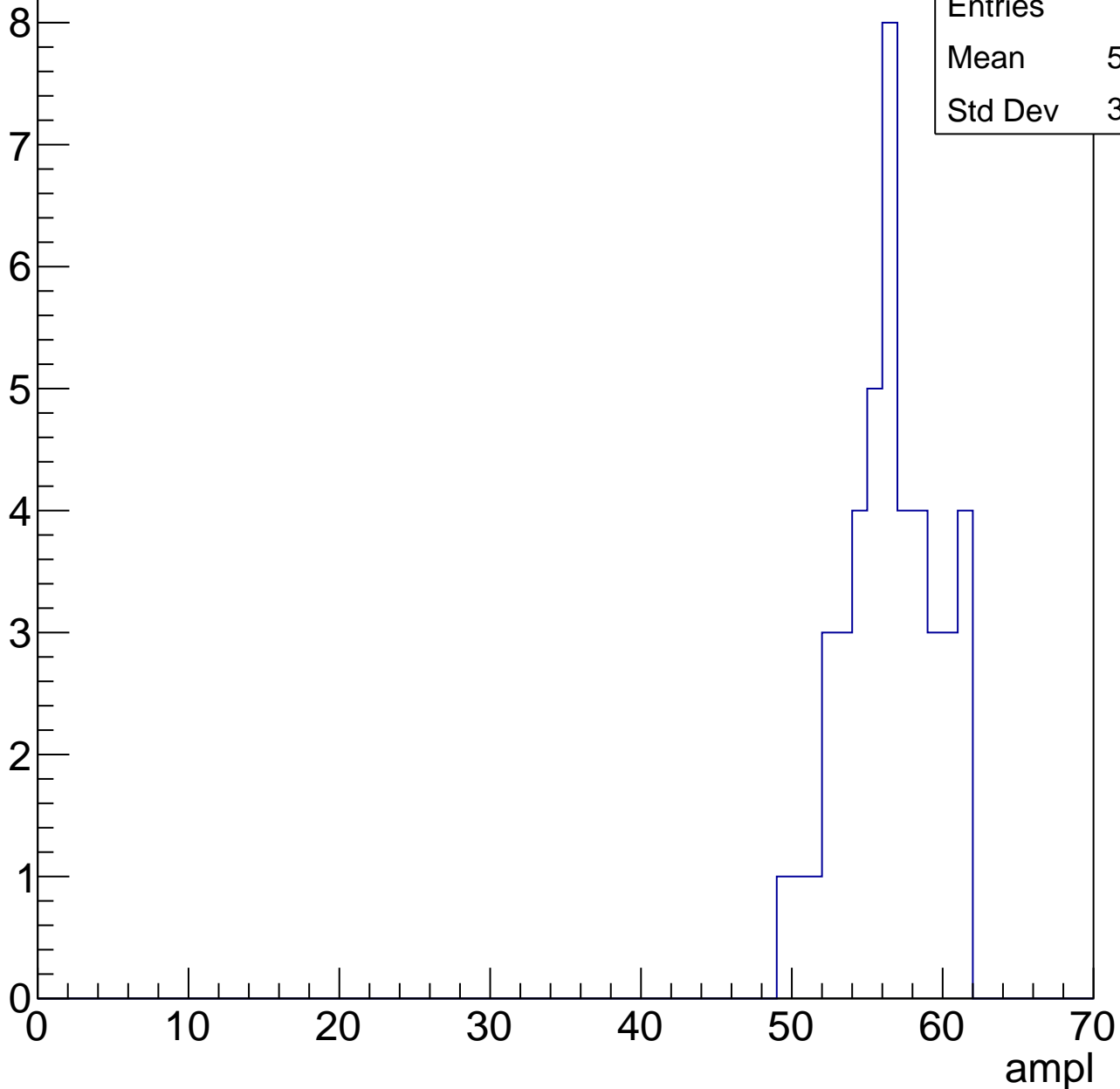


# B1L103S, U26-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	56.02
Std Dev	3.019

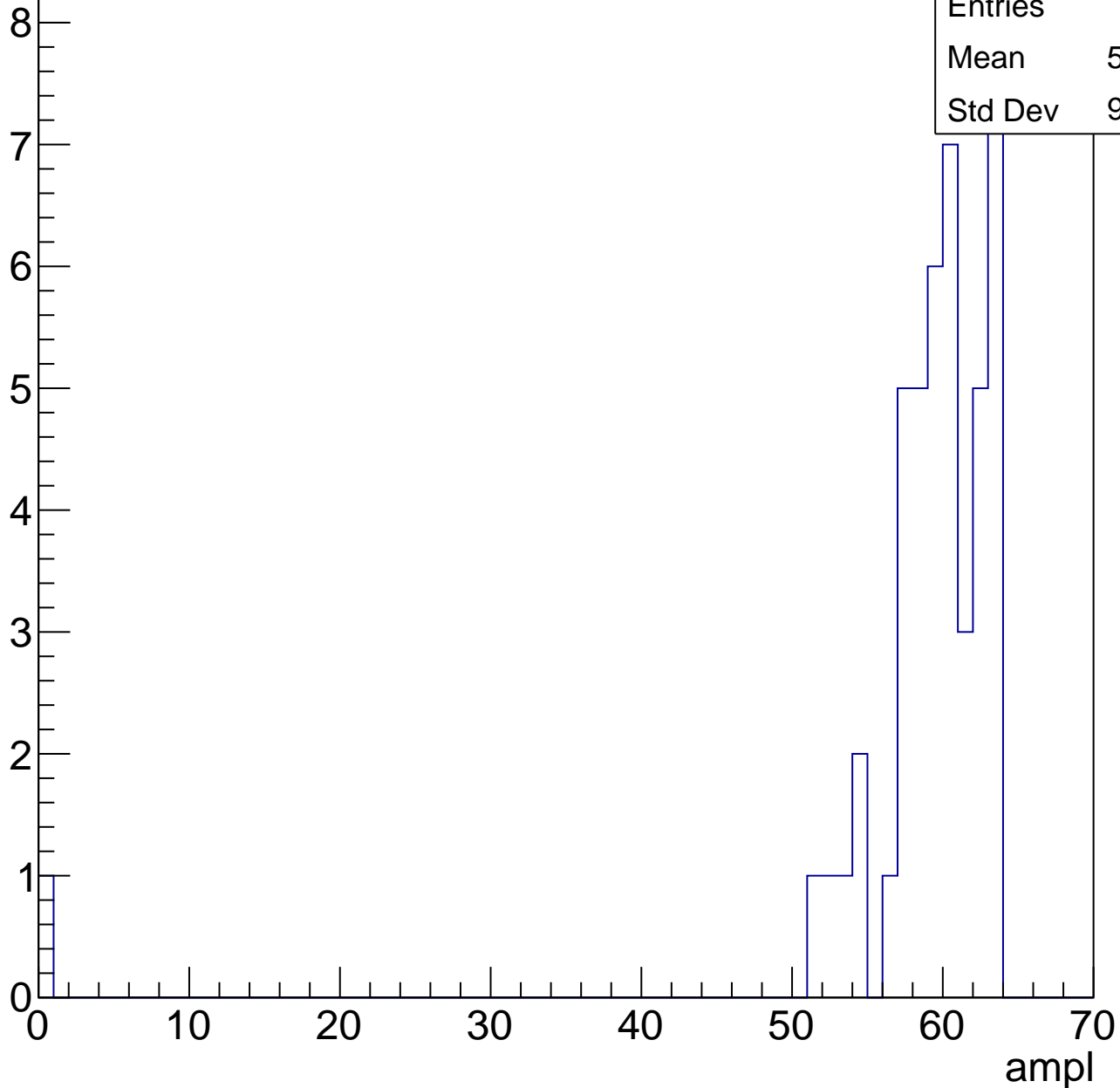


# B1L103S, U26-ch74, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

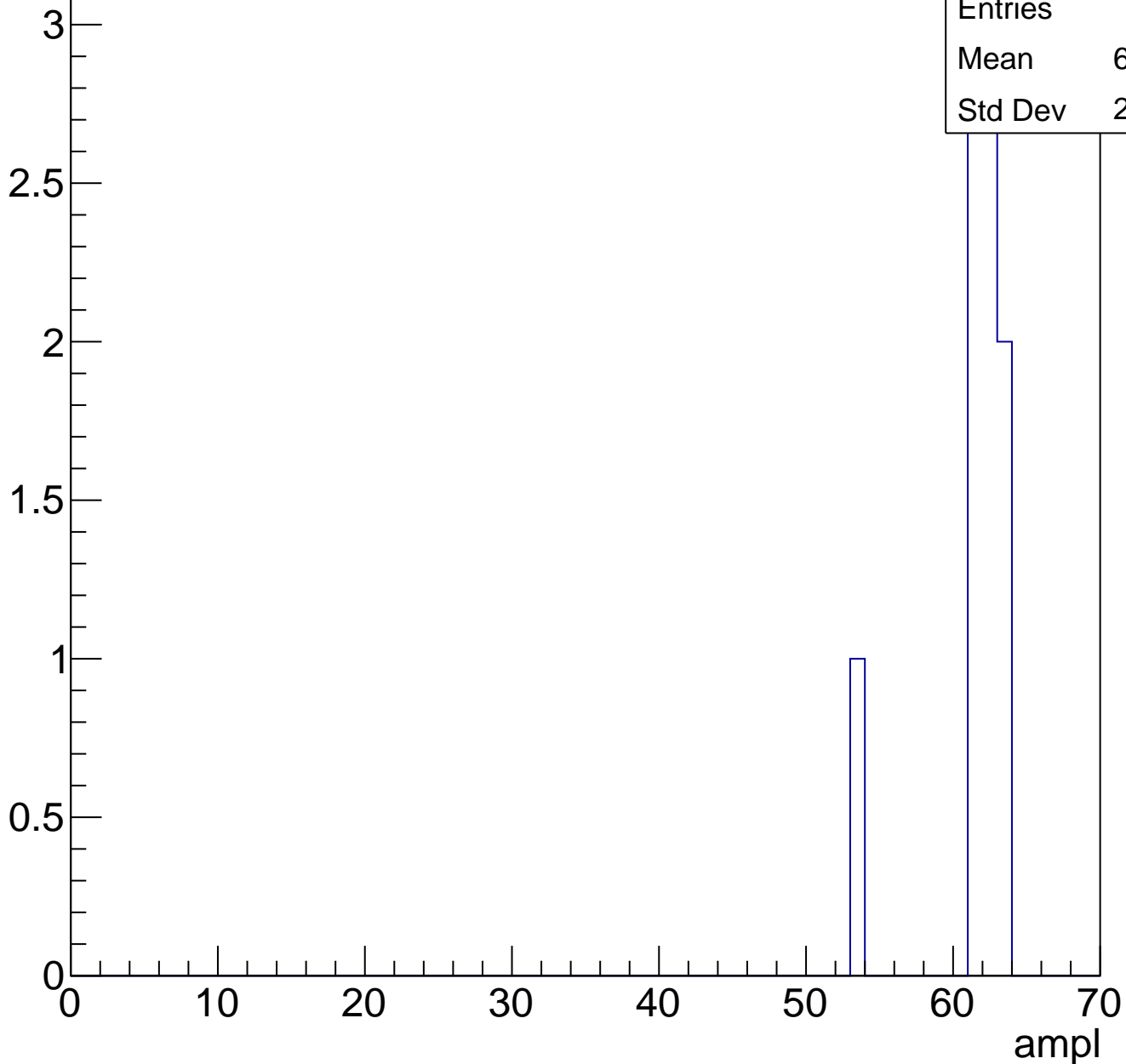
Entries	46
Mean	57.96
Std Dev	9.156



# B1L103S, U26-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch75, adc0

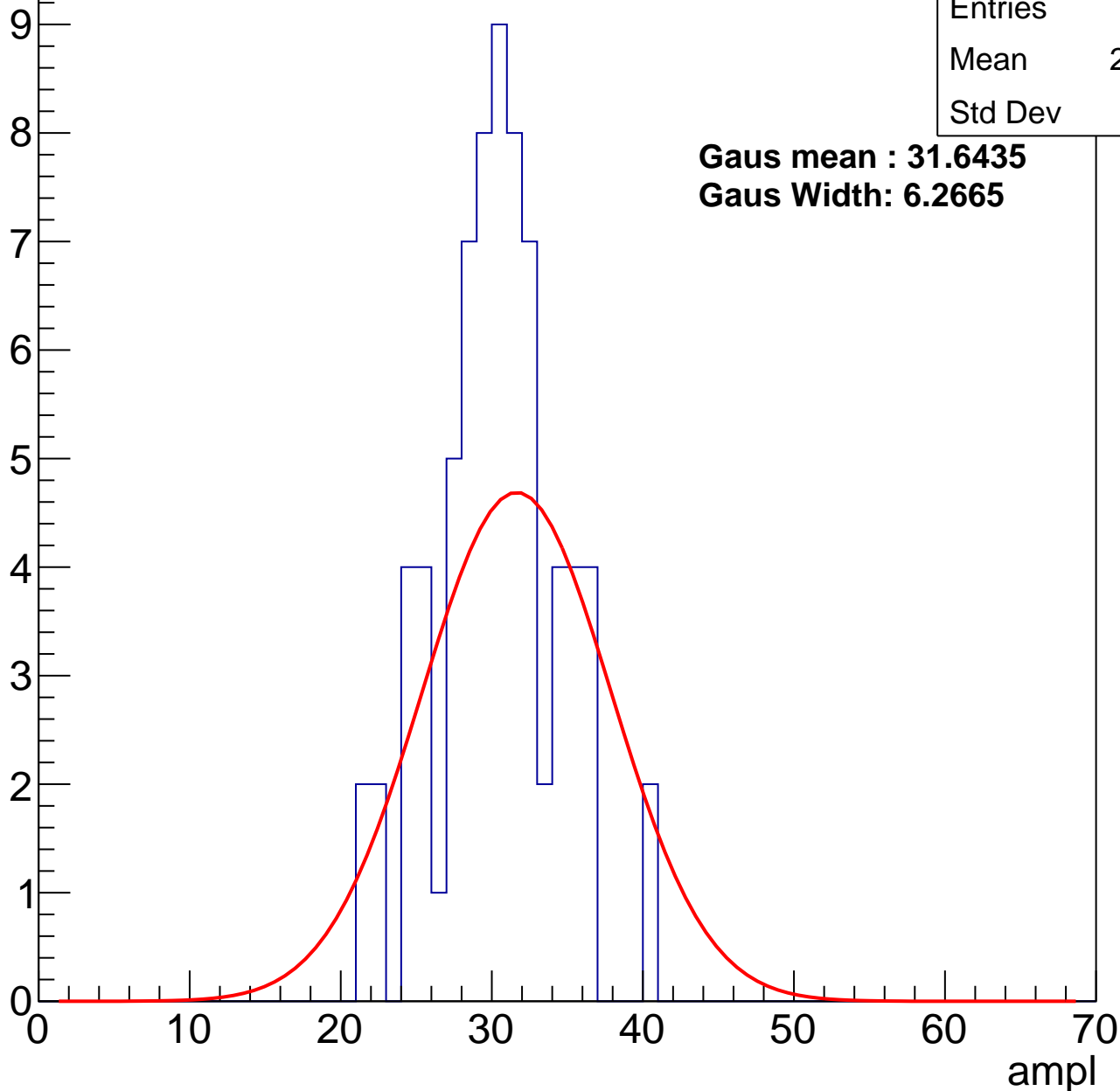
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	29.85
Std Dev	4.04

**Gaus mean : 31.6435**

**Gaus Width: 6.2665**



# B1L103S, U26-ch75, adc1

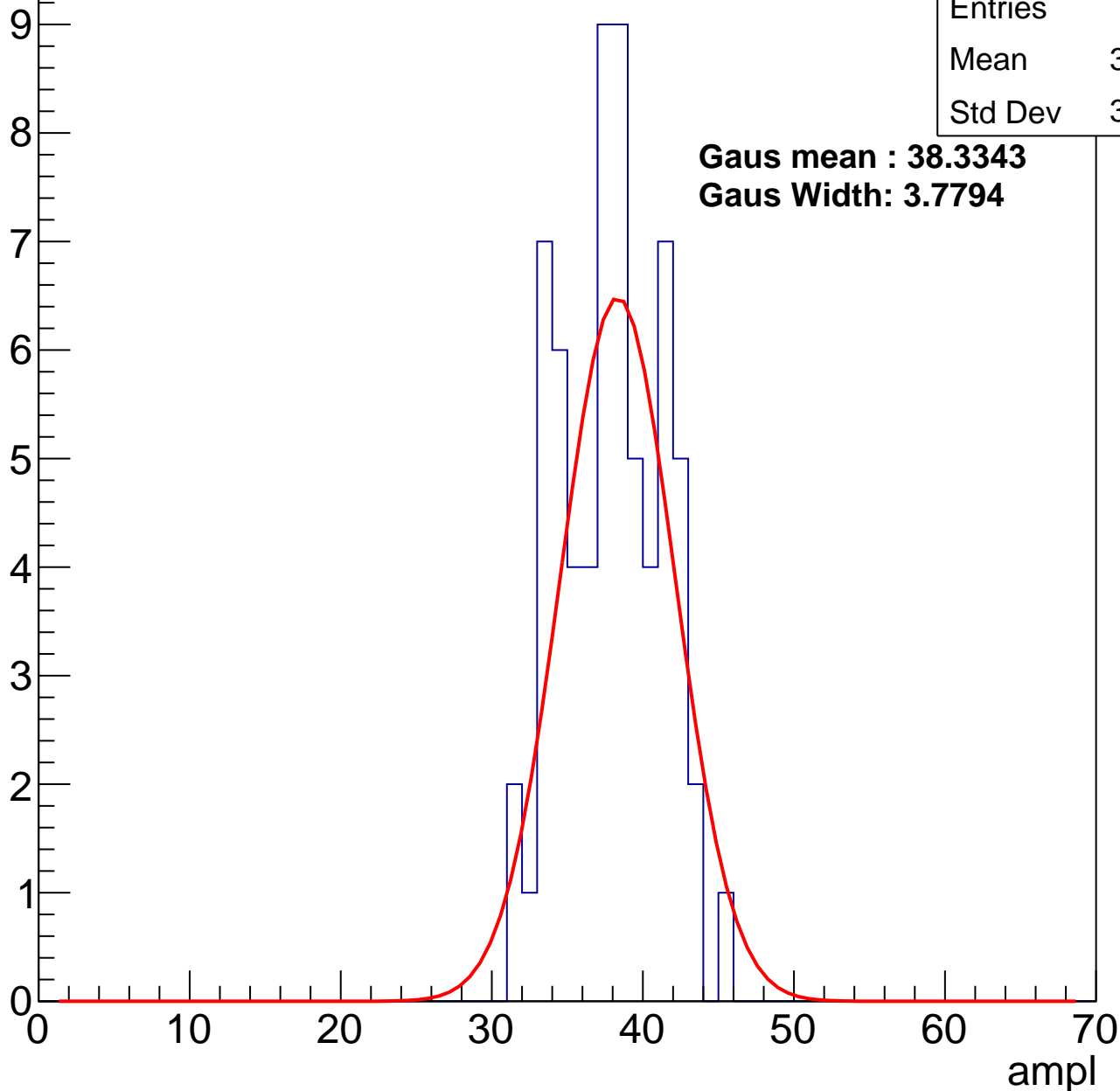
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	37.44
Std Dev	3.276

**Gaus mean : 38.3343**

**Gaus Width: 3.7794**



# B1L103S, U26-ch75, adc2

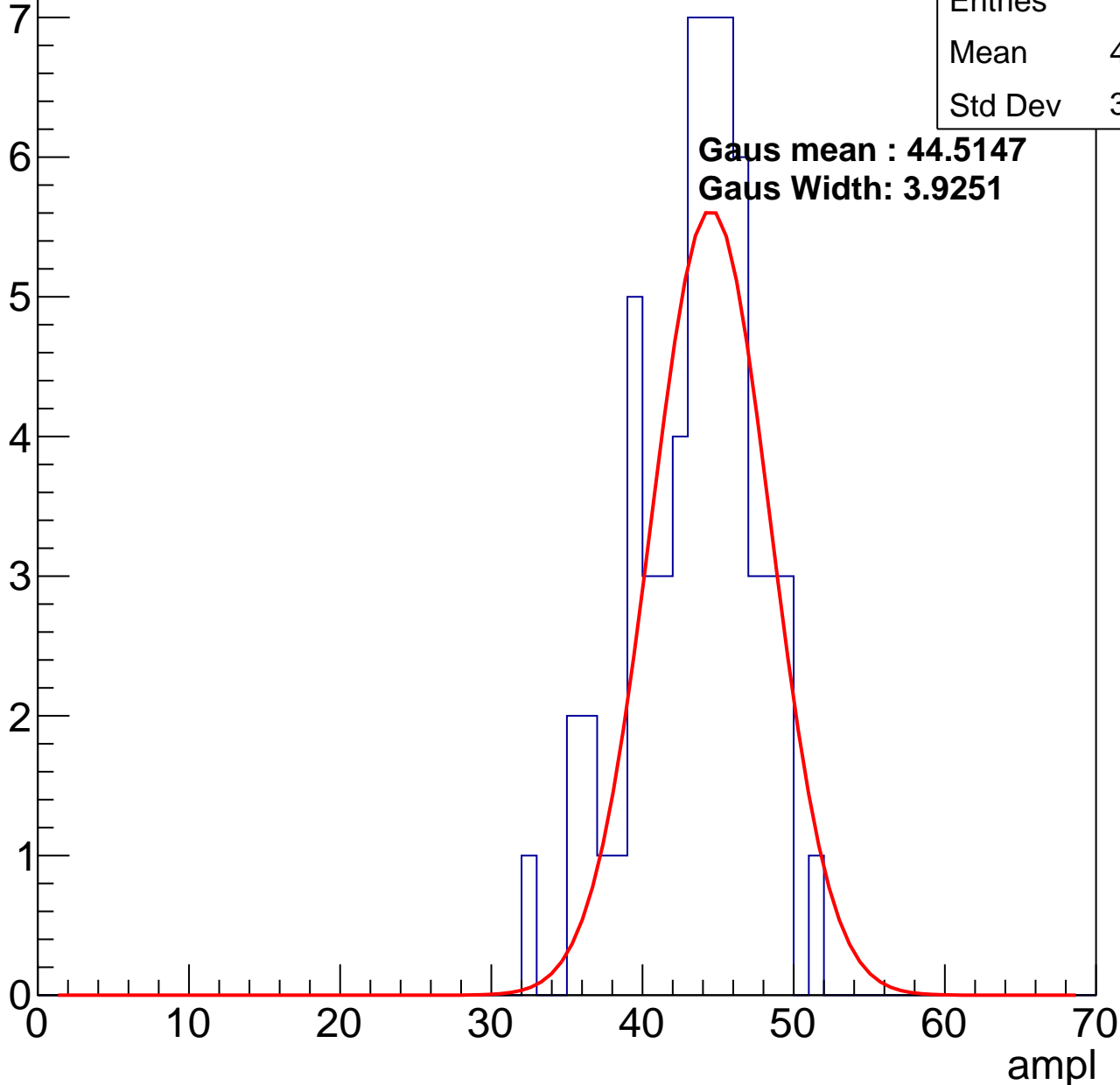
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	43.02
Std Dev	3.938

**Gaus mean : 44.5147**

**Gaus Width: 3.9251**



# B1L103S, U26-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	78
Mean	50.12
Std Dev	3.755

Entry

10

8

6

4

2

0

0

10

20

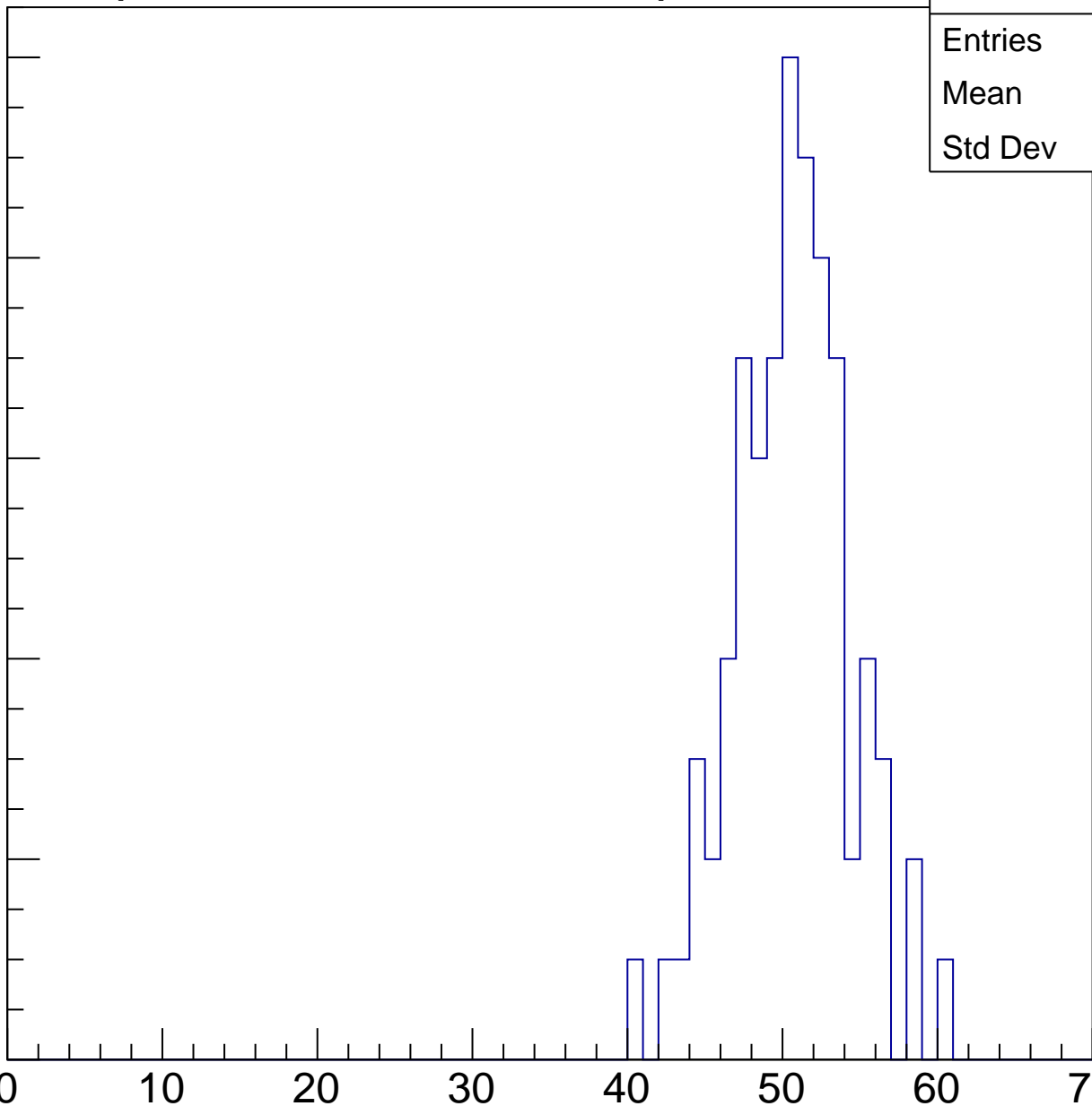
30

40

50

60

ampl

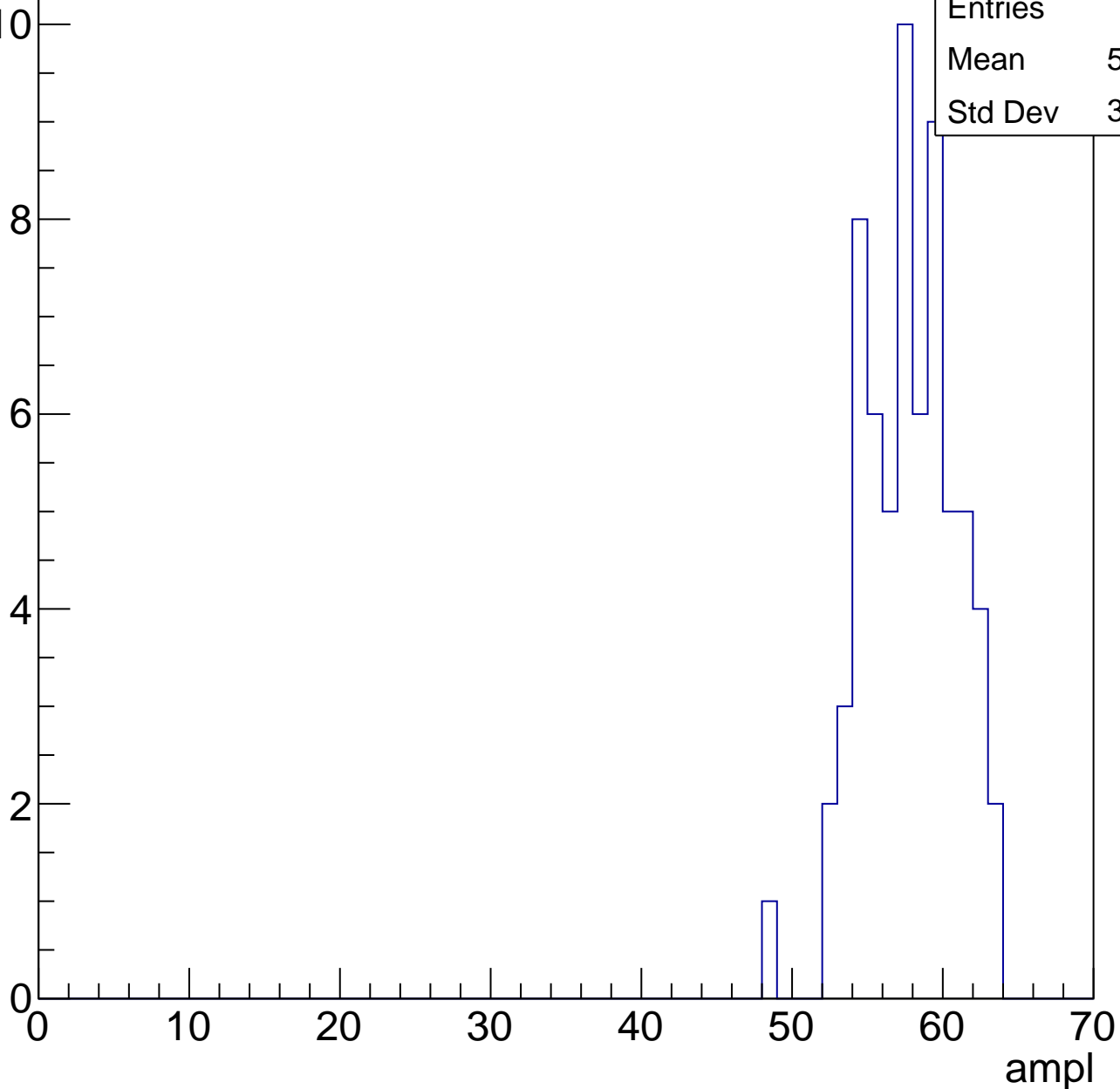


# B1L103S, U26-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	57.29
Std Dev	3.049

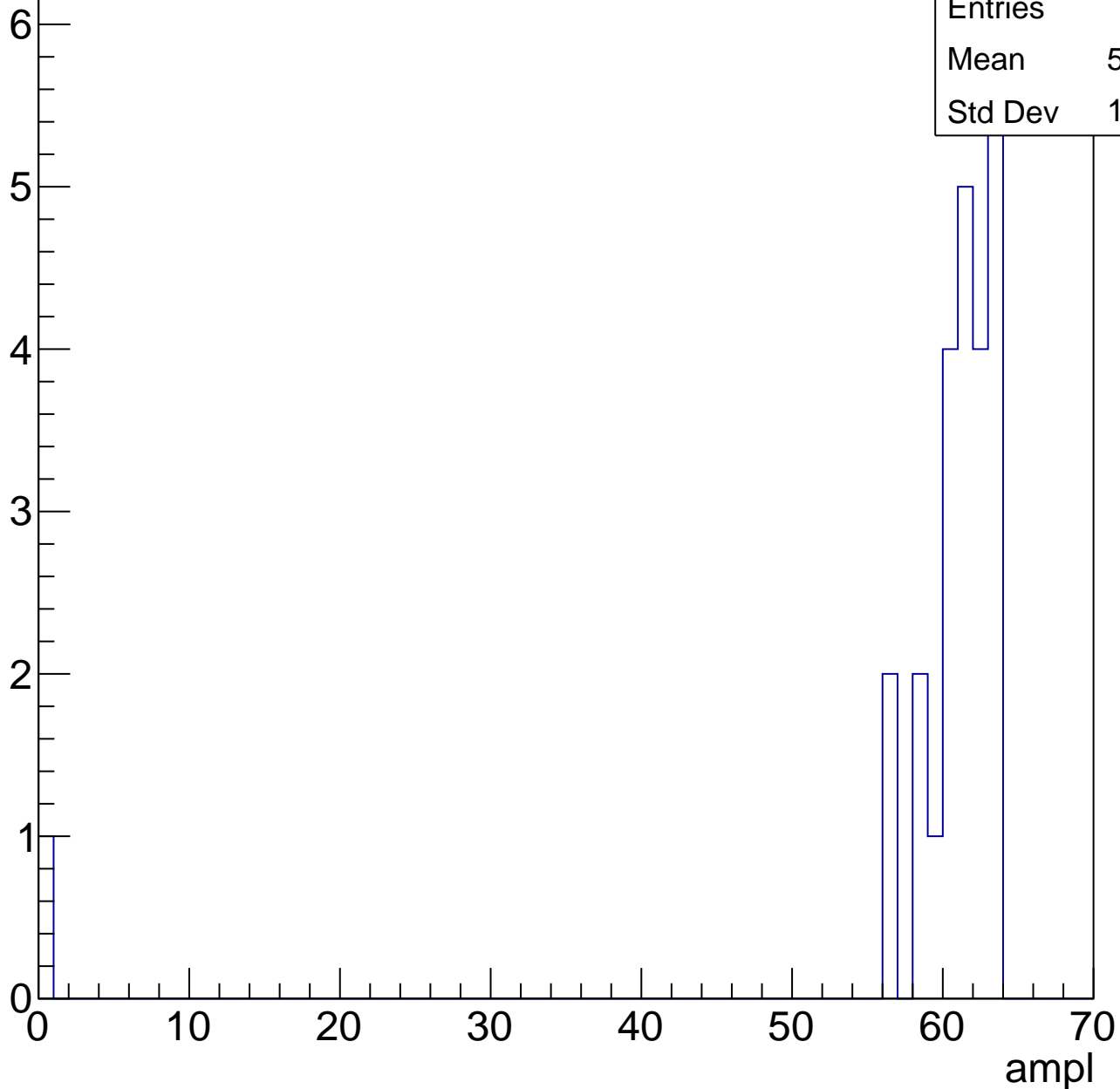


# B1L103S, U26-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	25
Mean	58.32
Std Dev	12.08



# B1L103S, U26-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U26-ch76, adc0

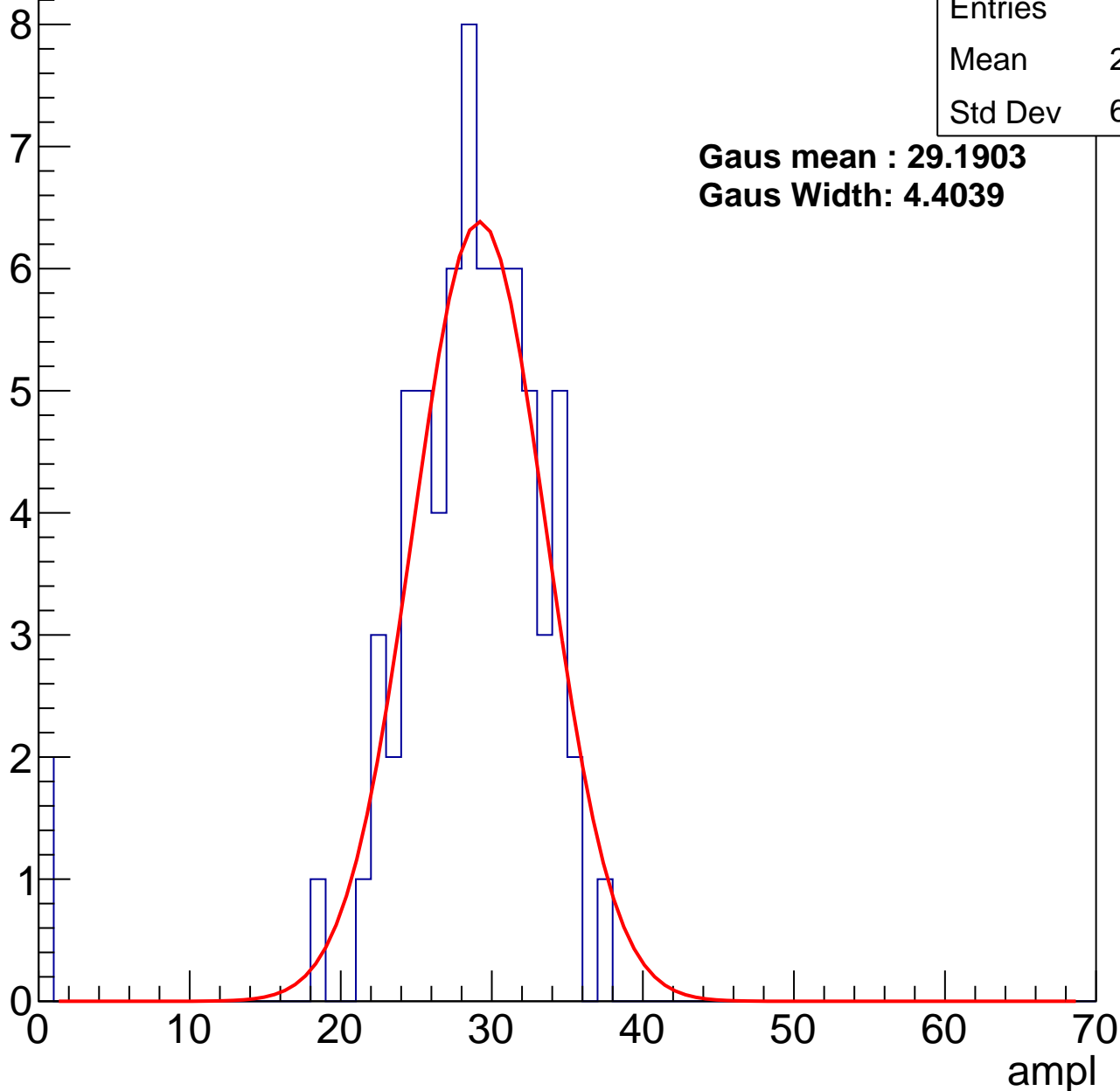
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	27.63
Std Dev	6.064

**Gaus mean : 29.1903**

**Gaus Width: 4.4039**



# B1L103S, U26-ch76, adc1

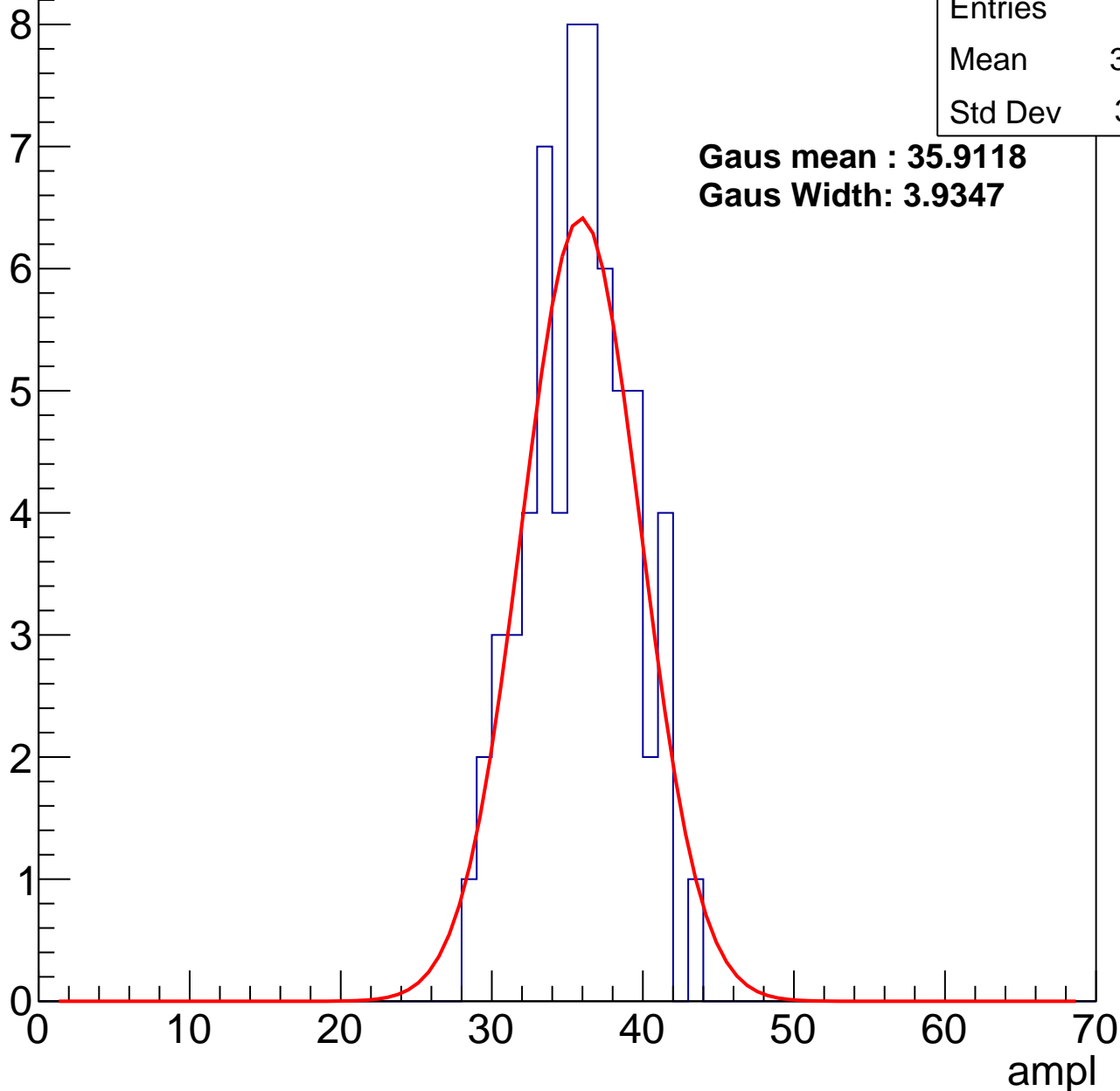
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	35.33
Std Dev	3.381

**Gaus mean : 35.9118**

**Gaus Width: 3.9347**



# B1L103S, U26-ch76, adc2

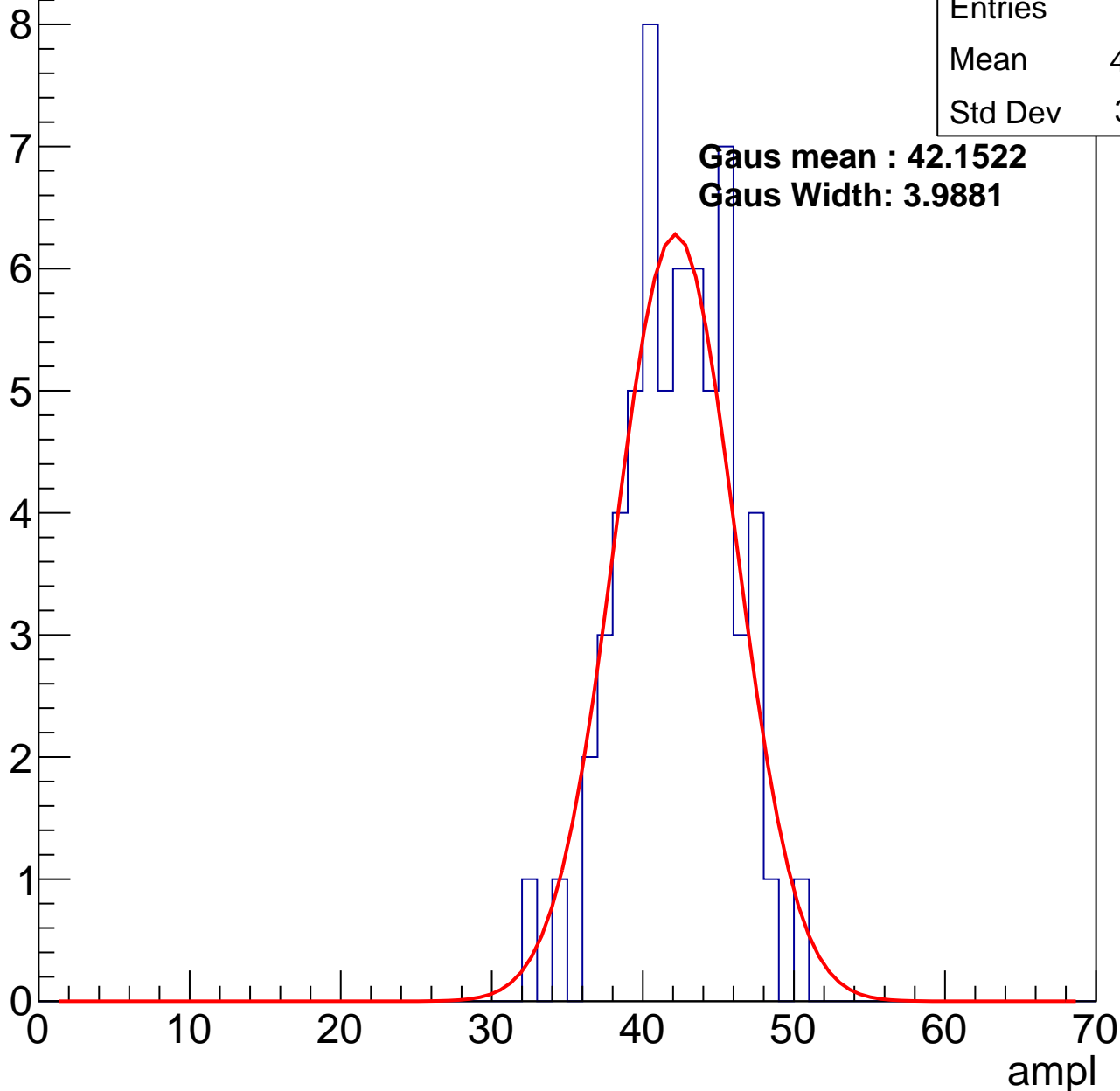
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	41.77
Std Dev	3.571

**Gaus mean : 42.1522**

**Gaus Width: 3.9881**

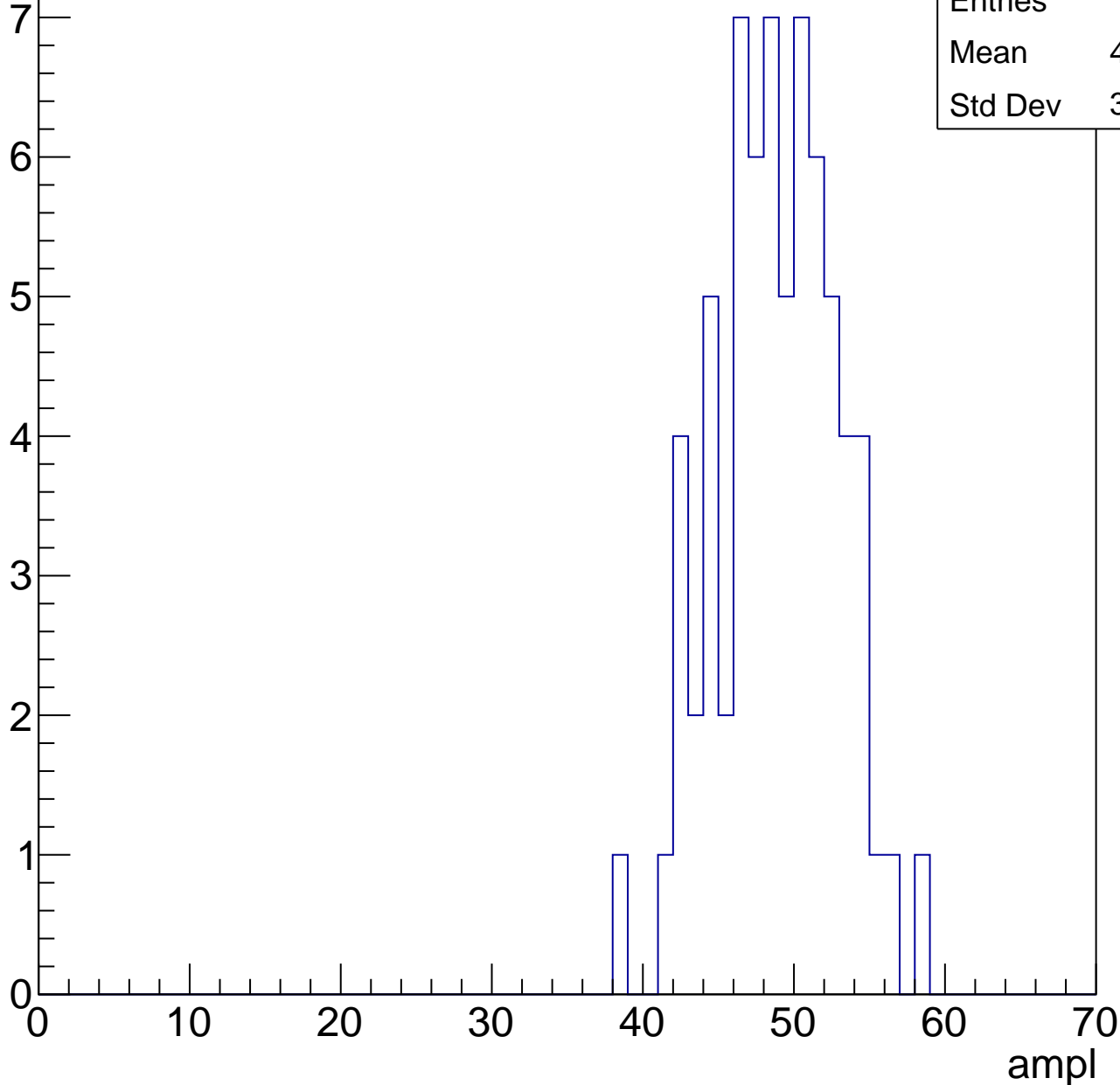


# B1L103S, U26-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	48.42
Std Dev	3.969

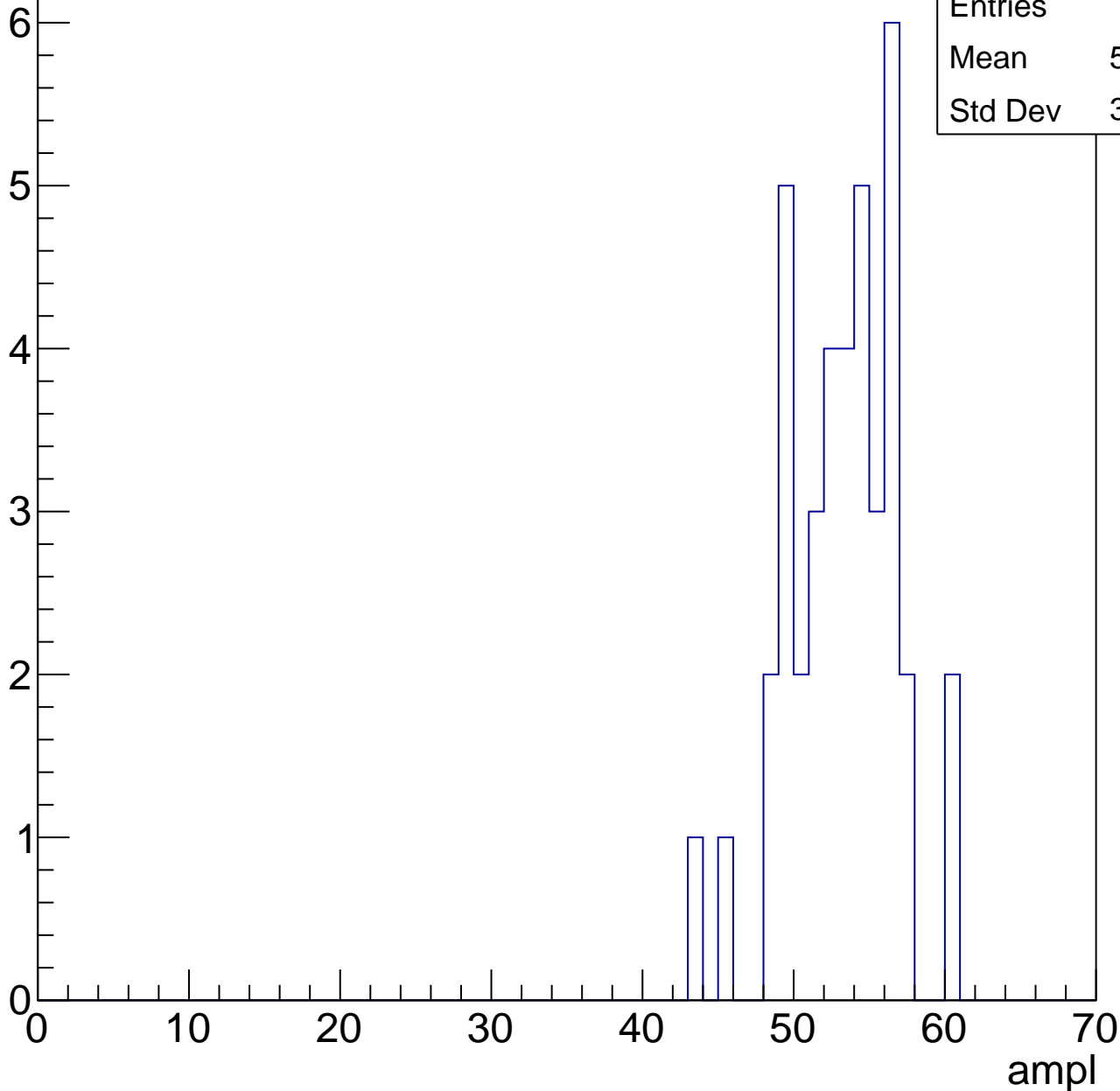


# B1L103S, U26-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

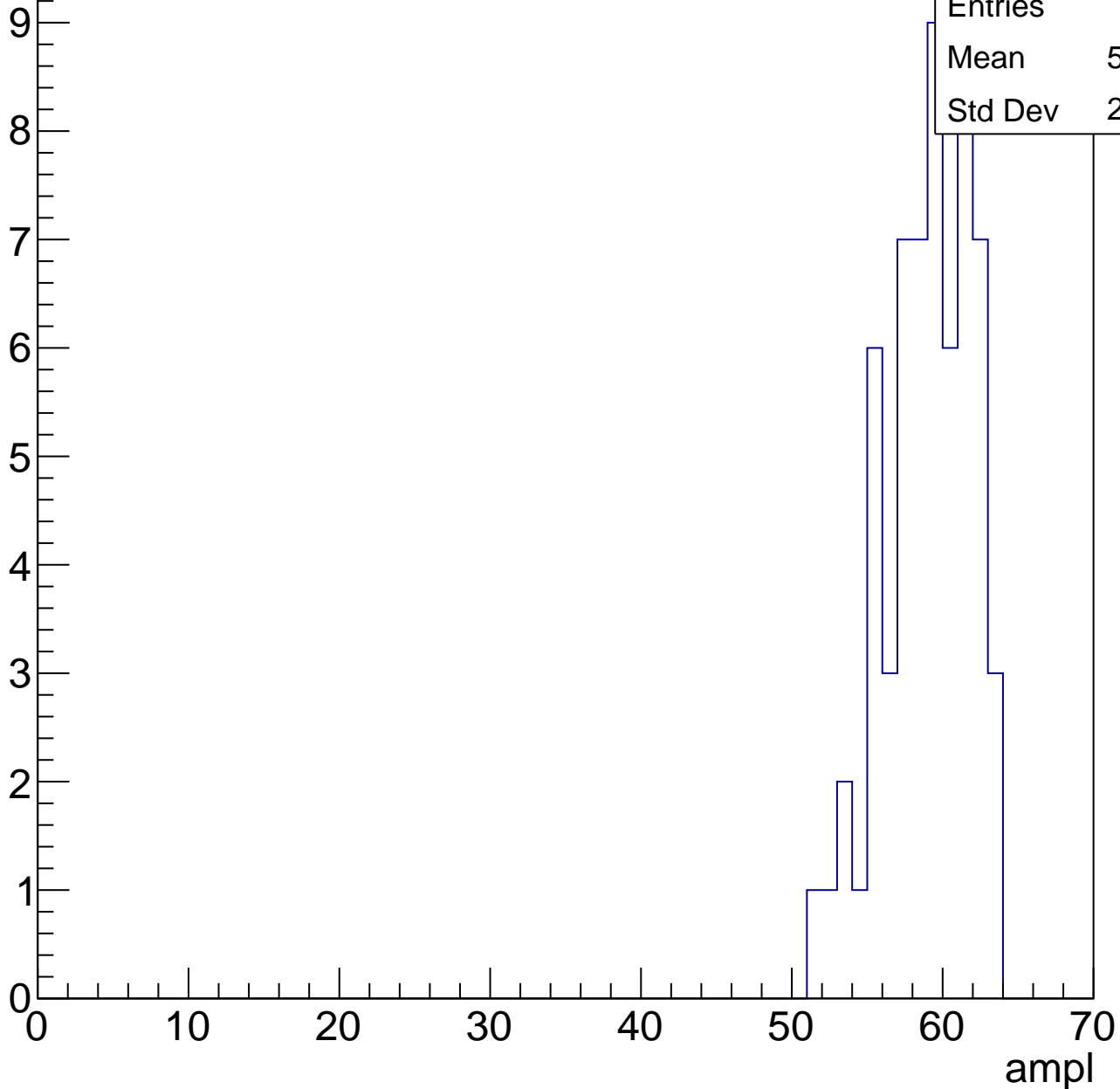
Entries	40
Mean	52.67
Std Dev	3.622



# B1L103S, U26-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

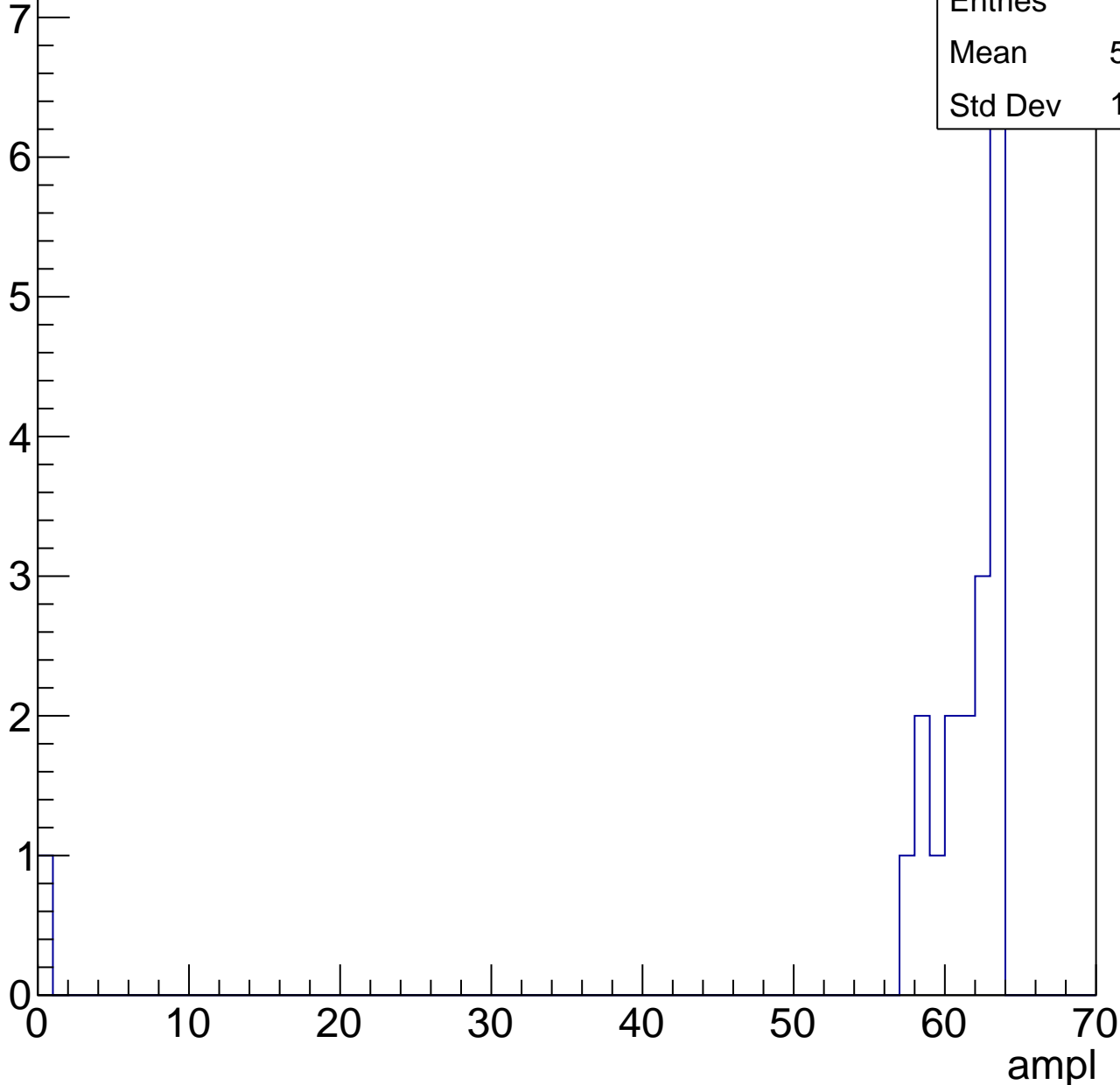


# B1L103S, U26-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	19
Mean	57.95
Std Dev	13.79





# B1L103S, U26-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U26-ch77, adc0

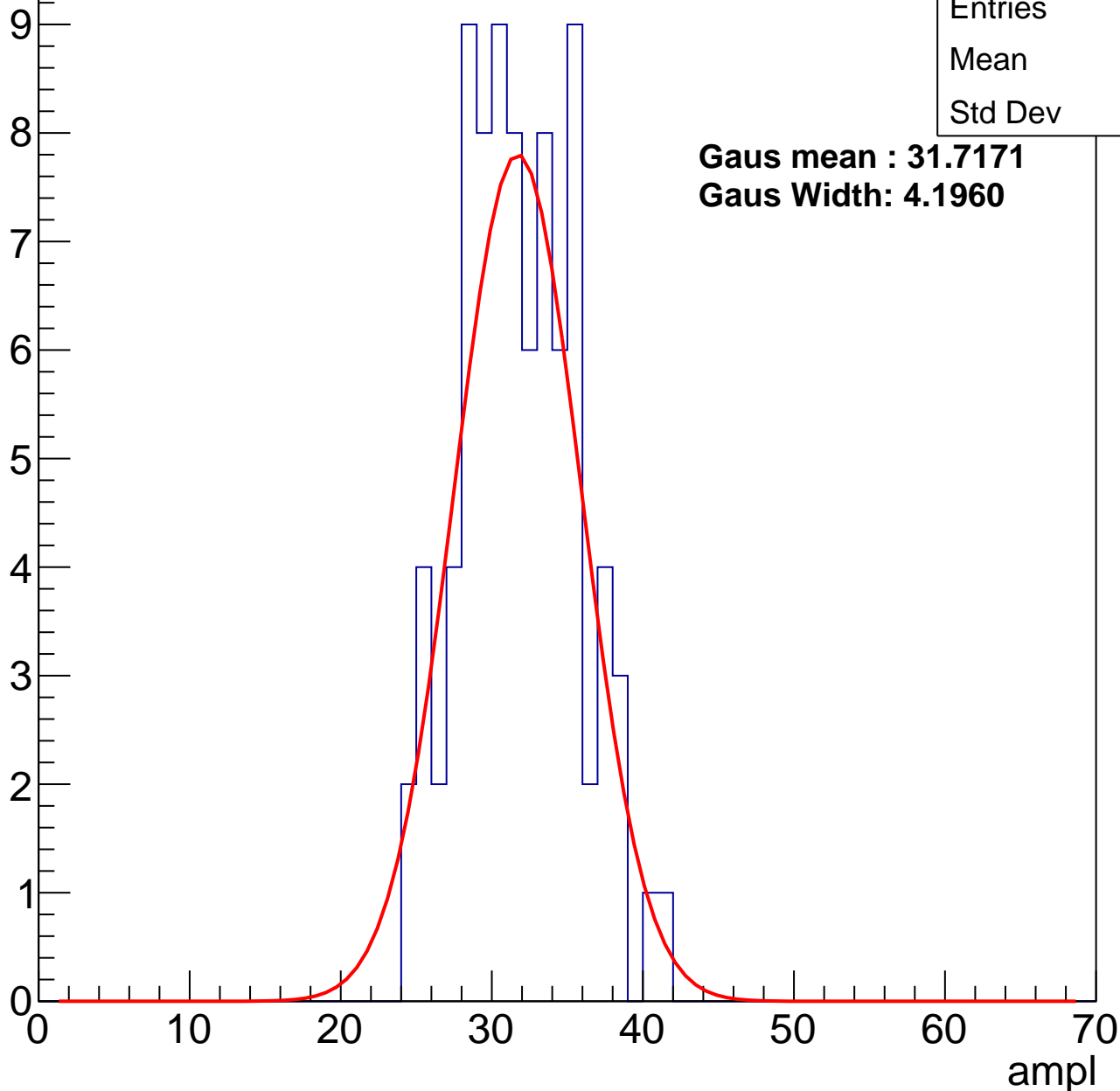
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	86
Mean	31.4
Std Dev	3.77

**Gaus mean : 31.7171**

**Gaus Width: 4.1960**



# B1L103S, U26-ch77, adc1

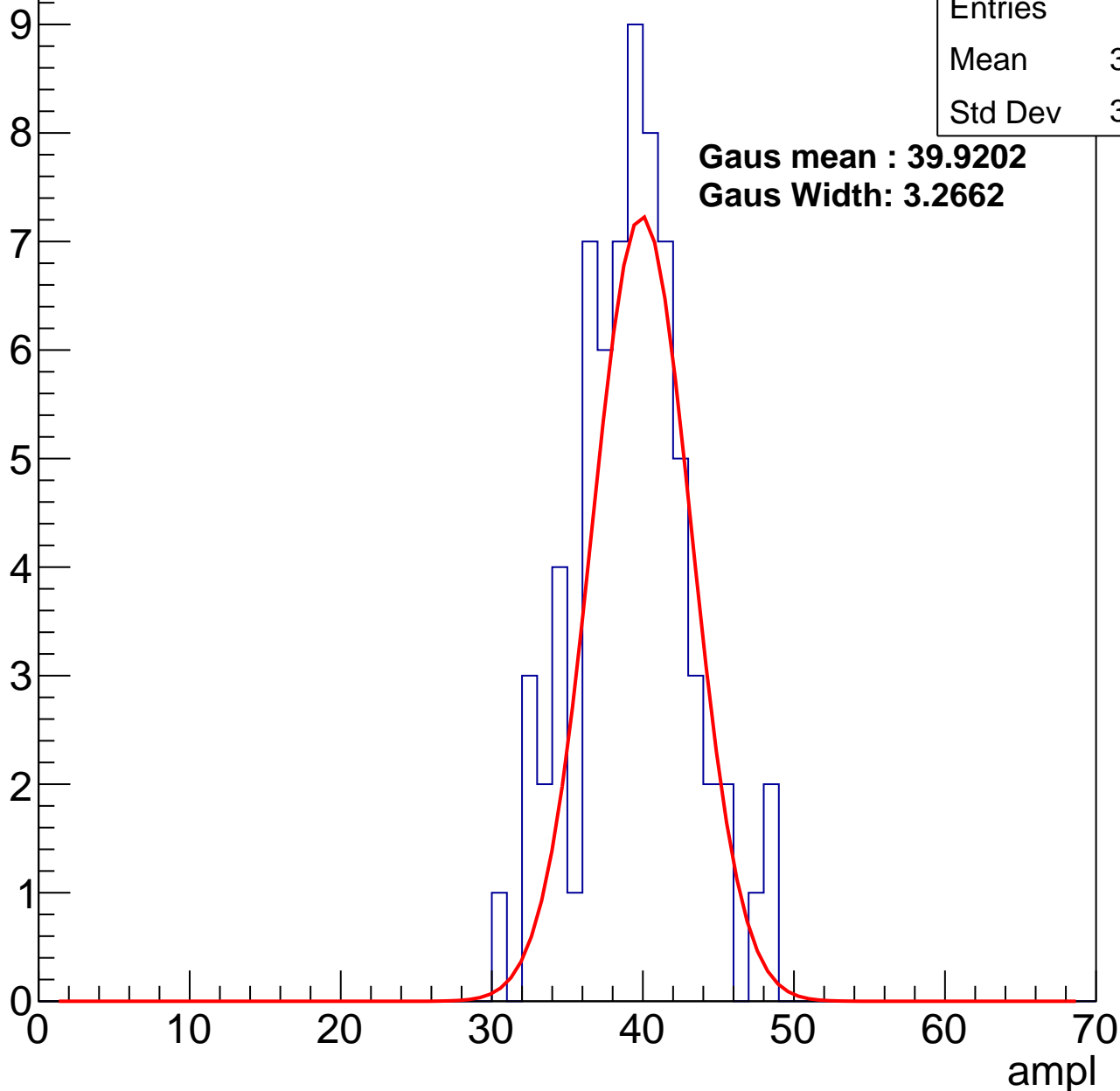
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	38.87
Std Dev	3.753

**Gaus mean : 39.9202**

**Gaus Width: 3.2662**



# B1L103S, U26-ch77, adc2

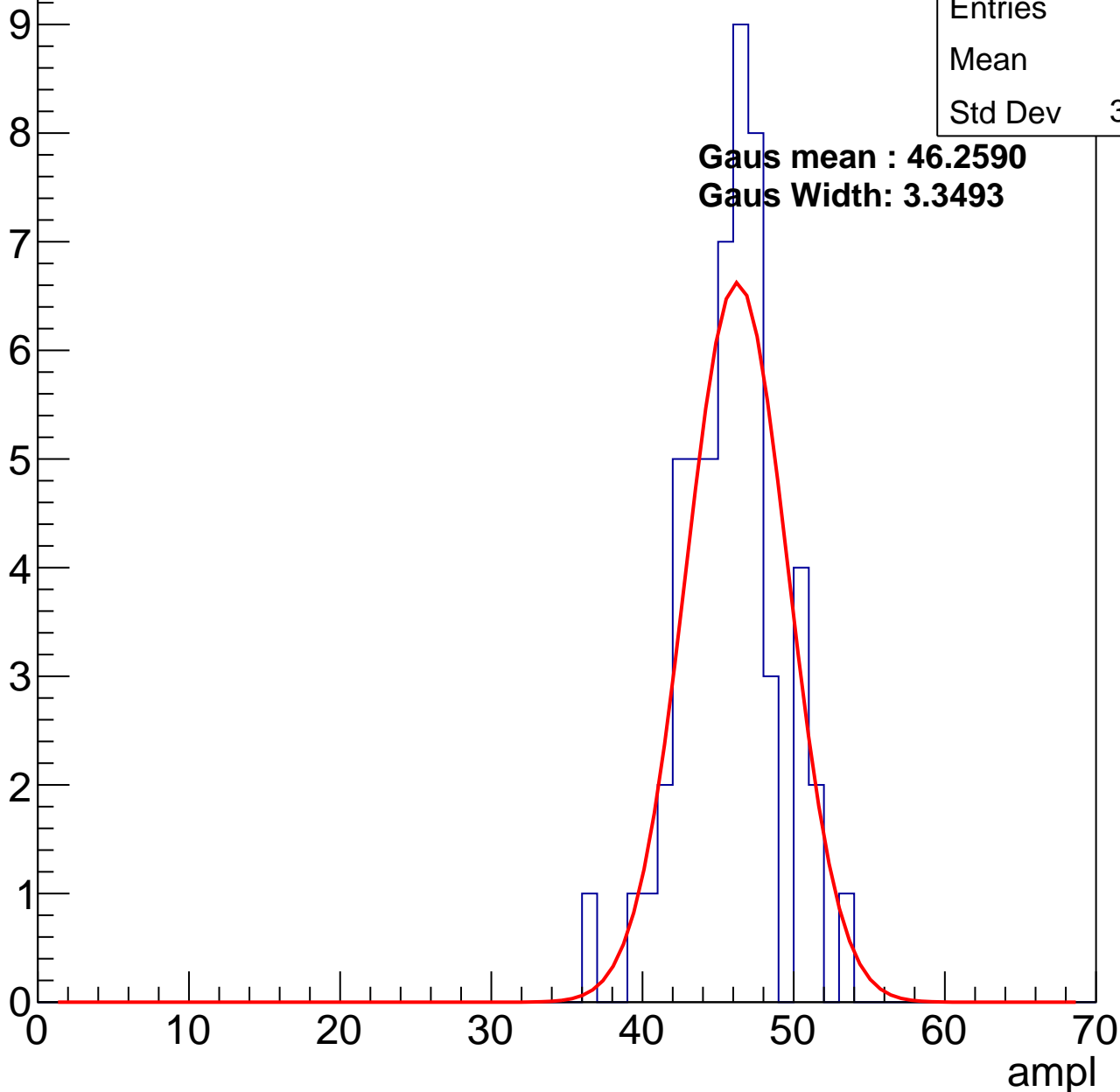
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	45.3
Std Dev	3.172

**Gaus mean : 46.2590**

**Gaus Width: 3.3493**

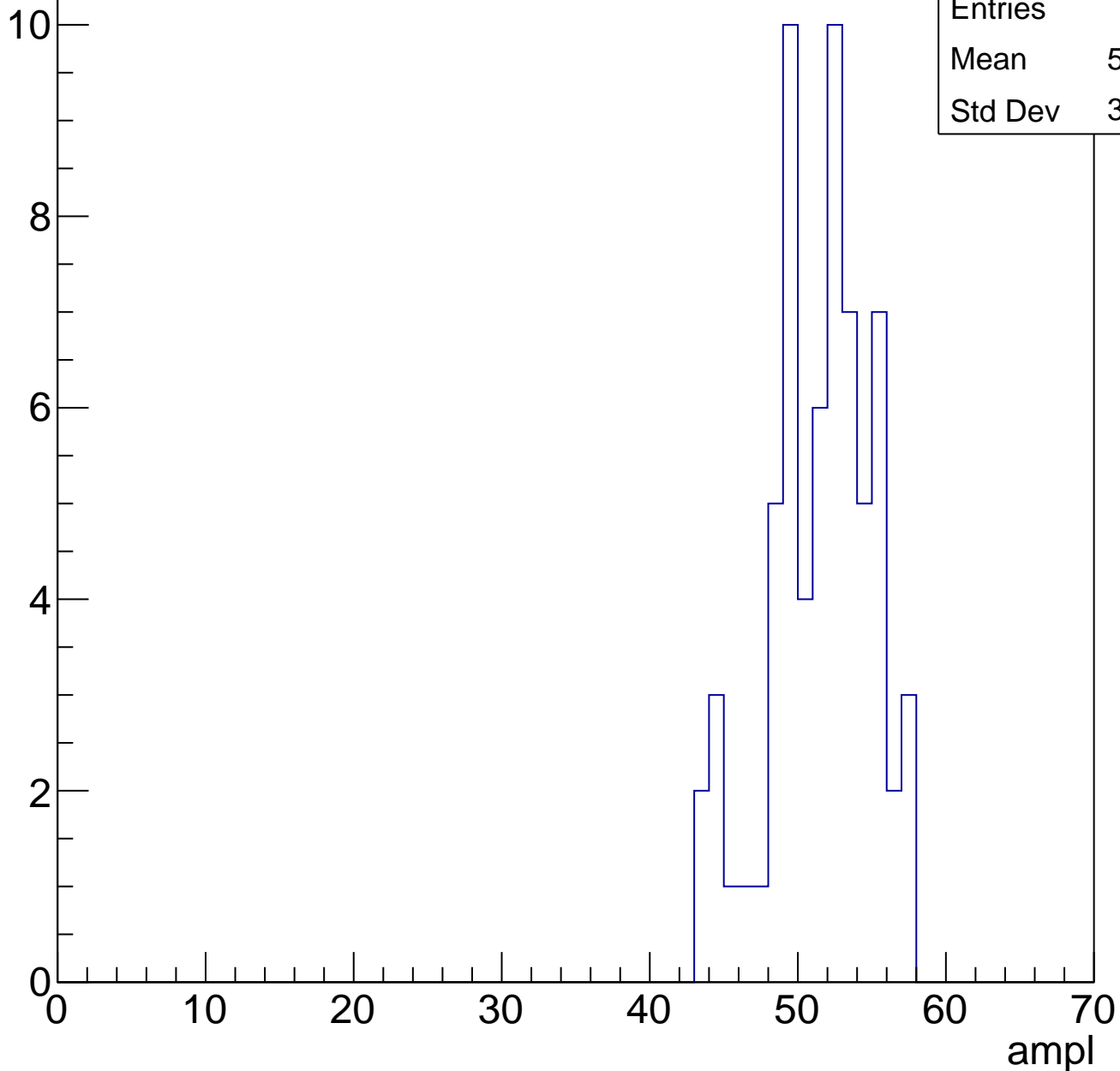


# B1L103S, U26-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	51.06
Std Dev	3.442

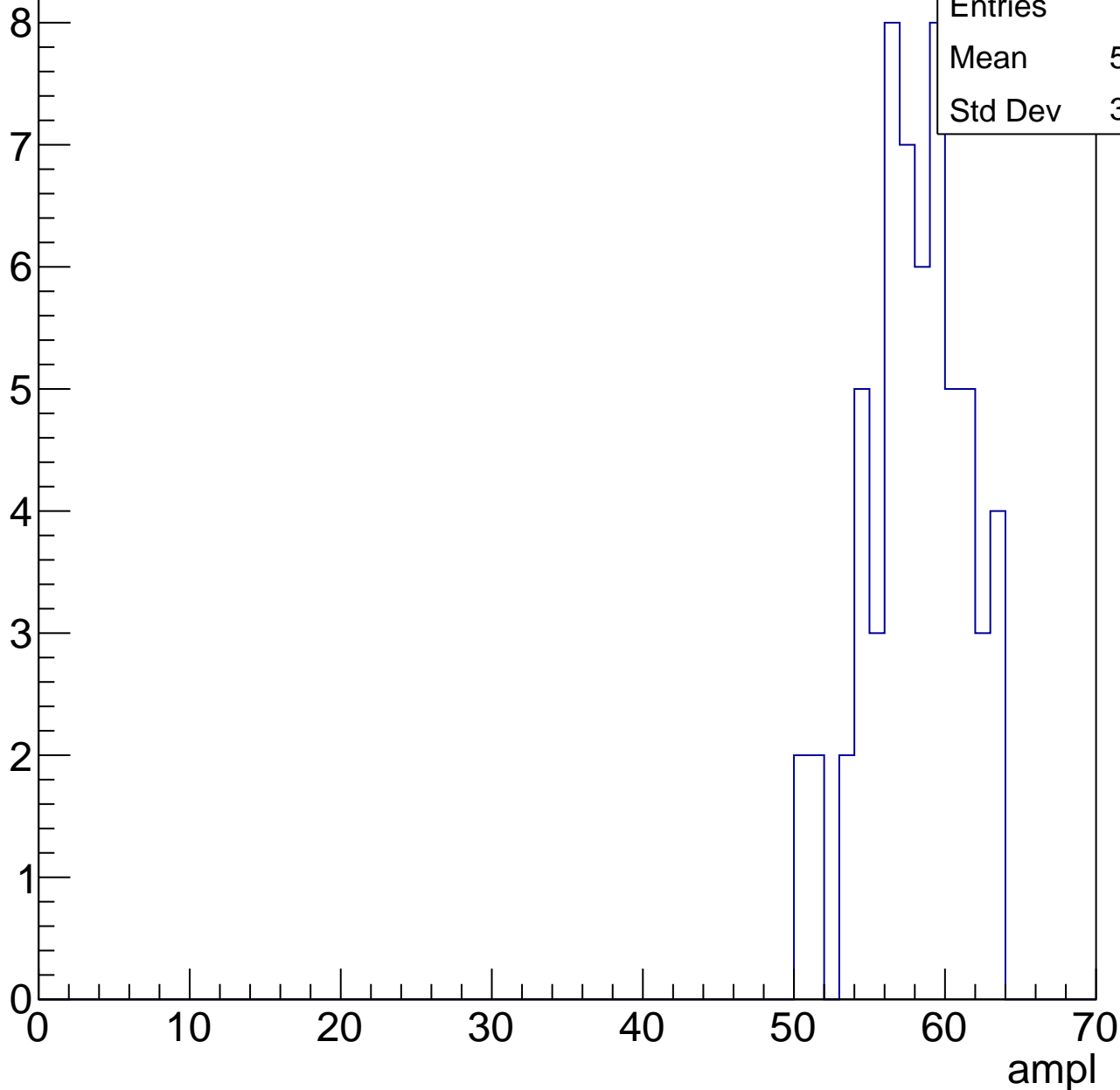


# B1L103S, U26-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	57.55
Std Dev	3.243

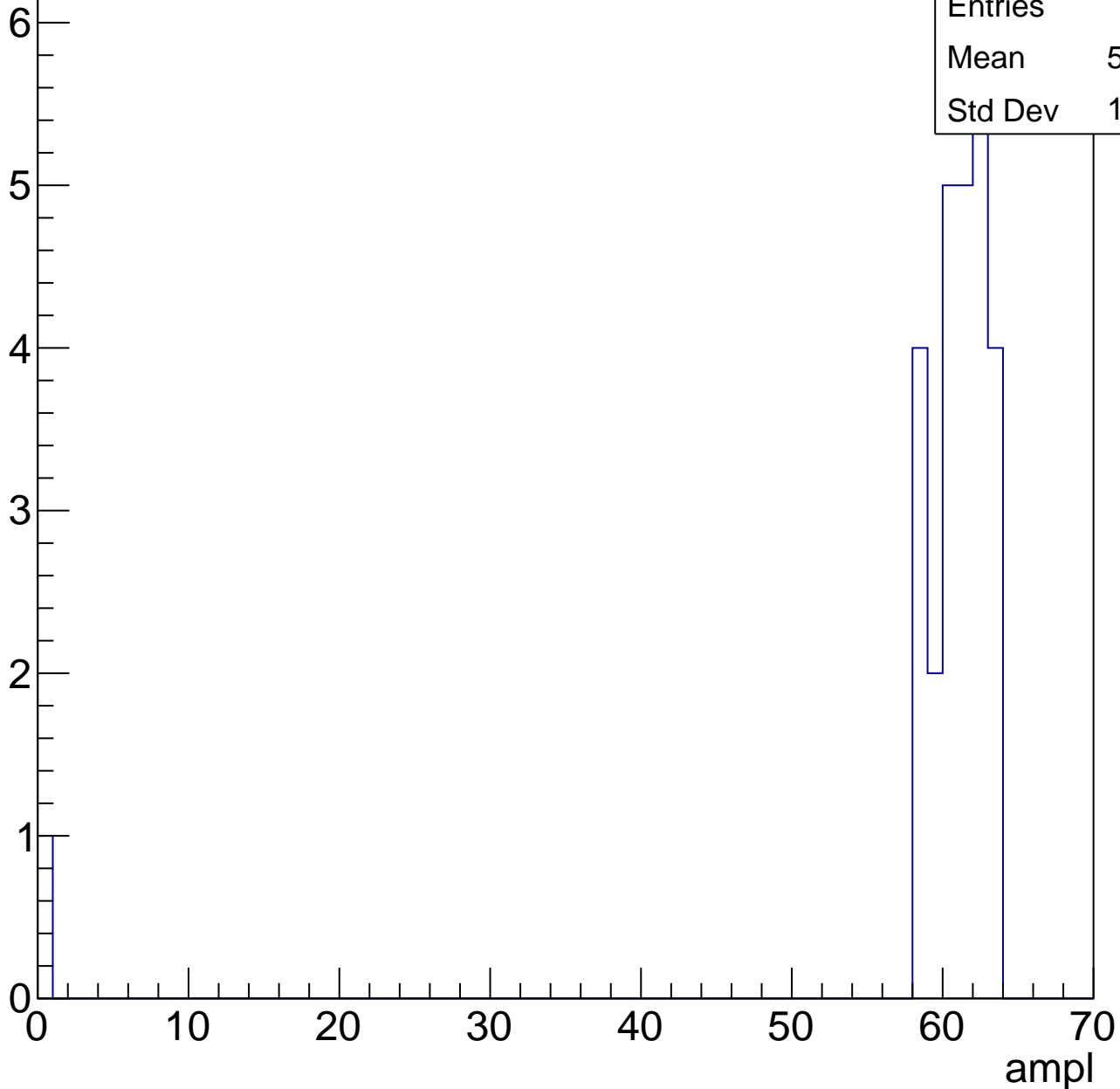


# B1L103S, U26-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	27
Mean	58.48
Std Dev	11.58



# B1L103S, U26-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	23
Std Dev	0

# B1L103S, U26-ch78, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

6  
5  
4  
3  
2  
1  
0

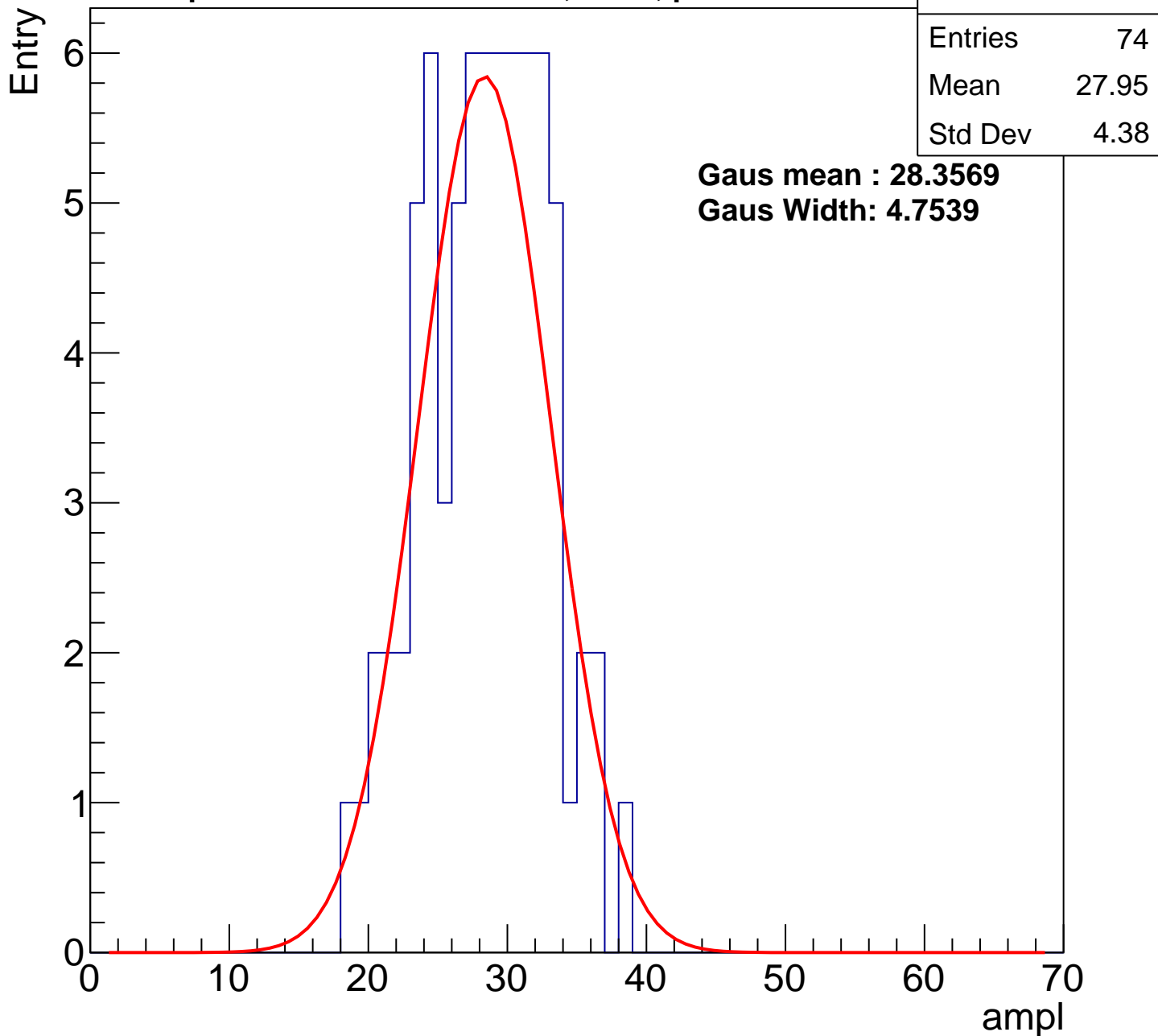
Entries	74
Mean	27.95
Std Dev	4.38

**Gaus mean : 28.3569**

**Gaus Width: 4.7539**

0 10 20 30 40 50 60 70

ampl



# B1L103S, U26-ch78, adc1

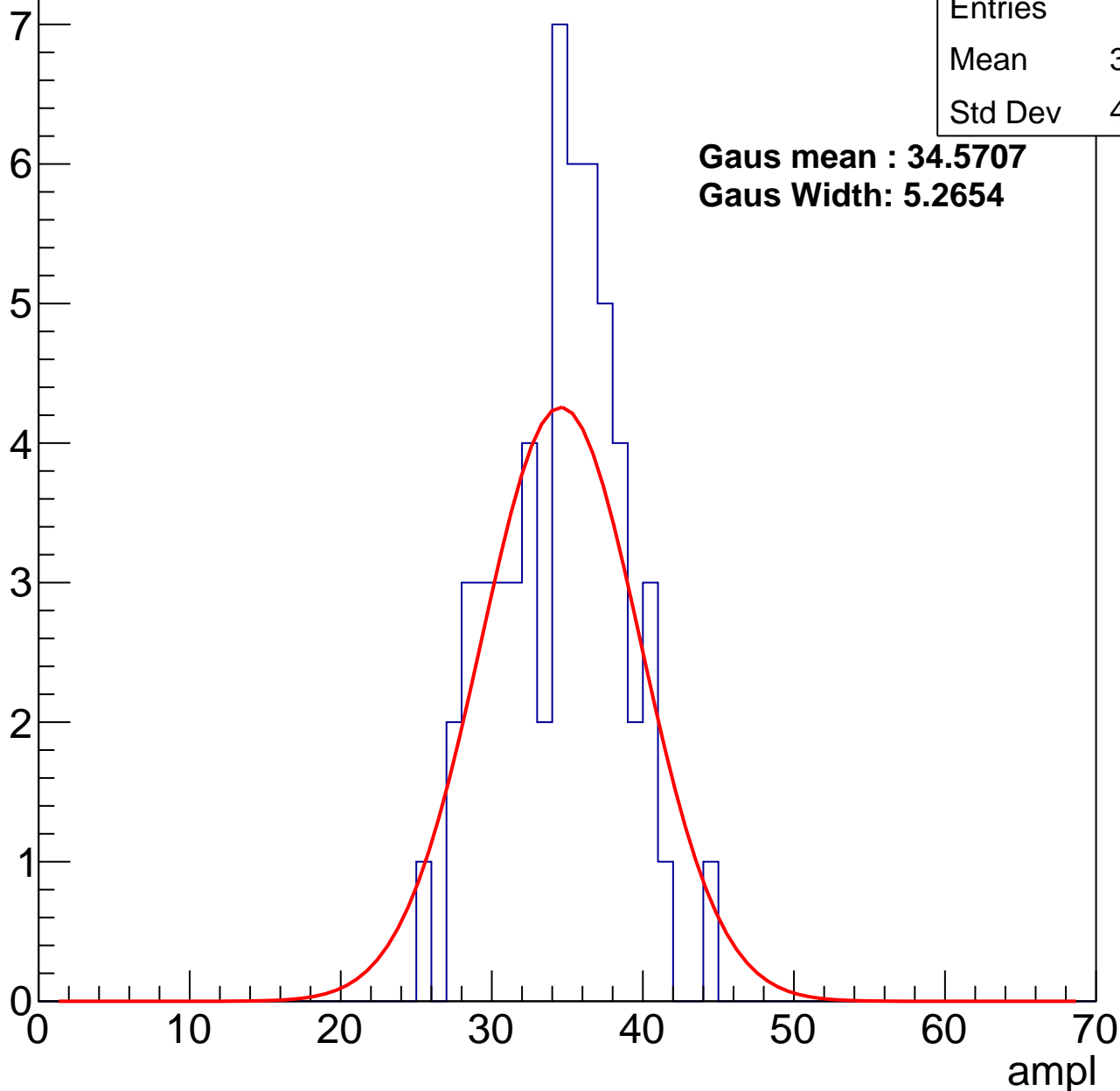
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	34.12
Std Dev	4.009

**Gaus mean : 34.5707**

**Gaus Width: 5.2654**



# B1L103S, U26-ch78, adc2

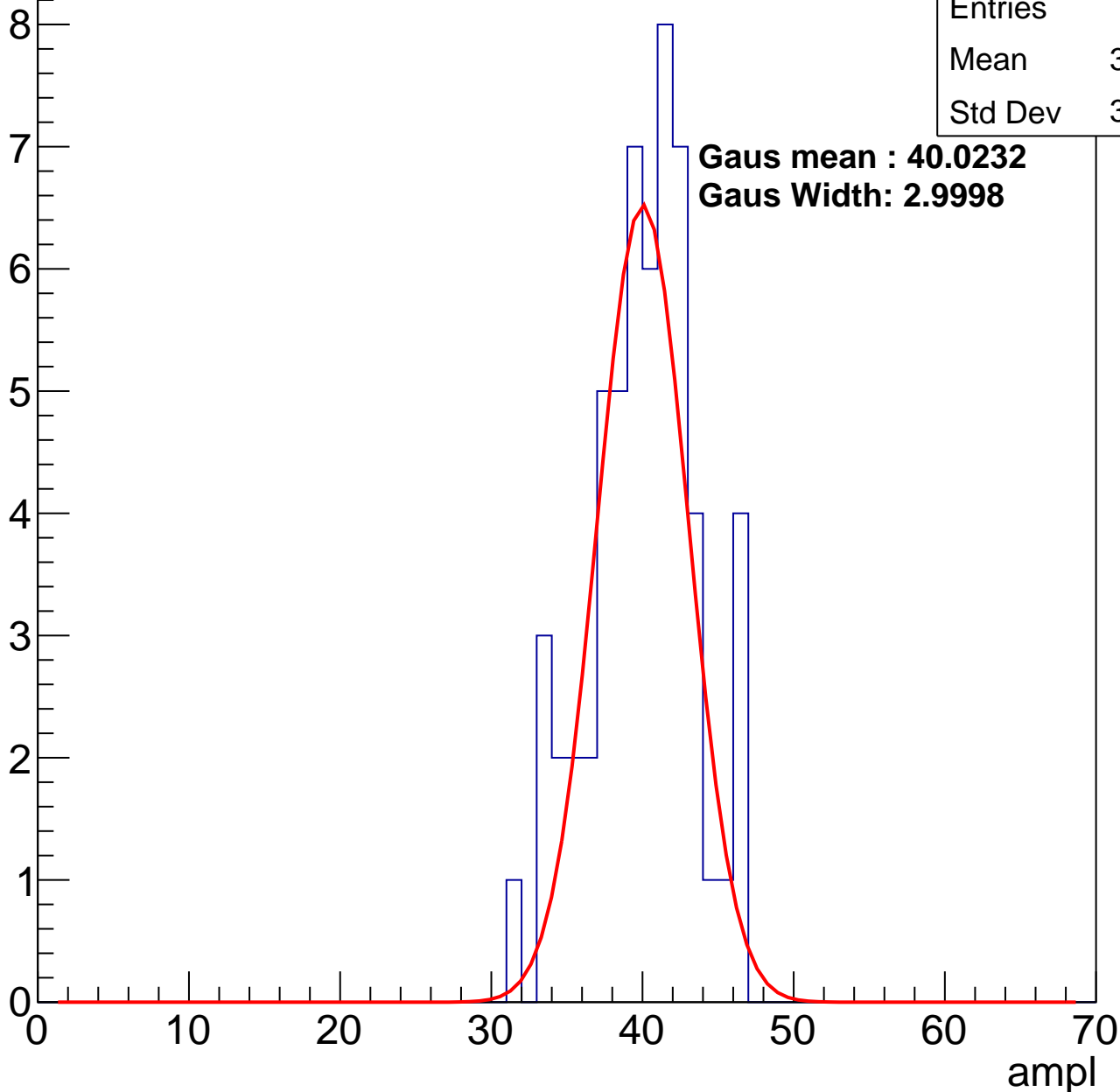
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	39.57
Std Dev	3.475

**Gaus mean : 40.0232**

**Gaus Width: 2.9998**

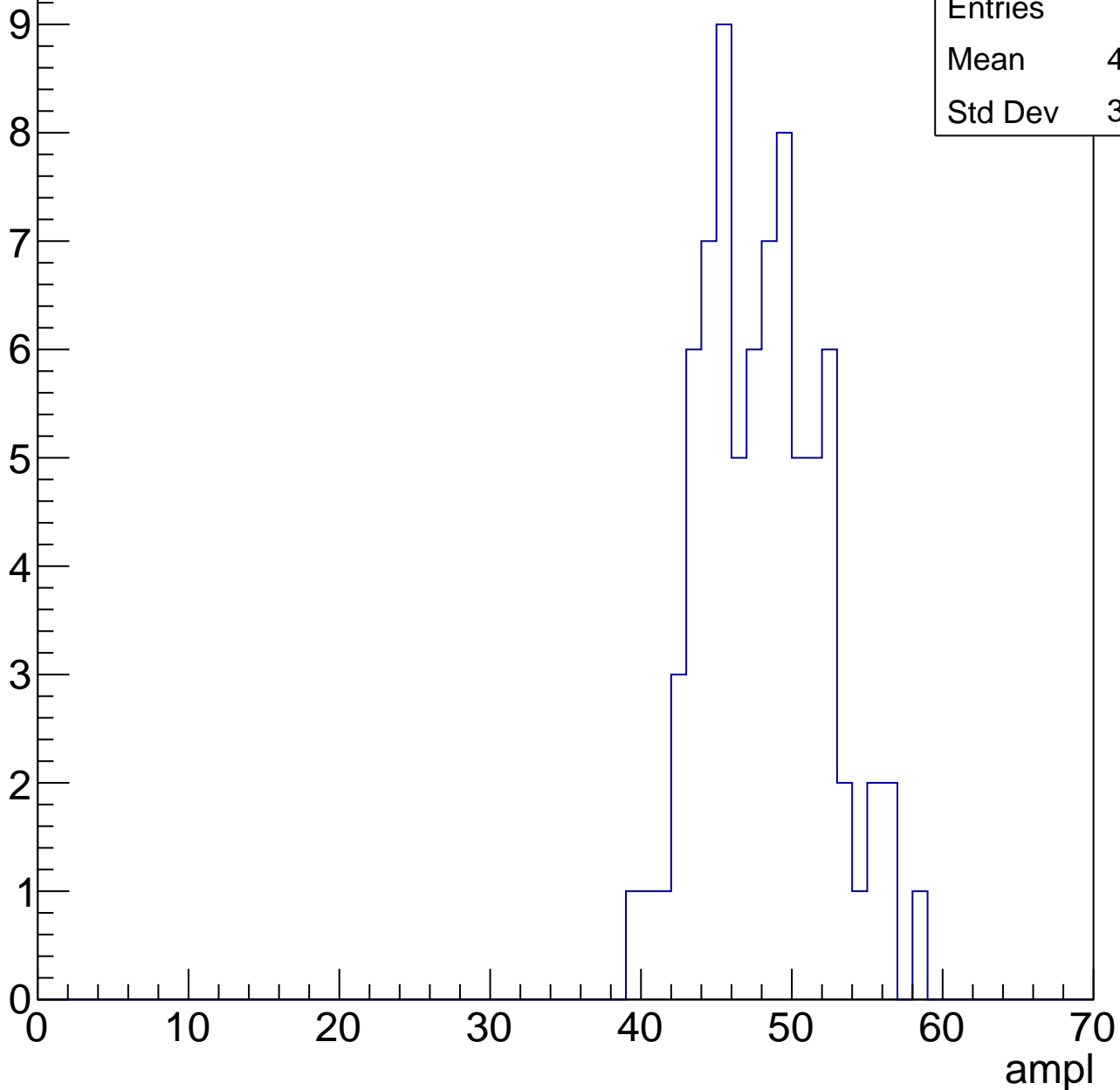


# B1L103S, U26-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	47.62
Std Dev	3.988

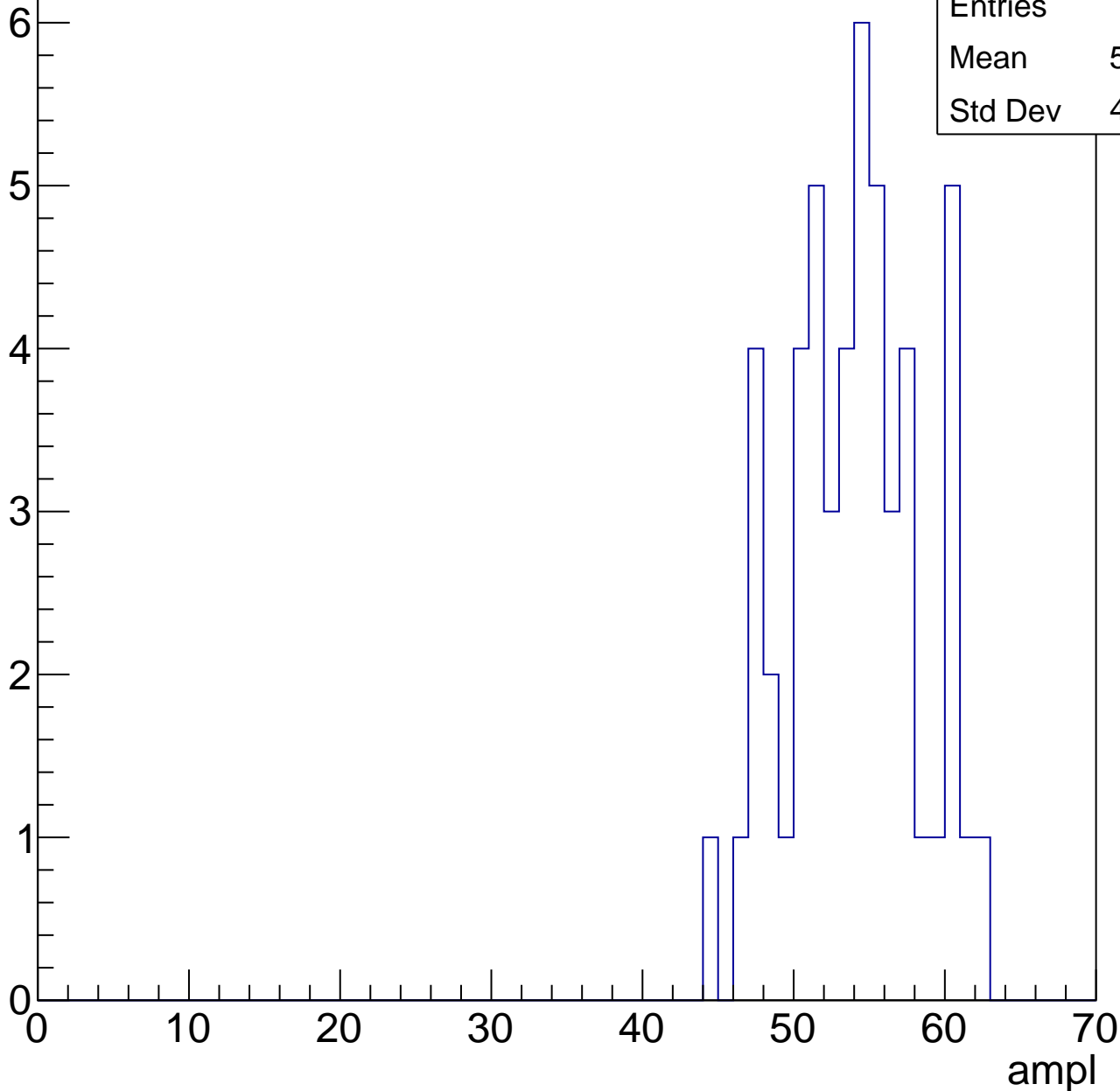


# B1L103S, U26-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	53.48
Std Dev	4.285

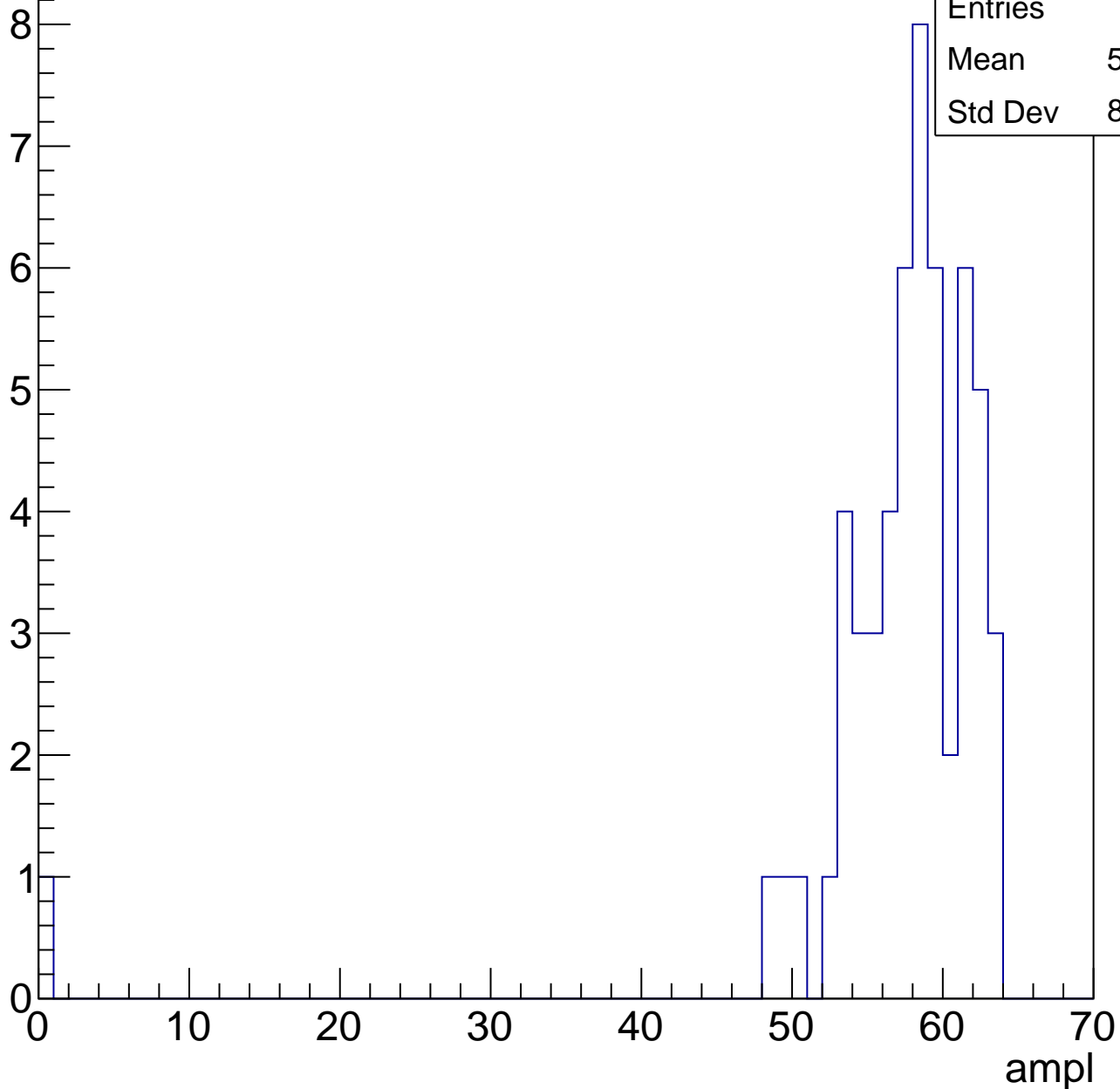


# B1L103S, U26-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	56.49
Std Dev	8.464

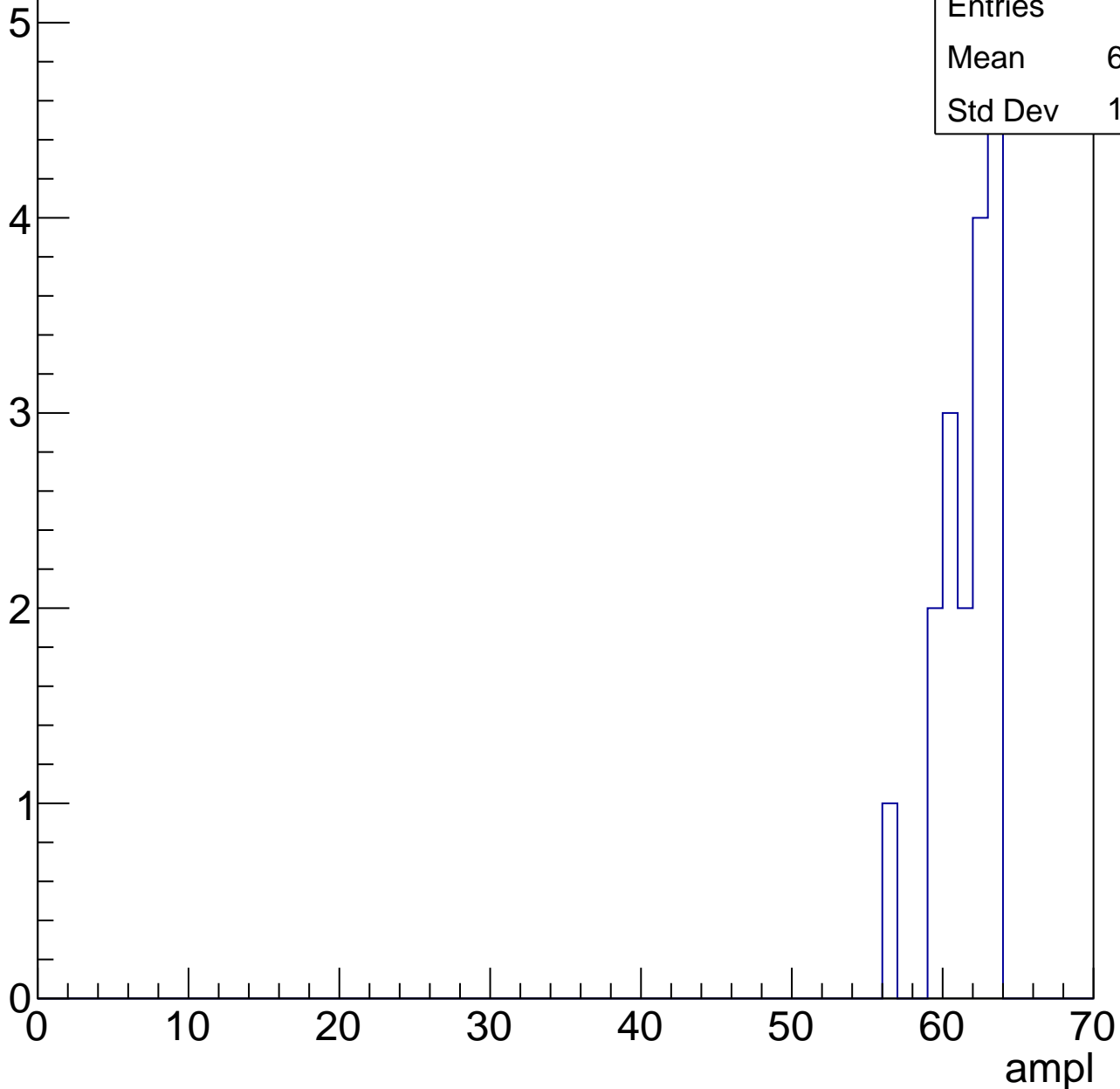


# B1L103S, U26-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	17
Mean	61.12
Std Dev	1.875





# B1L103S, U26-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

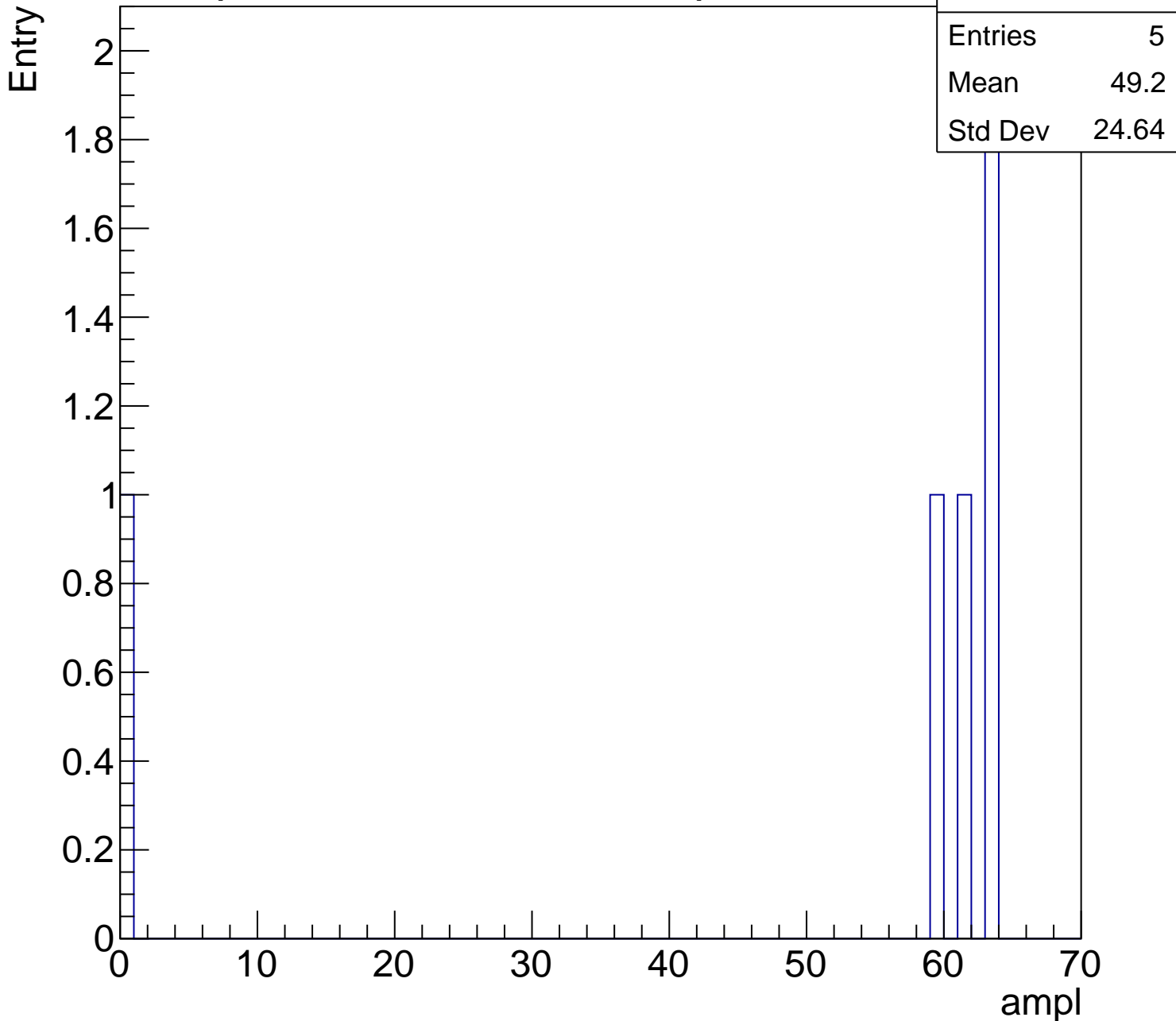
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	49.2
Std Dev	24.64

0 10 20 30 40 50 60 70

ampl



# B1L103S, U26-ch79, adc0

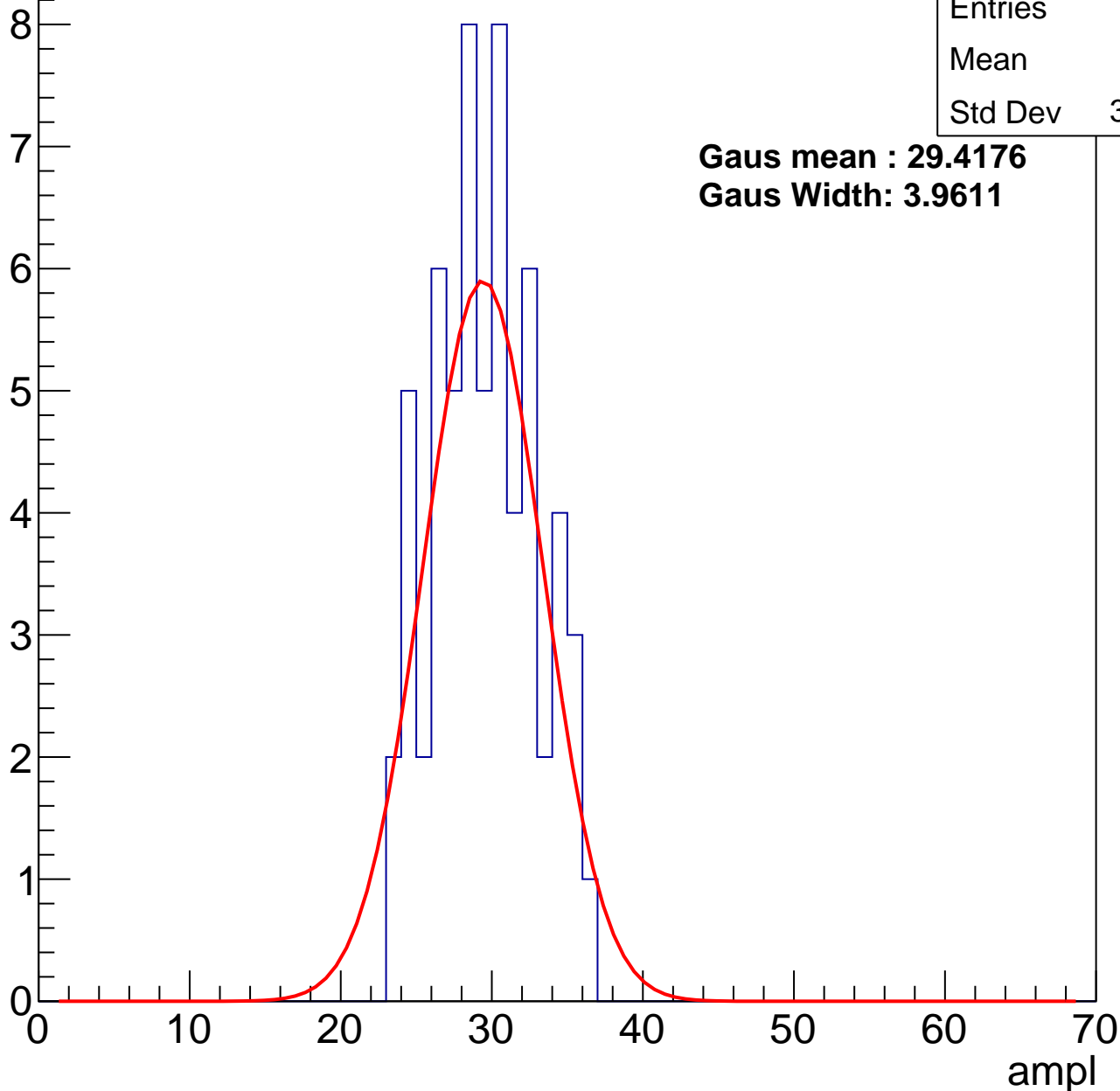
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	29.1
Std Dev	3.332

**Gaus mean : 29.4176**

**Gaus Width: 3.9611**



# B1L103S, U26-ch79, adc1

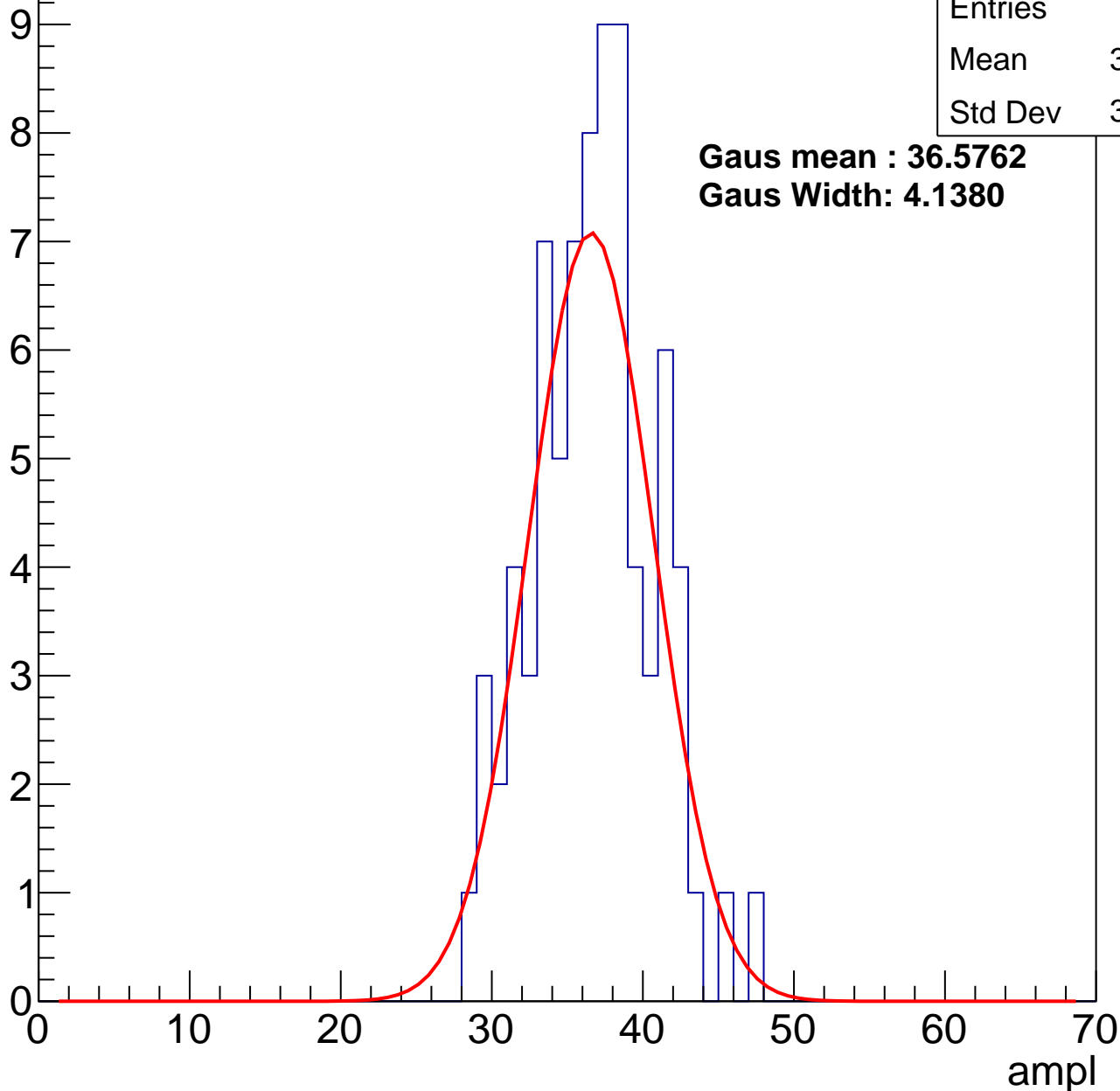
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	36.27
Std Dev	3.905

**Gaus mean : 36.5762**

**Gaus Width: 4.1380**



# B1L103S, U26-ch79, adc2

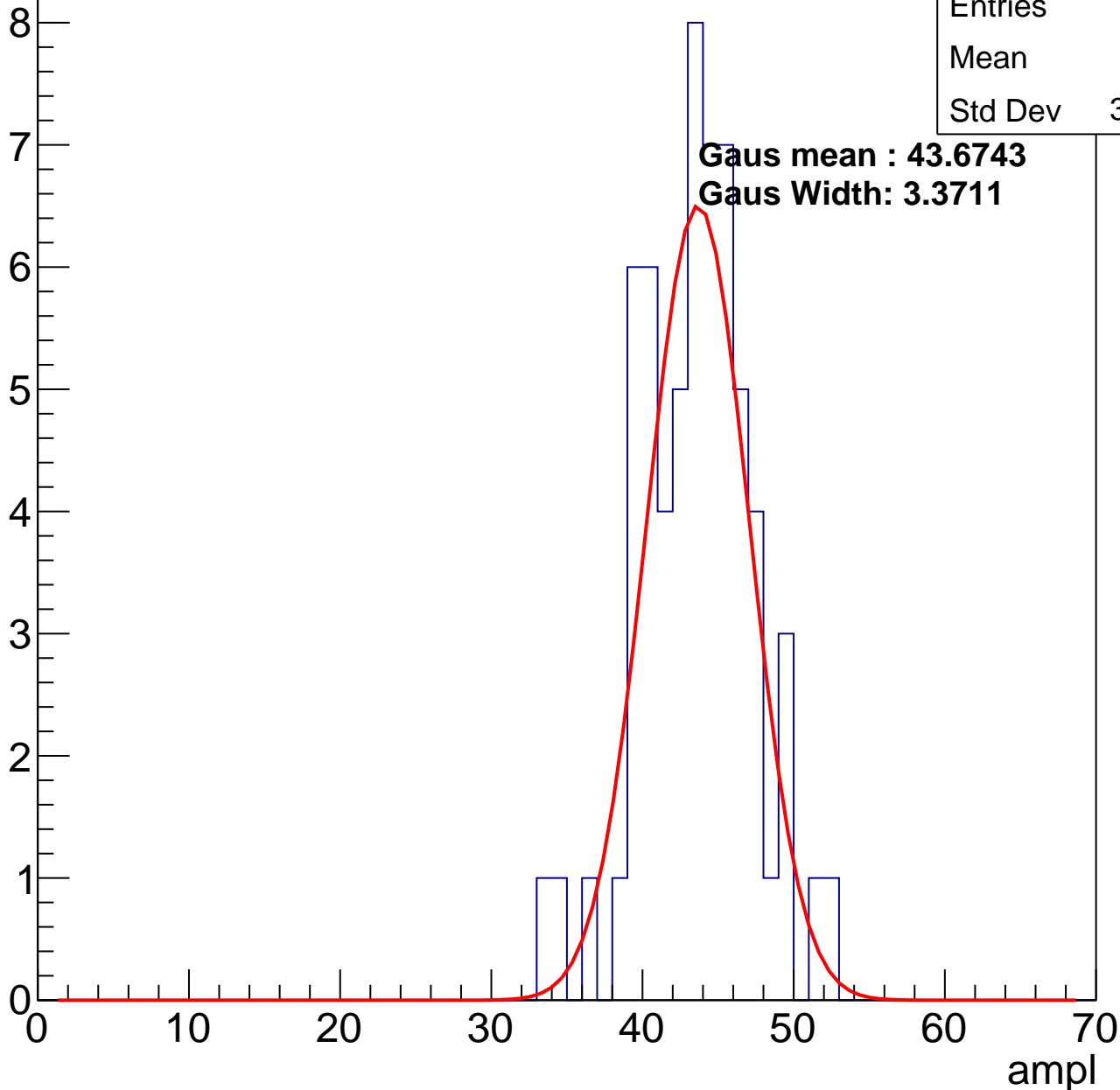
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	43.1
Std Dev	3.697

**Gaus mean : 43.6743**

**Gaus Width: 3.3711**

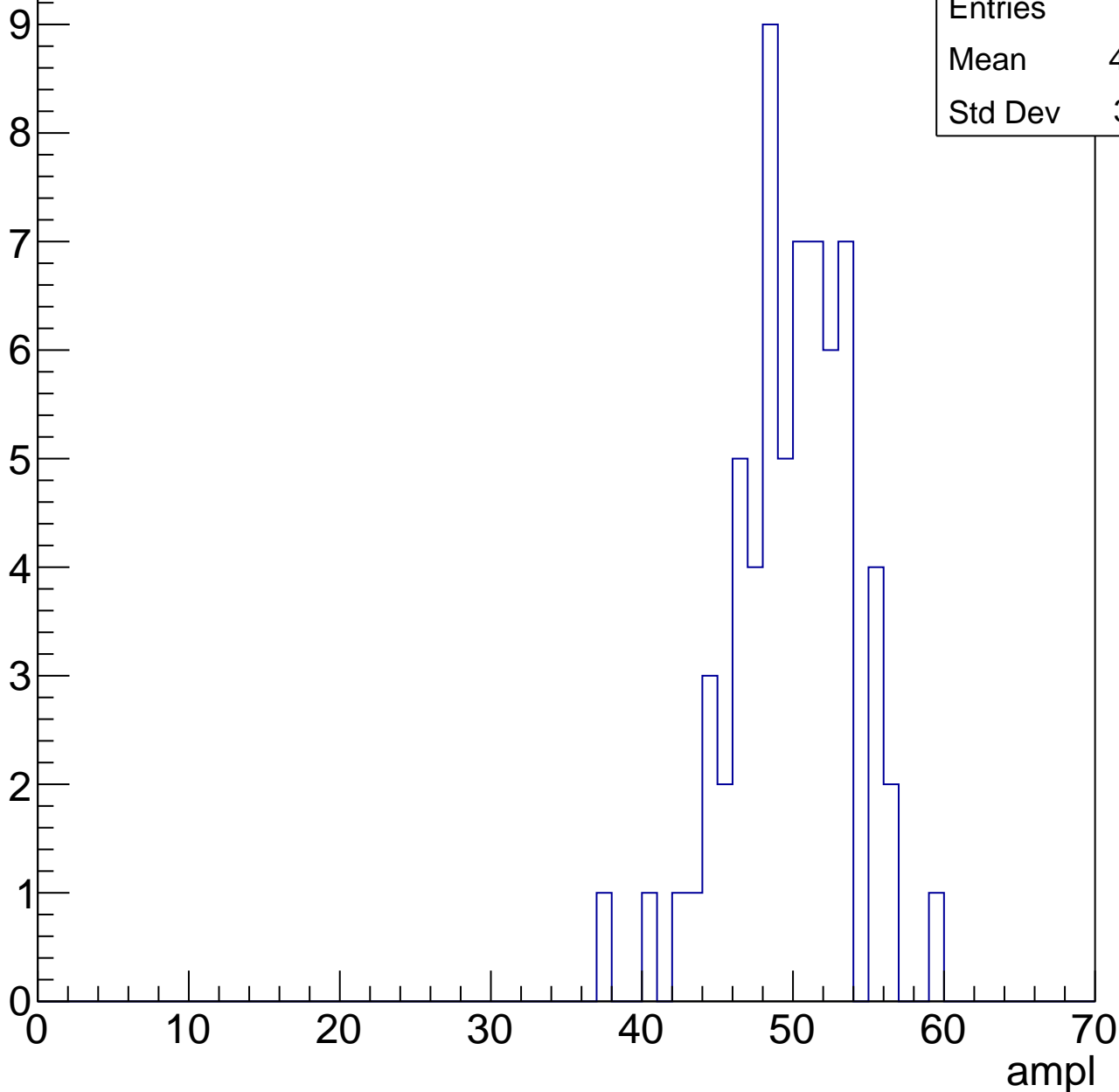


# B1L103S, U26-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	49.39
Std Dev	3.931

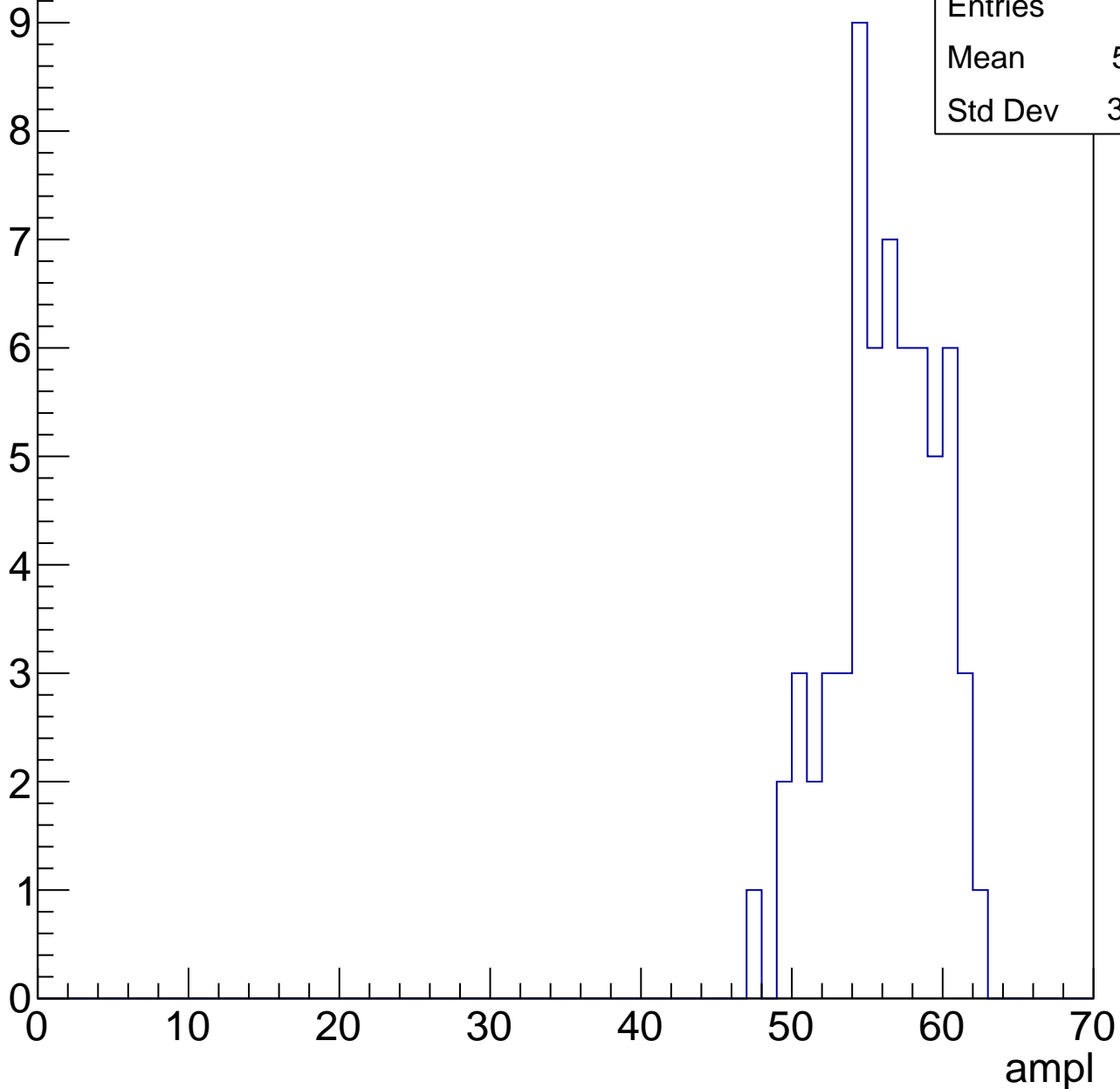


# B1L103S, U26-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	55.71
Std Dev	3.406

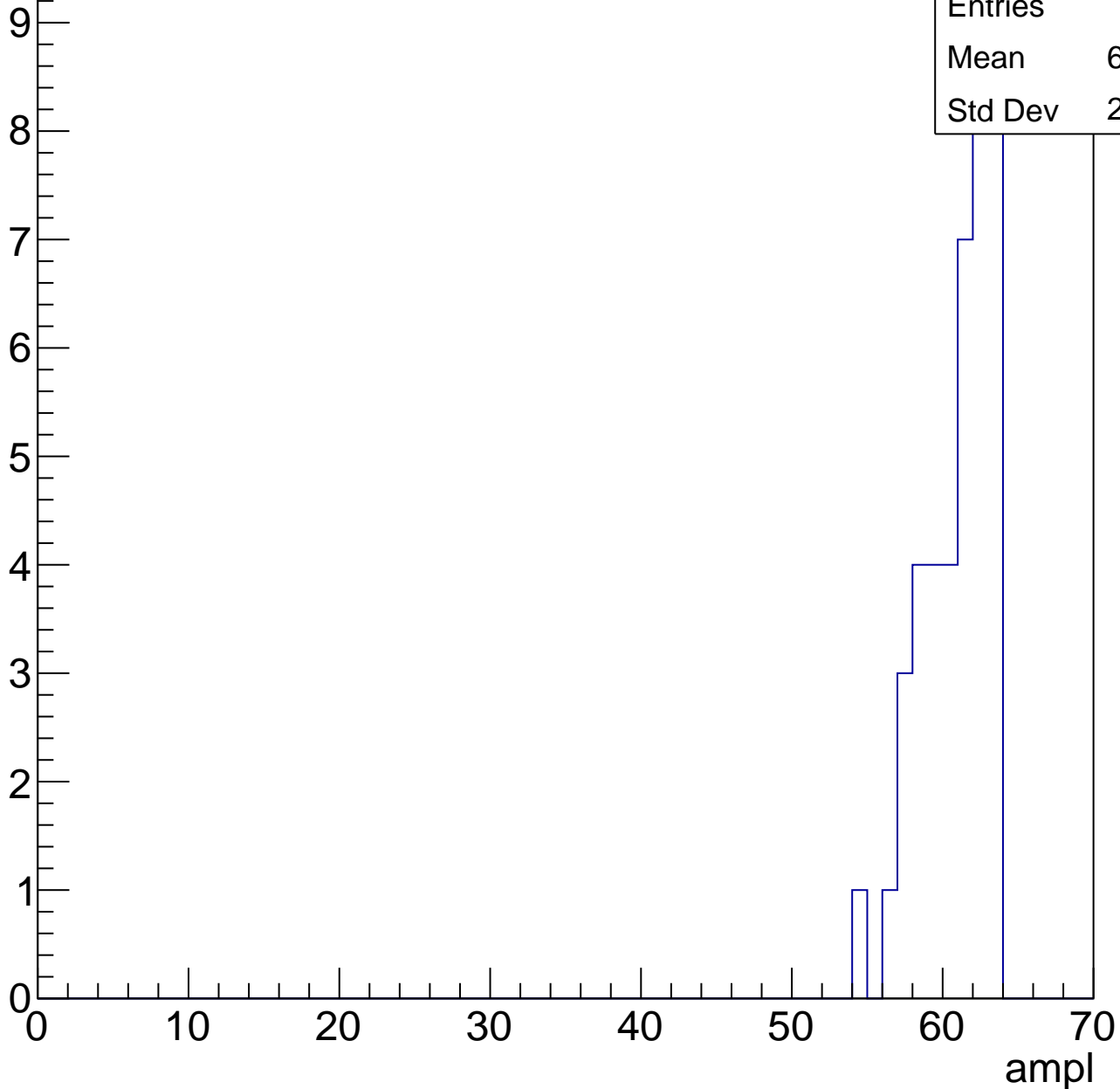


# B1L103S, U26-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

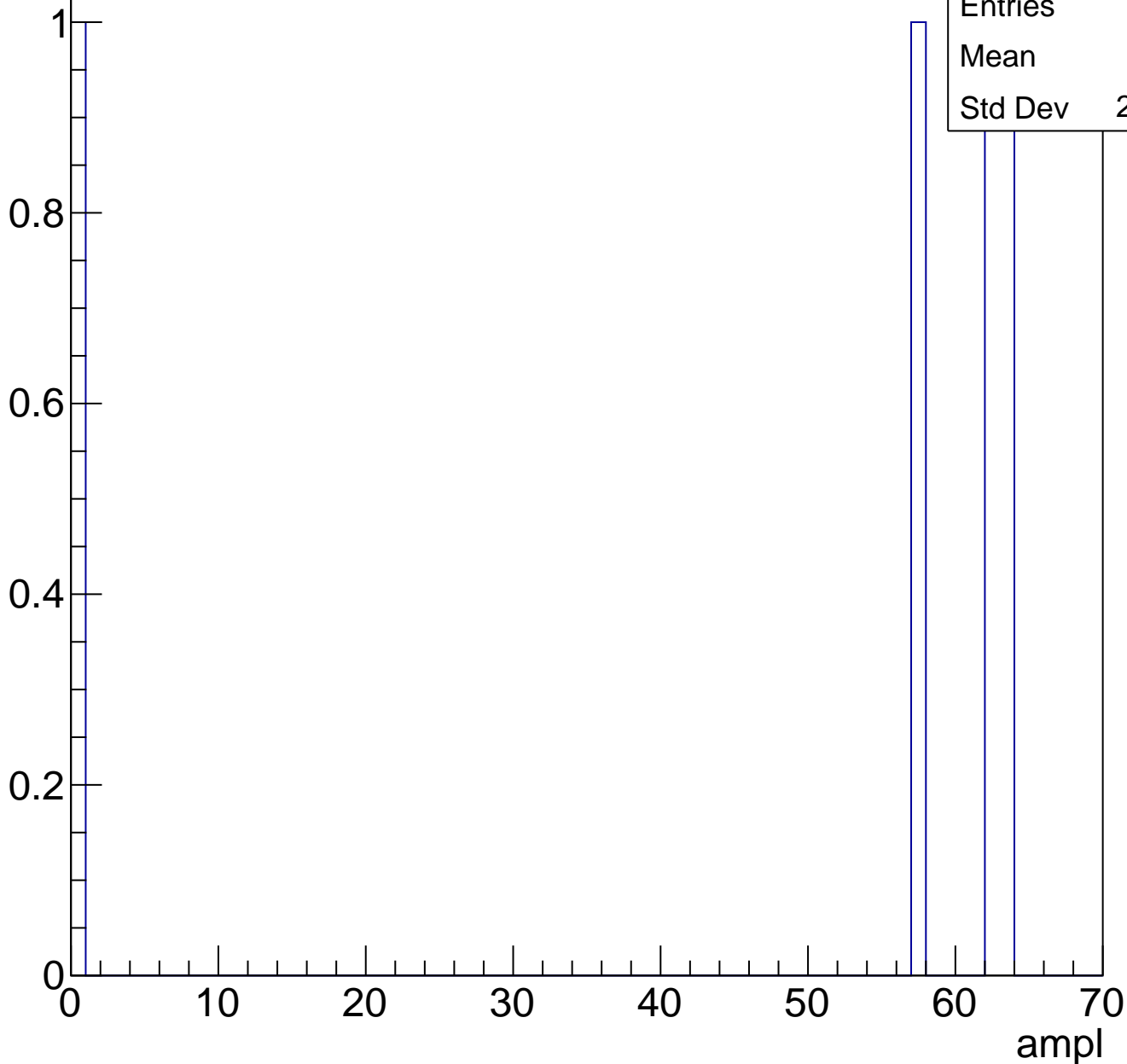
Entries	41
Mean	60.46
Std Dev	2.264



# B1L103S, U26-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch80, adc0

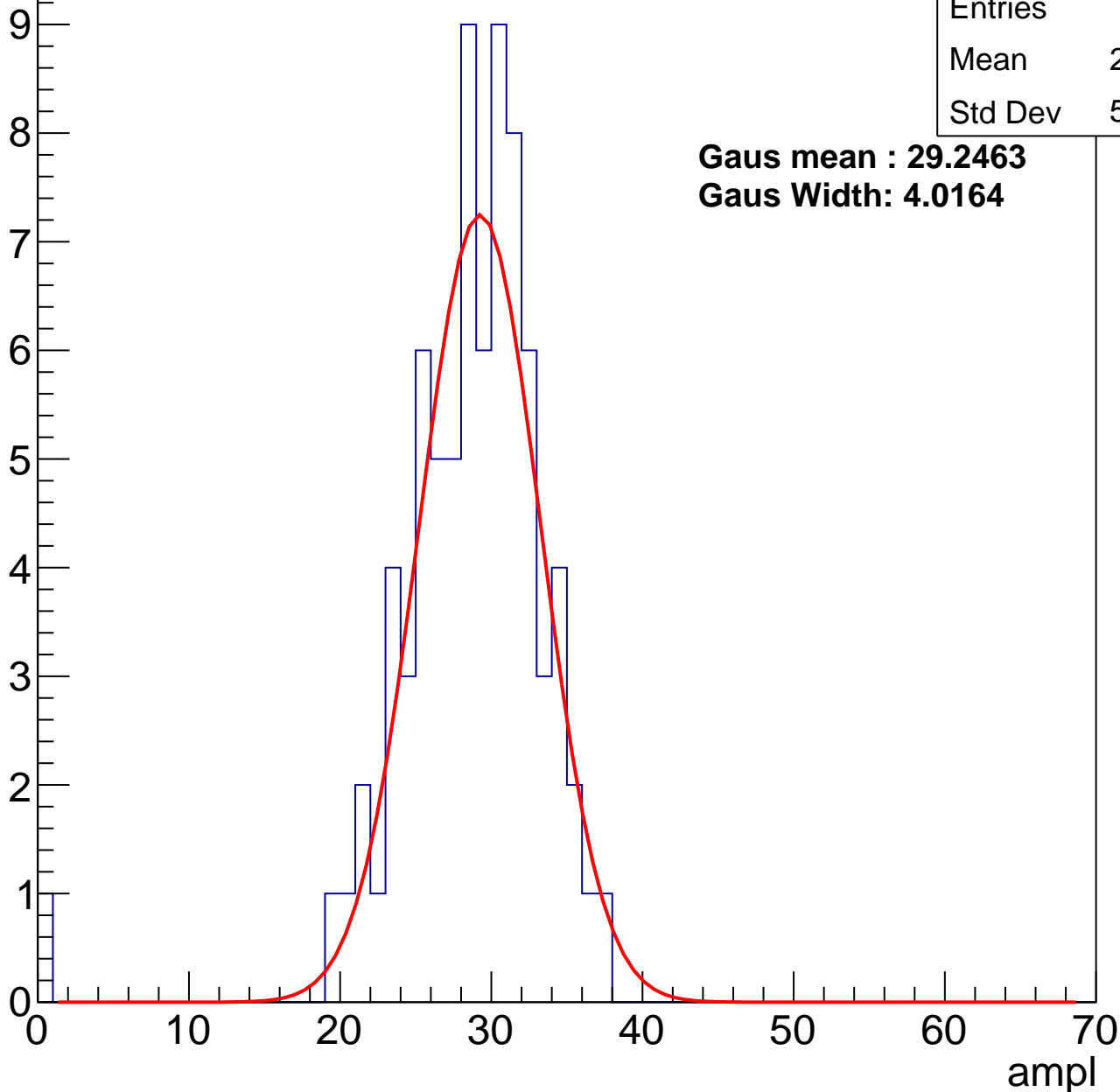
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	28.15
Std Dev	5.013

**Gaus mean : 29.2463**

**Gaus Width: 4.0164**



# B1L103S, U26-ch80, adc1

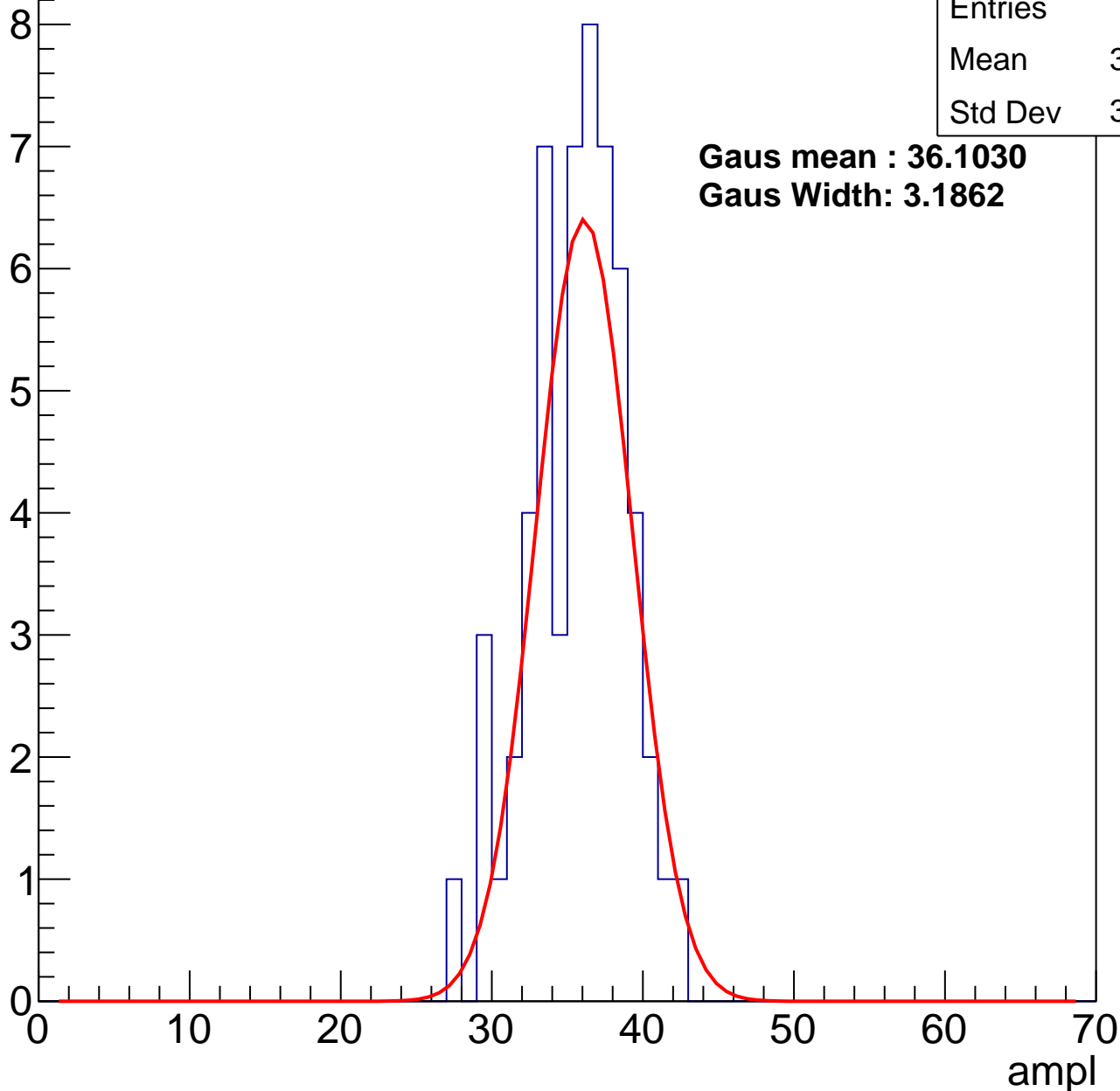
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	35.19
Std Dev	3.198

**Gaus mean : 36.1030**

**Gaus Width: 3.1862**



# B1L103S, U26-ch80, adc2

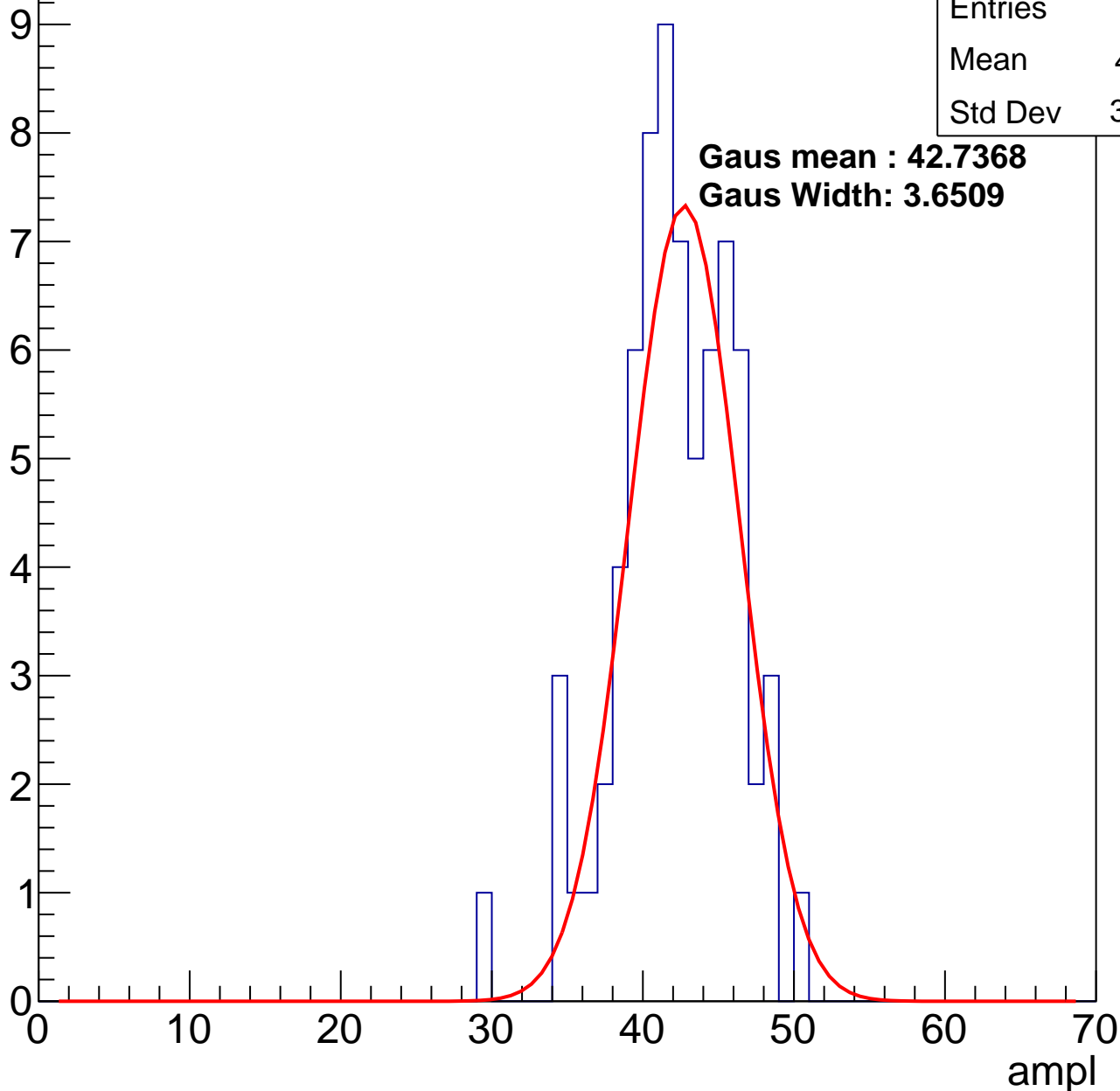
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	41.71
Std Dev	3.835

**Gaus mean : 42.7368**

**Gaus Width: 3.6509**

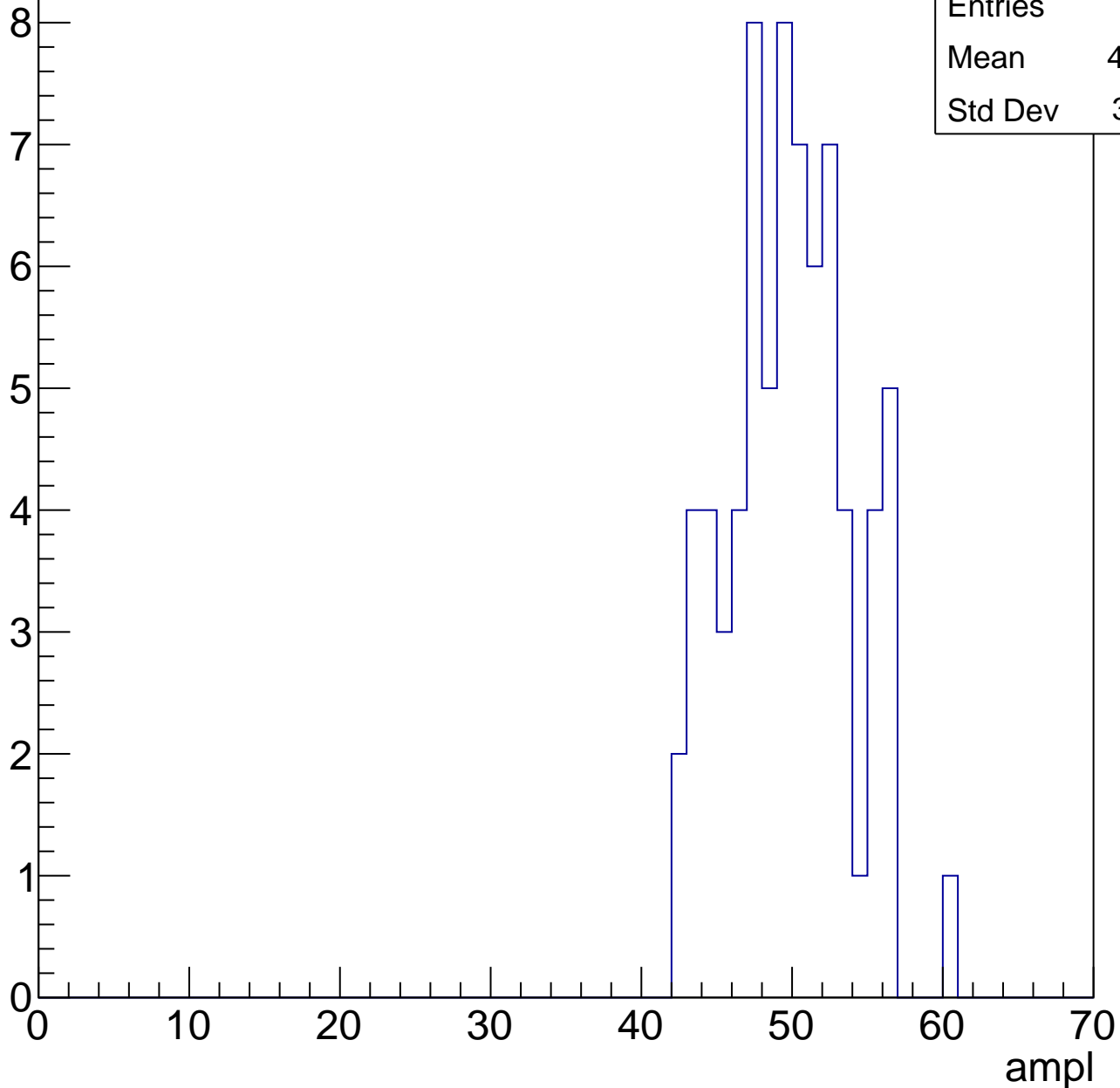


# B1L103S, U26-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	49.38
Std Dev	3.961

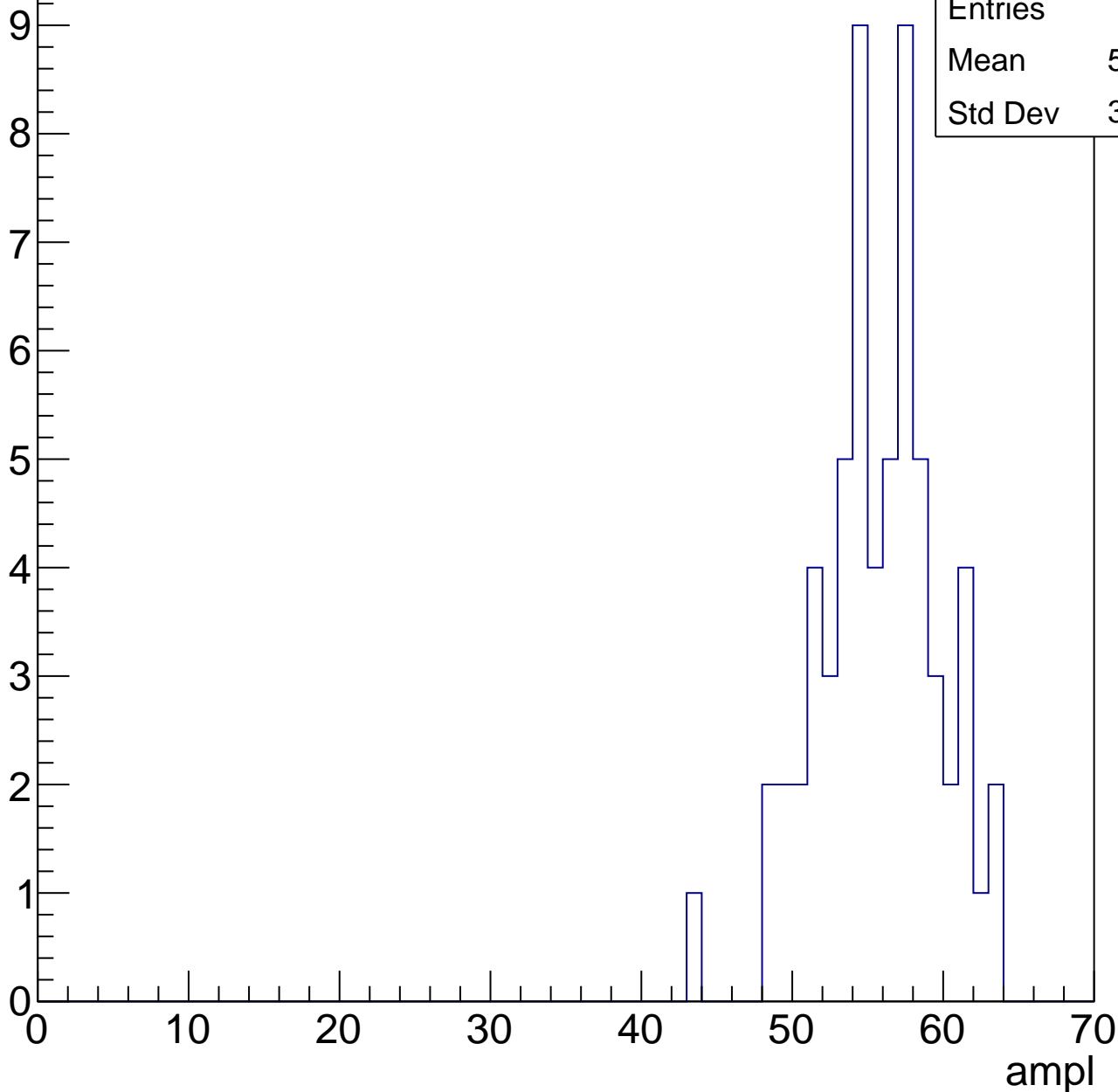


# B1L103S, U26-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	55.24
Std Dev	3.955

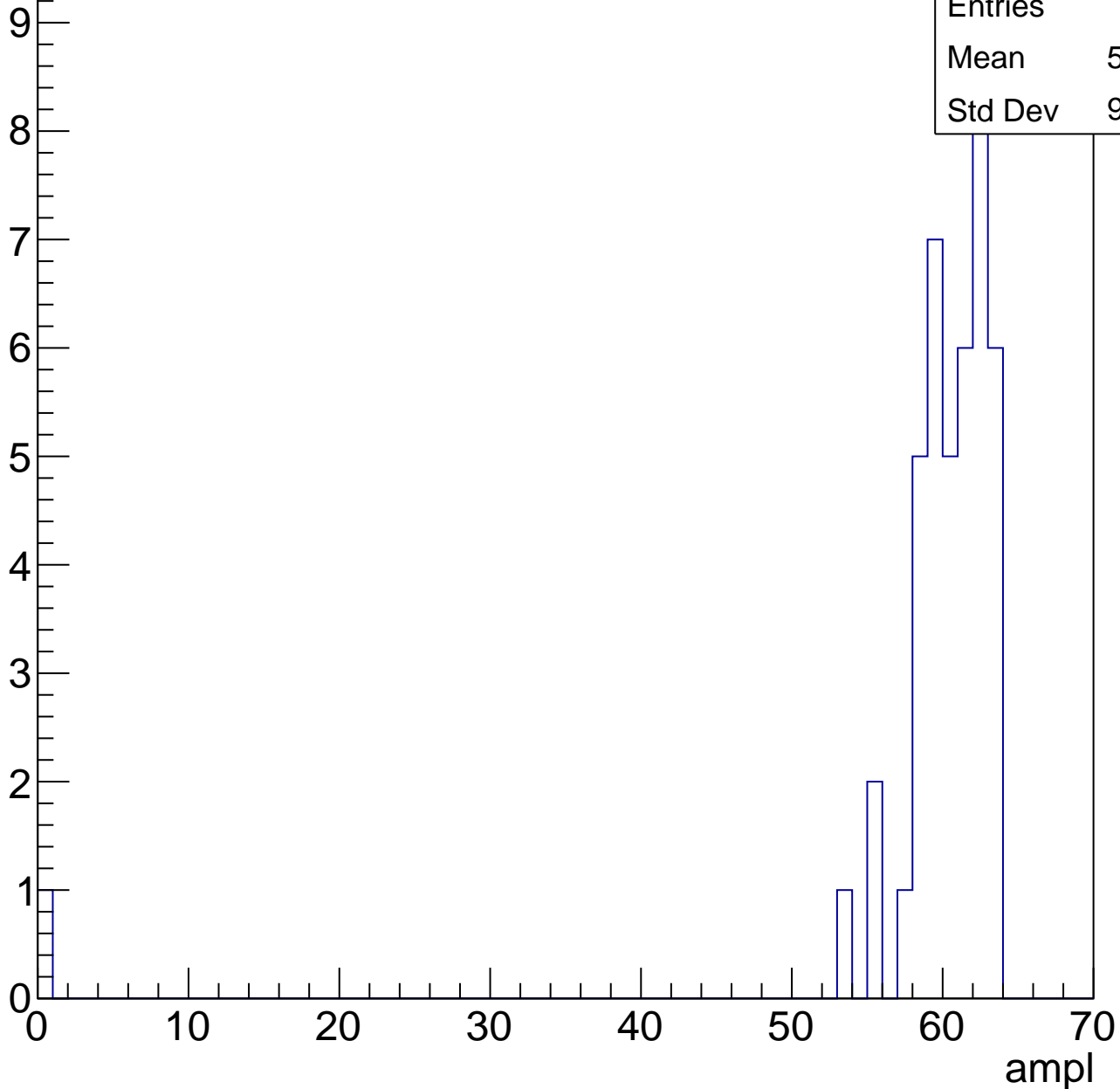


# B1L103S, U26-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	43
Mean	58.72
Std Dev	9.352



# B1L103S, U26-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	61.5
Std Dev	1.5

0 10 20 30 40 50 60 70

ampl



# B1L103S, U26-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U26-ch81, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	87
Mean	29.36
Std Dev	3.898

**Gaus mean : 30.1245**

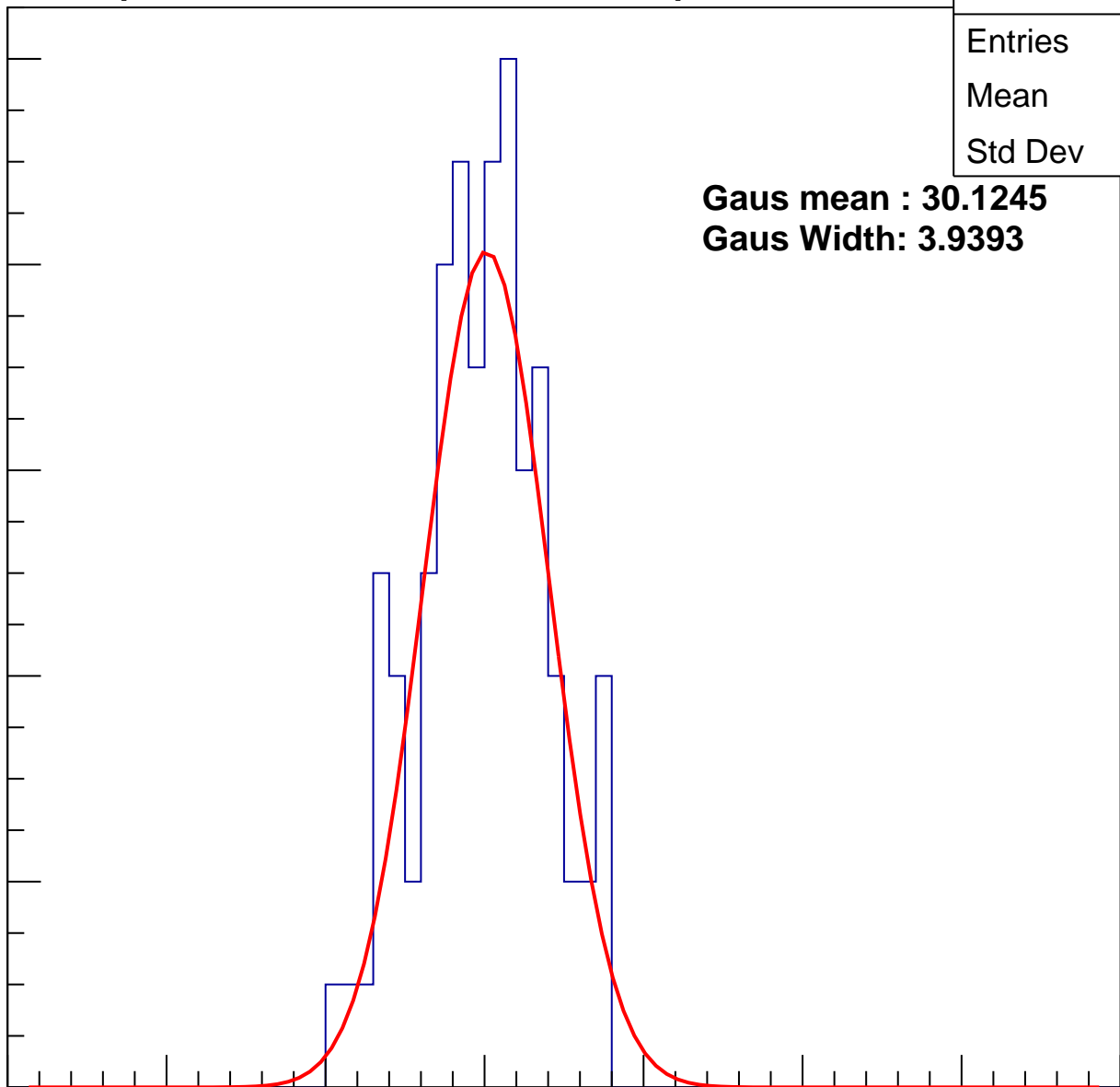
**Gaus Width: 3.9393**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch81, adc1

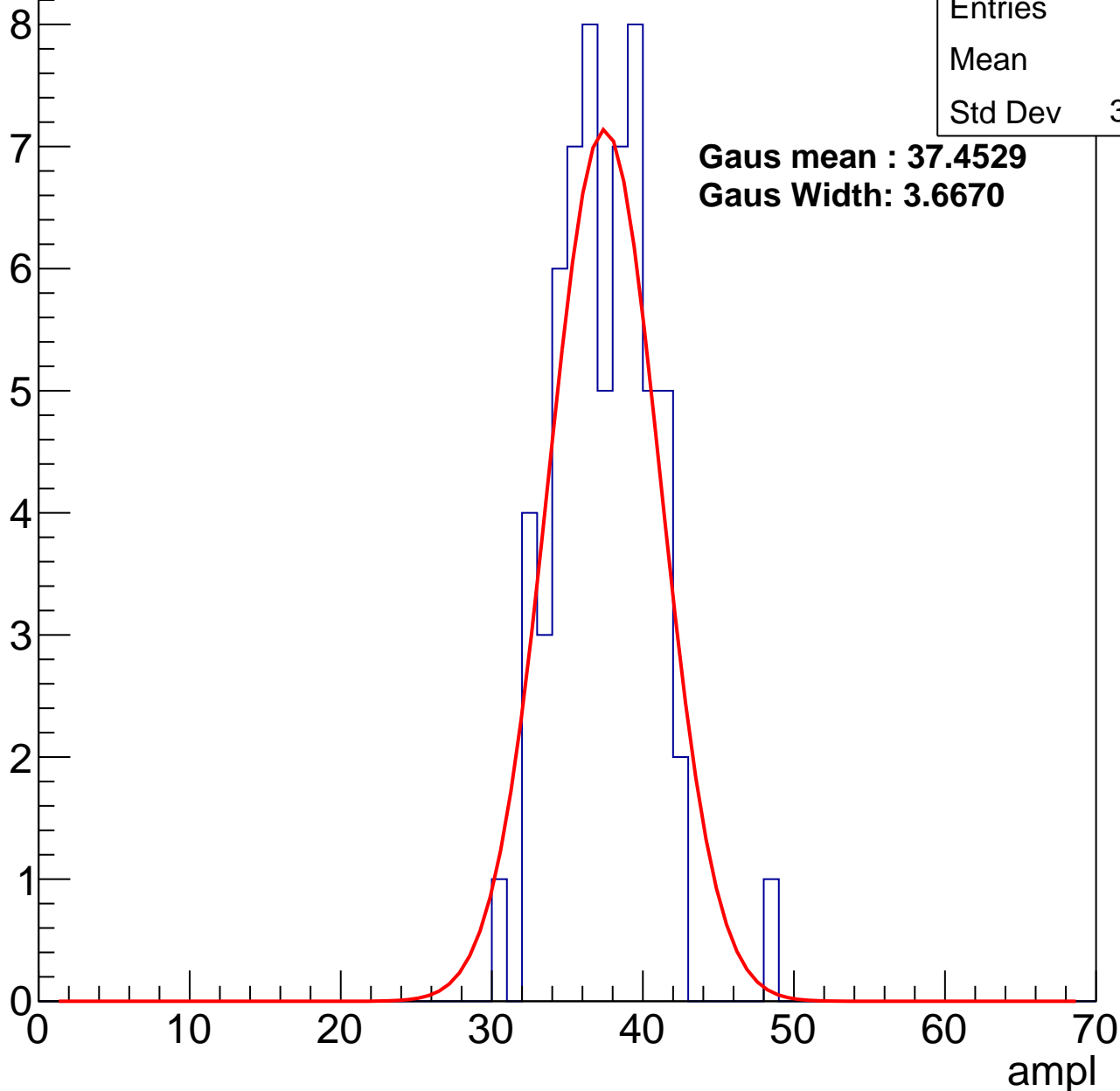
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	37
Std Dev	3.167

**Gaus mean : 37.4529**

**Gaus Width: 3.6670**



# B1L103S, U26-ch81, adc2

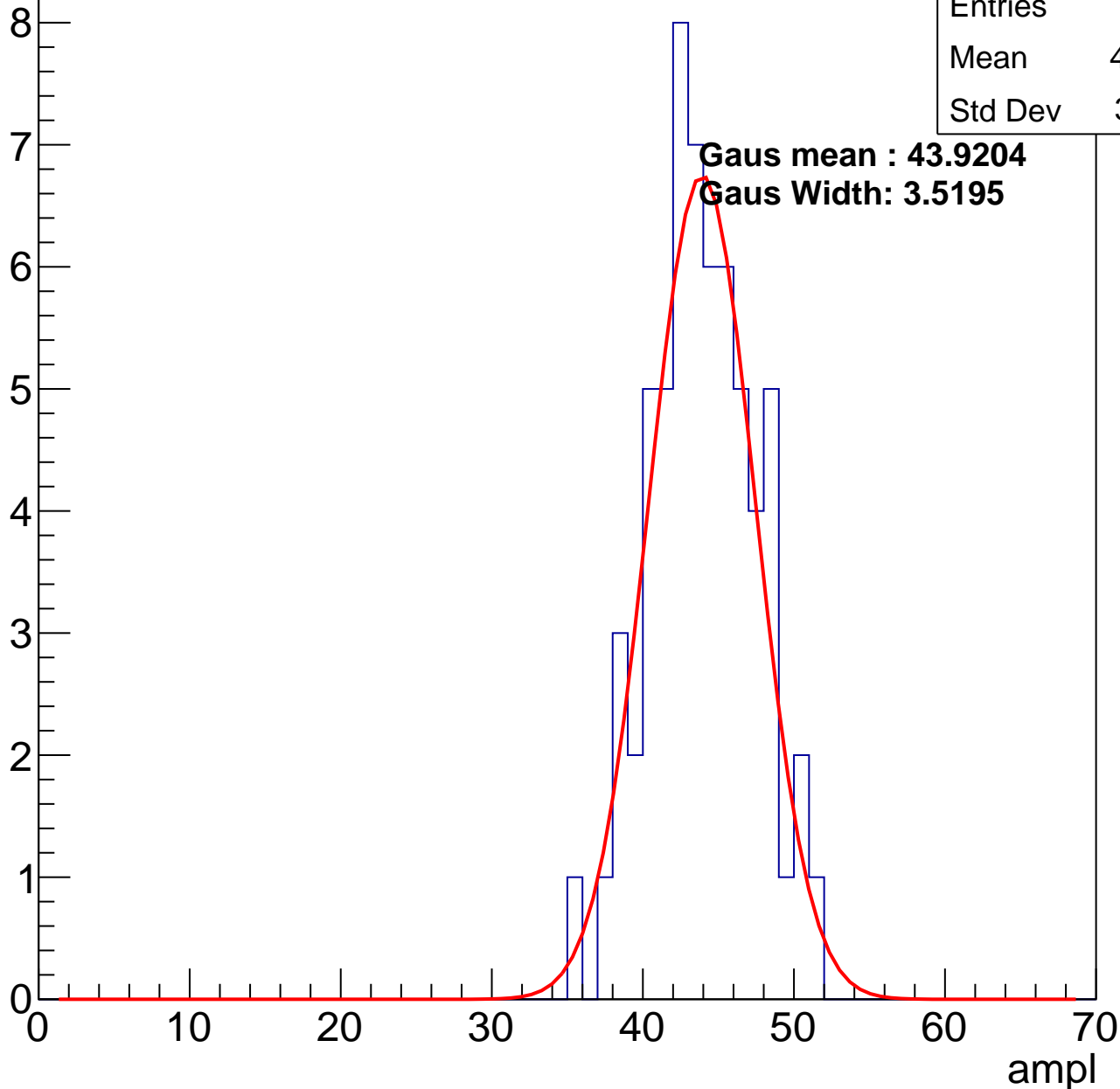
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	43.52
Std Dev	3.421

**Gaus mean : 43.9204**

**Gaus Width: 3.5195**

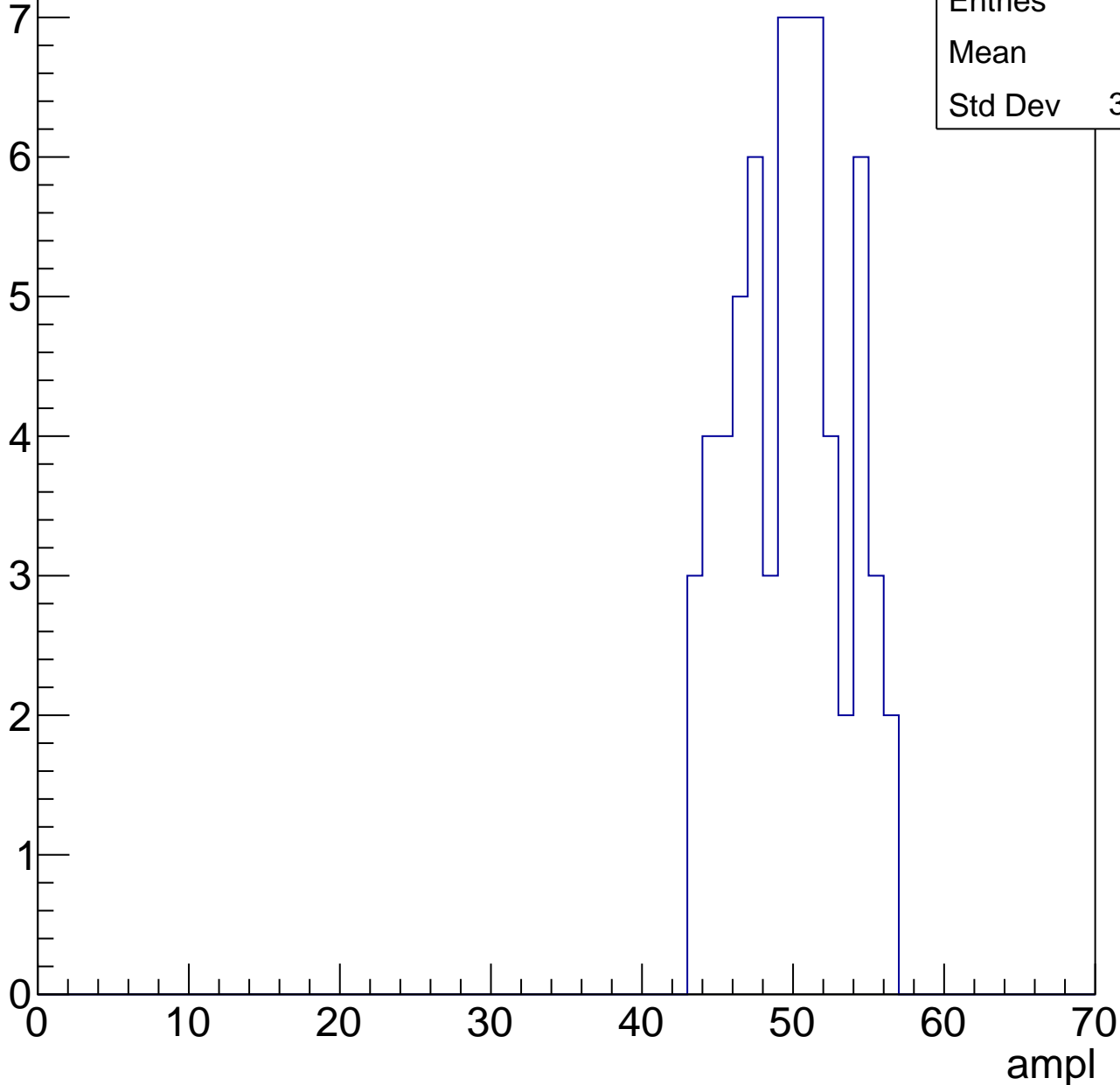


# B1L103S, U26-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	49.3
Std Dev	3.557

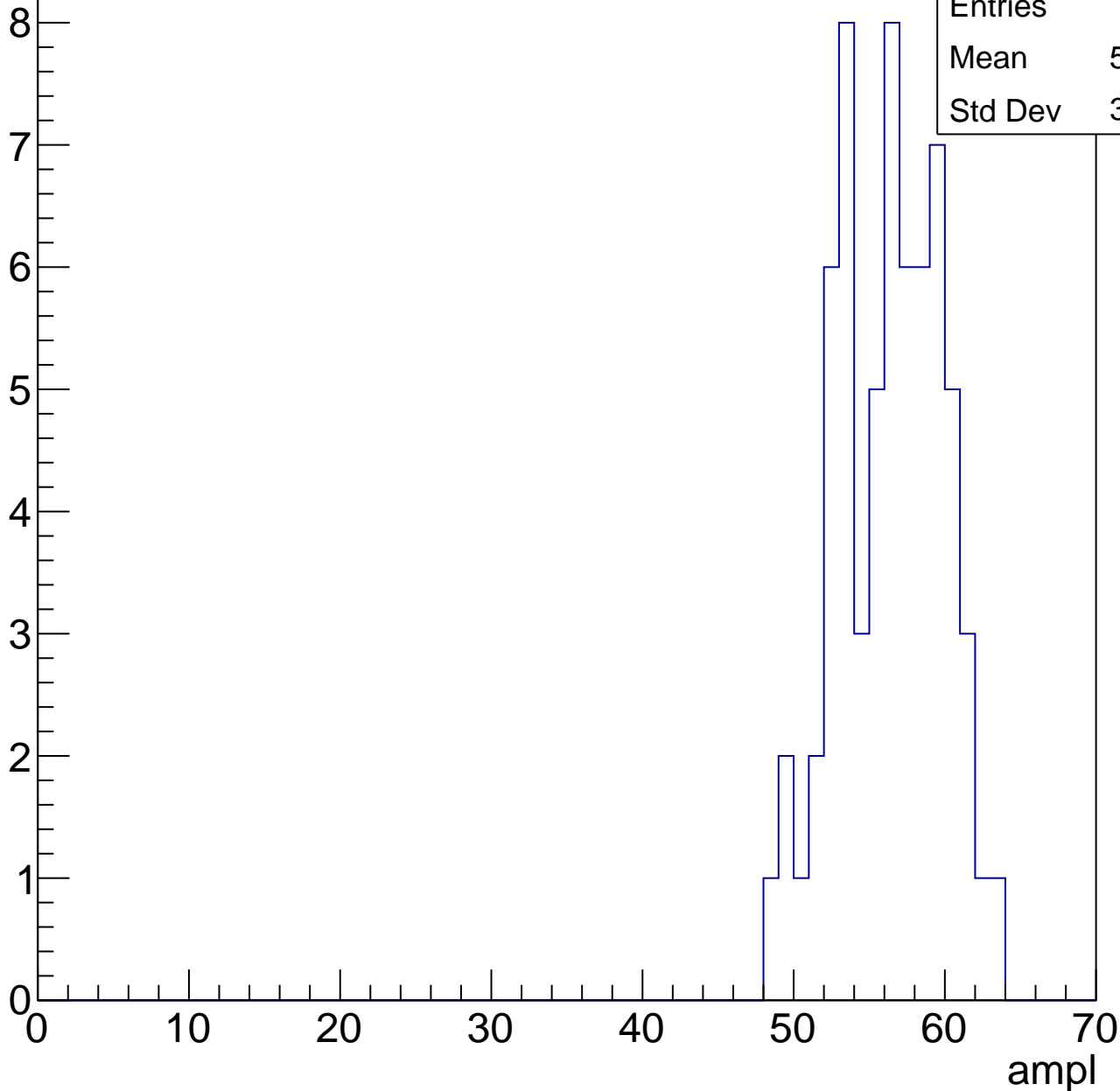


# B1L103S, U26-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	55.85
Std Dev	3.429

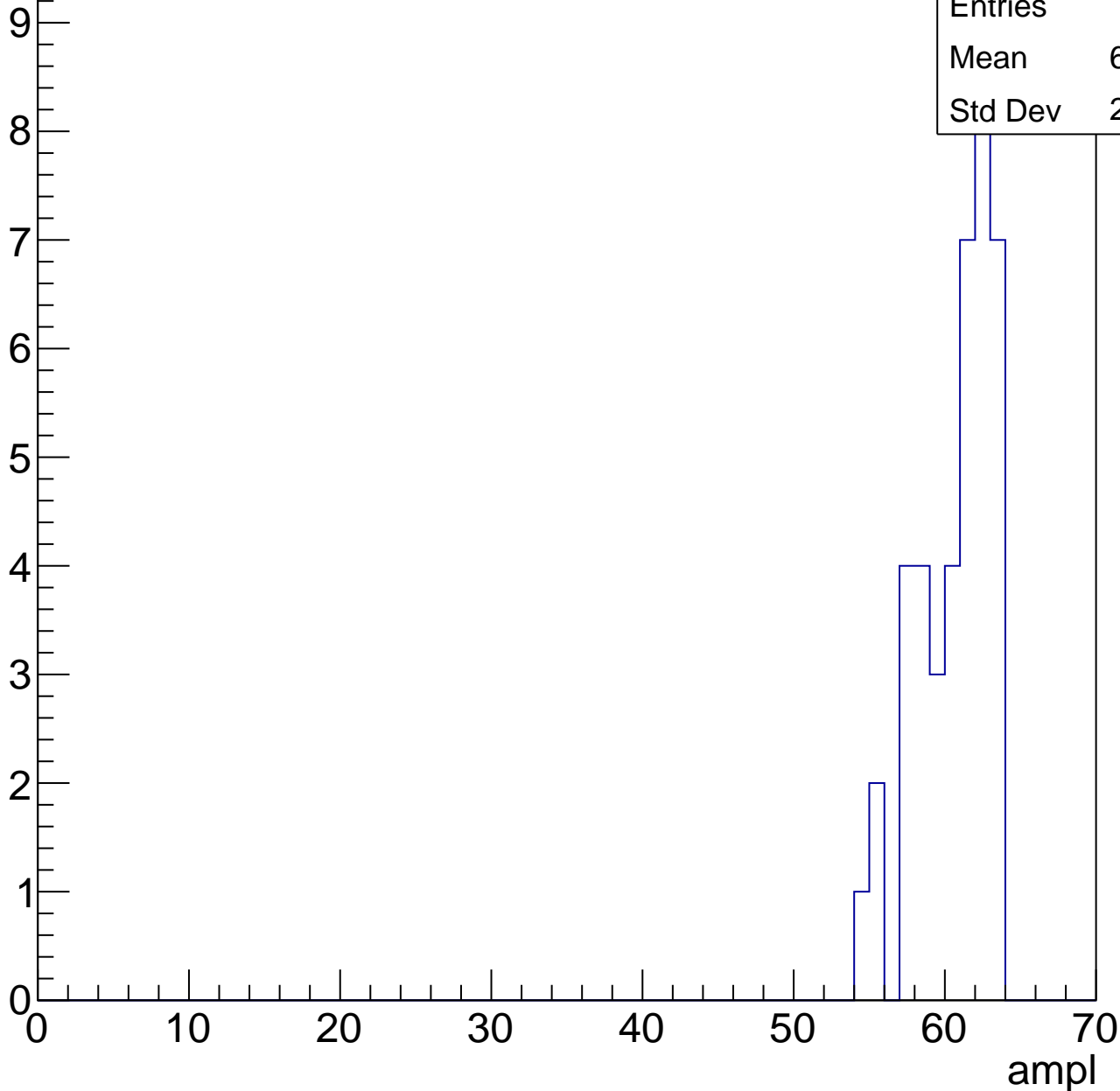


# B1L103S, U26-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

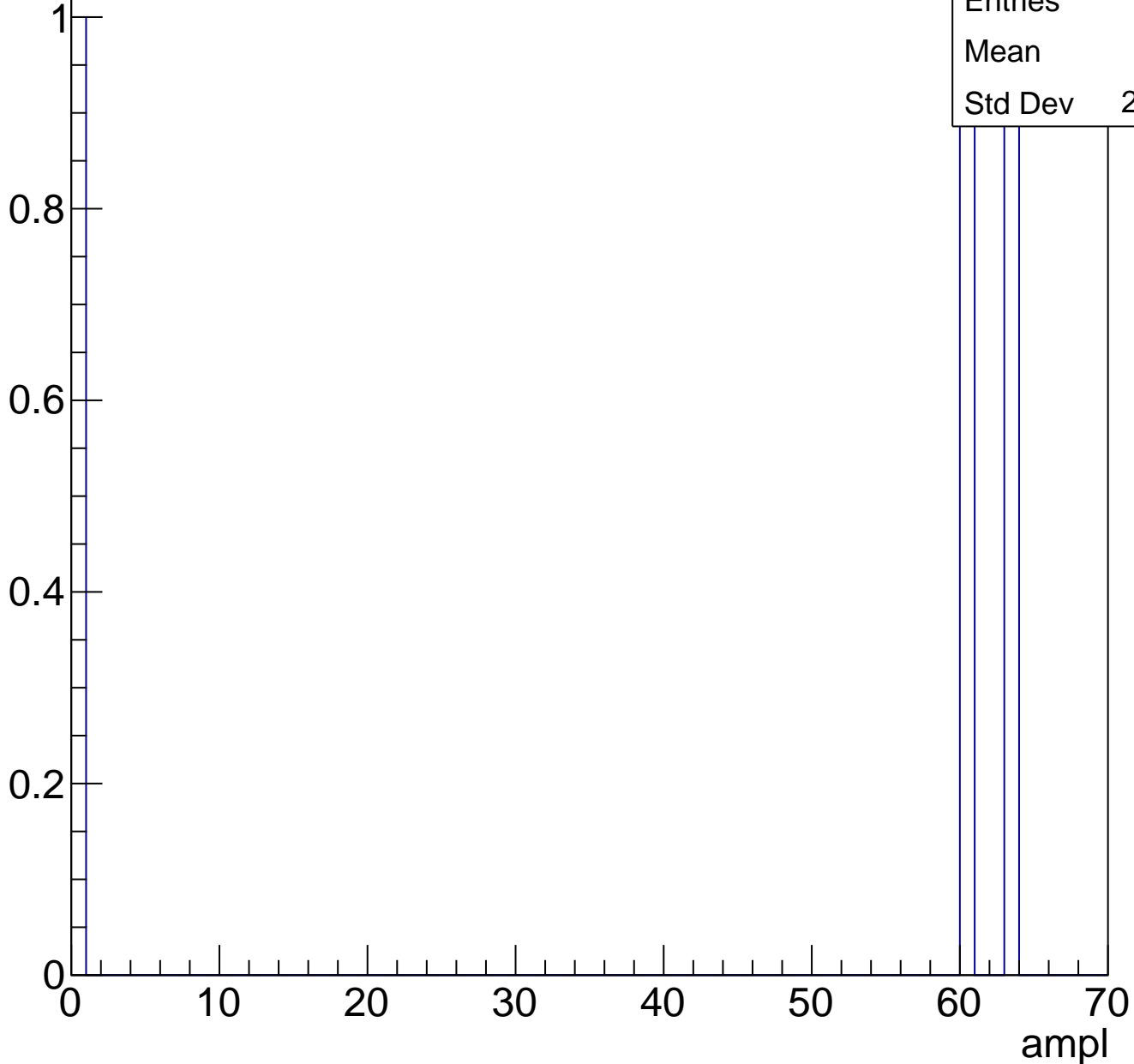
Entries	41
Mean	60.17
Std Dev	2.449



# B1L103S, U26-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

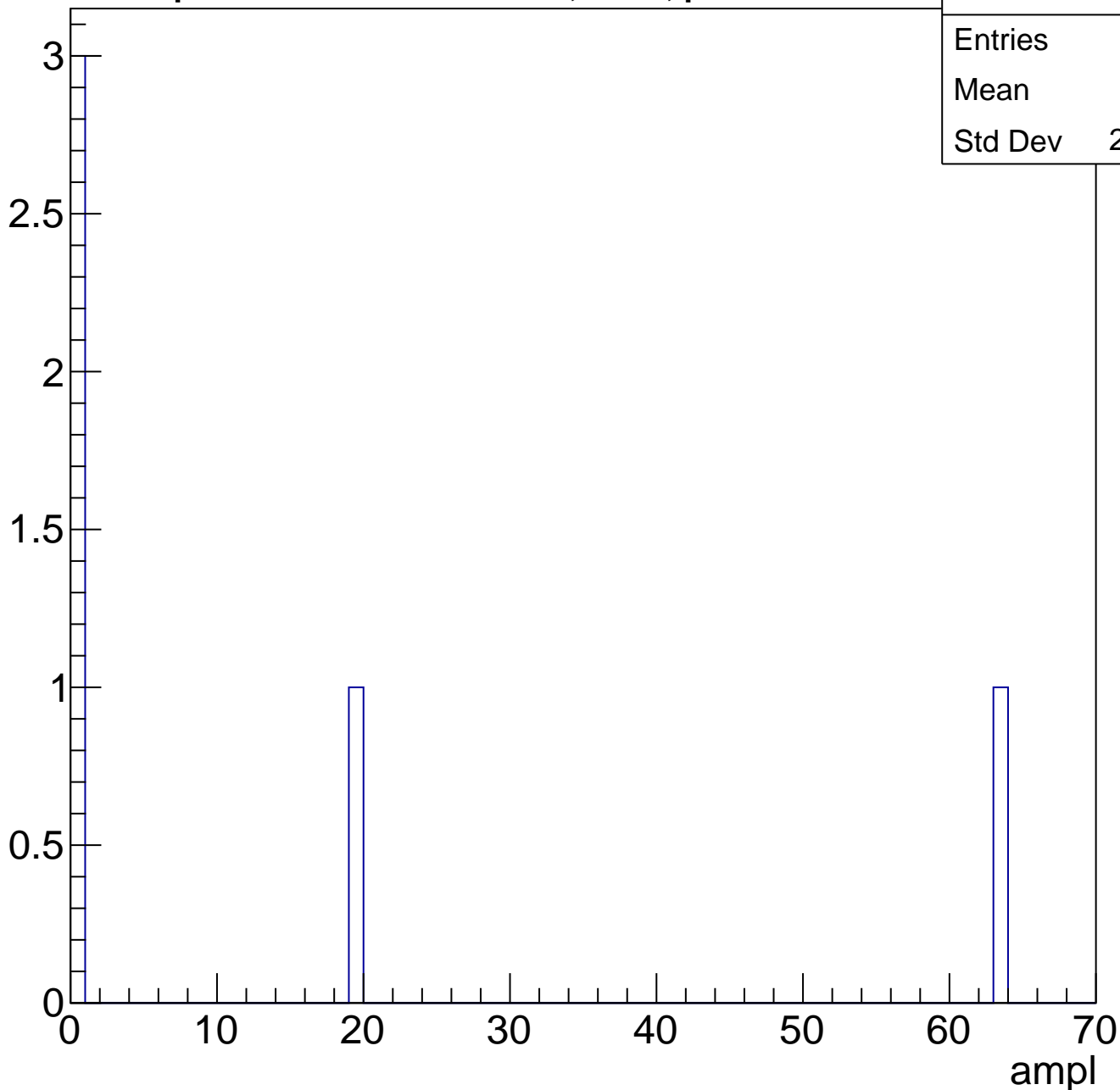




# B1L103S, U26-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	5
Mean	16.4
Std Dev	24.43

# B1L103S, U26-ch82, adc0

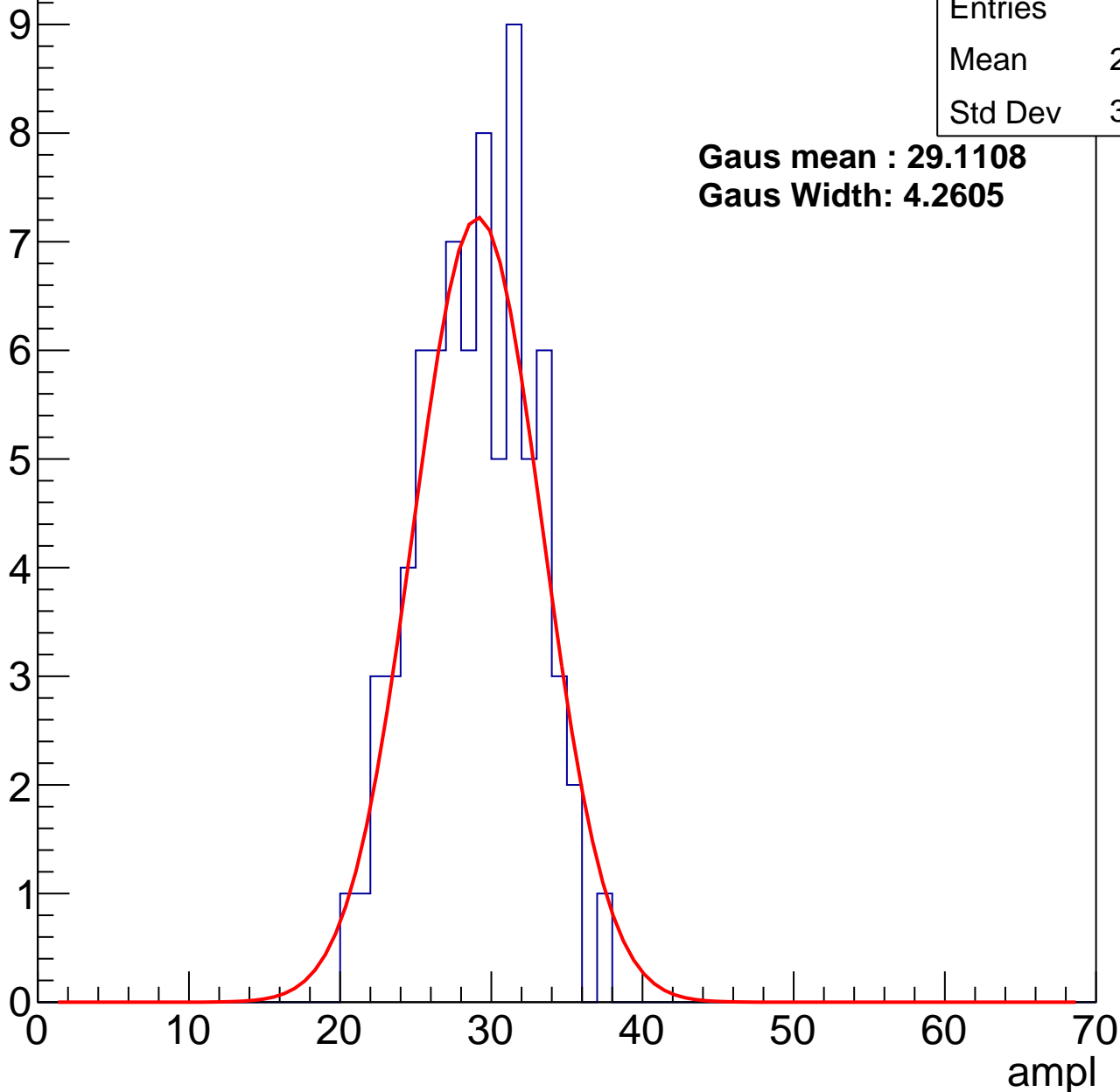
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	28.46
Std Dev	3.726

**Gaus mean : 29.1108**

**Gaus Width: 4.2605**



# B1L103S, U26-ch82, adc1

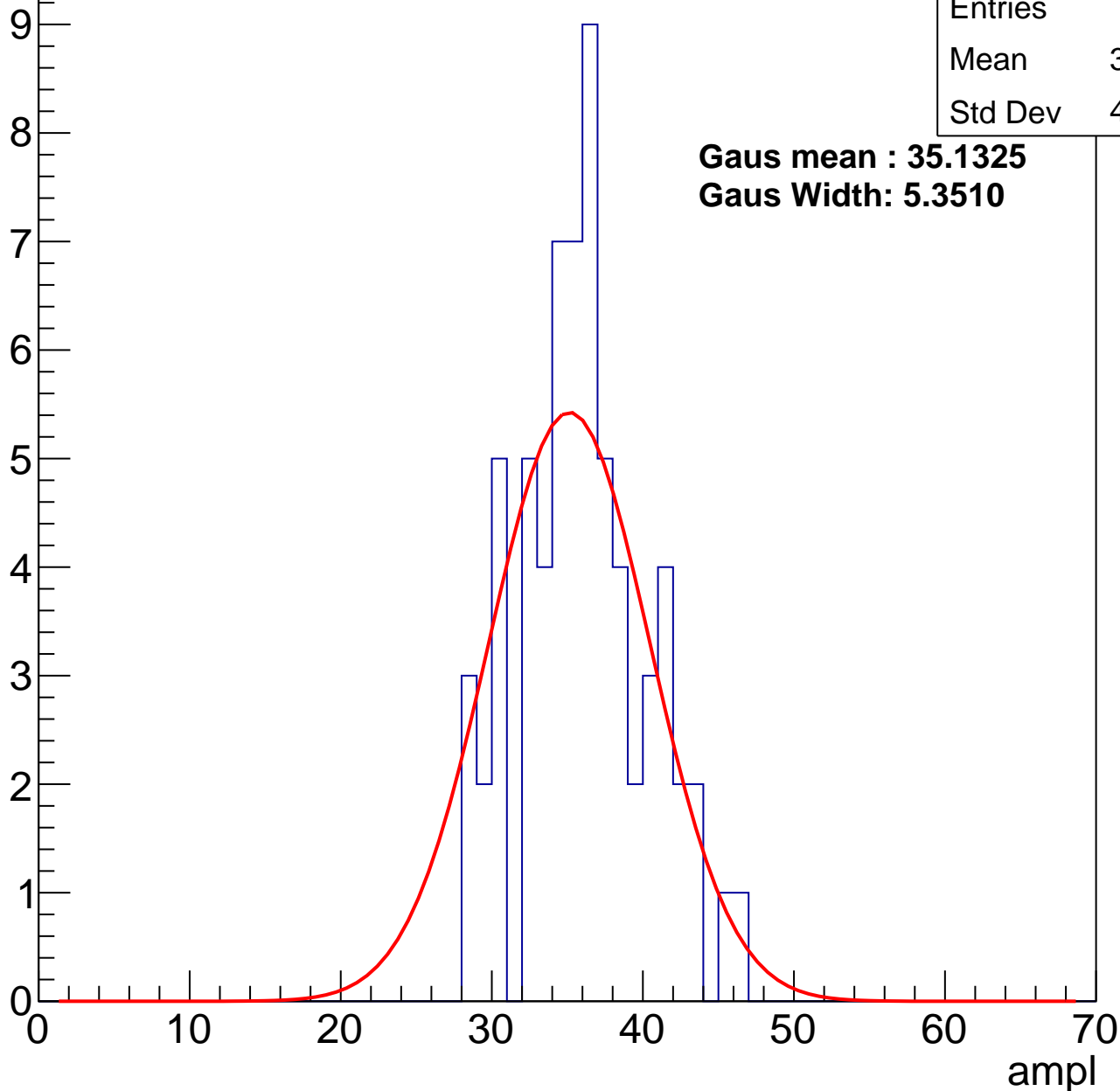
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	35.62
Std Dev	4.173

**Gaus mean : 35.1325**

**Gaus Width: 5.3510**



# B1L103S, U26-ch82, adc2

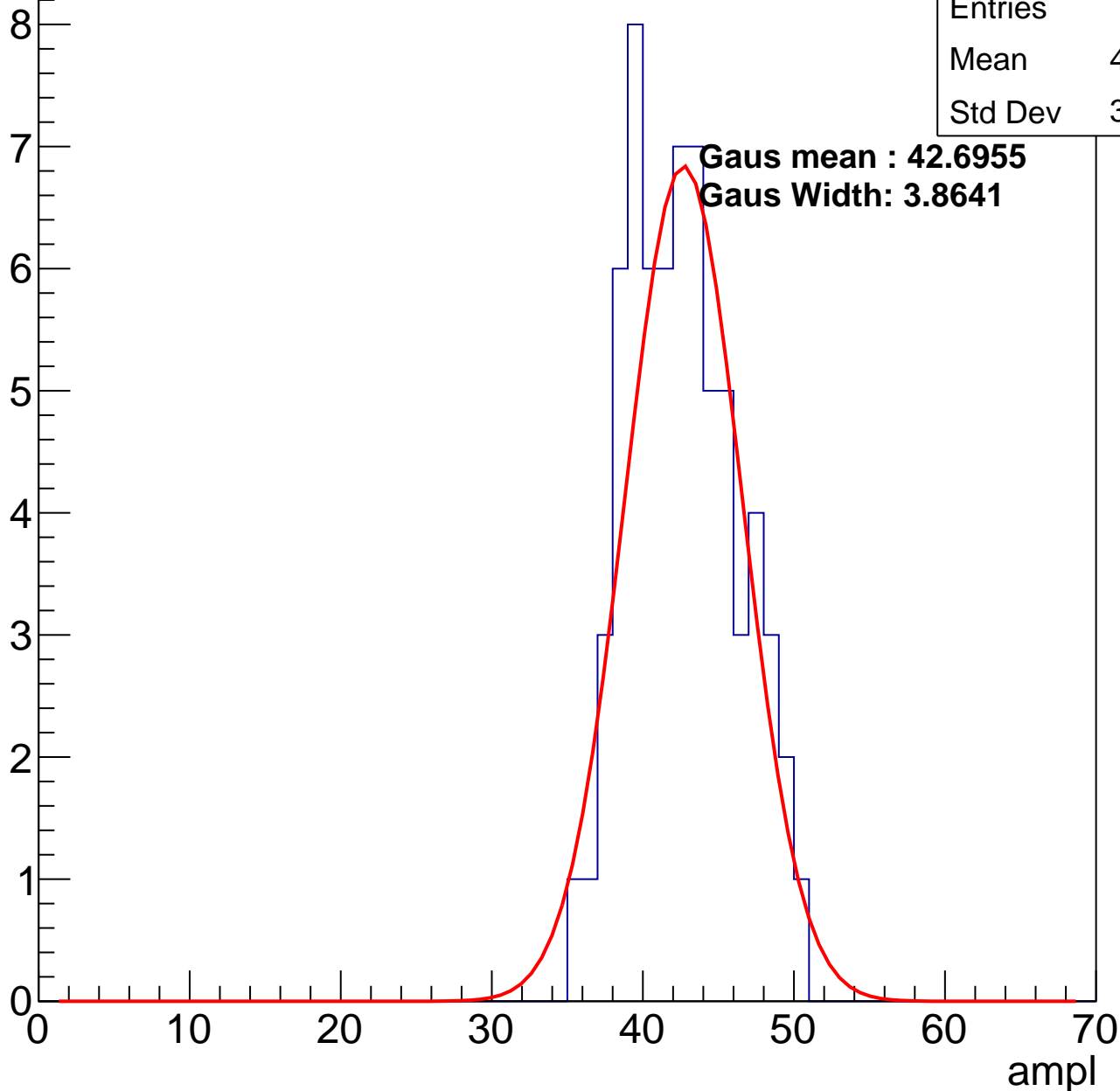
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	42.15
Std Dev	3.528

**Gaus mean : 42.6955**

**Gaus Width: 3.8641**



# B1L103S, U26-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	82
Mean	49.45
Std Dev	3.945

Entry

10

8

6

4

2

0

0

10

20

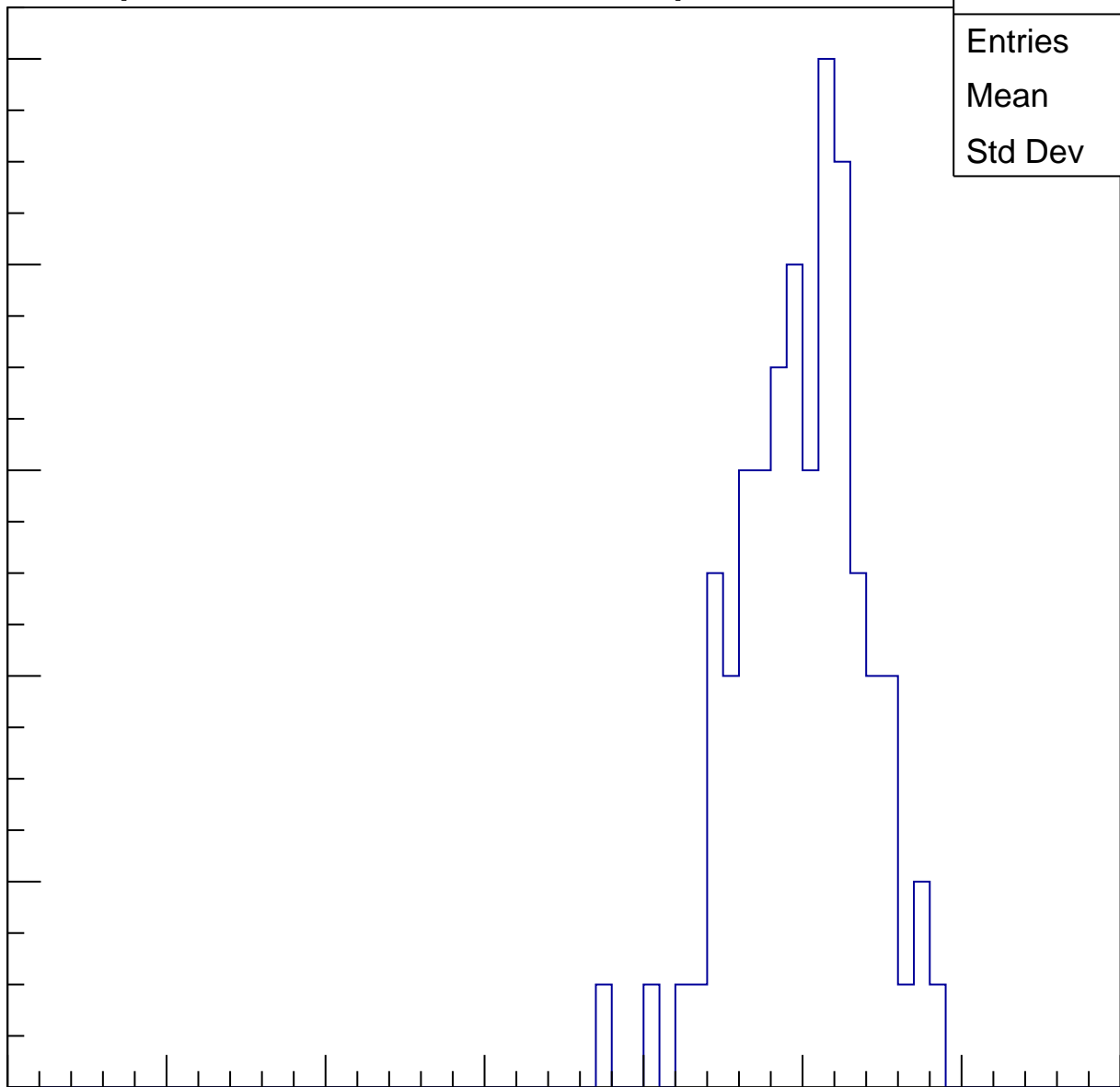
30

40

50

60

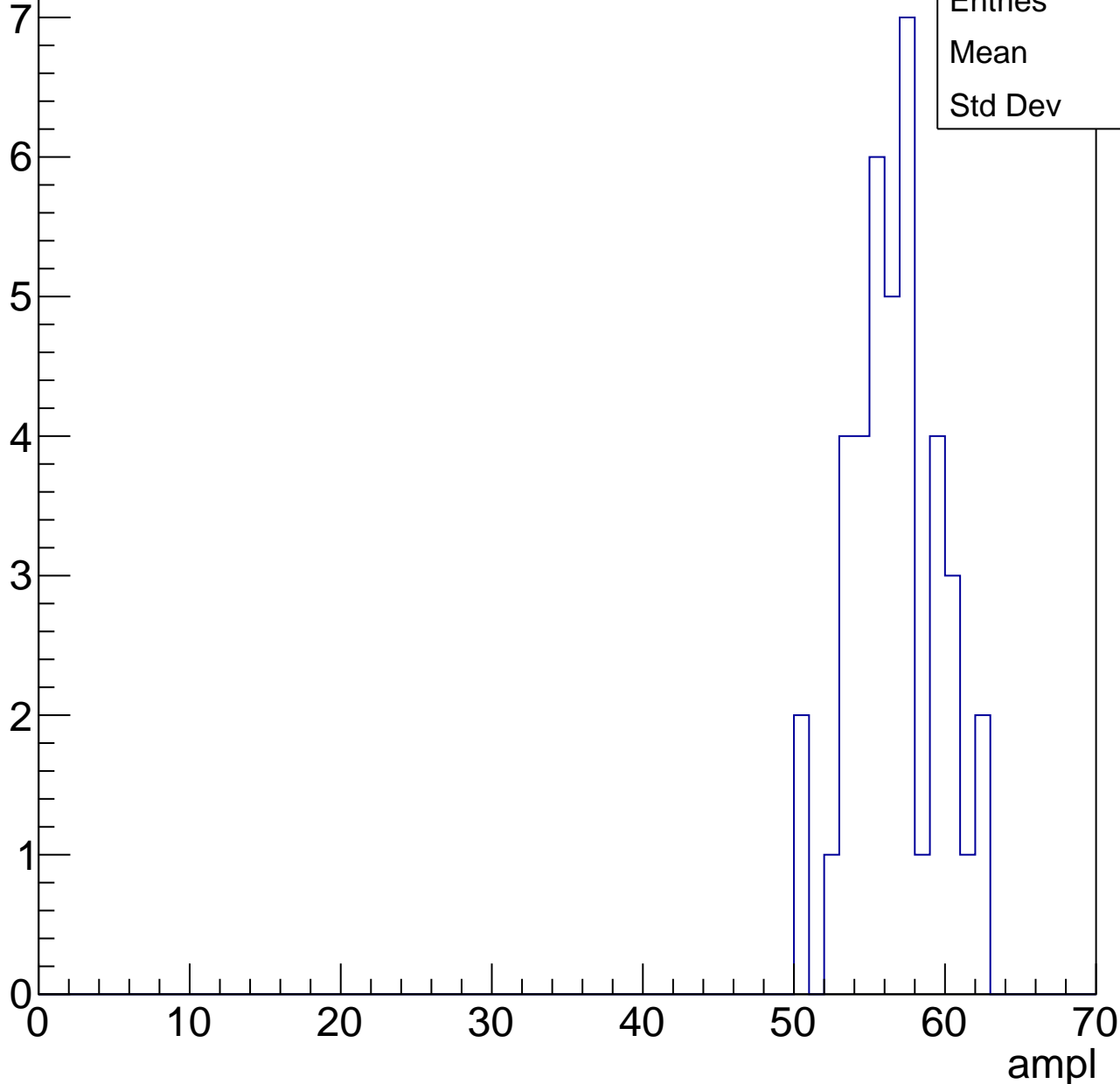
ampl



# B1L103S, U26-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

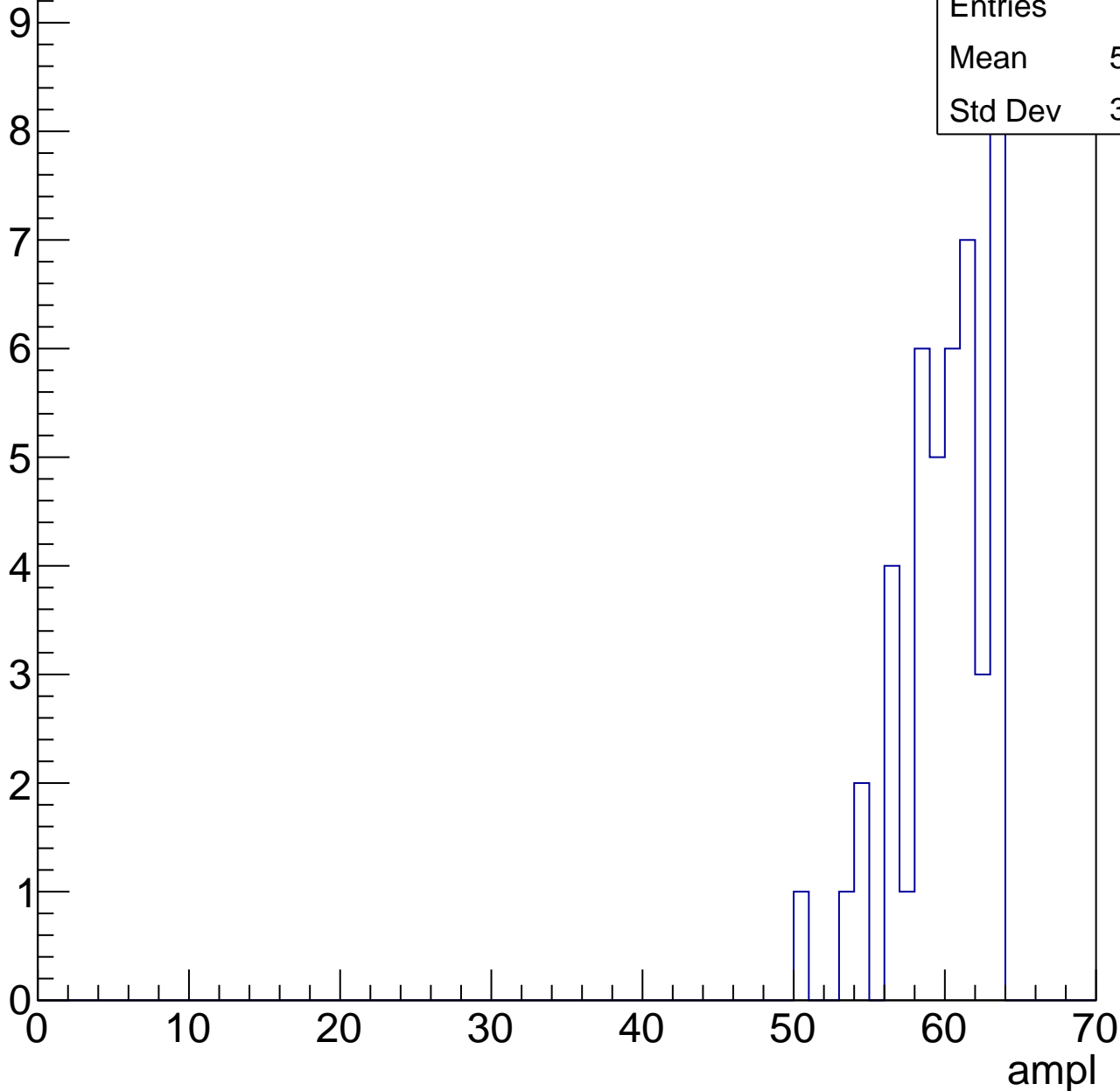


# B1L103S, U26-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	59.44
Std Dev	3.015

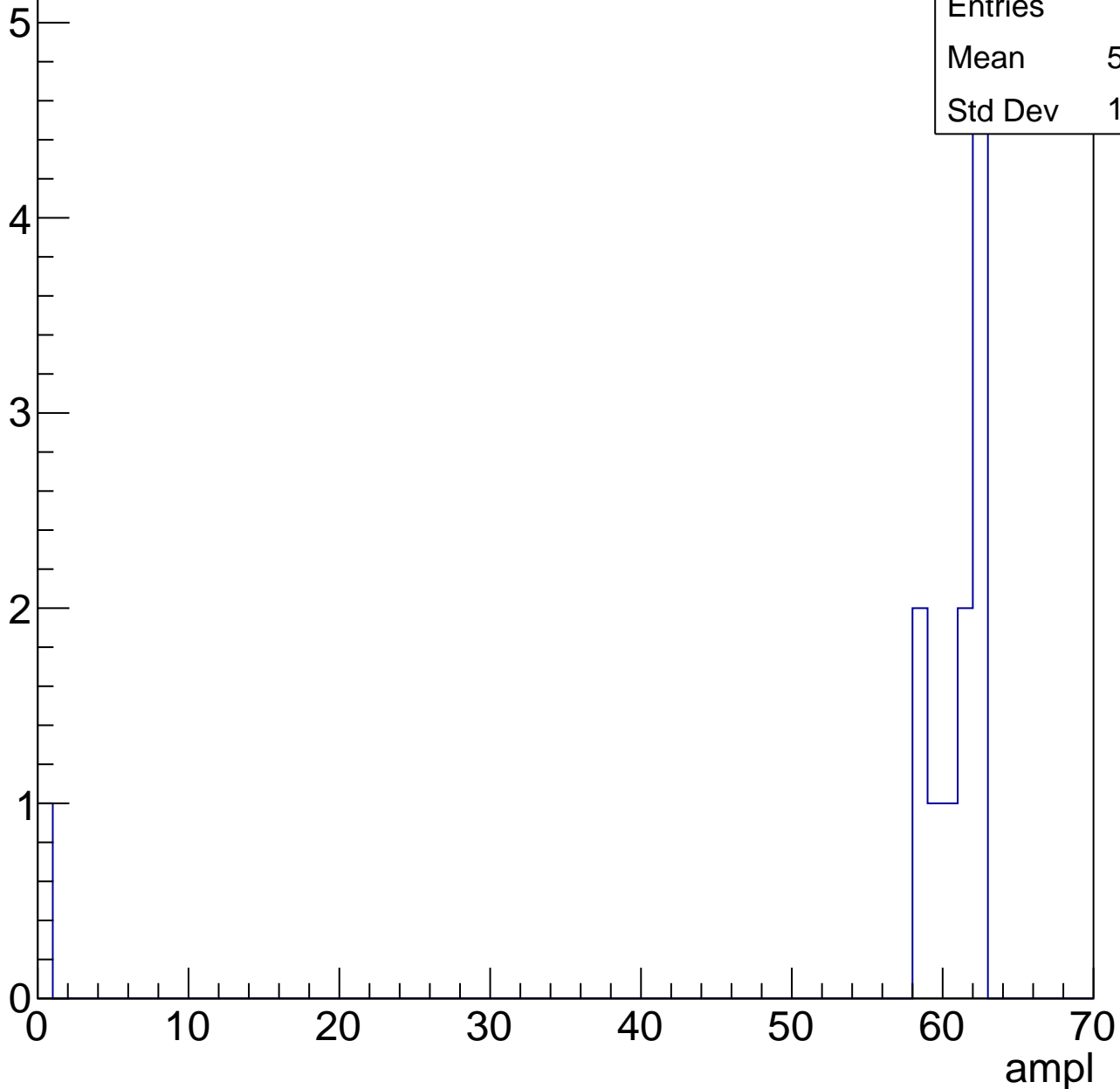


# B1L103S, U26-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	12
Mean	55.58
Std Dev	16.82





# B1L103S, U26-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch83, adc0

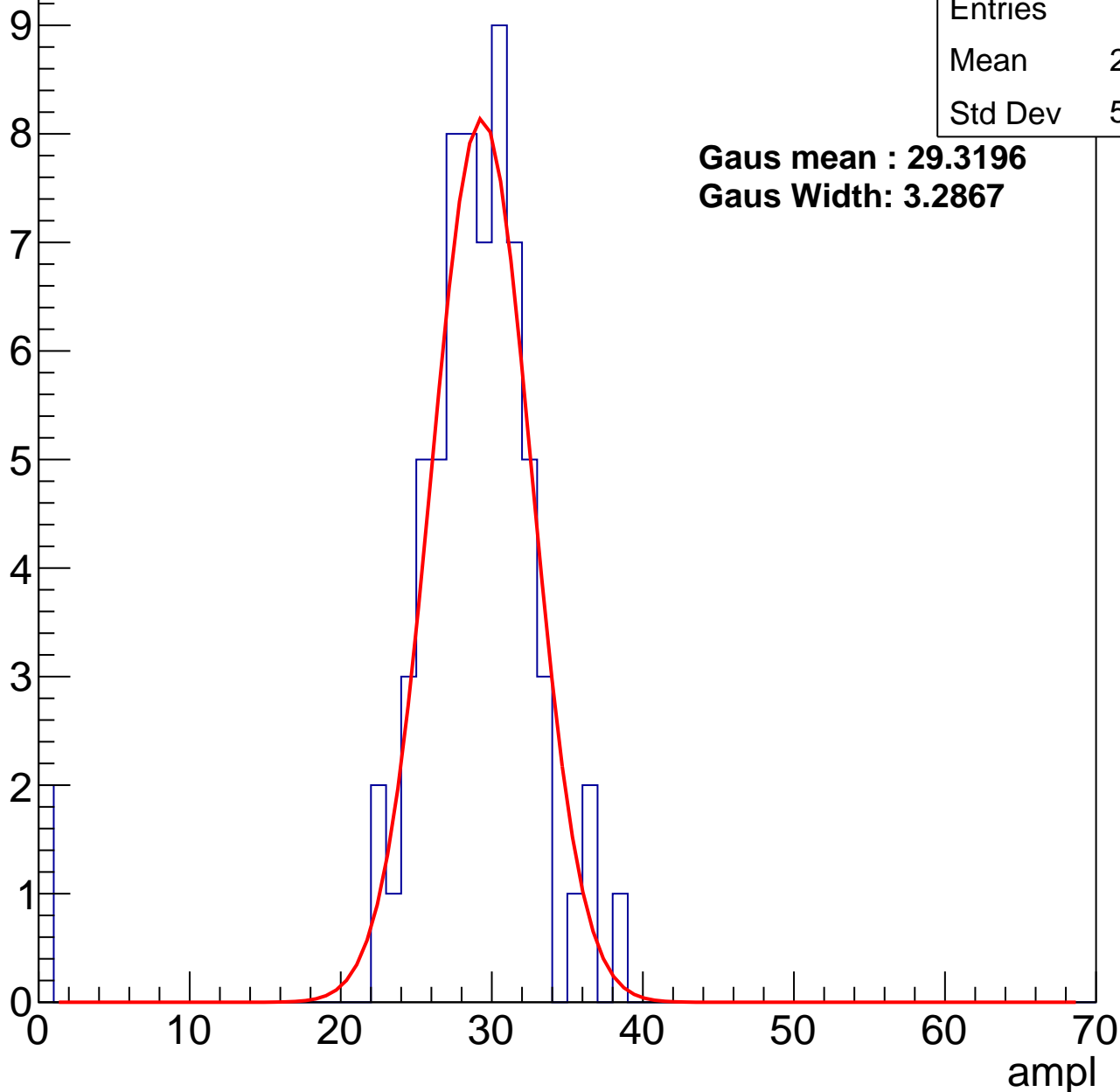
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	27.94
Std Dev	5.803

**Gaus mean : 29.3196**

**Gaus Width: 3.2867**



# B1L103S, U26-ch83, adc1

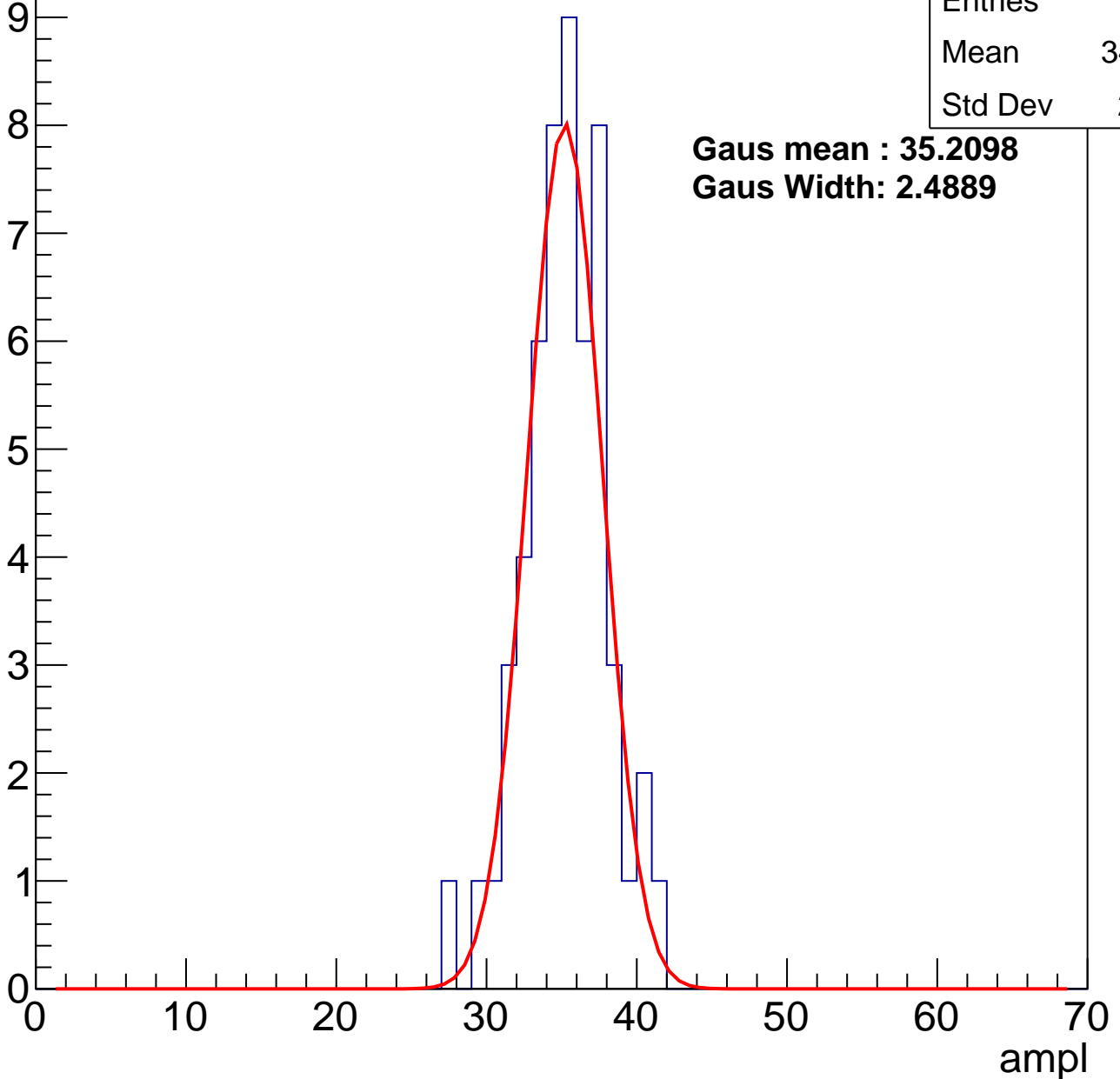
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	34.78
Std Dev	2.74

**Gaus mean : 35.2098**

**Gaus Width: 2.4889**



# B1L103S, U26-ch83, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	41.47
Std Dev	3.33

**Gaus mean : 41.9285**

**Gaus Width: 3.2176**

10

8

6

4

2

0

0

10

20

30

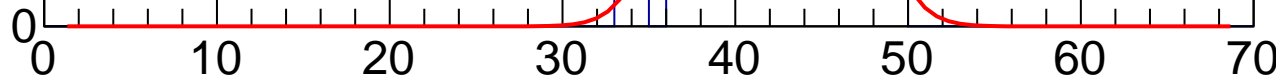
40

50

60

70

ampl

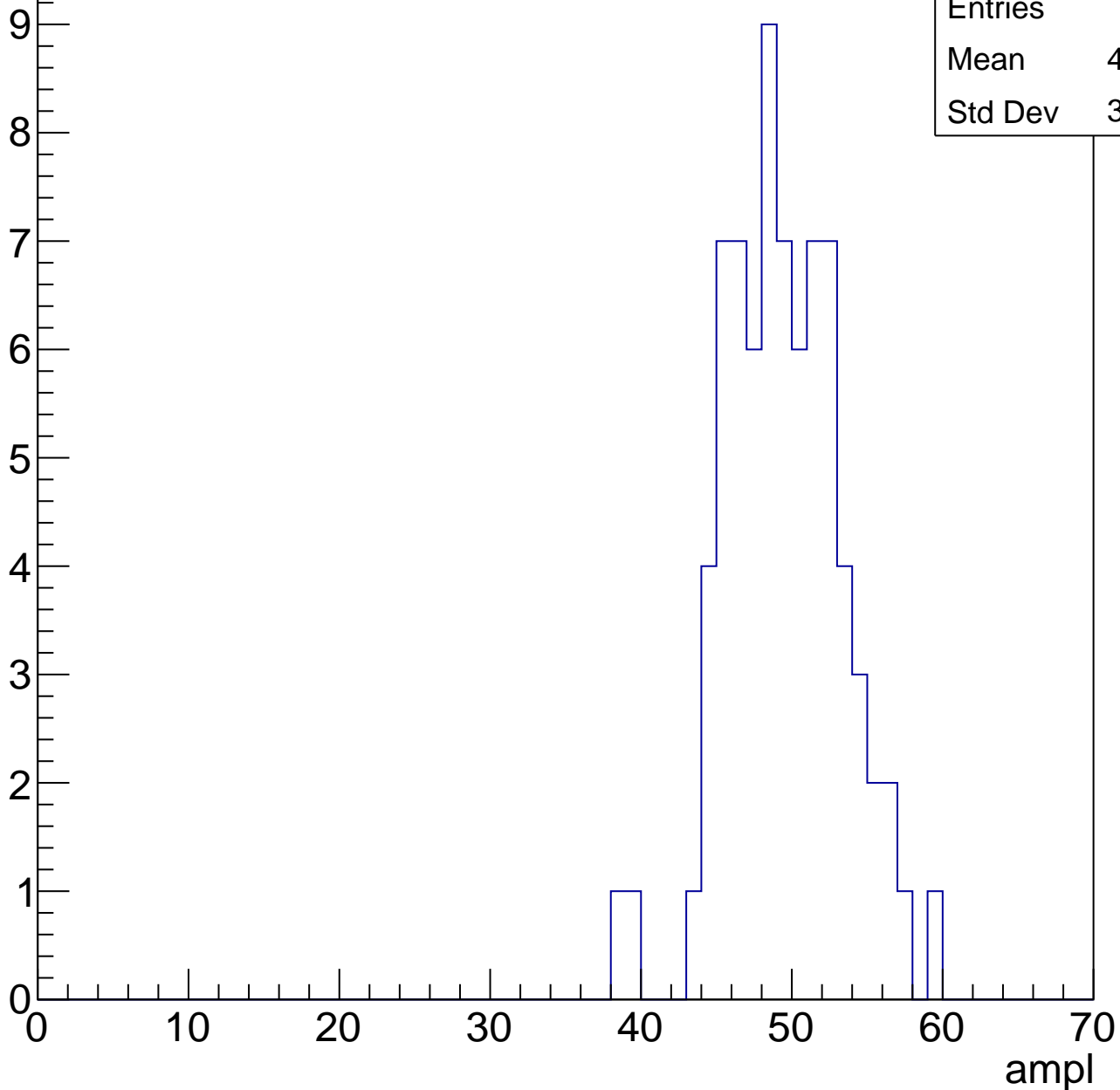


# B1L103S, U26-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	48.99
Std Dev	3.864

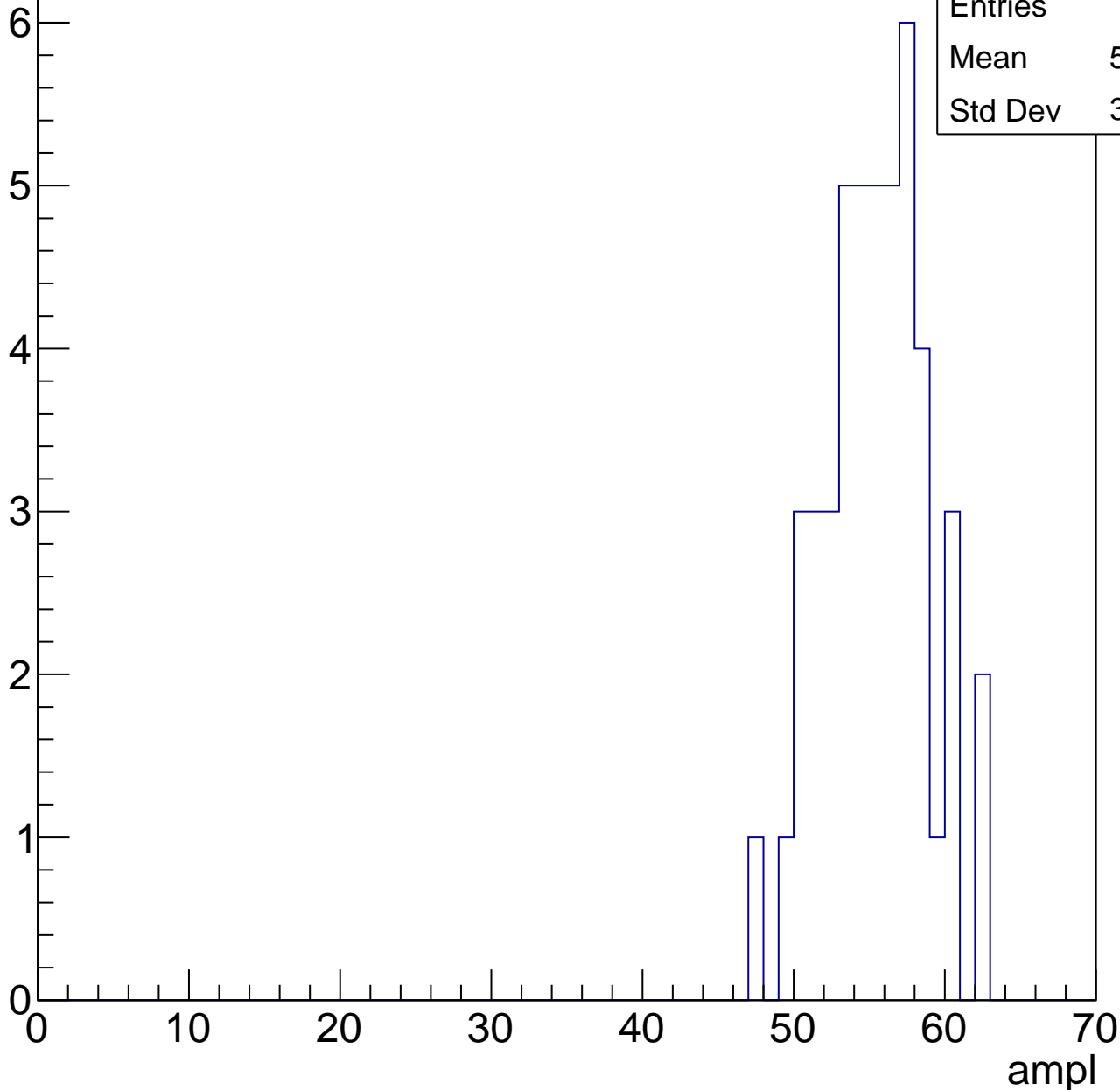


# B1L103S, U26-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	54.94
Std Dev	3.354

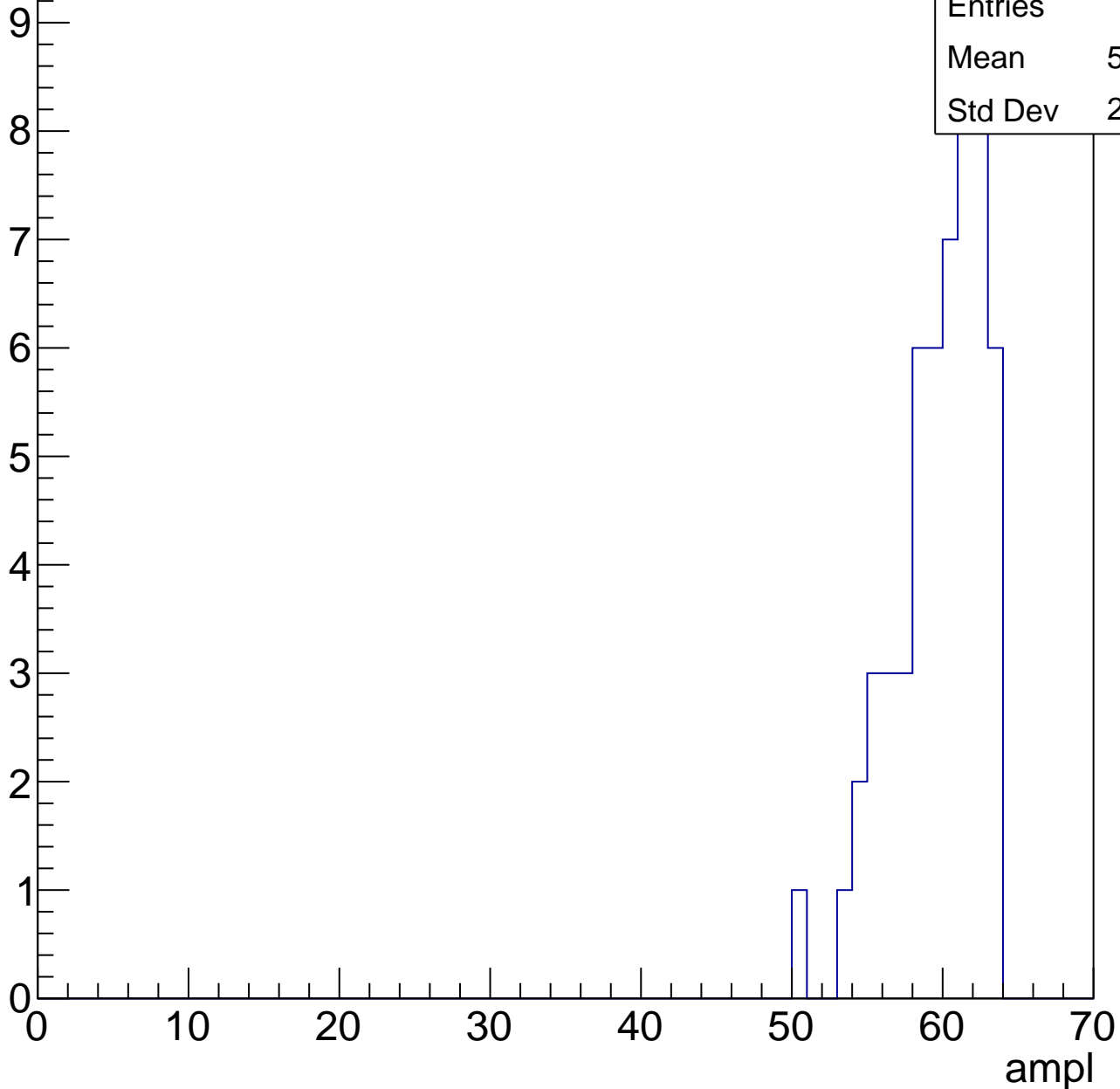


# B1L103S, U26-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

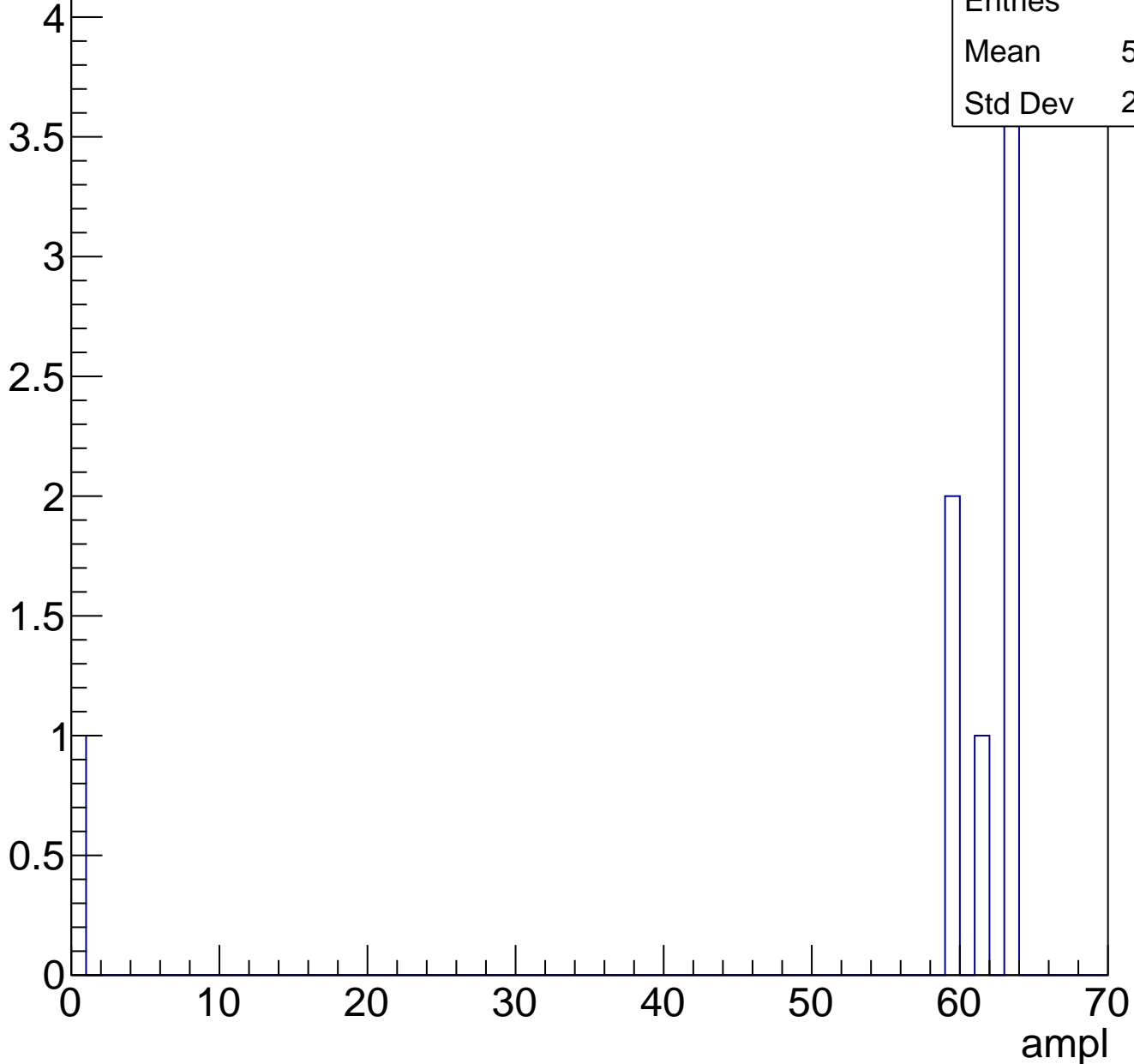
Entries	55
Mean	59.27
Std Dev	2.914



# B1L103S, U26-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch84, adc0

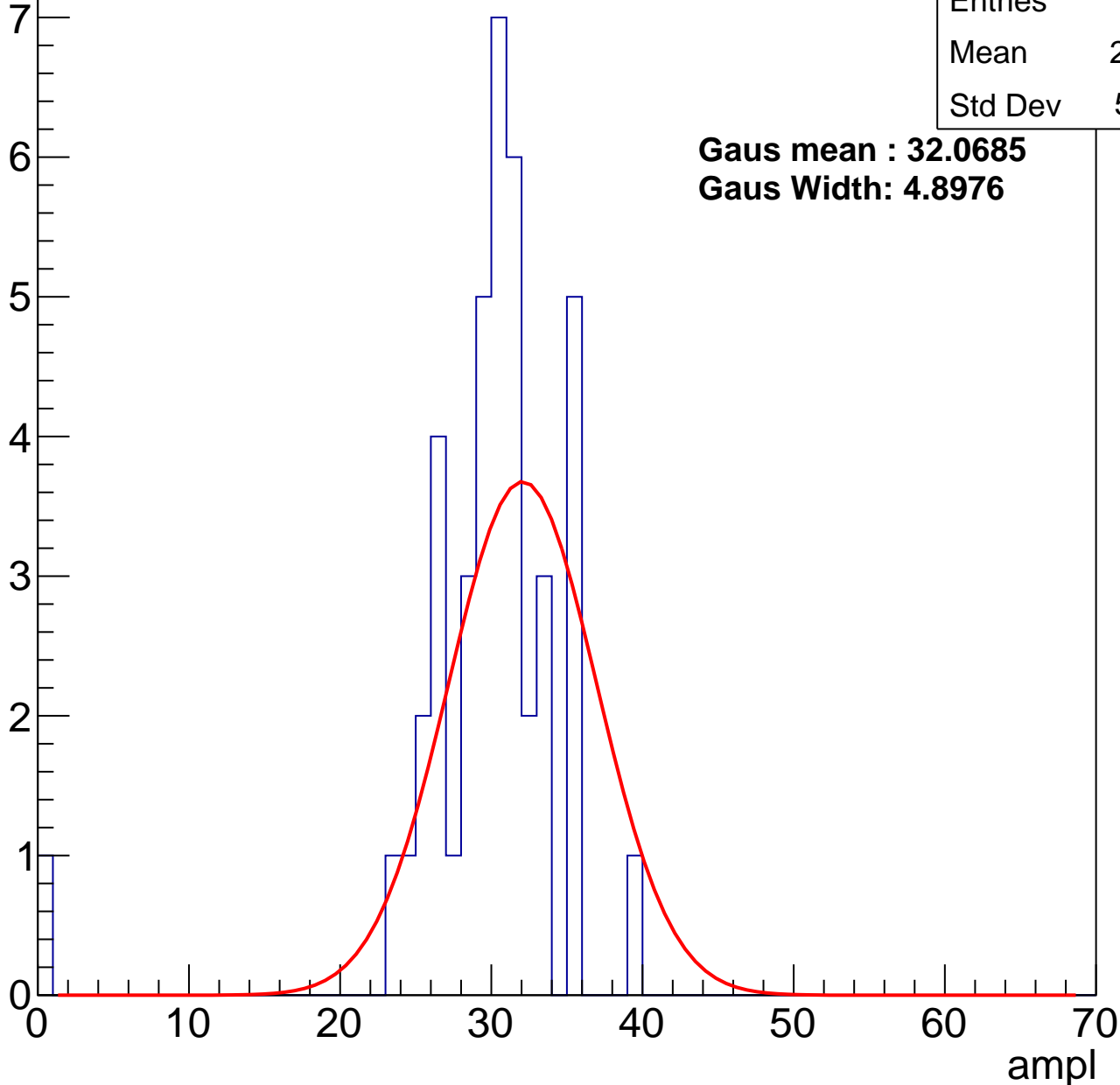
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	42
Mean	29.29
Std Dev	5.671

**Gaus mean : 32.0685**

**Gaus Width: 4.8976**



# B1L103S, U26-ch84, adc1

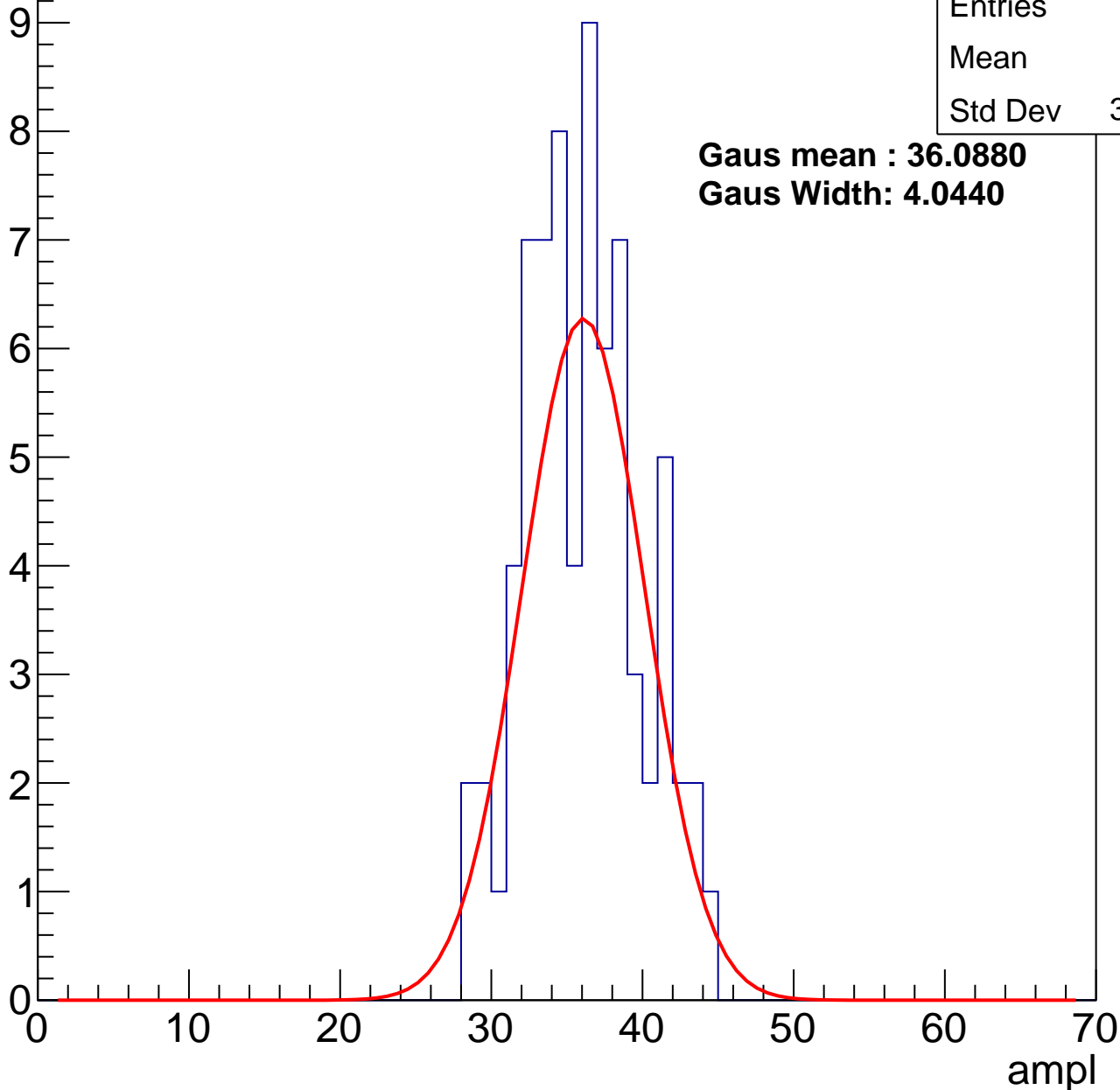
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	35.6
Std Dev	3.752

**Gaus mean : 36.0880**

**Gaus Width: 4.0440**



# B1L103S, U26-ch84, adc2

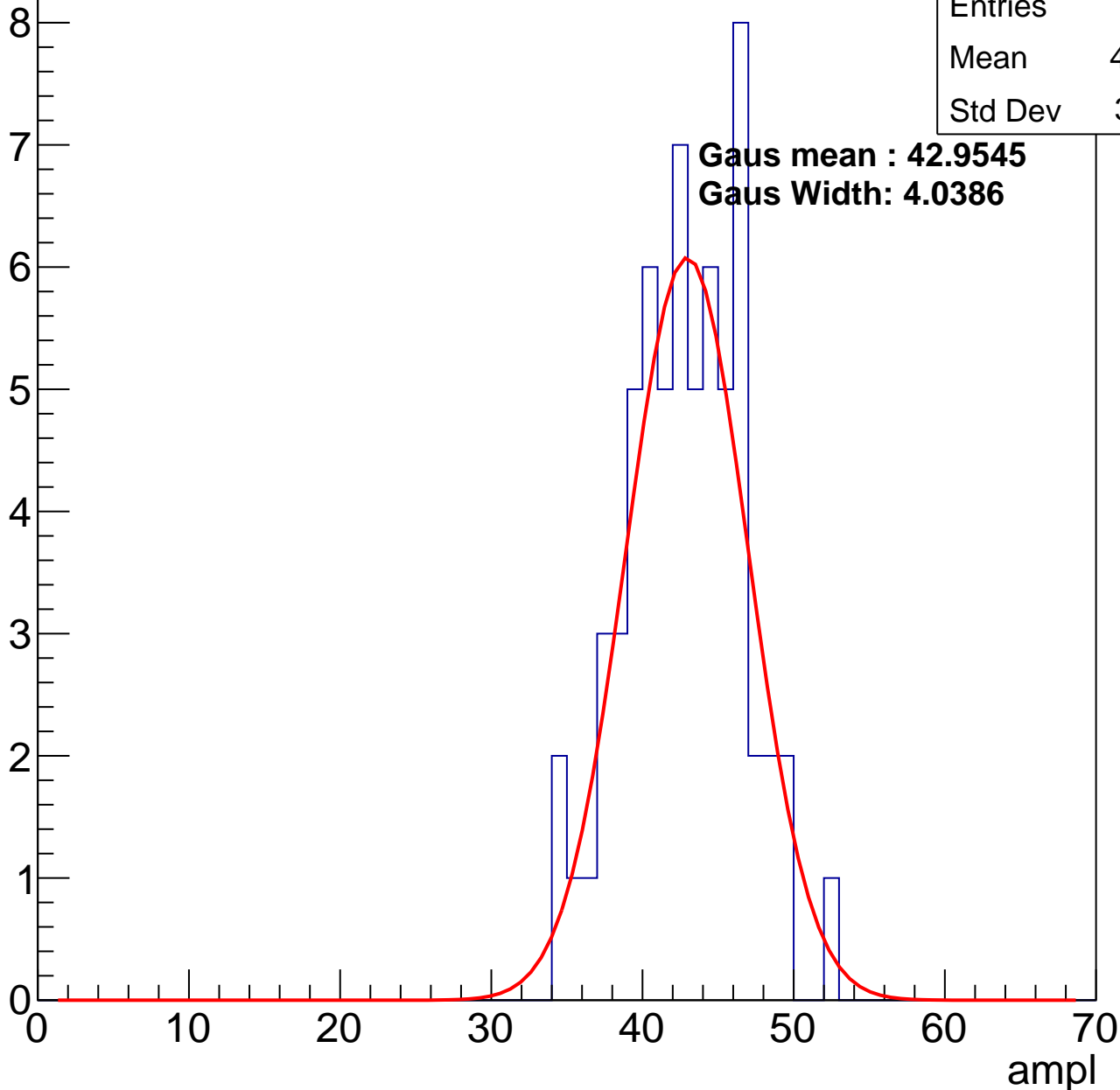
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	42.34
Std Dev	3.801

**Gaus mean : 42.9545**

**Gaus Width: 4.0386**

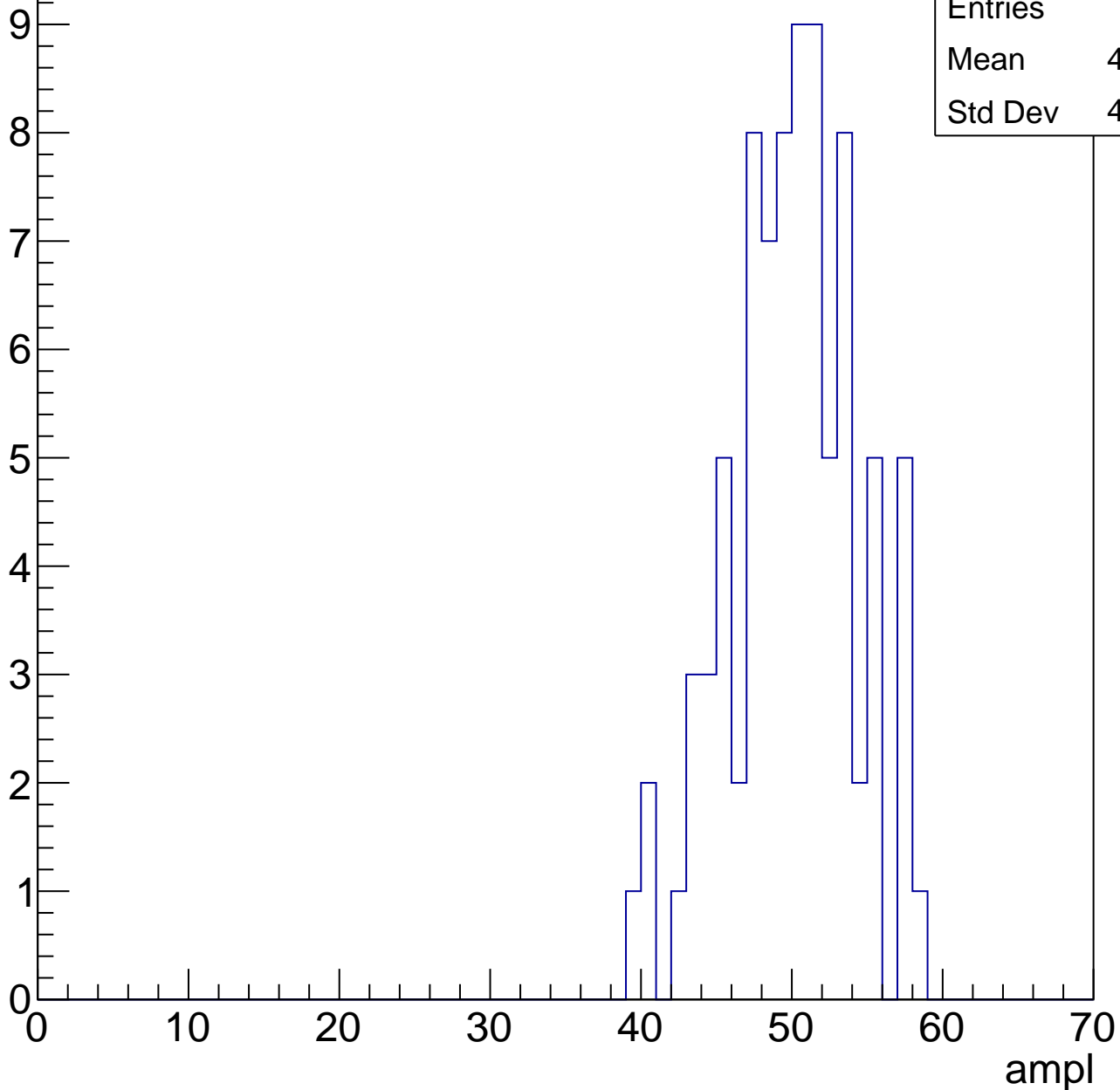


# B1L103S, U26-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

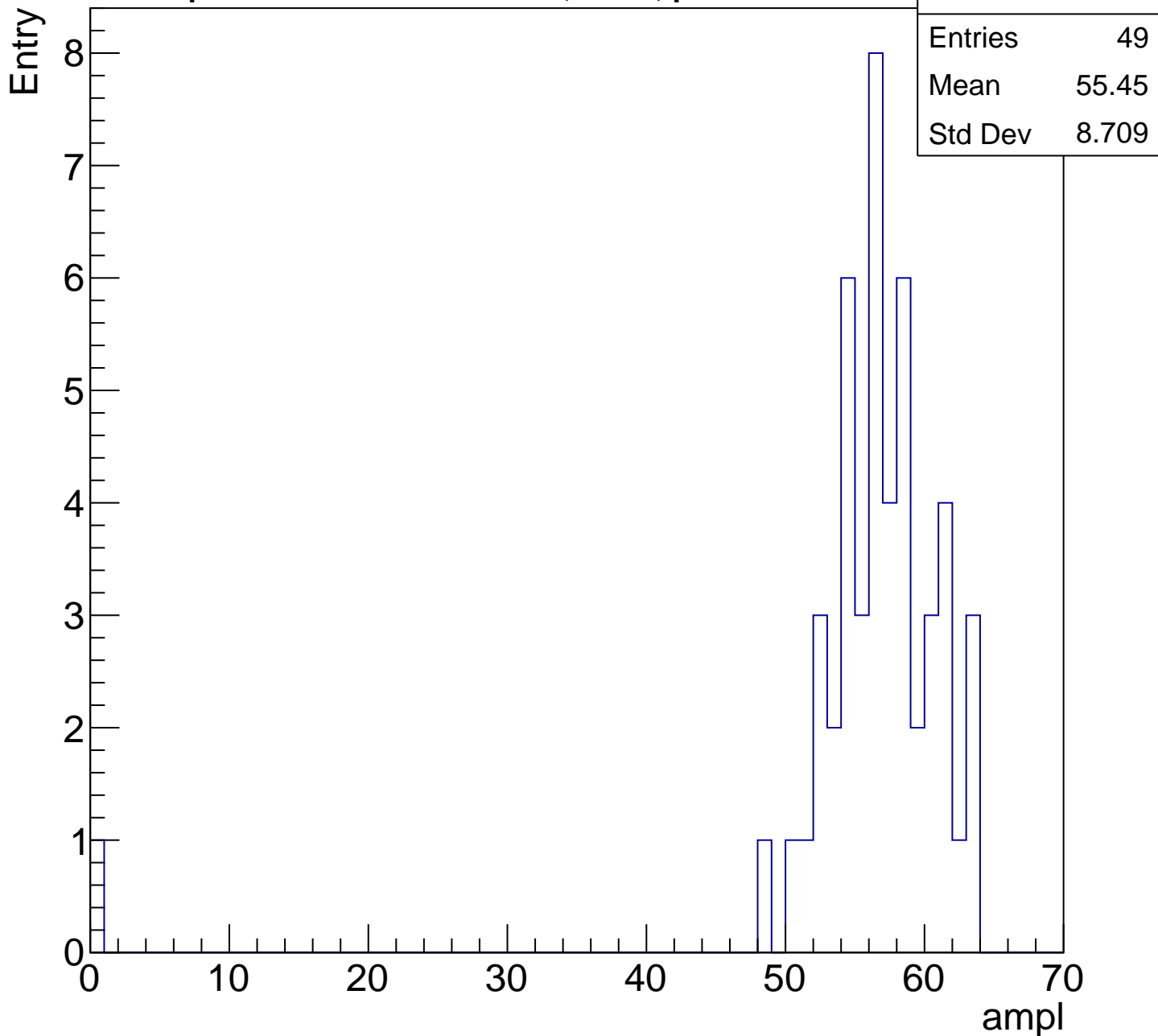
Entry

Entries	84
Mean	49.55
Std Dev	4.162



# B1L103S, U26-ch84, adc4

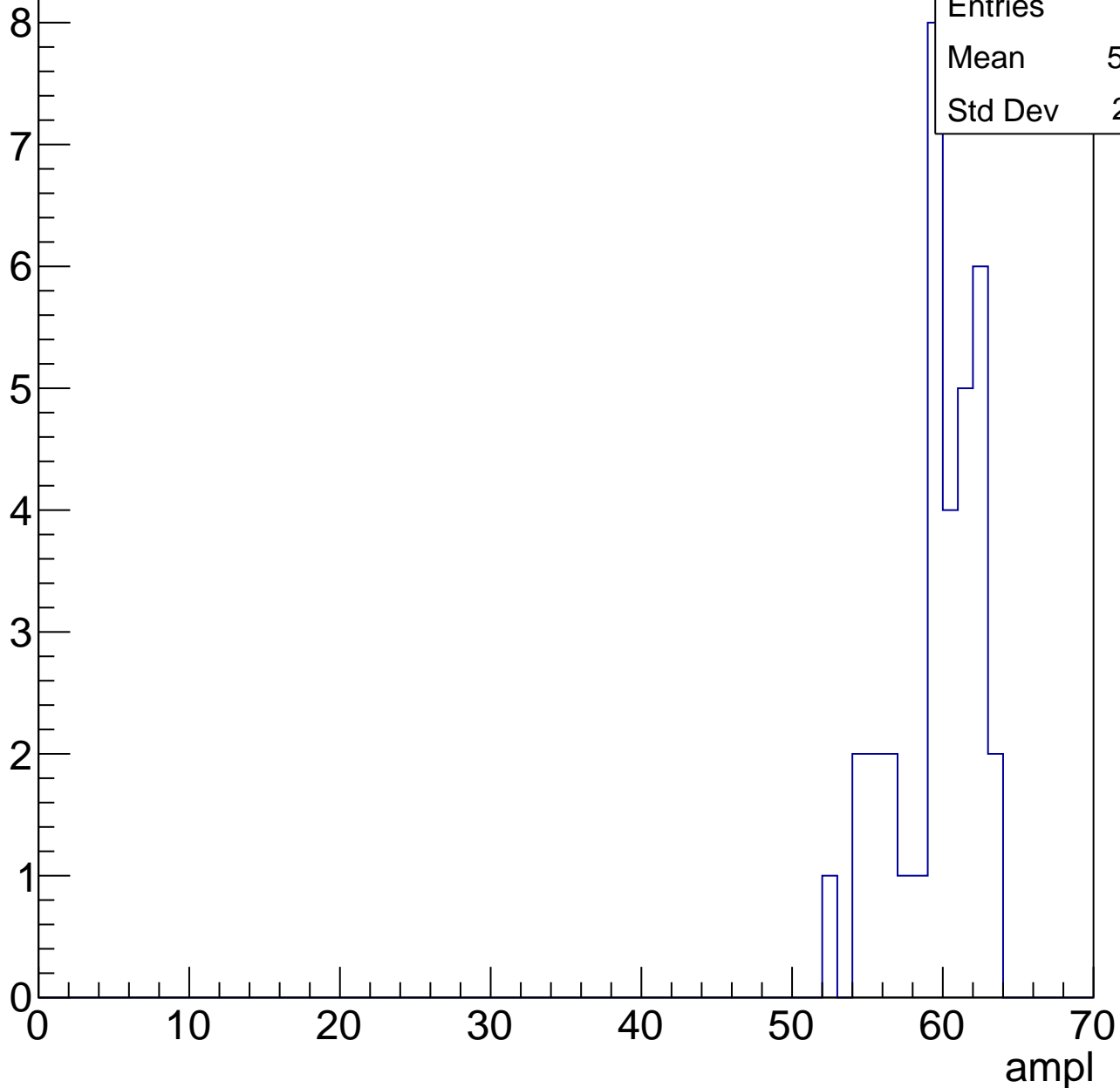
calib\_packv5\_042523\_0143.root, FC#7, port C2



# B1L103S, U26-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

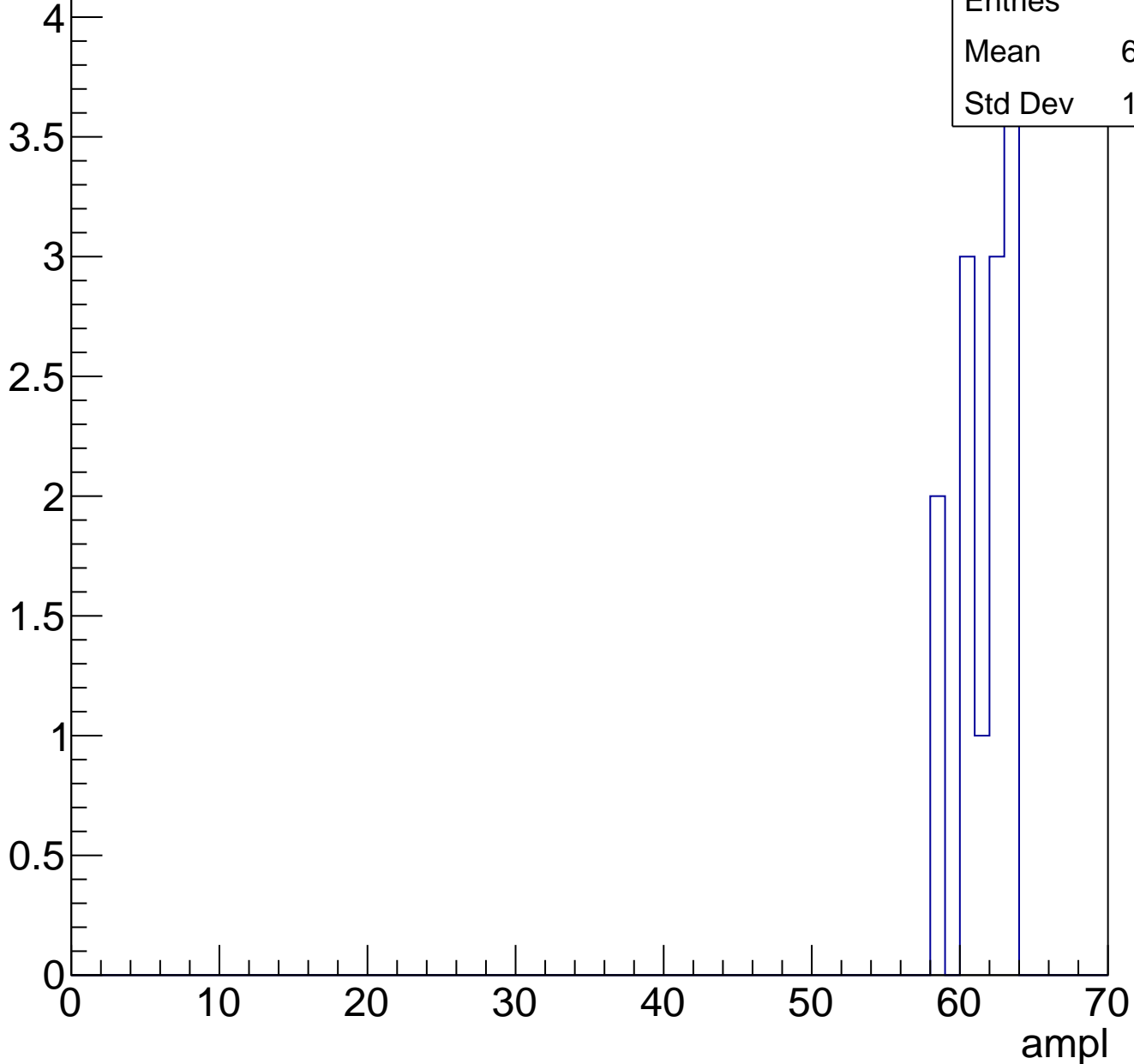
Entry



# B1L103S, U26-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch85, adc0

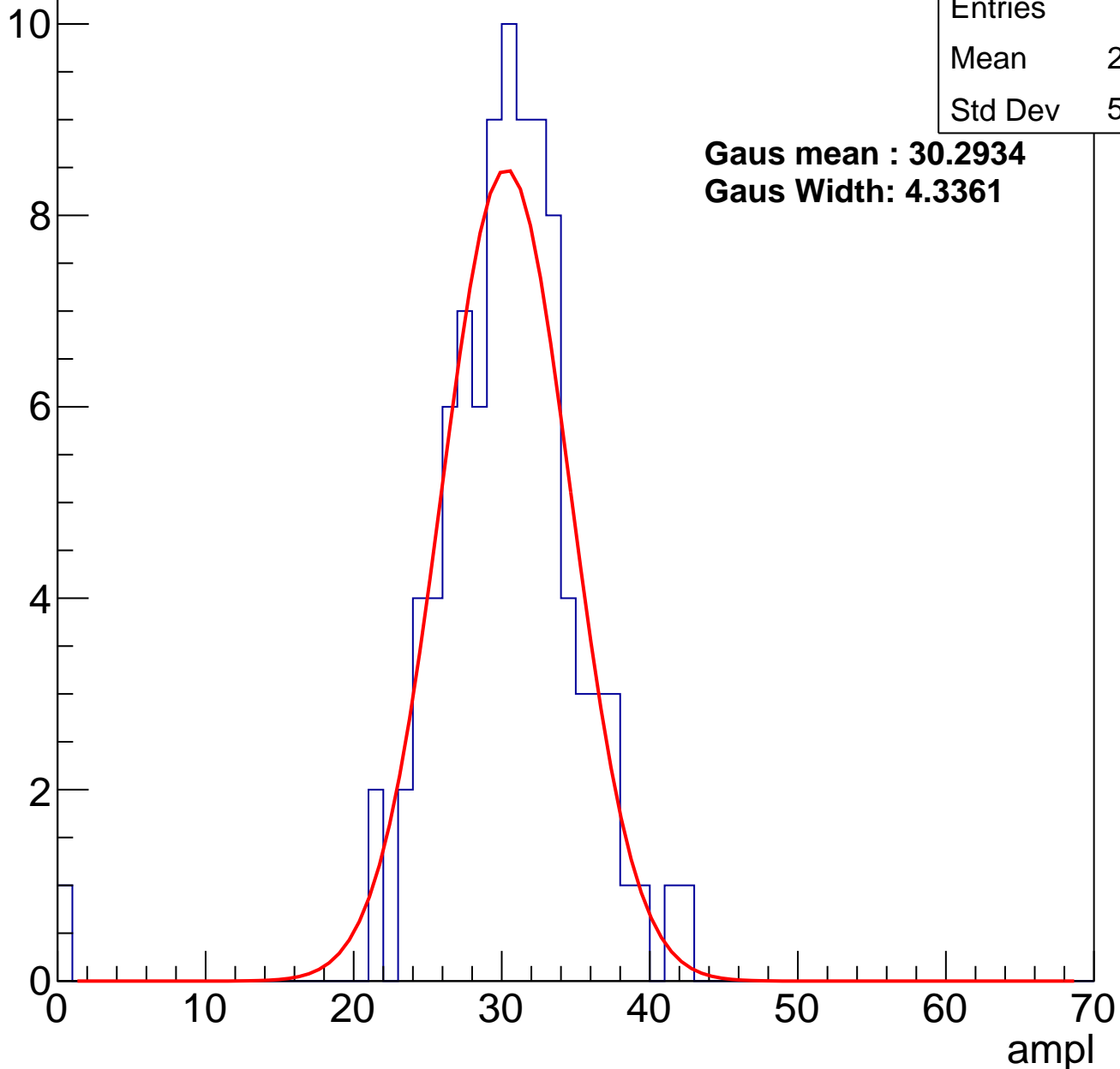
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	94
Mean	29.88
Std Dev	5.173

**Gaus mean : 30.2934**

**Gaus Width: 4.3361**

Entry



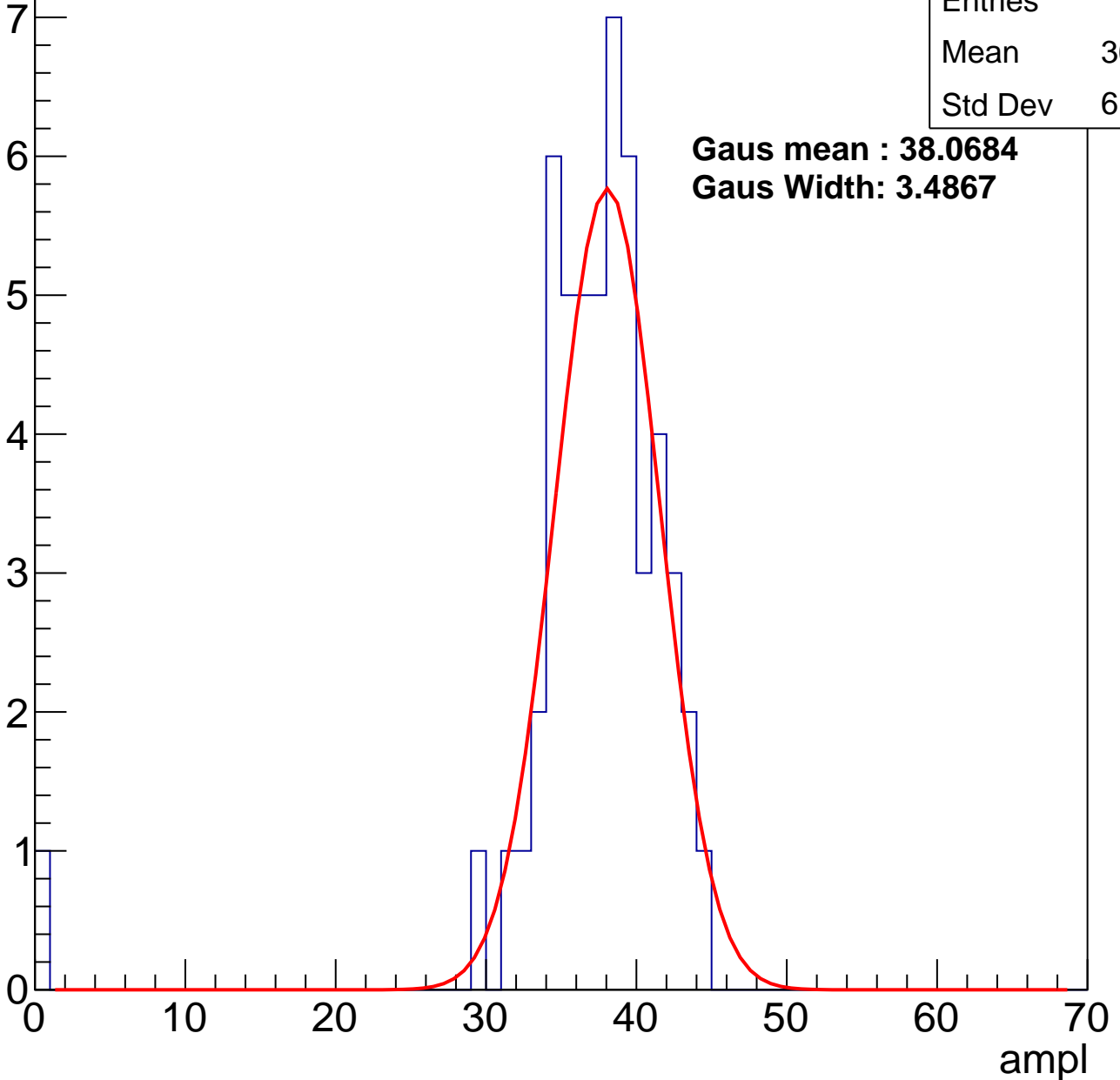
# B1L103S, U26-ch85, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	36.64
Std Dev	6.013

**Gaus mean : 38.0684**  
**Gaus Width: 3.4867**



# B1L103S, U26-ch85, adc2

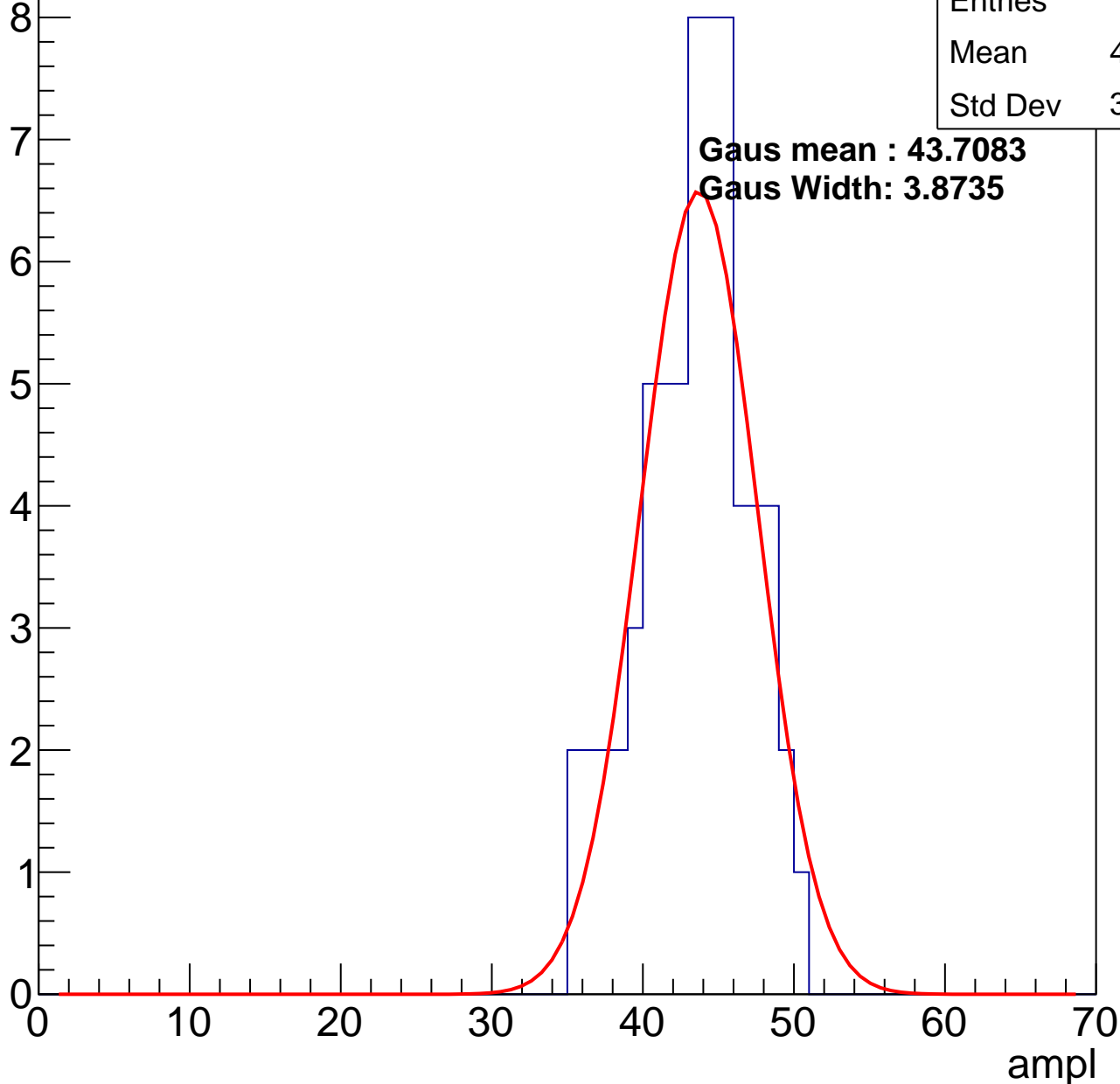
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	42.95
Std Dev	3.567

**Gaus mean : 43.7083**

**Gaus Width: 3.8735**

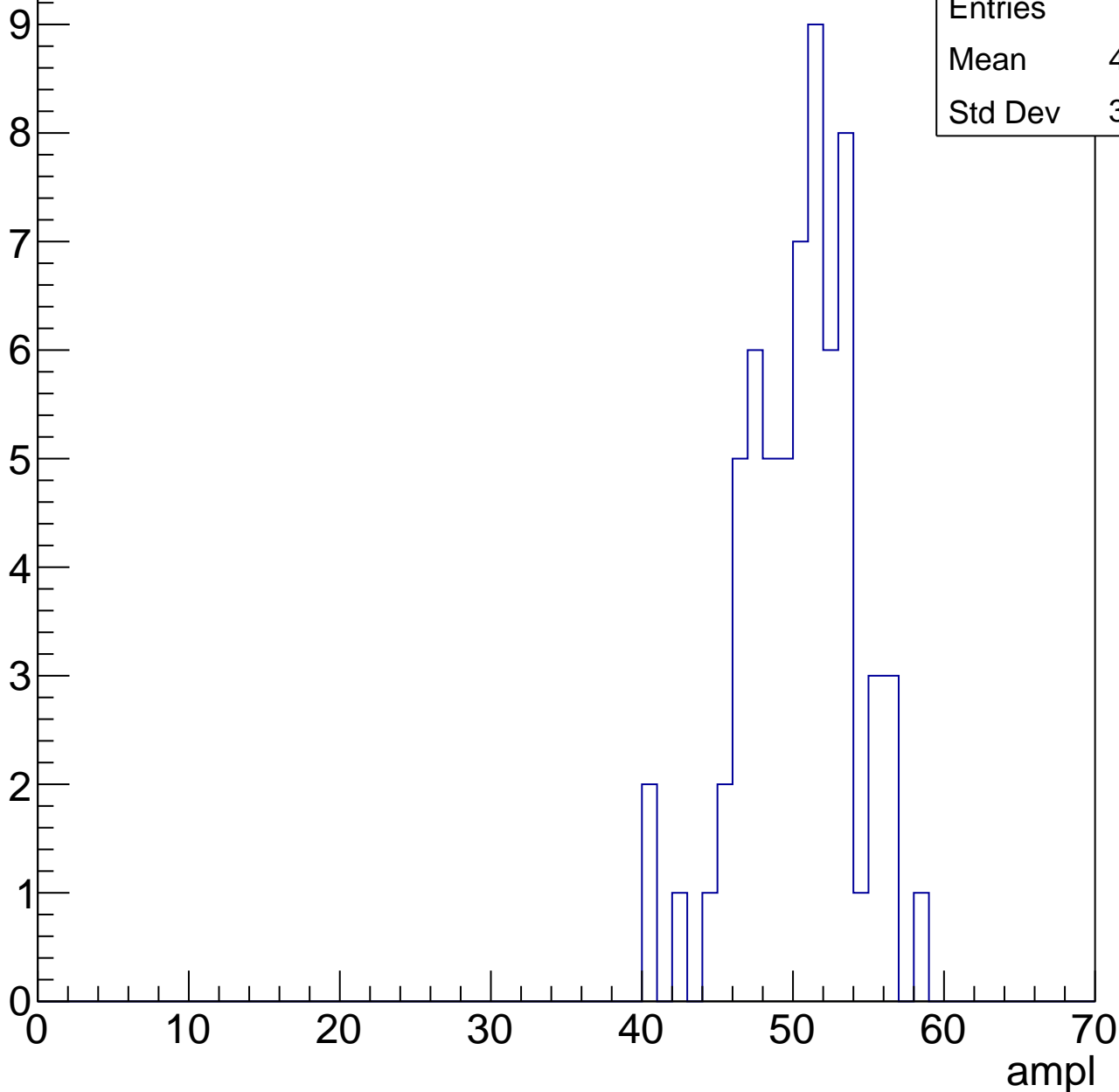


# B1L103S, U26-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	49.89
Std Dev	3.672

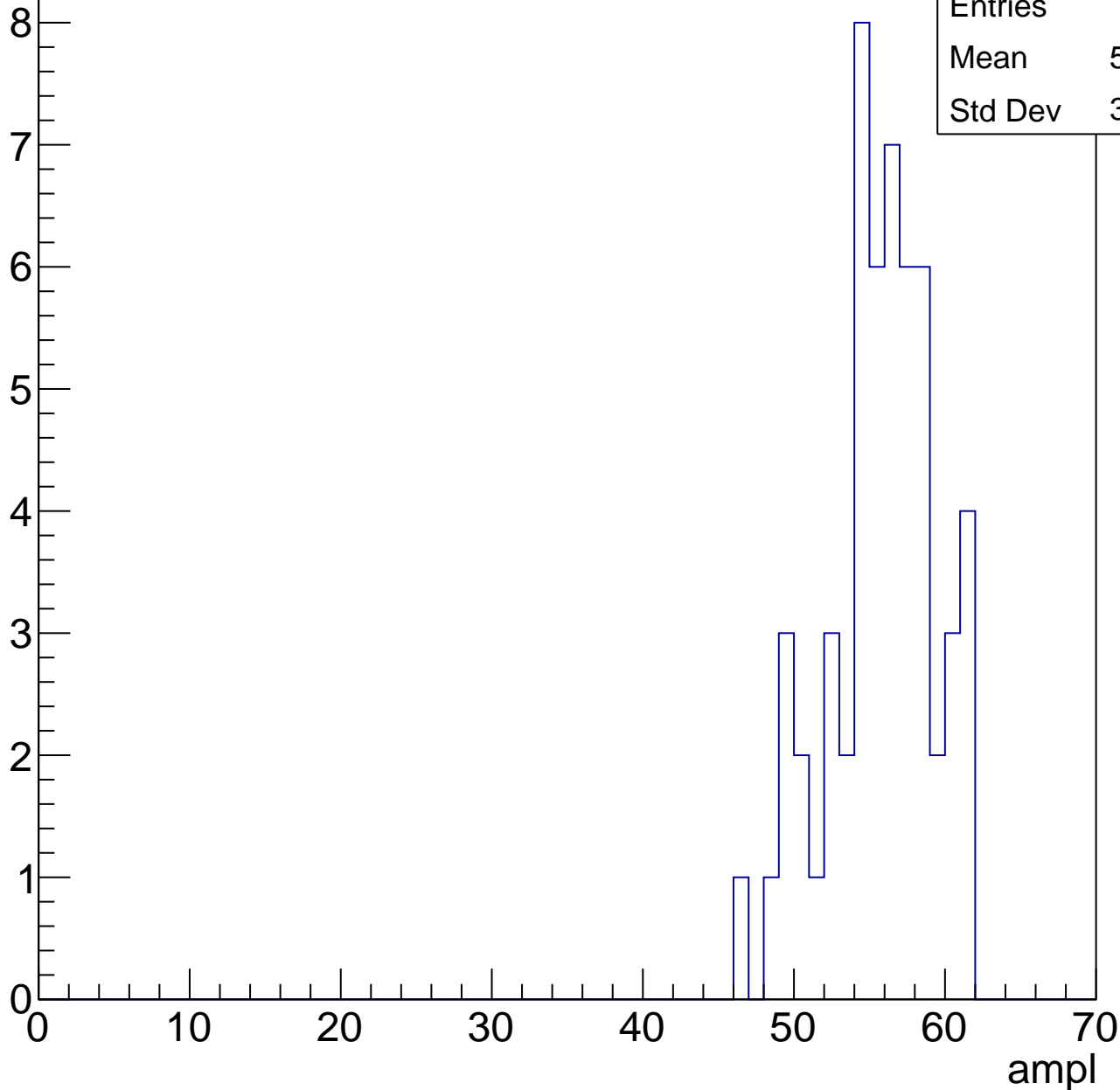


# B1L103S, U26-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	55.27
Std Dev	3.513

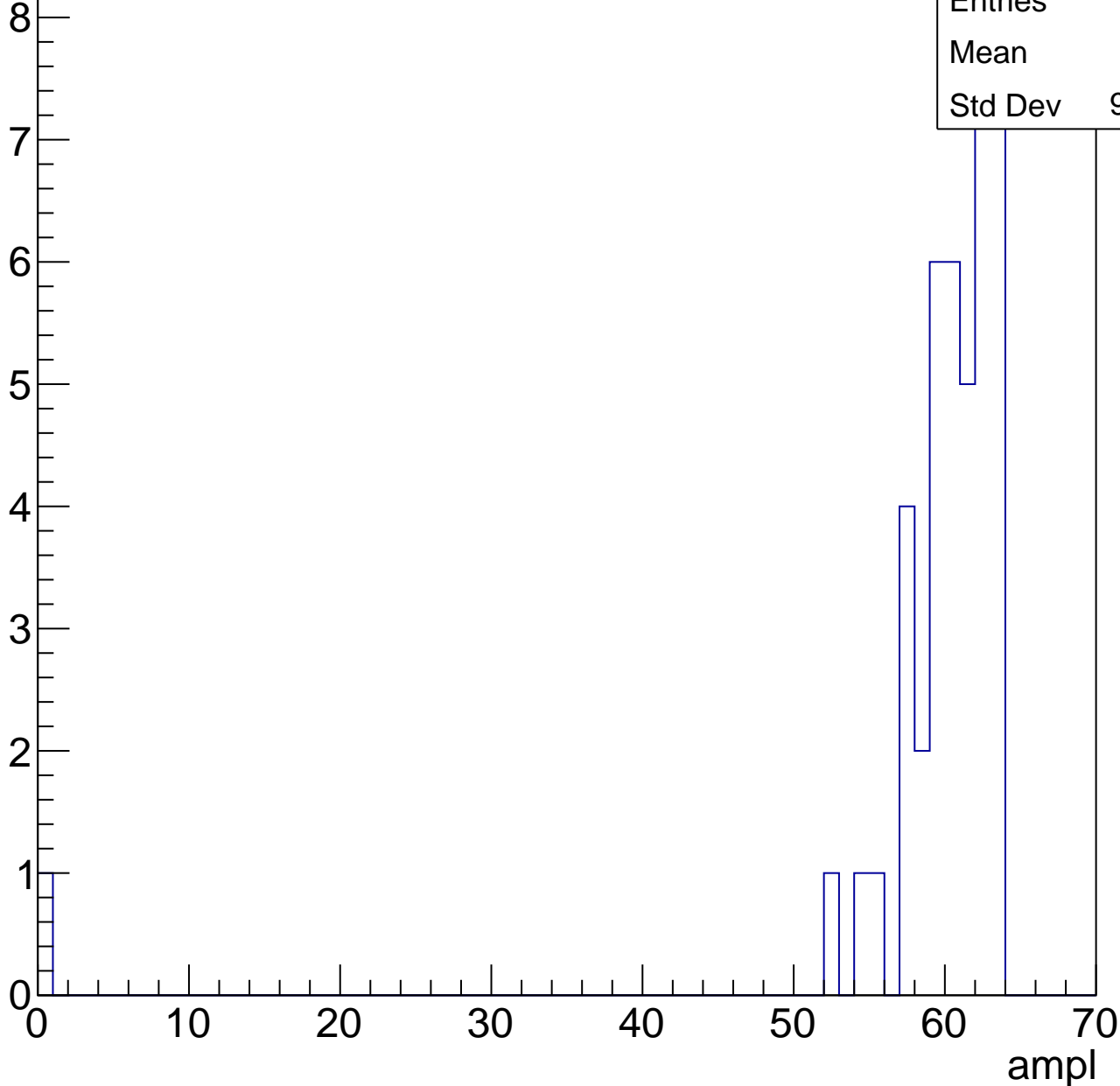


# B1L103S, U26-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	43
Mean	58.7
Std Dev	9.414



# B1L103S, U26-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

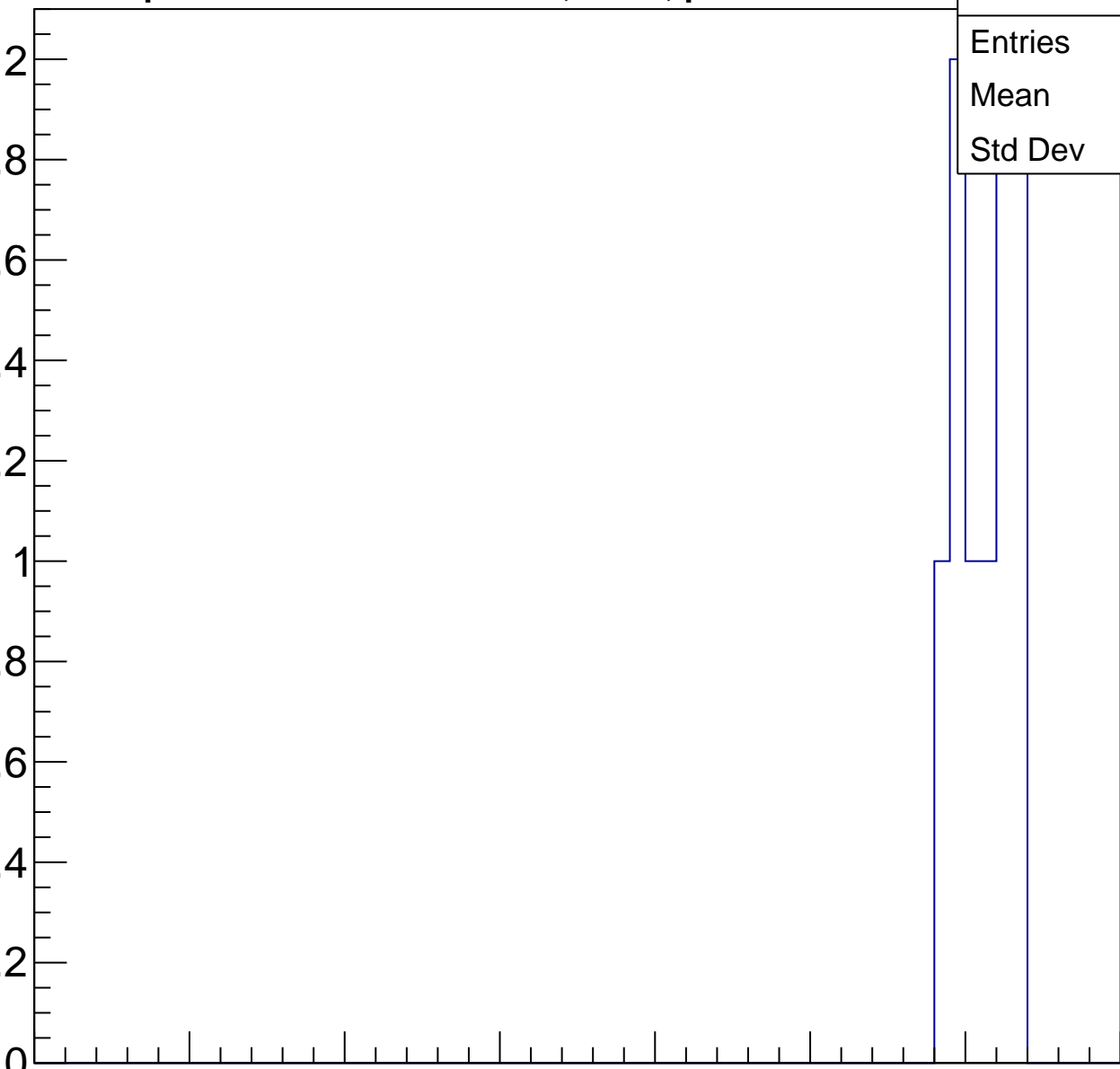
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	9
Mean	60.78
Std Dev	1.75

0 10 20 30 40 50 60 70

ampl





# B1L103S, U26-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L103S, U26-ch86, adc0

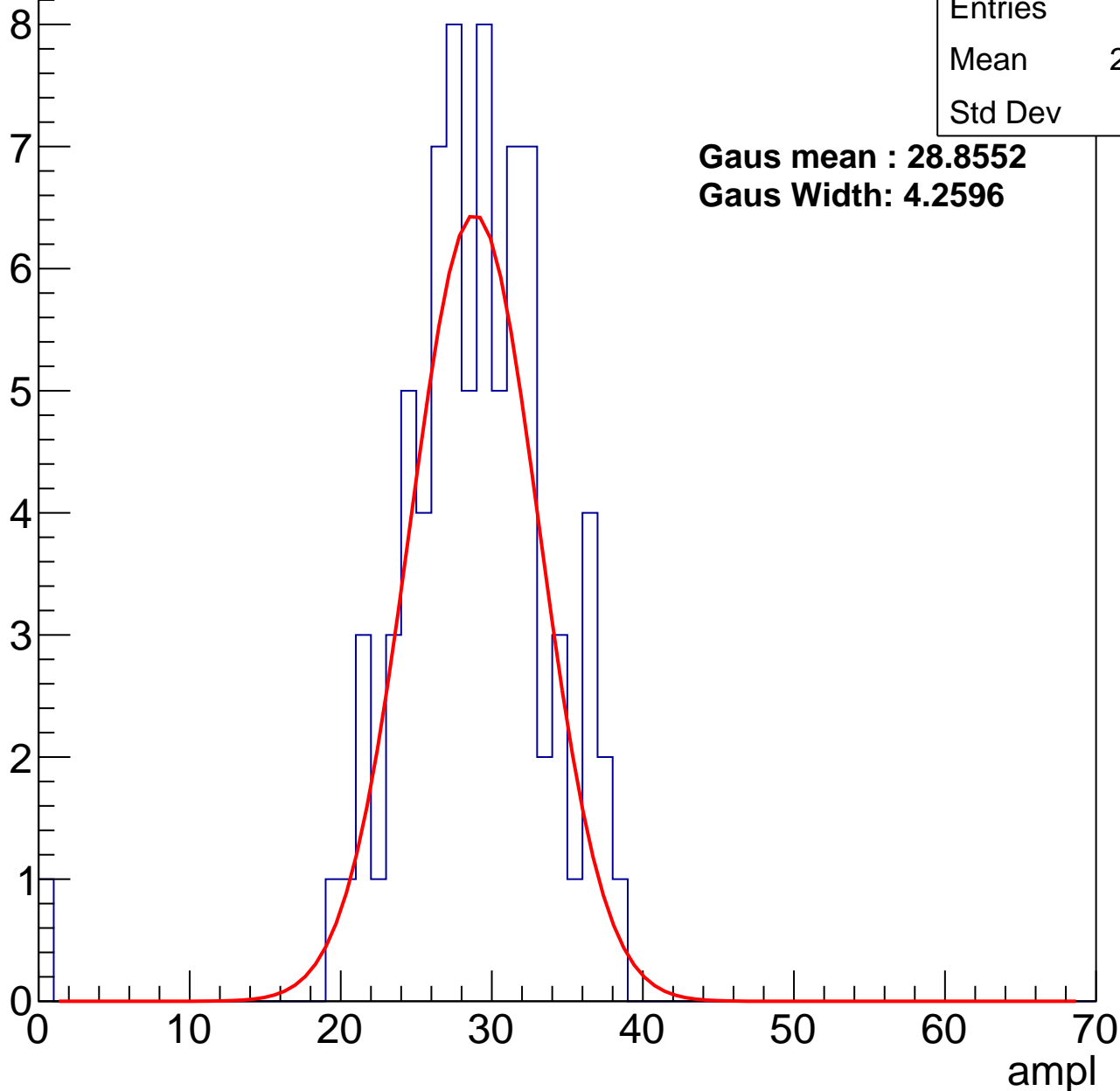
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	79
Mean	28.27
Std Dev	5.35

**Gaus mean : 28.8552**

**Gaus Width: 4.2596**



# B1L103S, U26-ch86, adc1

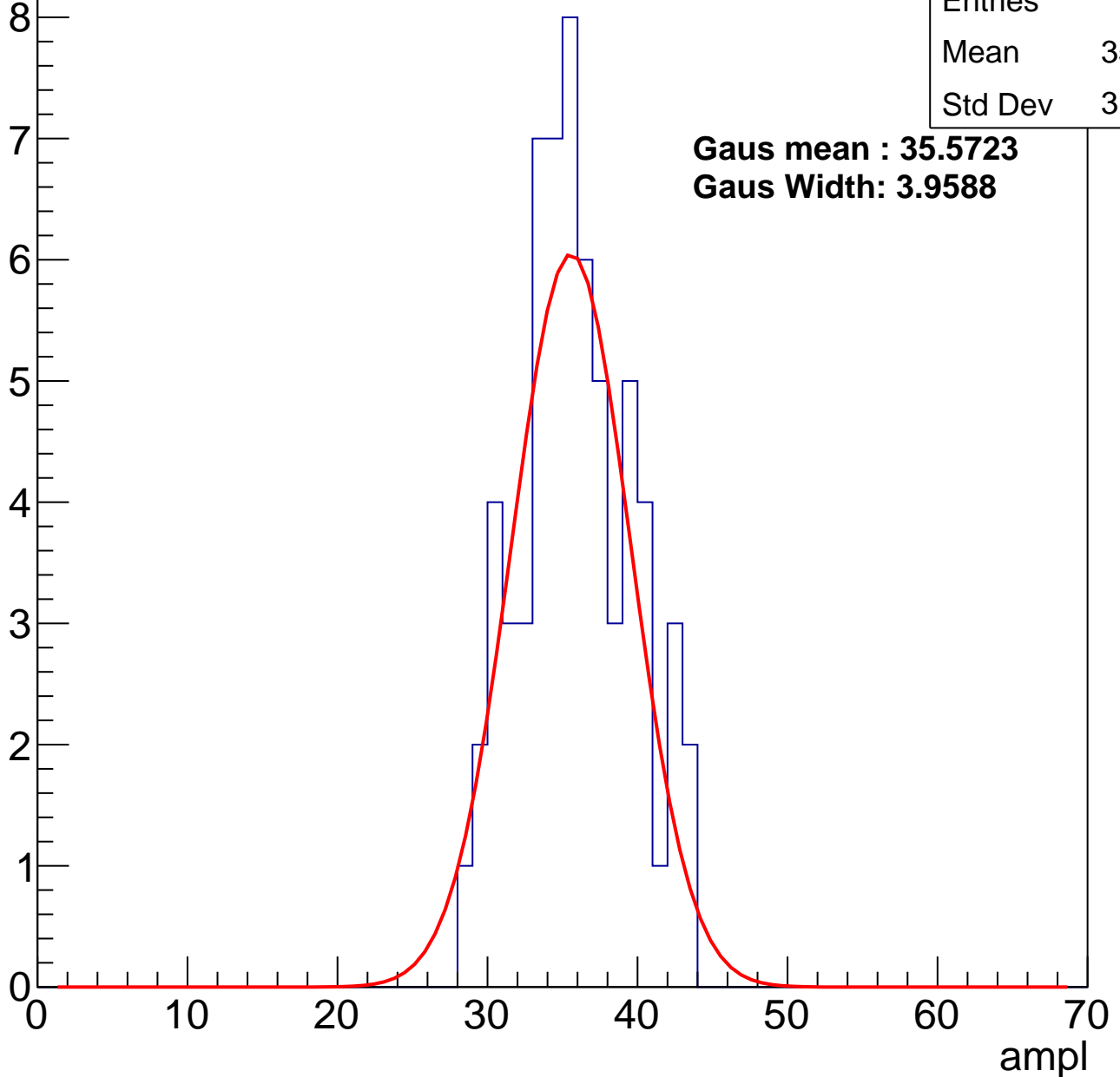
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	35.42
Std Dev	3.673

**Gaus mean : 35.5723**

**Gaus Width: 3.9588**



# B1L103S, U26-ch86, adc2

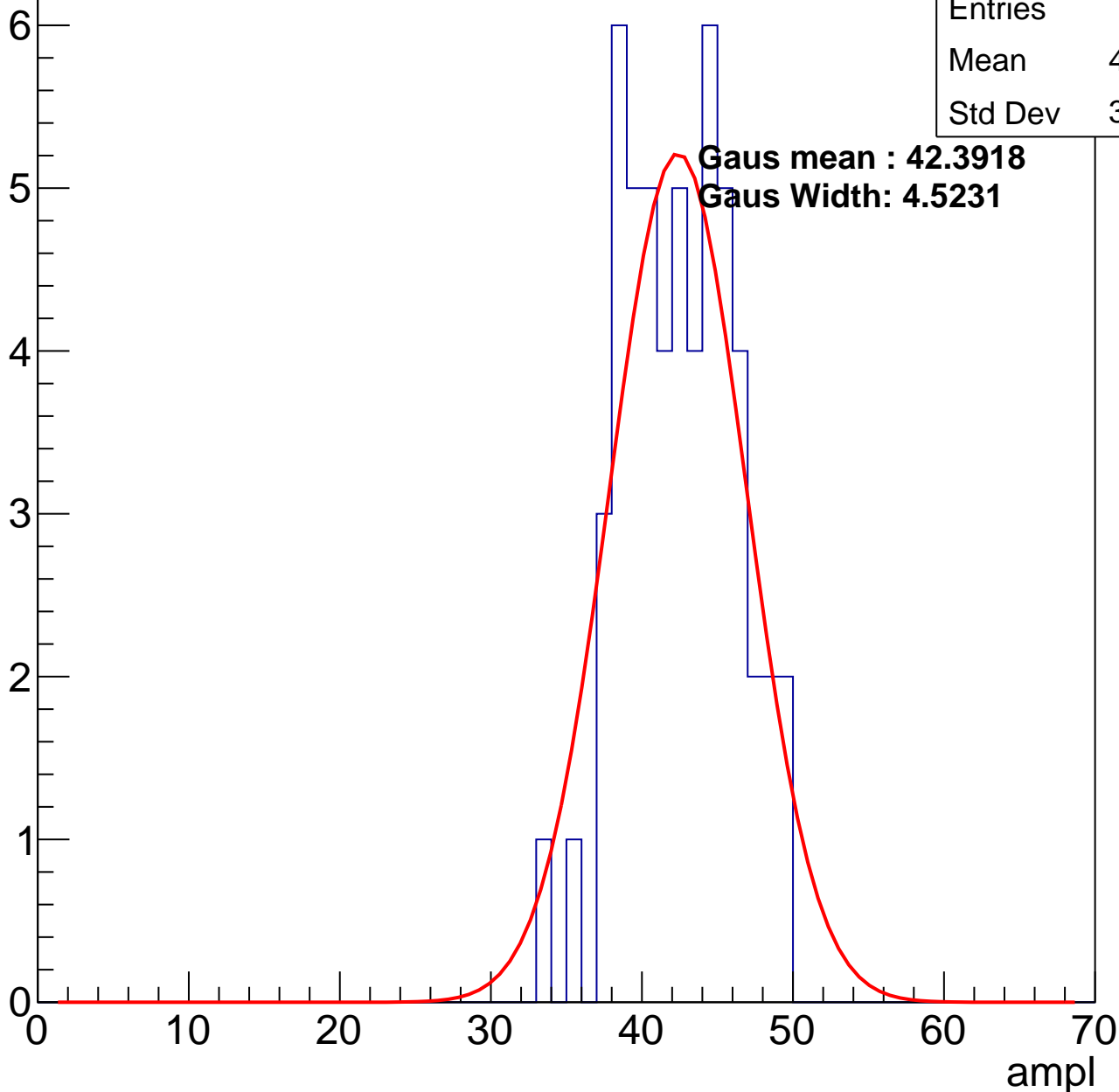
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	41.98
Std Dev	3.636

**Gaus mean : 42.3918**

**Gaus Width: 4.5231**

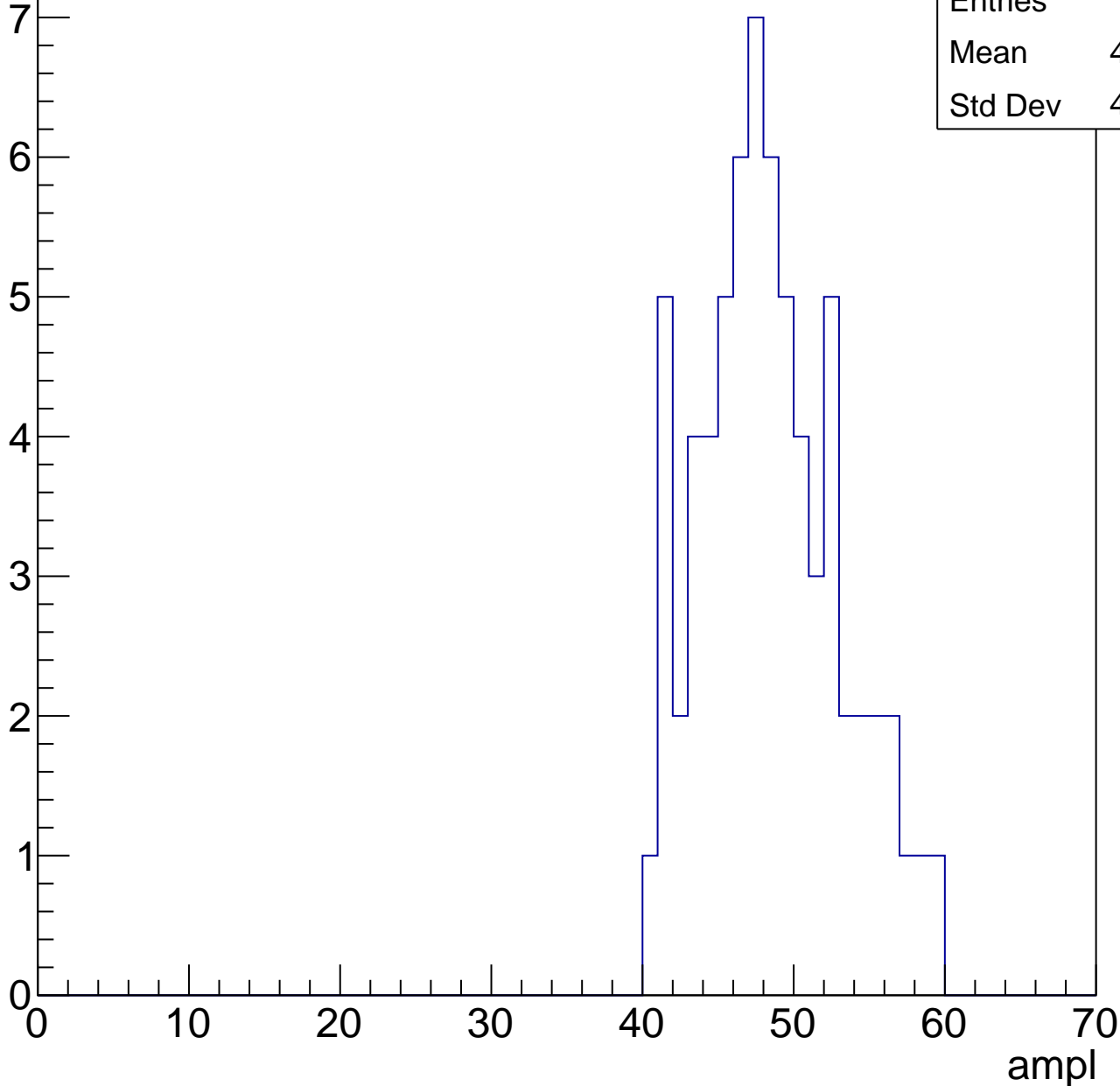


# B1L103S, U26-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

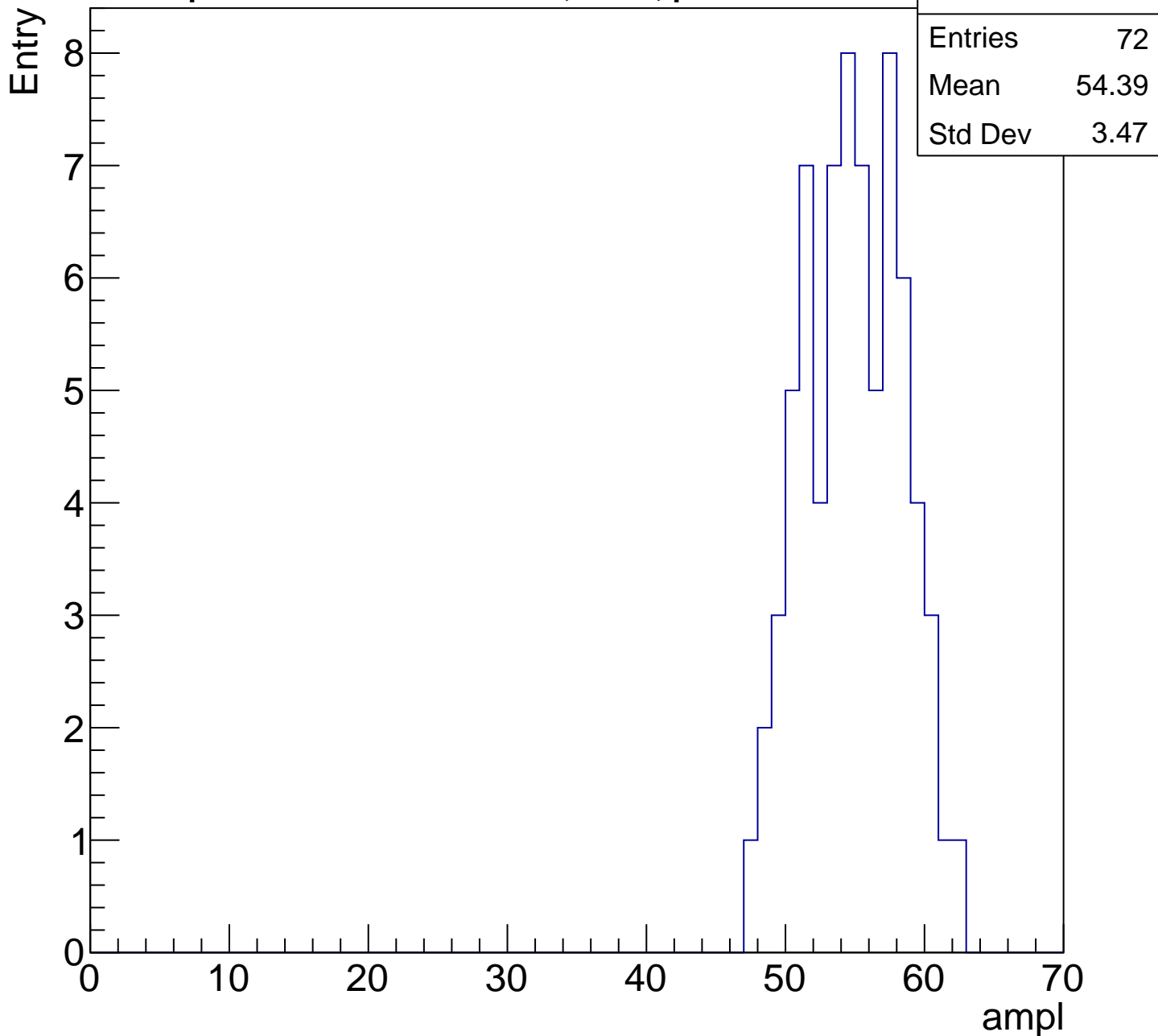
Entry

Entries	68
Mean	47.99
Std Dev	4.536



# B1L103S, U26-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

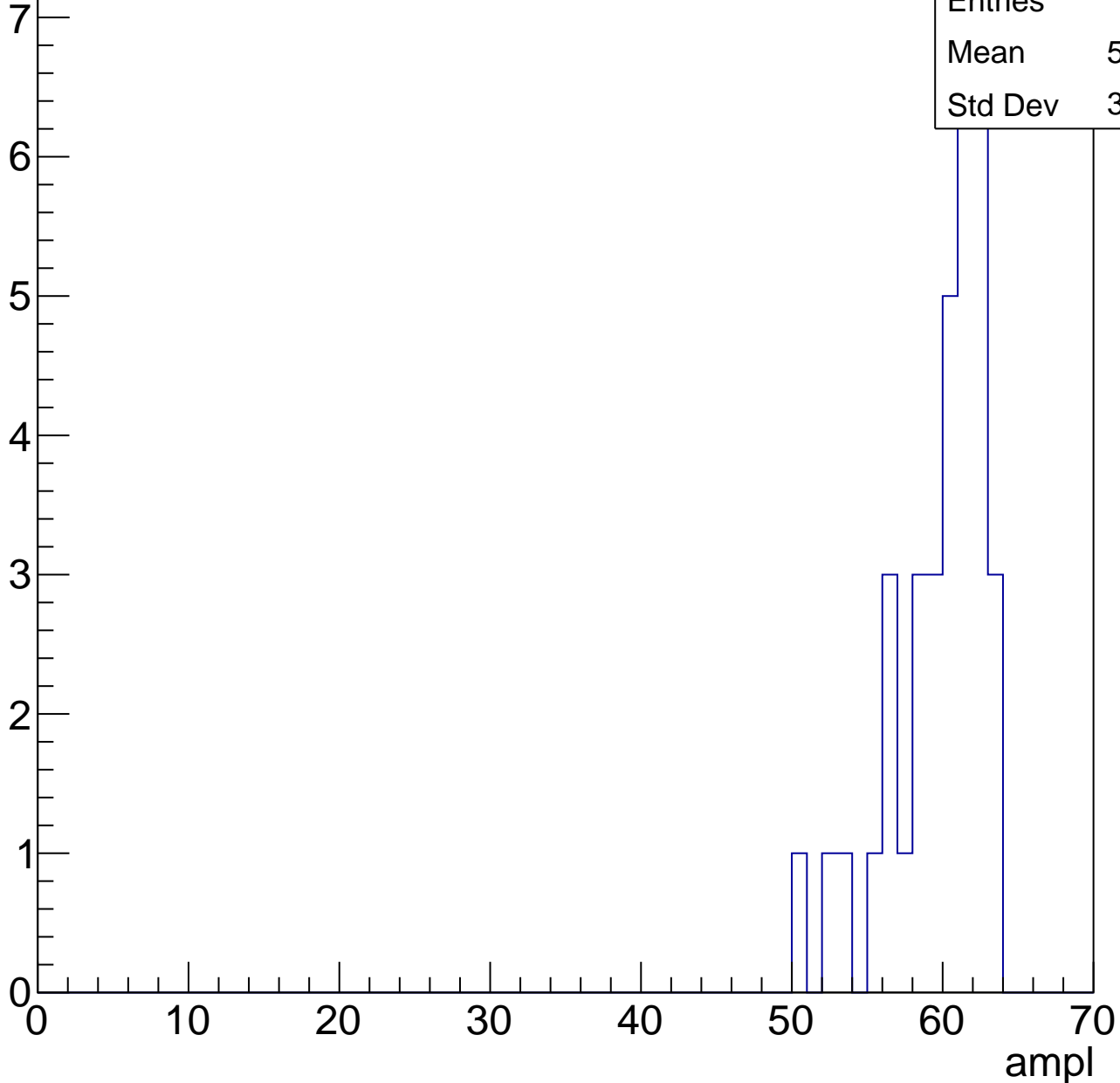


# B1L103S, U26-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	36
Mean	59.33
Std Dev	3.145

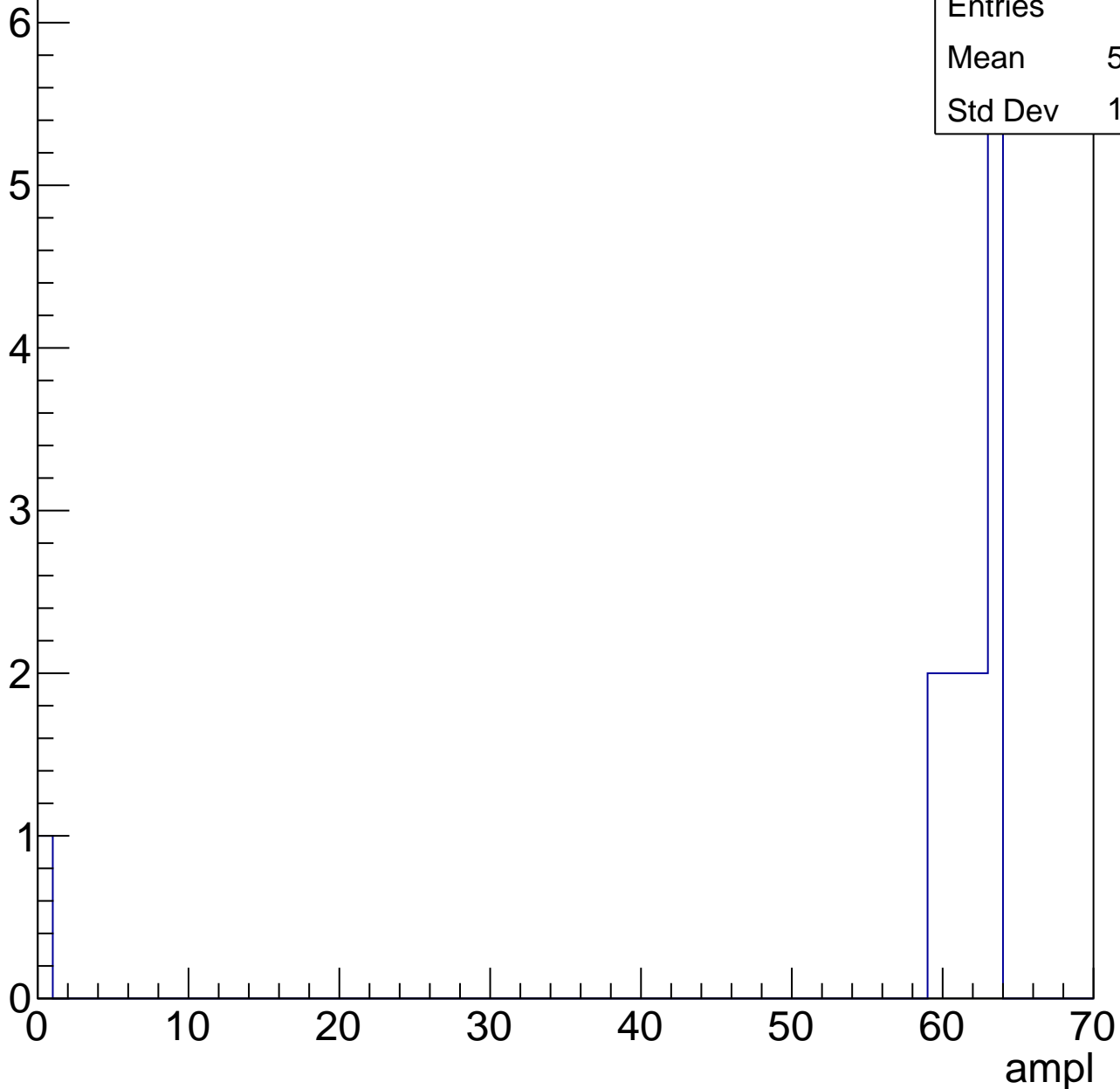


# B1L103S, U26-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	15
Mean	57.47
Std Dev	15.43





# B1L103S, U26-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch87, adc0

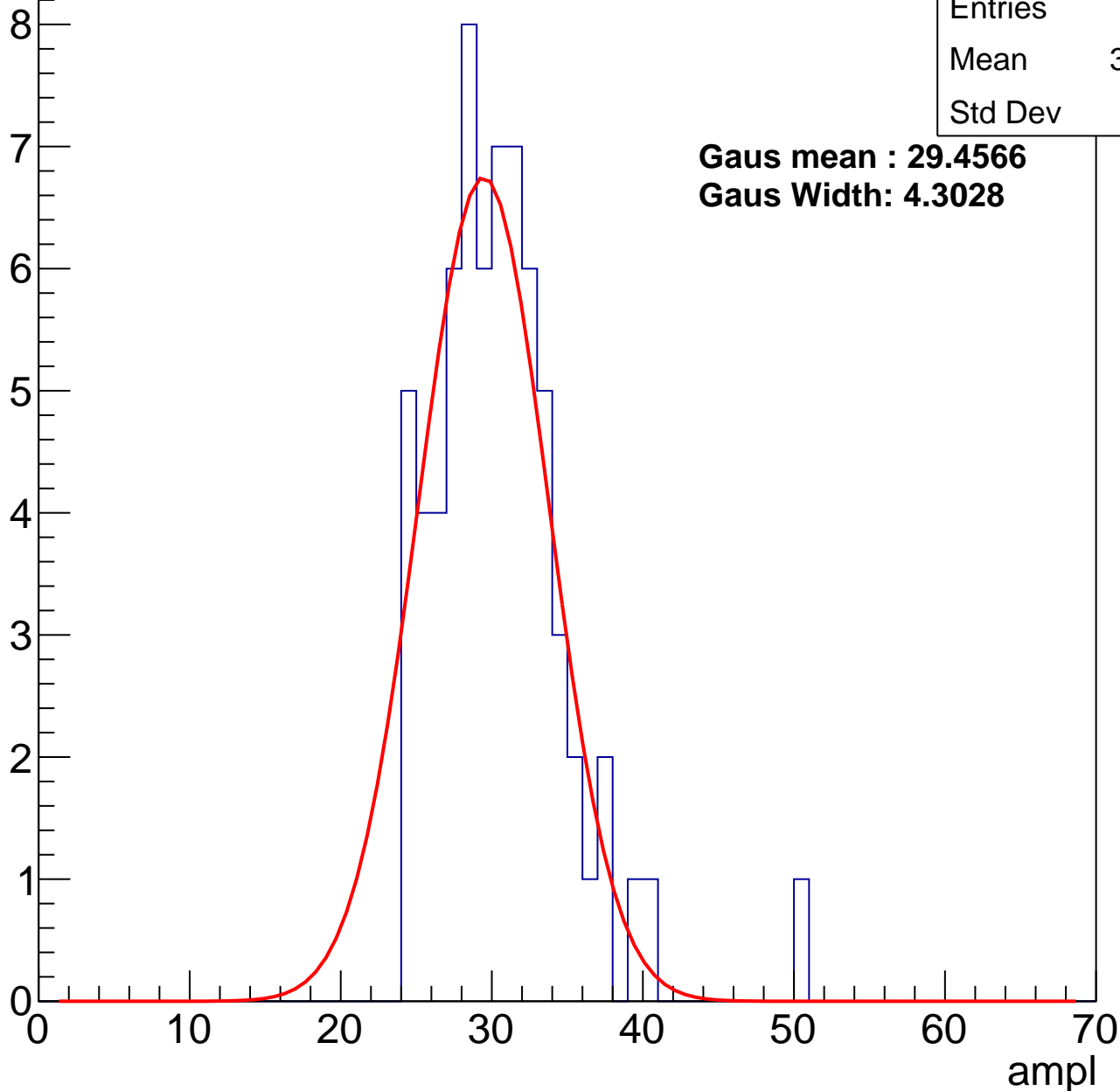
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	30.13
Std Dev	4.38

**Gaus mean : 29.4566**

**Gaus Width: 4.3028**



# B1L103S, U26-ch87, adc1

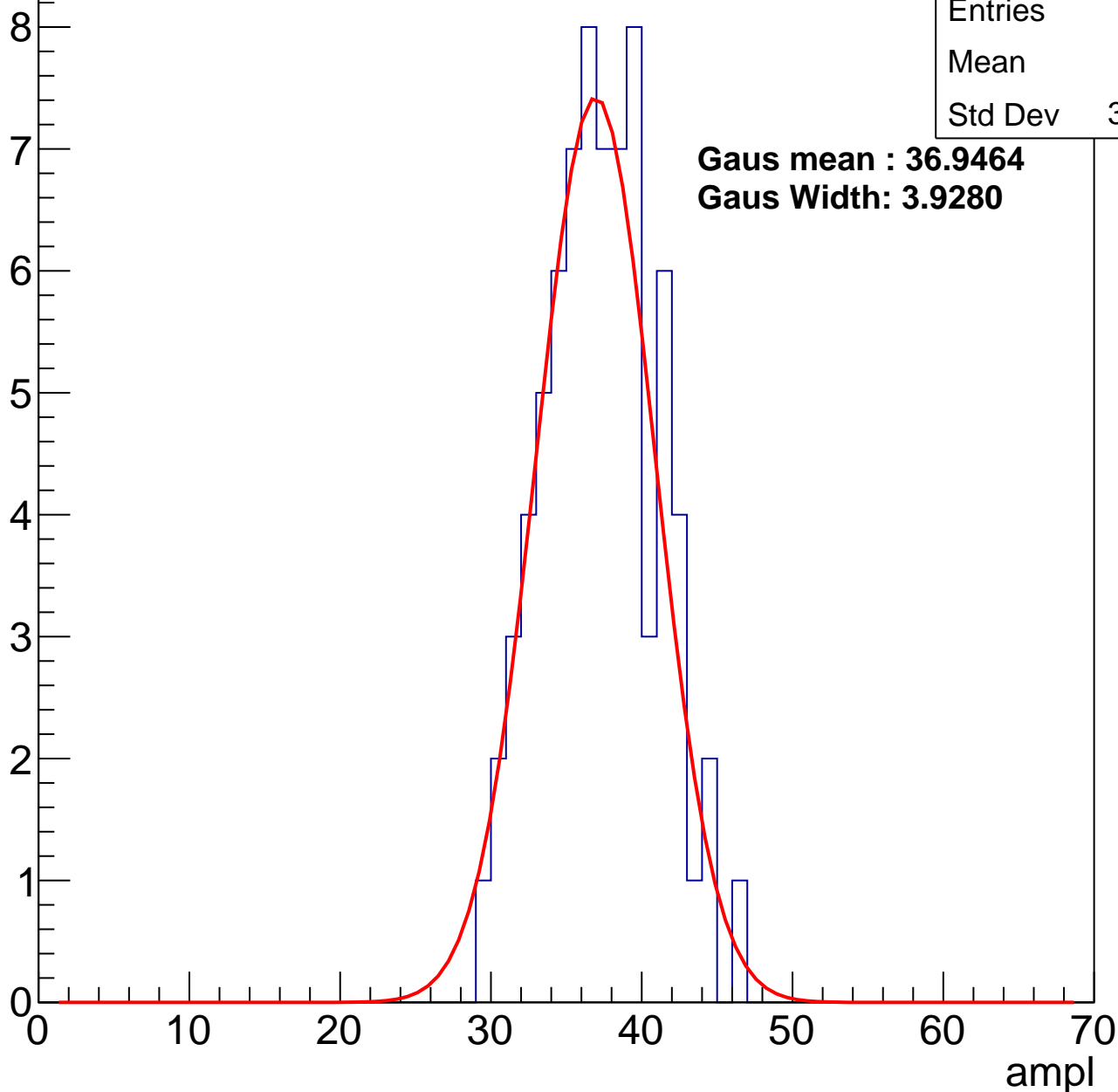
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	36.8
Std Dev	3.677

**Gaus mean : 36.9464**

**Gaus Width: 3.9280**



# B1L103S, U26-ch87, adc2

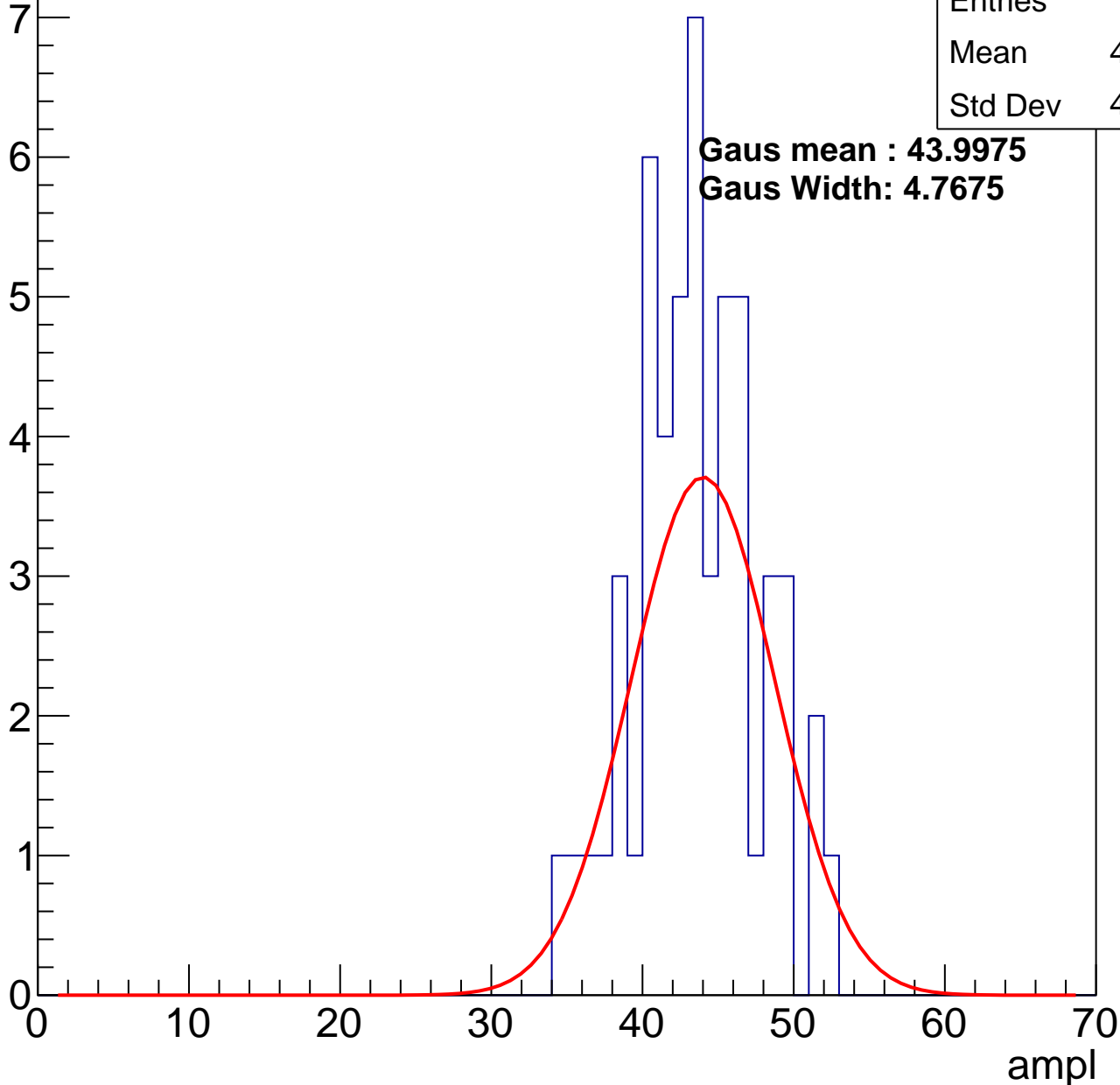
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	43.19
Std Dev	4.052

**Gaus mean : 43.9975**

**Gaus Width: 4.7675**

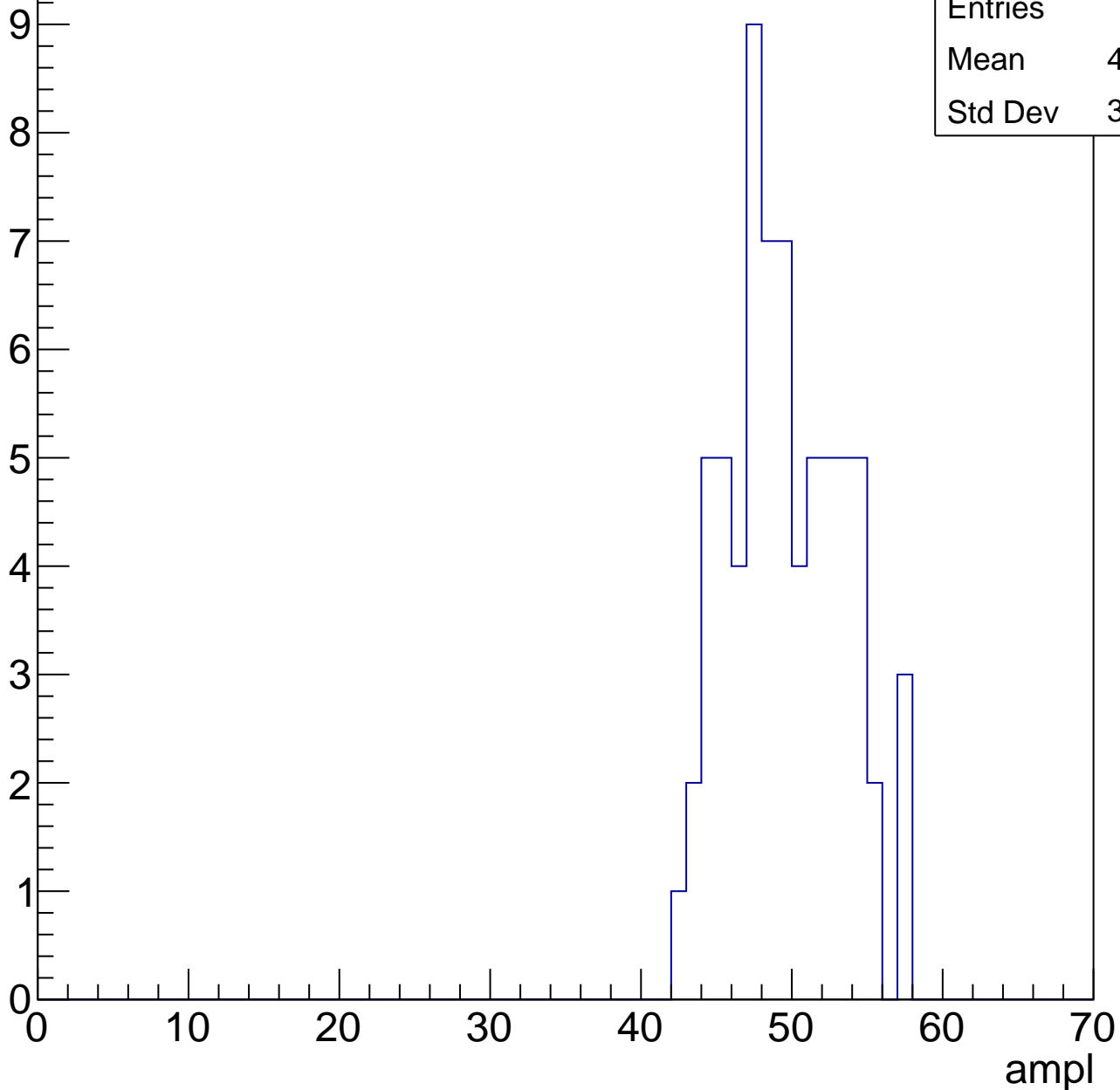


# B1L103S, U26-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	49.13
Std Dev	3.695

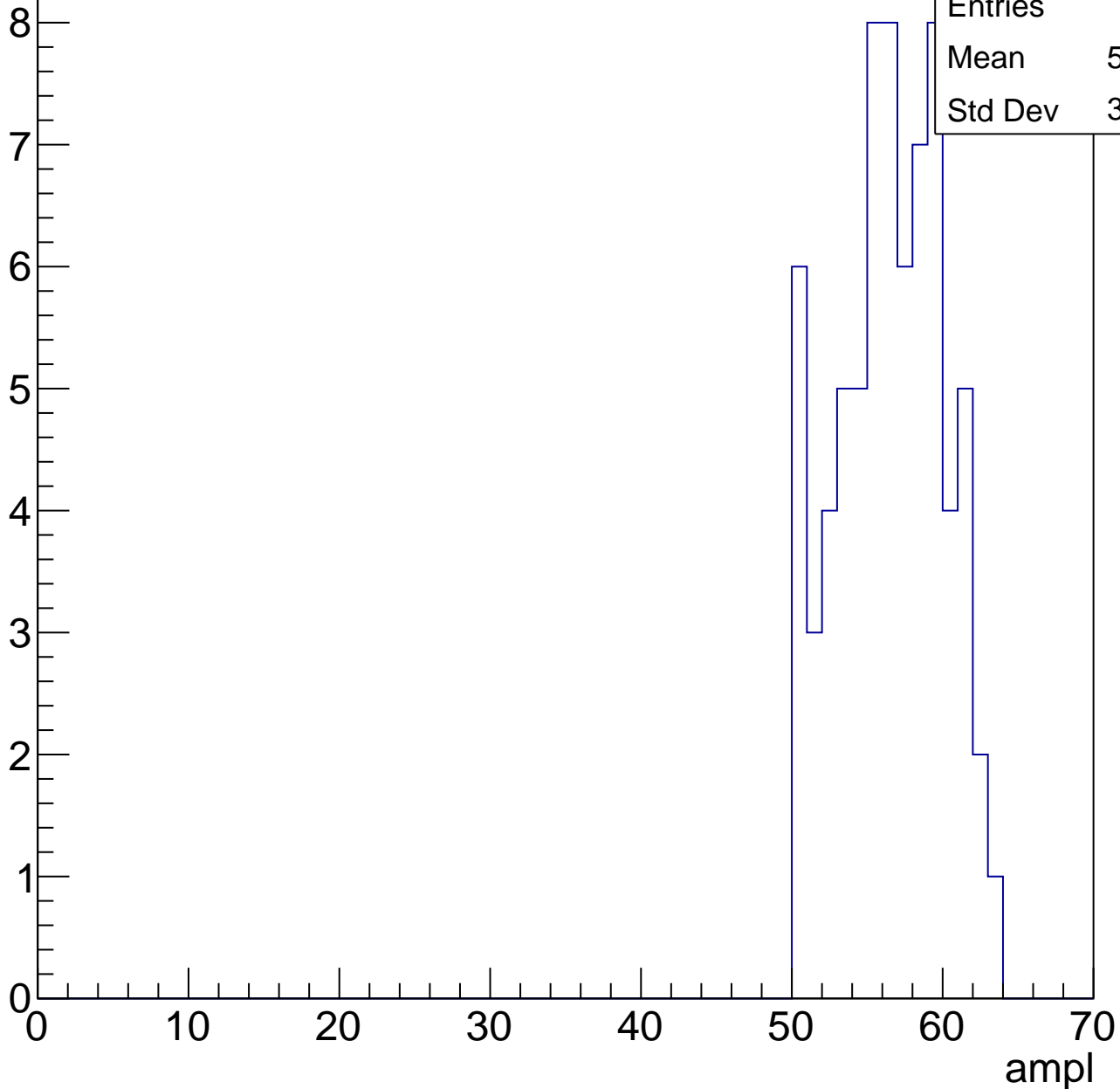


# B1L103S, U26-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	56.06
Std Dev	3.423

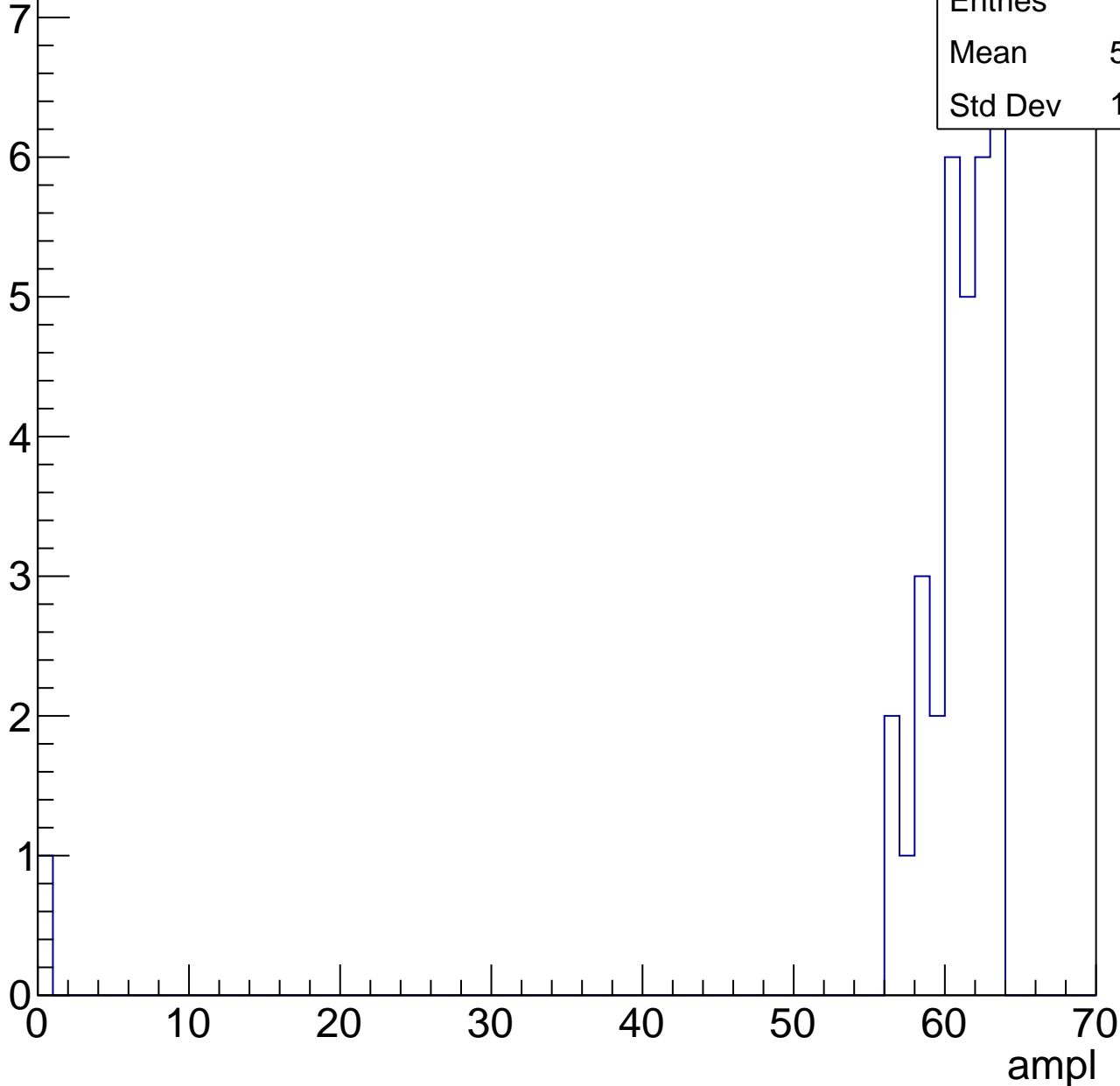


# B1L103S, U26-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	33
Mean	58.76
Std Dev	10.58



# B1L103S, U26-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U26-ch88, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	77
Mean	27.73
Std Dev	5.096

**Gaus mean : 29.1693**

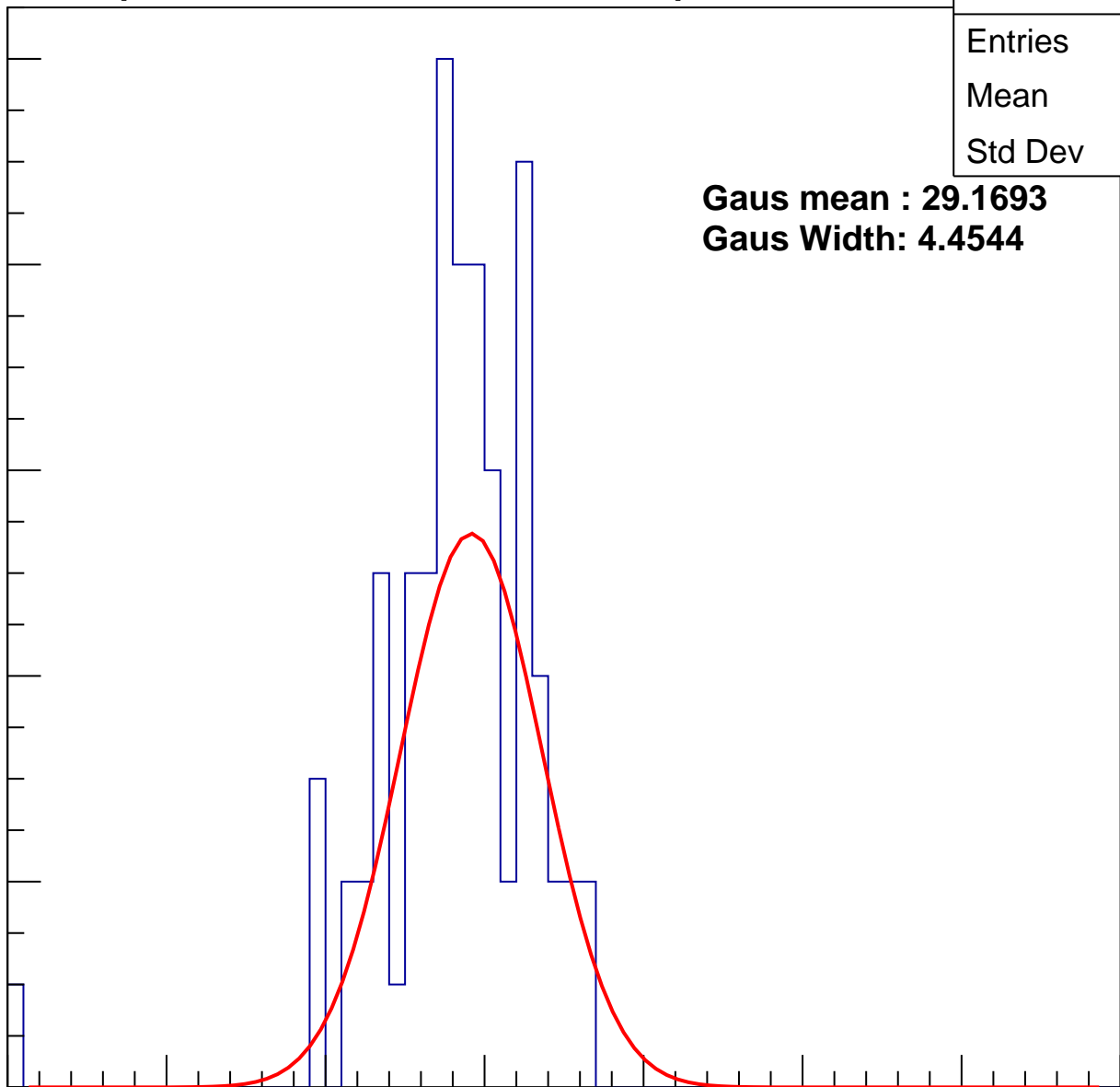
**Gaus Width: 4.4544**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch88, adc1

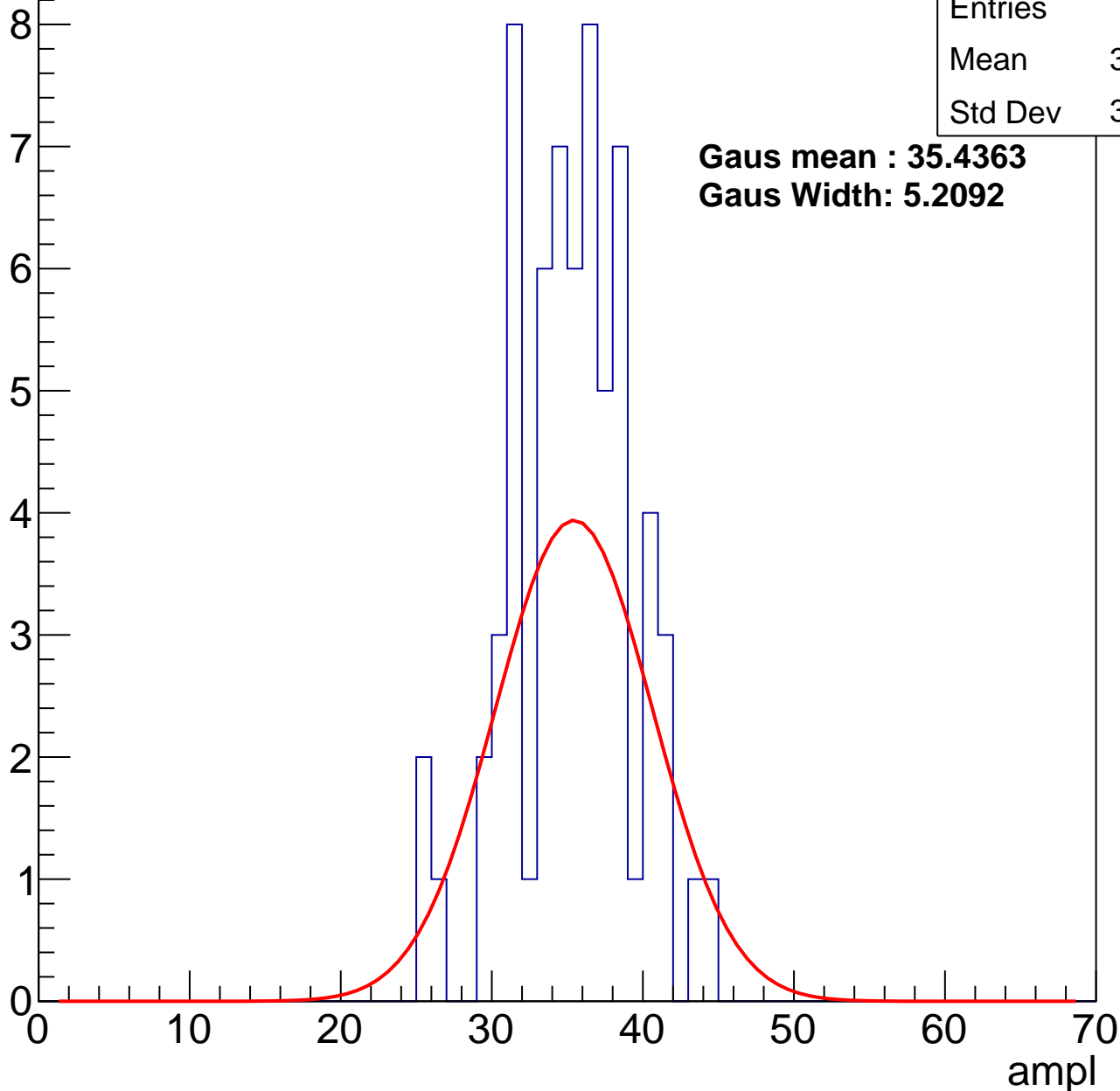
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	34.82
Std Dev	3.996

**Gaus mean : 35.4363**

**Gaus Width: 5.2092**



# B1L103S, U26-ch88, adc2

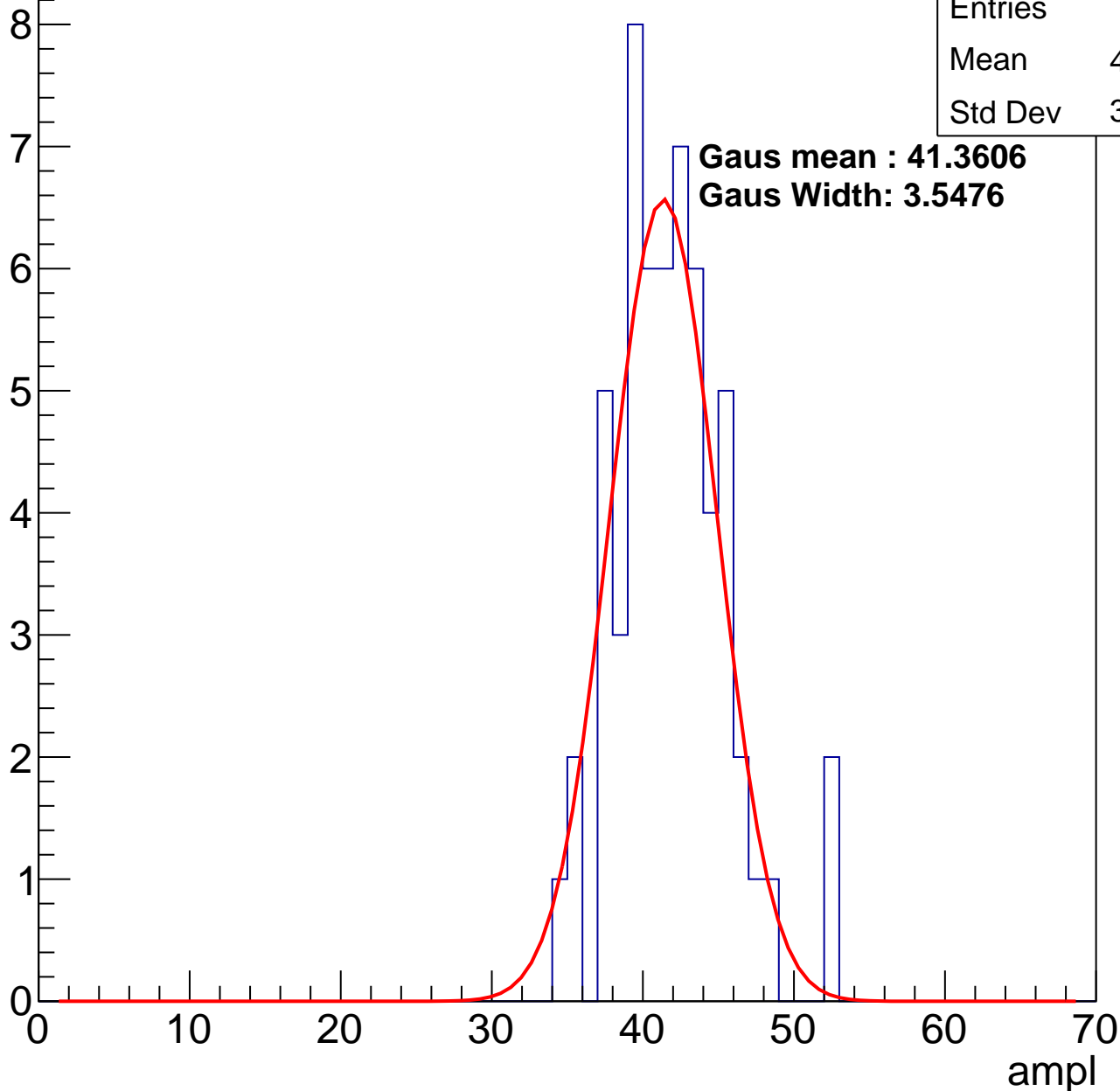
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	41.44
Std Dev	3.633

**Gaus mean : 41.3606**

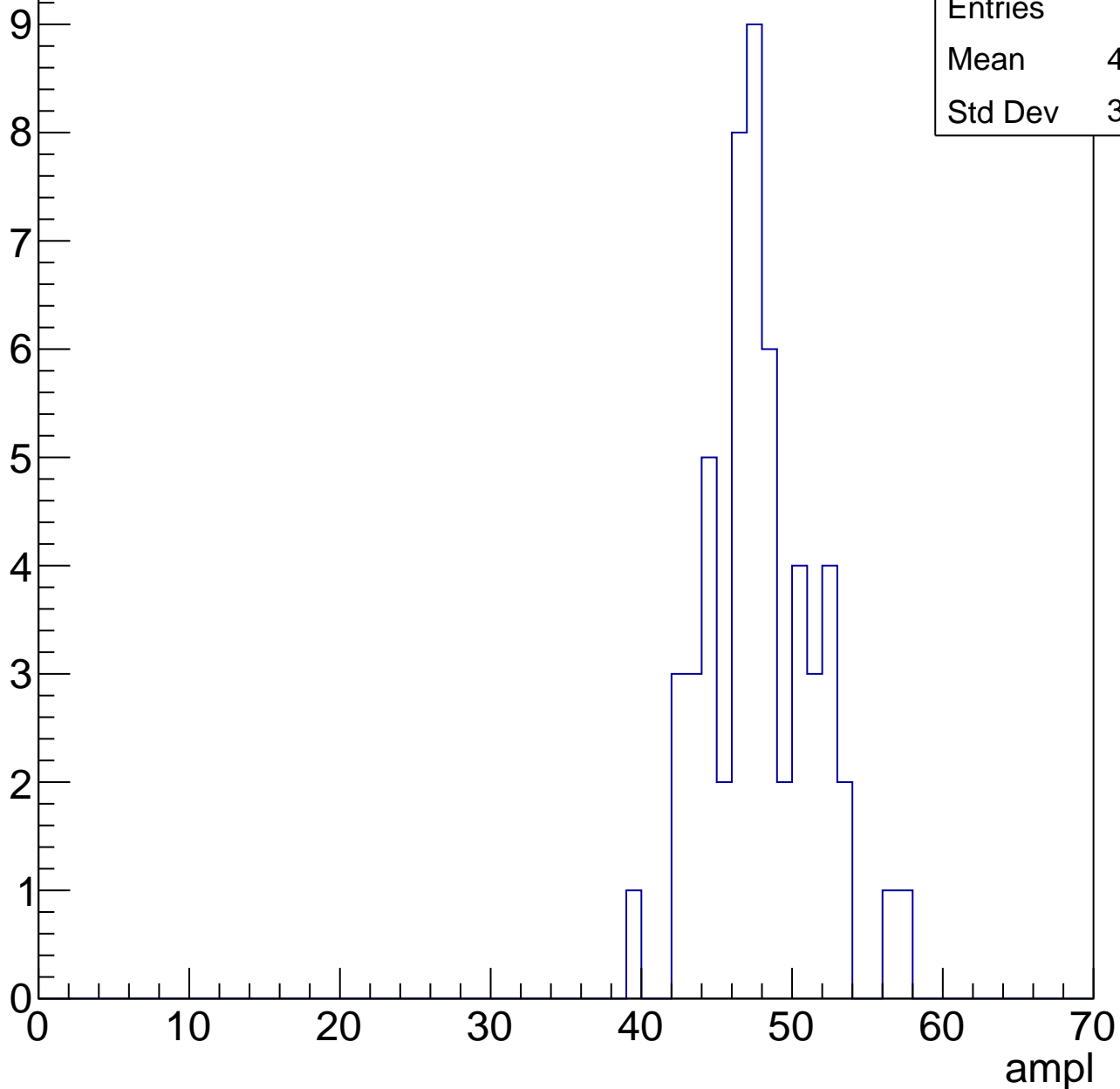
**Gaus Width: 3.5476**



# B1L103S, U26-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

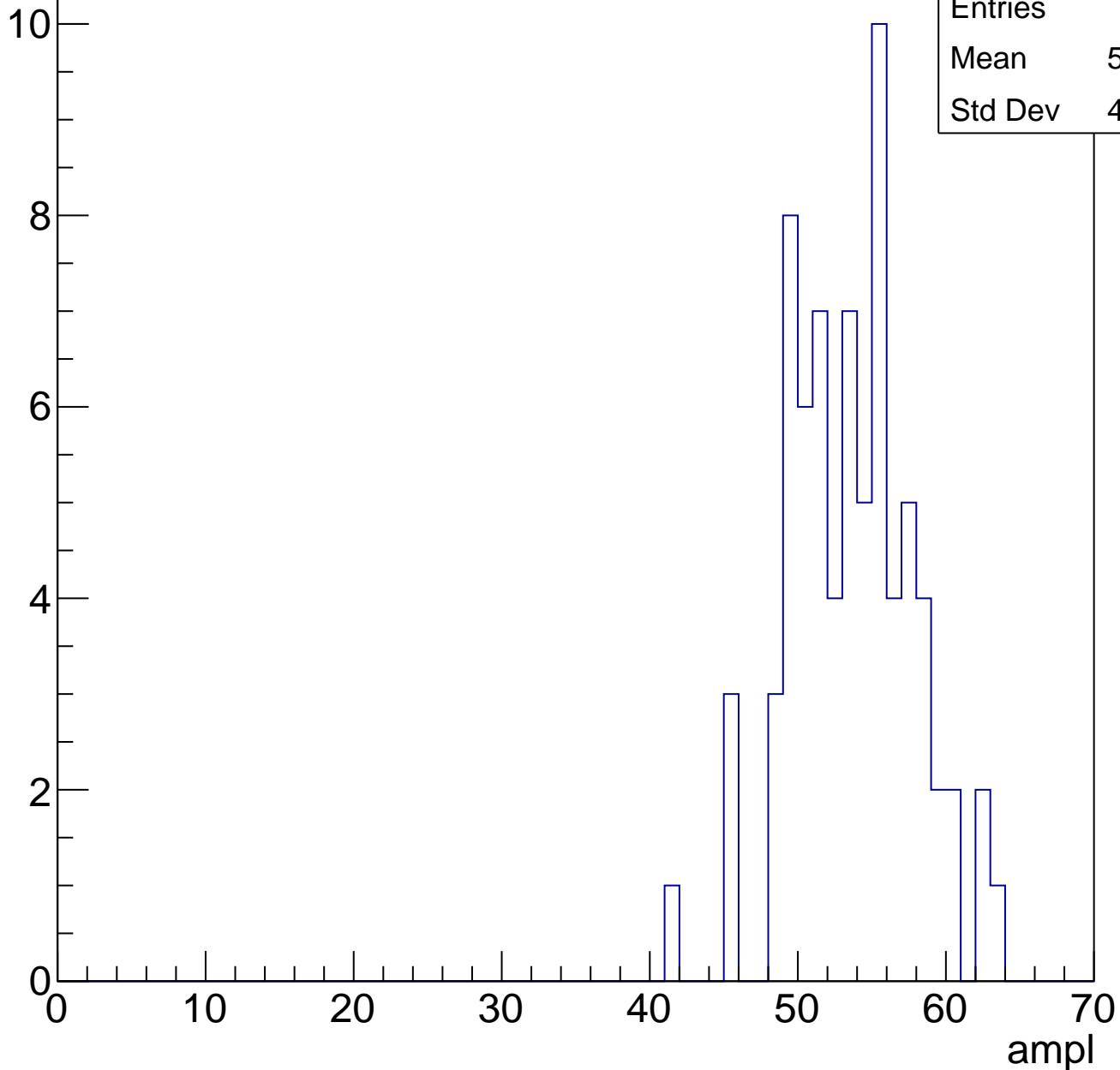


# B1L103S, U26-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	74
Mean	53.16
Std Dev	4.217

Entry



# B1L103S, U26-ch88, adc5

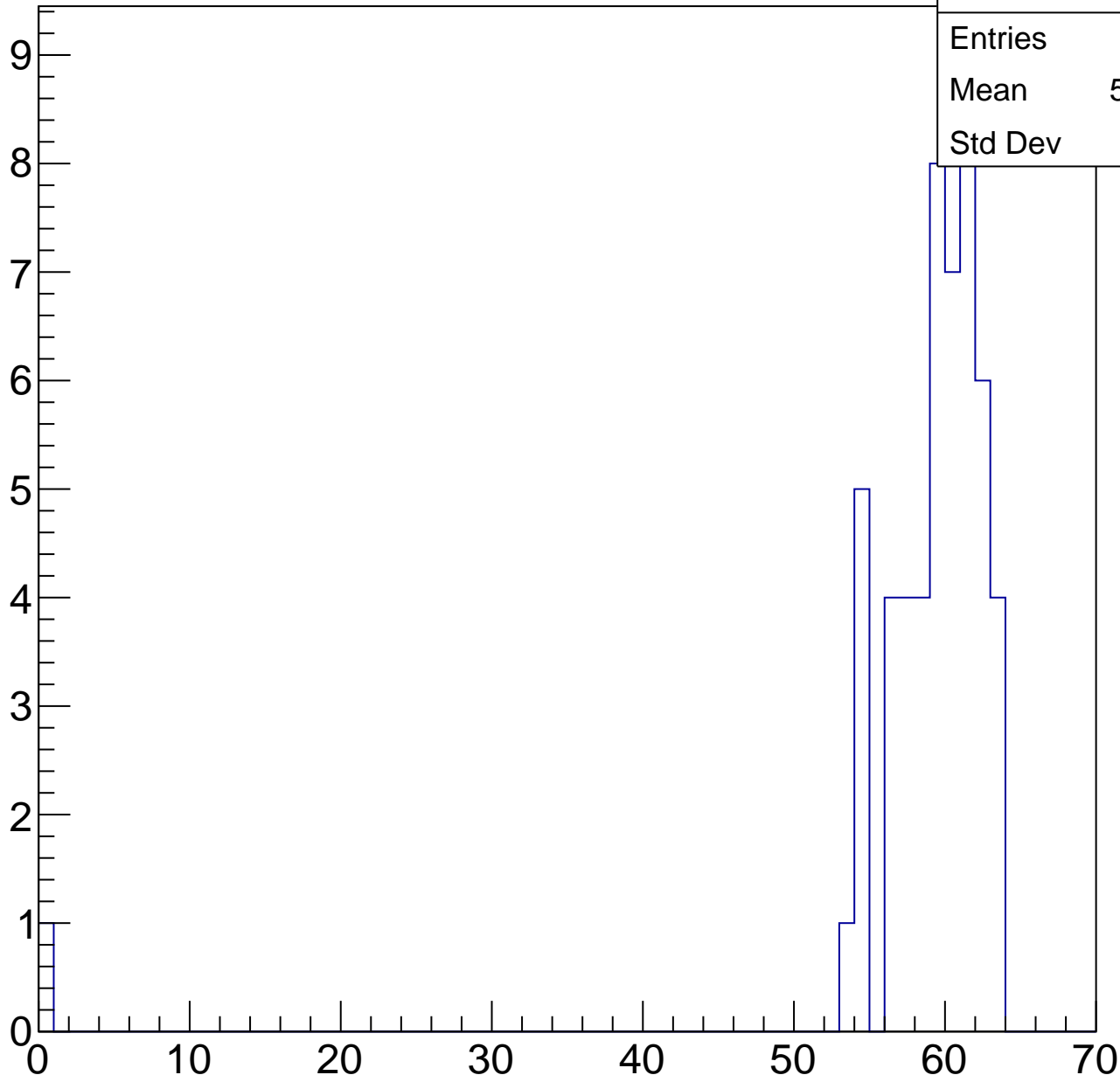
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	53
Mean	57.96
Std Dev	8.47

ampl

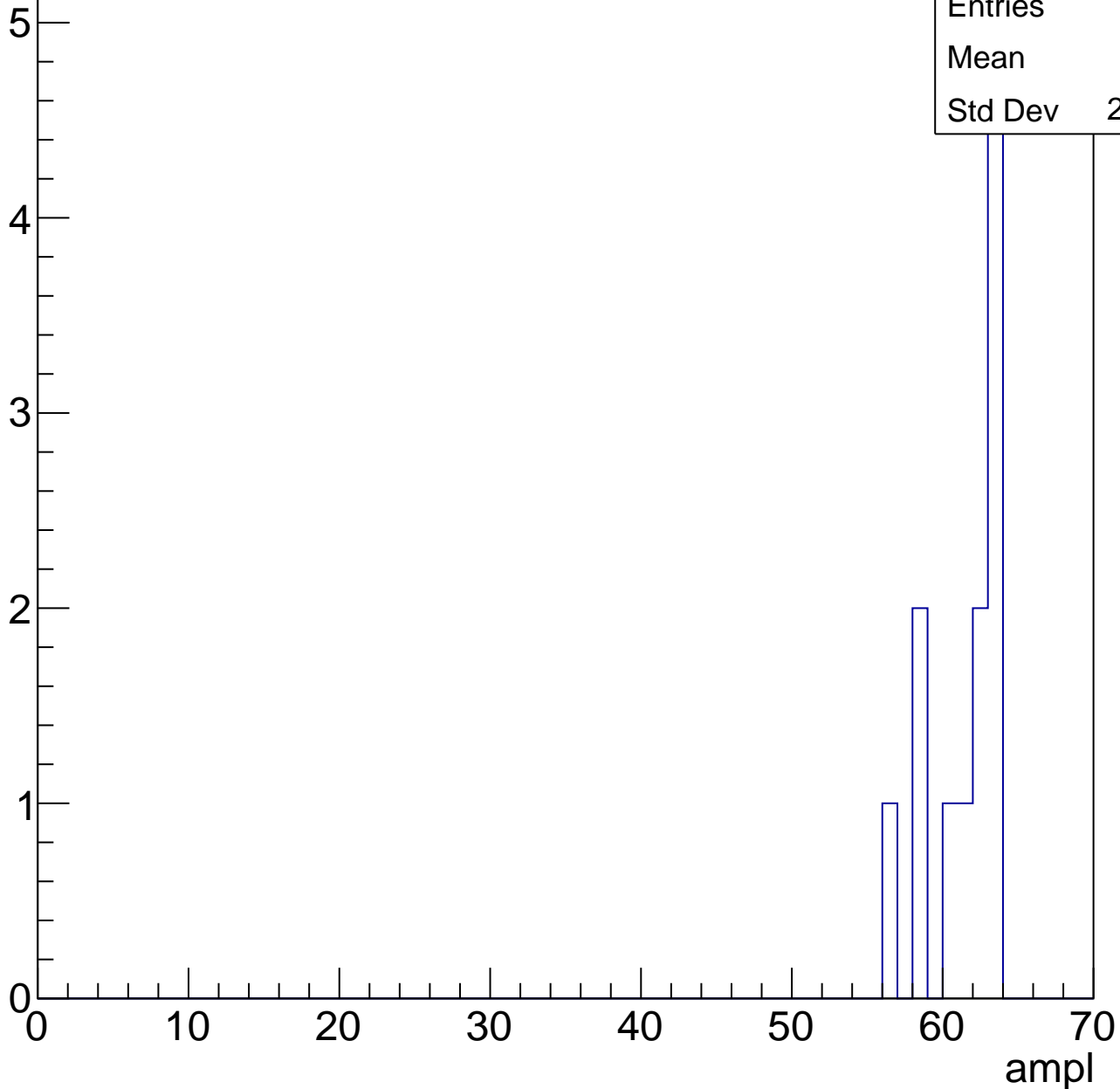


# B1L103S, U26-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	12
Mean	61
Std Dev	2.345





# B1L103S, U26-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L103S, U26-ch89, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	67
Mean	28.85
Std Dev	3.116

**Gaus mean : 29.3201**

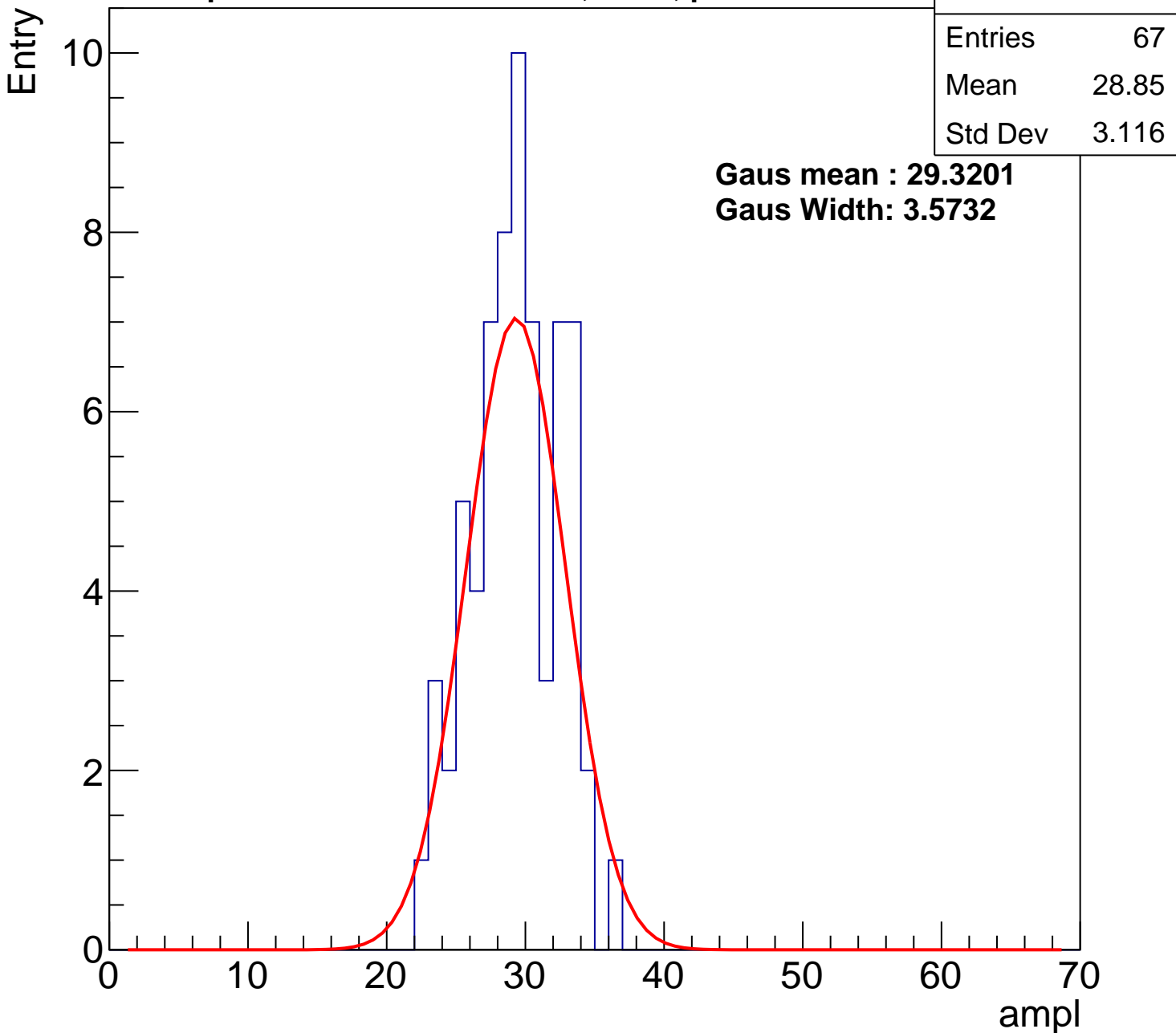
**Gaus Width: 3.5732**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



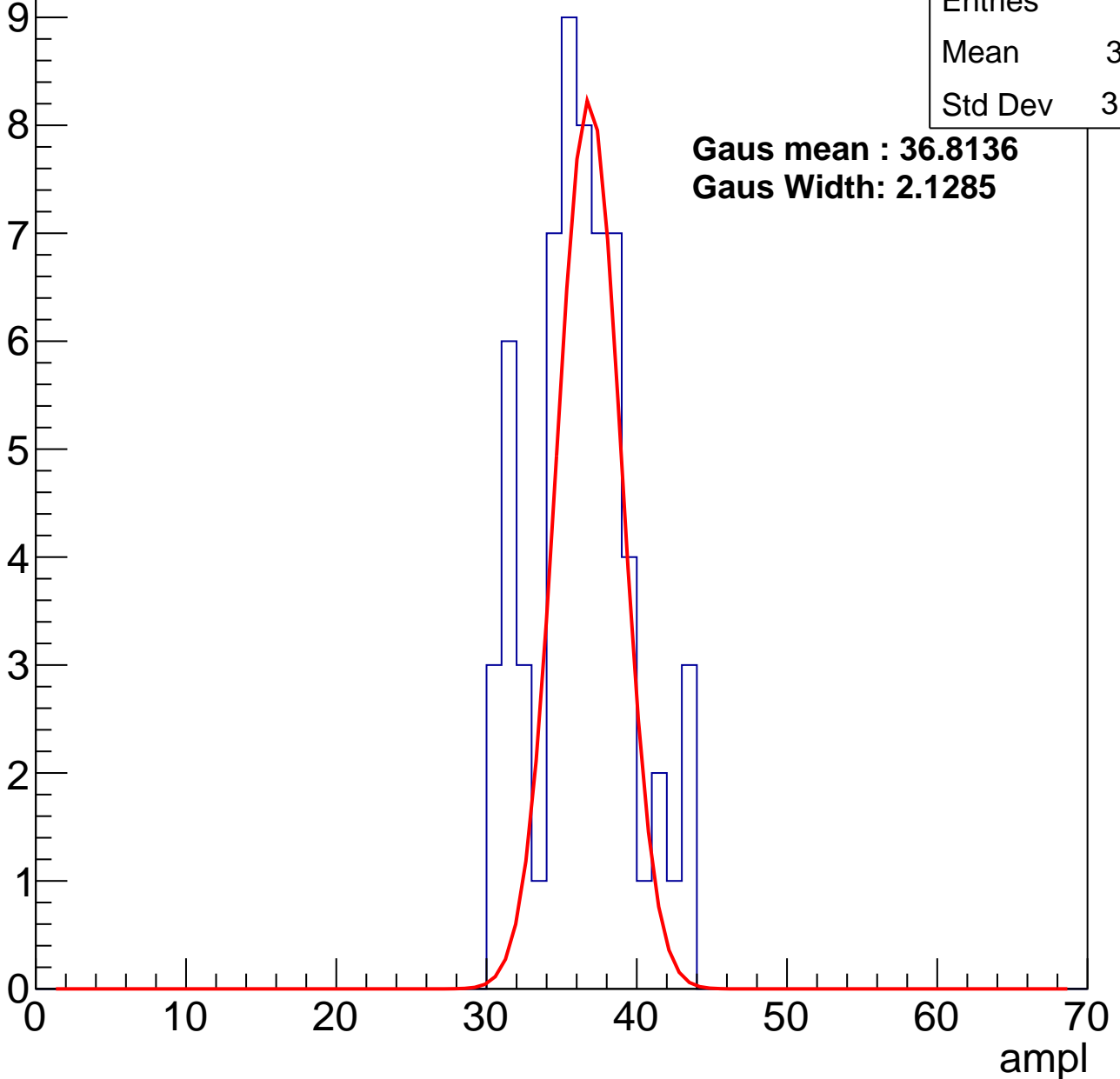
# B1L103S, U26-ch89, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	35.81
Std Dev	3.287

**Gaus mean : 36.8136**  
**Gaus Width: 2.1285**



# B1L103S, U26-ch89, adc2

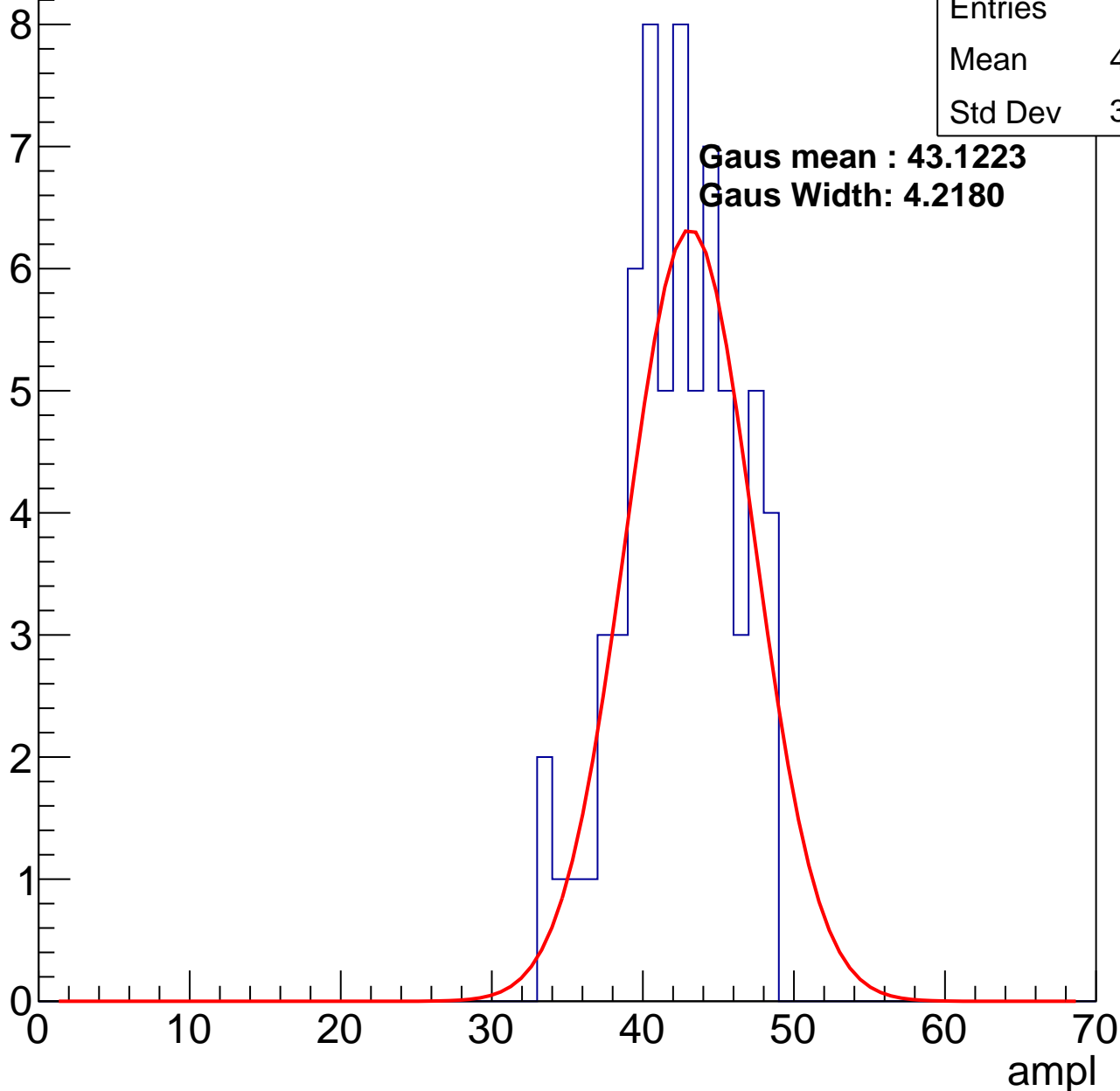
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	41.85
Std Dev	3.703

**Gaus mean : 43.1223**

**Gaus Width: 4.2180**

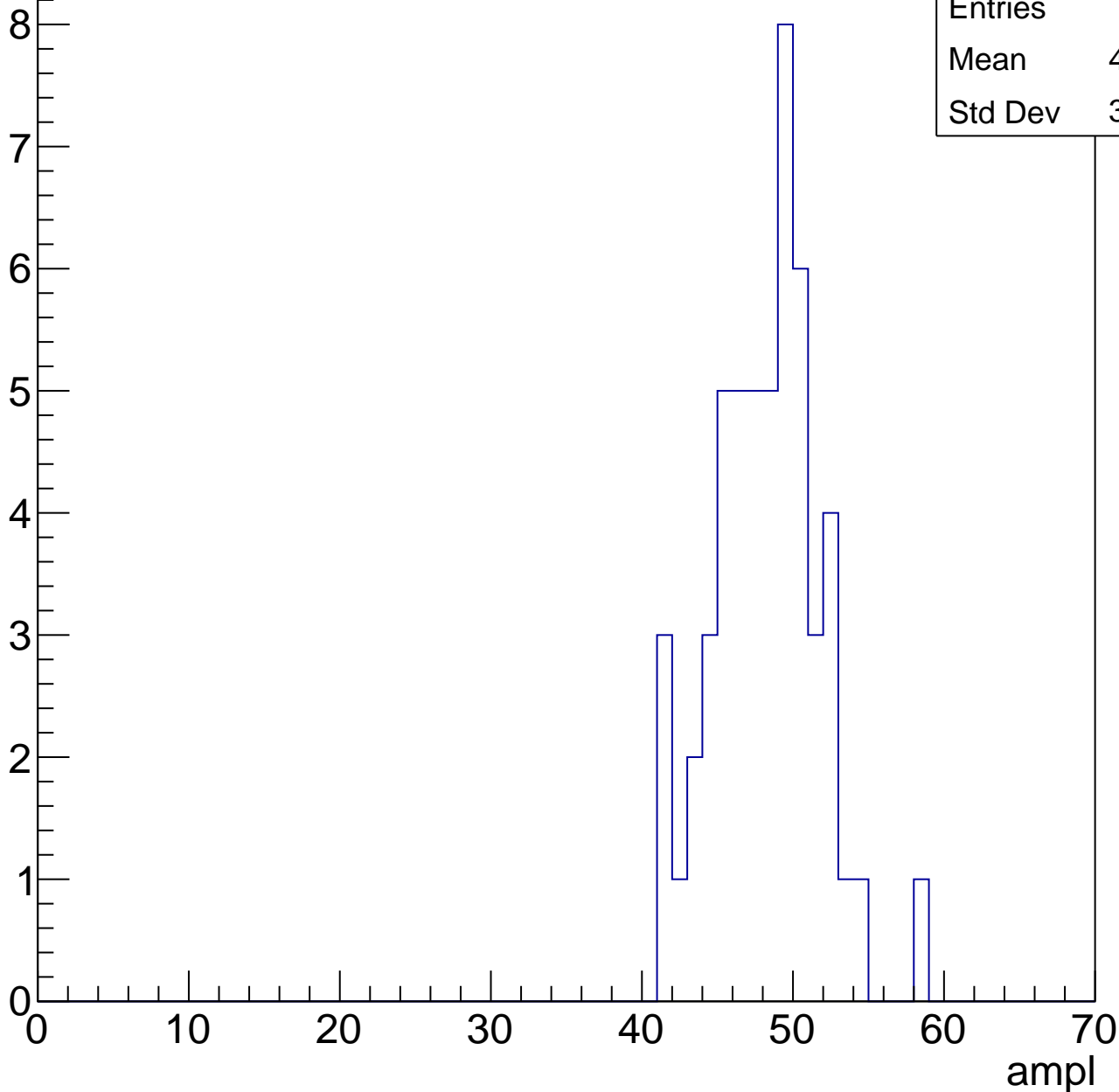


# B1L103S, U26-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

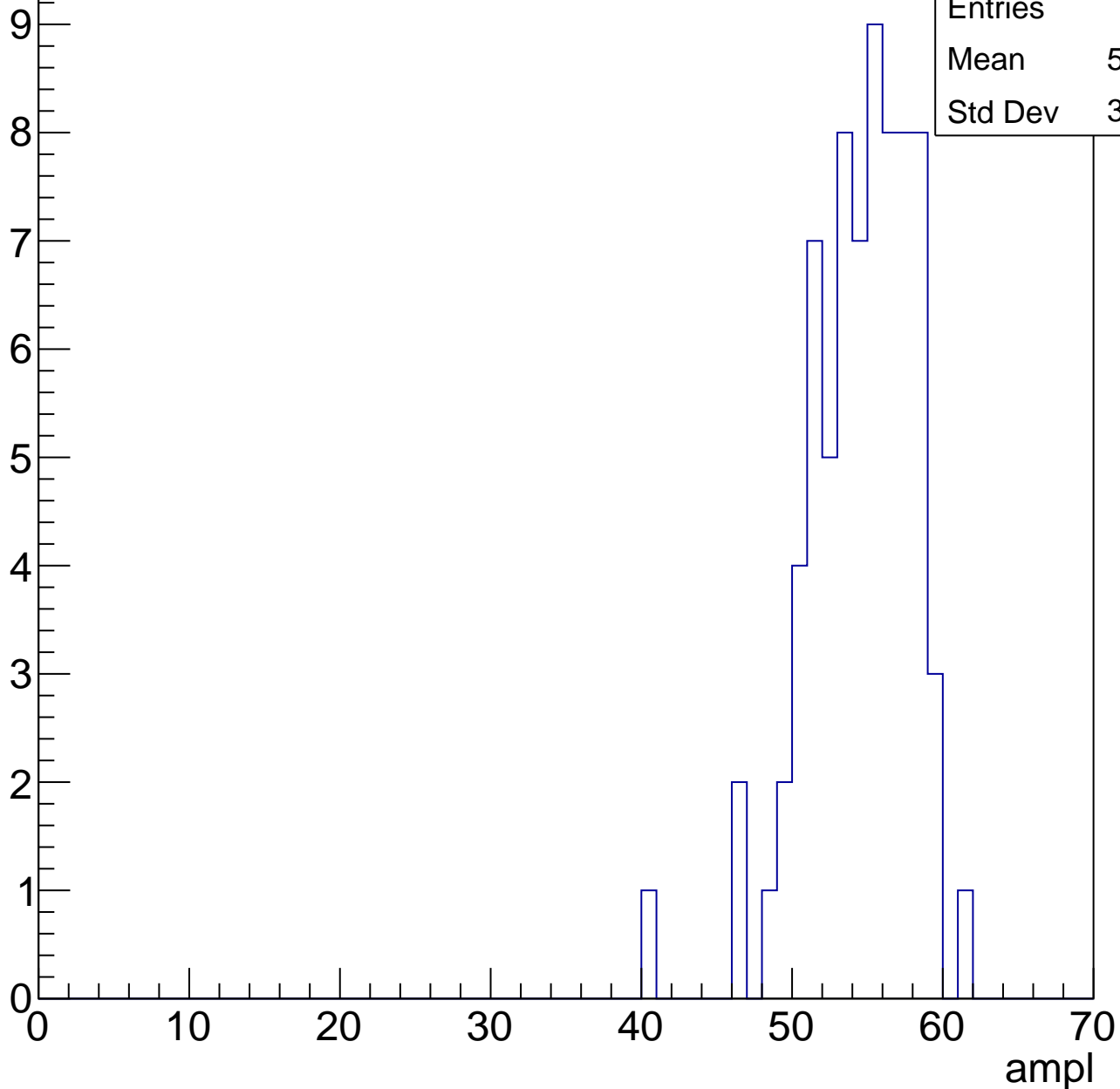
Entries	53
Mean	47.75
Std Dev	3.453



# B1L103S, U26-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

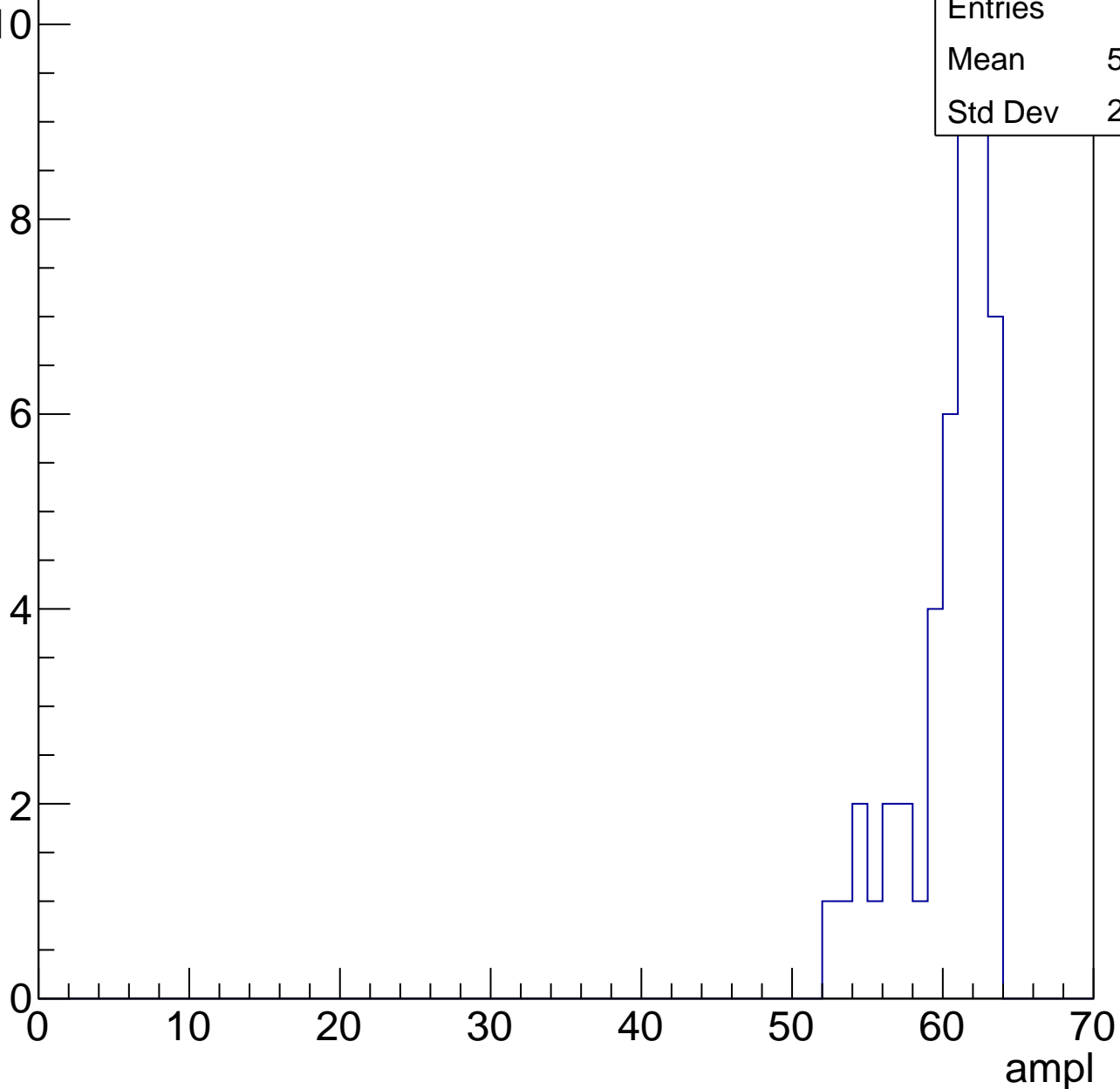


# B1L103S, U26-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

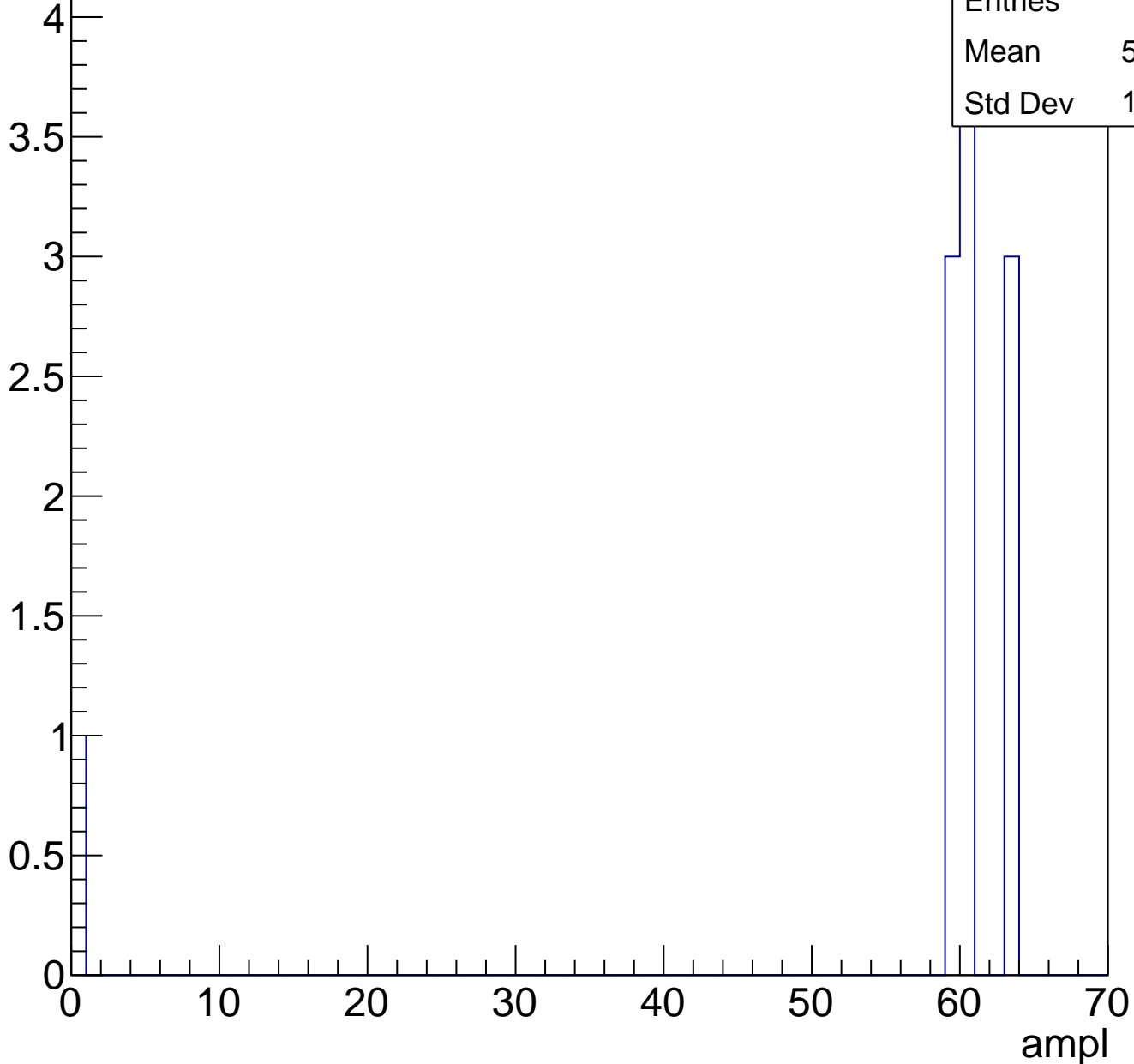
Entries	46
Mean	59.96
Std Dev	2.874



# B1L103S, U26-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	11
Mean	55.09
Std Dev	17.49



# B1L103S, U26-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U26-ch90, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	76
Mean	28.11
Std Dev	5.479

**Gaus mean : 29.4317**

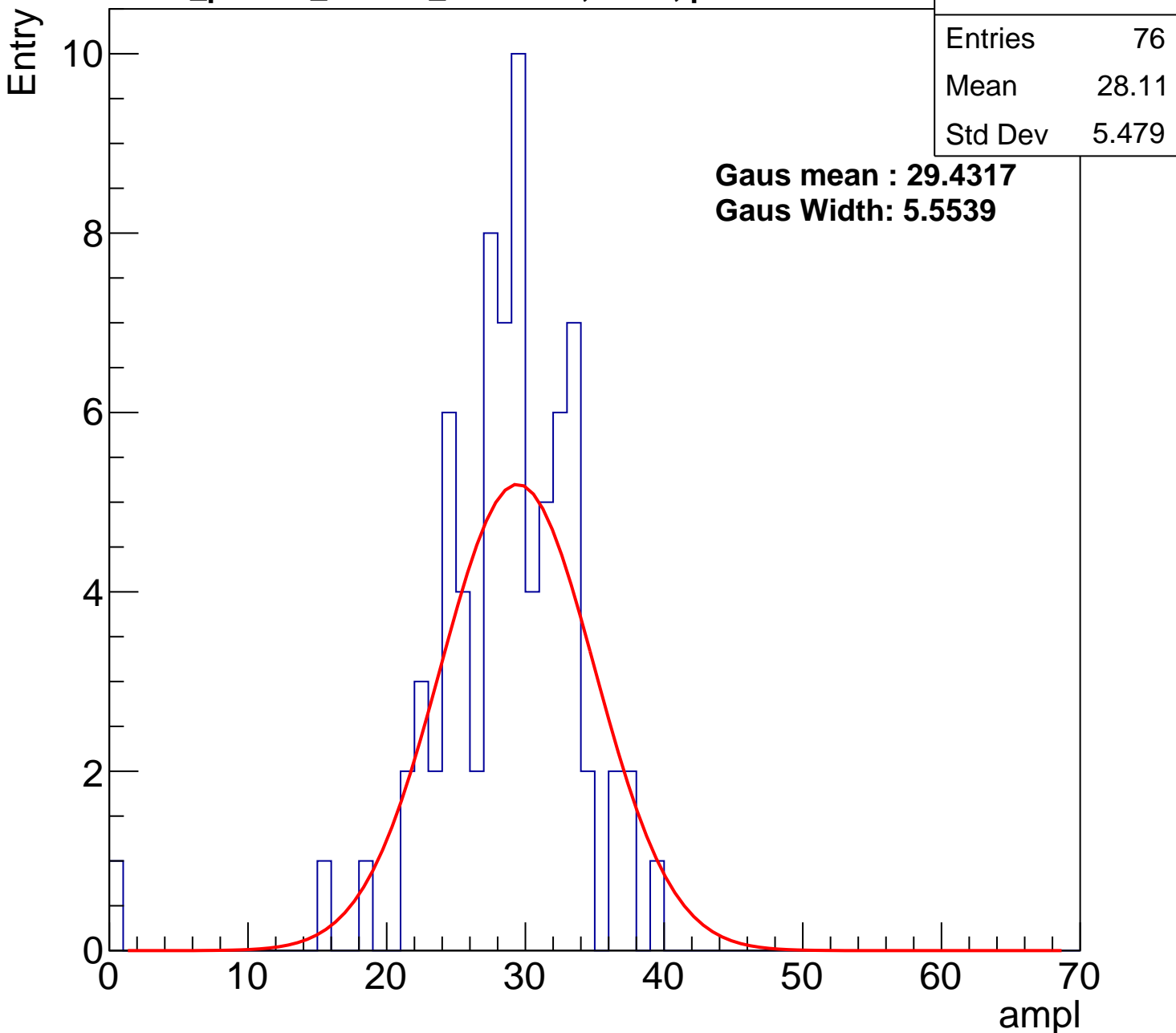
**Gaus Width: 5.5539**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch90, adc1

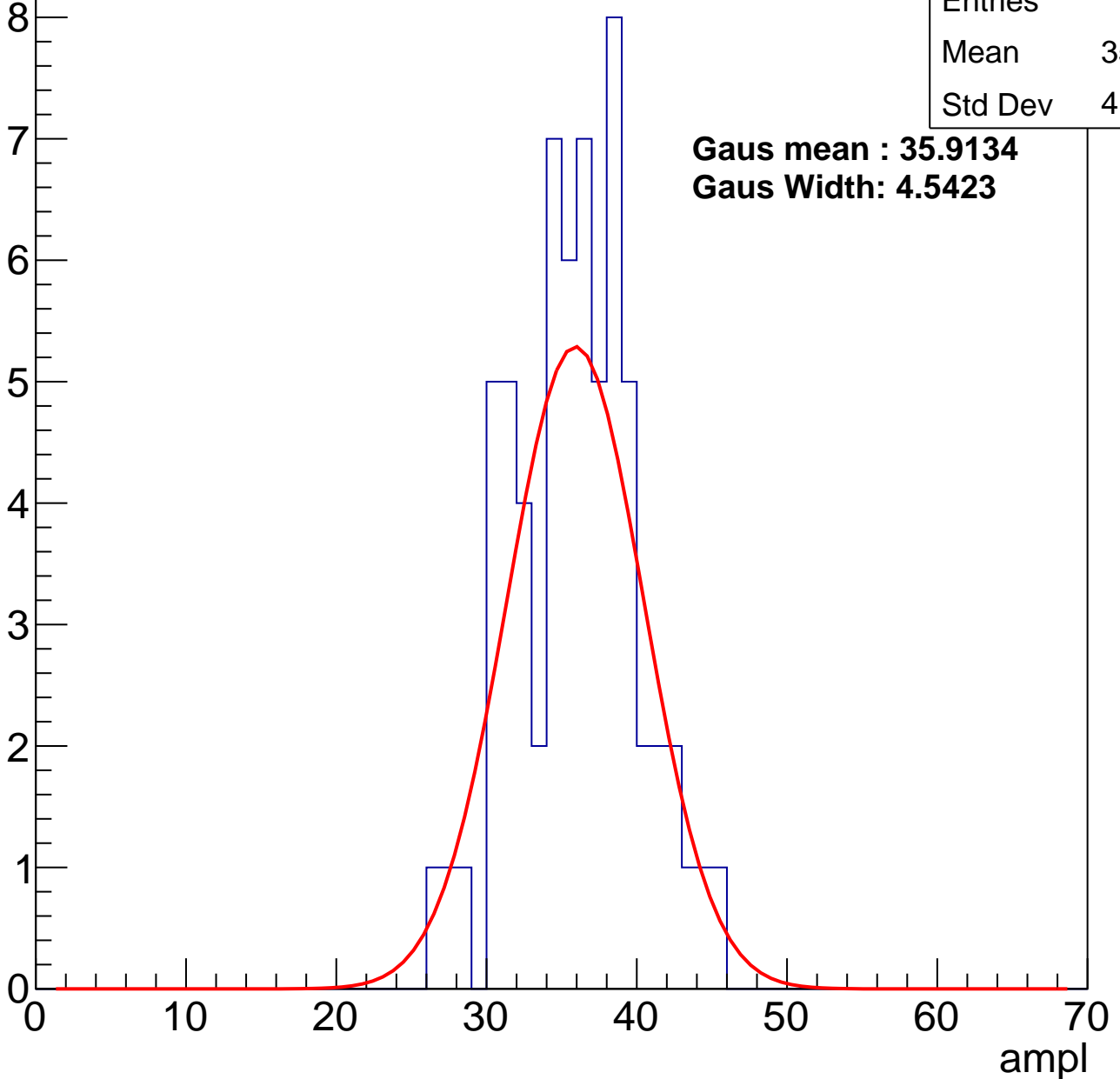
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	35.48
Std Dev	4.042

**Gaus mean : 35.9134**

**Gaus Width: 4.5423**



# B1L103S, U26-ch90, adc2

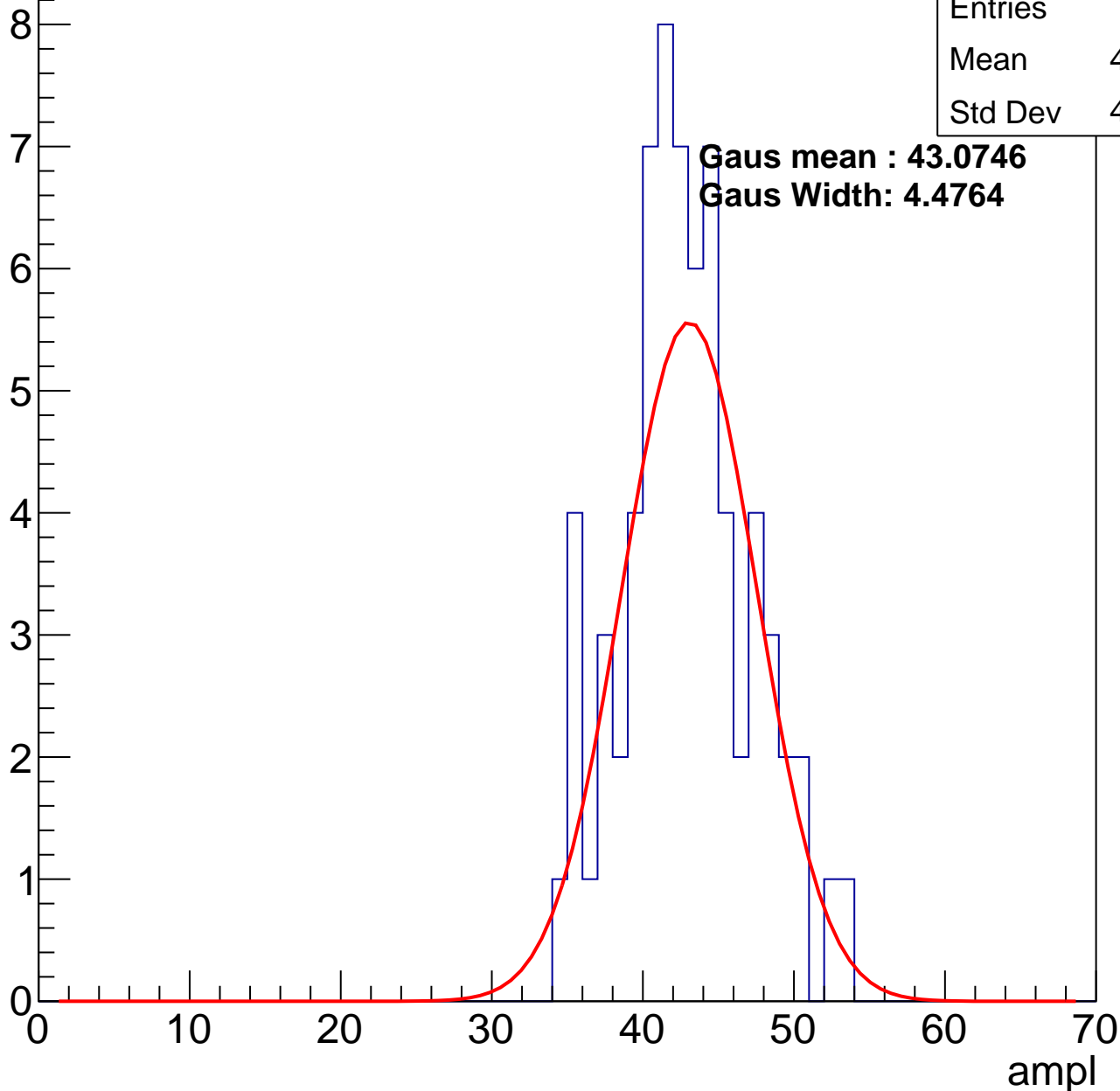
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	42.43
Std Dev	4.203

**Gaus mean : 43.0746**

**Gaus Width: 4.4764**

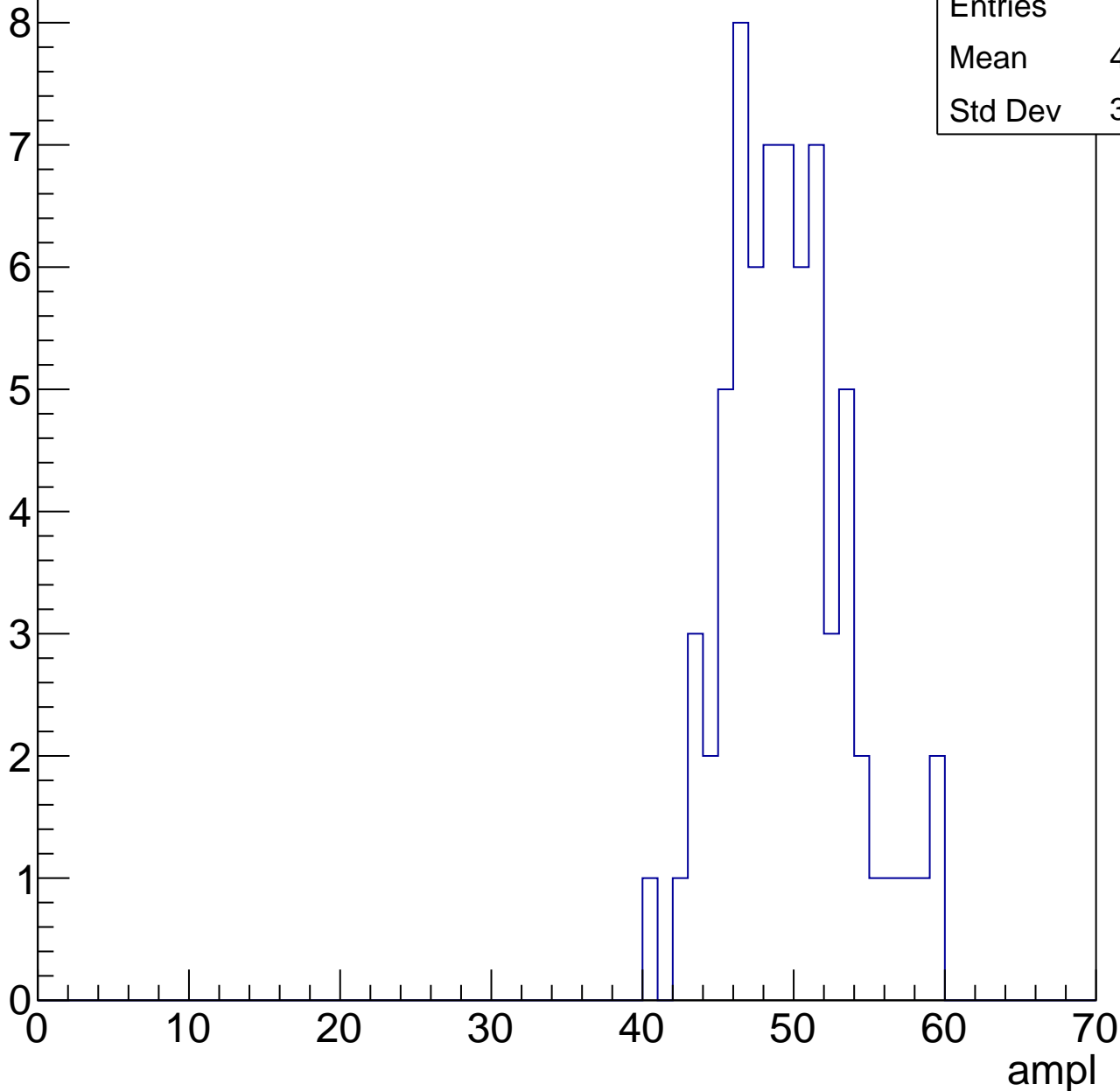


# B1L103S, U26-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

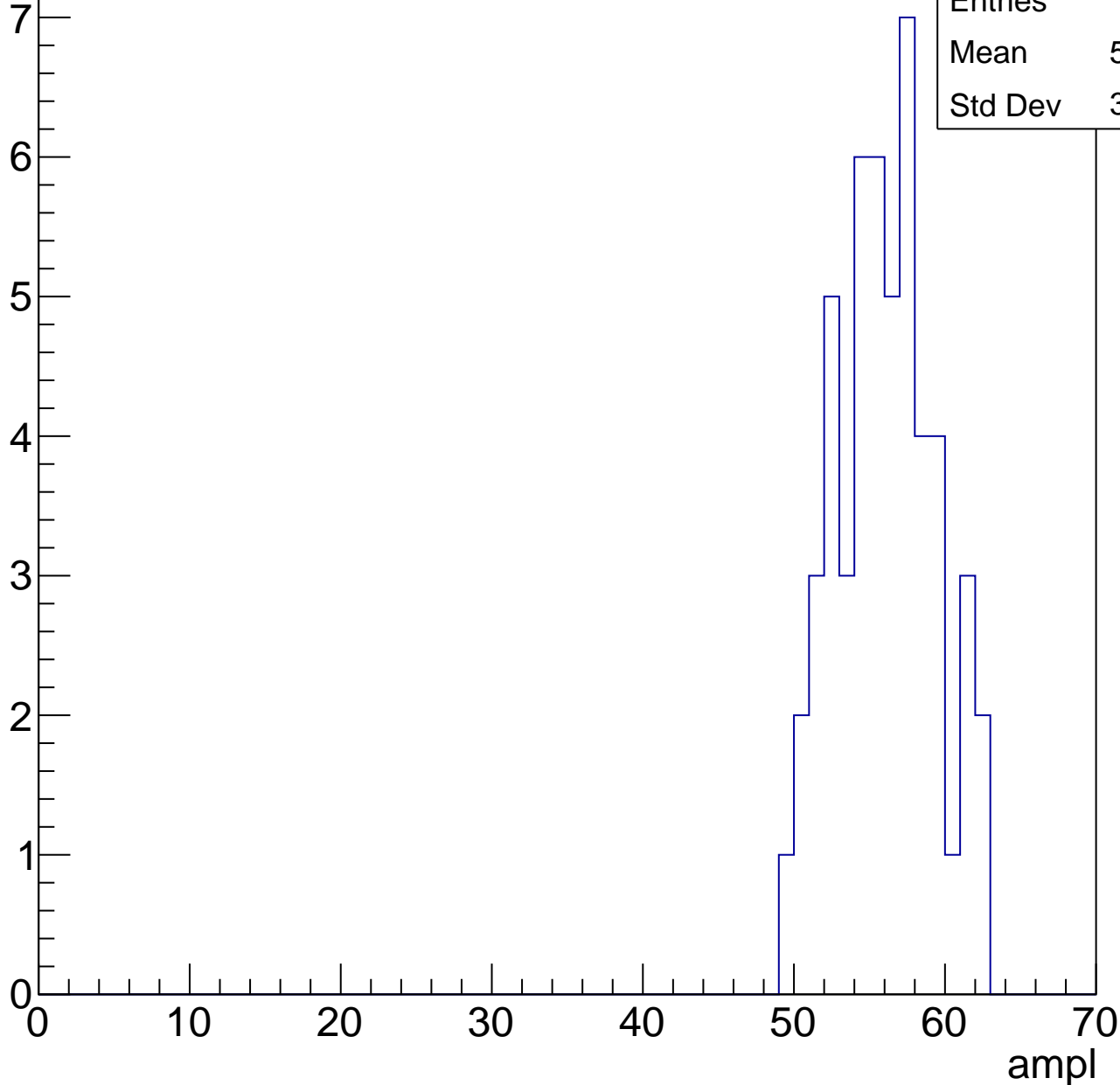
Entries	69
Mean	49.03
Std Dev	3.978



# B1L103S, U26-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



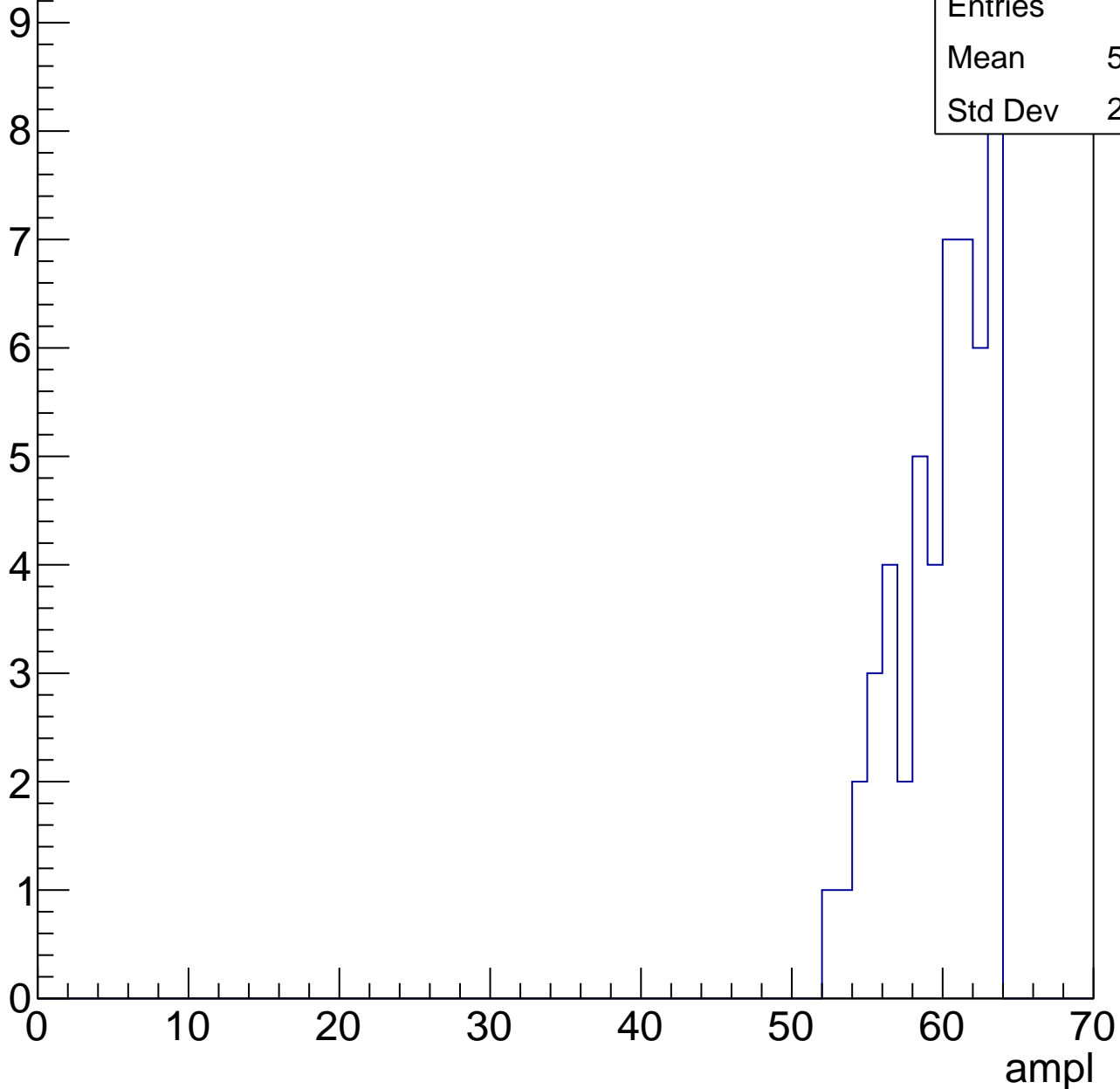
Entries	52
Mean	55.56
Std Dev	3.237

# B1L103S, U26-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	59.37
Std Dev	2.996



# B1L103S, U26-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

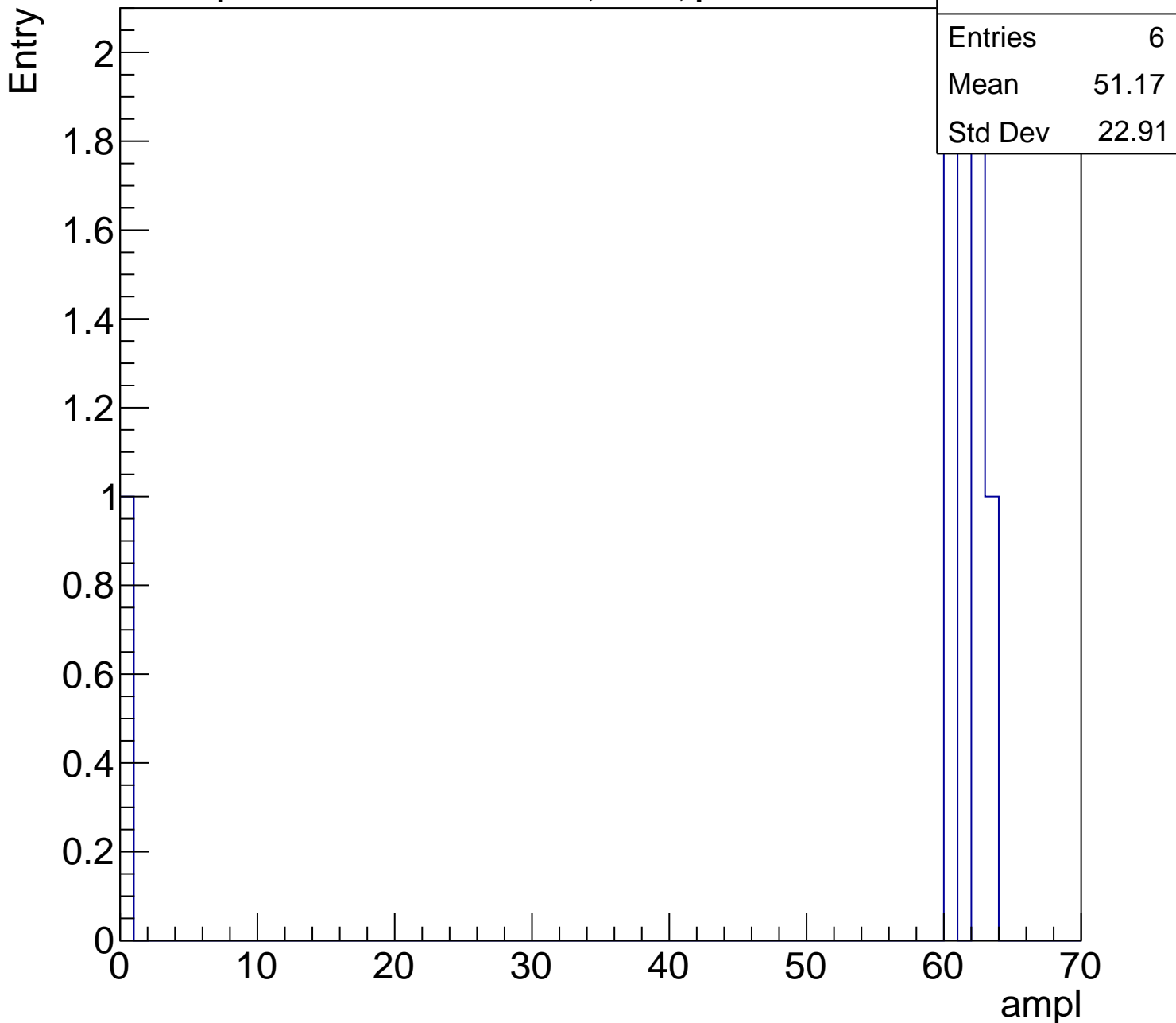
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	51.17
Std Dev	22.91

0 10 20 30 40 50 60 70

ampl





# B1L103S, U26-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U26-ch91, adc0

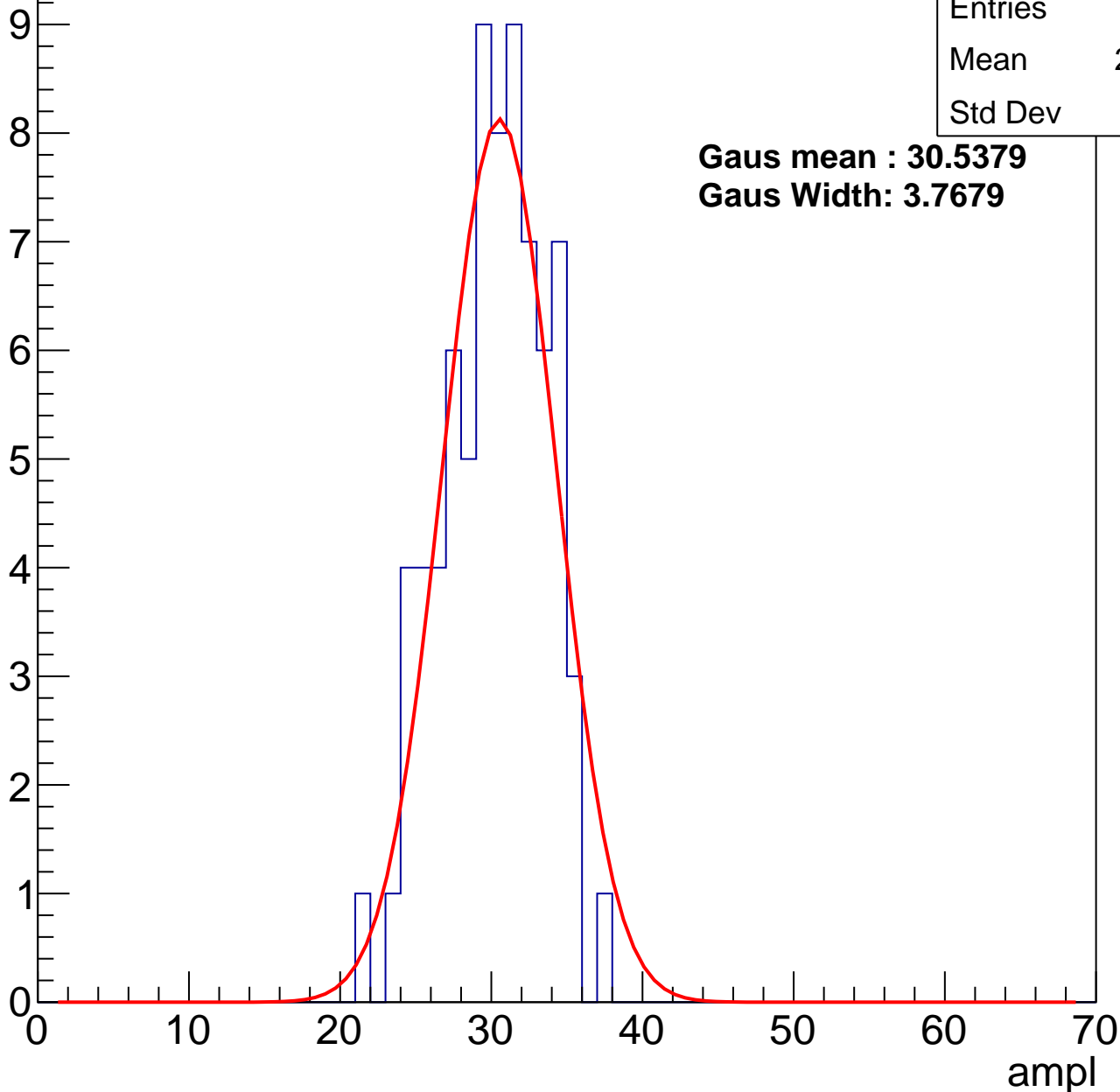
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	29.71
Std Dev	3.35

**Gaus mean : 30.5379**

**Gaus Width: 3.7679**



# B1L103S, U26-ch91, adc1

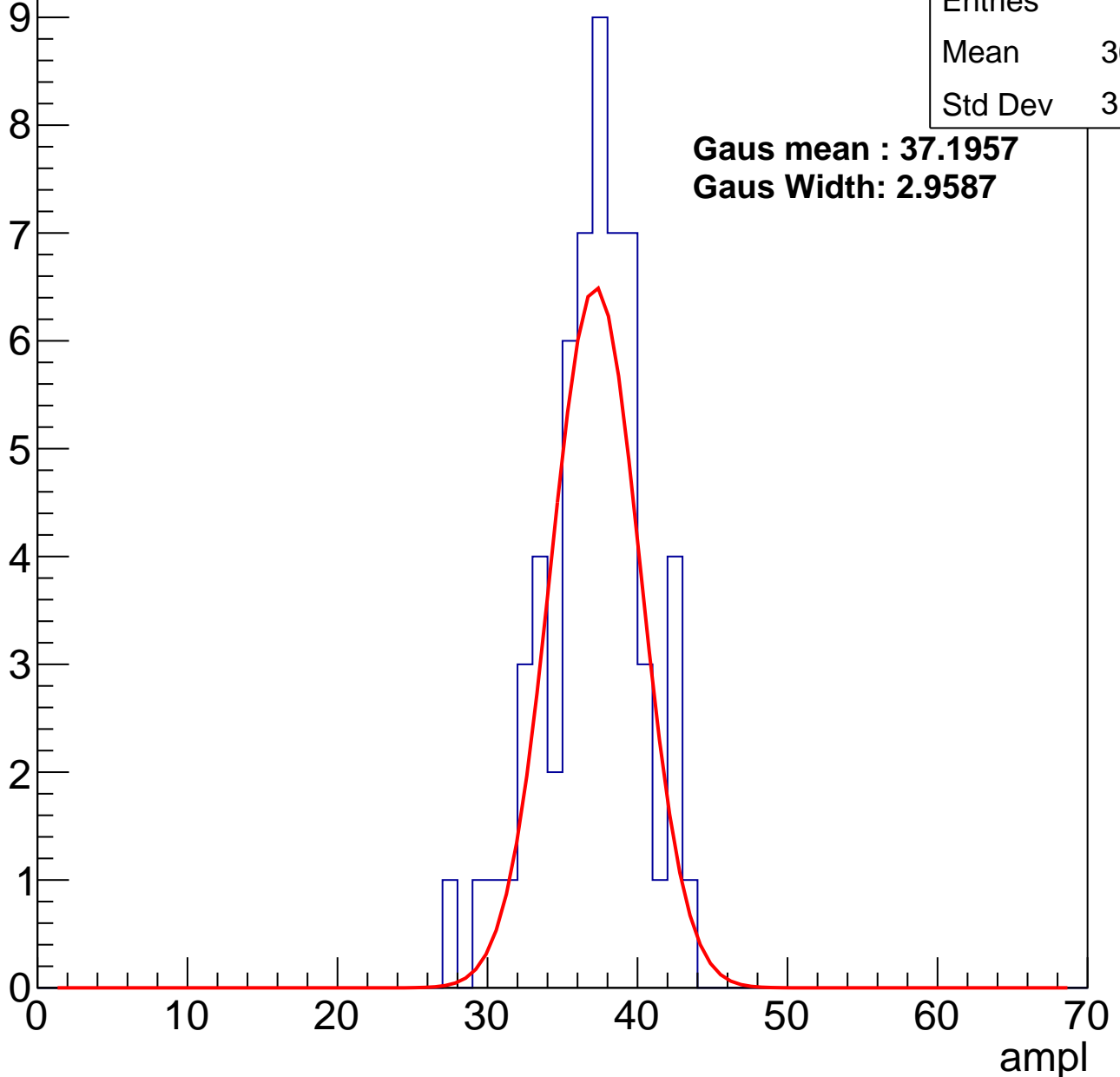
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	36.53
Std Dev	3.318

**Gaus mean : 37.1957**

**Gaus Width: 2.9587**



# B1L103S, U26-ch91, adc2

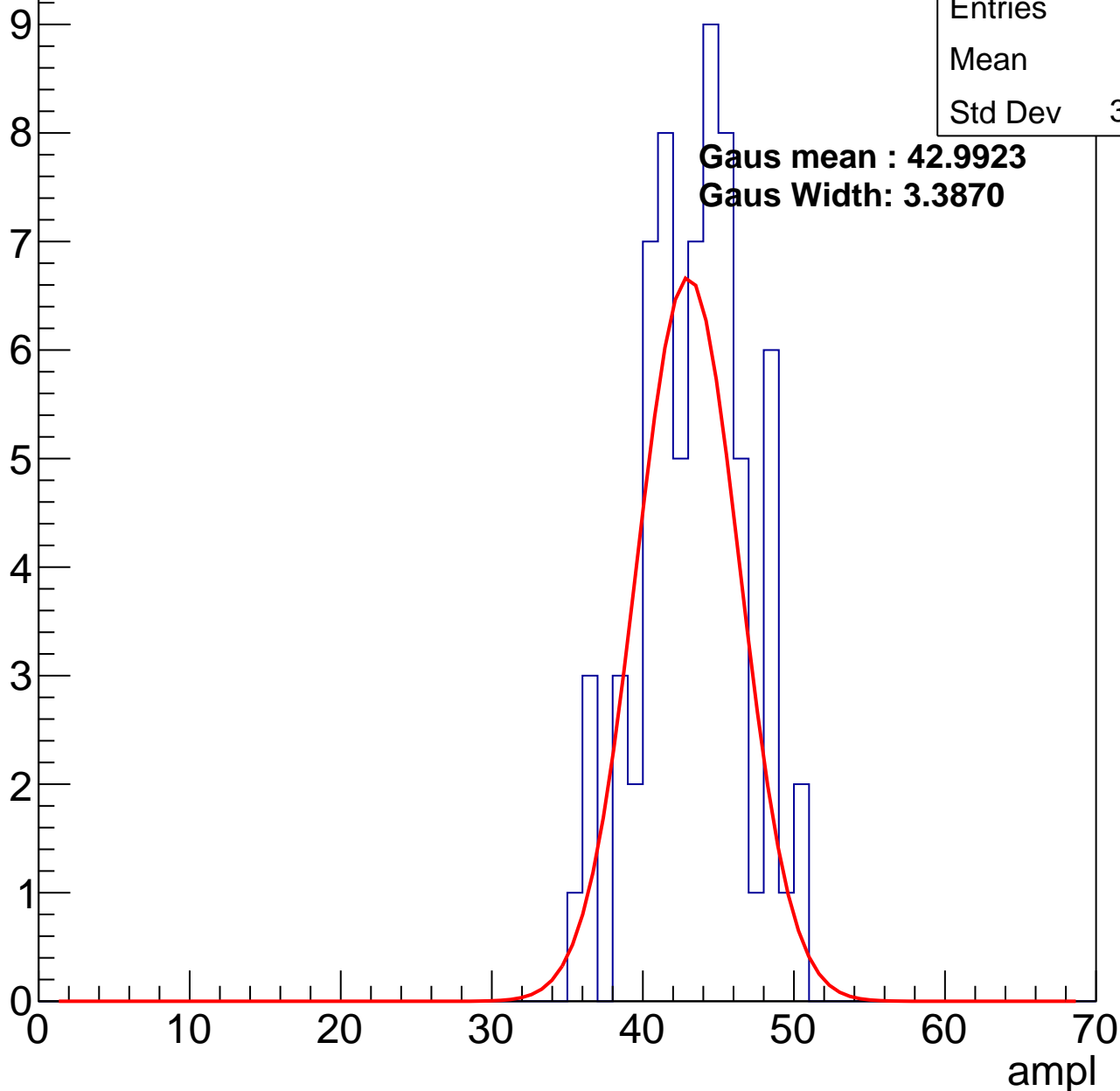
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	43
Std Dev	3.439

**Gaus mean : 42.9923**

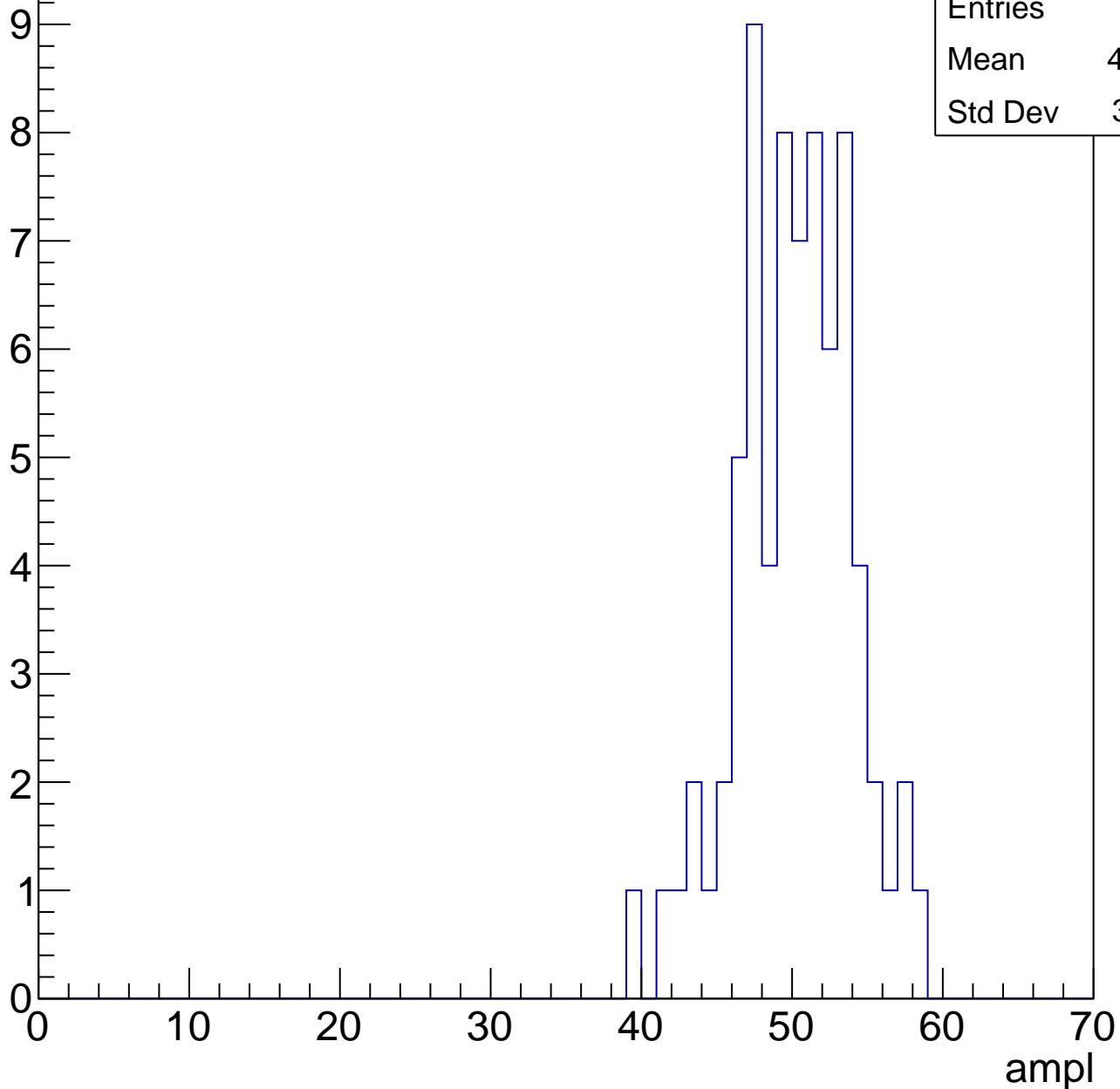
**Gaus Width: 3.3870**



# B1L103S, U26-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

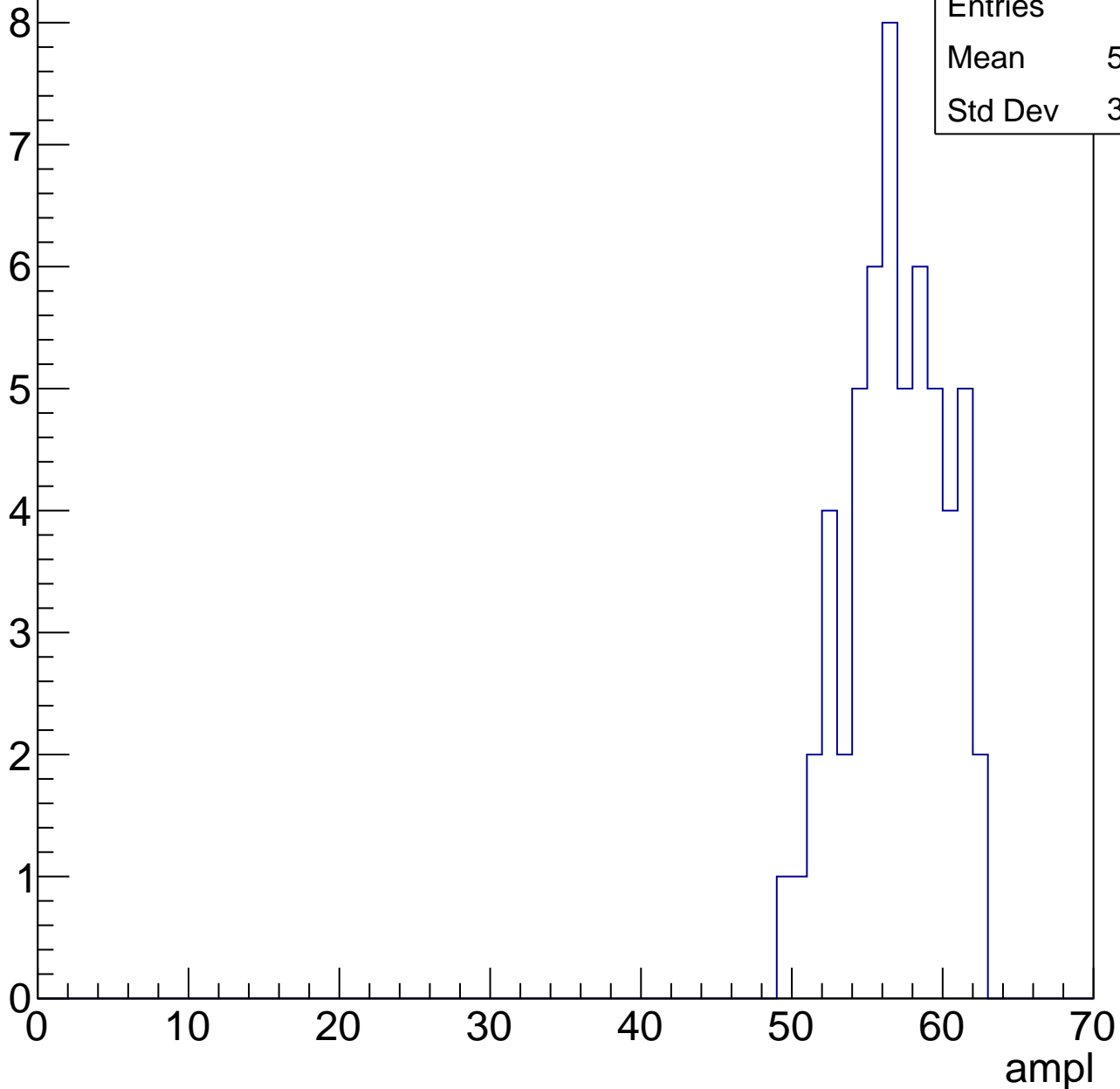


# B1L103S, U26-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	56.43
Std Dev	3.184

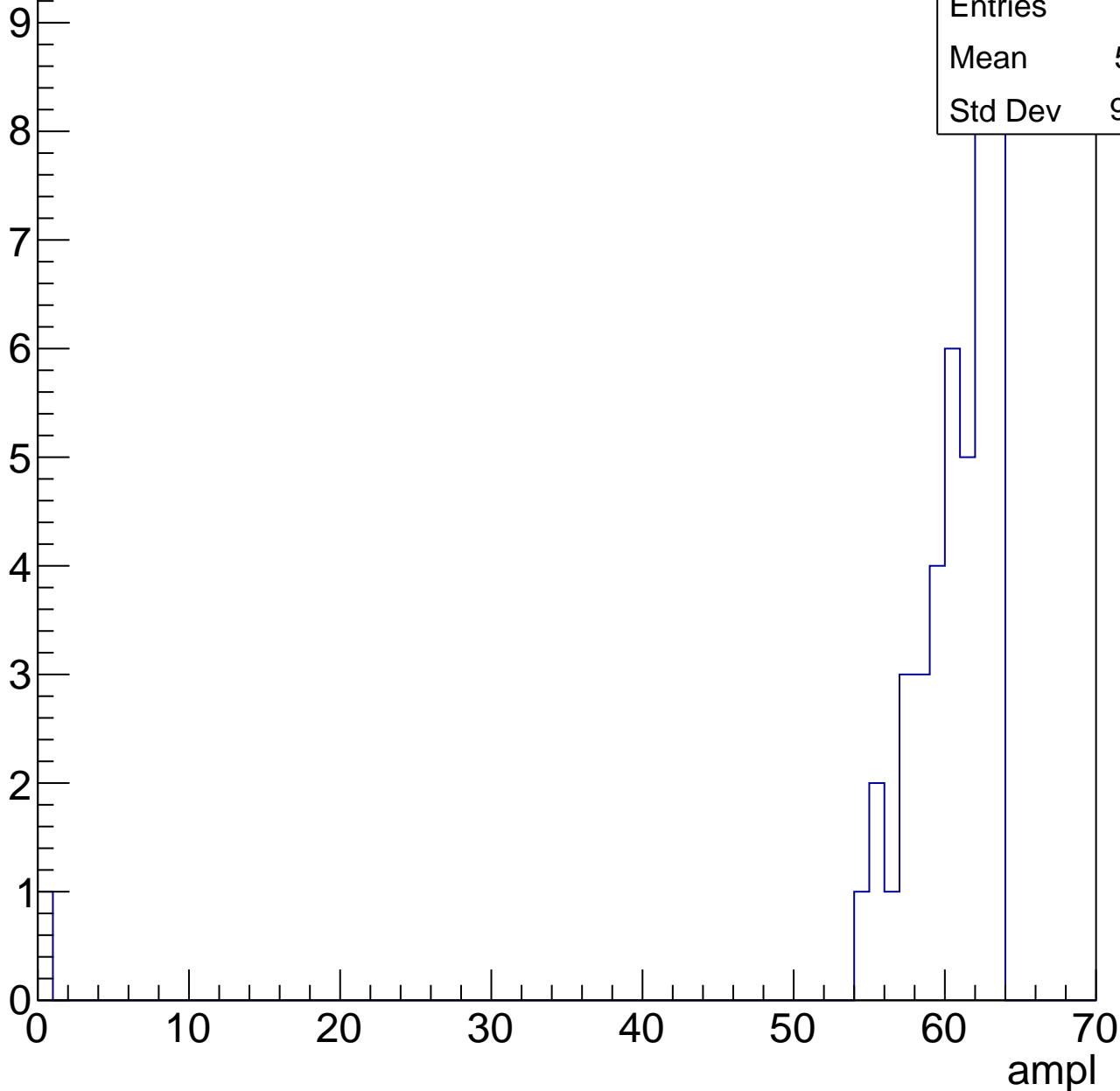


# B1L103S, U26-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	43
Mean	58.81
Std Dev	9.404



# B1L103S, U26-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L103S, U26-ch92, adc0

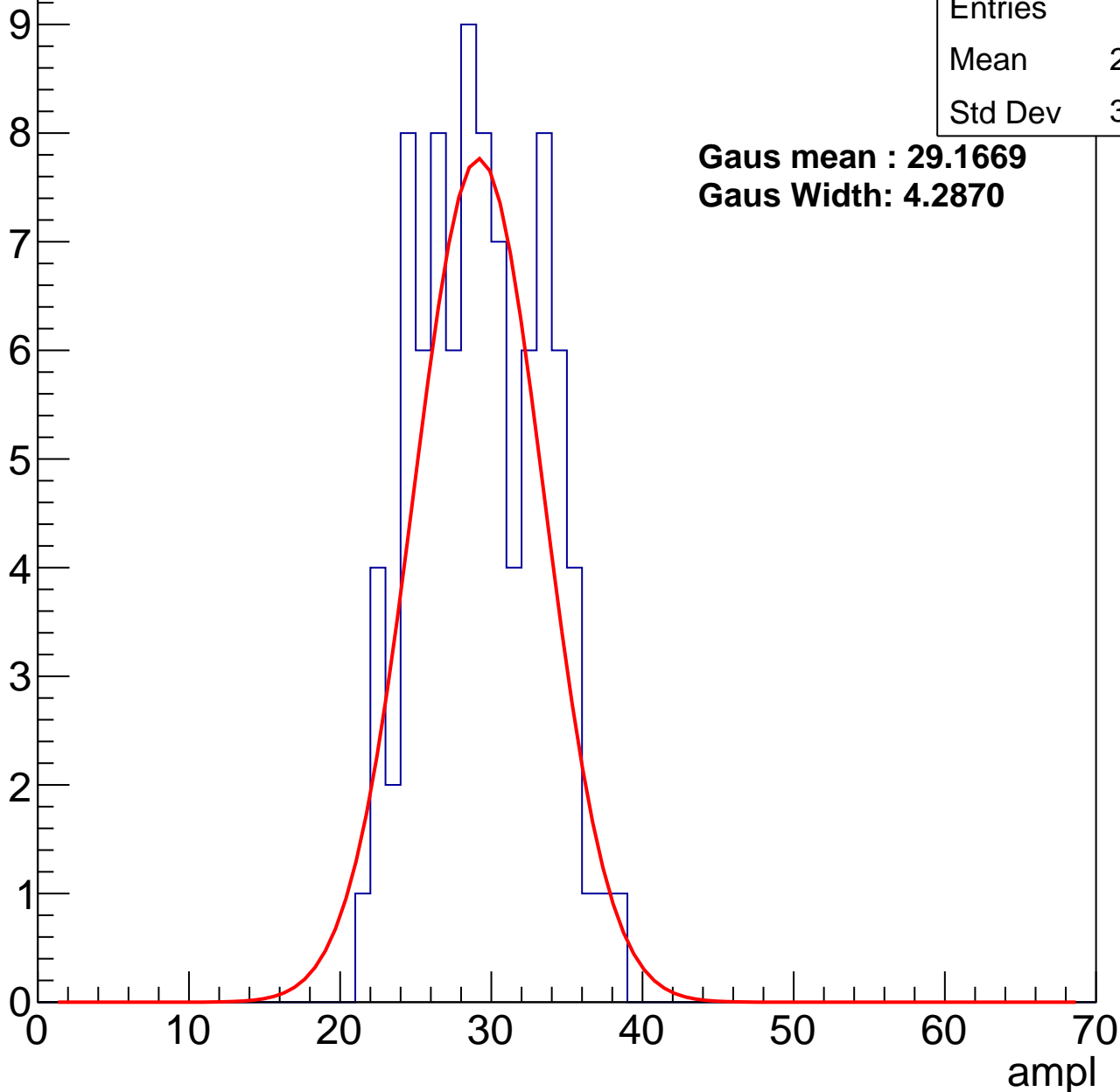
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	90
Mean	28.84
Std Dev	3.977

**Gaus mean : 29.1669**

**Gaus Width: 4.2870**



# B1L103S, U26-ch92, adc1

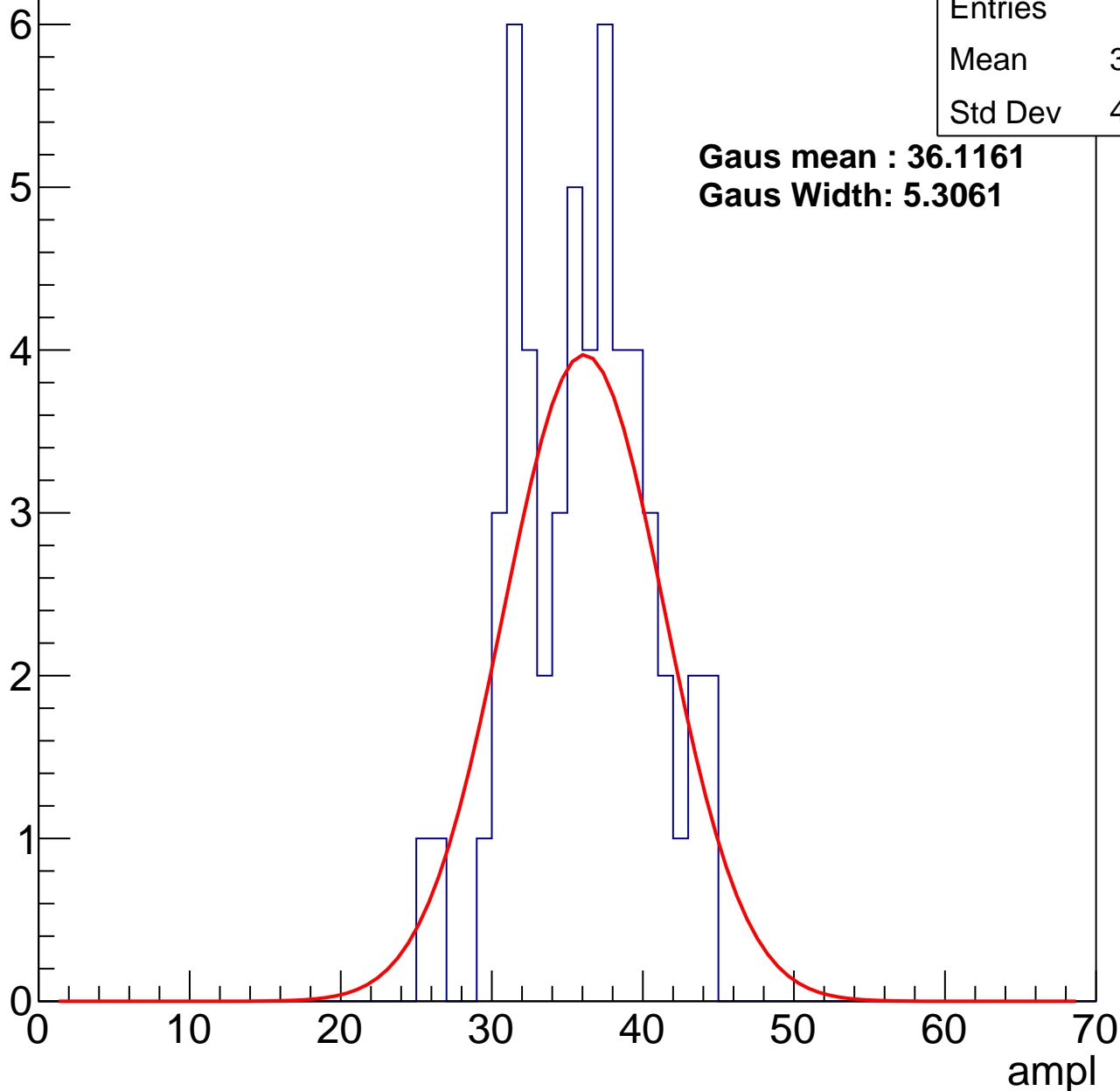
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	35.54
Std Dev	4.375

**Gaus mean : 36.1161**

**Gaus Width: 5.3061**



# B1L103S, U26-ch92, adc2

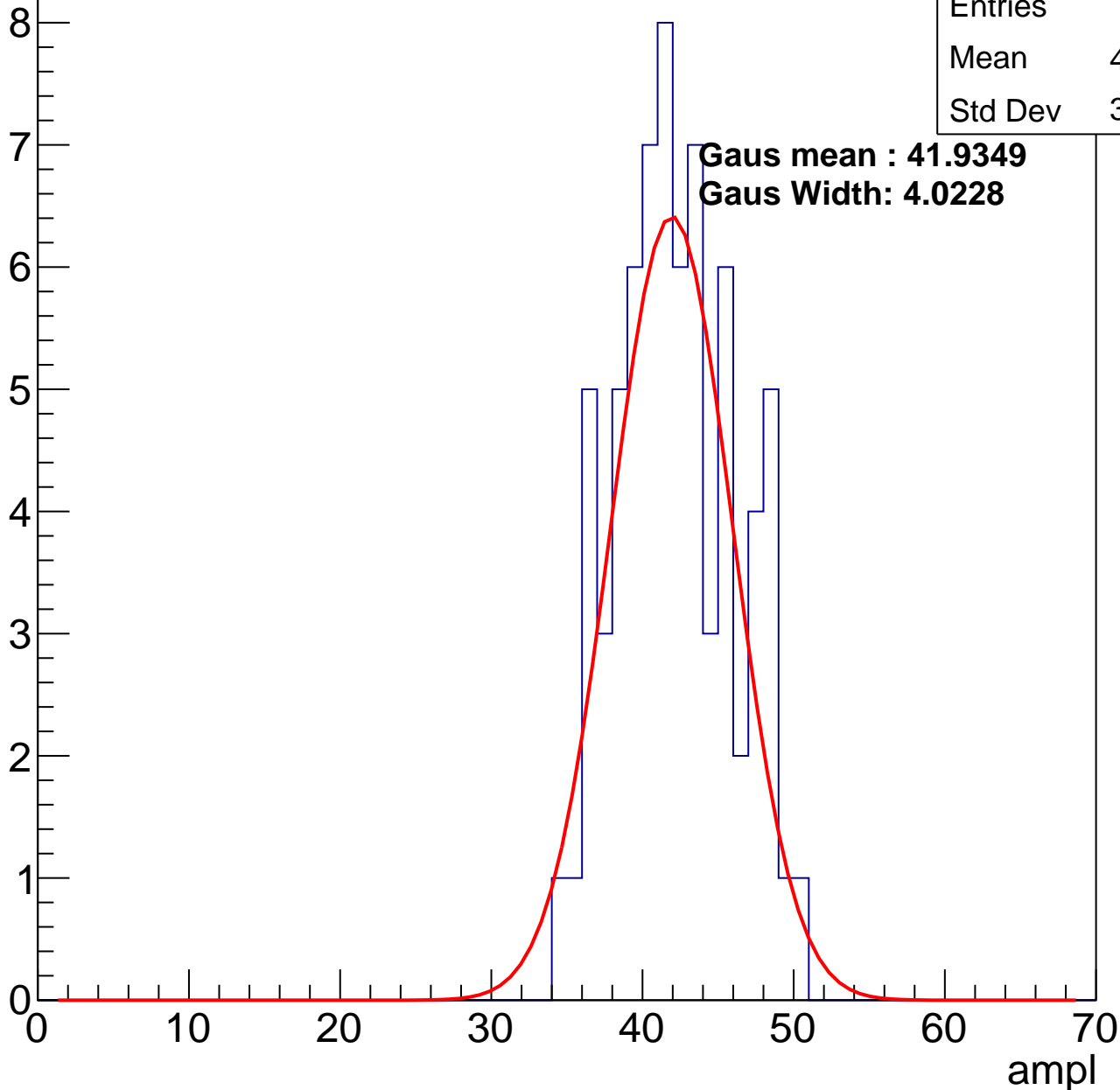
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	41.77
Std Dev	3.813

**Gaus mean : 41.9349**

**Gaus Width: 4.0228**

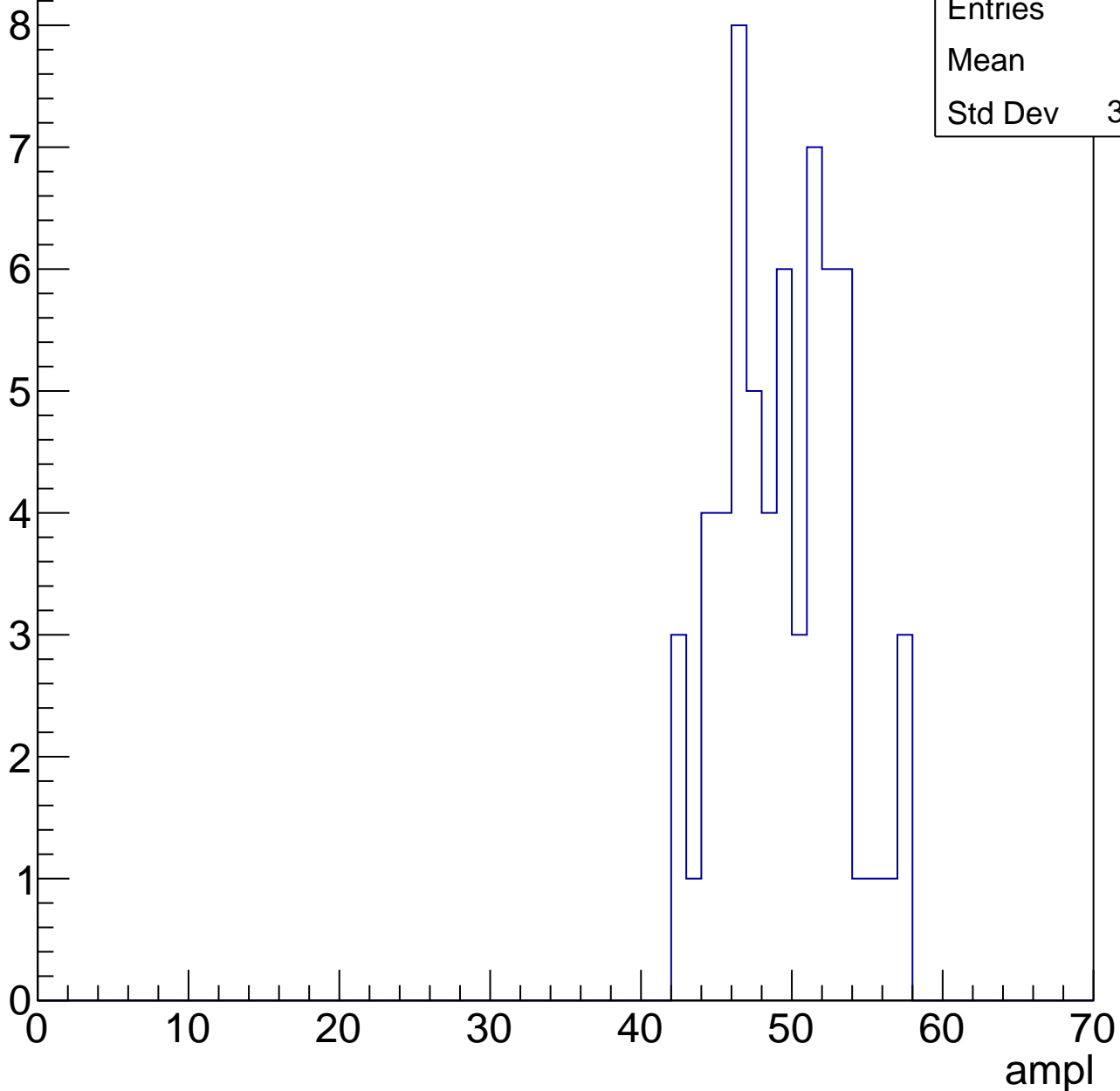


# B1L103S, U26-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	49
Std Dev	3.834

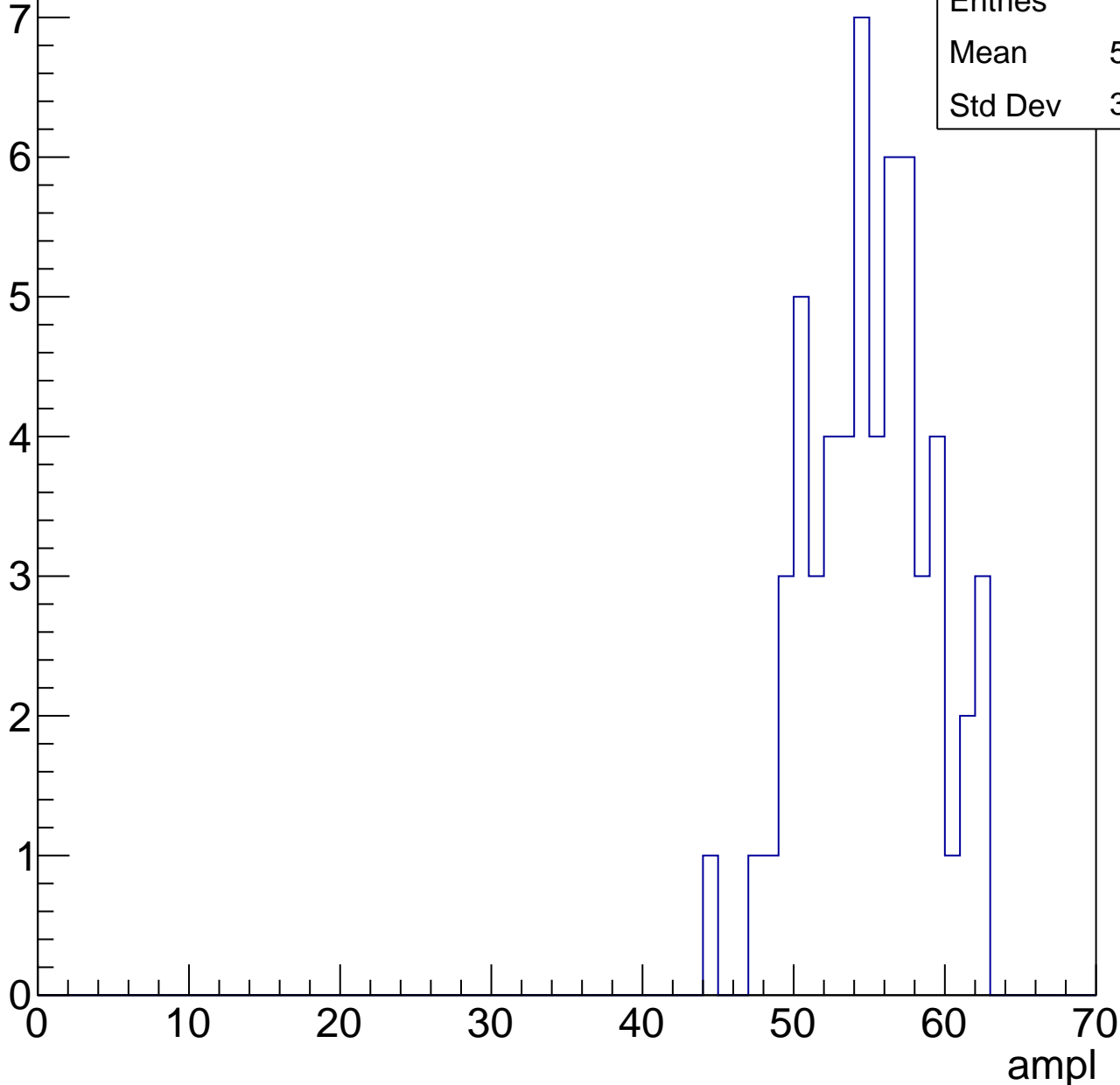


# B1L103S, U26-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	54.53
Std Dev	3.997

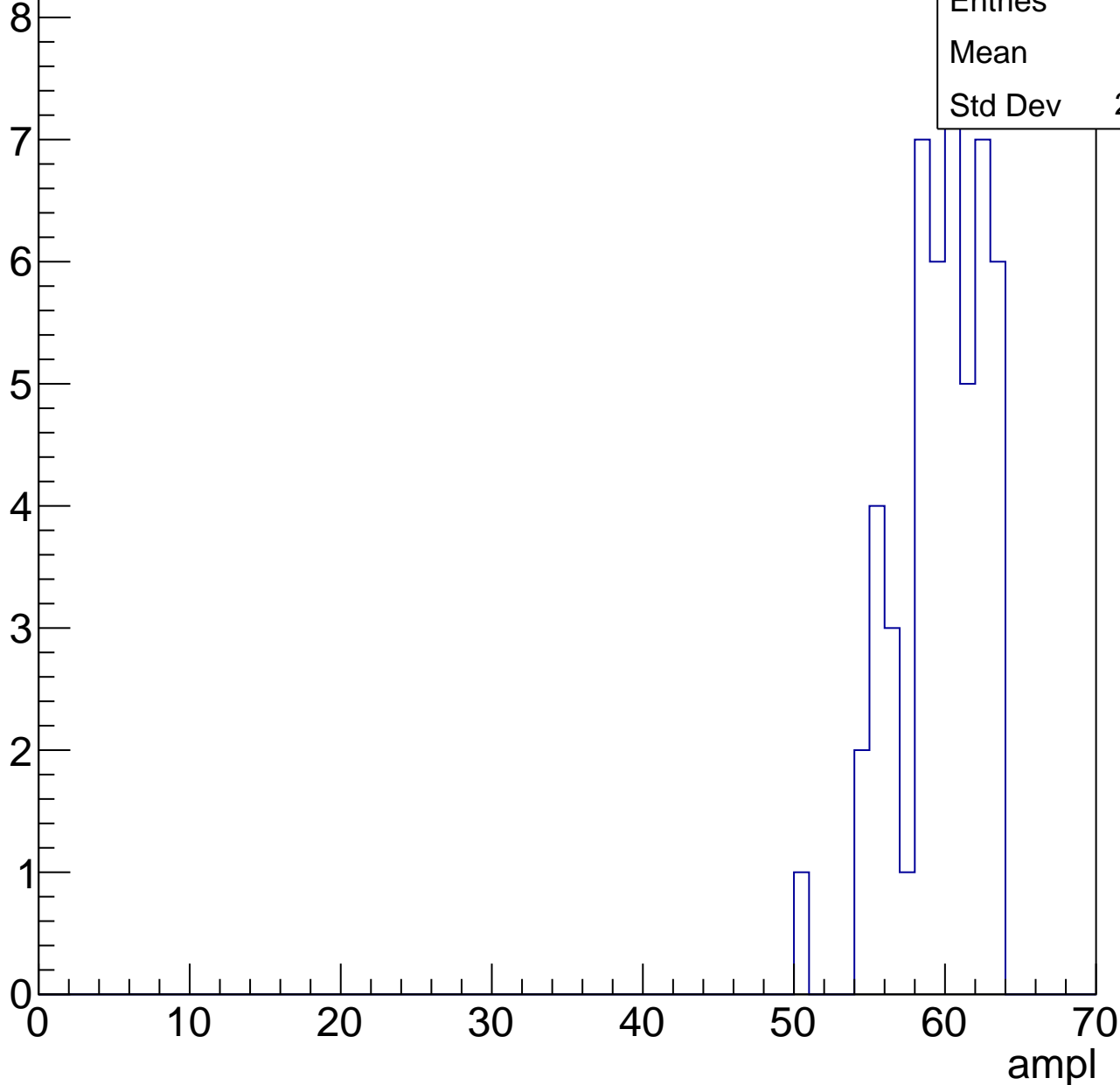


# B1L103S, U26-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

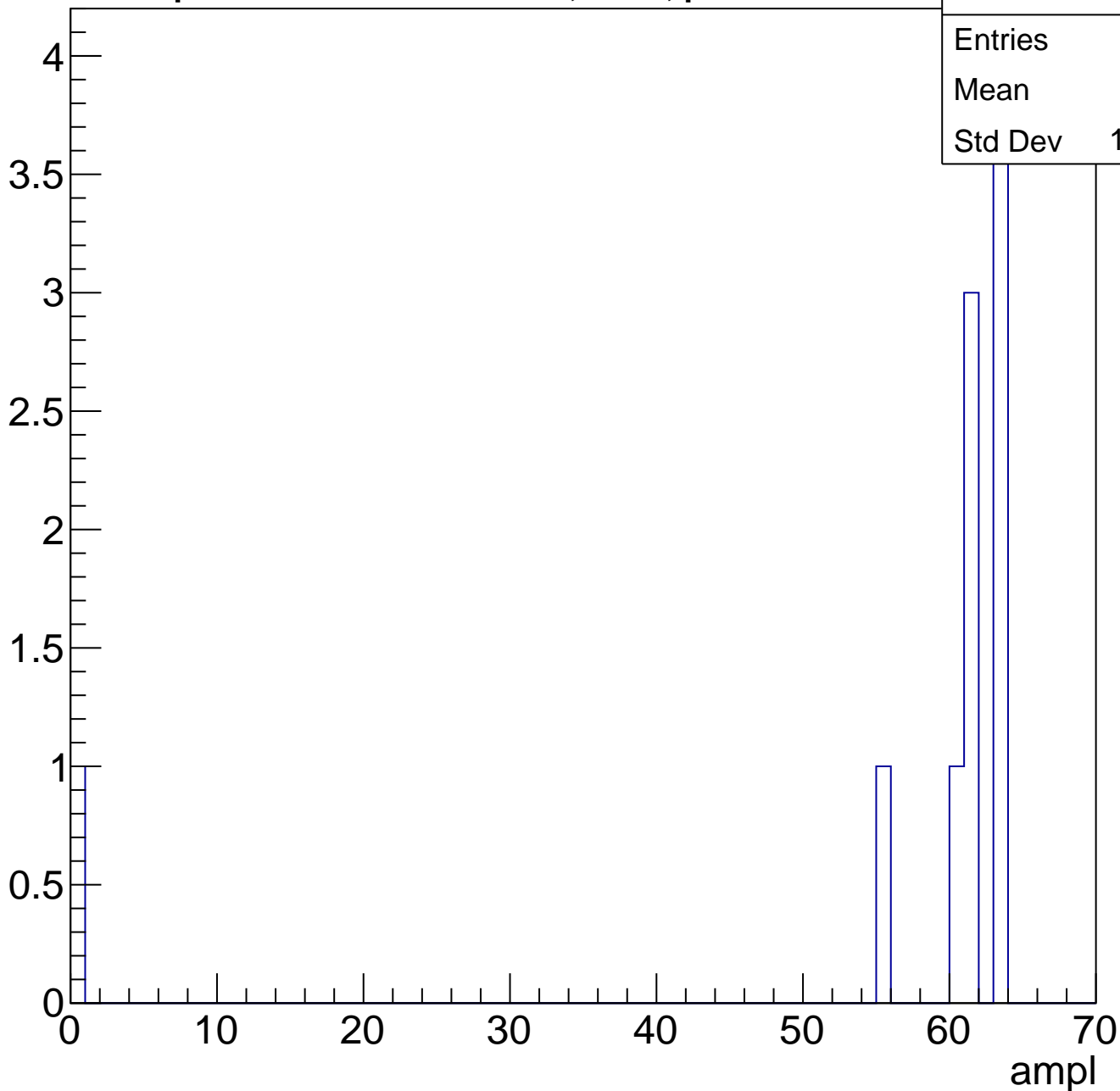
Entries	50
Mean	59.2
Std Dev	2.891



# B1L103S, U26-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U26-ch93, adc0

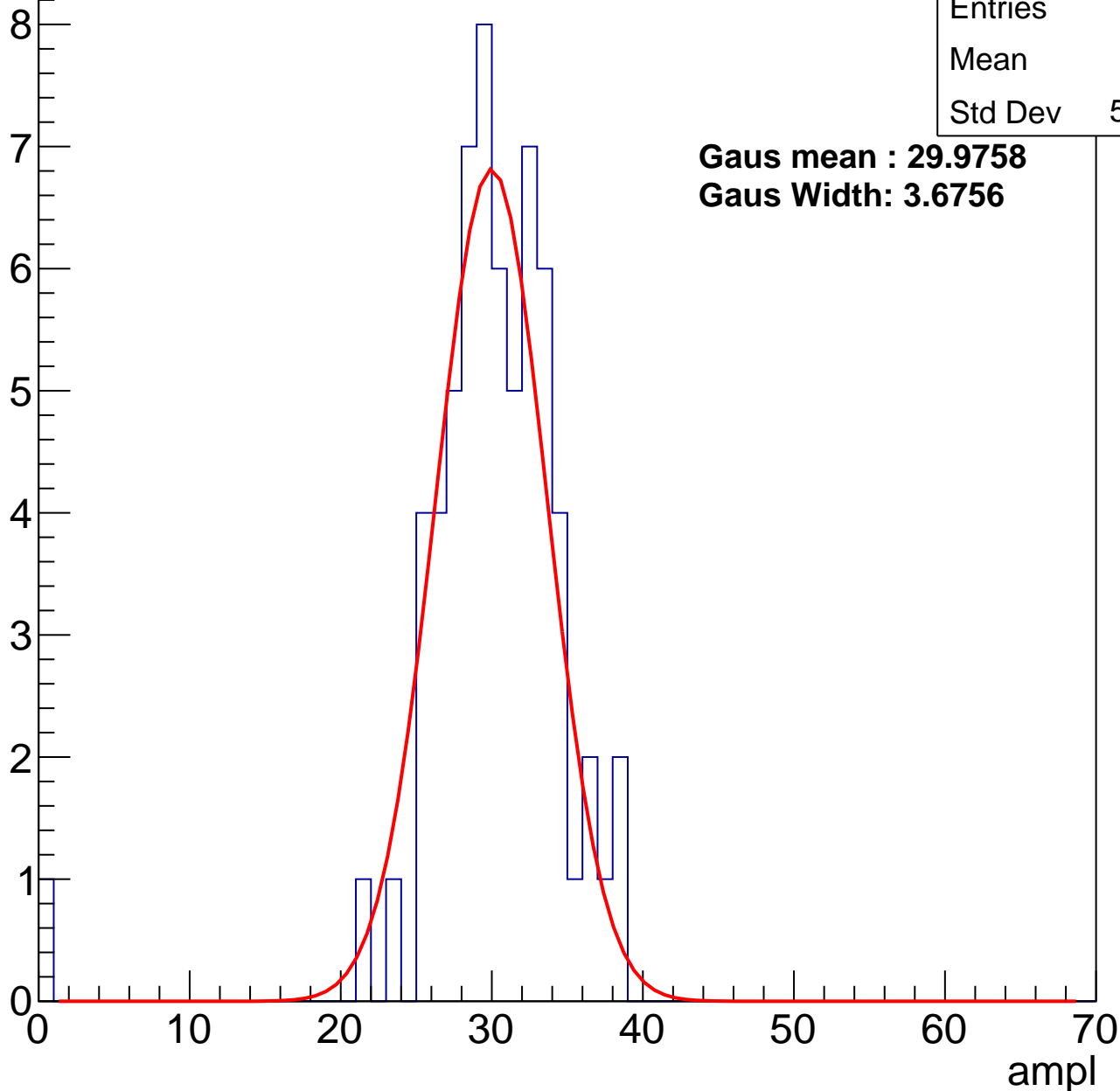
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	29.6
Std Dev	5.098

**Gaus mean : 29.9758**

**Gaus Width: 3.6756**



# B1L103S, U26-ch93, adc1

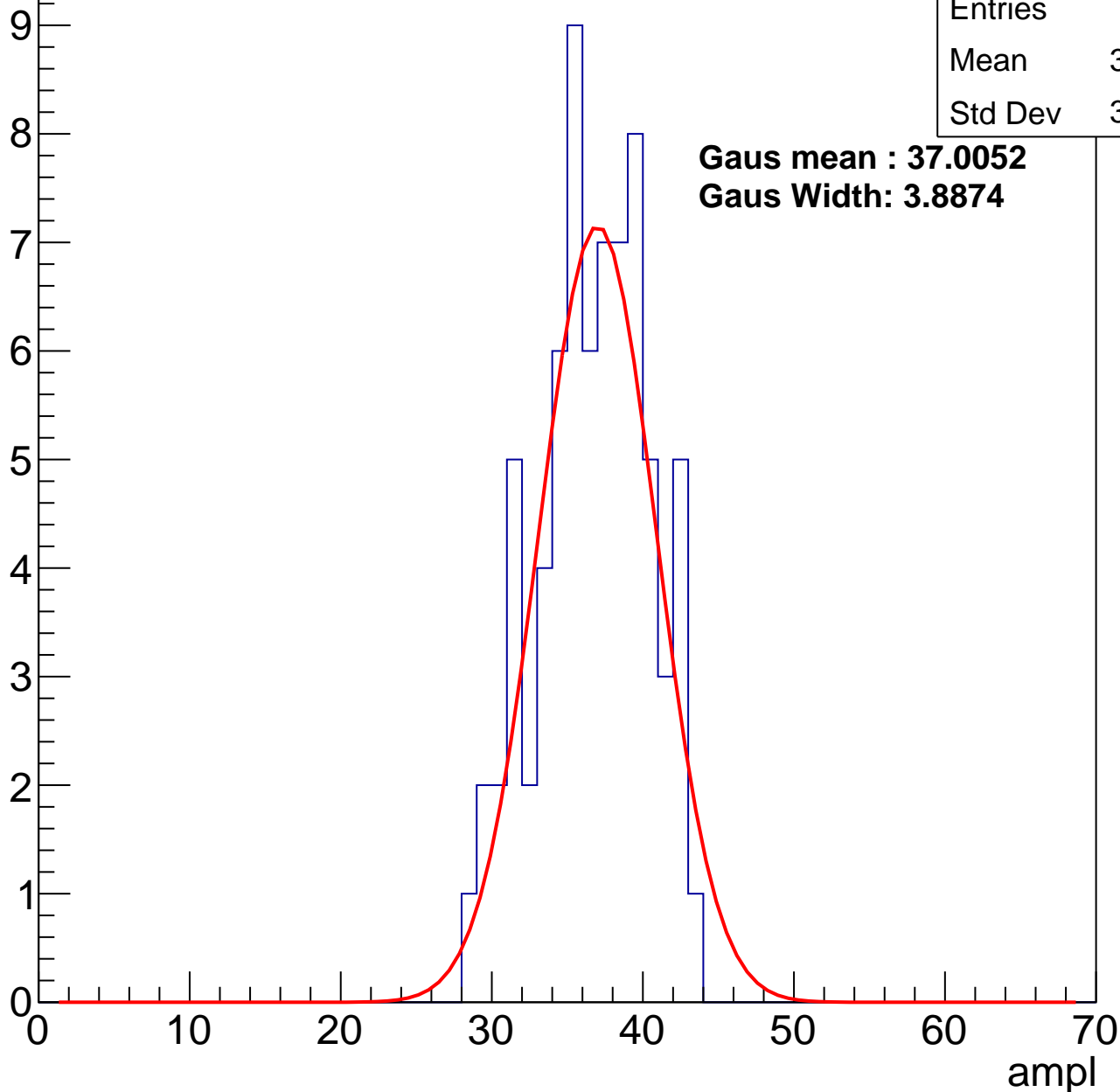
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	36.23
Std Dev	3.602

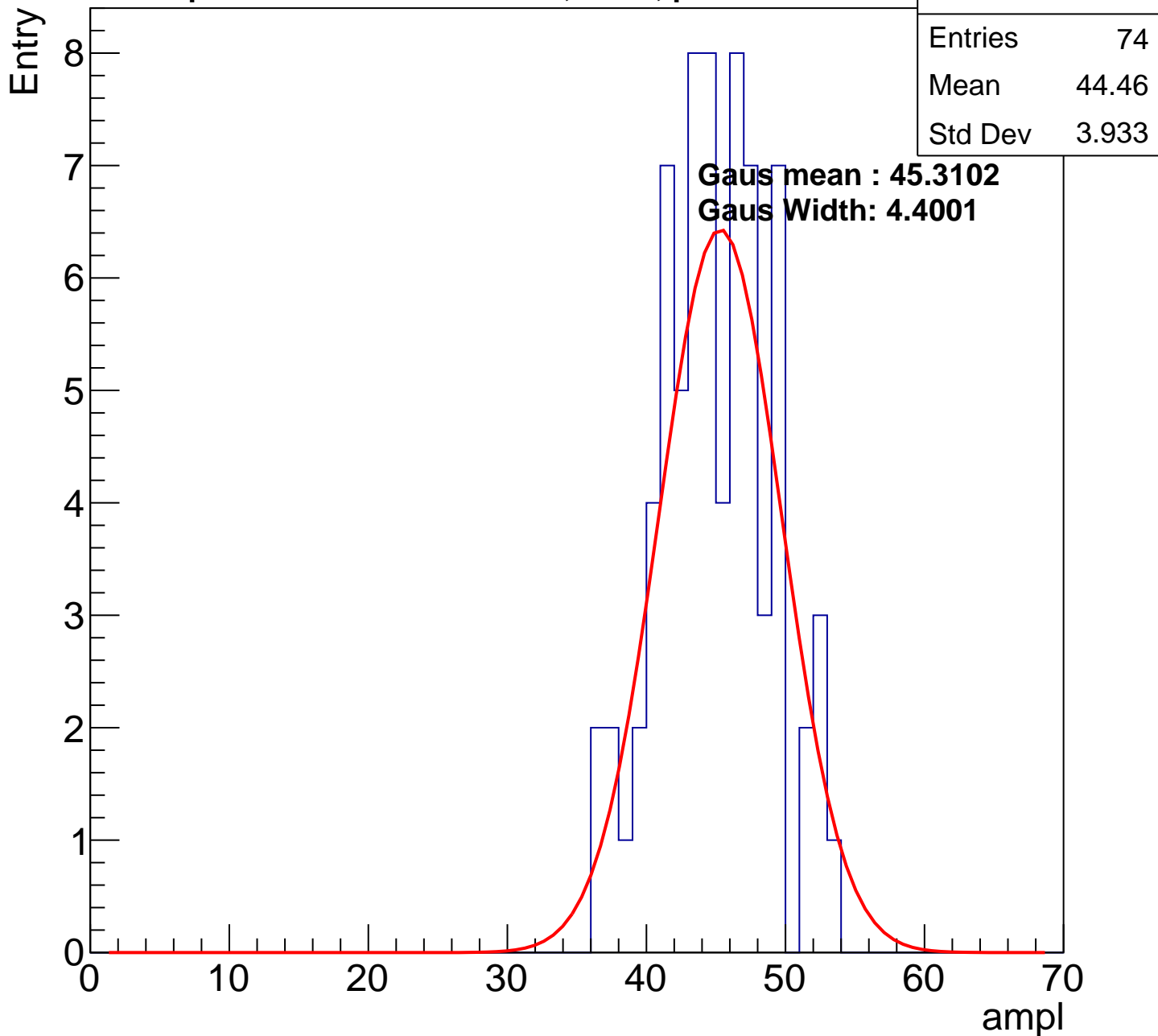
**Gaus mean : 37.0052**

**Gaus Width: 3.8874**



# B1L103S, U26-ch93, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

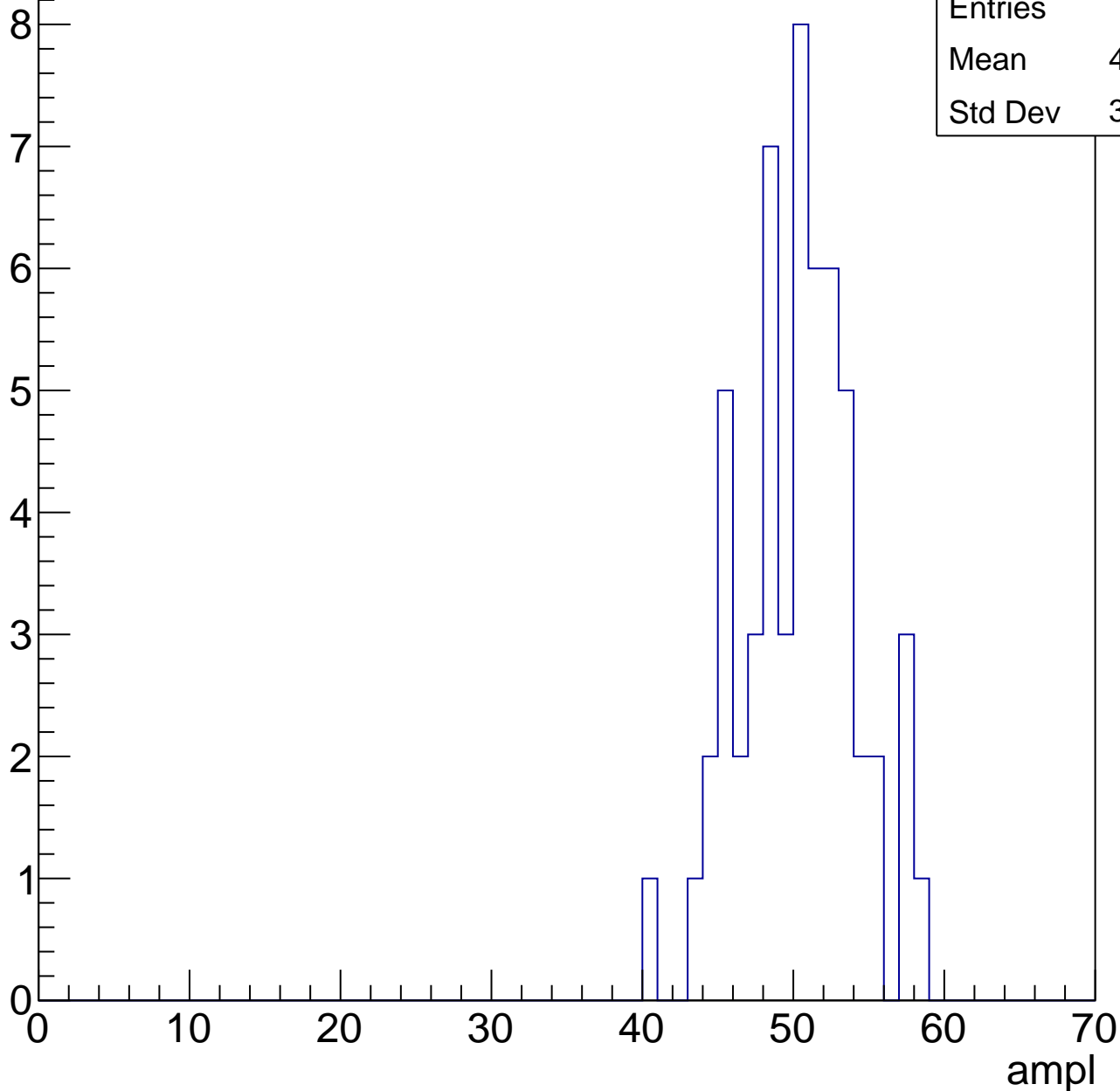


# B1L103S, U26-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	49.86
Std Dev	3.753

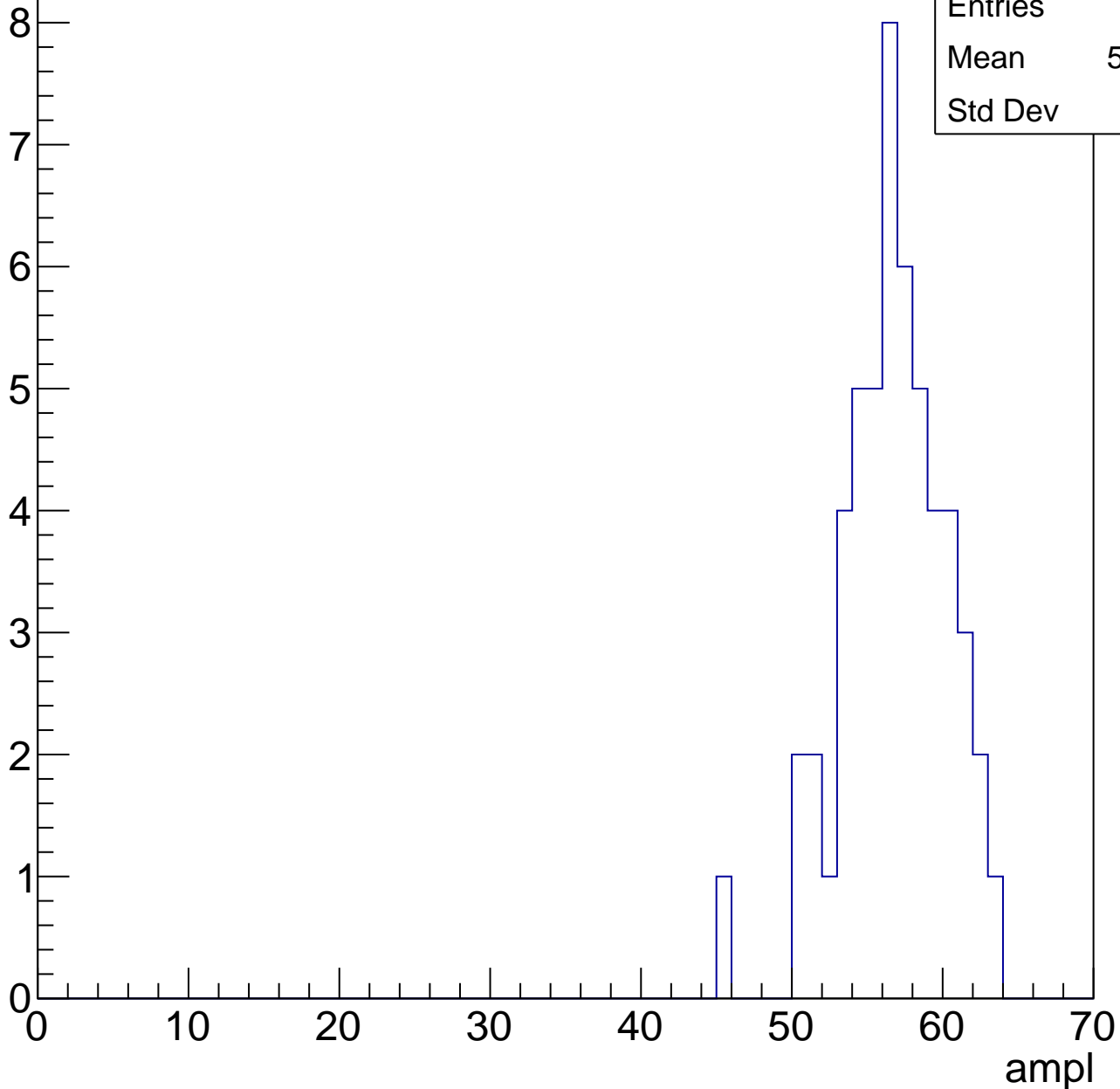


# B1L103S, U26-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	56.26
Std Dev	3.47

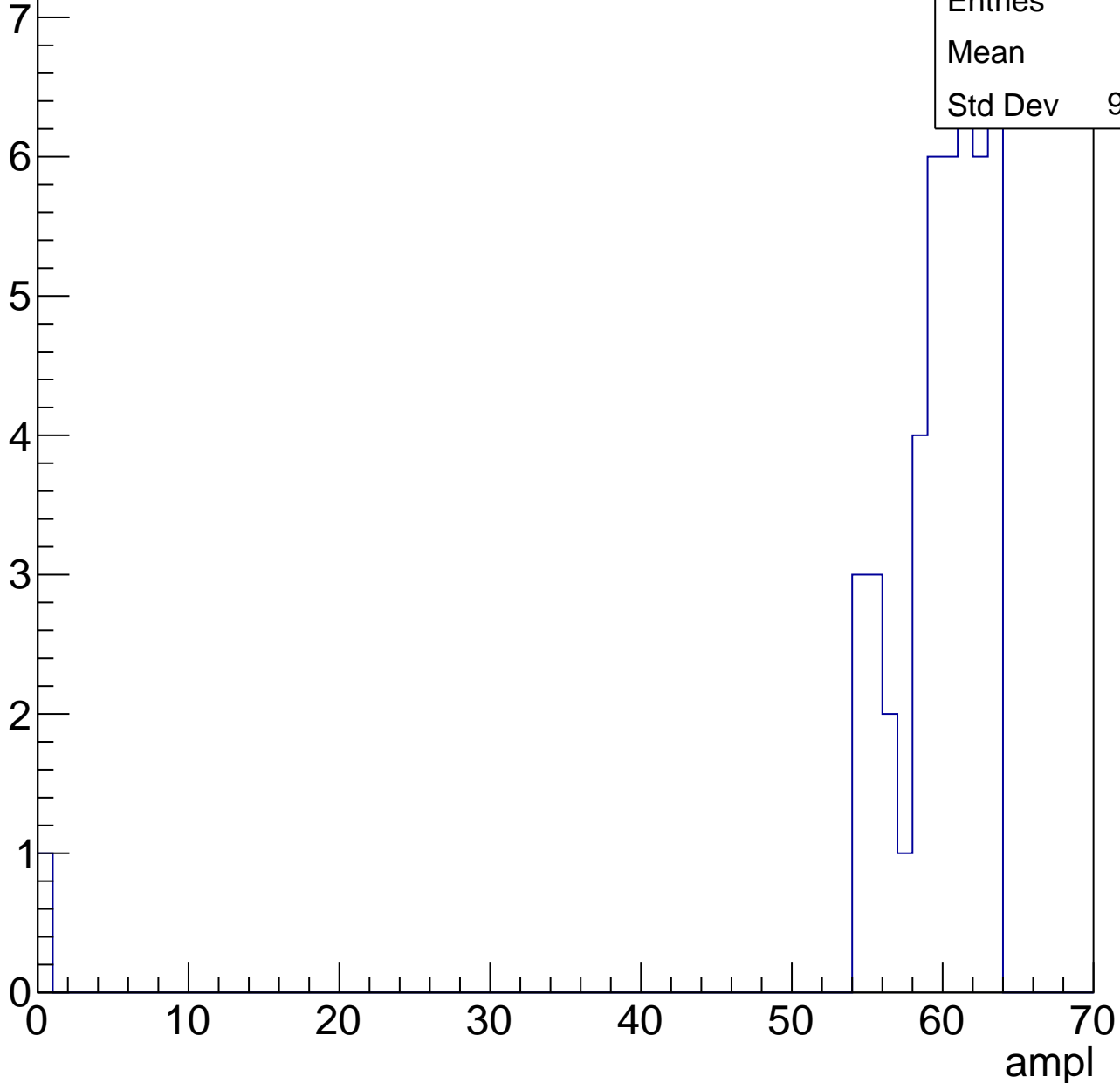


# B1L103S, U26-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	58.3
Std Dev	9.098



# B1L103S, U26-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	62.5
Std Dev	0.5

0 10 20 30 40 50 60 70

ampl



# B1L103S, U26-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch94, adc0

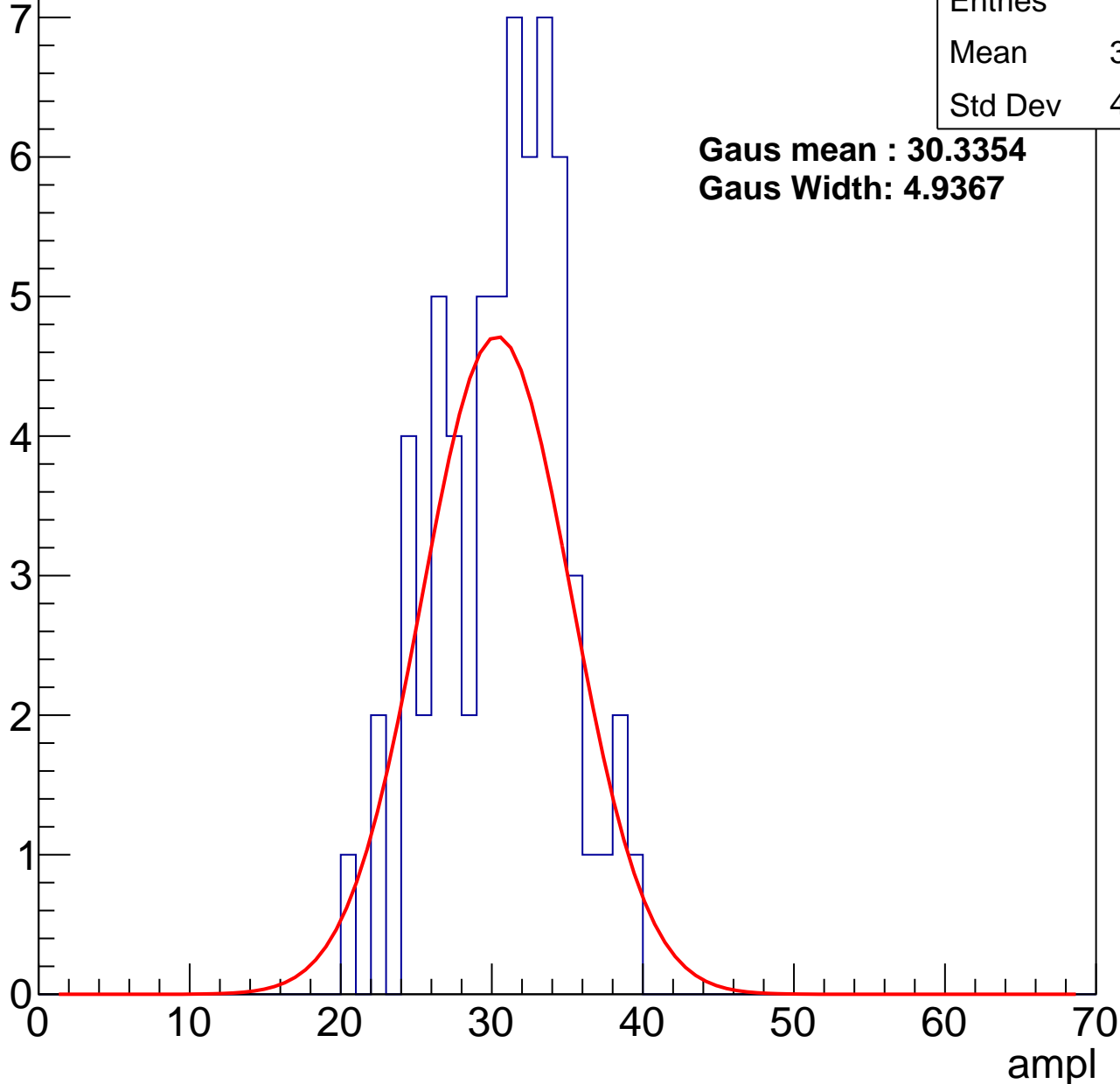
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	30.25
Std Dev	4.157

**Gaus mean : 30.3354**

**Gaus Width: 4.9367**



# B1L103S, U26-ch94, adc1

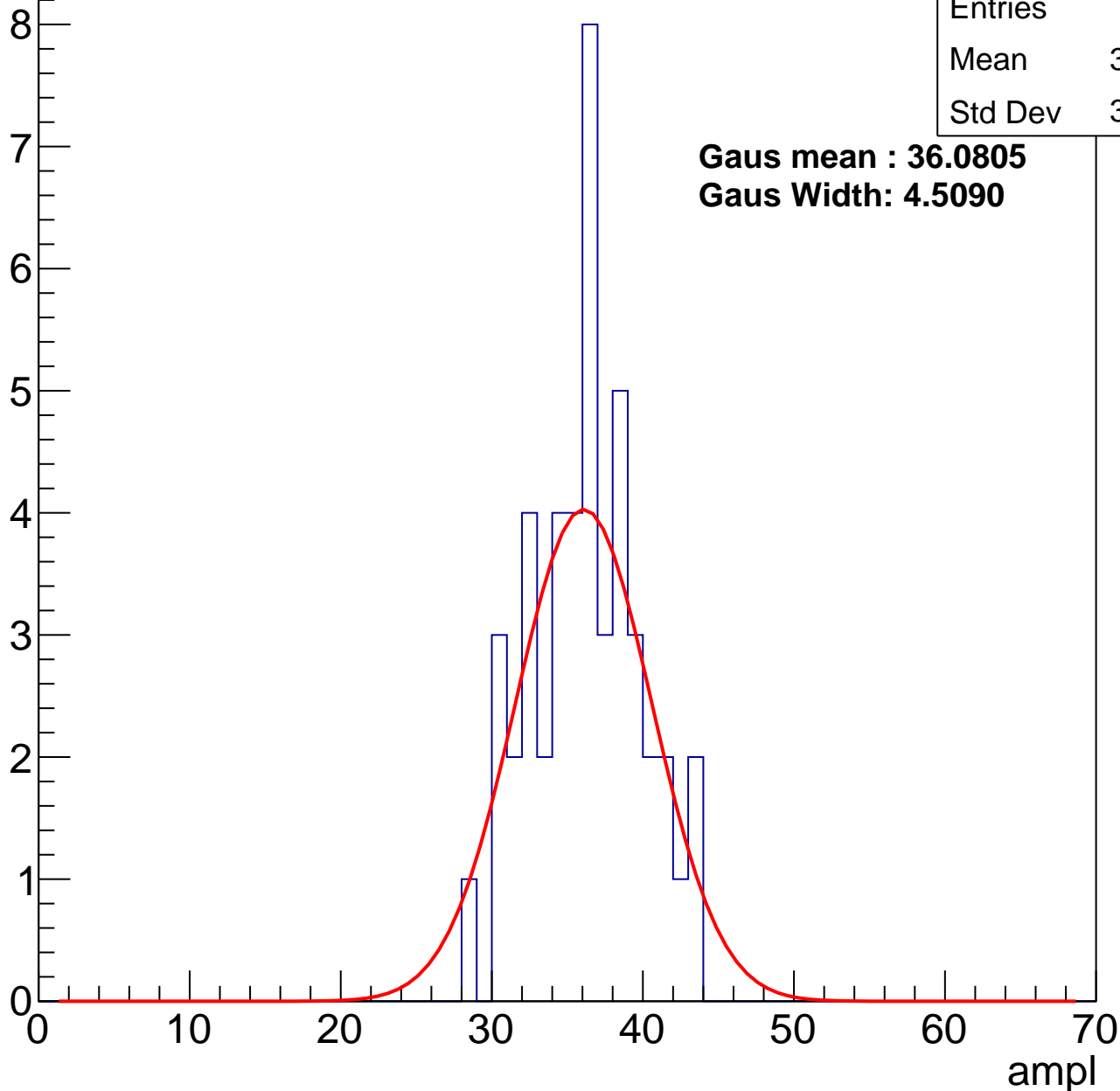
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	35.78
Std Dev	3.575

**Gaus mean : 36.0805**

**Gaus Width: 4.5090**



# B1L103S, U26-ch94, adc2

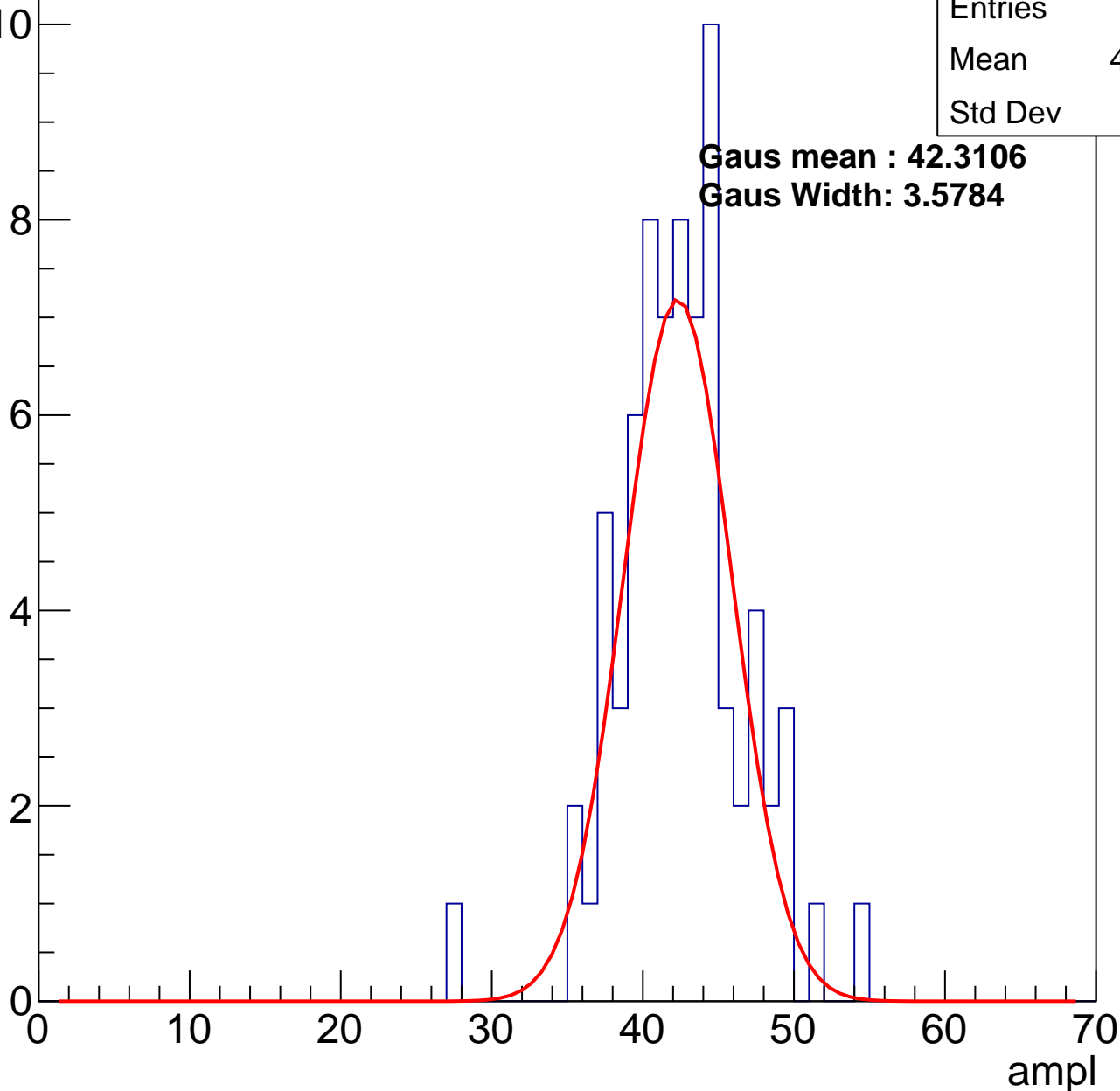
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	42.07
Std Dev	4.15

**Gaus mean : 42.3106**

**Gaus Width: 3.5784**

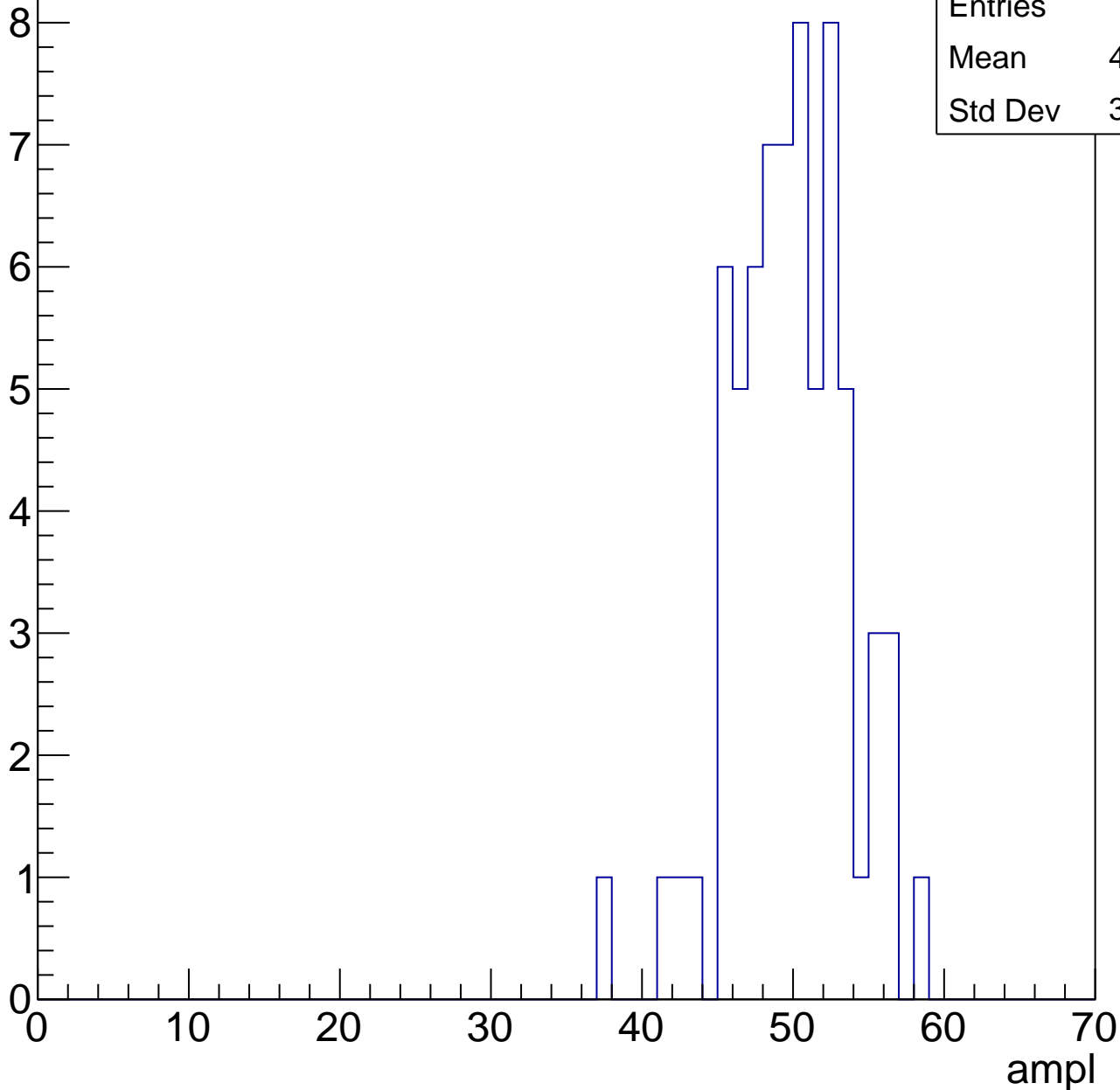


# B1L103S, U26-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	49.35
Std Dev	3.802

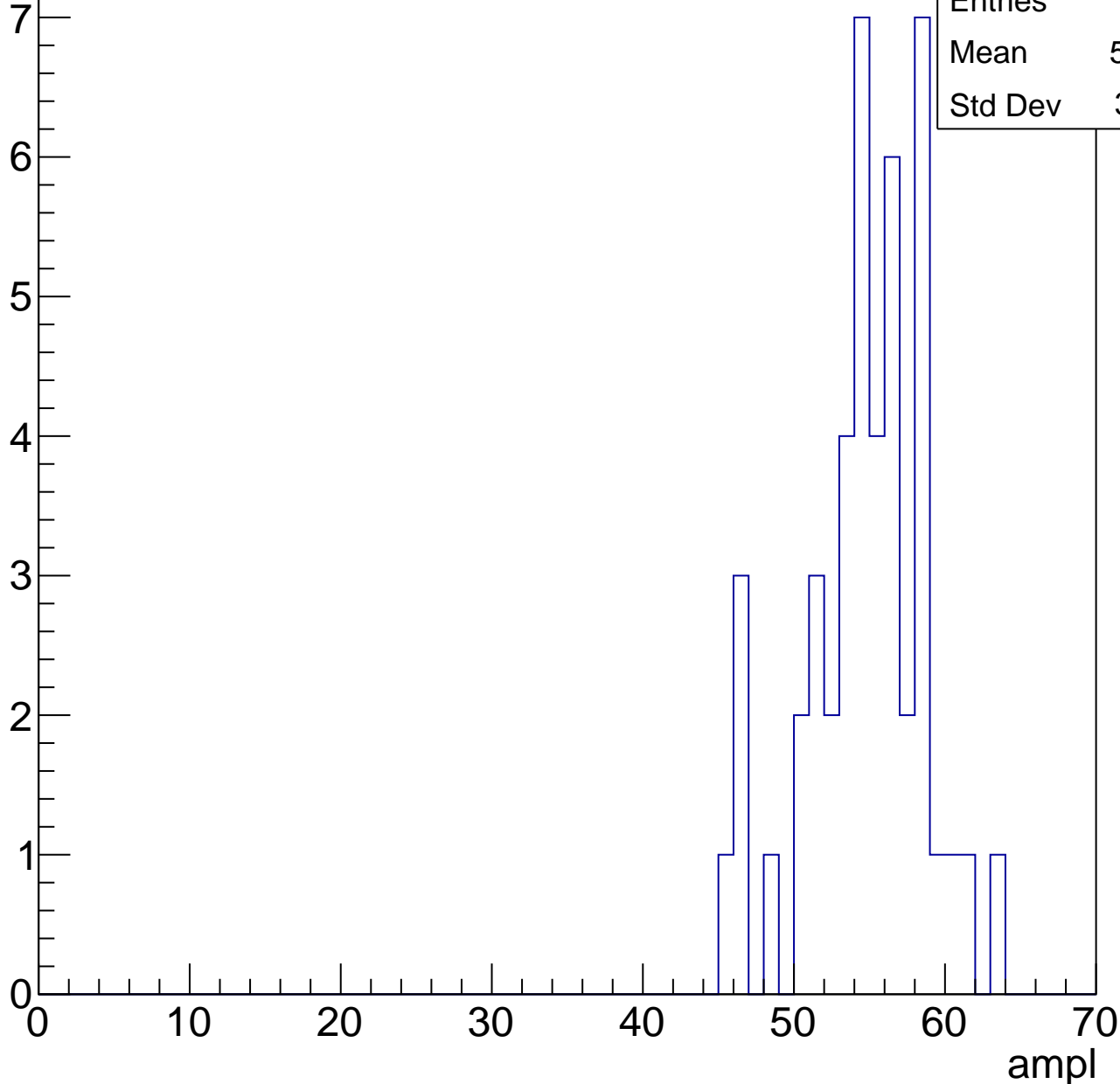


# B1L103S, U26-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

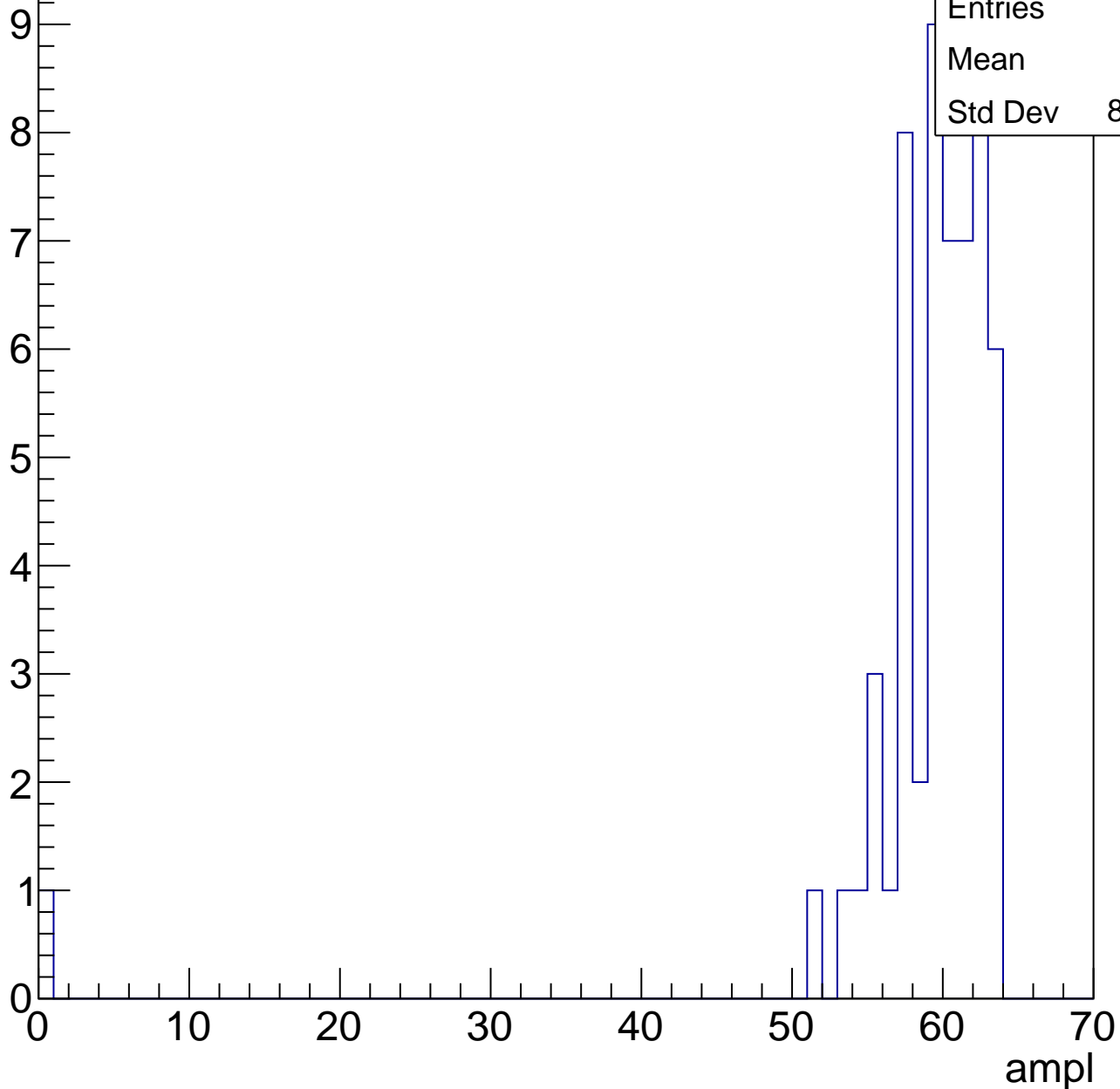
Entries	46
Mean	54.28
Std Dev	3.971



# B1L103S, U26-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



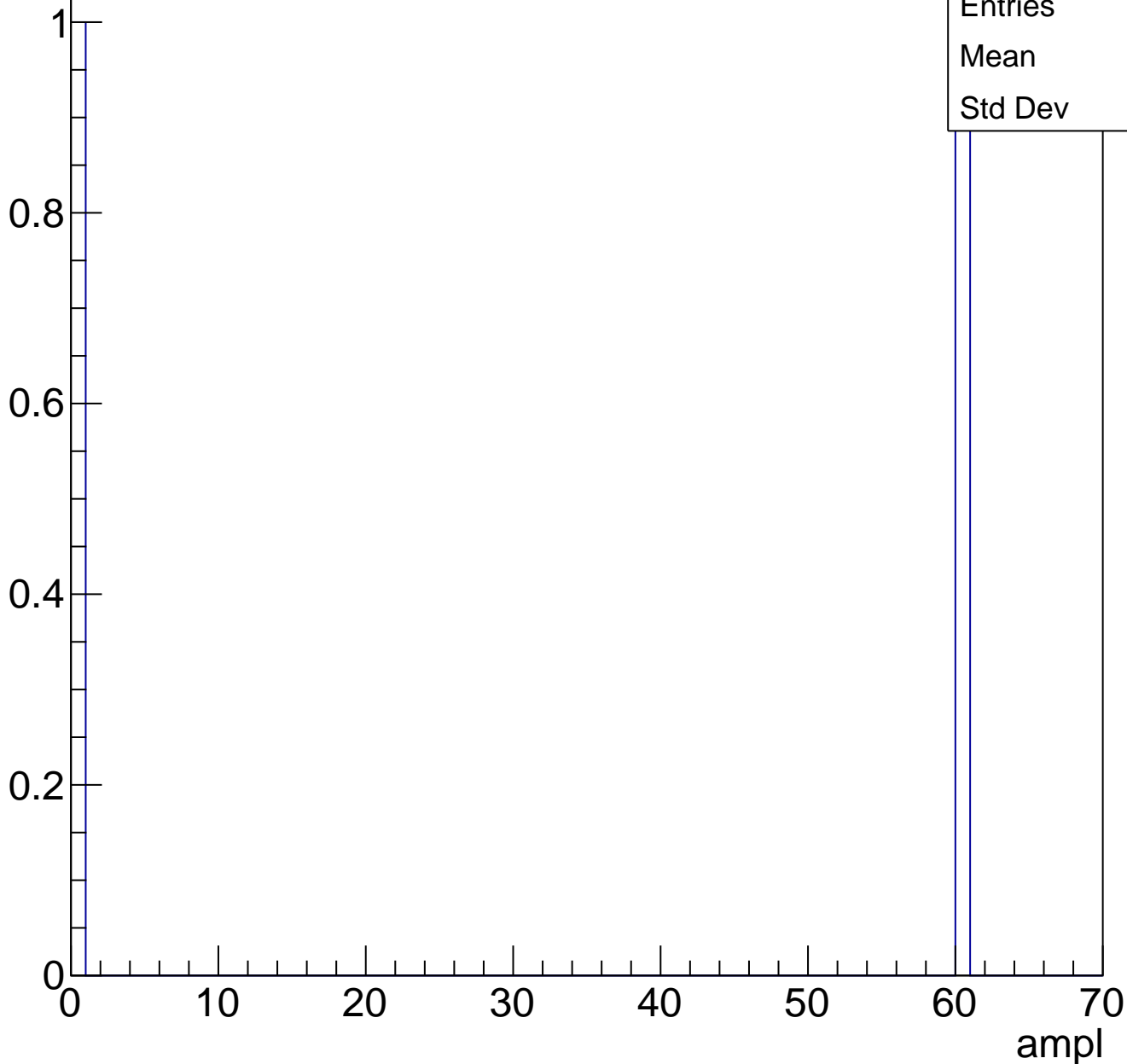
Entries	7
Mean	61.86
Std Dev	1.125



# B1L103S, U26-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch95, adc0

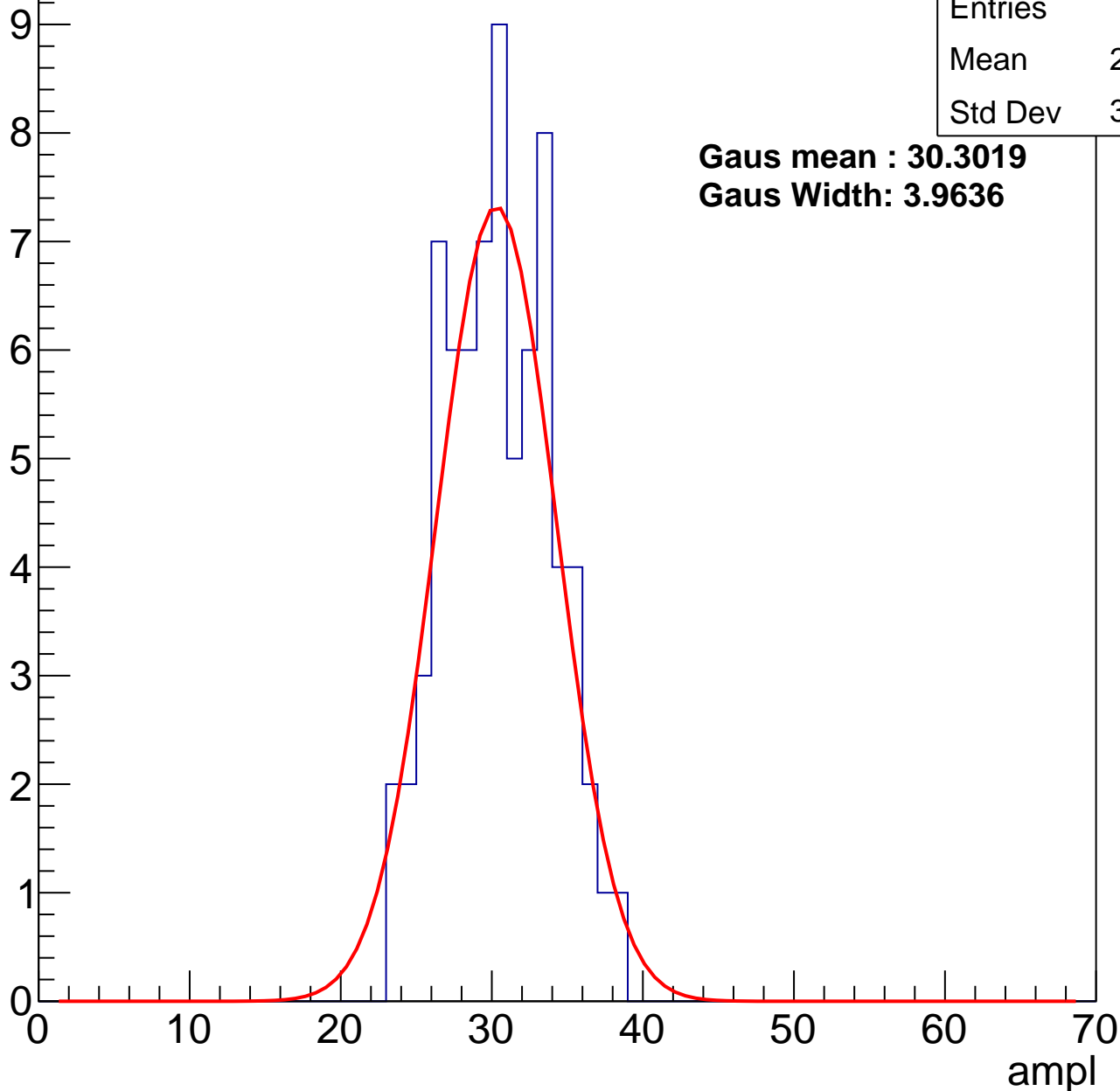
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	29.97
Std Dev	3.495

**Gaus mean : 30.3019**

**Gaus Width: 3.9636**



# B1L103S, U26-ch95, adc1

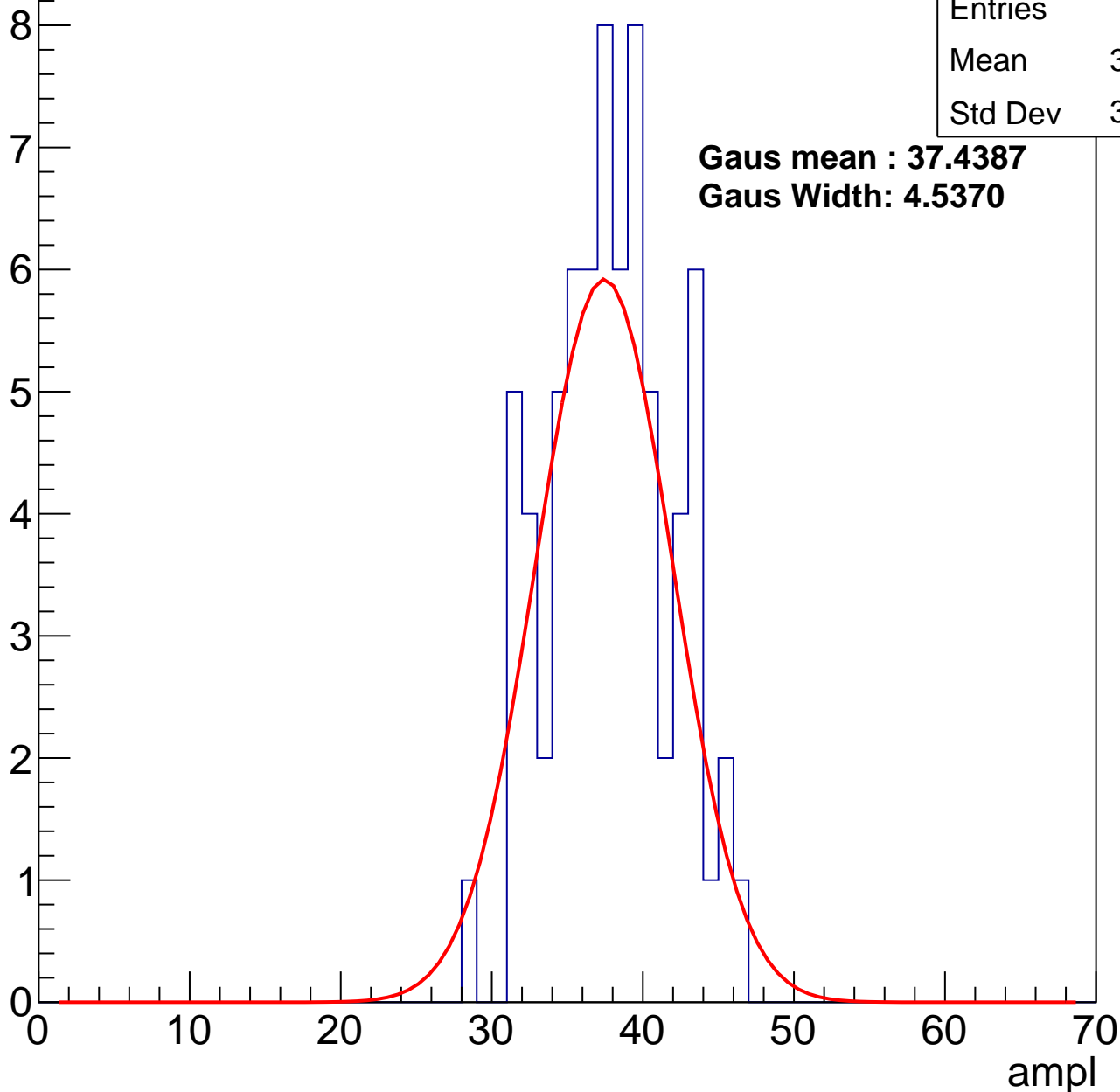
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	37.46
Std Dev	3.982

**Gaus mean : 37.4387**

**Gaus Width: 4.5370**



# B1L103S, U26-ch95, adc2

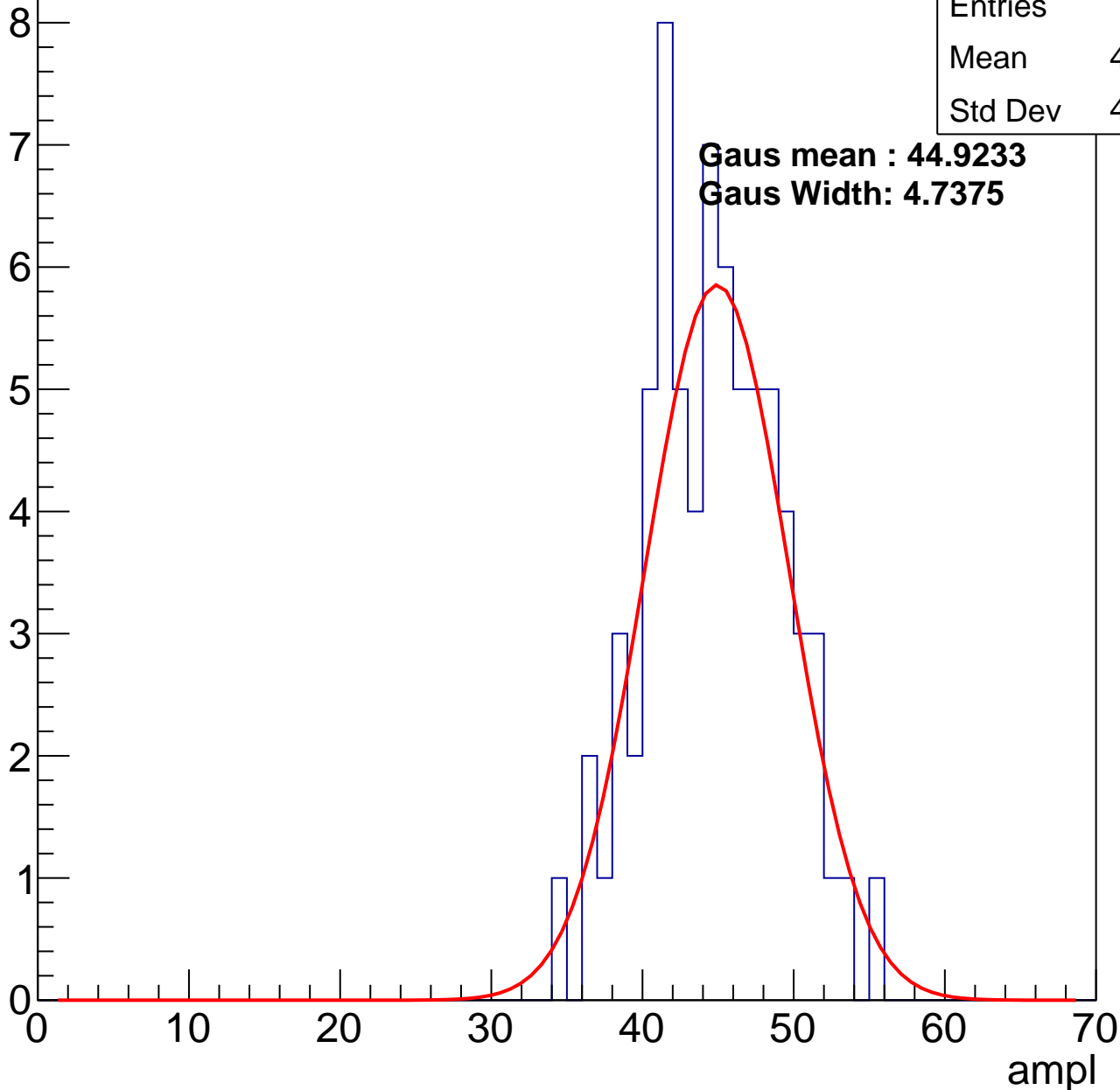
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	44.26
Std Dev	4.375

**Gaus mean : 44.9233**

**Gaus Width: 4.7375**

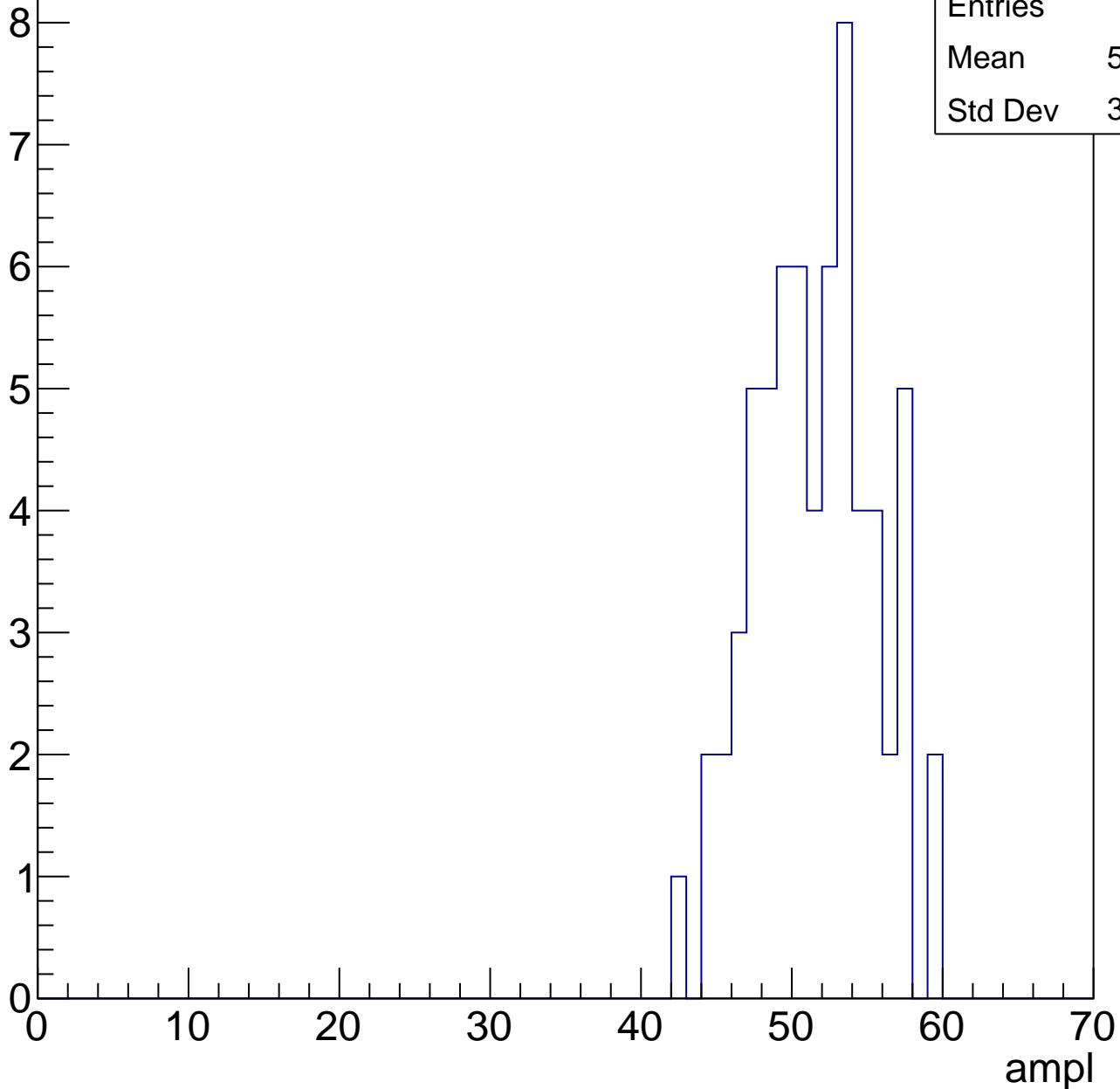


# B1L103S, U26-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	51.05
Std Dev	3.877

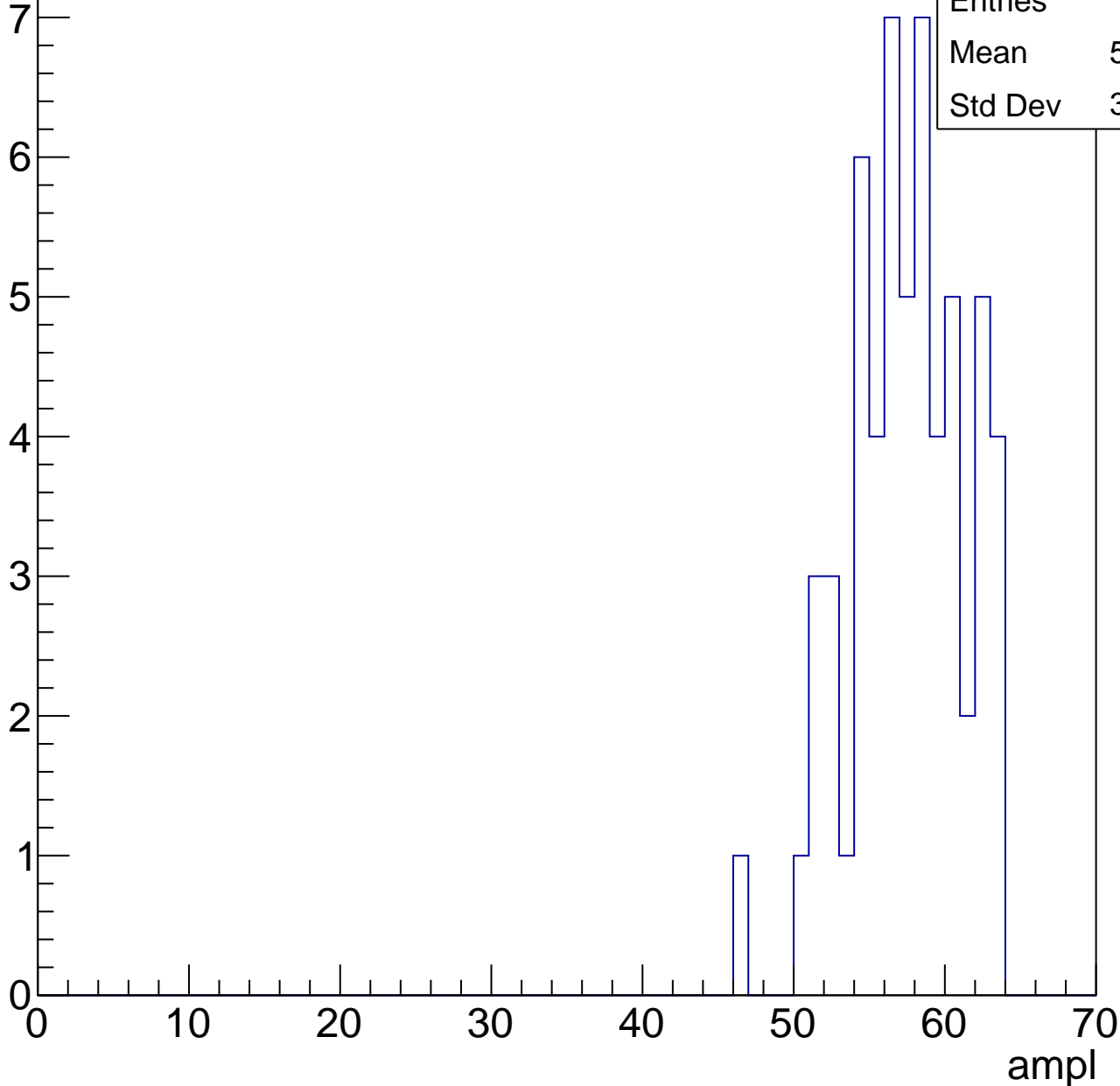


# B1L103S, U26-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	56.98
Std Dev	3.749

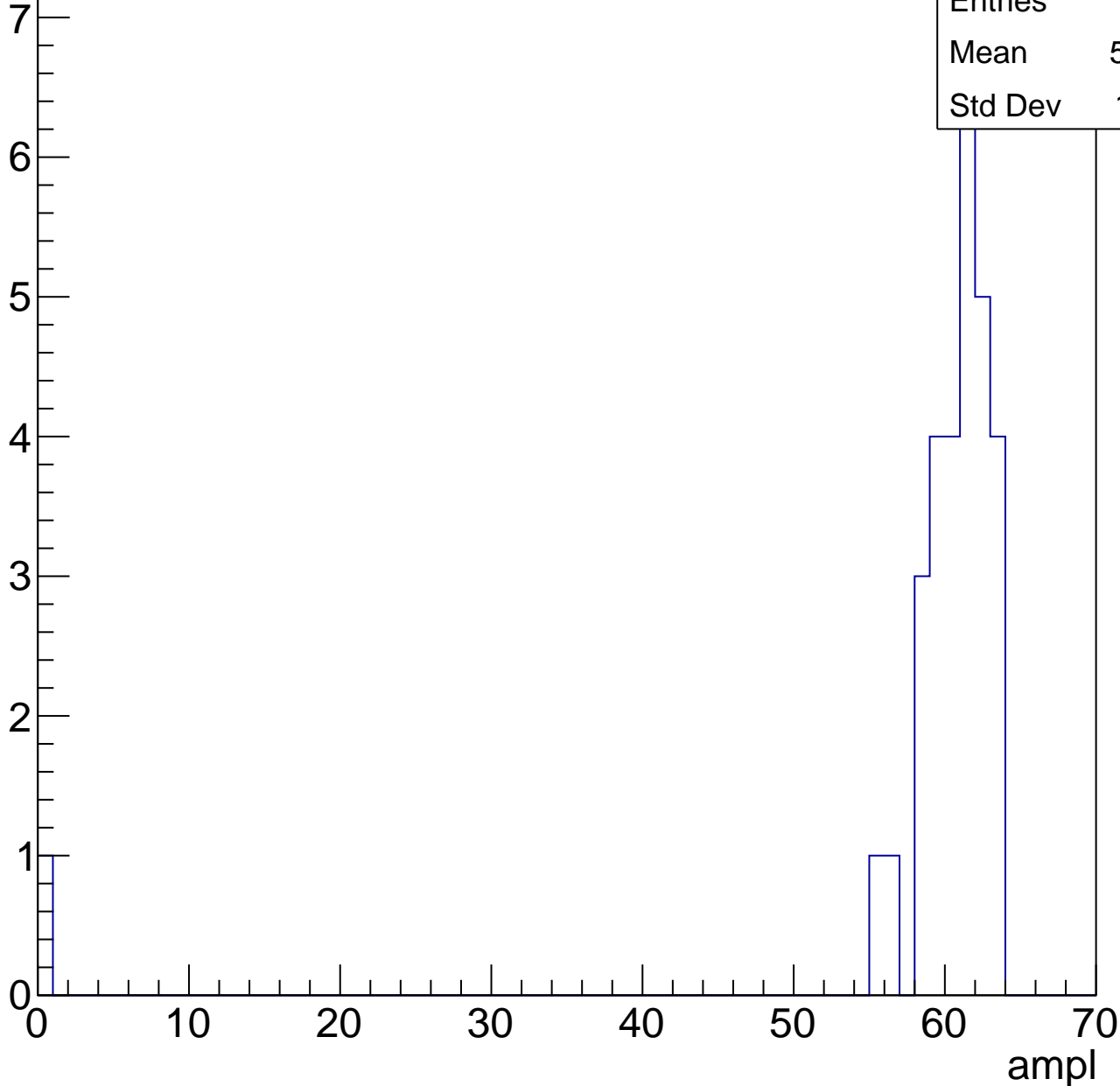


# B1L103S, U26-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	30
Mean	58.33
Std Dev	11.01



# B1L103S, U26-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch96, adc0

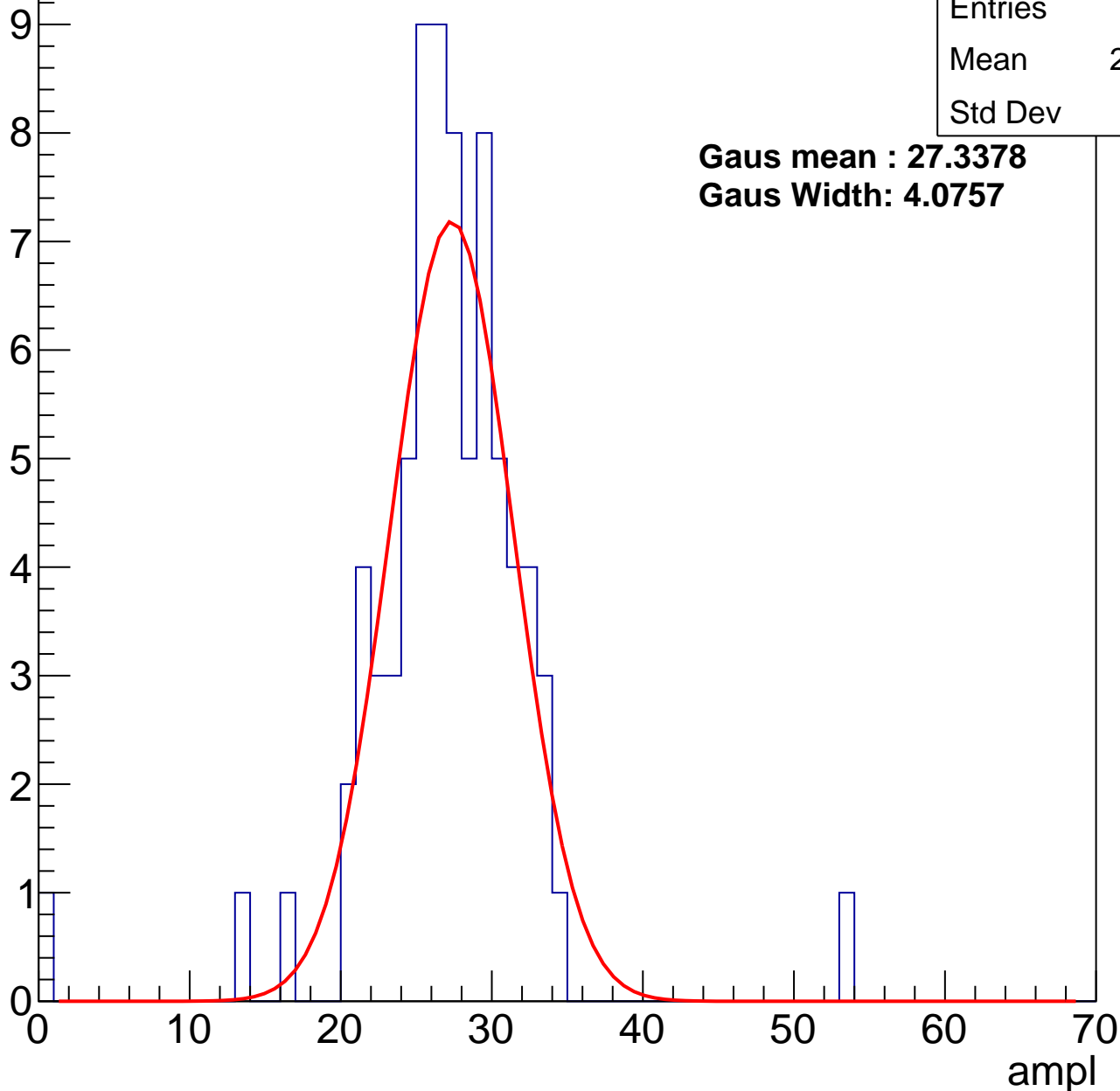
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	26.53
Std Dev	5.77

**Gaus mean : 27.3378**

**Gaus Width: 4.0757**



# B1L103S, U26-ch96, adc1

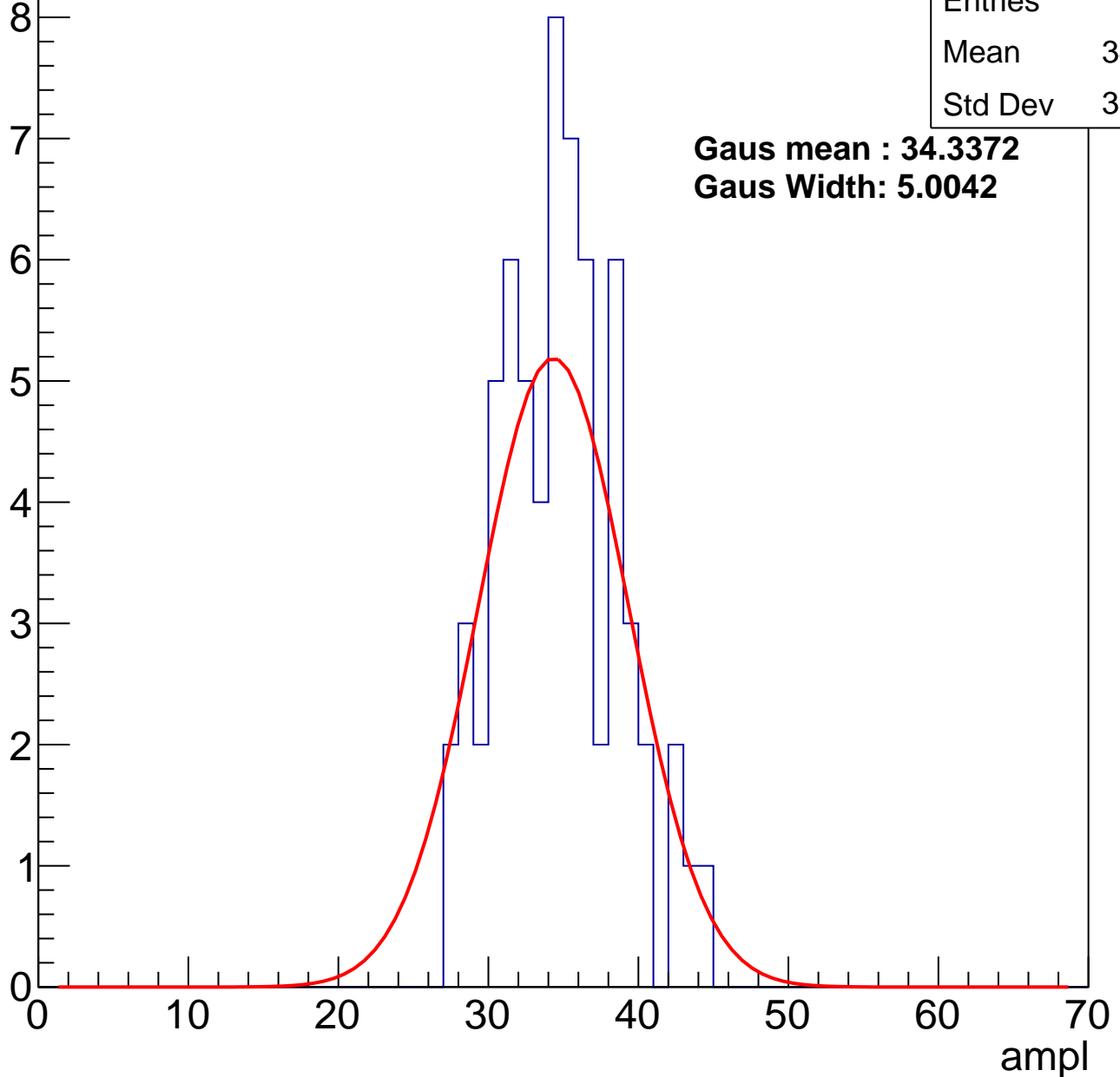
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	34.26
Std Dev	3.943

**Gaus mean : 34.3372**

**Gaus Width: 5.0042**



# B1L103S, U26-ch96, adc2

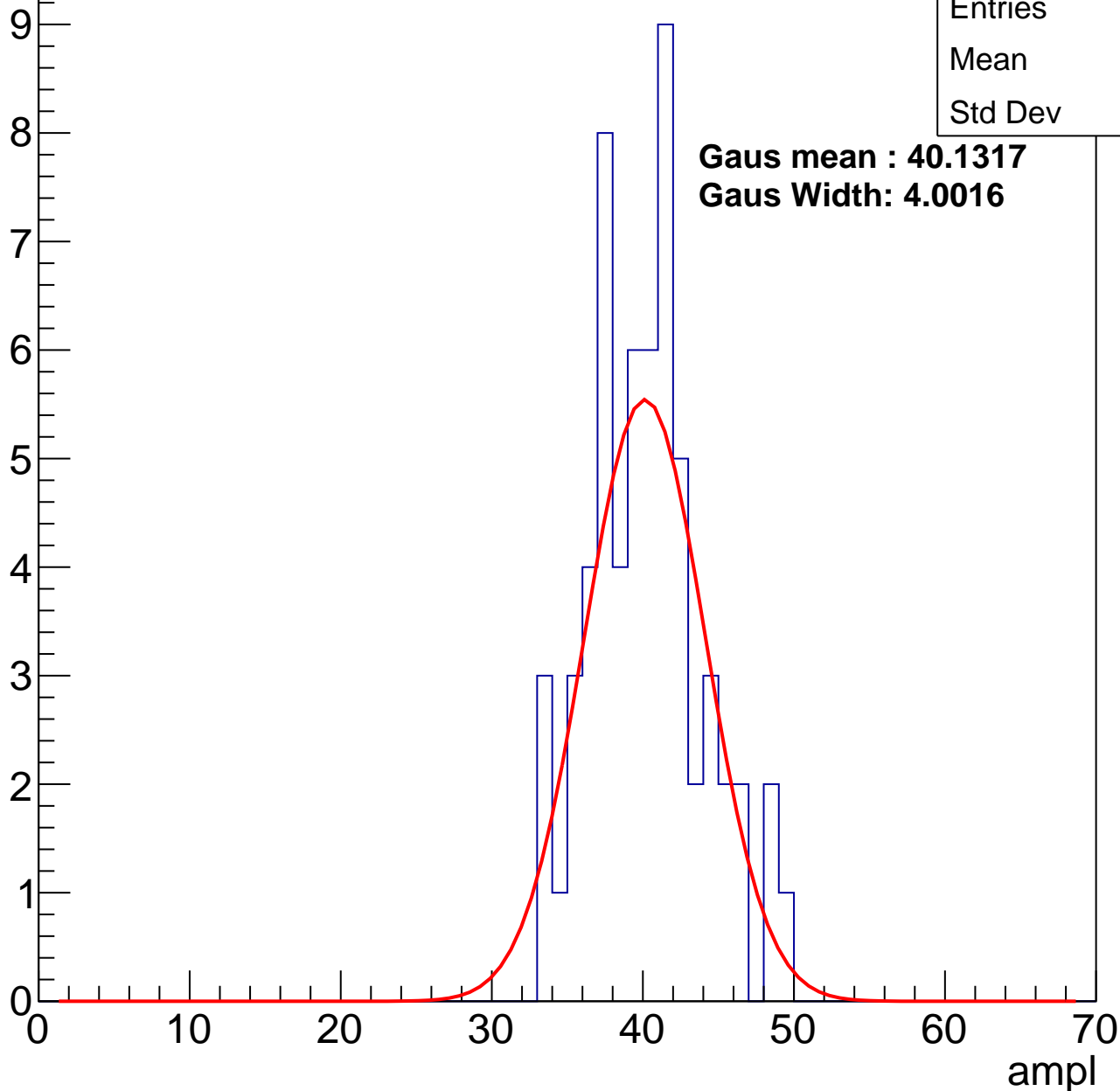
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	39.8
Std Dev	3.71

**Gaus mean : 40.1317**

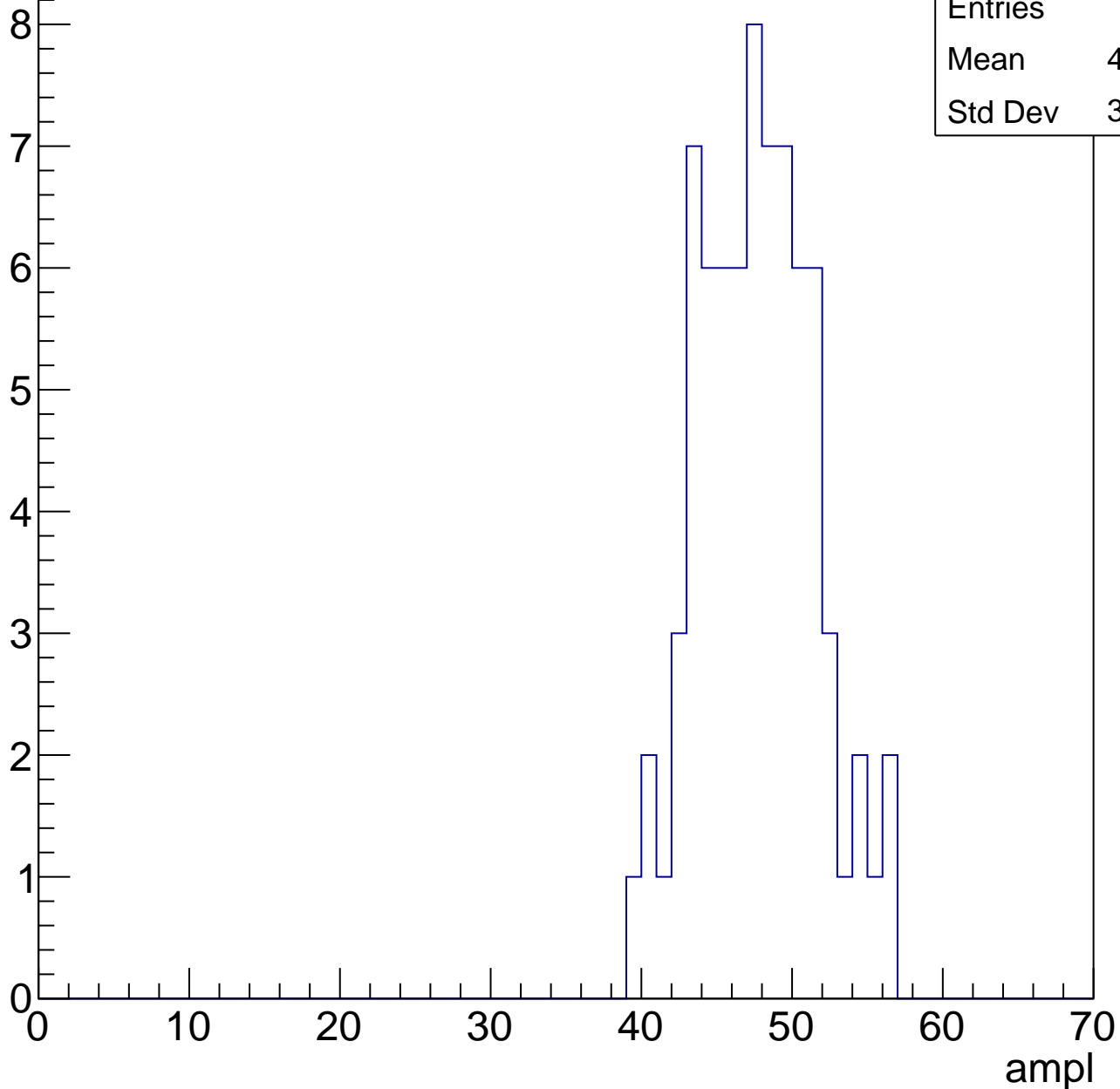
**Gaus Width: 4.0016**



# B1L103S, U26-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

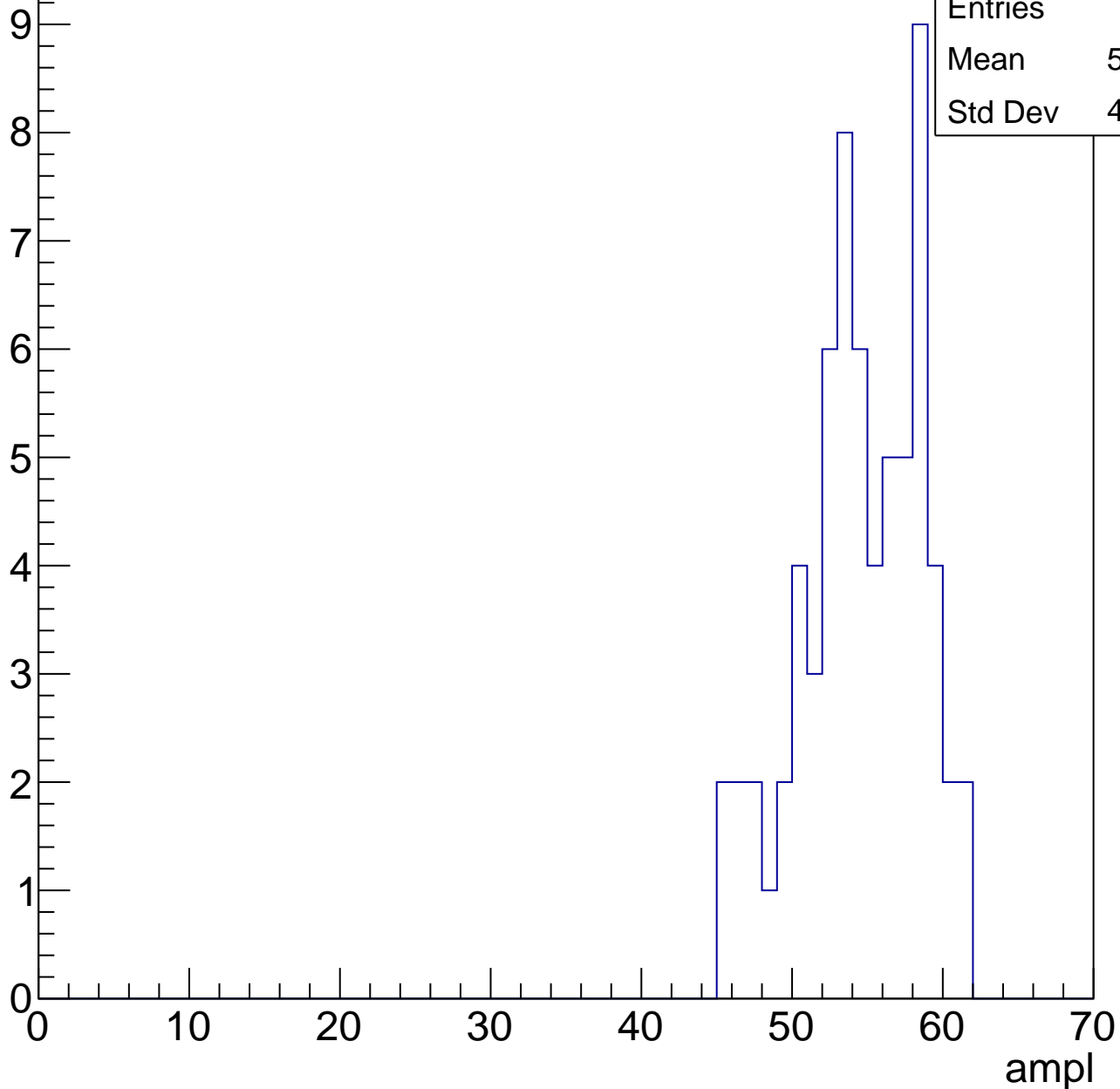


Entries	75
Mean	47.23
Std Dev	3.804

# B1L103S, U26-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

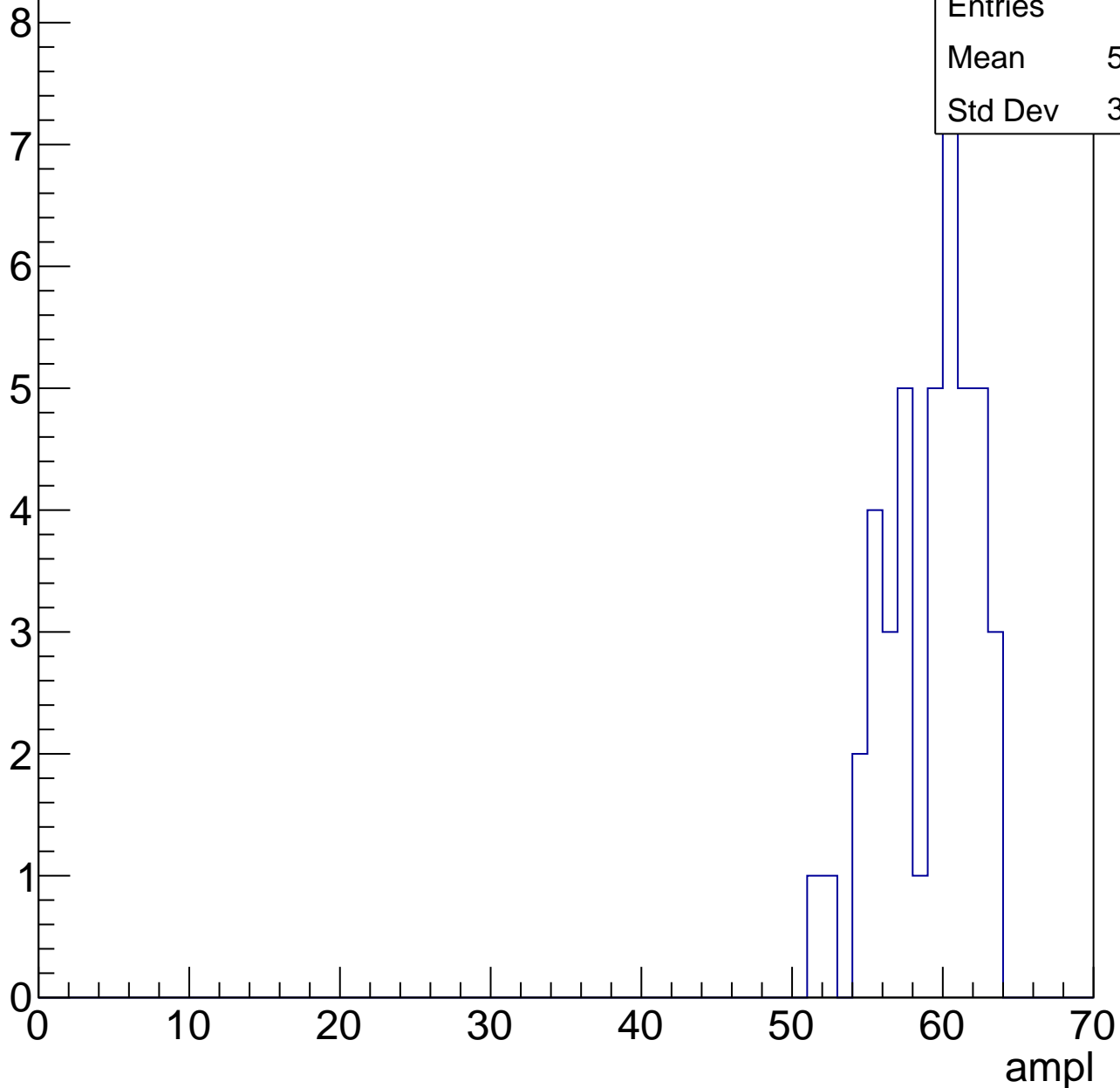


Entries	67
Mean	54.03
Std Dev	4.015

# B1L103S, U26-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

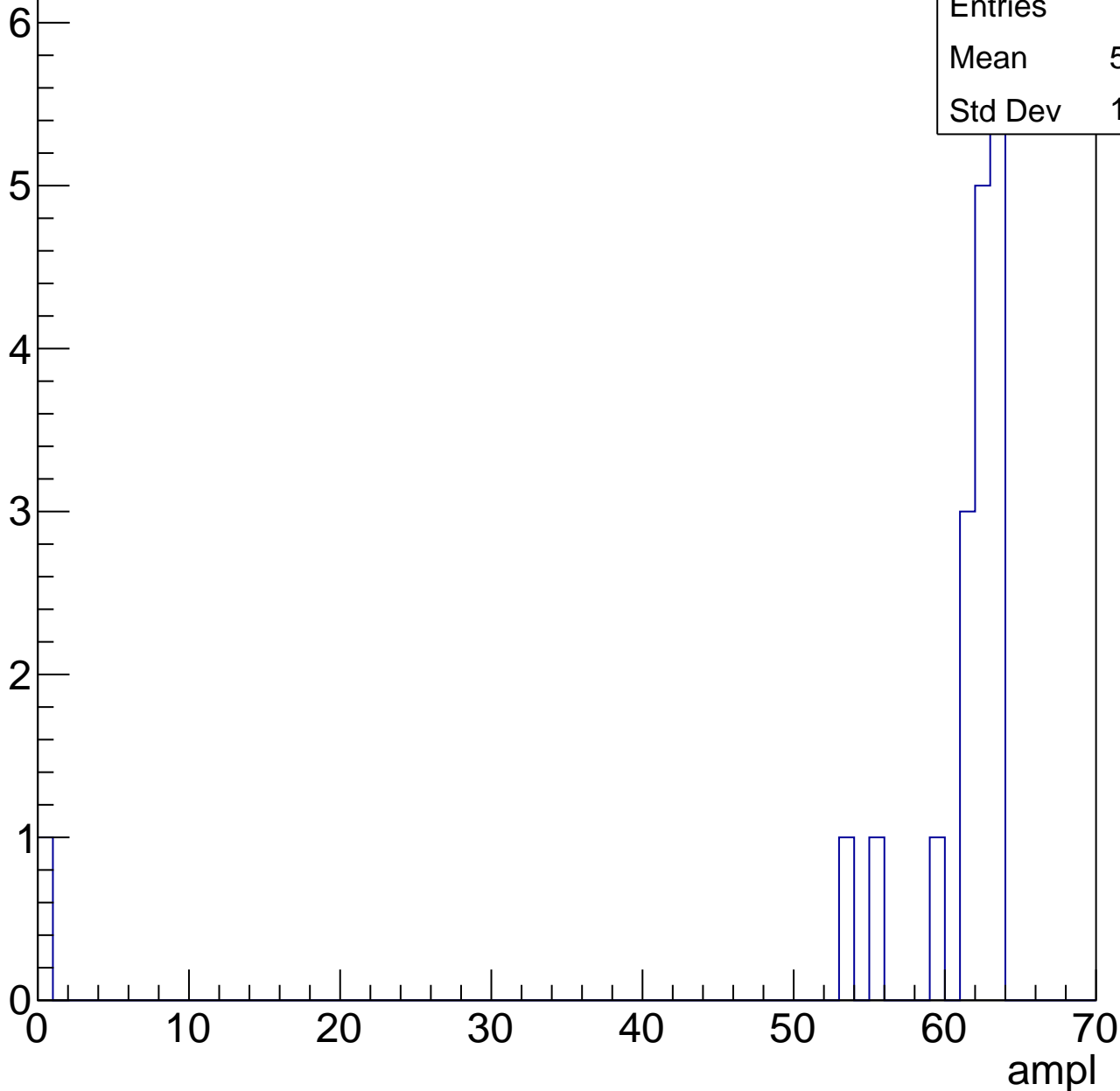


# B1L103S, U26-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	18
Mean	57.67
Std Dev	14.25





# B1L103S, U26-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch97, adc0

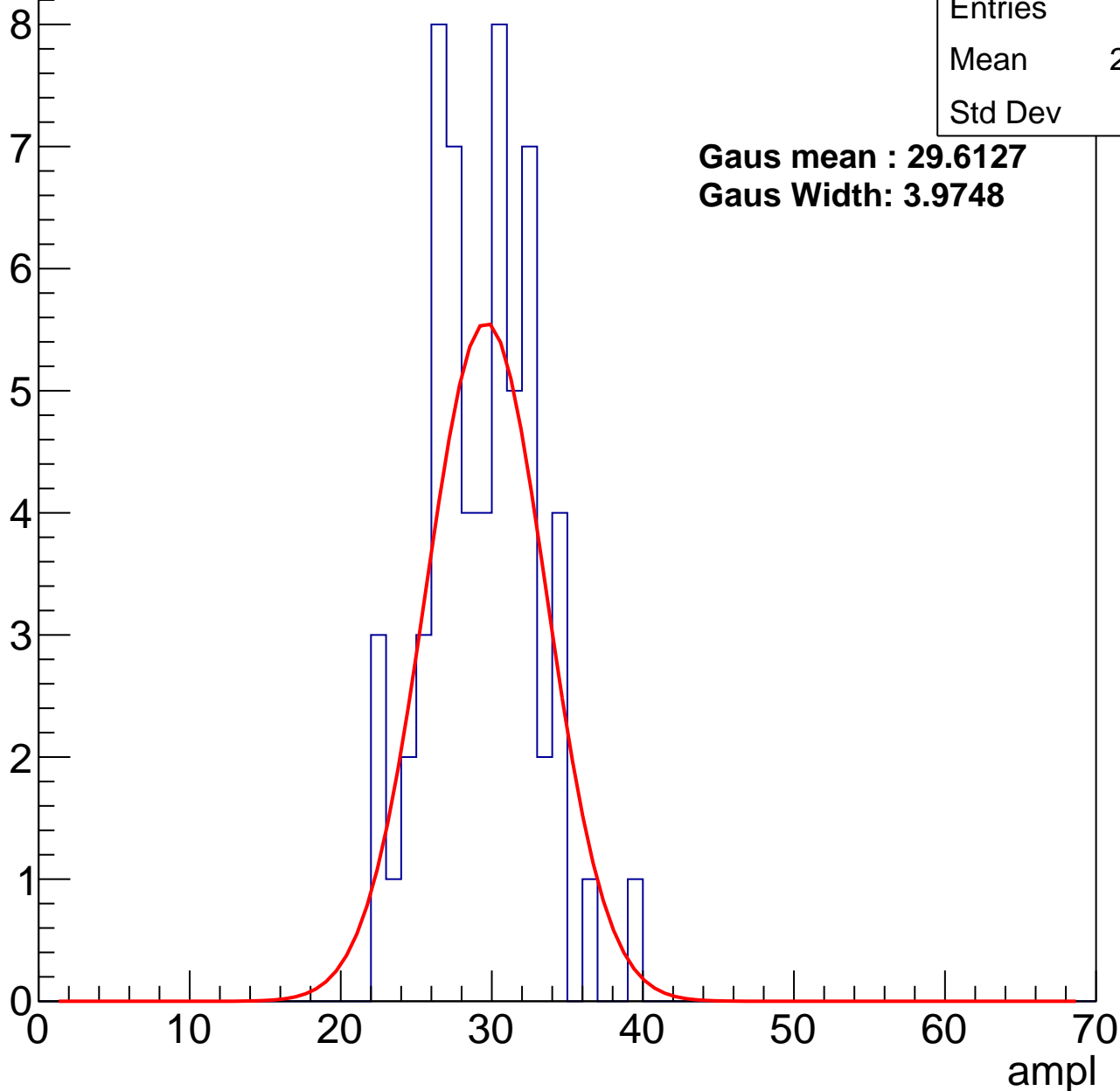
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	28.88
Std Dev	3.55

**Gaus mean : 29.6127**

**Gaus Width: 3.9748**



# B1L103S, U26-ch97, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	73
Mean	34.96
Std Dev	4.163

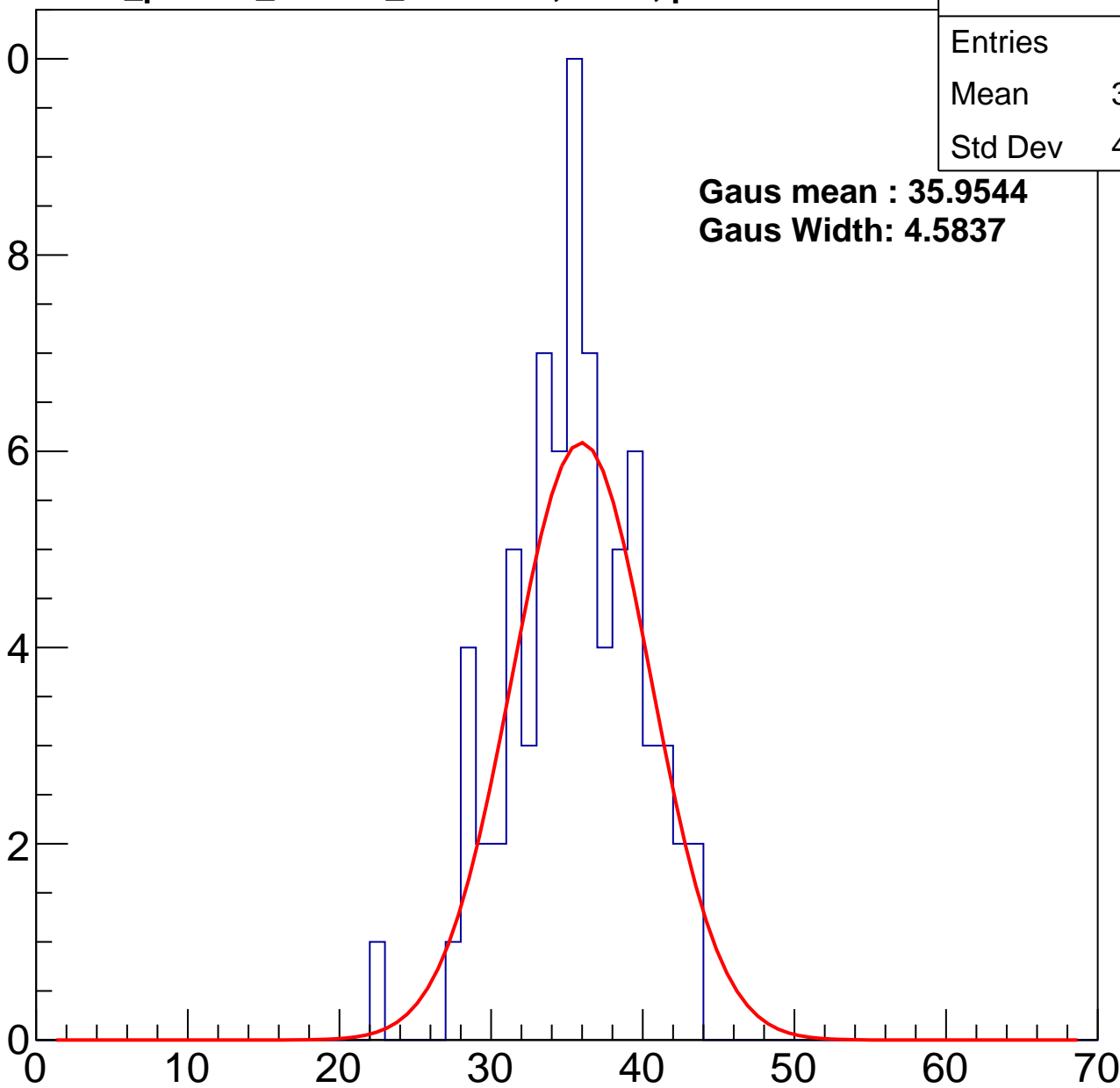
**Gaus mean : 35.9544**

**Gaus Width: 4.5837**

Entry

10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch97, adc2

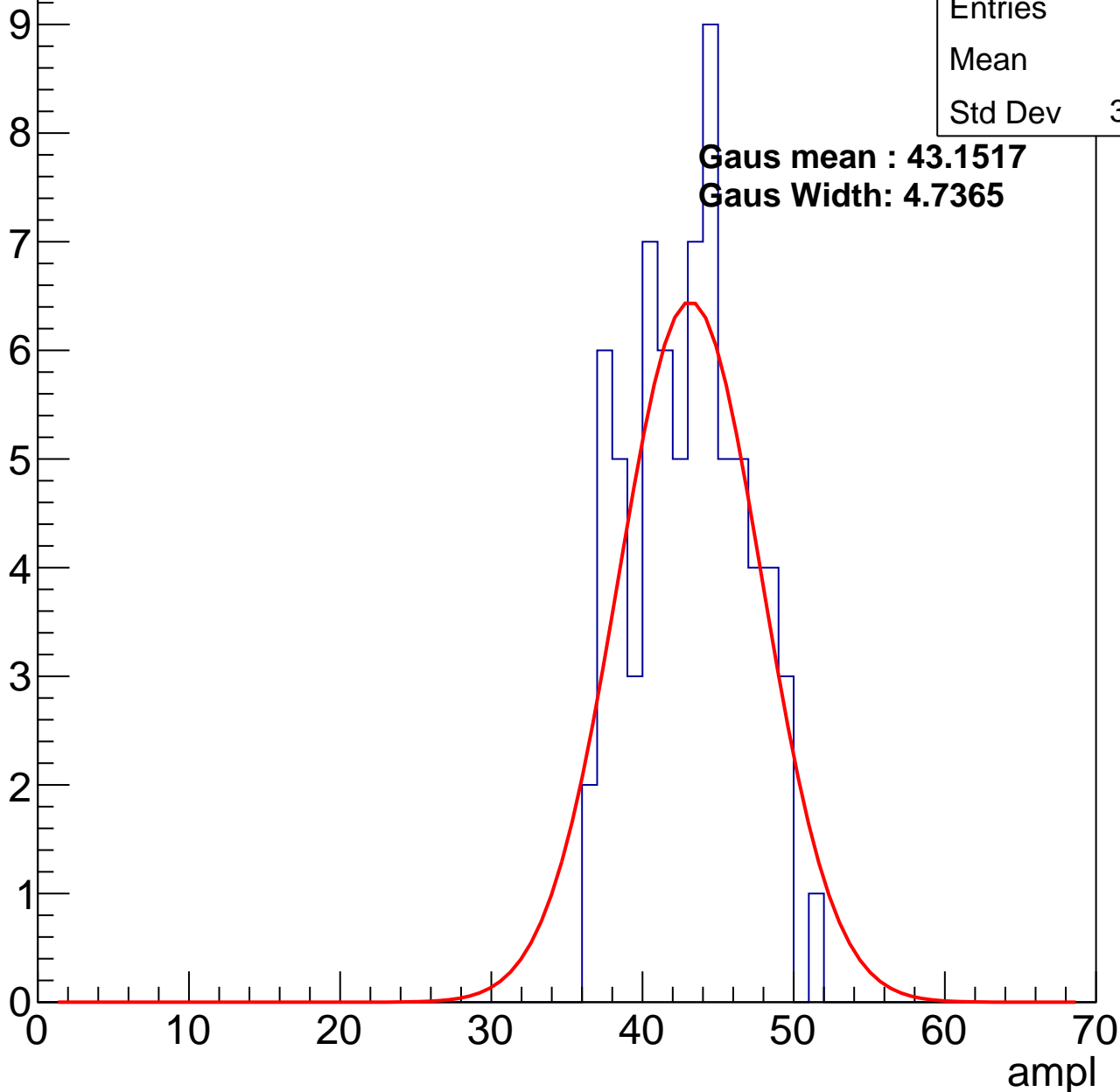
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	72
Mean	42.6
Std Dev	3.684

**Gaus mean : 43.1517**

**Gaus Width: 4.7365**



# B1L103S, U26-ch97, adc3

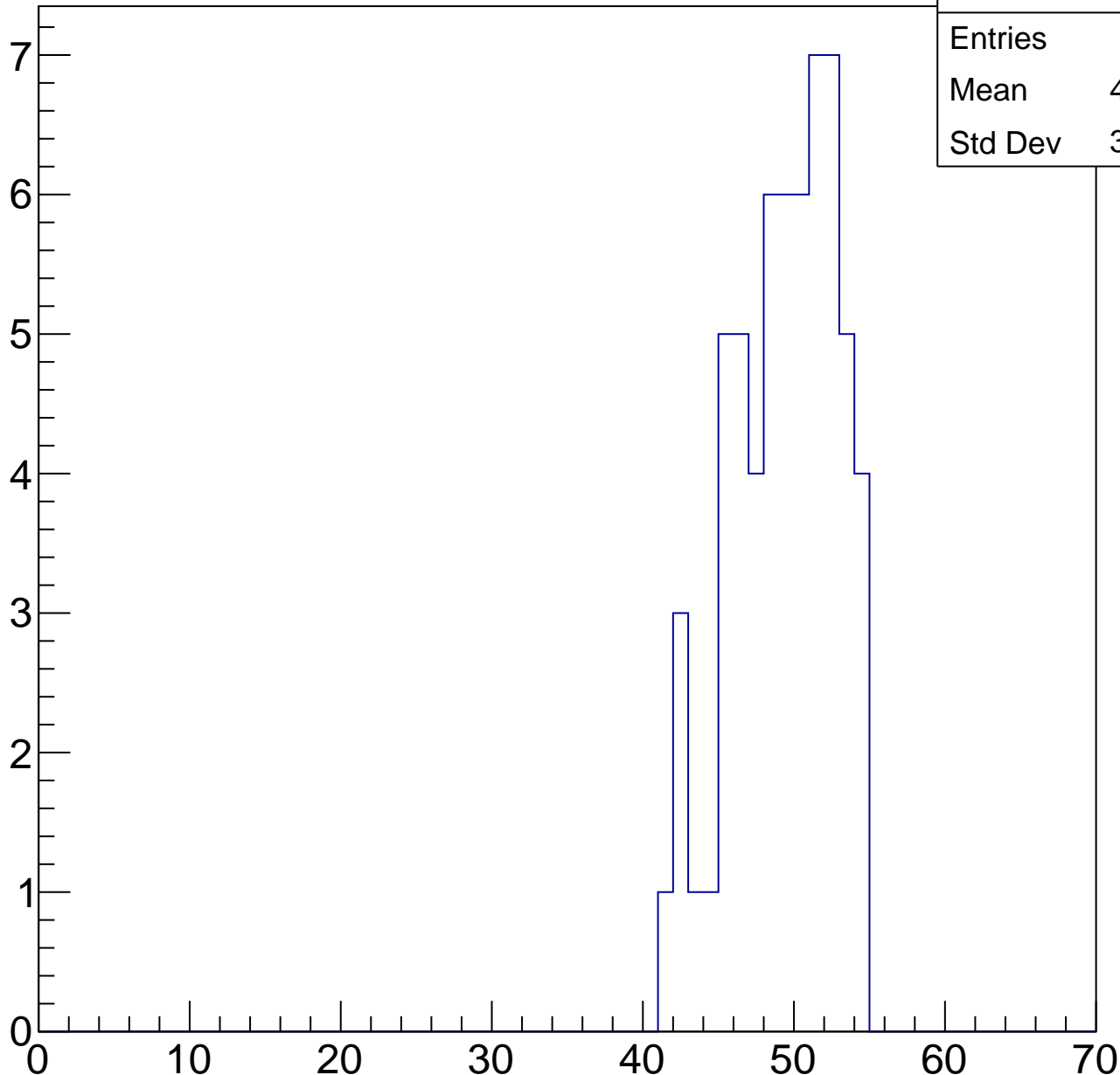
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	61
Mean	48.87
Std Dev	3.375

ampl

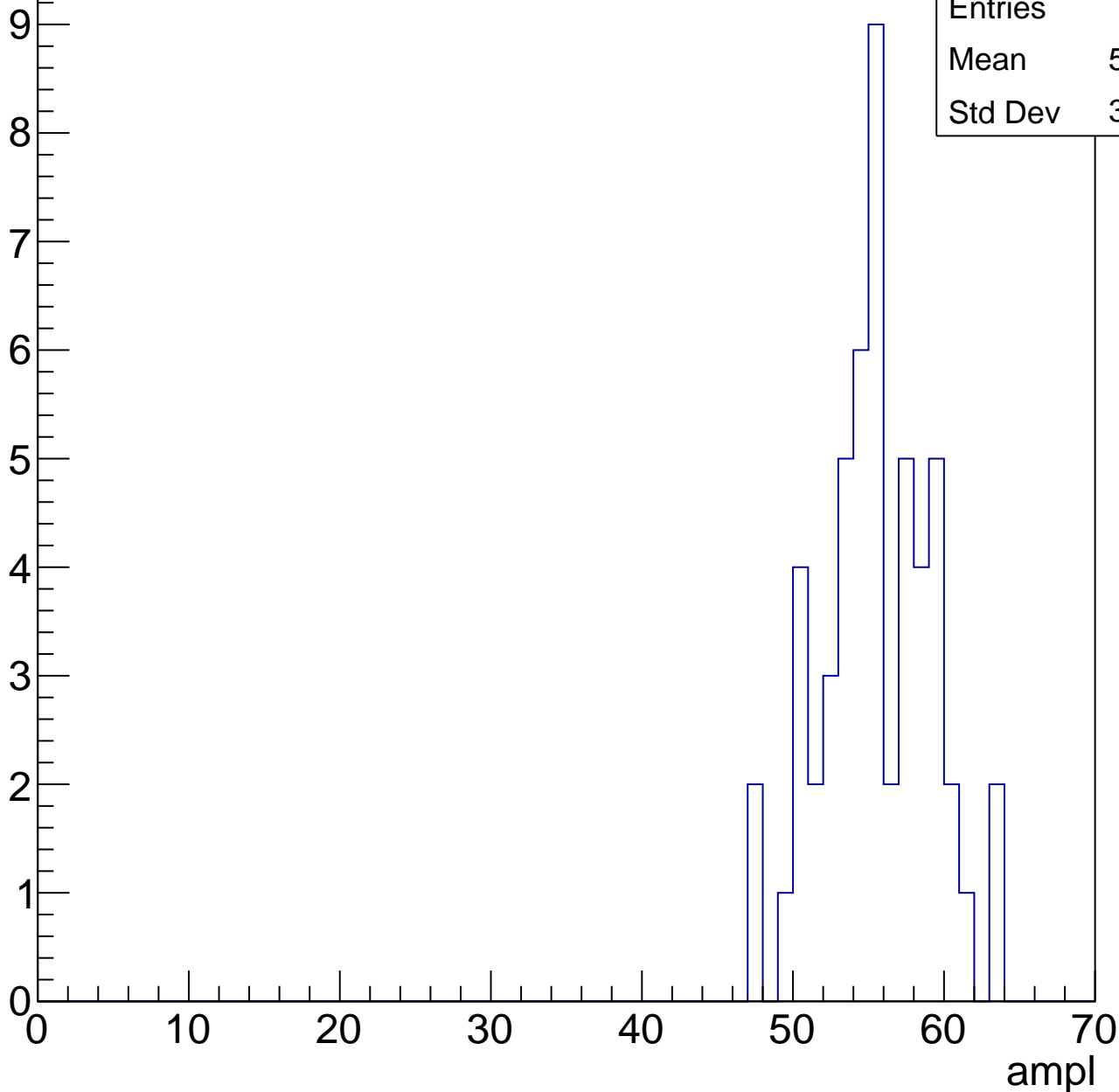


# B1L103S, U26-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	55.02
Std Dev	3.637



# B1L103S, U26-ch97, adc5

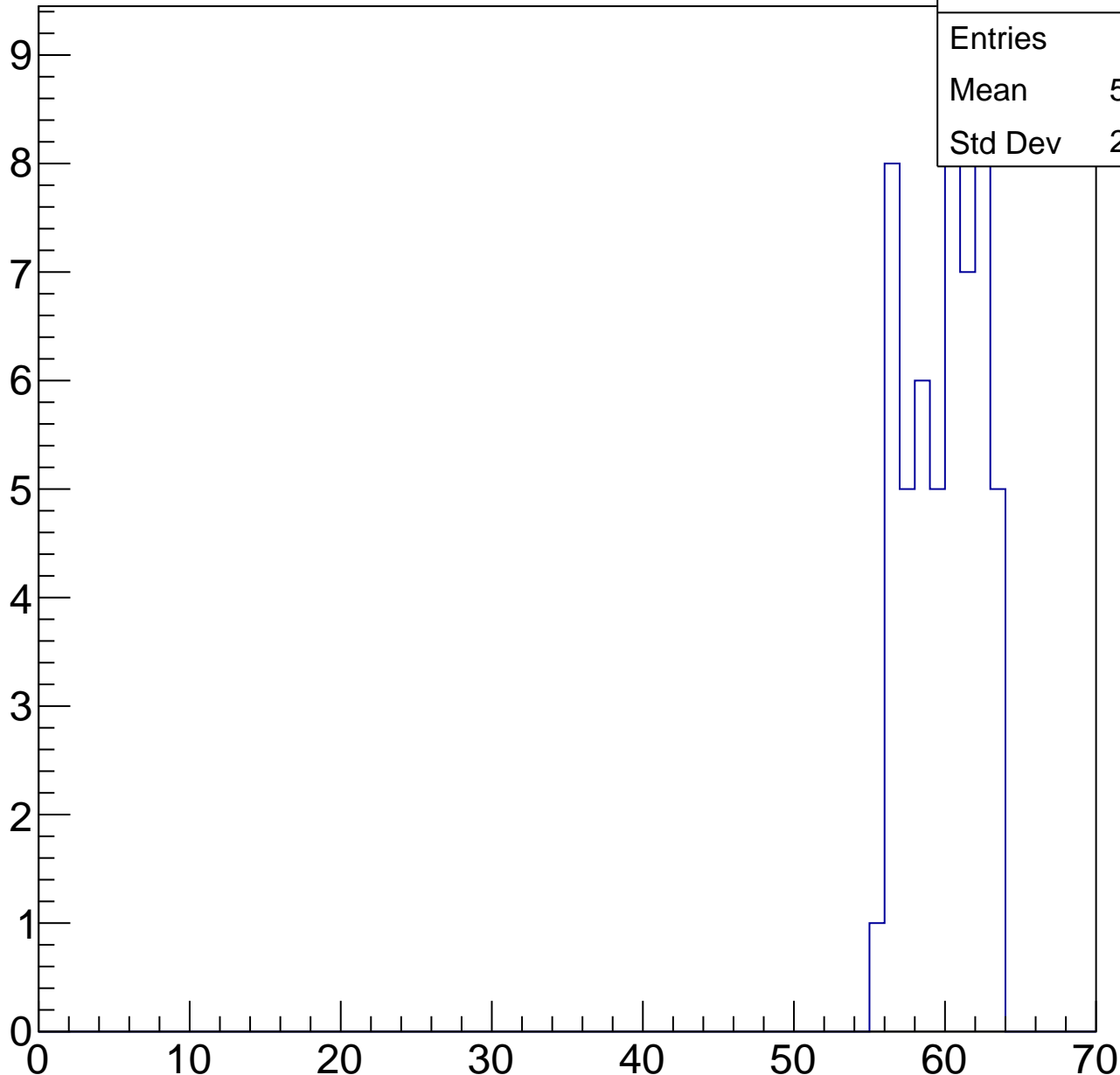
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	54
Mean	59.46
Std Dev	2.355

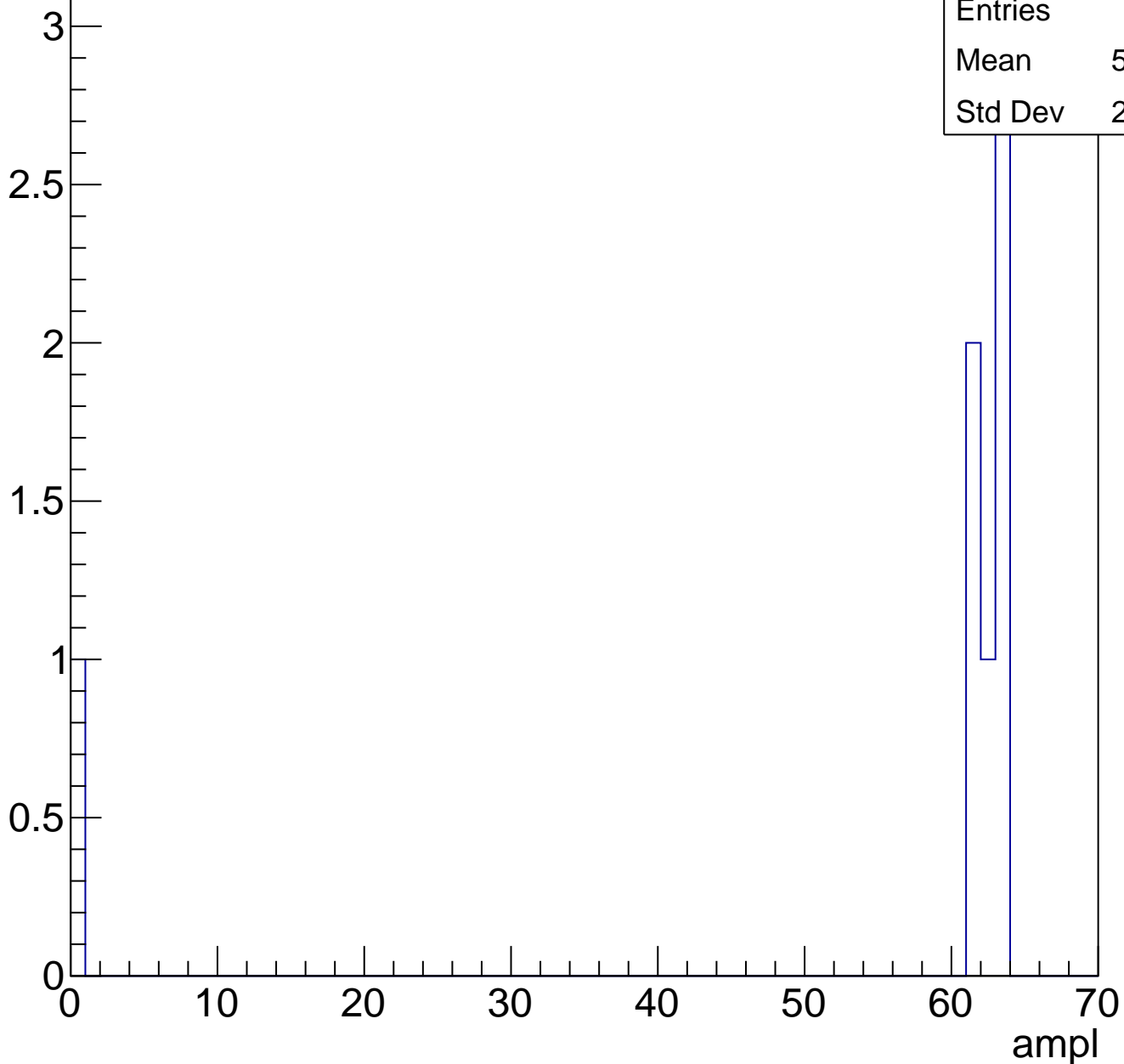
ampl



# B1L103S, U26-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U26-ch98, adc0

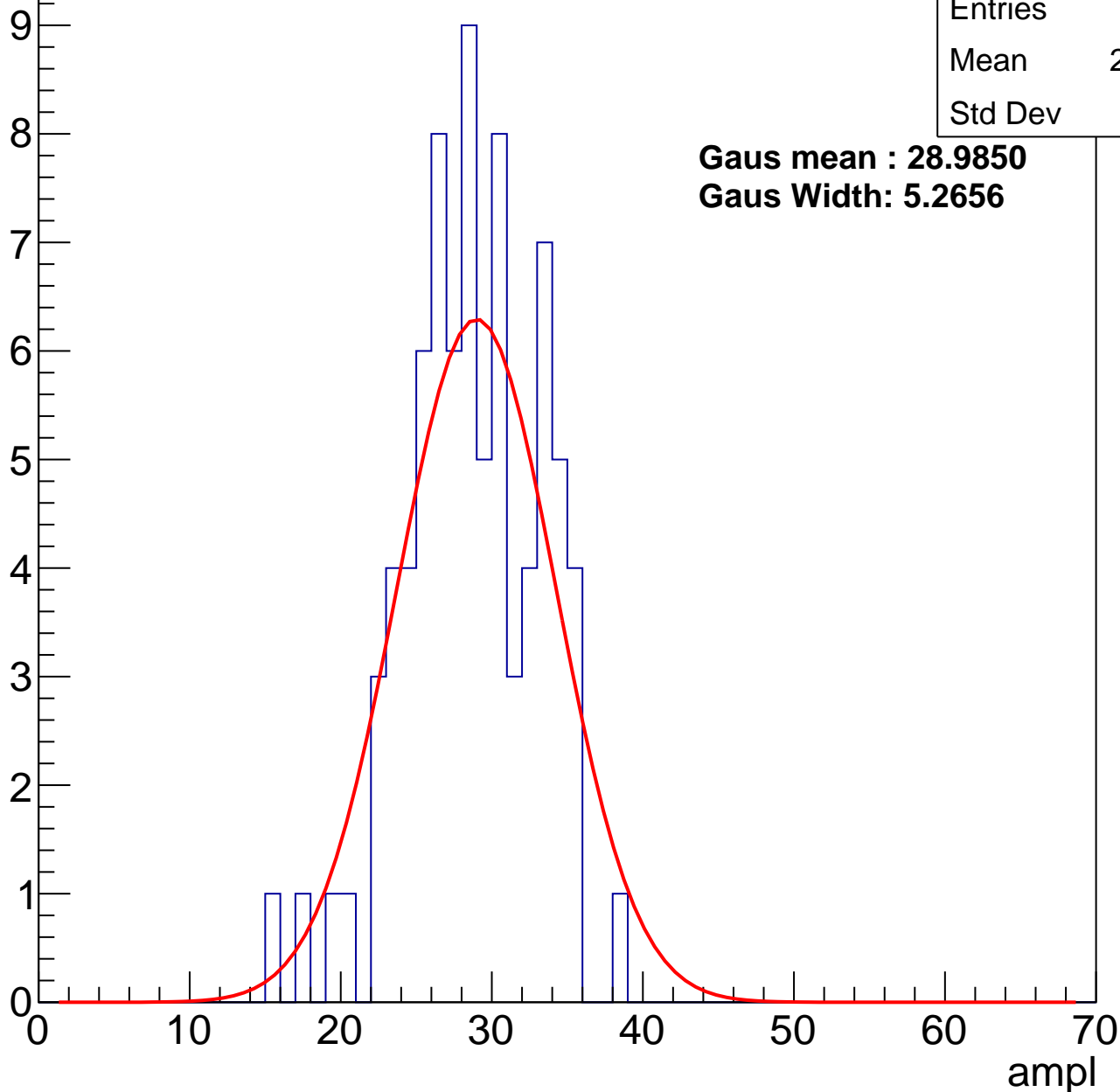
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	81
Mean	28.17
Std Dev	4.41

**Gaus mean : 28.9850**

**Gaus Width: 5.2656**



# B1L103S, U26-ch98, adc1

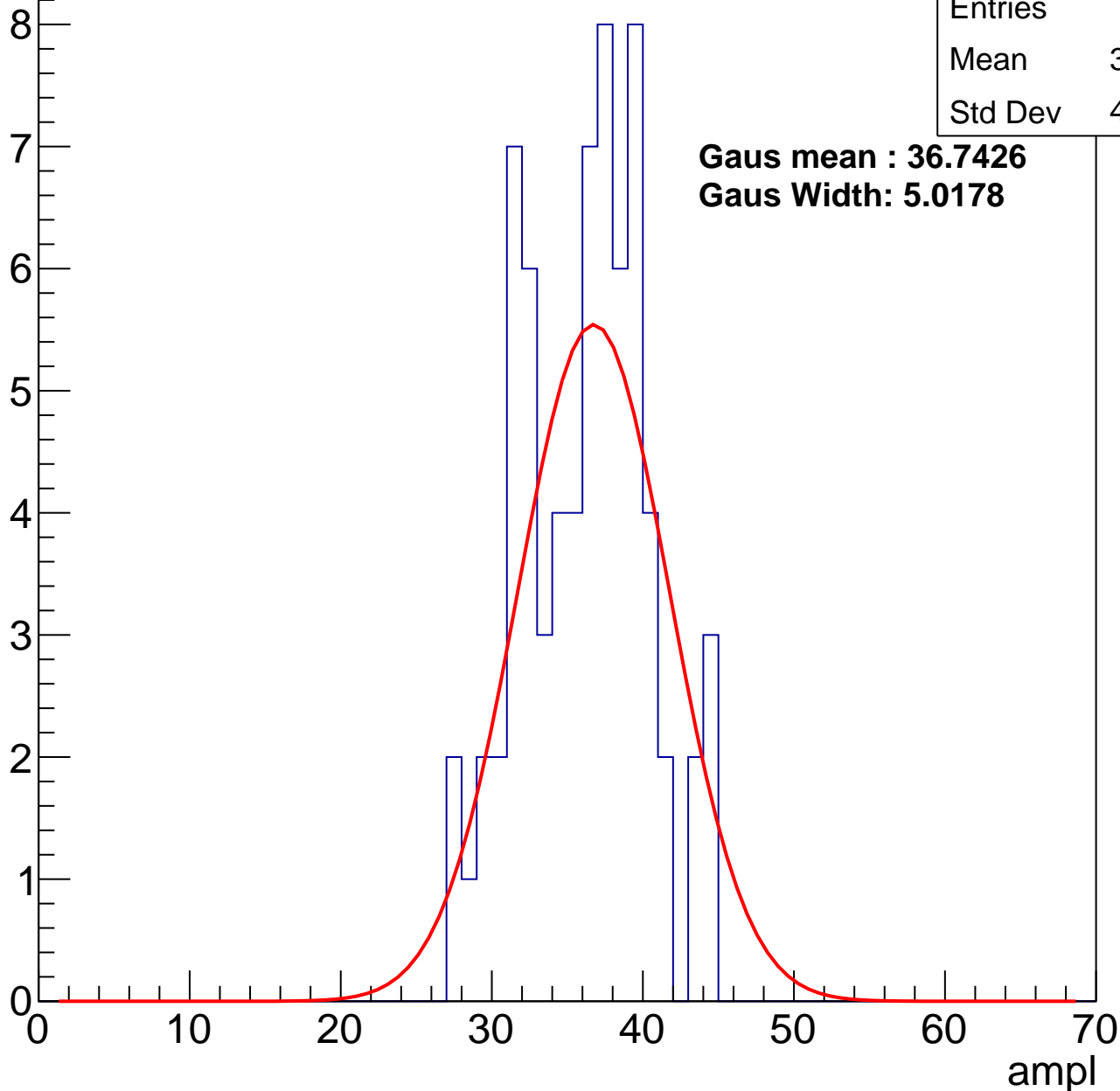
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	35.66
Std Dev	4.135

**Gaus mean : 36.7426**

**Gaus Width: 5.0178**



# B1L103S, U26-ch98, adc2

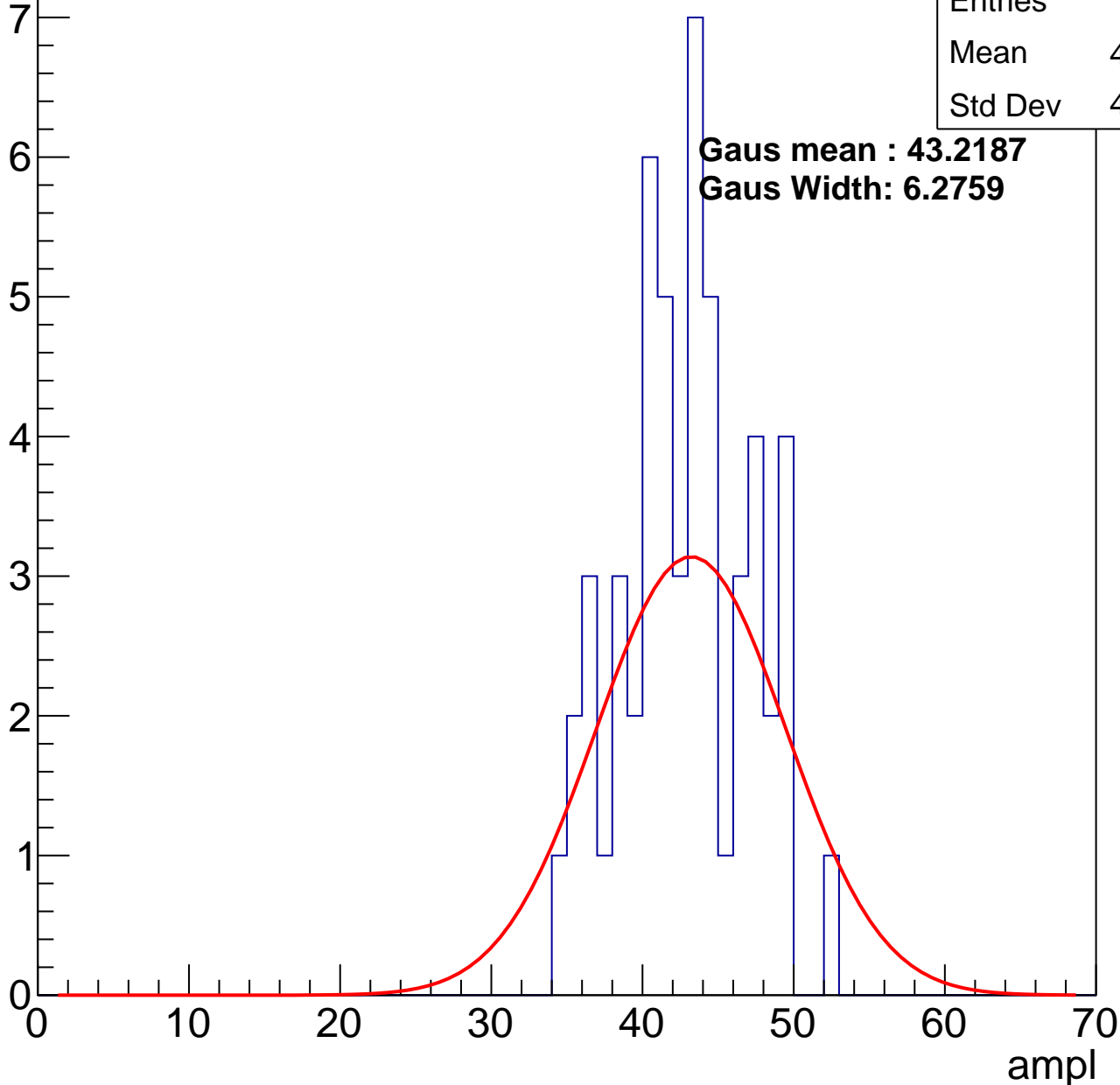
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	42.42
Std Dev	4.195

**Gaus mean : 43.2187**

**Gaus Width: 6.2759**

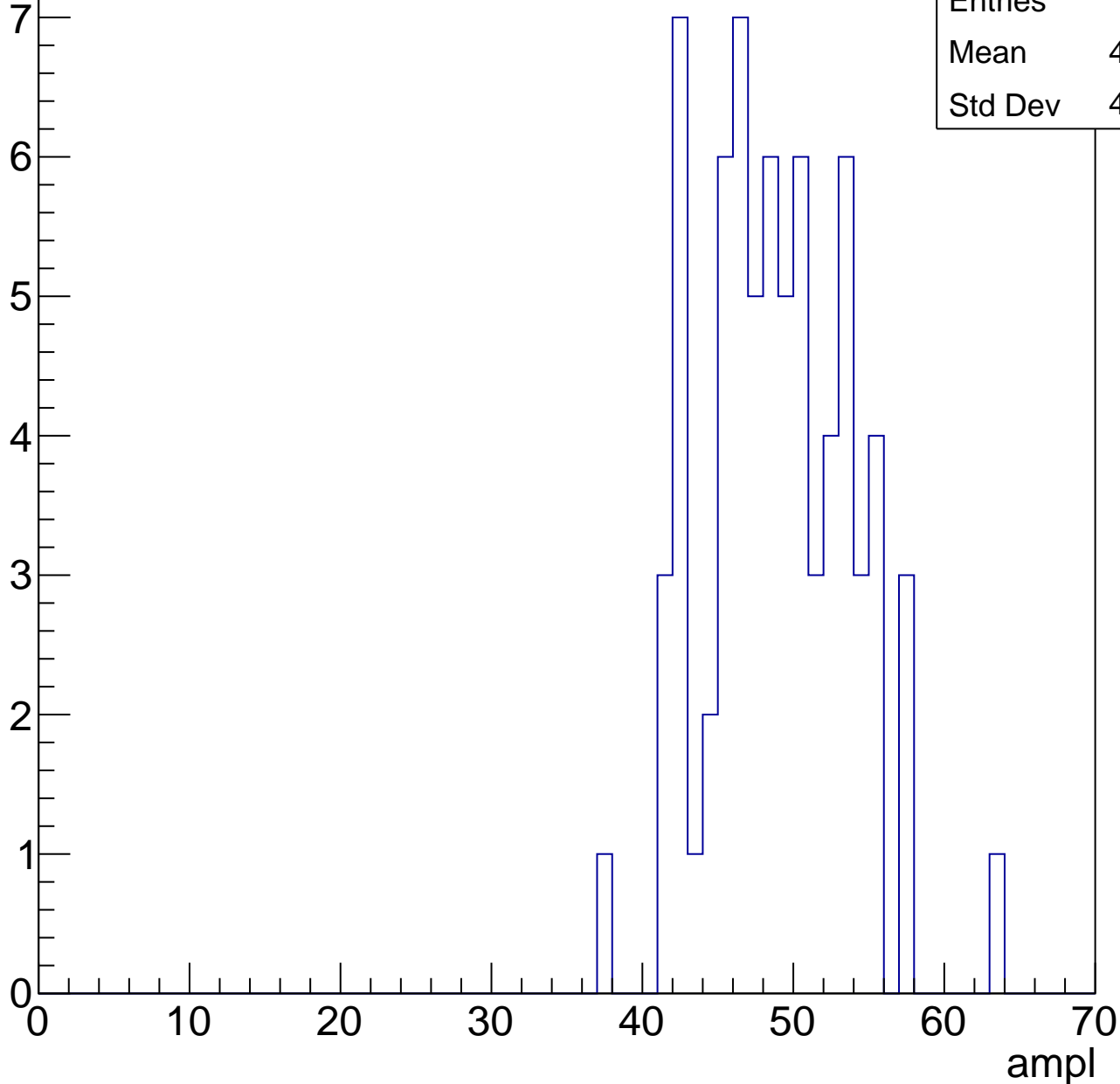


# B1L103S, U26-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	48.49
Std Dev	4.809

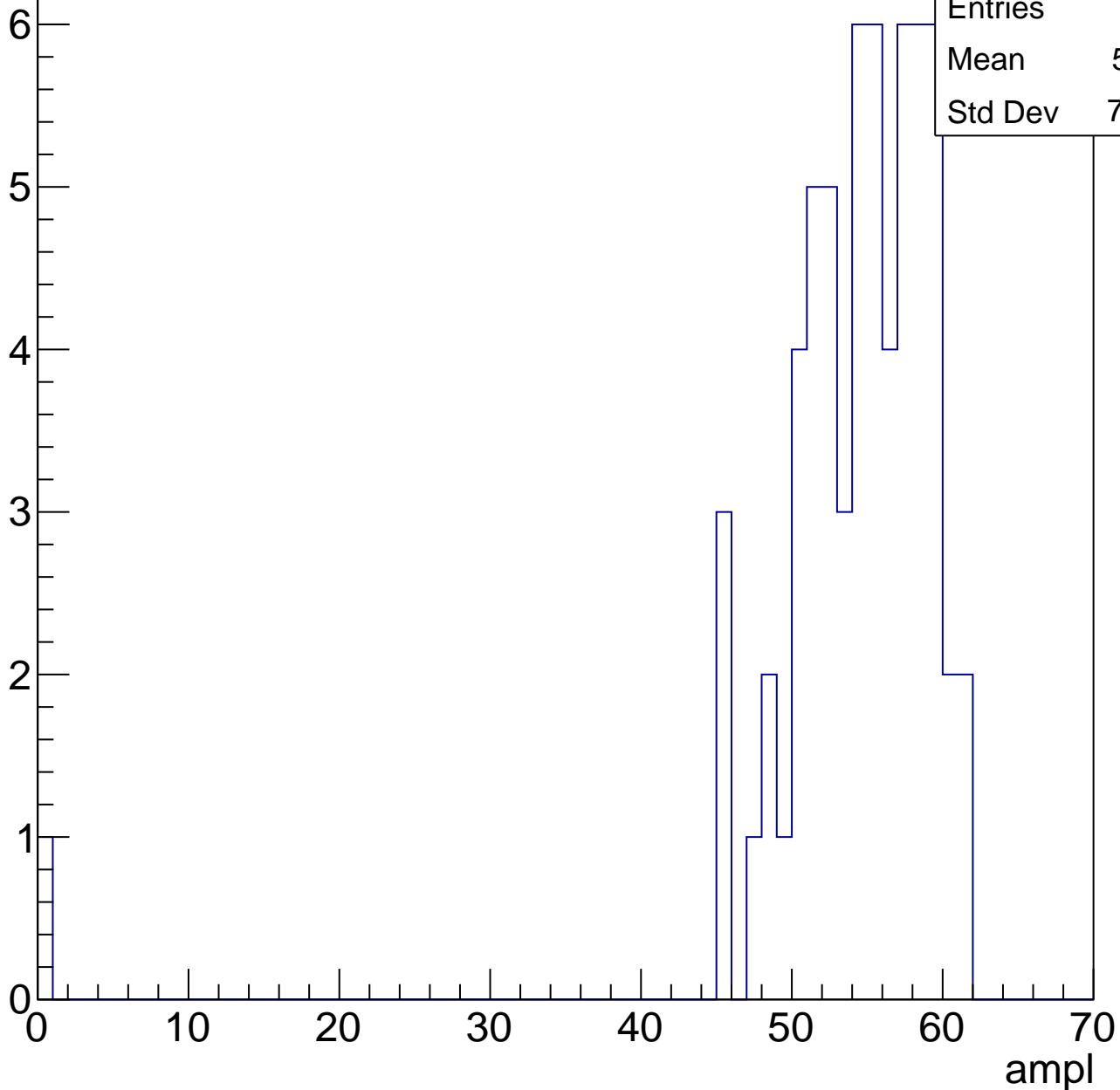


# B1L103S, U26-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	53.41
Std Dev	7.875

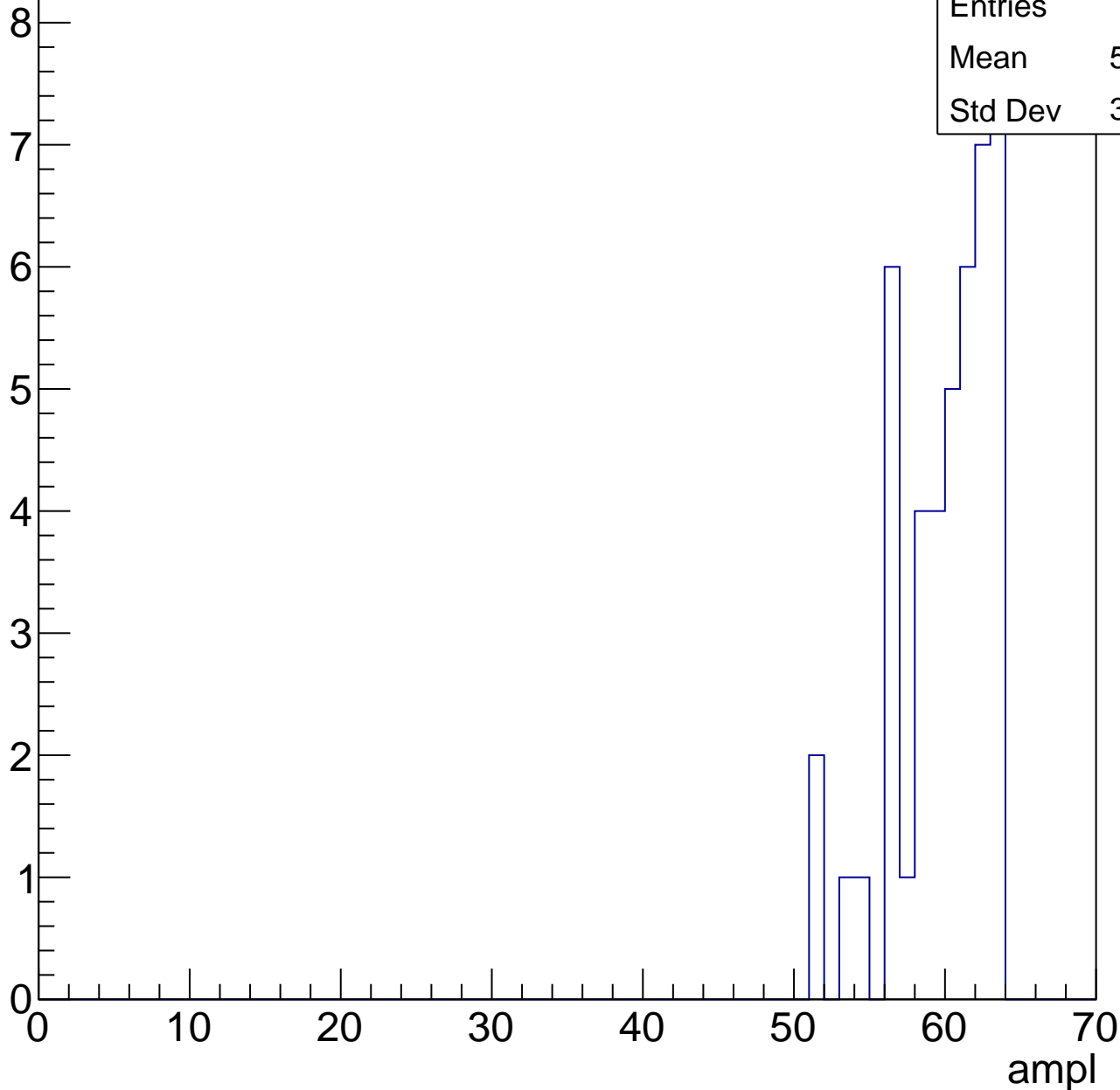


# B1L103S, U26-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	59.42
Std Dev	3.208



# B1L103S, U26-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

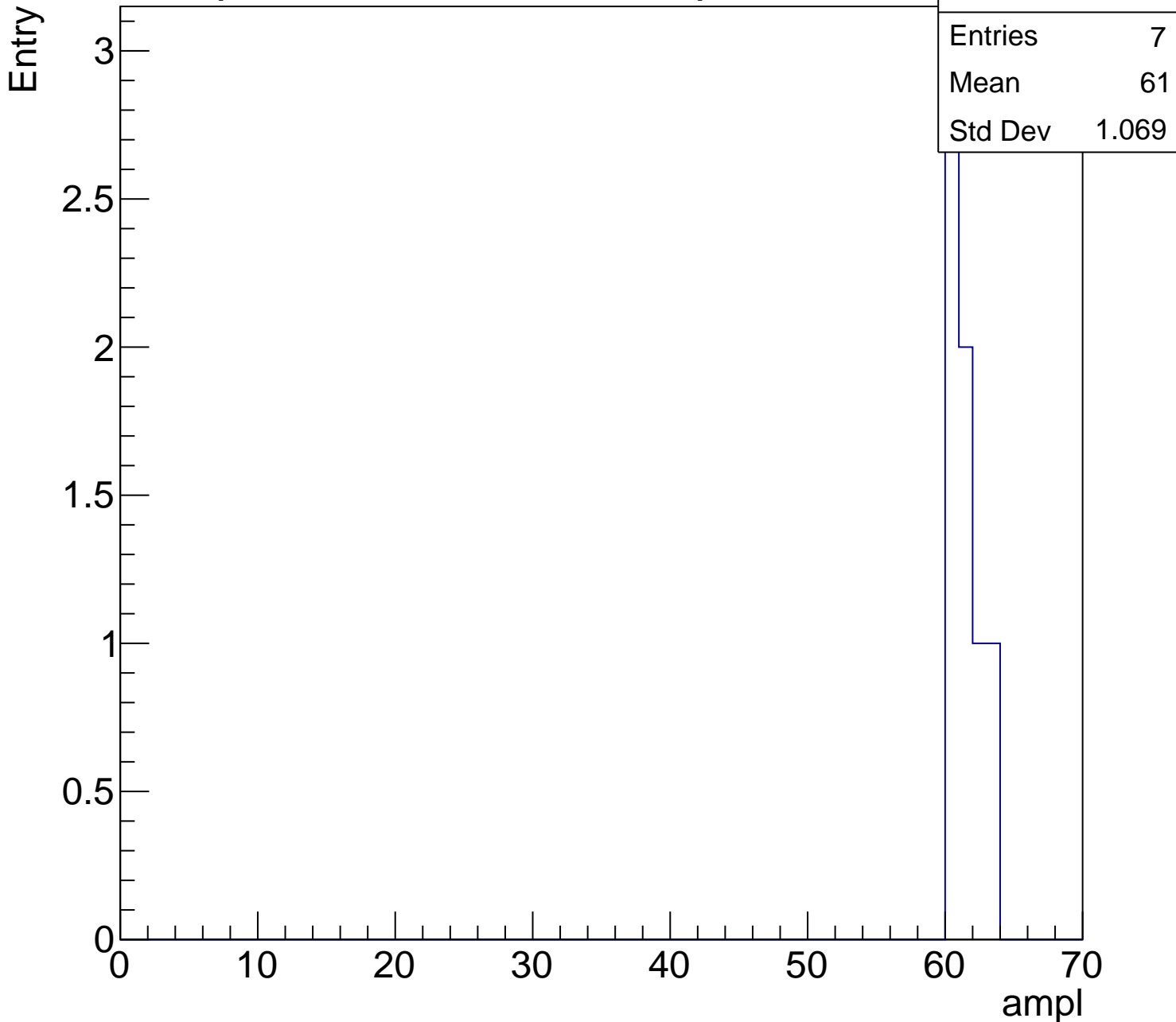
7

Mean

61

Std Dev

1.069

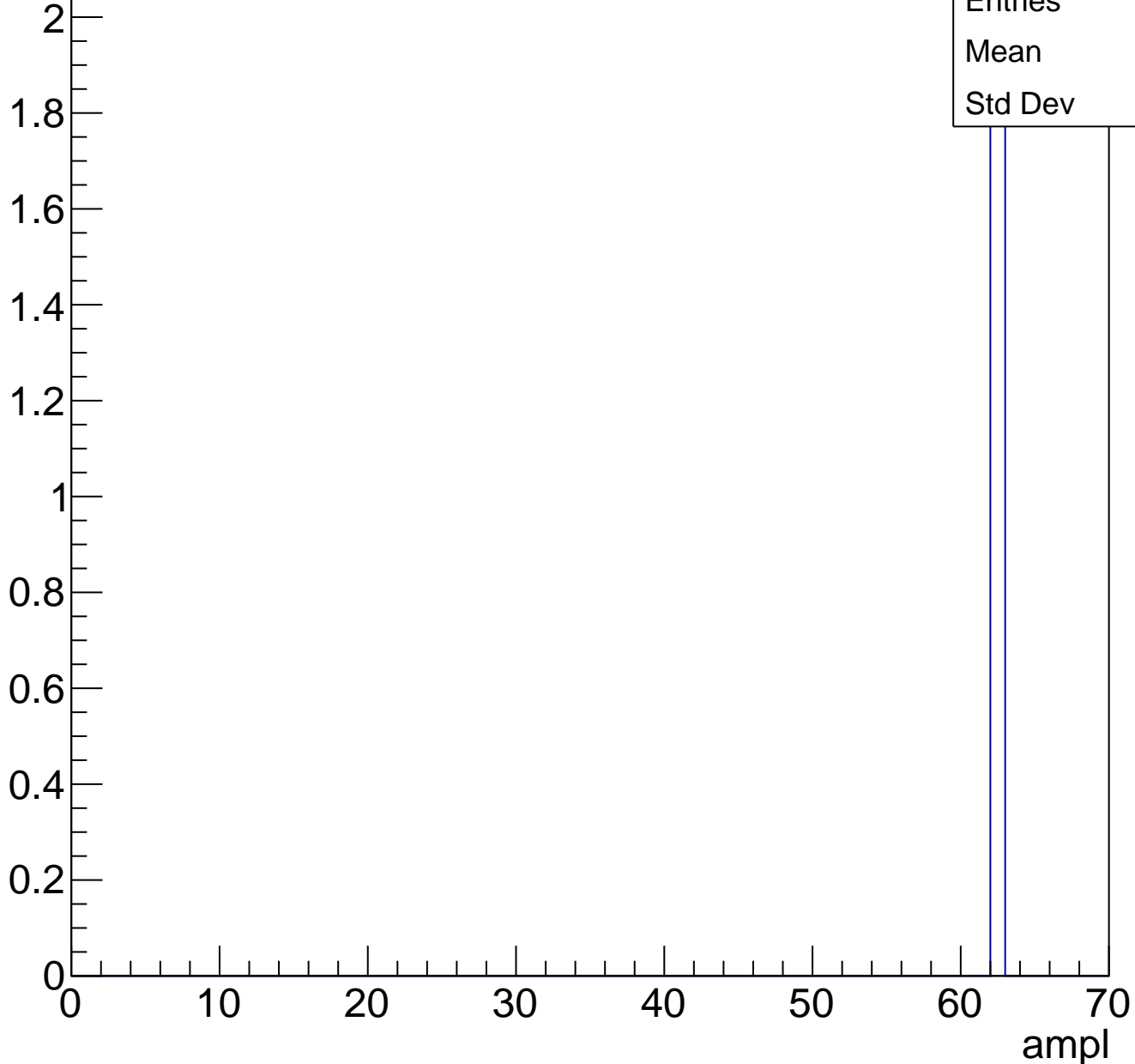




# B1L103S, U26-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch99, adc0

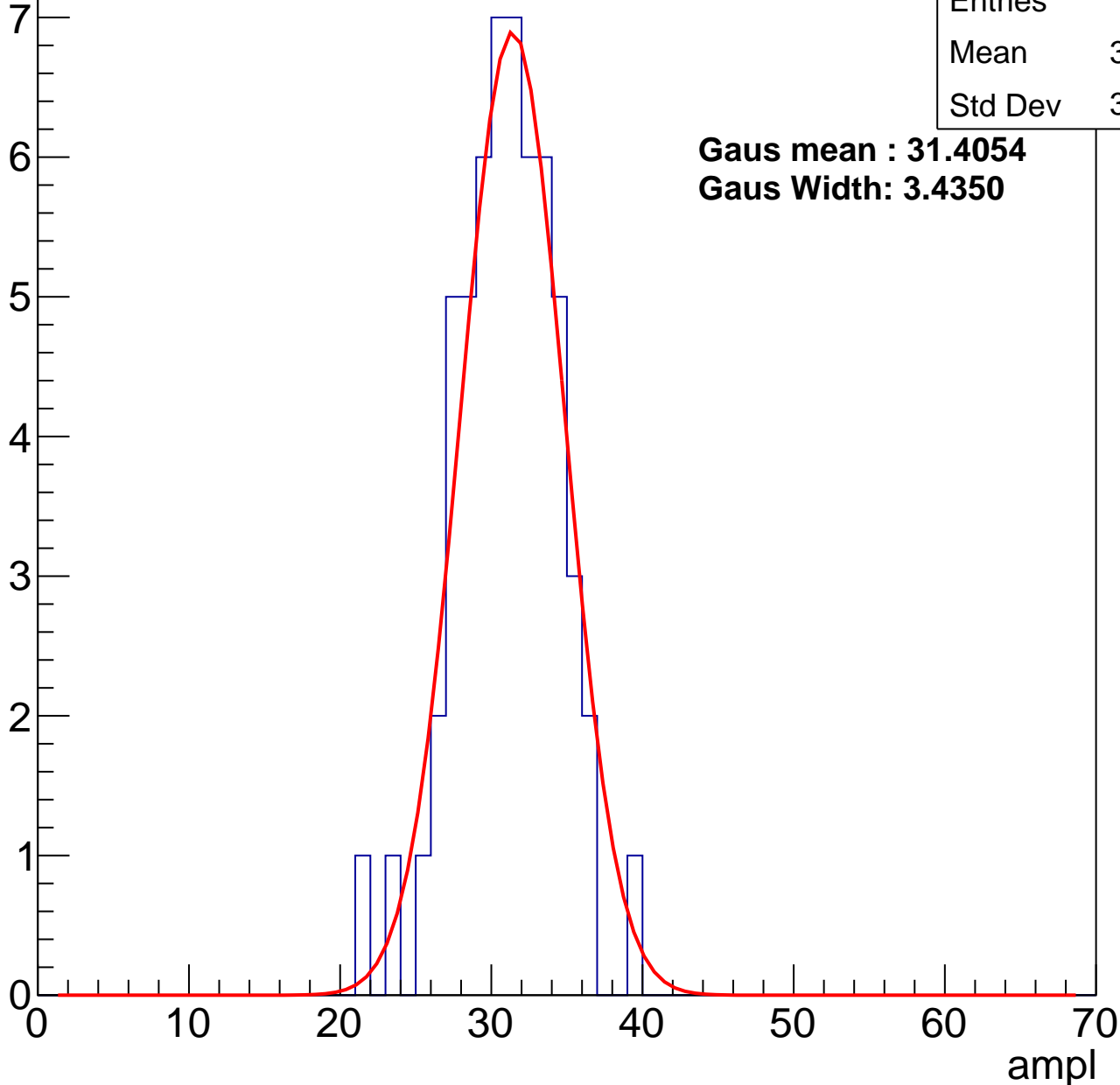
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	30.57
Std Dev	3.302

**Gaus mean : 31.4054**

**Gaus Width: 3.4350**



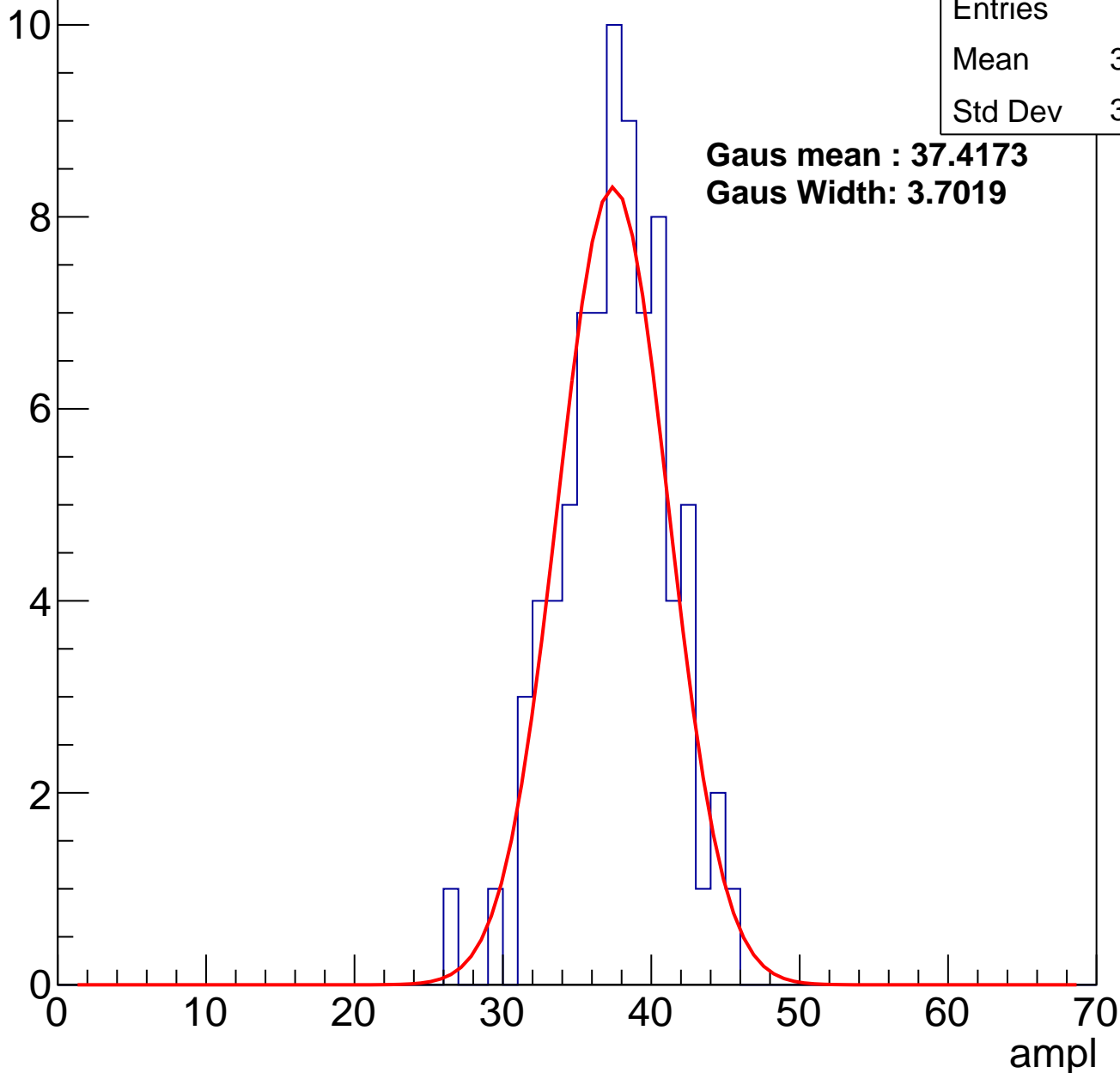
# B1L103S, U26-ch99, adc1

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	79
Mean	37.09
Std Dev	3.615

**Gaus mean : 37.4173**  
**Gaus Width: 3.7019**

Entry



# B1L103S, U26-ch99, adc2

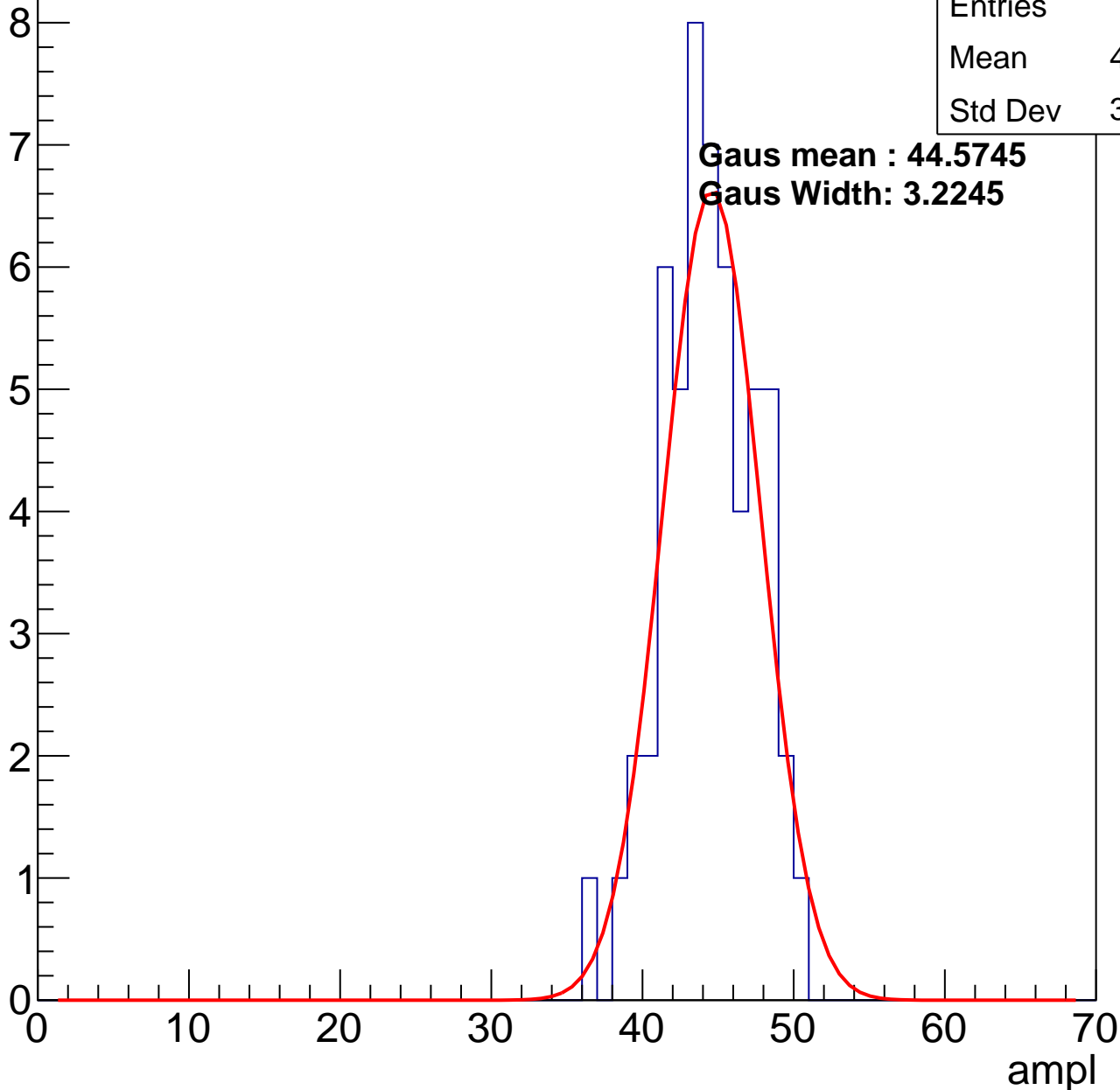
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	43.95
Std Dev	3.006

**Gaus mean : 44.5745**

**Gaus Width: 3.2245**

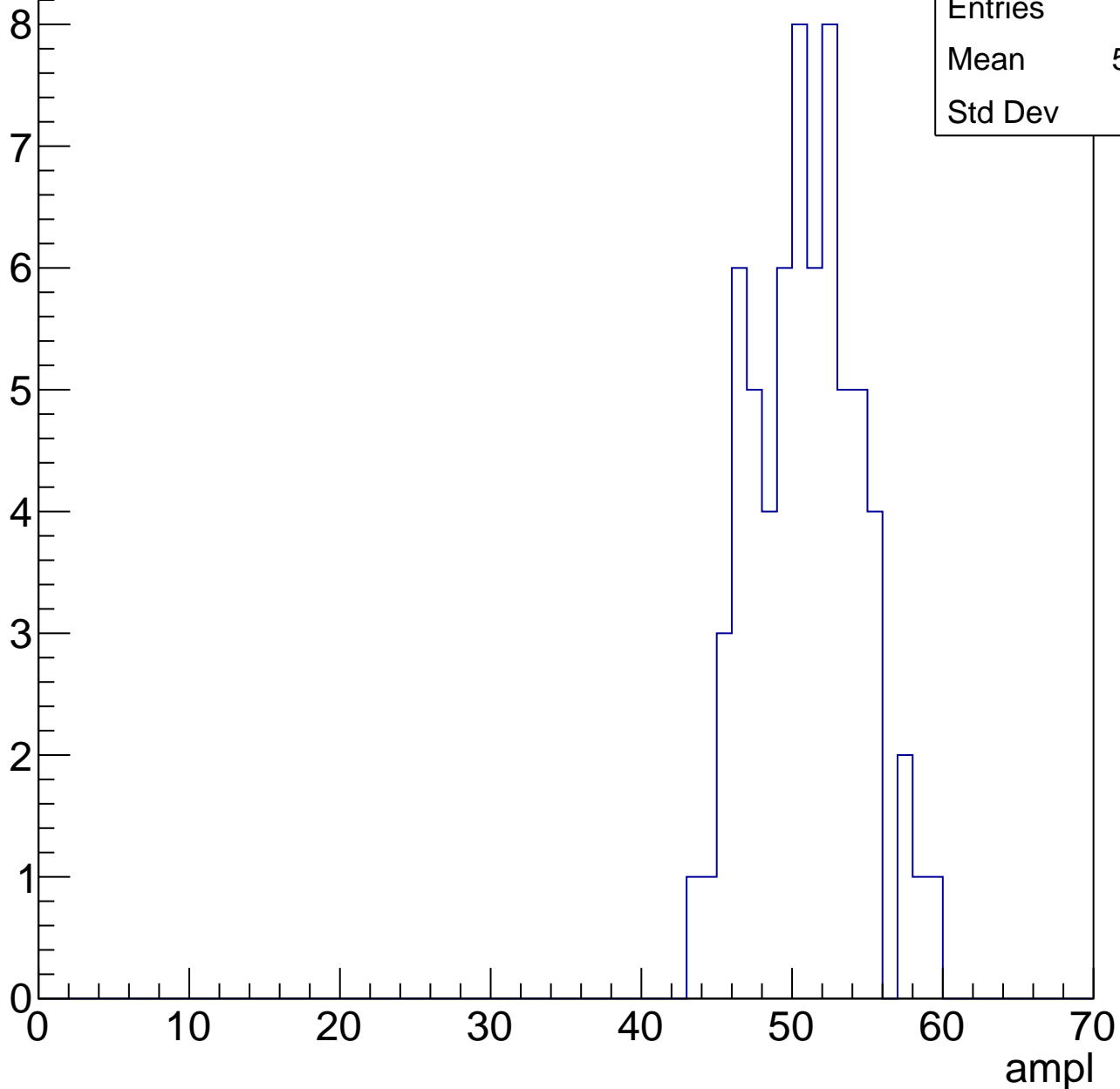


# B1L103S, U26-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	50.41
Std Dev	3.52

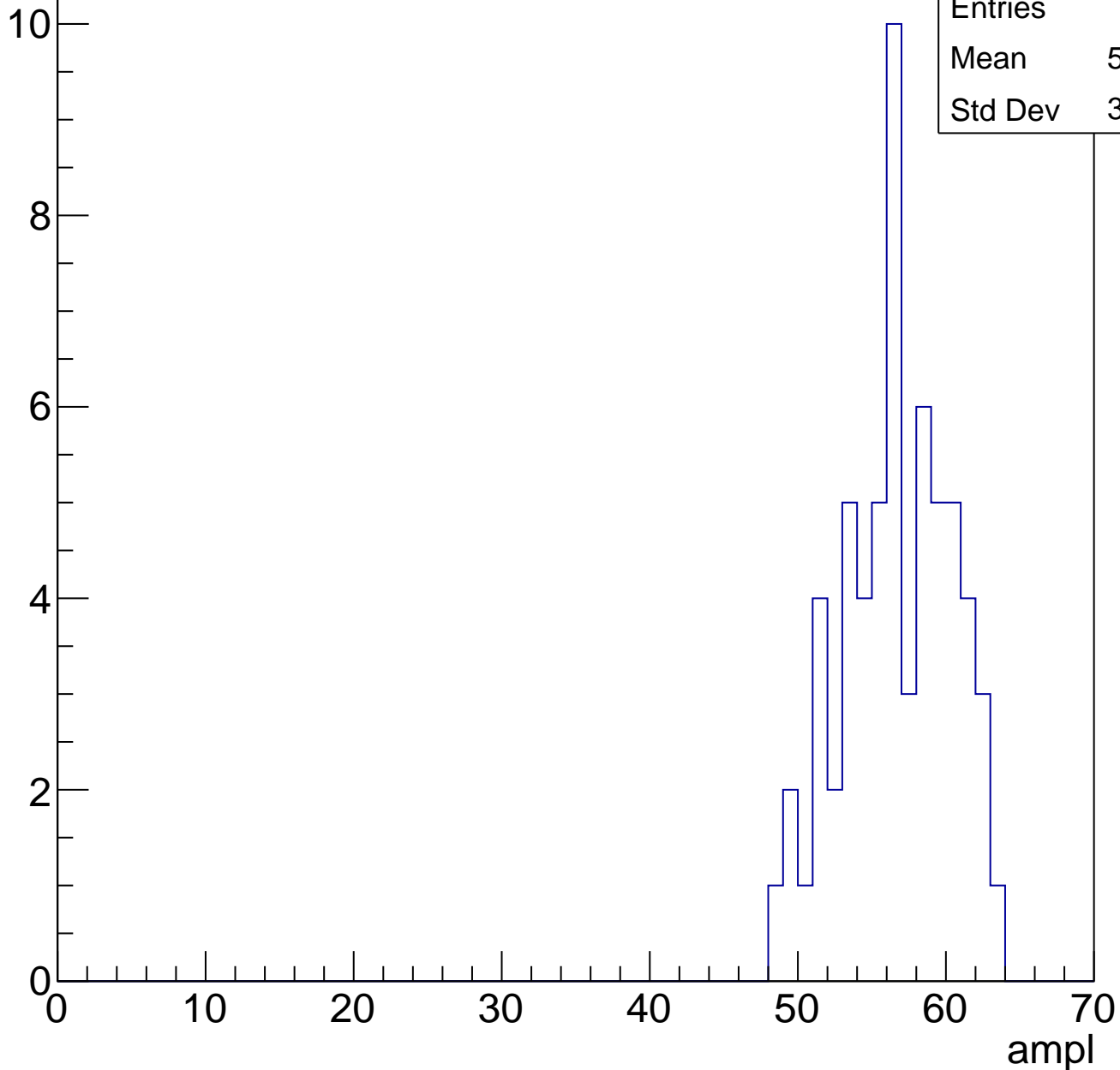


# B1L103S, U26-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	61
Mean	56.18
Std Dev	3.628

Entry

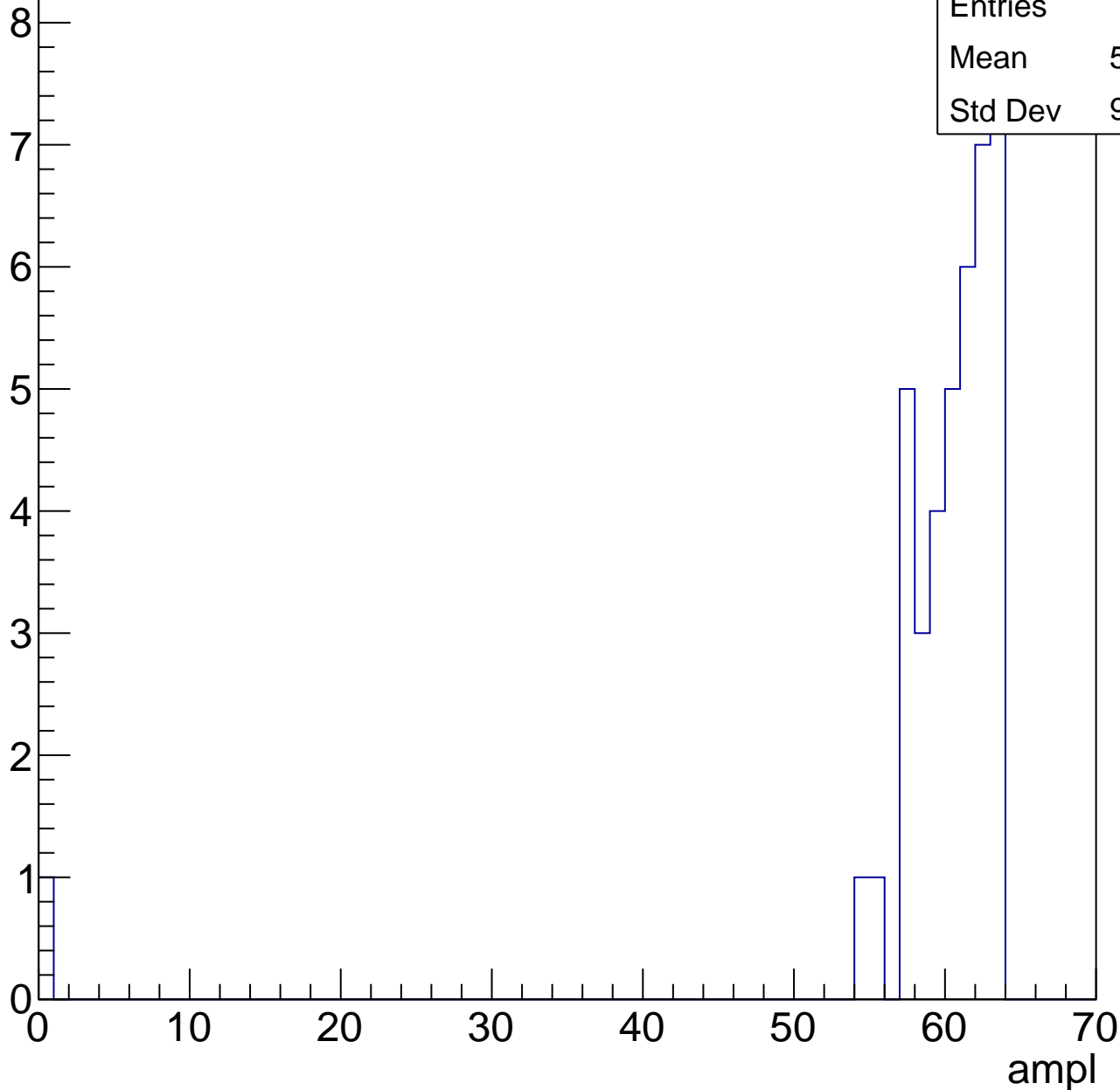


# B1L103S, U26-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	41
Mean	58.73
Std Dev	9.579



# B1L103S, U26-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	63
Std Dev	0

ampl



# B1L103S, U26-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U26-ch100, adc0

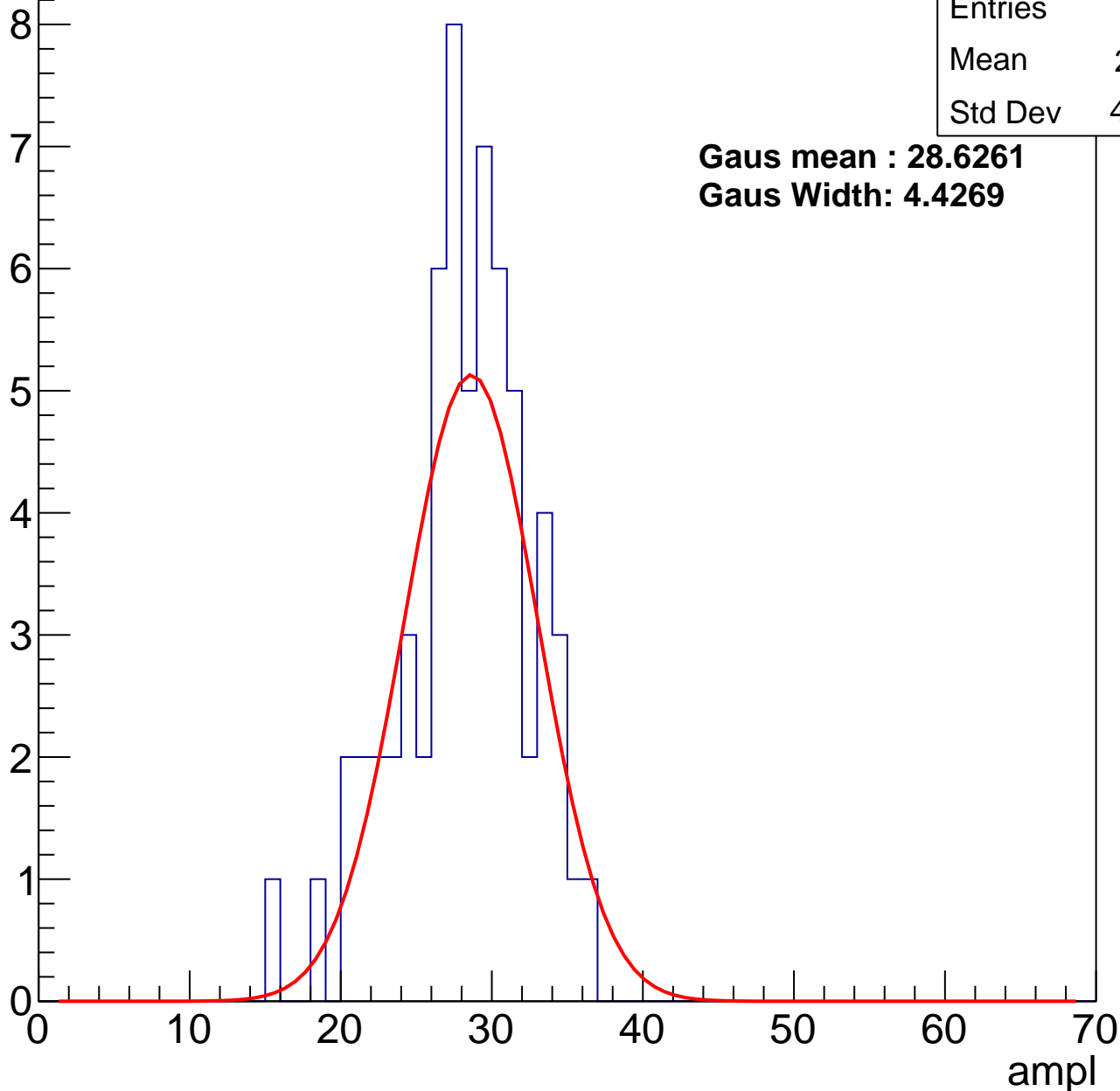
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	27.71
Std Dev	4.252

**Gaus mean : 28.6261**

**Gaus Width: 4.4269**



# B1L103S, U26-ch100, adc1

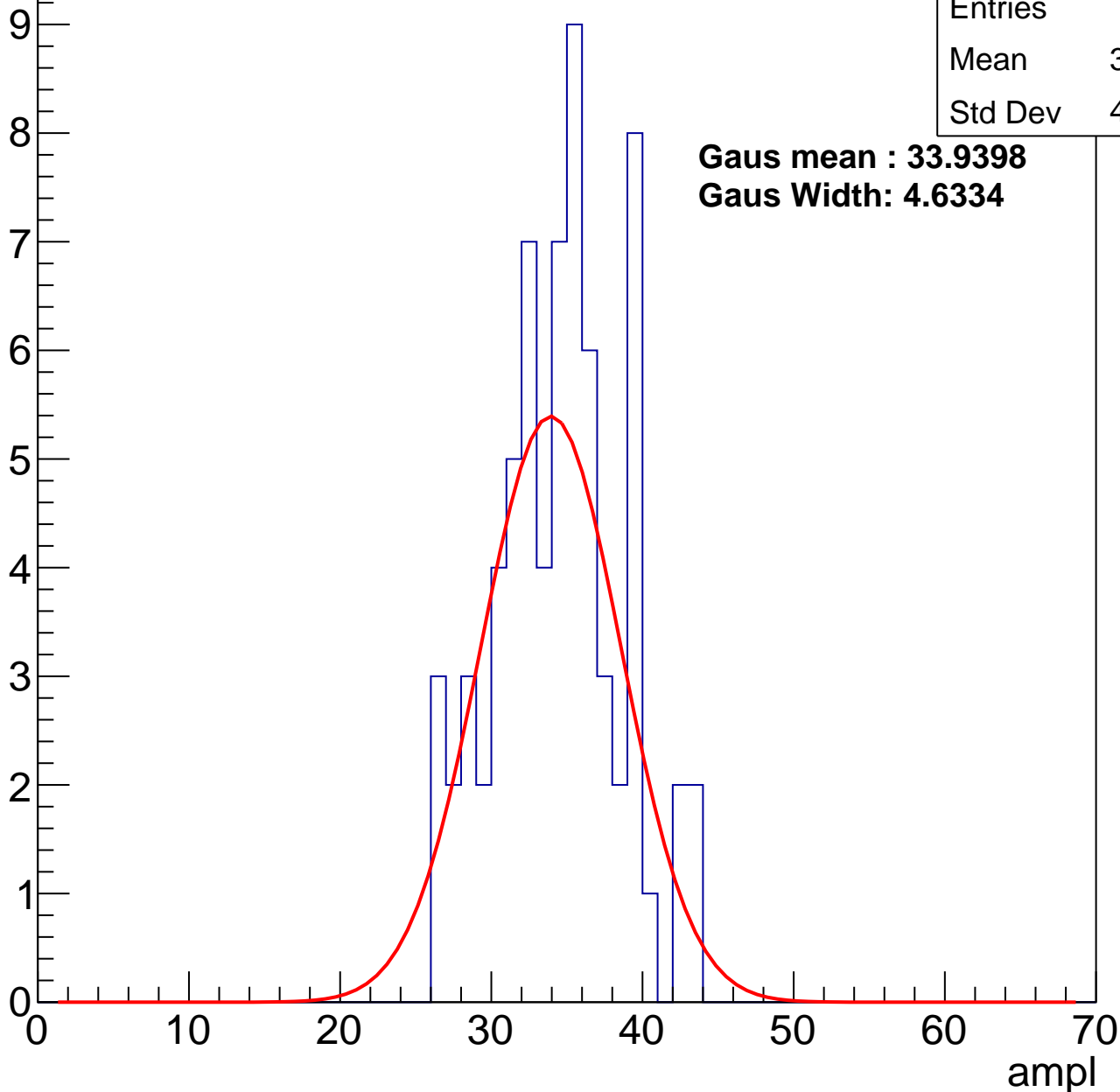
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	34.04
Std Dev	4.152

**Gaus mean : 33.9398**

**Gaus Width: 4.6334**



# B1L103S, U26-ch100, adc2

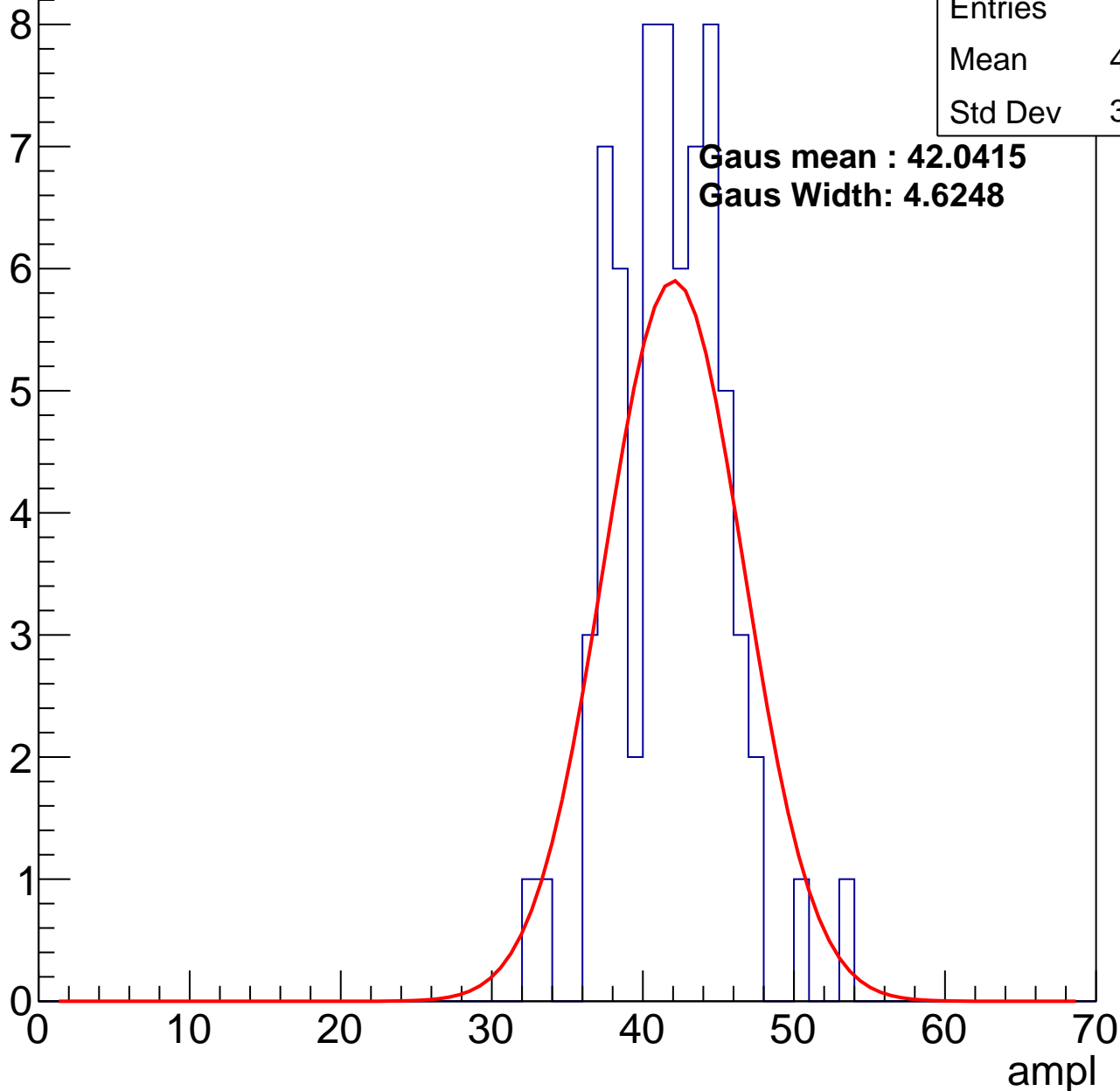
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	41.32
Std Dev	3.716

**Gaus mean : 42.0415**

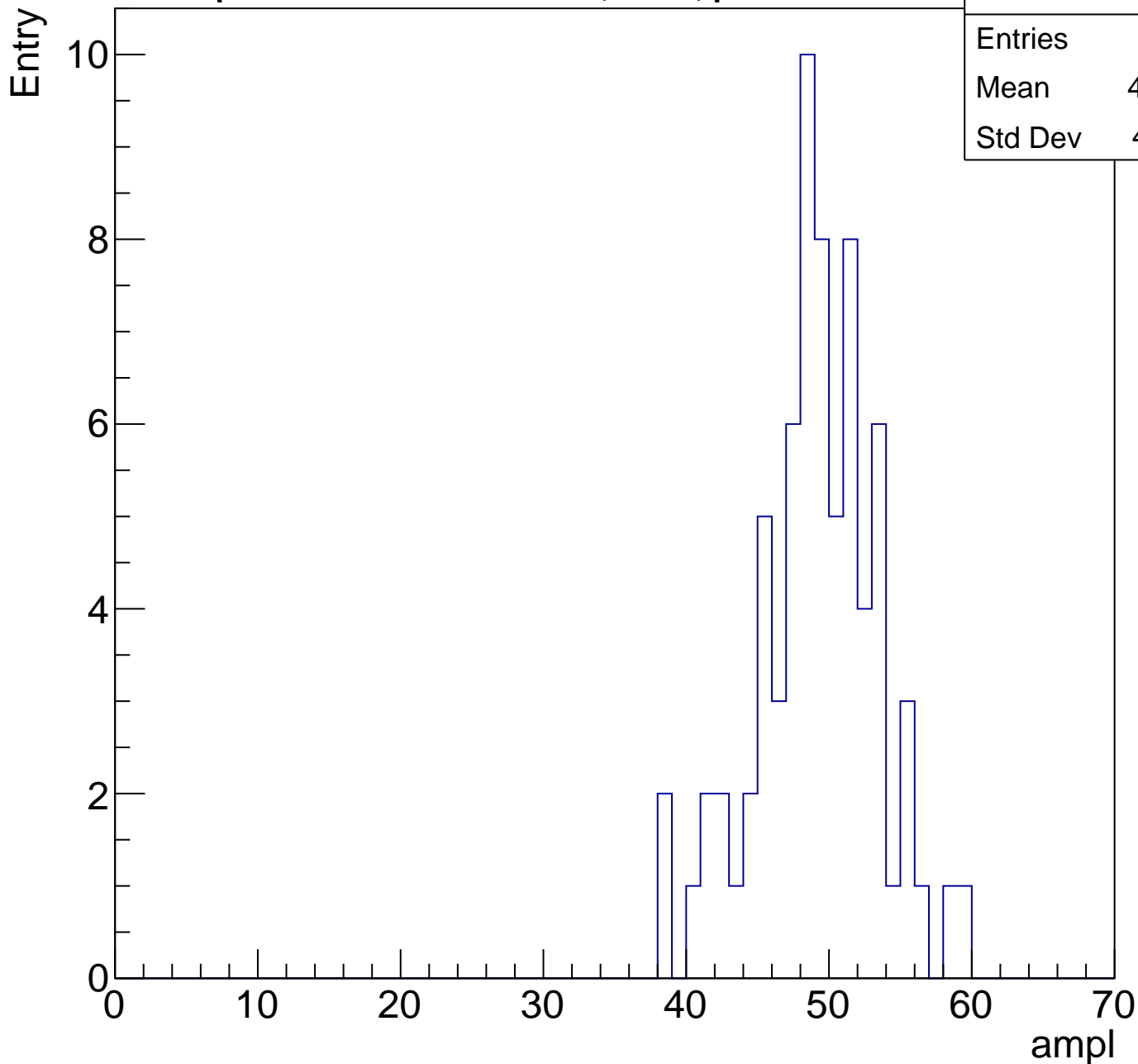
**Gaus Width: 4.6248**



# B1L103S, U26-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	72
Mean	48.69
Std Dev	4.251

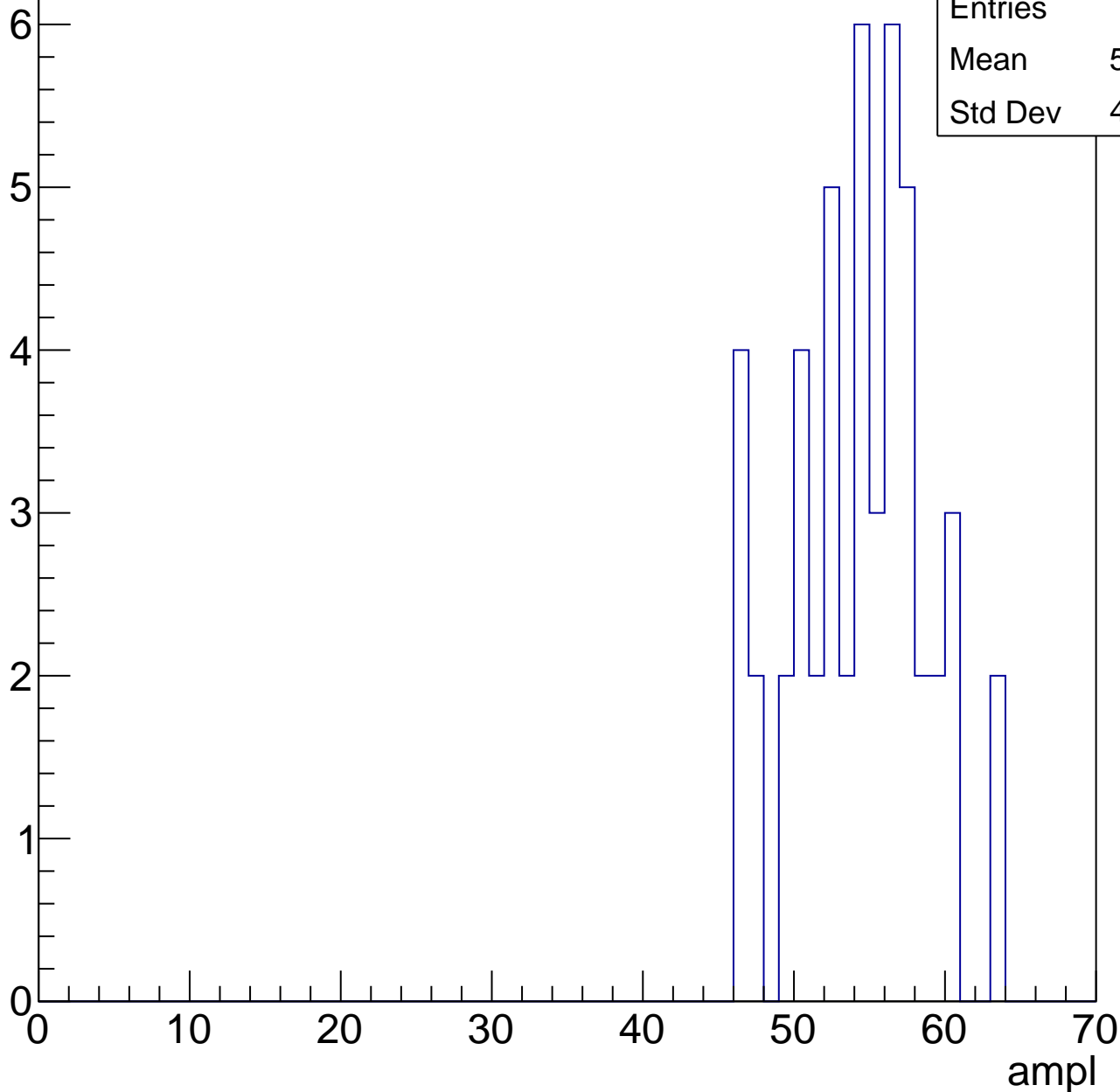


# B1L103S, U26-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	53.88
Std Dev	4.316

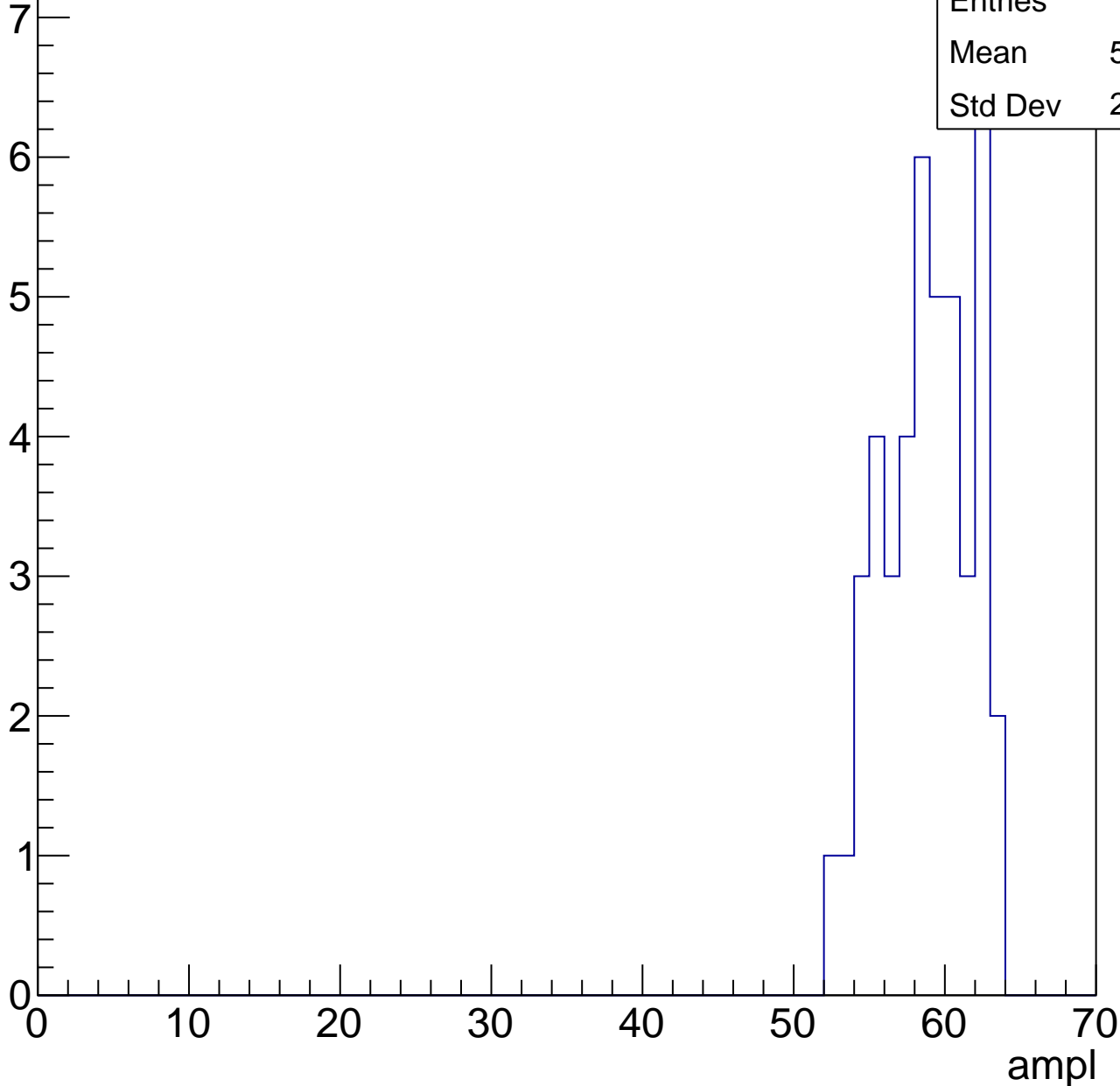


# B1L103S, U26-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

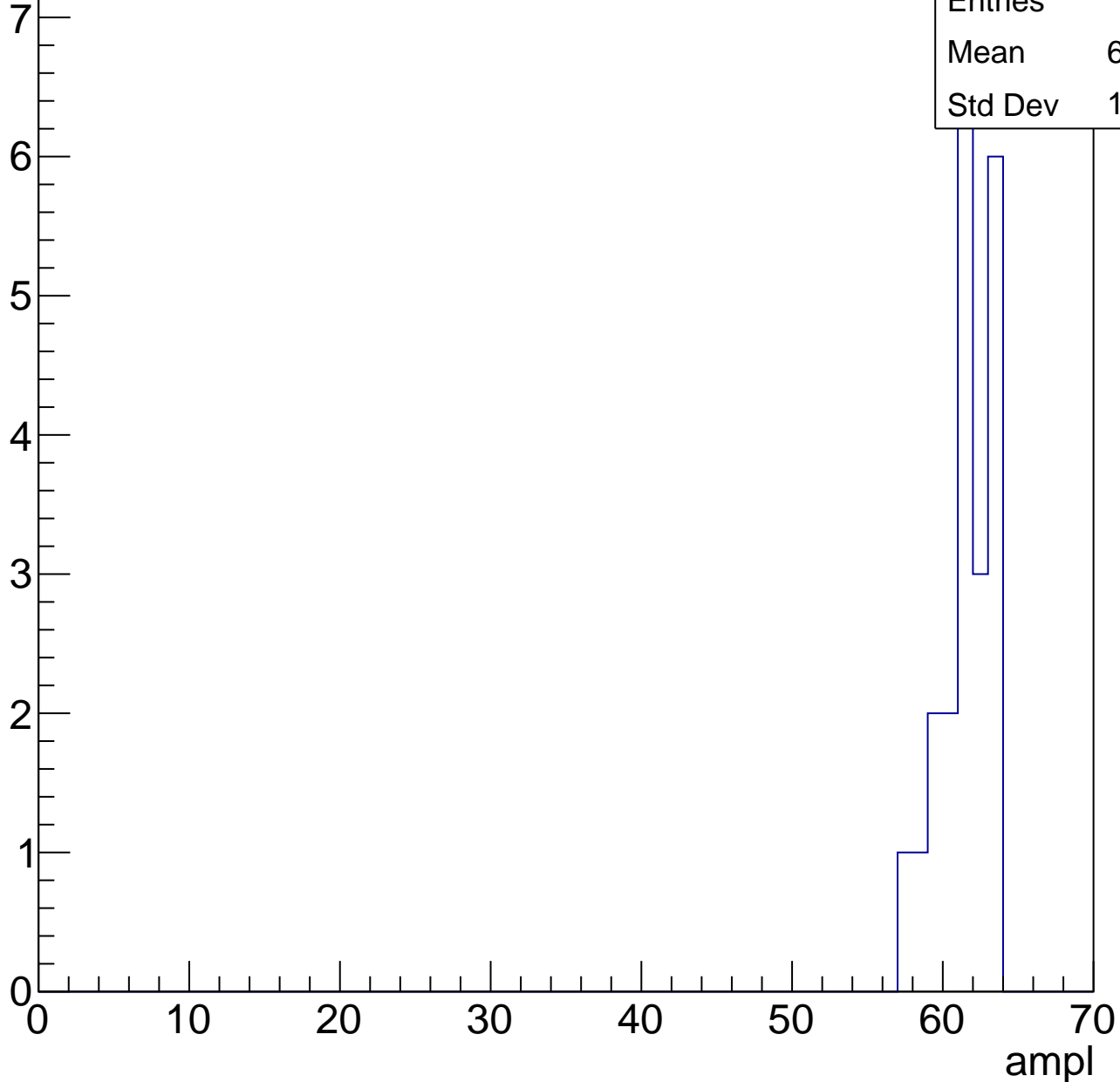
Entries	44
Mean	58.39
Std Dev	2.894



# B1L103S, U26-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch101, adc0

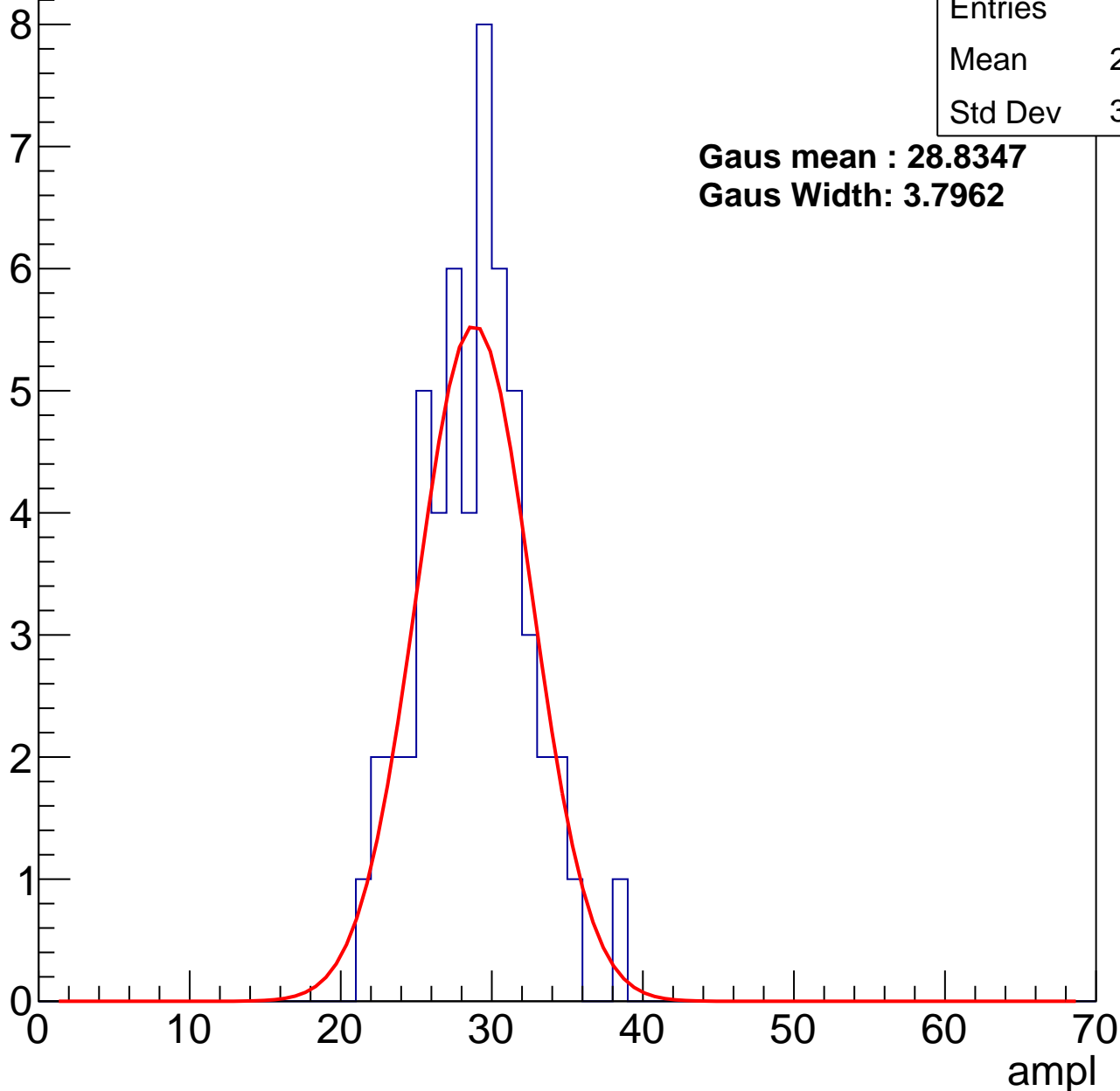
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	28.37
Std Dev	3.492

**Gaus mean : 28.8347**

**Gaus Width: 3.7962**



# B1L103S, U26-ch101, adc1

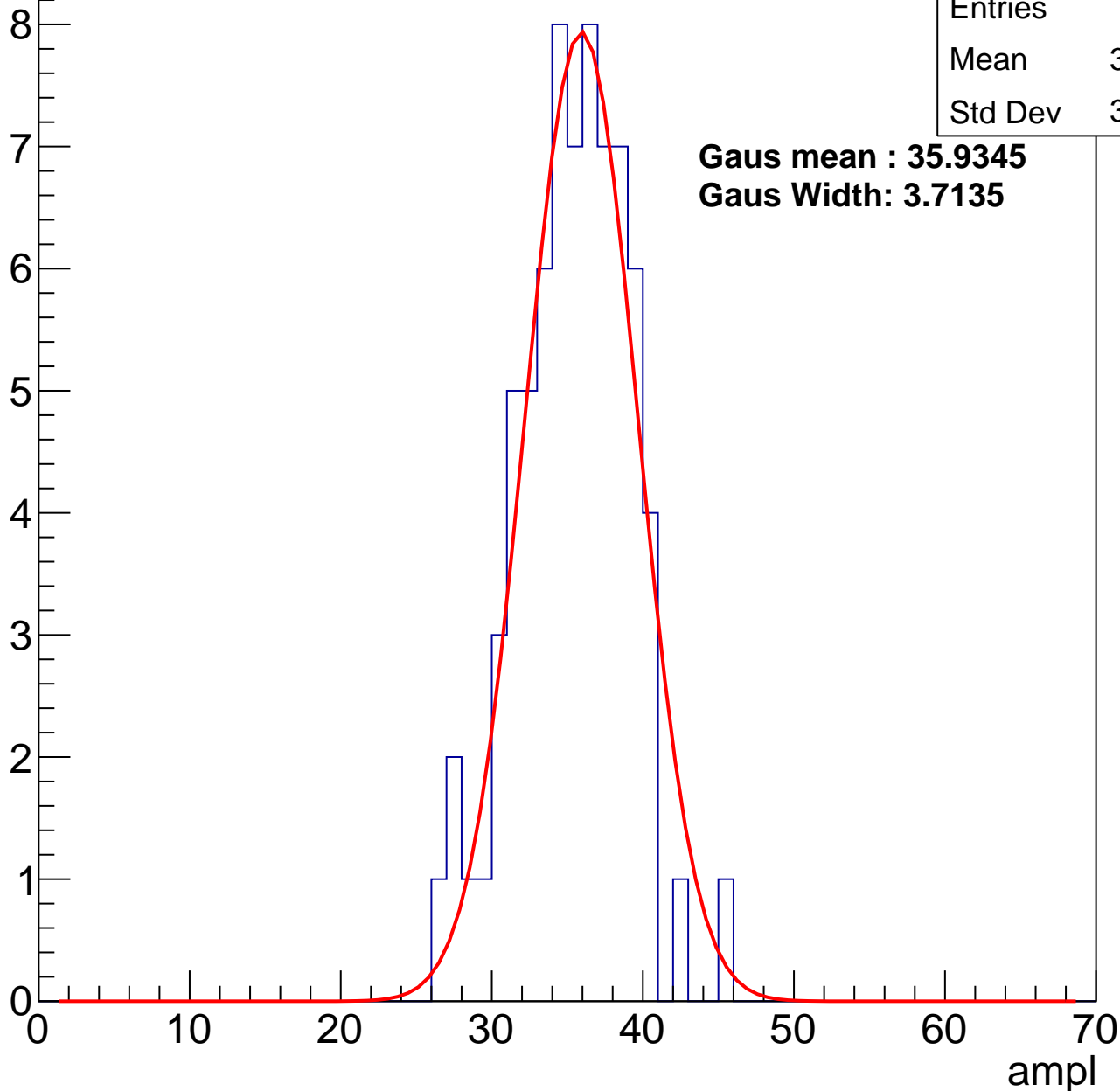
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	34.95
Std Dev	3.645

**Gaus mean : 35.9345**

**Gaus Width: 3.7135**



# B1L103S, U26-ch101, adc2

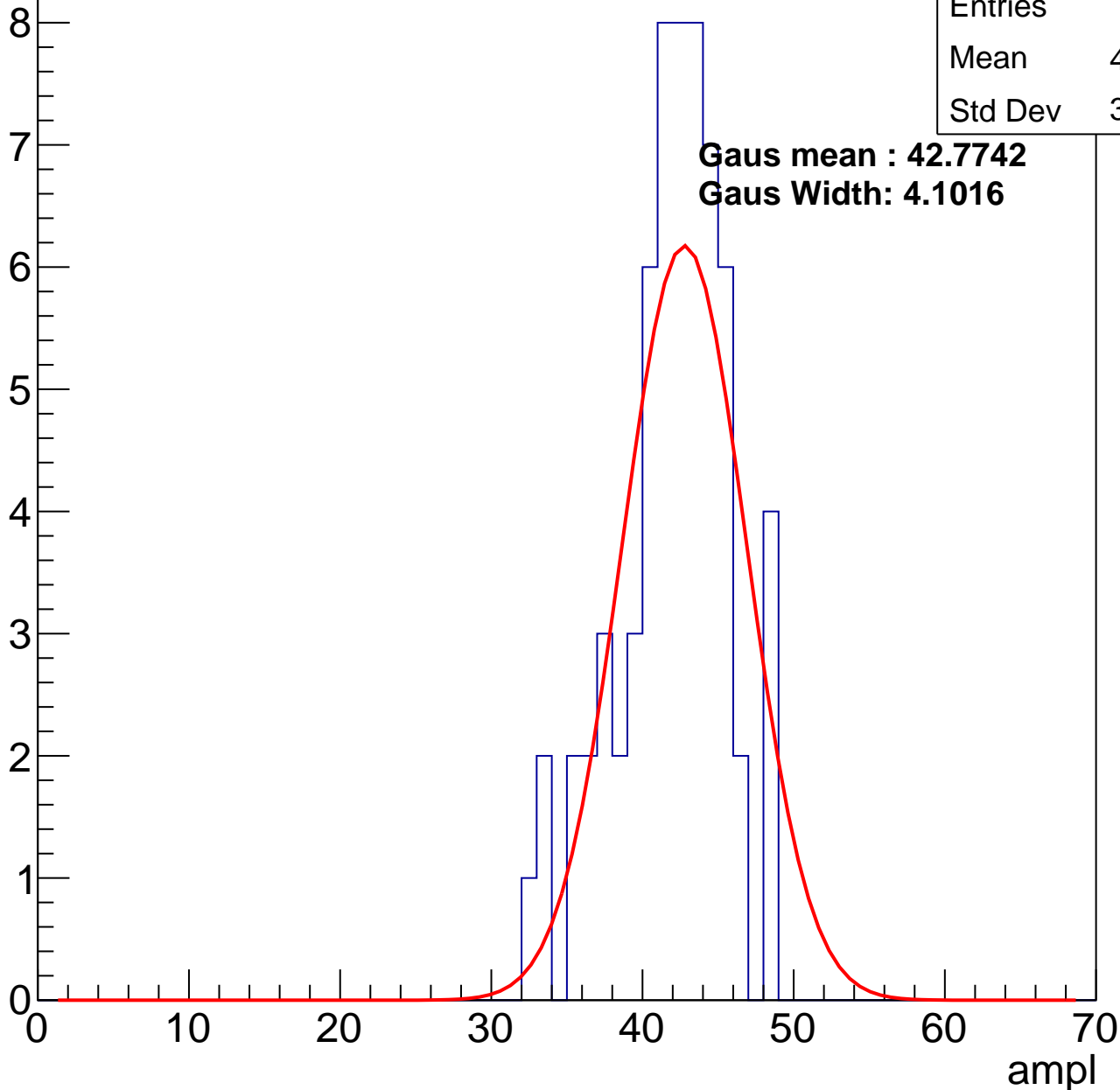
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	41.47
Std Dev	3.636

**Gaus mean : 42.7742**

**Gaus Width: 4.1016**

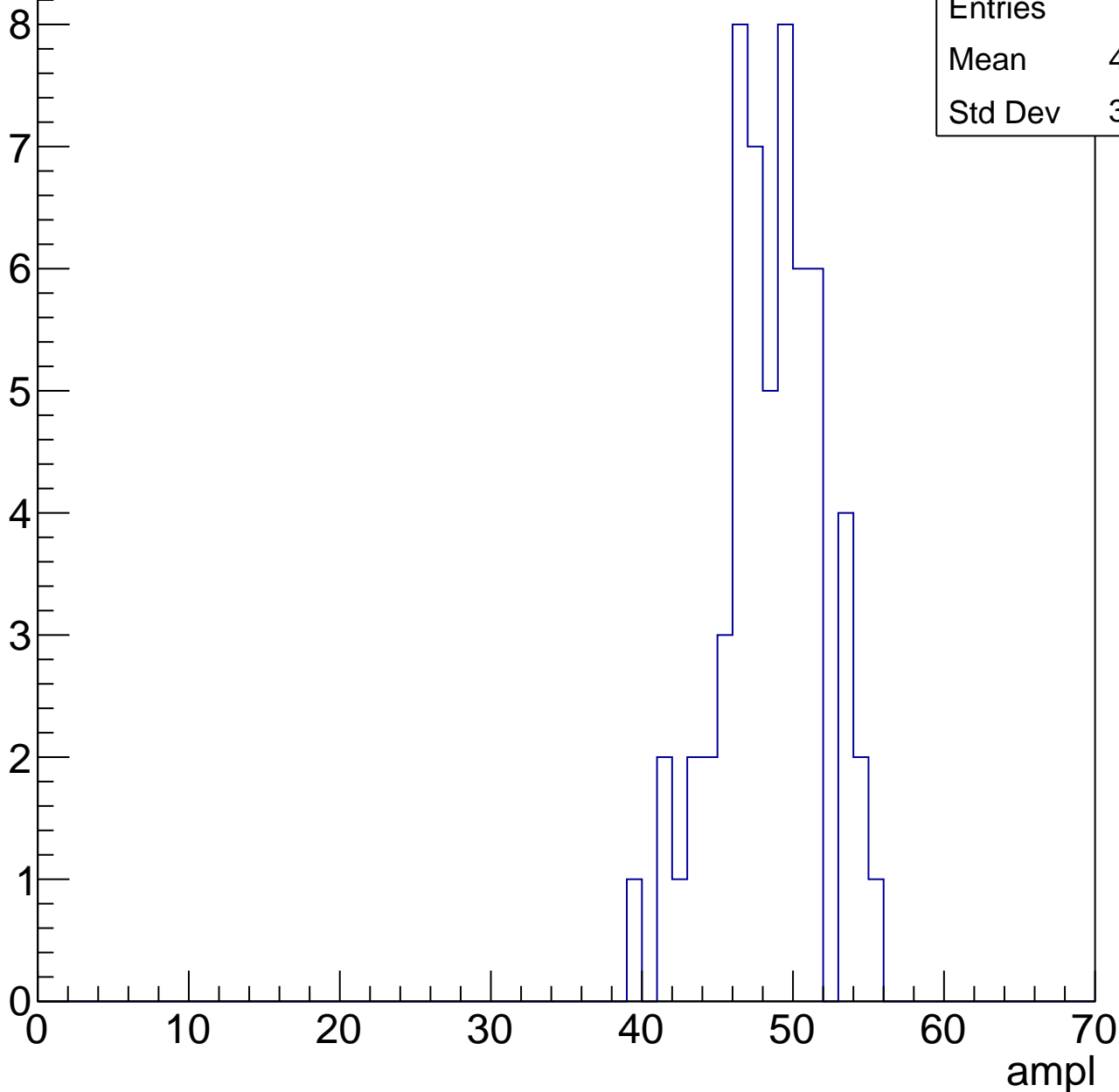


# B1L103S, U26-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	47.97
Std Dev	3.399

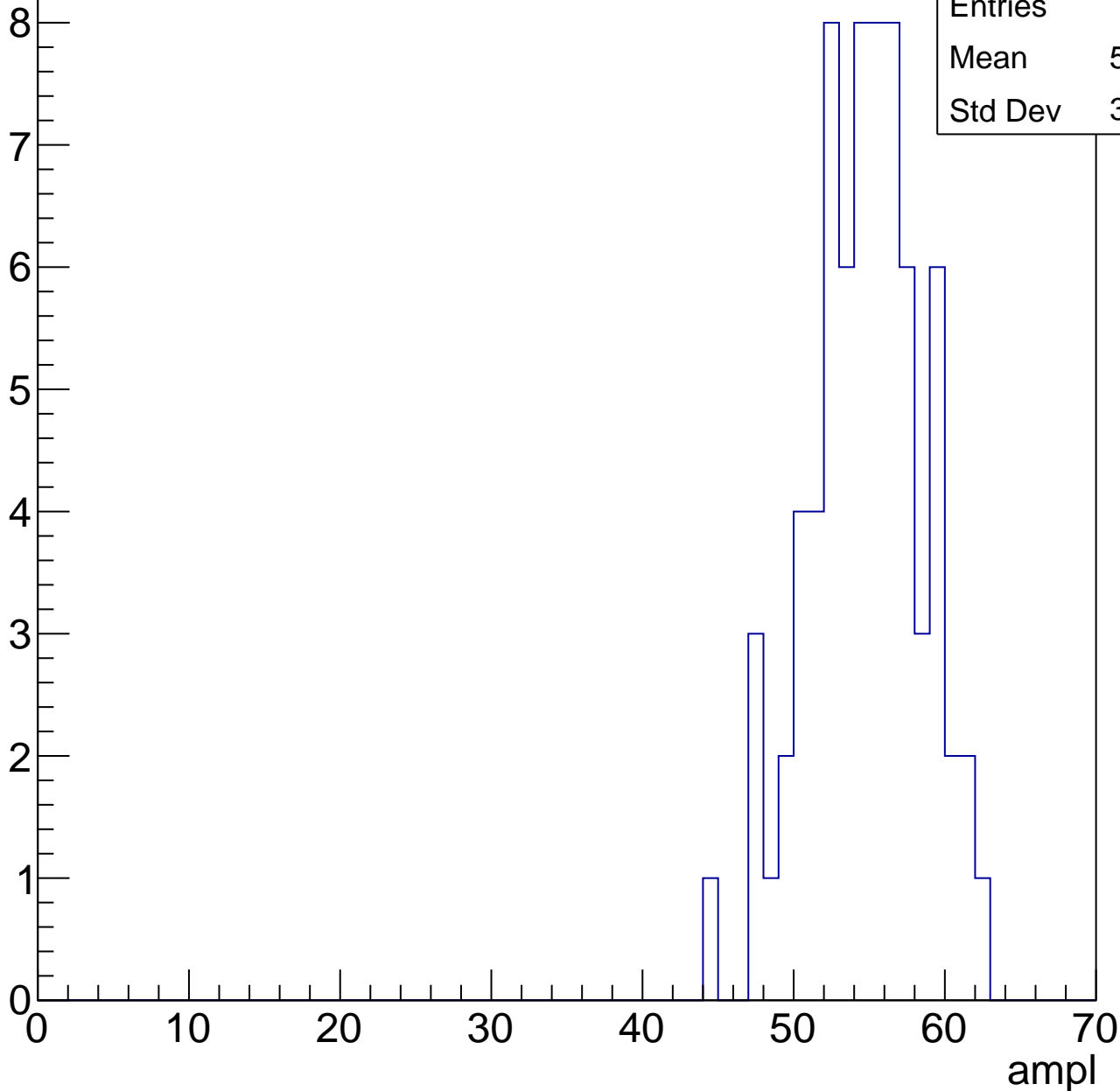


# B1L103S, U26-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	54.29
Std Dev	3.684

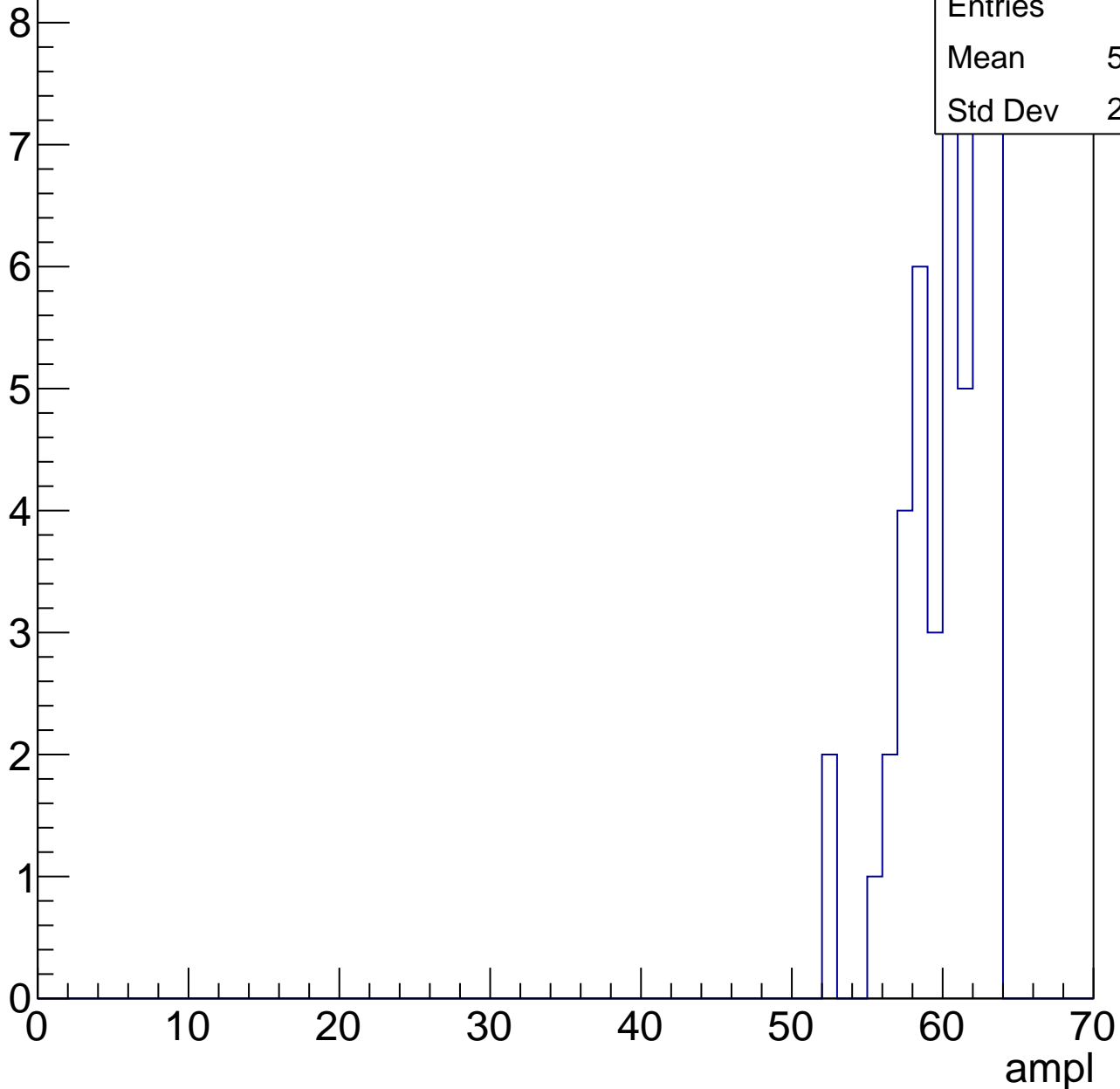


# B1L103S, U26-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

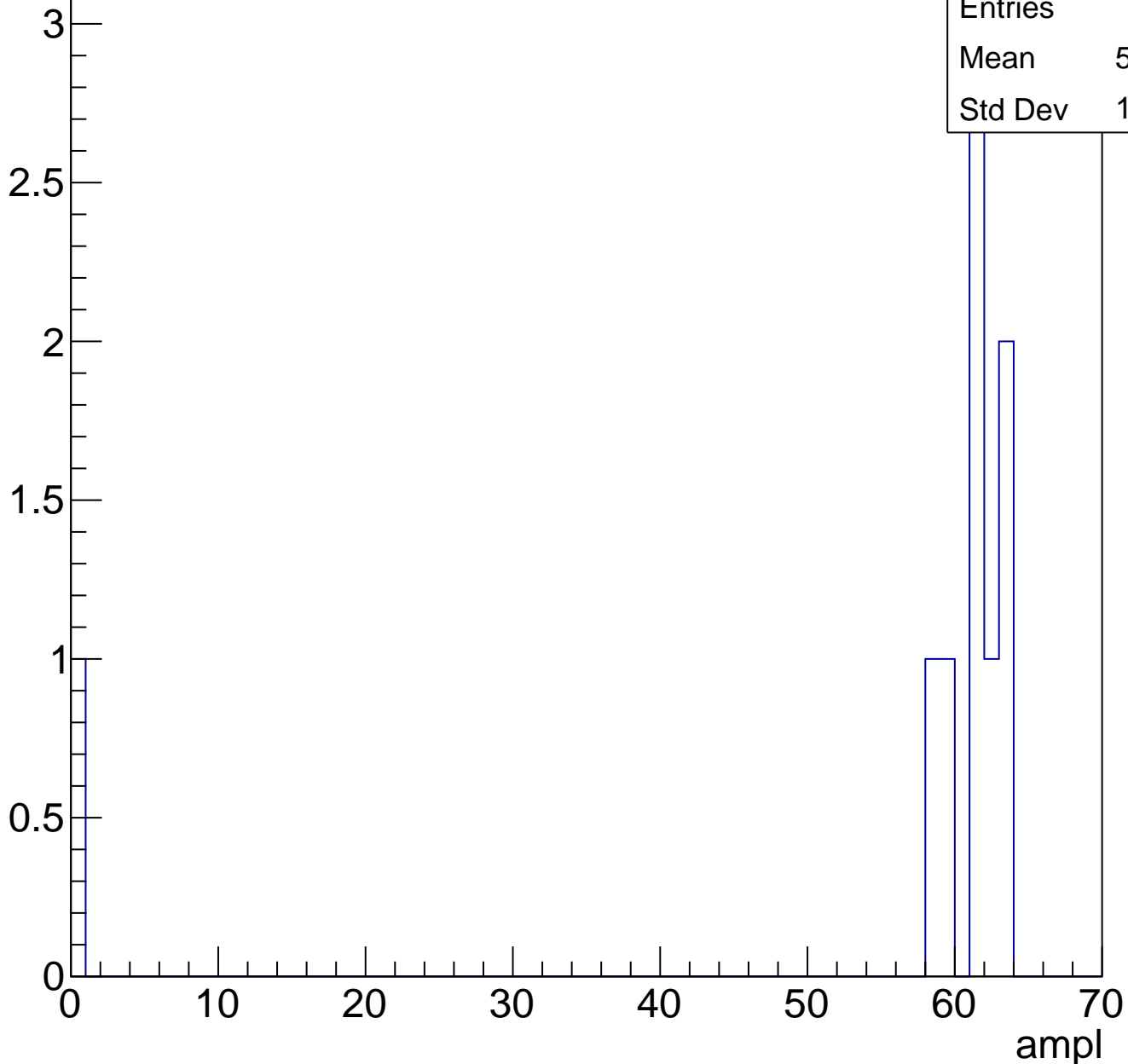
Entries	47
Mean	59.77
Std Dev	2.746



# B1L103S, U26-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U26-ch102, adc0

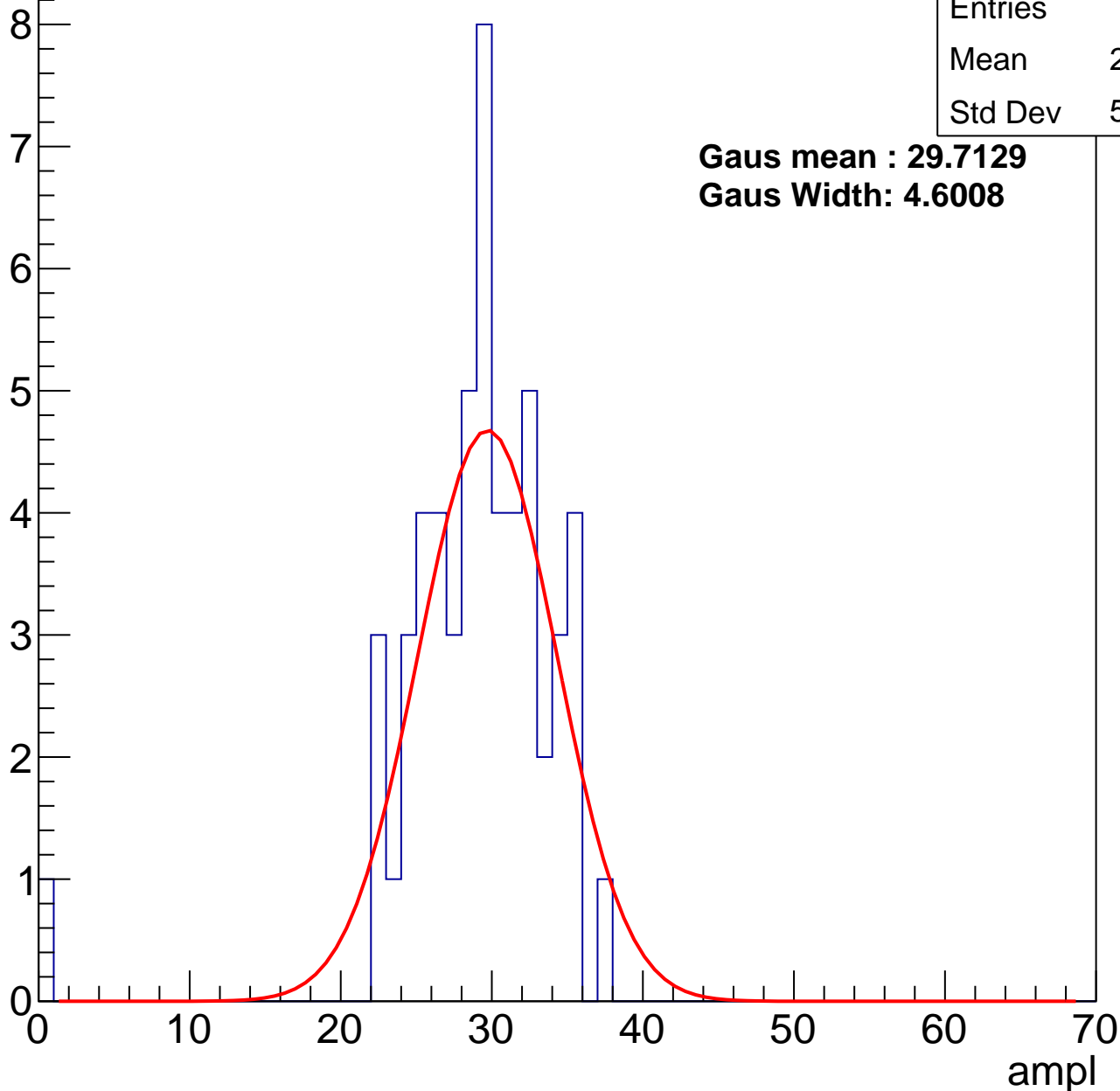
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	28.49
Std Dev	5.363

**Gaus mean : 29.7129**

**Gaus Width: 4.6008**



# B1L103S, U26-ch102, adc1

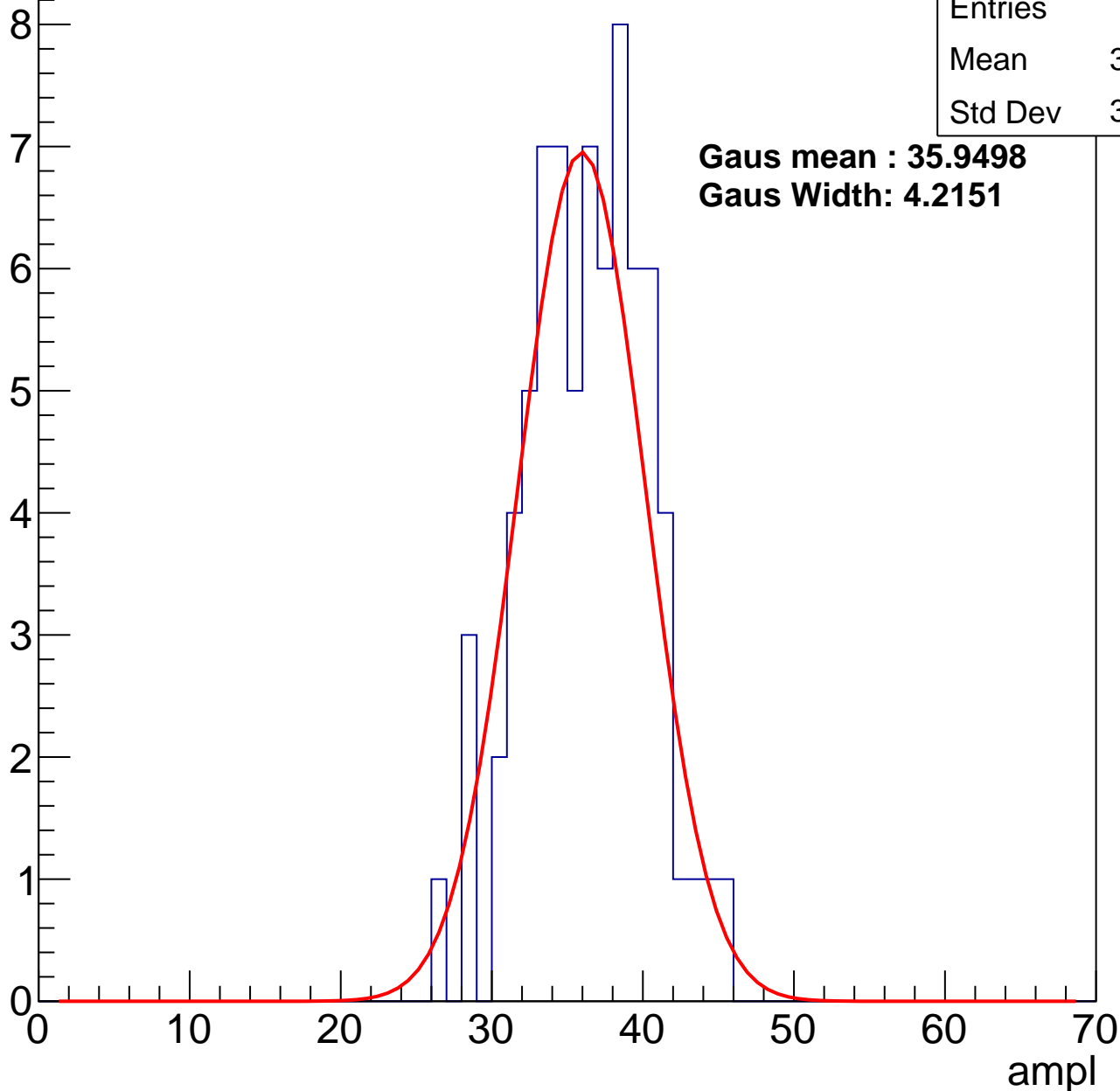
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	35.84
Std Dev	3.926

**Gaus mean : 35.9498**

**Gaus Width: 4.2151**



# B1L103S, U26-ch102, adc2

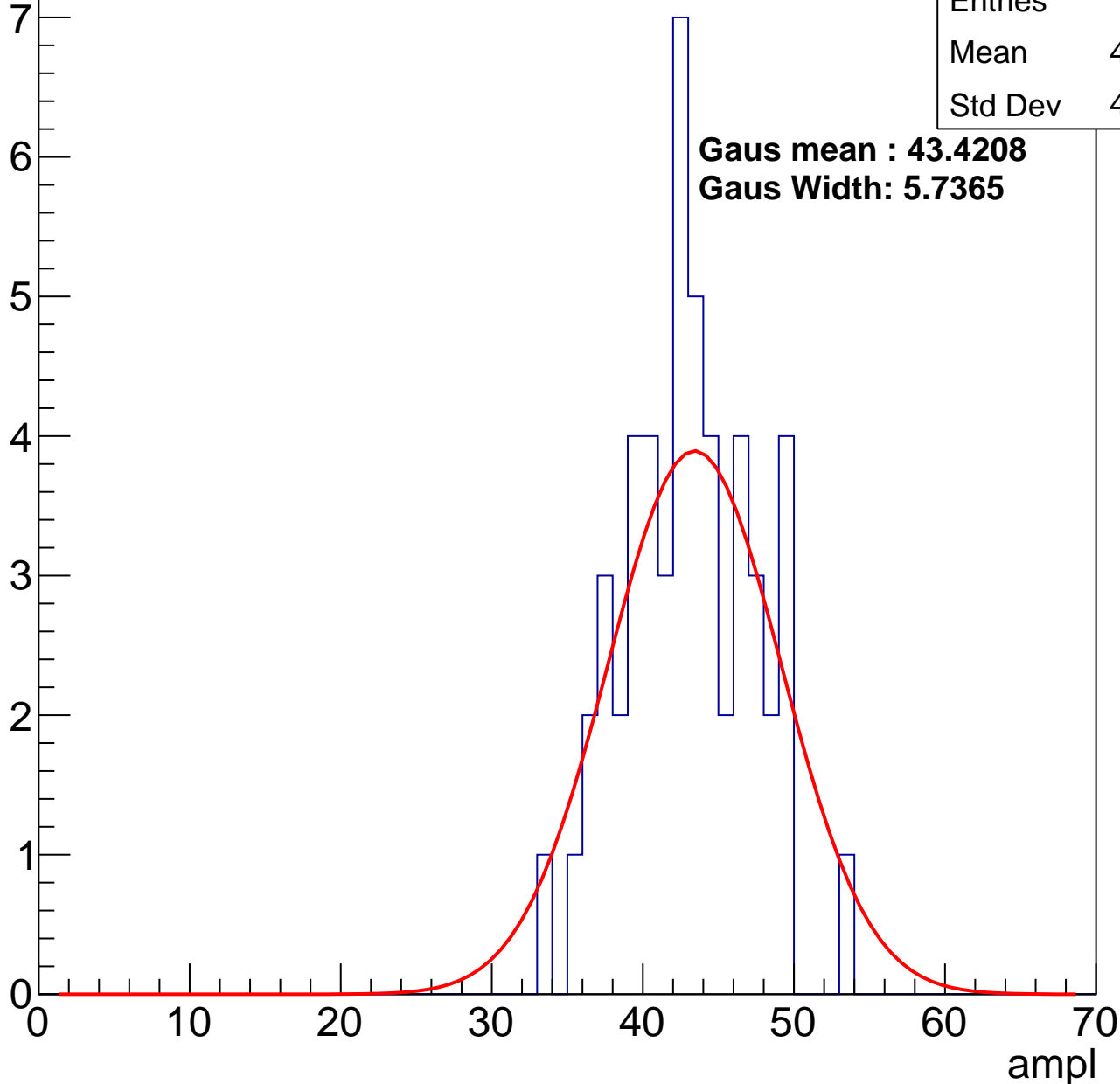
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	42.52
Std Dev	4.199

**Gaus mean : 43.4208**

**Gaus Width: 5.7365**

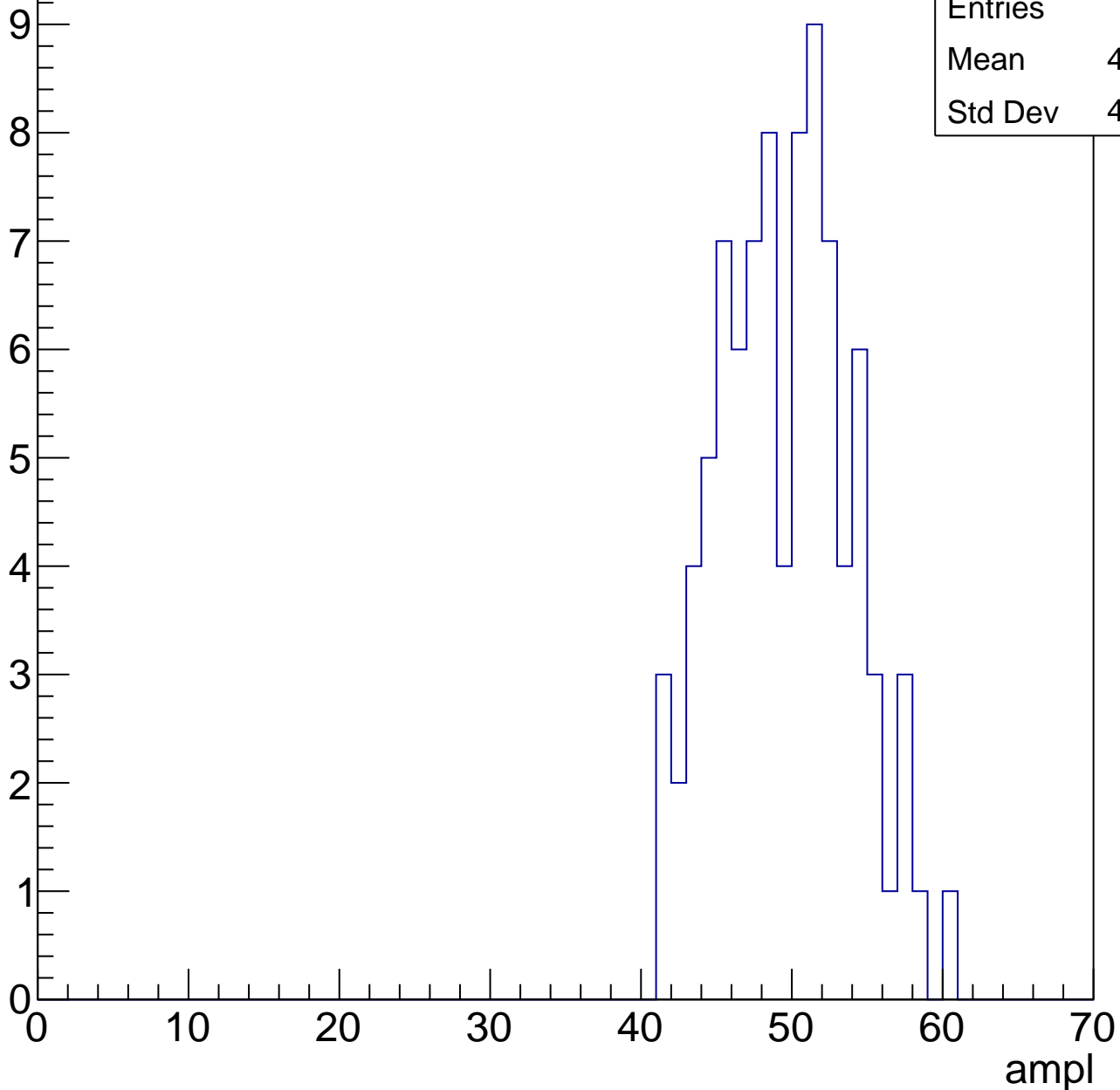


# B1L103S, U26-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

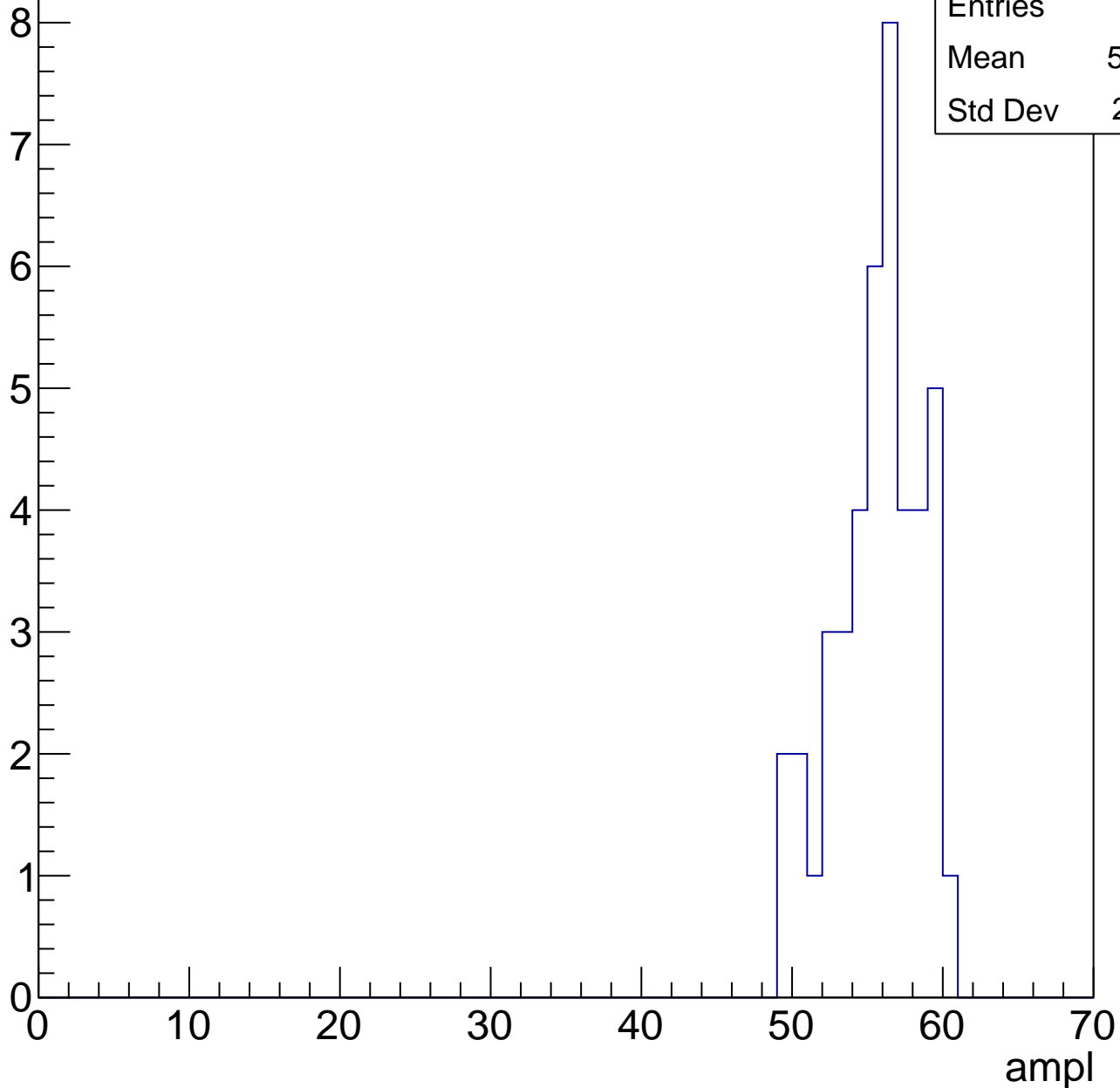
Entries	89
Mean	49.08
Std Dev	4.283



# B1L103S, U26-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	43
Mean	55.19
Std Dev	2.831

# B1L103S, U26-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

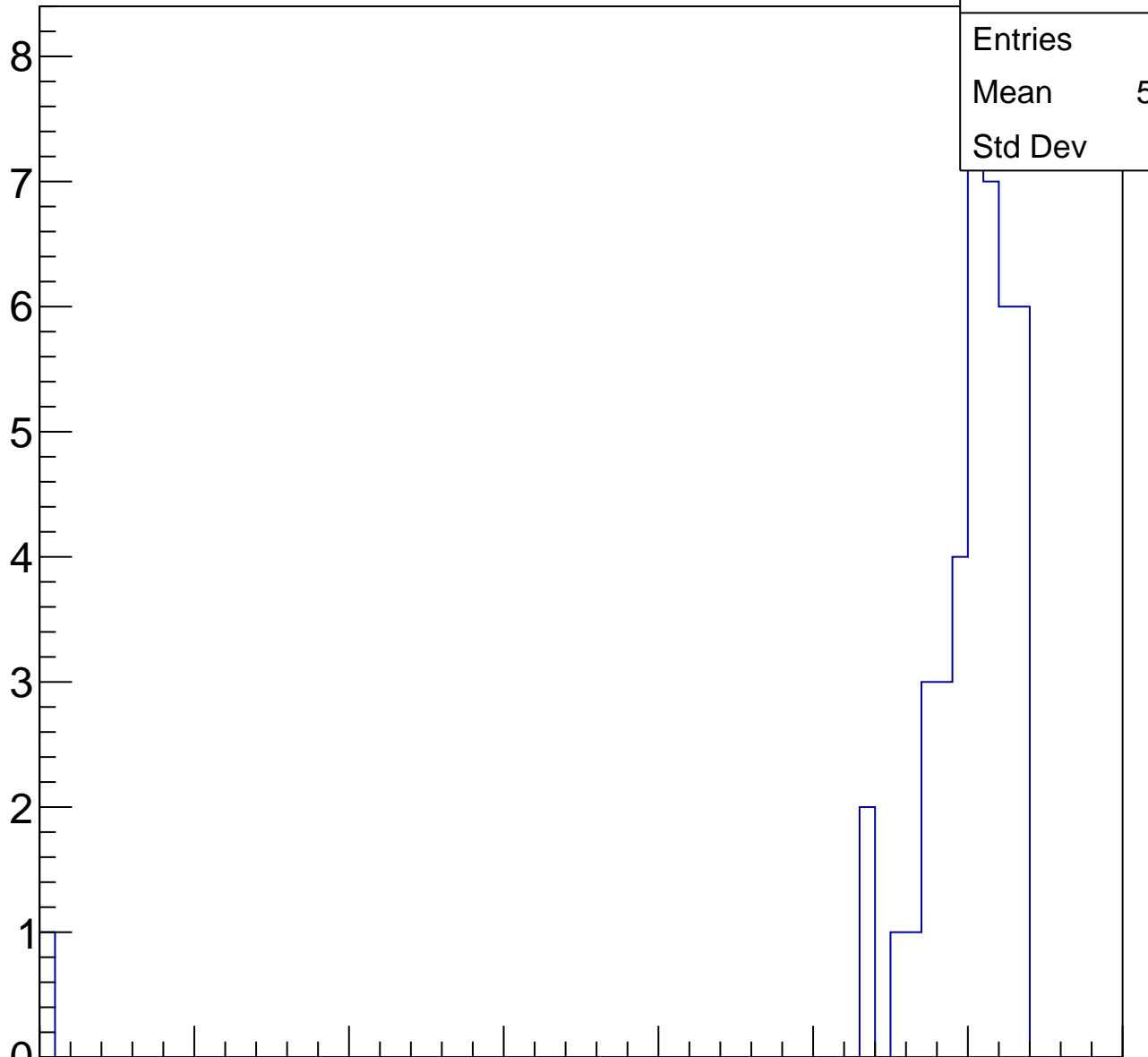
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	42
Mean	58.45
Std Dev	9.47

ampl

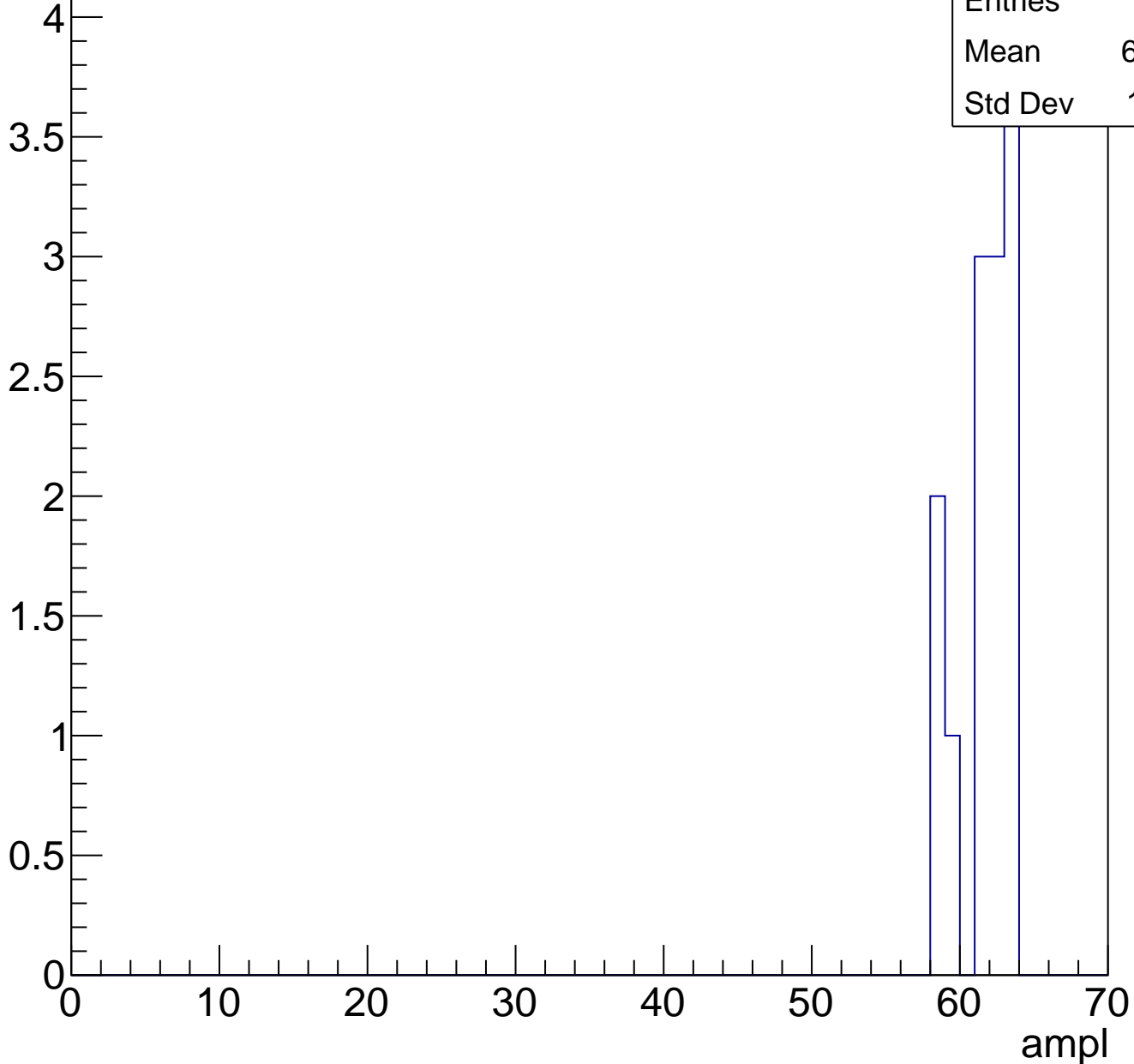
0 10 20 30 40 50 60 70



# B1L103S, U26-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

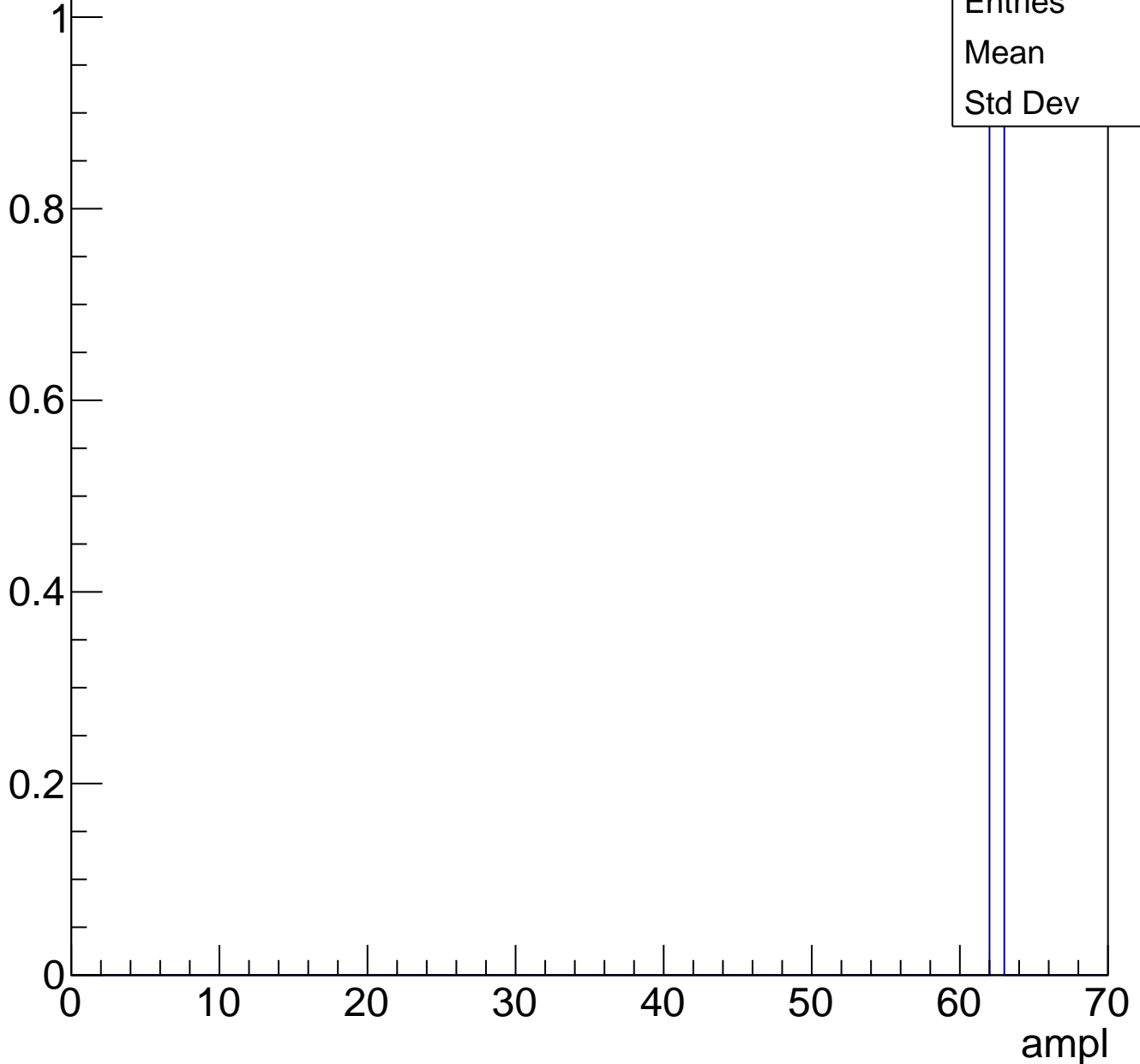




# B1L103S, U26-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	62
Std Dev	0

# B1L103S, U26-ch103, adc0

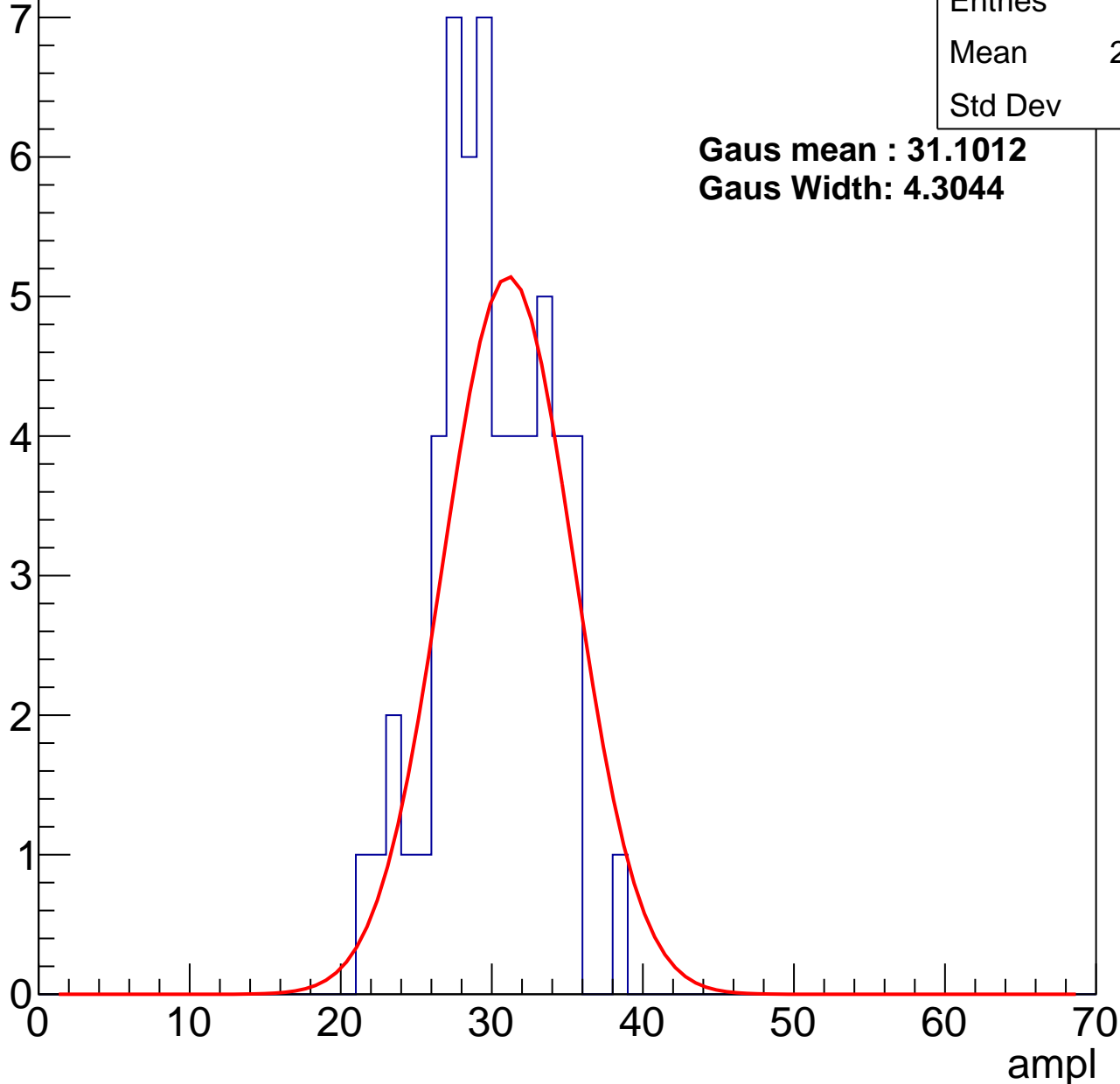
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	29.52
Std Dev	3.64

**Gaus mean : 31.1012**

**Gaus Width: 4.3044**



# B1L103S, U26-ch103, adc1

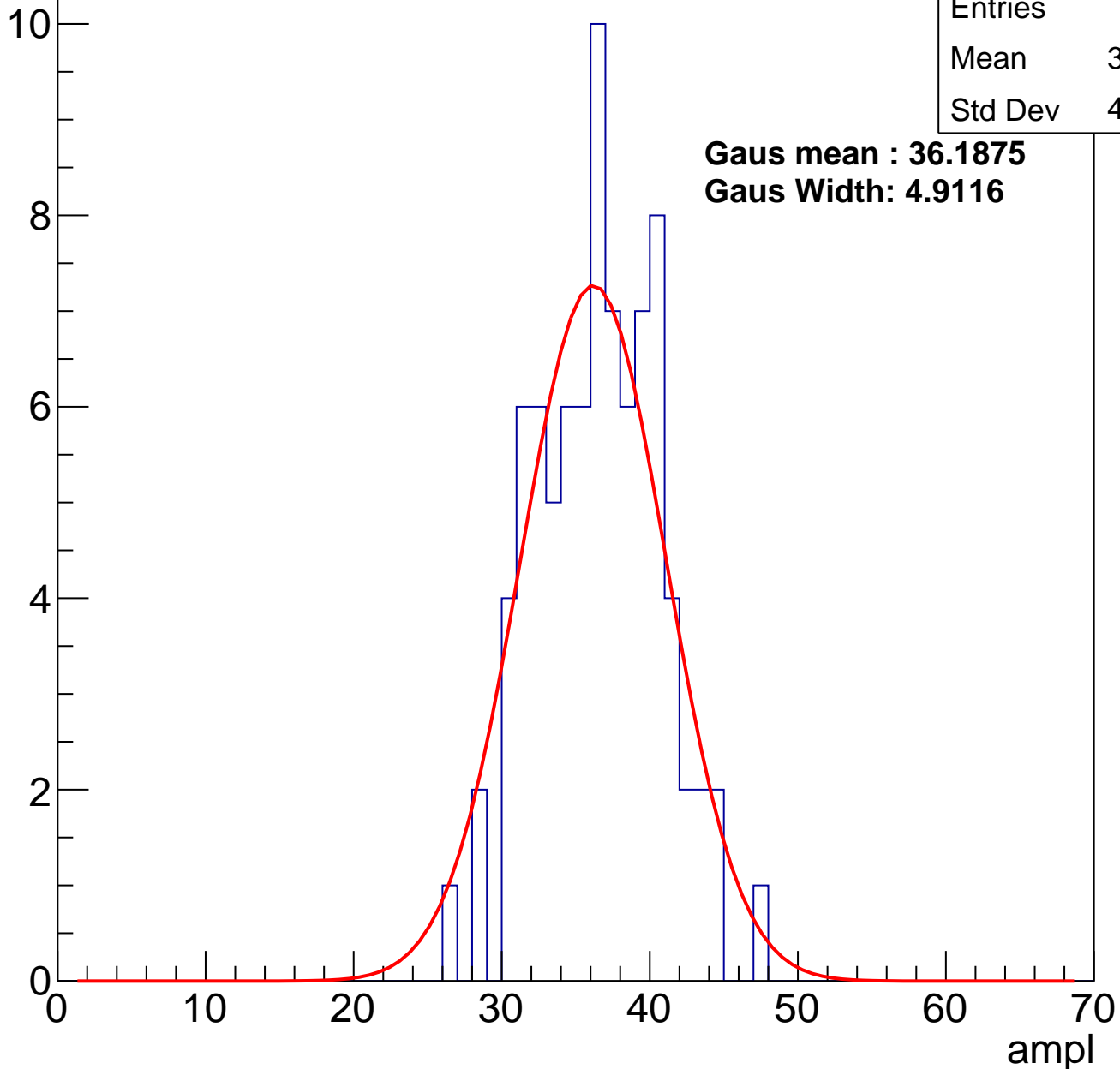
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	85
Mean	36.09
Std Dev	4.106

**Gaus mean : 36.1875**

**Gaus Width: 4.9116**

Entry



# B1L103S, U26-ch103, adc2

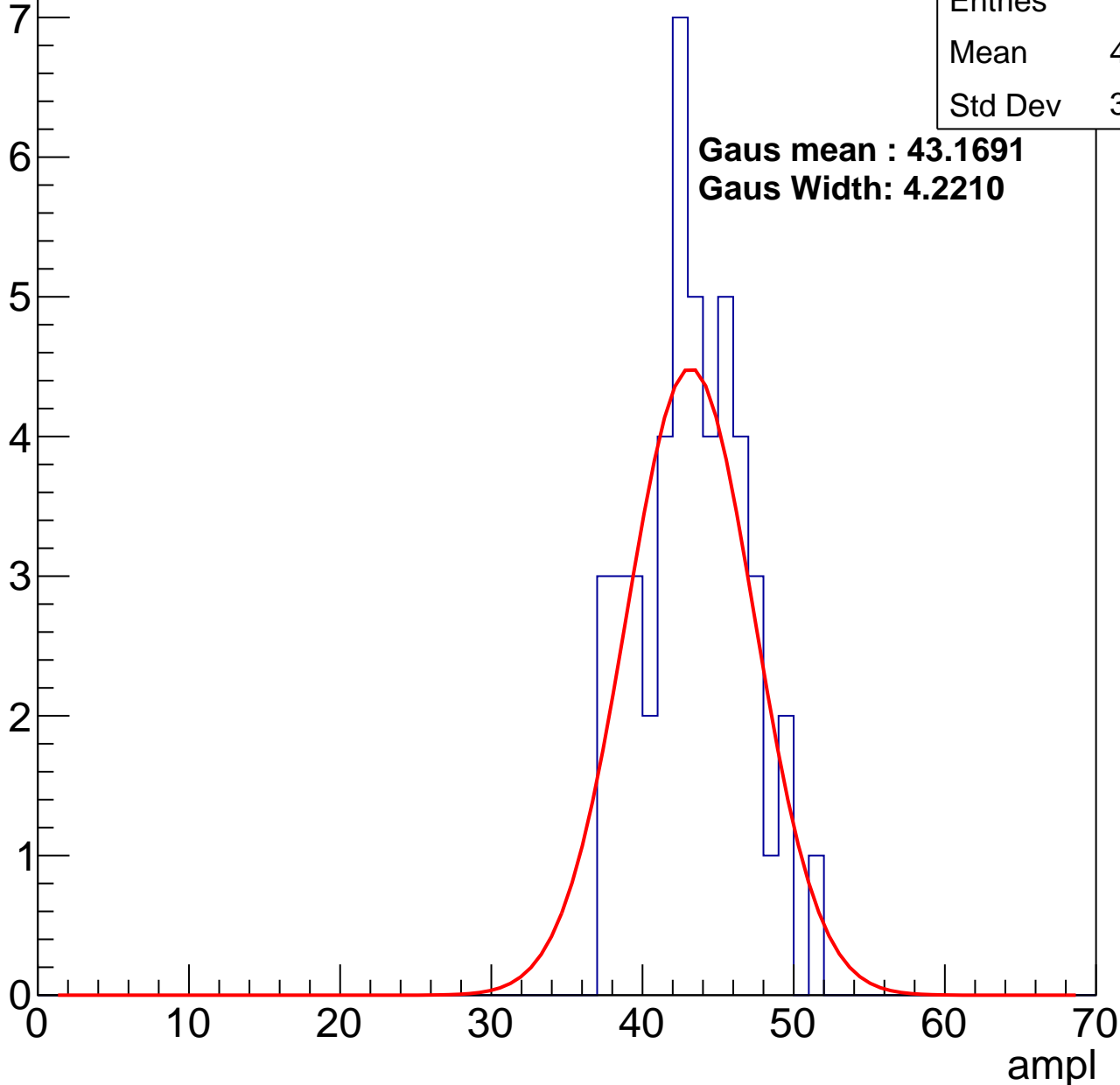
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	47
Mean	42.94
Std Dev	3.392

**Gaus mean : 43.1691**

**Gaus Width: 4.2210**

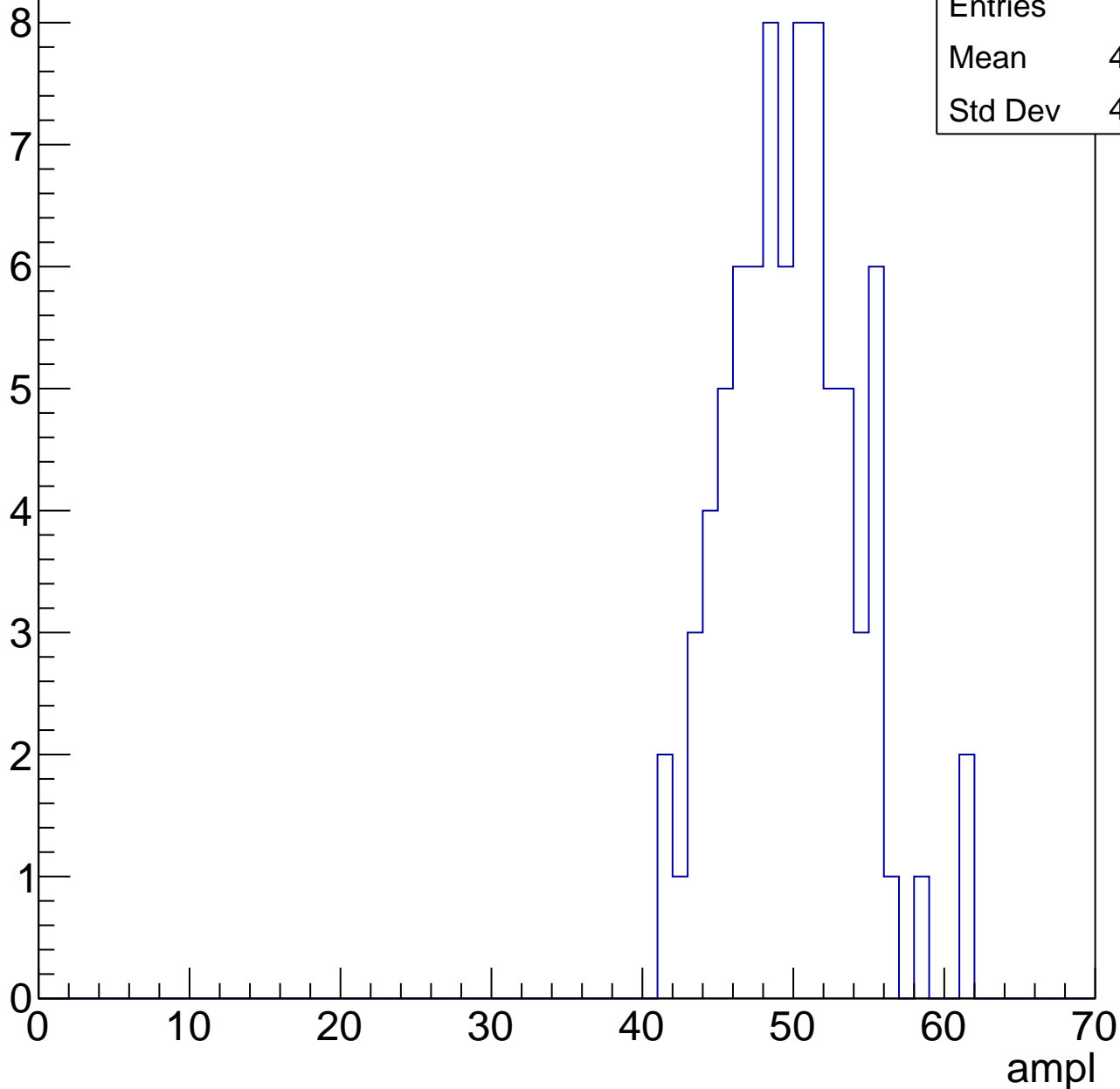


# B1L103S, U26-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	80
Mean	49.39
Std Dev	4.203

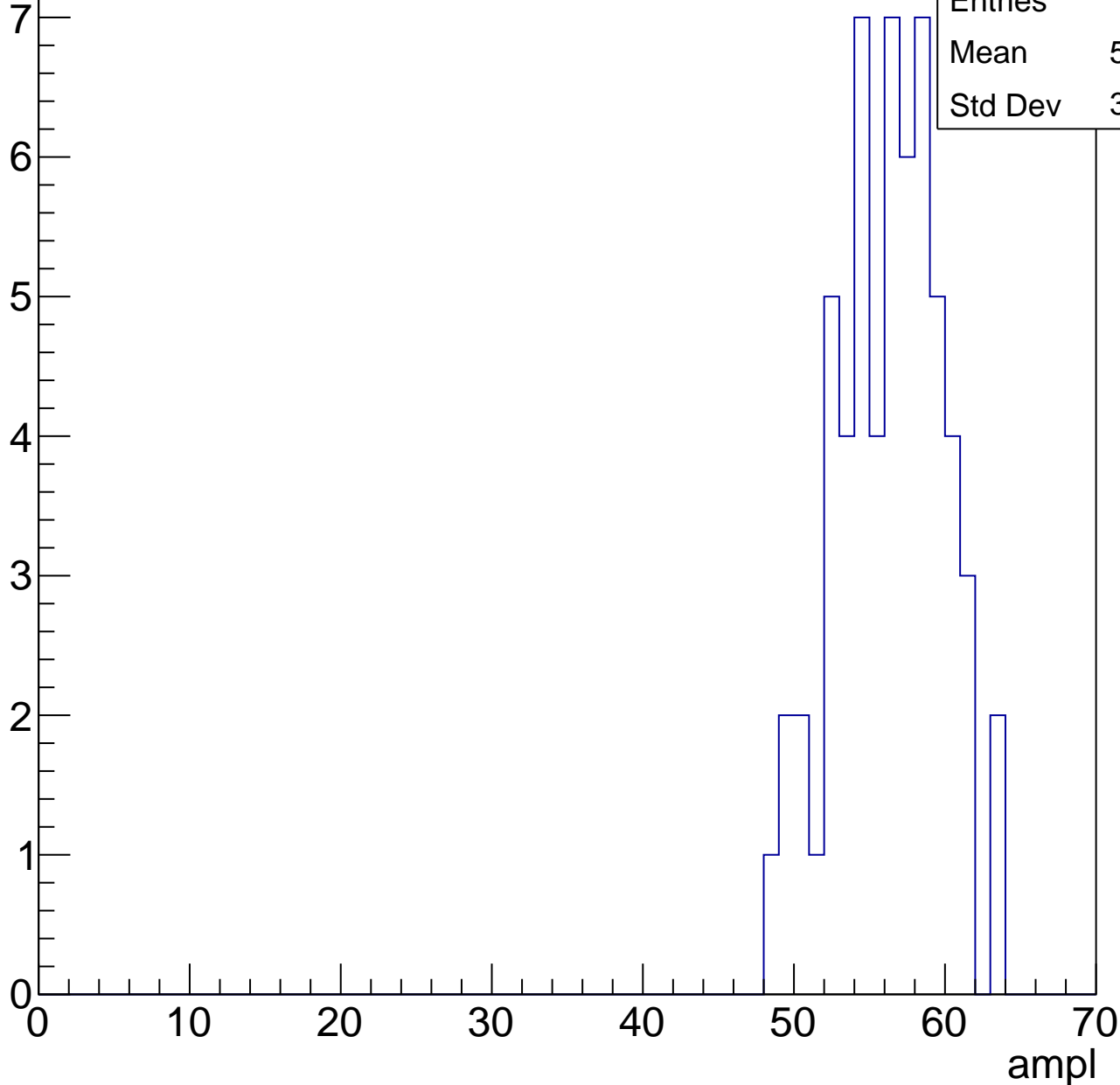


# B1L103S, U26-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	55.85
Std Dev	3.468

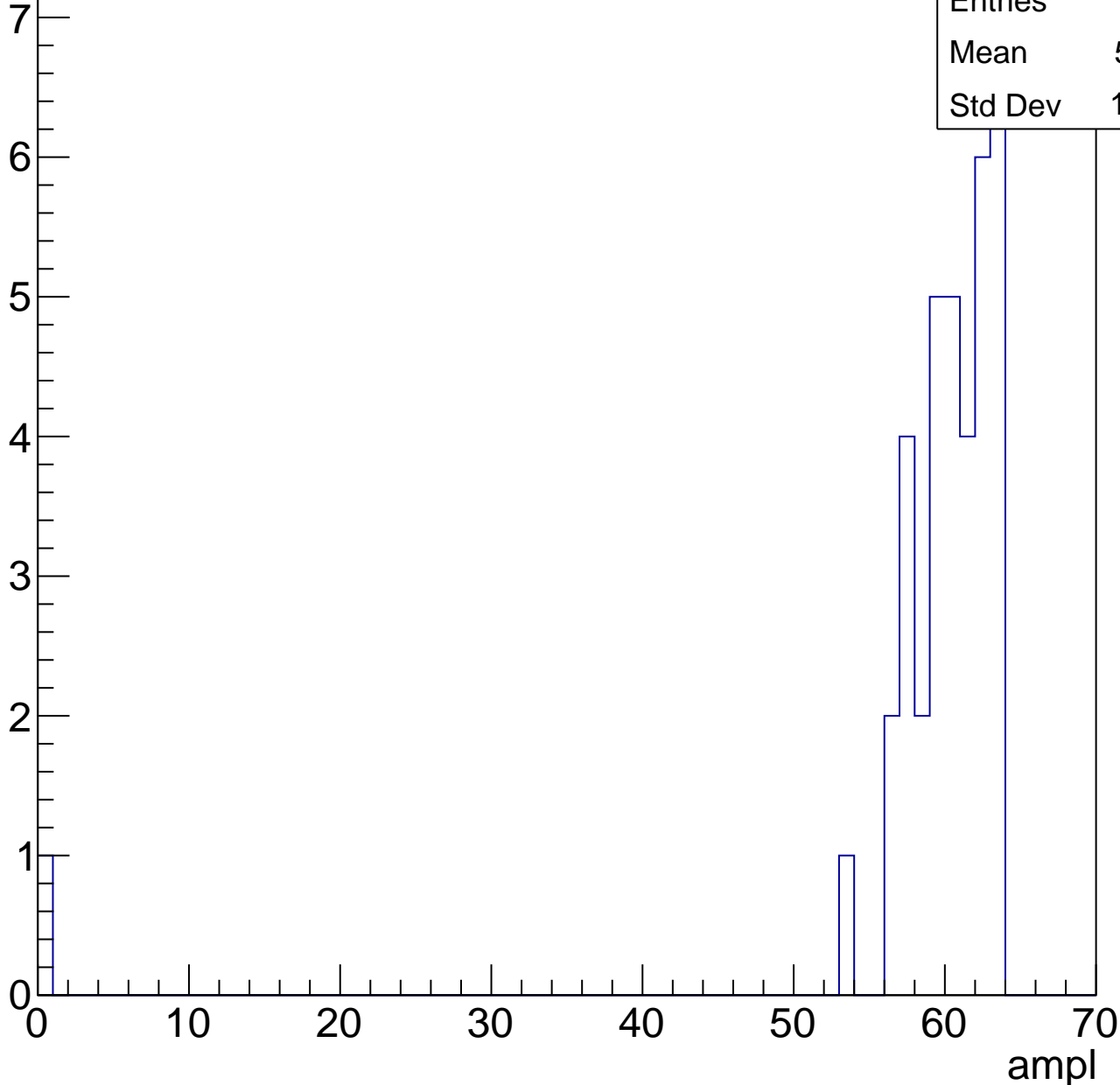


# B1L103S, U26-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

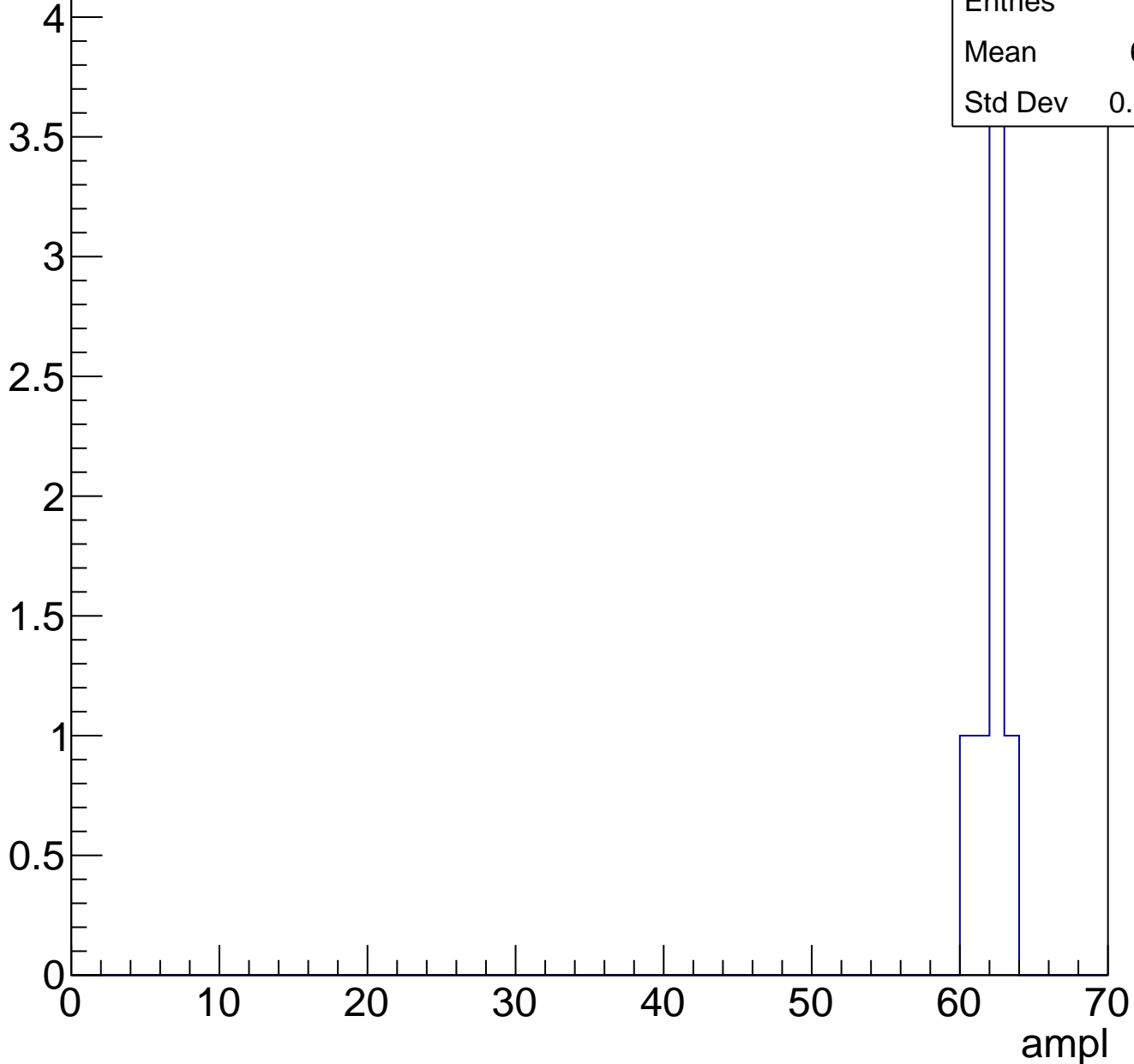
Entries	37
Mean	58.41
Std Dev	10.04



# B1L103S, U26-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch104, adc0

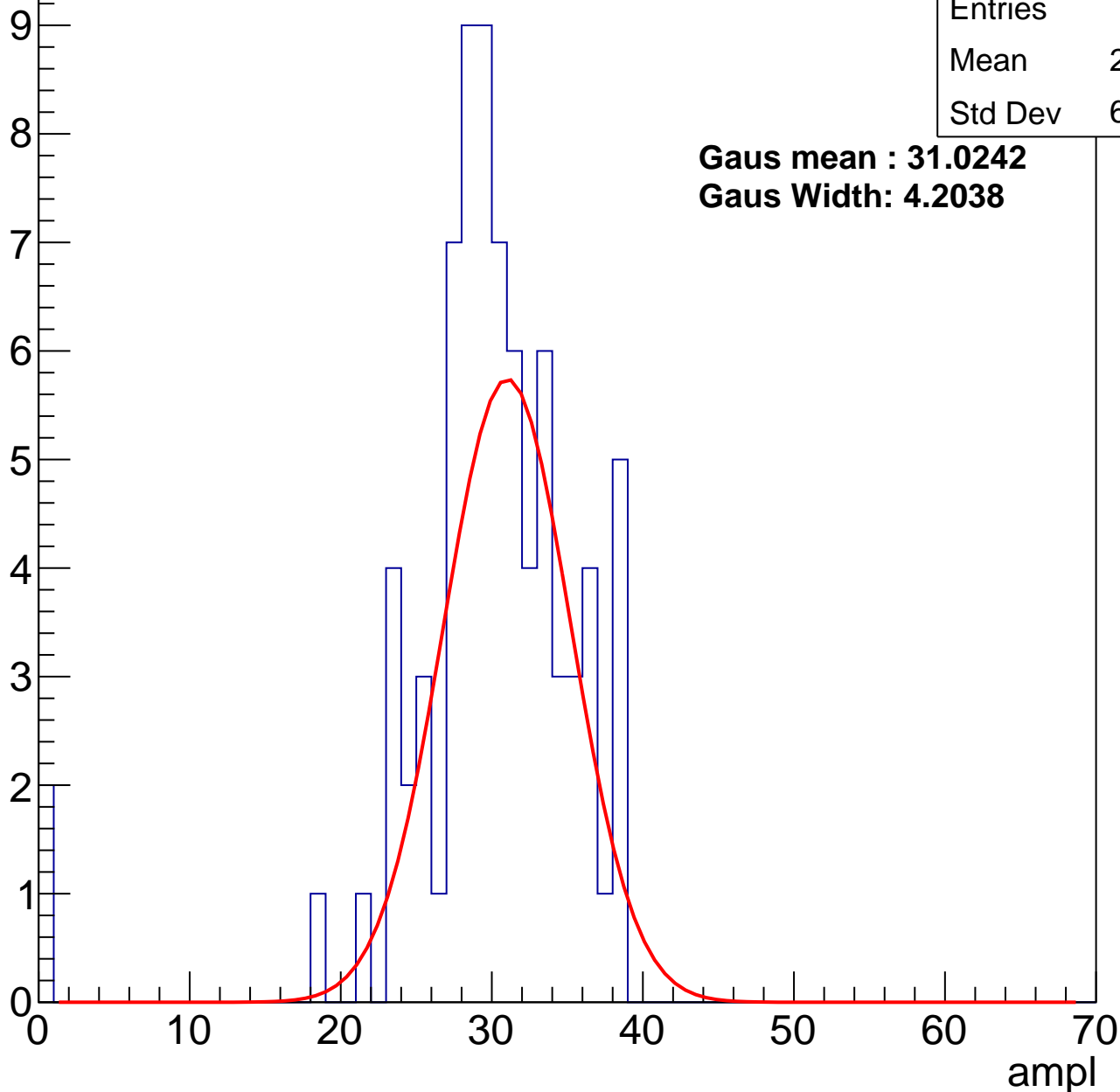
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	29.26
Std Dev	6.366

**Gaus mean : 31.0242**

**Gaus Width: 4.2038**



# B1L103S, U26-ch104, adc1

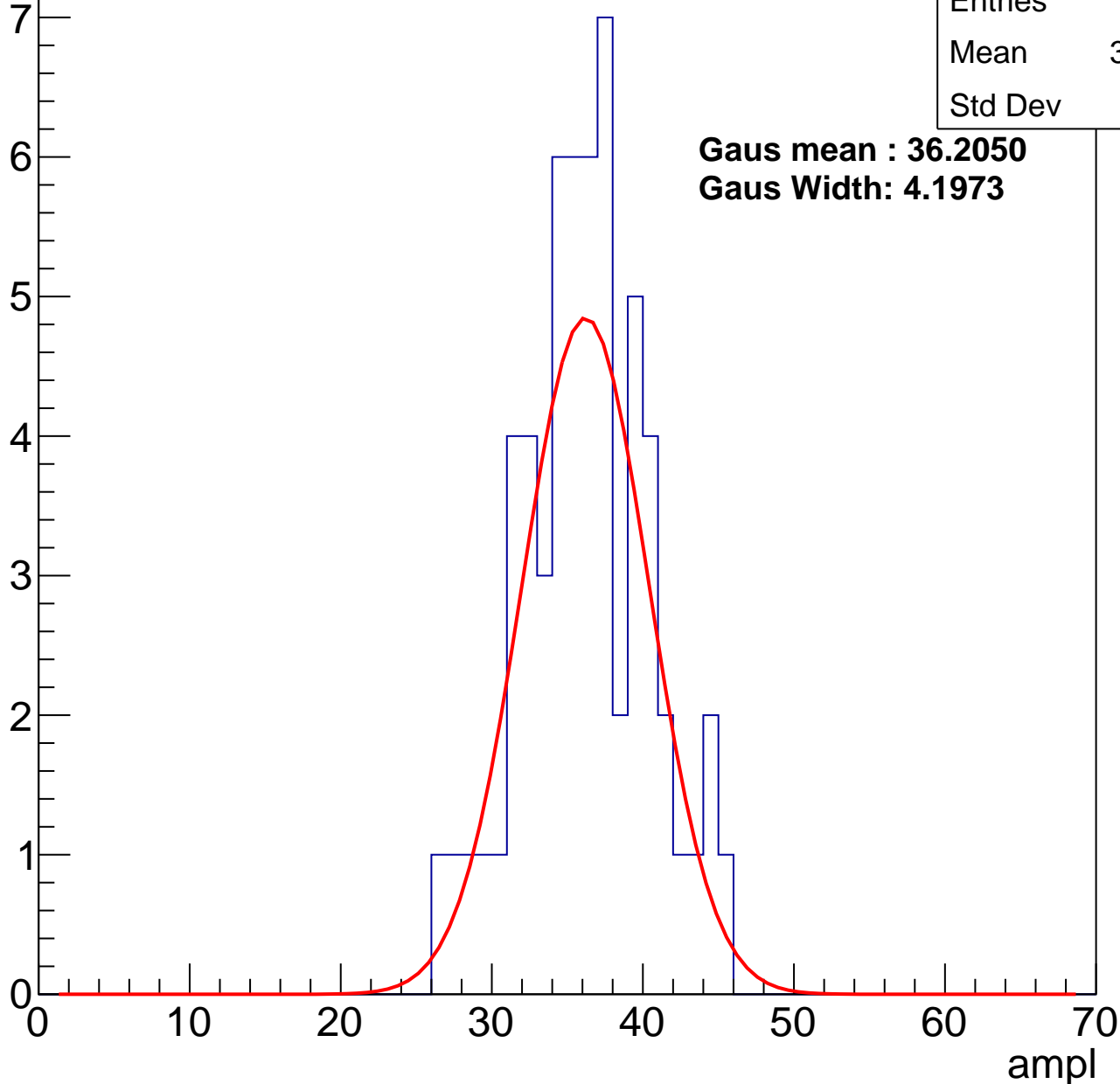
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	35.78
Std Dev	4.15

**Gaus mean : 36.2050**

**Gaus Width: 4.1973**



# B1L103S, U26-ch104, adc2

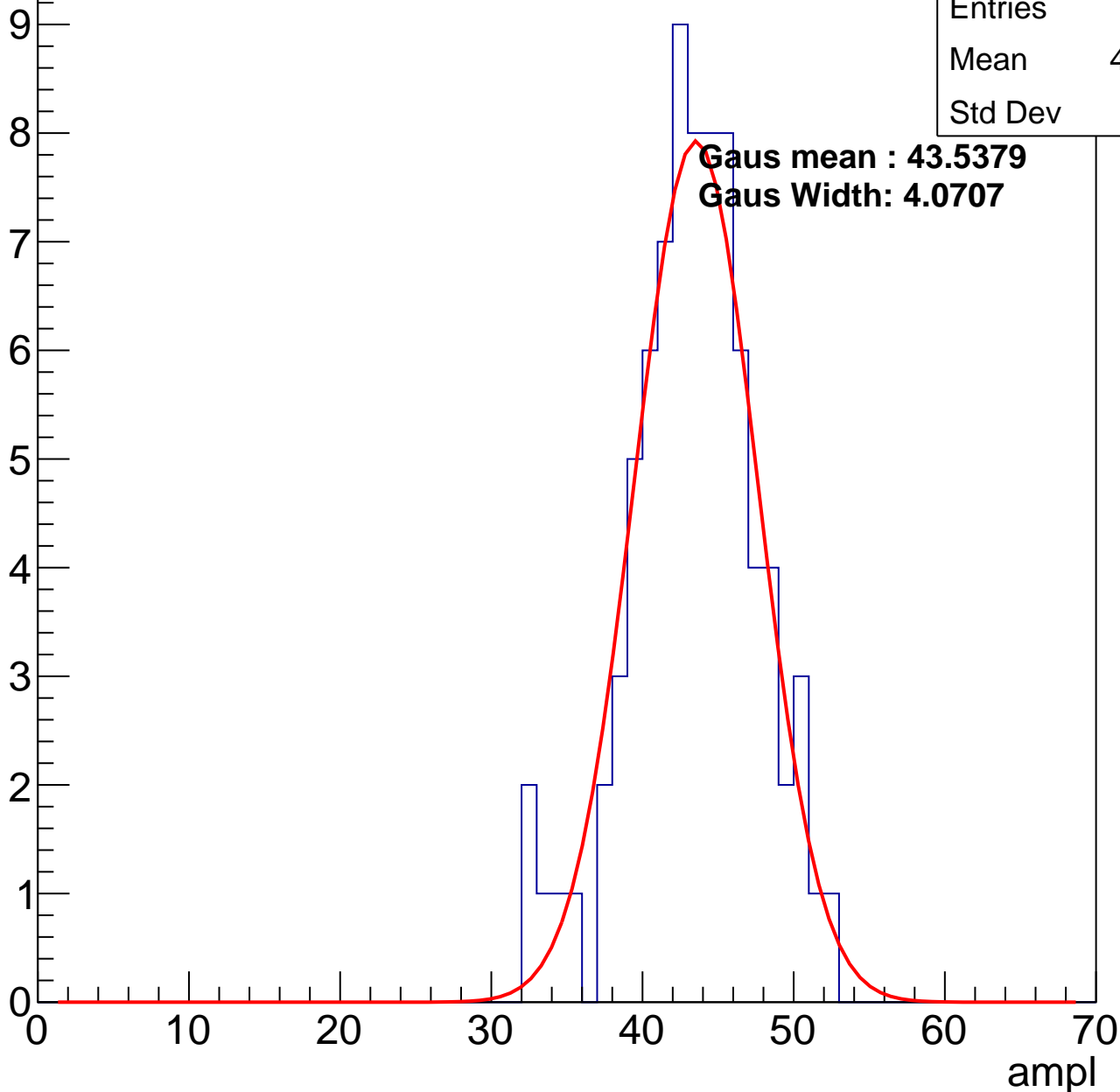
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	82
Mean	42.89
Std Dev	4.17

**Gaus mean : 43.5379**

**Gaus Width: 4.0707**

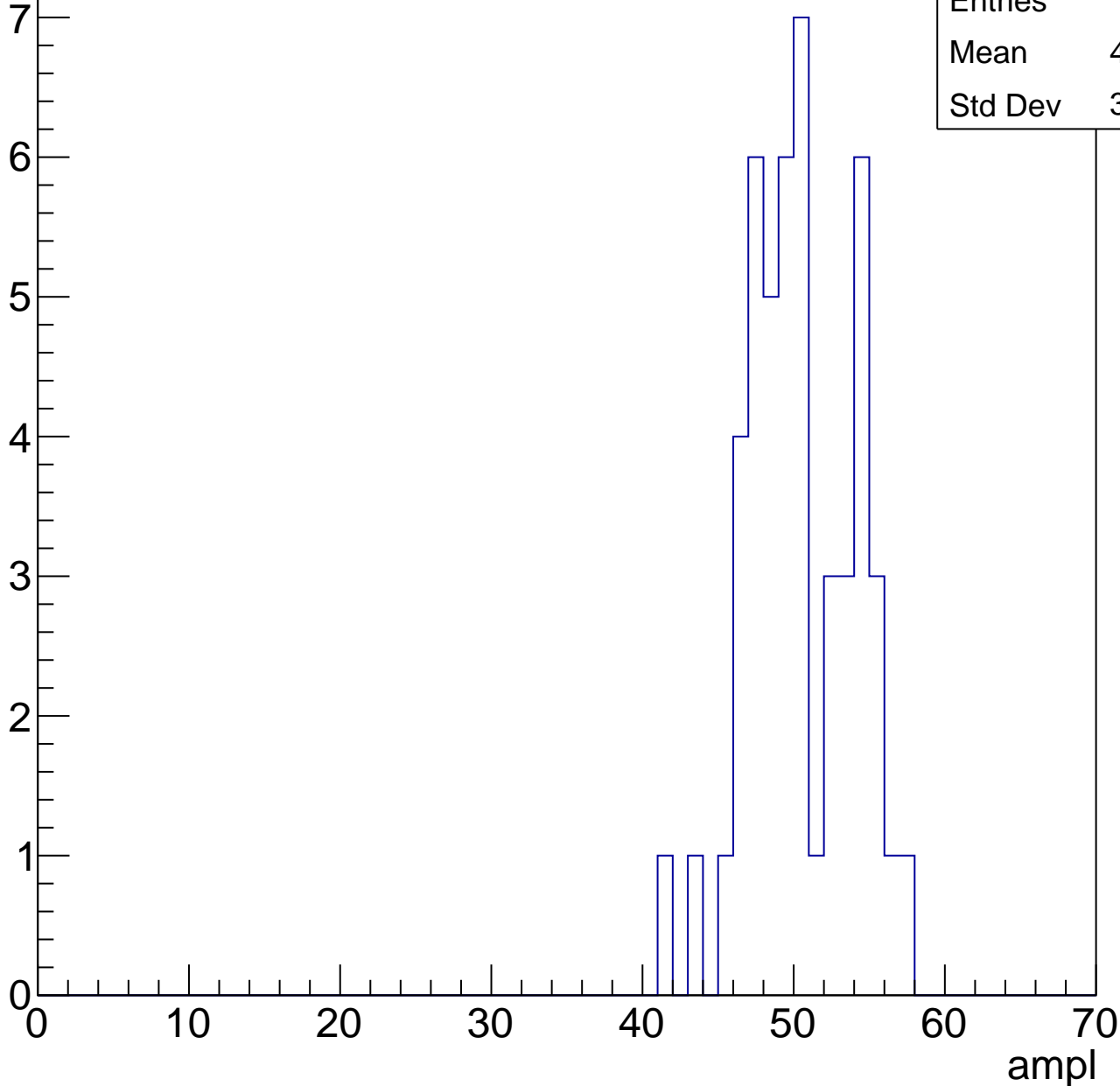


# B1L103S, U26-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	49.94
Std Dev	3.484

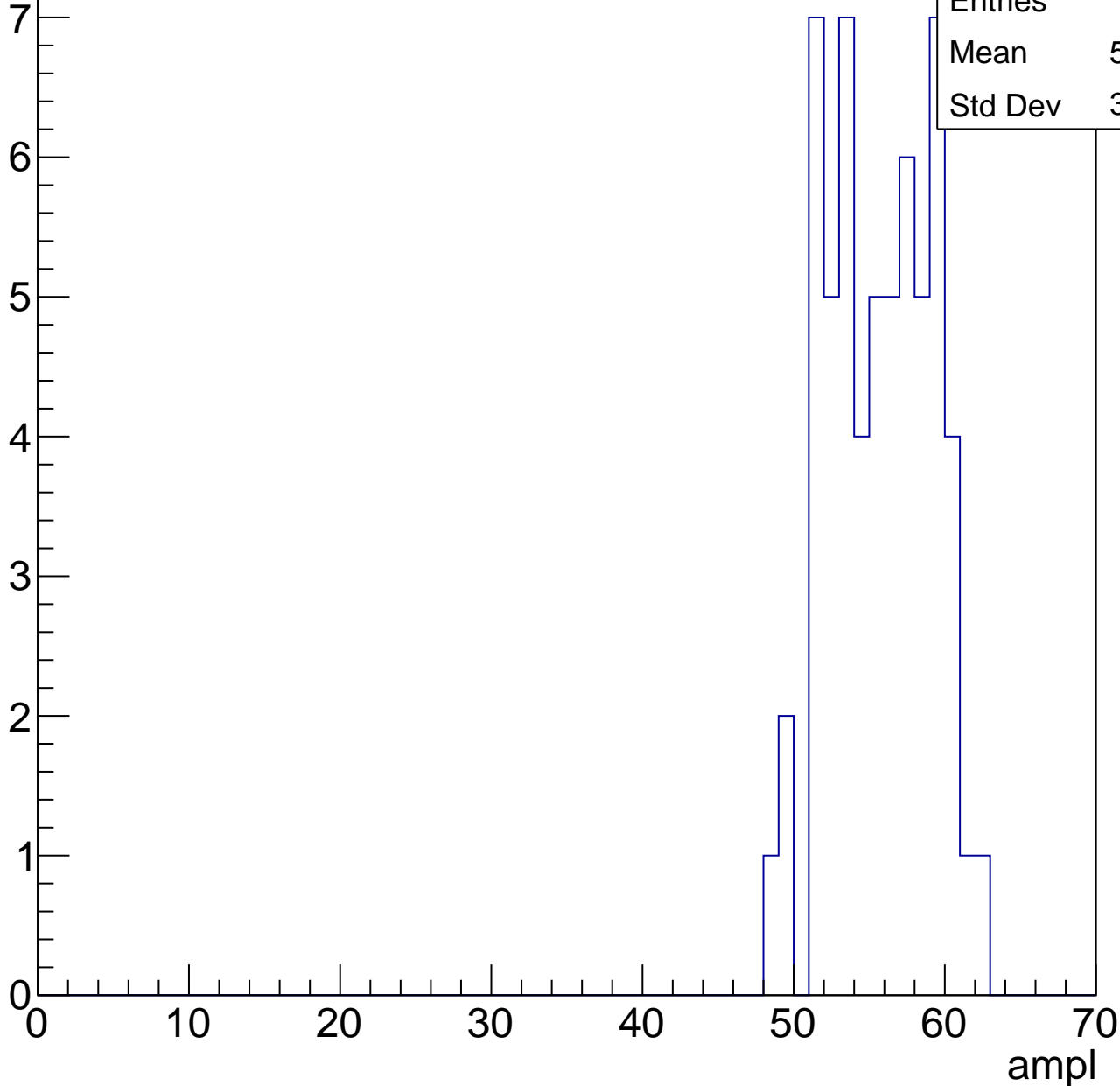


# B1L103S, U26-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	55.22
Std Dev	3.362

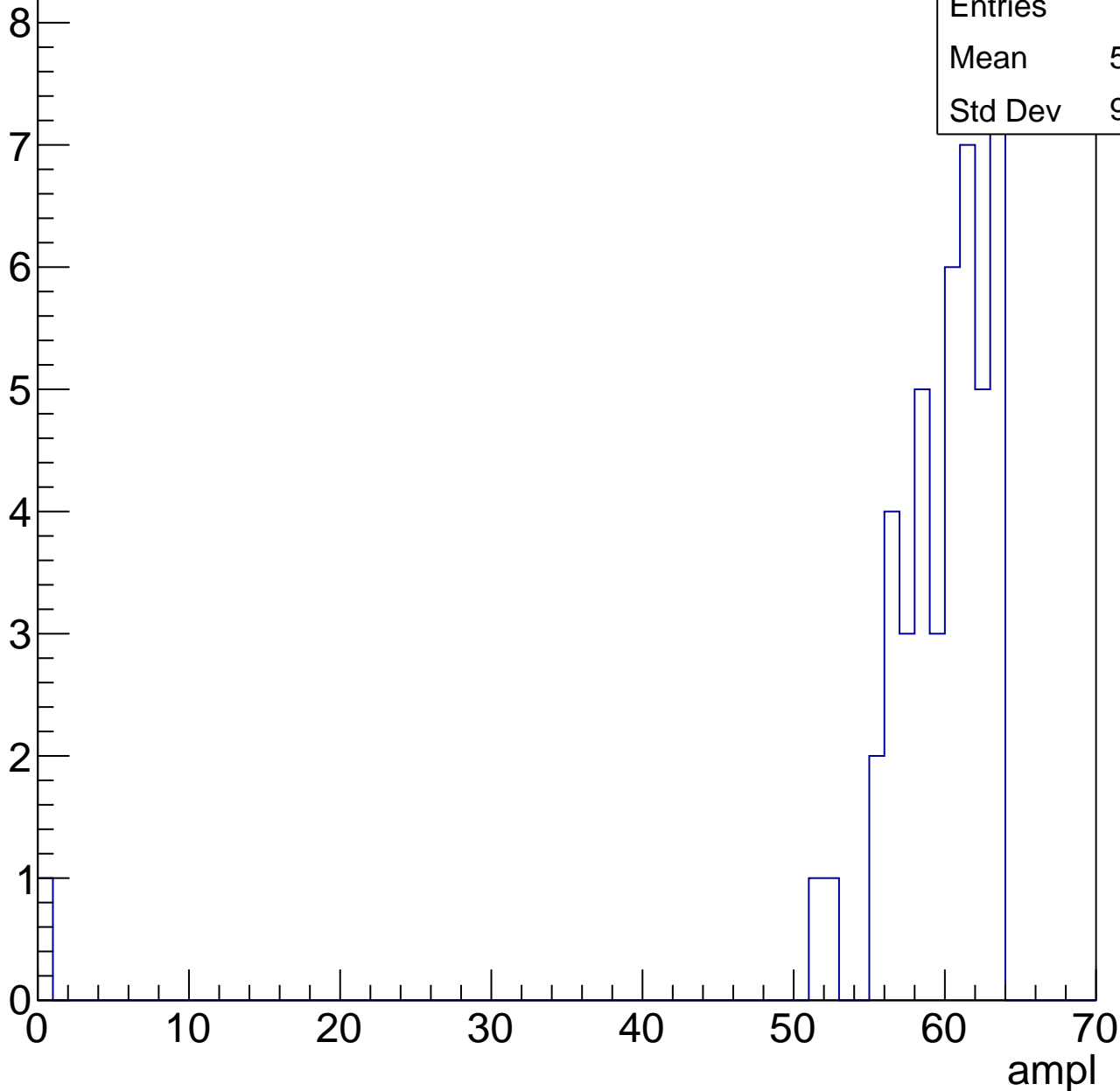


# B1L103S, U26-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	58.17
Std Dev	9.154



# B1L103S, U26-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	62
Std Dev	0.8165

ampl



# B1L103S, U26-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	41.33
Std Dev	29.23

ampl

# B1L103S, U26-ch105, adc0

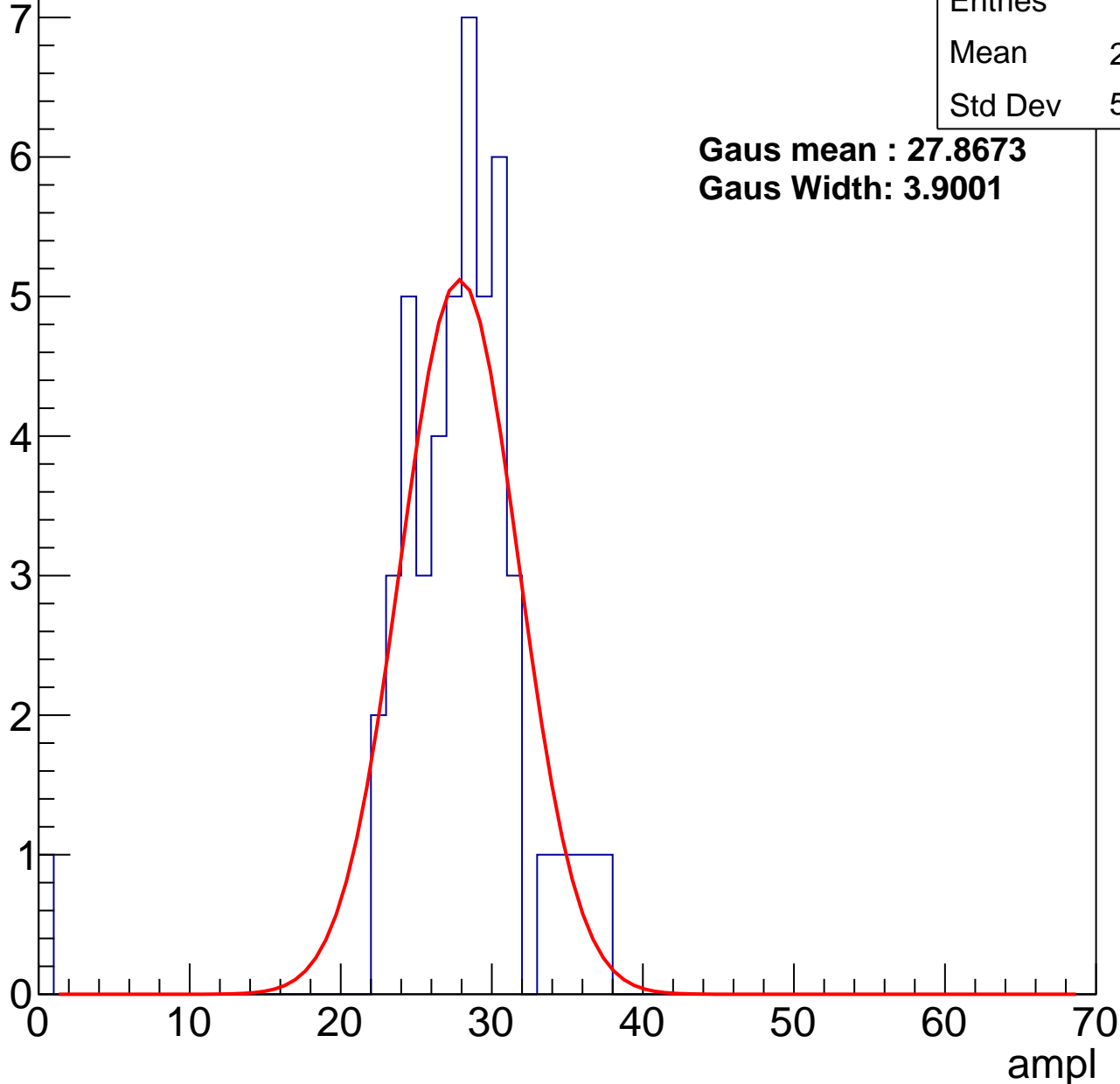
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	27.27
Std Dev	5.236

**Gaus mean : 27.8673**

**Gaus Width: 3.9001**



# B1L103S, U26-ch105, adc1

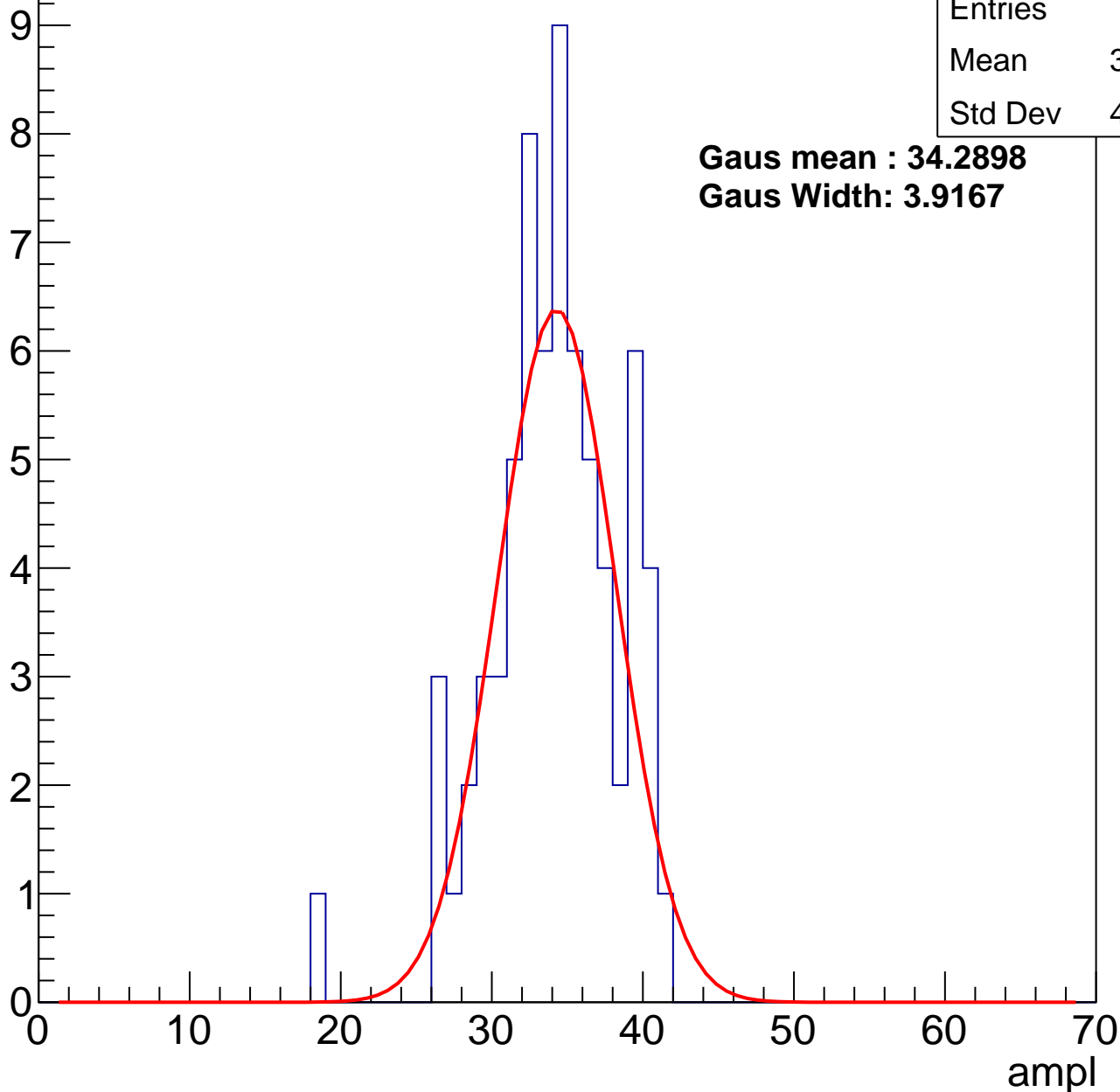
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	69
Mean	33.62
Std Dev	4.174

**Gaus mean : 34.2898**

**Gaus Width: 3.9167**



# B1L103S, U26-ch105, adc2

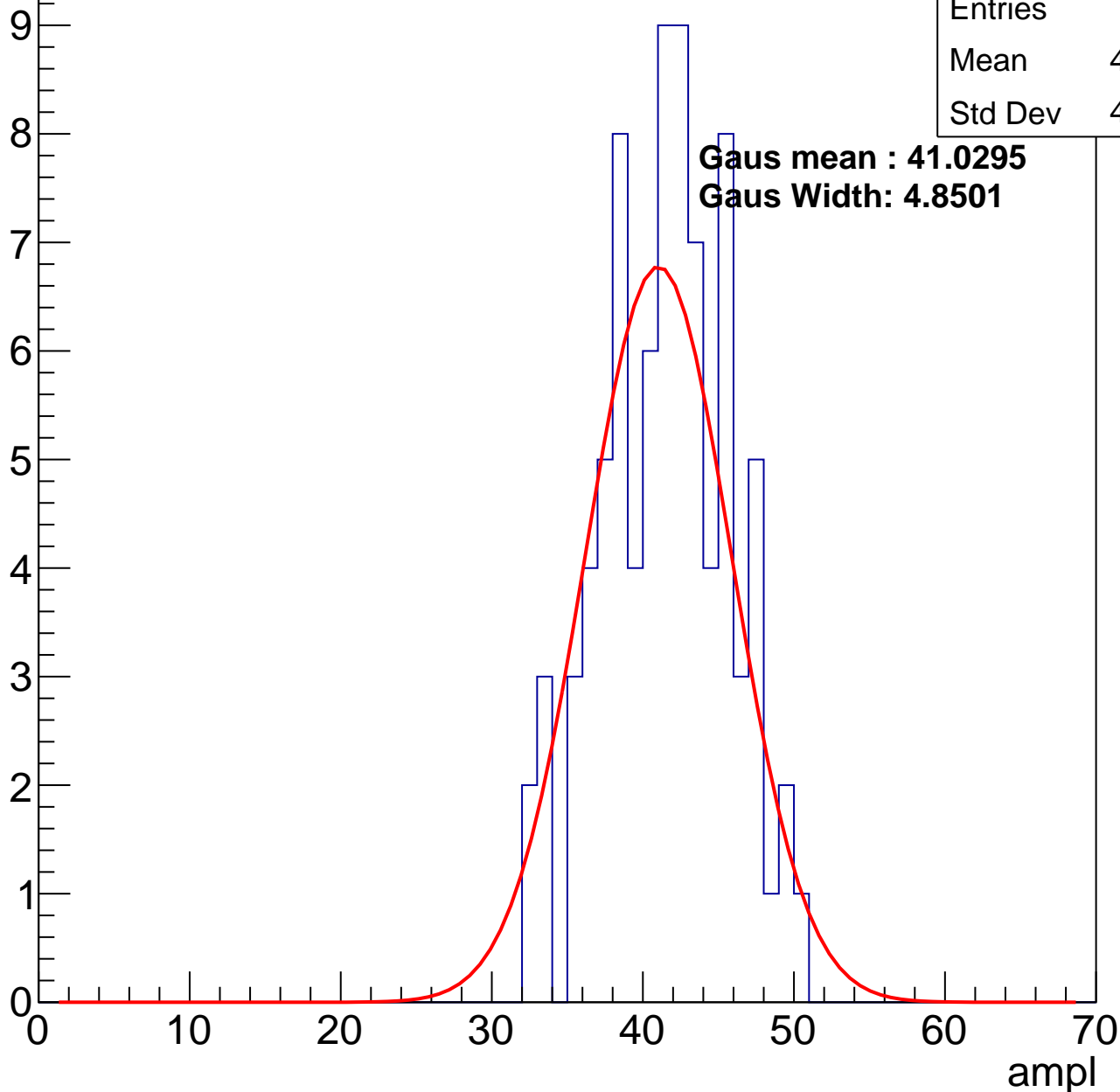
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	84
Mean	41.07
Std Dev	4.154

**Gaus mean : 41.0295**

**Gaus Width: 4.8501**

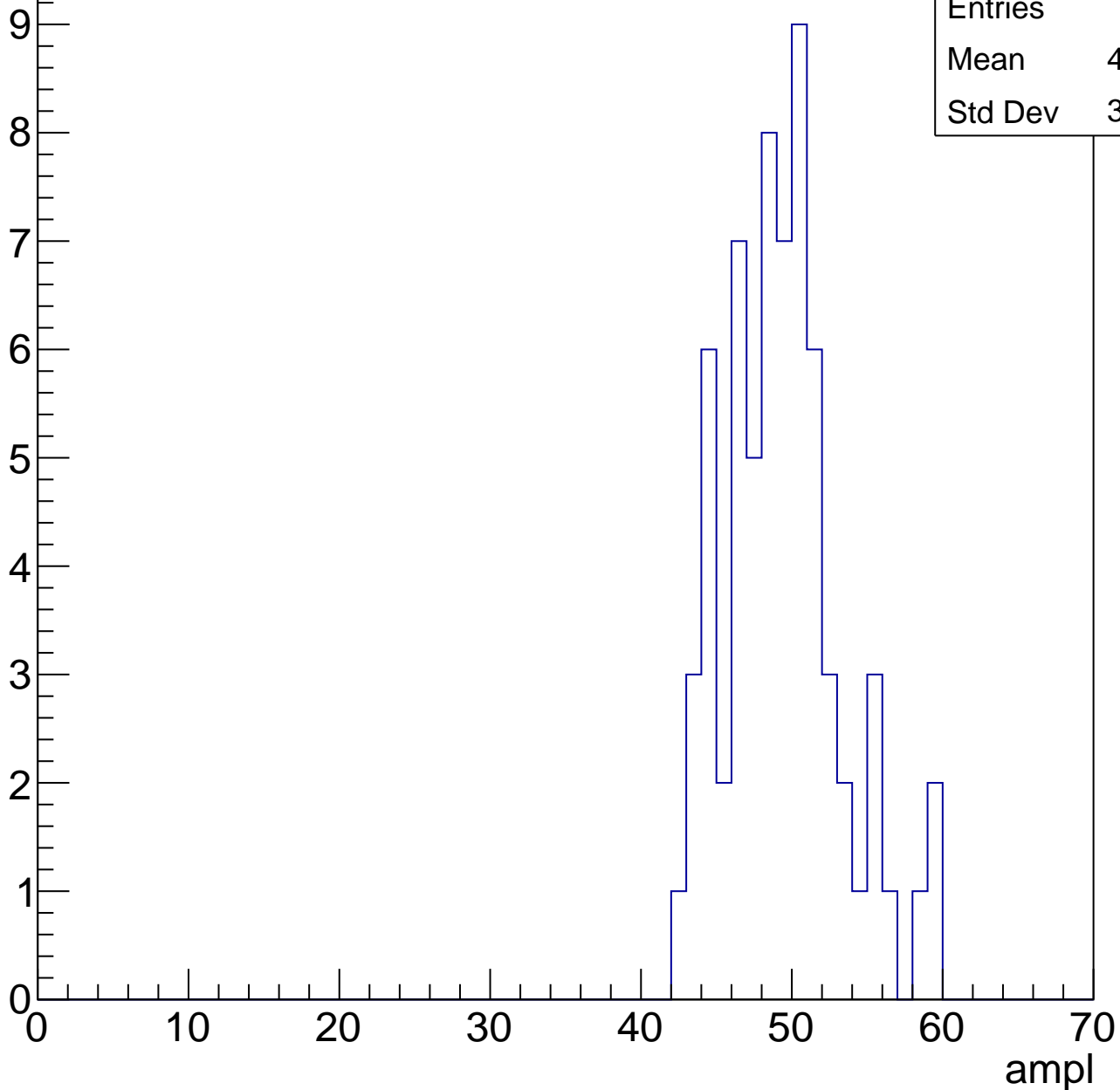


# B1L103S, U26-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	48.93
Std Dev	3.834

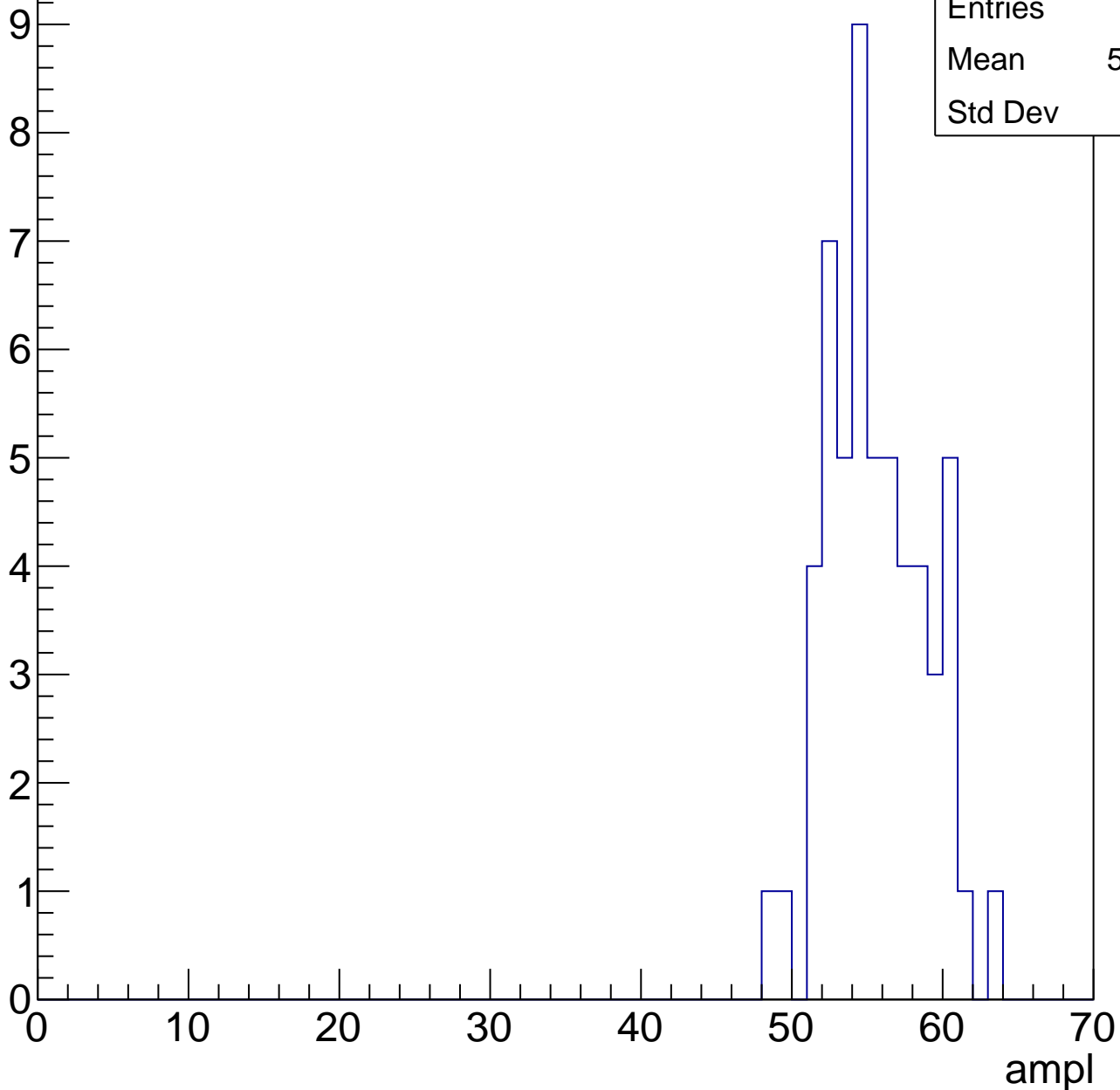


# B1L103S, U26-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	55.13
Std Dev	3.22

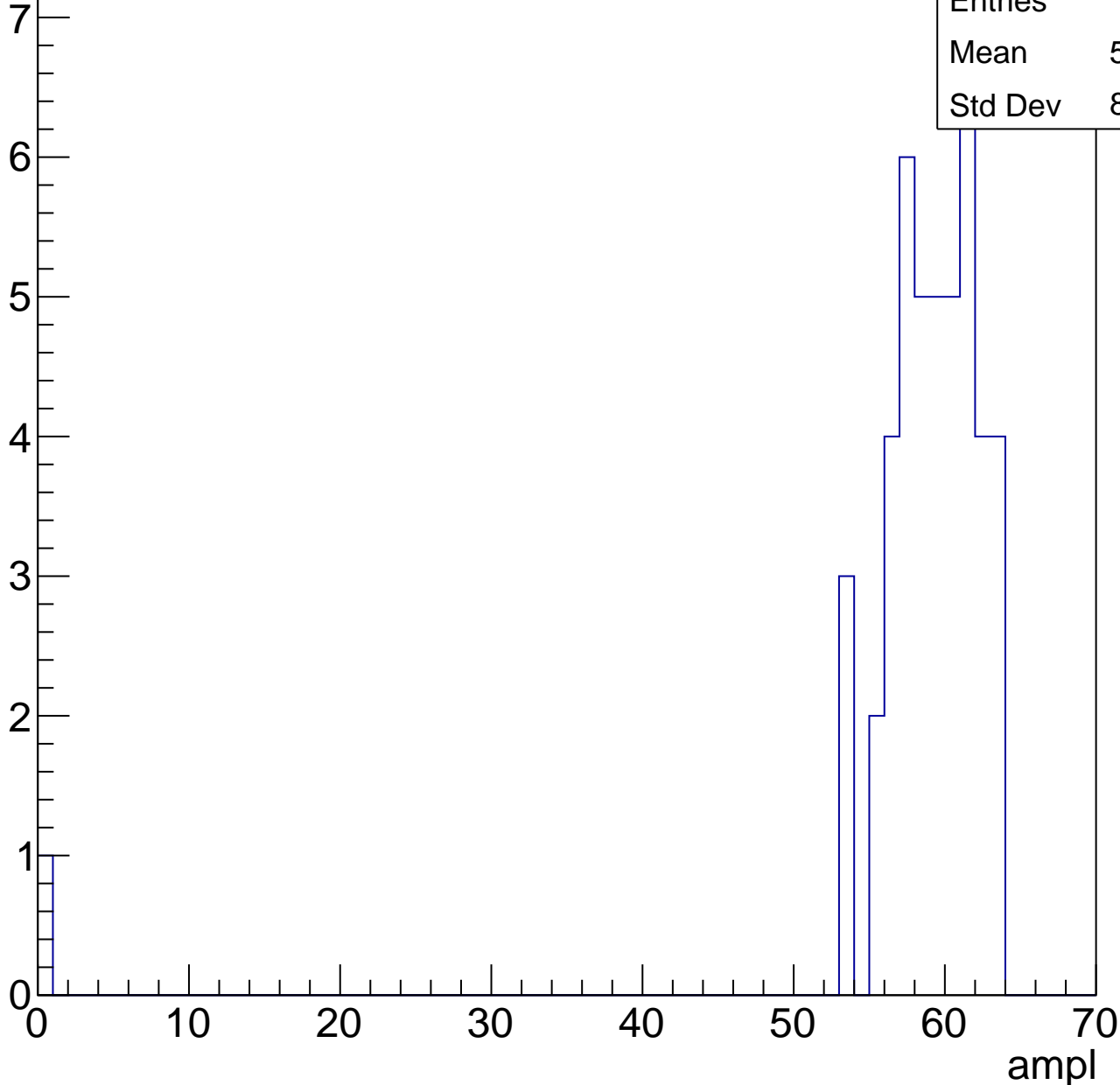


# B1L103S, U26-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	57.54
Std Dev	8.994

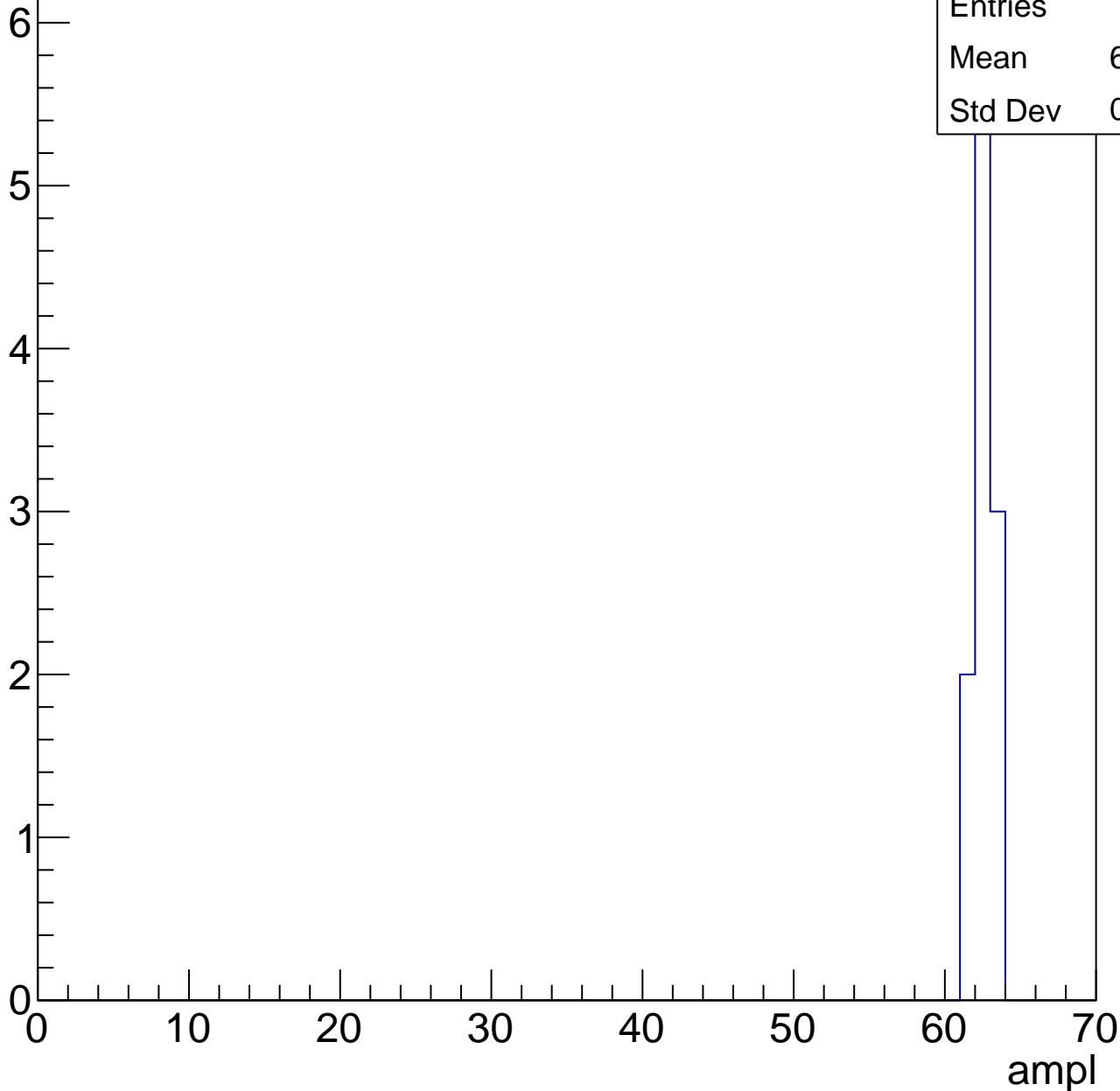


# B1L103S, U26-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	11
Mean	62.09
Std Dev	0.668





# B1L103S, U26-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch106, adc0

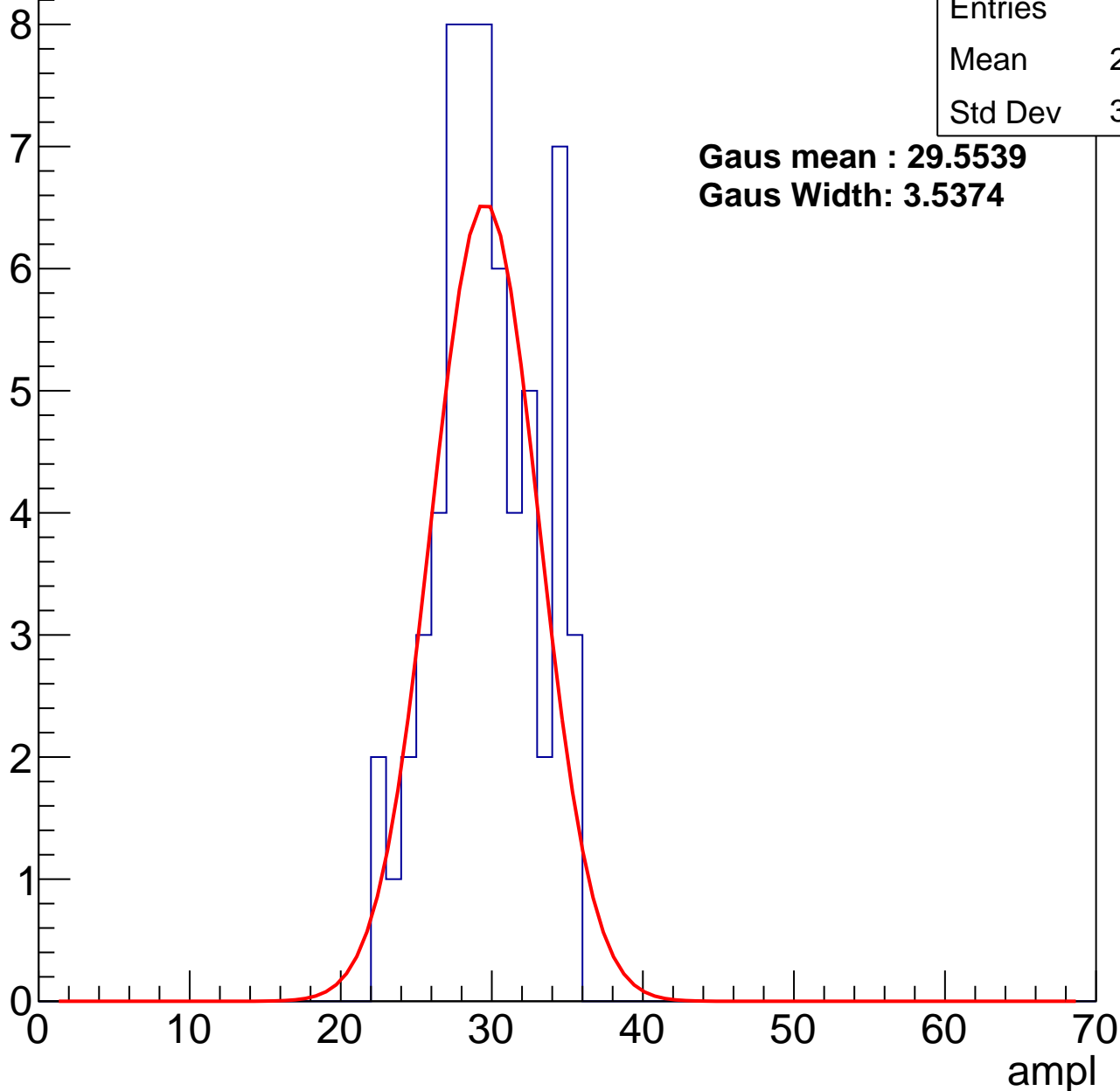
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	29.19
Std Dev	3.304

**Gaus mean : 29.5539**

**Gaus Width: 3.5374**



# B1L103S, U26-ch106, adc1

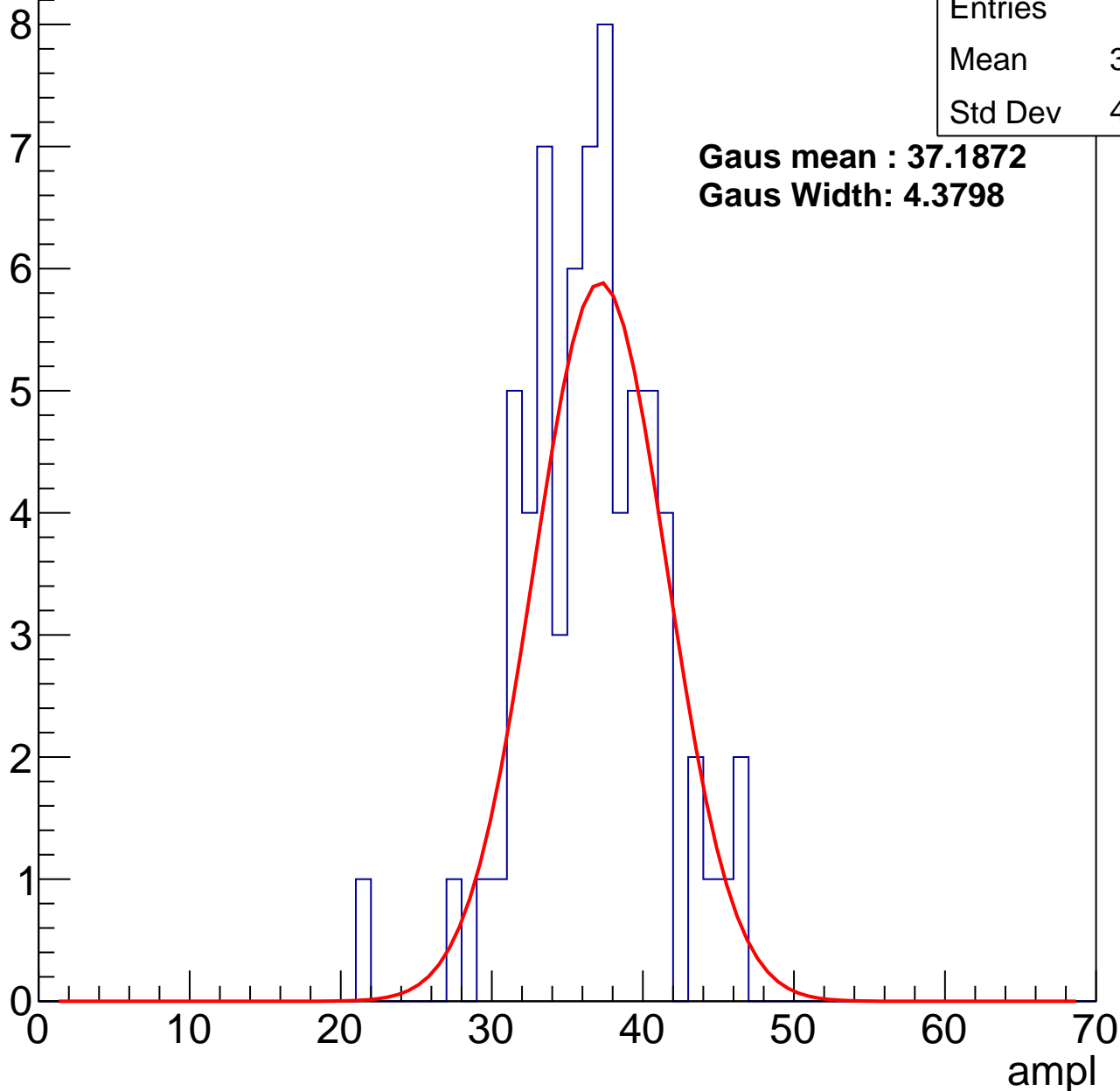
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	36.16
Std Dev	4.458

**Gaus mean : 37.1872**

**Gaus Width: 4.3798**



# B1L103S, U26-ch106, adc2

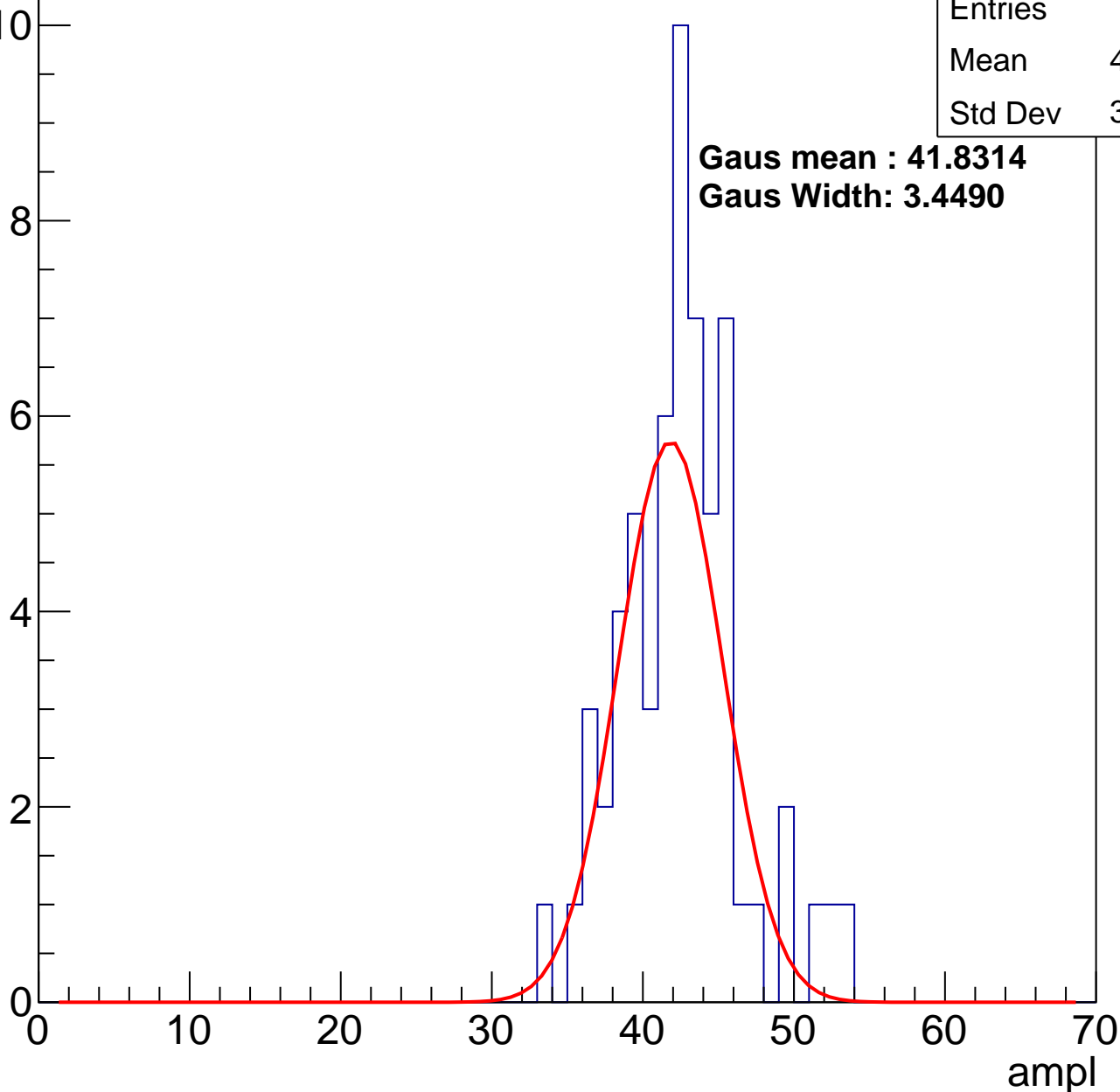
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	42.07
Std Dev	3.937

**Gaus mean : 41.8314**

**Gaus Width: 3.4490**

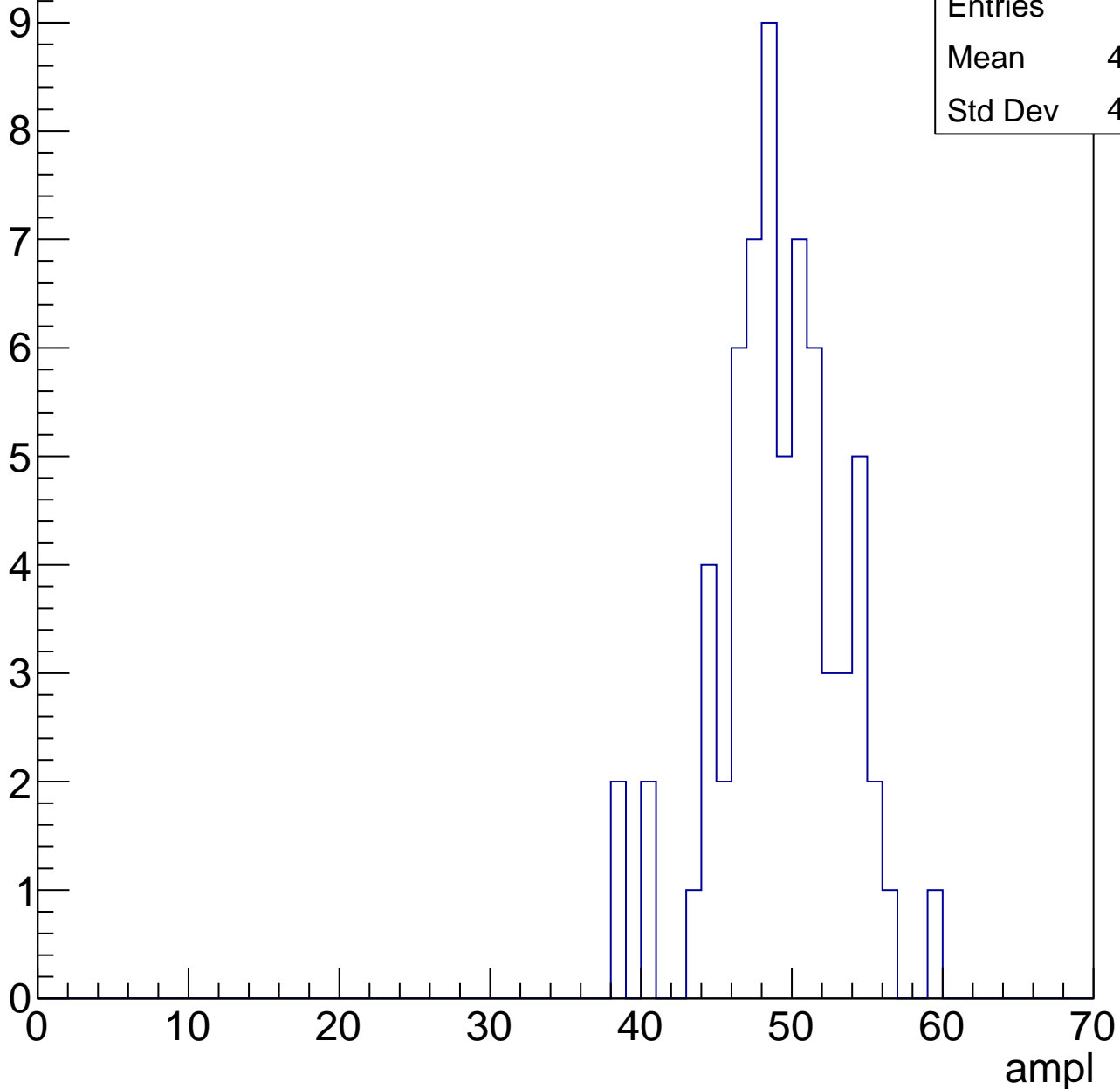


# B1L103S, U26-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	48.68
Std Dev	4.098

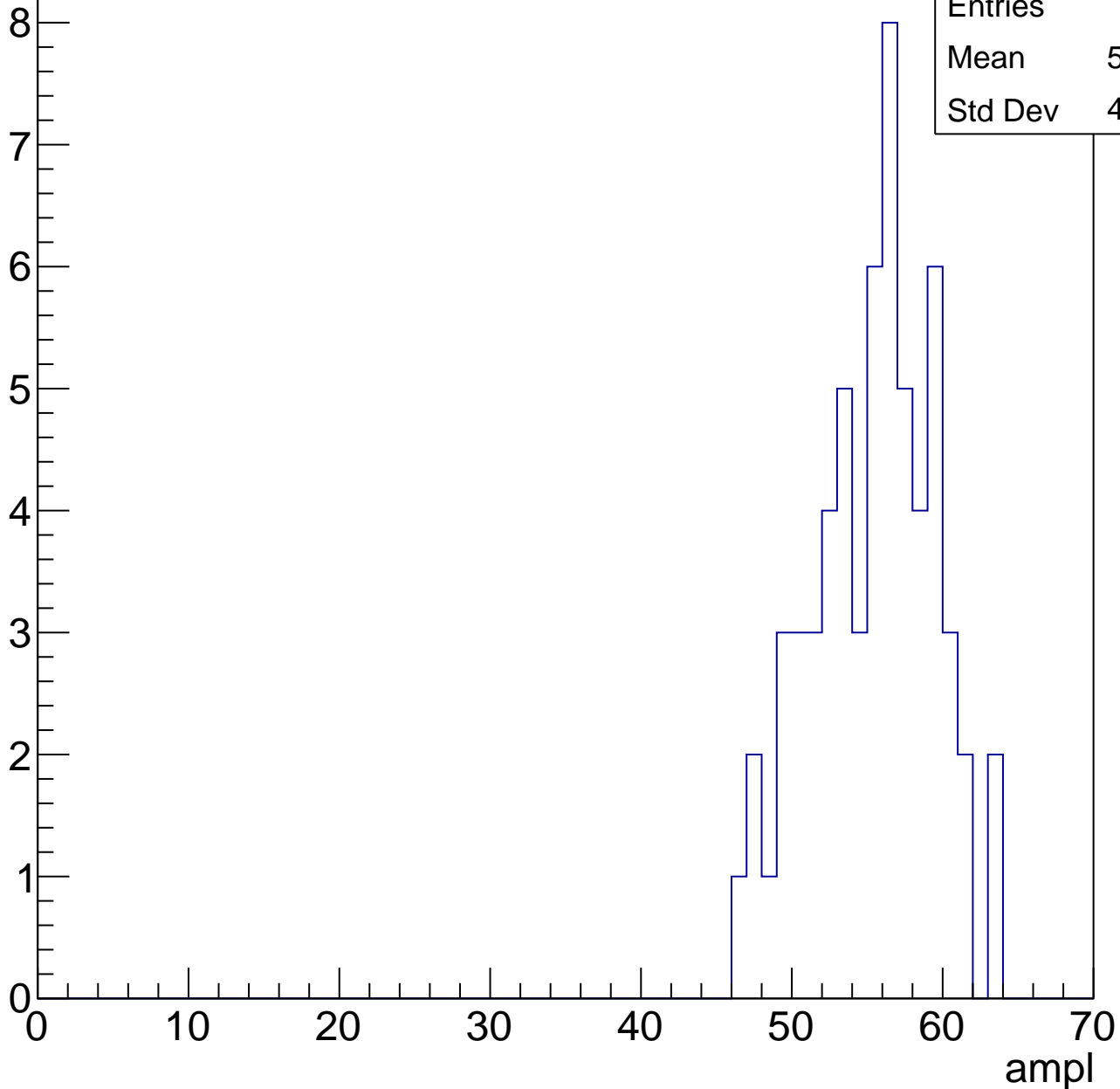


# B1L103S, U26-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	54.92
Std Dev	4.013

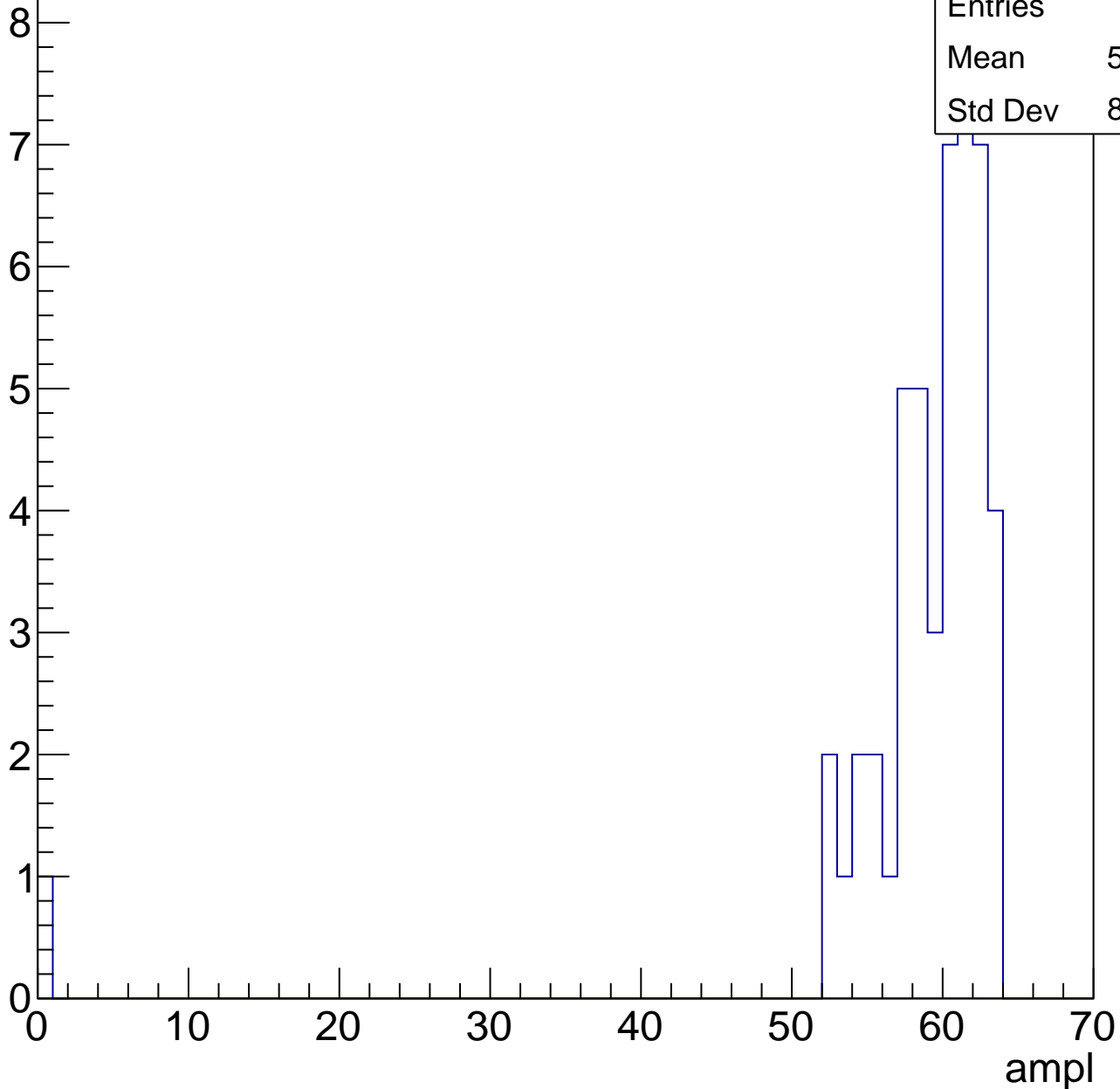


# B1L103S, U26-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

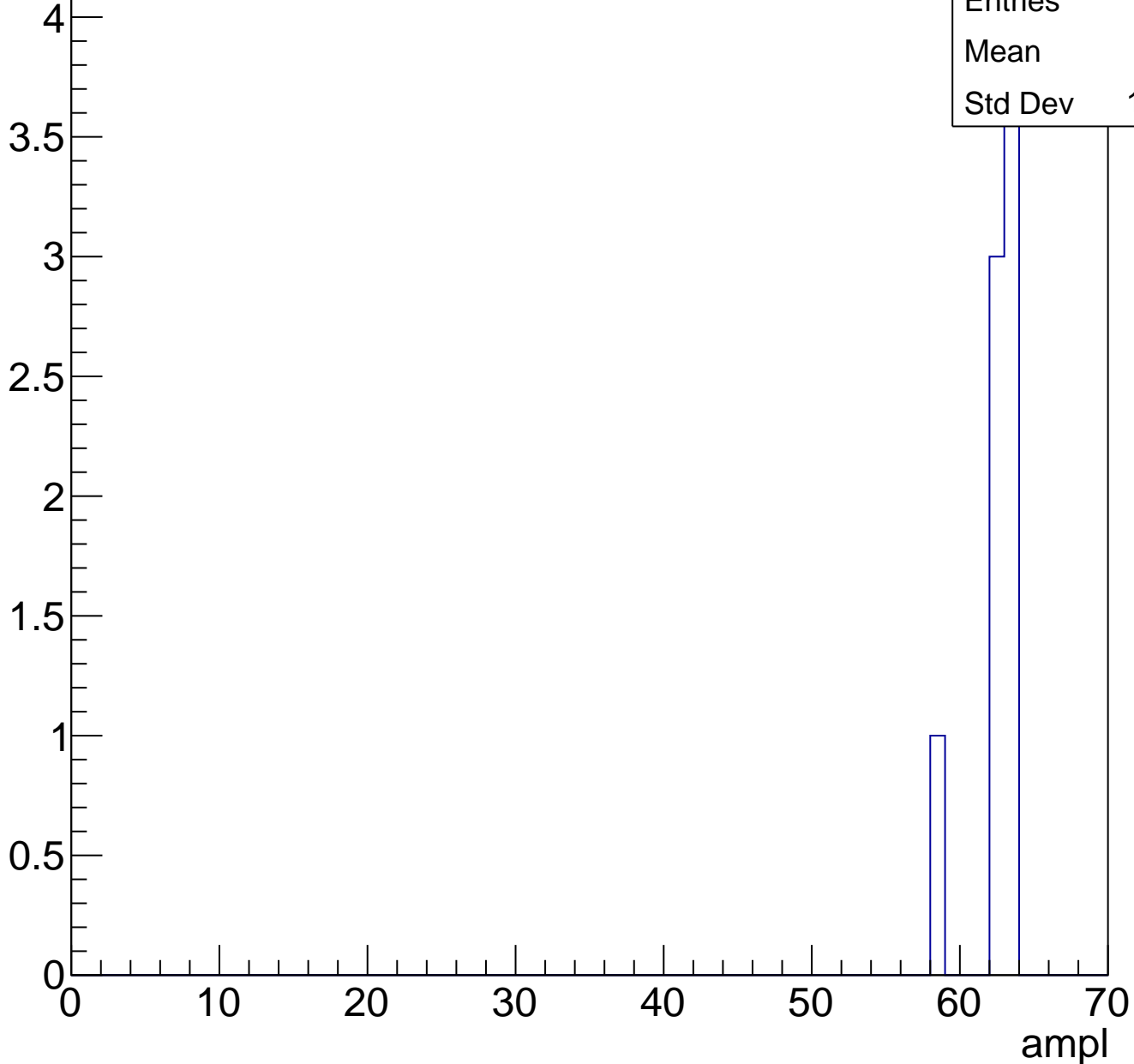
Entries	48
Mean	57.85
Std Dev	8.937



# B1L103S, U26-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch107, adc0

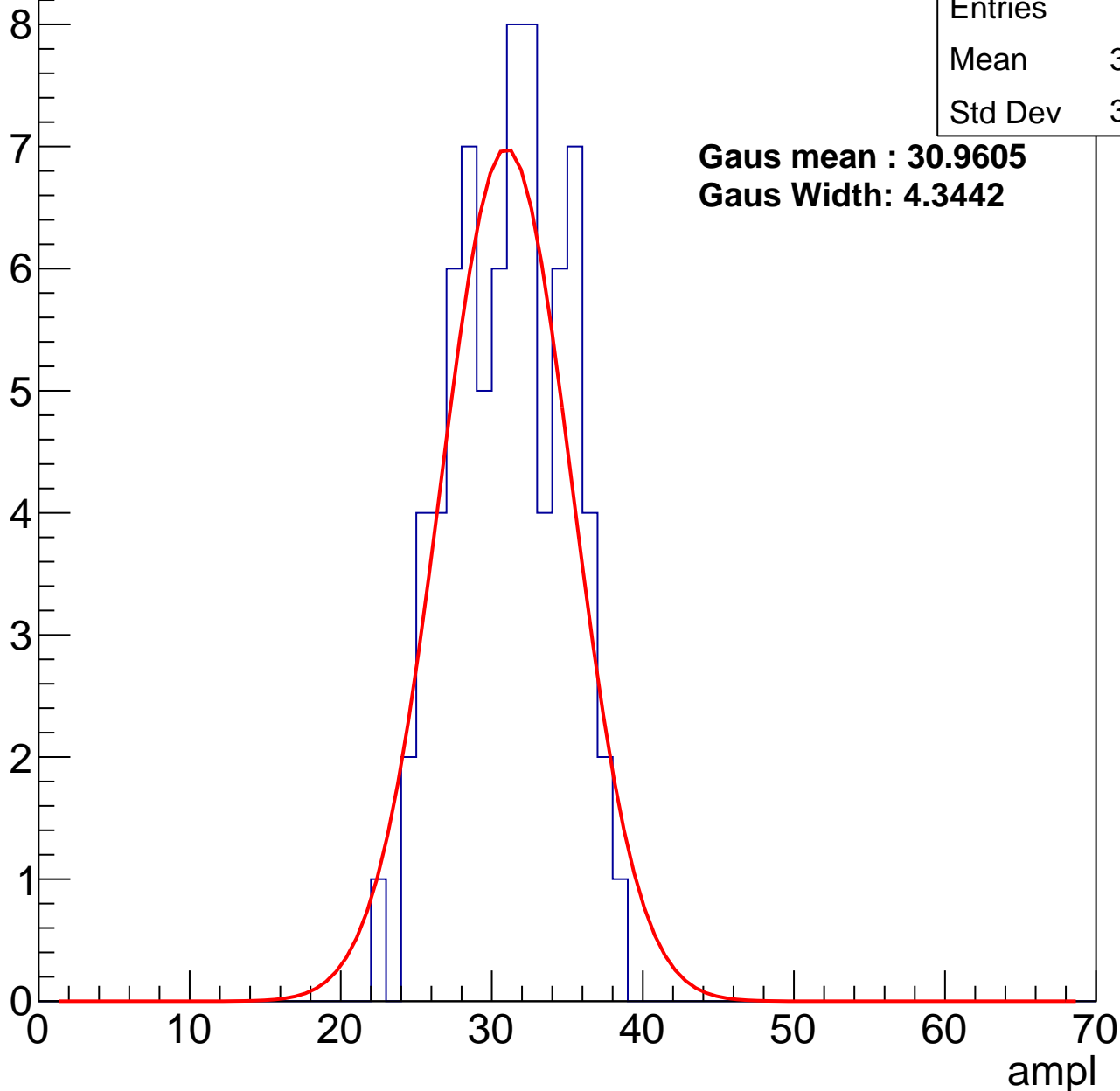
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	30.64
Std Dev	3.668

**Gaus mean : 30.9605**

**Gaus Width: 4.3442**



# B1L103S, U26-ch107, adc1

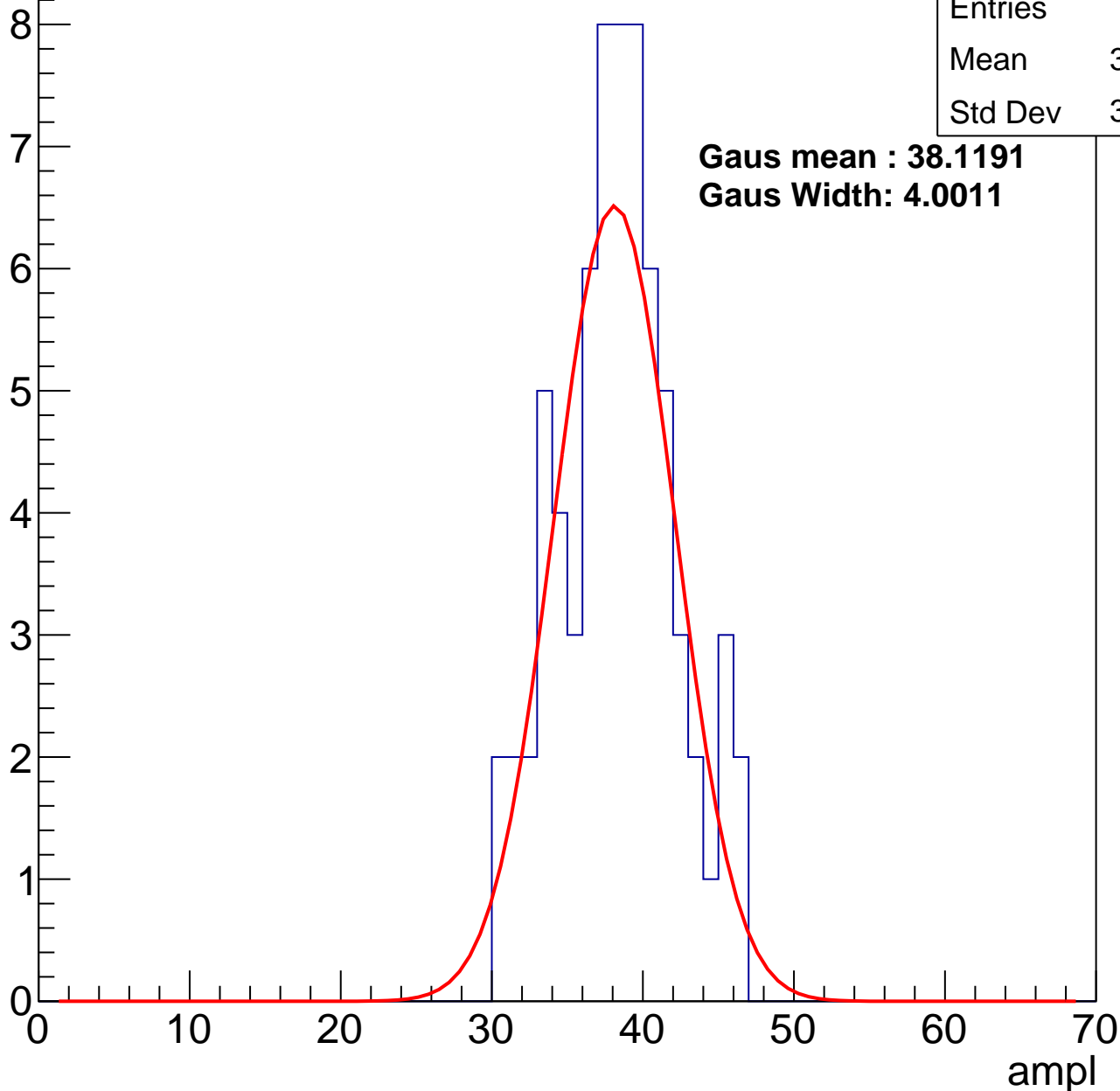
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	37.83
Std Dev	3.836

**Gaus mean : 38.1191**

**Gaus Width: 4.0011**



# B1L103S, U26-ch107, adc2

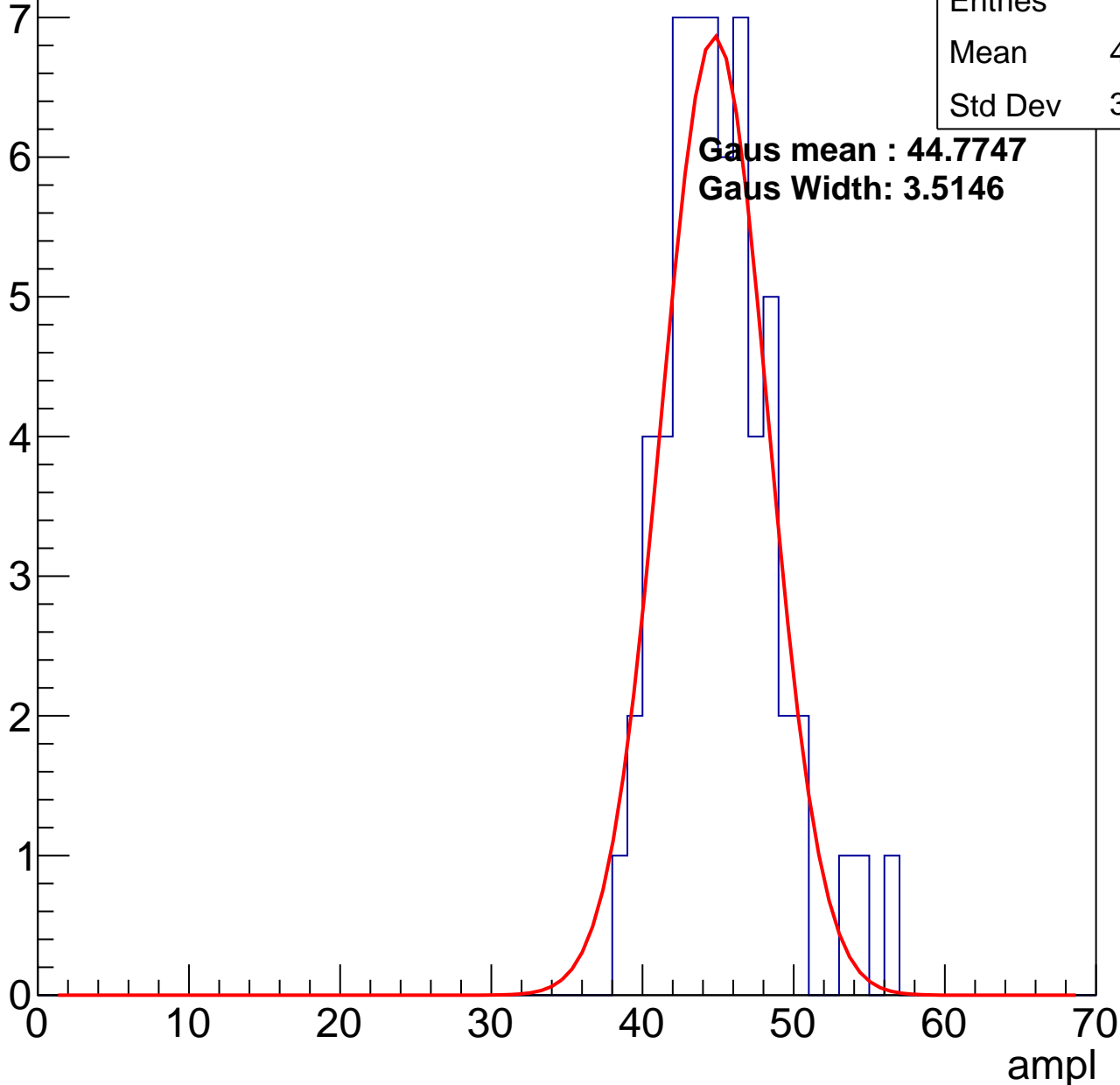
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	44.66
Std Dev	3.603

**Gaus mean : 44.7747**

**Gaus Width: 3.5146**

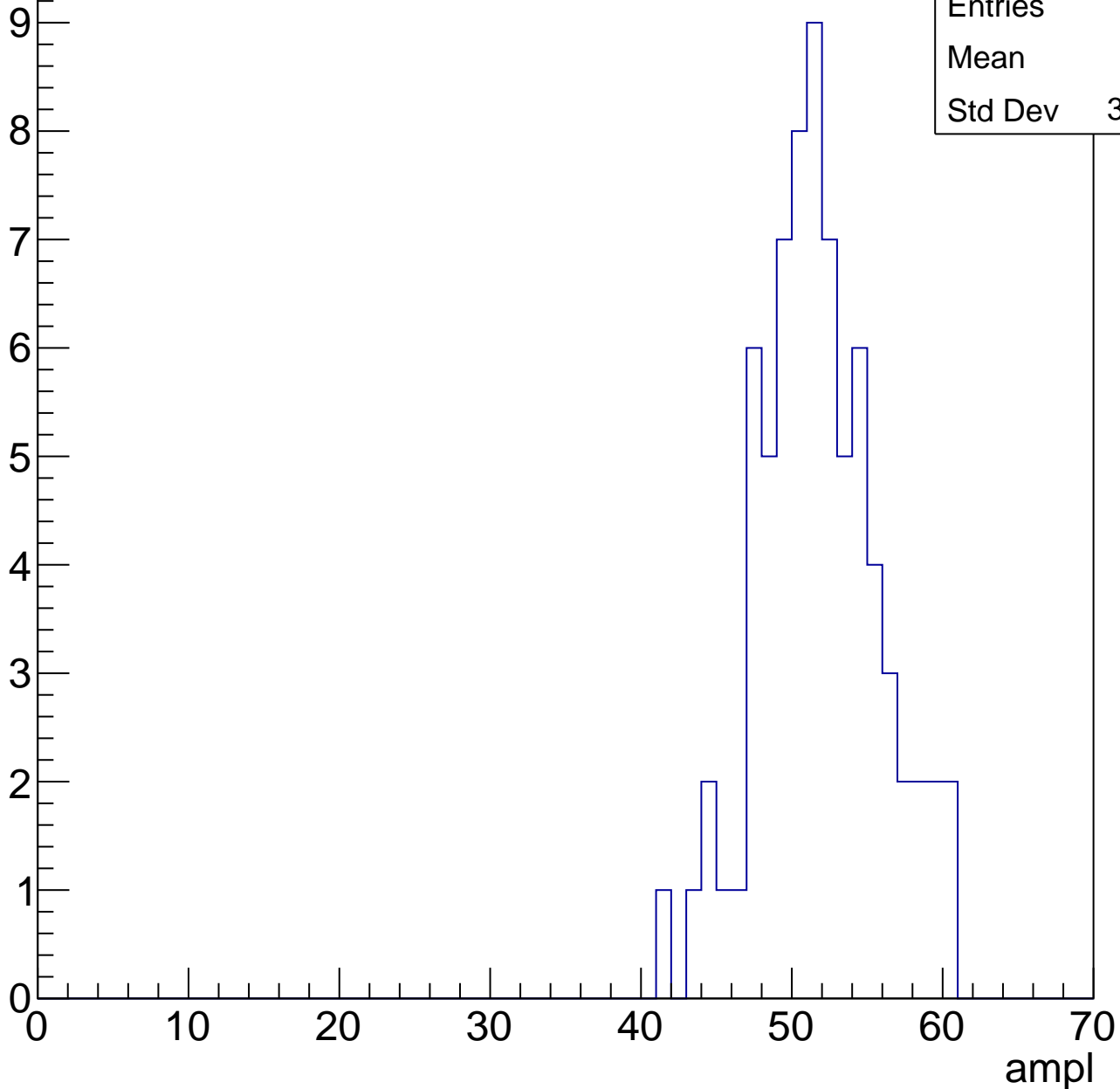


# B1L103S, U26-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	51.3
Std Dev	3.982

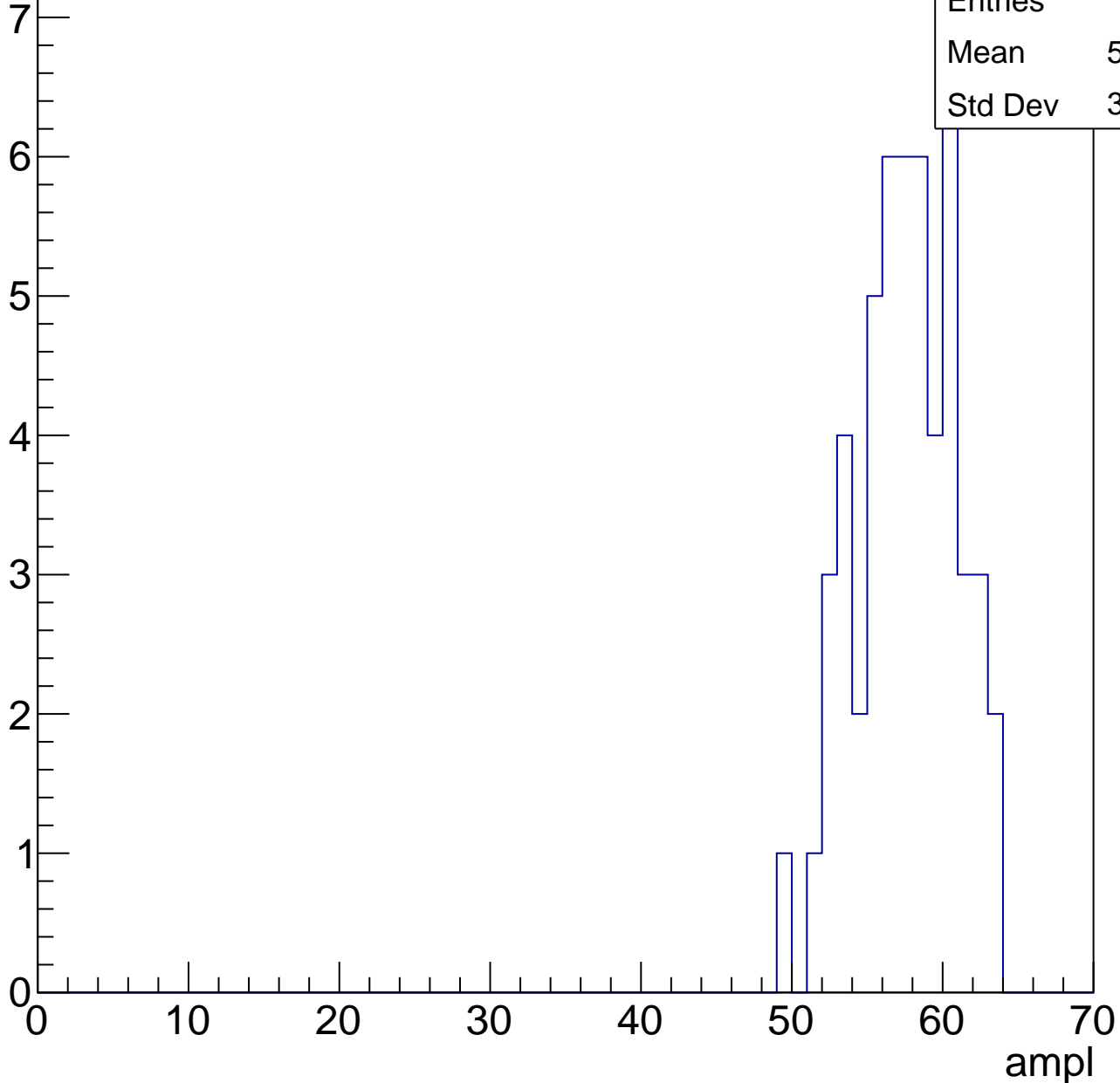


# B1L103S, U26-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	57.13
Std Dev	3.257

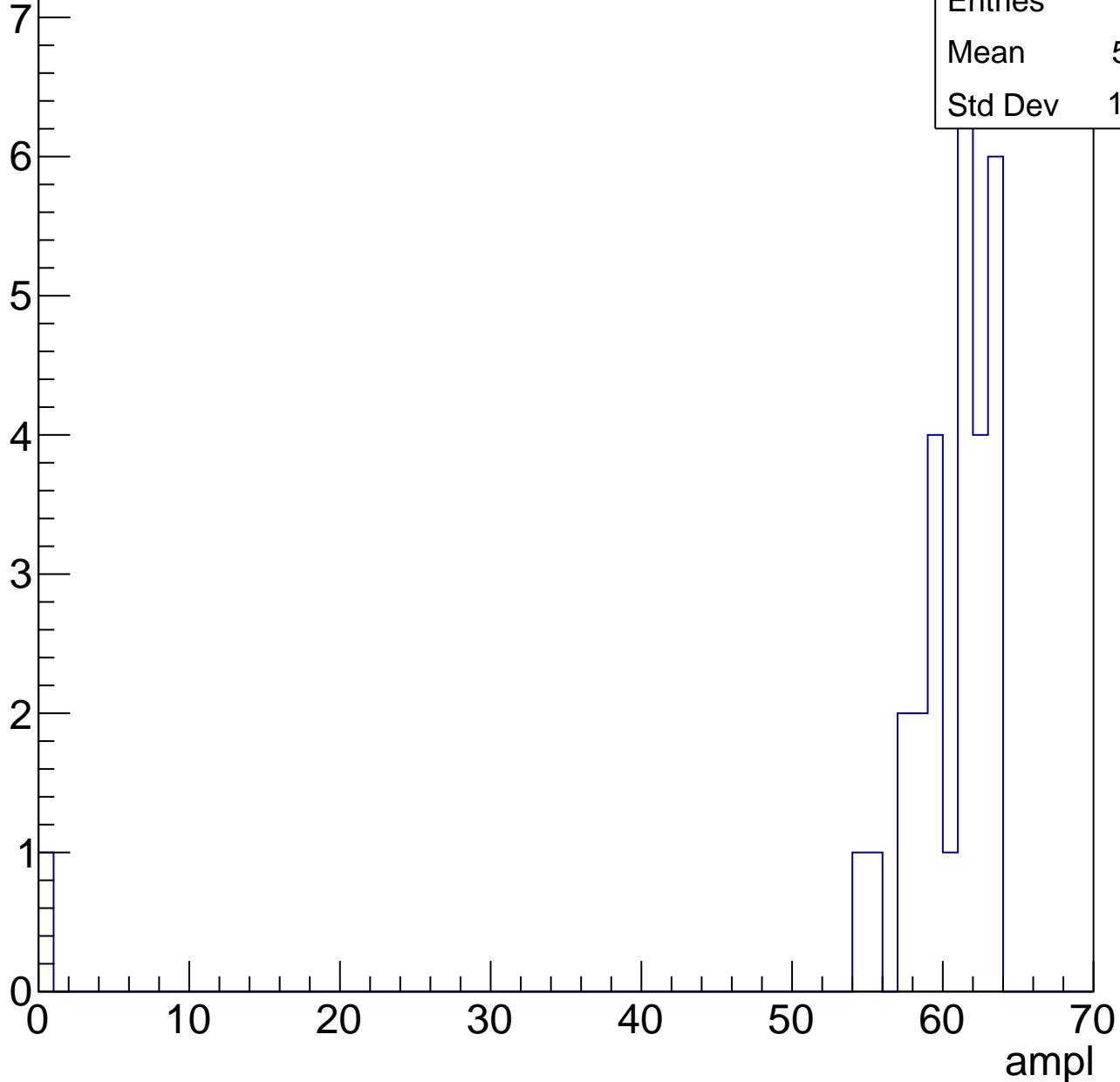


# B1L103S, U26-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	29
Mean	58.21
Std Dev	11.26



# B1L103S, U26-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	22
Std Dev	0

ampl

# B1L103S, U26-ch108, adc0

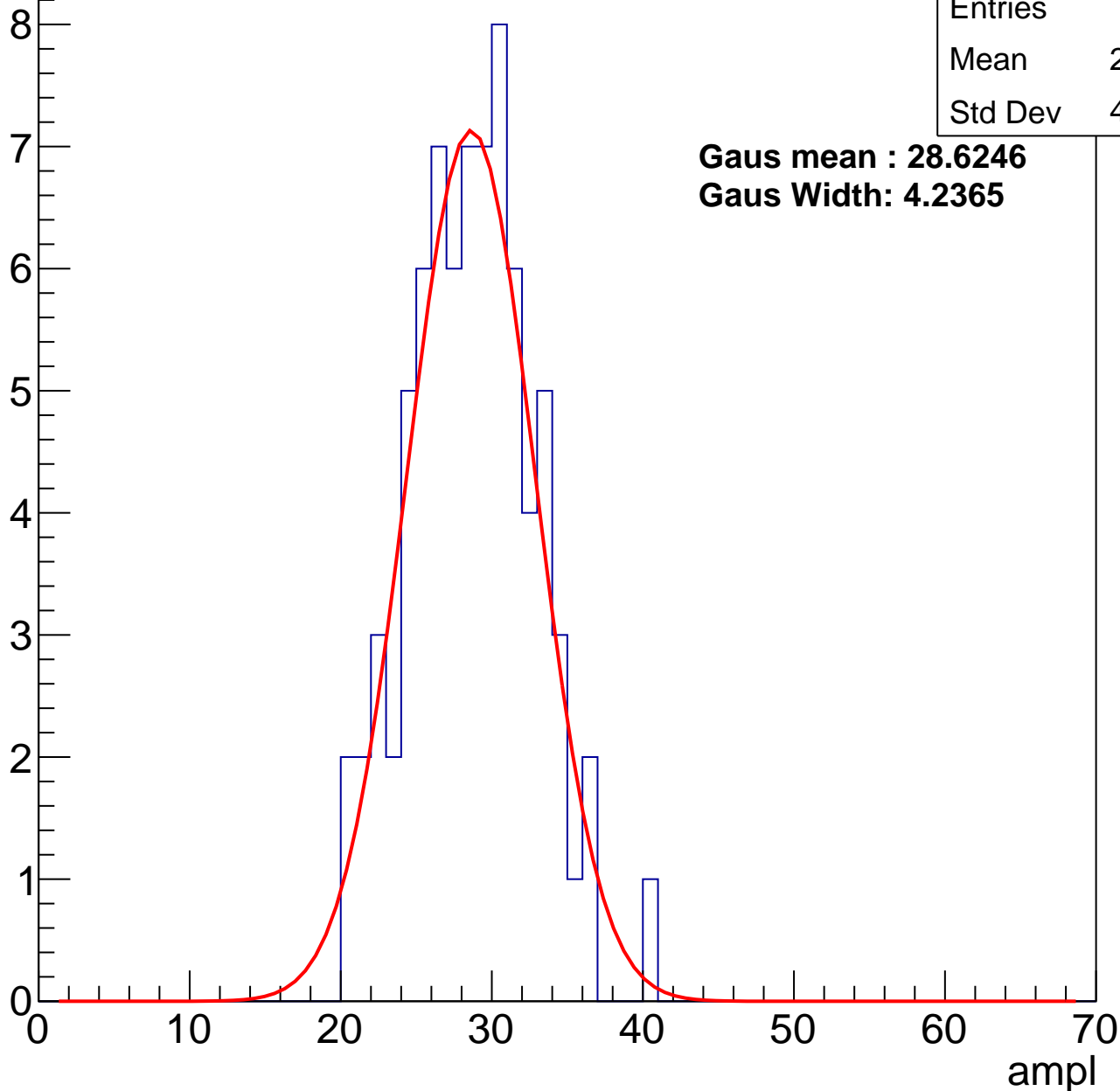
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	28.25
Std Dev	4.042

**Gaus mean : 28.6246**

**Gaus Width: 4.2365**



# B1L103S, U26-ch108, adc1

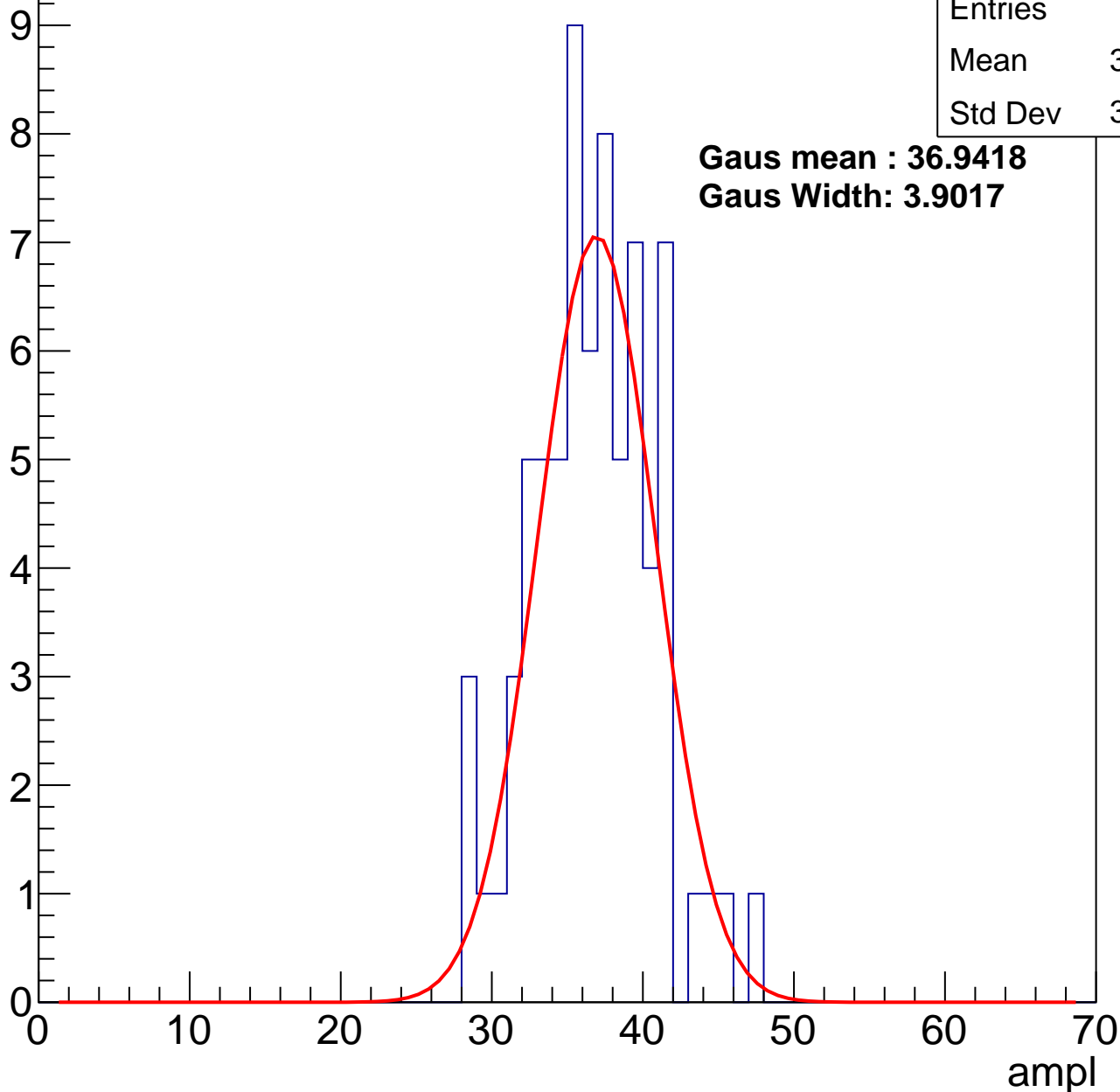
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	36.26
Std Dev	3.962

**Gaus mean : 36.9418**

**Gaus Width: 3.9017**



# B1L103S, U26-ch108, adc2

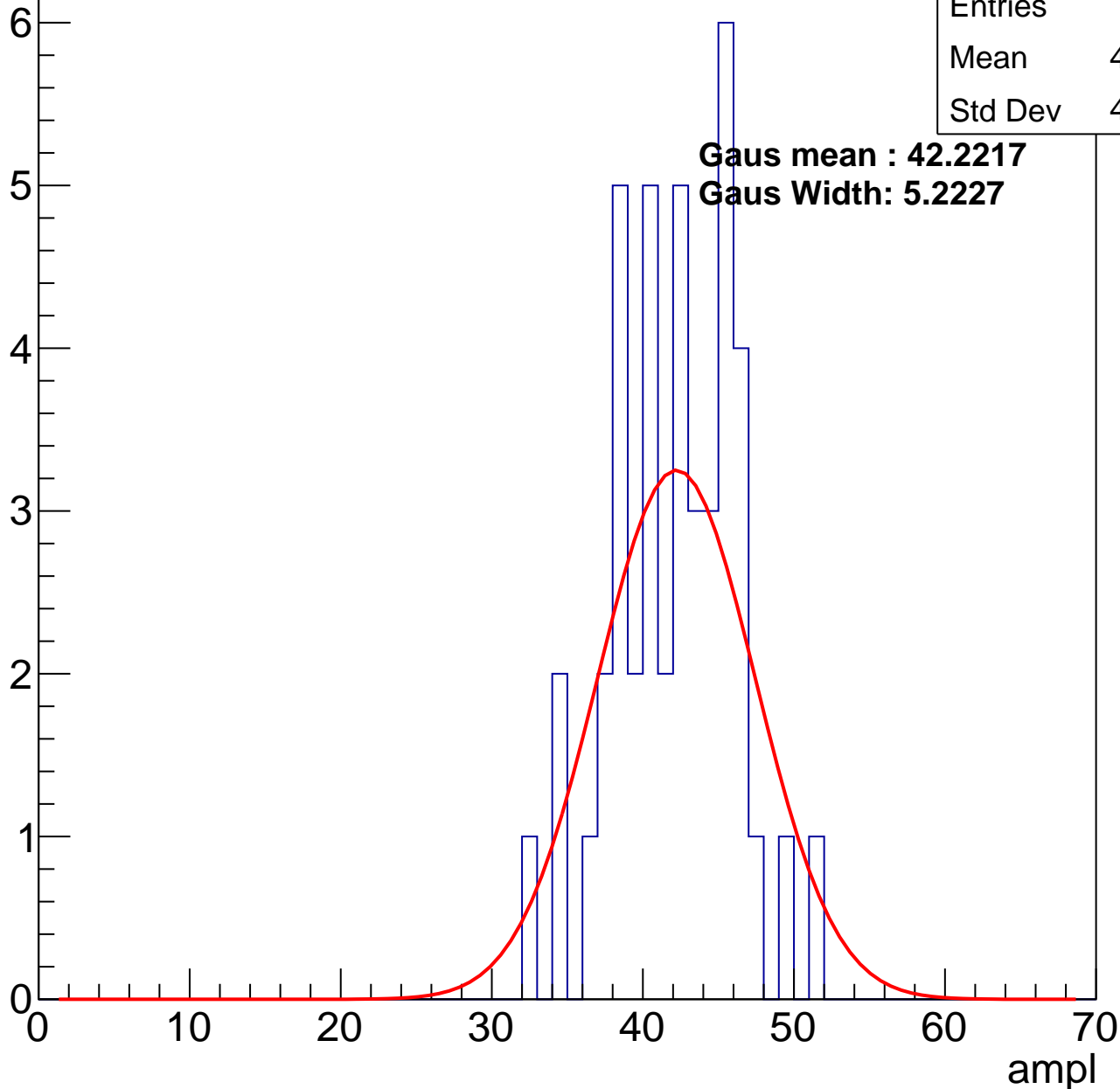
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	41.64
Std Dev	4.034

**Gaus mean : 42.2217**

**Gaus Width: 5.2227**

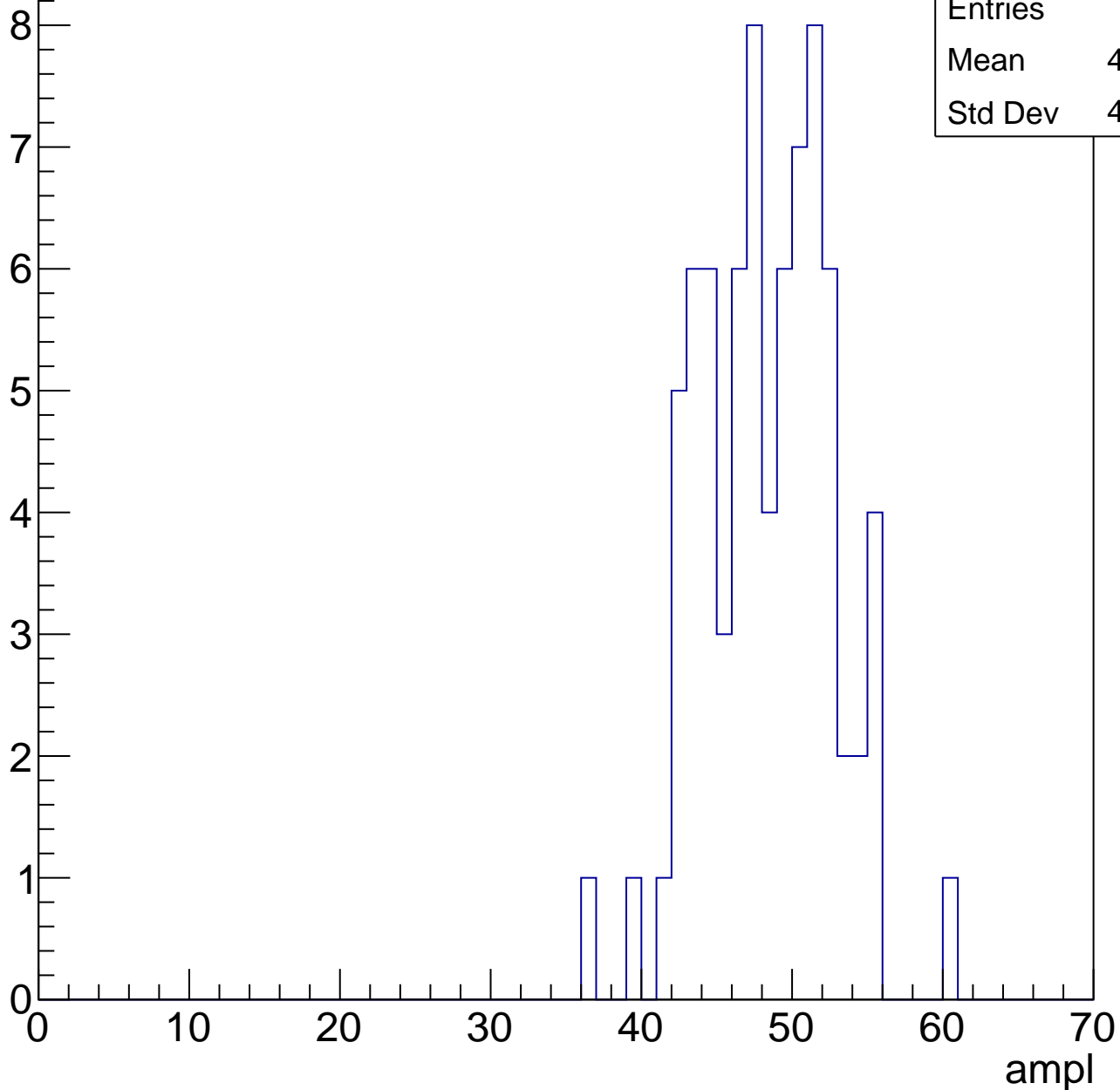


# B1L103S, U26-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	47.86
Std Dev	4.297

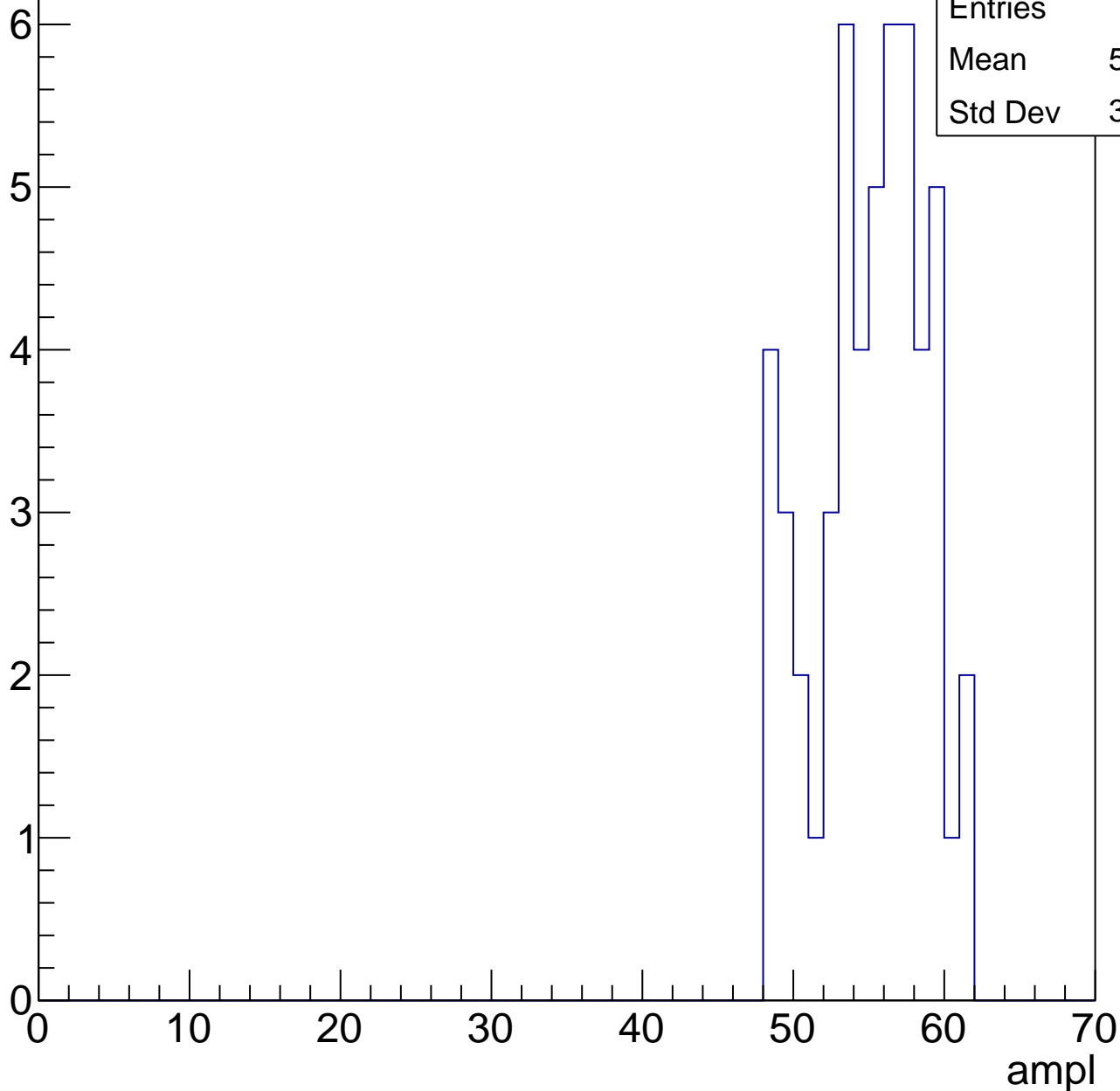


# B1L103S, U26-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	52
Mean	54.65
Std Dev	3.567

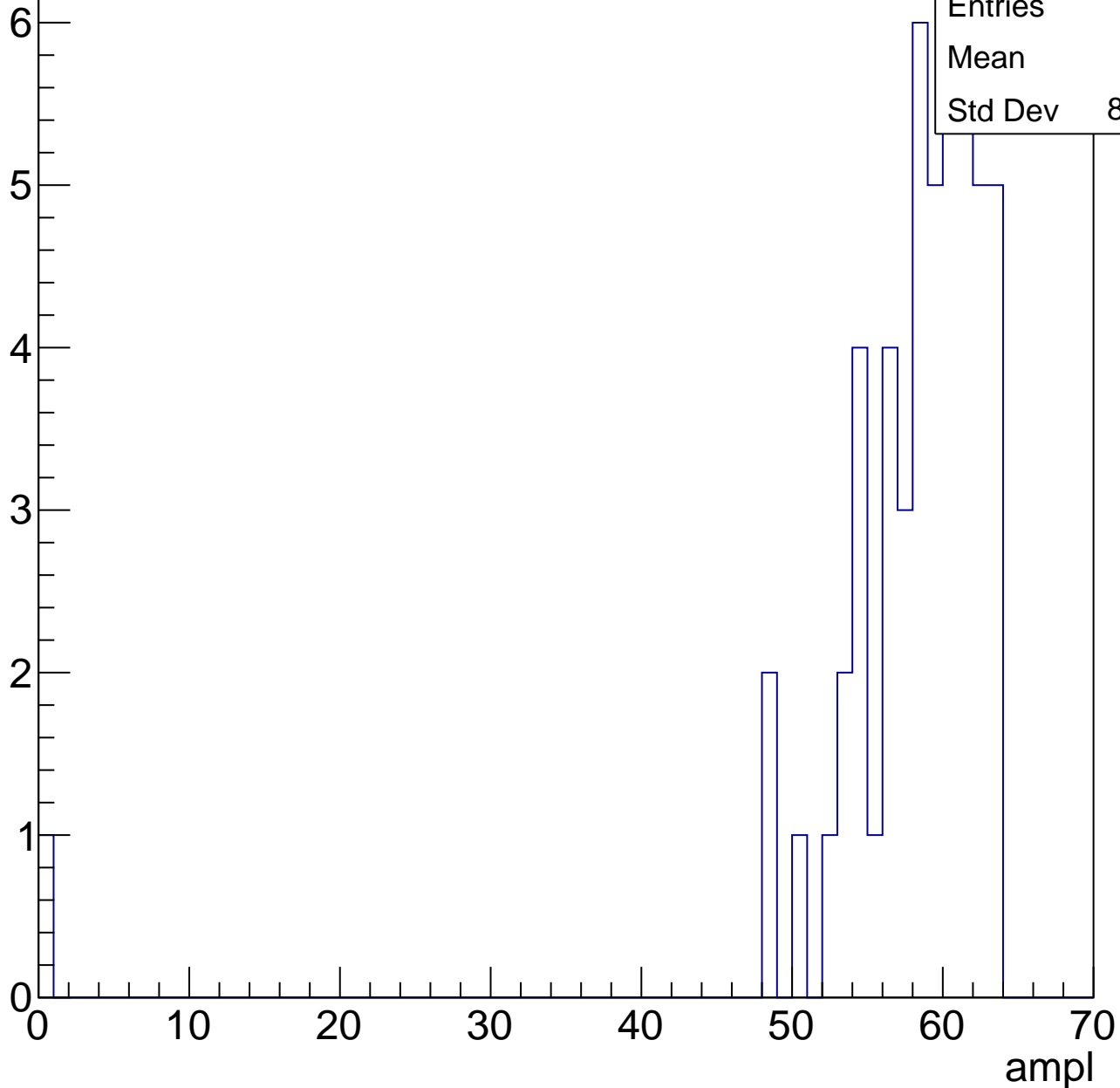


# B1L103S, U26-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

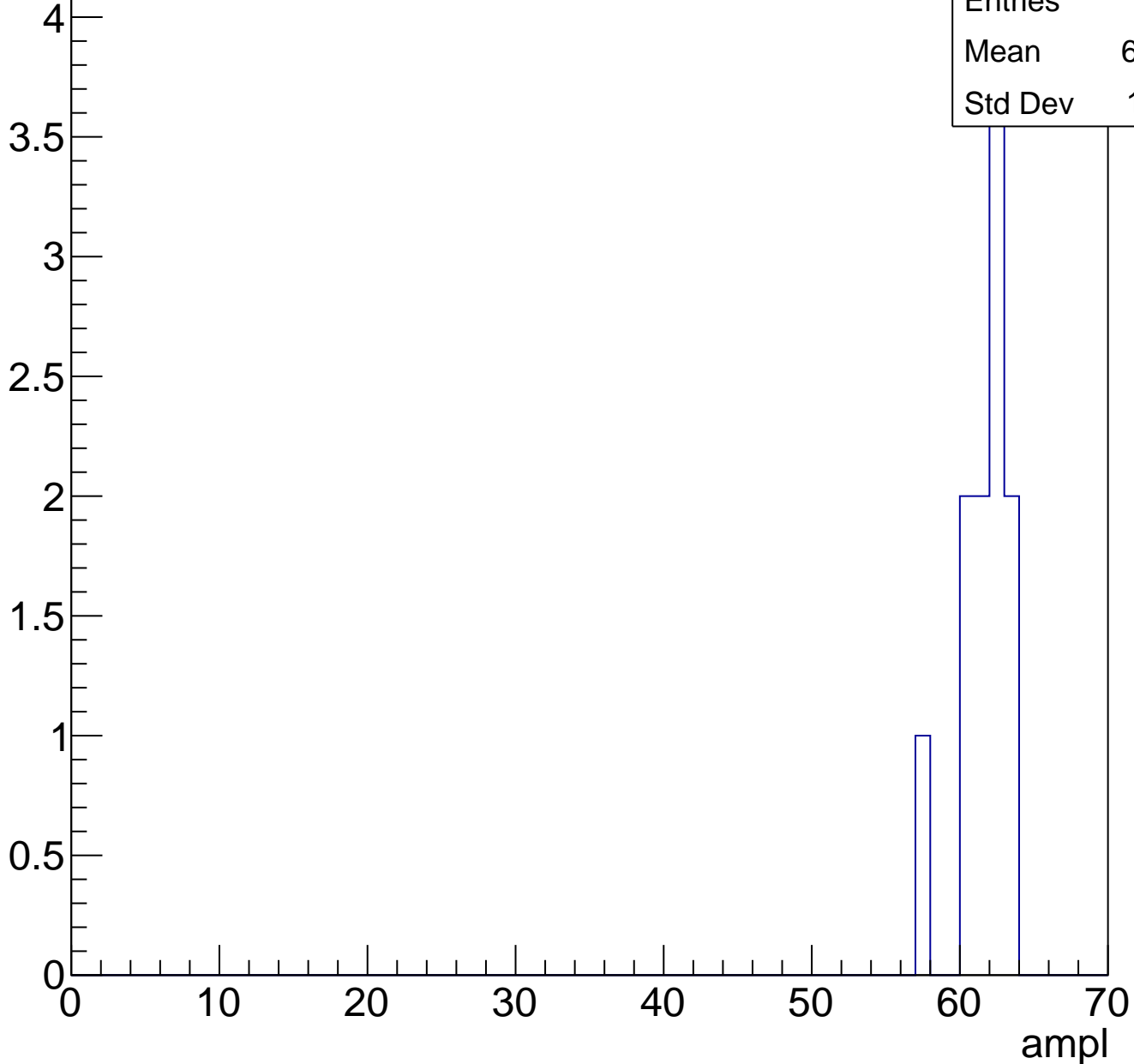
Entries	52
Mean	57
Std Dev	8.817



# B1L103S, U26-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



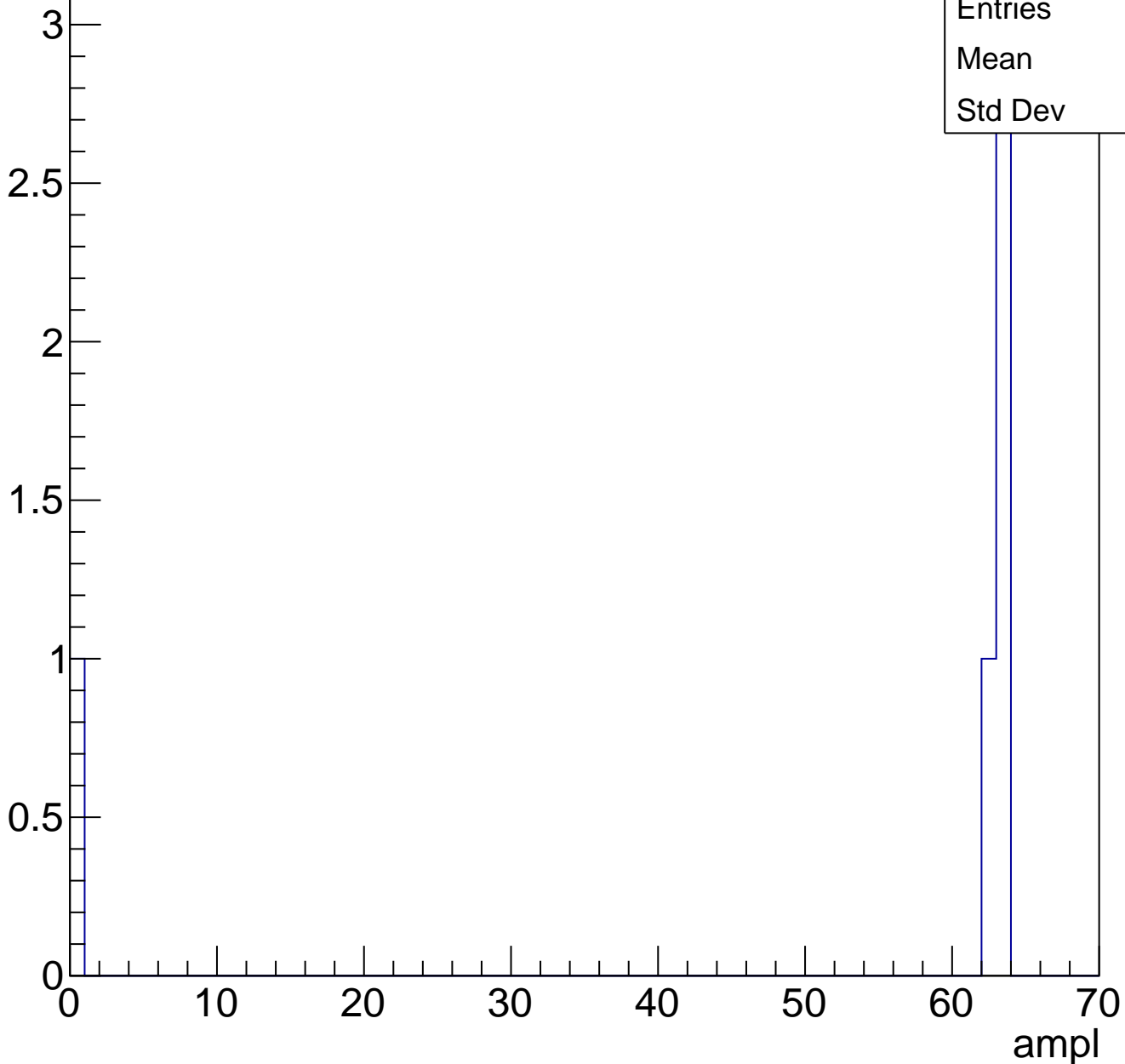
Entries	11
Mean	61.18
Std Dev	1.641



# B1L103S, U26-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch109, adc0

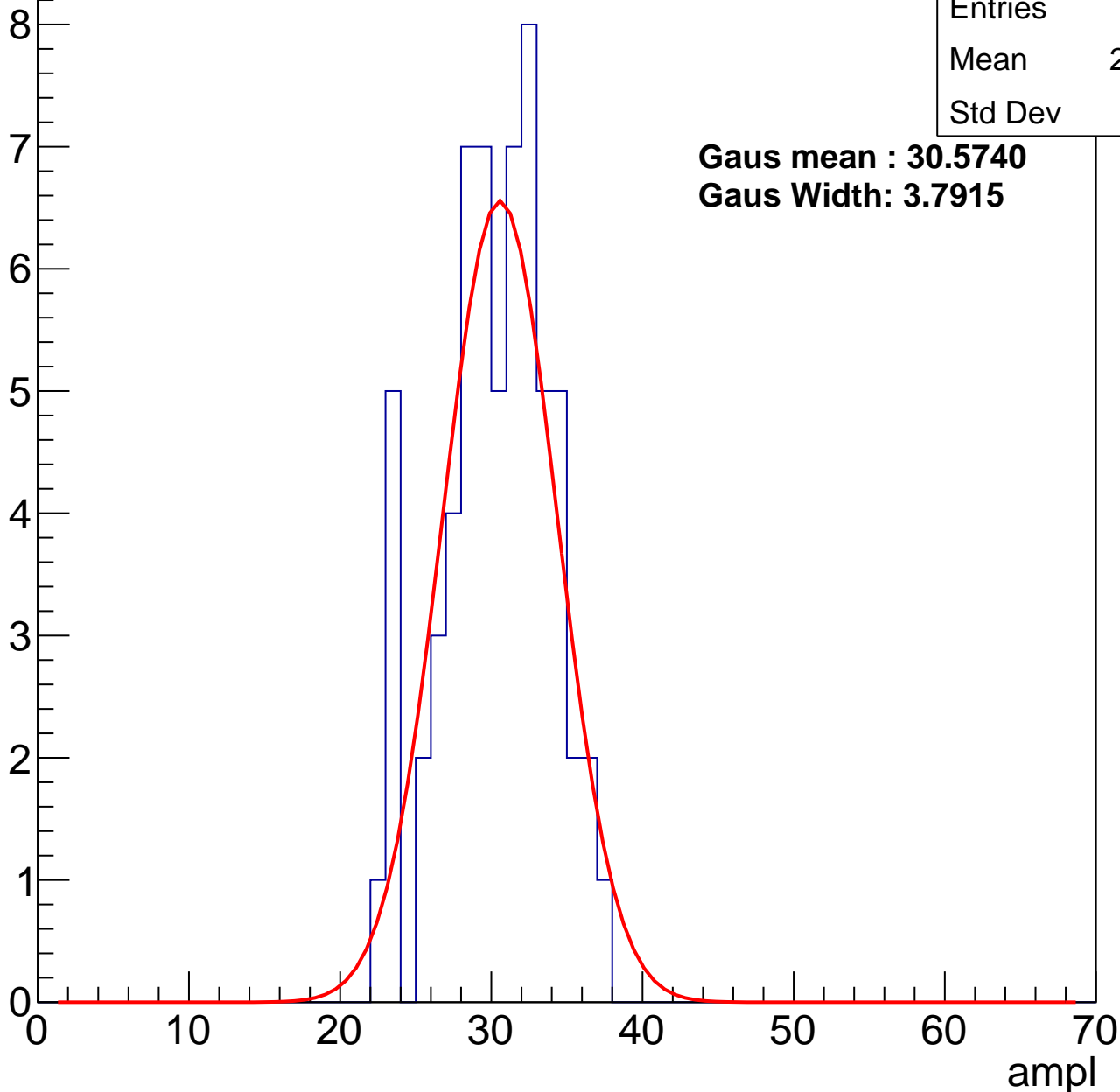
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	29.83
Std Dev	3.56

**Gaus mean : 30.5740**

**Gaus Width: 3.7915**



# B1L103S, U26-ch109, adc1

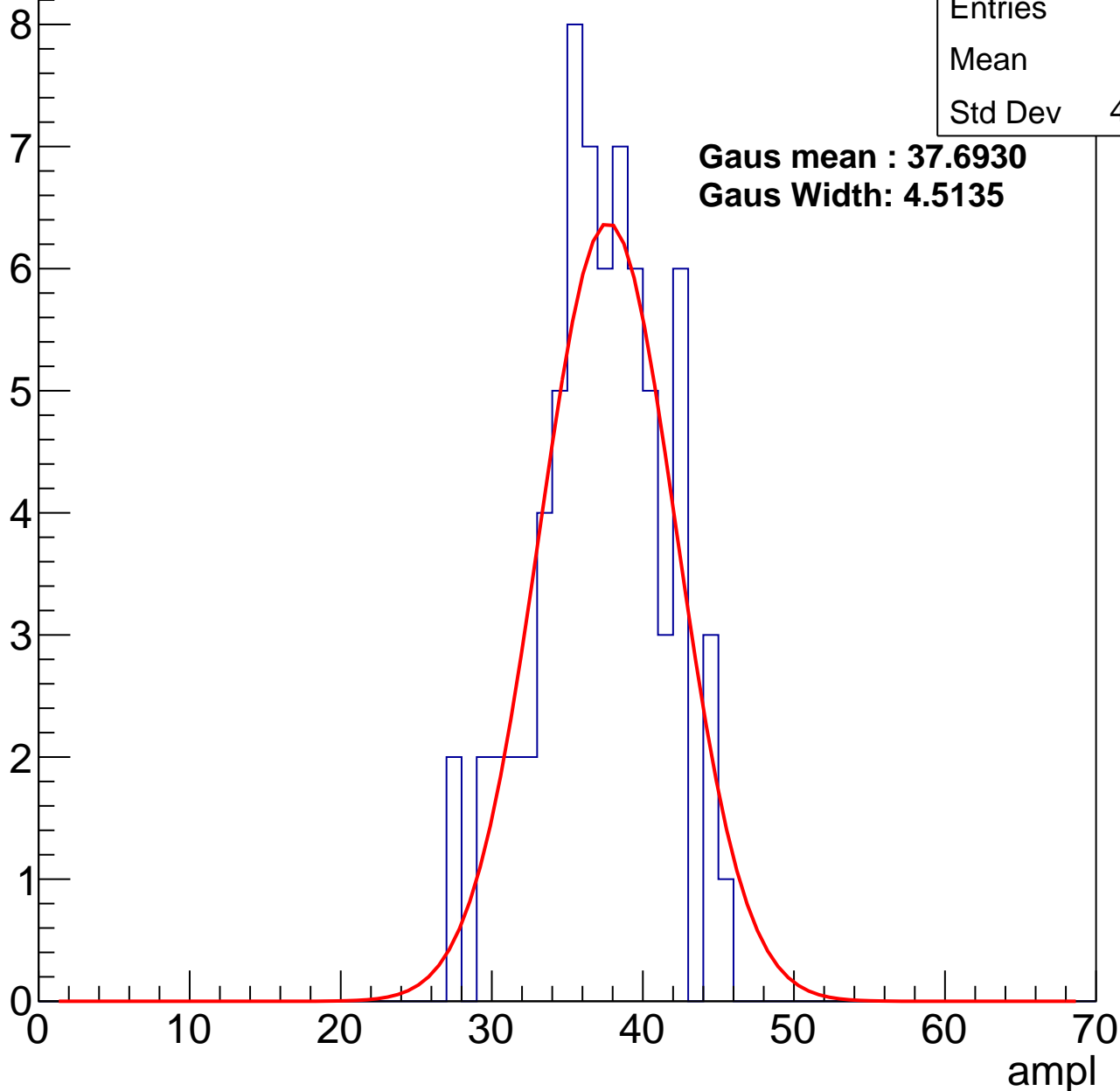
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	36.7
Std Dev	4.068

**Gaus mean : 37.6930**

**Gaus Width: 4.5135**



# B1L103S, U26-ch109, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	78
Mean	43.87
Std Dev	3.814

**Gaus mean : 44.3971**

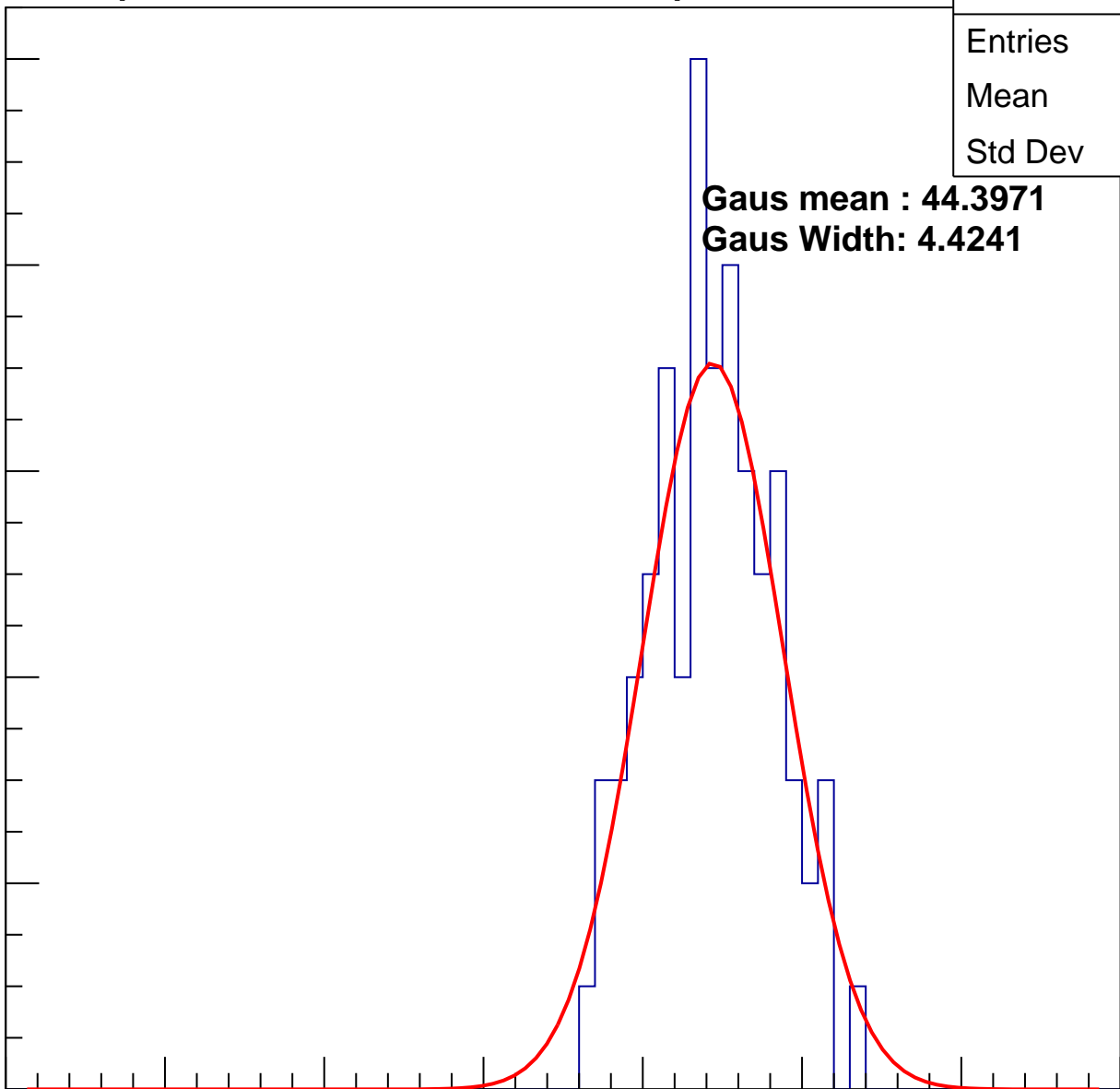
**Gaus Width: 4.4241**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

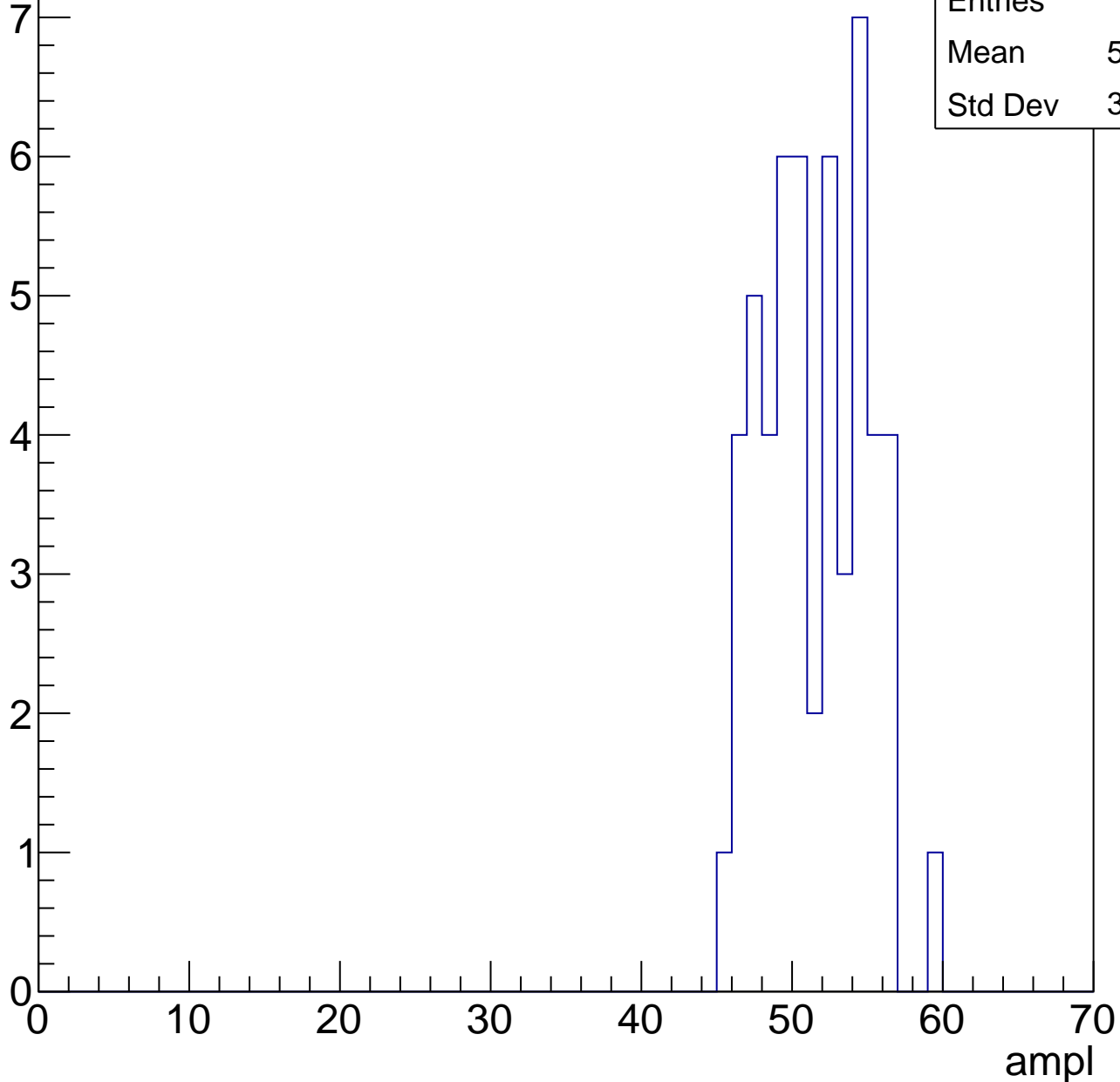


# B1L103S, U26-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	51.02
Std Dev	3.339

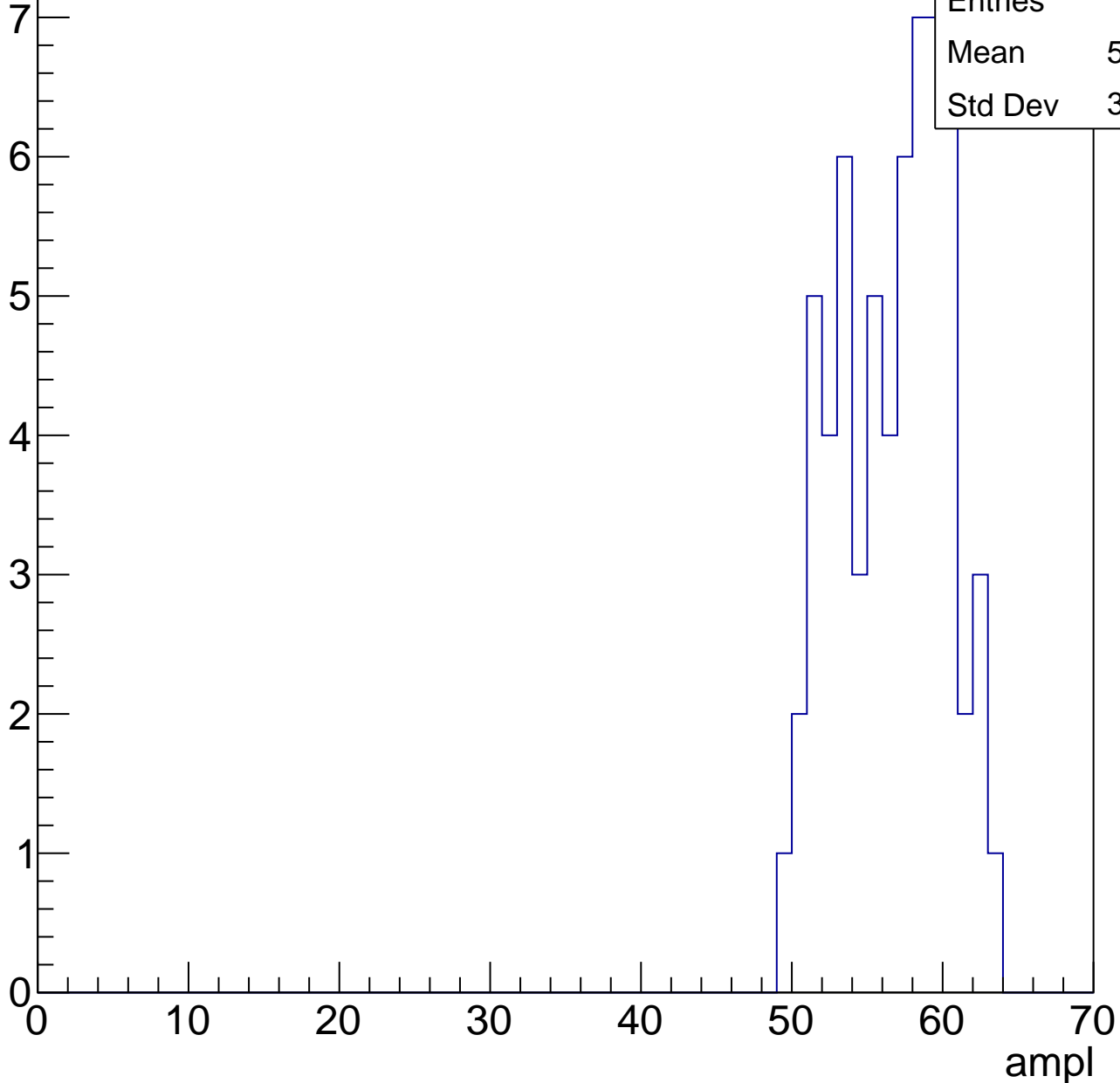


# B1L103S, U26-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	56.24
Std Dev	3.549

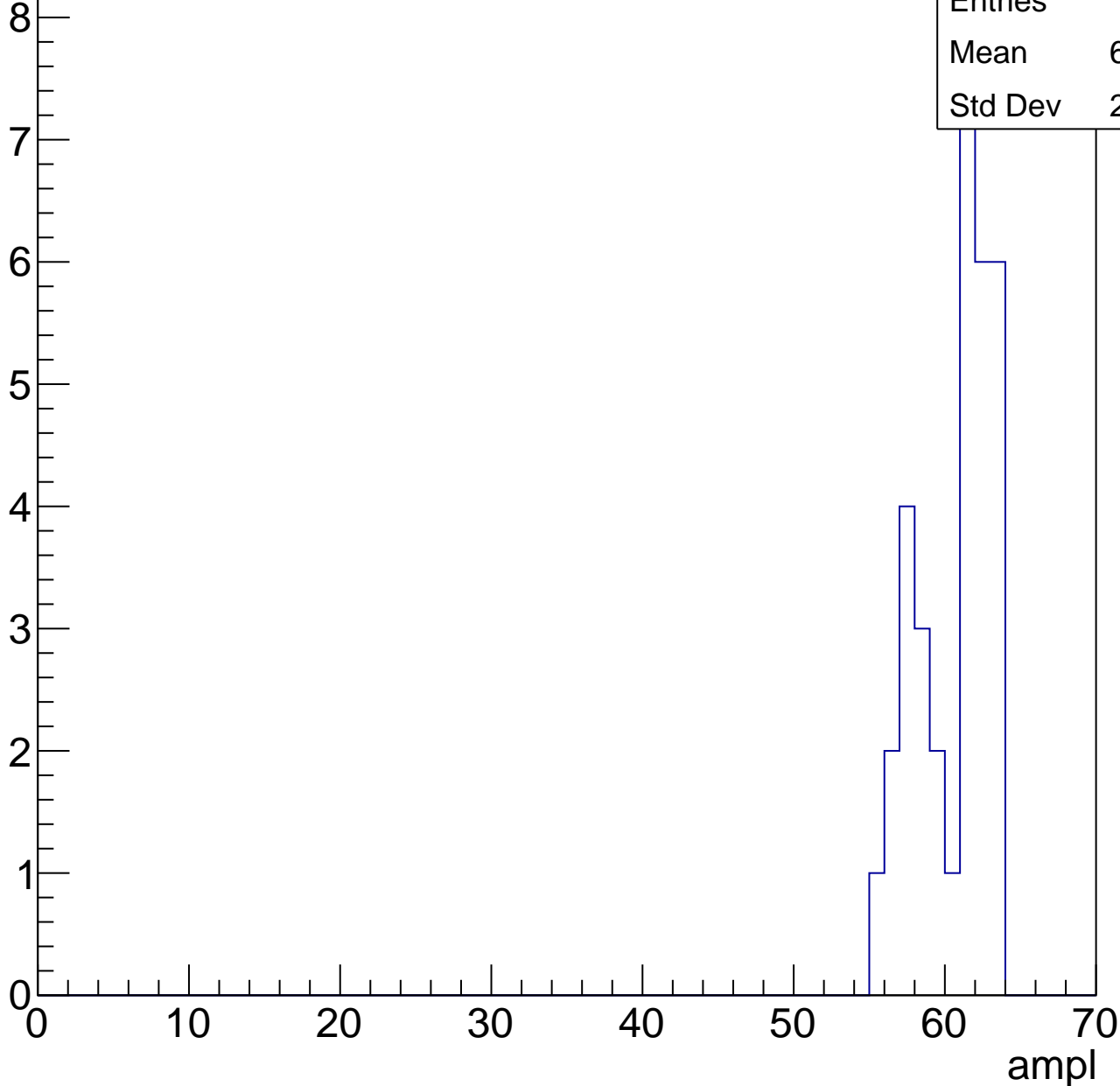


# B1L103S, U26-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

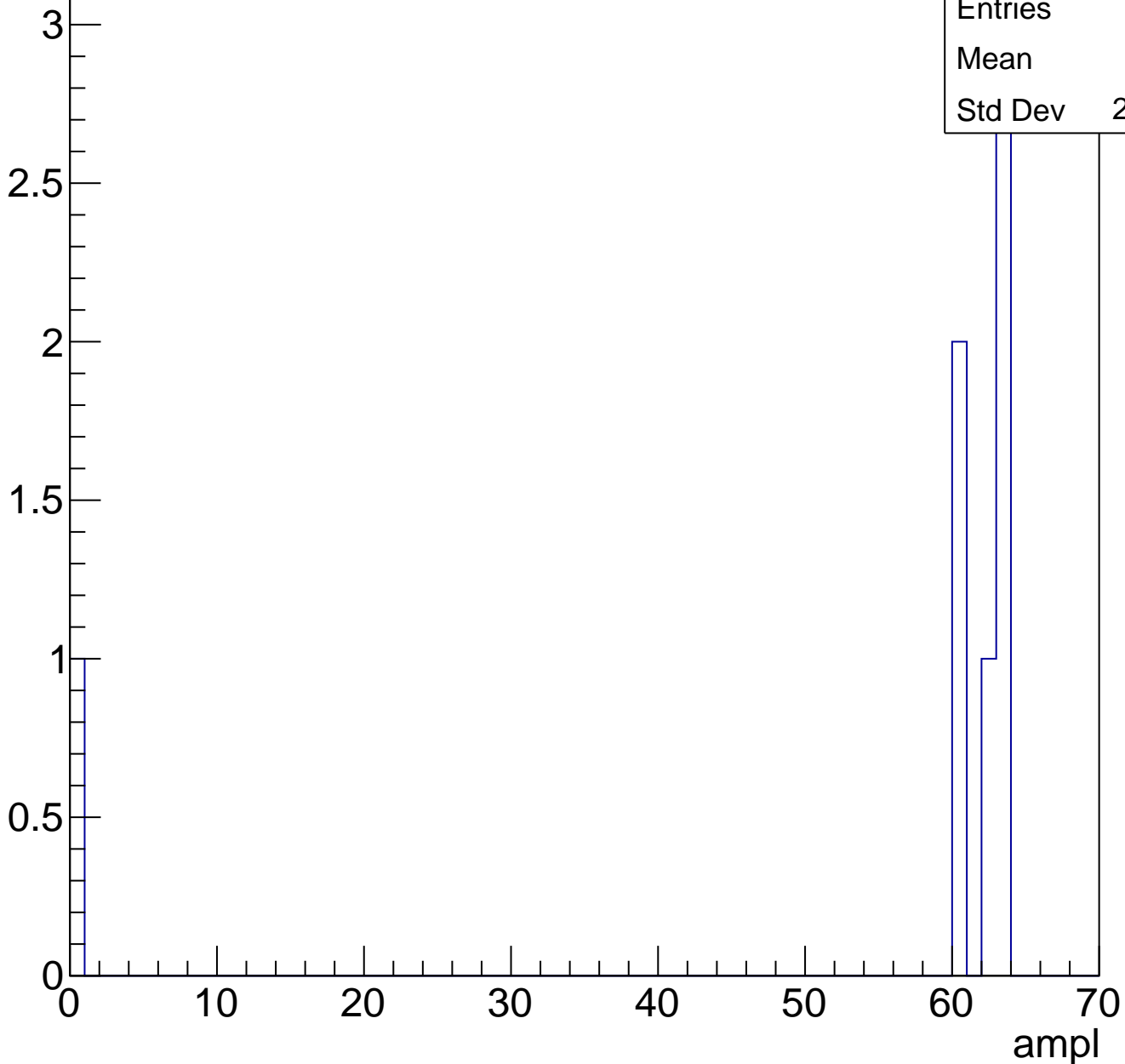
Entries	33
Mean	60.15
Std Dev	2.414



# B1L103S, U26-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

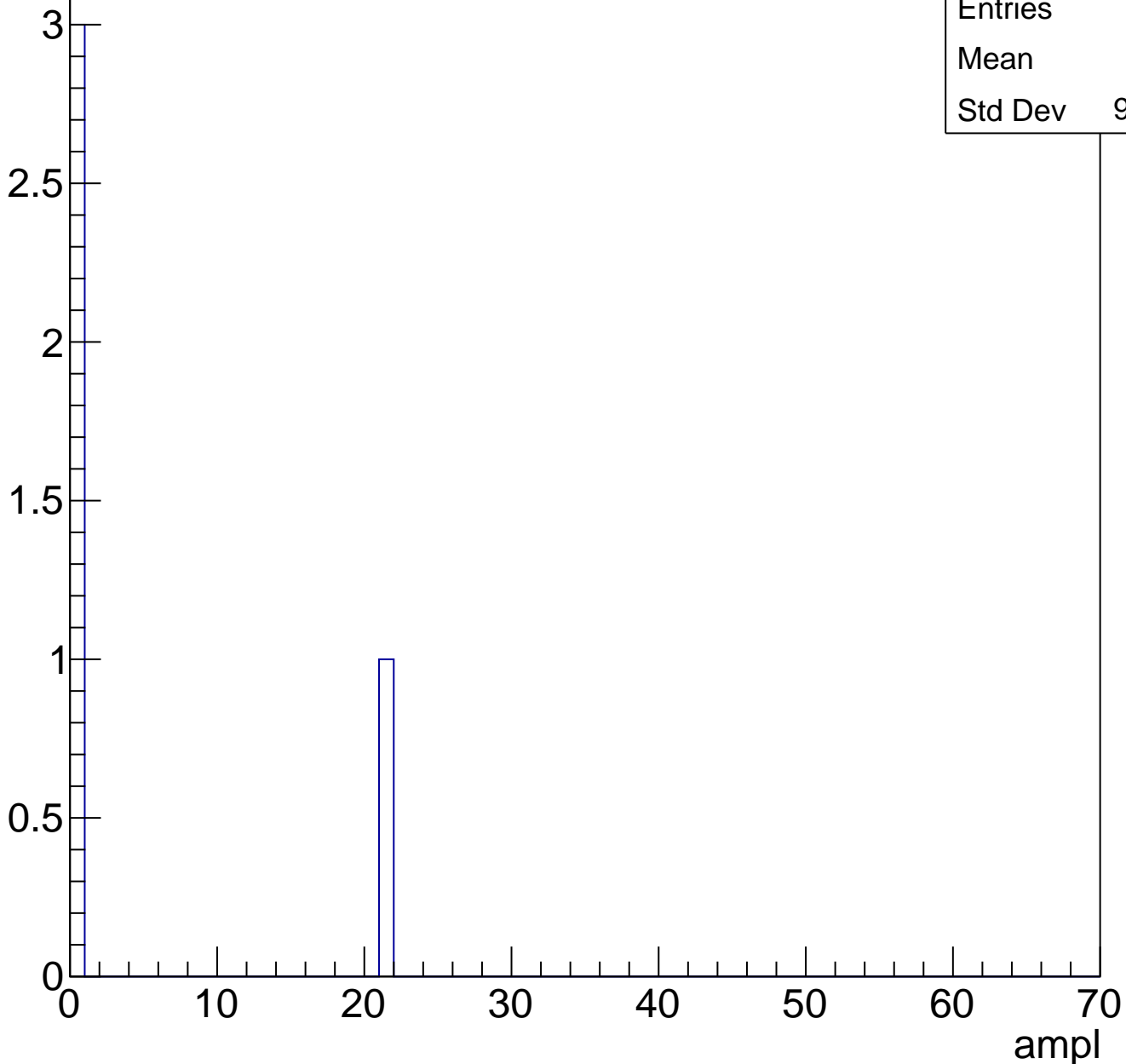




# B1L103S, U26-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch110, adc0

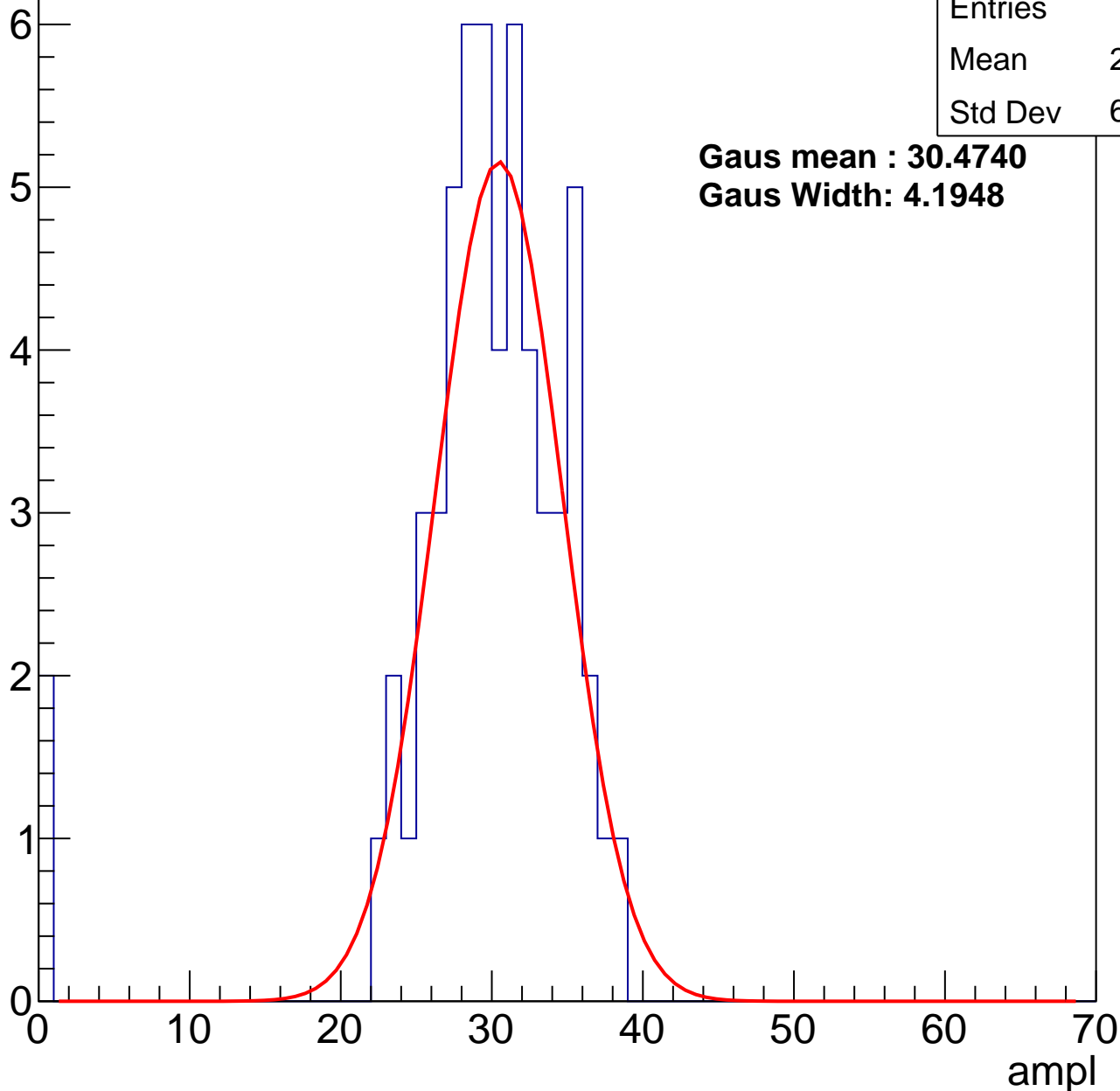
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	28.95
Std Dev	6.616

**Gaus mean : 30.4740**

**Gaus Width: 4.1948**



# B1L103S, U26-ch110, adc1

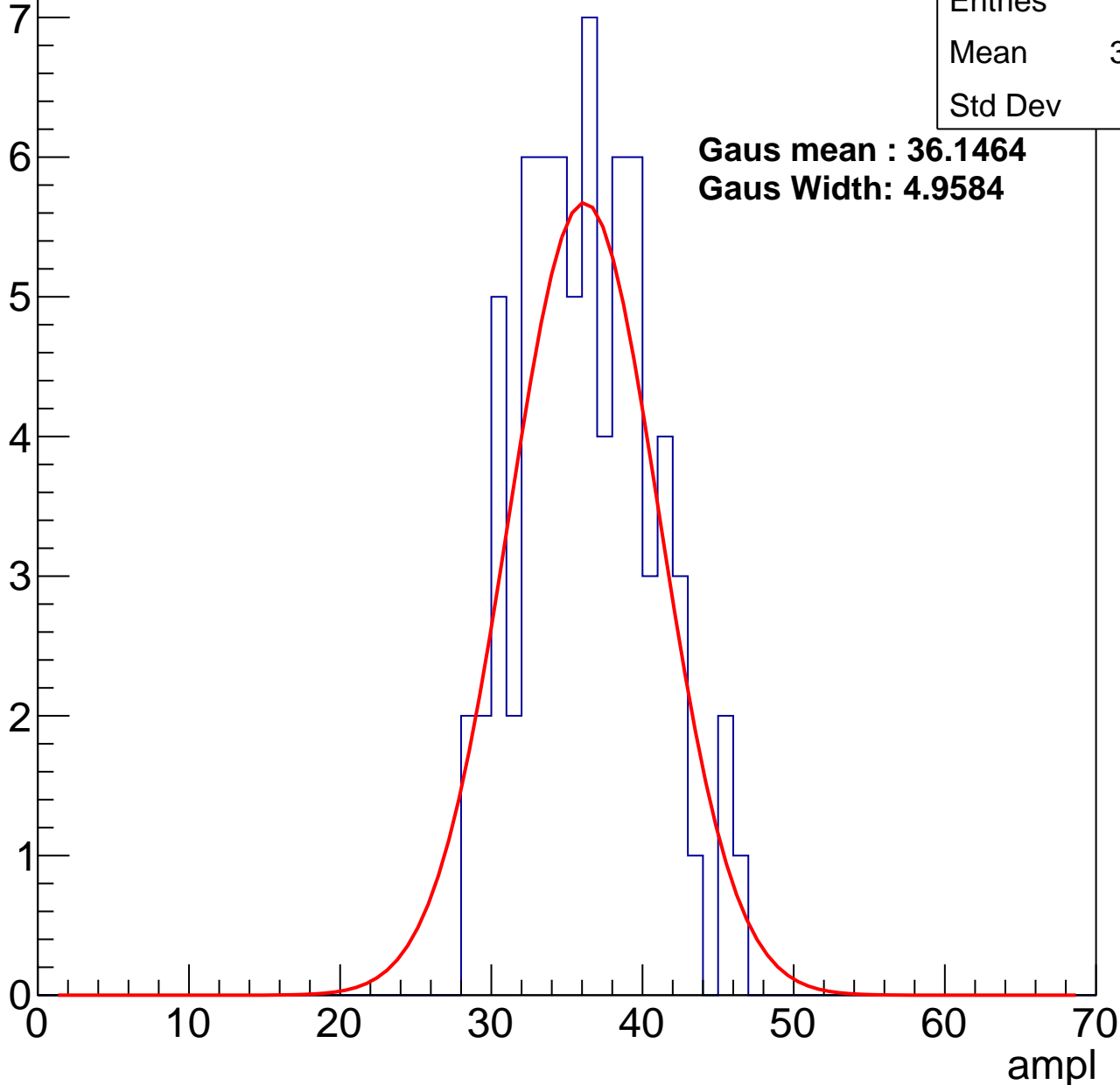
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	35.86
Std Dev	4.25

**Gaus mean : 36.1464**

**Gaus Width: 4.9584**



# B1L103S, U26-ch110, adc2

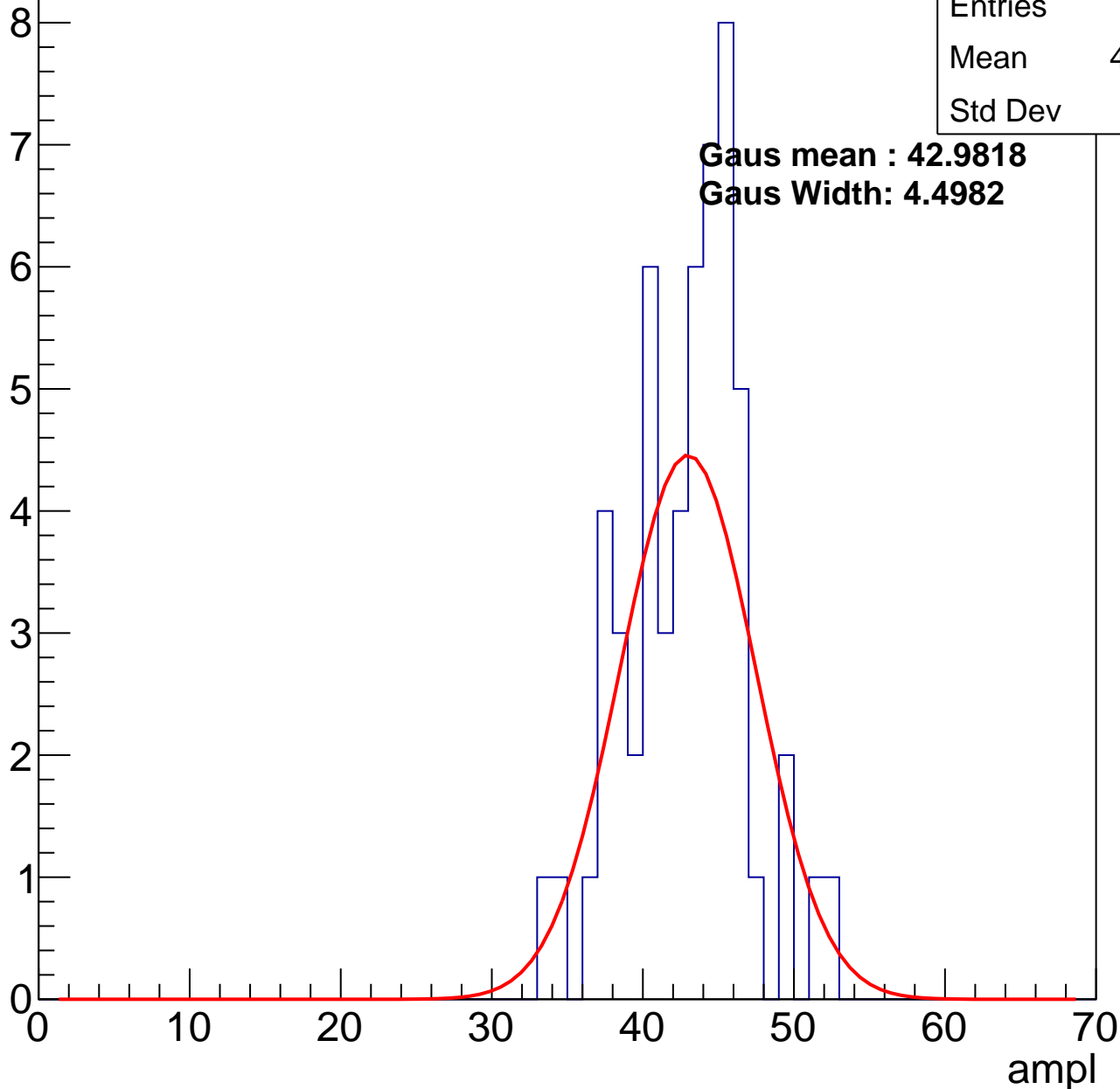
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	42.46
Std Dev	3.9

**Gaus mean : 42.9818**

**Gaus Width: 4.4982**

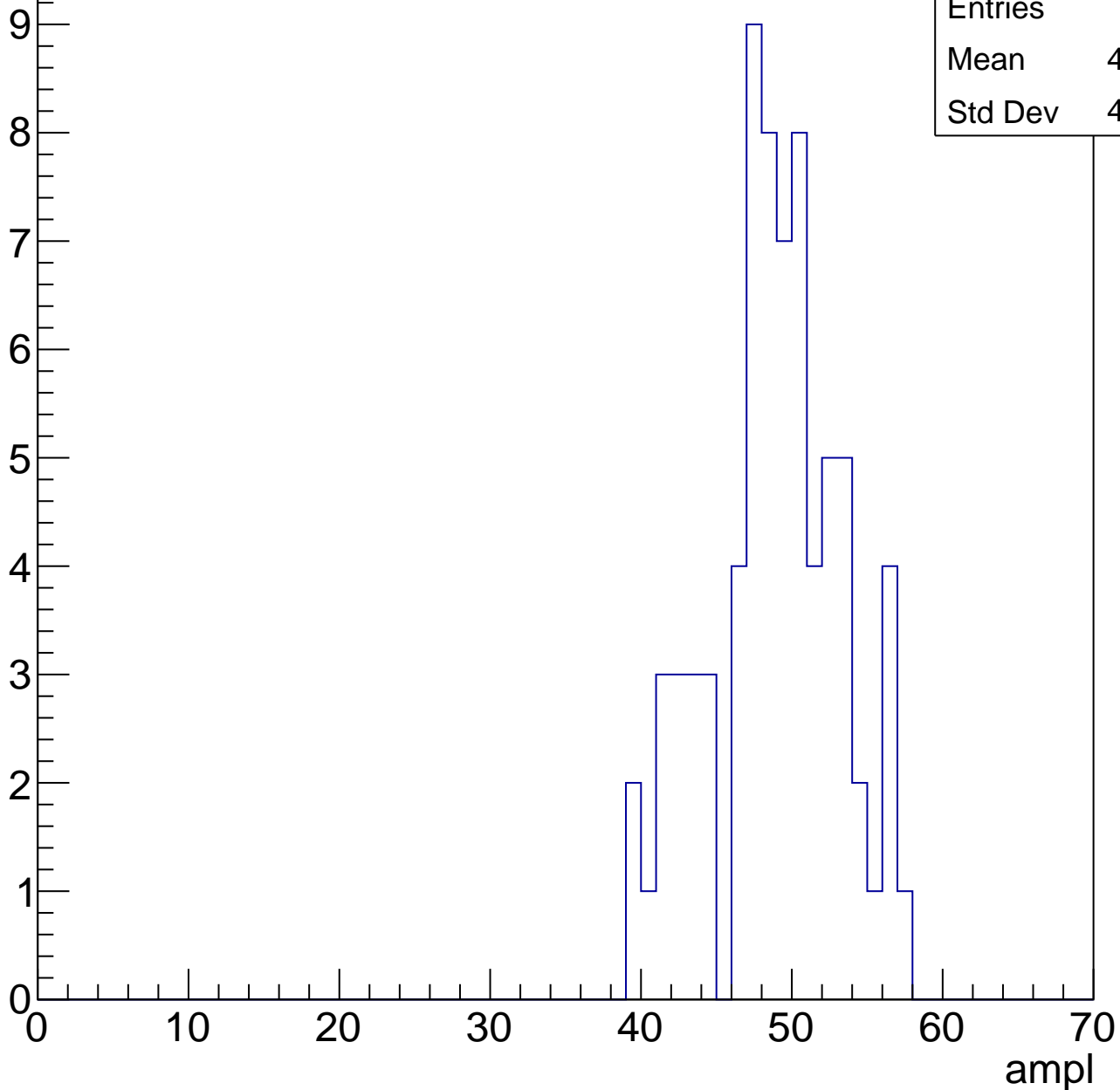


# B1L103S, U26-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	48.42
Std Dev	4.306

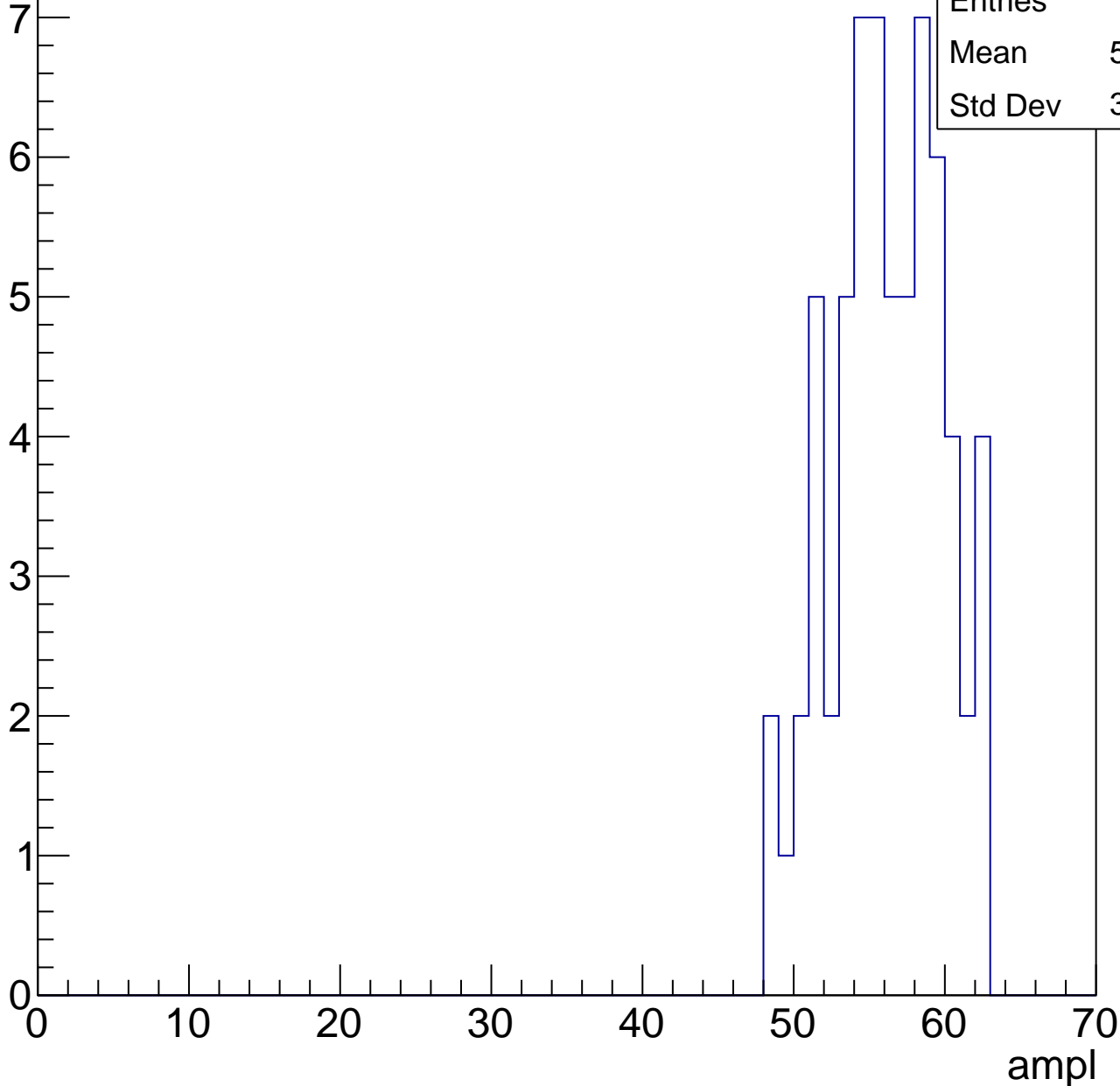


# B1L103S, U26-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	55.73
Std Dev	3.594

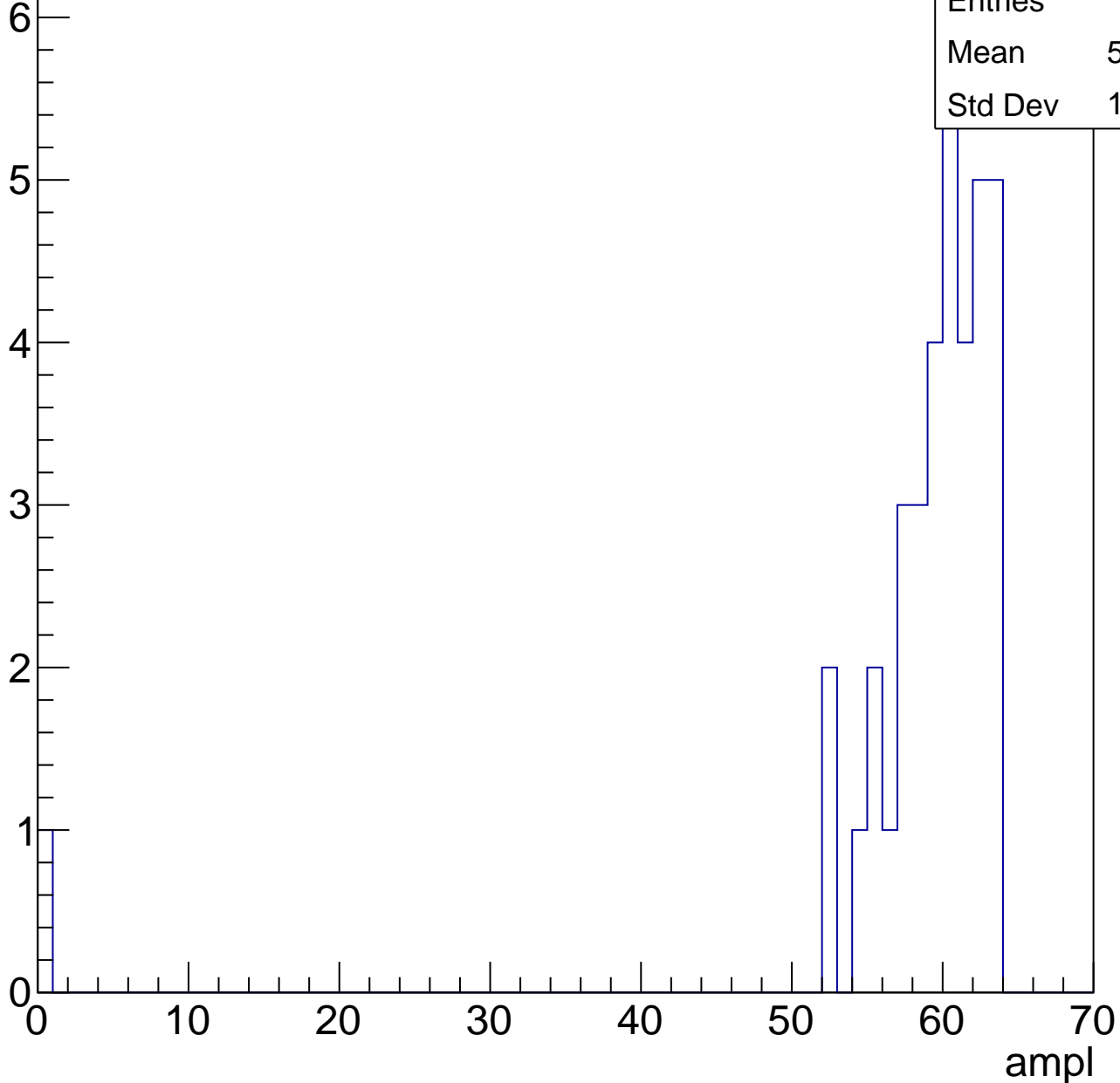


# B1L103S, U26-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	37
Mean	57.68
Std Dev	10.06

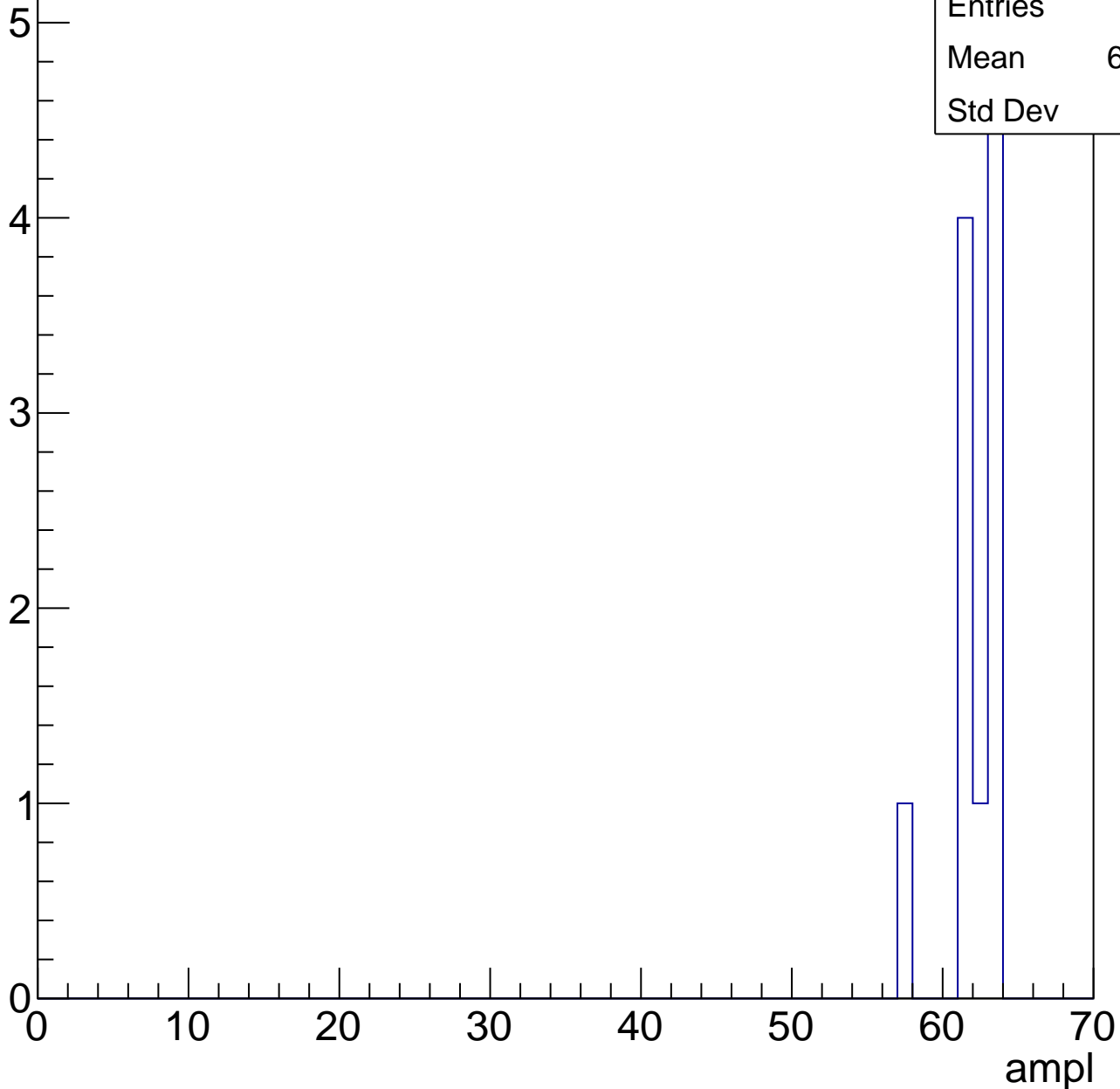


# B1L103S, U26-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	11
Mean	61.64
Std Dev	1.72





# B1L103S, U26-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U26-ch111, adc0

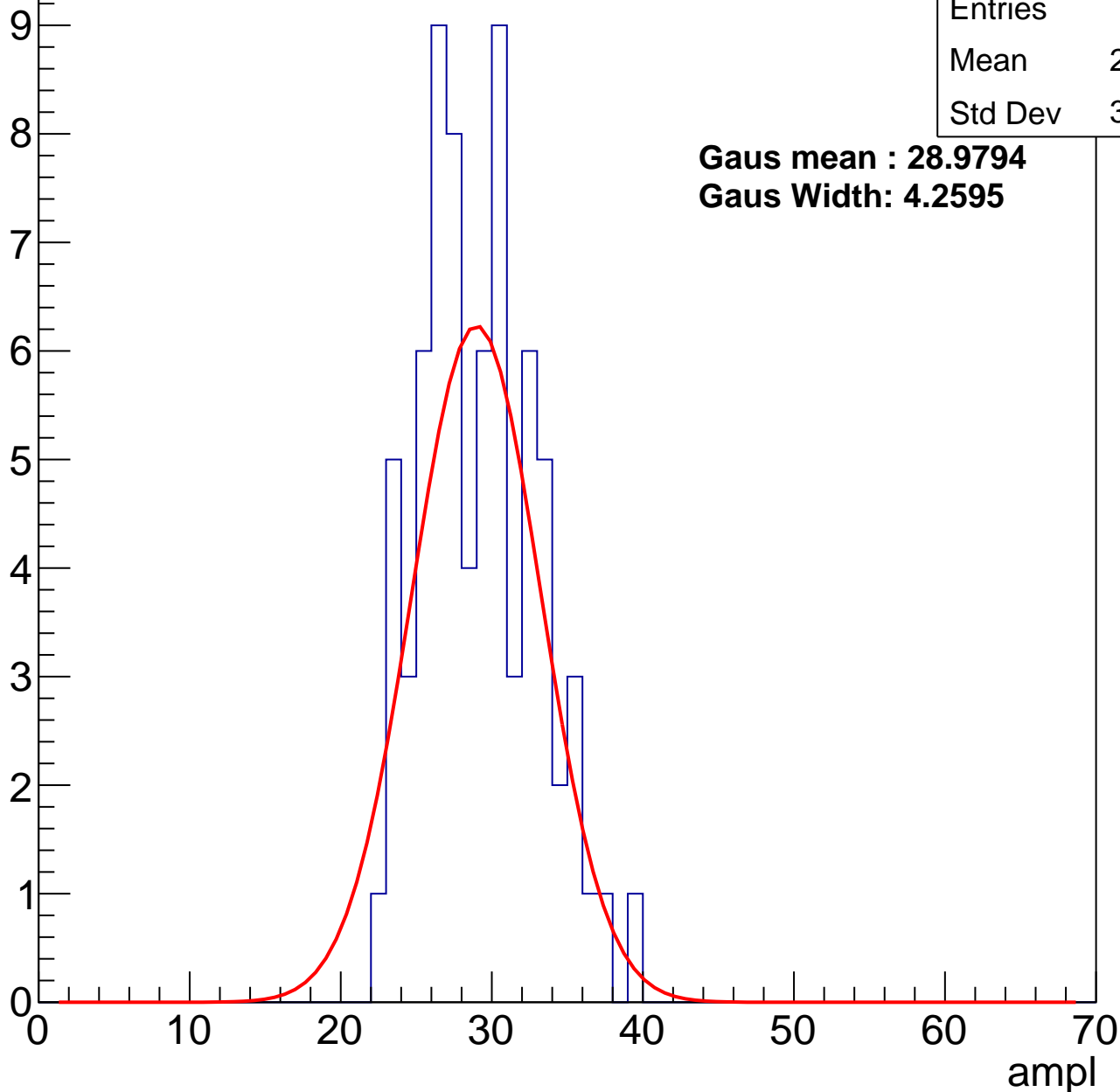
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	28.77
Std Dev	3.773

**Gaus mean : 28.9794**

**Gaus Width: 4.2595**



# B1L103S, U26-ch111, adc1

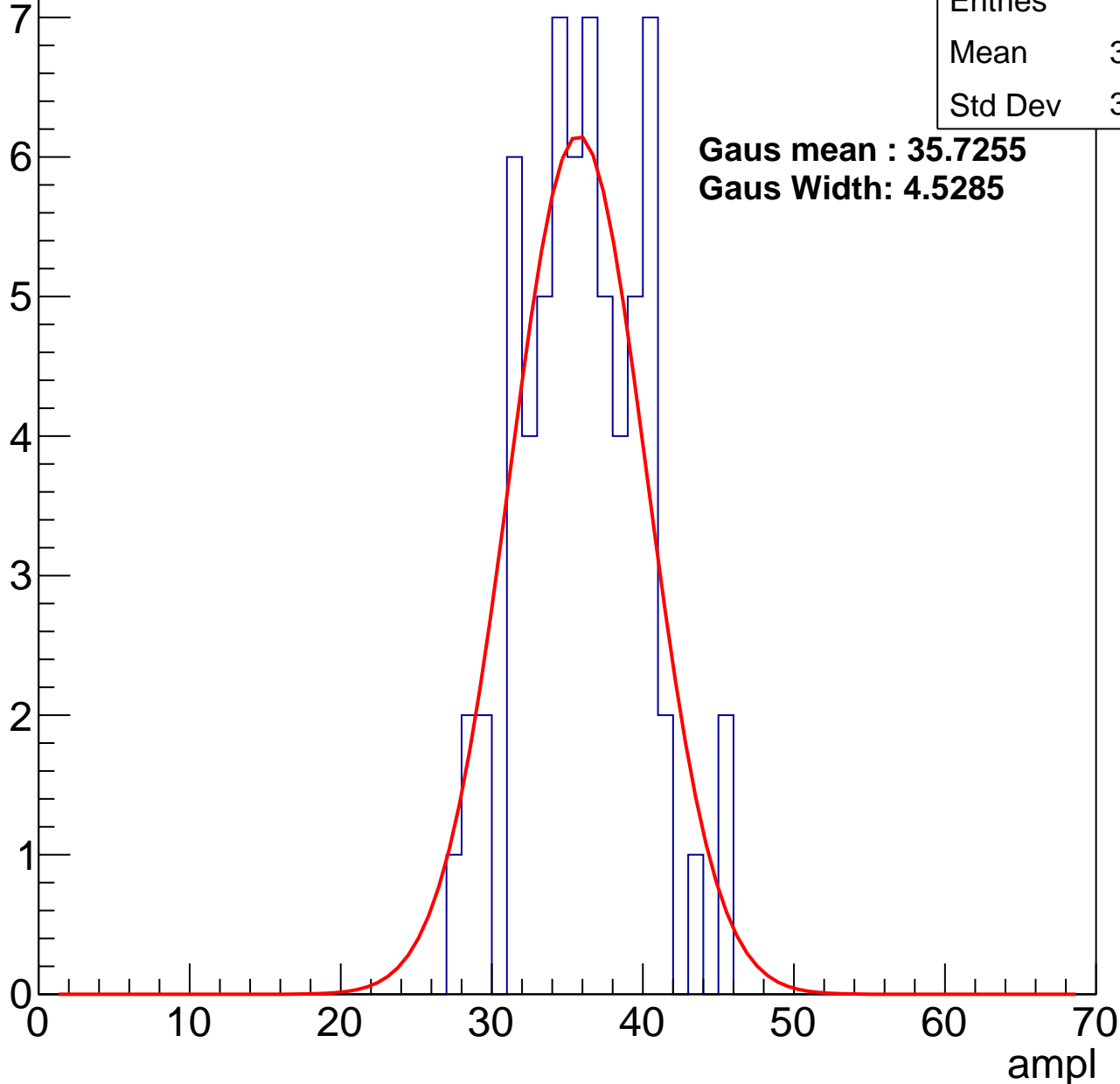
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	35.56
Std Dev	3.943

**Gaus mean : 35.7255**

**Gaus Width: 4.5285**



# B1L103S, U26-ch111, adc2

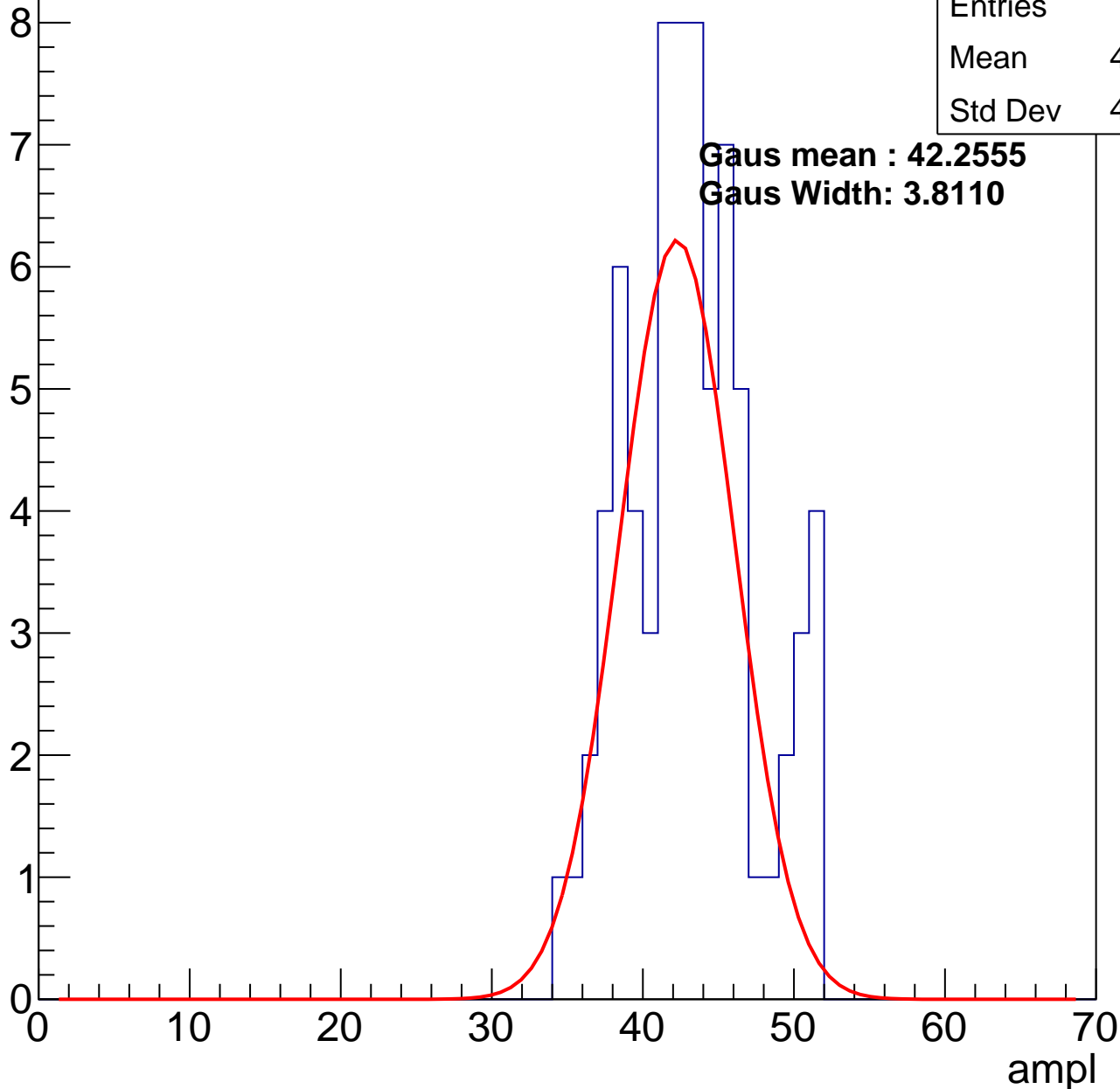
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	42.64
Std Dev	4.143

**Gaus mean : 42.2555**

**Gaus Width: 3.8110**

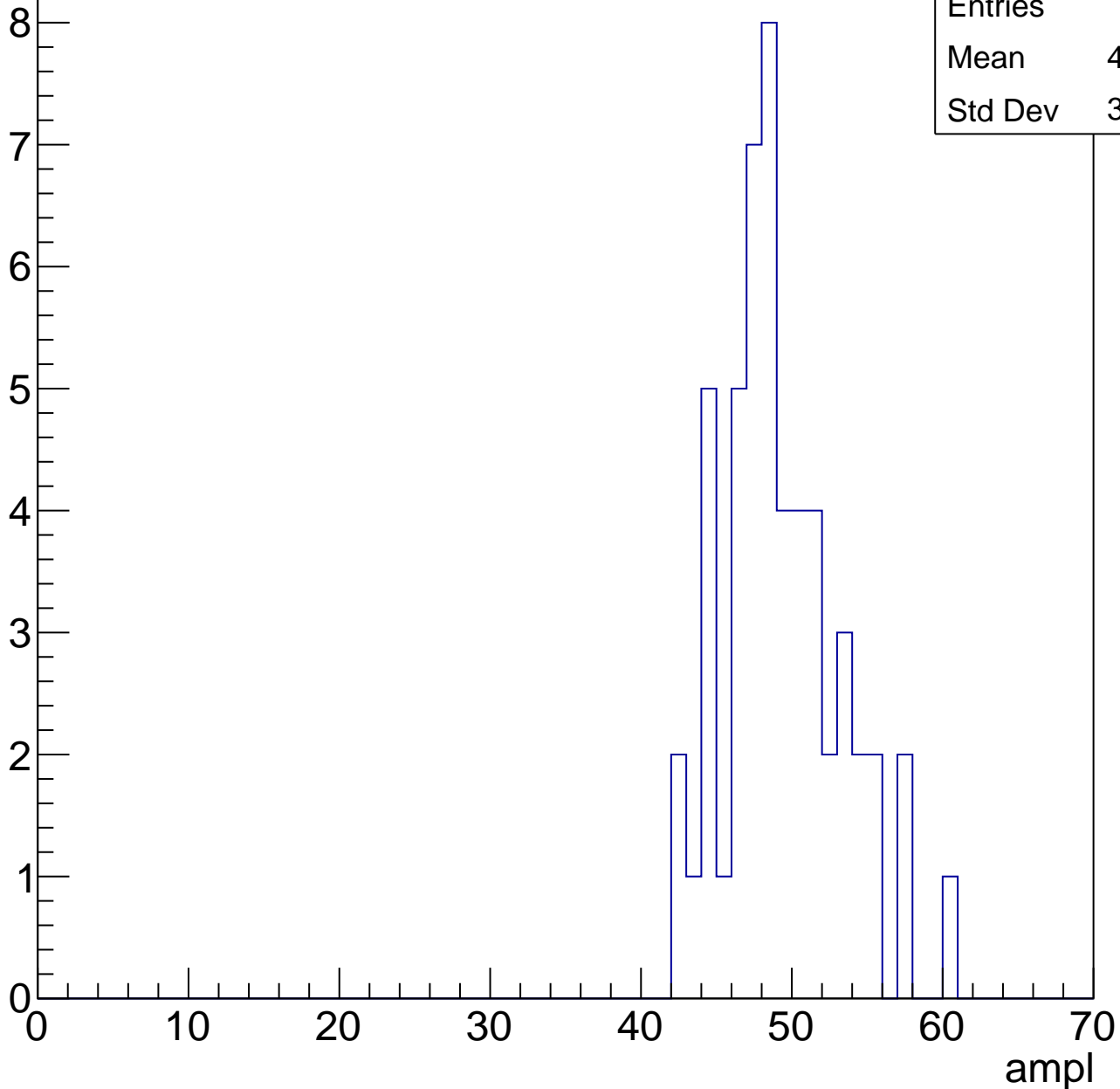


# B1L103S, U26-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	48.87
Std Dev	3.914

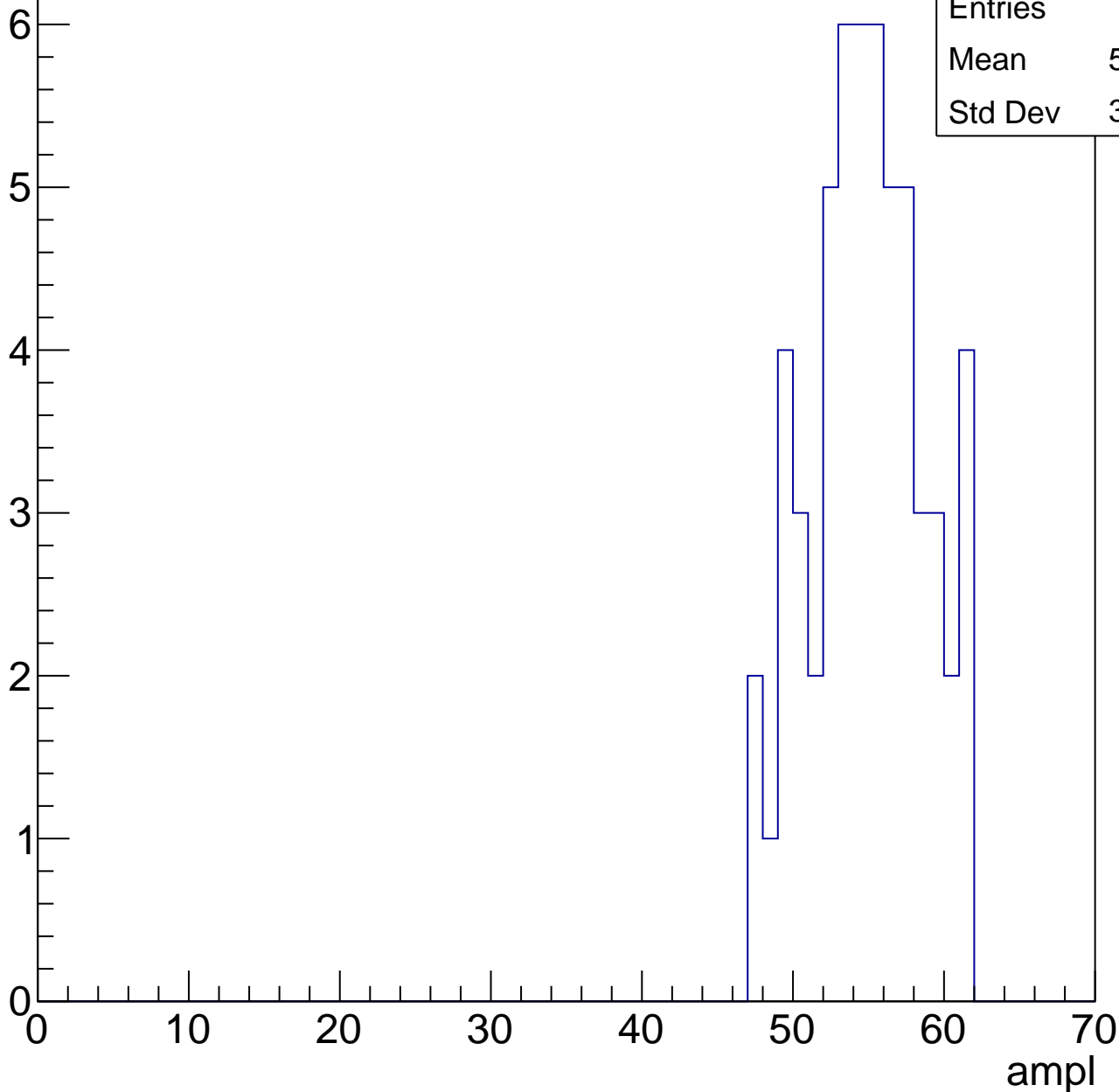


# B1L103S, U26-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	54.42
Std Dev	3.694

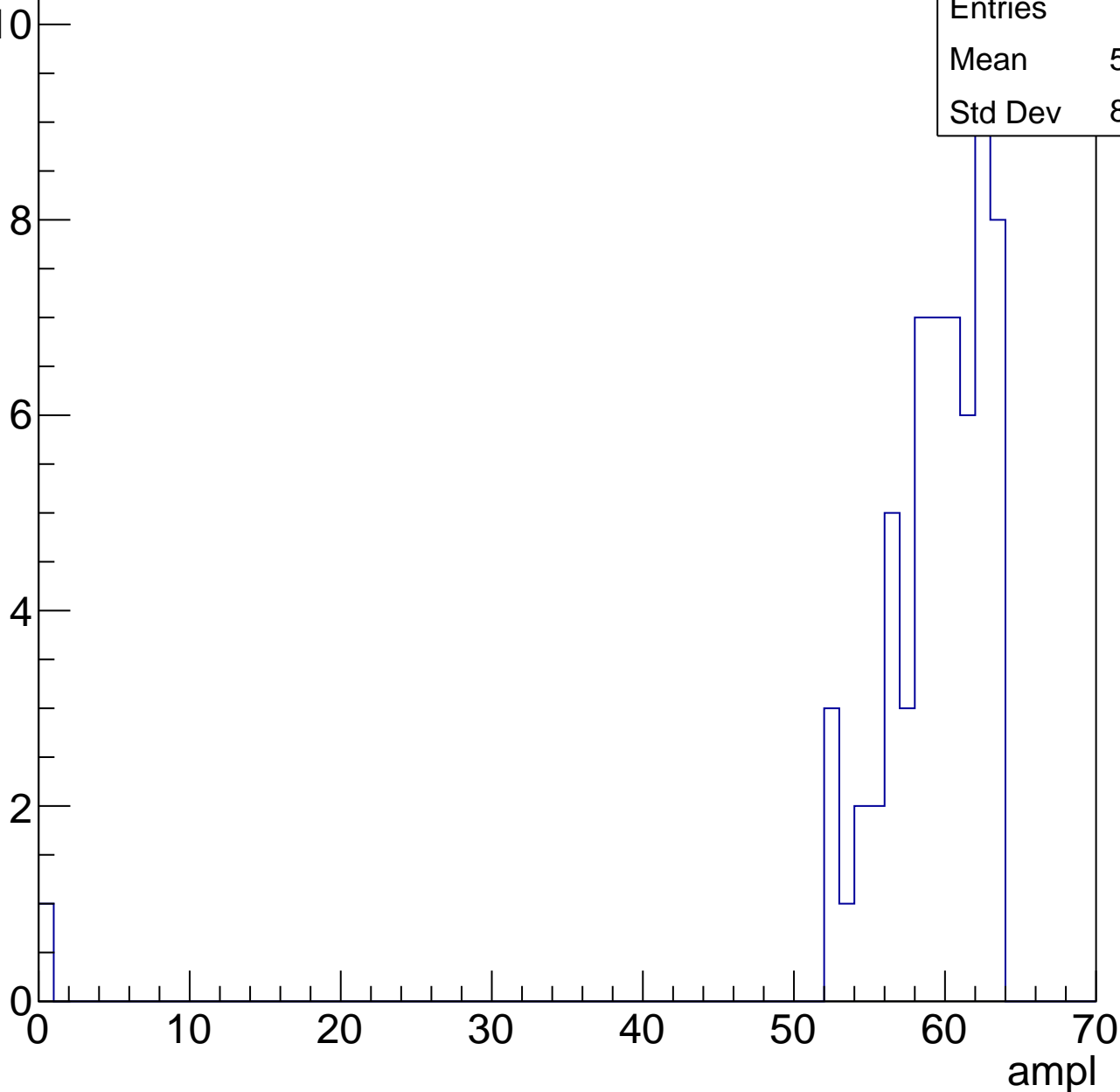


# B1L103S, U26-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	58.18
Std Dev	8.049



# B1L103S, U26-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U26-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	21
Std Dev	0

ampl

# B1L103S, U26-ch112, adc0

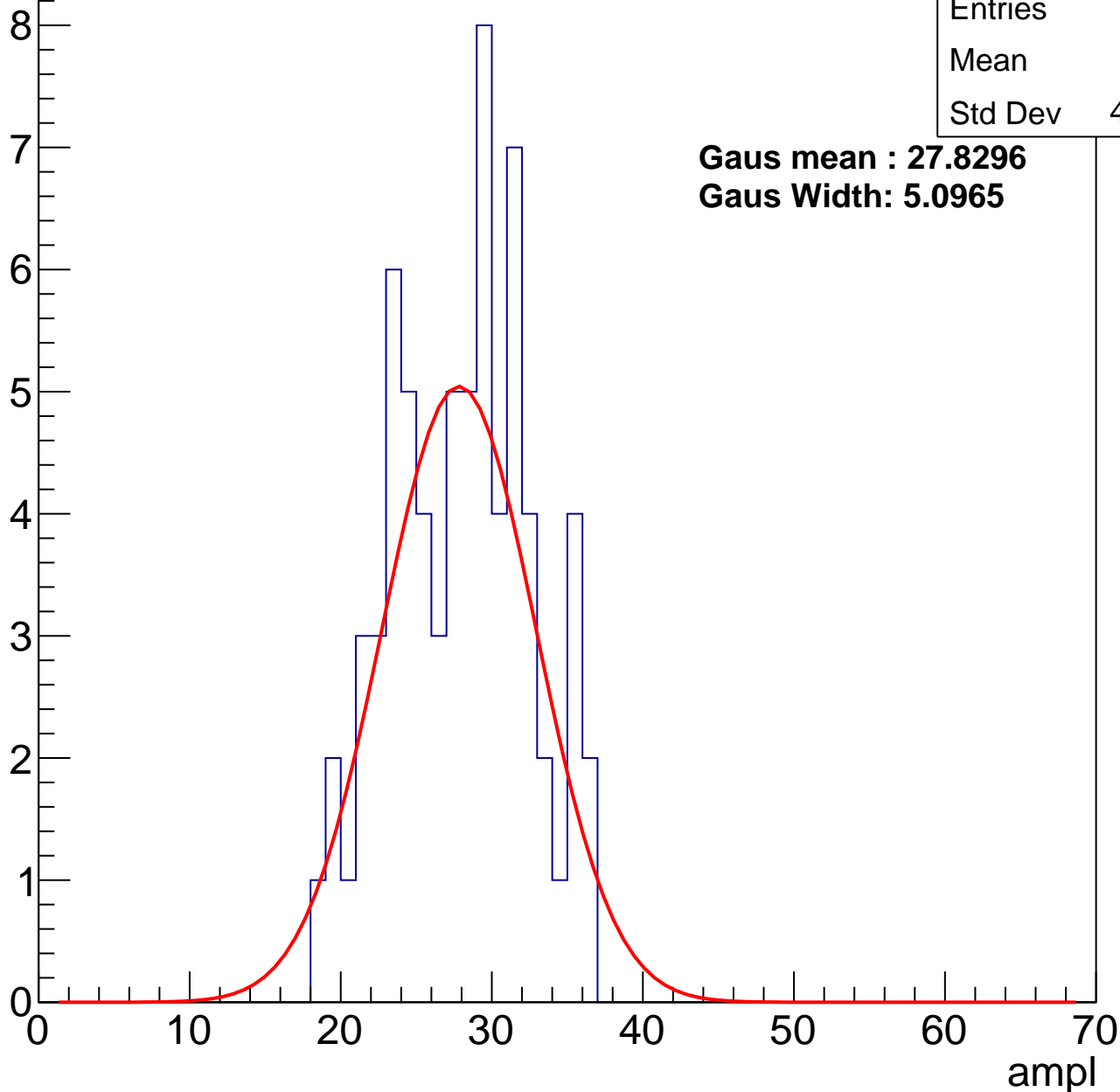
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	27.5
Std Dev	4.484

**Gaus mean : 27.8296**

**Gaus Width: 5.0965**



# B1L103S, U26-ch112, adc1

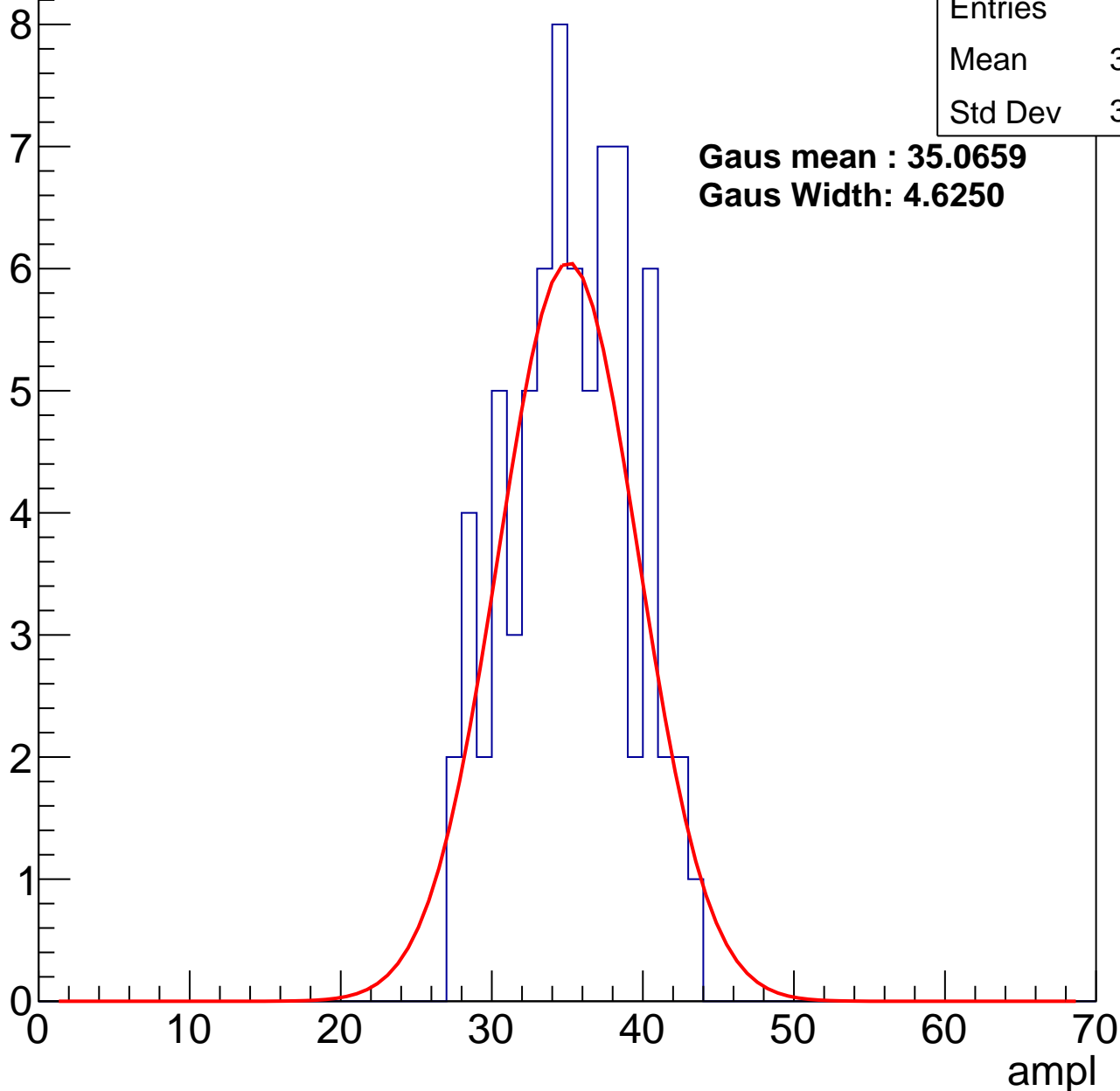
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	73
Mean	34.78
Std Dev	3.977

**Gaus mean : 35.0659**

**Gaus Width: 4.6250**



# B1L103S, U26-ch112, adc2

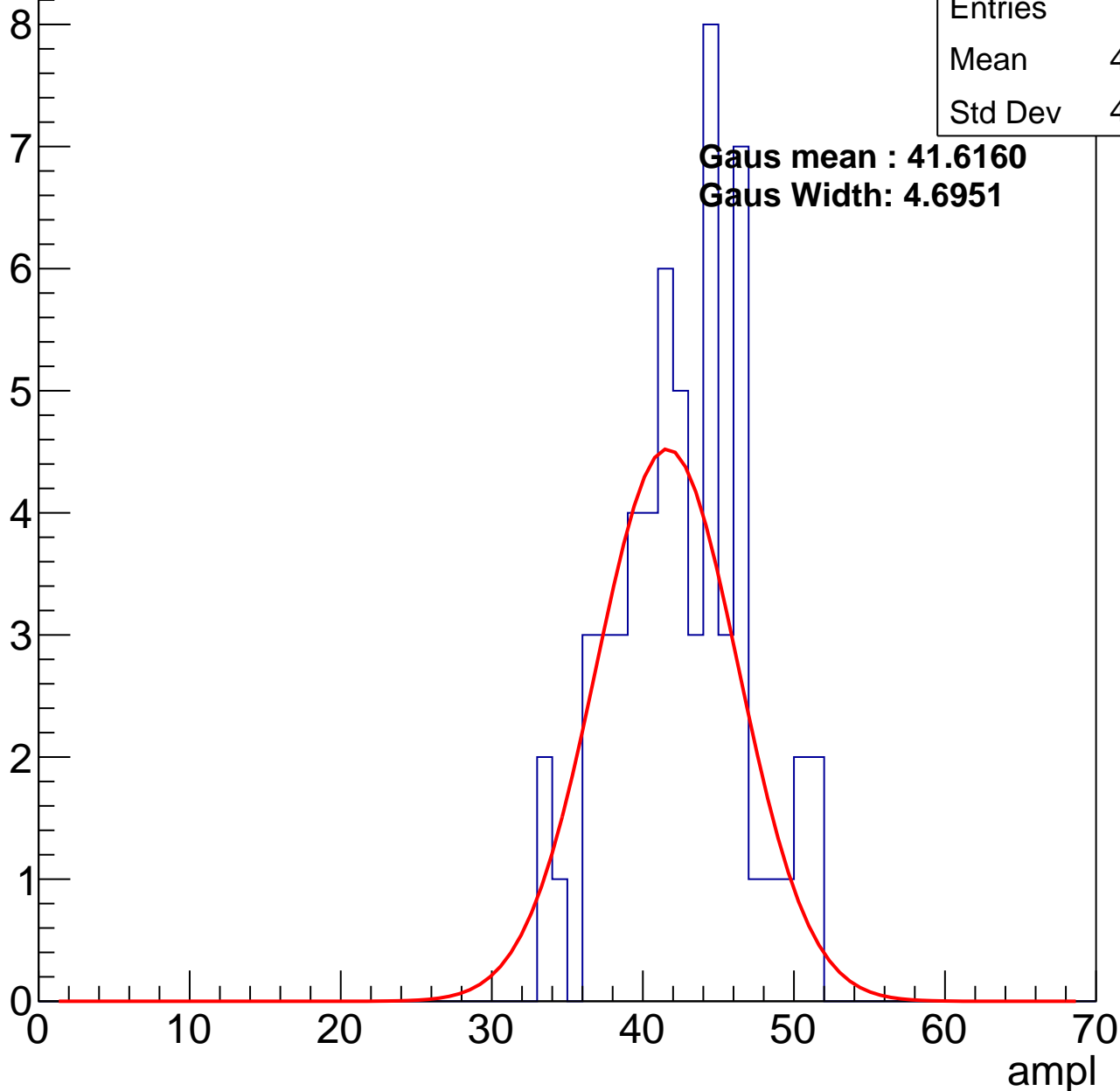
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	42.19
Std Dev	4.292

**Gaus mean : 41.6160**

**Gaus Width: 4.6951**

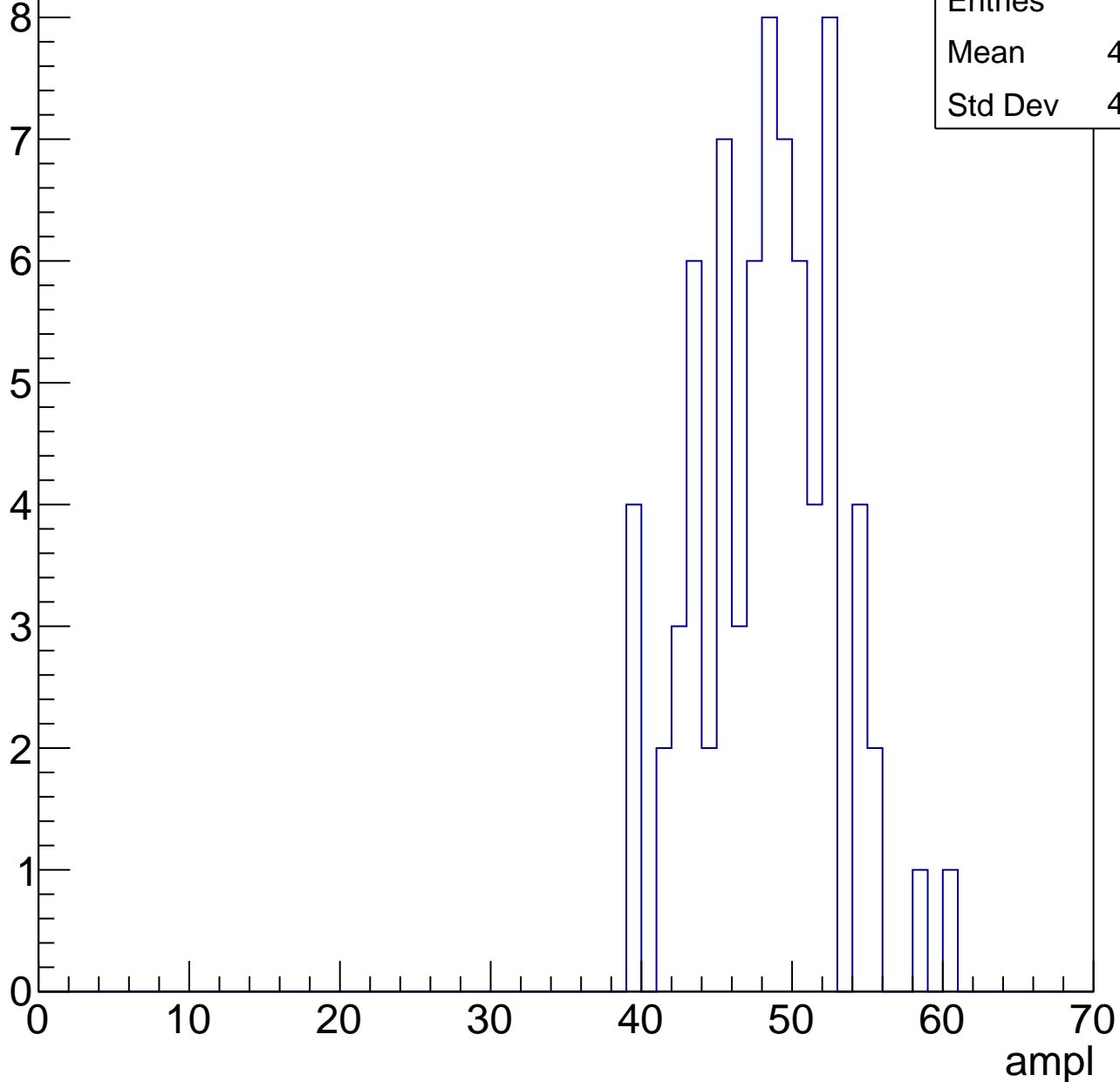


# B1L103S, U26-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	74
Mean	47.78
Std Dev	4.458

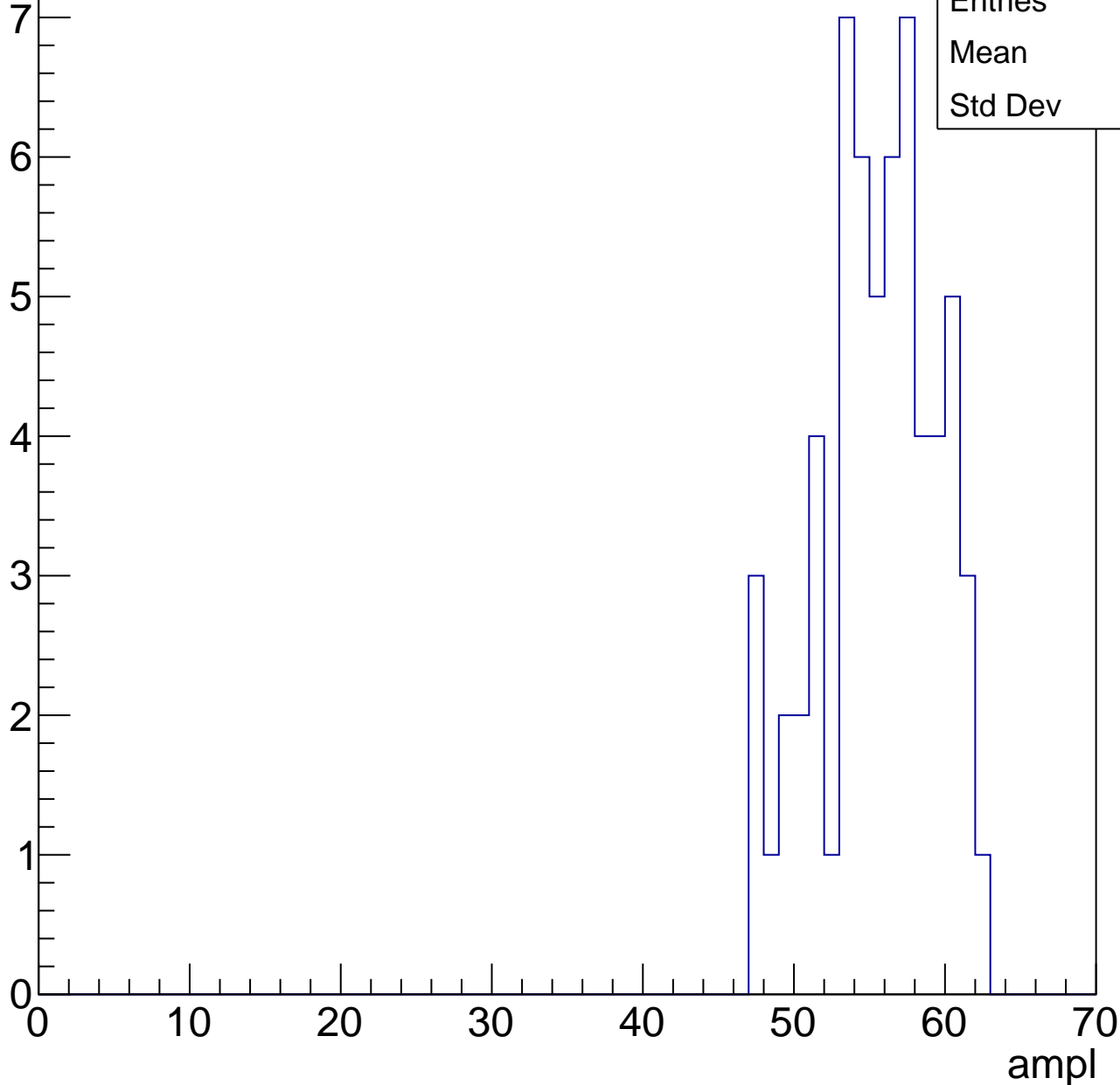


# B1L103S, U26-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	55.1
Std Dev	3.81

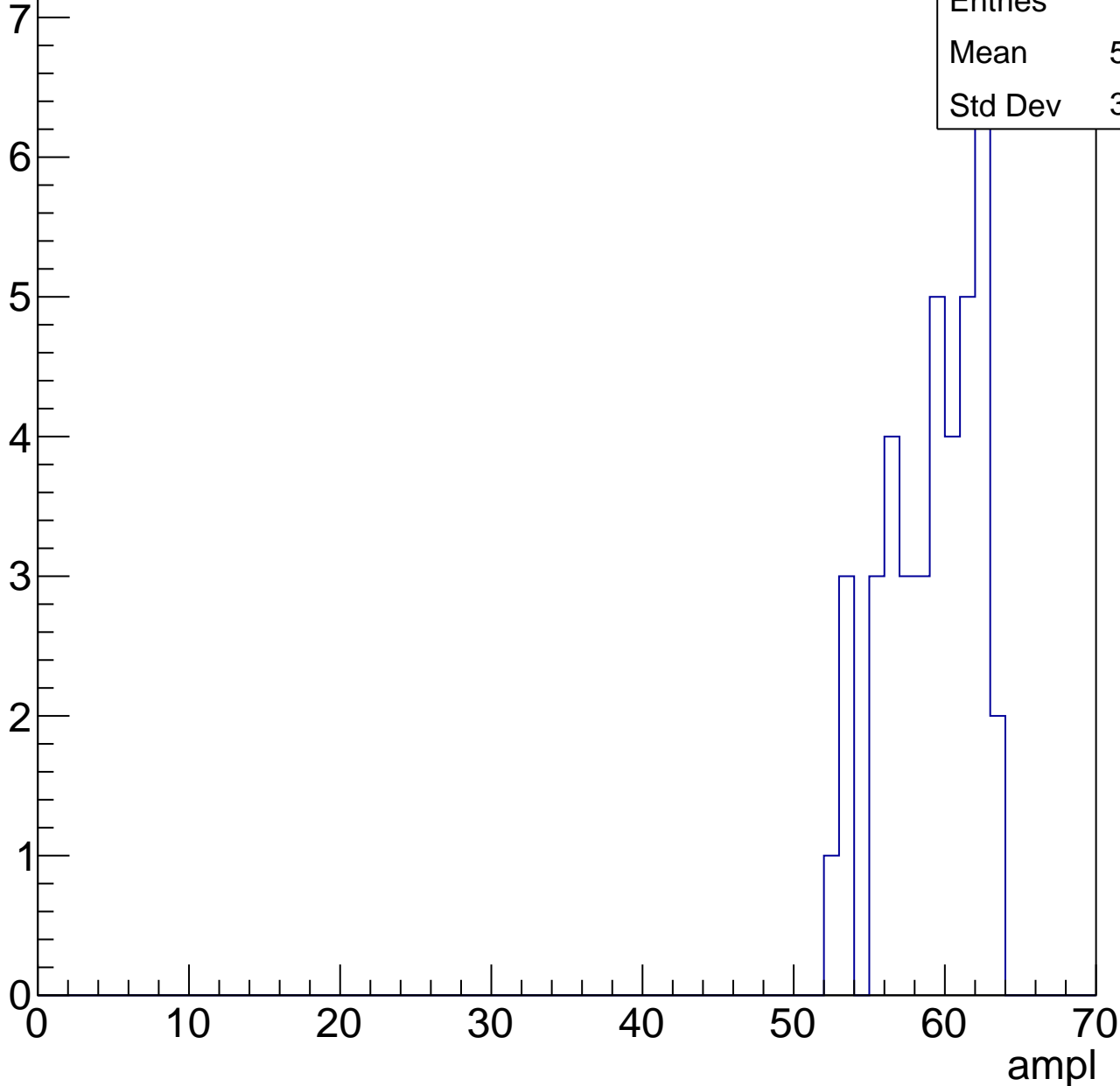


# B1L103S, U26-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	40
Mean	58.62
Std Dev	3.039

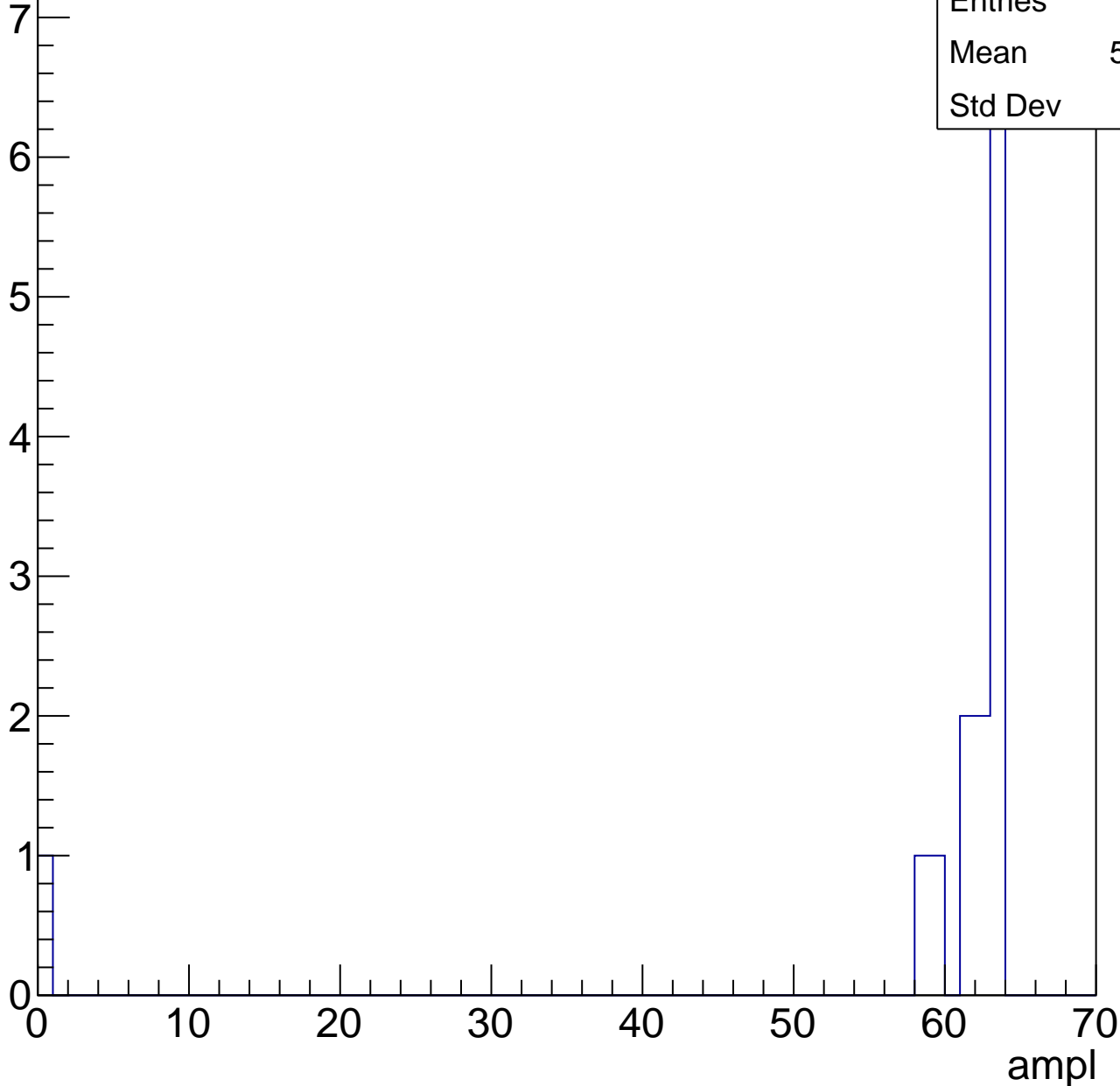


# B1L103S, U26-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	14
Mean	57.43
Std Dev	16





# B1L103S, U26-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U26-ch113, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	74
Mean	28.54
Std Dev	6.134

**Gaus mean : 30.2950**

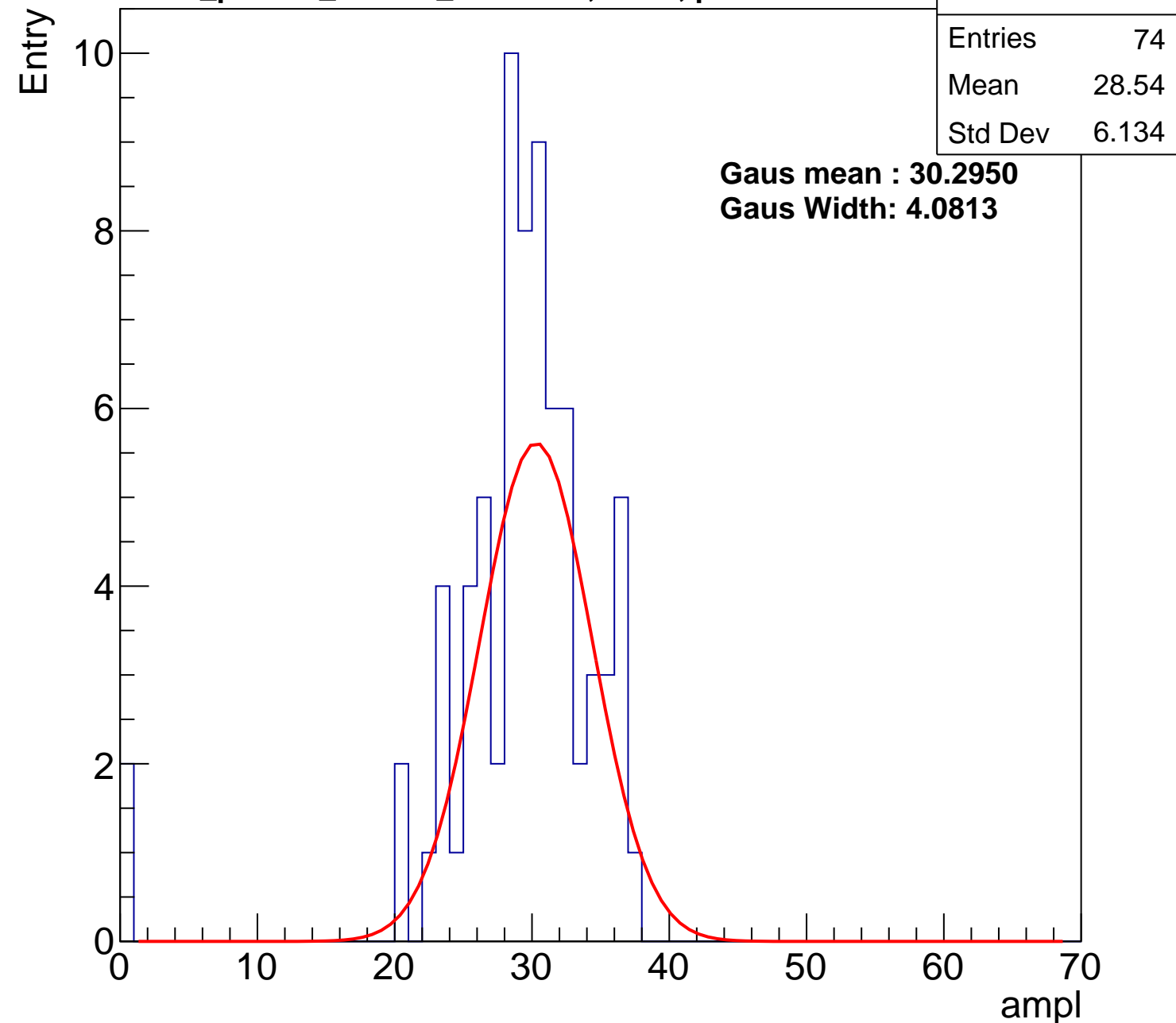
**Gaus Width: 4.0813**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch113, adc1

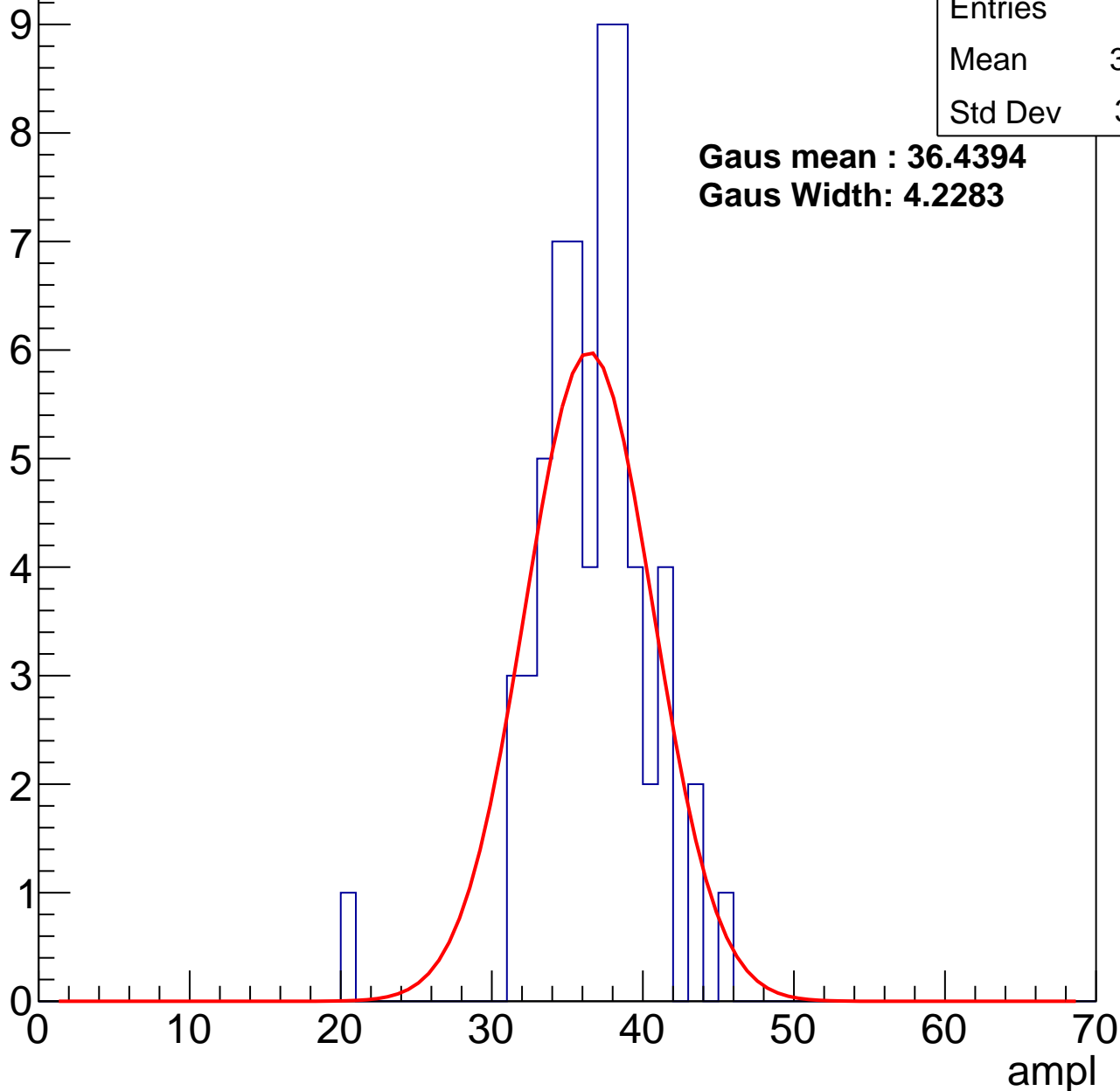
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	36.18
Std Dev	3.731

**Gaus mean : 36.4394**

**Gaus Width: 4.2283**



# B1L103S, U26-ch113, adc2

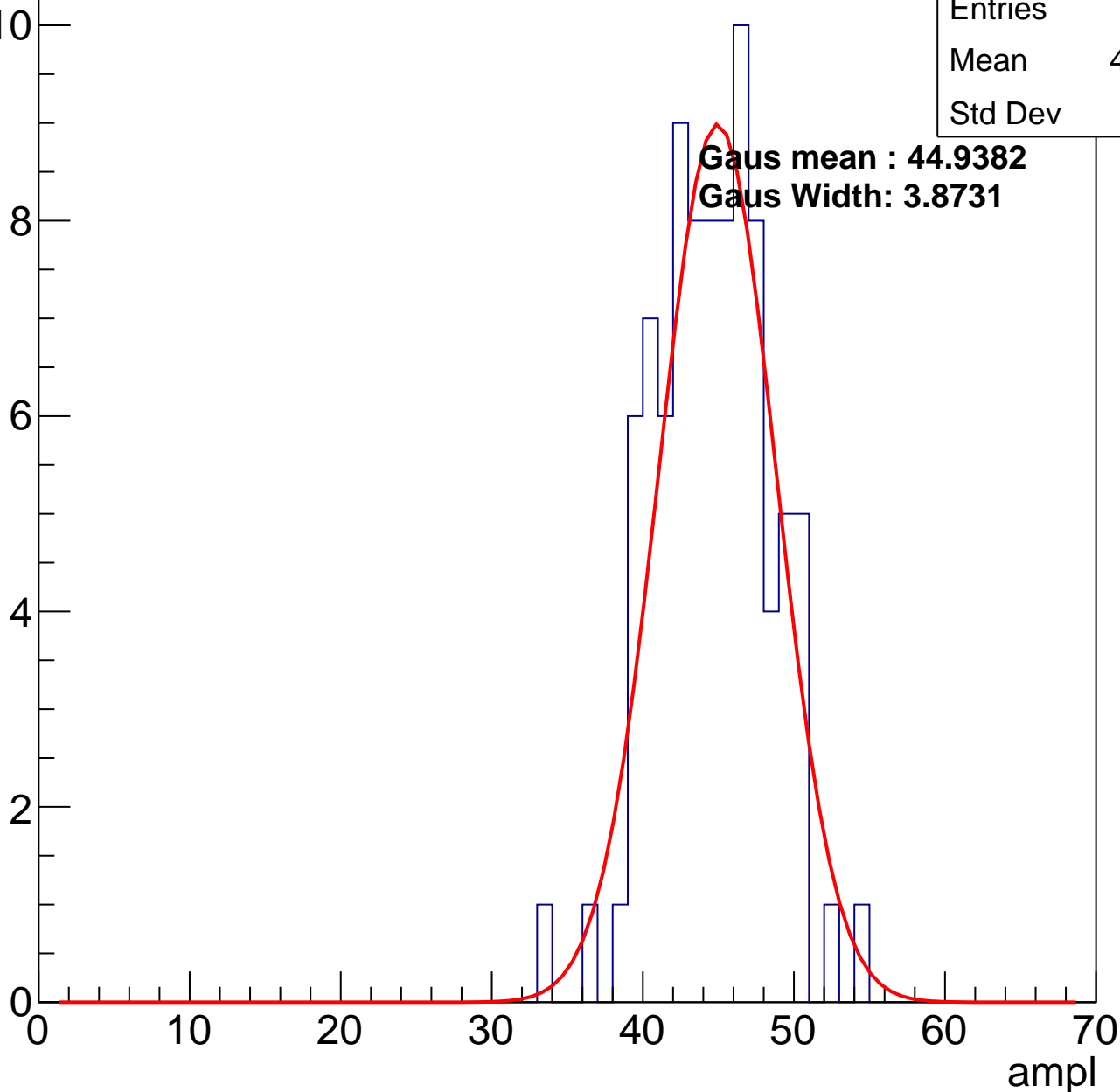
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	89
Mean	44.16
Std Dev	3.72

**Gaus mean : 44.9382**

**Gaus Width: 3.8731**

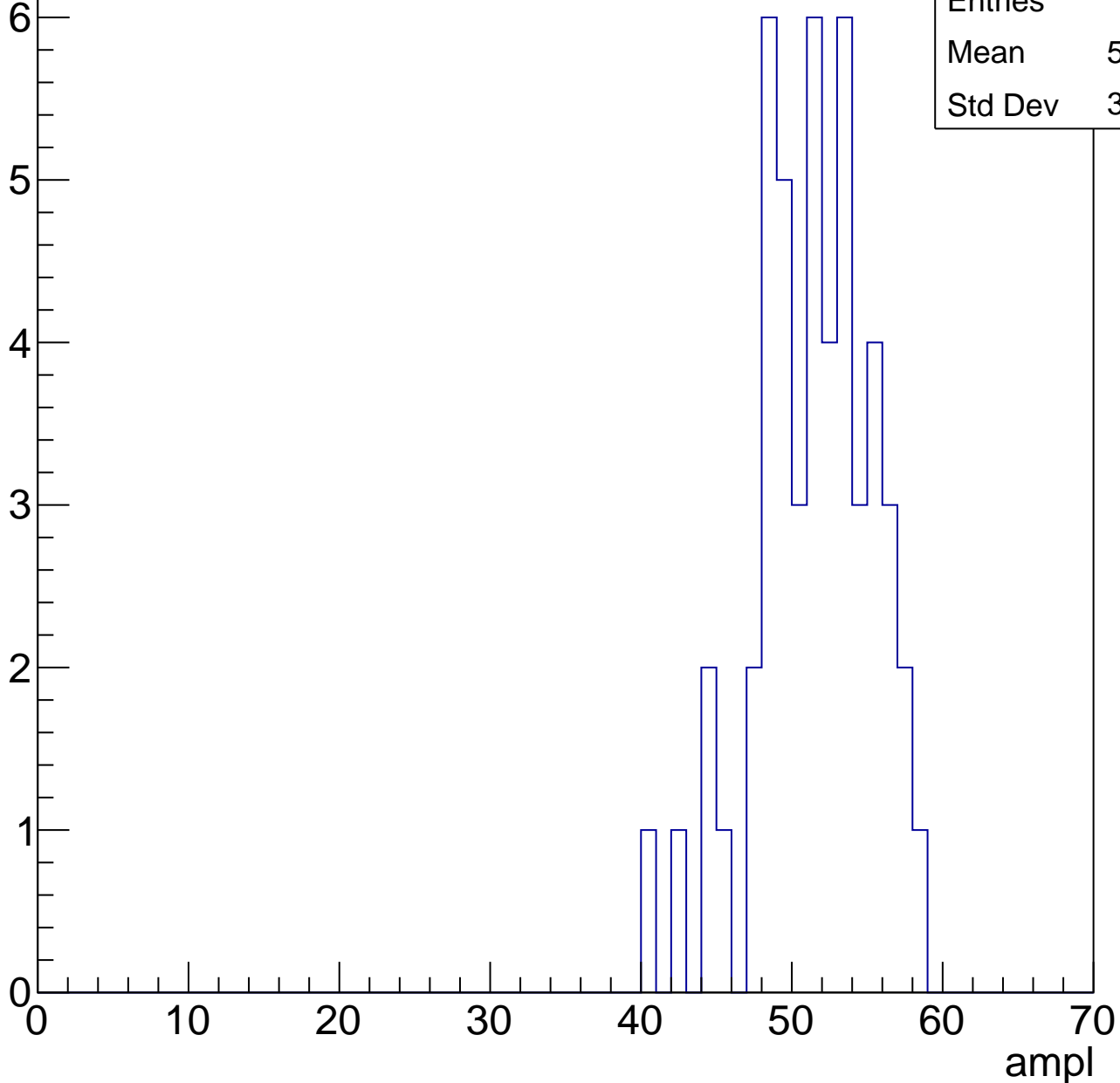


# B1L103S, U26-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	50.92
Std Dev	3.898

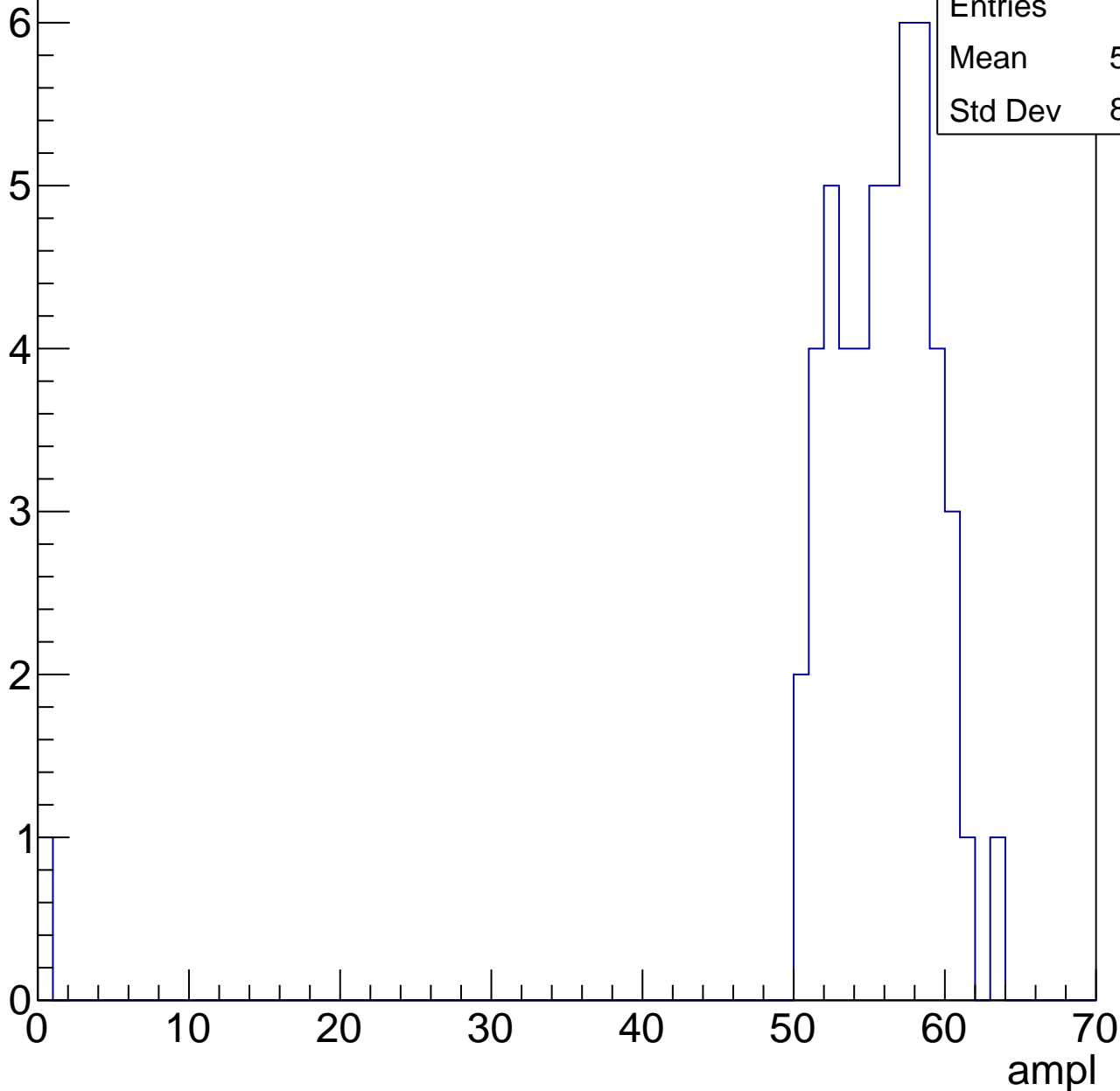


# B1L103S, U26-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	54.45
Std Dev	8.297



# B1L103S, U26-ch113, adc5

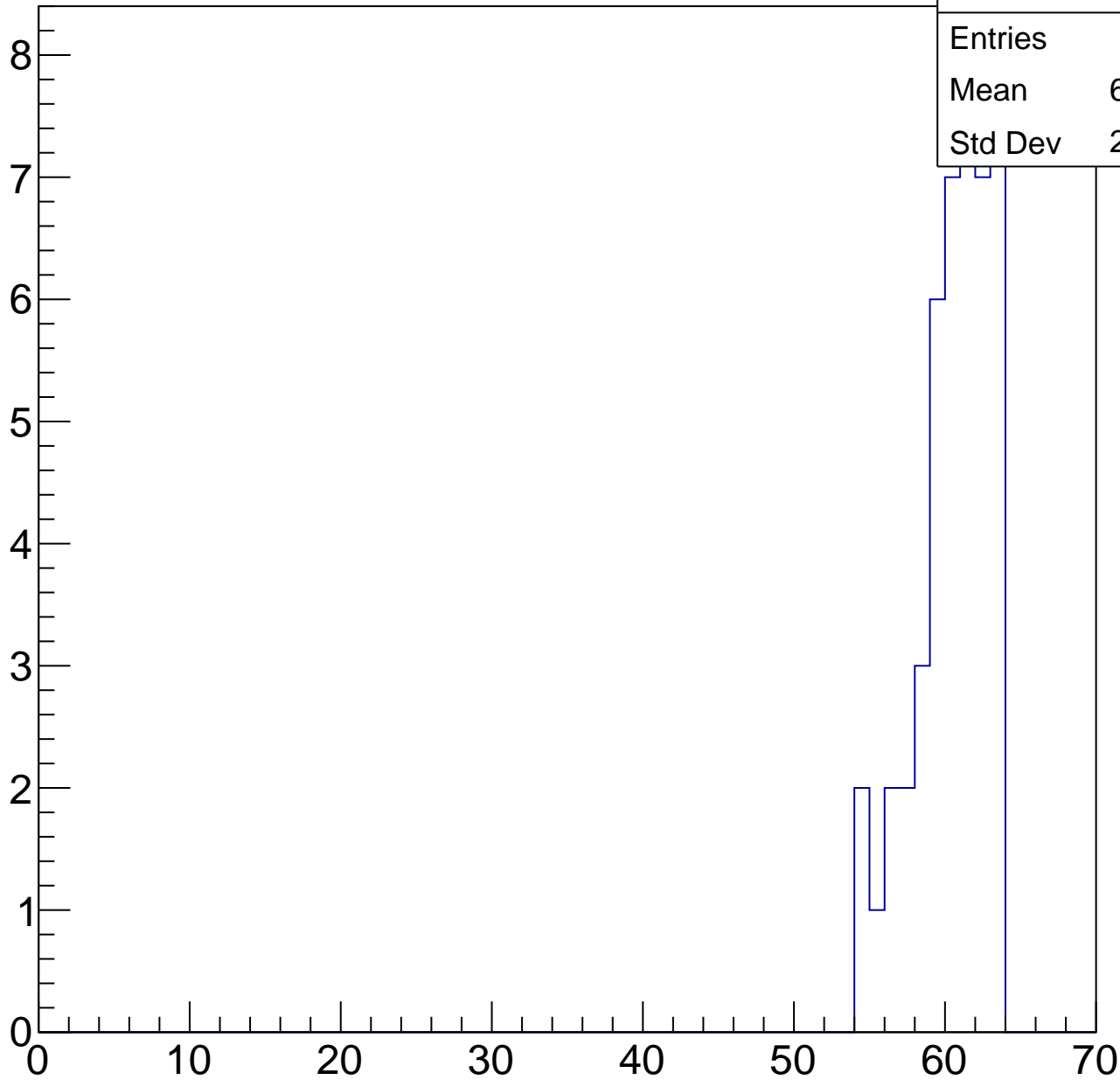
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	46
Mean	60.07
Std Dev	2.435

ampl



# B1L103S, U26-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U26-ch114, adc0

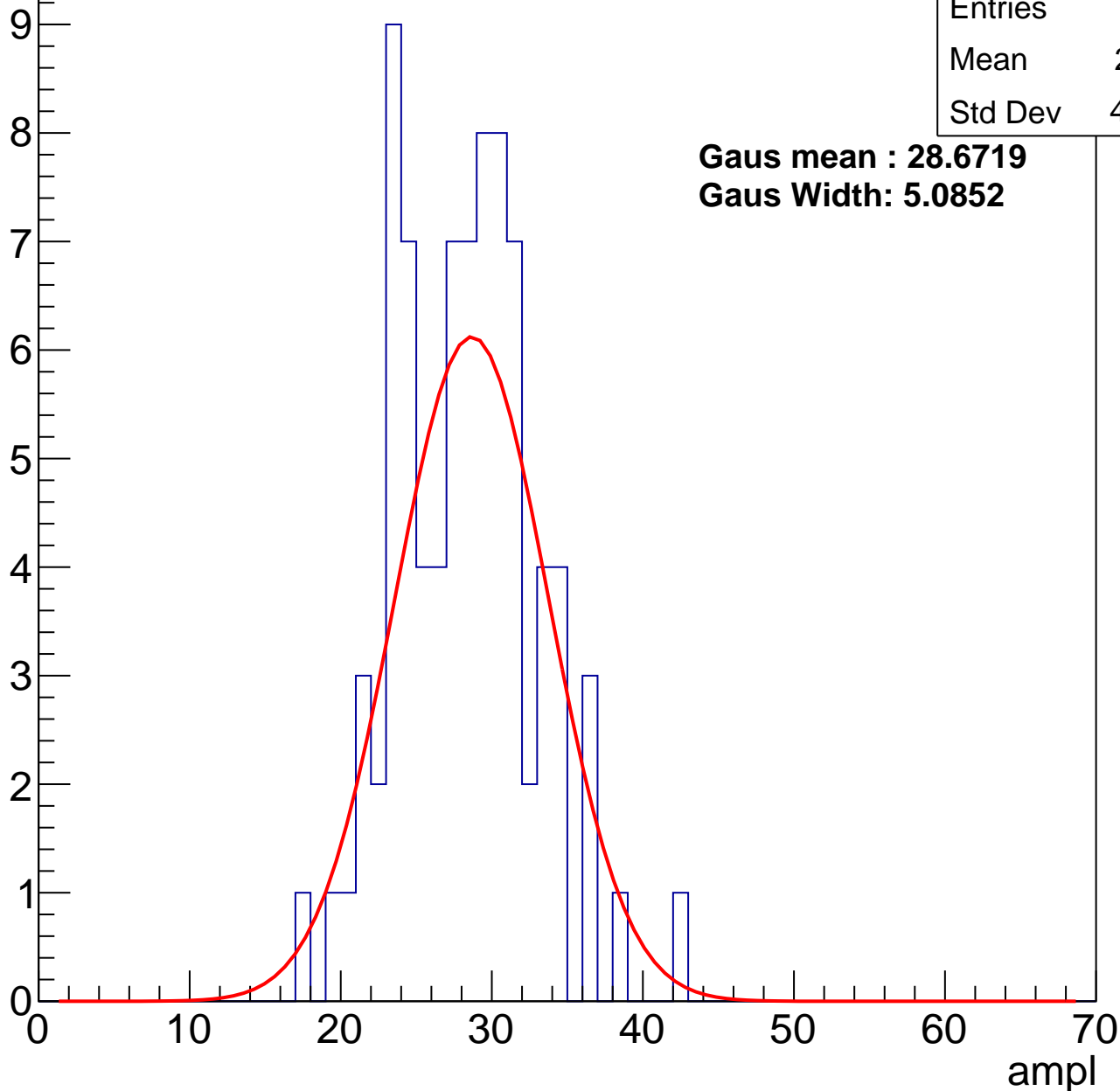
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	84
Mean	27.81
Std Dev	4.558

**Gaus mean : 28.6719**

**Gaus Width: 5.0852**



# B1L103S, U26-ch114, adc1

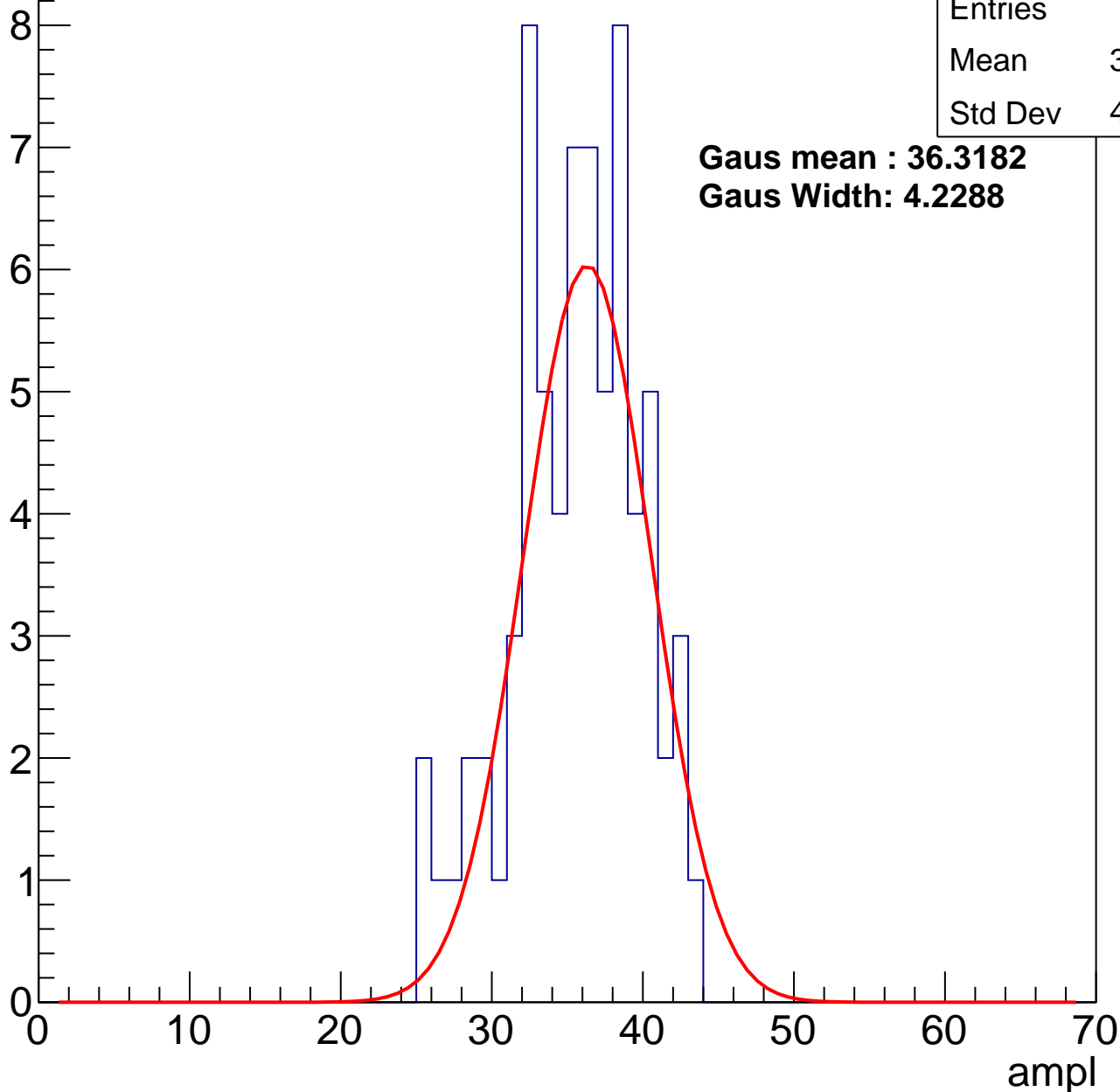
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	35.07
Std Dev	4.204

**Gaus mean : 36.3182**

**Gaus Width: 4.2288**



# B1L103S, U26-ch114, adc2

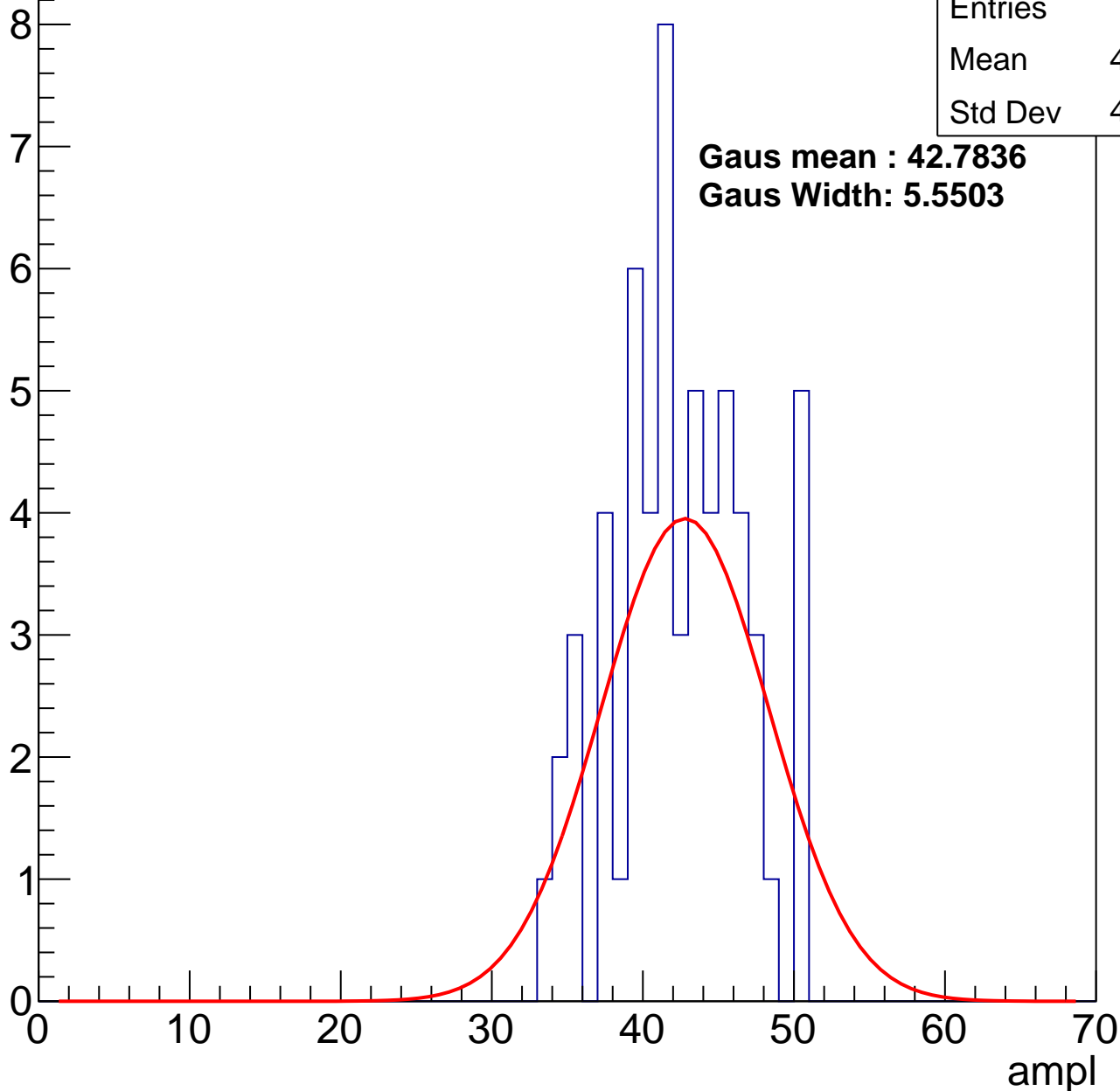
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	59
Mean	42.02
Std Dev	4.339

**Gaus mean : 42.7836**

**Gaus Width: 5.5503**

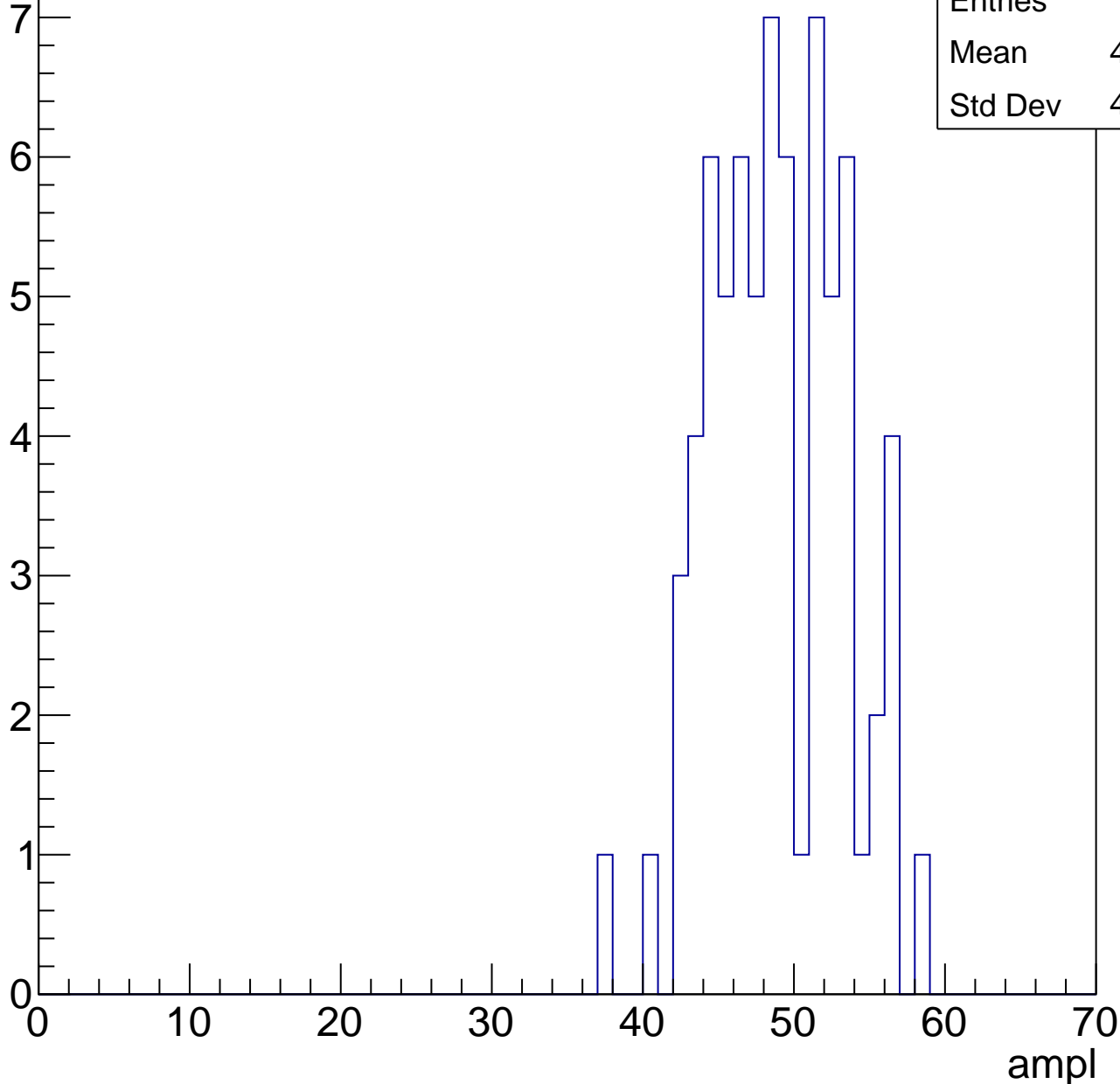


# B1L103S, U26-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	48.39
Std Dev	4.352

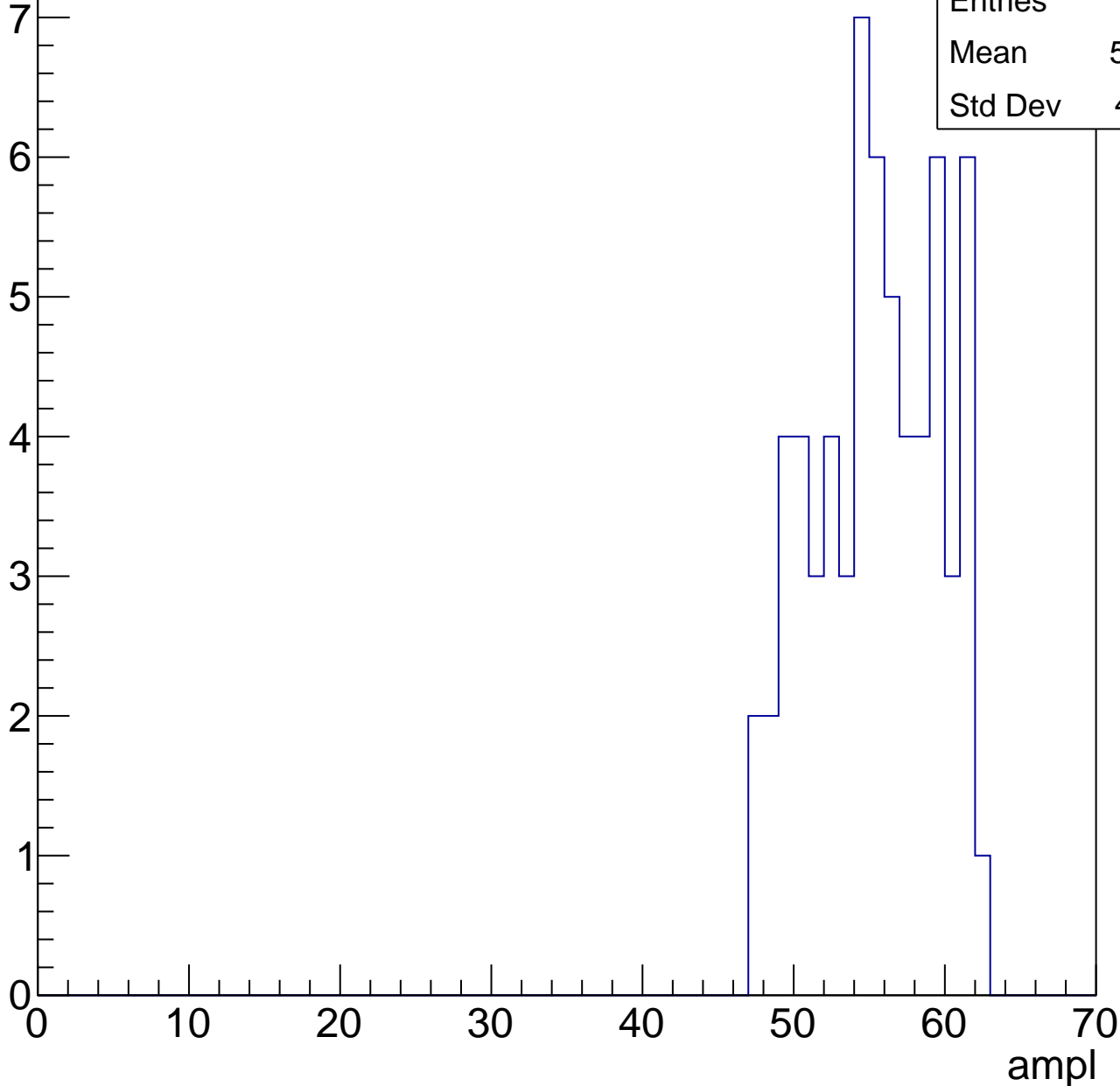


# B1L103S, U26-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	54.94
Std Dev	4.081

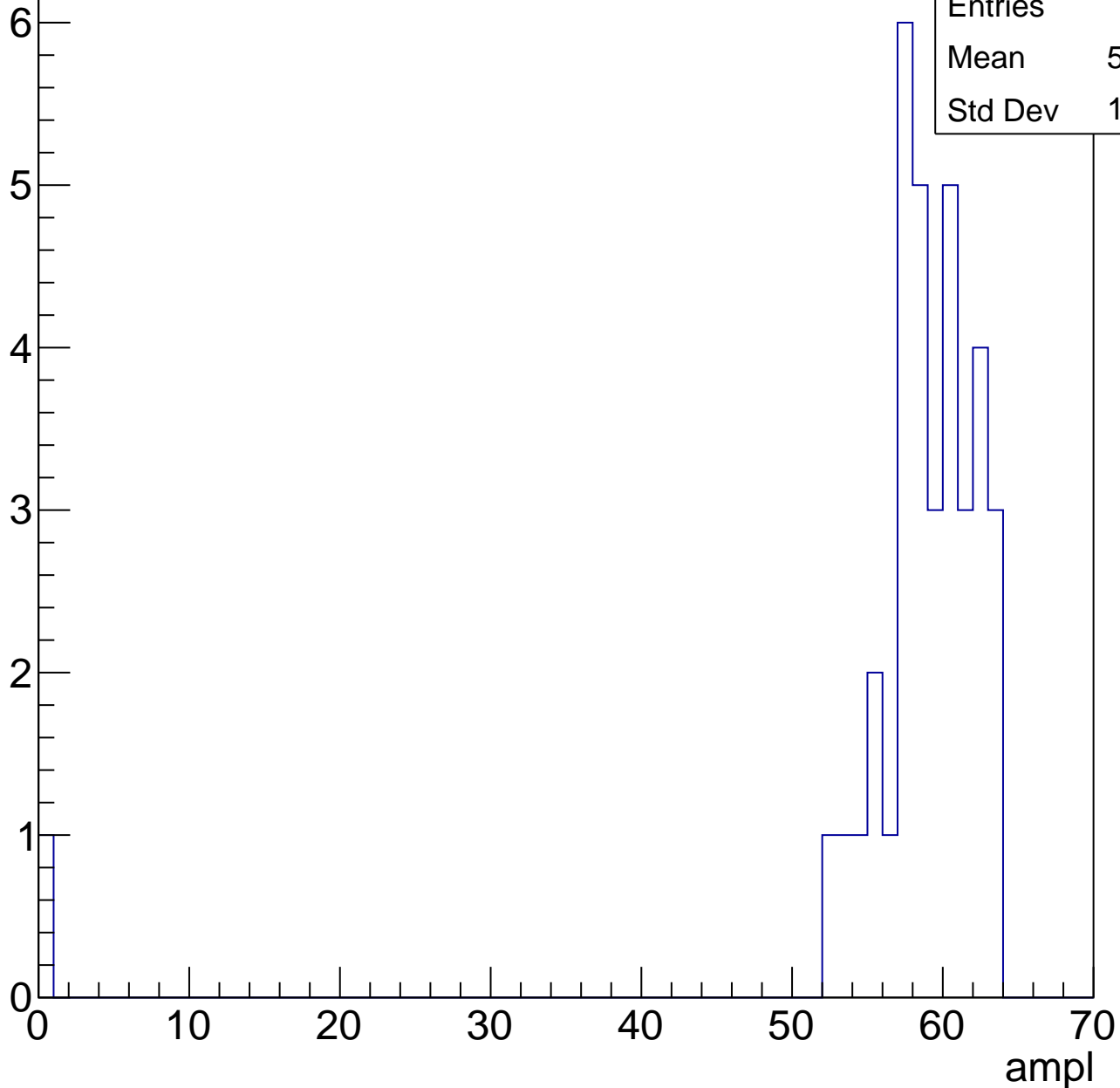


# B1L103S, U26-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	36
Mean	57.06
Std Dev	10.04

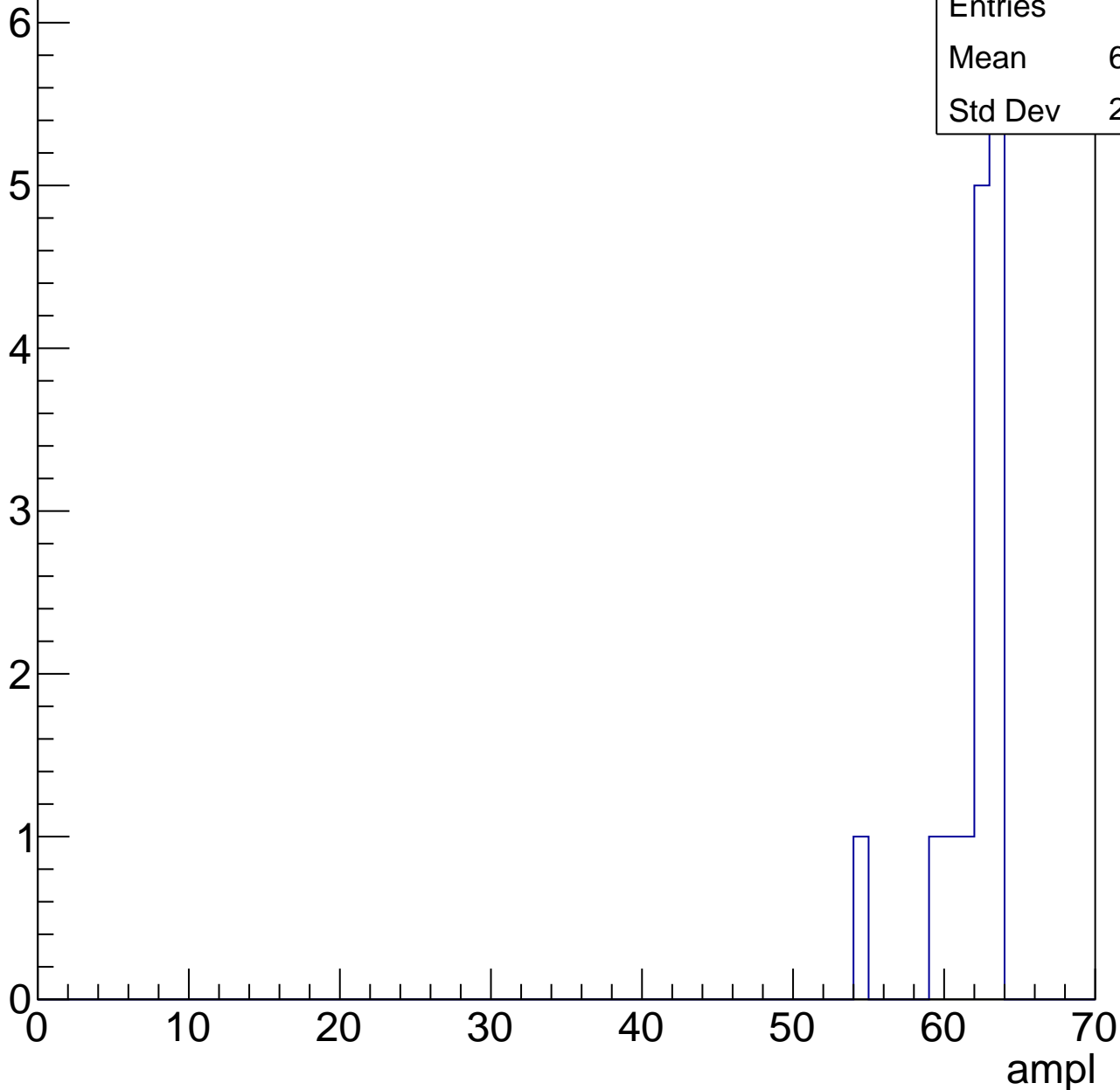


# B1L103S, U26-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	15
Mean	61.47
Std Dev	2.306

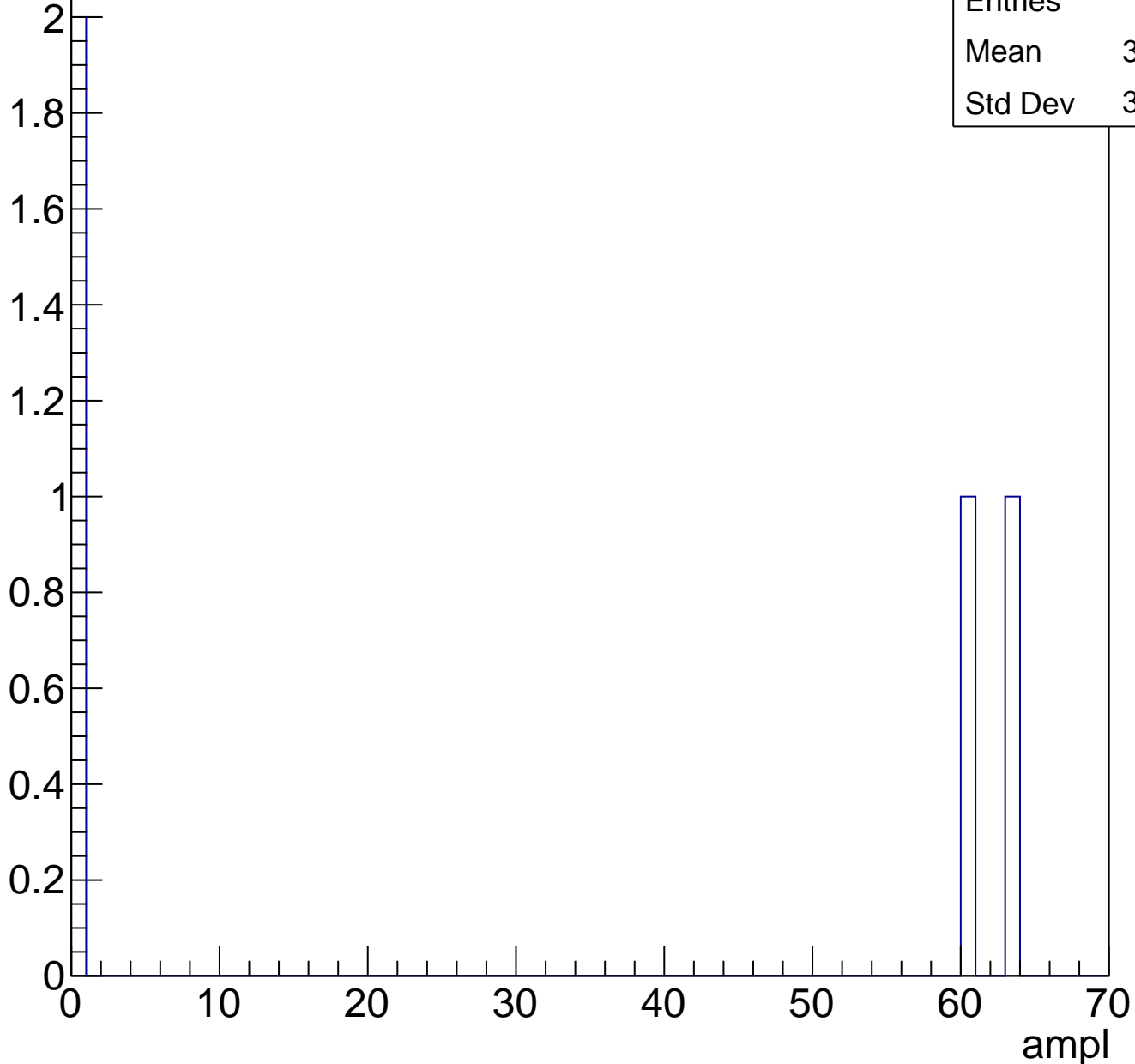




# B1L103S, U26-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	4
Mean	30.75
Std Dev	30.77

# B1L103S, U26-ch115, adc0

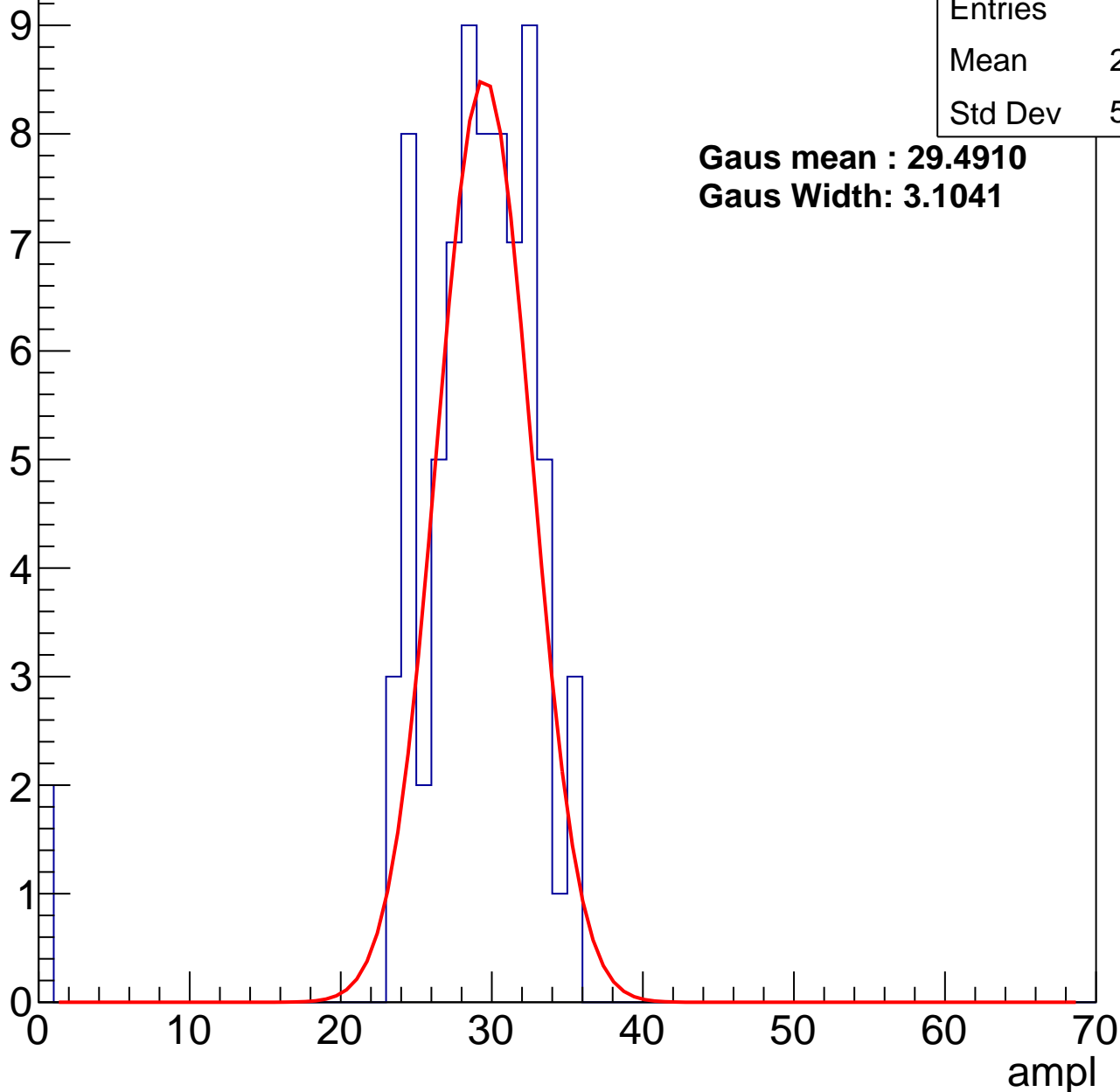
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	28.09
Std Dev	5.548

**Gaus mean : 29.4910**

**Gaus Width: 3.1041**



# B1L103S, U26-ch115, adc1

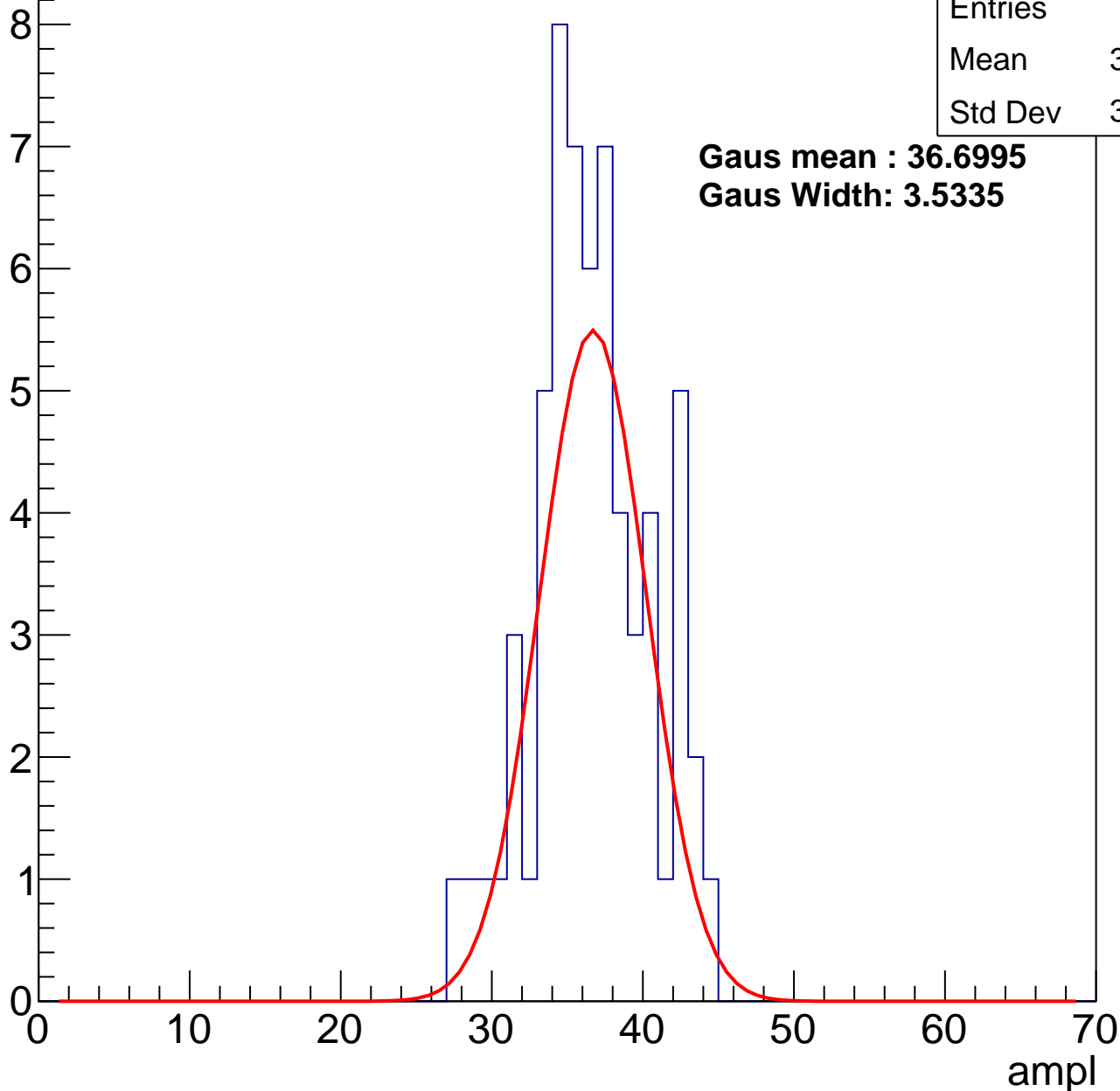
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	36.16
Std Dev	3.808

**Gaus mean : 36.6995**

**Gaus Width: 3.5335**



# B1L103S, U26-ch115, adc2

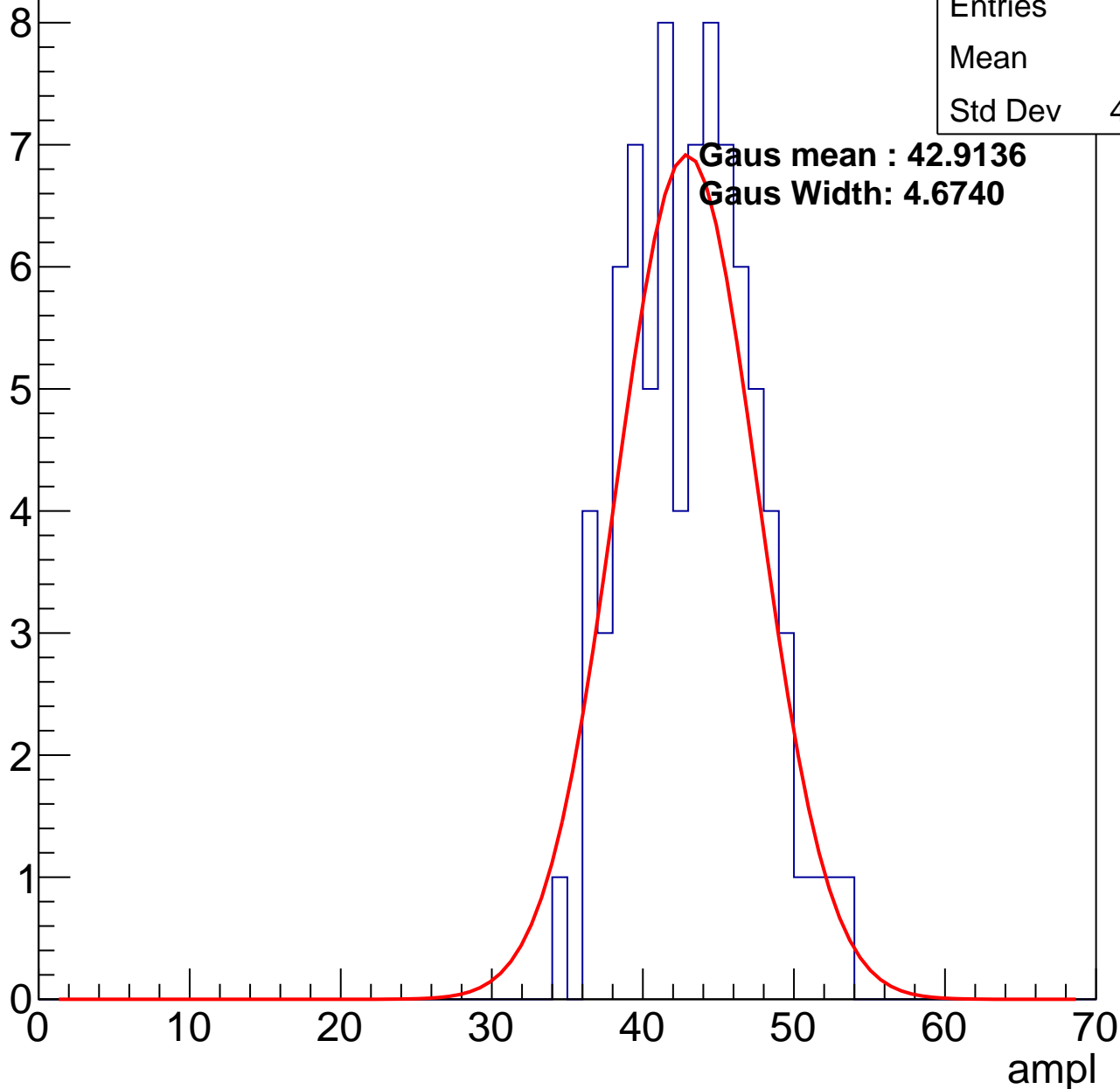
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	82
Mean	42.8
Std Dev	4.127

**Gaus mean : 42.9136**

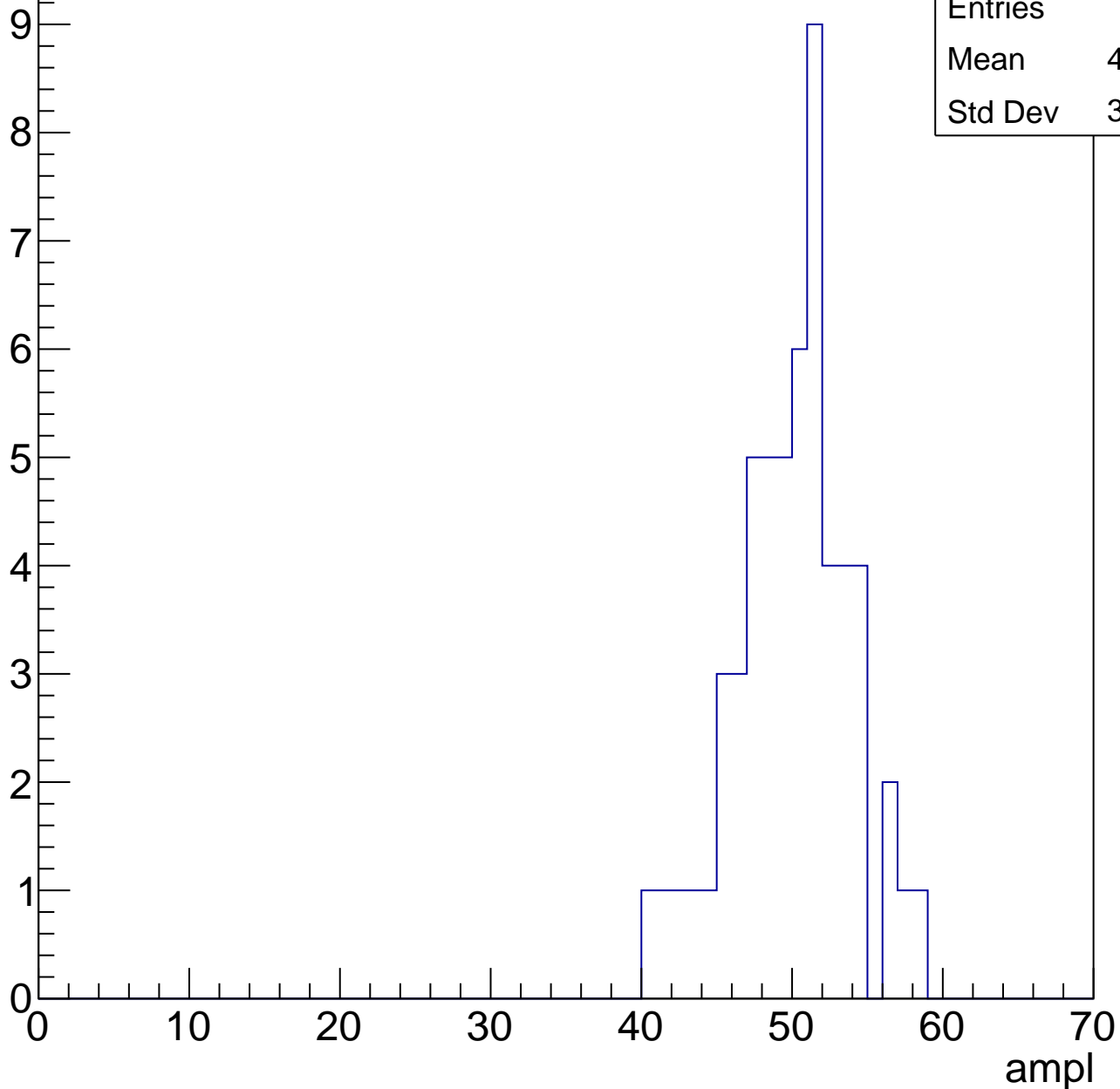
**Gaus Width: 4.6740**



# B1L103S, U26-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

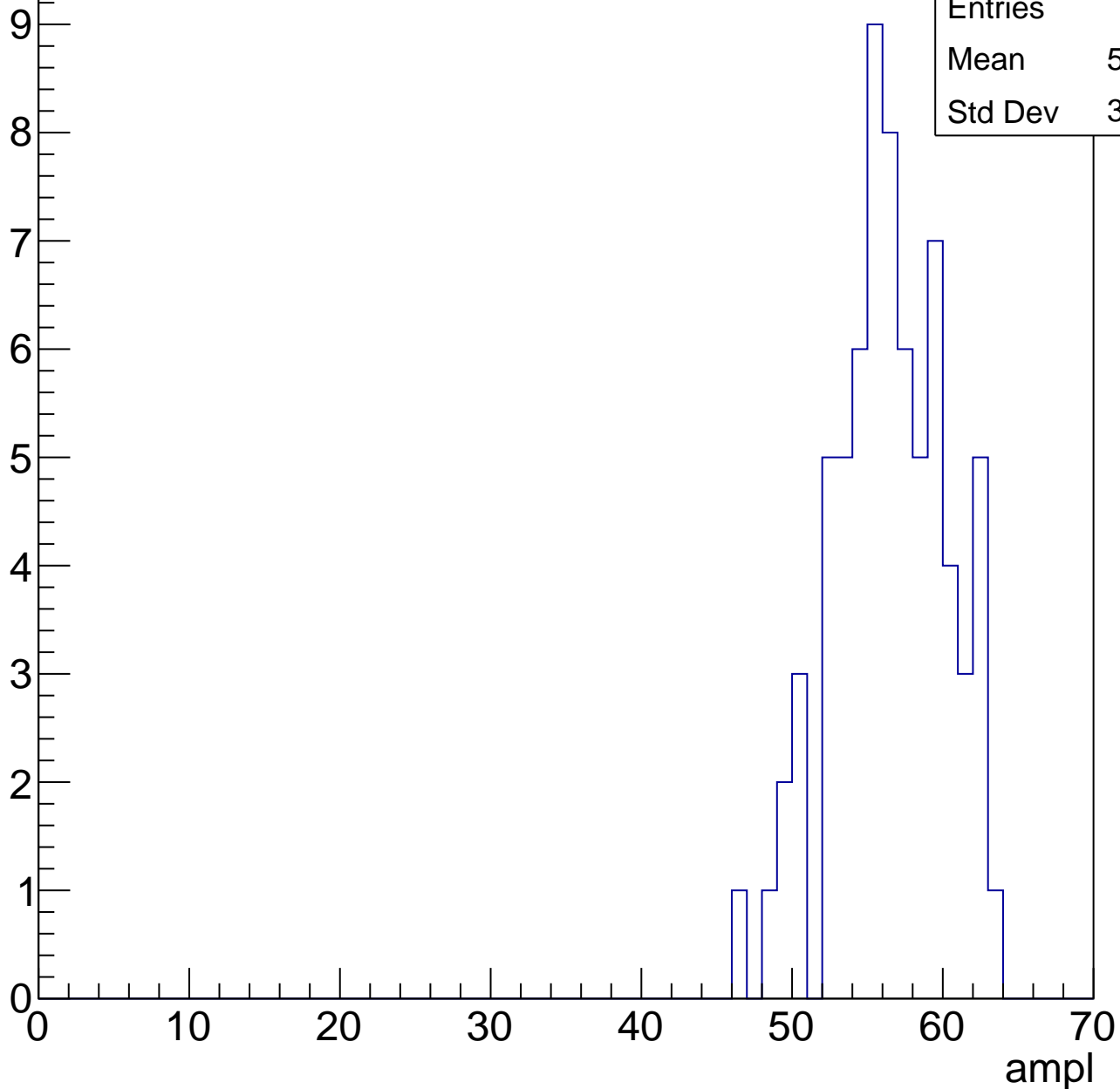


# B1L103S, U26-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	71
Mean	55.99
Std Dev	3.725

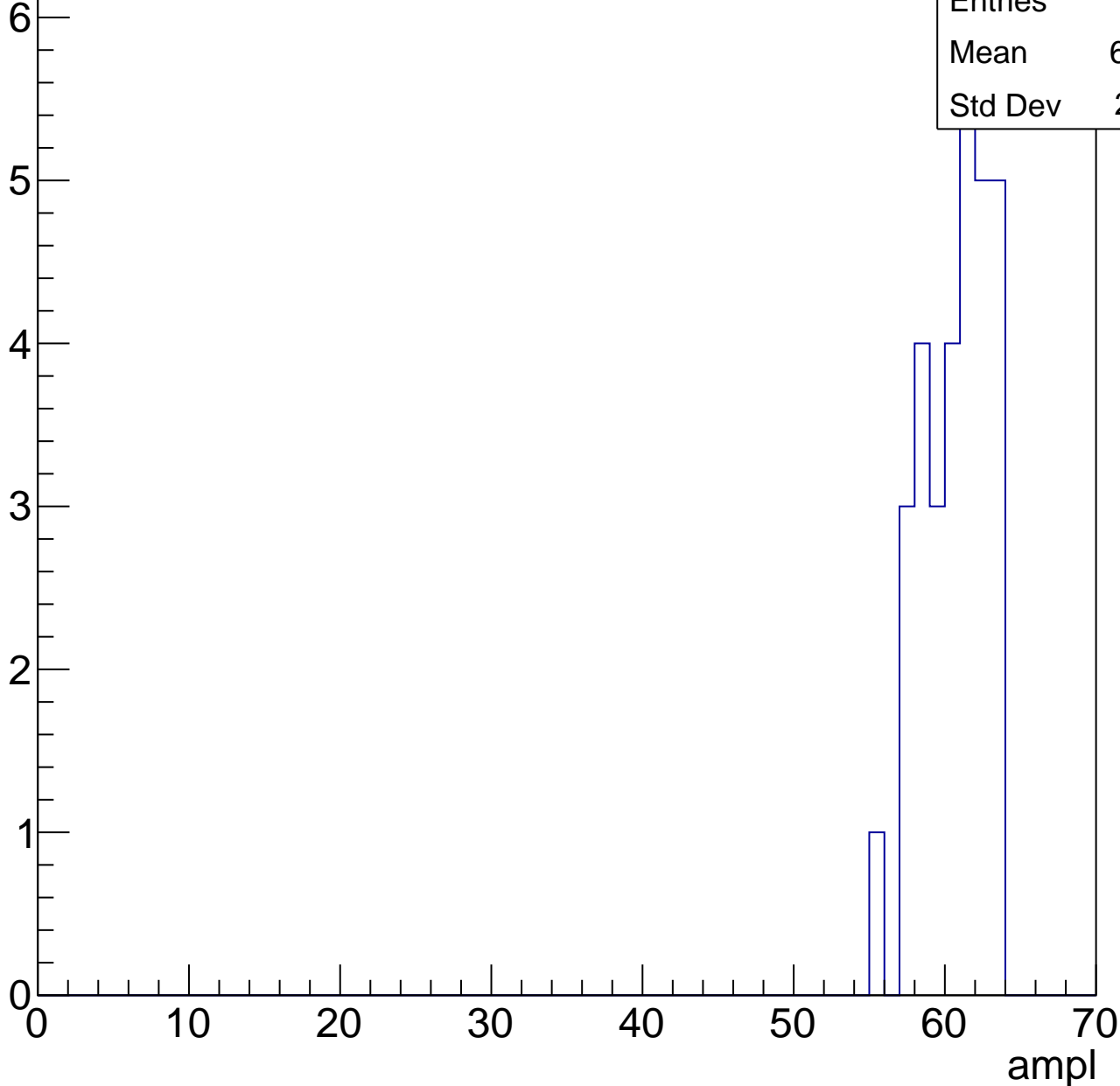


# B1L103S, U26-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

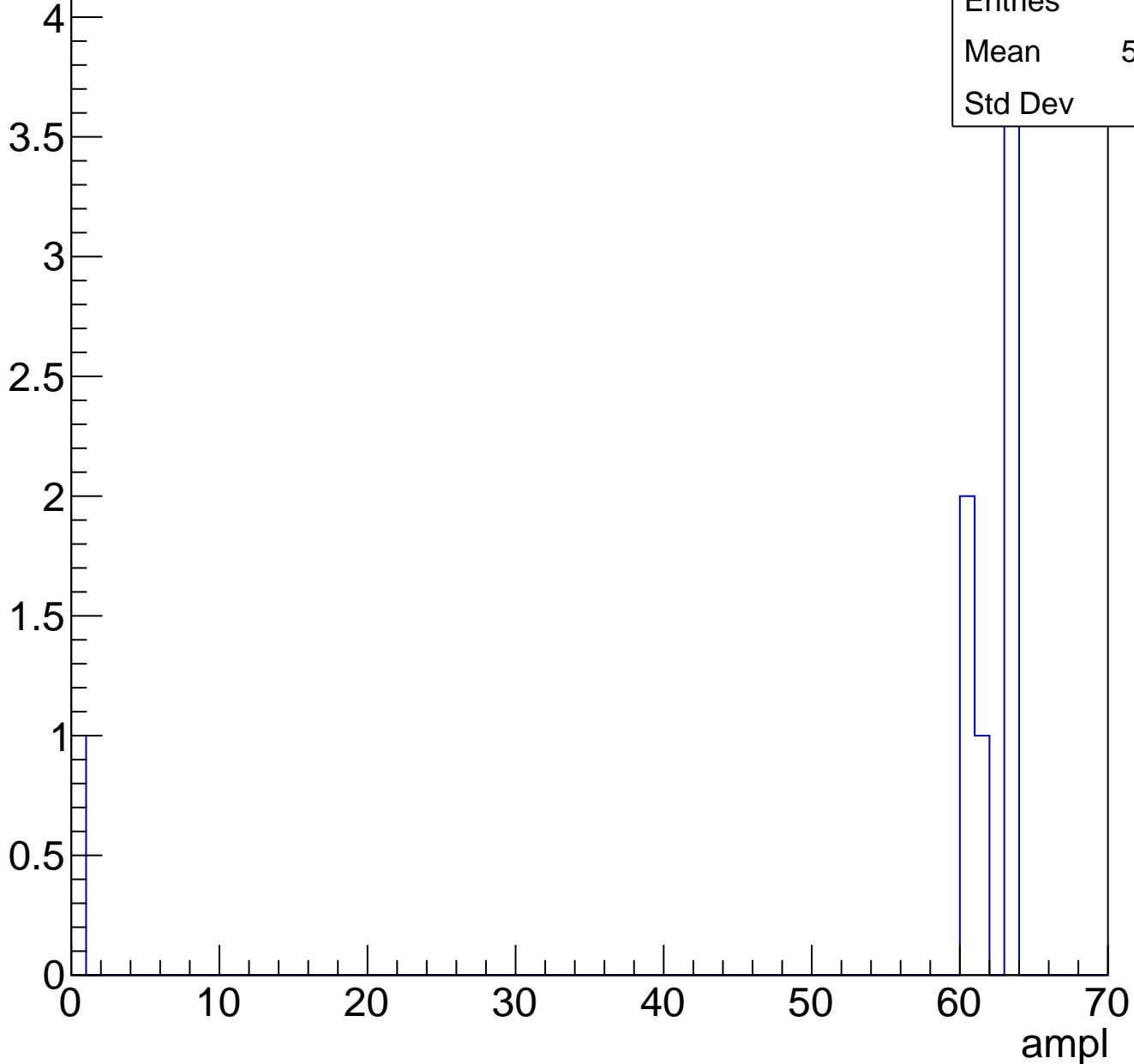
Entries	31
Mean	60.19
Std Dev	2.131



# B1L103S, U26-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	8
Mean	54.12
Std Dev	20.5



# B1L103S, U26-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch116, adc0

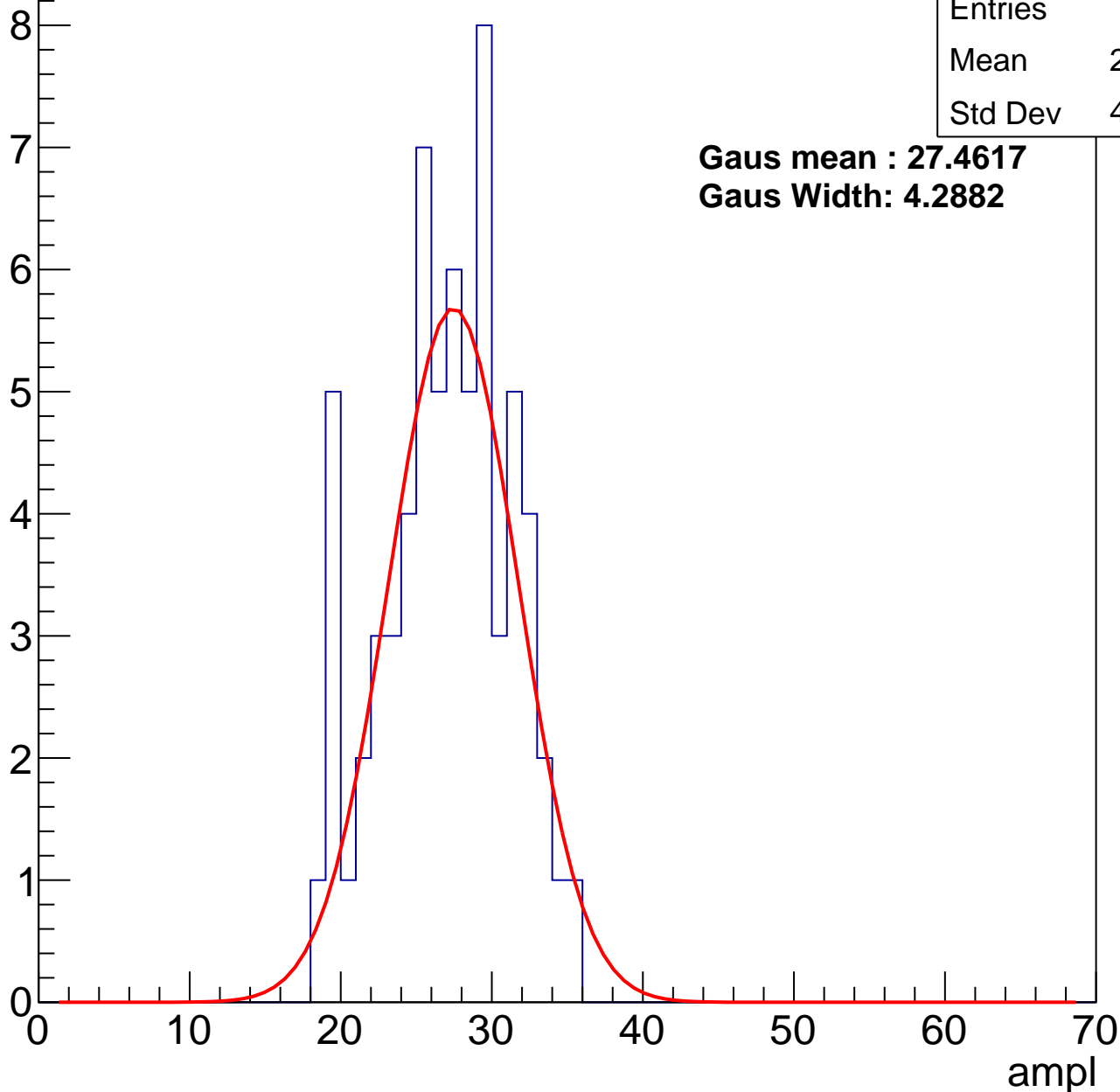
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	26.56
Std Dev	4.138

**Gaus mean : 27.4617**

**Gaus Width: 4.2882**



# B1L103S, U26-ch116, adc1

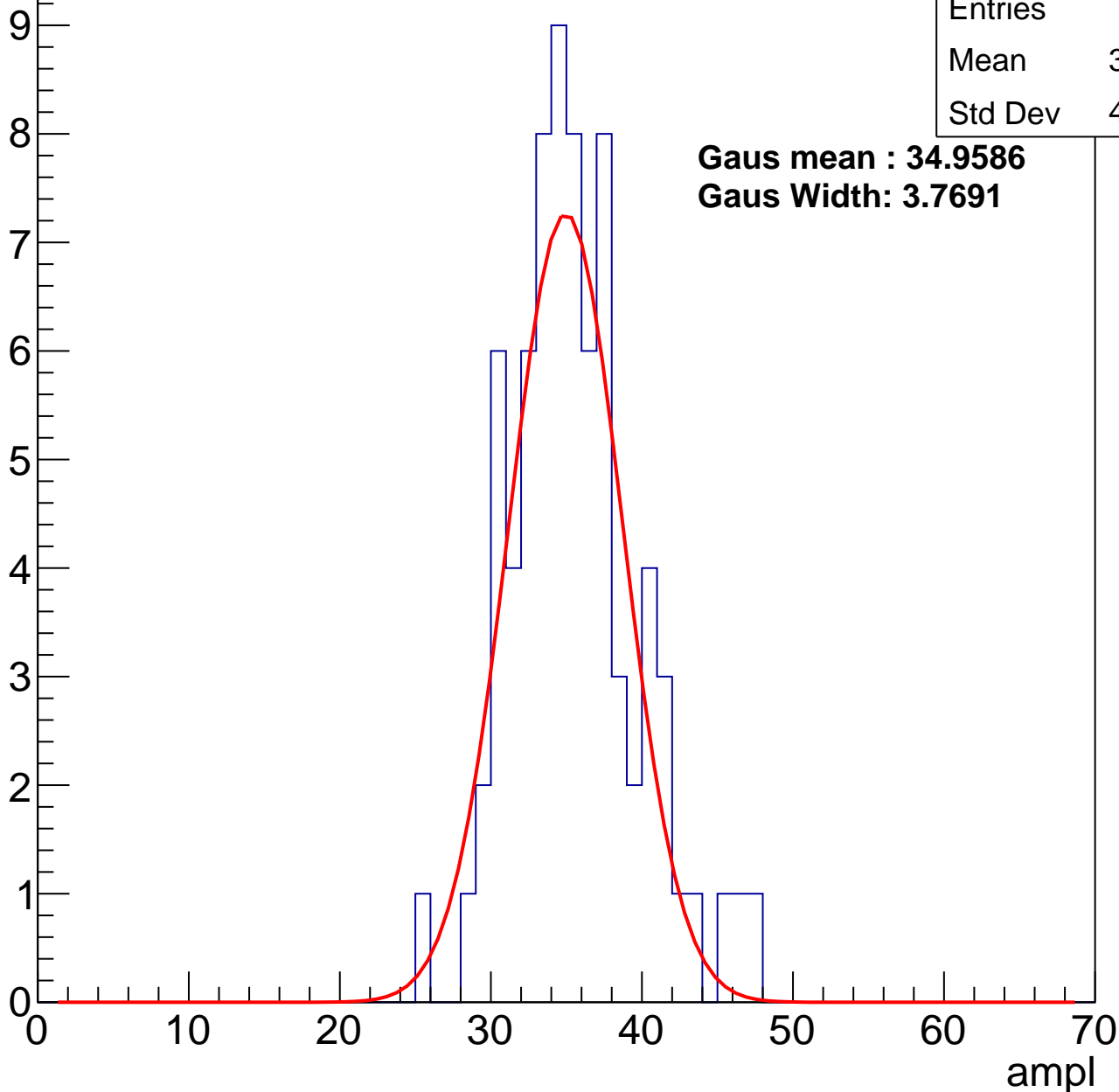
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	76
Mean	35.09
Std Dev	4.155

**Gaus mean : 34.9586**

**Gaus Width: 3.7691**



# B1L103S, U26-ch116, adc2

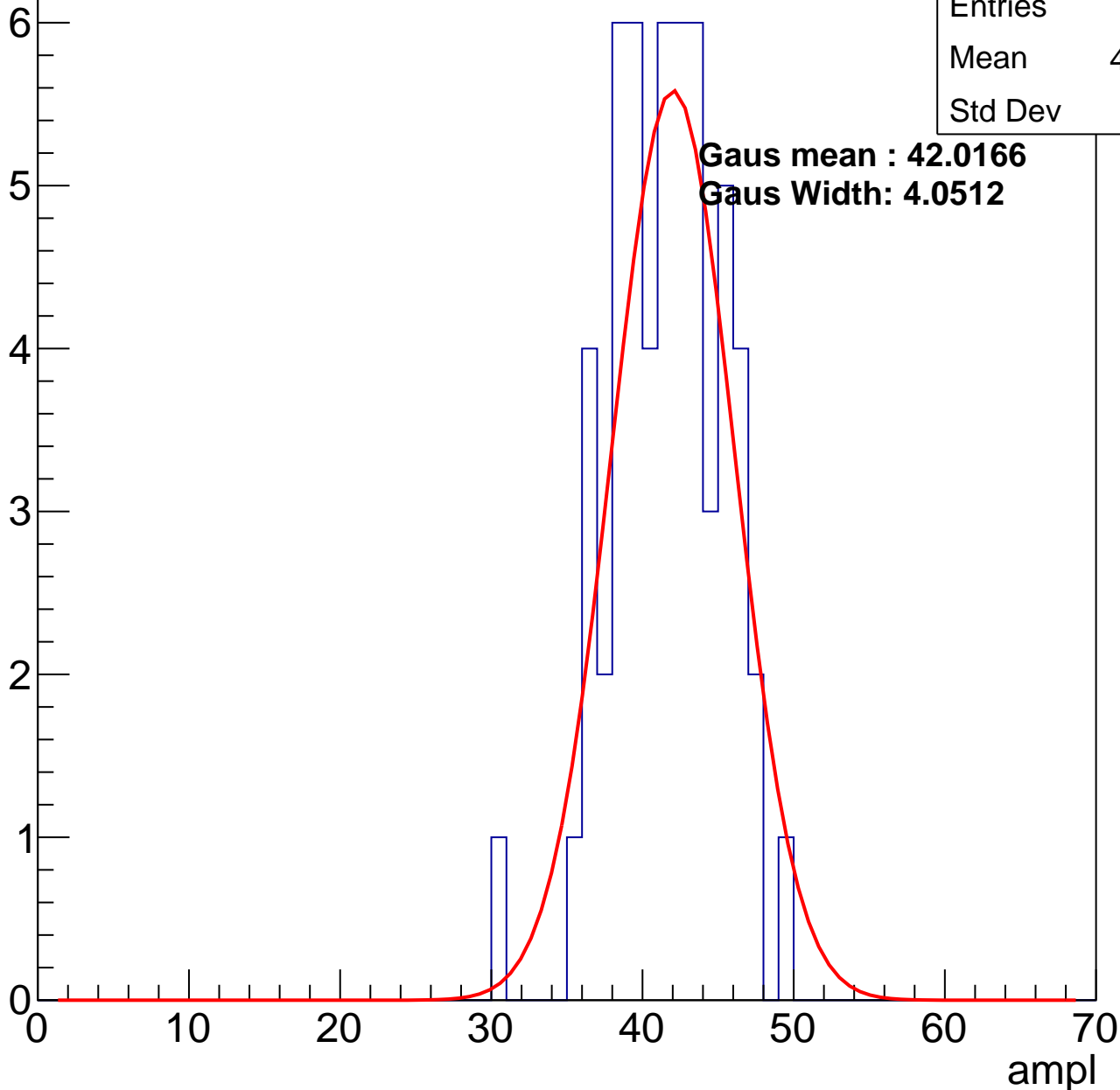
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	41.14
Std Dev	3.61

**Gaus mean : 42.0166**

**Gaus Width: 4.0512**

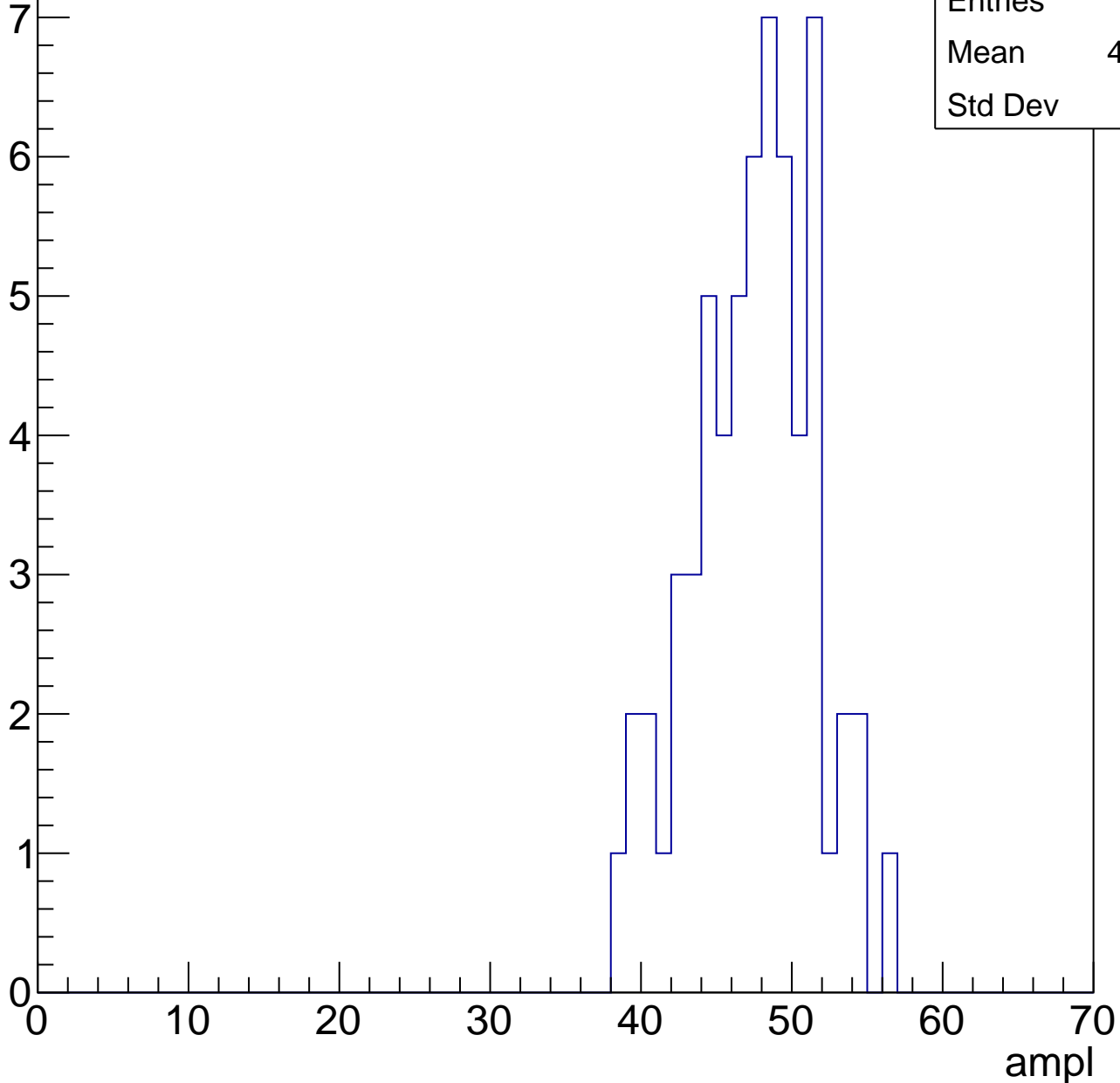


# B1L103S, U26-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

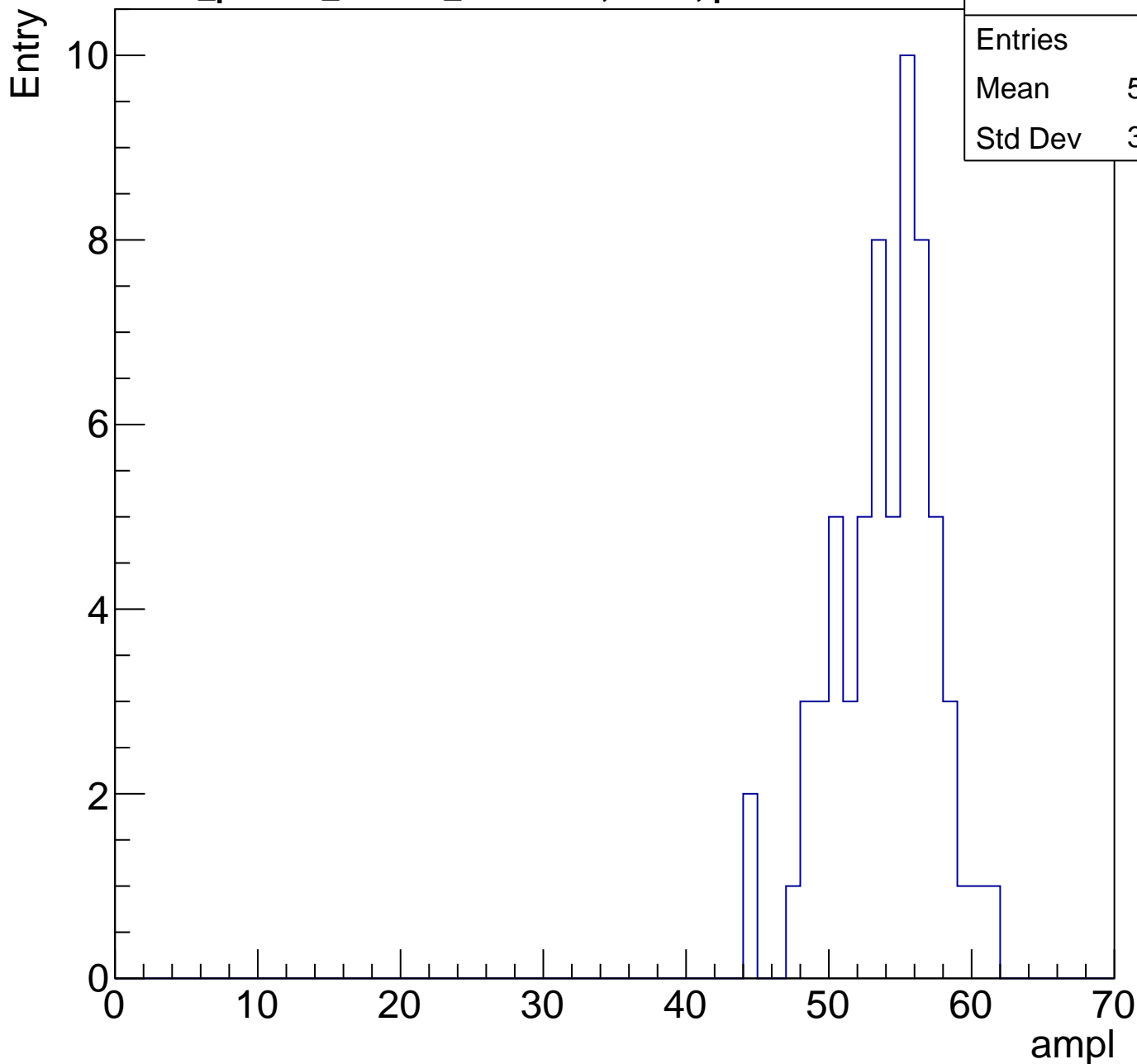
Entries	62
Mean	46.98
Std Dev	3.99



# B1L103S, U26-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	64
Mean	53.44
Std Dev	3.517

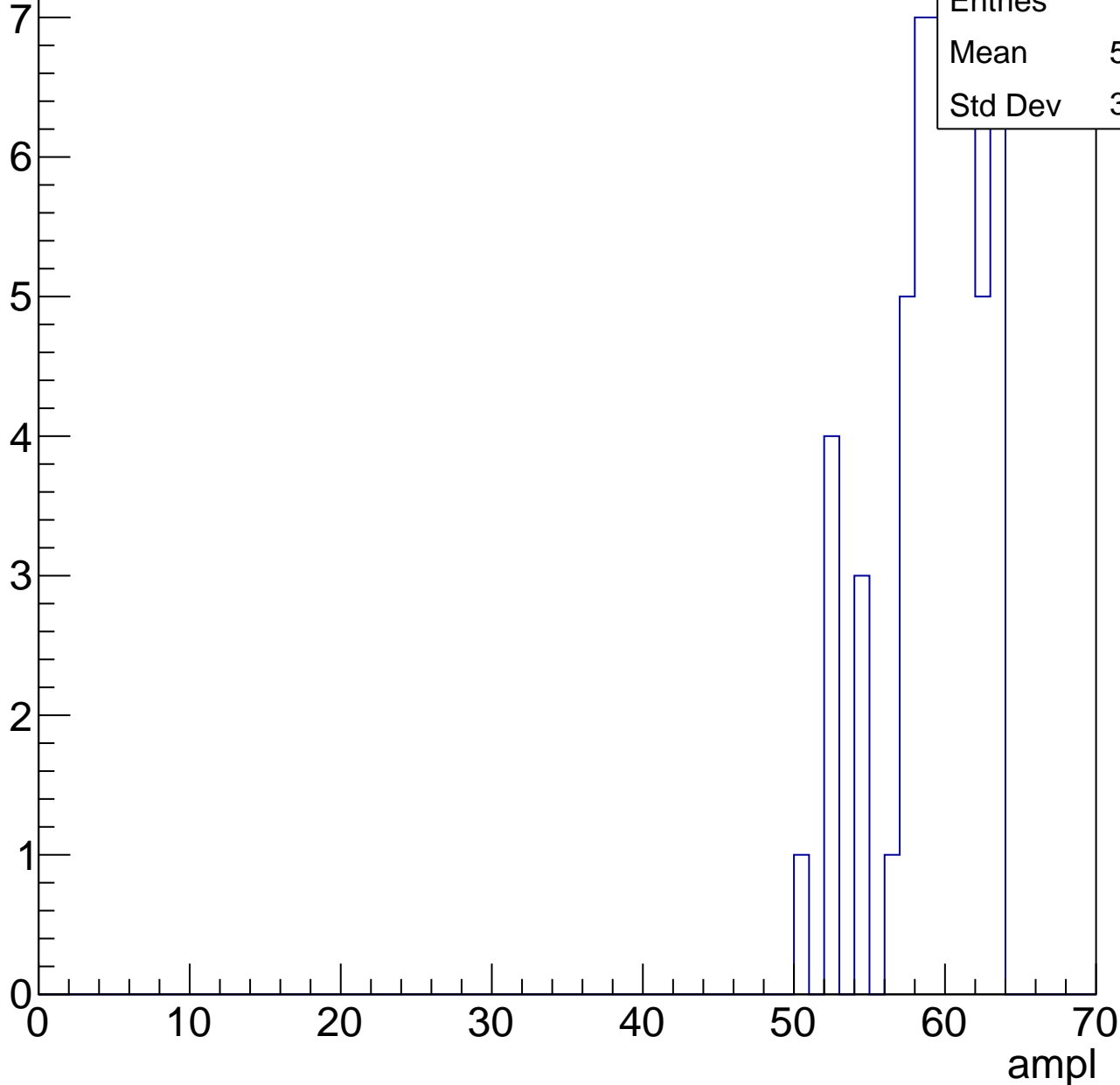


# B1L103S, U26-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

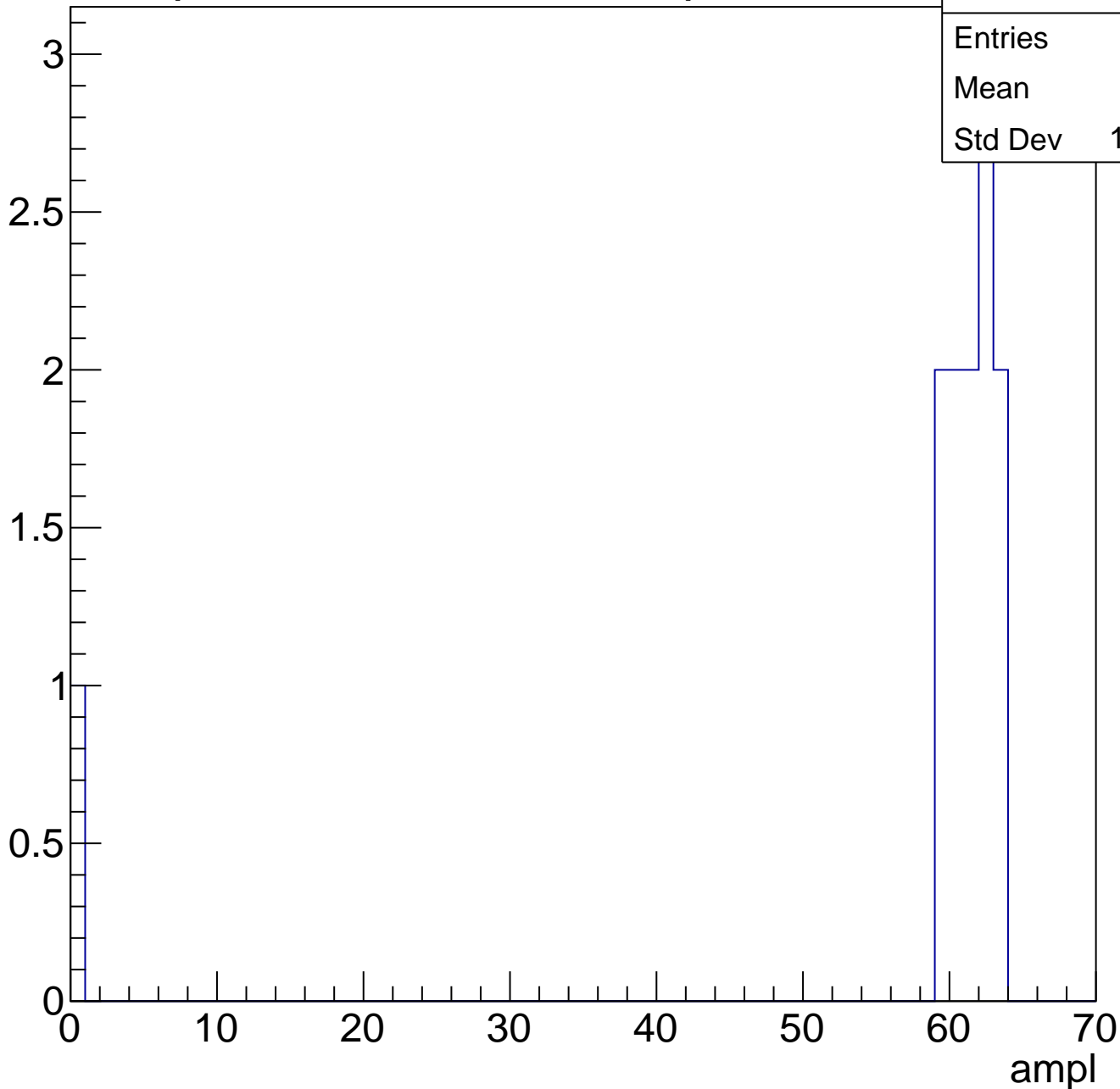
Entries	54
Mean	58.85
Std Dev	3.274



# B1L103S, U26-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



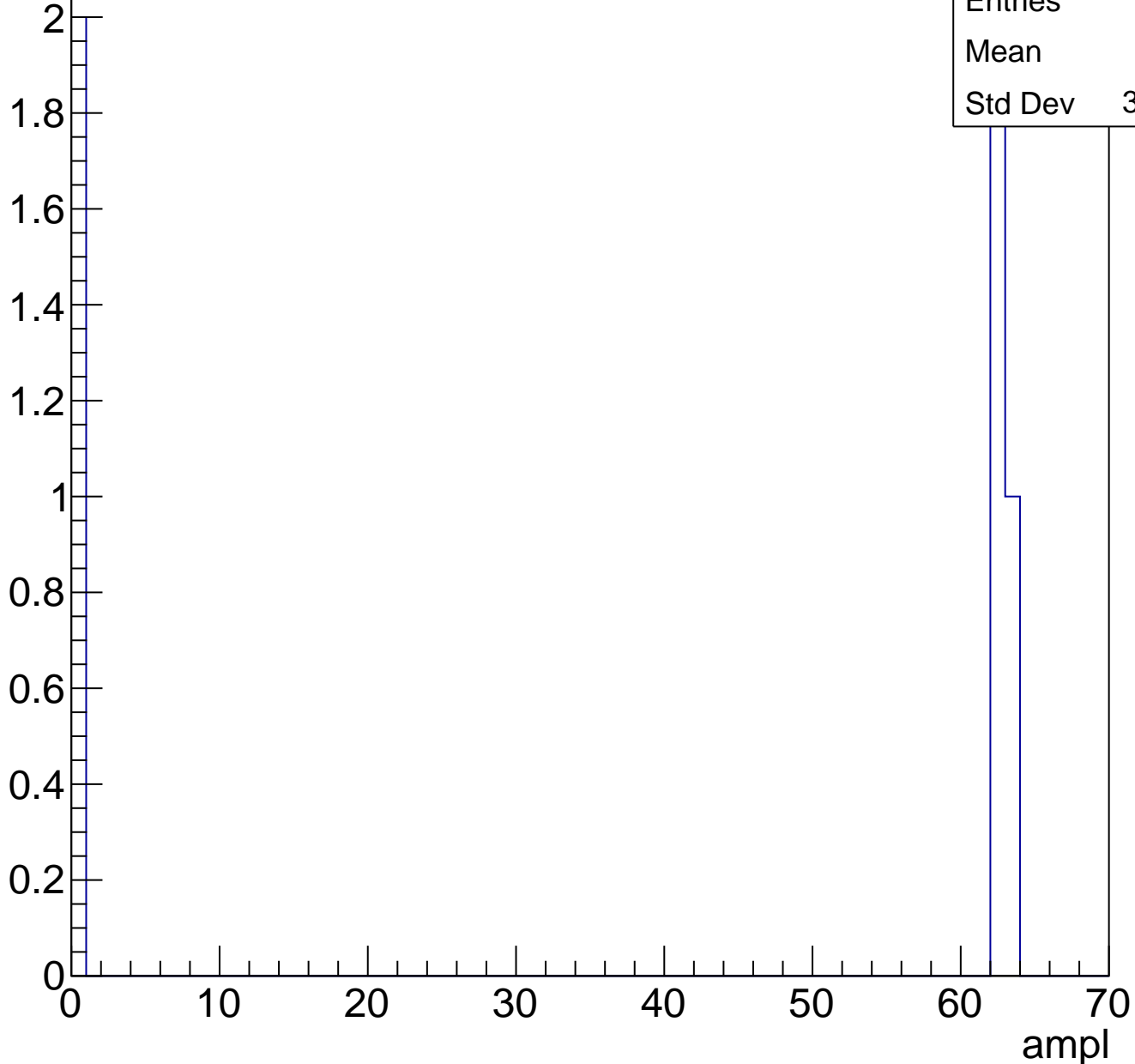
Entries	12
Mean	56
Std Dev	16.94



# B1L103S, U26-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch117, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	93
Mean	30.03
Std Dev	5.667

**Gaus mean : 30.7225**

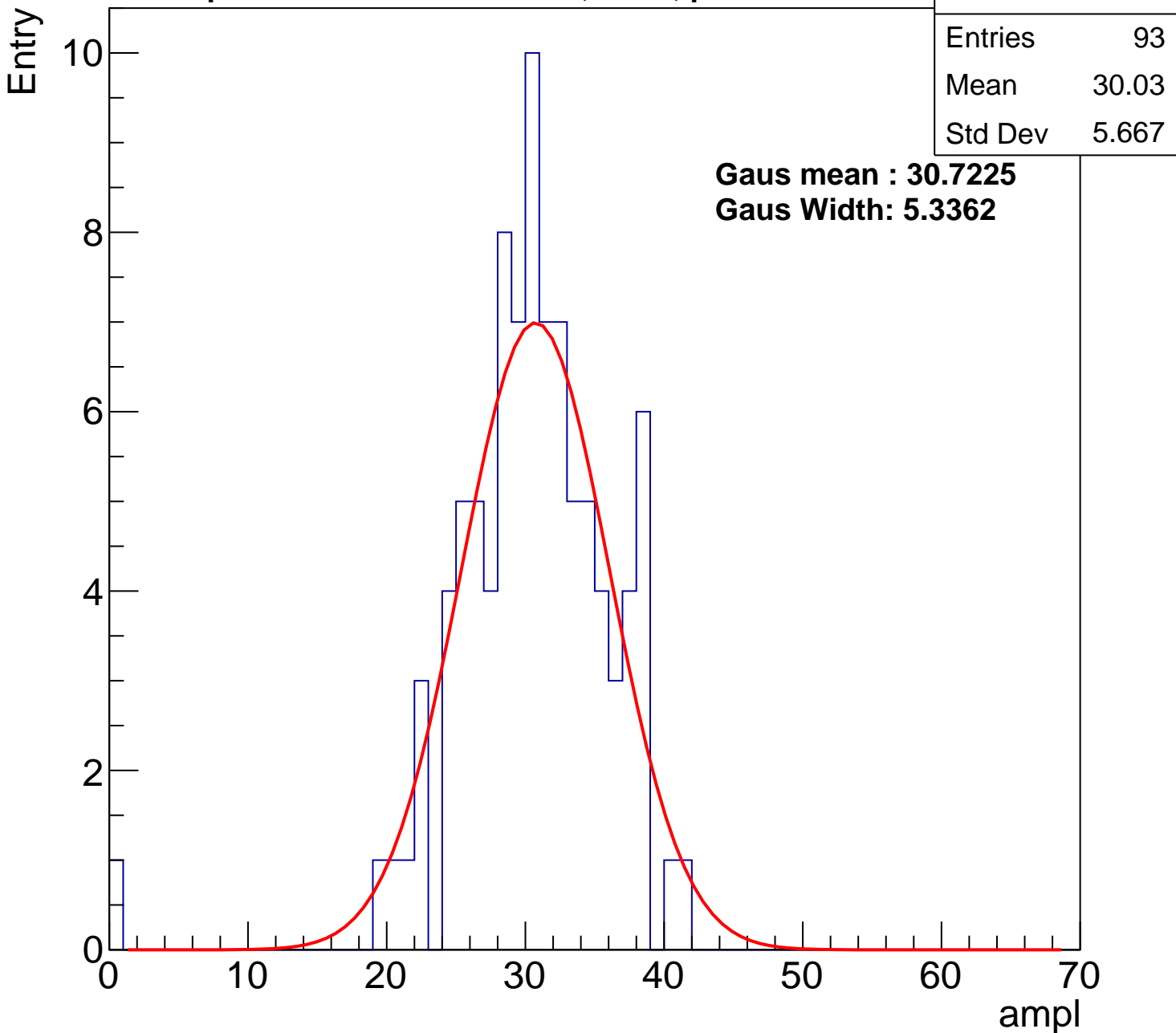
**Gaus Width: 5.3362**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch117, adc1

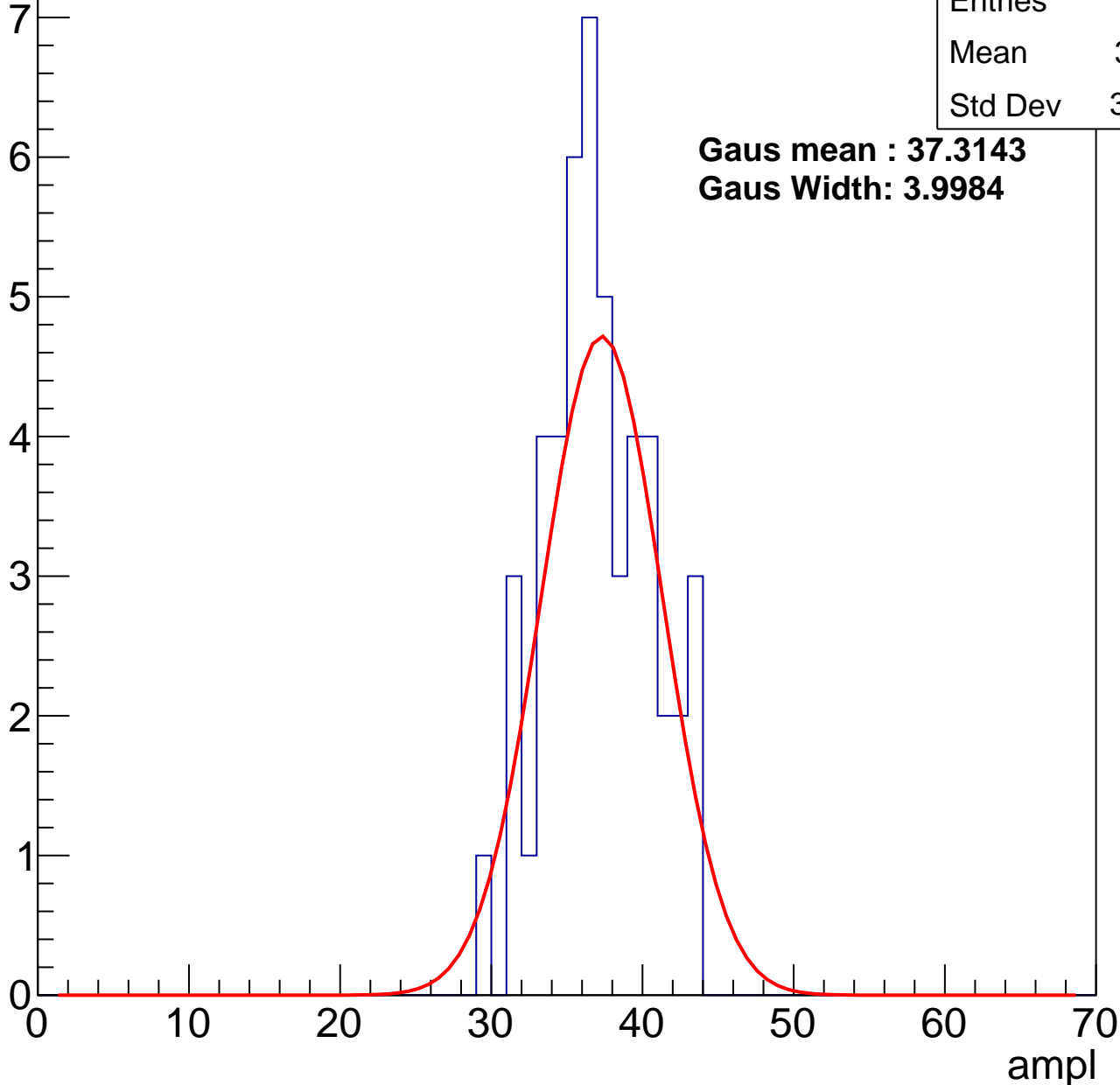
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	49
Mean	36.61
Std Dev	3.398

**Gaus mean : 37.3143**

**Gaus Width: 3.9984**



# B1L103S, U26-ch117, adc2

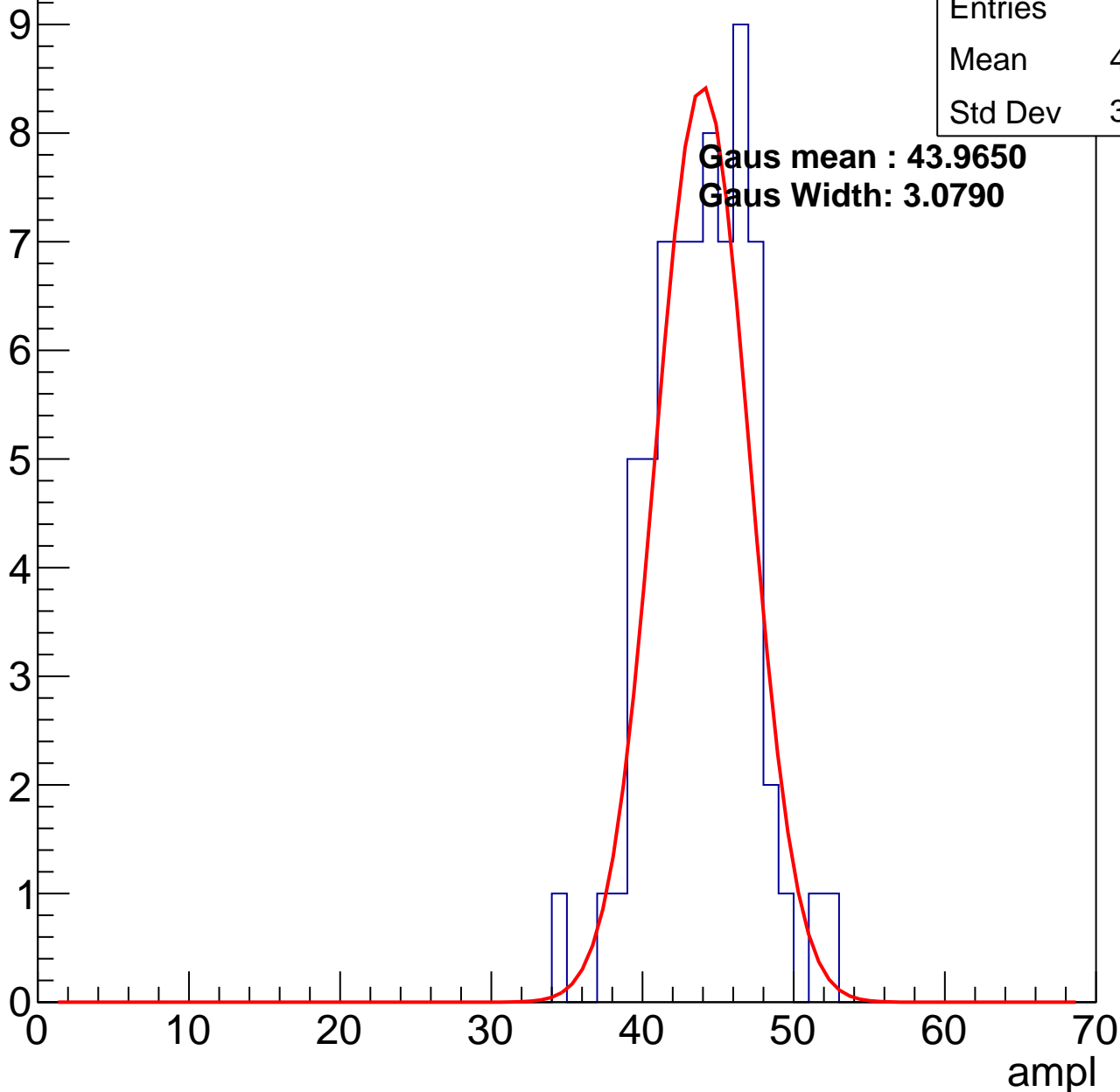
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	43.49
Std Dev	3.263

**Gaus mean : 43.9650**

**Gaus Width: 3.0790**

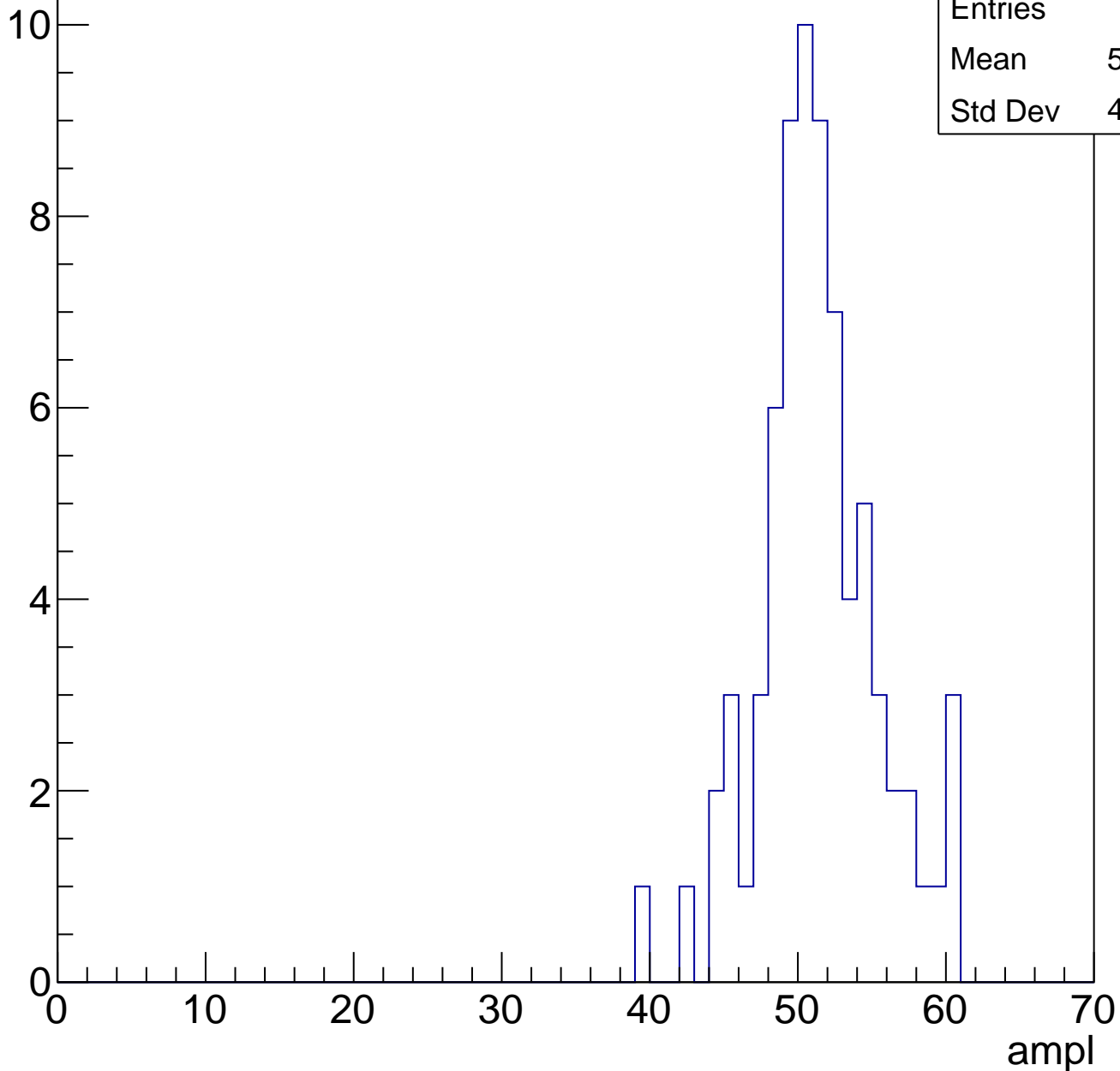


# B1L103S, U26-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entries	73
Mean	50.86
Std Dev	4.049

Entry

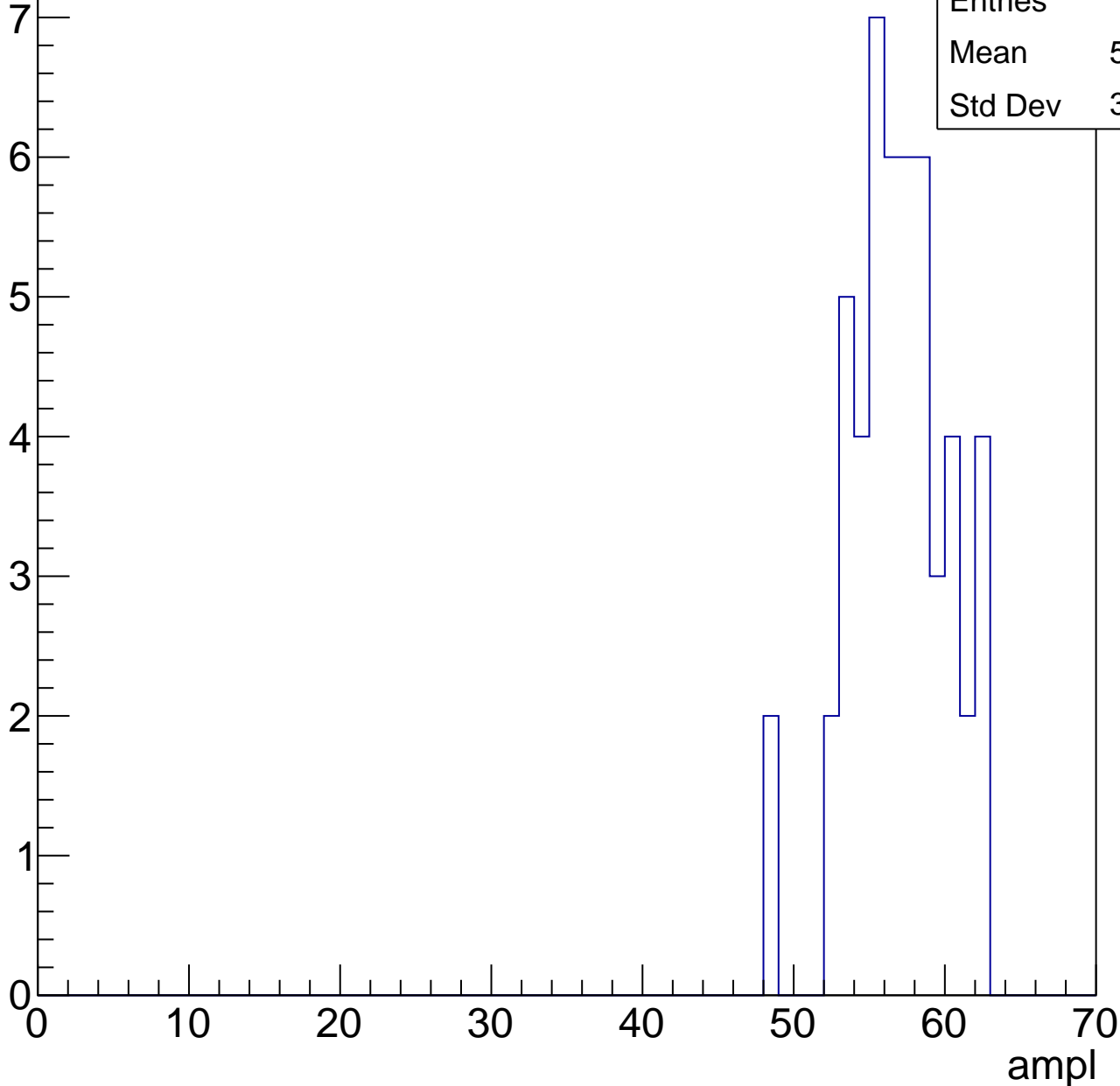


# B1L103S, U26-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	56.45
Std Dev	3.232

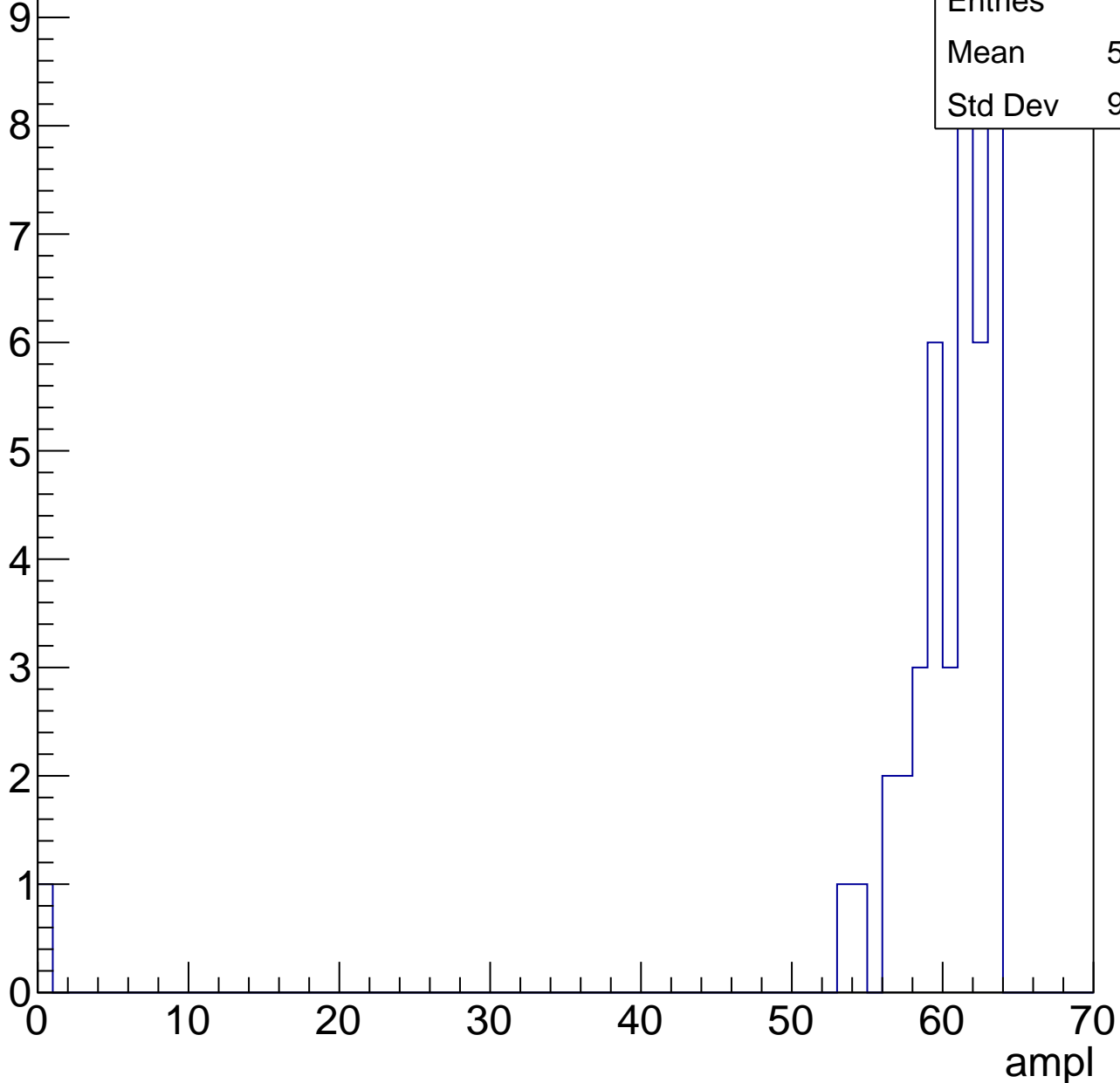


# B1L103S, U26-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	42
Mean	58.76
Std Dev	9.514



# B1L103S, U26-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch118, adc0

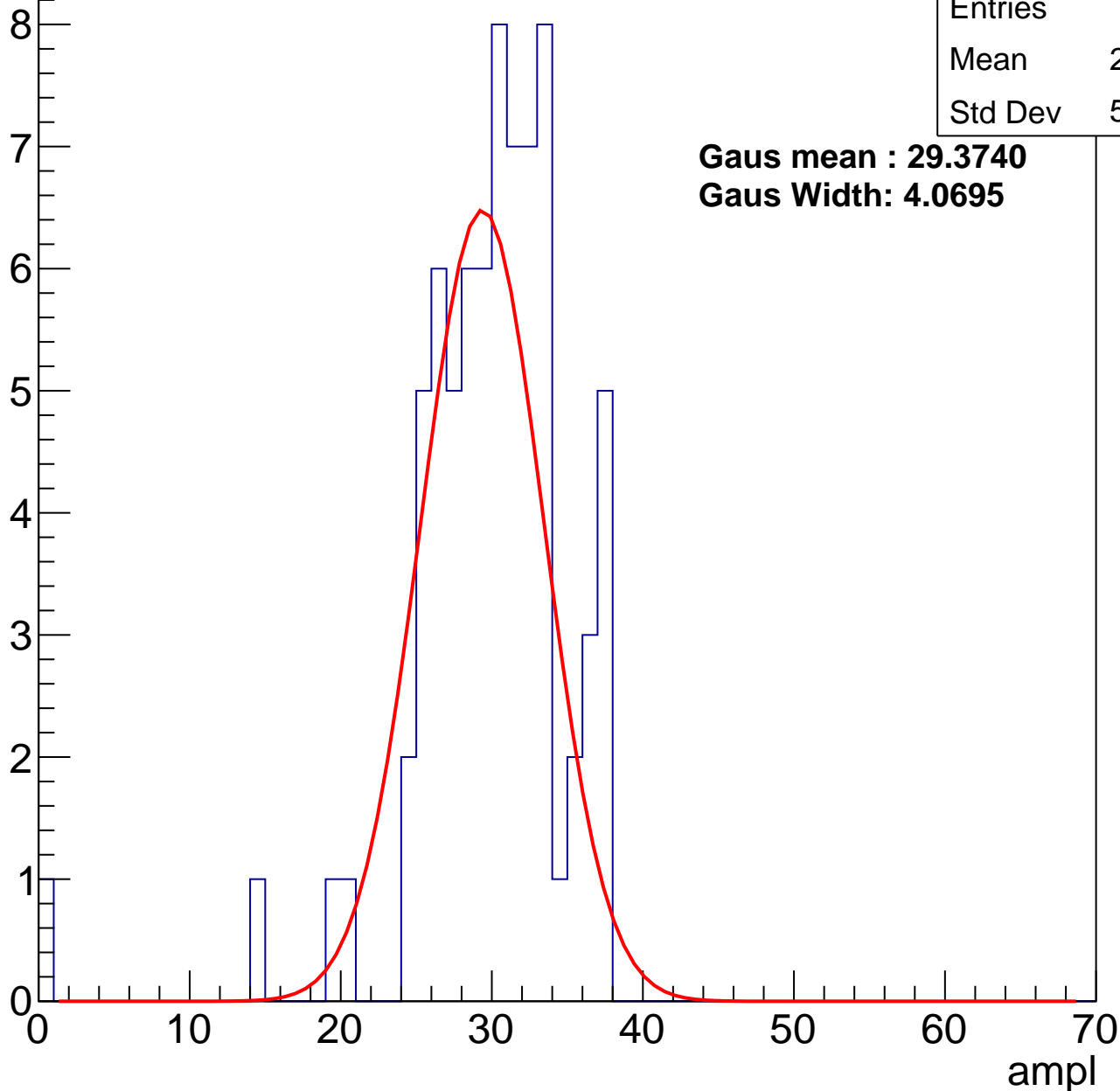
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	29.35
Std Dev	5.464

**Gaus mean : 29.3740**

**Gaus Width: 4.0695**



# B1L103S, U26-ch118, adc1

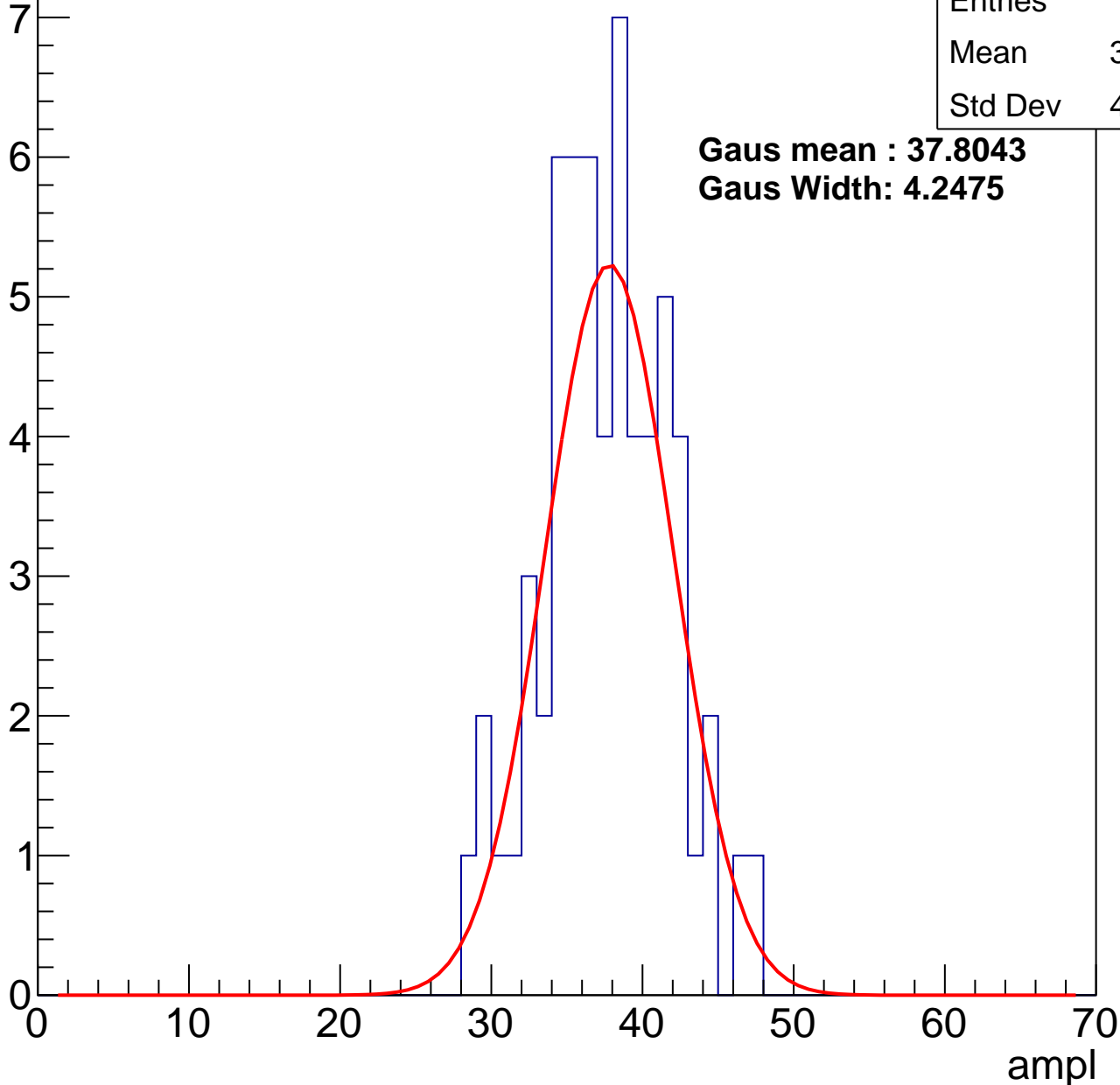
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	61
Mean	37.15
Std Dev	4.124

**Gaus mean : 37.8043**

**Gaus Width: 4.2475**

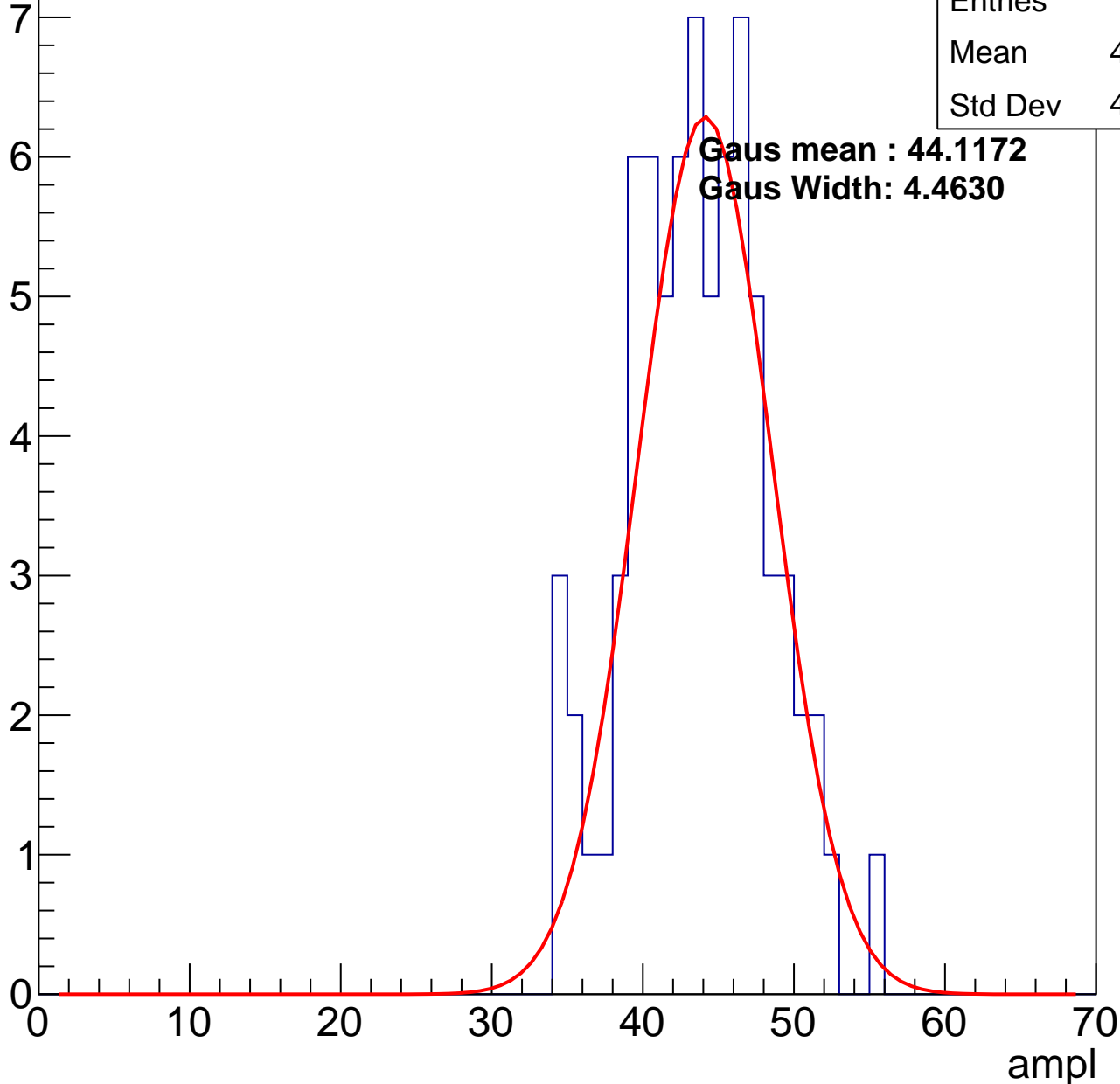


# B1L103S, U26-ch118, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	43.17
Std Dev	4.488

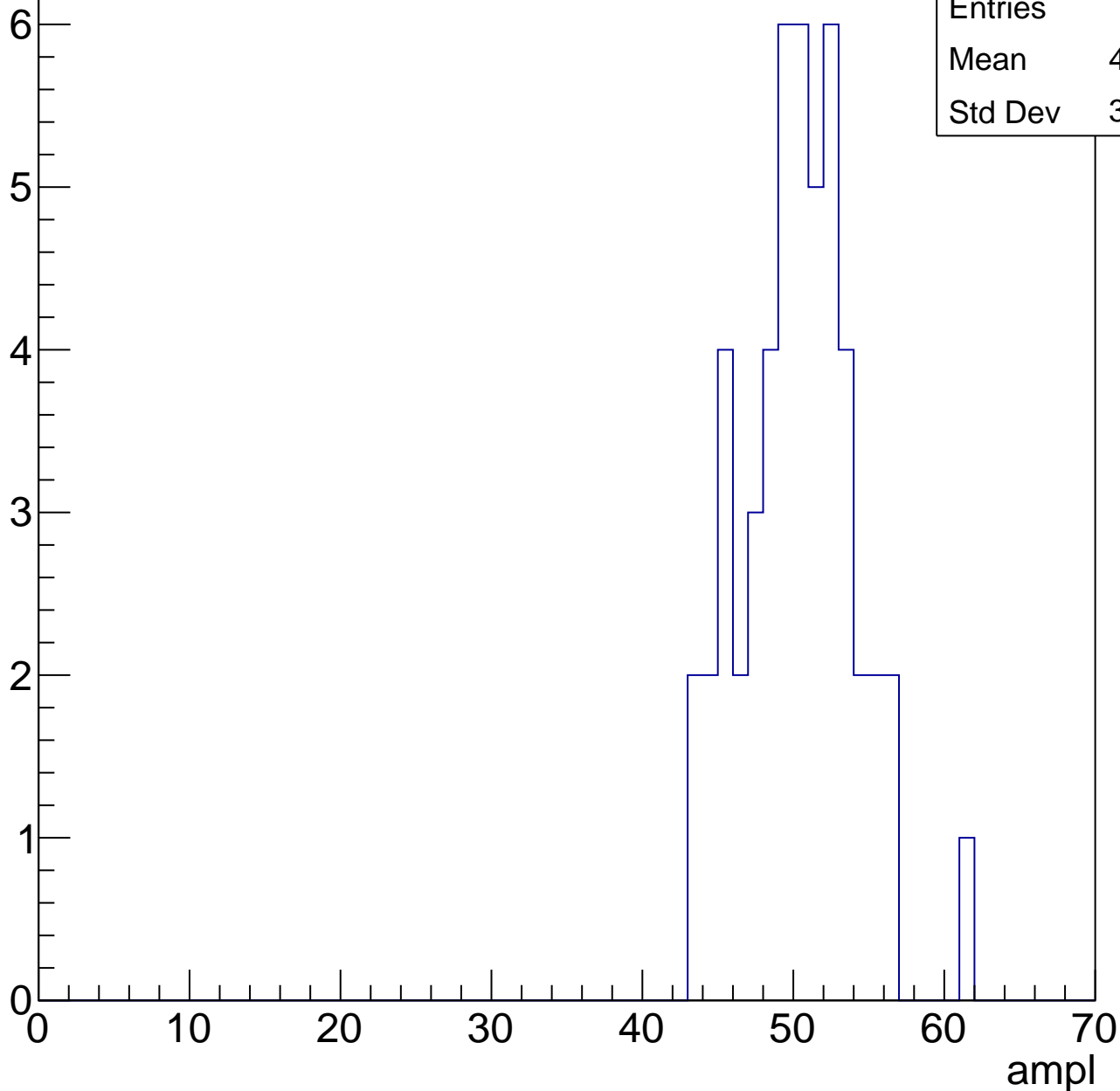


# B1L103S, U26-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	49.86
Std Dev	3.678

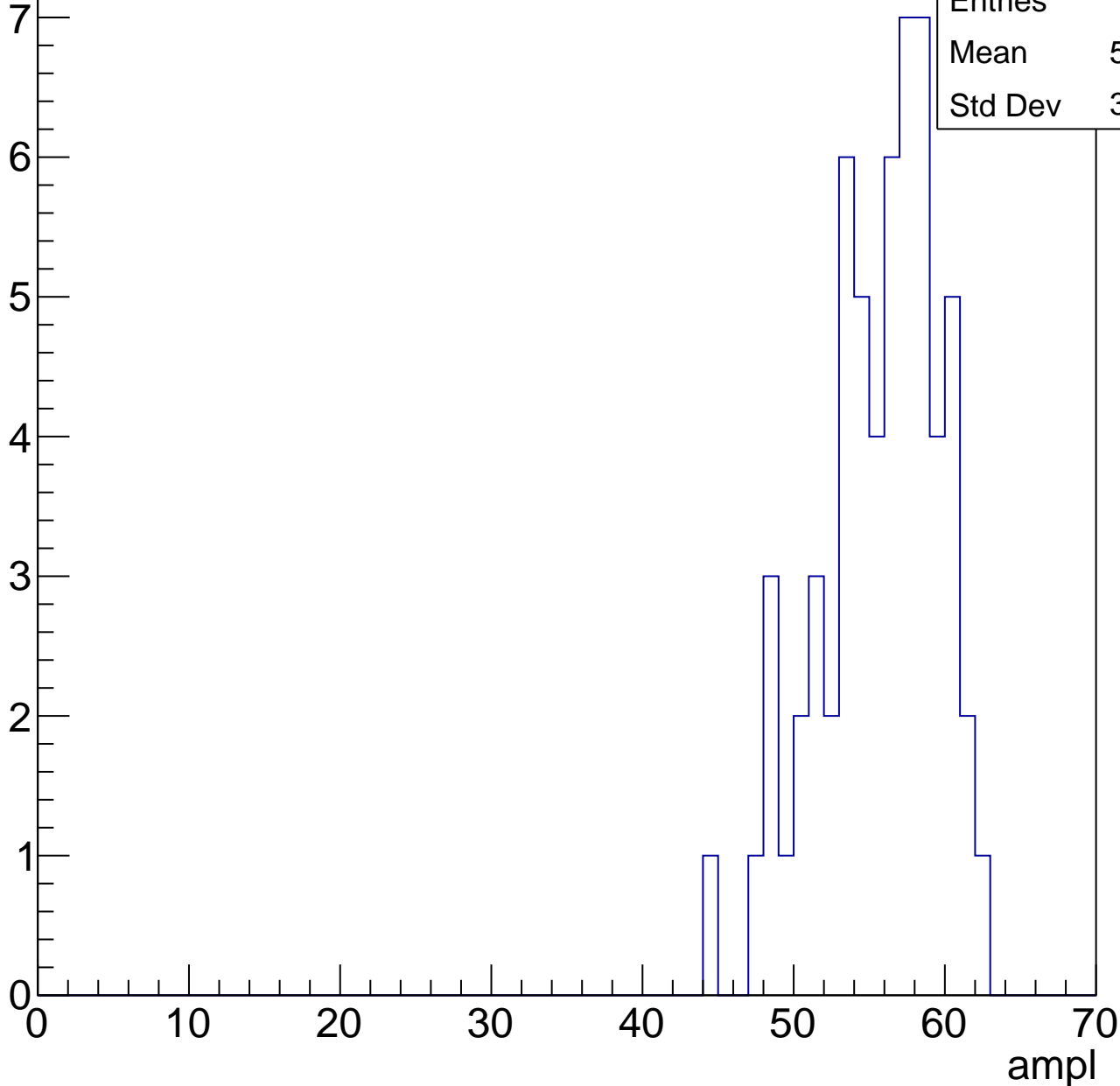


# B1L103S, U26-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	55.17
Std Dev	3.912

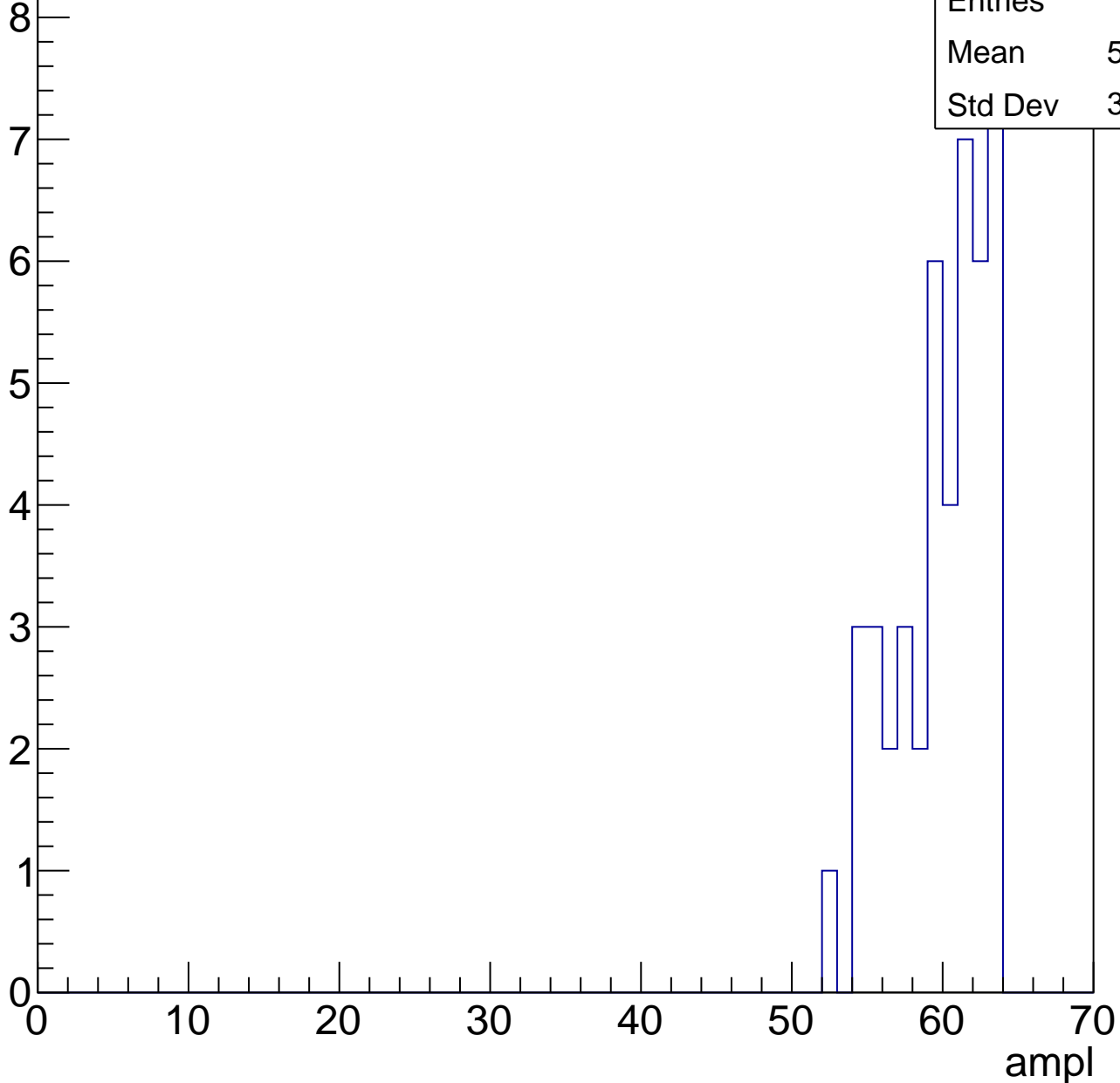


# B1L103S, U26-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

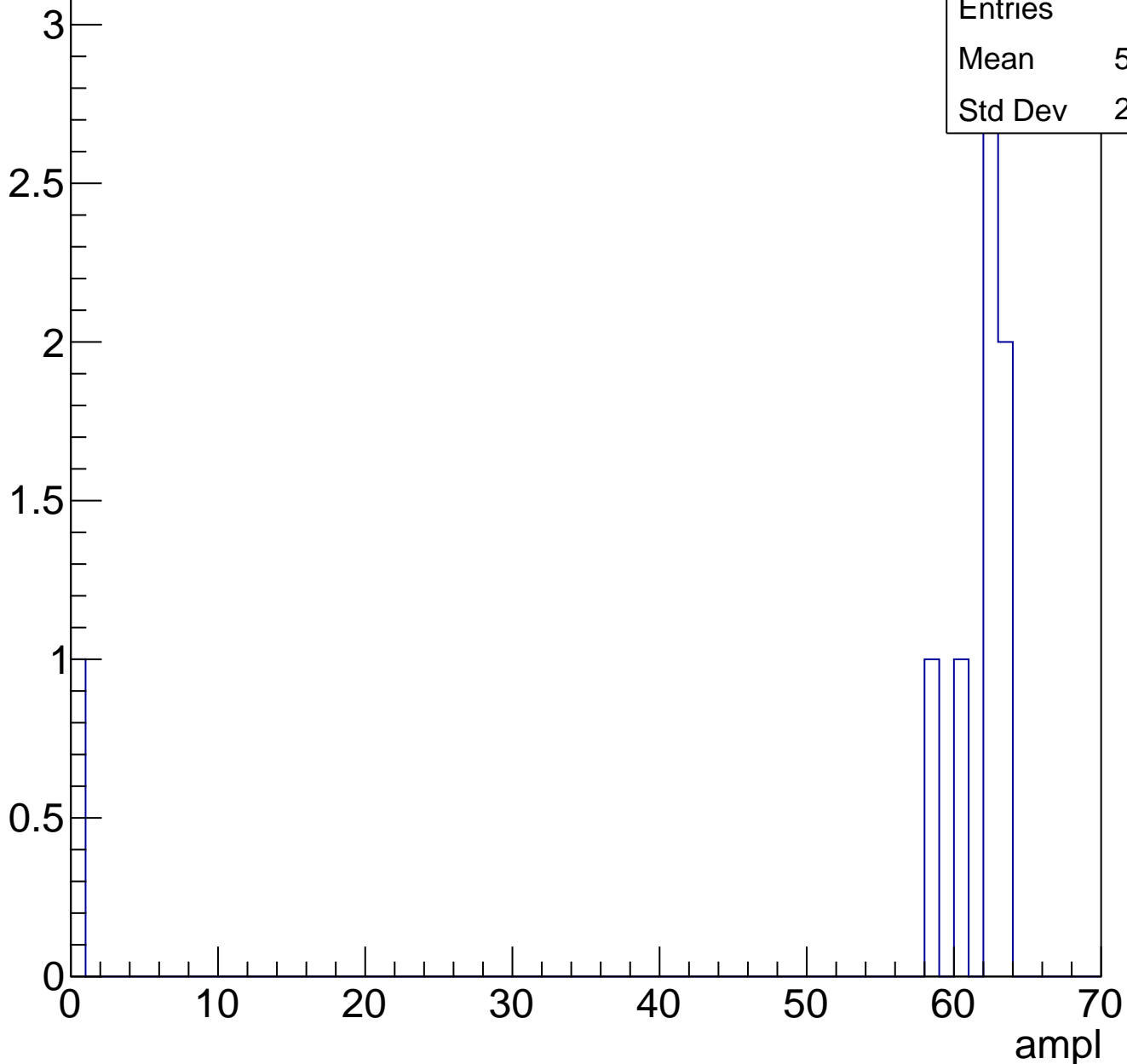
Entries	45
Mean	59.44
Std Dev	3.015



# B1L103S, U26-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U26-ch119, adc0

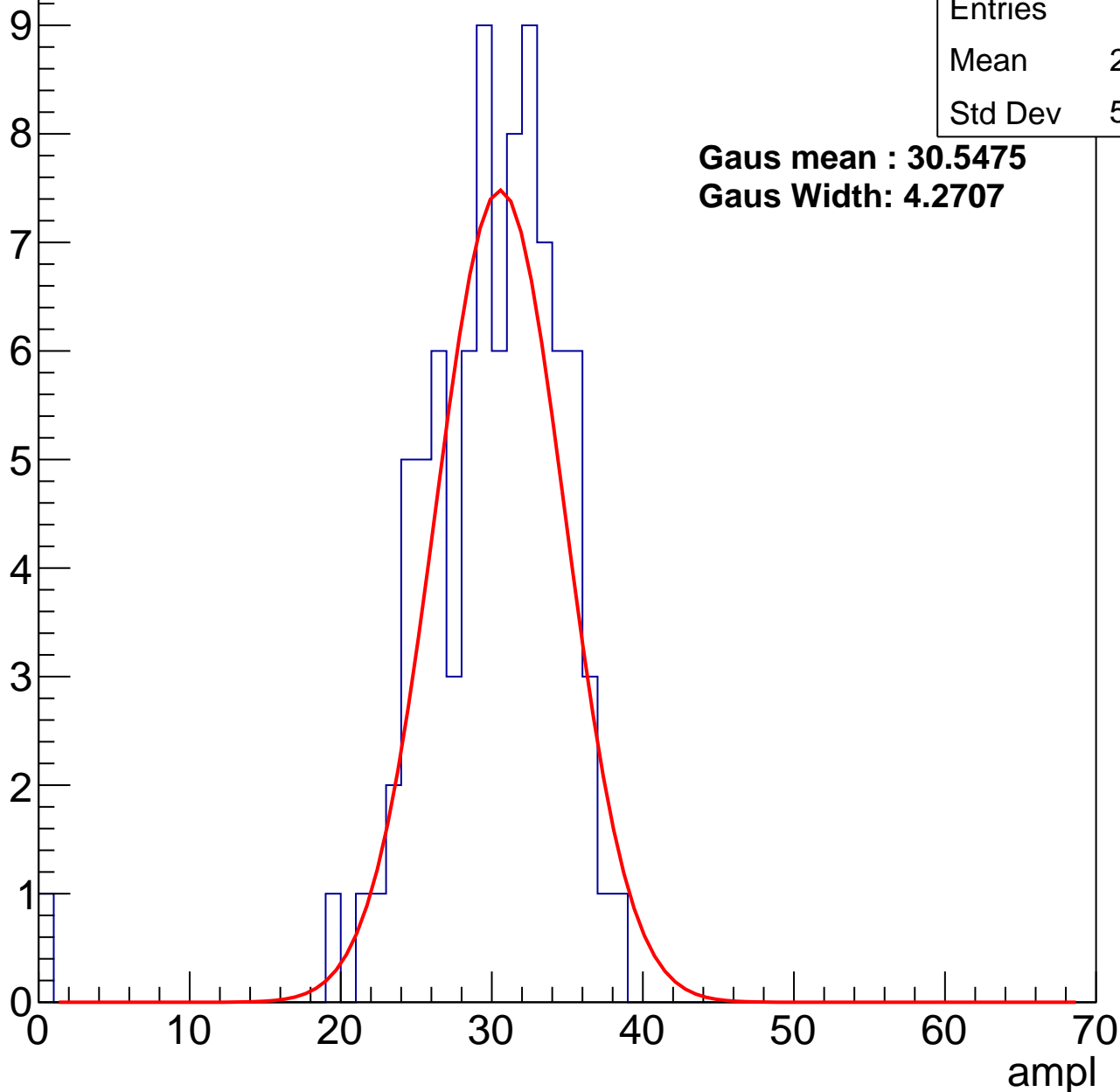
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	87
Mean	29.46
Std Dev	5.112

**Gaus mean : 30.5475**

**Gaus Width: 4.2707**



# B1L103S, U26-ch119, adc1

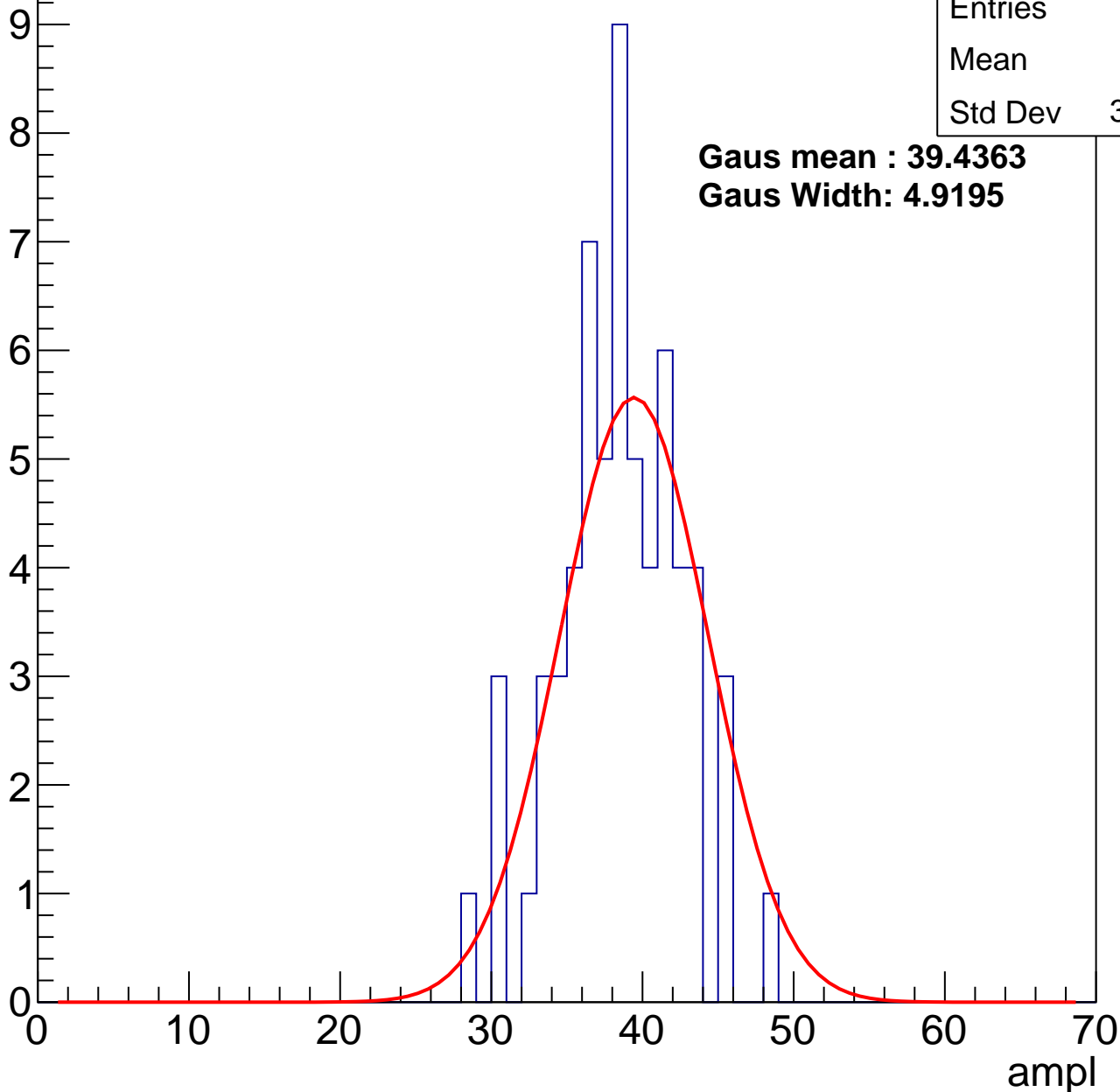
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	38
Std Dev	3.996

**Gaus mean : 39.4363**

**Gaus Width: 4.9195**



# B1L103S, U26-ch119, adc2

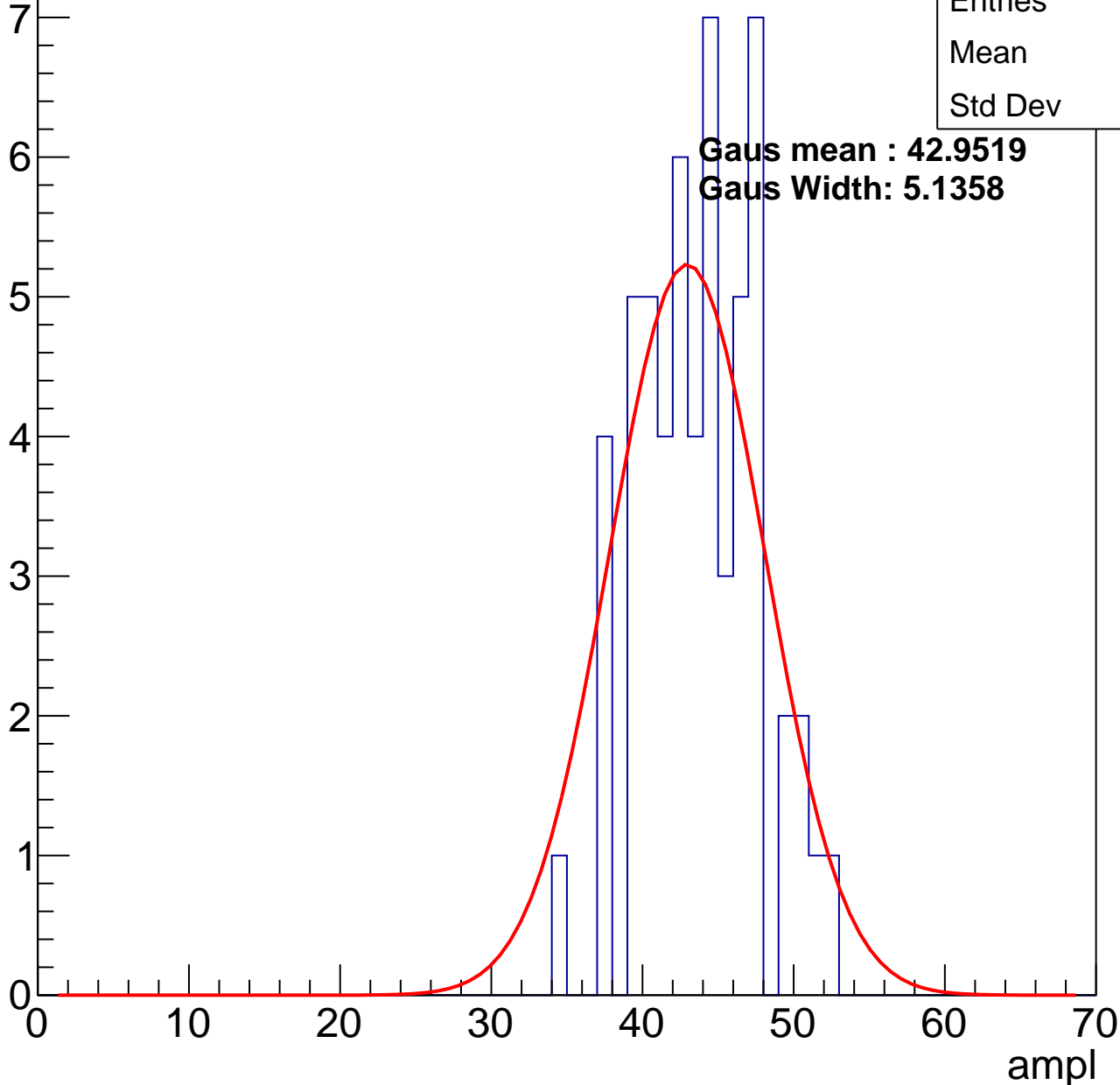
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	43.3
Std Dev	3.88

**Gaus mean : 42.9519**

**Gaus Width: 5.1358**

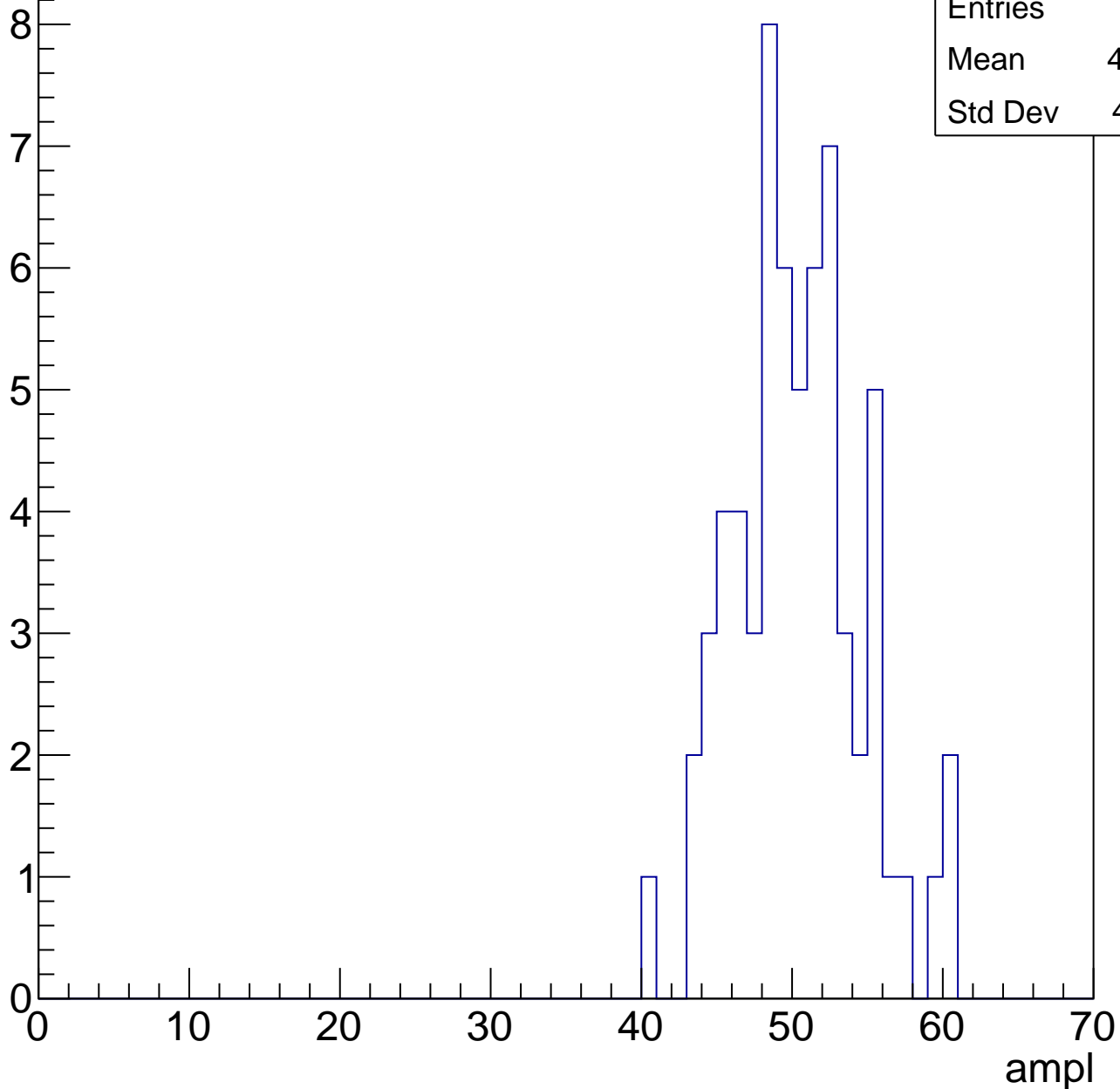


# B1L103S, U26-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	64
Mean	49.92
Std Dev	4.181

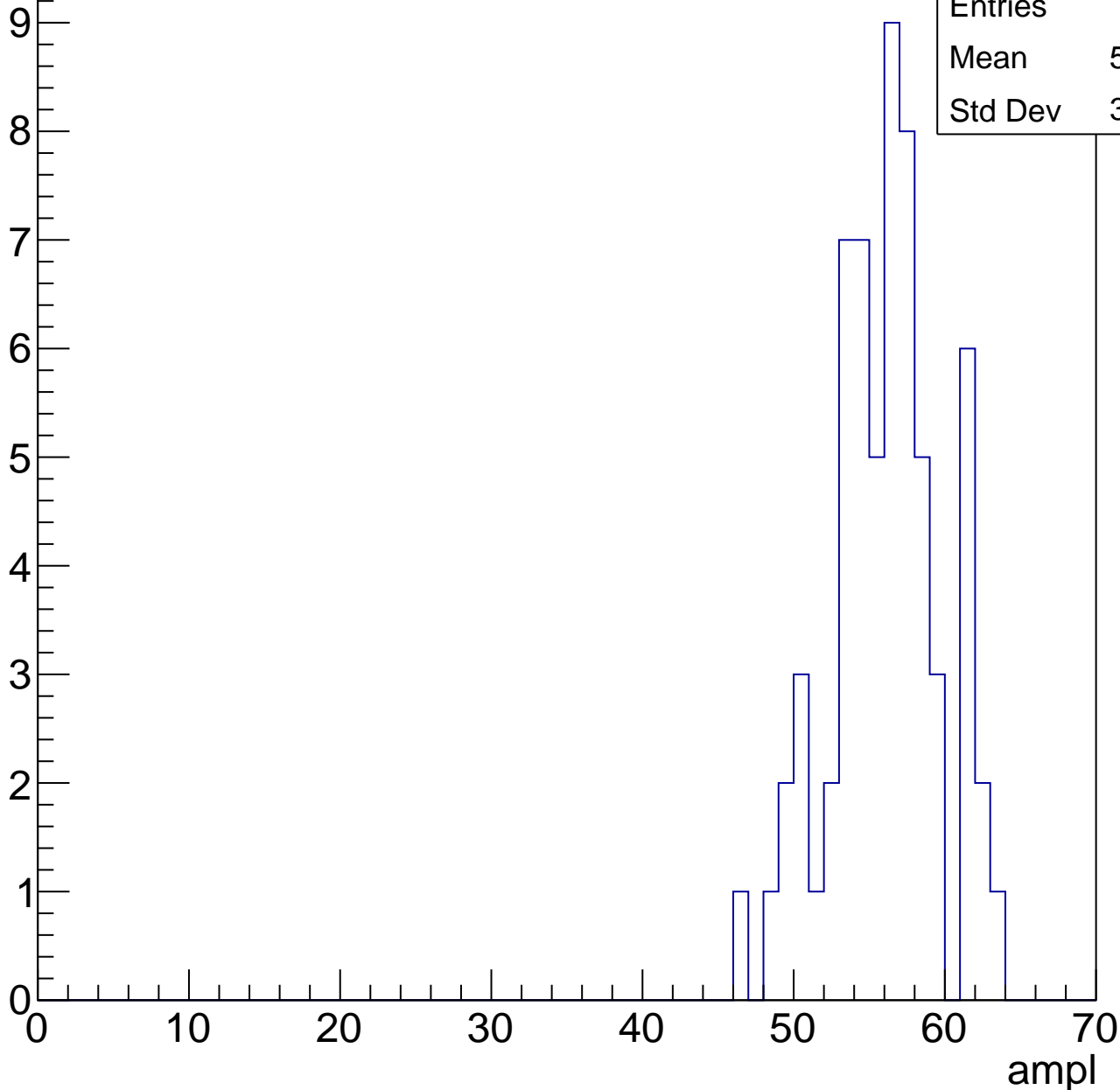


# B1L103S, U26-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	55.57
Std Dev	3.646

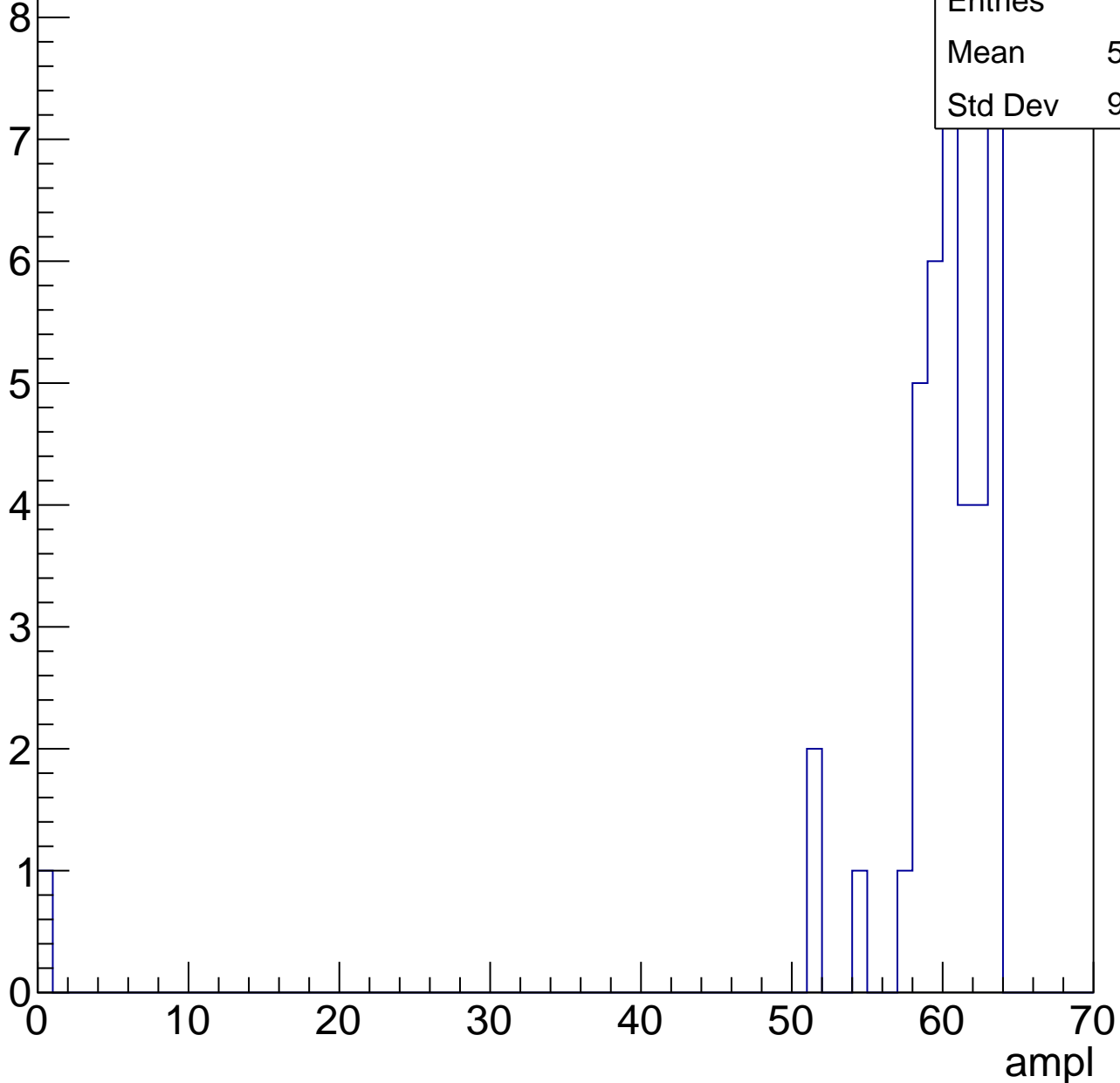


# B1L103S, U26-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

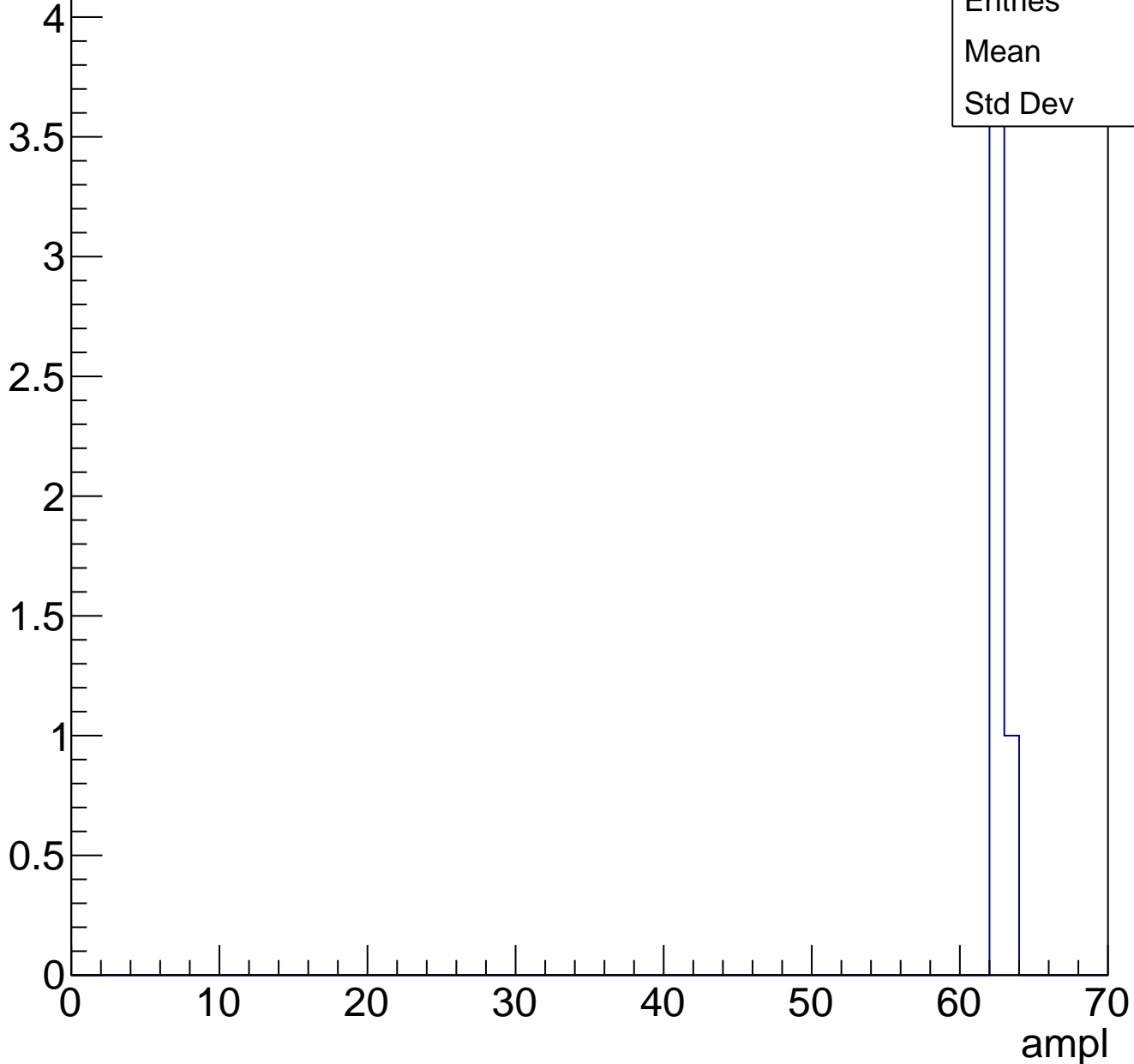
Entries	40
Mean	58.33
Std Dev	9.763



# B1L103S, U26-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U26-ch120, adc0

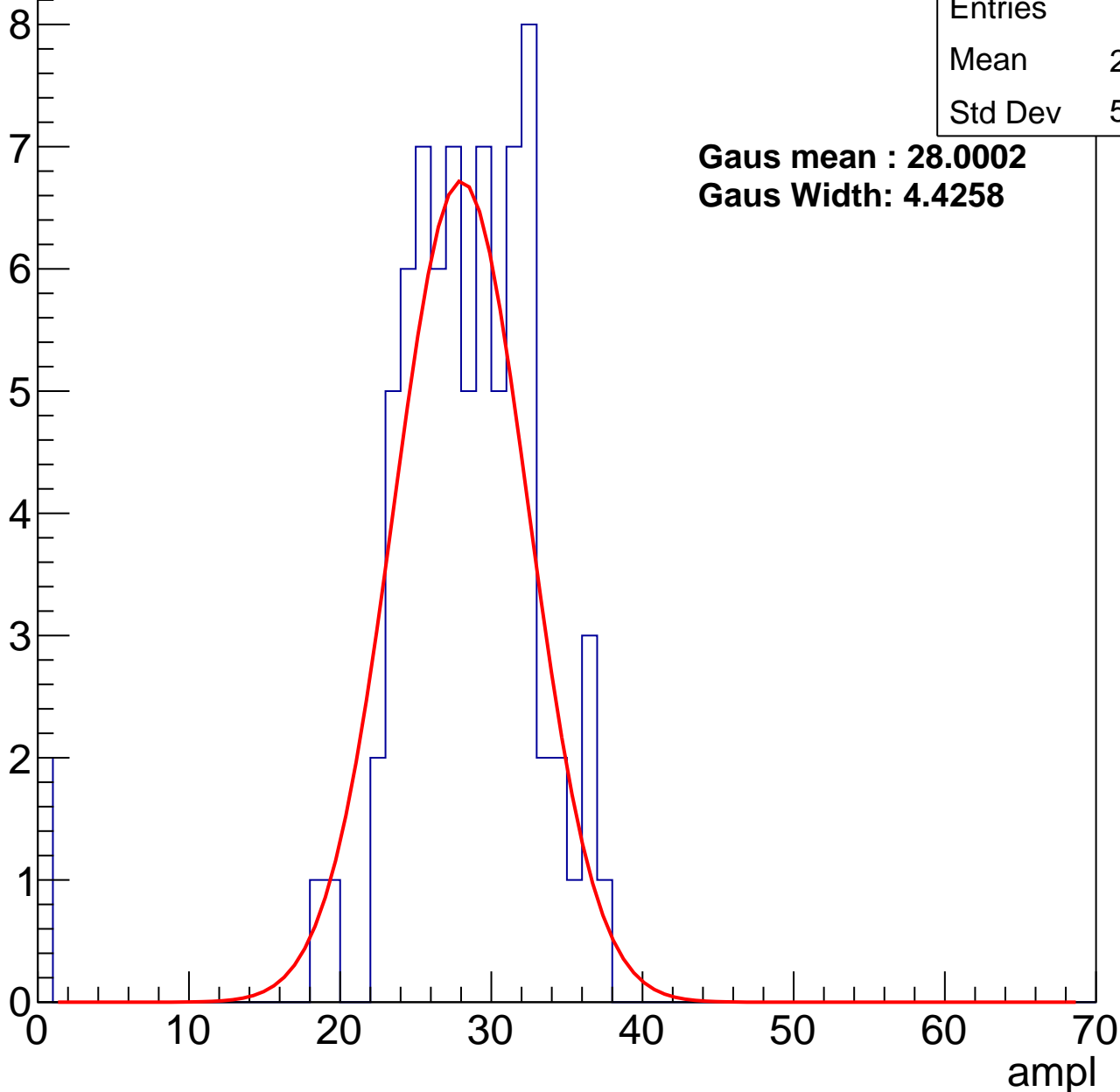
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	27.44
Std Dev	5.963

**Gaus mean : 28.0002**

**Gaus Width: 4.4258**



# B1L103S, U26-ch120, adc1

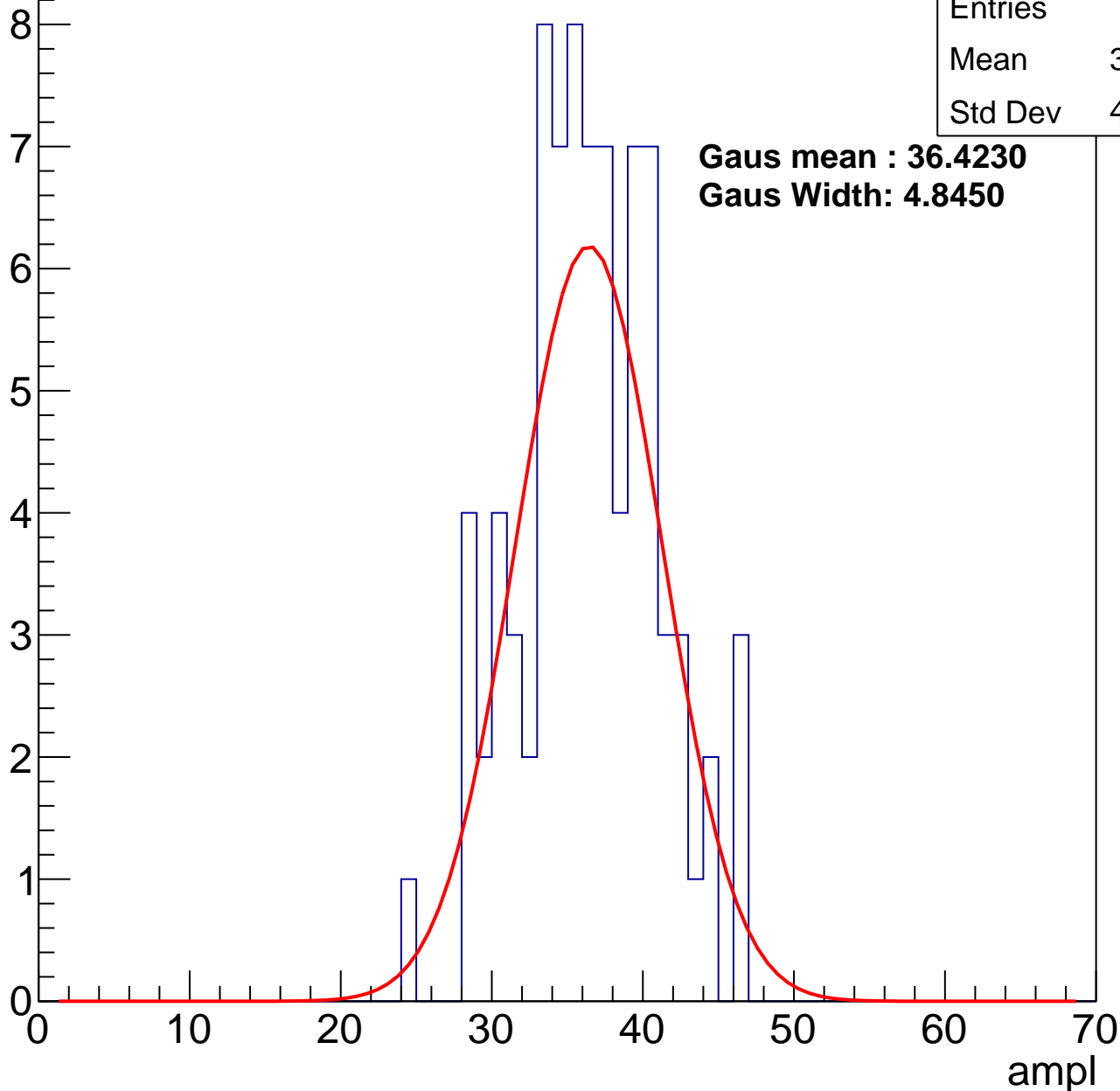
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	35.99
Std Dev	4.546

**Gaus mean : 36.4230**

**Gaus Width: 4.8450**



# B1L103S, U26-ch120, adc2

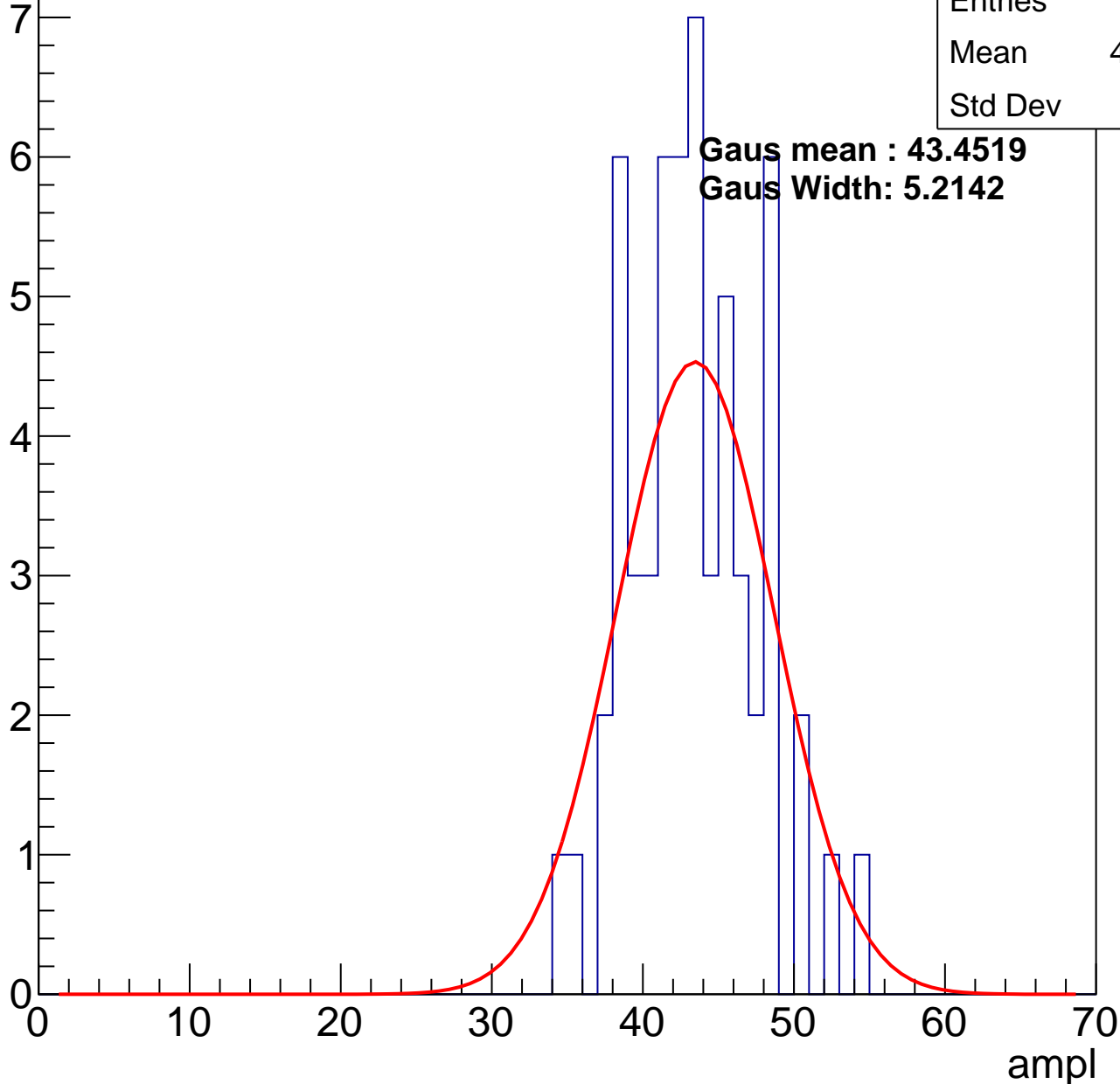
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	58
Mean	42.93
Std Dev	4.16

**Gaus mean : 43.4519**

**Gaus Width: 5.2142**

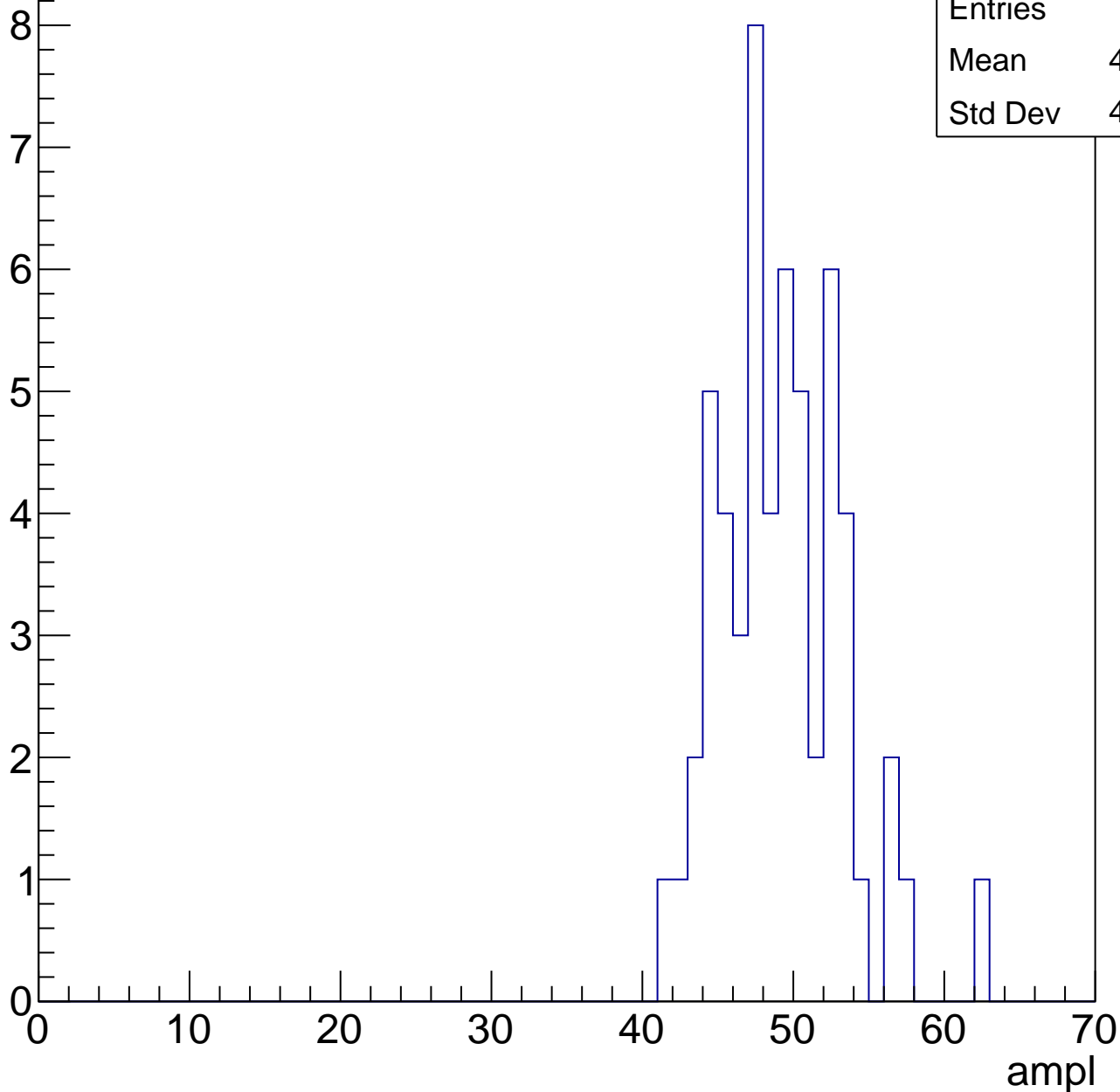


# B1L103S, U26-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	56
Mean	48.75
Std Dev	4.054

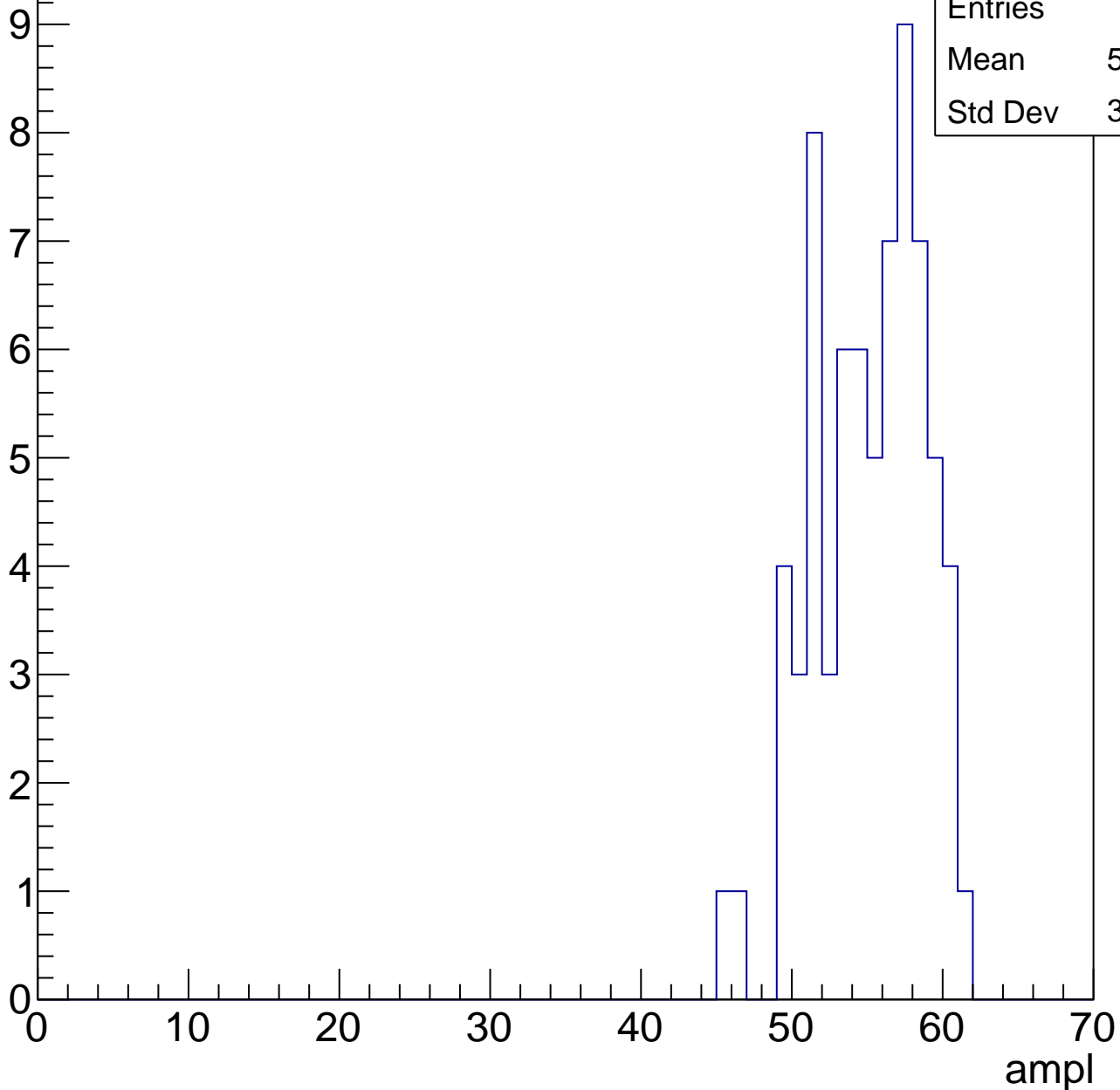


# B1L103S, U26-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	70
Mean	54.64
Std Dev	3.582

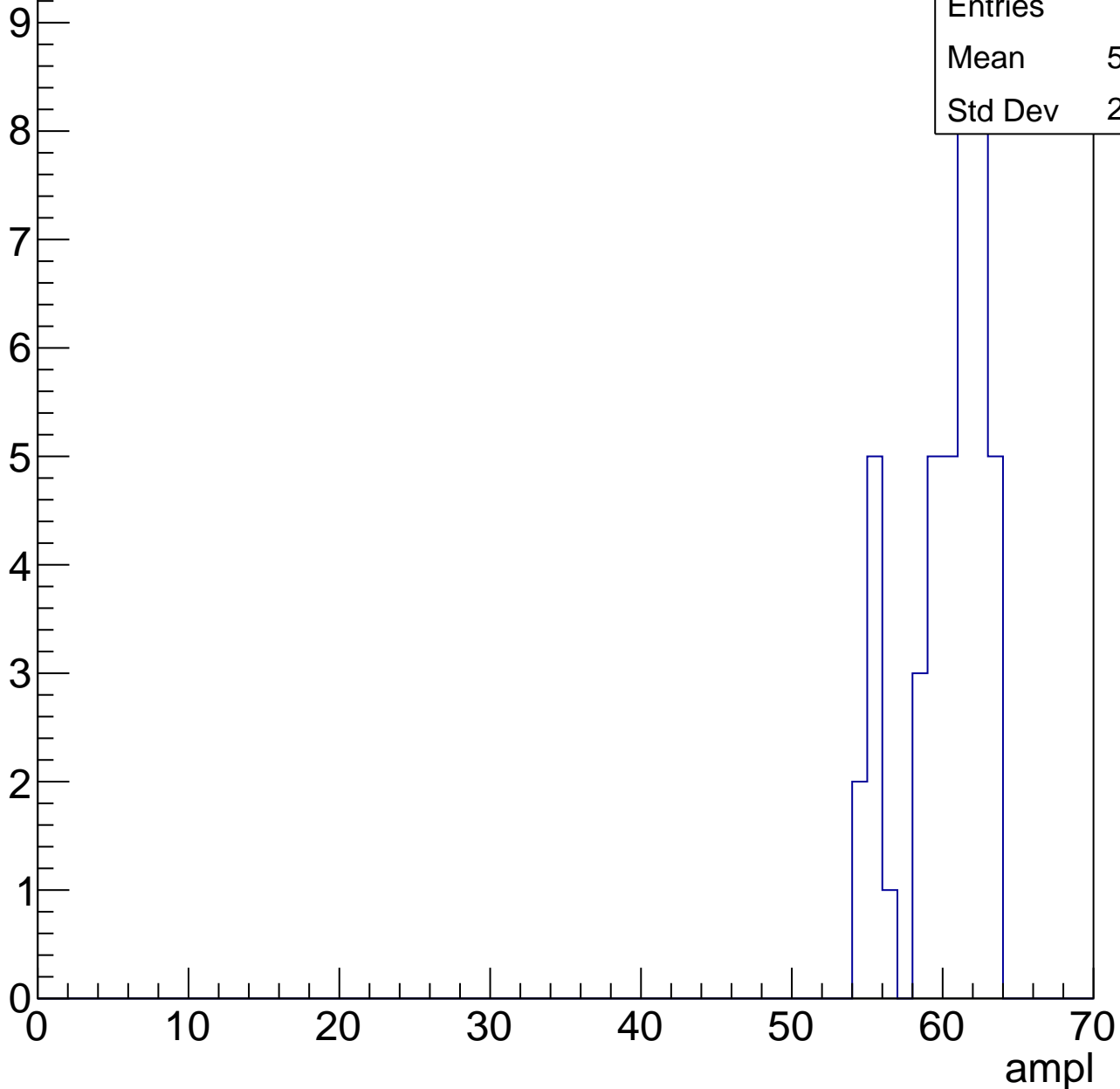


# B1L103S, U26-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	59.77
Std Dev	2.687

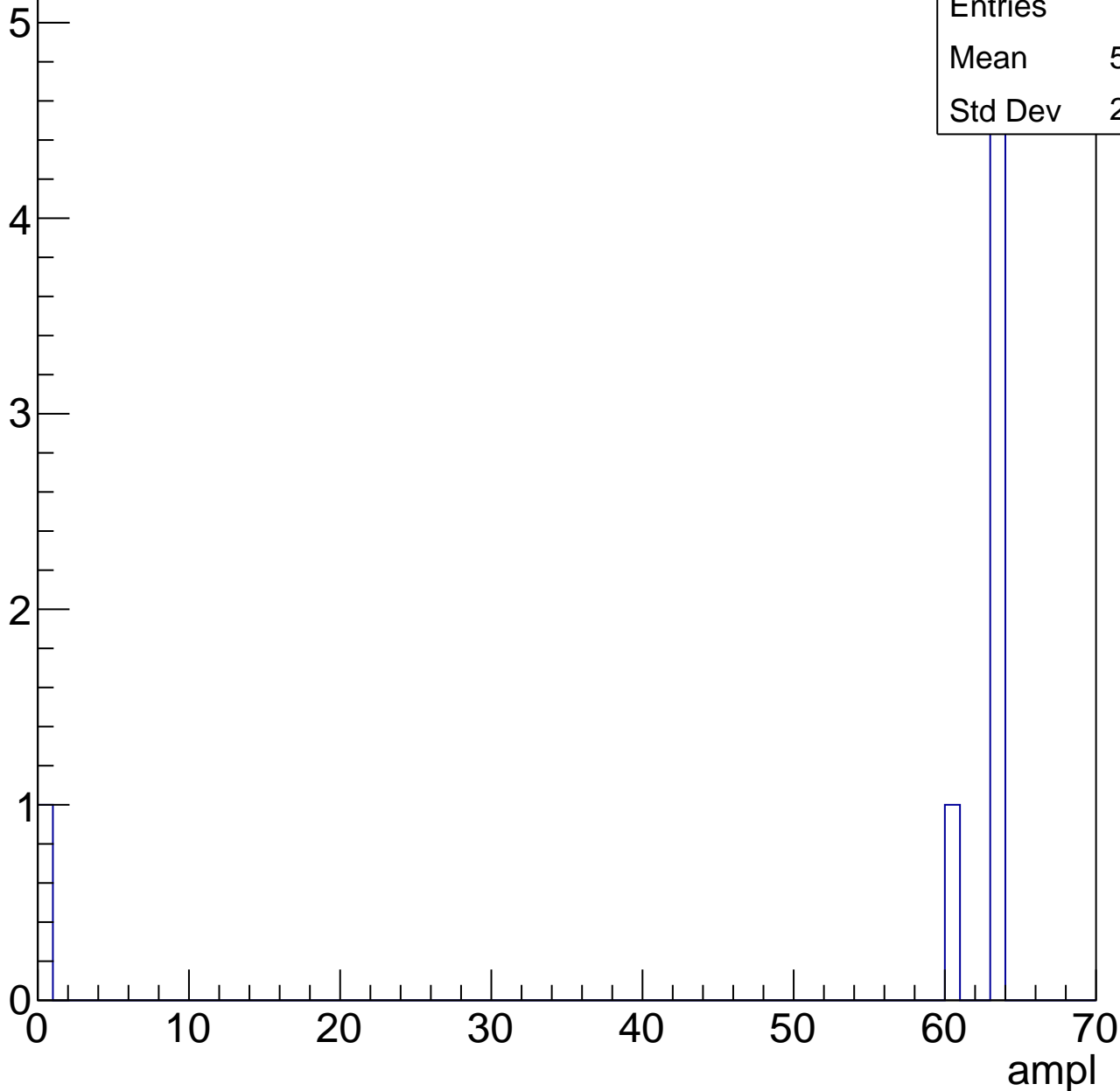


# B1L103S, U26-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	7
Mean	53.57
Std Dev	21.89





# B1L103S, U26-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



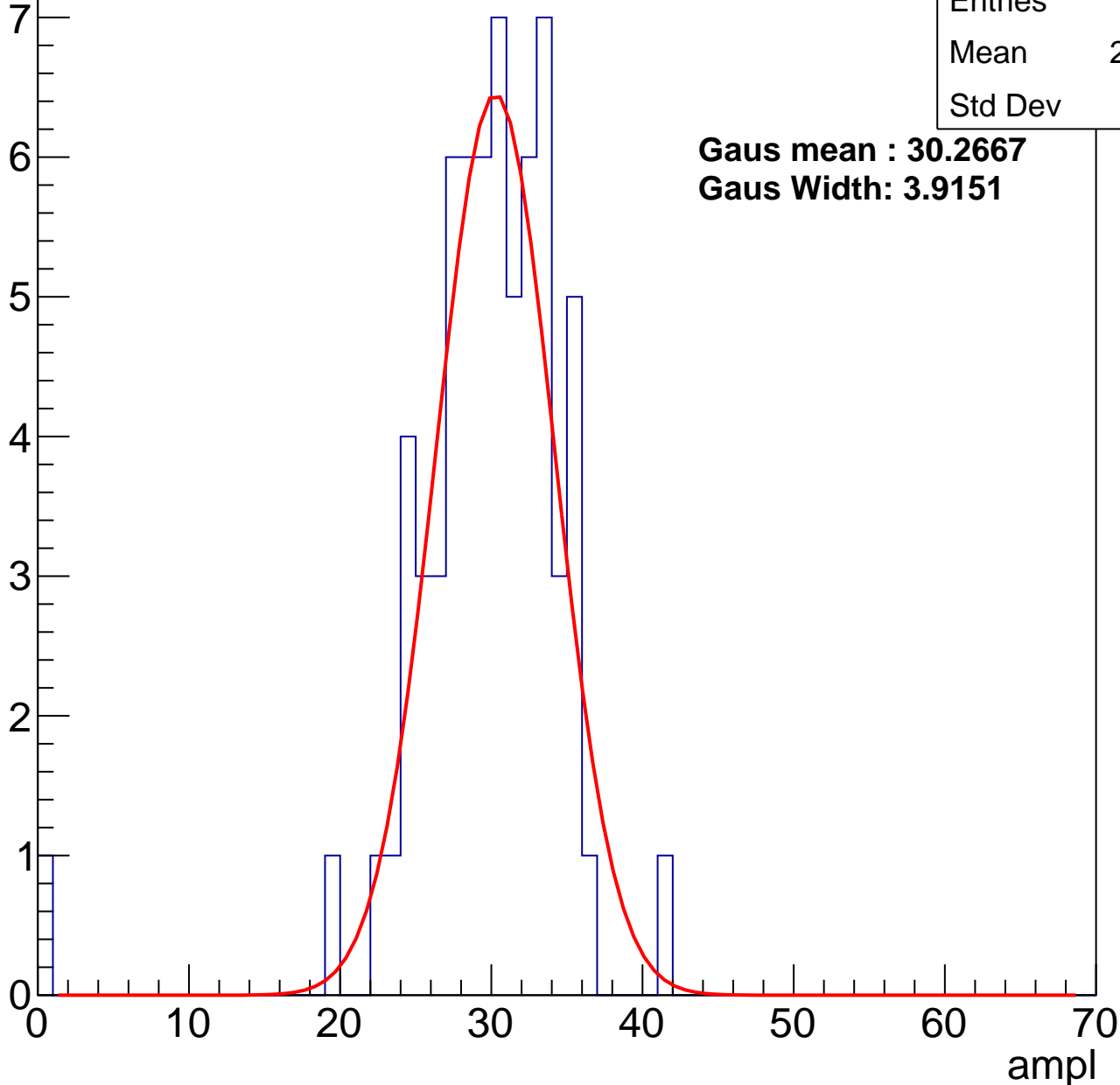
# B1L103S, U26-ch121, adc0

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	67
Mean	29.24
Std Dev	5.28

**Gaus mean : 30.2667**  
**Gaus Width: 3.9151**



# B1L103S, U26-ch121, adc1

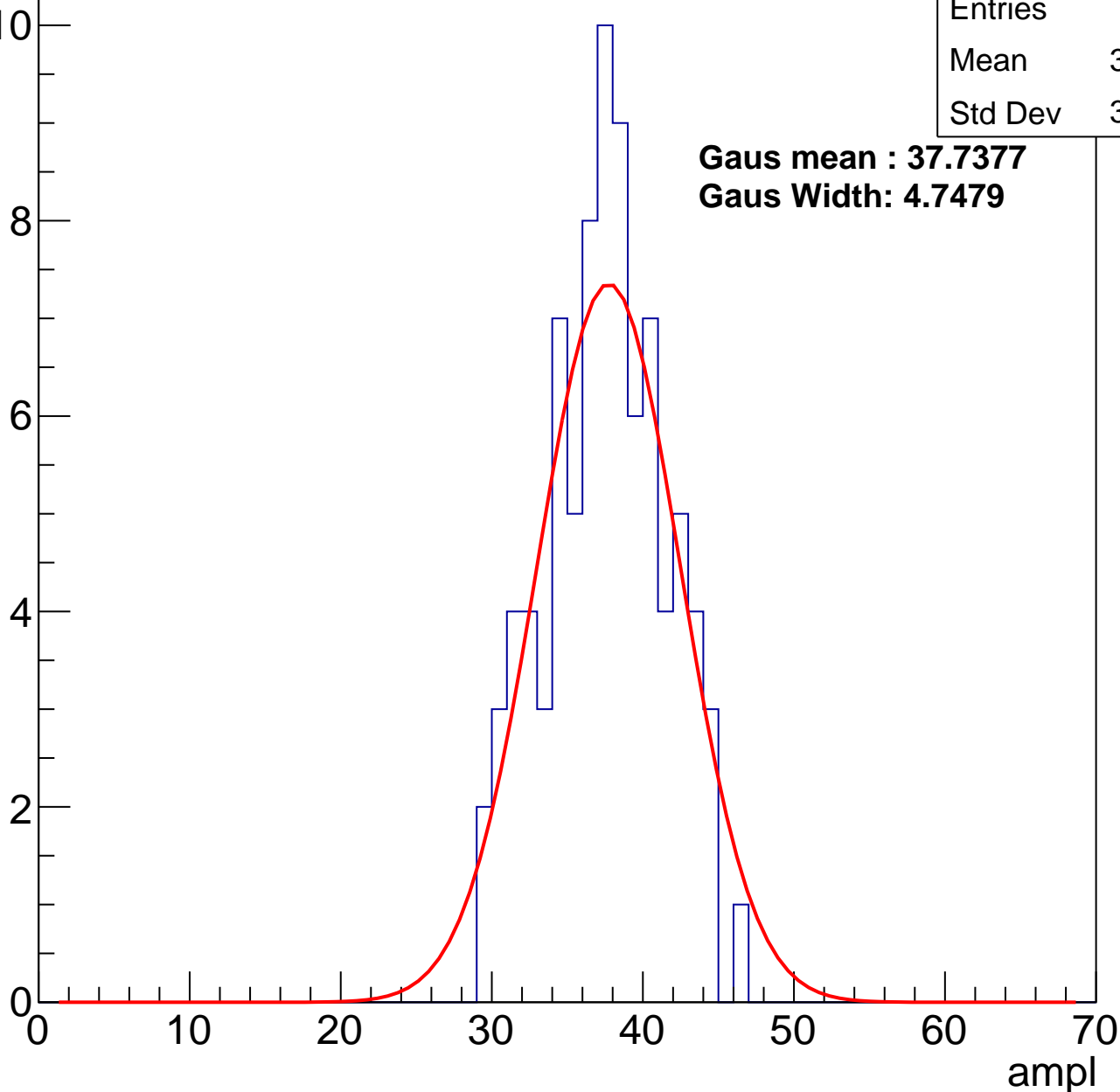
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	85
Mean	37.06
Std Dev	3.933

**Gaus mean : 37.7377**

**Gaus Width: 4.7479**

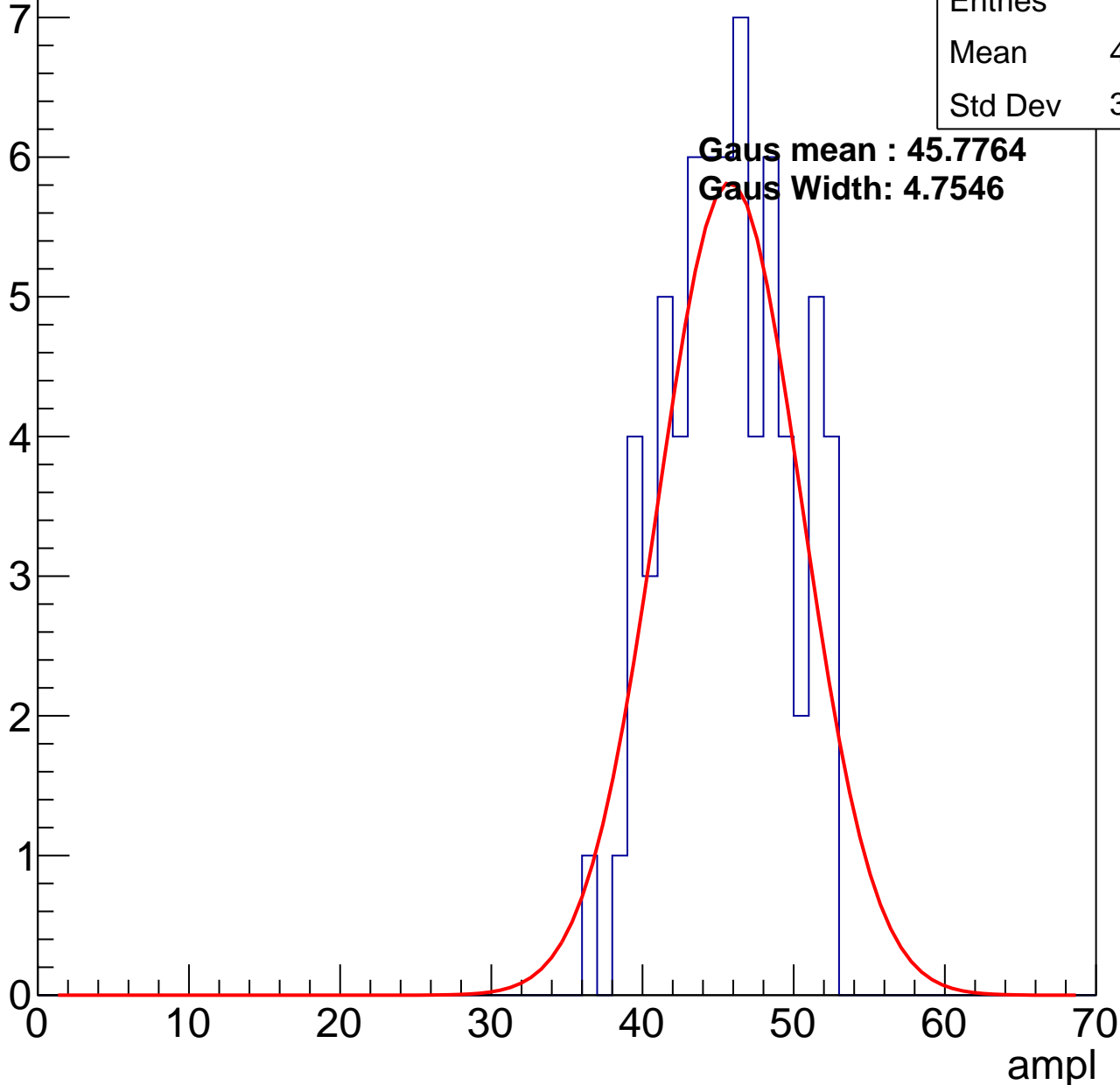


# B1L103S, U26-ch121, adc2

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	45.18
Std Dev	3.948

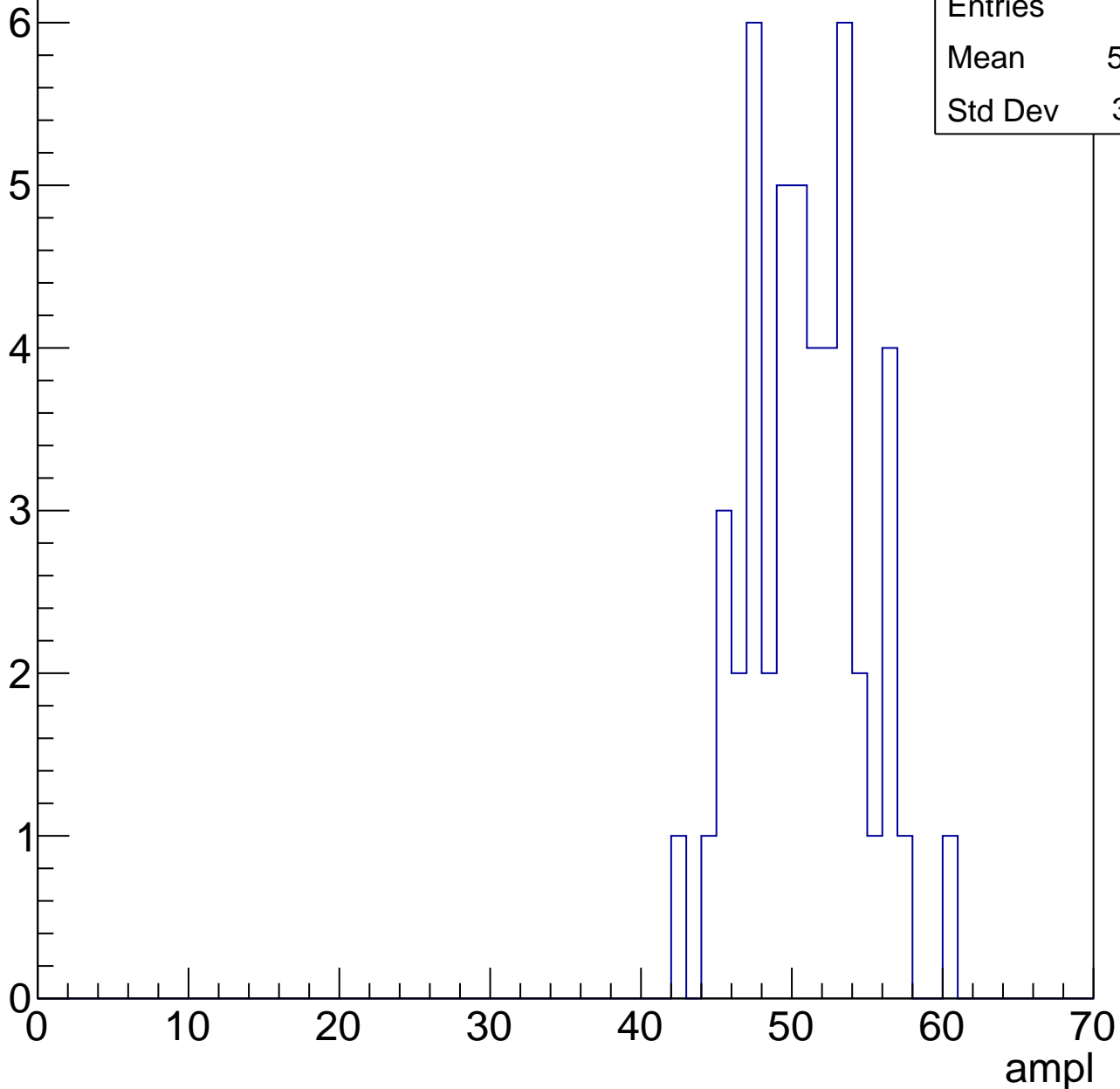


# B1L103S, U26-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	50.42
Std Dev	3.791

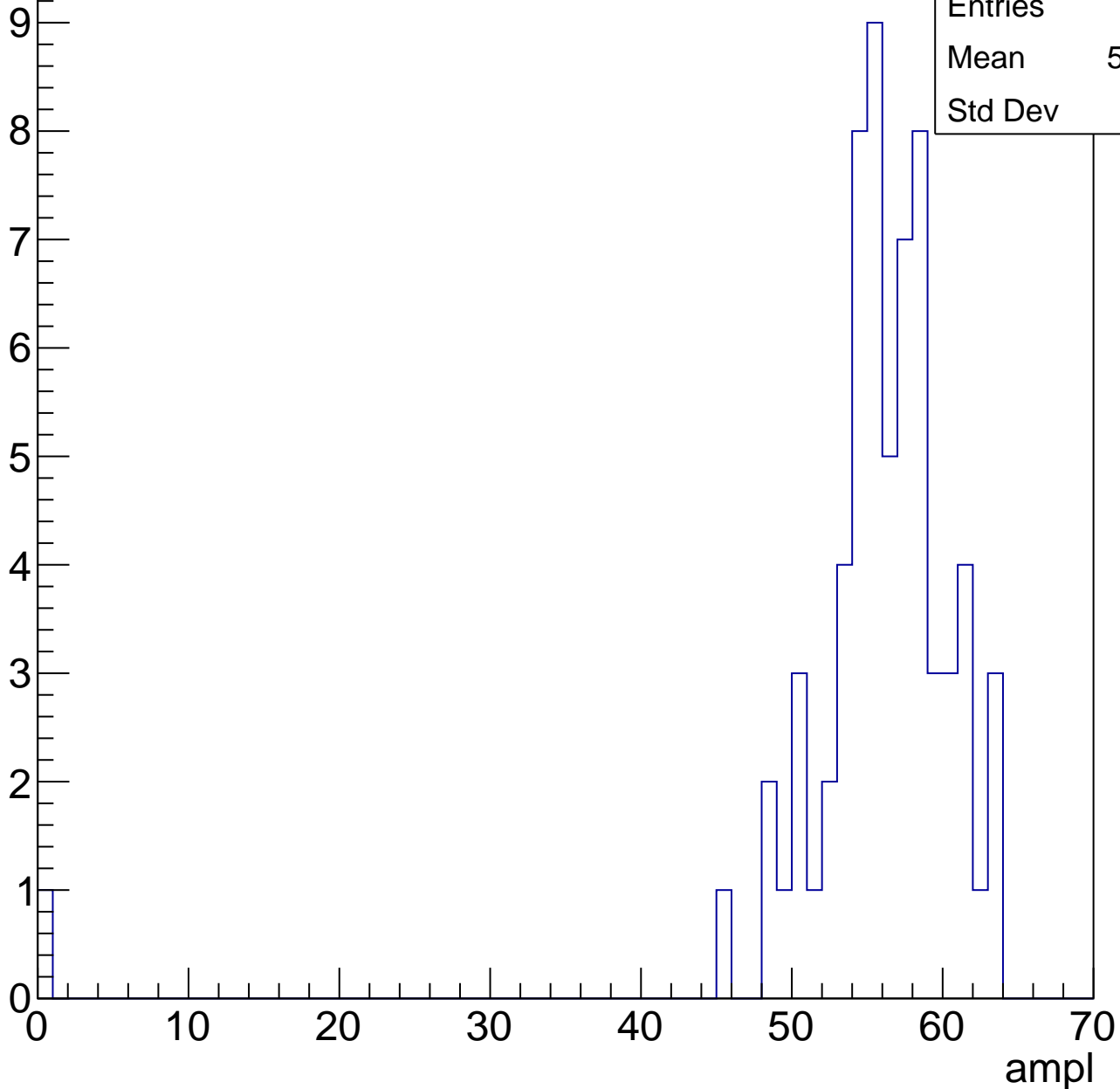


# B1L103S, U26-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	66
Mean	54.98
Std Dev	7.79



# B1L103S, U26-ch121, adc5

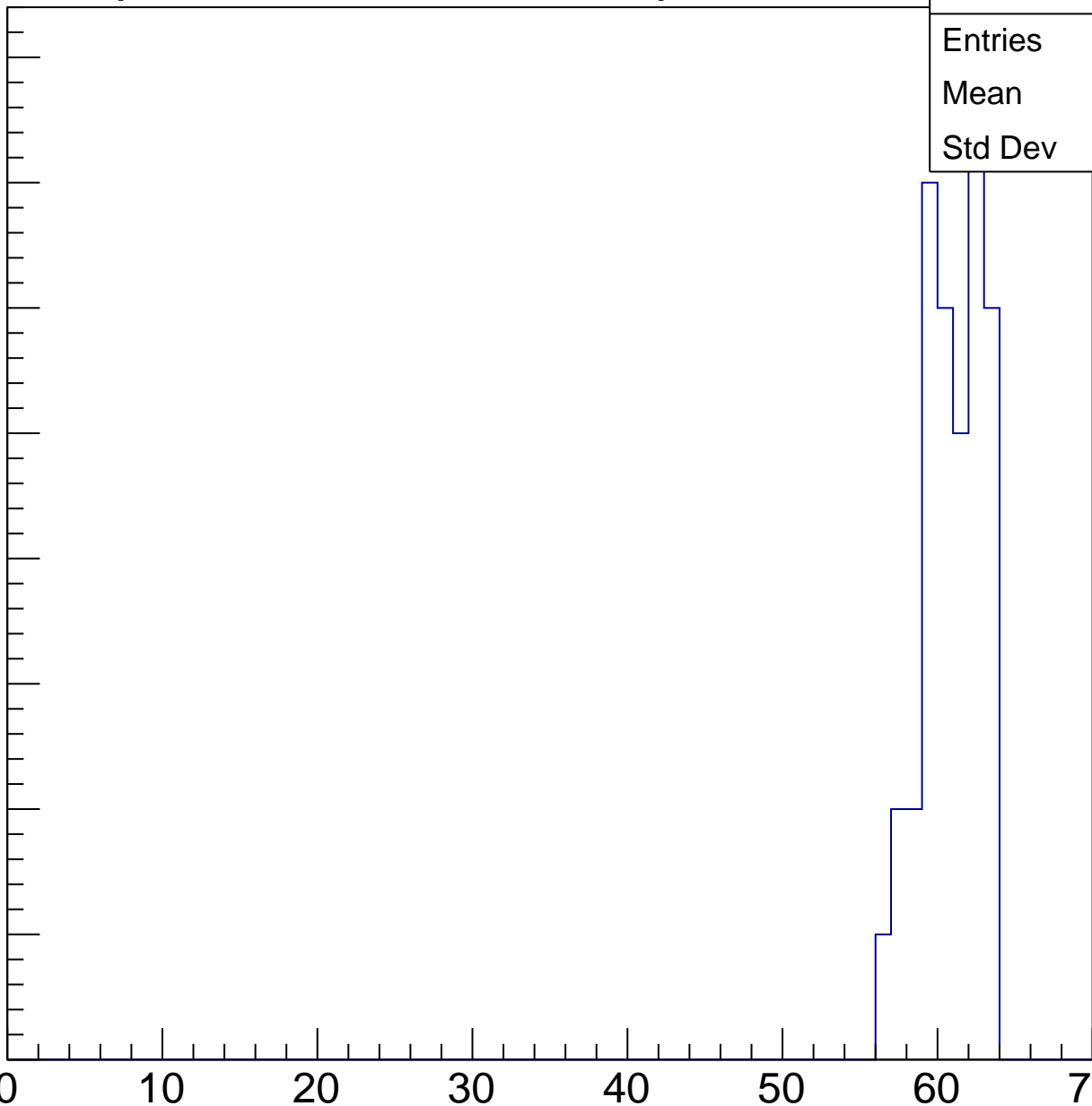
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	37
Mean	60.49
Std Dev	1.883

ampl



# B1L103S, U26-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L103S, U26-ch122, adc0

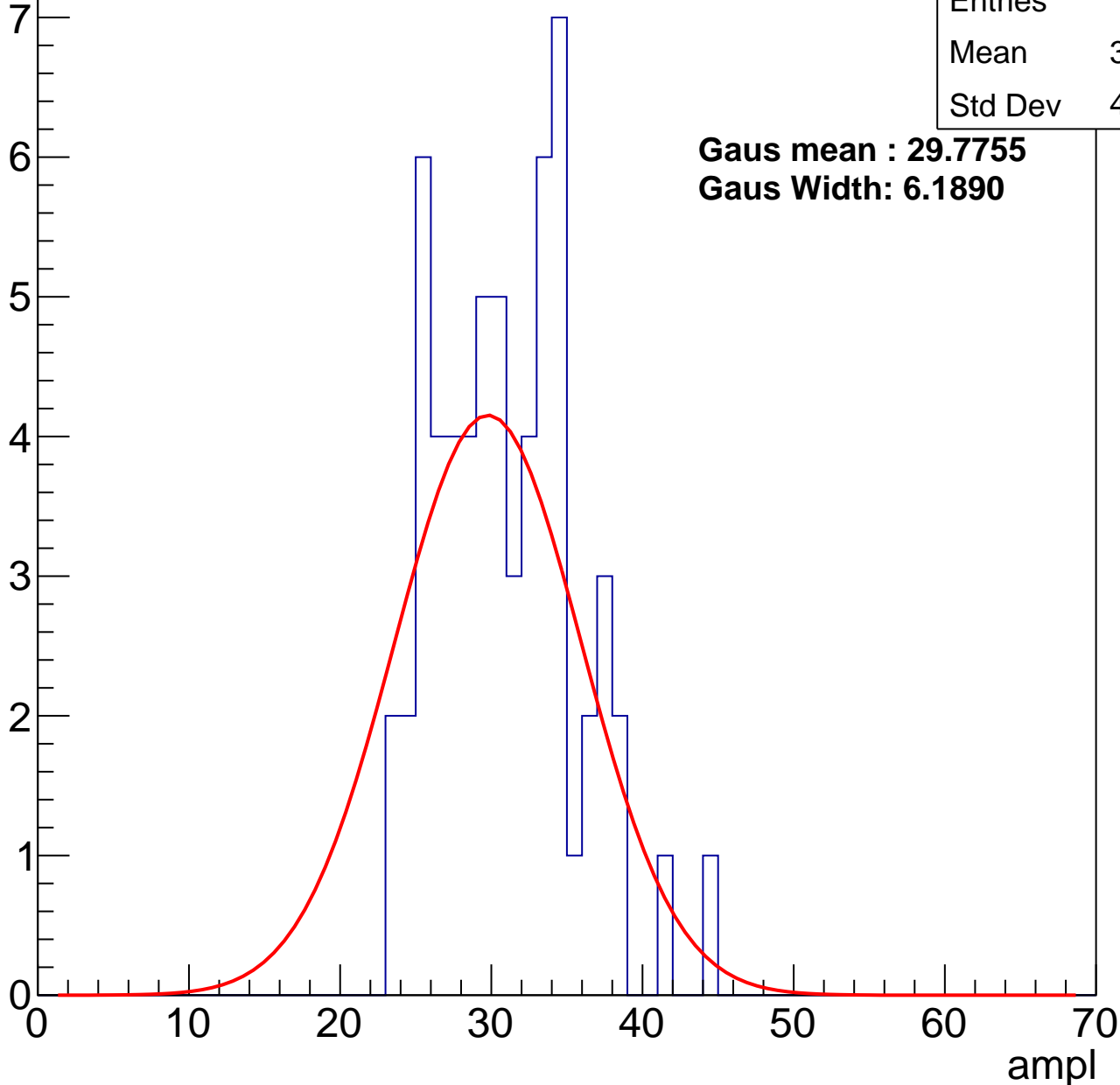
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	30.63
Std Dev	4.562

**Gaus mean : 29.7755**

**Gaus Width: 6.1890**



# B1L103S, U26-ch122, adc1

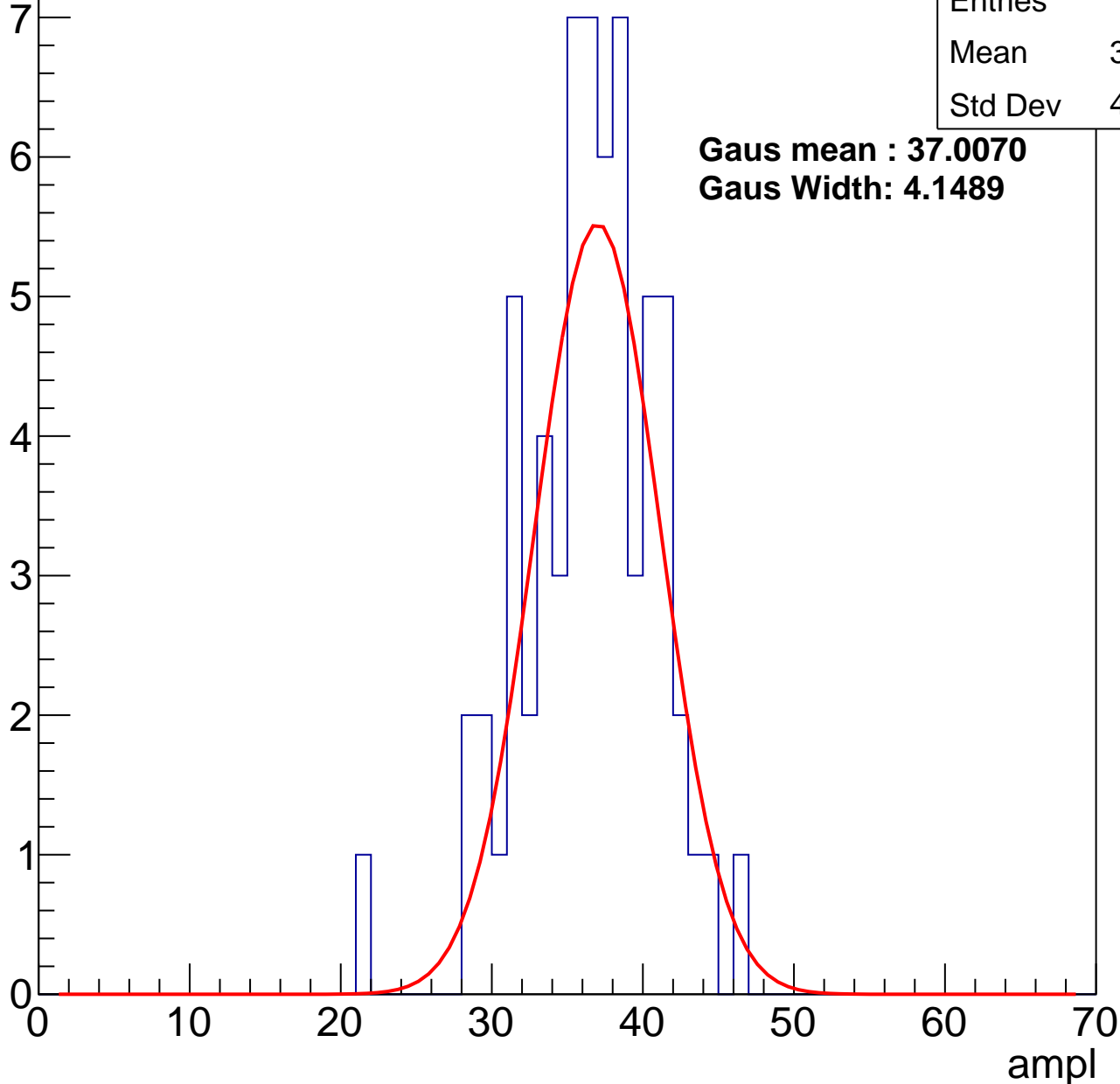
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	36.03
Std Dev	4.385

**Gaus mean : 37.0070**

**Gaus Width: 4.1489**



# B1L103S, U26-ch122, adc2

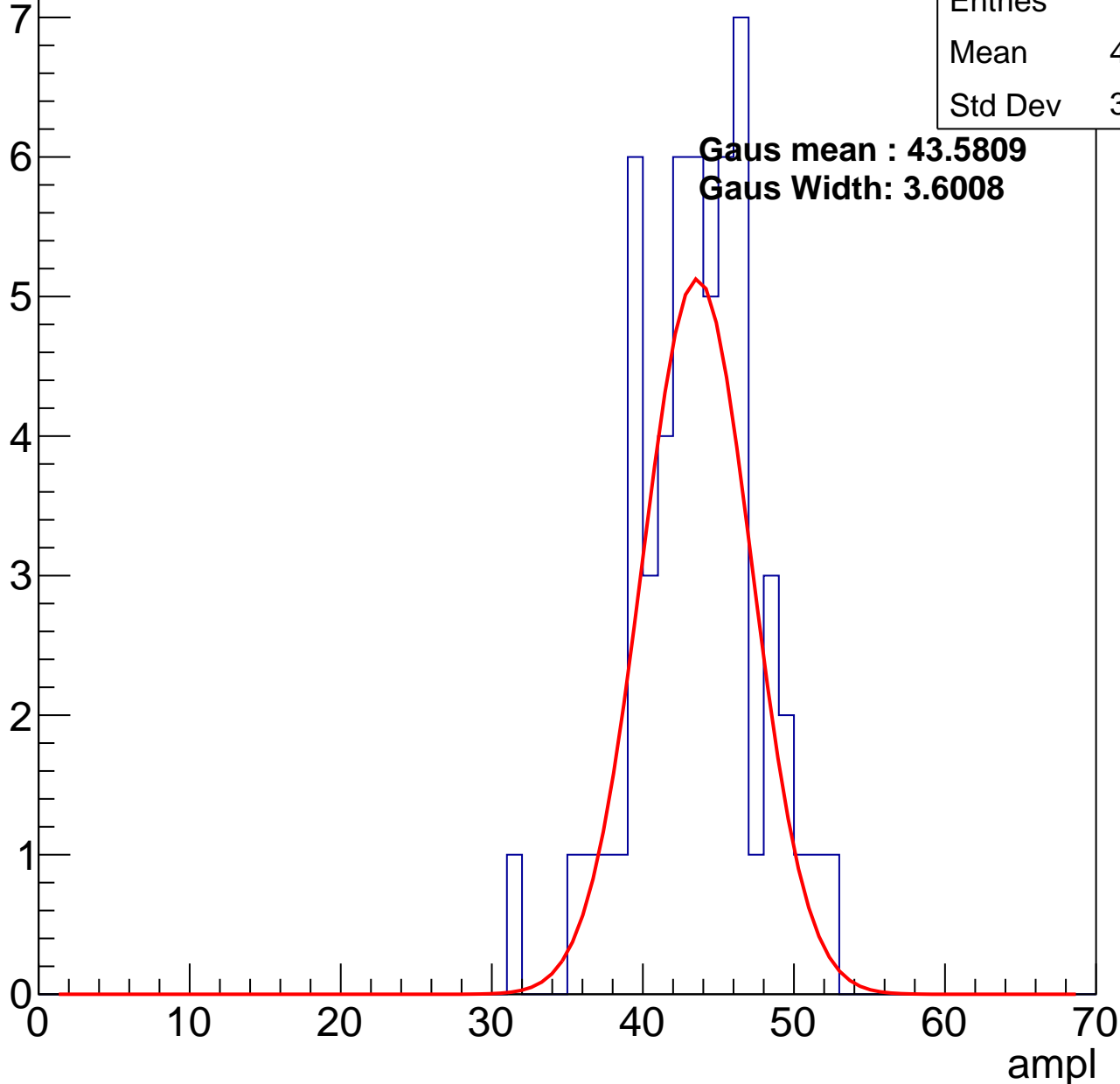
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	57
Mean	43.14
Std Dev	3.998

**Gaus mean : 43.5809**

**Gaus Width: 3.6008**

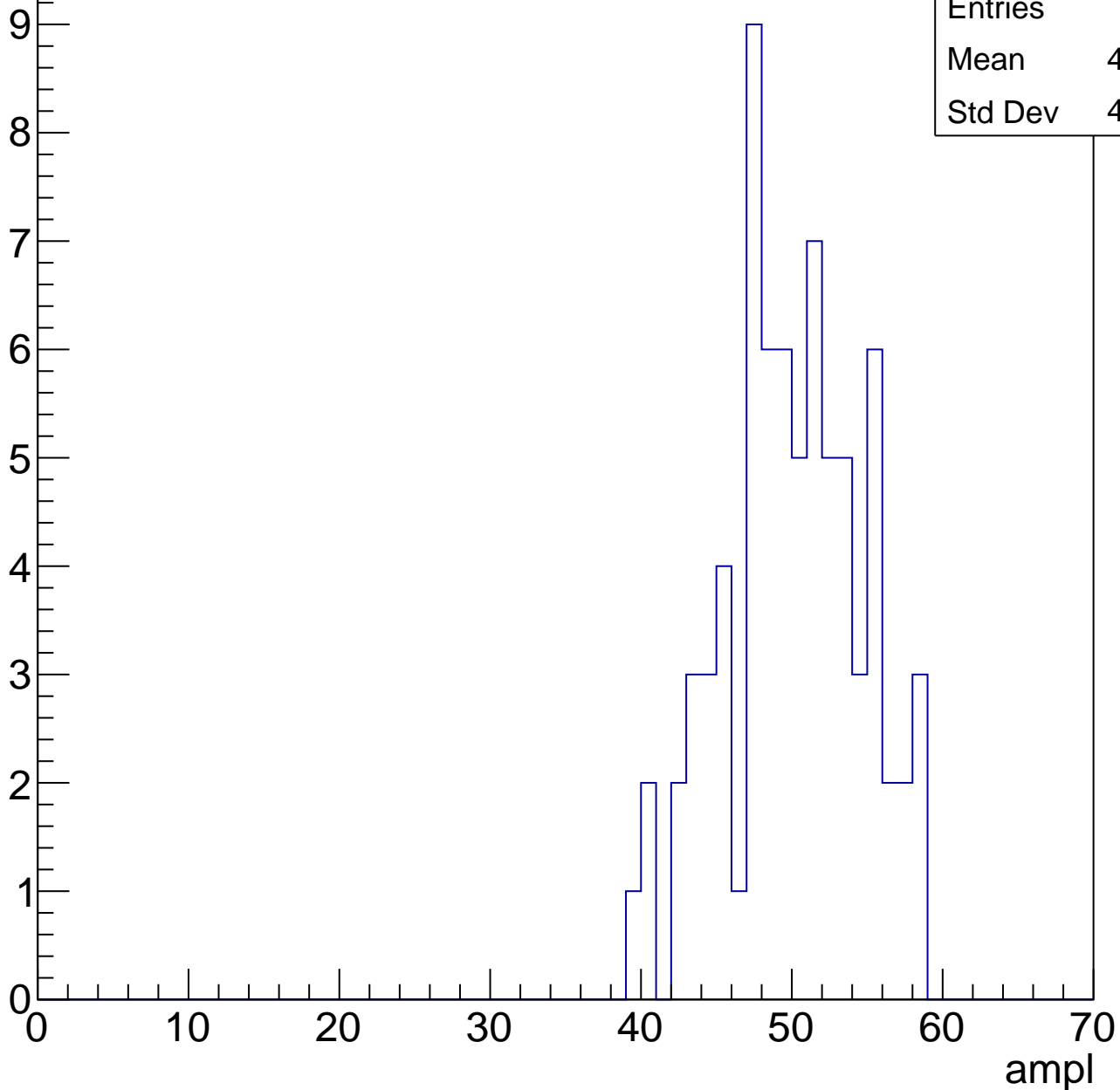


# B1L103S, U26-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	49.59
Std Dev	4.546

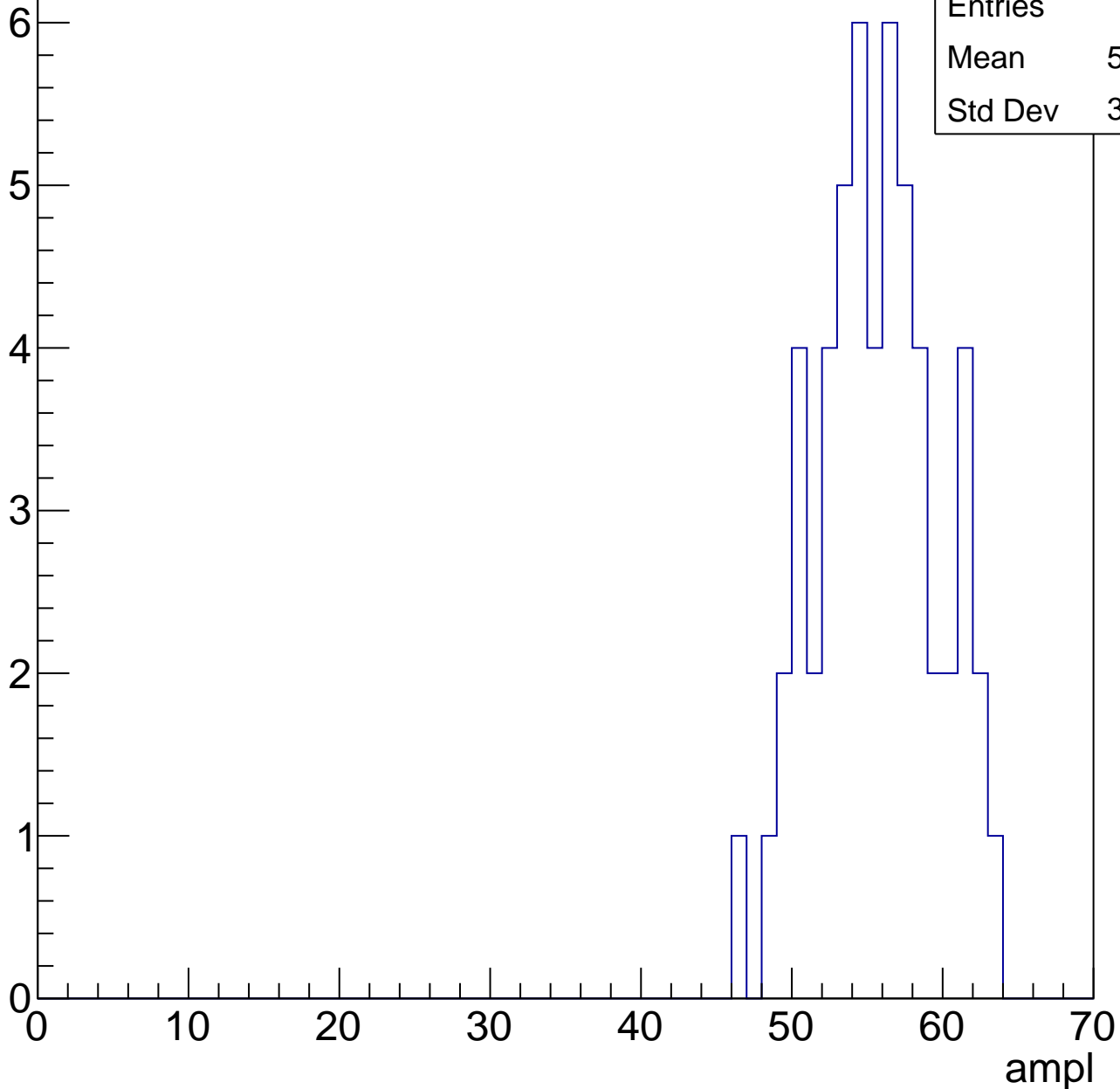


# B1L103S, U26-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	55
Mean	55.15
Std Dev	3.919

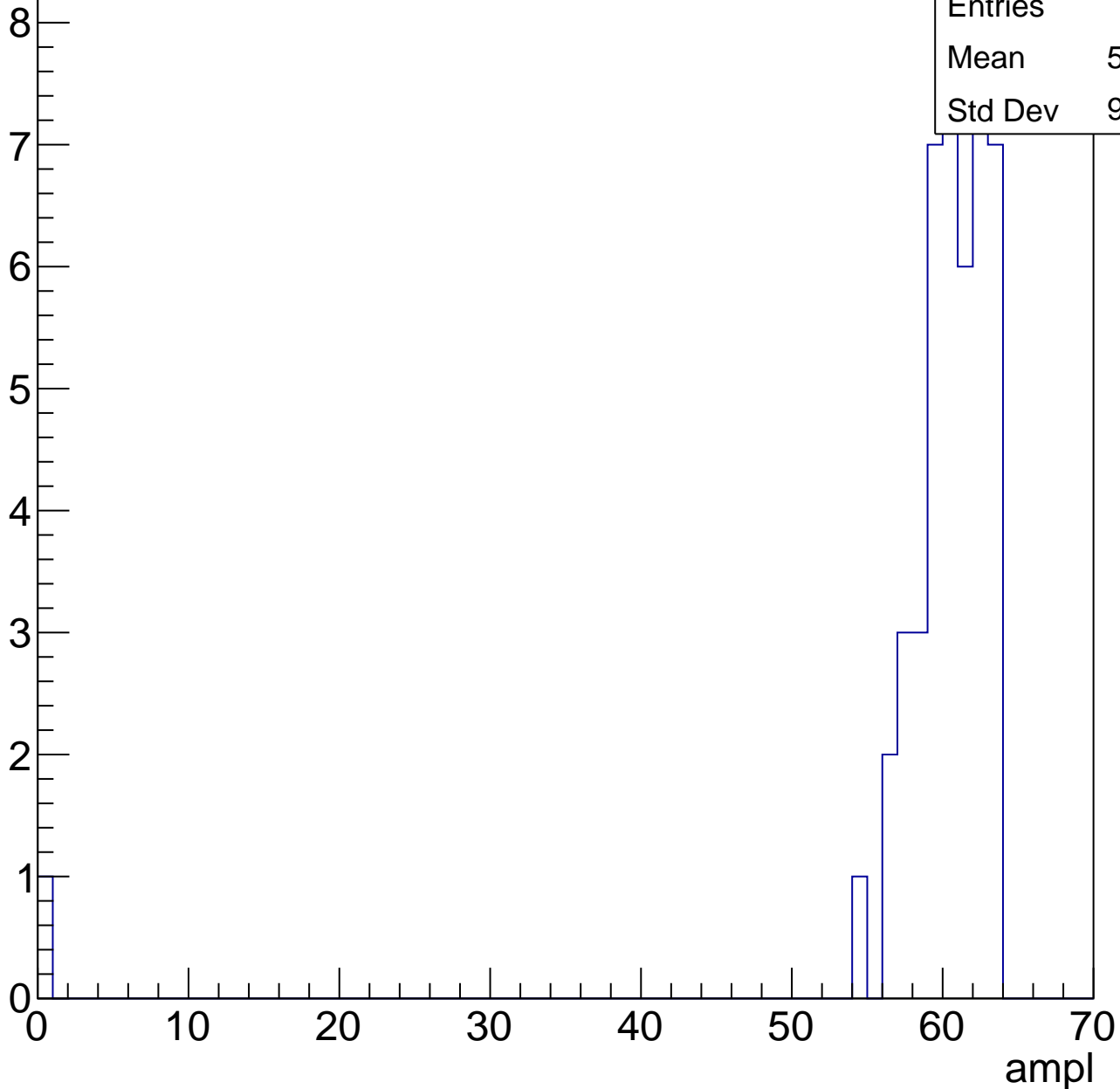


# B1L103S, U26-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	46
Mean	58.85
Std Dev	9.034



# B1L103S, U26-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	61.67
Std Dev	1.886

0 10 20 30 40 50 60 70

ampl





# B1L103S, U26-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch123, adc0

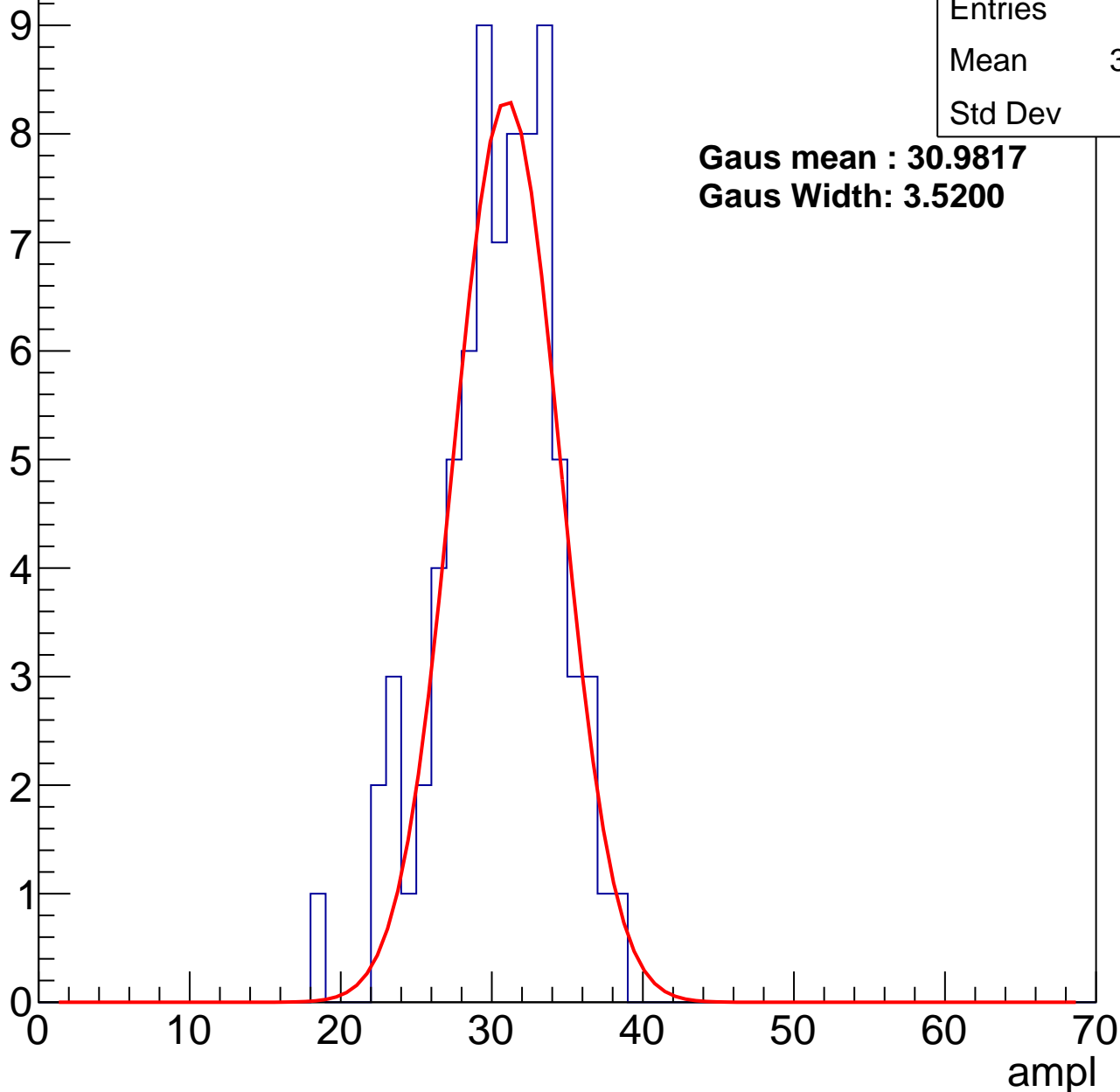
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	30.03
Std Dev	3.83

**Gaus mean : 30.9817**

**Gaus Width: 3.5200**



# B1L103S, U26-ch123, adc1

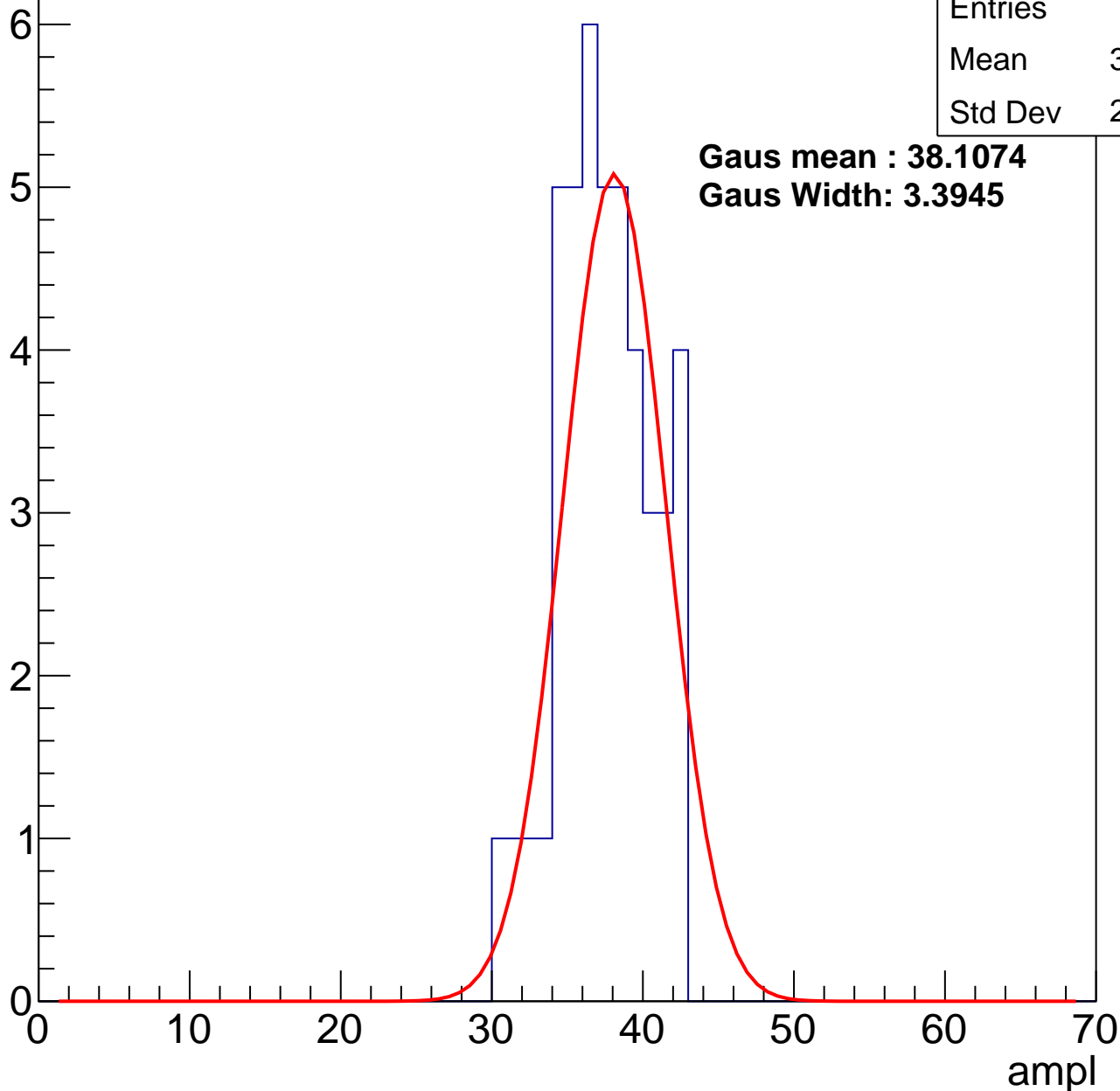
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	37.02
Std Dev	2.989

**Gaus mean : 38.1074**

**Gaus Width: 3.3945**



# B1L103S, U26-ch123, adc2

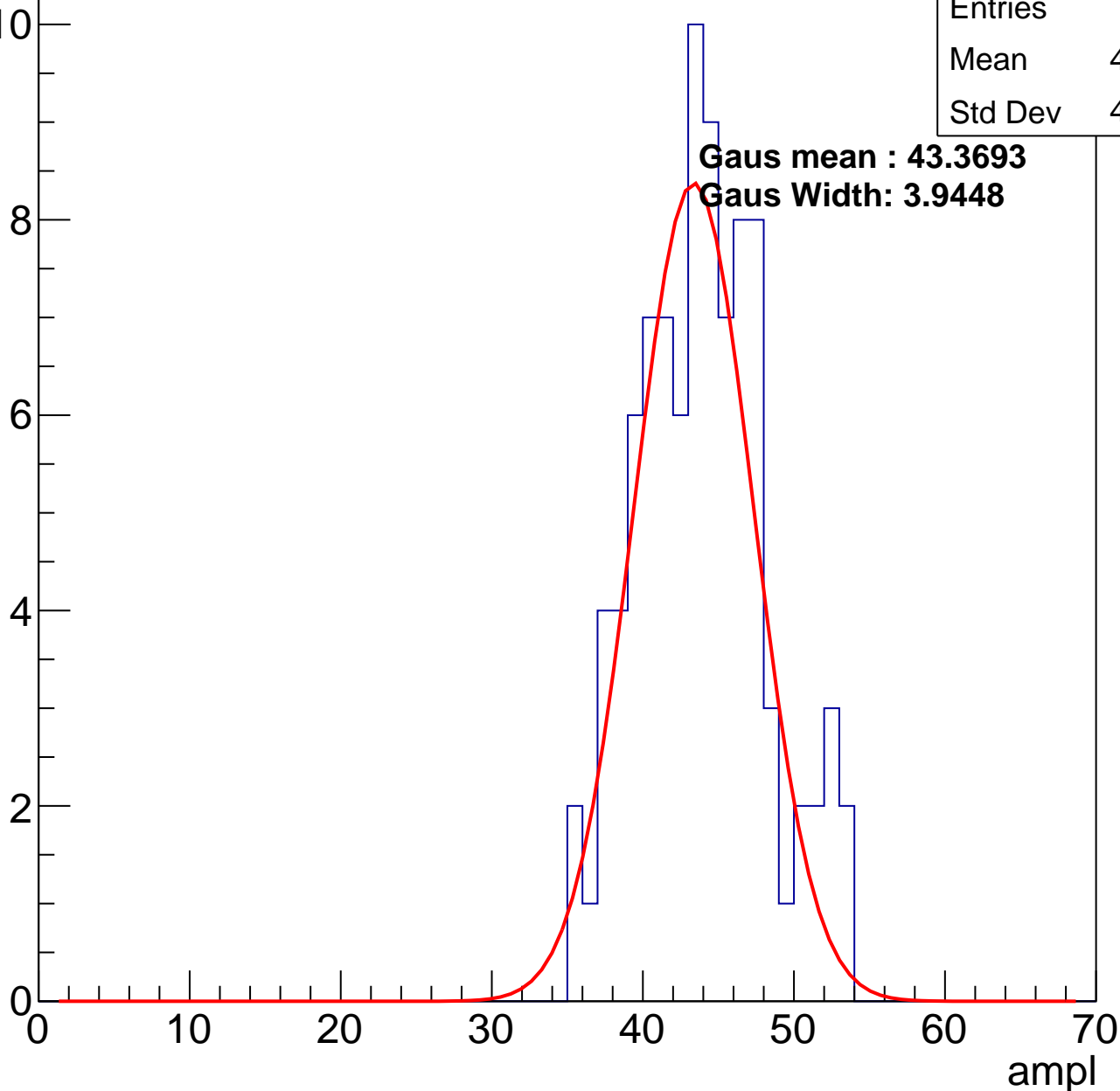
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	92
Mean	43.49
Std Dev	4.182

**Gaus mean : 43.3693**

**Gaus Width: 3.9448**

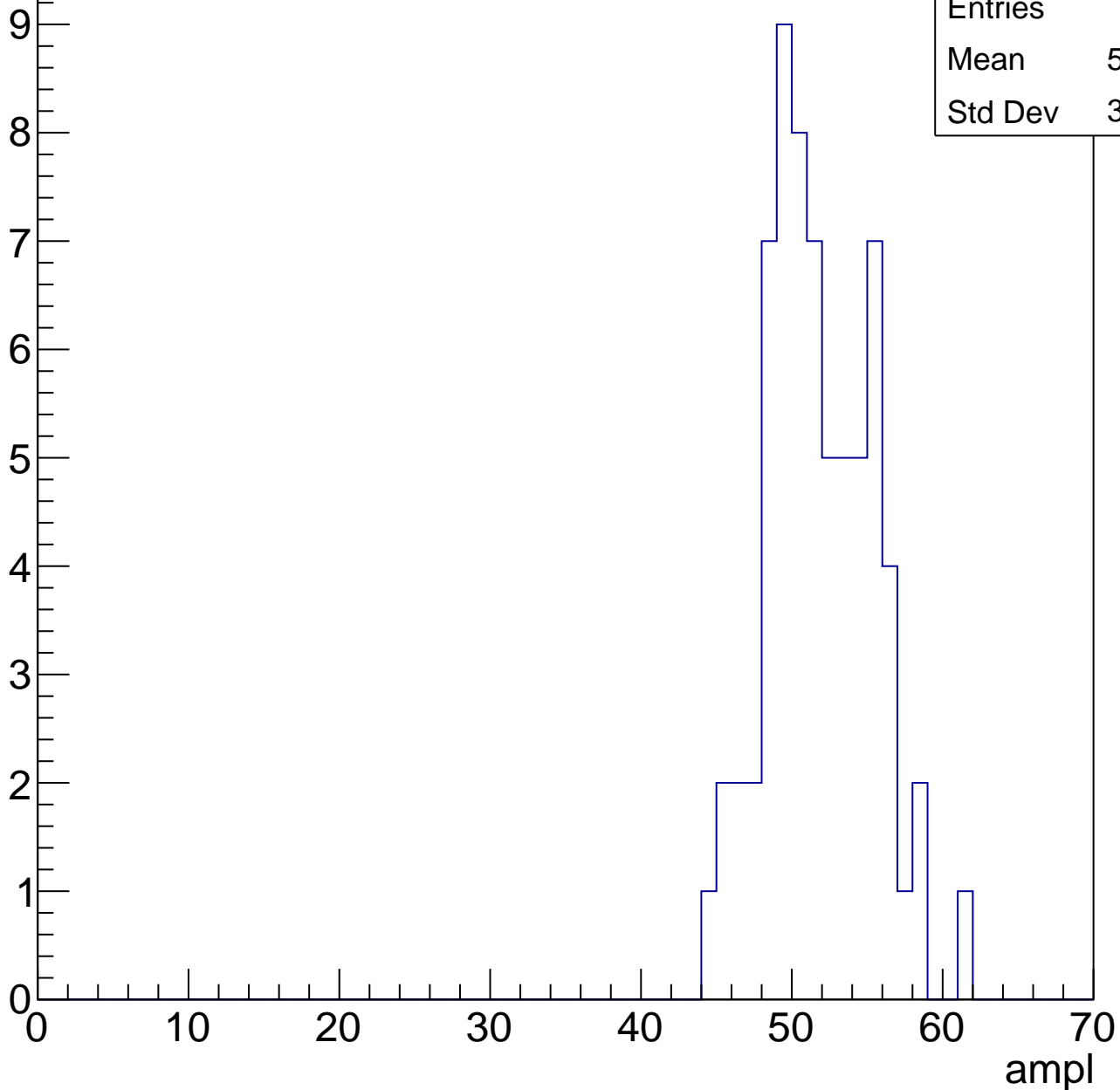


# B1L103S, U26-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	68
Mean	51.35
Std Dev	3.467

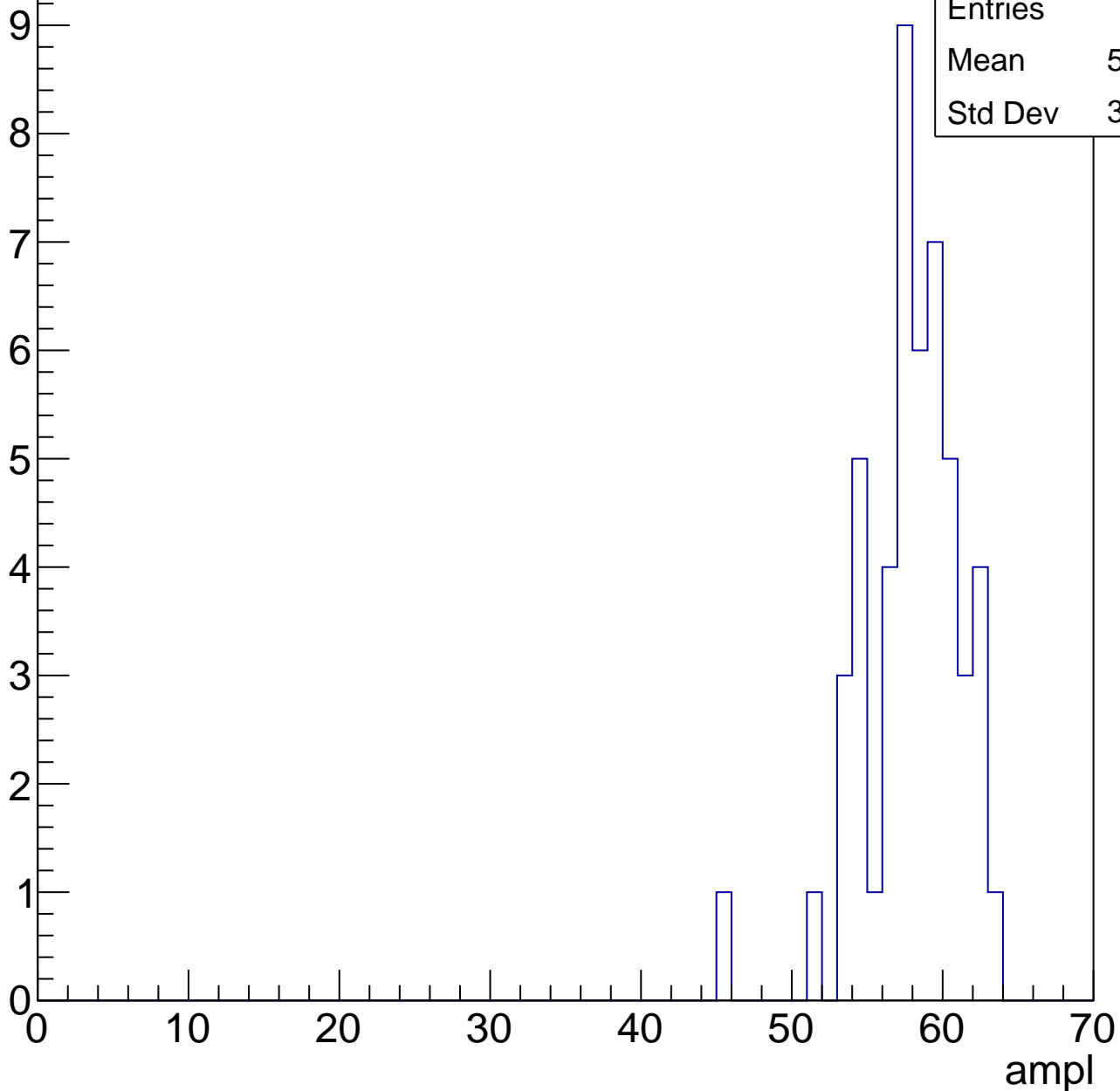


# B1L103S, U26-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	57.44
Std Dev	3.269

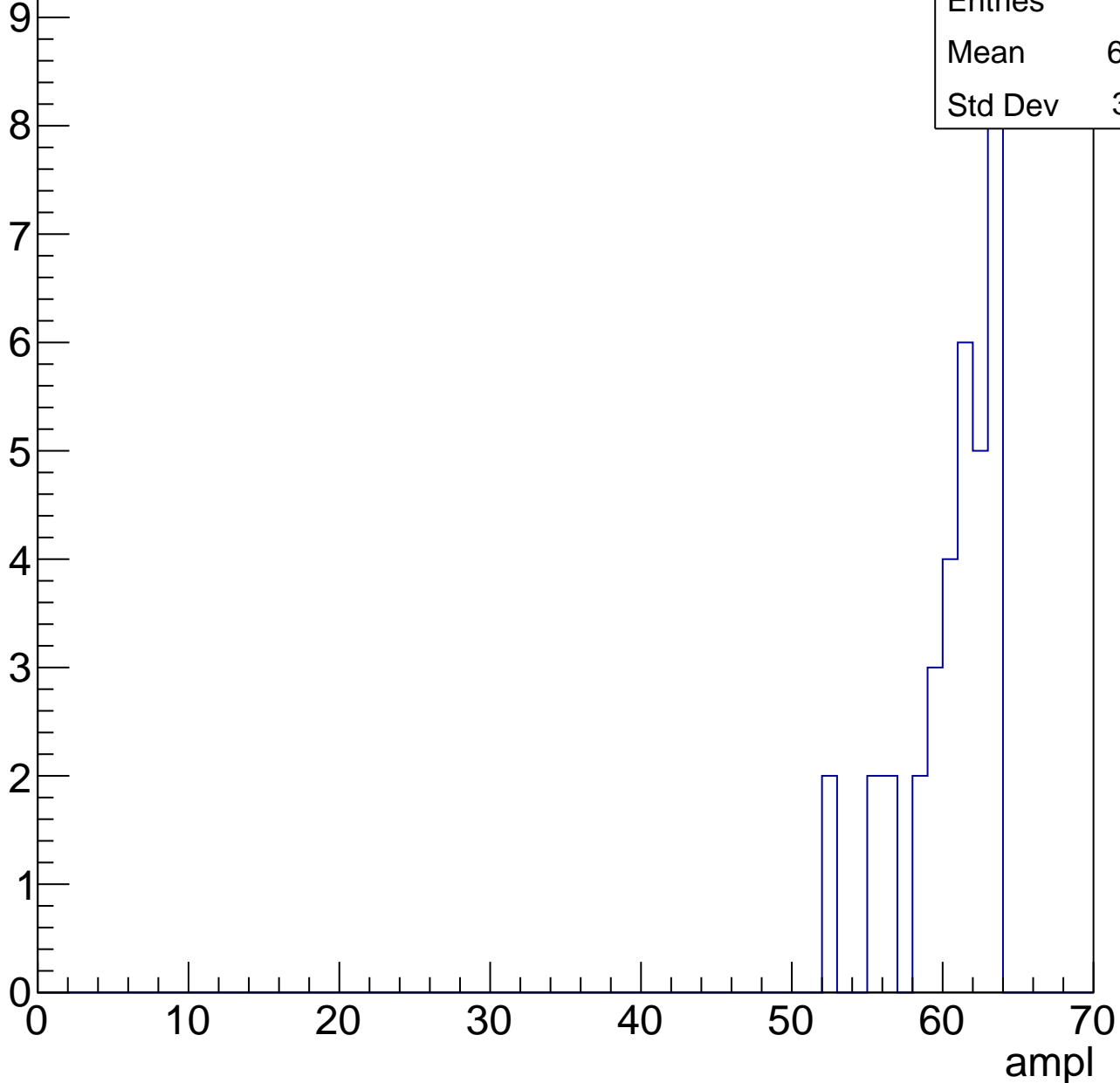


# B1L103S, U26-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

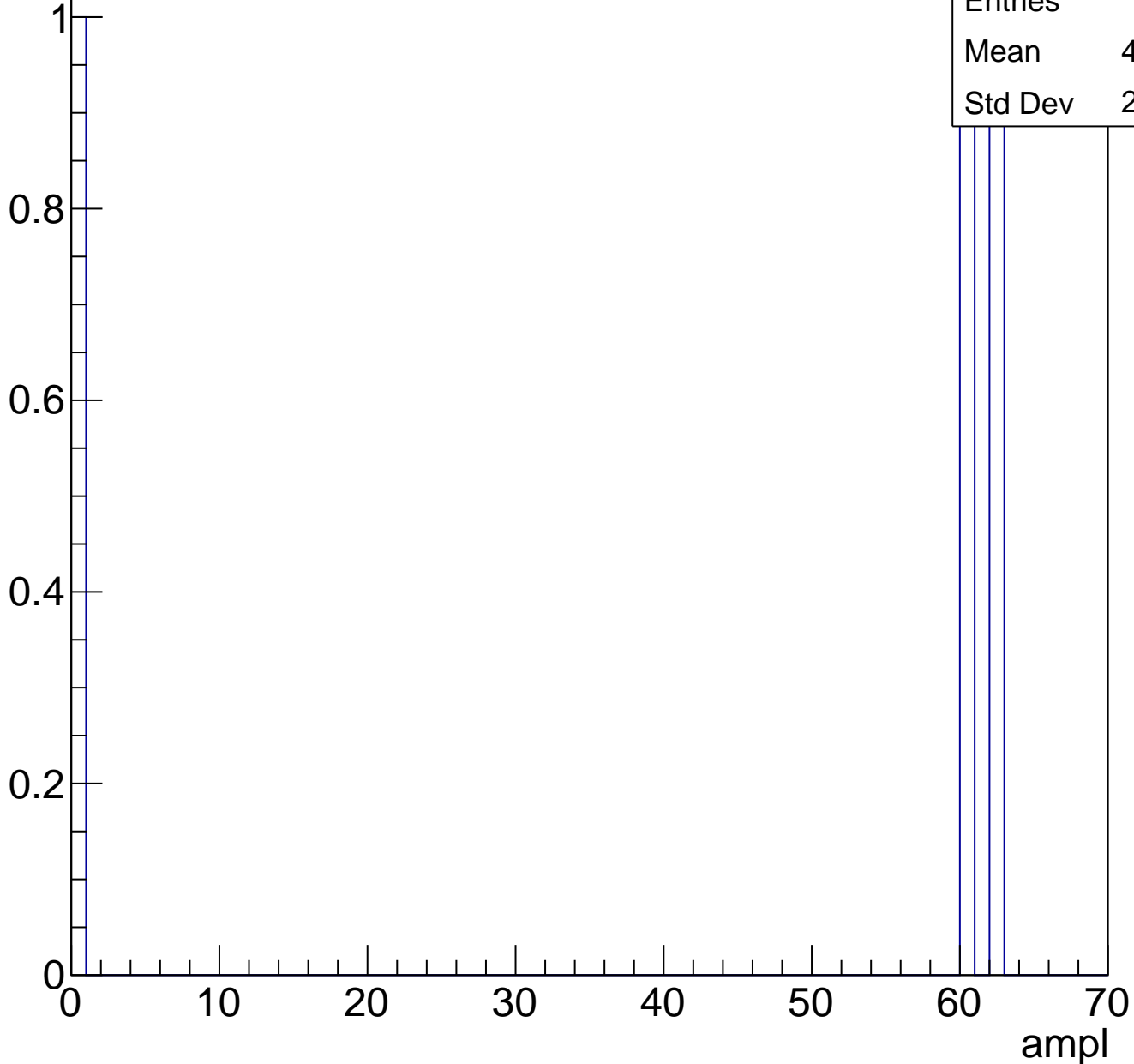
Entries	35
Mean	60.06
Std Dev	3.061



# B1L103S, U26-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch124, adc0

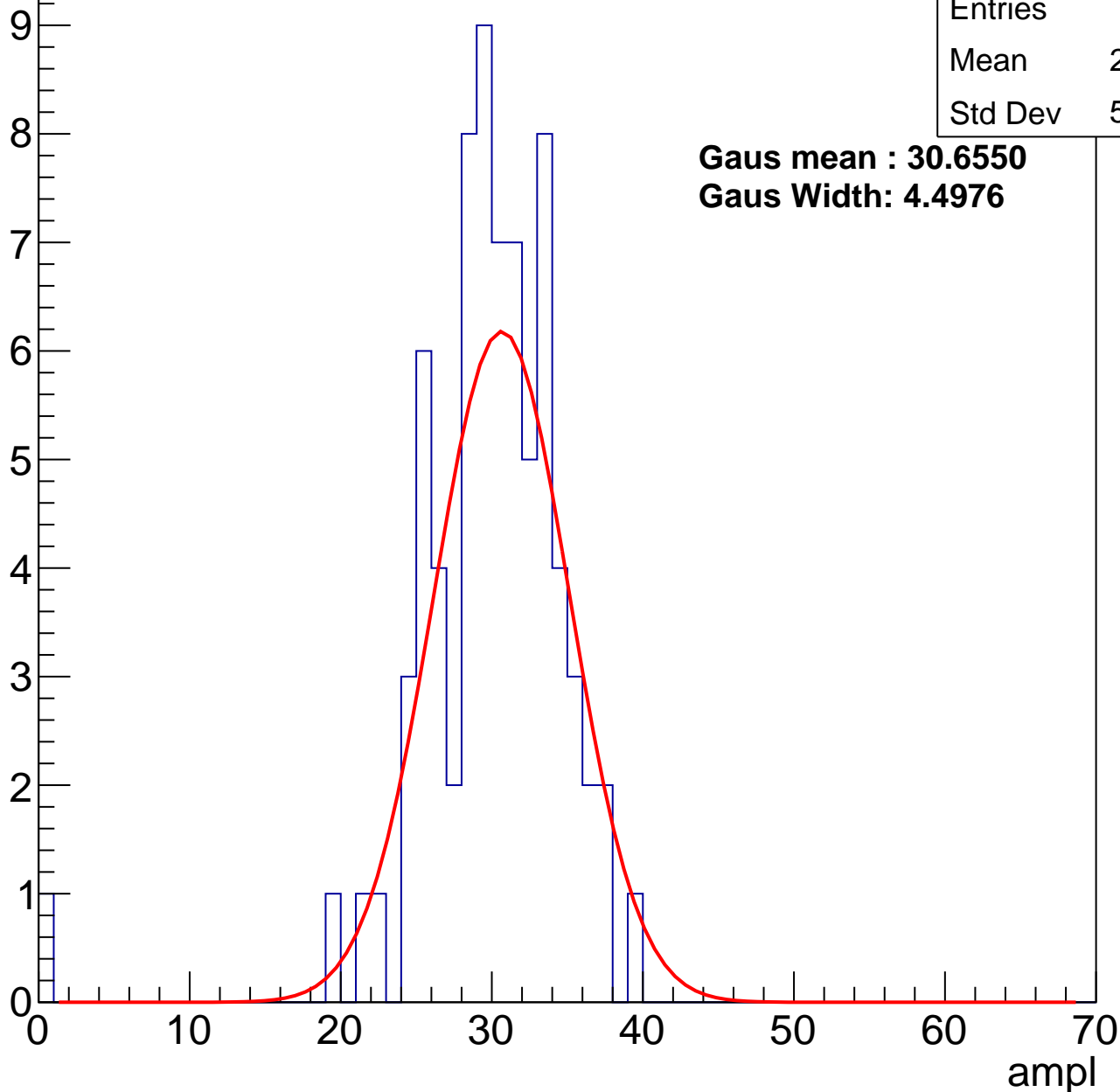
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	29.39
Std Dev	5.174

**Gaus mean : 30.6550**

**Gaus Width: 4.4976**



# B1L103S, U26-ch124, adc1

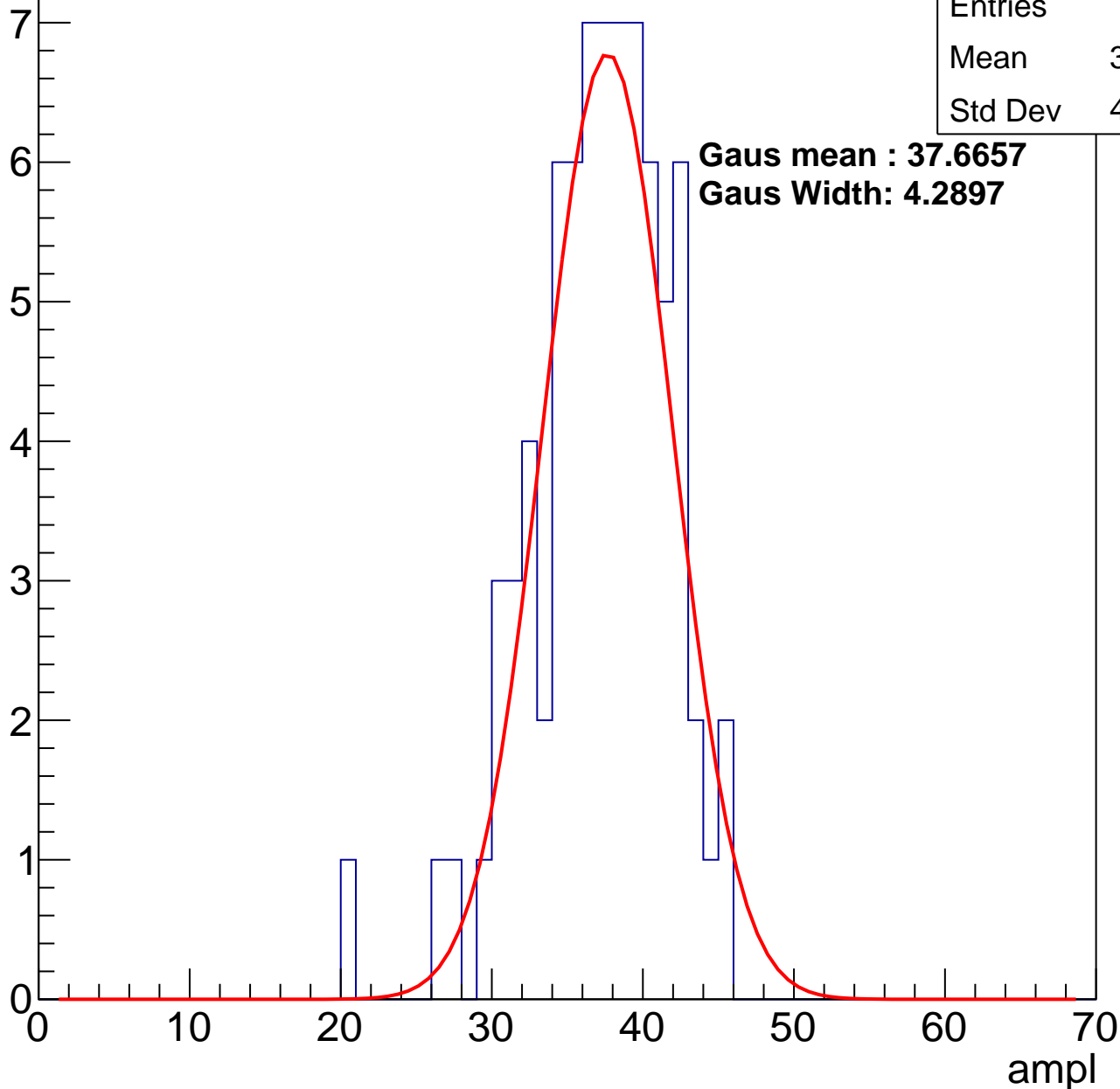
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	78
Mean	36.67
Std Dev	4.537

**Gaus mean : 37.6657**

**Gaus Width: 4.2897**



# B1L103S, U26-ch124, adc2

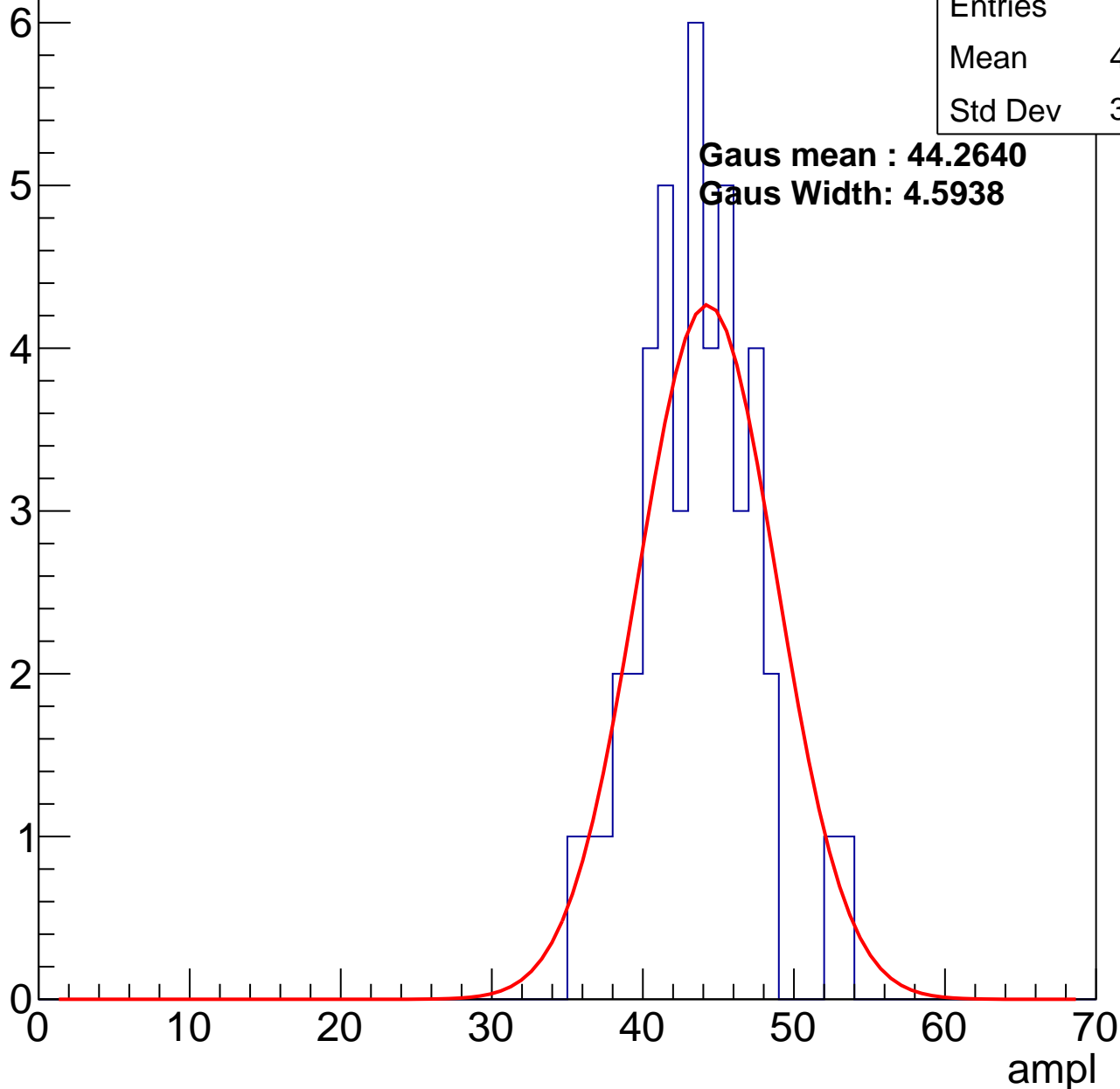
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	45
Mean	43.09
Std Dev	3.758

**Gaus mean : 44.2640**

**Gaus Width: 4.5938**

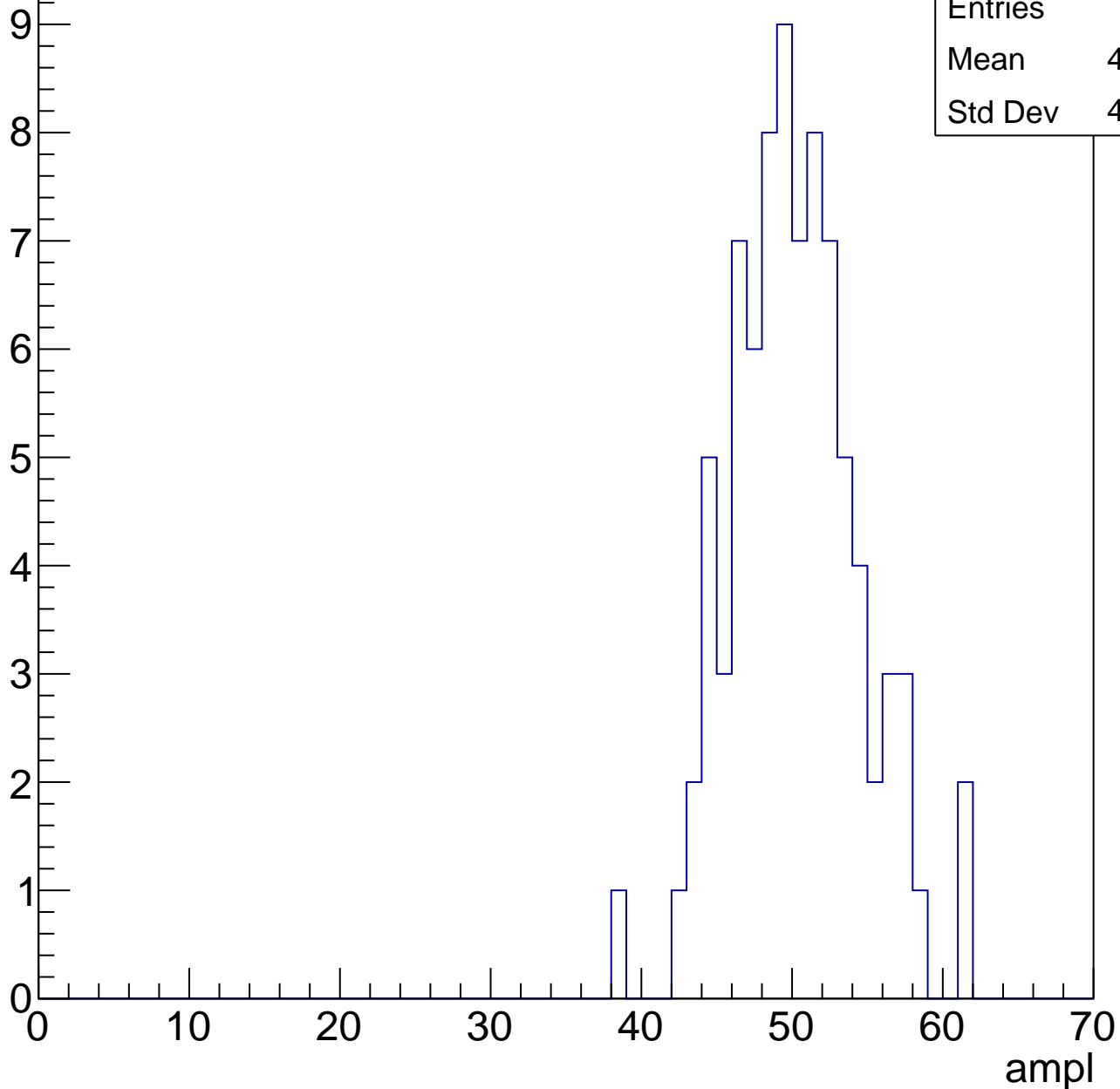


# B1L103S, U26-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	84
Mean	49.79
Std Dev	4.254

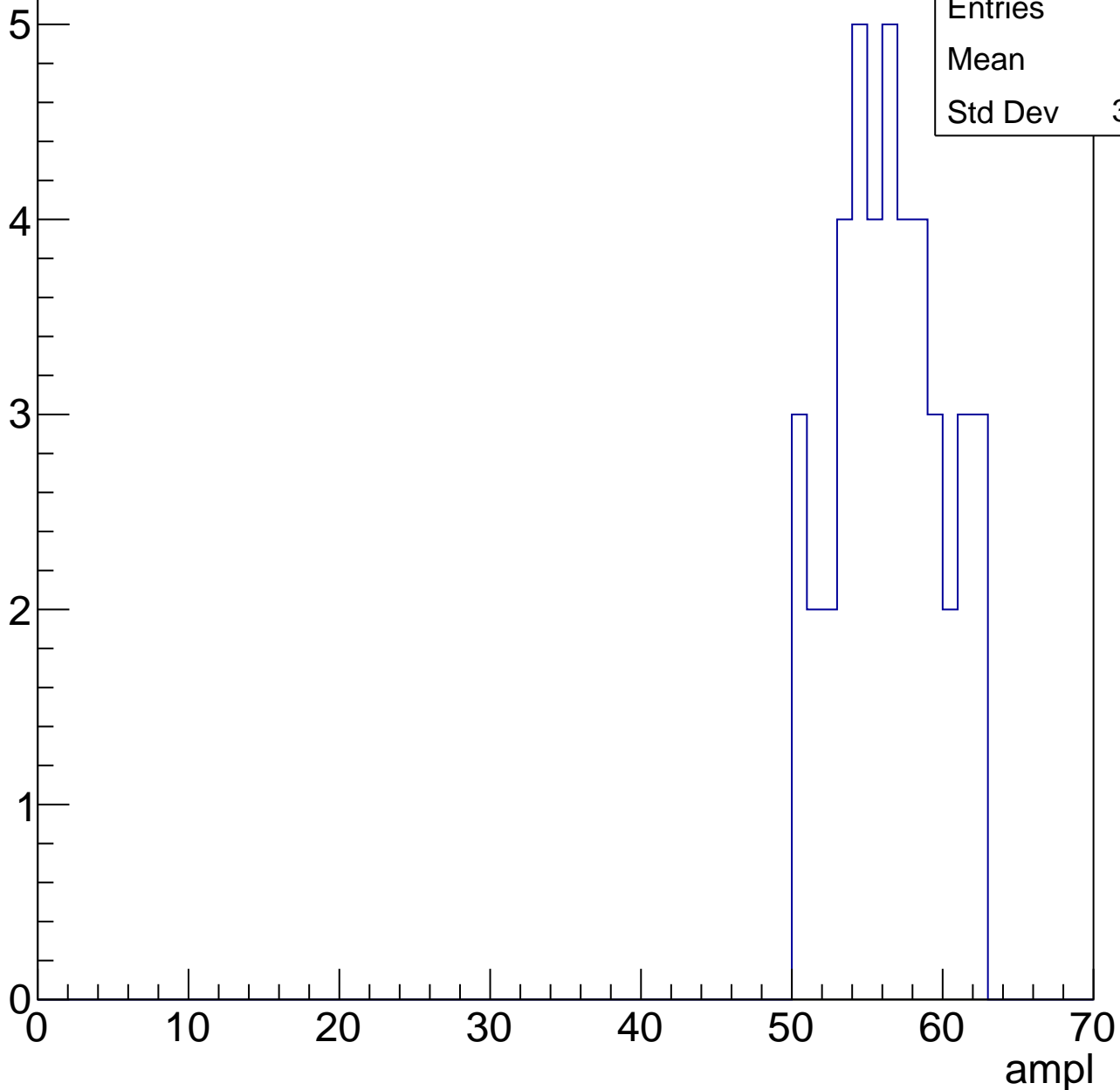


# B1L103S, U26-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	56
Std Dev	3.411

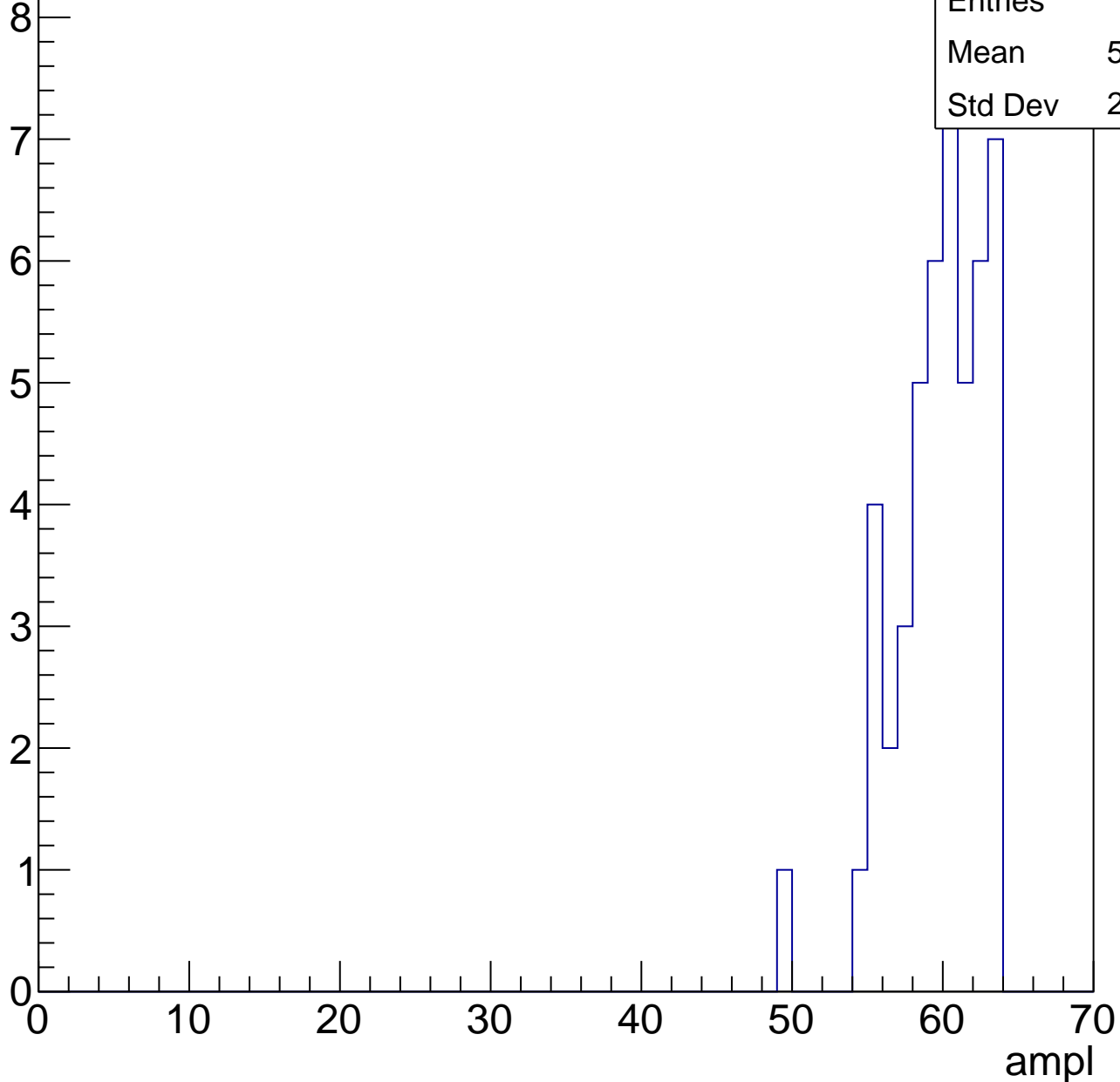


# B1L103S, U26-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	48
Mean	59.33
Std Dev	2.932



# B1L103S, U26-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L103S, U26-ch125, adc0

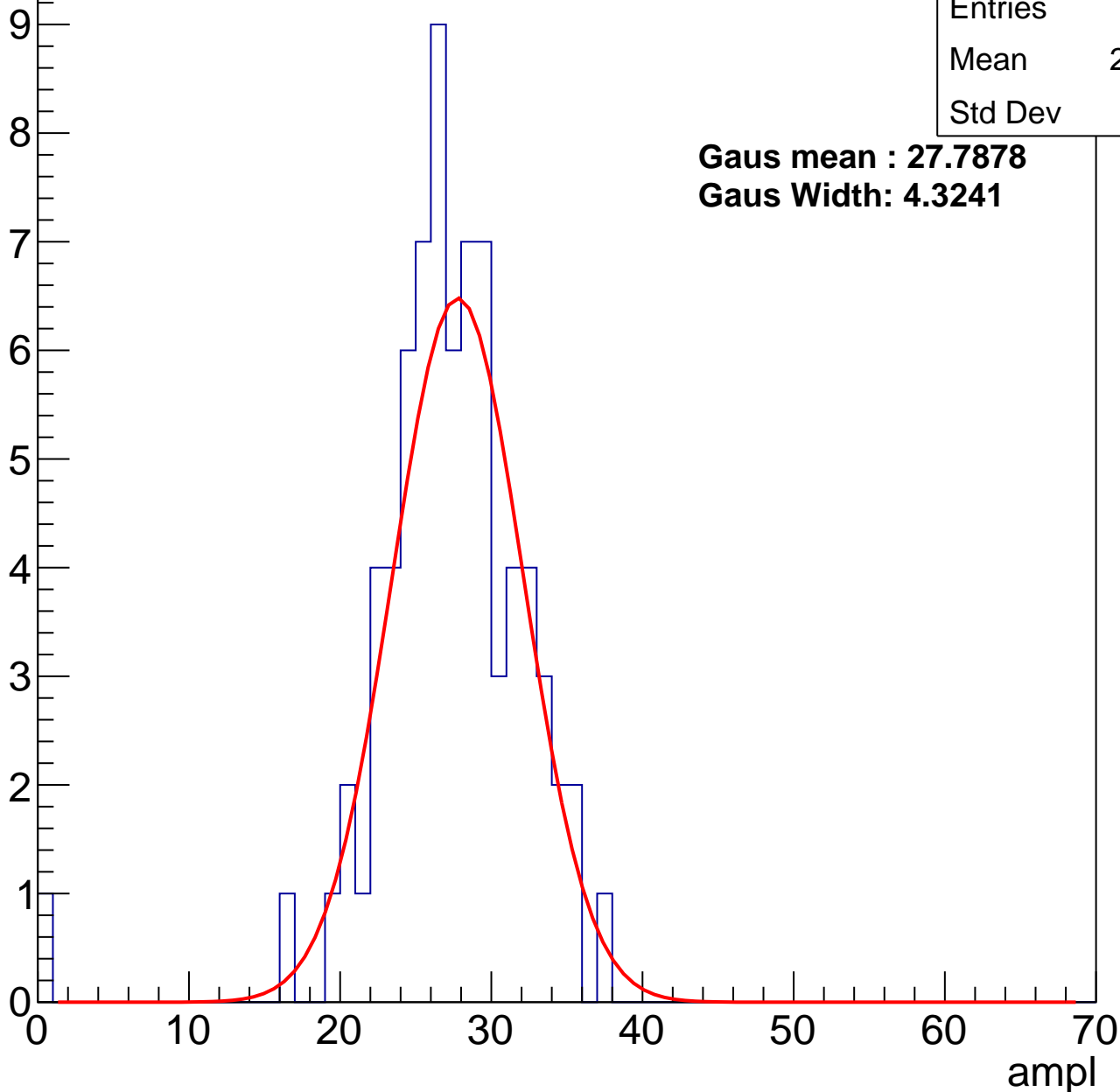
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	75
Mean	26.75
Std Dev	5.11

**Gaus mean : 27.7878**

**Gaus Width: 4.3241**



# B1L103S, U26-ch125, adc1

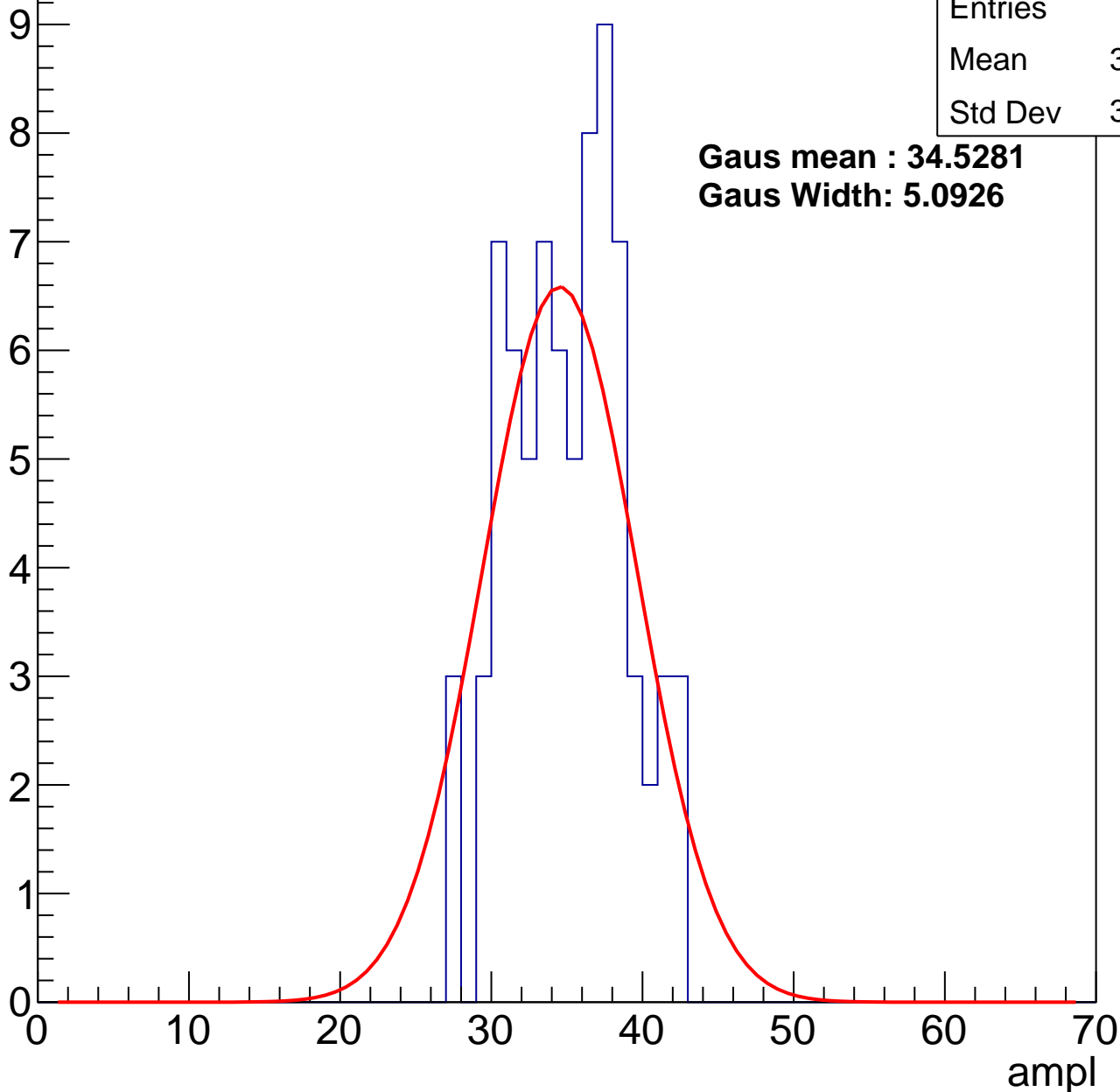
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	77
Mean	34.64
Std Dev	3.779

**Gaus mean : 34.5281**

**Gaus Width: 5.0926**



# B1L103S, U26-ch125, adc2

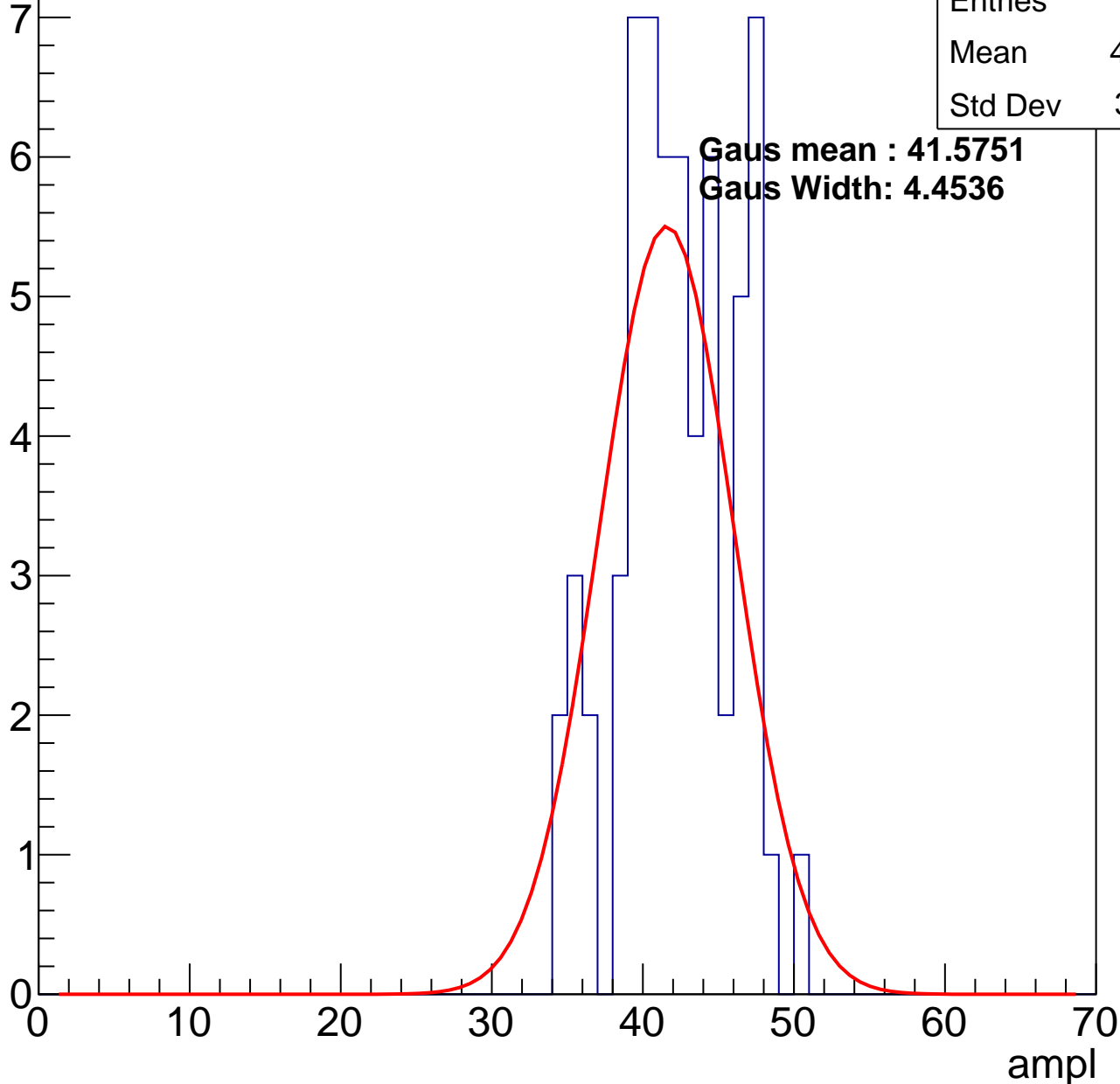
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	62
Mean	41.82
Std Dev	3.791

**Gaus mean : 41.5751**

**Gaus Width: 4.4536**

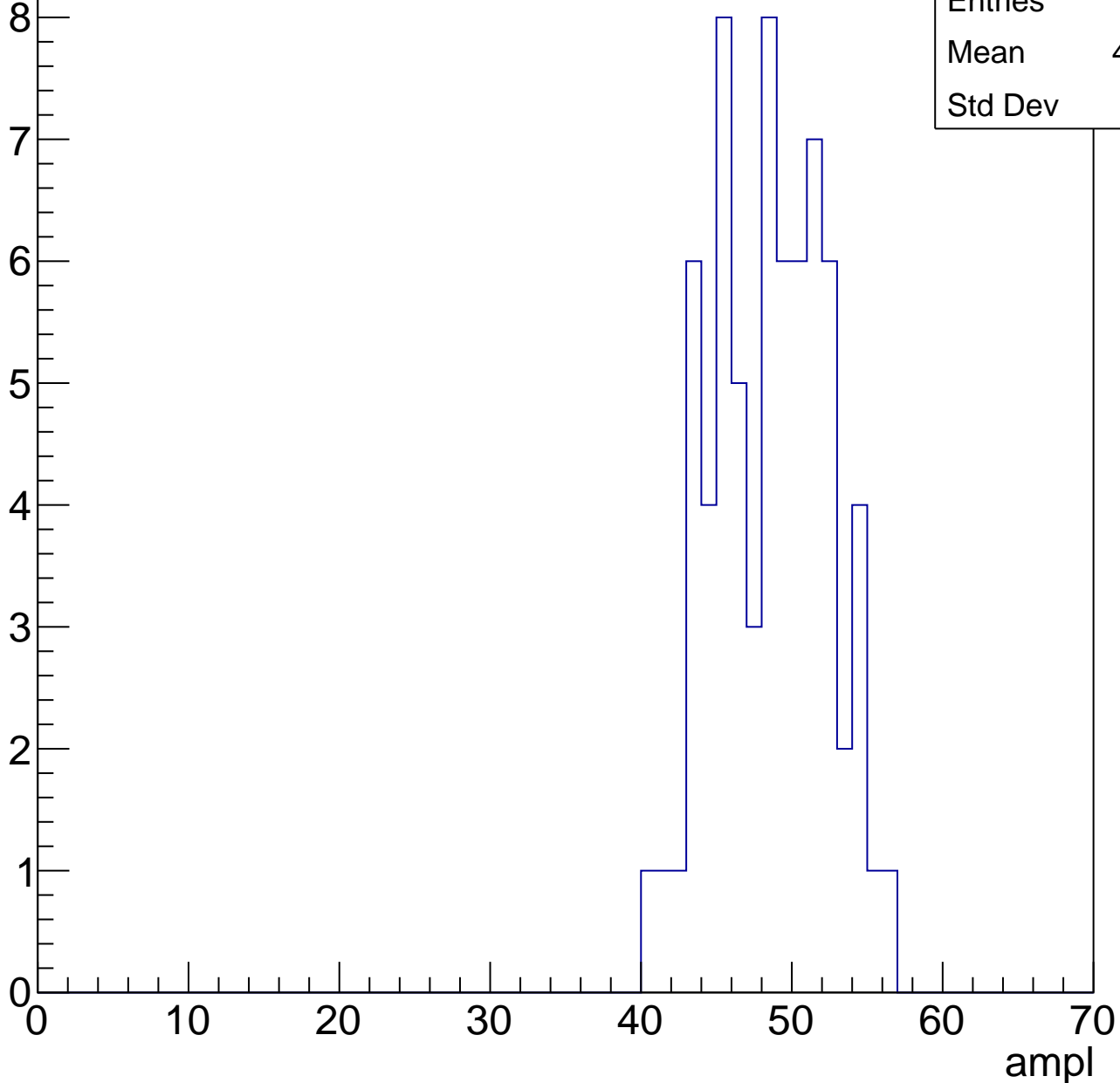


# B1L103S, U26-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

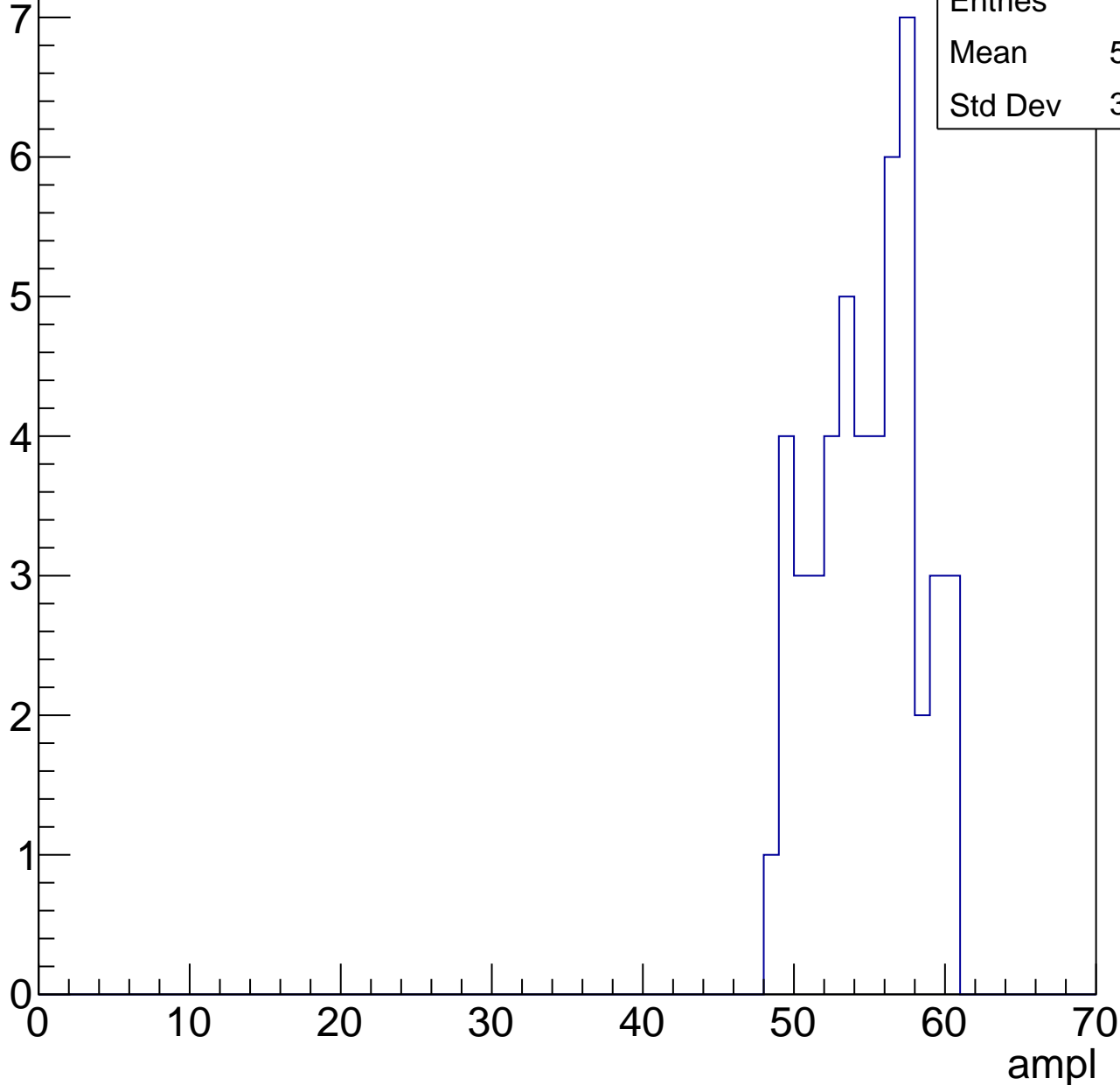
Entries	70
Mean	48.11
Std Dev	3.69



# B1L103S, U26-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

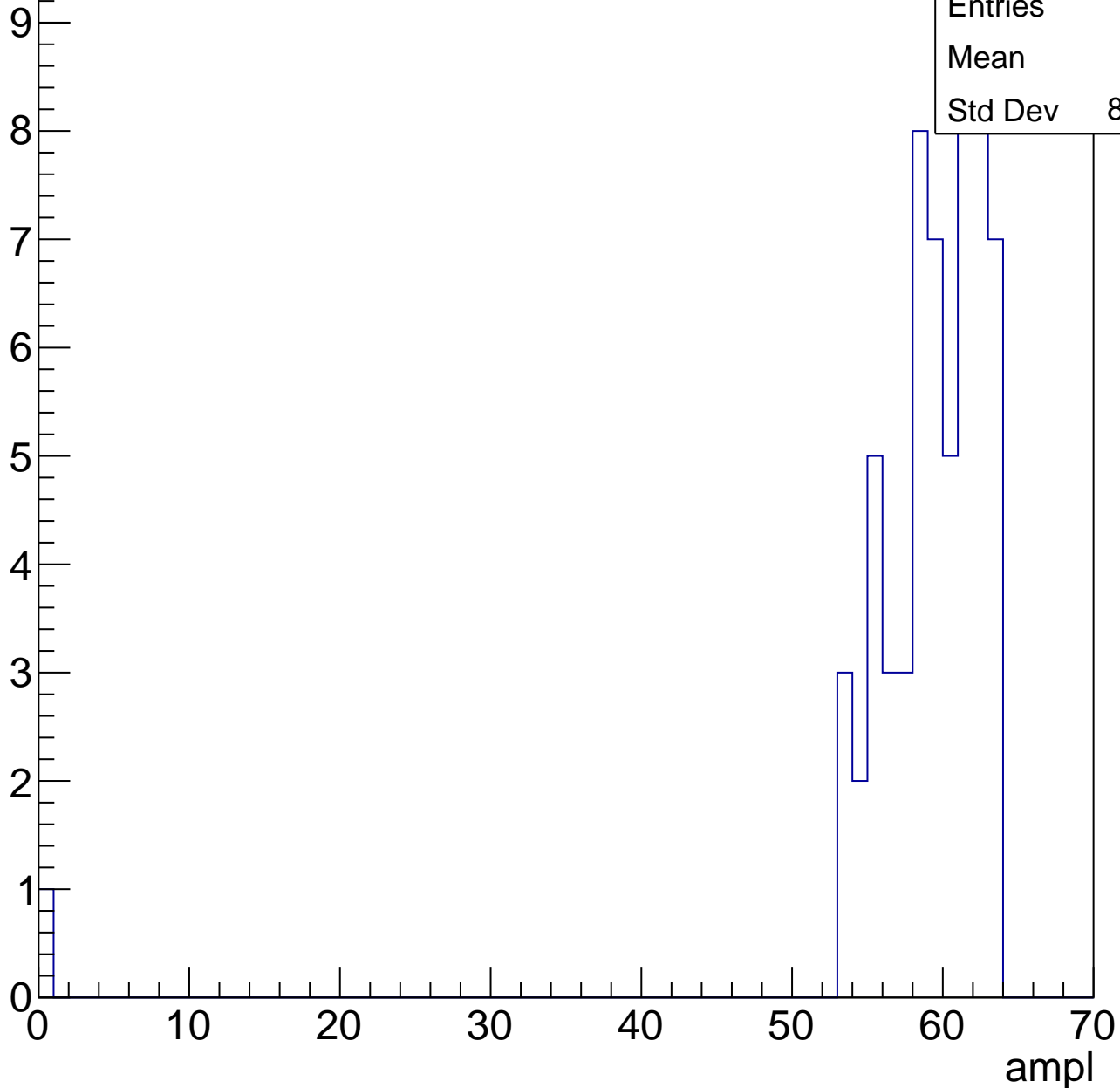
Entry



# B1L103S, U26-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

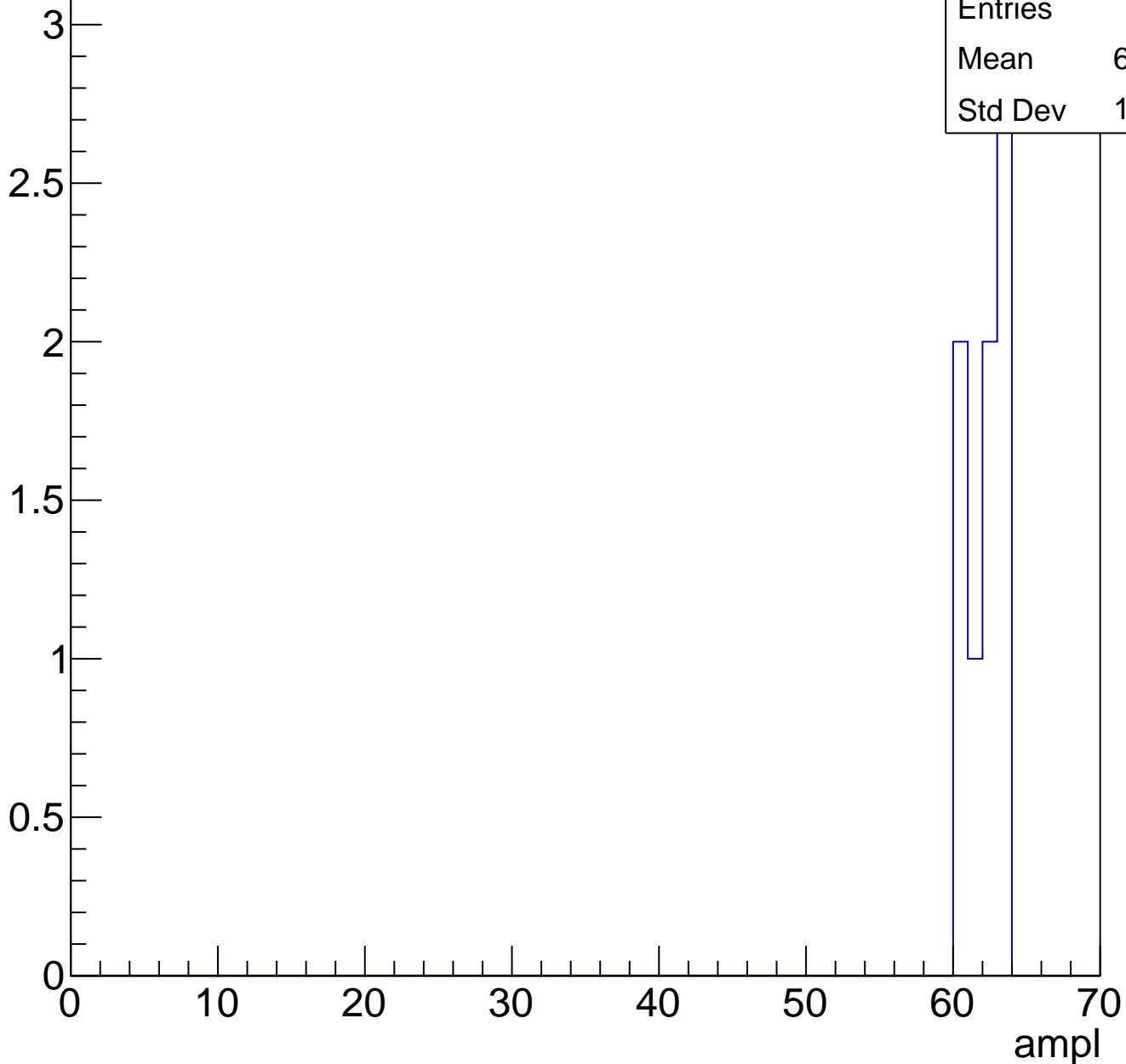
Entry



# B1L103S, U26-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch126, adc0

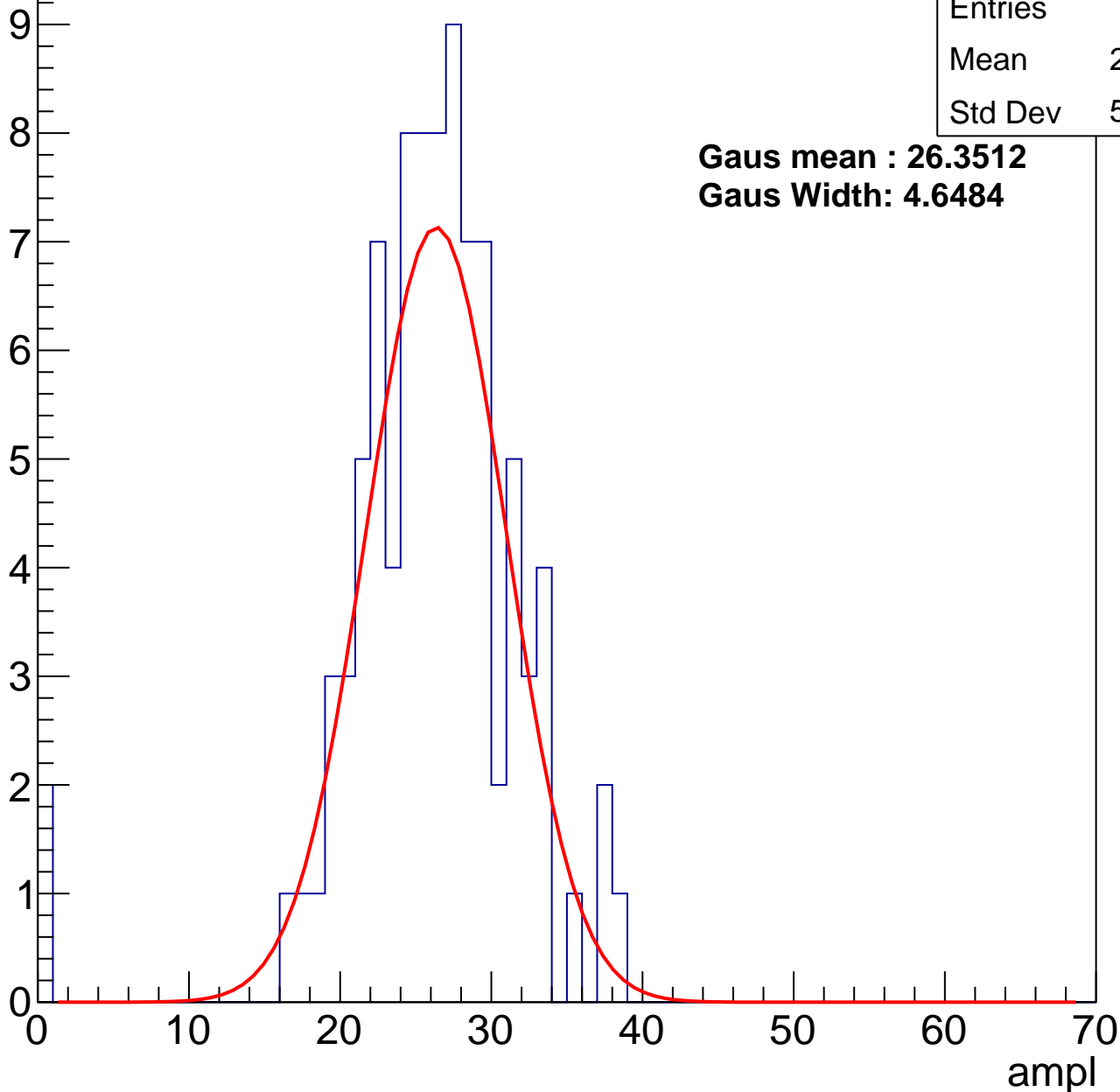
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	92
Mean	25.55
Std Dev	5.874

**Gaus mean : 26.3512**

**Gaus Width: 4.6484**



# B1L103S, U26-ch126, adc1

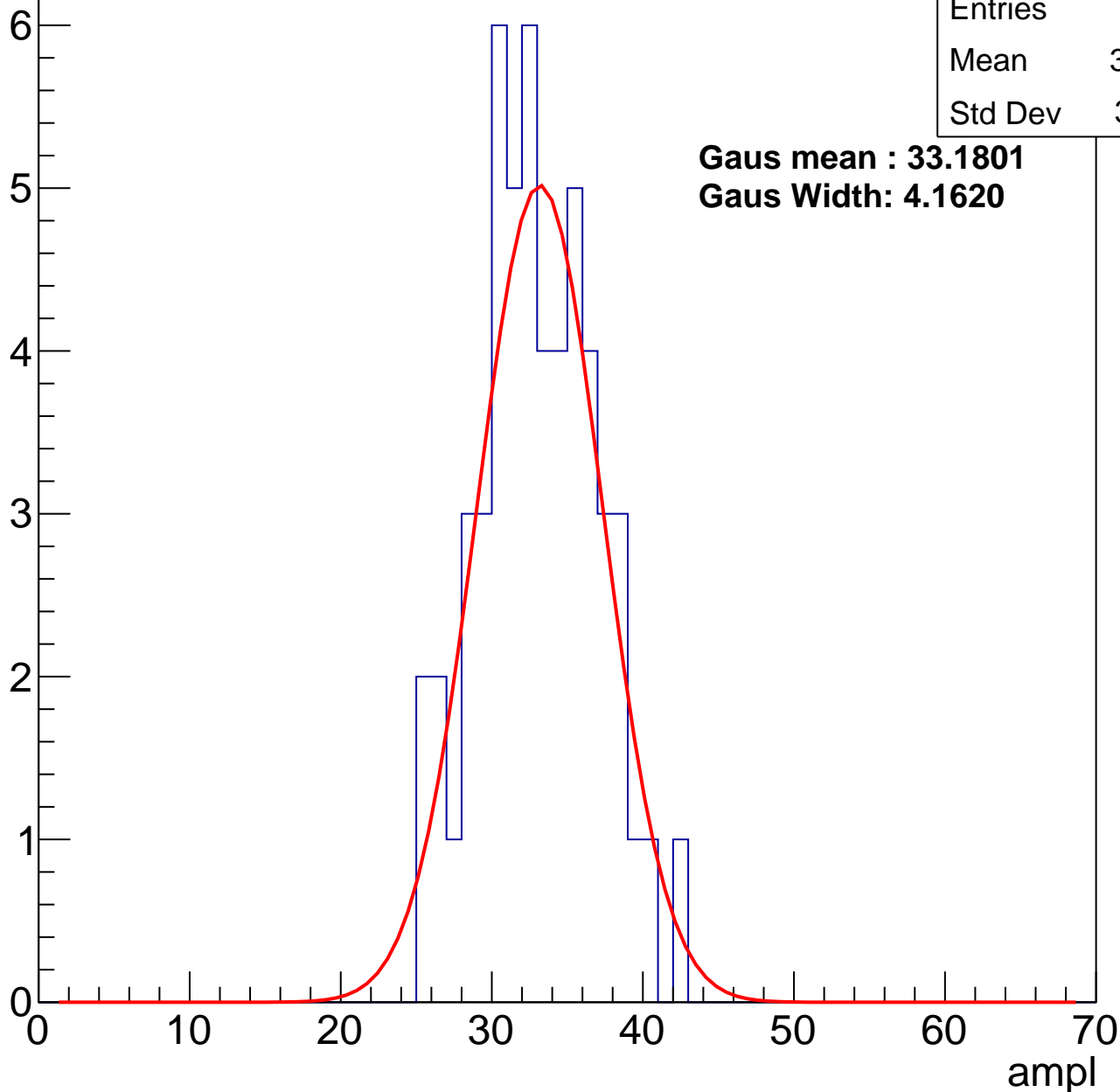
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	54
Mean	32.59
Std Dev	3.861

**Gaus mean : 33.1801**

**Gaus Width: 4.1620**



# B1L103S, U26-ch126, adc2

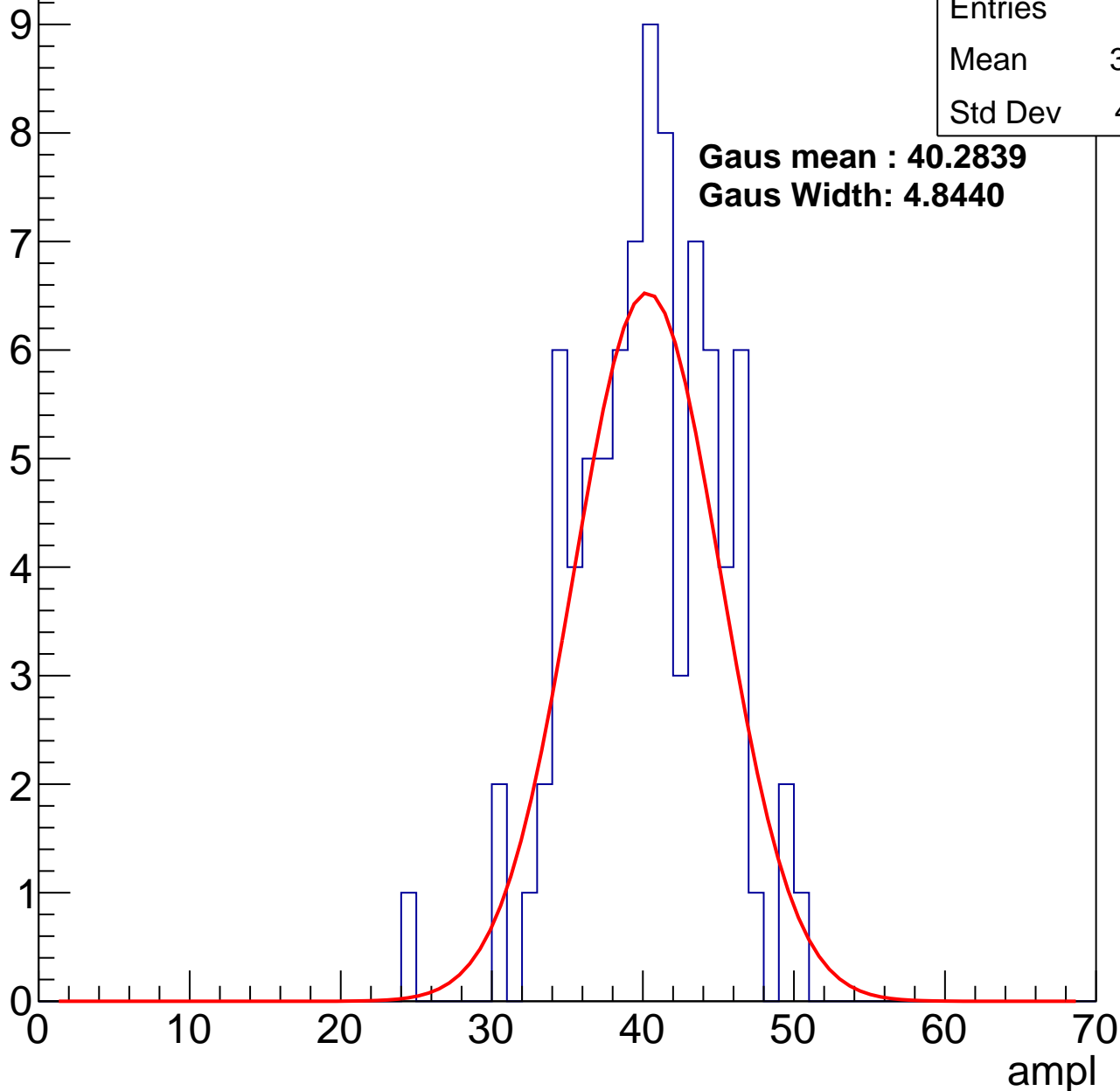
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	86
Mean	39.79
Std Dev	4.691

**Gaus mean : 40.2839**

**Gaus Width: 4.8440**

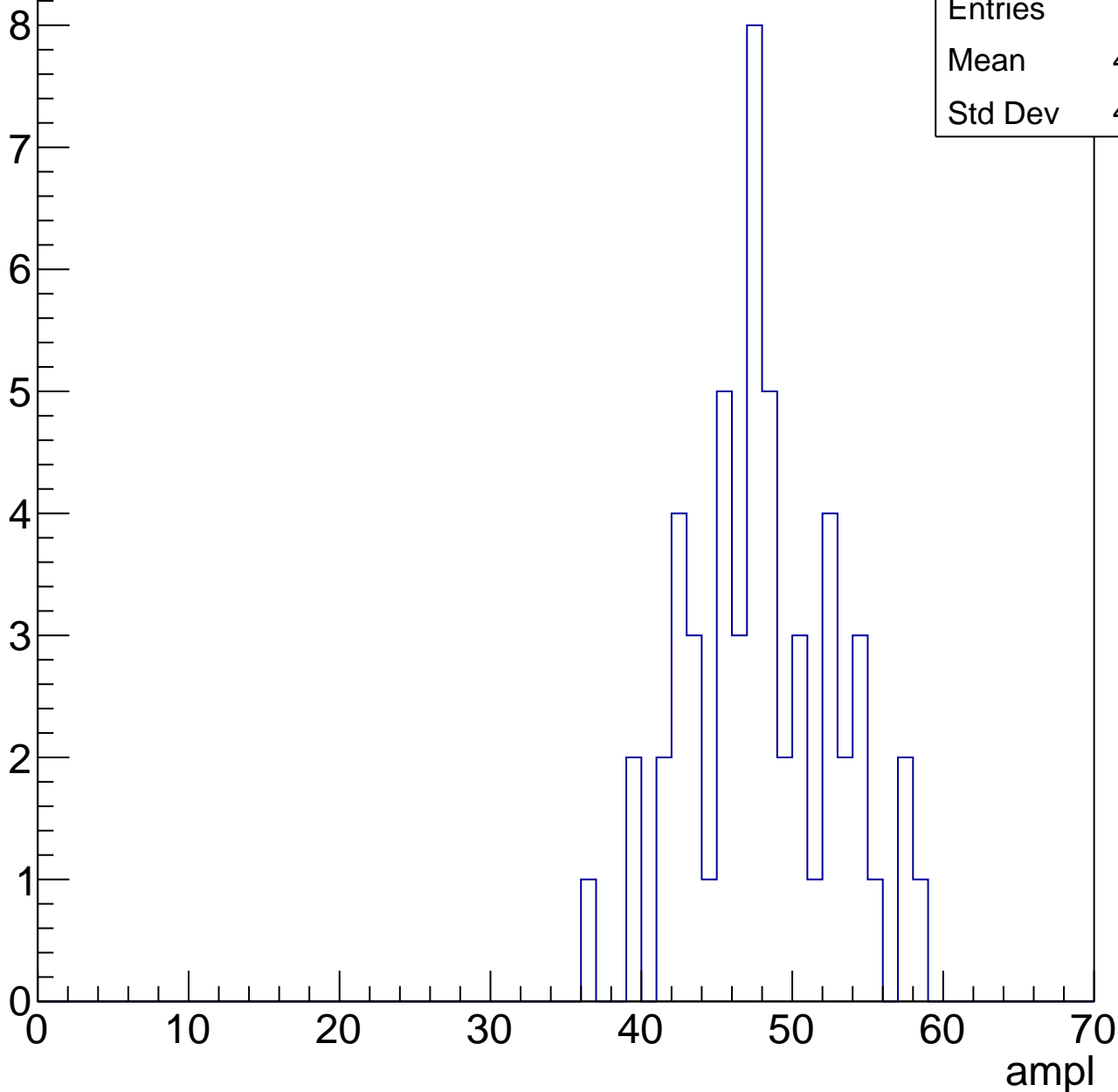


# B1L103S, U26-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	53
Mean	47.51
Std Dev	4.851

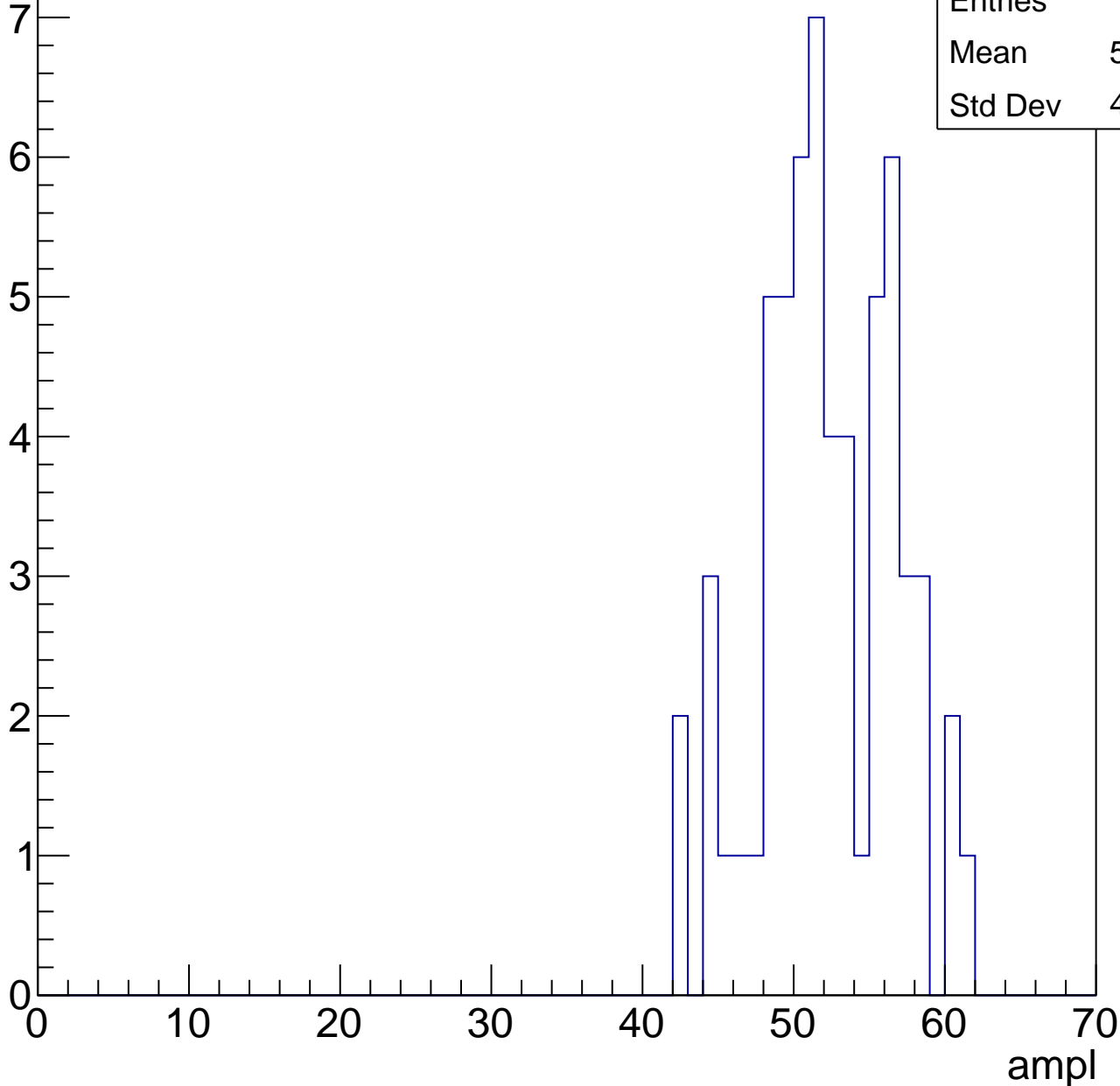


# B1L103S, U26-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	60
Mean	51.78
Std Dev	4.465

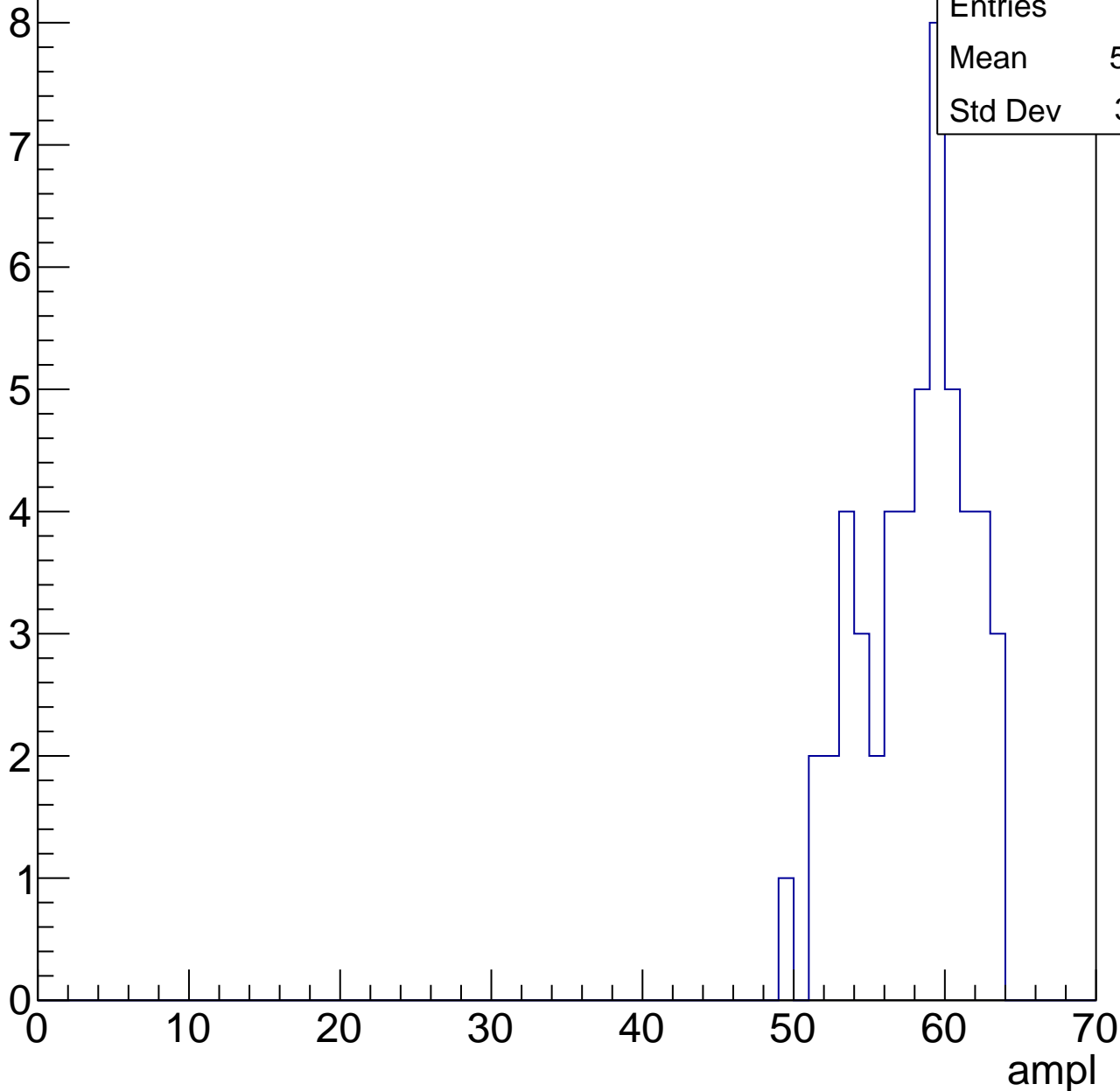


# B1L103S, U26-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	51
Mean	57.53
Std Dev	3.511

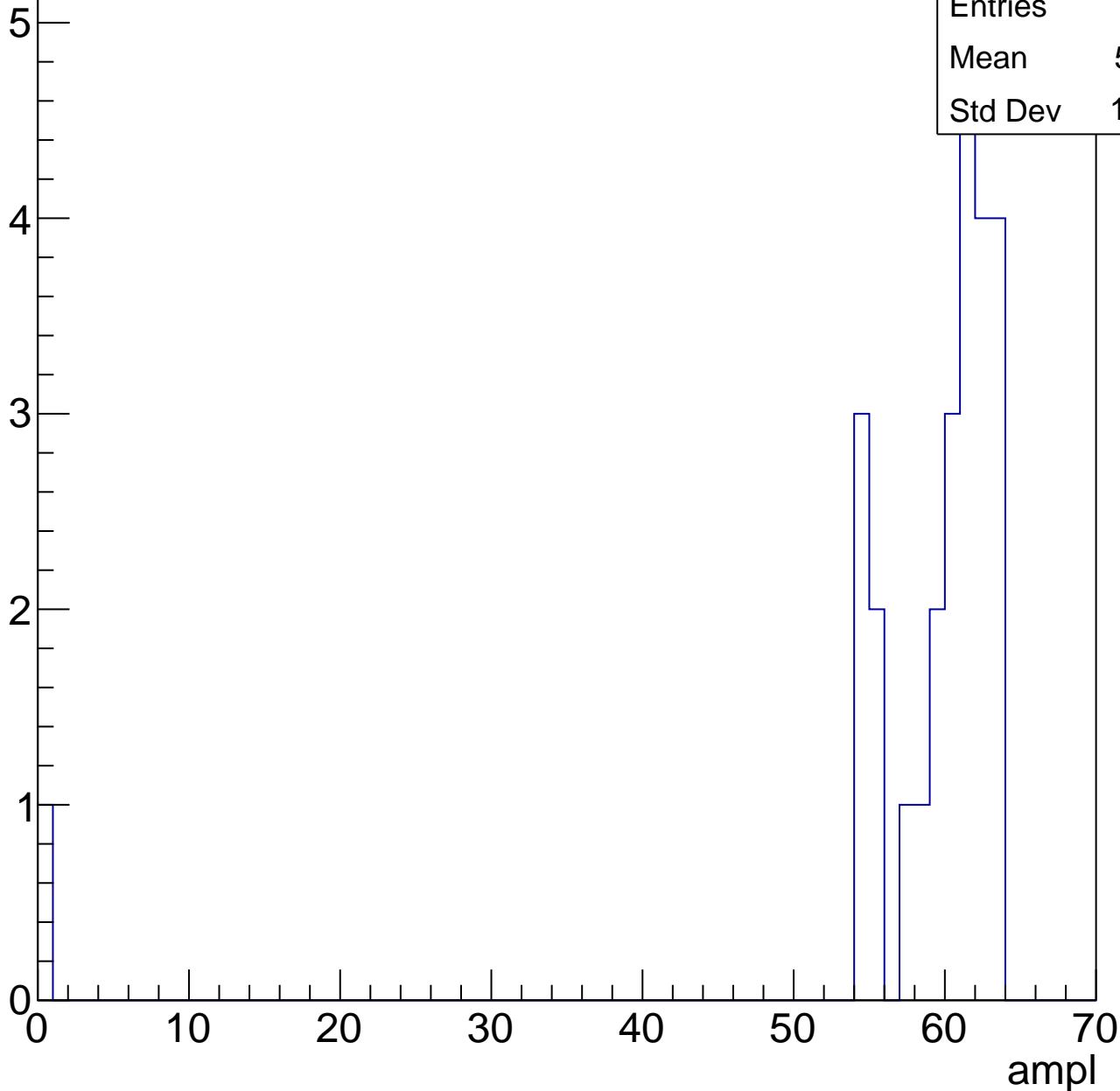


# B1L103S, U26-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	26
Mean	57.31
Std Dev	11.83

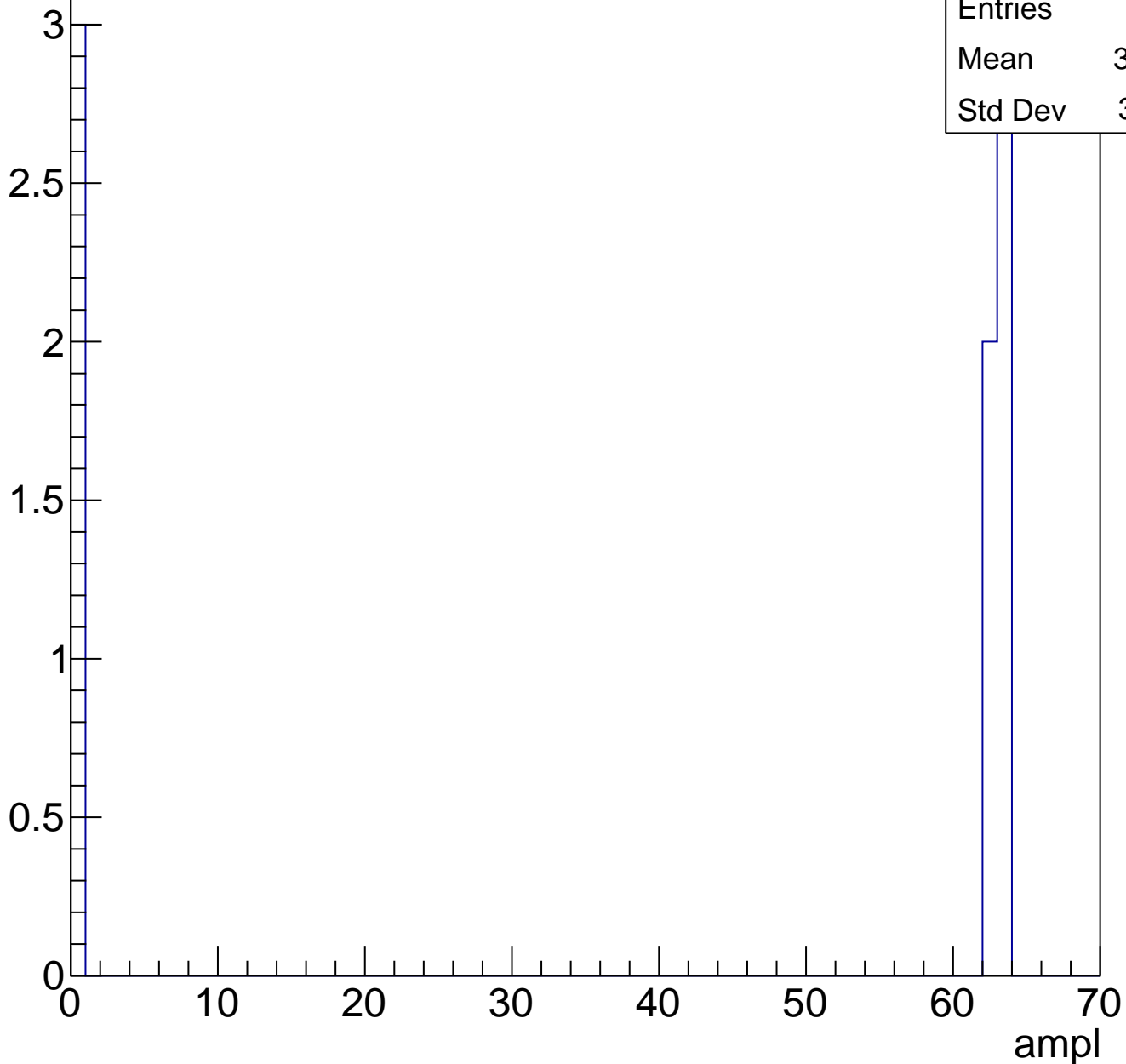




# B1L103S, U26-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch127, adc0

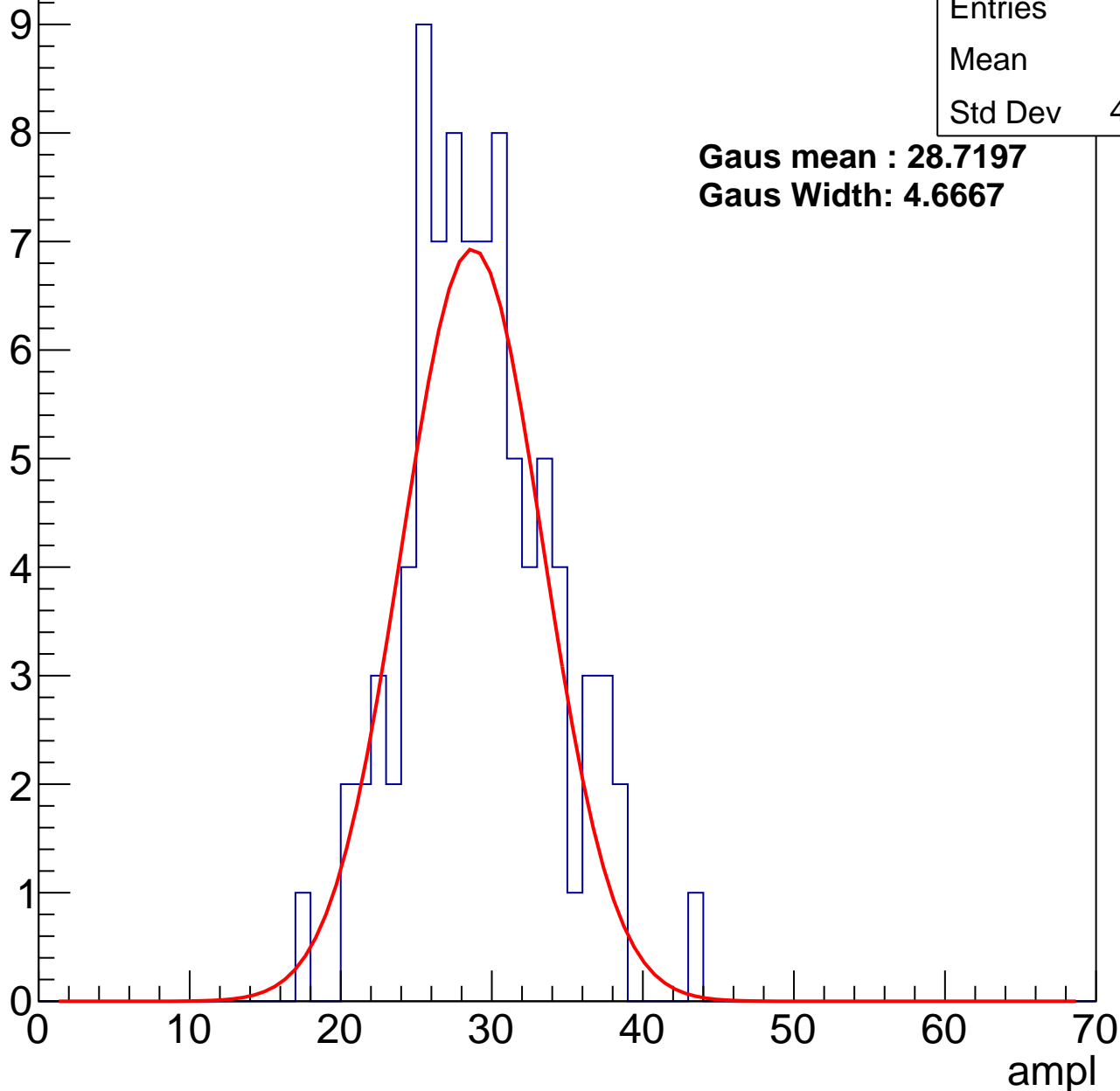
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	88
Mean	28.7
Std Dev	4.729

**Gaus mean : 28.7197**

**Gaus Width: 4.6667**



# B1L103S, U26-ch127, adc1

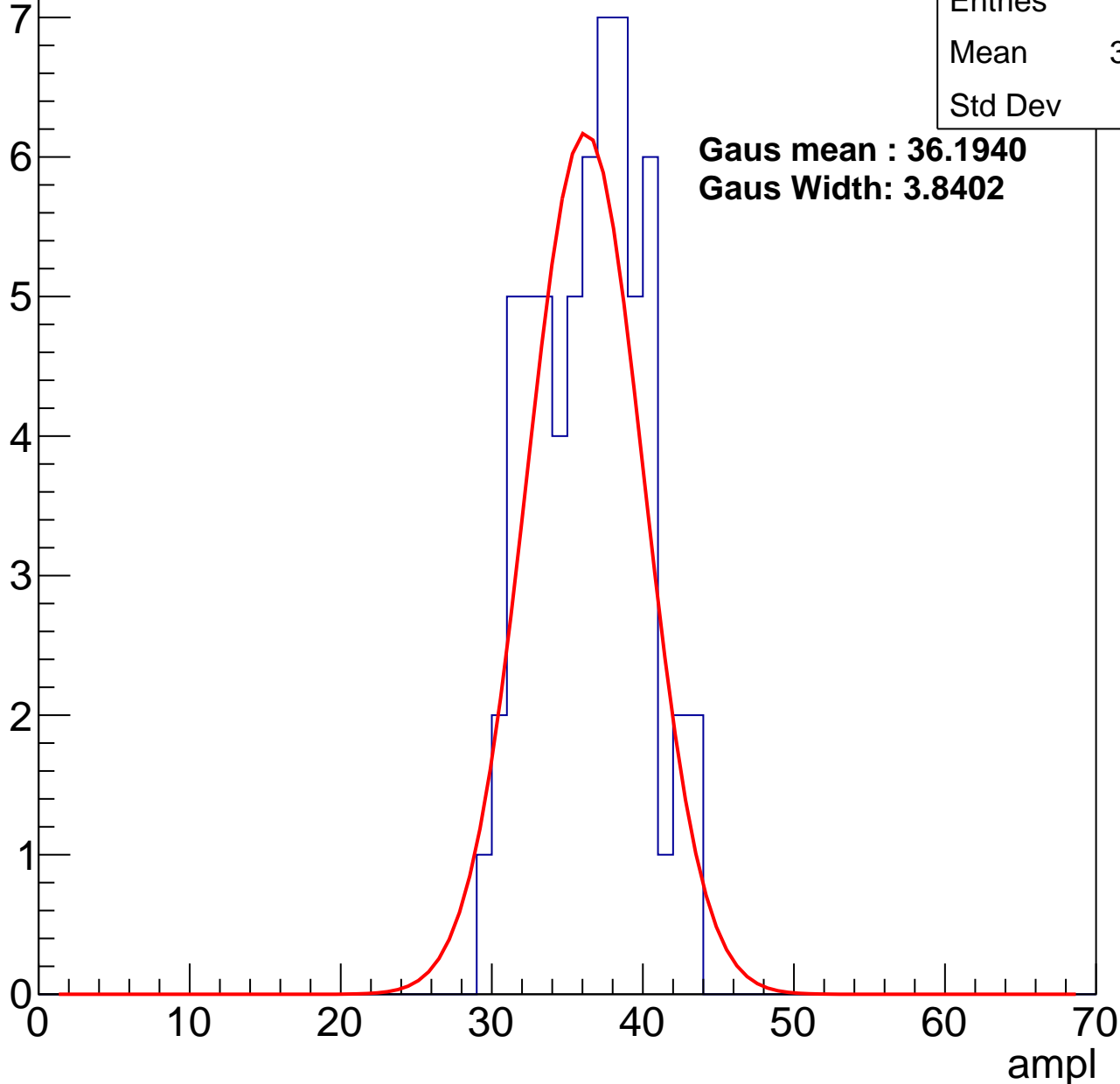
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	63
Mean	35.98
Std Dev	3.48

**Gaus mean : 36.1940**

**Gaus Width: 3.8402**



# B1L103S, U26-ch127, adc2

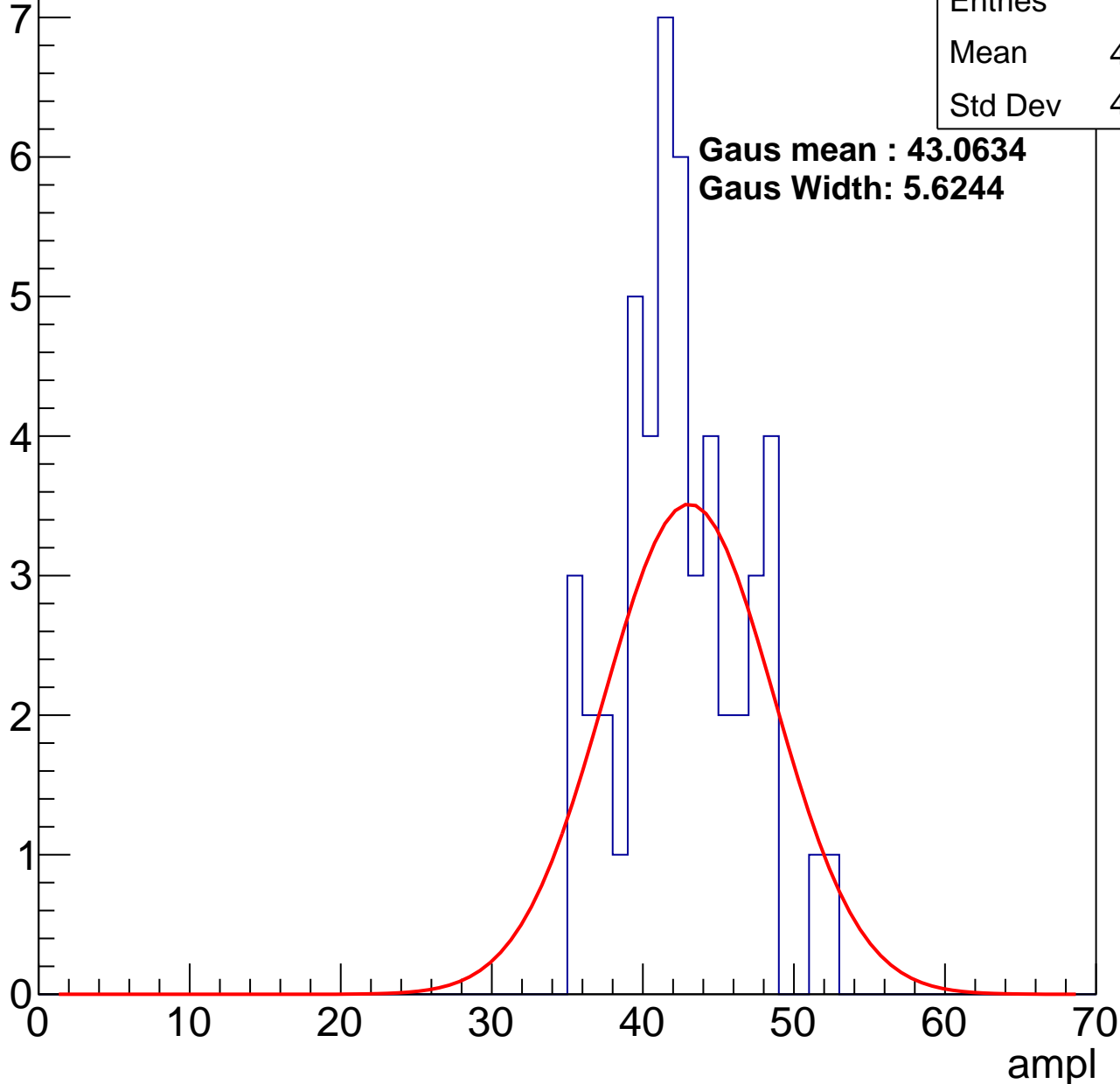
calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	50
Mean	42.12
Std Dev	4.053

**Gaus mean : 43.0634**

**Gaus Width: 5.6244**

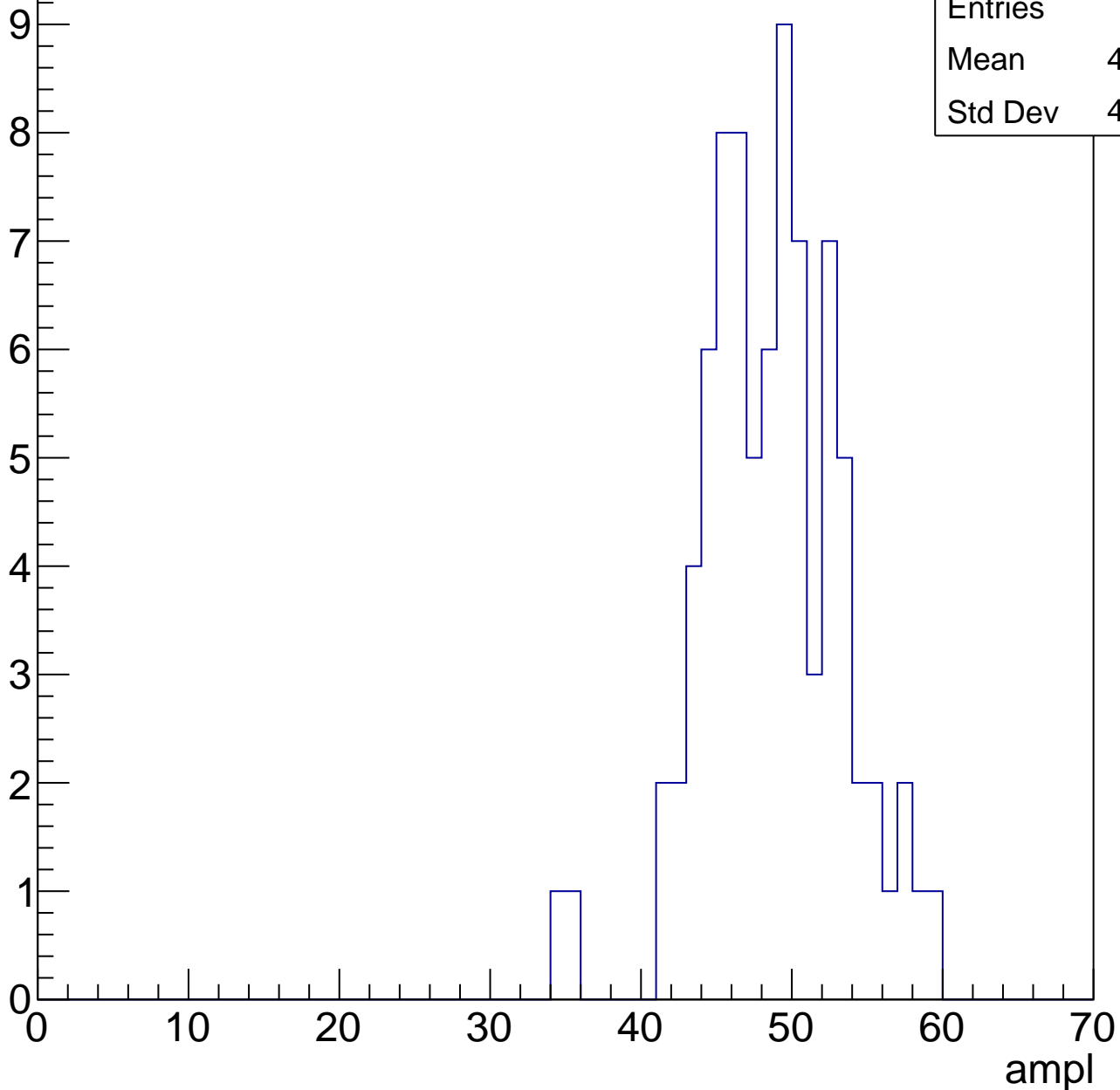


# B1L103S, U26-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	83
Mean	48.19
Std Dev	4.598

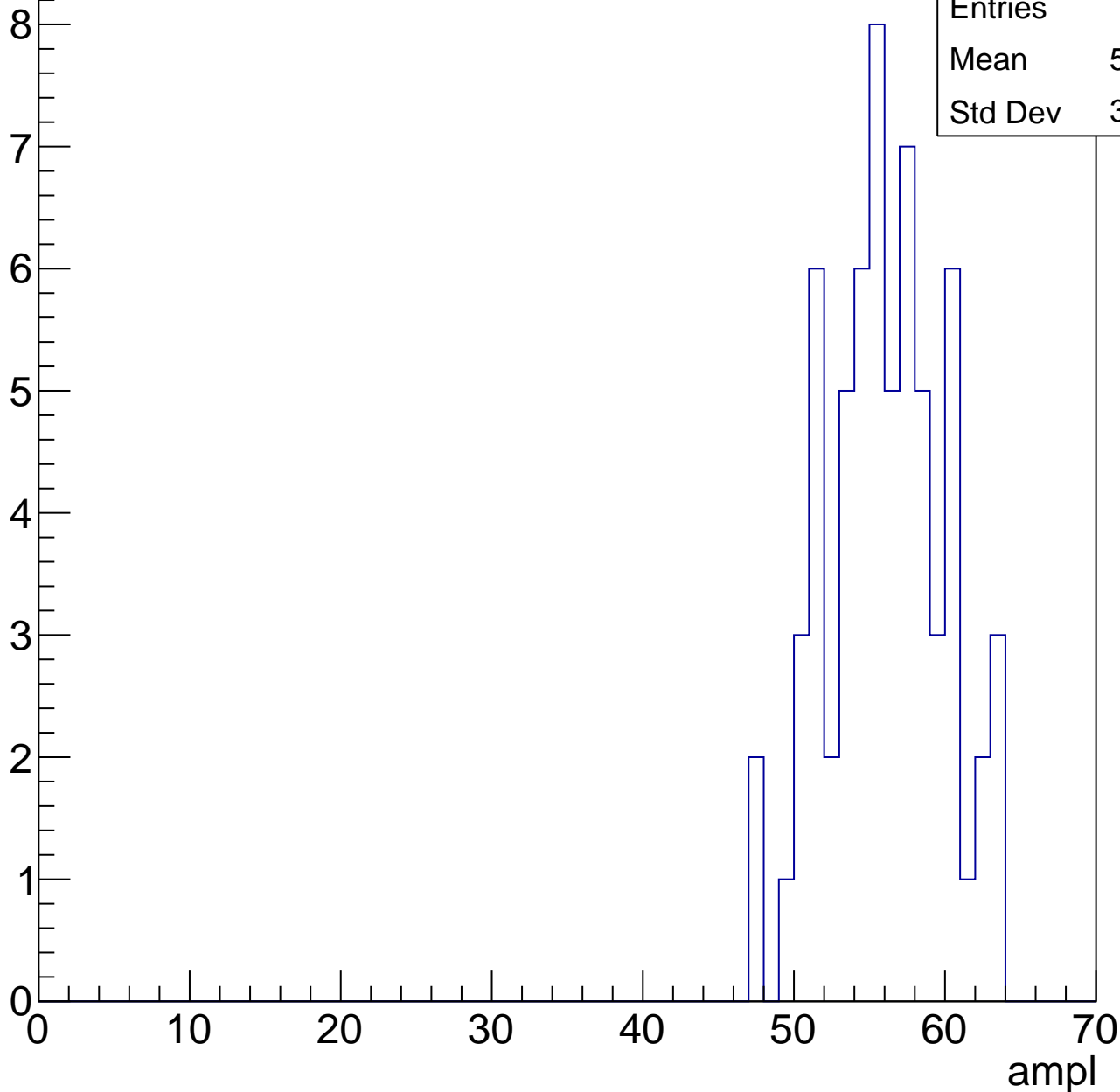


# B1L103S, U26-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	65
Mean	55.57
Std Dev	3.843

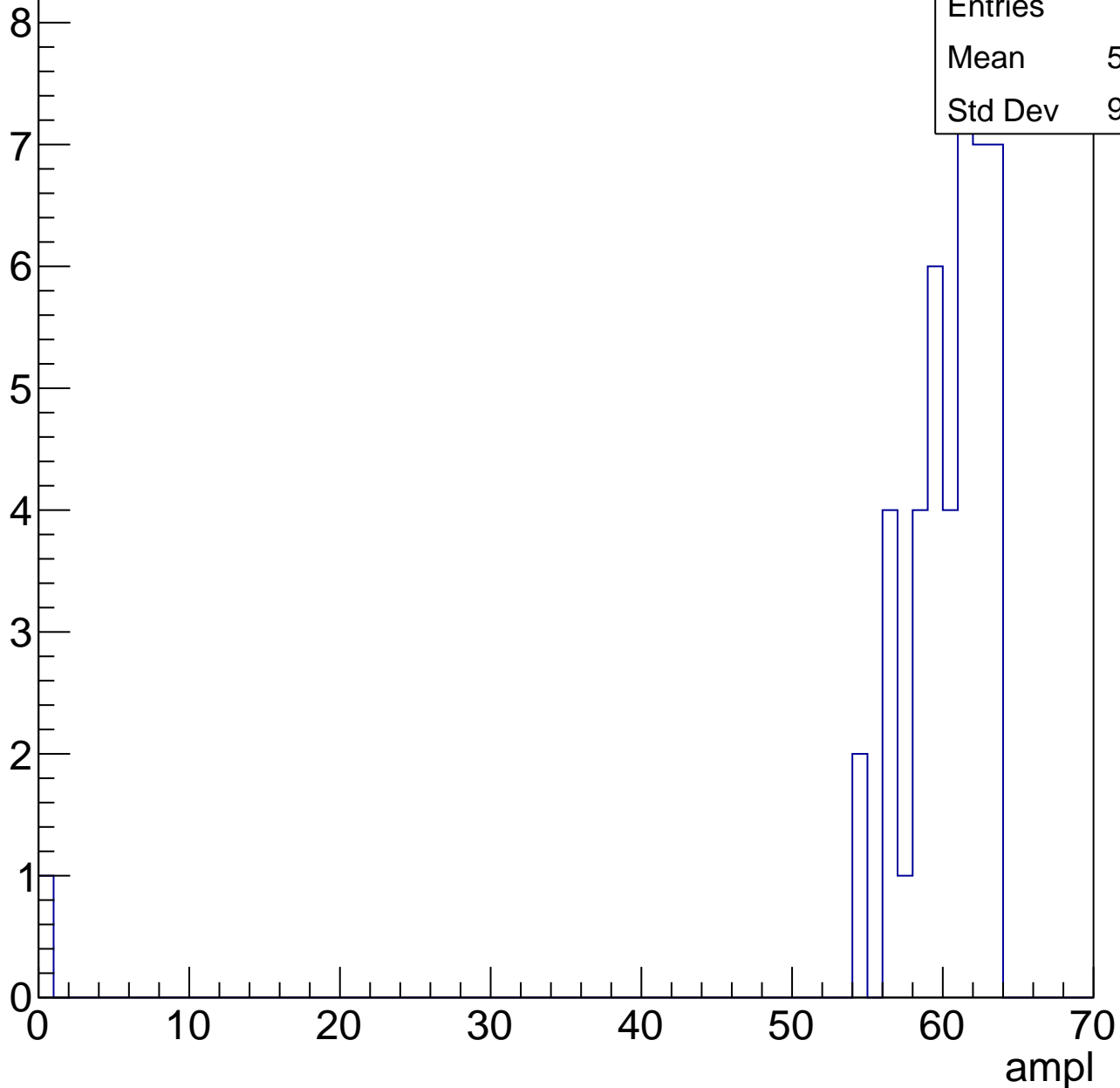


# B1L103S, U26-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

Entries	44
Mean	58.59
Std Dev	9.267



# B1L103S, U26-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry





# B1L103S, U26-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry



# B1L103S, U26-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#7, port C2

Entry

