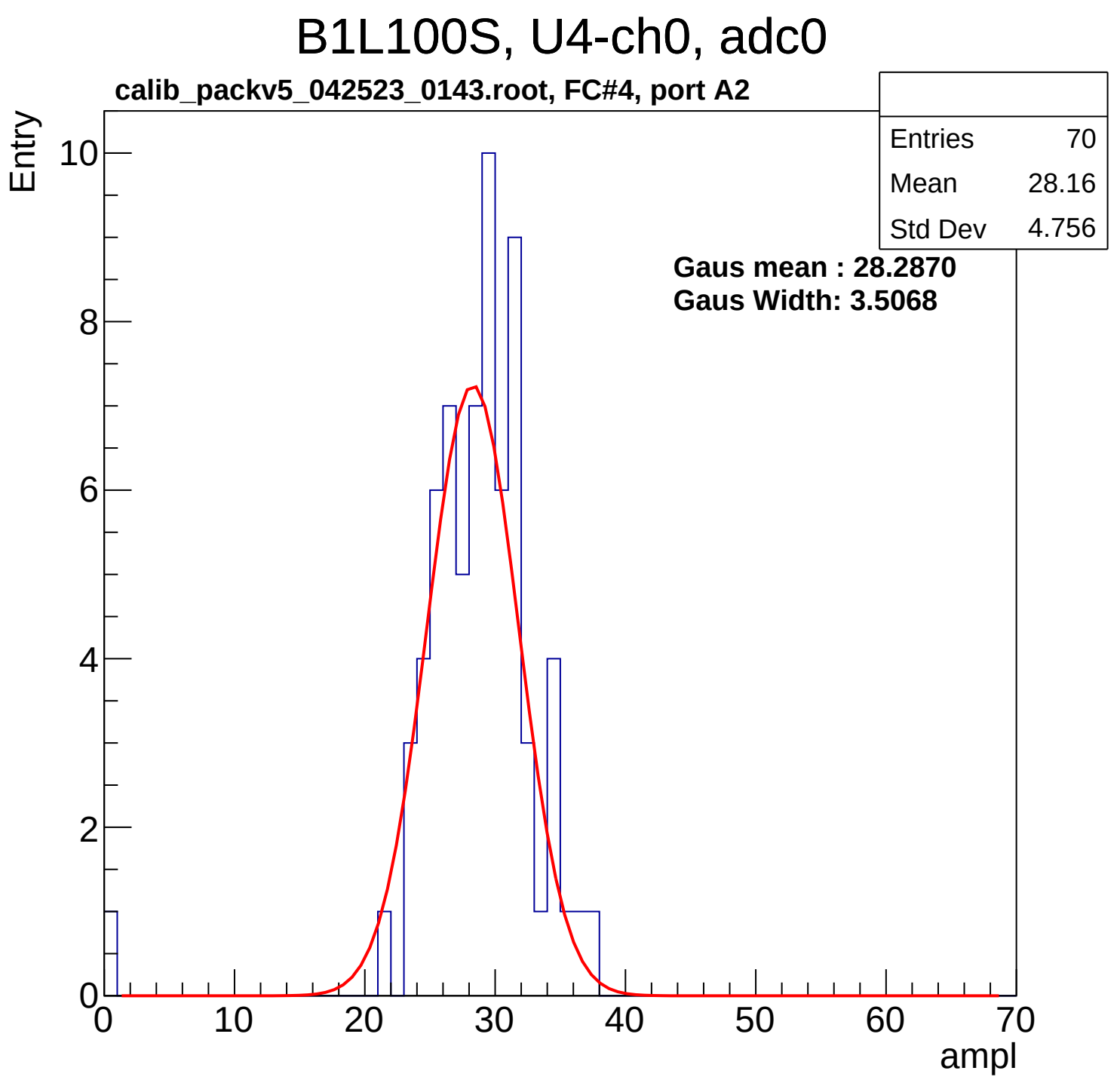
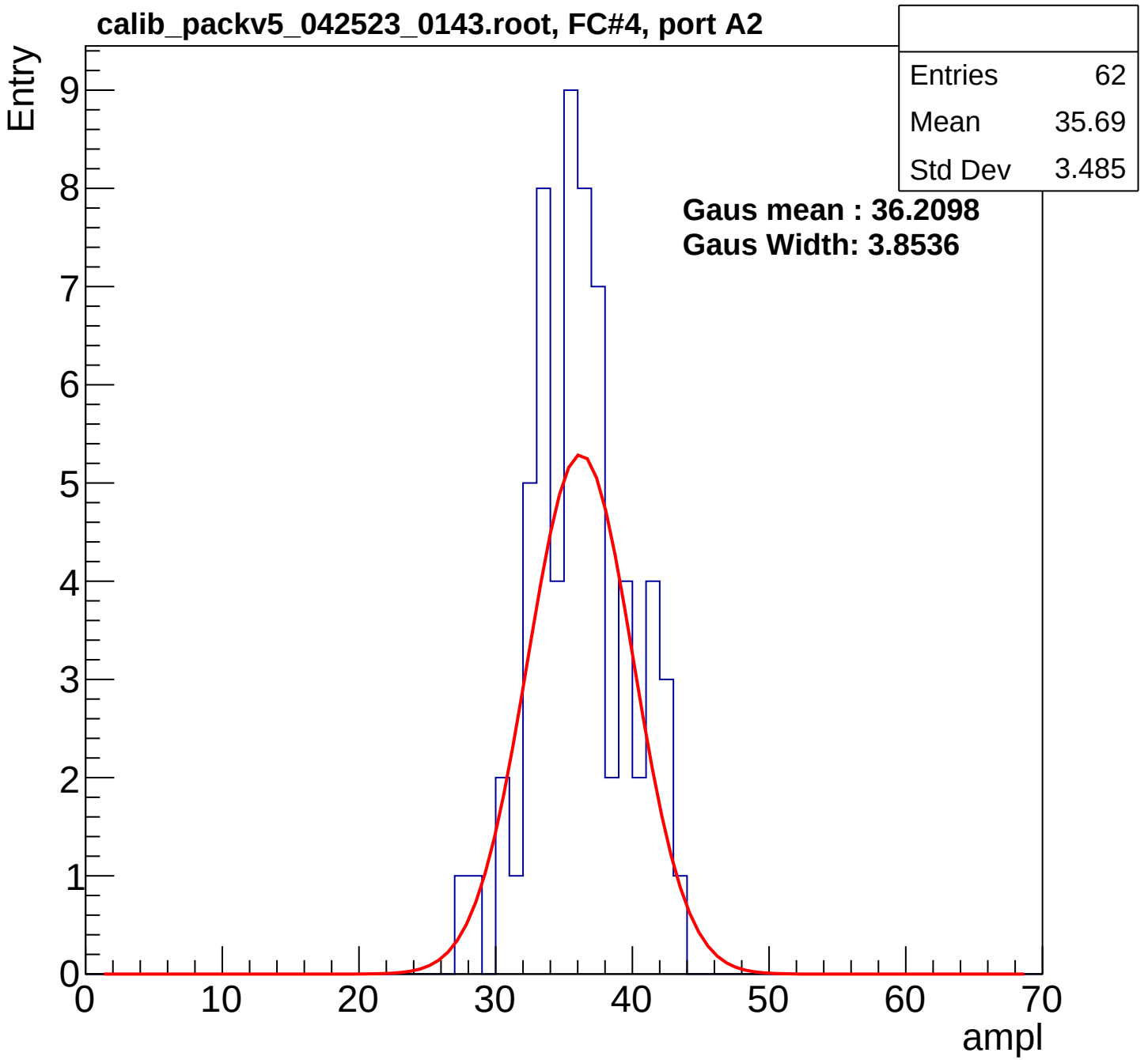
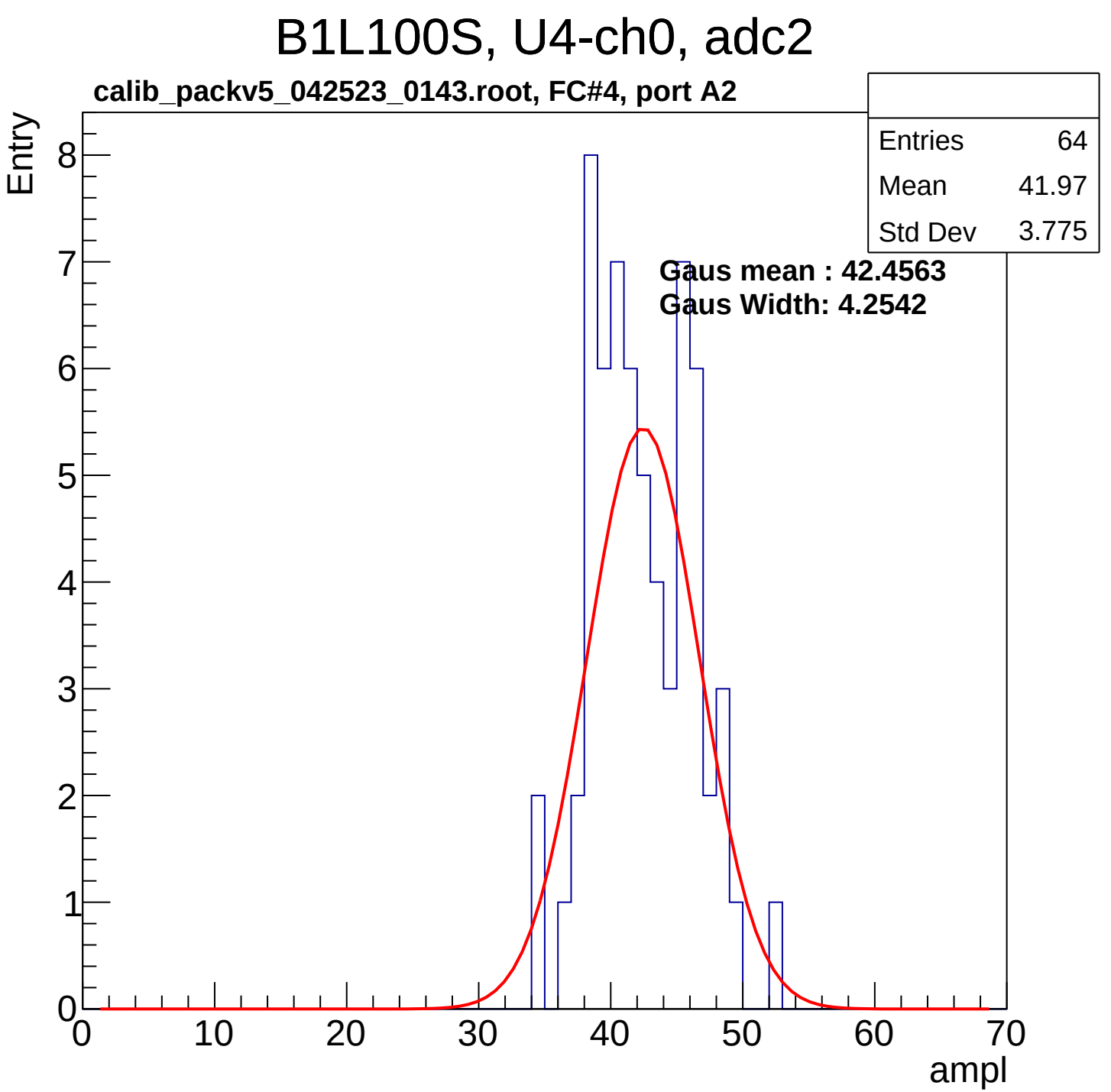
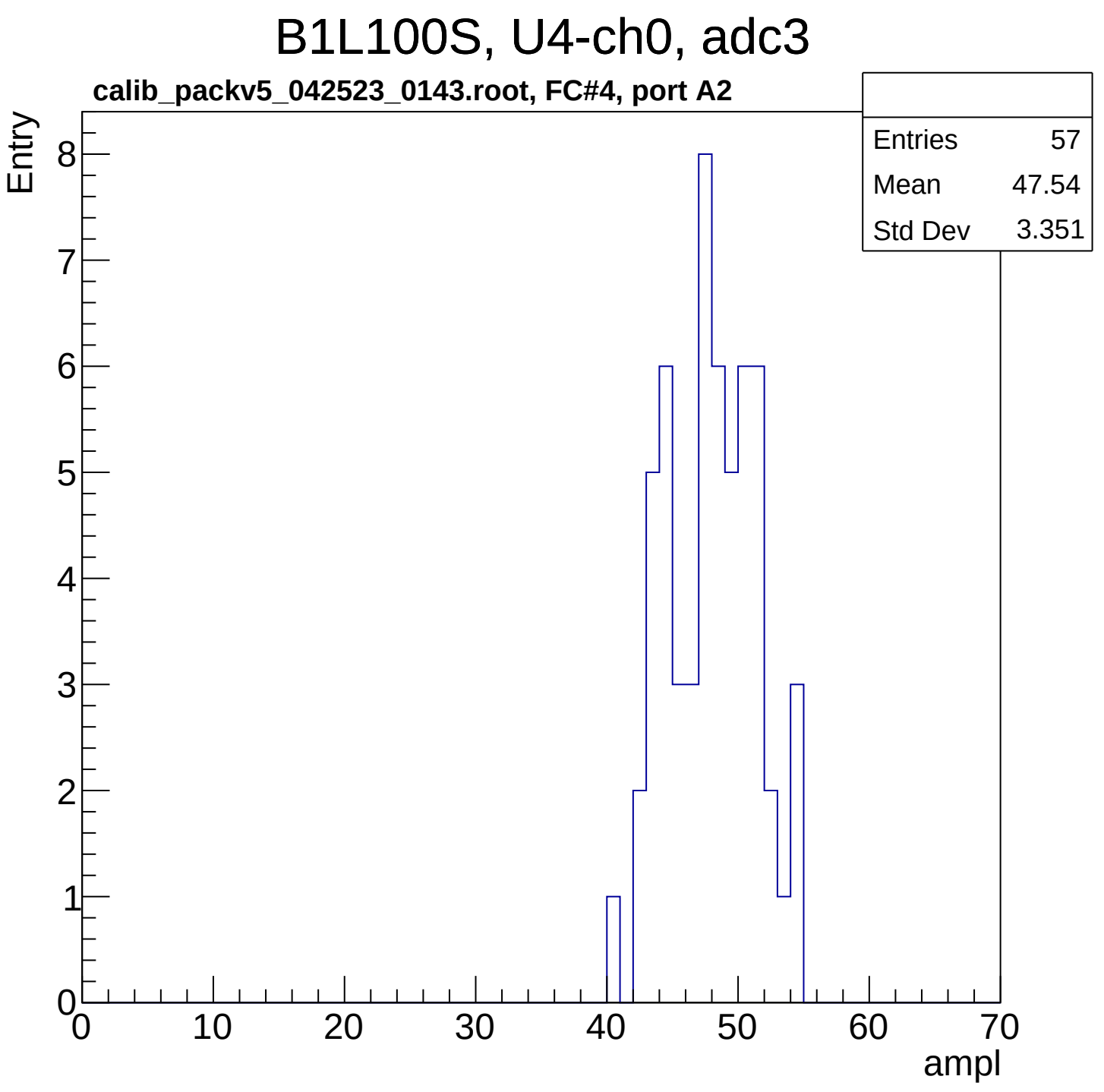
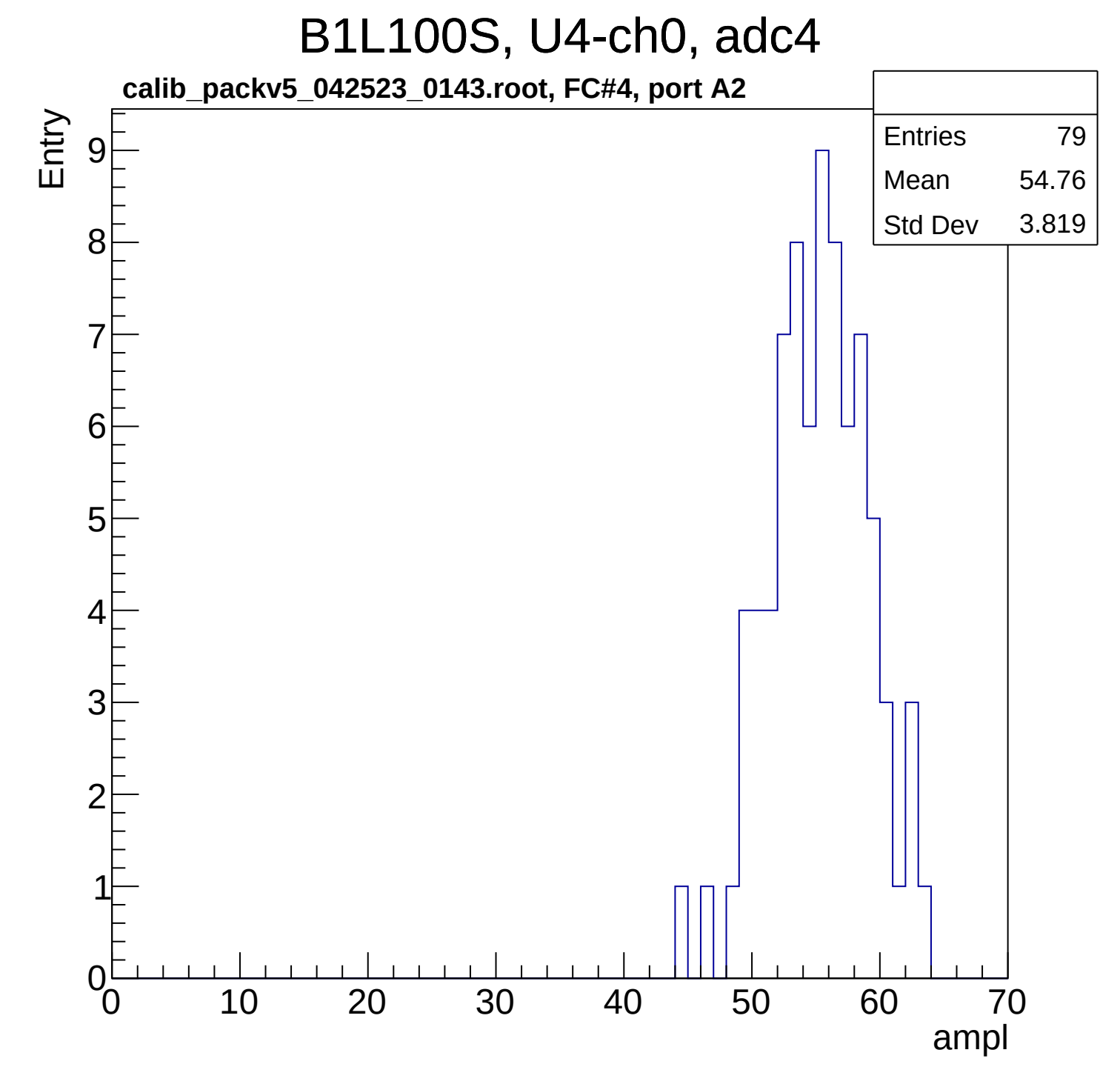
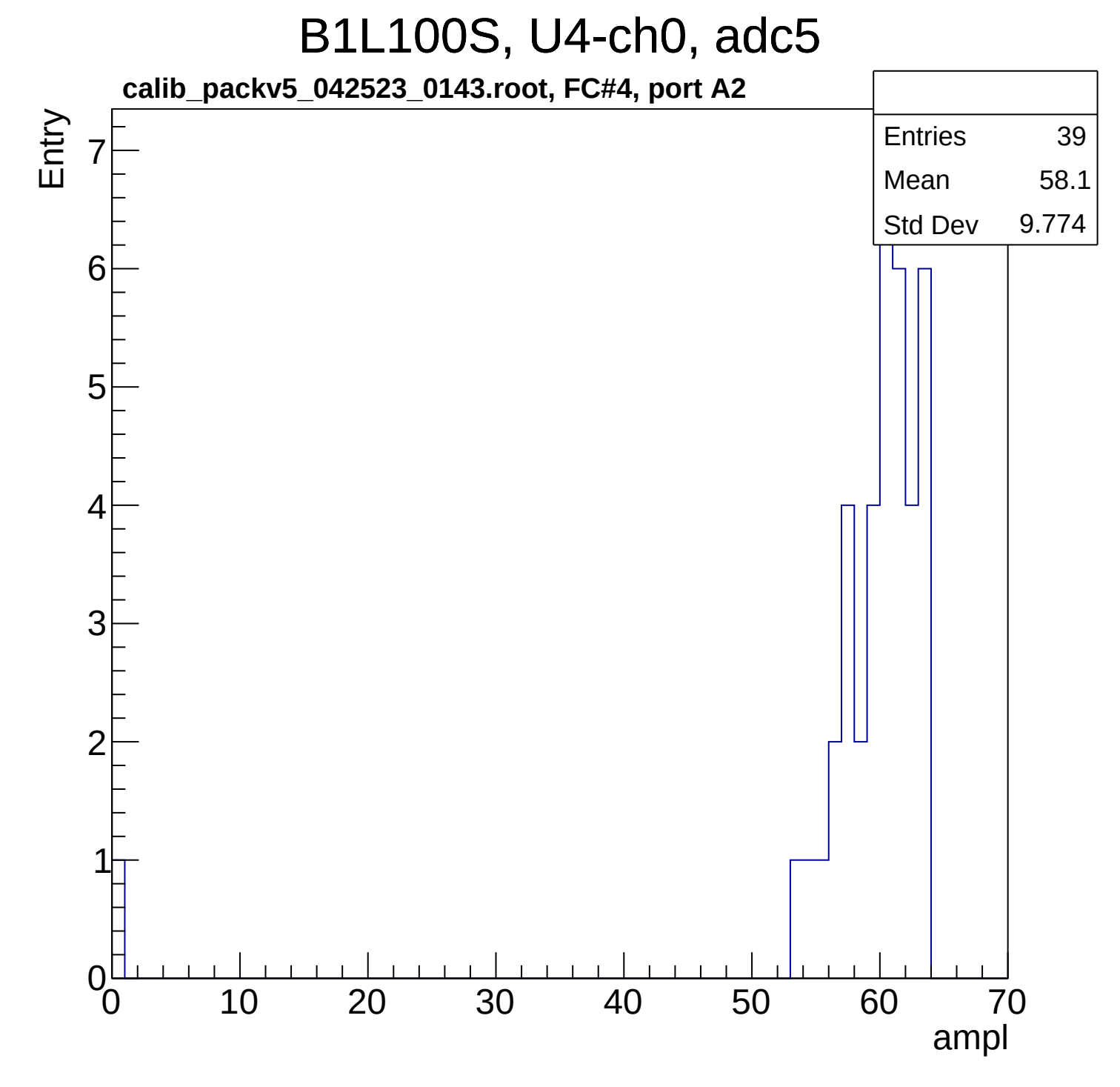

B1L100S, U4-ch0, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 28.16
Std Dev 4.756
Gaus mean : 28.2870
Gaus Width: 3.5068
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

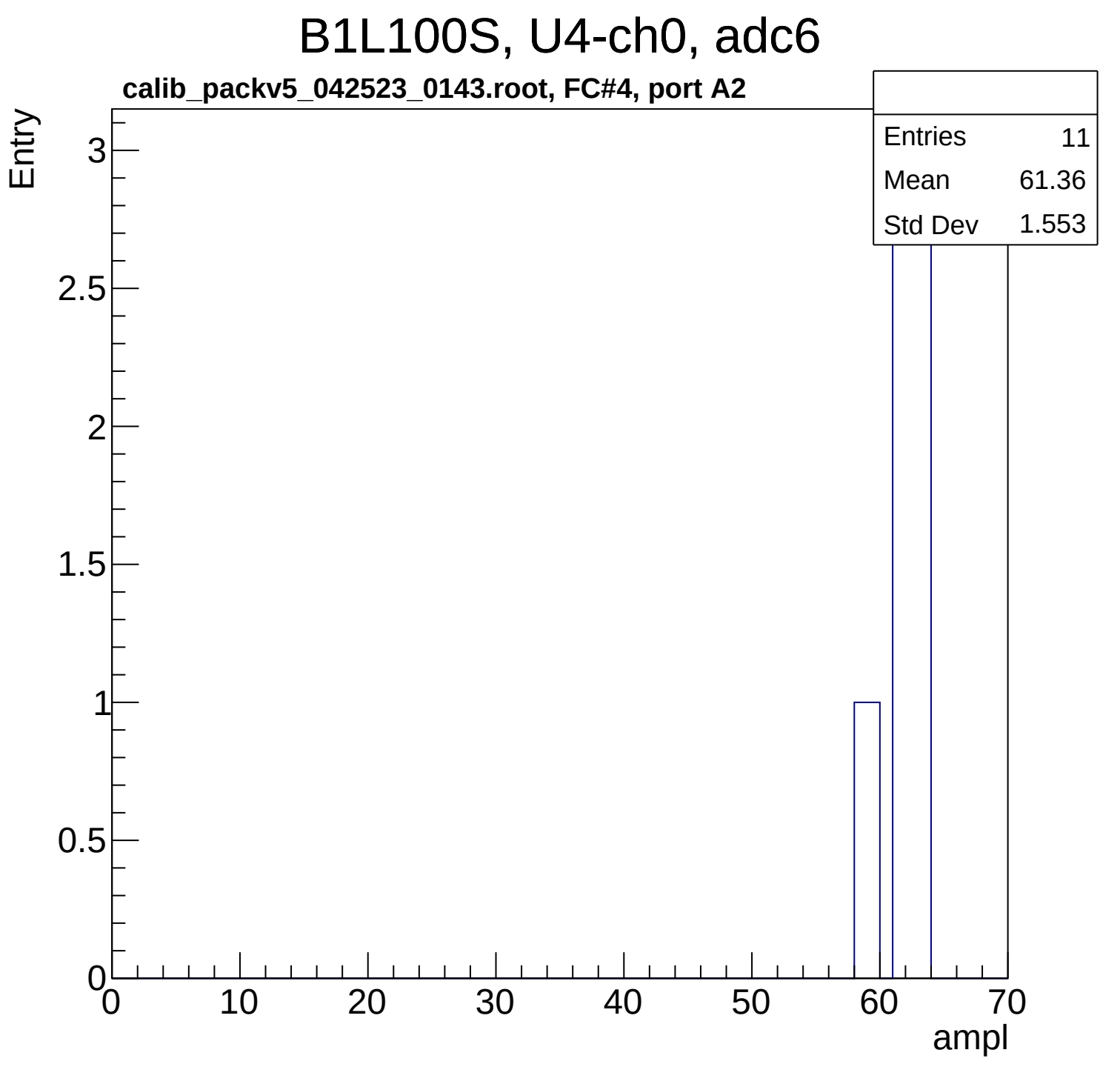

B1L100S, U4-ch0, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 35.69
Std Dev 3.485
Gaus mean : 36.2098
Gaus Width: 3.8536
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

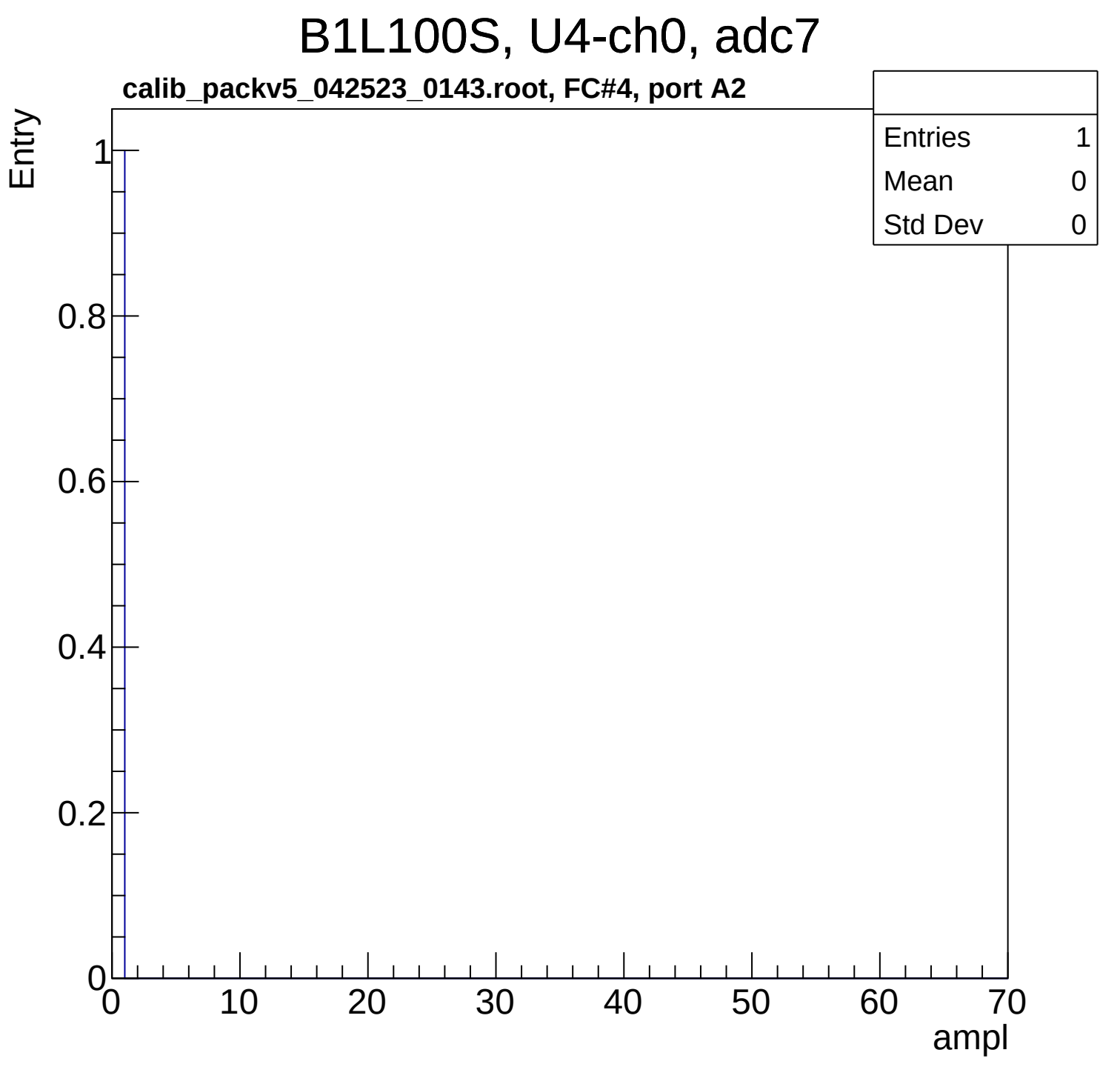

B1L100S, U4-ch0, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 41.97
Std Dev 3.775
Gaus mean : 42.4563
Gaus Width: 4.2542
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

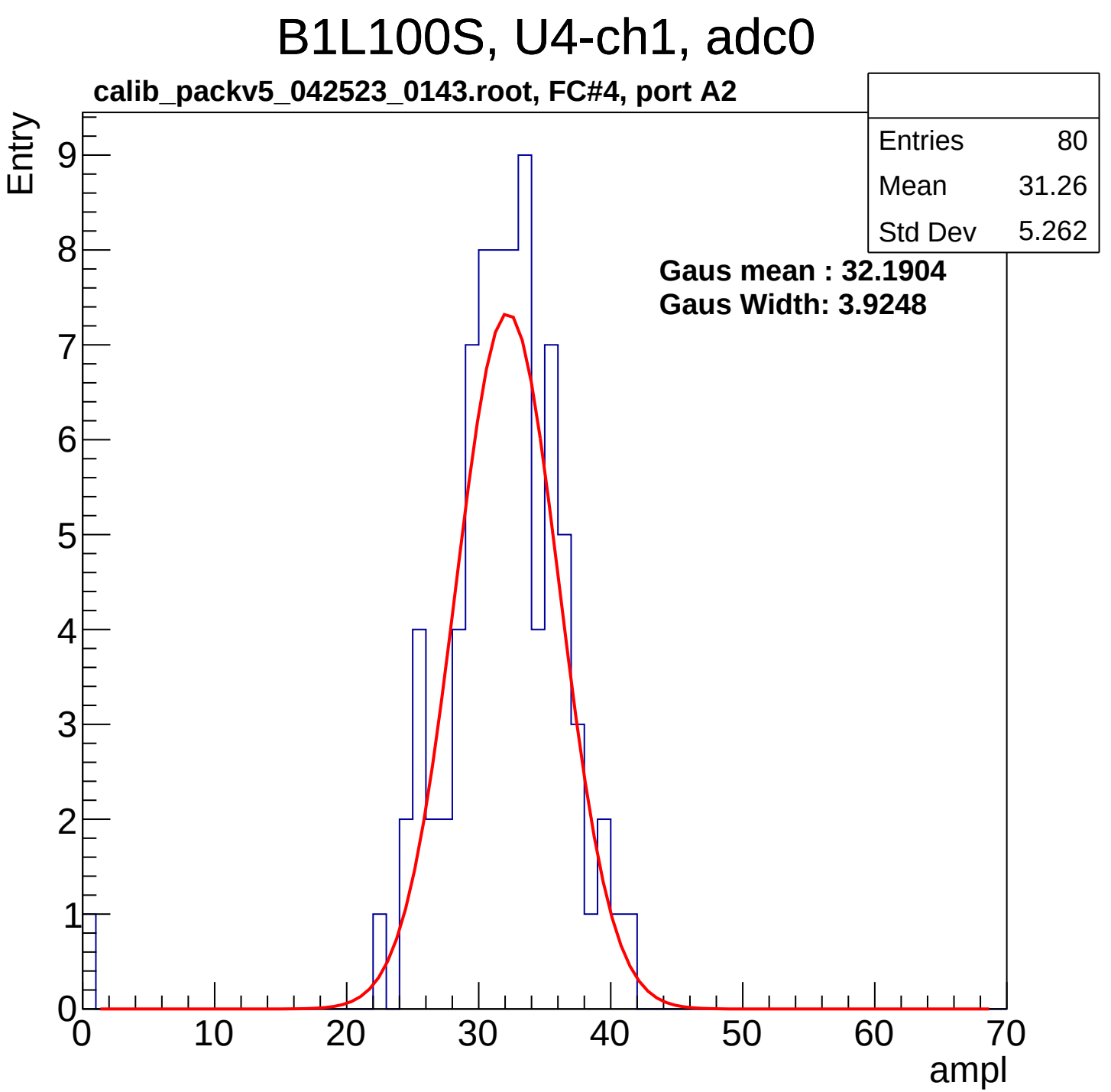

B1L100S, U4-ch0, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 47.54
Std Dev 3.351
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

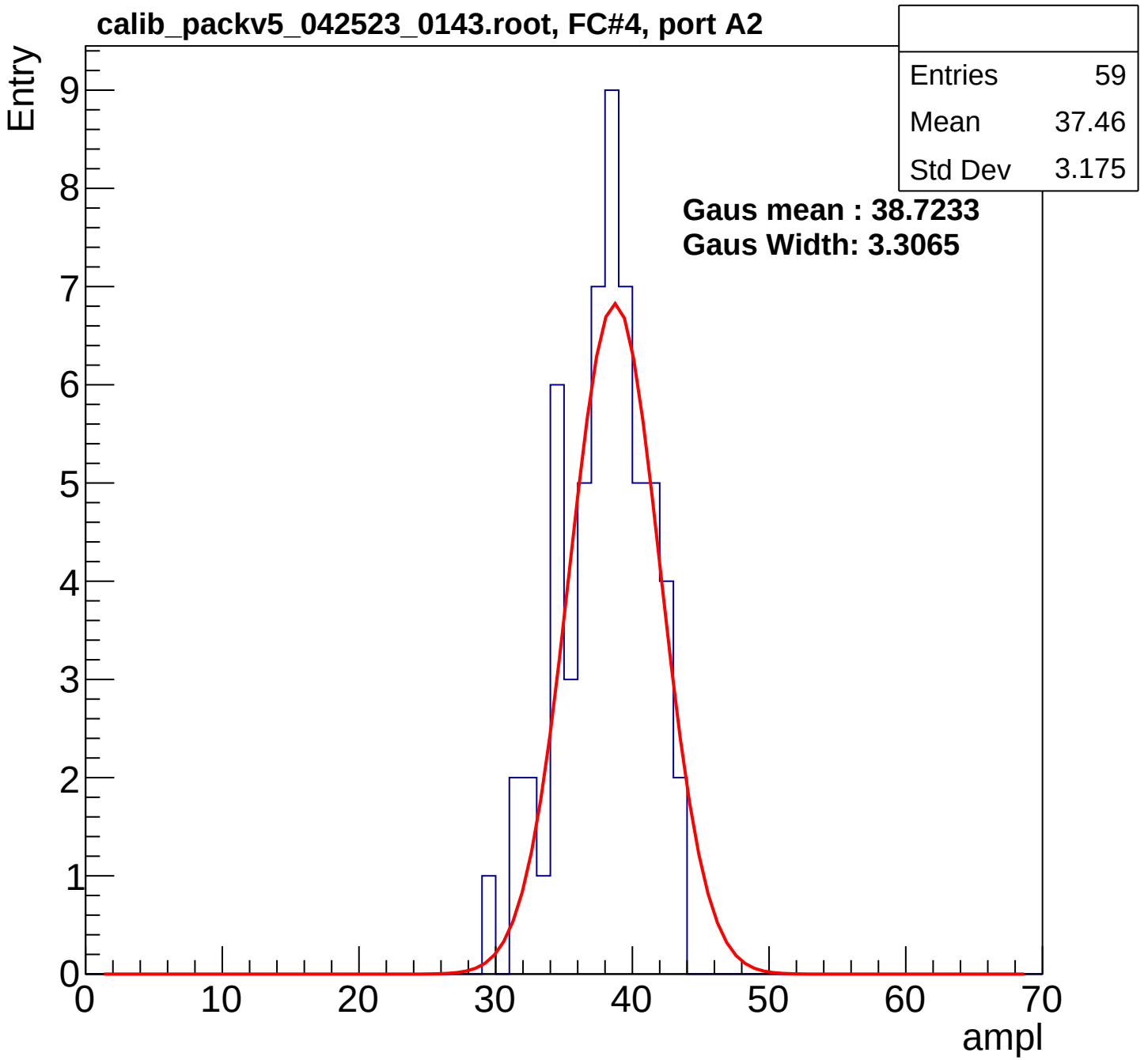

B1L100S, U4-ch0, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 54.76
Std Dev 3.819
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

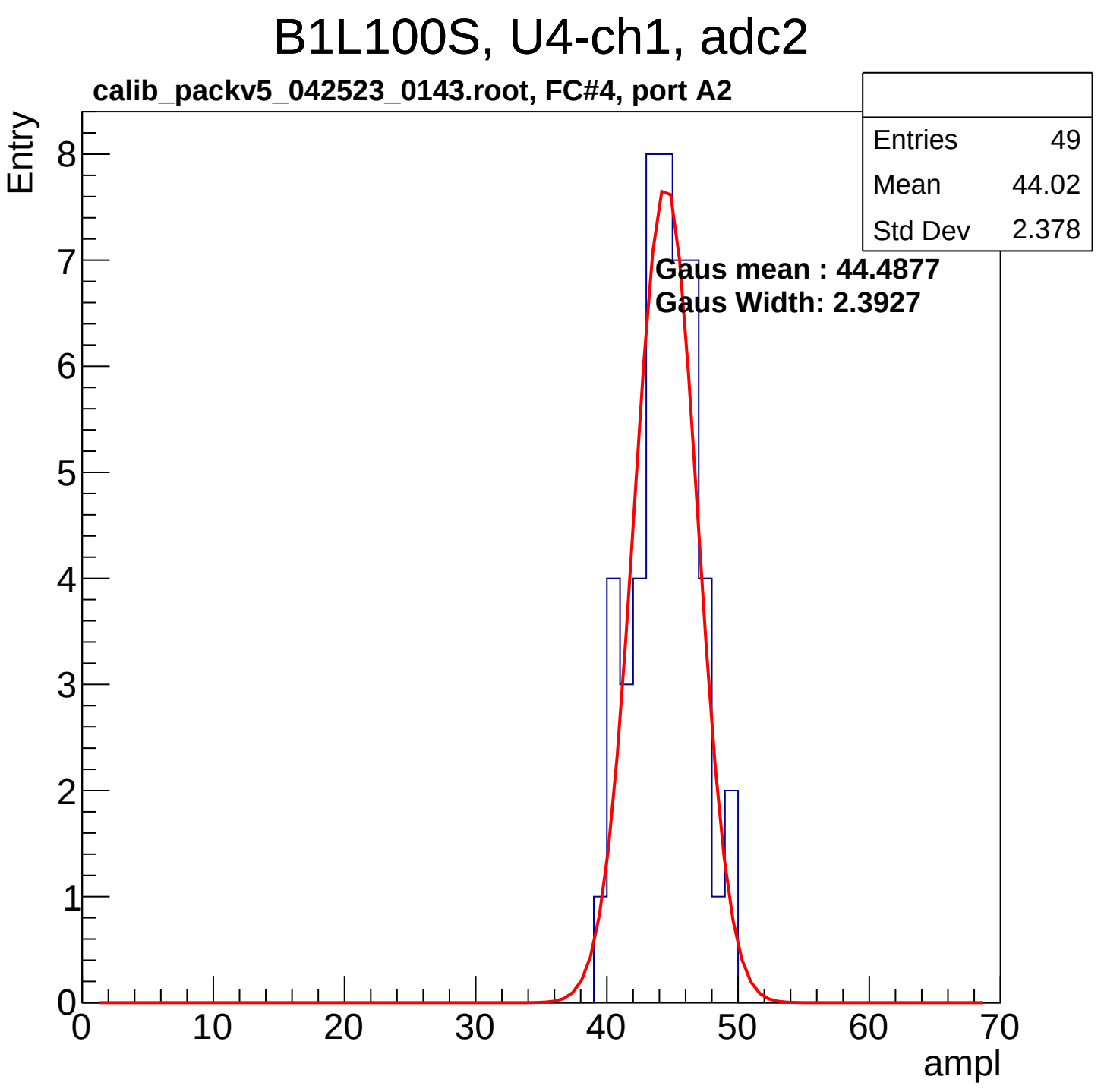

B1L100S, U4-ch0, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 39
Mean 58.1
Std Dev 9.774
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

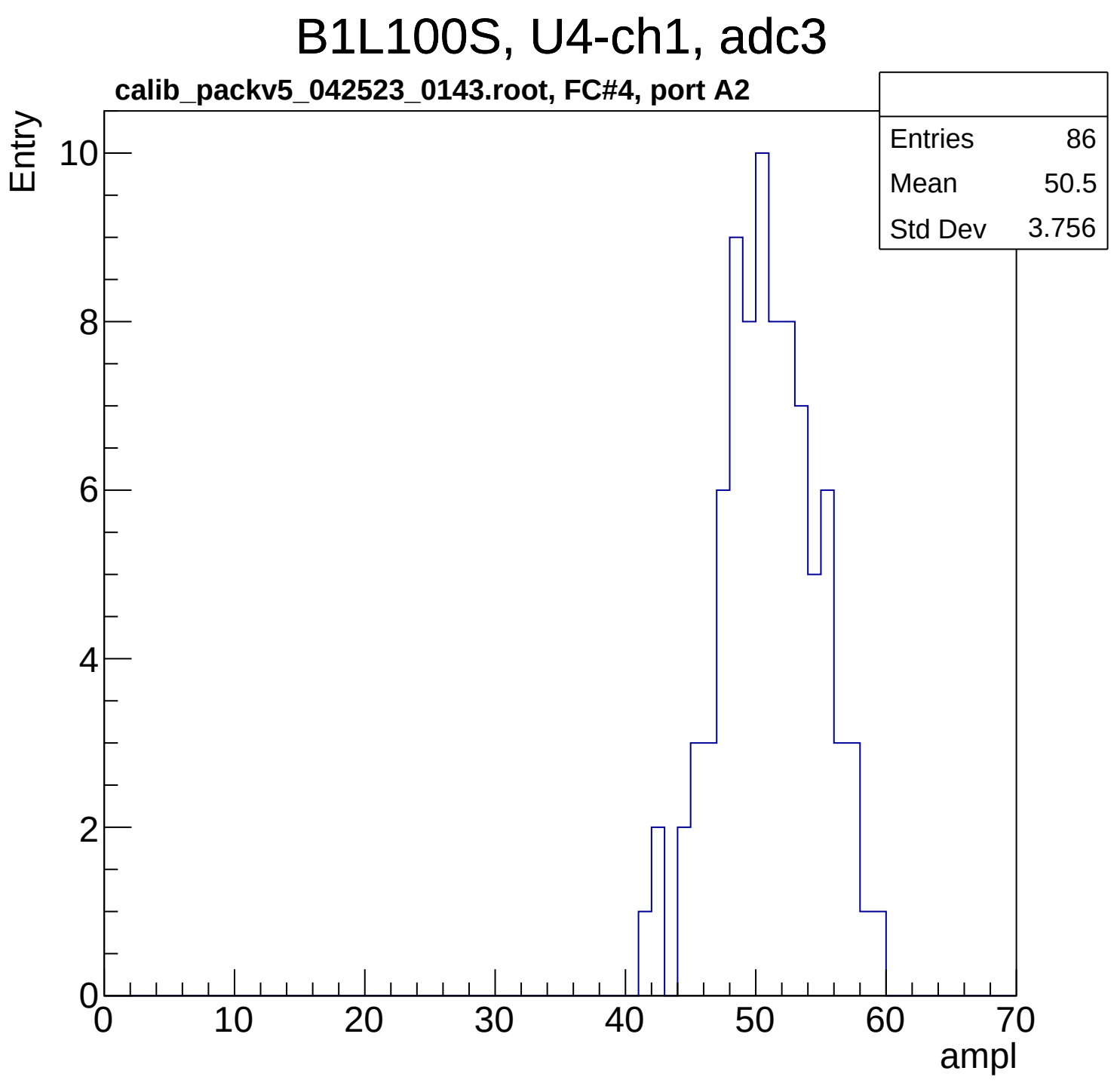

B1L100S, U4-ch0, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 61.36
Std Dev 1.553
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

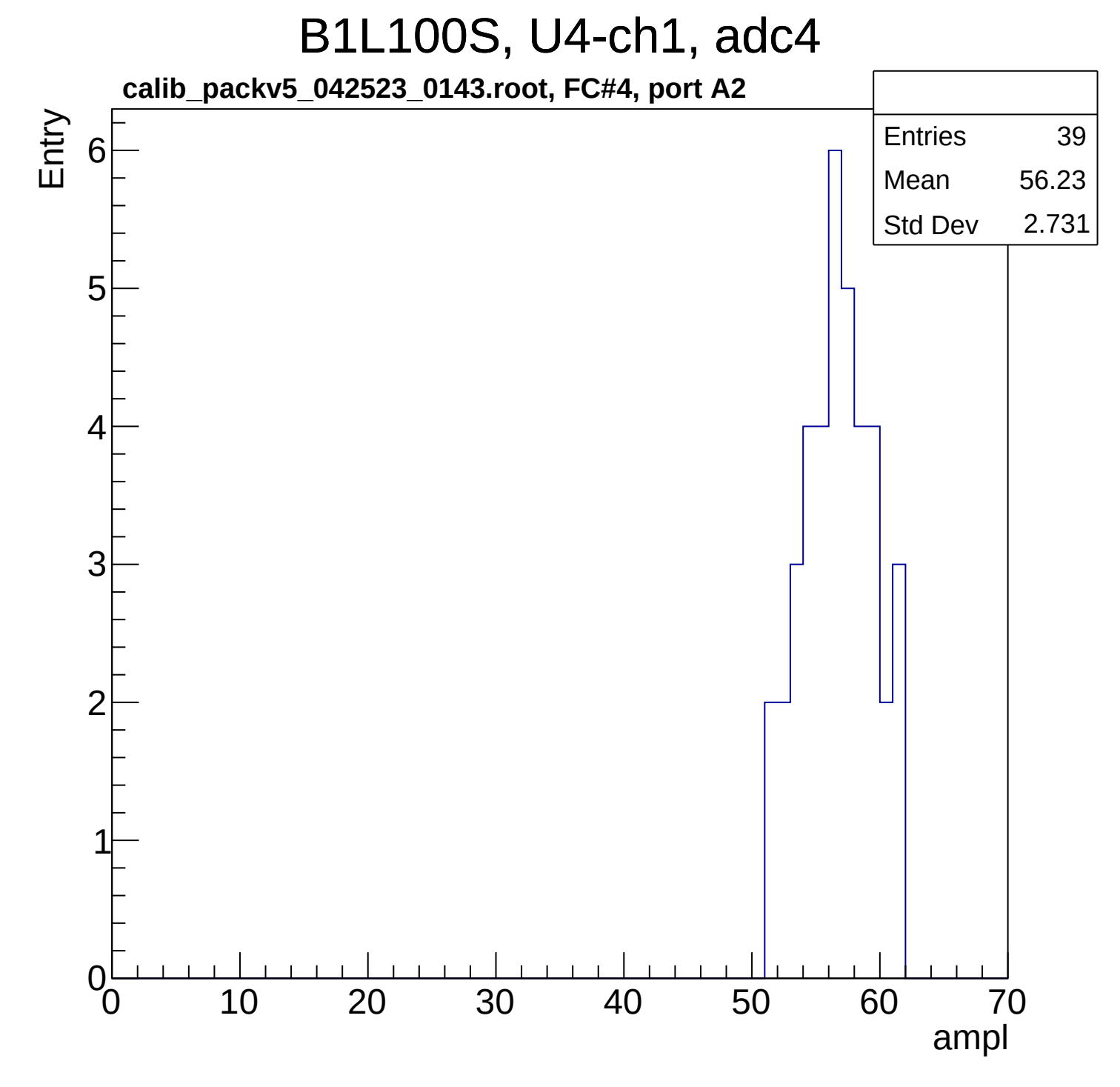

B1L100S, U4-ch0, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

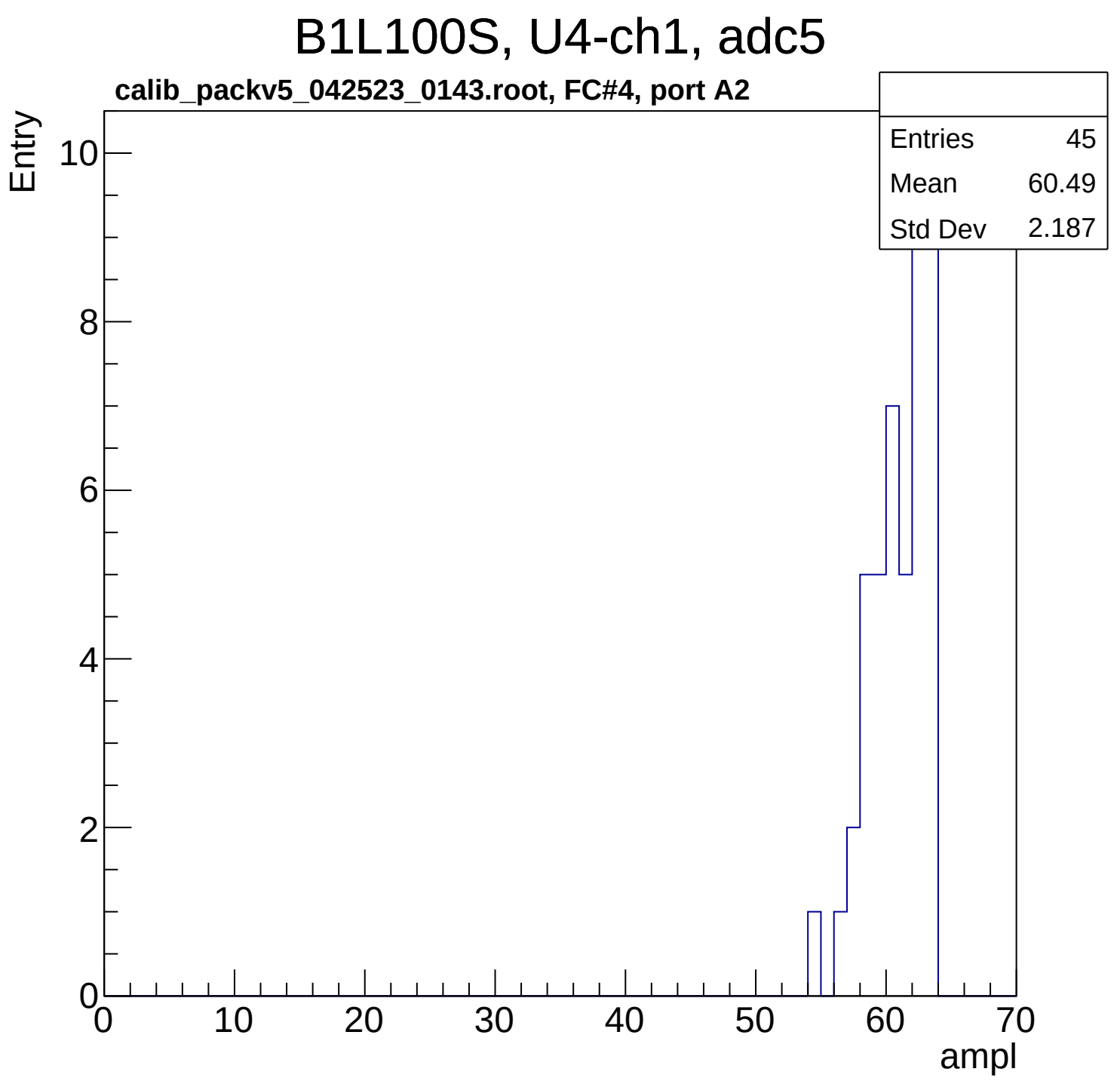

B1L100S, U4-ch1, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 31.26
Std Dev 5.262
Gaus mean : 32.1904
Gaus Width: 3.9248
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

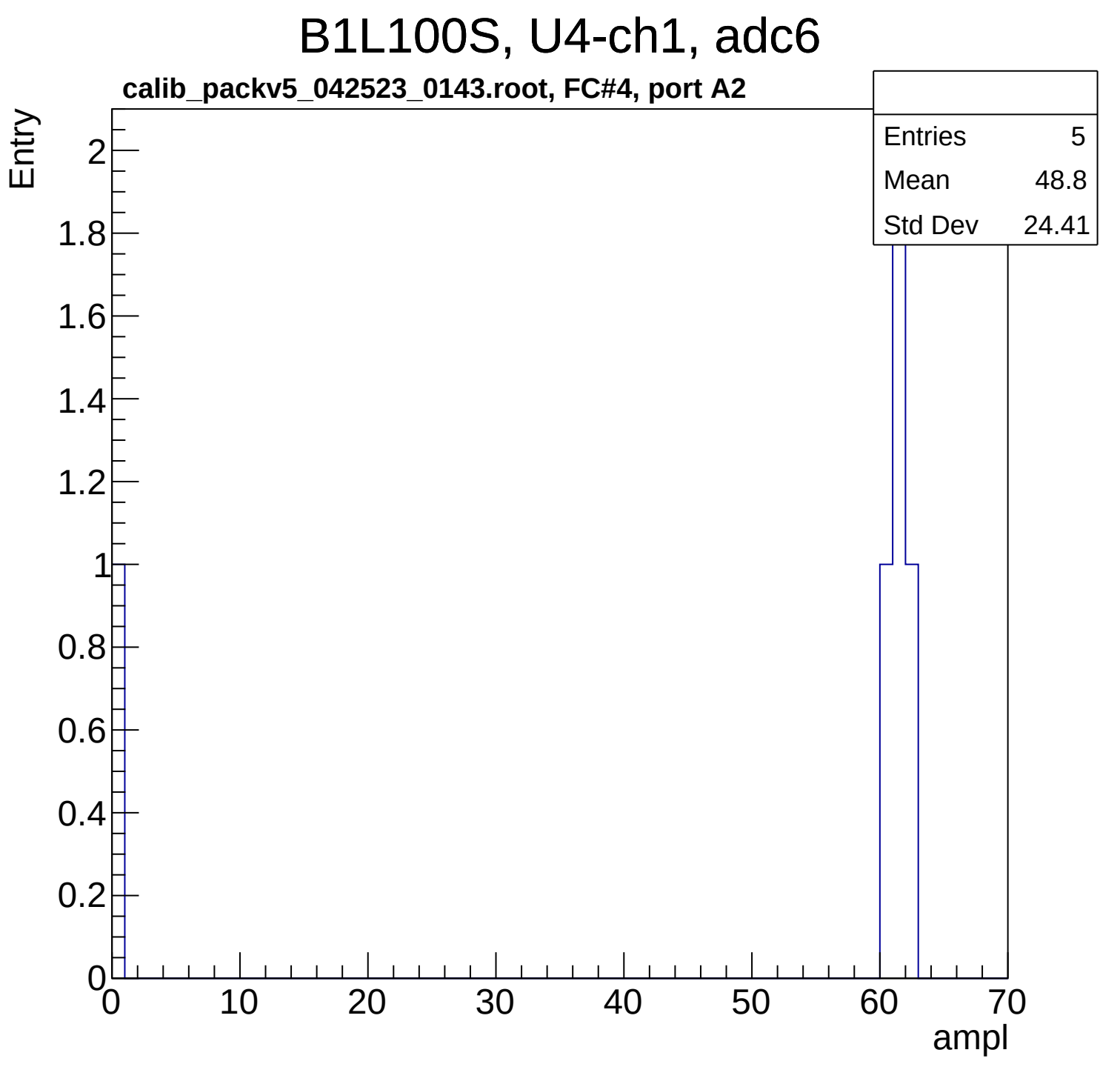

B1L100S, U4-ch1, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 37.46
Std Dev 3.175
Gaus mean : 38.7233
Gaus Width: 3.3065
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

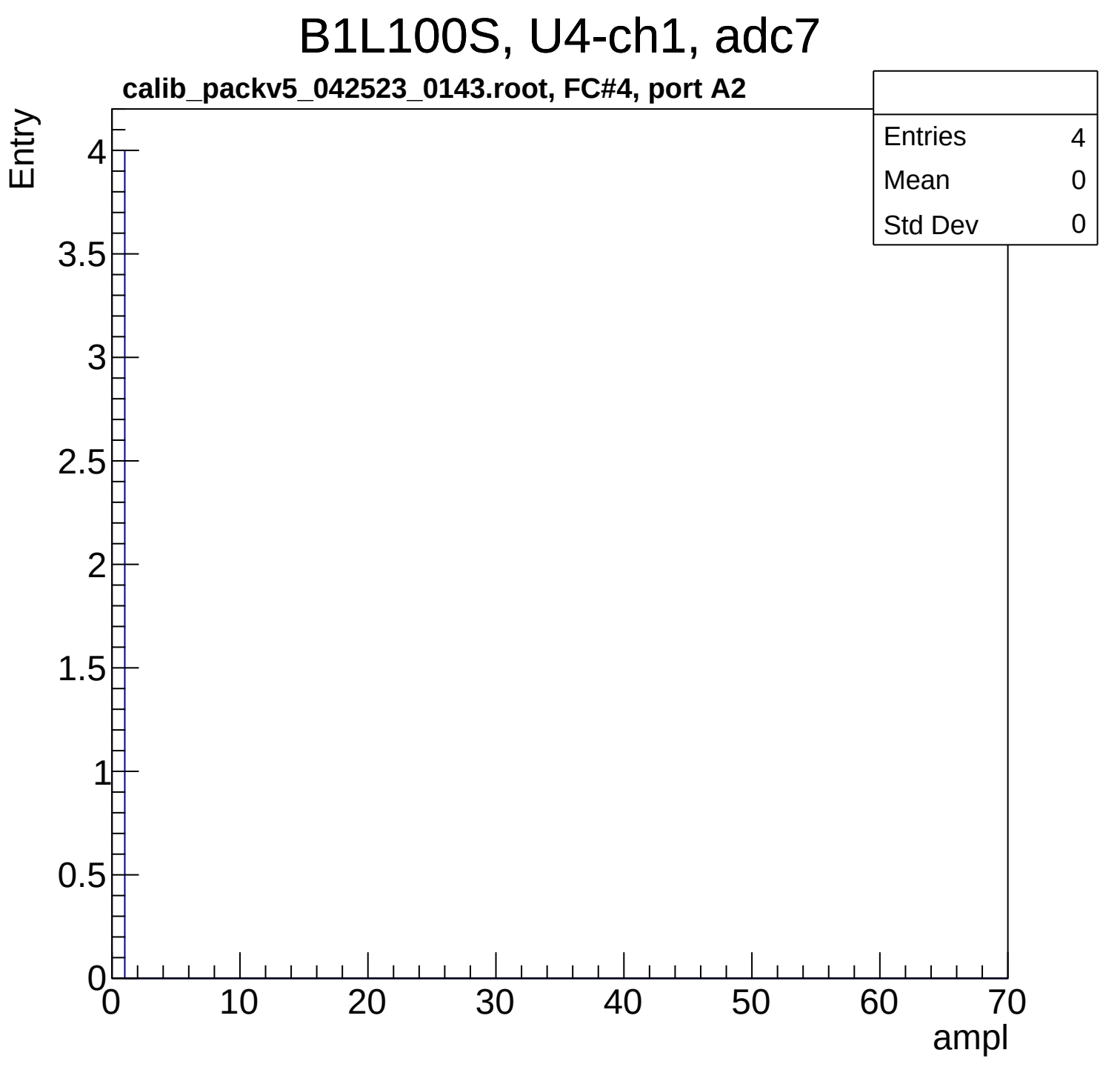

B1L100S, U4-ch1, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 44.02
Std Dev 2.378
Gaus mean : 44.4877
Gaus Width: 2.3927
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

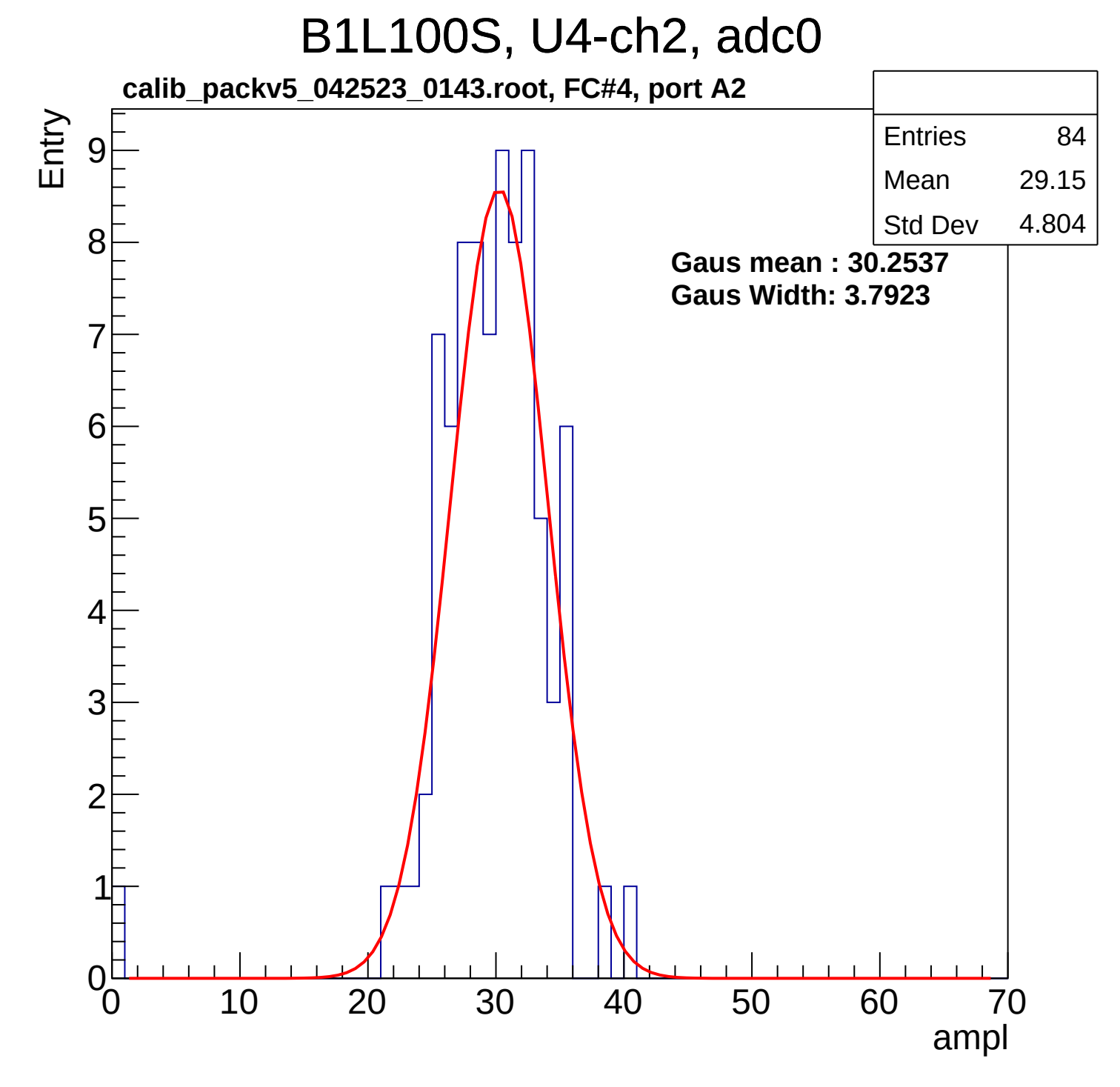

B1L100S, U4-ch1, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 86
Mean 50.5
Std Dev 3.756
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

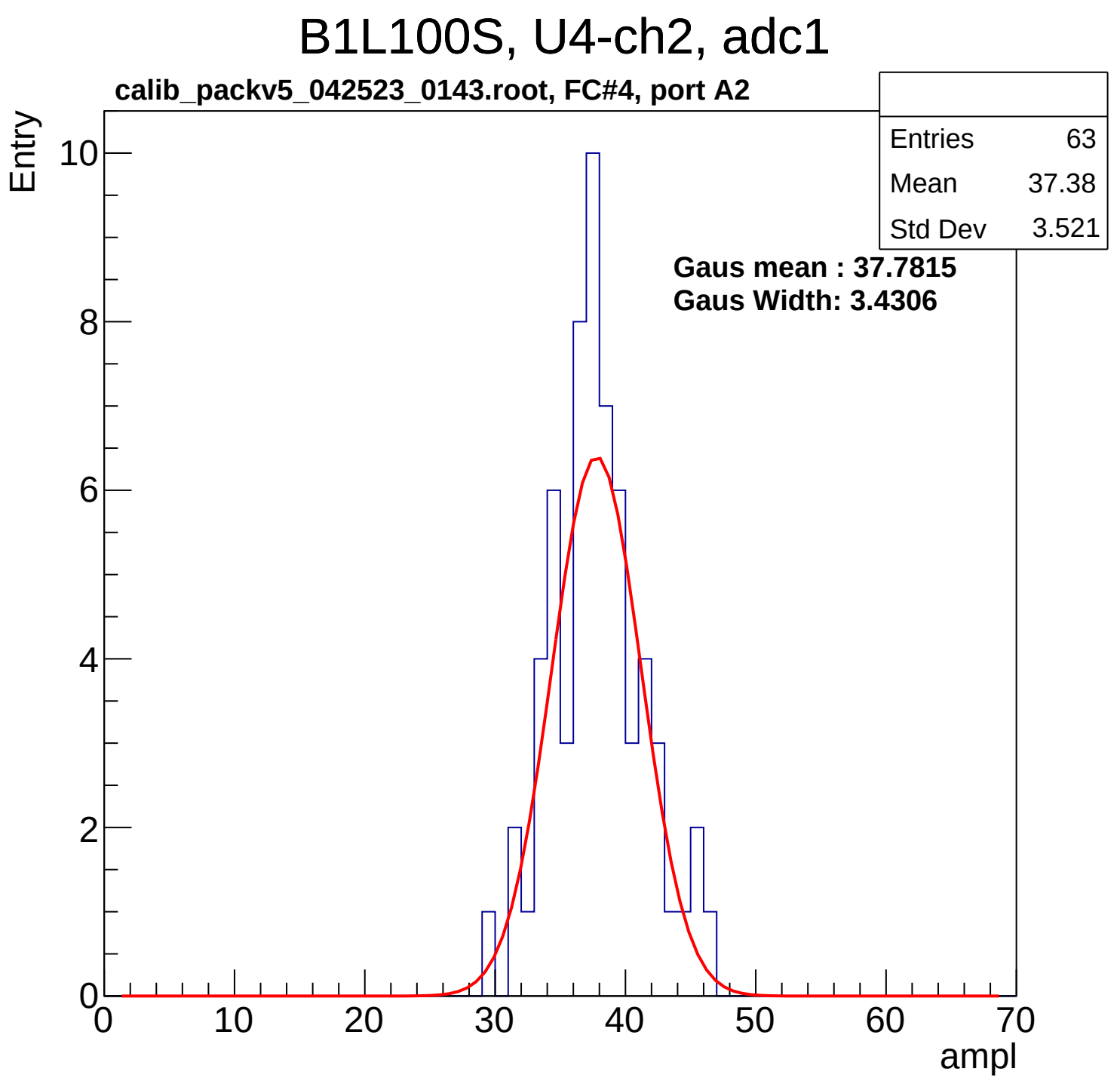

B1L100S, U4-ch1, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 39
Mean 56.23
Std Dev 2.731
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

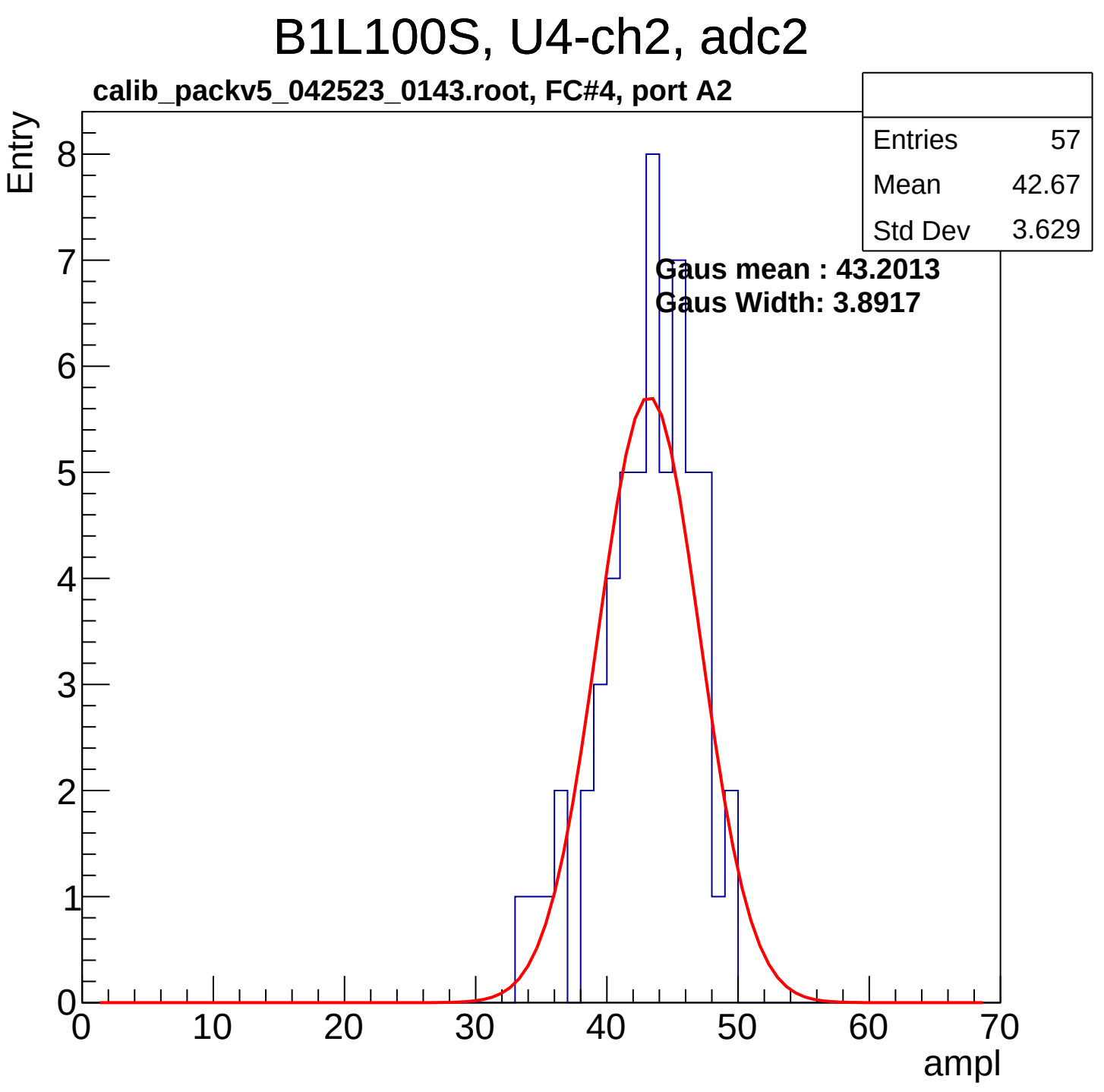

B1L100S, U4-ch1, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 45
Mean 60.49
Std Dev 2.187
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

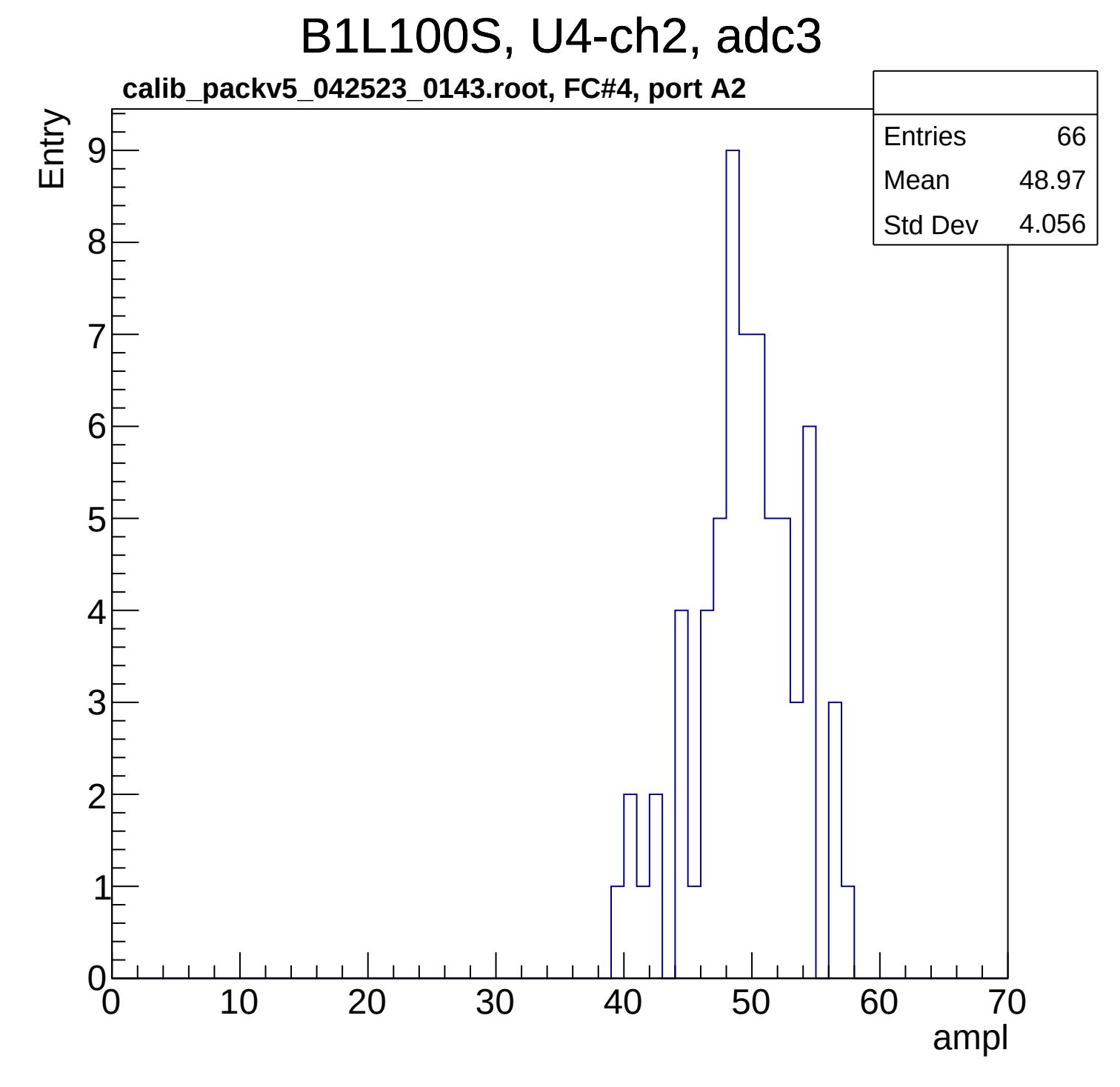

B1L100S, U4-ch1, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 5
Mean 48.8
Std Dev 24.41
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

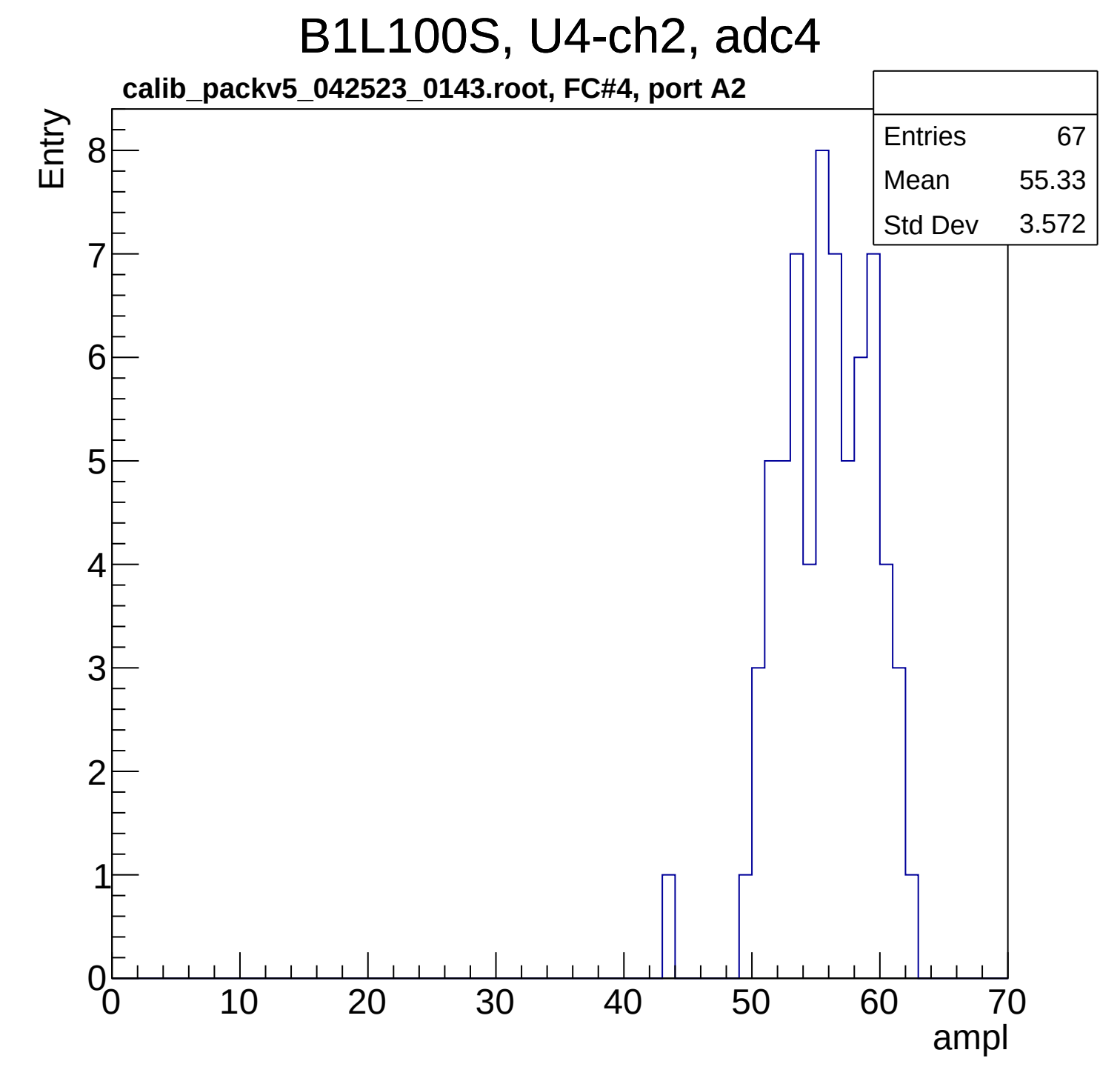

B1L100S, U4-ch1, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 0
Std Dev 0
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

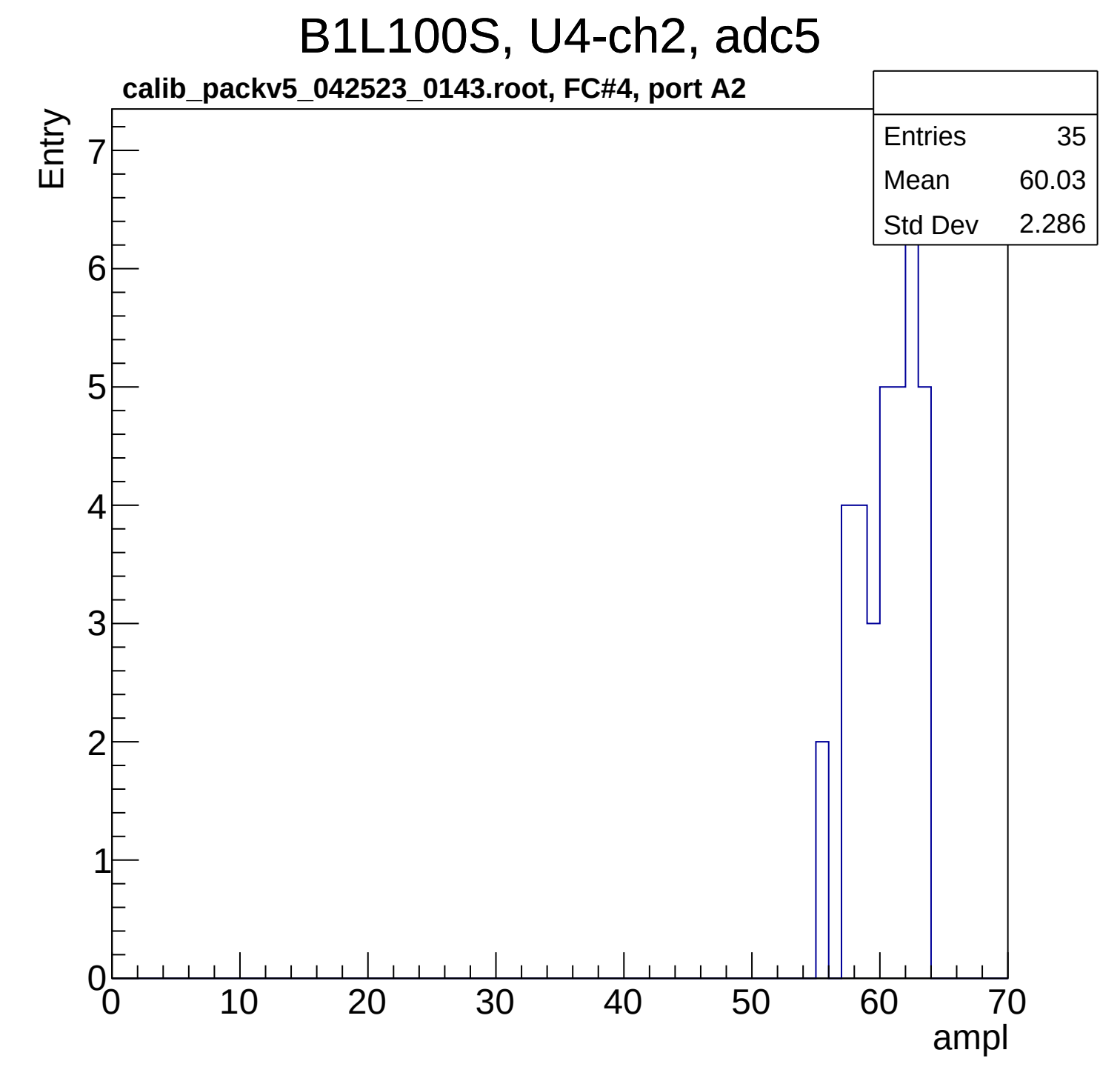

B1L100S, U4-ch2, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 84
Mean 29.15
Std Dev 4.804
Gaus mean : 30.2537
Gaus Width: 3.7923
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

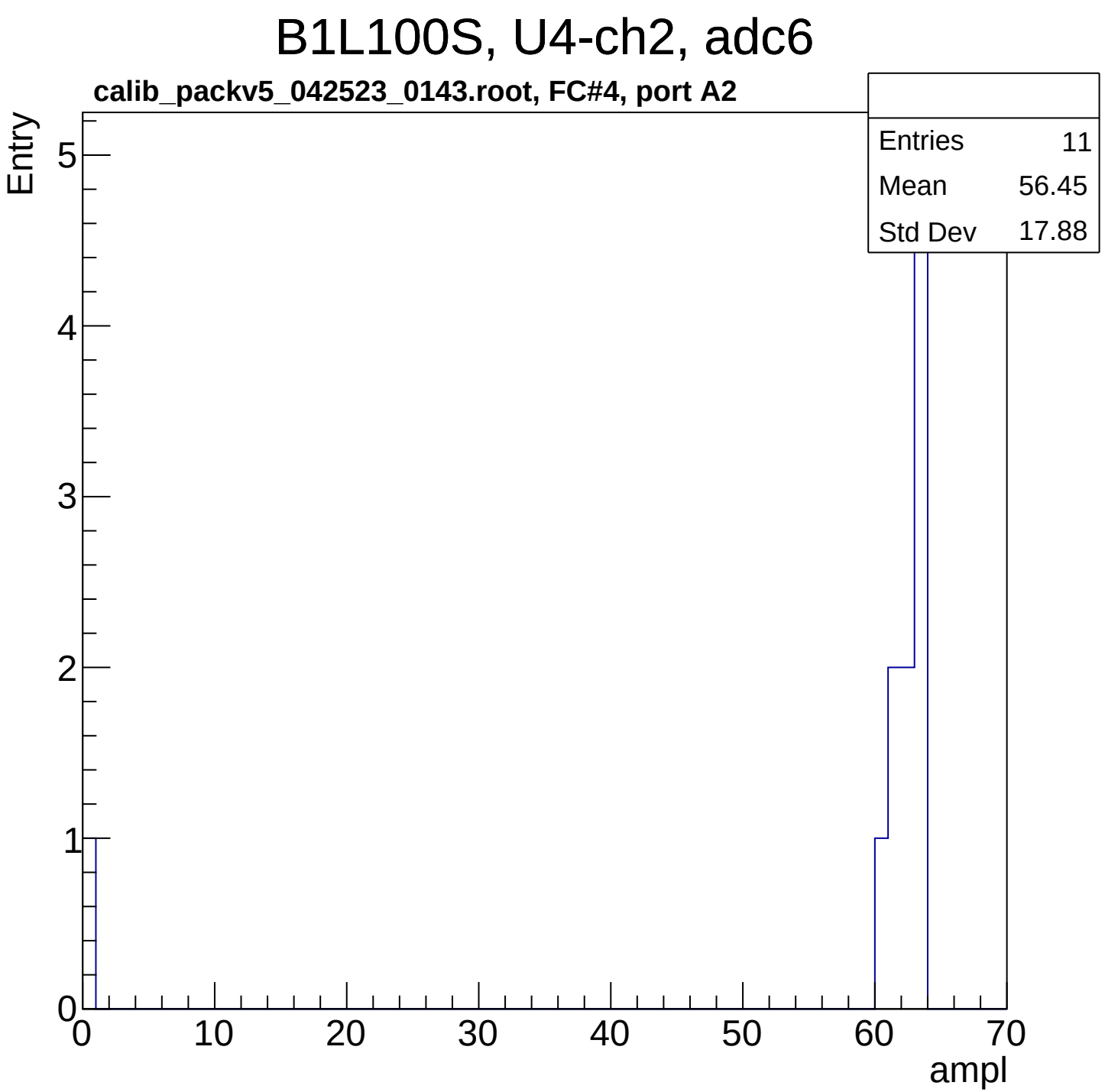

B1L100S, U4-ch2, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 37.38
Std Dev 3.521
Gaus mean : 37.7815
Gaus Width: 3.4306
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

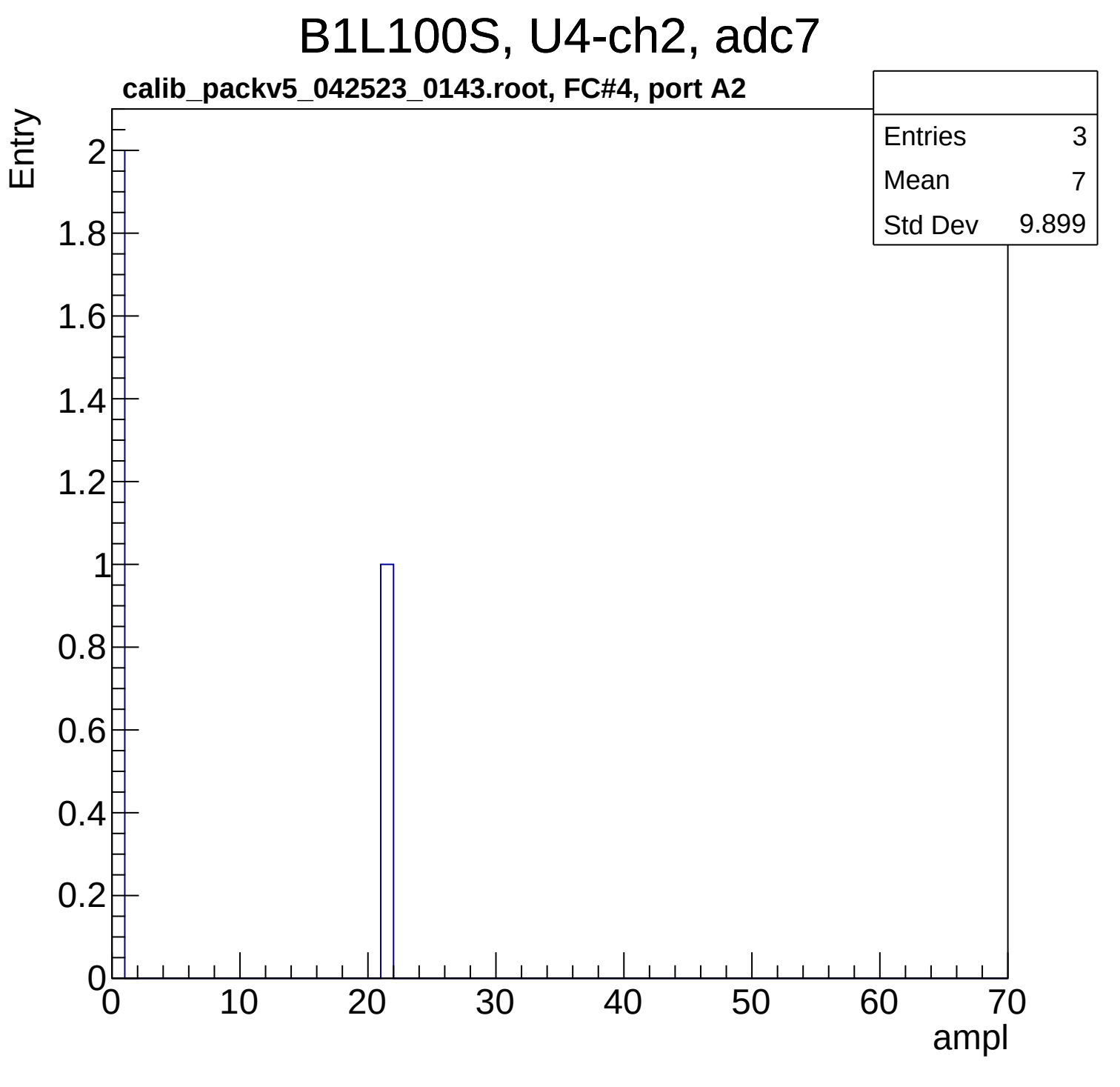

B1L100S, U4-ch2, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 42.67
Std Dev 3.629
Gaus mean : 43.2013
Gaus Width: 3.8917
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

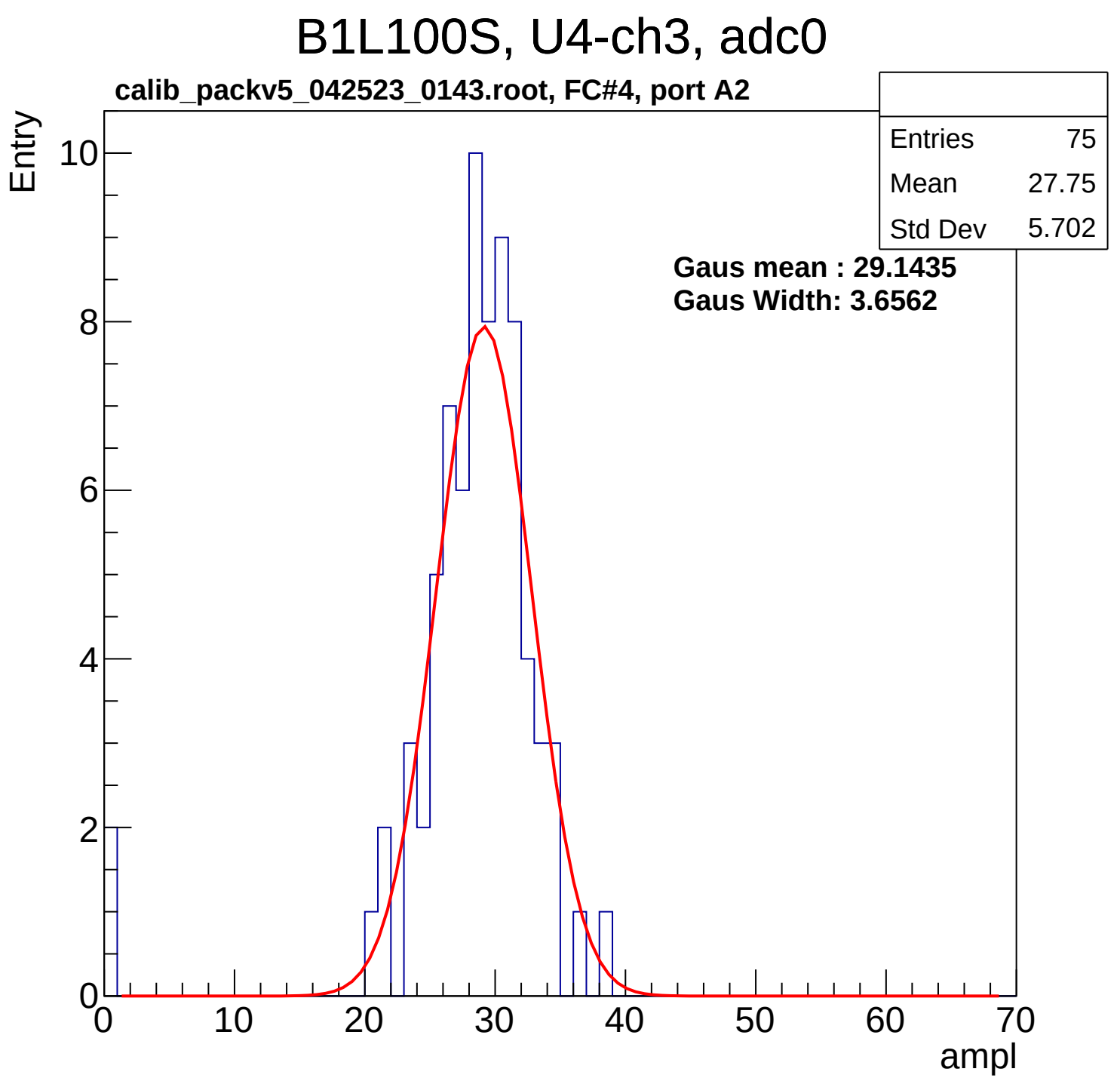

B1L100S, U4-ch2, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 48.97
Std Dev 4.056
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

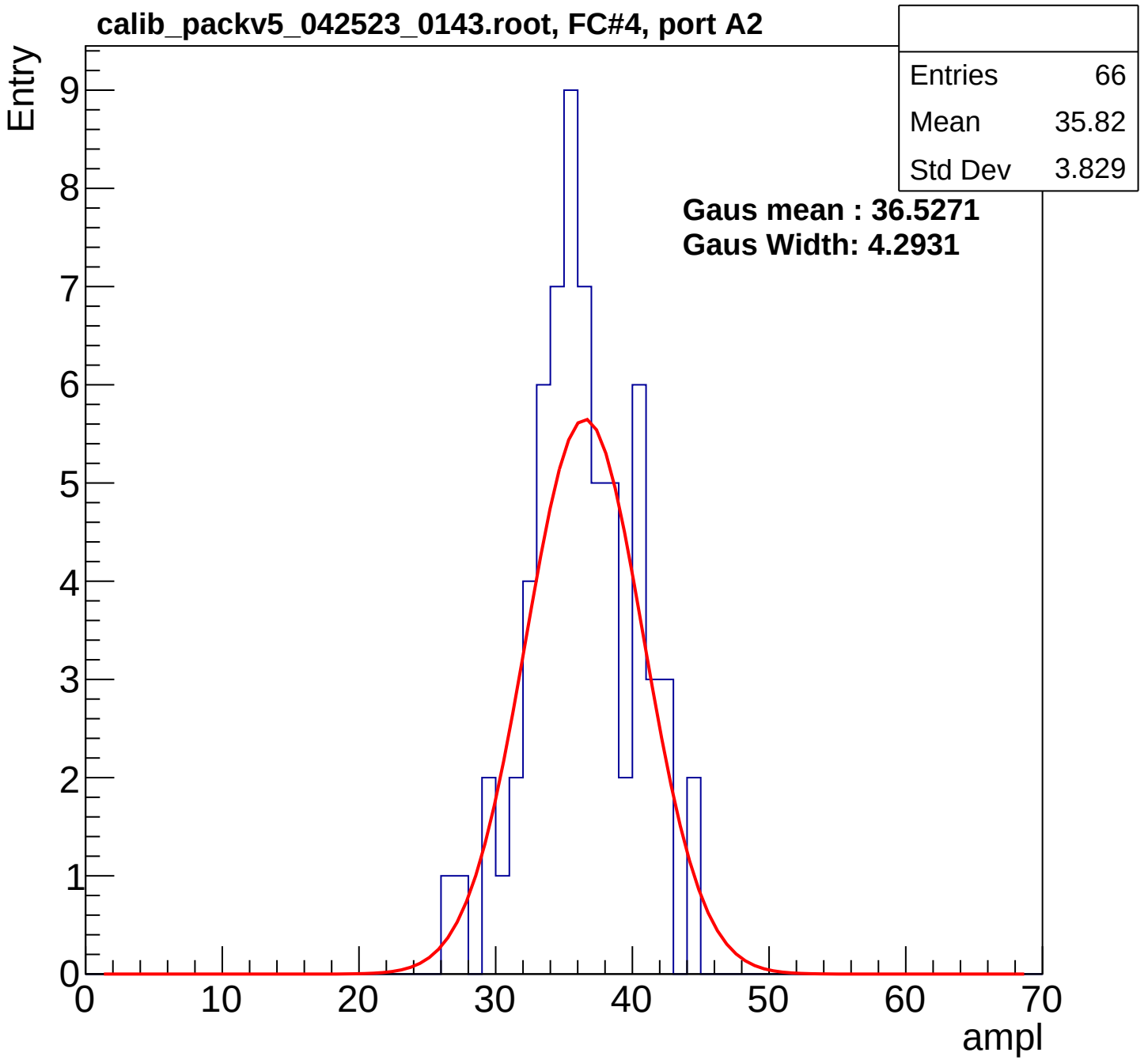

B1L100S, U4-ch2, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 55.33
Std Dev 3.572
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

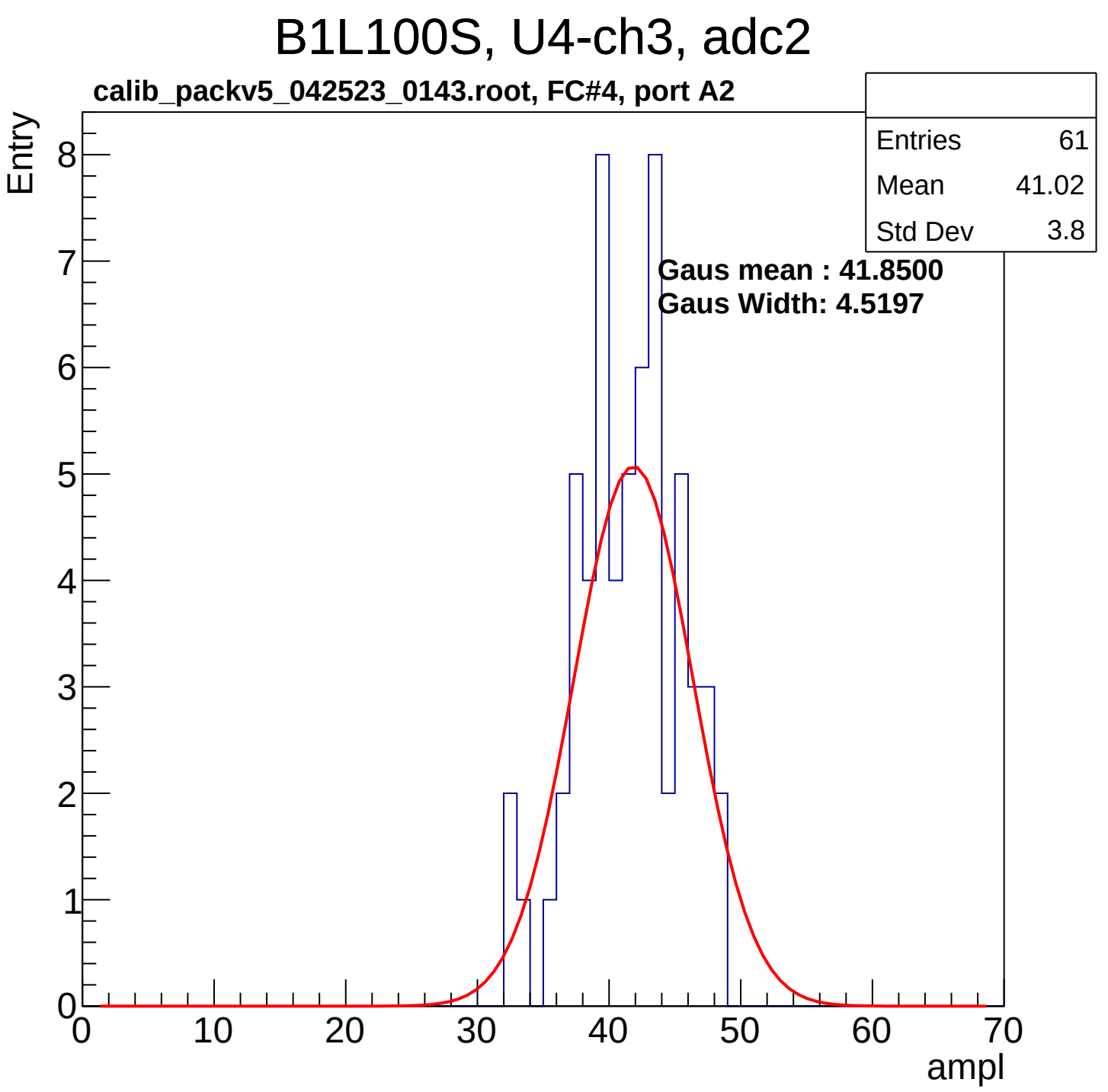

B1L100S, U4-ch2, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 35
Mean 60.03
Std Dev 2.286
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

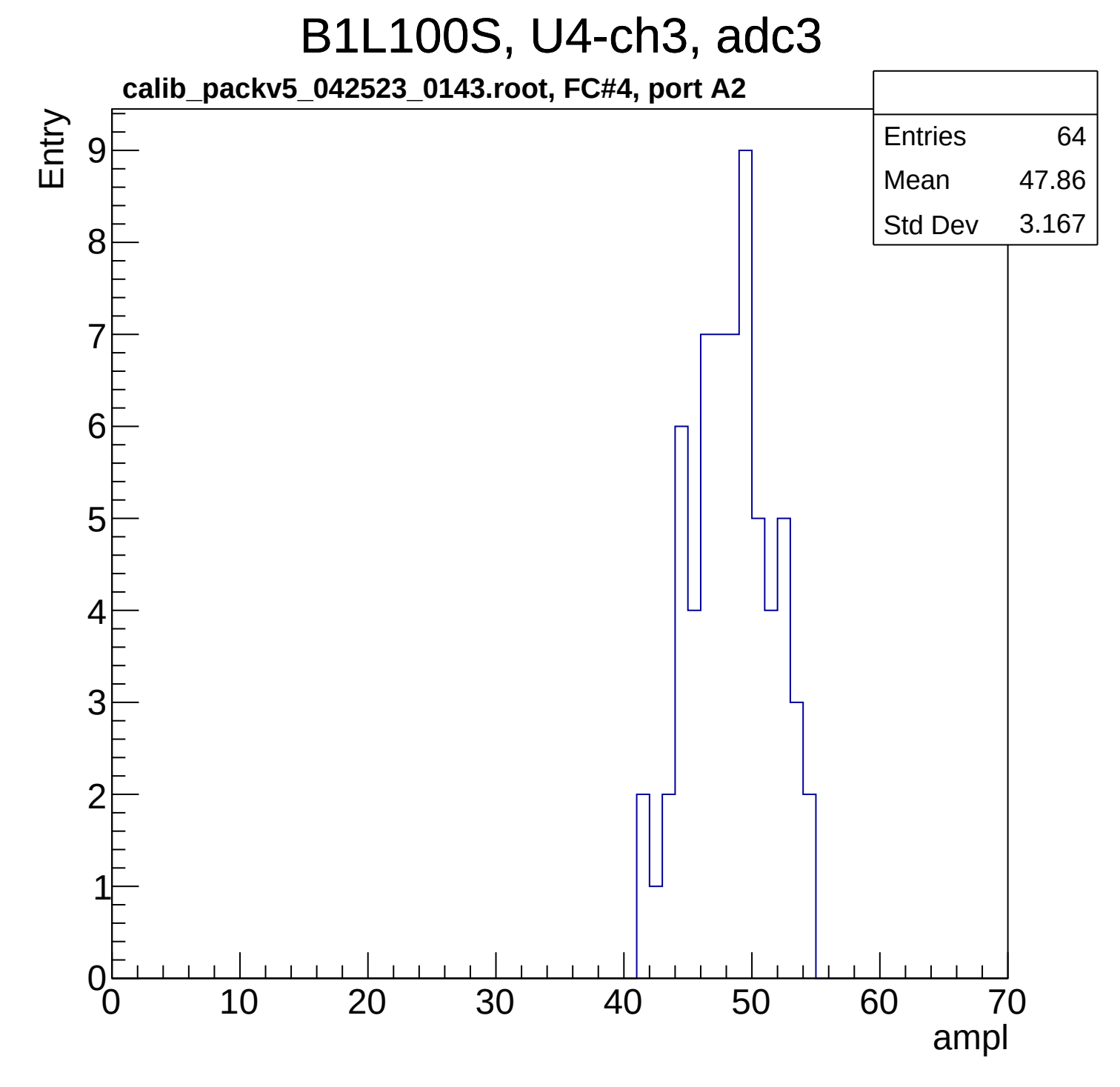

B1L100S, U4-ch2, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 56.45
Std Dev 17.88
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

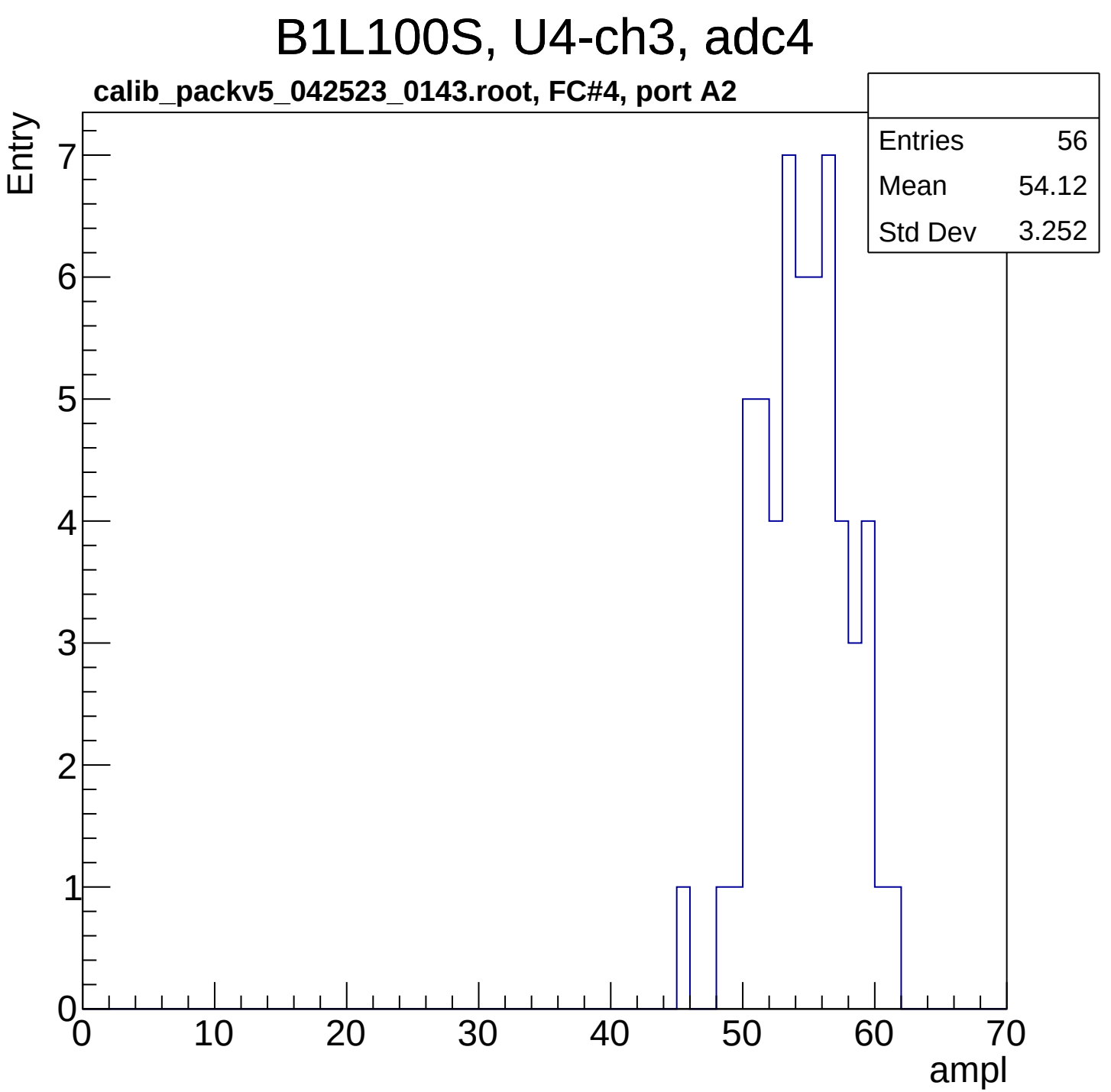

B1L100S, U4-ch2, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 7
Std Dev 9.899
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

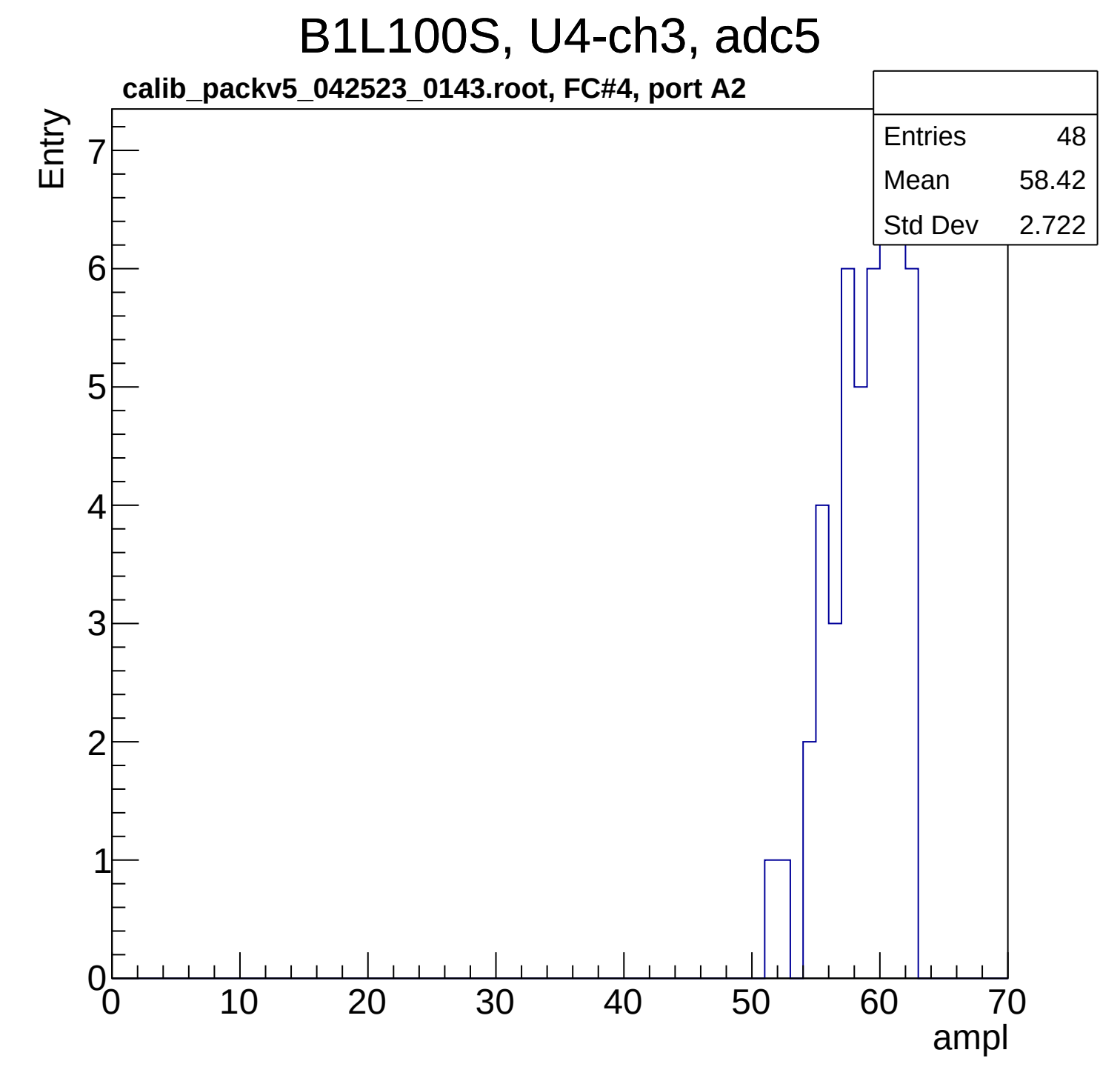

B1L100S, U4-ch3, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 27.75
Std Dev 5.702
Gaus mean : 29.1435
Gaus Width: 3.6562
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

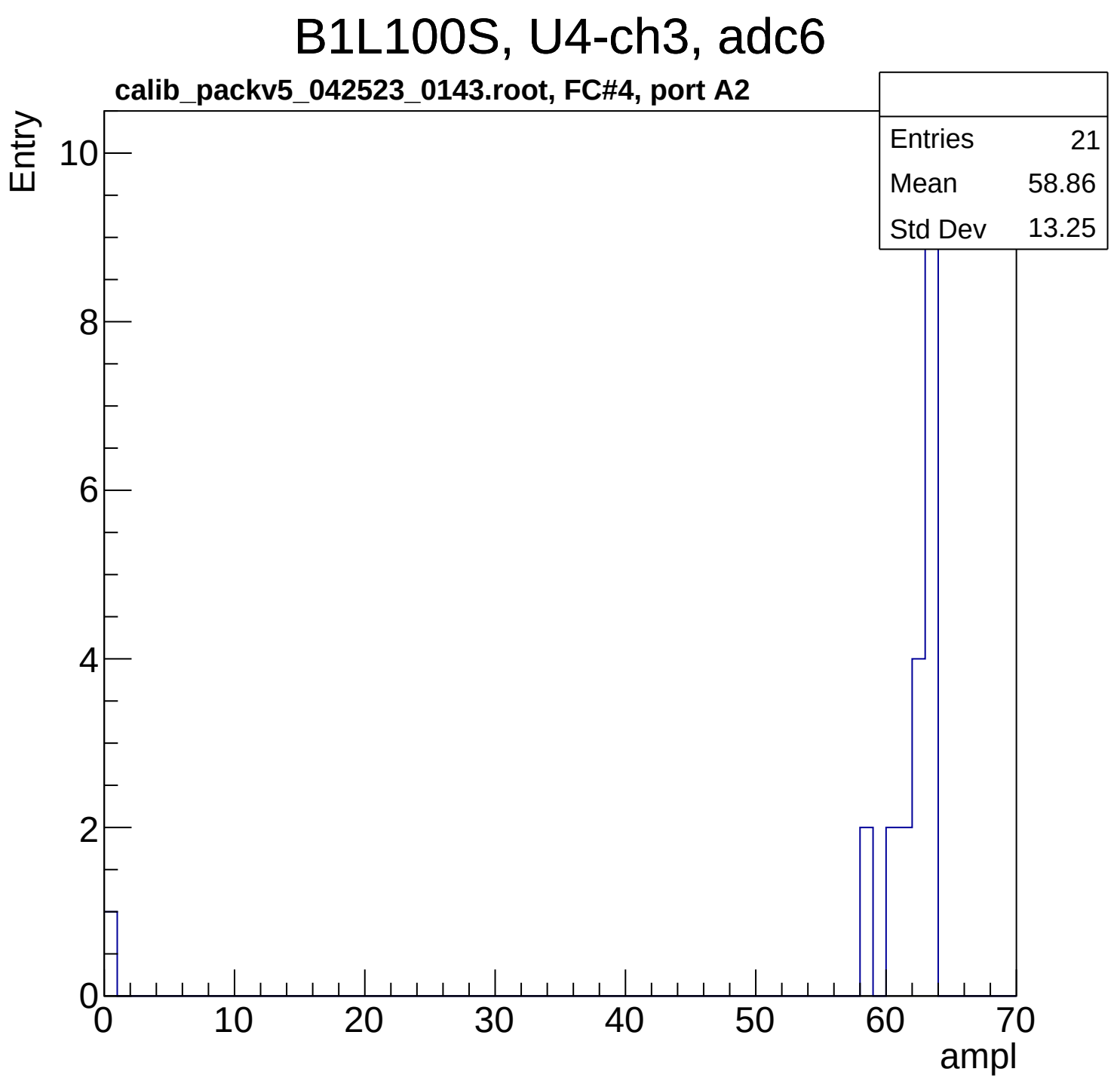

B1L100S, U4-ch3, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 35.82
Std Dev 3.829
Gaus mean : 36.5271
Gaus Width: 4.2931
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

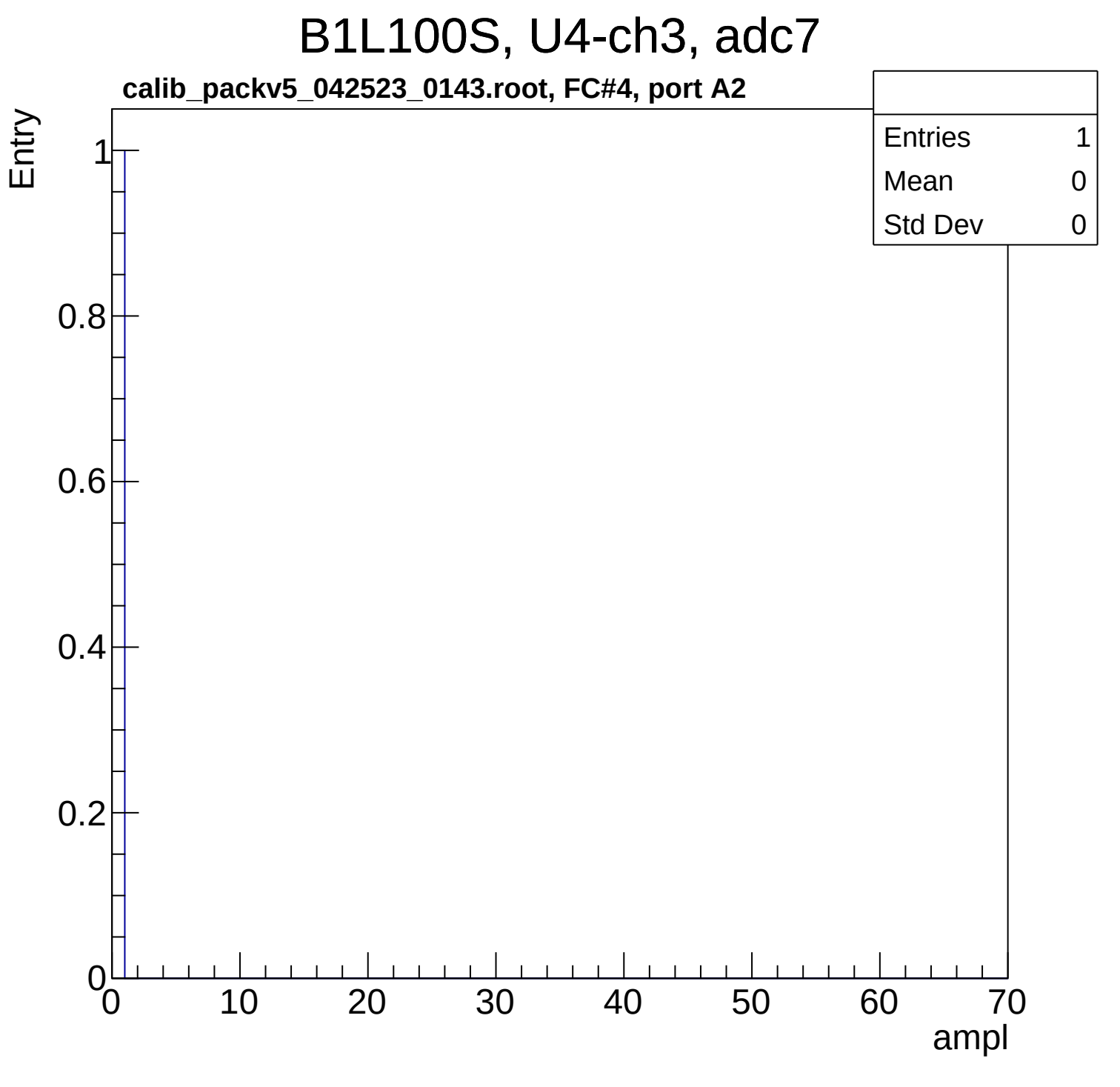

B1L100S, U4-ch3, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 41.02
Std Dev 3.8
Gaus mean : 41.8500
Gaus Width: 4.5197
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

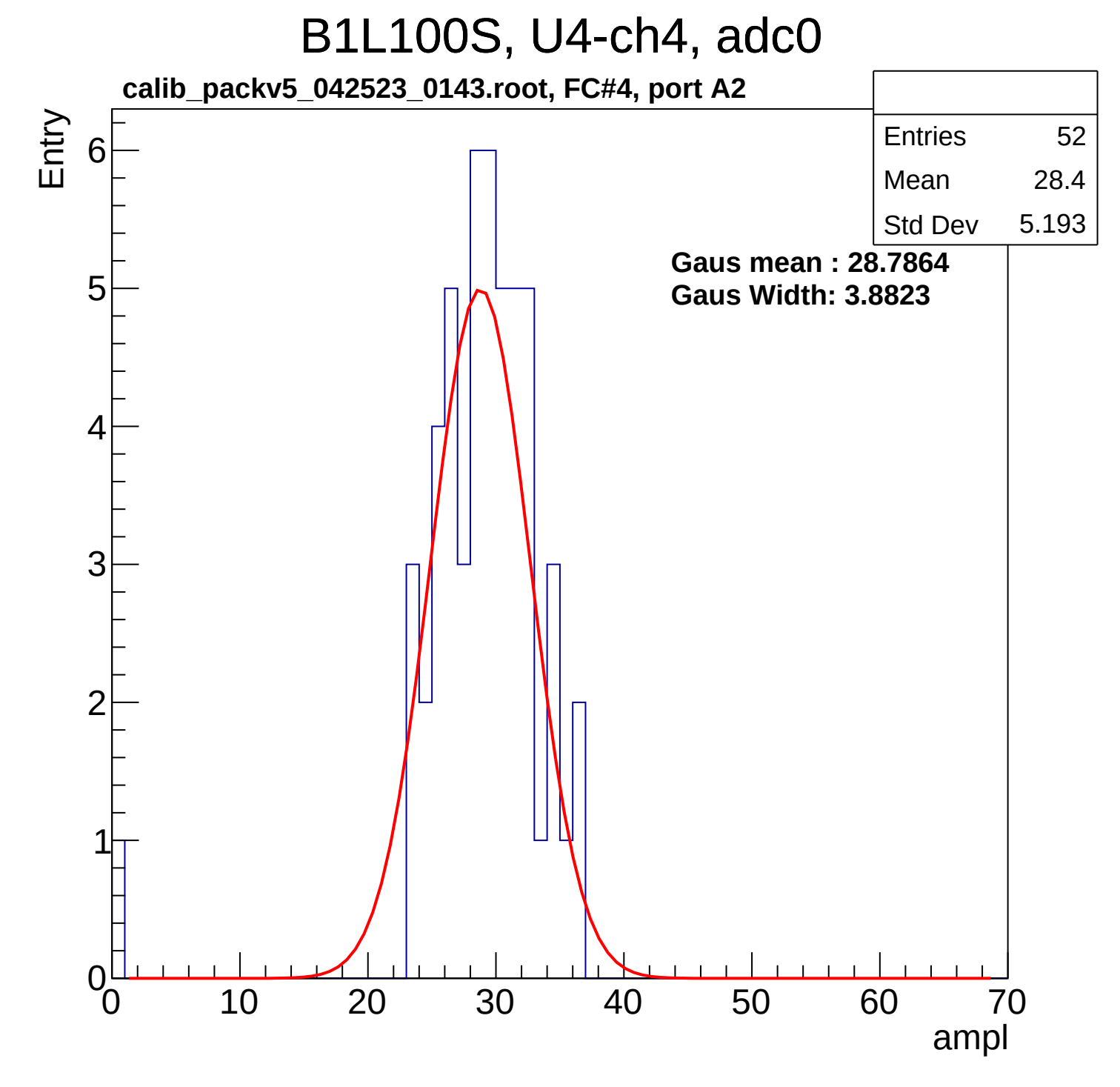

B1L100S, U4-ch3, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 47.86
Std Dev 3.167
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

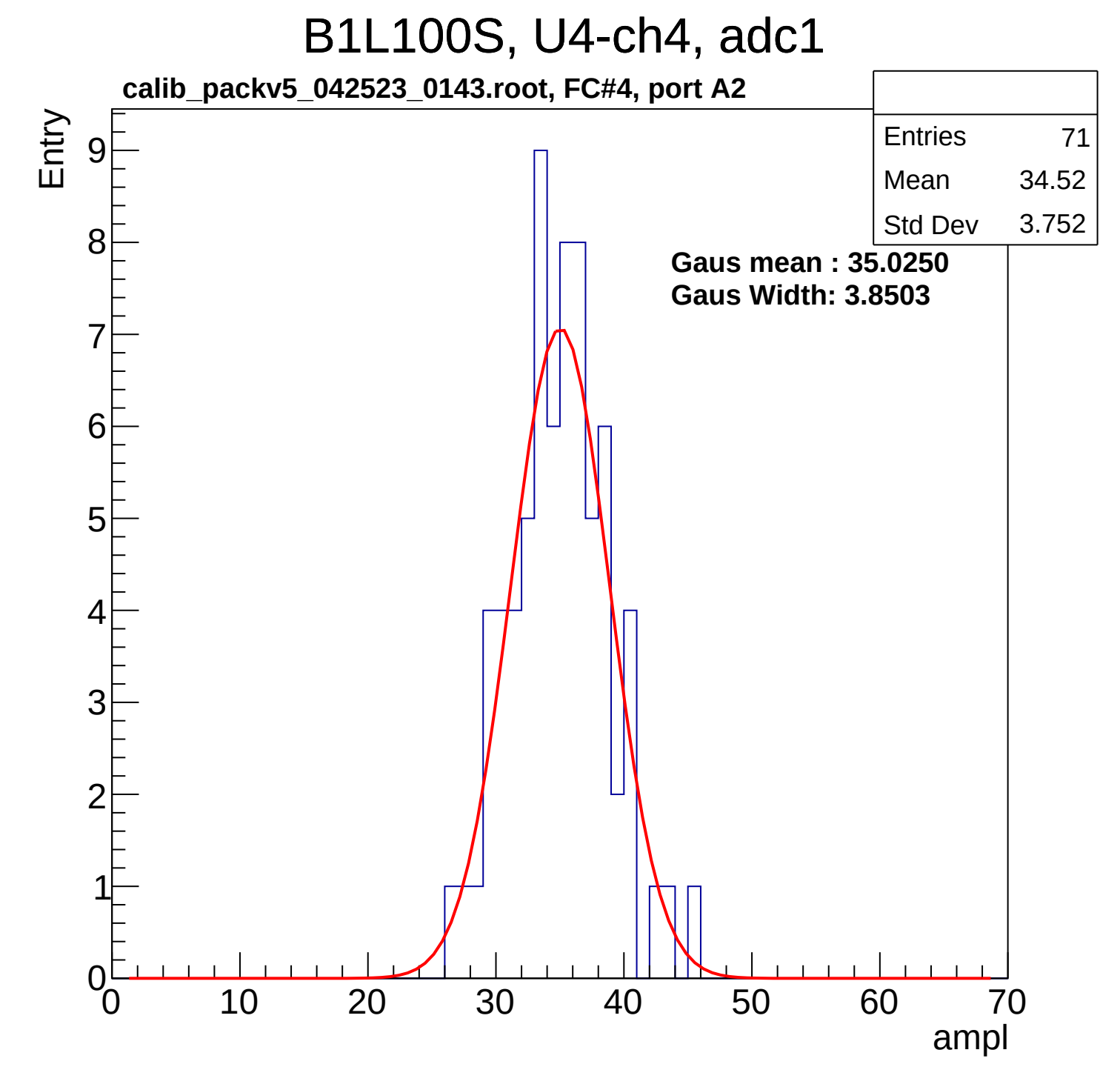

B1L100S, U4-ch3, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 54.12
Std Dev 3.252
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

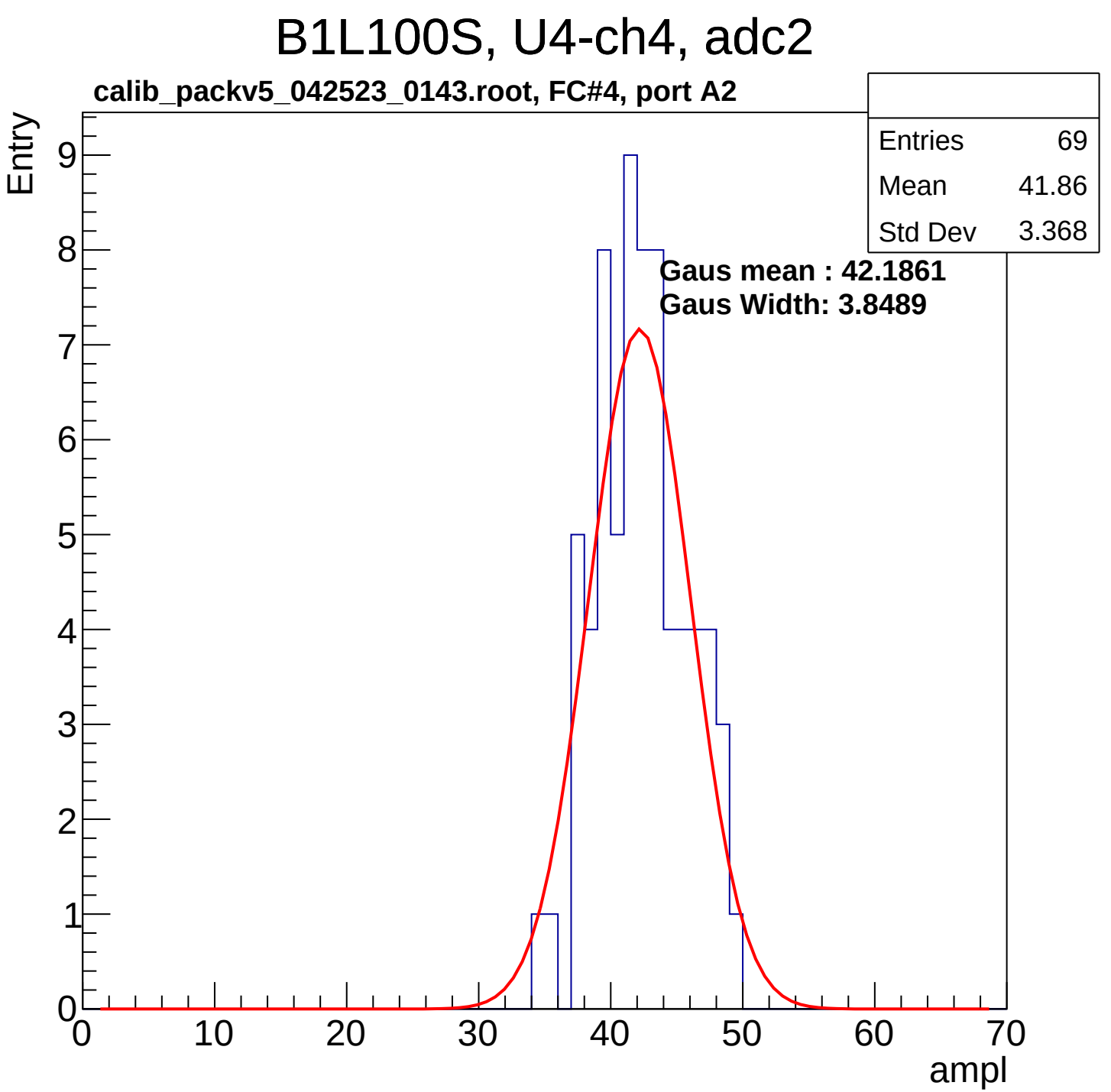

B1L100S, U4-ch3, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 58.42
Std Dev 2.722
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

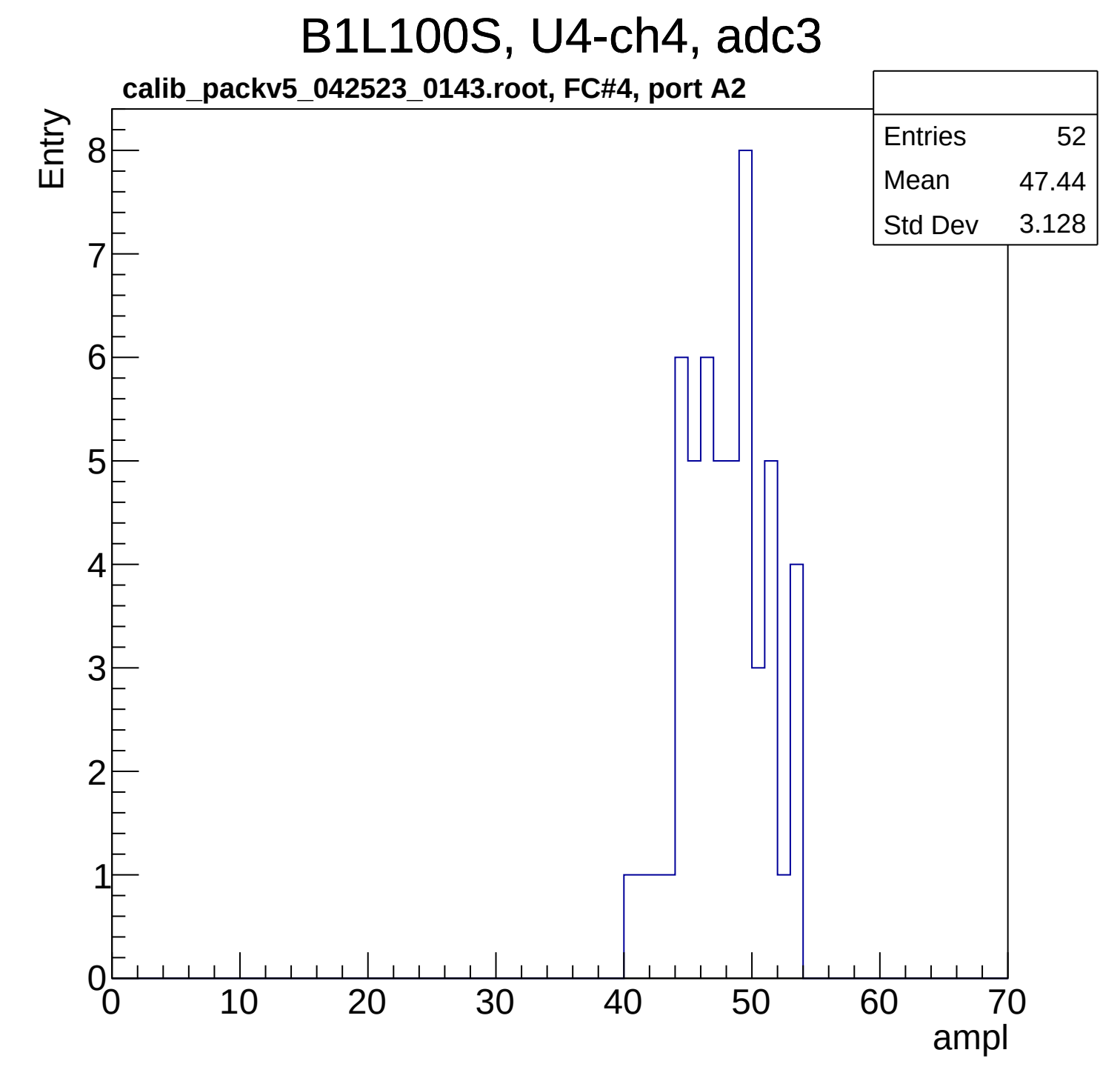

B1L100S, U4-ch3, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 21
Mean 58.86
Std Dev 13.25
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

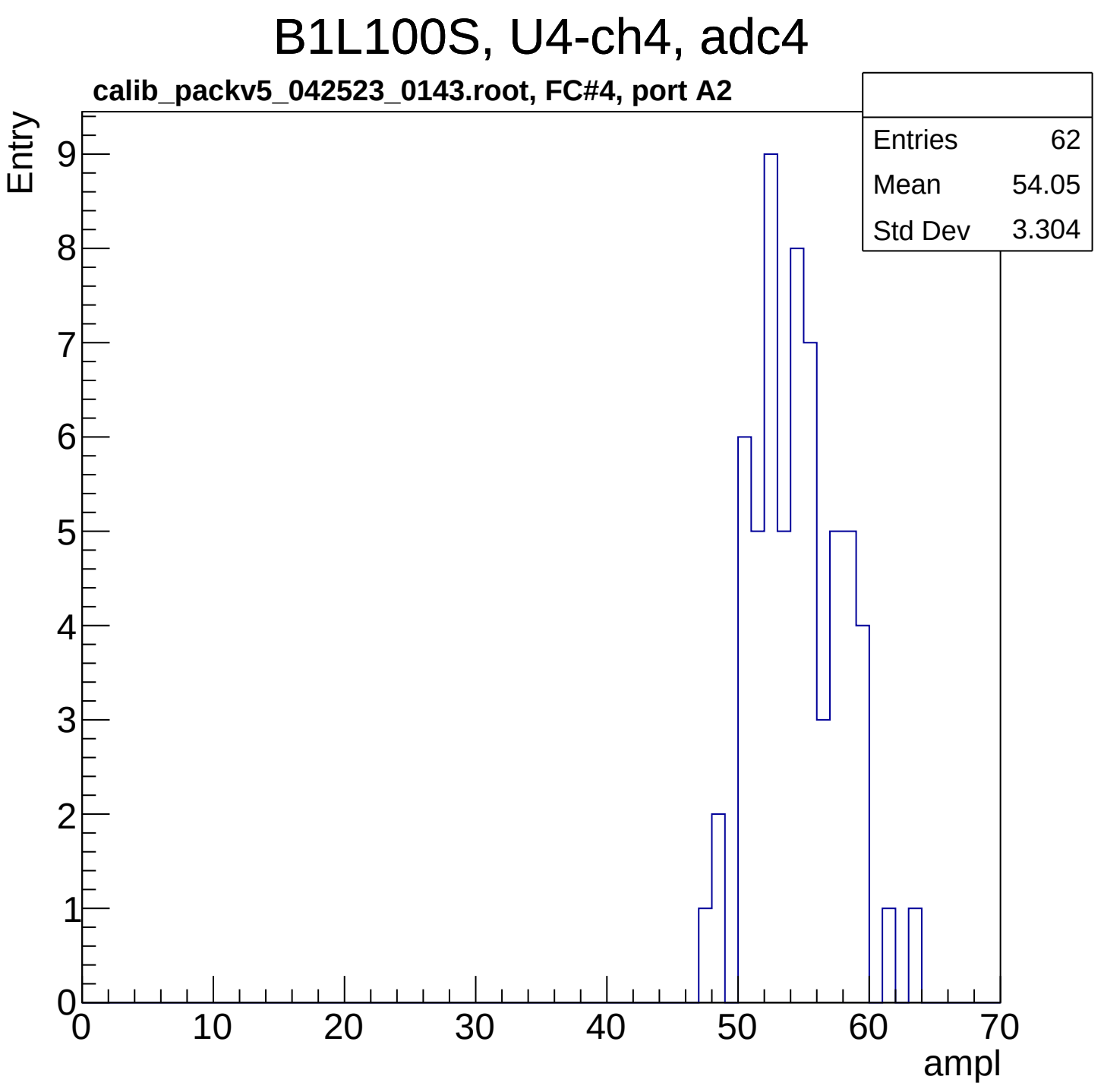

B1L100S, U4-ch3, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

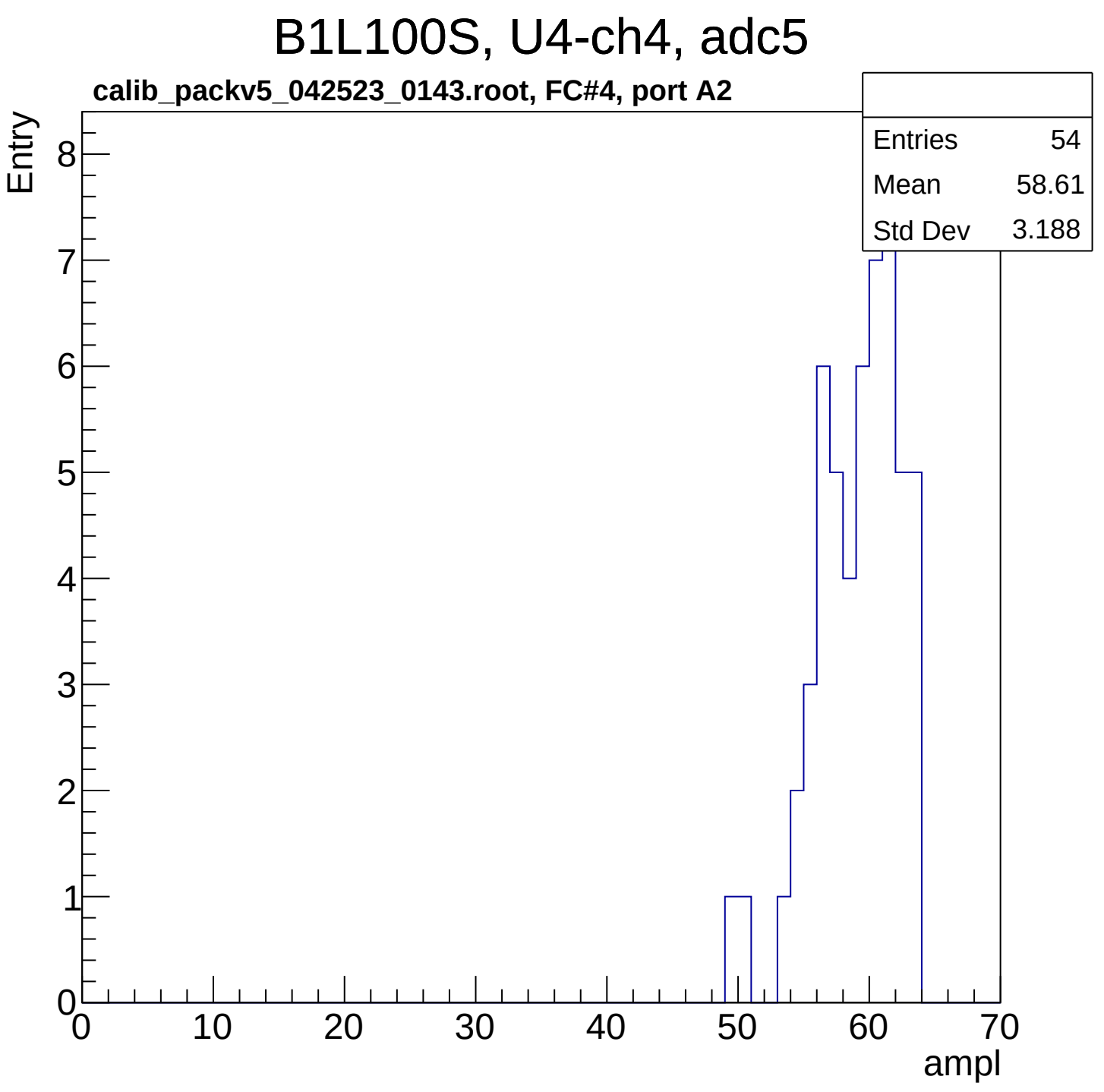

B1L100S, U4-ch4, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 28.4
Std Dev 5.193
Gaus mean : 28.7864
Gaus Width: 3.8823
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

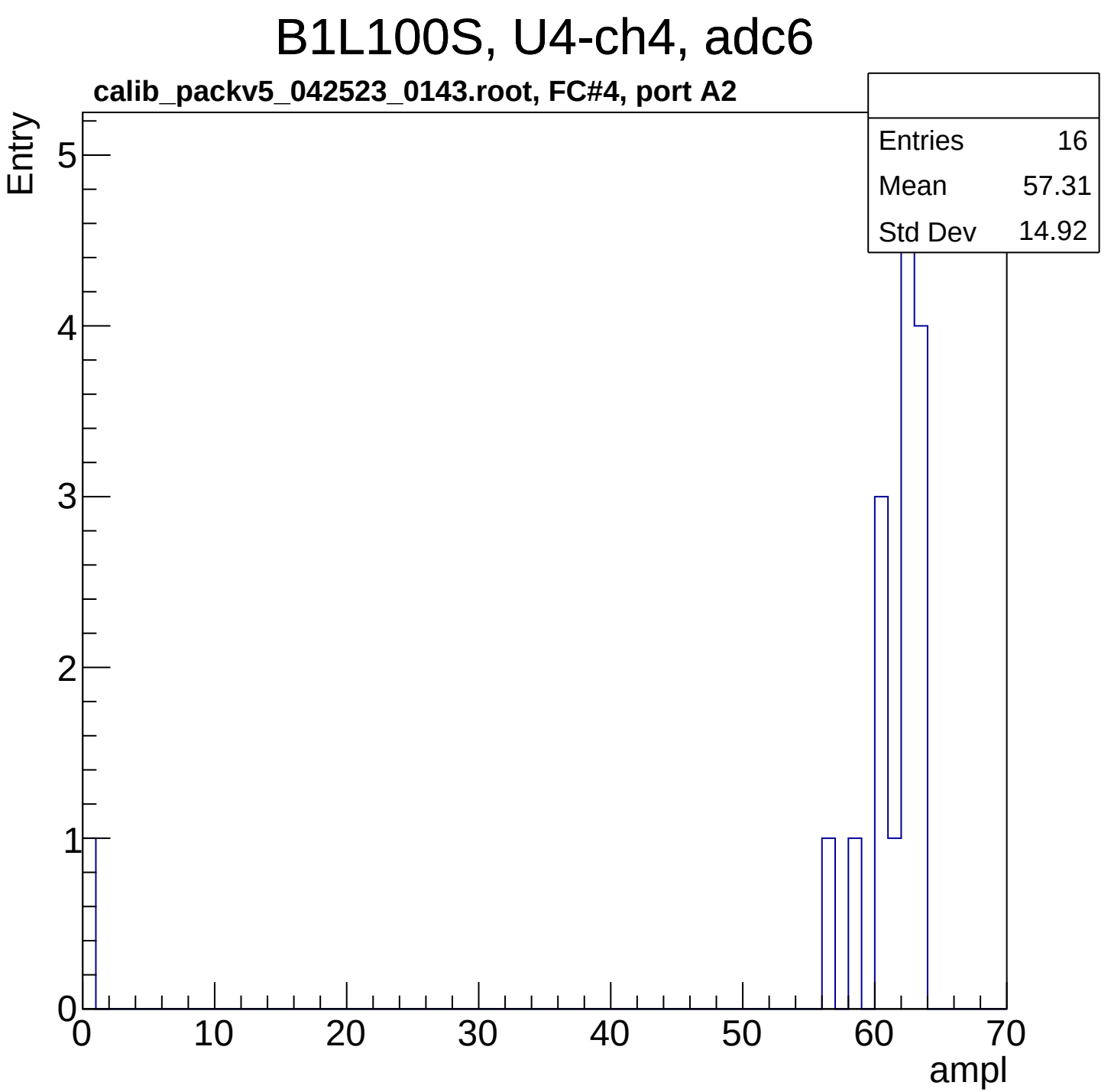

B1L100S, U4-ch4, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 34.52
Std Dev 3.752
Gaus mean : 35.0250
Gaus Width: 3.8503
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

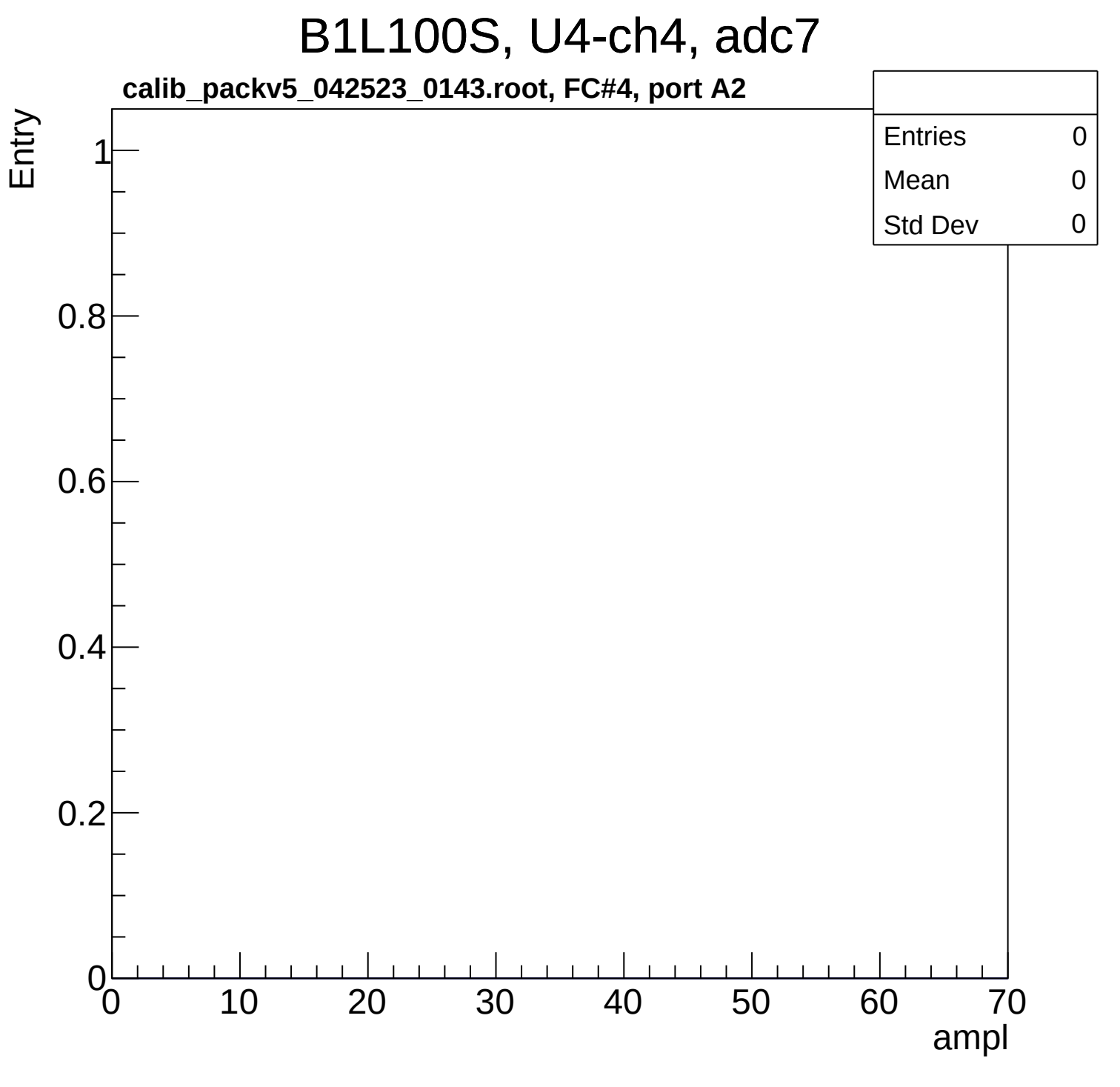

B1L100S, U4-ch4, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 41.86
Std Dev 3.368
Gaus mean : 42.1861
Gaus Width: 3.8489
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

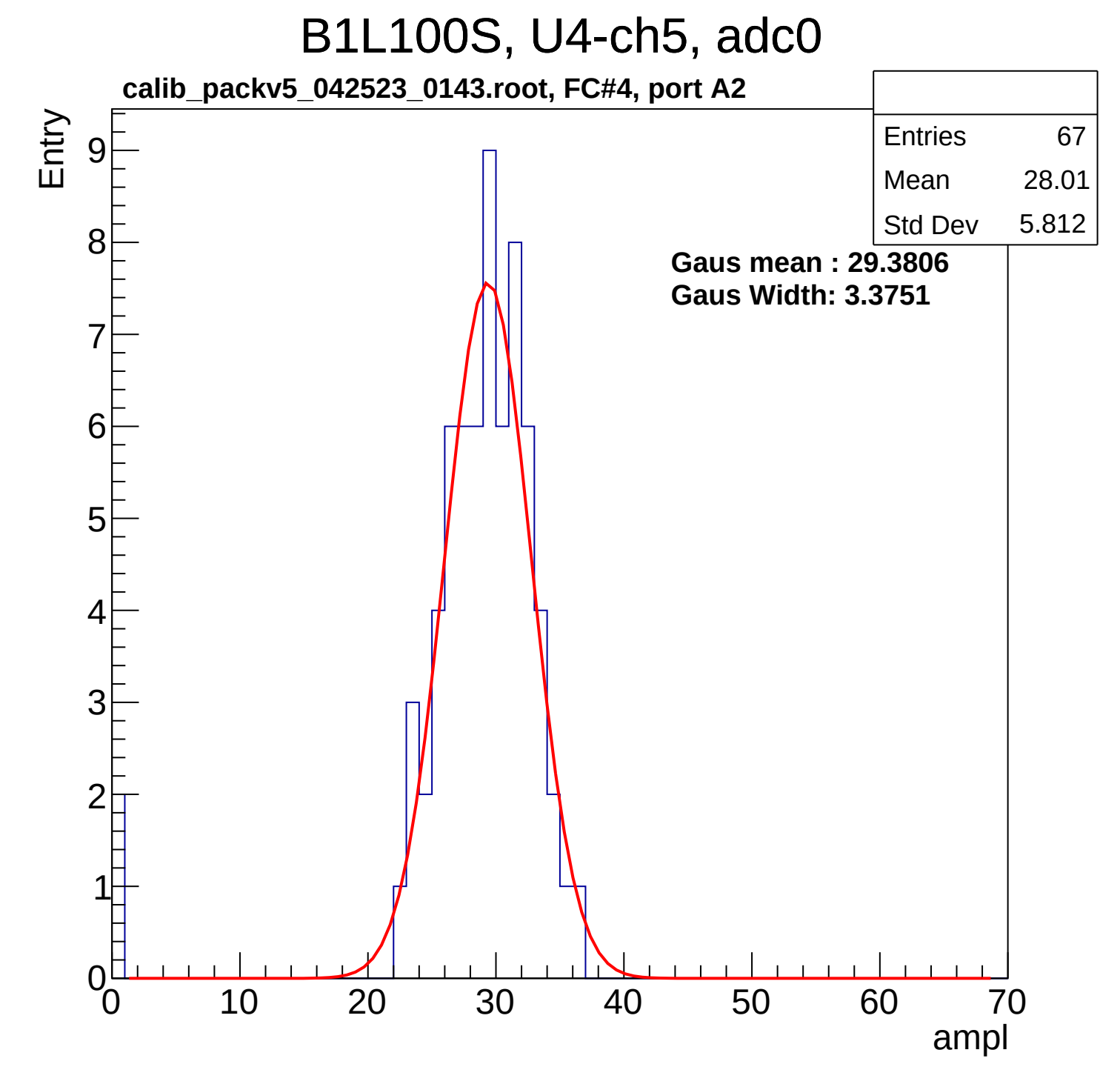

B1L100S, U4-ch4, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 47.44
Std Dev 3.128
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

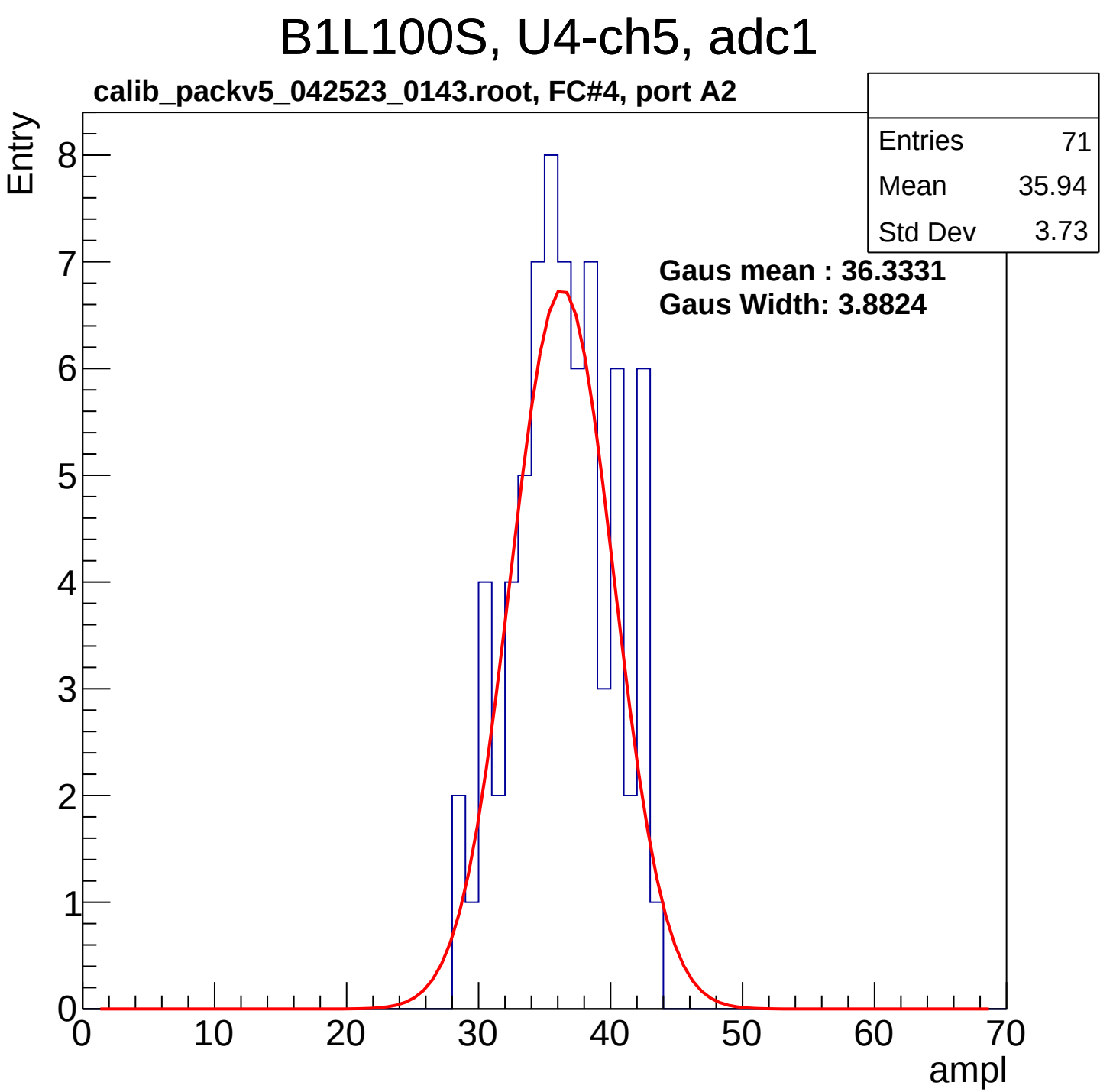

B1L100S, U4-ch4, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 54.05
Std Dev 3.304
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

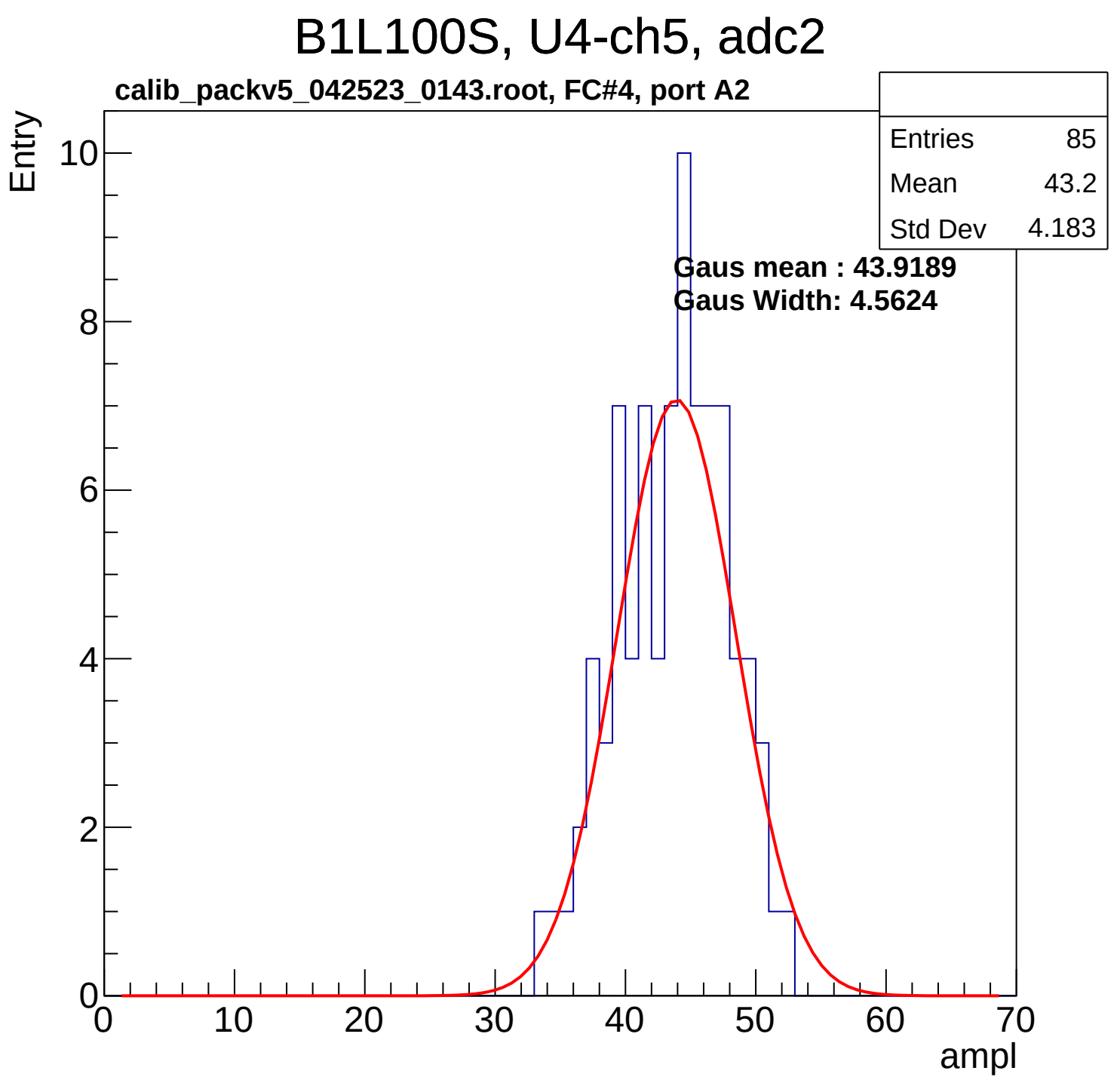

B1L100S, U4-ch4, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 58.61
Std Dev 3.188
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

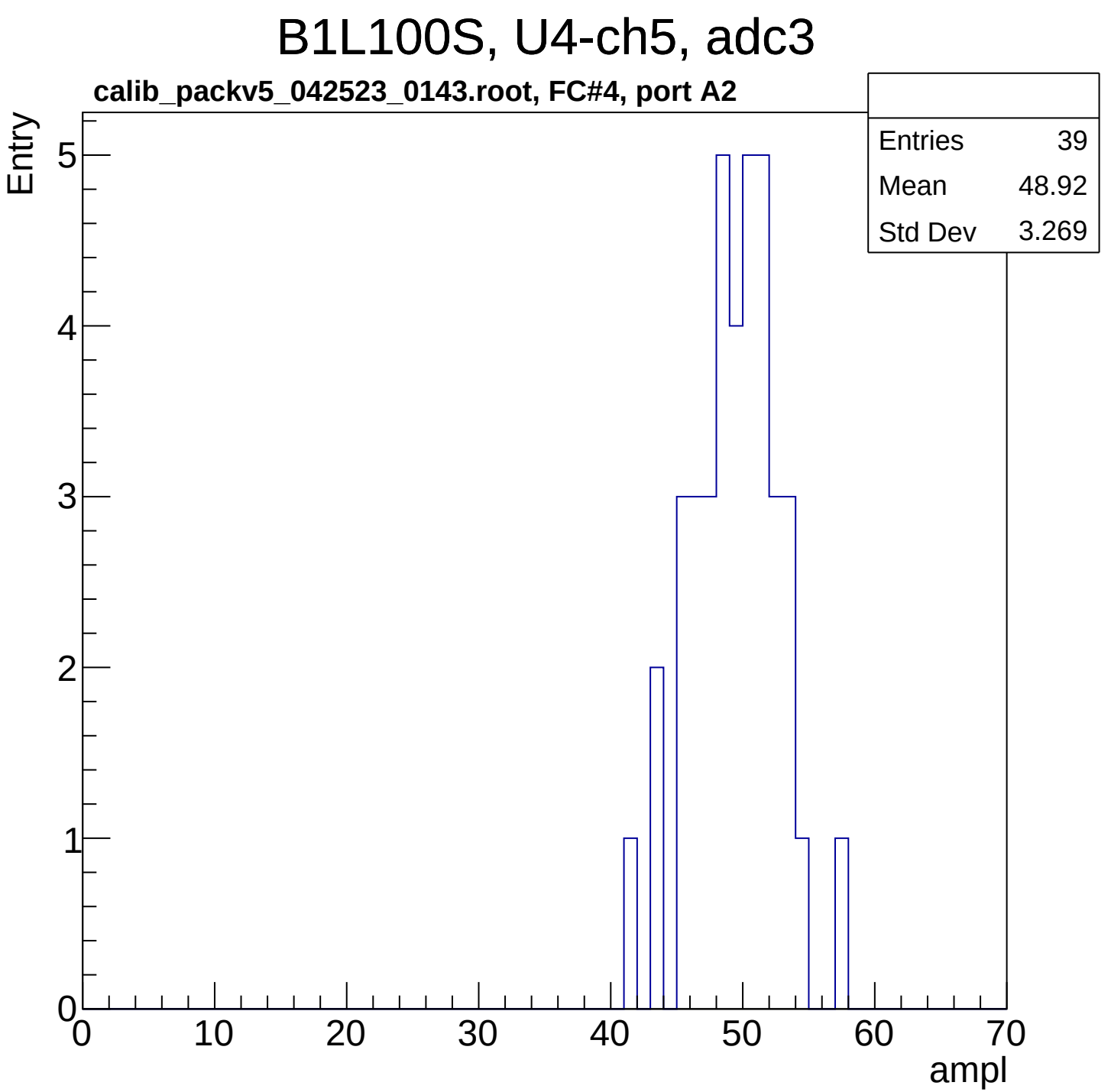

B1L100S, U4-ch4, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 16
Mean 57.31
Std Dev 14.92
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

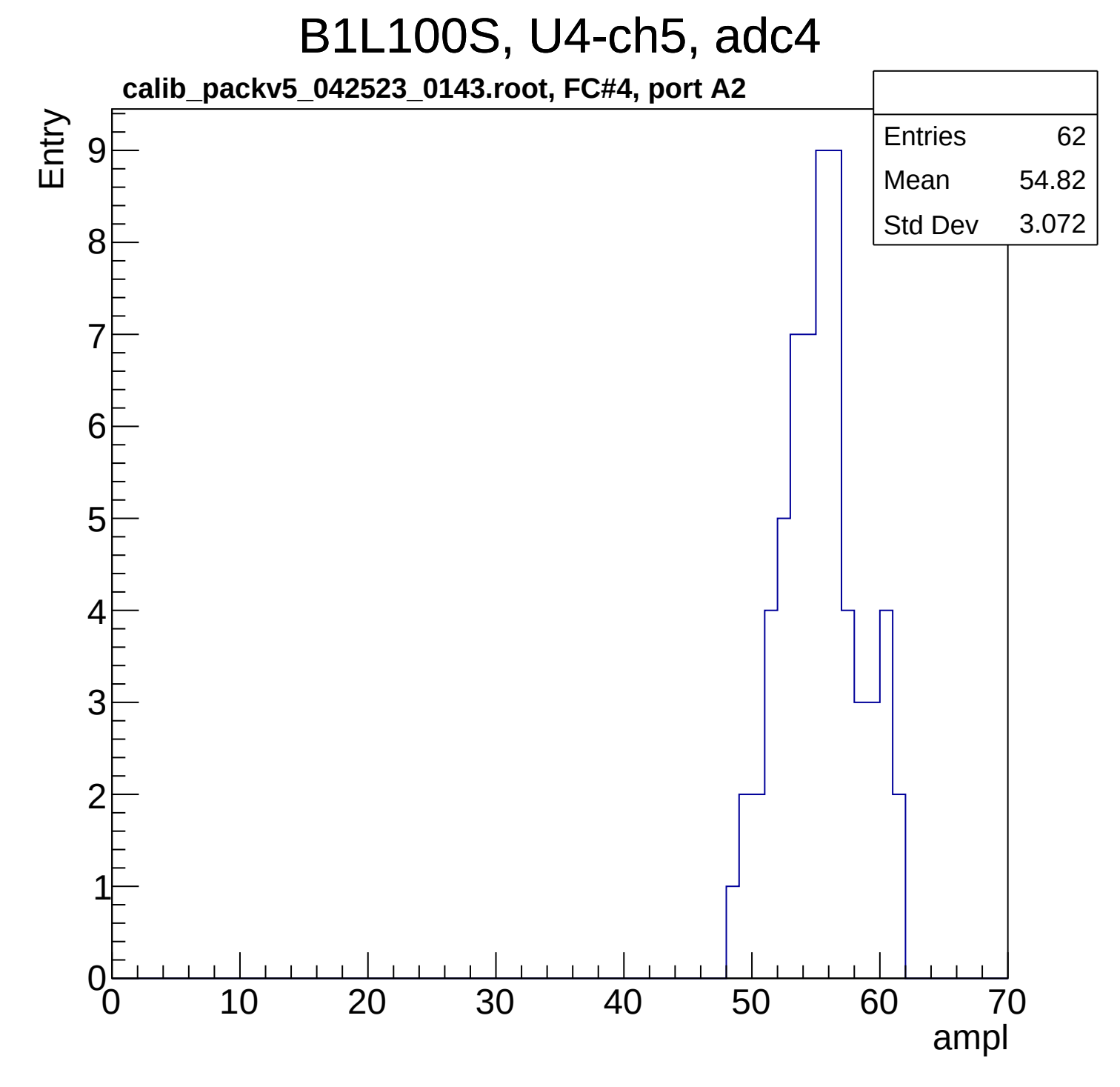

B1L100S, U4-ch4, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

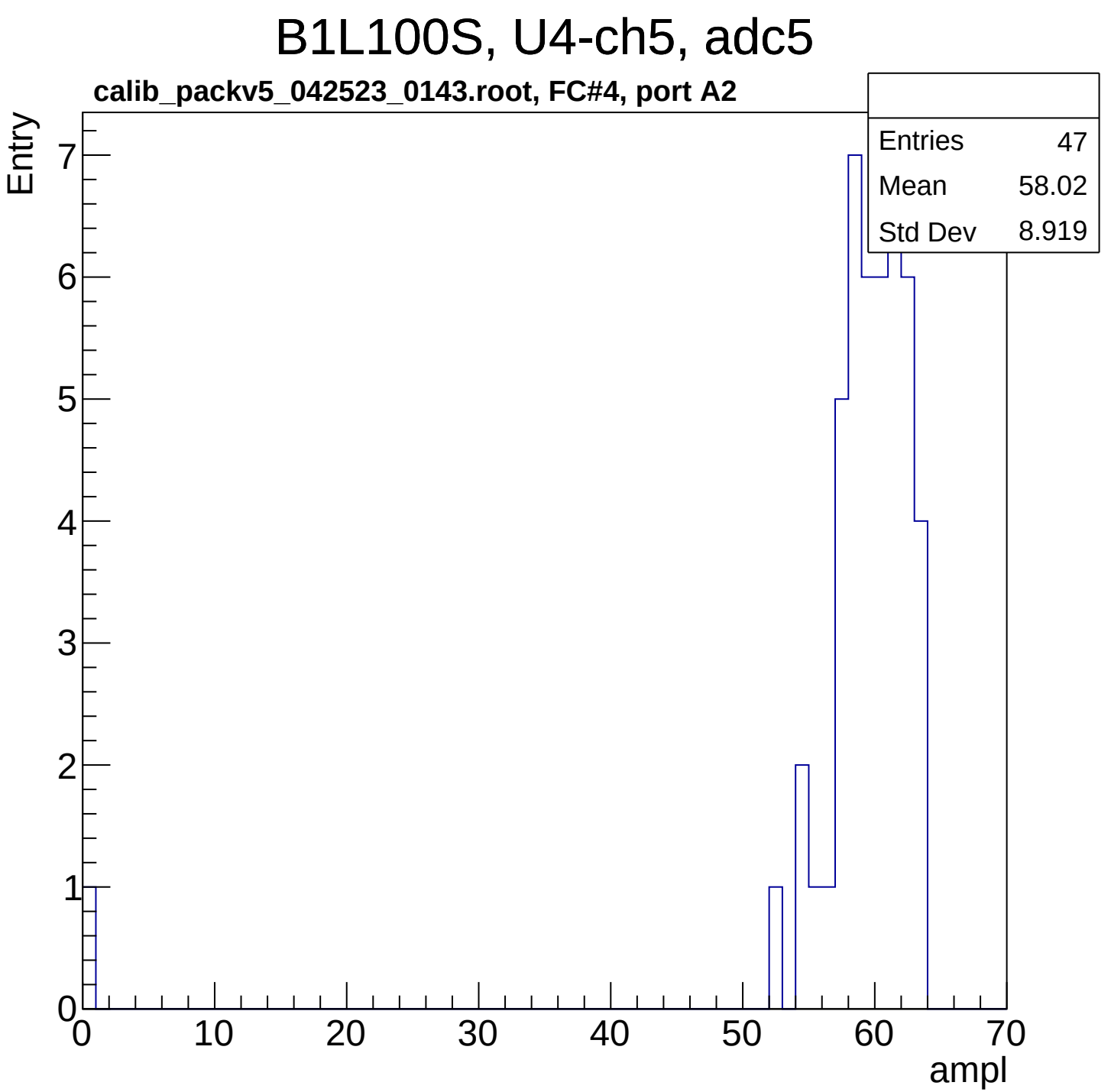

B1L100S, U4-ch5, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 28.01
Std Dev 5.812
Gaus mean : 29.3806
Gaus Width: 3.3751
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

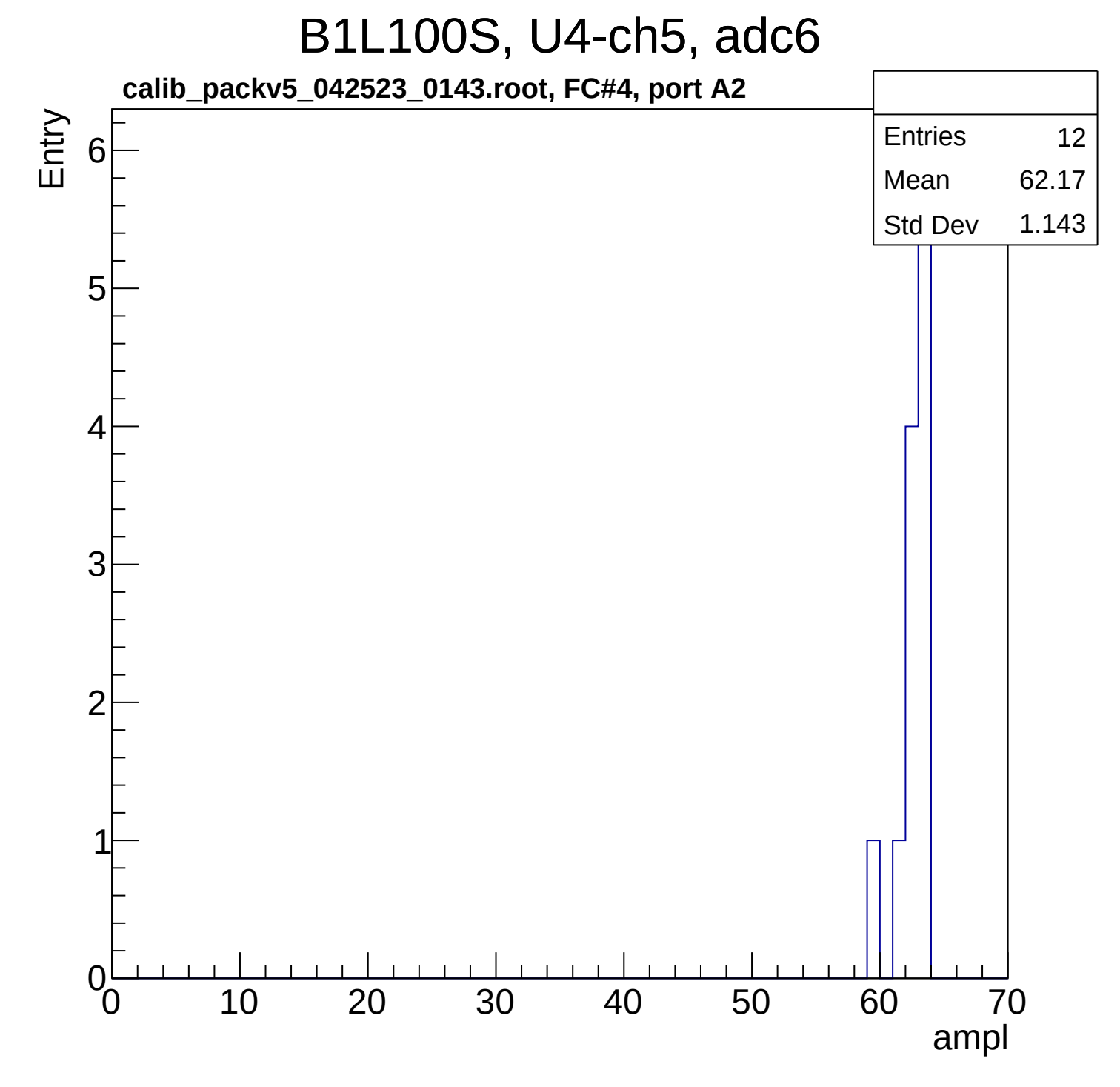

B1L100S, U4-ch5, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 35.94
Std Dev 3.73
Gaus mean : 36.3331
Gaus Width: 3.8824
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

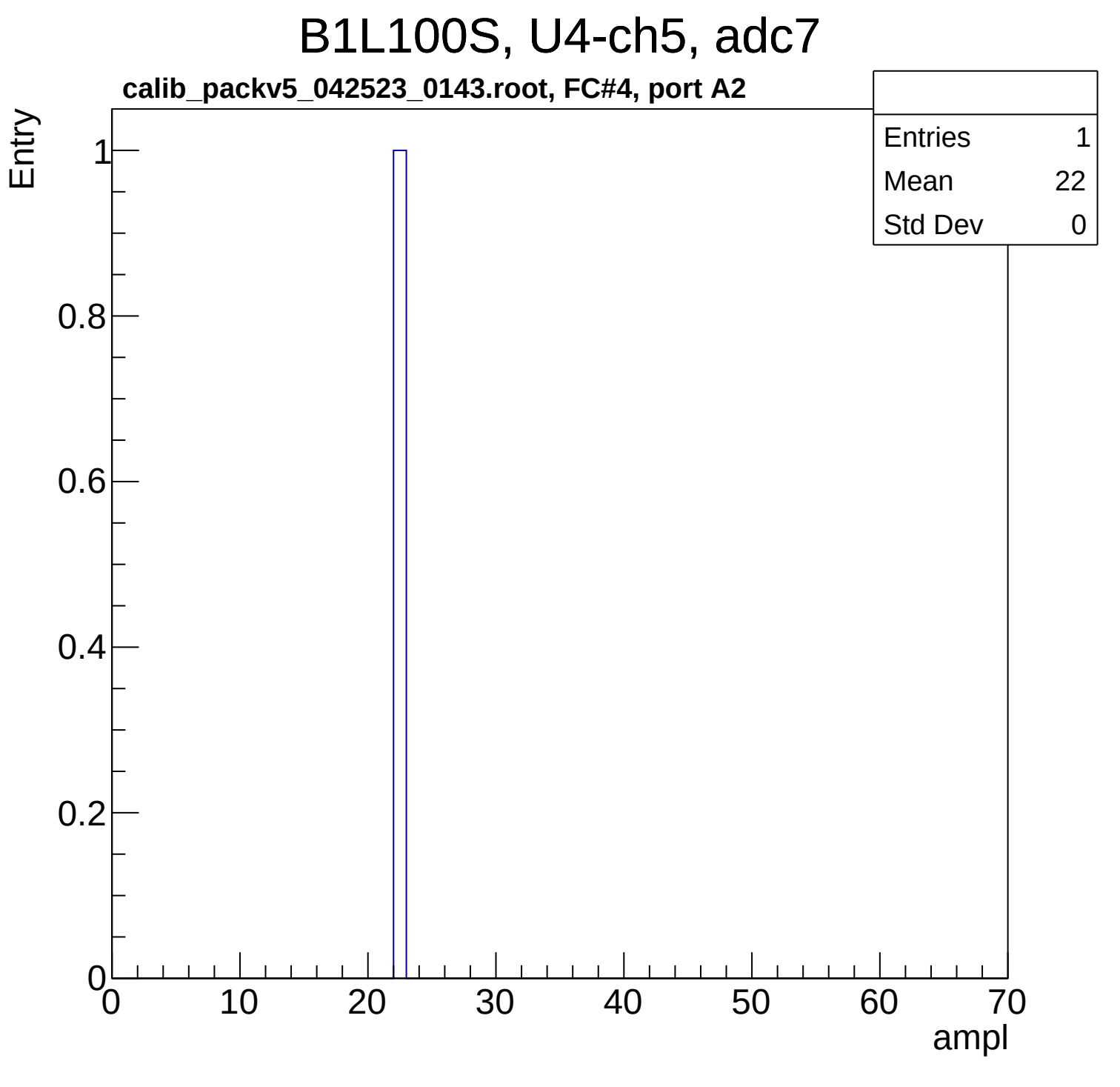

B1L100S, U4-ch5, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 85
Mean 43.2
Std Dev 4.183
Gaus mean : 43.9189
Gaus Width: 4.5624
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

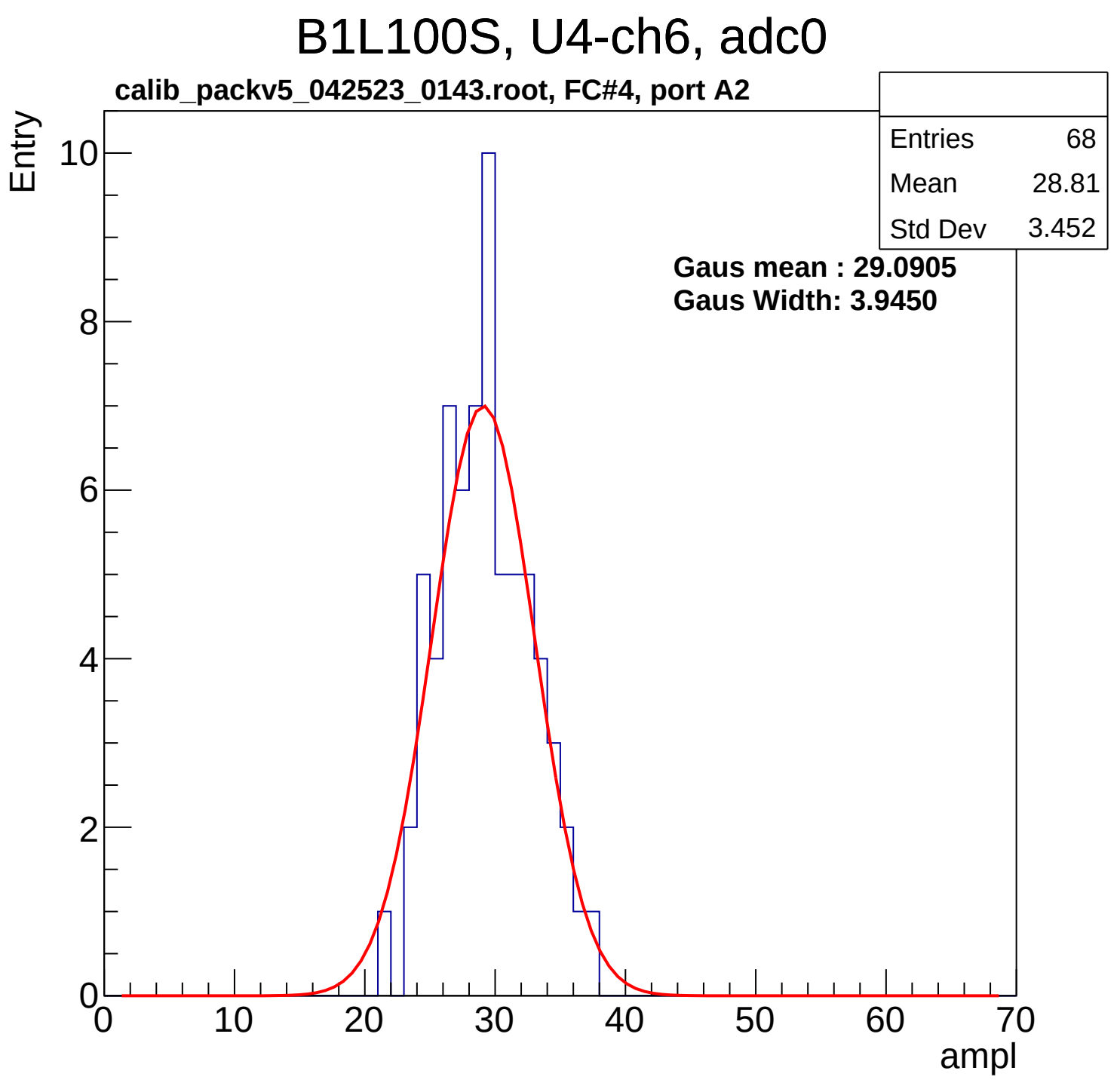

B1L100S, U4-ch5, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 39
Mean 48.92
Std Dev 3.269
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

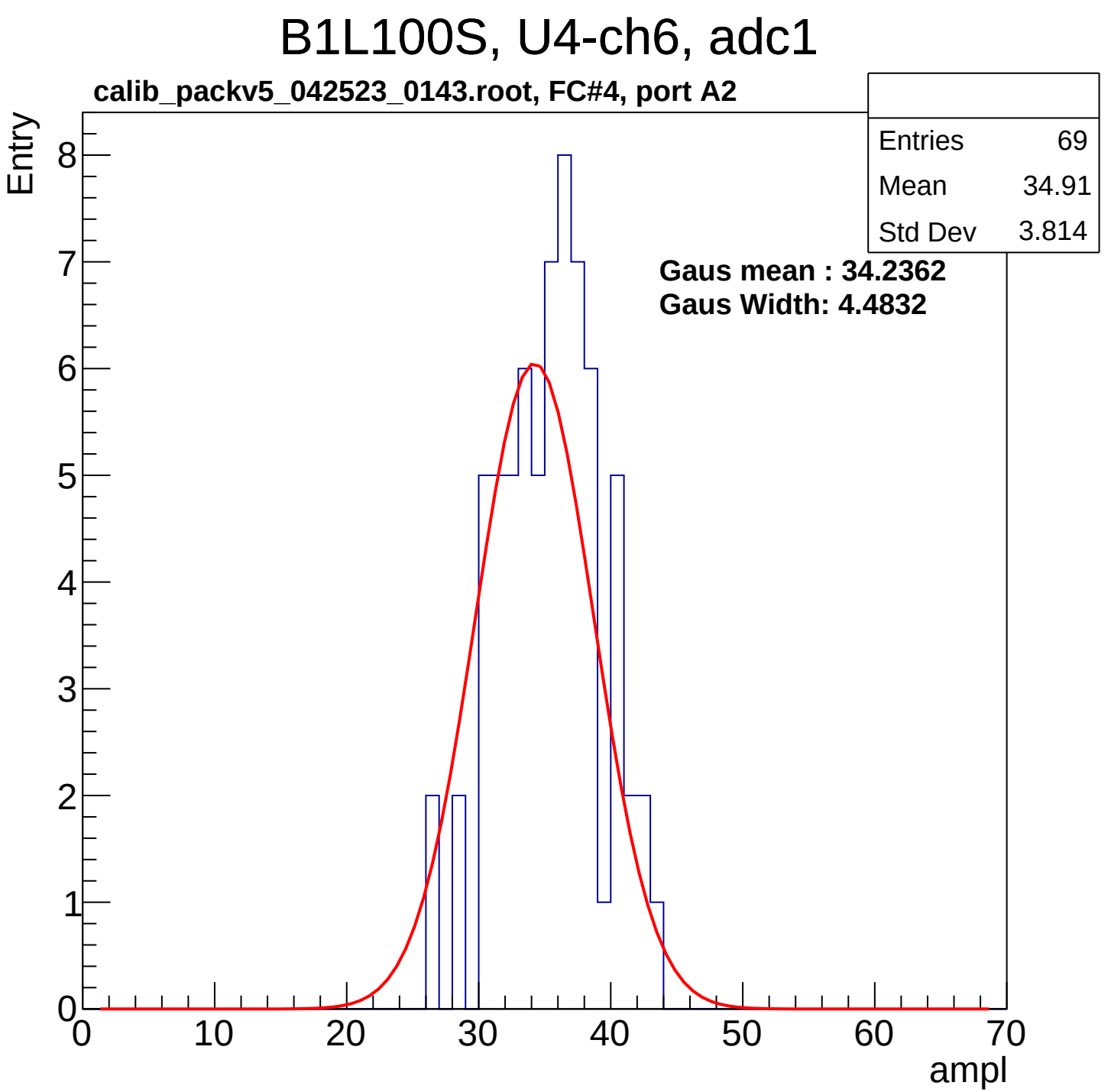

B1L100S, U4-ch5, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 54.82
Std Dev 3.072
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

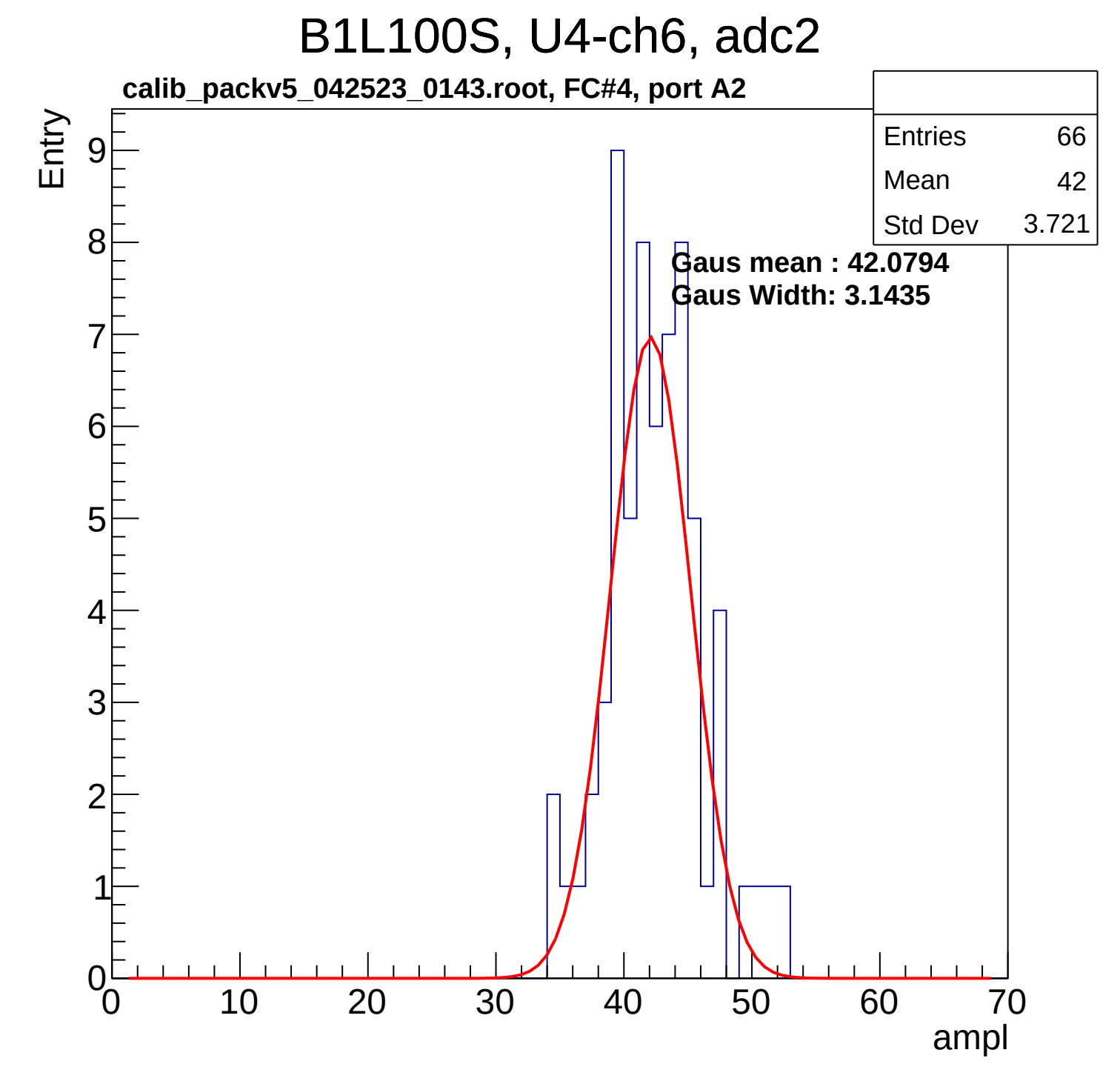

B1L100S, U4-ch5, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 58.02
Std Dev 8.919
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

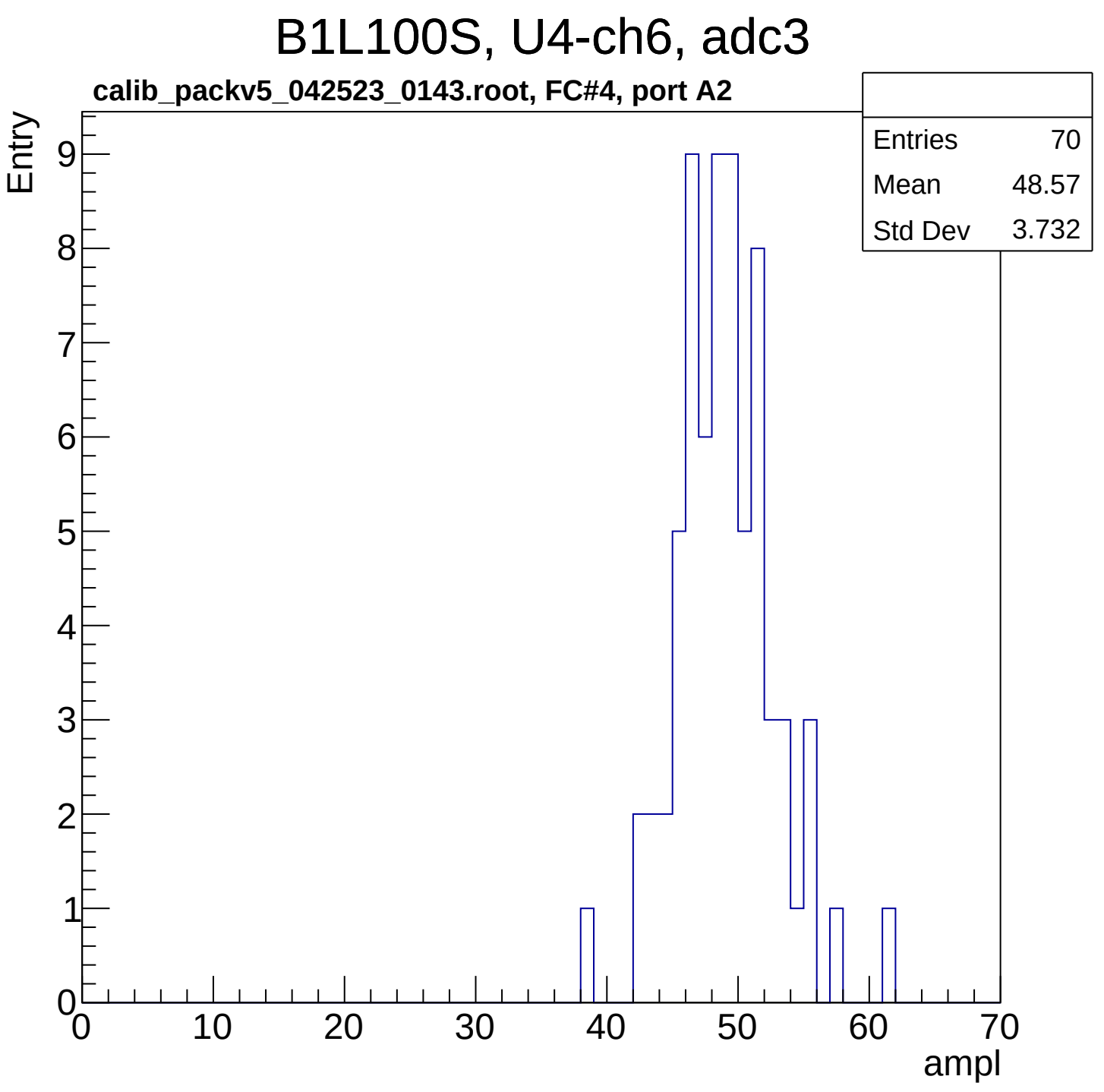

B1L100S, U4-ch5, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 12
Mean 62.17
Std Dev 1.143
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

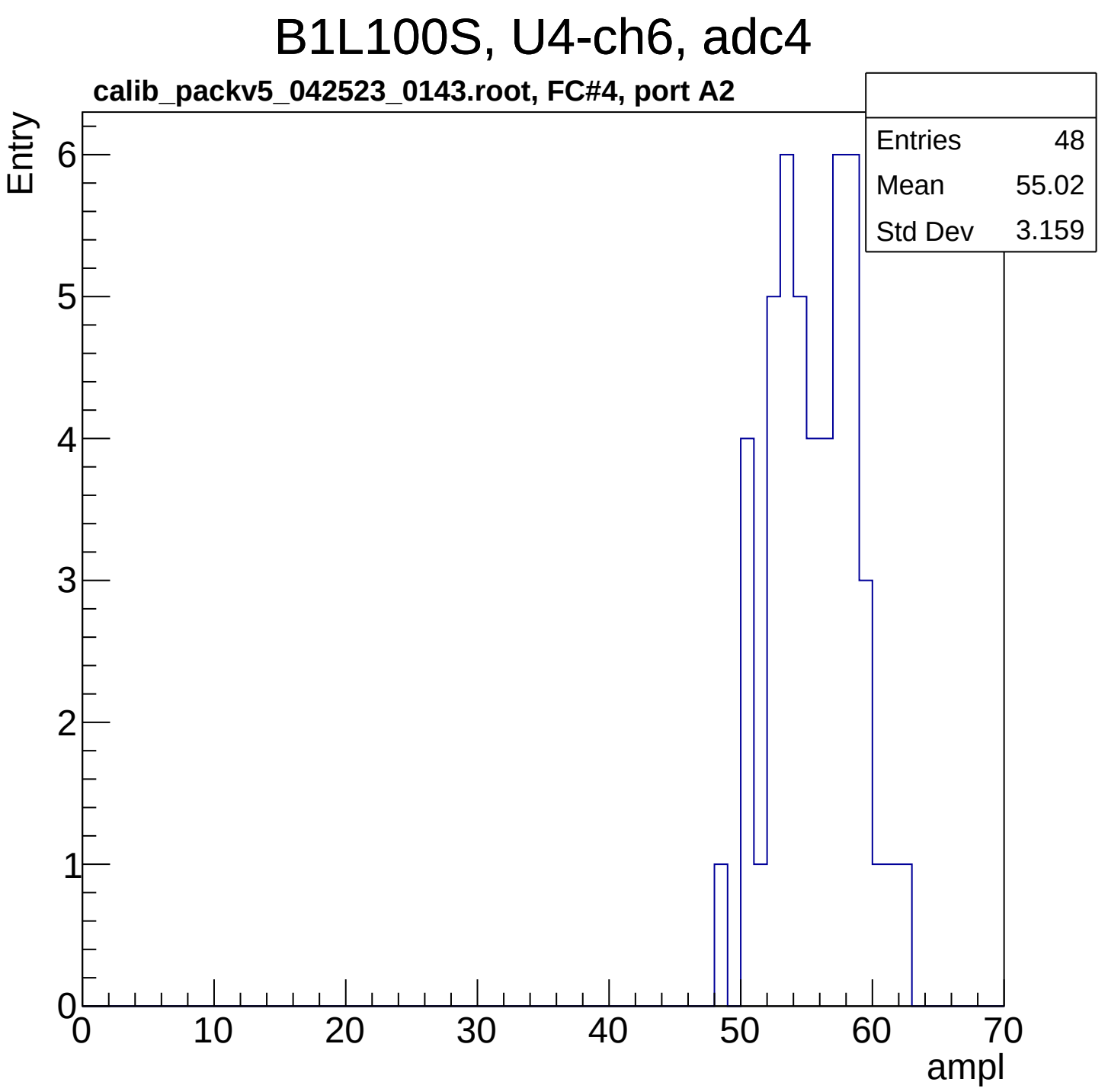

B1L100S, U4-ch5, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 22
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

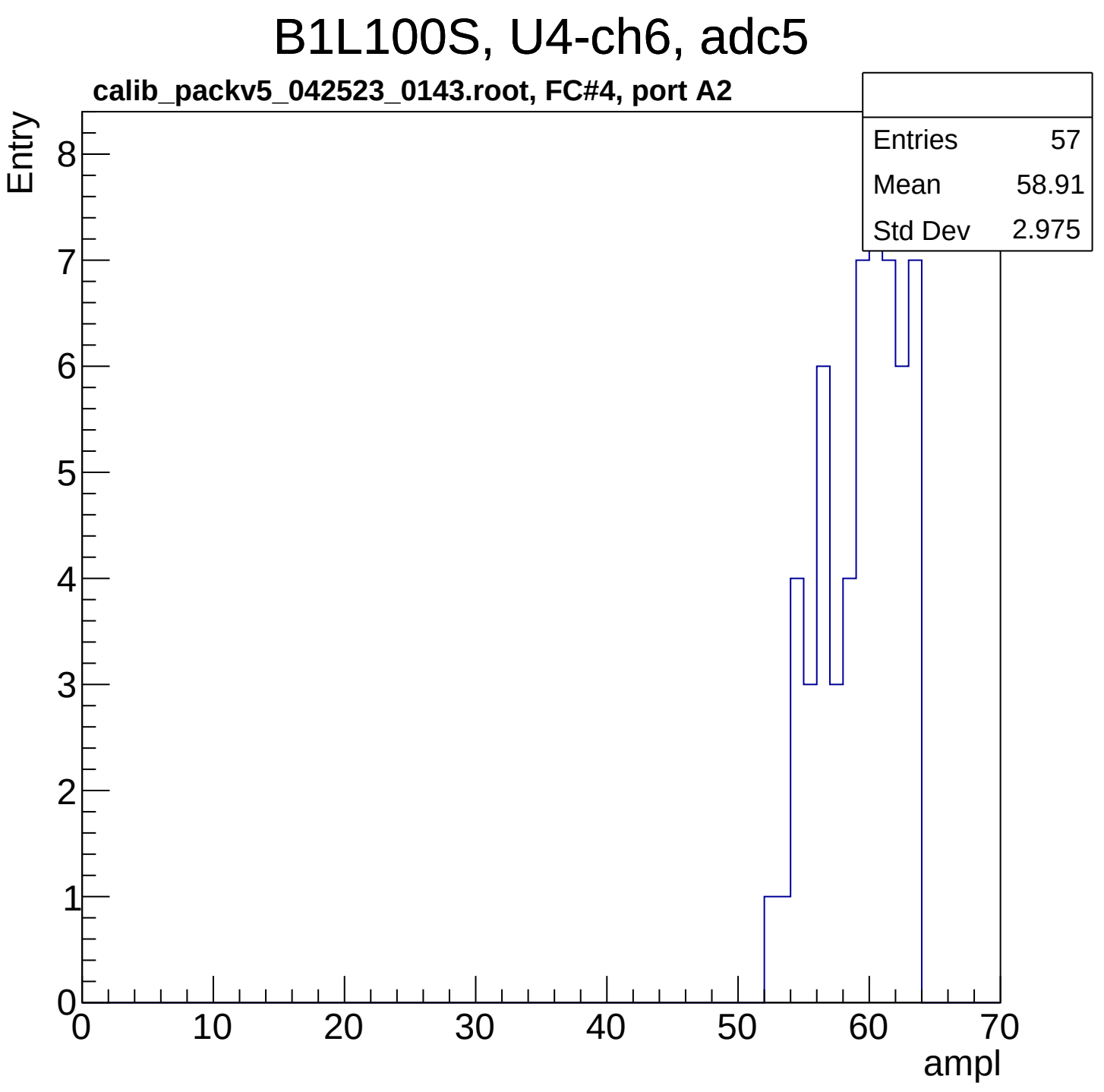

B1L100S, U4-ch6, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 28.81
Std Dev 3.452
Gaus mean : 29.0905
Gaus Width: 3.9450
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

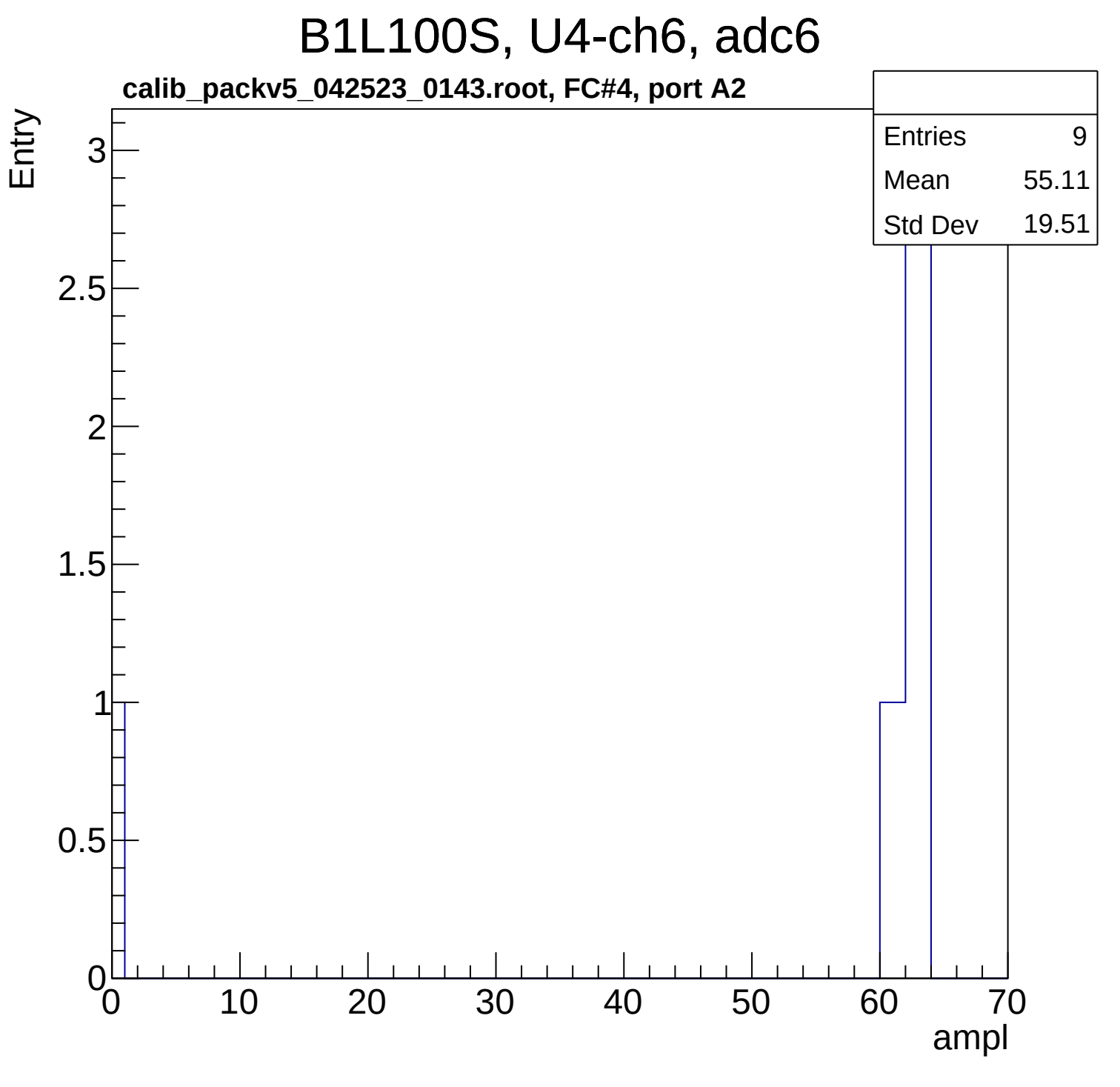

B1L100S, U4-ch6, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 34.91
Std Dev 3.814
Gaus mean : 34.2362
Gaus Width: 4.4832
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

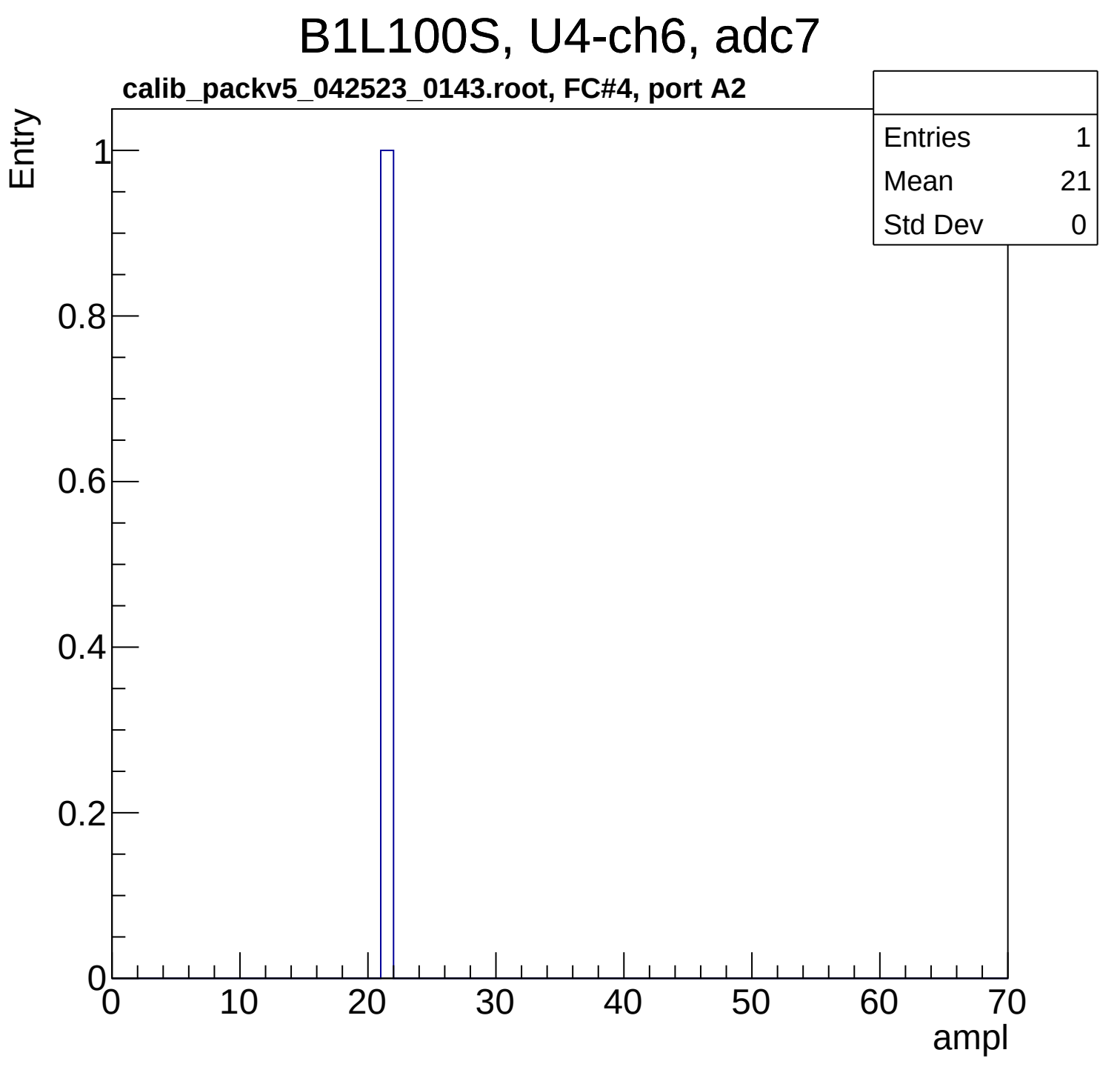

B1L100S, U4-ch6, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 42
Std Dev 3.721
Gaus mean : 42.0794
Gaus Width: 3.1435
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

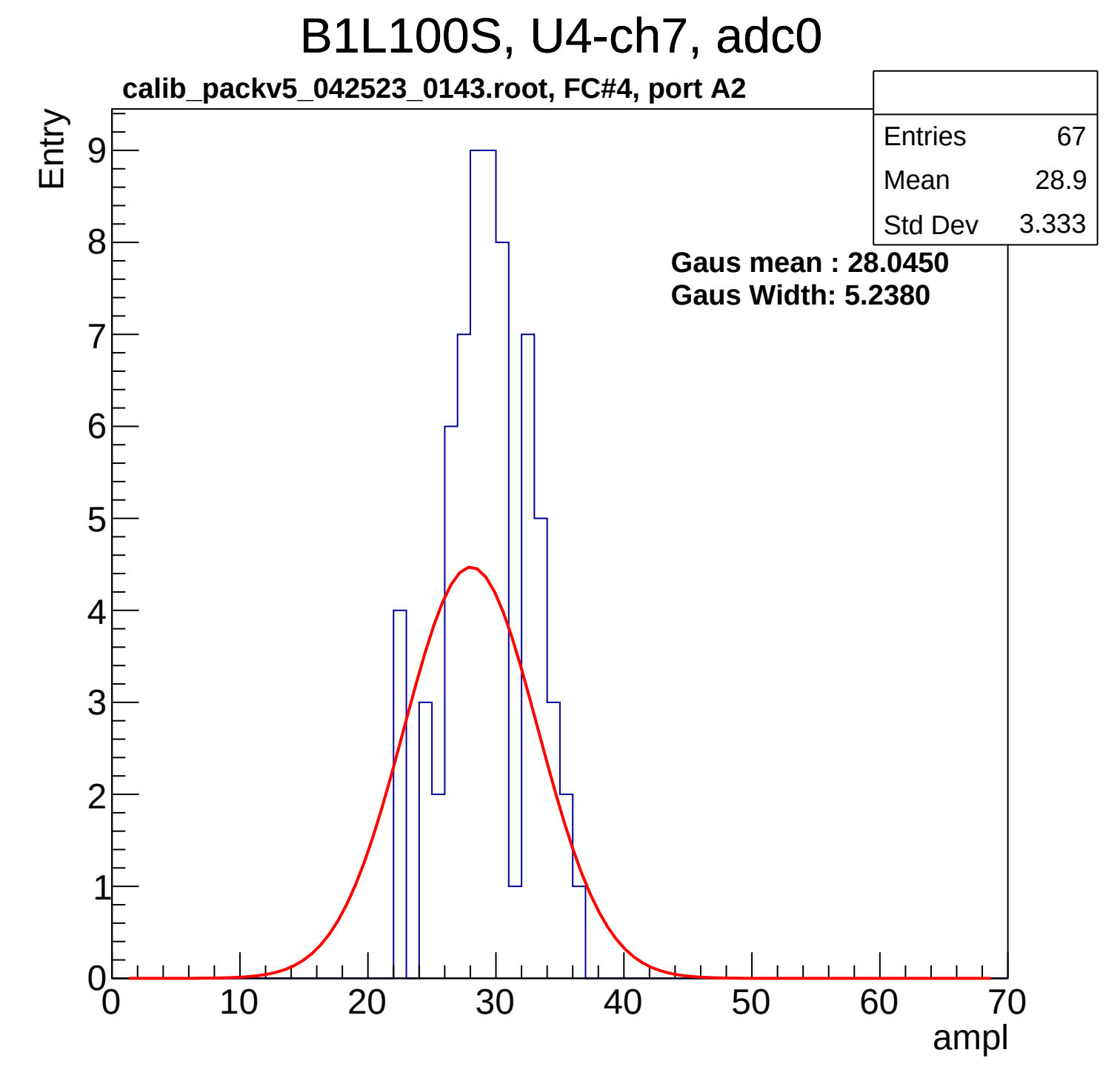

B1L100S, U4-ch6, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 48.57
Std Dev 3.732
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

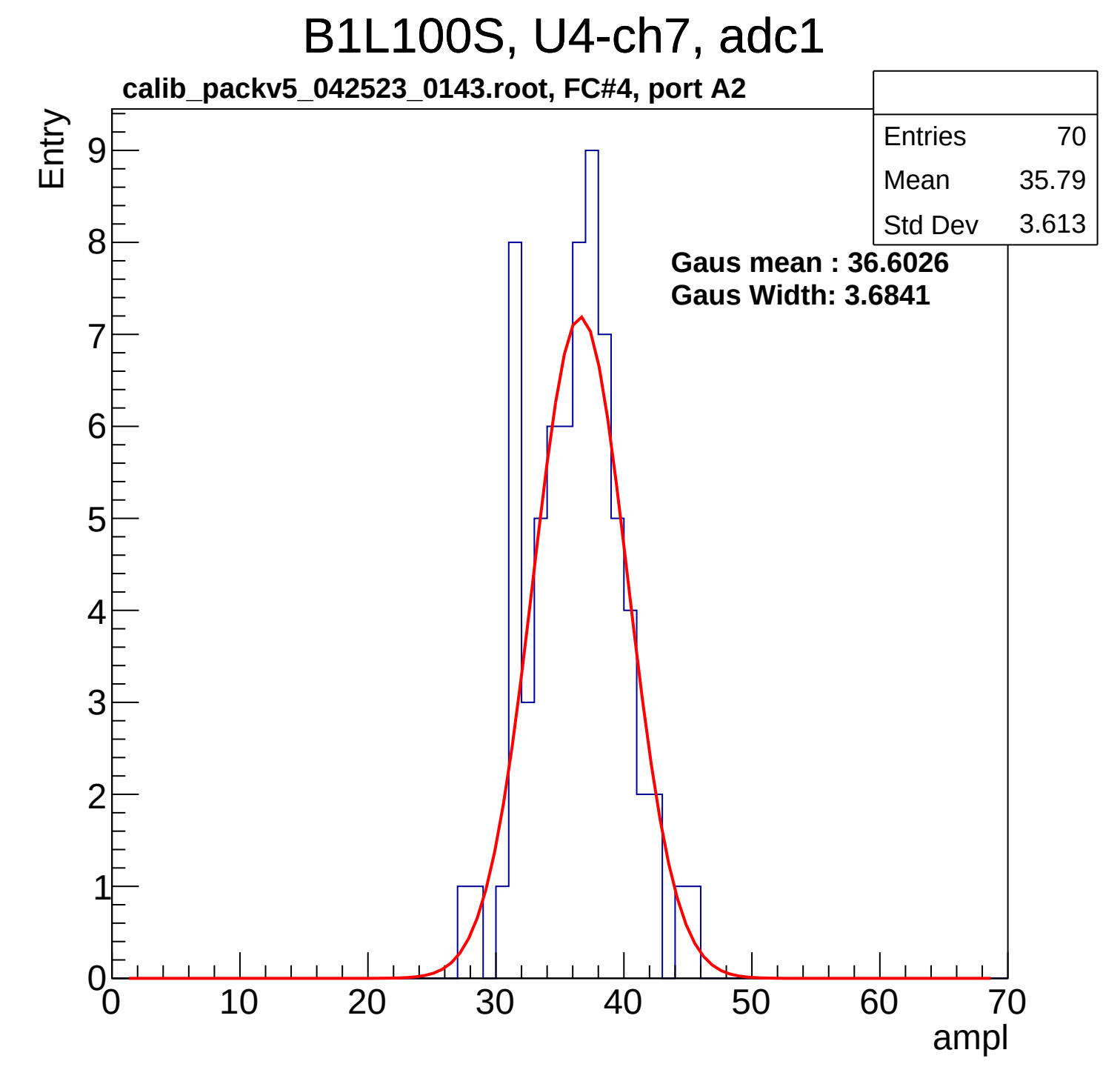

B1L100S, U4-ch6, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 55.02
Std Dev 3.159
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

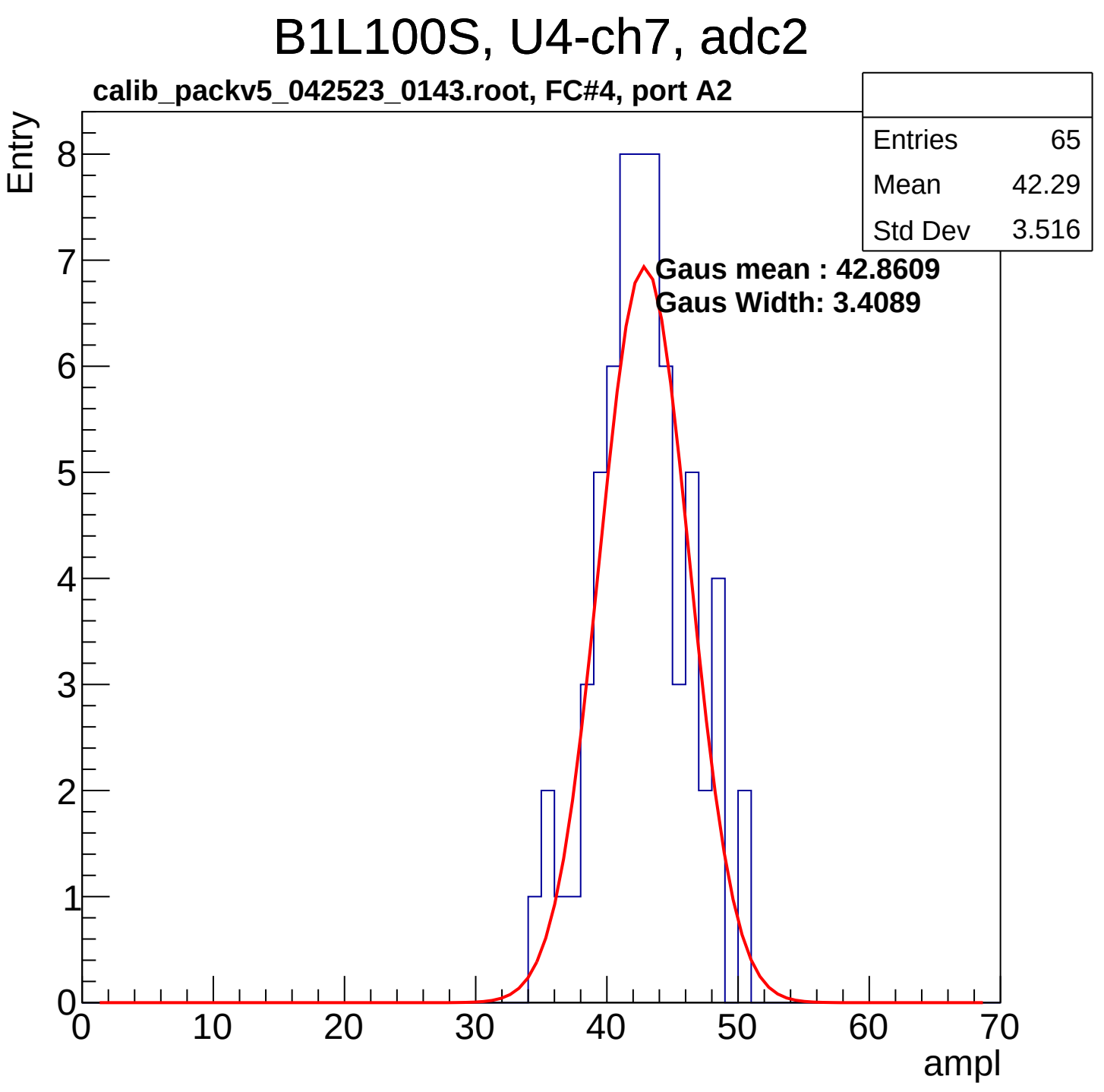

B1L100S, U4-ch6, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 58.91
Std Dev 2.975
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

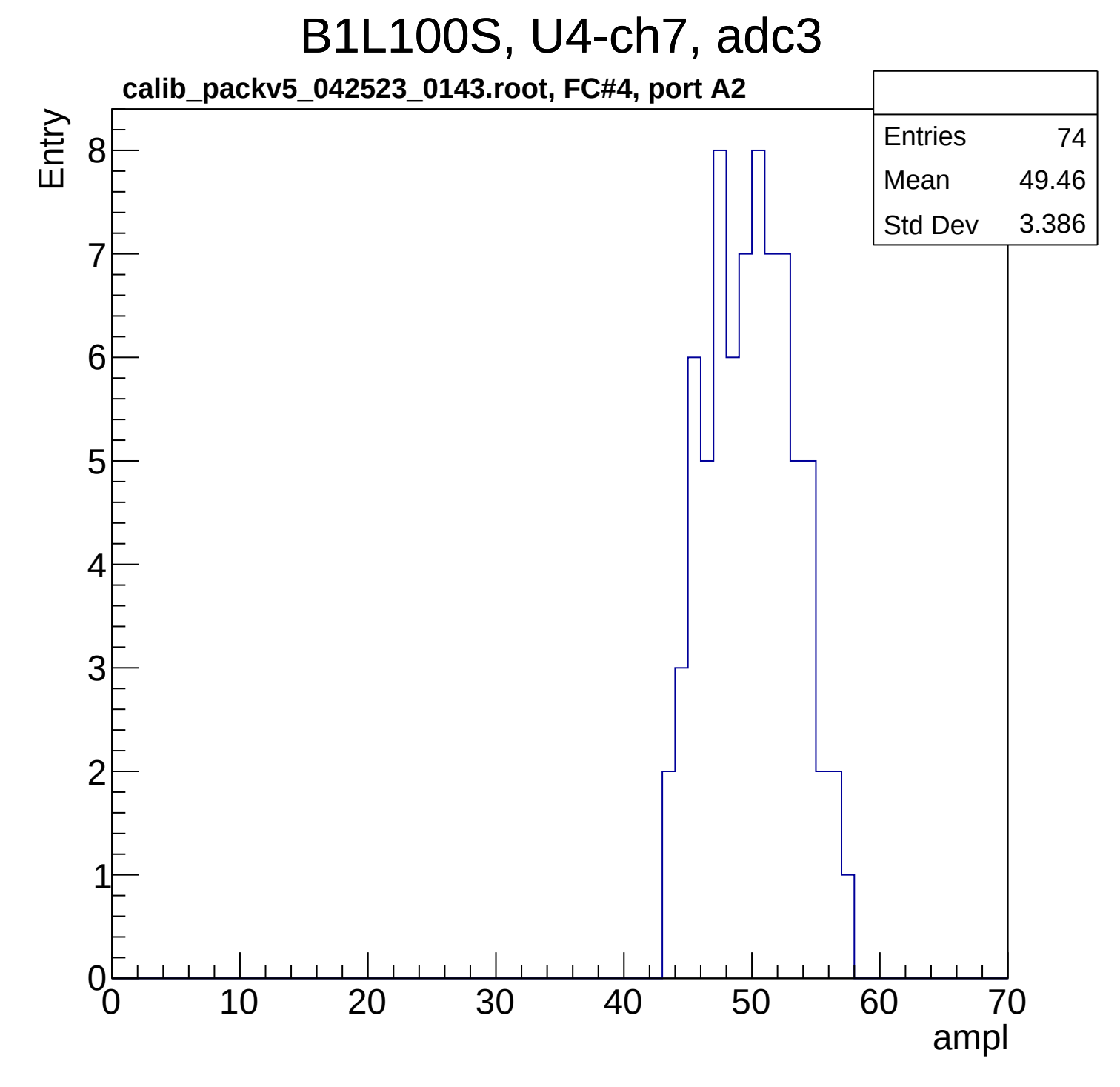

B1L100S, U4-ch6, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 55.11
Std Dev 19.51
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

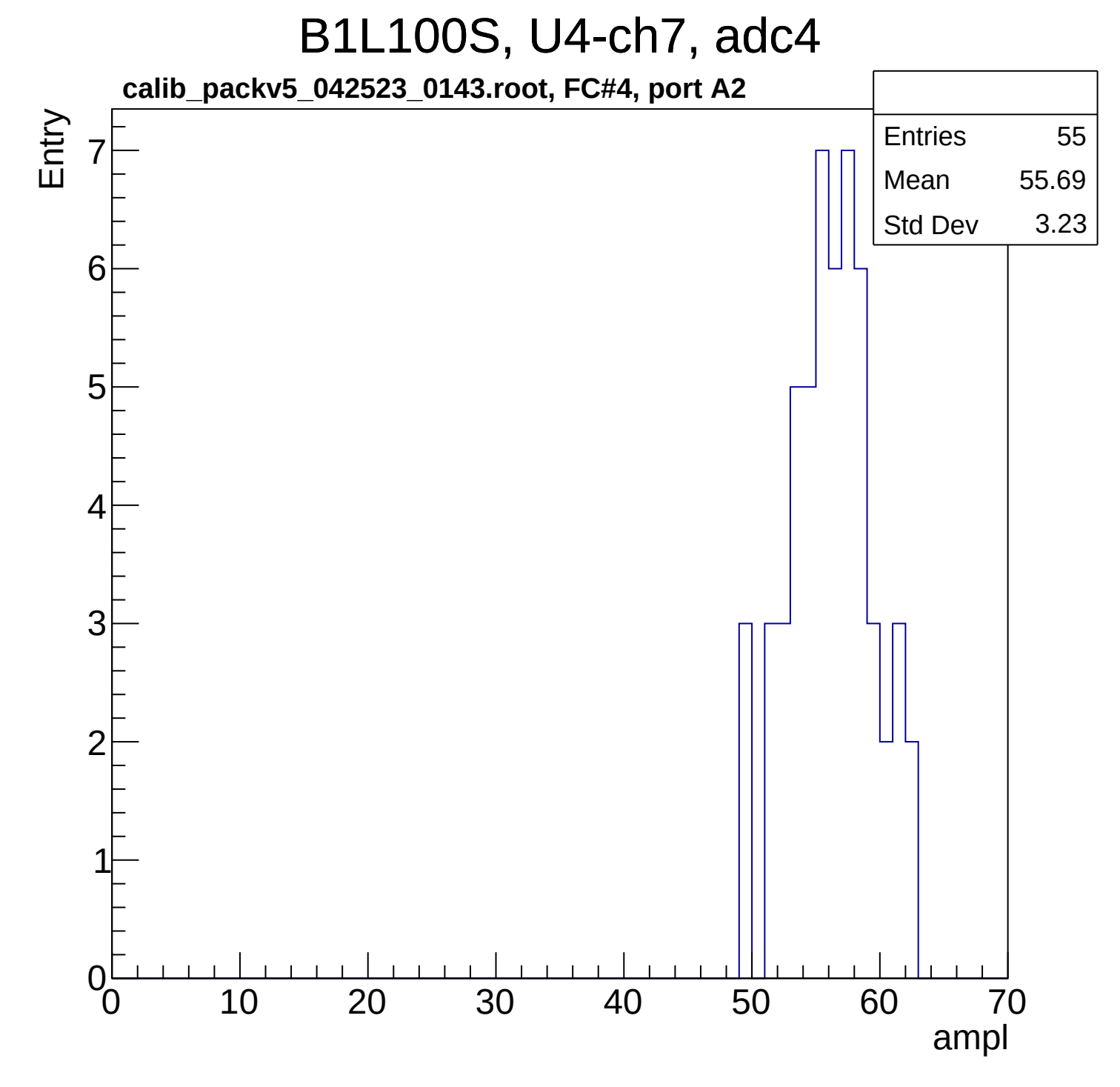

B1L100S, U4-ch6, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 21
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

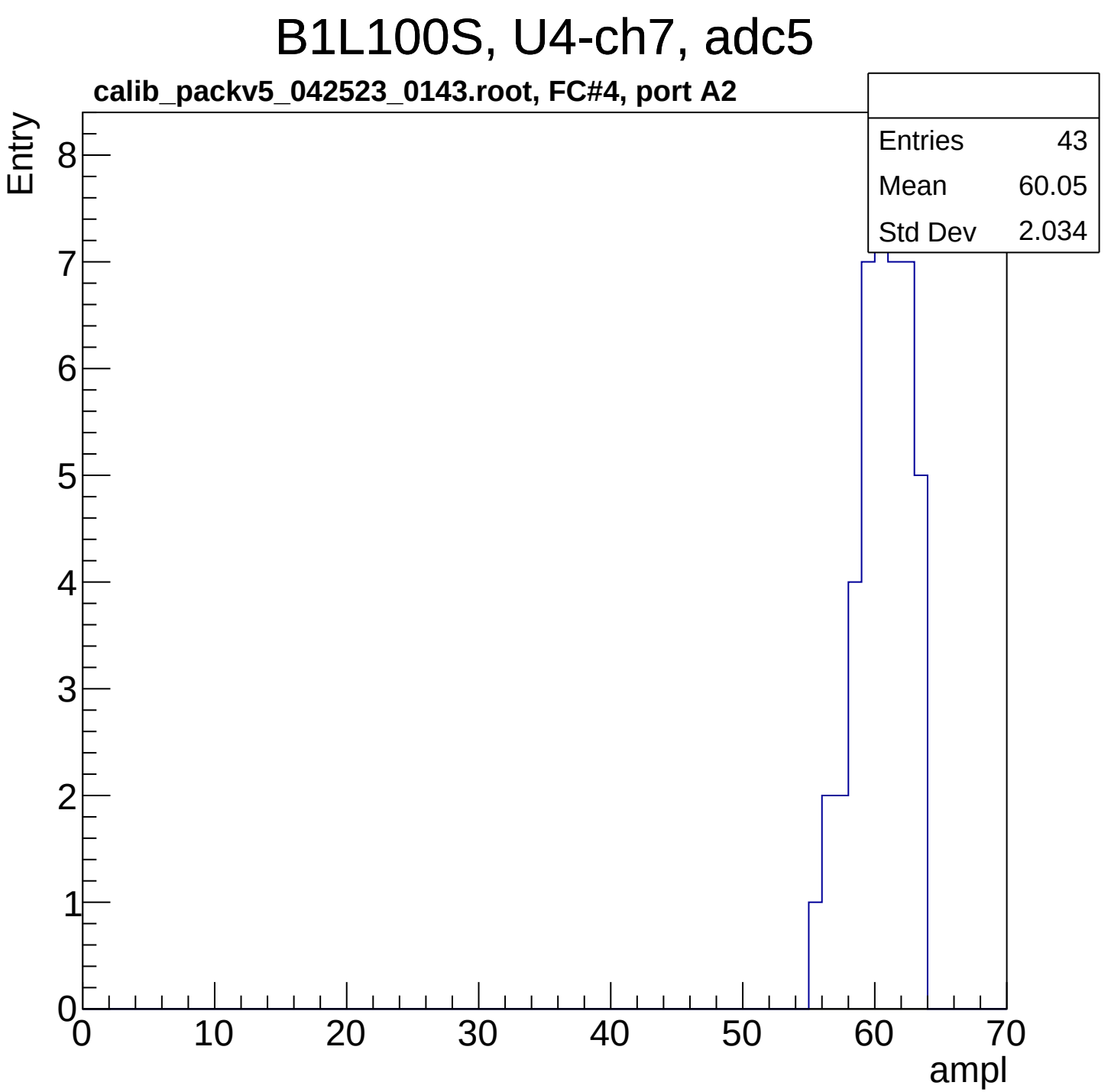

B1L100S, U4-ch7, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 28.9
Std Dev 3.333
Gaus mean : 28.0450
Gaus Width: 5.2380
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

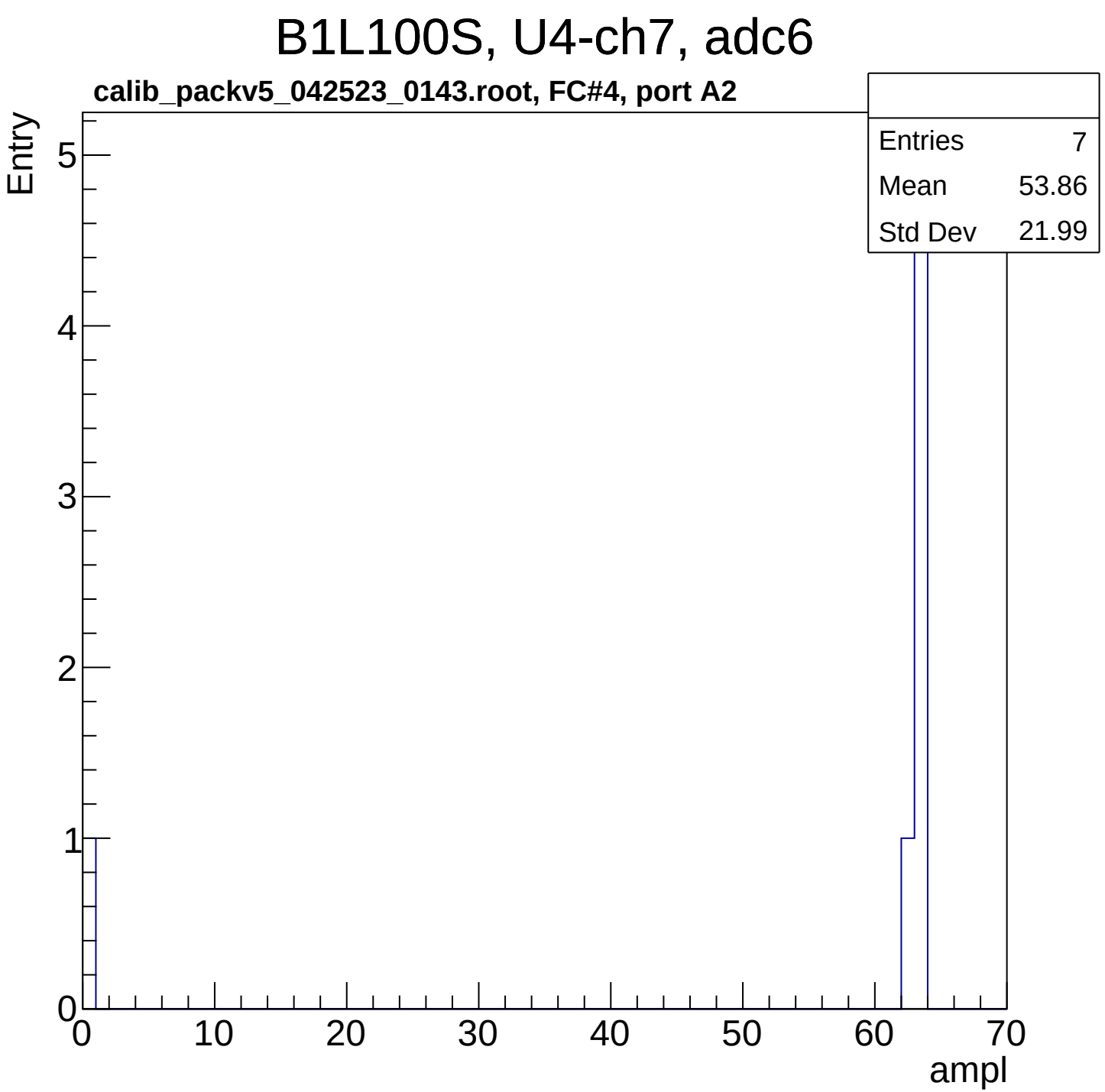

B1L100S, U4-ch7, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 35.79
Std Dev 3.613
Gaus mean : 36.6026
Gaus Width: 3.6841
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

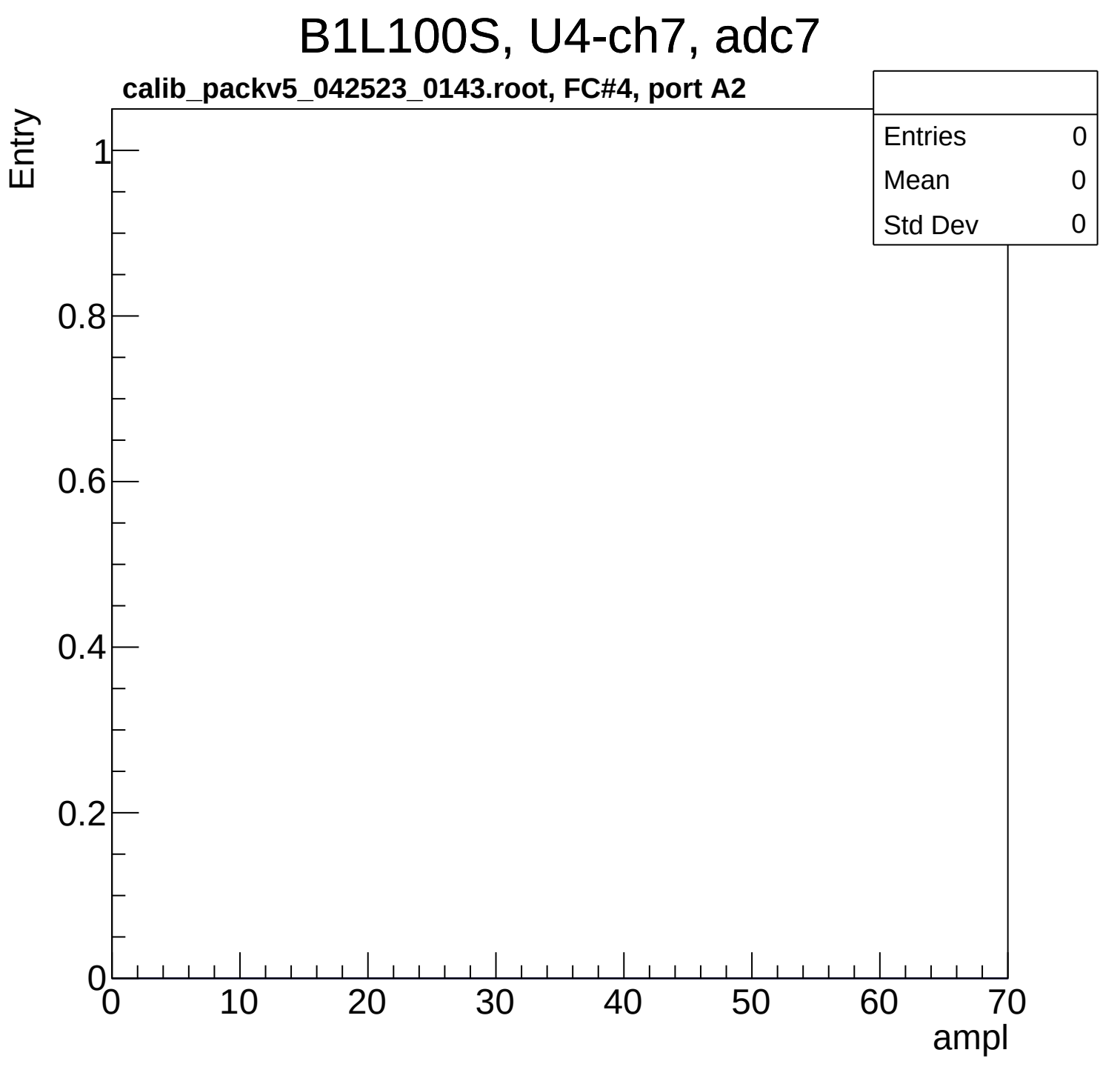

B1L100S, U4-ch7, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 42.29
Std Dev 3.516
Gaus mean : 42.8609
Gaus Width: 3.4089
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

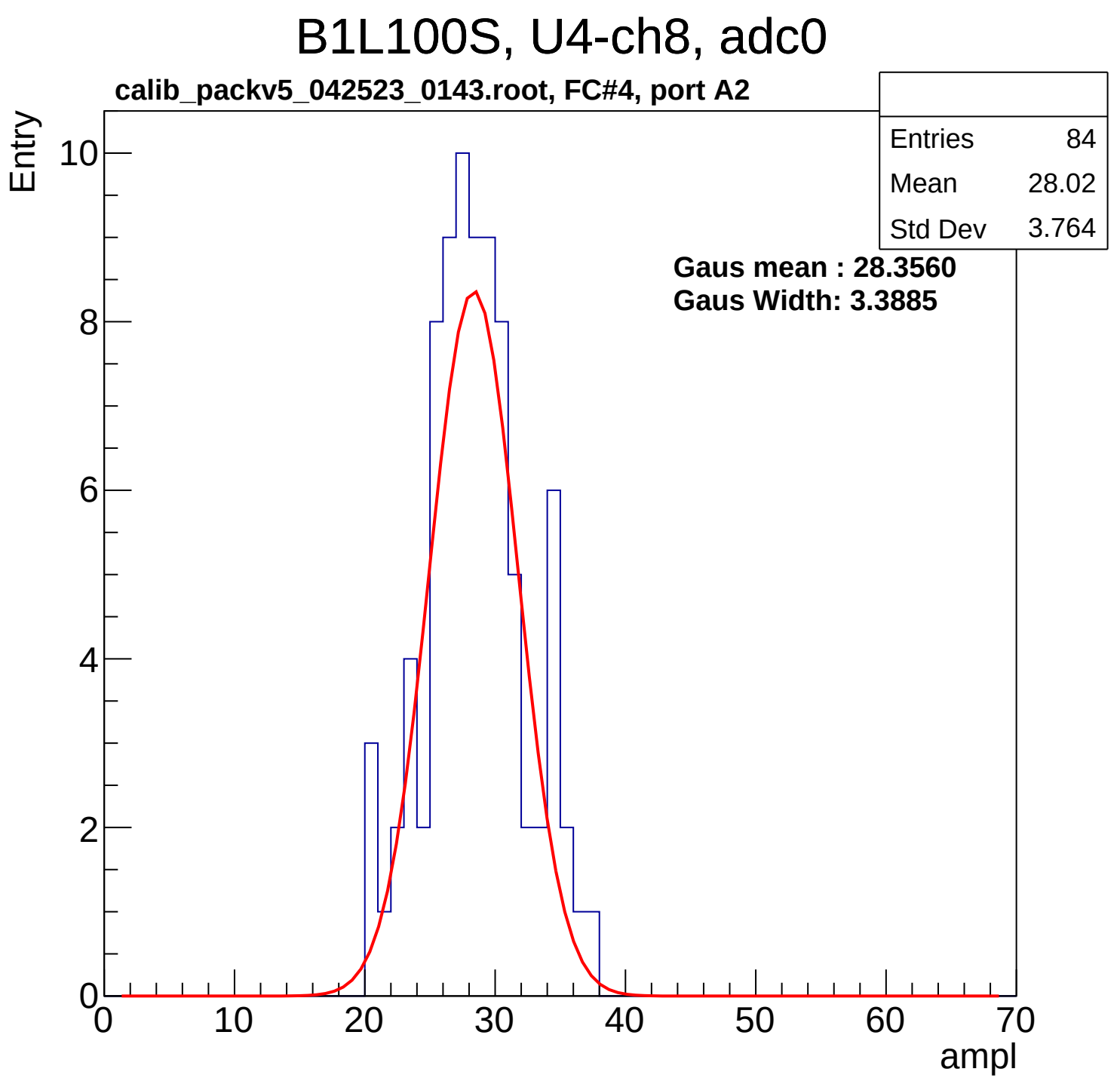

B1L100S, U4-ch7, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 49.46
Std Dev 3.386
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

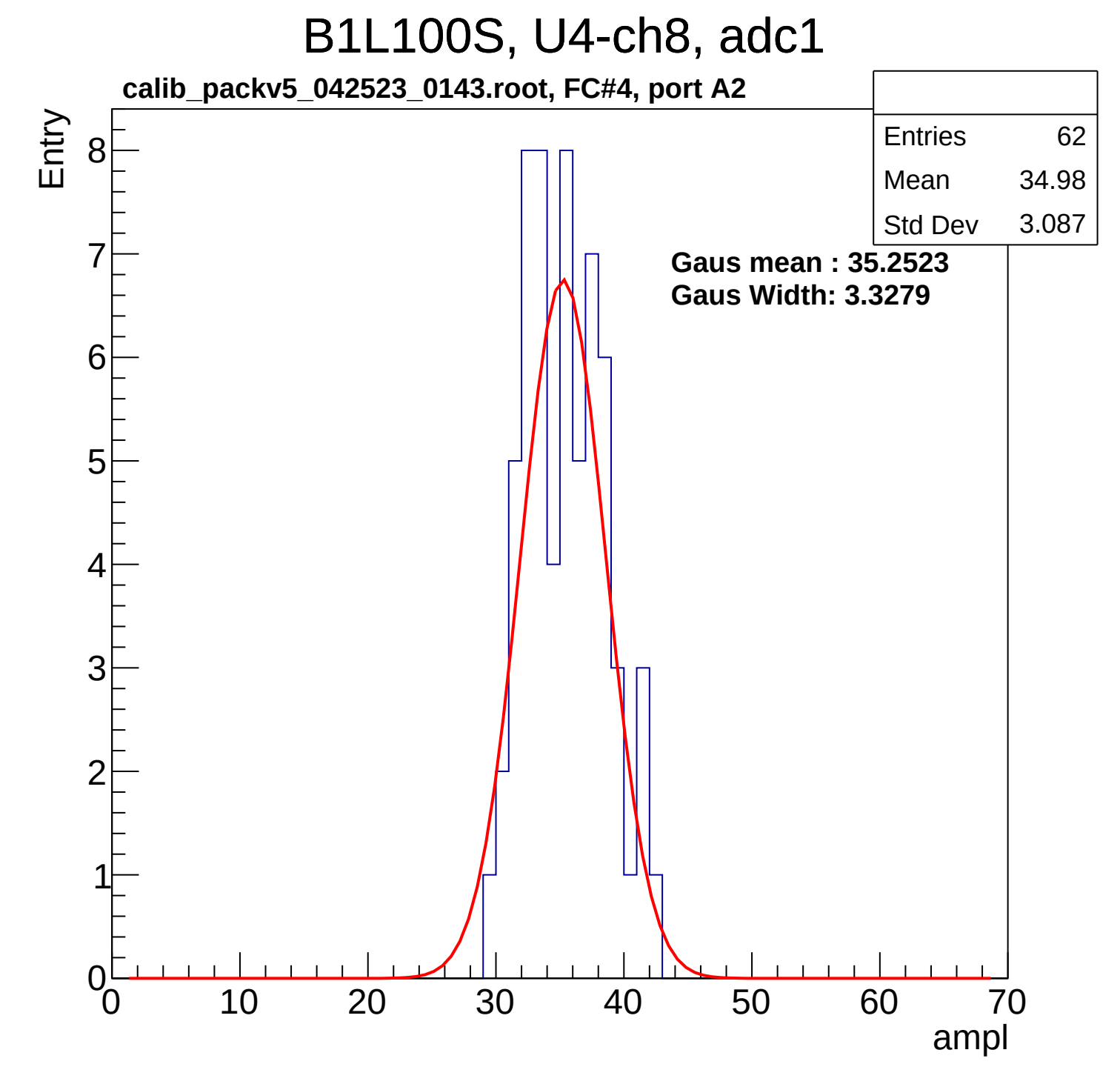

B1L100S, U4-ch7, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 55.69
Std Dev 3.23
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

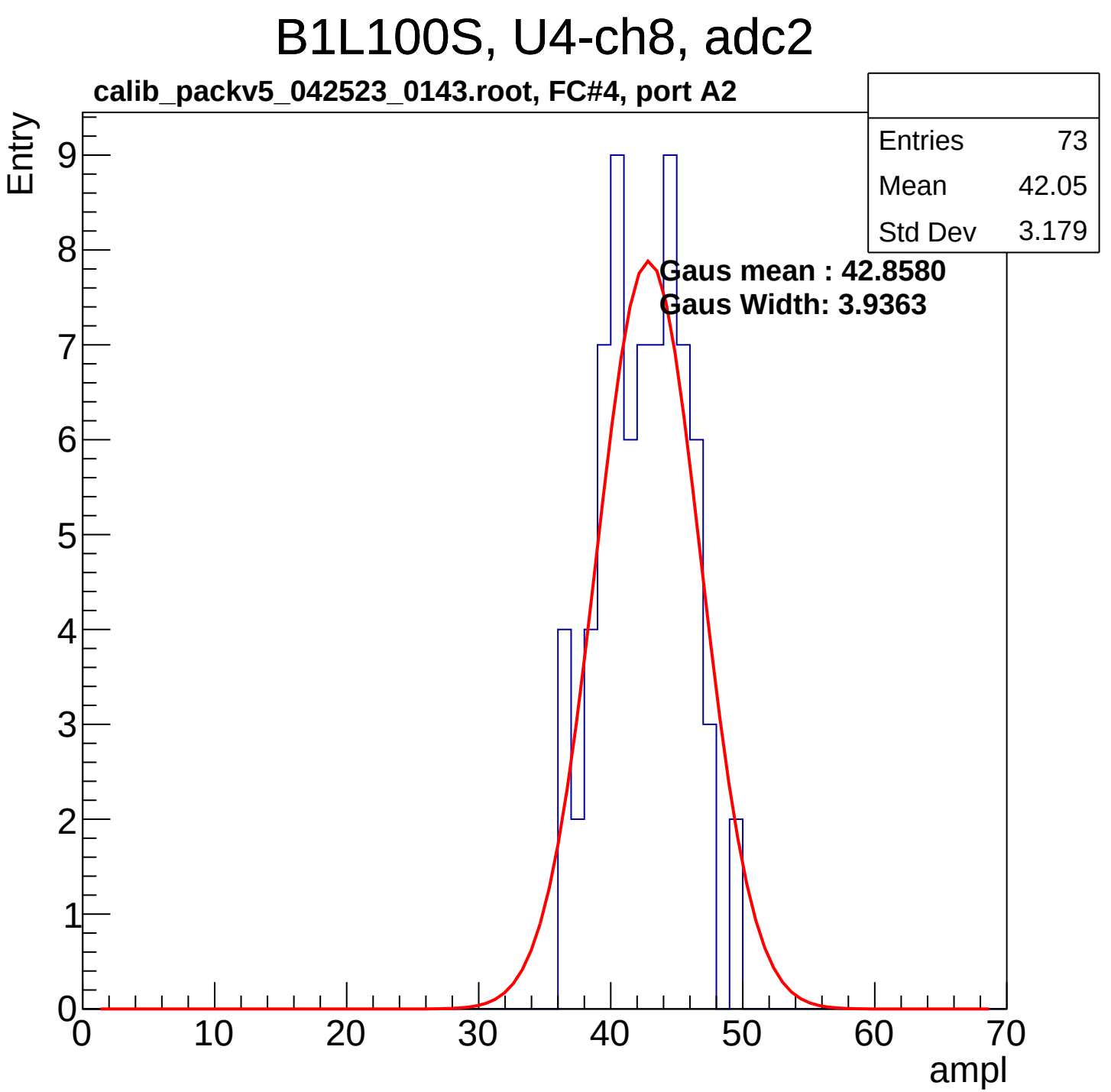

B1L100S, U4-ch7, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 60.05
Std Dev 2.034
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

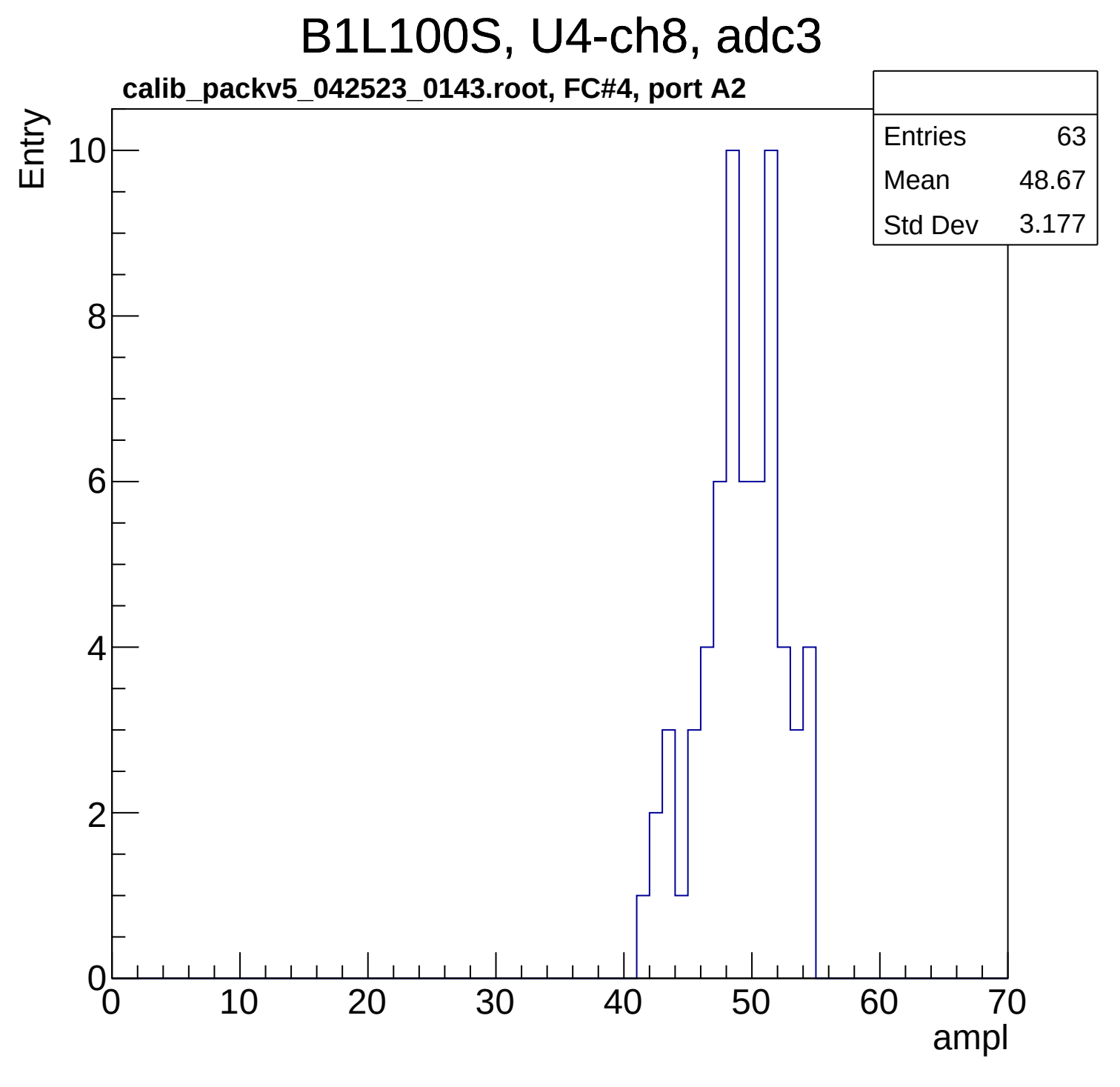

B1L100S, U4-ch7, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 53.86
Std Dev 21.99
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

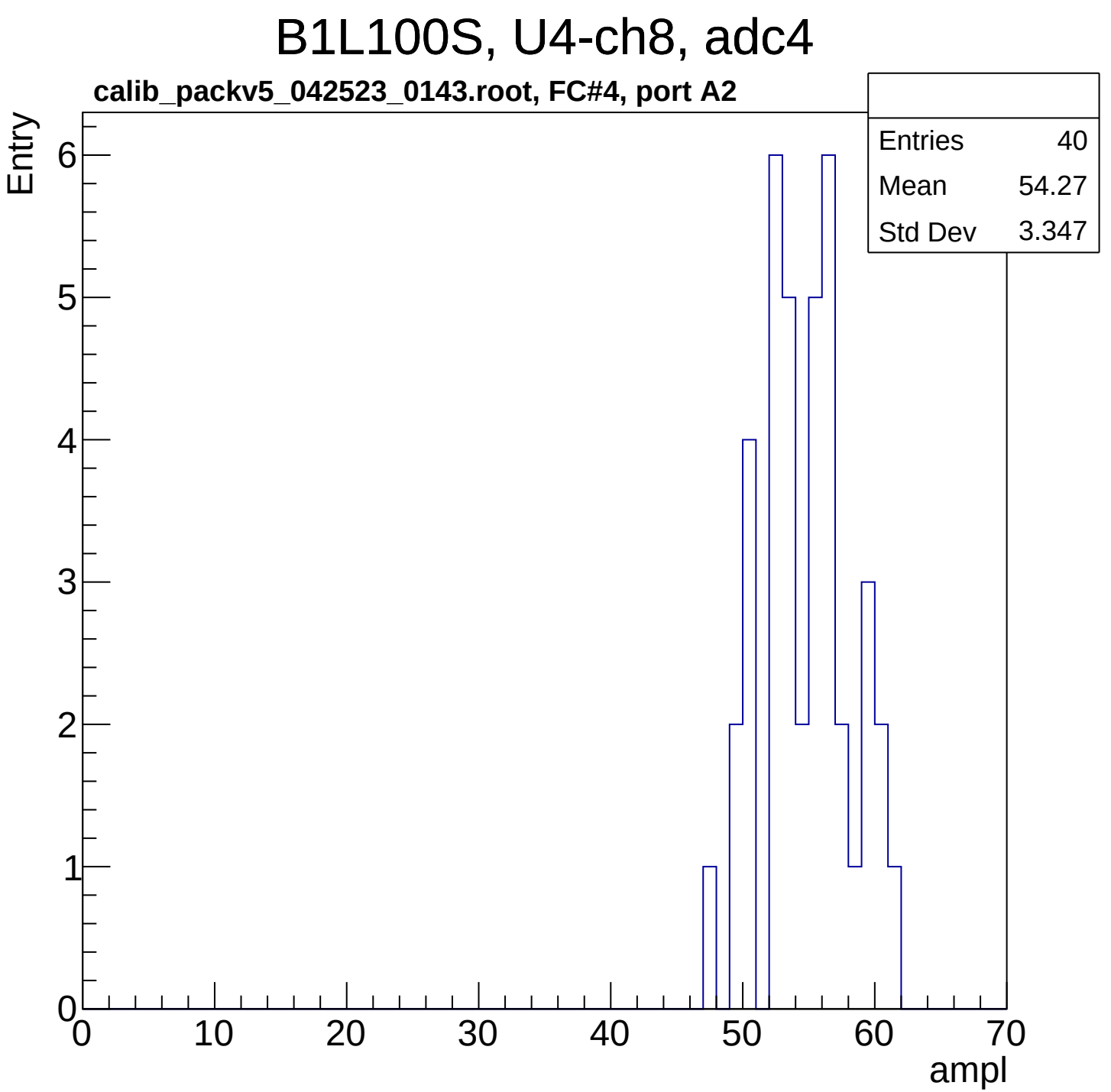

B1L100S, U4-ch7, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

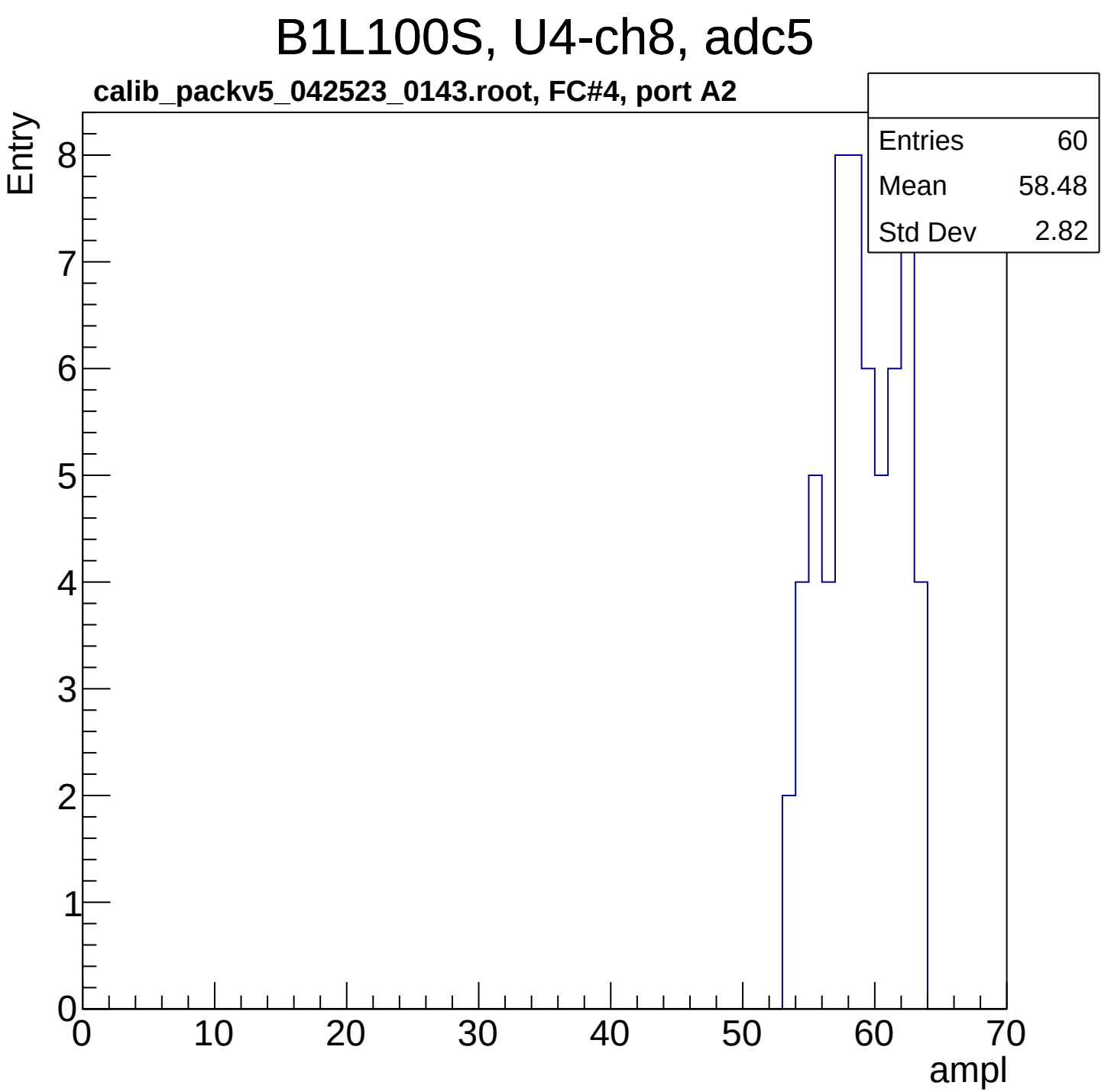

B1L100S, U4-ch8, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 84
Mean 28.02
Std Dev 3.764
Gaus mean : 28.3560
Gaus Width: 3.3885
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

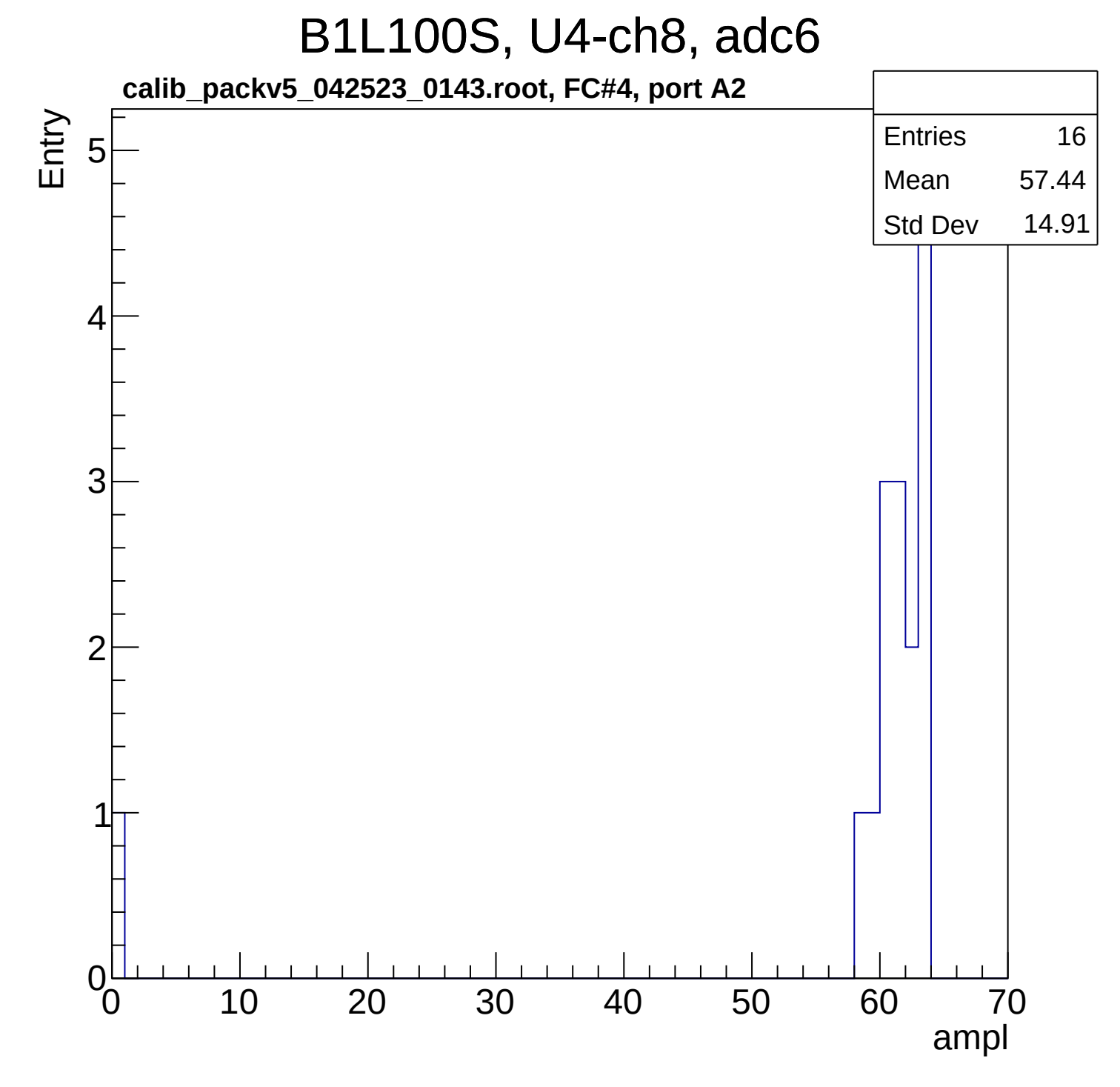

B1L100S, U4-ch8, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 34.98
Std Dev 3.087
Gaus mean : 35.2523
Gaus Width: 3.3279
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

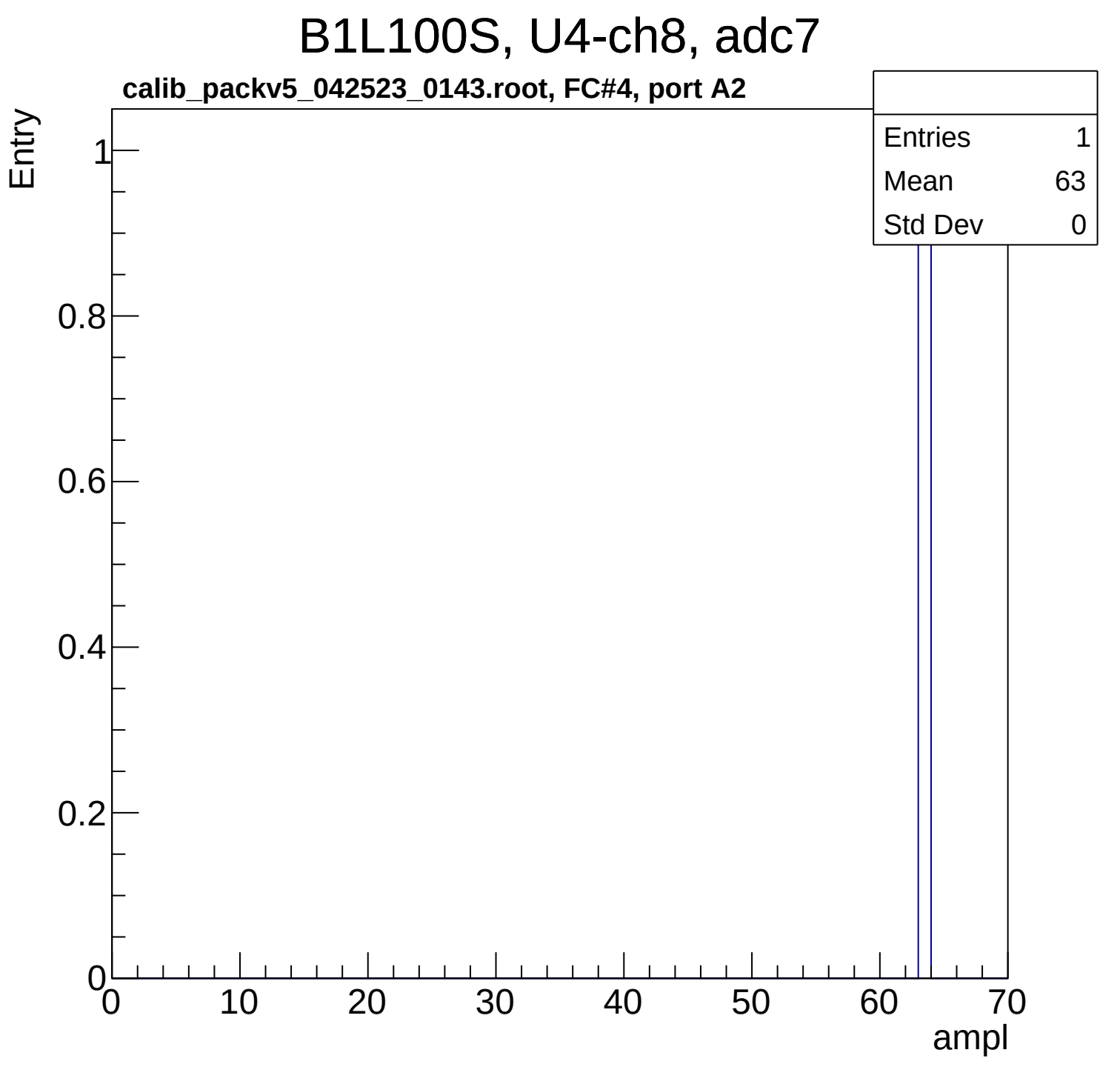

B1L100S, U4-ch8, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 42.05
Std Dev 3.179
Gaus mean : 42.8580
Gaus Width: 3.9363
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

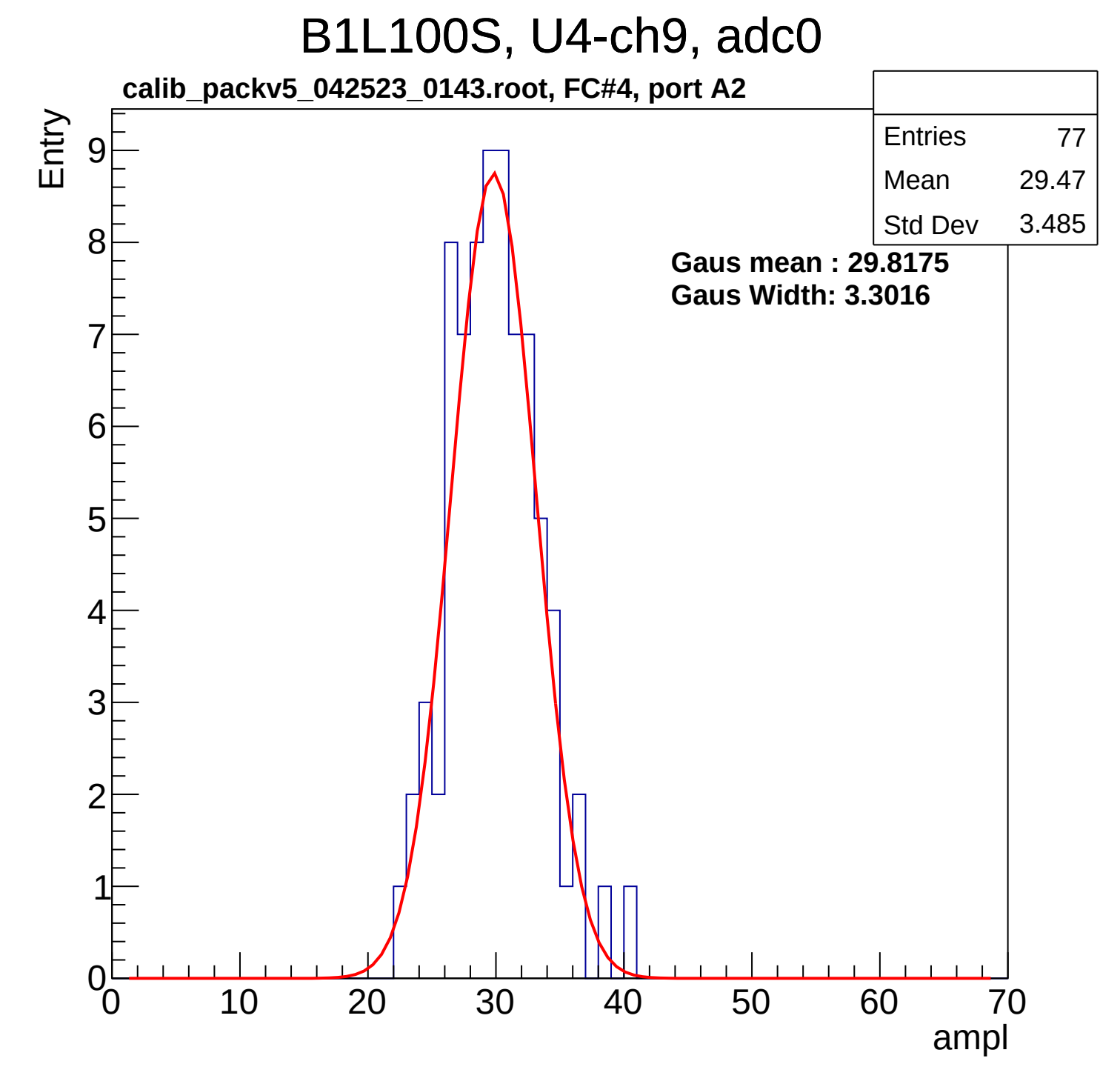

B1L100S, U4-ch8, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 48.67
Std Dev 3.177
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

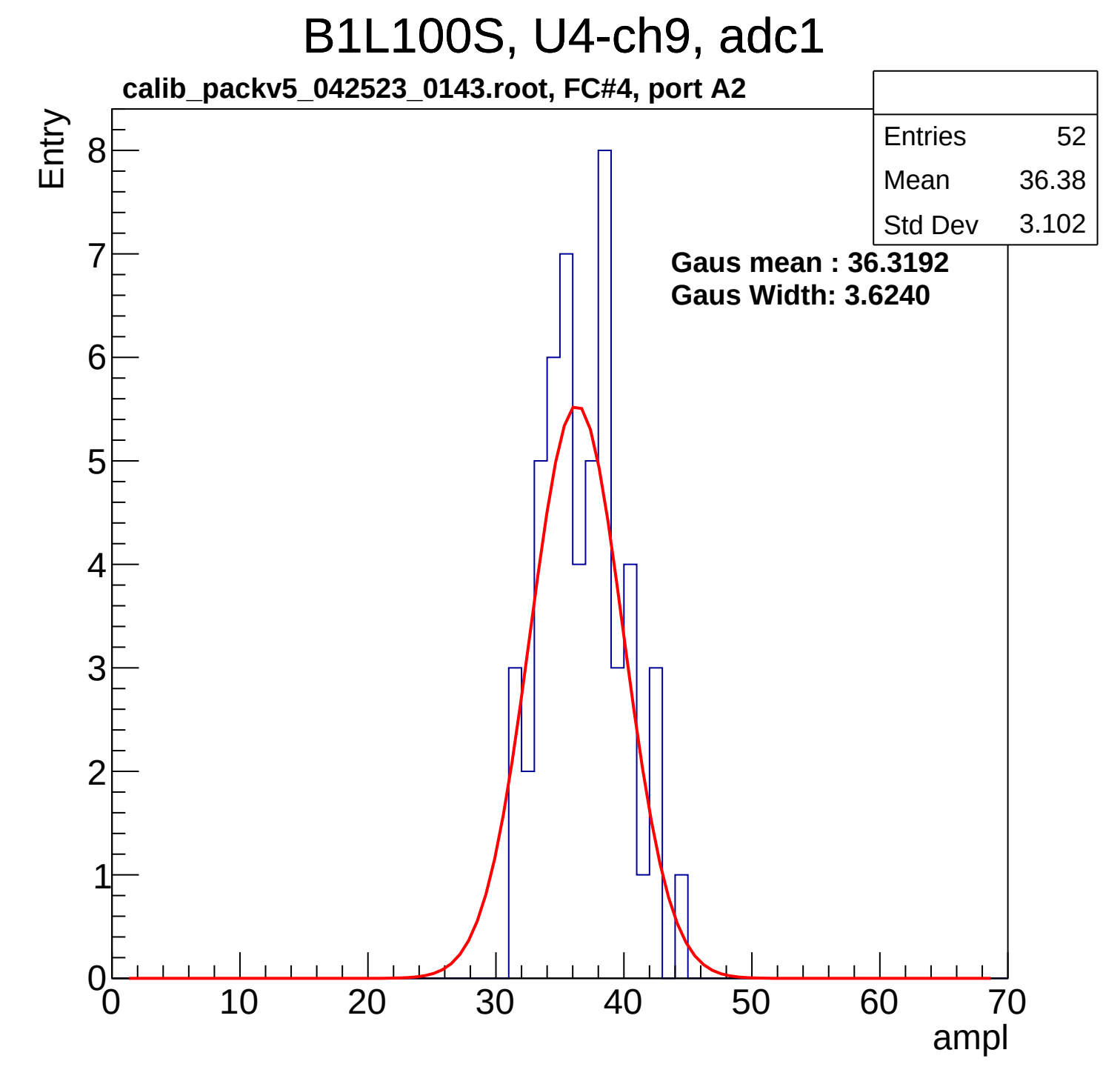

B1L100S, U4-ch8, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 40
Mean 54.27
Std Dev 3.347
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

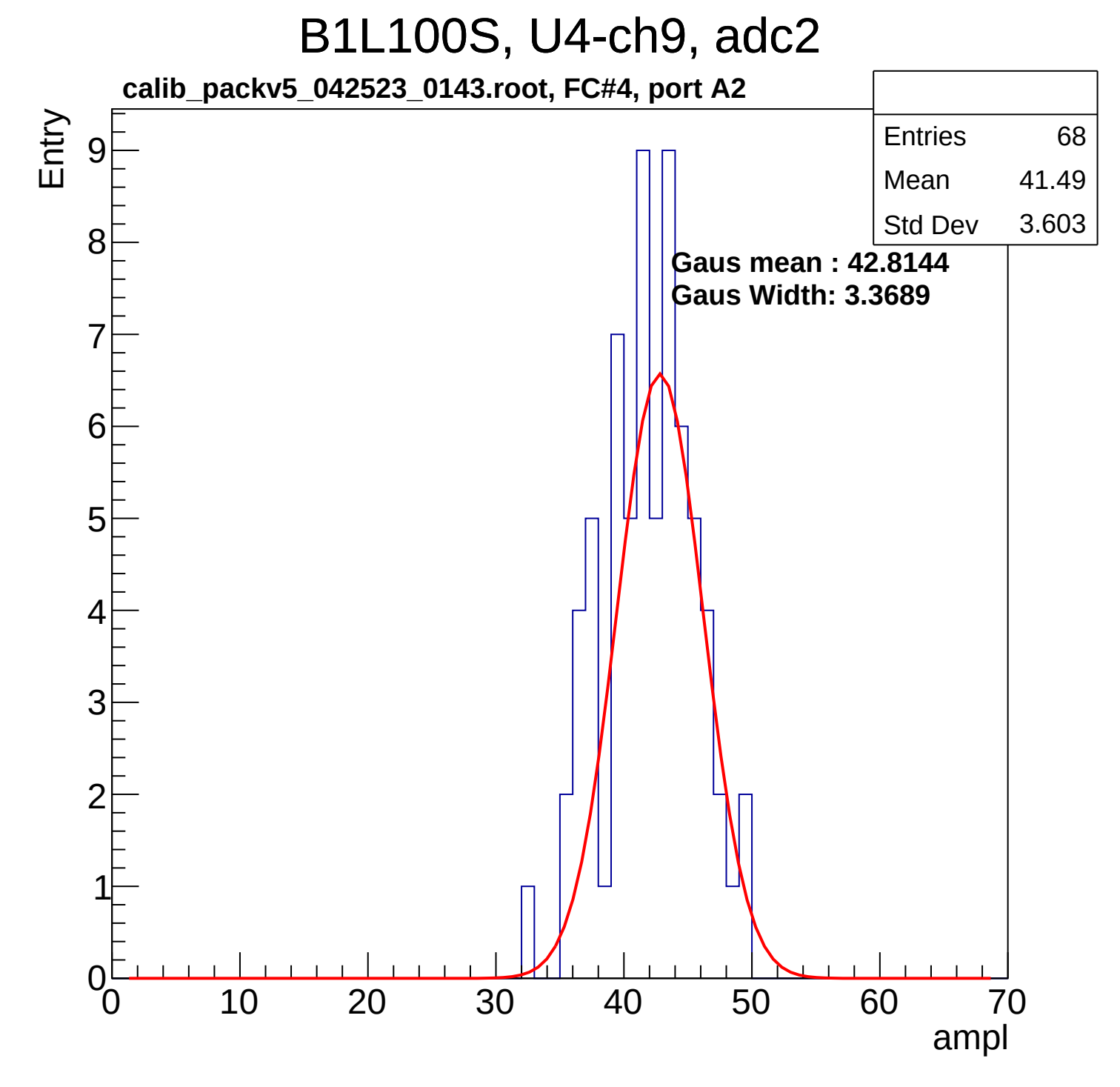

B1L100S, U4-ch8, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 58.48
Std Dev 2.82
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

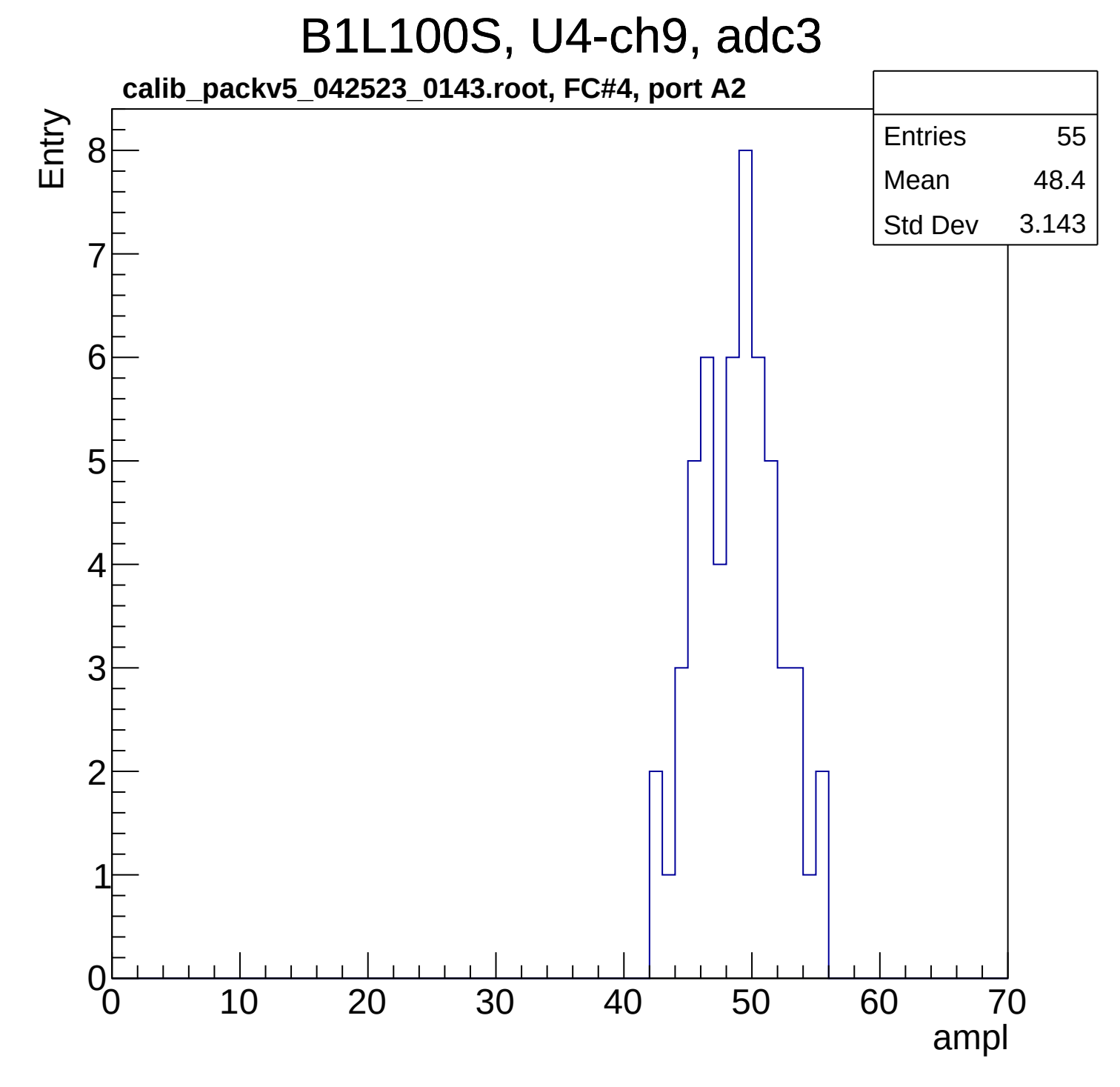

B1L100S, U4-ch8, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 16
Mean 57.44
Std Dev 14.91
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

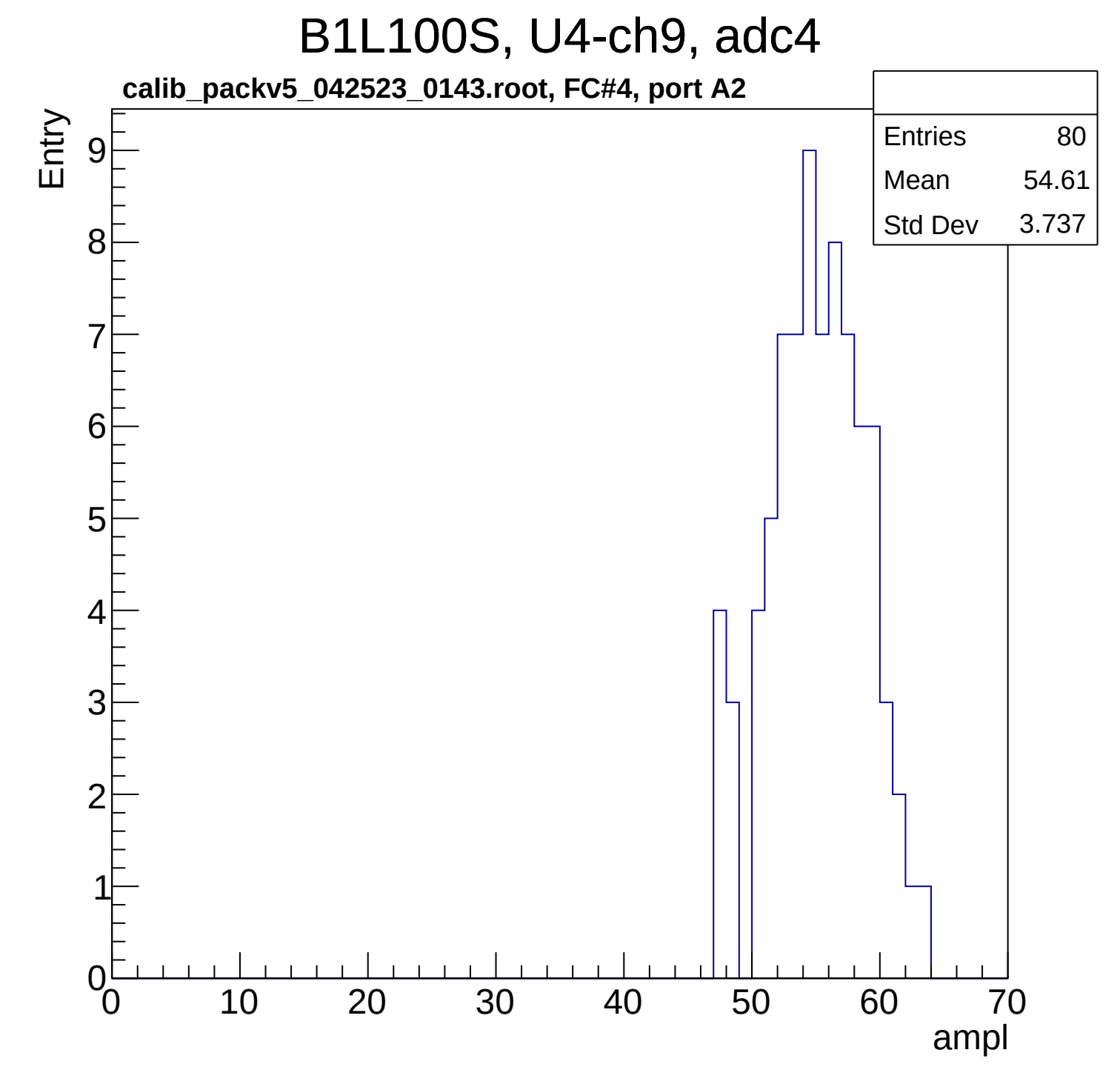

B1L100S, U4-ch8, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

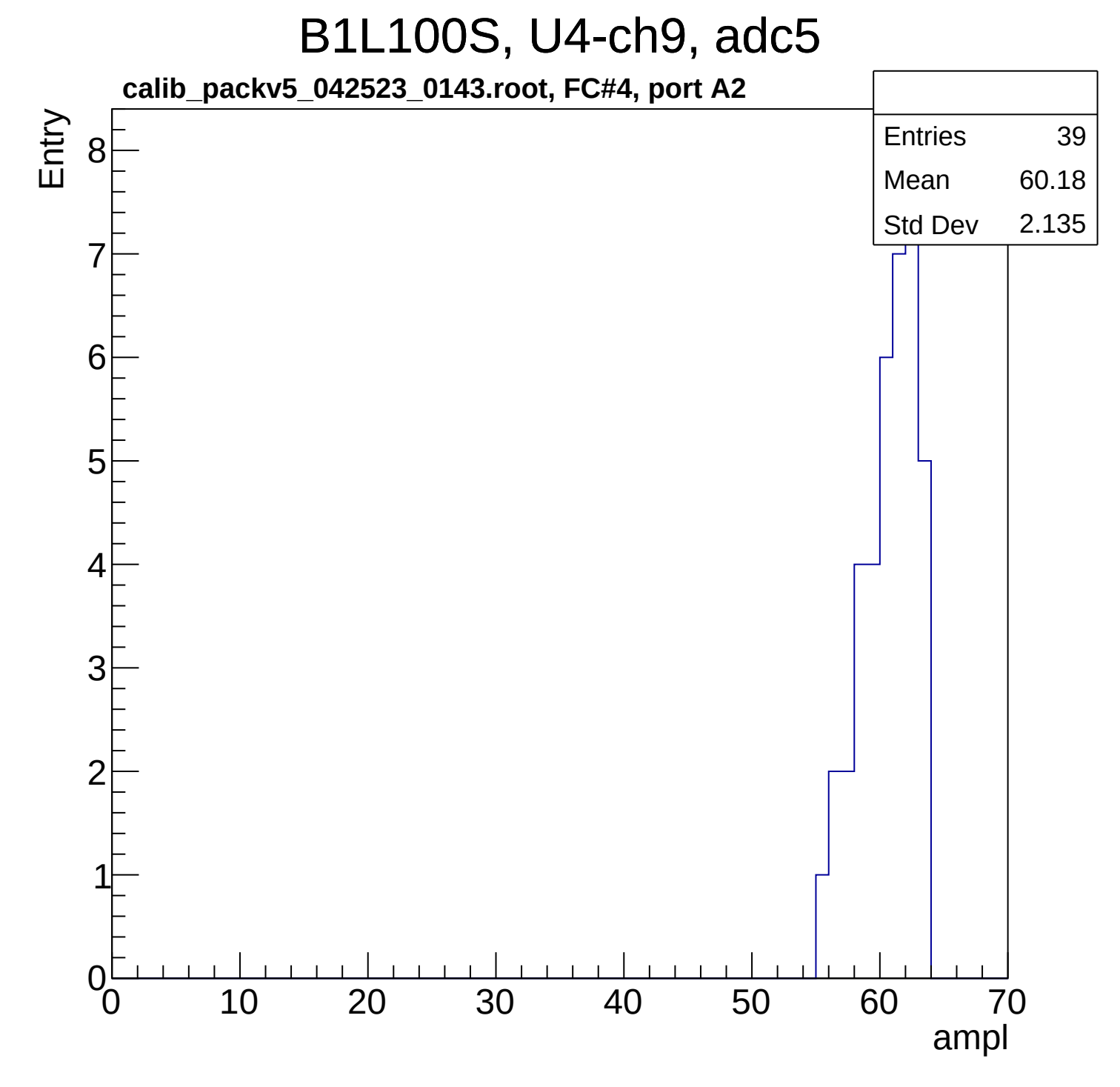

B1L100S, U4-ch9, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 29.47
Std Dev 3.485
Gaus mean : 29.8175
Gaus Width: 3.3016
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

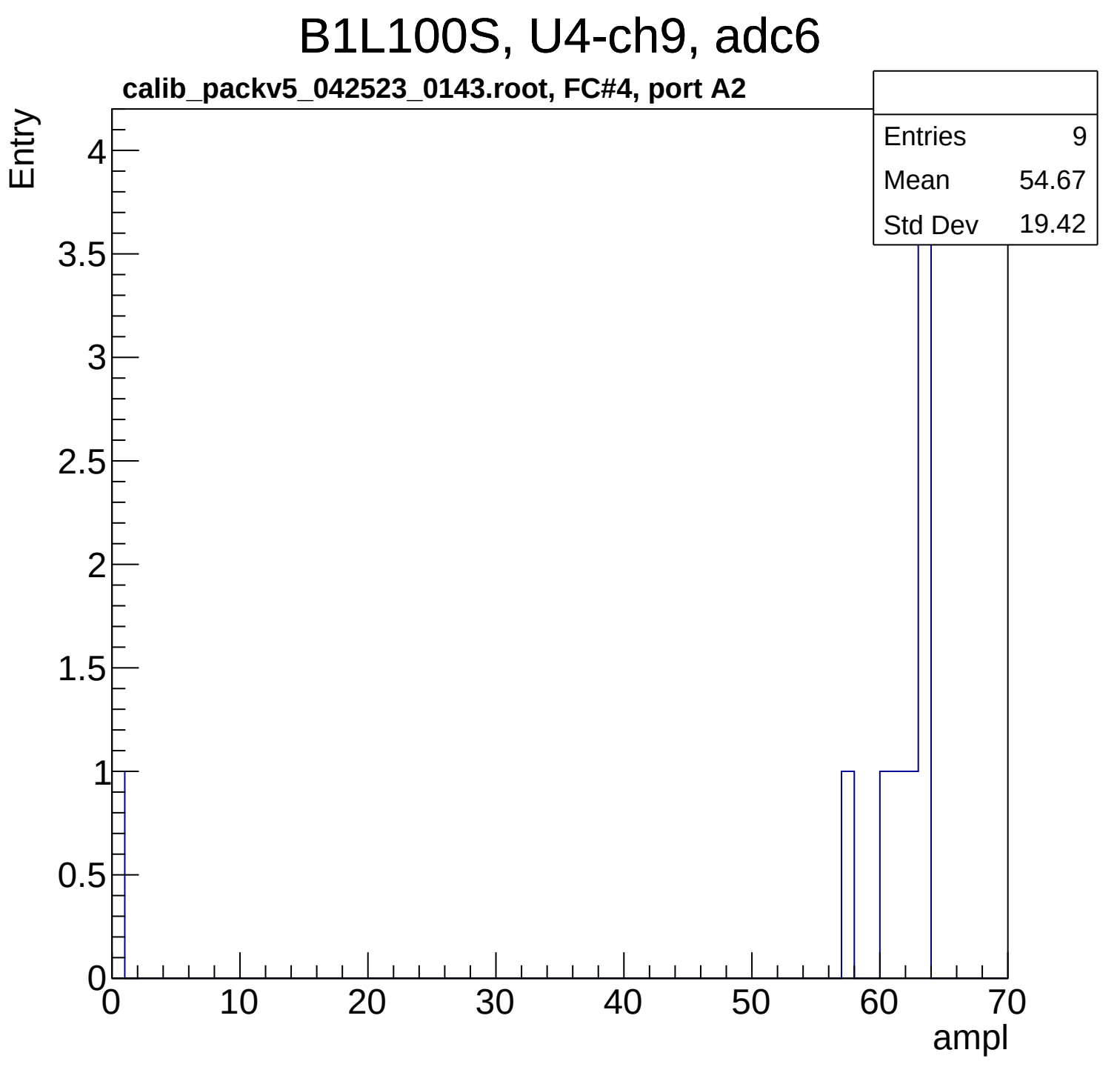

B1L100S, U4-ch9, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 36.38
Std Dev 3.102
Gaus mean : 36.3192
Gaus Width: 3.6240
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

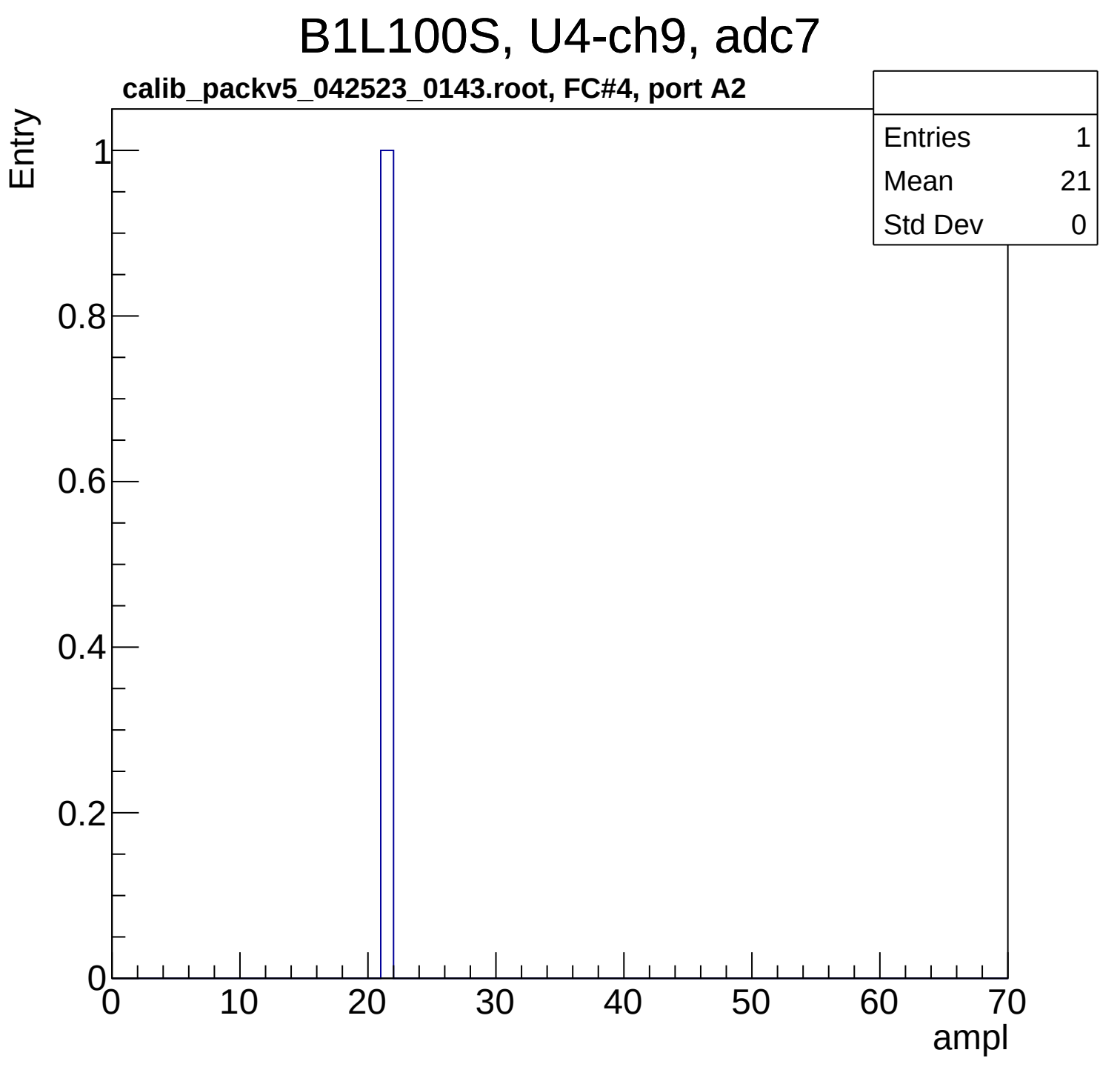

B1L100S, U4-ch9, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 41.49
Std Dev 3.603
Gaus mean : 42.8144
Gaus Width: 3.3689
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

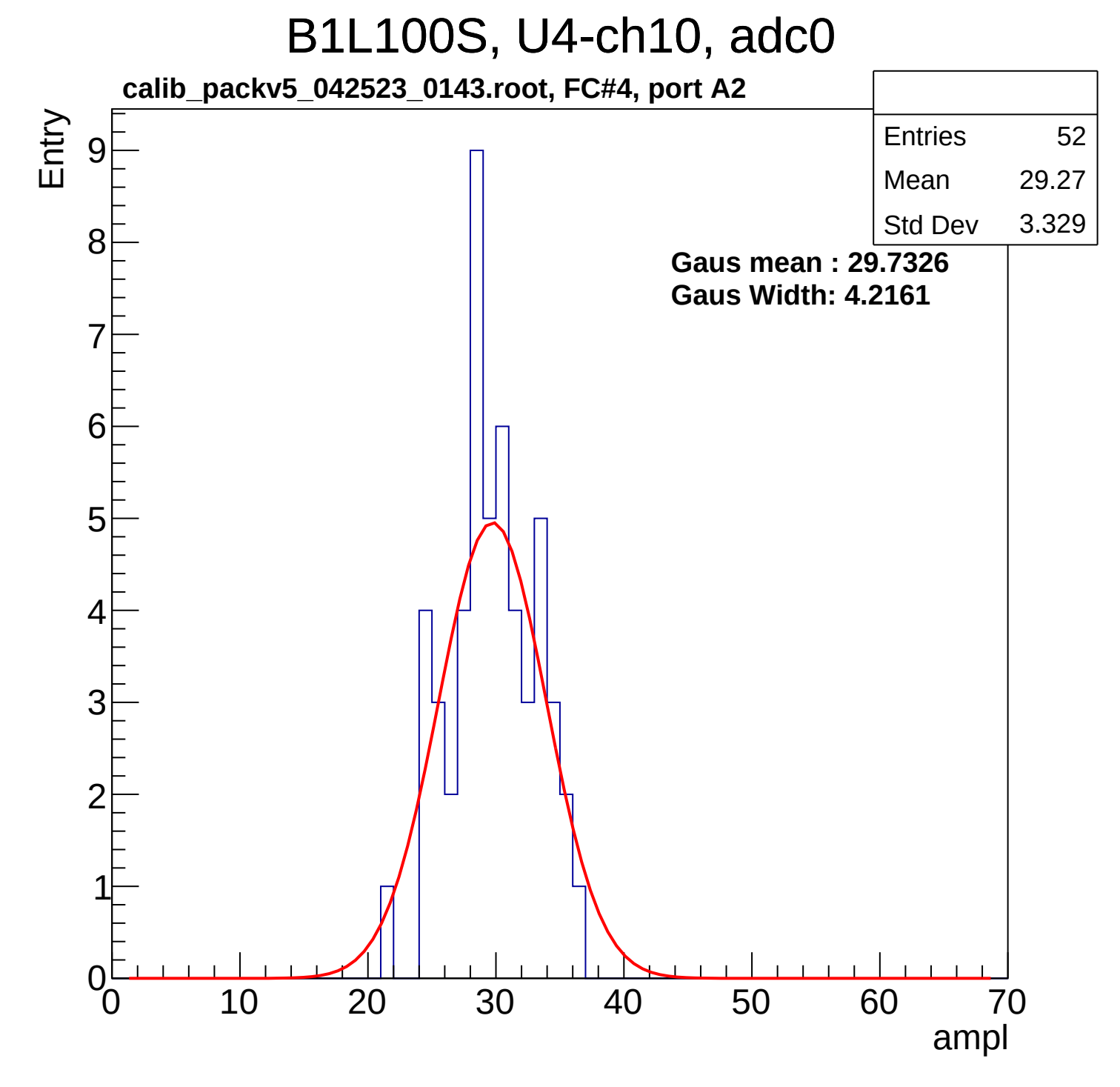

B1L100S, U4-ch9, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 48.4
Std Dev 3.143
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

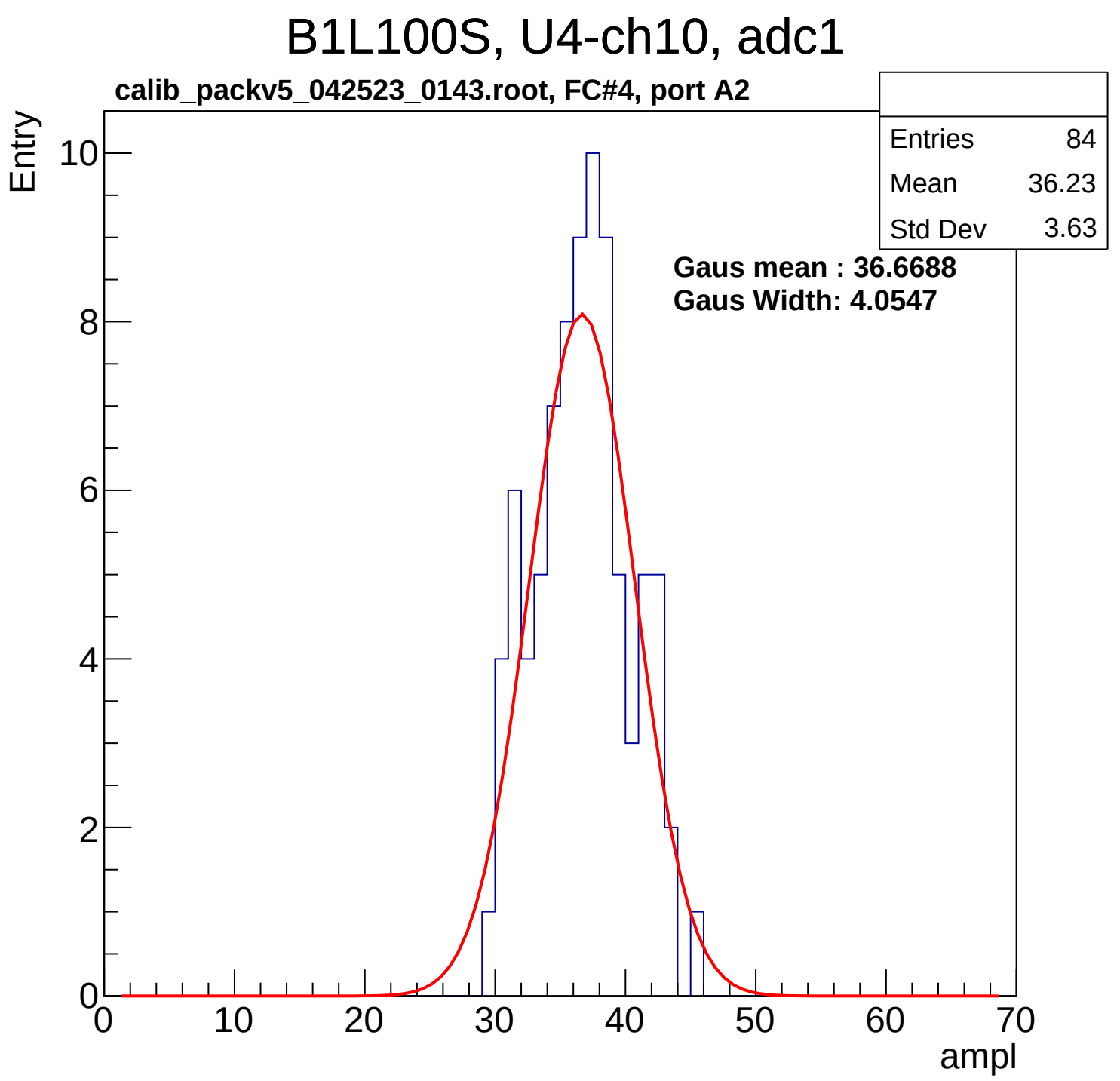

B1L100S, U4-ch9, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 54.61
Std Dev 3.737
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

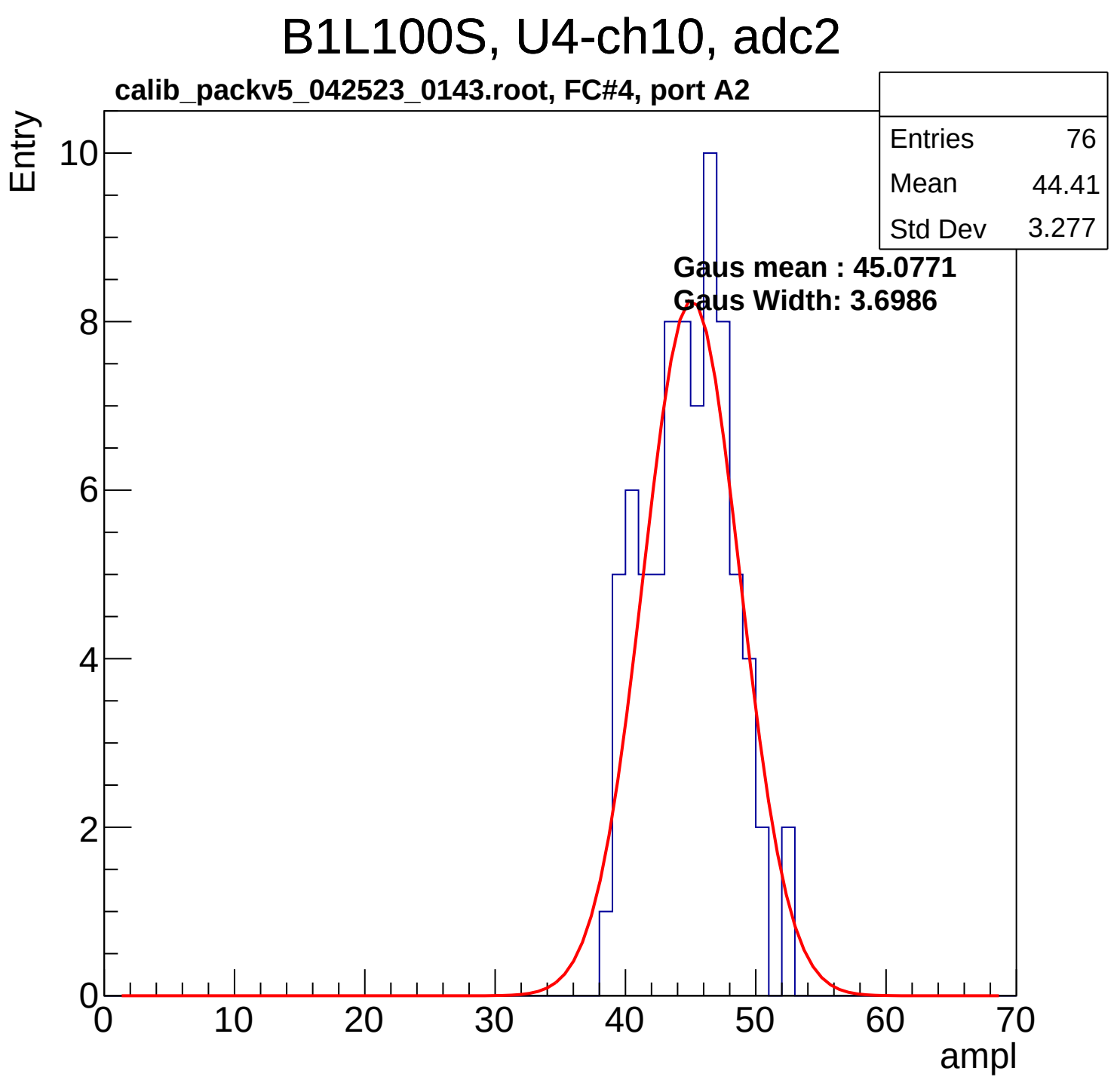

B1L100S, U4-ch9, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 39
Mean 60.18
Std Dev 2.135
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

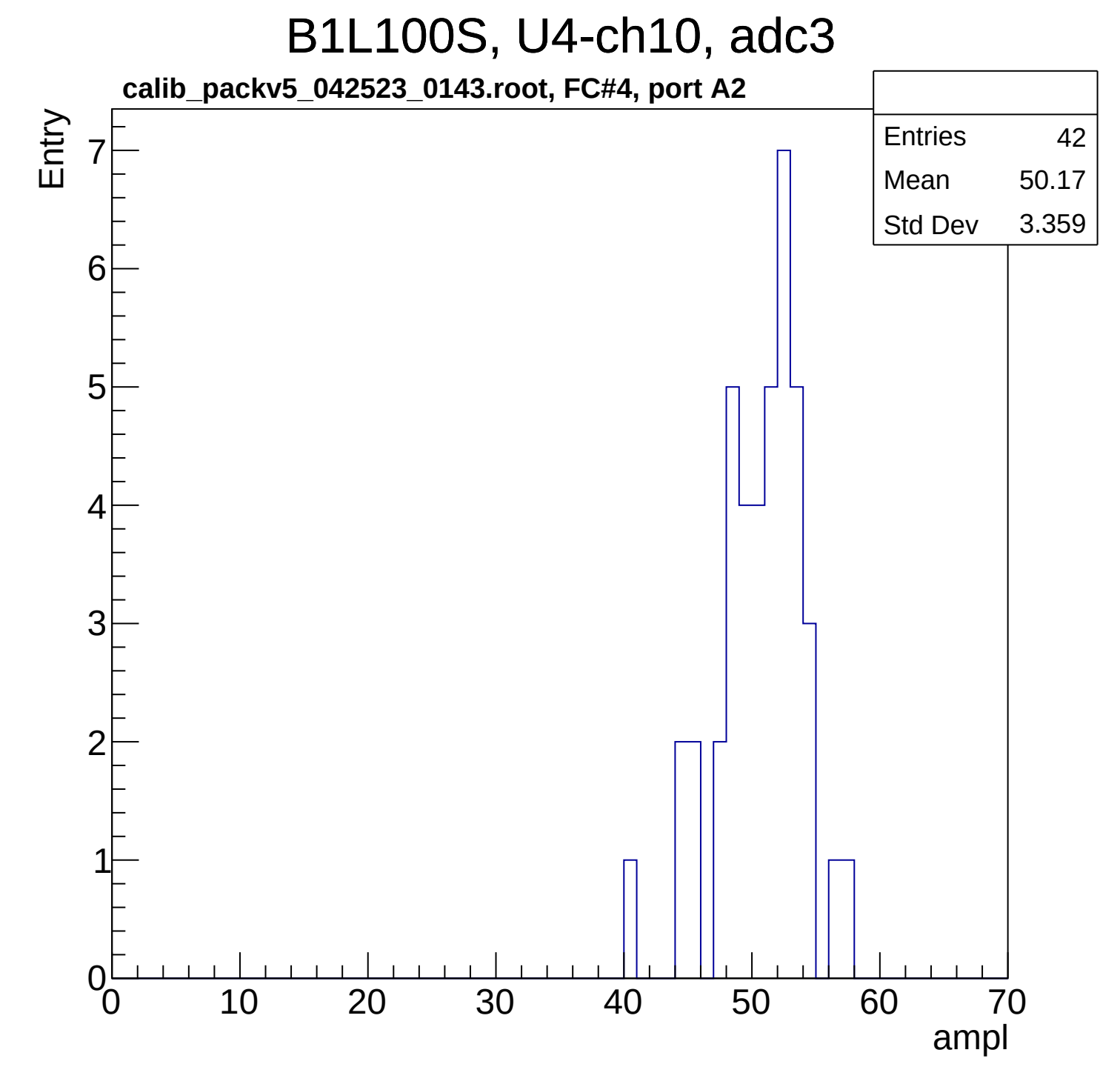

B1L100S, U4-ch9, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 54.67
Std Dev 19.42
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

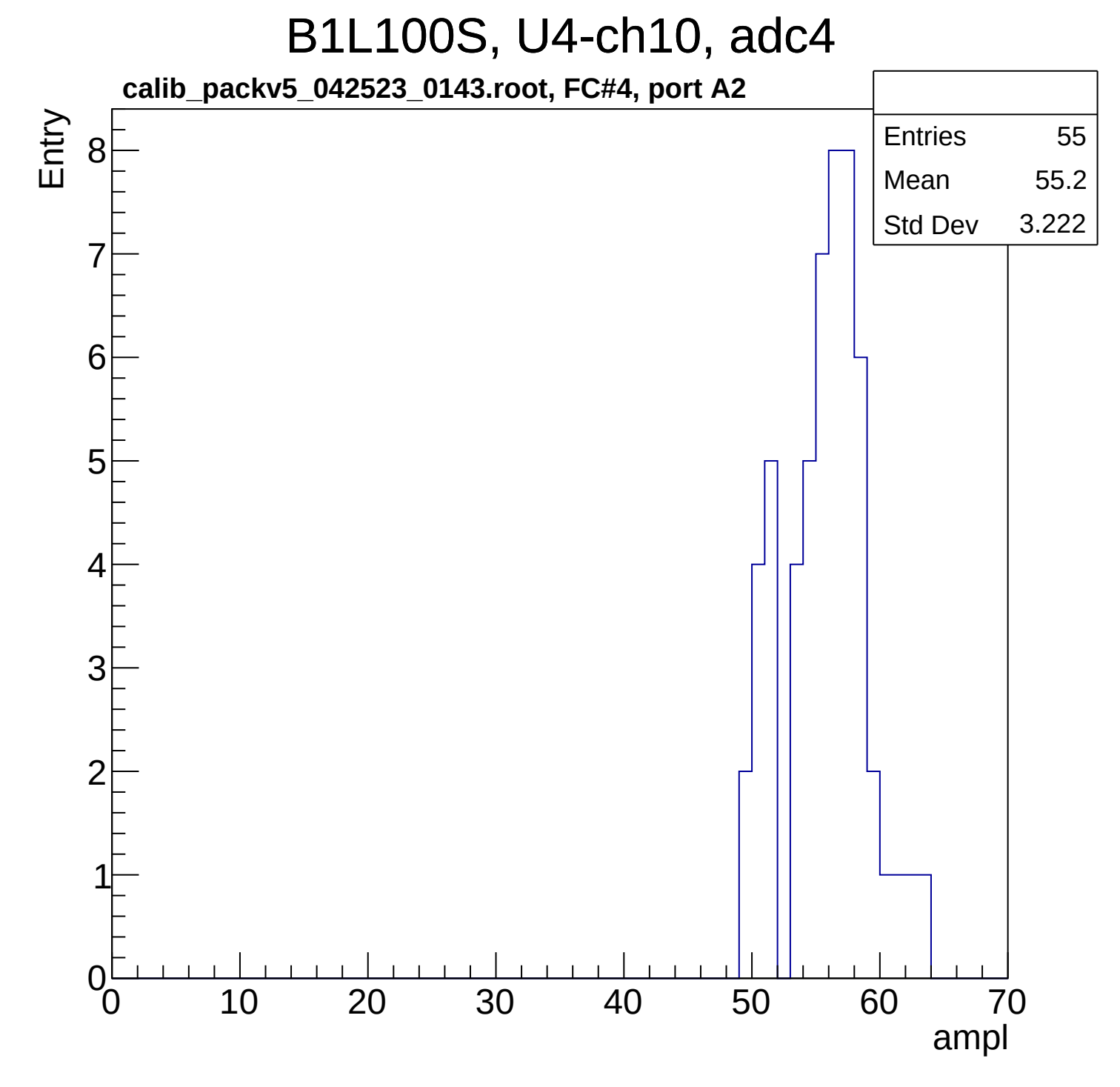

B1L100S, U4-ch9, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 21
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

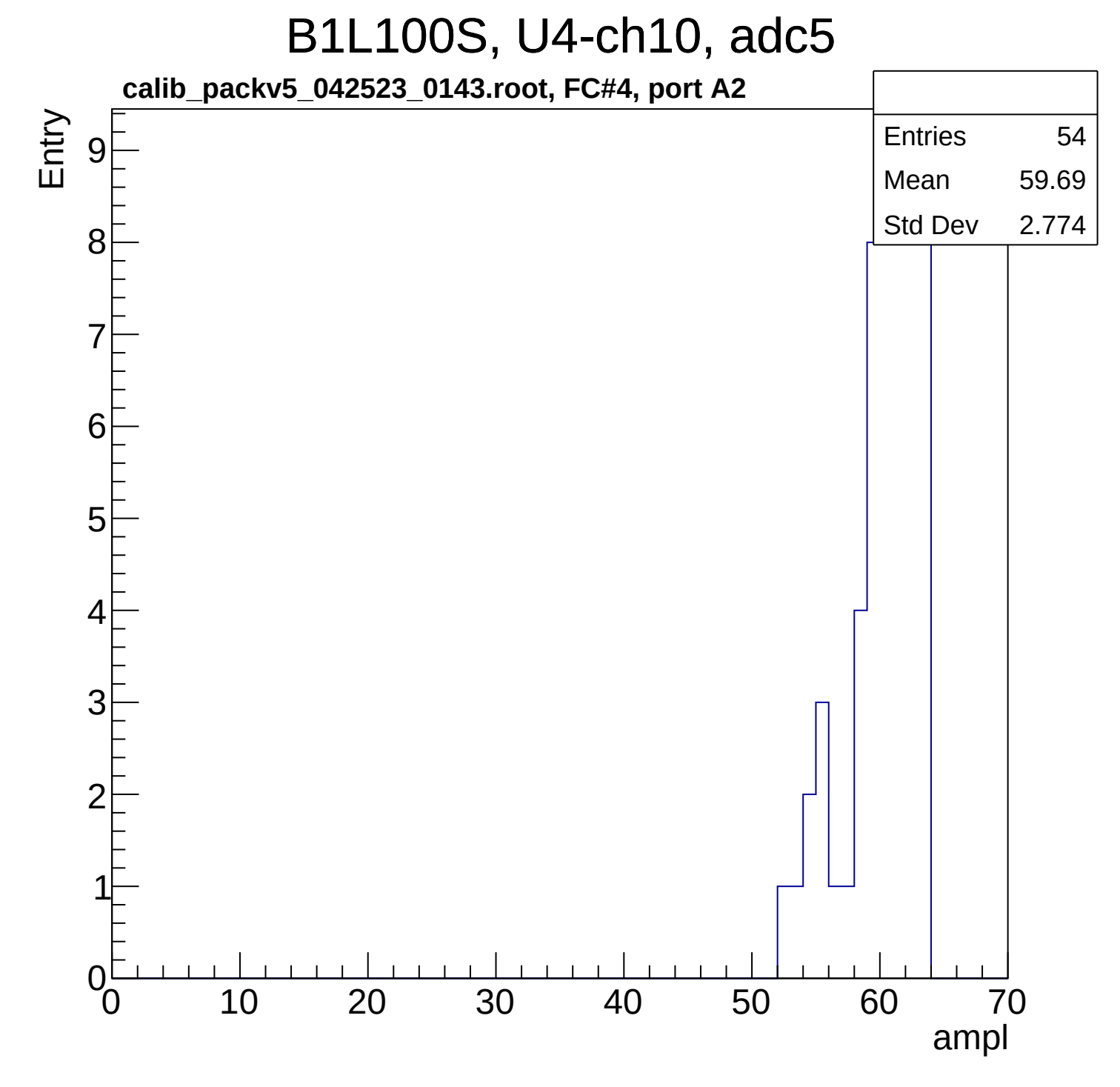

B1L100S, U4-ch10, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 29.27
Std Dev 3.329
Gaus mean : 29.7326
Gaus Width: 4.2161
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

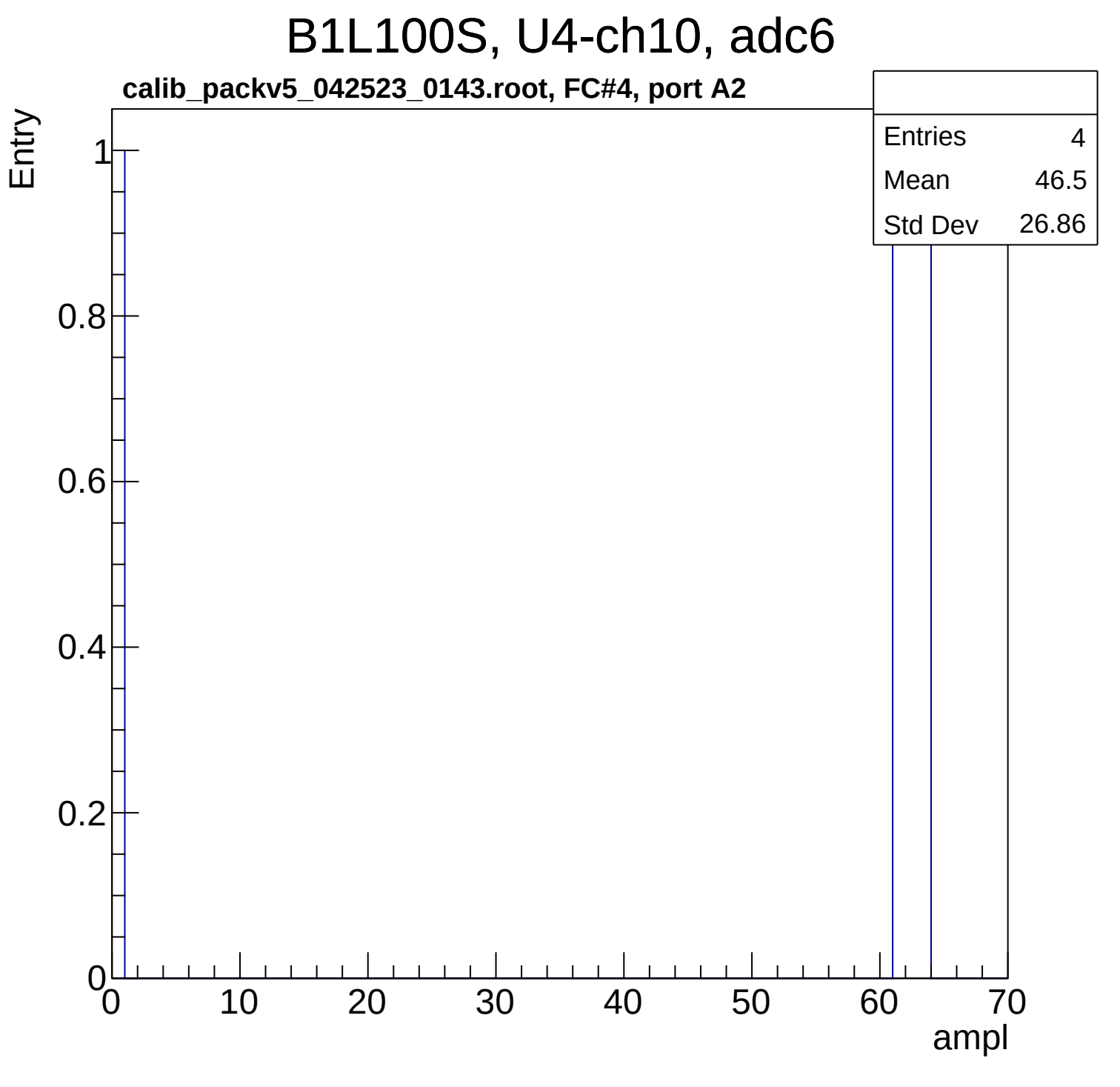

B1L100S, U4-ch10, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 84
Mean 36.23
Std Dev 3.63
Gaus mean : 36.6688
Gaus Width: 4.0547
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

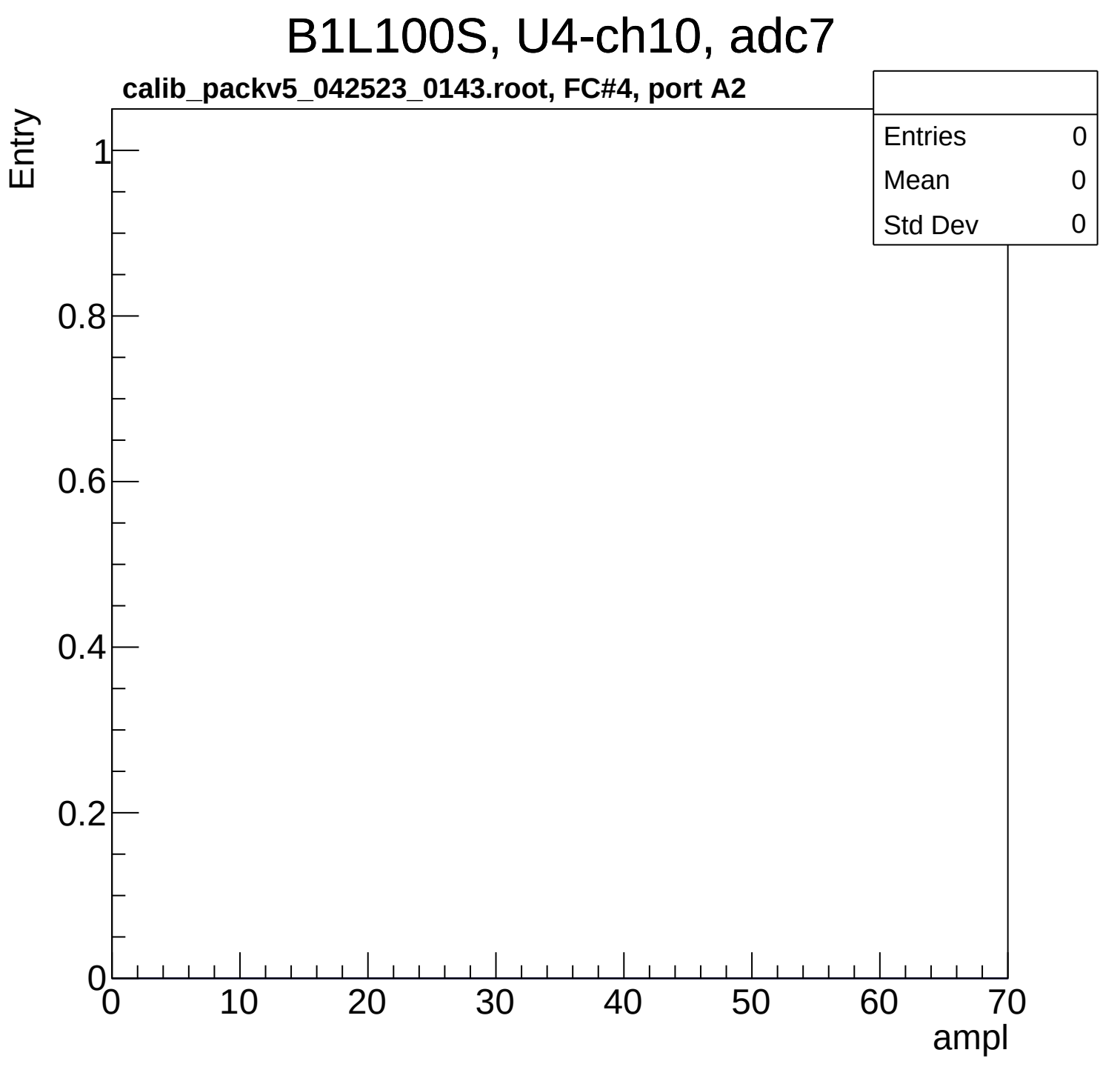

B1L100S, U4-ch10, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 44.41
Std Dev 3.277
Gaus mean : 45.0771
Gaus Width: 3.6986
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

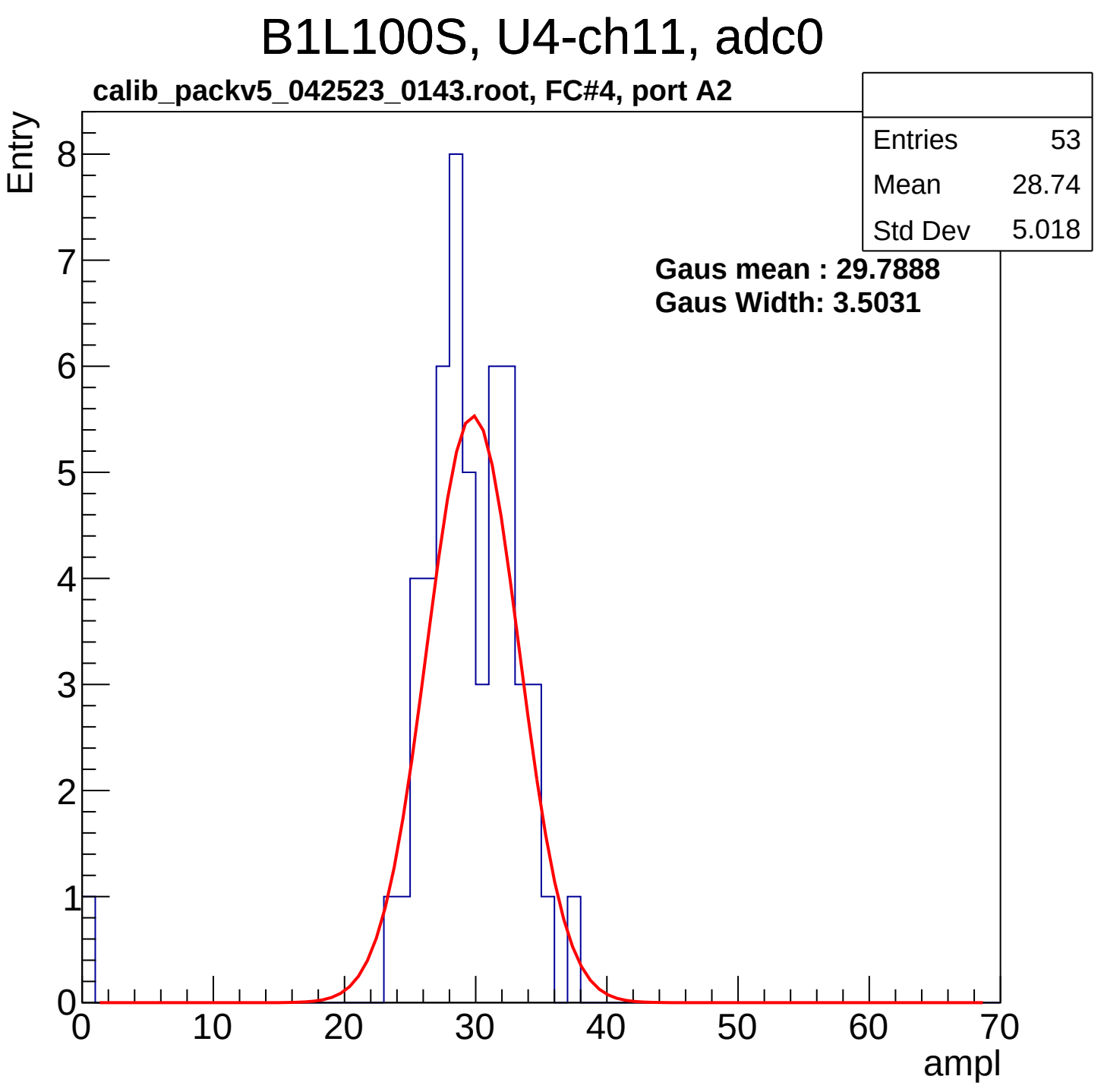

B1L100S, U4-ch10, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 42
Mean 50.17
Std Dev 3.359
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

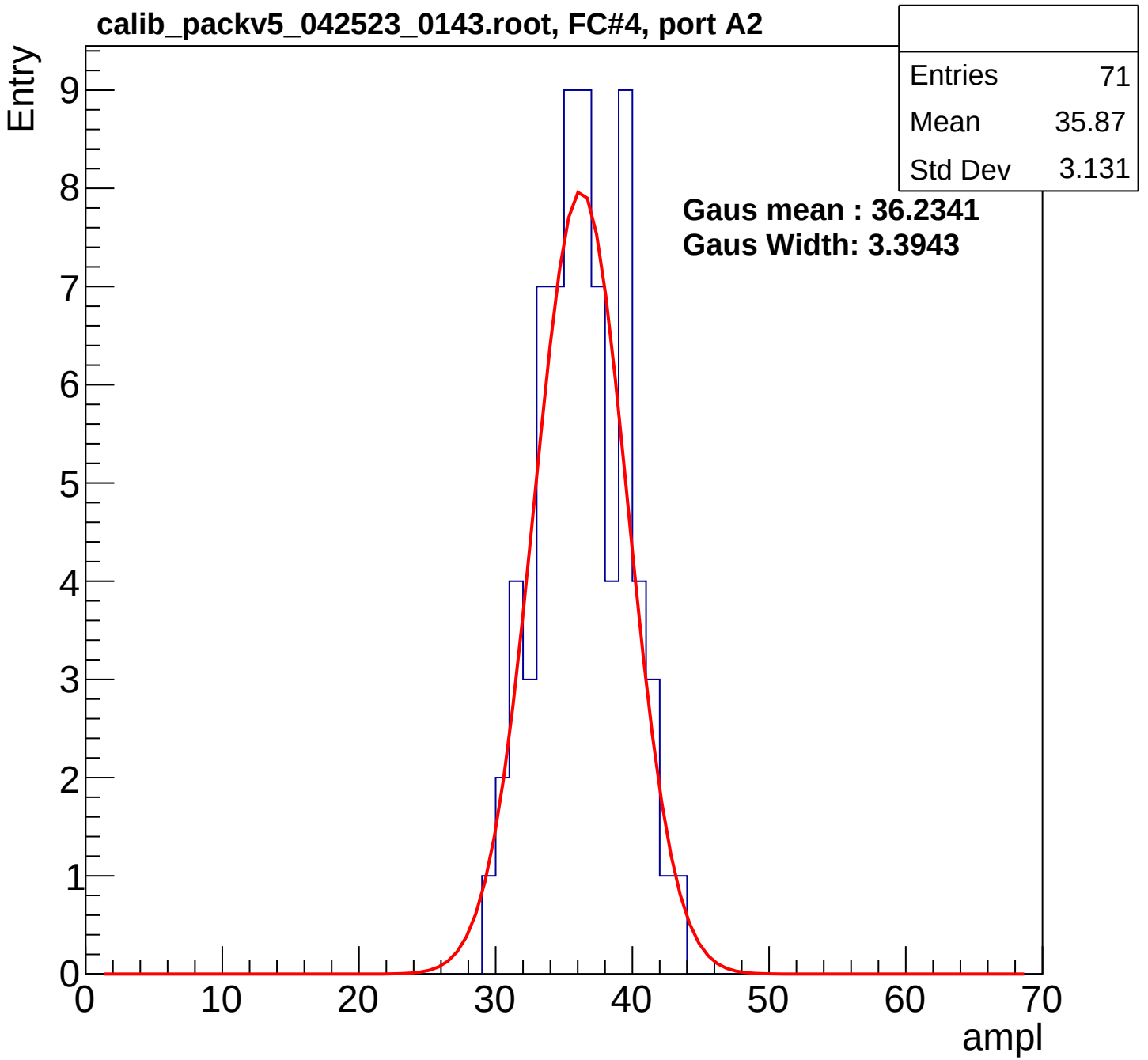

B1L100S, U4-ch10, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 55.2
Std Dev 3.222
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

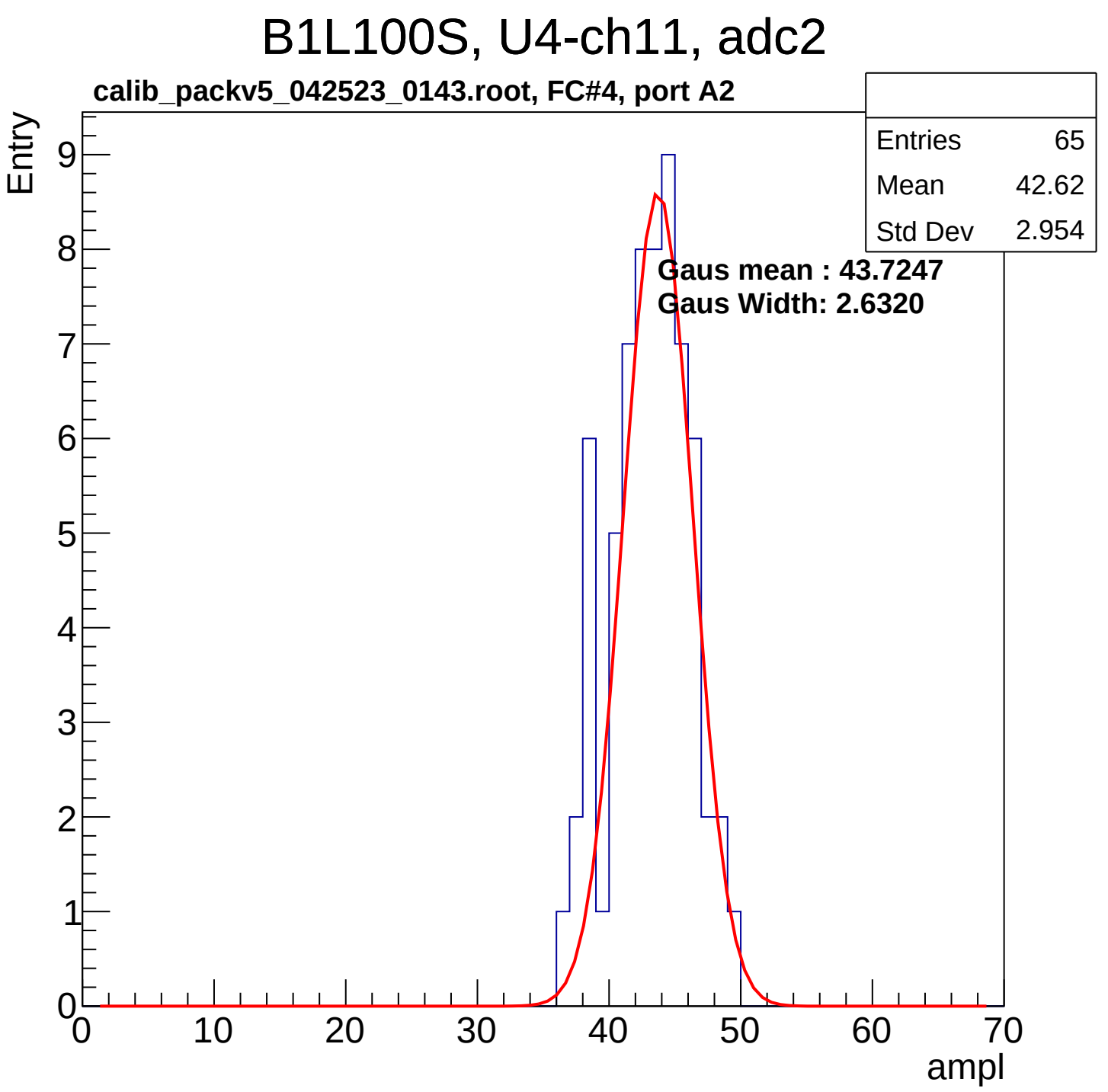

B1L100S, U4-ch10, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 59.69
Std Dev 2.774
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

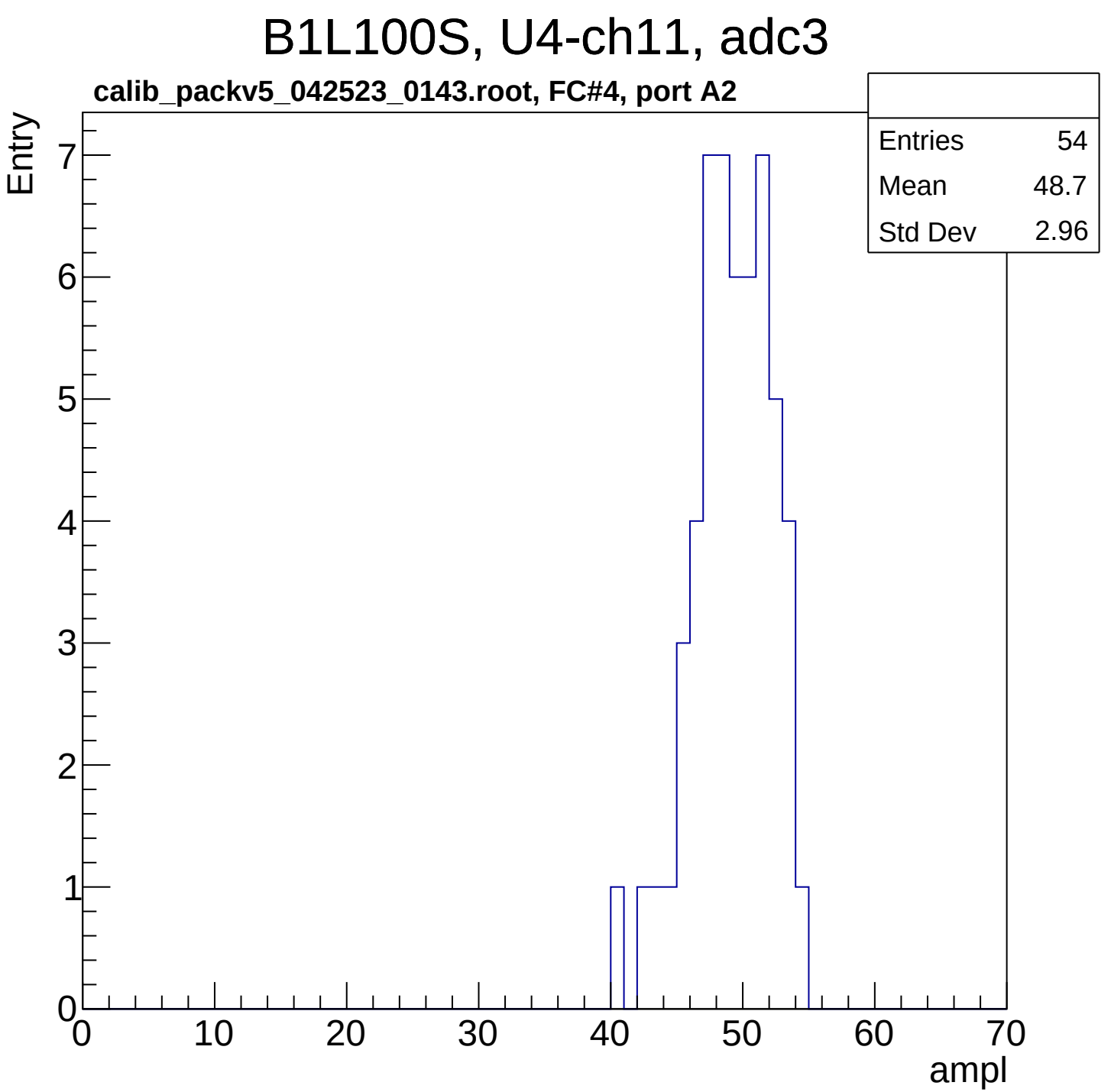

B1L100S, U4-ch10, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 46.5
Std Dev 26.86
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

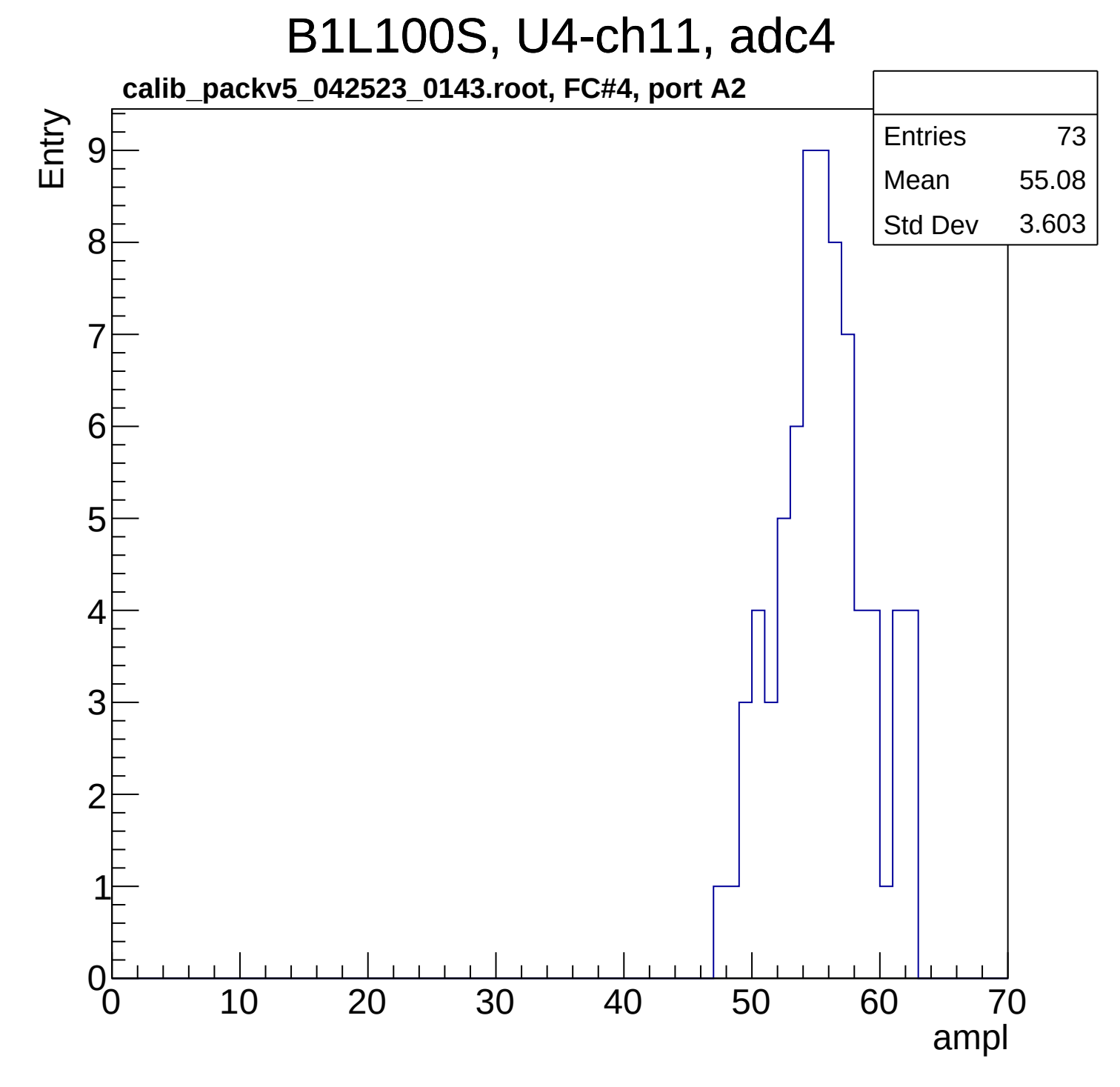

B1L100S, U4-ch10, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

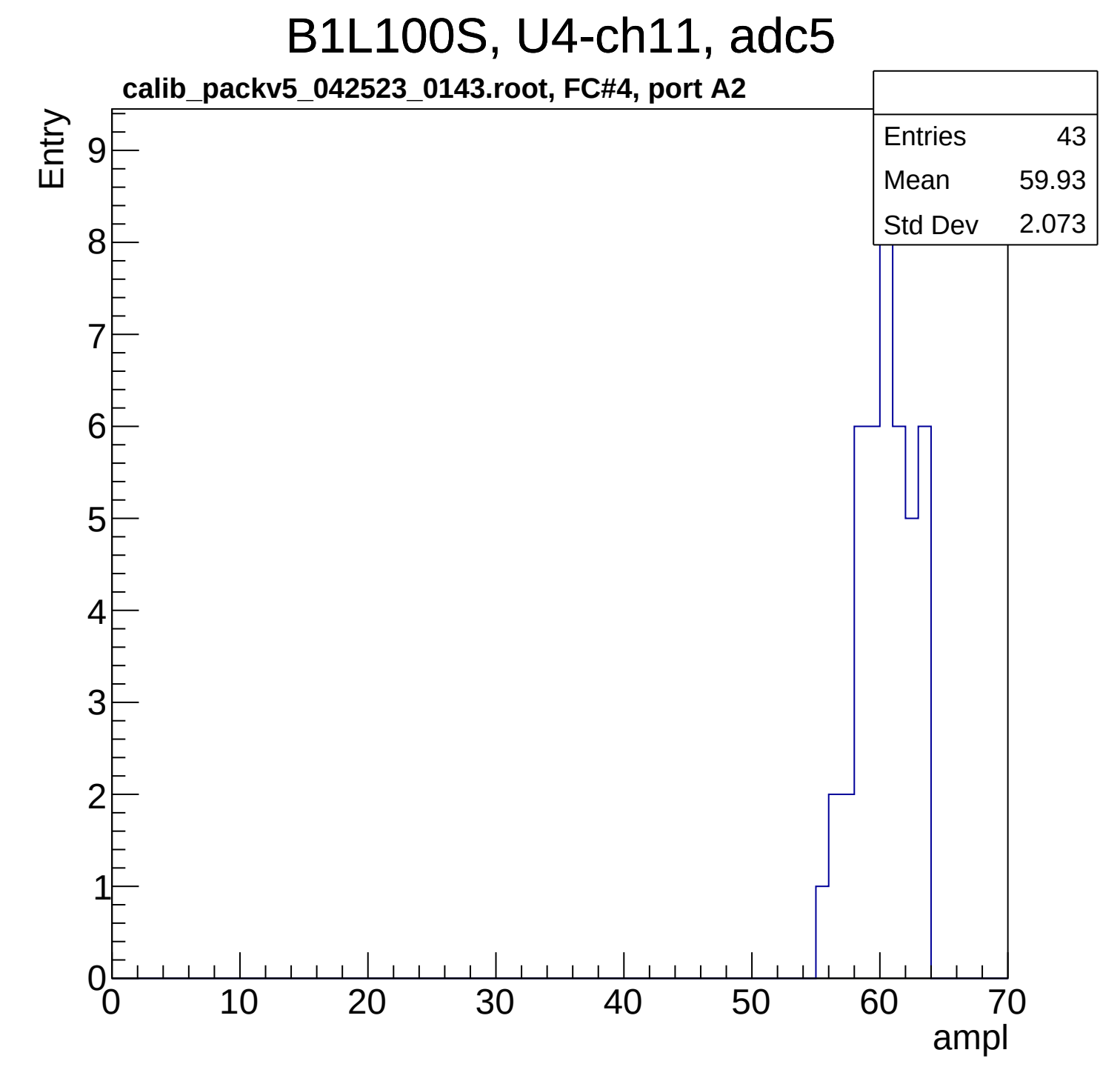

B1L100S, U4-ch11, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 28.74
Std Dev 5.018
Gaus mean : 29.7888
Gaus Width: 3.5031
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

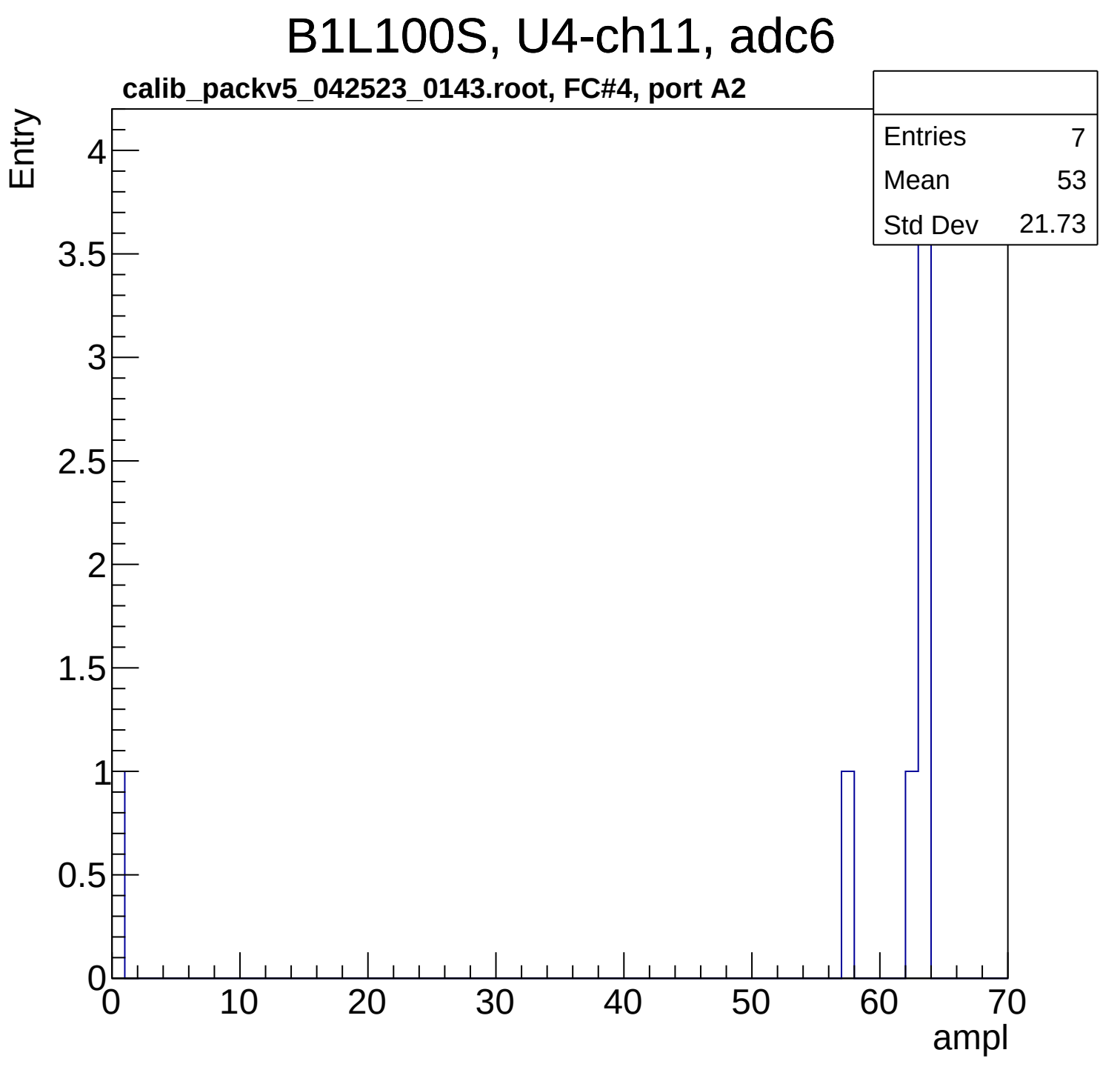

B1L100S, U4-ch11, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 35.87
Std Dev 3.131
Gaus mean : 36.2341
Gaus Width: 3.3943
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

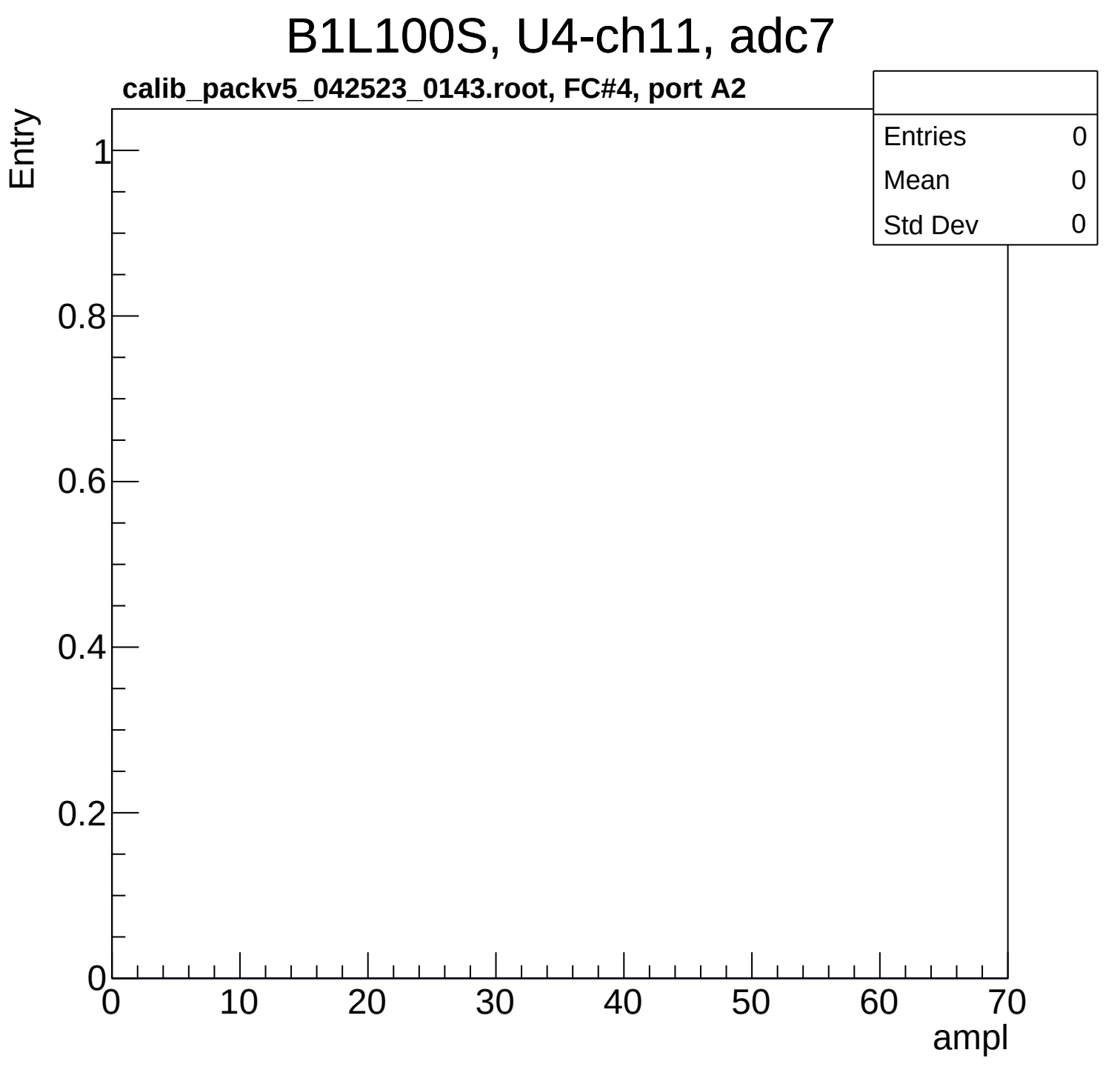

B1L100S, U4-ch11, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 42.62
Std Dev 2.954
Gaus mean : 43.7247
Gaus Width: 2.6320
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

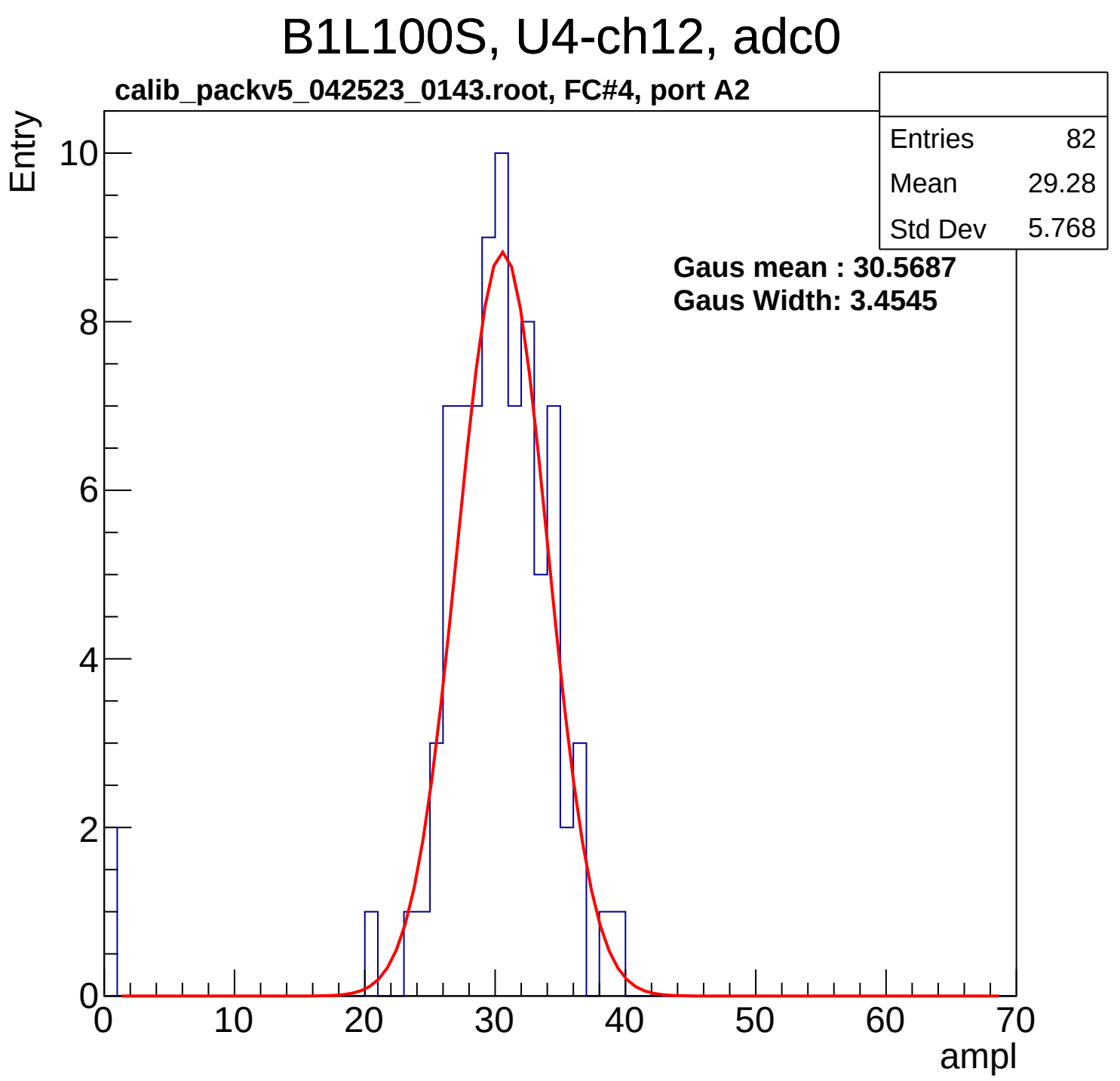

B1L100S, U4-ch11, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 48.7
Std Dev 2.96
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

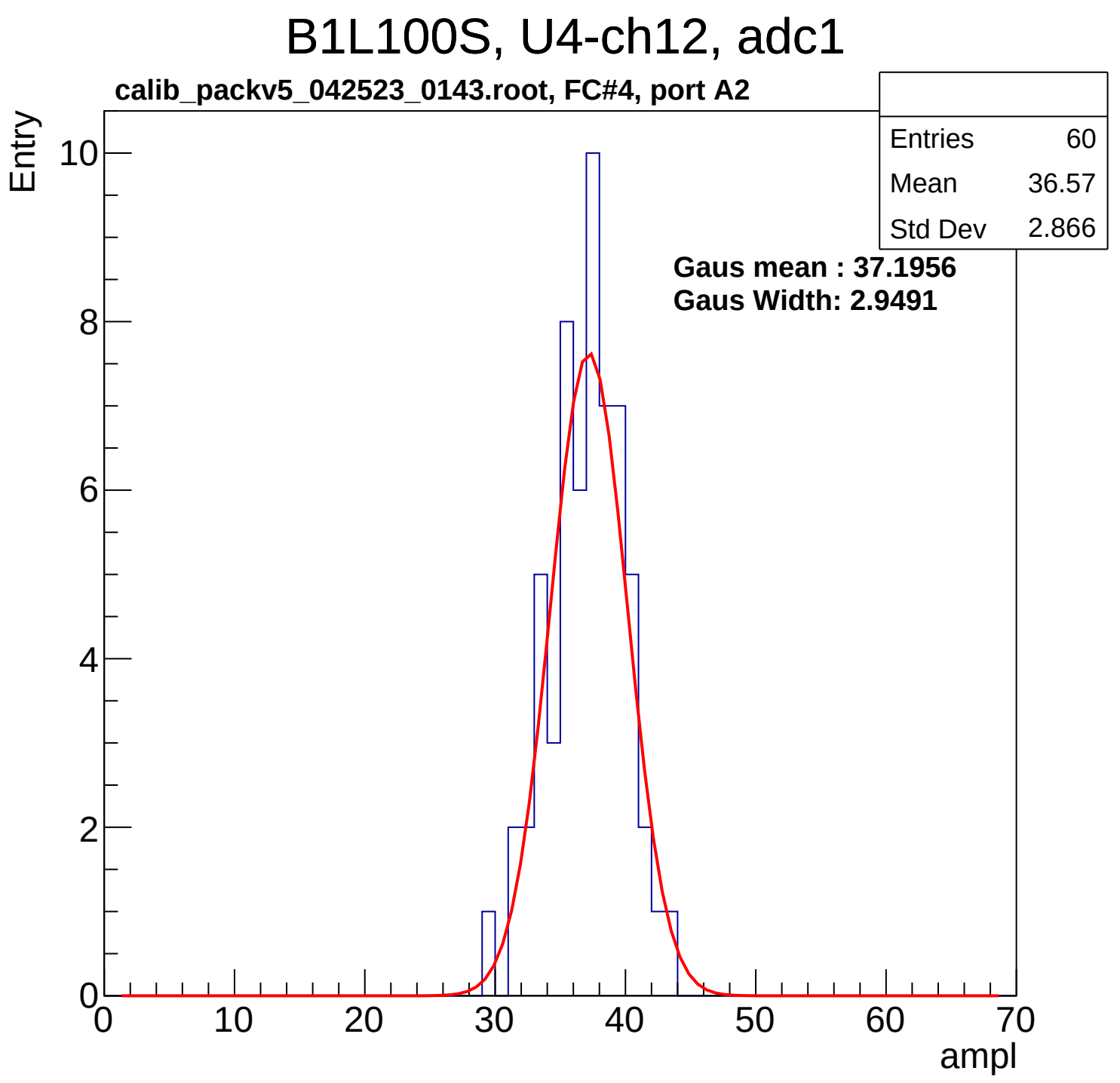

B1L100S, U4-ch11, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 55.08
Std Dev 3.603
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

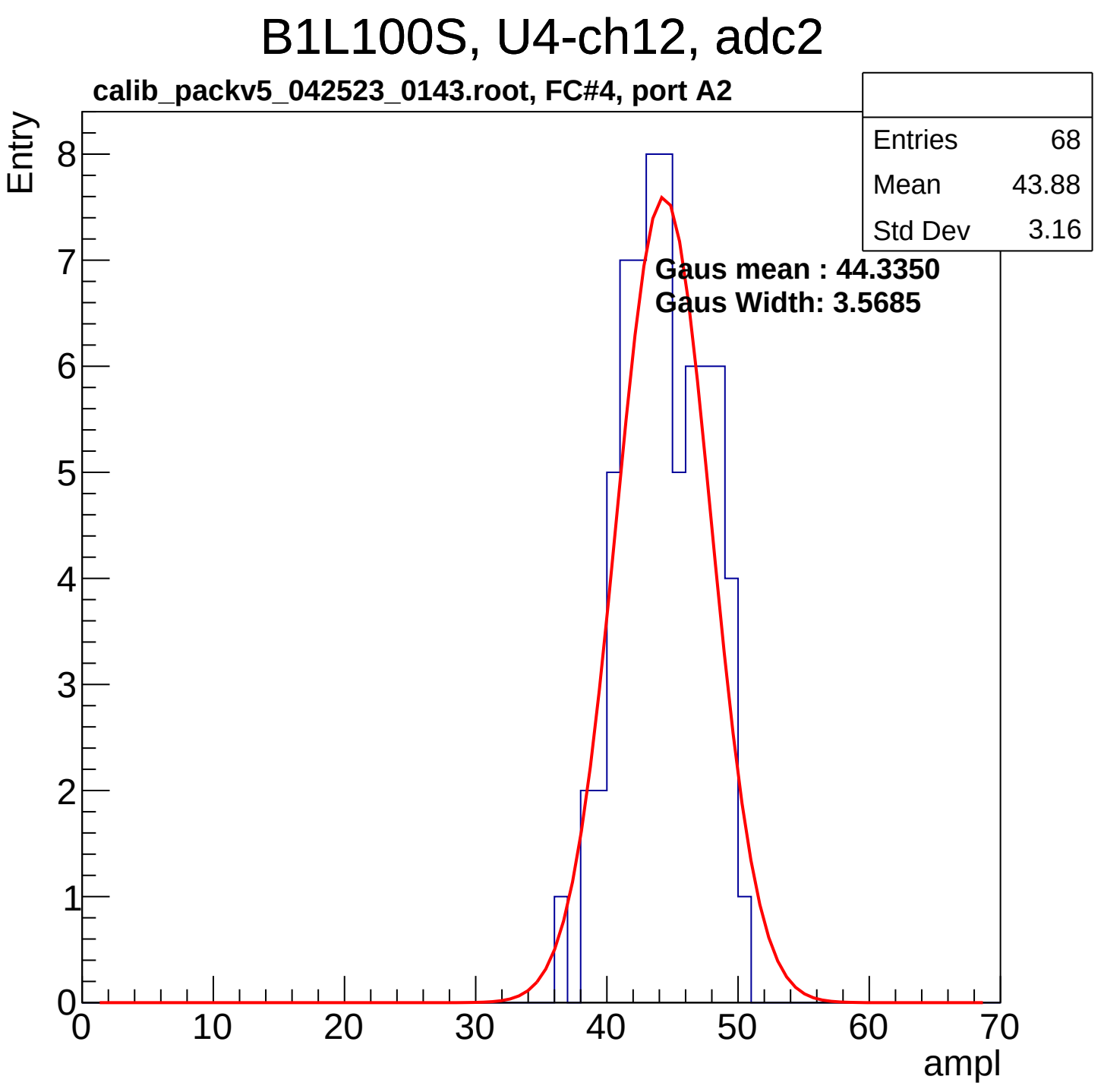

B1L100S, U4-ch11, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 59.93
Std Dev 2.073
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

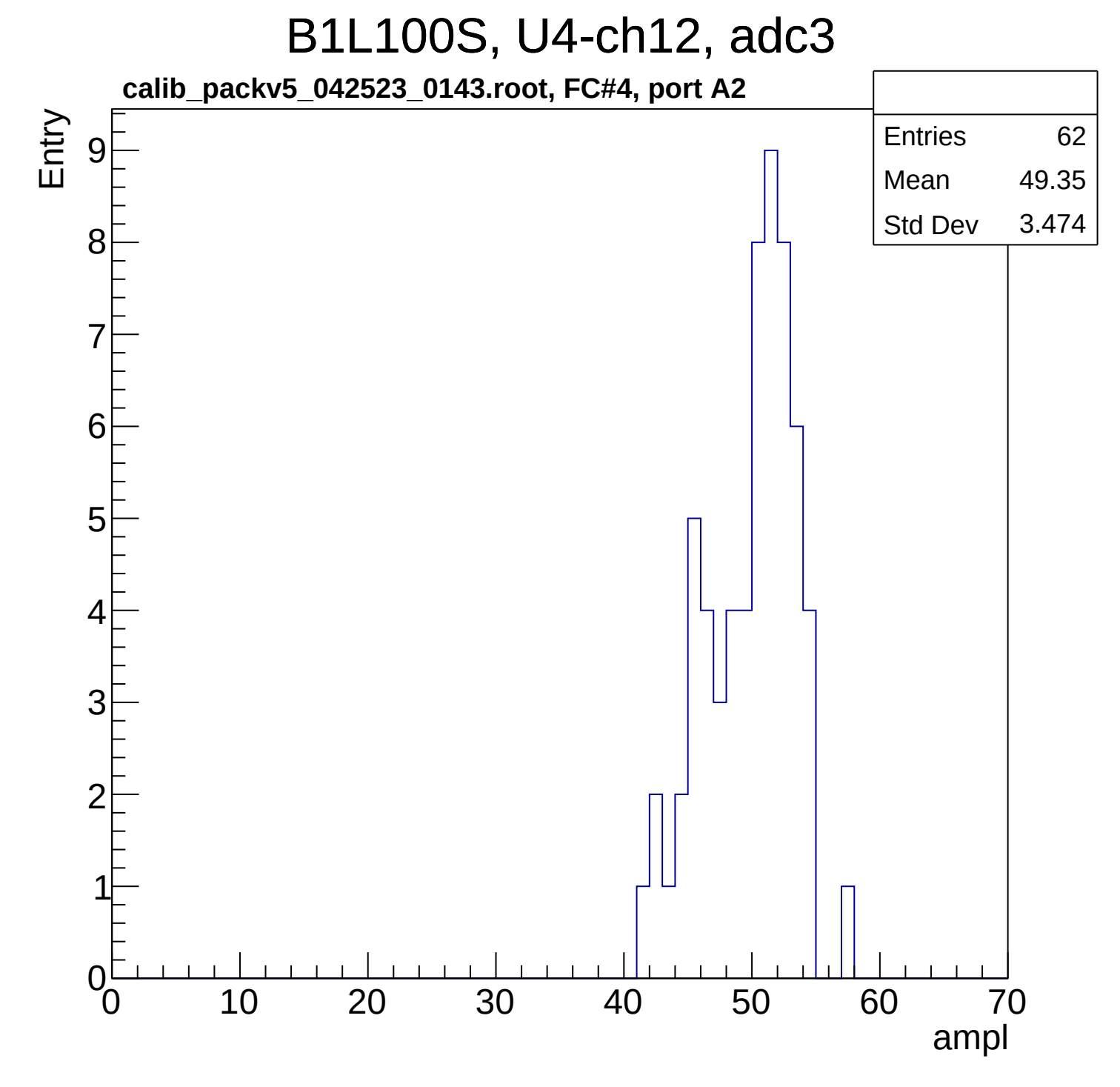

B1L100S, U4-ch11, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 53
Std Dev 21.73
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

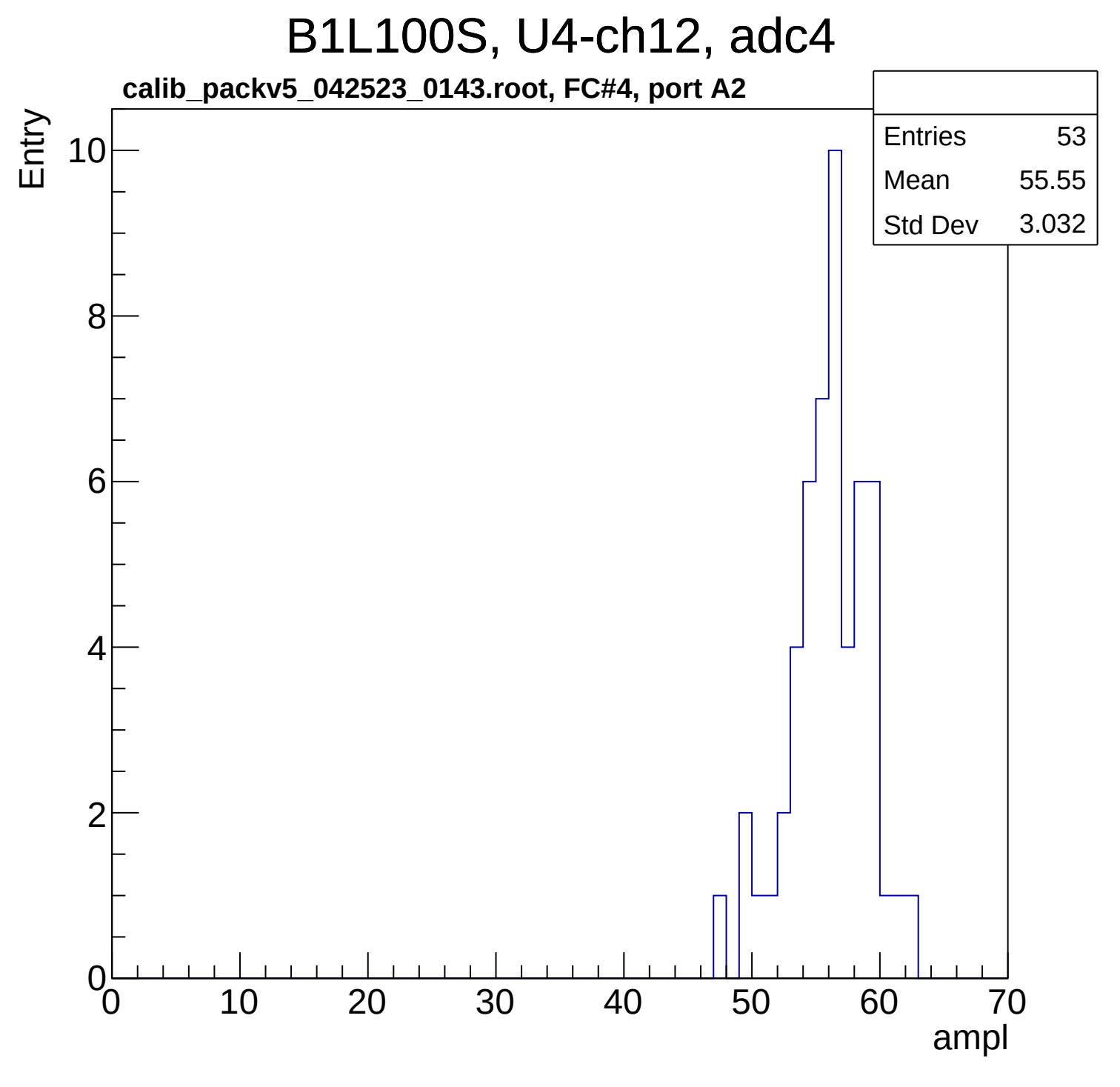

B1L100S, U4-ch11, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

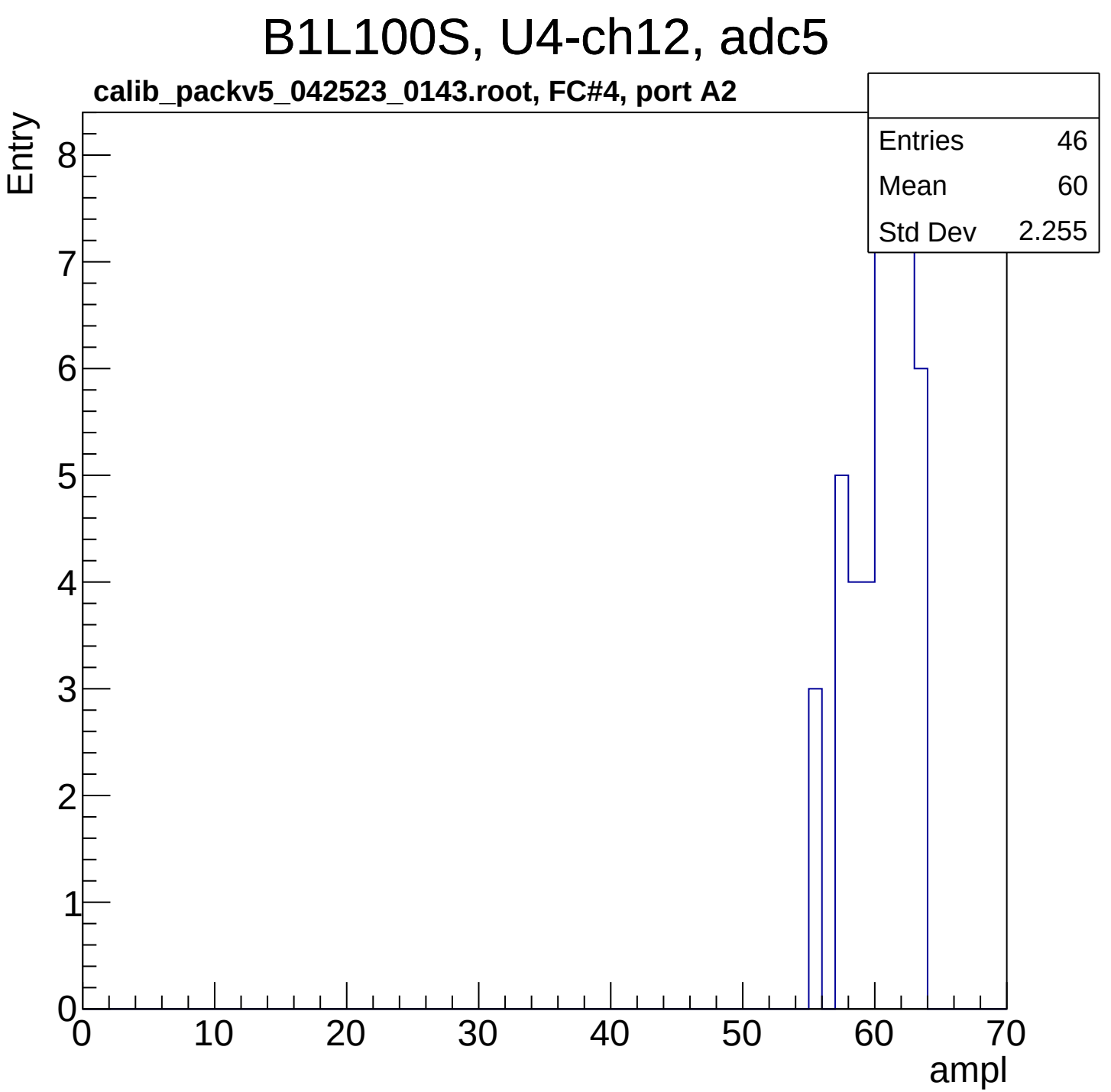

B1L100S, U4-ch12, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 29.28
Std Dev 5.768
Gaus mean : 30.5687
Gaus Width: 3.4545
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

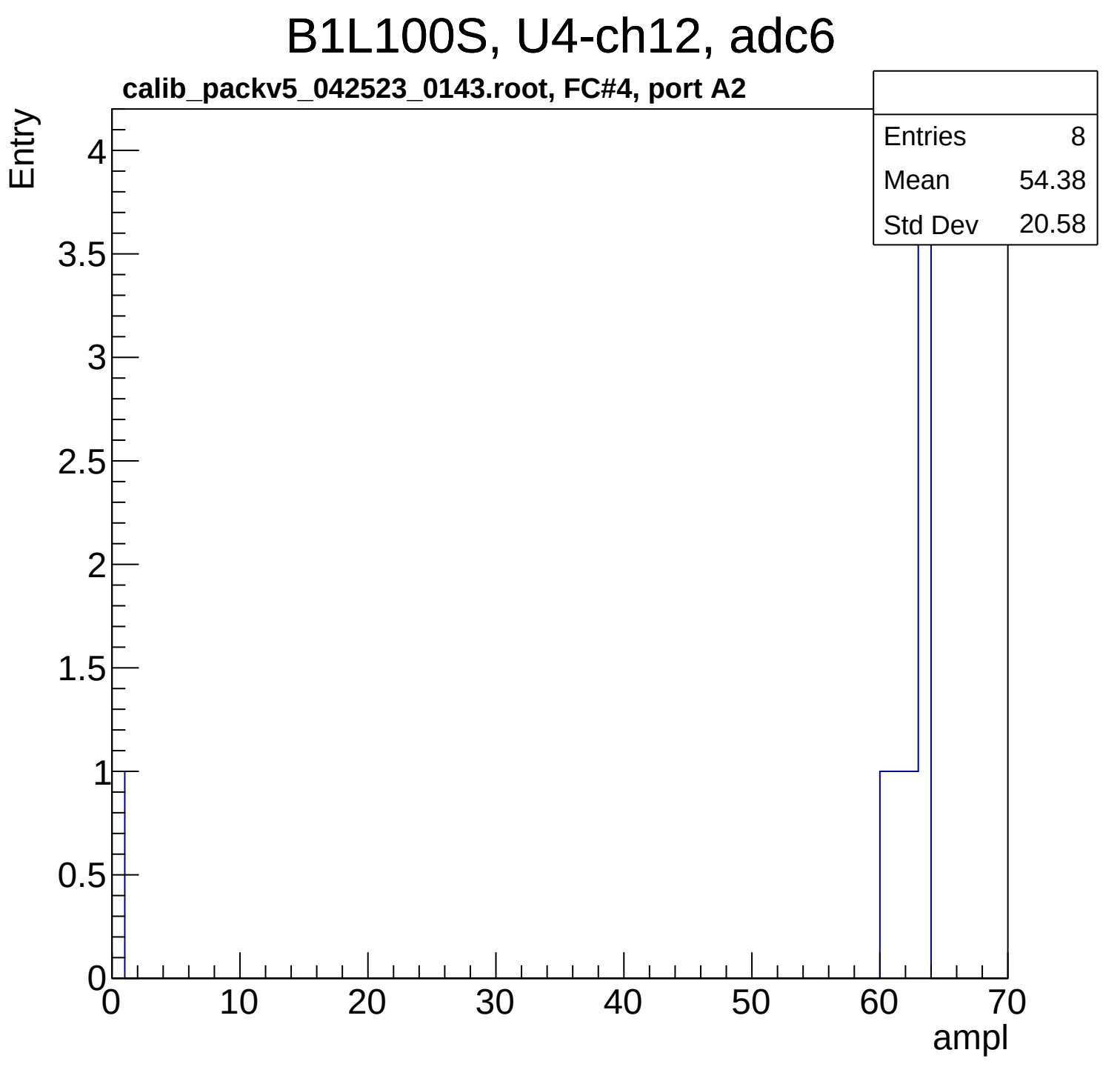

B1L100S, U4-ch12, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 36.57
Std Dev 2.866
Gaus mean : 37.1956
Gaus Width: 2.9491
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

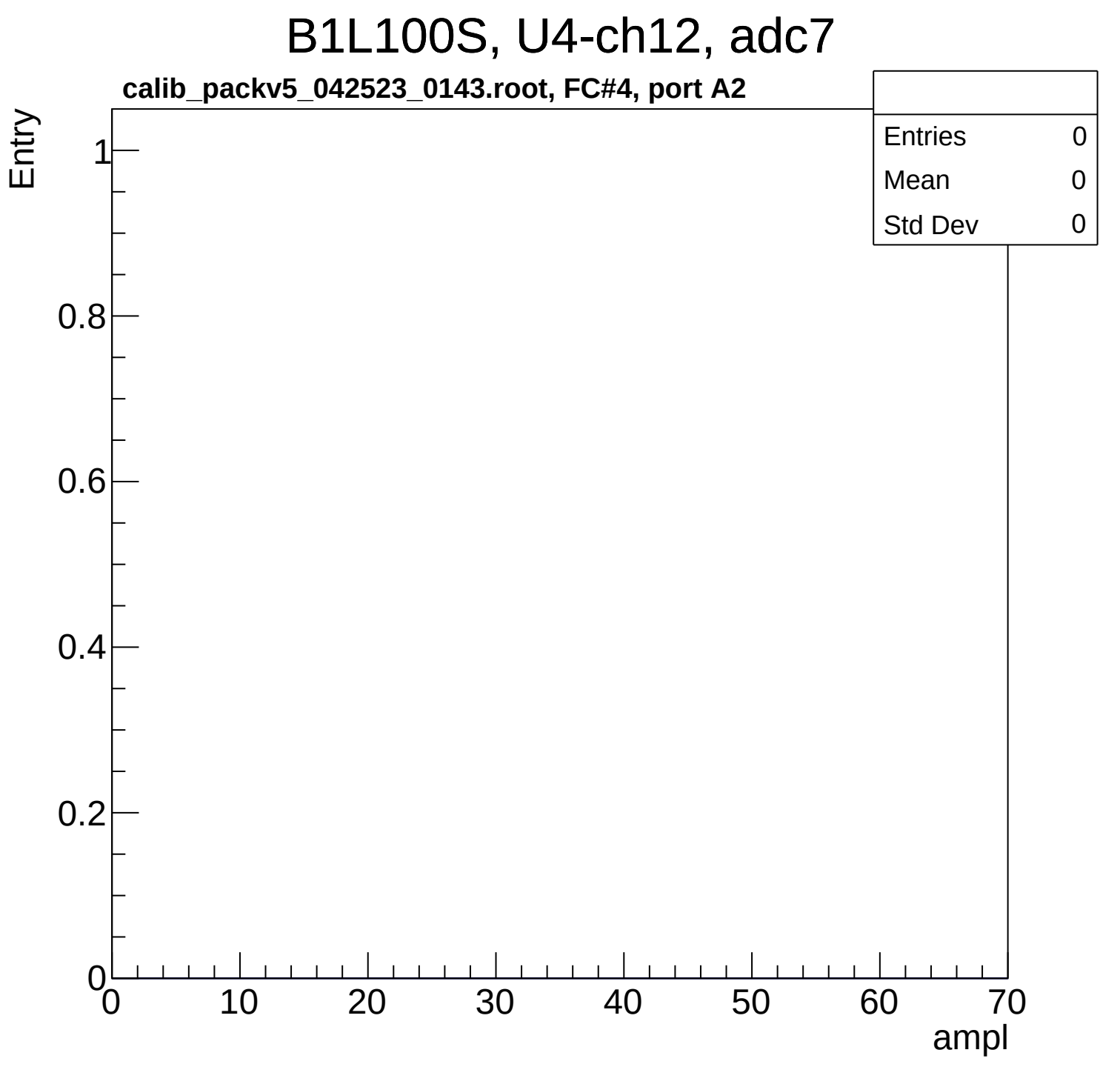

B1L100S, U4-ch12, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 43.88
Std Dev 3.16
Gaus mean : 44.3350
Gaus Width: 3.5685
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

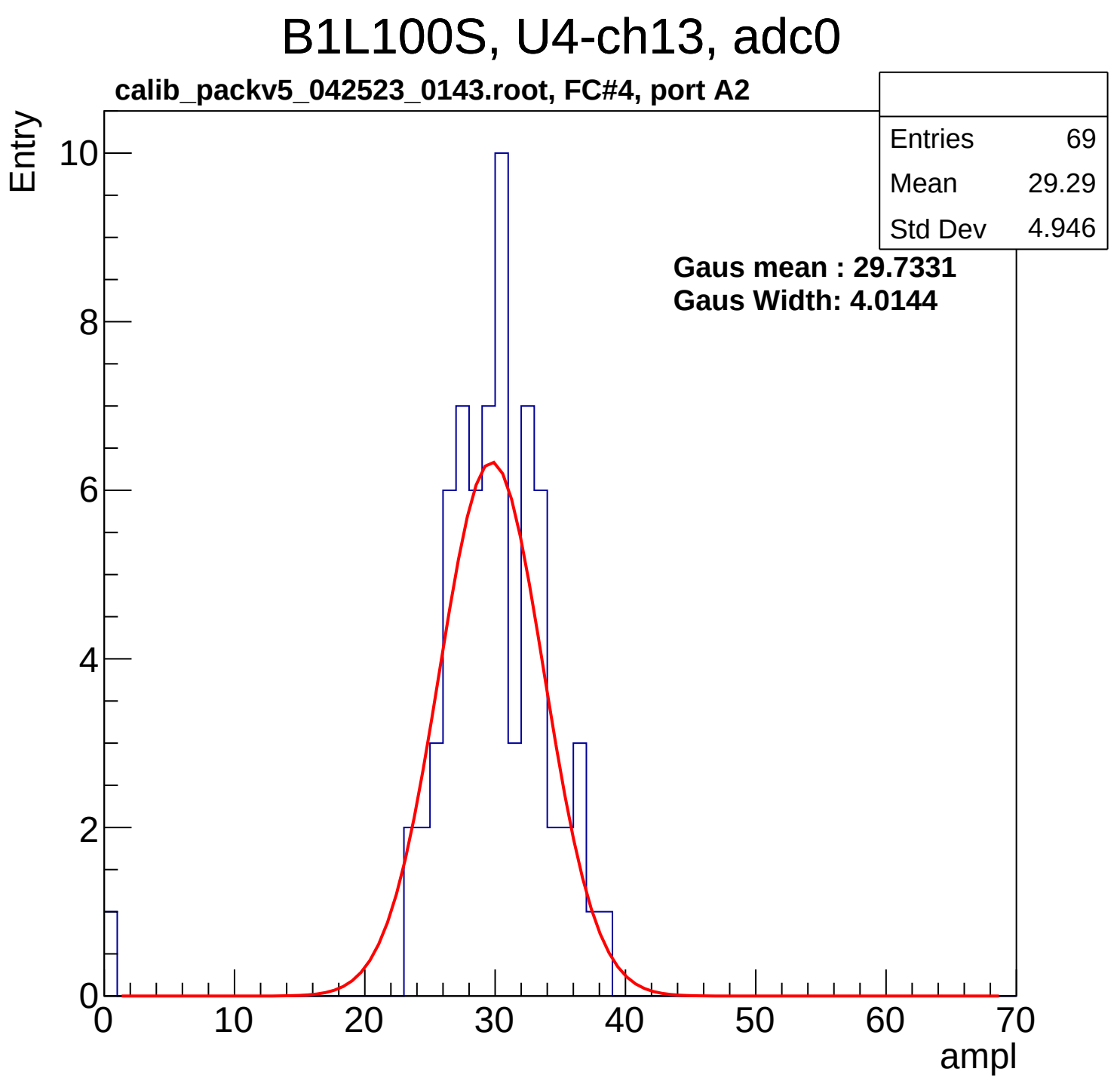

B1L100S, U4-ch12, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 49.35
Std Dev 3.474
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

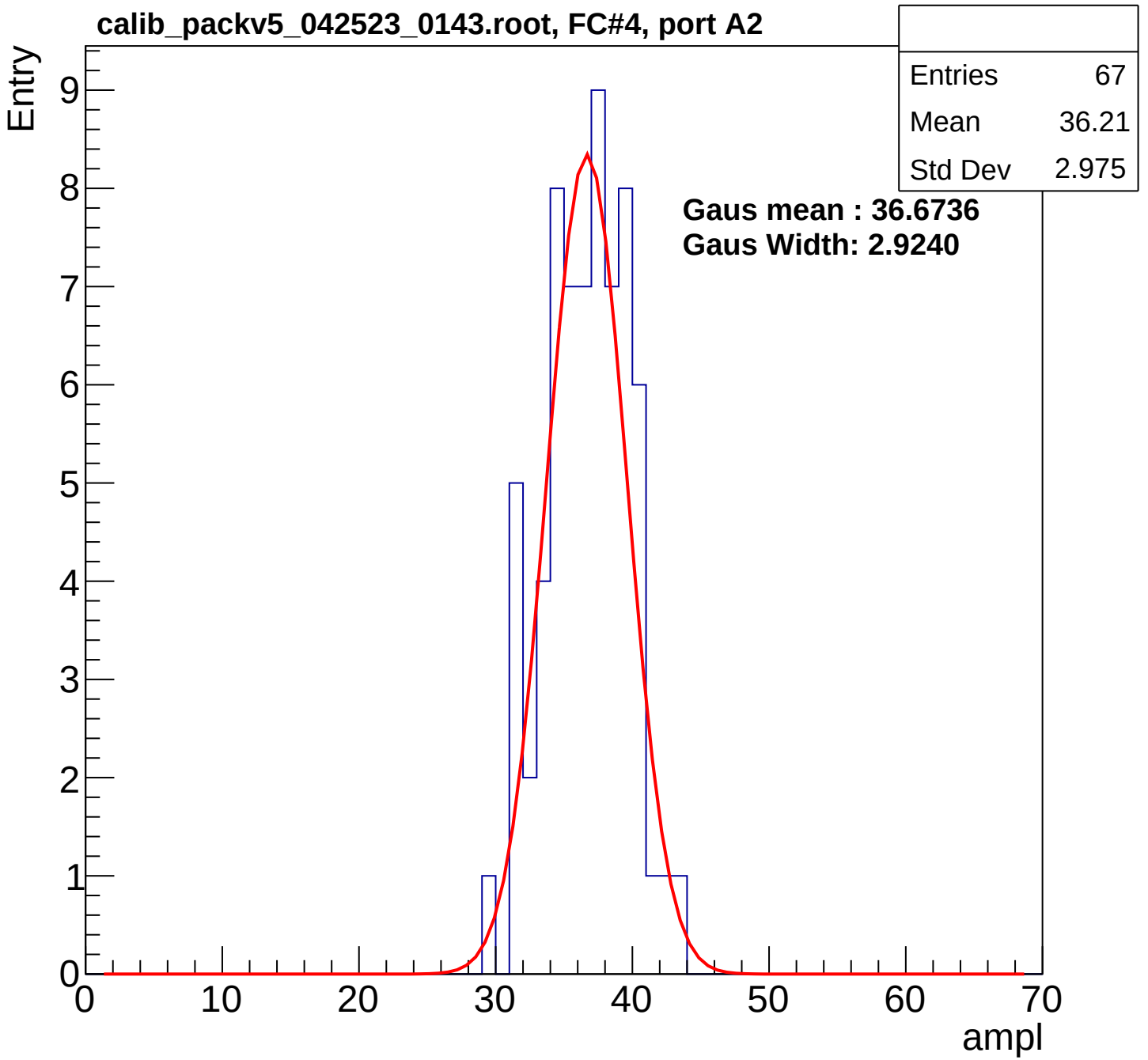

B1L100S, U4-ch12, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 55.55
Std Dev 3.032
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

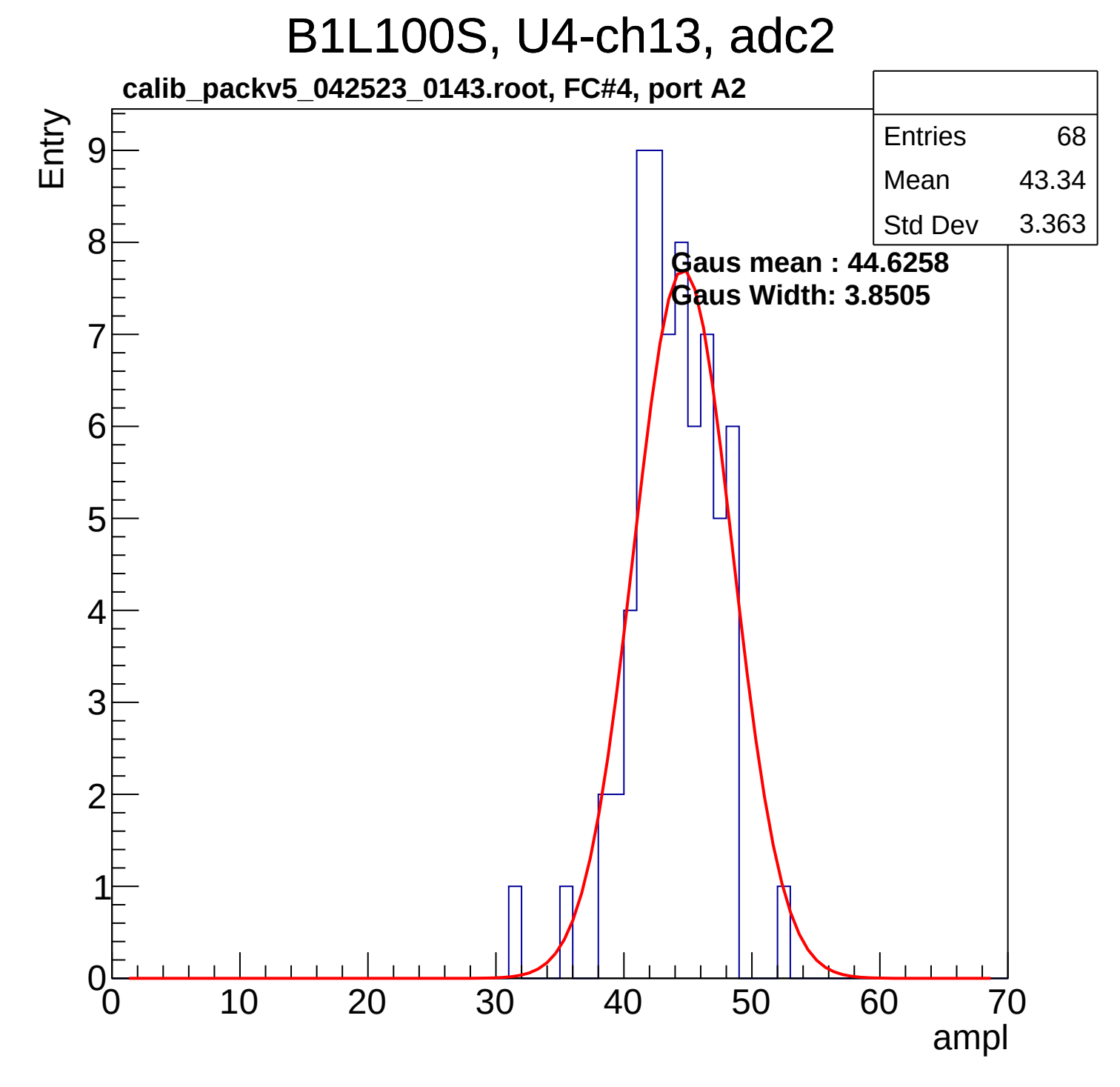

B1L100S, U4-ch12, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 60
Std Dev 2.255
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

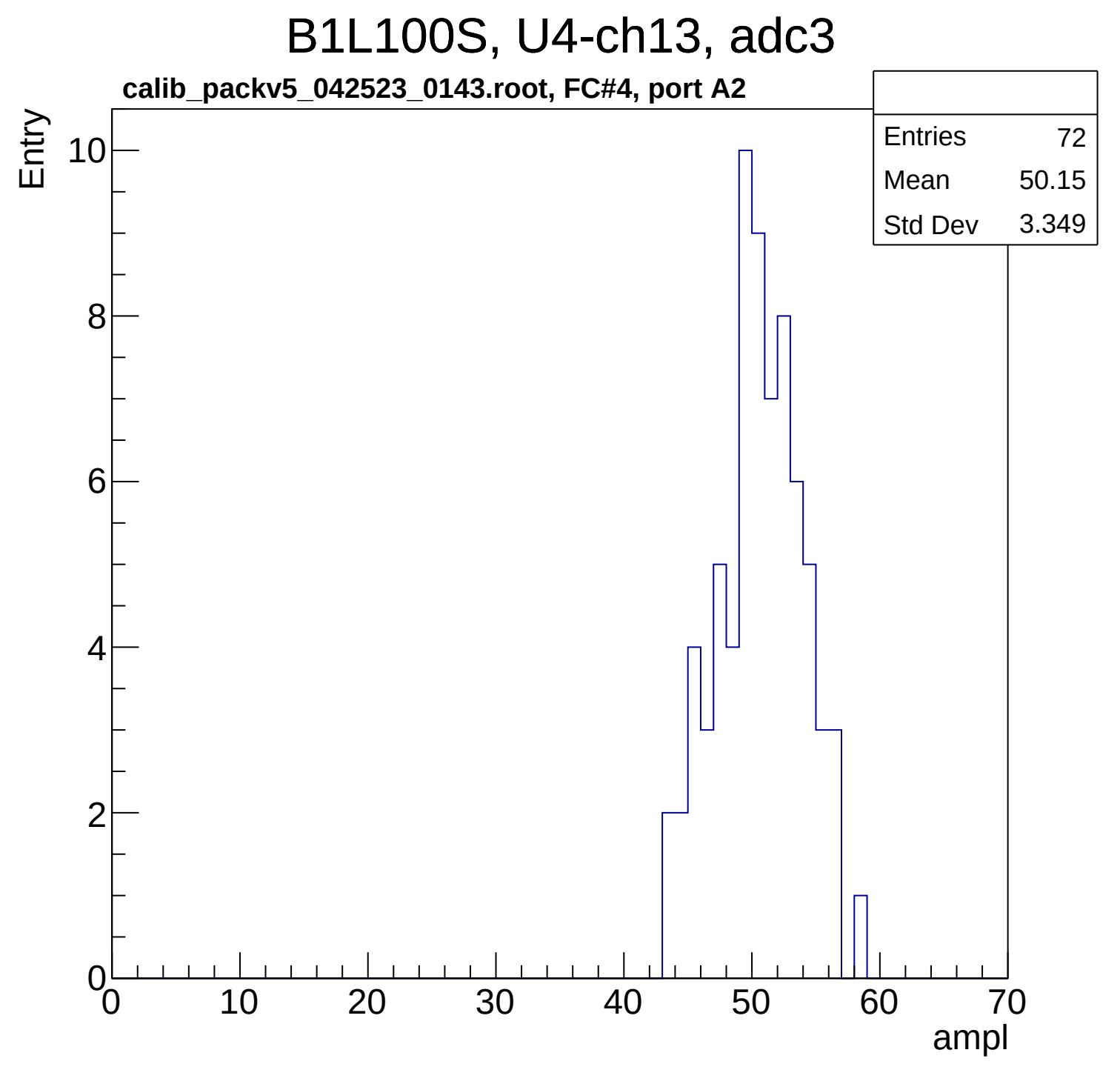

B1L100S, U4-ch12, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 8
Mean 54.38
Std Dev 20.58
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

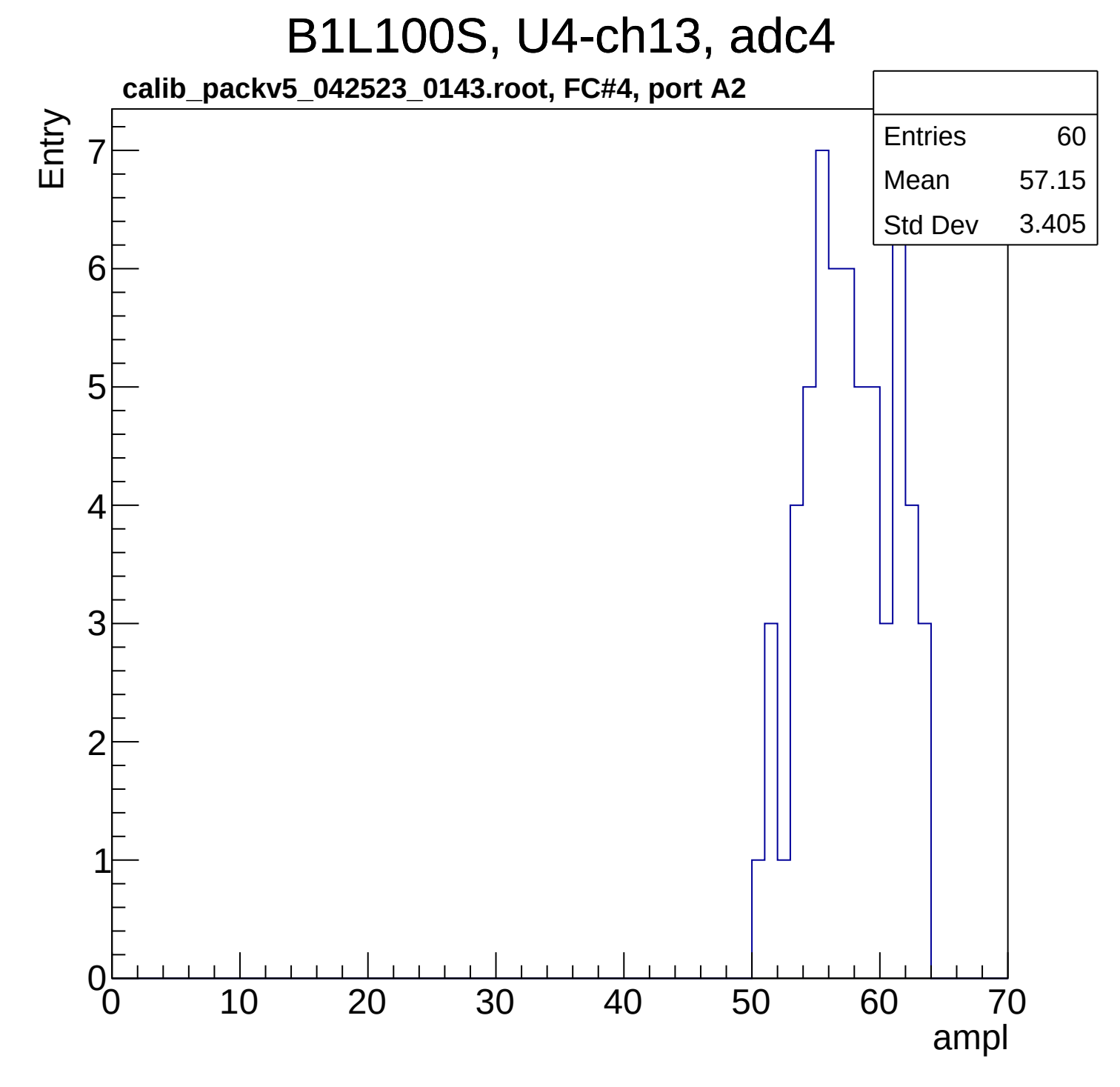

B1L100S, U4-ch12, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

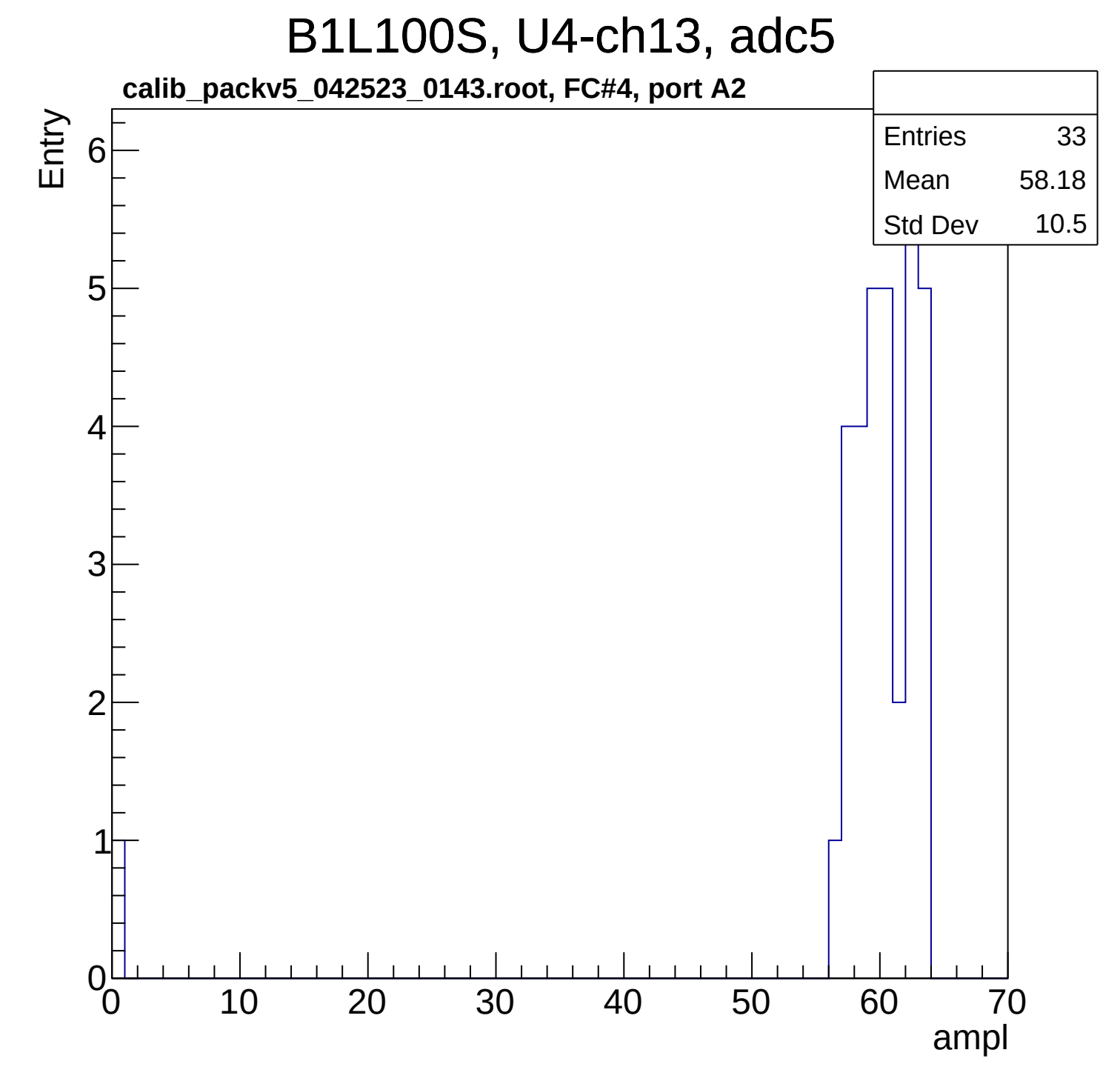

B1L100S, U4-ch13, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 29.29
Std Dev 4.946
Gaus mean : 29.7331
Gaus Width: 4.0144
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

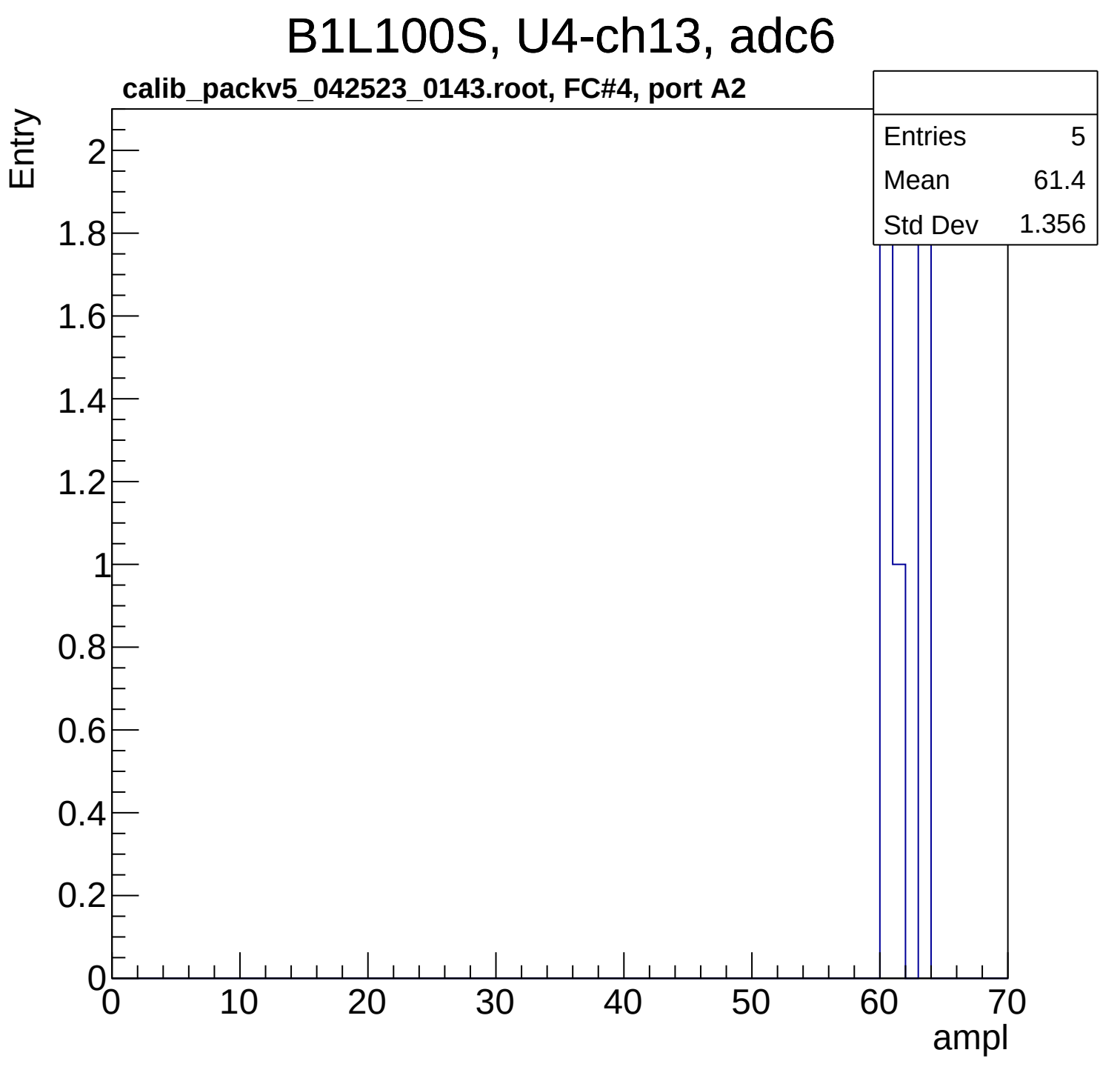

B1L100S, U4-ch13, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 36.21
Std Dev 2.975
Gaus mean : 36.6736
Gaus Width: 2.9240
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

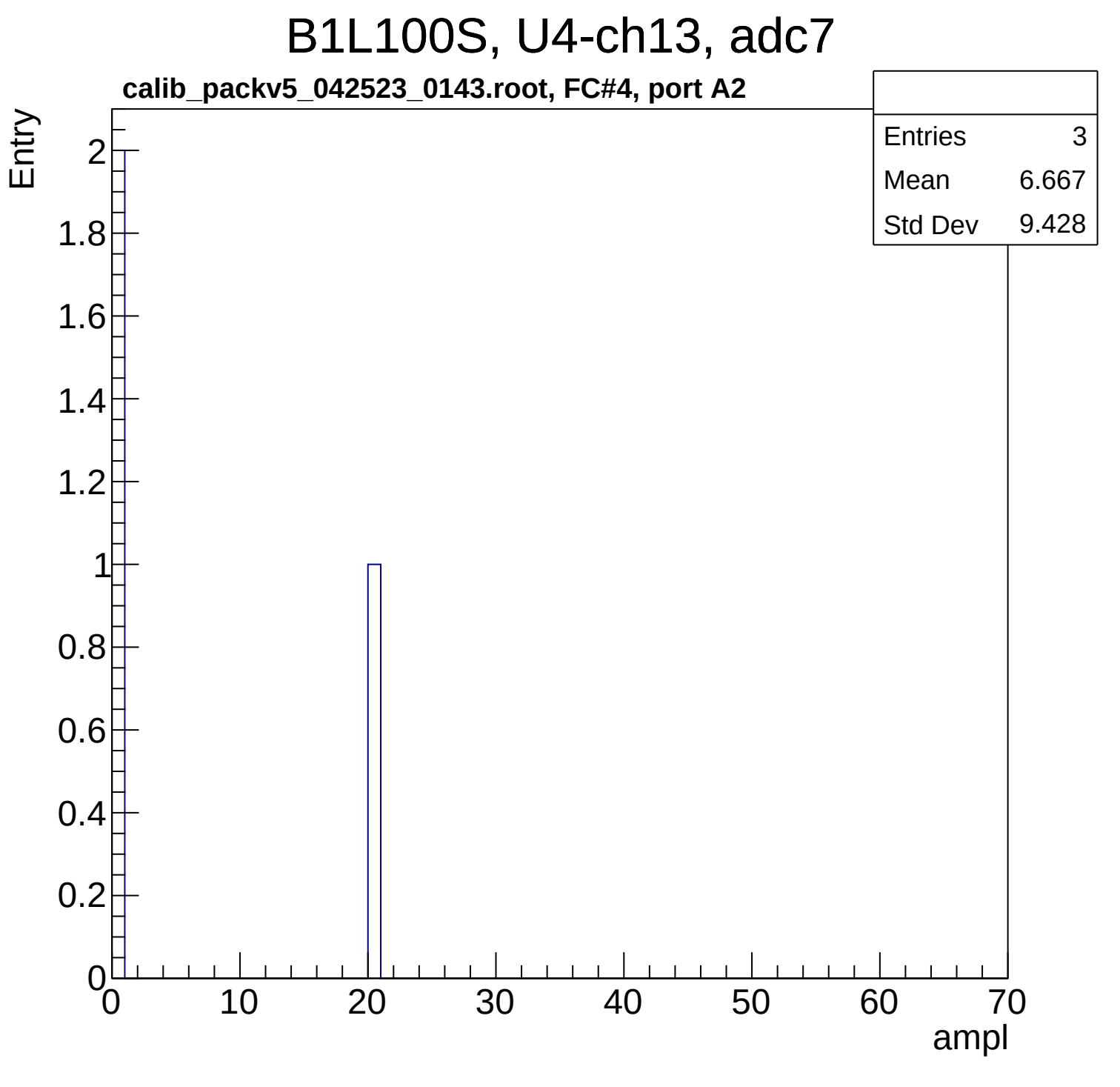

B1L100S, U4-ch13, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 43.34
Std Dev 3.363
Gaus mean : 44.6258
Gaus Width: 3.8505
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

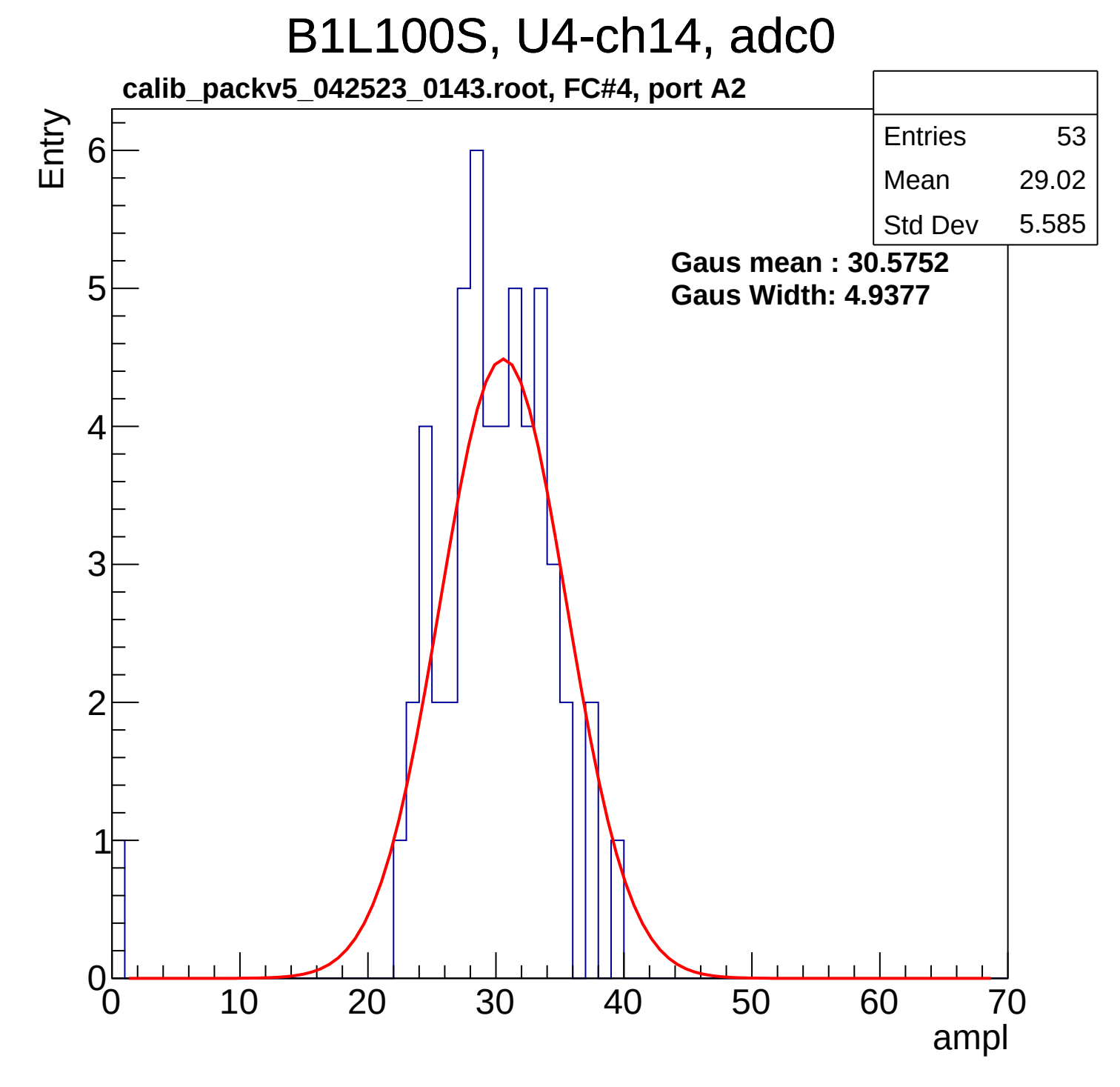

B1L100S, U4-ch13, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 50.15
Std Dev 3.349
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

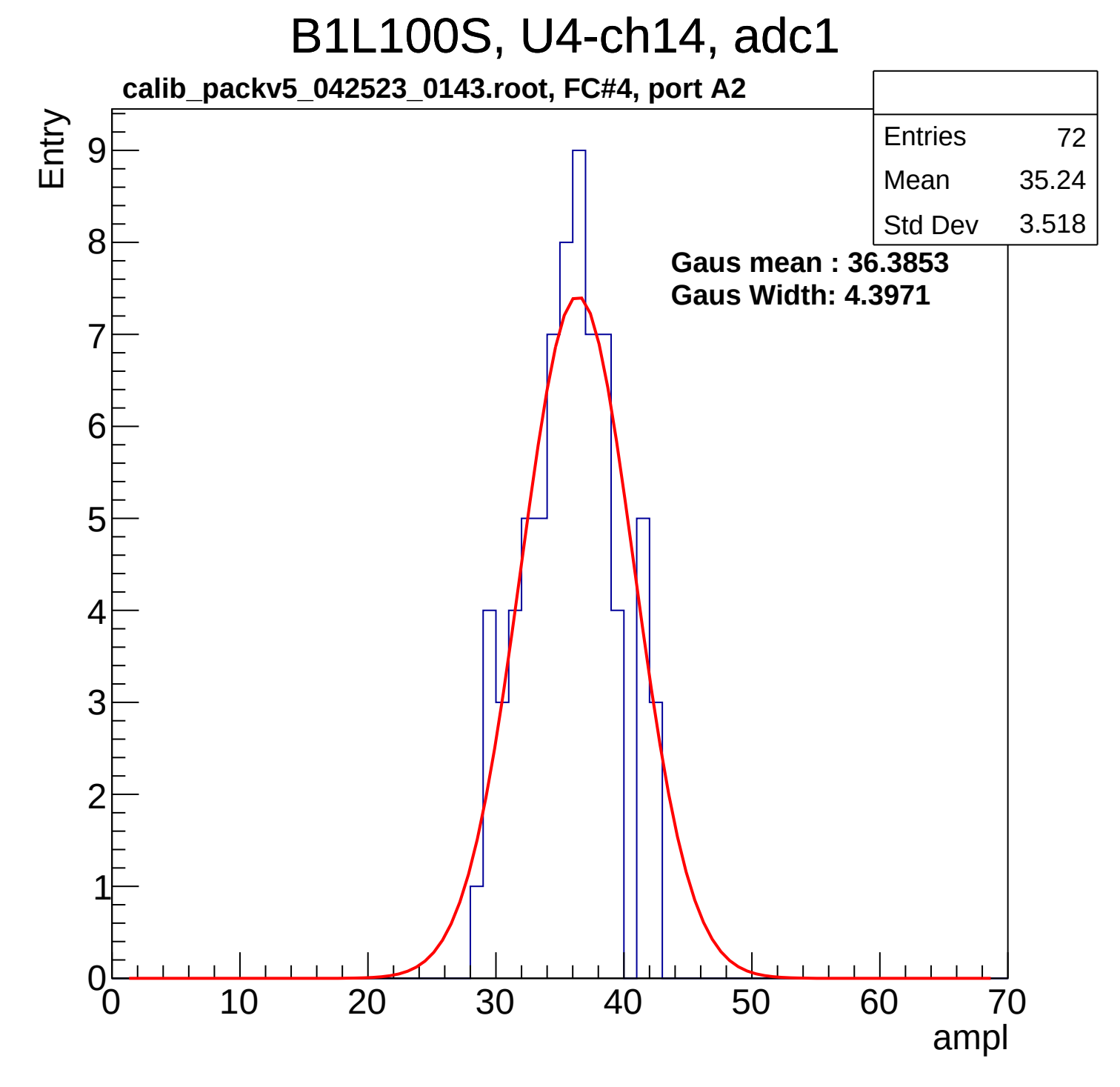

B1L100S, U4-ch13, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 57.15
Std Dev 3.405
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

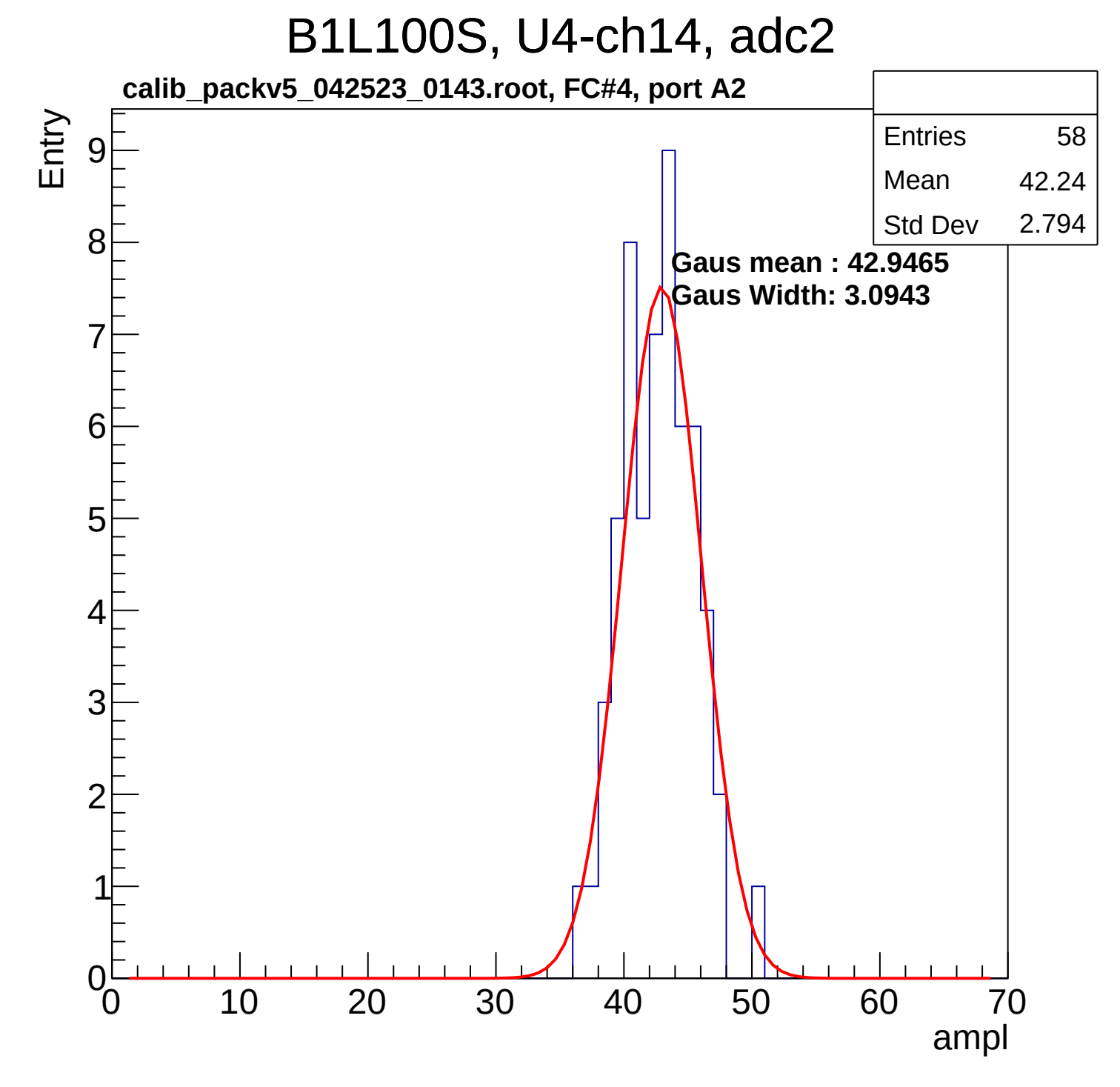

B1L100S, U4-ch13, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 33
Mean 58.18
Std Dev 10.5
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

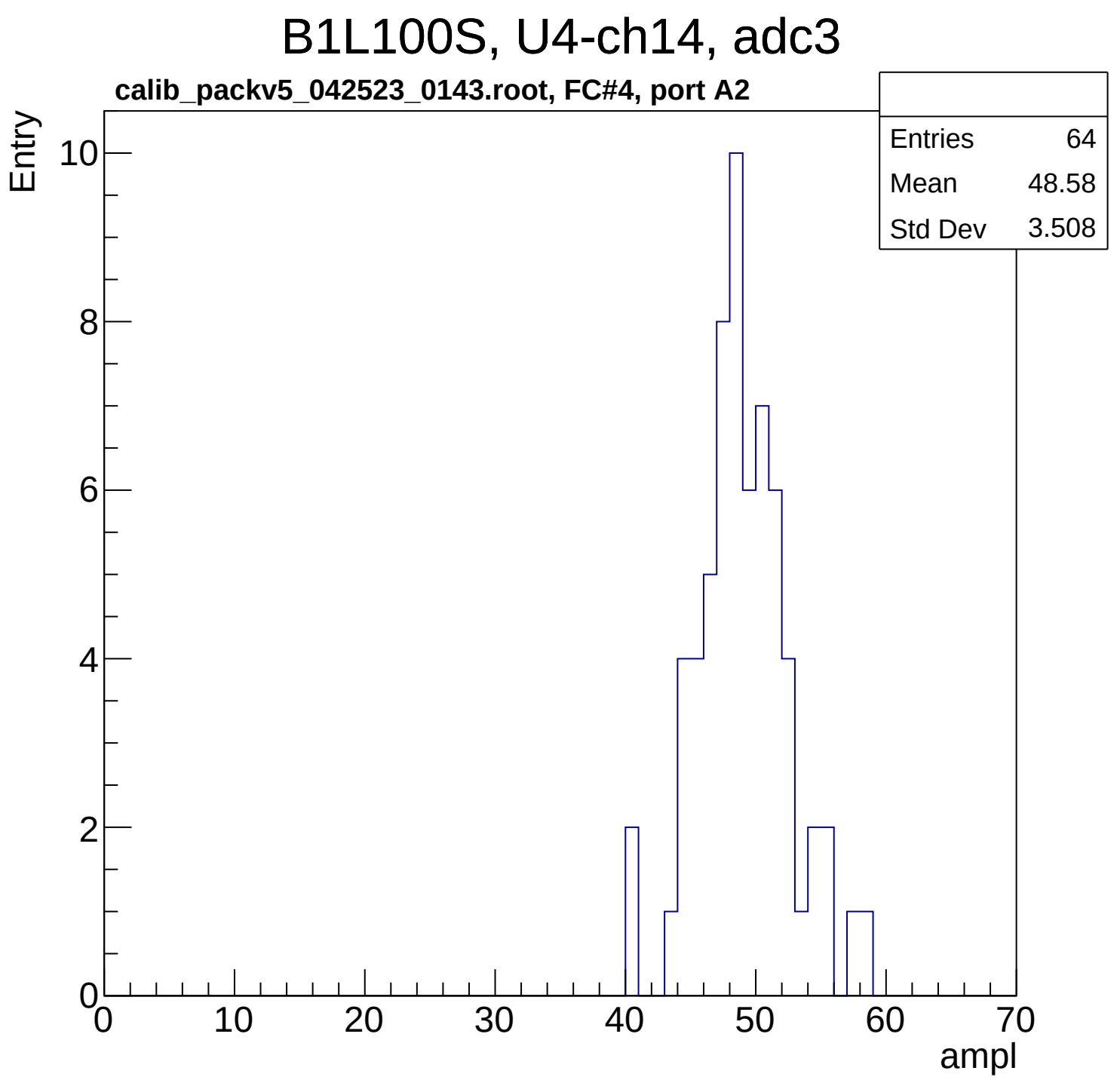

B1L100S, U4-ch13, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 5
Mean 61.4
Std Dev 1.356
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

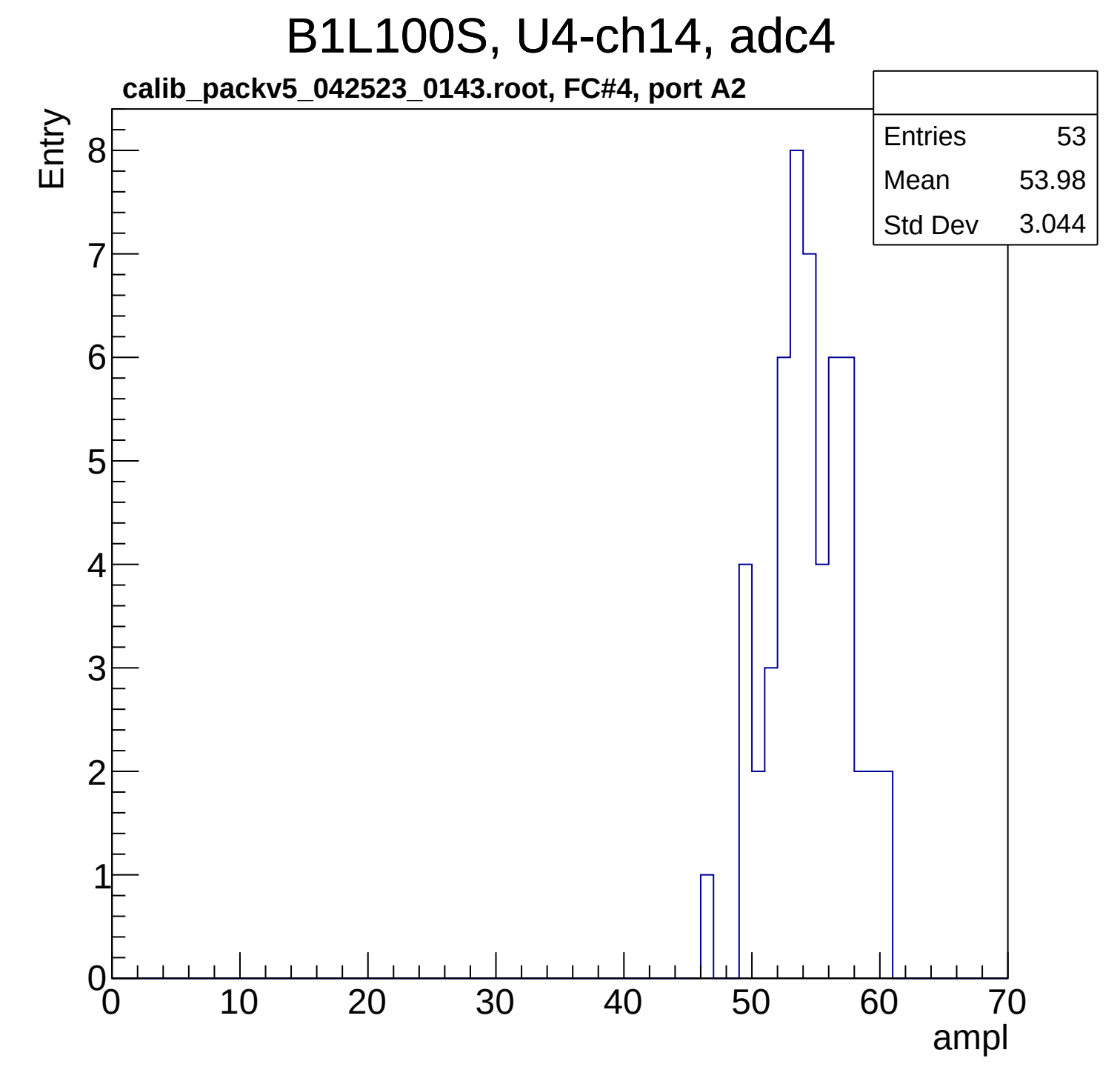

B1L100S, U4-ch13, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 6.667
Std Dev 9.428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

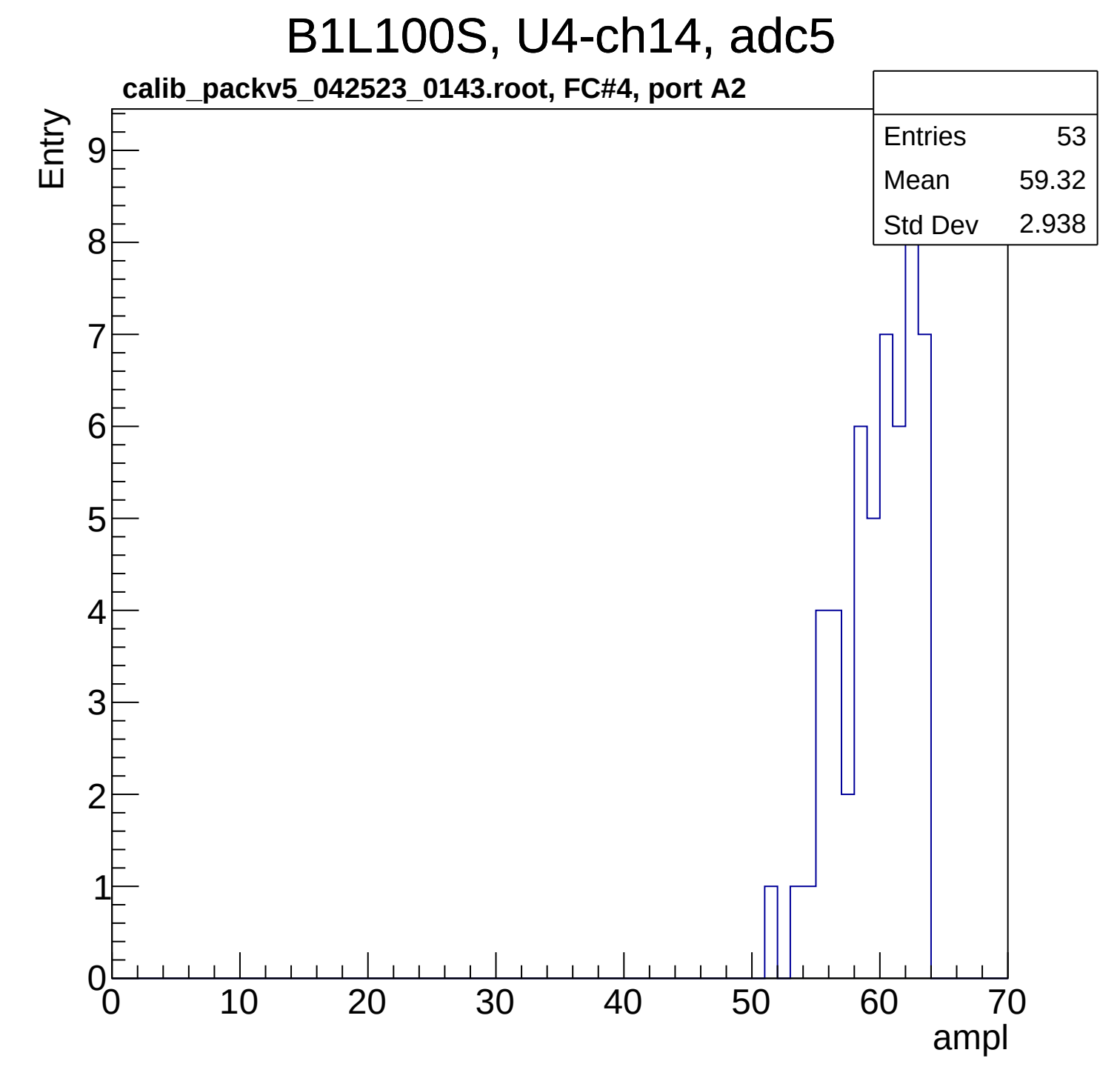

B1L100S, U4-ch14, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 29.02
Std Dev 5.585
Gaus mean : 30.5752
Gaus Width: 4.9377
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

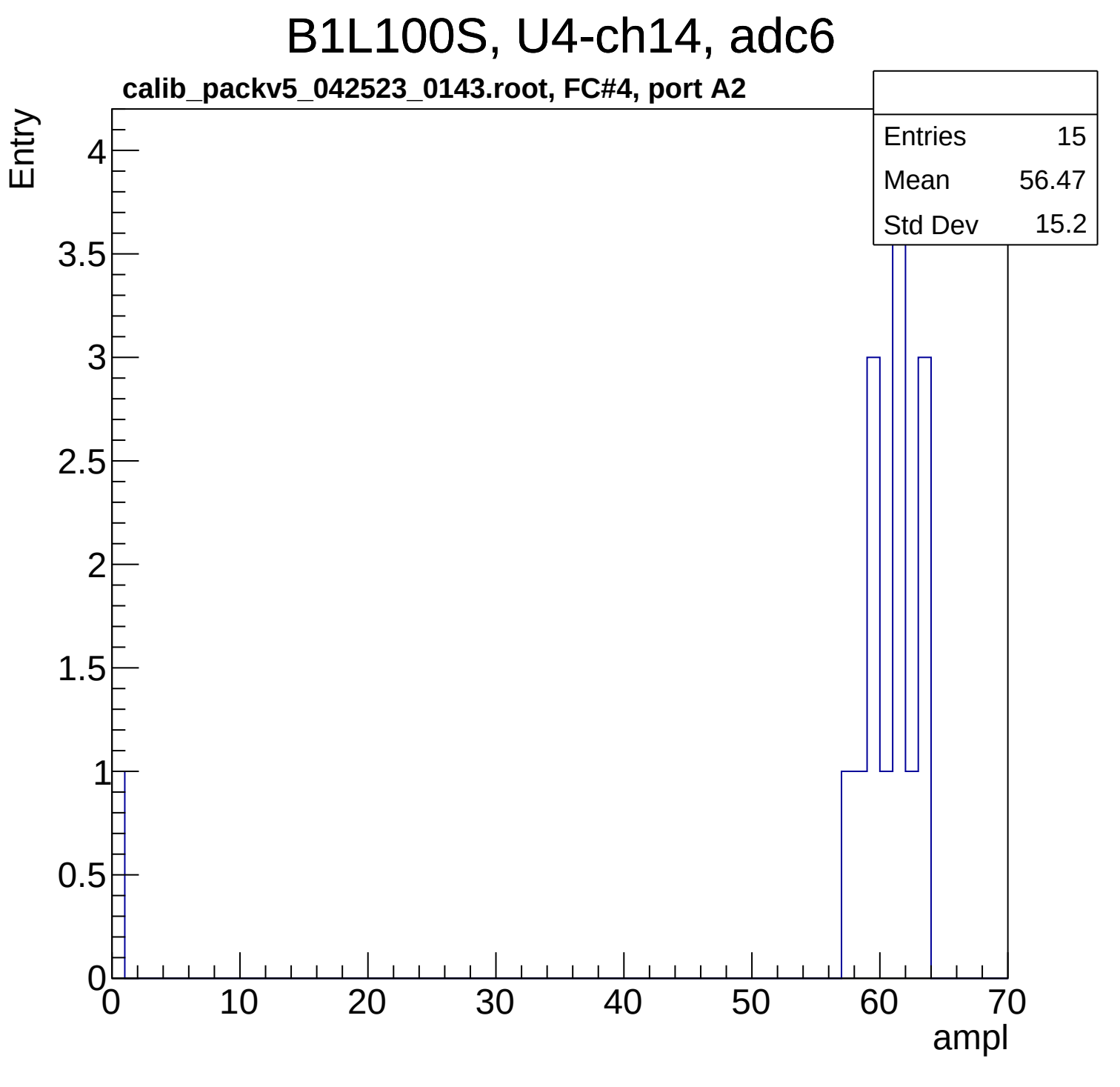

B1L100S, U4-ch14, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 35.24
Std Dev 3.518
Gaus mean : 36.3853
Gaus Width: 4.3971
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

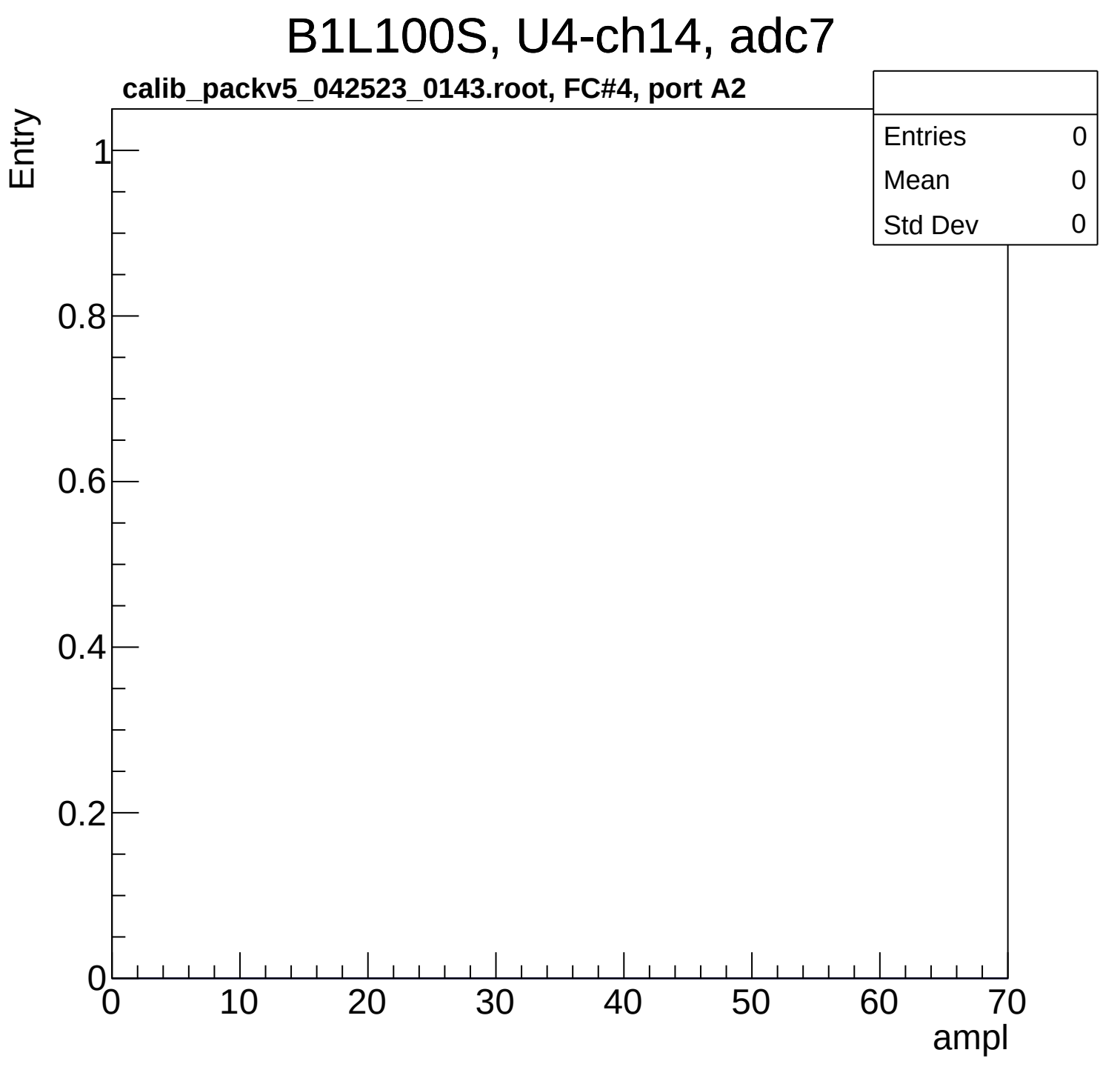

B1L100S, U4-ch14, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 42.24
Std Dev 2.794
Gaus mean : 42.9465
Gaus Width: 3.0943
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

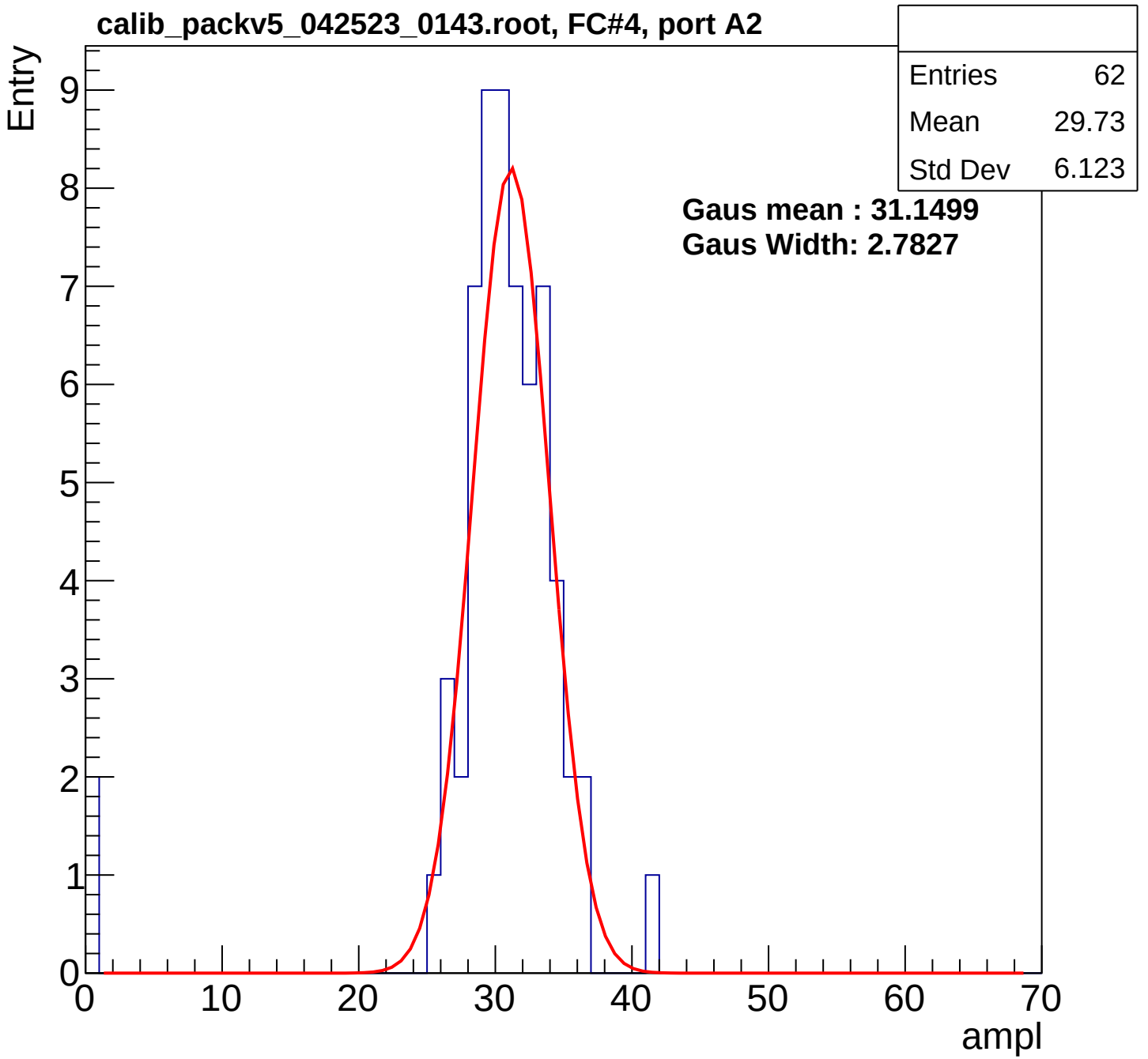

B1L100S, U4-ch14, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 48.58
Std Dev 3.508
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

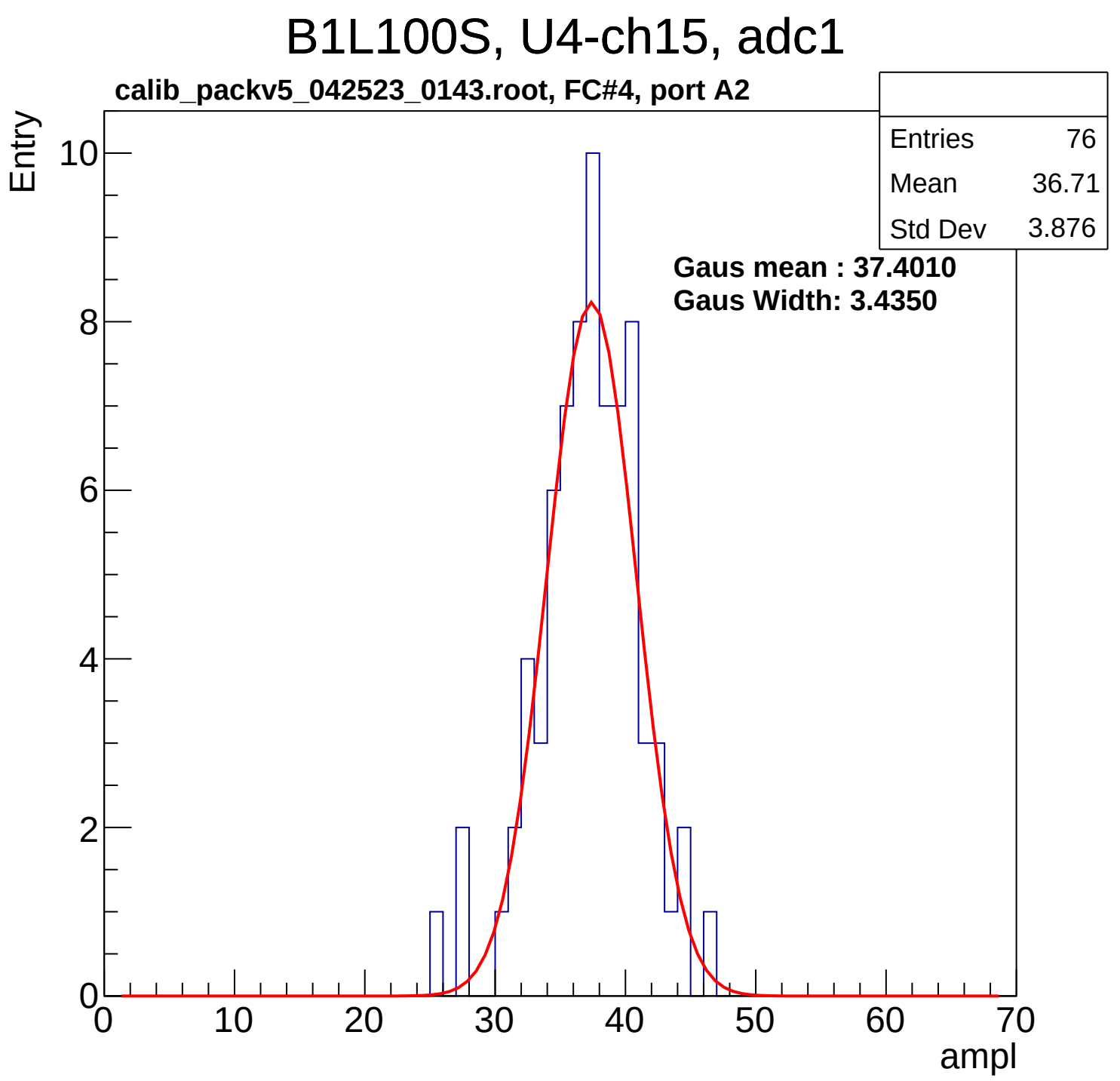

B1L100S, U4-ch14, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 53.98
Std Dev 3.044
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

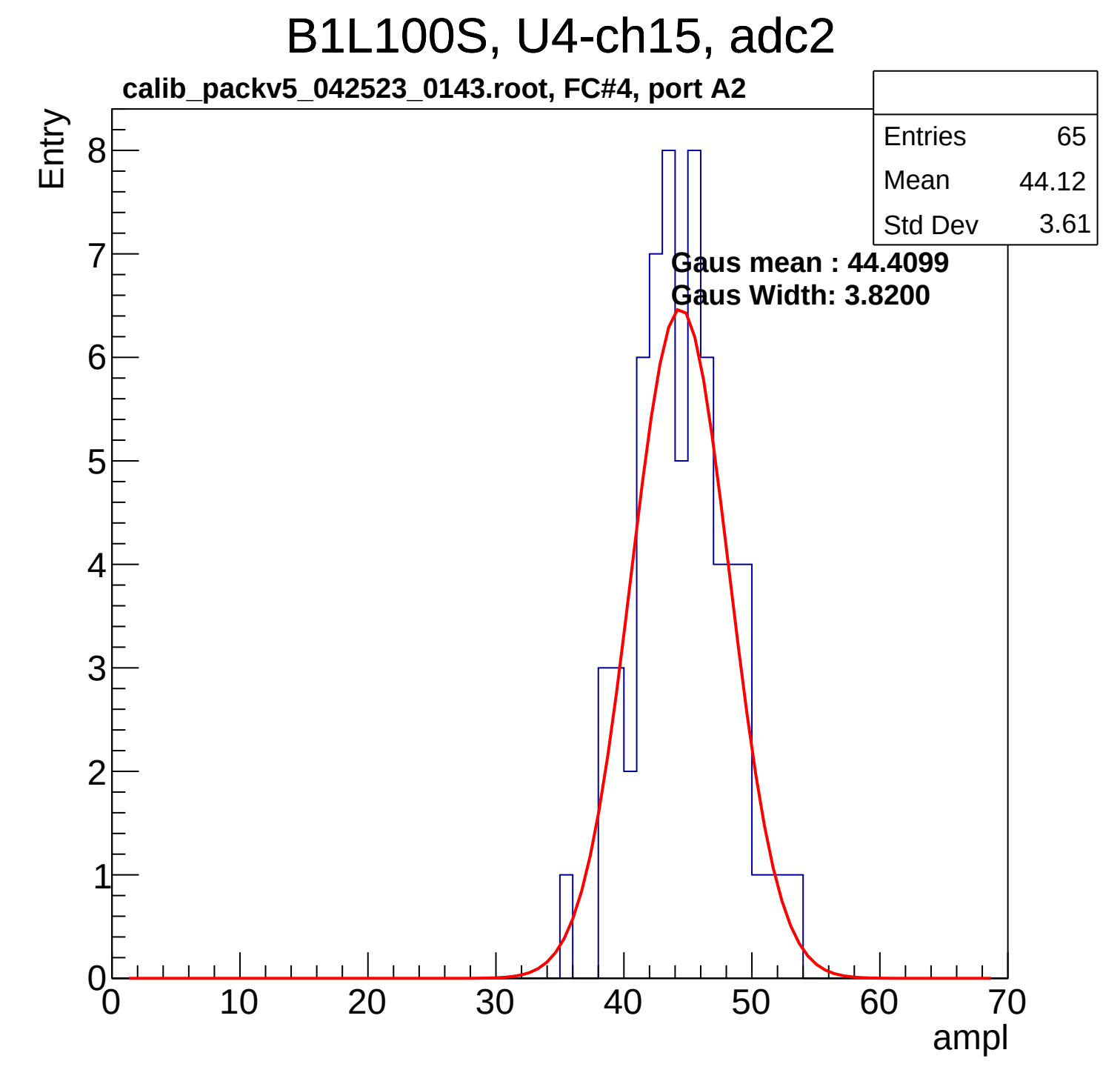

B1L100S, U4-ch14, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 59.32
Std Dev 2.938
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

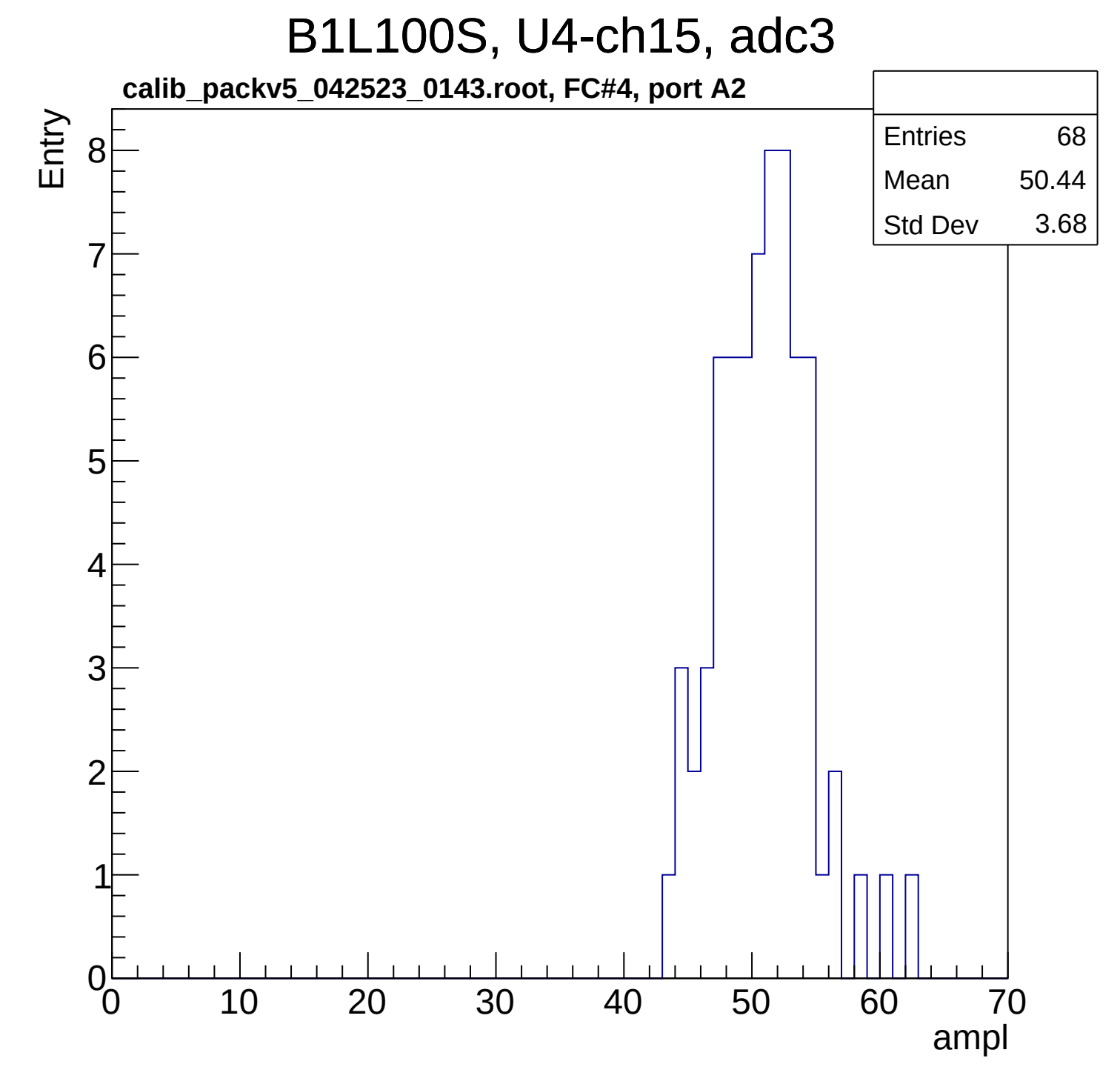

B1L100S, U4-ch14, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 15
Mean 56.47
Std Dev 15.2
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

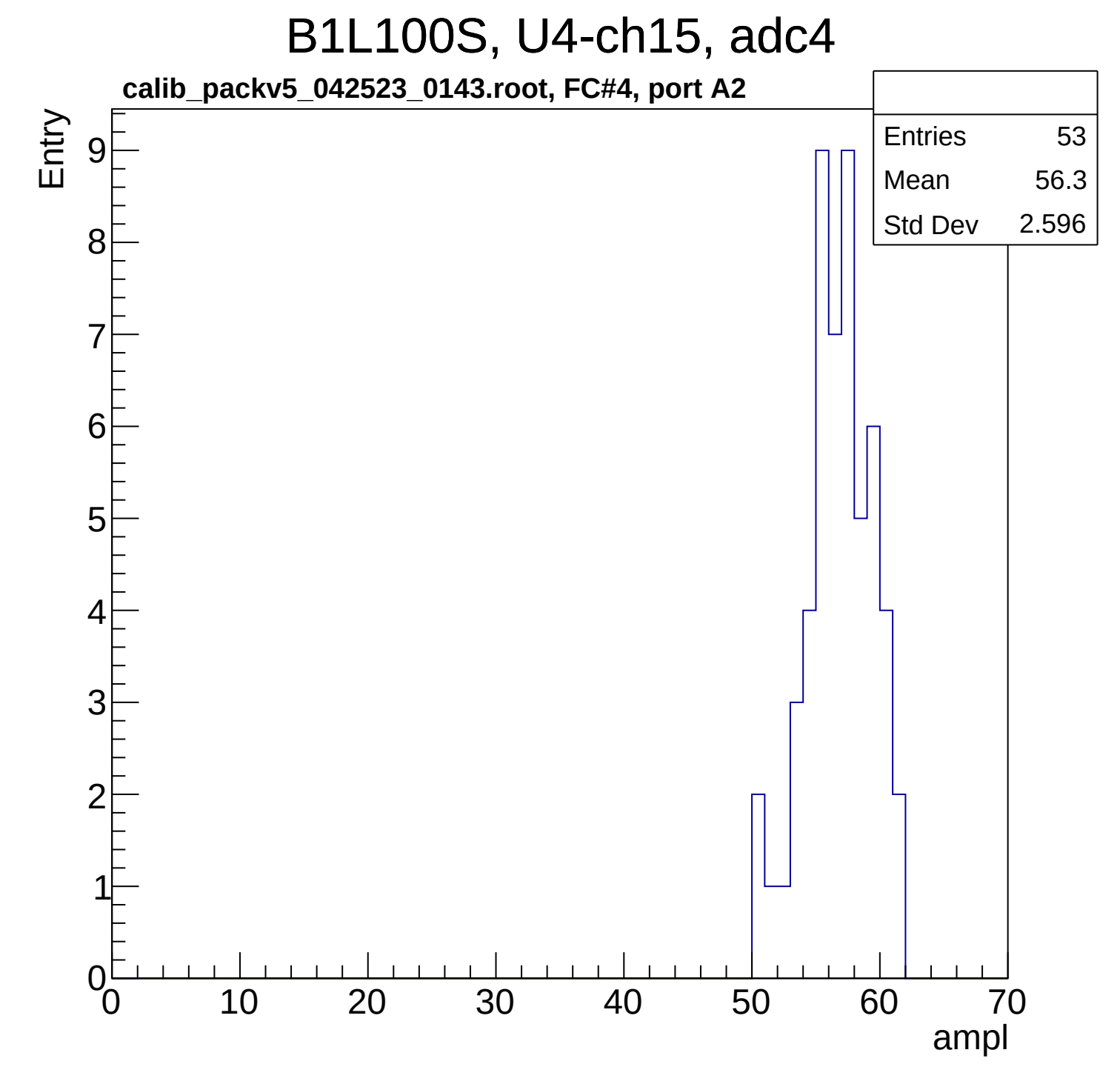

B1L100S, U4-ch14, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

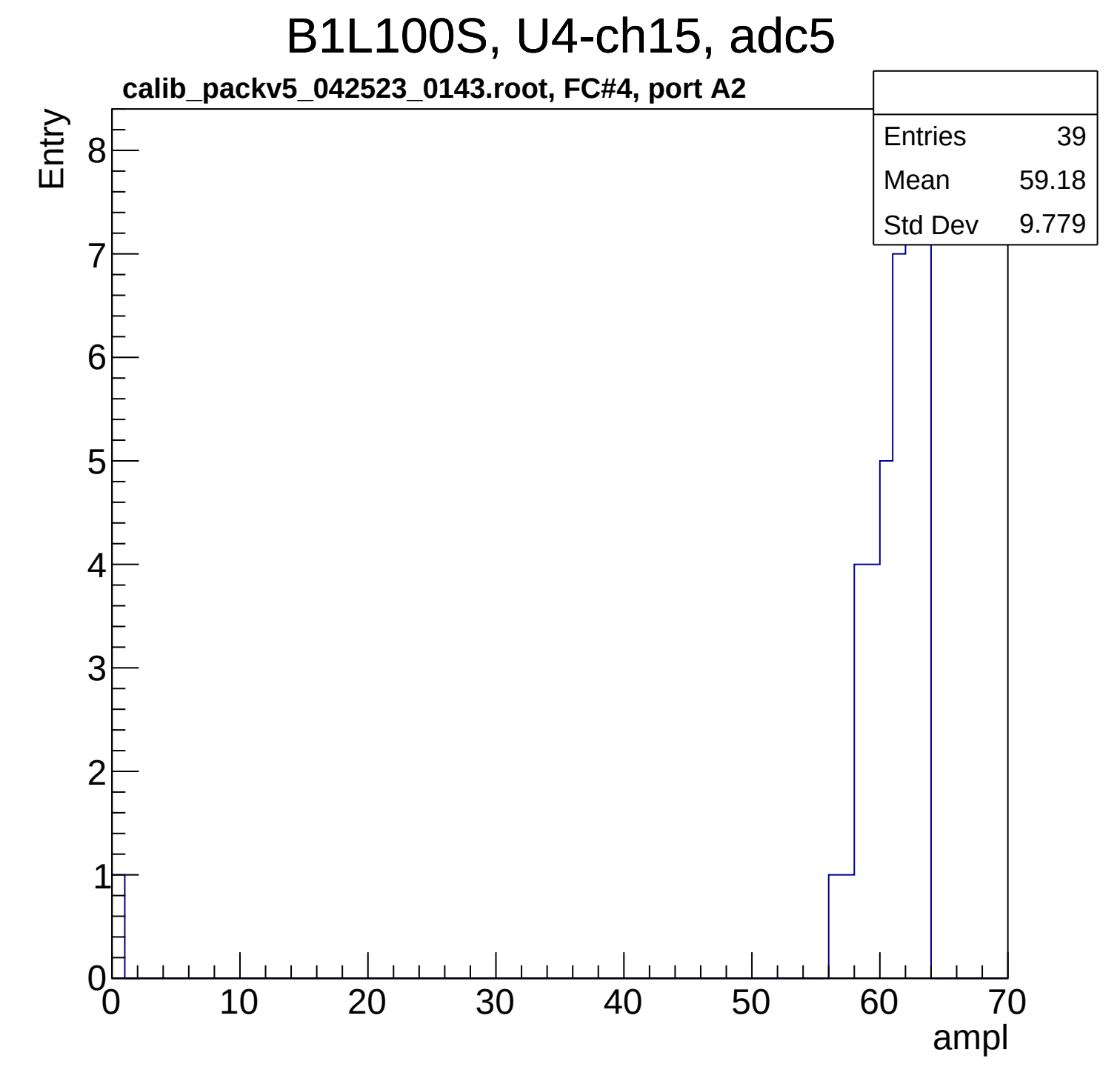

B1L100S, U4-ch15, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 29.73
Std Dev 6.123
Gaus mean : 31.1499
Gaus Width: 2.7827
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

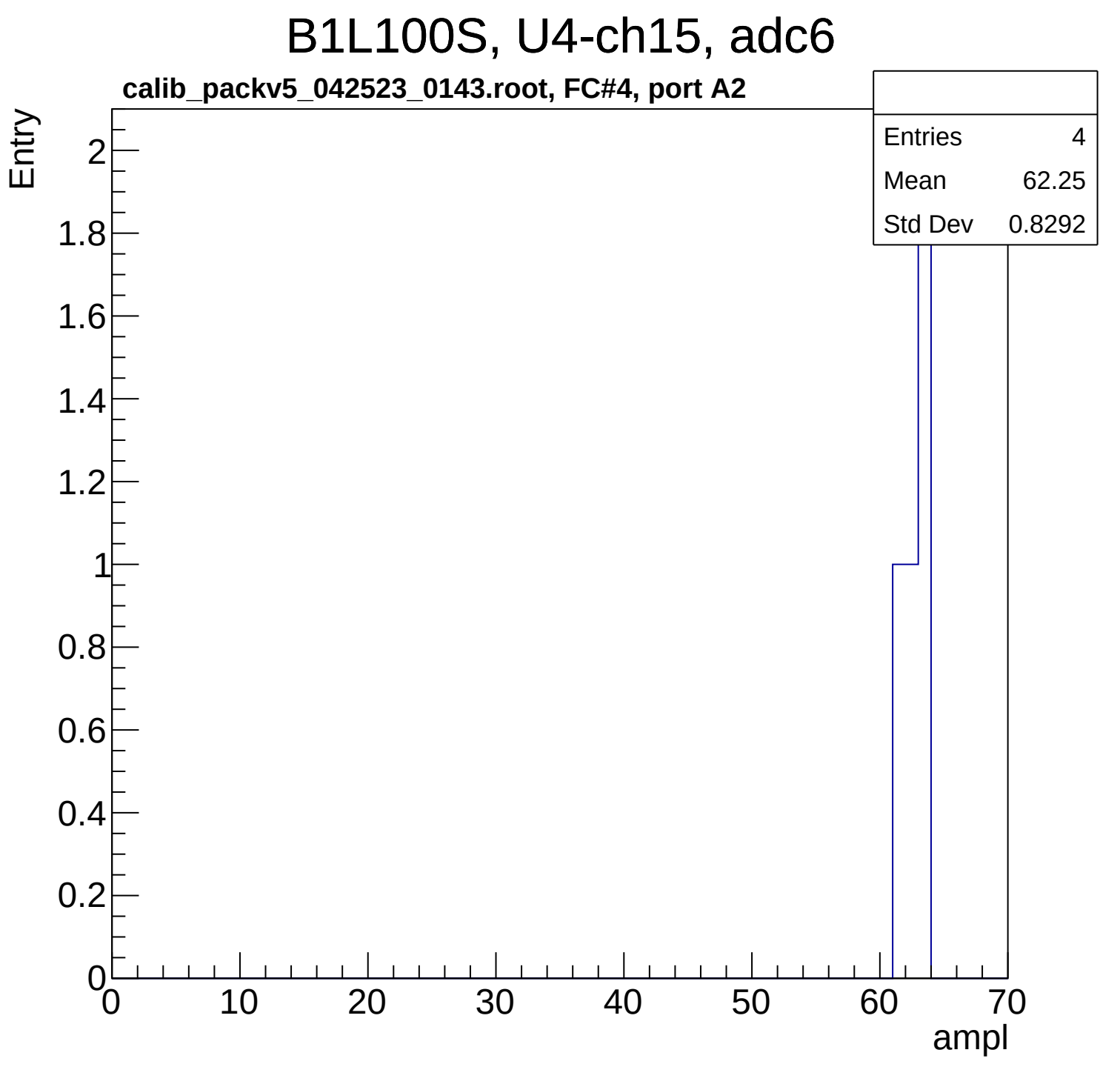

B1L100S, U4-ch15, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 36.71
Std Dev 3.876
Gaus mean : 37.4010
Gaus Width: 3.4350
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

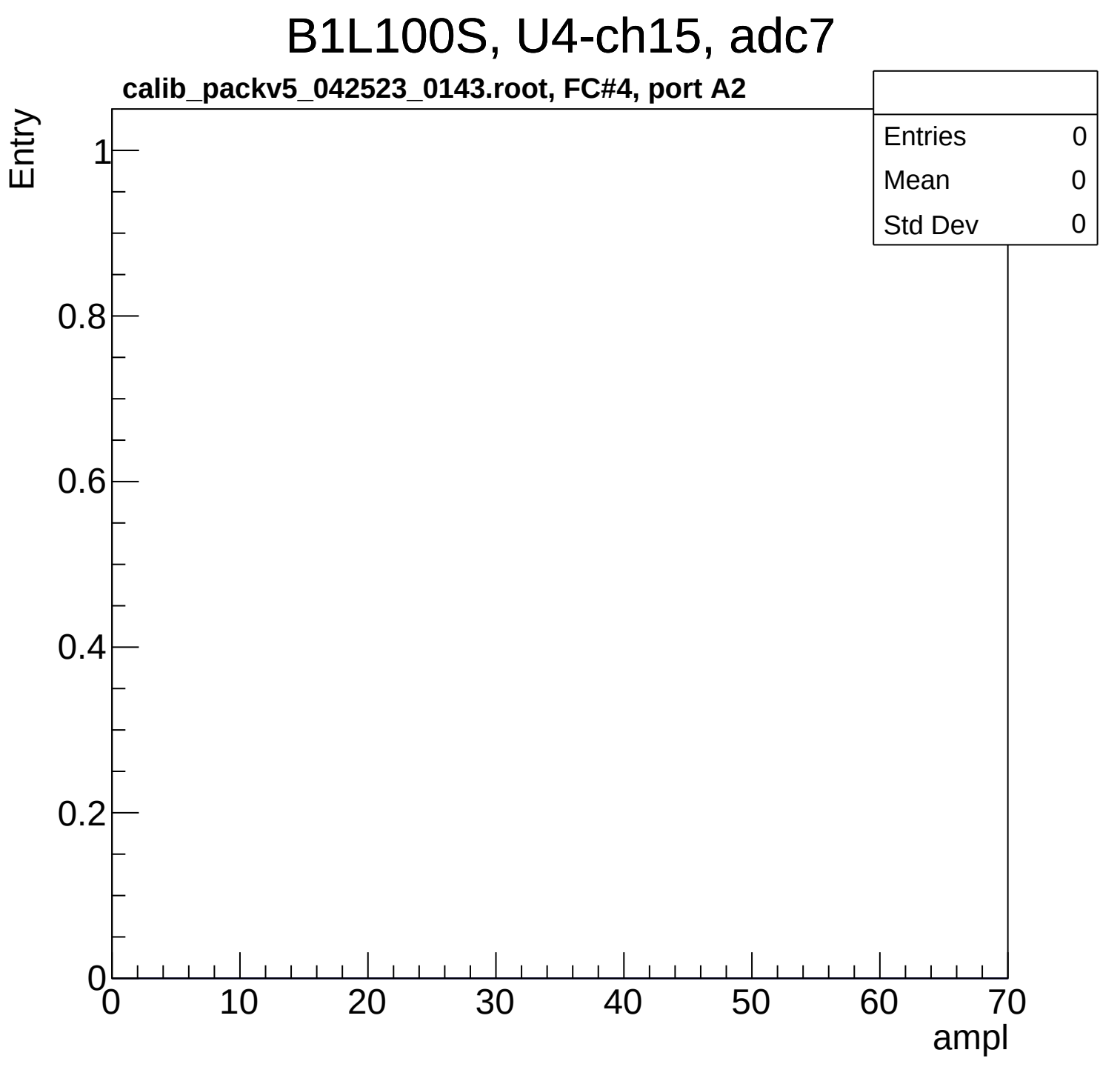

B1L100S, U4-ch15, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 44.12
Std Dev 3.61
Gaus mean : 44.4099
Gaus Width: 3.8200
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

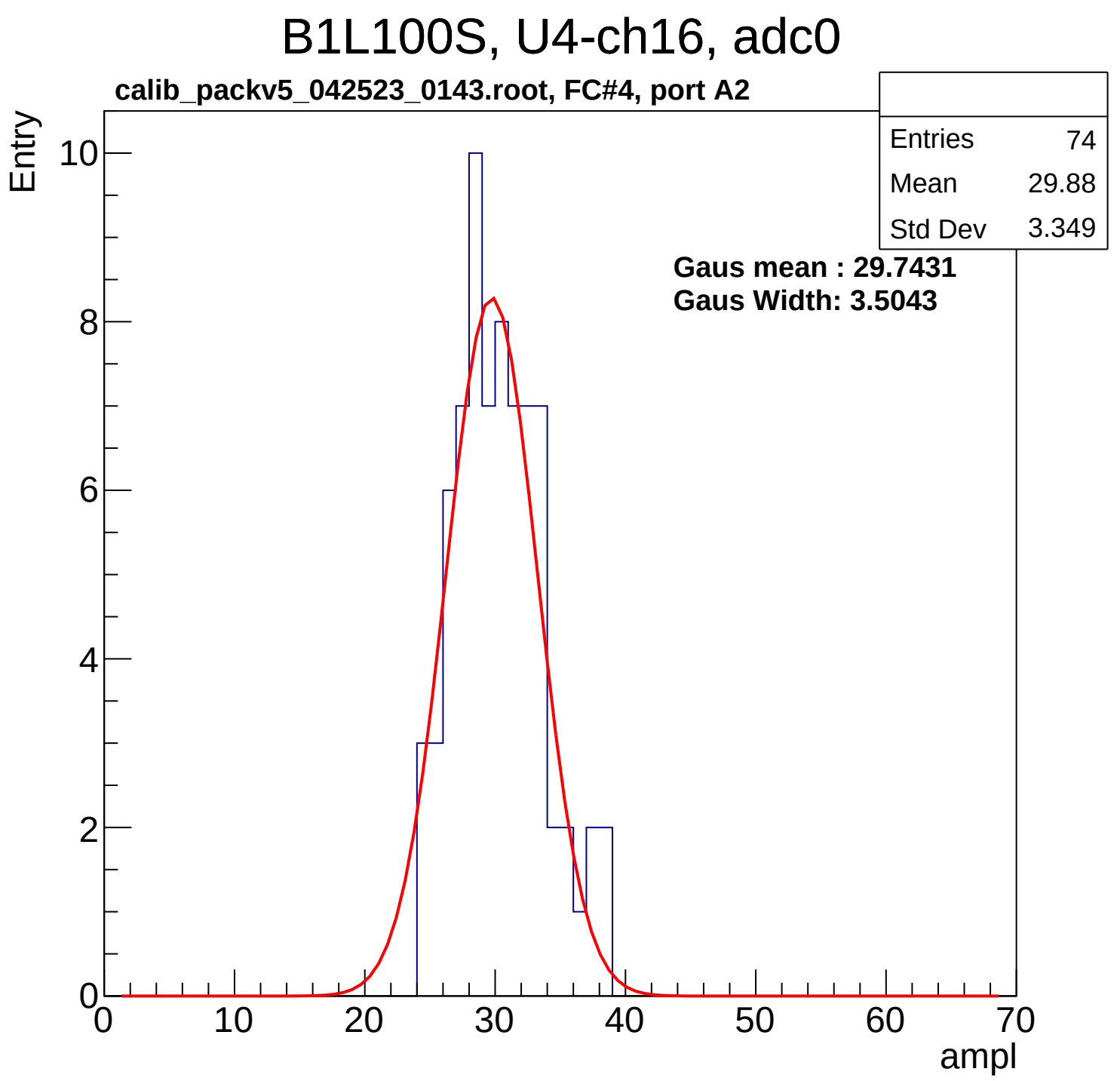

B1L100S, U4-ch15, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 50.44
Std Dev 3.68
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

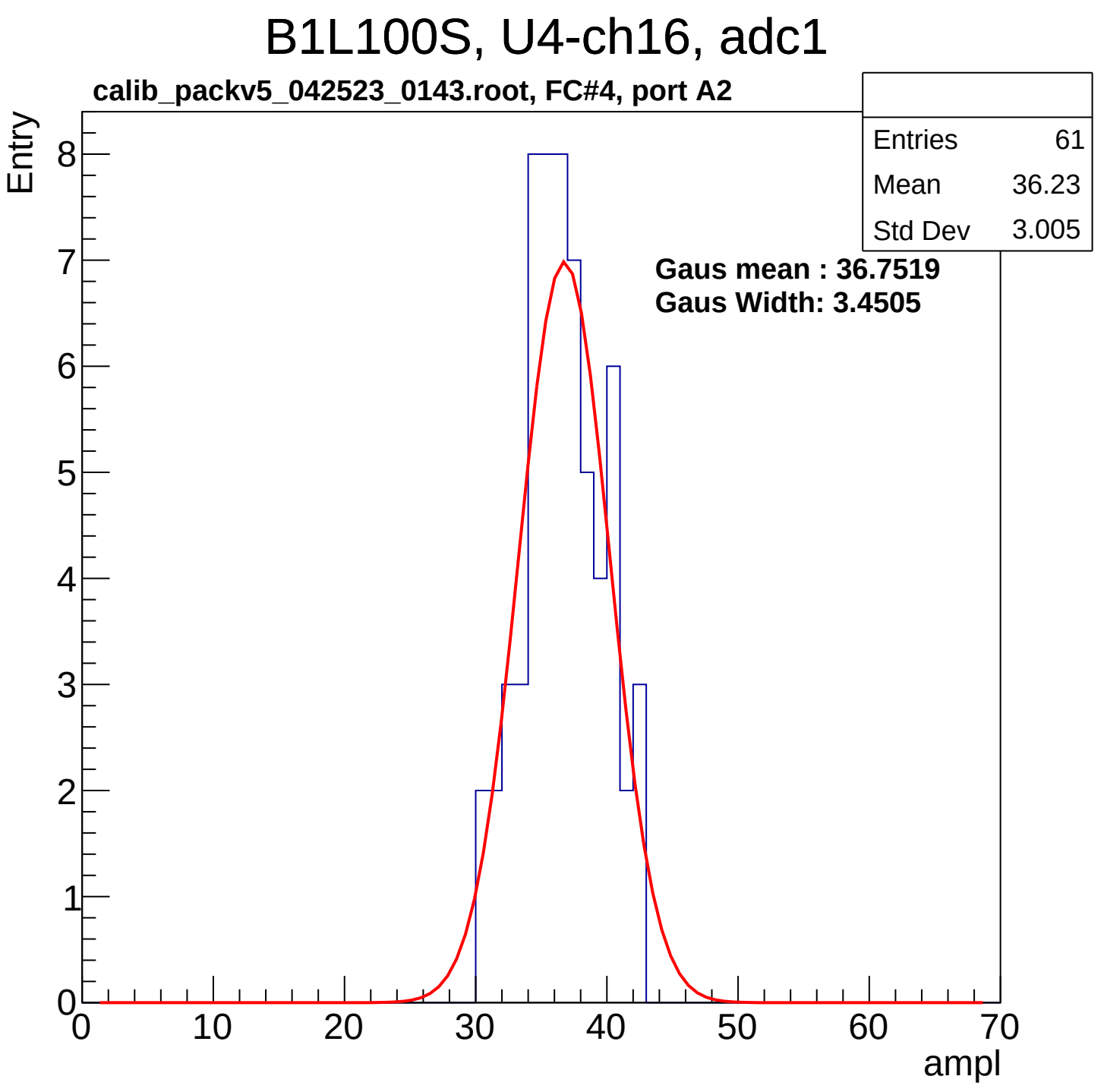

B1L100S, U4-ch15, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 56.3
Std Dev 2.596
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

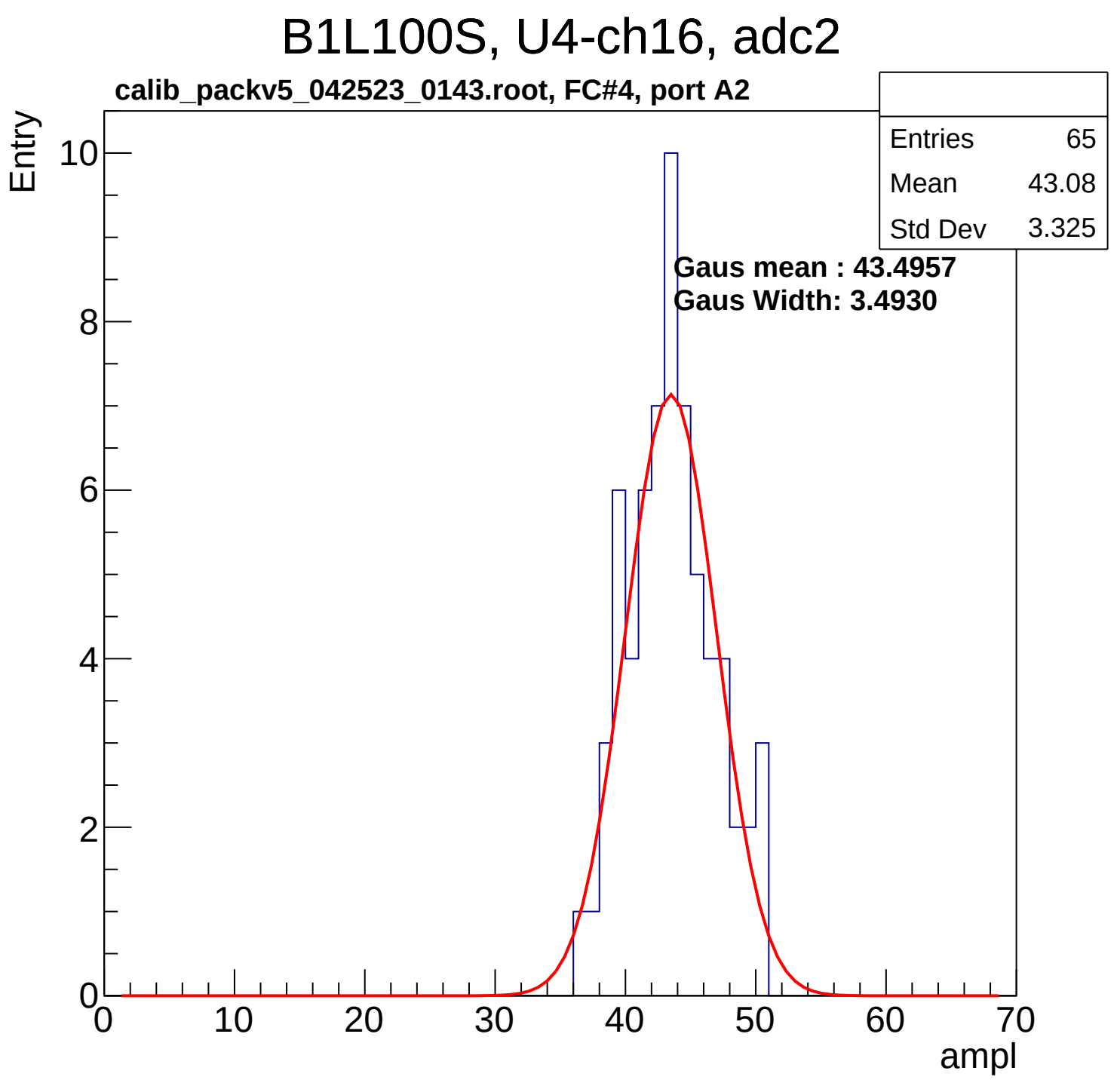

B1L100S, U4-ch15, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 39
Mean 59.18
Std Dev 9.779
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

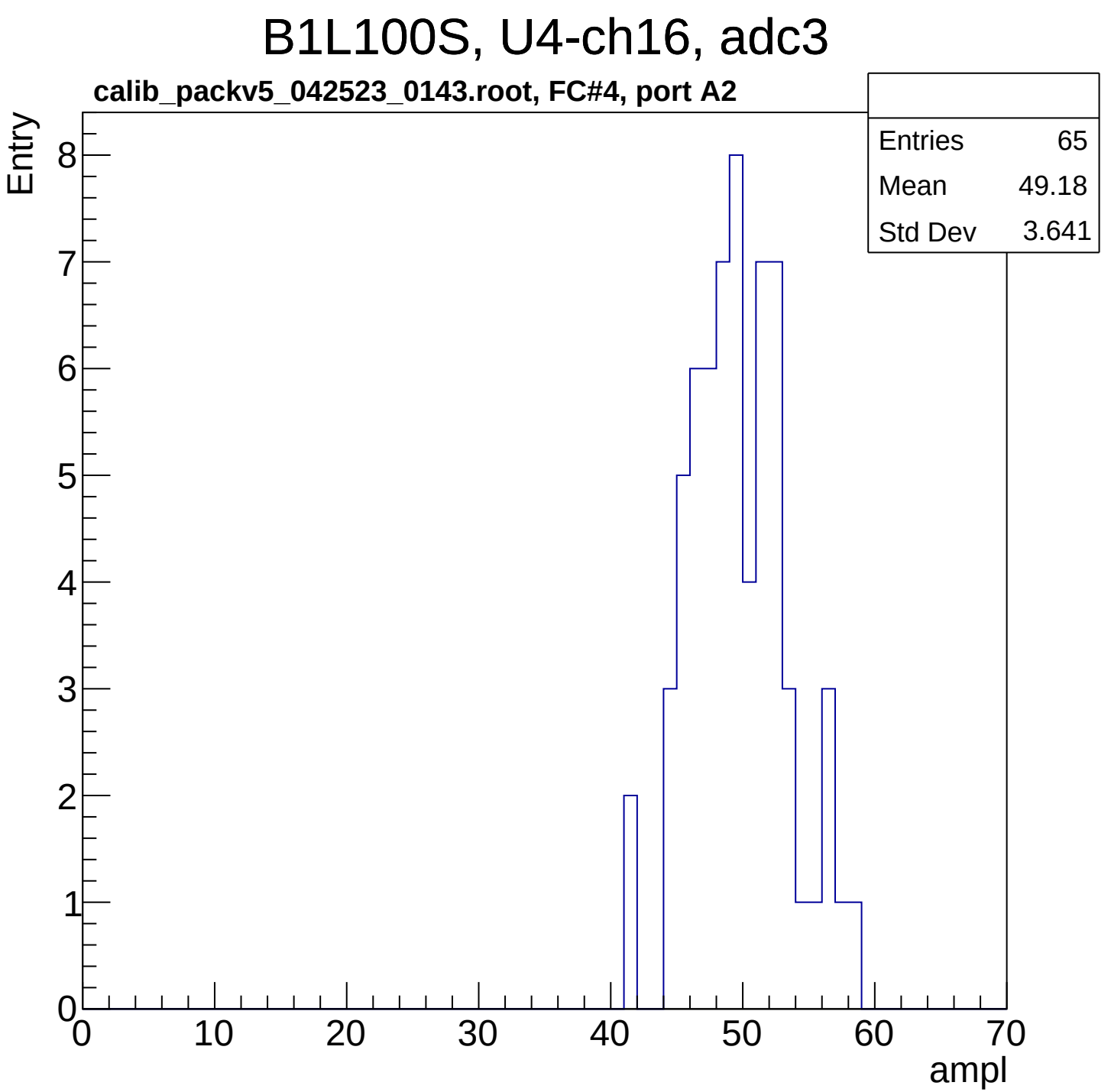

B1L100S, U4-ch15, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

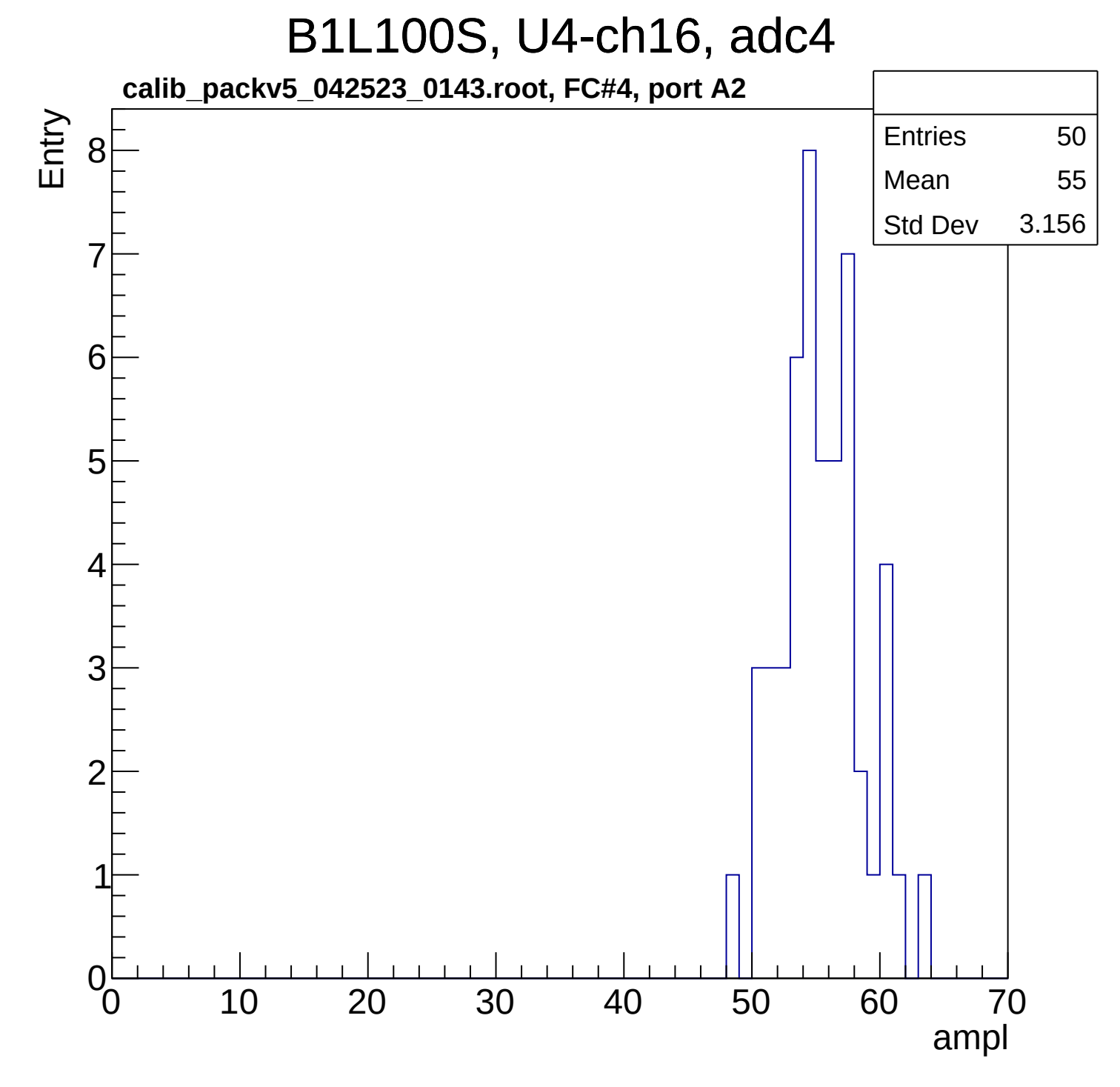

B1L100S, U4-ch15, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

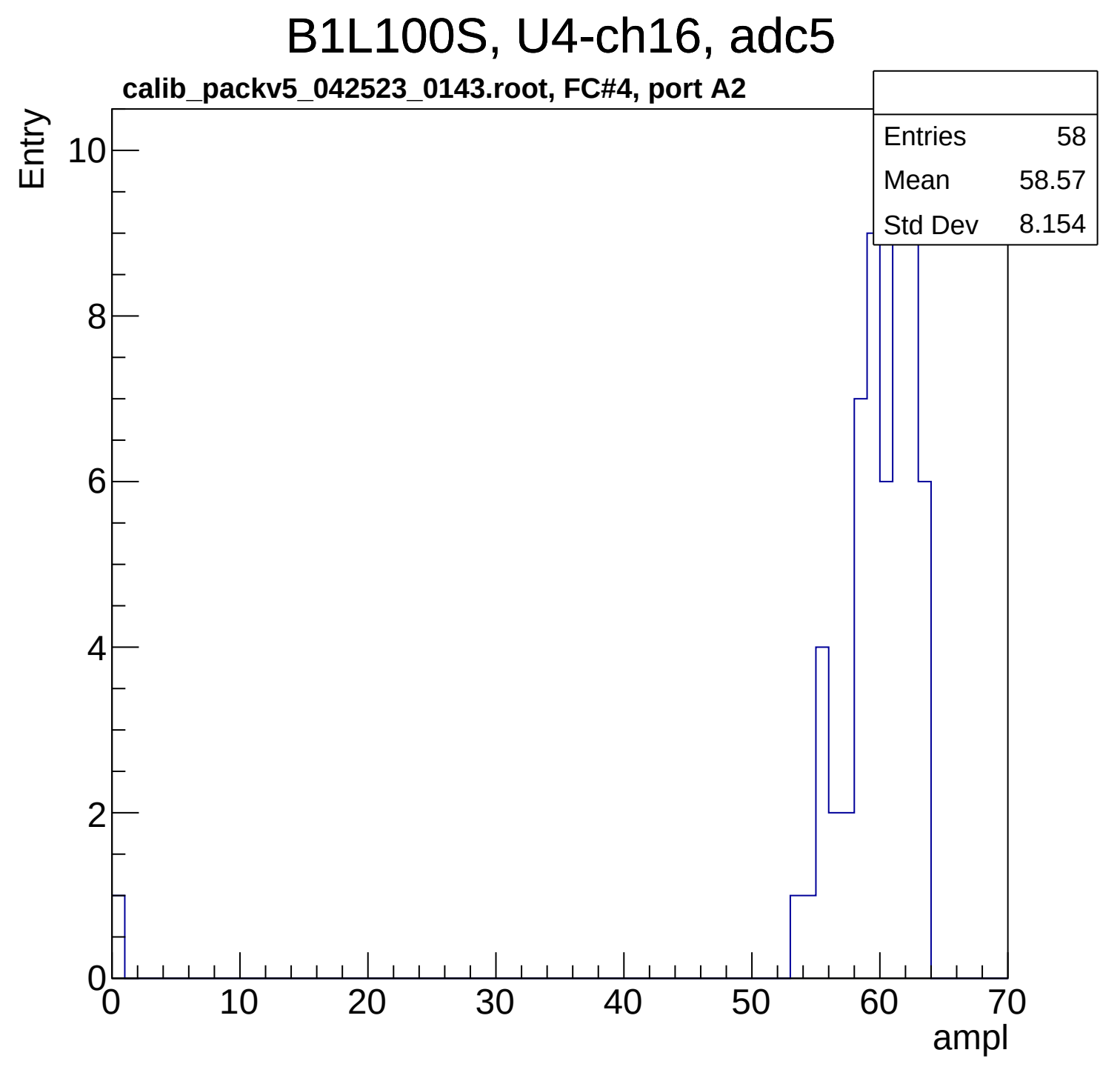

B1L100S, U4-ch16, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 29.88
Std Dev 3.349
Gaus mean : 29.7431
Gaus Width: 3.5043
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

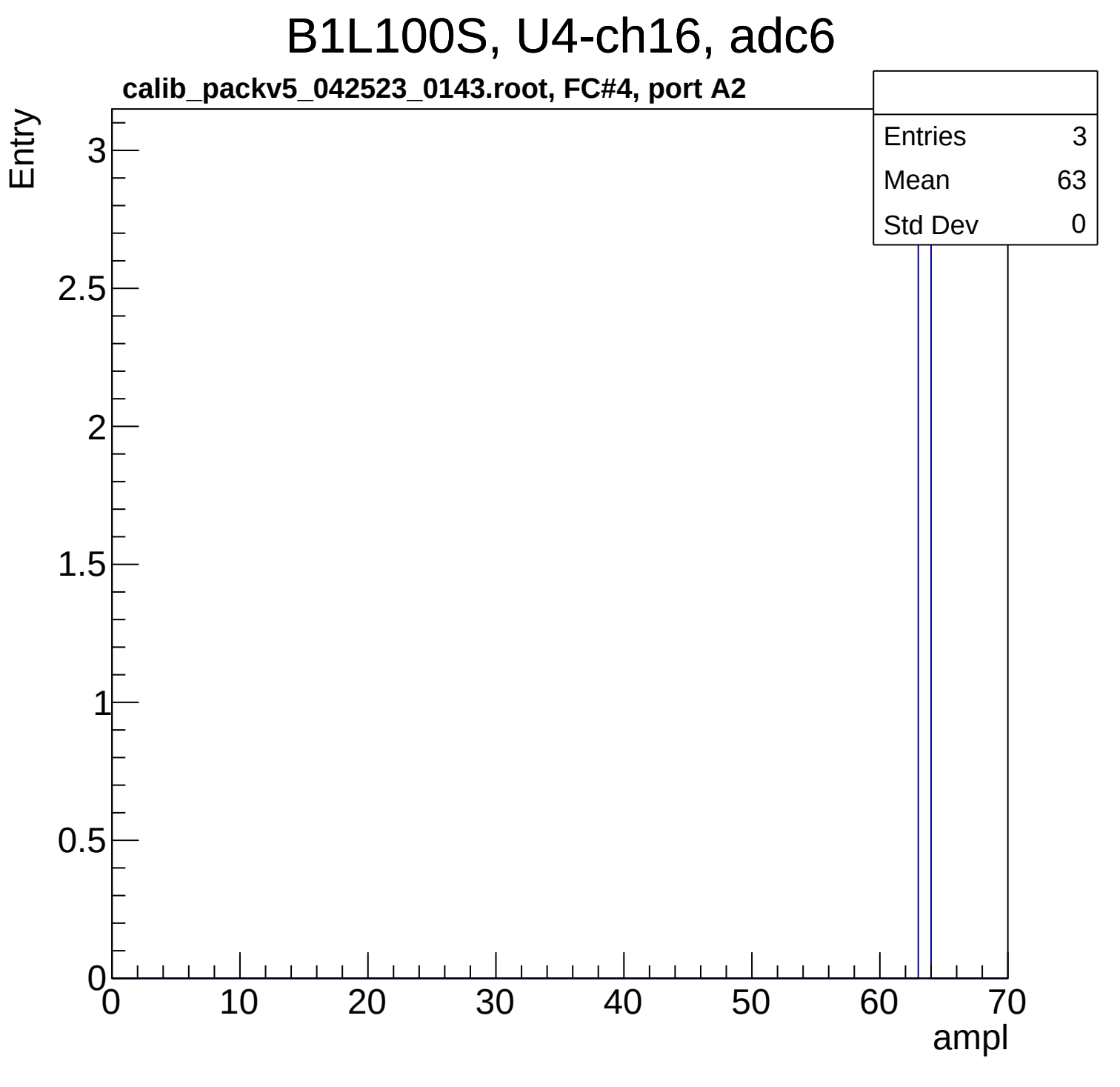

B1L100S, U4-ch16, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 36.23
Std Dev 3.005
Gaus mean : 36.7519
Gaus Width: 3.4505
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

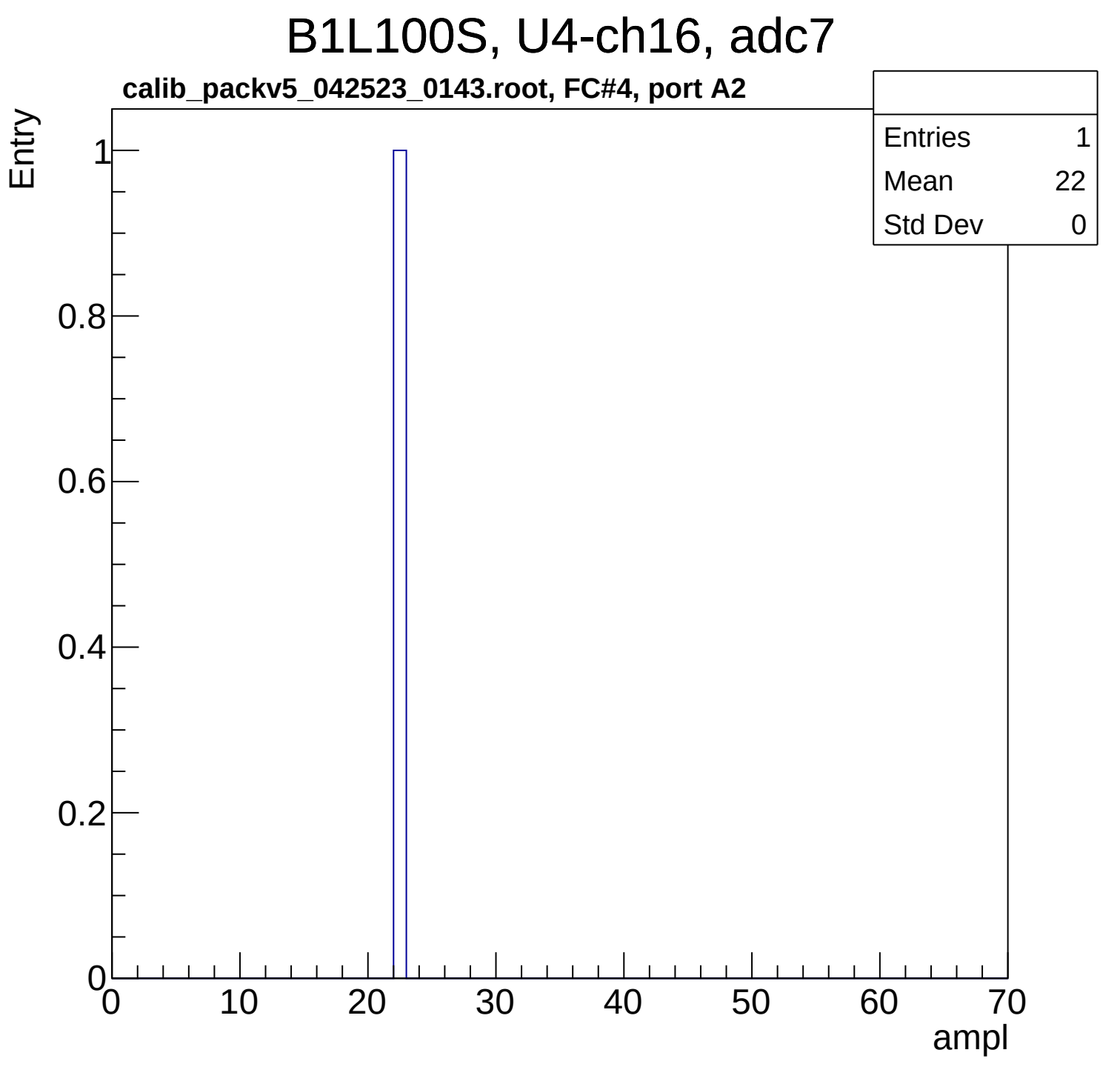

B1L100S, U4-ch16, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 43.08
Std Dev 3.325
Gaus mean : 43.4957
Gaus Width: 3.4930
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

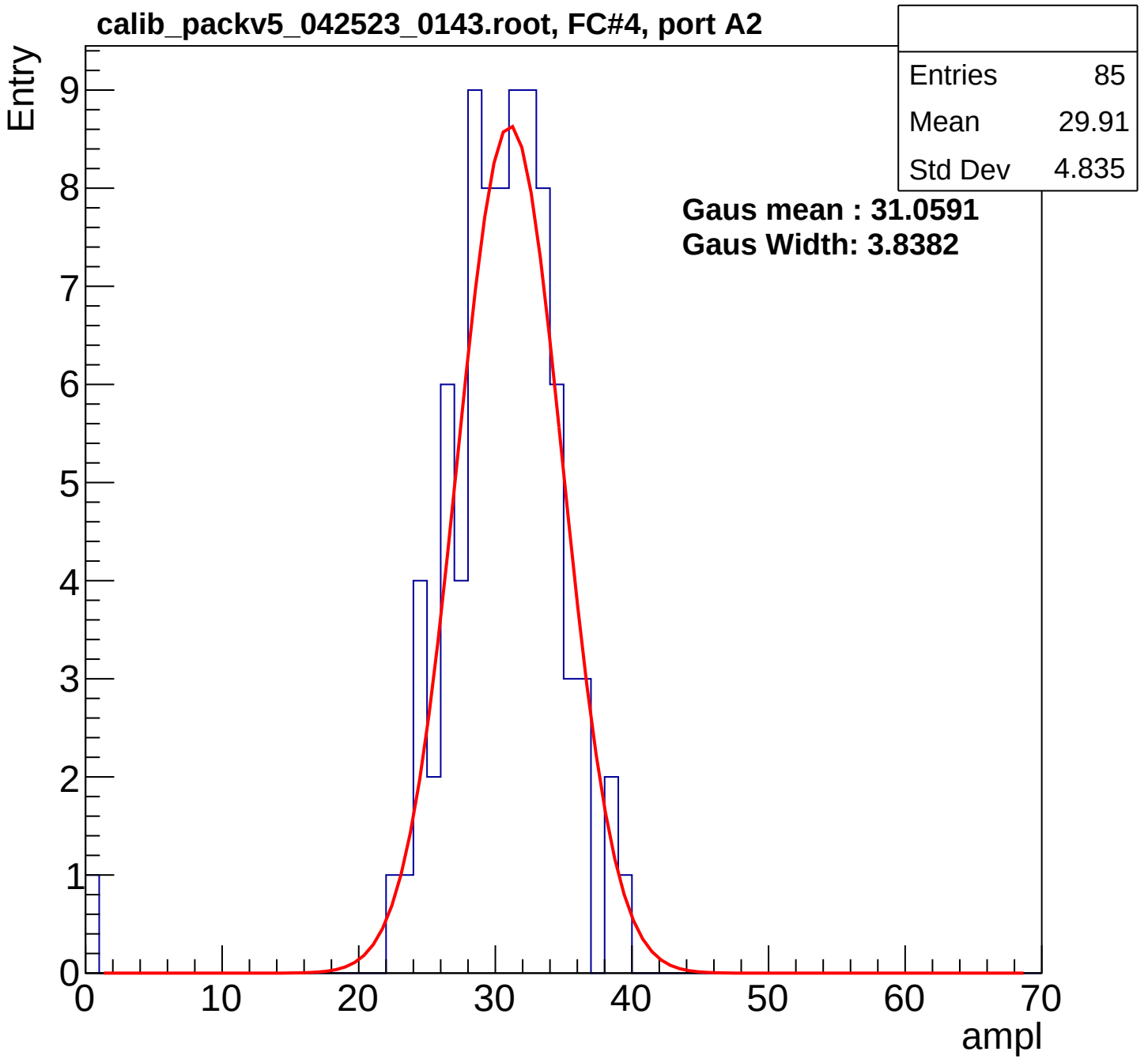

B1L100S, U4-ch16, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 49.18
Std Dev 3.641
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

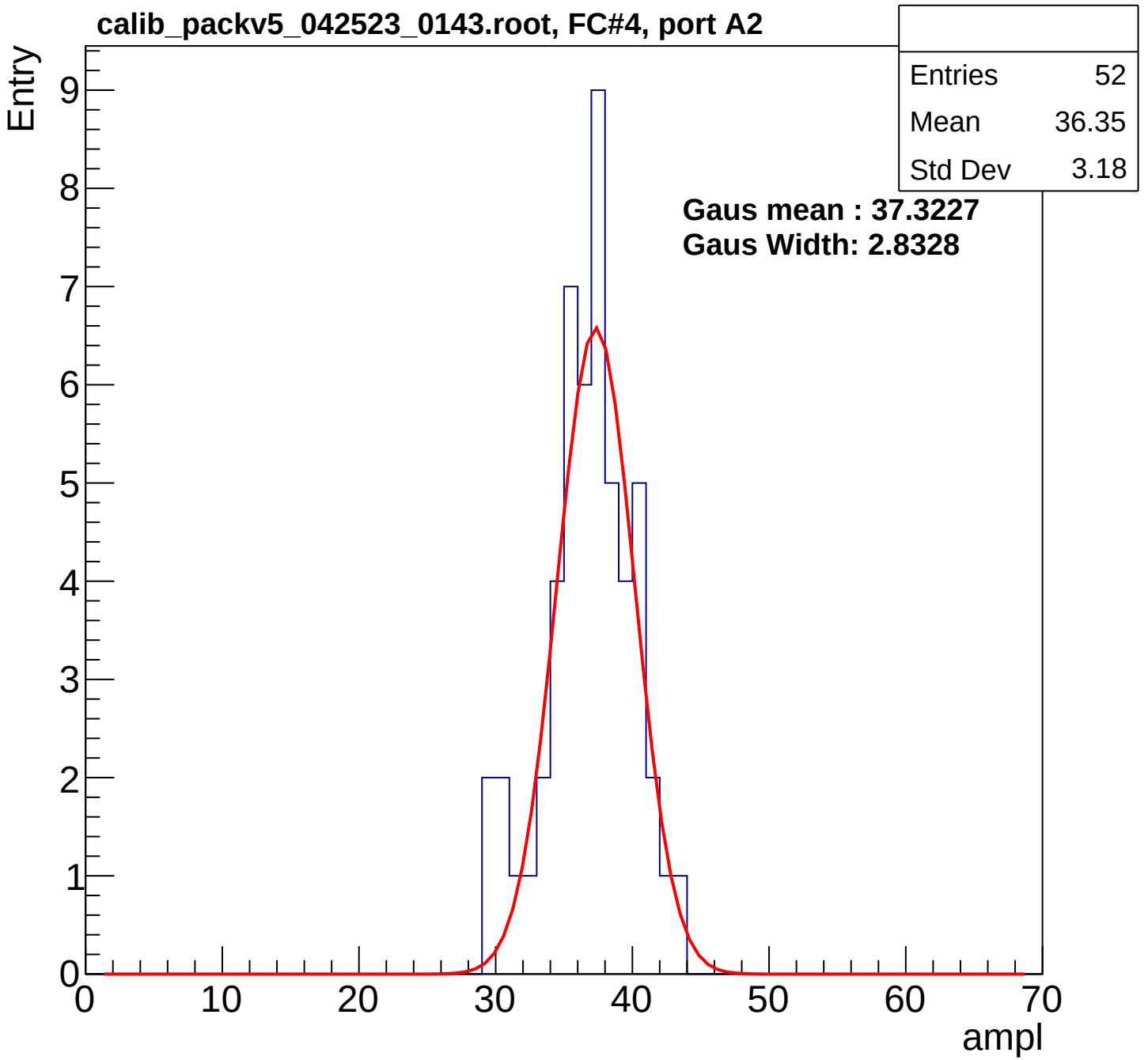

B1L100S, U4-ch16, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 55
Std Dev 3.156
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

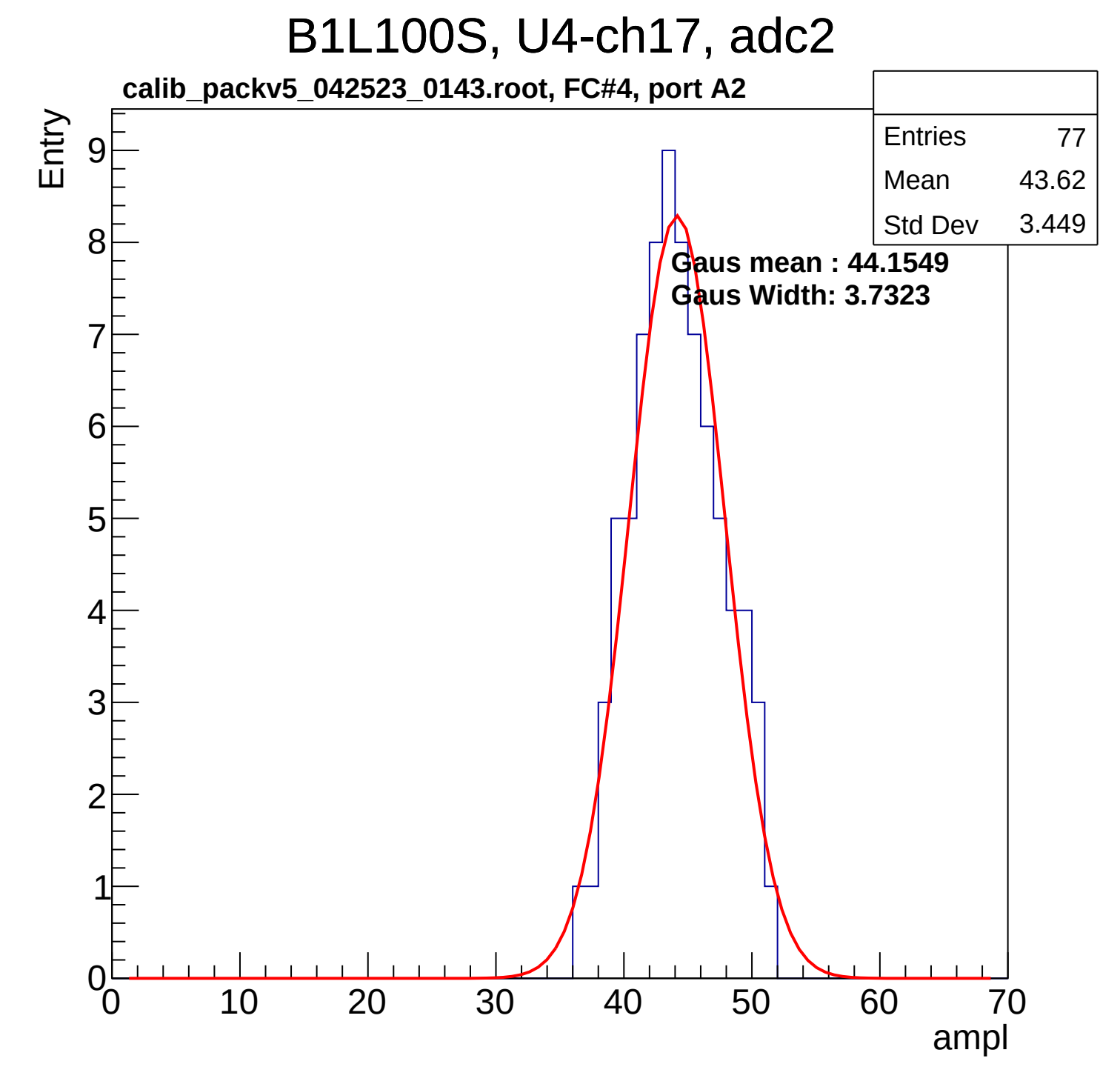

B1L100S, U4-ch16, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 58.57
Std Dev 8.154
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

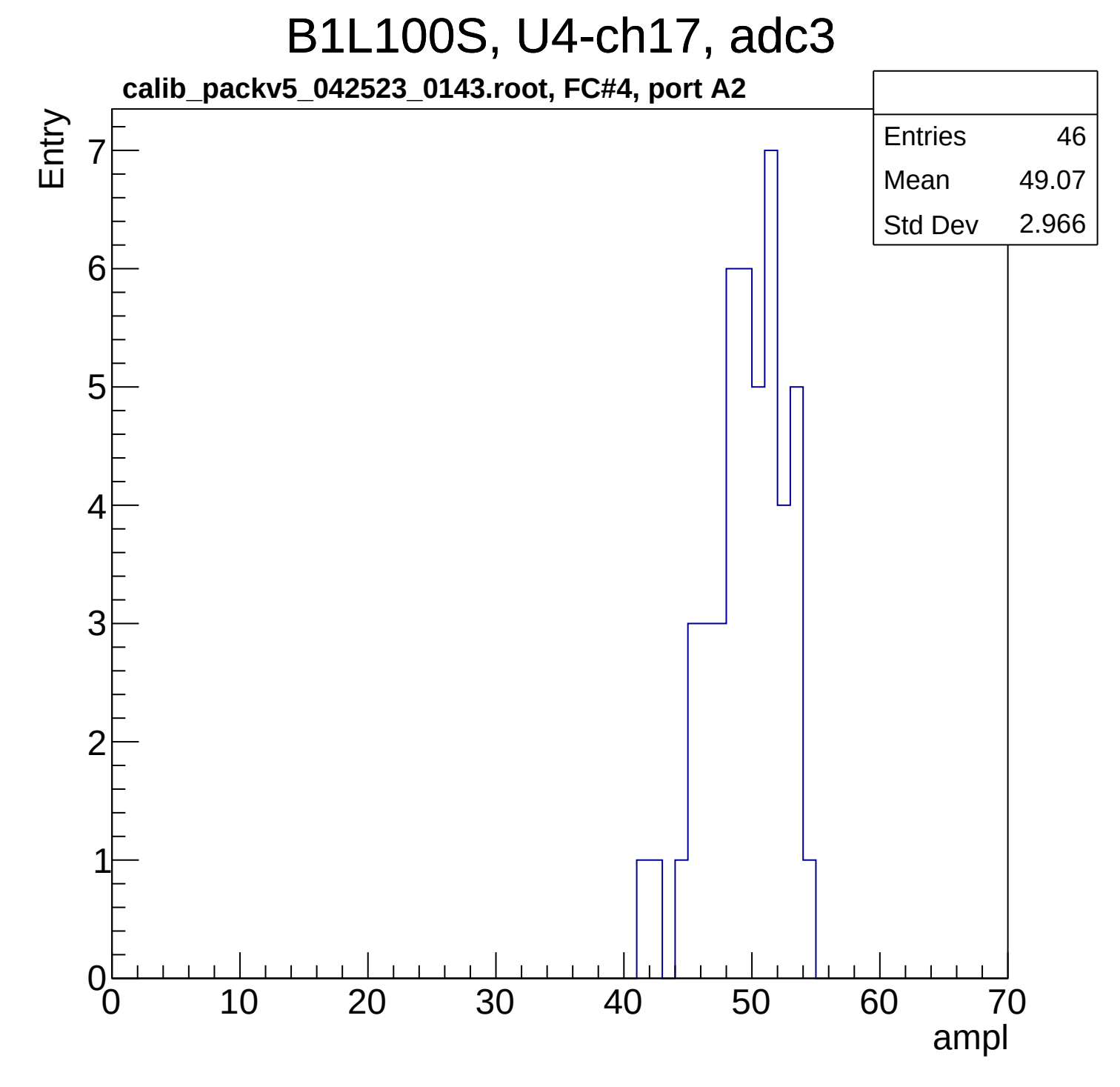

B1L100S, U4-ch16, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 63
Std Dev 0
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

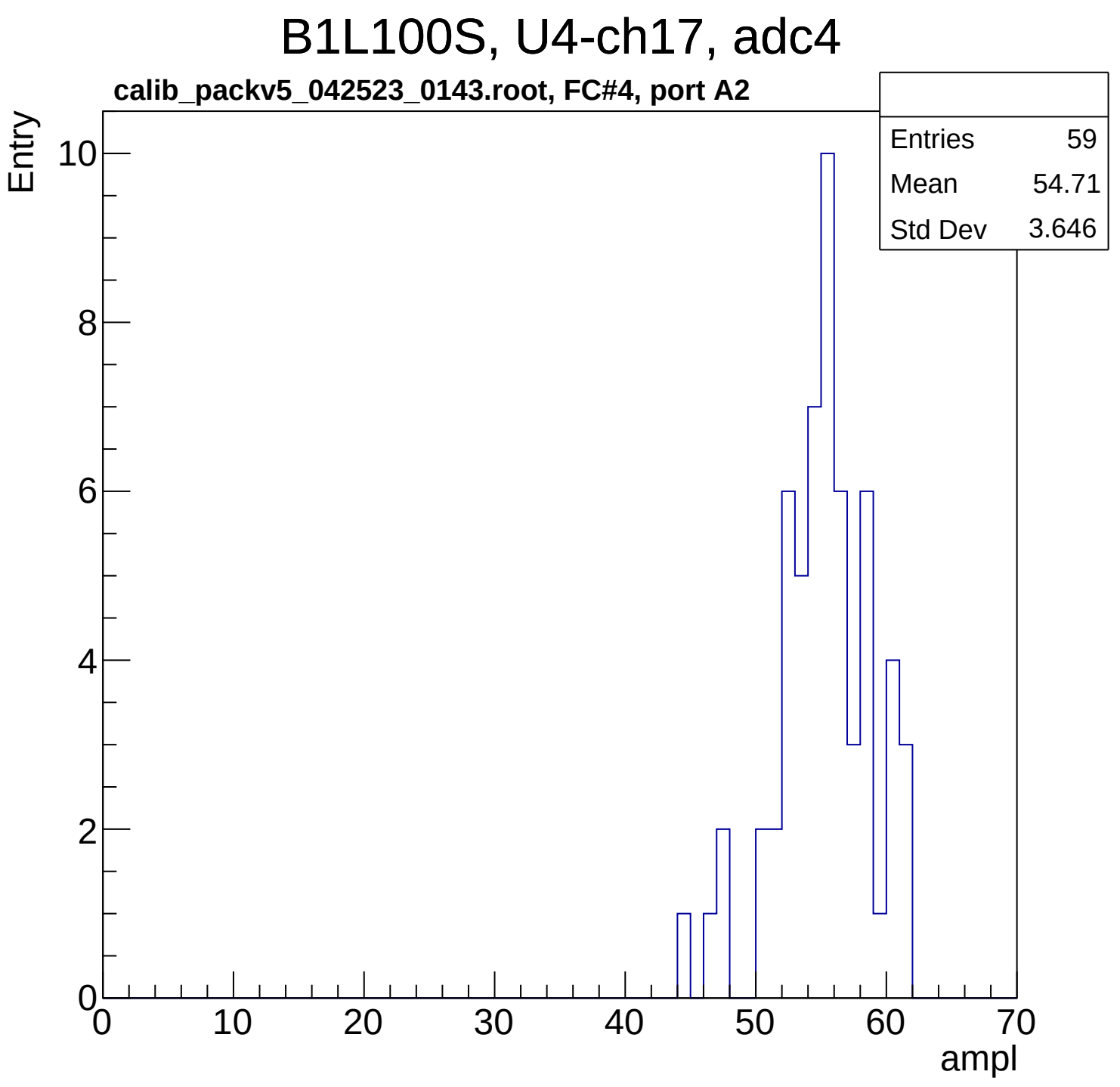

B1L100S, U4-ch16, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 22
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

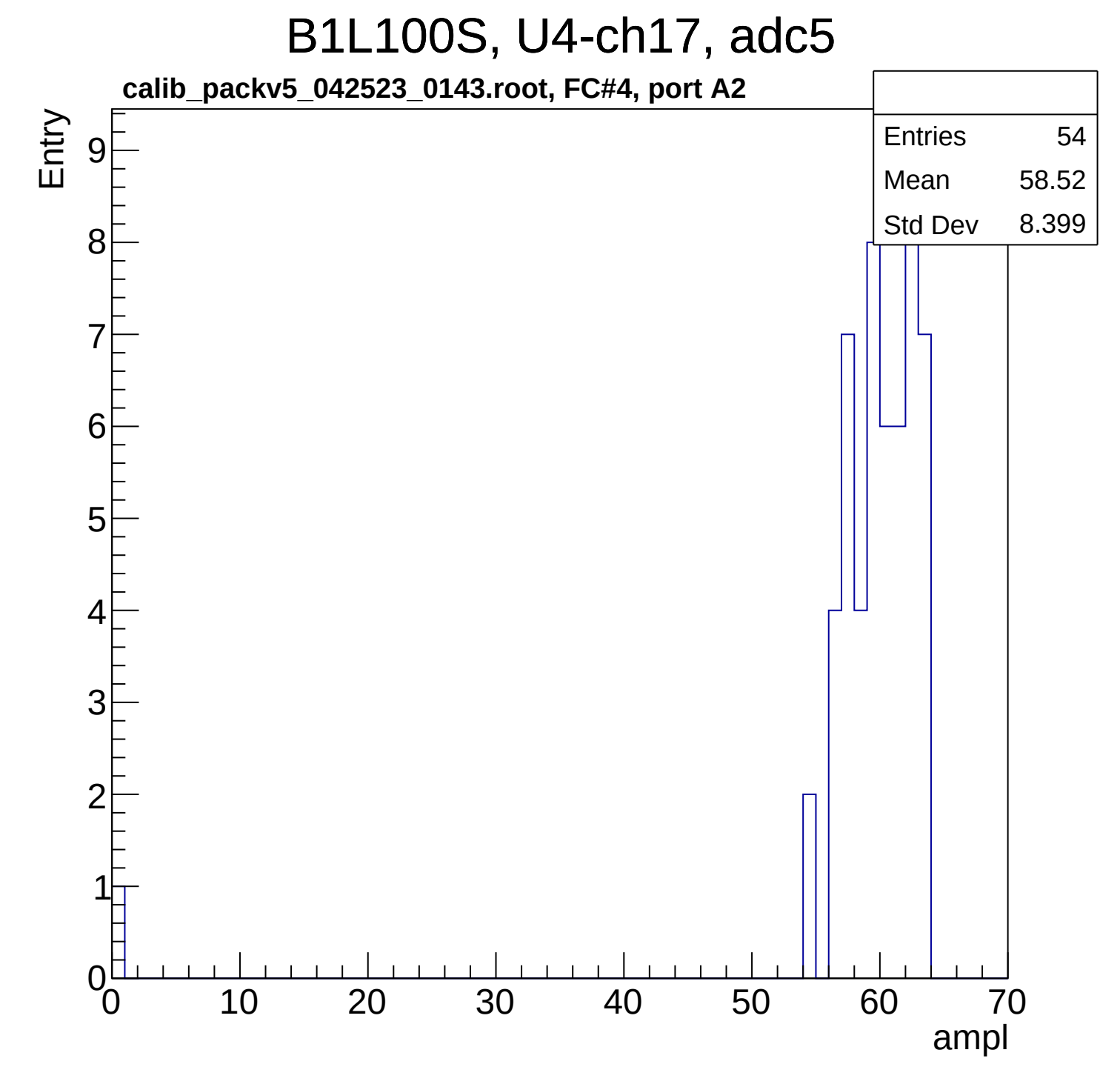

B1L100S, U4-ch17, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 85
Mean 29.91
Std Dev 4.835
Gaus mean : 31.0591
Gaus Width: 3.8382
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

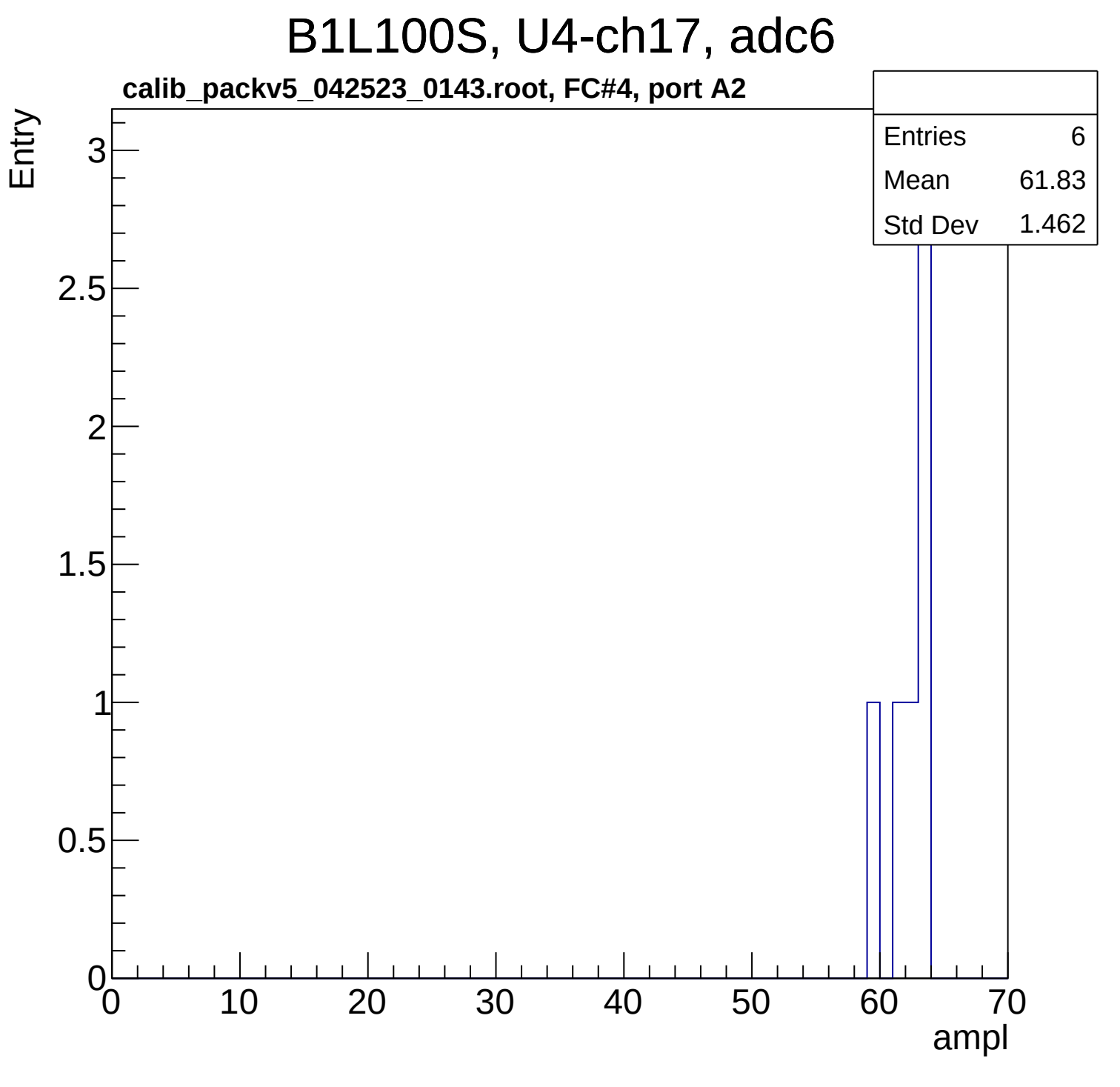

B1L100S, U4-ch17, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 36.35
Std Dev 3.18
Gaus mean : 37.3227
Gaus Width: 2.8328
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

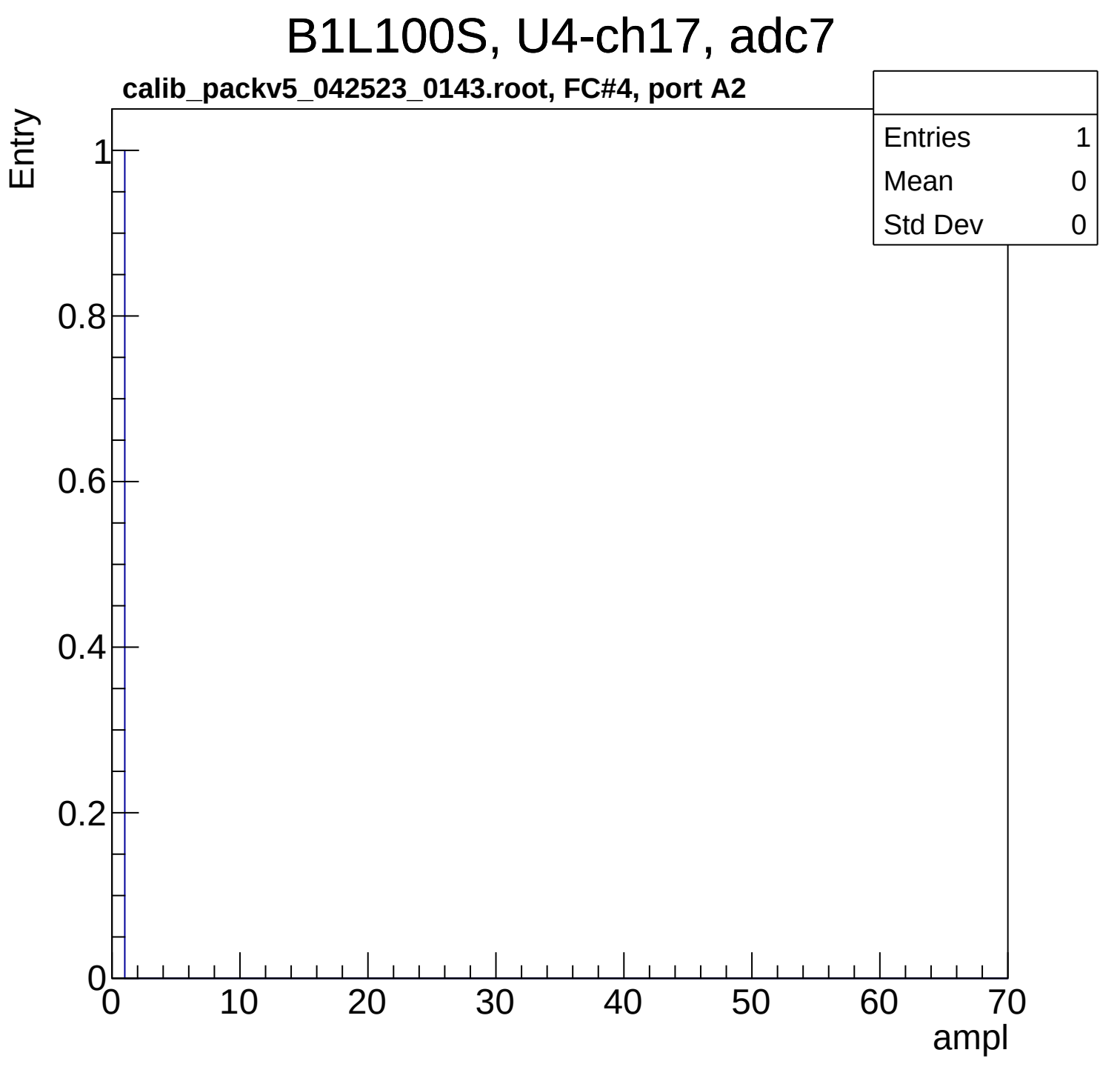

B1L100S, U4-ch17, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 43.62
Std Dev 3.449
Gaus mean : 44.1549
Gaus Width: 3.7323
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

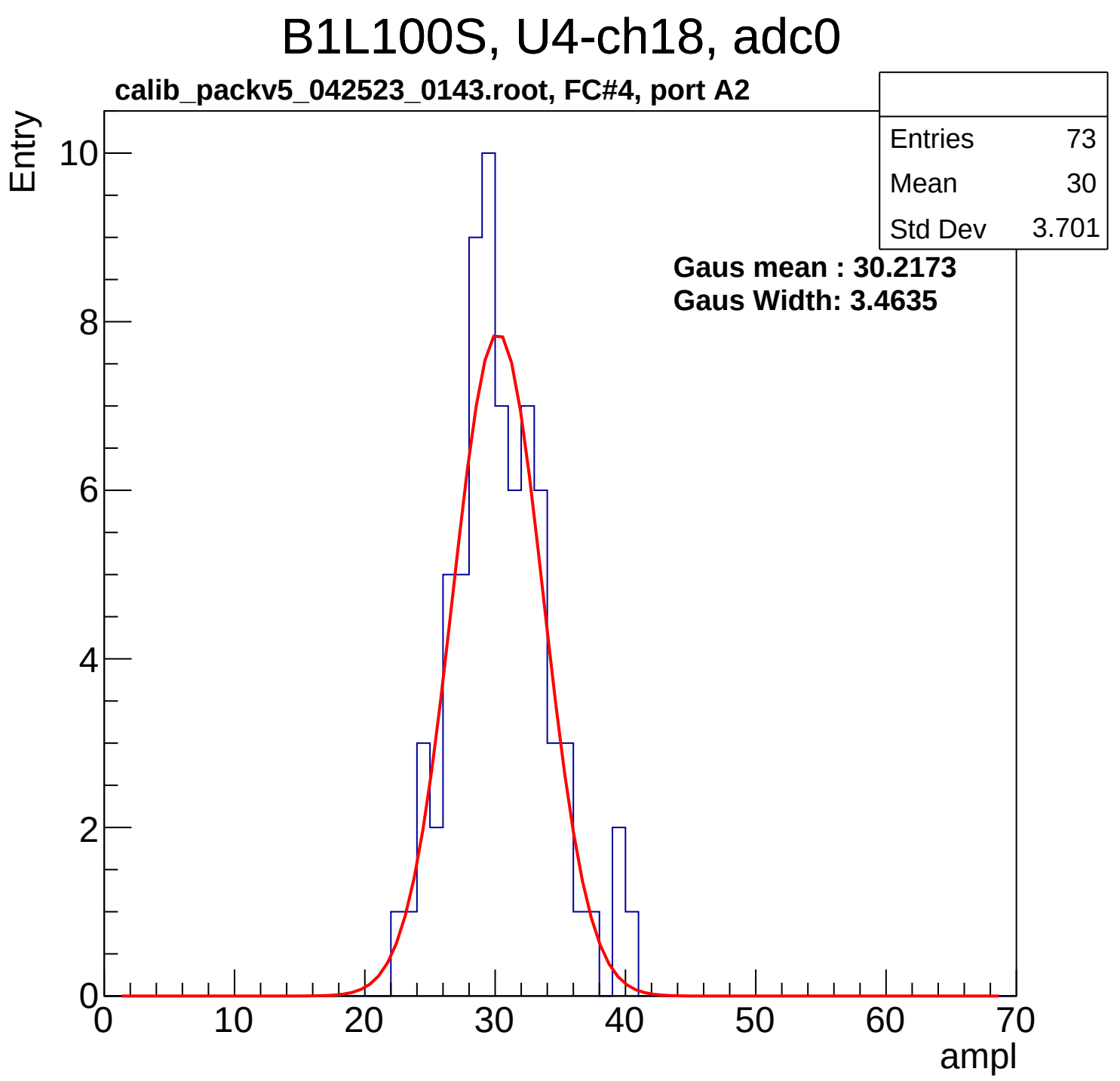

B1L100S, U4-ch17, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 49.07
Std Dev 2.966
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

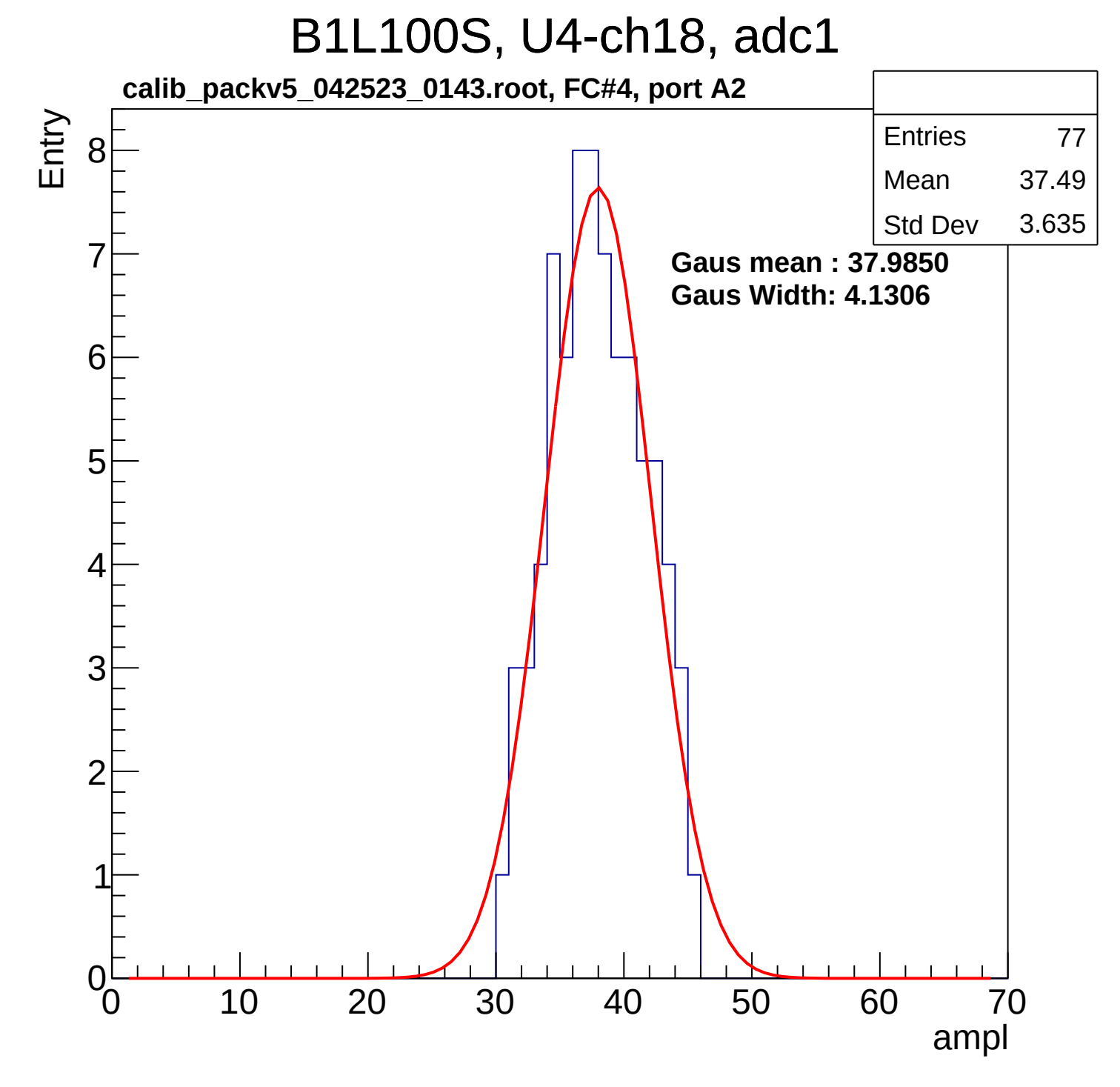

B1L100S, U4-ch17, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 54.71
Std Dev 3.646
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

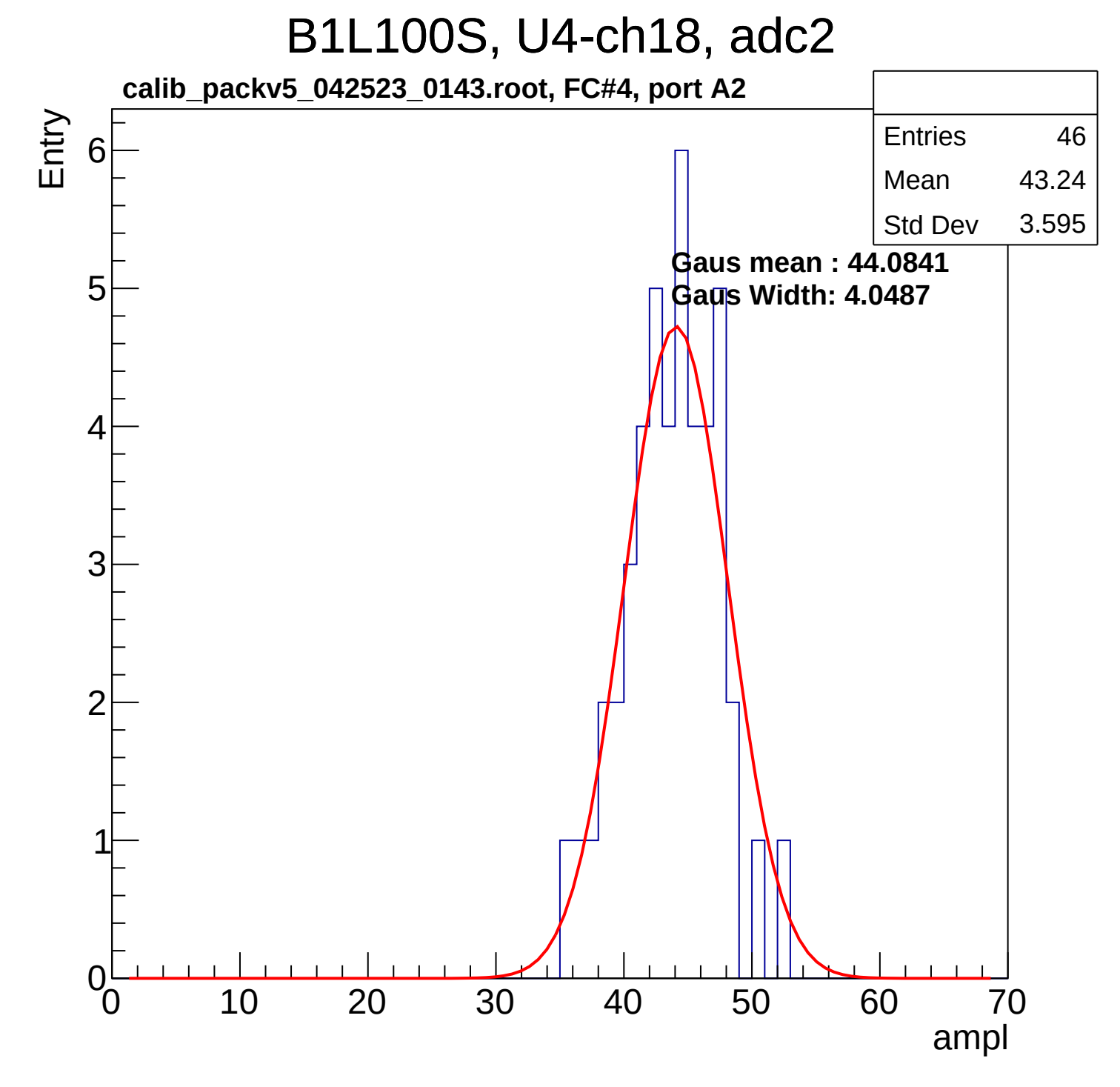

B1L100S, U4-ch17, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 58.52
Std Dev 8.399
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

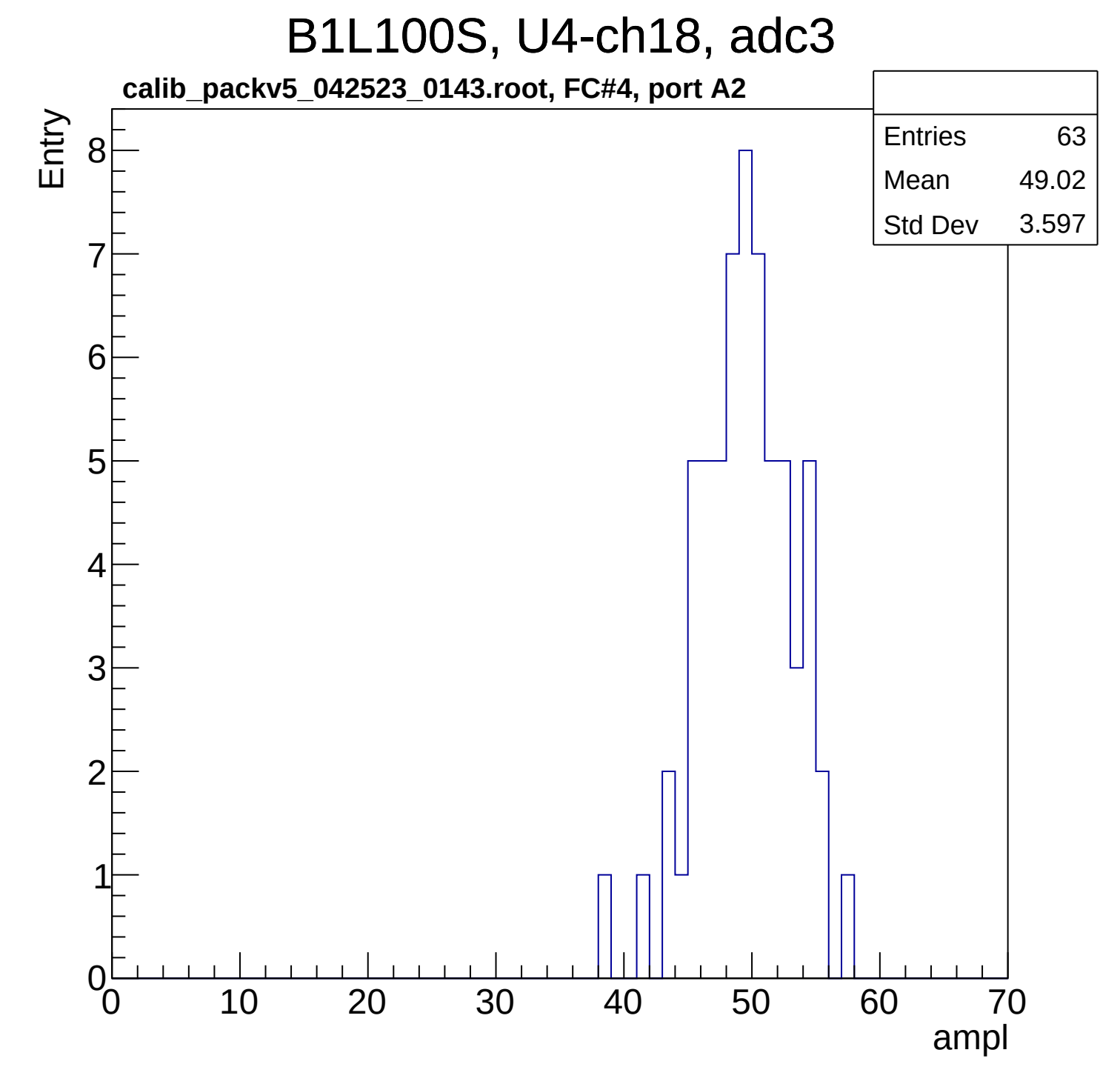

B1L100S, U4-ch17, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 61.83
Std Dev 1.462
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

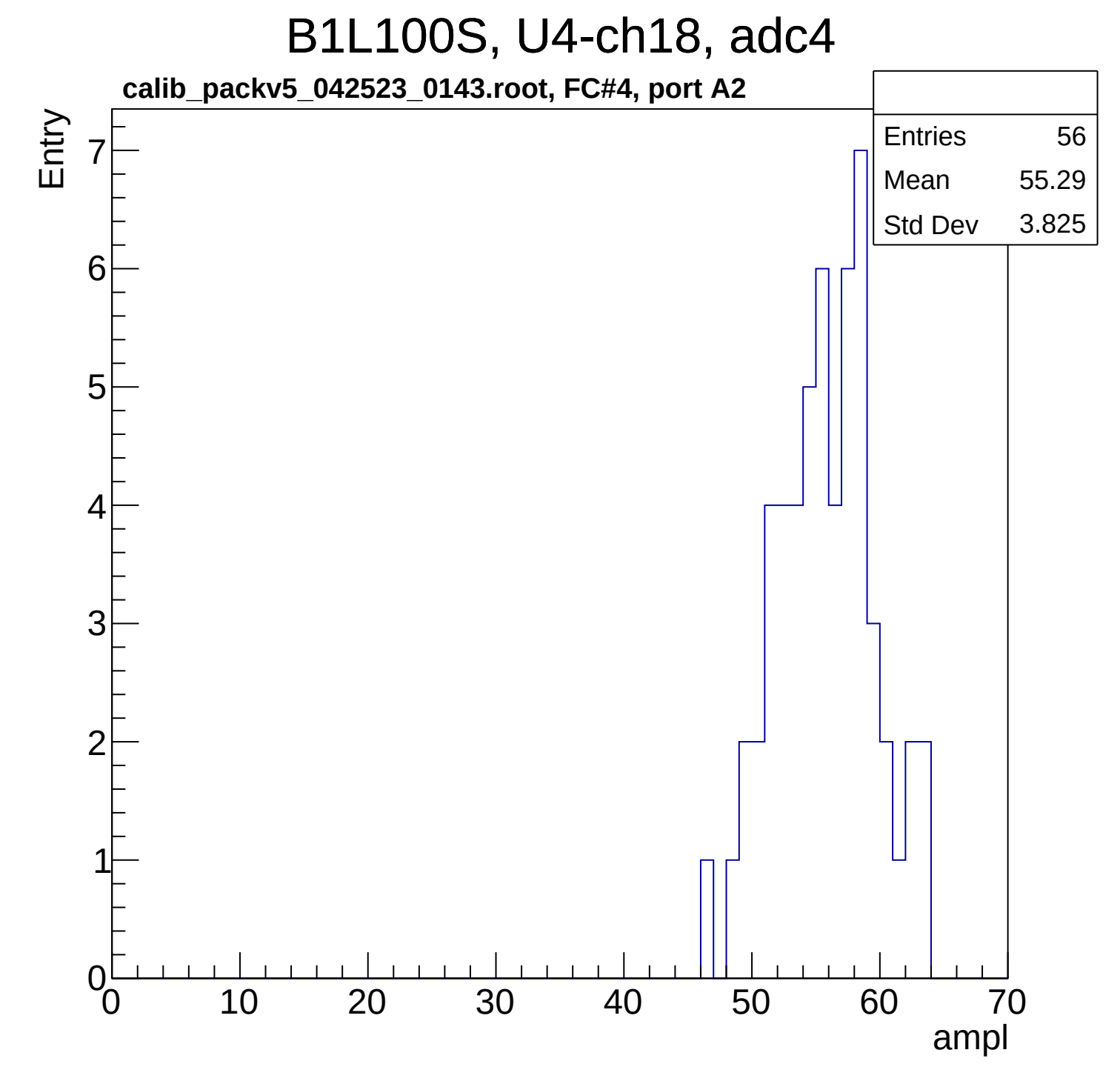

B1L100S, U4-ch17, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

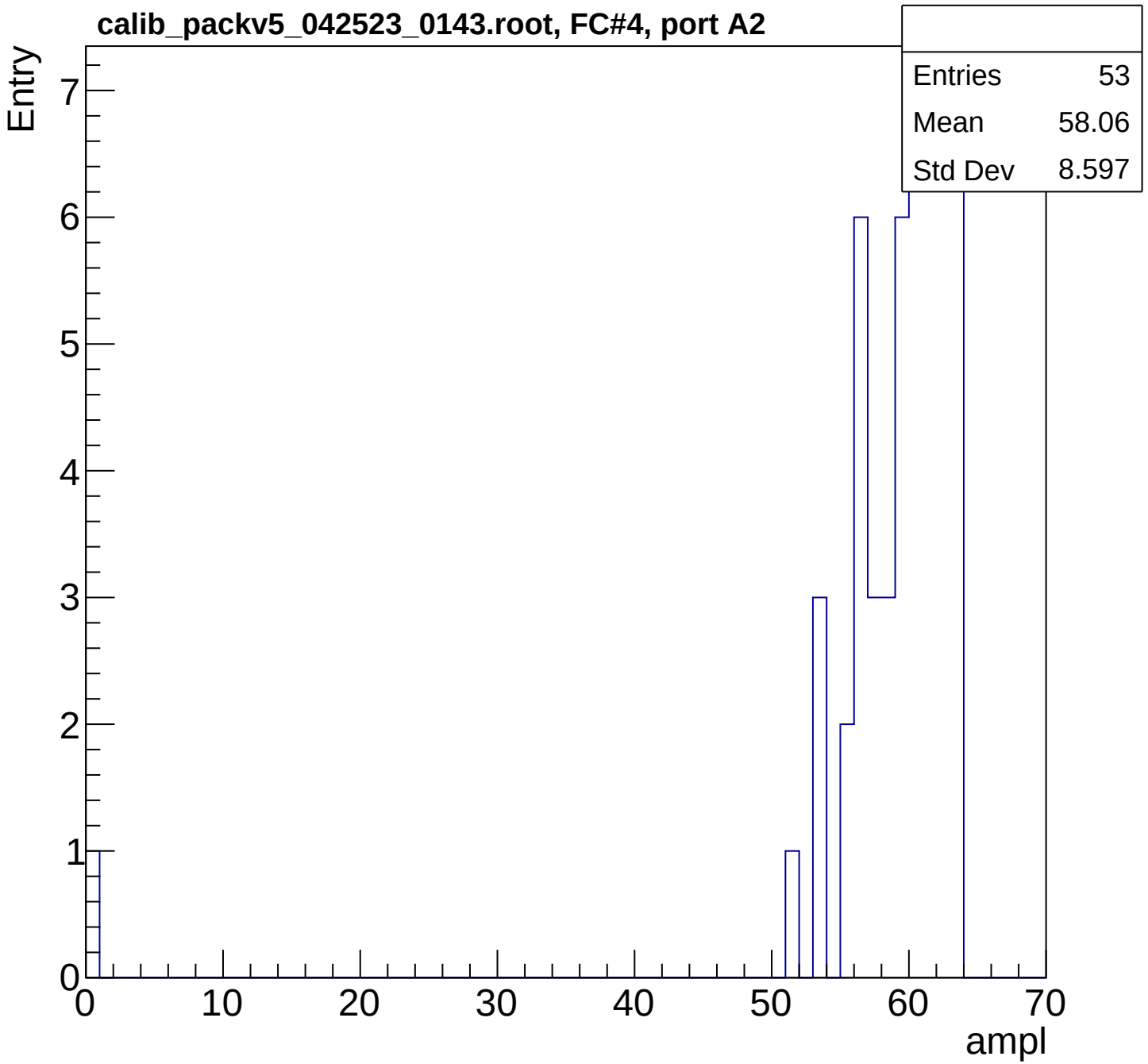

B1L100S, U4-ch18, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 30
Std Dev 3.701
Gaus mean : 30.2173
Gaus Width: 3.4635
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

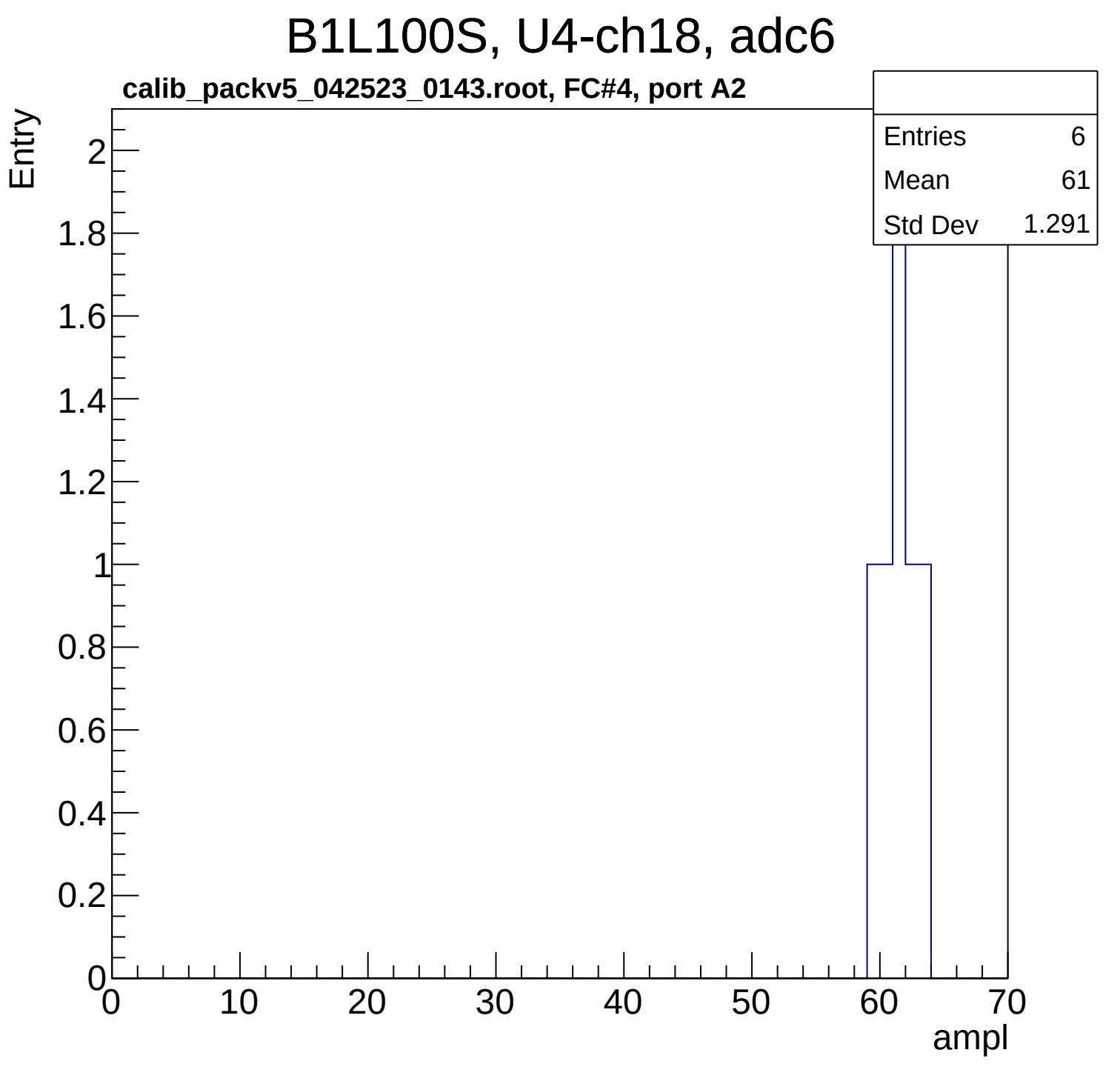

B1L100S, U4-ch18, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 37.49
Std Dev 3.635
Gaus mean : 37.9850
Gaus Width: 4.1306
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

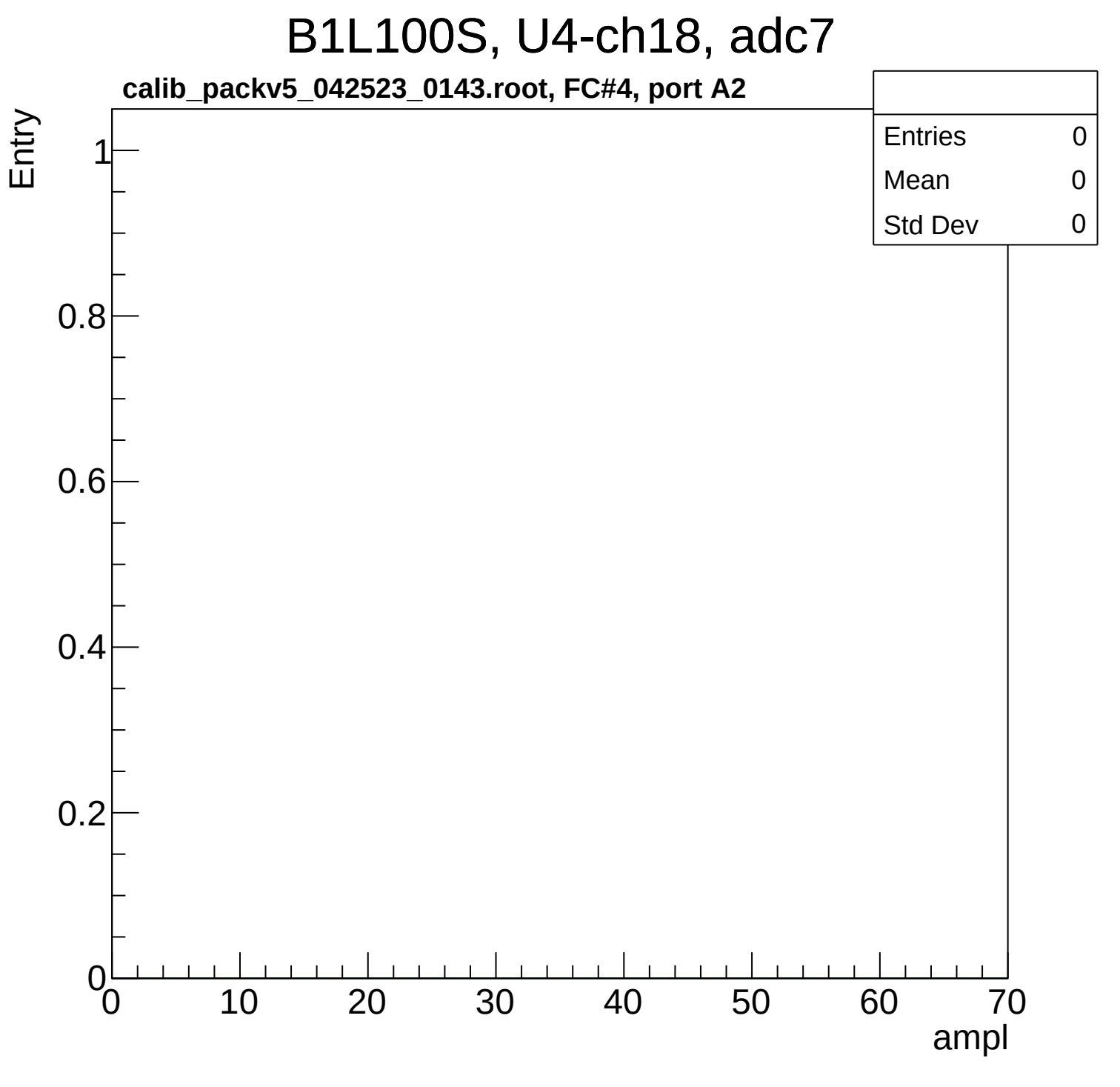

B1L100S, U4-ch18, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 43.24
Std Dev 3.595
Gaus mean : 44.0841
Gaus Width: 4.0487
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

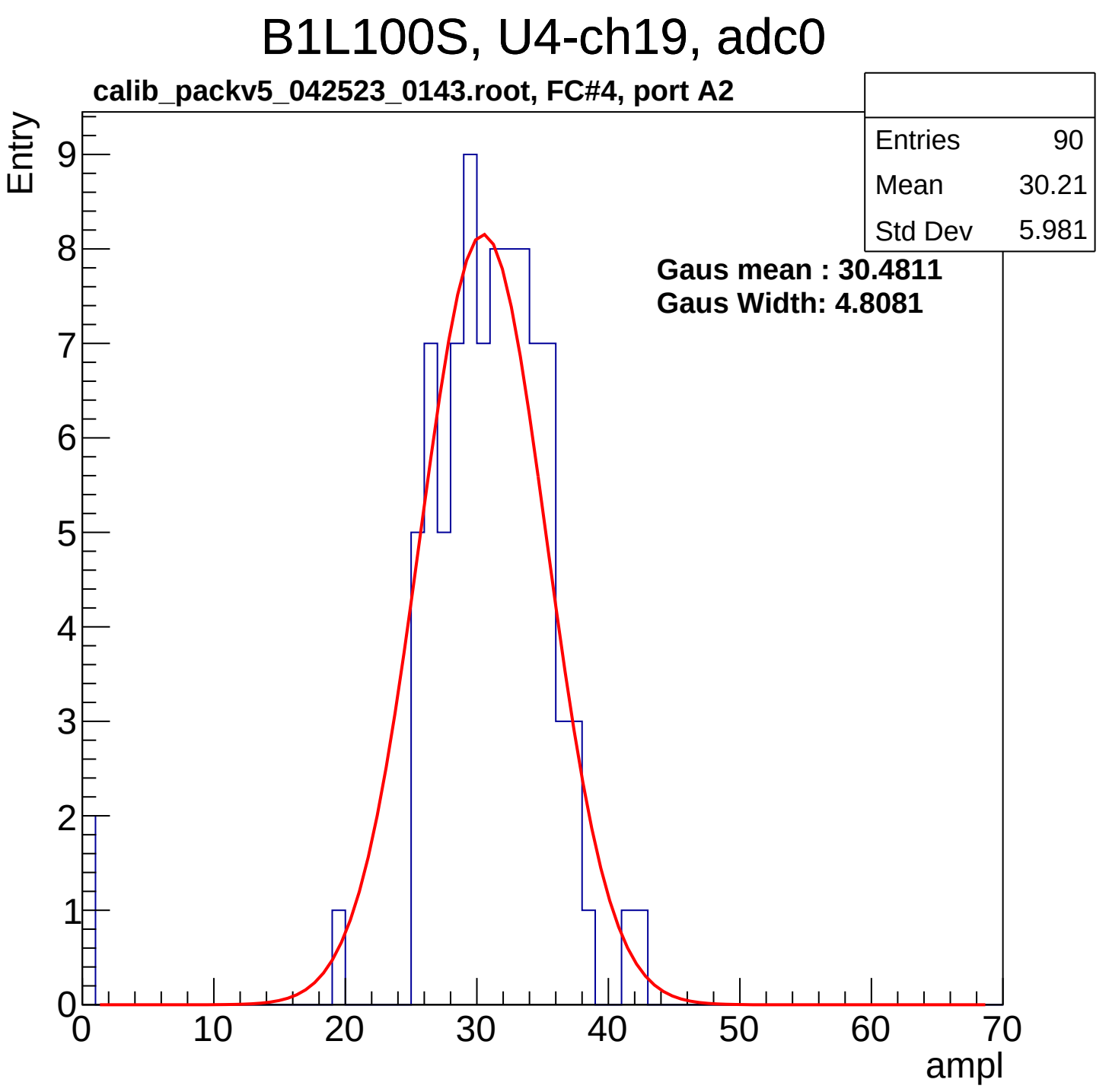

B1L100S, U4-ch18, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 49.02
Std Dev 3.597
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

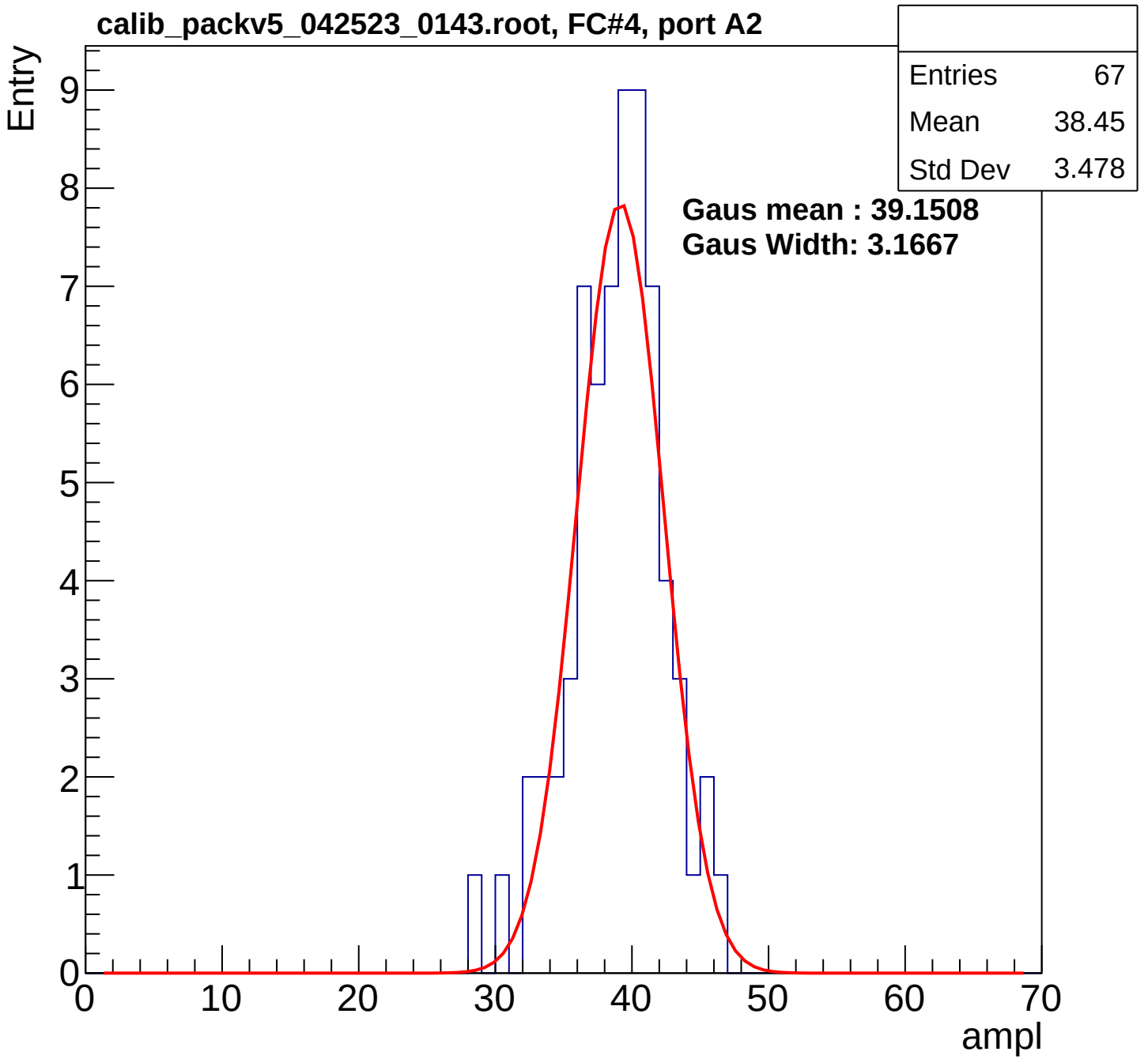

B1L100S, U4-ch18, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 55.29
Std Dev 3.825
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

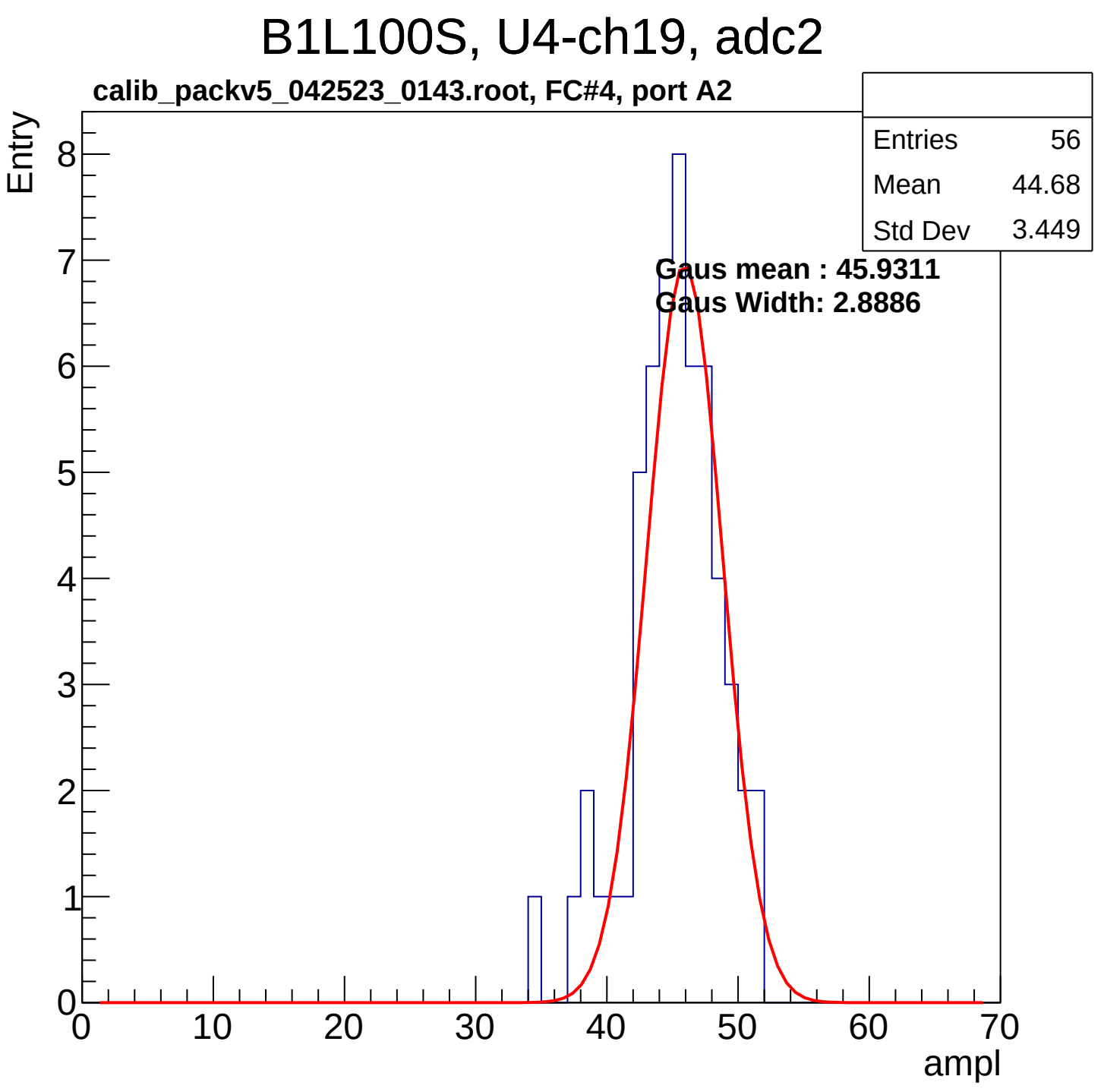

B1L100S, U4-ch18, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 58.06
Std Dev 8.597
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

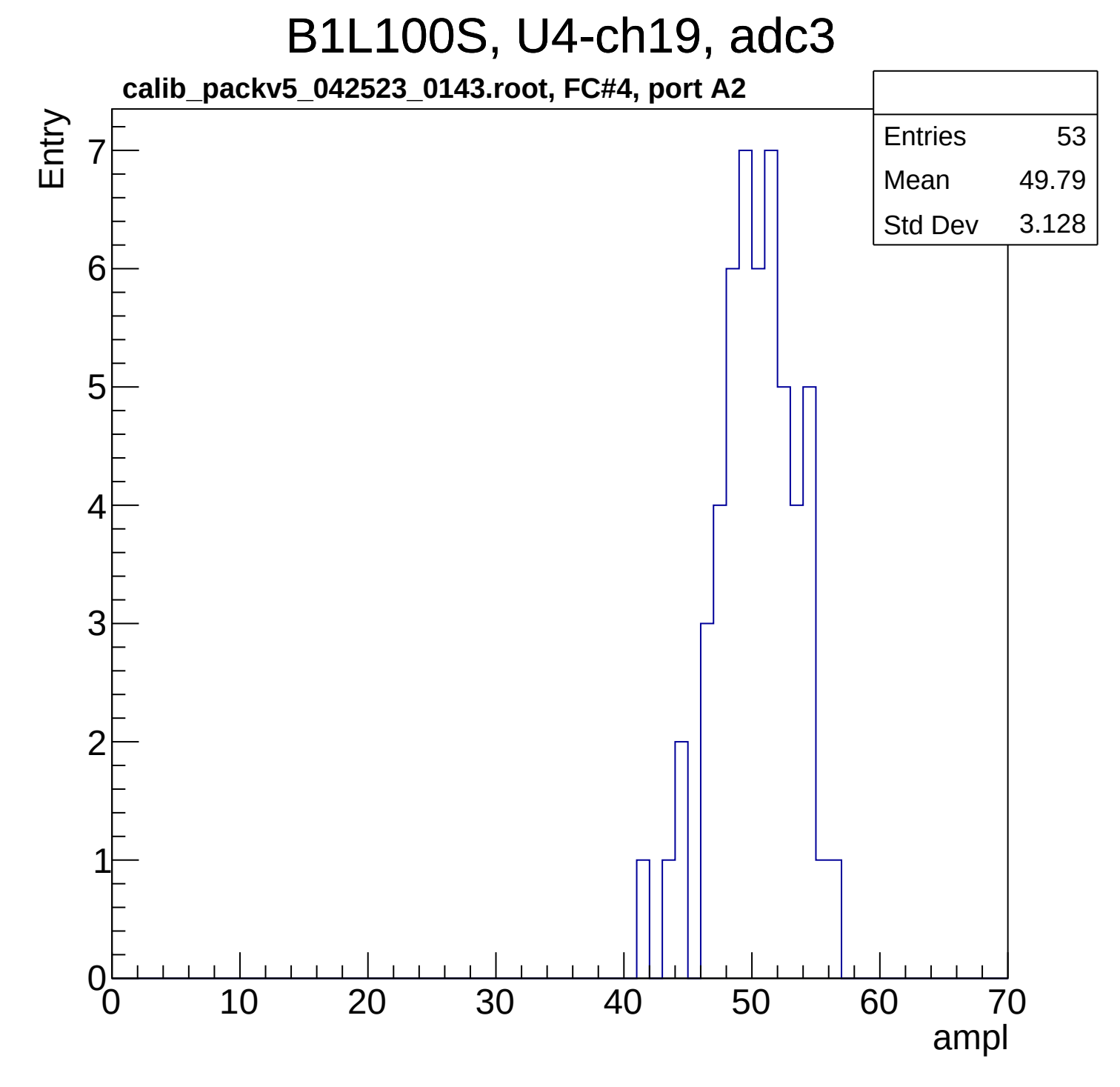

B1L100S, U4-ch18, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 61
Std Dev 1.291
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

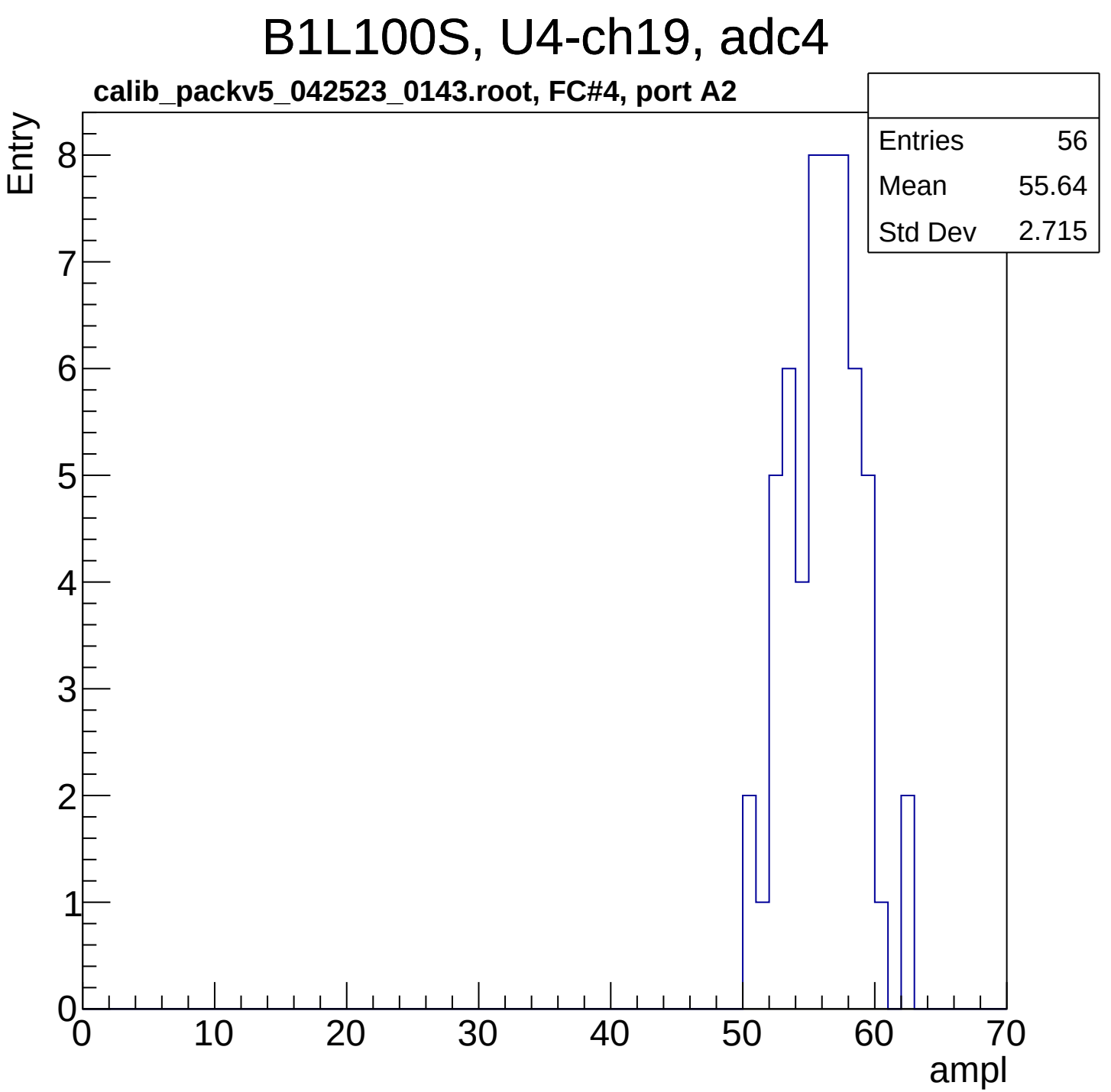

B1L100S, U4-ch18, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

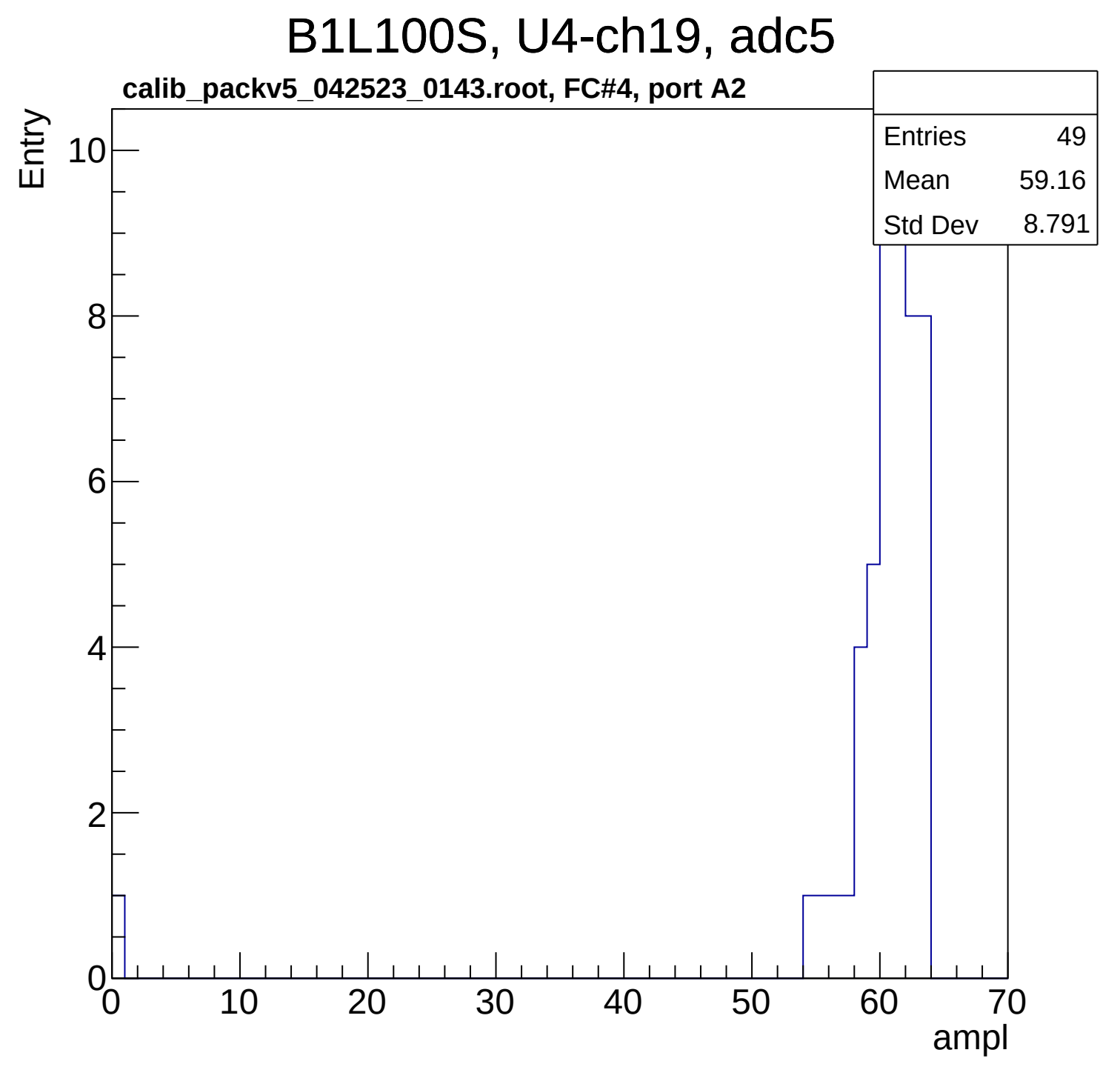

B1L100S, U4-ch19, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 90
Mean 30.21
Std Dev 5.981
Gaus mean : 30.4811
Gaus Width: 4.8081
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

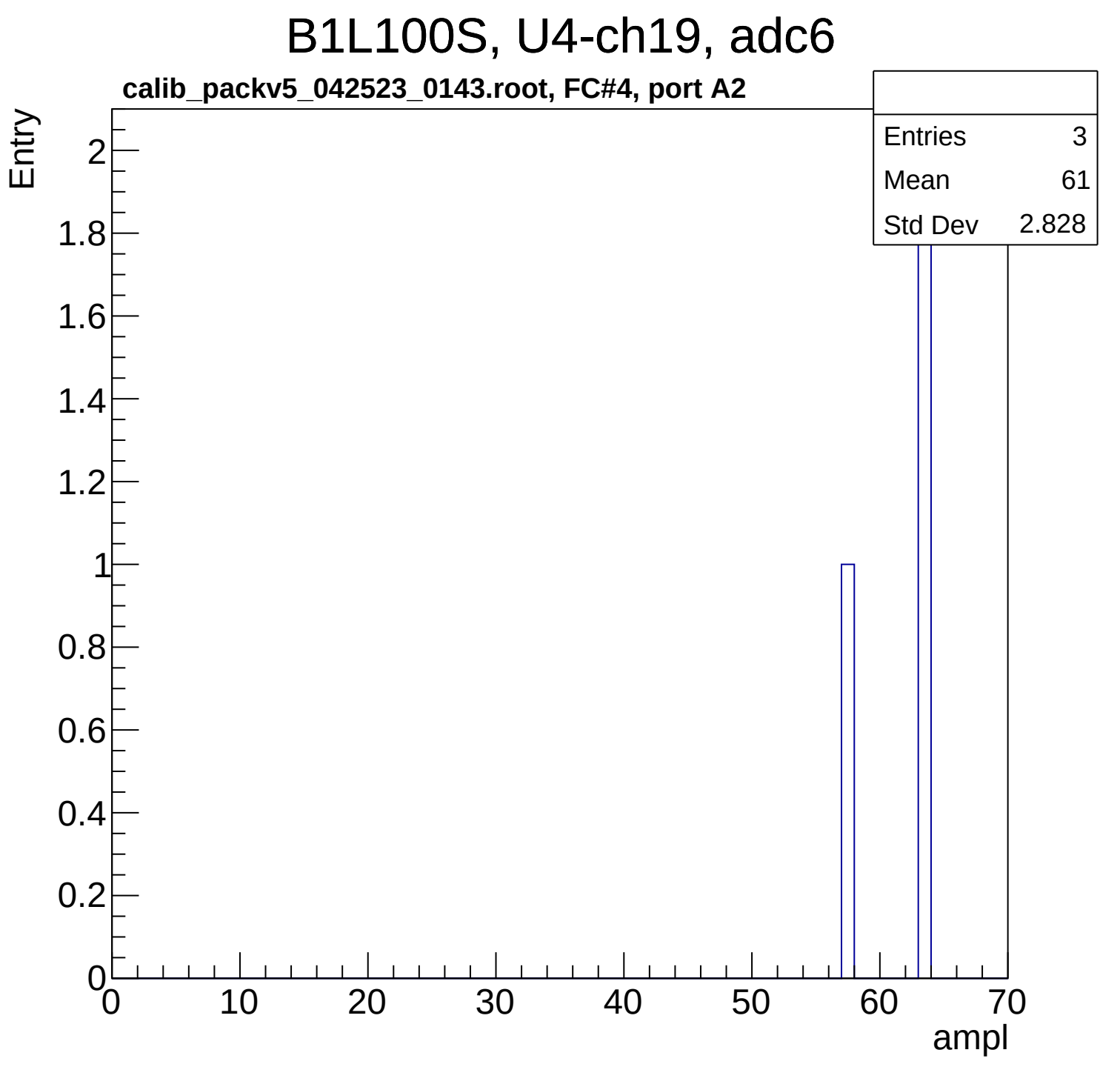

B1L100S, U4-ch19, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 38.45
Std Dev 3.478
Gaus mean : 39.1508
Gaus Width: 3.1667
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

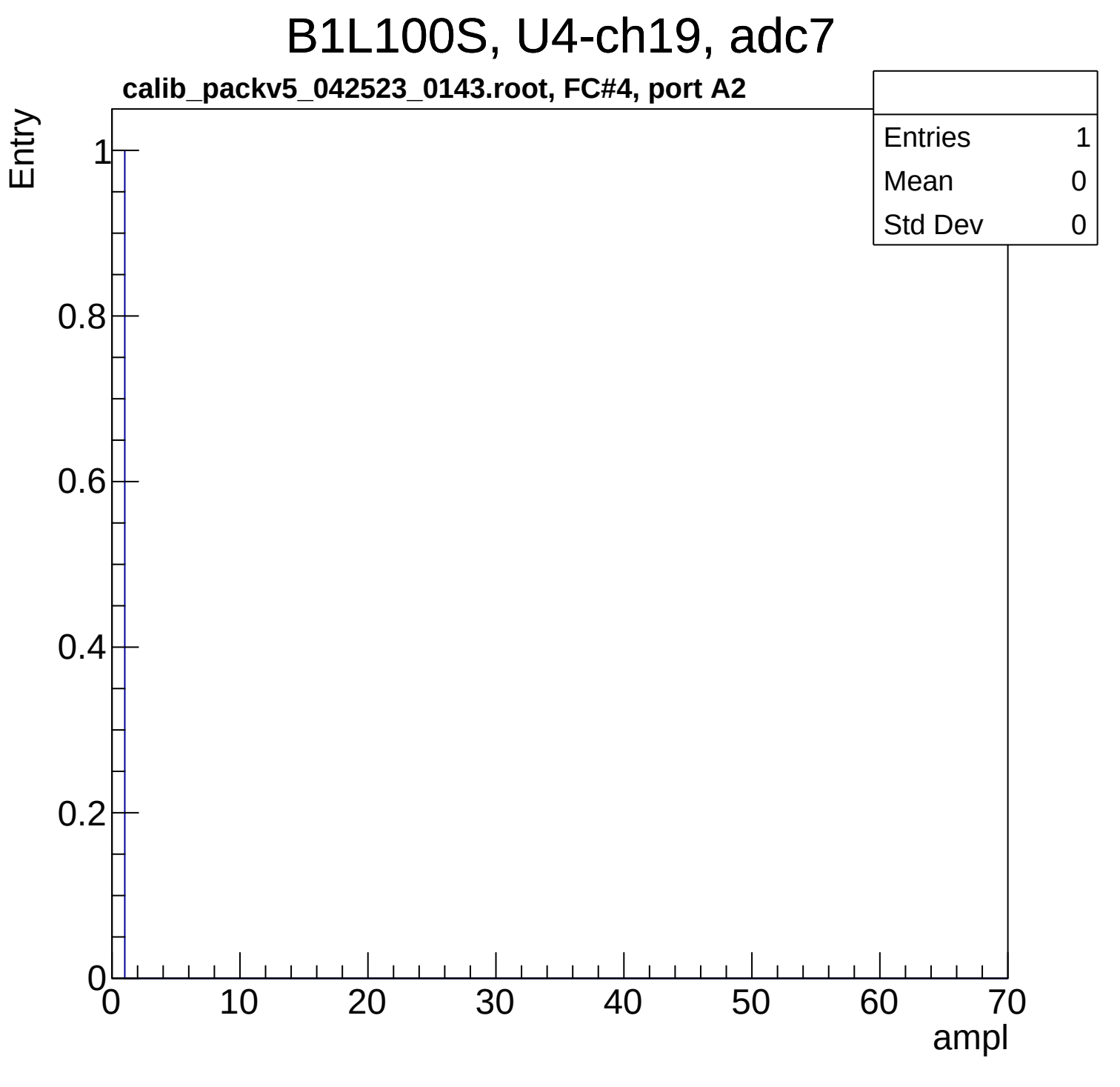

B1L100S, U4-ch19, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 44.68
Std Dev 3.449
Gaus mean : 45.9311
Gaus Width: 2.8886
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

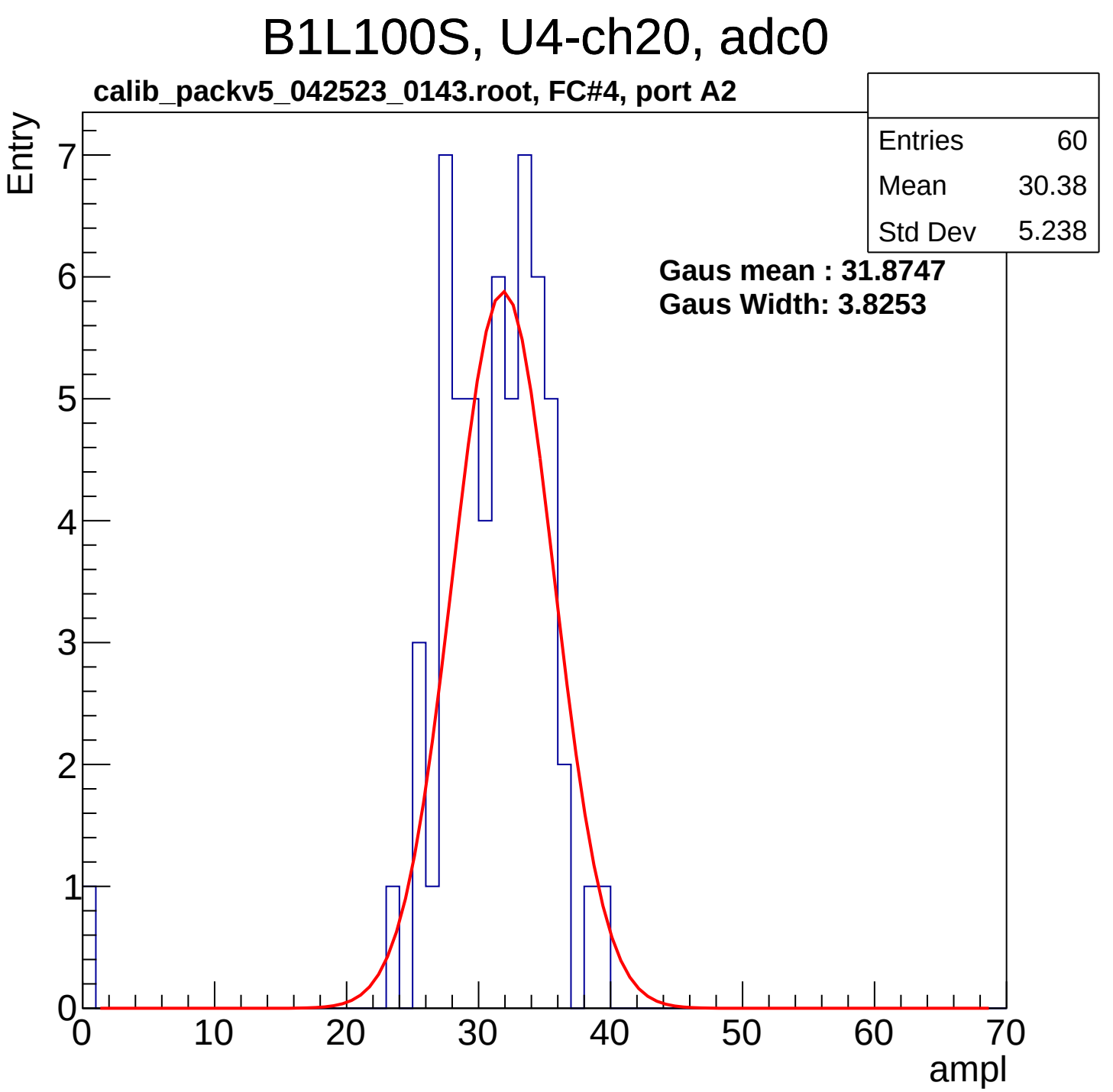

B1L100S, U4-ch19, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 49.79
Std Dev 3.128
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

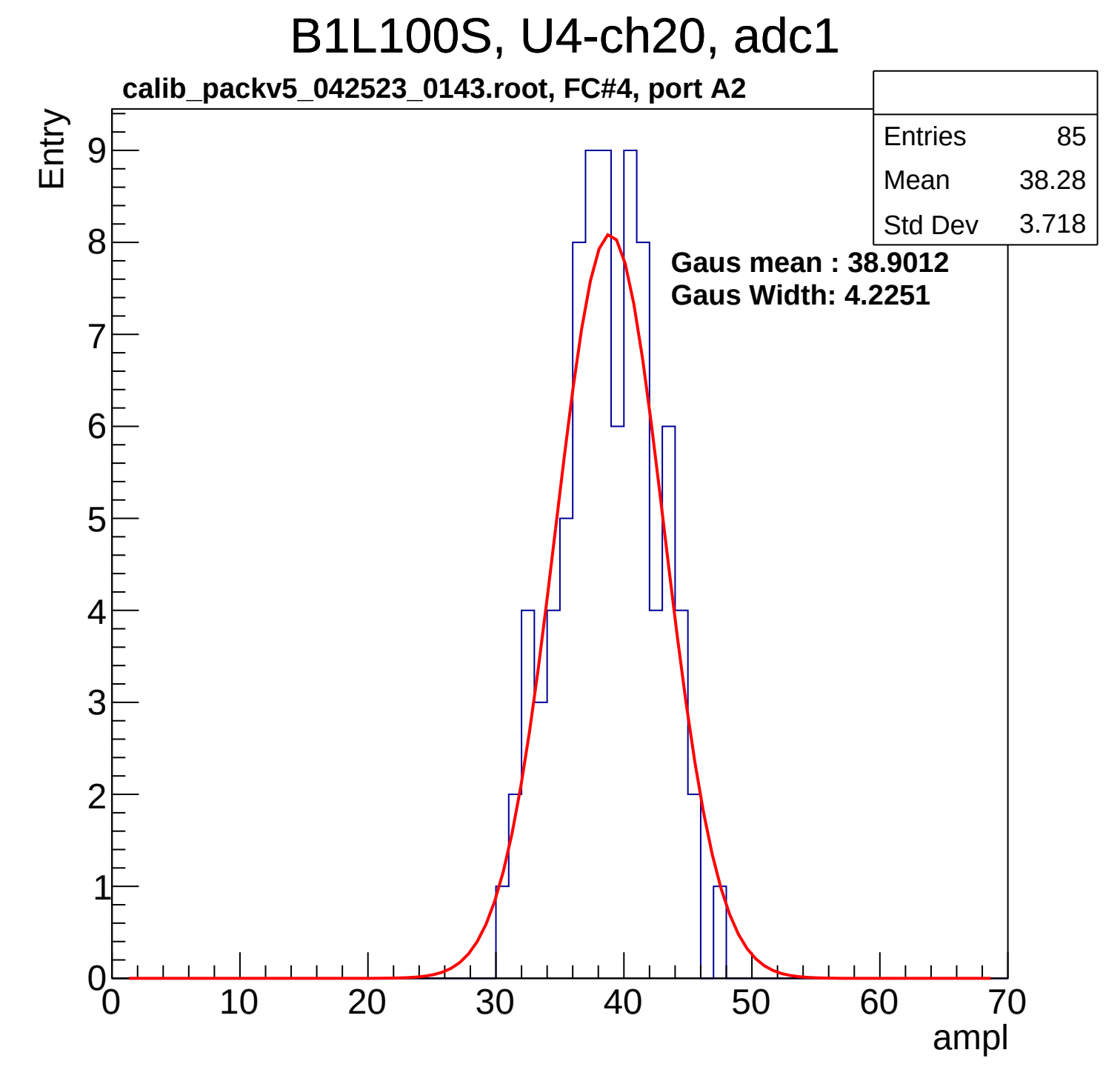

B1L100S, U4-ch19, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 55.64
Std Dev 2.715
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

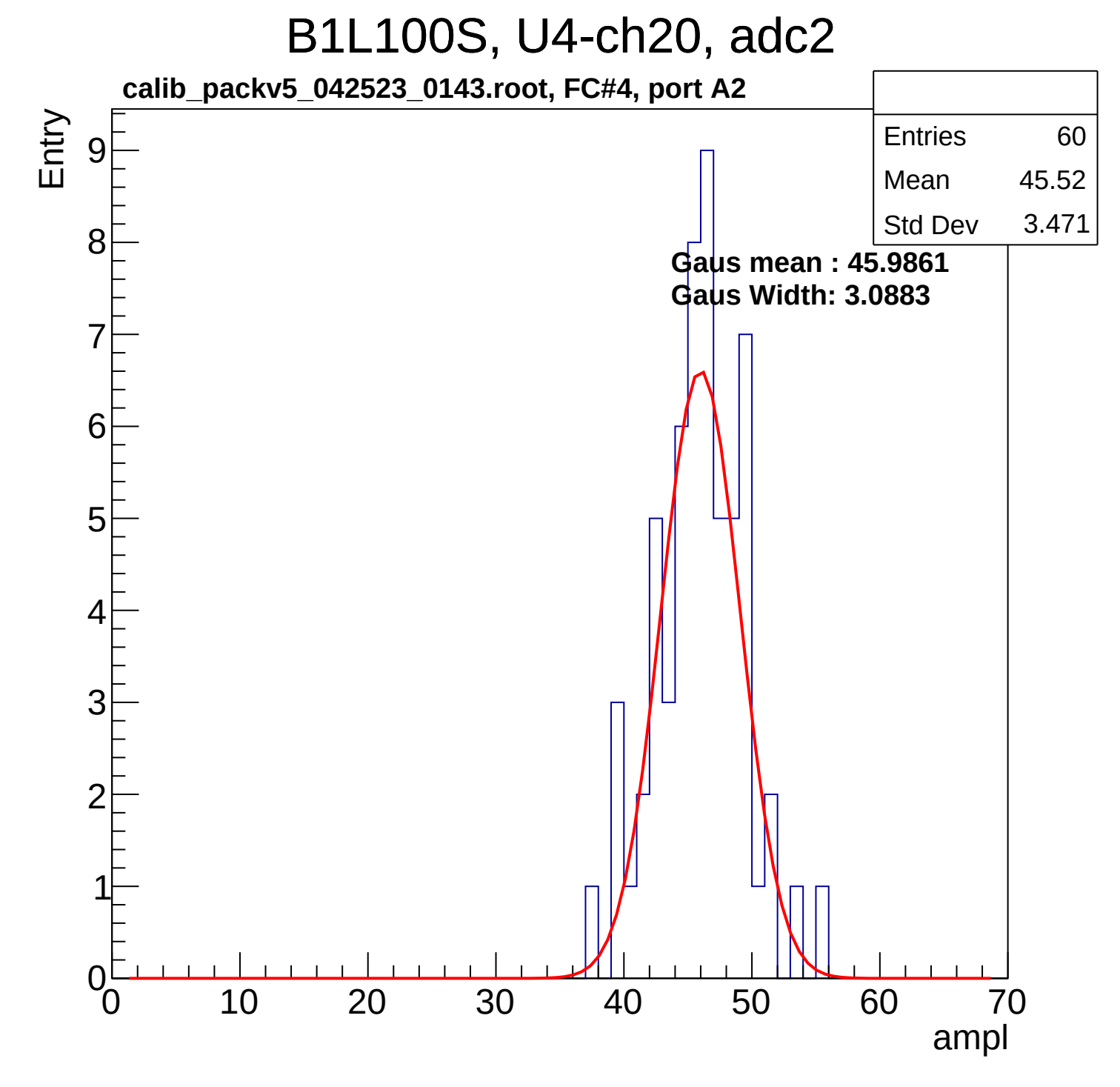

B1L100S, U4-ch19, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 59.16
Std Dev 8.791
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

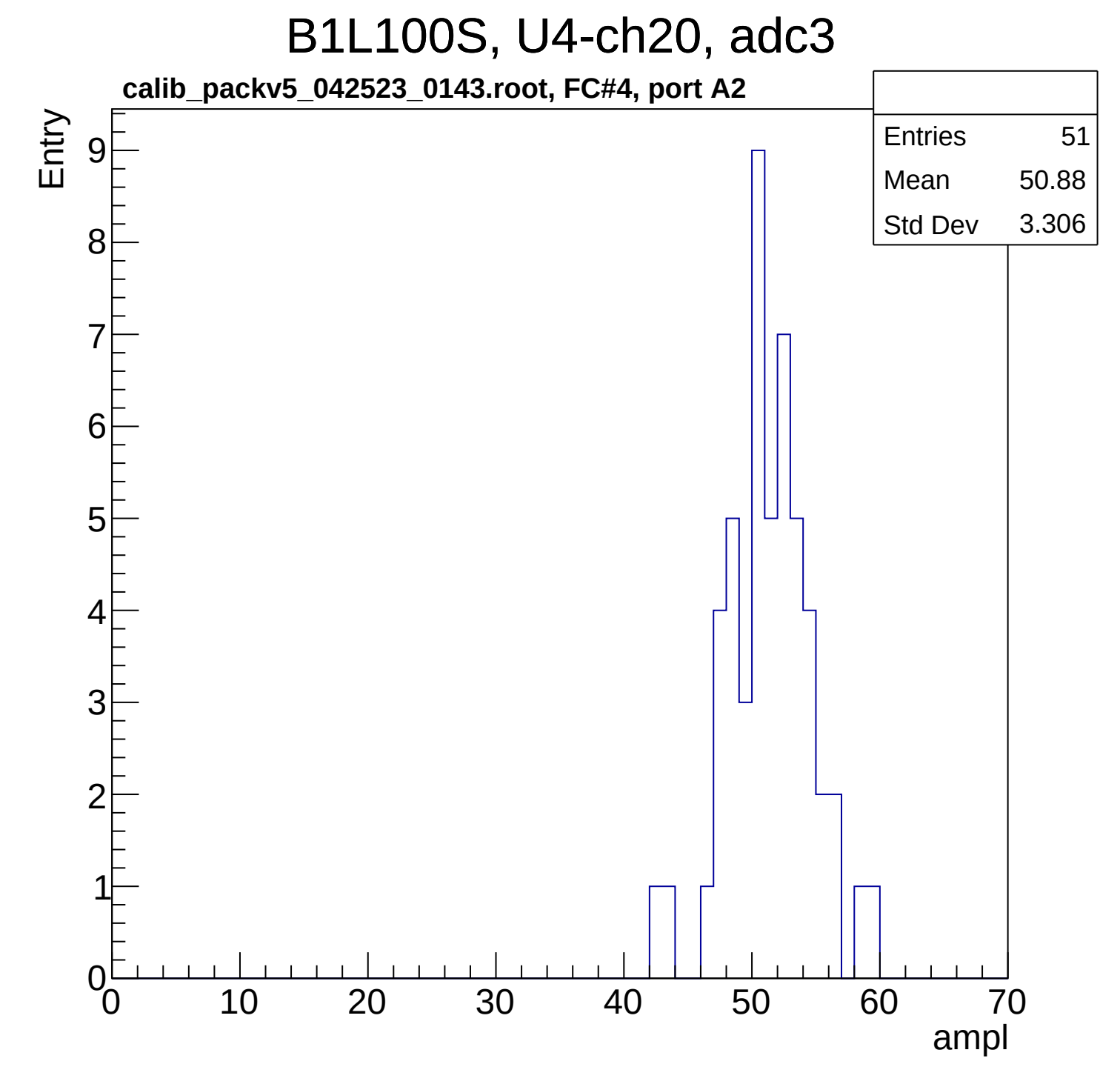

B1L100S, U4-ch19, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 61
Std Dev 2.828
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

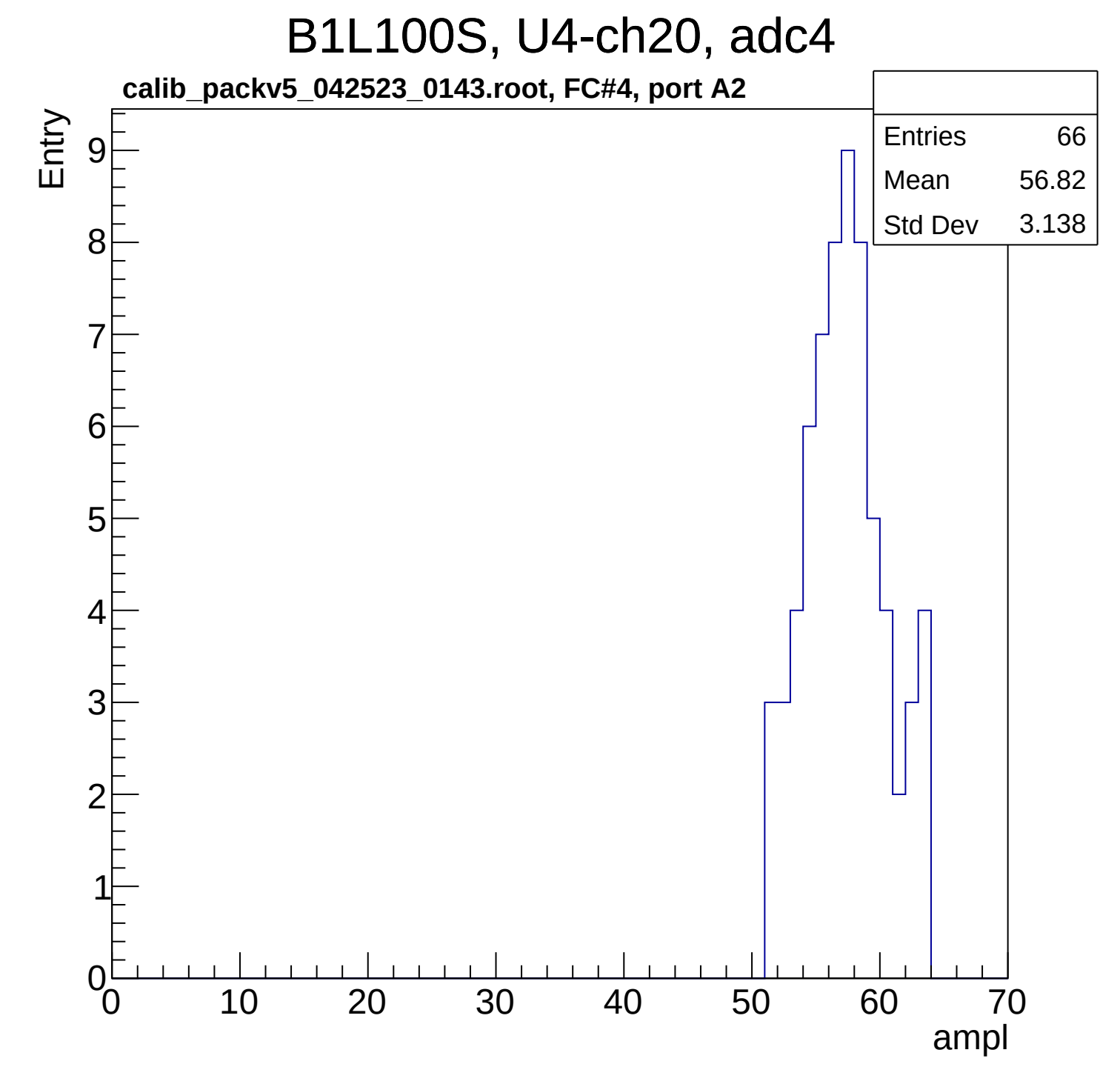

B1L100S, U4-ch19, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

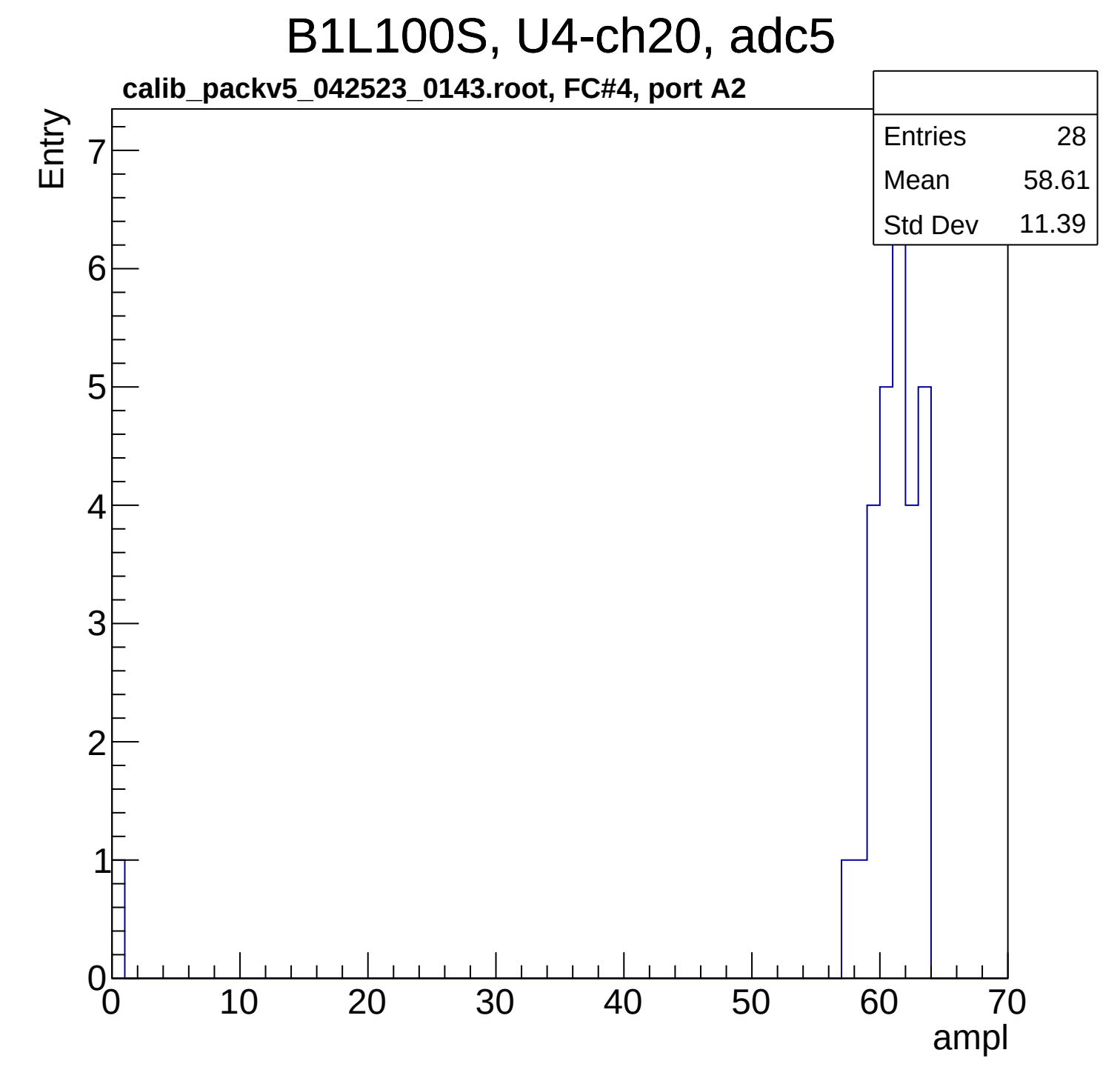

B1L100S, U4-ch20, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 30.38
Std Dev 5.238
Gaus mean : 31.8747
Gaus Width: 3.8253
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

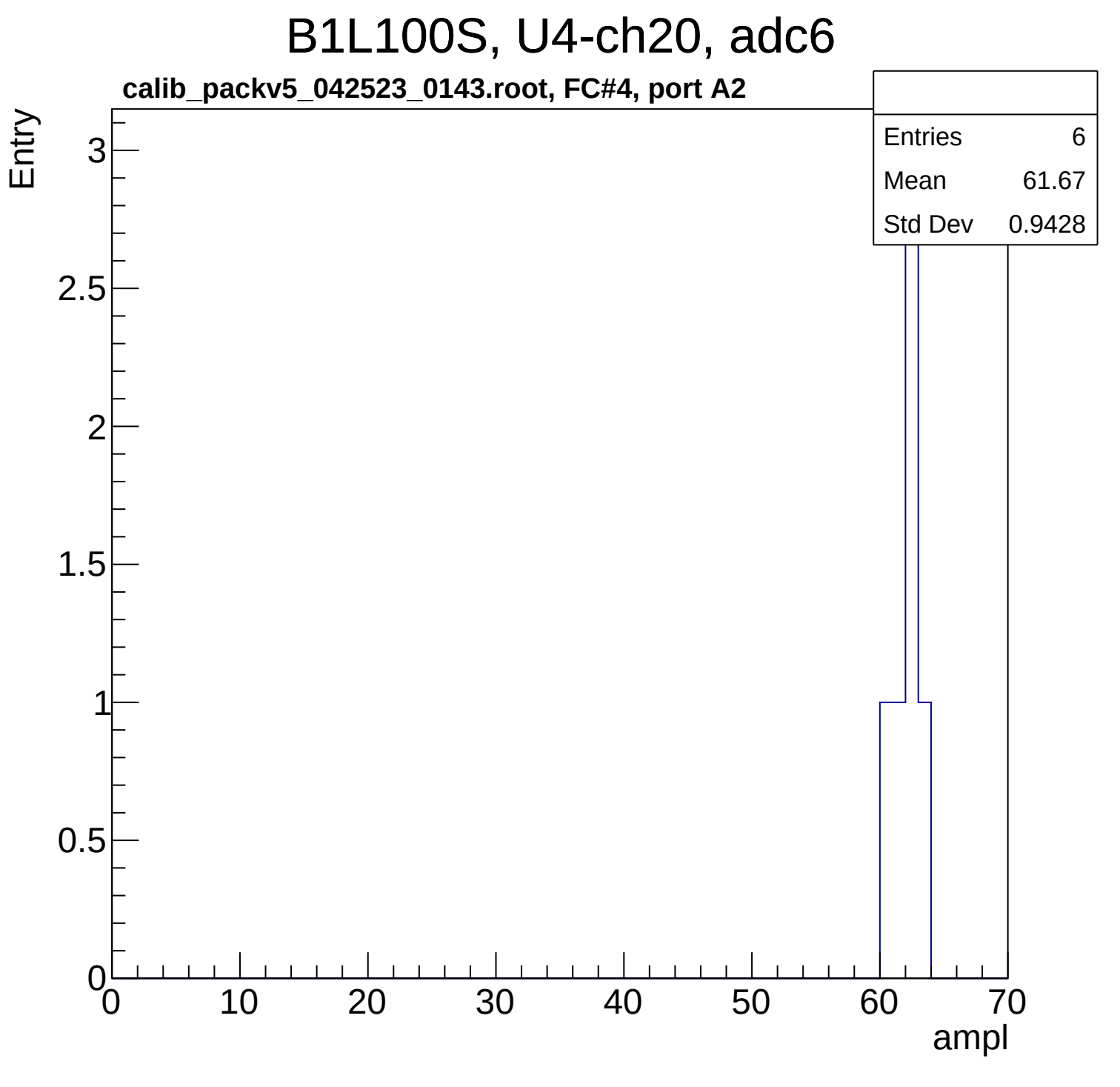

B1L100S, U4-ch20, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 85
Mean 38.28
Std Dev 3.718
Gaus mean : 38.9012
Gaus Width: 4.2251
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

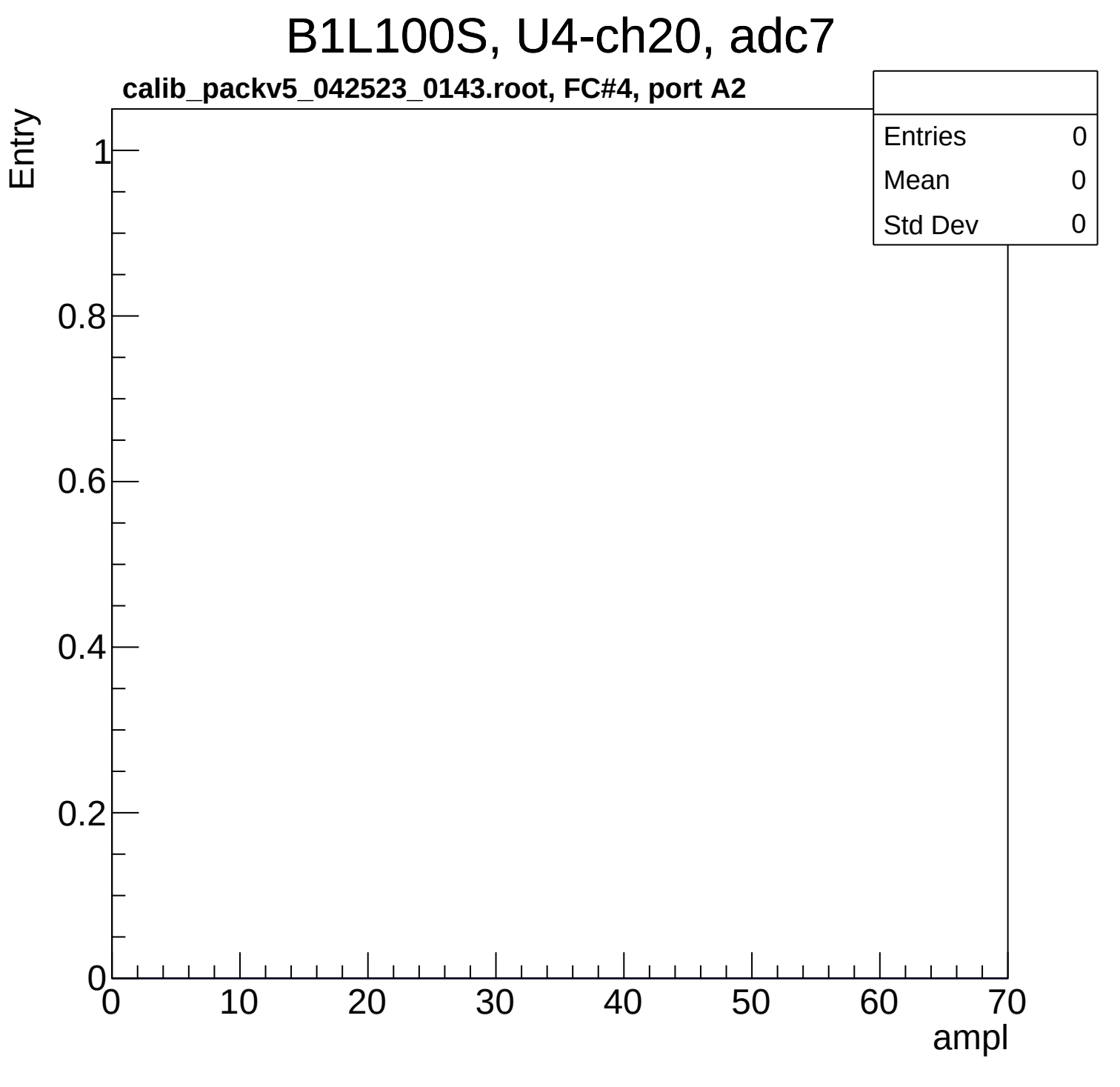

B1L100S, U4-ch20, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 45.52
Std Dev 3.471
Gaus mean : 45.9861
Gaus Width: 3.0883
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

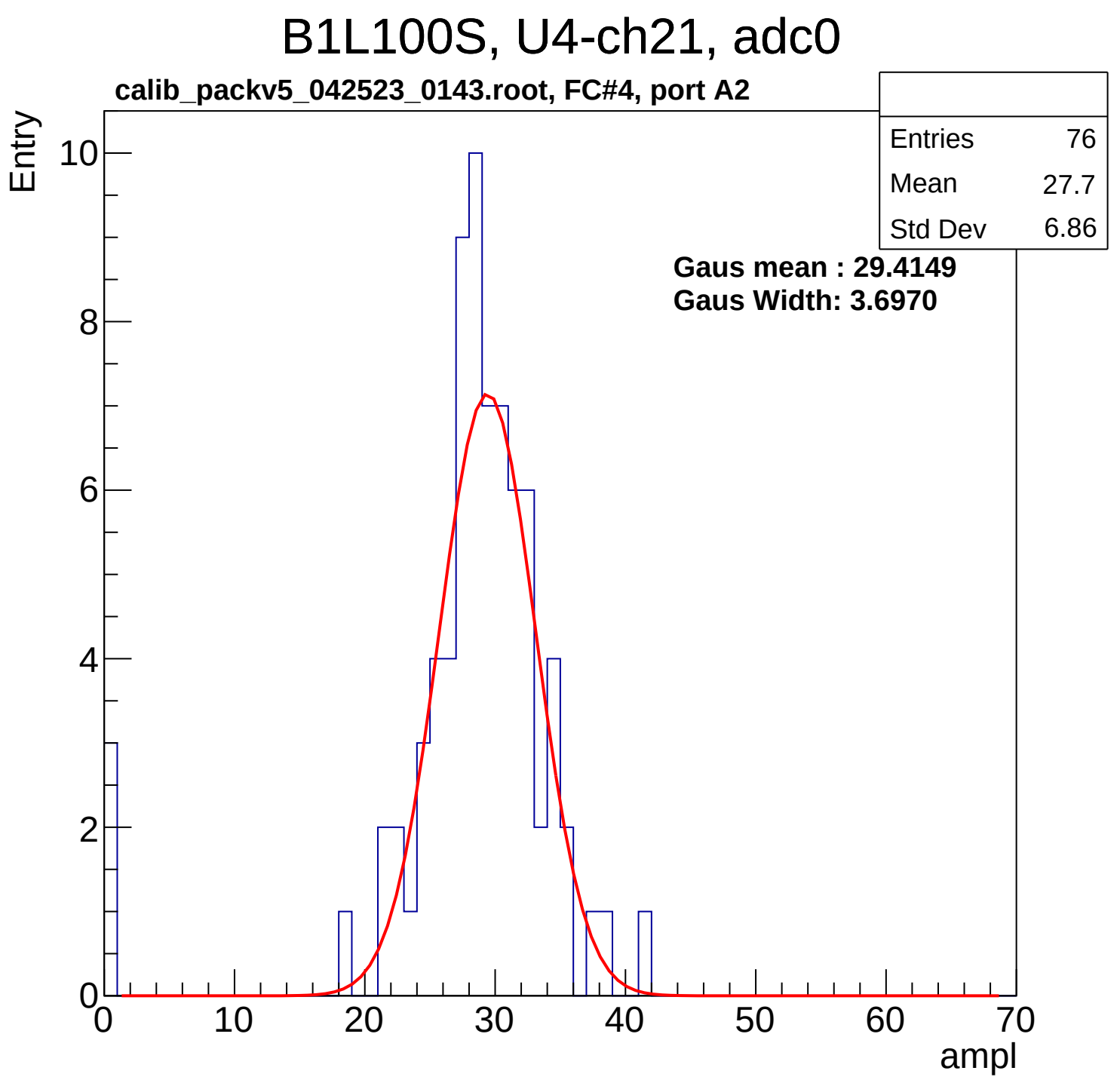

B1L100S, U4-ch20, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 50.88
Std Dev 3.306
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

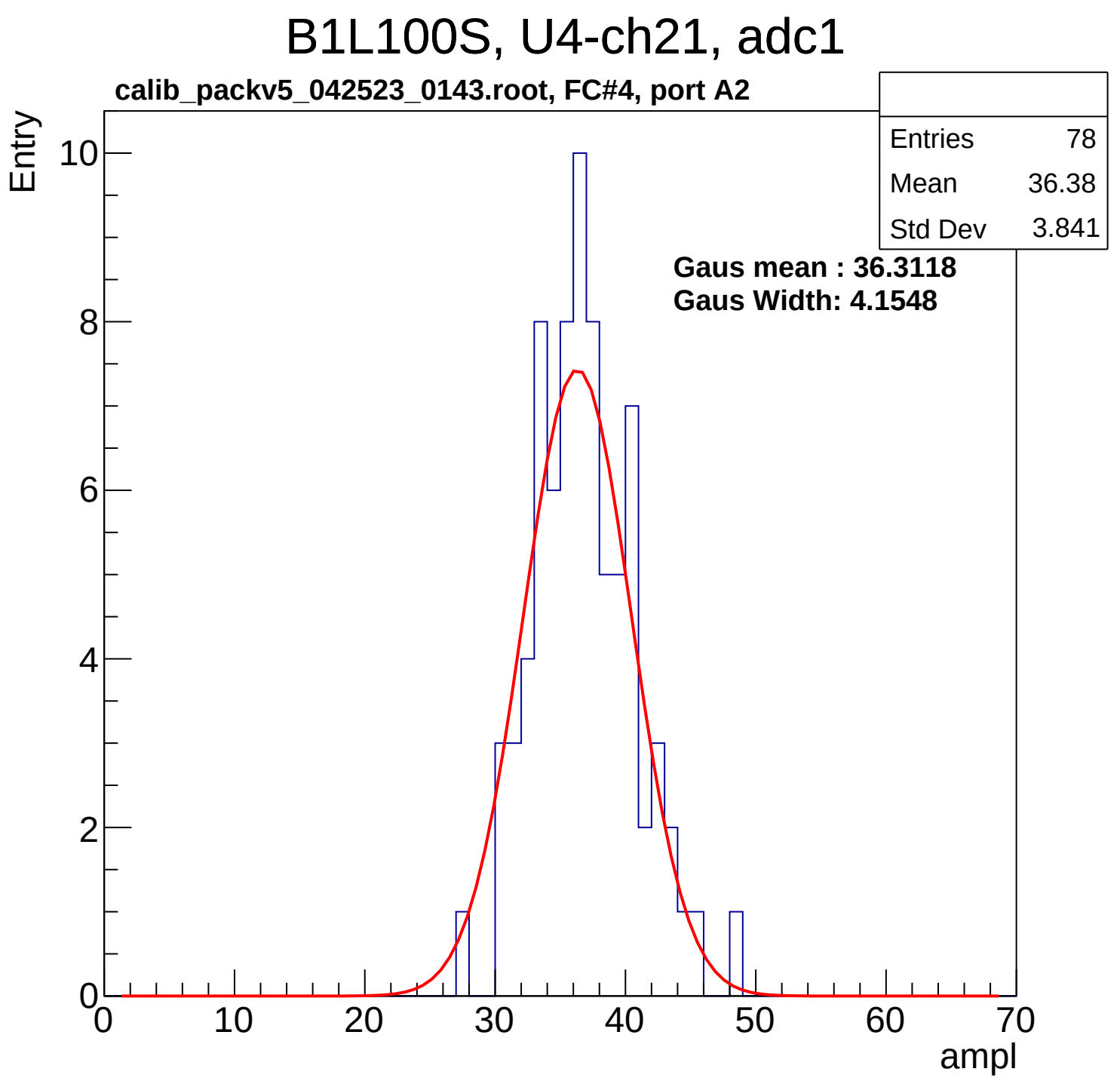

B1L100S, U4-ch20, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 56.82
Std Dev 3.138
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

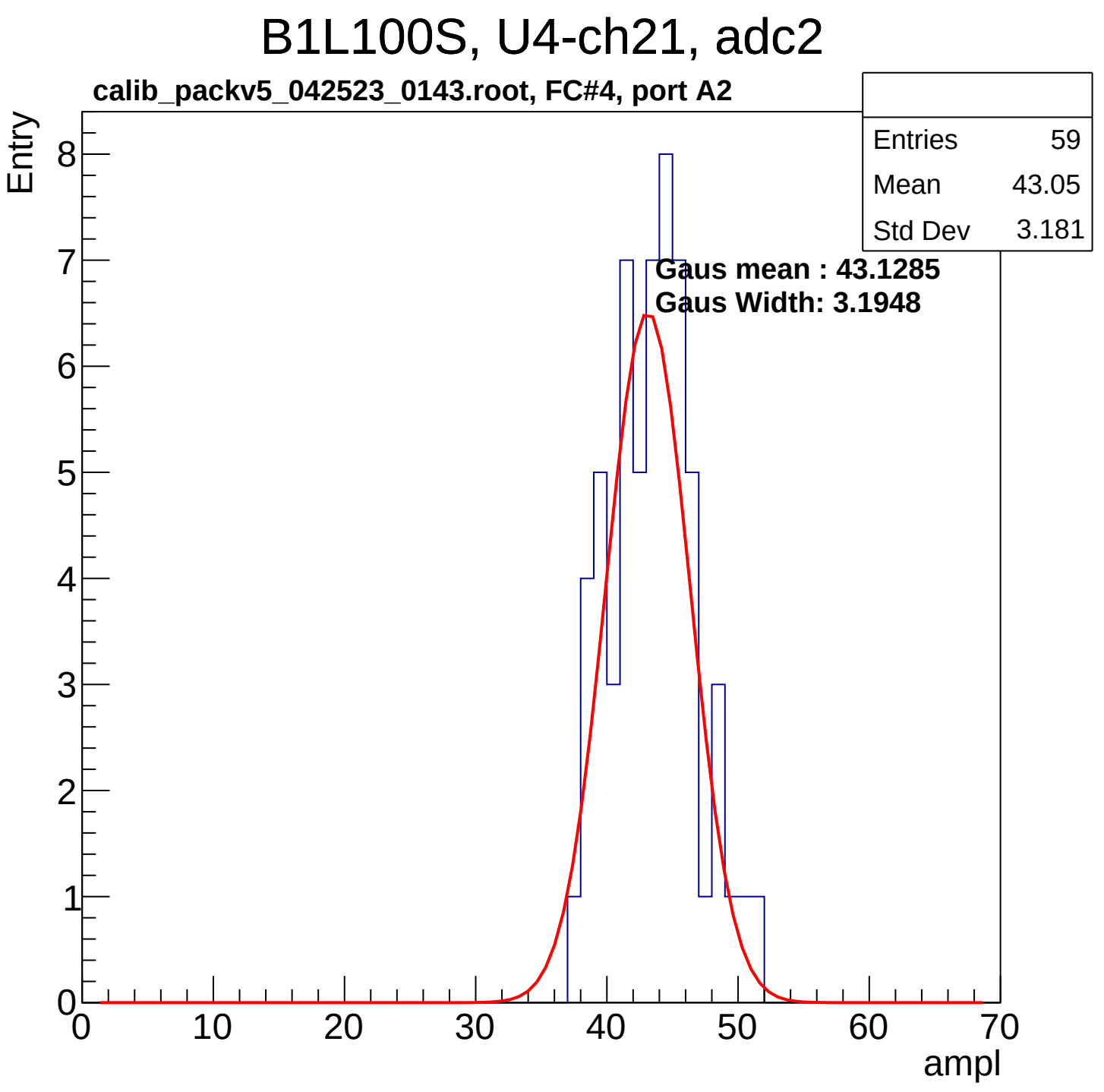

B1L100S, U4-ch20, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 28
Mean 58.61
Std Dev 11.39
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

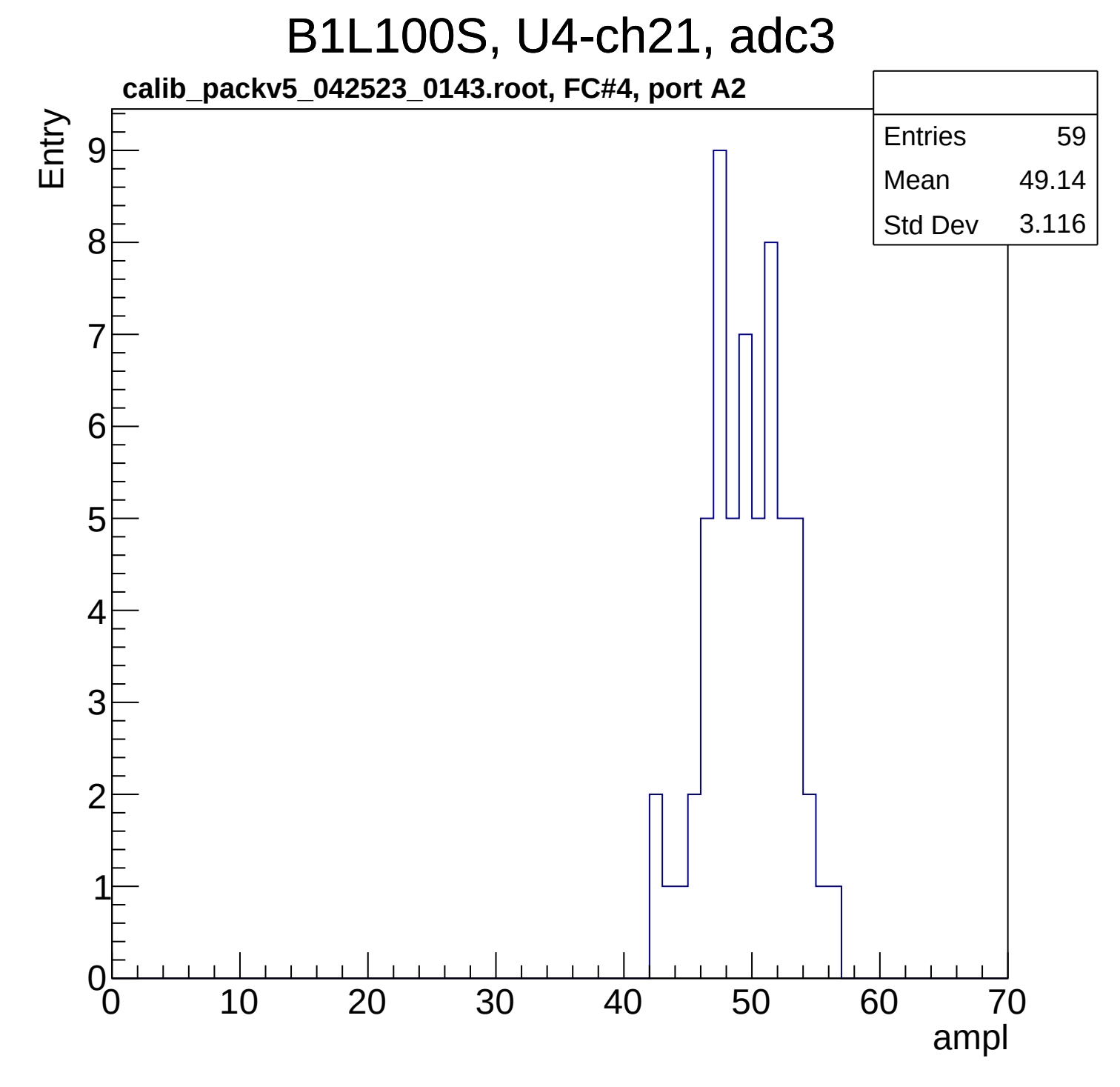

B1L100S, U4-ch20, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 61.67
Std Dev 0.9428
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

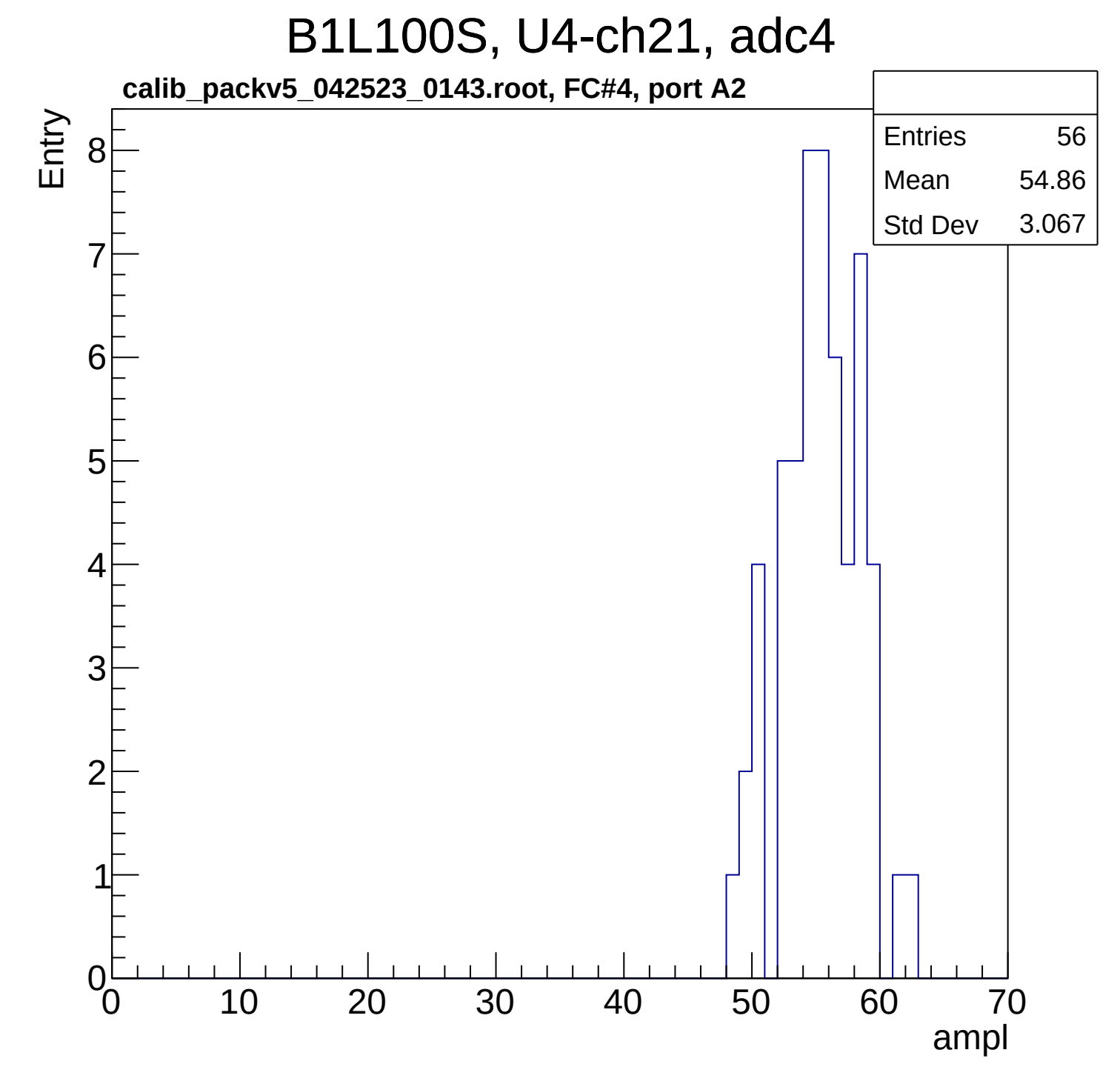

B1L100S, U4-ch20, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

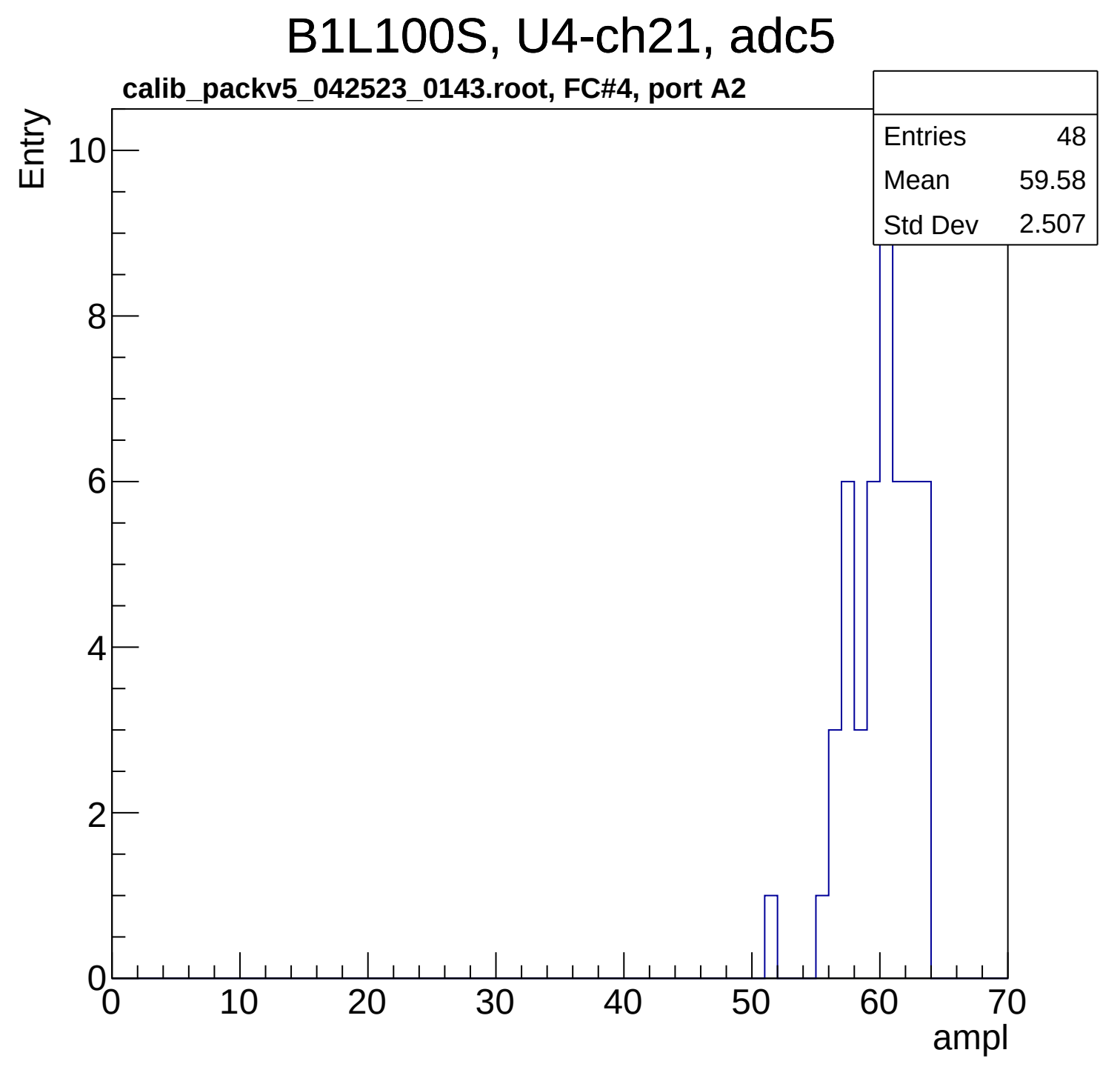

B1L100S, U4-ch21, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 27.7
Std Dev 6.86
Gaus mean : 29.4149
Gaus Width: 3.6970
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

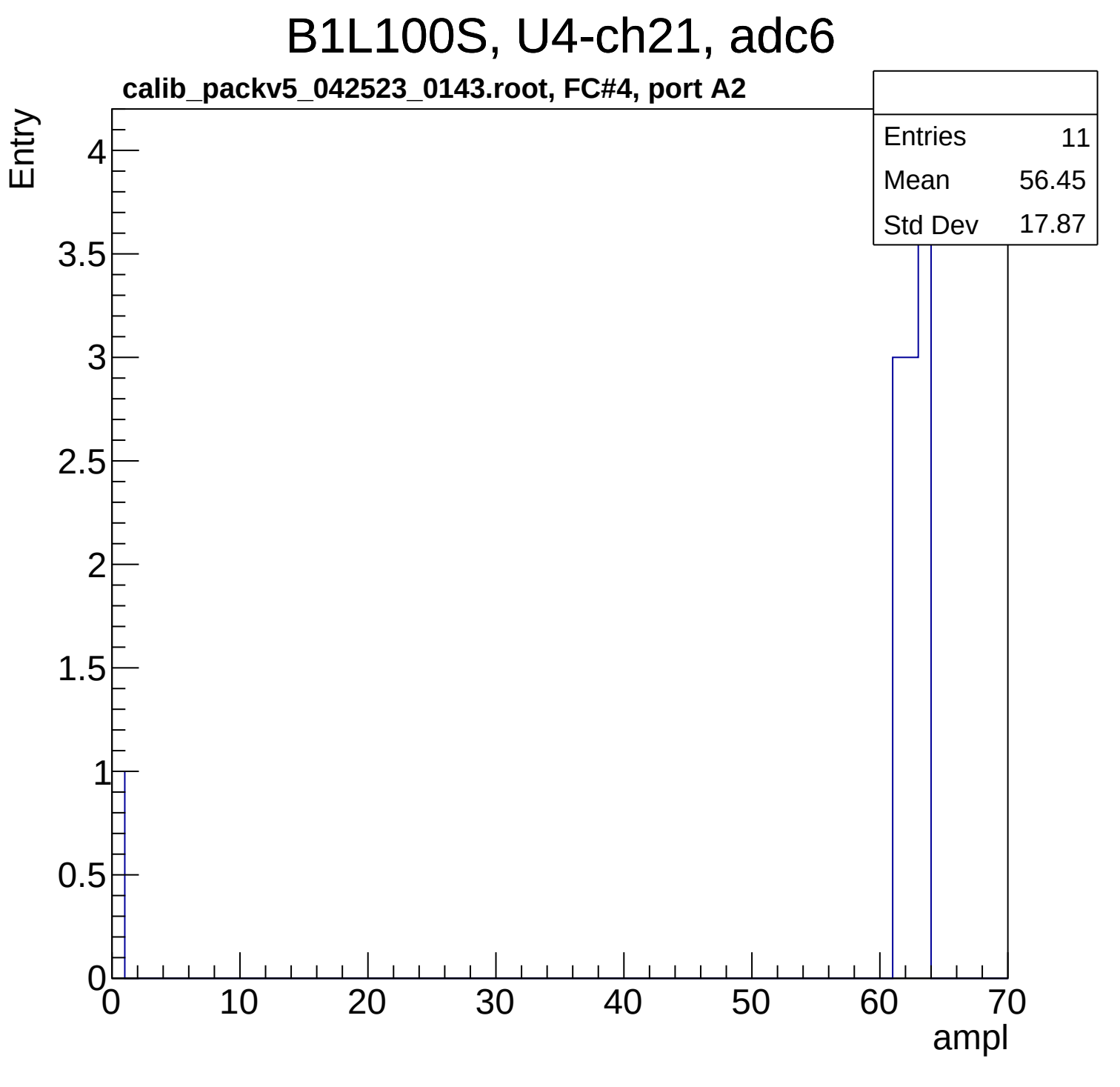

B1L100S, U4-ch21, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 36.38
Std Dev 3.841
Gaus mean : 36.3118
Gaus Width: 4.1548
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

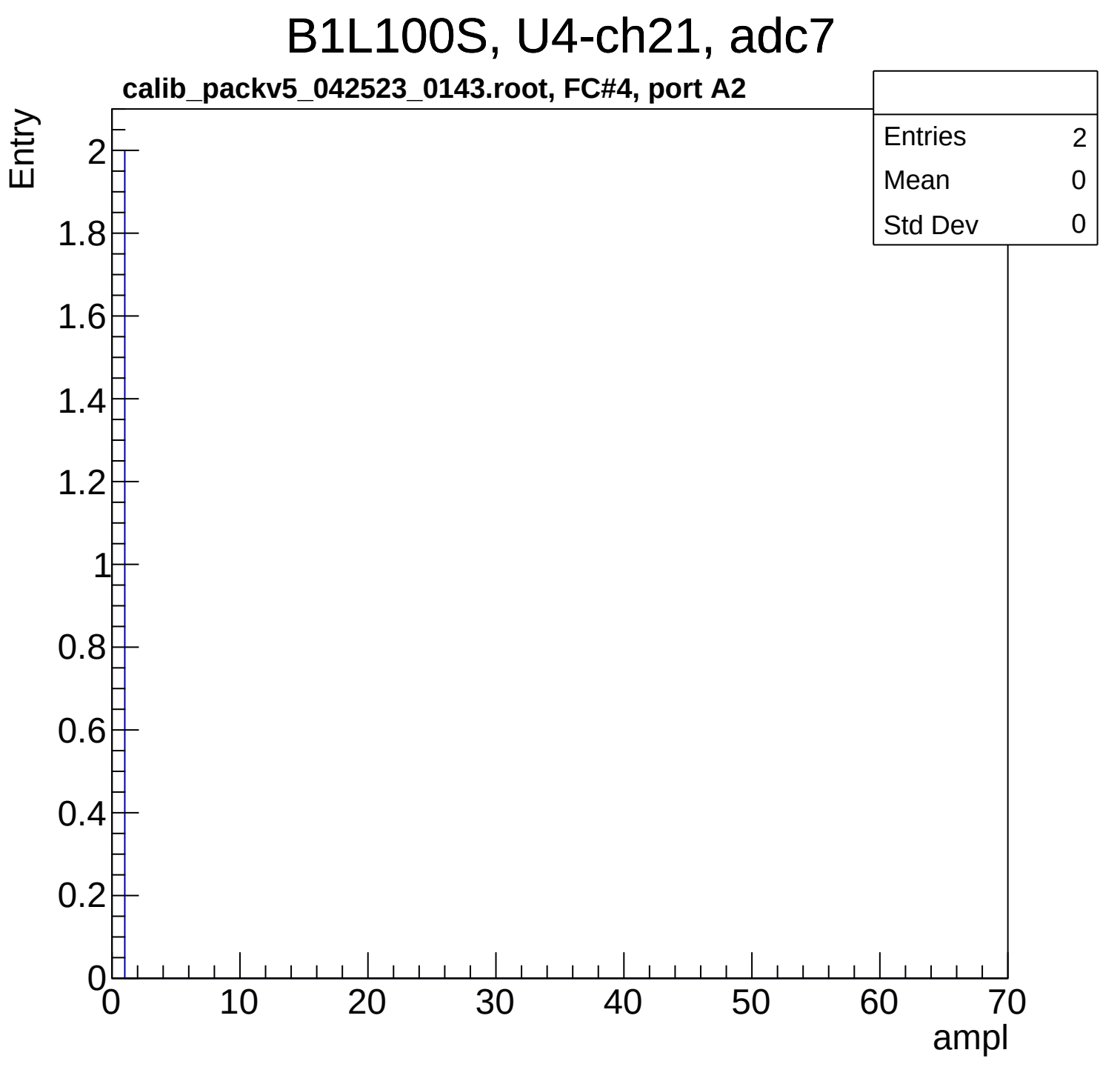

B1L100S, U4-ch21, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 43.05
Std Dev 3.181
Gaus mean : 43.1285
Gaus Width: 3.1948
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

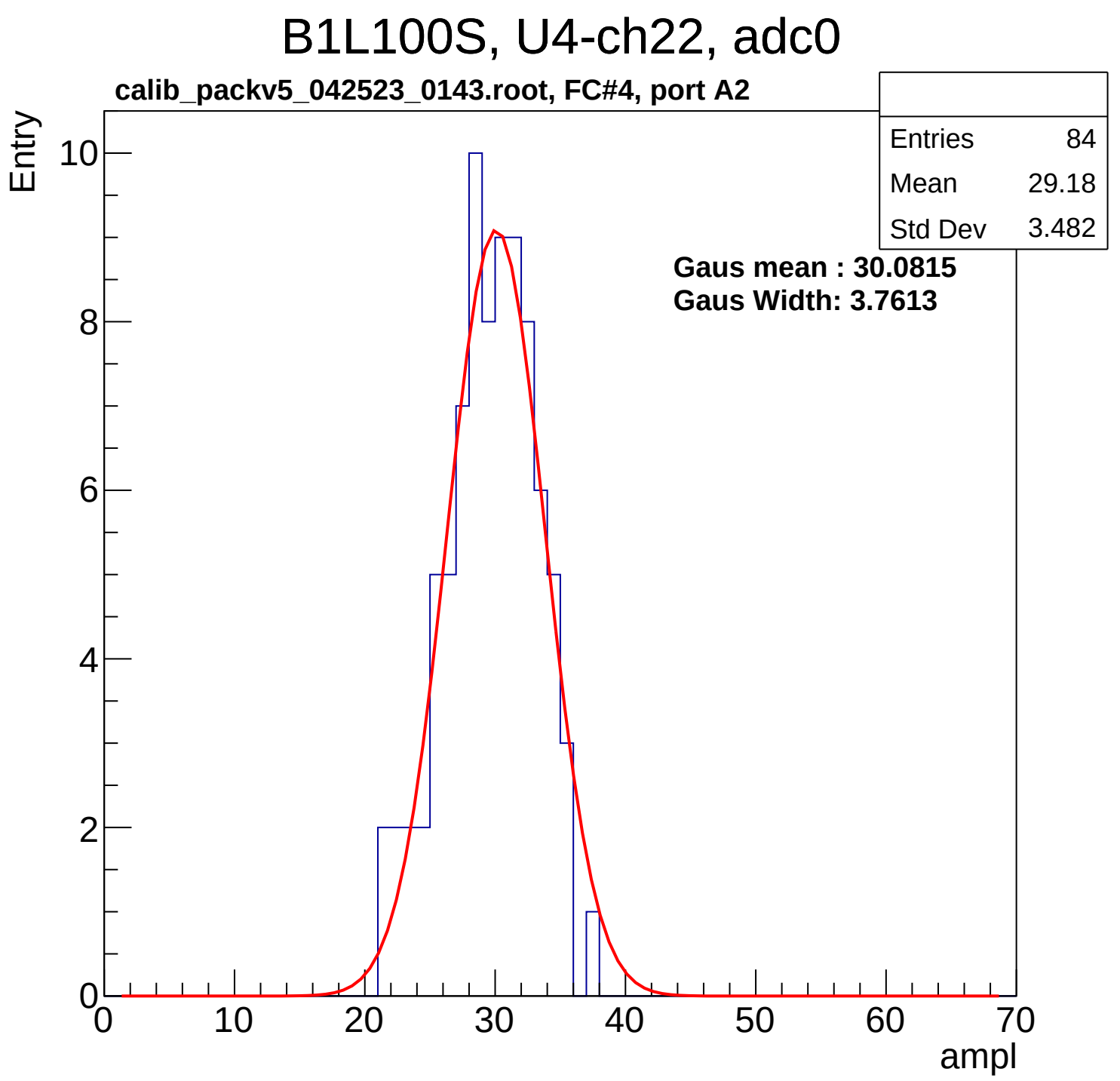

B1L100S, U4-ch21, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 49.14
Std Dev 3.116
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

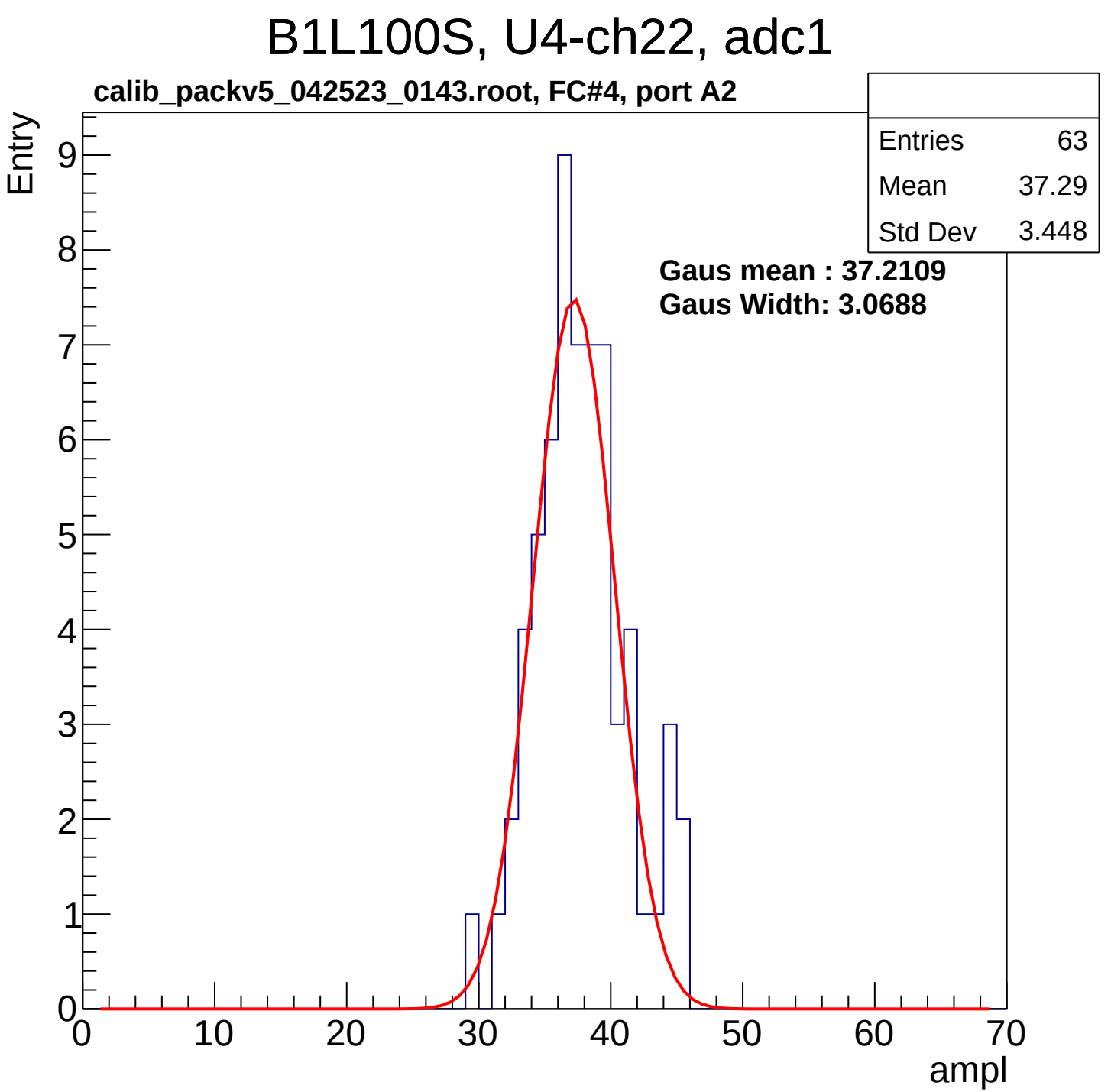

B1L100S, U4-ch21, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 54.86
Std Dev 3.067
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

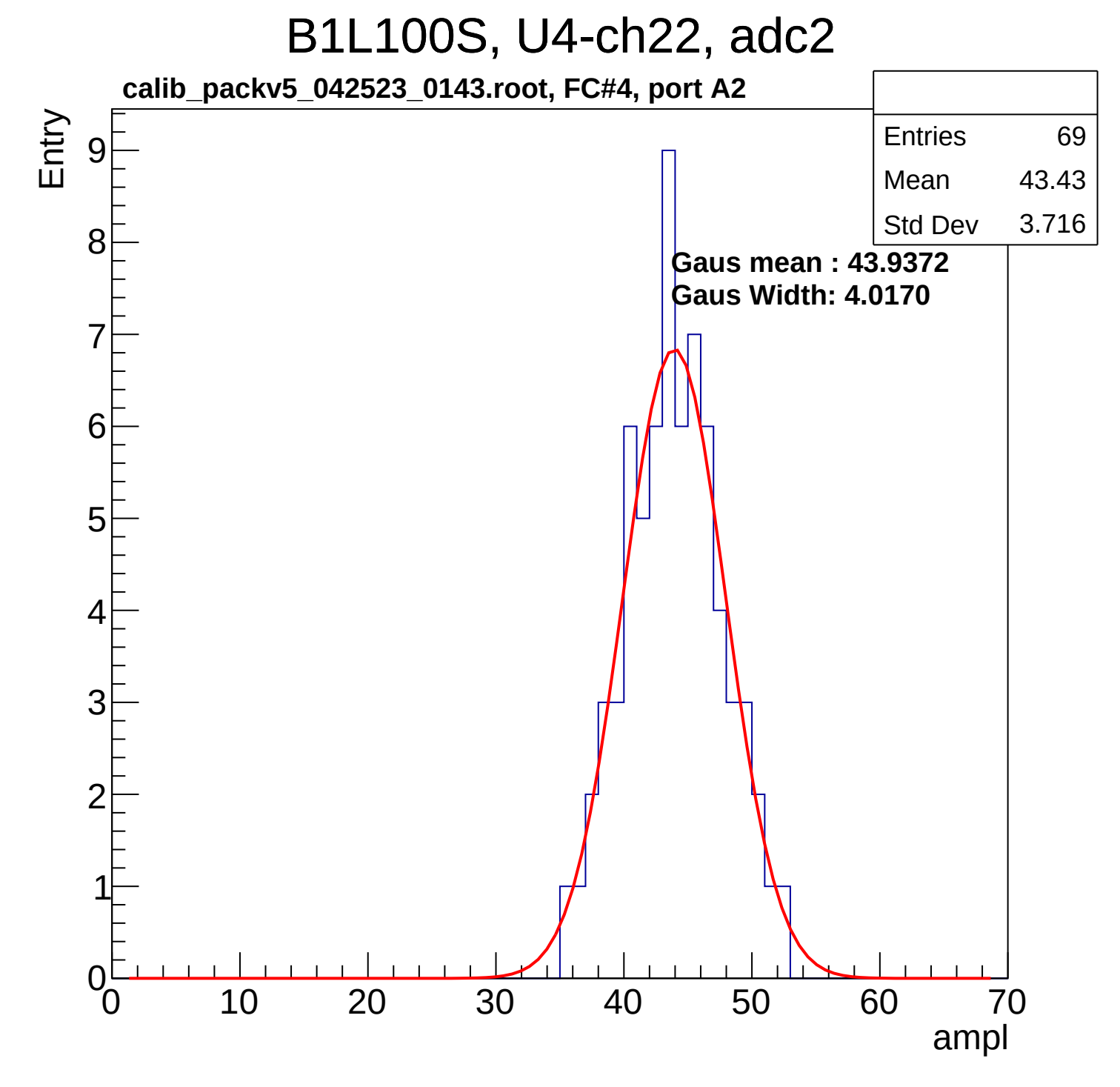

B1L100S, U4-ch21, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 59.58
Std Dev 2.507
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

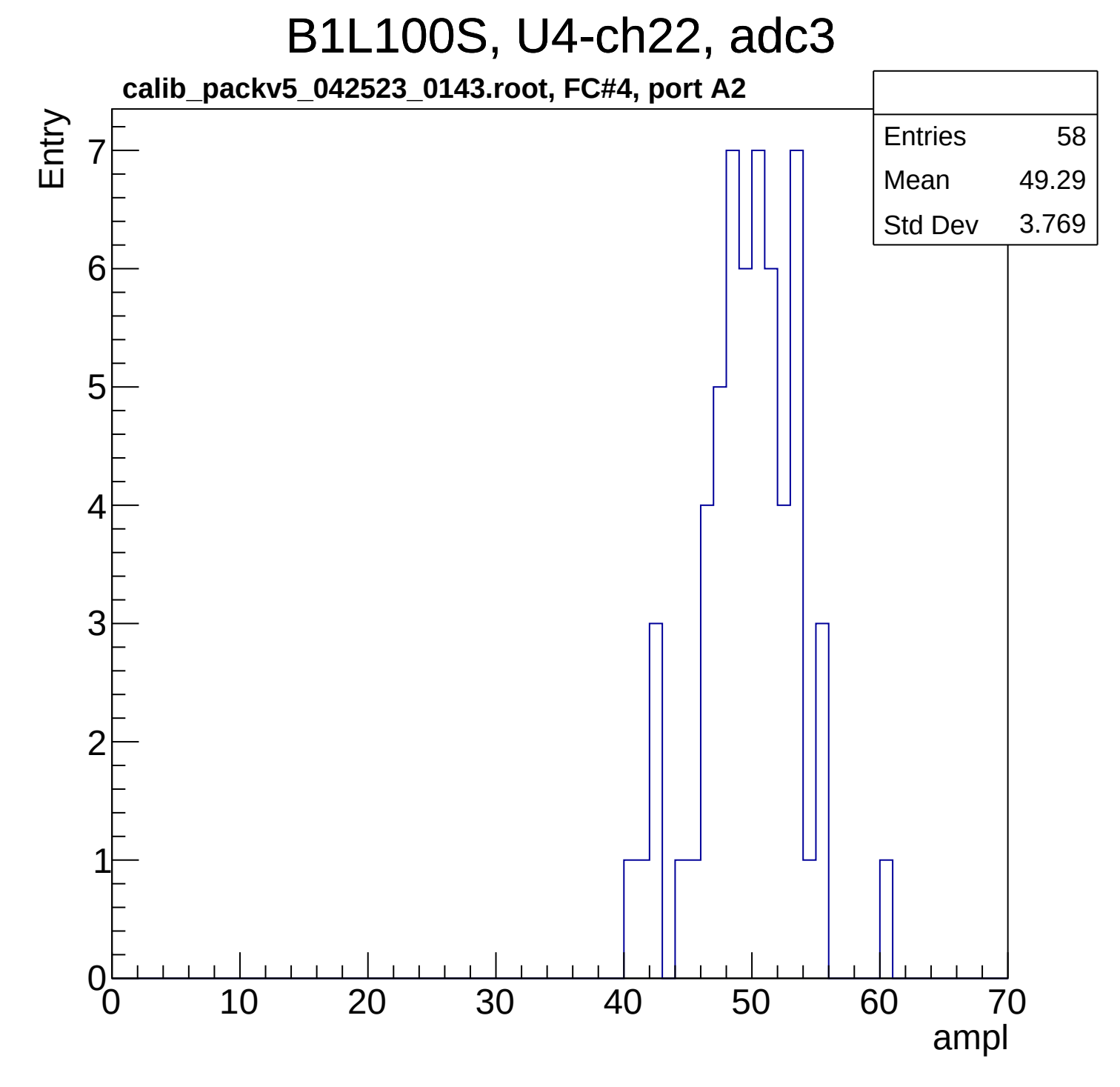

B1L100S, U4-ch21, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 56.45
Std Dev 17.87
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

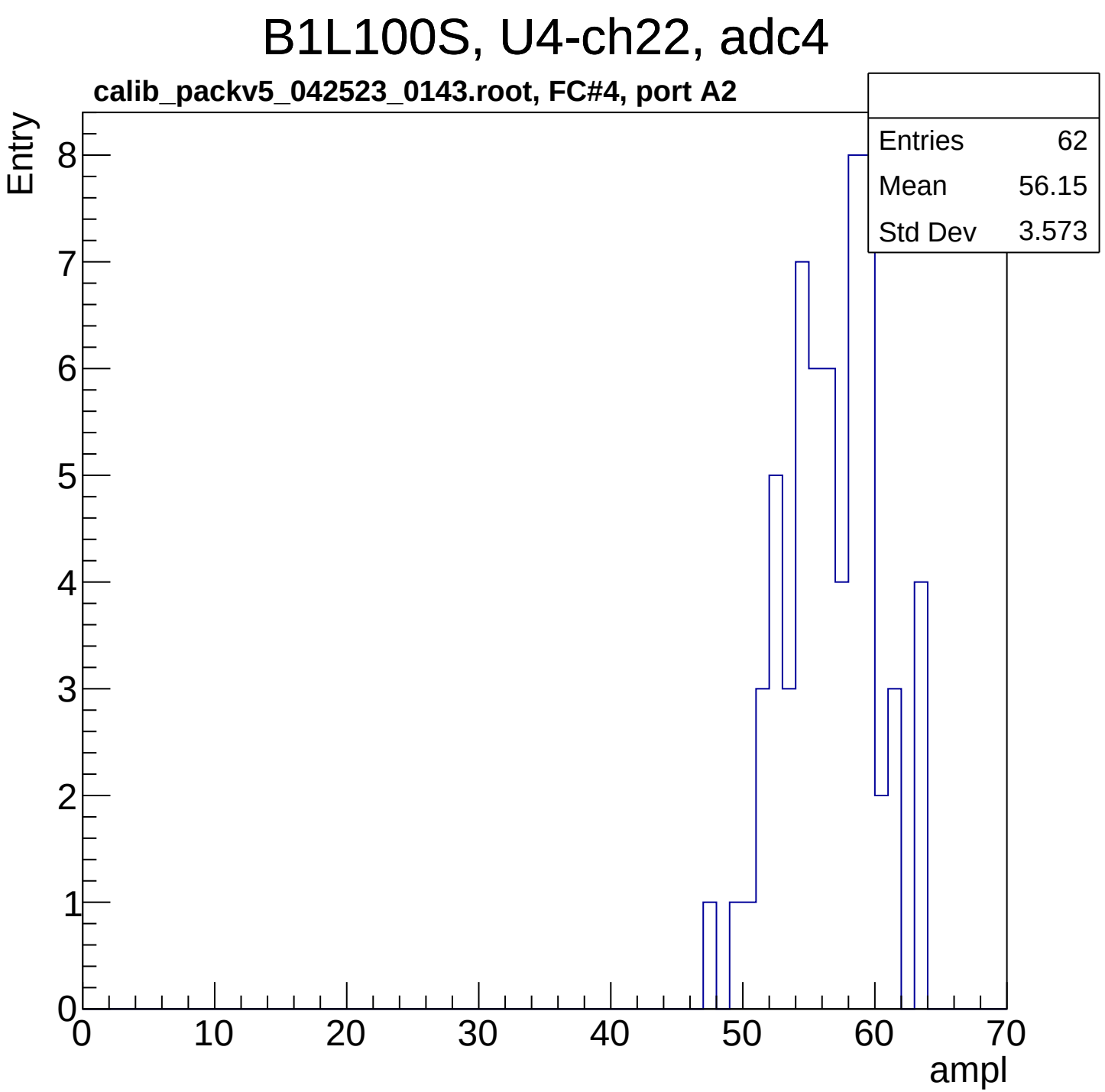

B1L100S, U4-ch21, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

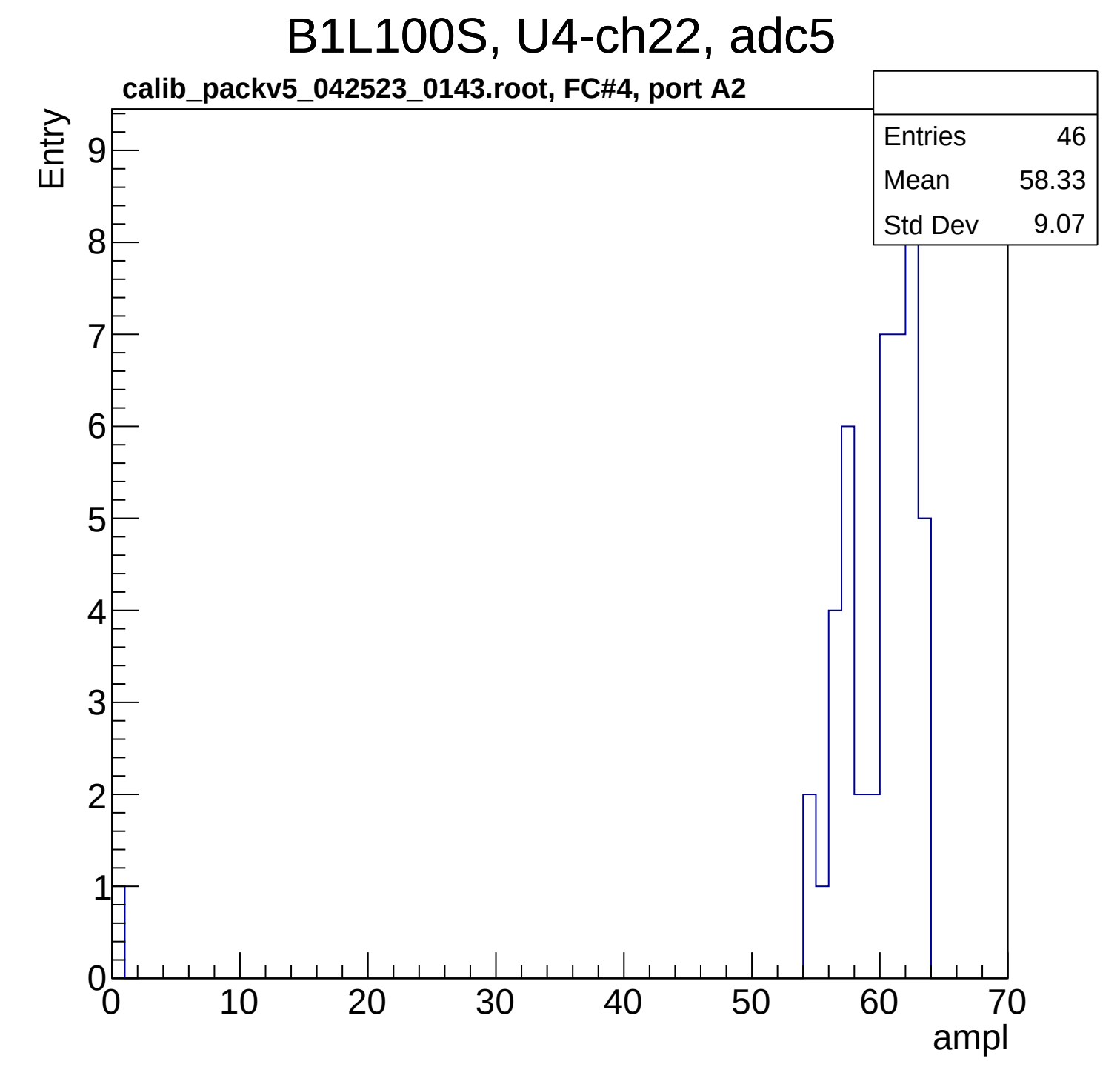

B1L100S, U4-ch22, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 84
Mean 29.18
Std Dev 3.482
Gaus mean : 30.0815
Gaus Width: 3.7613
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

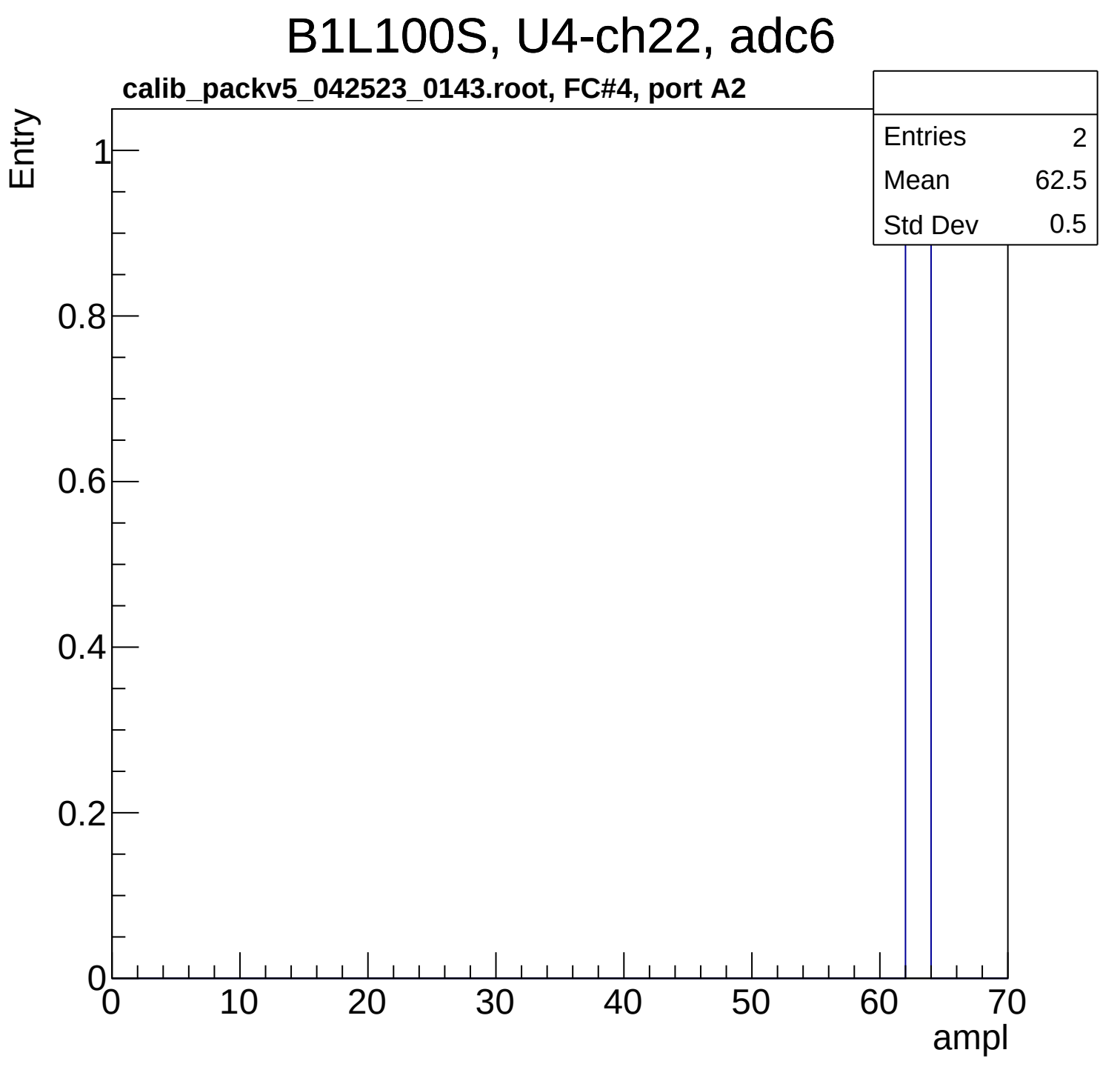

B1L100S, U4-ch22, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 37.29
Std Dev 3.448
Gaus mean : 37.2109
Gaus Width: 3.0688
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

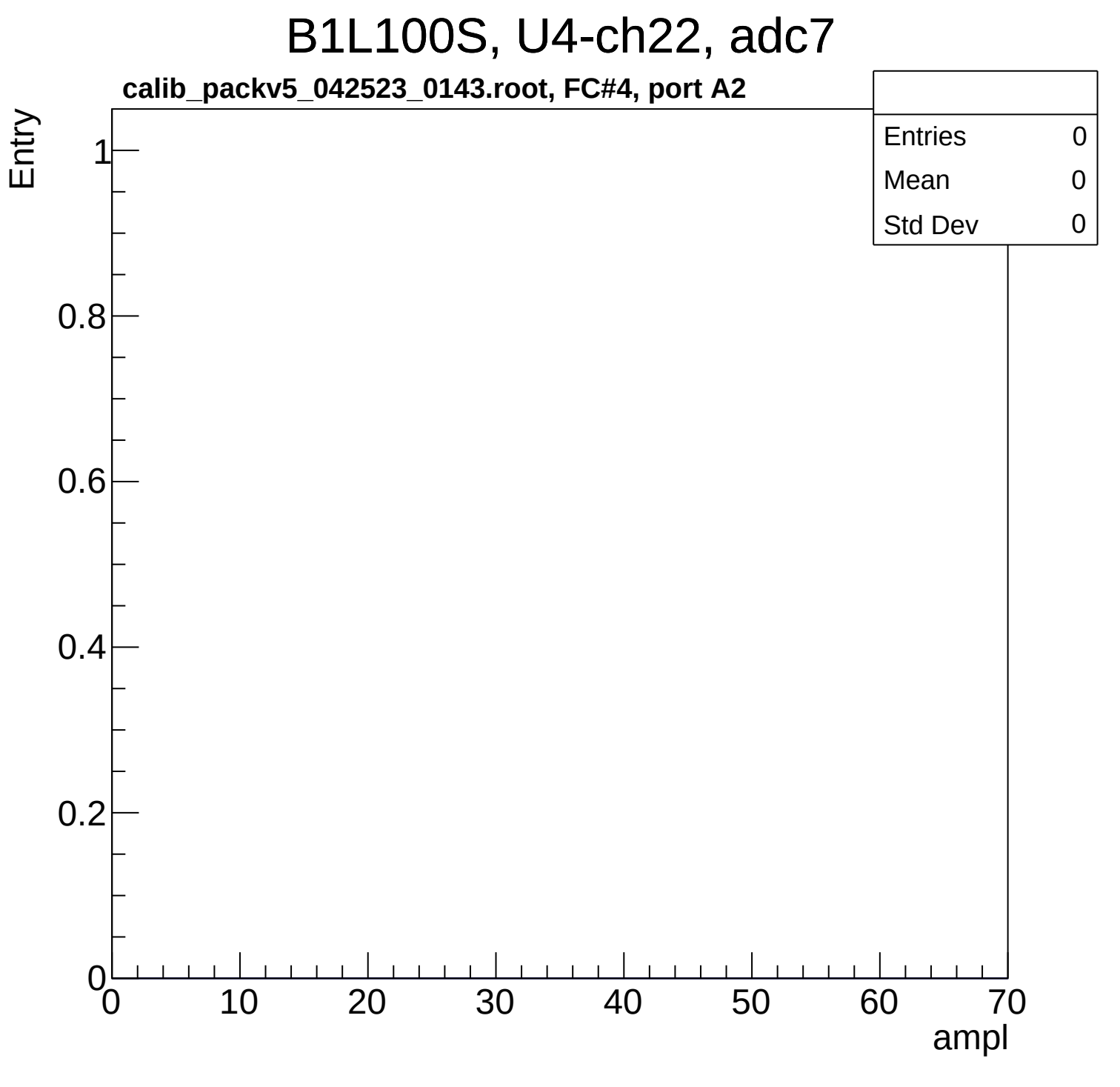

B1L100S, U4-ch22, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 43.43
Std Dev 3.716
Gaus mean : 43.9372
Gaus Width: 4.0170
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

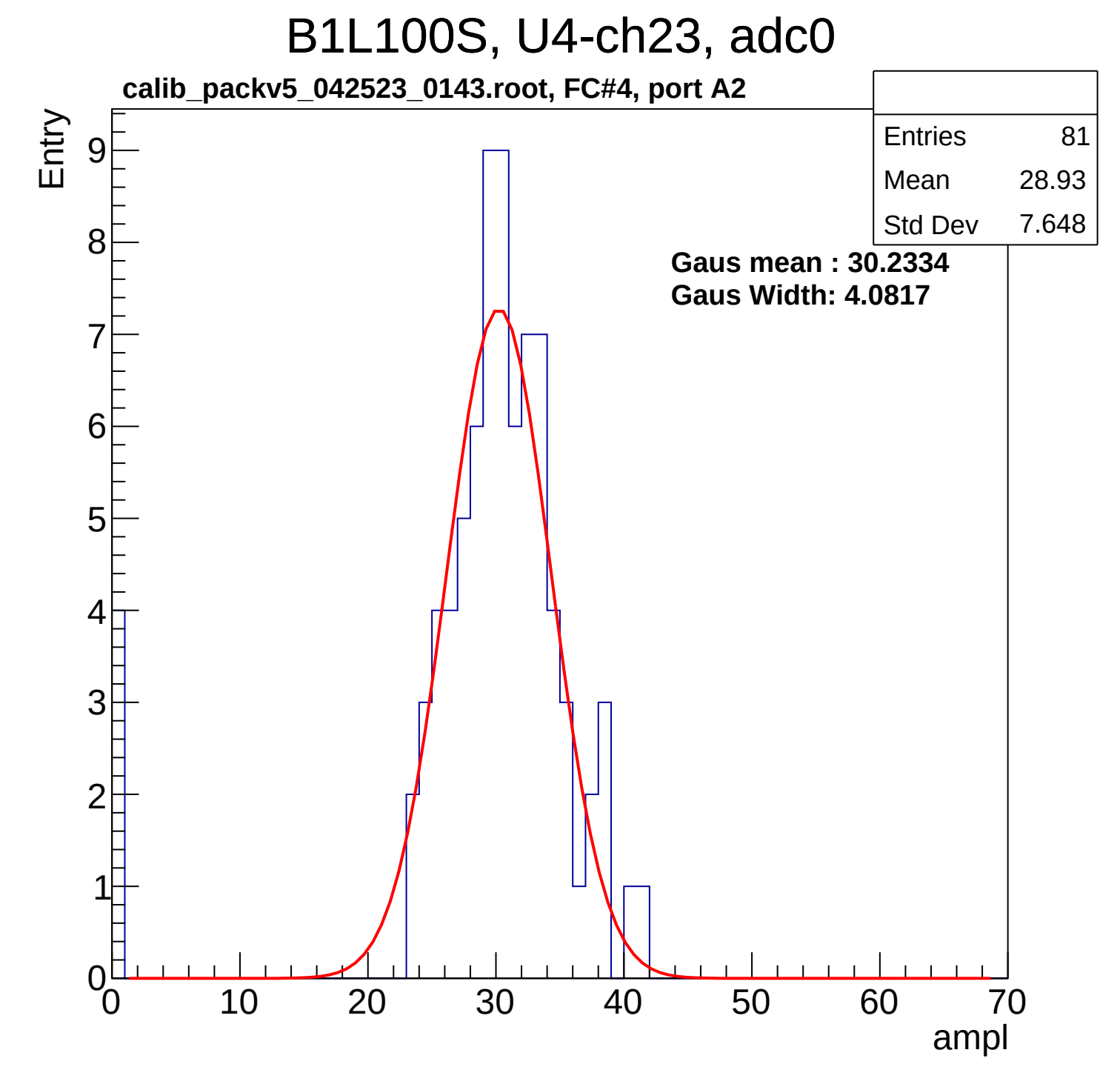

B1L100S, U4-ch22, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 49.29
Std Dev 3.769
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

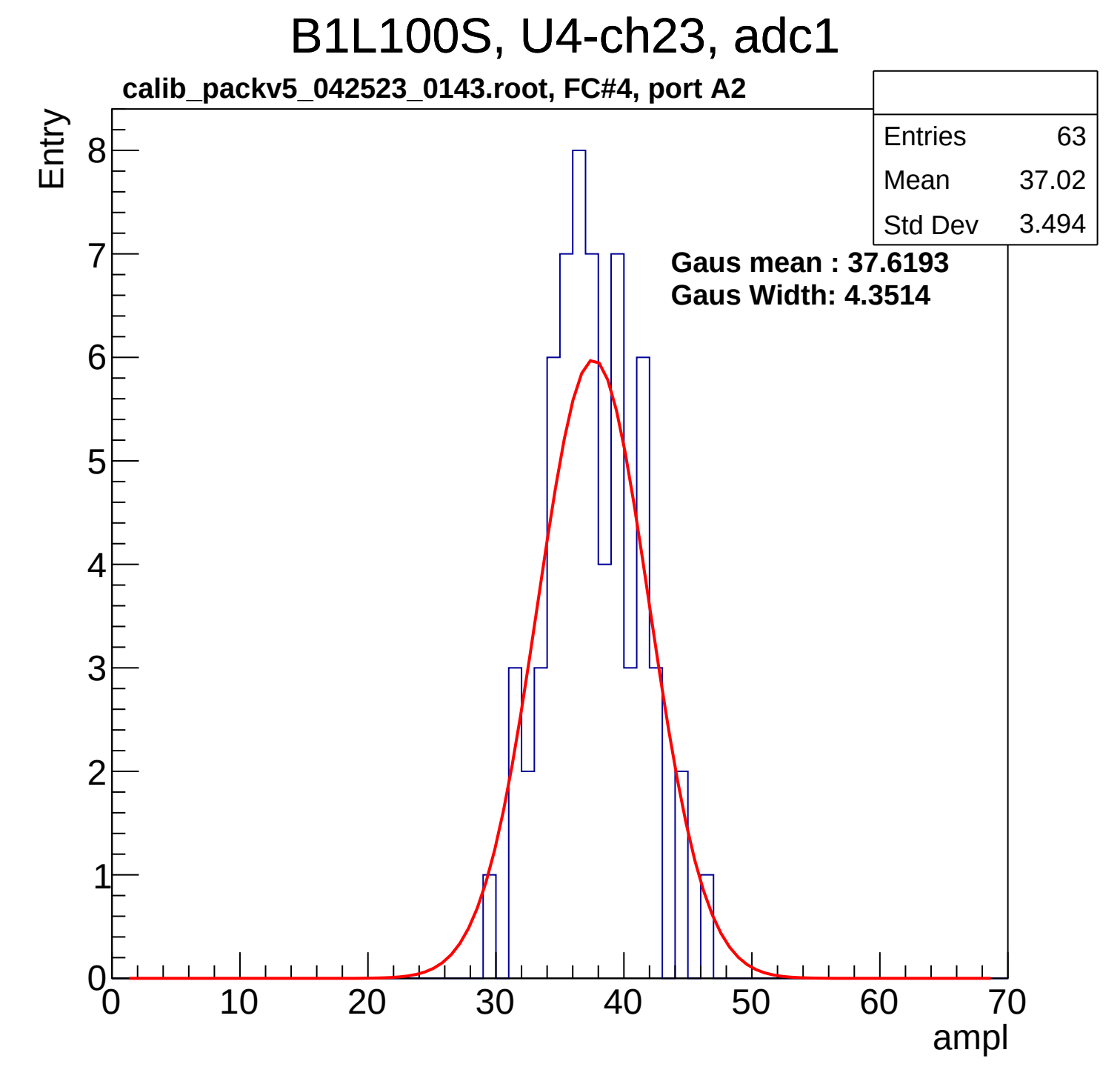

B1L100S, U4-ch22, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 56.15
Std Dev 3.573
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

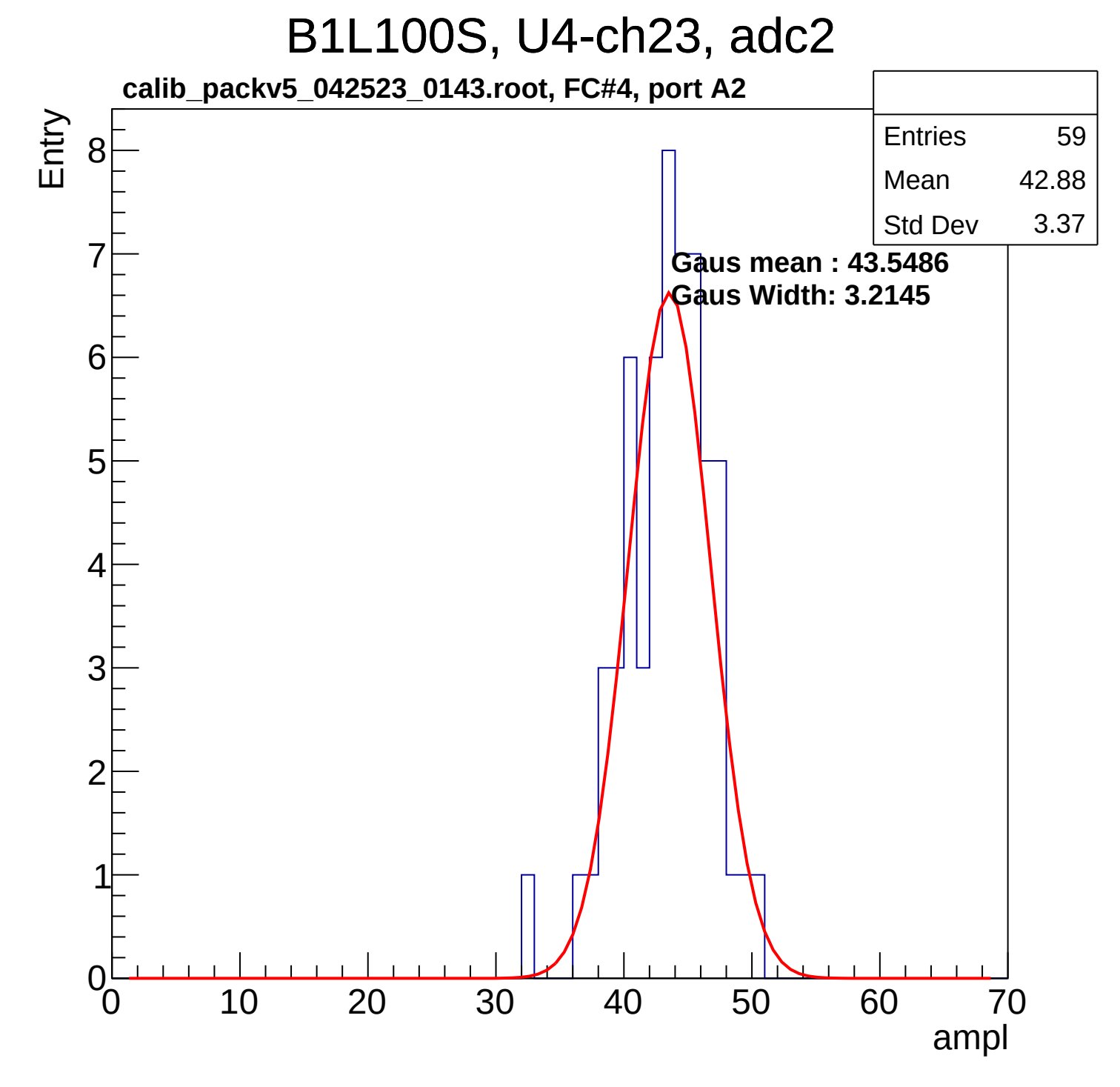

B1L100S, U4-ch22, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 58.33
Std Dev 9.07
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

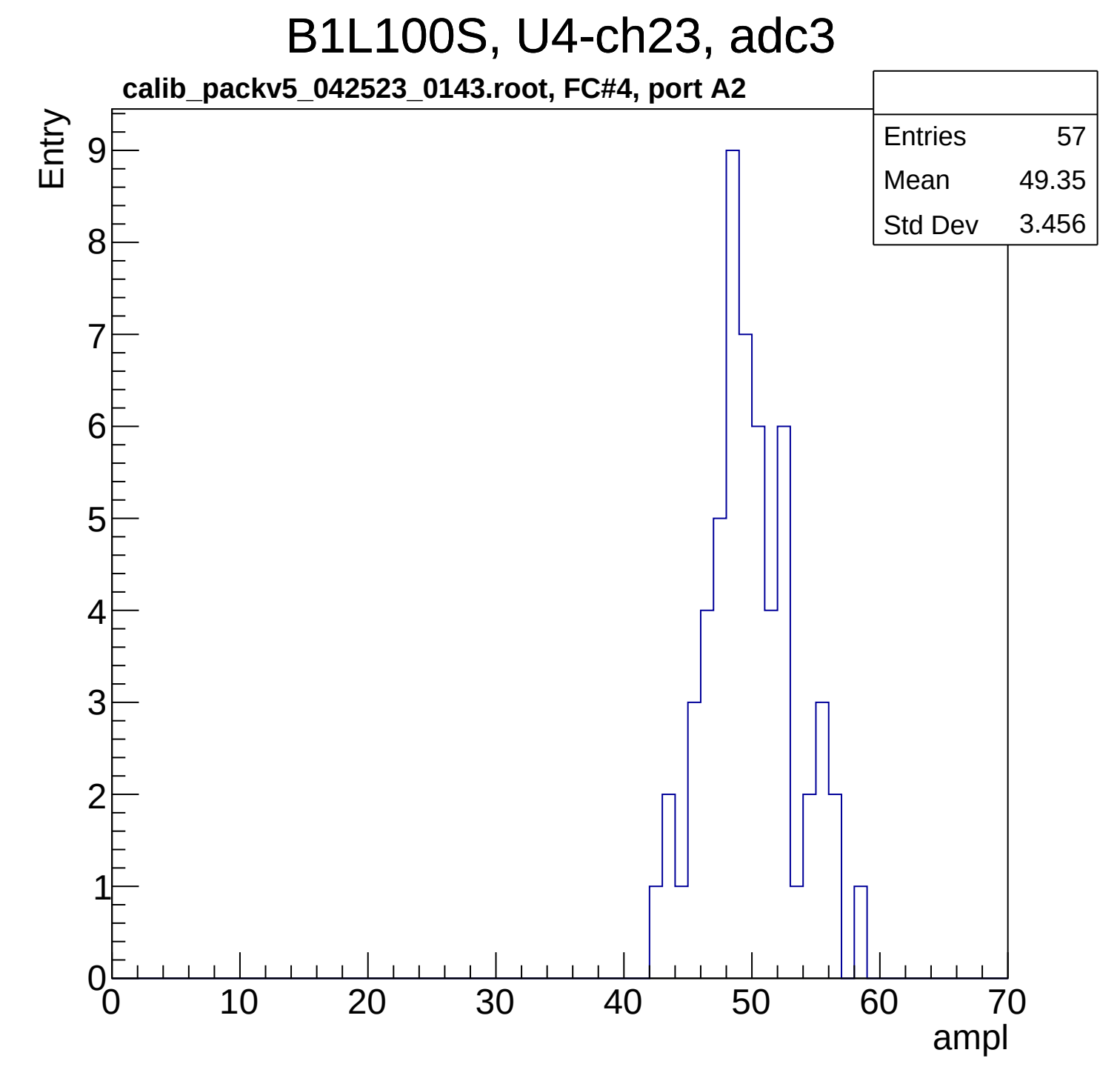

B1L100S, U4-ch22, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

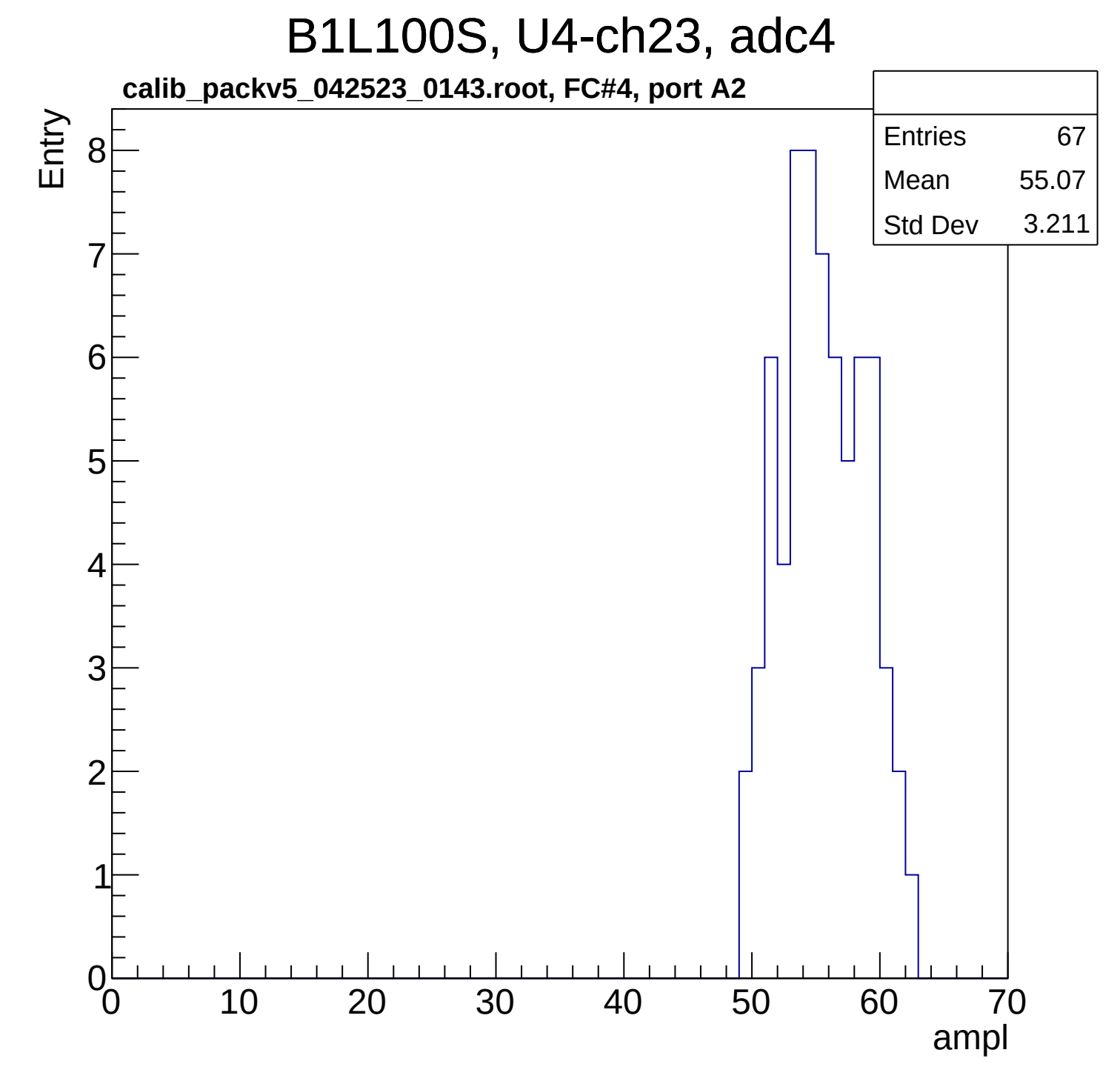

B1L100S, U4-ch22, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

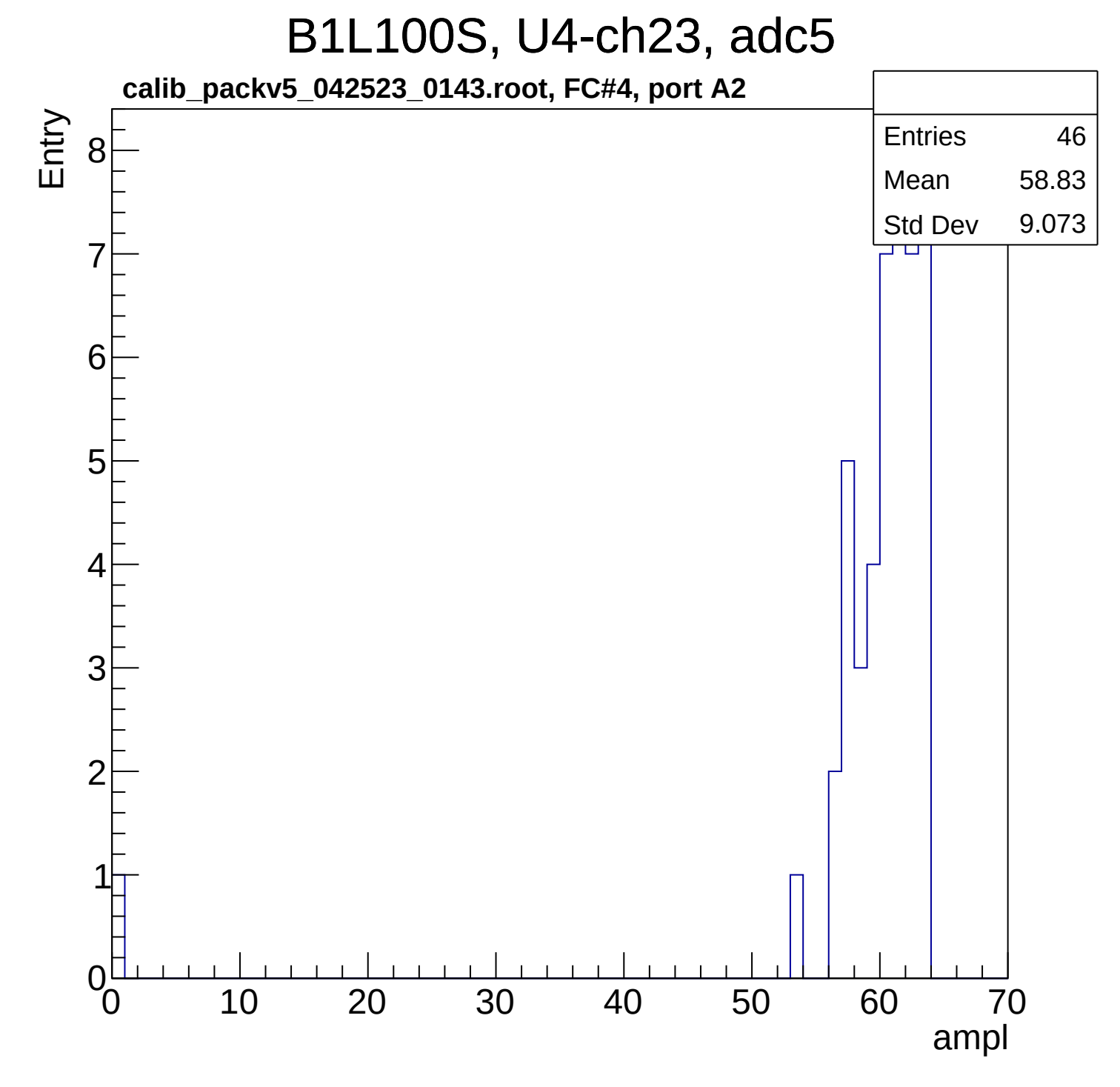

B1L100S, U4-ch23, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 28.93
Std Dev 7.648
Gaus mean : 30.2334
Gaus Width: 4.0817
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

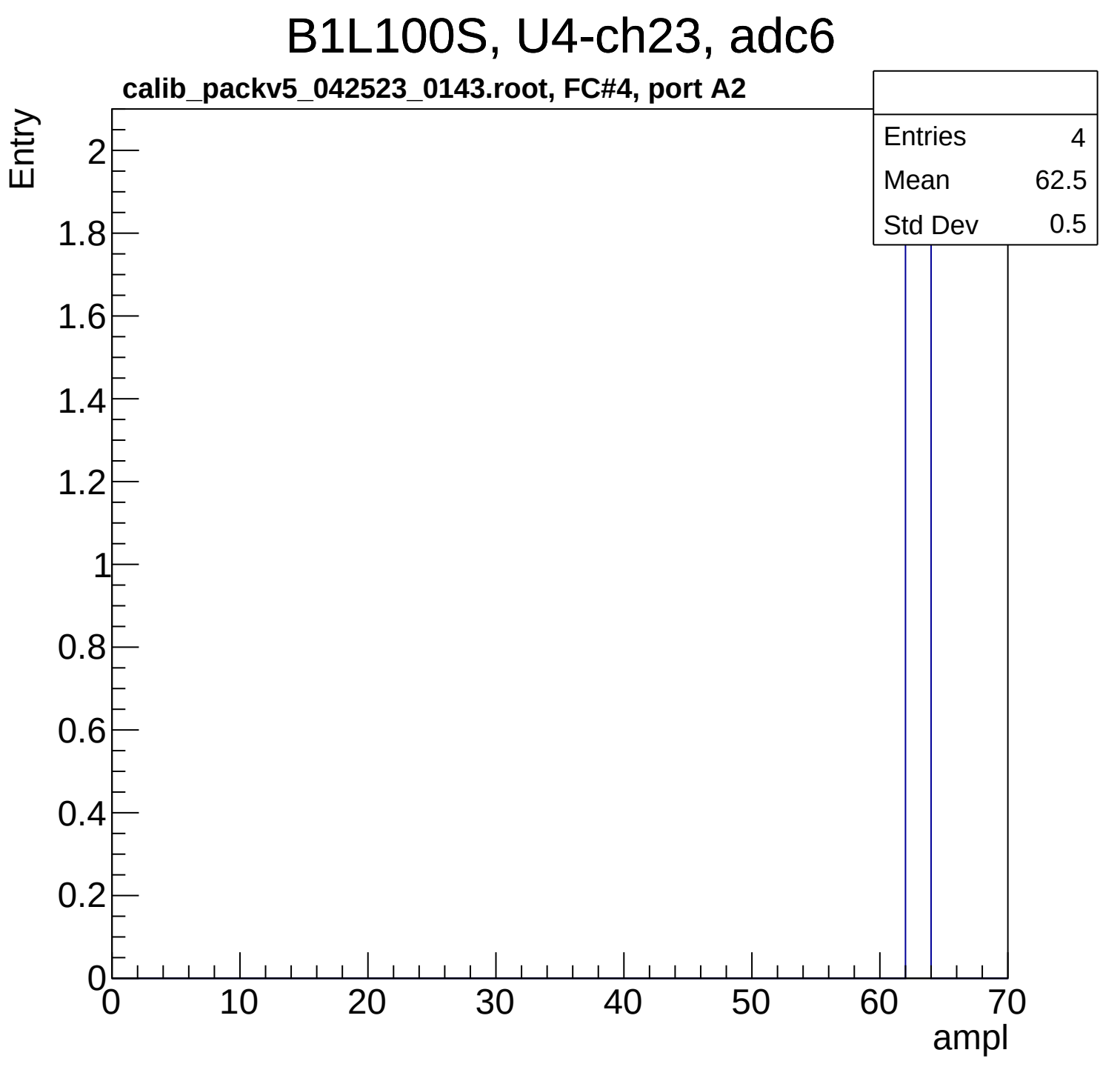

B1L100S, U4-ch23, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 37.02
Std Dev 3.494
Gaus mean : 37.6193
Gaus Width: 4.3514
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

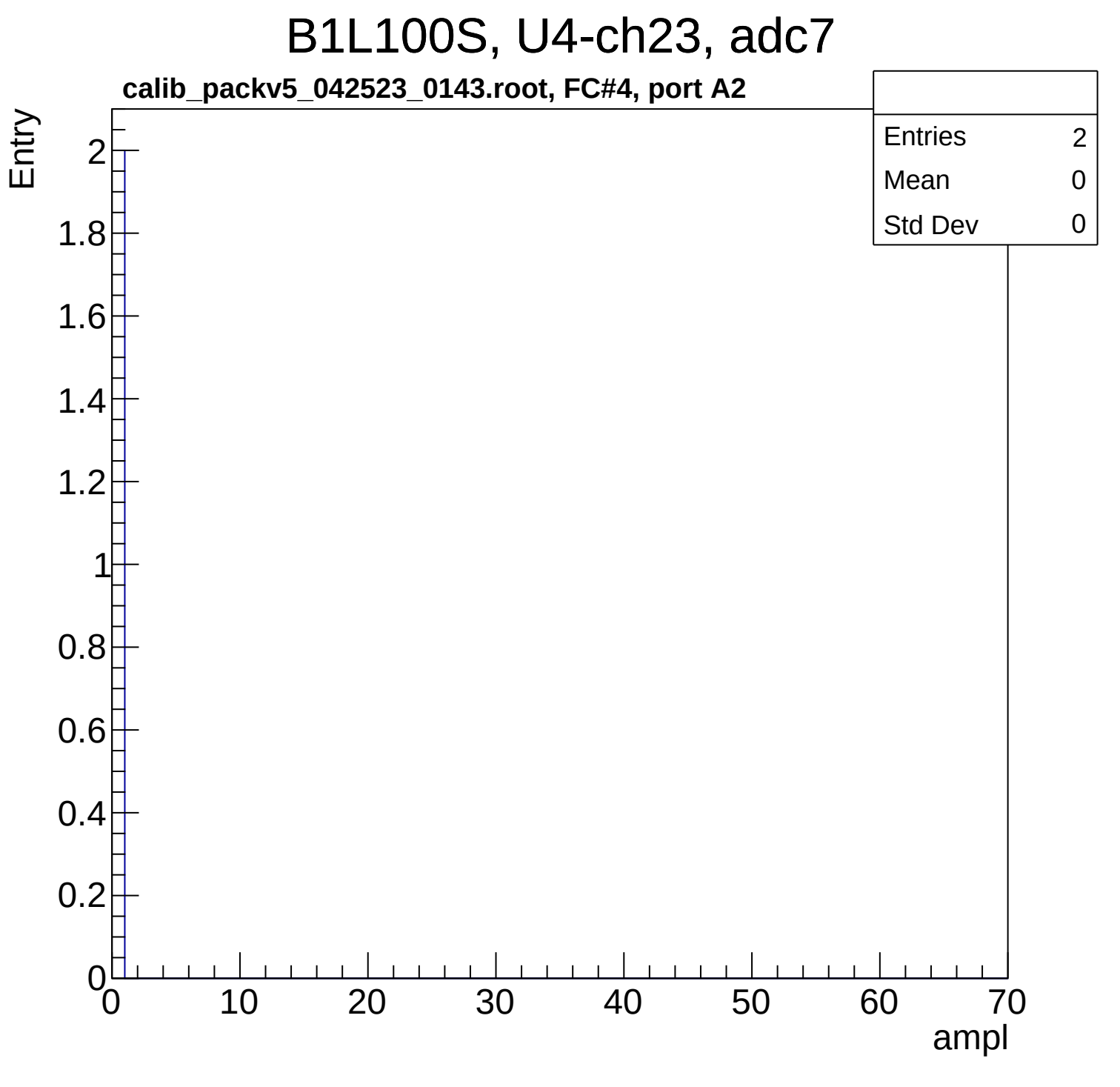

B1L100S, U4-ch23, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 42.88
Std Dev 3.37
Gaus mean : 43.5486
Gaus Width: 3.2145
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

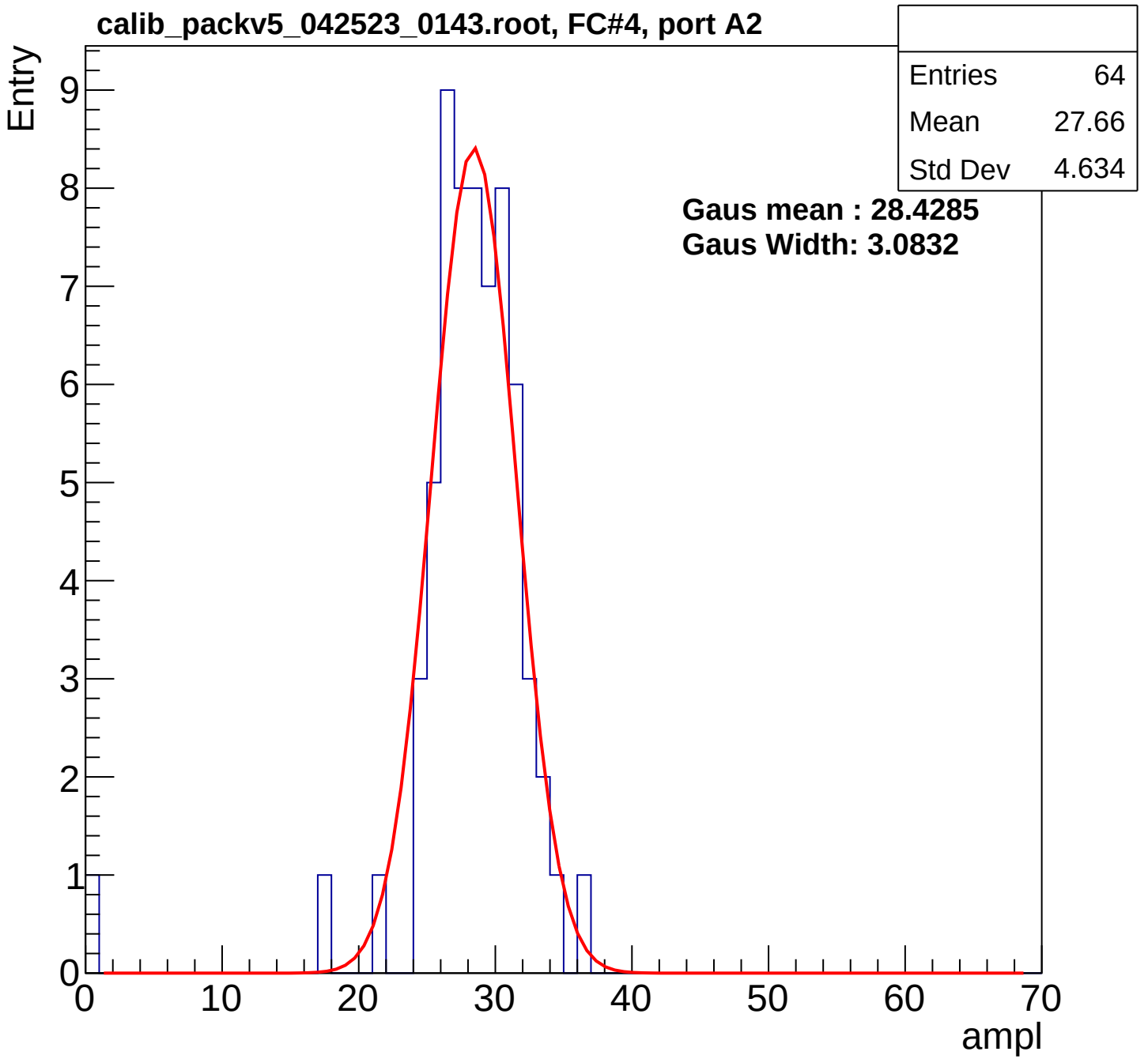

B1L100S, U4-ch23, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 49.35
Std Dev 3.456
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

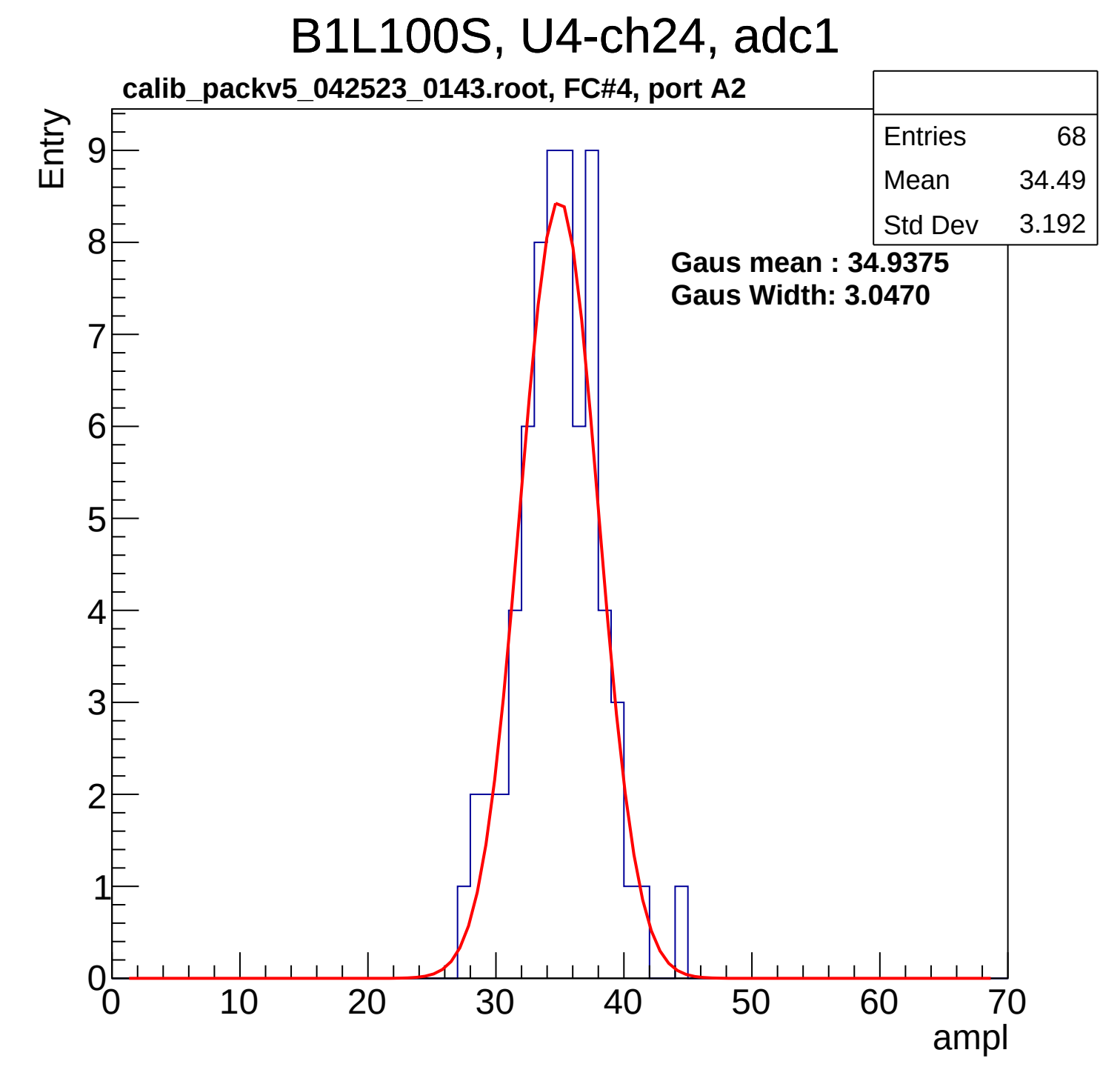

B1L100S, U4-ch23, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 55.07
Std Dev 3.211
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

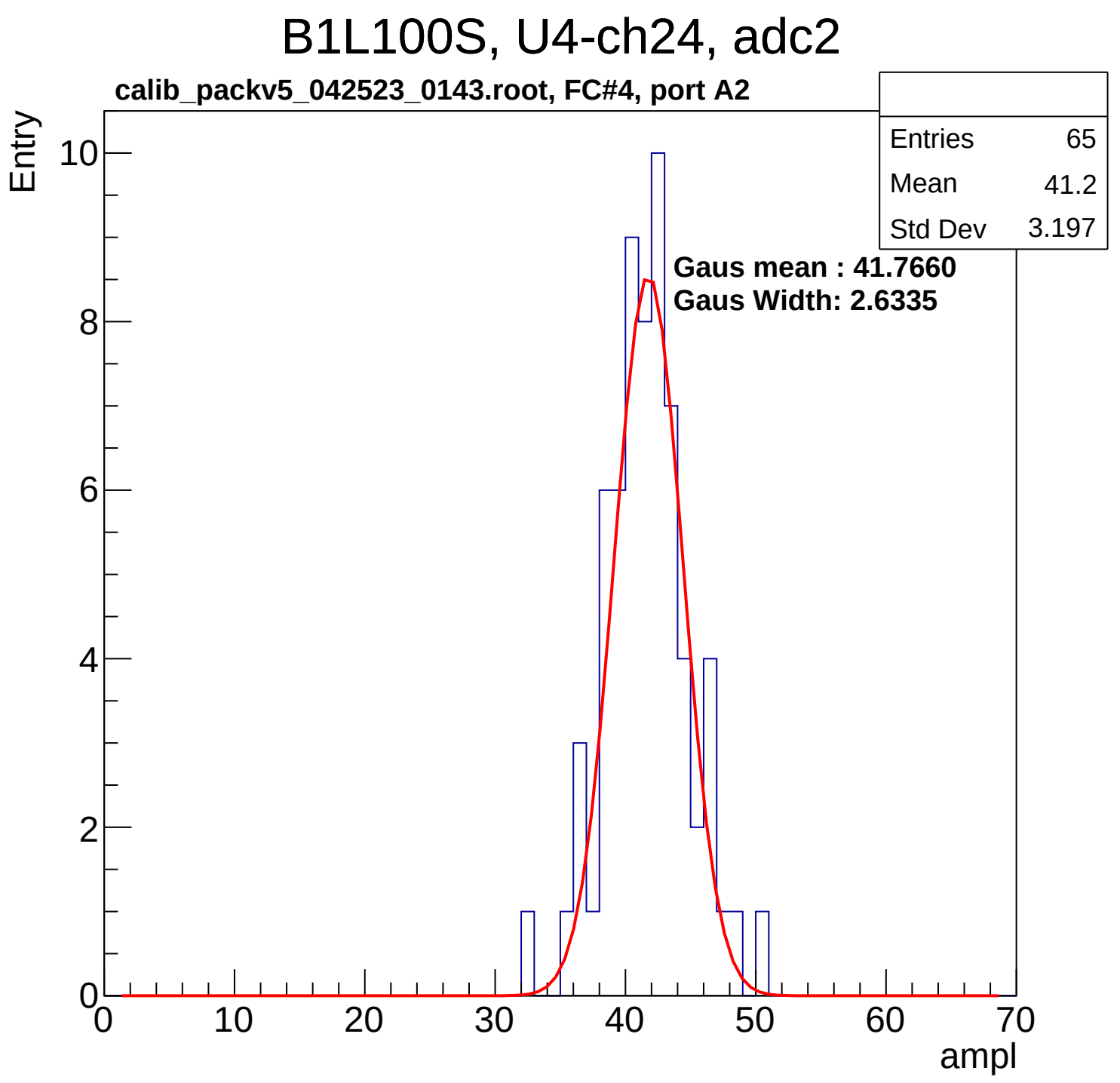

B1L100S, U4-ch23, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 58.83
Std Dev 9.073
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

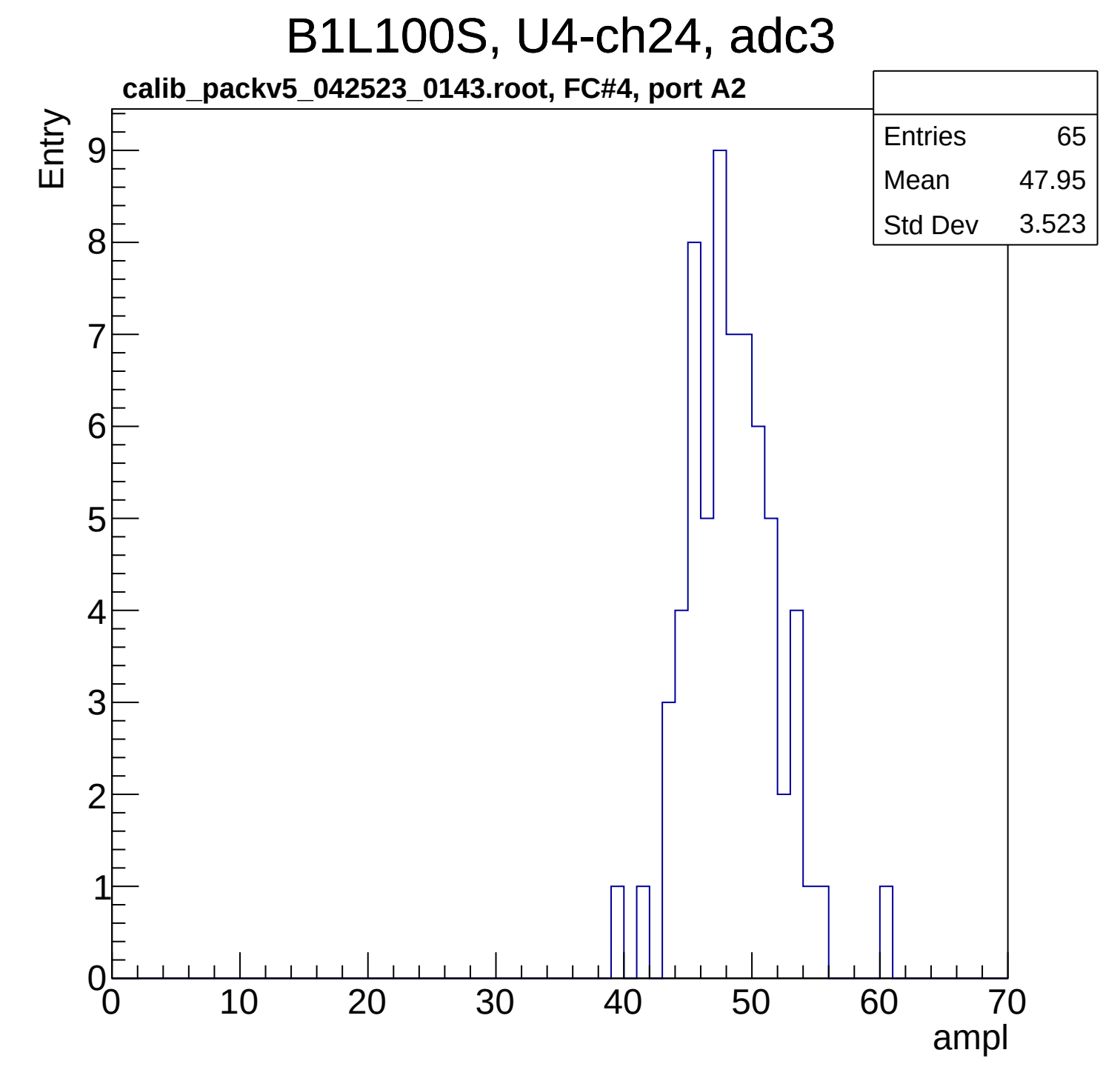

B1L100S, U4-ch23, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 62.5
Std Dev 0.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

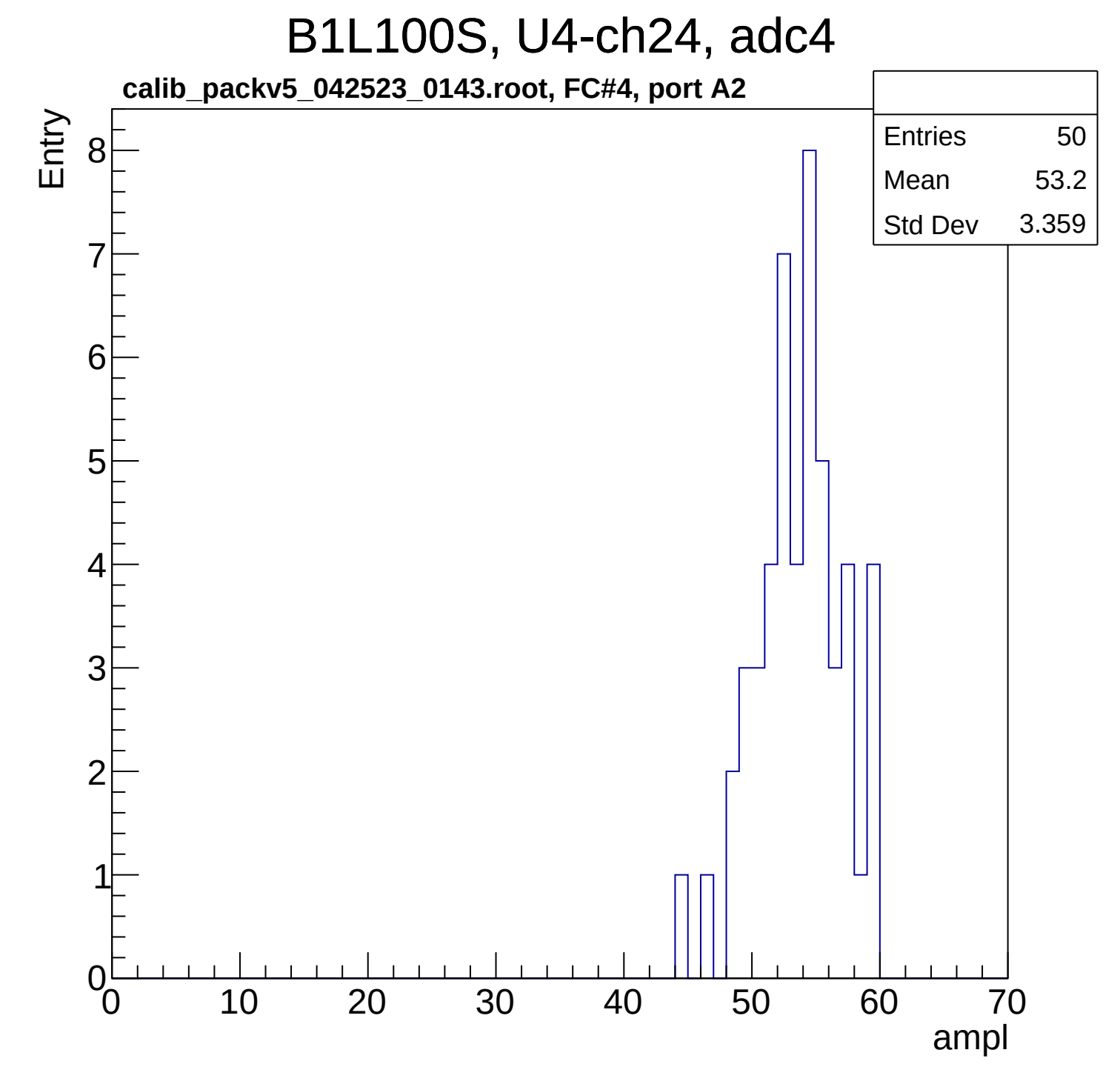

B1L100S, U4-ch23, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

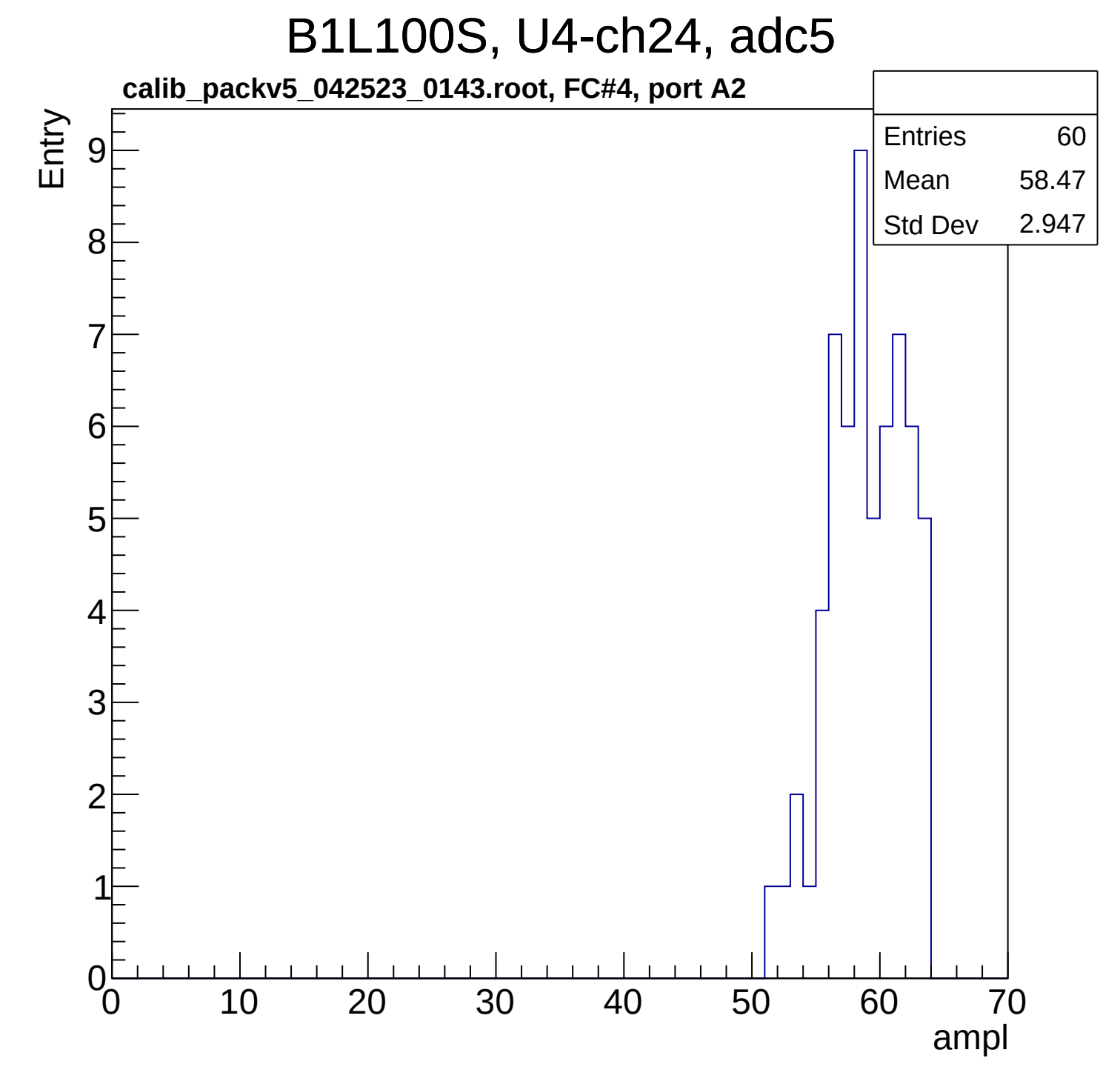

B1L100S, U4-ch24, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 27.66
Std Dev 4.634
Gaus mean : 28.4285
Gaus Width: 3.0832
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

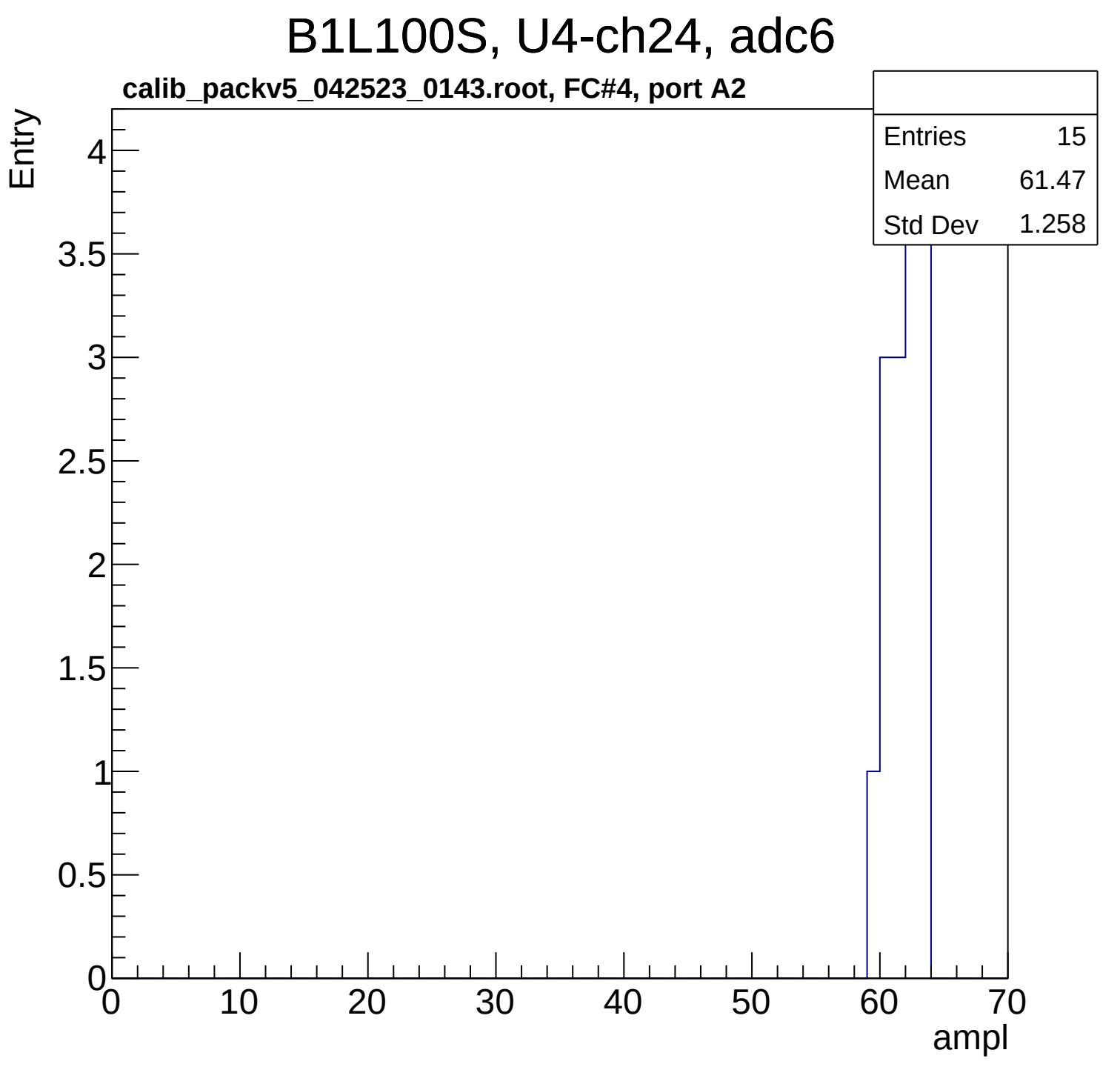

B1L100S, U4-ch24, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 34.49
Std Dev 3.192
Gaus mean : 34.9375
Gaus Width: 3.0470
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

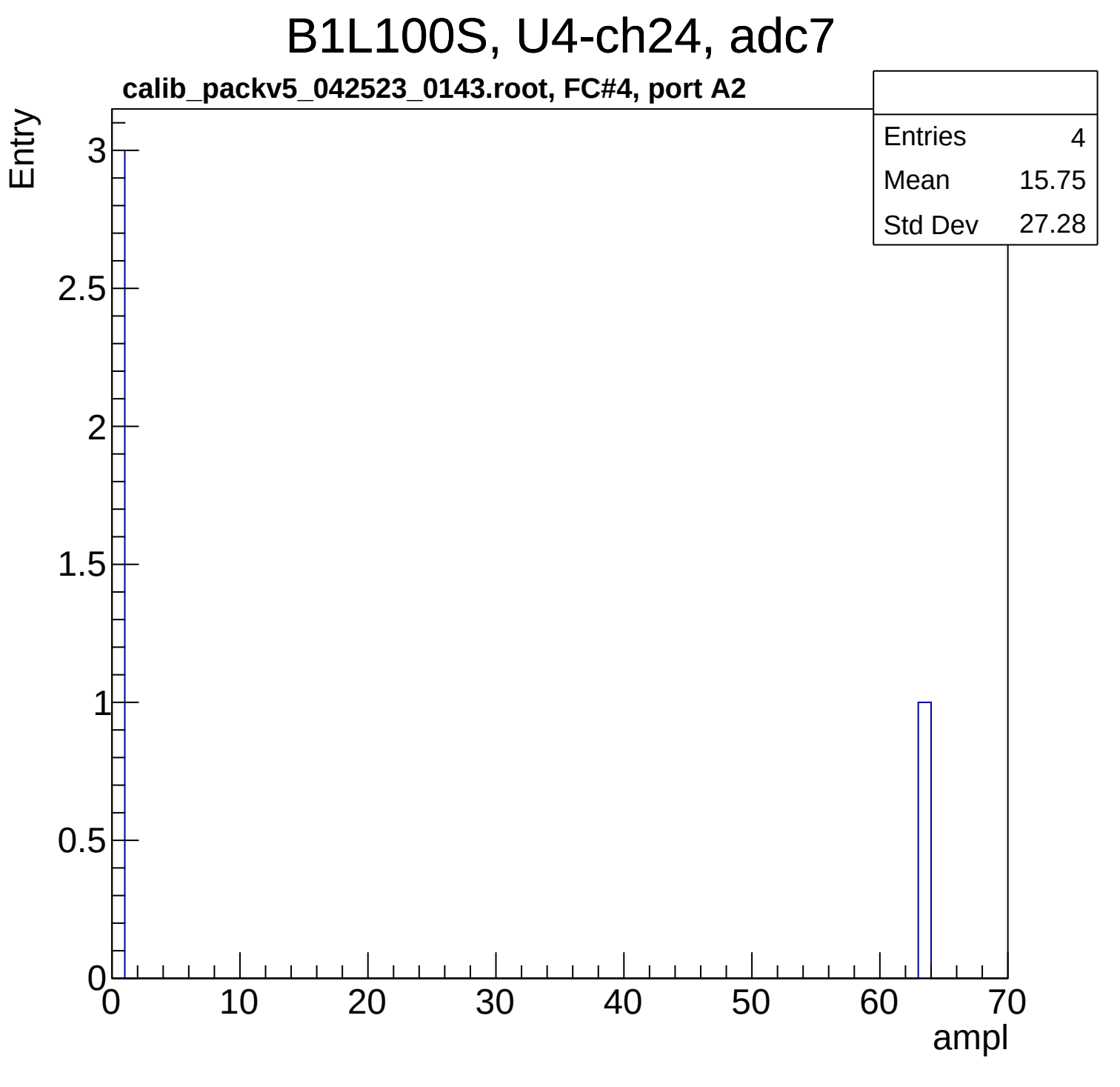

B1L100S, U4-ch24, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 41.2
Std Dev 3.197
Gaus mean : 41.7660
Gaus Width: 2.6335
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

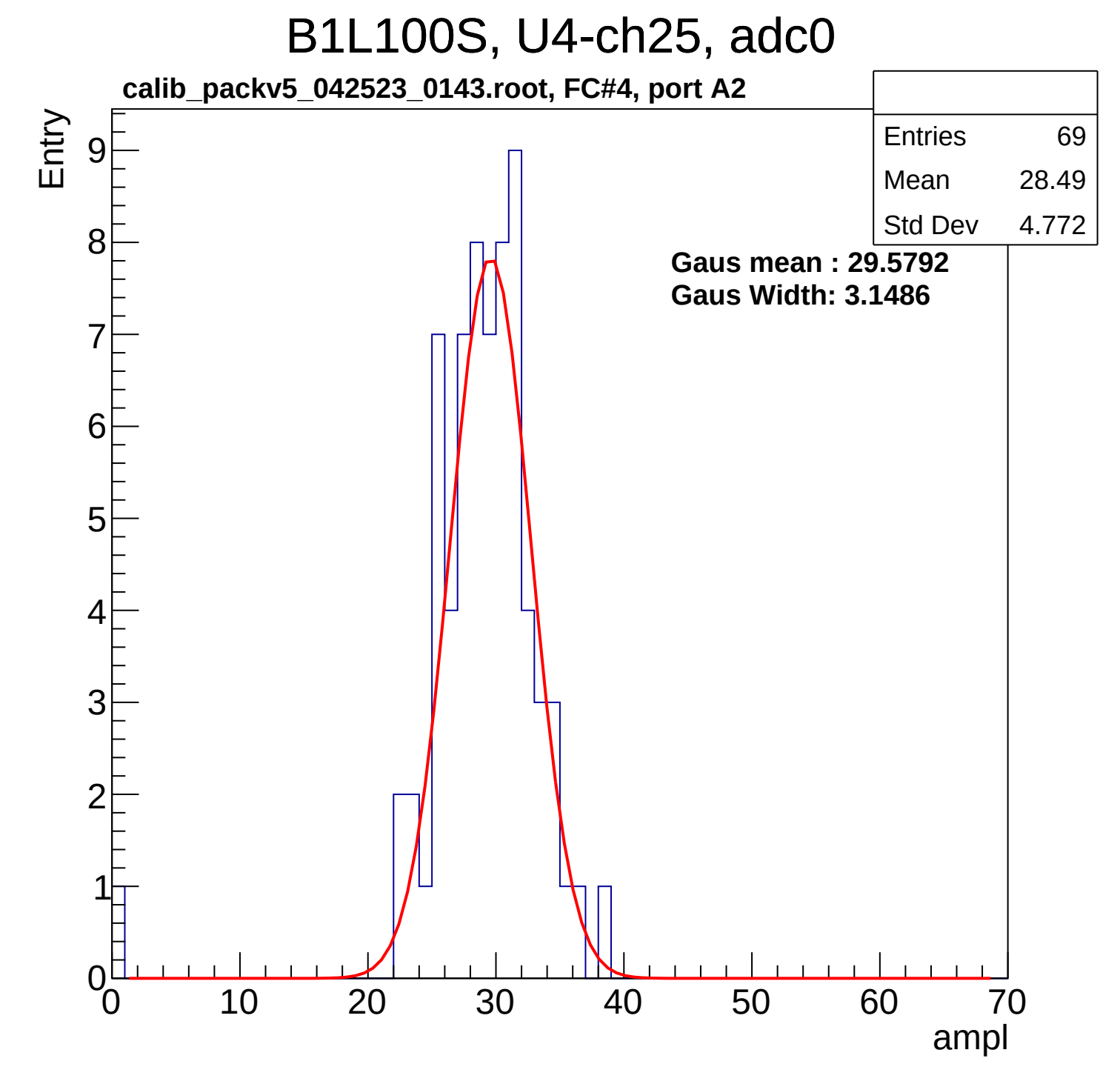

B1L100S, U4-ch24, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 47.95
Std Dev 3.523
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

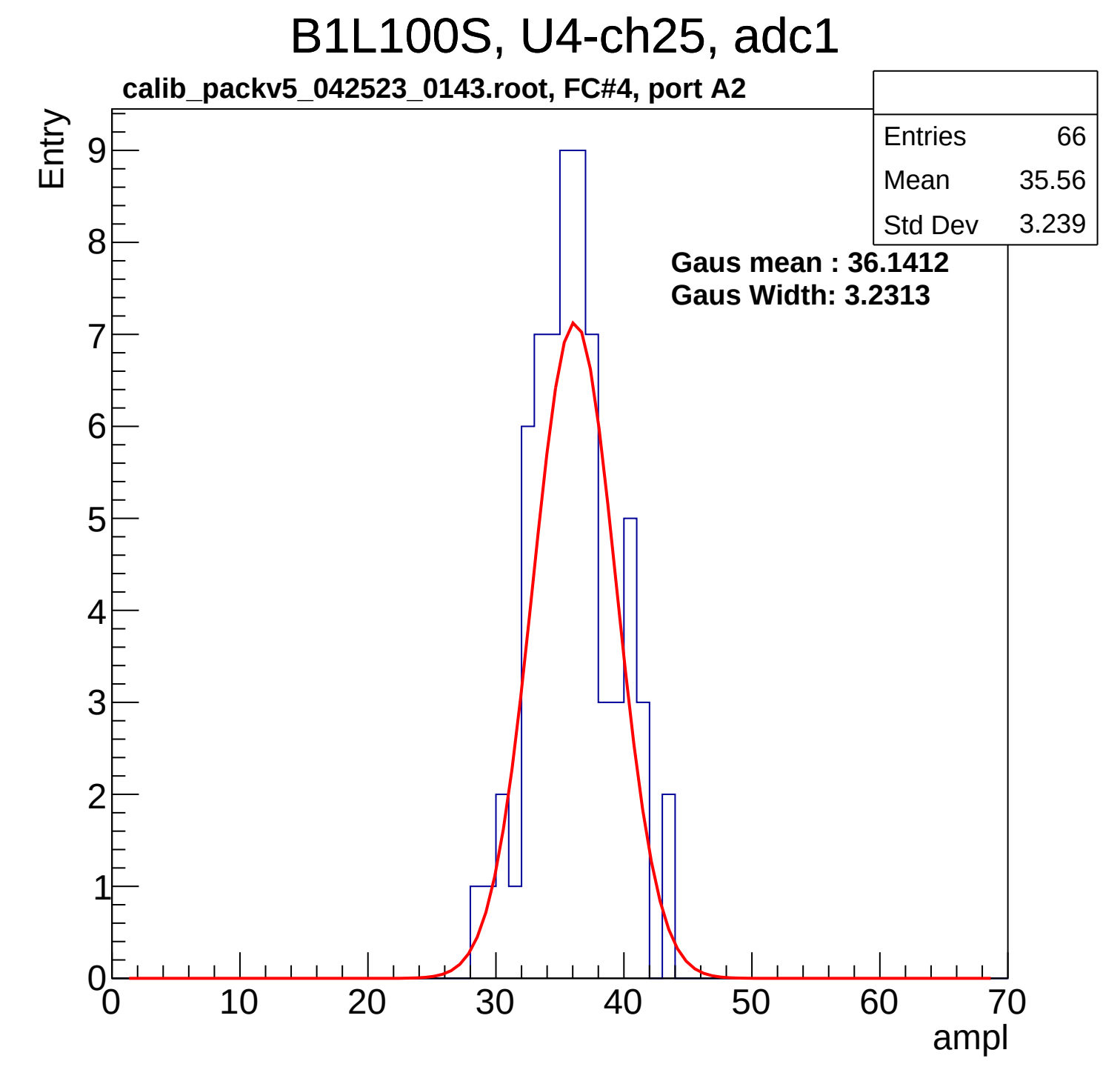

B1L100S, U4-ch24, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 53.2
Std Dev 3.359
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

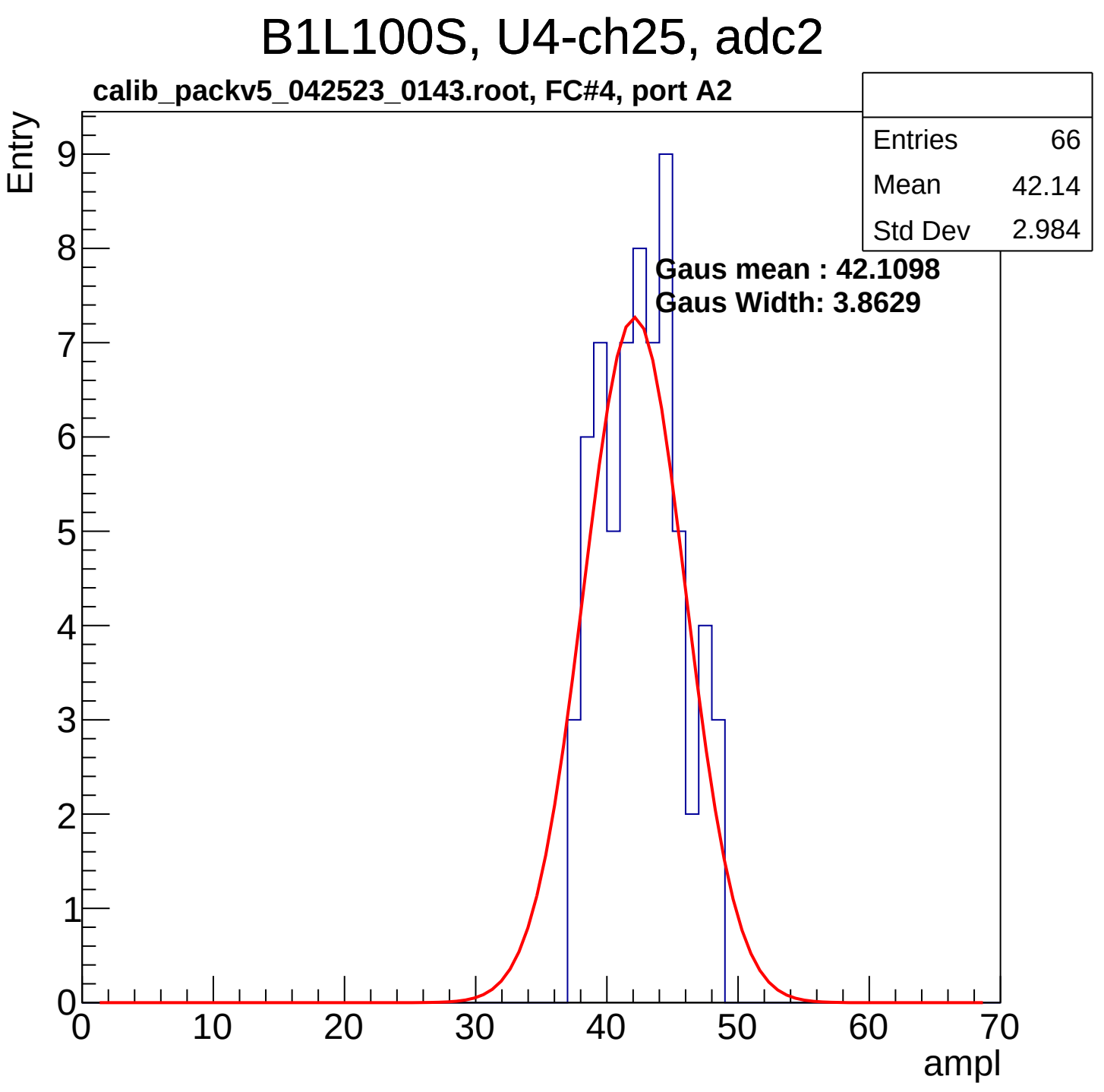

B1L100S, U4-ch24, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 58.47
Std Dev 2.947
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

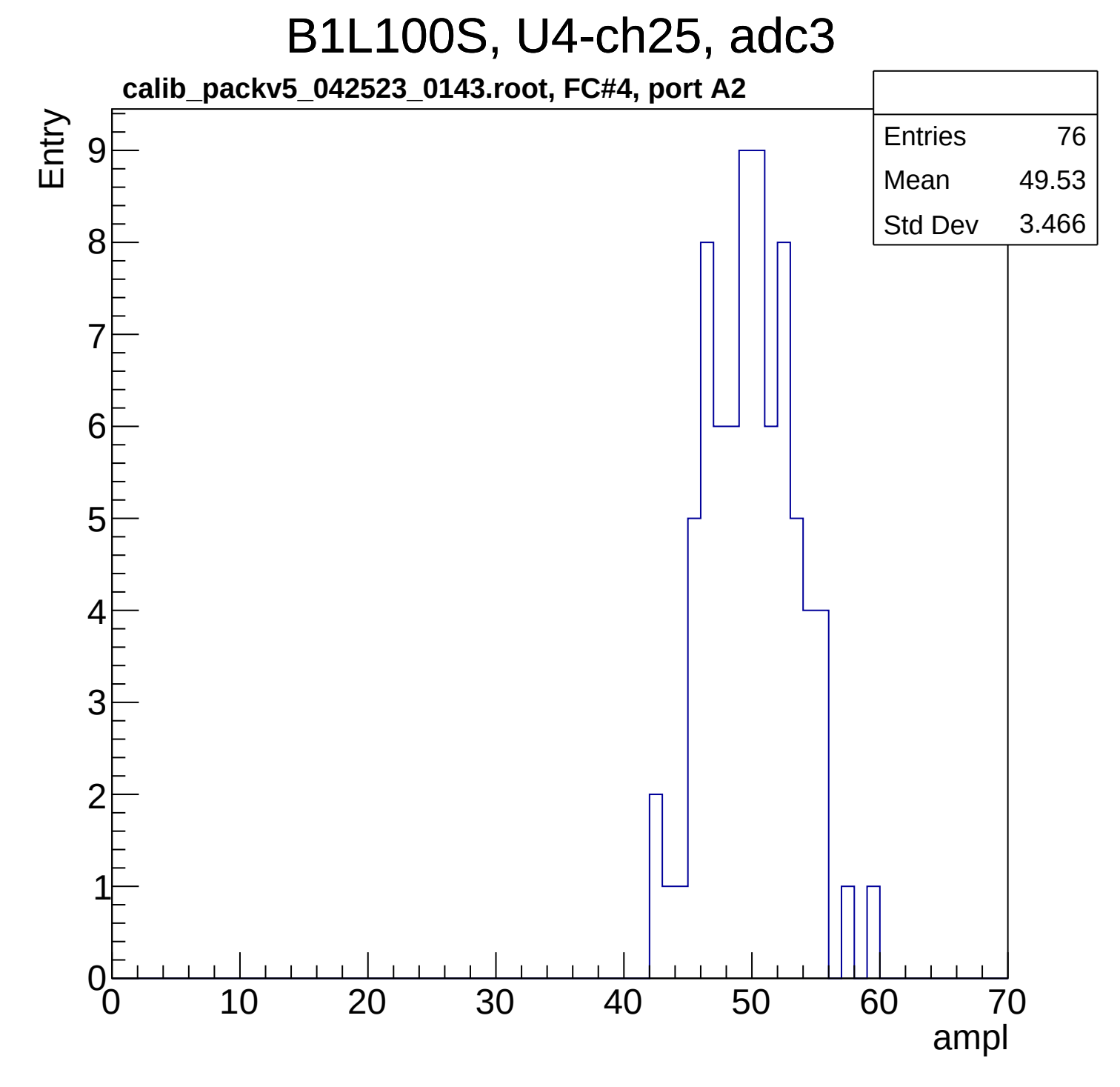

B1L100S, U4-ch24, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 15
Mean 61.47
Std Dev 1.258
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

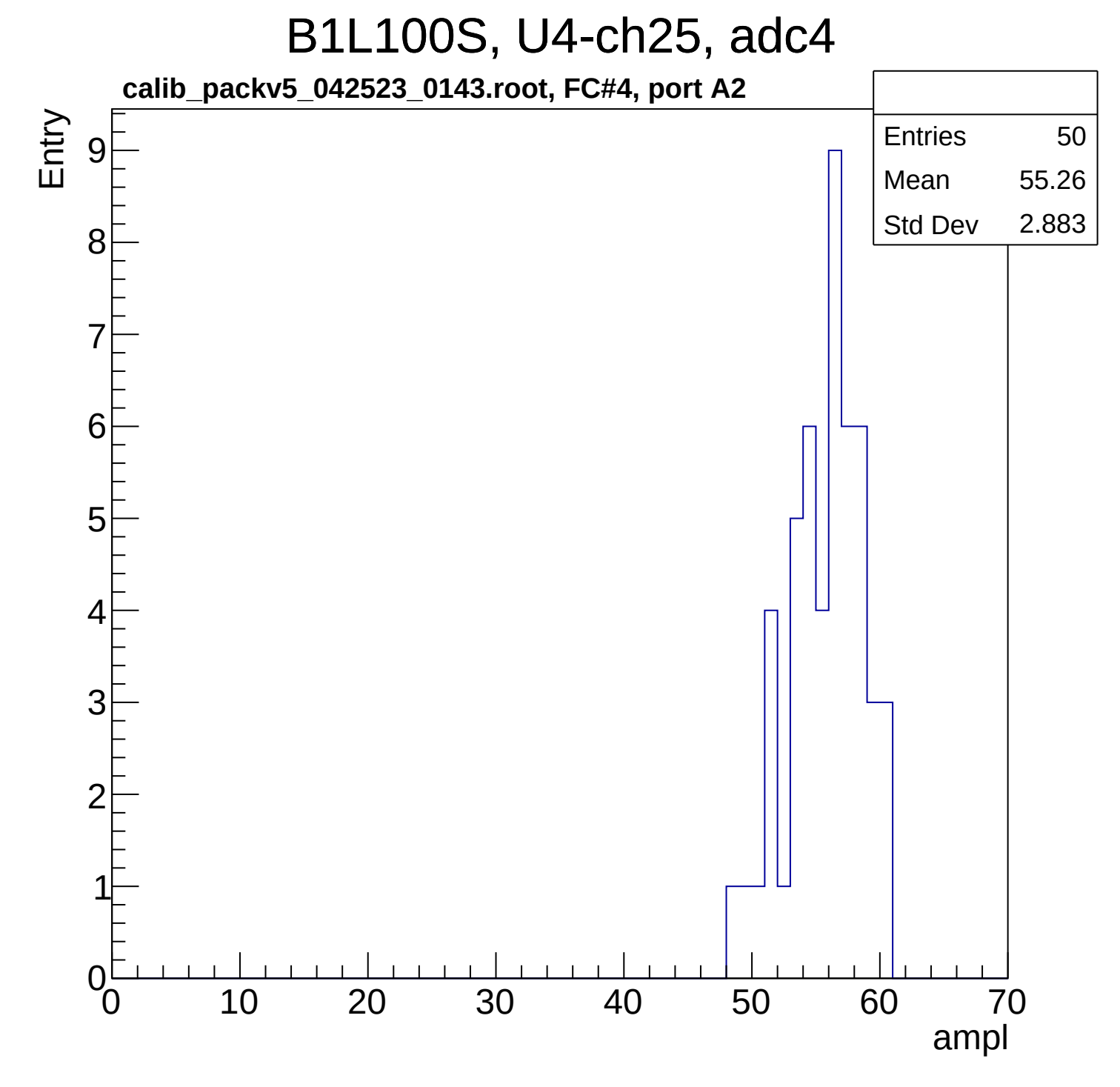

B1L100S, U4-ch24, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 15.75
Std Dev 27.28
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

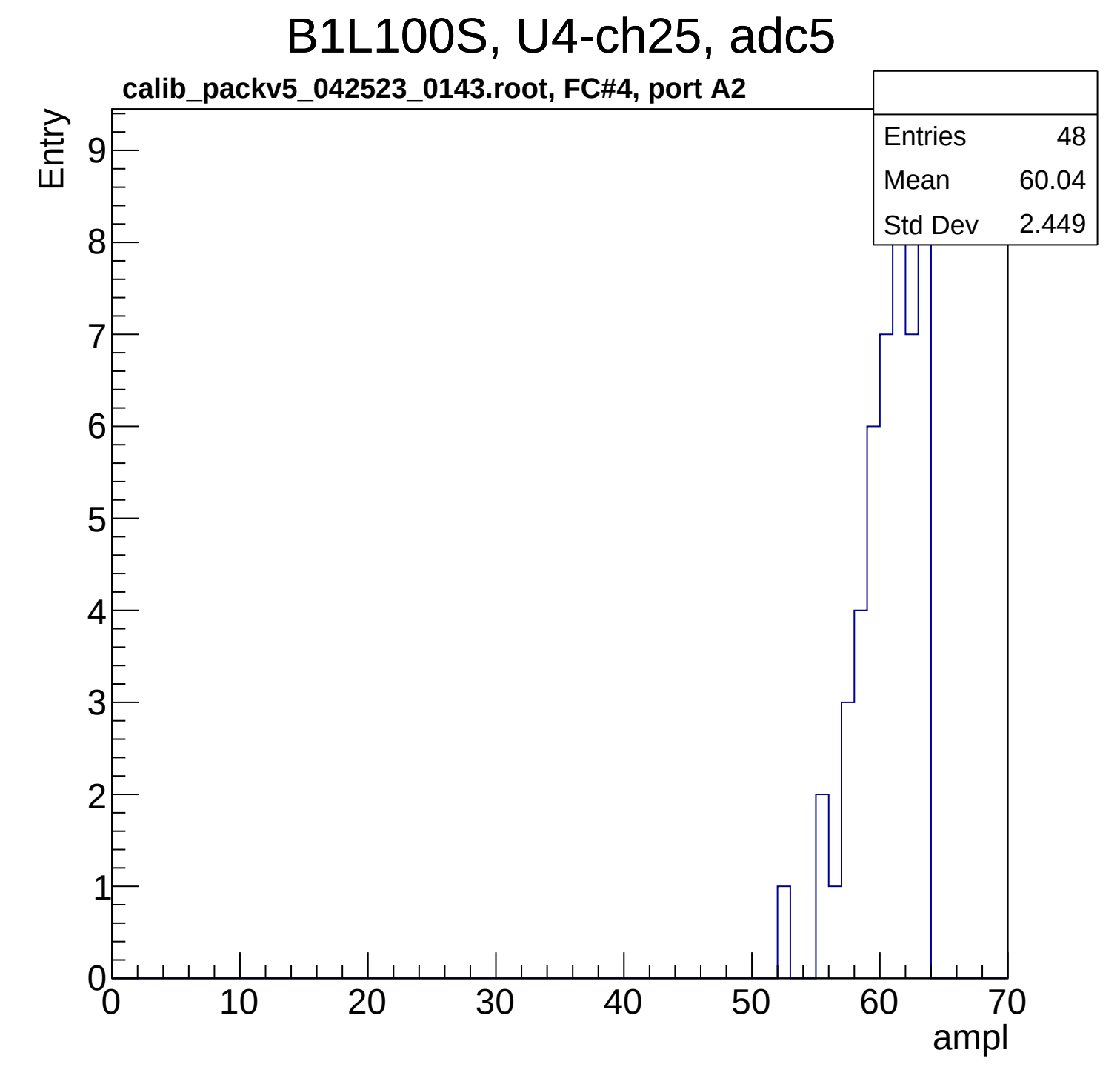

B1L100S, U4-ch25, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 28.49
Std Dev 4.772
Gaus mean : 29.5792
Gaus Width: 3.1486
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

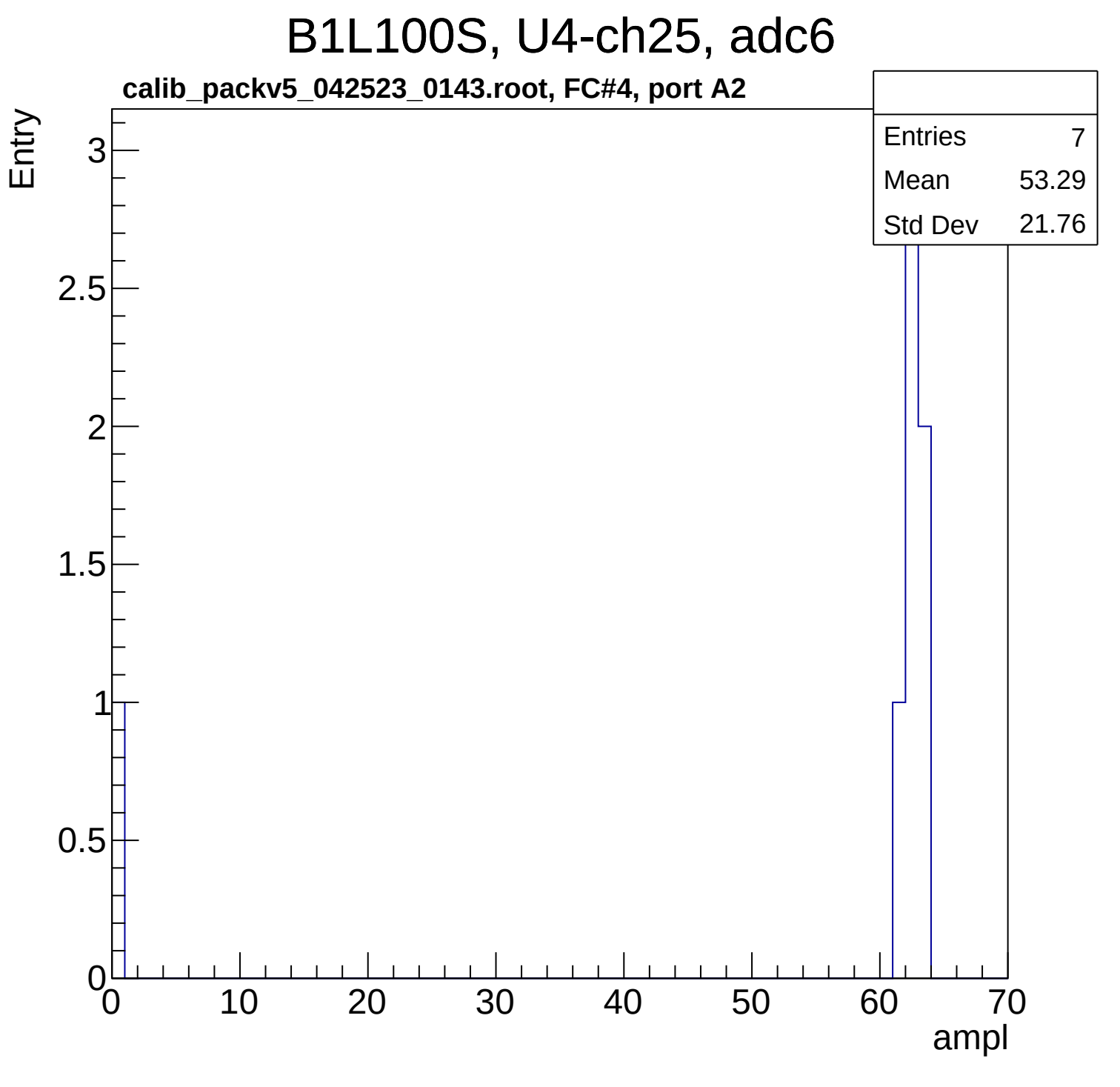

B1L100S, U4-ch25, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 35.56
Std Dev 3.239
Gaus mean : 36.1412
Gaus Width: 3.2313
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

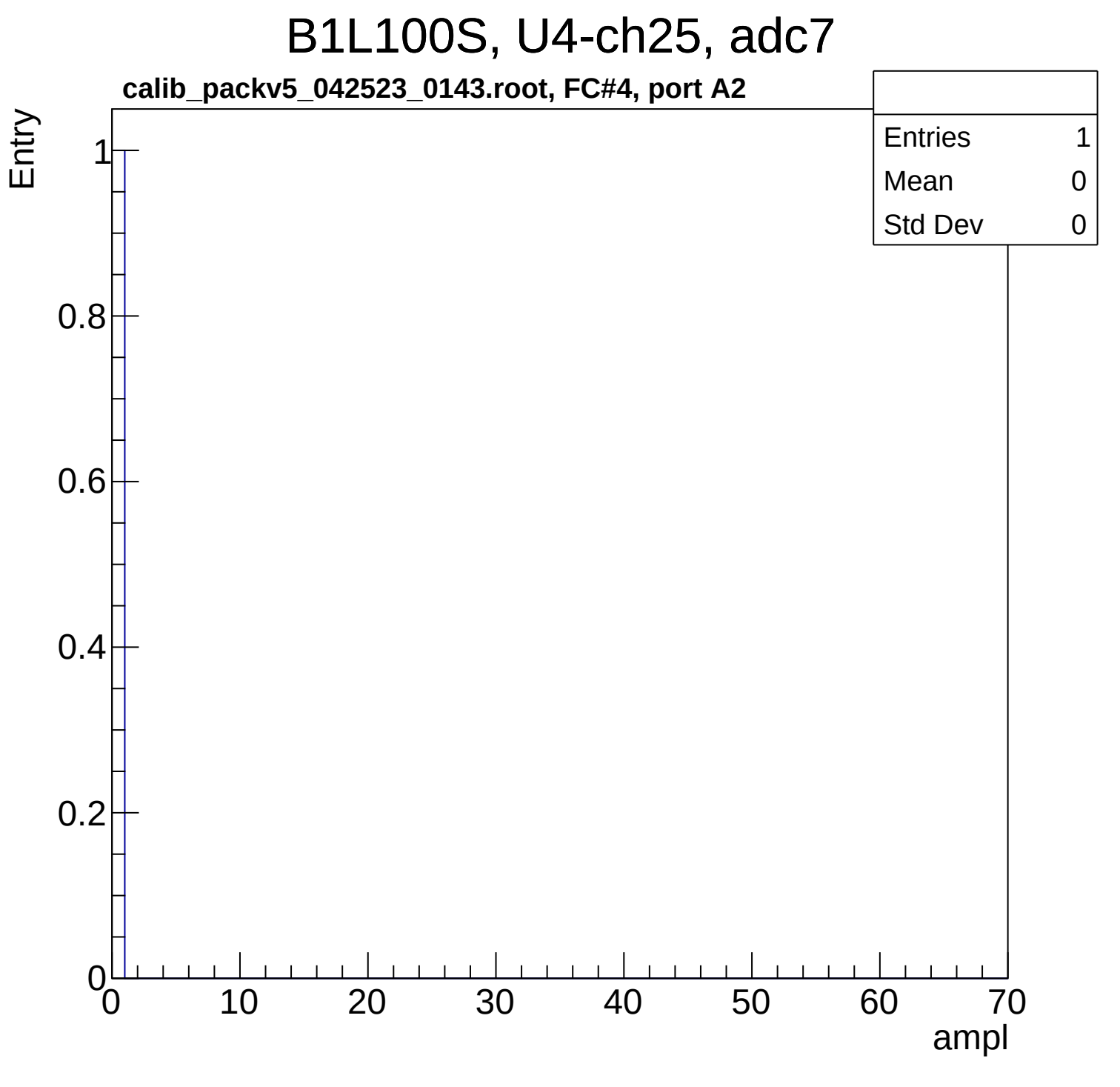

B1L100S, U4-ch25, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 42.14
Std Dev 2.984
Gaus mean : 42.1098
Gaus Width: 3.8629
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

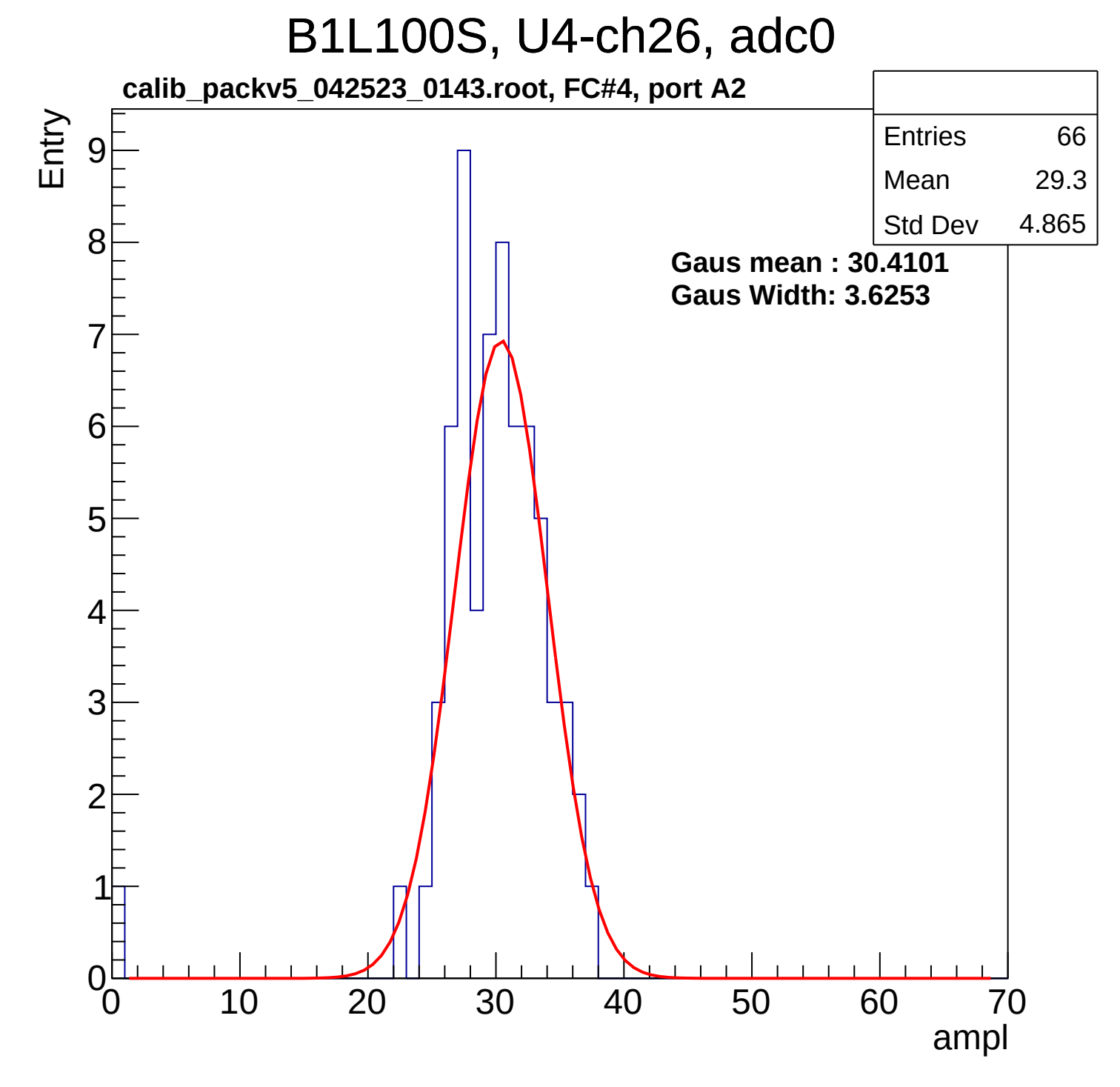

B1L100S, U4-ch25, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 49.53
Std Dev 3.466
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

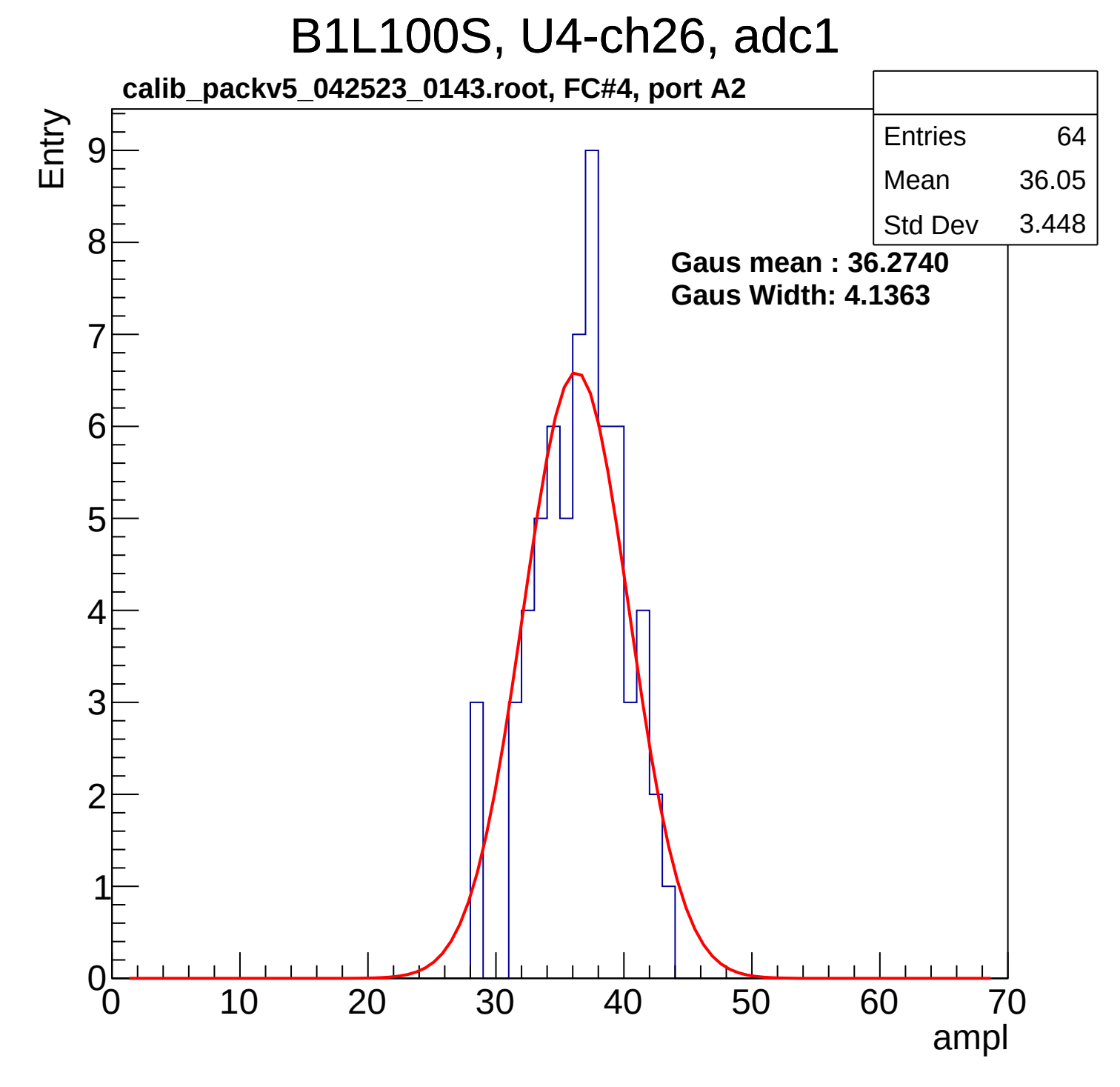

B1L100S, U4-ch25, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 55.26
Std Dev 2.883
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

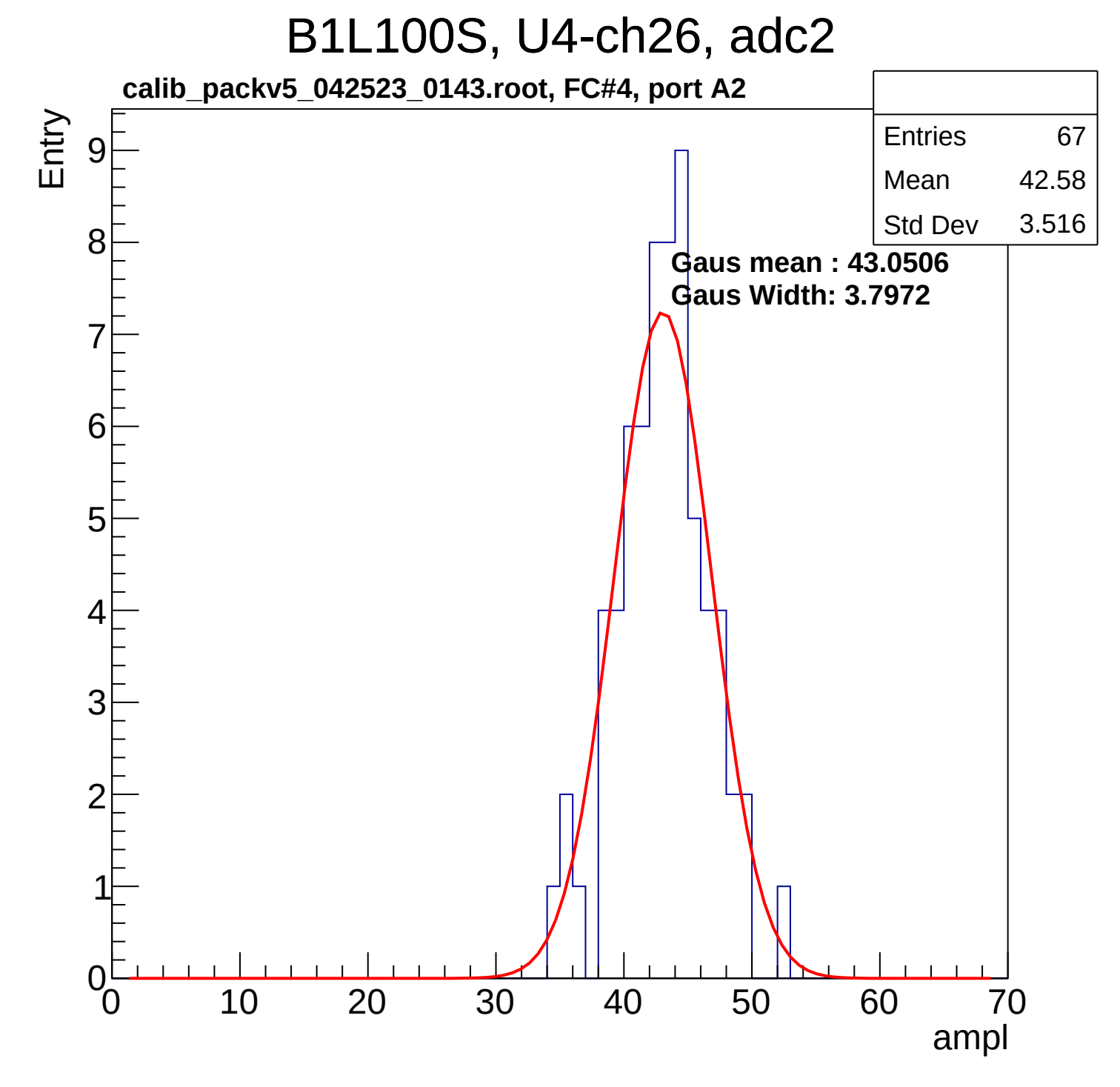

B1L100S, U4-ch25, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 60.04
Std Dev 2.449
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

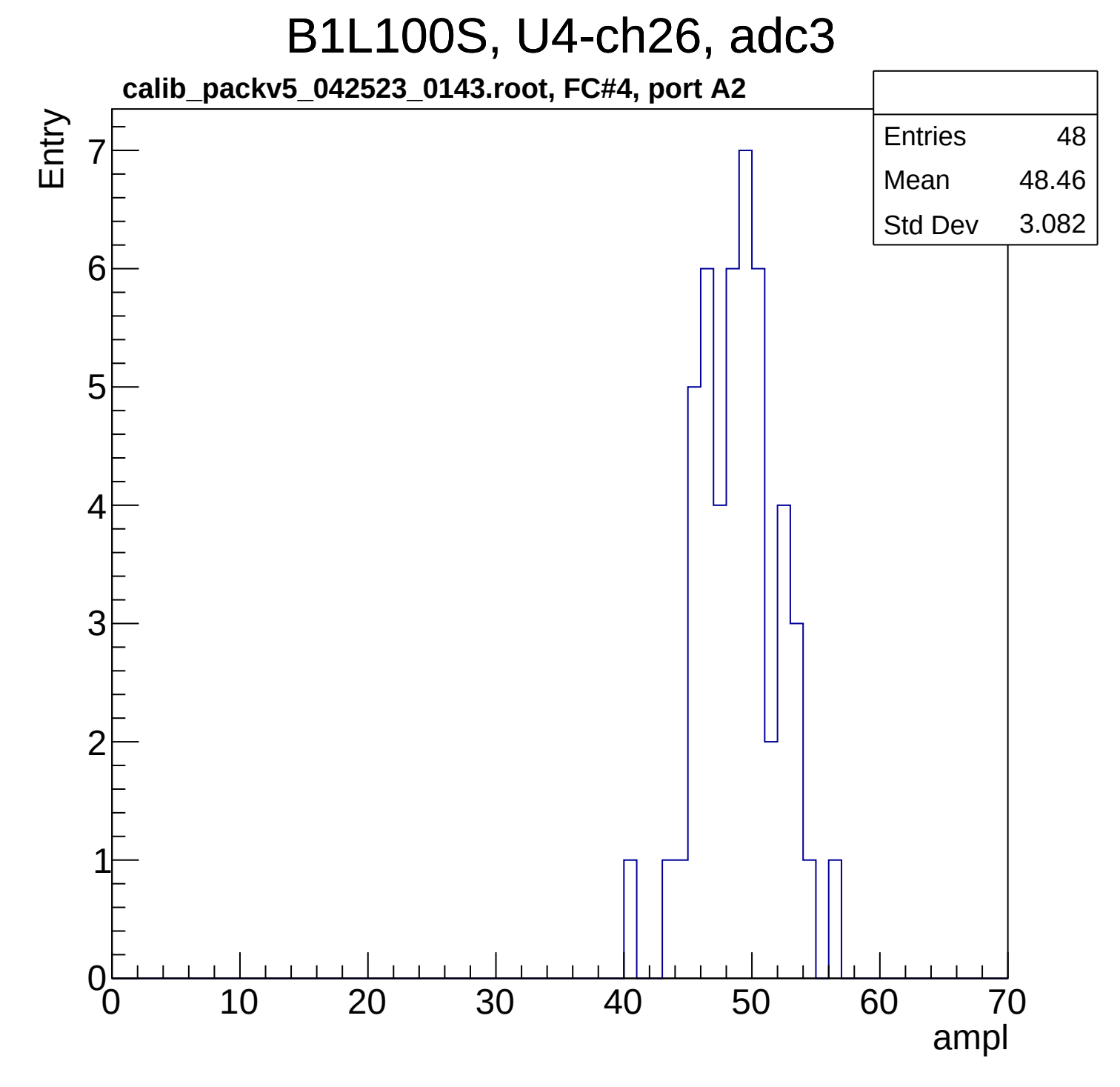

B1L100S, U4-ch25, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 53.29
Std Dev 21.76
Entry
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70
ampl

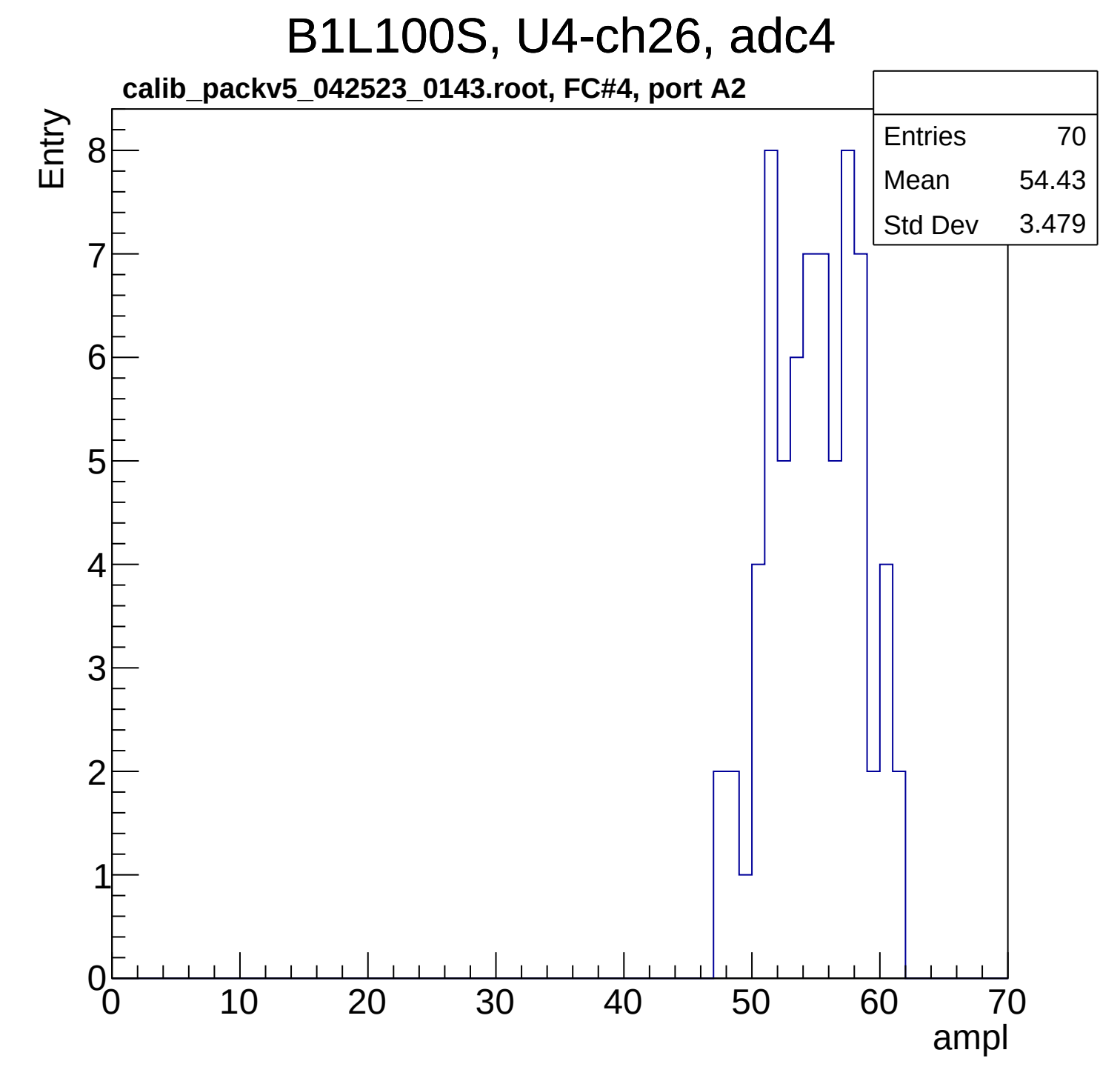

B1L100S, U4-ch25, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

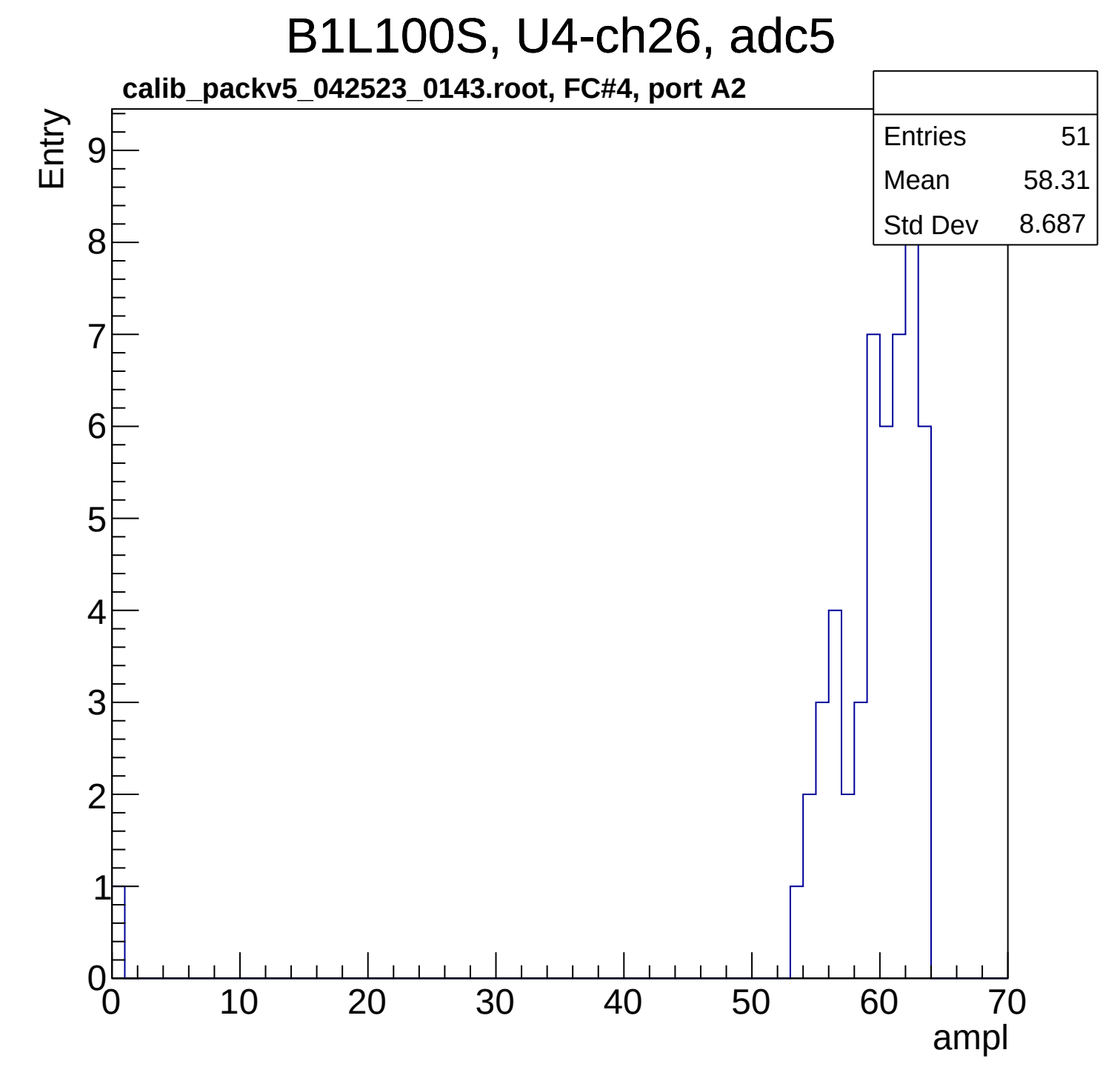

B1L100S, U4-ch26, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 29.3
Std Dev 4.865
Gaus mean : 30.4101
Gaus Width: 3.6253
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

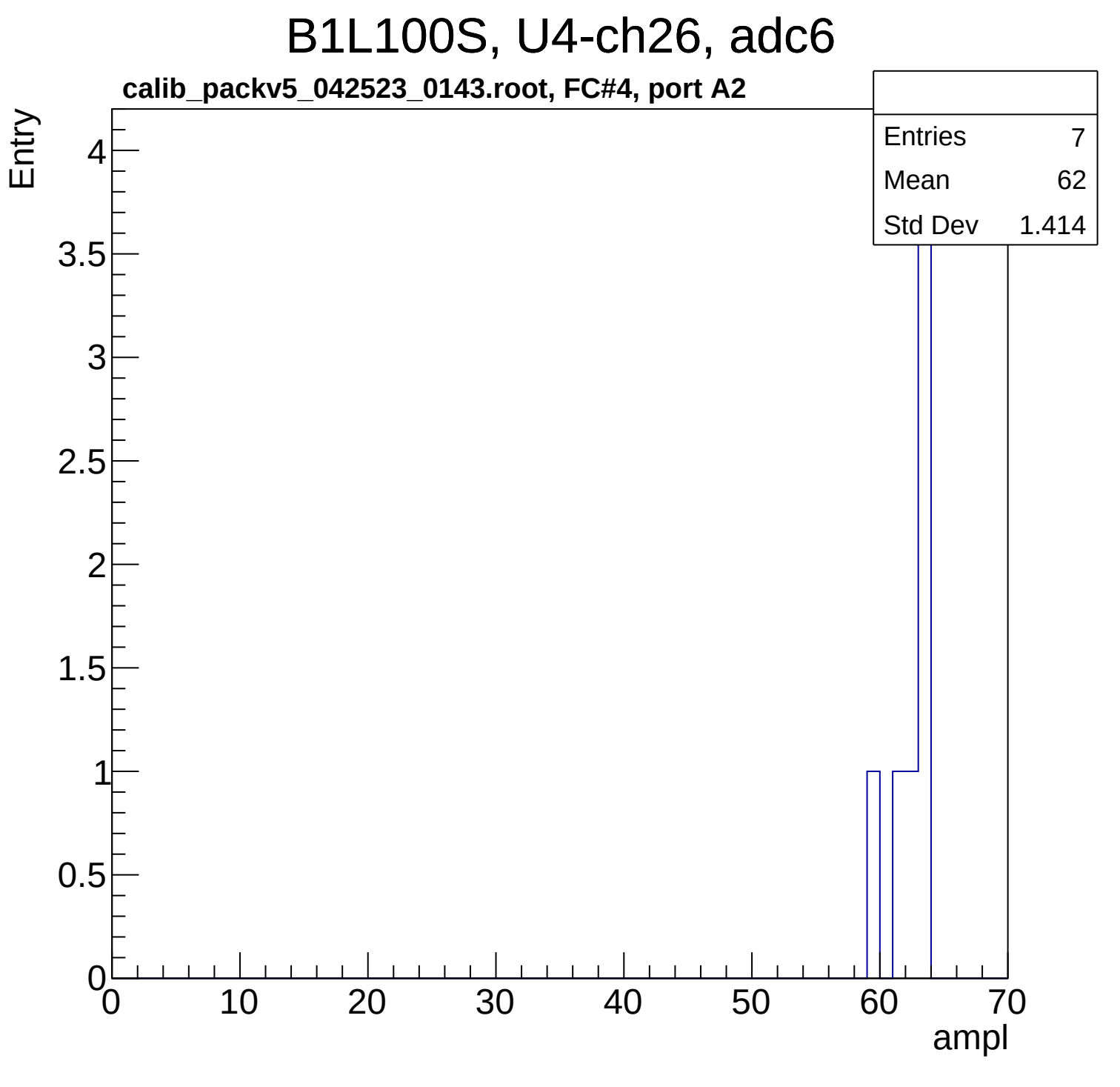

B1L100S, U4-ch26, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 36.05
Std Dev 3.448
Gaus mean : 36.2740
Gaus Width: 4.1363
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

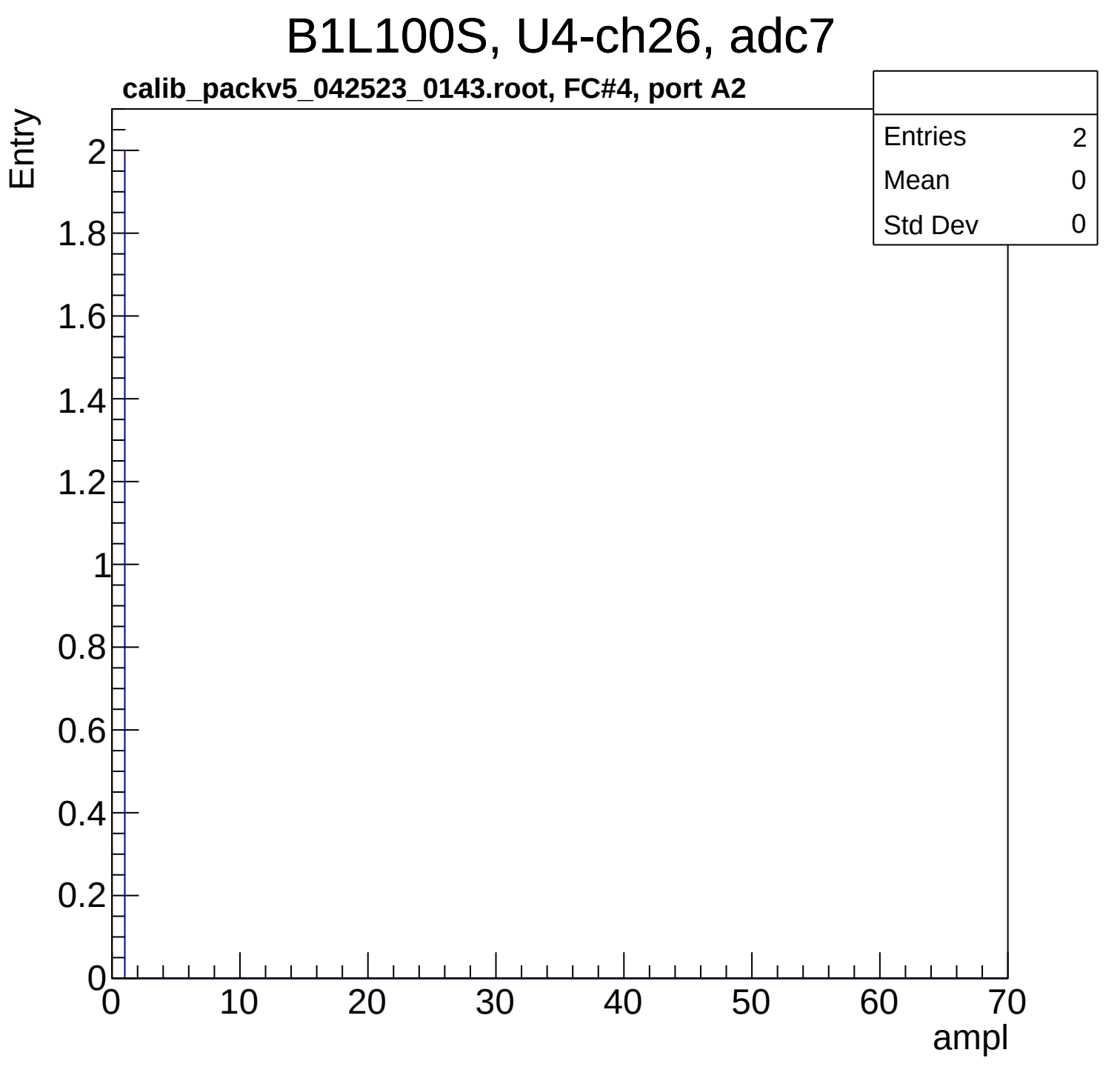

B1L100S, U4-ch26, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 42.58
Std Dev 3.516
Gaus mean : 43.0506
Gaus Width: 3.7972
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

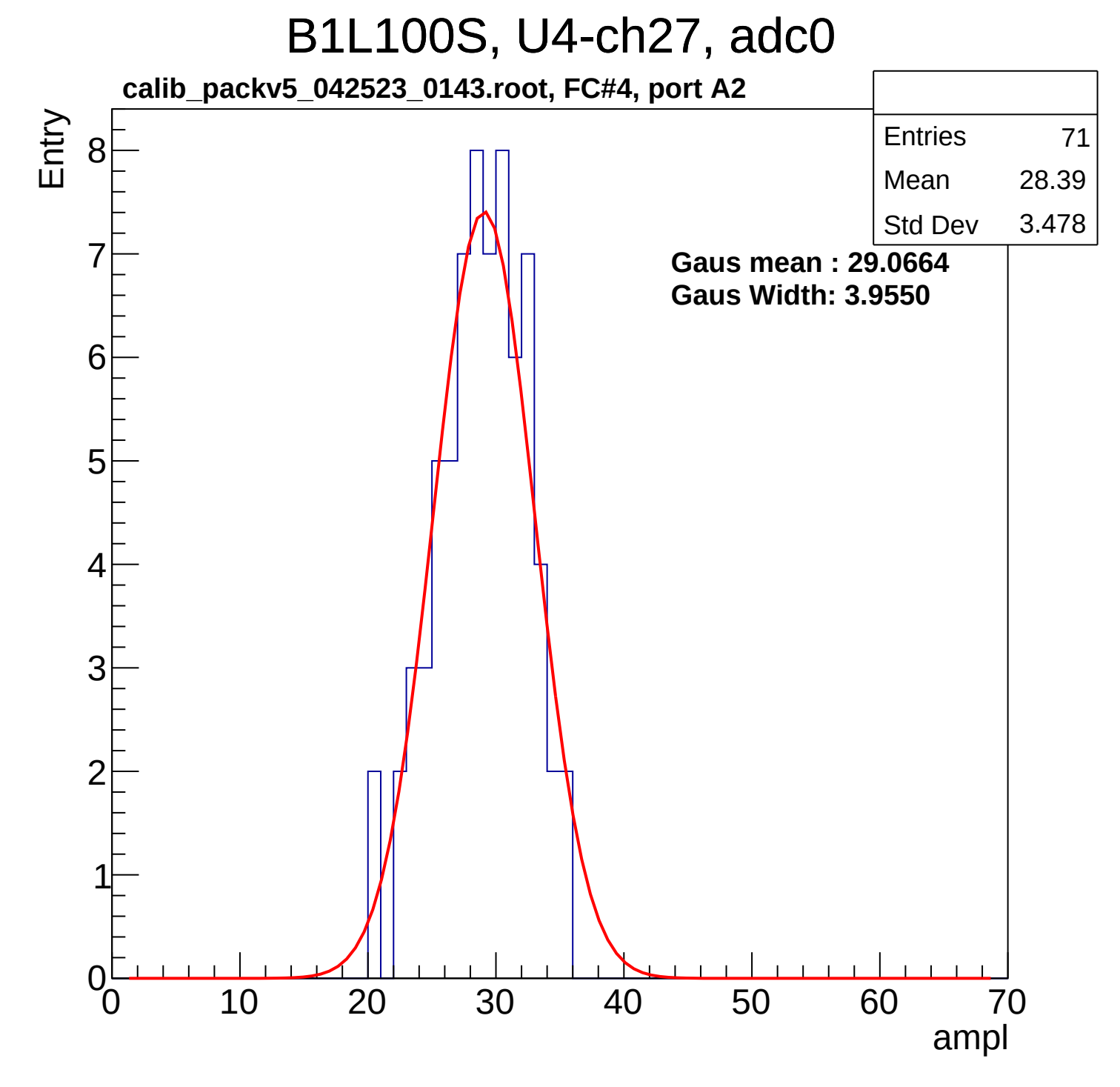

B1L100S, U4-ch26, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 48.46
Std Dev 3.082
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

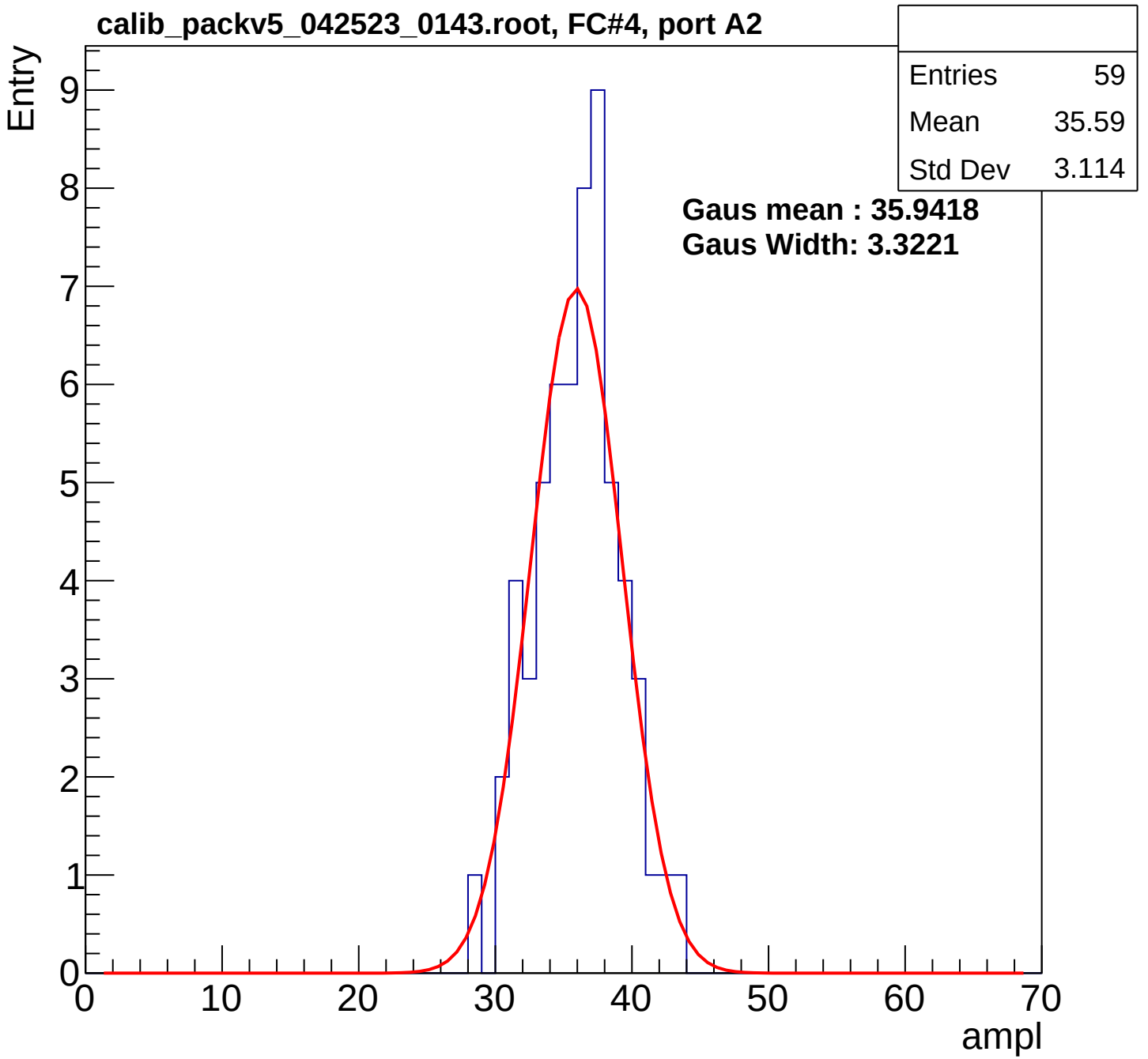

B1L100S, U4-ch26, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 54.43
Std Dev 3.479
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

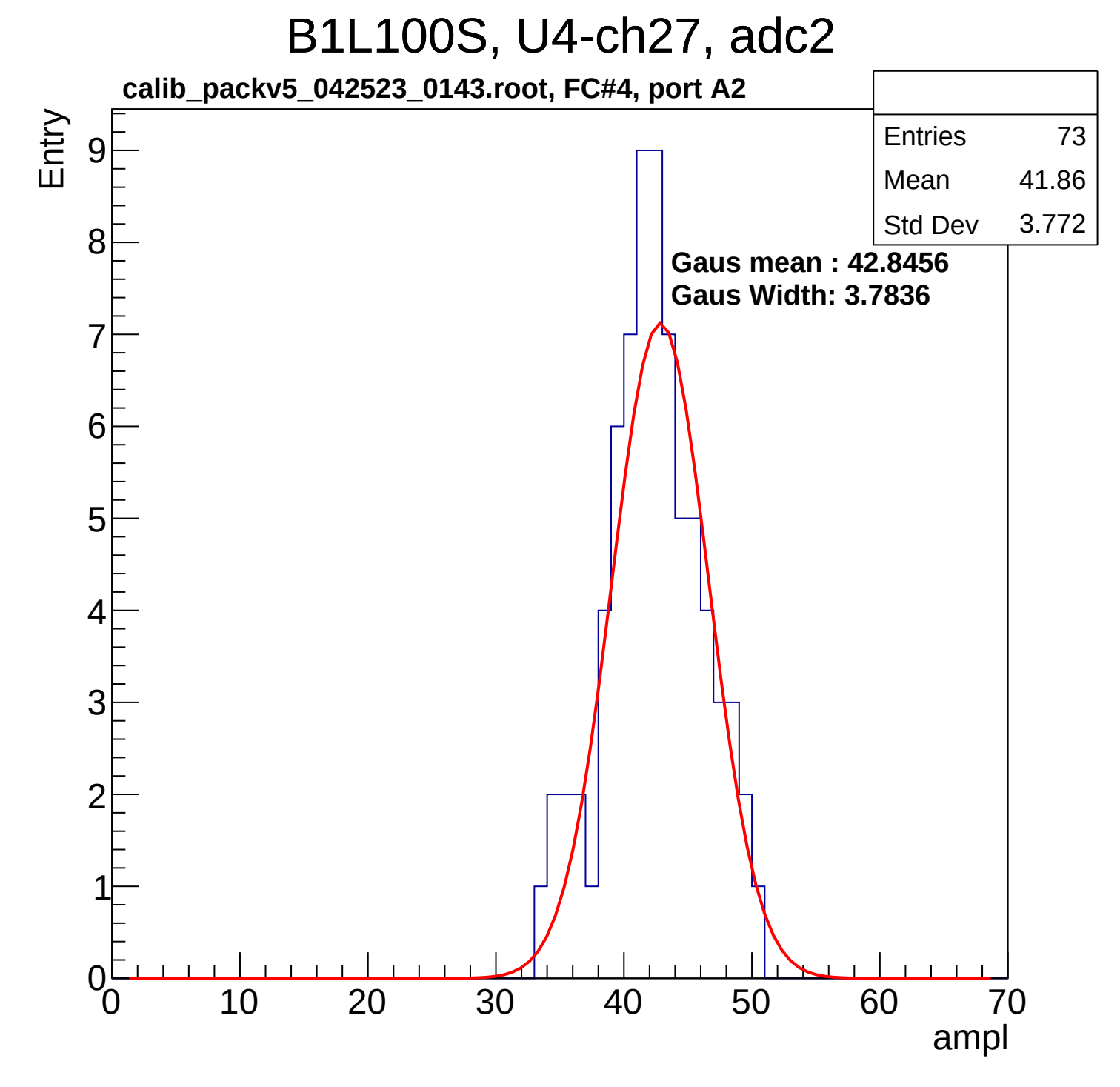

B1L100S, U4-ch26, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 58.31
Std Dev 8.687
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

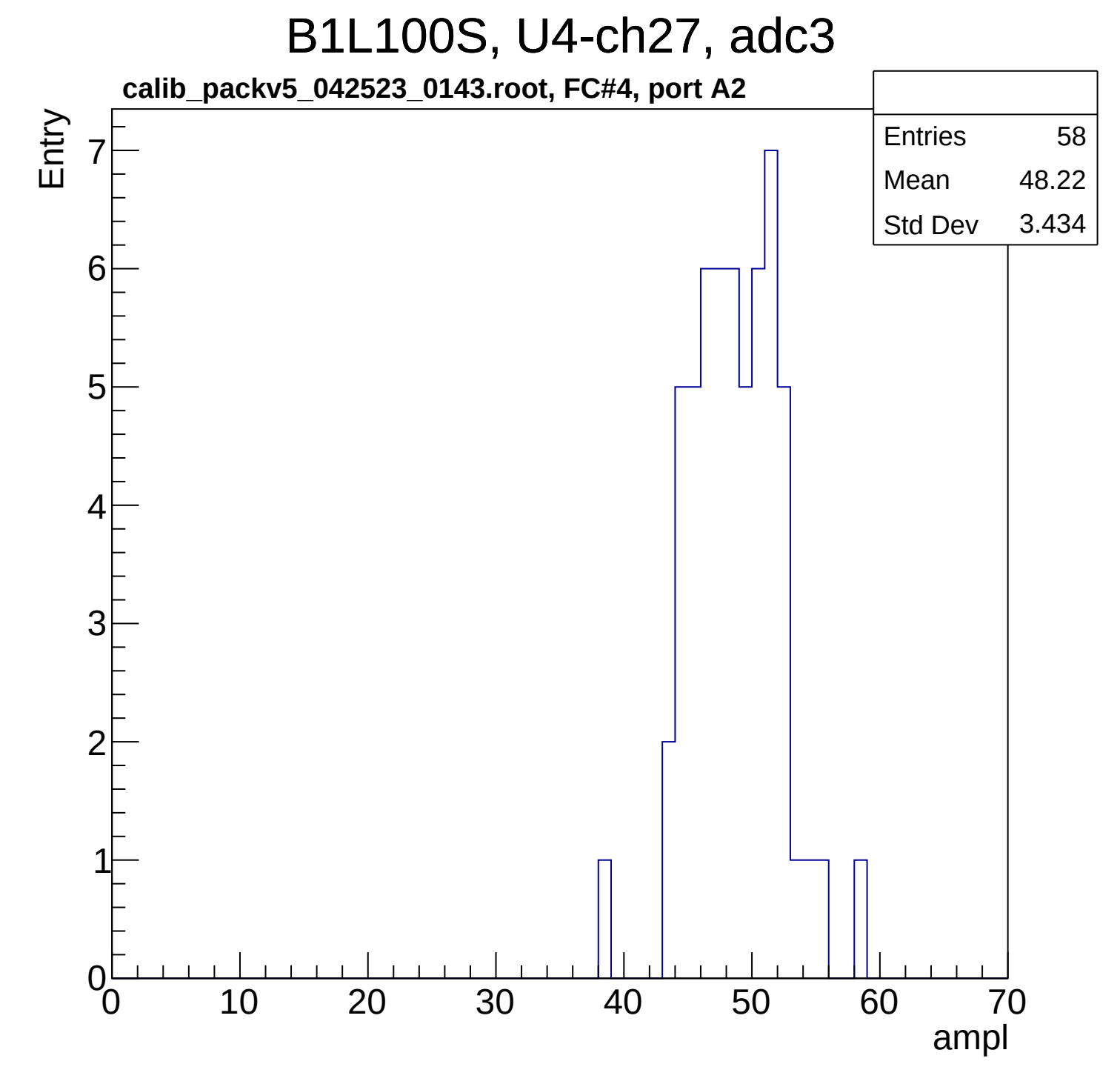

B1L100S, U4-ch26, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 62
Std Dev 1.414
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

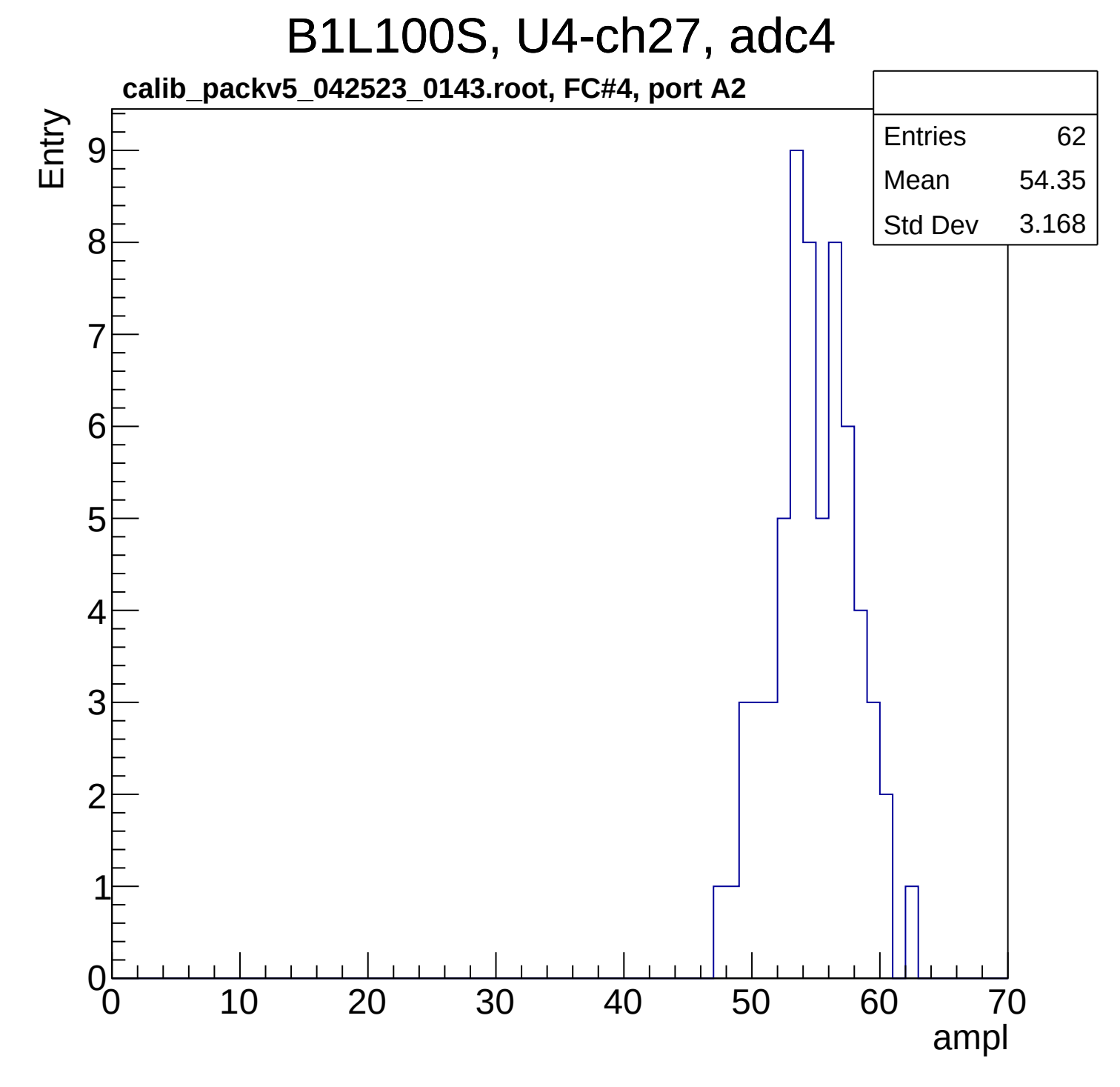

B1L100S, U4-ch26, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

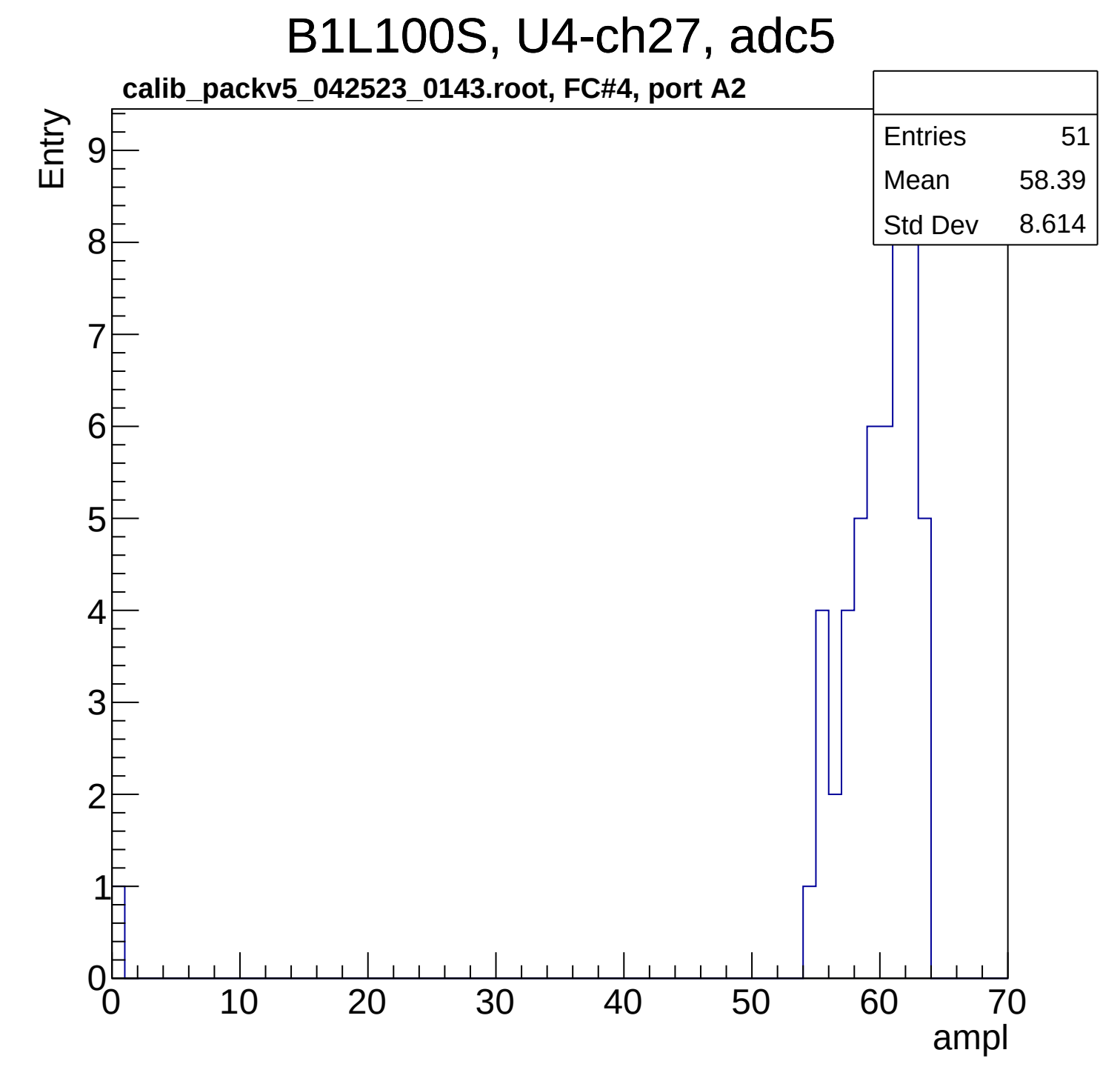

B1L100S, U4-ch27, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 28.39
Std Dev 3.478
Gaus mean : 29.0664
Gaus Width: 3.9550
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

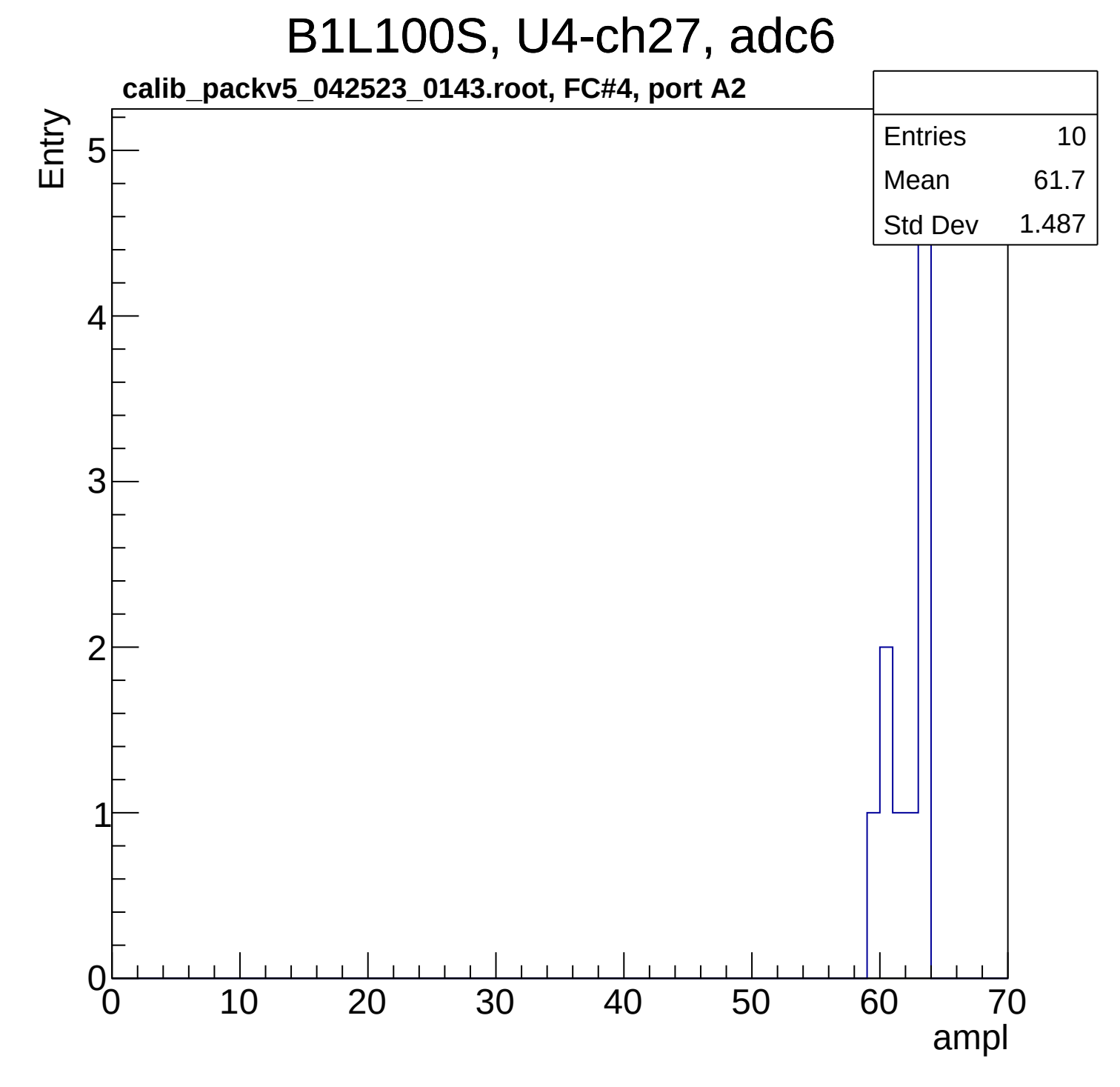

B1L100S, U4-ch27, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 35.59
Std Dev 3.114
Gaus mean : 35.9418
Gaus Width: 3.3221
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

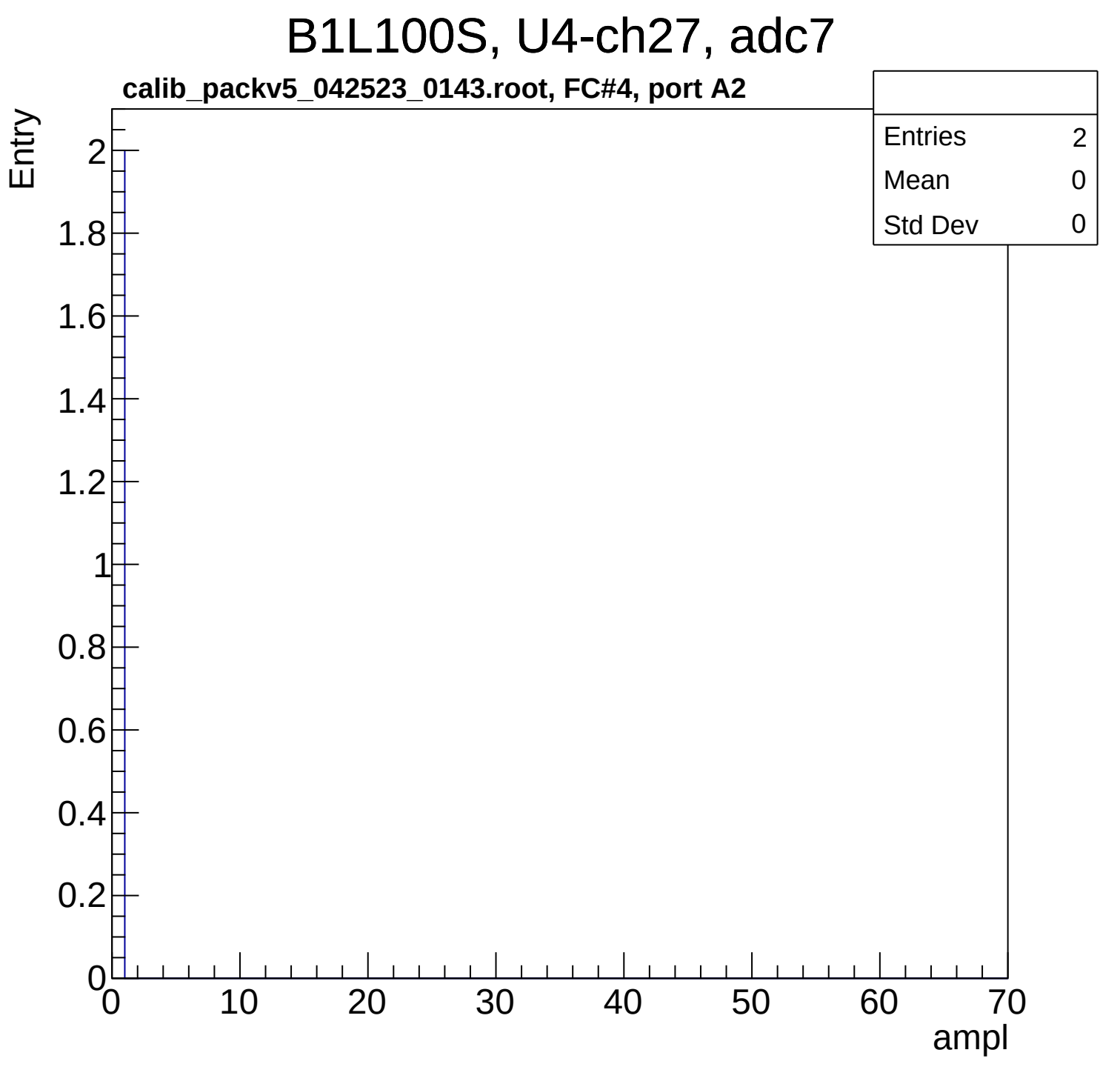

B1L100S, U4-ch27, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 41.86
Std Dev 3.772
Gaus mean : 42.8456
Gaus Width: 3.7836
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

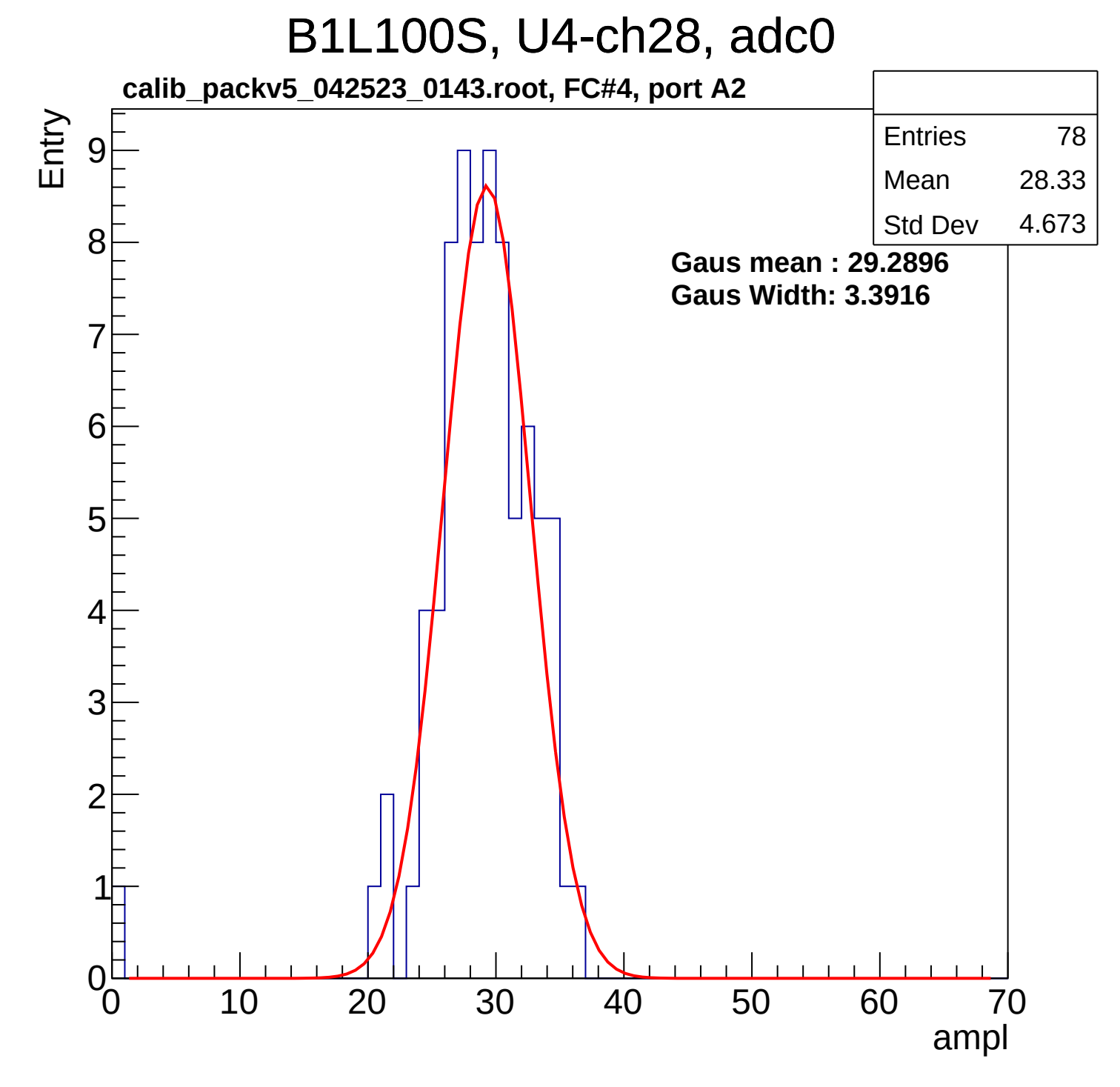

B1L100S, U4-ch27, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 48.22
Std Dev 3.434
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

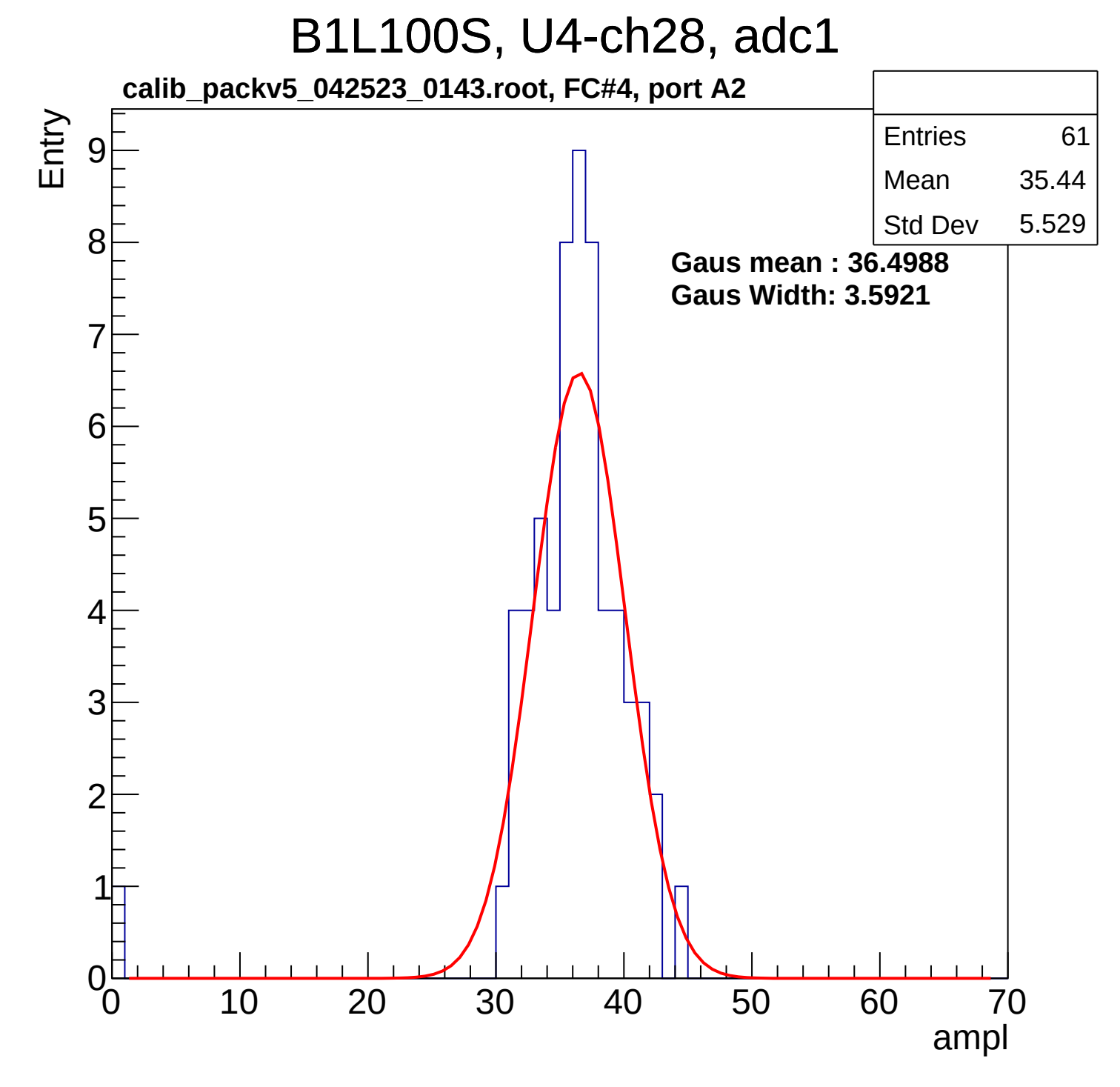

B1L100S, U4-ch27, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 54.35
Std Dev 3.168
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

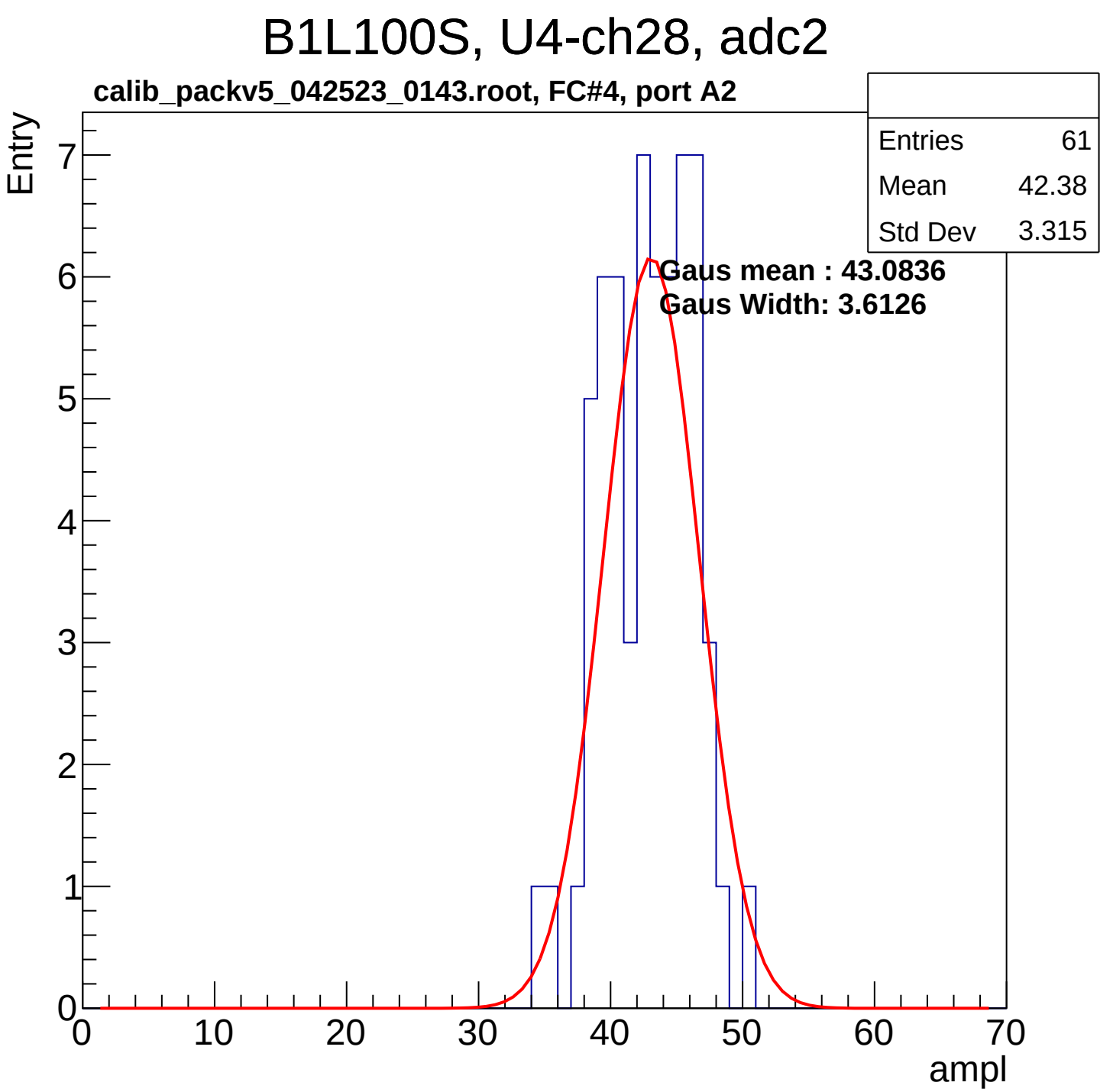

B1L100S, U4-ch27, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 58.39
Std Dev 8.614
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

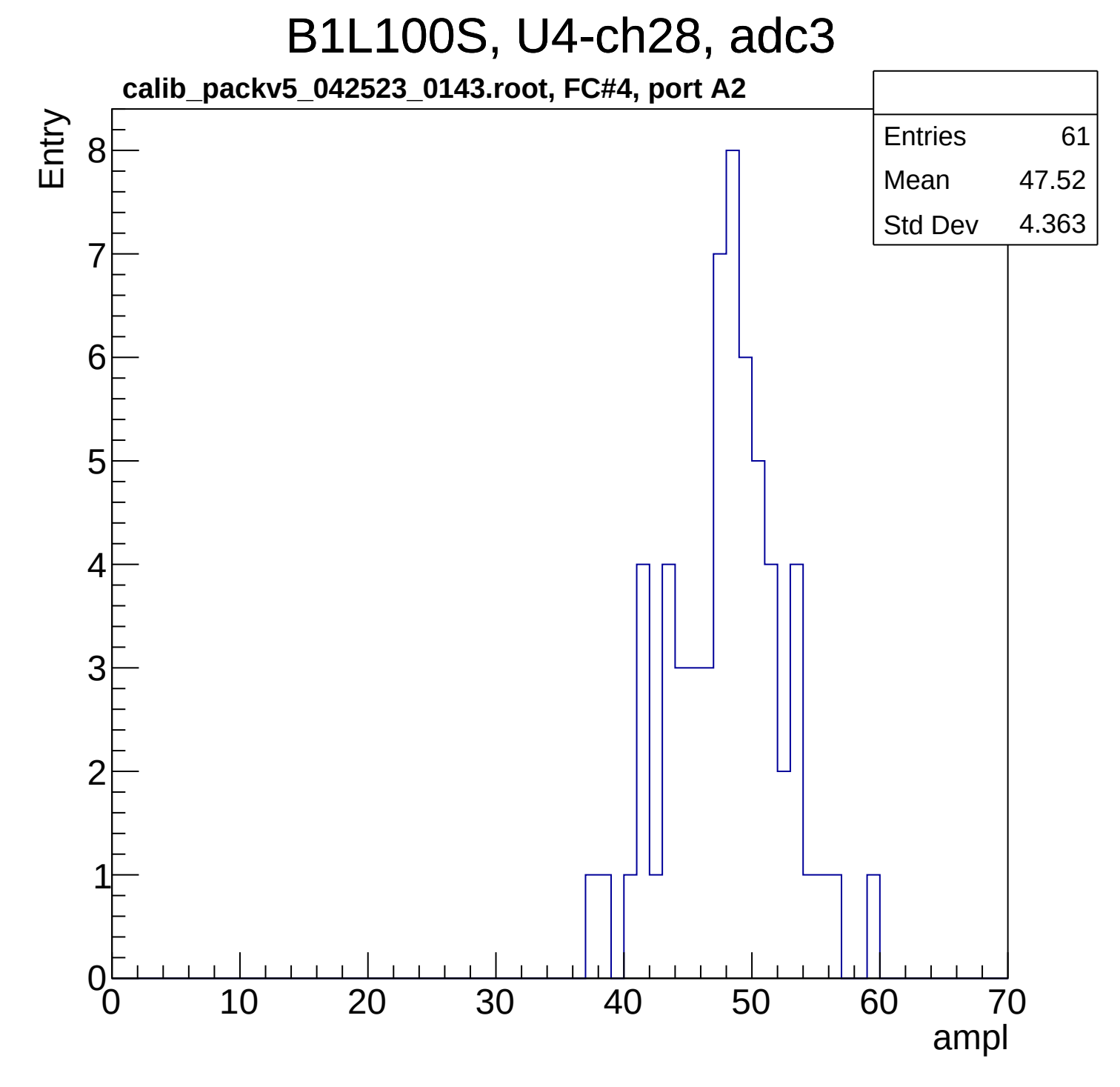

B1L100S, U4-ch27, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 61.7
Std Dev 1.487
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

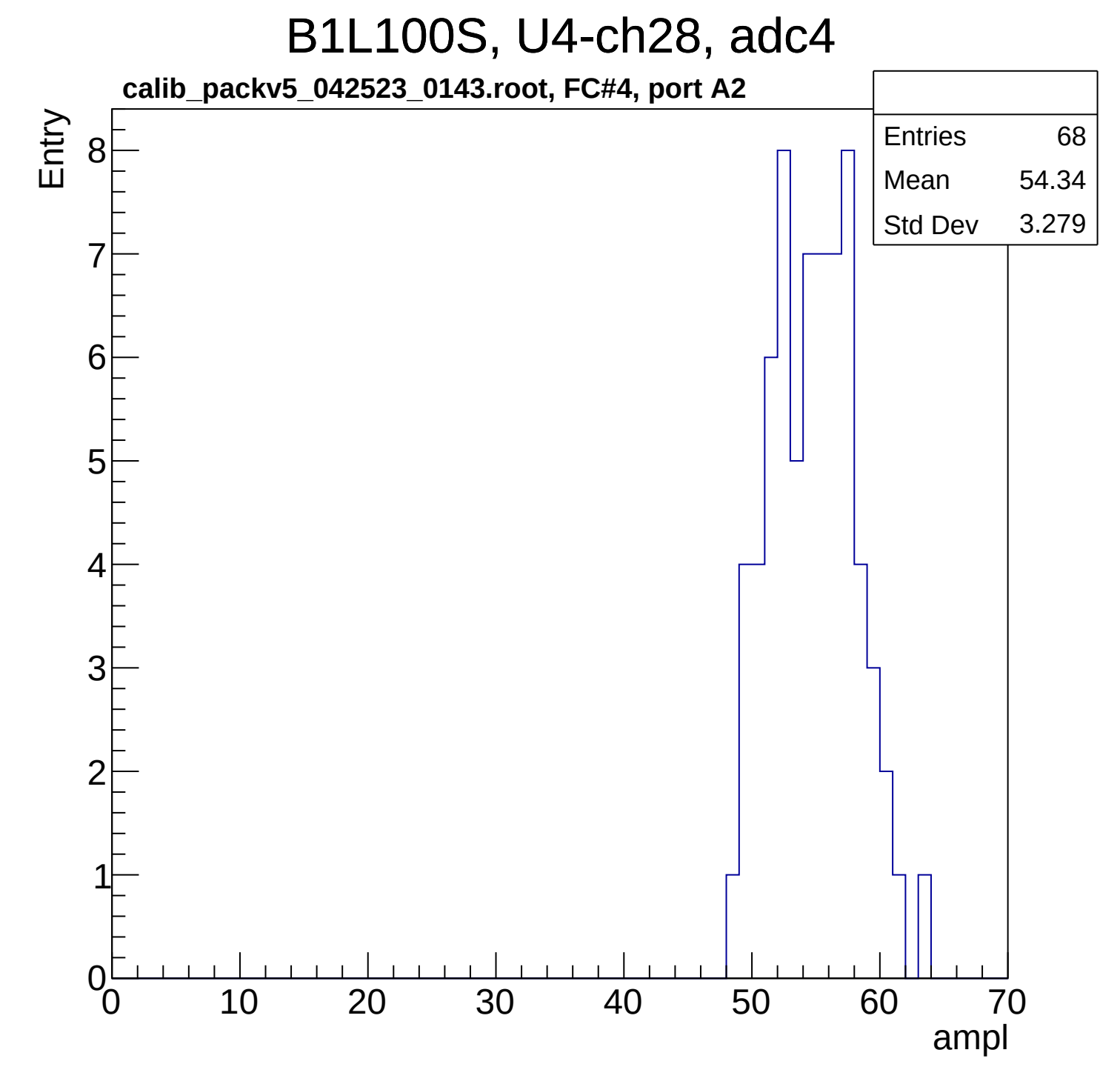

B1L100S, U4-ch27, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

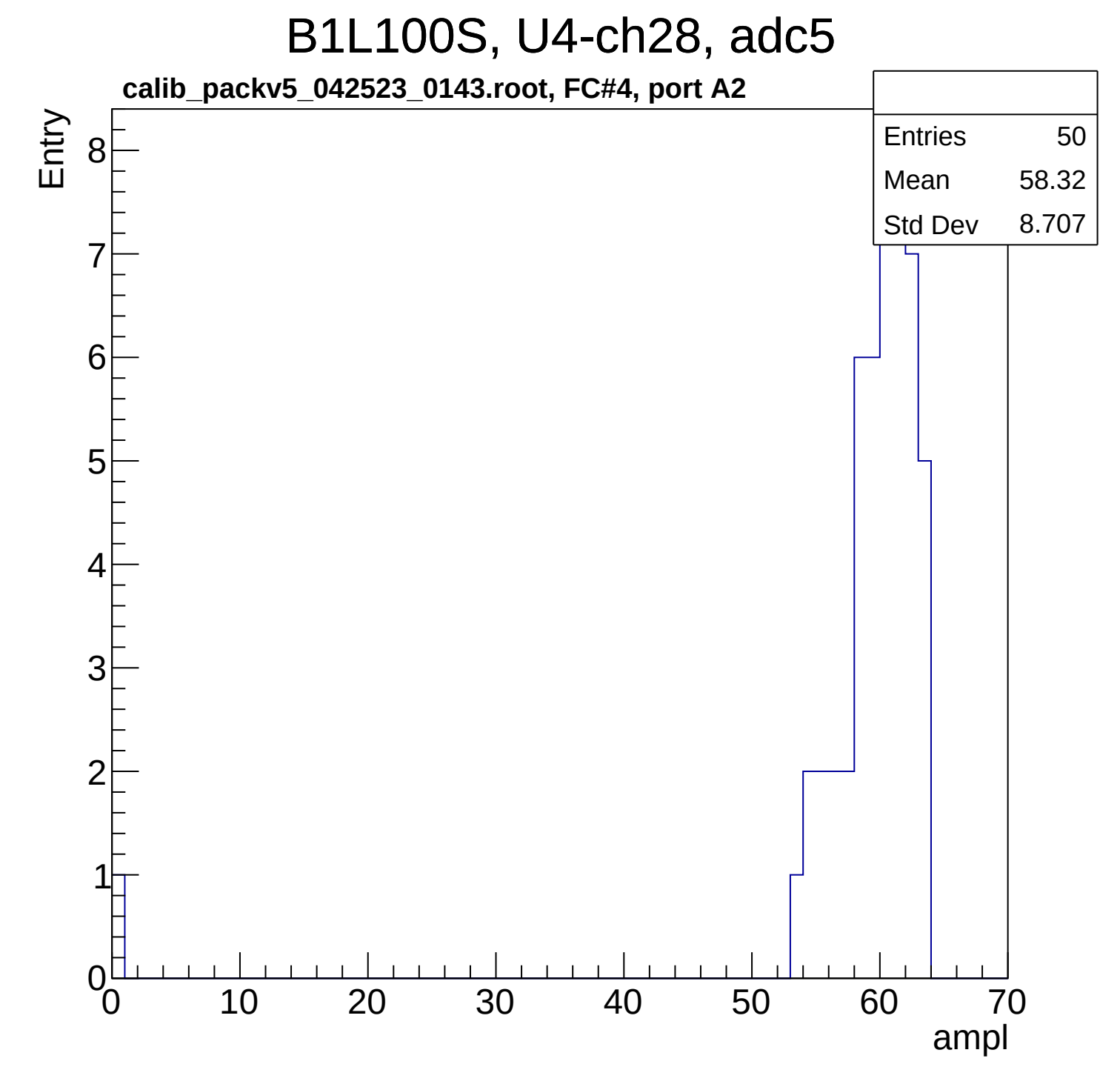

B1L100S, U4-ch28, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 28.33
Std Dev 4.673
Gaus mean : 29.2896
Gaus Width: 3.3916
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

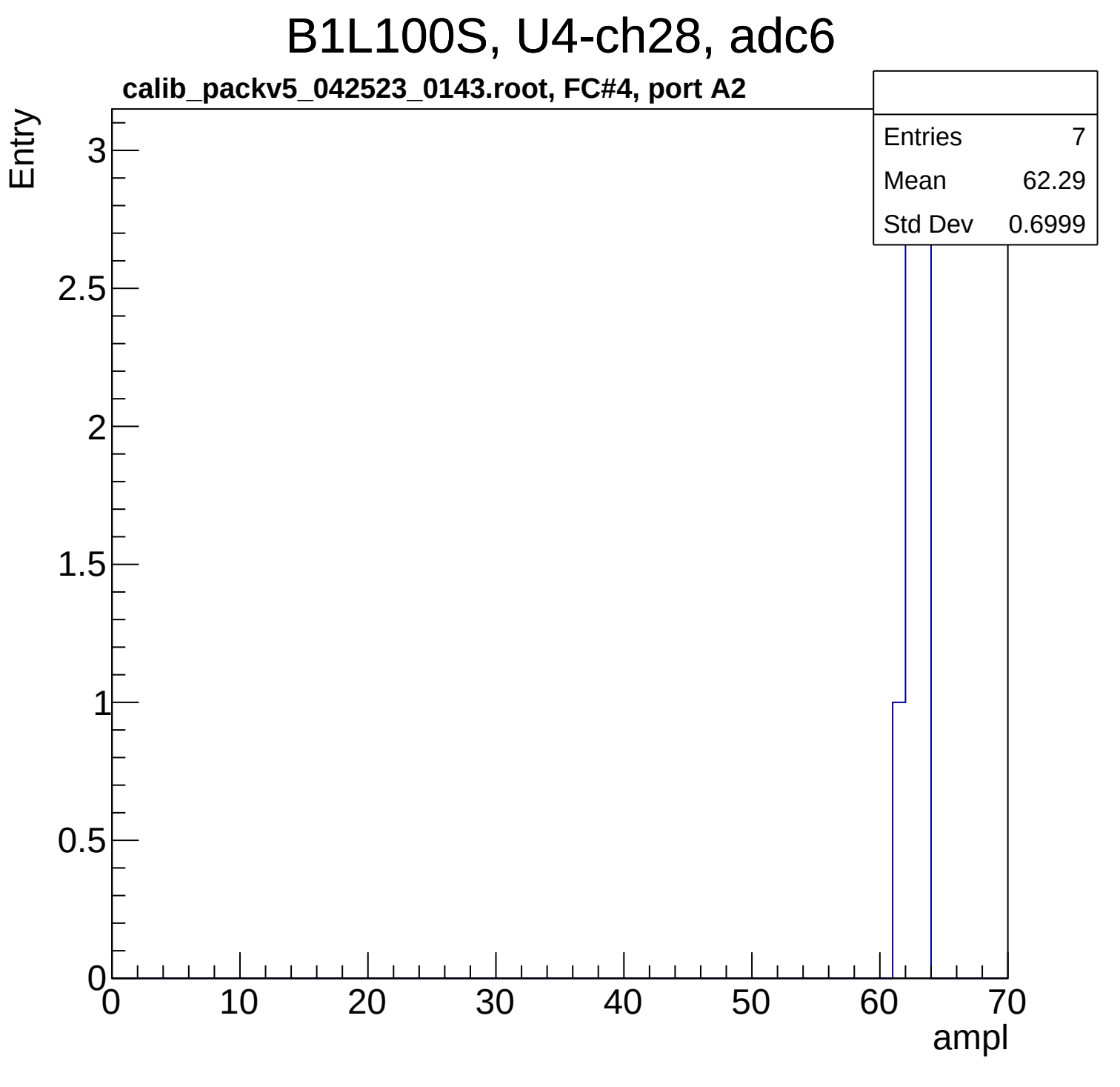

B1L100S, U4-ch28, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 35.44
Std Dev 5.529
Gaus mean : 36.4988
Gaus Width: 3.5921
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

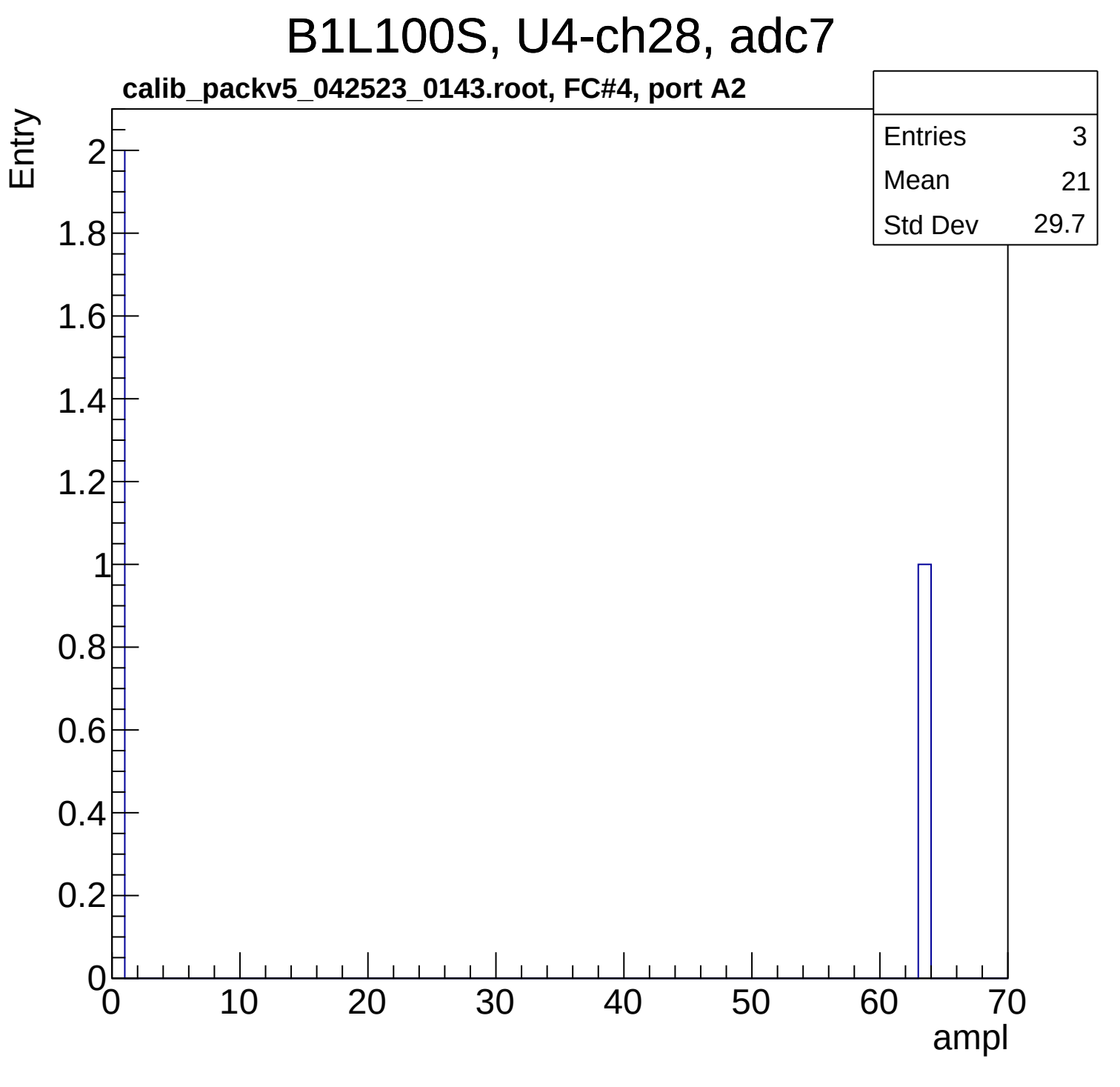

B1L100S, U4-ch28, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 42.38
Std Dev 3.315
Gaus mean : 43.0836
Gaus Width: 3.6126
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

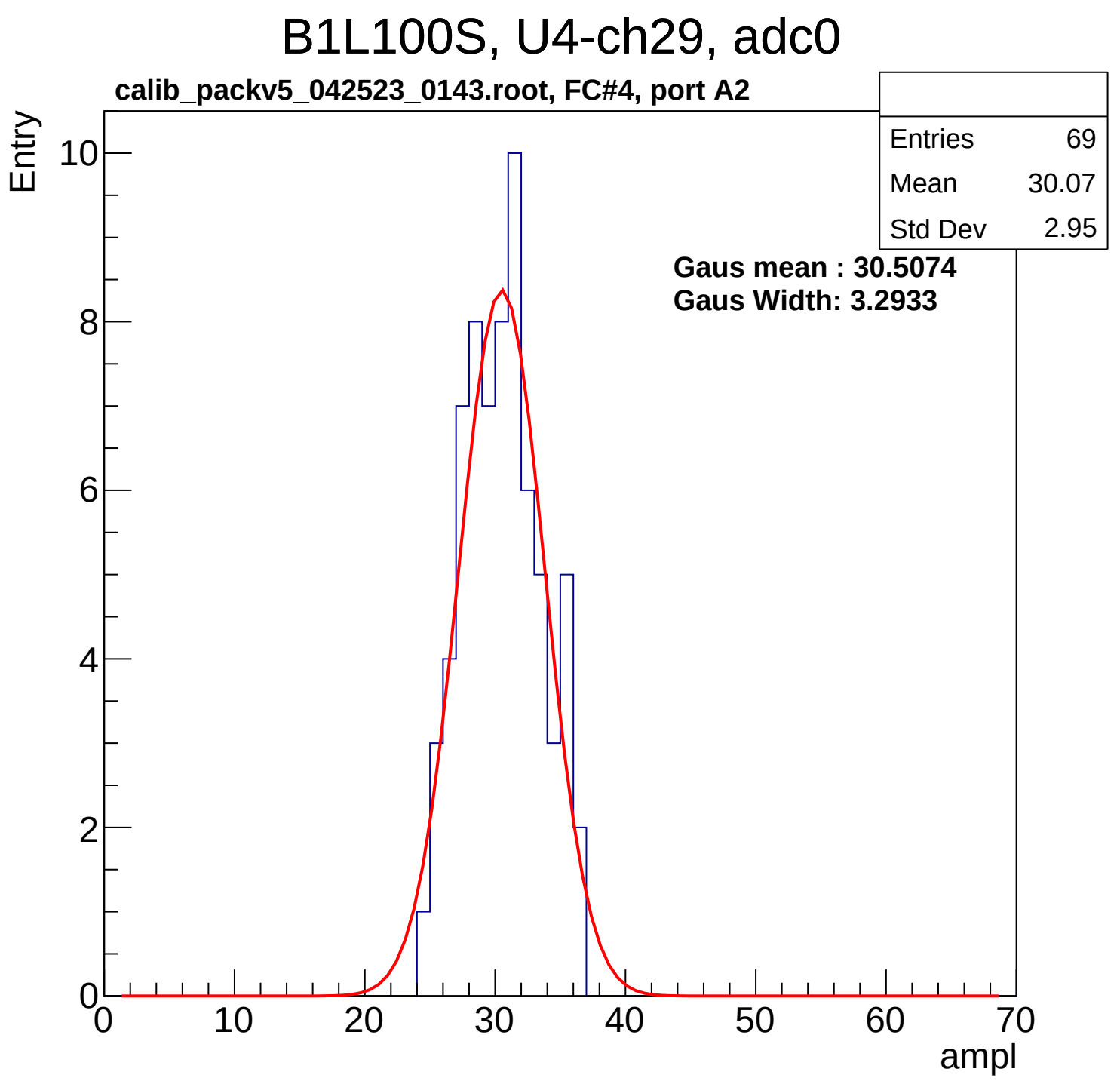

B1L100S, U4-ch28, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 47.52
Std Dev 4.363
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

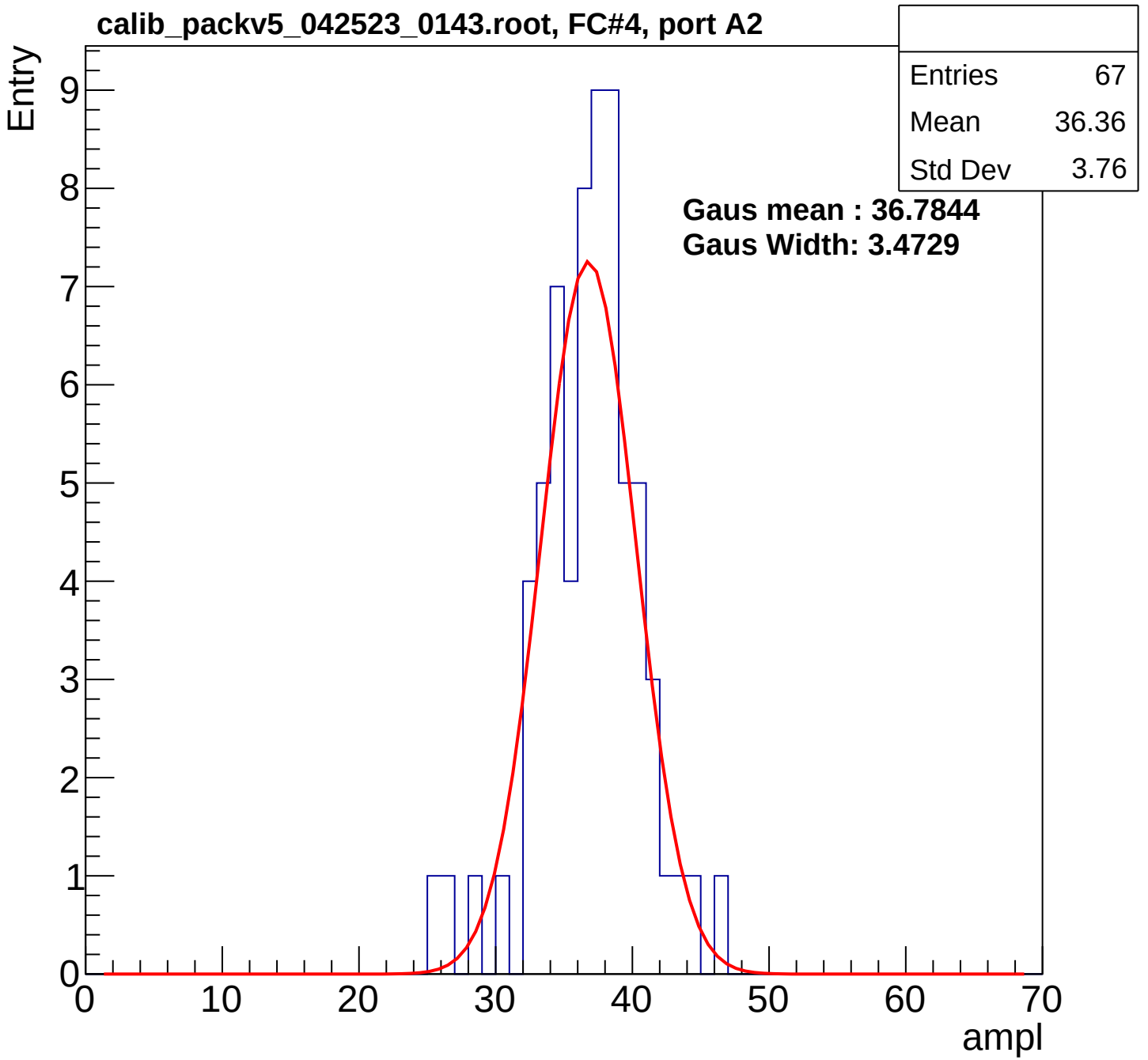

B1L100S, U4-ch28, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 54.34
Std Dev 3.279
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

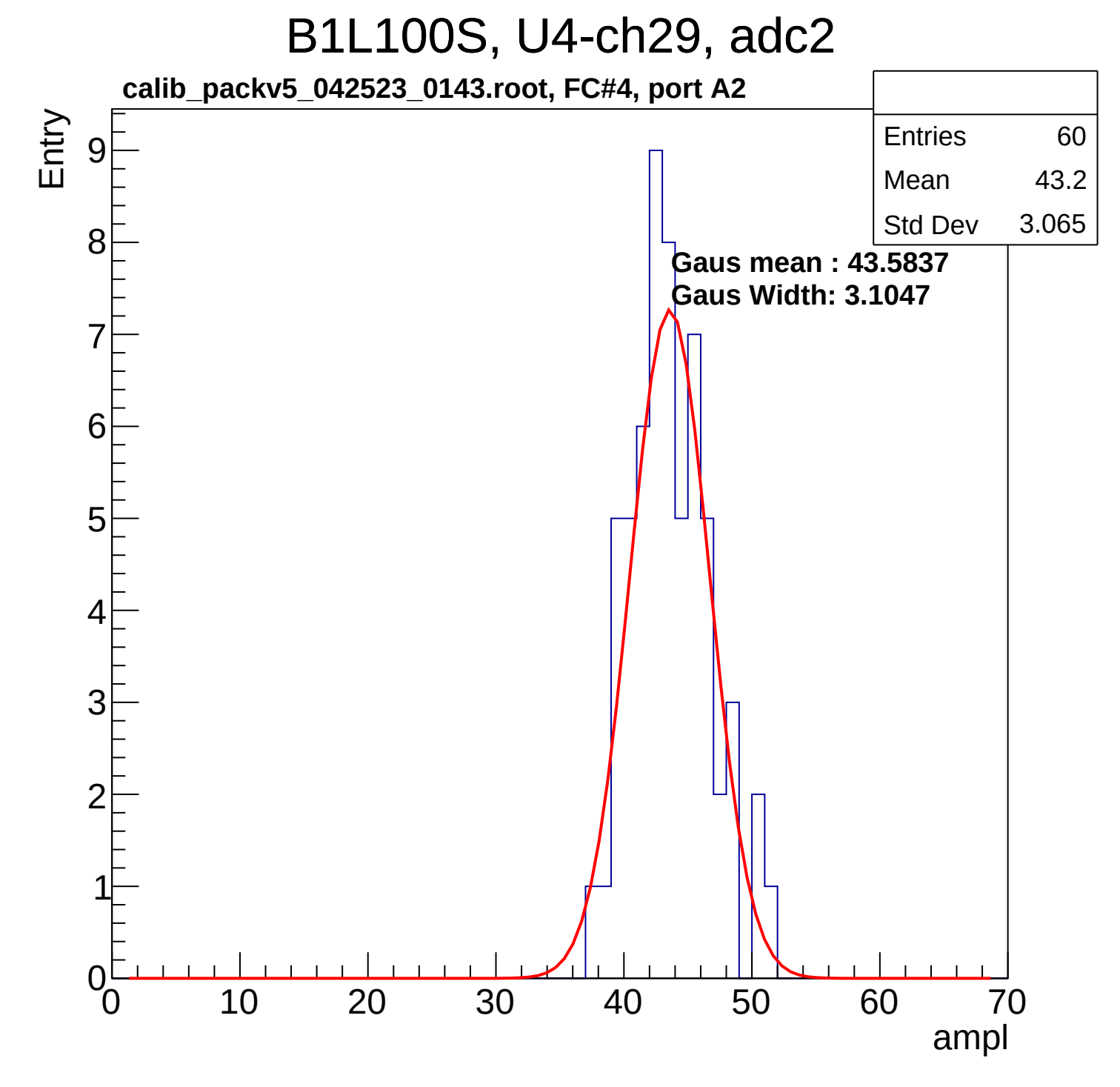

B1L100S, U4-ch28, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 58.32
Std Dev 8.707
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

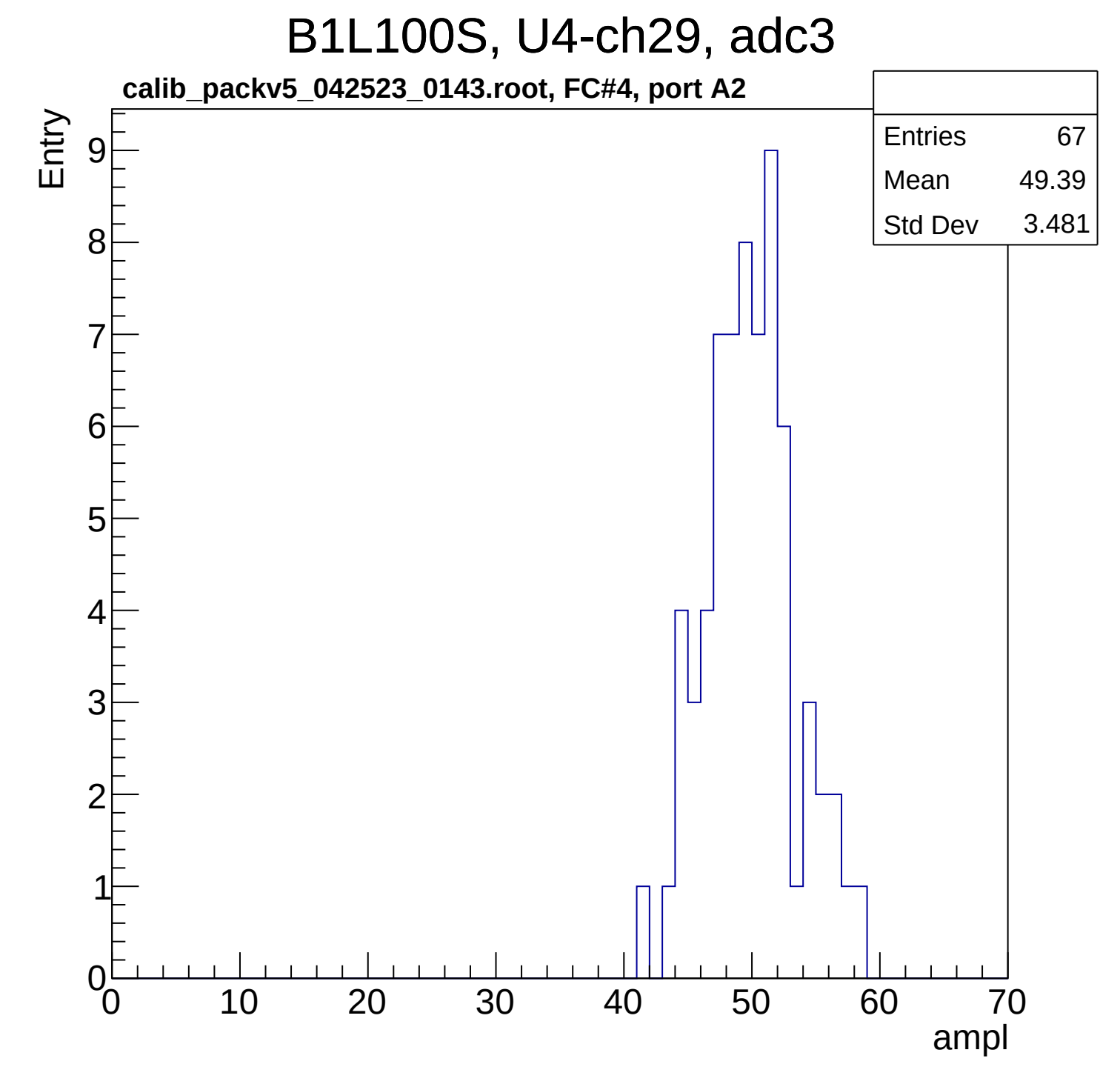

B1L100S, U4-ch28, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 62.29
Std Dev 0.6999
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

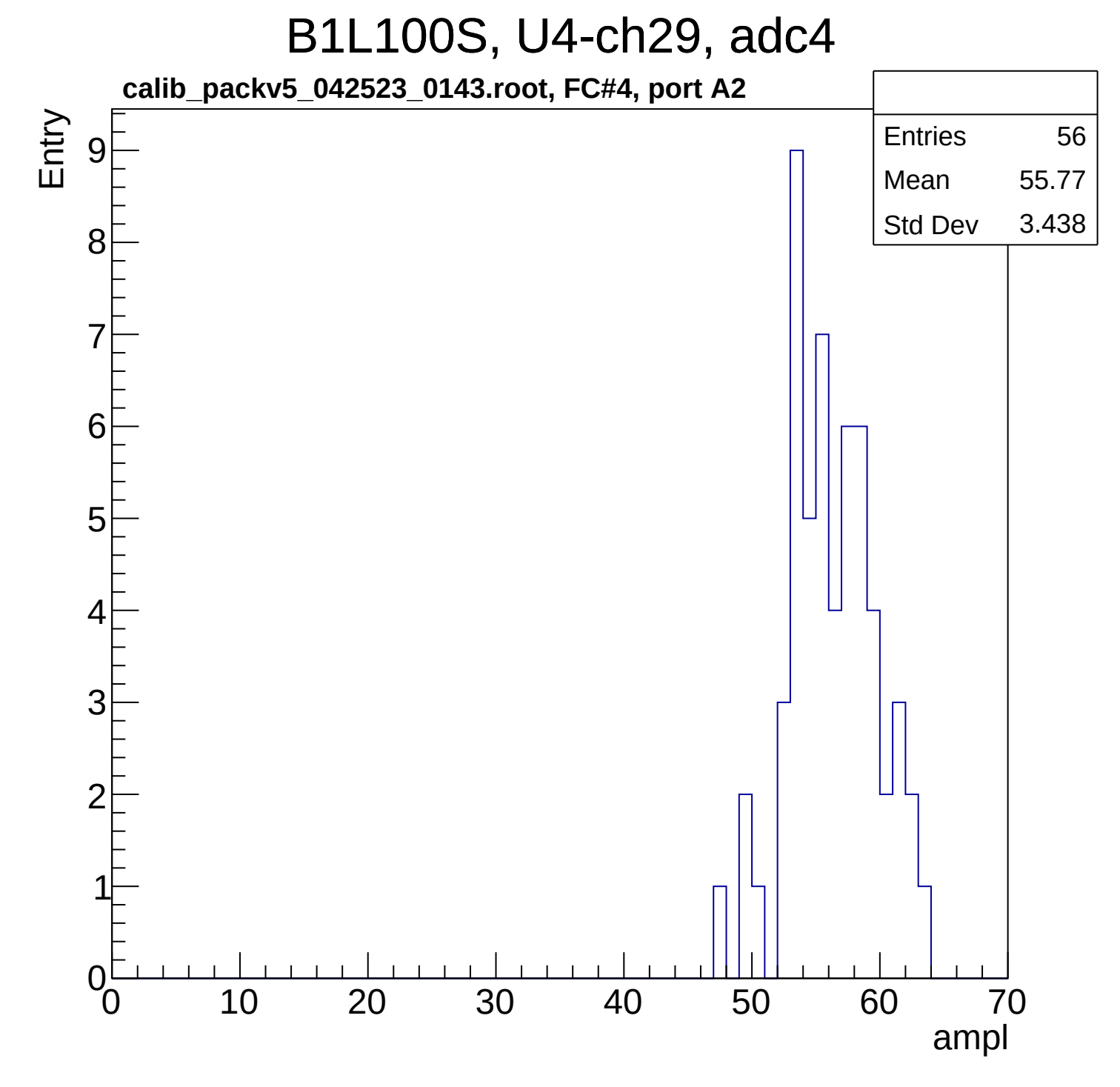

B1L100S, U4-ch28, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 21
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

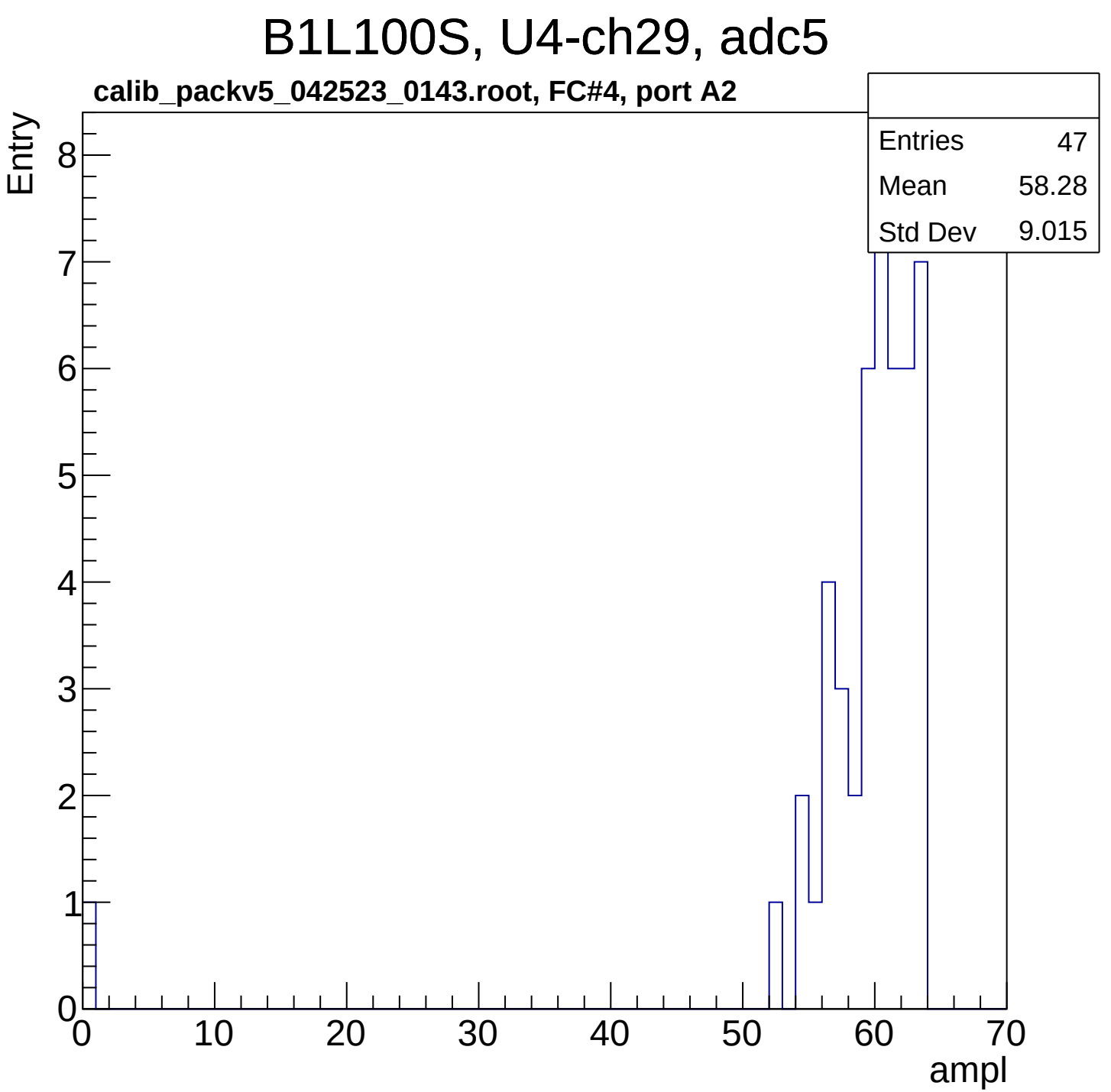

B1L100S, U4-ch29, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 30.07
Std Dev 2.95
Gaus mean : 30.5074
Gaus Width: 3.2933
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

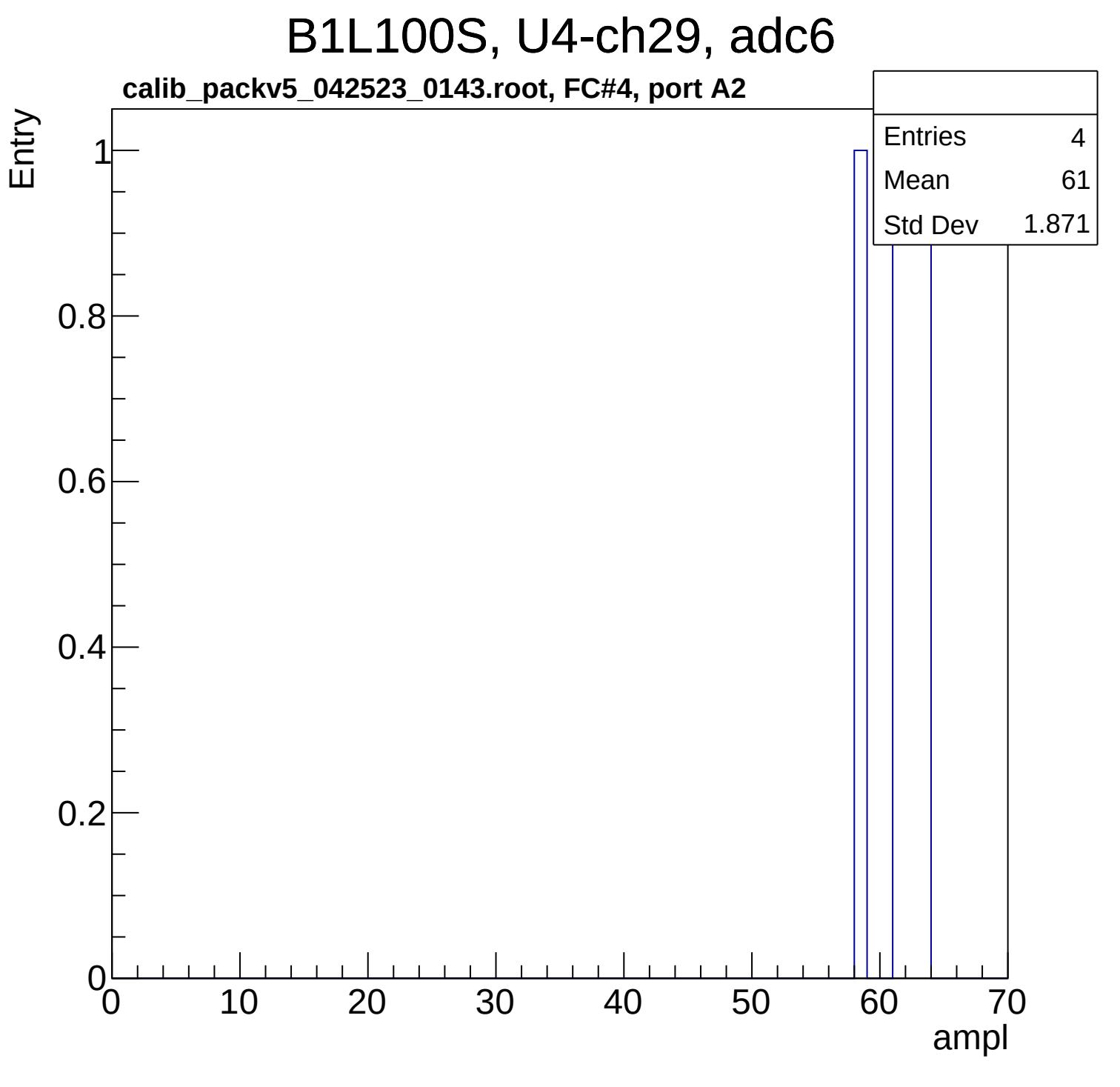

B1L100S, U4-ch29, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 36.36
Std Dev 3.76
Gaus mean : 36.7844
Gaus Width: 3.4729
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

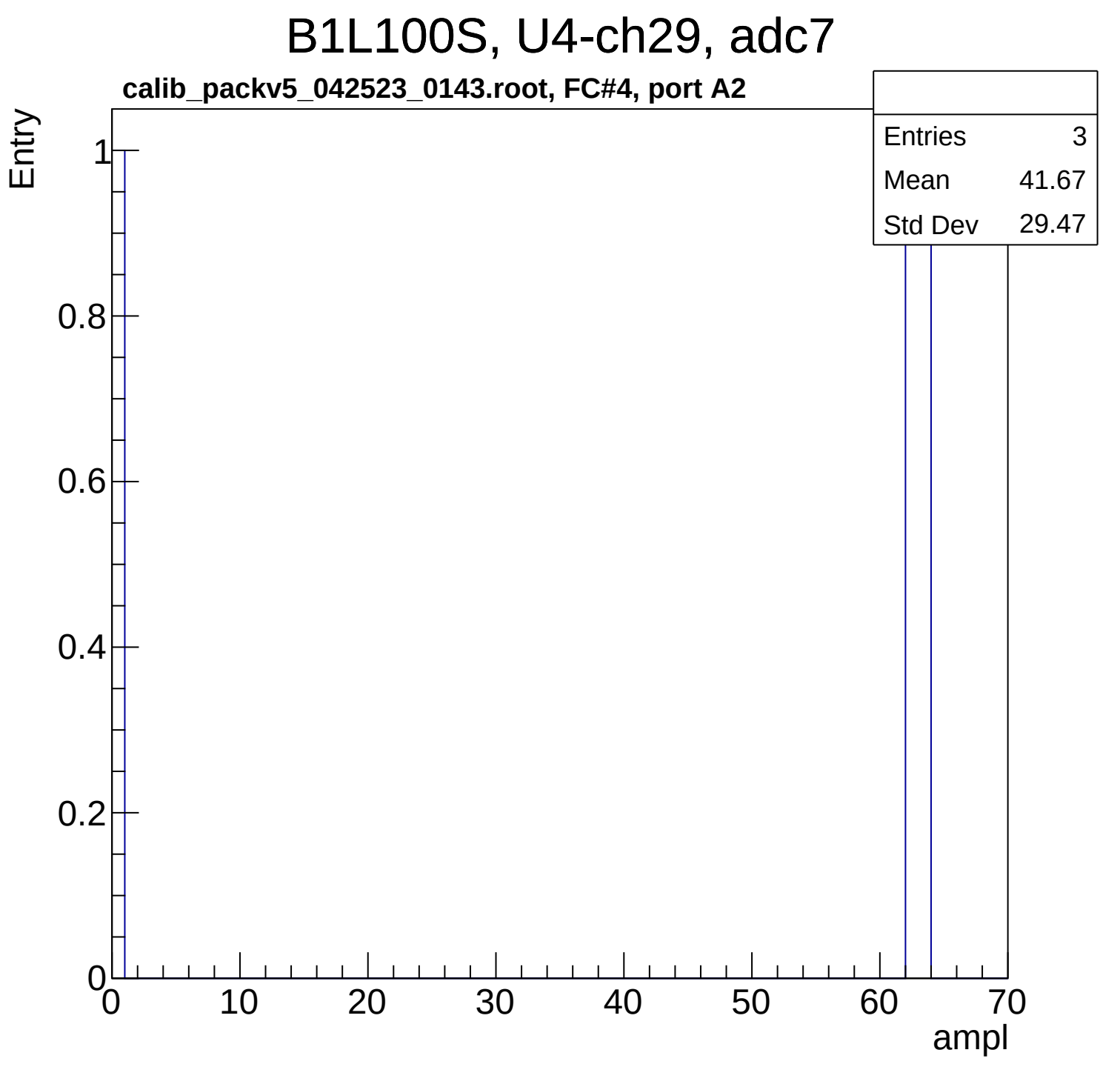

B1L100S, U4-ch29, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 43.2
Std Dev 3.065
Gaus mean : 43.5837
Gaus Width: 3.1047
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

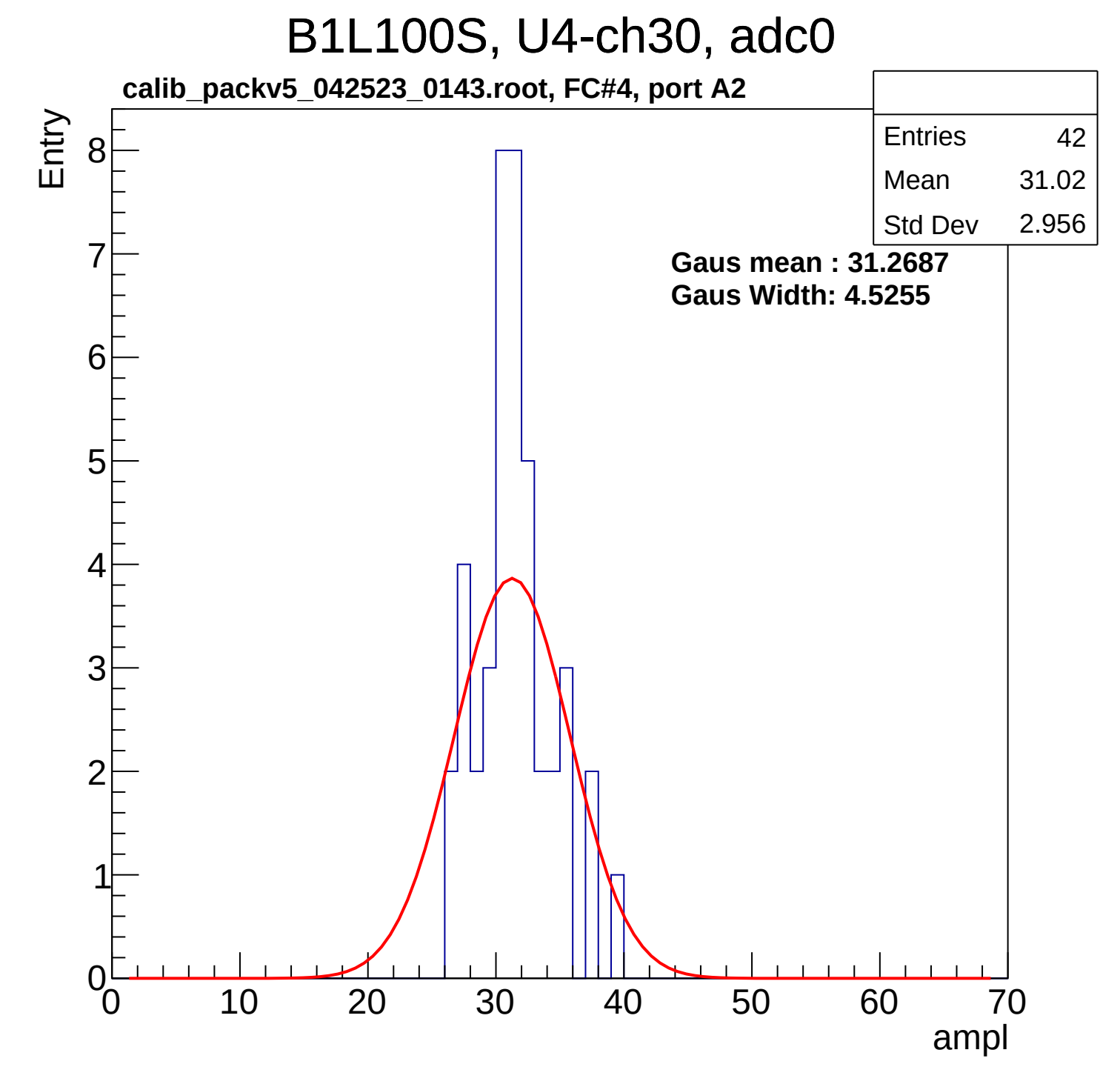

B1L100S, U4-ch29, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 49.39
Std Dev 3.481
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

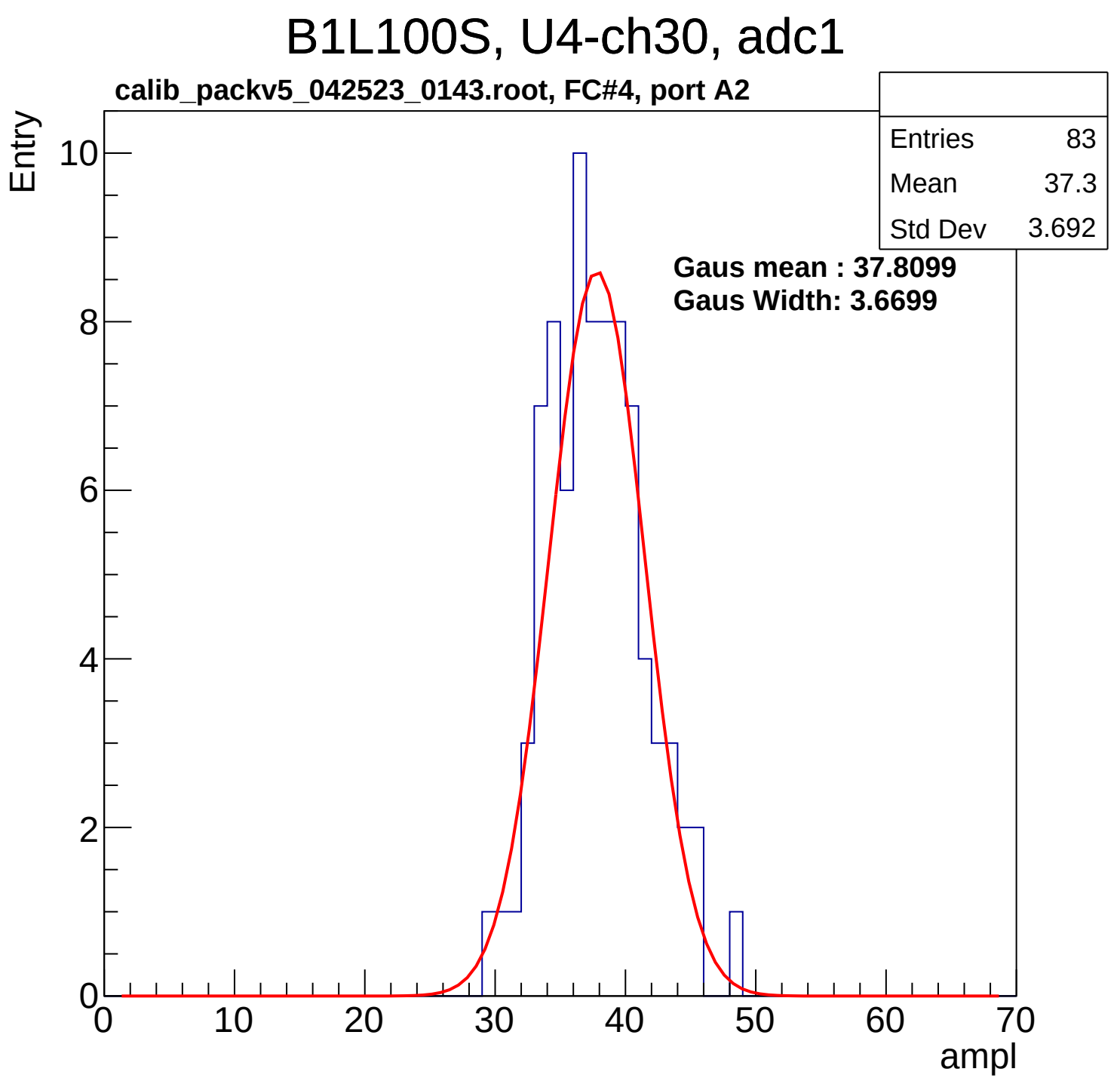

B1L100S, U4-ch29, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 55.77
Std Dev 3.438
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

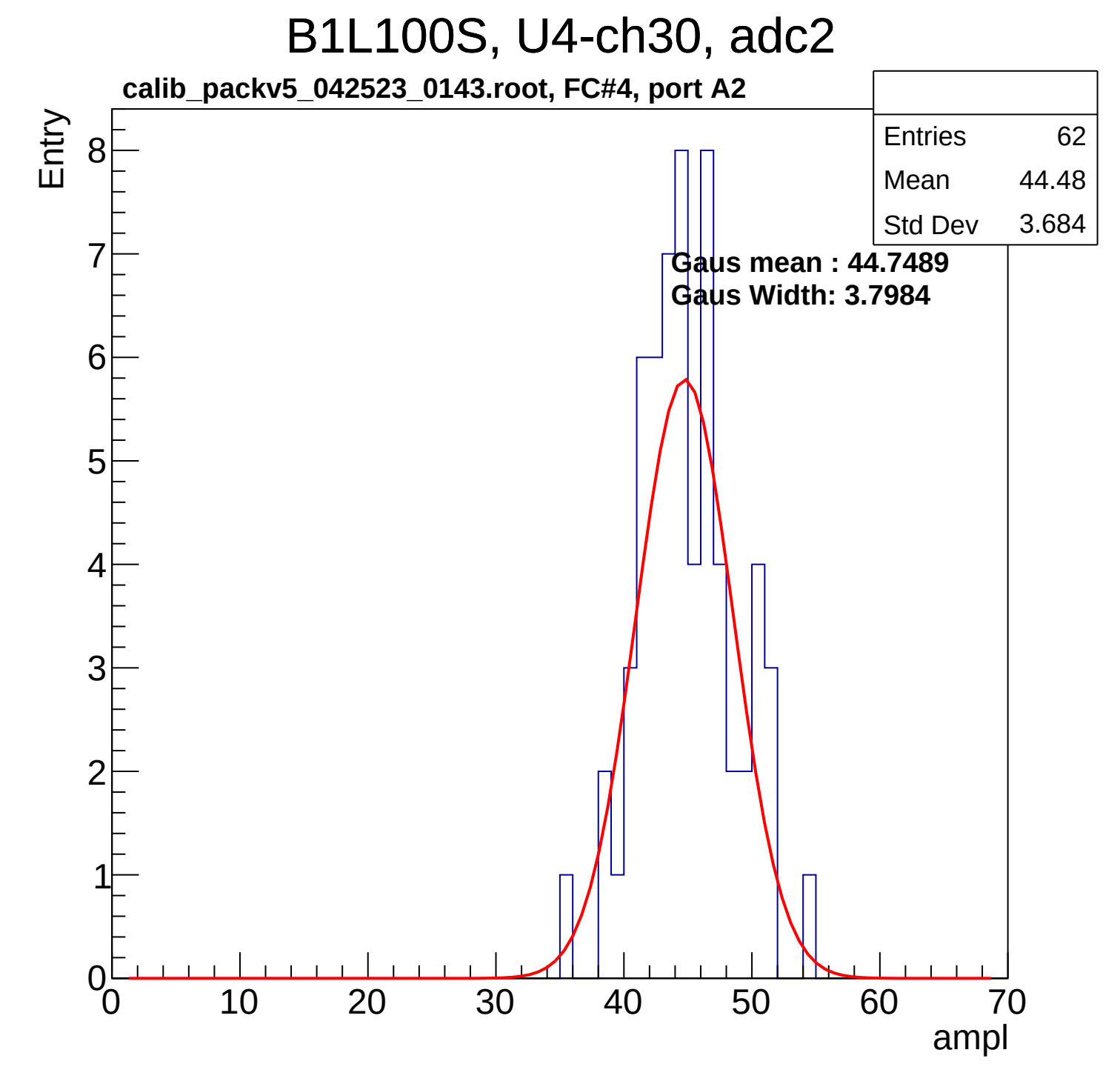

B1L100S, U4-ch29, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 58.28
Std Dev 9.015
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

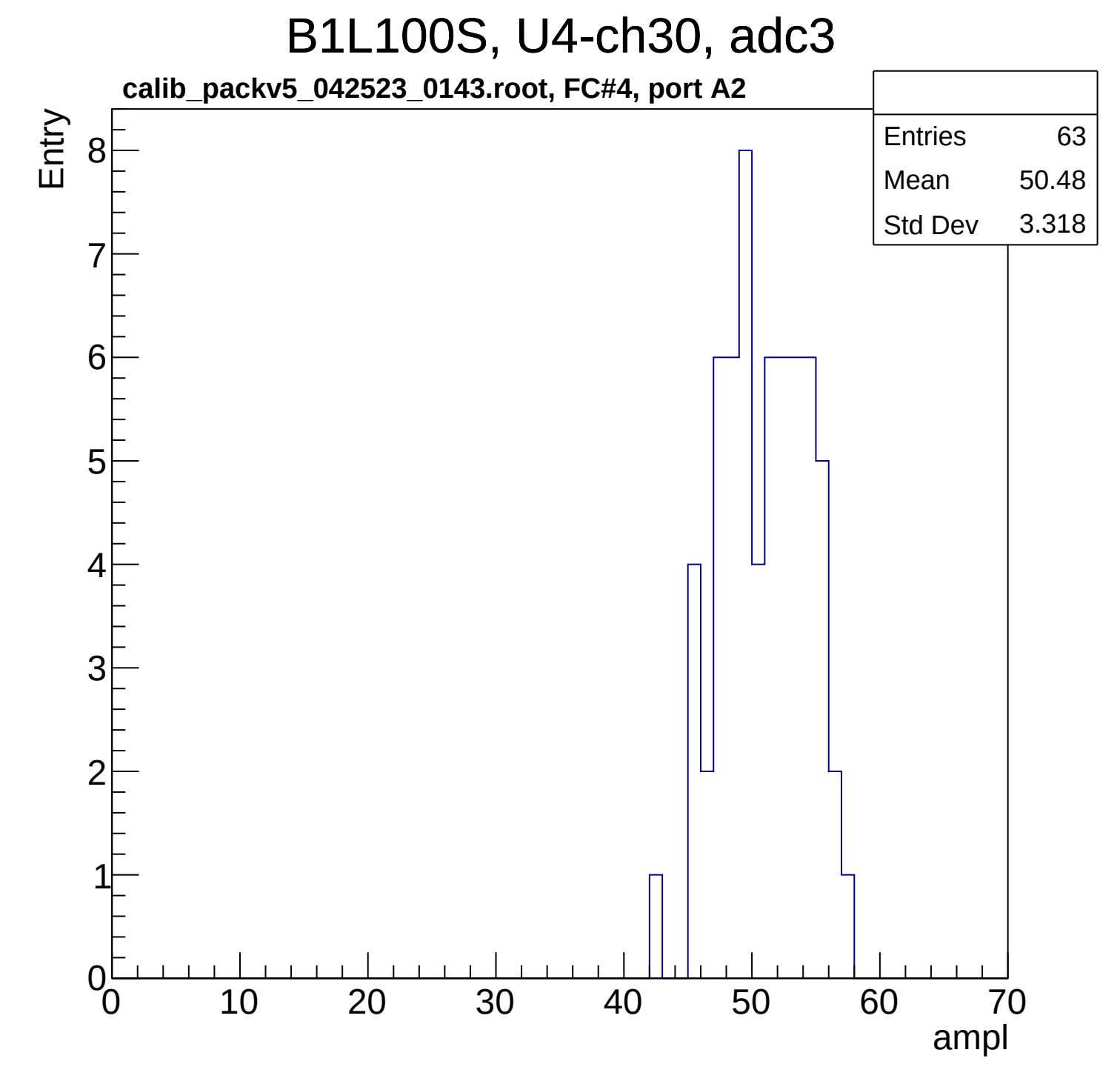

B1L100S, U4-ch29, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 61
Std Dev 1.871
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

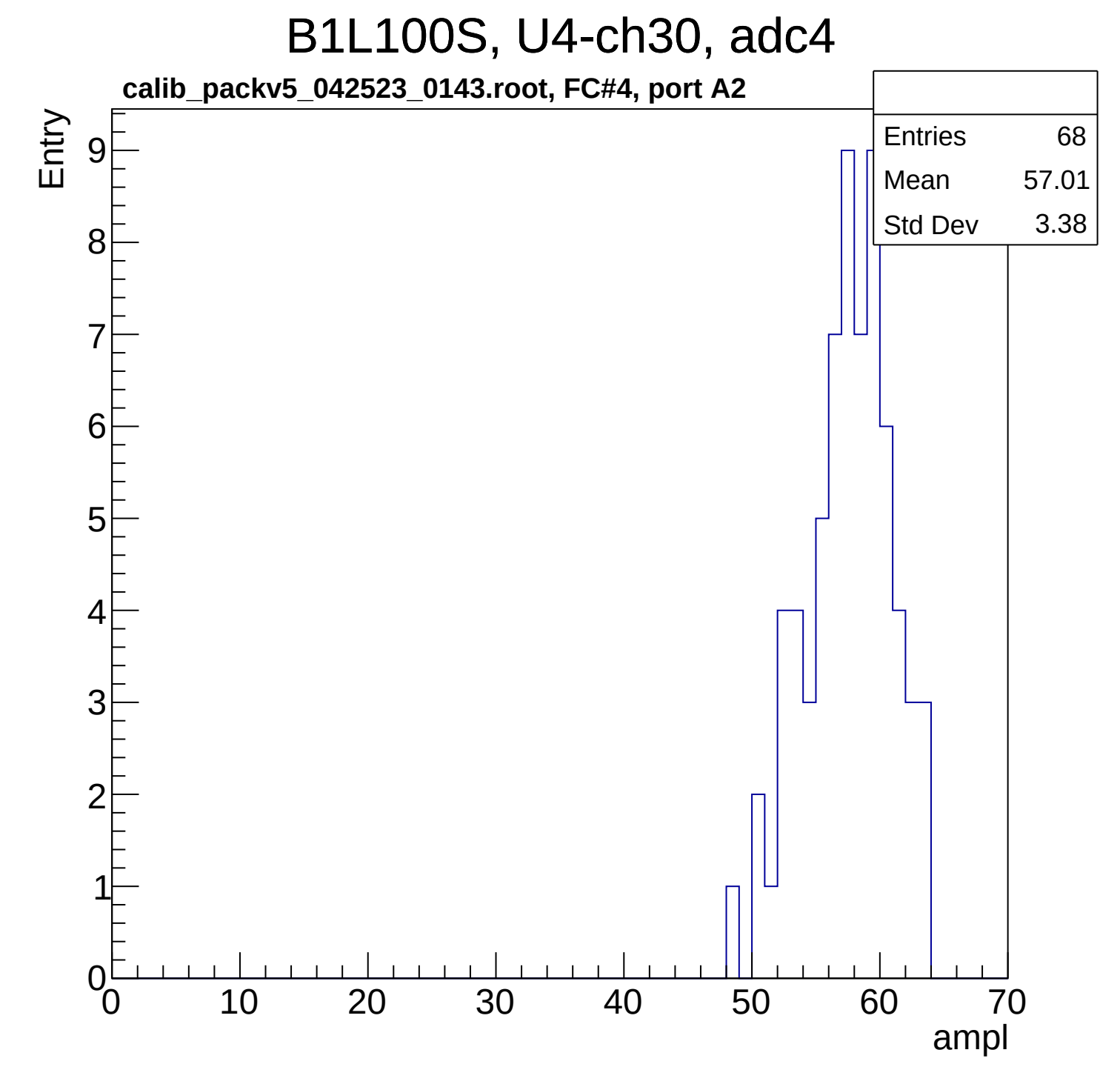

B1L100S, U4-ch29, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 41.67
Std Dev 29.47
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

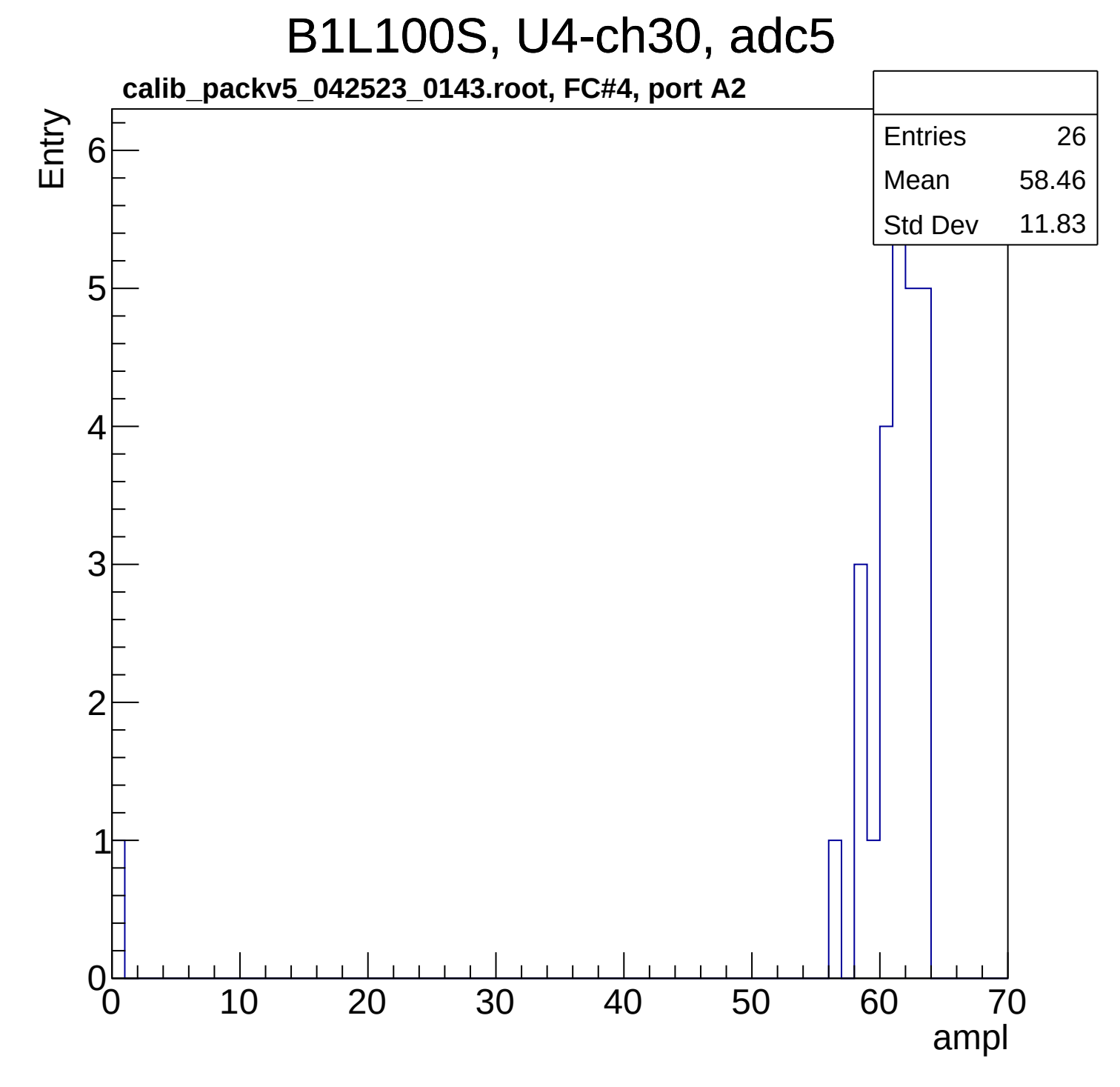

B1L100S, U4-ch30, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 42
Mean 31.02
Std Dev 2.956
Gaus mean : 31.2687
Gaus Width: 4.5255
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

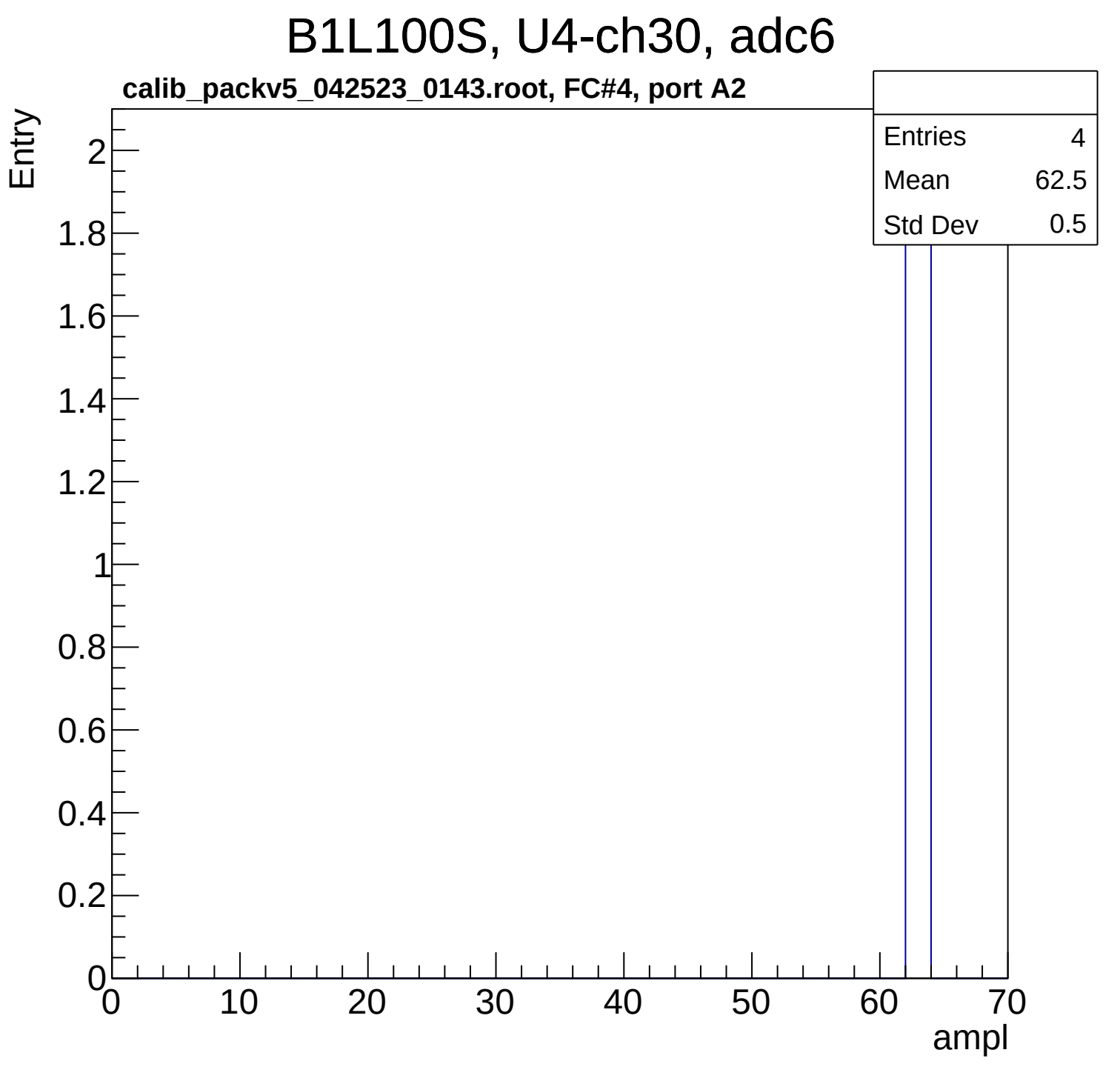

B1L100S, U4-ch30, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 83
Mean 37.3
Std Dev 3.692
Gaus mean : 37.8099
Gaus Width: 3.6699
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

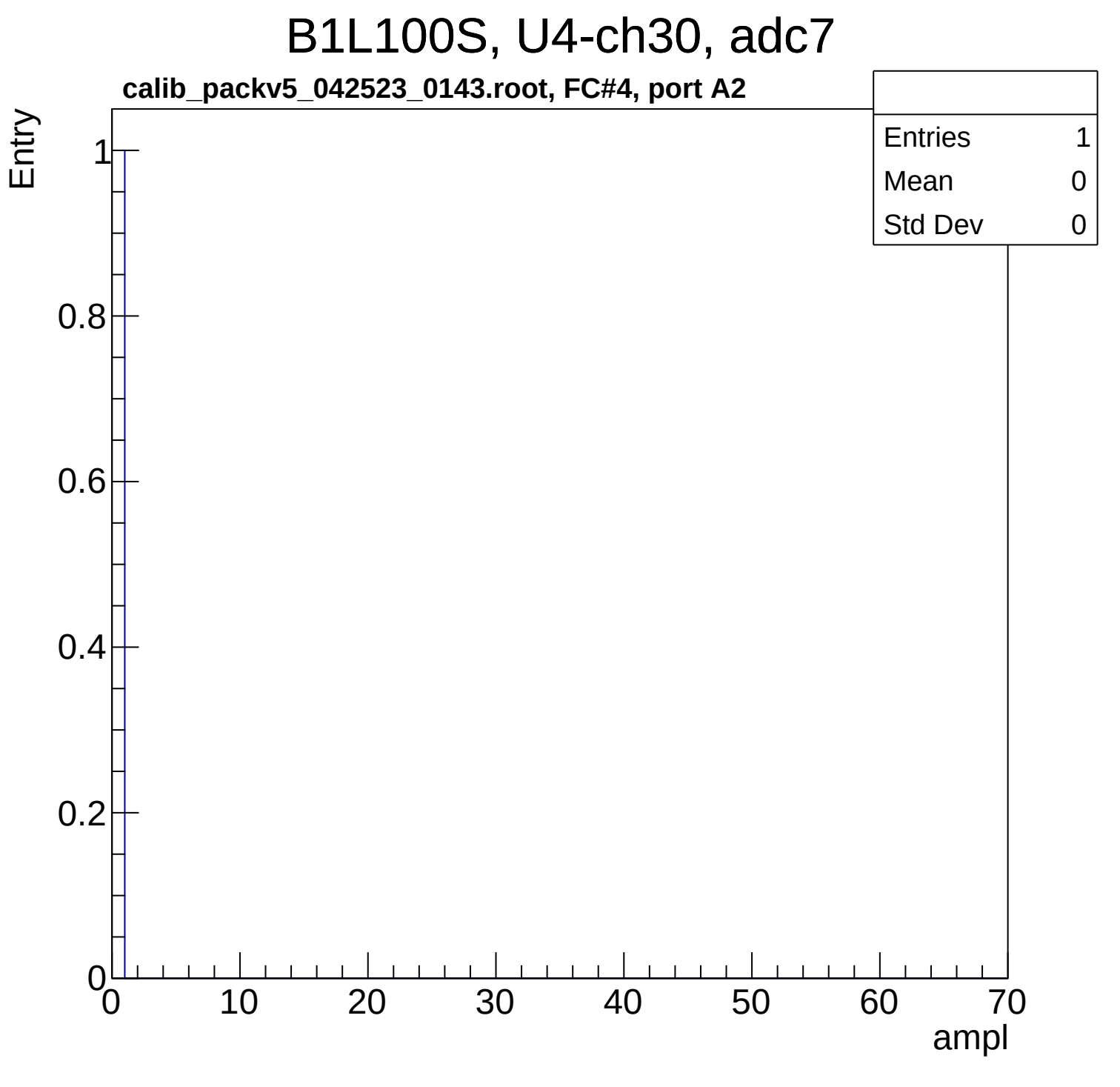

B1L100S, U4-ch30, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 44.48
Std Dev 3.684
Gaus mean : 44.7489
Gaus Width: 3.7984
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

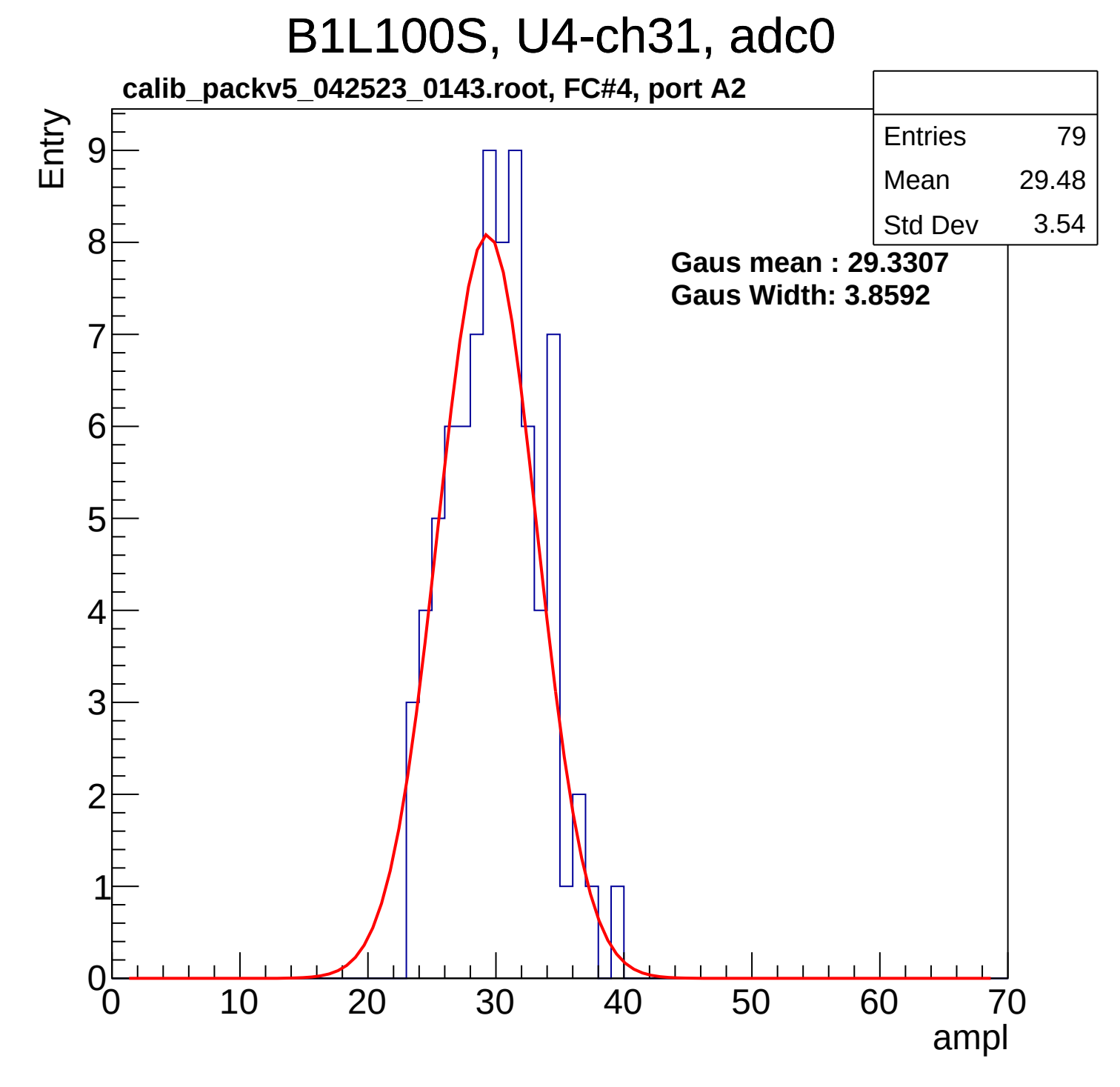

B1L100S, U4-ch30, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 50.48
Std Dev 3.318
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

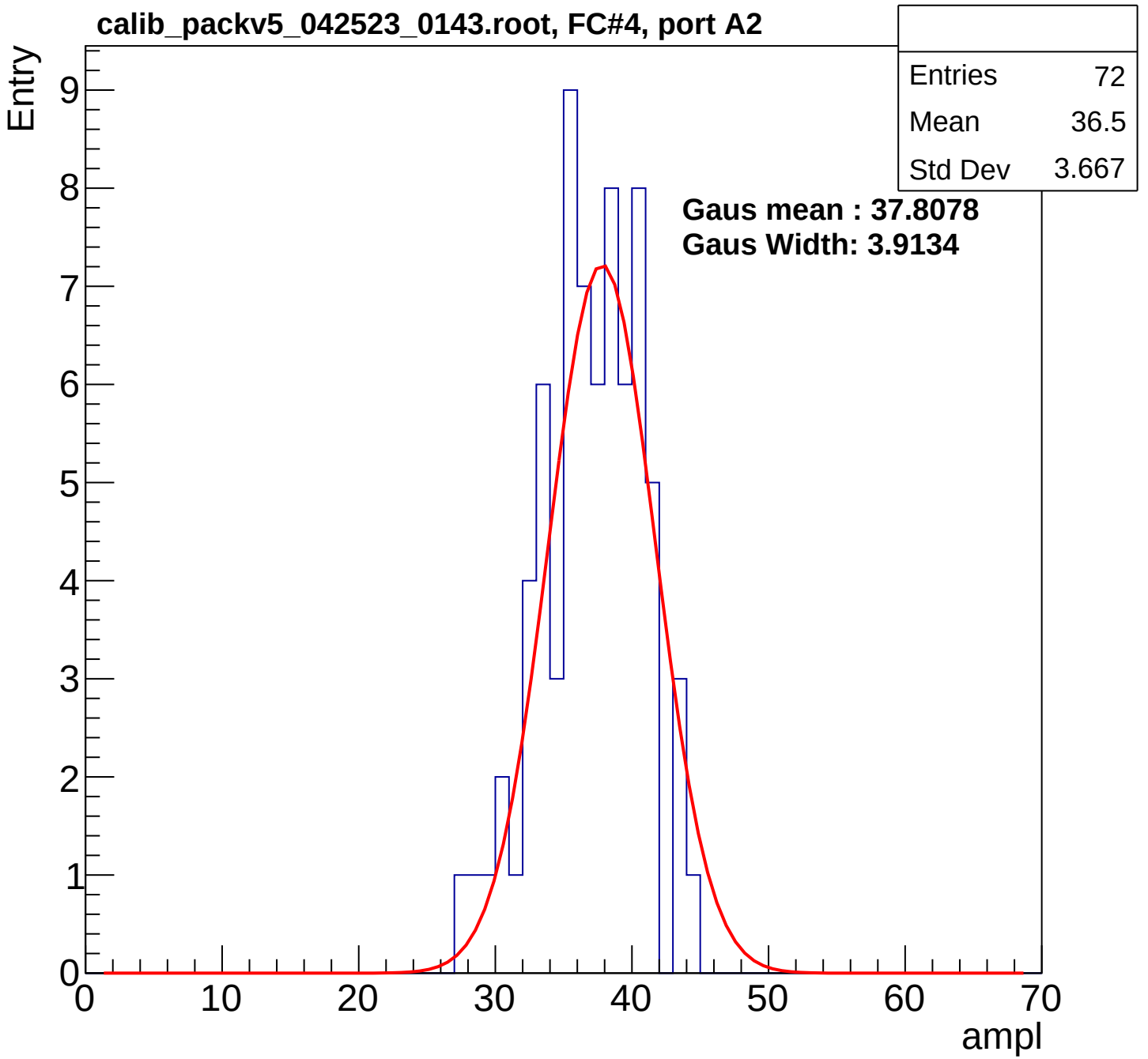

B1L100S, U4-ch30, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 57.01
Std Dev 3.38
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

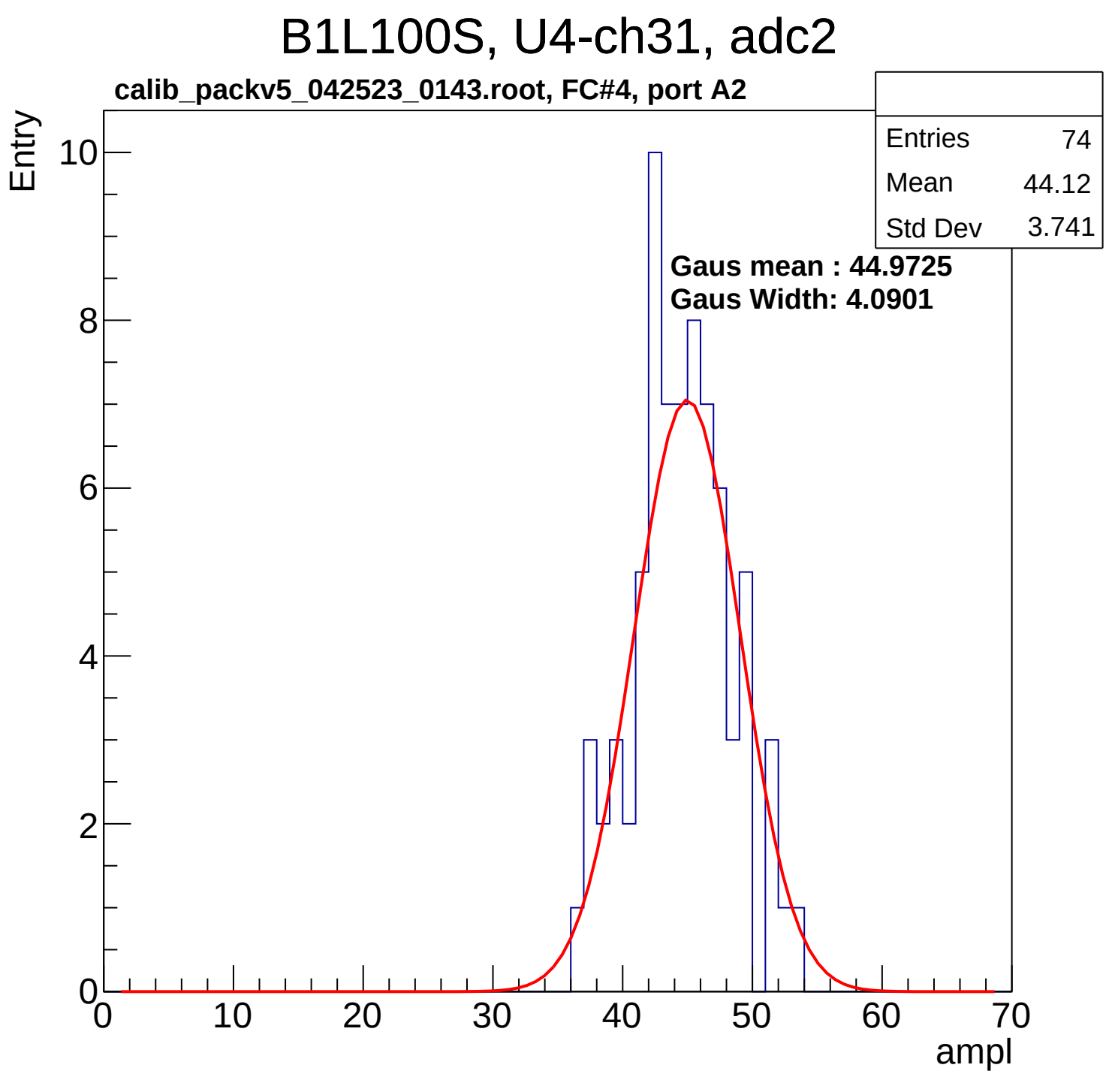

B1L100S, U4-ch30, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 26
Mean 58.46
Std Dev 11.83
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

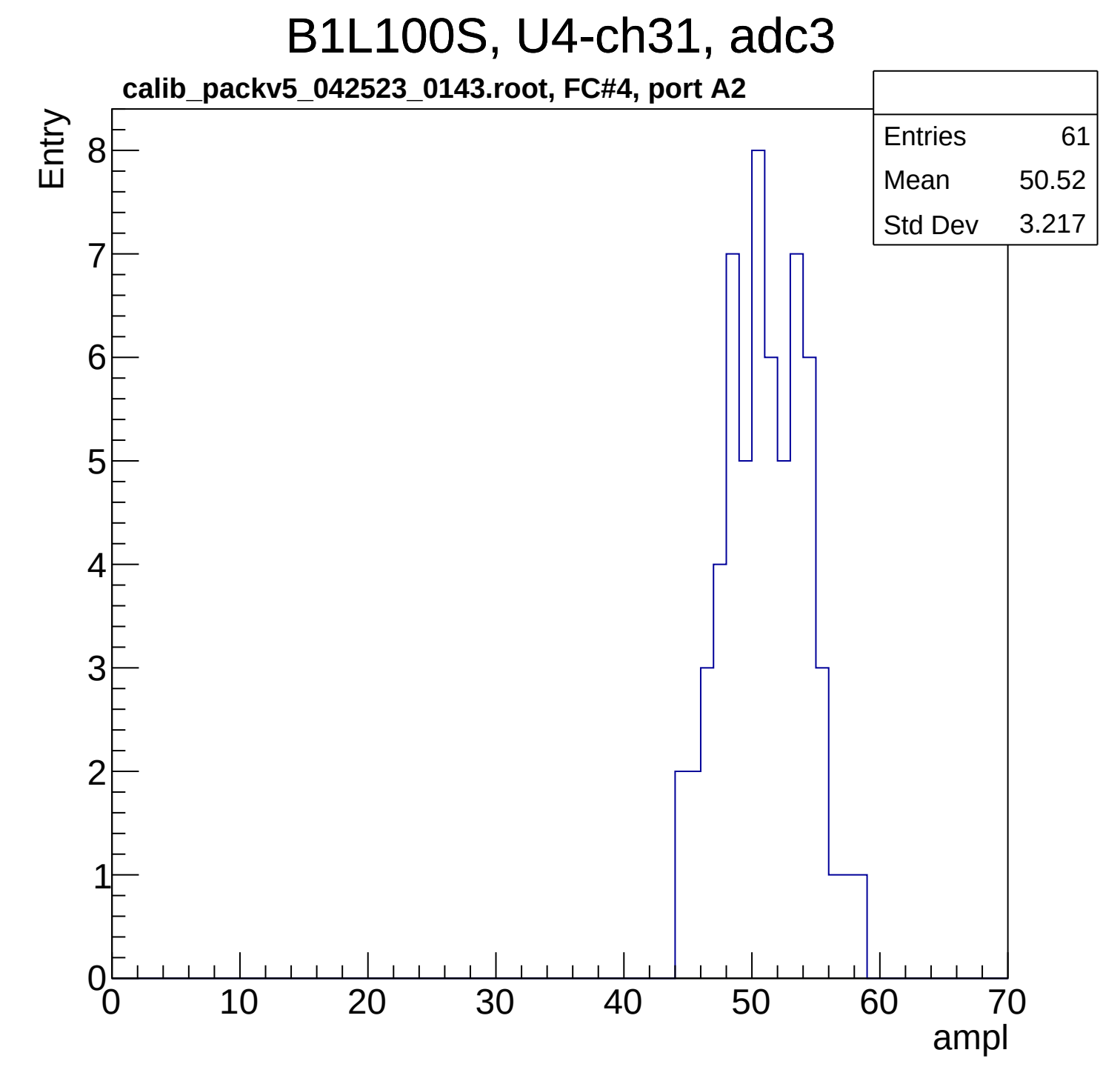

B1L100S, U4-ch30, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 62.5
Std Dev 0.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

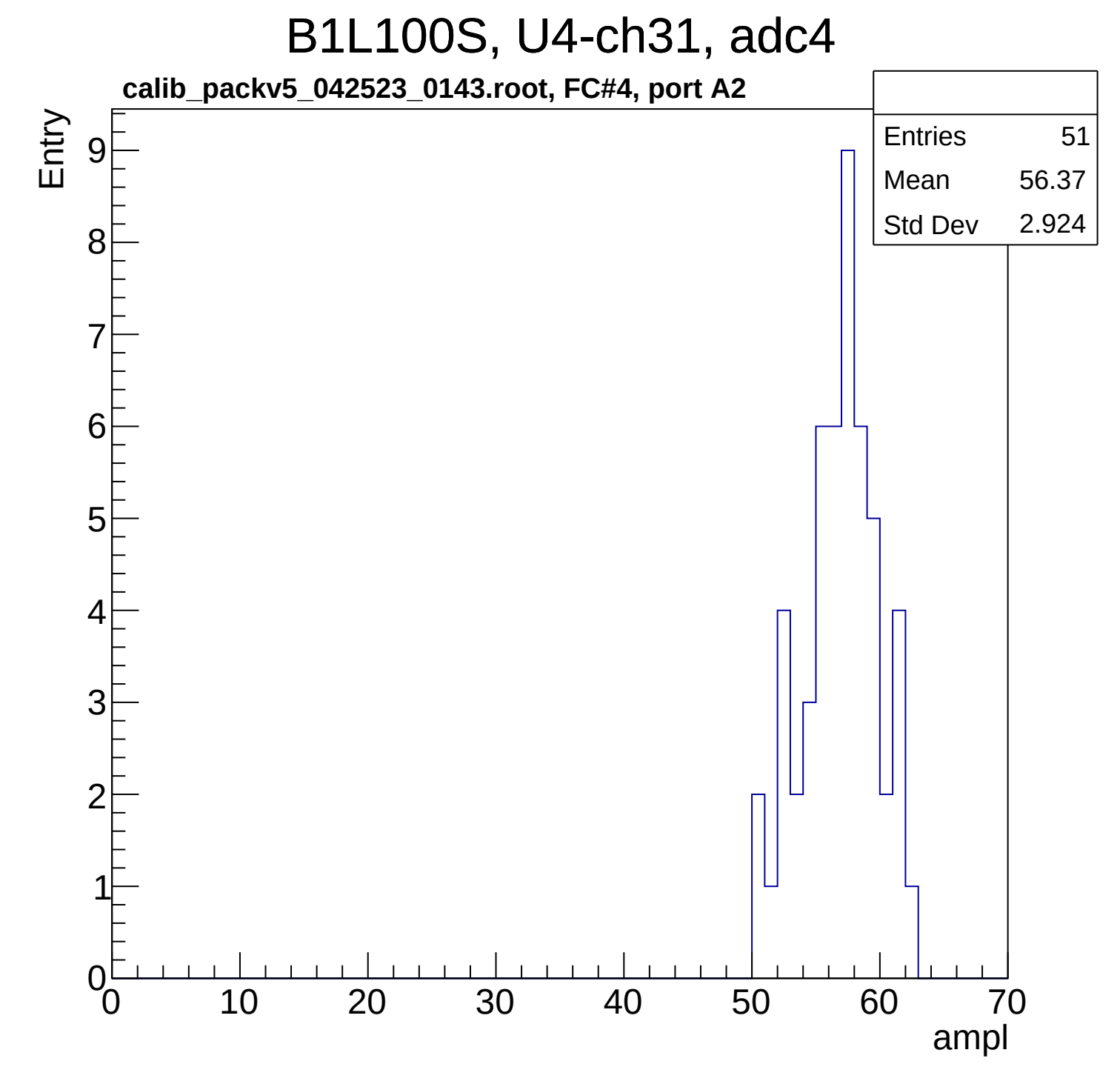

B1L100S, U4-ch30, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

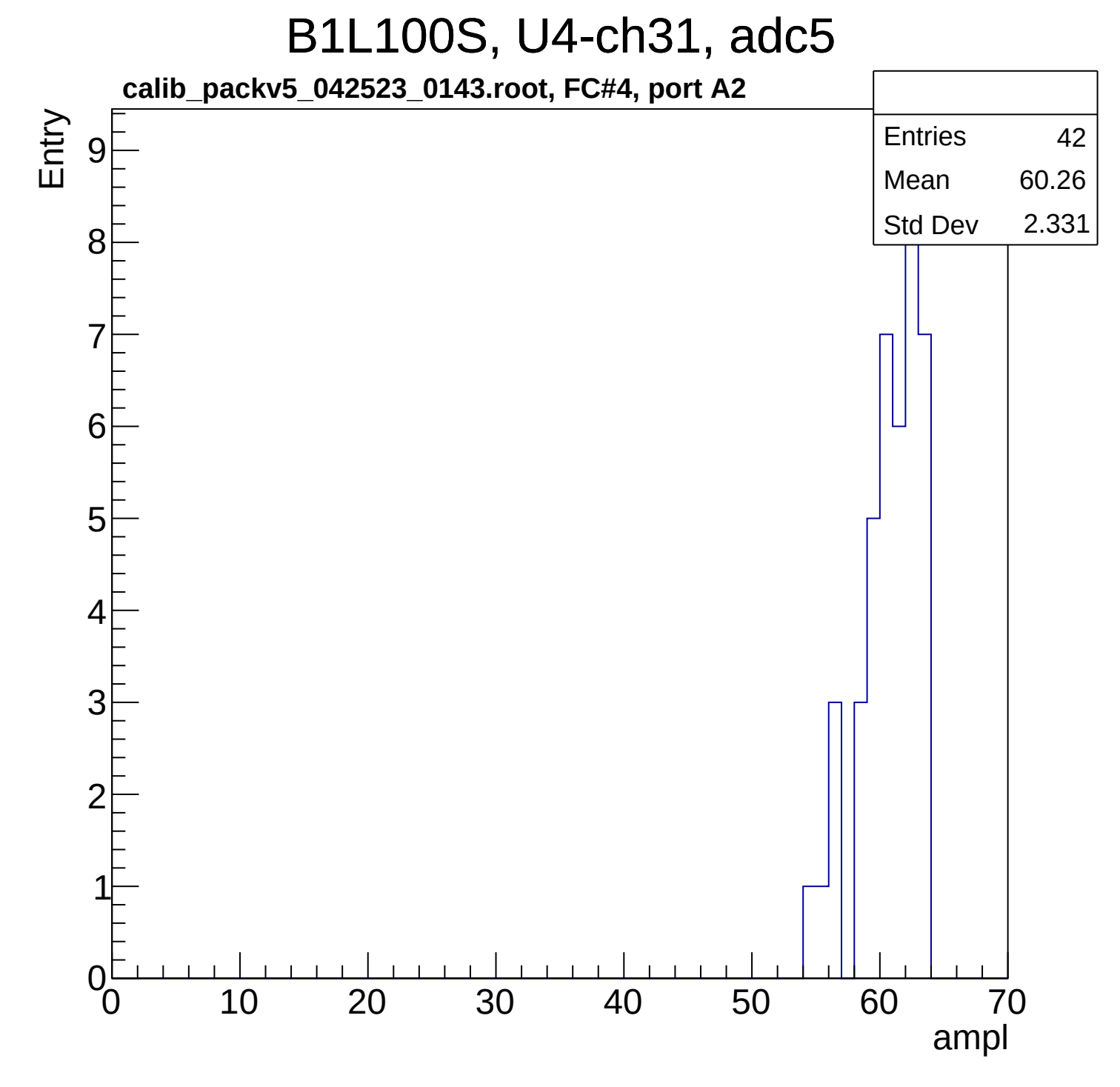

B1L100S, U4-ch31, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 29.48
Std Dev 3.54
Gaus mean : 29.3307
Gaus Width: 3.8592
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

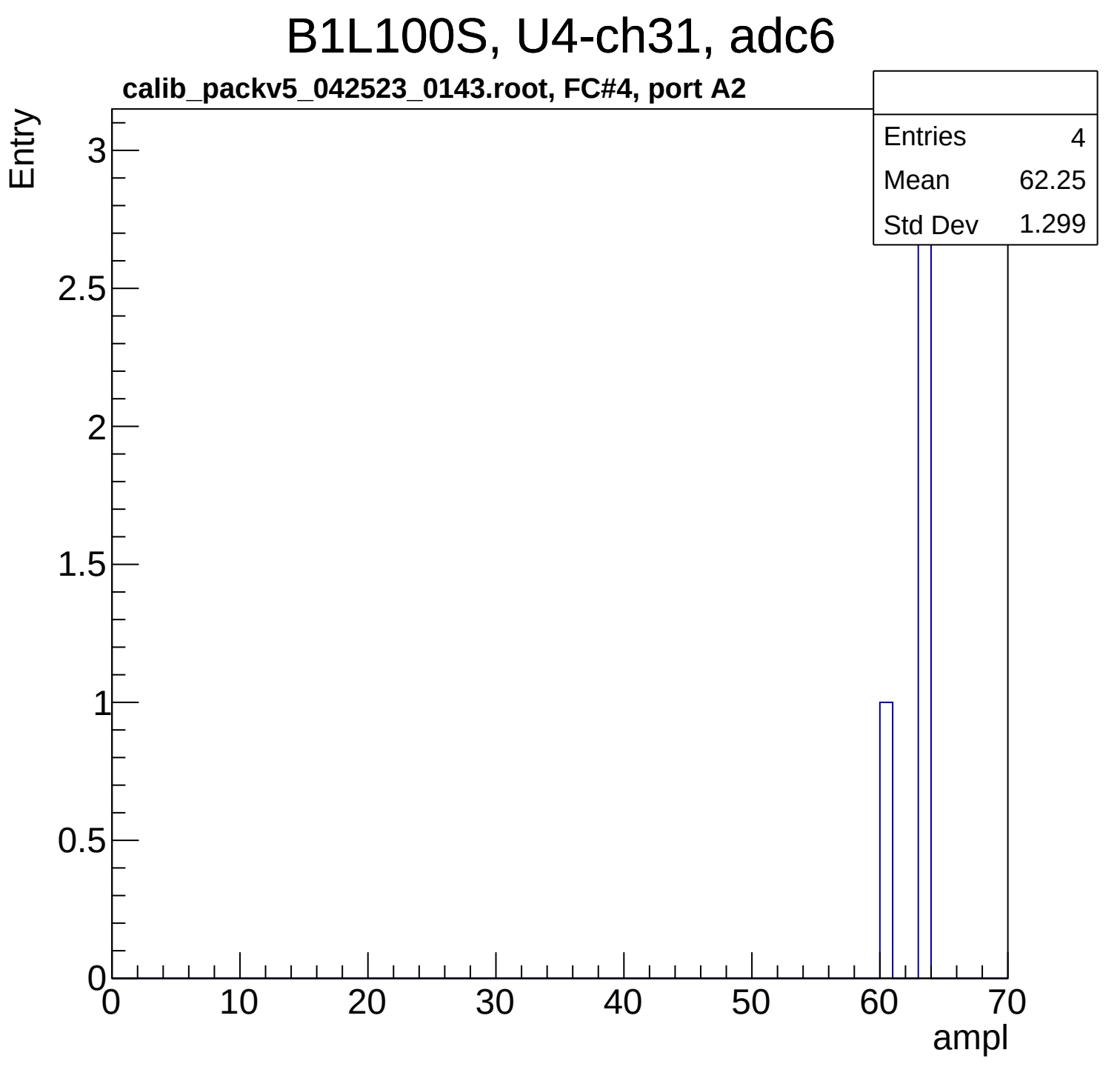

B1L100S, U4-ch31, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 36.5
Std Dev 3.667
Gaus mean : 37.8078
Gaus Width: 3.9134
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

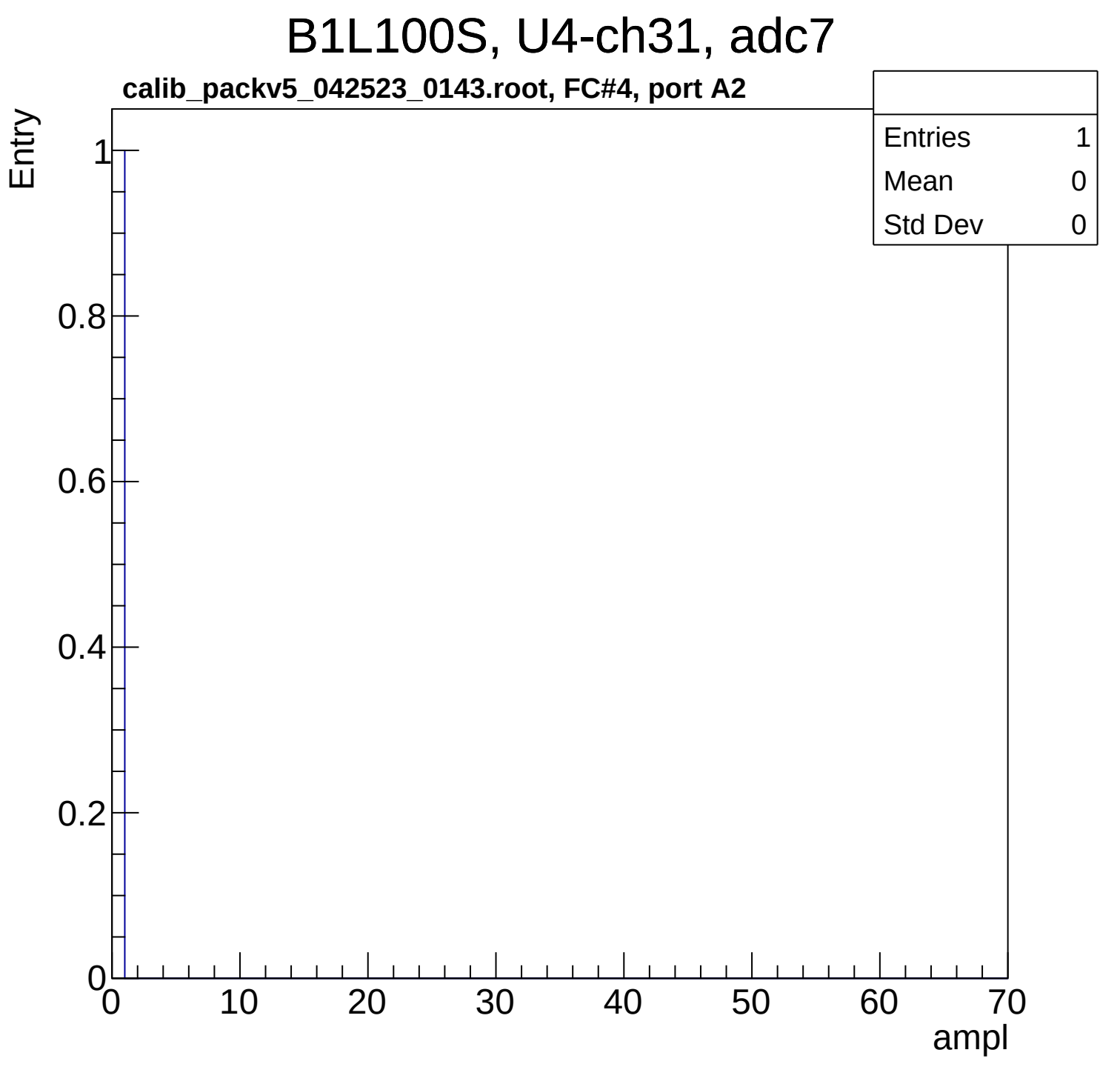

B1L100S, U4-ch31, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 44.12
Std Dev 3.741
Gaus mean : 44.9725
Gaus Width: 4.0901
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

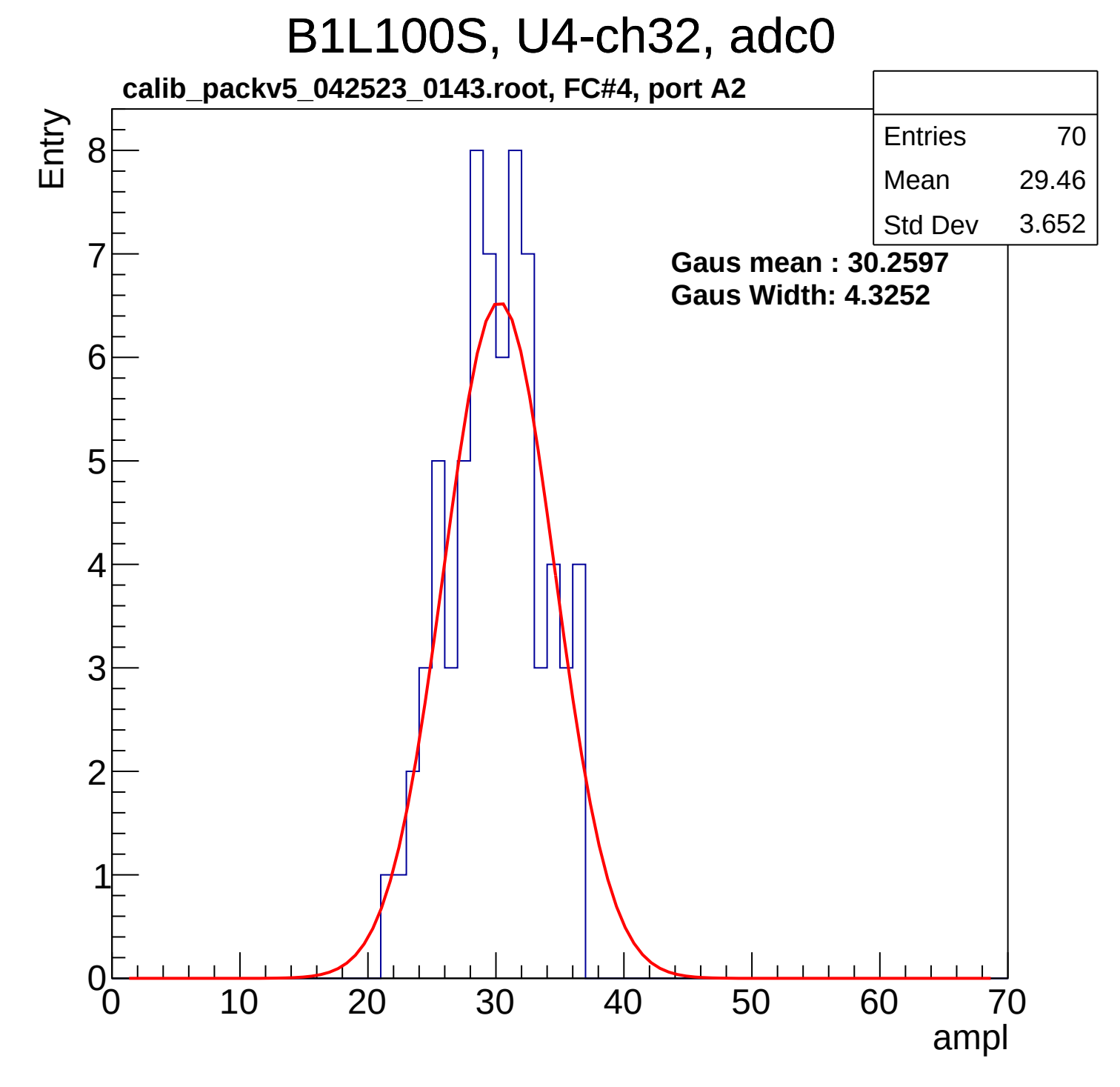

B1L100S, U4-ch31, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 50.52
Std Dev 3.217
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

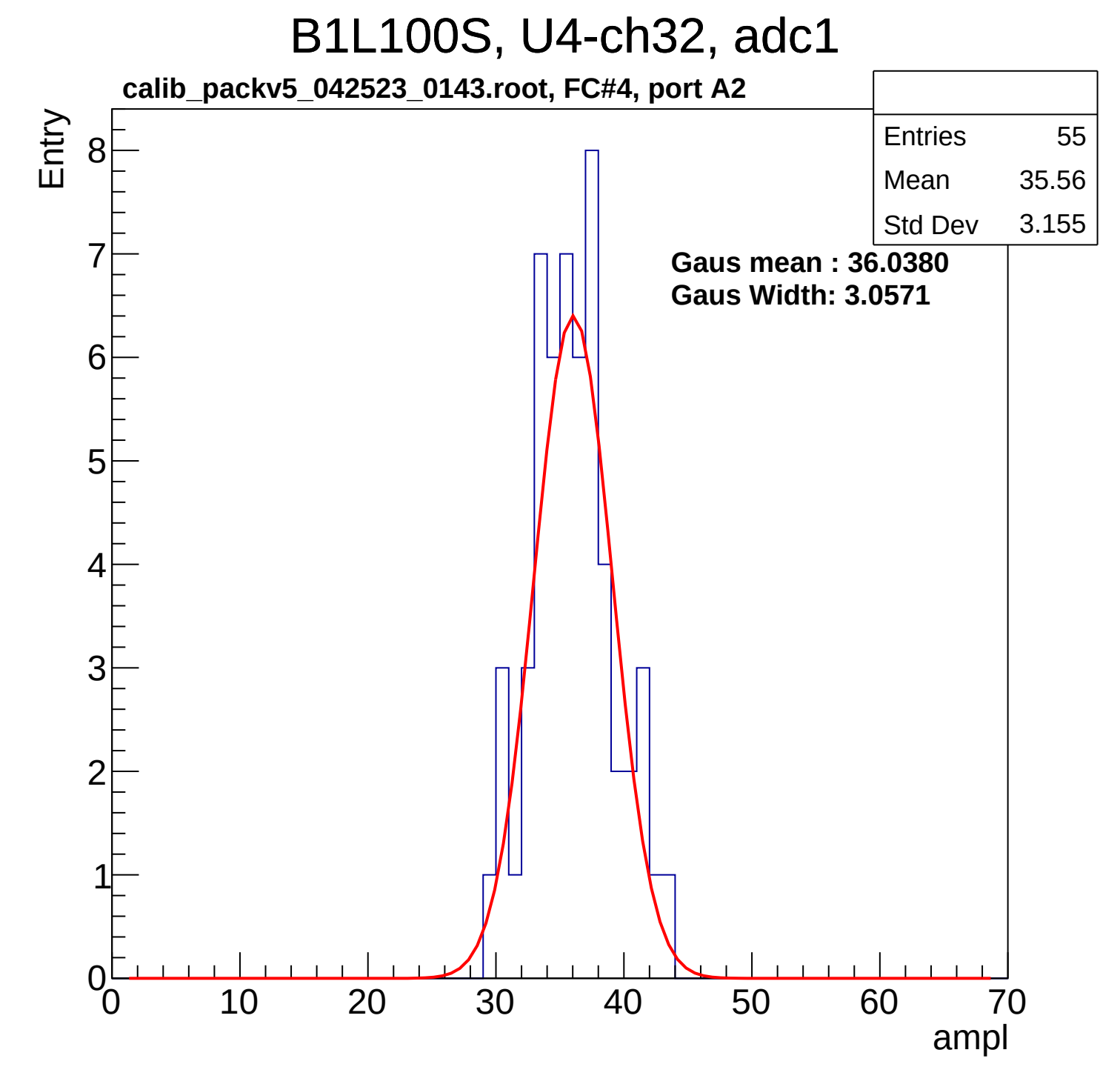

B1L100S, U4-ch31, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 56.37
Std Dev 2.924
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

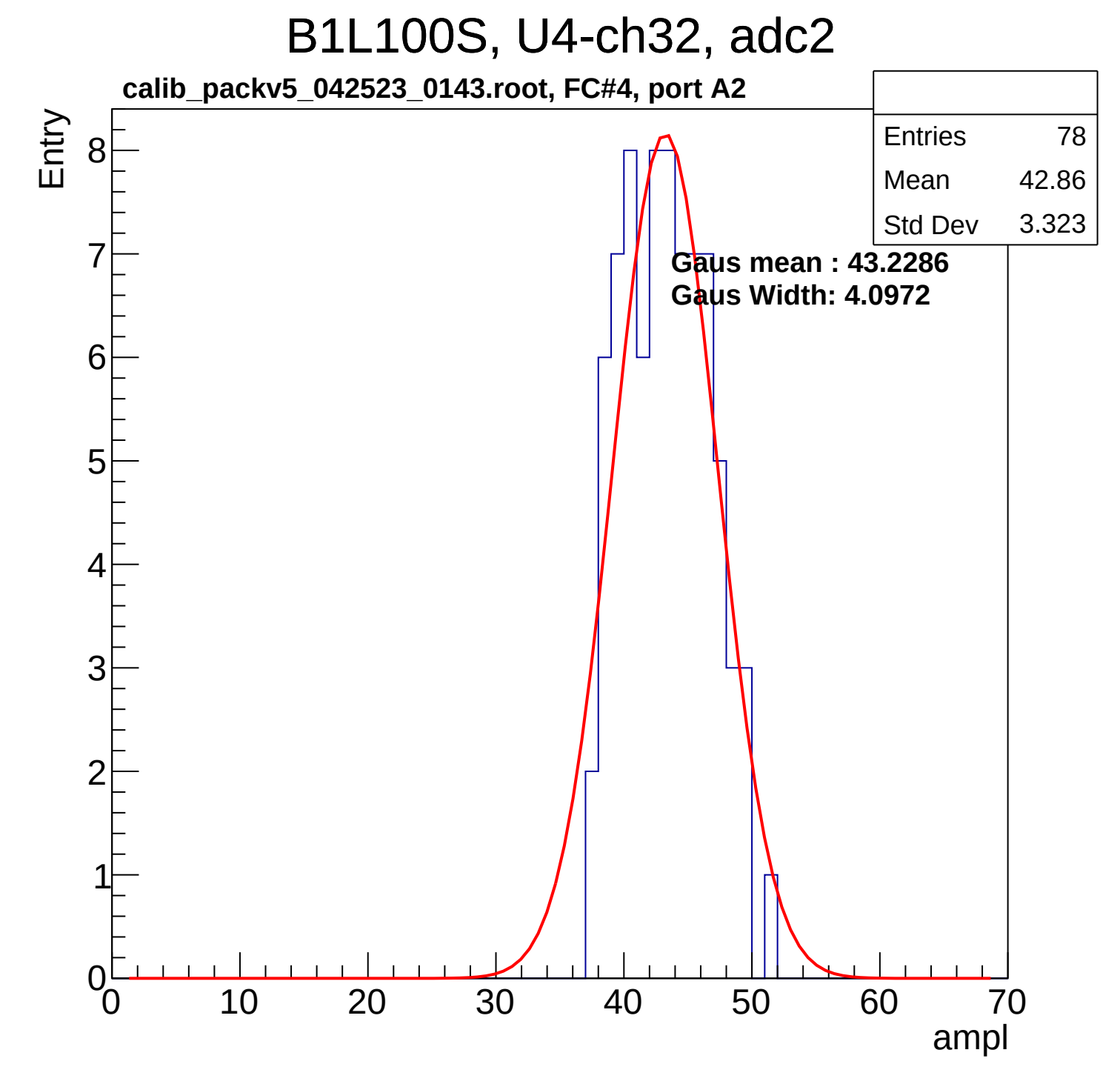

B1L100S, U4-ch31, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 42
Mean 60.26
Std Dev 2.331
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

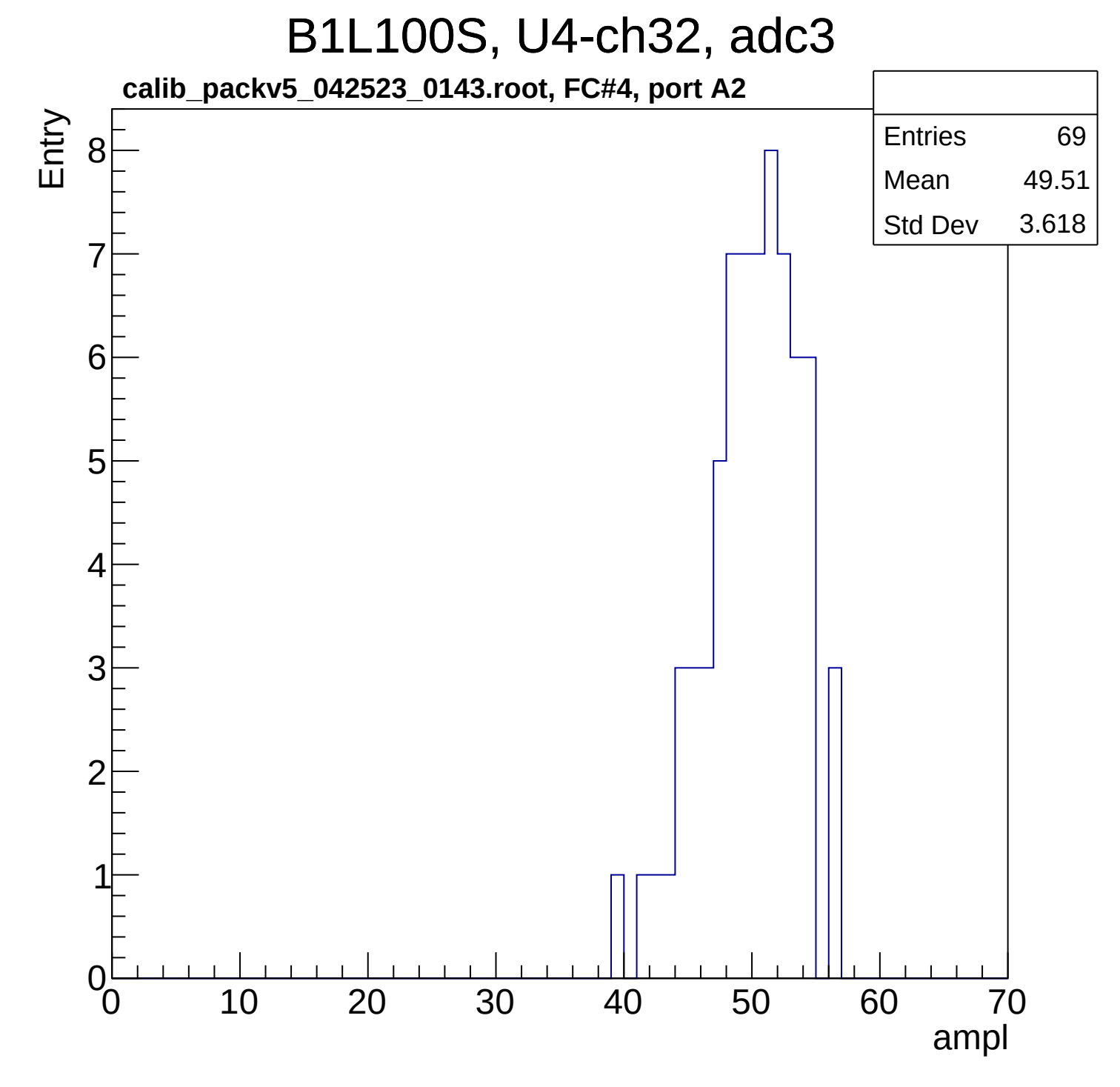

B1L100S, U4-ch31, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 62.25
Std Dev 1.299
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

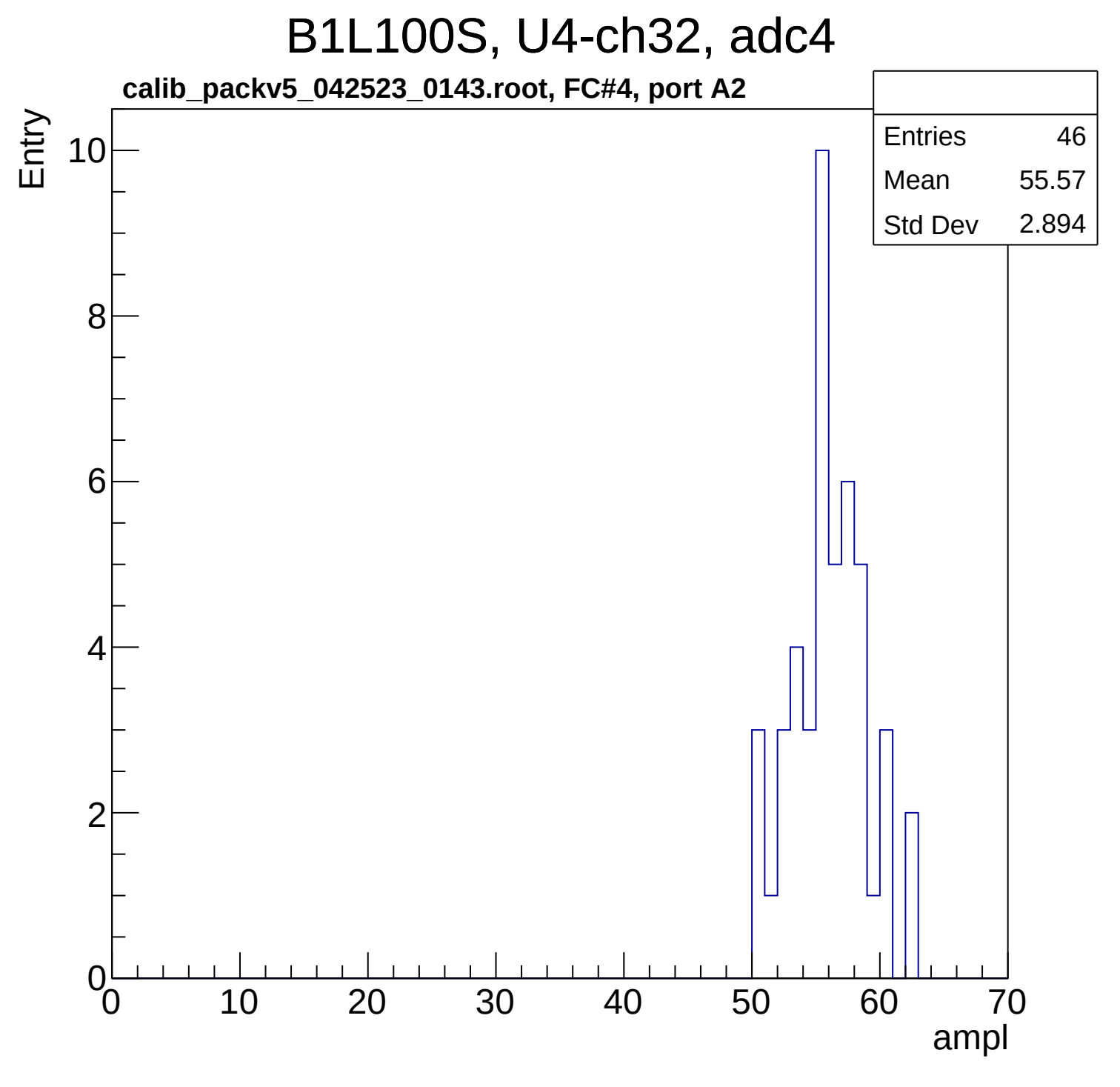

B1L100S, U4-ch31, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

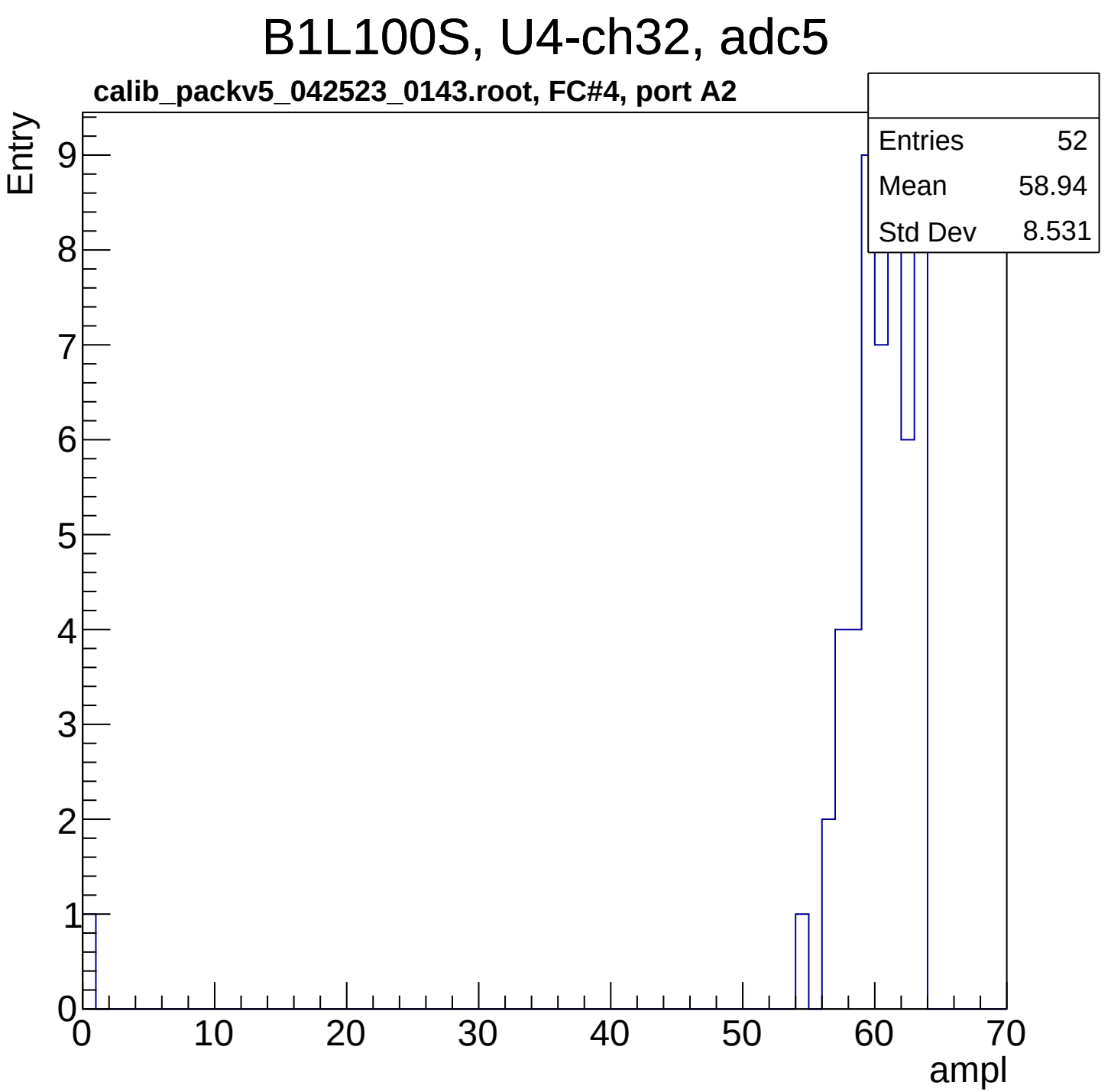

B1L100S, U4-ch32, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 29.46
Std Dev 3.652
Gaus mean : 30.2597
Gaus Width: 4.3252
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

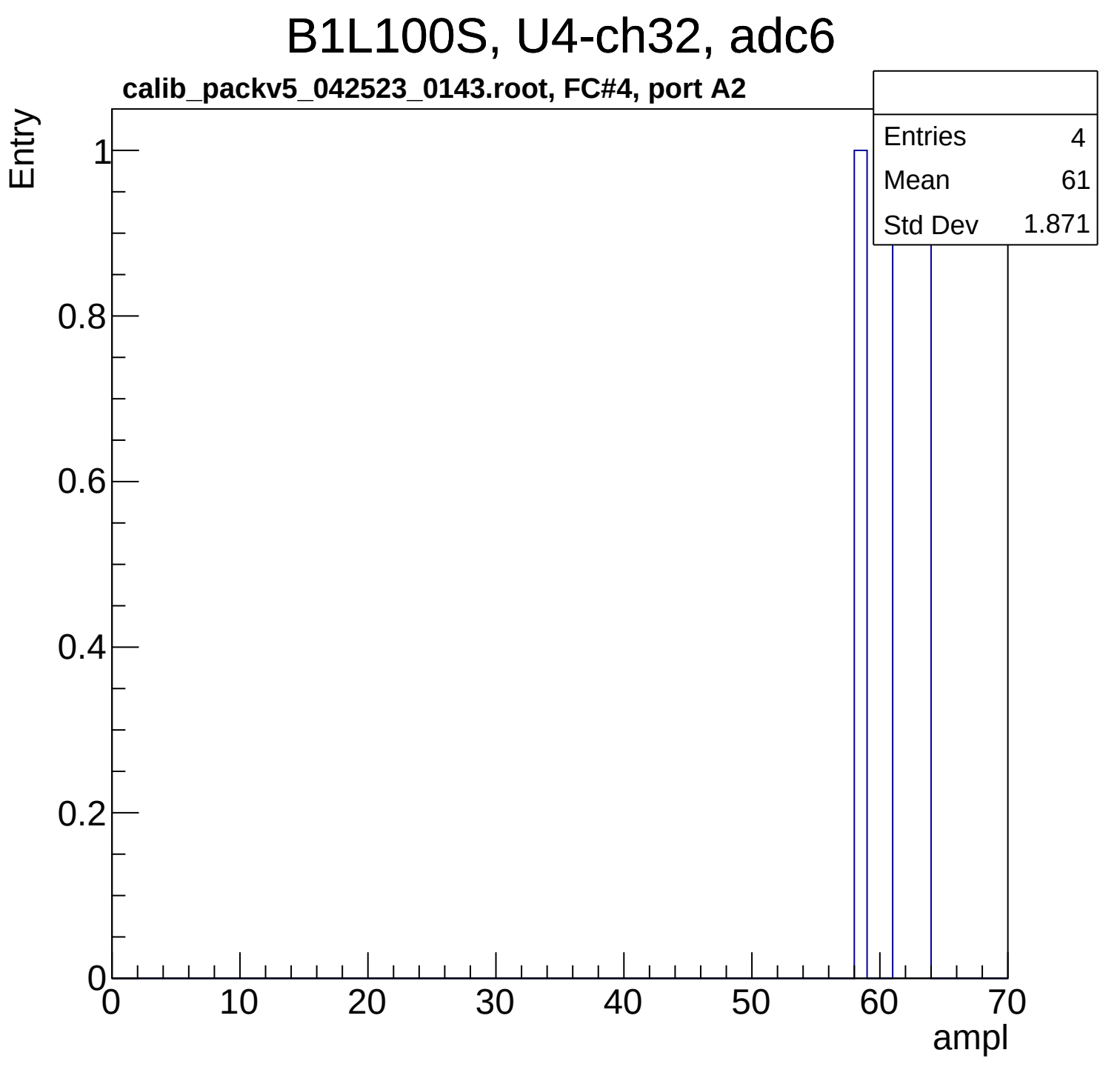

B1L100S, U4-ch32, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 35.56
Std Dev 3.155
Gaus mean : 36.0380
Gaus Width: 3.0571
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

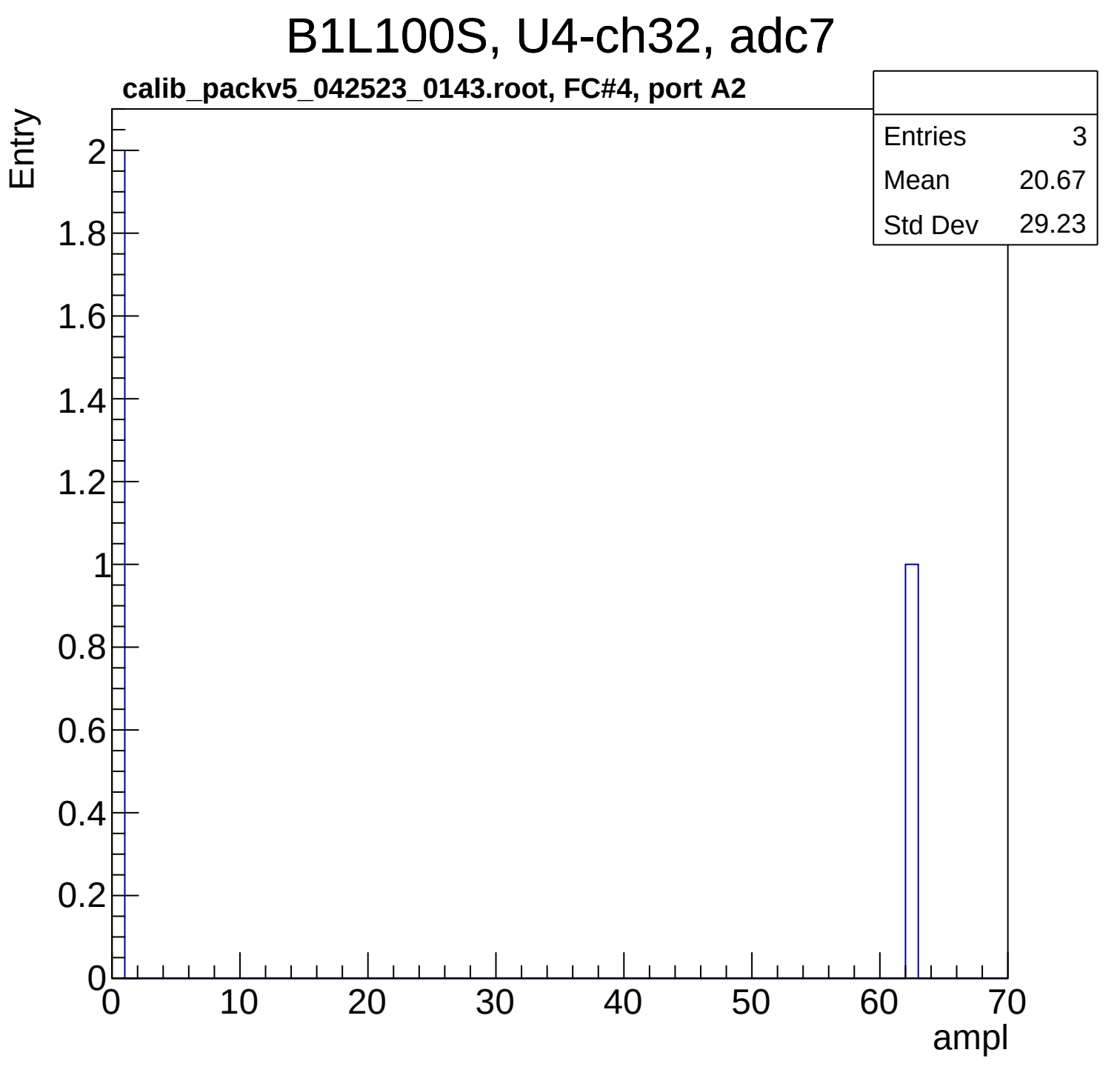

B1L100S, U4-ch32, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 42.86
Std Dev 3.323
Gaus mean : 43.2286
Gaus Width: 4.0972
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

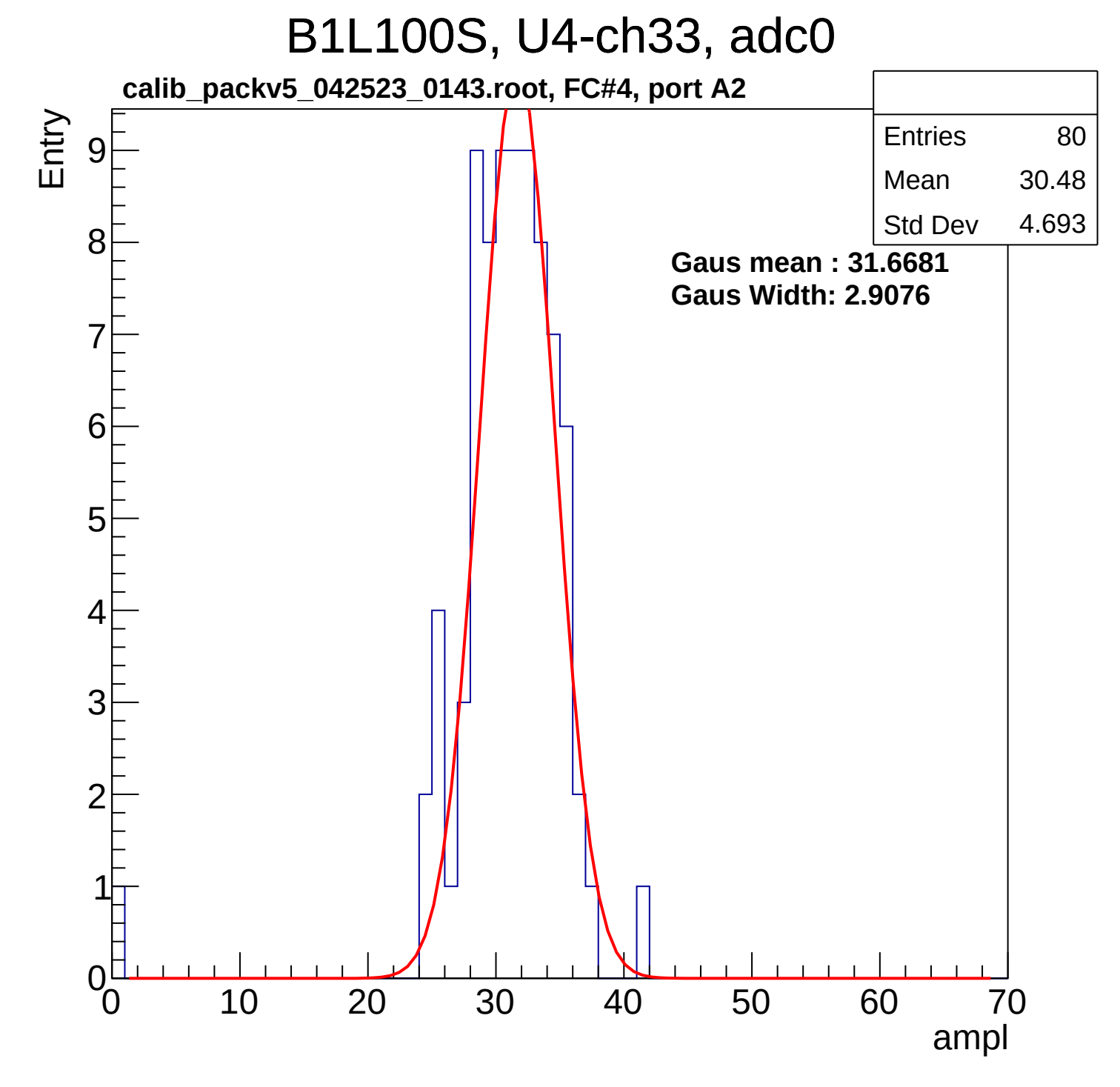

B1L100S, U4-ch32, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 49.51
Std Dev 3.618
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

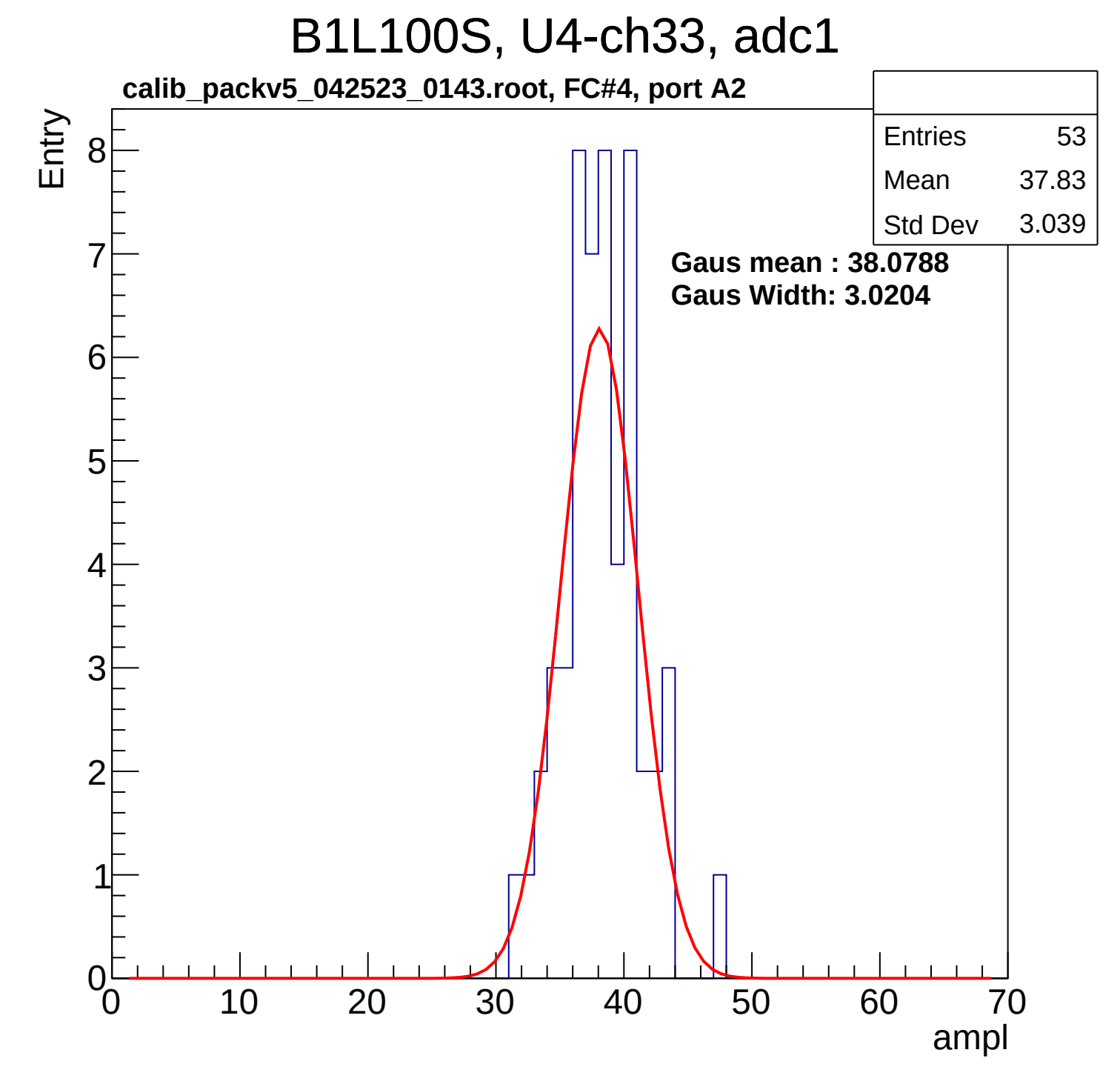

B1L100S, U4-ch32, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 55.57
Std Dev 2.894
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

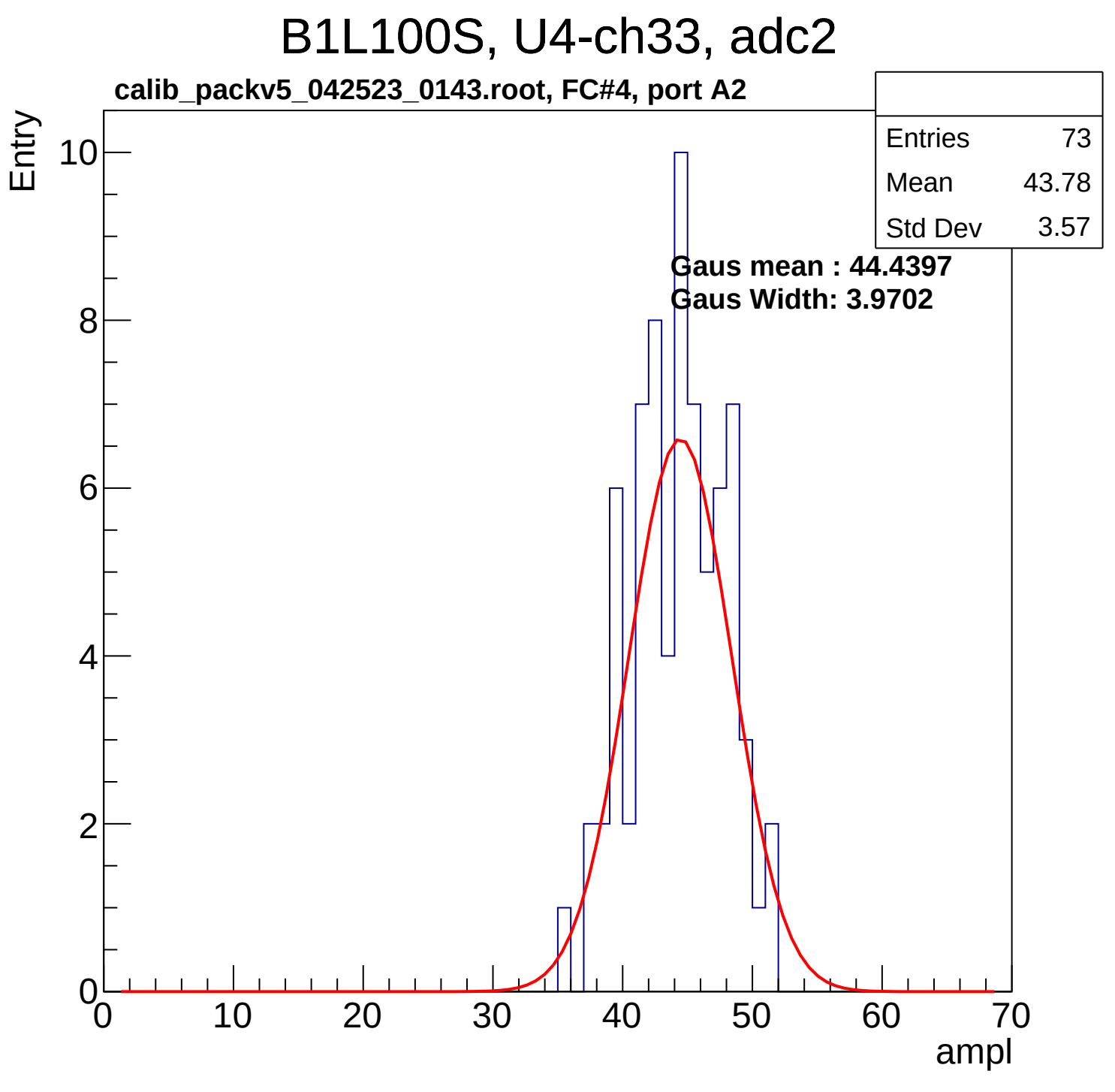

B1L100S, U4-ch32, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 58.94
Std Dev 8.531
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

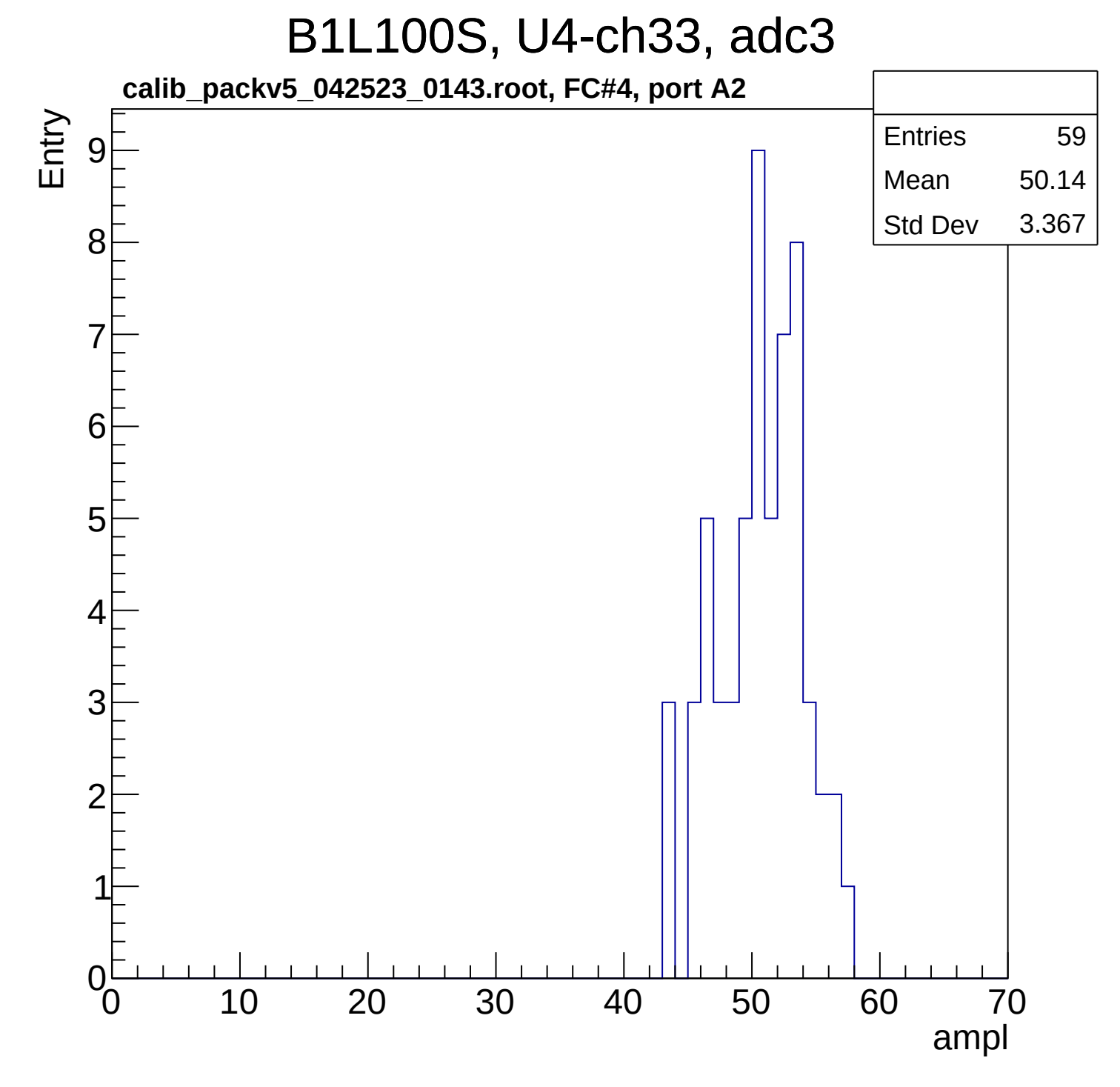

B1L100S, U4-ch32, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 61
Std Dev 1.871
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

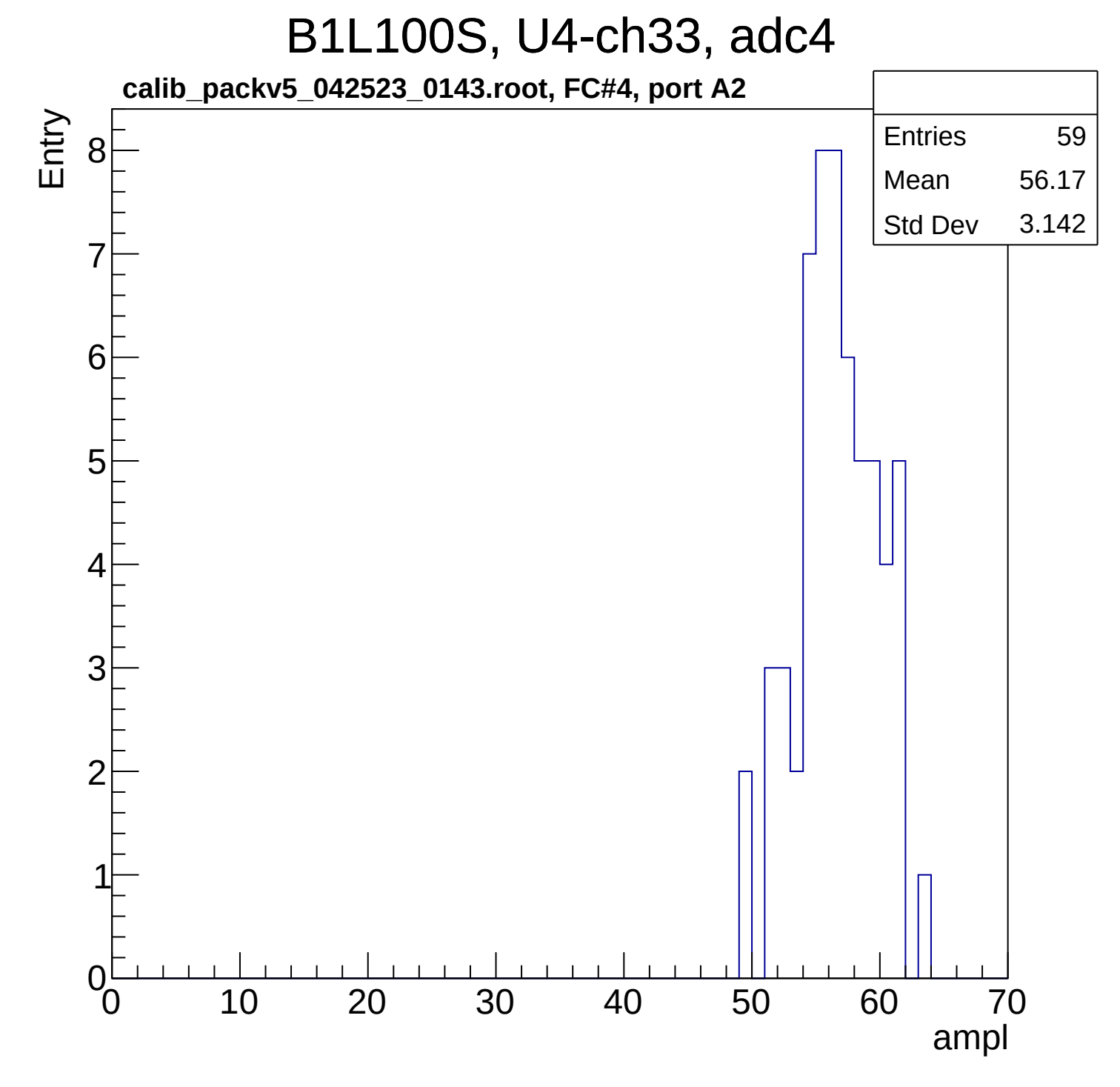

B1L100S, U4-ch32, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 20.67
Std Dev 29.23
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

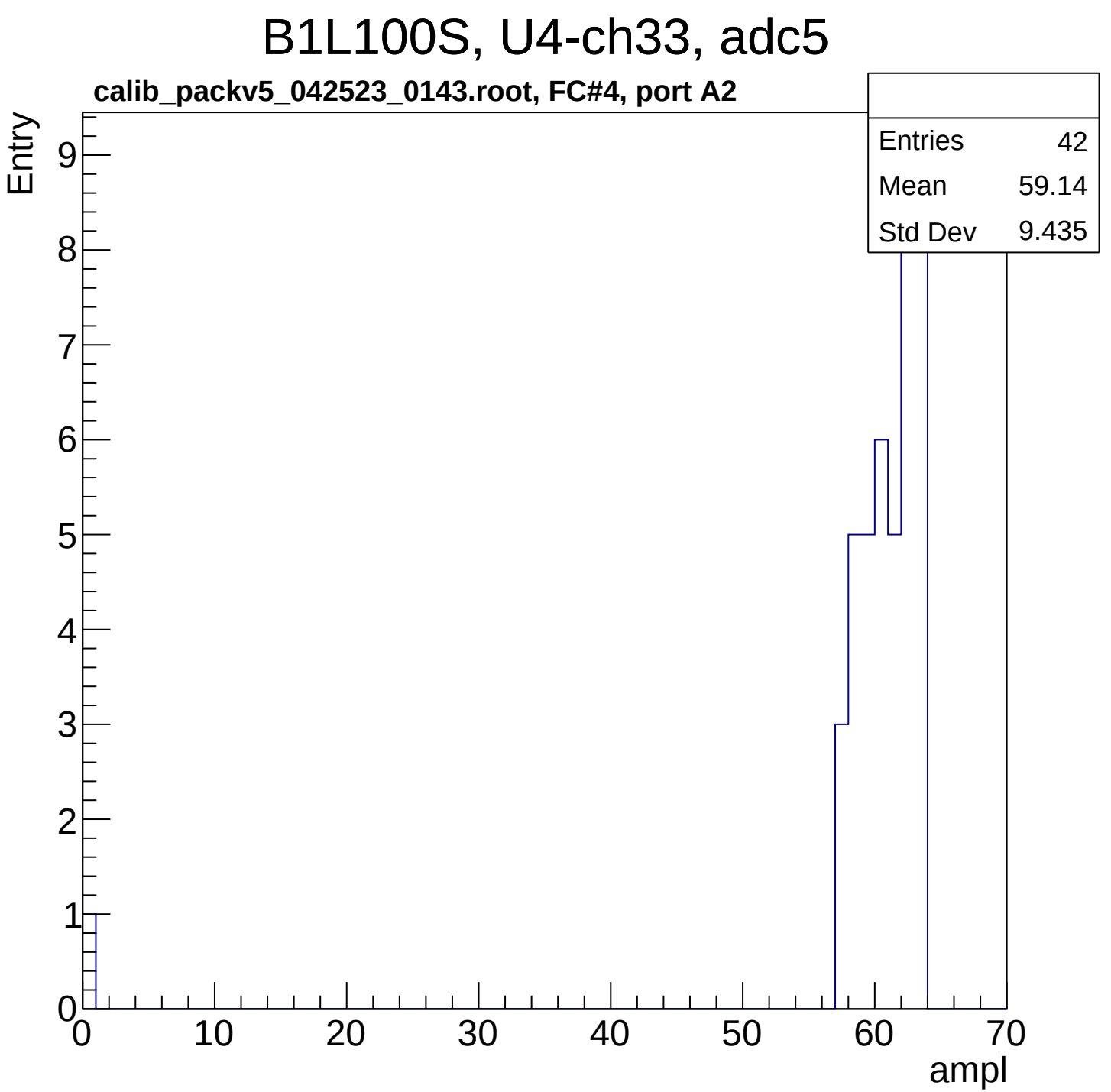

B1L100S, U4-ch33, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 30.48
Std Dev 4.693
Gaus mean : 31.6681
Gaus Width: 2.9076
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

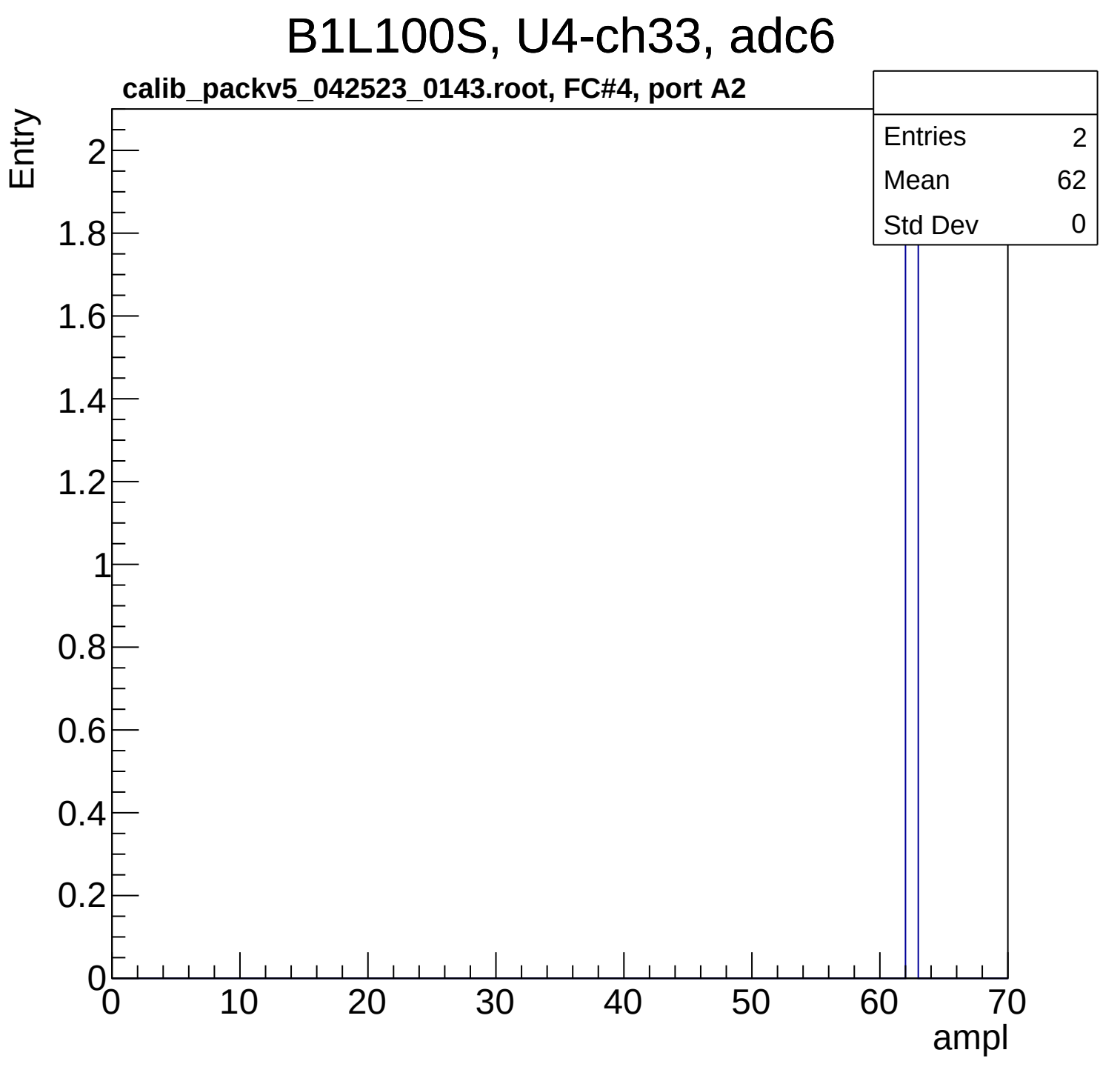

B1L100S, U4-ch33, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 37.83
Std Dev 3.039
Gaus mean : 38.0788
Gaus Width: 3.0204
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

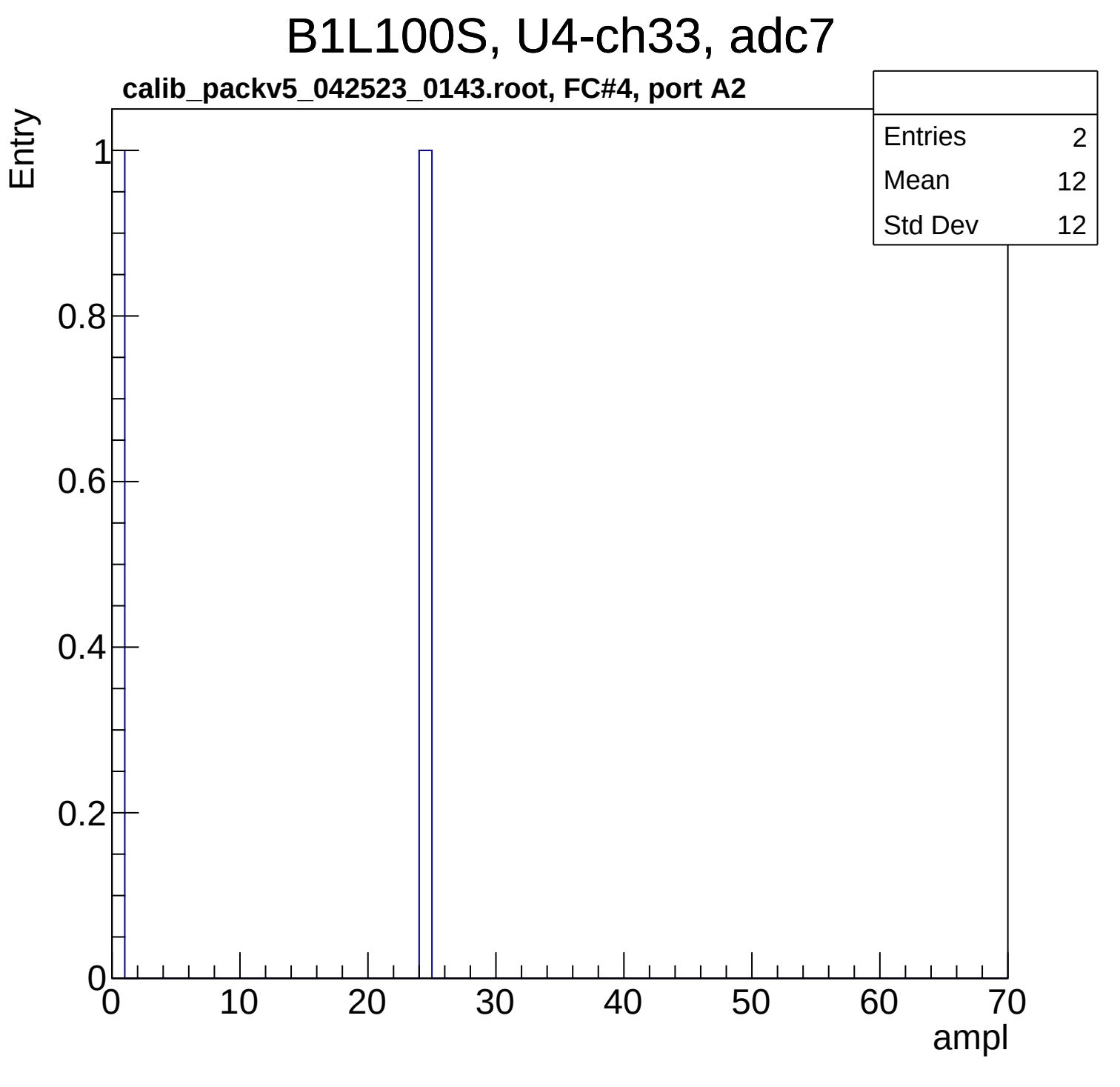

B1L100S, U4-ch33, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 43.78
Std Dev 3.57
Gaus mean : 44.4397
Gaus Width: 3.9702
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

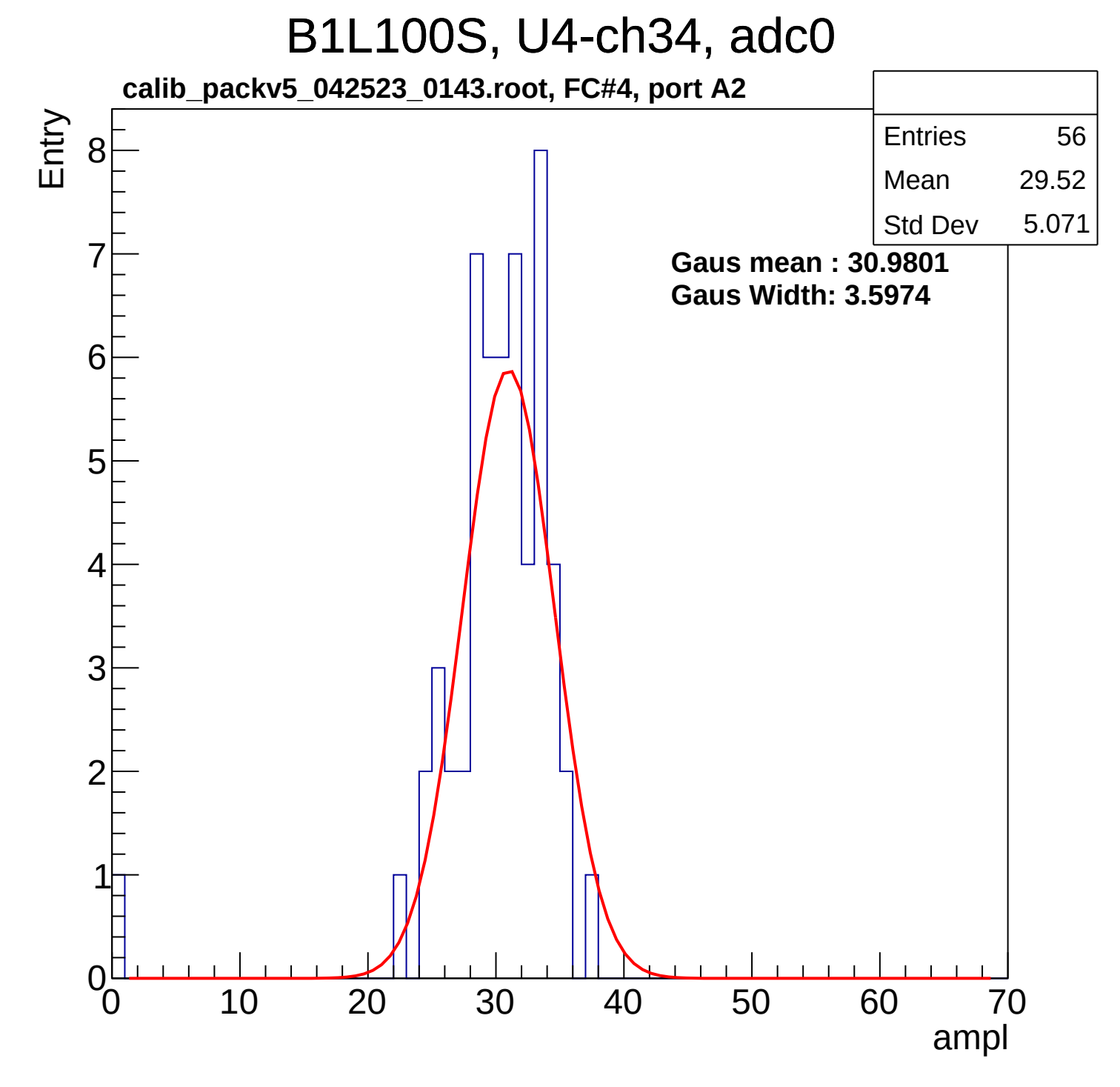

B1L100S, U4-ch33, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 50.14
Std Dev 3.367
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

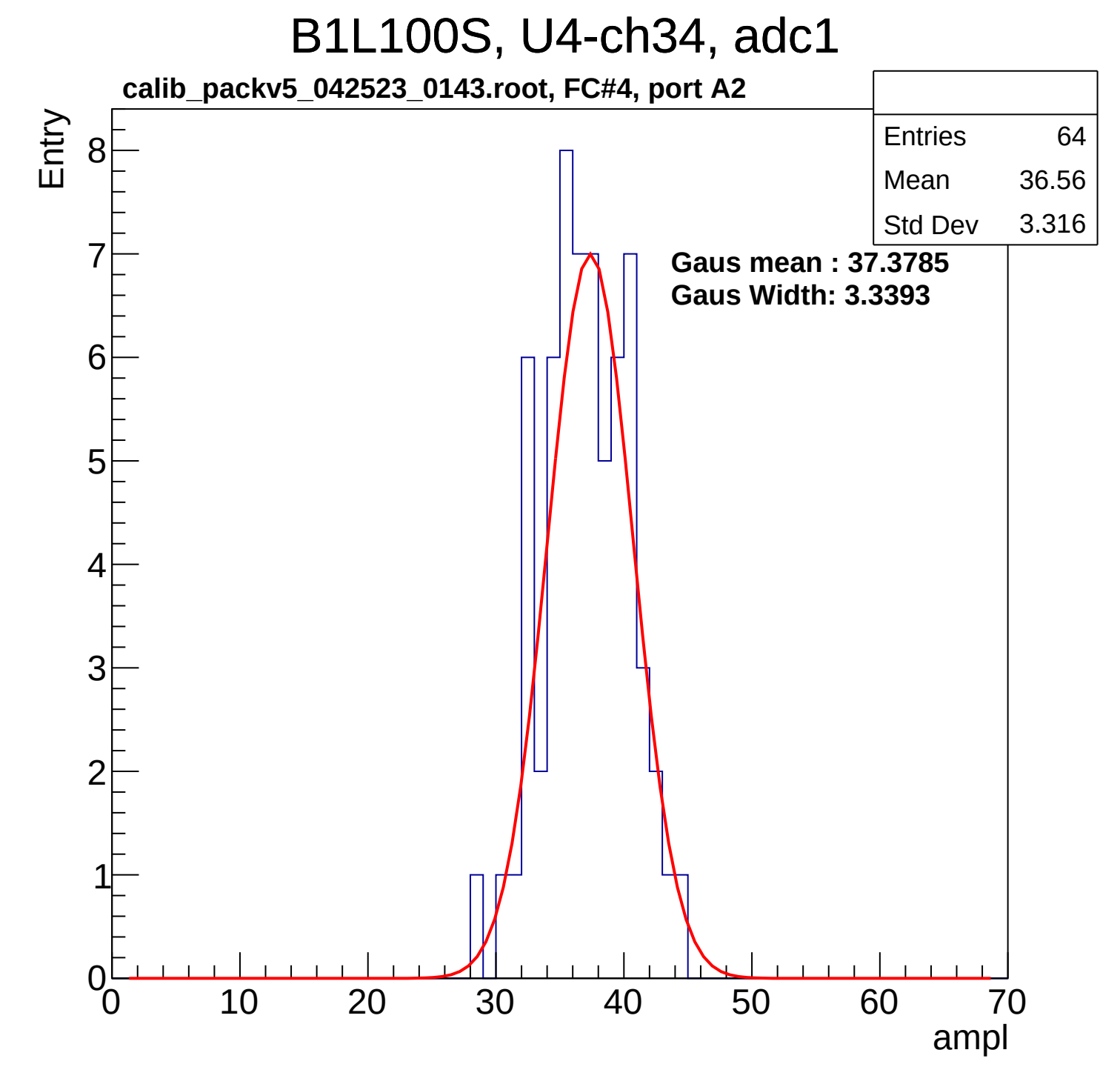

B1L100S, U4-ch33, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 56.17
Std Dev 3.142
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

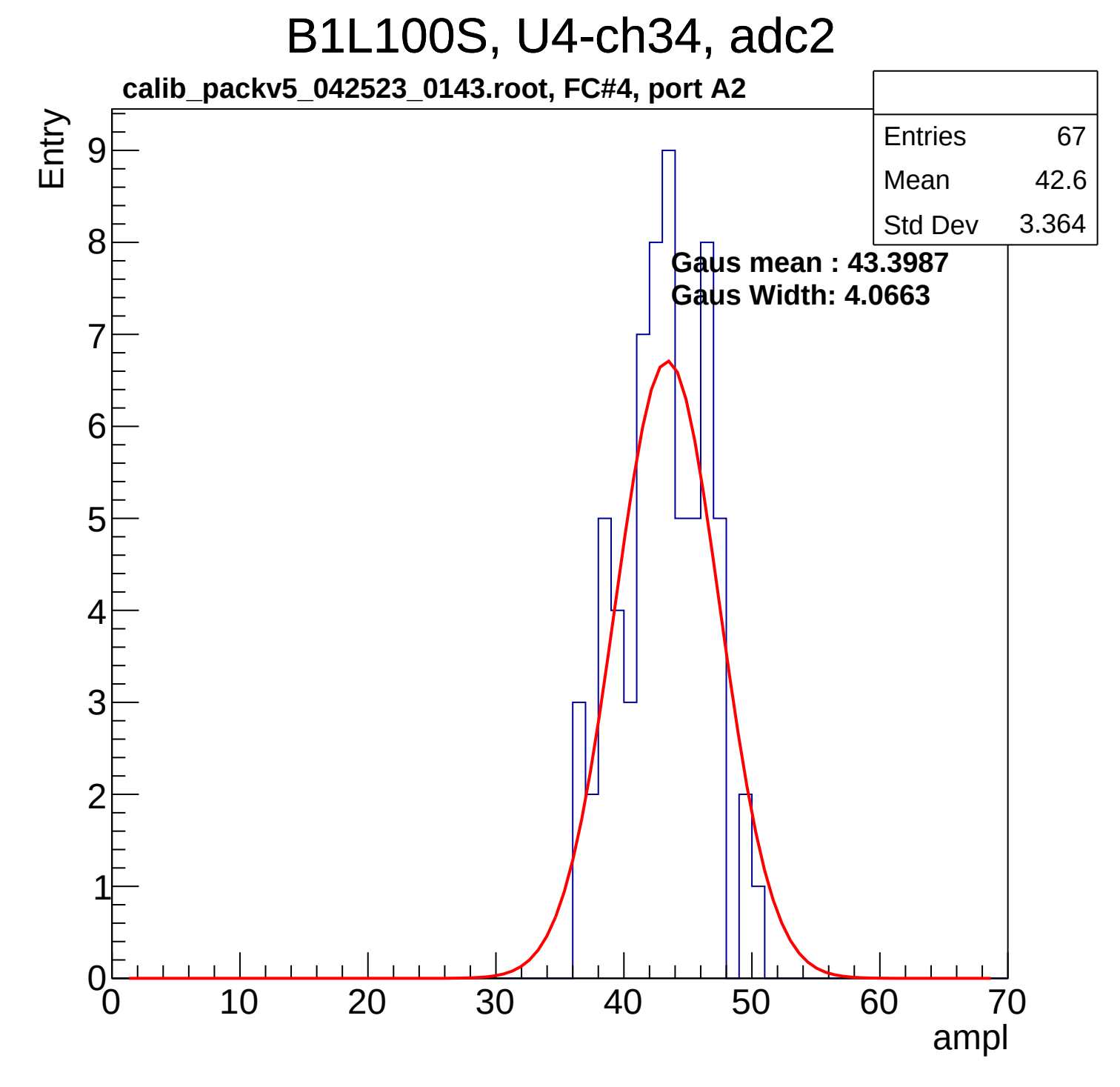

B1L100S, U4-ch33, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 42
Mean 59.14
Std Dev 9.435
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

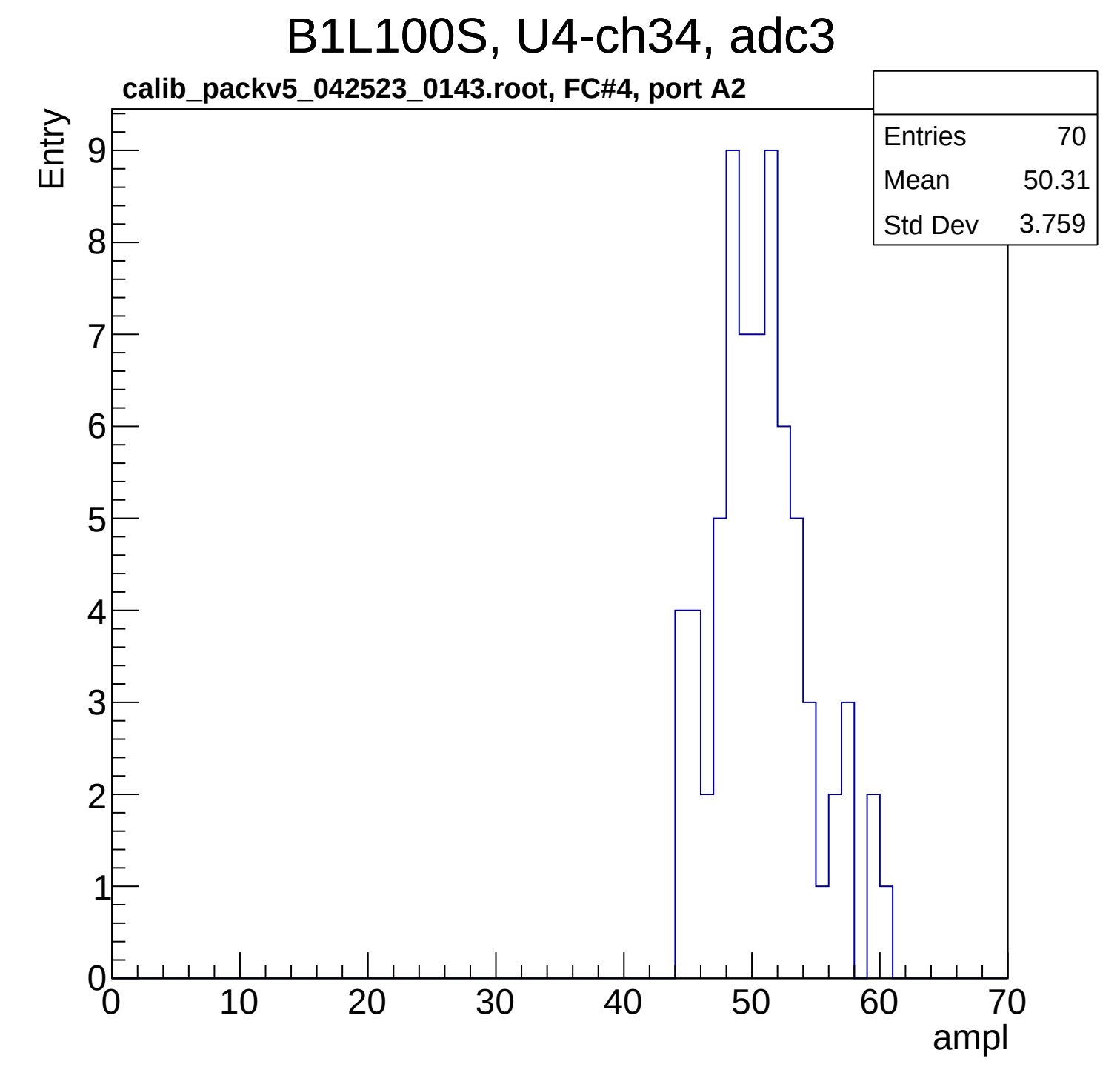

B1L100S, U4-ch33, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 62
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

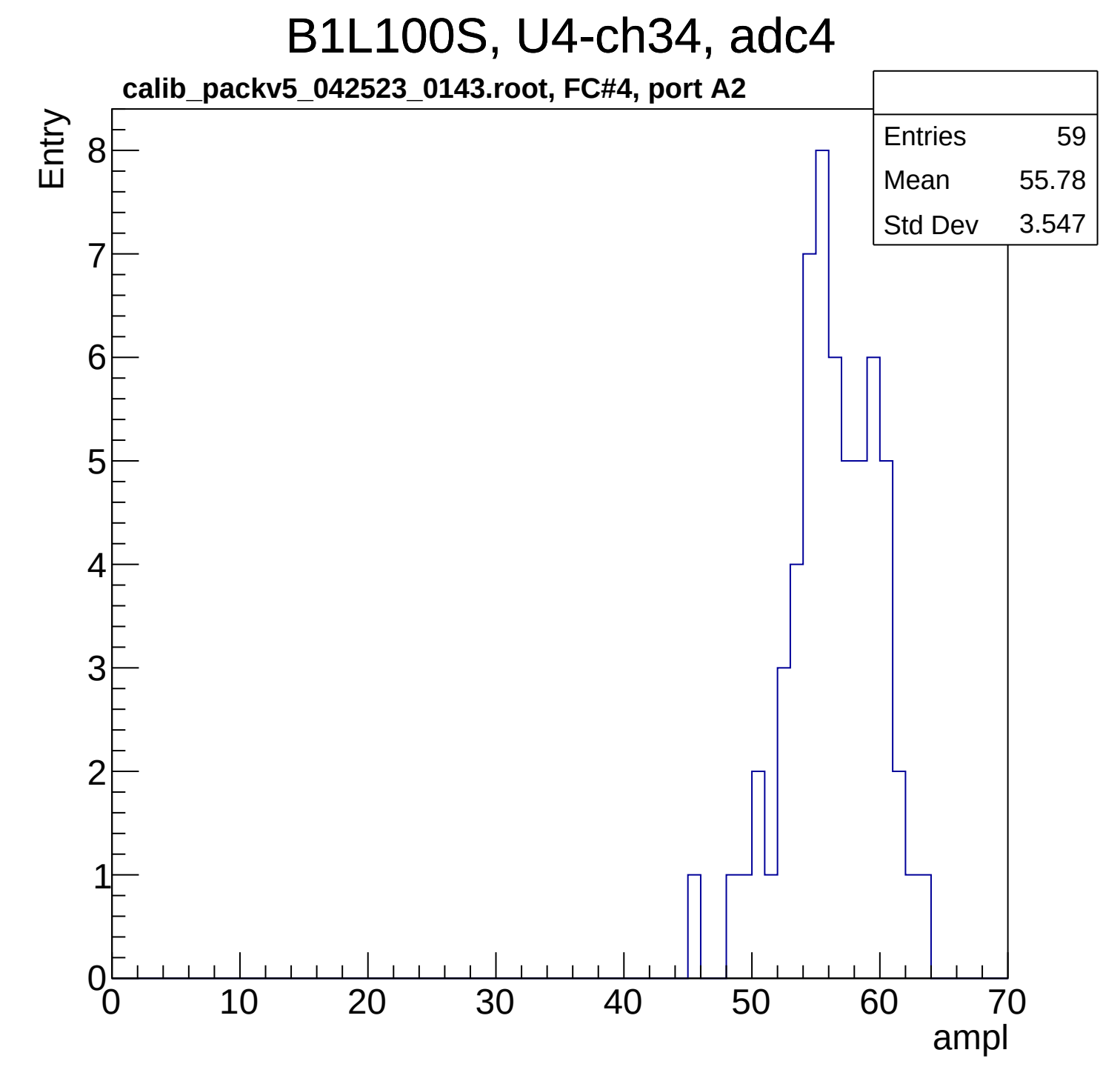

B1L100S, U4-ch33, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 12
Std Dev 12
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

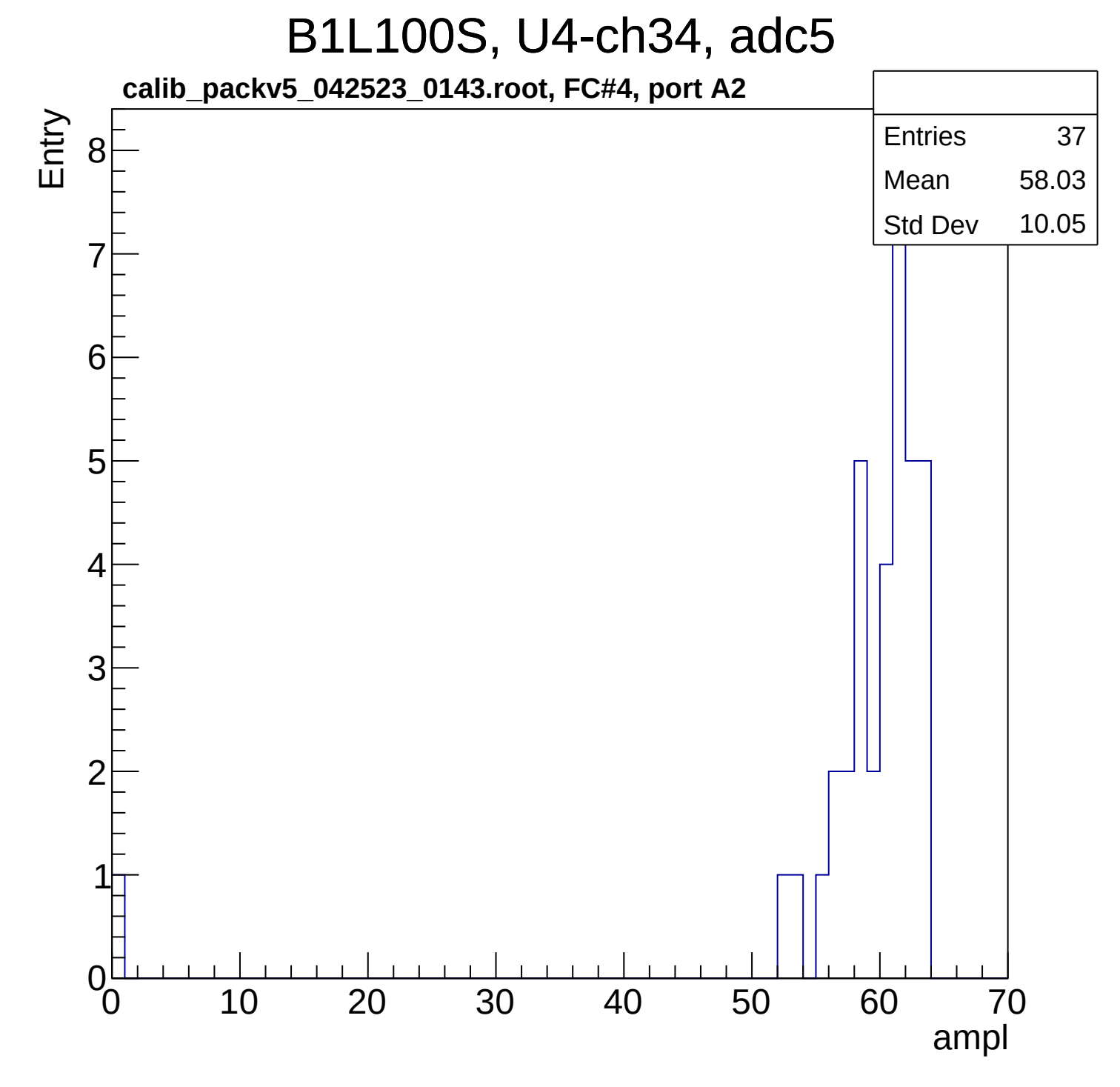

B1L100S, U4-ch34, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 29.52
Std Dev 5.071
Gaus mean : 30.9801
Gaus Width: 3.5974
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

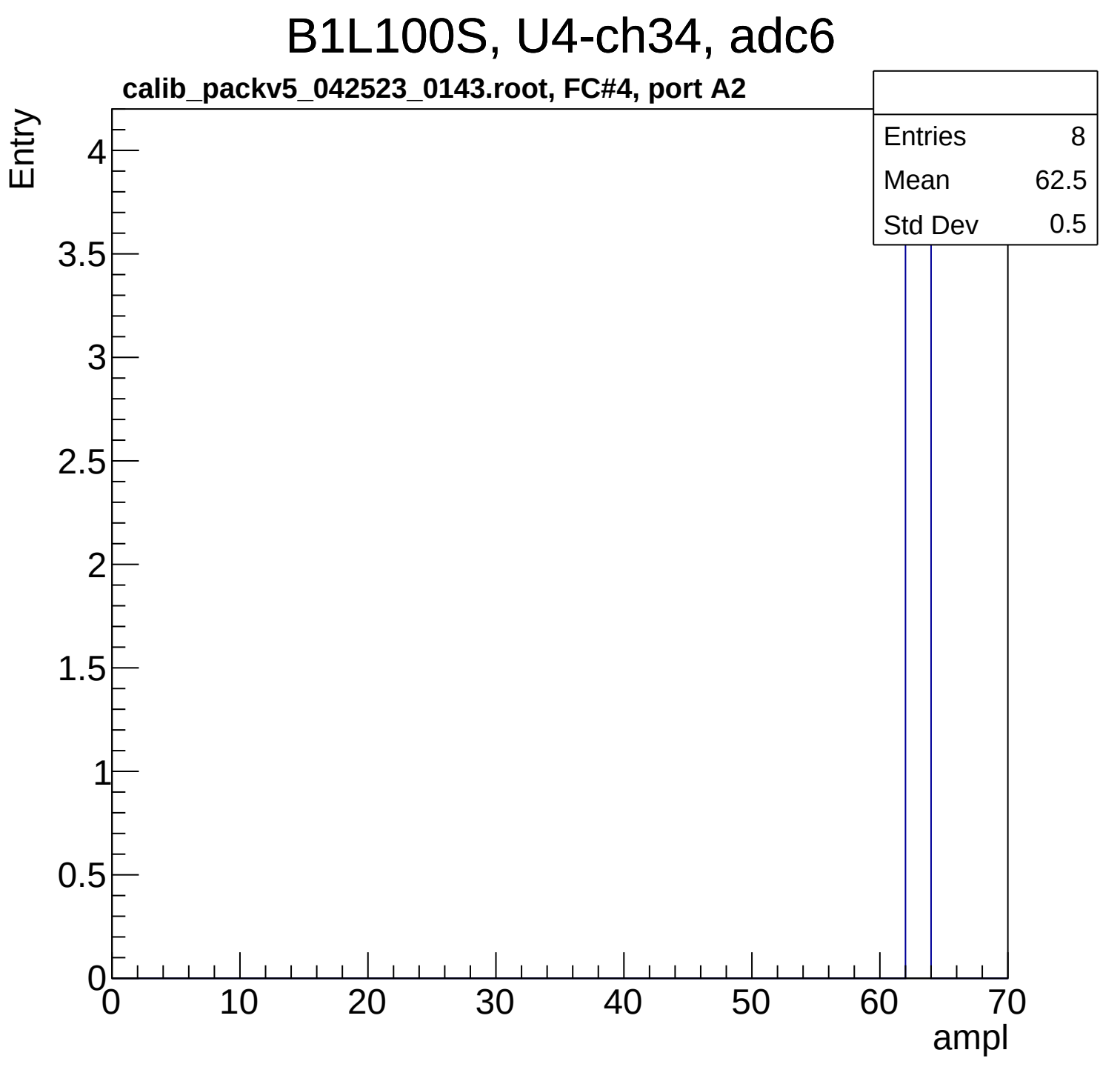

B1L100S, U4-ch34, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 36.56
Std Dev 3.316
Gaus mean : 37.3785
Gaus Width: 3.3393
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

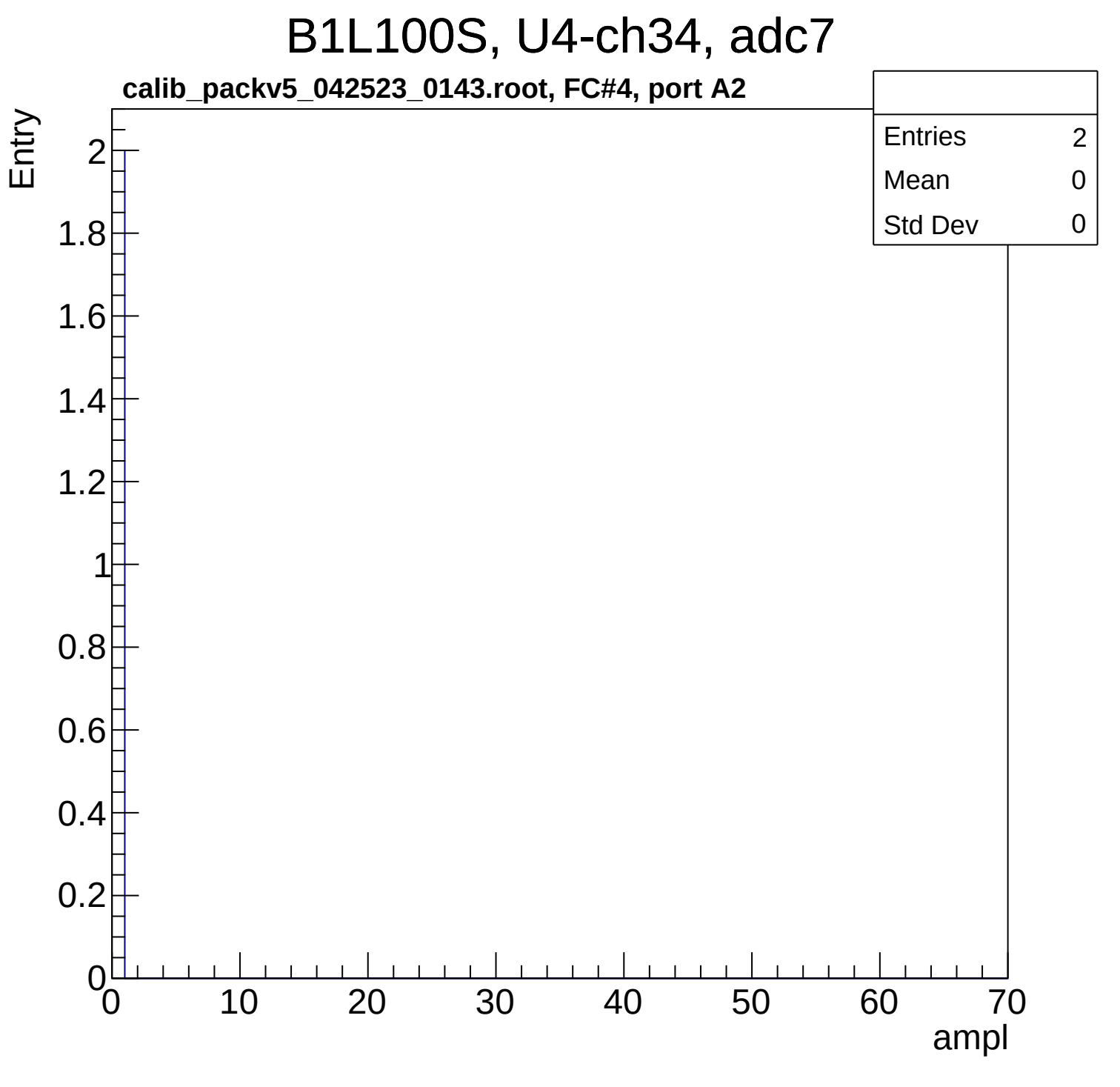

B1L100S, U4-ch34, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 42.6
Std Dev 3.364
Gaus mean : 43.3987
Gaus Width: 4.0663
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

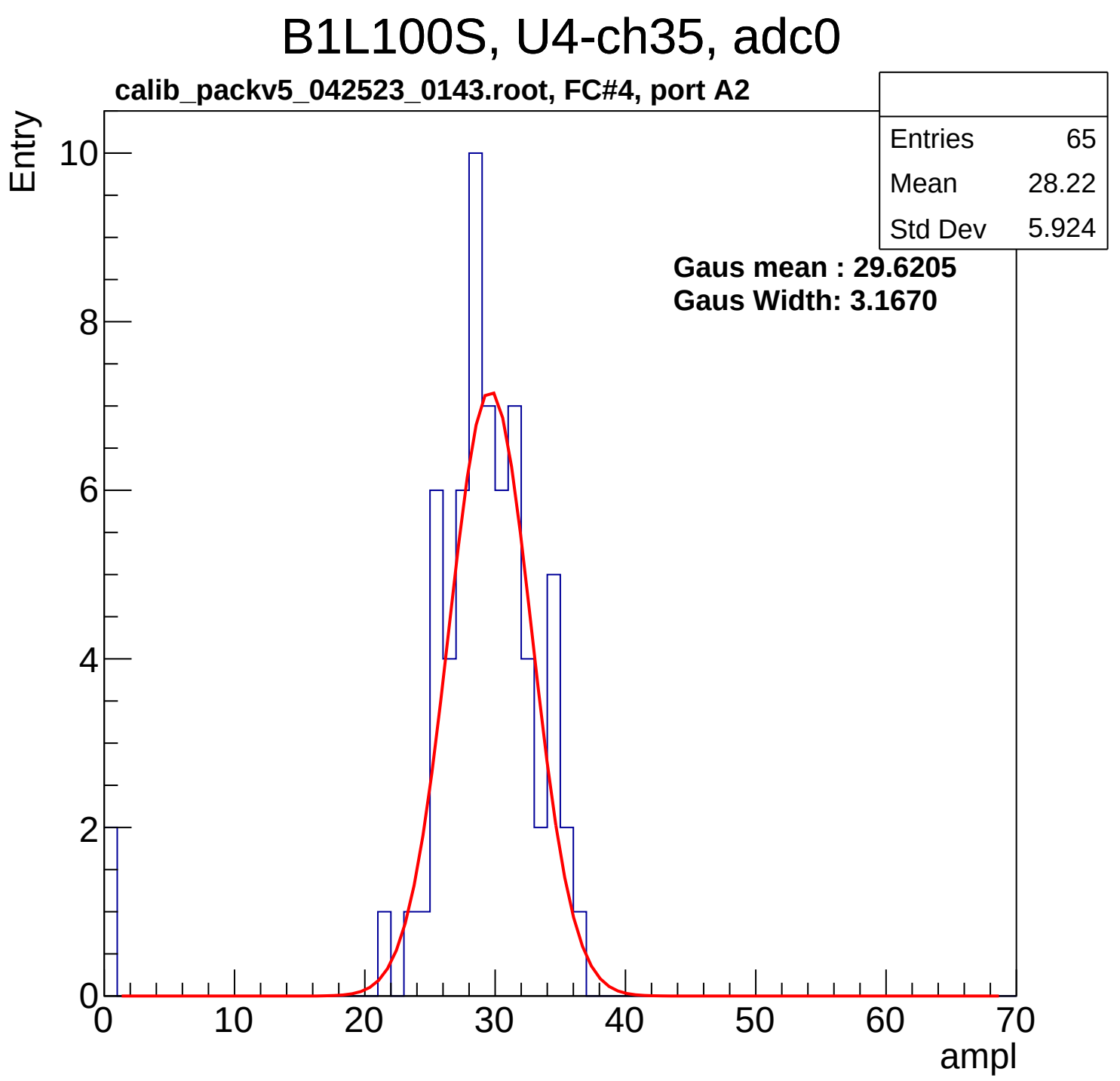

B1L100S, U4-ch34, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 50.31
Std Dev 3.759
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

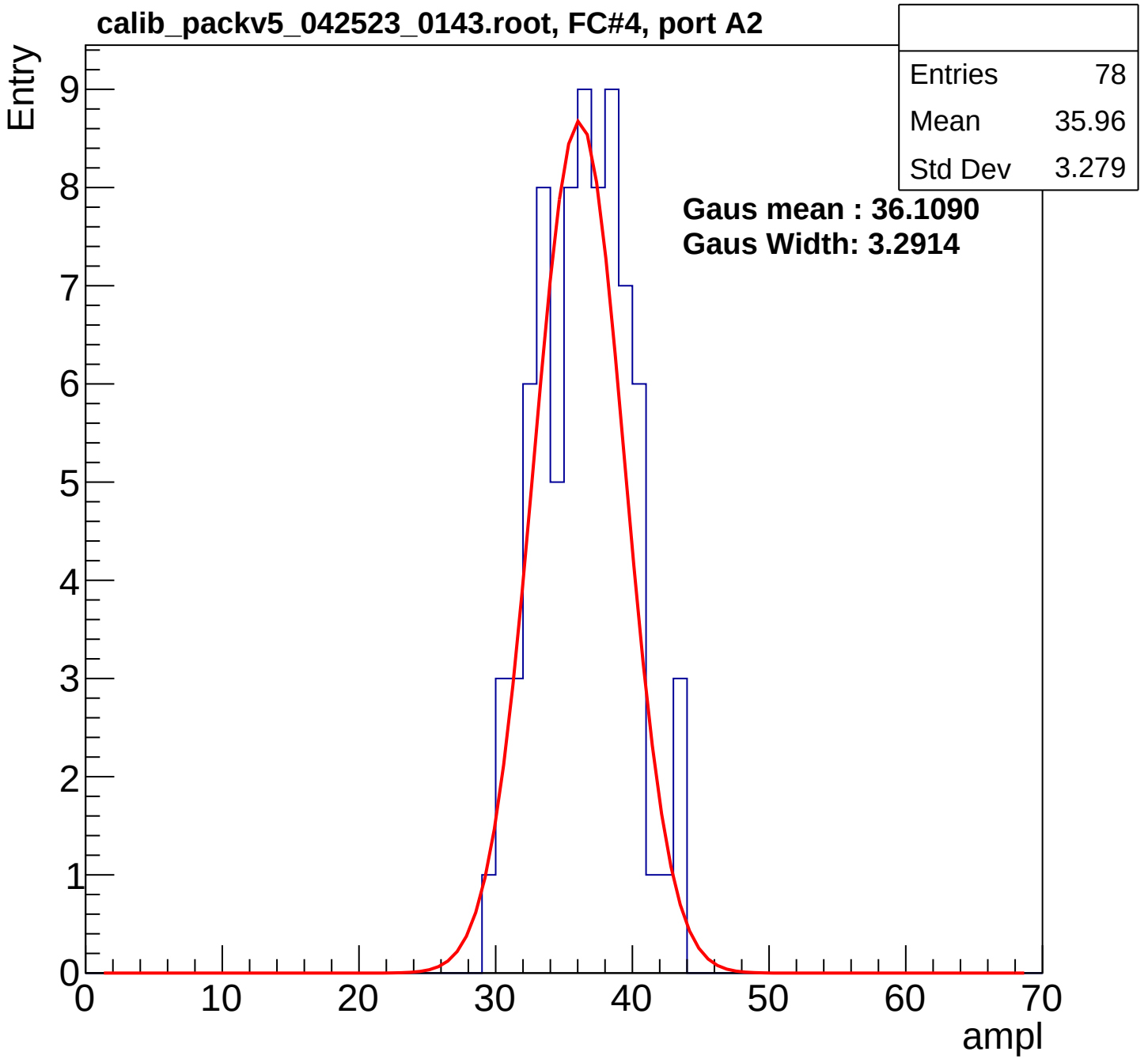

B1L100S, U4-ch34, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 55.78
Std Dev 3.547
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

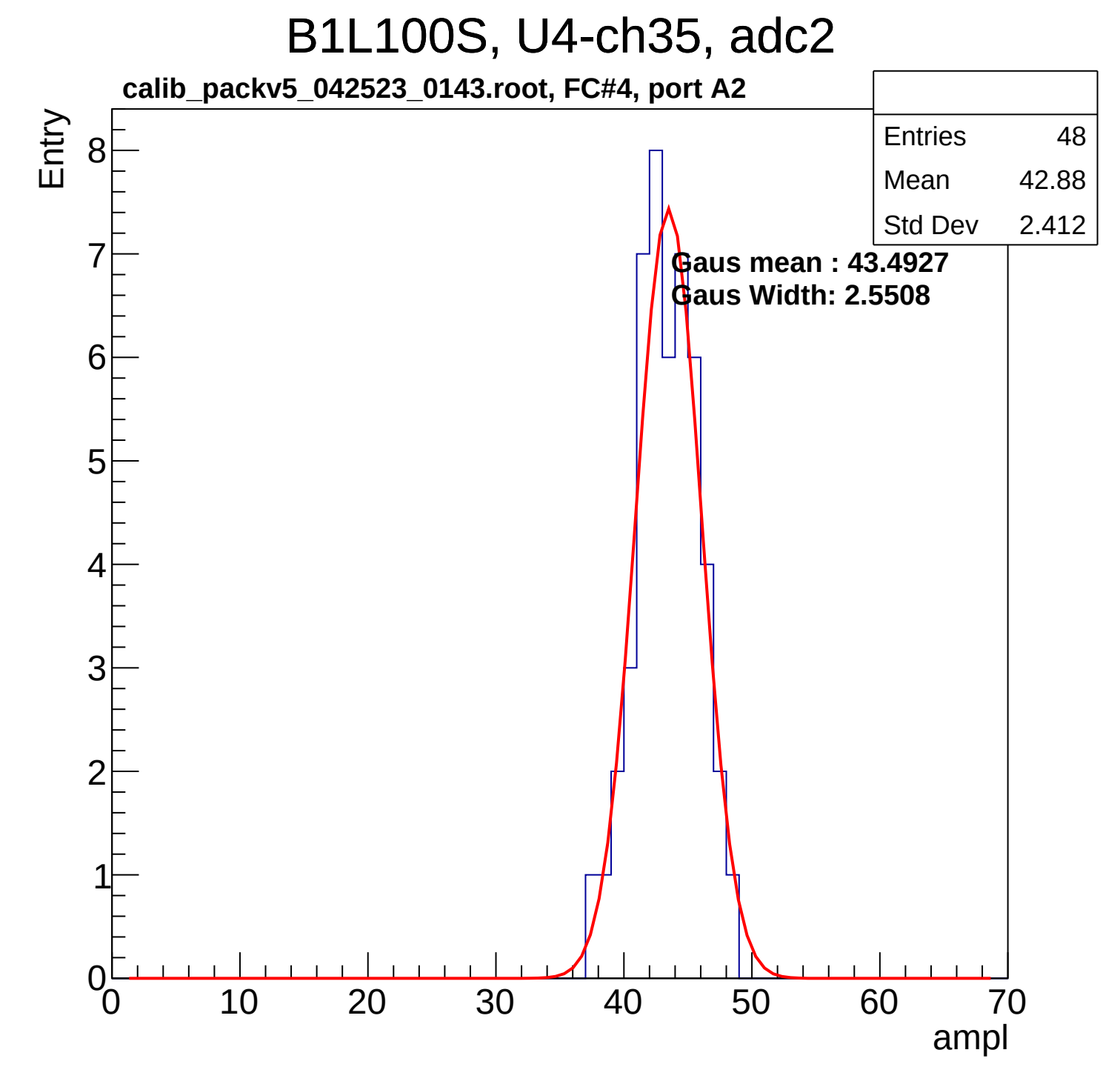

B1L100S, U4-ch34, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 37
Mean 58.03
Std Dev 10.05
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

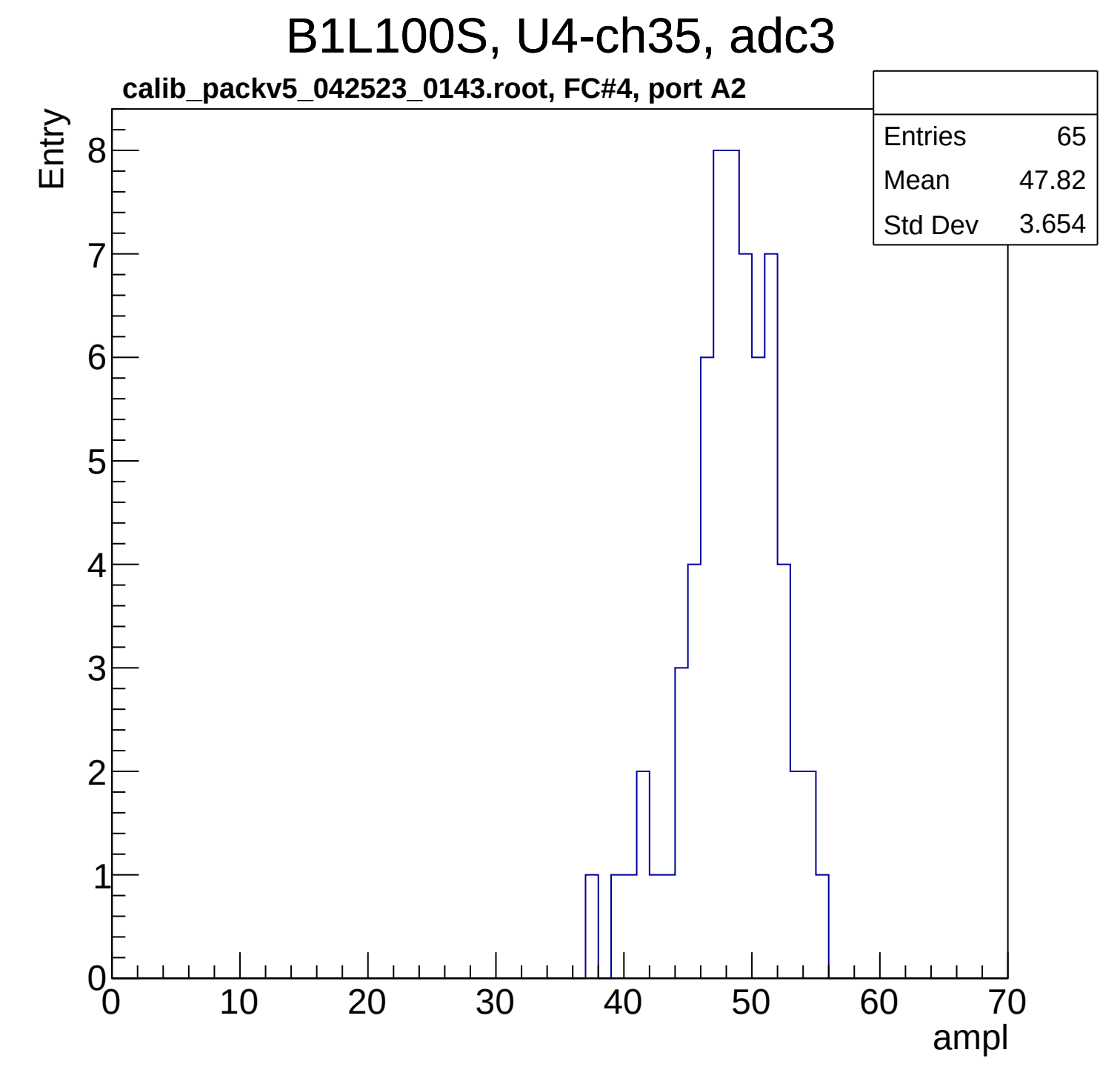

B1L100S, U4-ch34, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 8
Mean 62.5
Std Dev 0.5
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

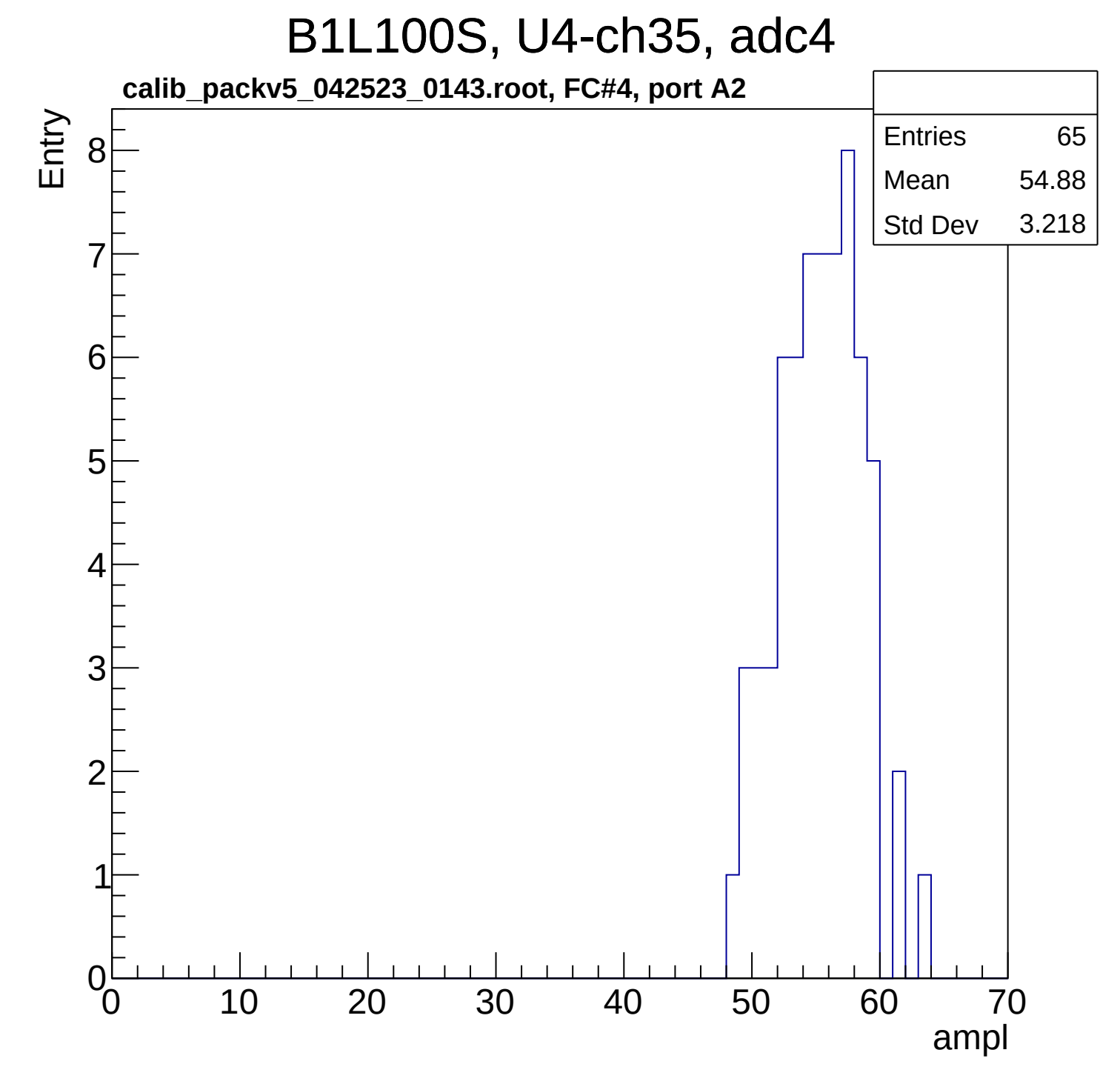

B1L100S, U4-ch34, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

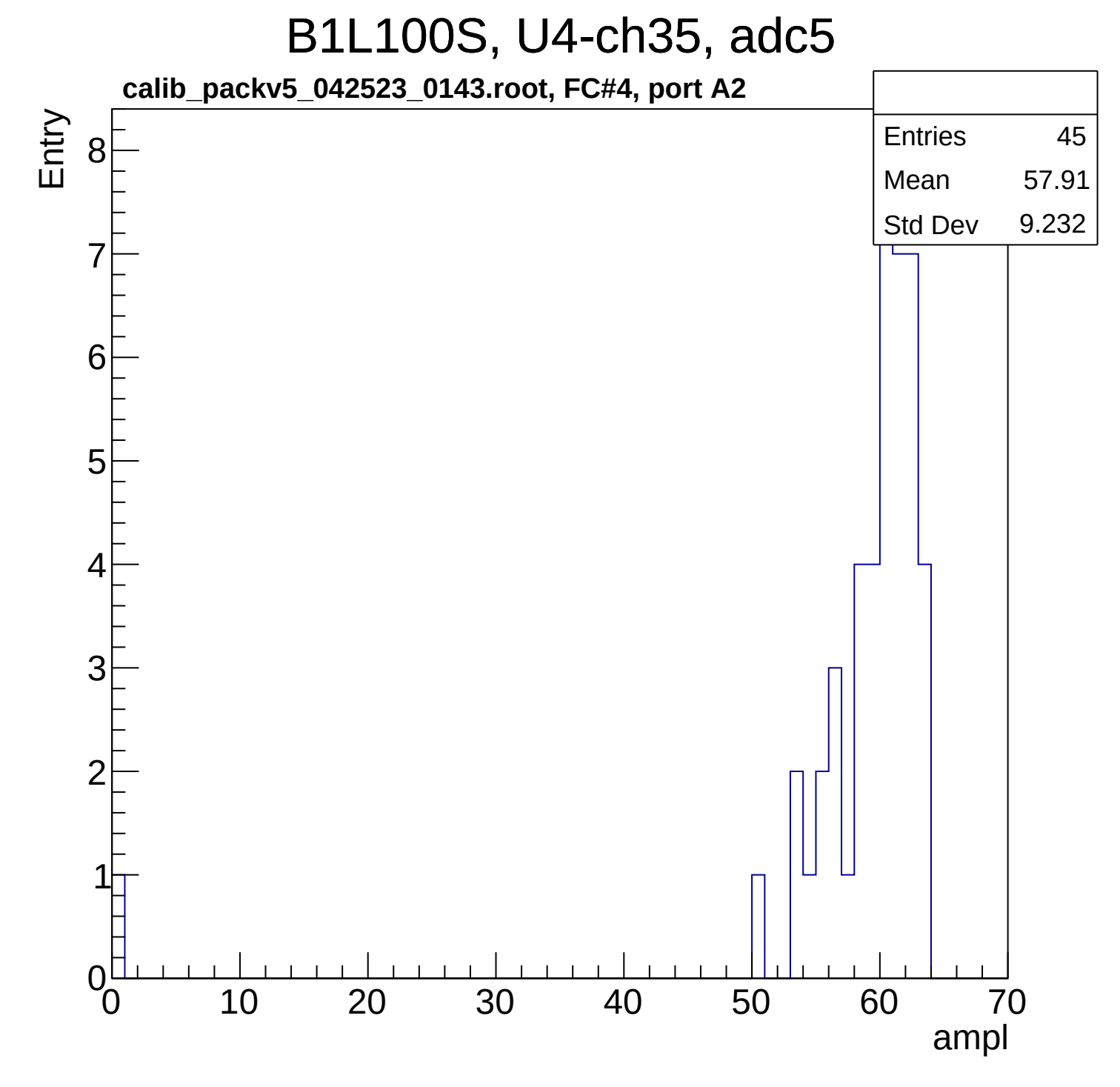

B1L100S, U4-ch35, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 28.22
Std Dev 5.924
Gaus mean : 29.6205
Gaus Width: 3.1670
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

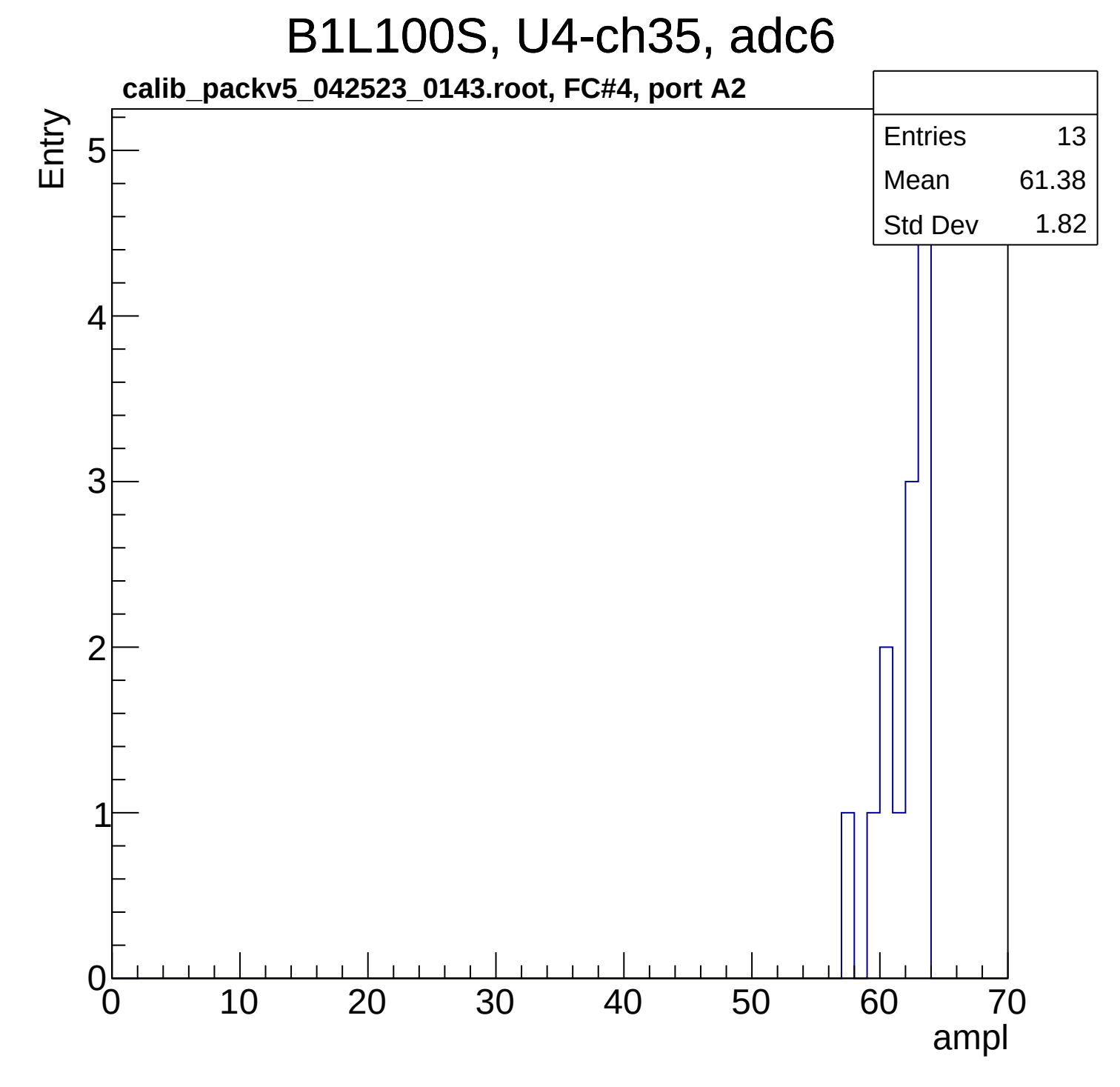

B1L100S, U4-ch35, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 35.96
Std Dev 3.279
Gaus mean : 36.1090
Gaus Width: 3.2914
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

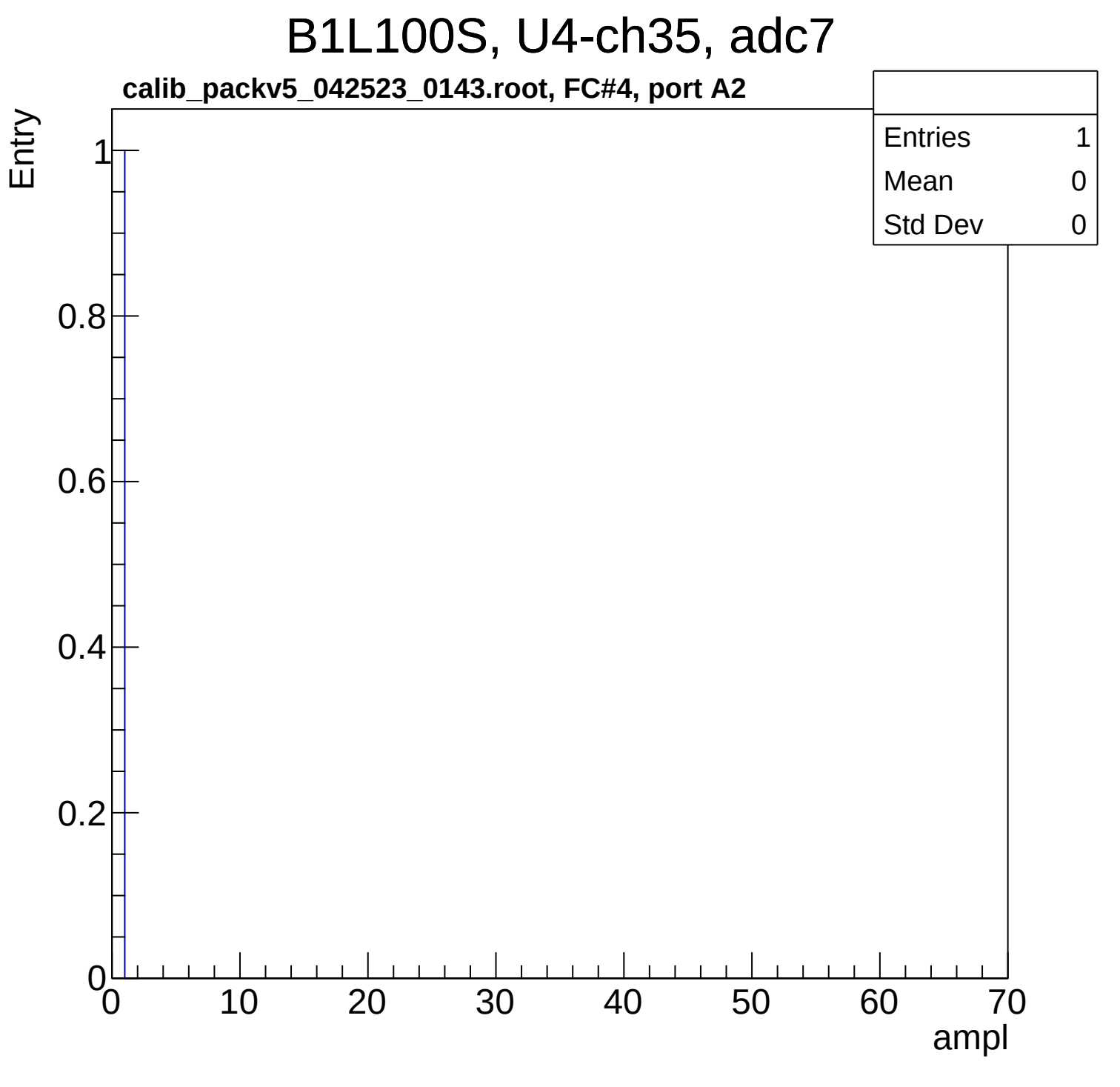

B1L100S, U4-ch35, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 42.88
Std Dev 2.412
Gaus mean : 43.4927
Gaus Width: 2.5508
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

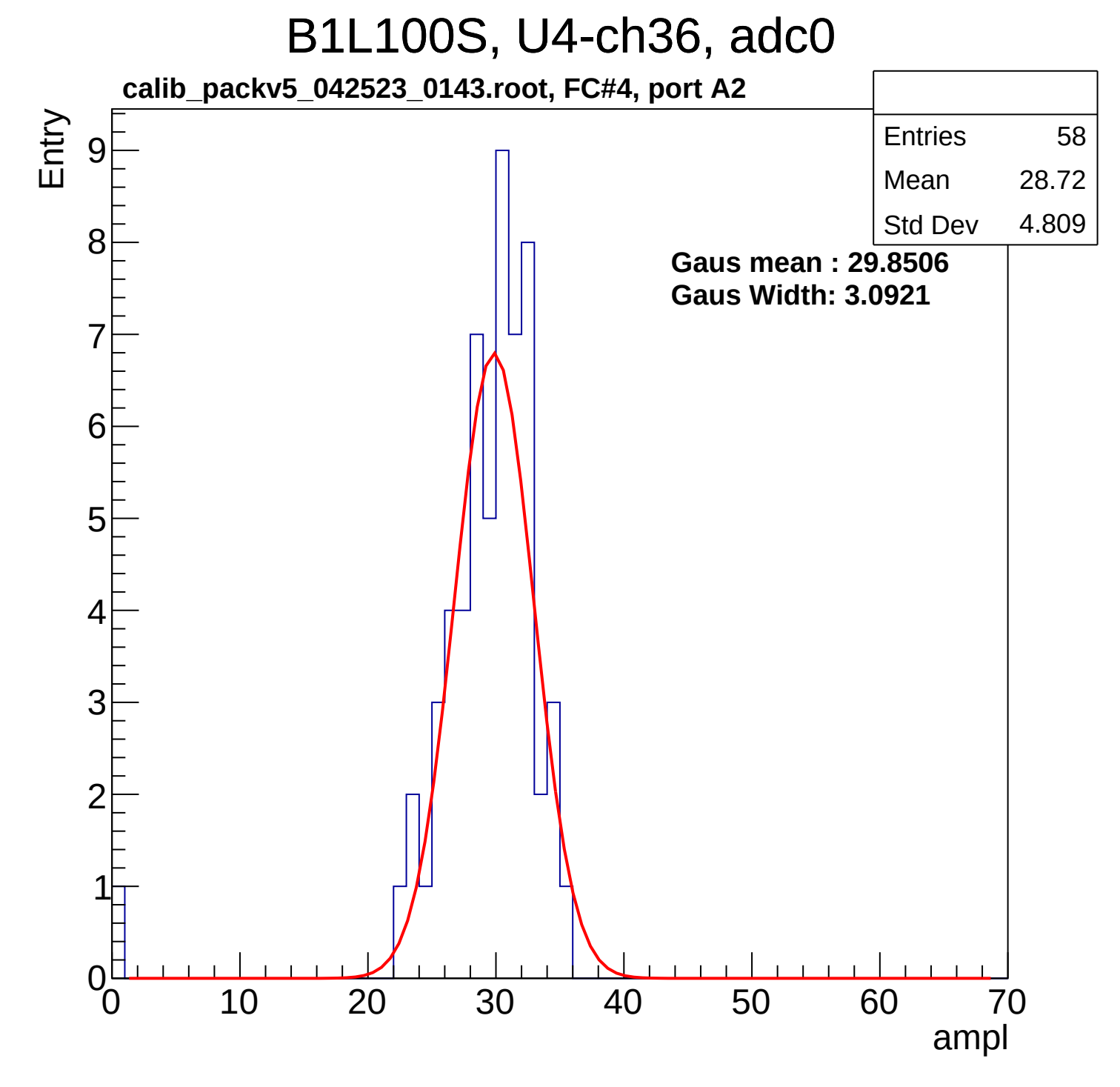

B1L100S, U4-ch35, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 47.82
Std Dev 3.654
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

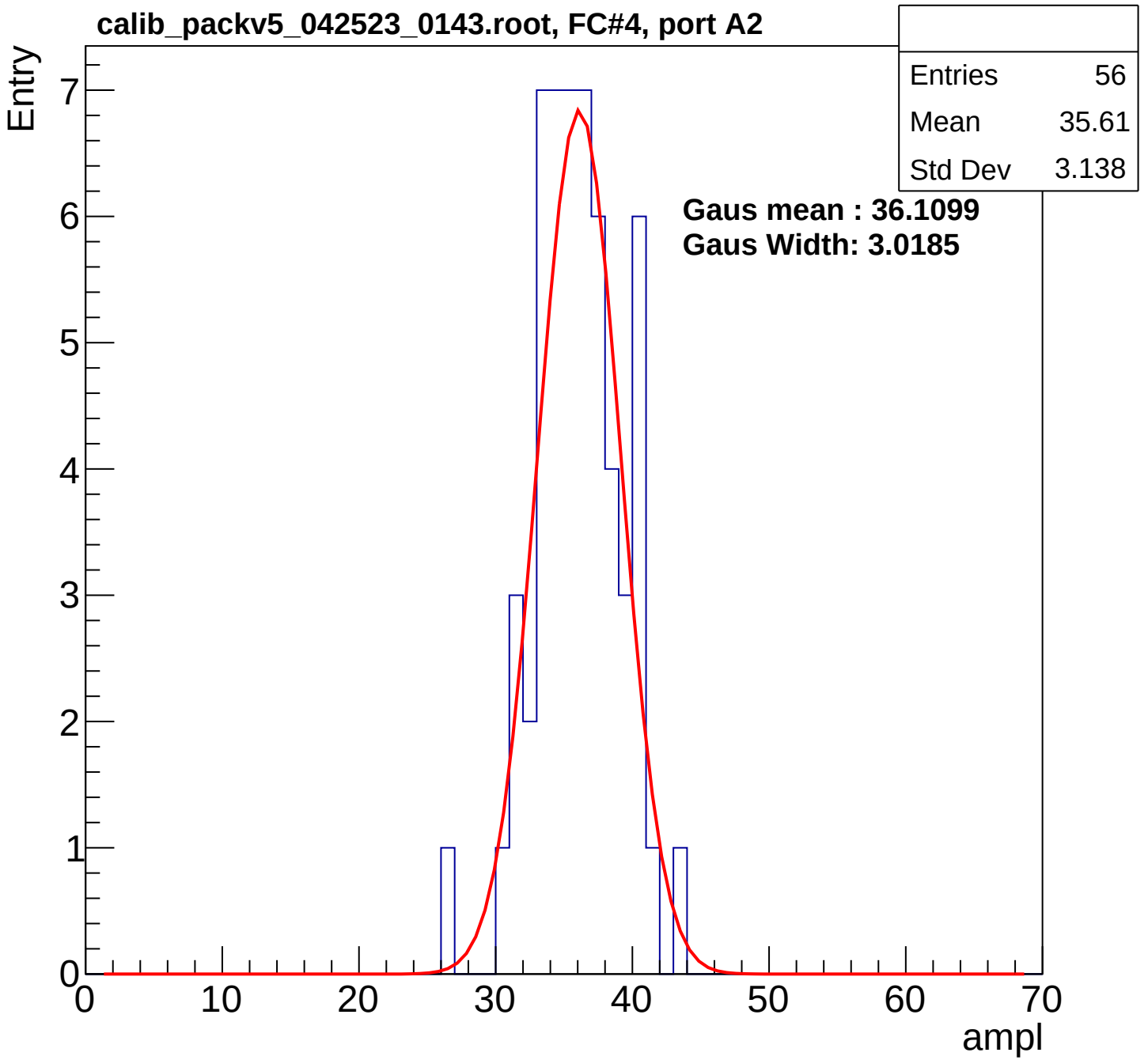

B1L100S, U4-ch35, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 54.88
Std Dev 3.218
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

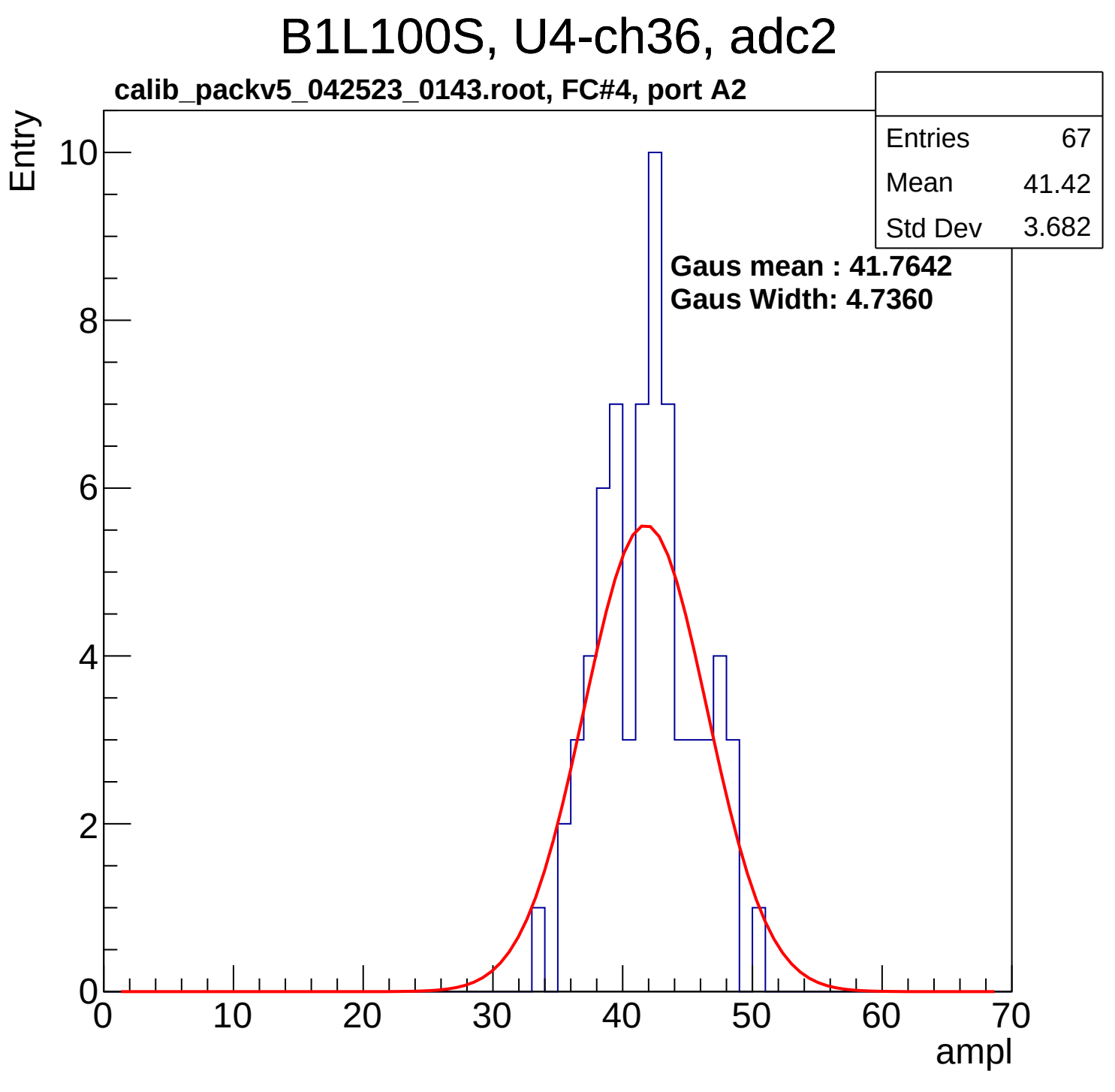

B1L100S, U4-ch35, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 45
Mean 57.91
Std Dev 9.232
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

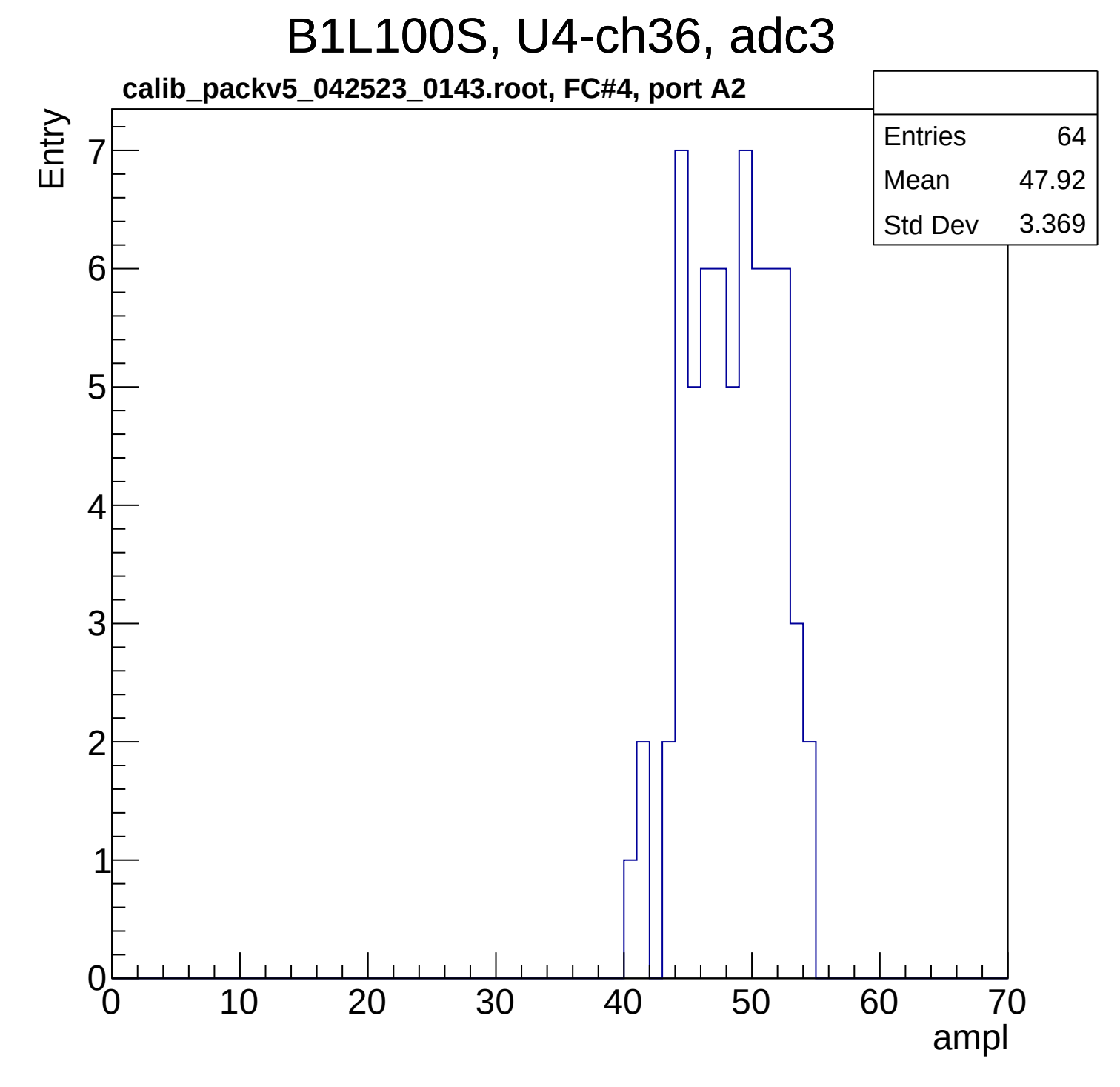

B1L100S, U4-ch35, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 13
Mean 61.38
Std Dev 1.82
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

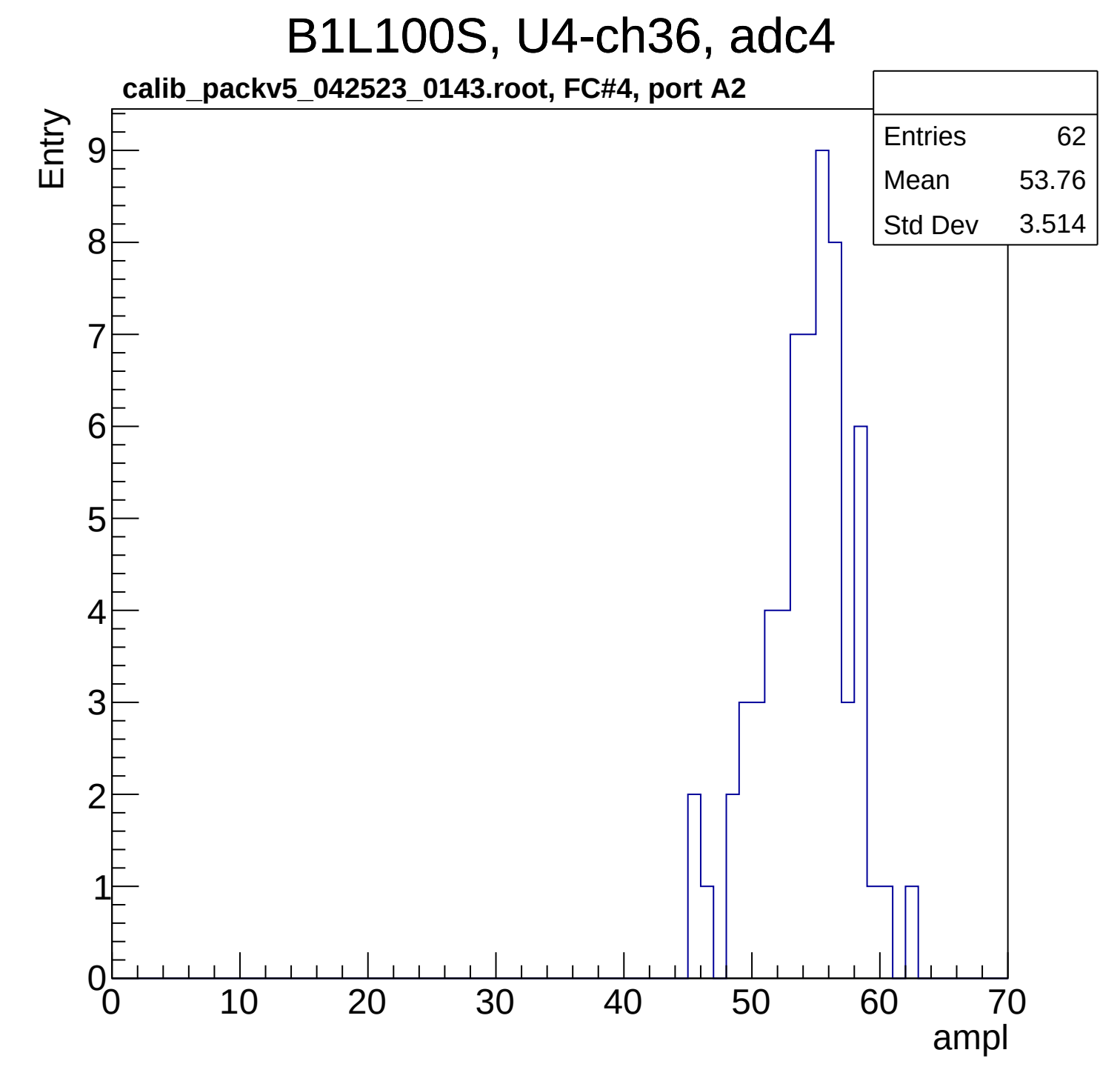

B1L100S, U4-ch35, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

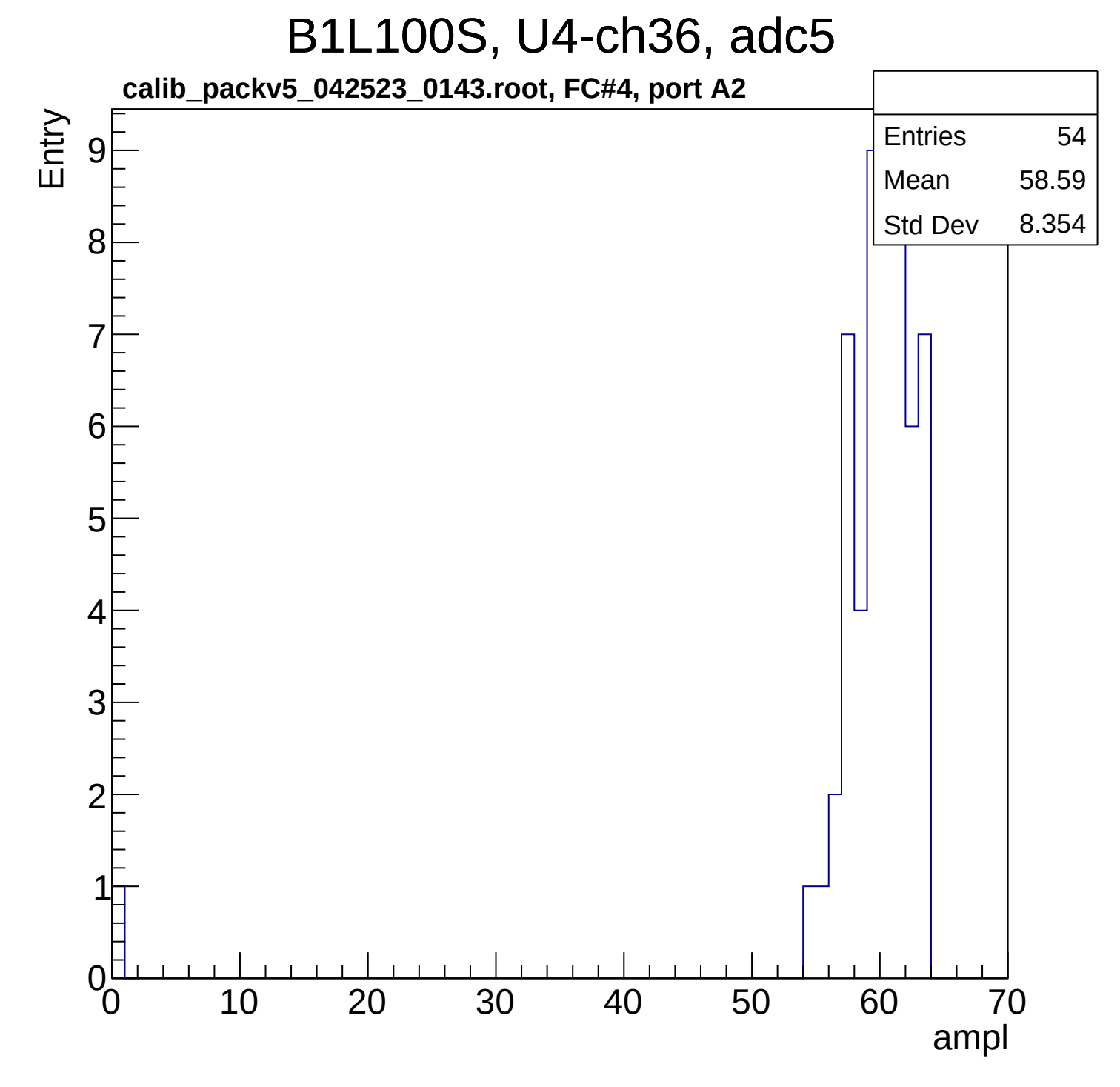

B1L100S, U4-ch36, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 28.72
Std Dev 4.809
Gaus mean : 29.8506
Gaus Width: 3.0921
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

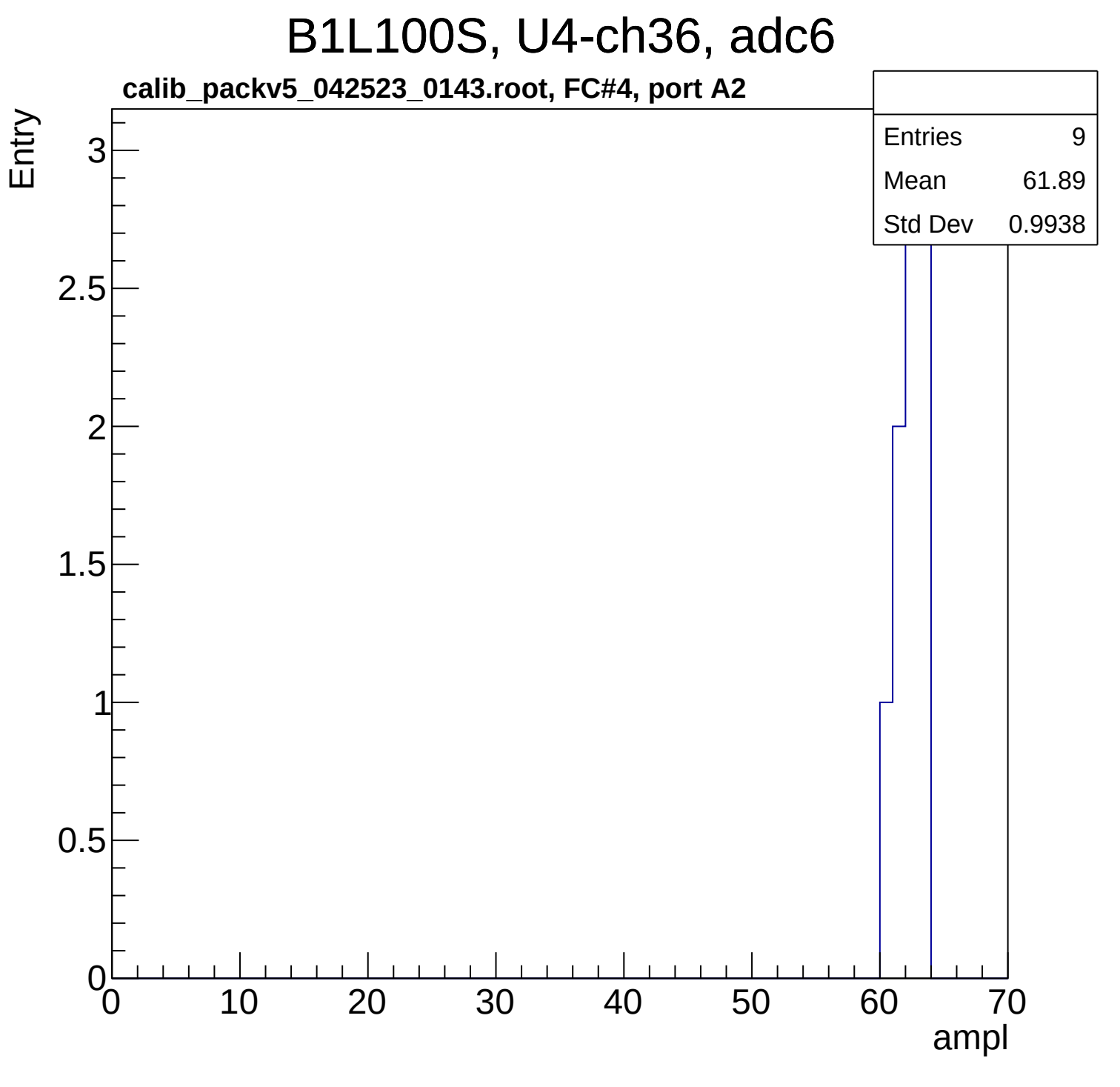

B1L100S, U4-ch36, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 35.61
Std Dev 3.138
Gaus mean : 36.1099
Gaus Width: 3.0185
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

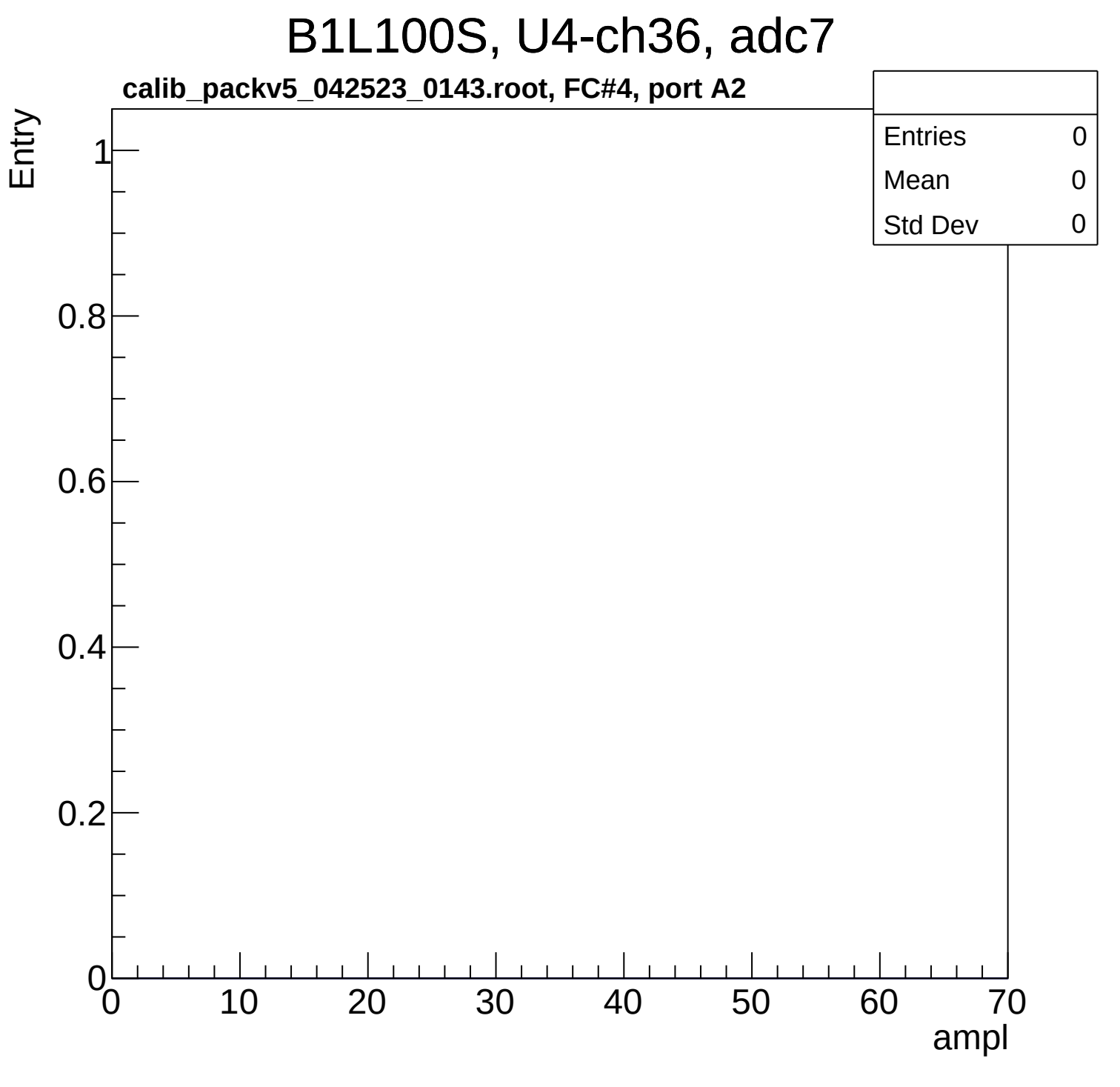

B1L100S, U4-ch36, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 41.42
Std Dev 3.682
Gaus mean : 41.7642
Gaus Width: 4.7360
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

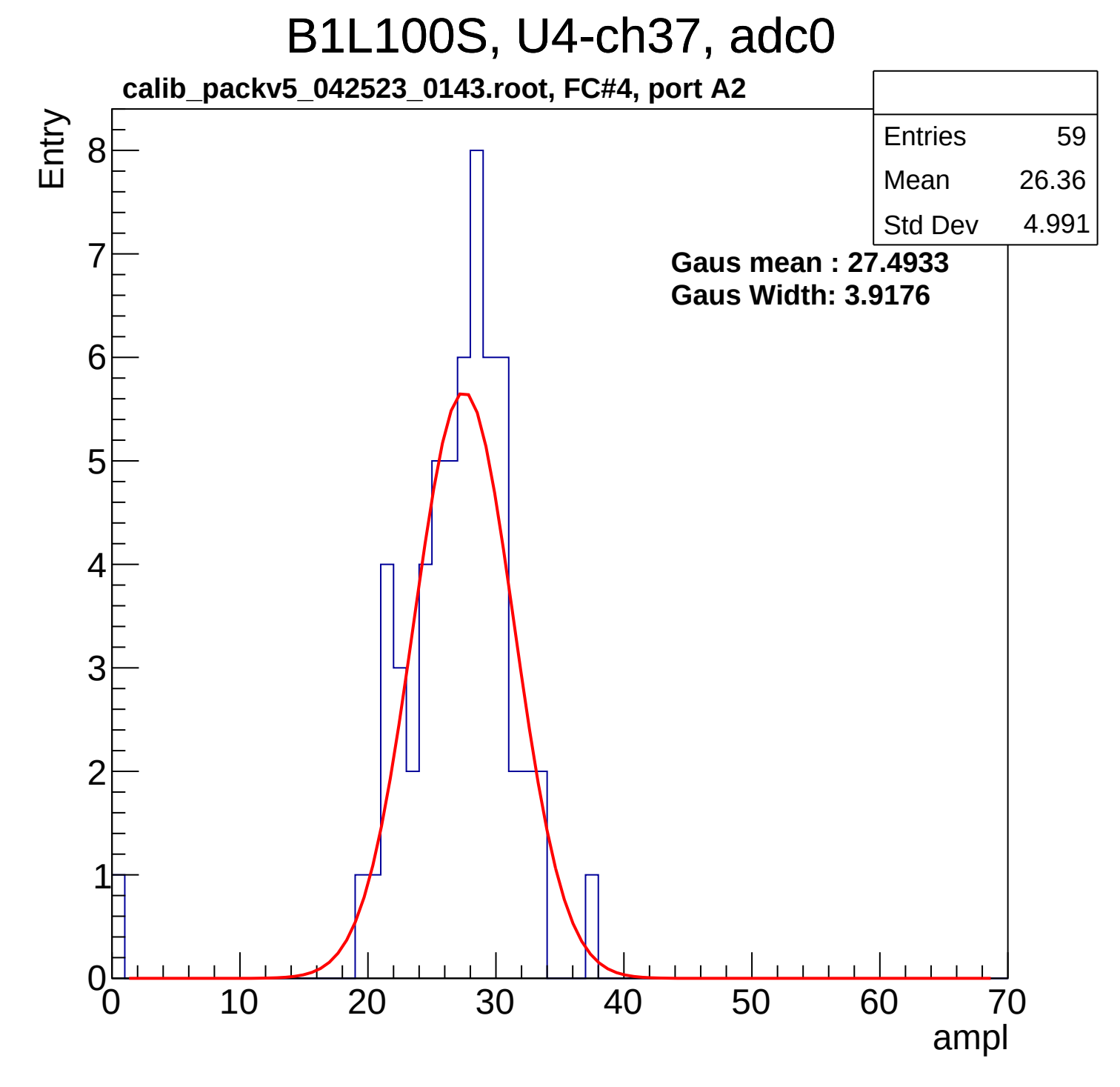

B1L100S, U4-ch36, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 47.92
Std Dev 3.369
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

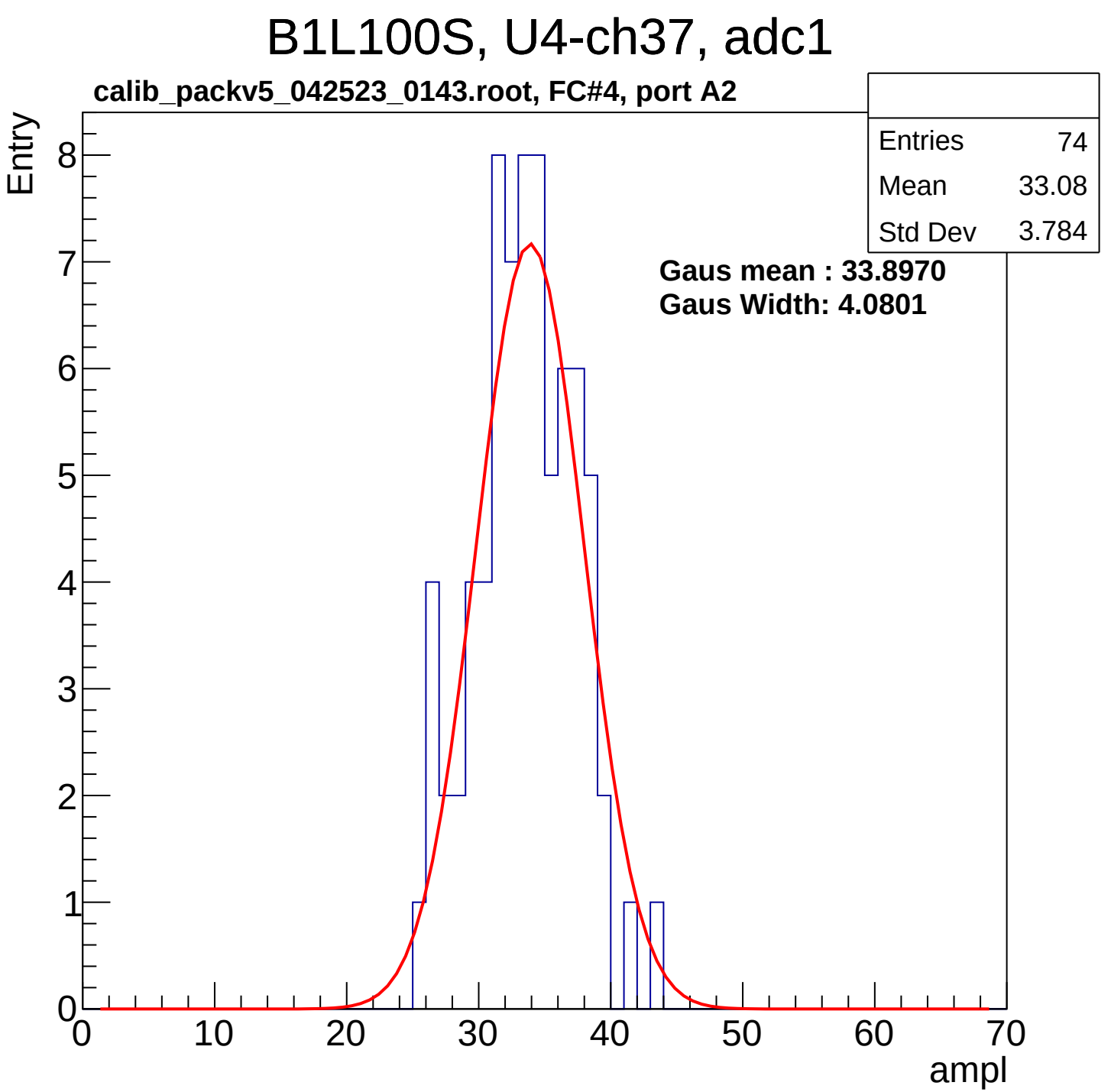

B1L100S, U4-ch36, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 53.76
Std Dev 3.514
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

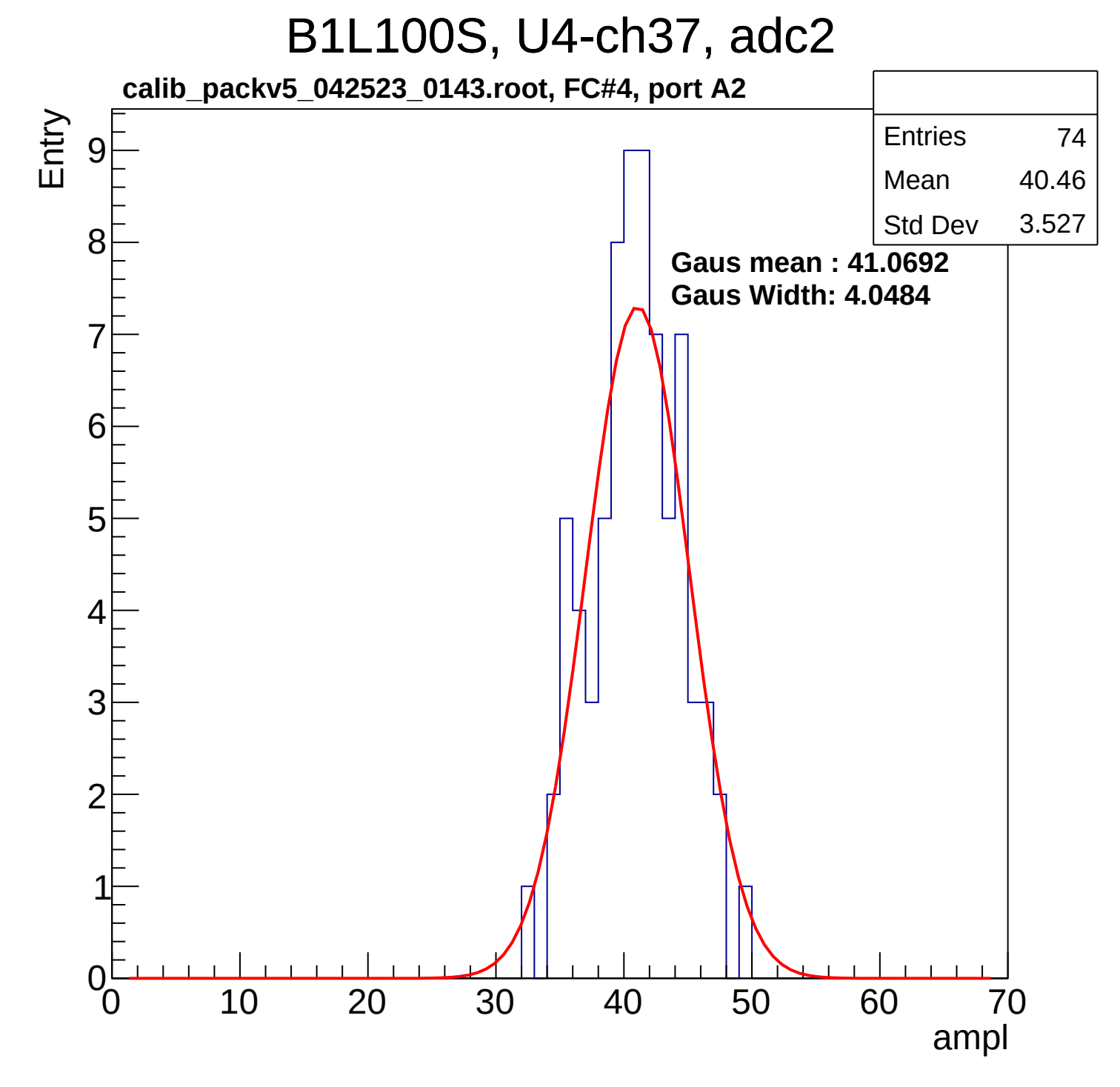

B1L100S, U4-ch36, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 58.59
Std Dev 8.354
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

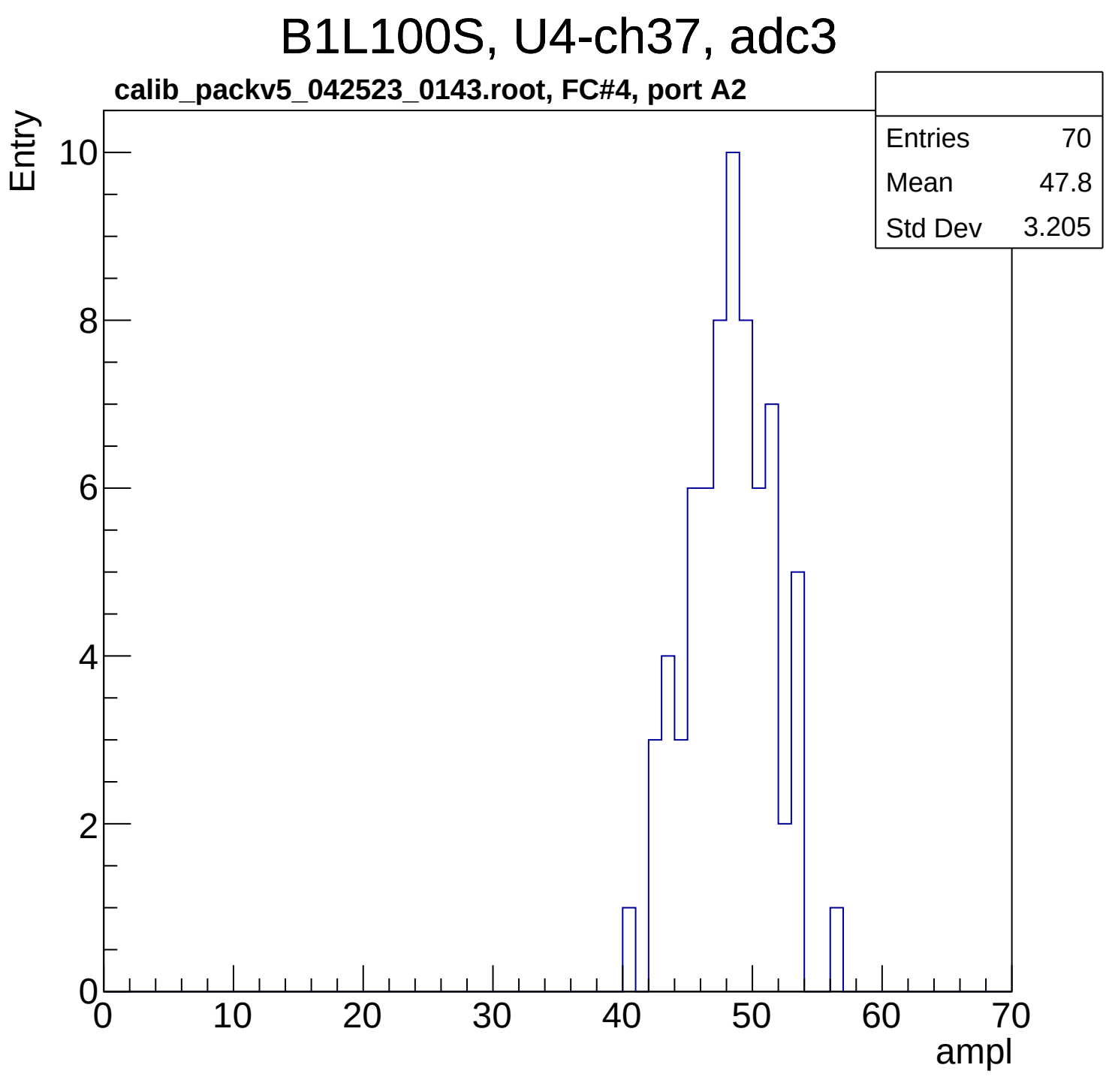

B1L100S, U4-ch36, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 61.89
Std Dev 0.9938
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

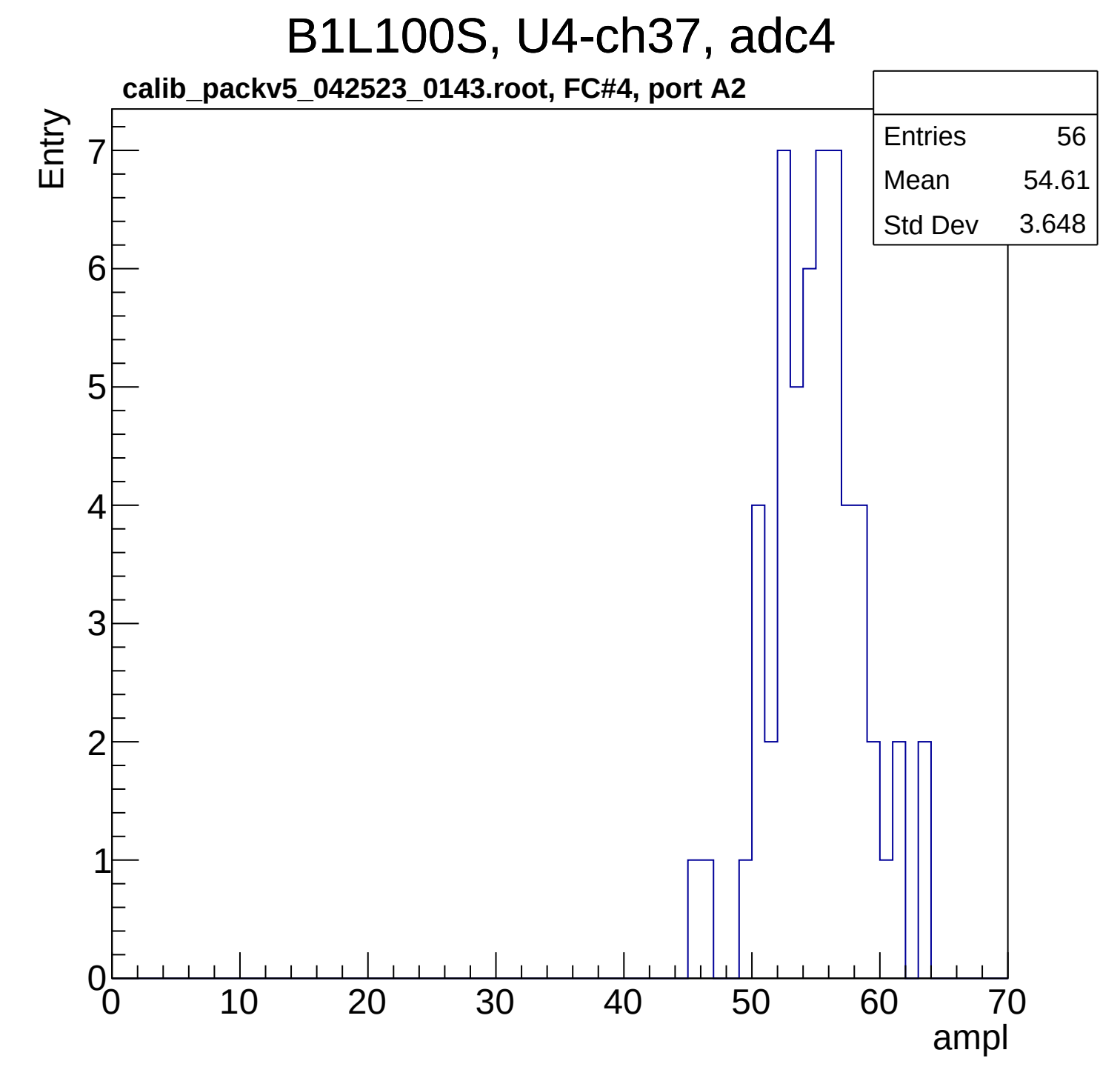

B1L100S, U4-ch36, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

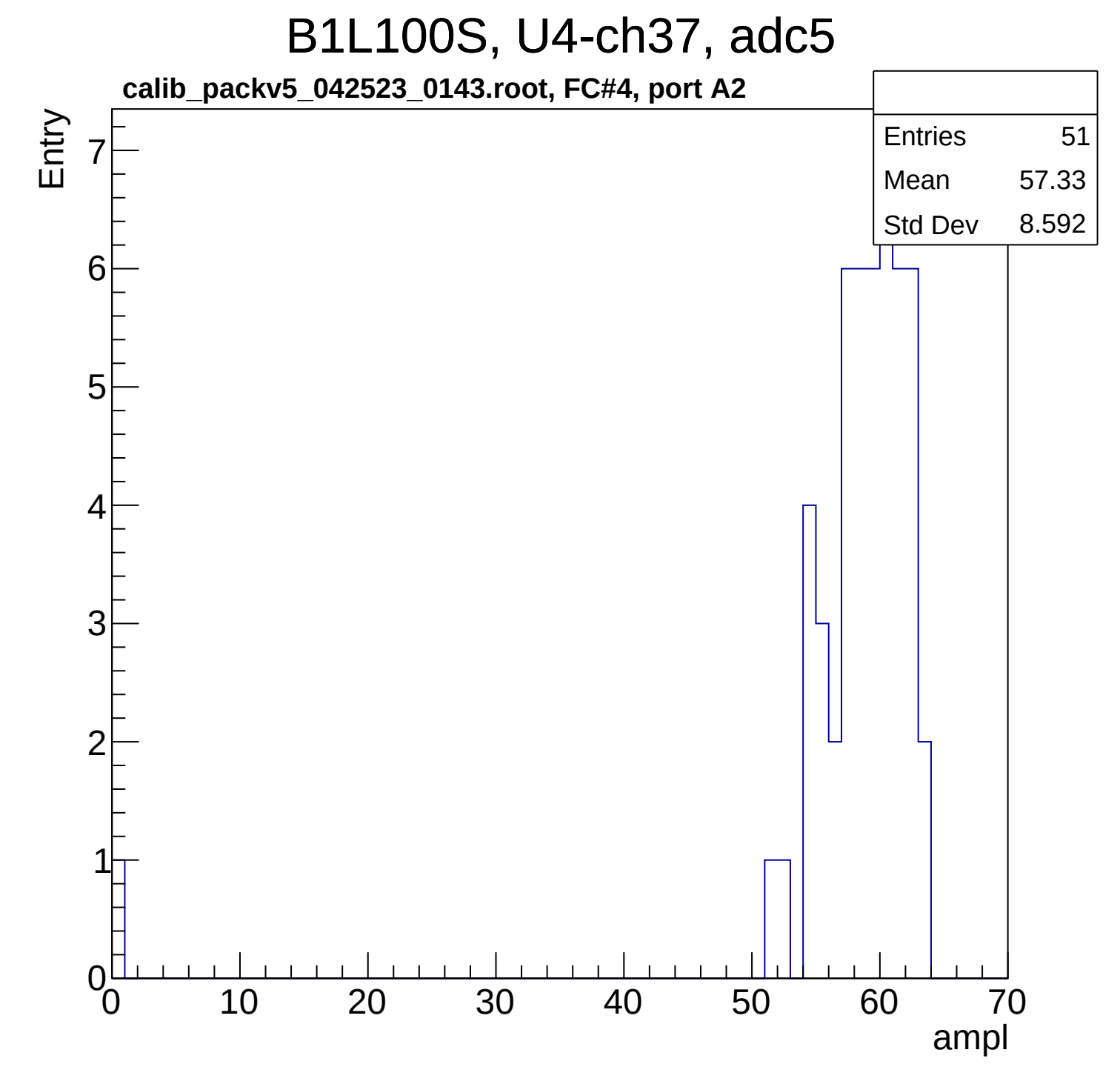

B1L100S, U4-ch37, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 26.36
Std Dev 4.991
Gaus mean : 27.4933
Gaus Width: 3.9176
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

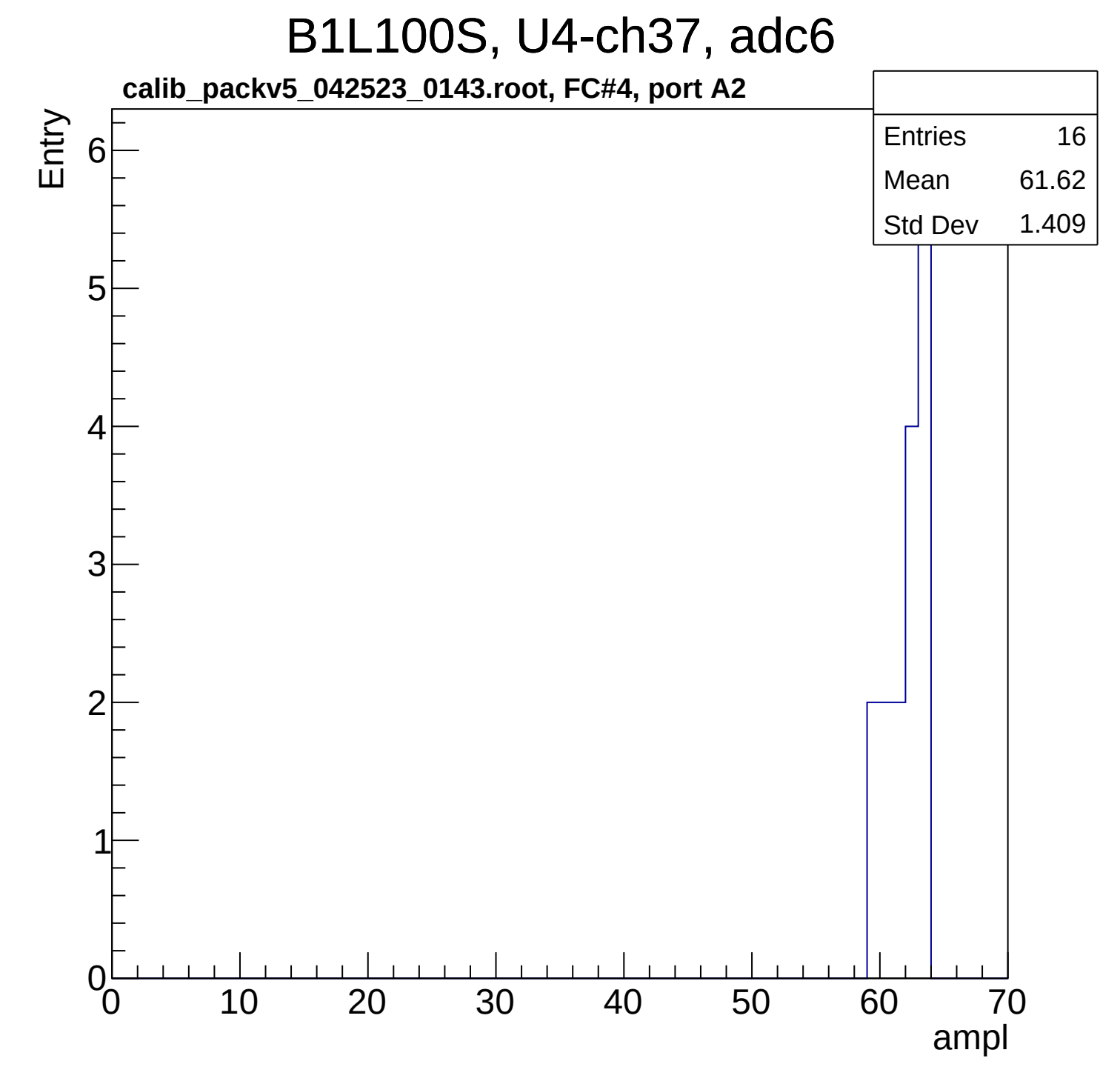

B1L100S, U4-ch37, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 33.08
Std Dev 3.784
Gaus mean : 33.8970
Gaus Width: 4.0801
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

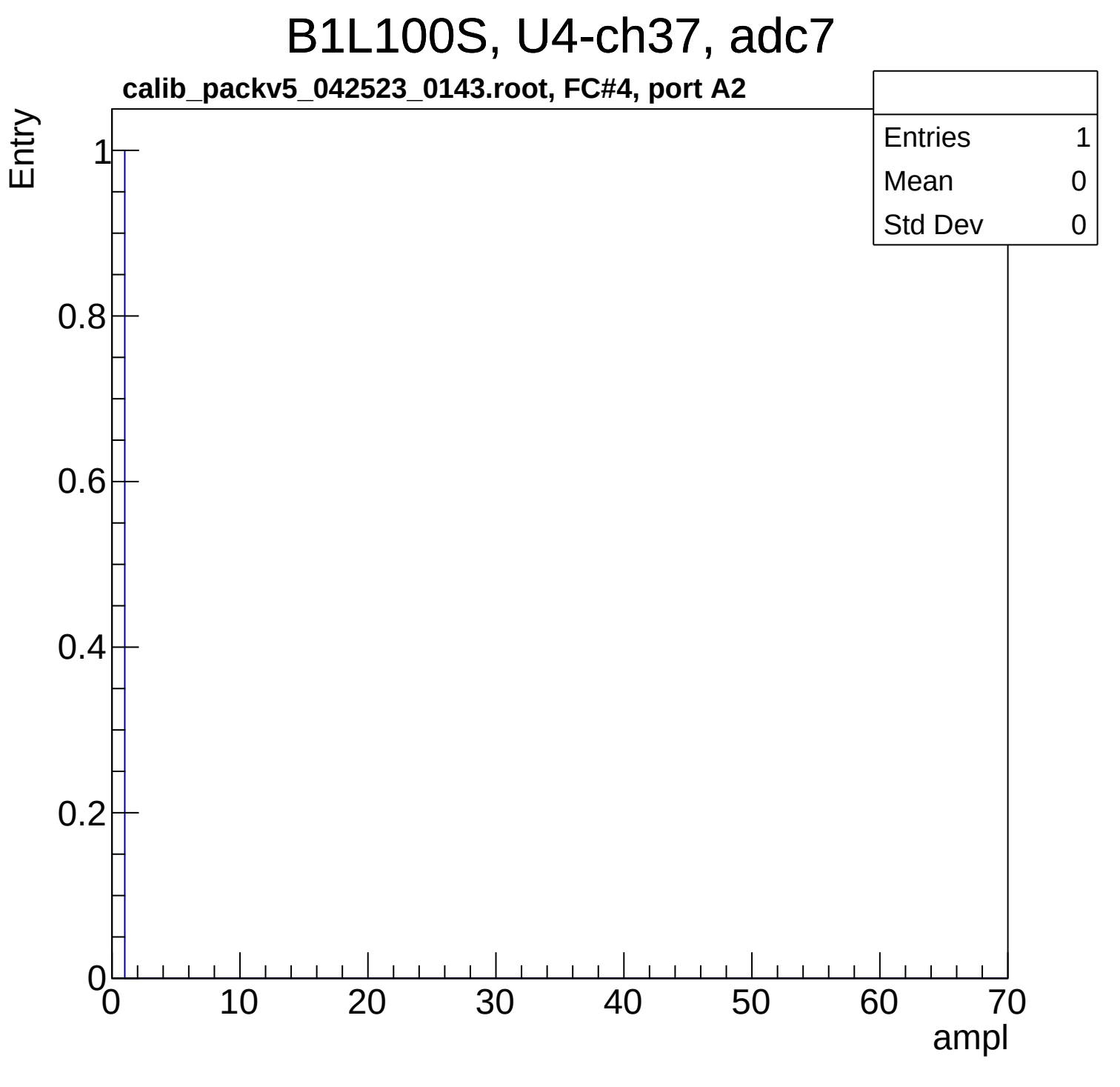

B1L100S, U4-ch37, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 40.46
Std Dev 3.527
Gaus mean : 41.0692
Gaus Width: 4.0484
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

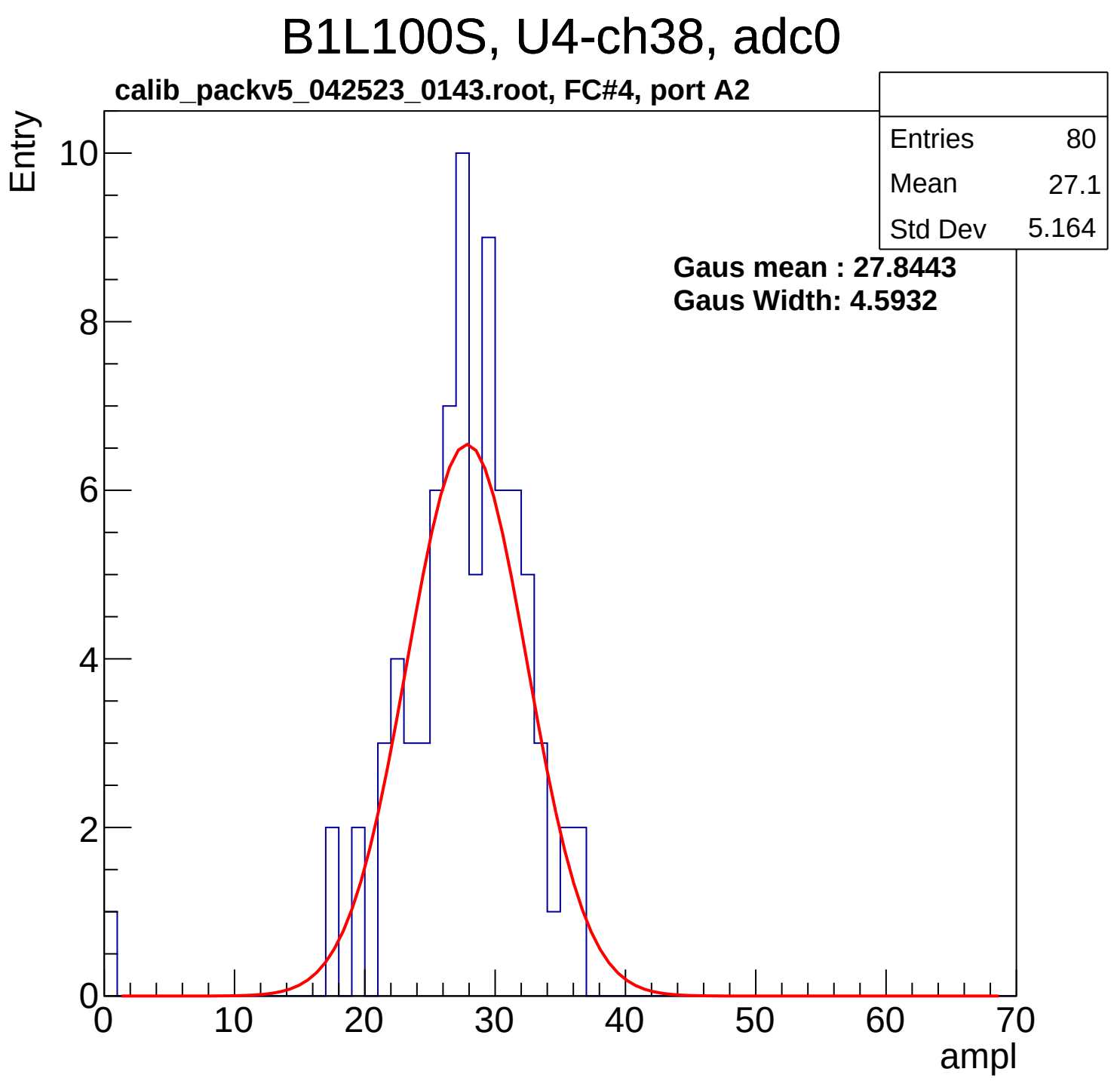

B1L100S, U4-ch37, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 47.8
Std Dev 3.205
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

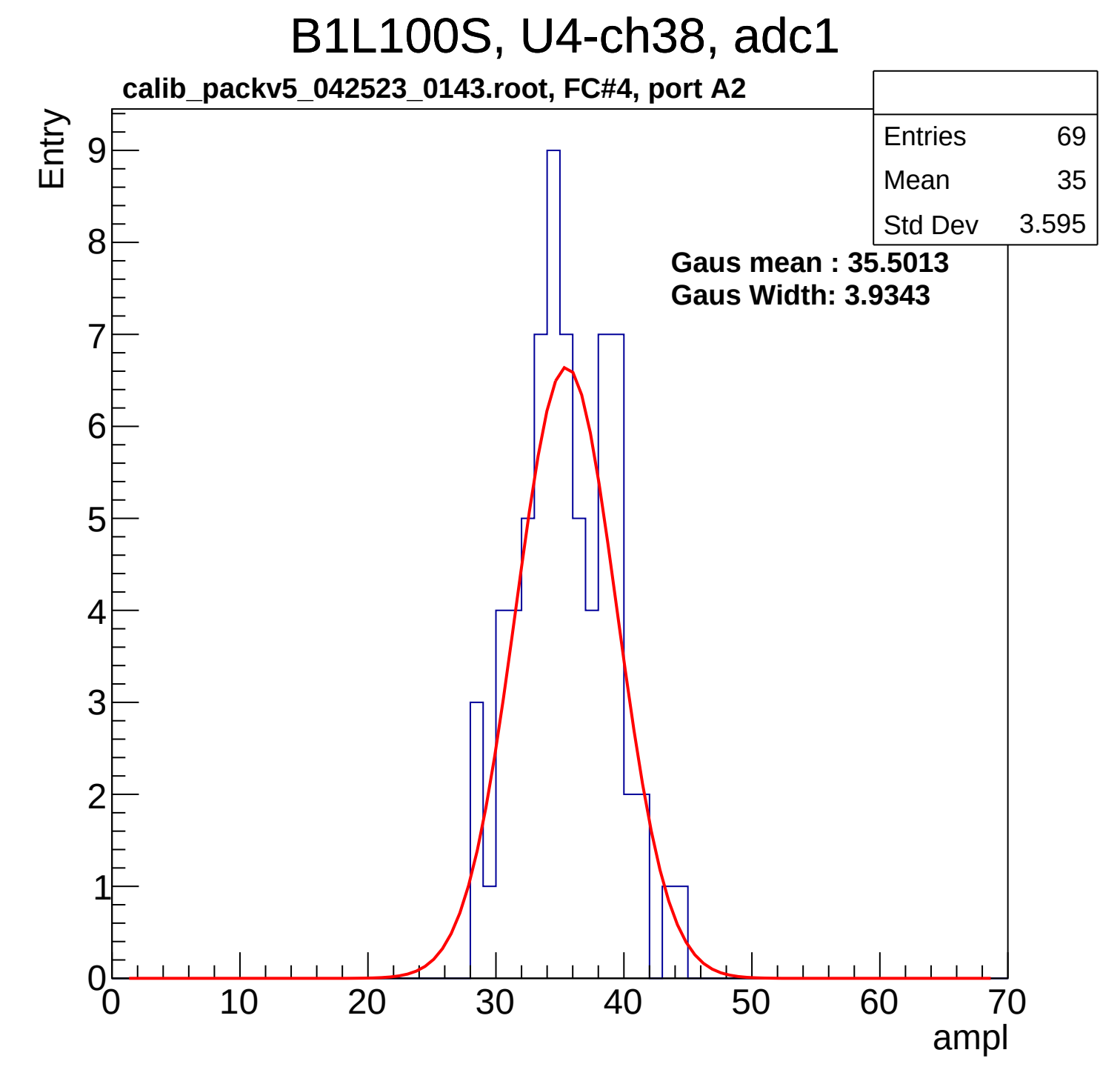

B1L100S, U4-ch37, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 54.61
Std Dev 3.648
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

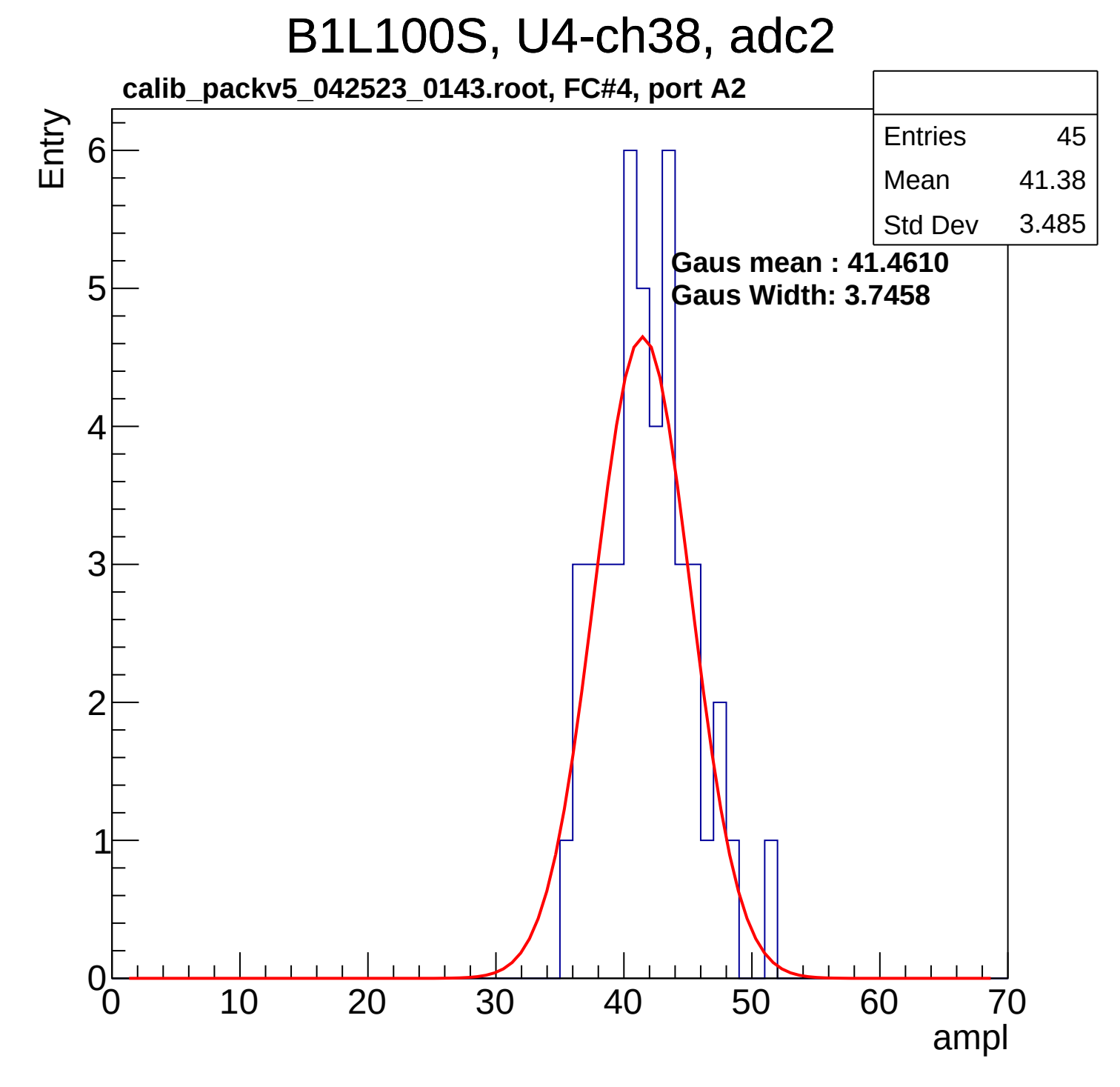

B1L100S, U4-ch37, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 57.33
Std Dev 8.592
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

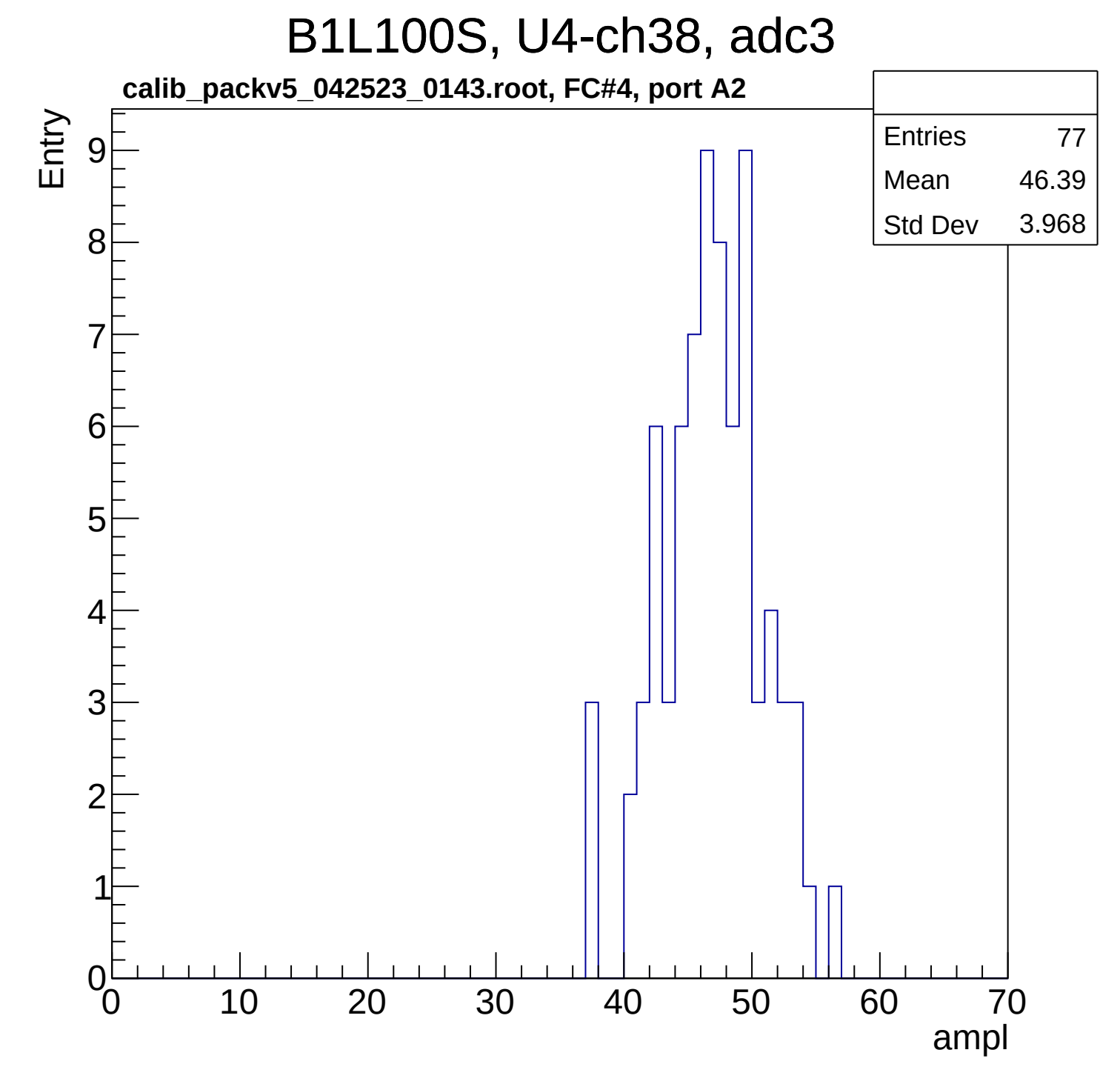

B1L100S, U4-ch37, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 16
Mean 61.62
Std Dev 1.409
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

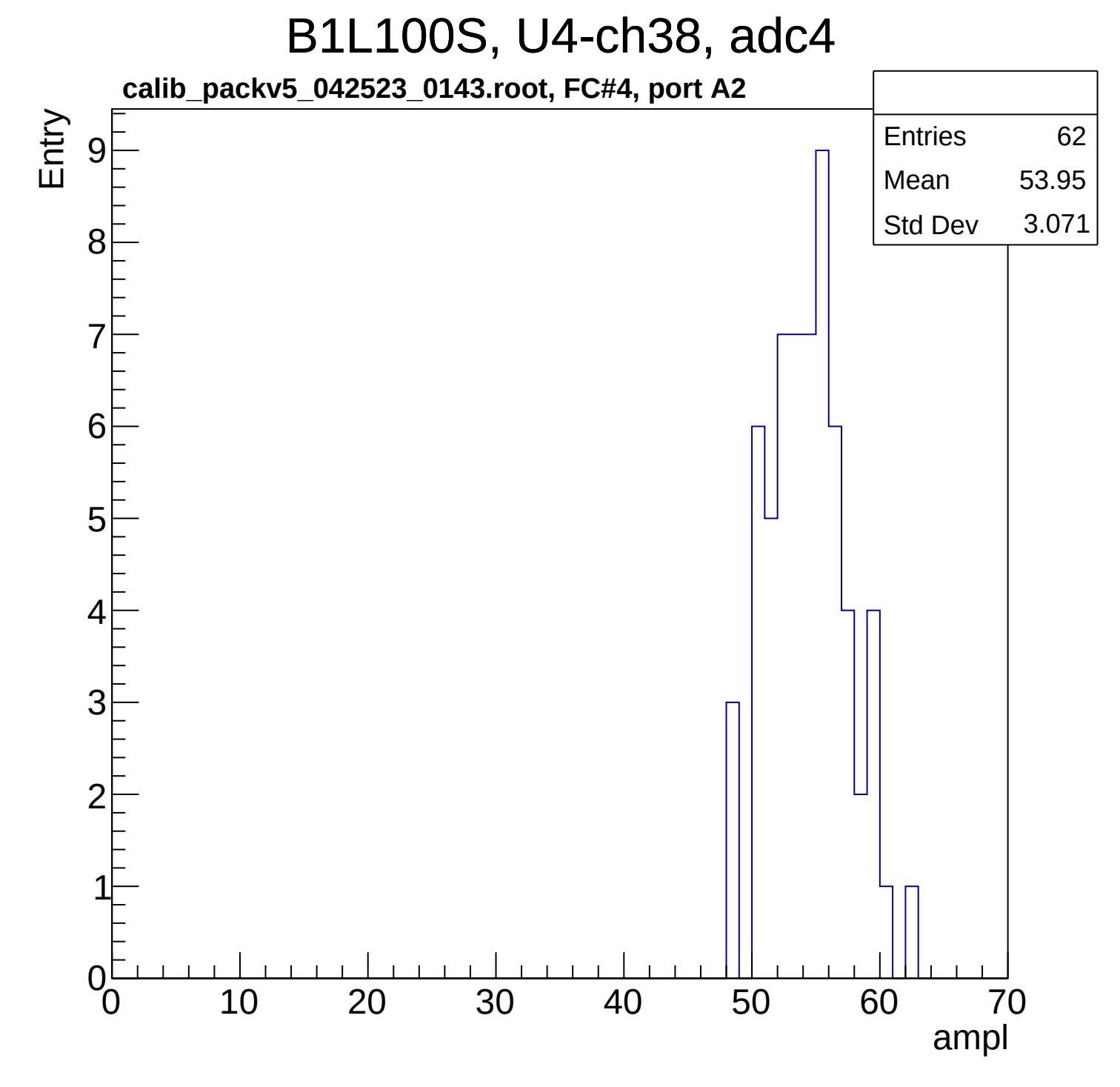

B1L100S, U4-ch37, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

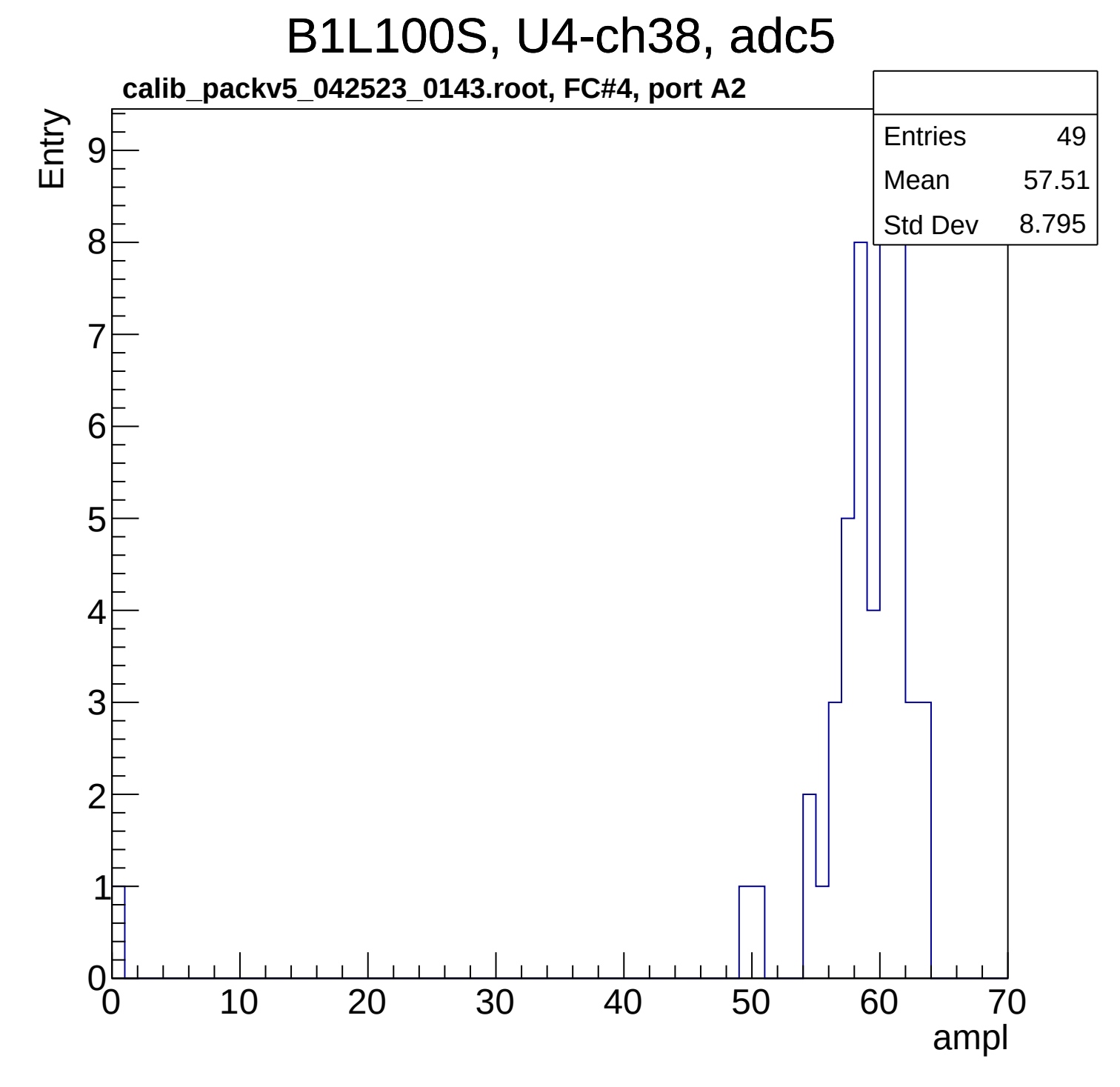

B1L100S, U4-ch38, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 27.1
Std Dev 5.164
Gaus mean : 27.8443
Gaus Width: 4.5932
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

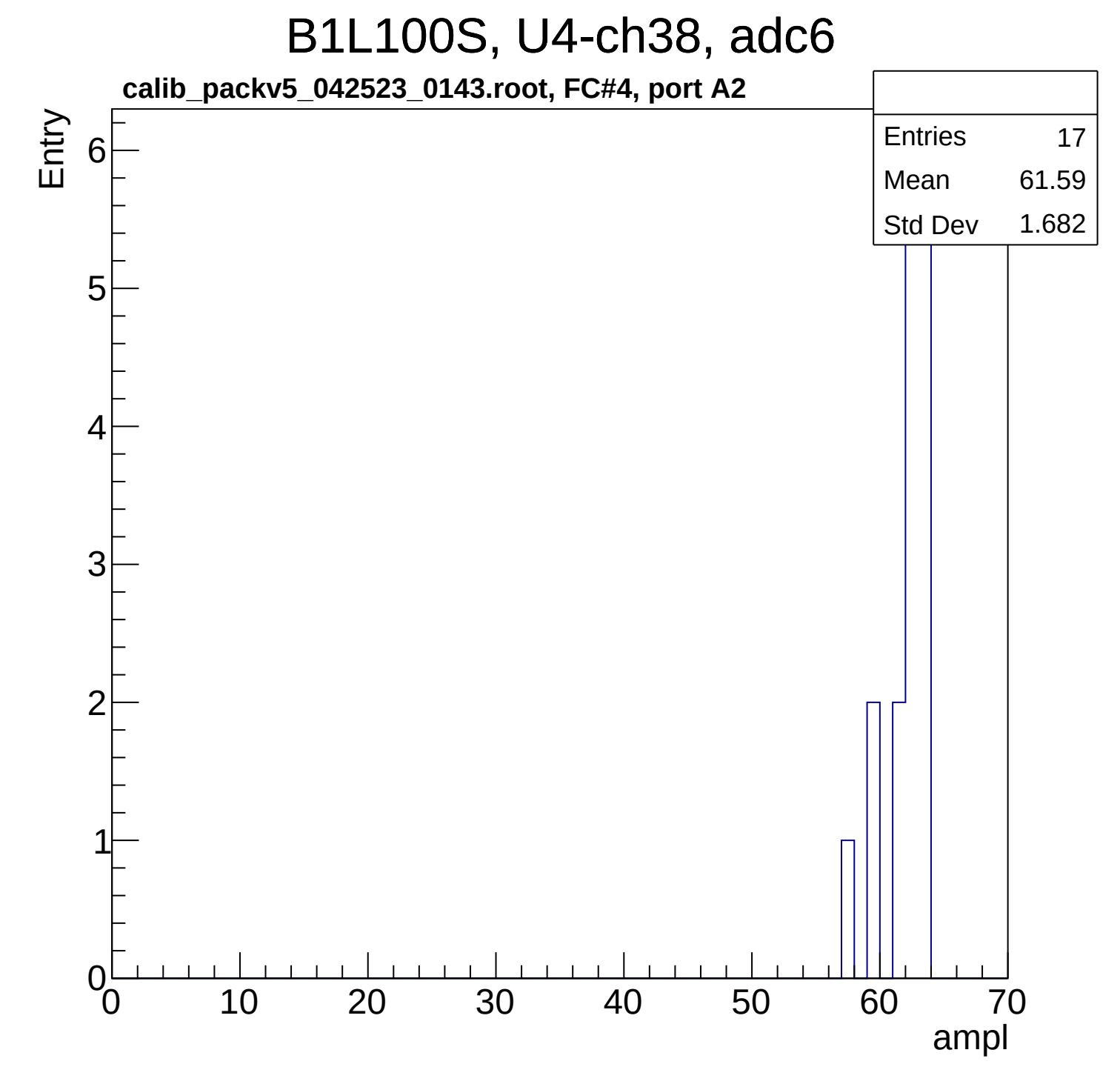

B1L100S, U4-ch38, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 35
Std Dev 3.595
Gaus mean : 35.5013
Gaus Width: 3.9343
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

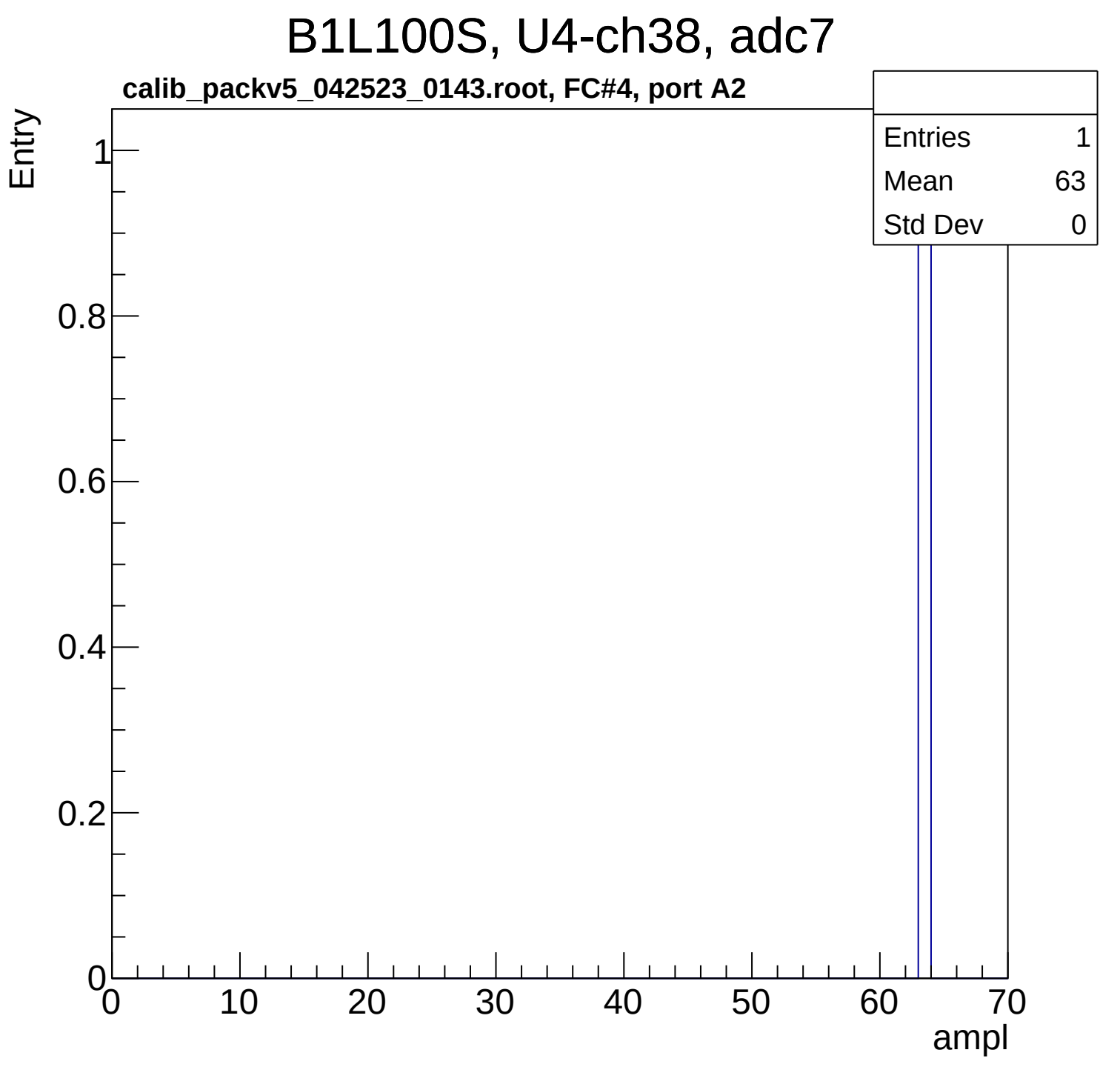

B1L100S, U4-ch38, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 45
Mean 41.38
Std Dev 3.485
Gaus mean : 41.4610
Gaus Width: 3.7458
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

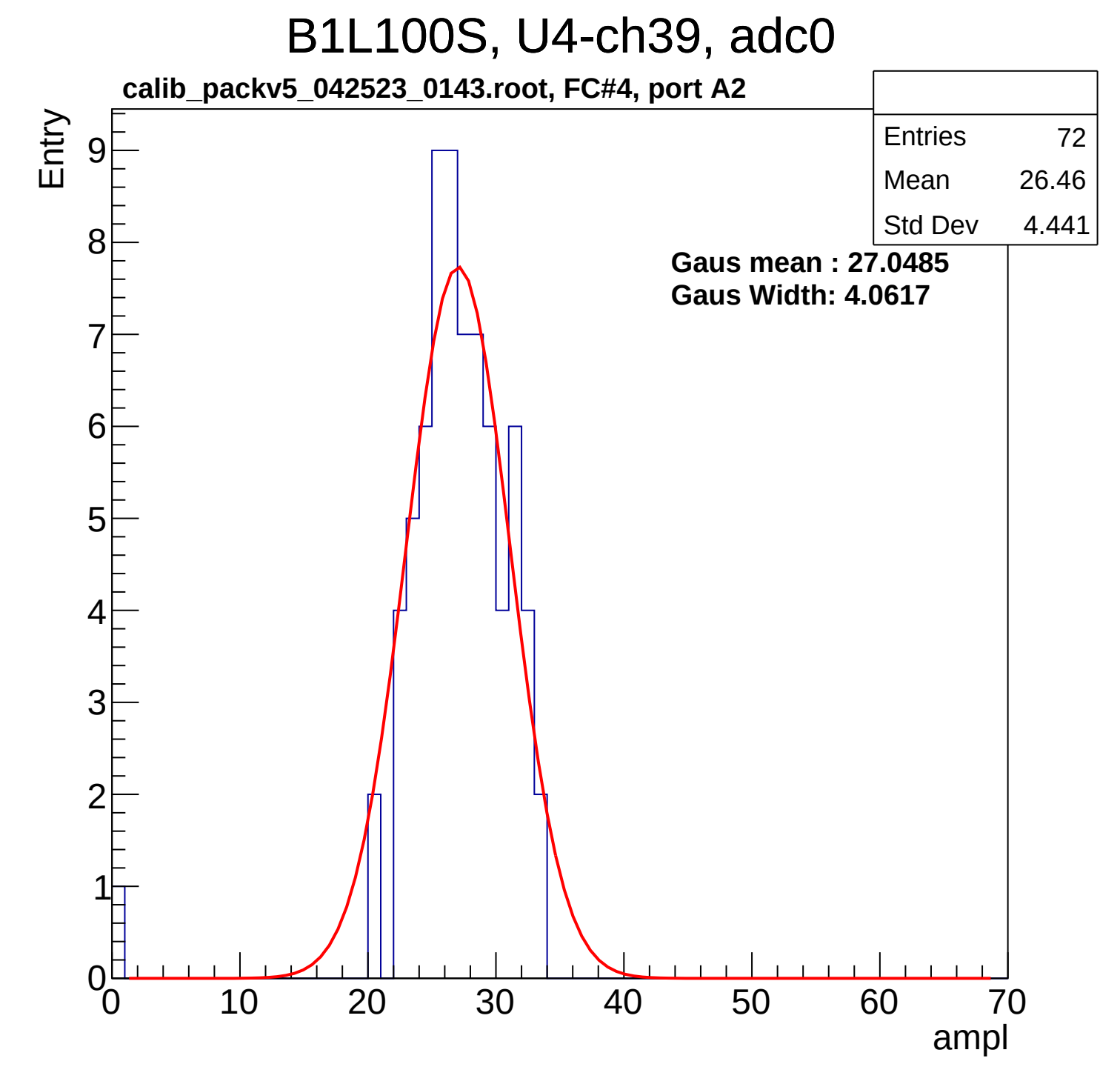

B1L100S, U4-ch38, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 46.39
Std Dev 3.968
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

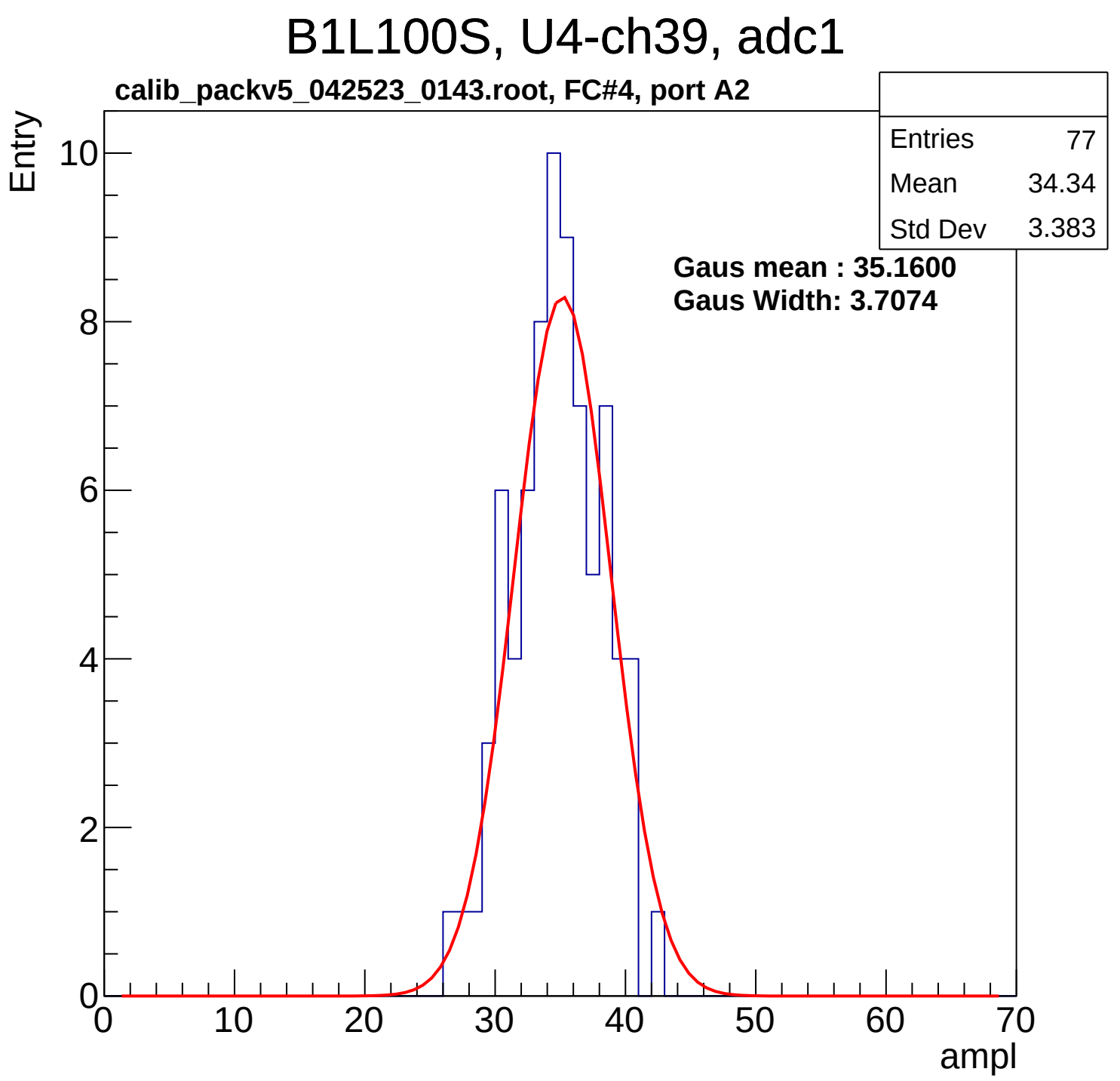

B1L100S, U4-ch38, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 53.95
Std Dev 3.071
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

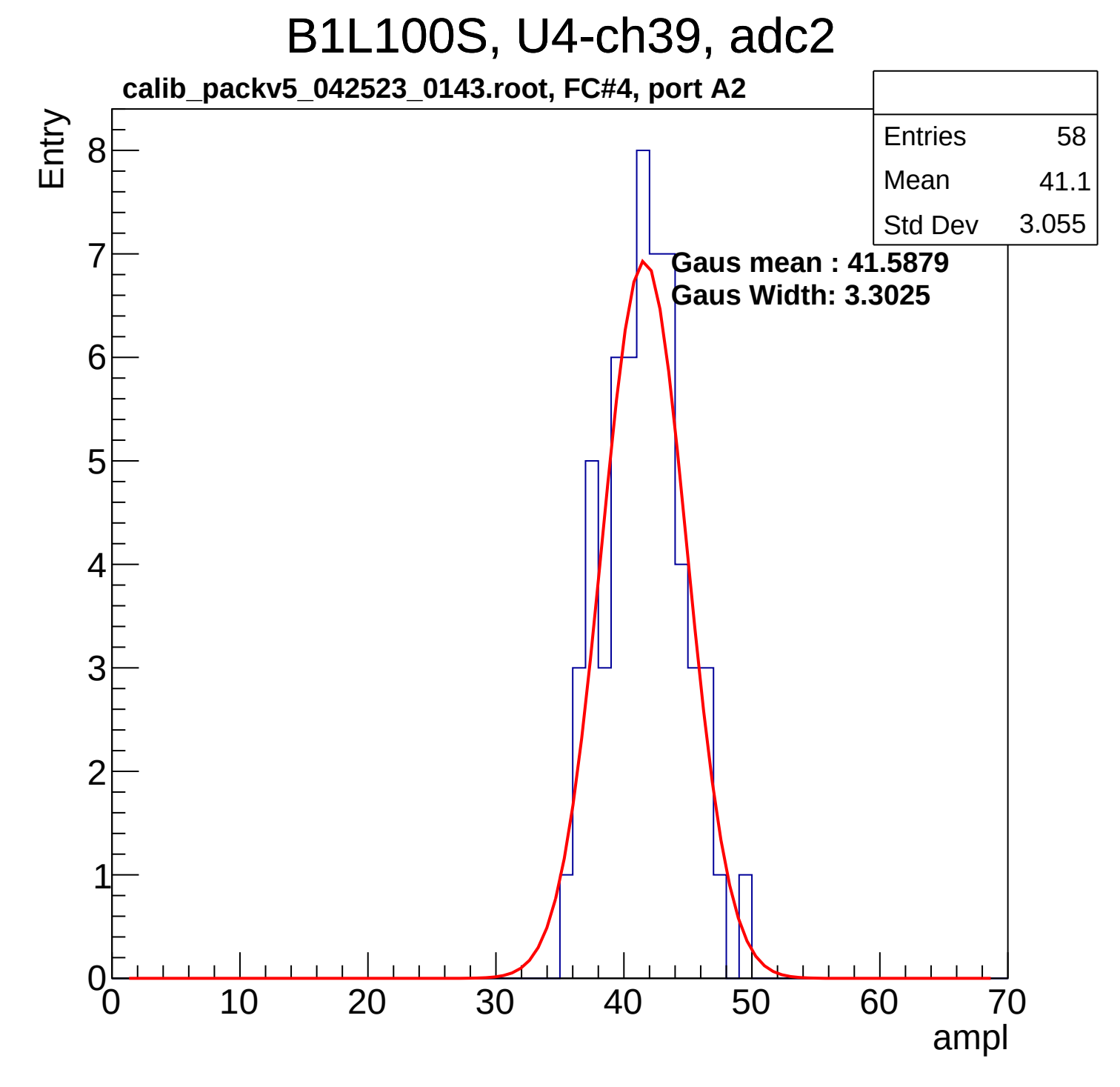

B1L100S, U4-ch38, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 57.51
Std Dev 8.795
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

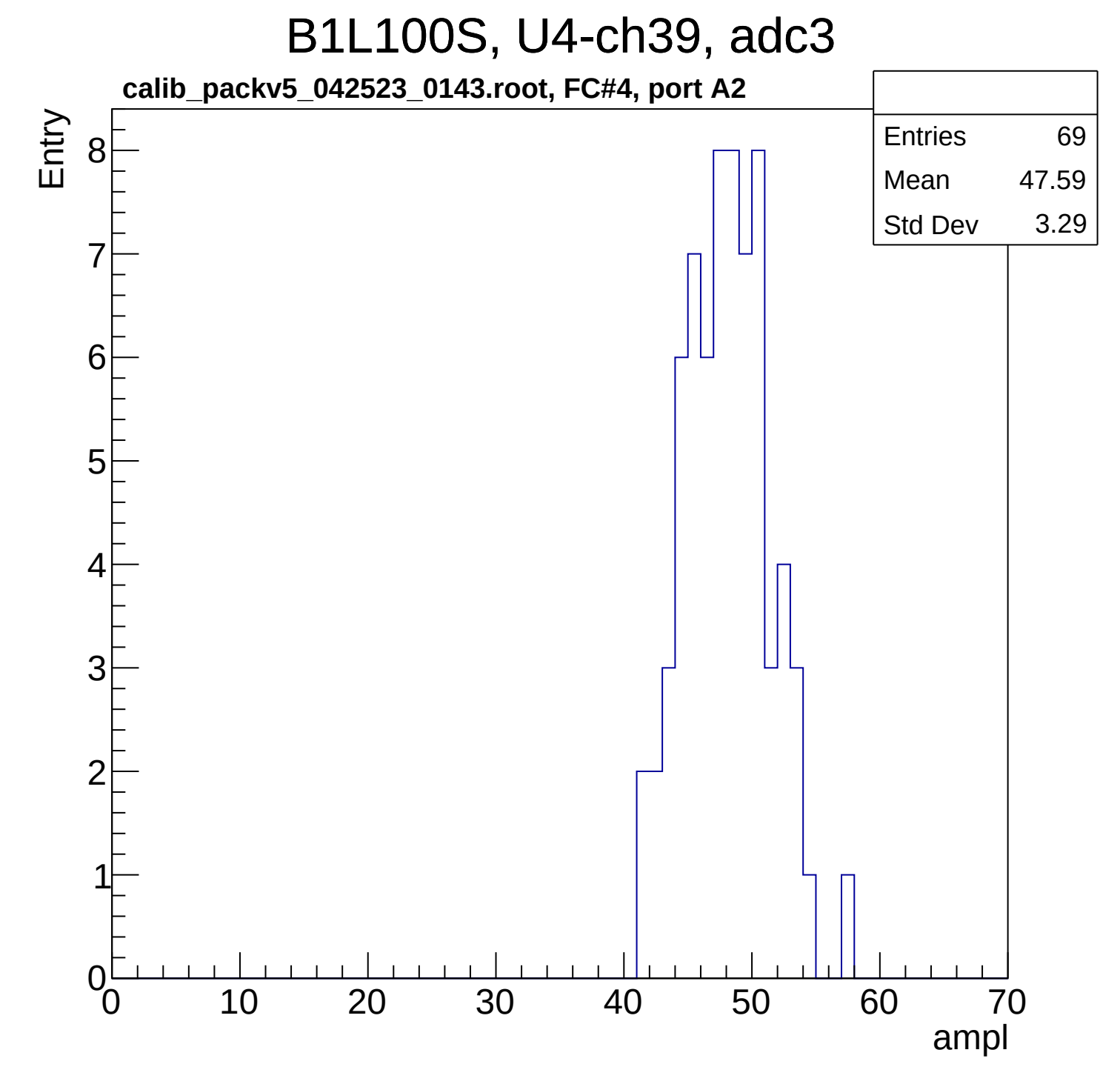

B1L100S, U4-ch38, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 17
Mean 61.59
Std Dev 1.682
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

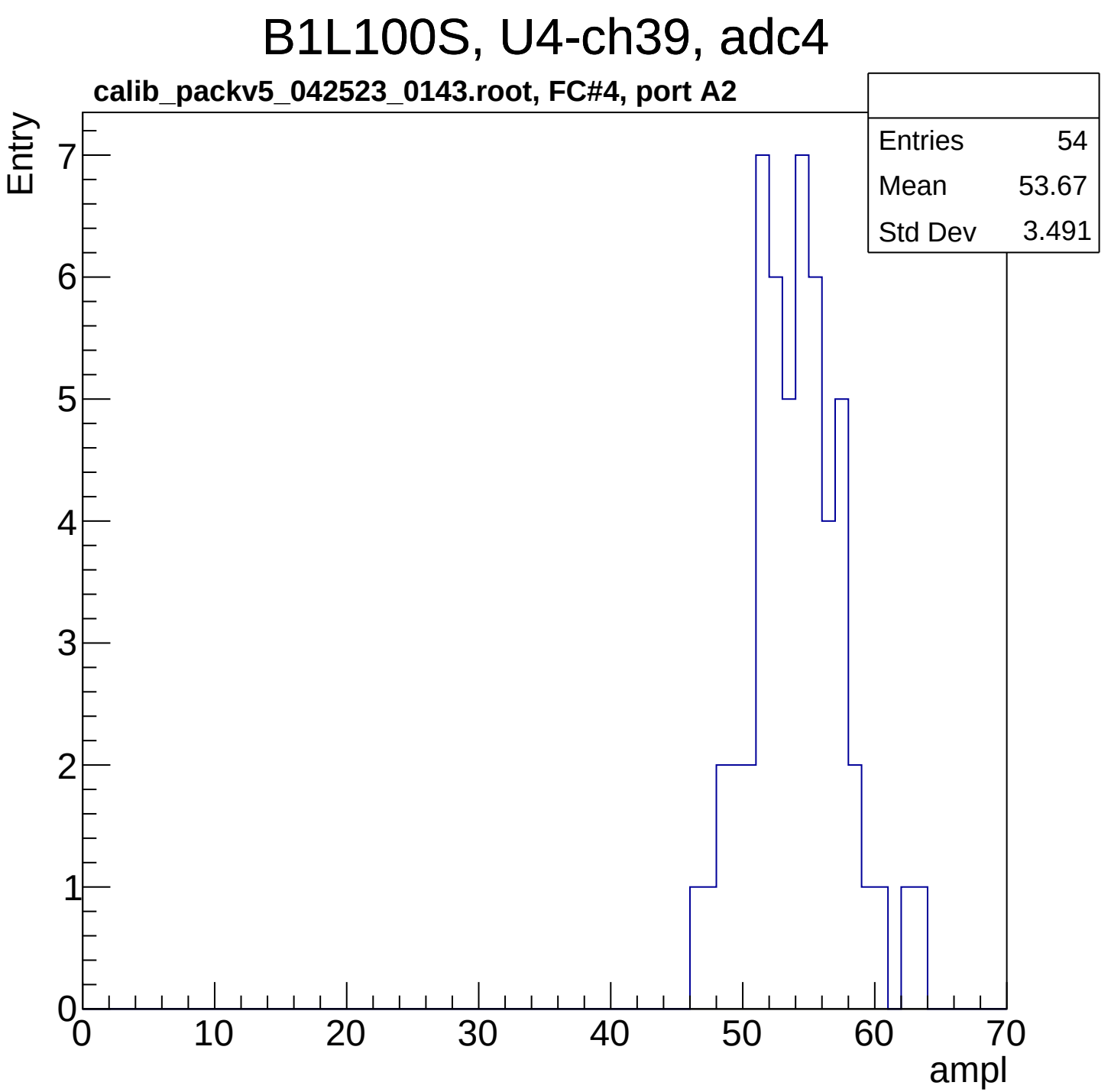

B1L100S, U4-ch38, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

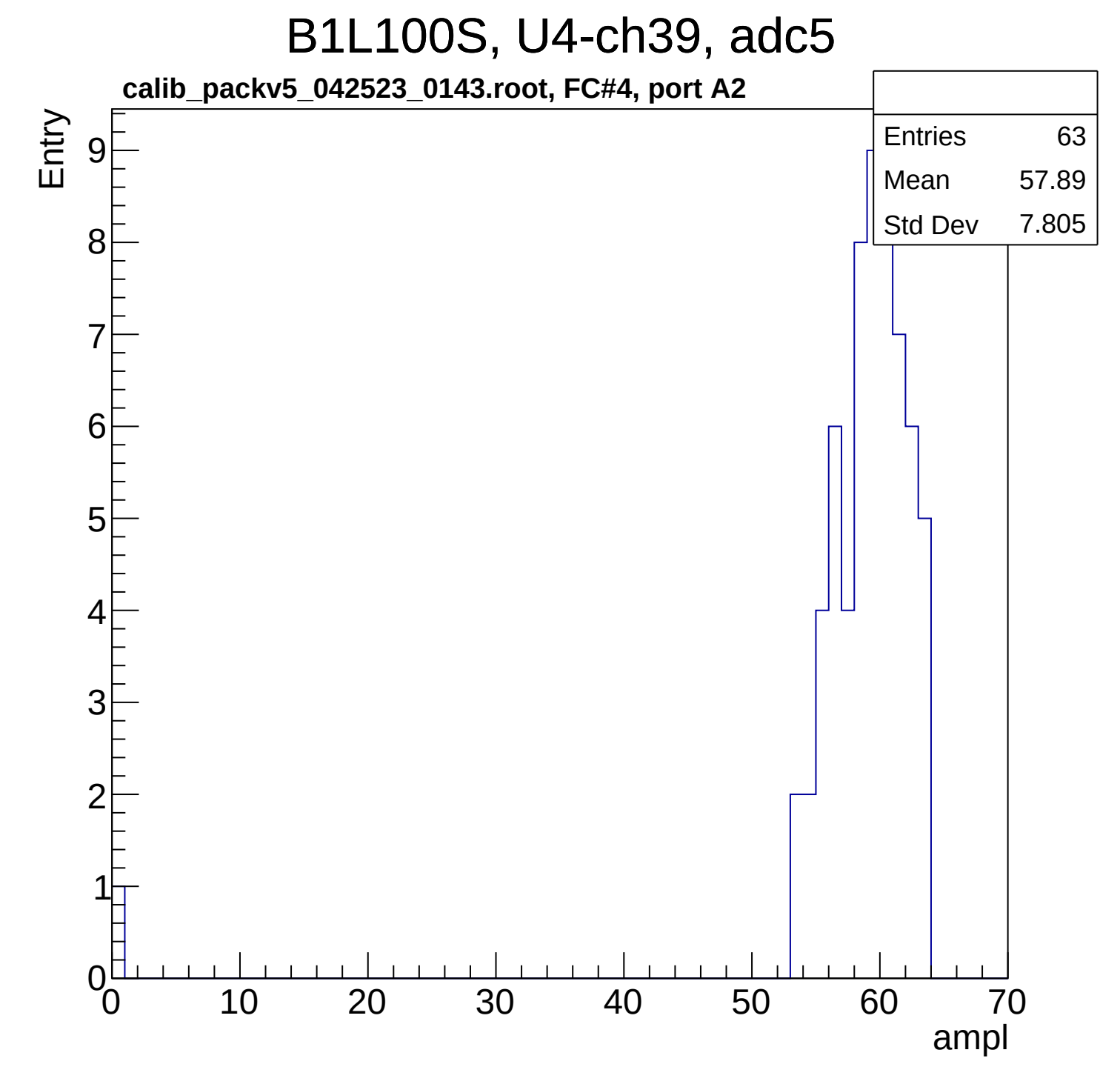

B1L100S, U4-ch39, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 26.46
Std Dev 4.441
Gaus mean : 27.0485
Gaus Width: 4.0617
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

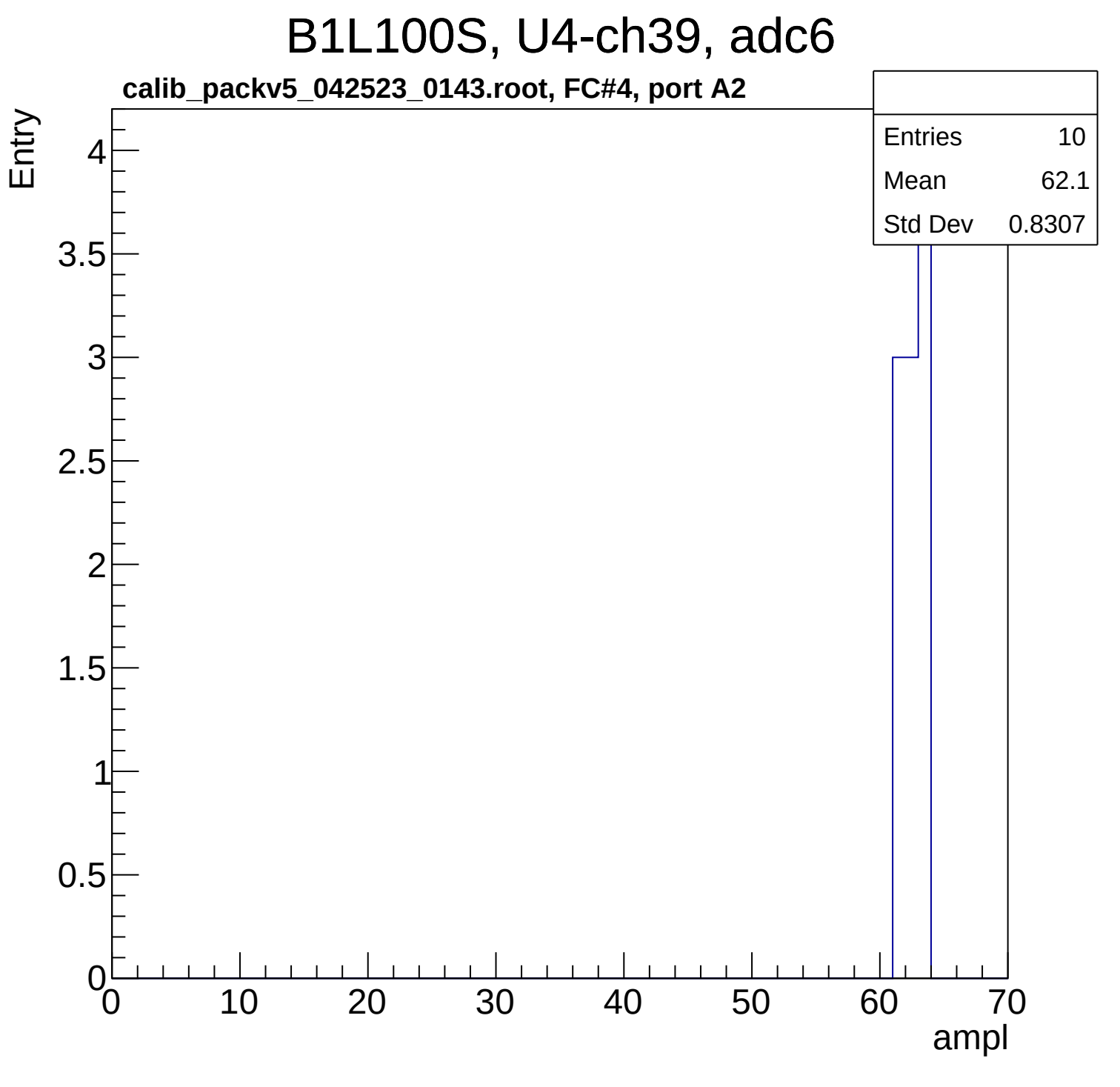

B1L100S, U4-ch39, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 34.34
Std Dev 3.383
Gaus mean : 35.1600
Gaus Width: 3.7074
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

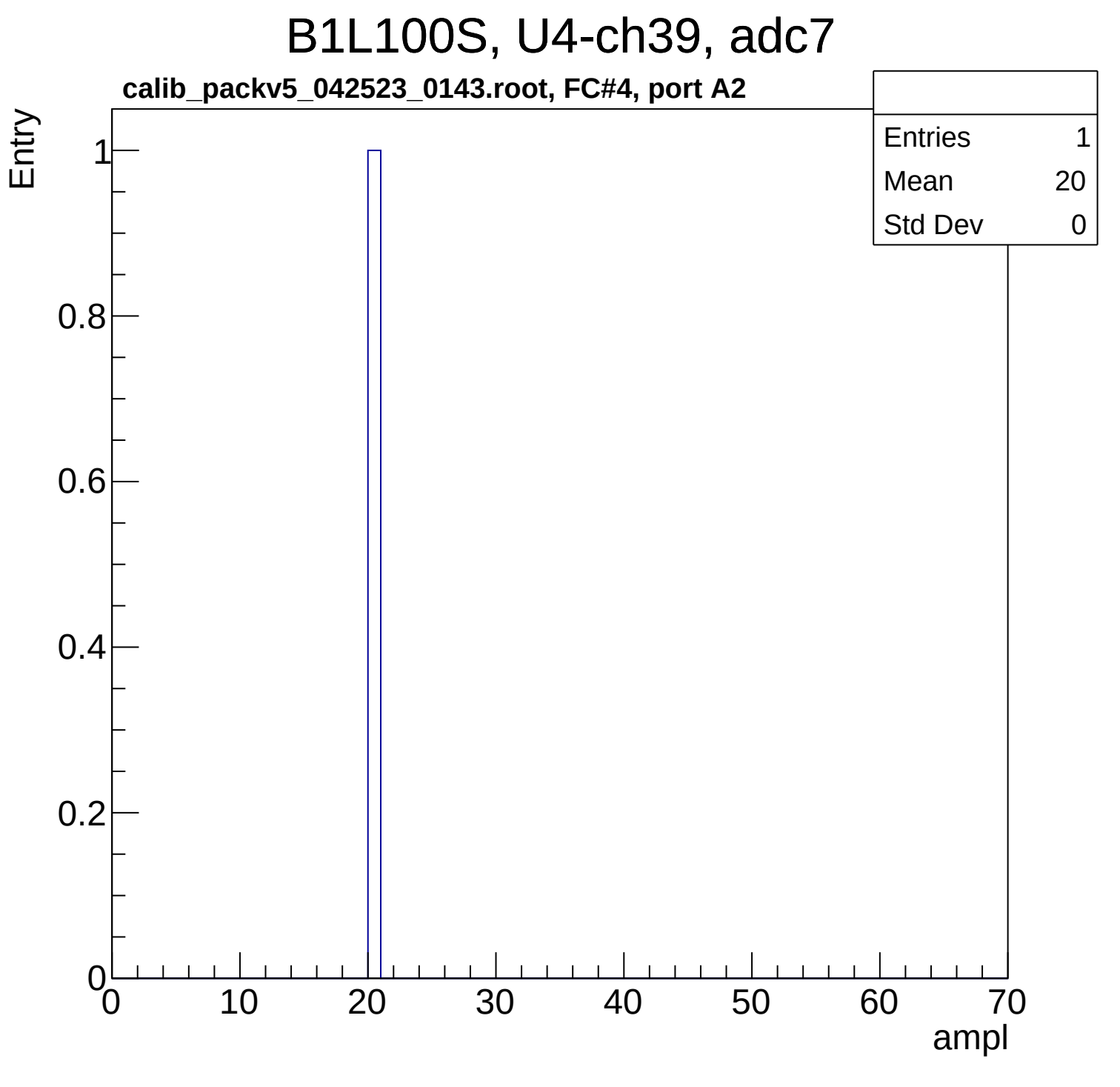

B1L100S, U4-ch39, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 41.1
Std Dev 3.055
Gaus mean : 41.5879
Gaus Width: 3.3025
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

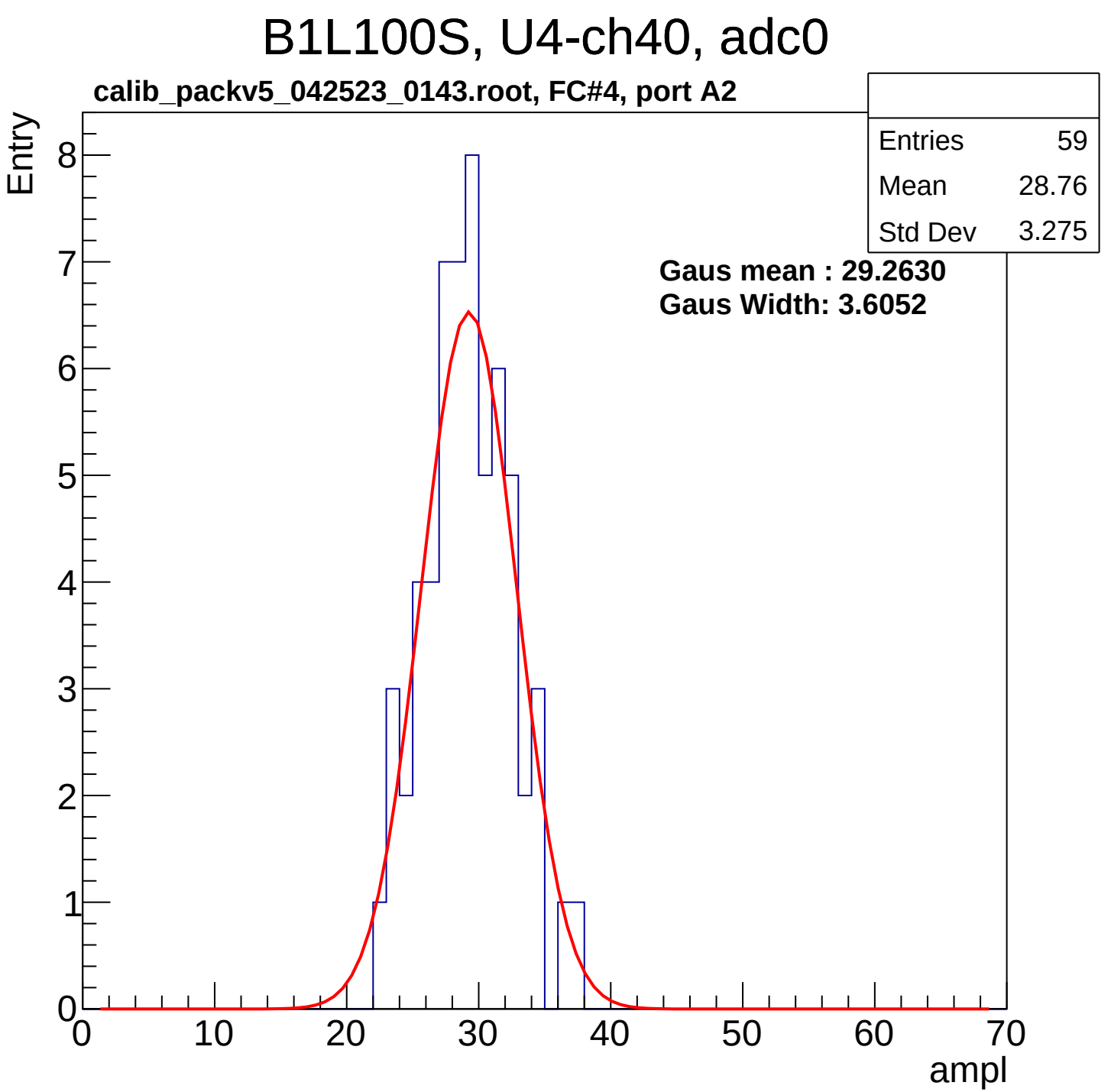

B1L100S, U4-ch39, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 47.59
Std Dev 3.29
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

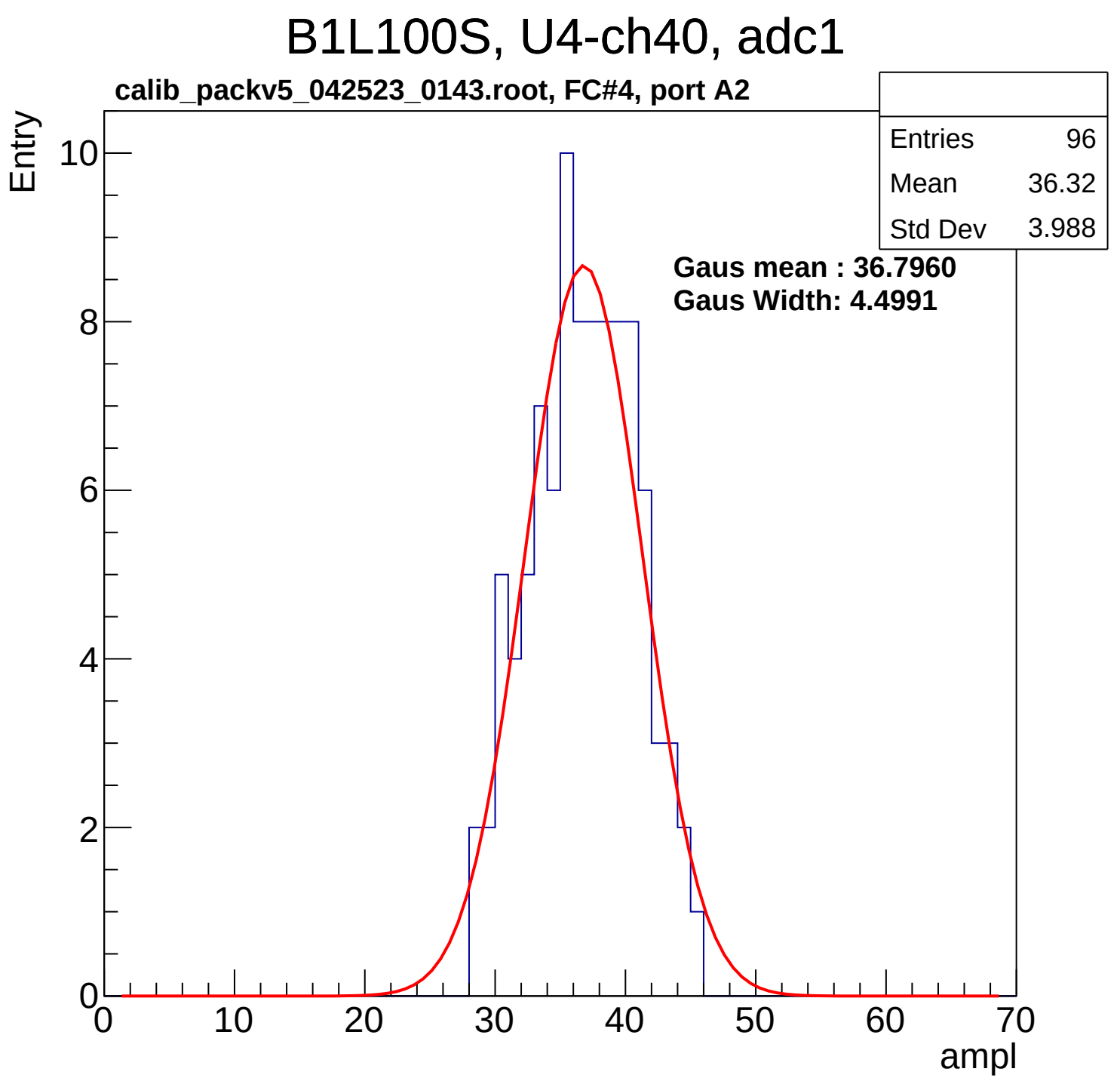

B1L100S, U4-ch39, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 53.67
Std Dev 3.491
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

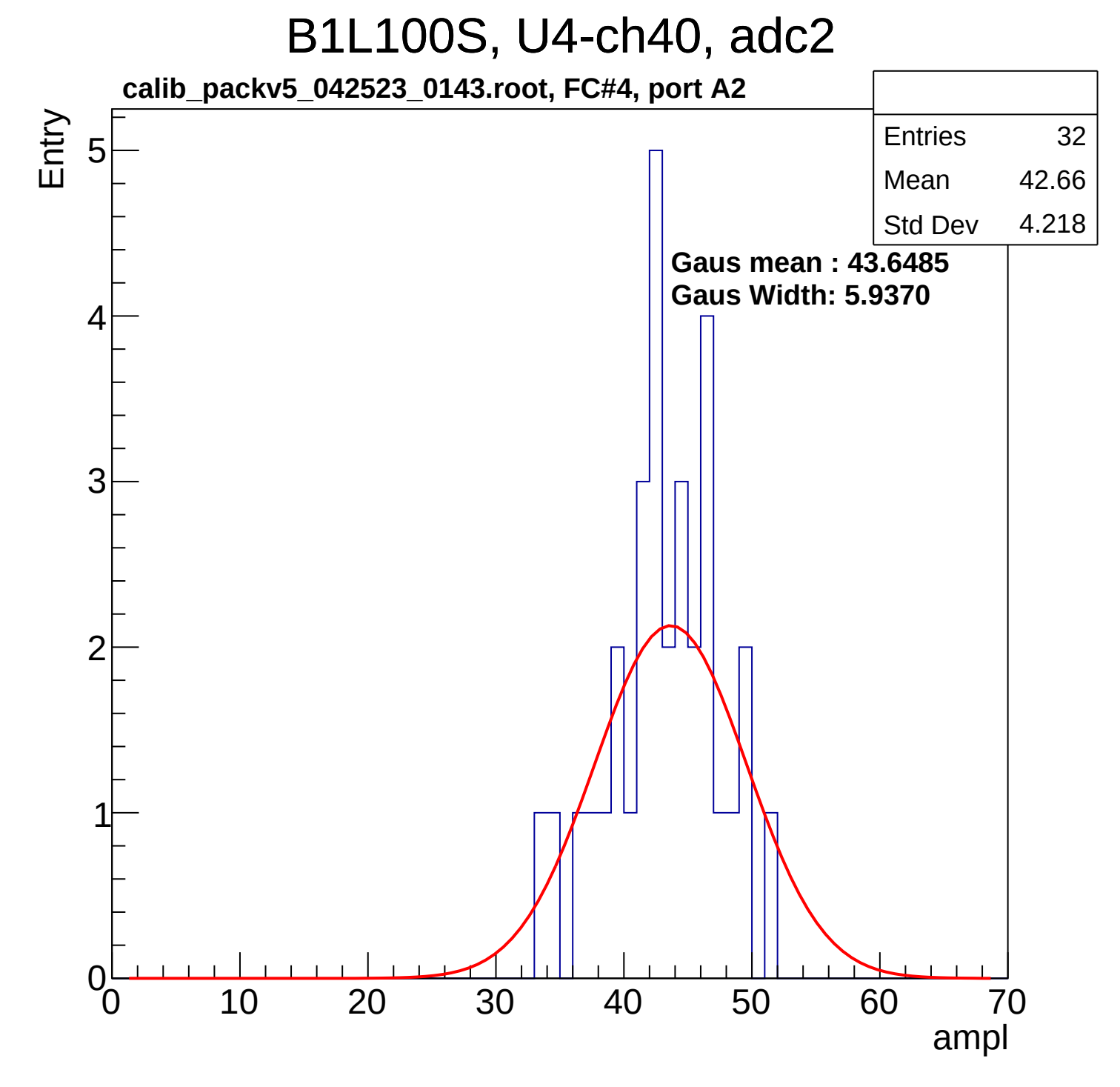

B1L100S, U4-ch39, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 57.89
Std Dev 7.805
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

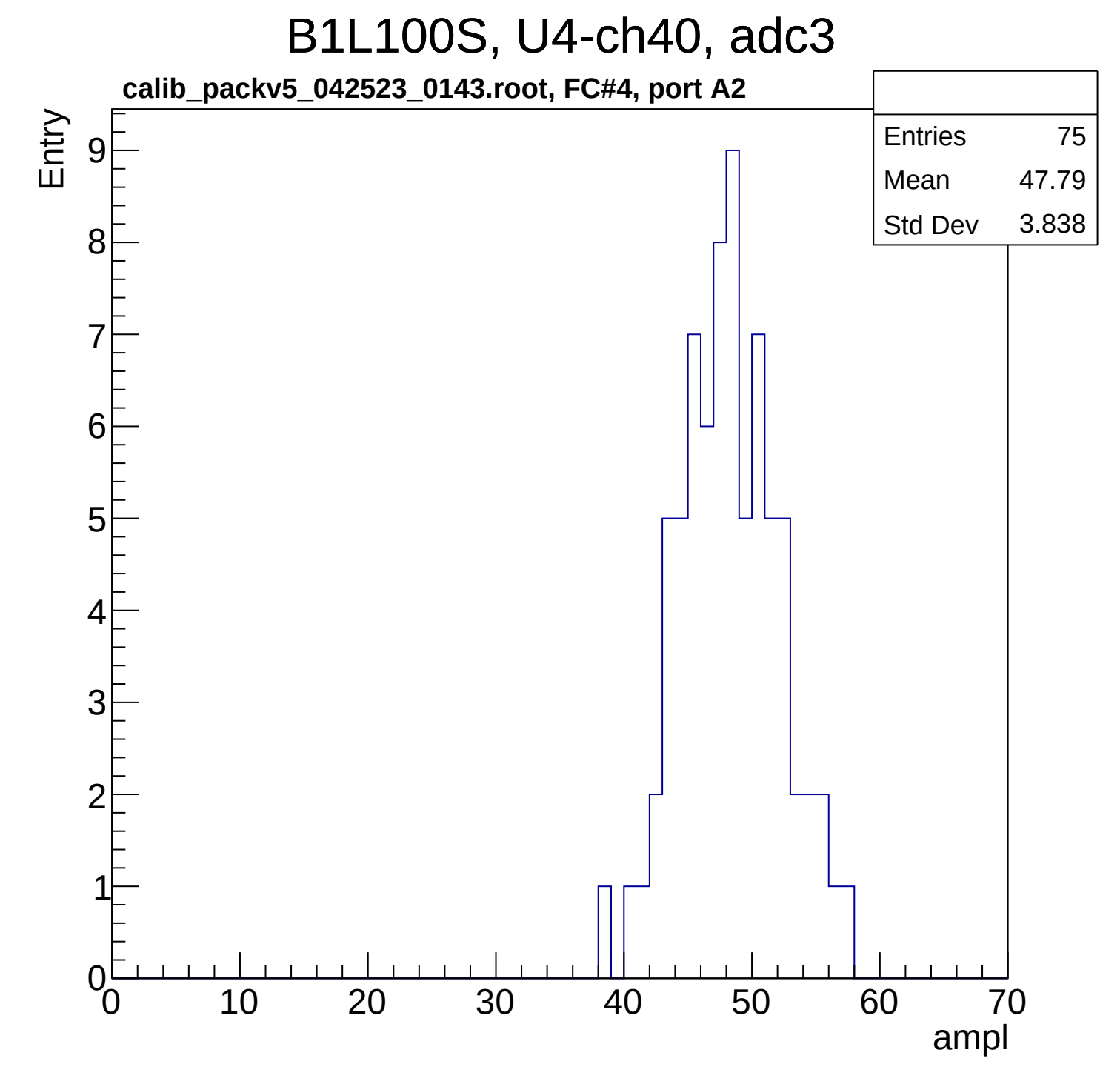

B1L100S, U4-ch39, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 62.1
Std Dev 0.8307
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

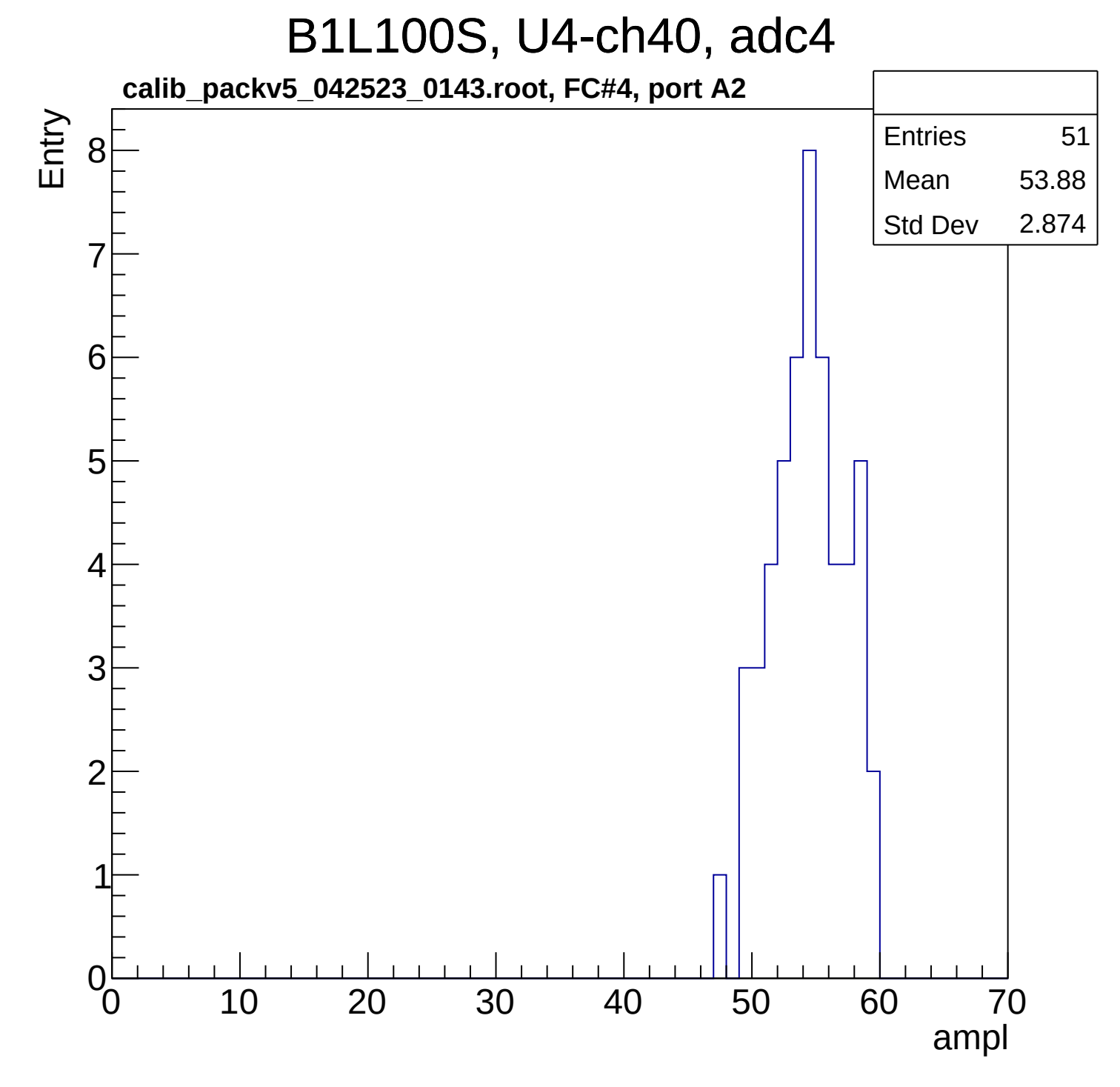

B1L100S, U4-ch39, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 20
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

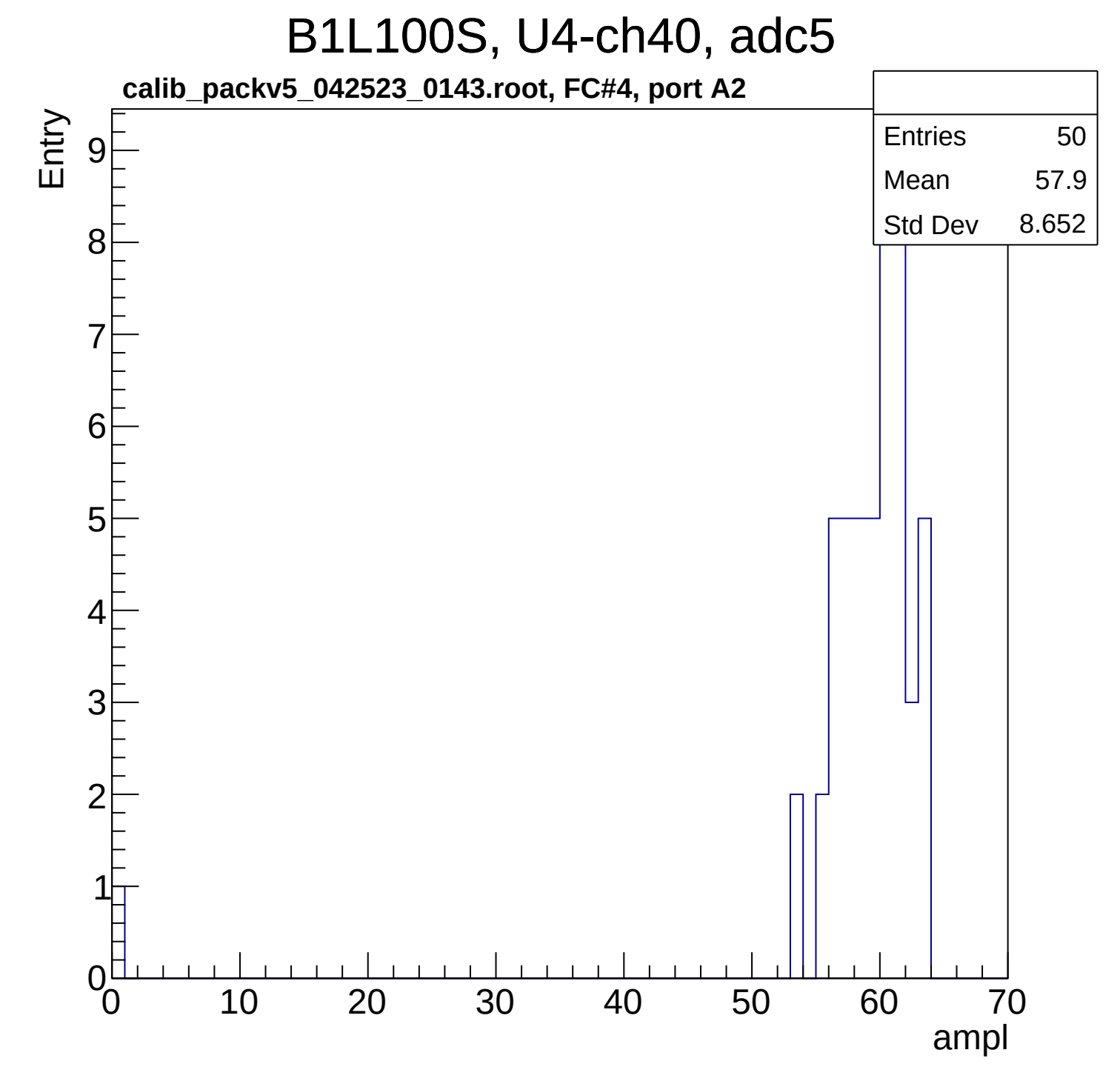

B1L100S, U4-ch40, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 28.76
Std Dev 3.275
Gaus mean : 29.2630
Gaus Width: 3.6052
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

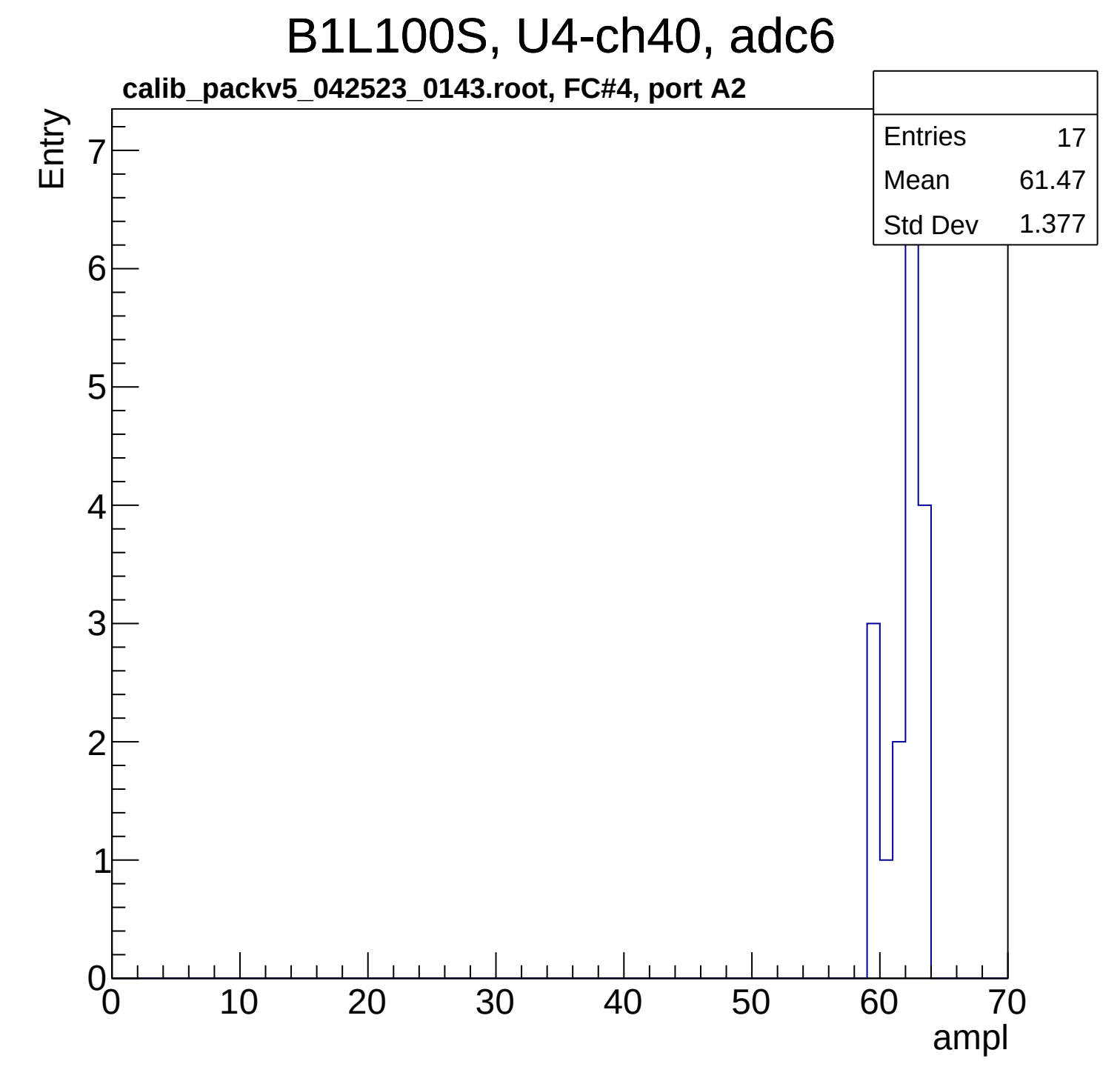

B1L100S, U4-ch40, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 96
Mean 36.32
Std Dev 3.988
Gaus mean : 36.7960
Gaus Width: 4.4991
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

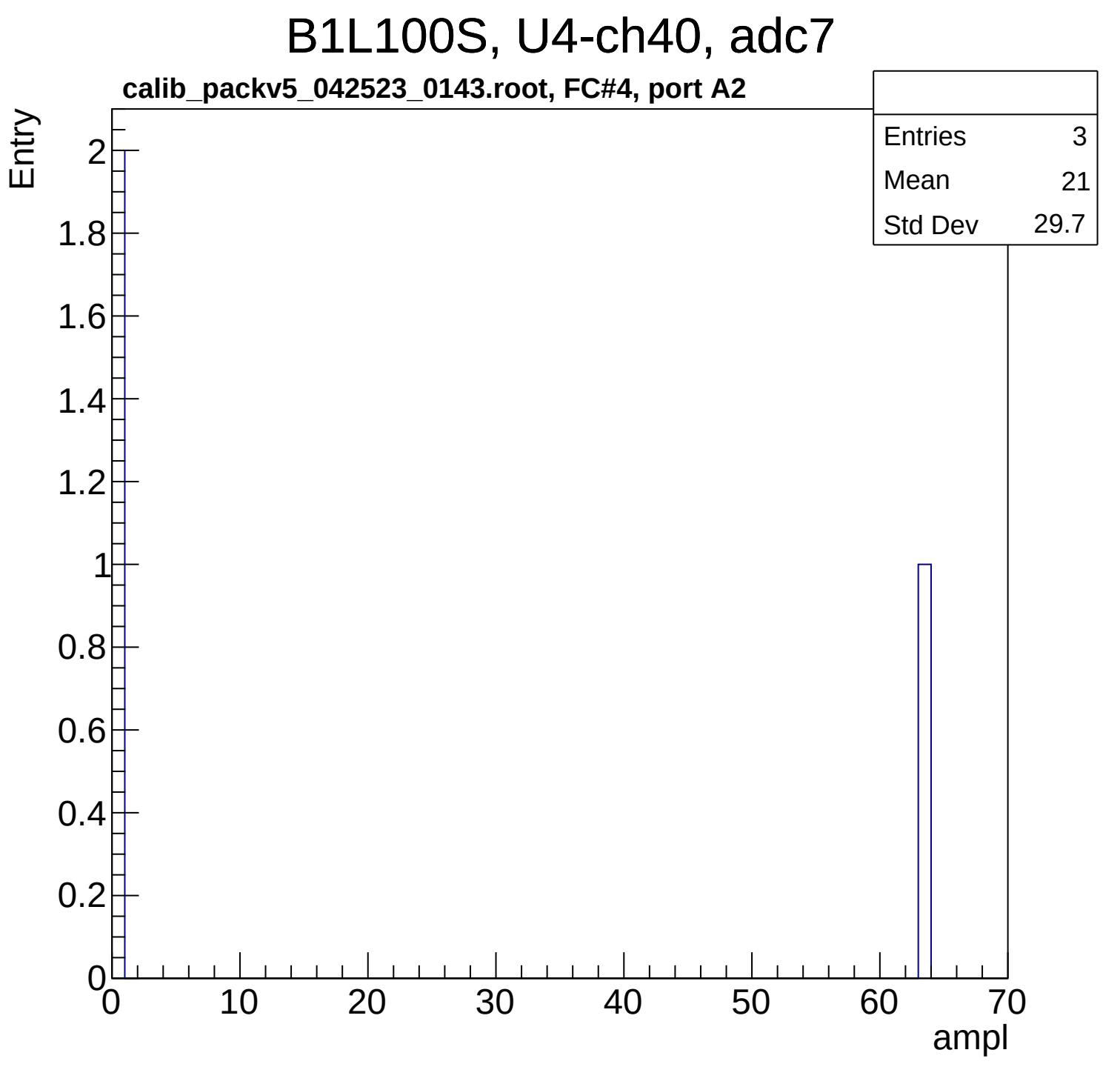

B1L100S, U4-ch40, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 32
Mean 42.66
Std Dev 4.218
Gaus mean : 43.6485
Gaus Width: 5.9370
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

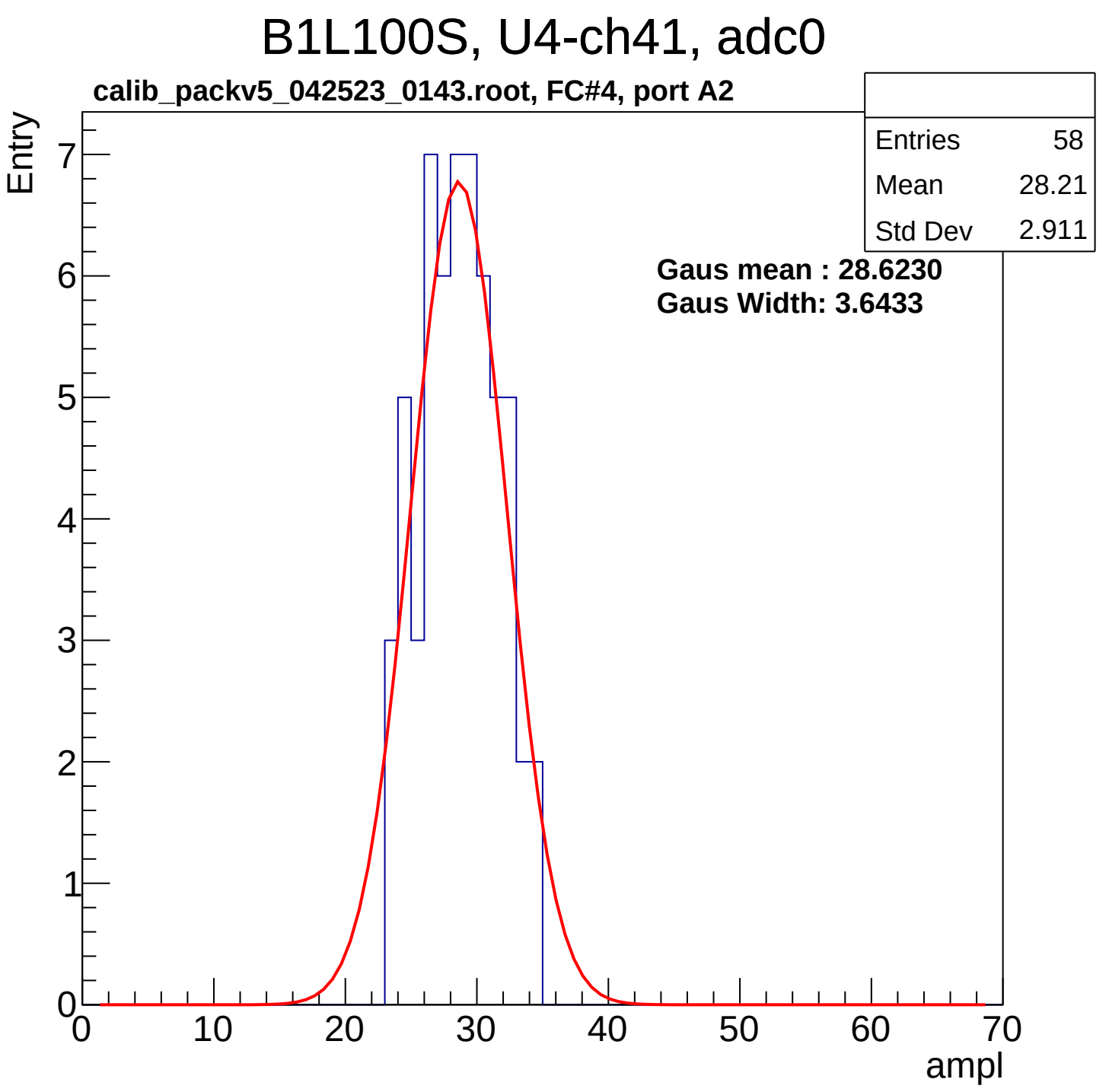

B1L100S, U4-ch40, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 47.79
Std Dev 3.838
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

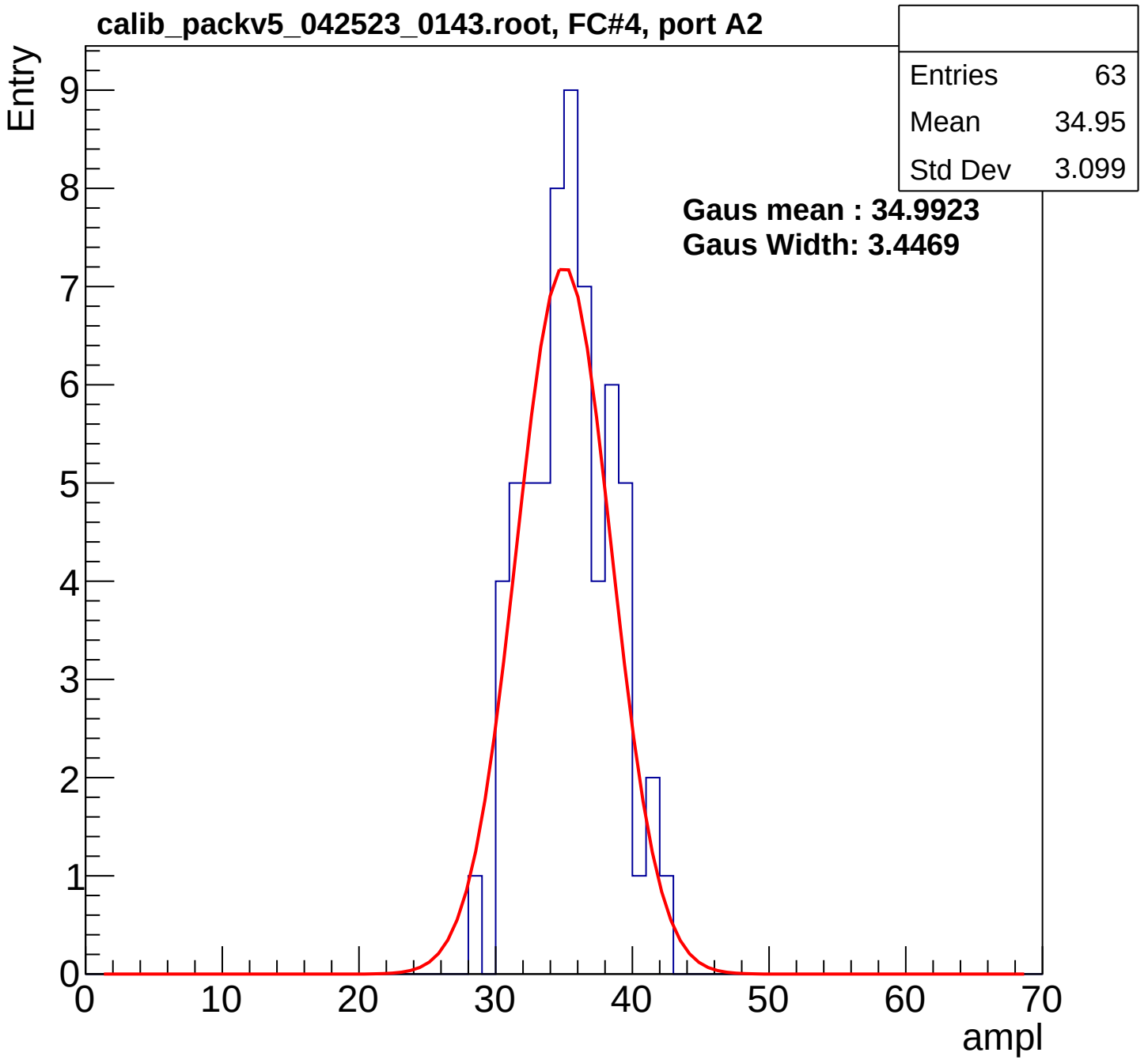

B1L100S, U4-ch40, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 53.88
Std Dev 2.874
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

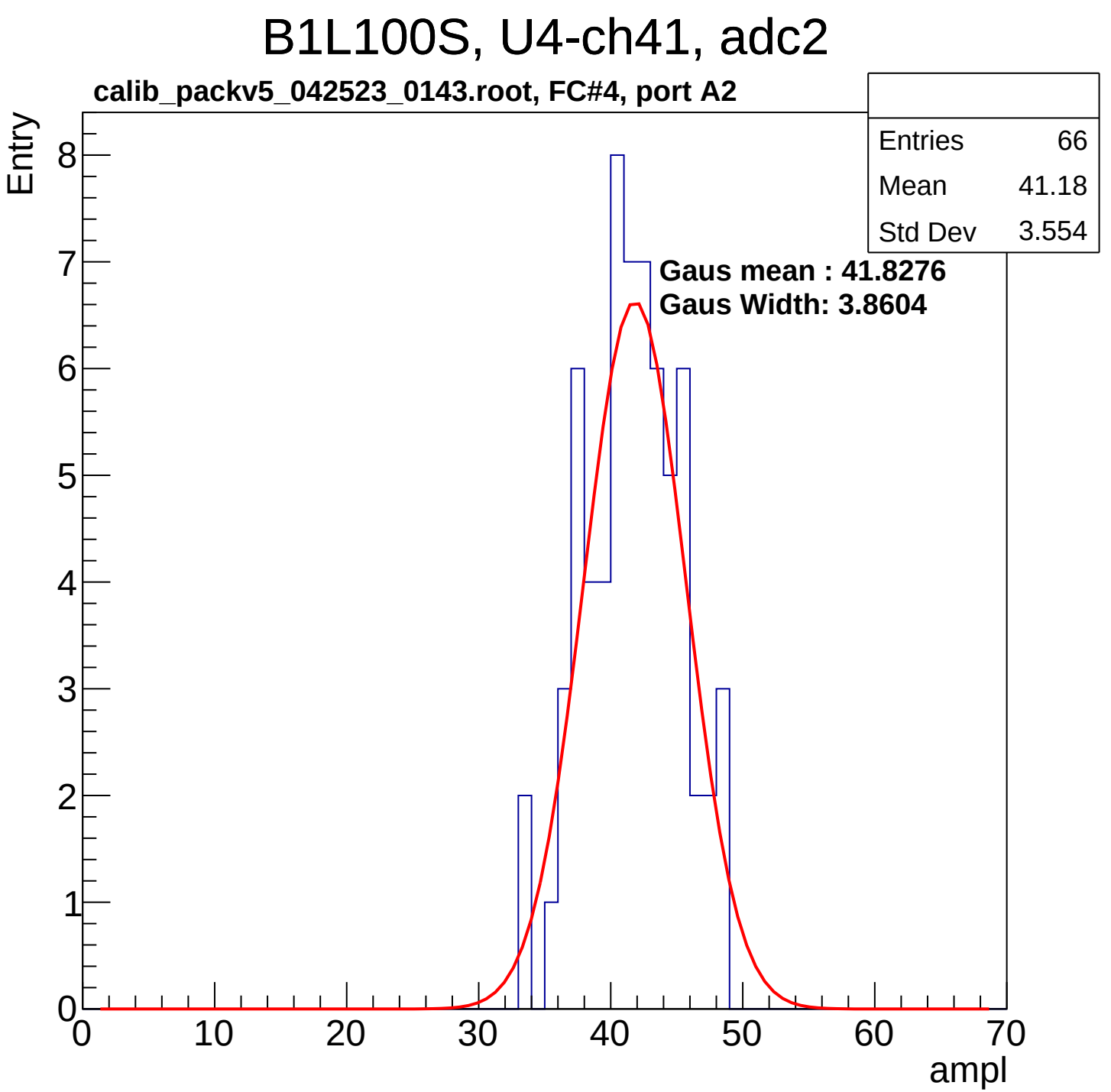

B1L100S, U4-ch40, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 57.9
Std Dev 8.652
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

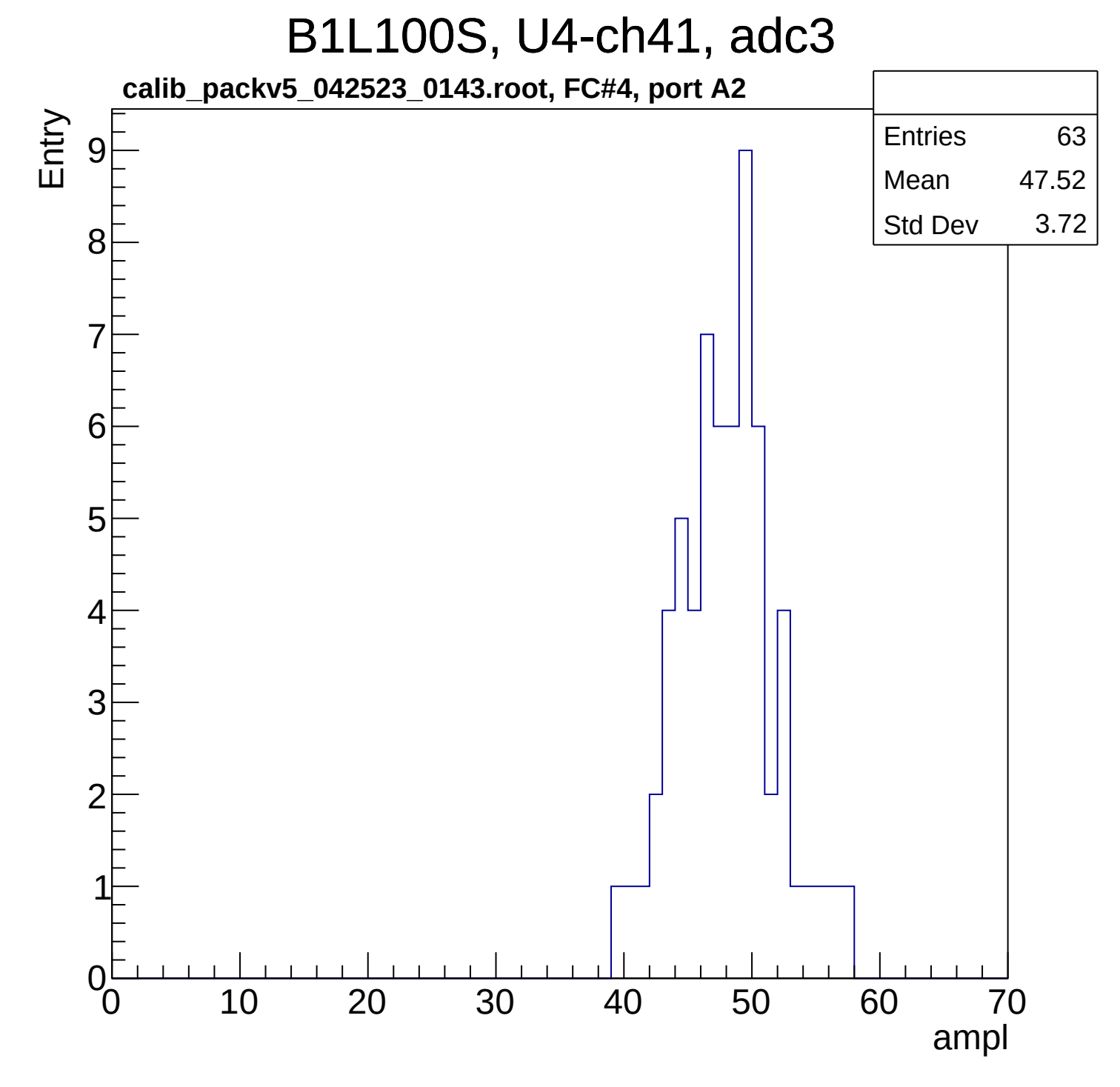

B1L100S, U4-ch40, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 17
Mean 61.47
Std Dev 1.377
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

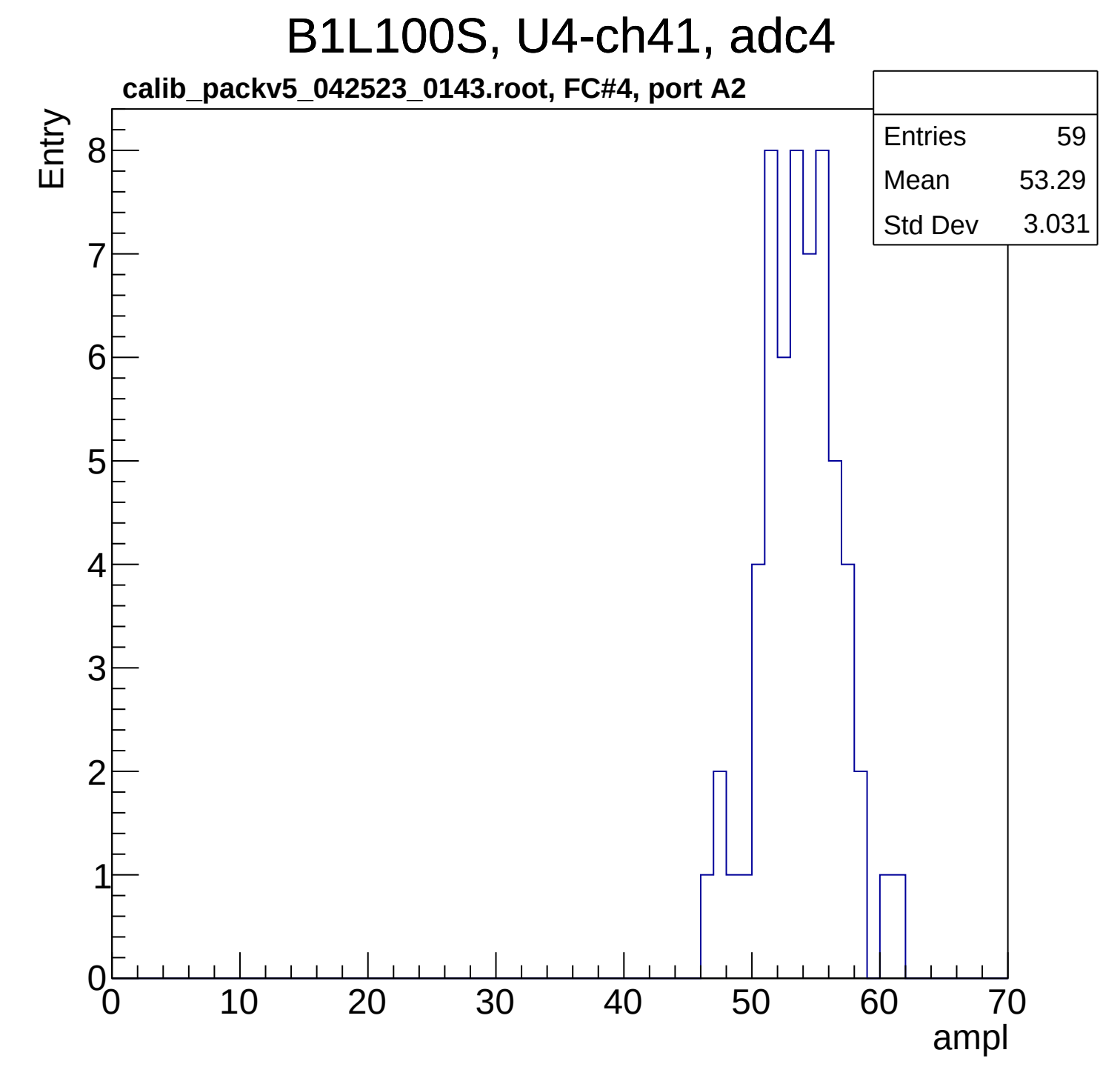

B1L100S, U4-ch40, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 21
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

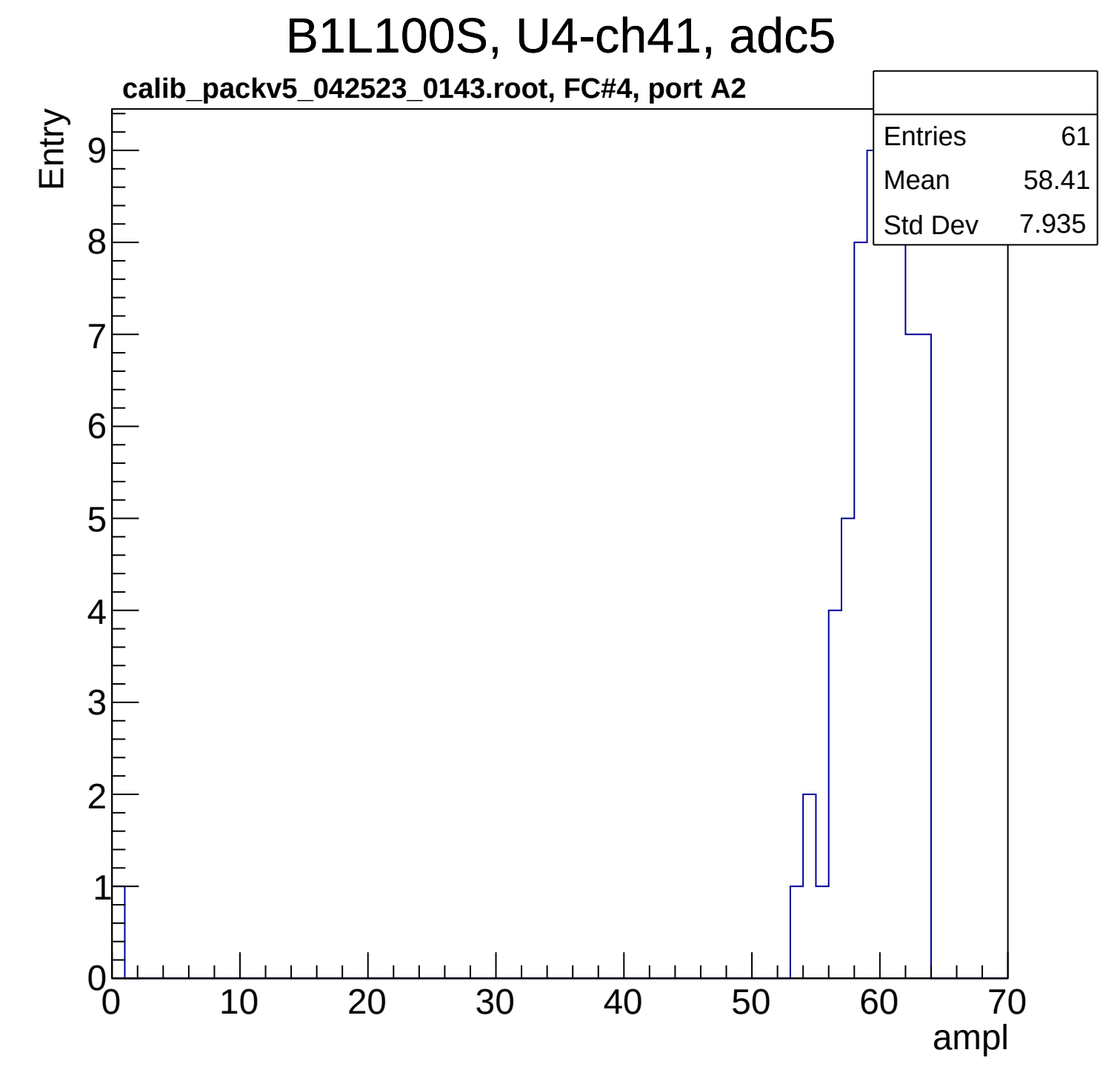

B1L100S, U4-ch41, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 28.21
Std Dev 2.911
Gaus mean : 28.6230
Gaus Width: 3.6433
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

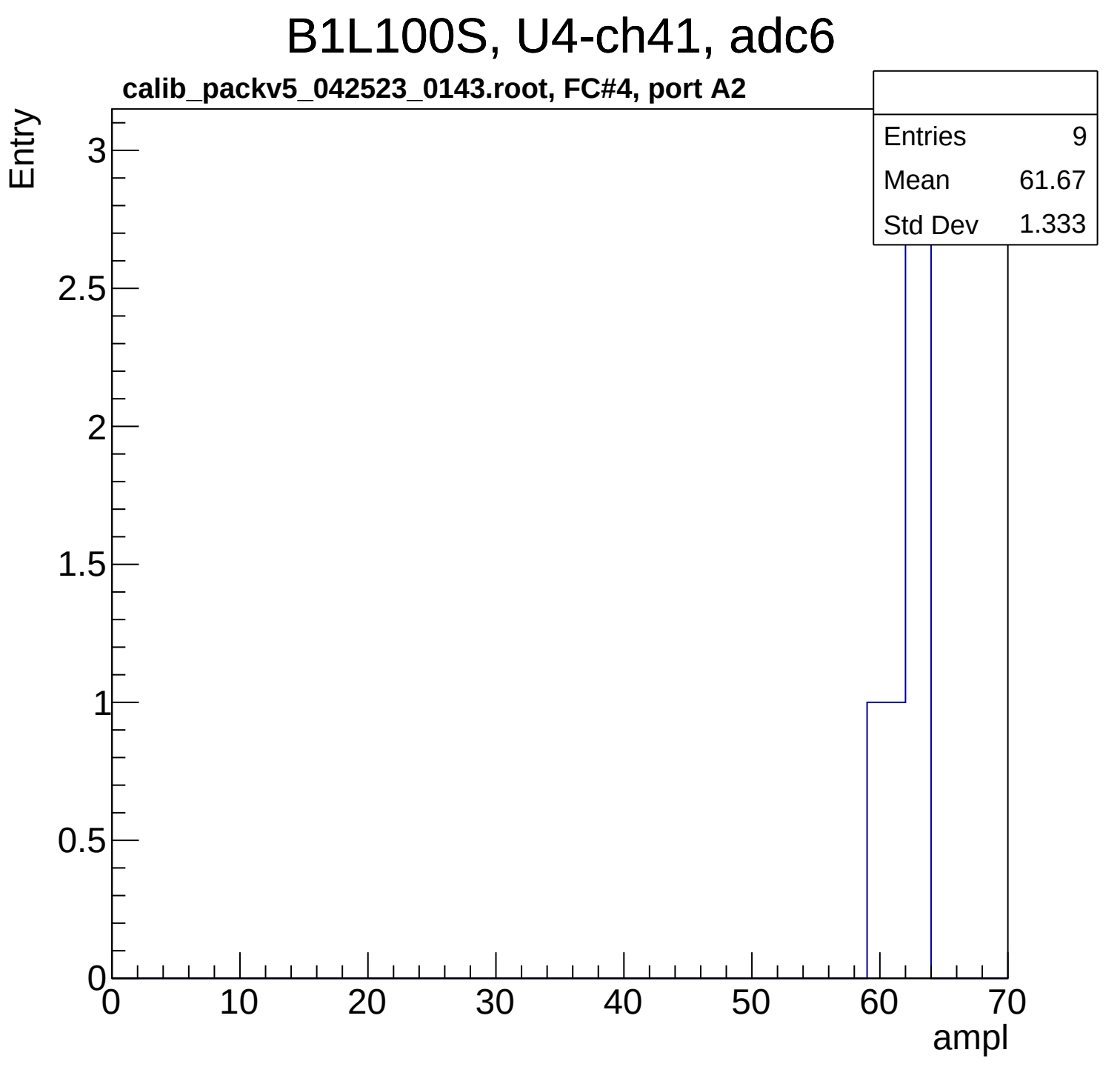

B1L100S, U4-ch41, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 34.95
Std Dev 3.099
Gaus mean : 34.9923
Gaus Width: 3.4469
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

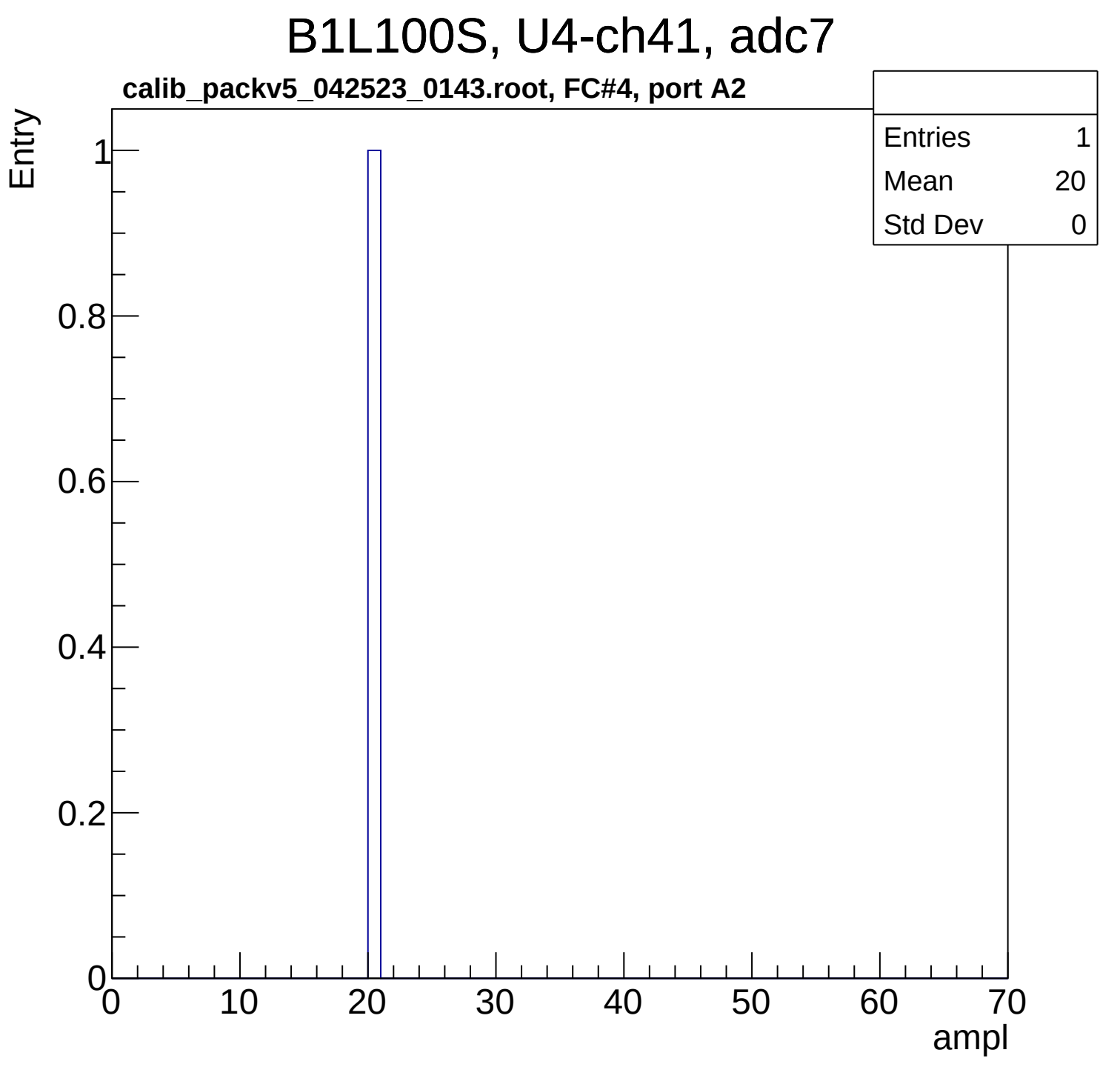

B1L100S, U4-ch41, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 41.18
Std Dev 3.554
Gaus mean : 41.8276
Gaus Width: 3.8604
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

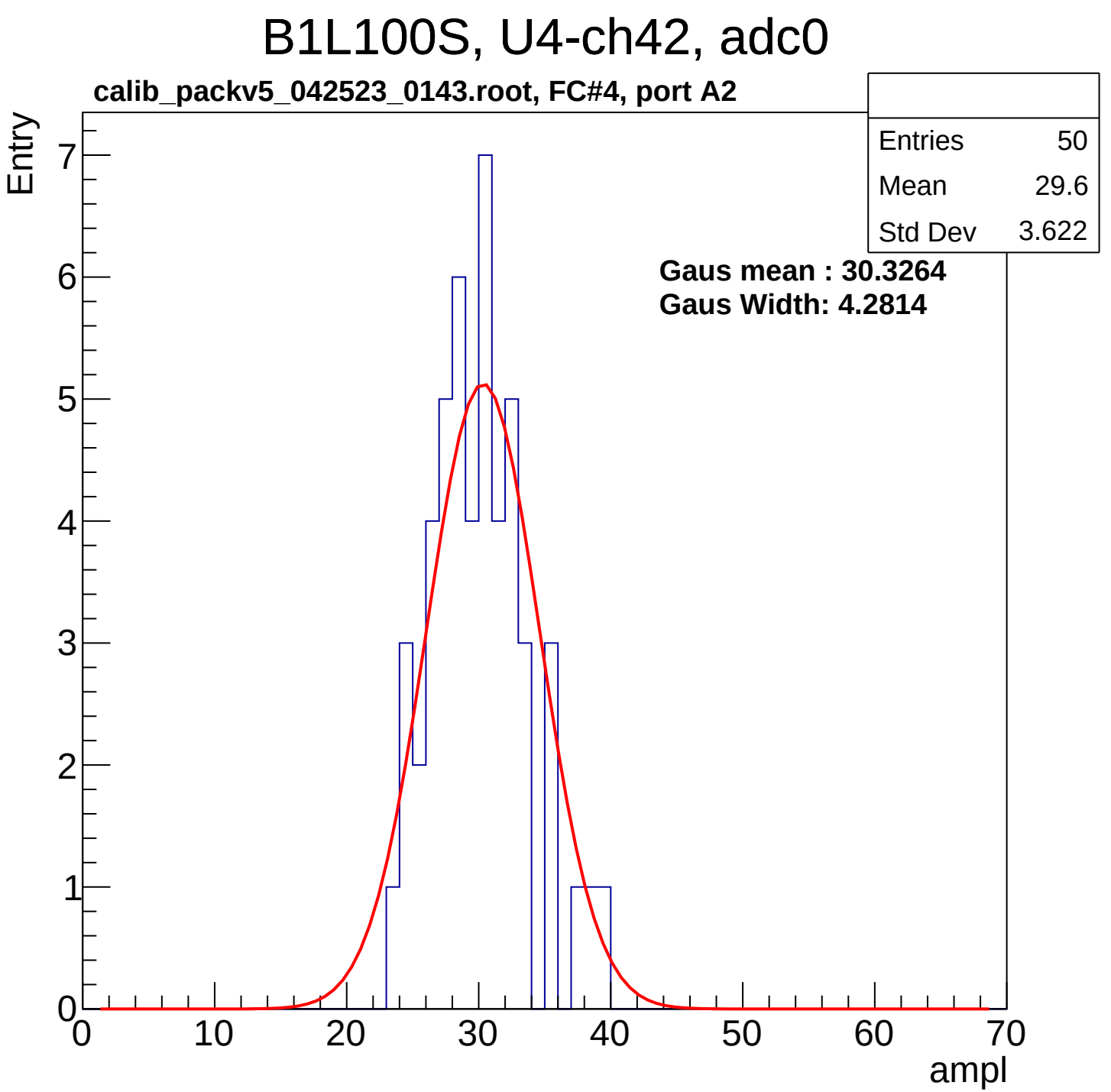

B1L100S, U4-ch41, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 47.52
Std Dev 3.72
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

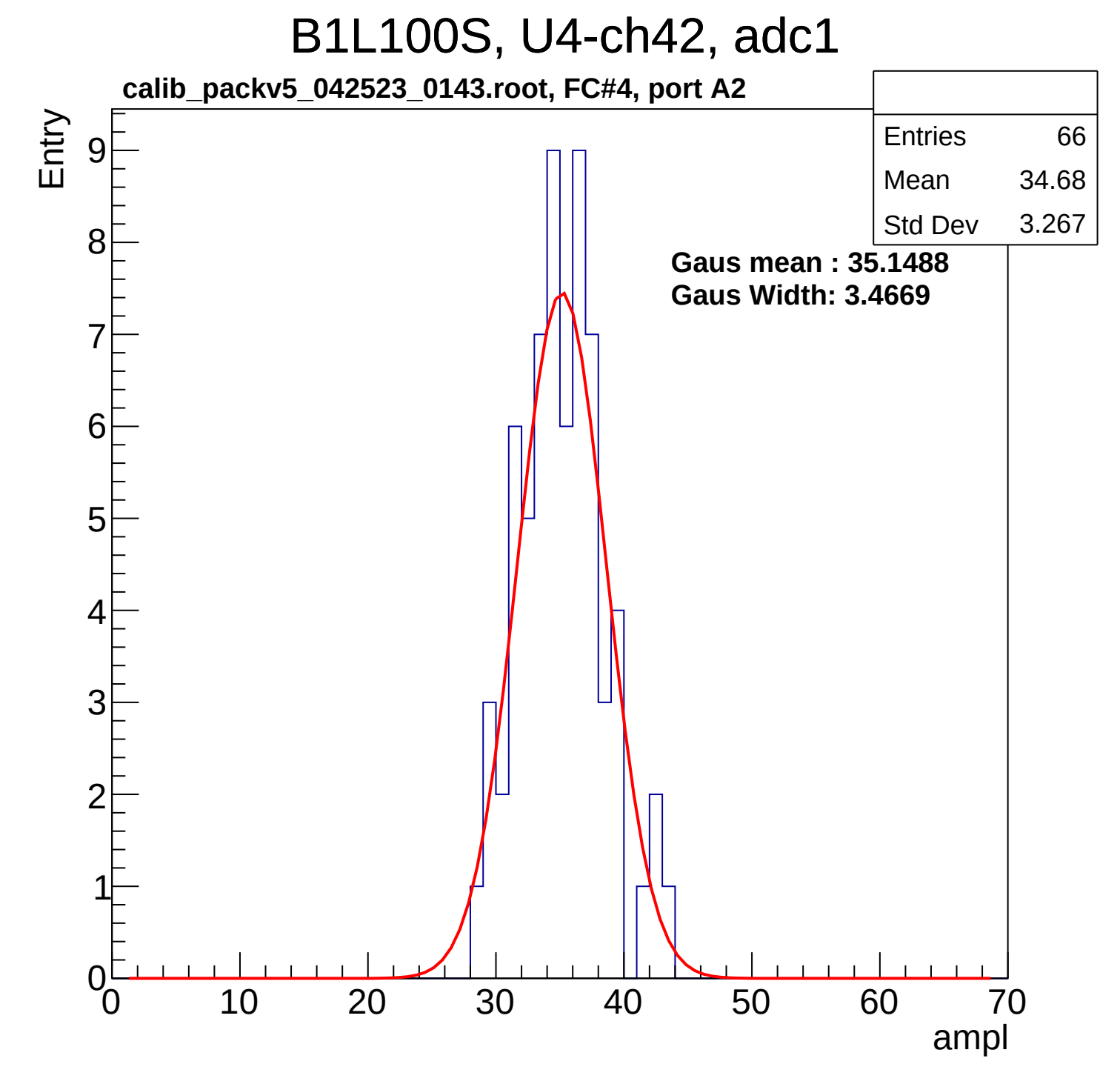

B1L100S, U4-ch41, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 53.29
Std Dev 3.031
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

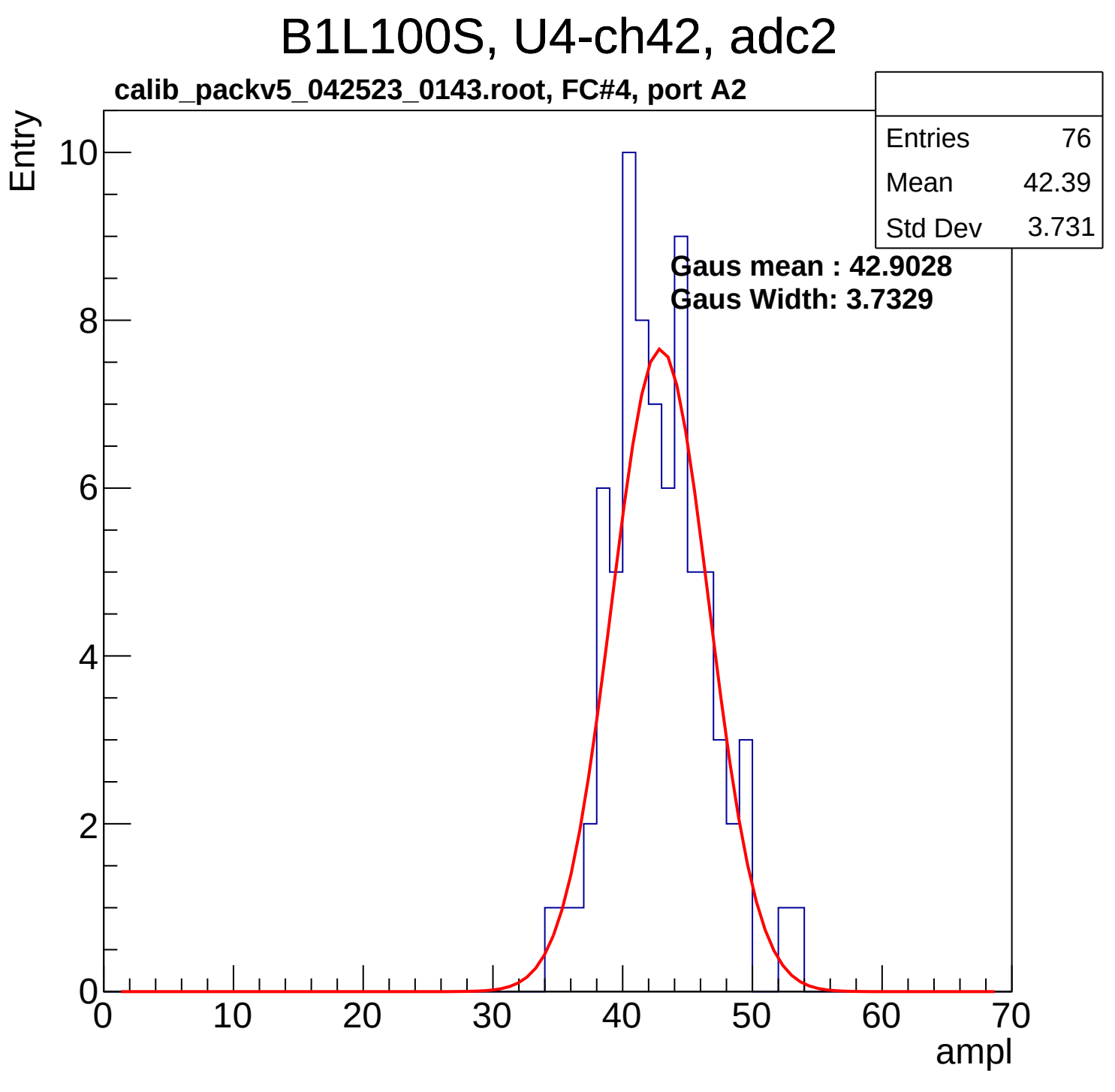

B1L100S, U4-ch41, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 58.41
Std Dev 7.935
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

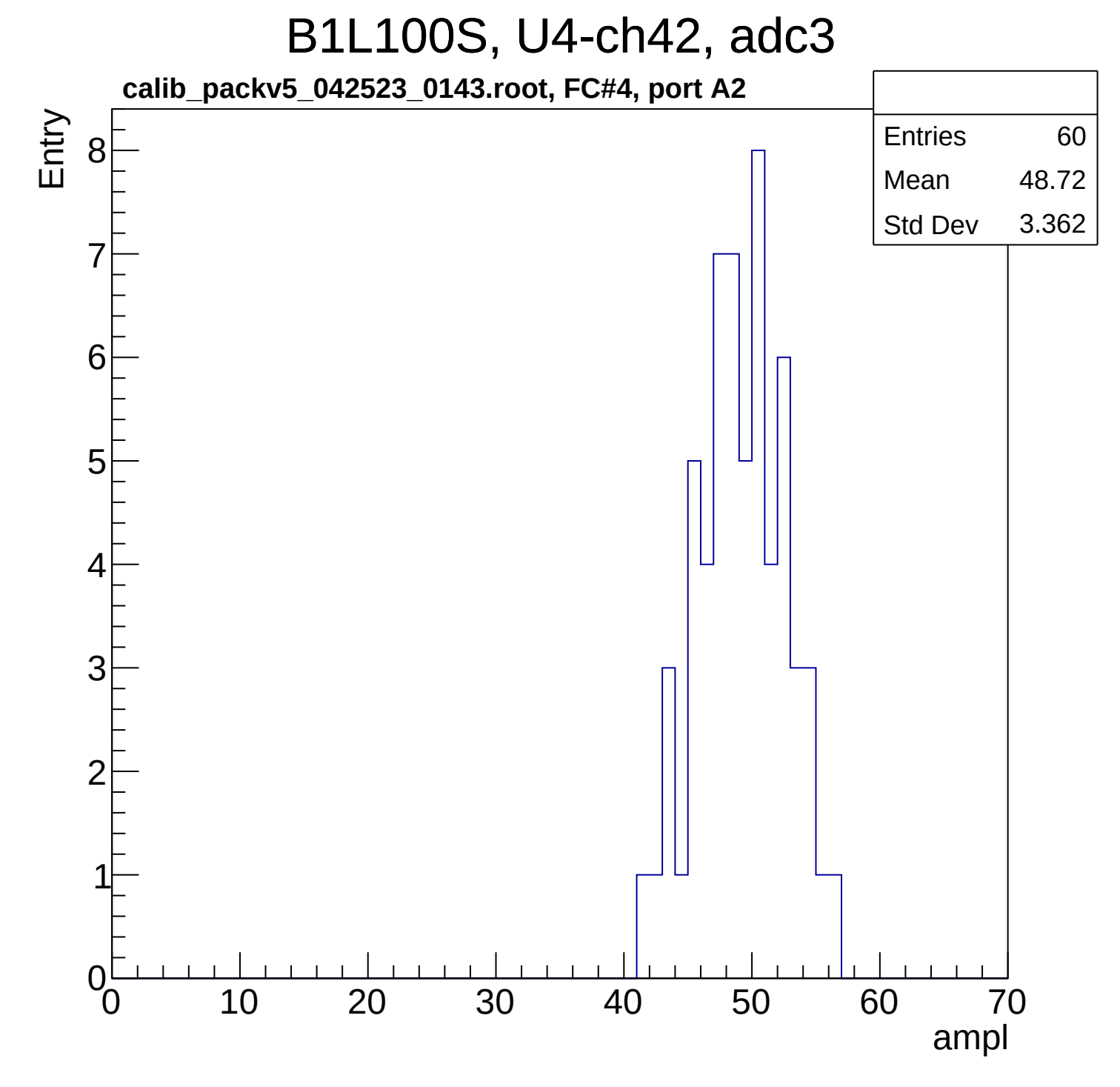

B1L100S, U4-ch41, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 61.67
Std Dev 1.333
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

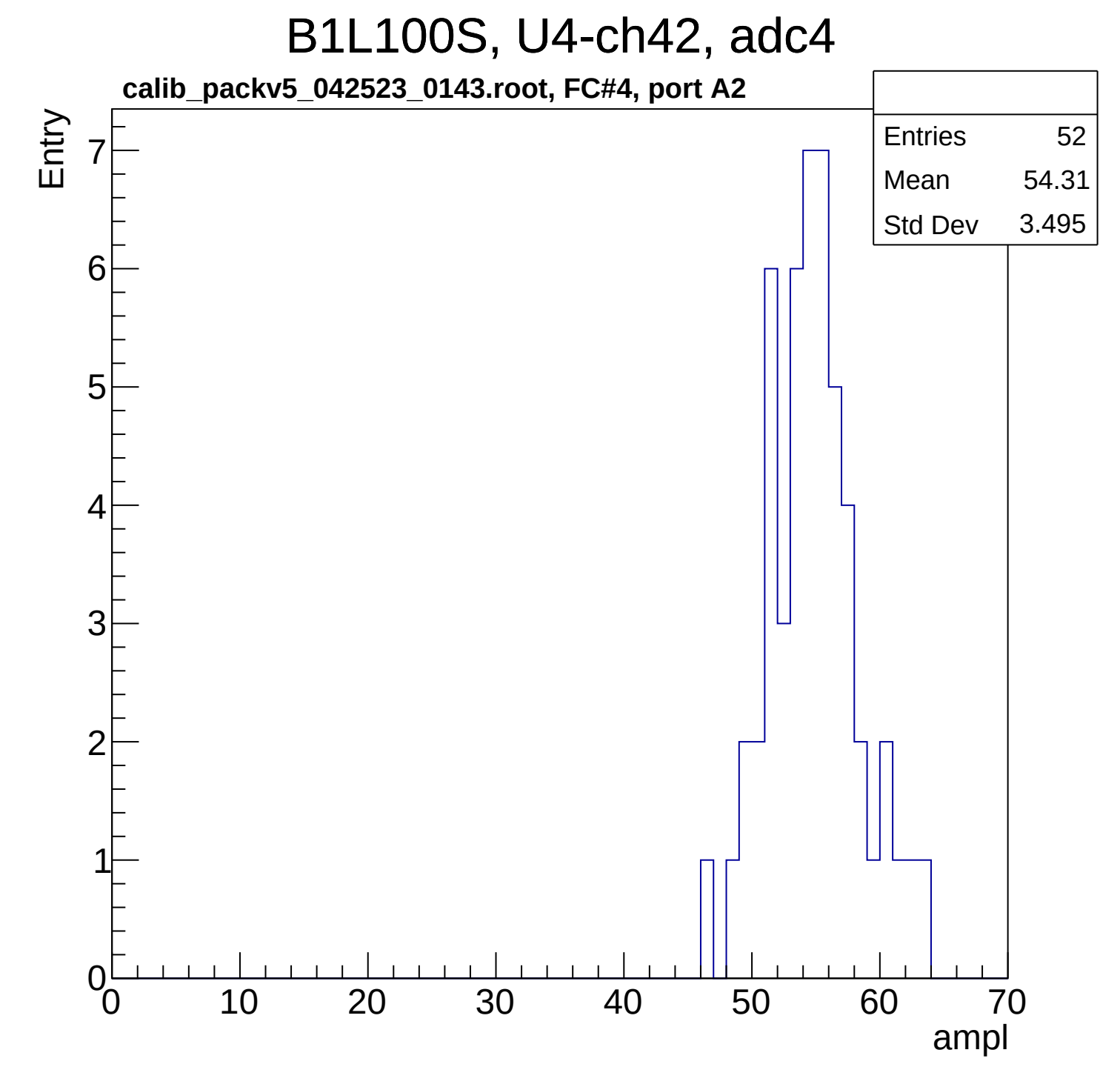

B1L100S, U4-ch41, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 20
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

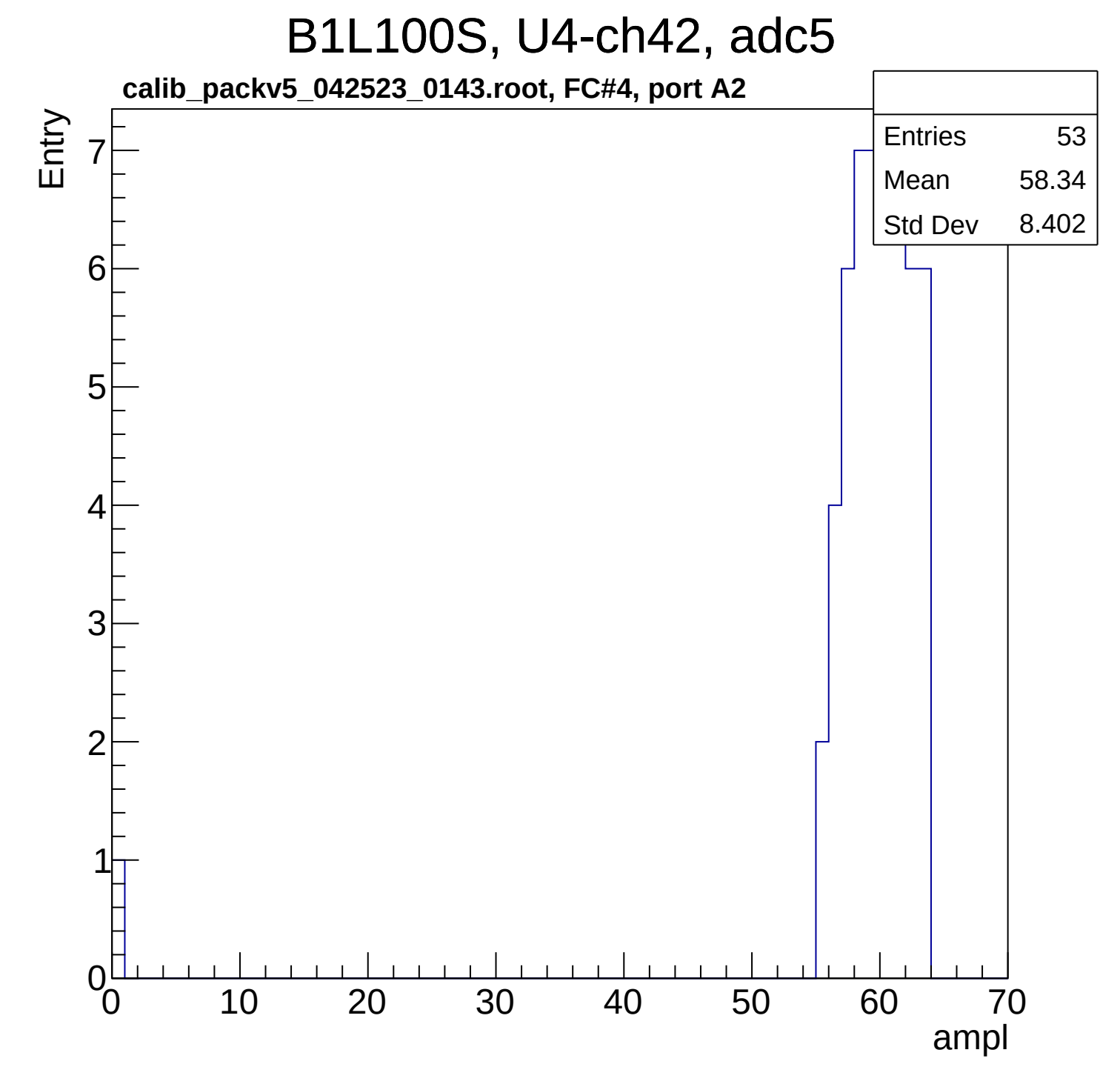

B1L100S, U4-ch42, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 29.6
Std Dev 3.622
Gaus mean : 30.3264
Gaus Width: 4.2814
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

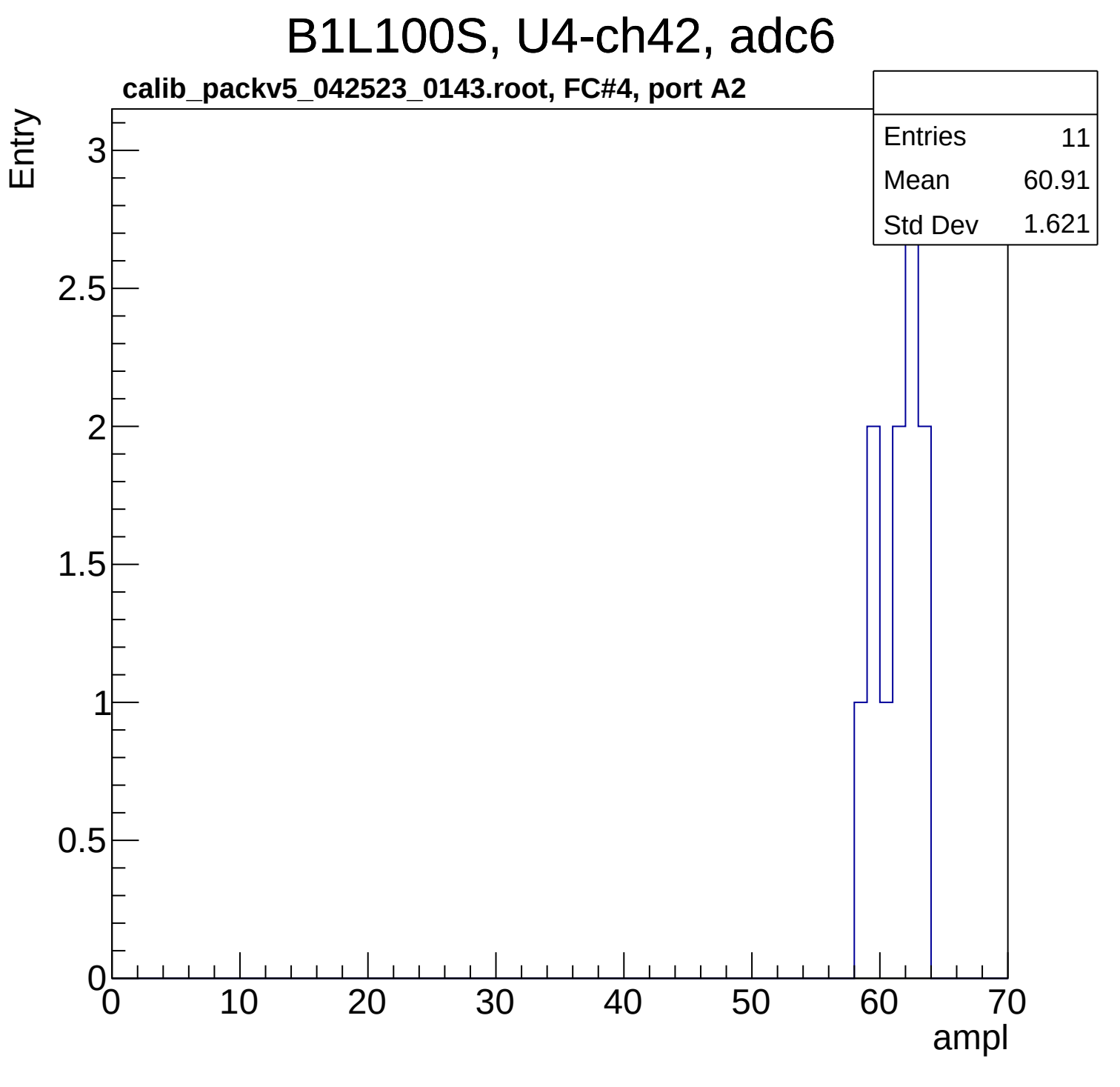

B1L100S, U4-ch42, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 34.68
Std Dev 3.267
Gaus mean : 35.1488
Gaus Width: 3.4669
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

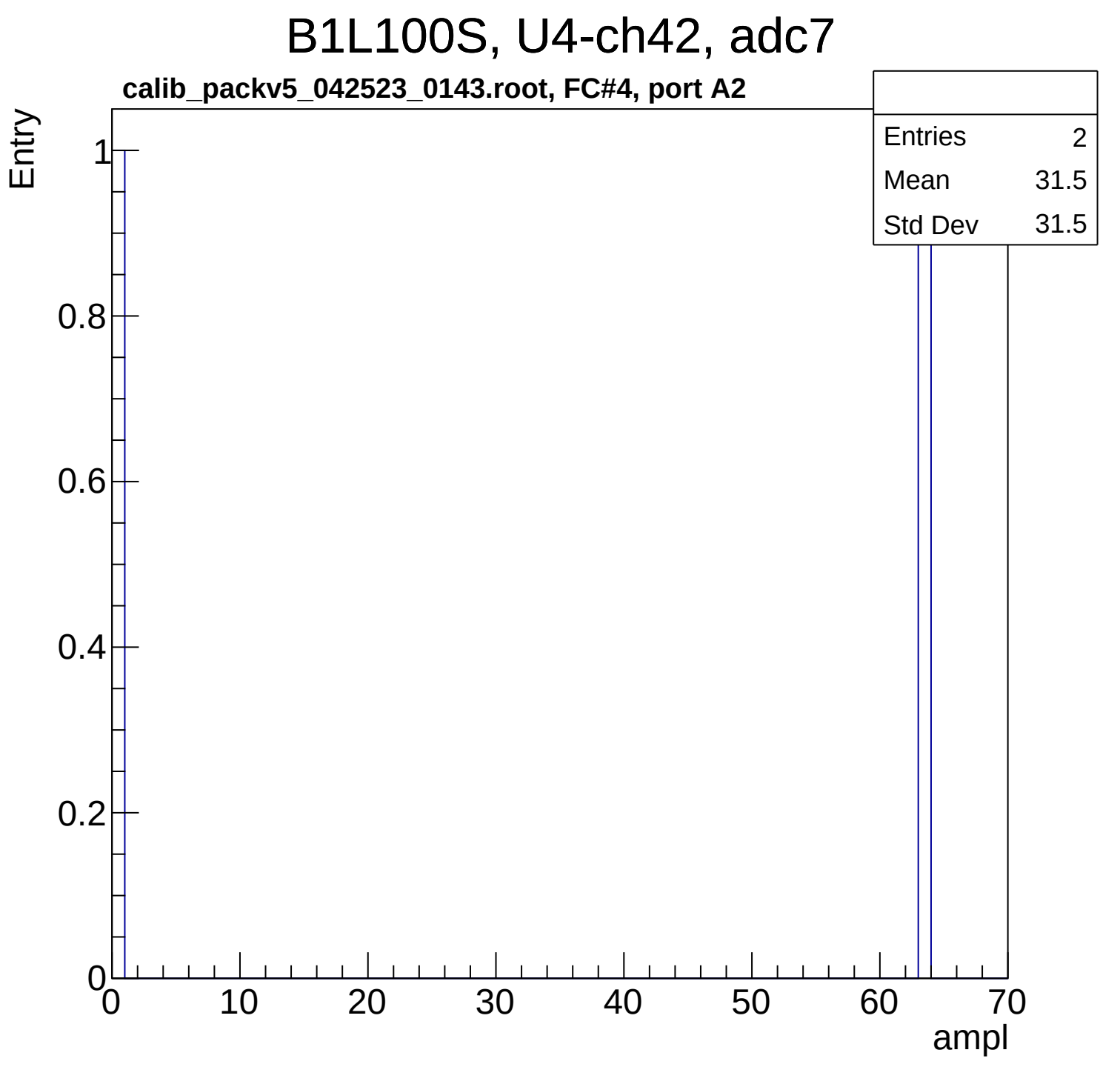

B1L100S, U4-ch42, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 42.39
Std Dev 3.731
Gaus mean : 42.9028
Gaus Width: 3.7329
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

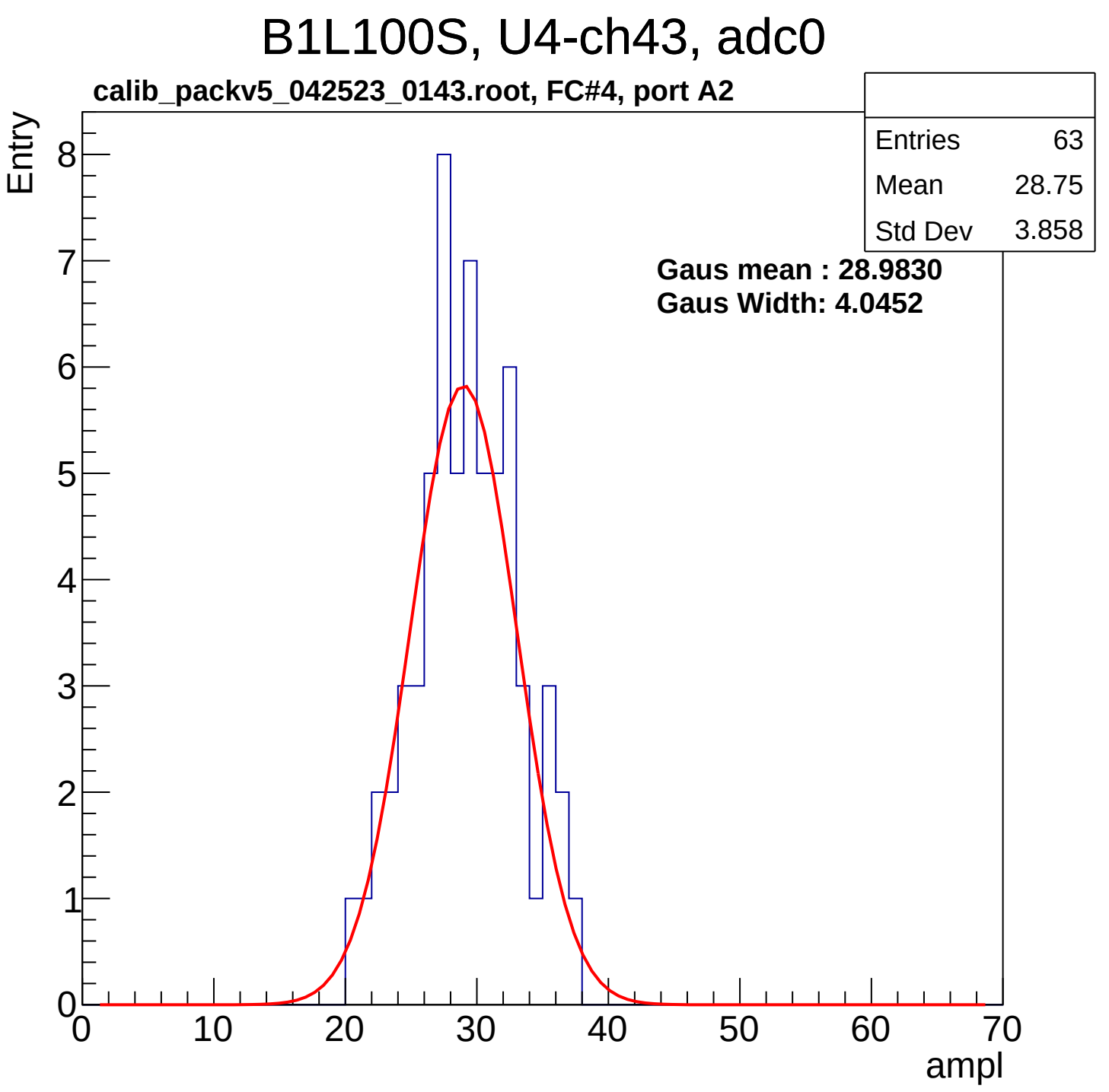

B1L100S, U4-ch42, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 48.72
Std Dev 3.362
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

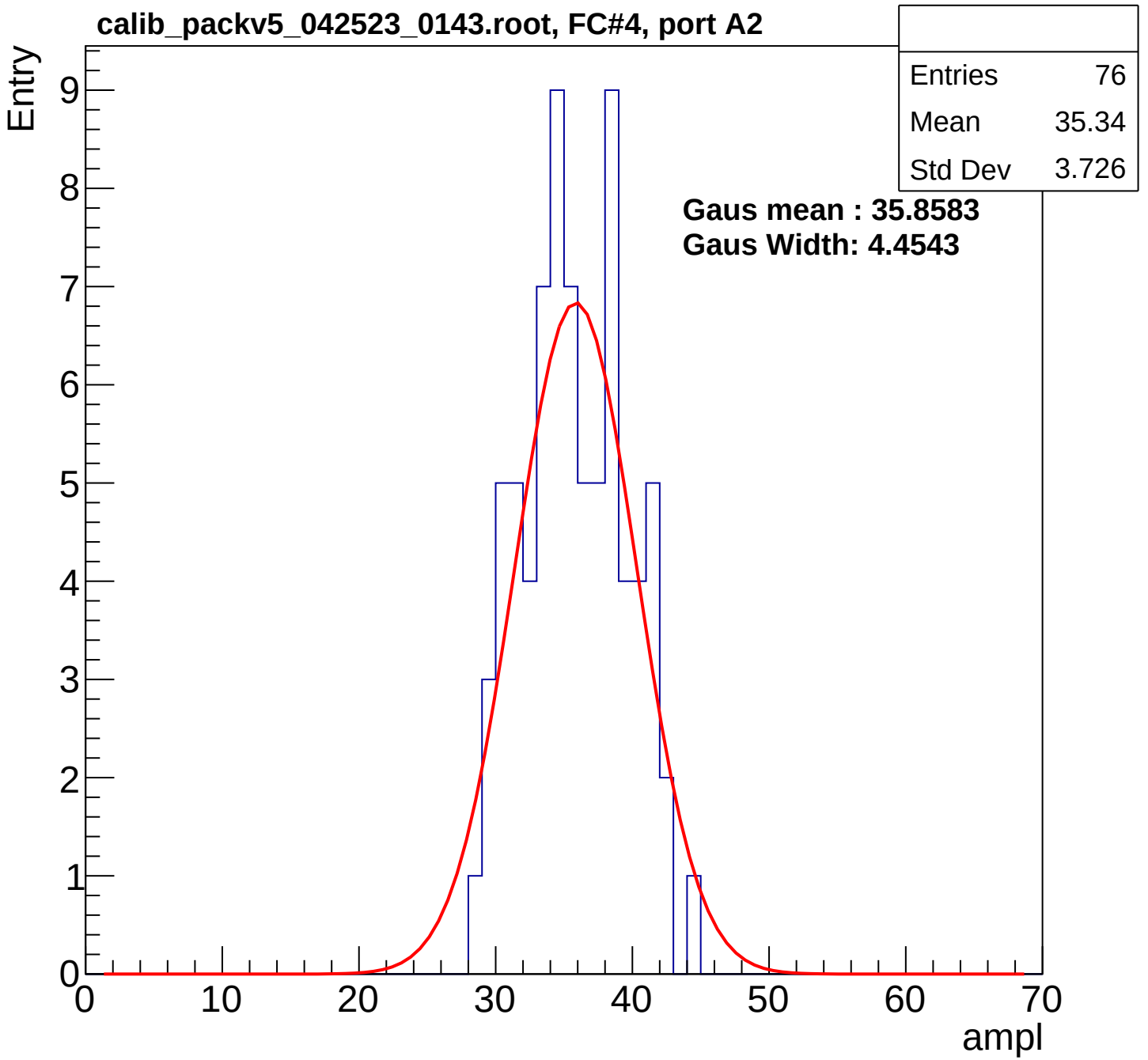

B1L100S, U4-ch42, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 54.31
Std Dev 3.495
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

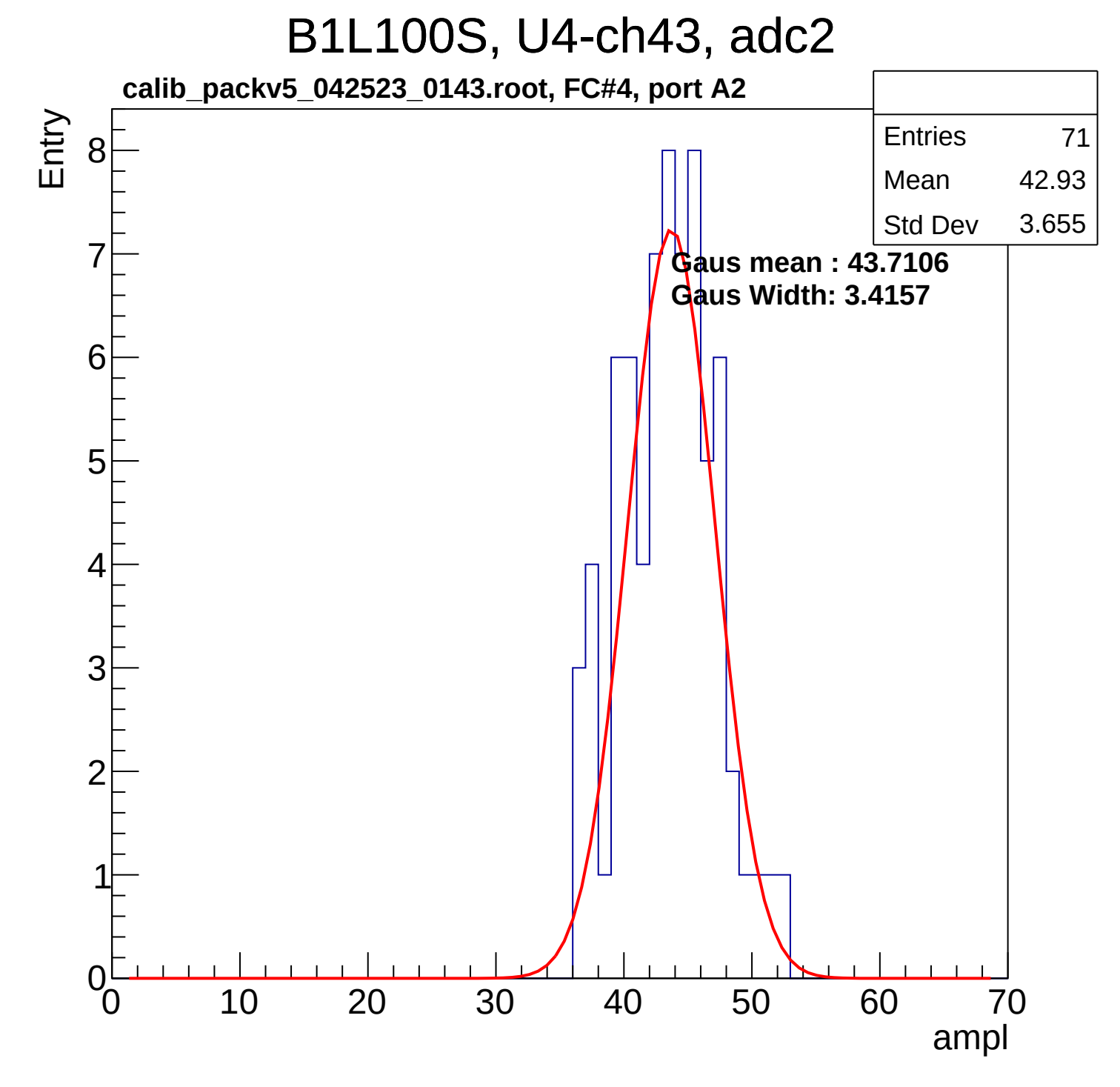

B1L100S, U4-ch42, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 58.34
Std Dev 8.402
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

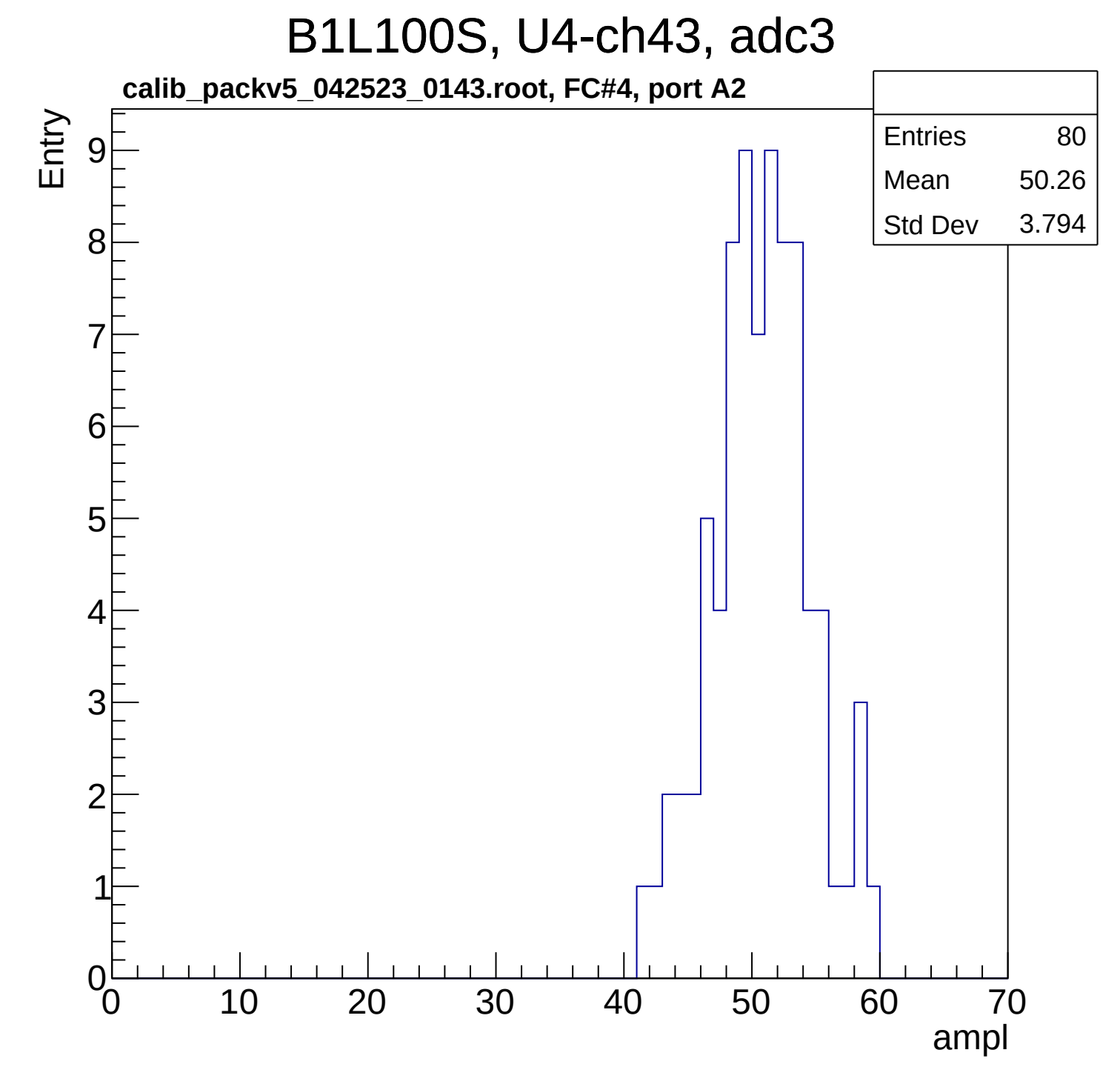

B1L100S, U4-ch42, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 60.91
Std Dev 1.621
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

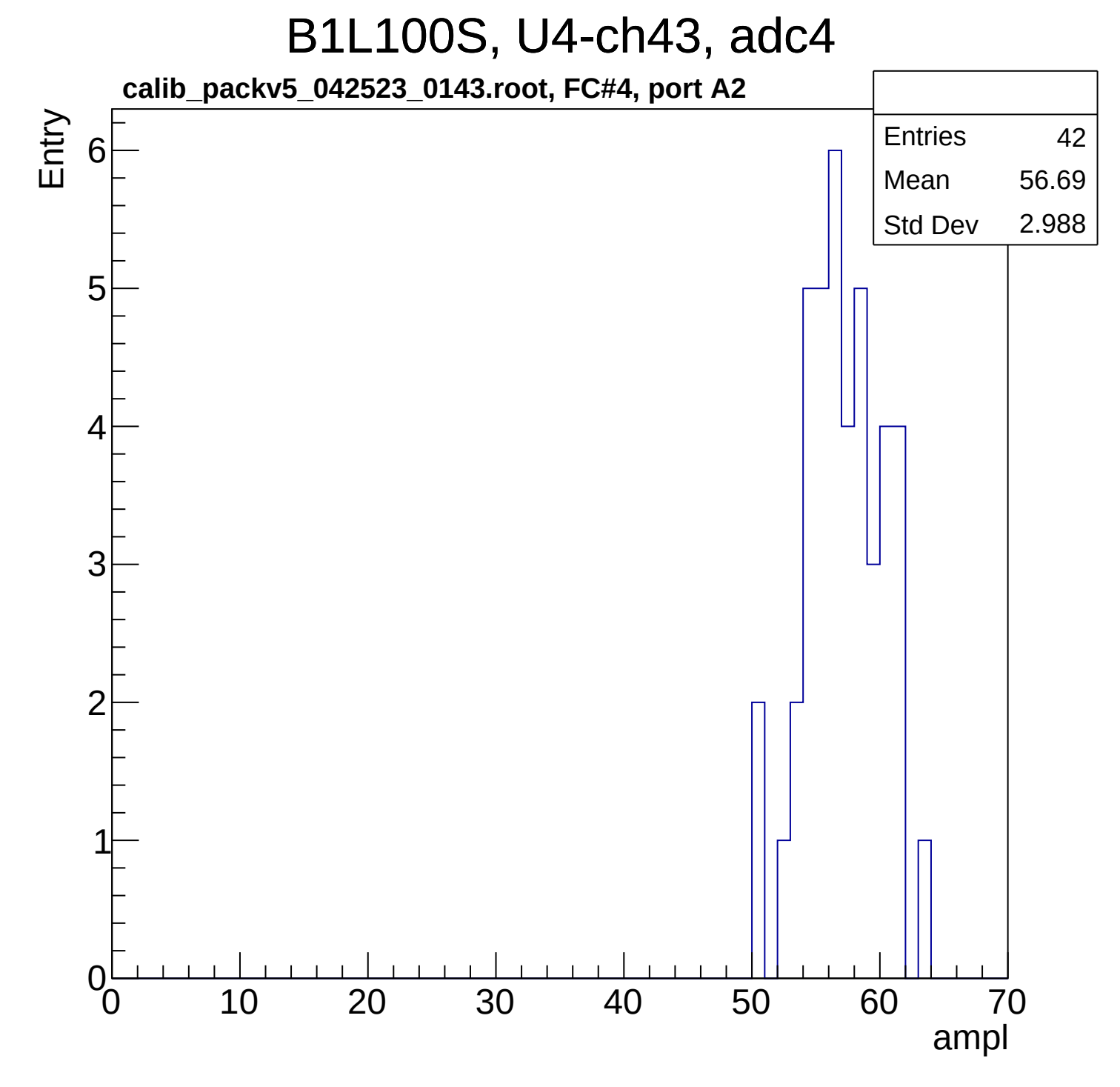

B1L100S, U4-ch42, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

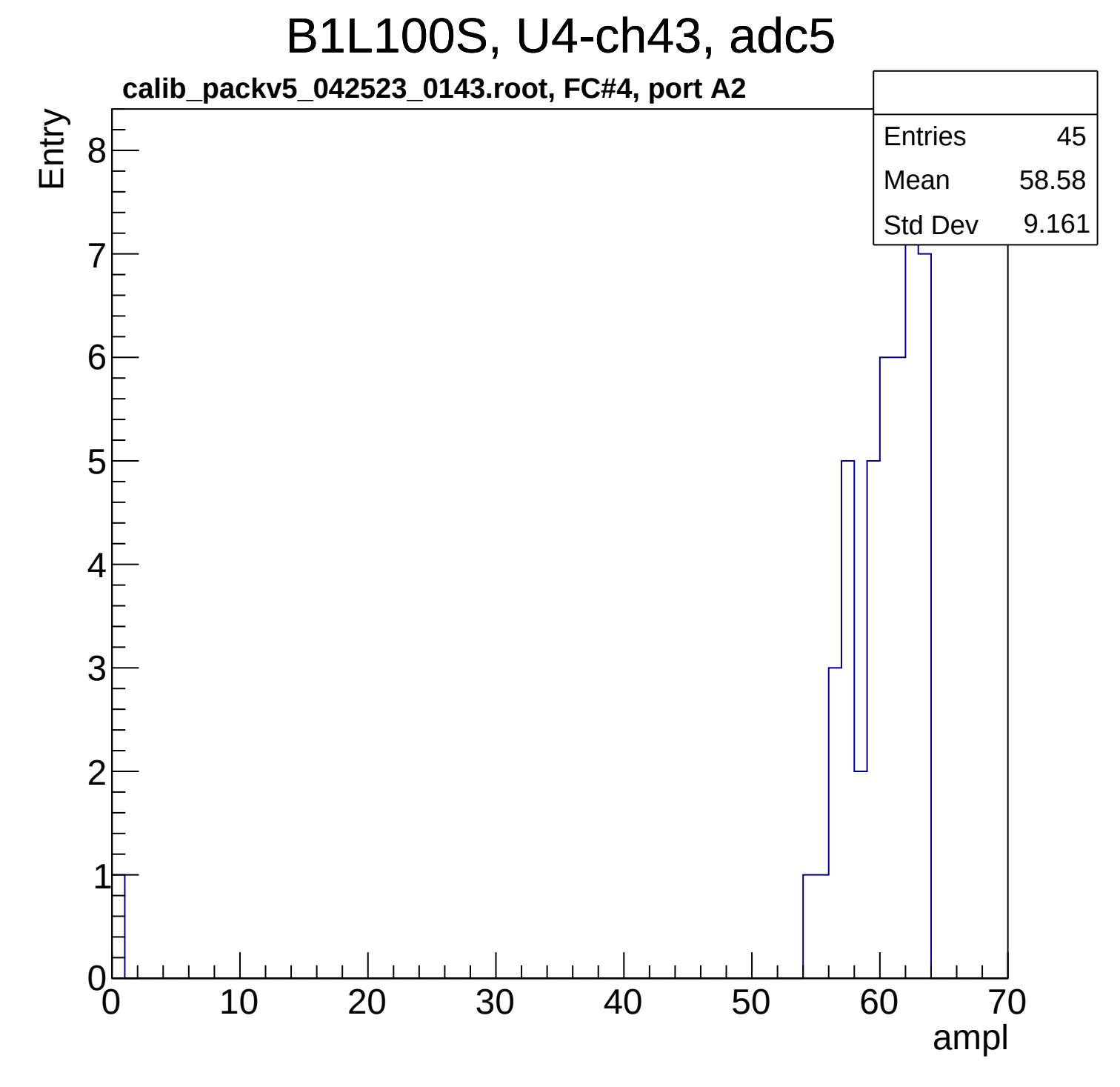

B1L100S, U4-ch43, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 28.75
Std Dev 3.858
Gaus mean : 28.9830
Gaus Width: 4.0452
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

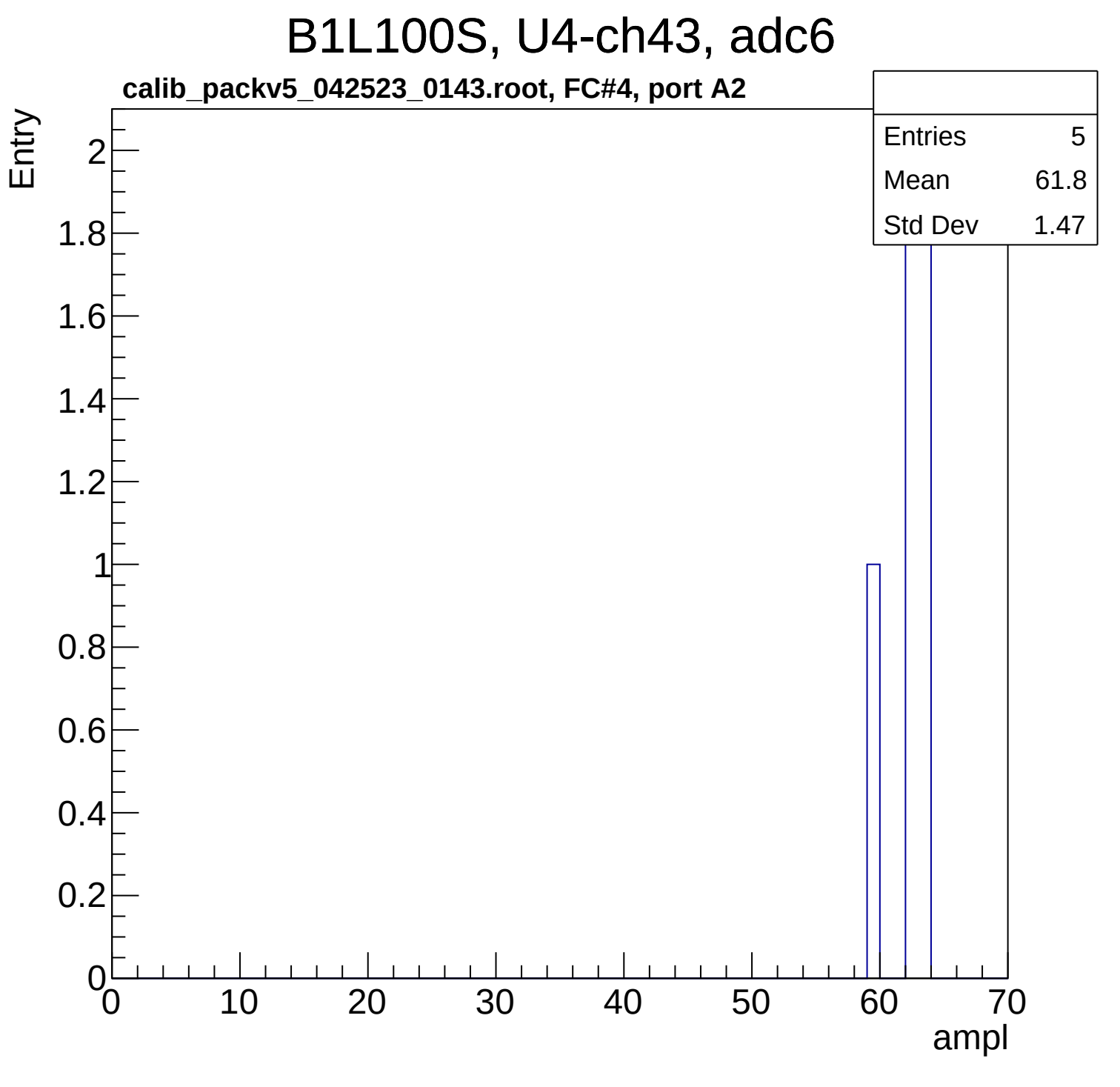

B1L100S, U4-ch43, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 35.34
Std Dev 3.726
Gaus mean : 35.8583
Gaus Width: 4.4543
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

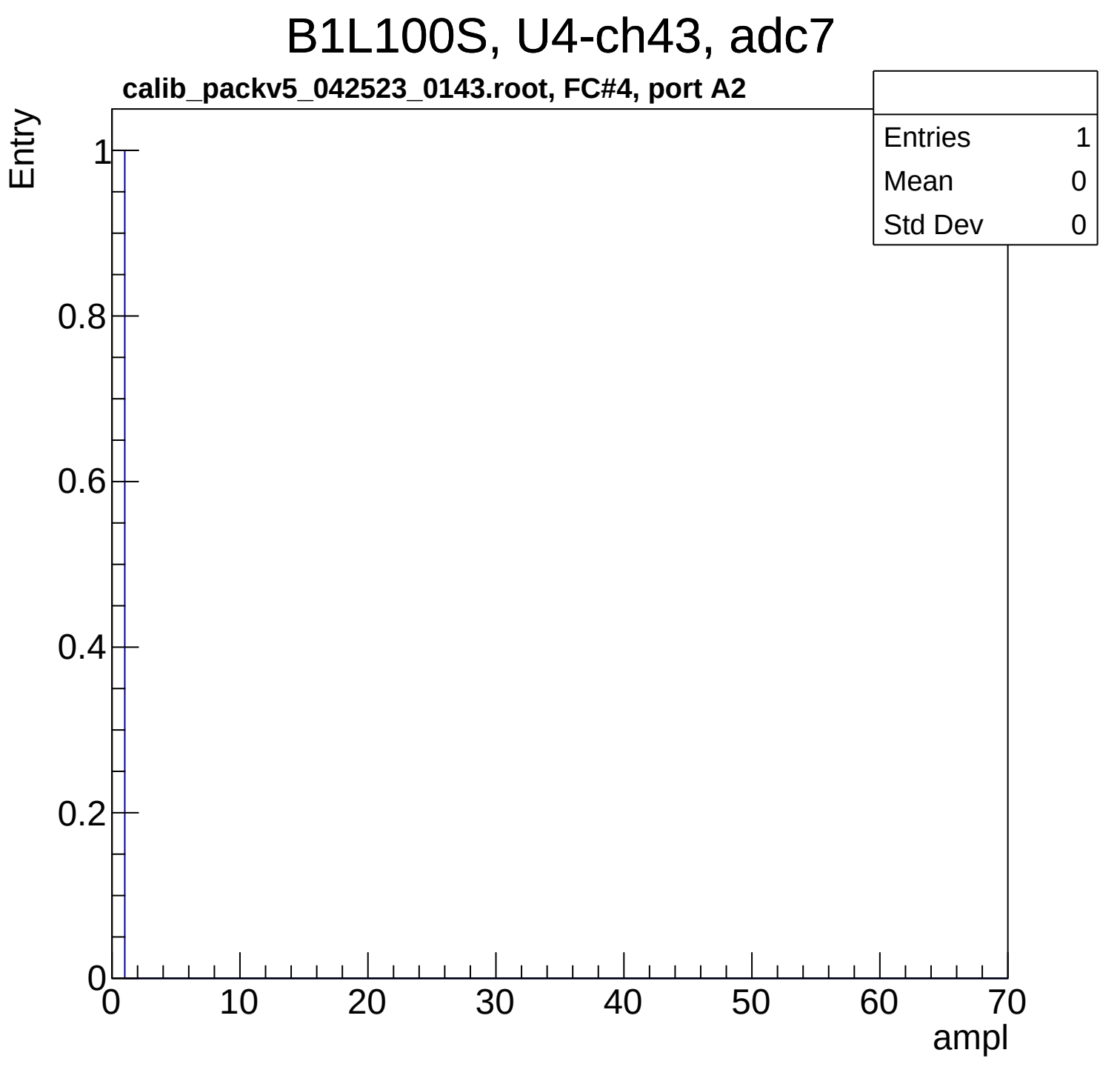

B1L100S, U4-ch43, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 42.93
Std Dev 3.655
Gaus mean : 43.7106
Gaus Width: 3.4157
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

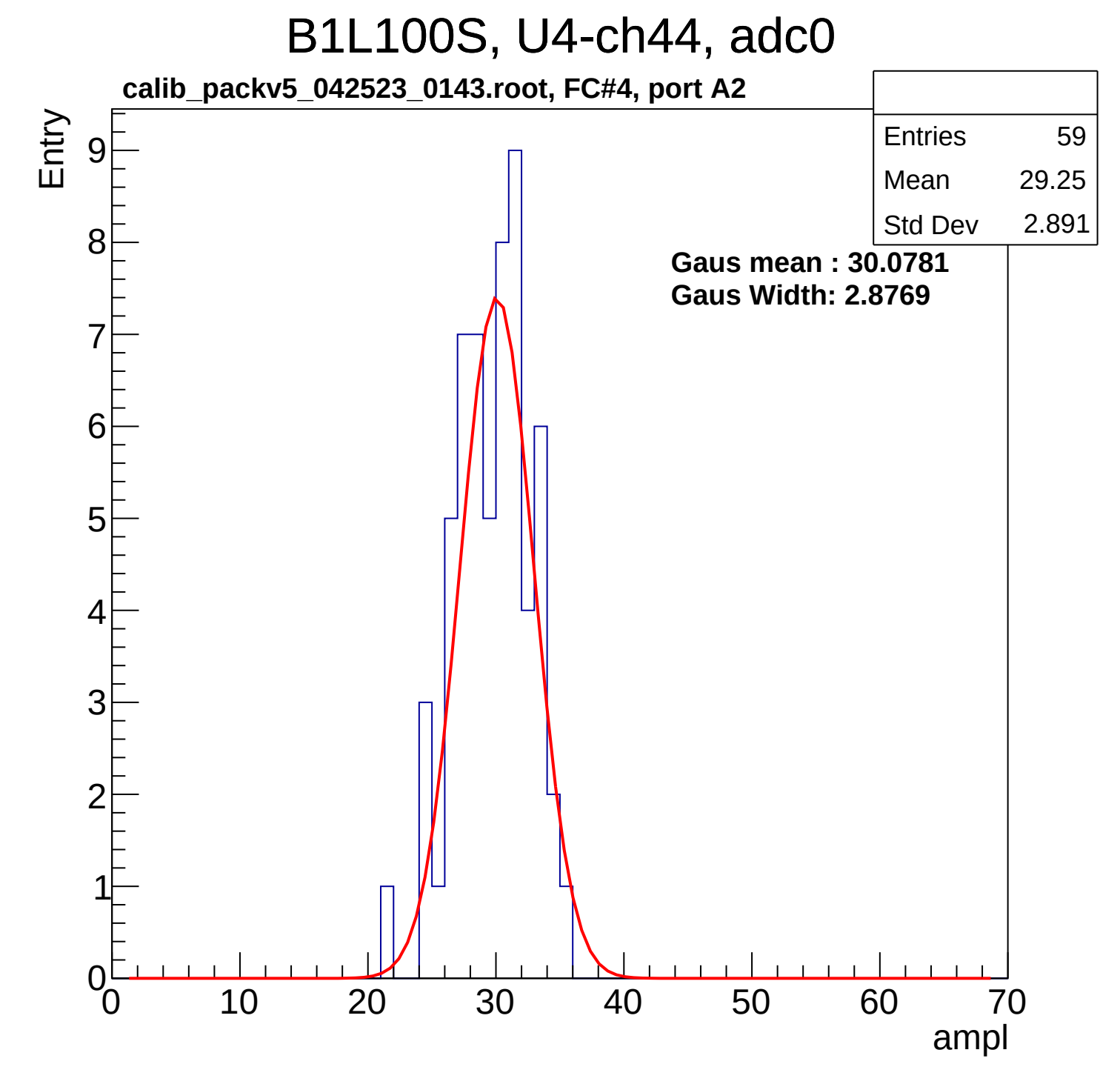

B1L100S, U4-ch43, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 50.26
Std Dev 3.794
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

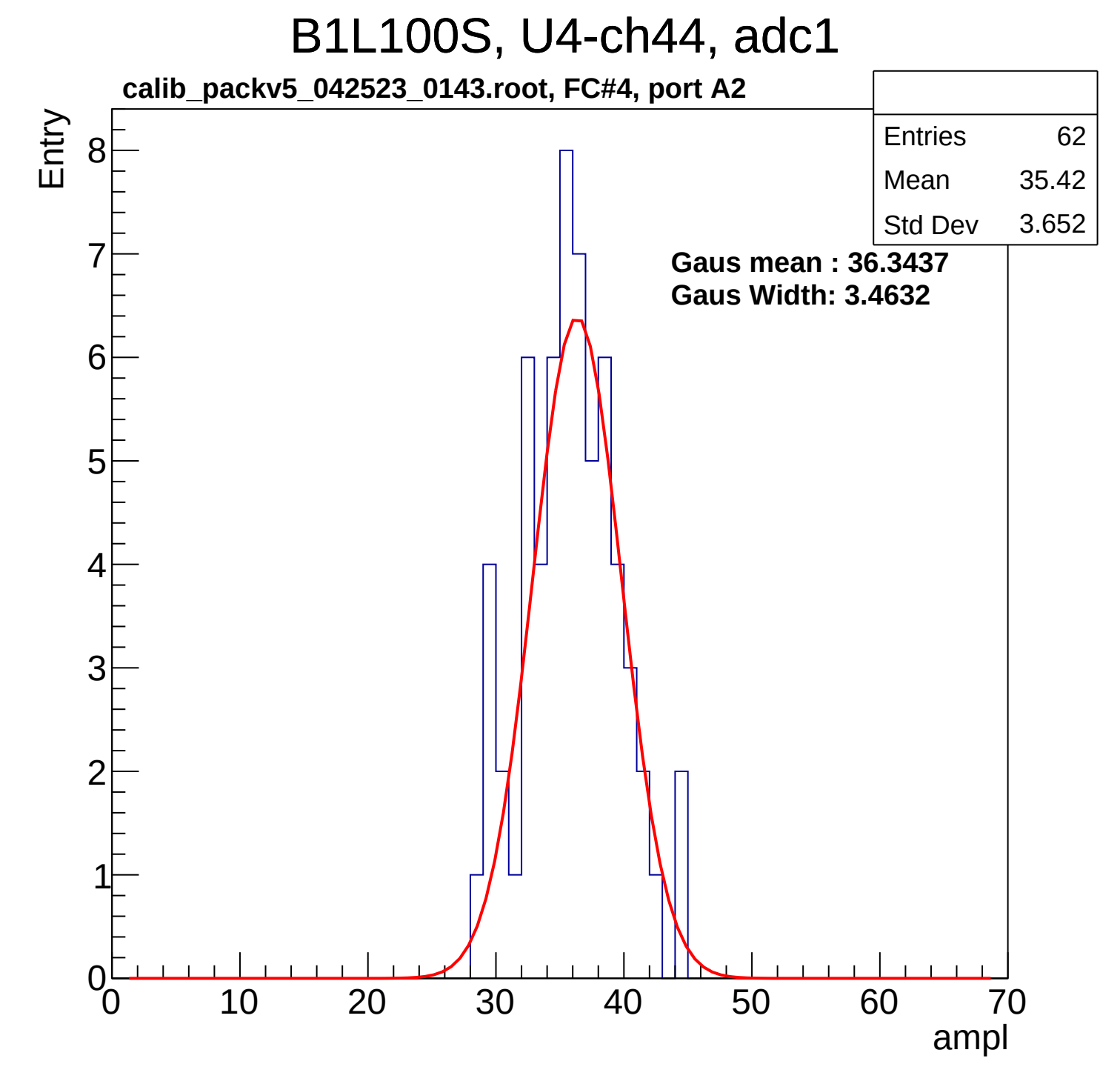

B1L100S, U4-ch43, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 42
Mean 56.69
Std Dev 2.988
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

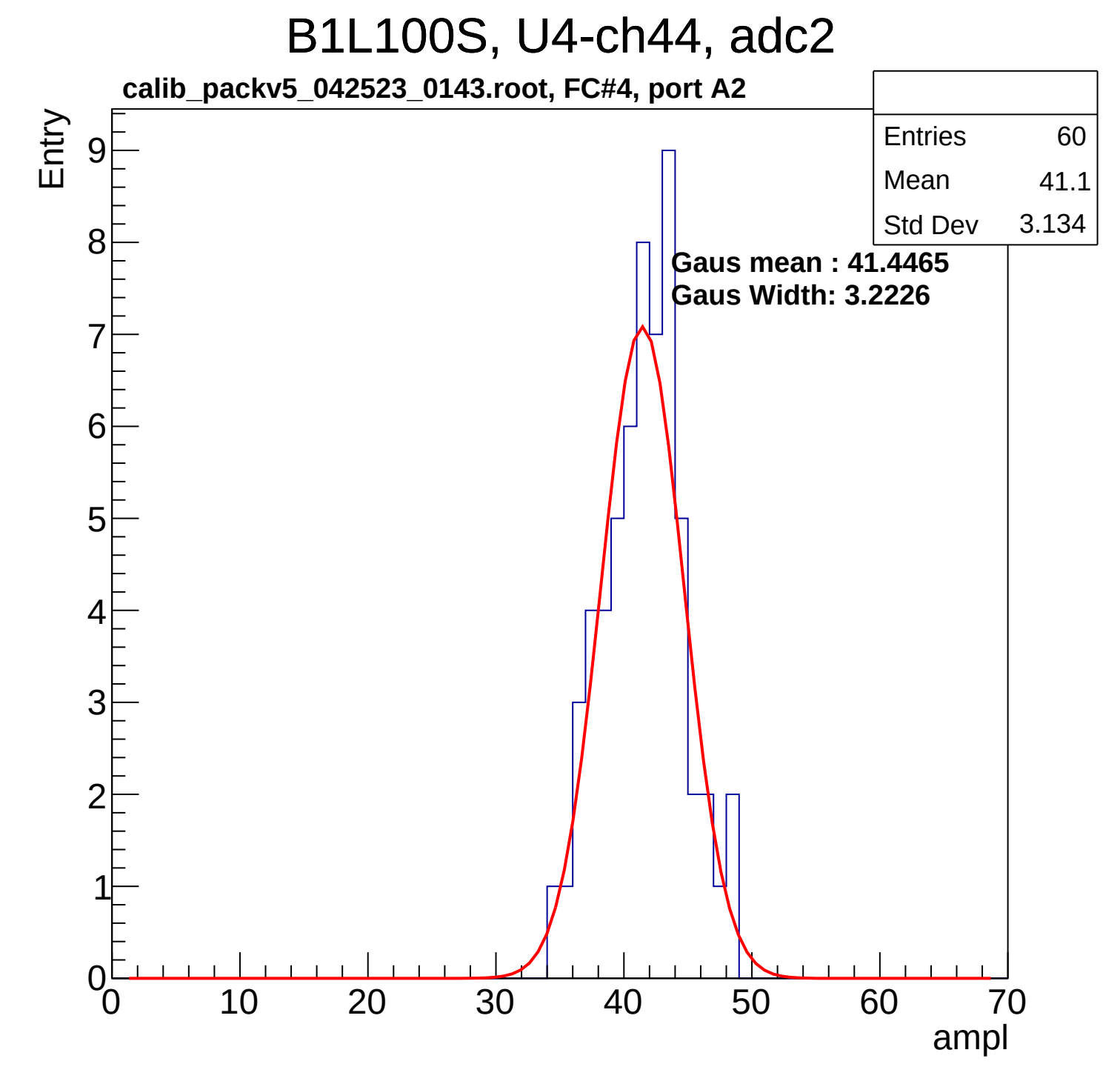

B1L100S, U4-ch43, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 45
Mean 58.58
Std Dev 9.161
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

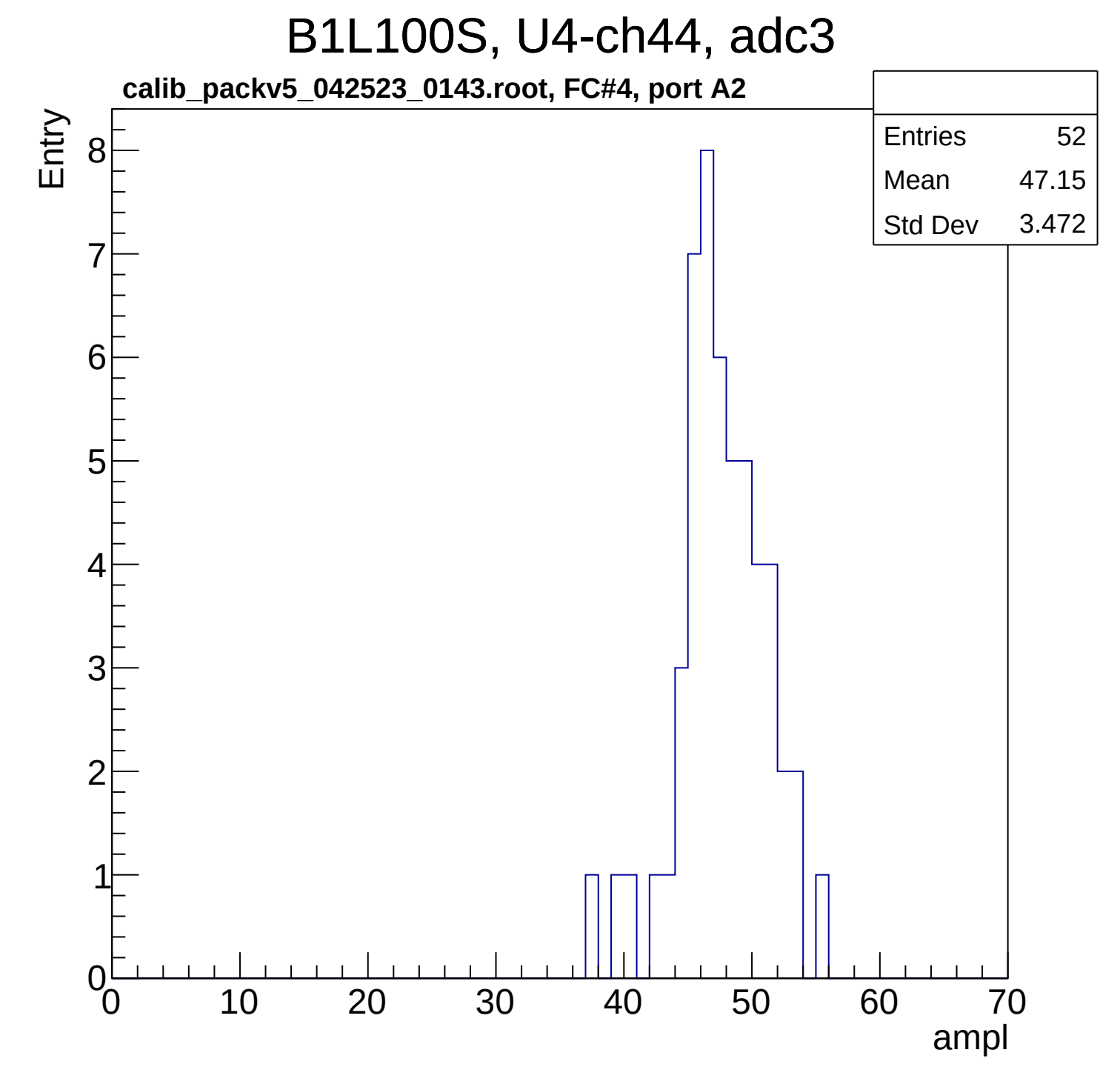

B1L100S, U4-ch43, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 5
Mean 61.8
Std Dev 1.47
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

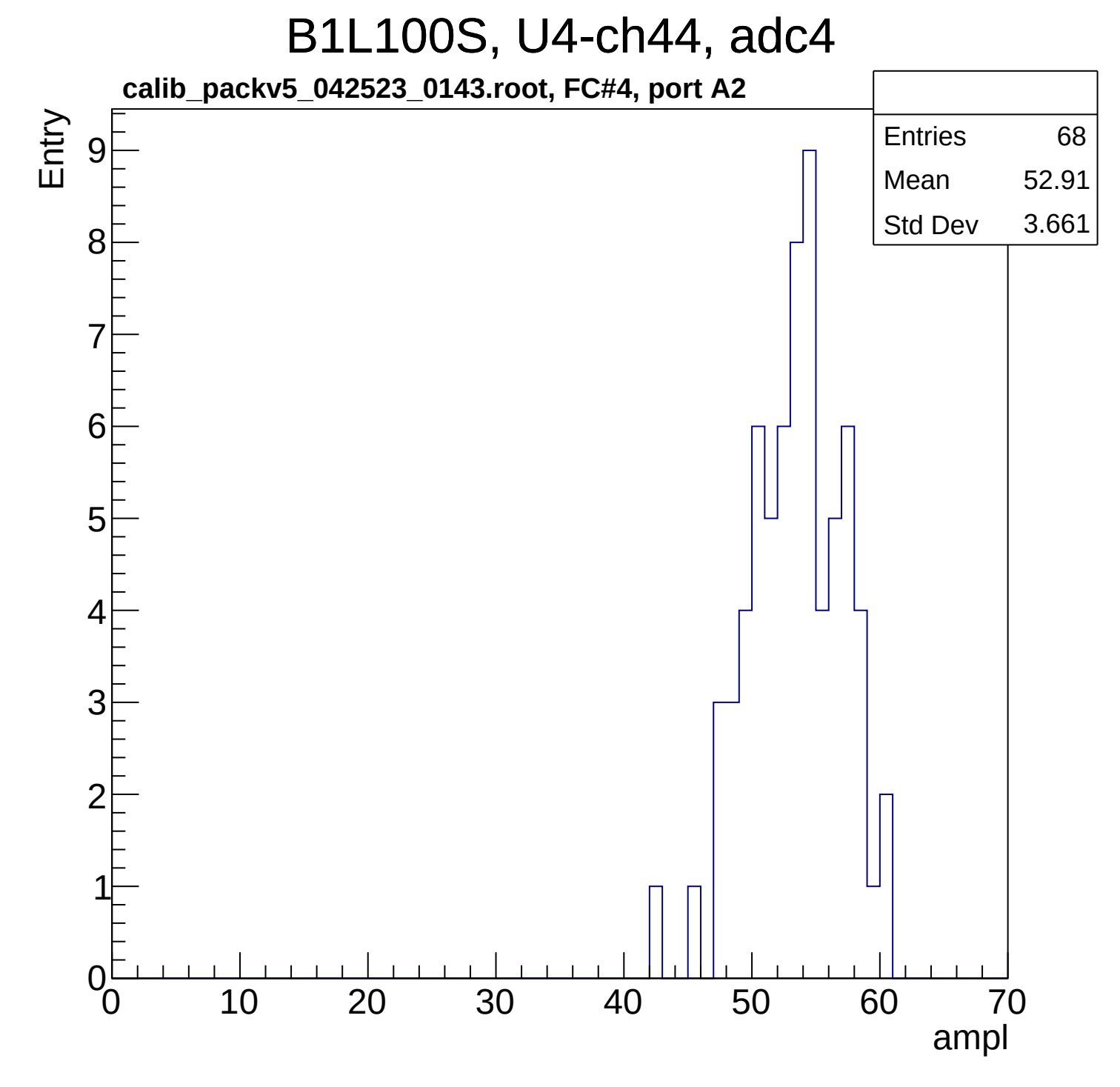

B1L100S, U4-ch43, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

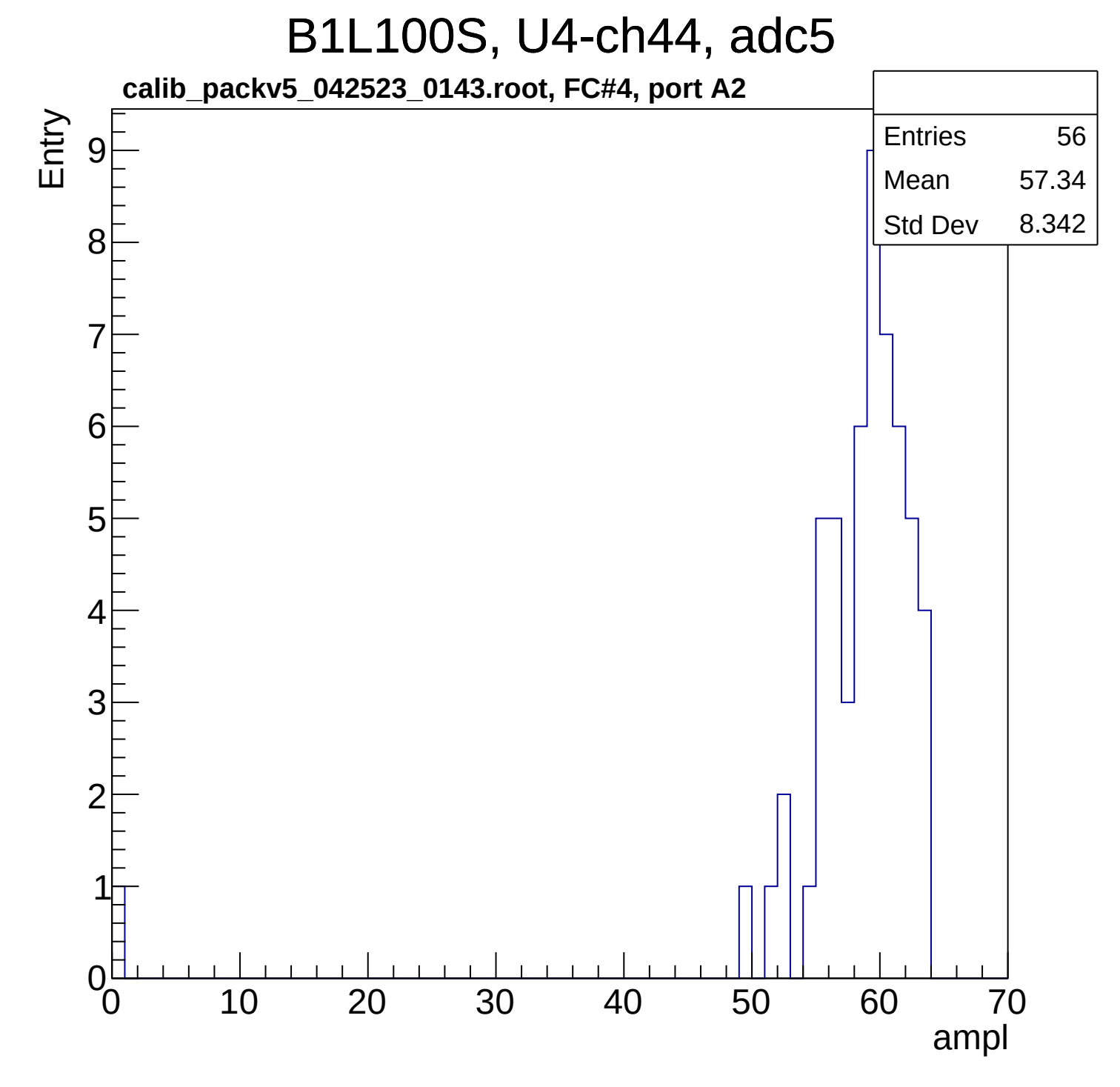

B1L100S, U4-ch44, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 29.25
Std Dev 2.891
Gaus mean : 30.0781
Gaus Width: 2.8769
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

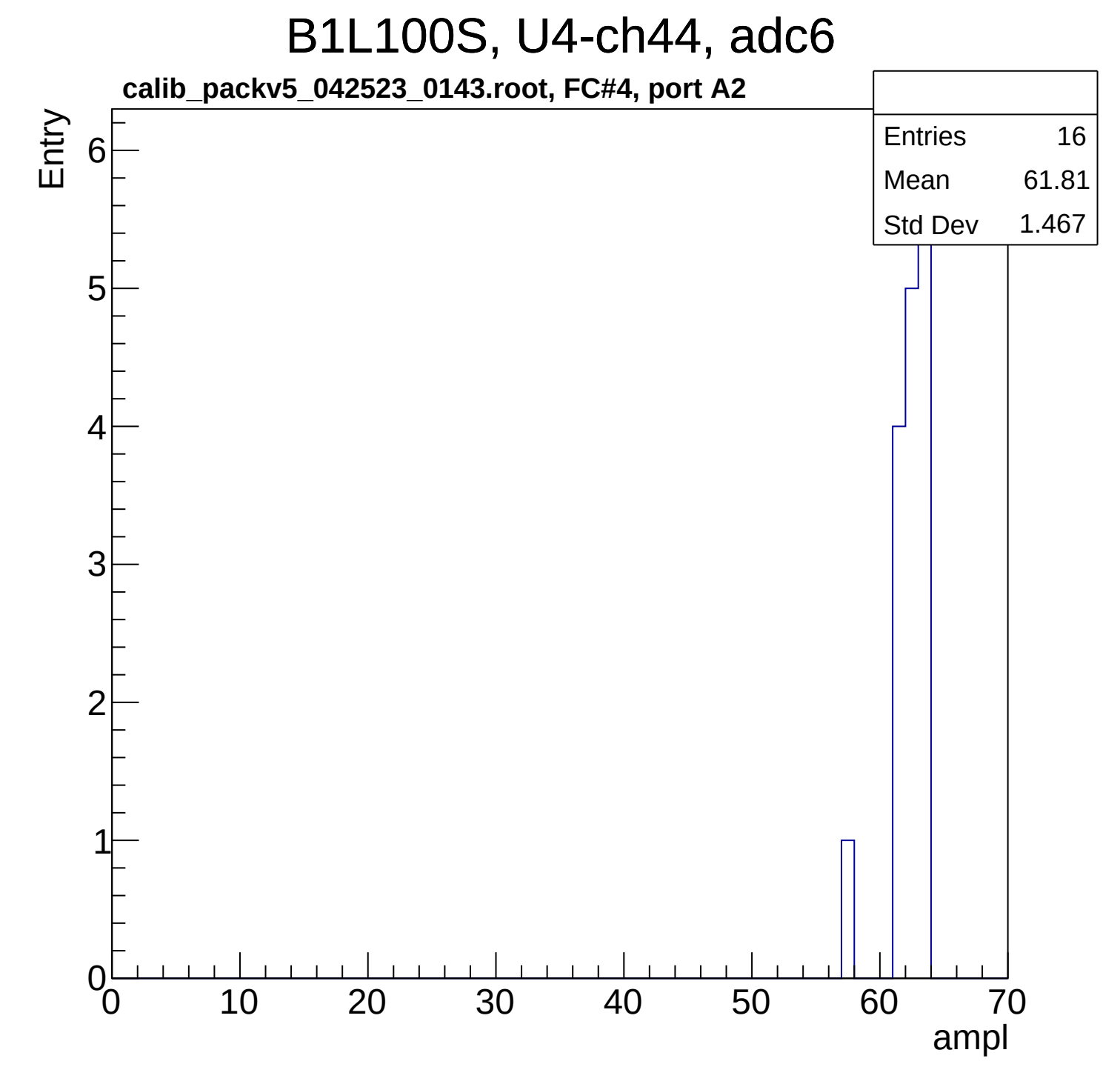

B1L100S, U4-ch44, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 35.42
Std Dev 3.652
Gaus mean : 36.3437
Gaus Width: 3.4632
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

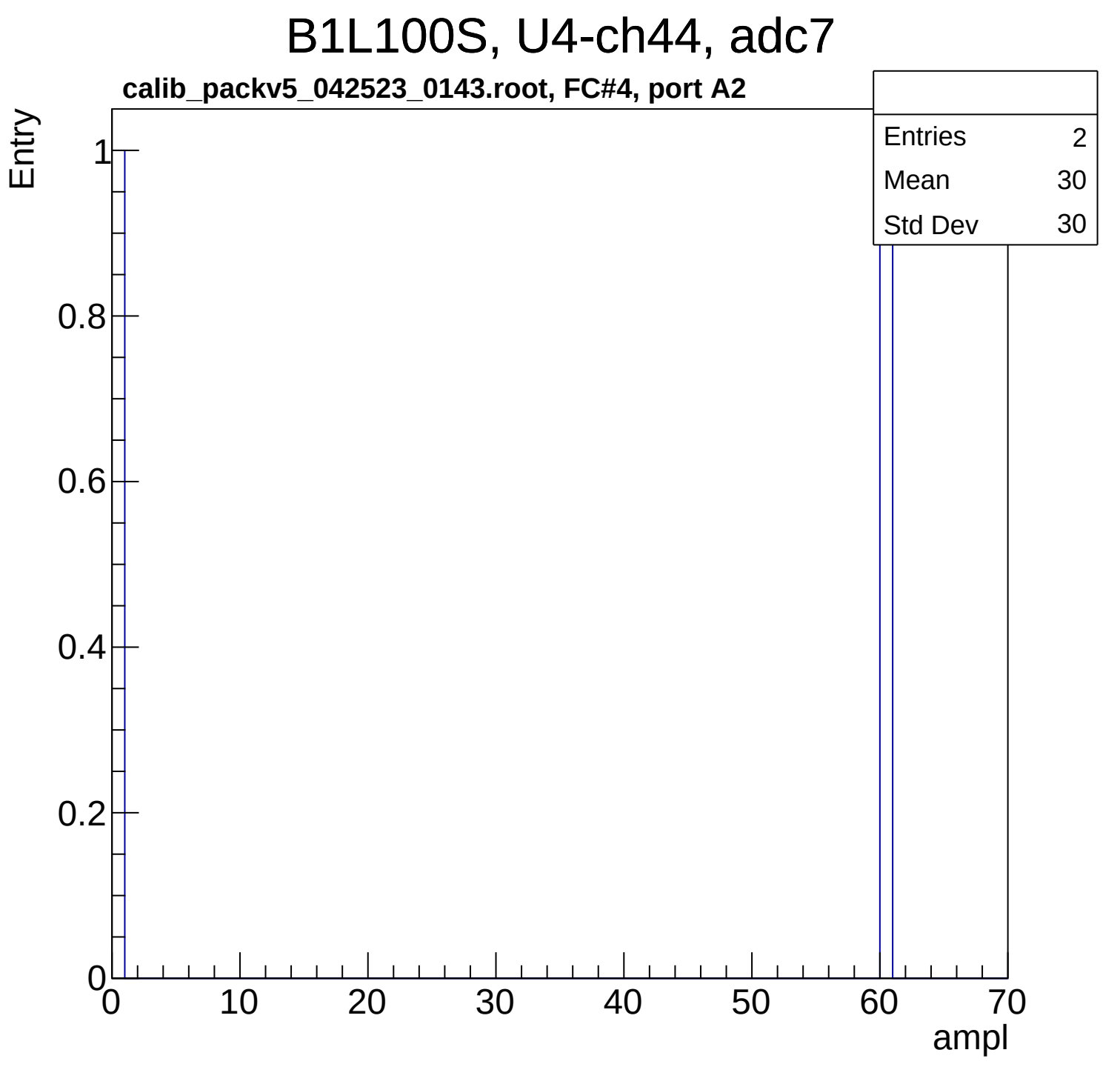

B1L100S, U4-ch44, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 41.1
Std Dev 3.134
Gaus mean : 41.4465
Gaus Width: 3.2226
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

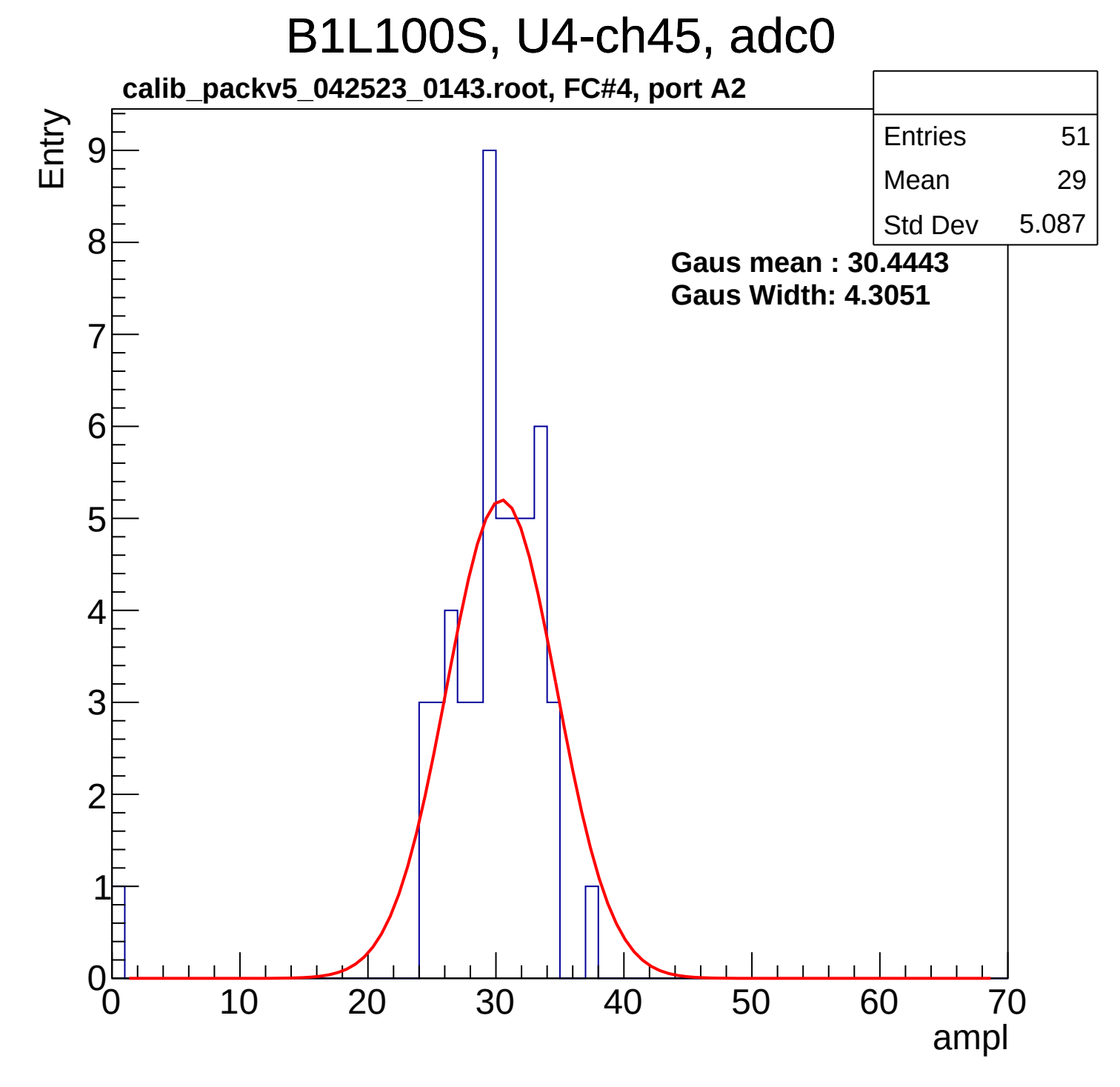

B1L100S, U4-ch44, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 47.15
Std Dev 3.472
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

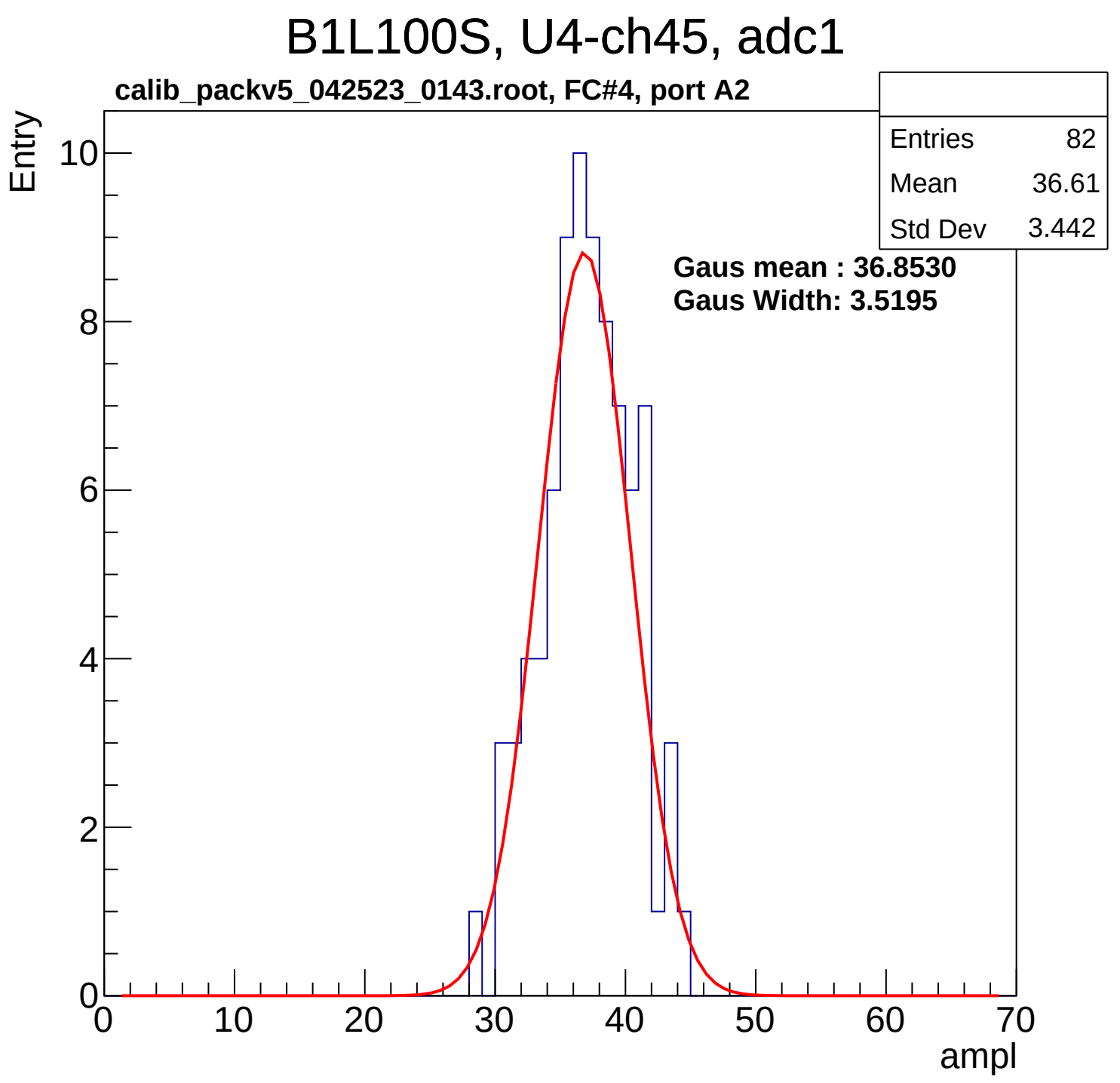

B1L100S, U4-ch44, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 52.91
Std Dev 3.661
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

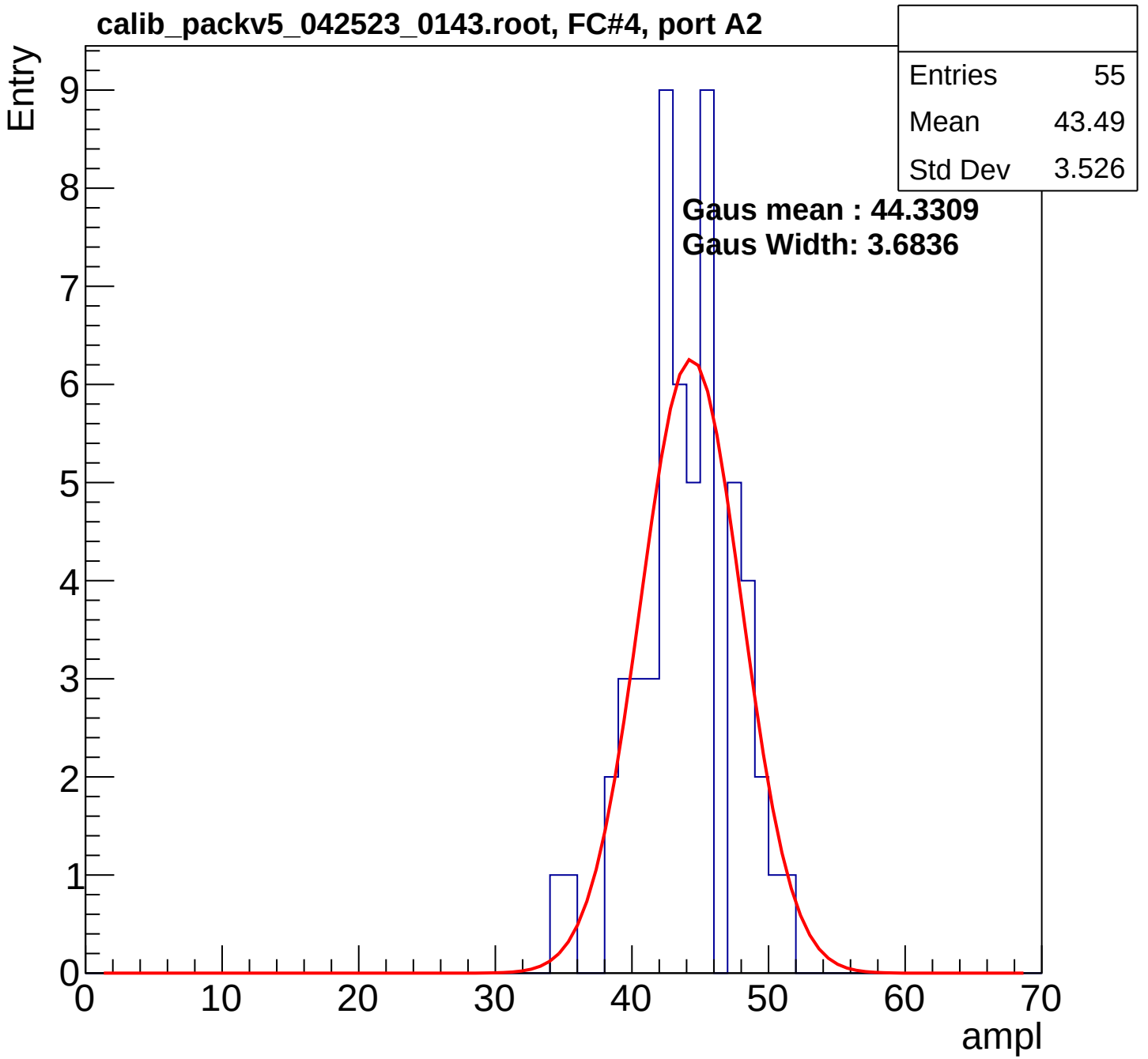

B1L100S, U4-ch44, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 57.34
Std Dev 8.342
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

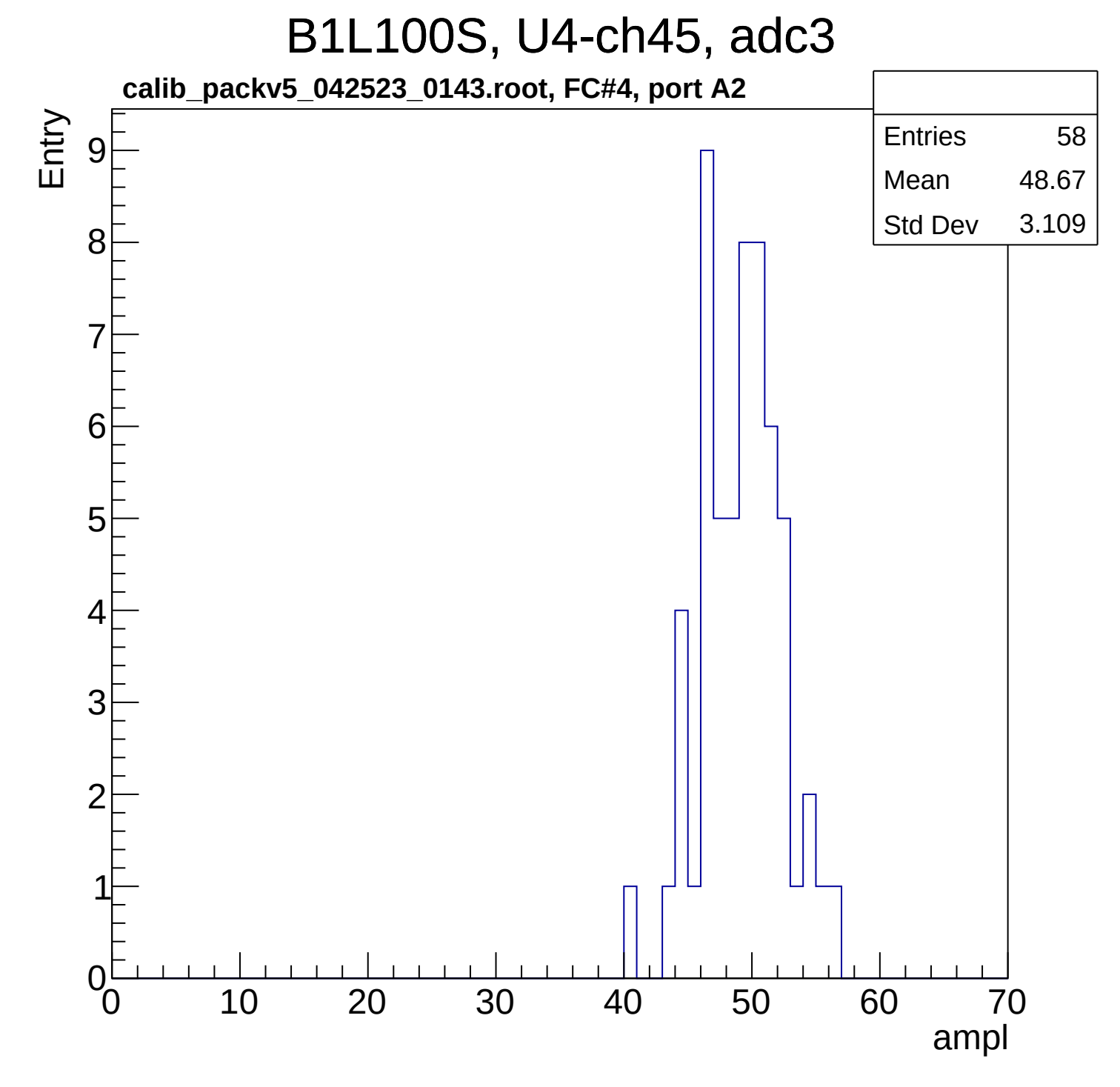

B1L100S, U4-ch44, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 16
Mean 61.81
Std Dev 1.467
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

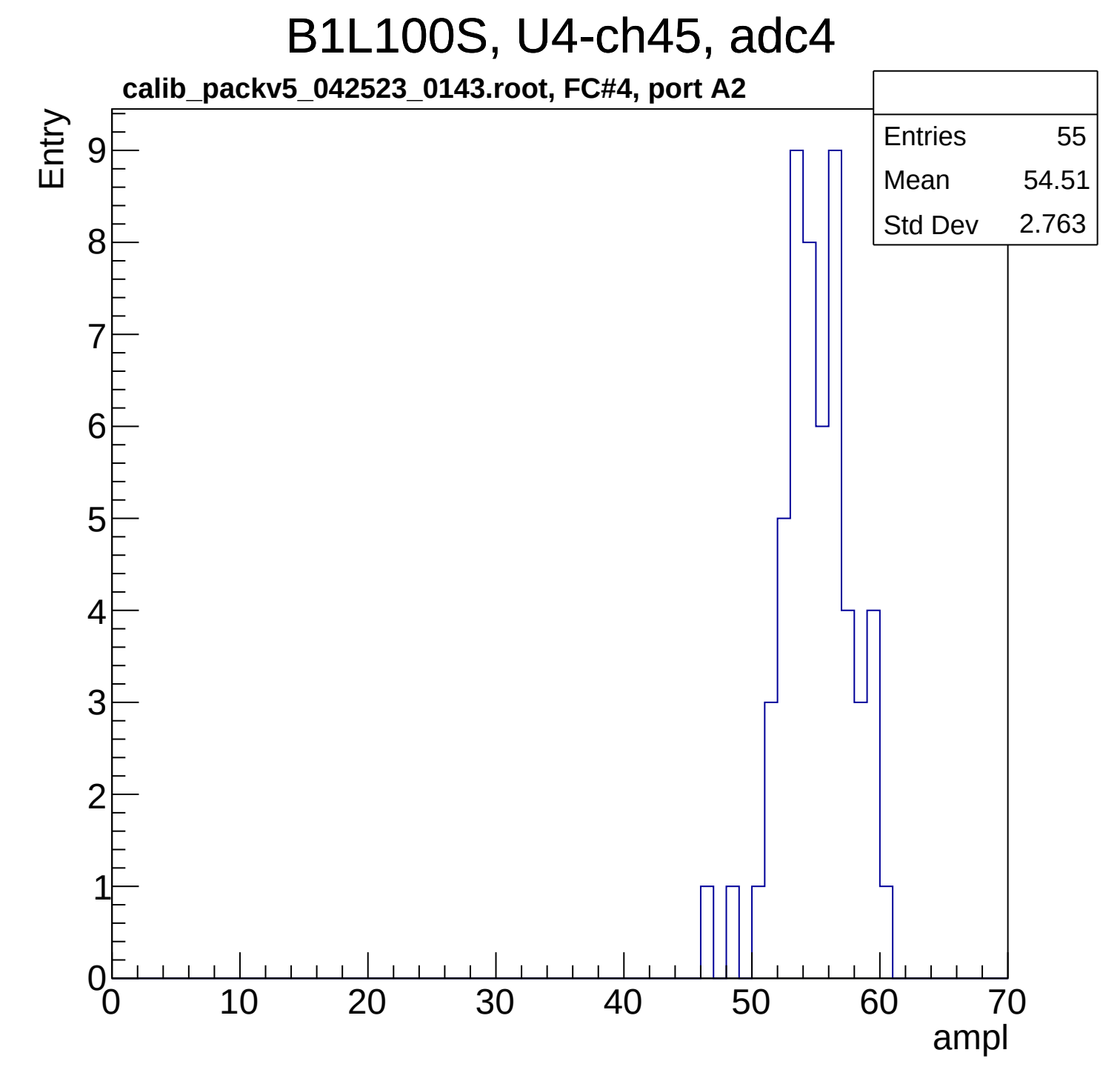

B1L100S, U4-ch44, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 30
Std Dev 30
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

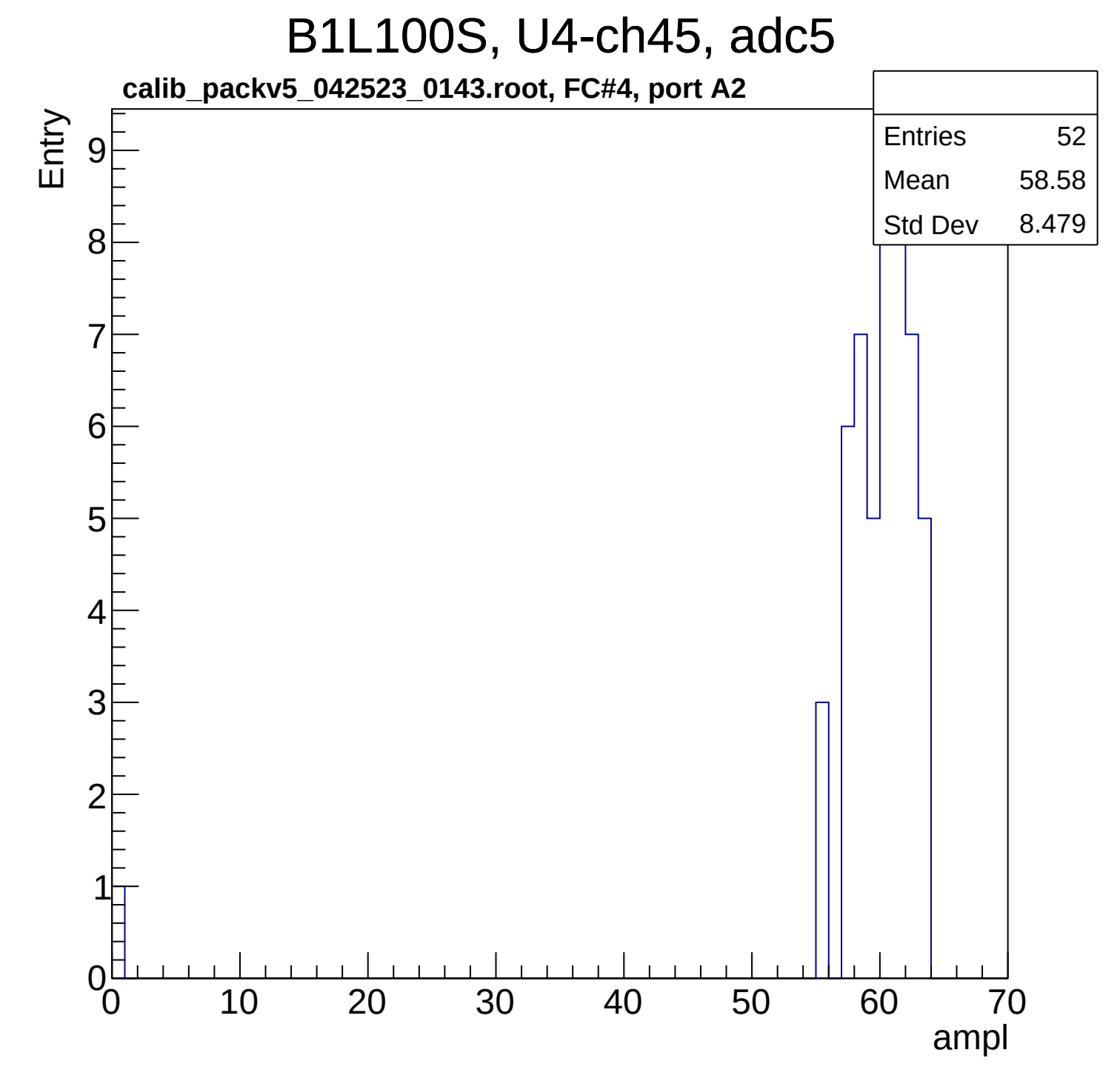

B1L100S, U4-ch45, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 29
Std Dev 5.087
Gaus mean : 30.4443
Gaus Width: 4.3051
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

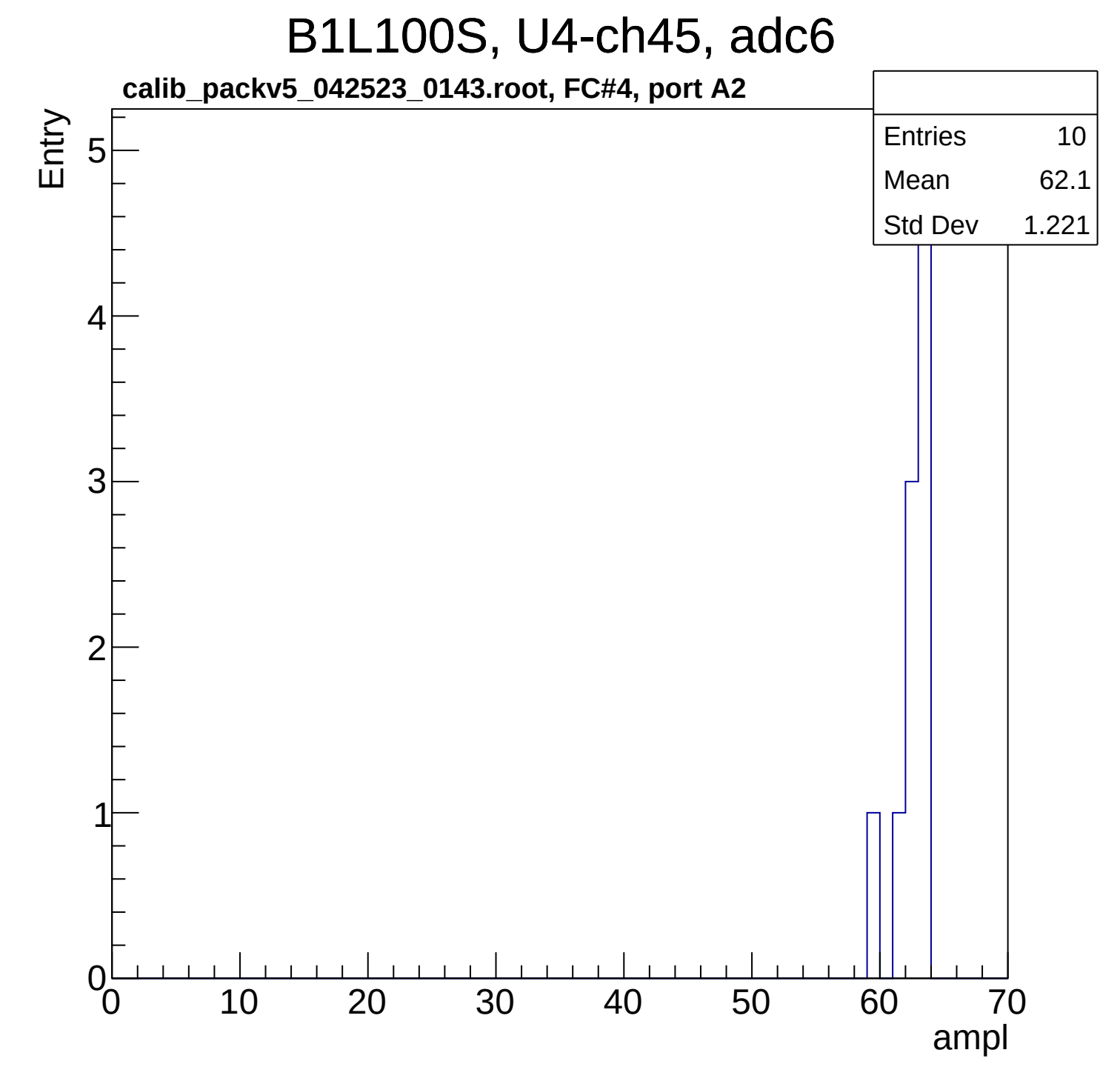

B1L100S, U4-ch45, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 36.61
Std Dev 3.442
Gaus mean : 36.8530
Gaus Width: 3.5195
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

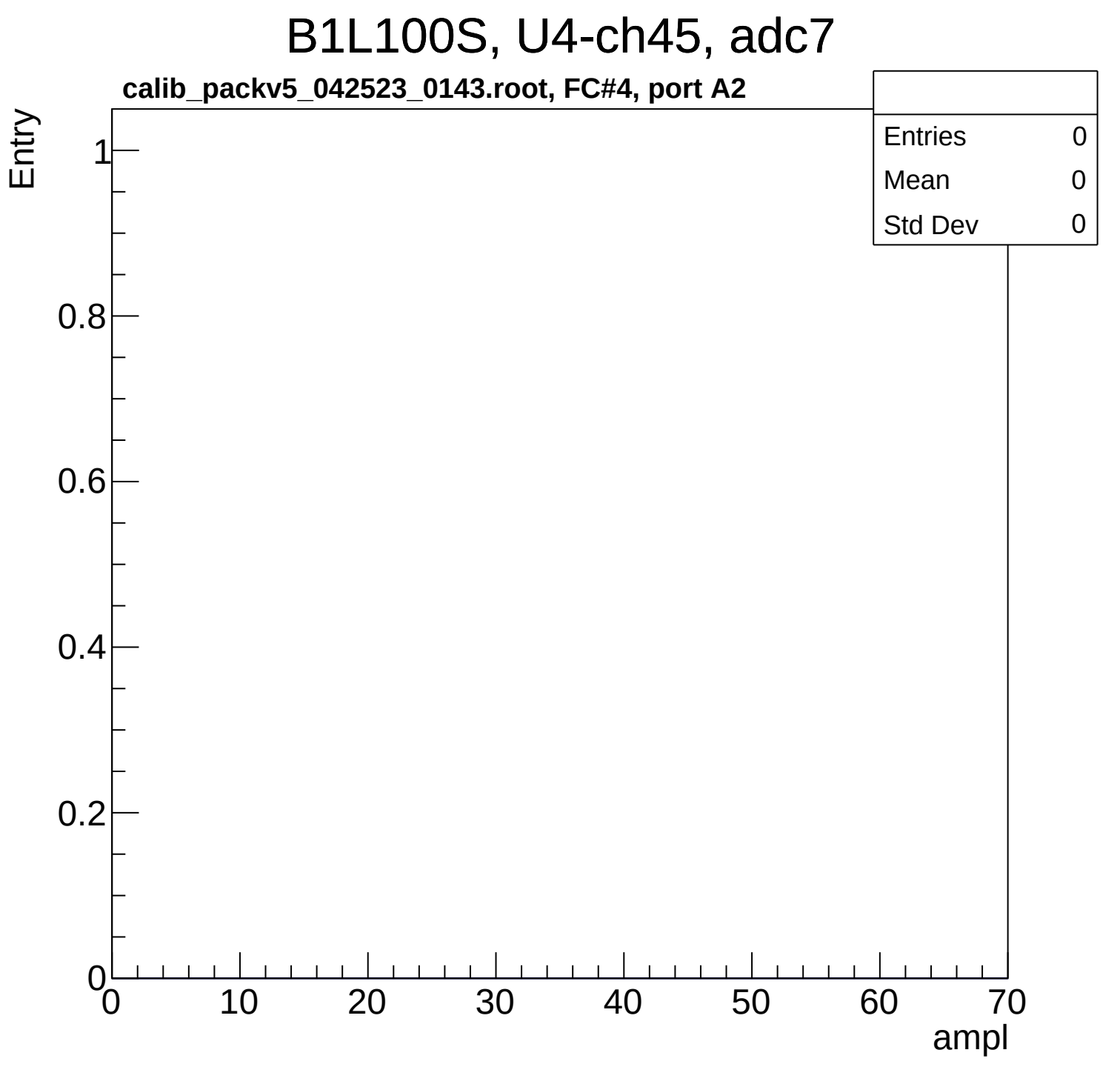

B1L100S, U4-ch45, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 43.49
Std Dev 3.526
Gaus mean : 44.3309
Gaus Width: 3.6836
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

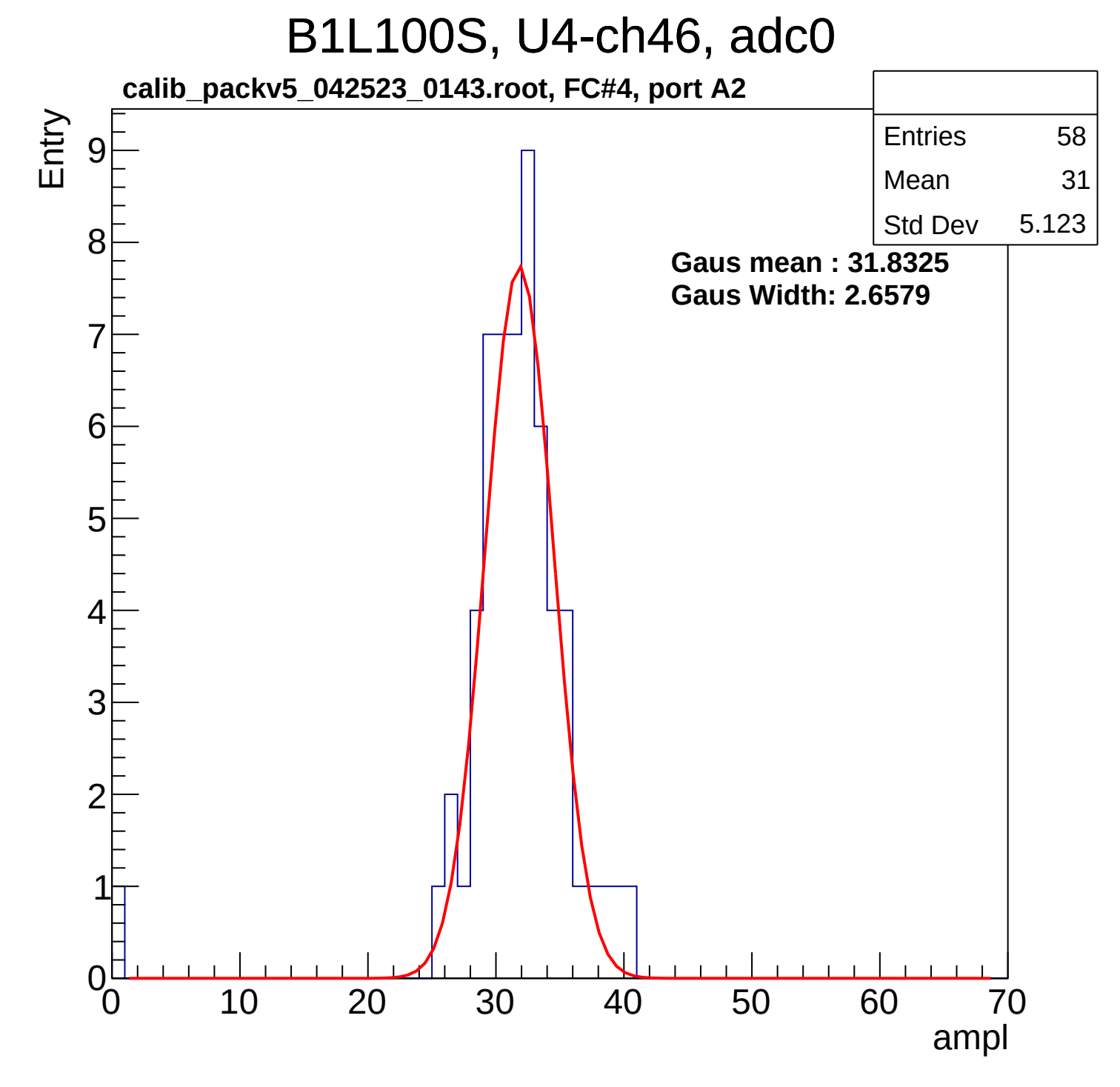

B1L100S, U4-ch45, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 48.67
Std Dev 3.109
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

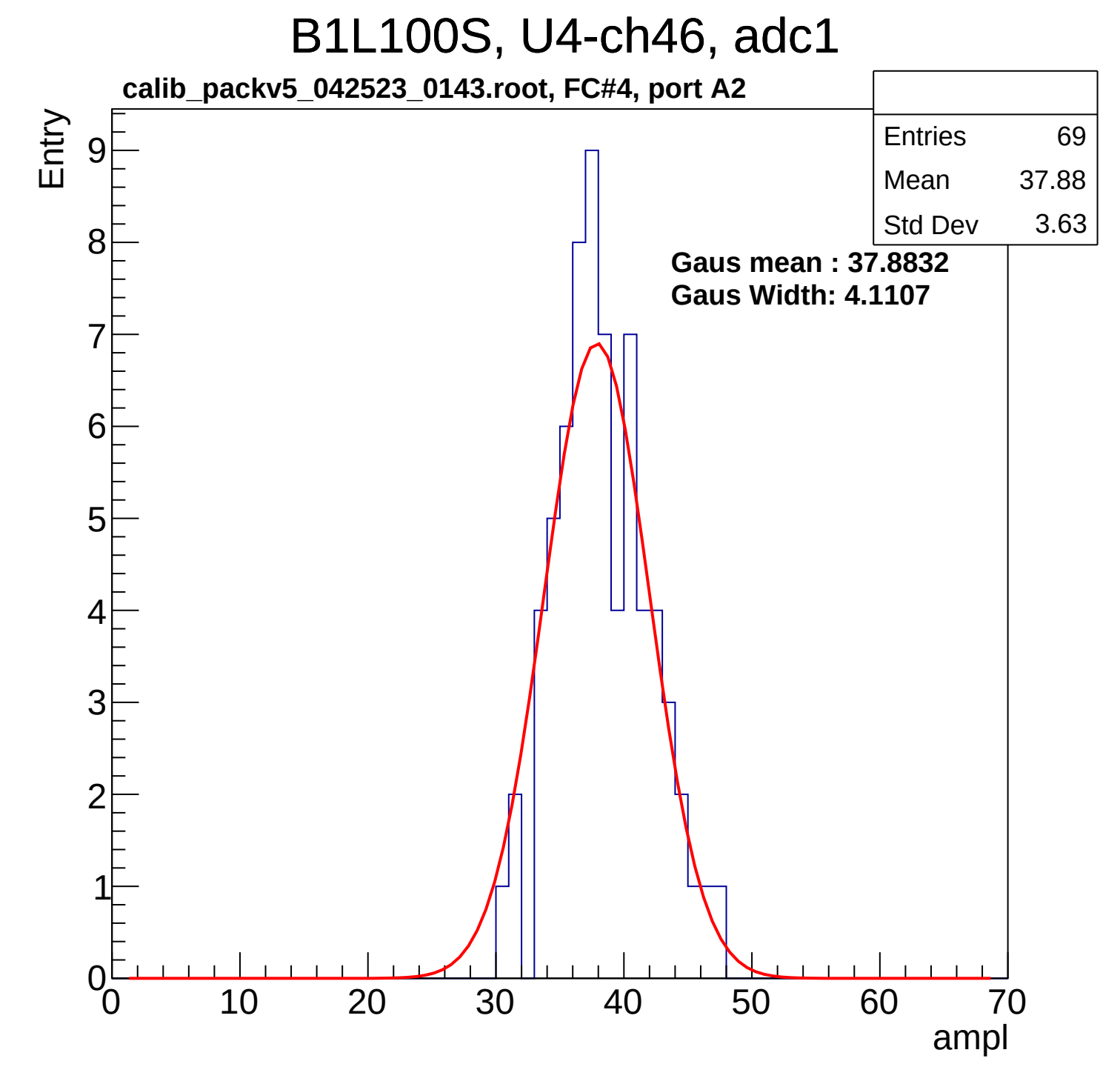

B1L100S, U4-ch45, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 54.51
Std Dev 2.763
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

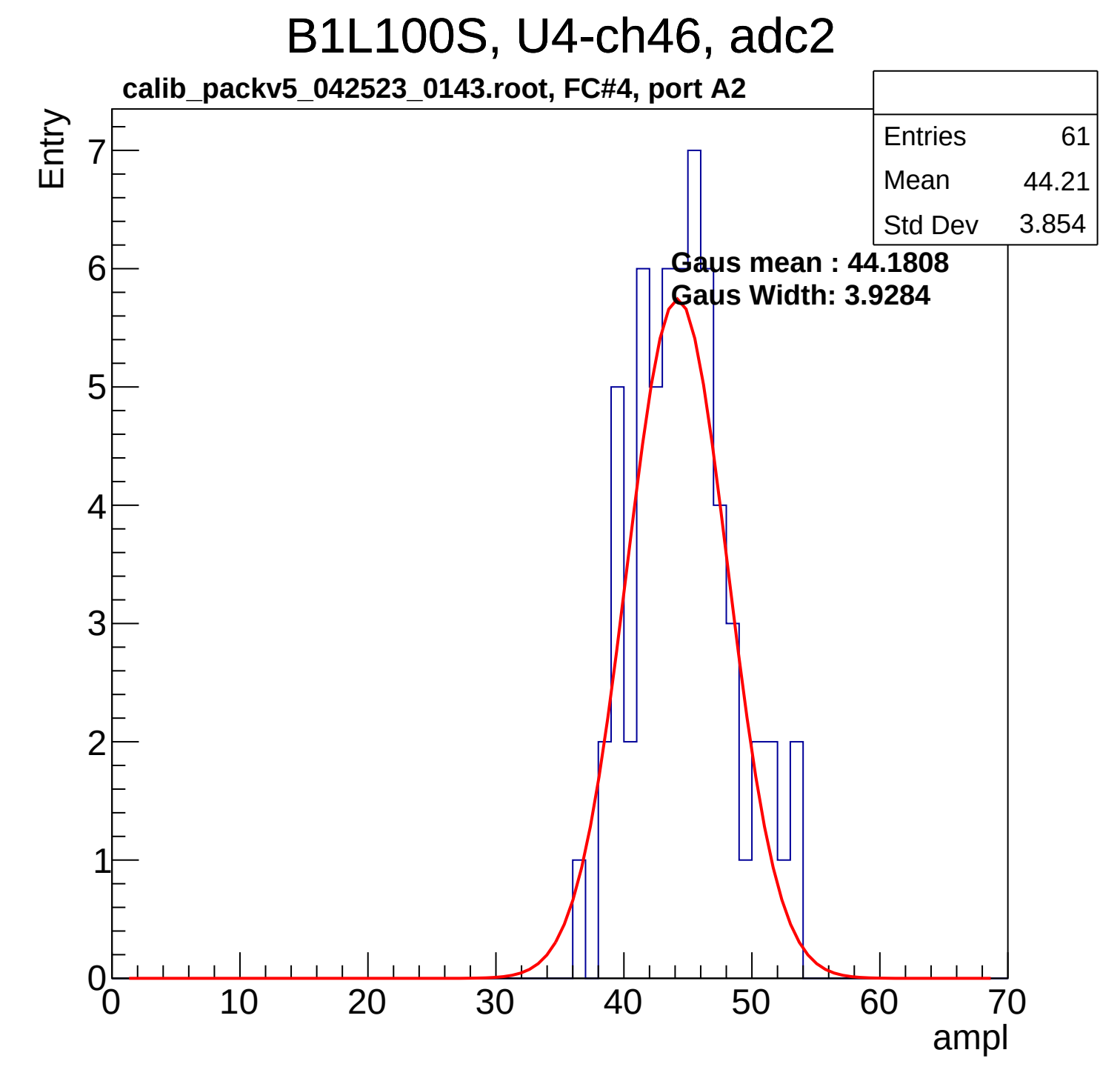

B1L100S, U4-ch45, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 58.58
Std Dev 8.479
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

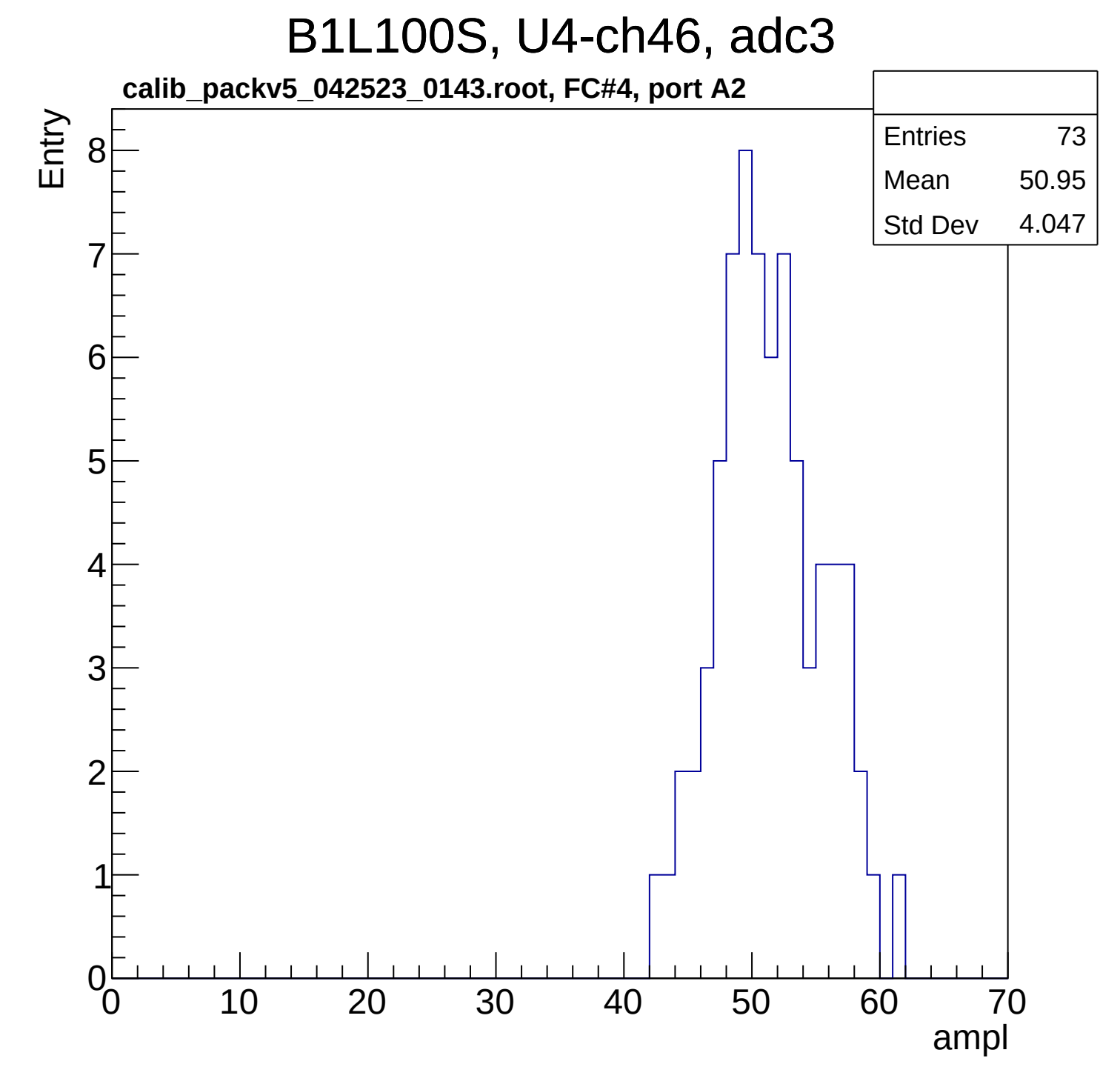

B1L100S, U4-ch45, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 62.1
Std Dev 1.221
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

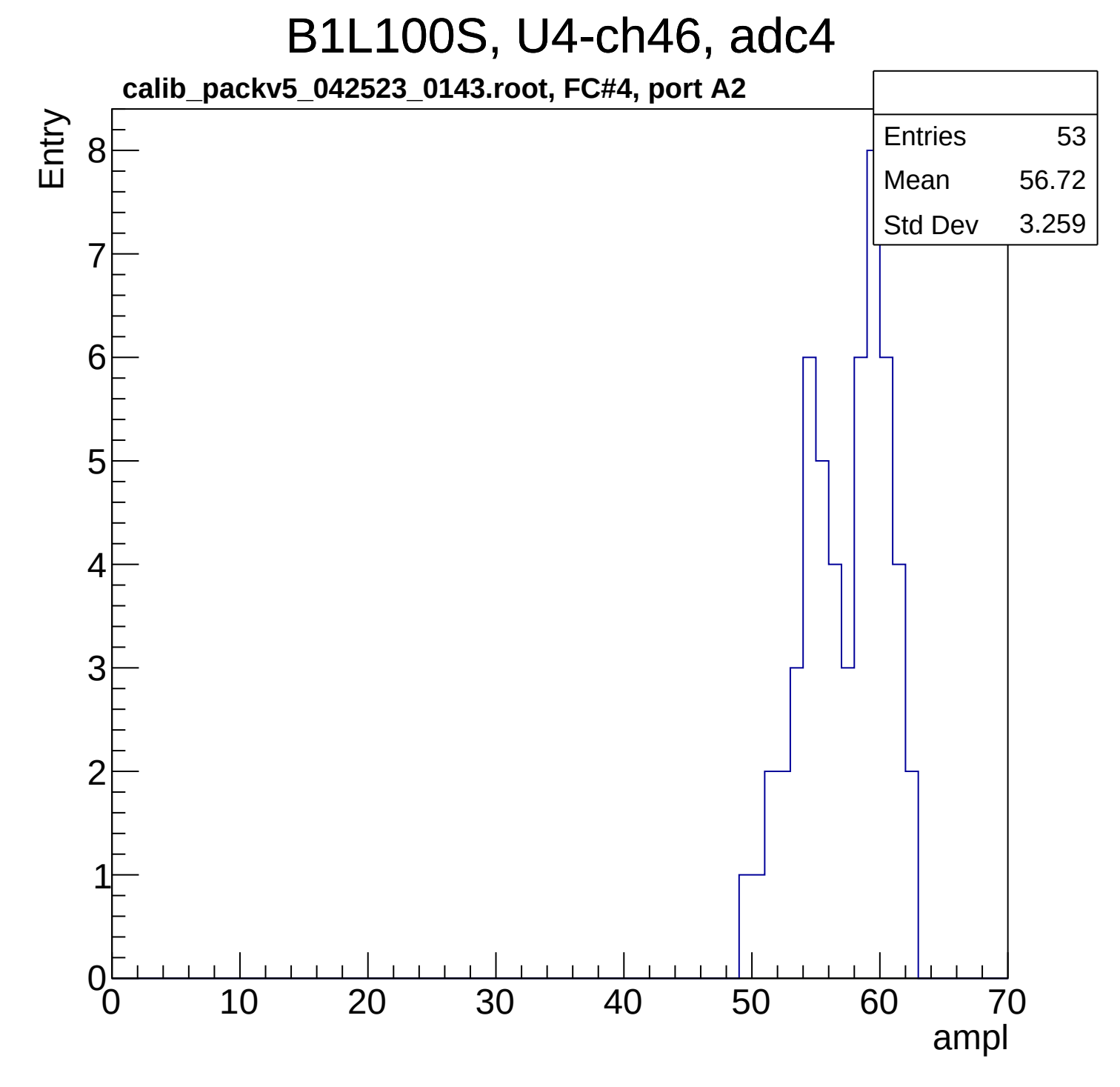

B1L100S, U4-ch45, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

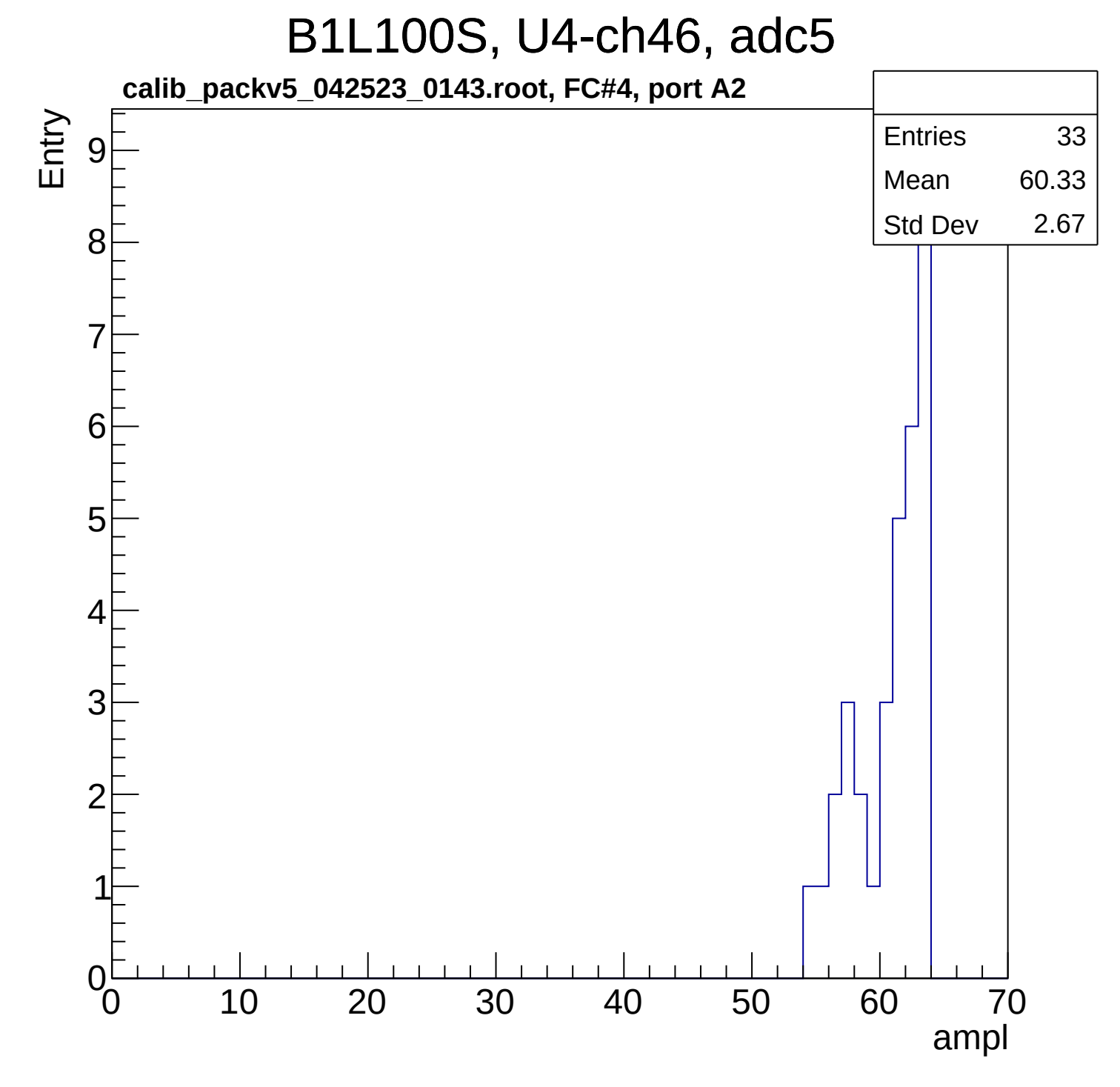

B1L100S, U4-ch46, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 31
Std Dev 5.123
Gaus mean : 31.8325
Gaus Width: 2.6579
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

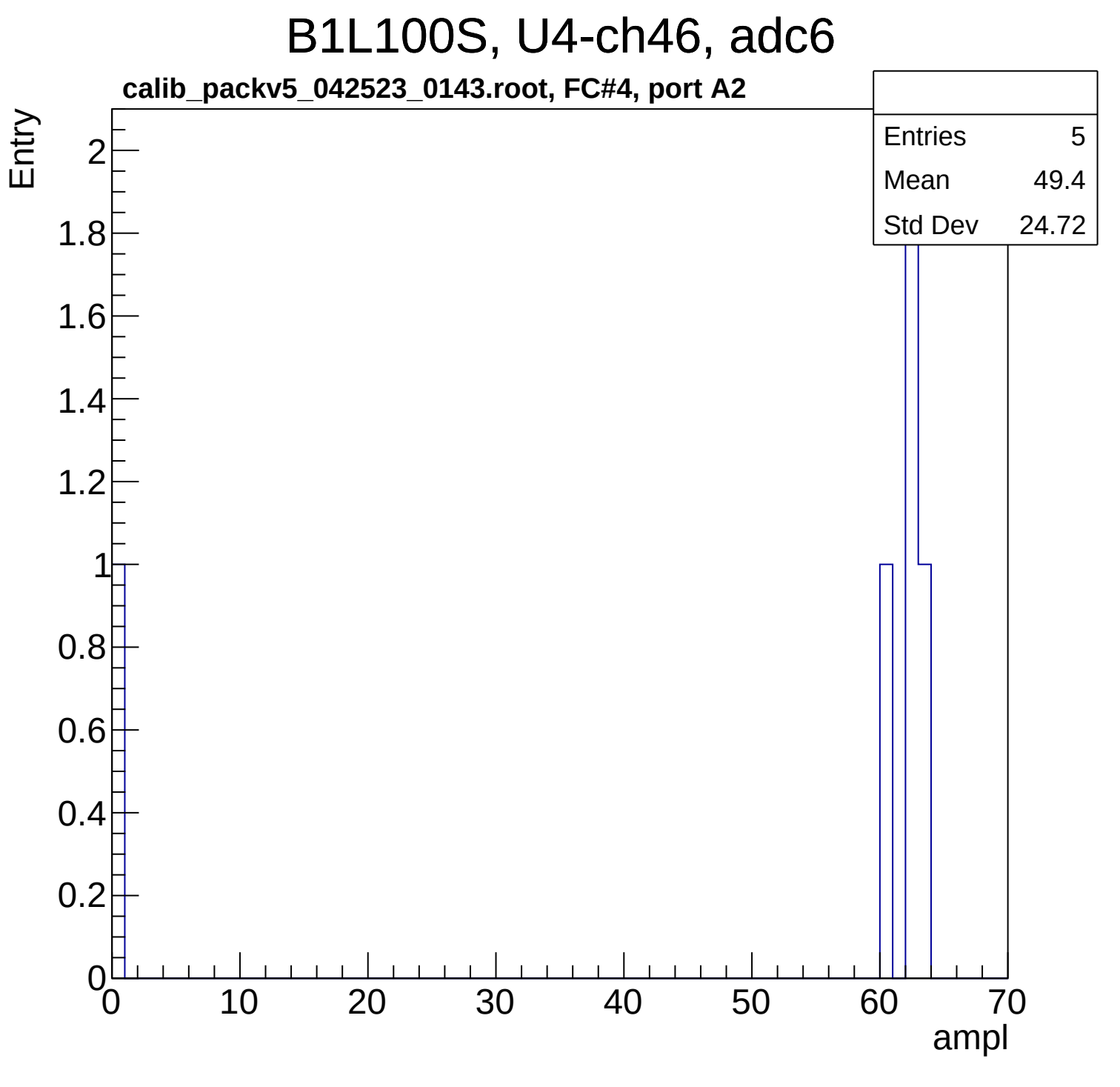

B1L100S, U4-ch46, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 37.88
Std Dev 3.63
Gaus mean : 37.8832
Gaus Width: 4.1107
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

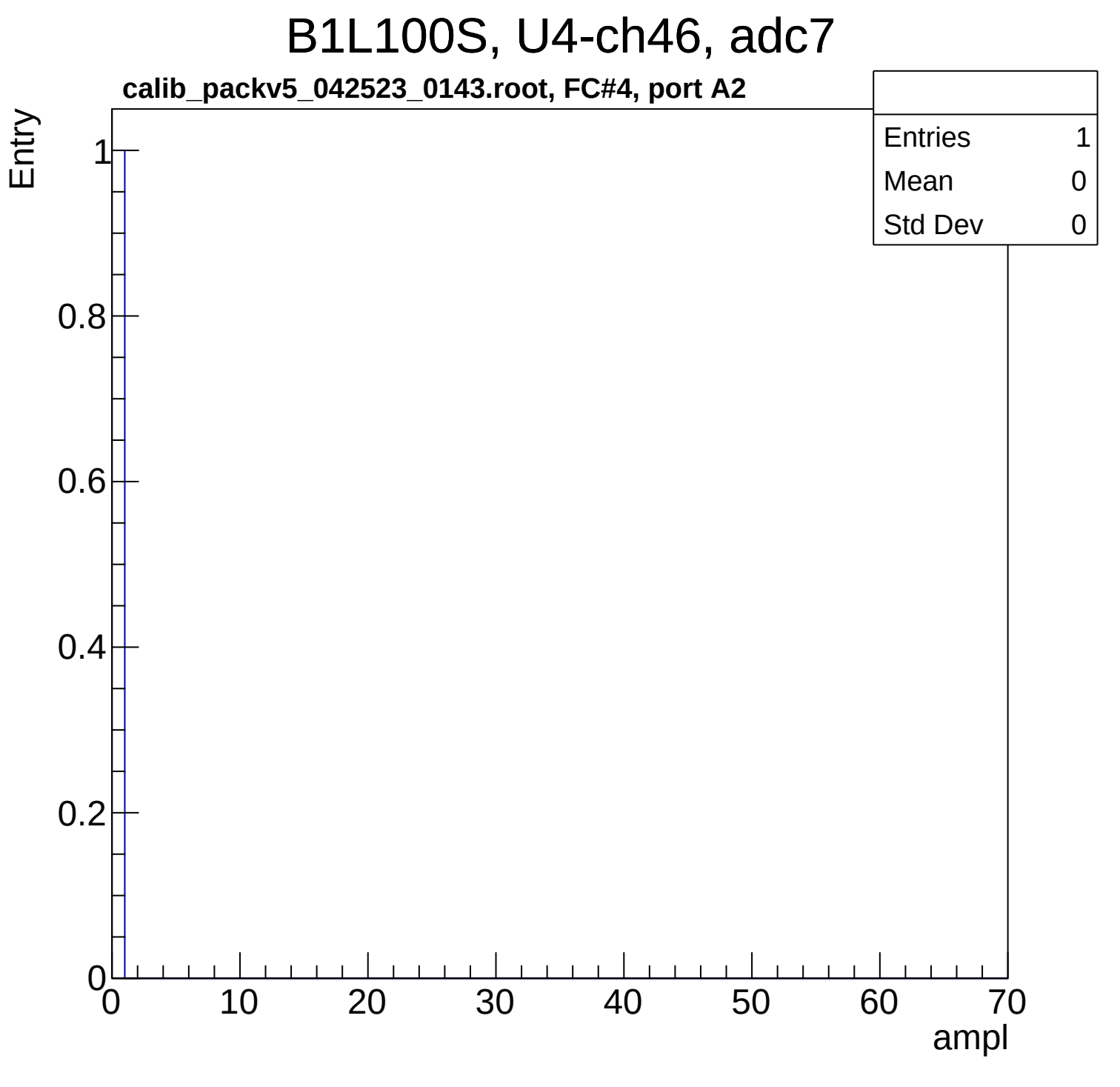

B1L100S, U4-ch46, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 44.21
Std Dev 3.854
Gaus mean : 44.1808
Gaus Width: 3.9284
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

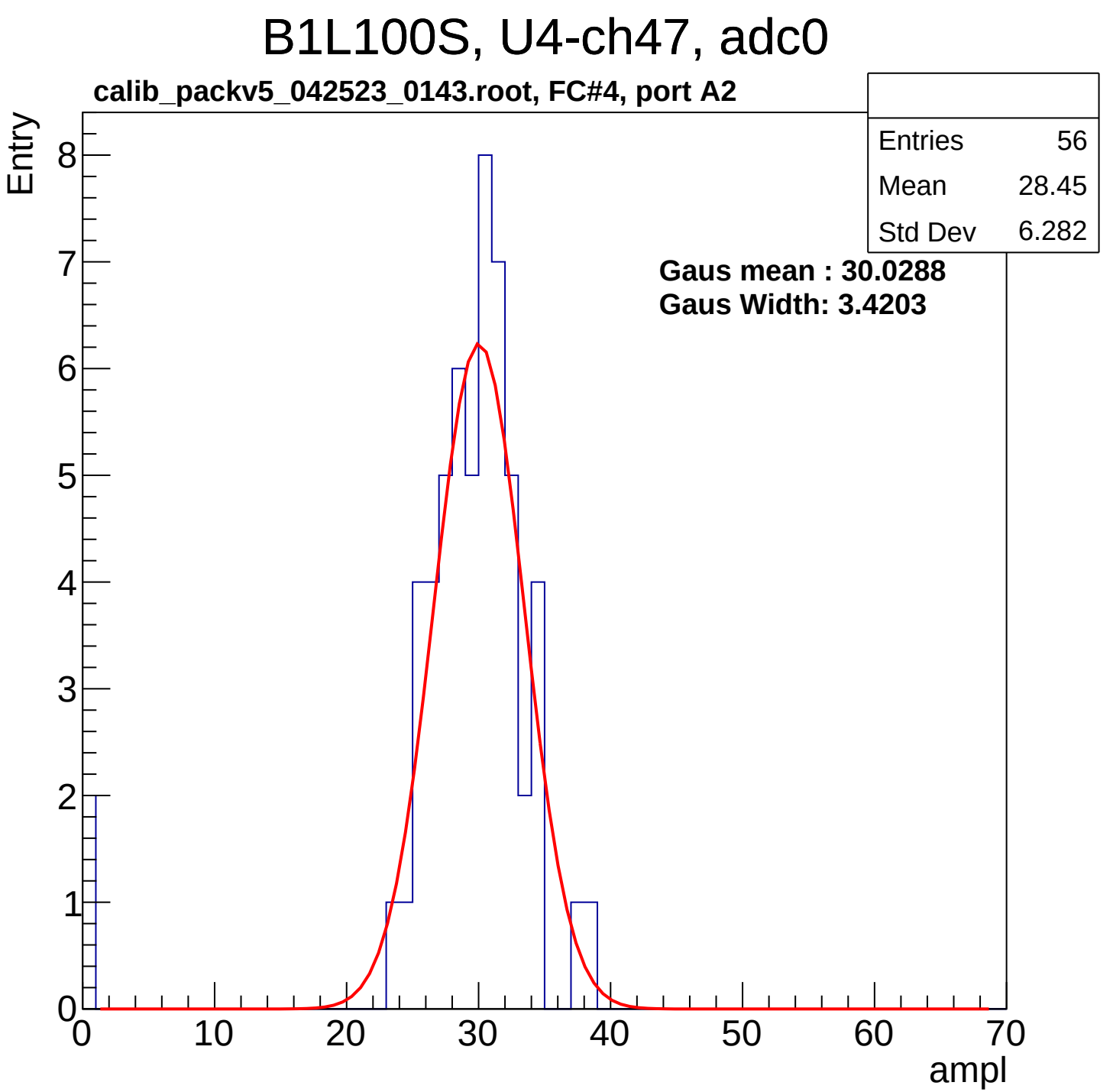

B1L100S, U4-ch46, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 50.95
Std Dev 4.047
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

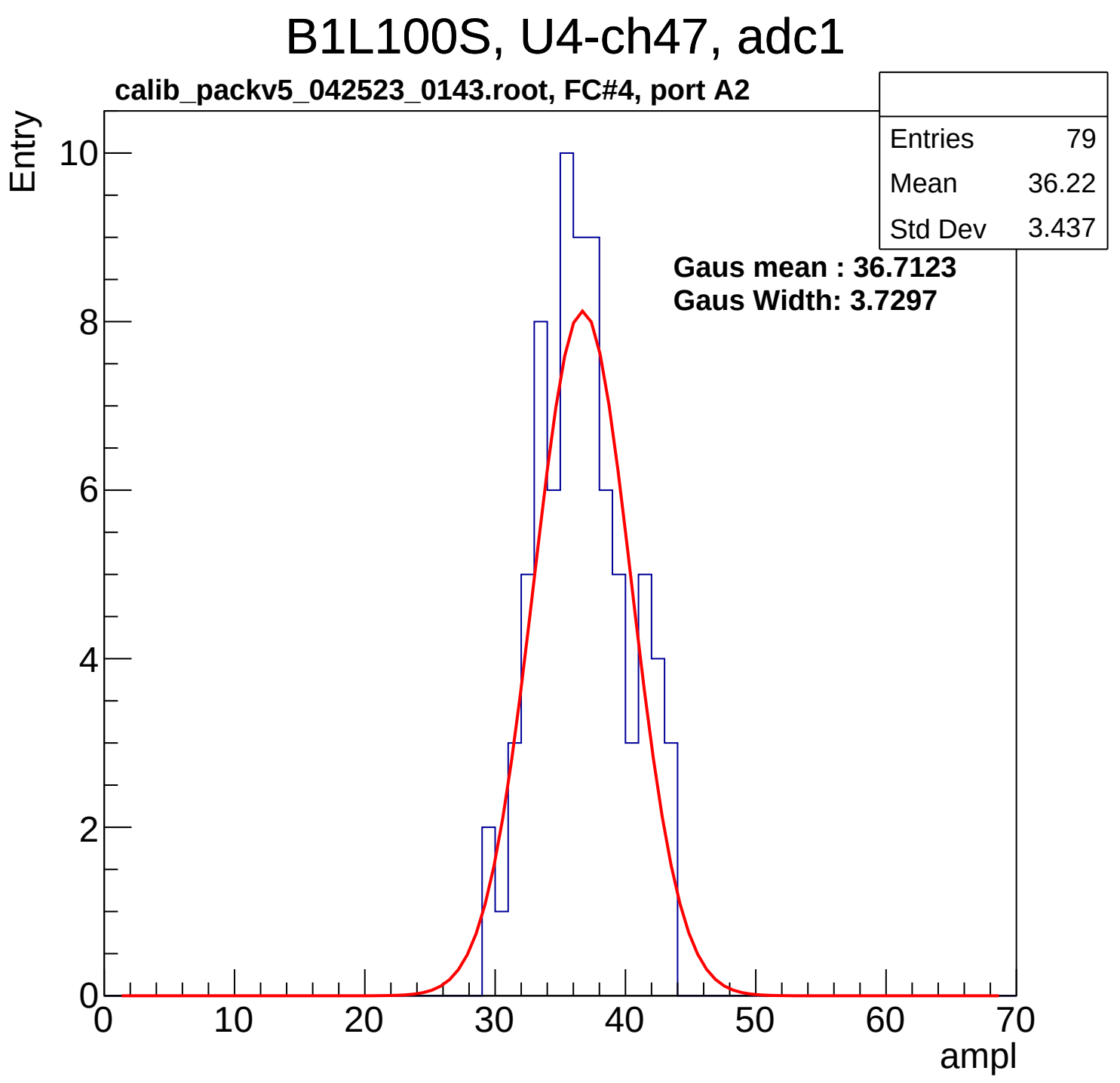

B1L100S, U4-ch46, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 56.72
Std Dev 3.259
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

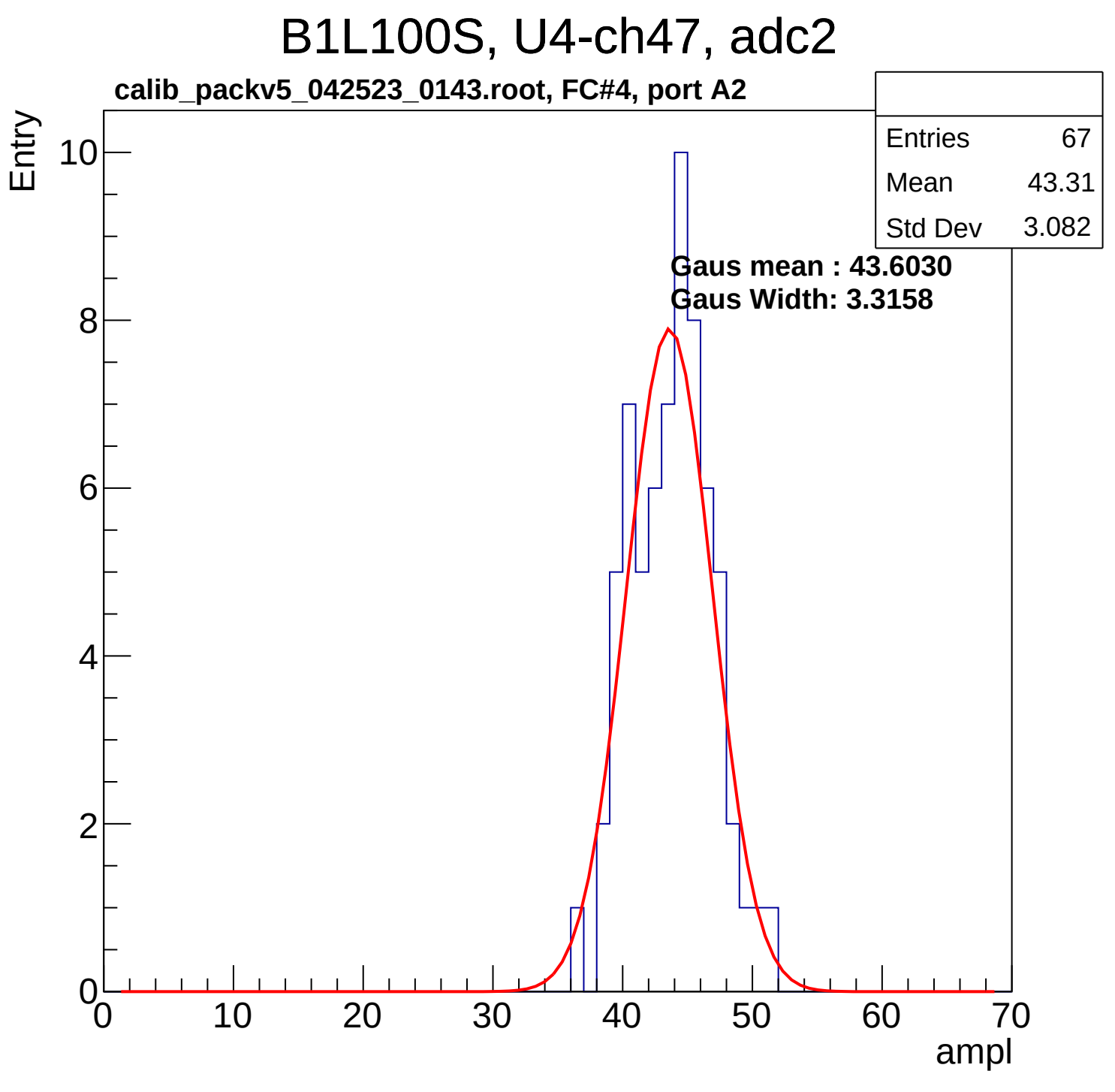

B1L100S, U4-ch46, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 33
Mean 60.33
Std Dev 2.67
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

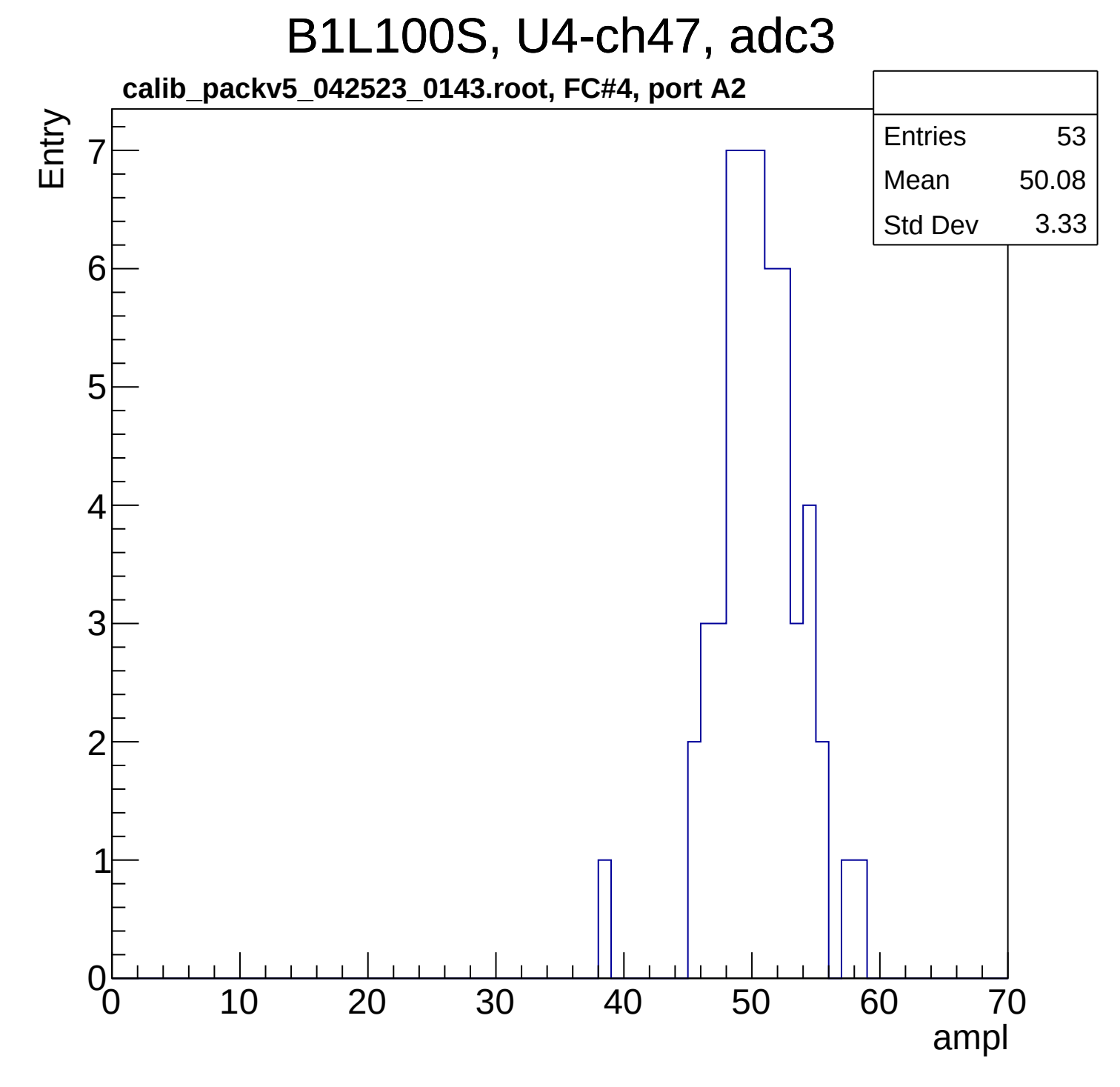

B1L100S, U4-ch46, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 5
Mean 49.4
Std Dev 24.72
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

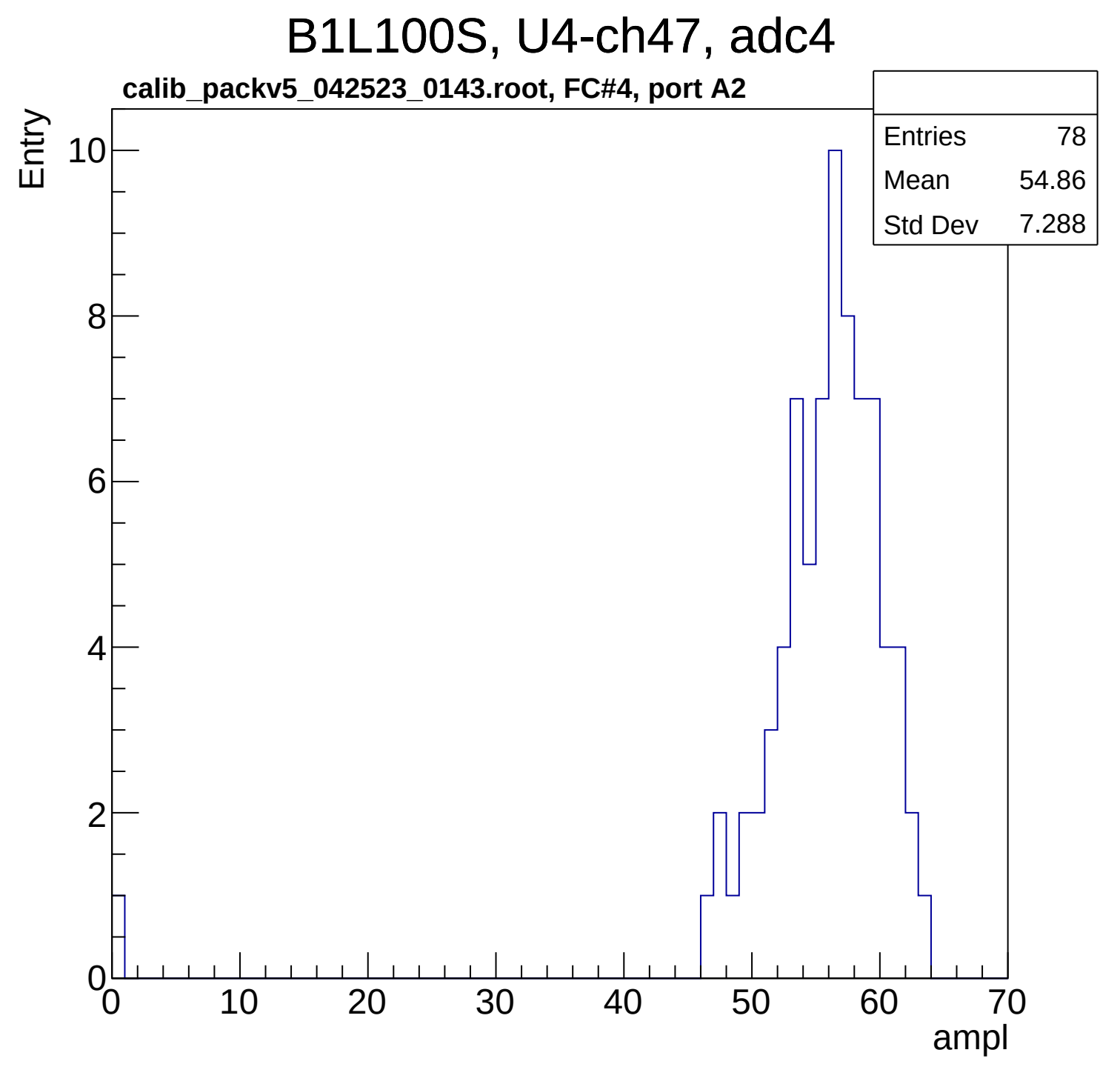

B1L100S, U4-ch46, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

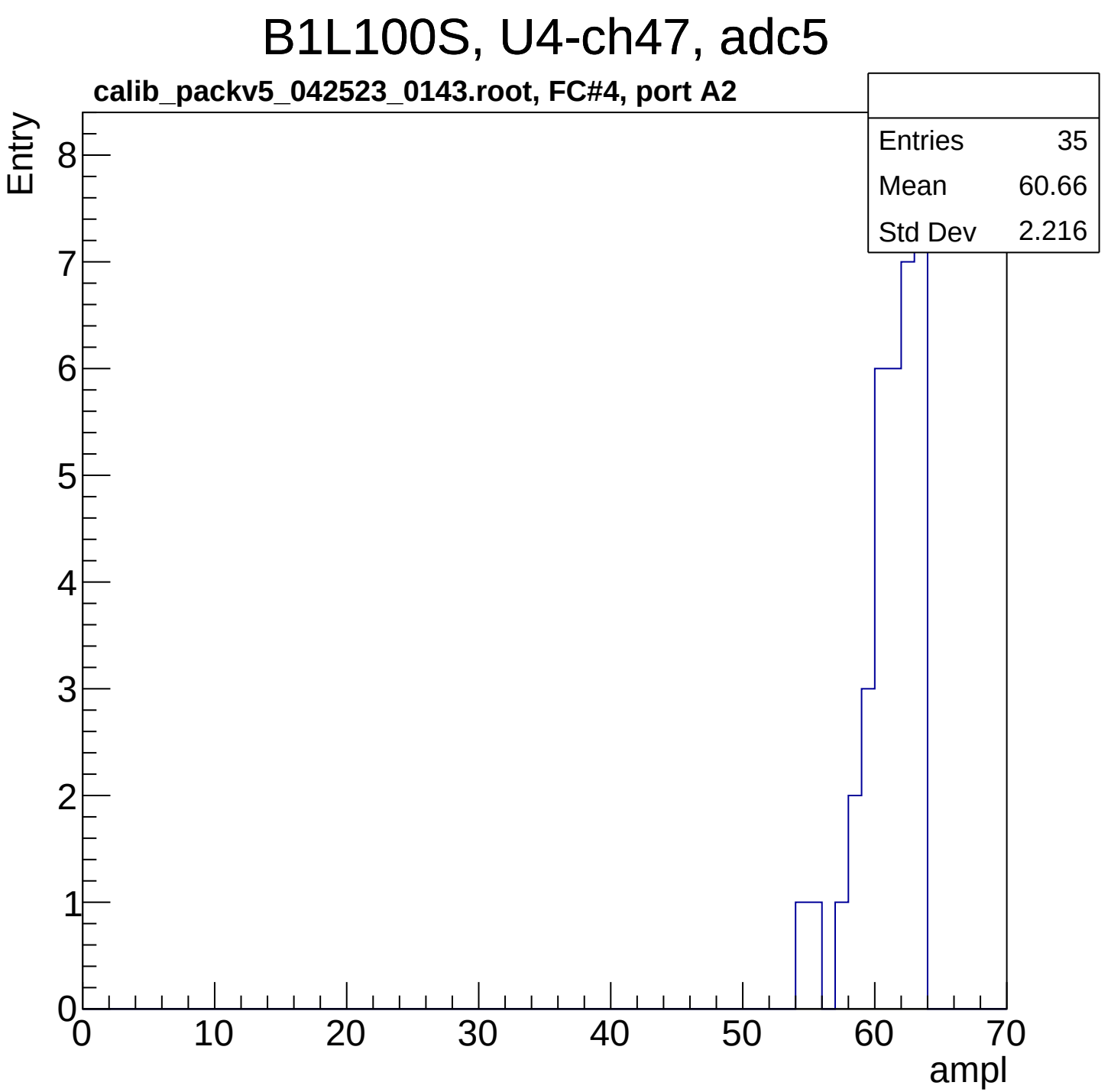

B1L100S, U4-ch47, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 28.45
Std Dev 6.282
Gaus mean : 30.0288
Gaus Width: 3.4203
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

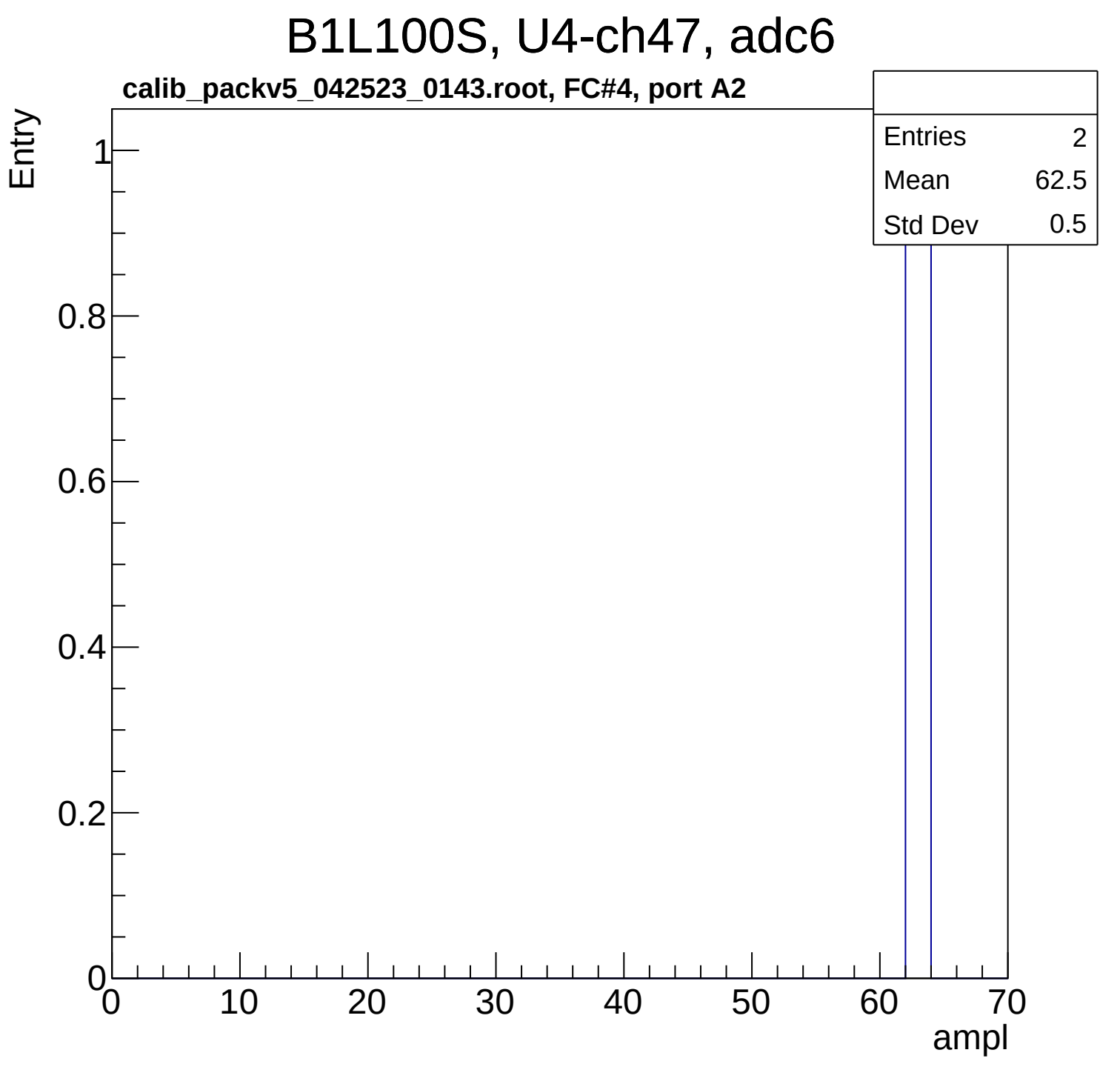

B1L100S, U4-ch47, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 36.22
Std Dev 3.437
Gaus mean : 36.7123
Gaus Width: 3.7297
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

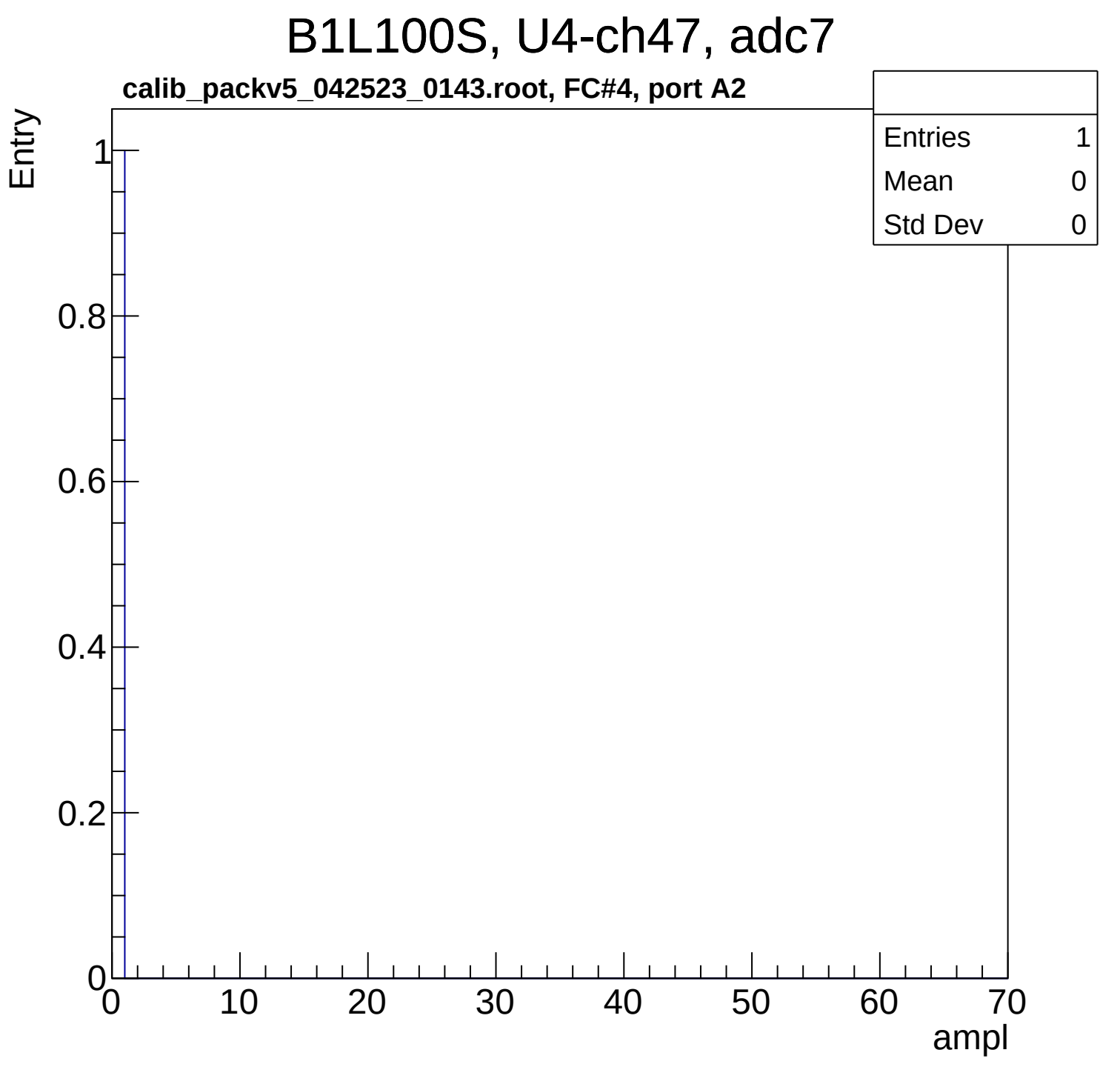

B1L100S, U4-ch47, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 43.31
Std Dev 3.082
Gaus mean : 43.6030
Gaus Width: 3.3158
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

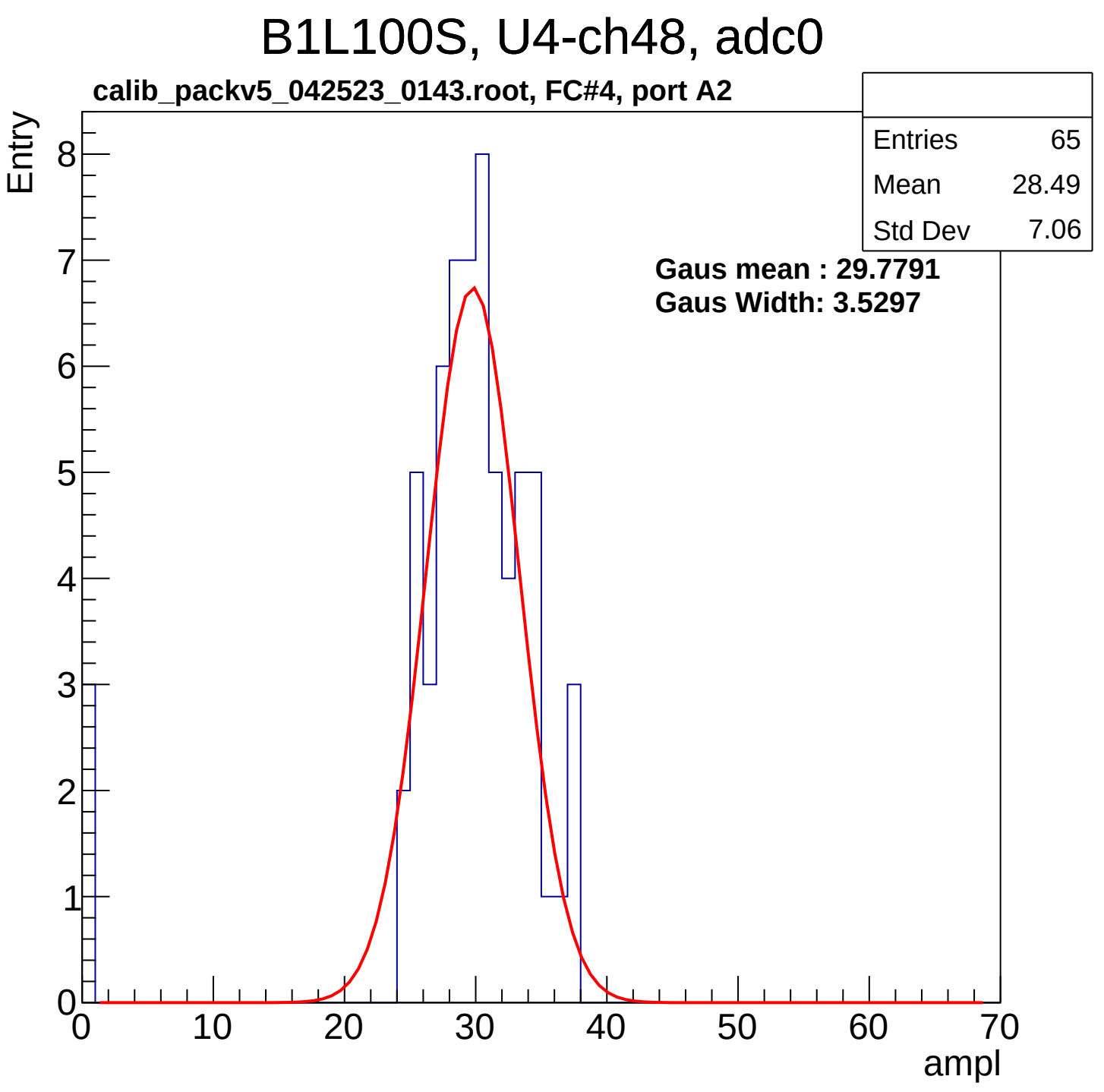

B1L100S, U4-ch47, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 50.08
Std Dev 3.33
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

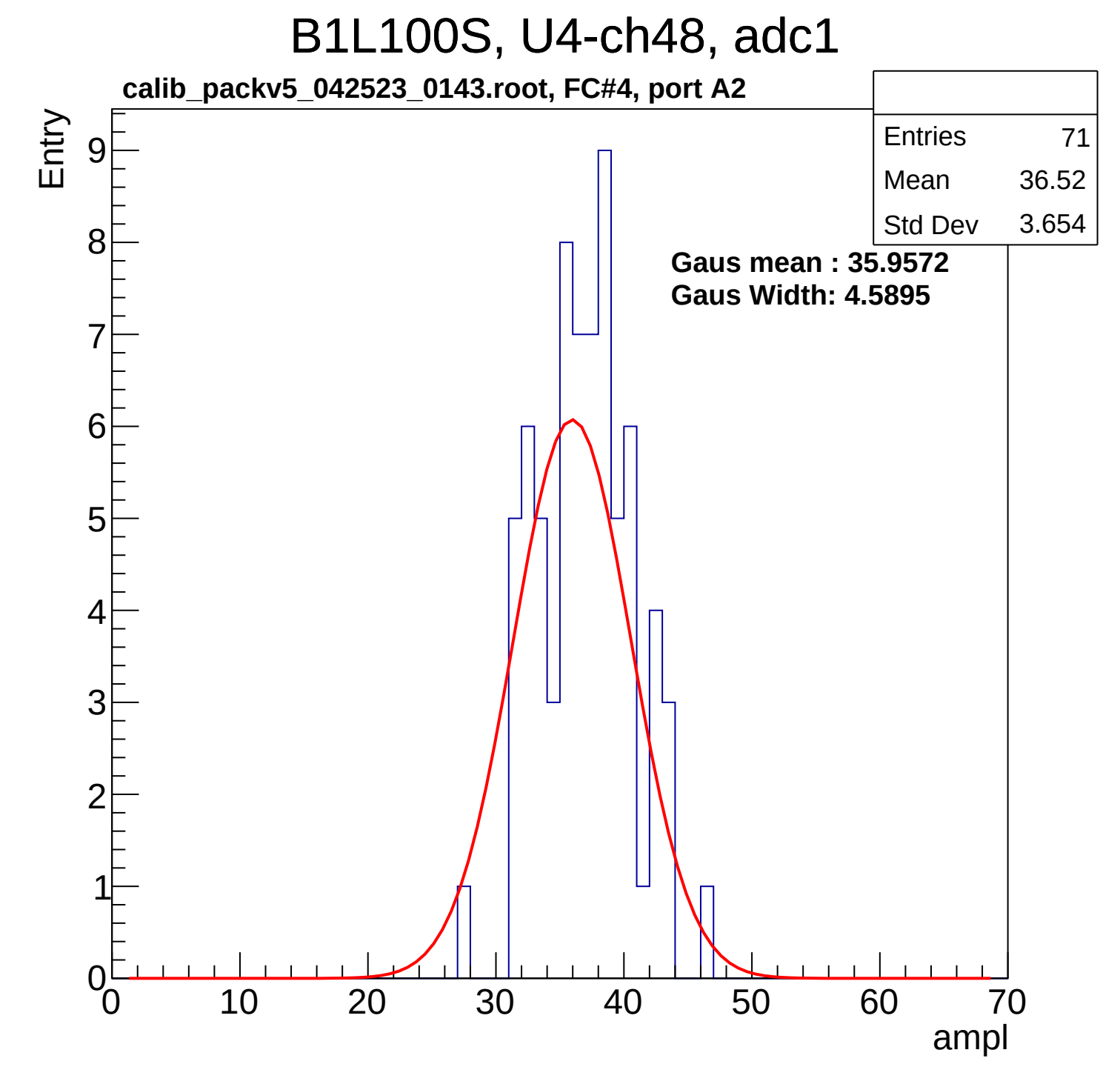

B1L100S, U4-ch47, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 54.86
Std Dev 7.288
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

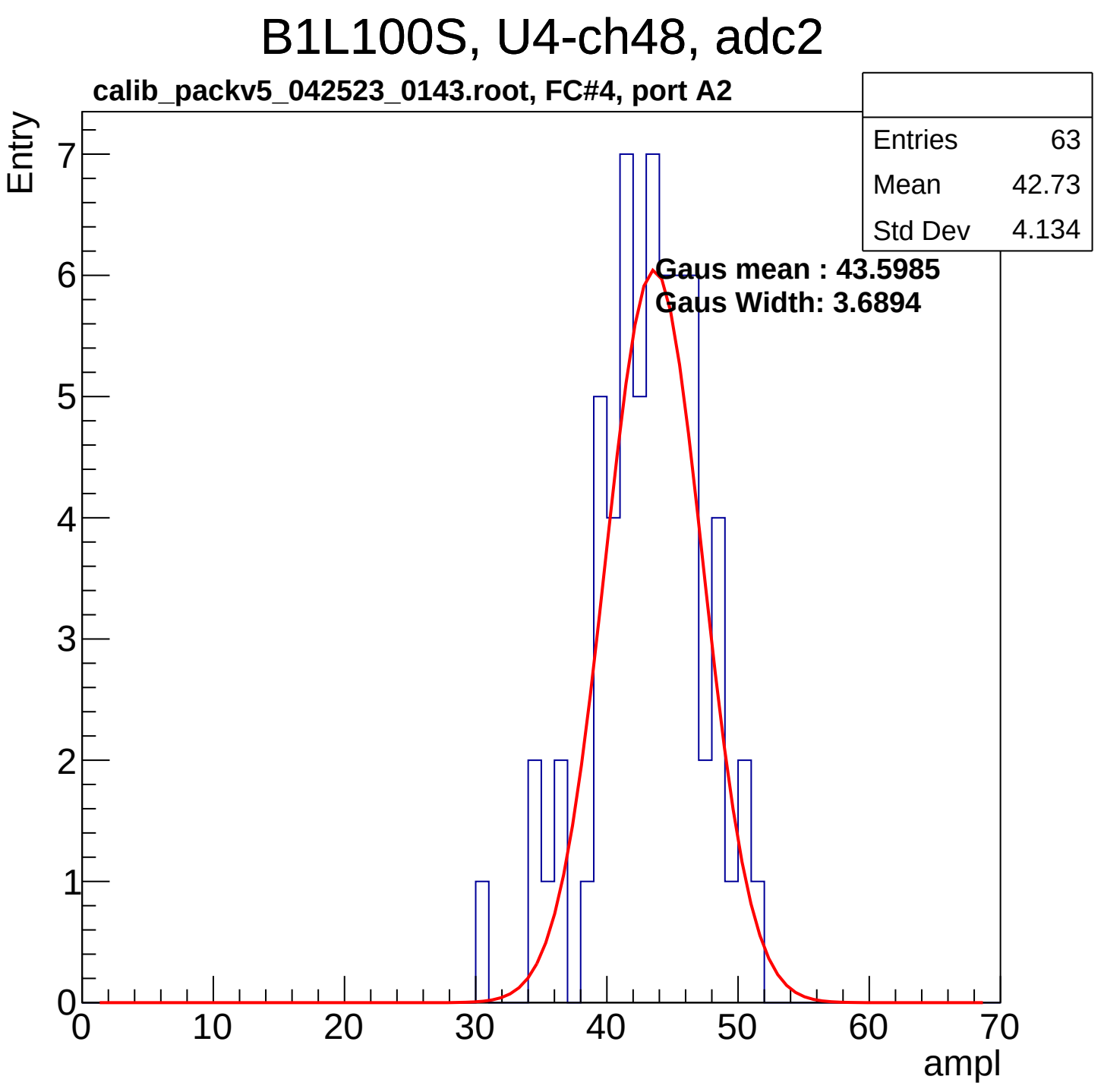

B1L100S, U4-ch47, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 35
Mean 60.66
Std Dev 2.216
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

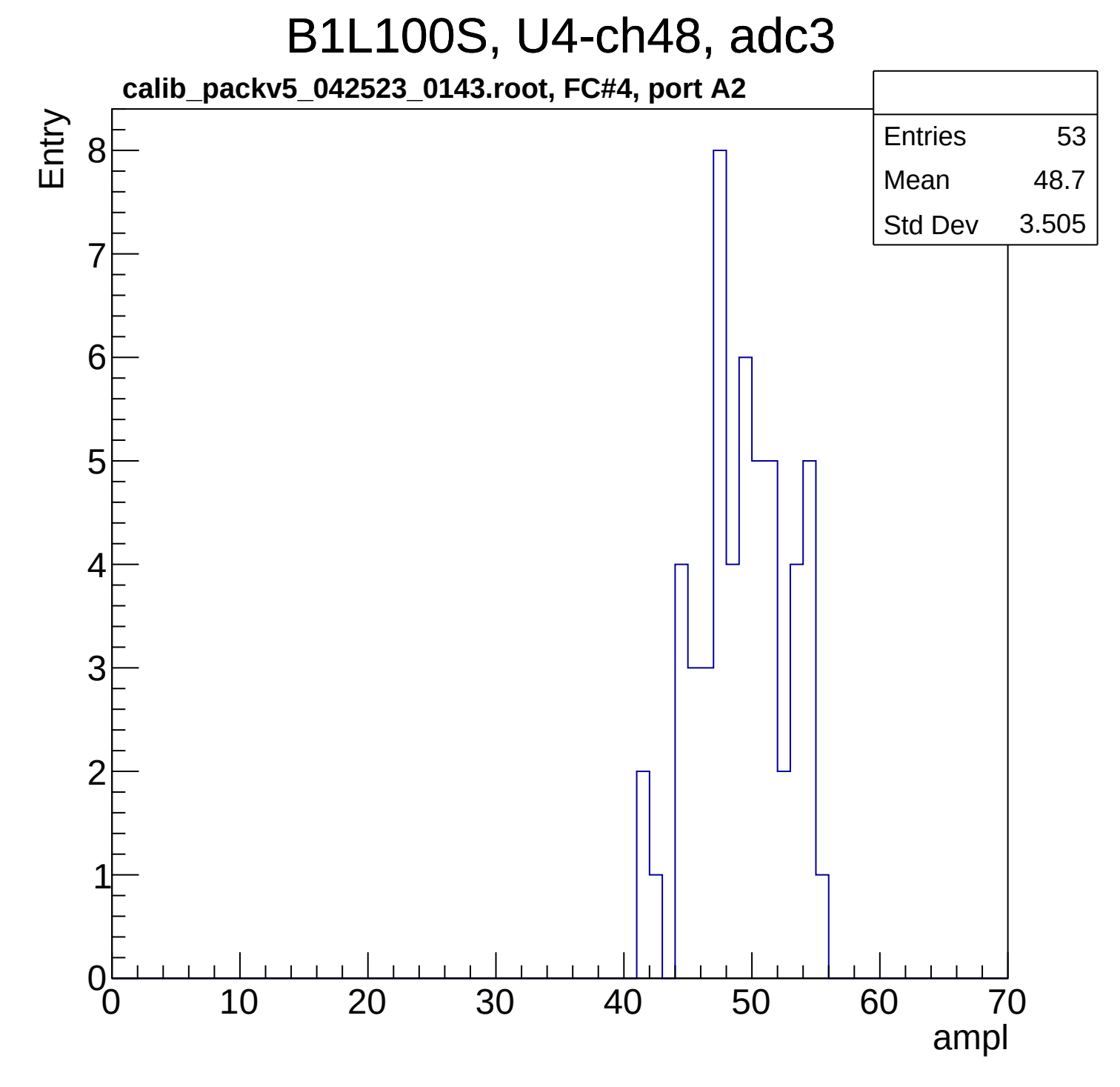

B1L100S, U4-ch47, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

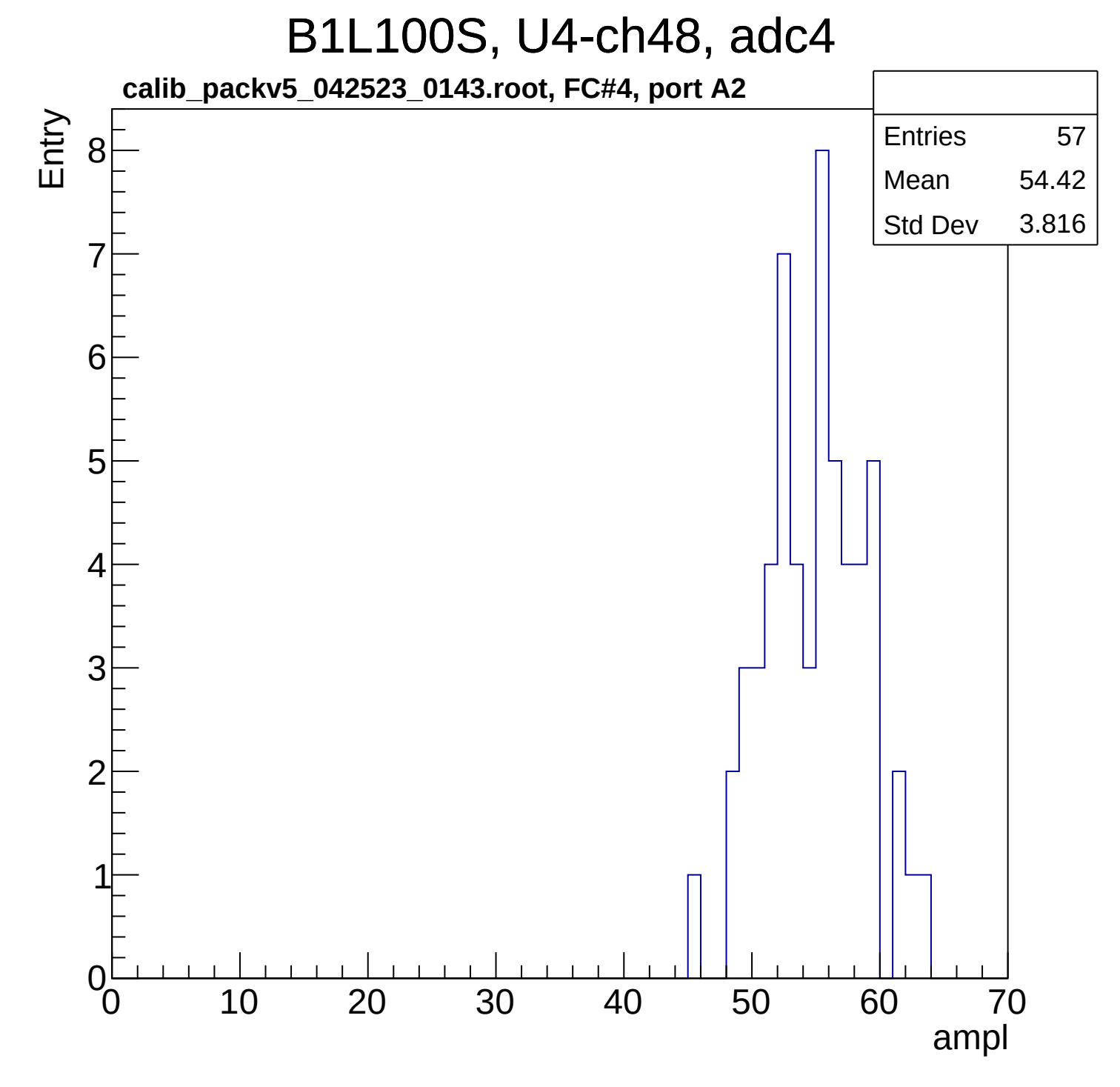

B1L100S, U4-ch47, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

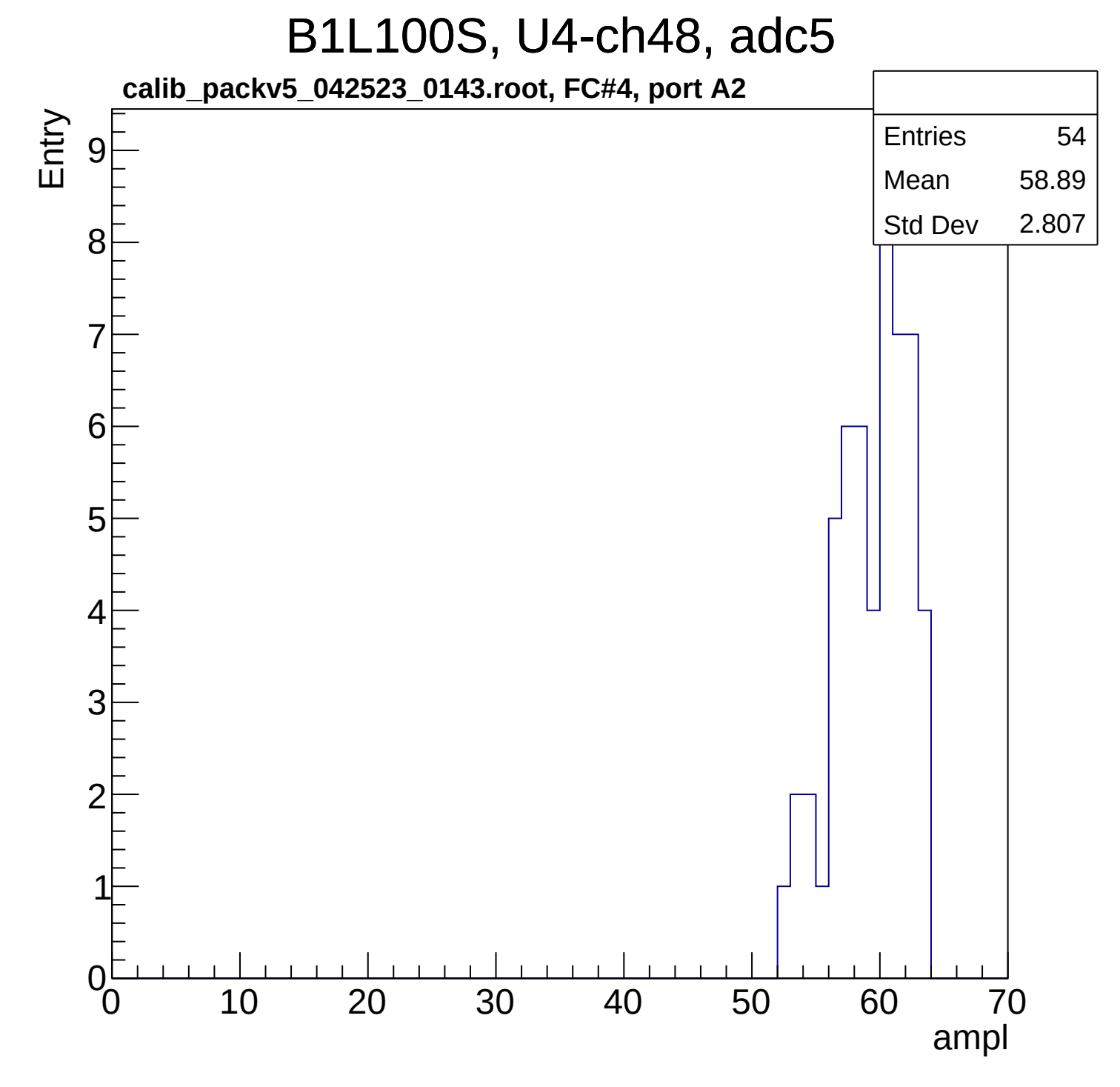

B1L100S, U4-ch48, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 28.49
Std Dev 7.06
Gaus mean : 29.7791
Gaus Width: 3.5297
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

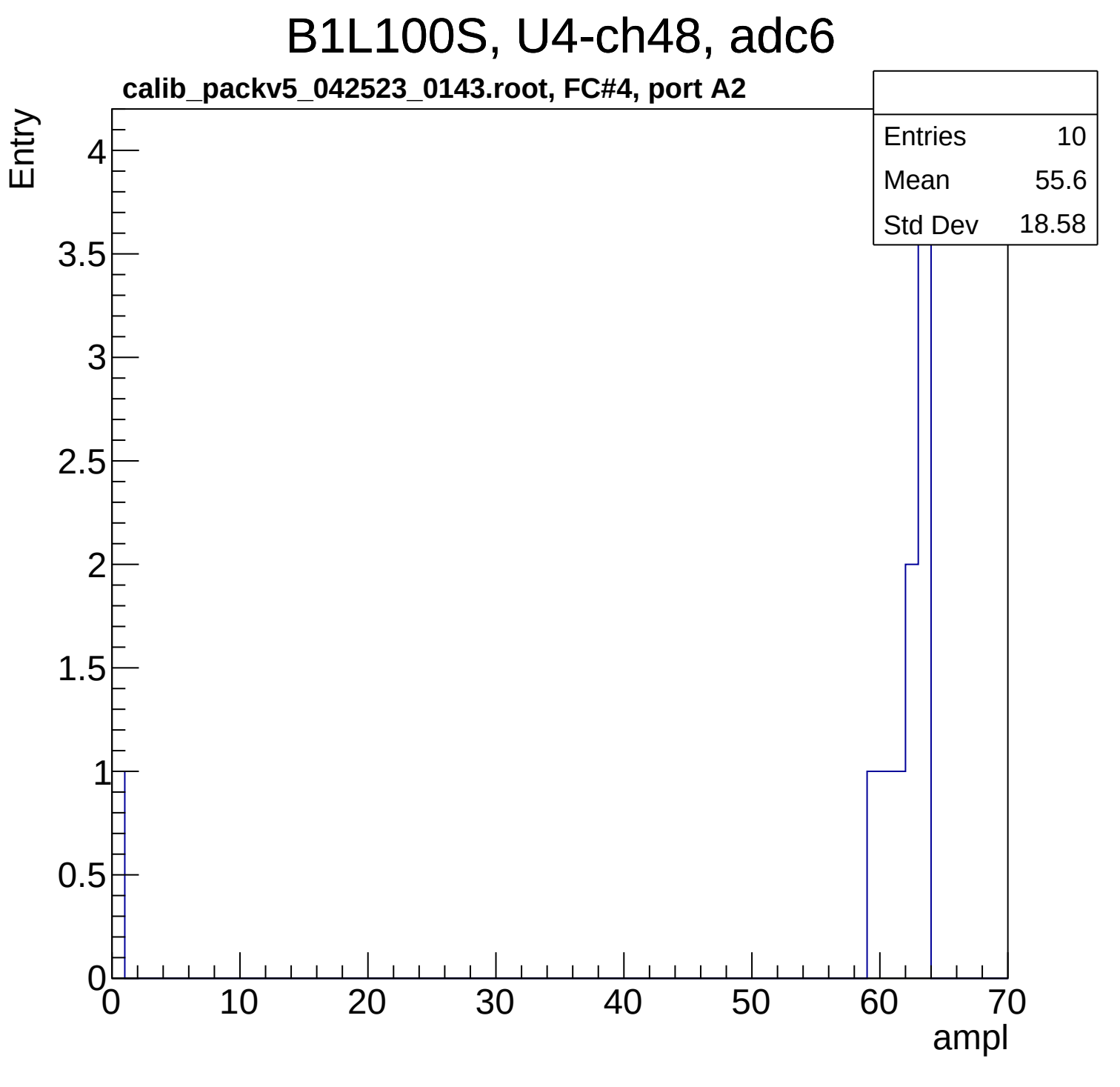

B1L100S, U4-ch48, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 36.52
Std Dev 3.654
Gaus mean : 35.9572
Gaus Width: 4.5895
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

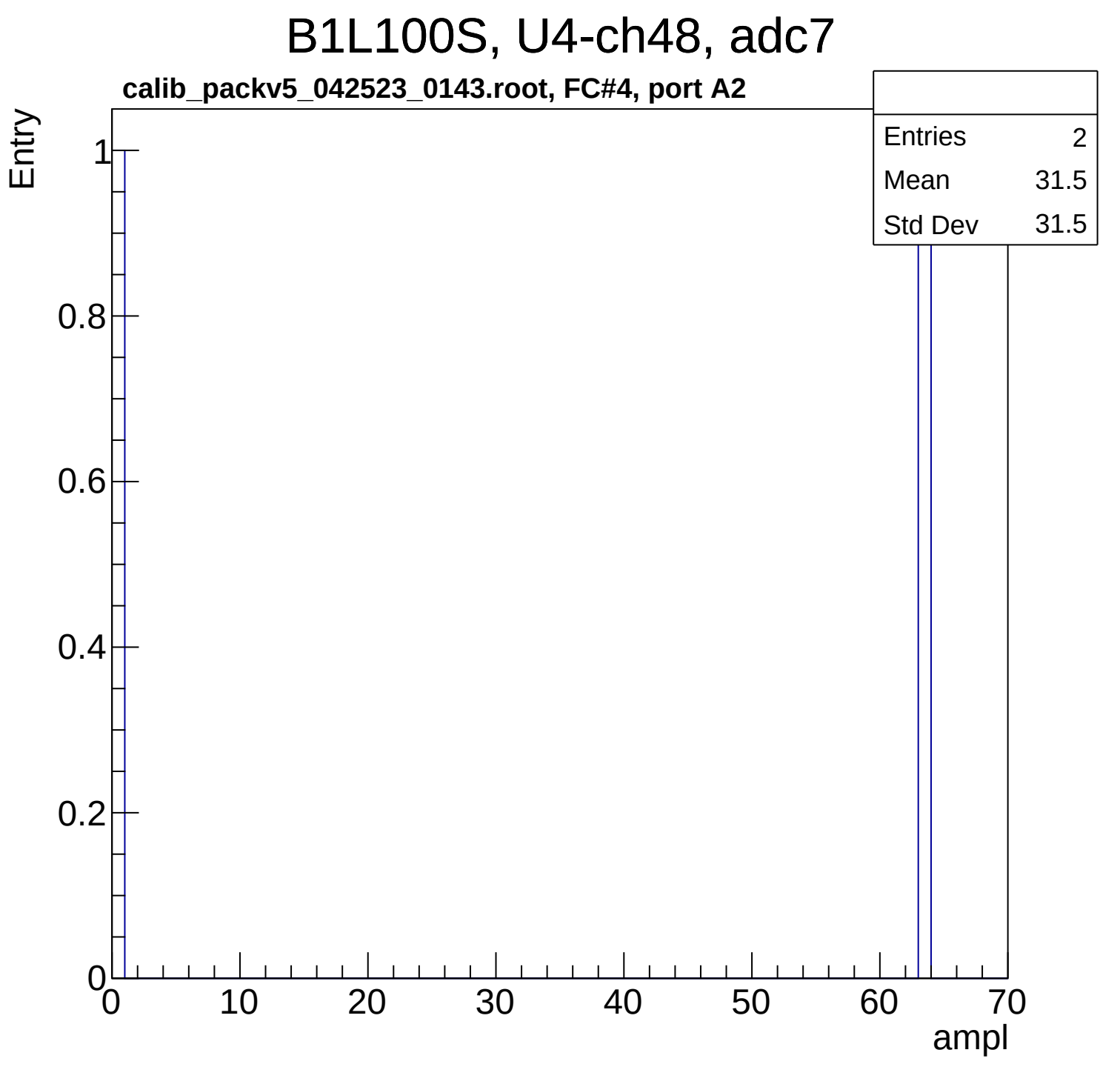

B1L100S, U4-ch48, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 42.73
Std Dev 4.134
Gaus mean : 43.5985
Gaus Width: 3.6894
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

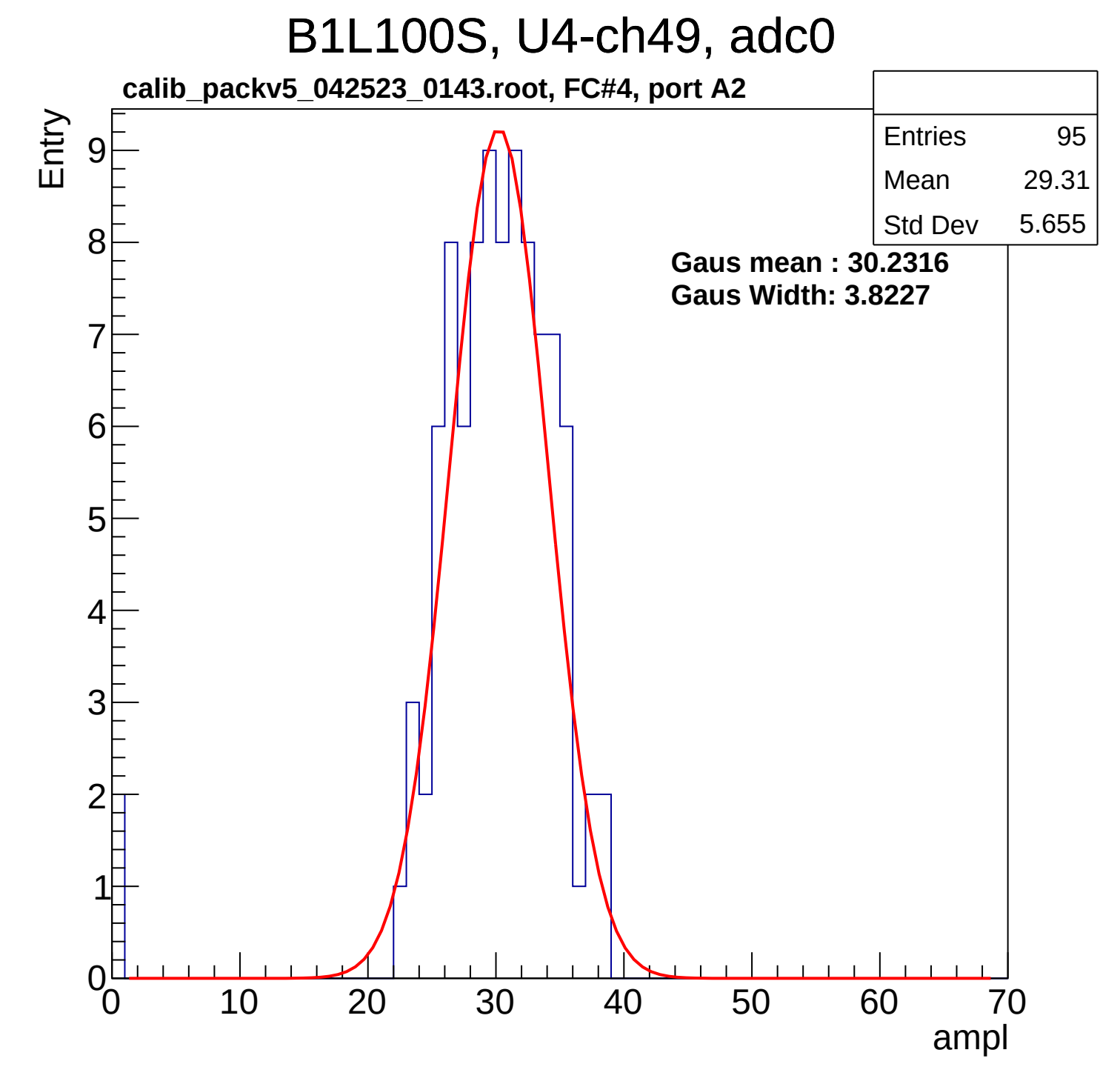

B1L100S, U4-ch48, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 48.7
Std Dev 3.505
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

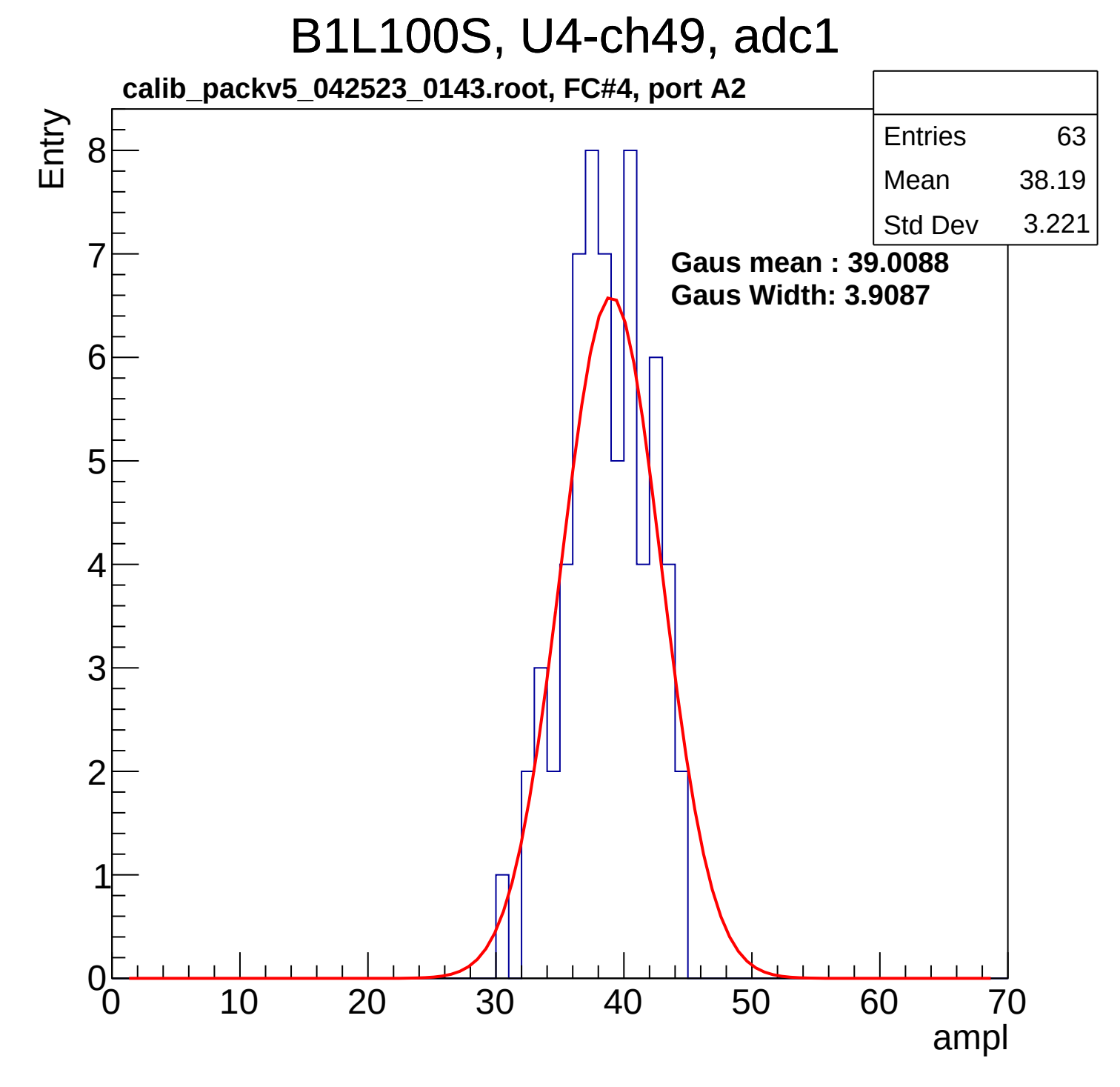

B1L100S, U4-ch48, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 54.42
Std Dev 3.816
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

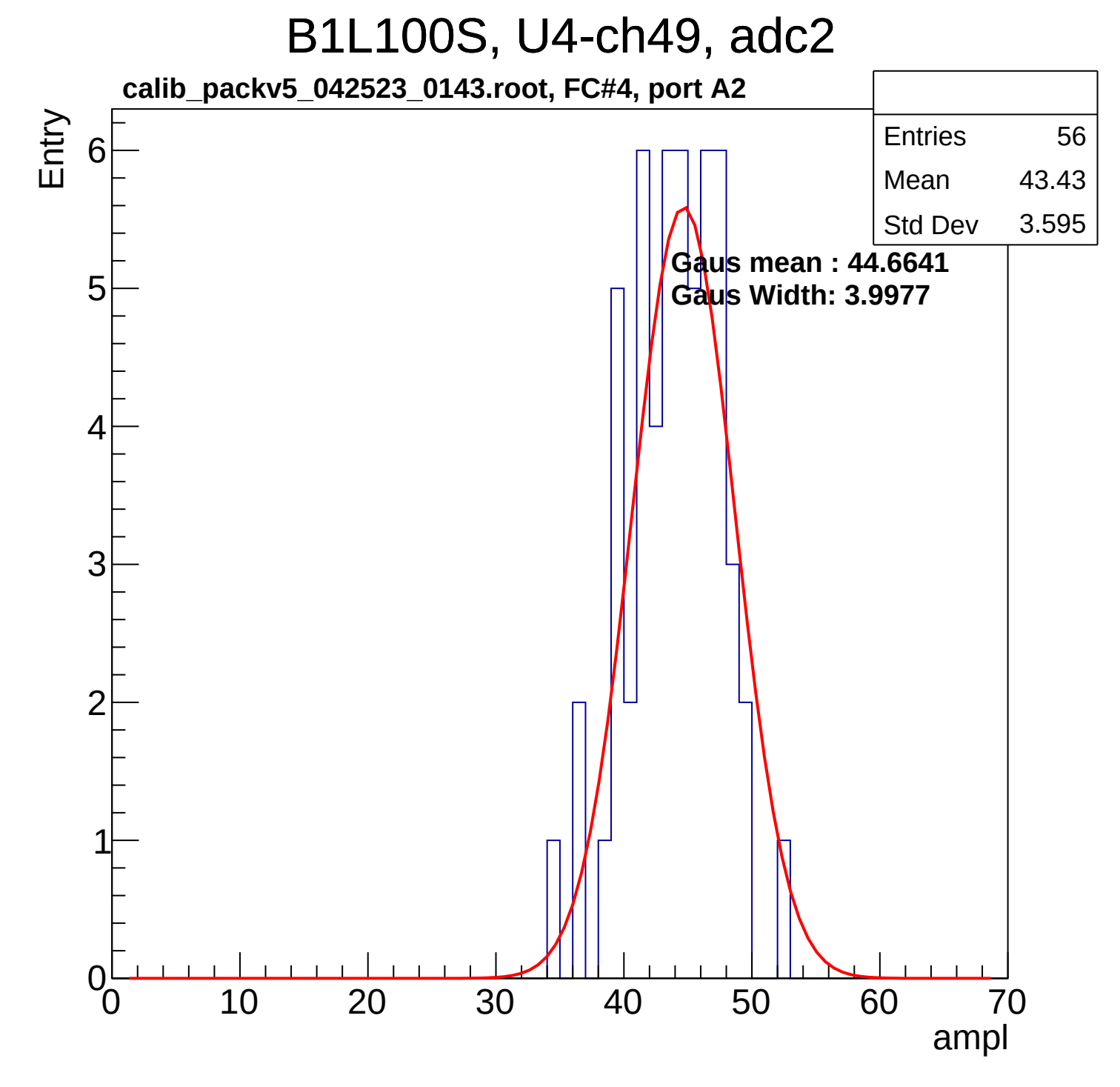

B1L100S, U4-ch48, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 58.89
Std Dev 2.807
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

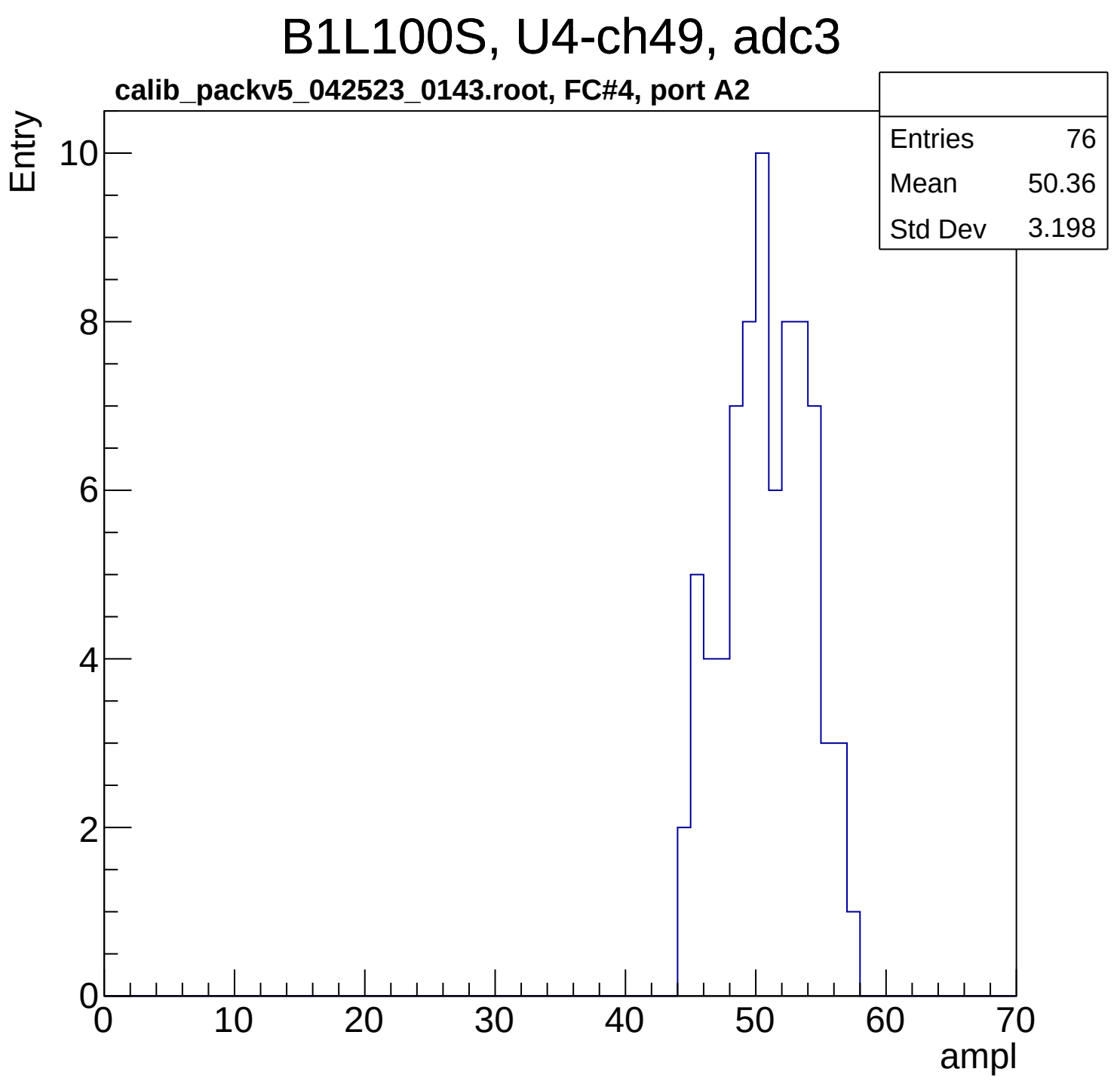

B1L100S, U4-ch48, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 55.6
Std Dev 18.58
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

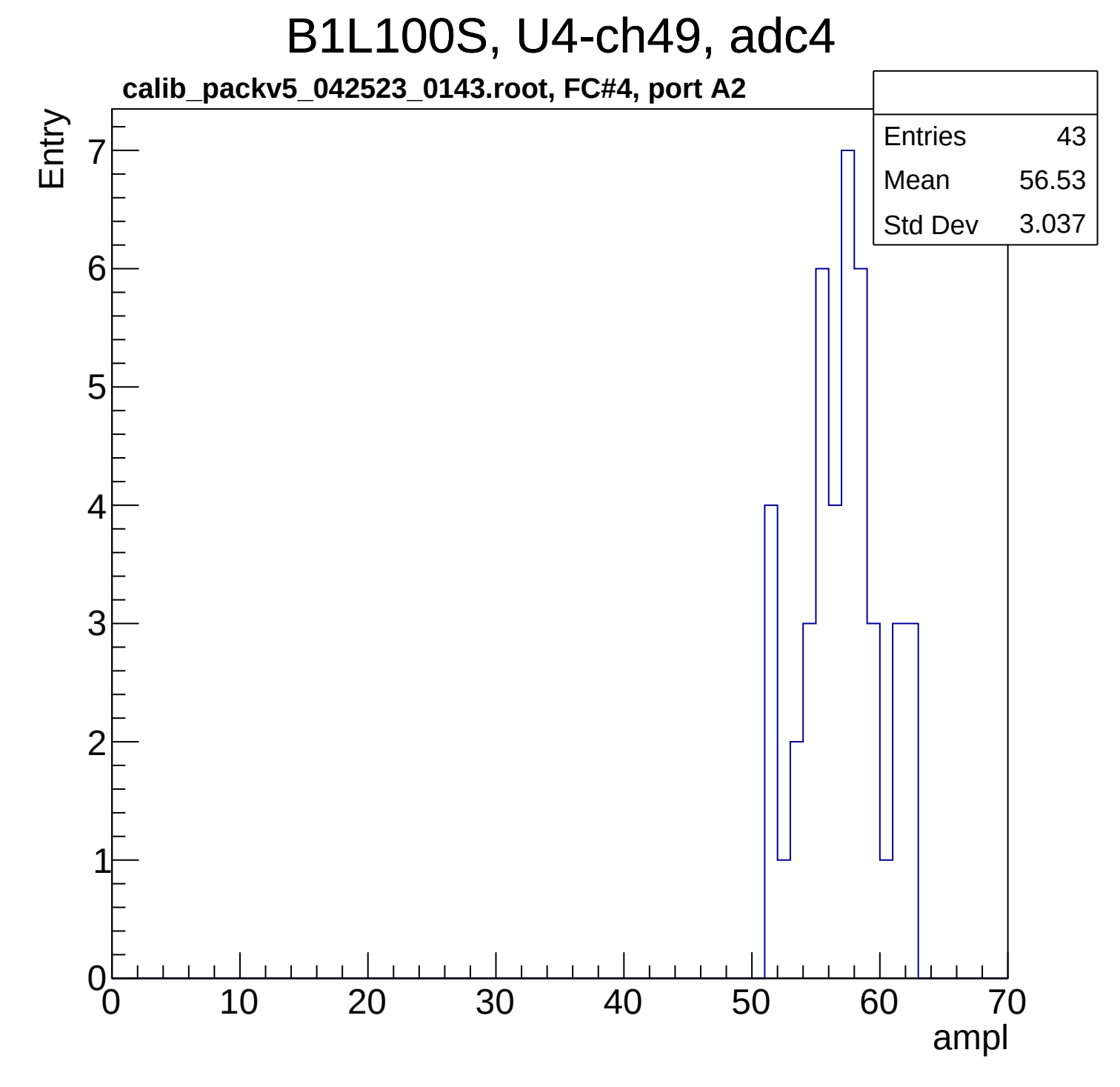

B1L100S, U4-ch48, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

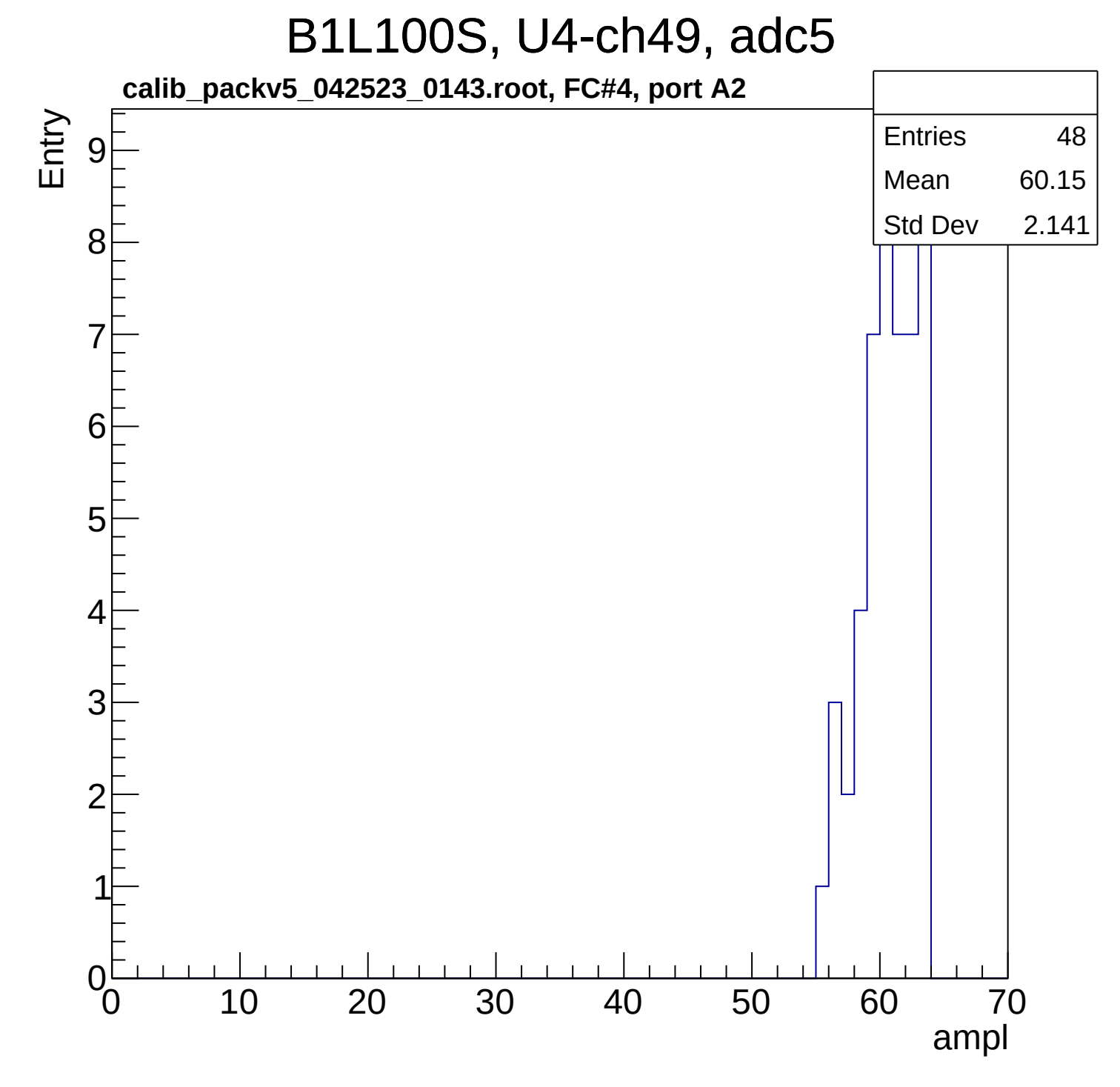

B1L100S, U4-ch49, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 95
Mean 29.31
Std Dev 5.655
Gaus mean : 30.2316
Gaus Width: 3.8227
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

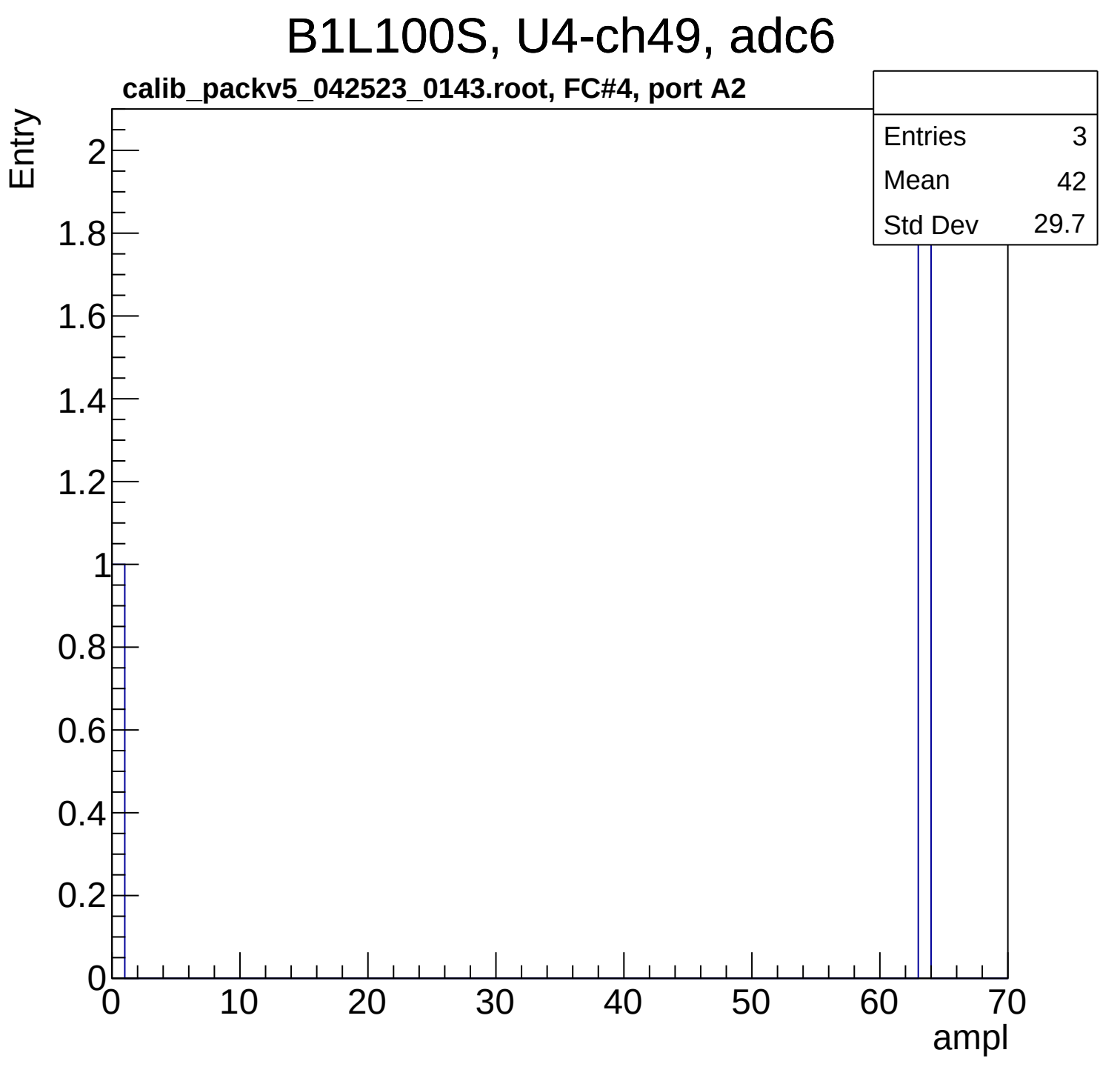

B1L100S, U4-ch49, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 38.19
Std Dev 3.221
Gaus mean : 39.0088
Gaus Width: 3.9087
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

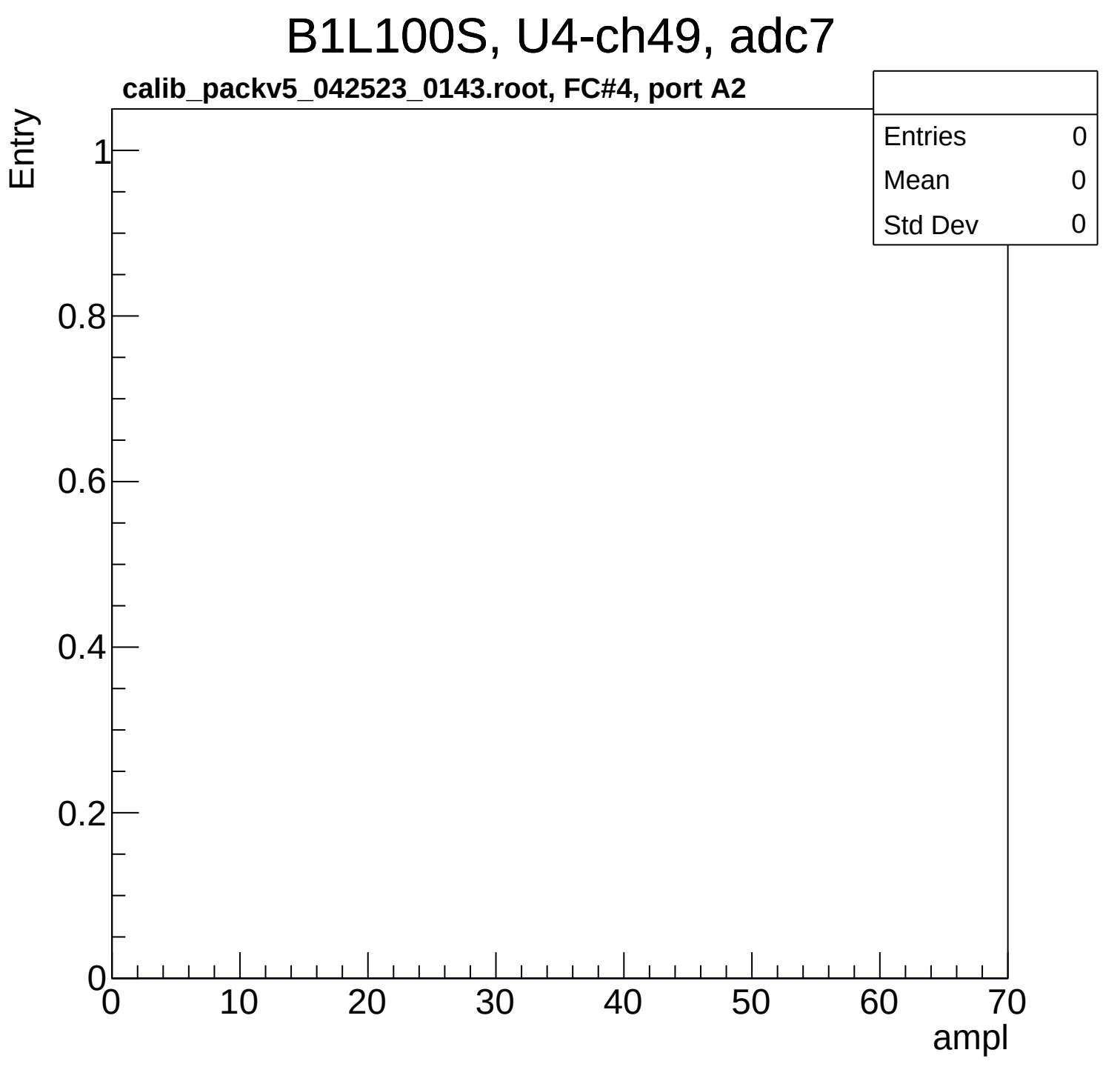

B1L100S, U4-ch49, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 43.43
Std Dev 3.595
Gaus mean : 44.6641
Gaus Width: 3.9977
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

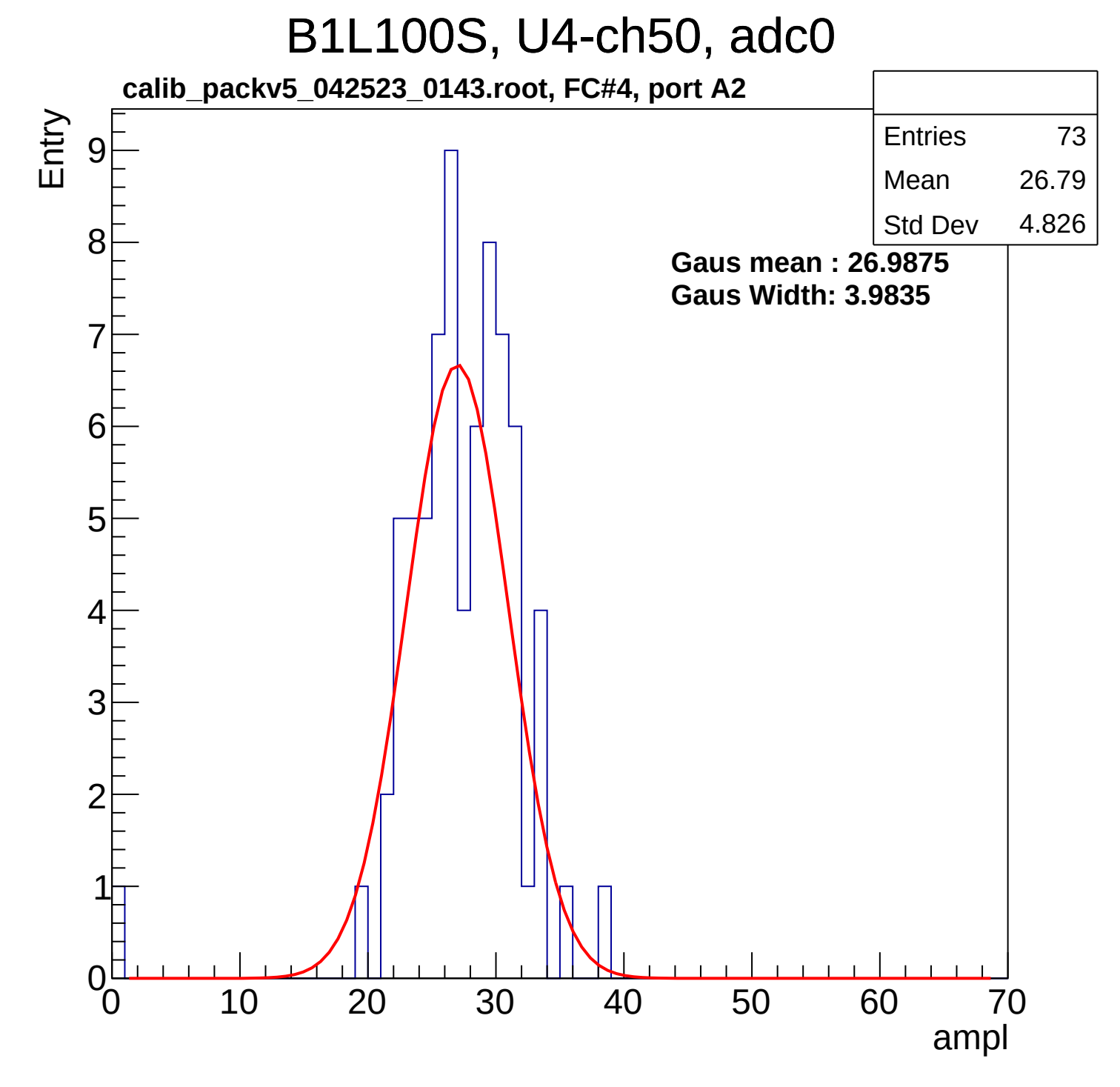

B1L100S, U4-ch49, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 50.36
Std Dev 3.198
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

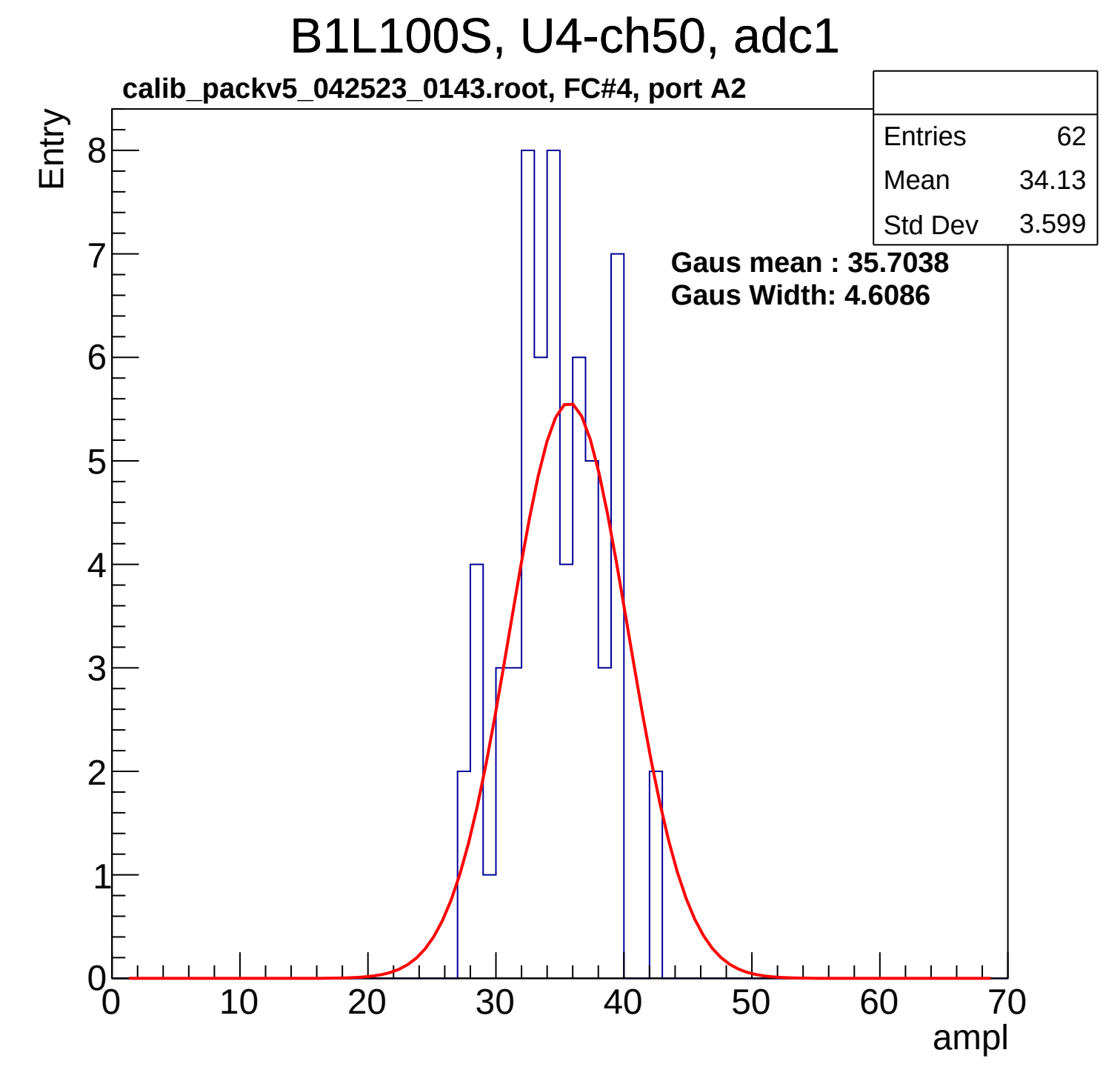

B1L100S, U4-ch49, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 56.53
Std Dev 3.037
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

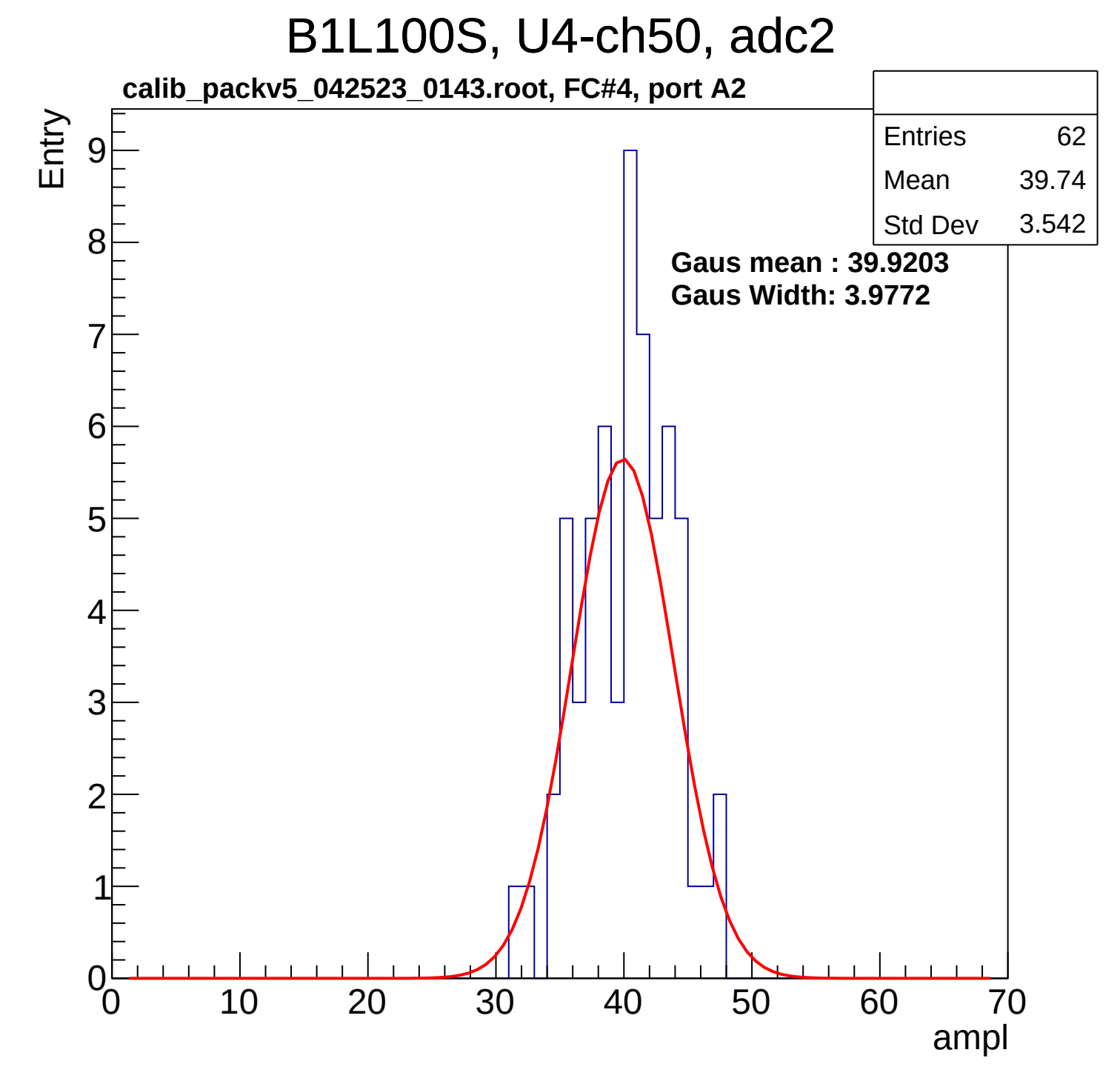

B1L100S, U4-ch49, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 60.15
Std Dev 2.141
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

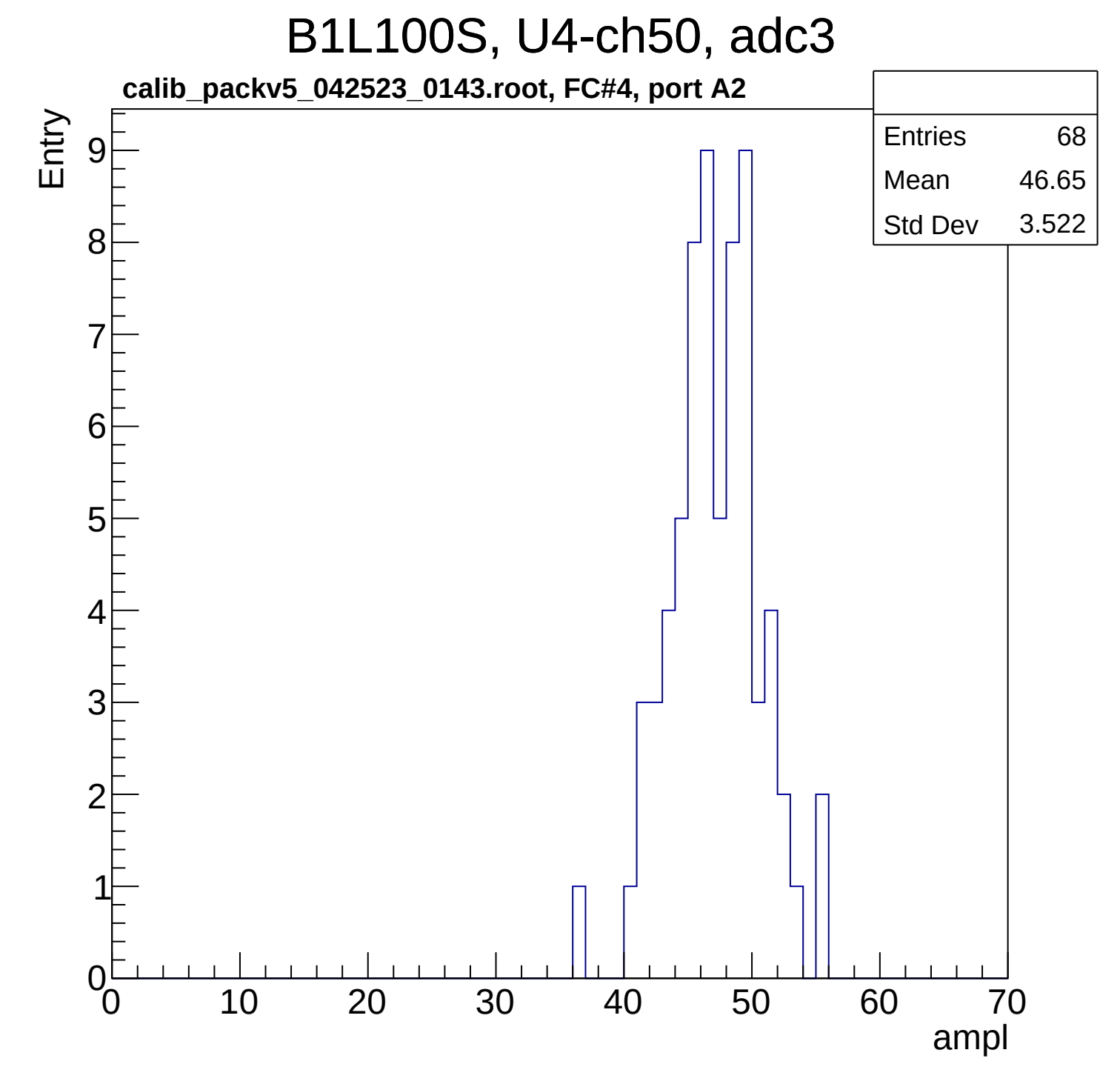

B1L100S, U4-ch49, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 42
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

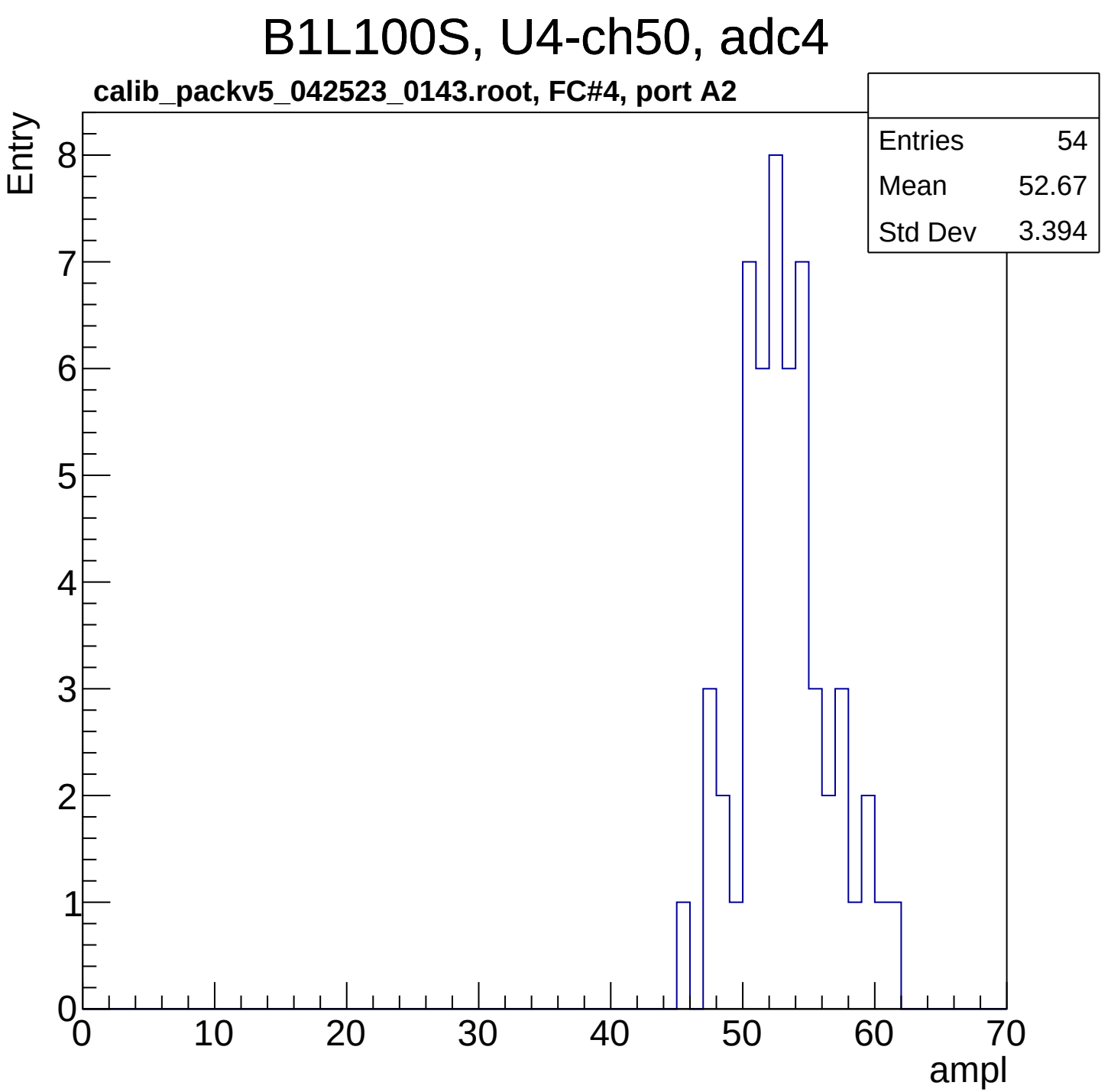

B1L100S, U4-ch49, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

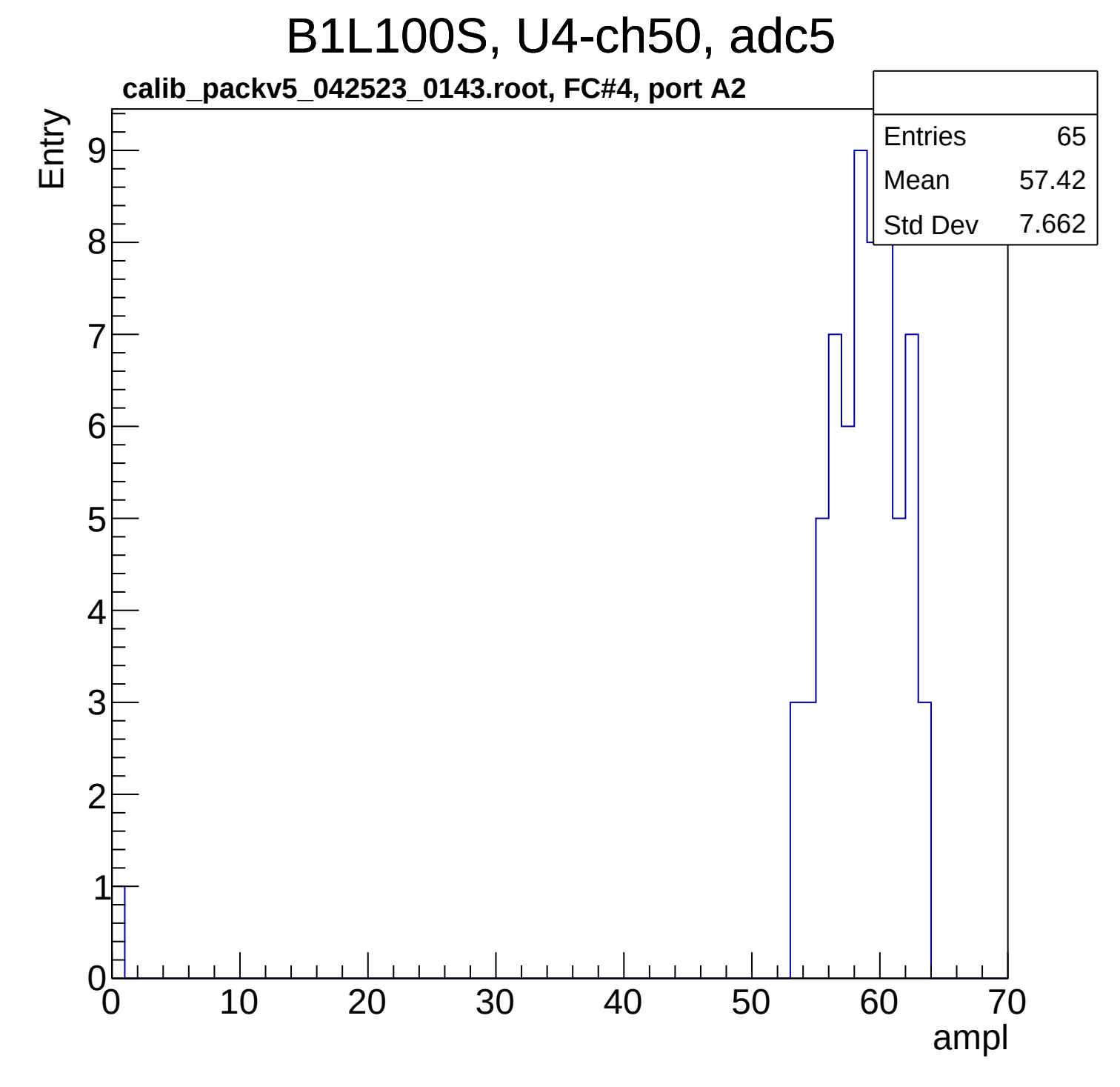

B1L100S, U4-ch50, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 26.79
Std Dev 4.826
Gaus mean : 26.9875
Gaus Width: 3.9835
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

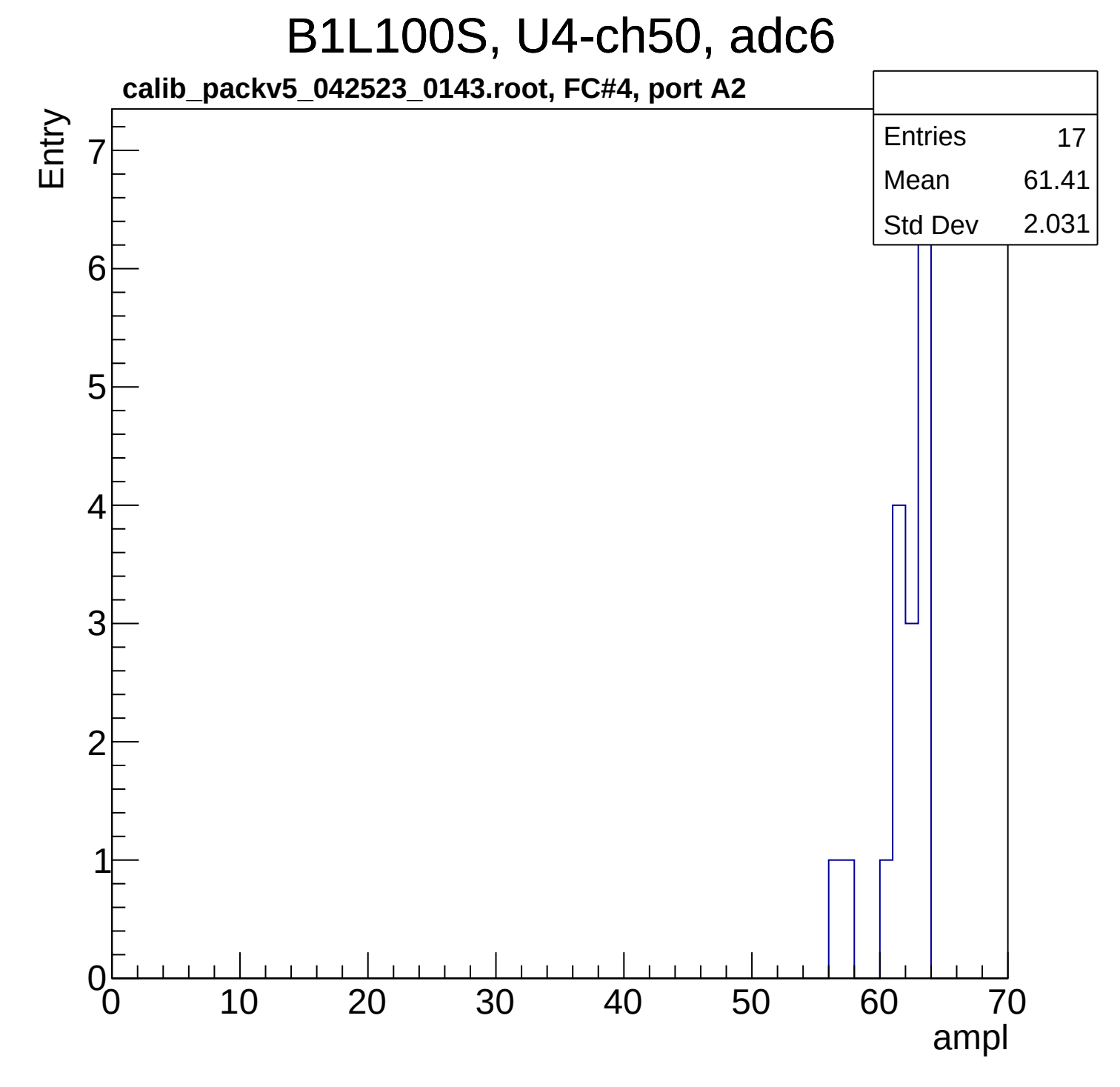

B1L100S, U4-ch50, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 34.13
Std Dev 3.599
Gaus mean : 35.7038
Gaus Width: 4.6086
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

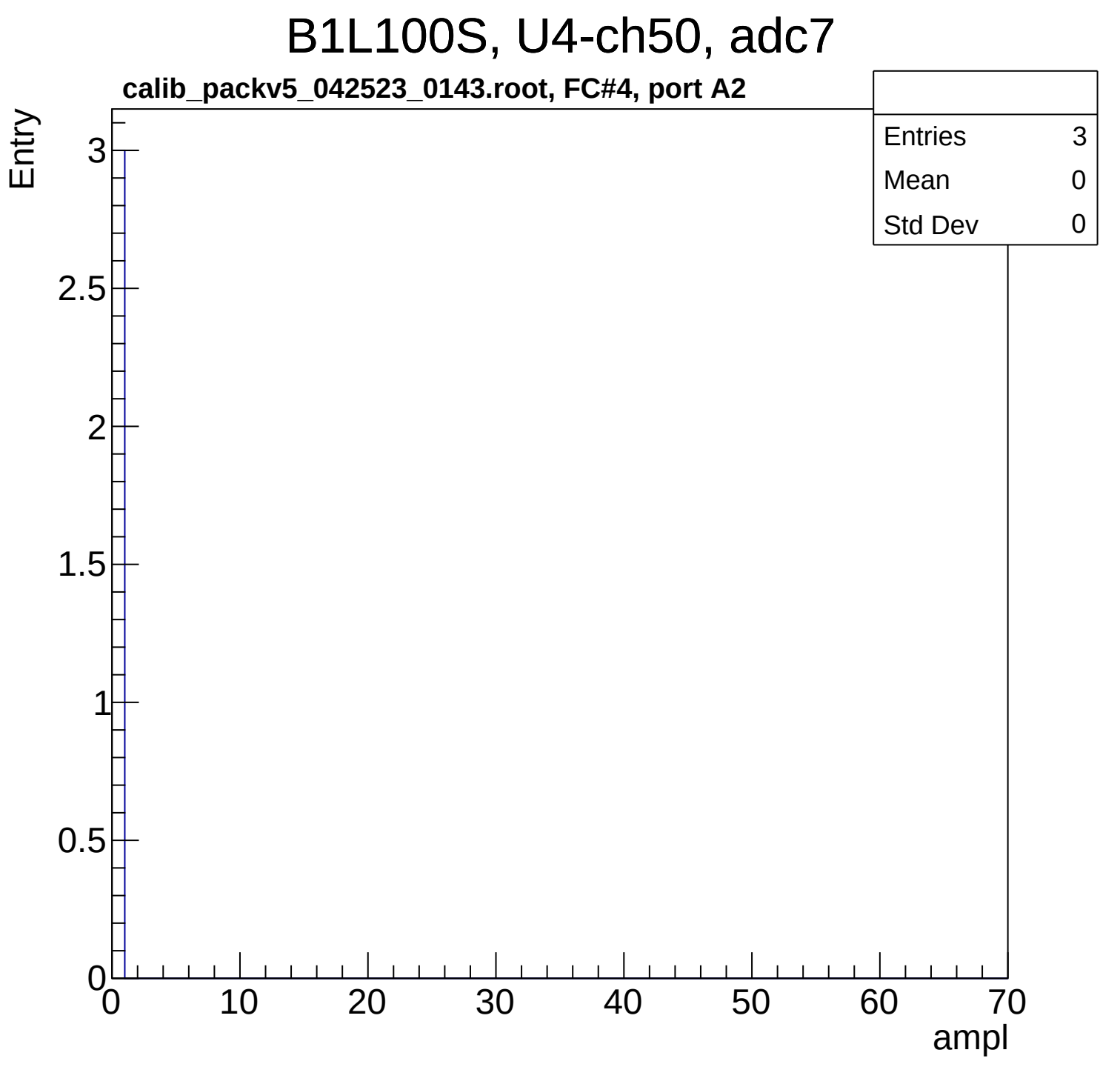

B1L100S, U4-ch50, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 39.74
Std Dev 3.542
Gaus mean : 39.9203
Gaus Width: 3.9772
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

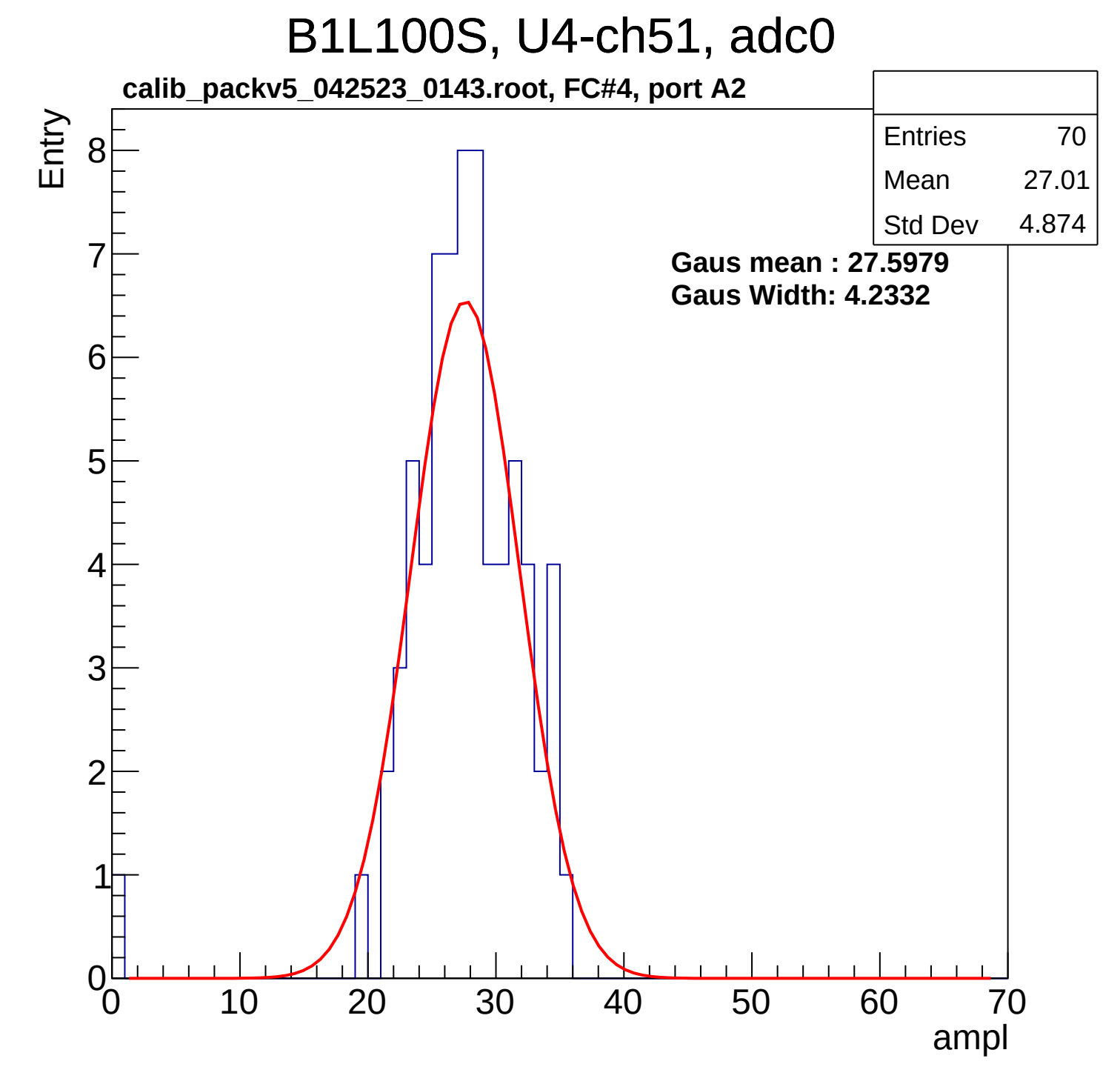

B1L100S, U4-ch50, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 46.65
Std Dev 3.522
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

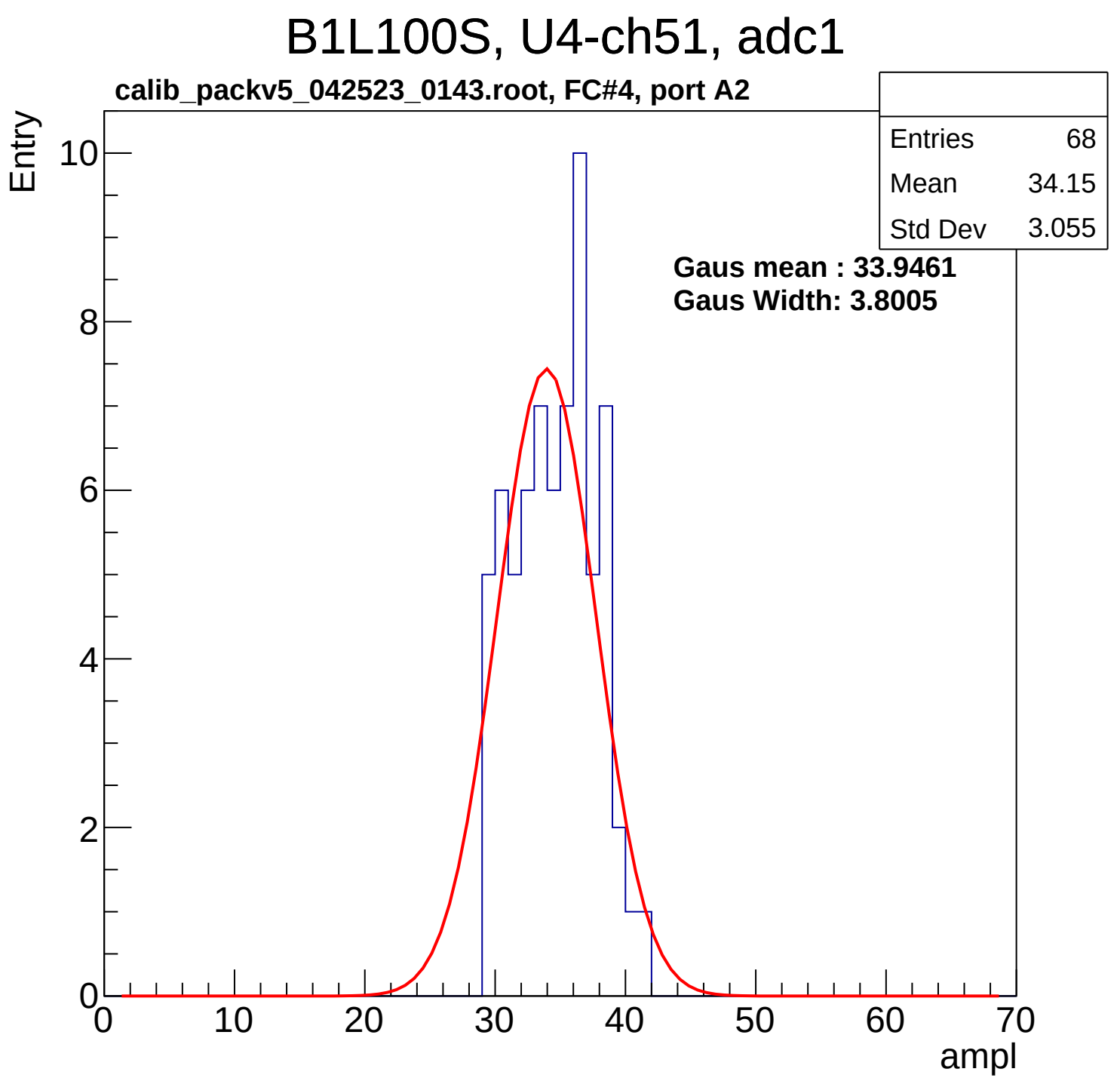

B1L100S, U4-ch50, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 52.67
Std Dev 3.394
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

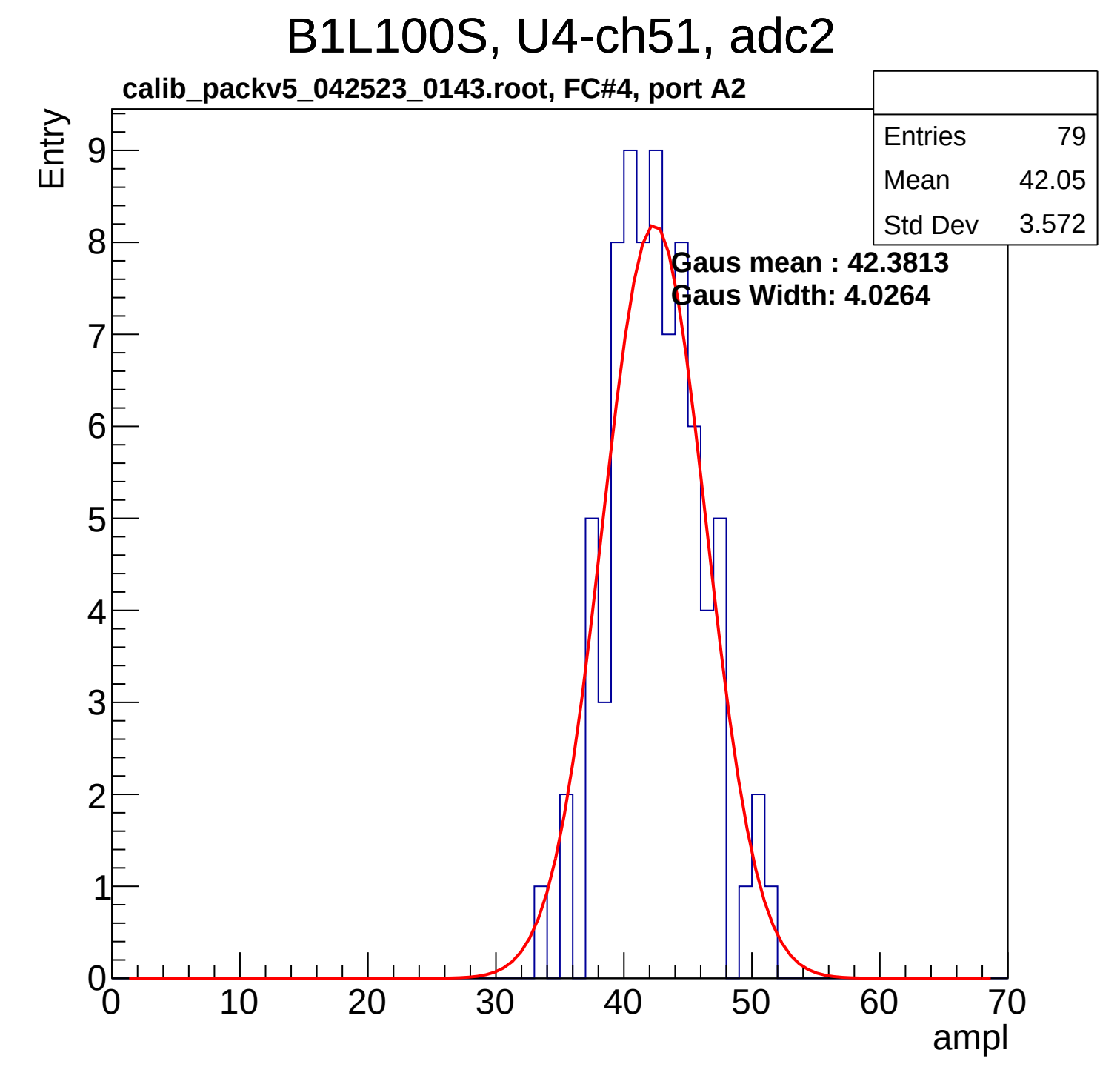

B1L100S, U4-ch50, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 57.42
Std Dev 7.662
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

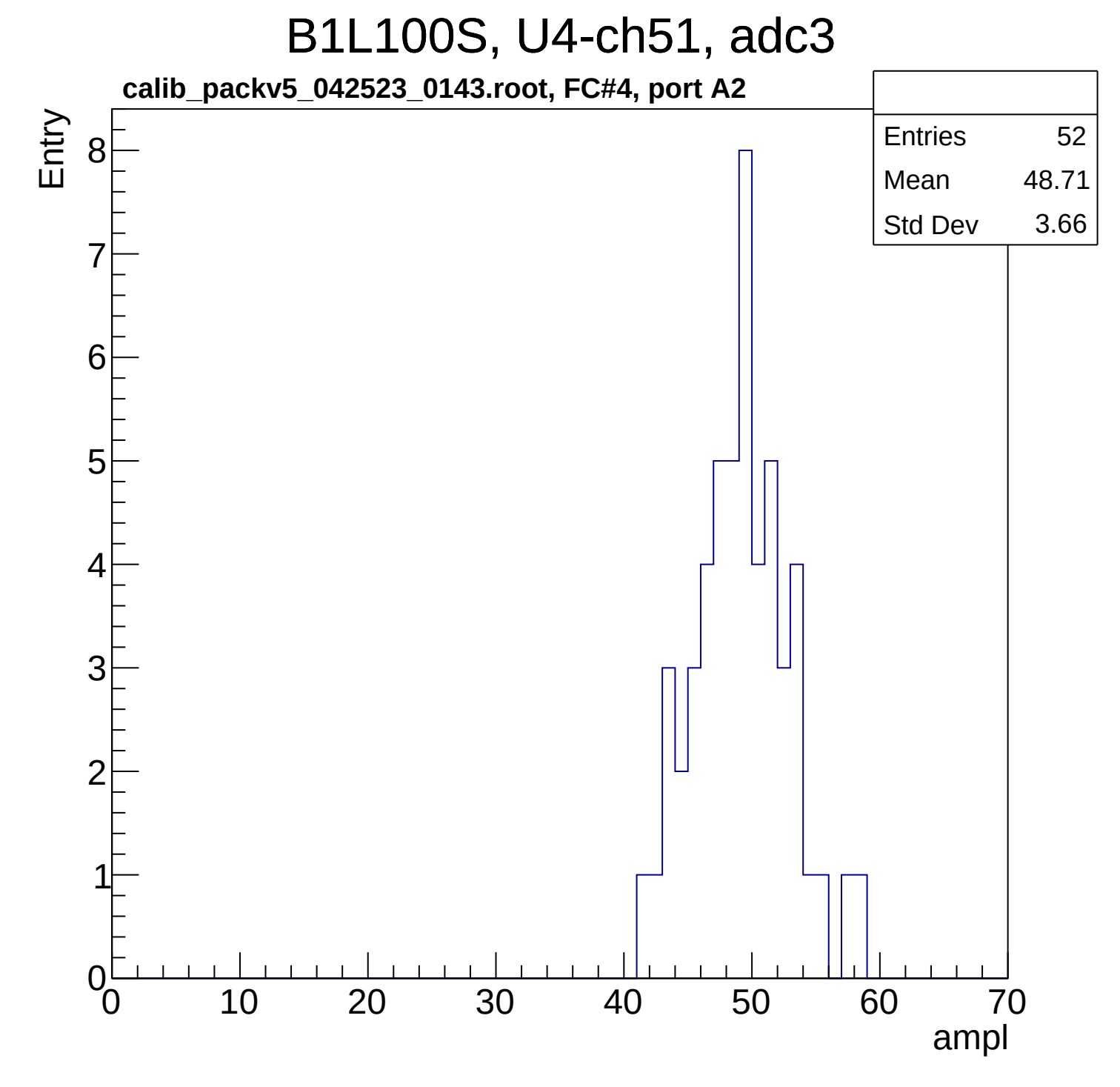

B1L100S, U4-ch50, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 17
Mean 61.41
Std Dev 2.031
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

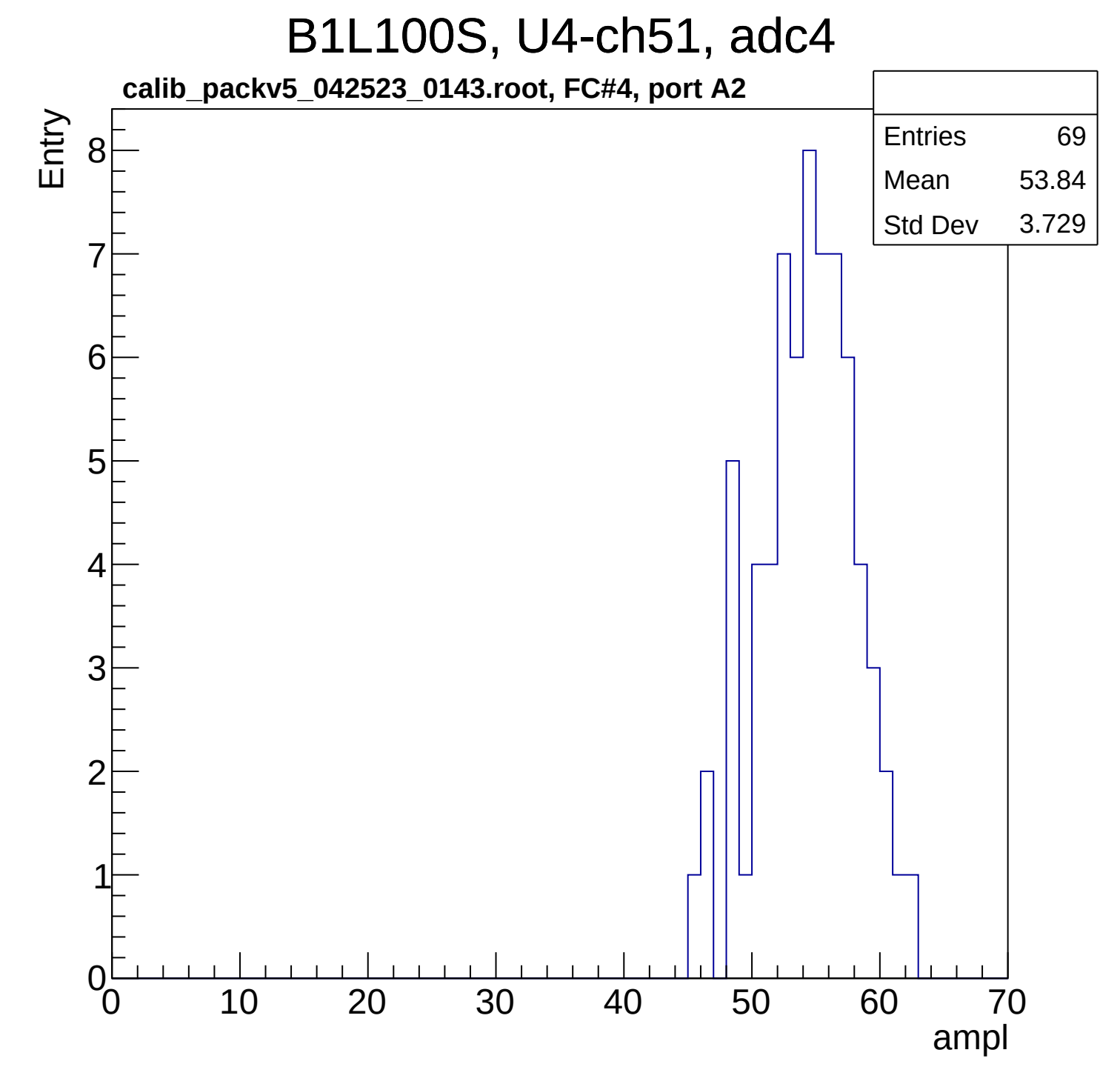

B1L100S, U4-ch50, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 0
Std Dev 0
Entry
3
2.5
2
1.5
1
0.5
0
0
10
20
30
40
50
60
70
ampl

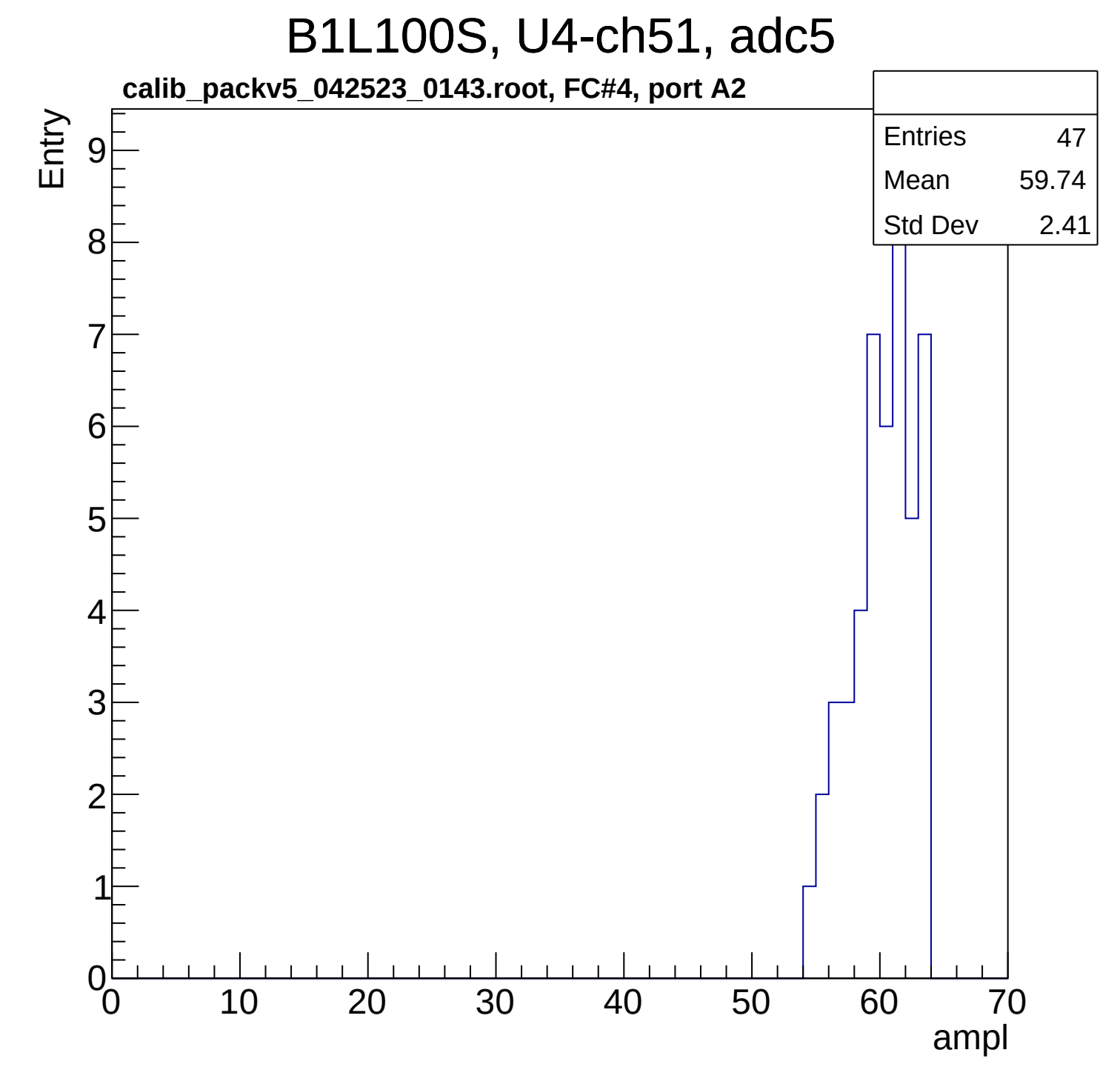

B1L100S, U4-ch51, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 27.01
Std Dev 4.874
Gaus mean : 27.5979
Gaus Width: 4.2332
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

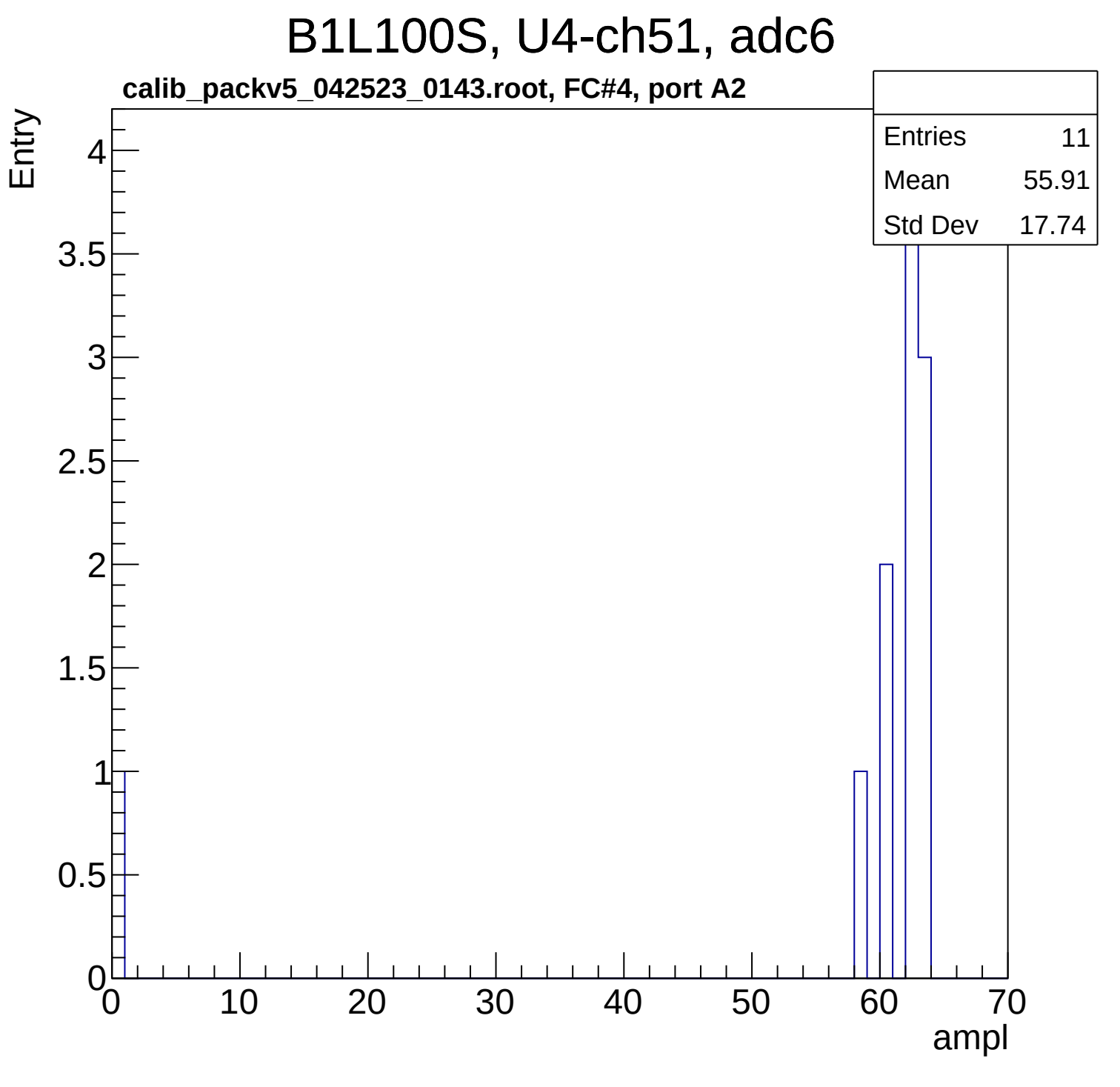

B1L100S, U4-ch51, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 34.15
Std Dev 3.055
Gaus mean : 33.9461
Gaus Width: 3.8005
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

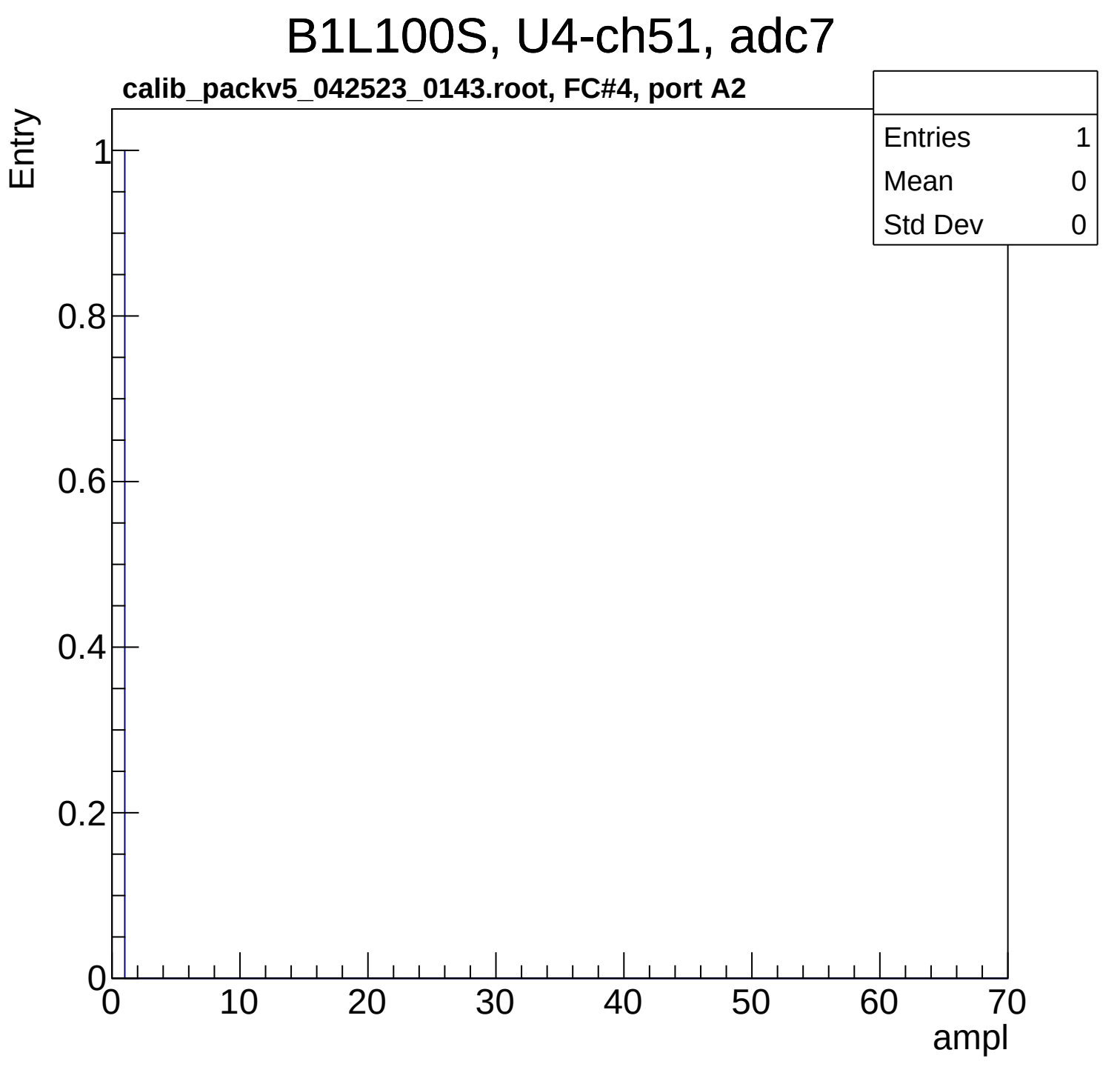

B1L100S, U4-ch51, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 42.05
Std Dev 3.572
Gaus mean : 42.3813
Gaus Width: 4.0264
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

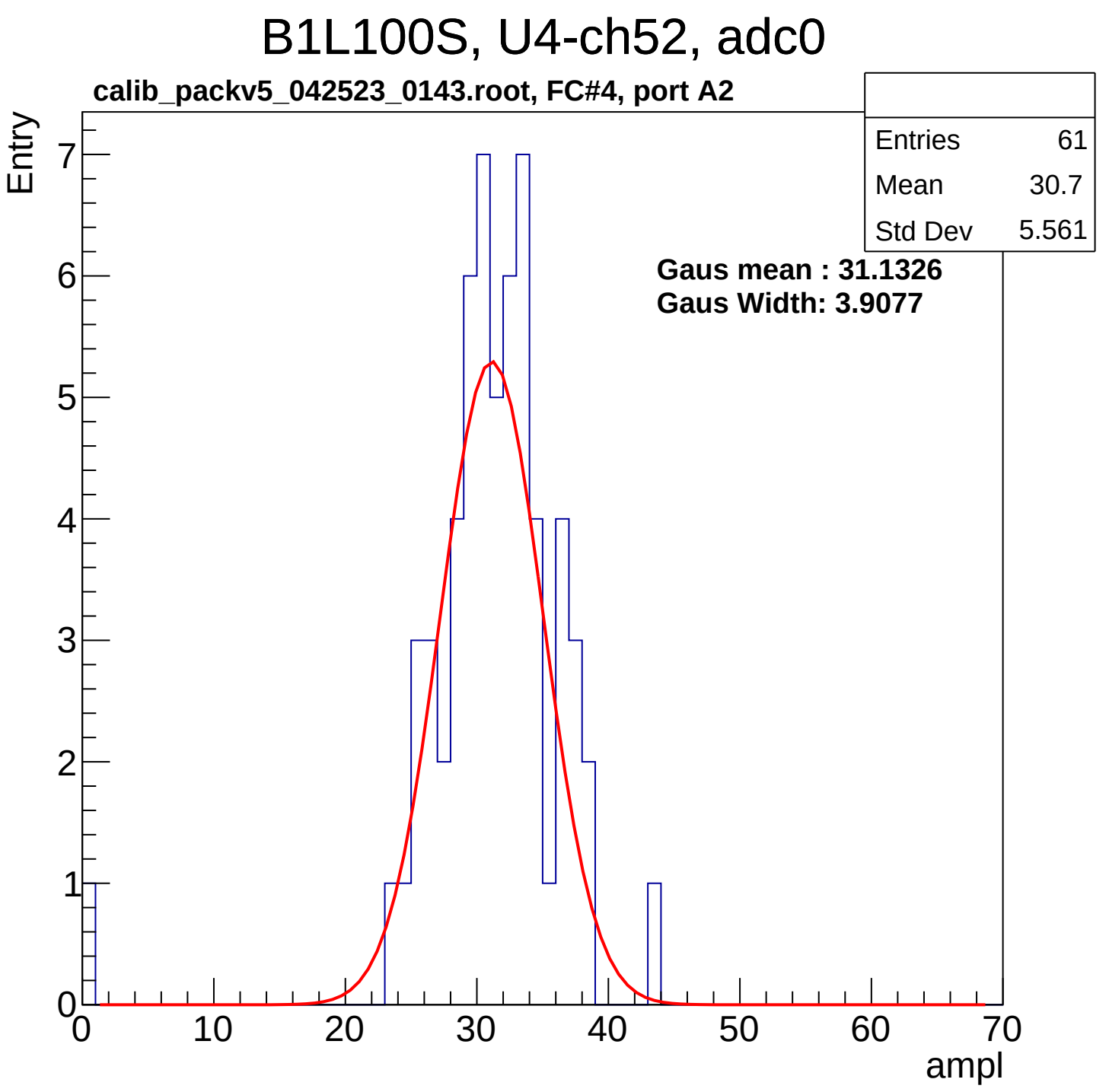

B1L100S, U4-ch51, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 48.71
Std Dev 3.66
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

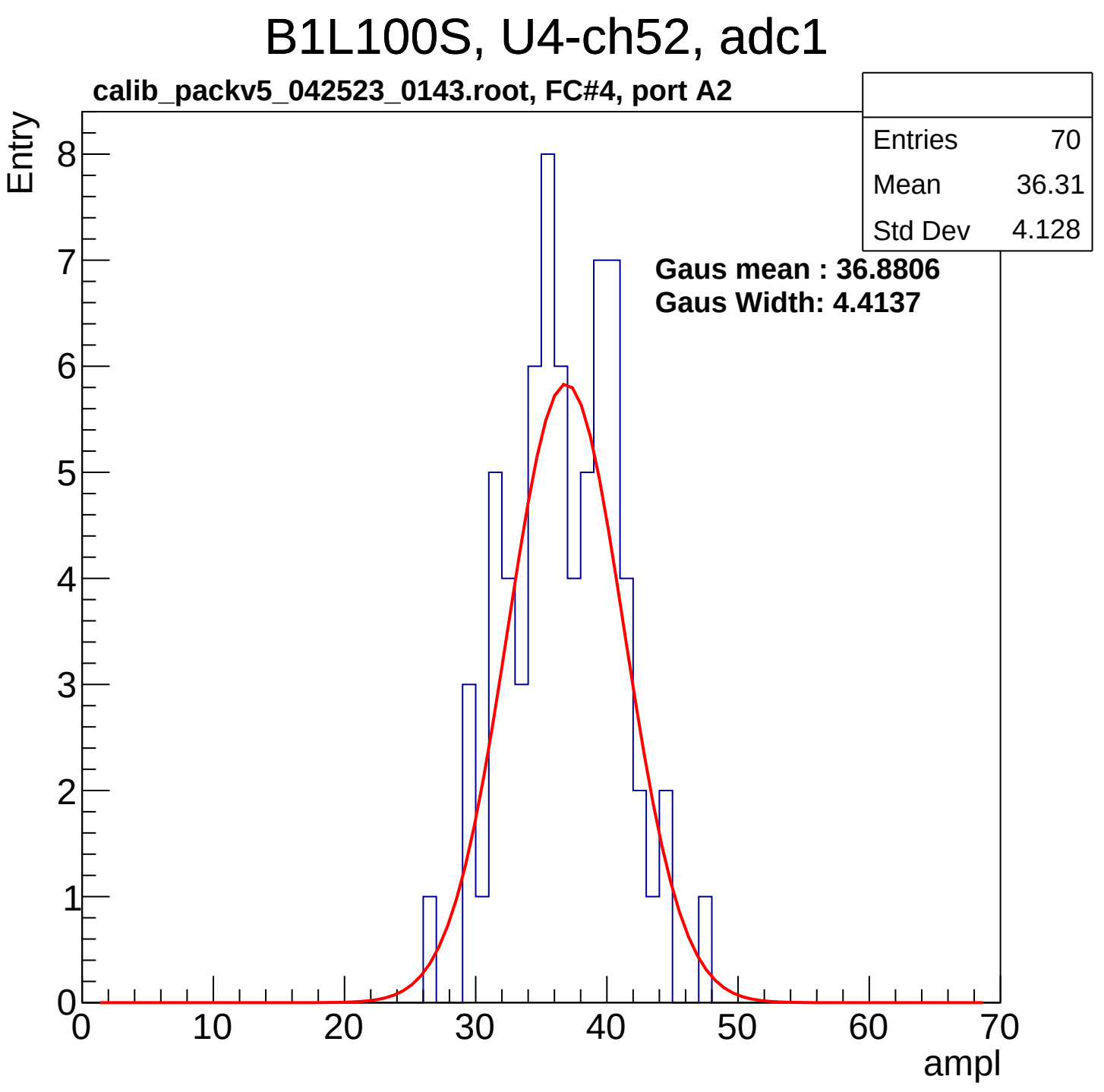

B1L100S, U4-ch51, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 53.84
Std Dev 3.729
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

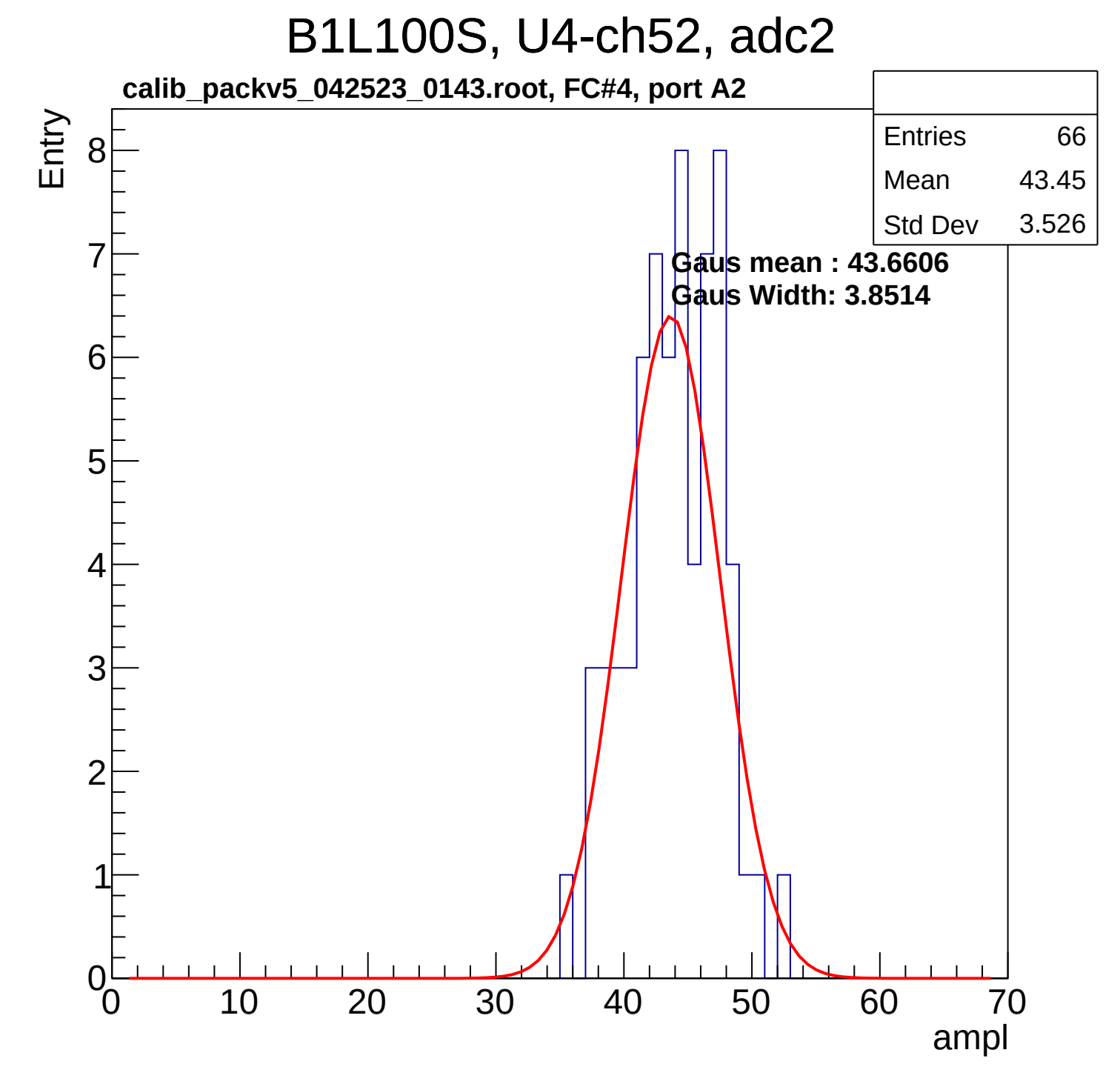

B1L100S, U4-ch51, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 59.74
Std Dev 2.41
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

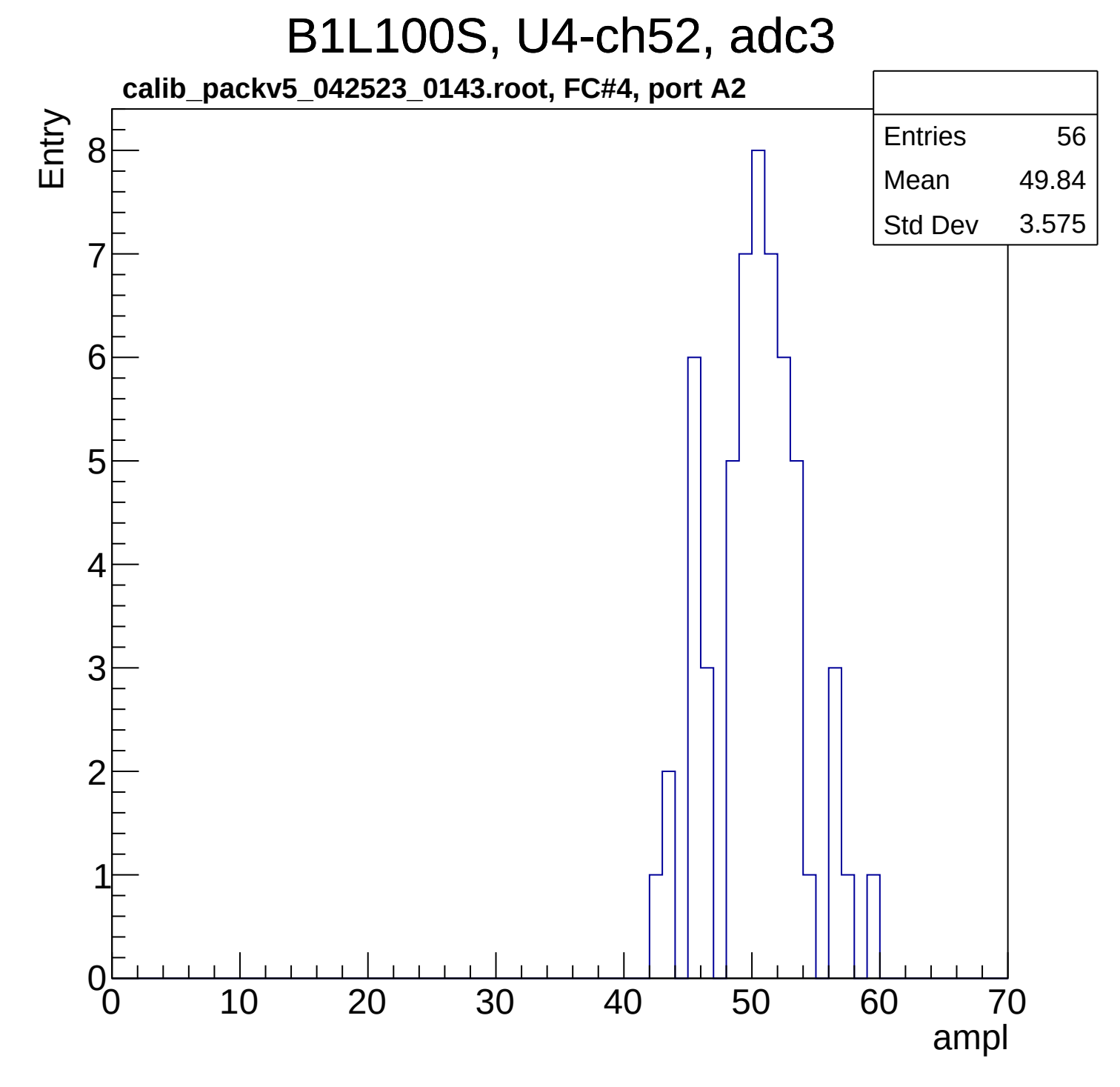

B1L100S, U4-ch51, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 55.91
Std Dev 17.74
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

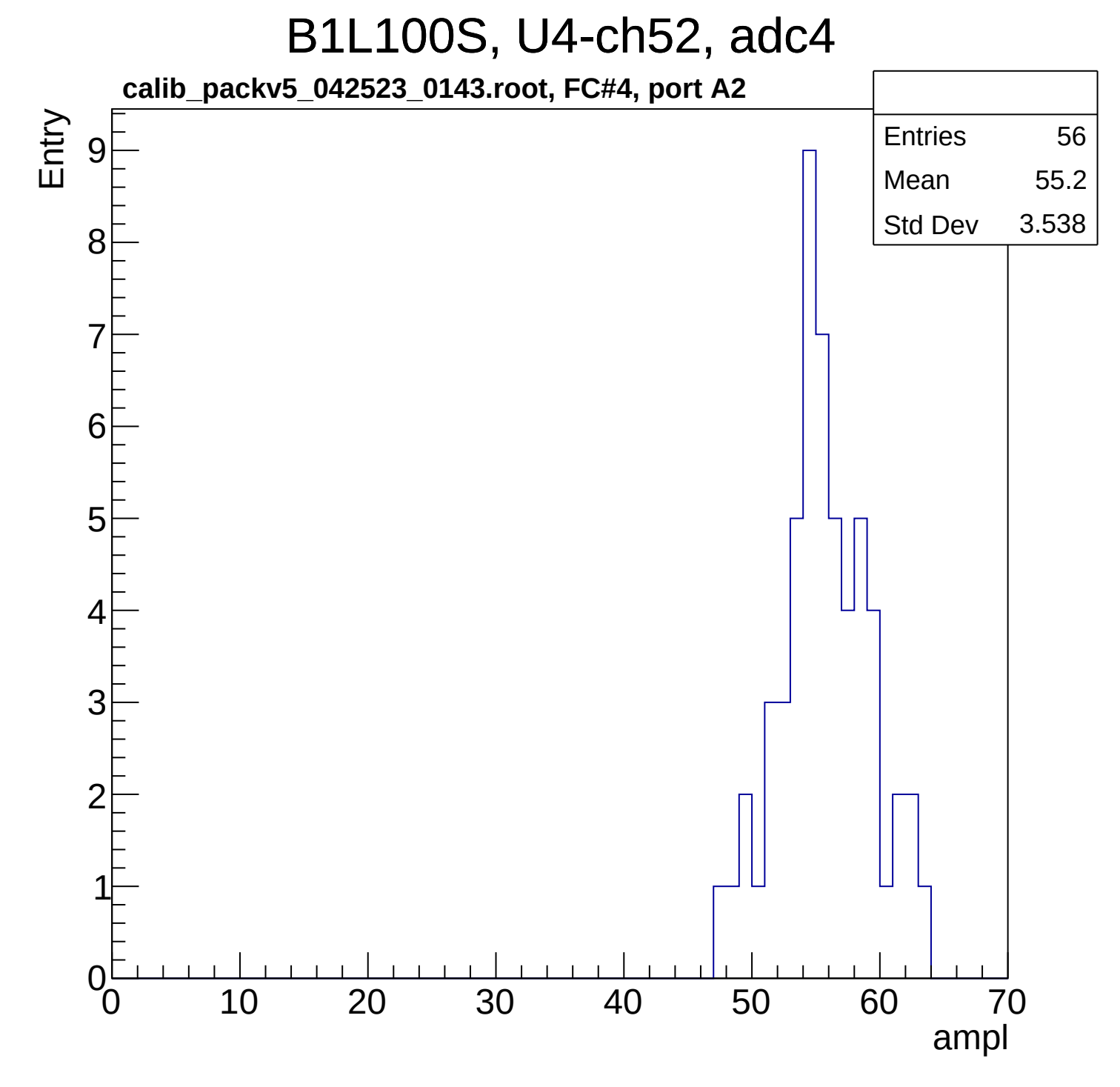

B1L100S, U4-ch51, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

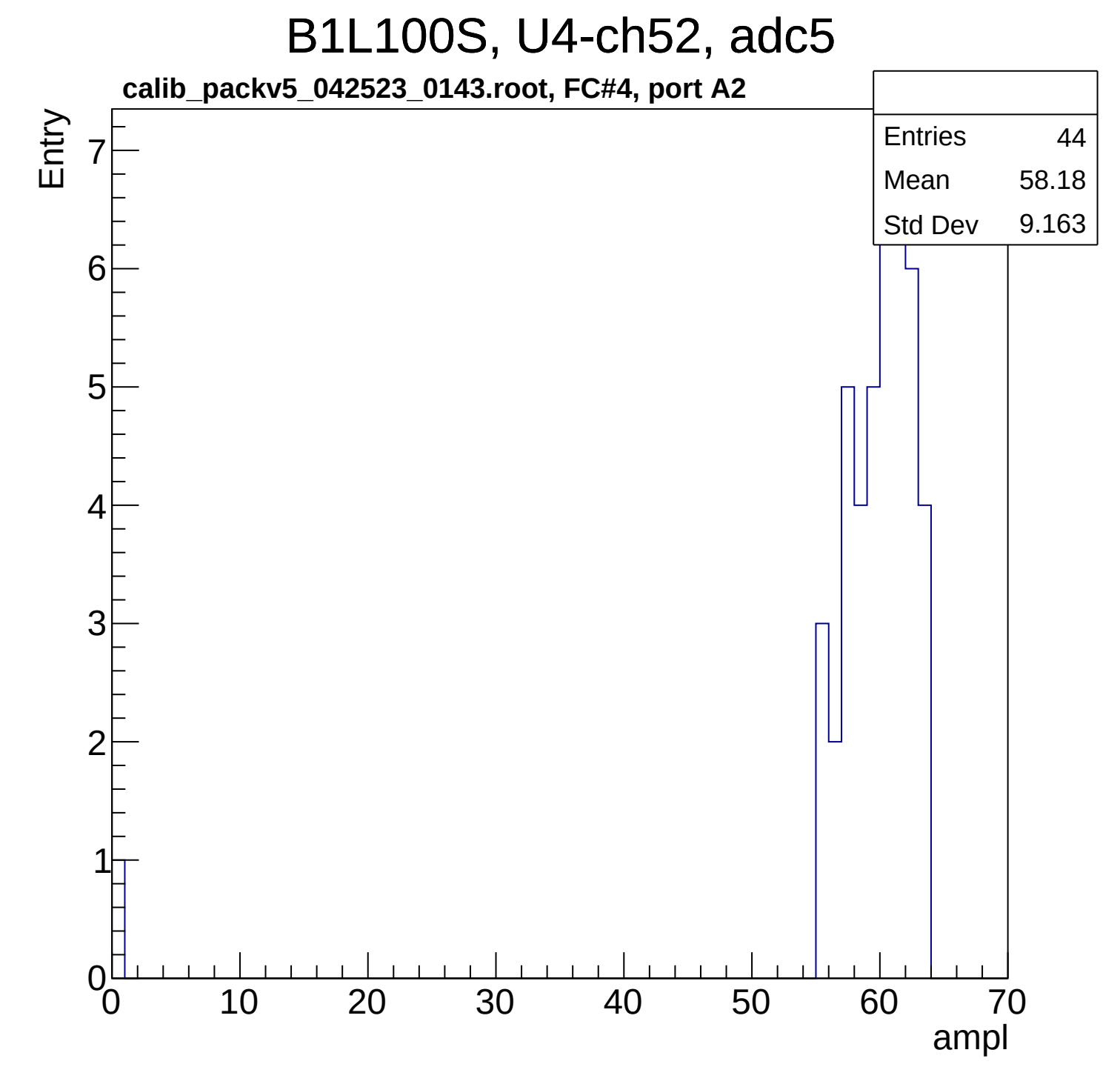

B1L100S, U4-ch52, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 30.7
Std Dev 5.561
Gaus mean : 31.1326
Gaus Width: 3.9077
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

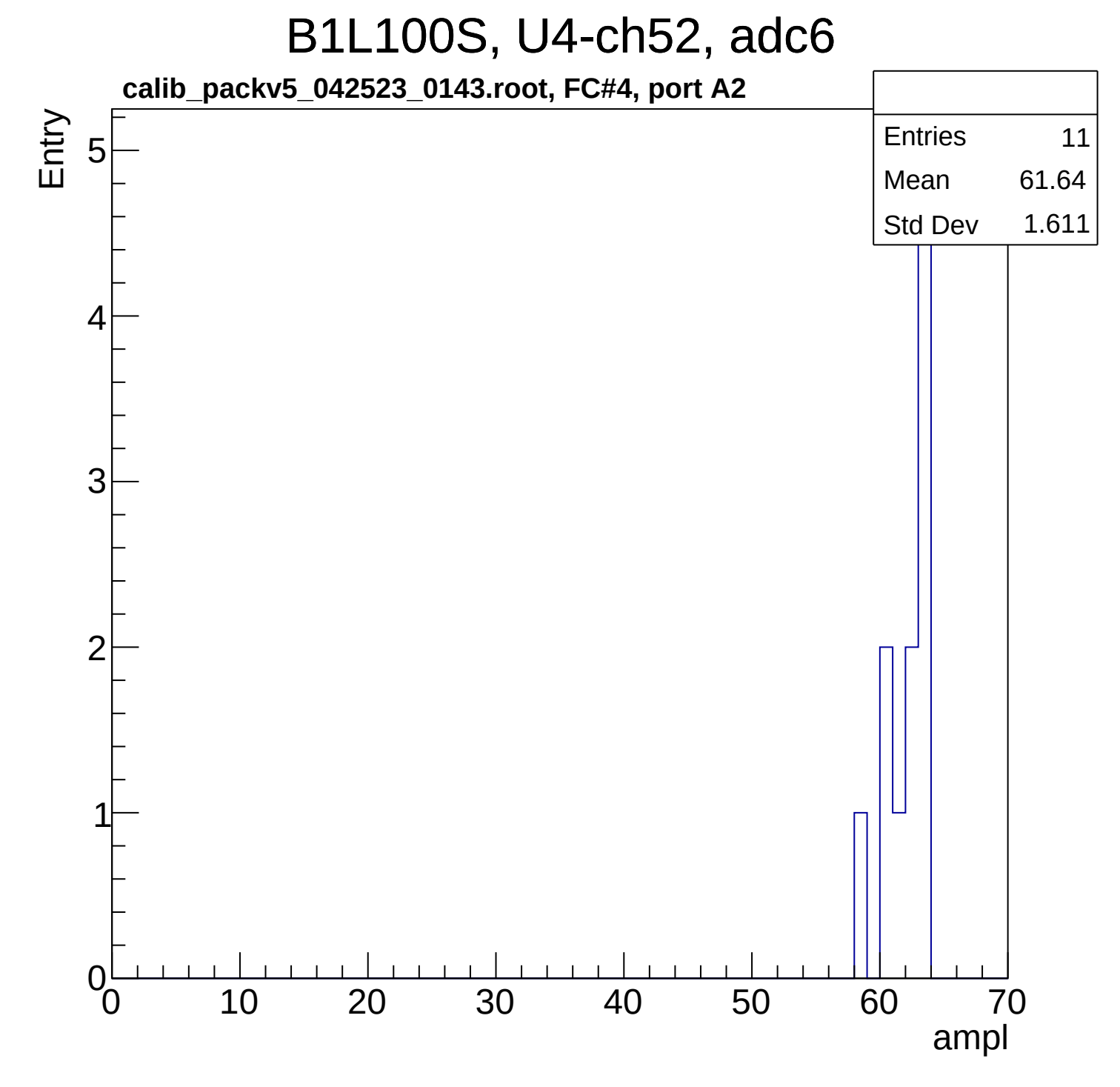

B1L100S, U4-ch52, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 36.31
Std Dev 4.128
Gaus mean : 36.8806
Gaus Width: 4.4137
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

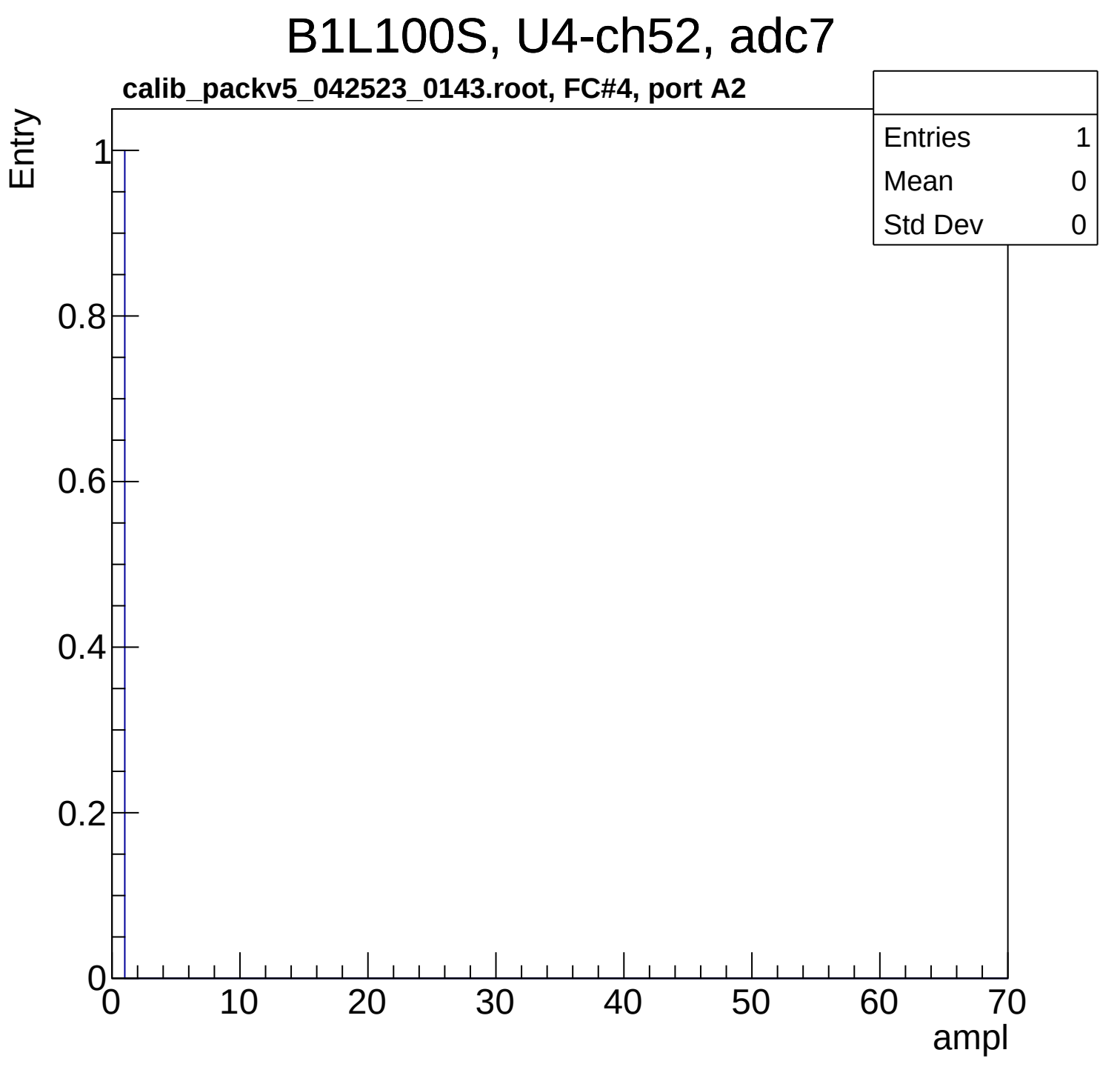

B1L100S, U4-ch52, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 43.45
Std Dev 3.526
Gaus mean : 43.6606
Gaus Width: 3.8514
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

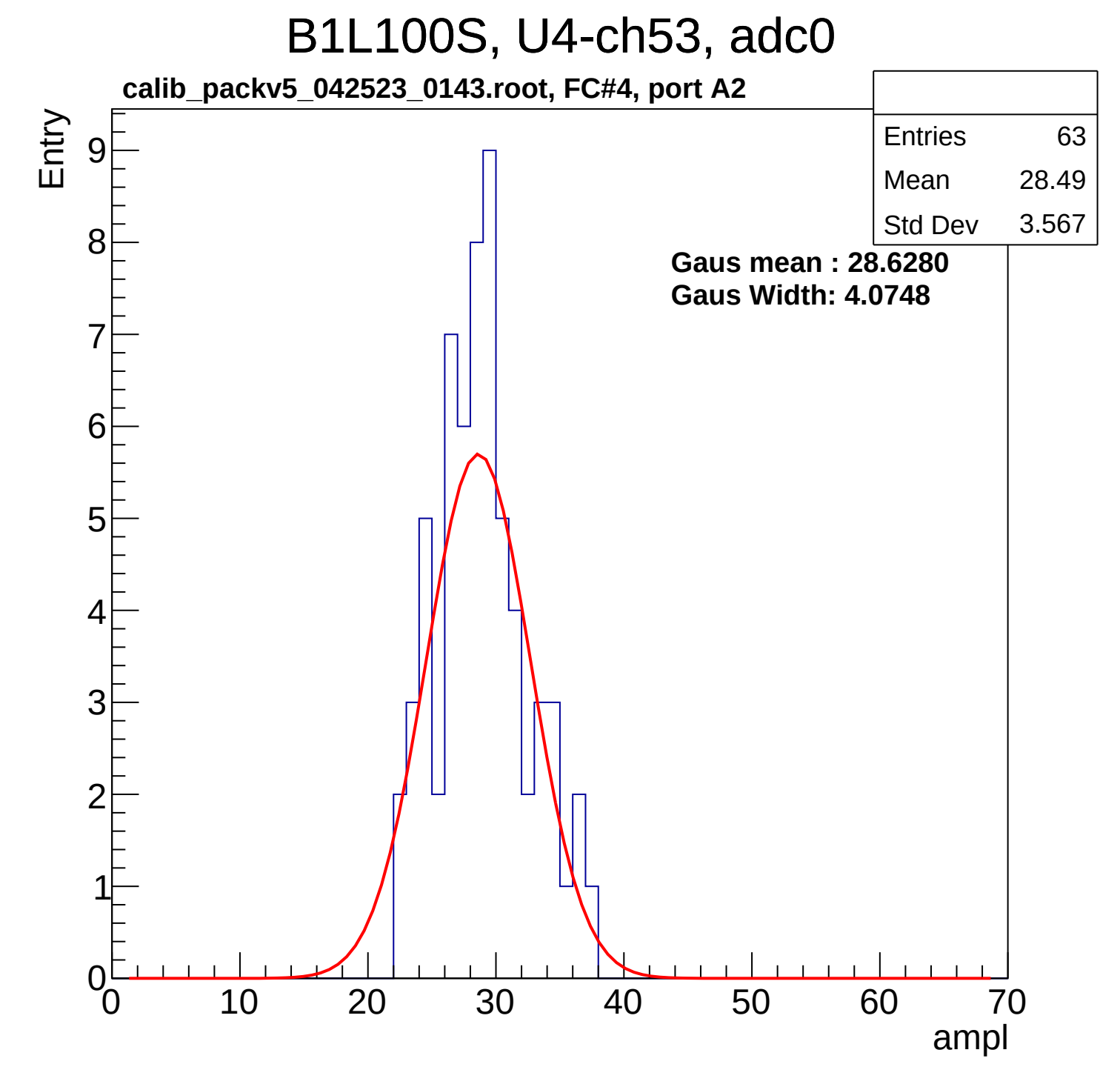

B1L100S, U4-ch52, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 49.84
Std Dev 3.575
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

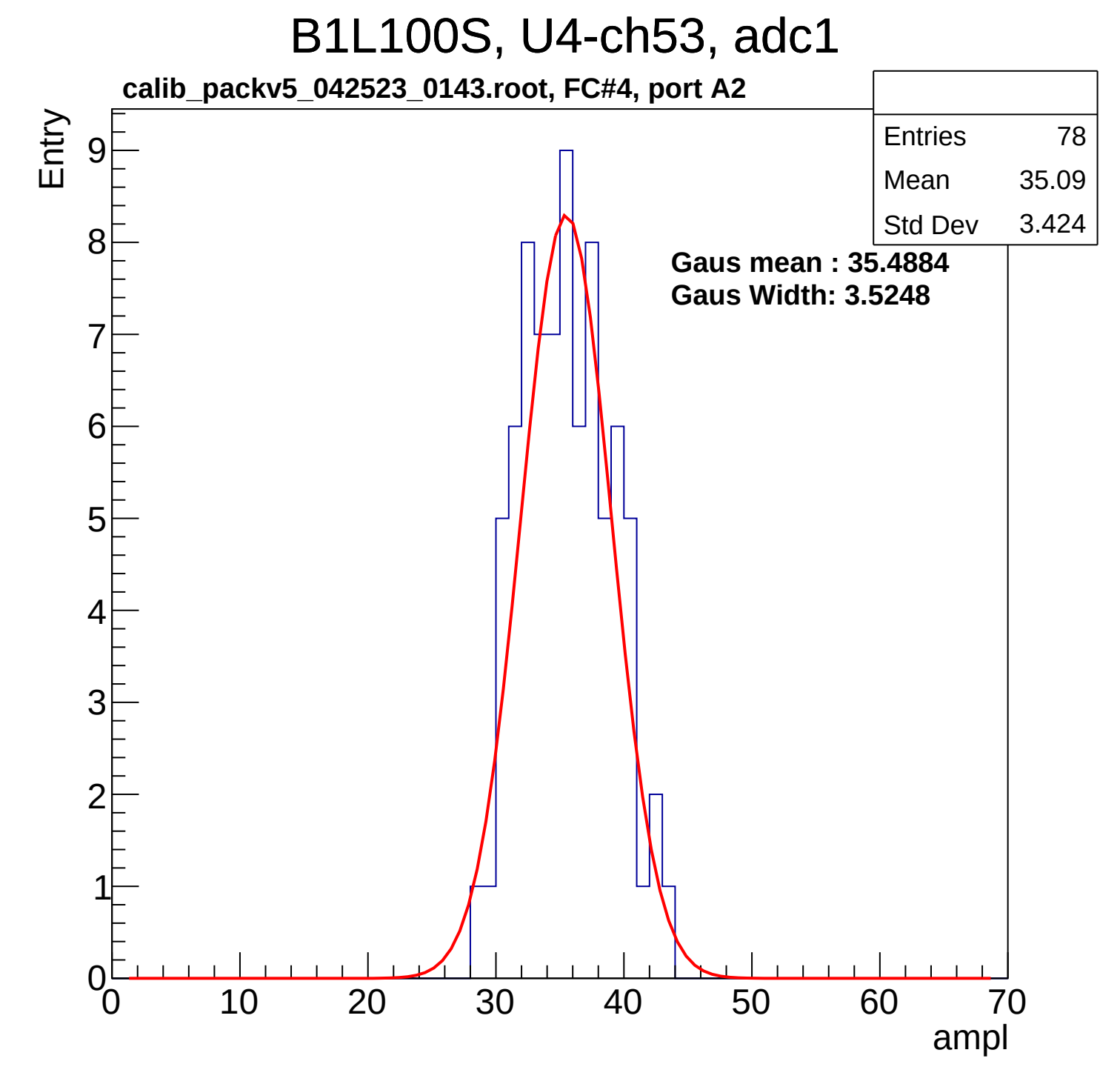

B1L100S, U4-ch52, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 55.2
Std Dev 3.538
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

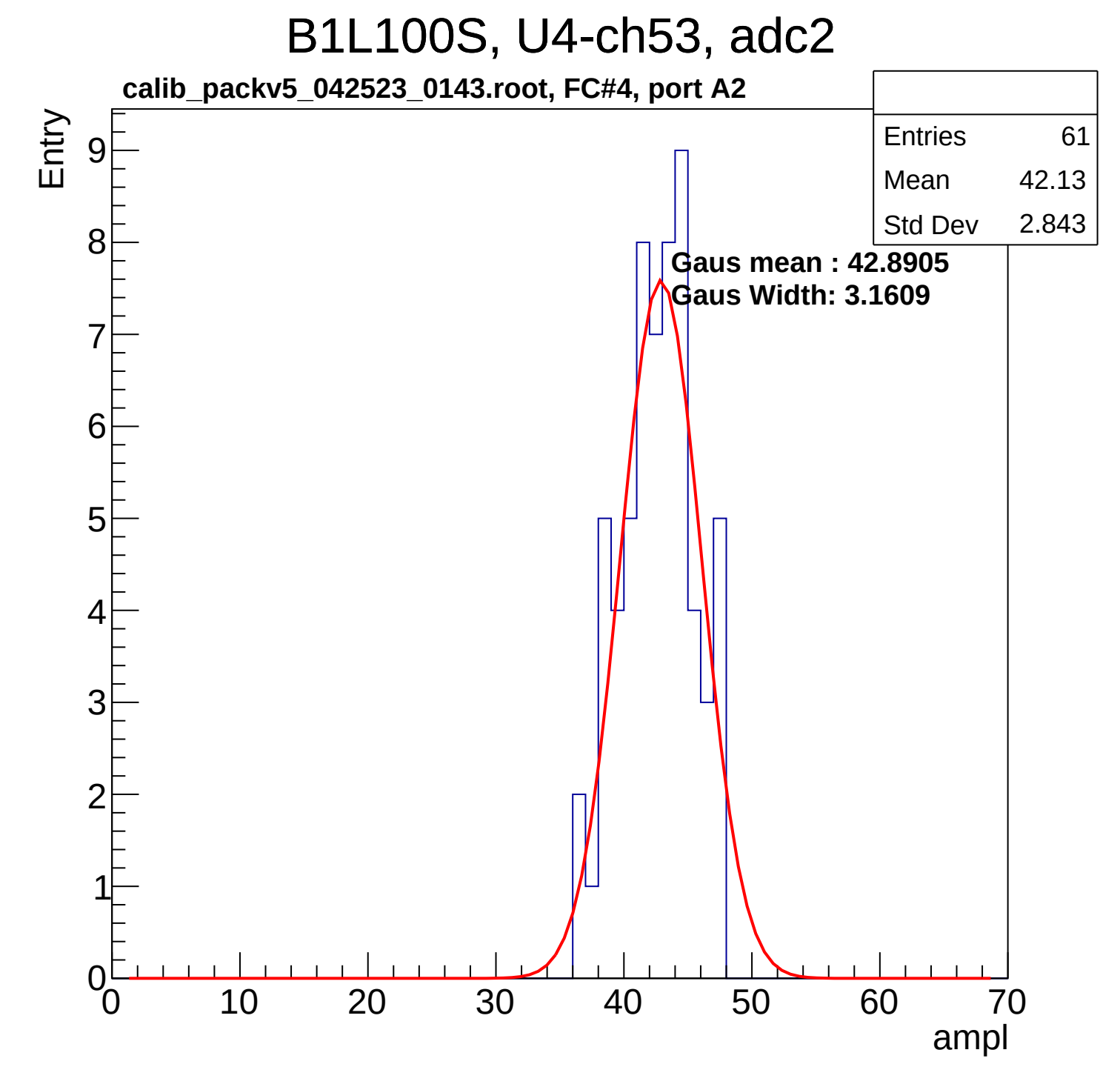

B1L100S, U4-ch52, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 44
Mean 58.18
Std Dev 9.163
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

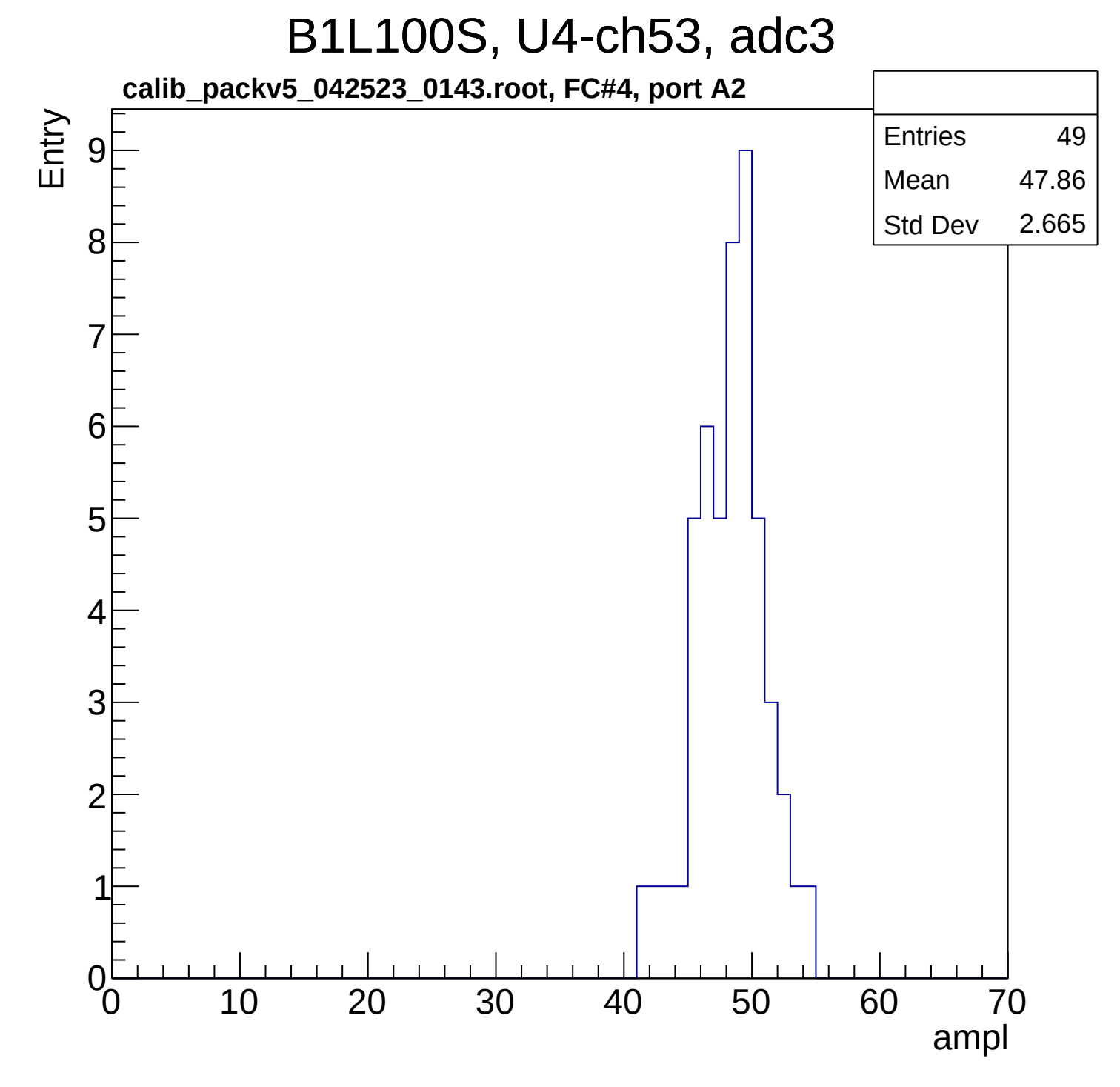

B1L100S, U4-ch52, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 61.64
Std Dev 1.611
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

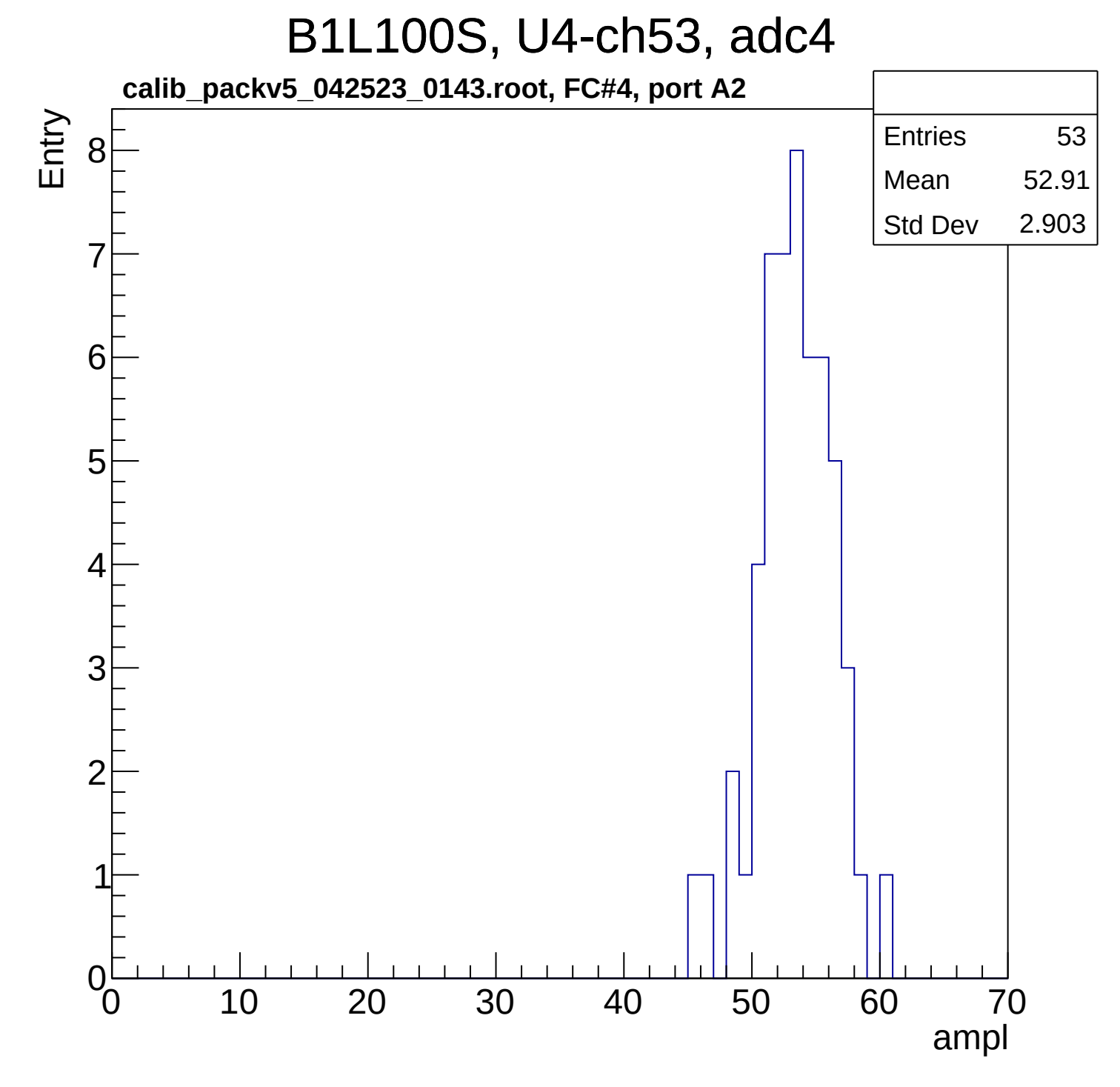

B1L100S, U4-ch52, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

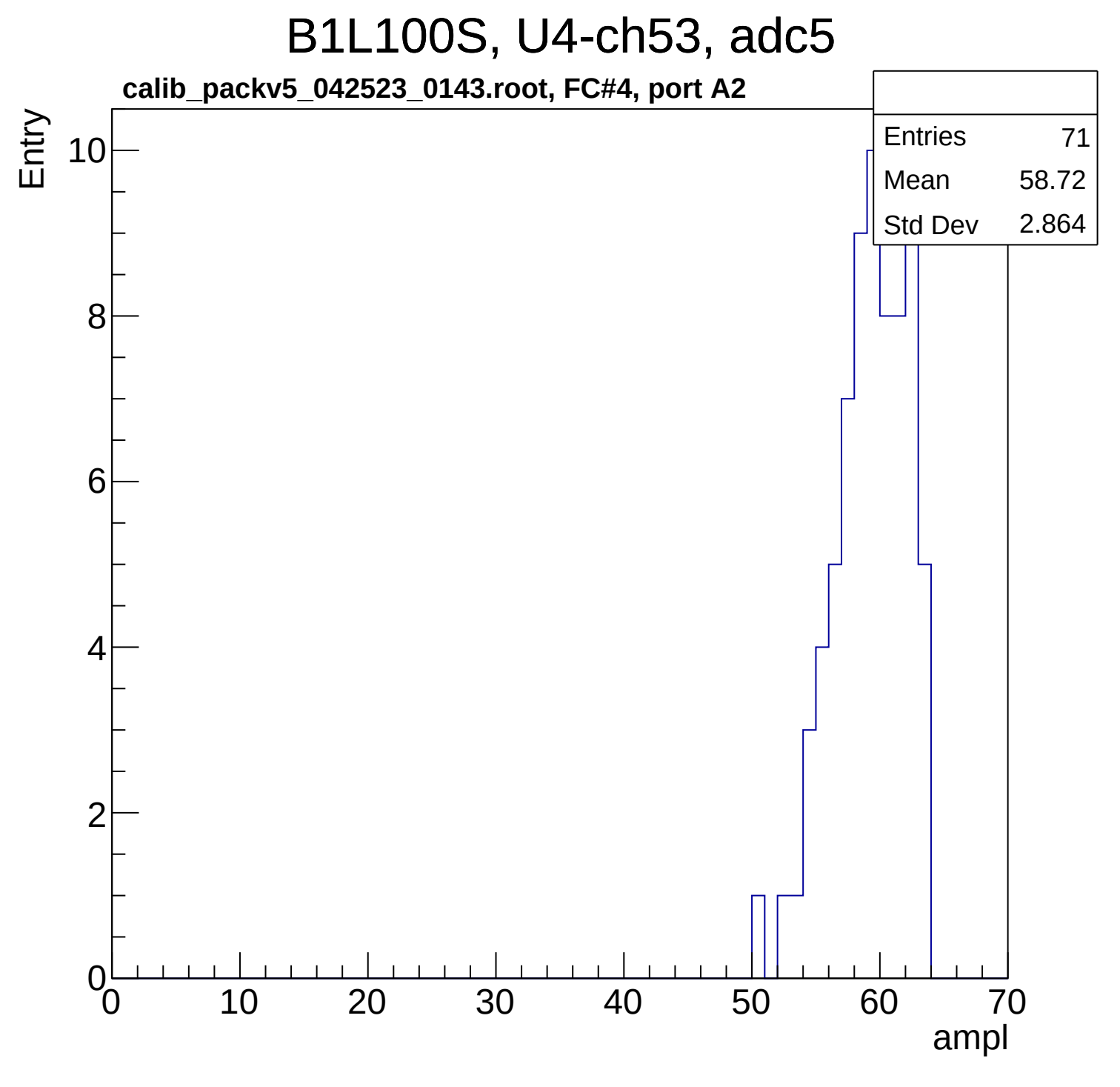

B1L100S, U4-ch53, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 28.49
Std Dev 3.567
Gaus mean : 28.6280
Gaus Width: 4.0748
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

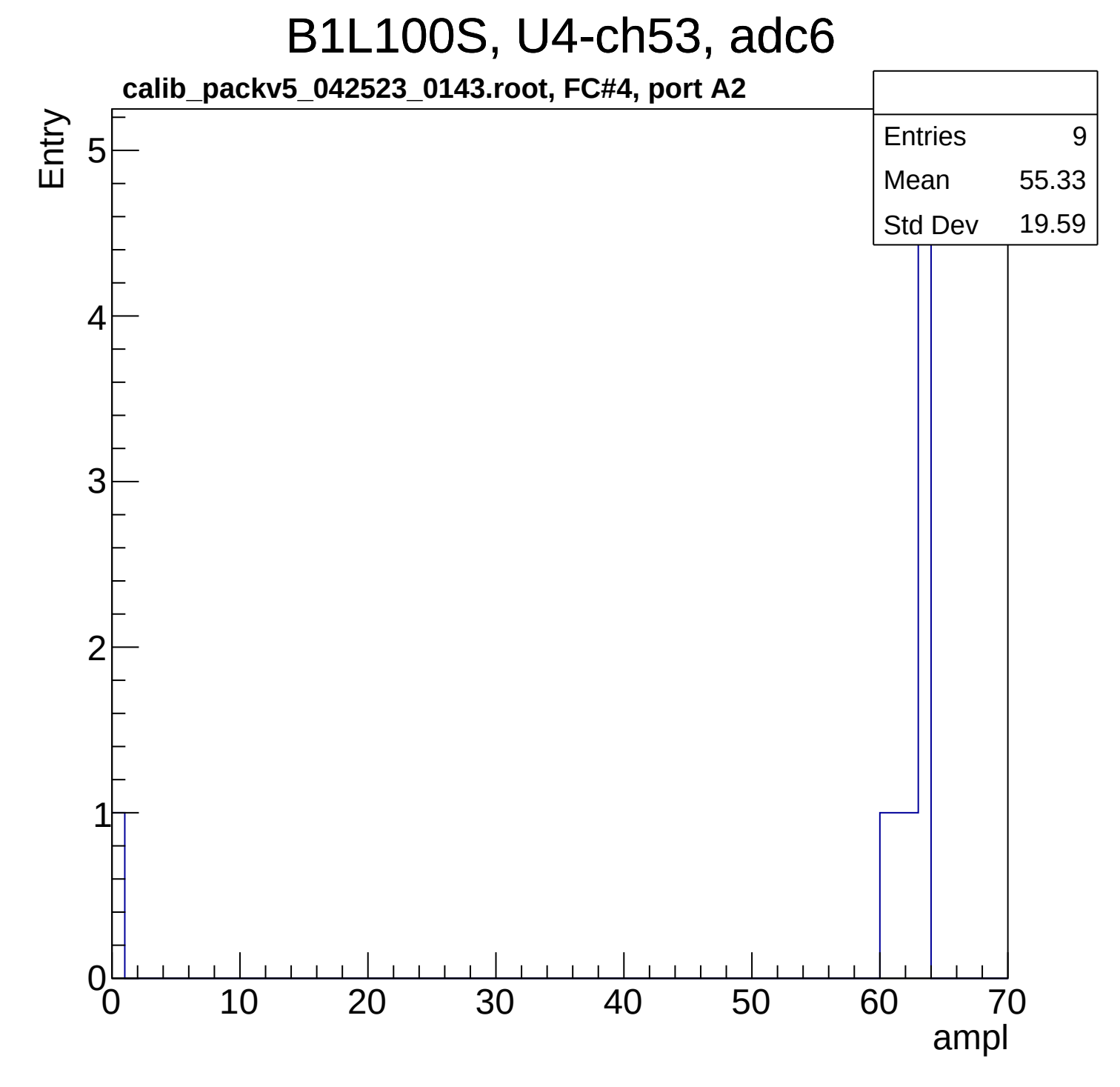

B1L100S, U4-ch53, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 35.09
Std Dev 3.424
Gaus mean : 35.4884
Gaus Width: 3.5248
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

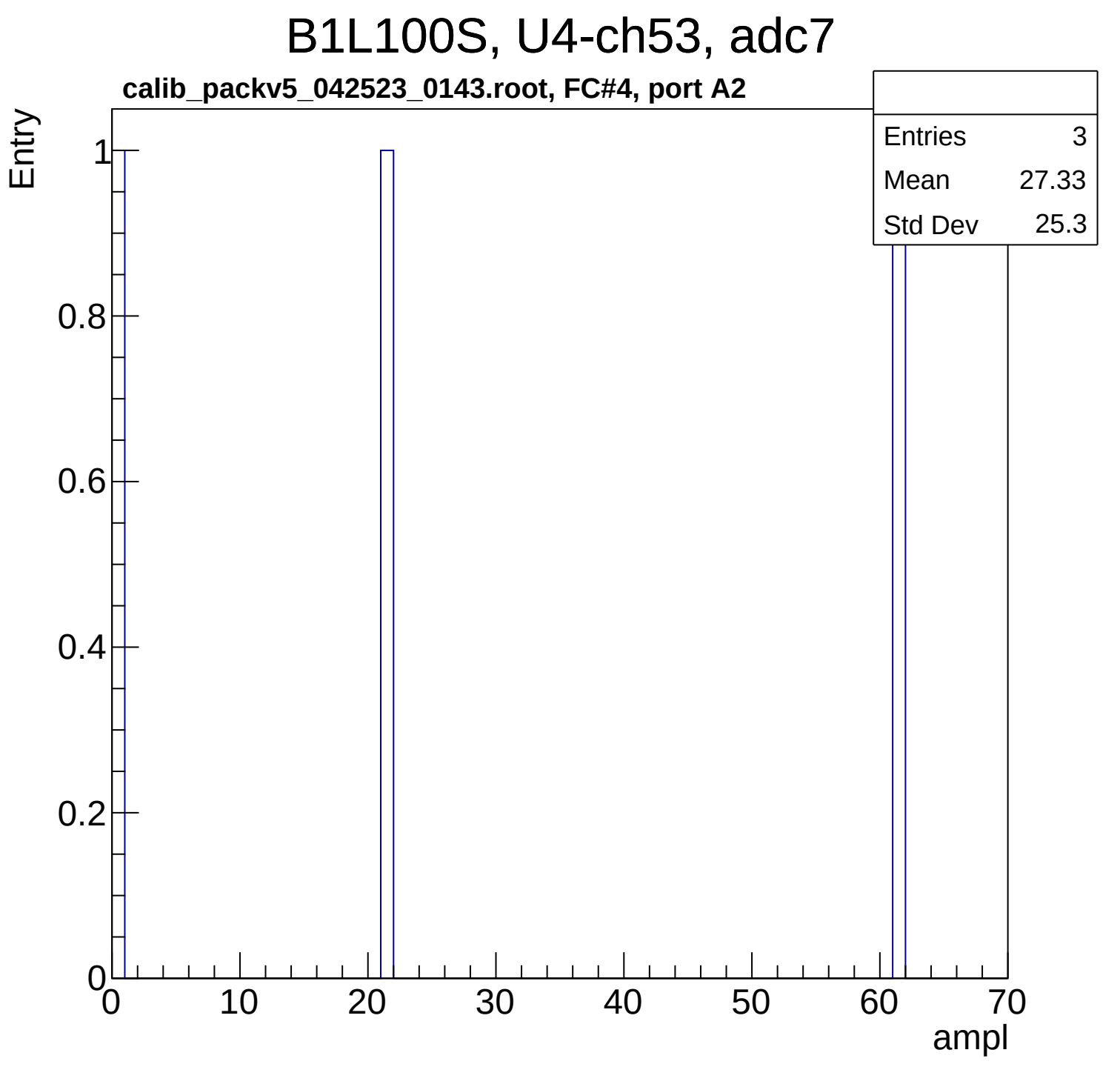

B1L100S, U4-ch53, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 42.13
Std Dev 2.843
Gaus mean : 42.8905
Gaus Width: 3.1609
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

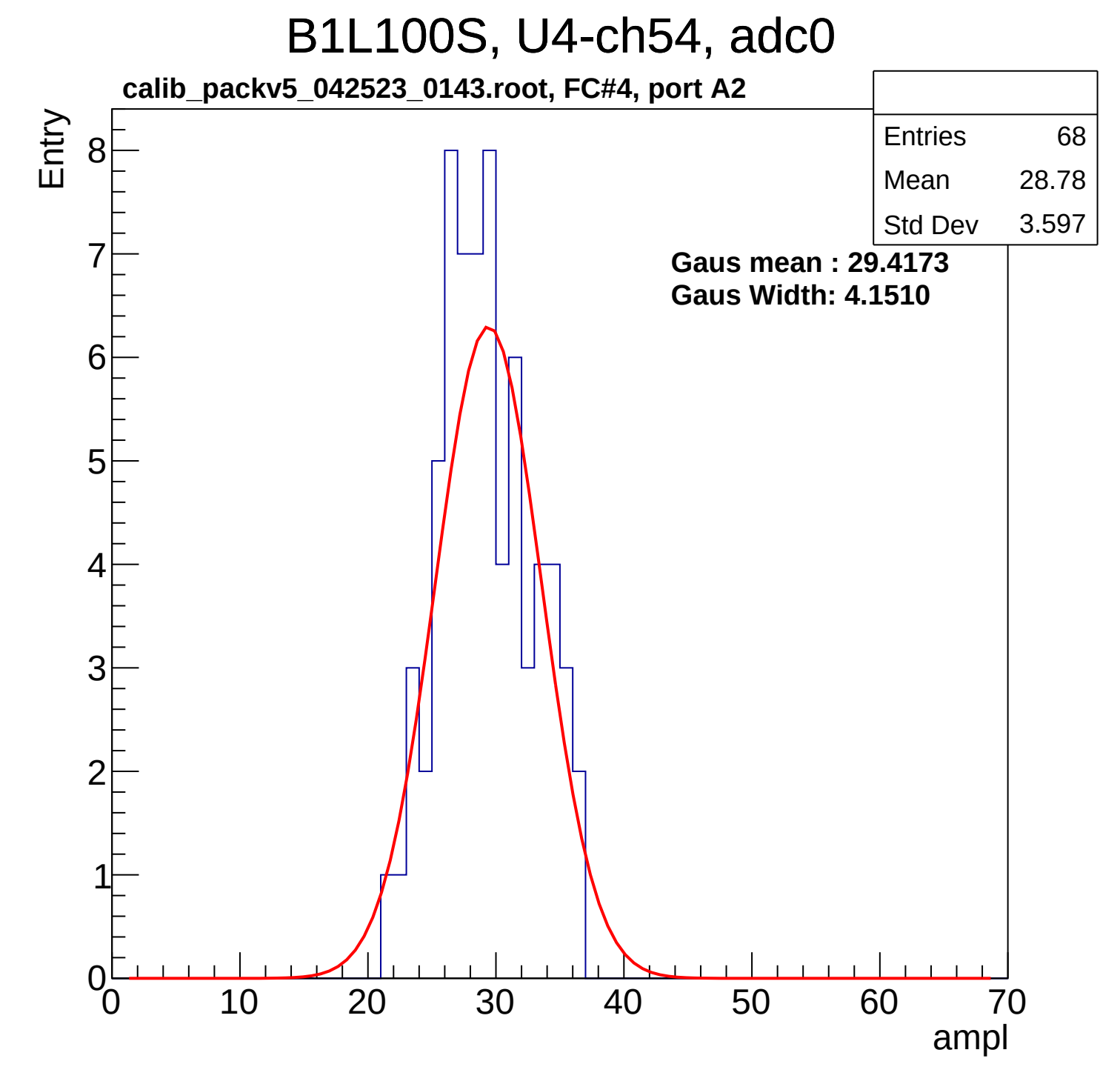

B1L100S, U4-ch53, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 47.86
Std Dev 2.665
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

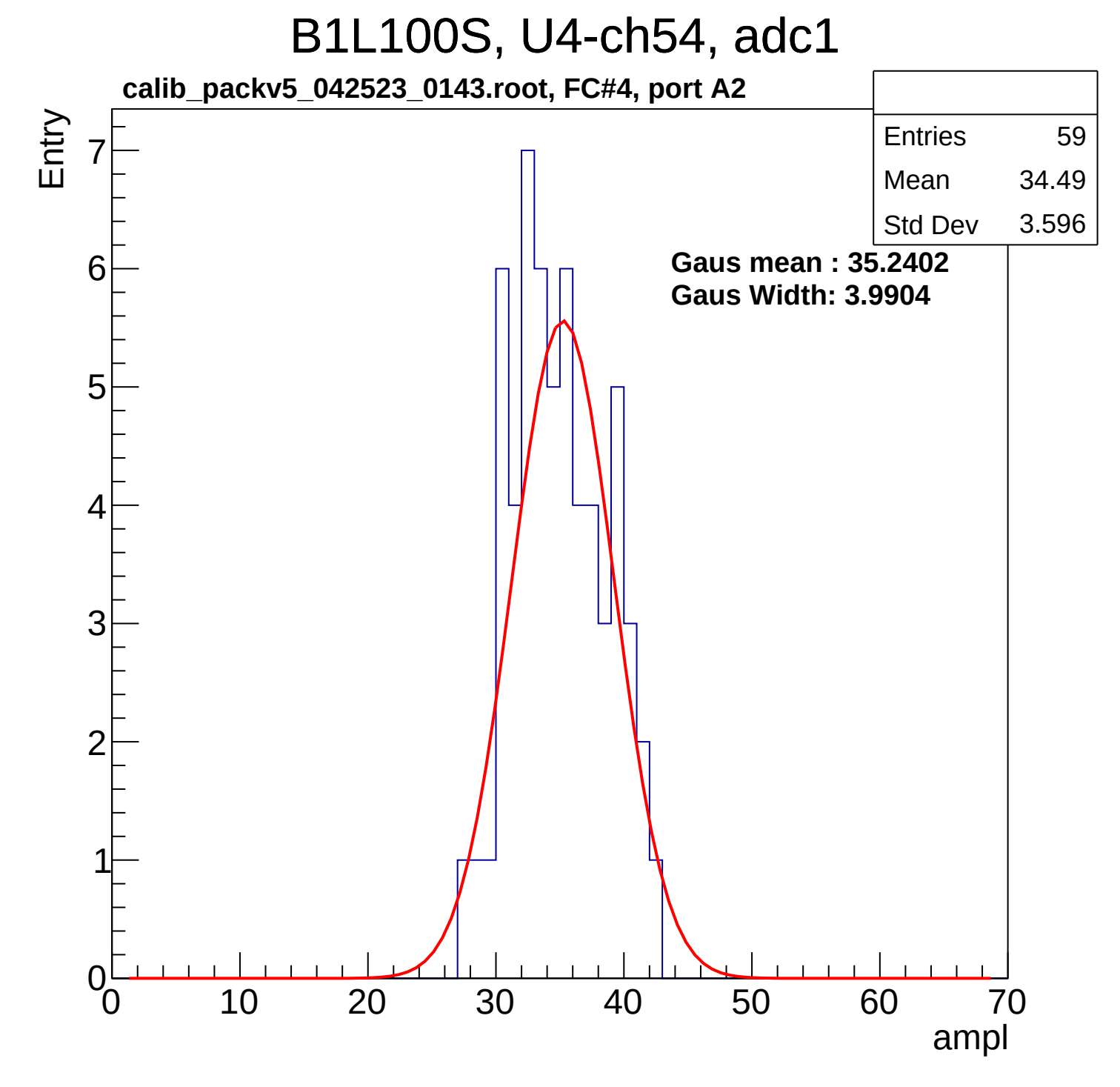

B1L100S, U4-ch53, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 52.91
Std Dev 2.903
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

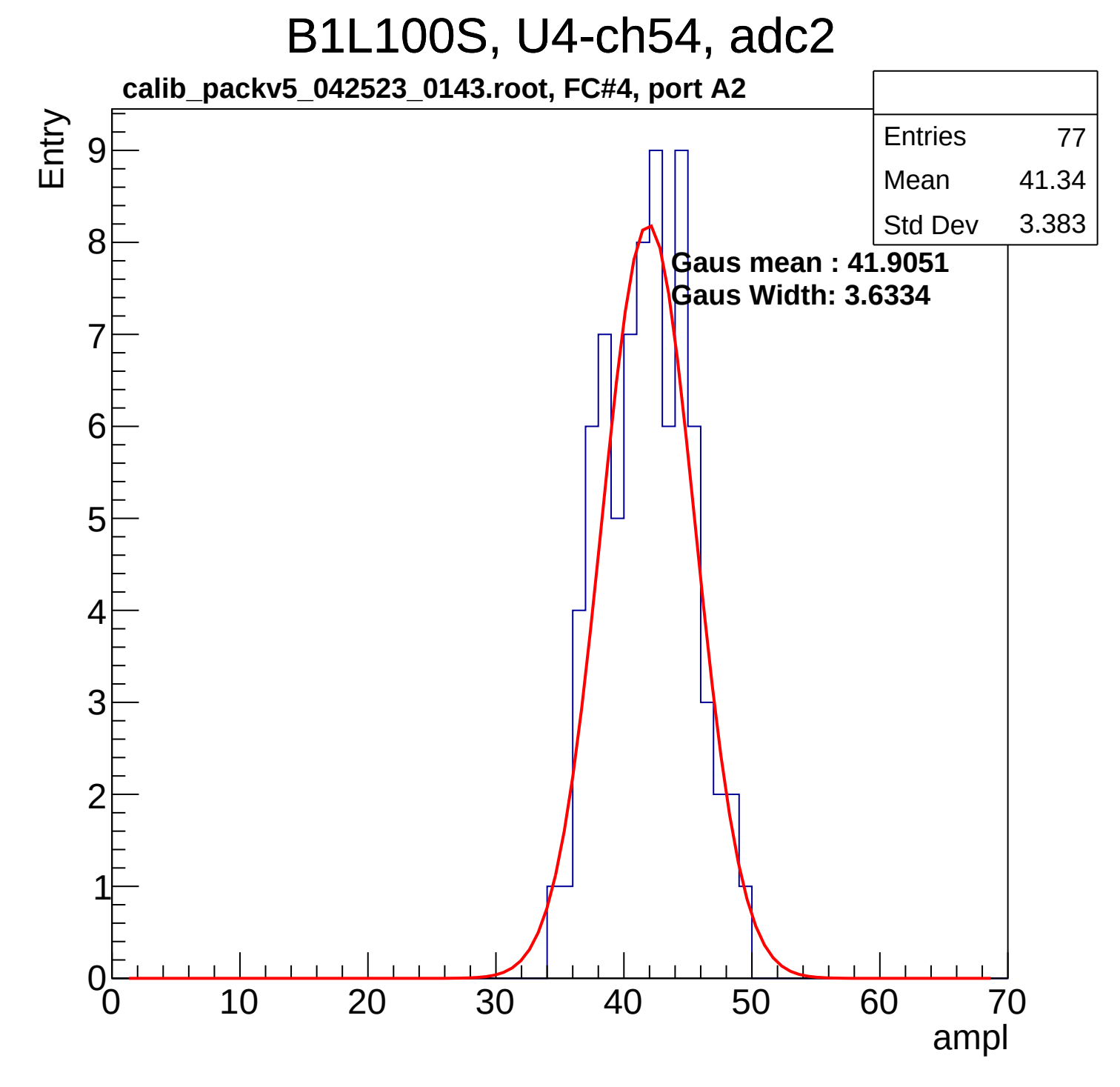

B1L100S, U4-ch53, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 58.72
Std Dev 2.864
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

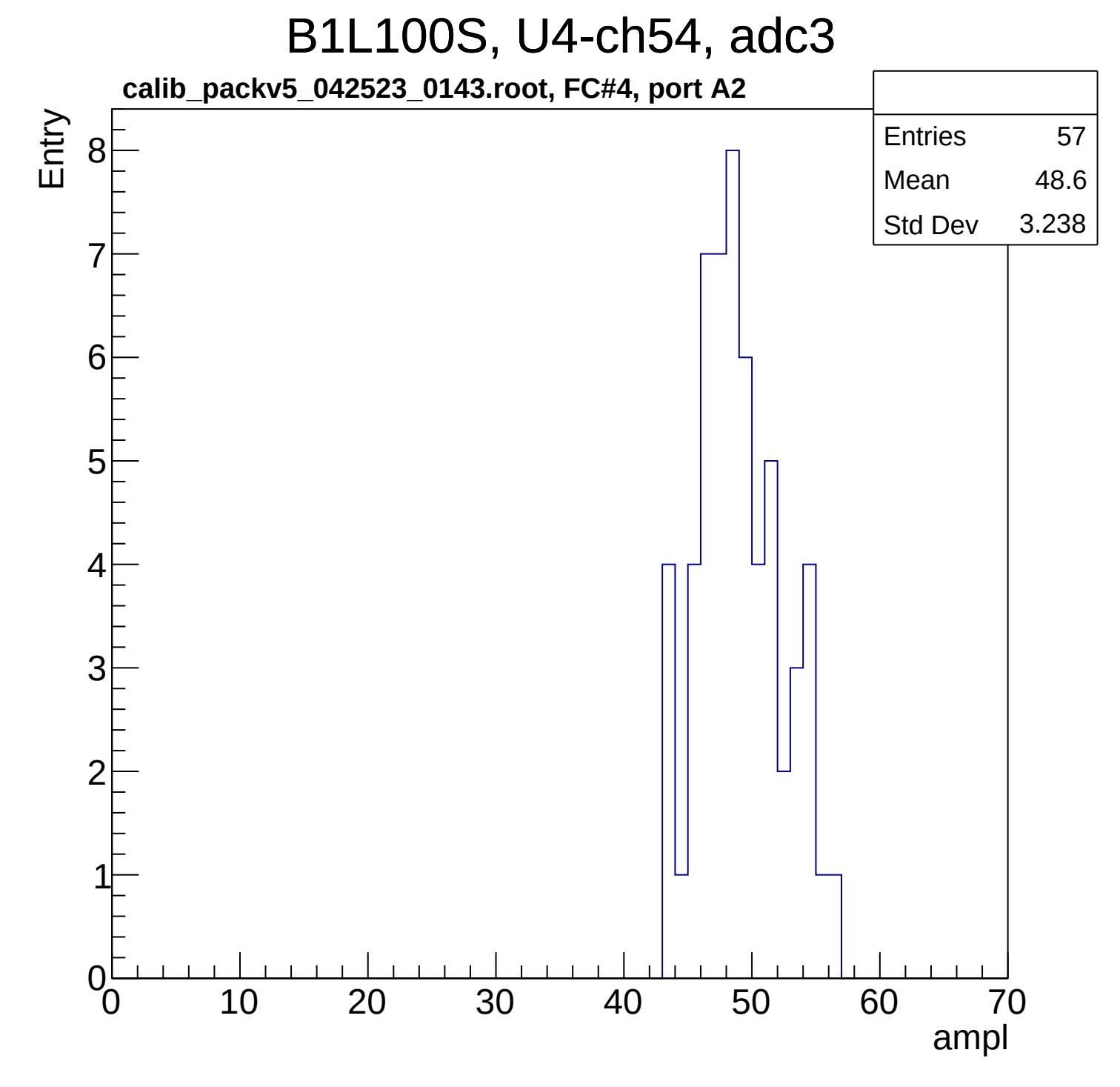

B1L100S, U4-ch53, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 55.33
Std Dev 19.59
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

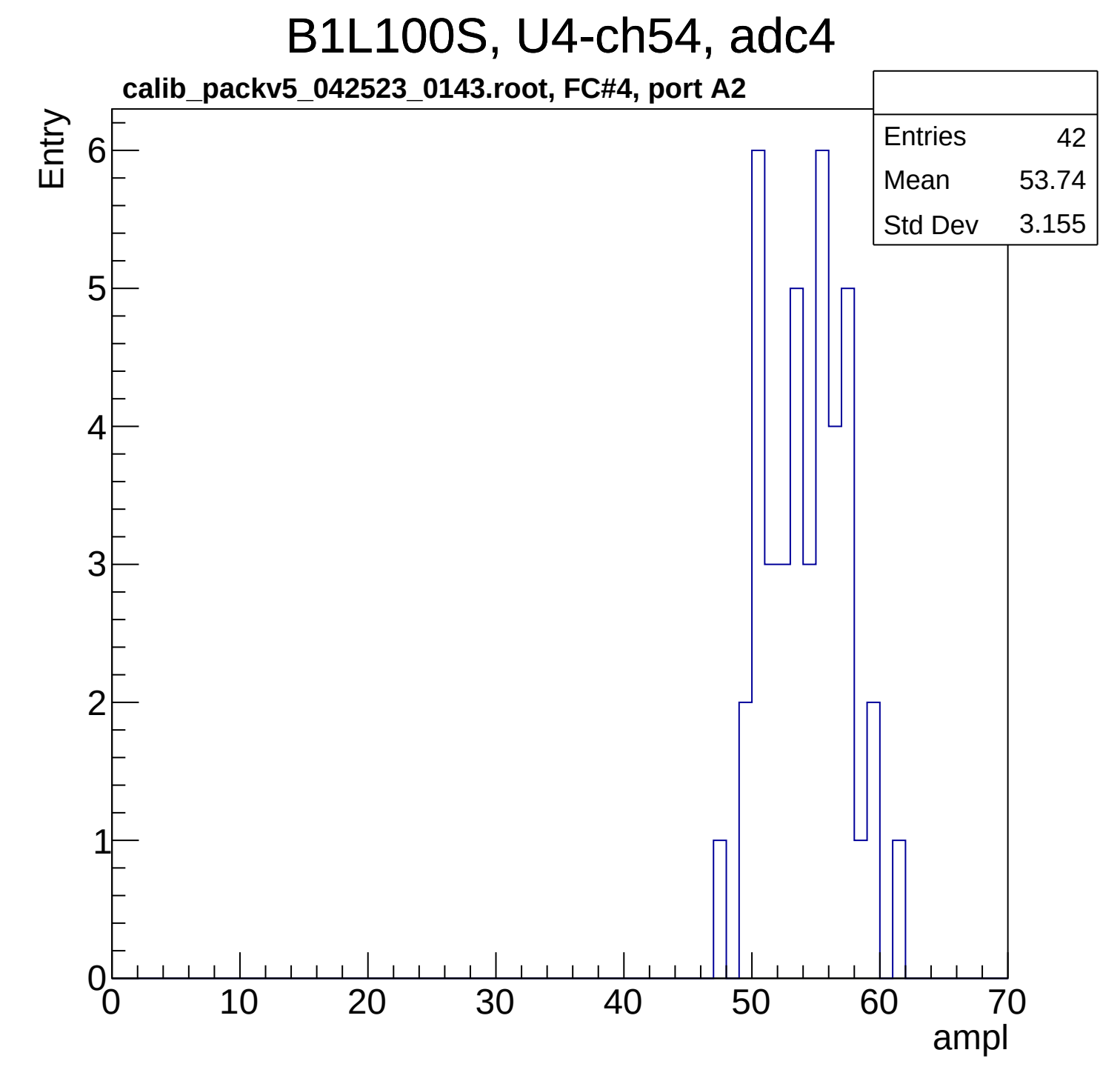

B1L100S, U4-ch53, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 27.33
Std Dev 25.3
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

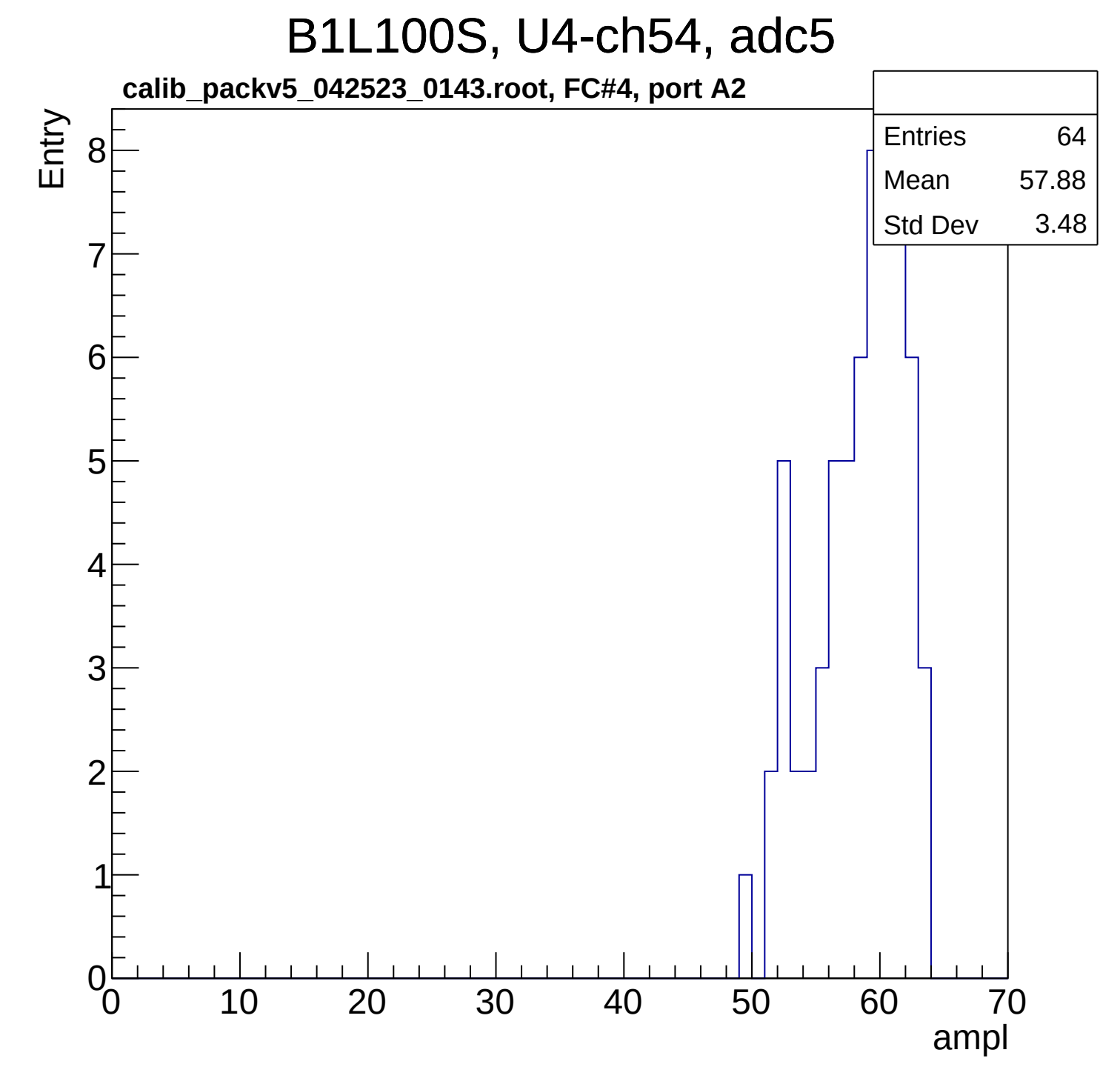

B1L100S, U4-ch54, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 28.78
Std Dev 3.597
Gaus mean : 29.4173
Gaus Width: 4.1510
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

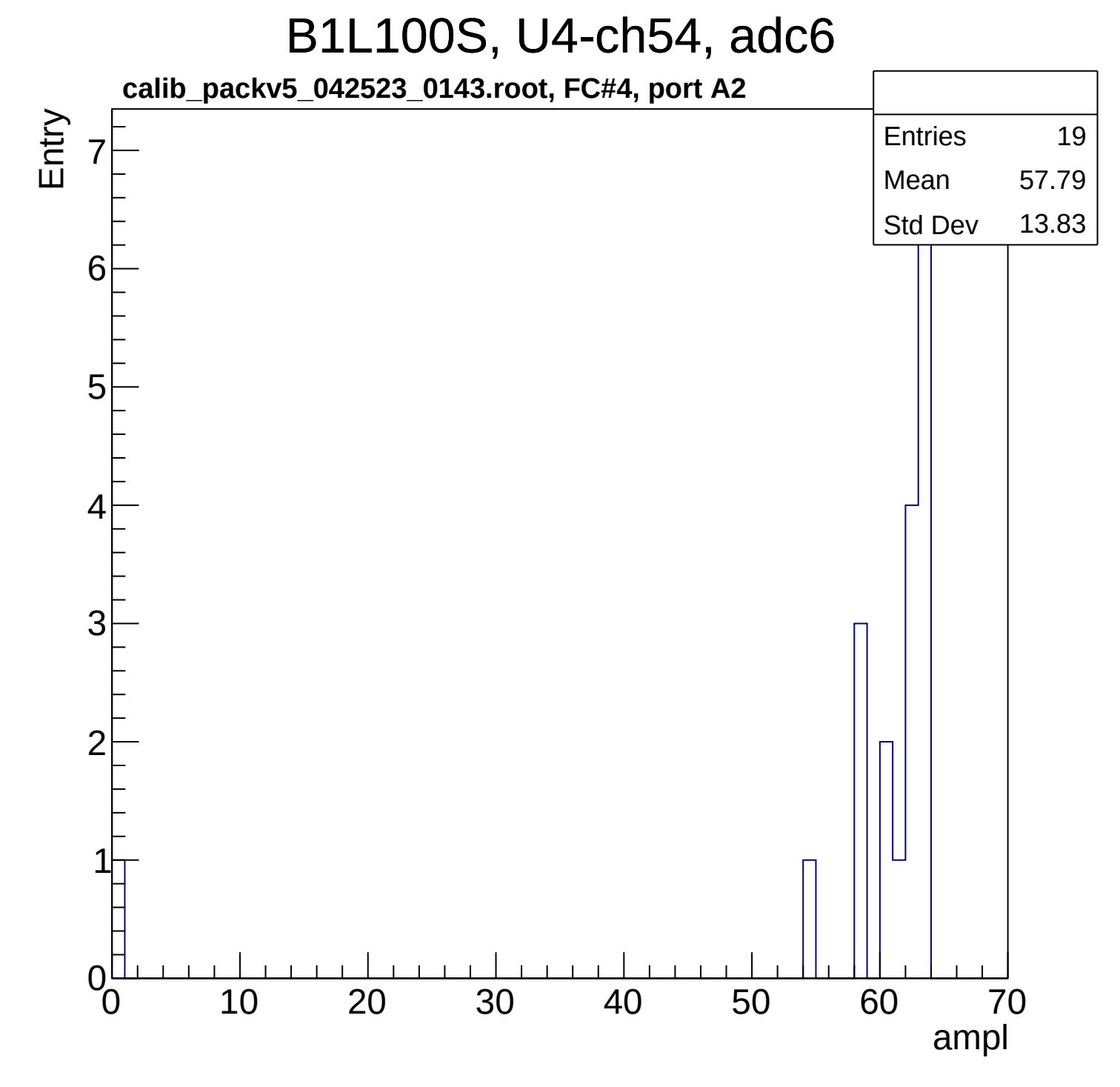

B1L100S, U4-ch54, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 34.49
Std Dev 3.596
Gaus mean : 35.2402
Gaus Width: 3.9904
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

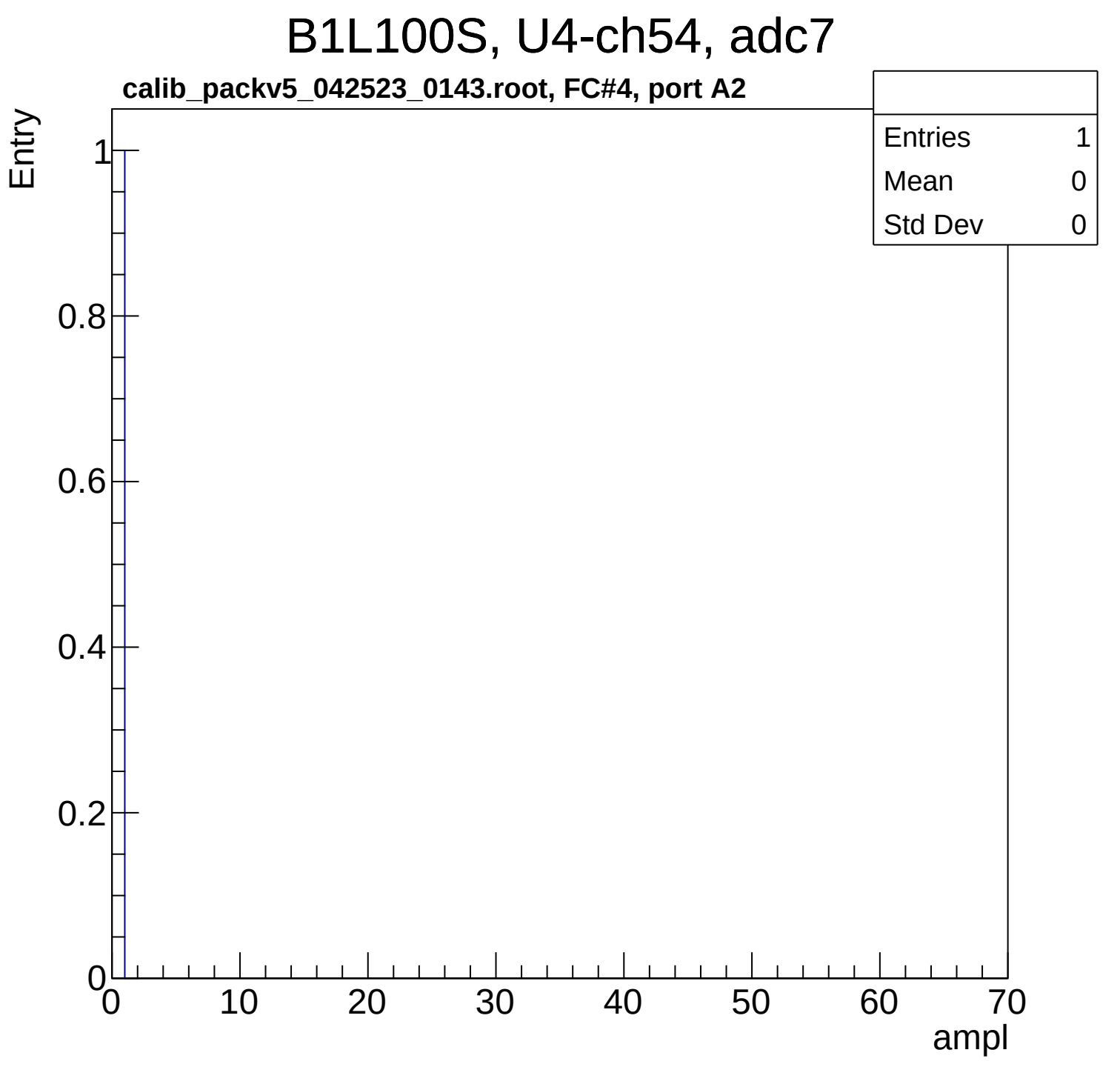

B1L100S, U4-ch54, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 41.34
Std Dev 3.383
Gaus mean : 41.9051
Gaus Width: 3.6334
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

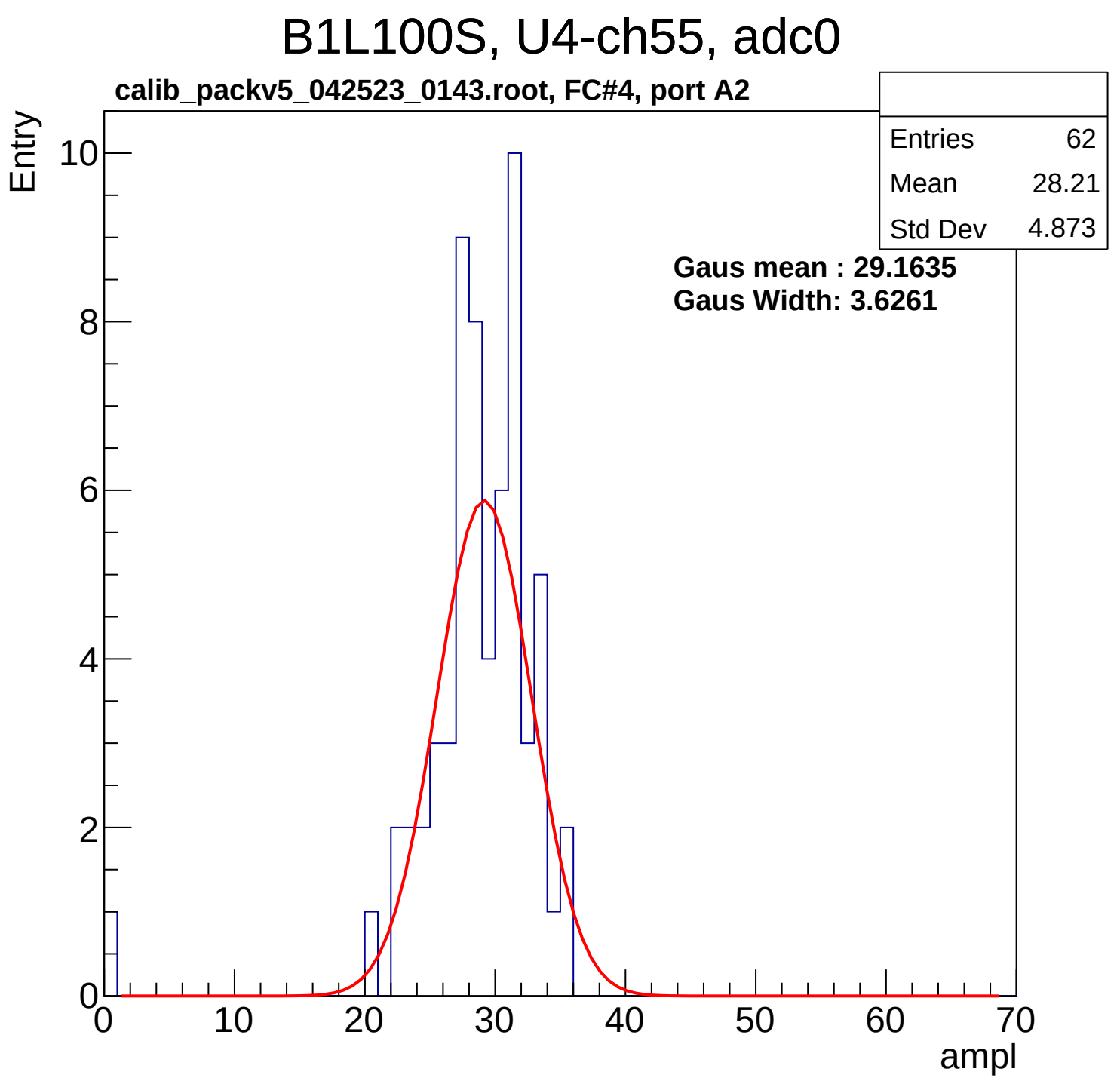

B1L100S, U4-ch54, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 48.6
Std Dev 3.238
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

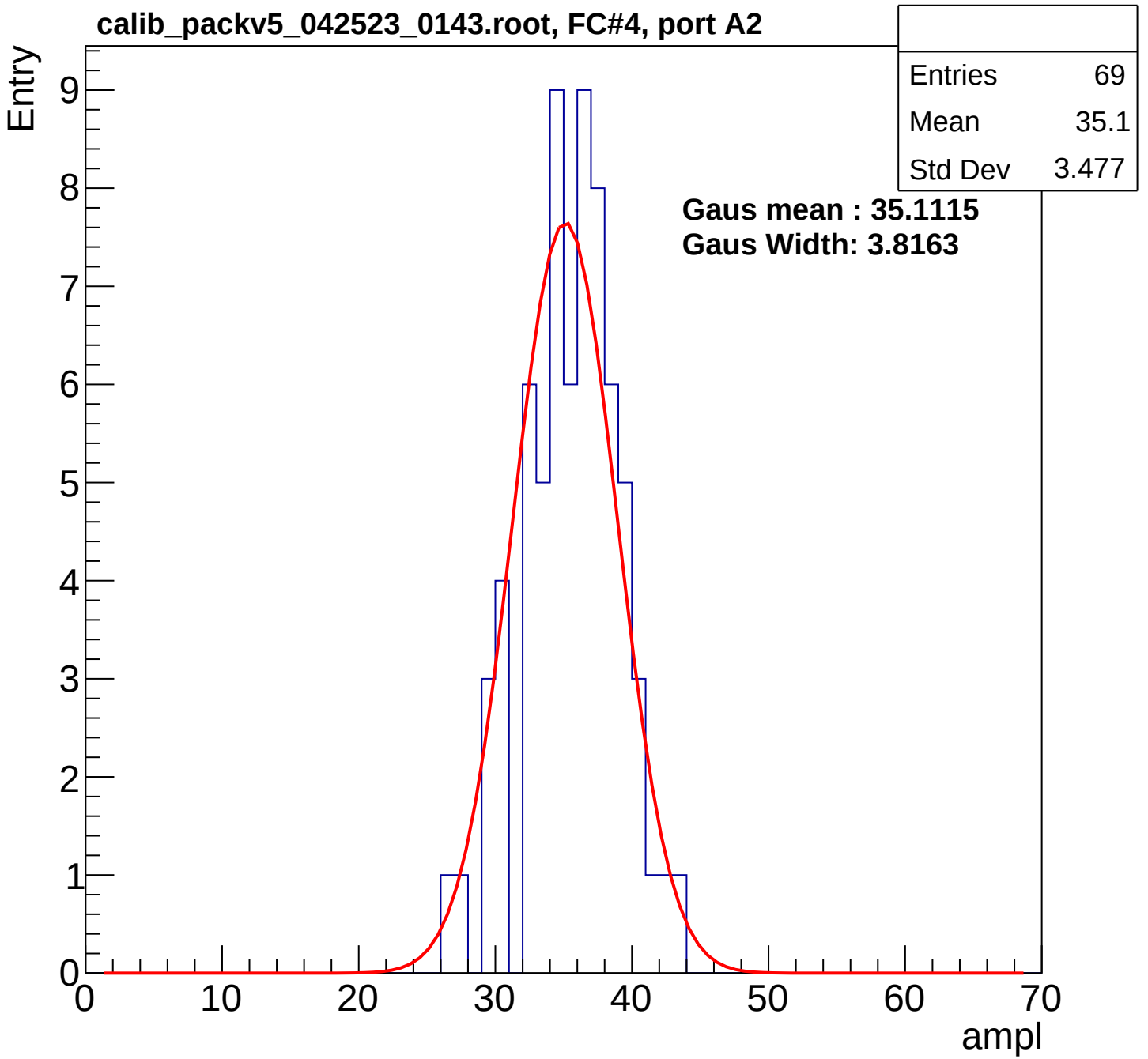

B1L100S, U4-ch54, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 42
Mean 53.74
Std Dev 3.155
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

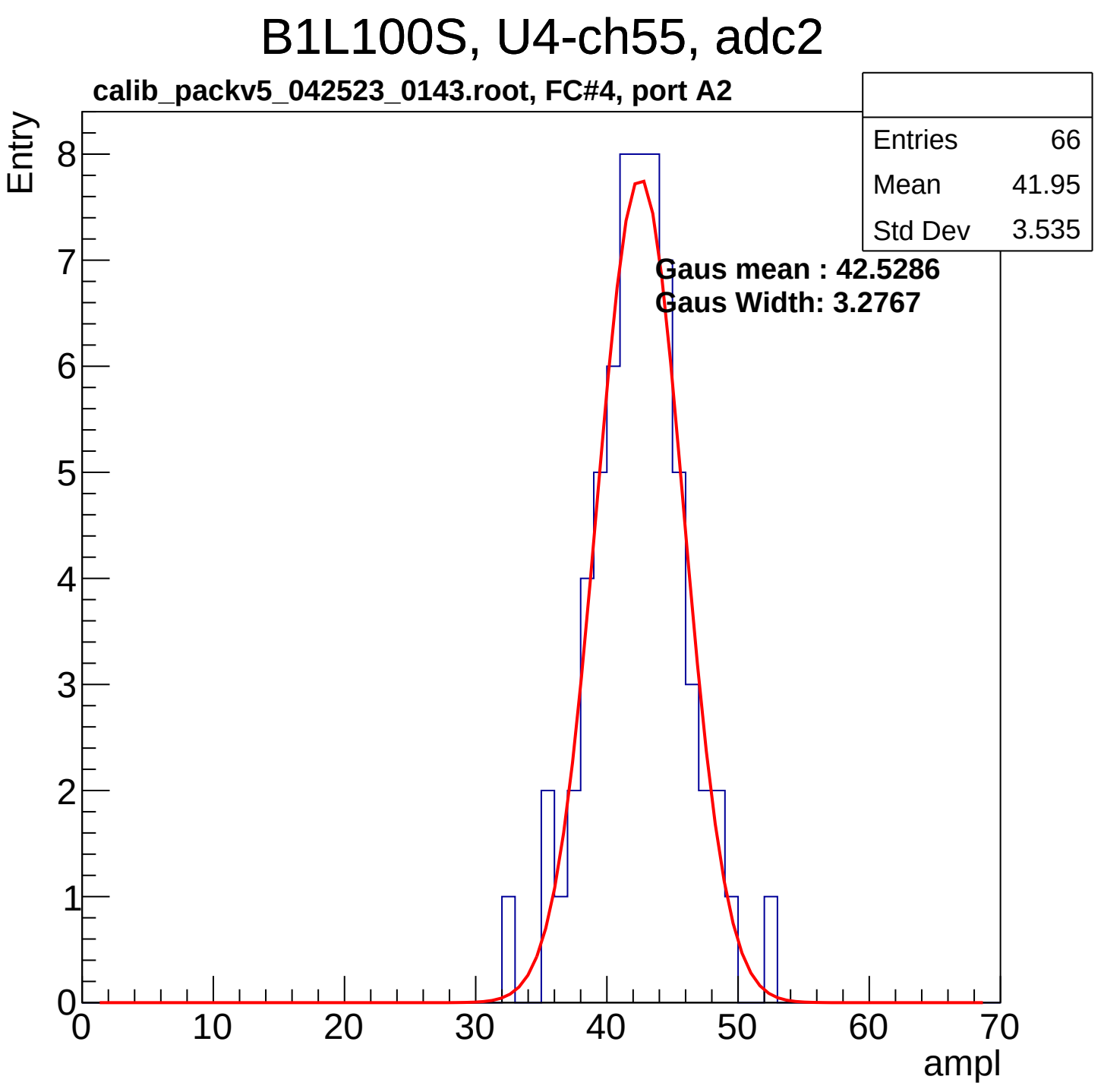

B1L100S, U4-ch54, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 57.88
Std Dev 3.48
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

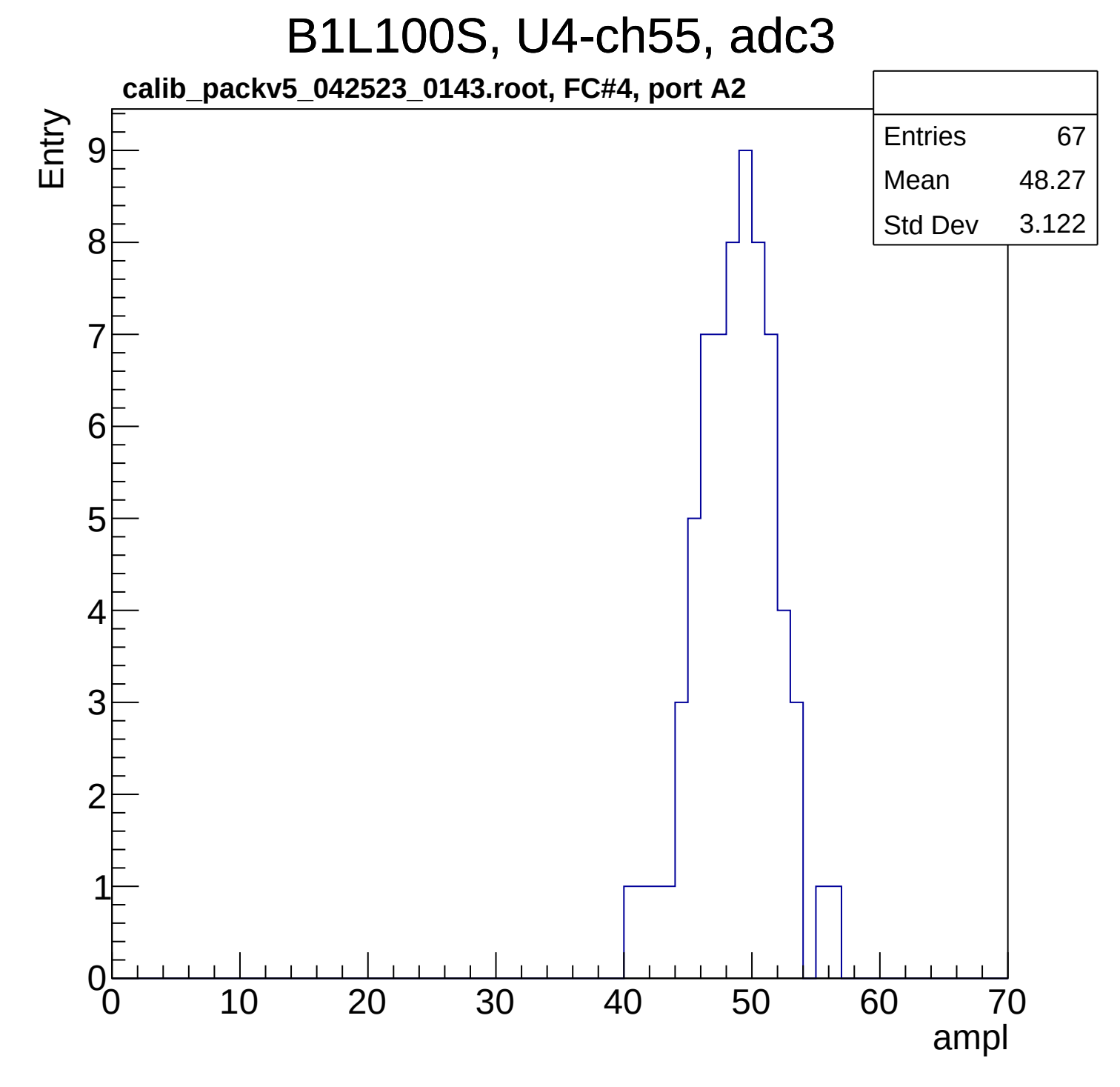

B1L100S, U4-ch54, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 19
Mean 57.79
Std Dev 13.83
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

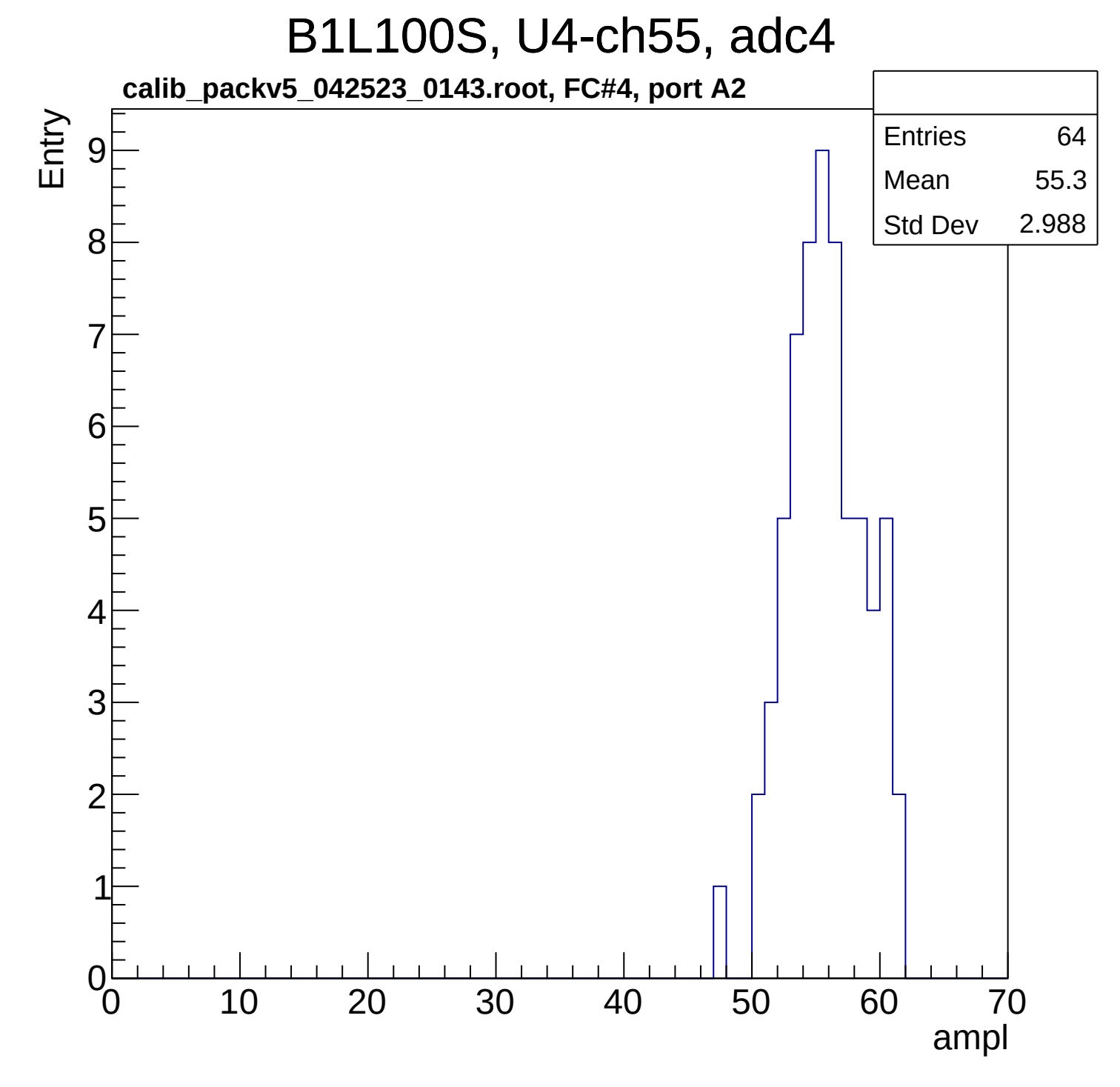

B1L100S, U4-ch54, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

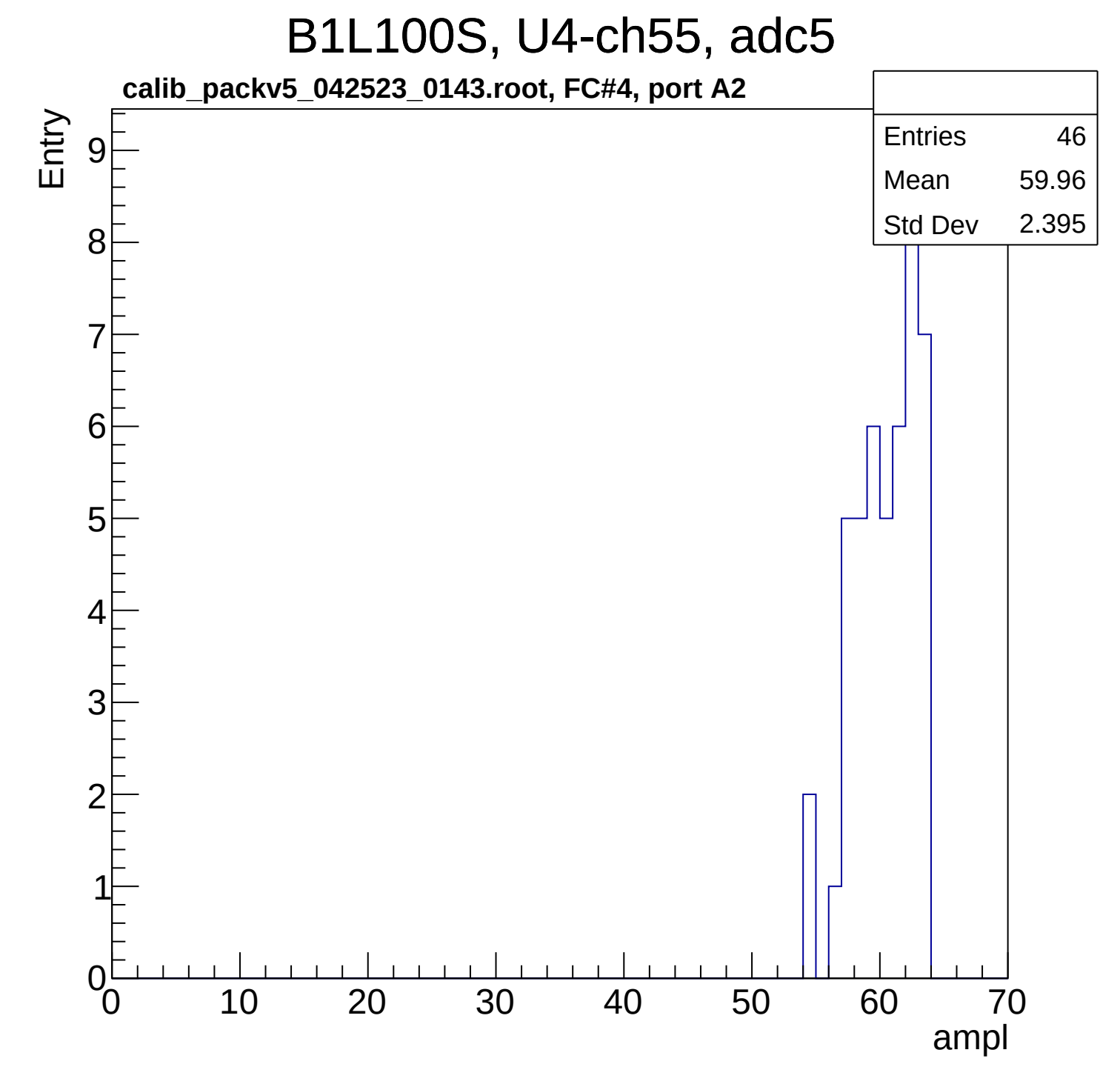

B1L100S, U4-ch55, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 28.21
Std Dev 4.873
Gaus mean : 29.1635
Gaus Width: 3.6261
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

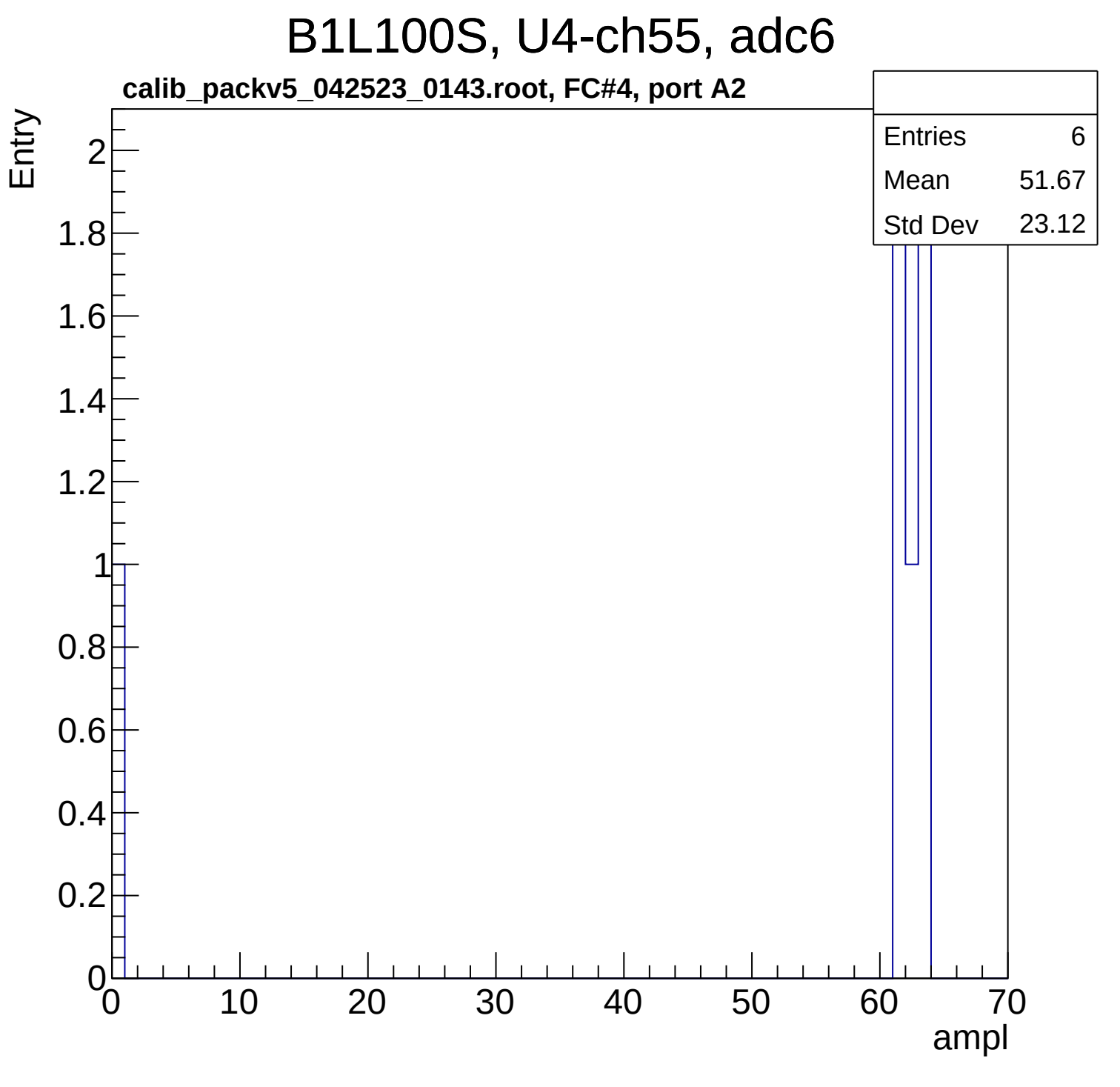

B1L100S, U4-ch55, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 35.1
Std Dev 3.477
Gaus mean : 35.1115
Gaus Width: 3.8163
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

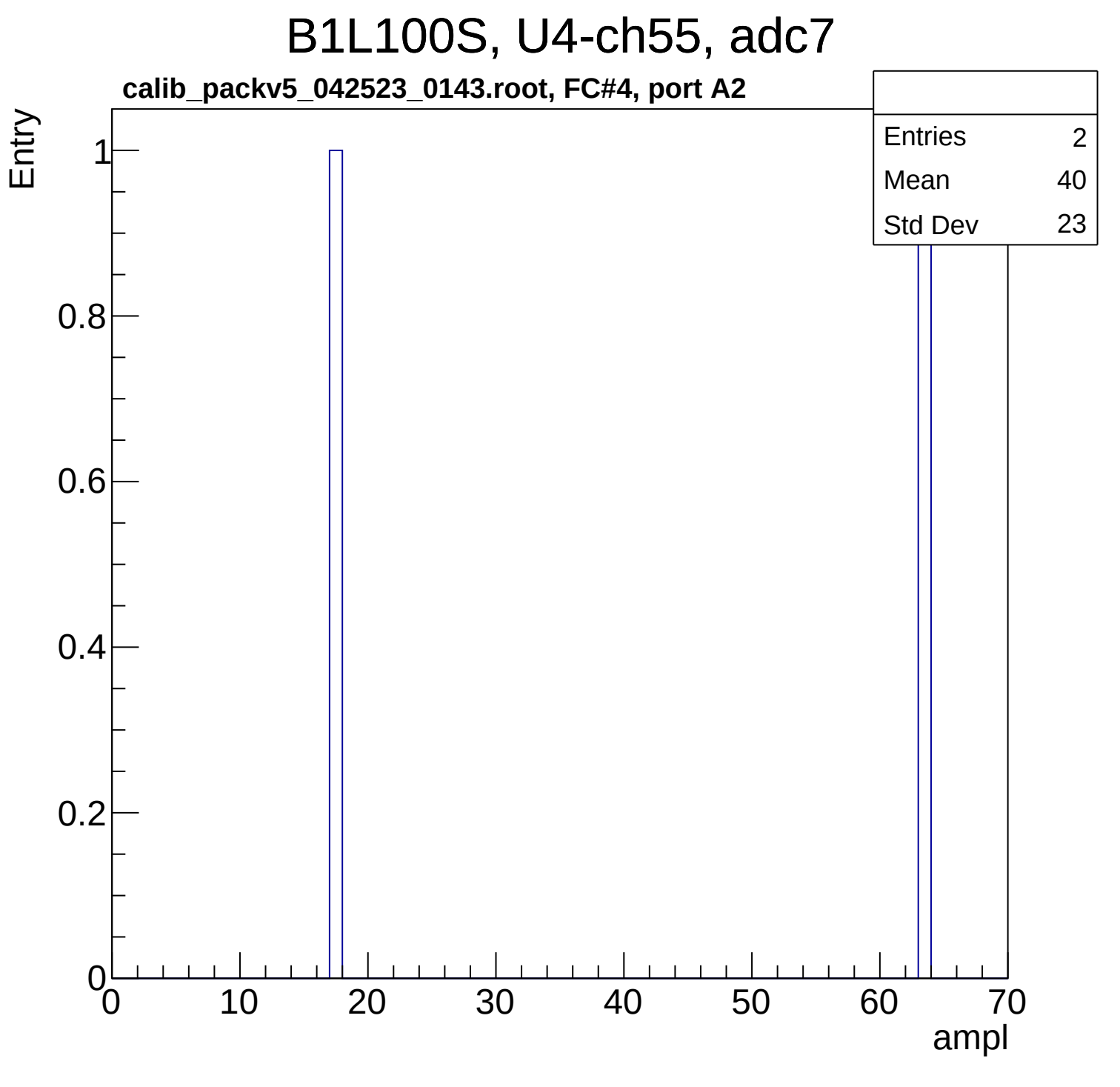

B1L100S, U4-ch55, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 41.95
Std Dev 3.535
Gaus mean : 42.5286
Gaus Width: 3.2767
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

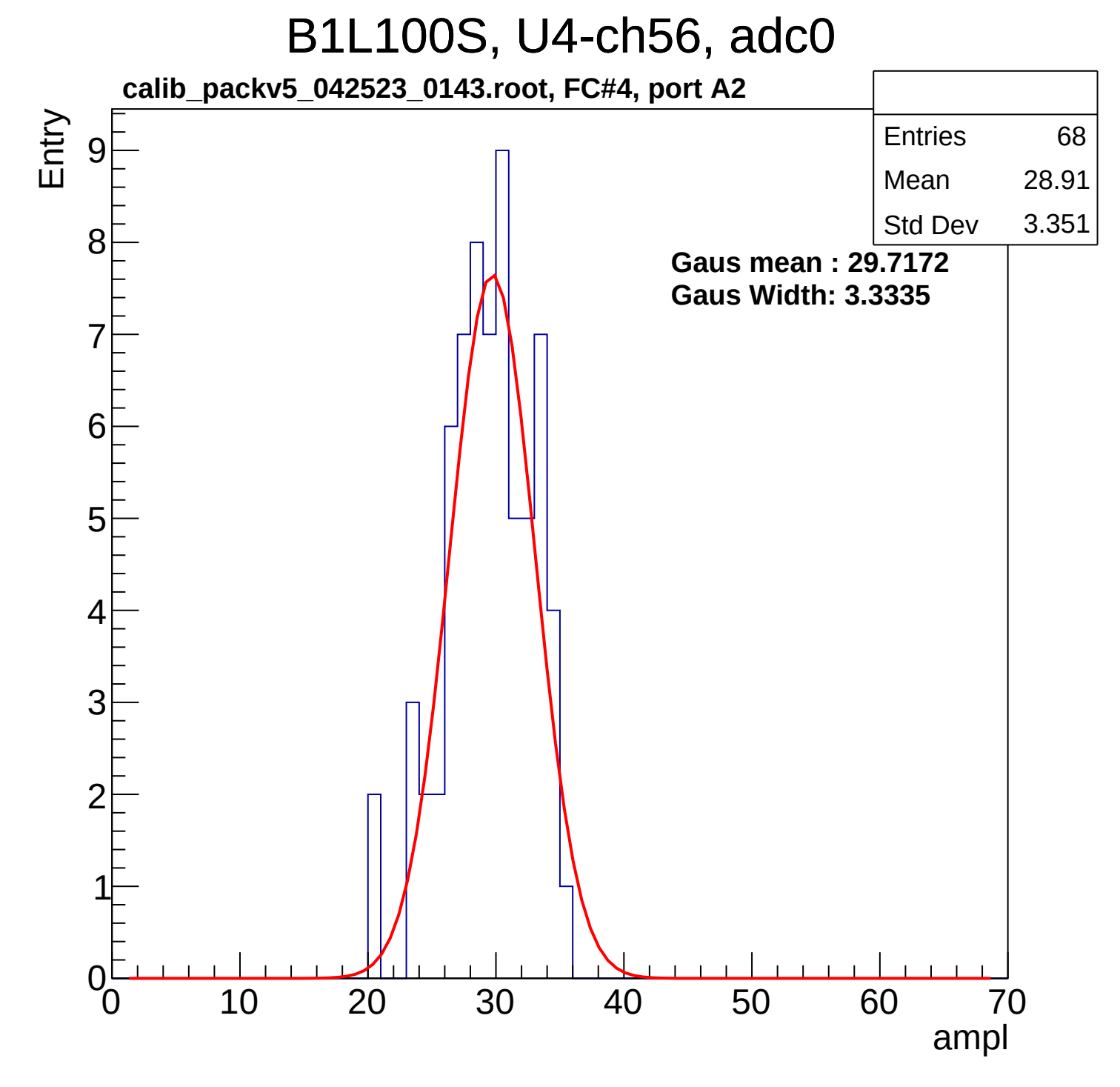

B1L100S, U4-ch55, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 48.27
Std Dev 3.122
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

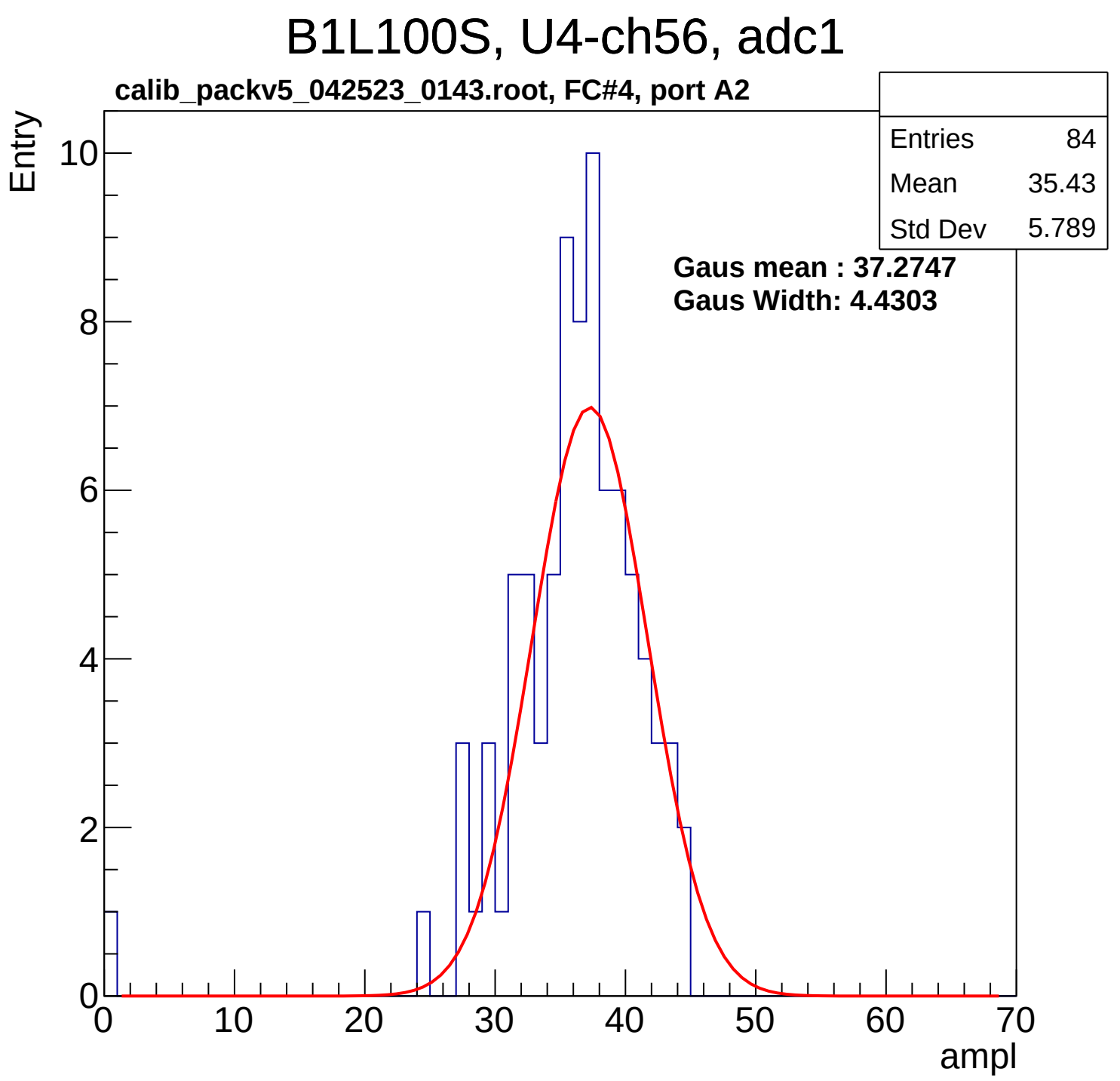

B1L100S, U4-ch55, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 55.3
Std Dev 2.988
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

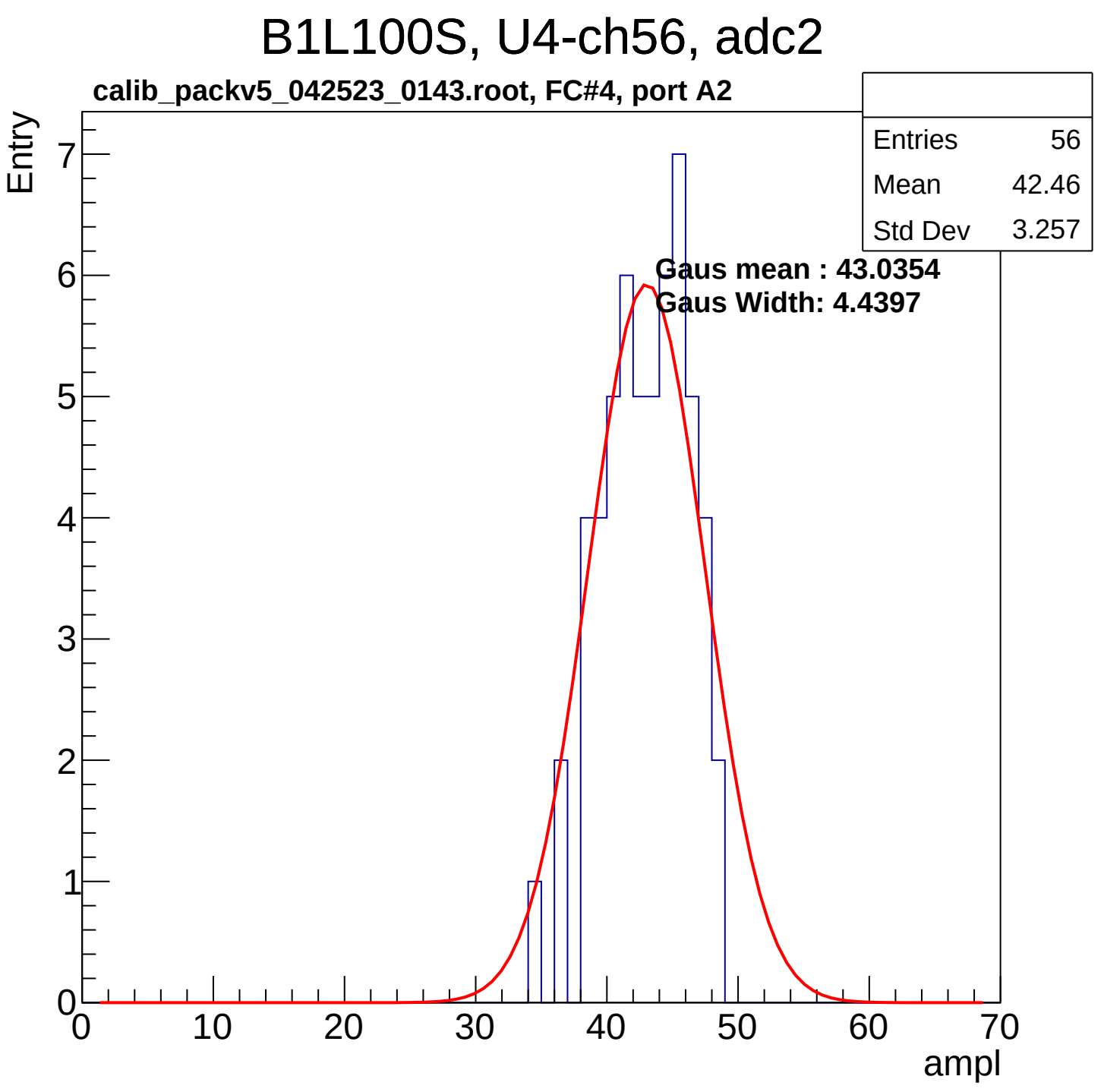

B1L100S, U4-ch55, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 59.96
Std Dev 2.395
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

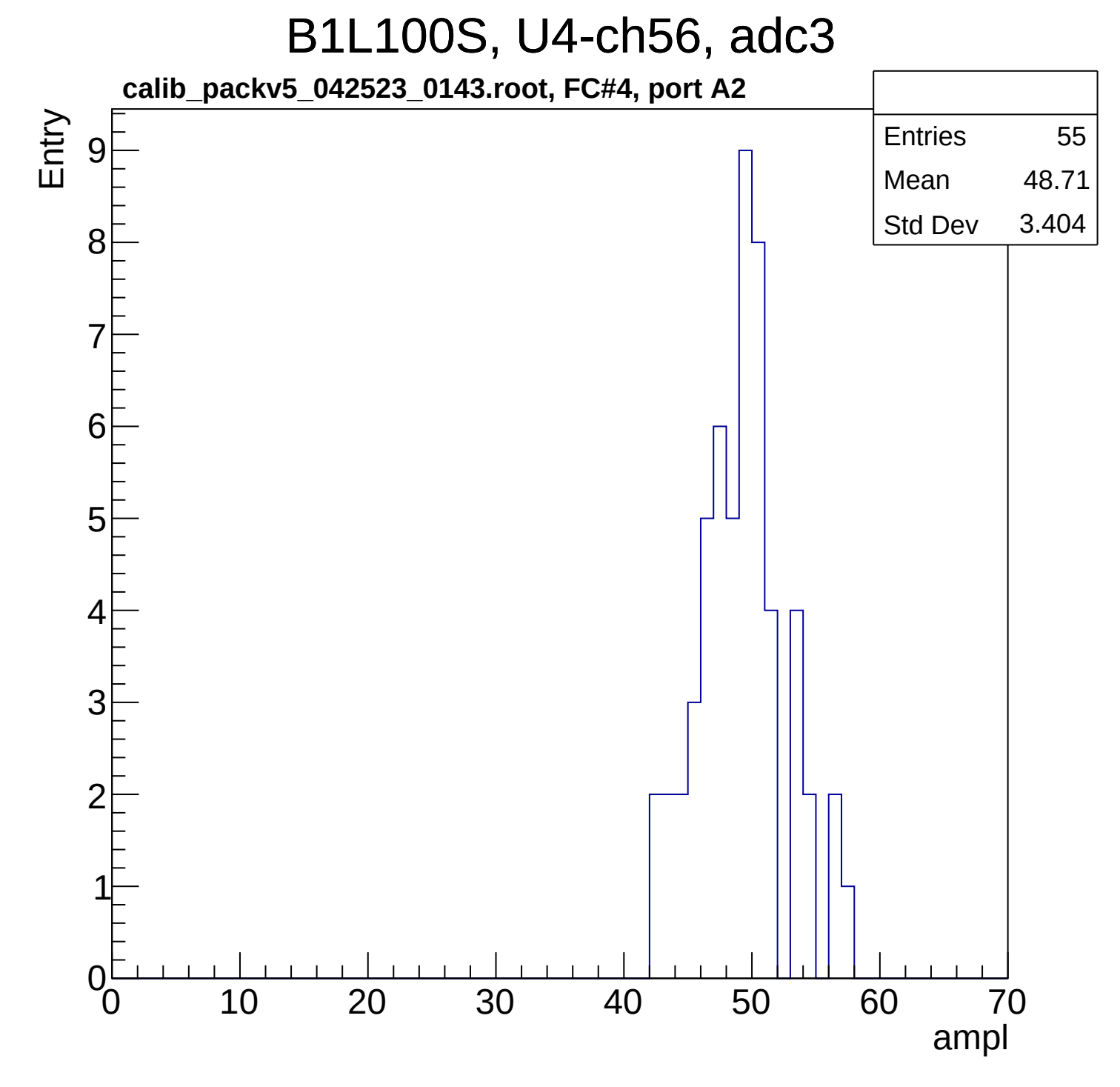

B1L100S, U4-ch55, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 51.67
Std Dev 23.12
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

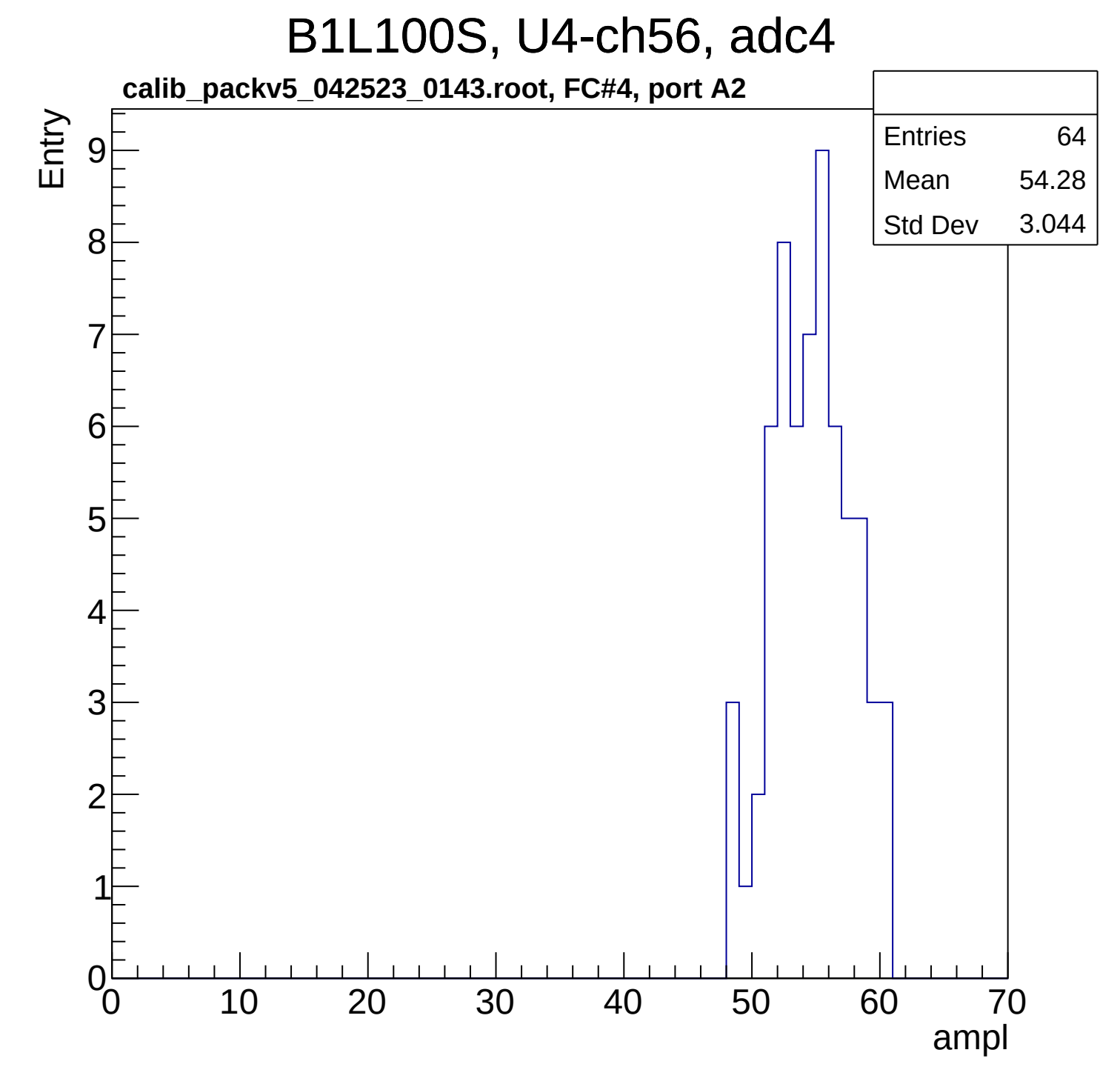

B1L100S, U4-ch55, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 40
Std Dev 23
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

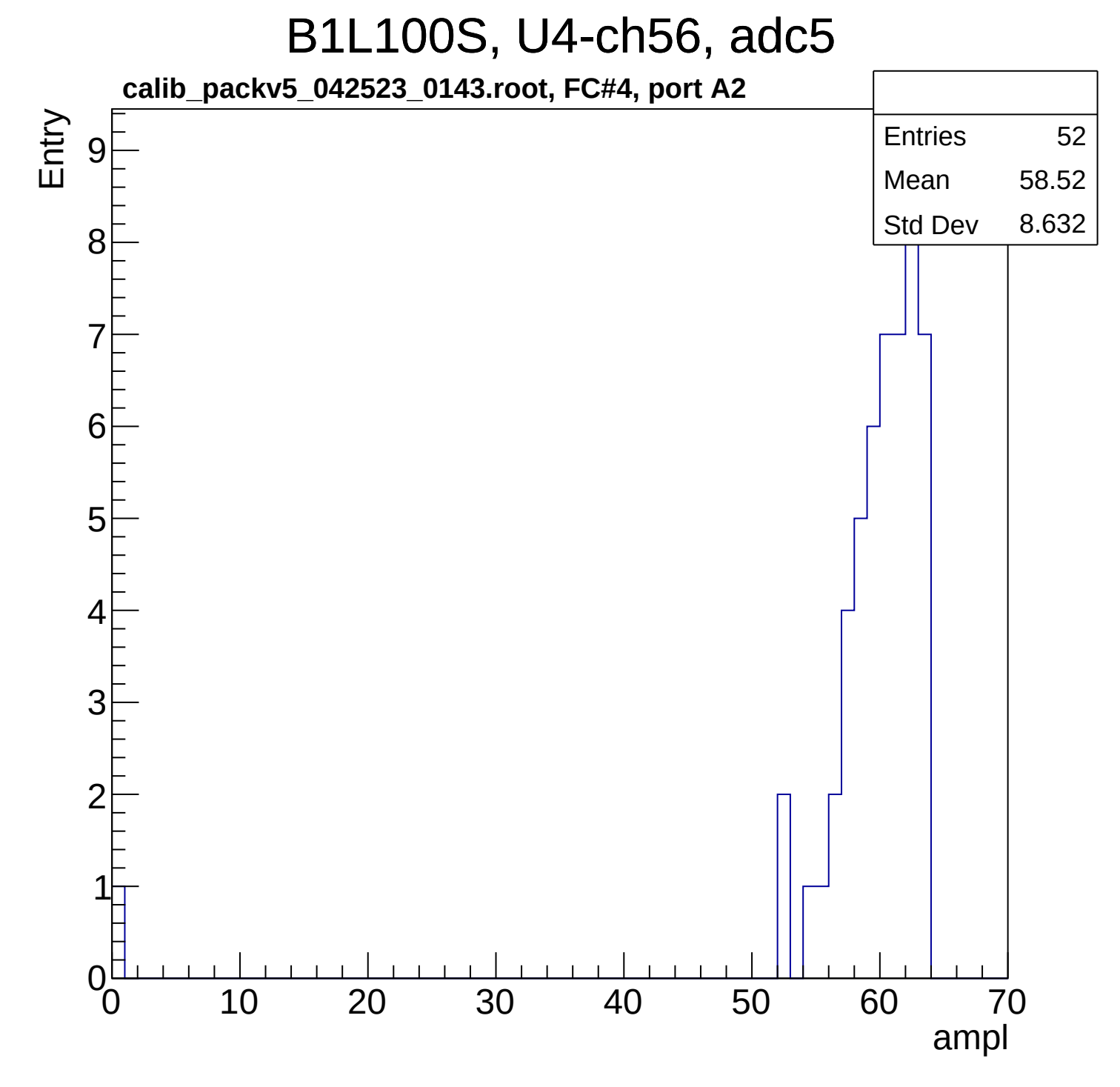

B1L100S, U4-ch56, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 28.91
Std Dev 3.351
Gaus mean : 29.7172
Gaus Width: 3.3335
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

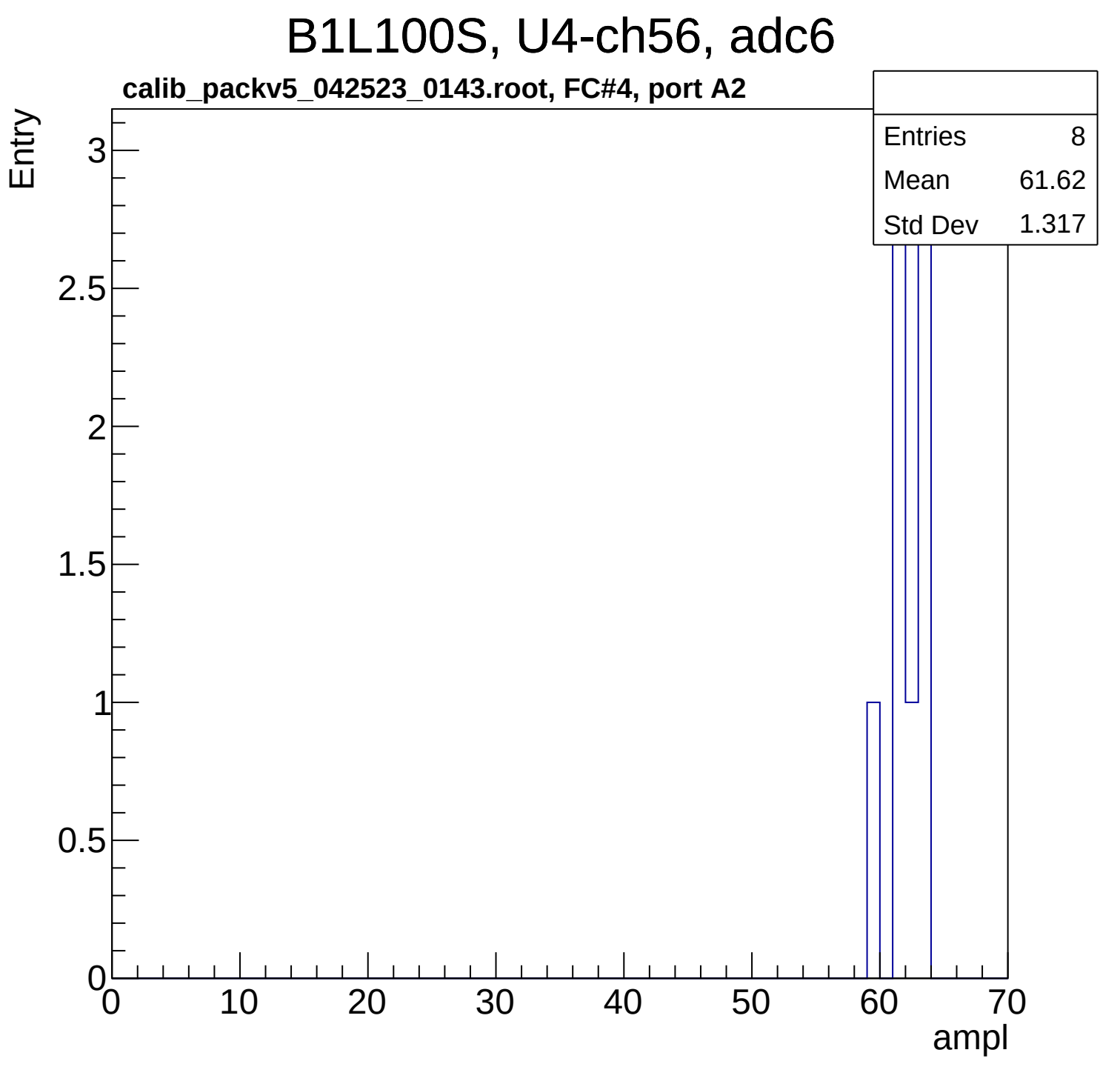

B1L100S, U4-ch56, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 84
Mean 35.43
Std Dev 5.789
Gaus mean : 37.2747
Gaus Width: 4.4303
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

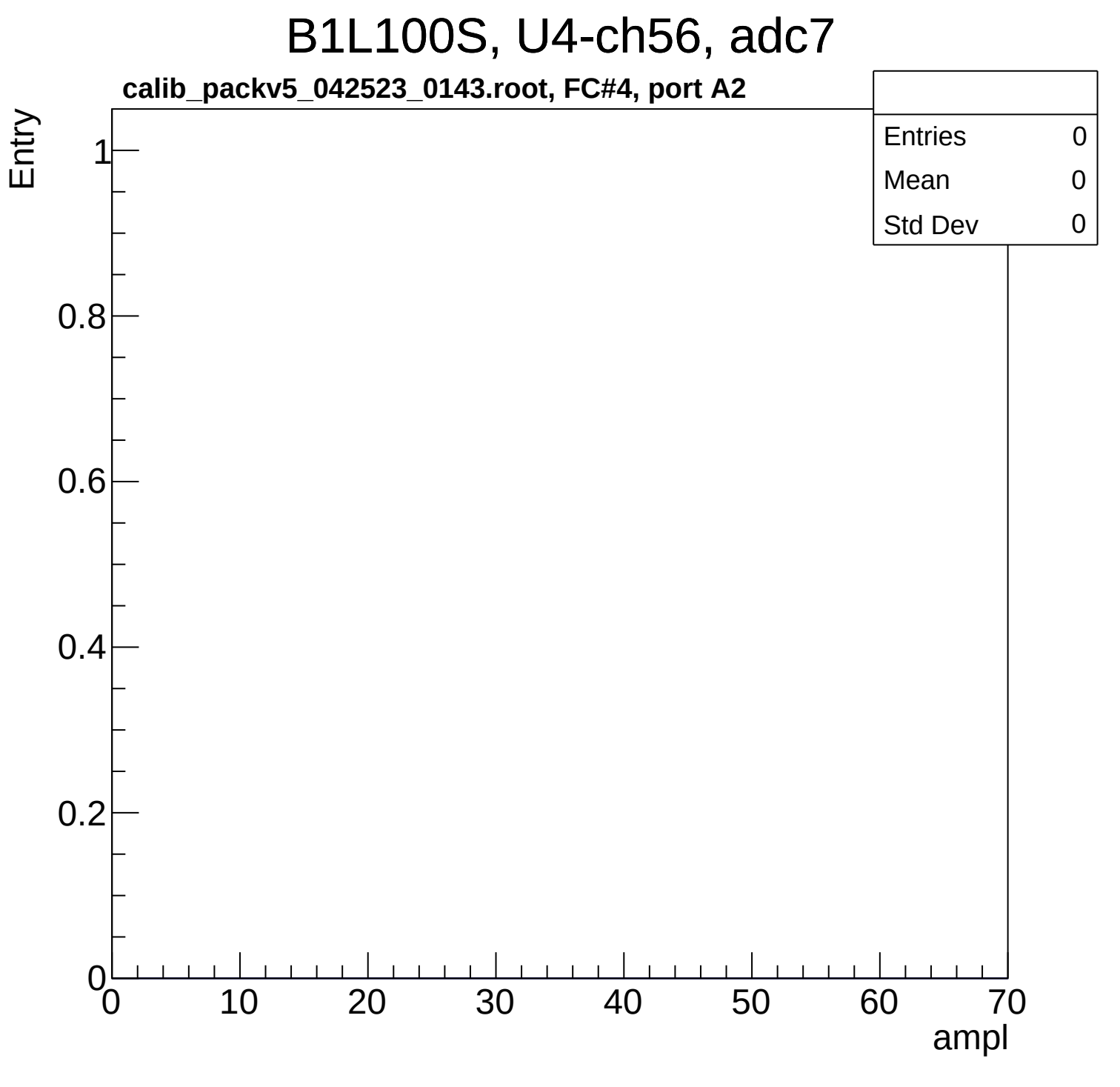

B1L100S, U4-ch56, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 42.46
Std Dev 3.257
Gaus mean : 43.0354
Gaus Width: 4.4397
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

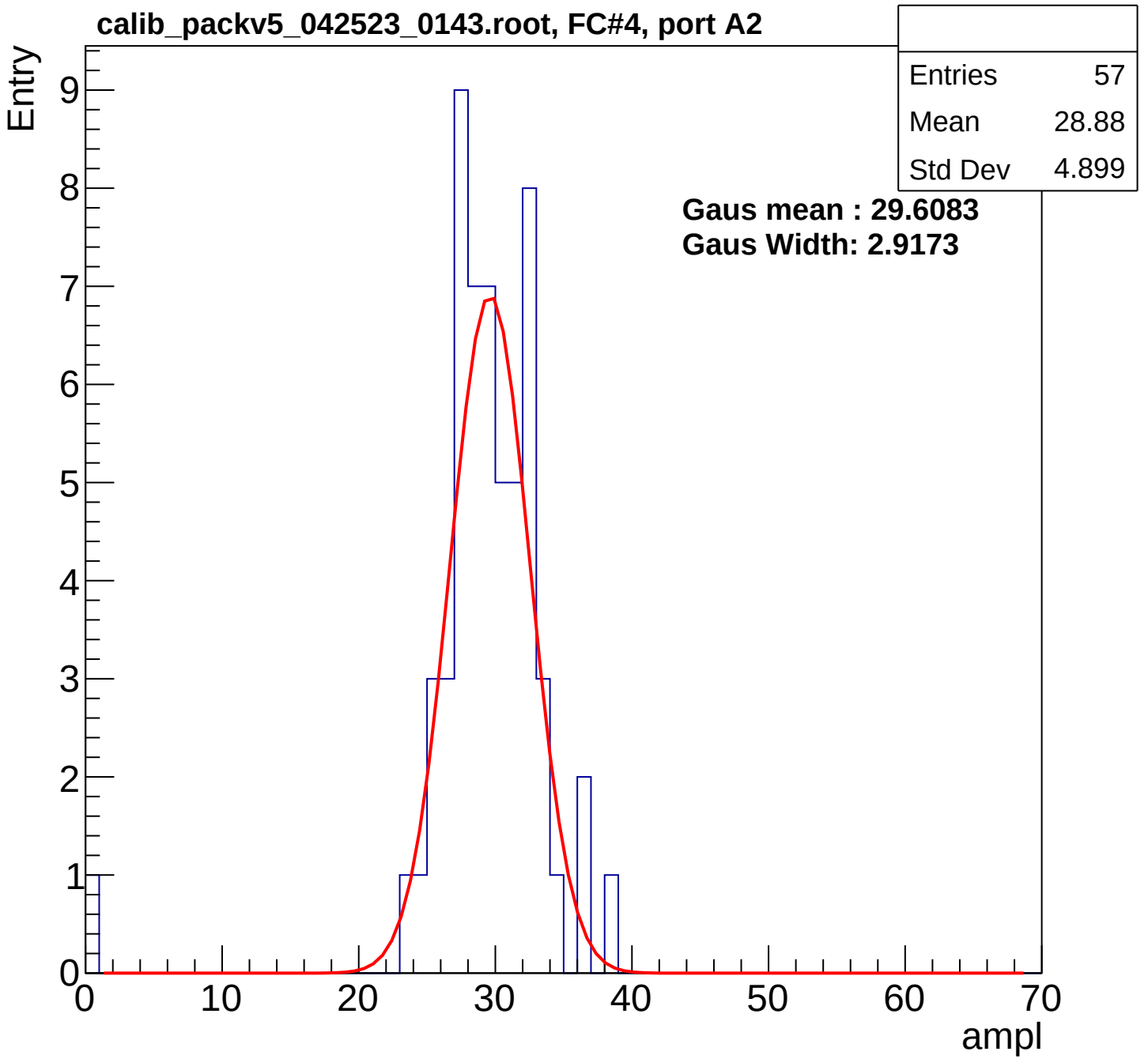

B1L100S, U4-ch56, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 48.71
Std Dev 3.404
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

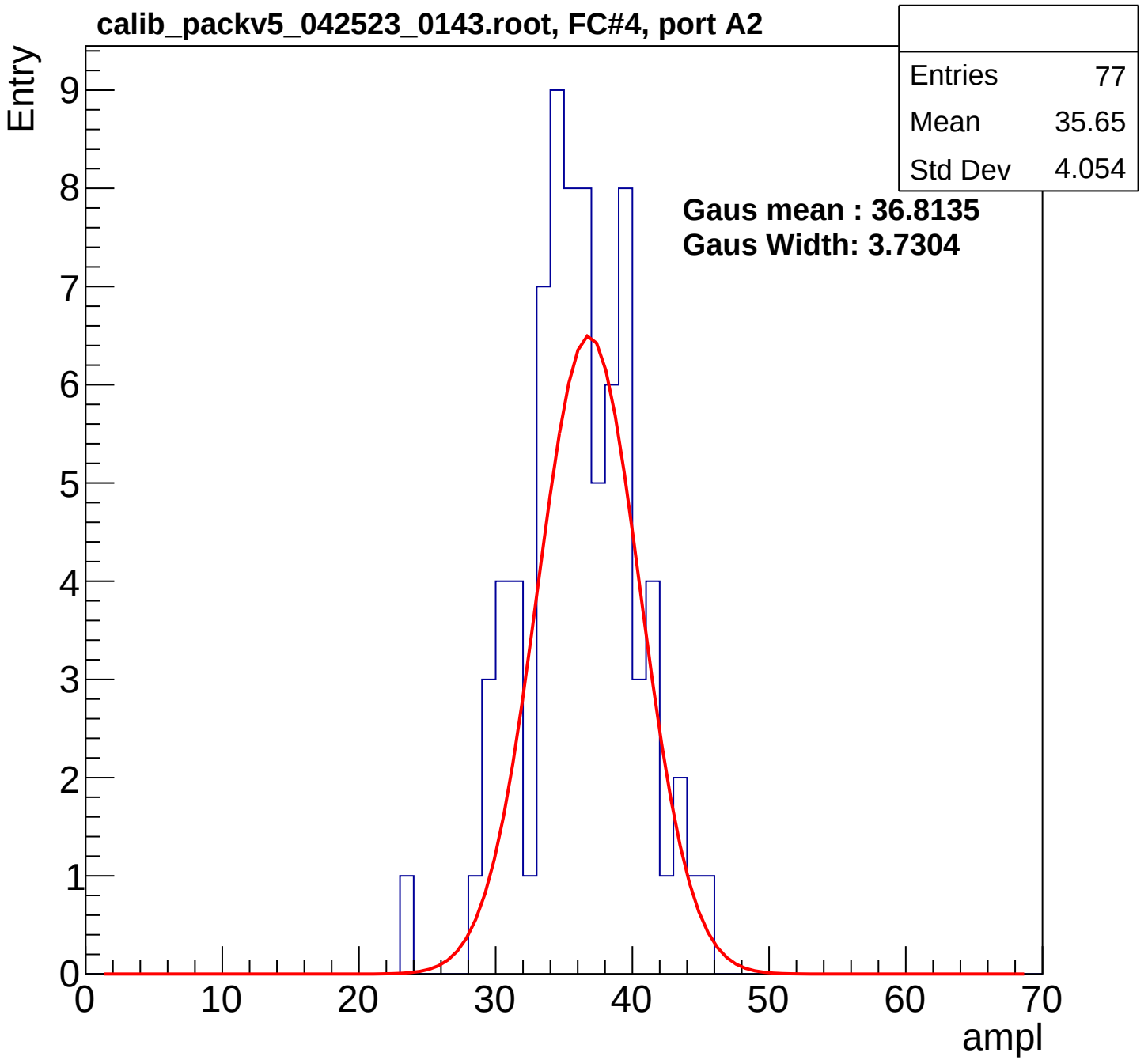

B1L100S, U4-ch56, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 54.28
Std Dev 3.044
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

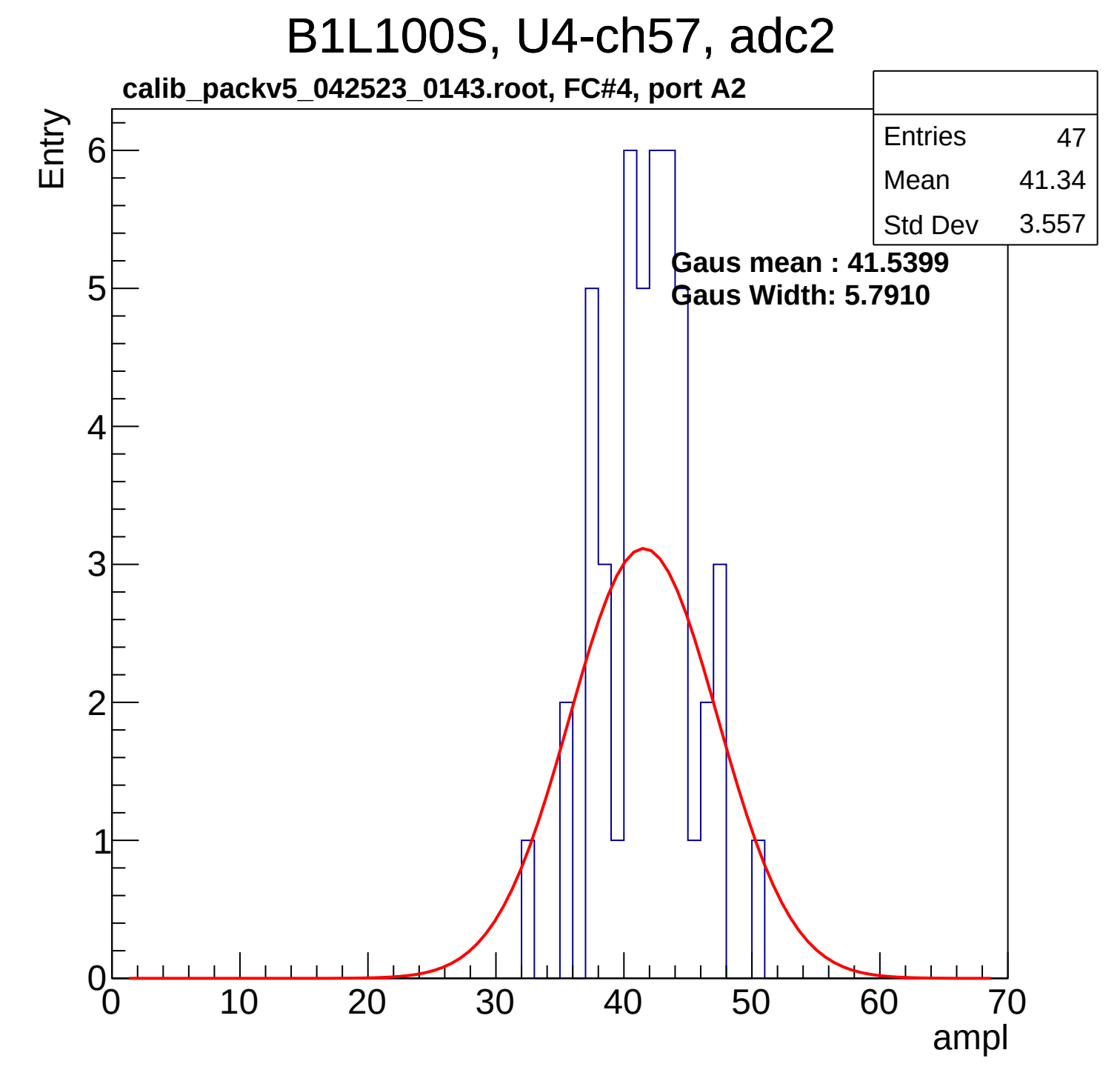

B1L100S, U4-ch56, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 58.52
Std Dev 8.632
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

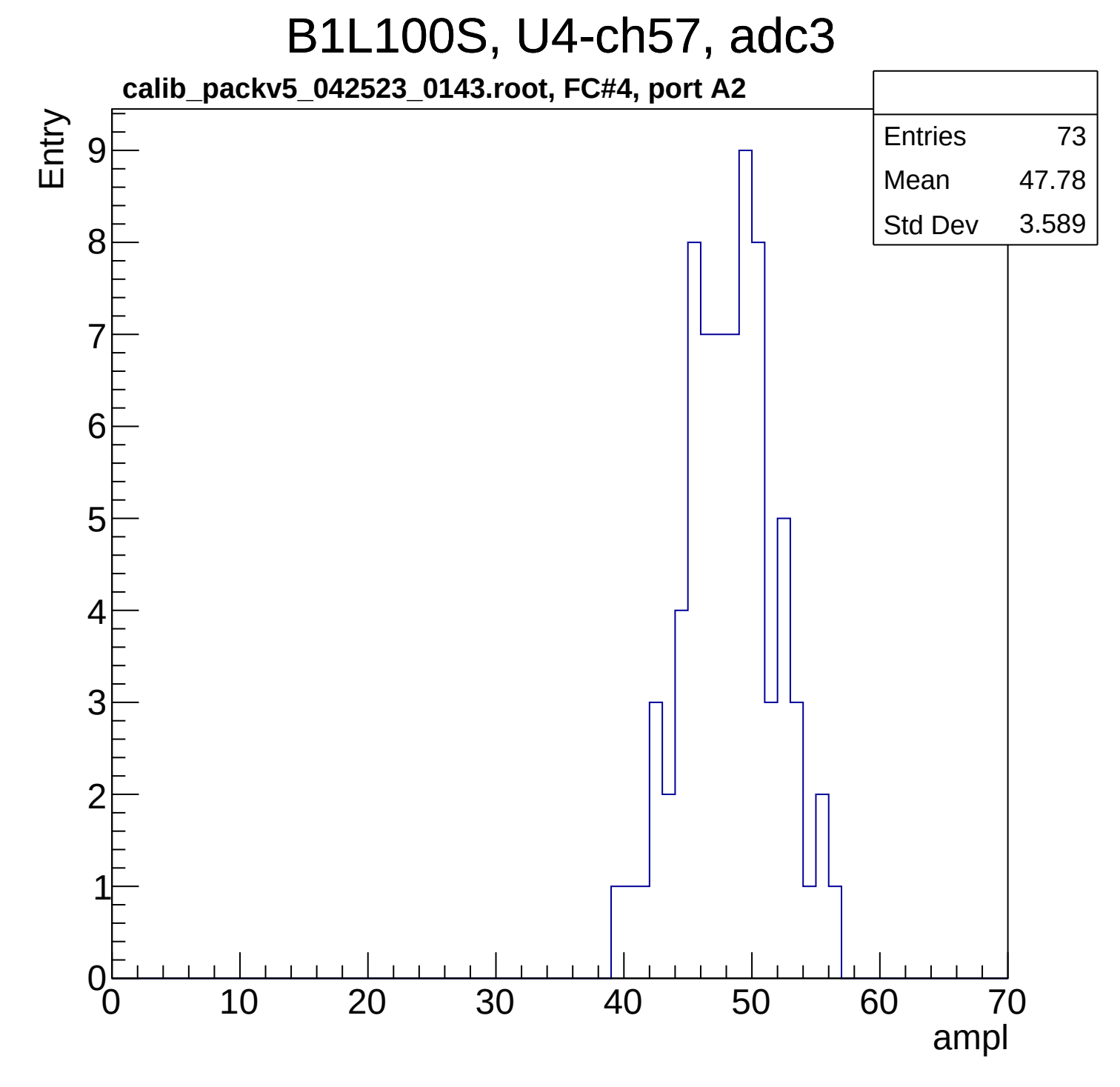

B1L100S, U4-ch56, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 8
Mean 61.62
Std Dev 1.317
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

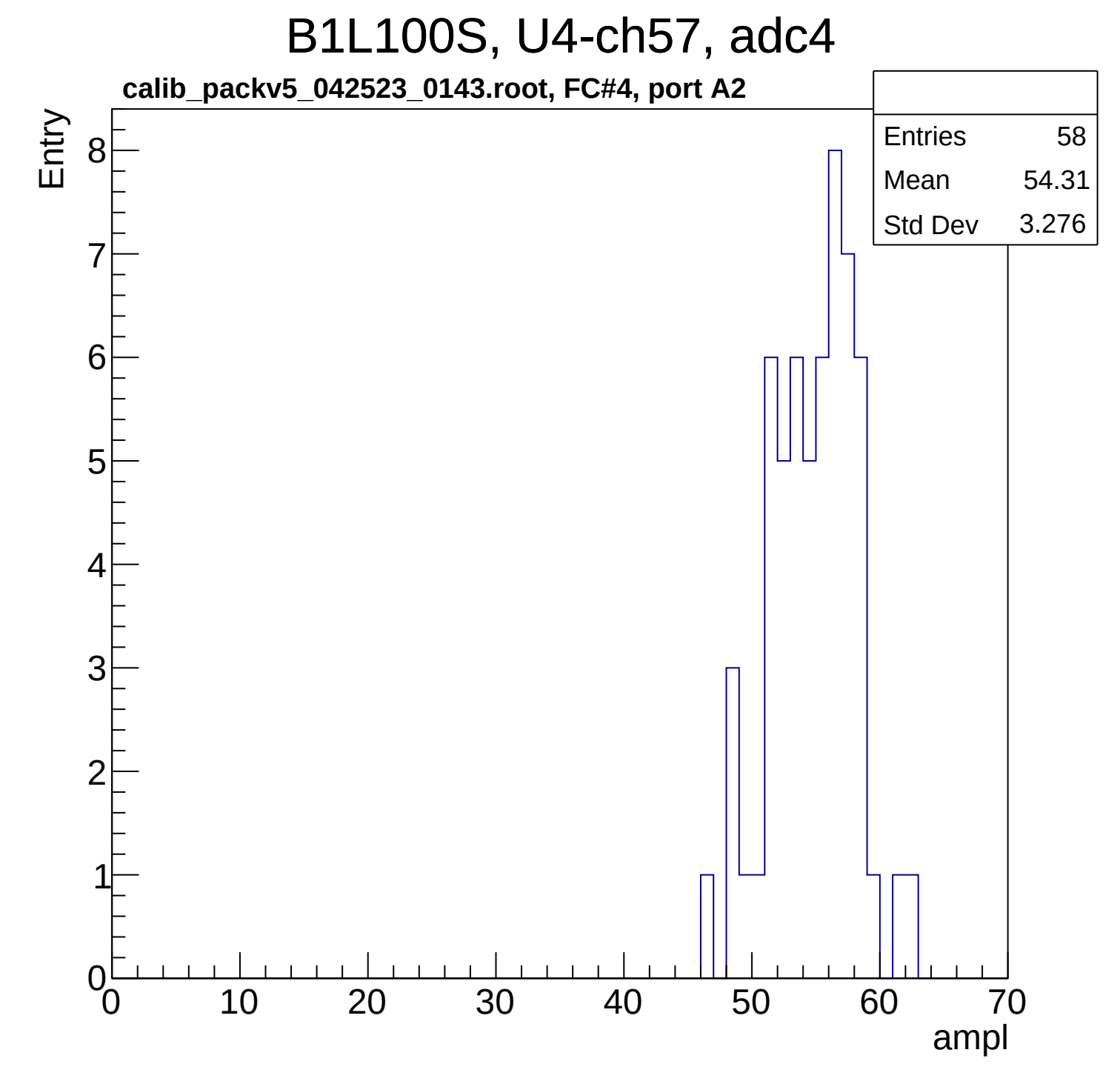

B1L100S, U4-ch56, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

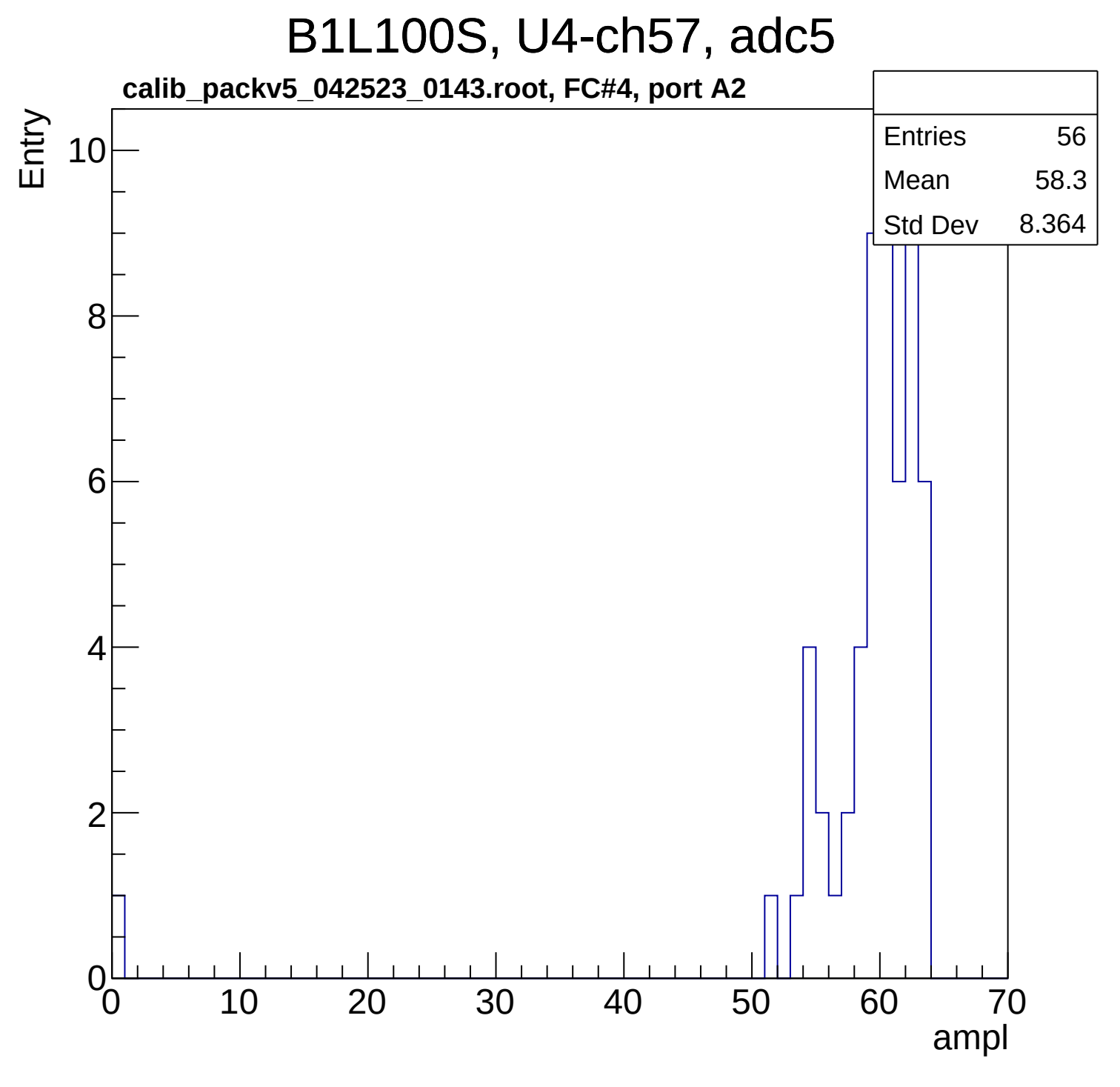

B1L100S, U4-ch57, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 28.88
Std Dev 4.899
Gaus mean : 29.6083
Gaus Width: 2.9173
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

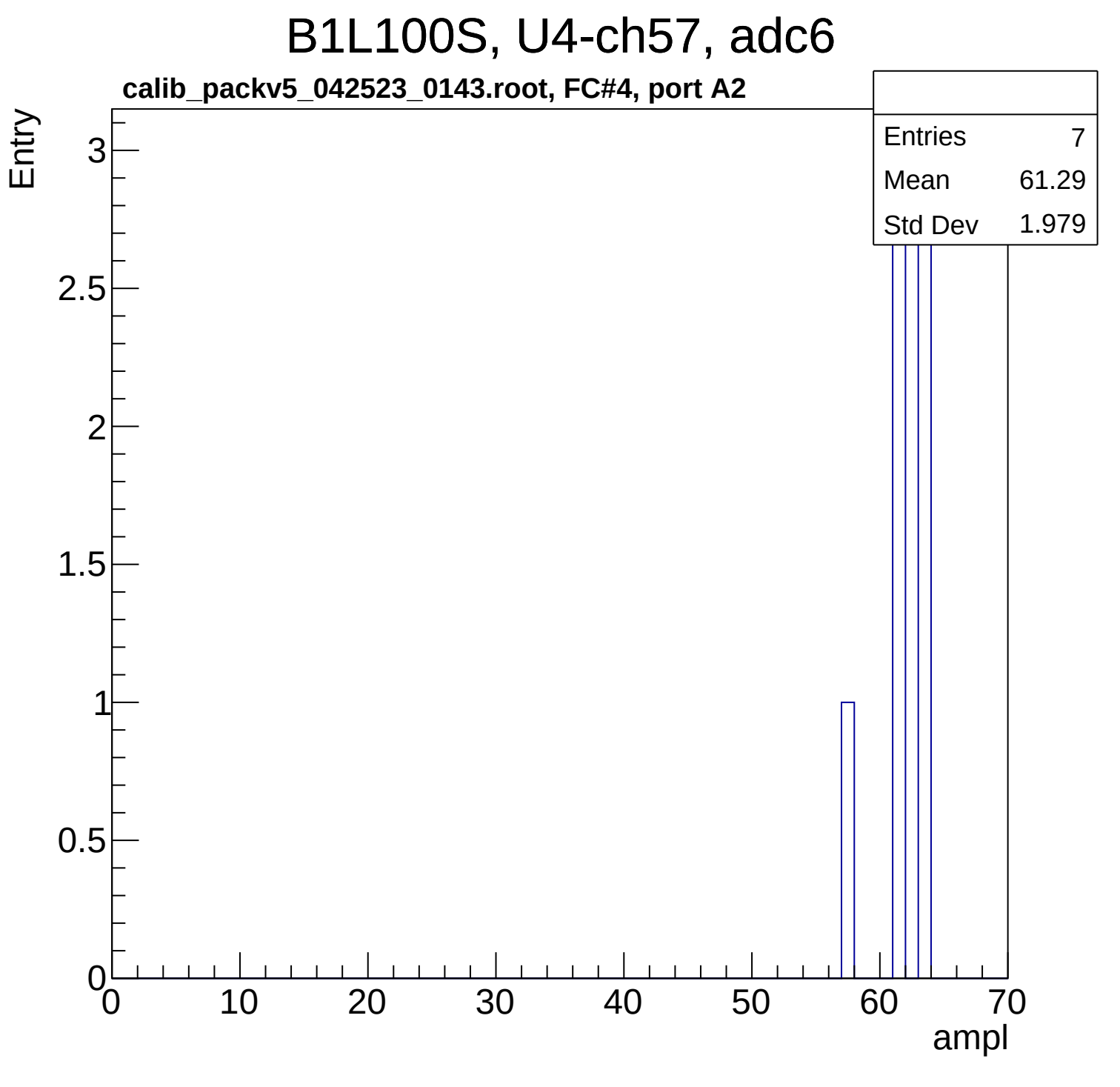

B1L100S, U4-ch57, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 35.65
Std Dev 4.054
Gaus mean : 36.8135
Gaus Width: 3.7304
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

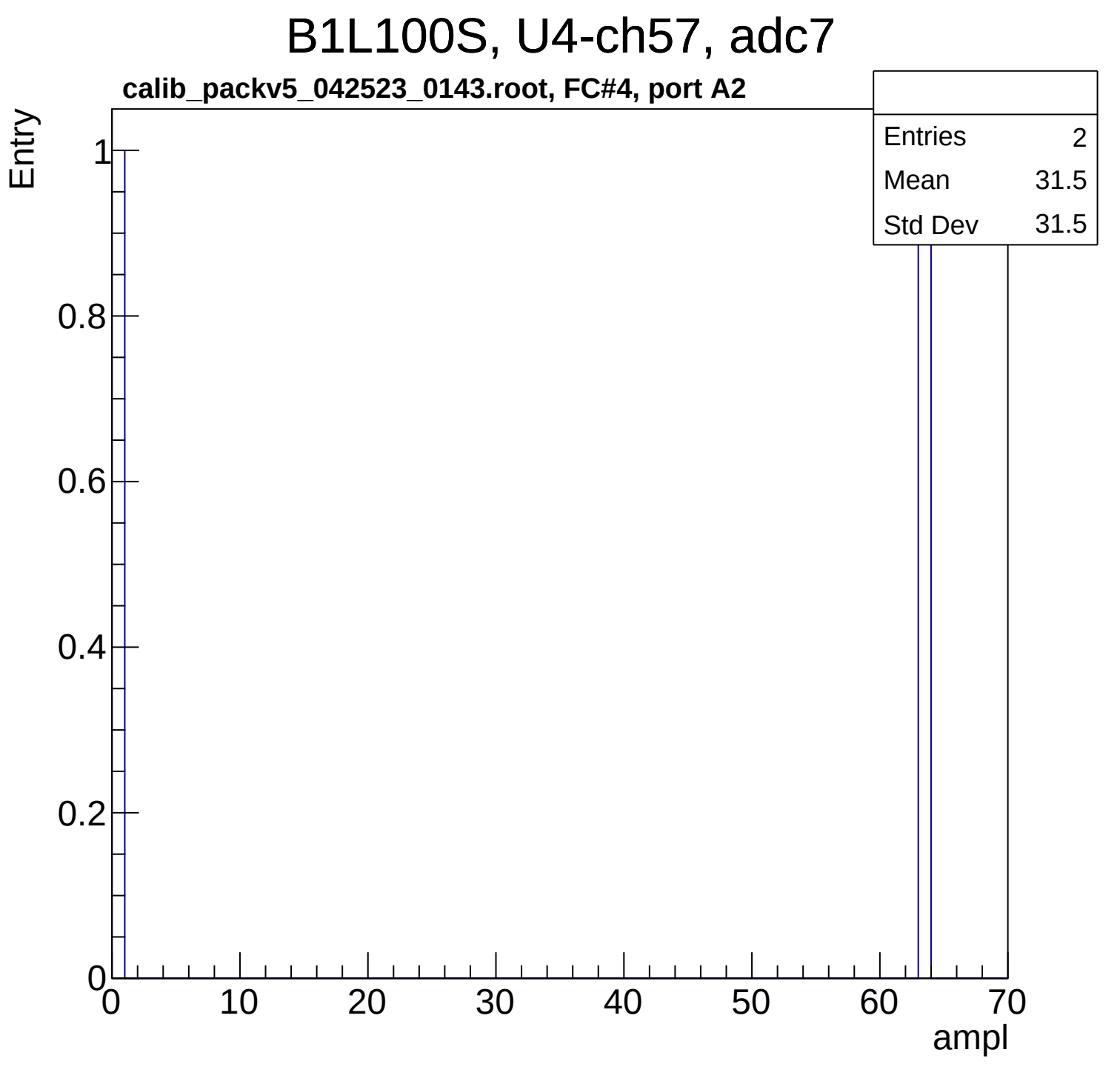

B1L100S, U4-ch57, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 41.34
Std Dev 3.557
Gaus mean : 41.5399
Gaus Width: 5.7910
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

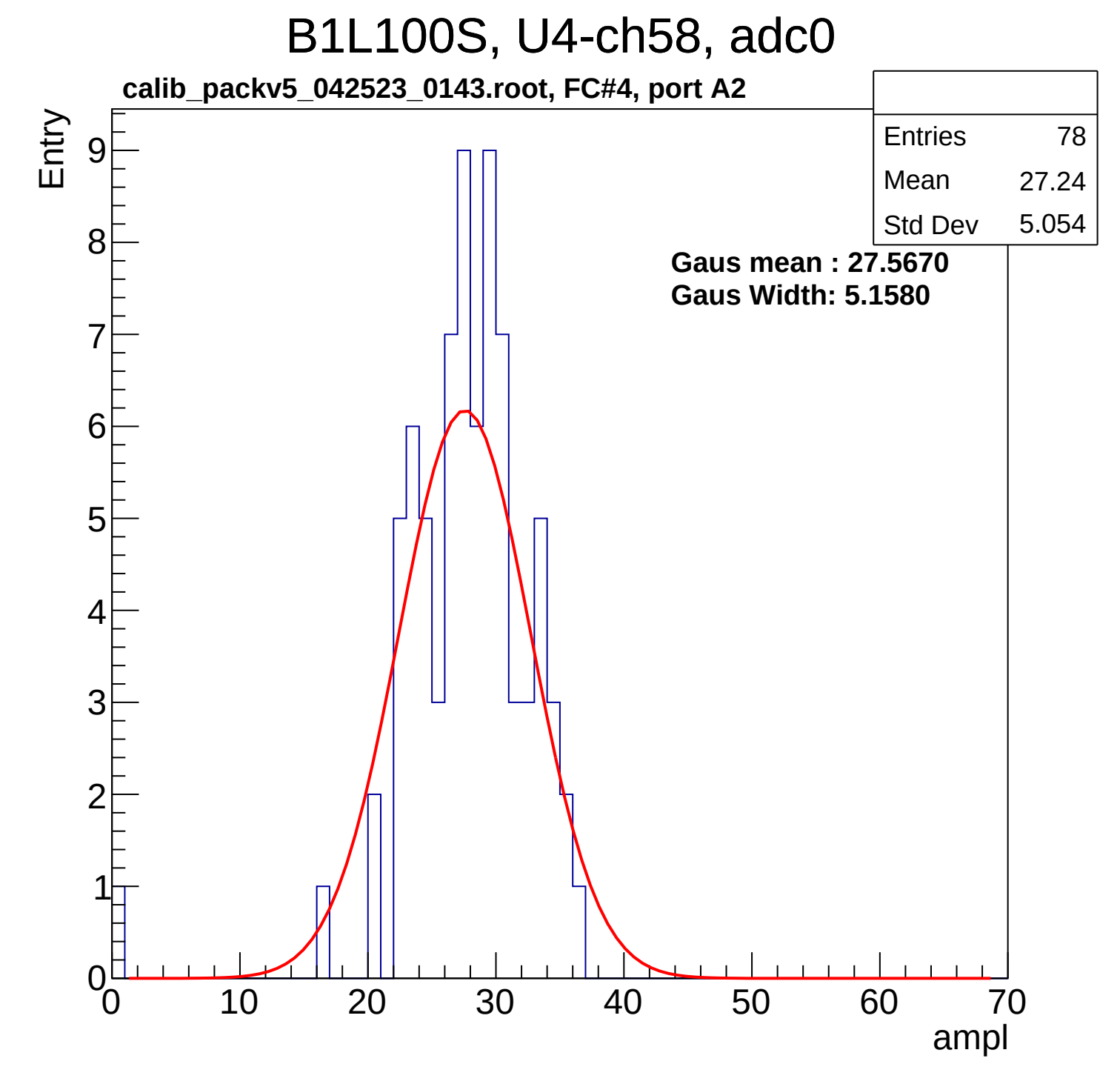

B1L100S, U4-ch57, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 47.78
Std Dev 3.589
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

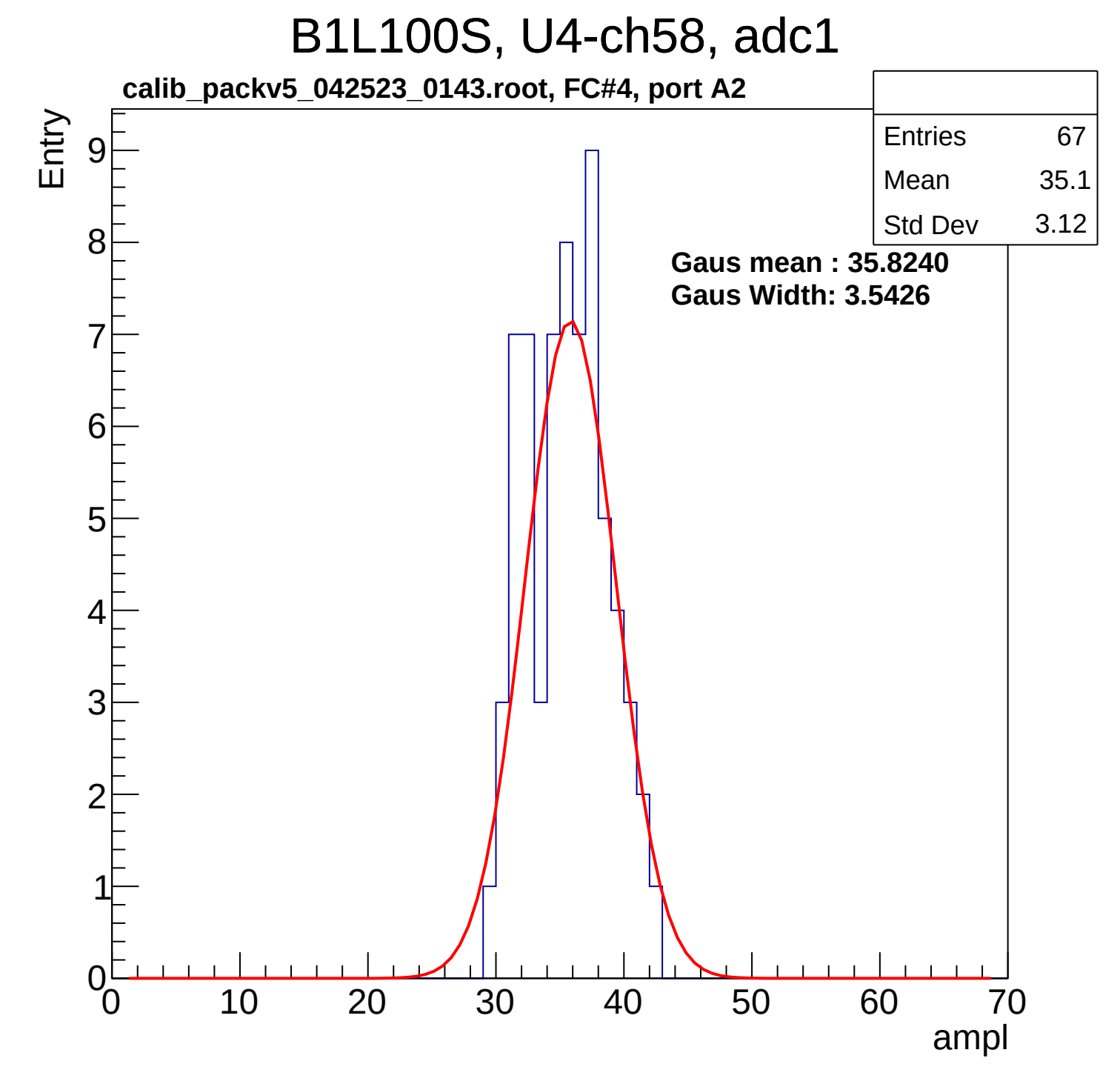

B1L100S, U4-ch57, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 54.31
Std Dev 3.276
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

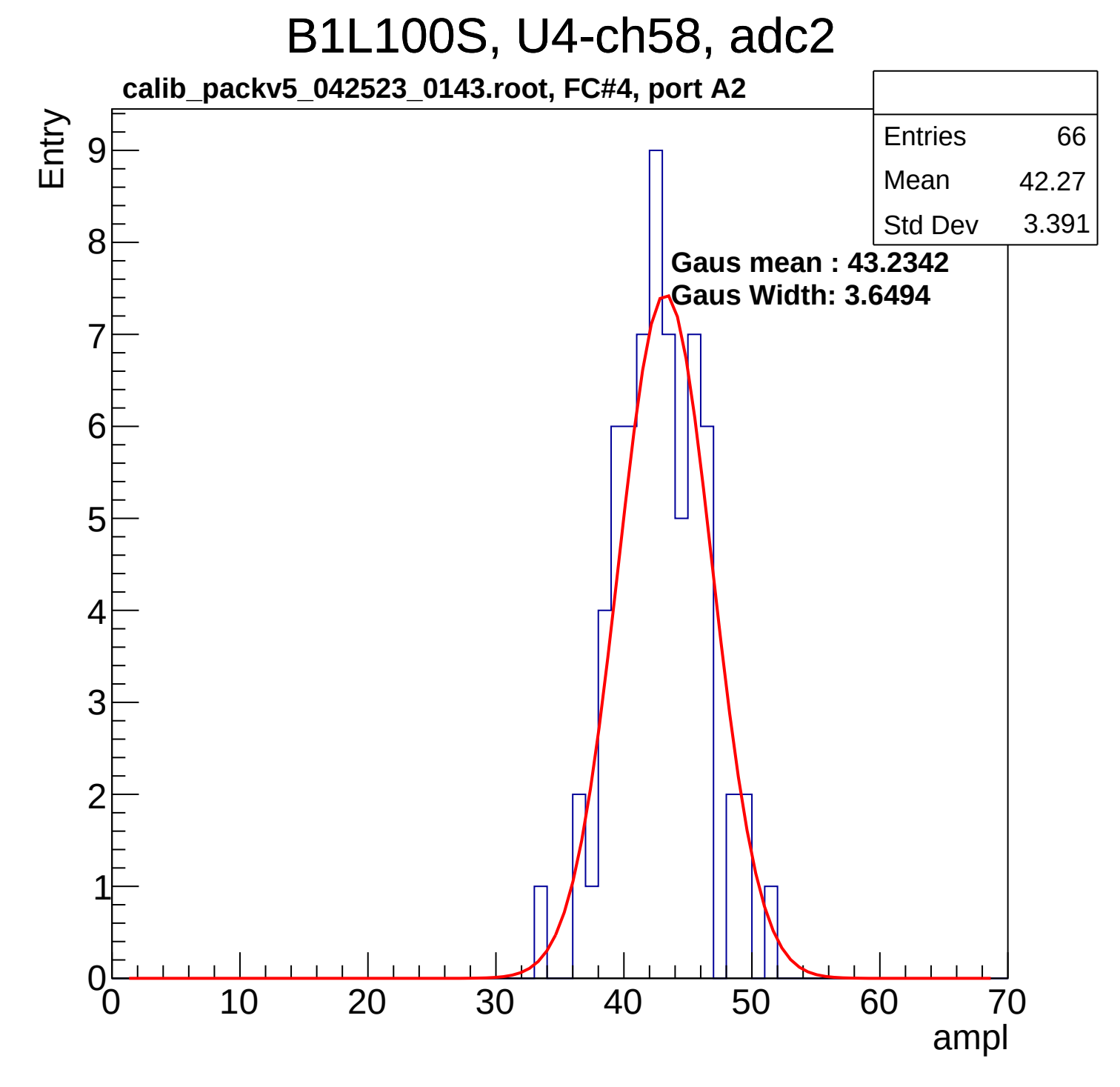

B1L100S, U4-ch57, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 58.3
Std Dev 8.364
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

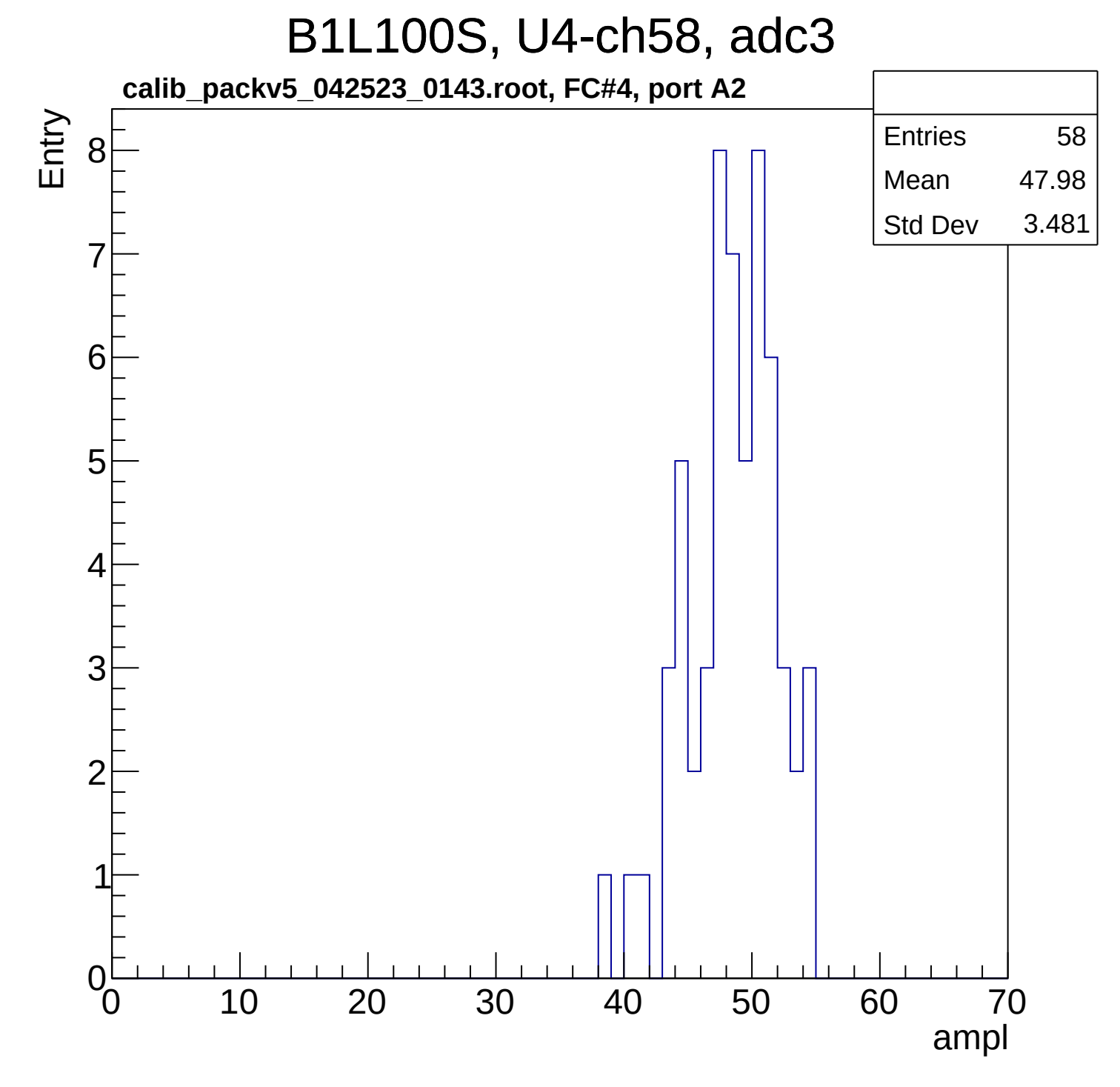

B1L100S, U4-ch57, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 61.29
Std Dev 1.979
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

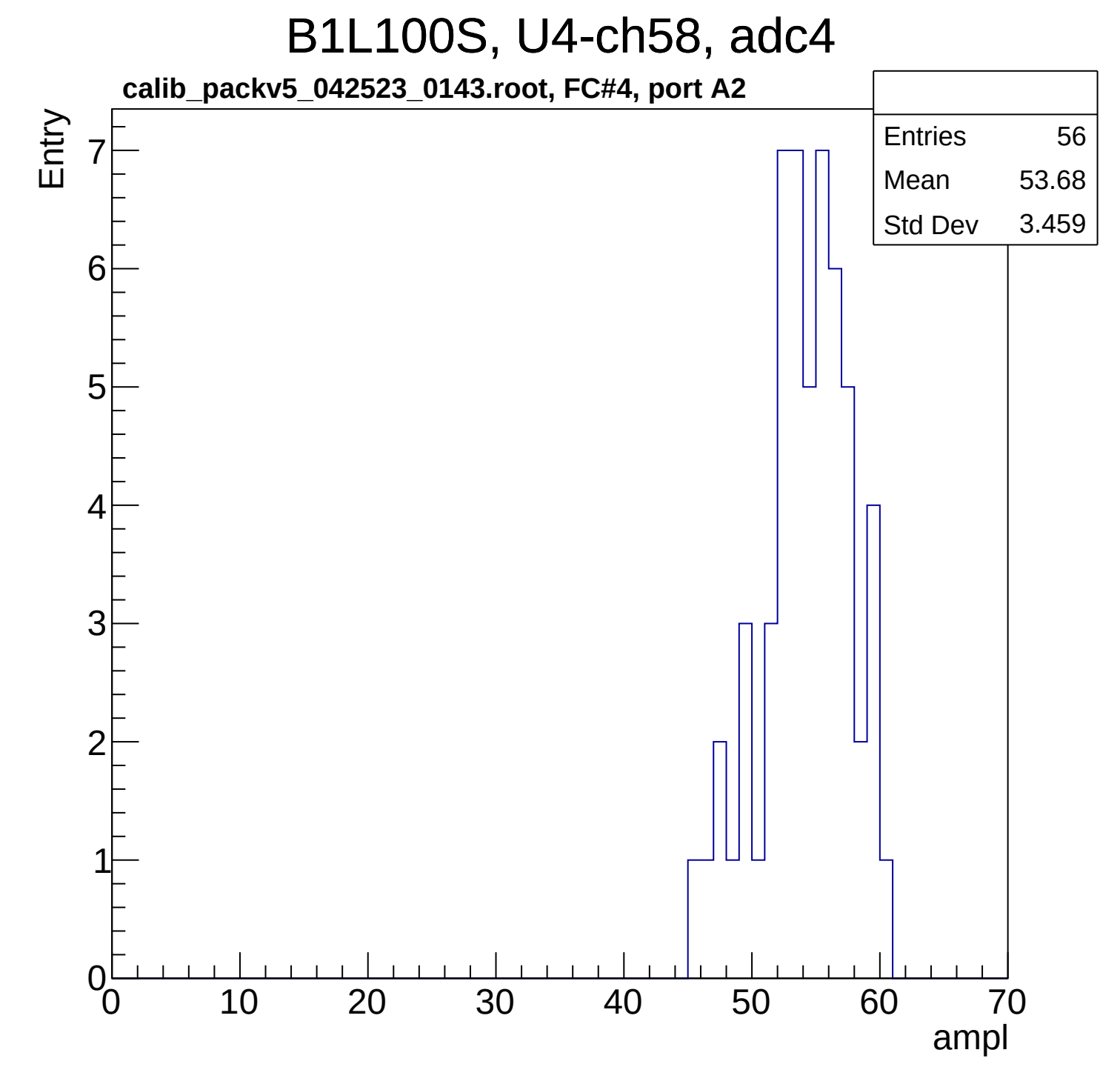

B1L100S, U4-ch57, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

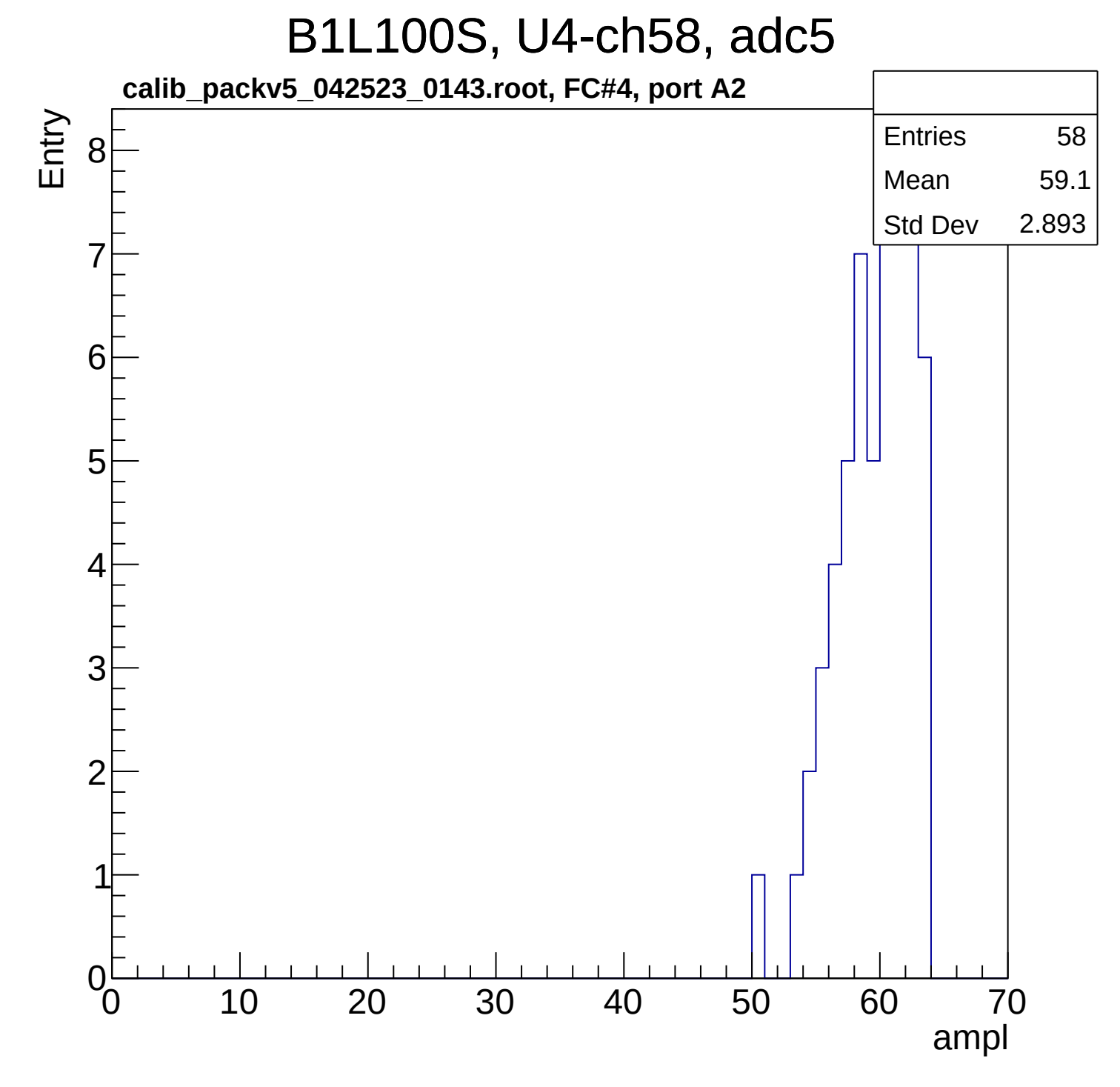

B1L100S, U4-ch58, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 27.24
Std Dev 5.054
Gaus mean : 27.5670
Gaus Width: 5.1580
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

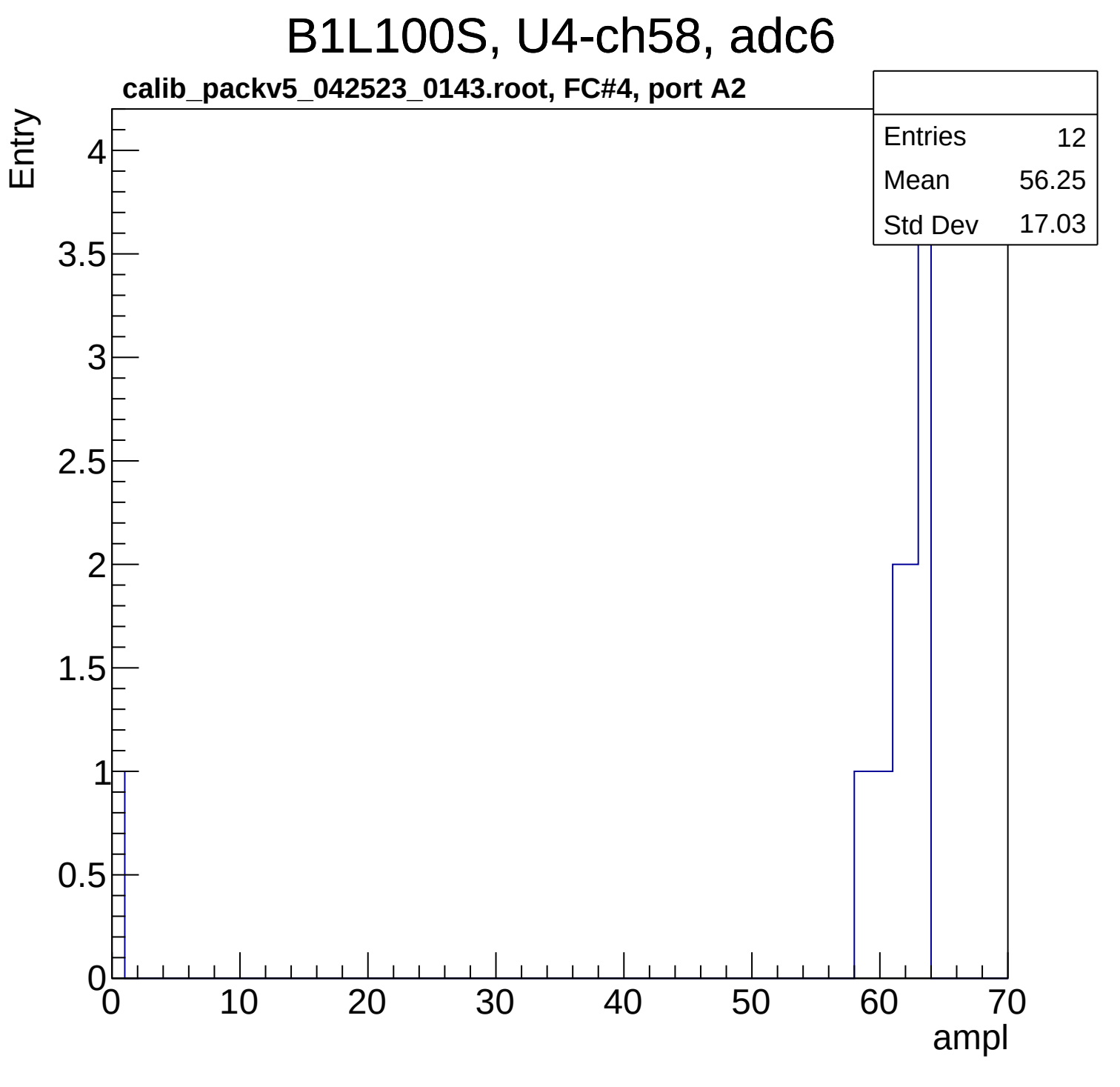

B1L100S, U4-ch58, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 35.1
Std Dev 3.12
Gaus mean : 35.8240
Gaus Width: 3.5426
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

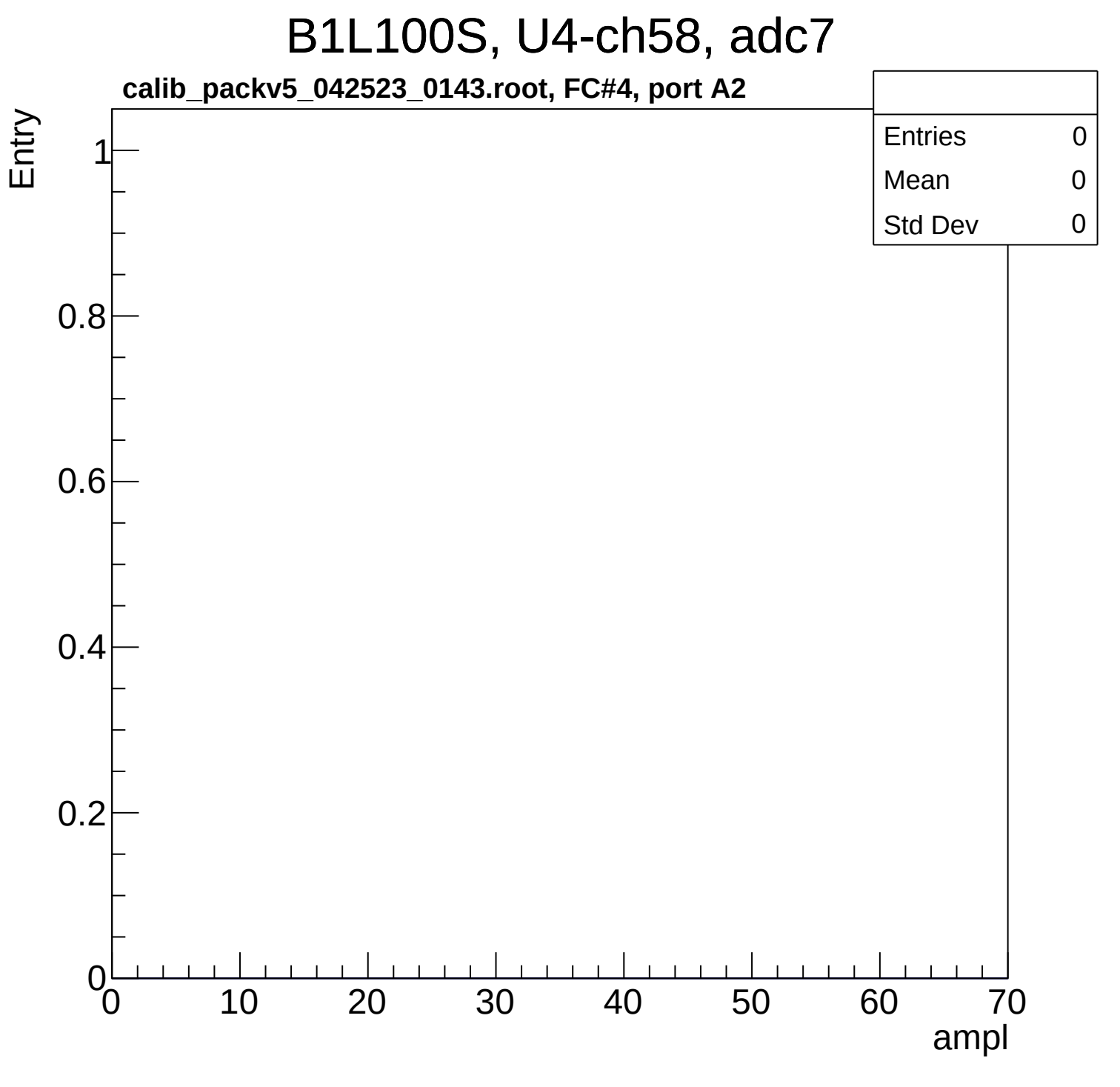

B1L100S, U4-ch58, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 42.27
Std Dev 3.391
Gaus mean : 43.2342
Gaus Width: 3.6494
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

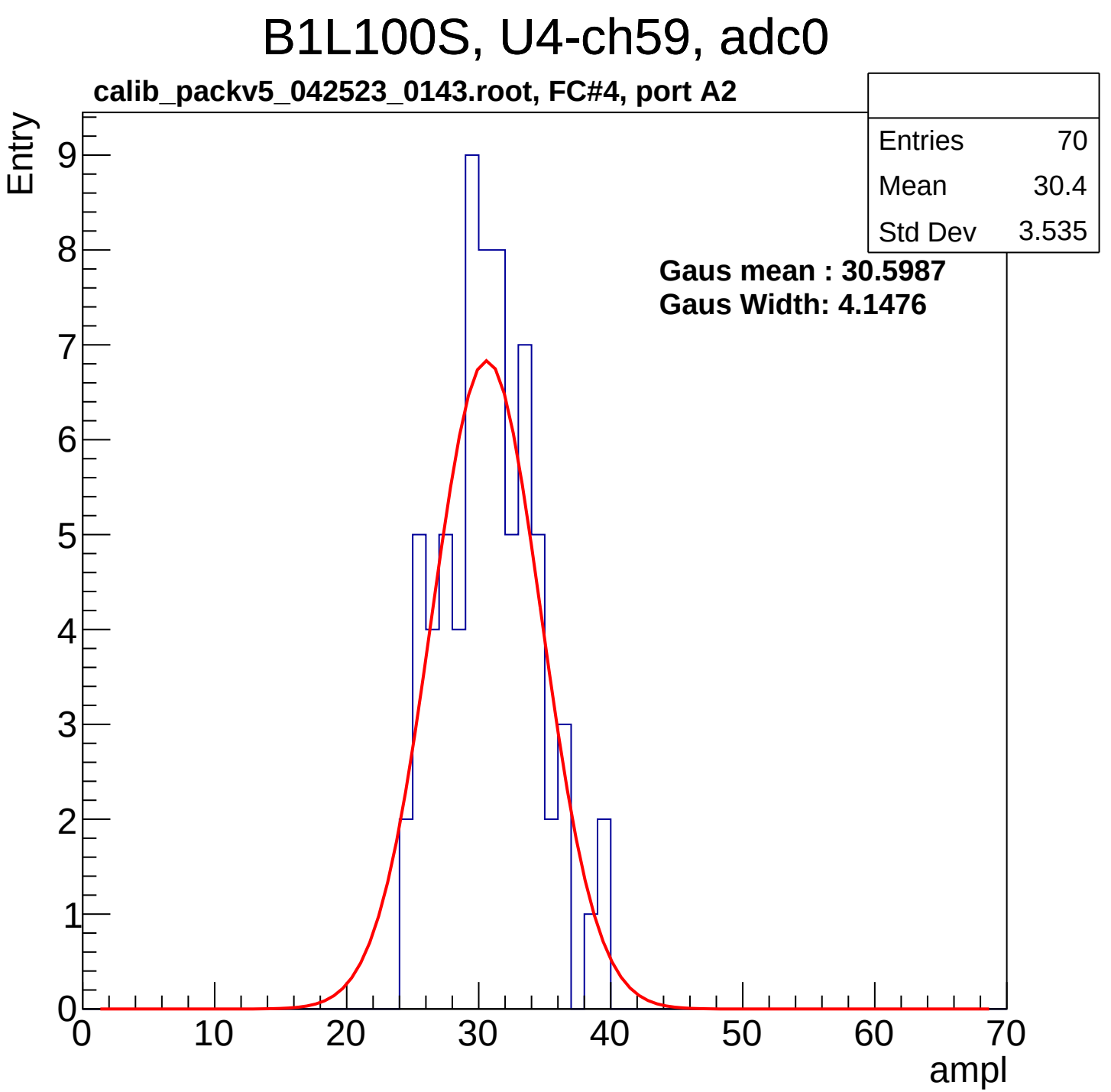

B1L100S, U4-ch58, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 47.98
Std Dev 3.481
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

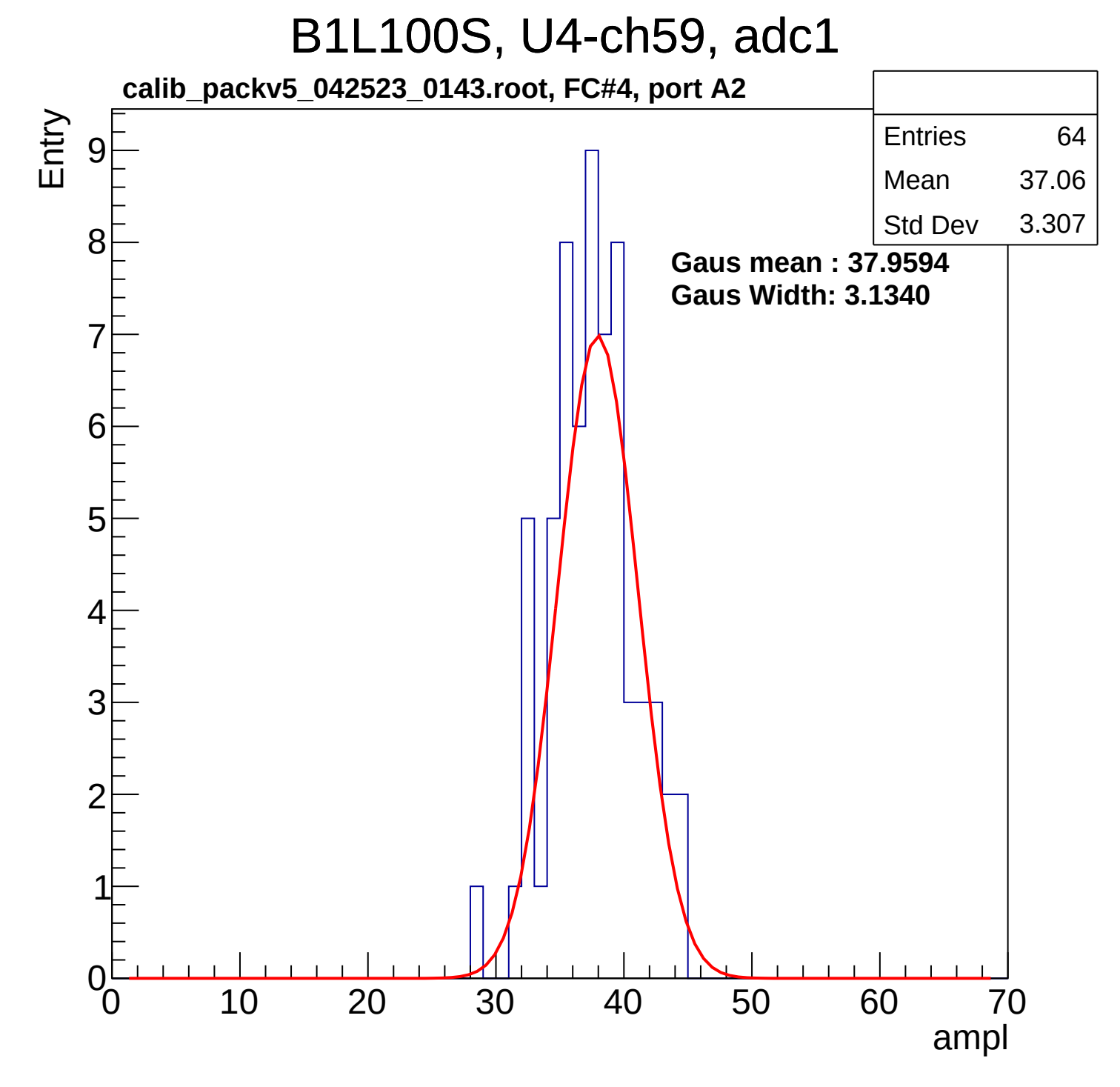

B1L100S, U4-ch58, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 53.68
Std Dev 3.459
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

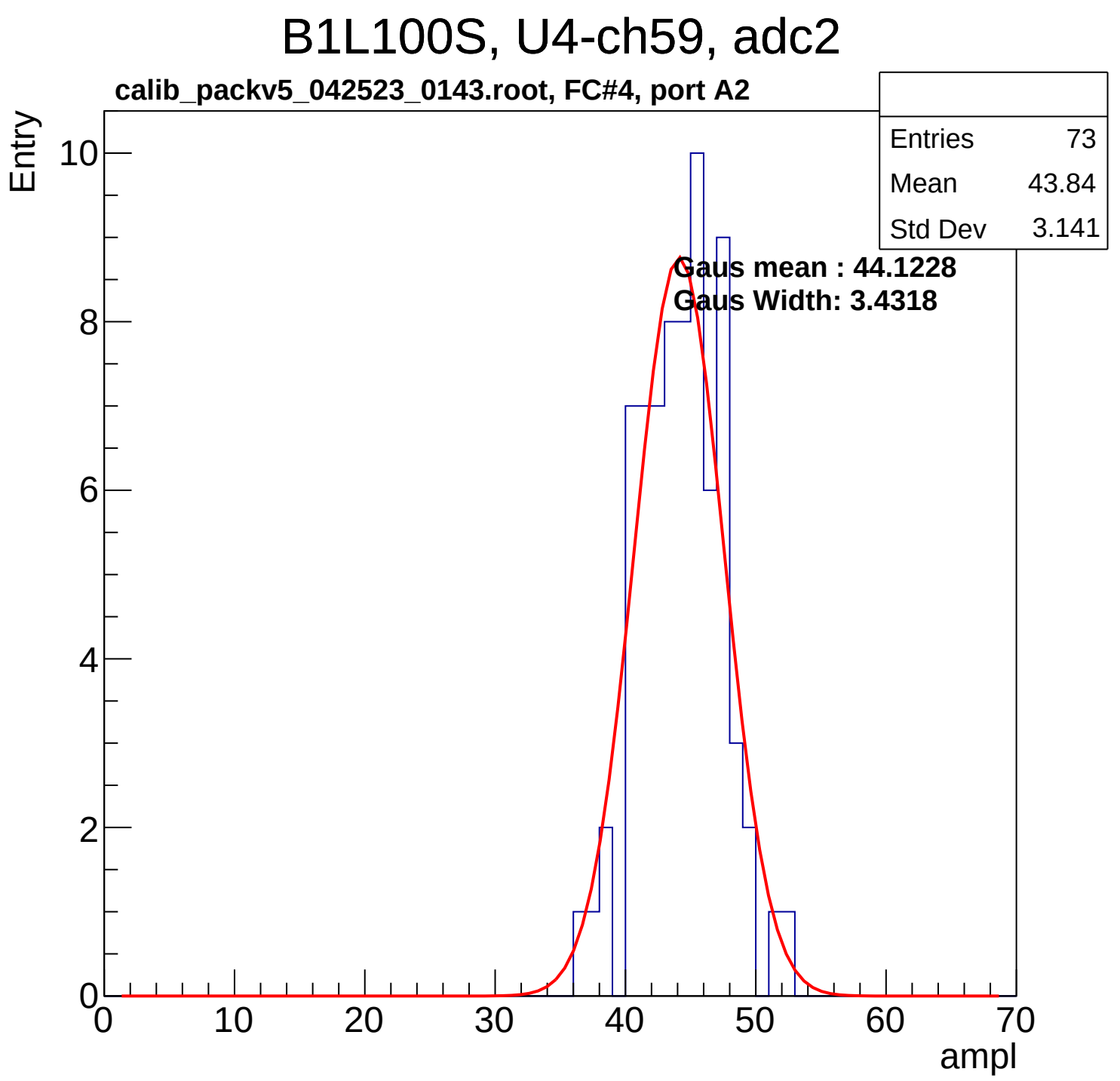

B1L100S, U4-ch58, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 59.1
Std Dev 2.893
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

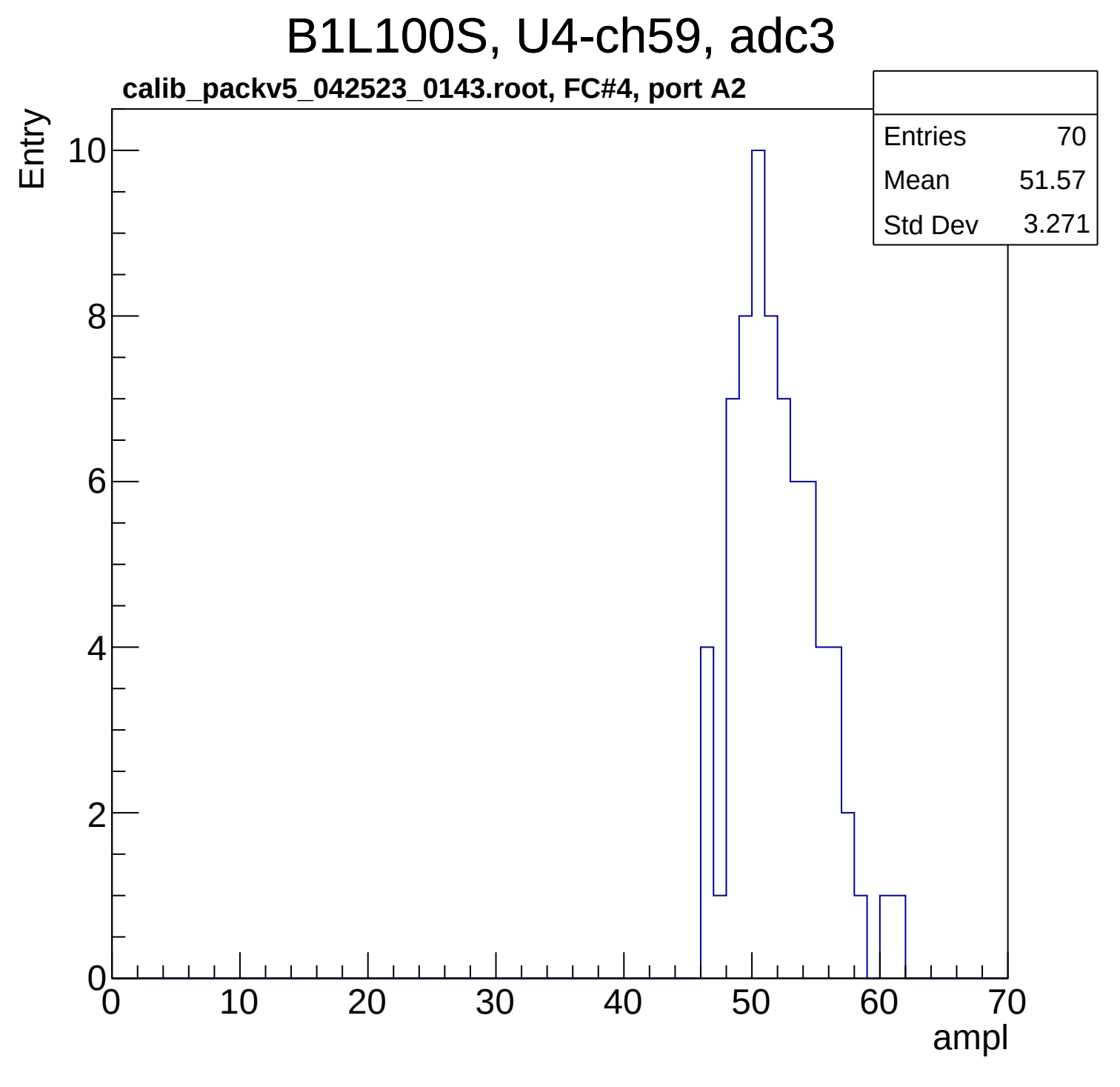

B1L100S, U4-ch58, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 12
Mean 56.25
Std Dev 17.03
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

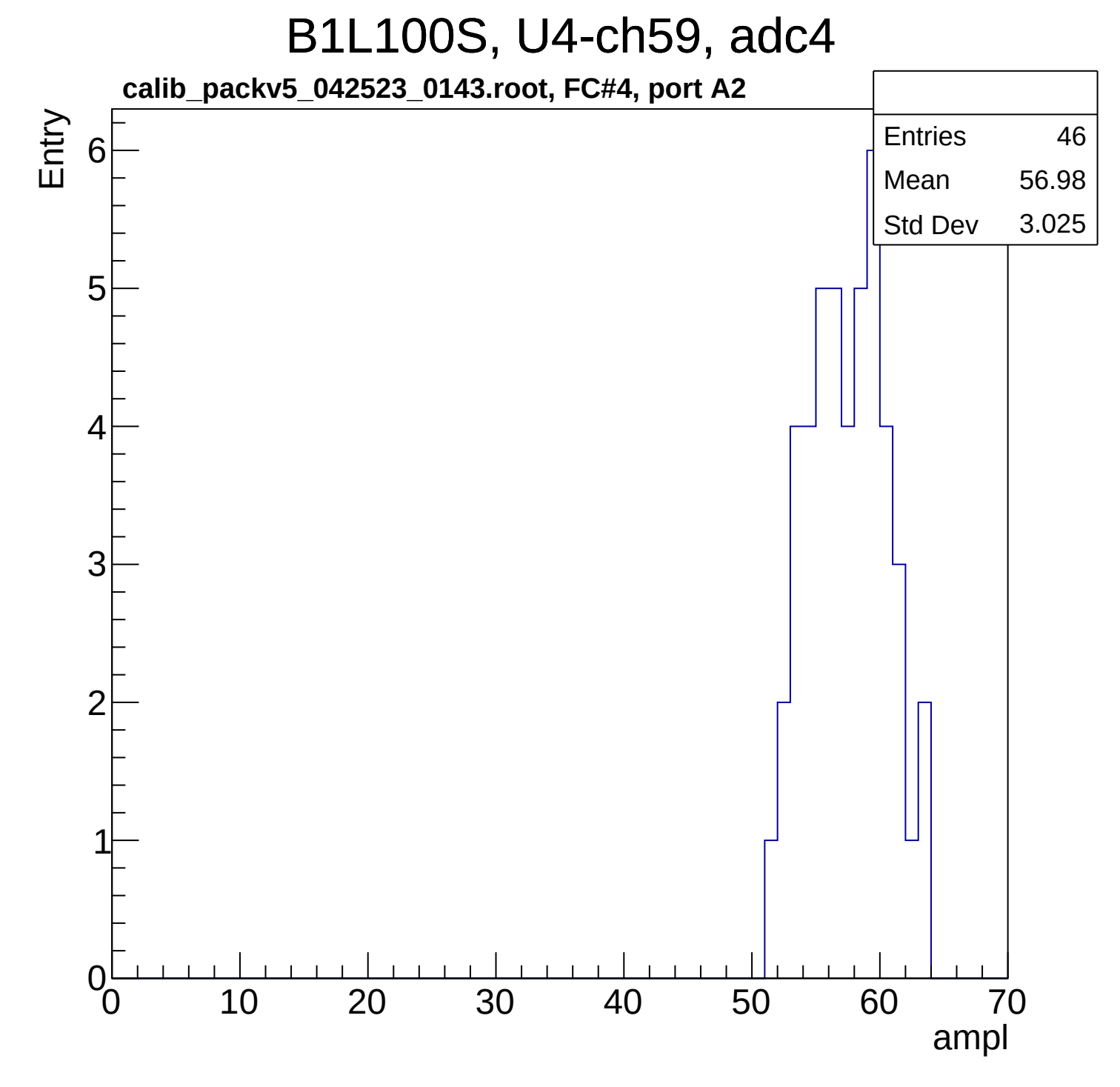

B1L100S, U4-ch58, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

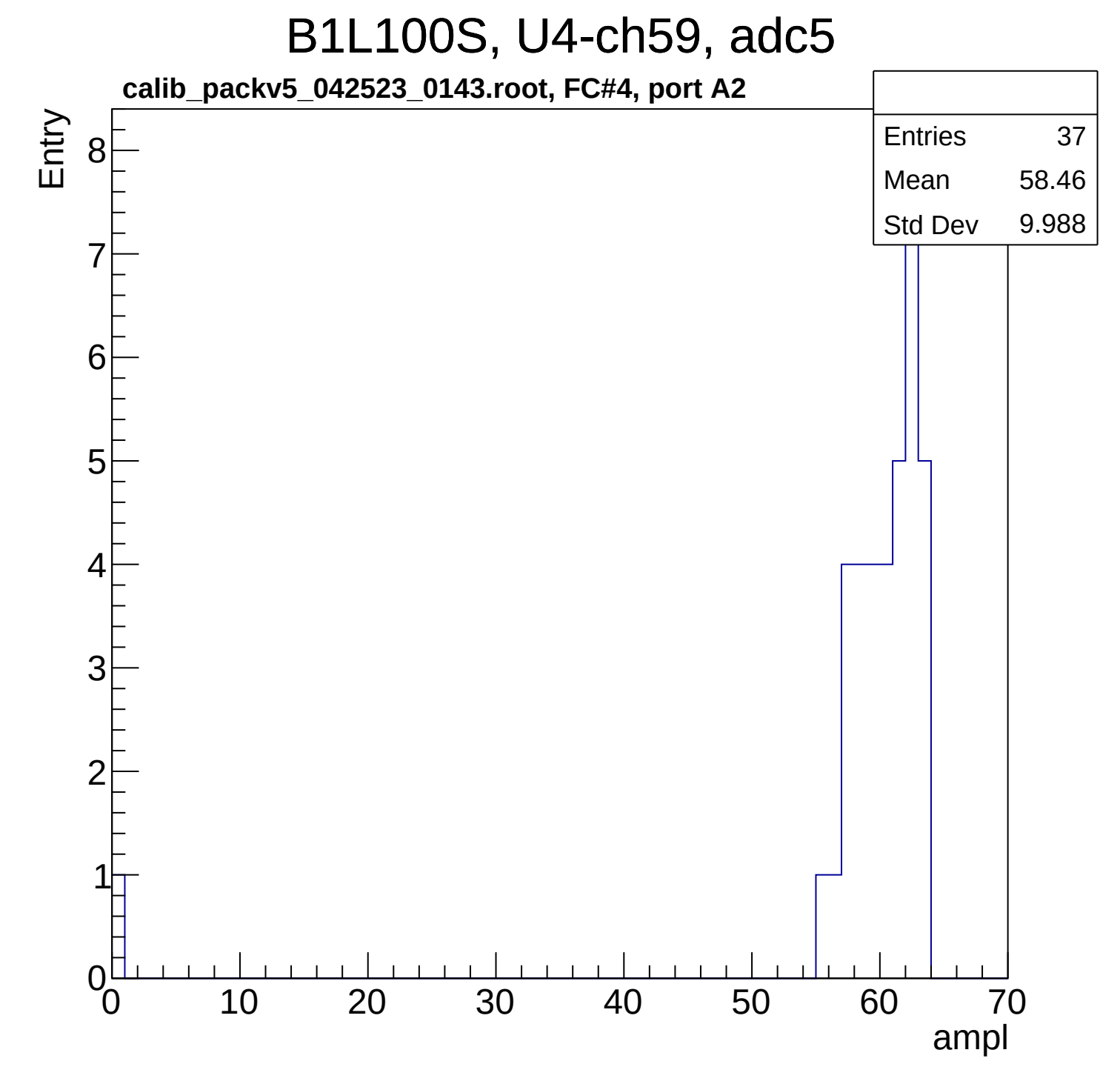

B1L100S, U4-ch59, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 30.4
Std Dev 3.535
Gaus mean : 30.5987
Gaus Width: 4.1476
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

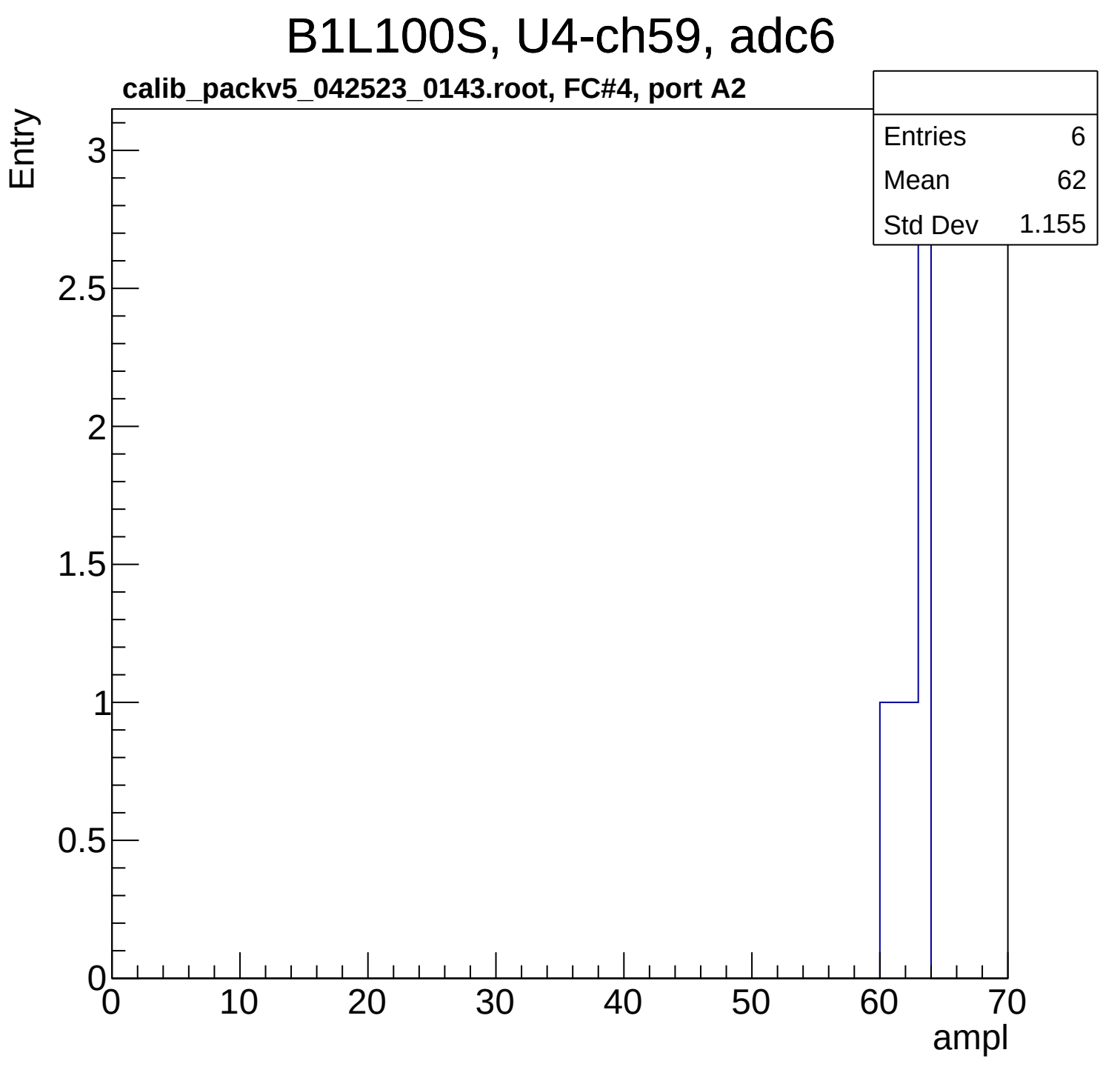

B1L100S, U4-ch59, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 37.06
Std Dev 3.307
Gaus mean : 37.9594
Gaus Width: 3.1340
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

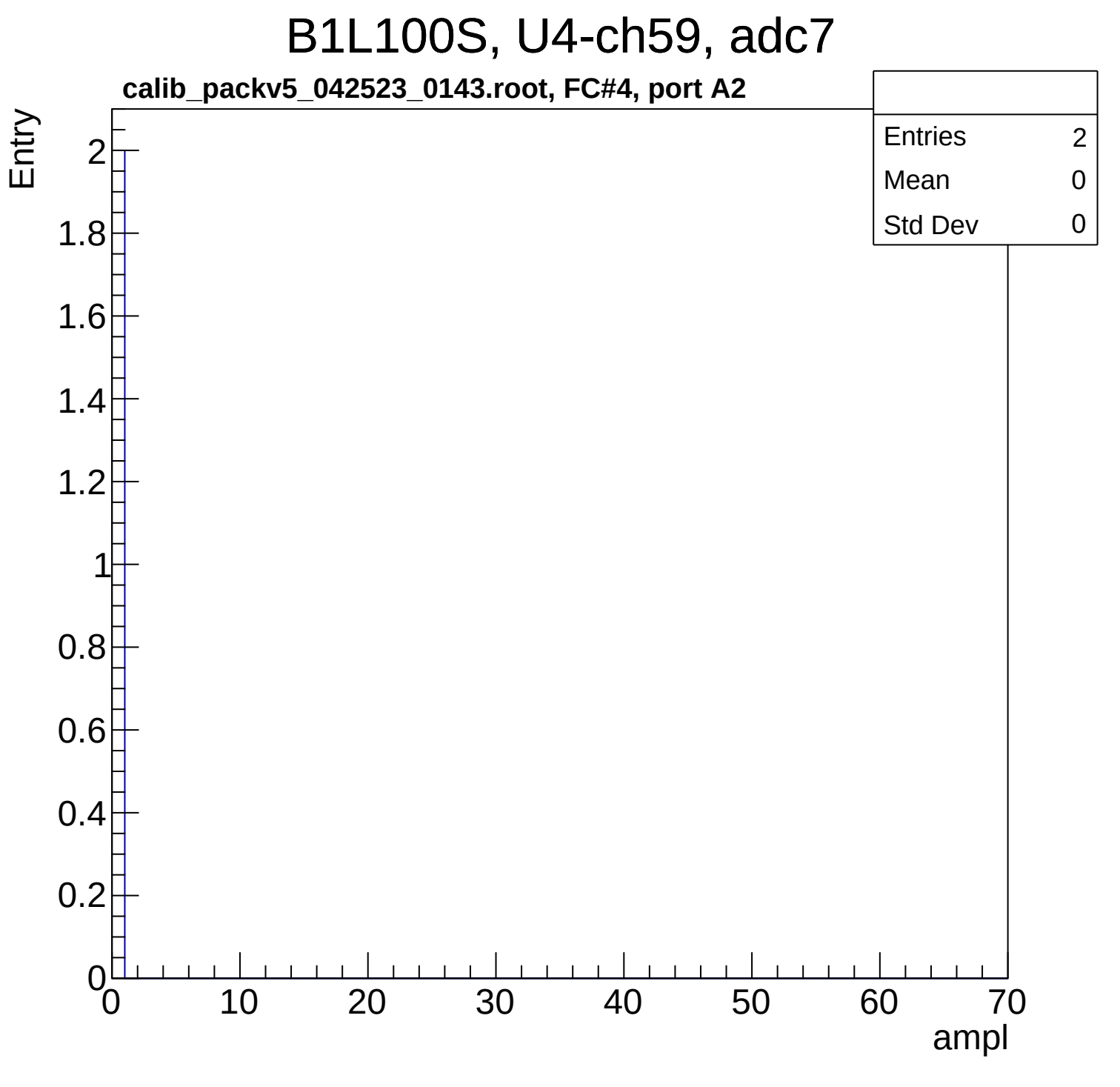

B1L100S, U4-ch59, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 43.84
Std Dev 3.141
Gaus mean : 44.1228
Gaus Width: 3.4318
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

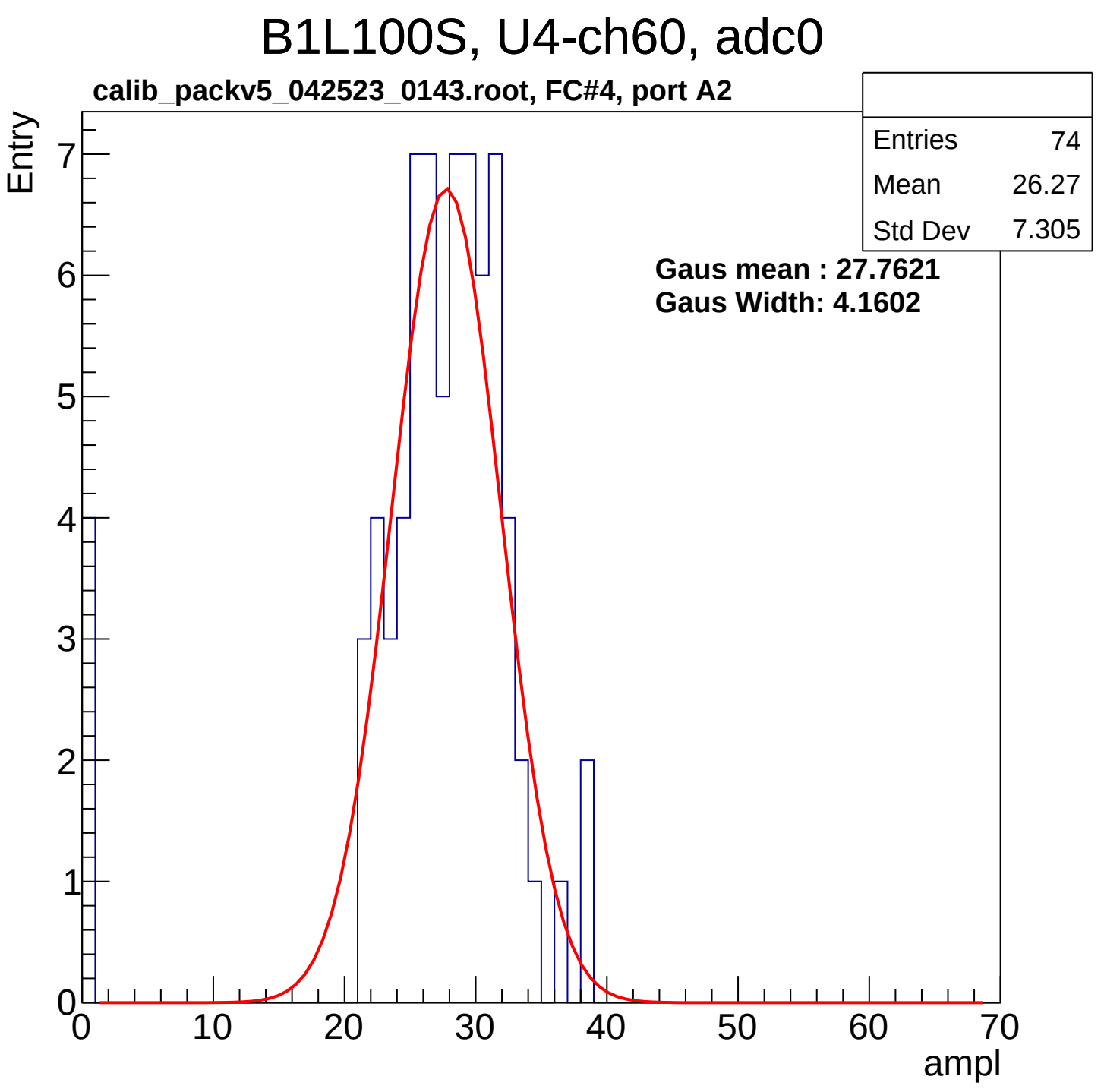

B1L100S, U4-ch59, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 51.57
Std Dev 3.271
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

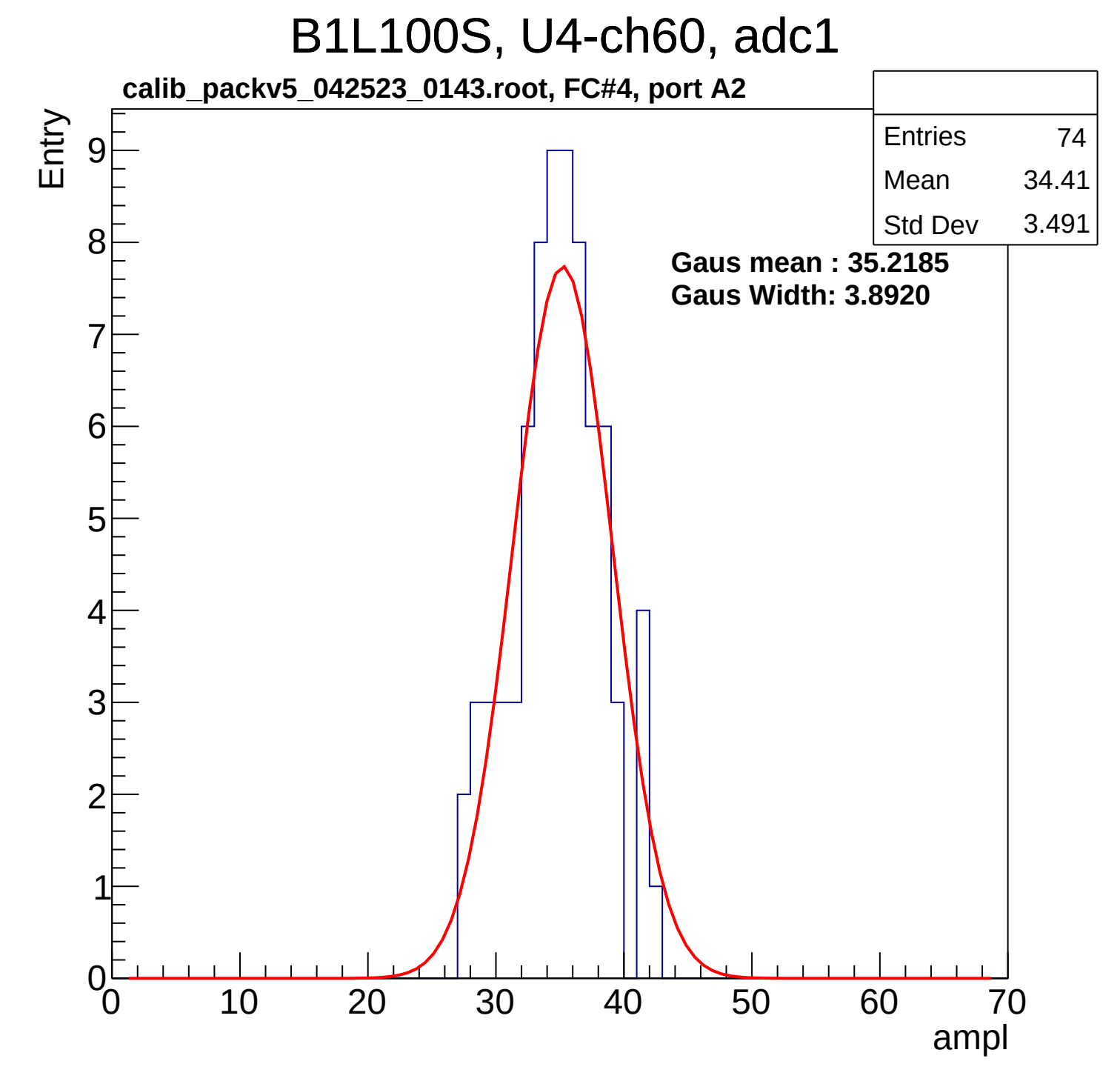

B1L100S, U4-ch59, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 56.98
Std Dev 3.025
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

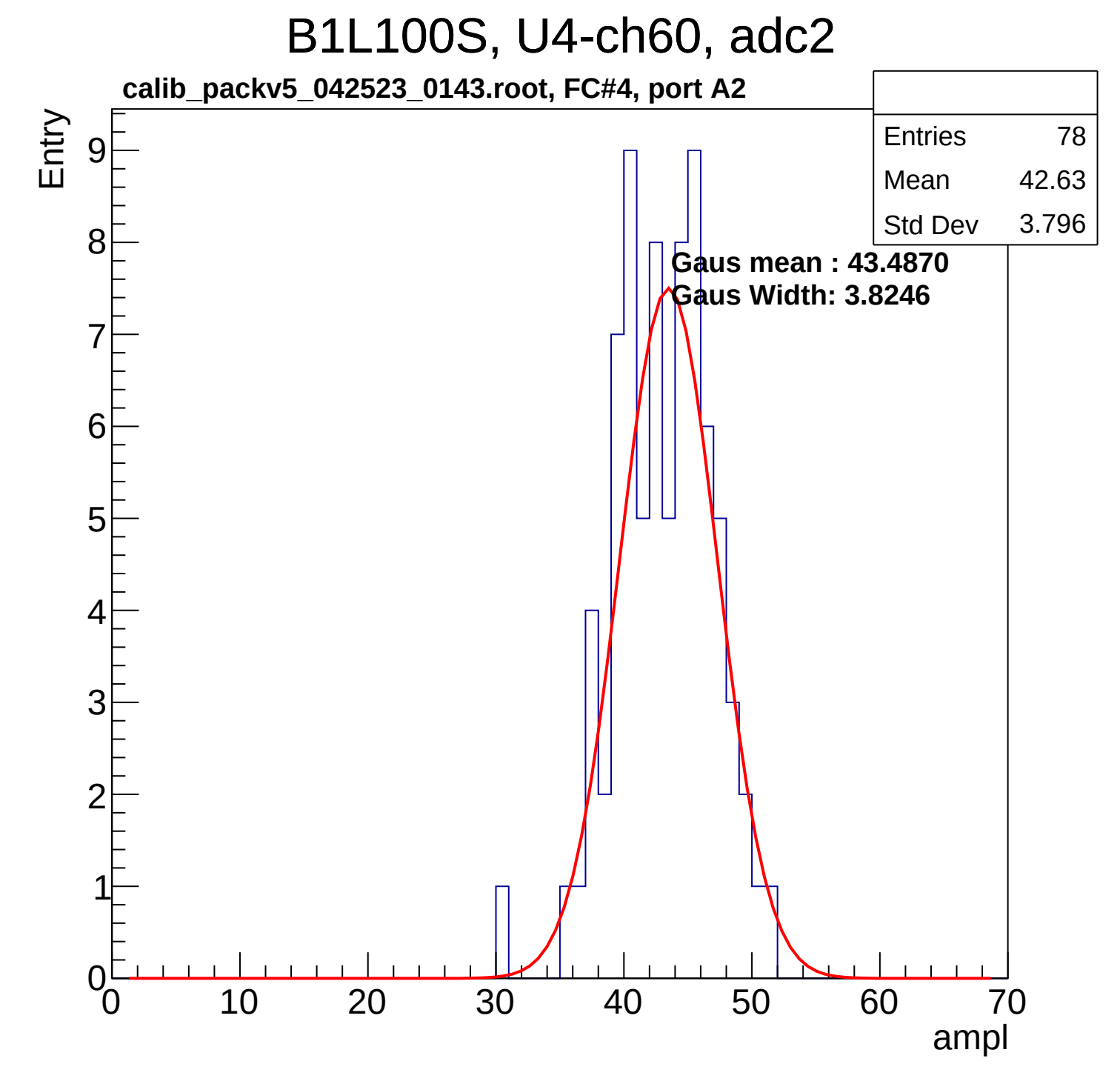

B1L100S, U4-ch59, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 37
Mean 58.46
Std Dev 9.988
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

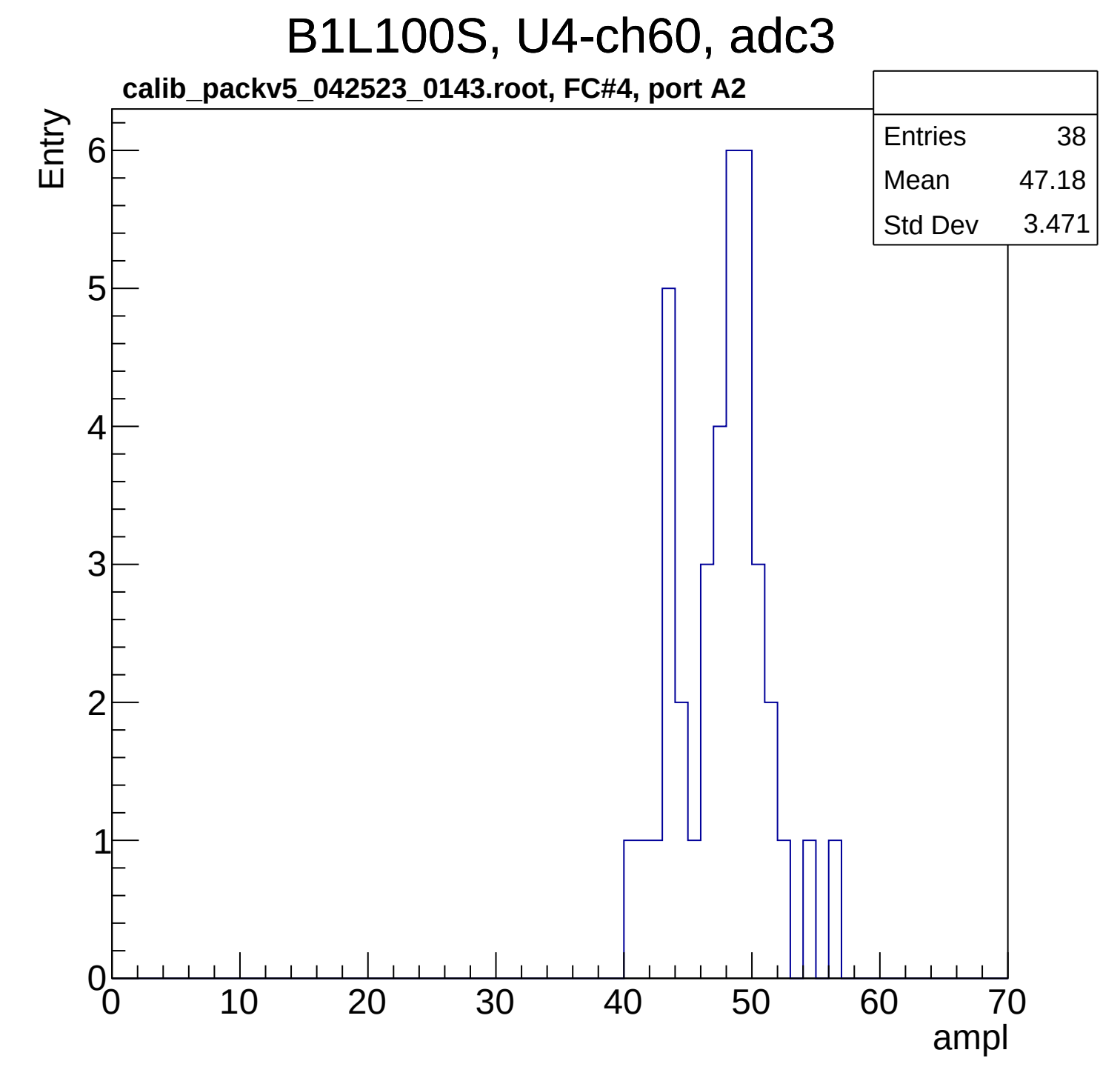

B1L100S, U4-ch59, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 62
Std Dev 1.155
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

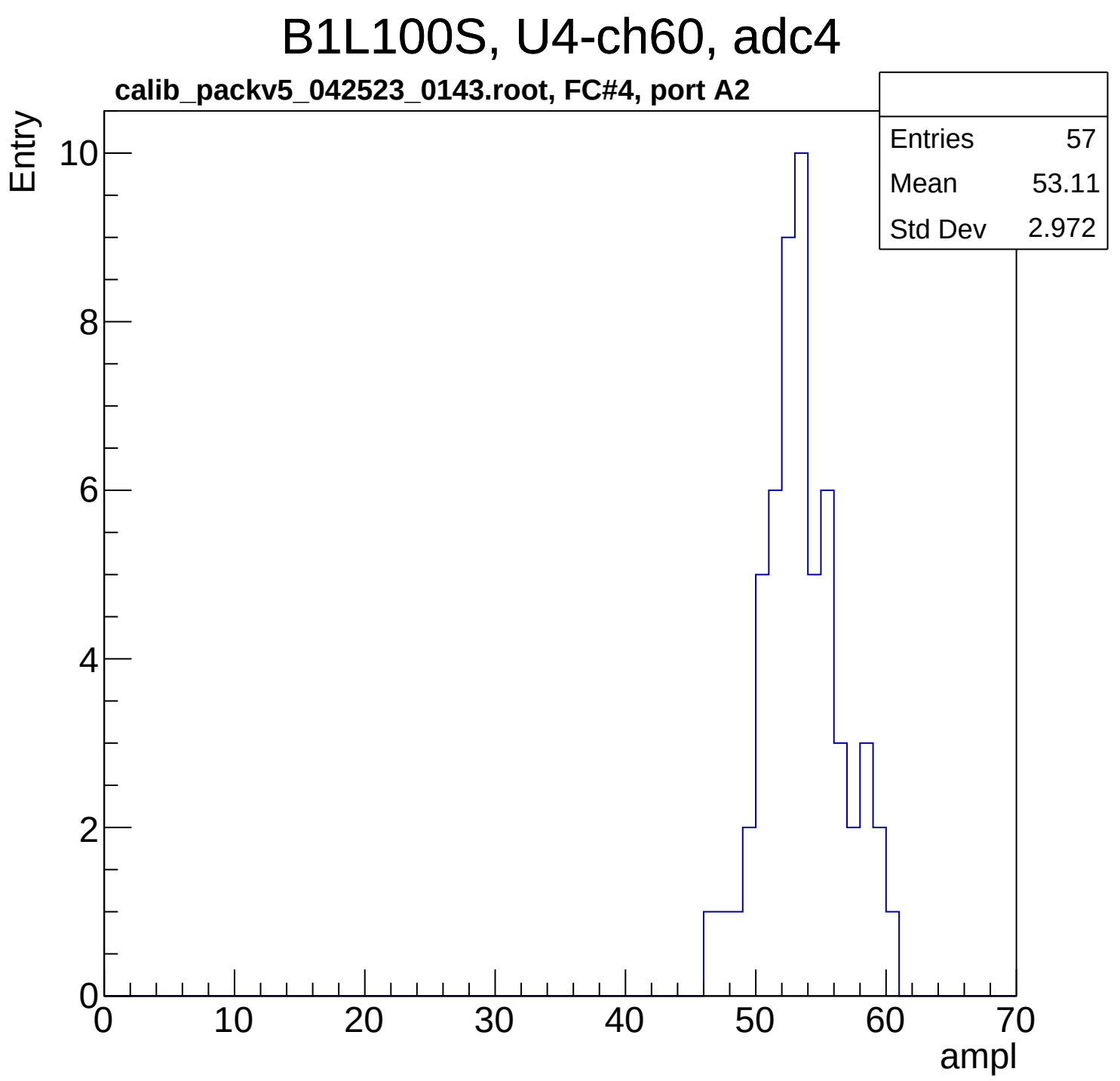

B1L100S, U4-ch59, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

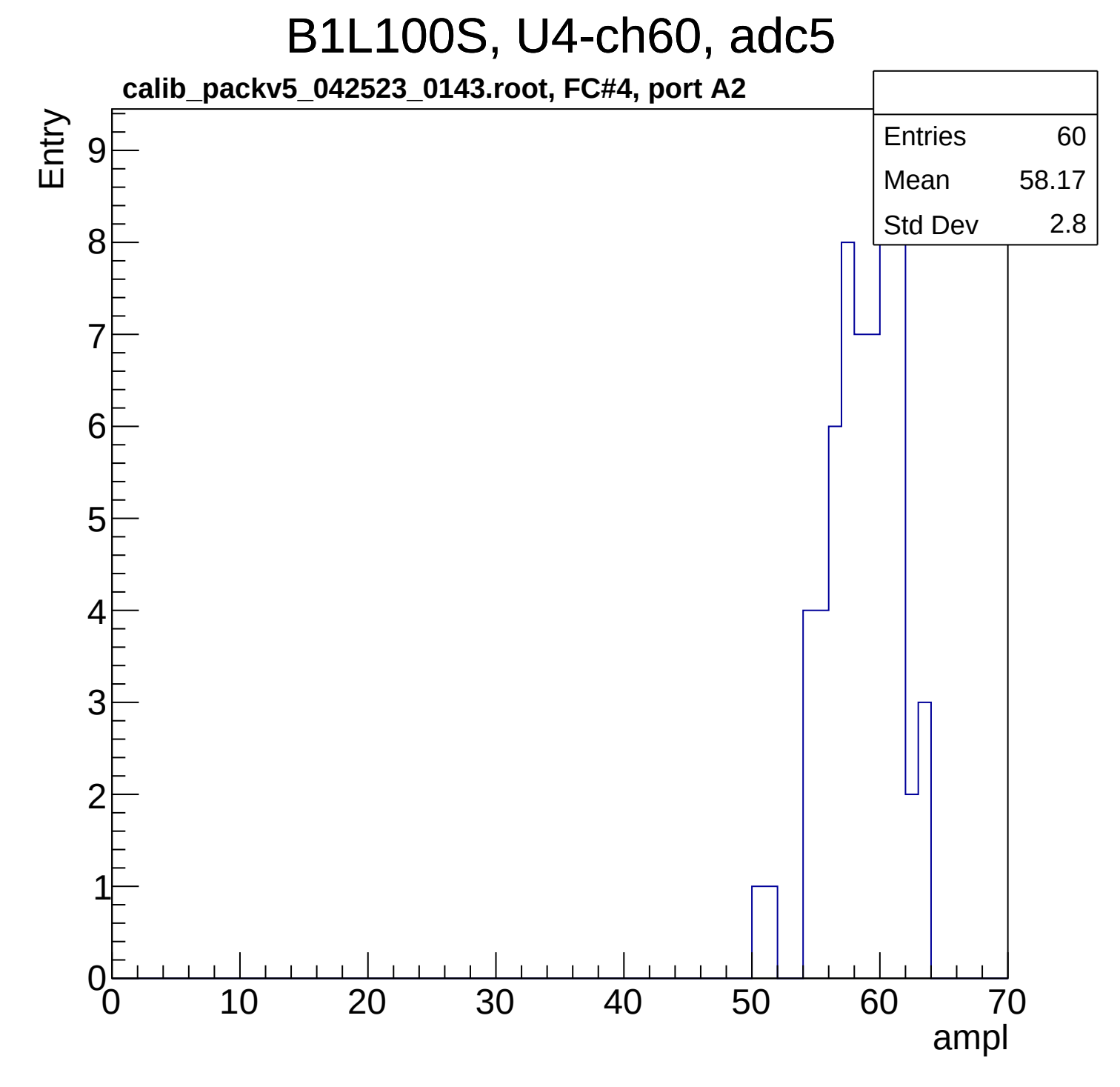

B1L100S, U4-ch60, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 26.27
Std Dev 7.305
Gaus mean : 27.7621
Gaus Width: 4.1602
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

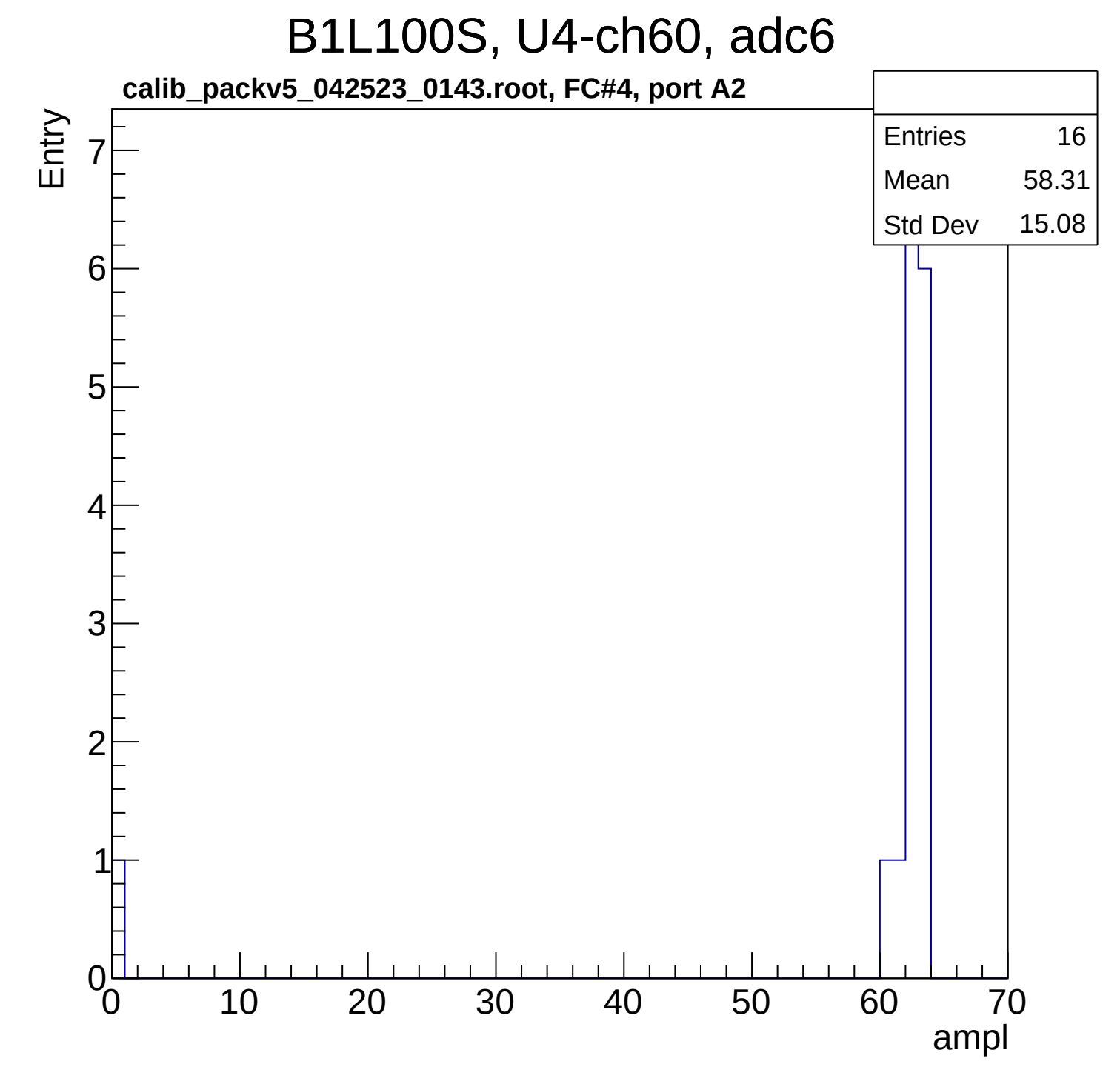

B1L100S, U4-ch60, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 34.41
Std Dev 3.491
Gaus mean : 35.2185
Gaus Width: 3.8920
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

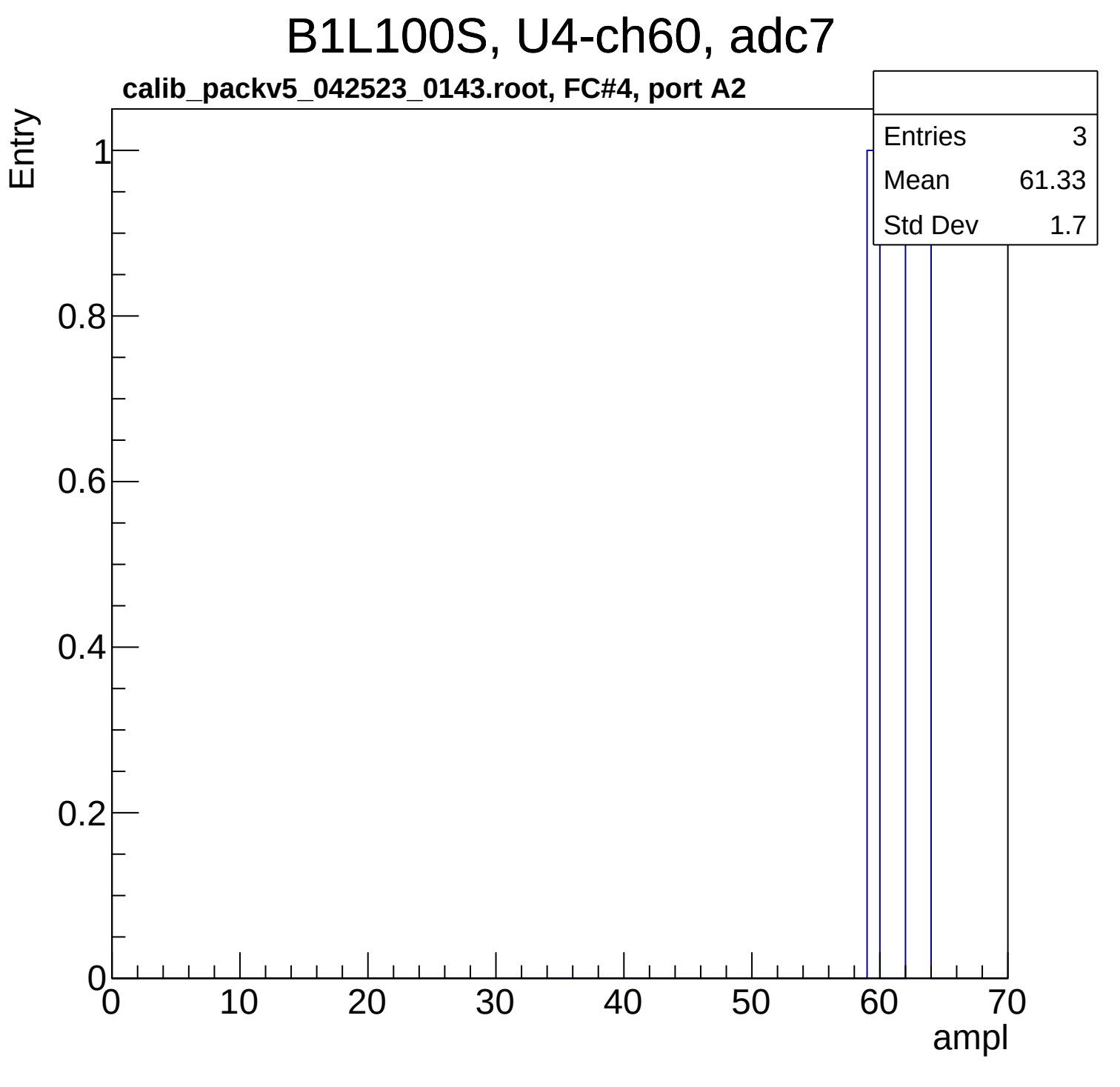

B1L100S, U4-ch60, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 42.63
Std Dev 3.796
Gaus mean : 43.4870
Gaus Width: 3.8246
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

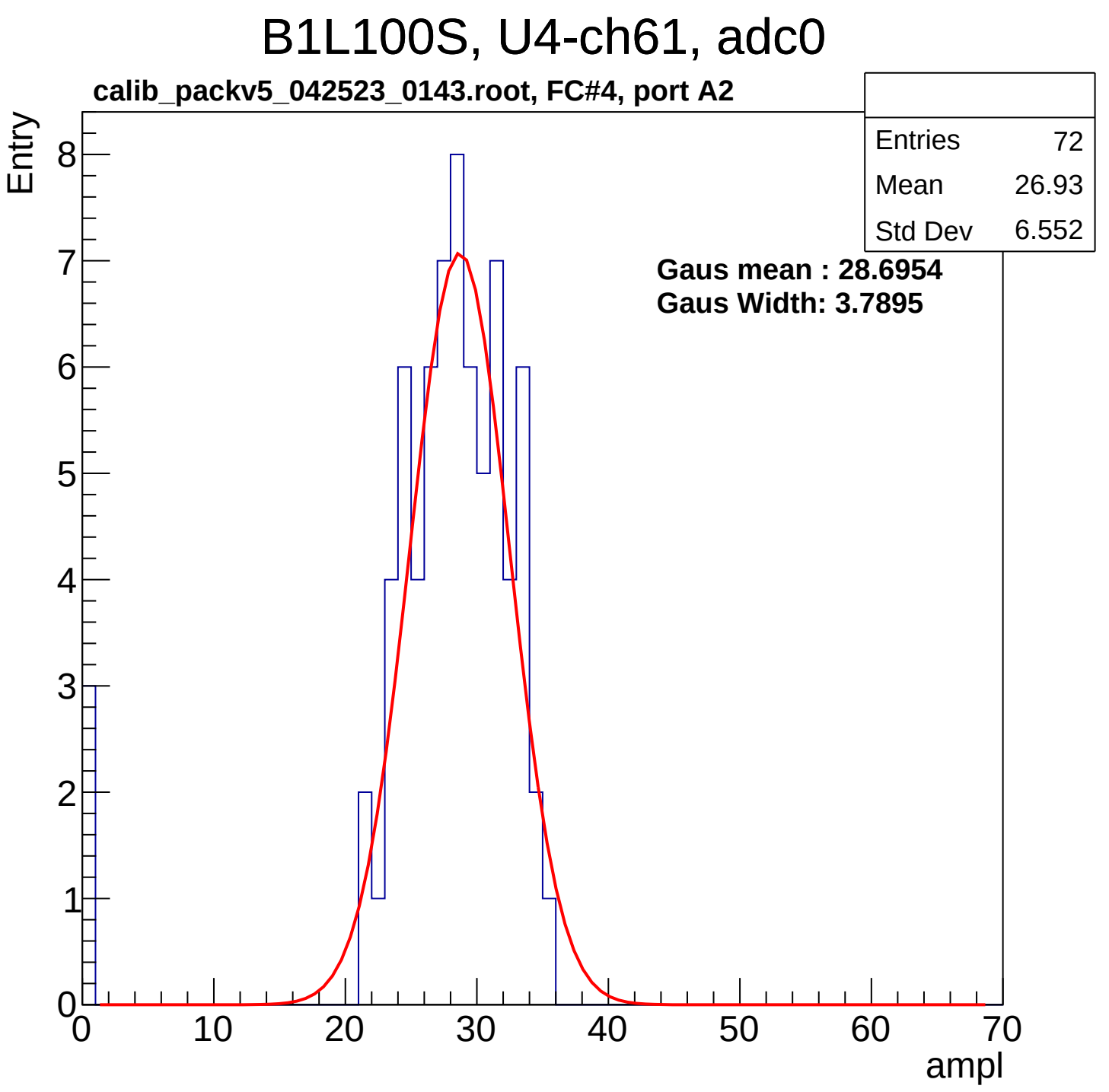

B1L100S, U4-ch60, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 38
Mean 47.18
Std Dev 3.471
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

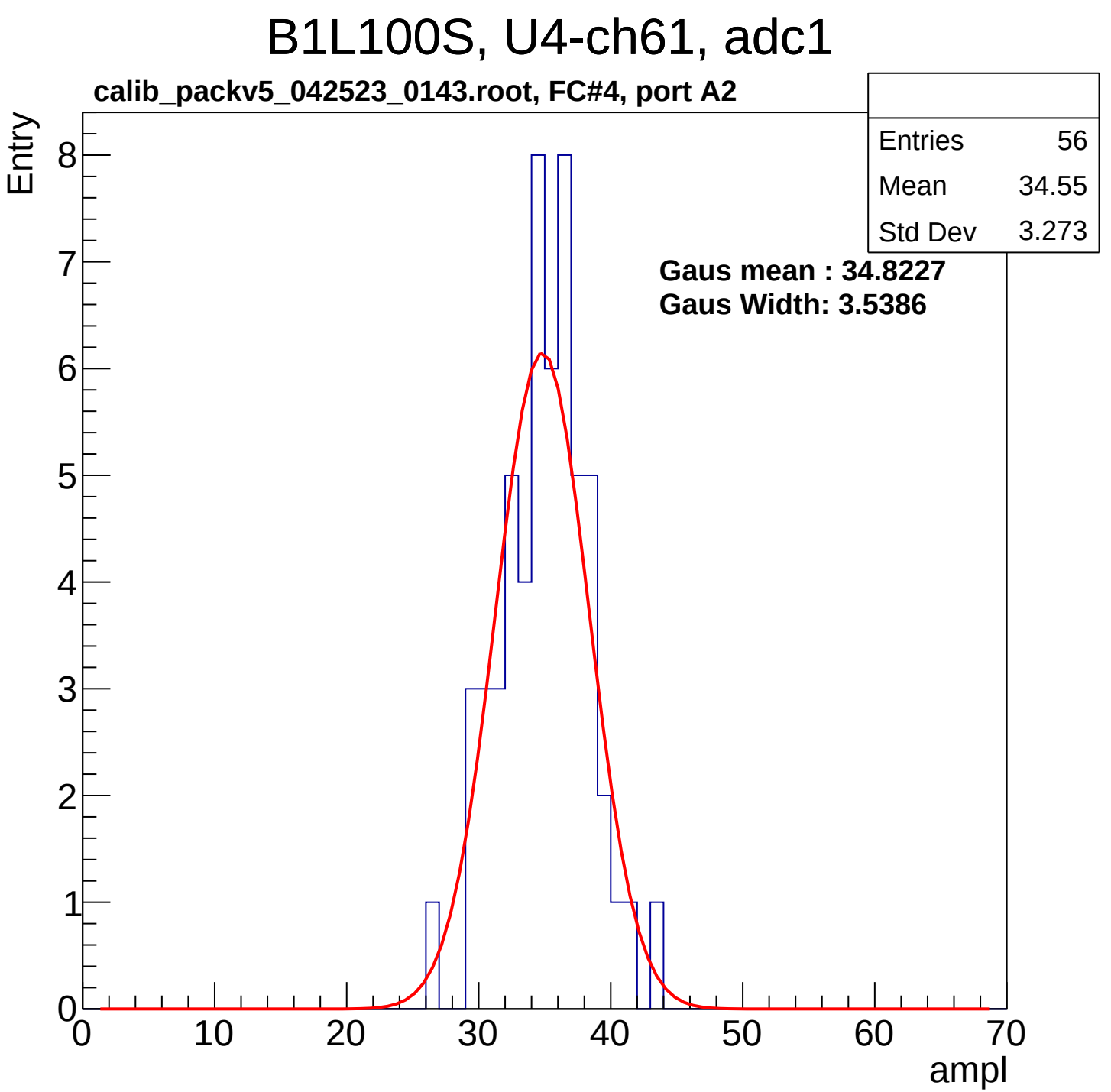

B1L100S, U4-ch60, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 53.11
Std Dev 2.972
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

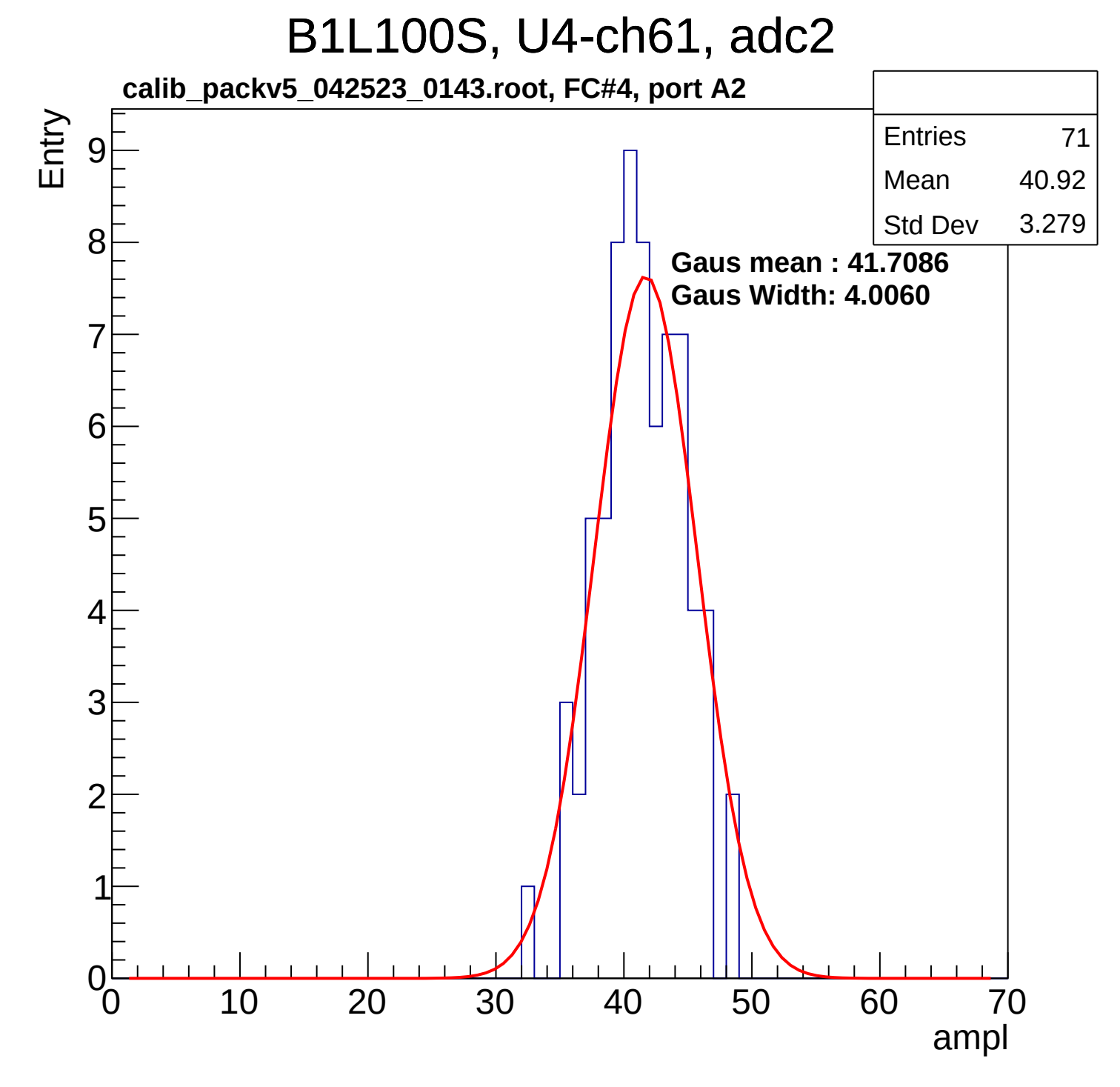

B1L100S, U4-ch60, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 58.17
Std Dev 2.8
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

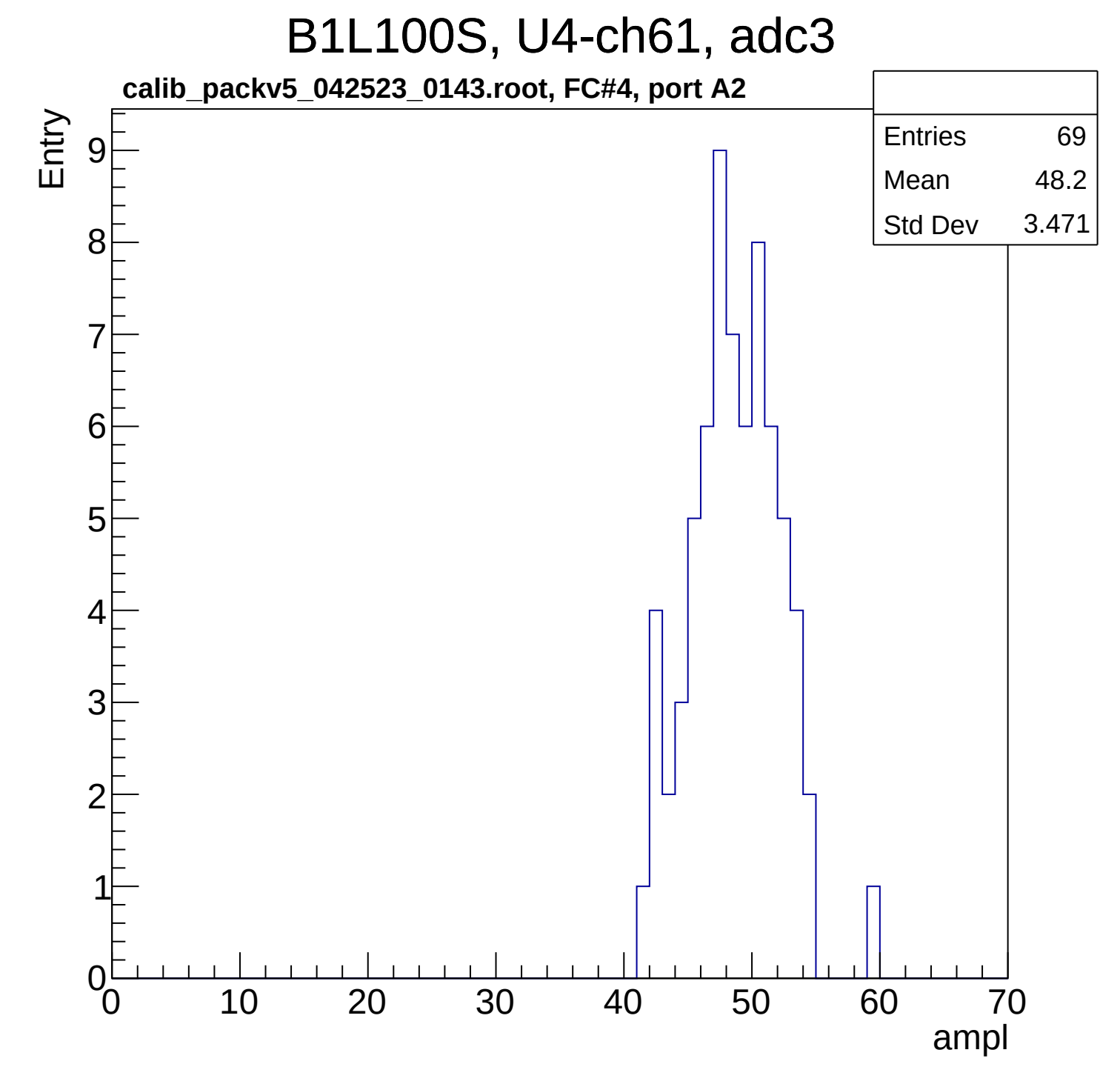

B1L100S, U4-ch60, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 16
Mean 58.31
Std Dev 15.08
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

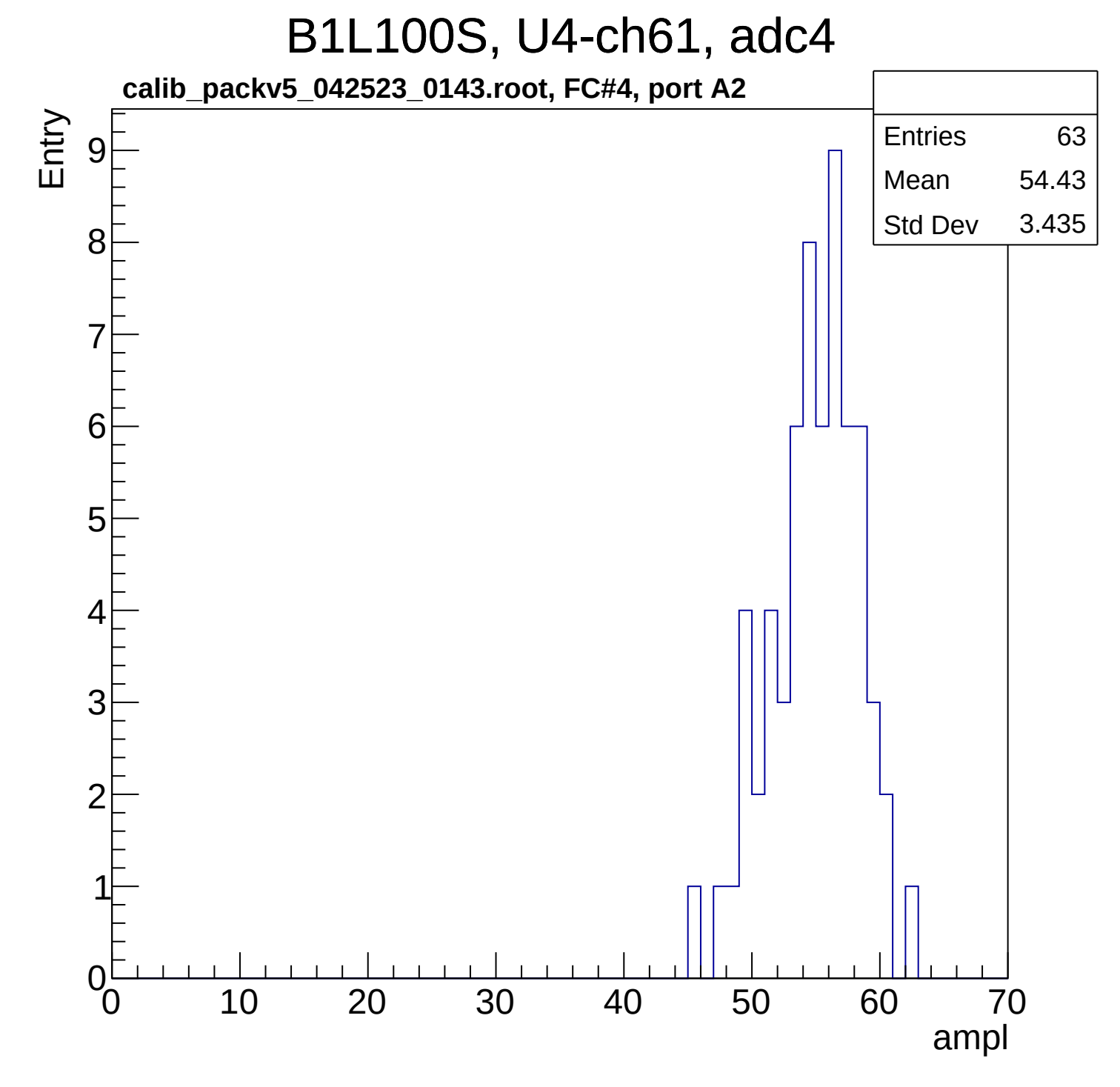

B1L100S, U4-ch60, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 61.33
Std Dev 1.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

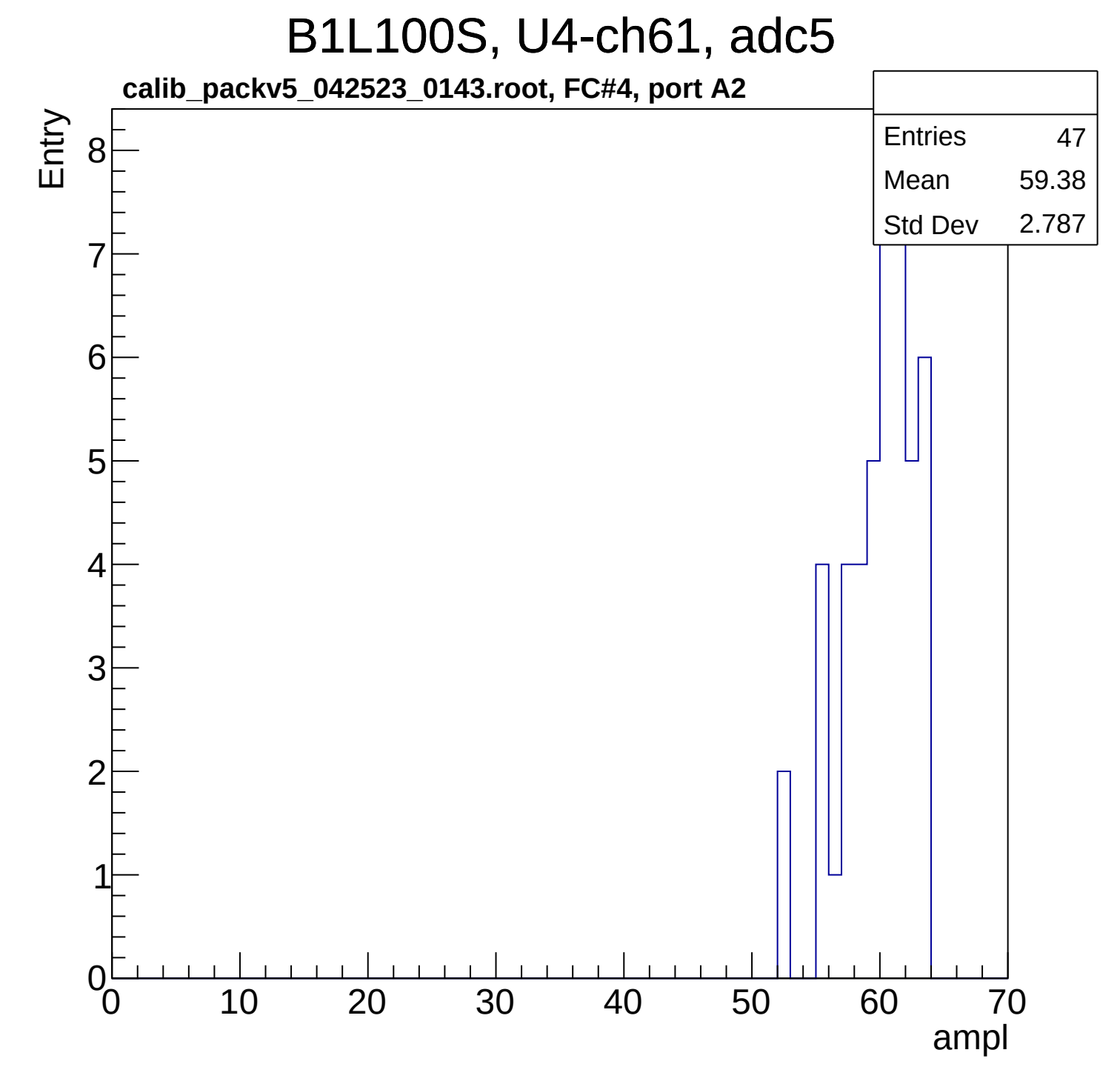

B1L100S, U4-ch61, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 26.93
Std Dev 6.552
Gaus mean : 28.6954
Gaus Width: 3.7895
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

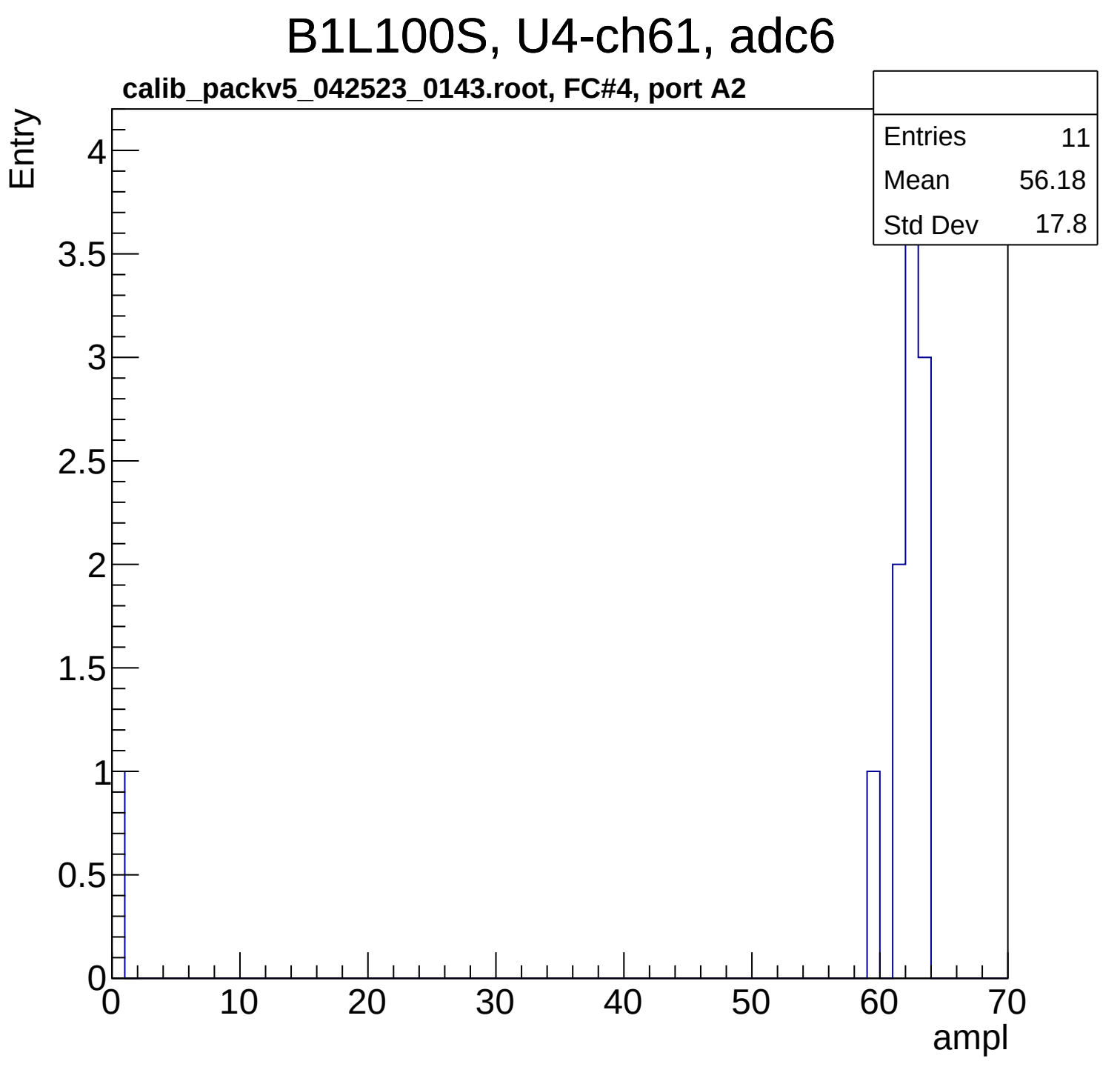

B1L100S, U4-ch61, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 34.55
Std Dev 3.273
Gaus mean : 34.8227
Gaus Width: 3.5386
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

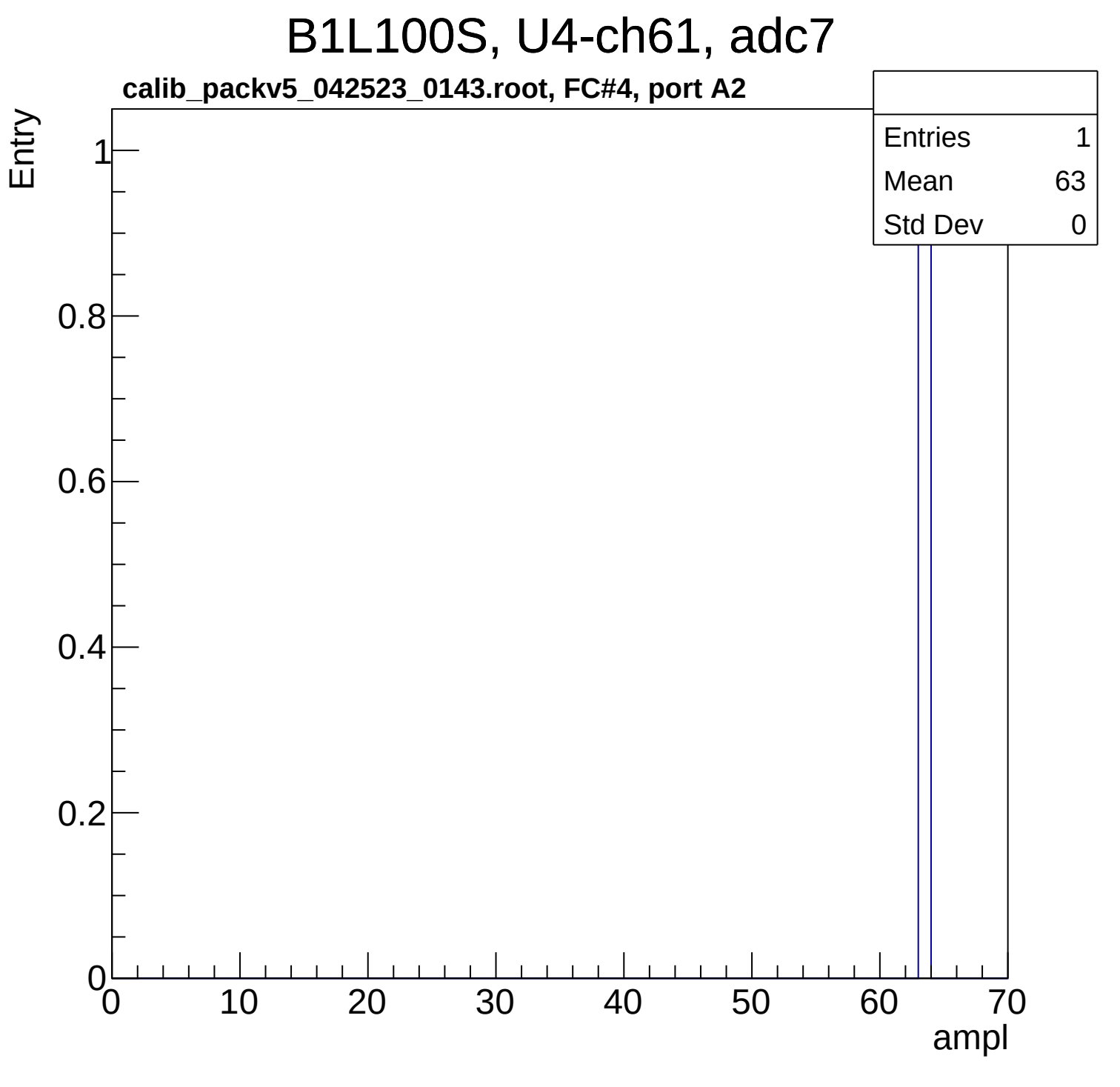

B1L100S, U4-ch61, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 40.92
Std Dev 3.279
Gaus mean : 41.7086
Gaus Width: 4.0060
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

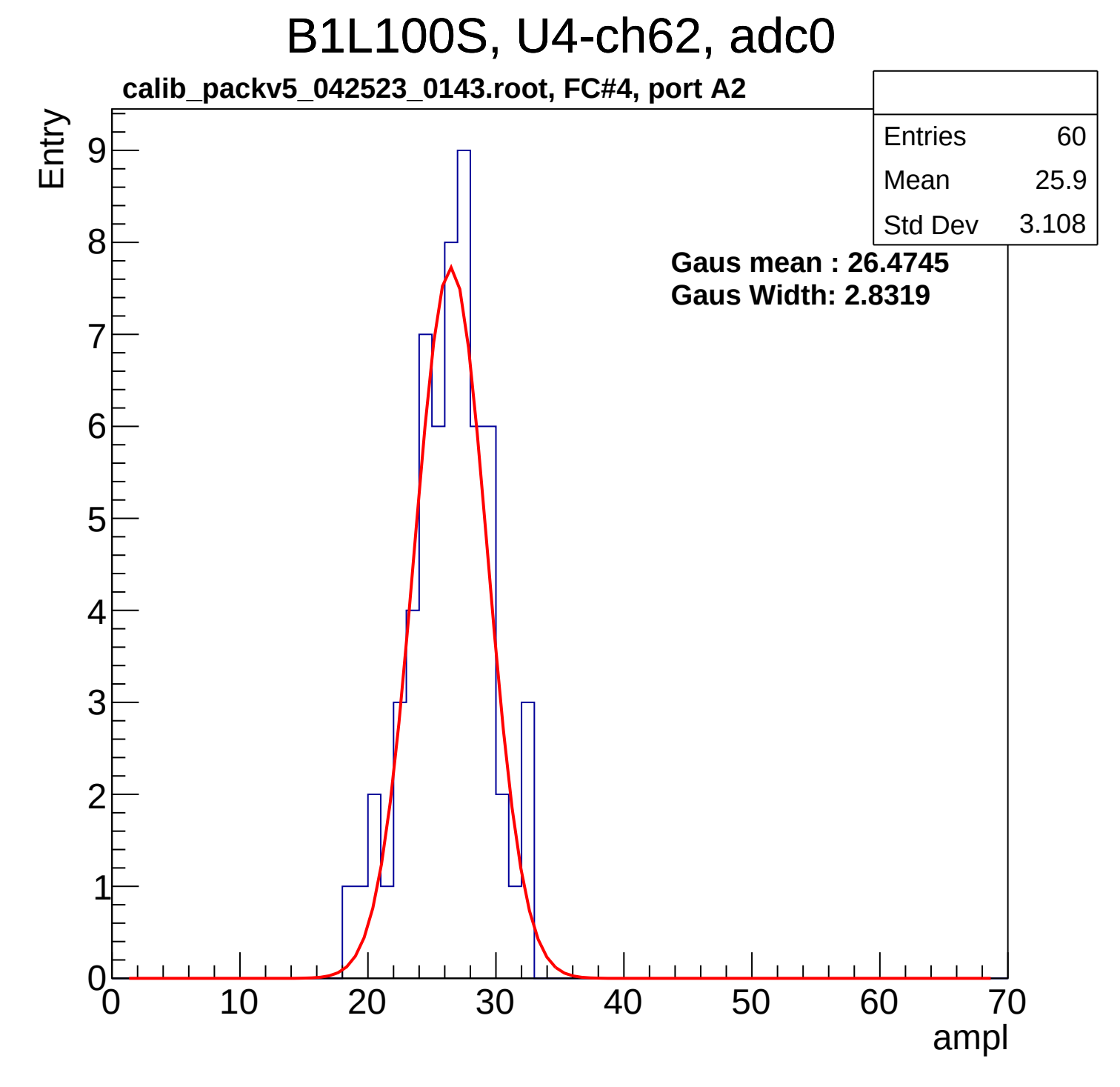

B1L100S, U4-ch61, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 48.2
Std Dev 3.471
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

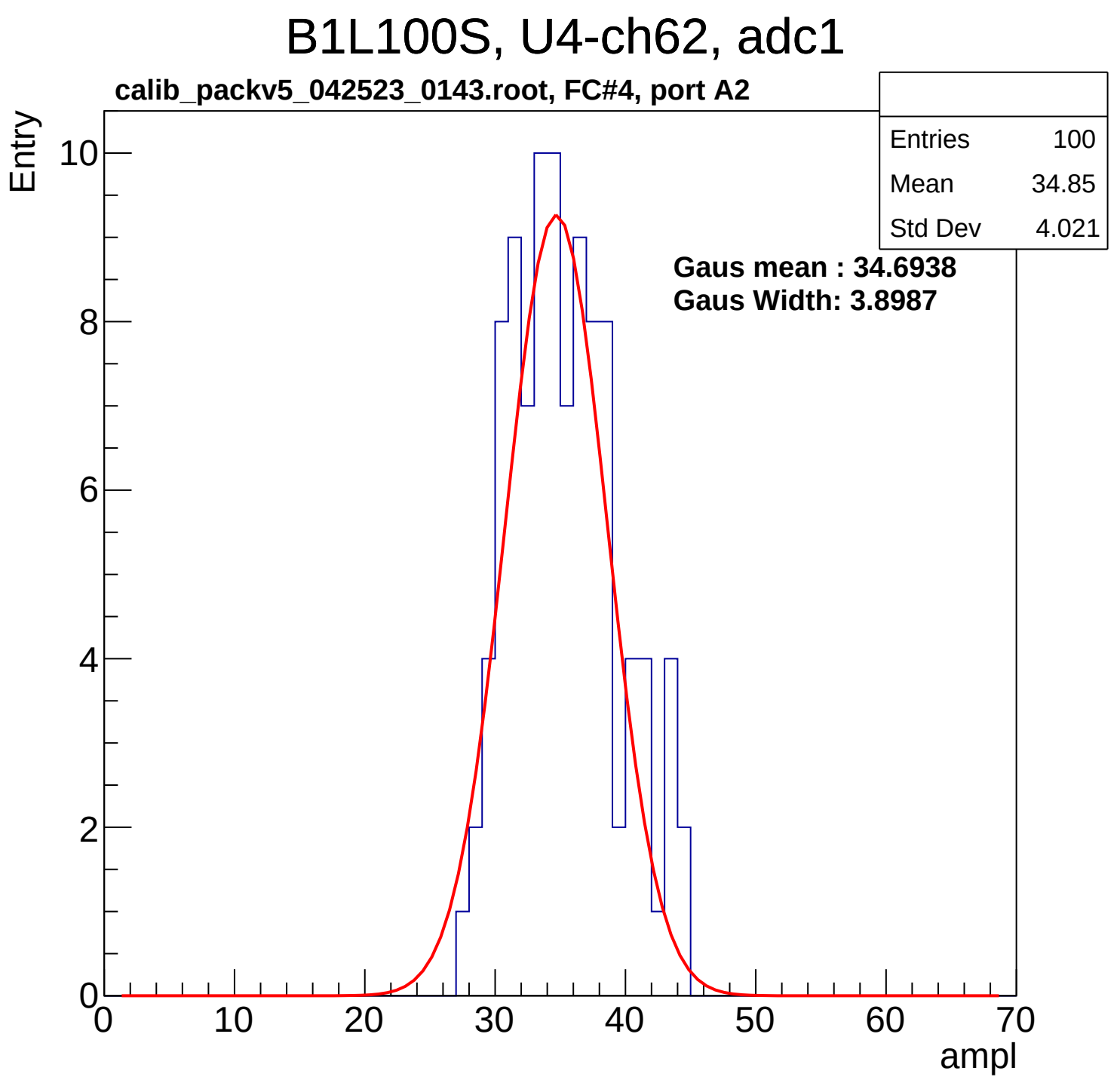

B1L100S, U4-ch61, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 54.43
Std Dev 3.435
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

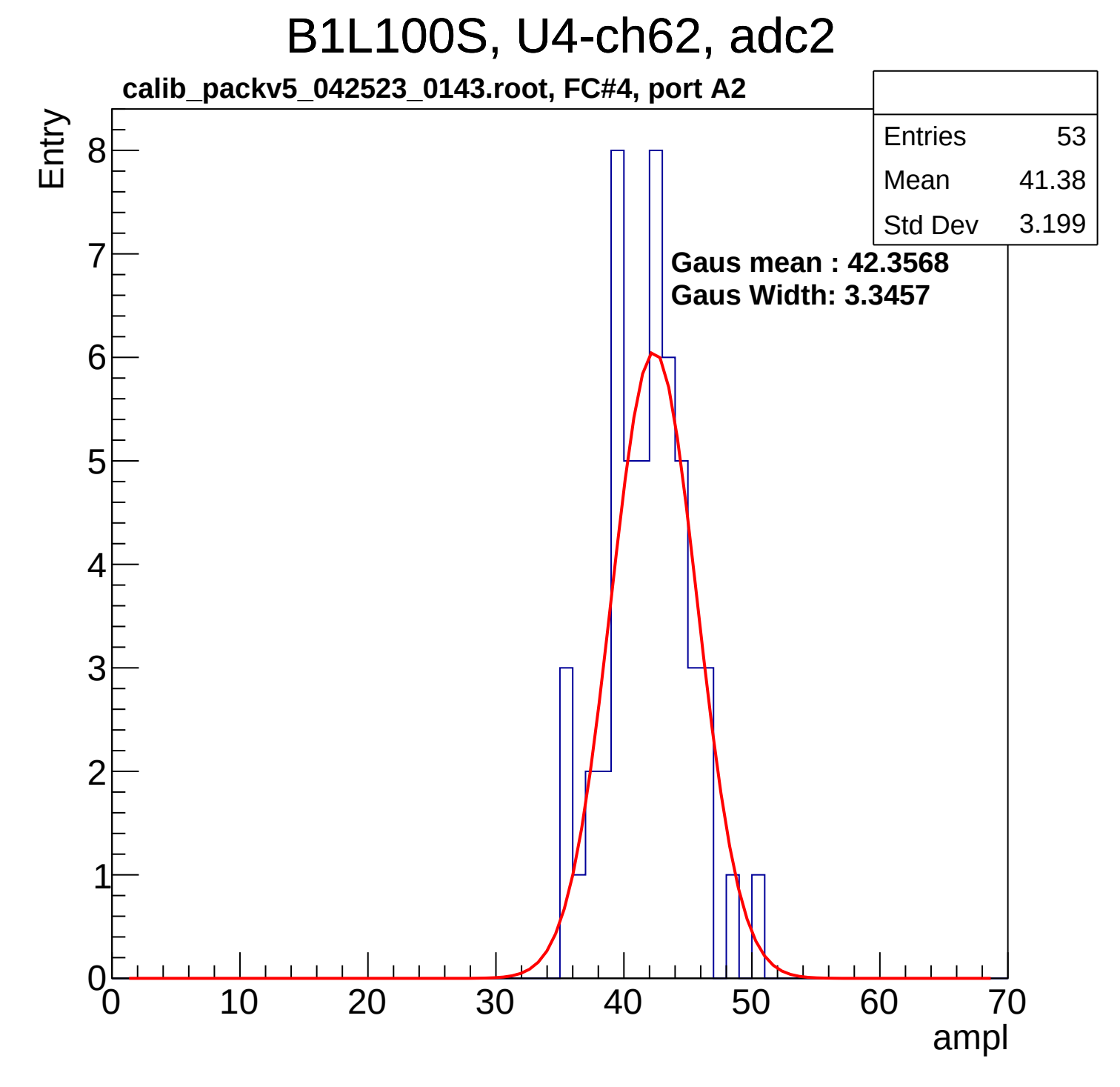

B1L100S, U4-ch61, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 59.38
Std Dev 2.787
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

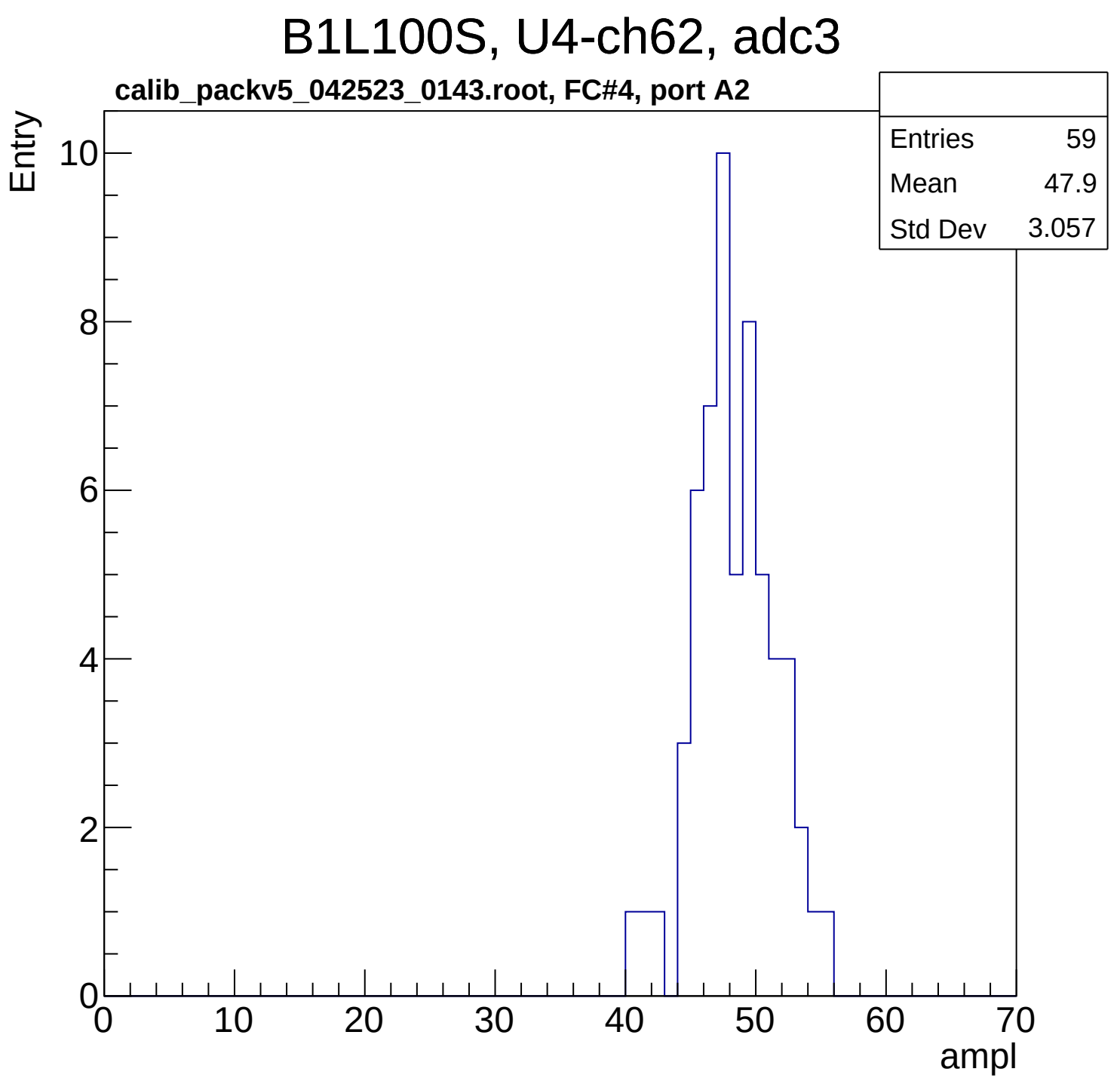

B1L100S, U4-ch61, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 56.18
Std Dev 17.8
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

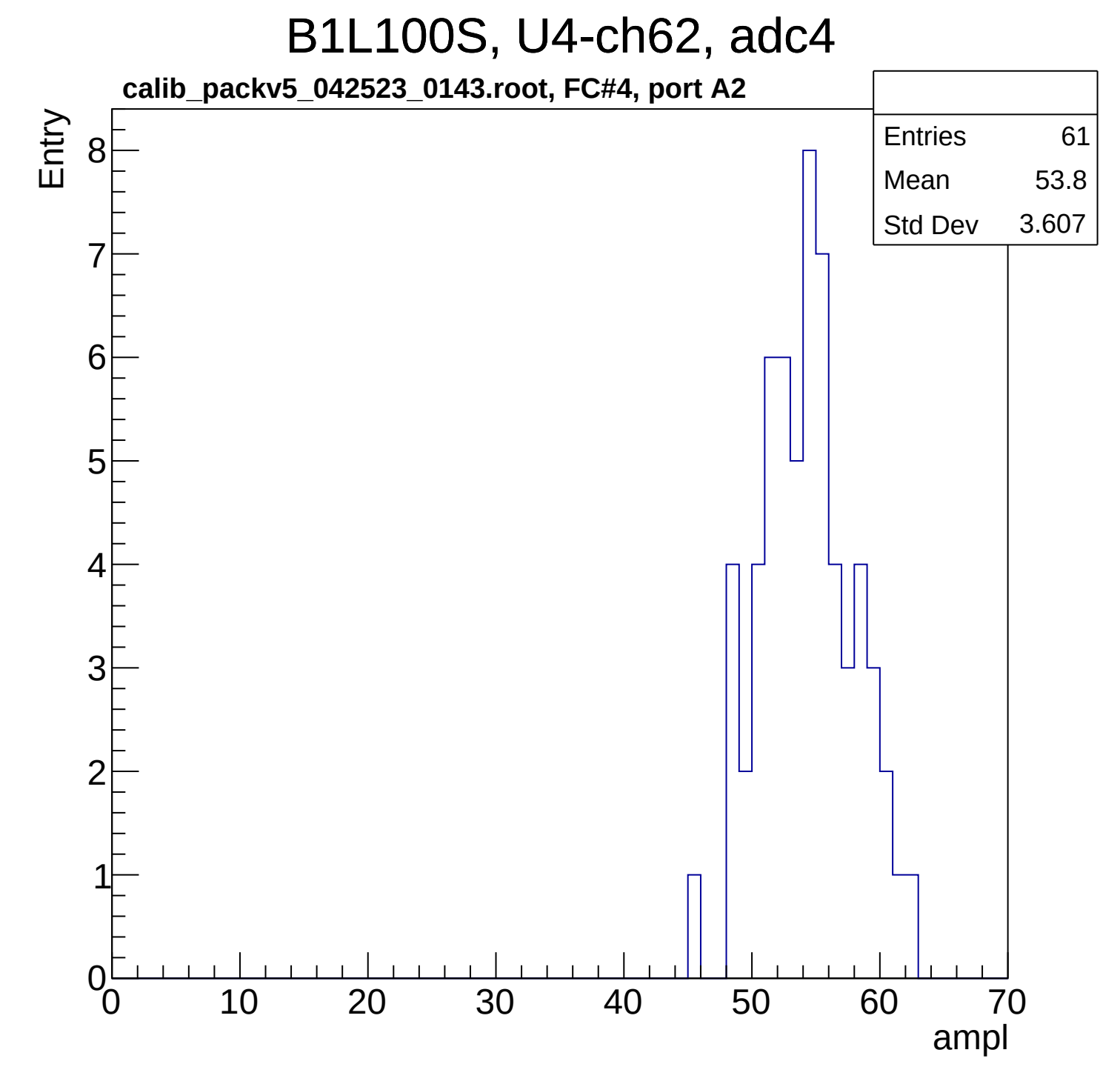

B1L100S, U4-ch61, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

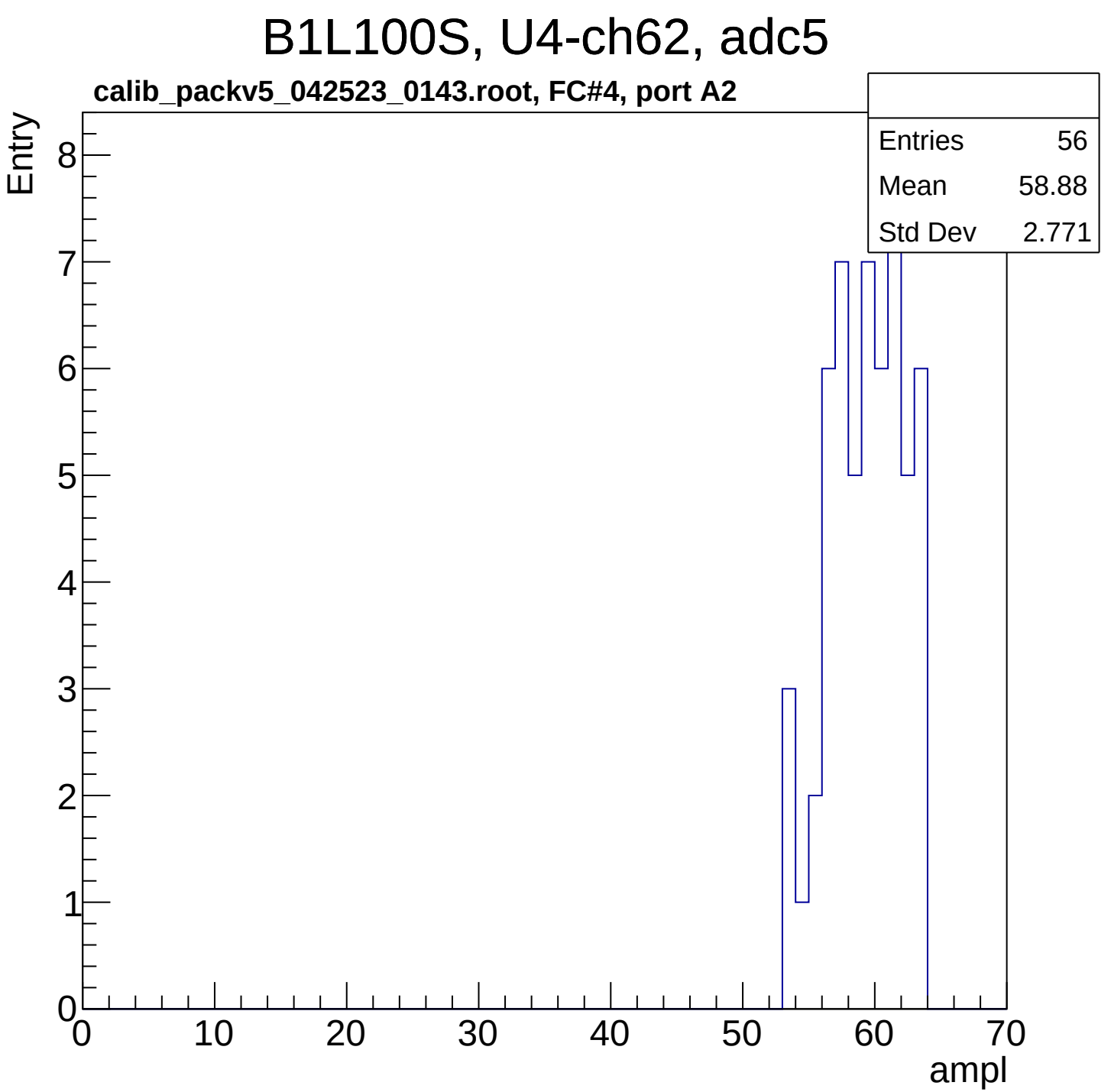

B1L100S, U4-ch62, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 25.9
Std Dev 3.108
Gaus mean : 26.4745
Gaus Width: 2.8319
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

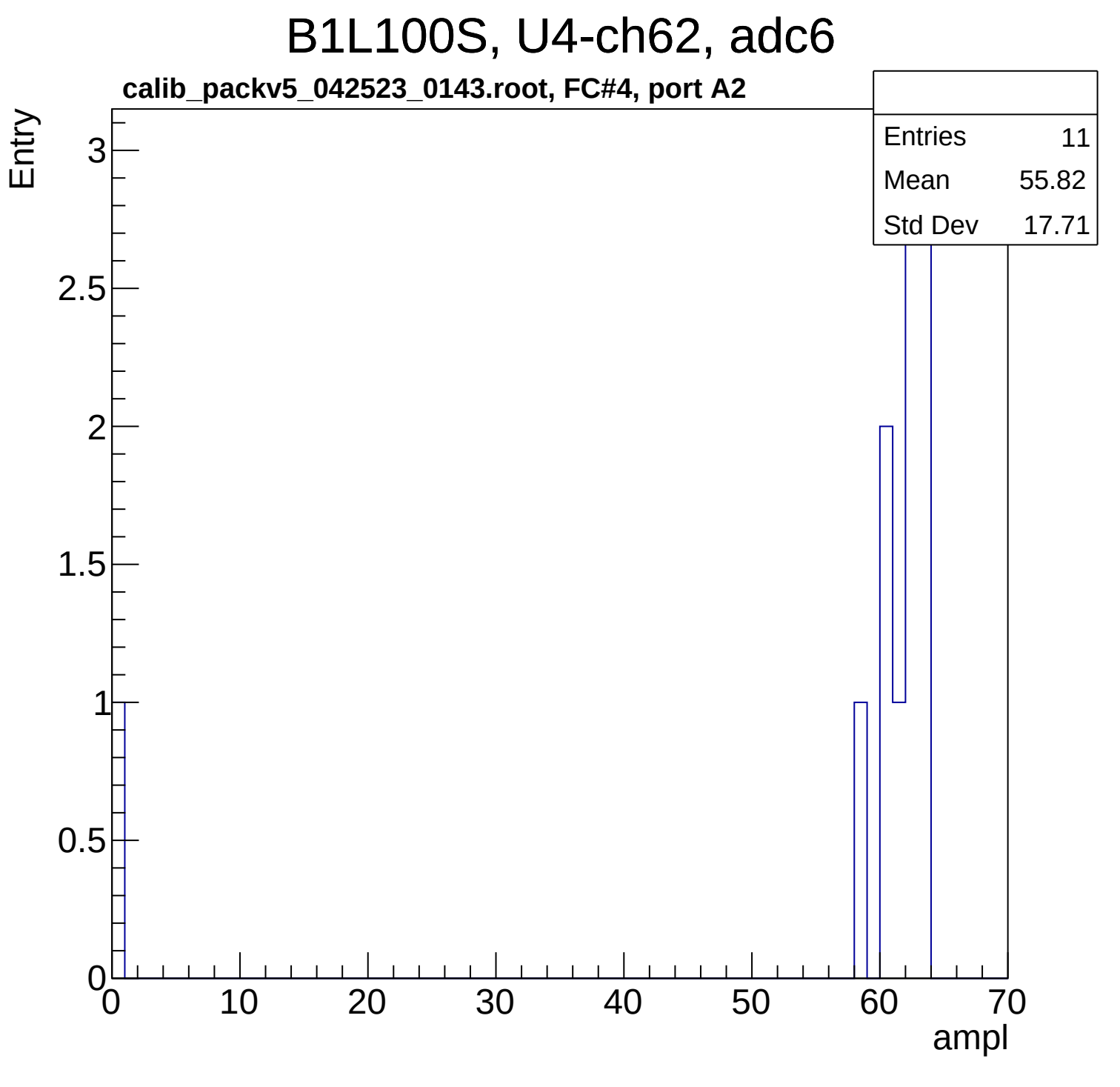

B1L100S, U4-ch62, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 100
Mean 34.85
Std Dev 4.021
Gaus mean : 34.6938
Gaus Width: 3.8987
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

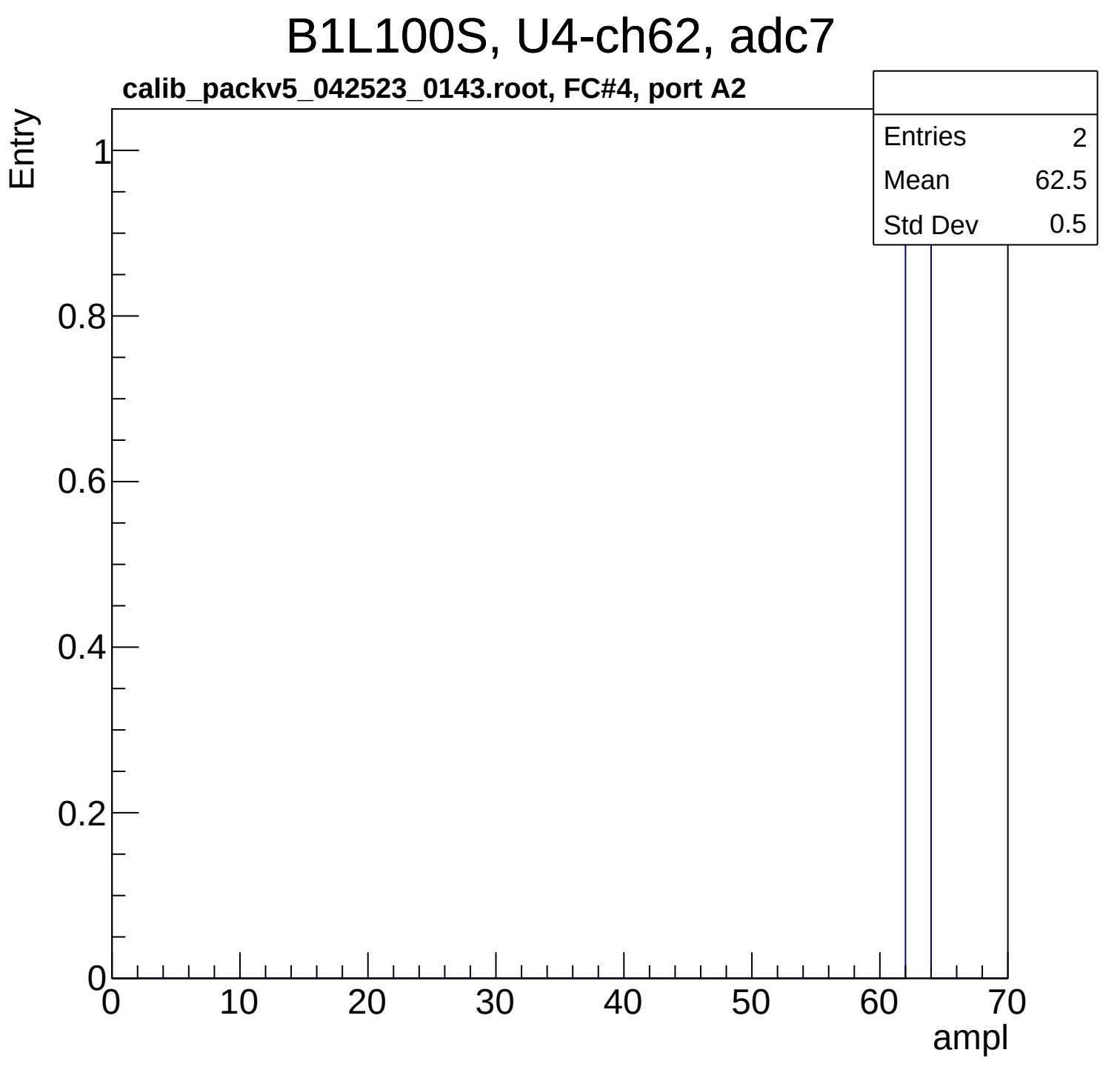

B1L100S, U4-ch62, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 41.38
Std Dev 3.199
Gaus mean : 42.3568
Gaus Width: 3.3457
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

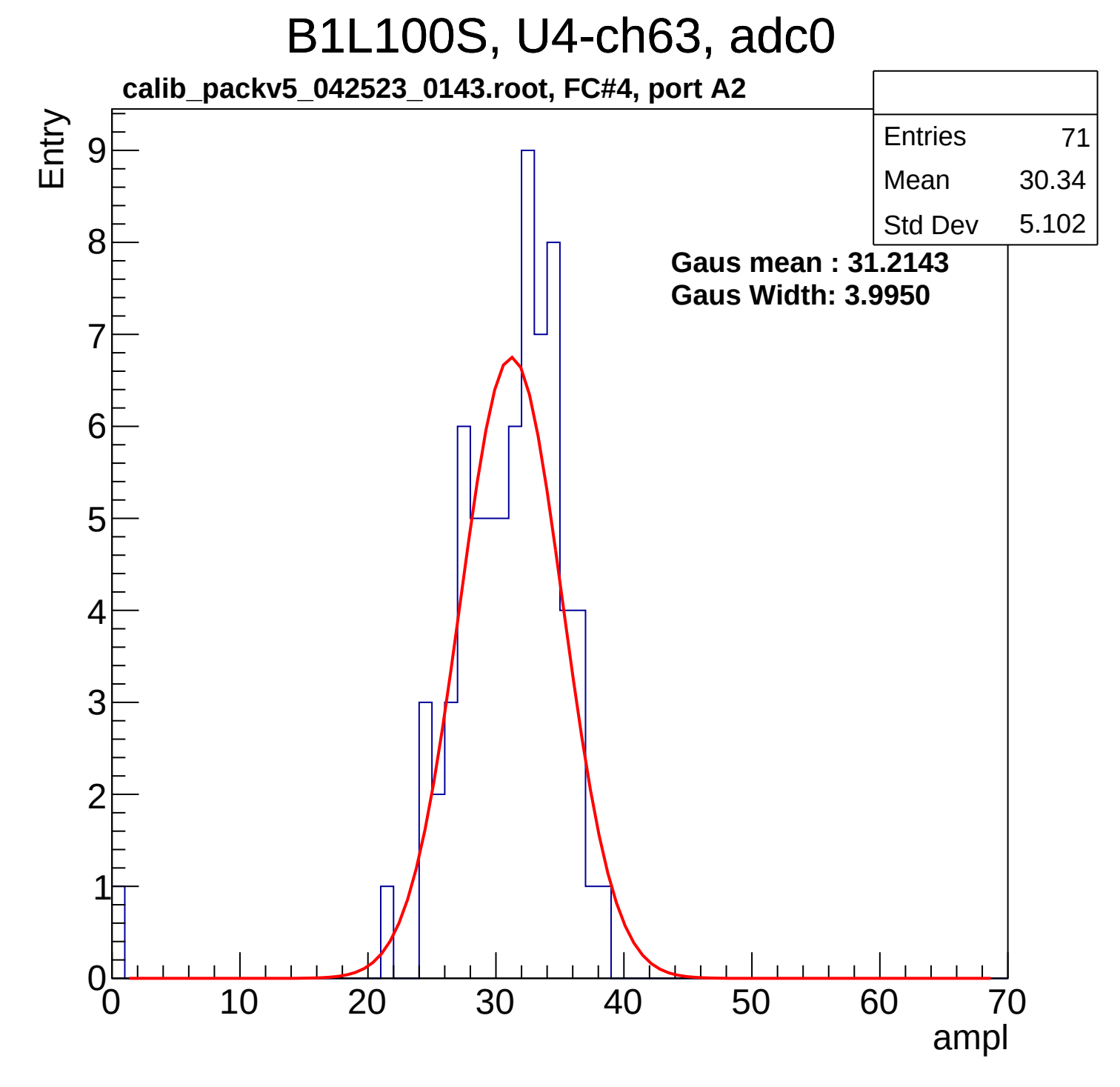

B1L100S, U4-ch62, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 47.9
Std Dev 3.057
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

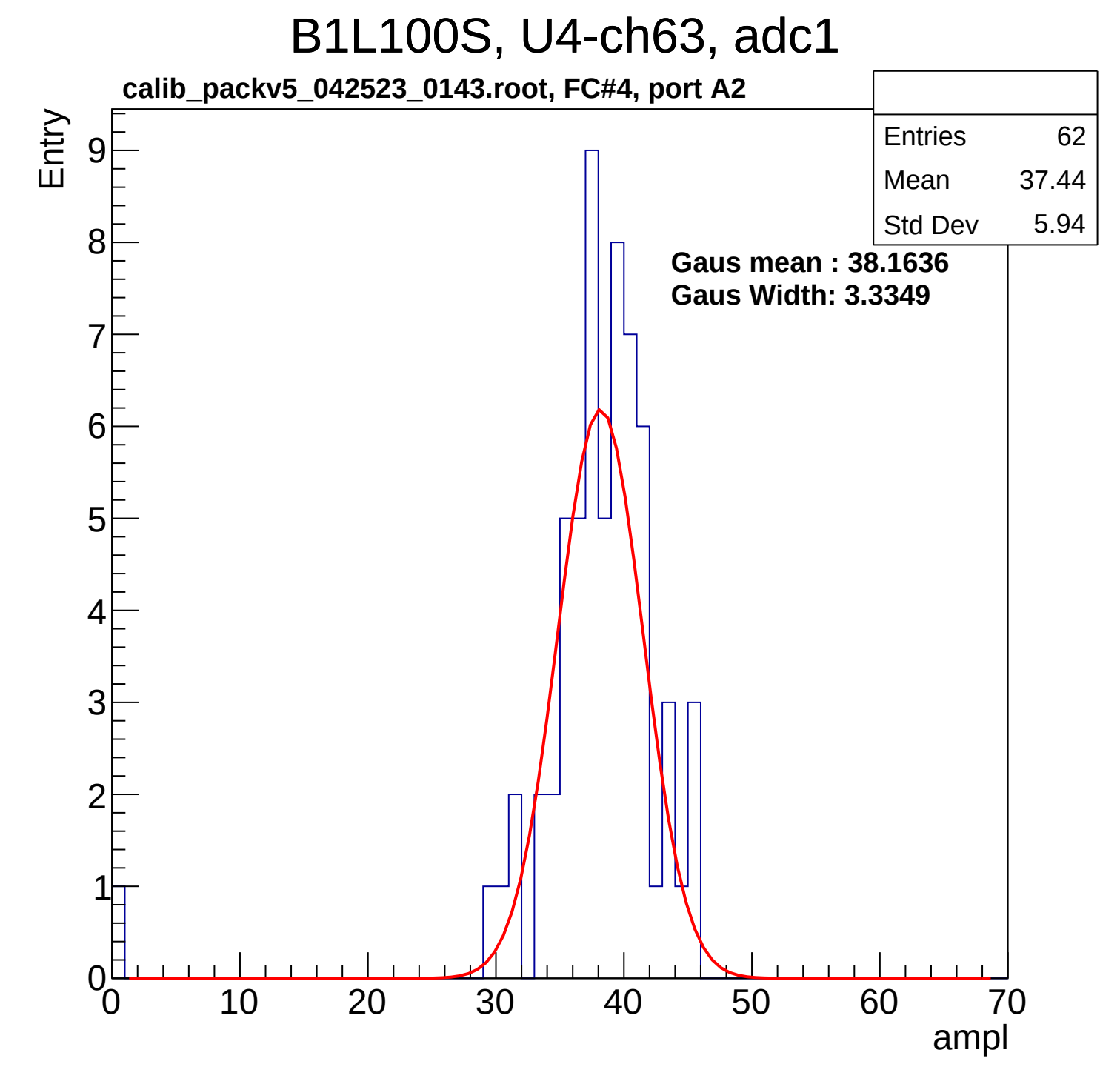

B1L100S, U4-ch62, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 53.8
Std Dev 3.607
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

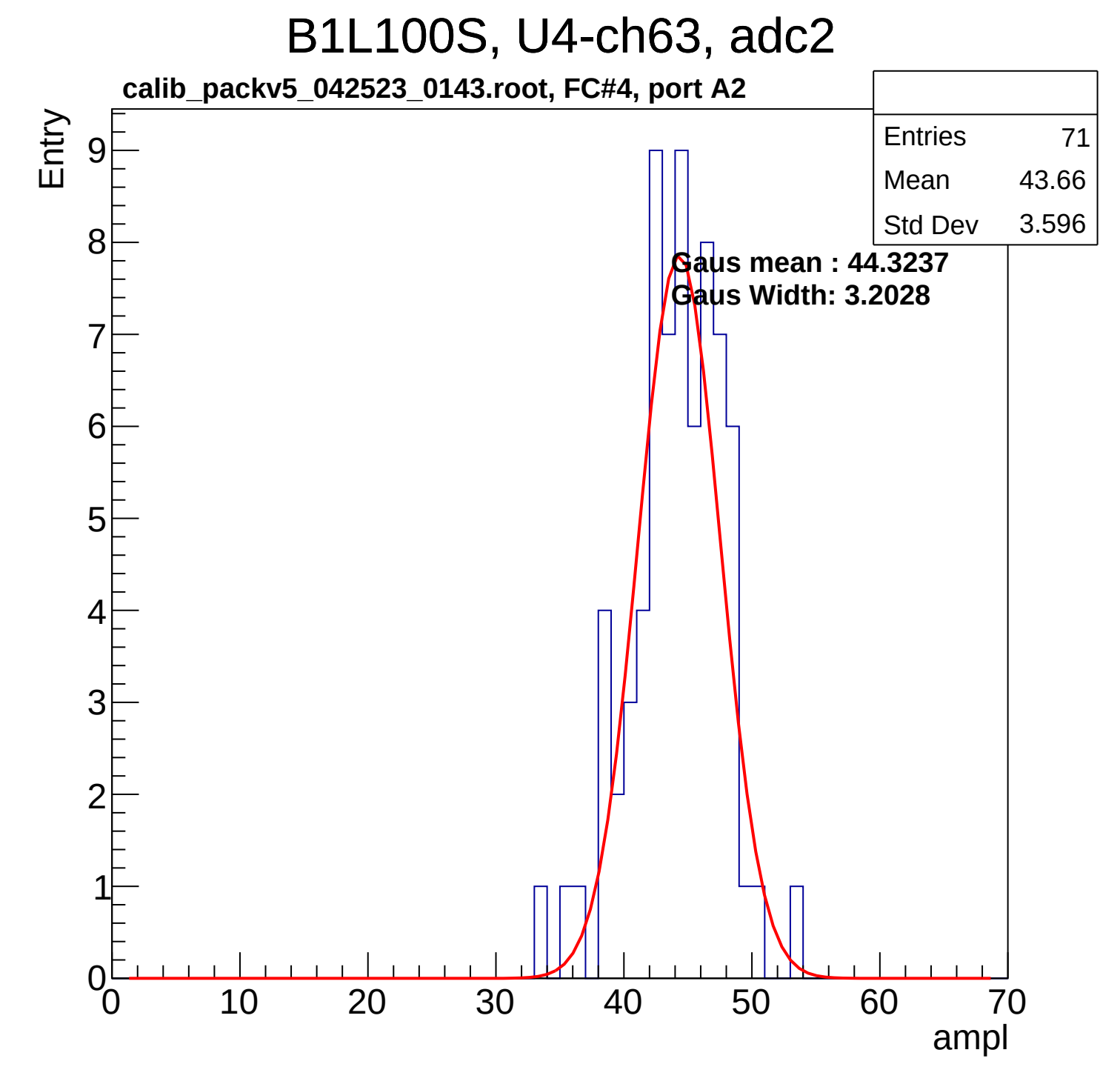

B1L100S, U4-ch62, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 58.88
Std Dev 2.771
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

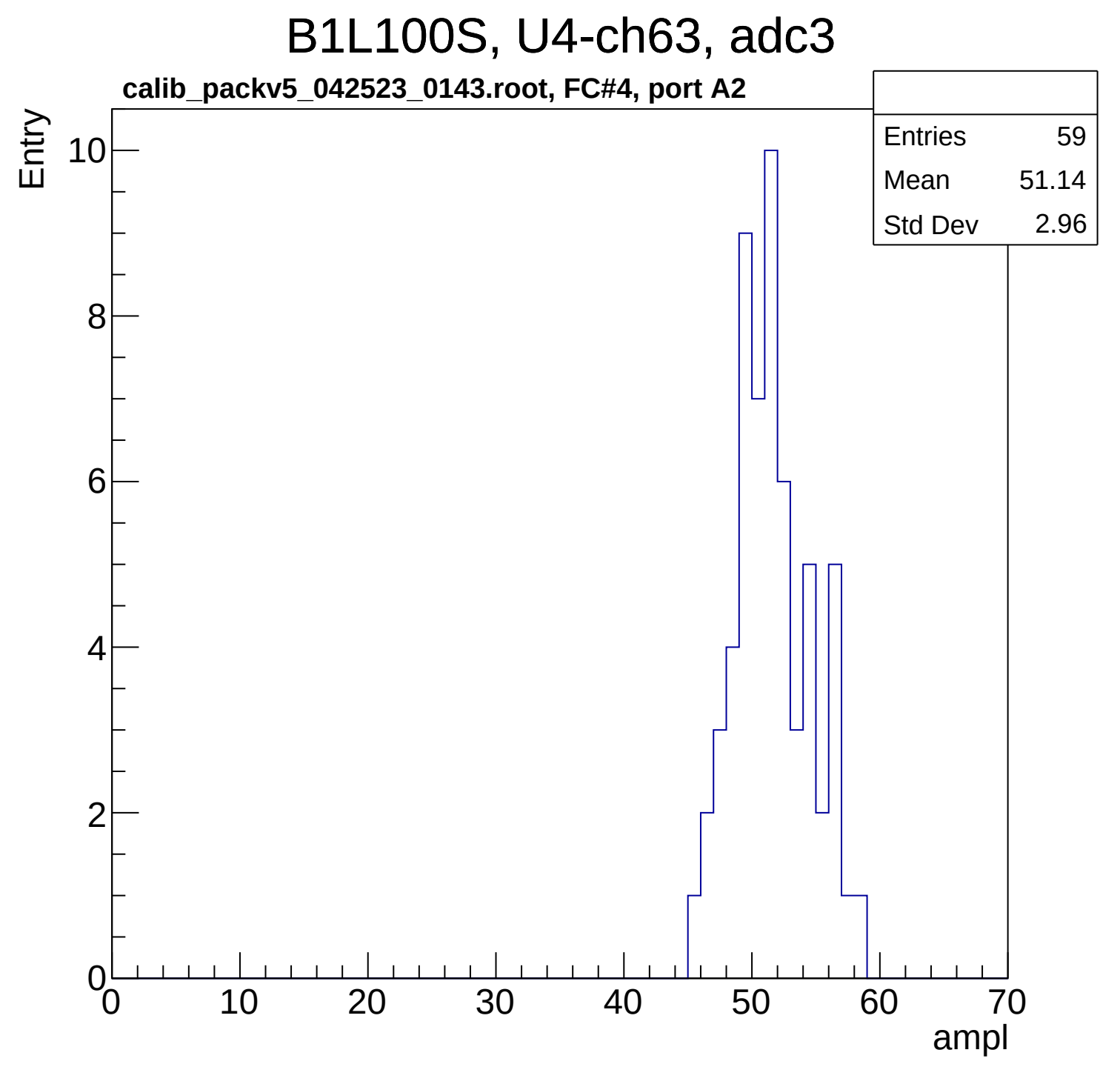

B1L100S, U4-ch62, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 55.82
Std Dev 17.71
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

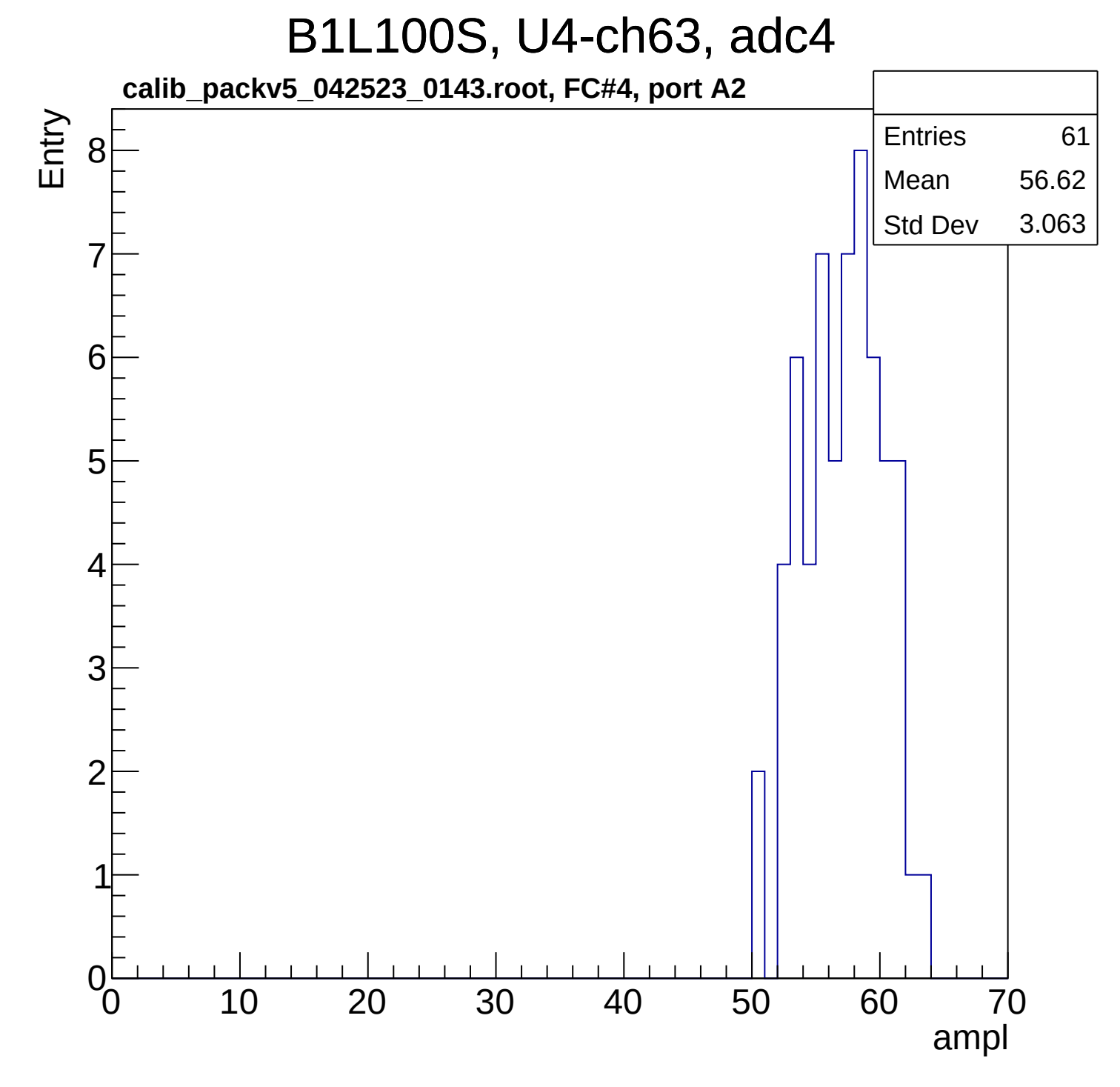

B1L100S, U4-ch62, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

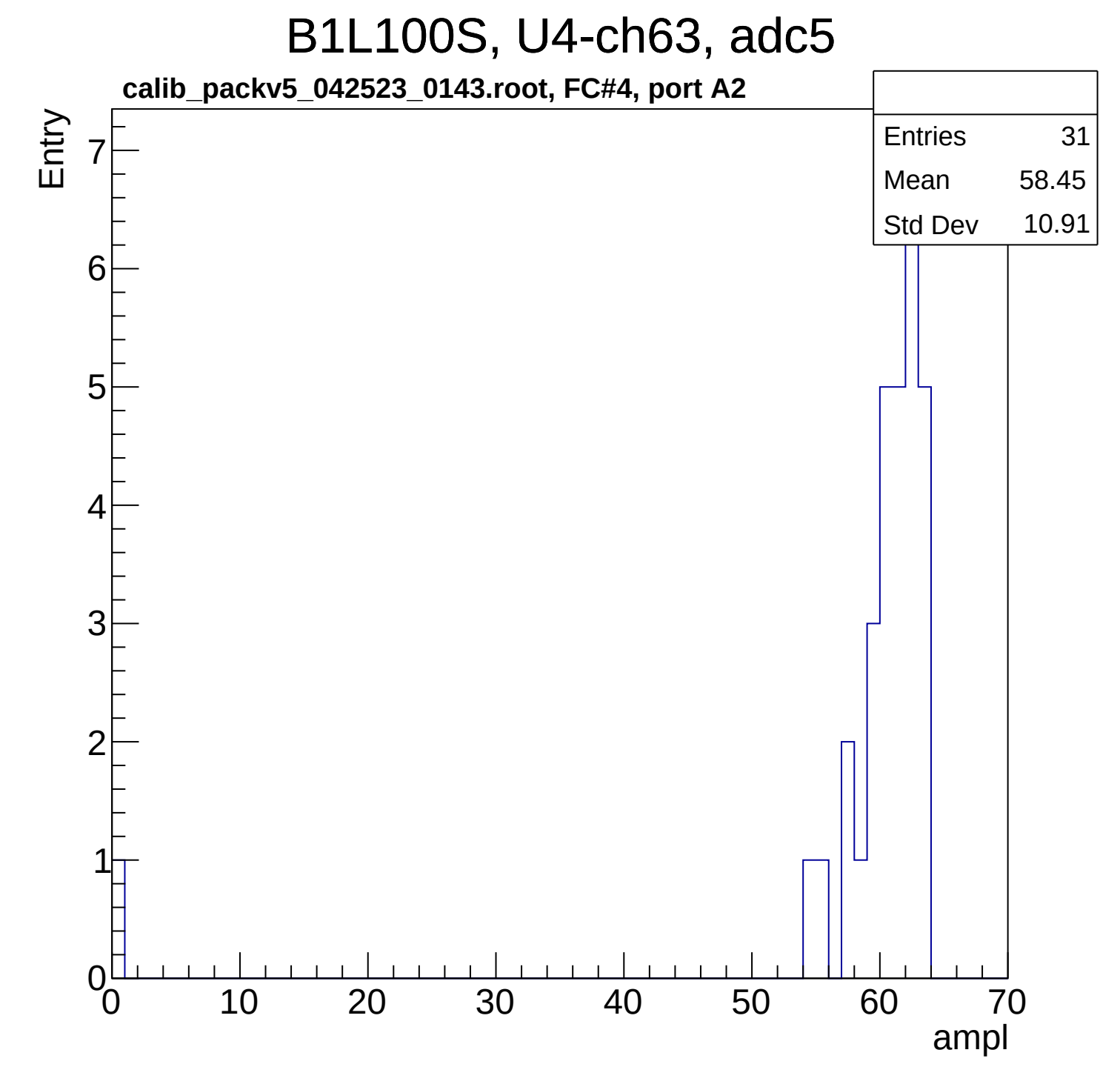

B1L100S, U4-ch63, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 30.34
Std Dev 5.102
Gaus mean : 31.2143
Gaus Width: 3.9950
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

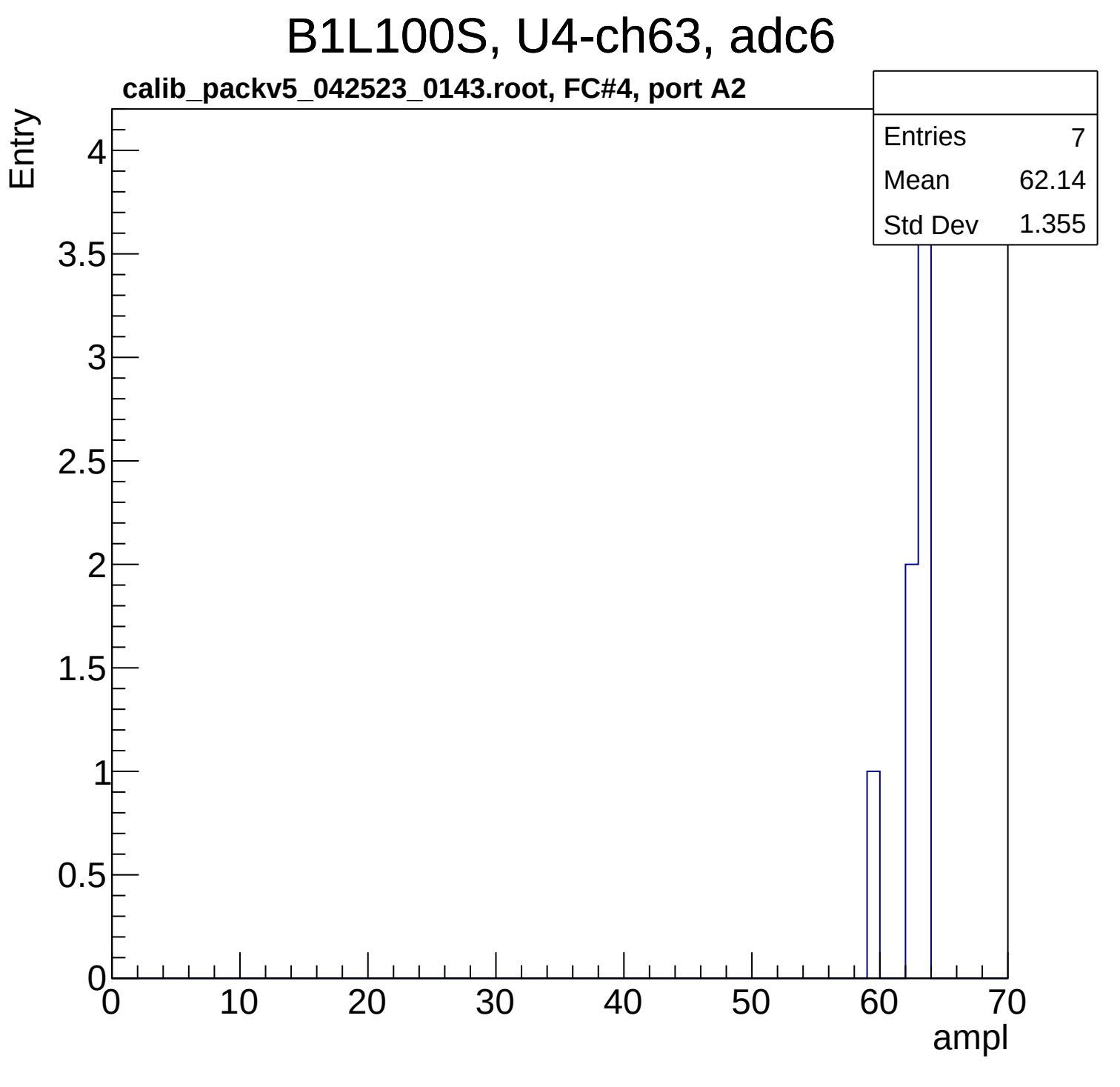

B1L100S, U4-ch63, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 37.44
Std Dev 5.94
Gaus mean : 38.1636
Gaus Width: 3.3349
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

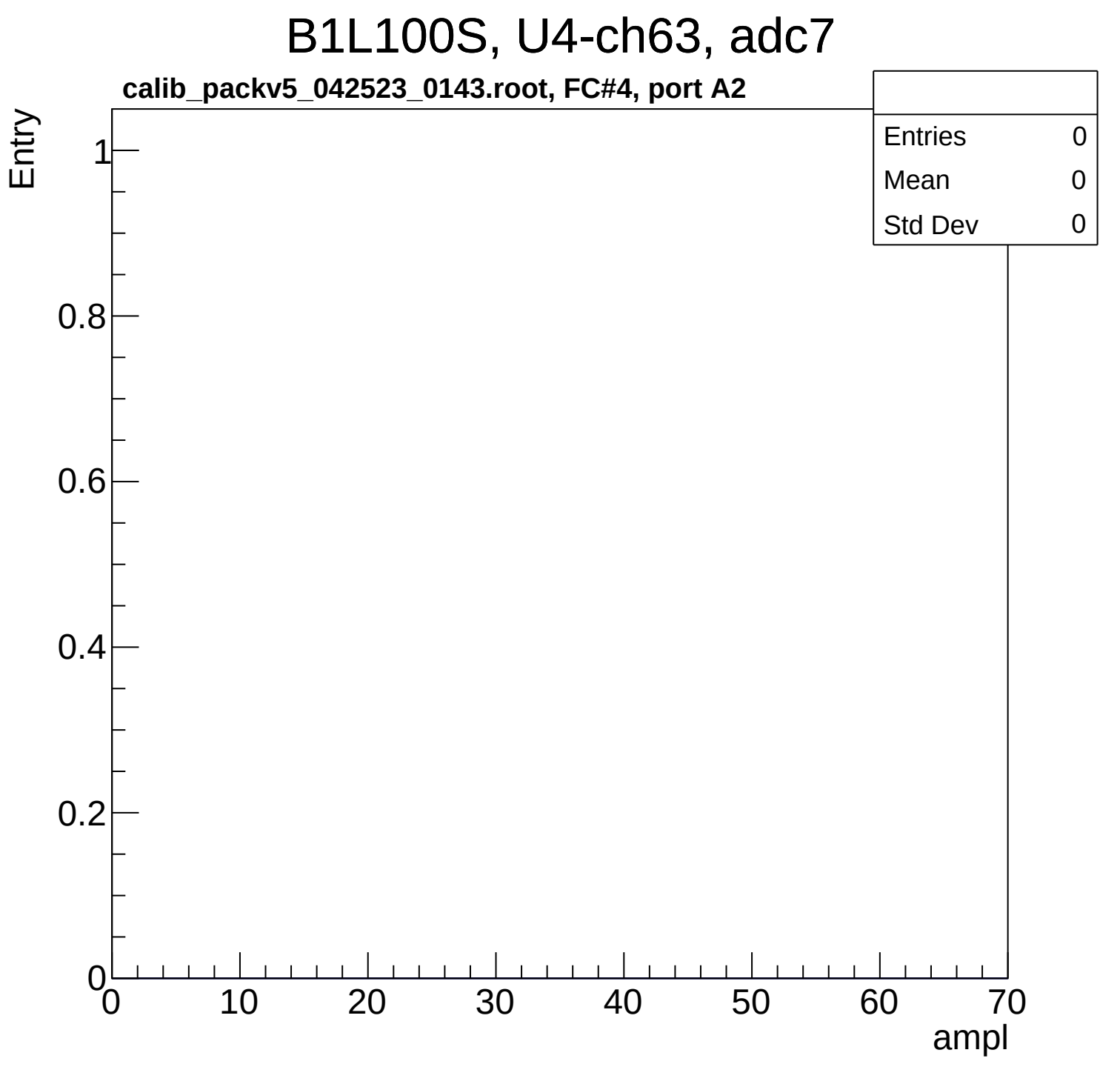

B1L100S, U4-ch63, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 43.66
Std Dev 3.596
Gaus mean : 44.3237
Gaus Width: 3.2028
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

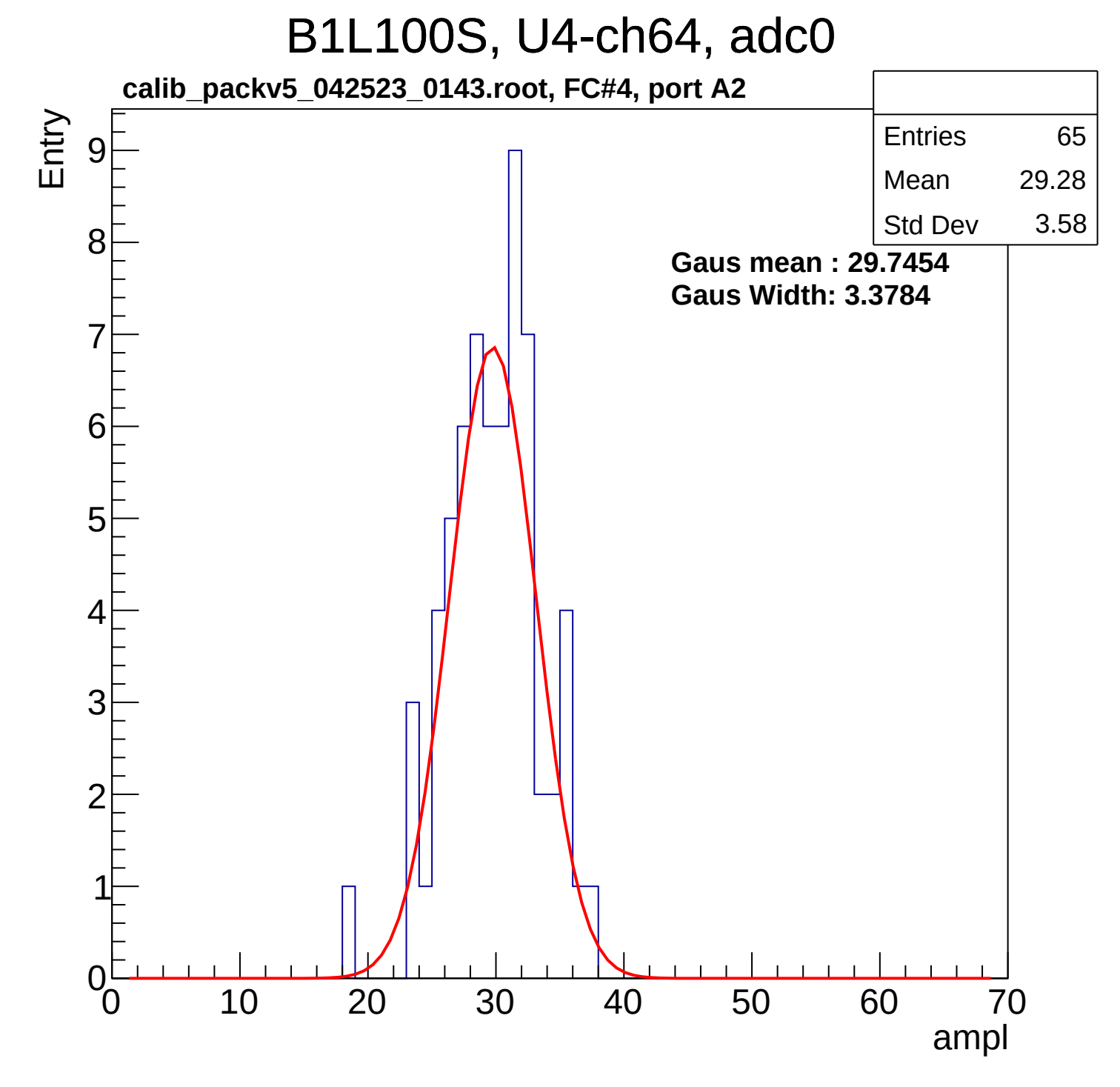

B1L100S, U4-ch63, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 51.14
Std Dev 2.96
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

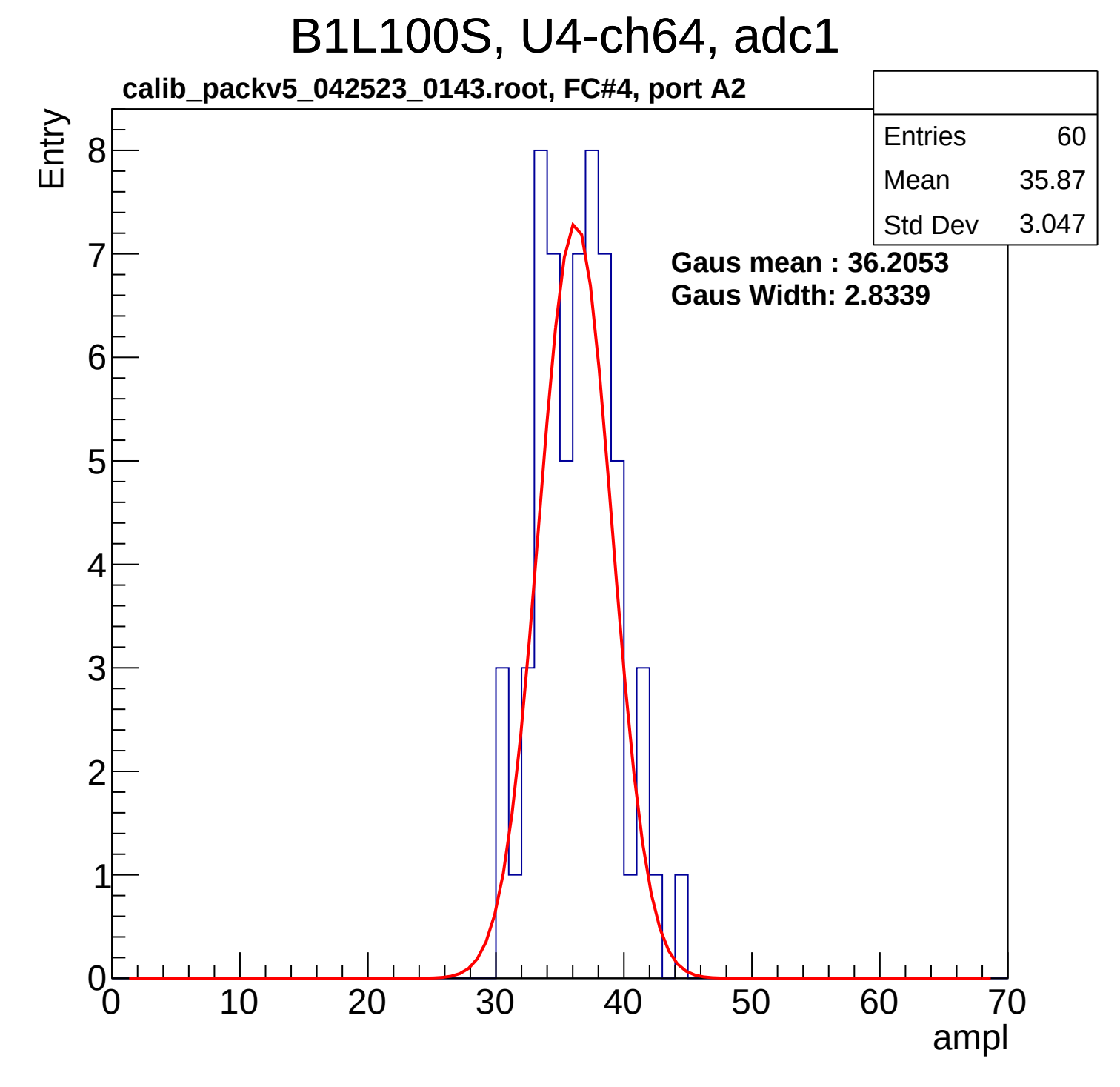

B1L100S, U4-ch63, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 56.62
Std Dev 3.063
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

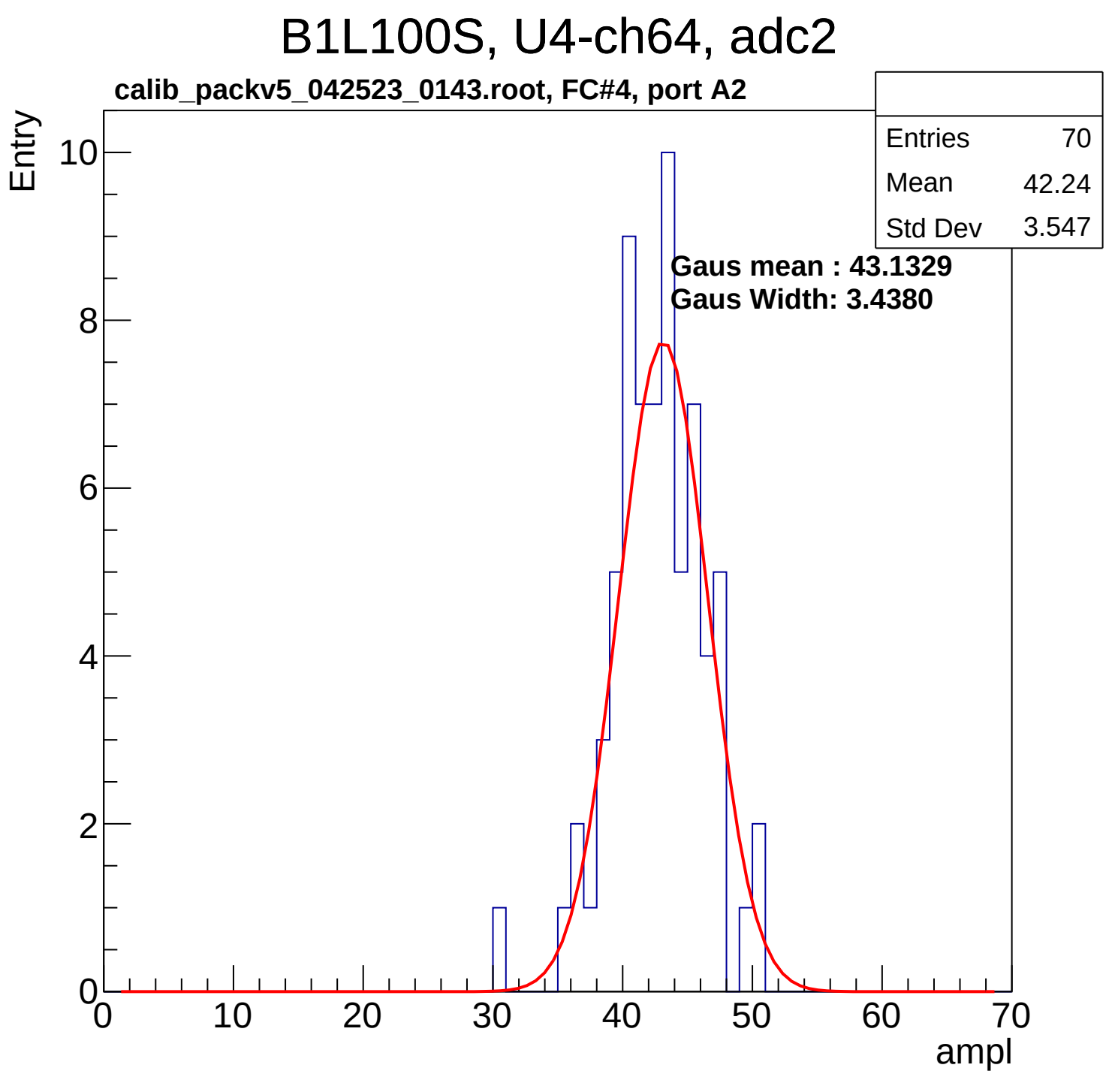

B1L100S, U4-ch63, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 31
Mean 58.45
Std Dev 10.91
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

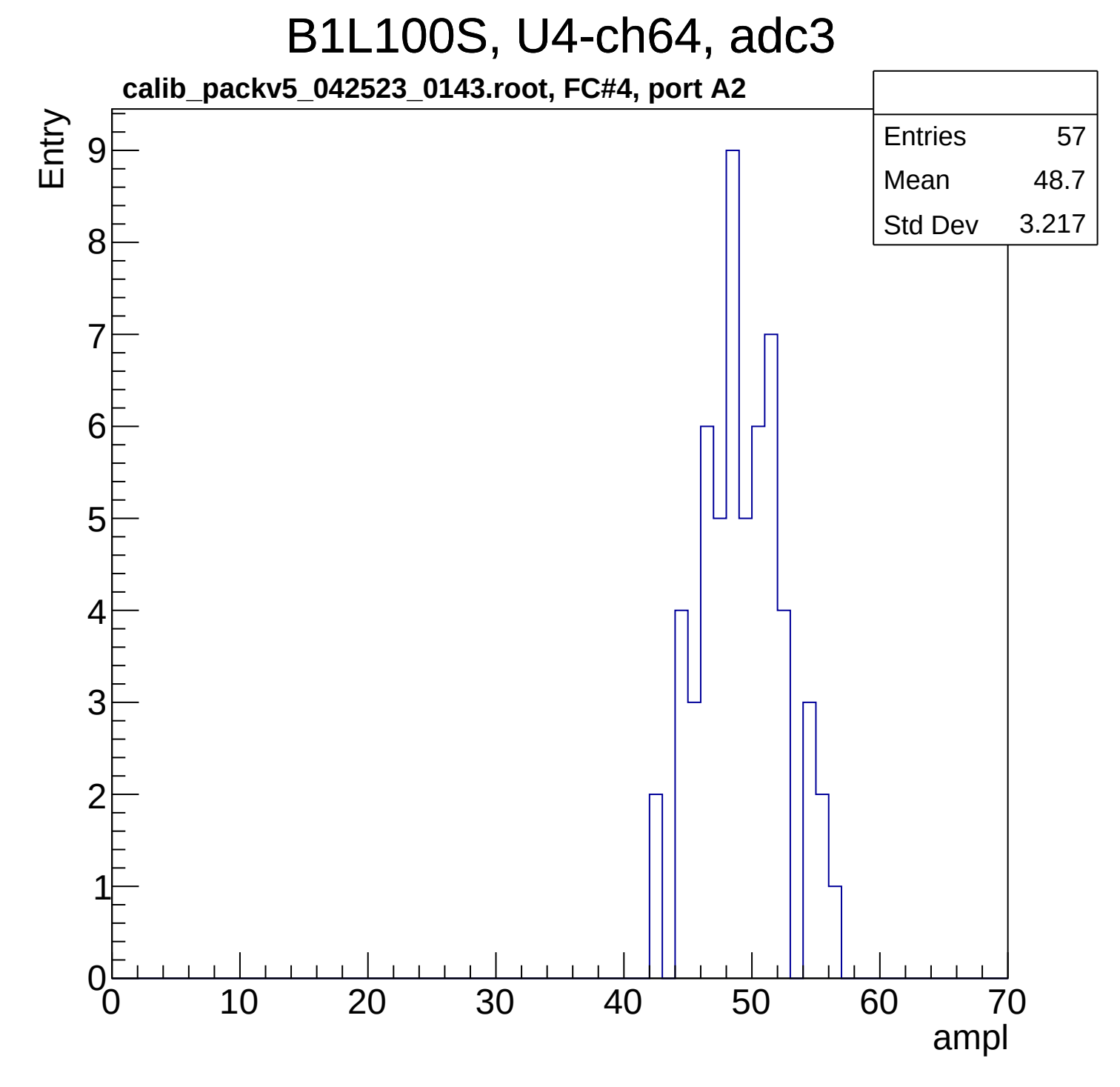

B1L100S, U4-ch63, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 62.14
Std Dev 1.355
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

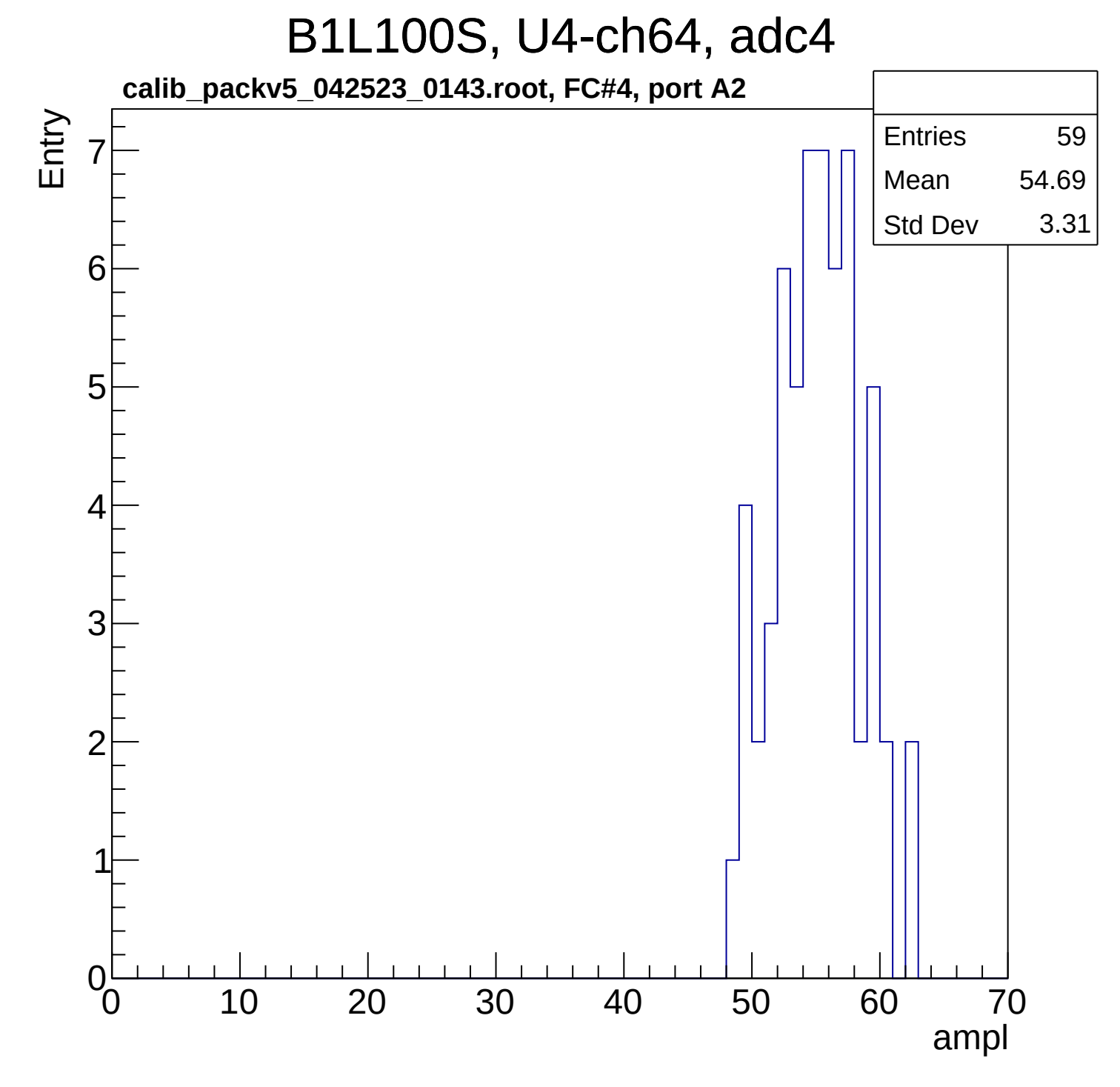

B1L100S, U4-ch63, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

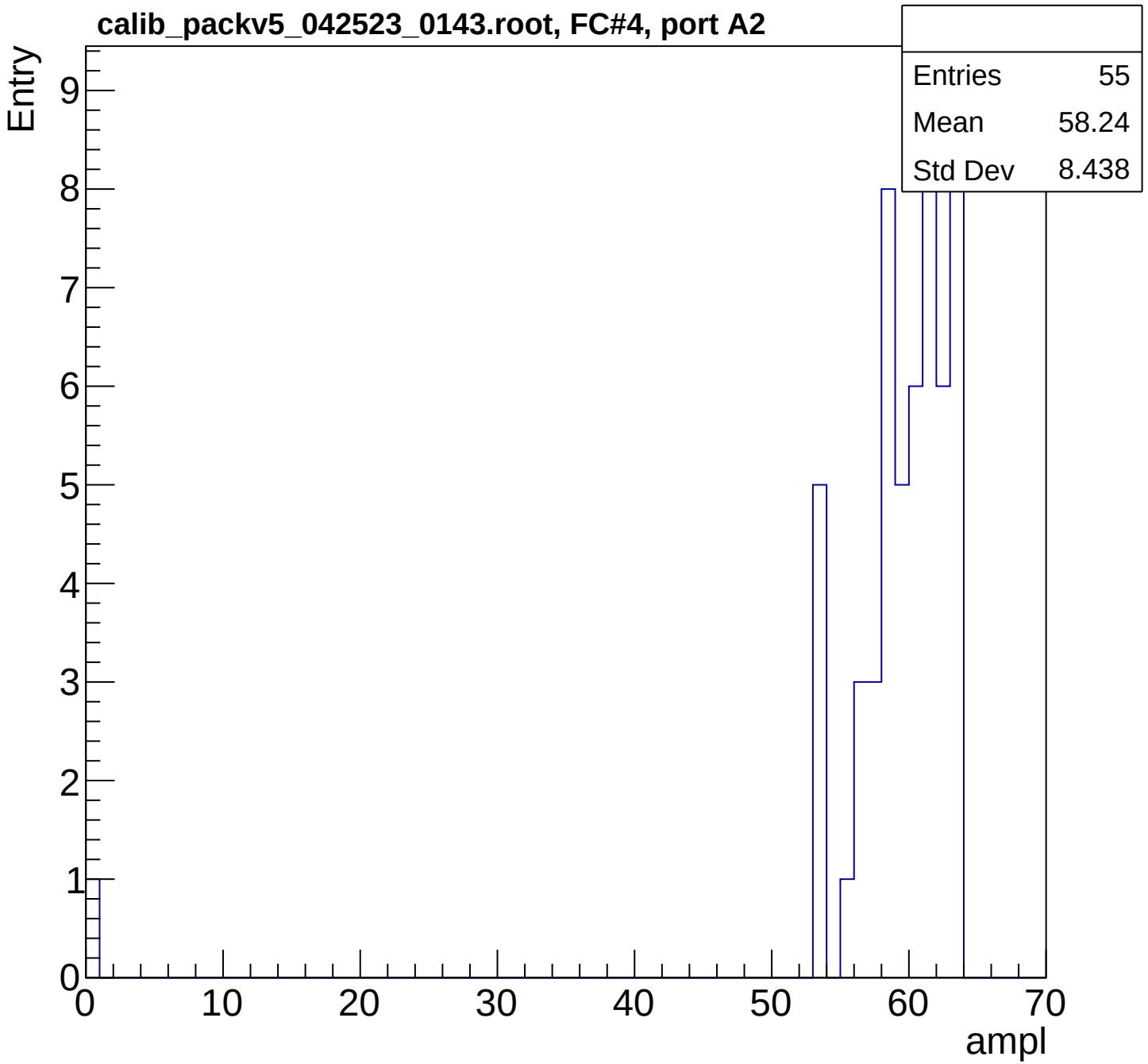

B1L100S, U4-ch64, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 29.28
Std Dev 3.58
Gaus mean : 29.7454
Gaus Width: 3.3784
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

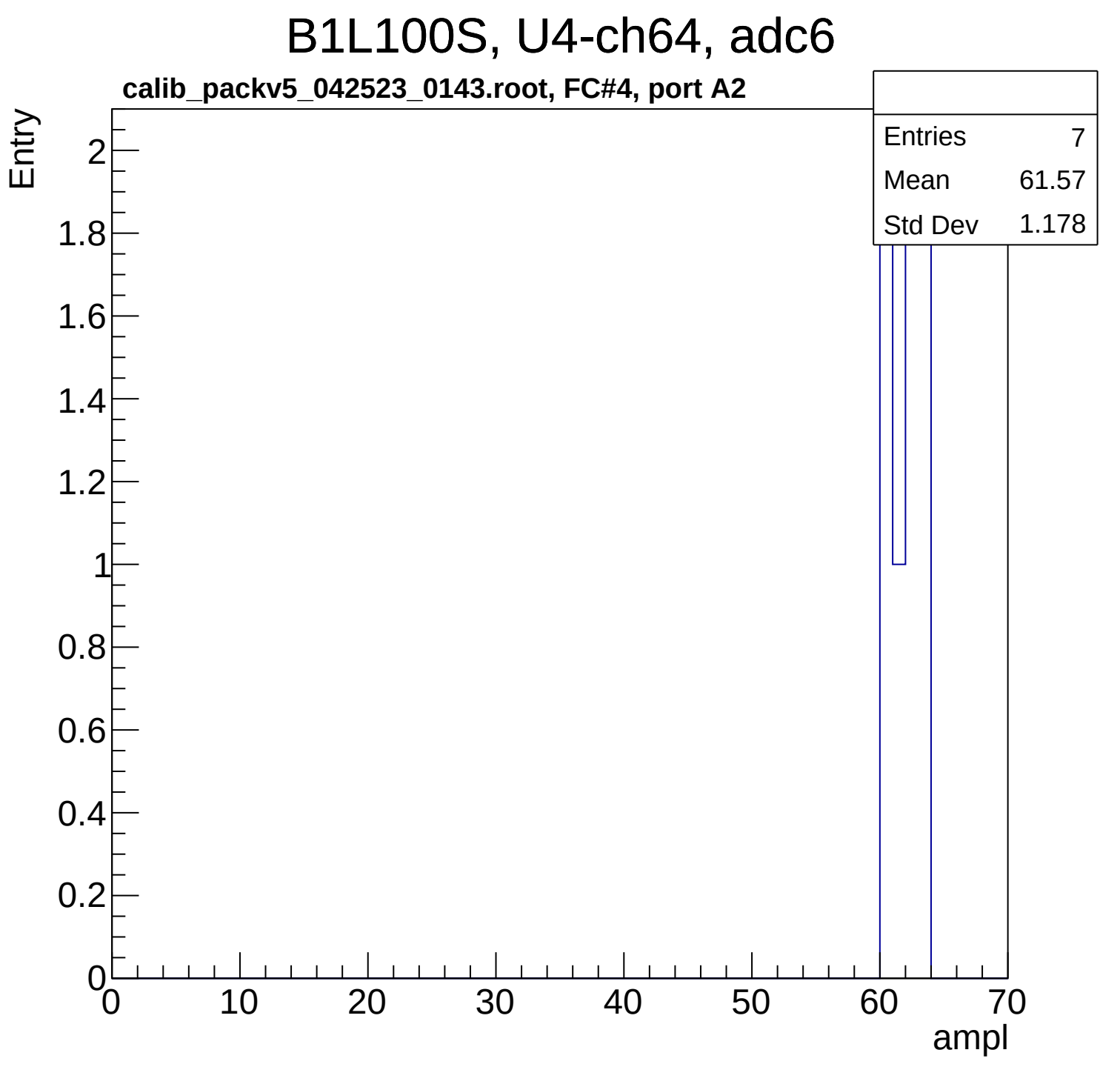

B1L100S, U4-ch64, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 35.87
Std Dev 3.047
Gaus mean : 36.2053
Gaus Width: 2.8339
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

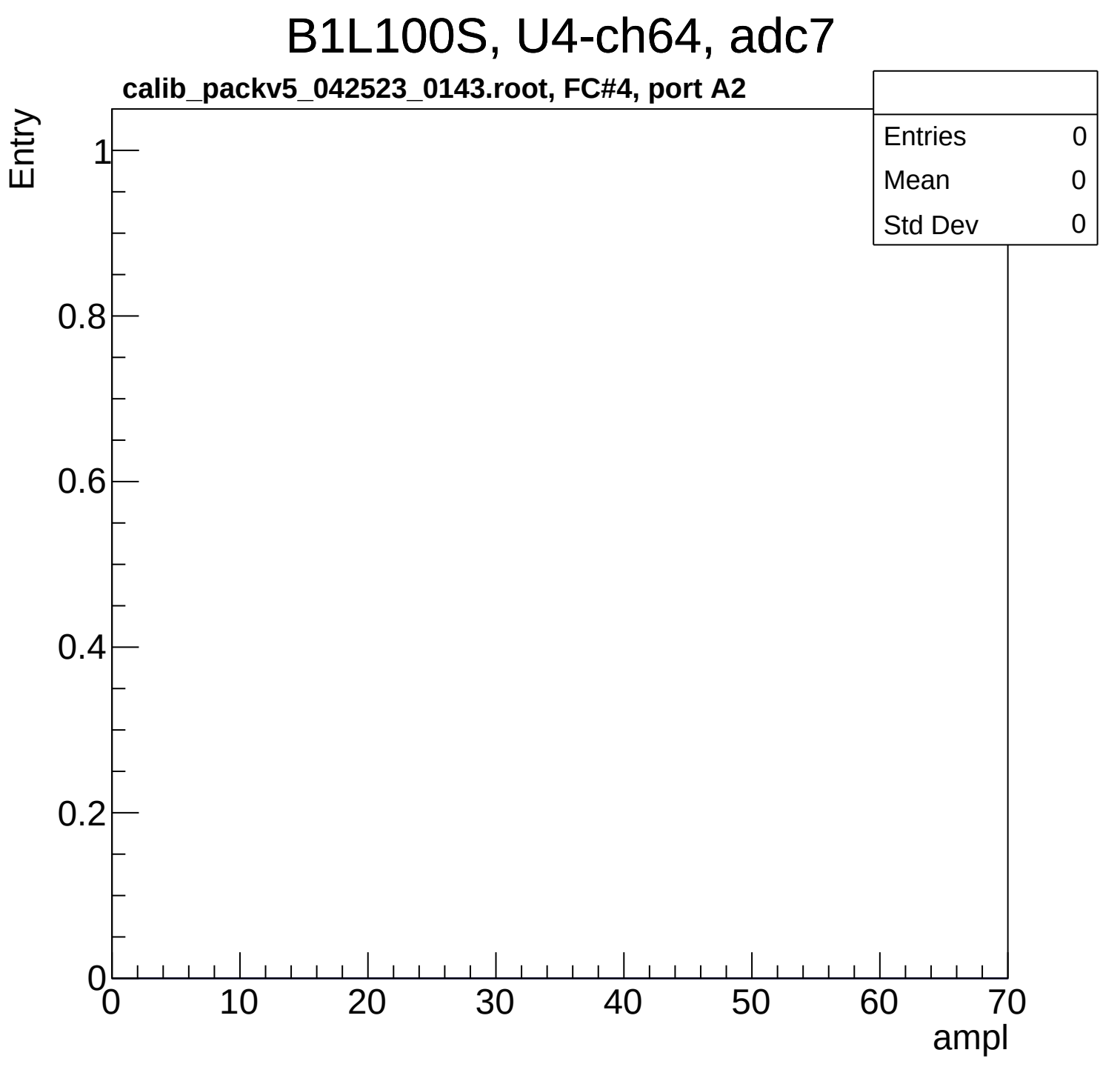

B1L100S, U4-ch64, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 42.24
Std Dev 3.547
Gaus mean : 43.1329
Gaus Width: 3.4380
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

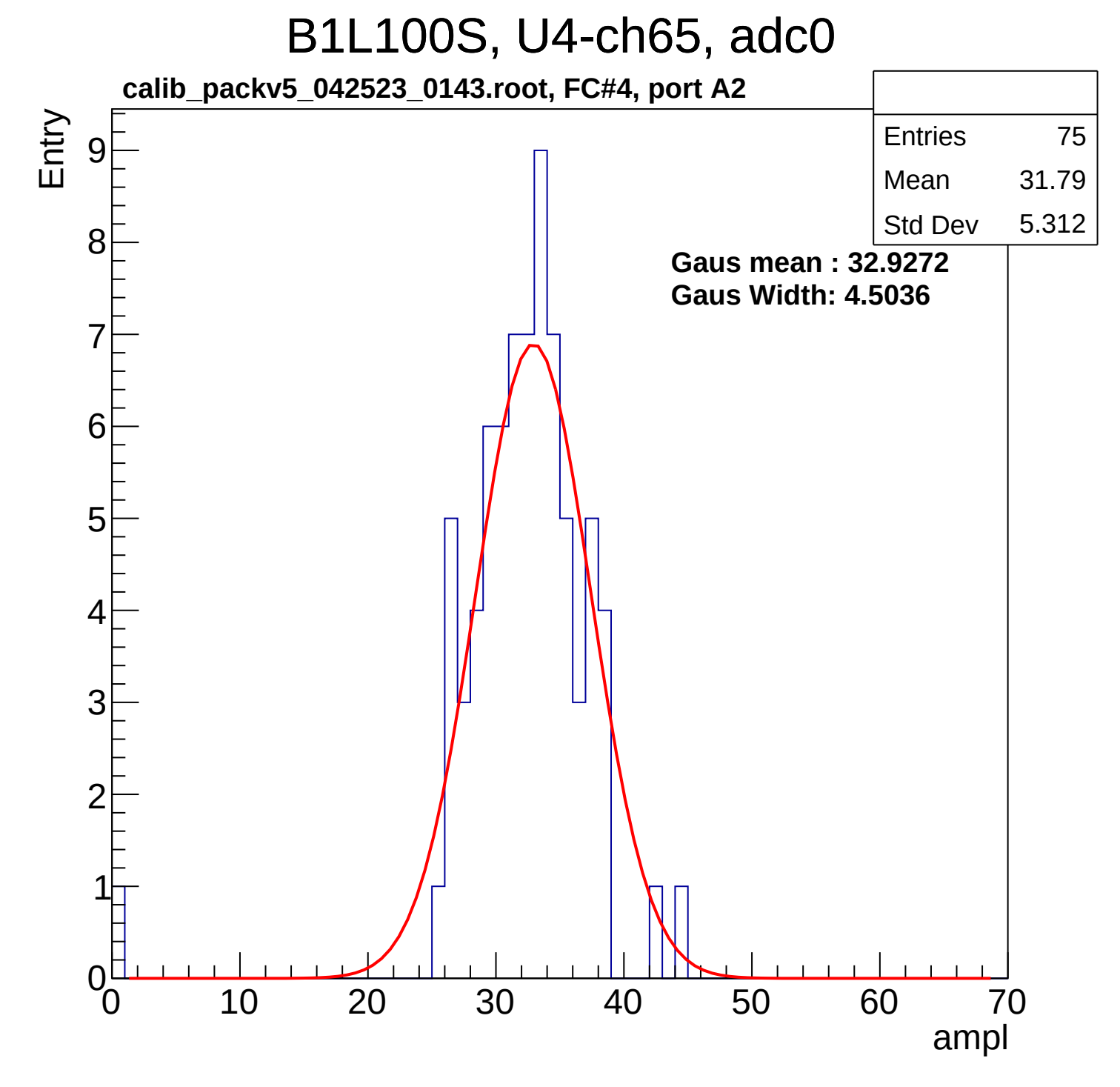

B1L100S, U4-ch64, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 48.7
Std Dev 3.217
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

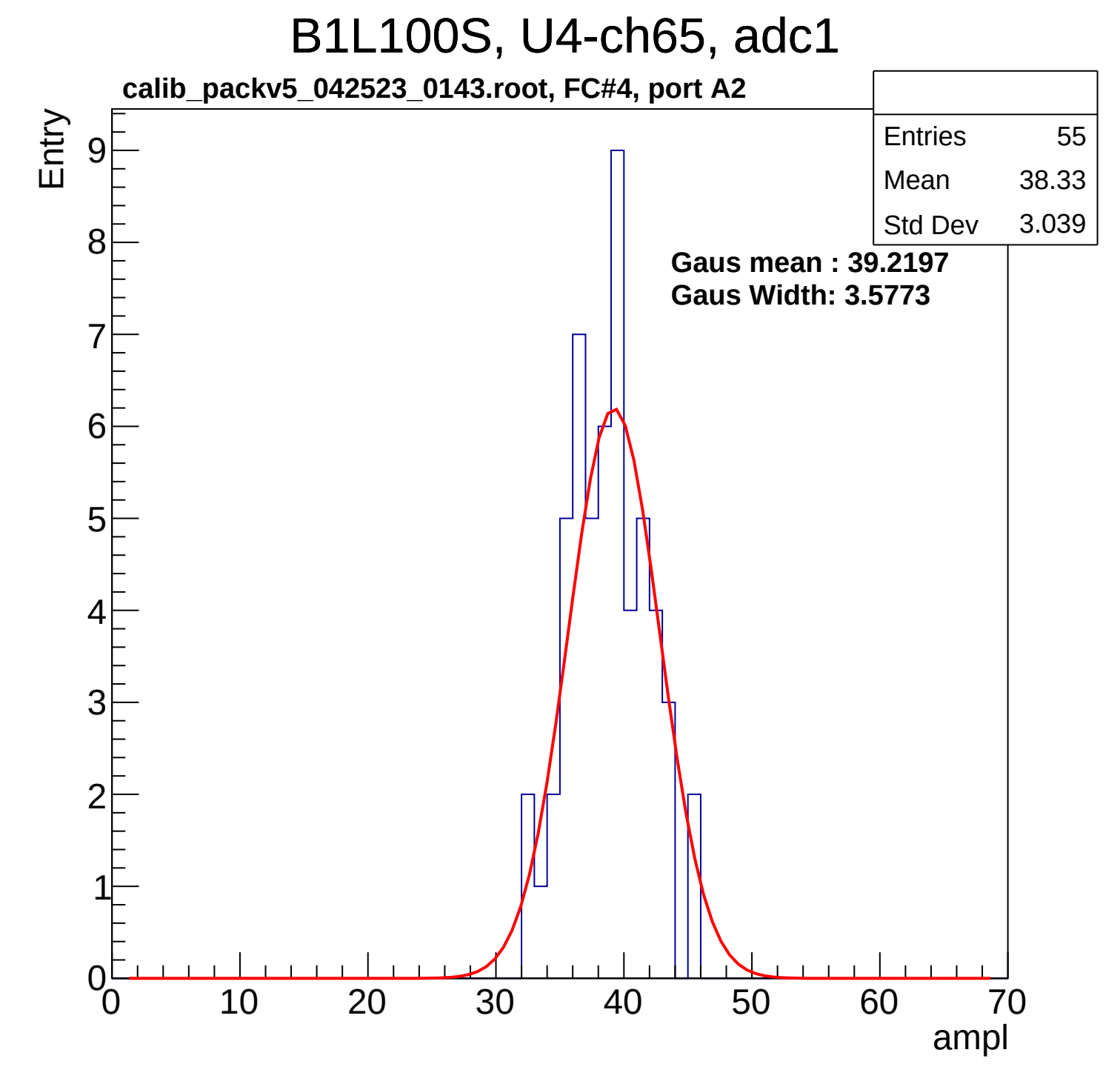

B1L100S, U4-ch64, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 54.69
Std Dev 3.31
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

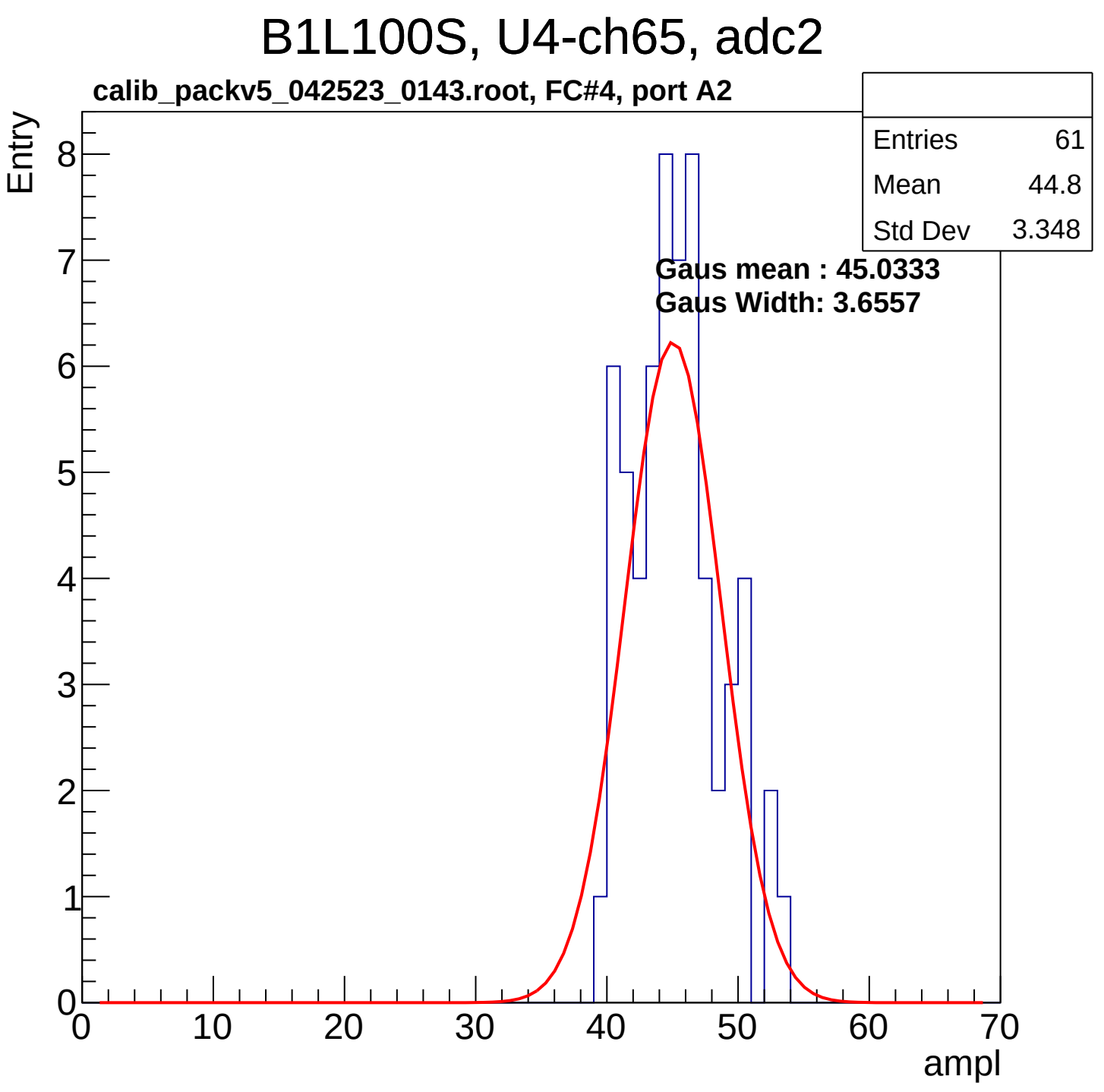

B1L100S, U4-ch64, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 58.24
Std Dev 8.438
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

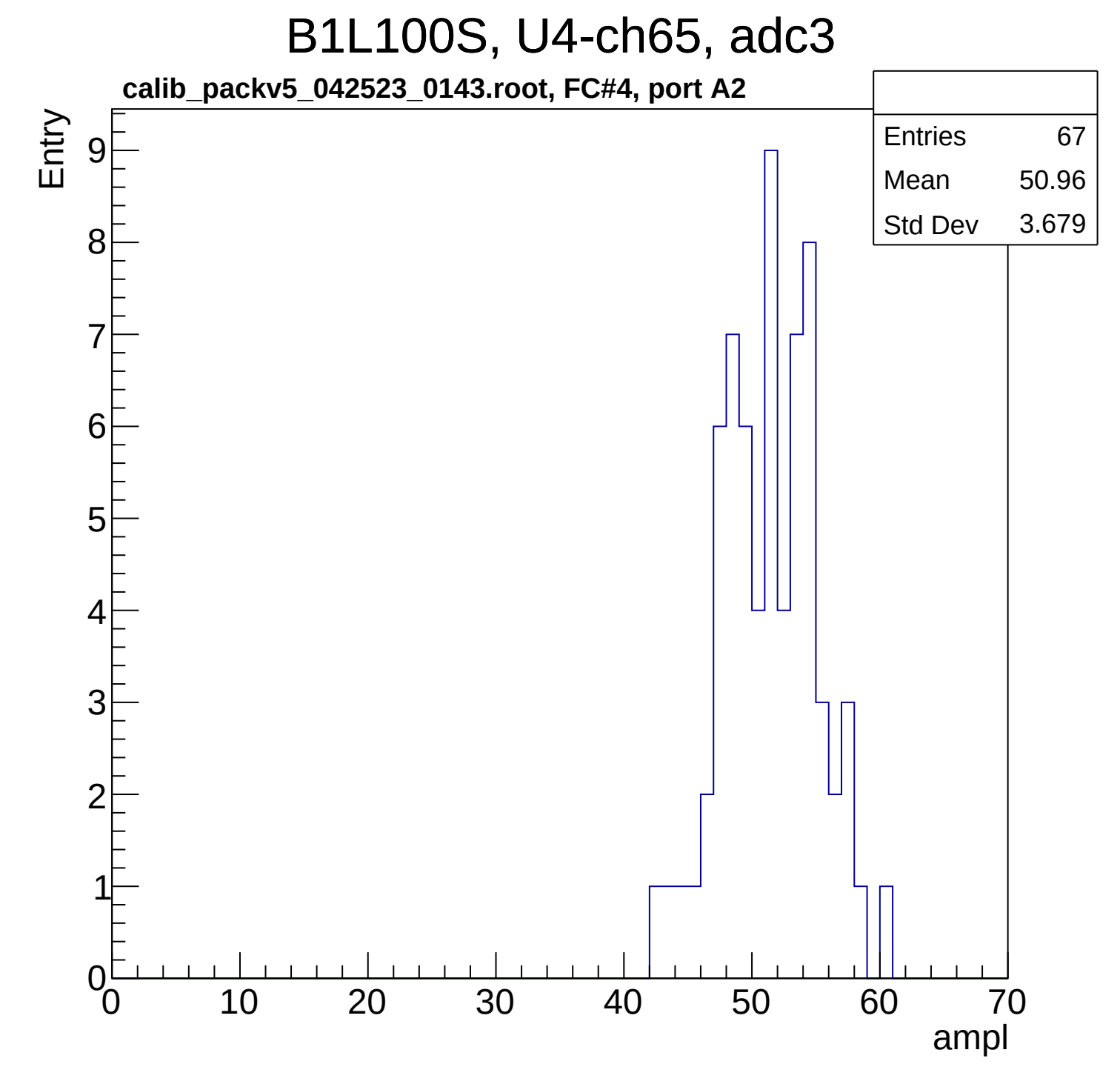

B1L100S, U4-ch64, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 61.57
Std Dev 1.178
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

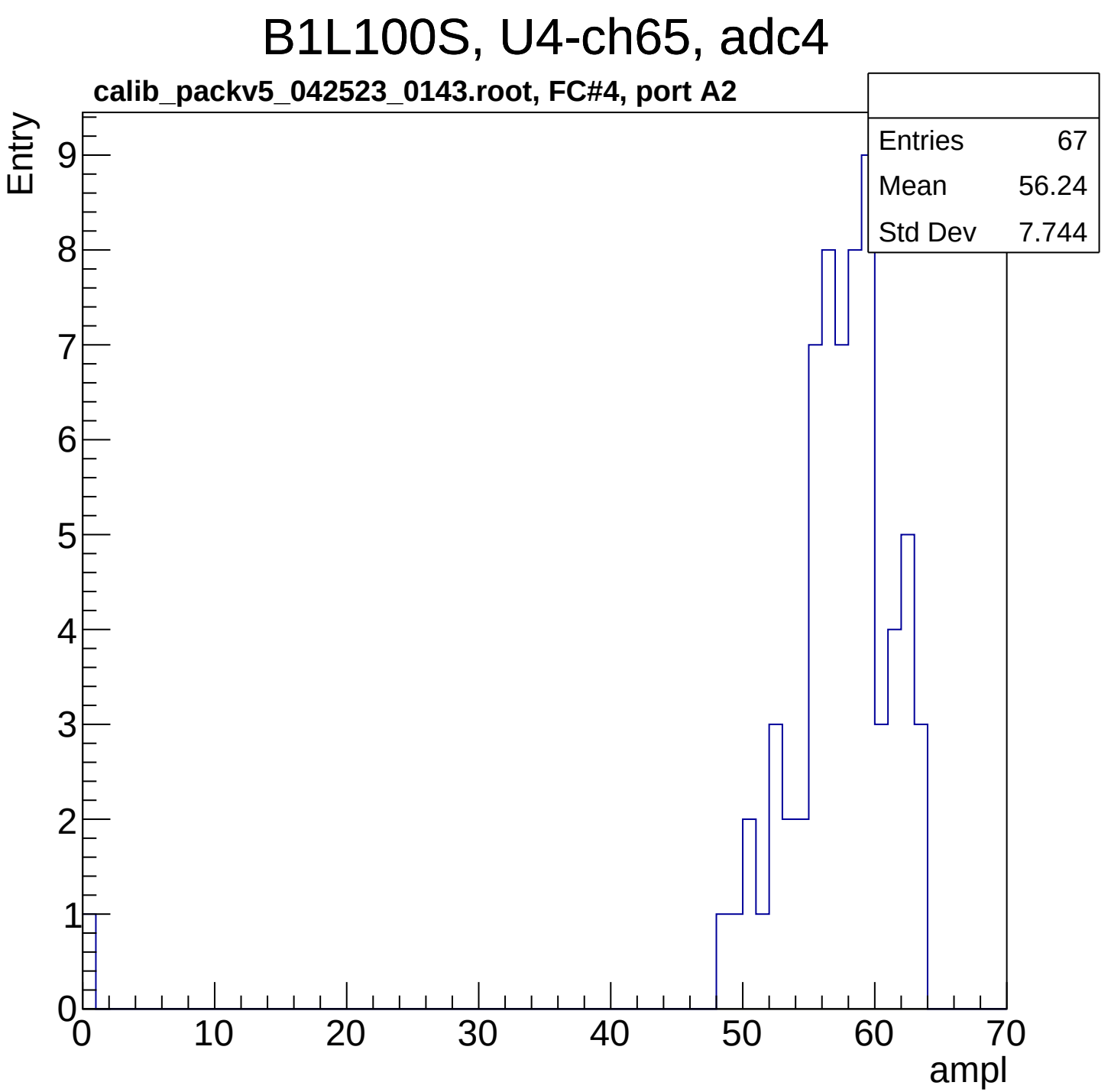

B1L100S, U4-ch64, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

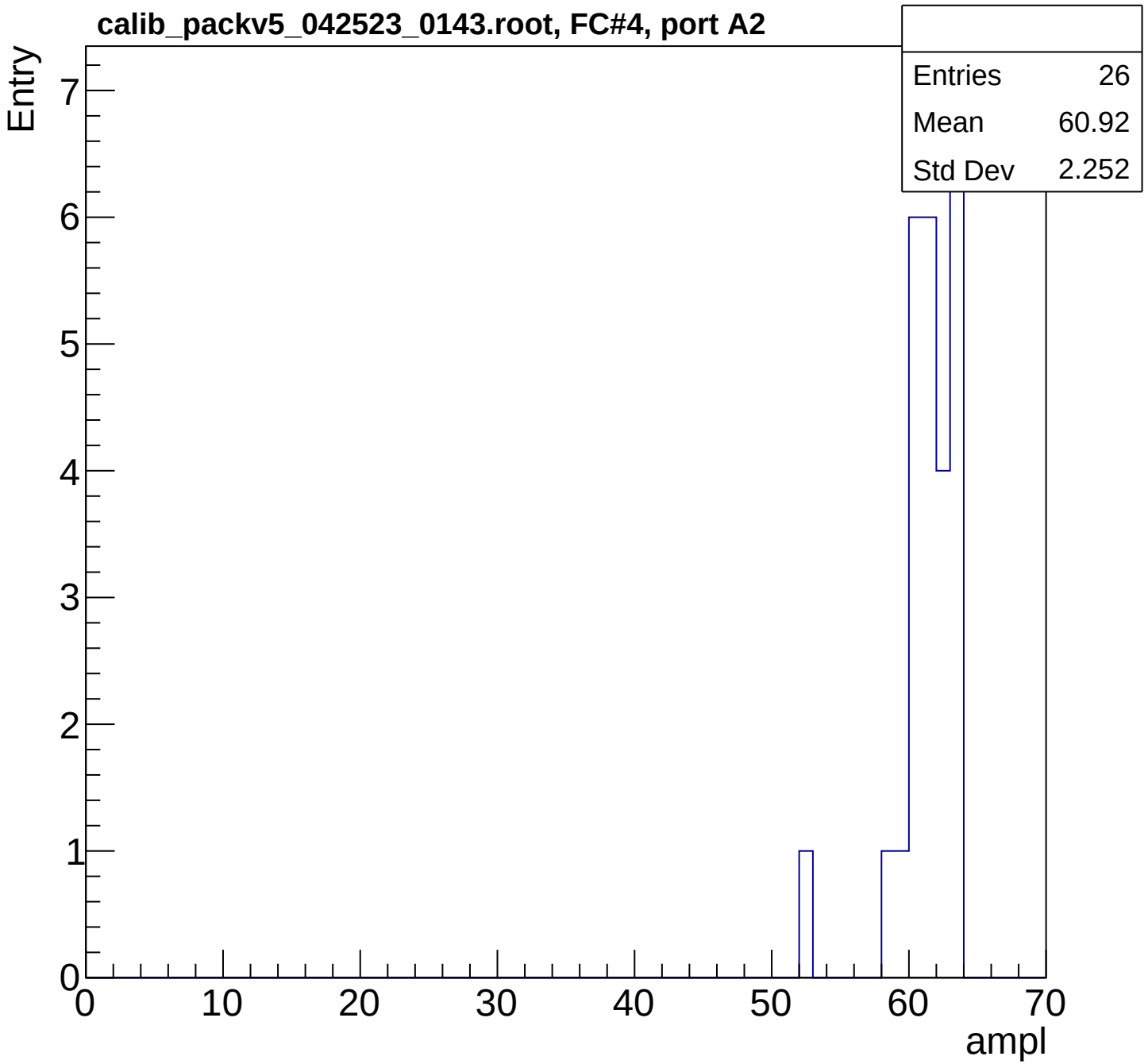

B1L100S, U4-ch65, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 31.79
Std Dev 5.312
Gaus mean : 32.9272
Gaus Width: 4.5036
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

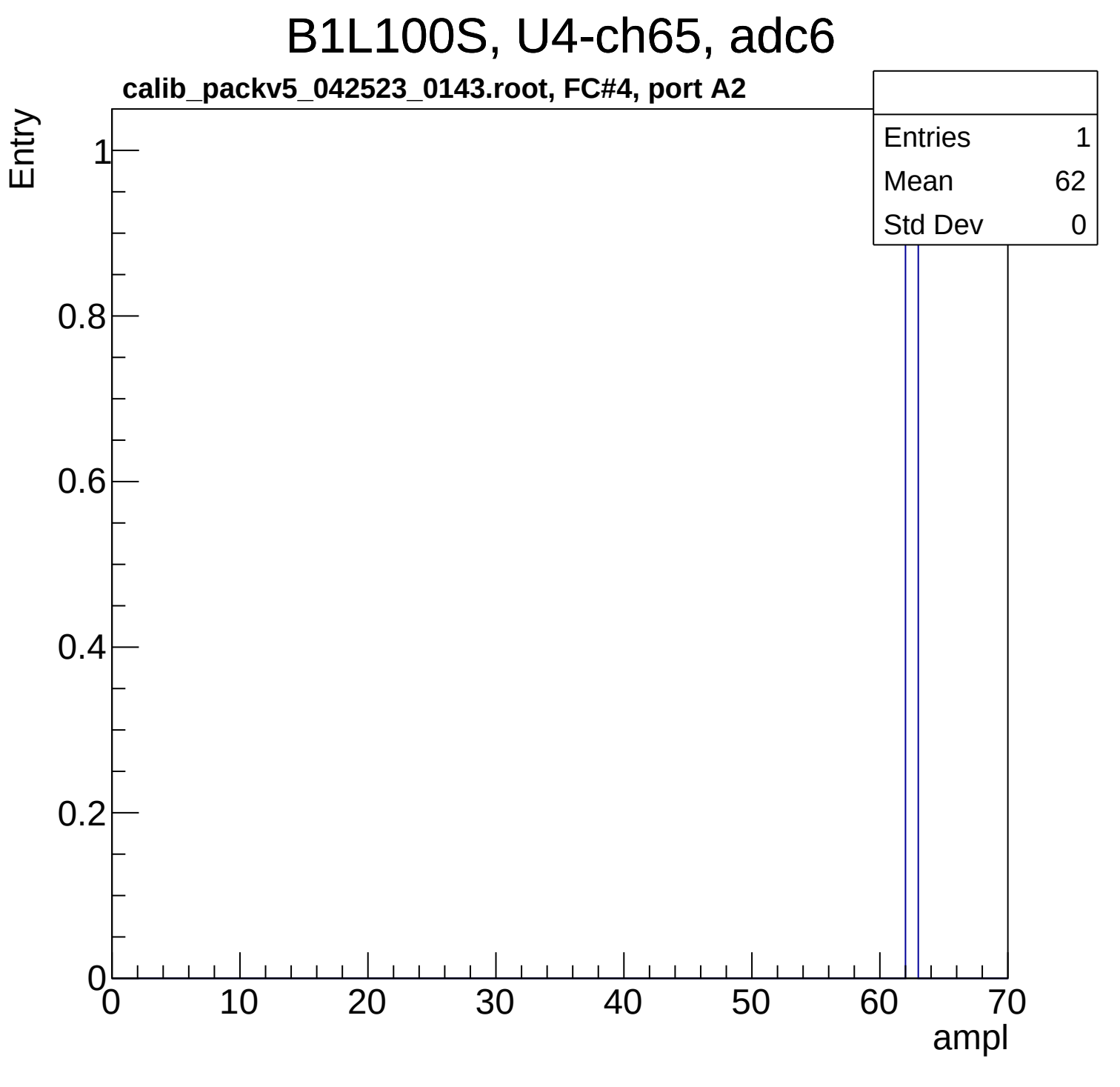

B1L100S, U4-ch65, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 38.33
Std Dev 3.039
Gaus mean : 39.2197
Gaus Width: 3.5773
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

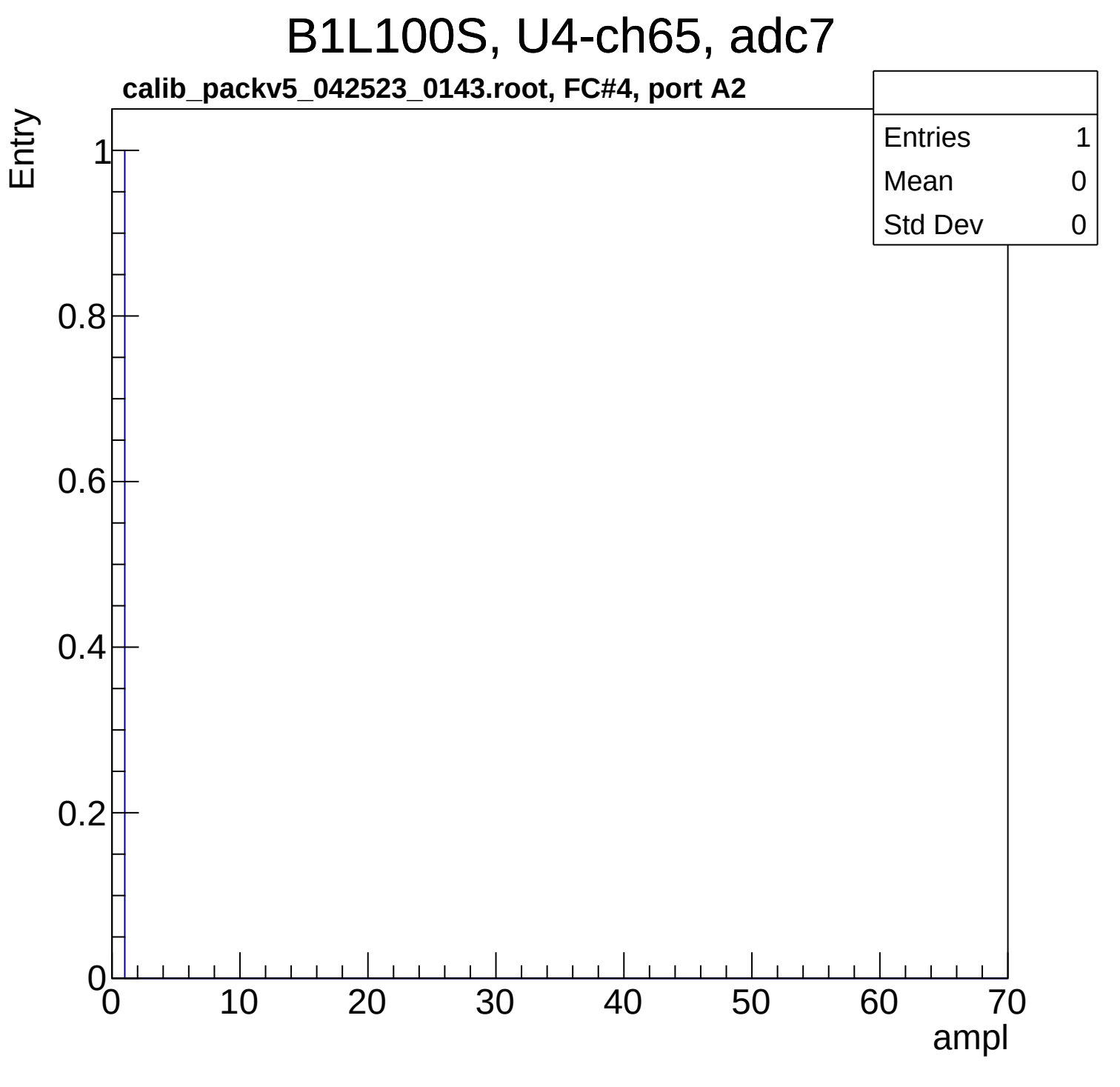

B1L100S, U4-ch65, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 44.8
Std Dev 3.348
Gaus mean : 45.0333
Gaus Width: 3.6557
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

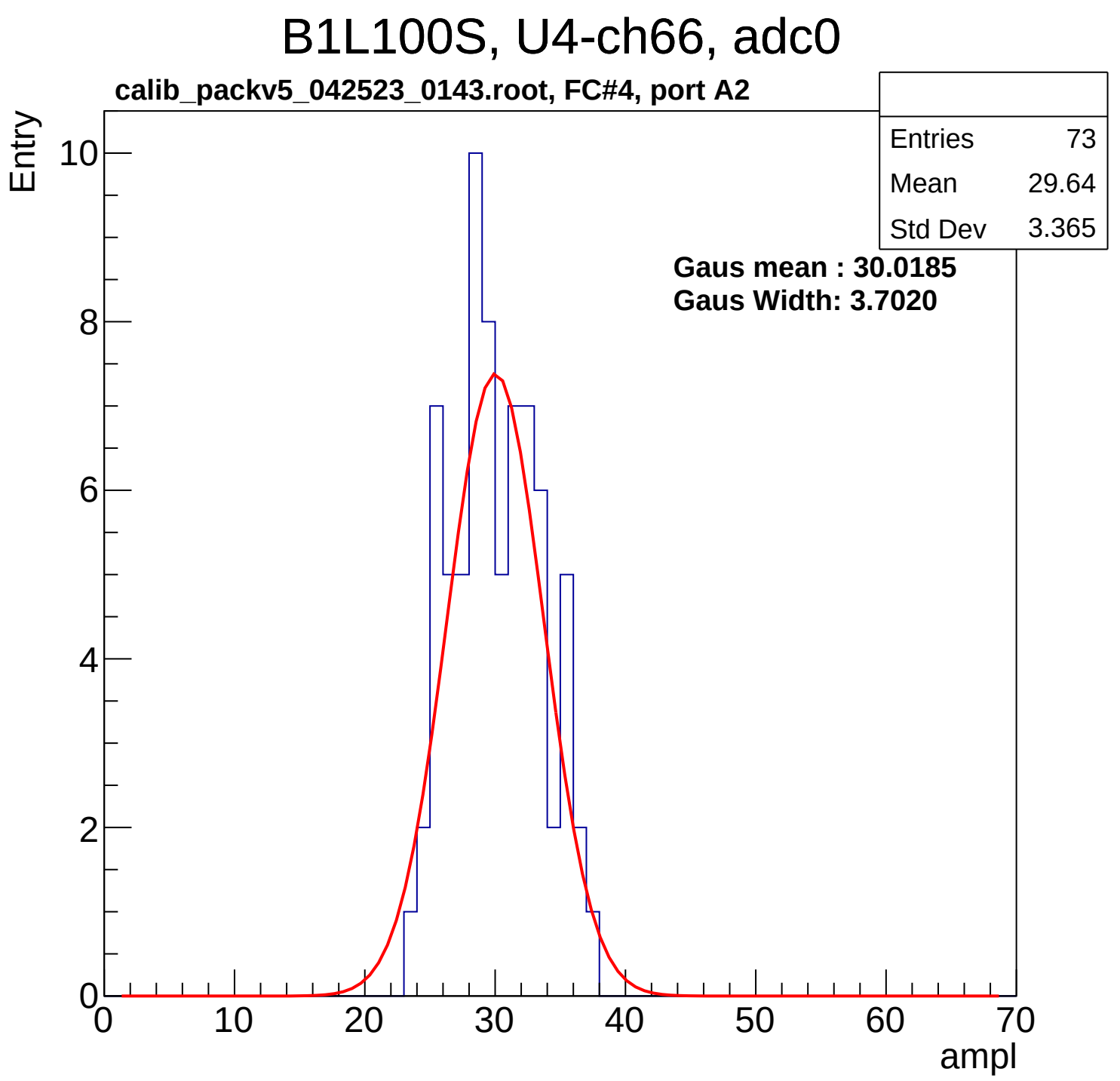

B1L100S, U4-ch65, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 50.96
Std Dev 3.679
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

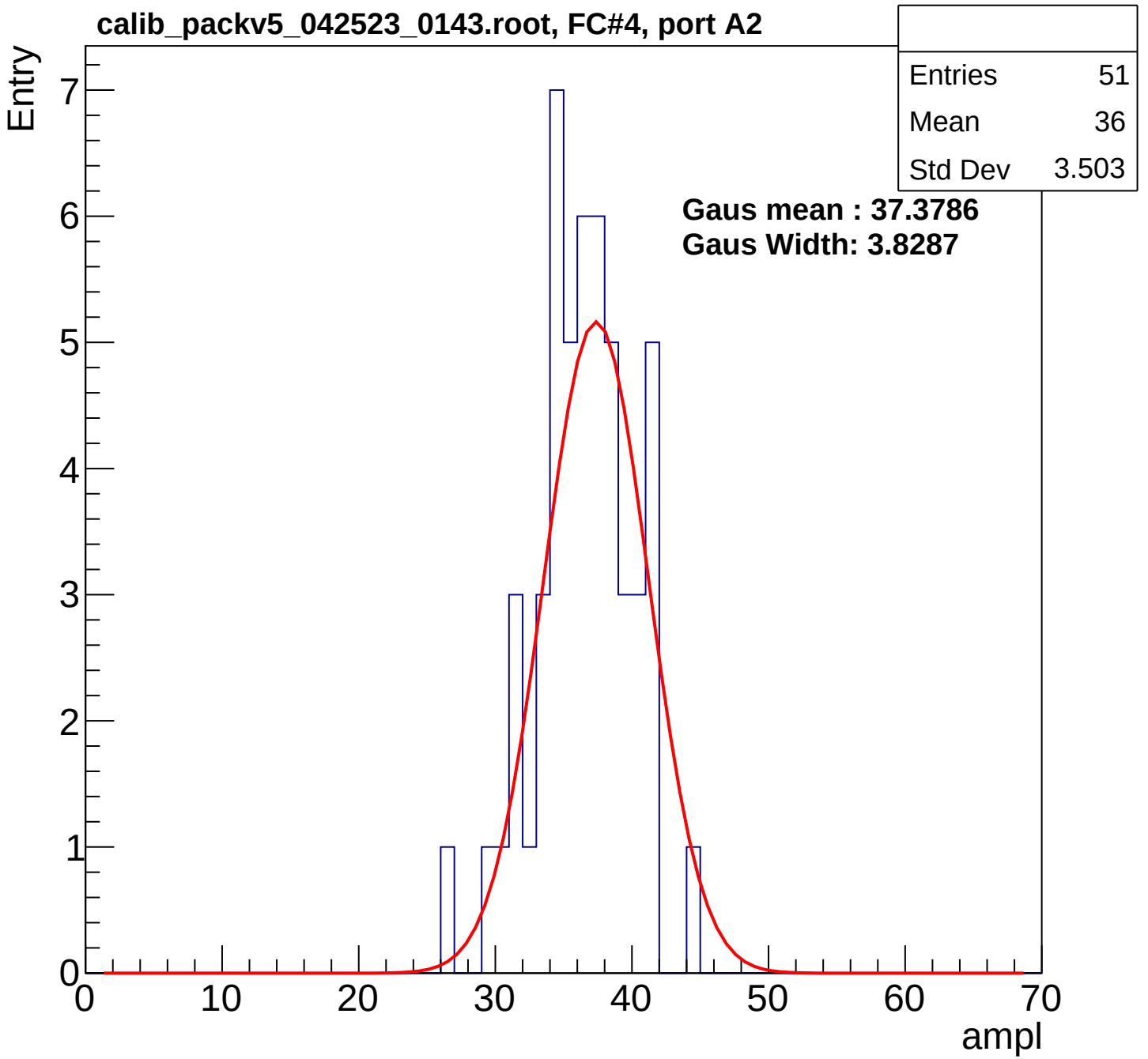

B1L100S, U4-ch65, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 56.24
Std Dev 7.744
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

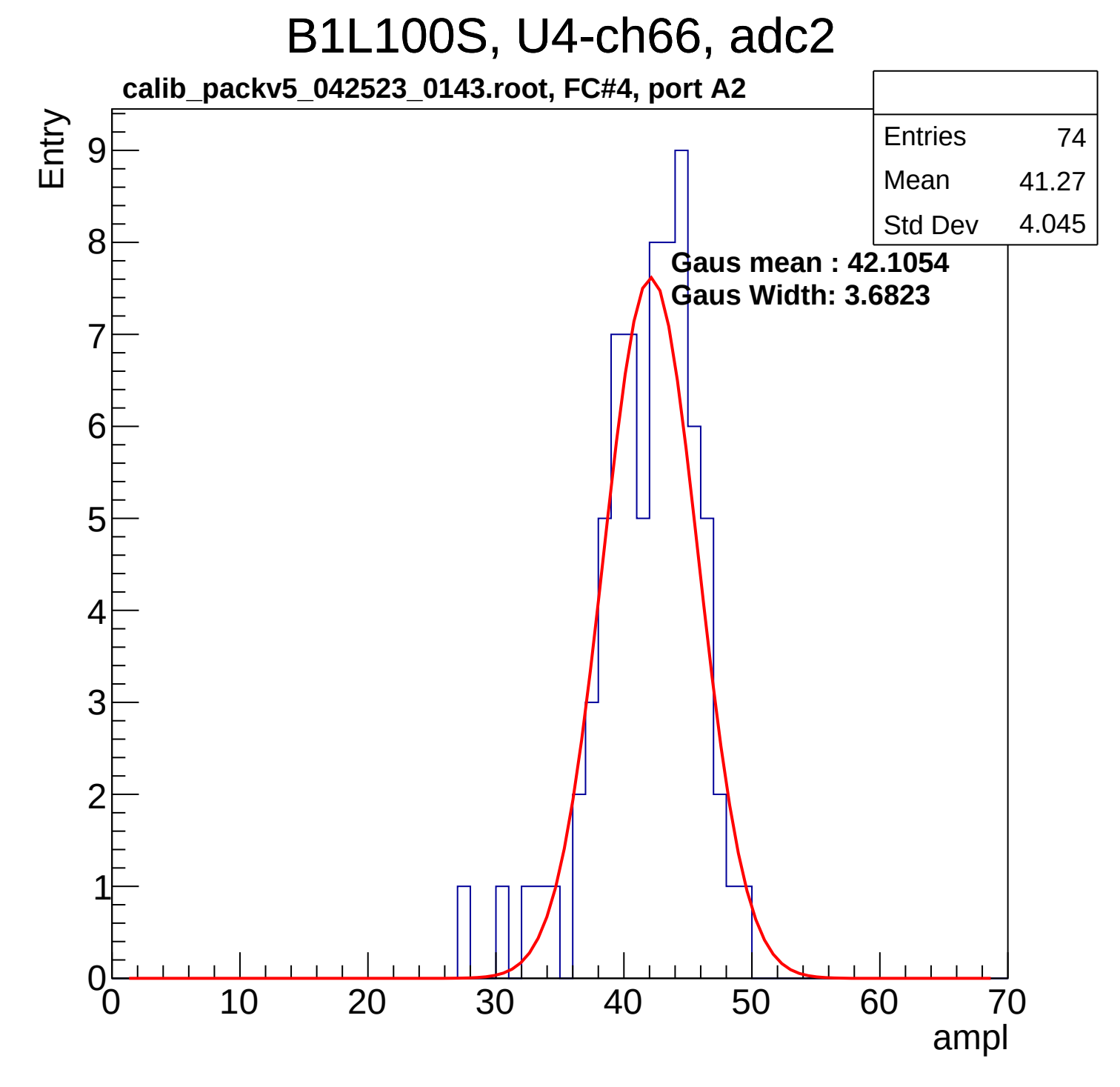

B1L100S, U4-ch65, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 26
Mean 60.92
Std Dev 2.252
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

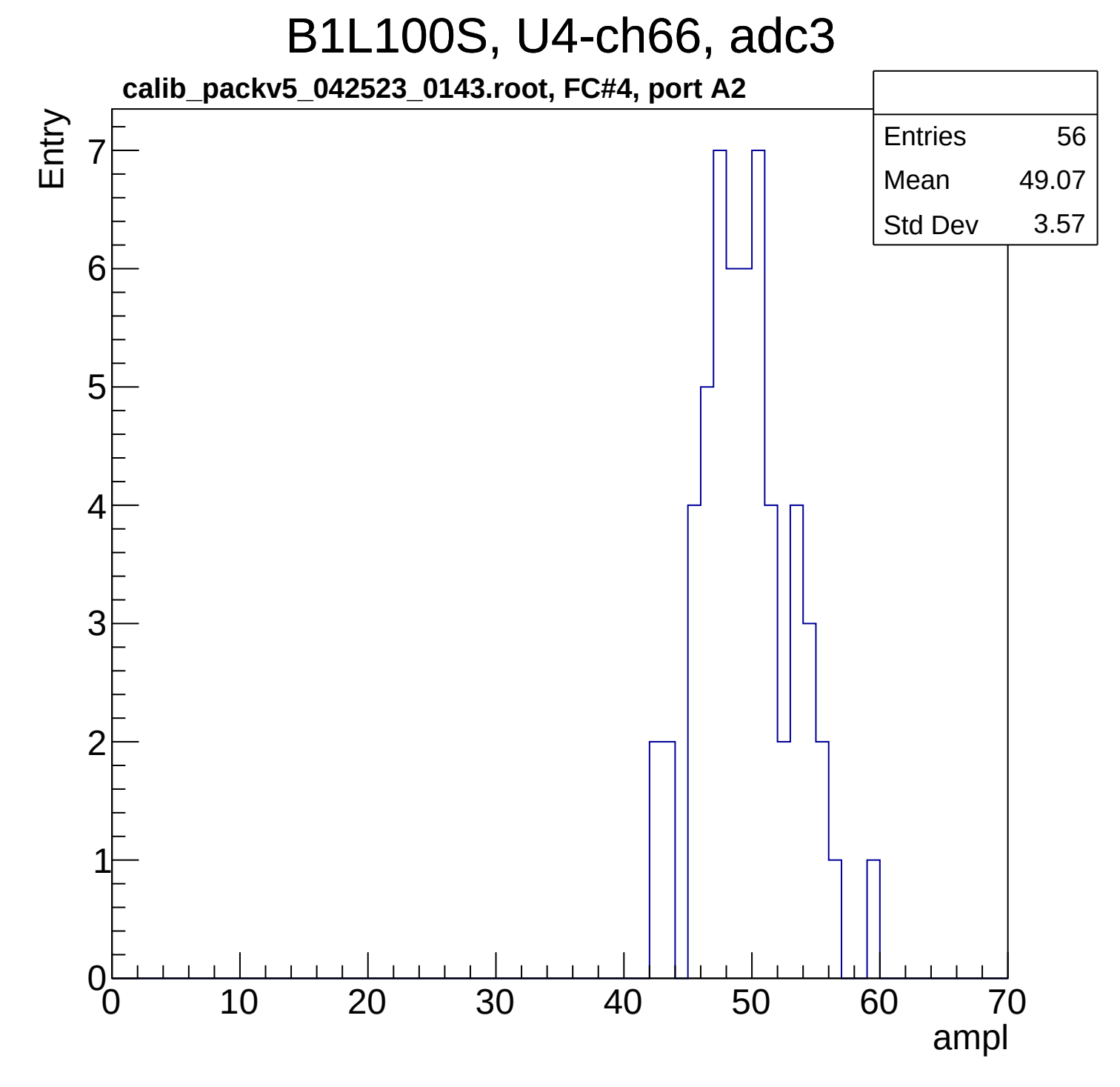

B1L100S, U4-ch65, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

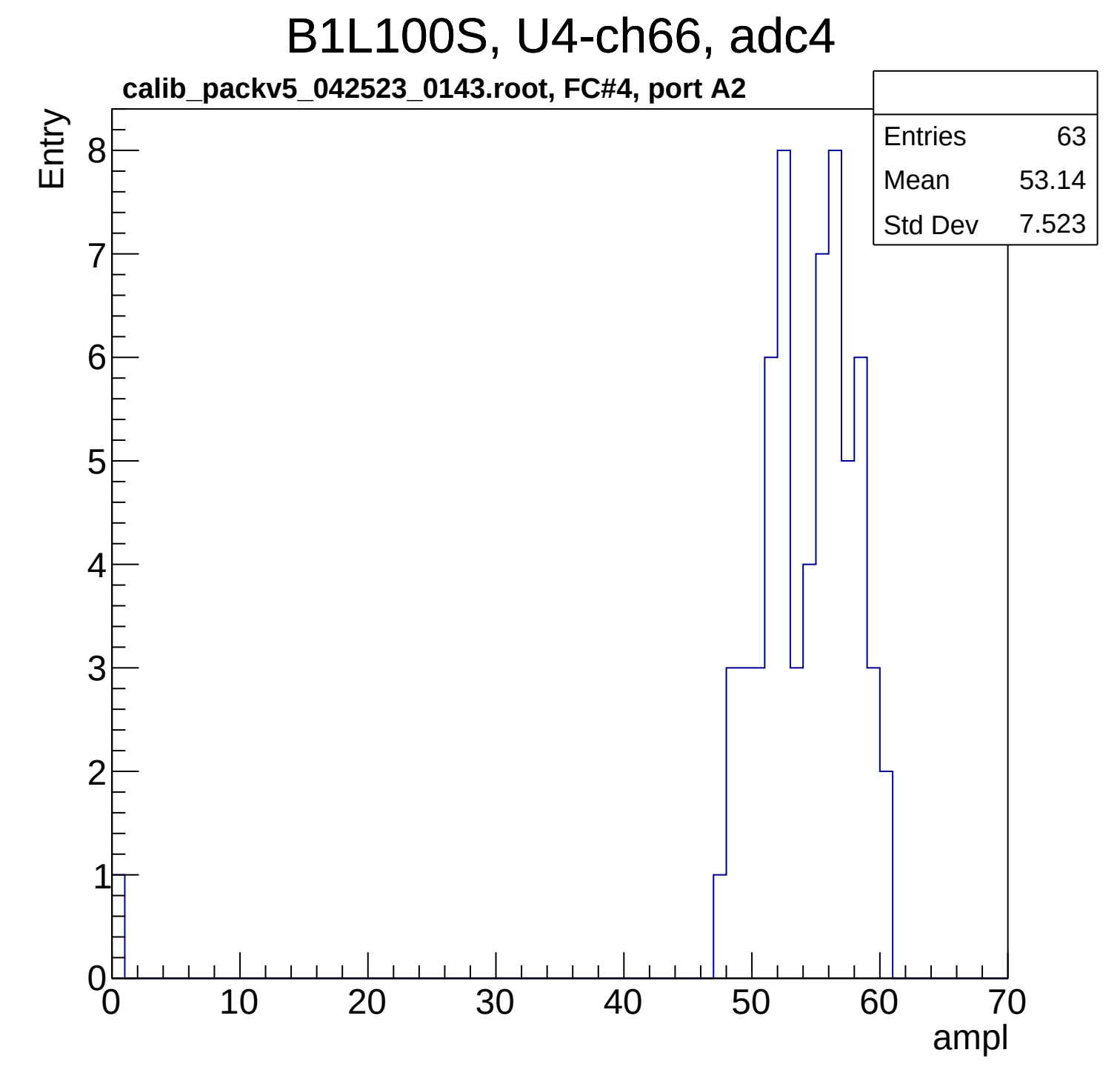

B1L100S, U4-ch65, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

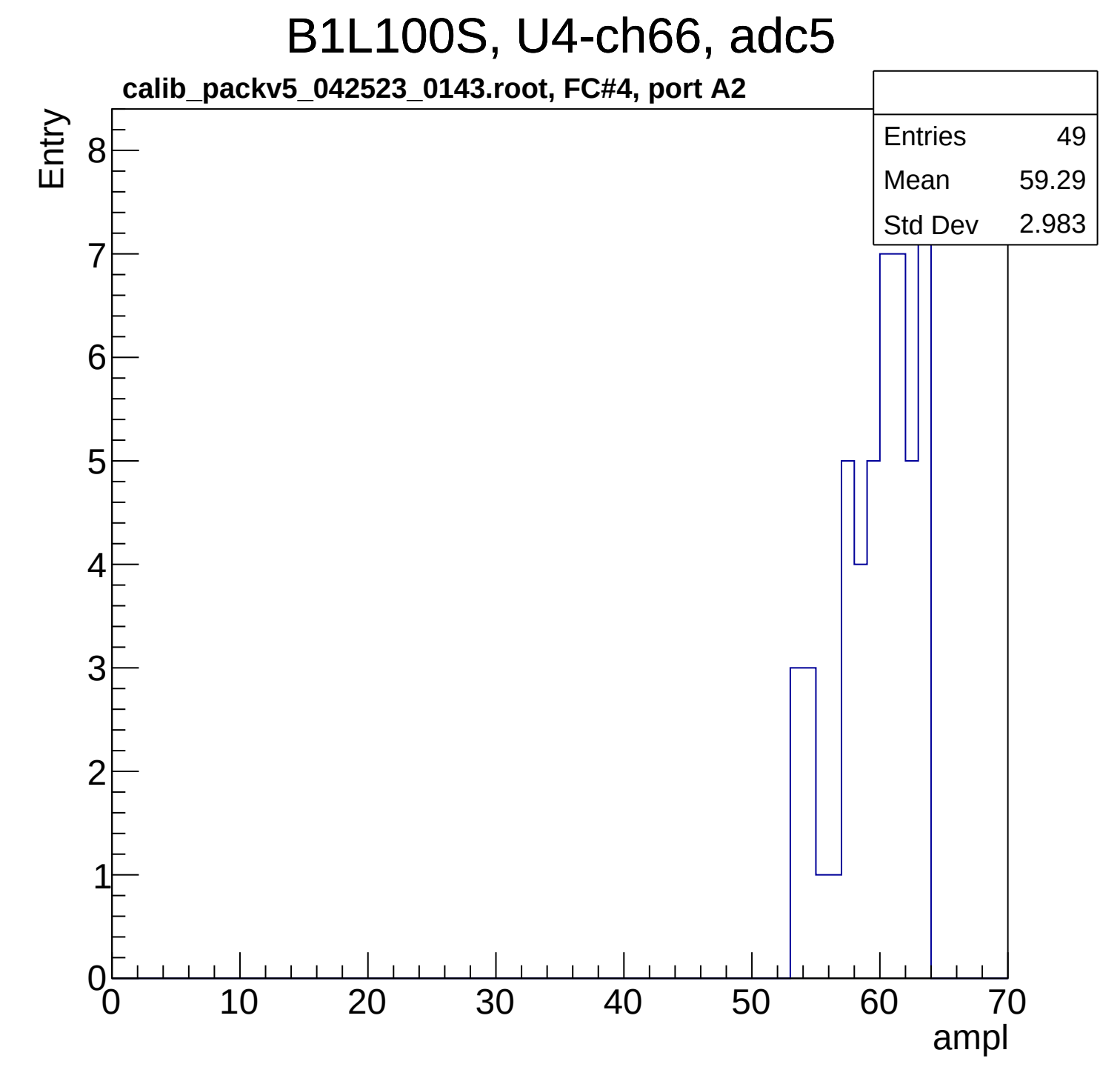

B1L100S, U4-ch66, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 29.64
Std Dev 3.365
Gaus mean : 30.0185
Gaus Width: 3.7020
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

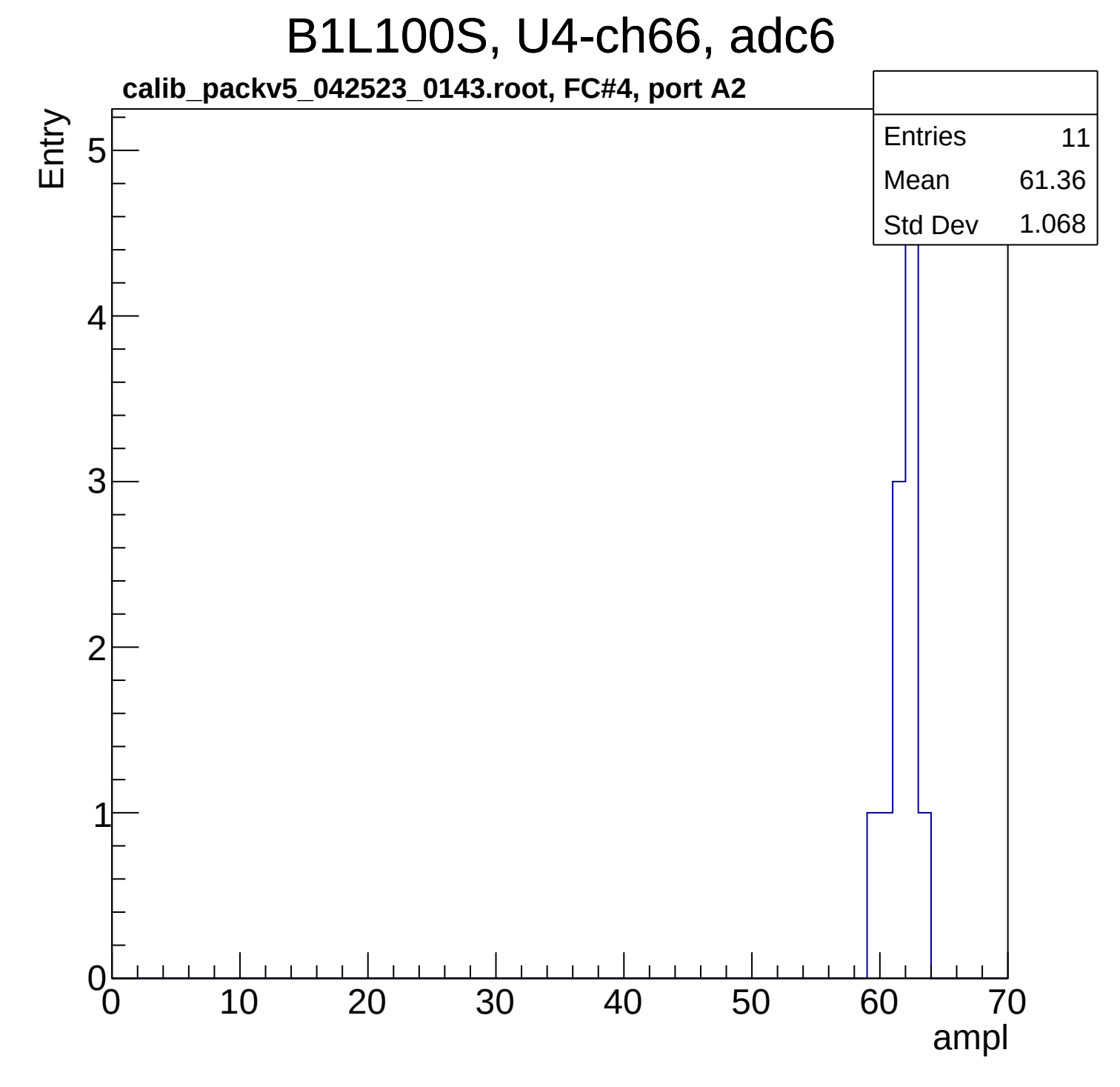

B1L100S, U4-ch66, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 36
Std Dev 3.503
Gaus mean : 37.3786
Gaus Width: 3.8287
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

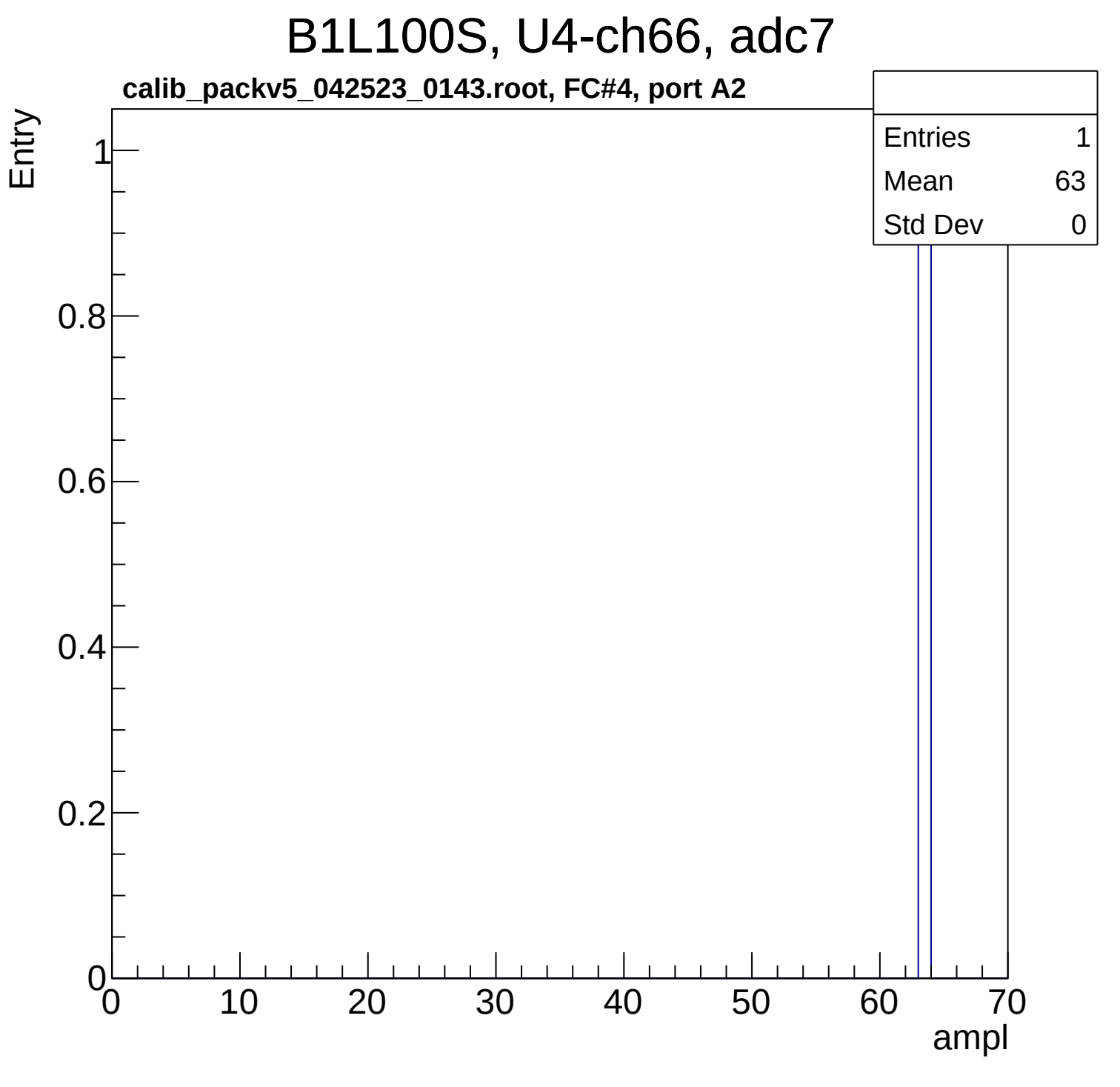

B1L100S, U4-ch66, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 41.27
Std Dev 4.045
Gaus mean : 42.1054
Gaus Width: 3.6823
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

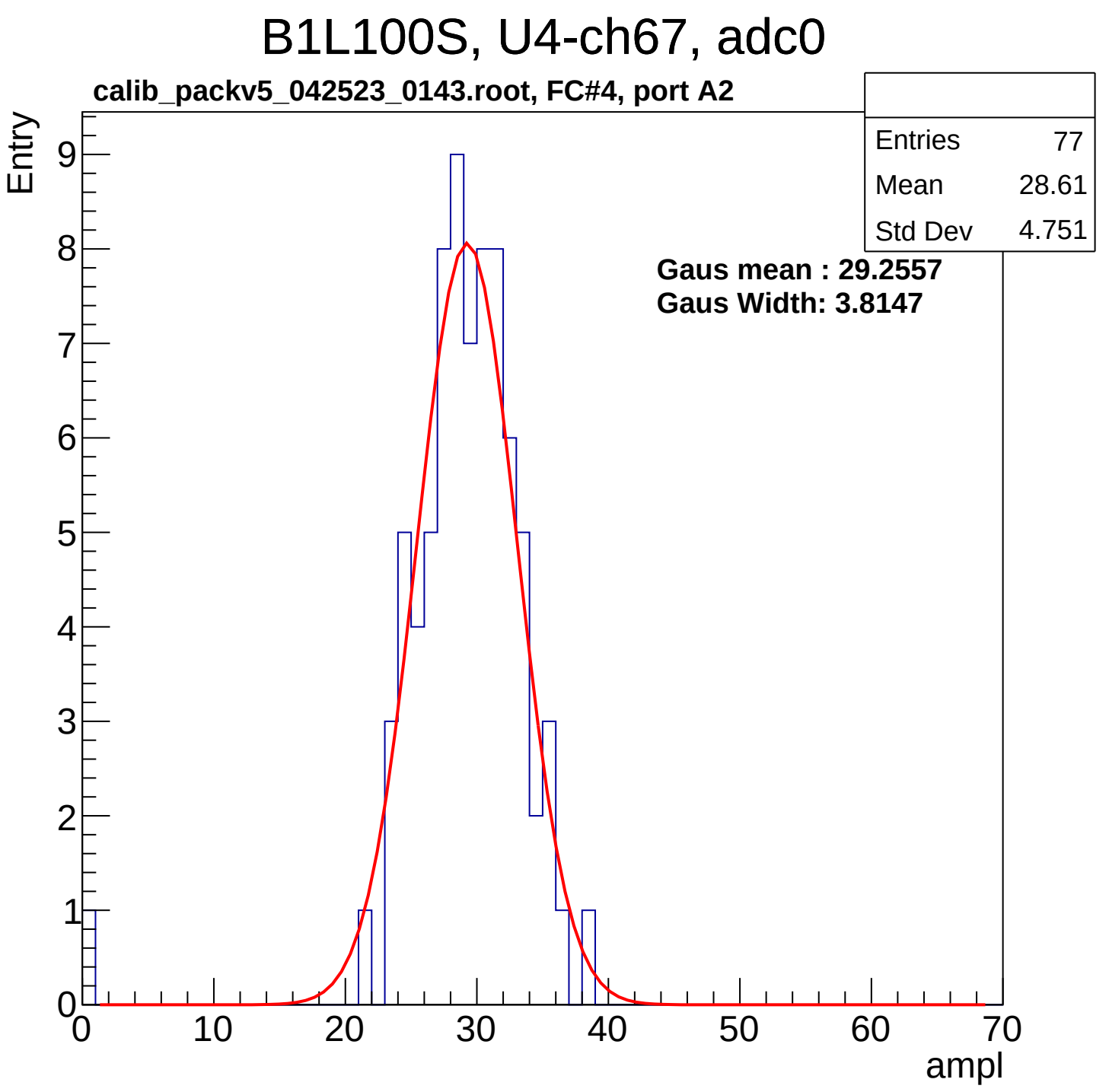

B1L100S, U4-ch66, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 49.07
Std Dev 3.57
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

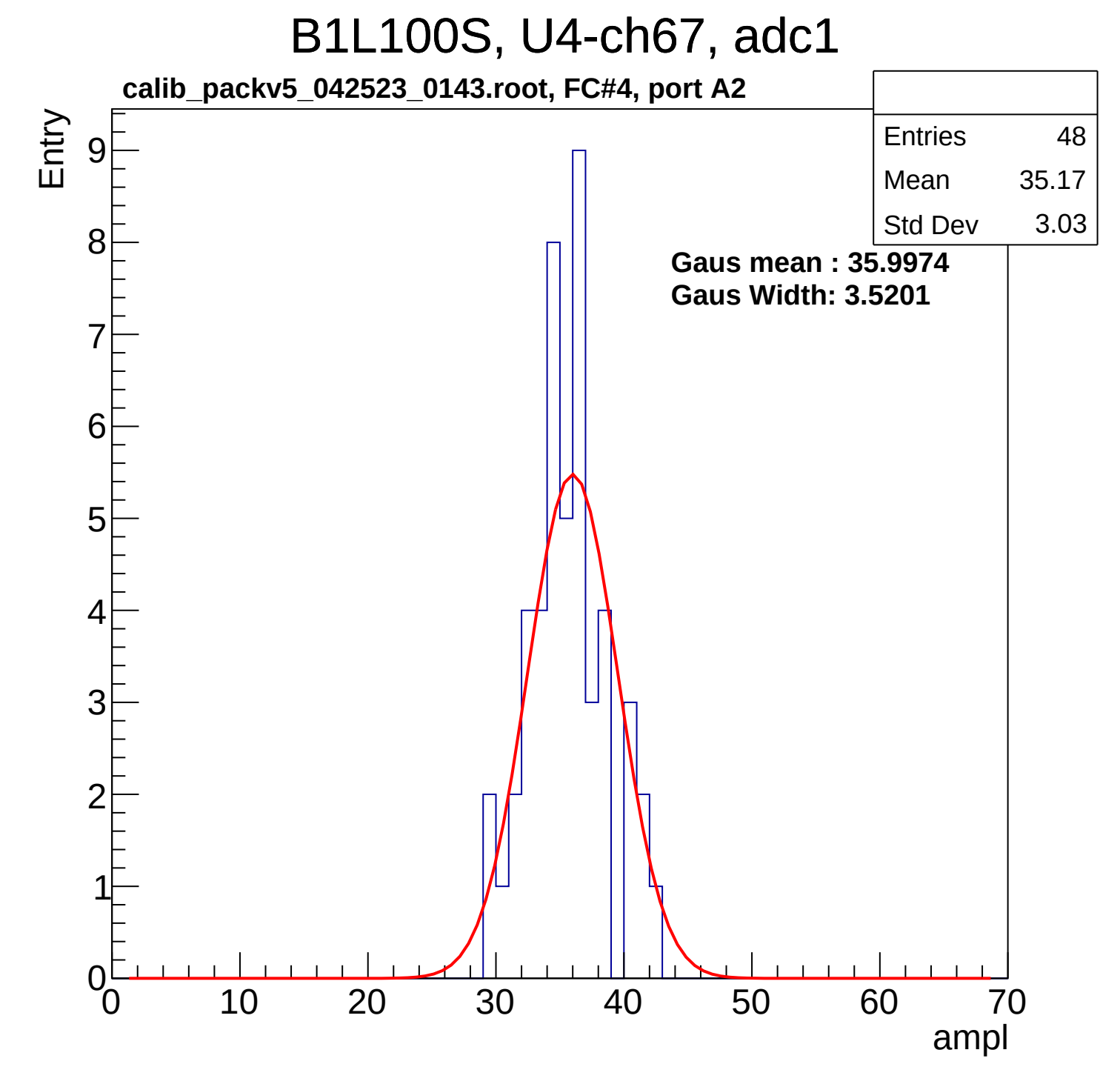

B1L100S, U4-ch66, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 53.14
Std Dev 7.523
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

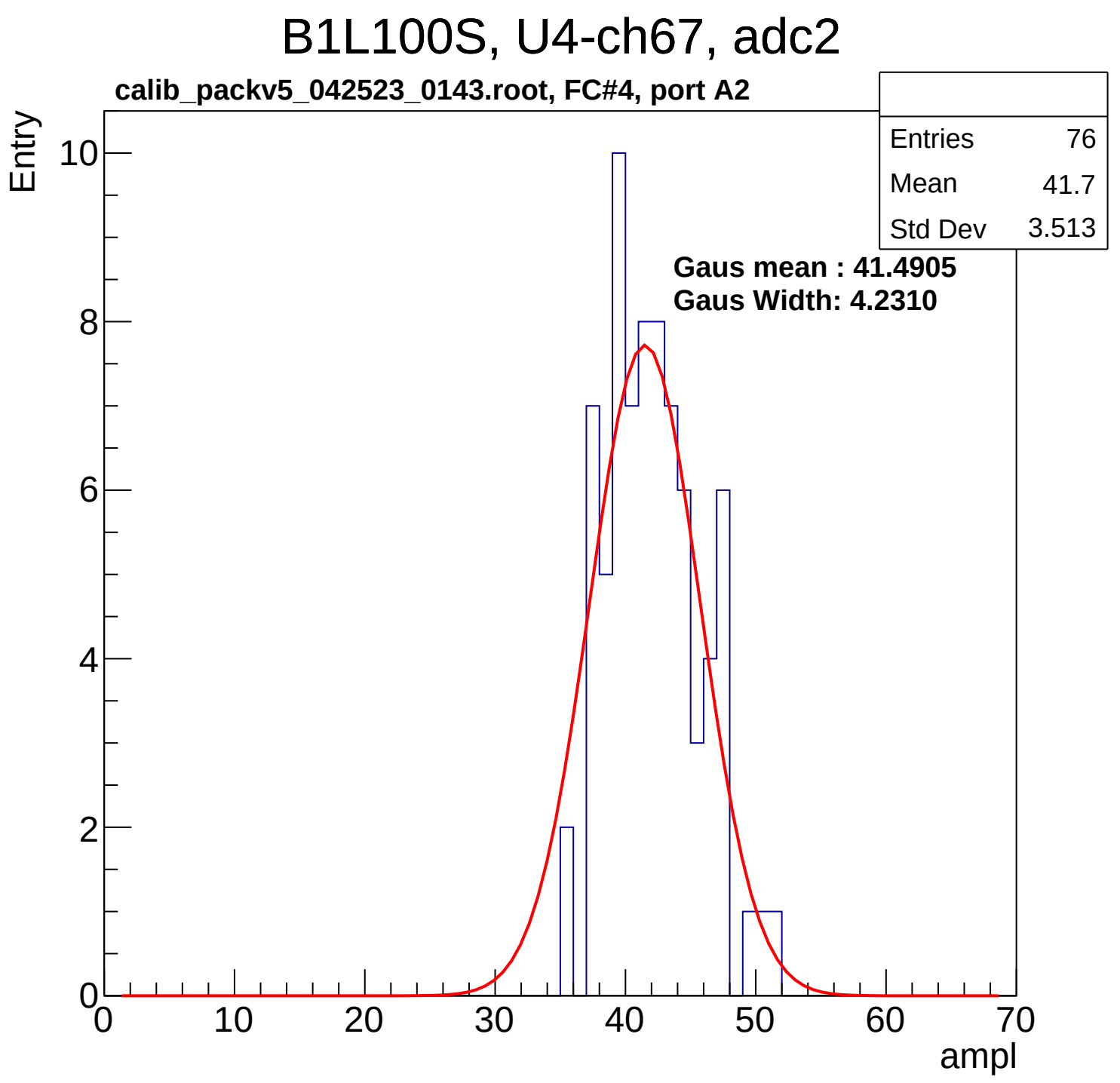

B1L100S, U4-ch66, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 59.29
Std Dev 2.983
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

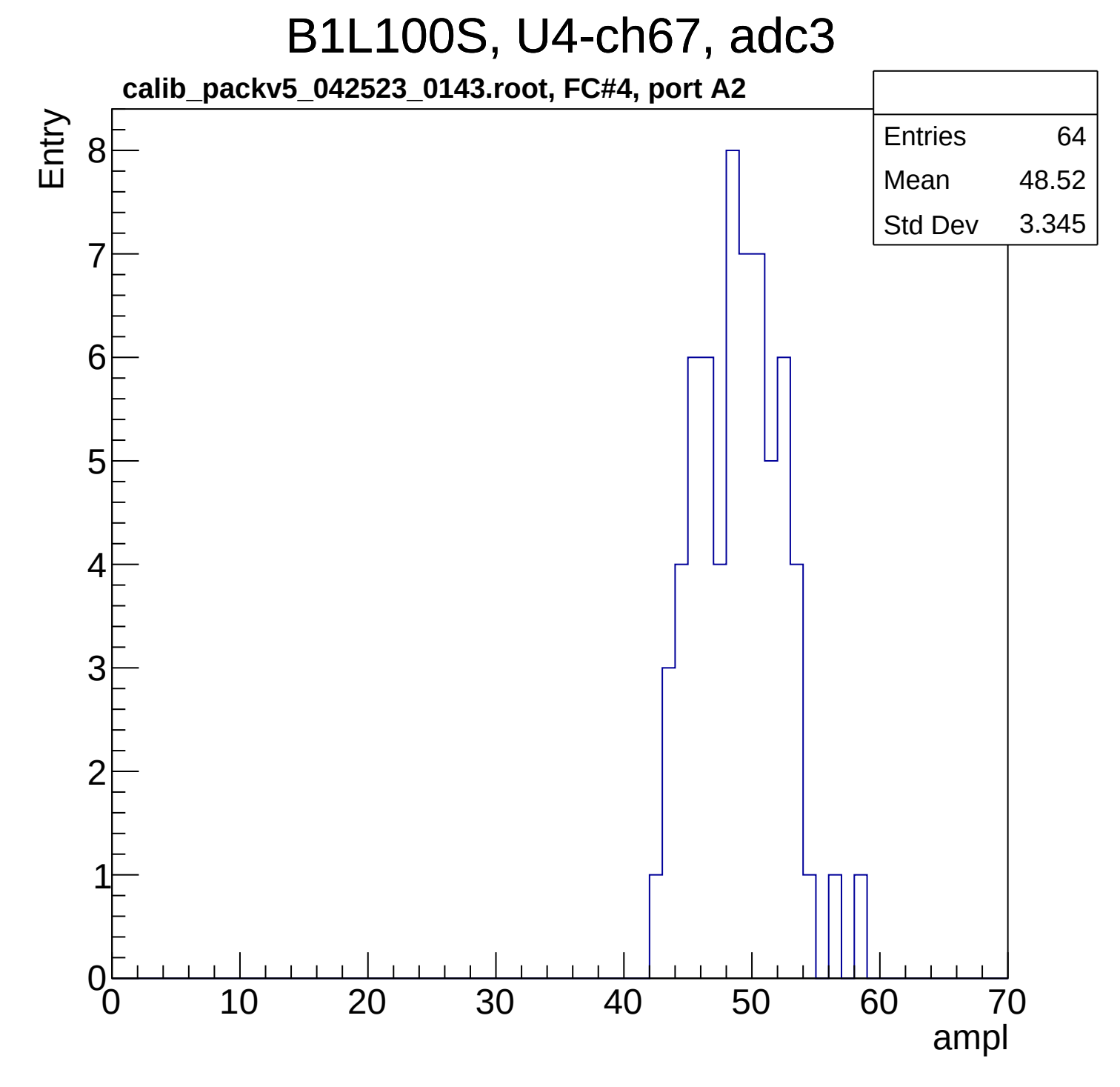

B1L100S, U4-ch66, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 61.36
Std Dev 1.068
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

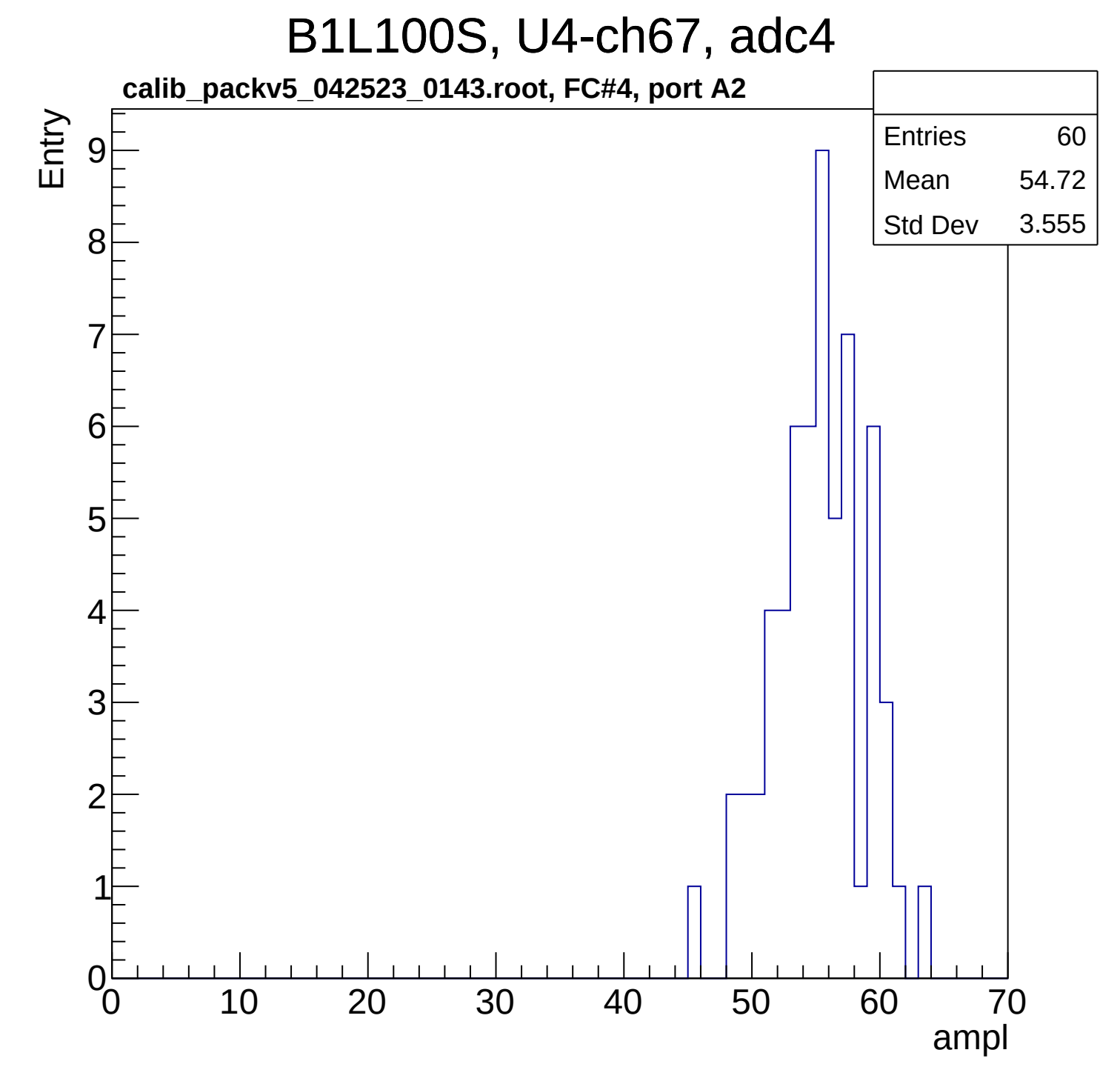

B1L100S, U4-ch66, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

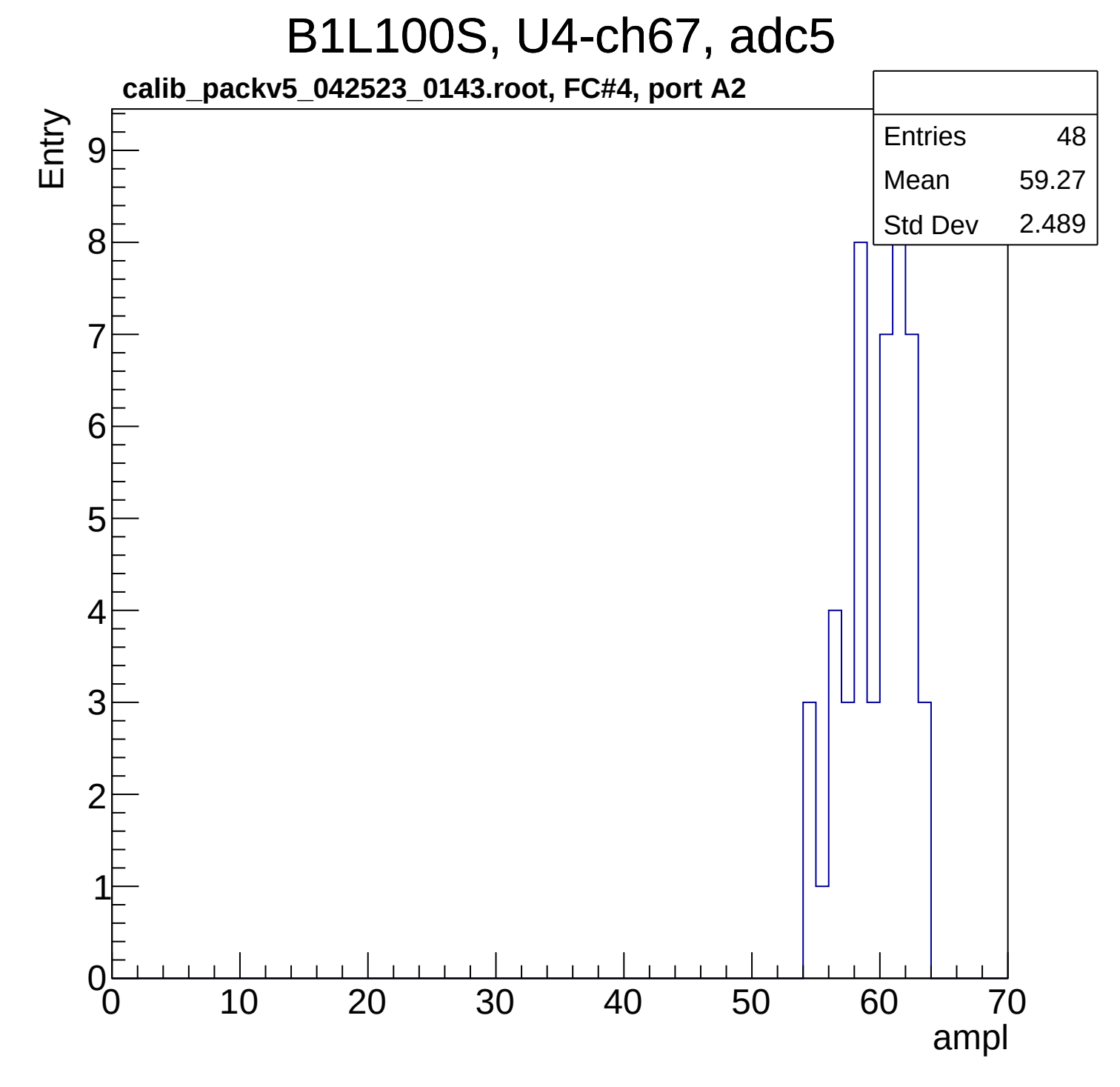

B1L100S, U4-ch67, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 28.61
Std Dev 4.751
Gaus mean : 29.2557
Gaus Width: 3.8147
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

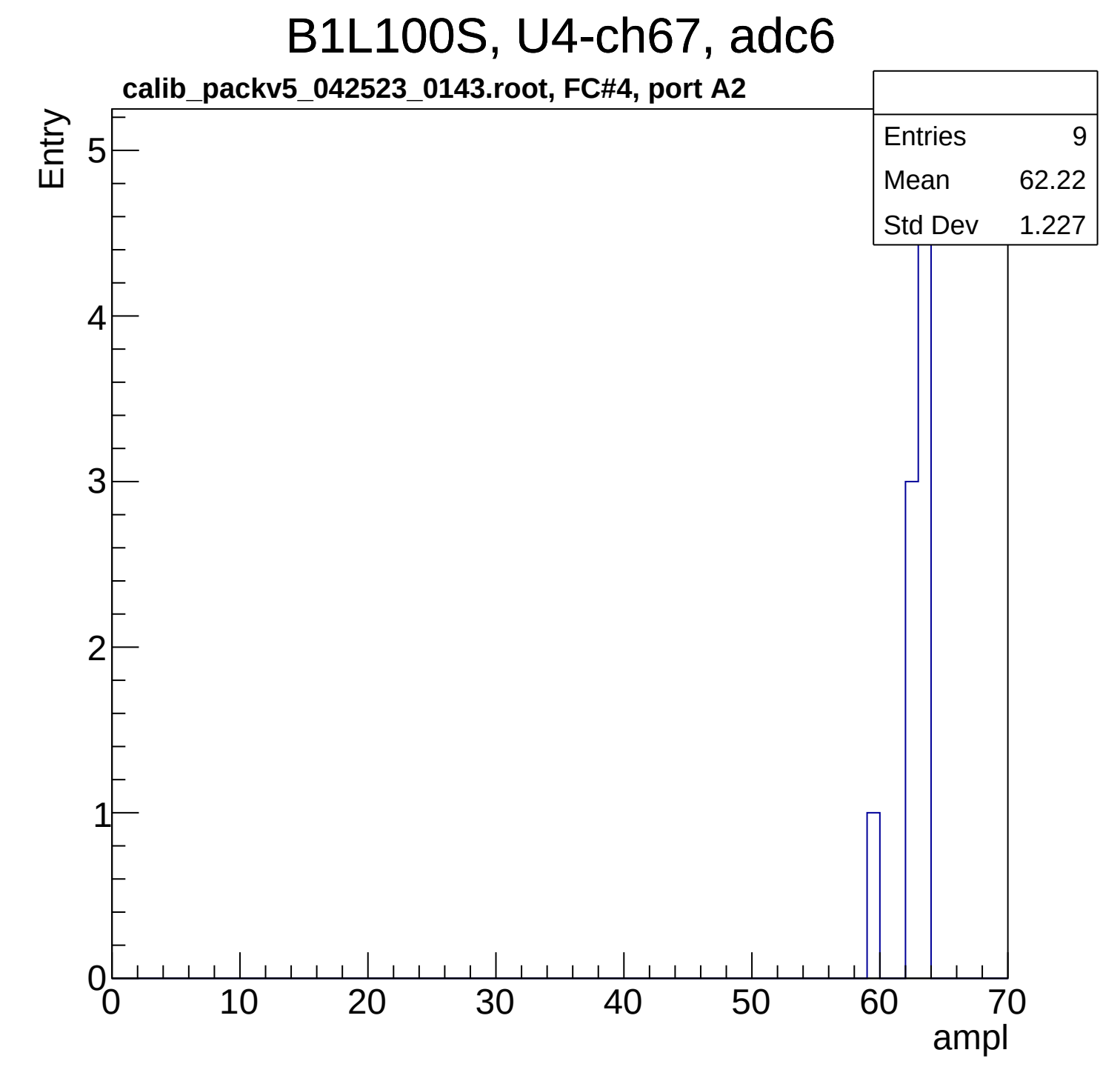

B1L100S, U4-ch67, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 35.17
Std Dev 3.03
Gaus mean : 35.9974
Gaus Width: 3.5201
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

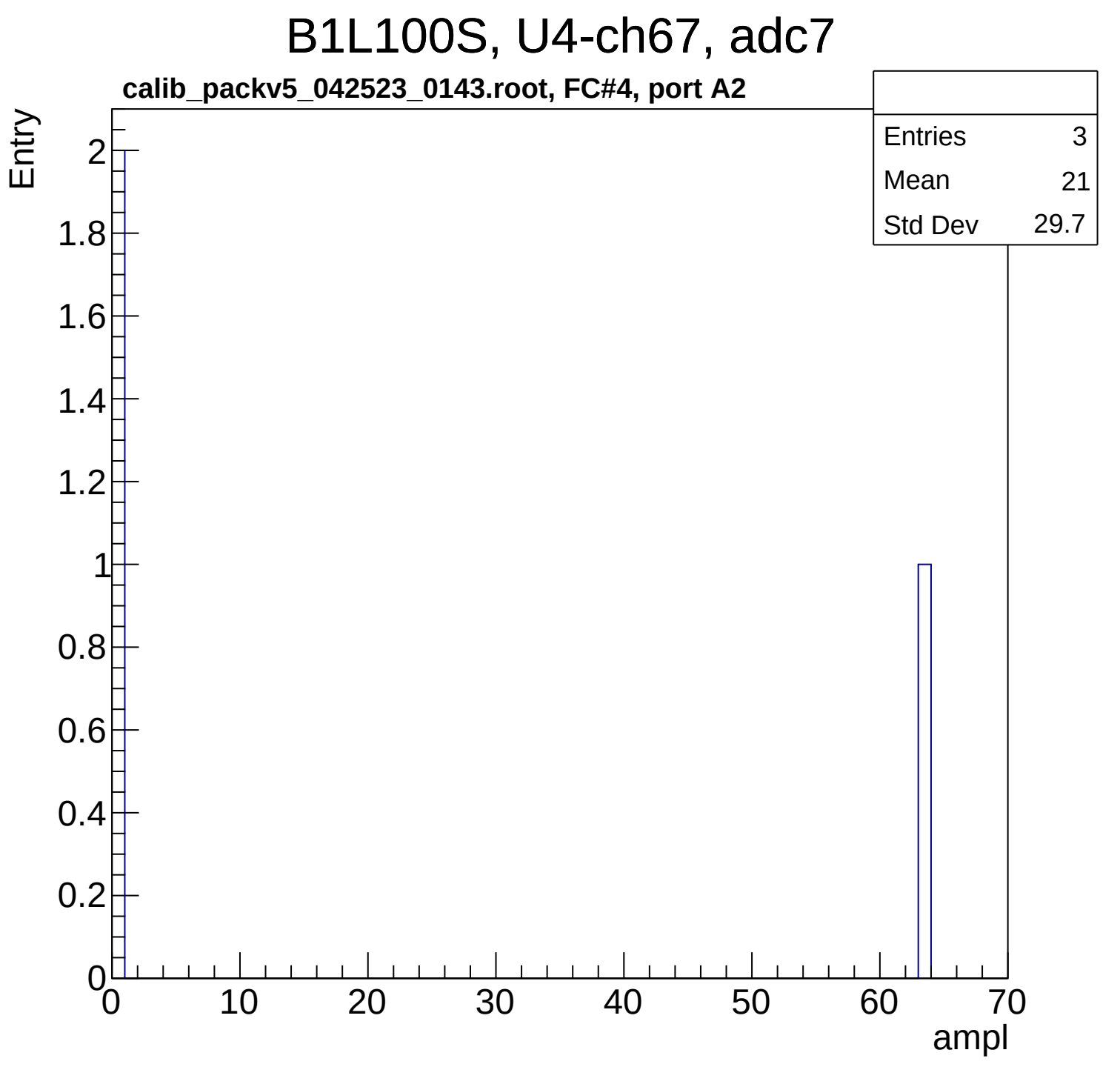

B1L100S, U4-ch67, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 41.7
Std Dev 3.513
Gaus mean : 41.4905
Gaus Width: 4.2310
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

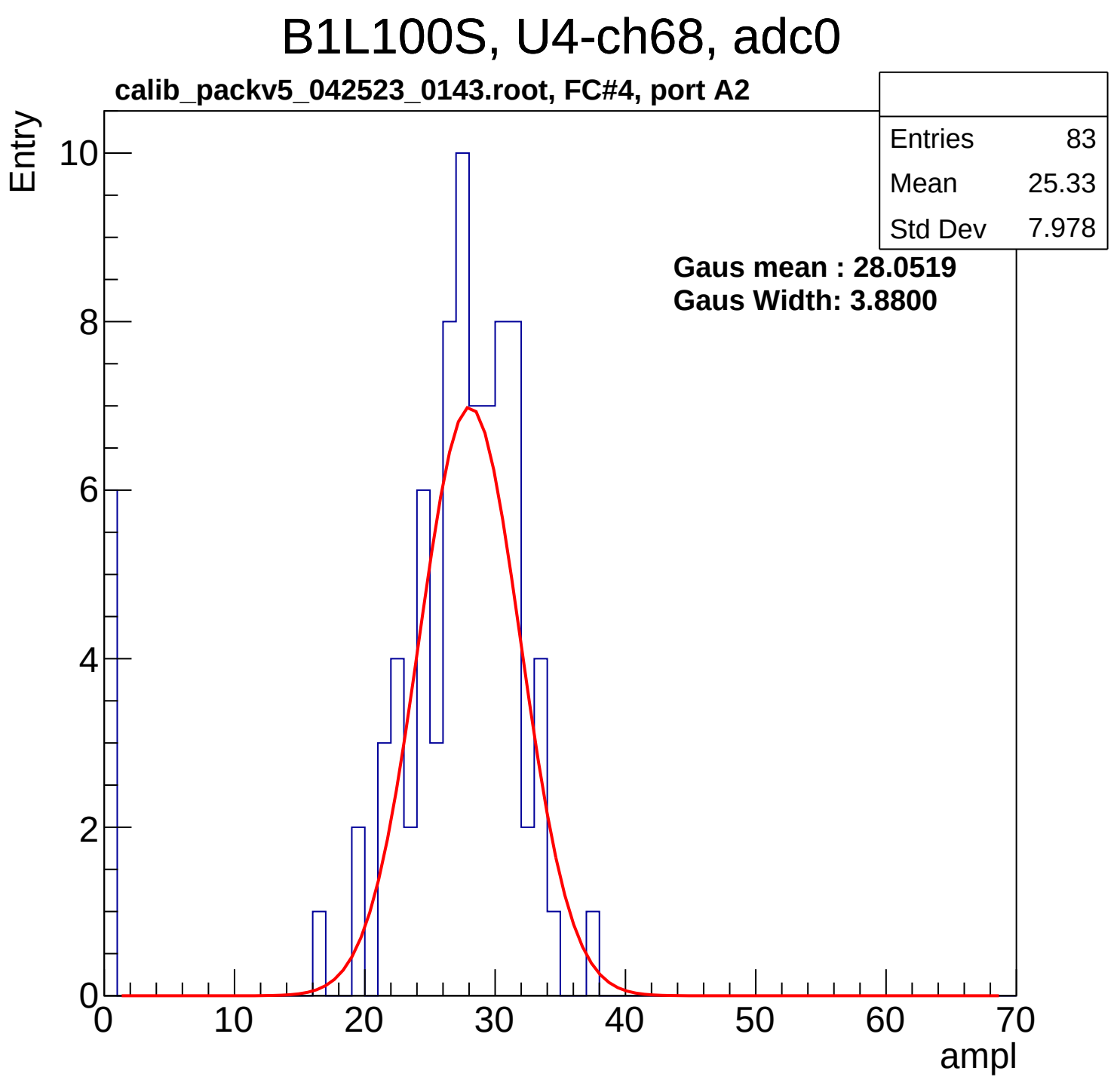

B1L100S, U4-ch67, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 48.52
Std Dev 3.345
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

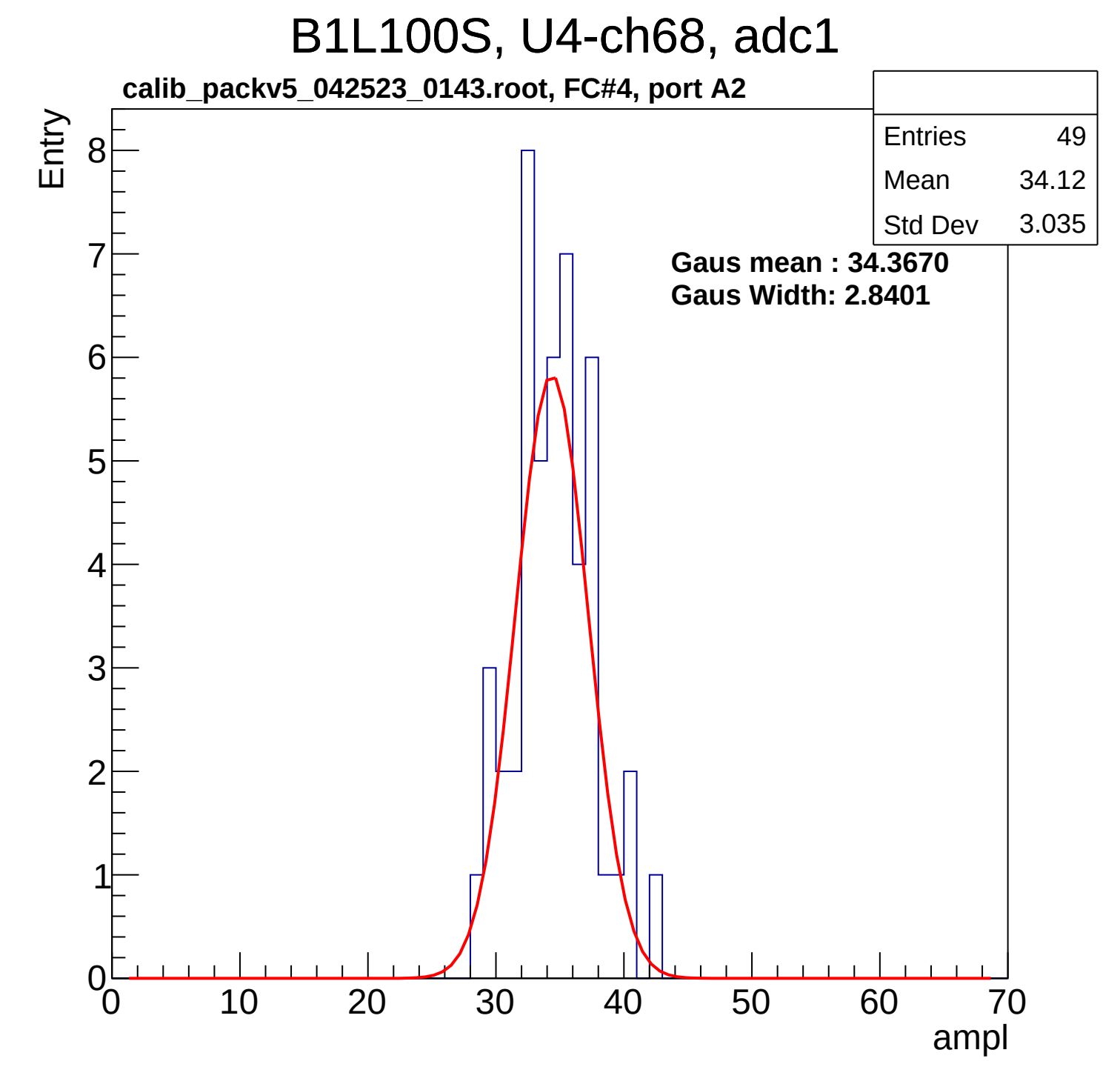

B1L100S, U4-ch67, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 54.72
Std Dev 3.555
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

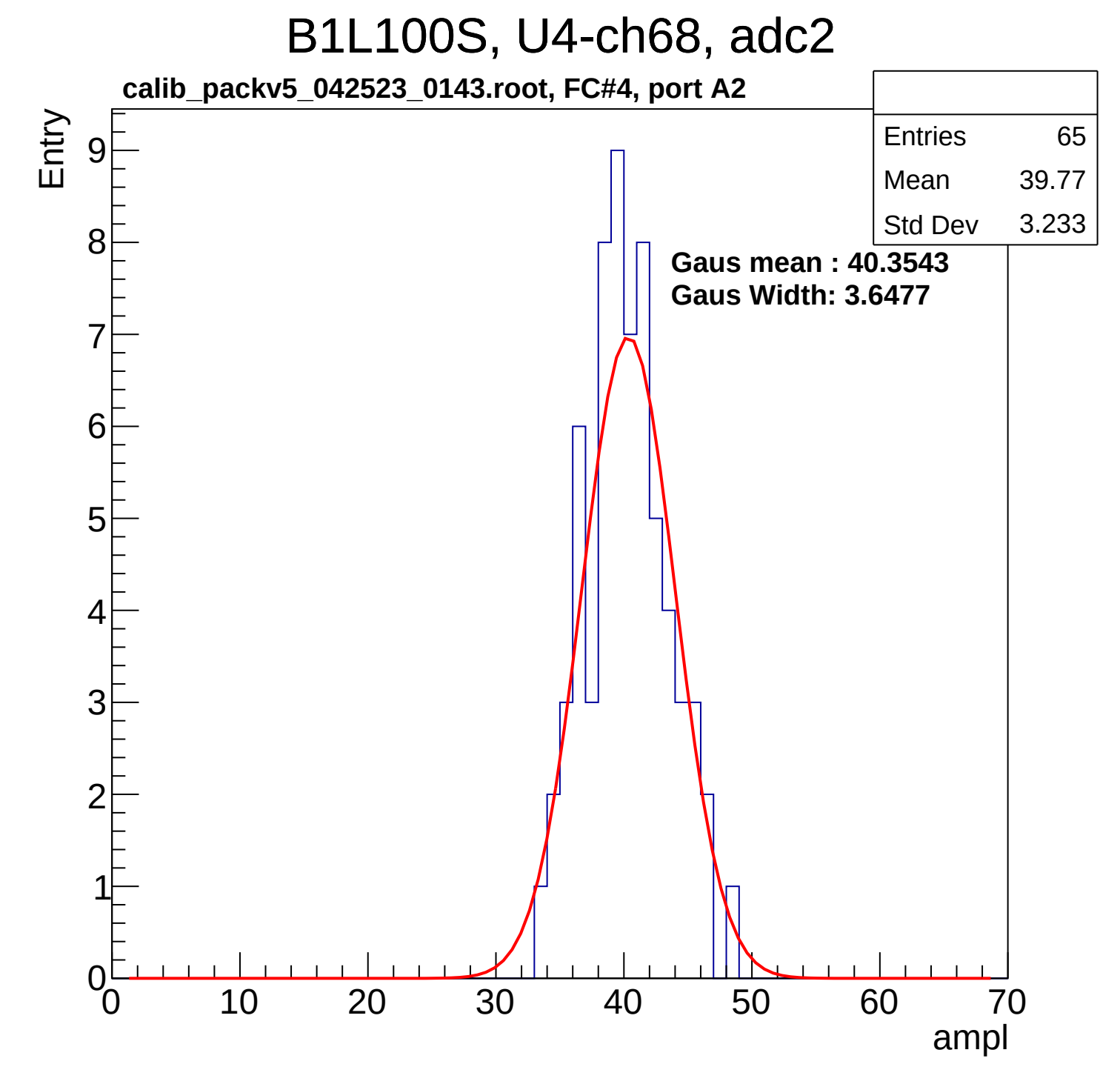

B1L100S, U4-ch67, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 59.27
Std Dev 2.489
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

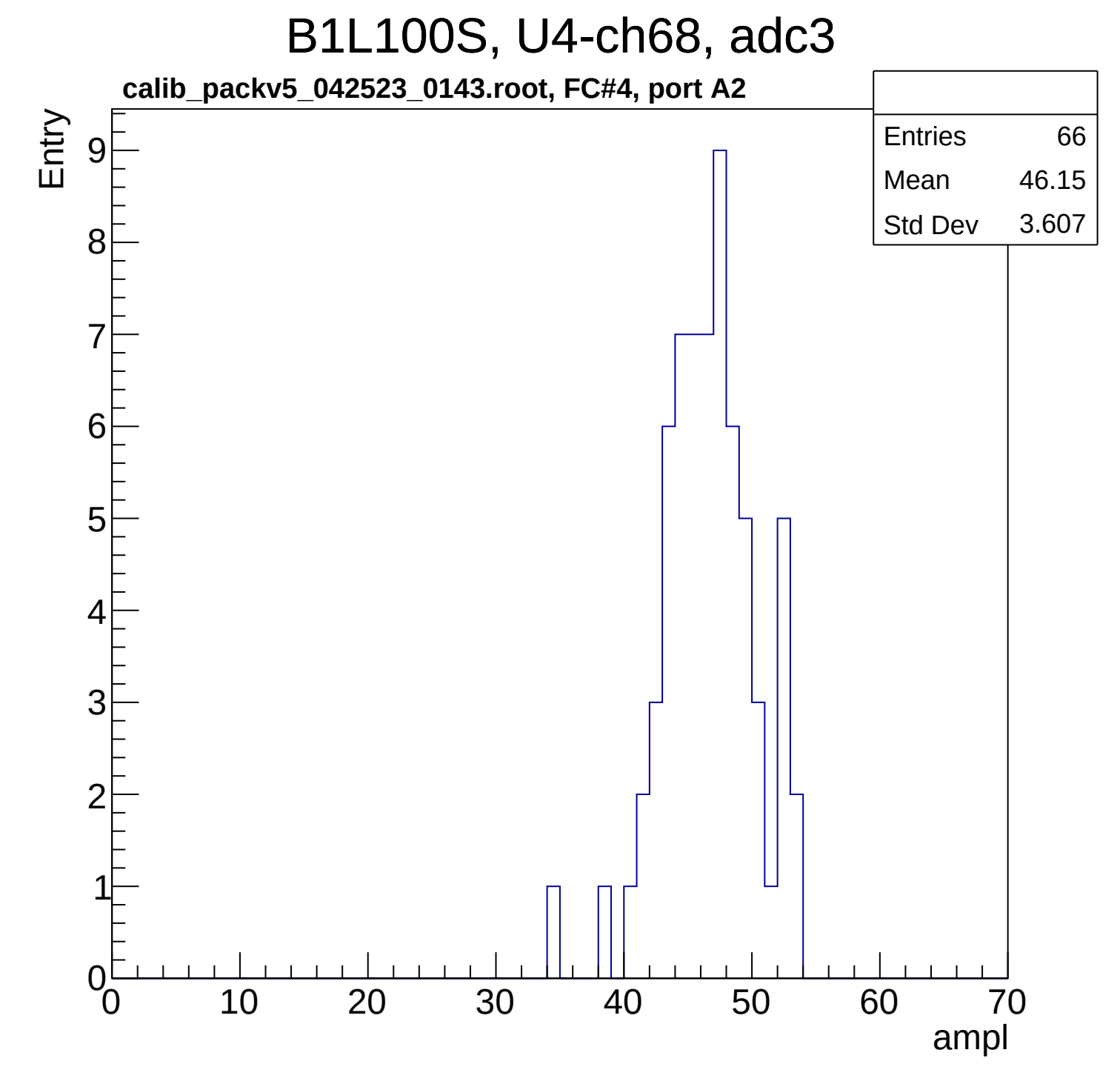

B1L100S, U4-ch67, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 62.22
Std Dev 1.227
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

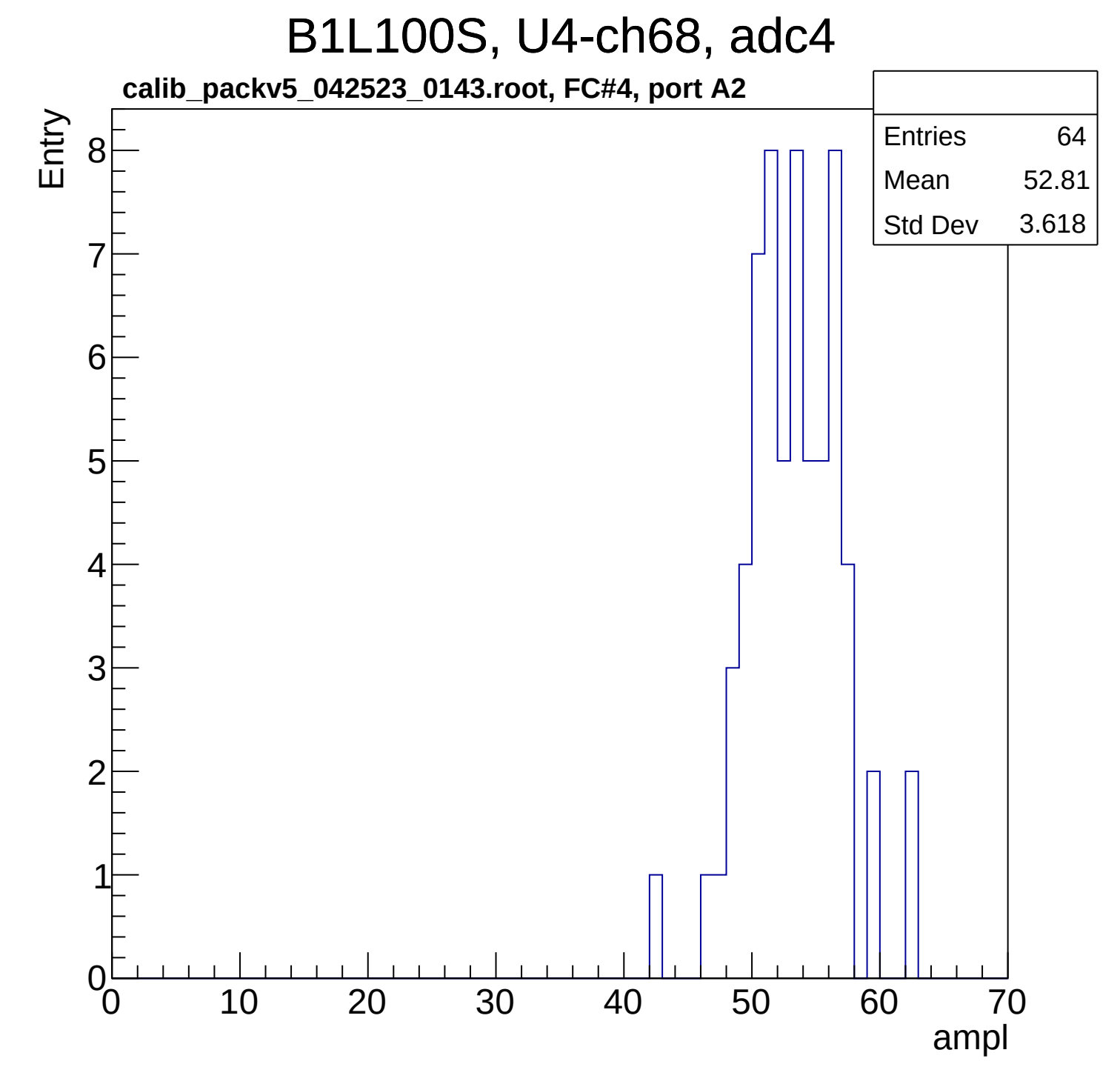

B1L100S, U4-ch67, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 21
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

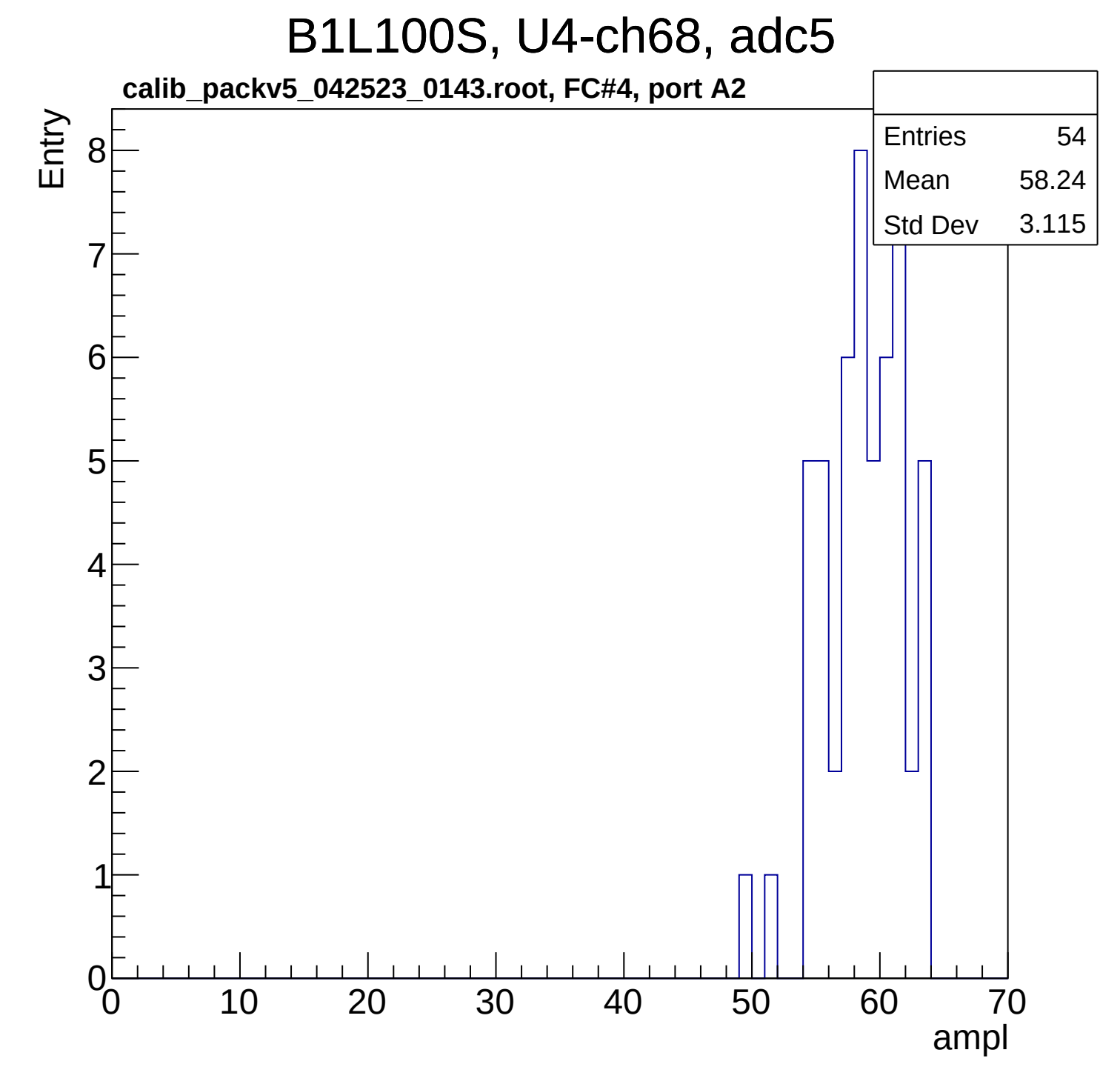

B1L100S, U4-ch68, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 83
Mean 25.33
Std Dev 7.978
Gaus mean : 28.0519
Gaus Width: 3.8800
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

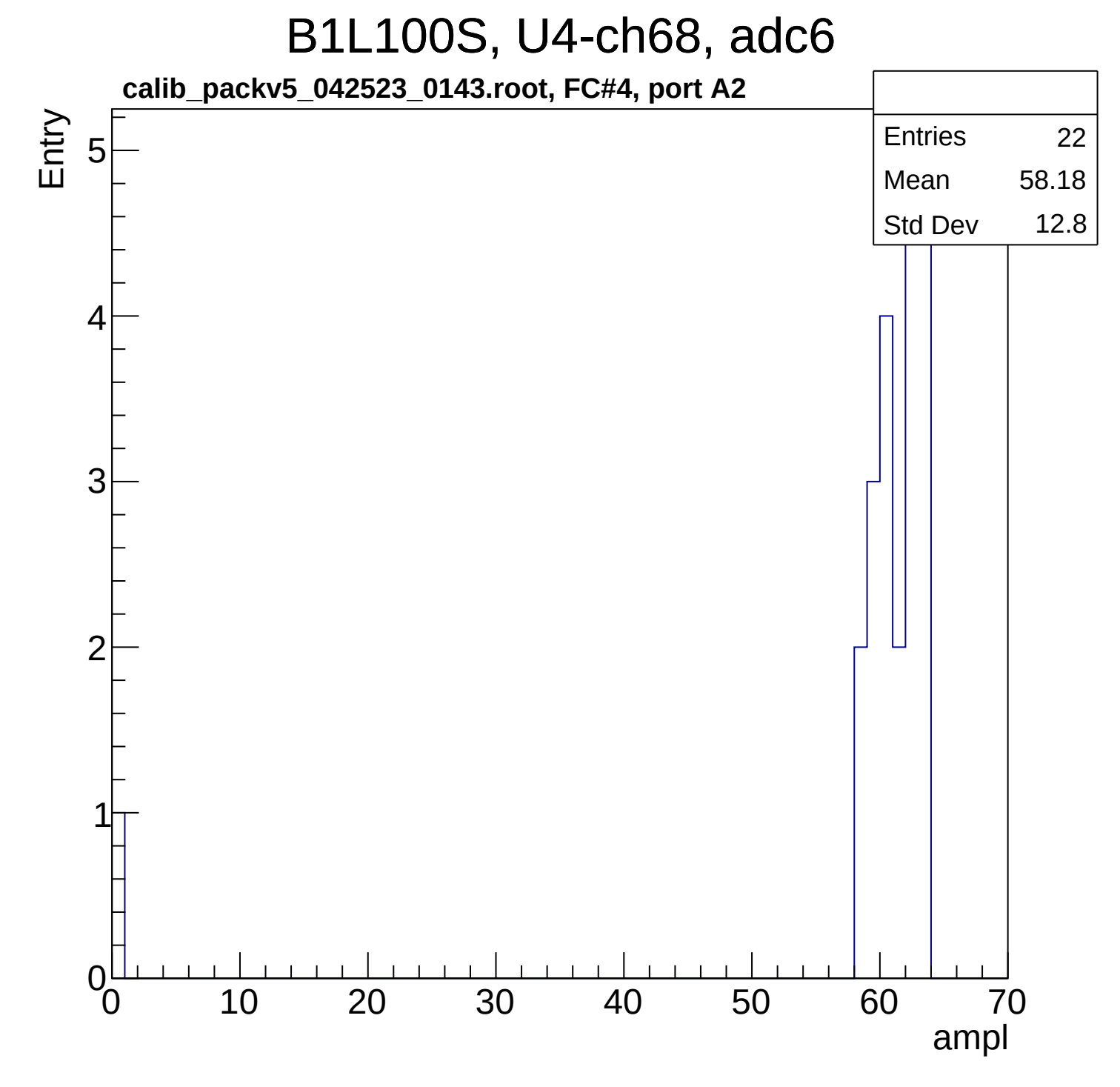

B1L100S, U4-ch68, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 34.12
Std Dev 3.035
Gaus mean : 34.3670
Gaus Width: 2.8401
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

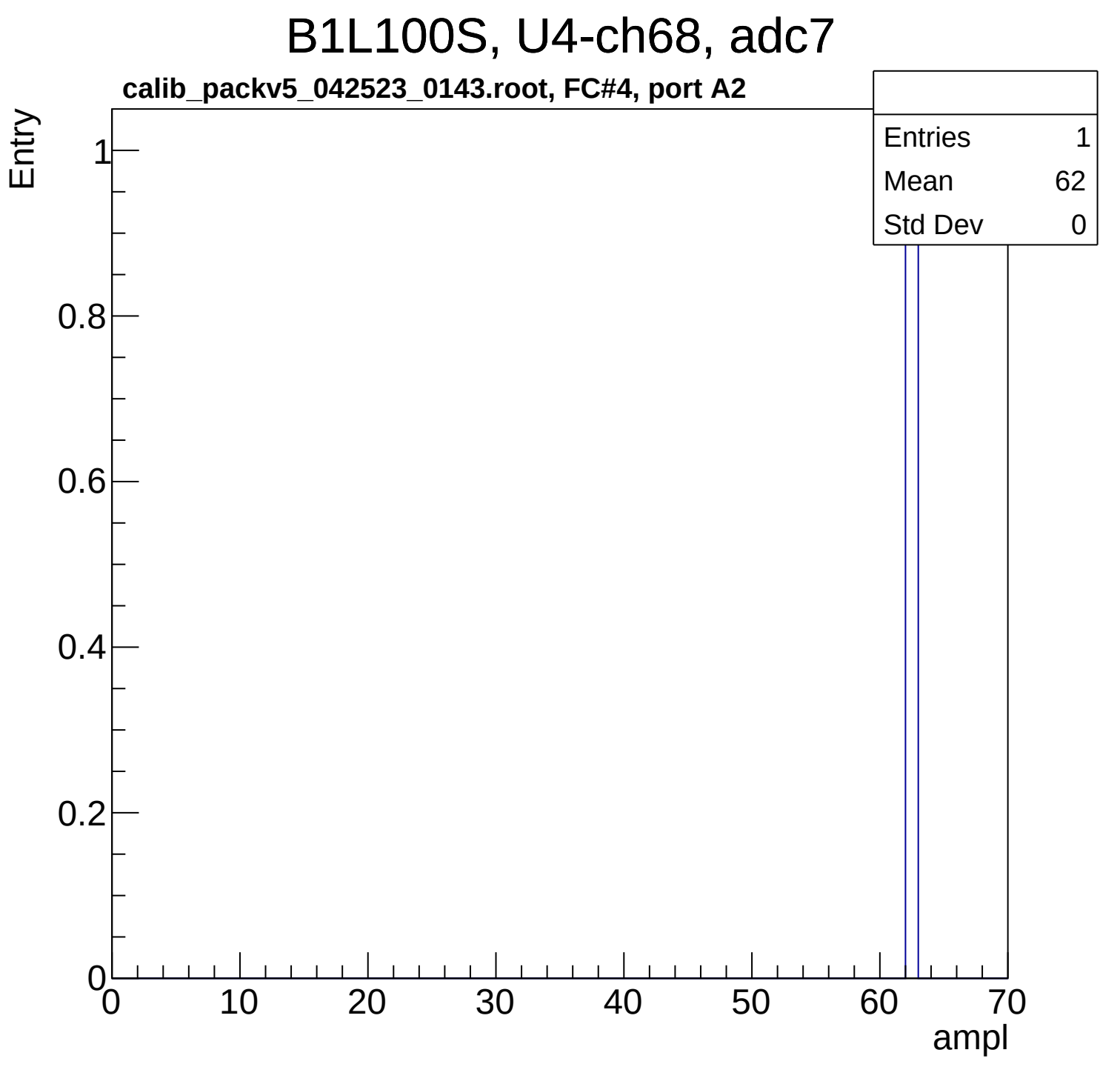

B1L100S, U4-ch68, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 39.77
Std Dev 3.233
Gaus mean : 40.3543
Gaus Width: 3.6477
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

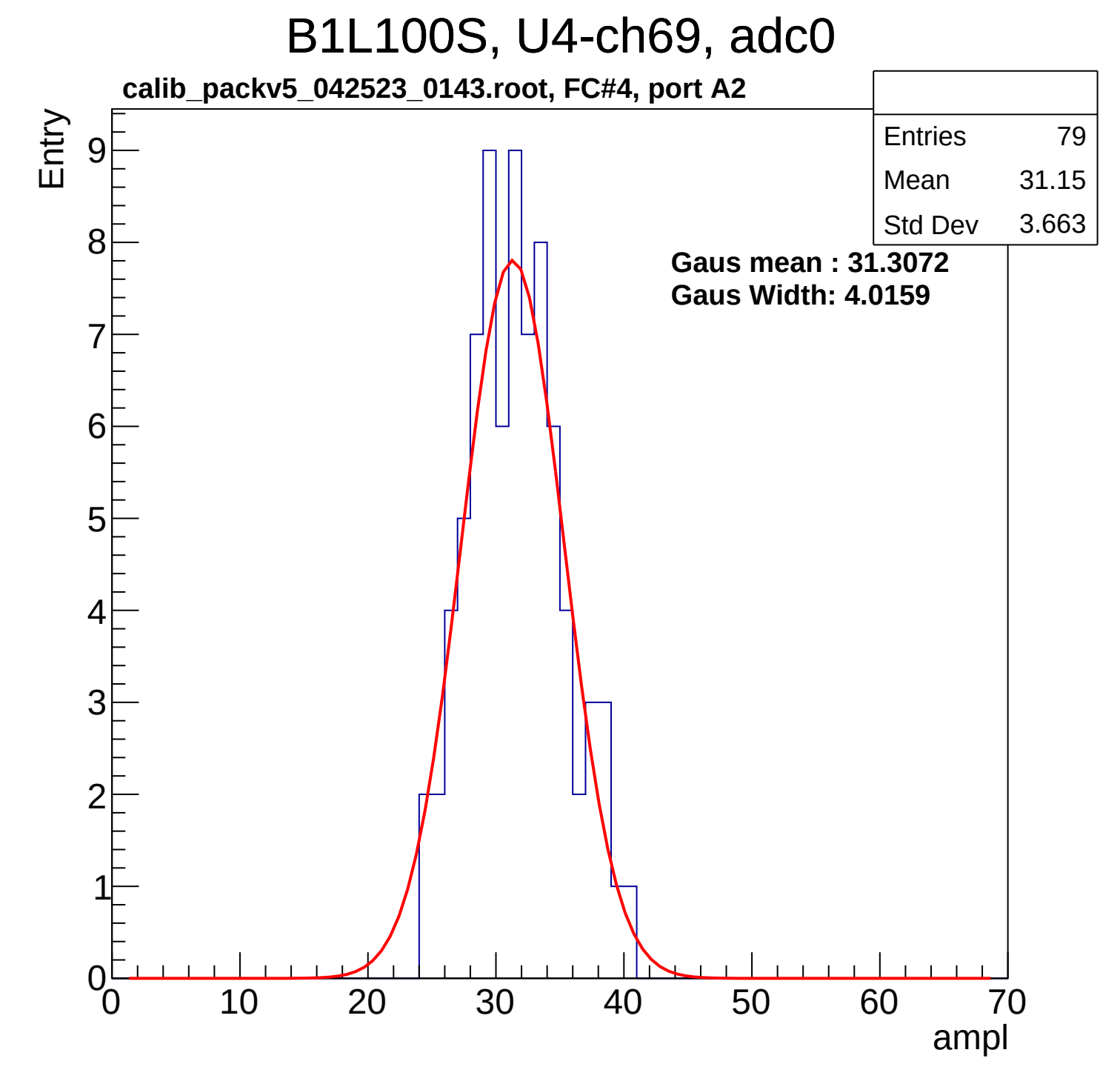

B1L100S, U4-ch68, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 46.15
Std Dev 3.607
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

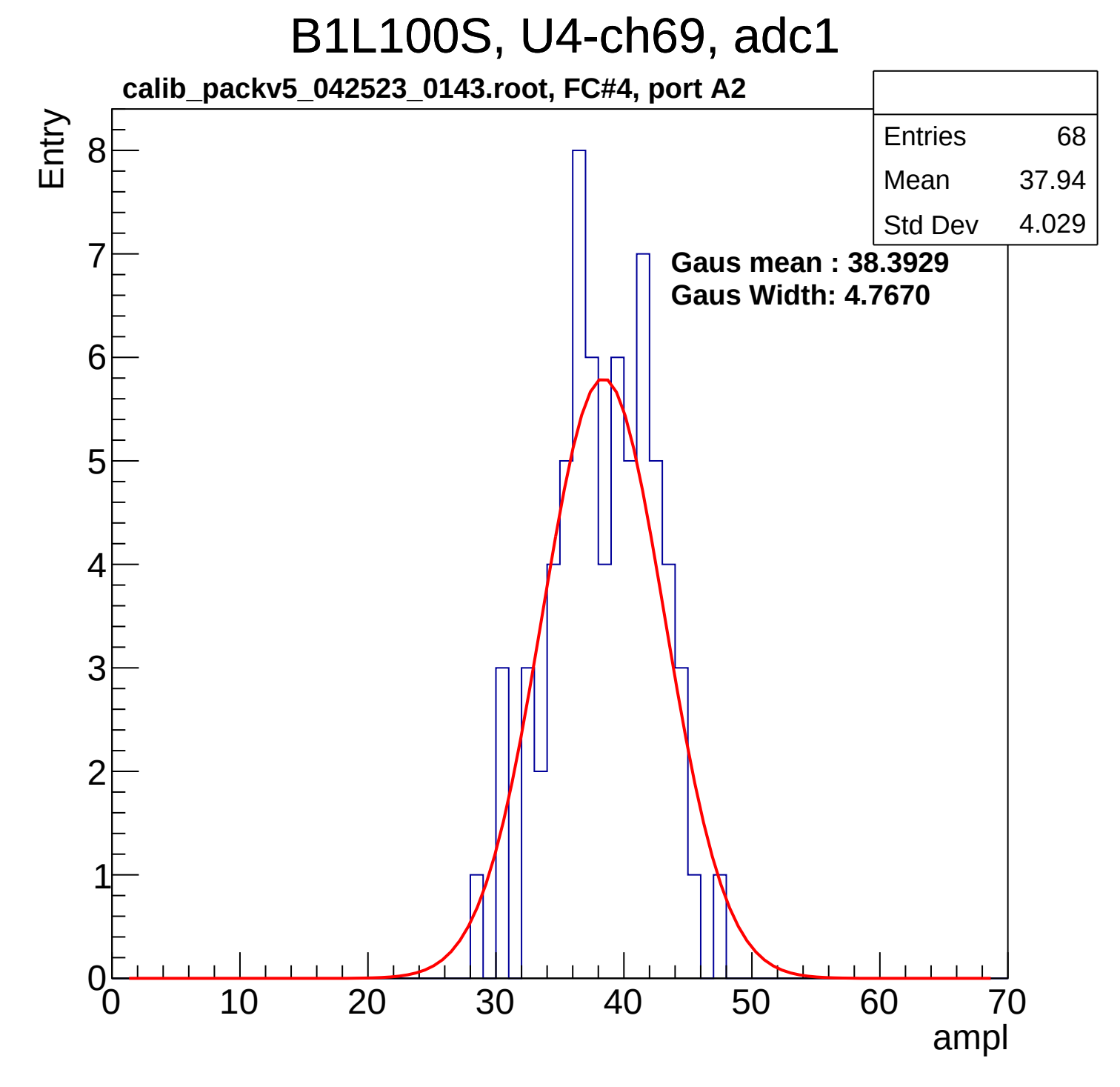

B1L100S, U4-ch68, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 52.81
Std Dev 3.618
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

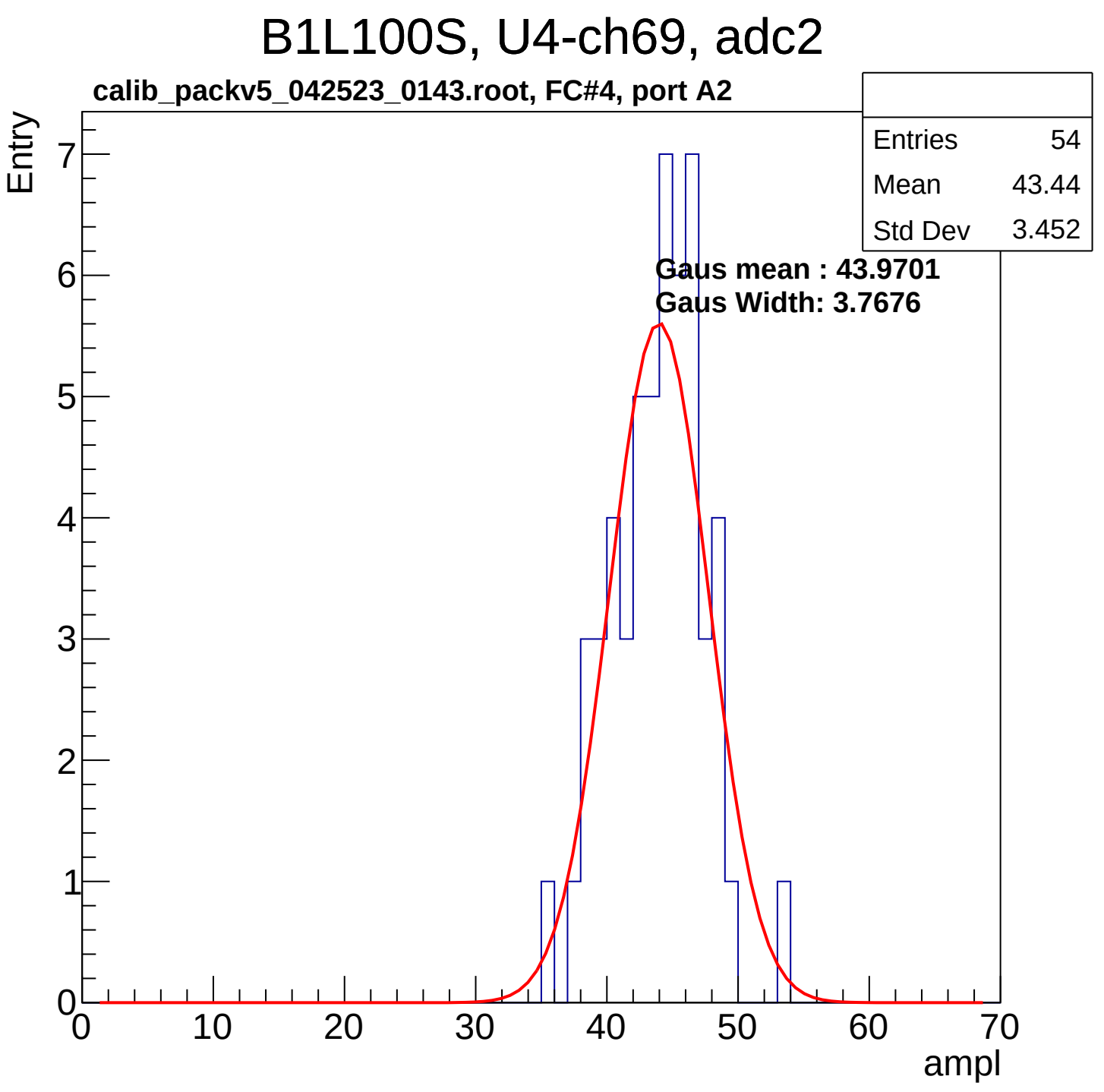

B1L100S, U4-ch68, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 58.24
Std Dev 3.115
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

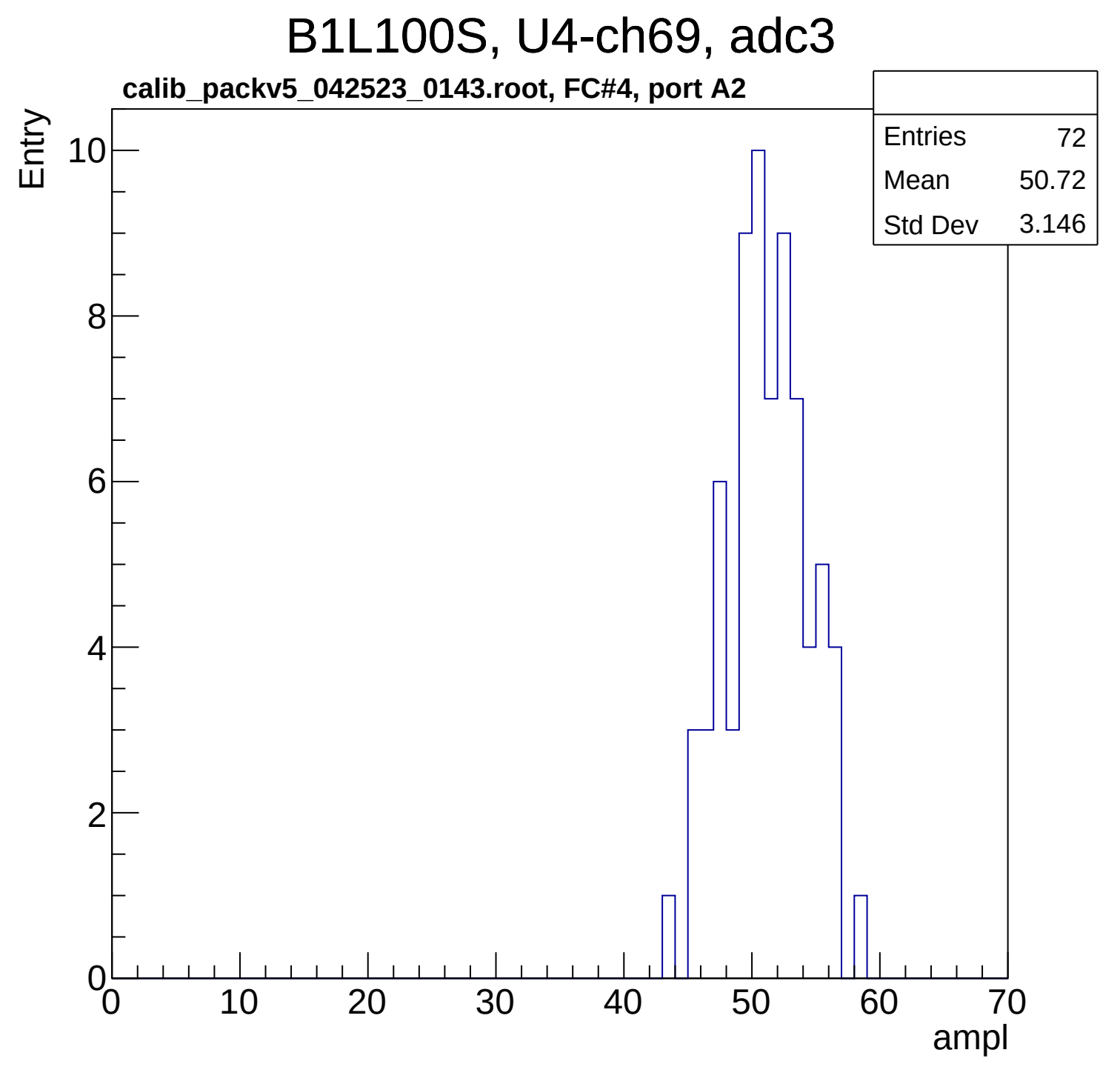

B1L100S, U4-ch68, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 22
Mean 58.18
Std Dev 12.8
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

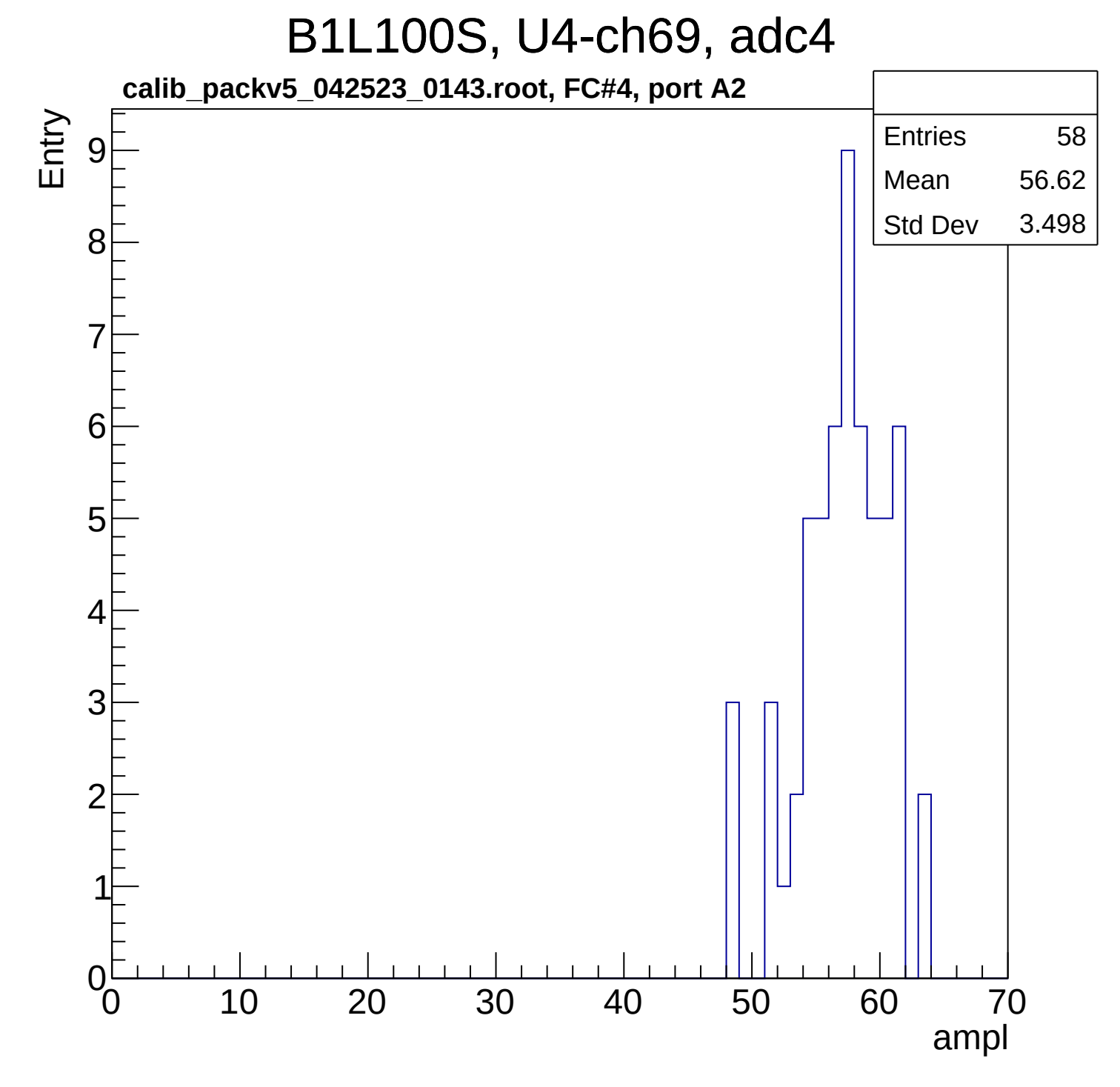

B1L100S, U4-ch68, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

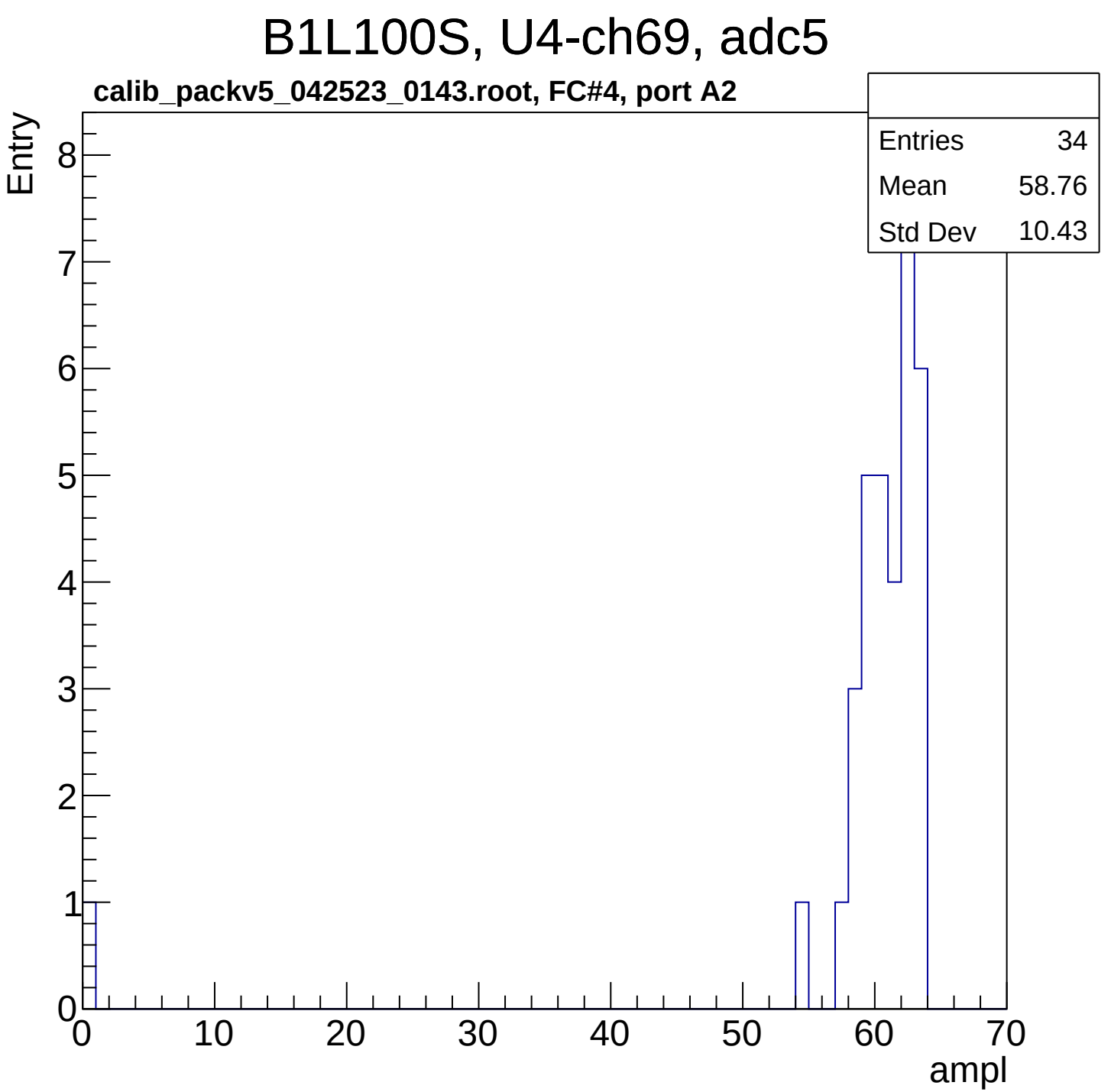

B1L100S, U4-ch69, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 31.15
Std Dev 3.663
Gaus mean : 31.3072
Gaus Width: 4.0159
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

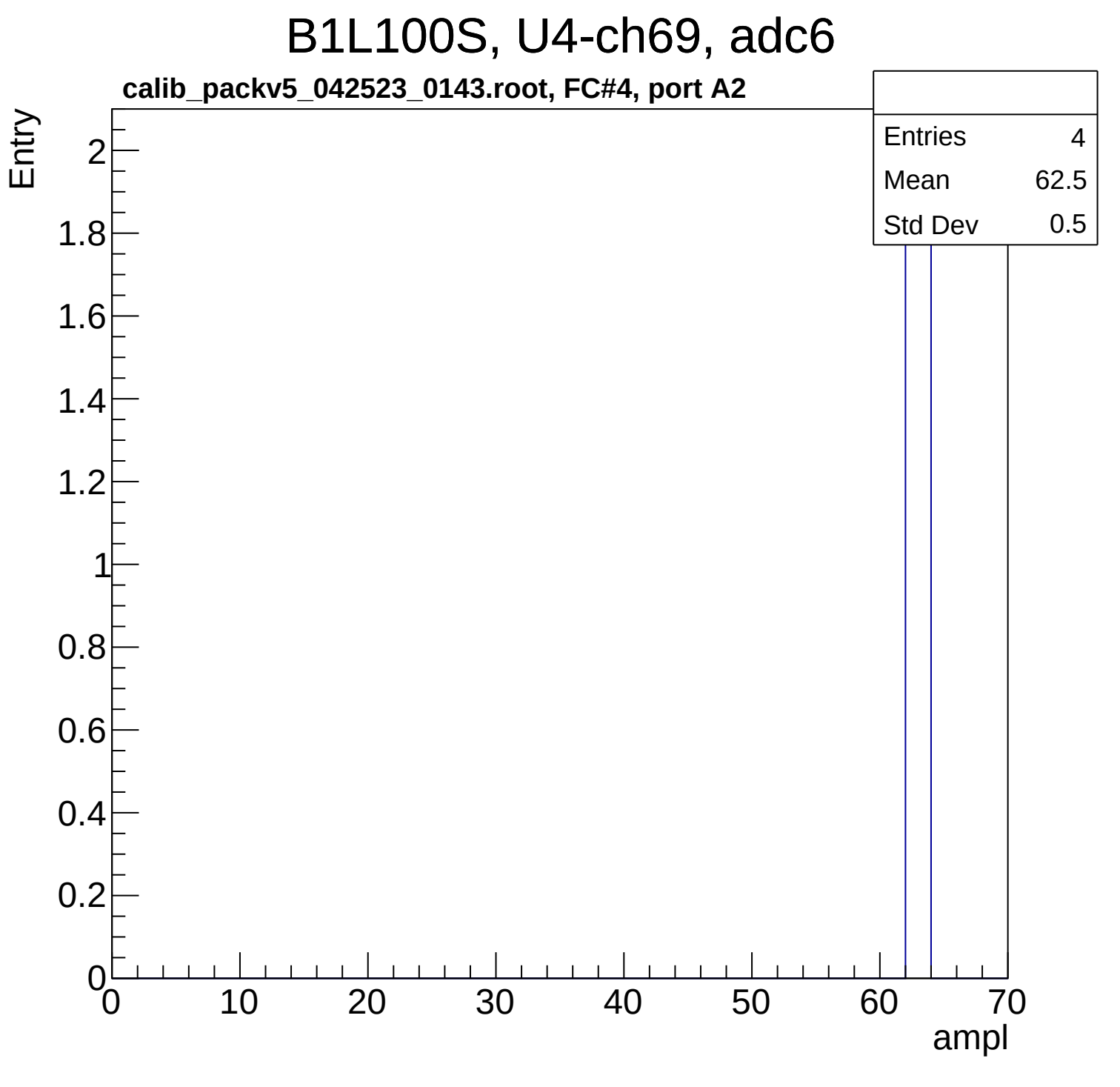

B1L100S, U4-ch69, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 37.94
Std Dev 4.029
Gaus mean : 38.3929
Gaus Width: 4.7670
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

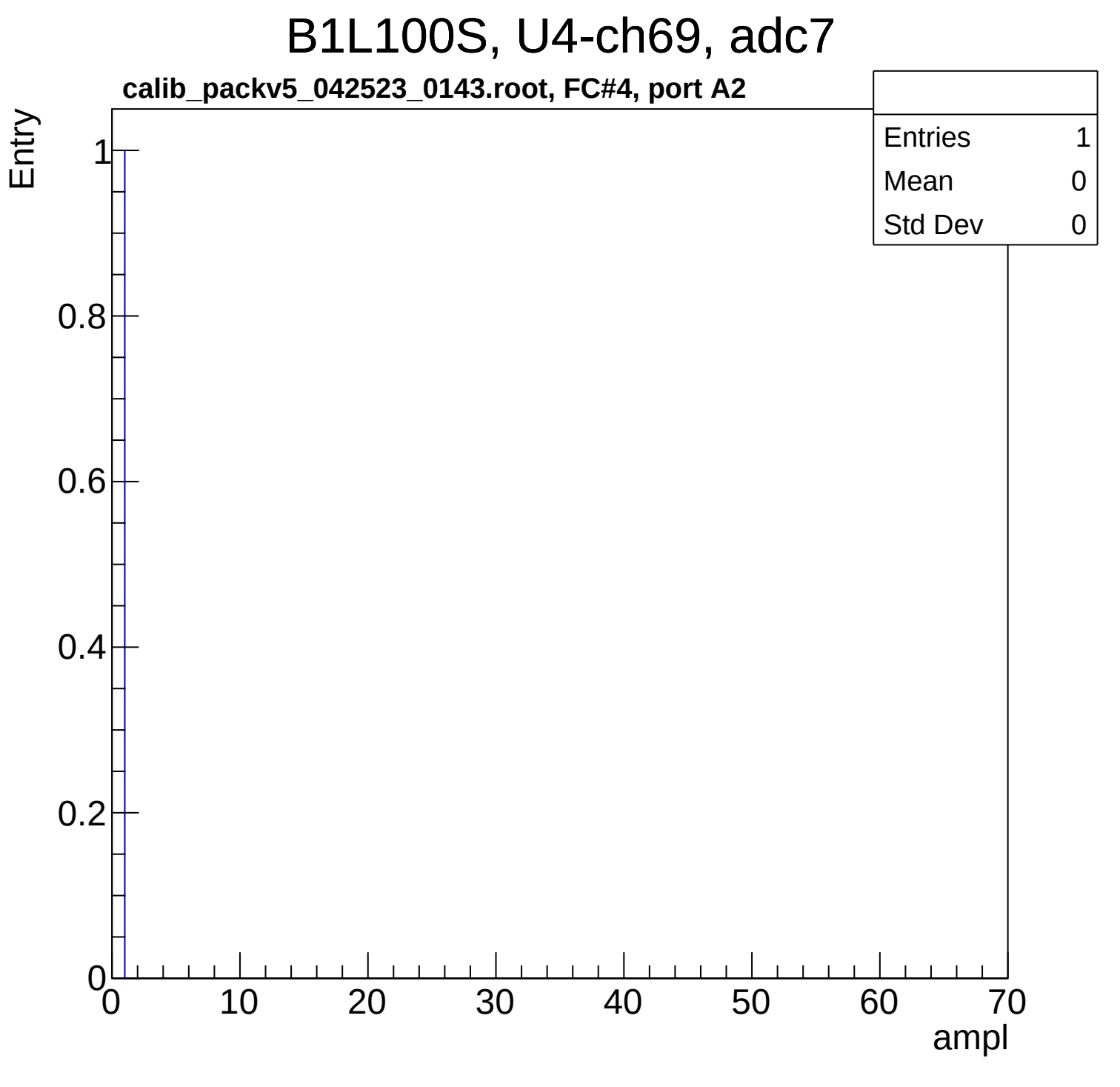

B1L100S, U4-ch69, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 43.44
Std Dev 3.452
Gaus mean : 43.9701
Gaus Width: 3.7676
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

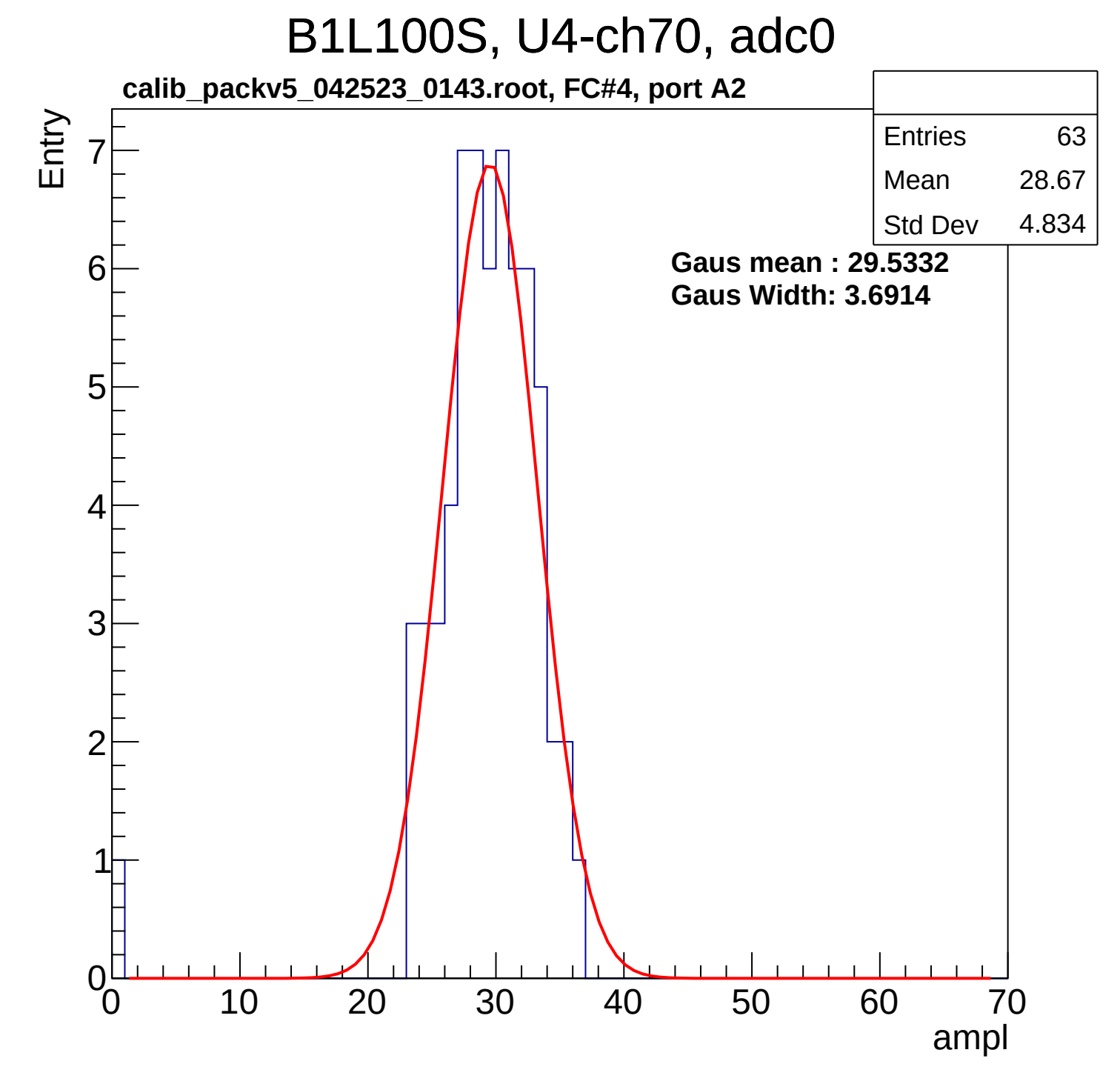

B1L100S, U4-ch69, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 50.72
Std Dev 3.146
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

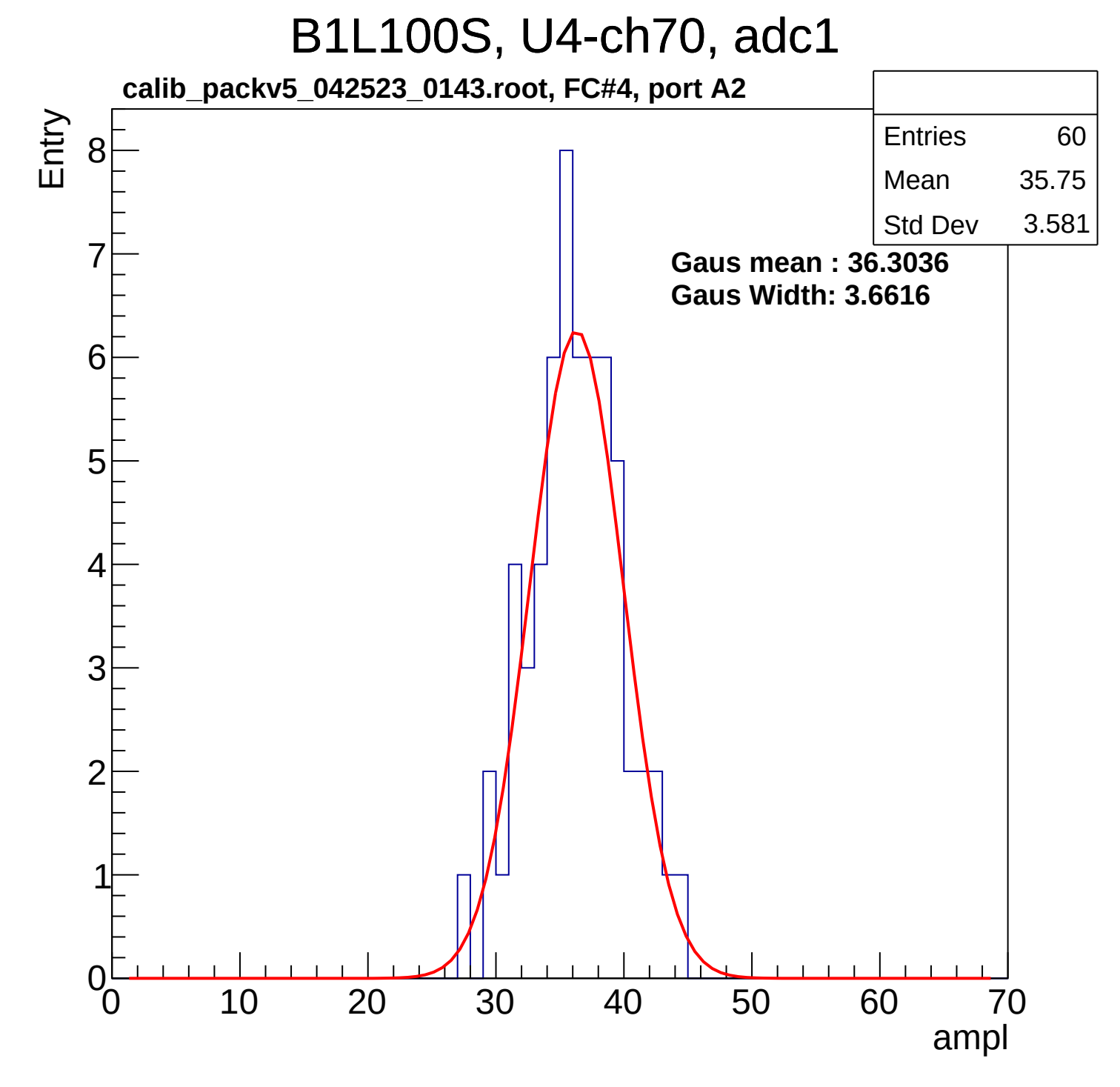

B1L100S, U4-ch69, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 56.62
Std Dev 3.498
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

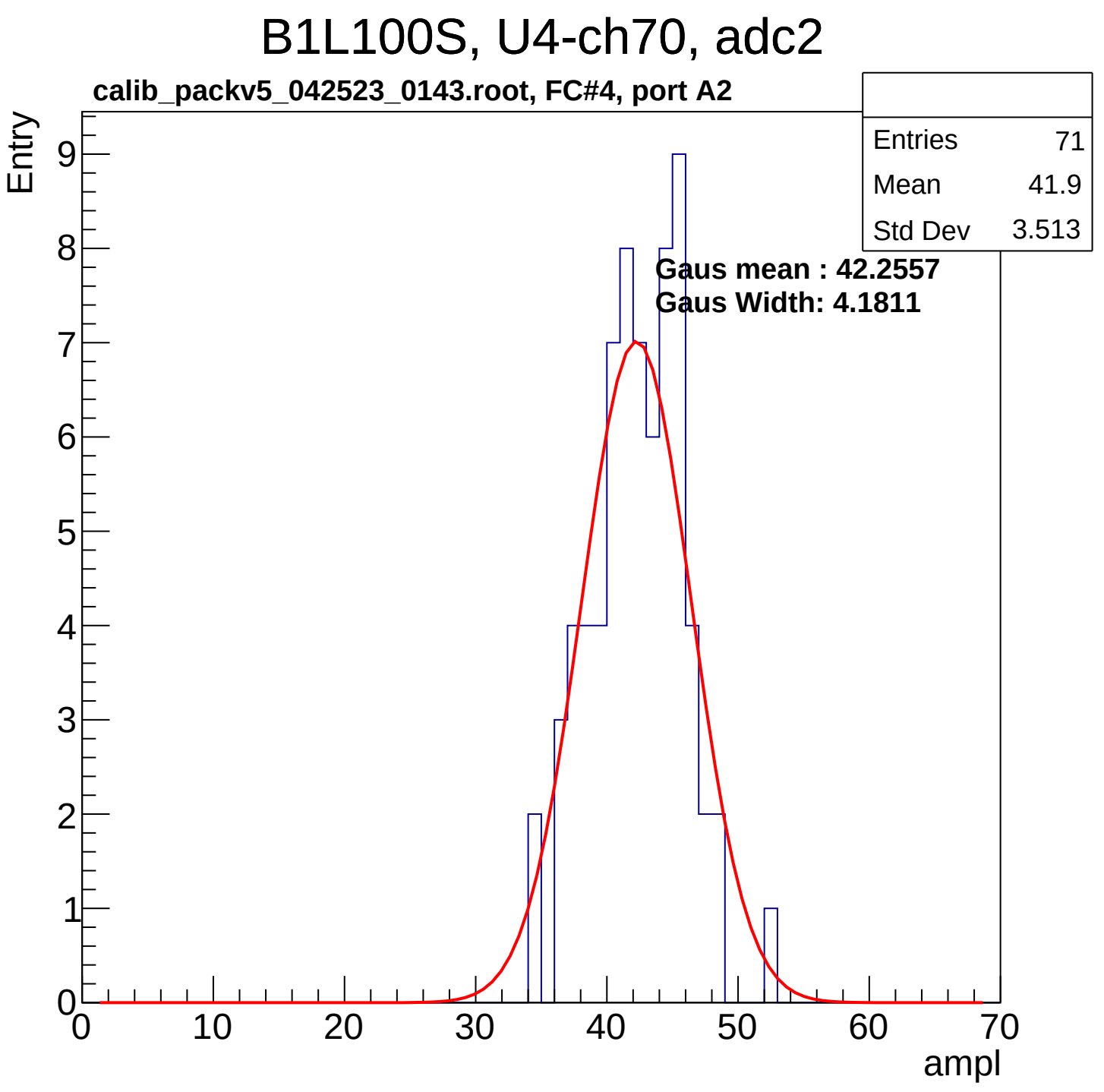

B1L100S, U4-ch69, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 34
Mean 58.76
Std Dev 10.43
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

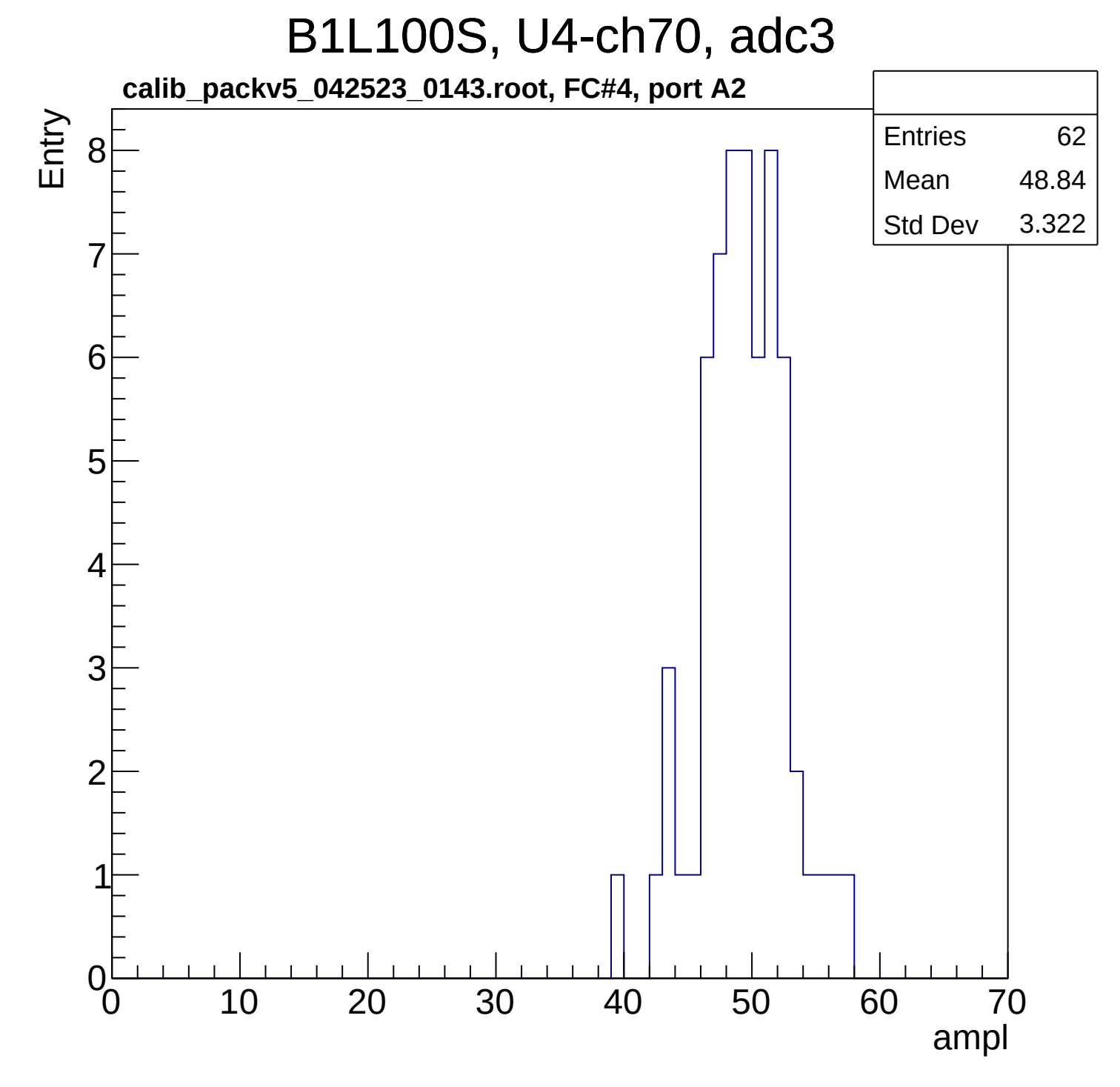

B1L100S, U4-ch69, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 62.5
Std Dev 0.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

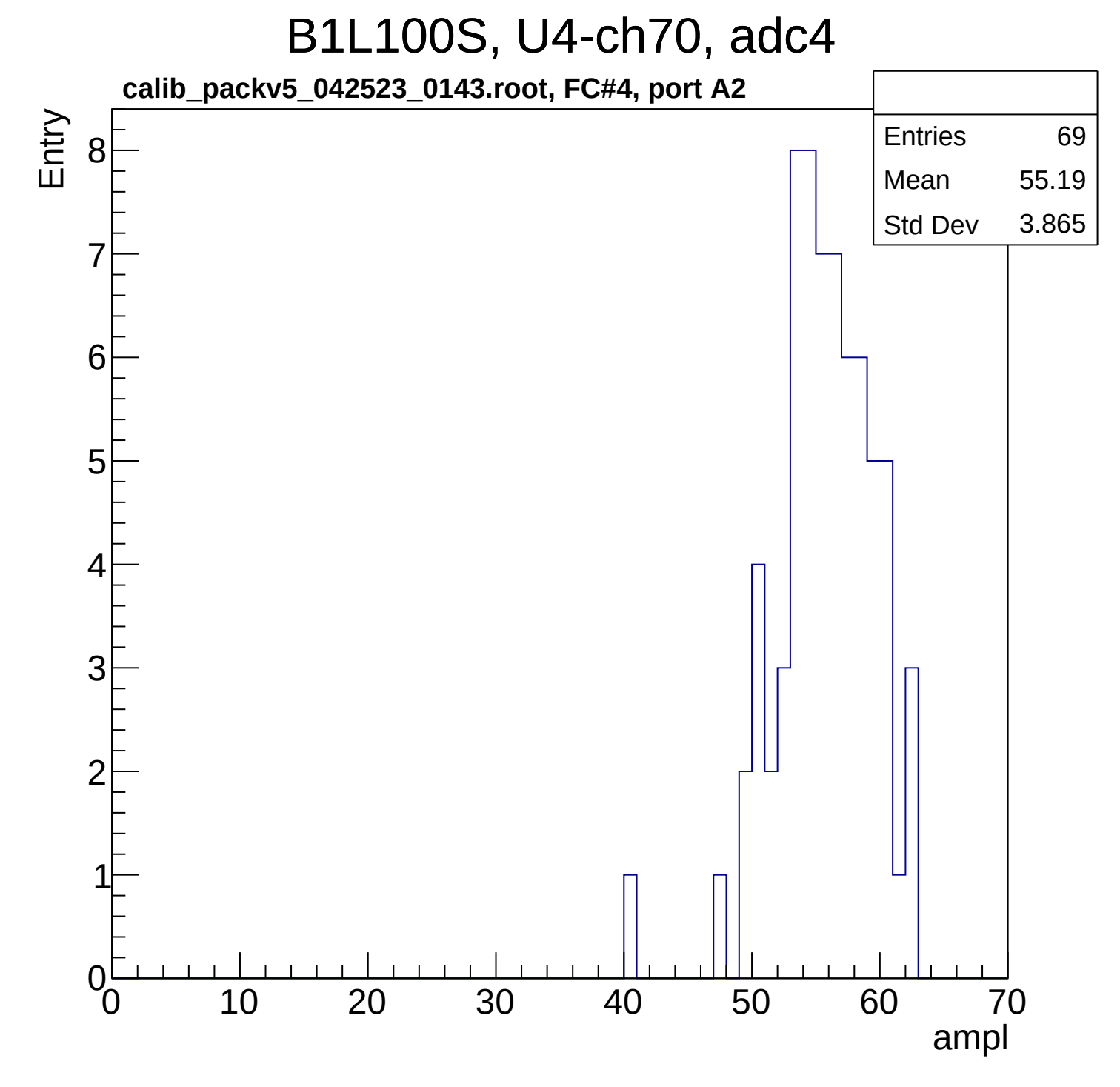

B1L100S, U4-ch69, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

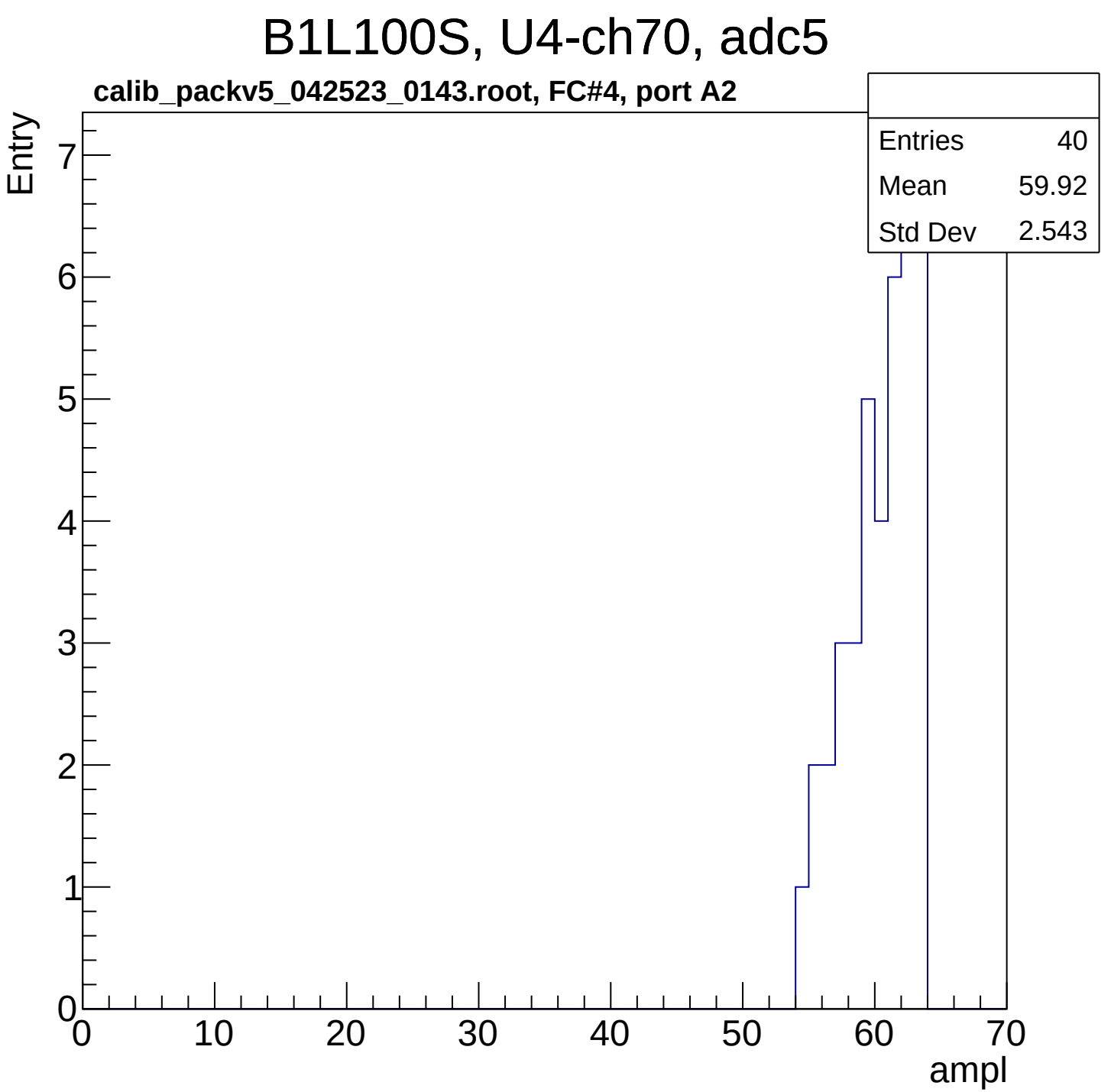

B1L100S, U4-ch70, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 28.67
Std Dev 4.834
Gaus mean : 29.5332
Gaus Width: 3.6914
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

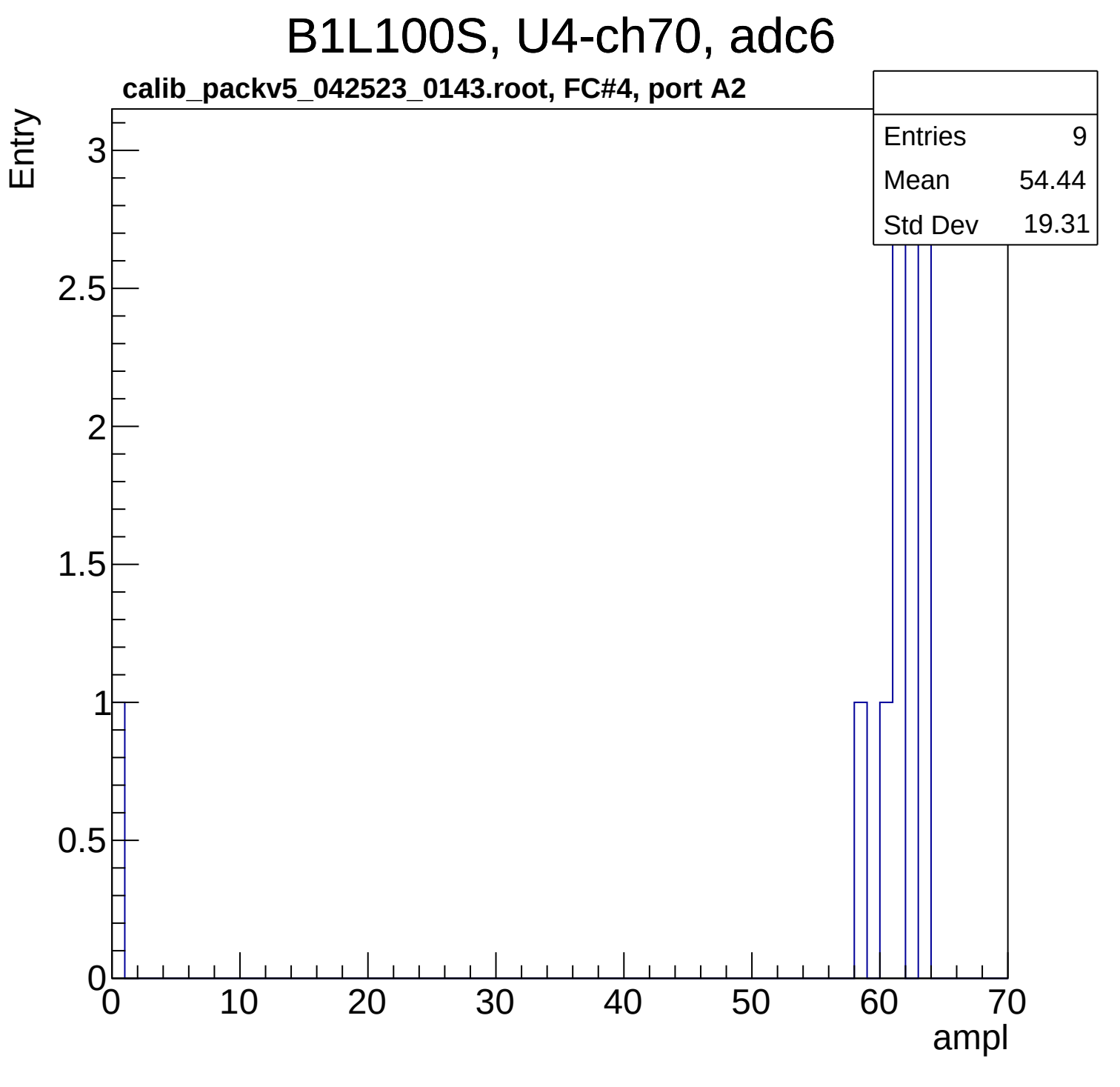

B1L100S, U4-ch70, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 35.75
Std Dev 3.581
Gaus mean : 36.3036
Gaus Width: 3.6616
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

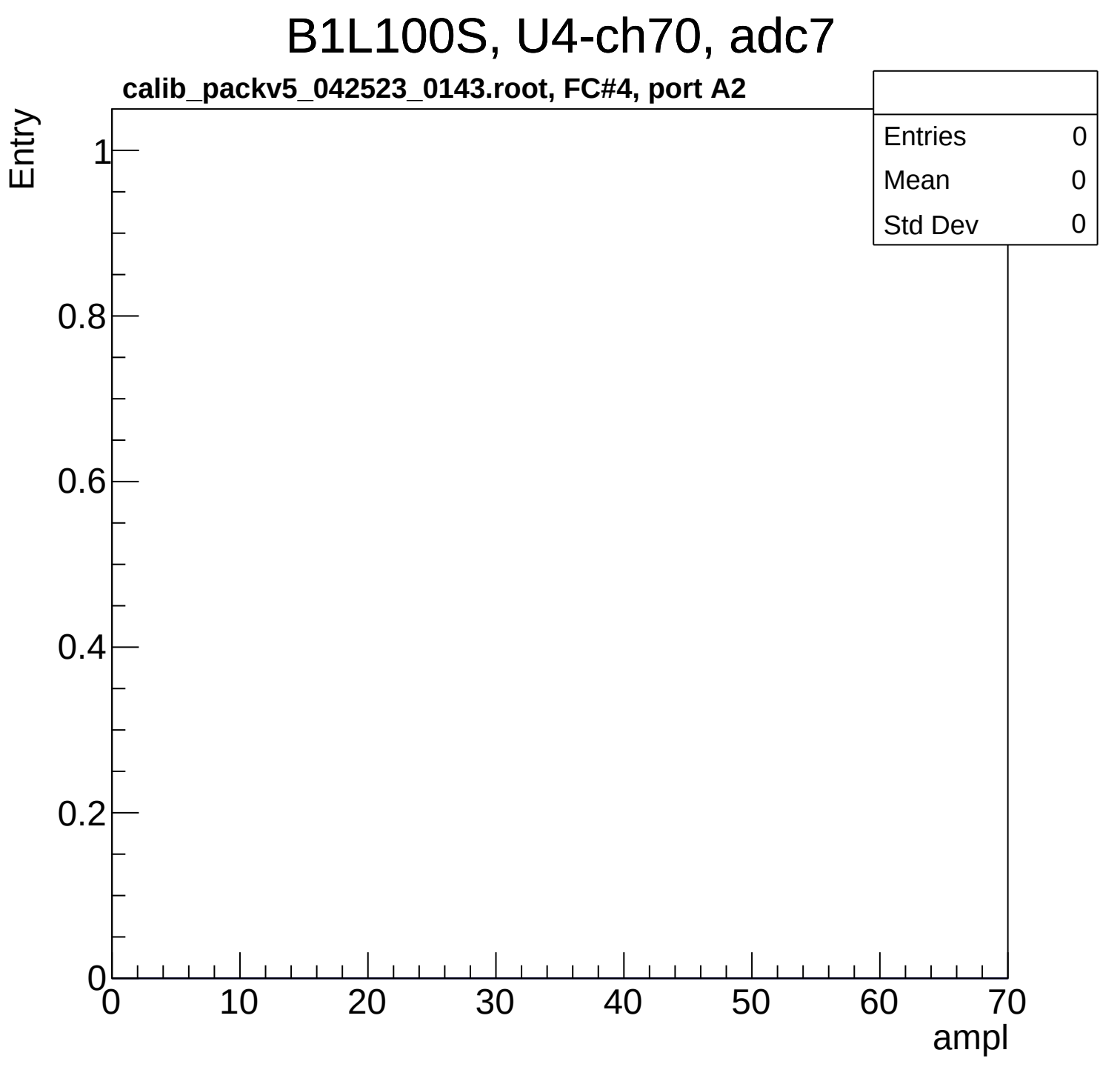

B1L100S, U4-ch70, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 41.9
Std Dev 3.513
Gaus mean : 42.2557
Gaus Width: 4.1811
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

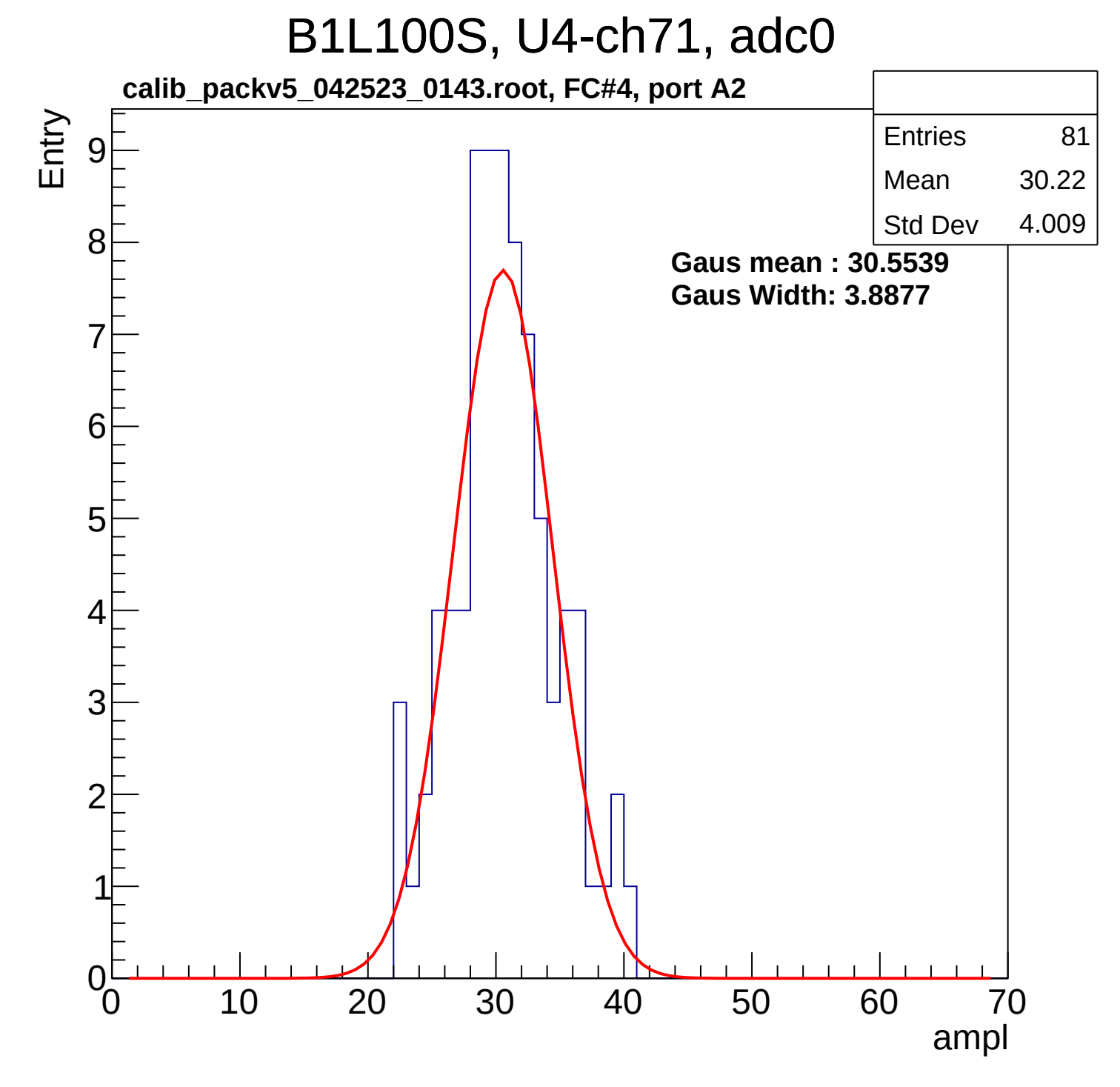

B1L100S, U4-ch70, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 48.84
Std Dev 3.322
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

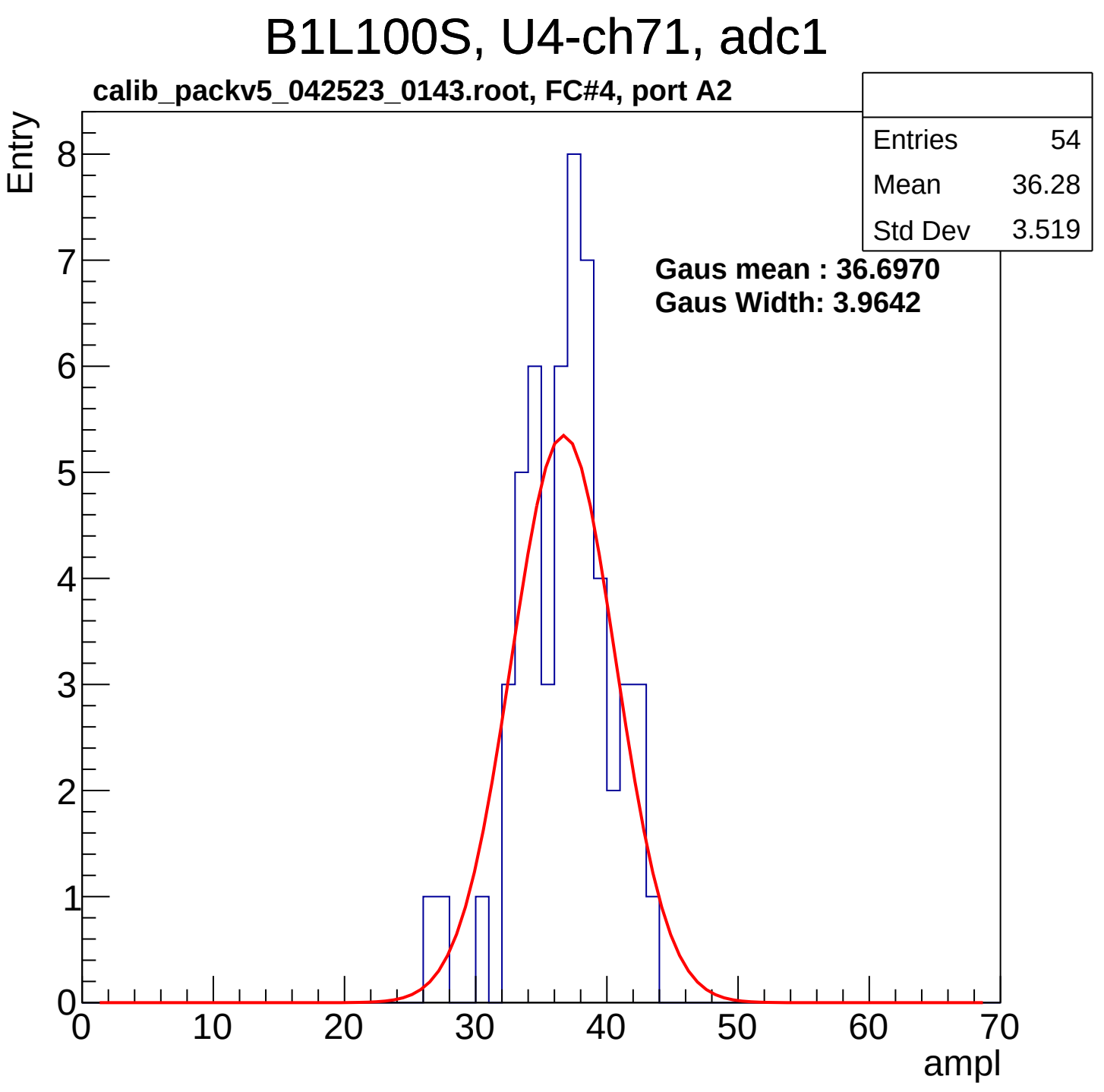

B1L100S, U4-ch70, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 55.19
Std Dev 3.865
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

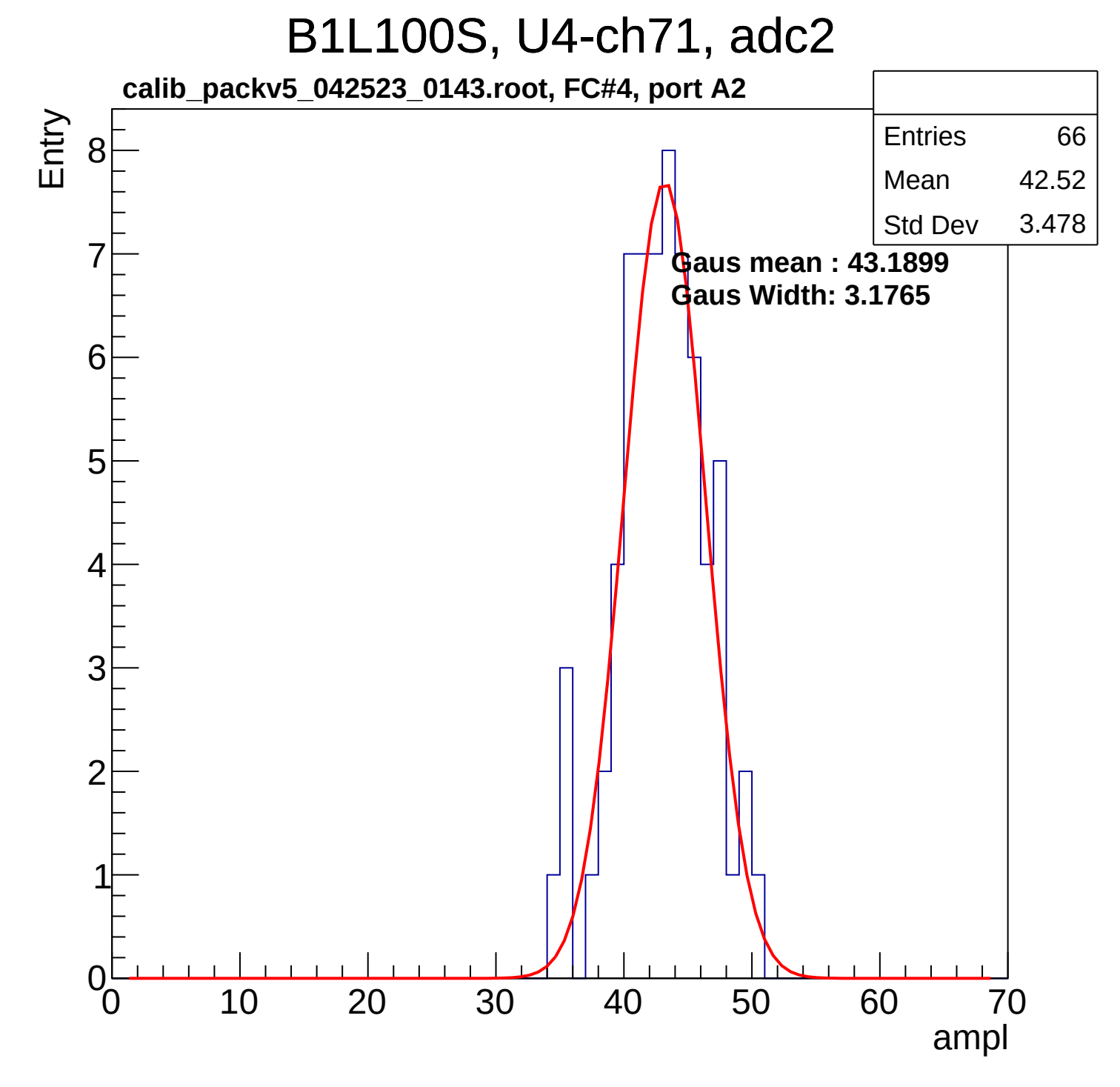

B1L100S, U4-ch70, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 40
Mean 59.92
Std Dev 2.543
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

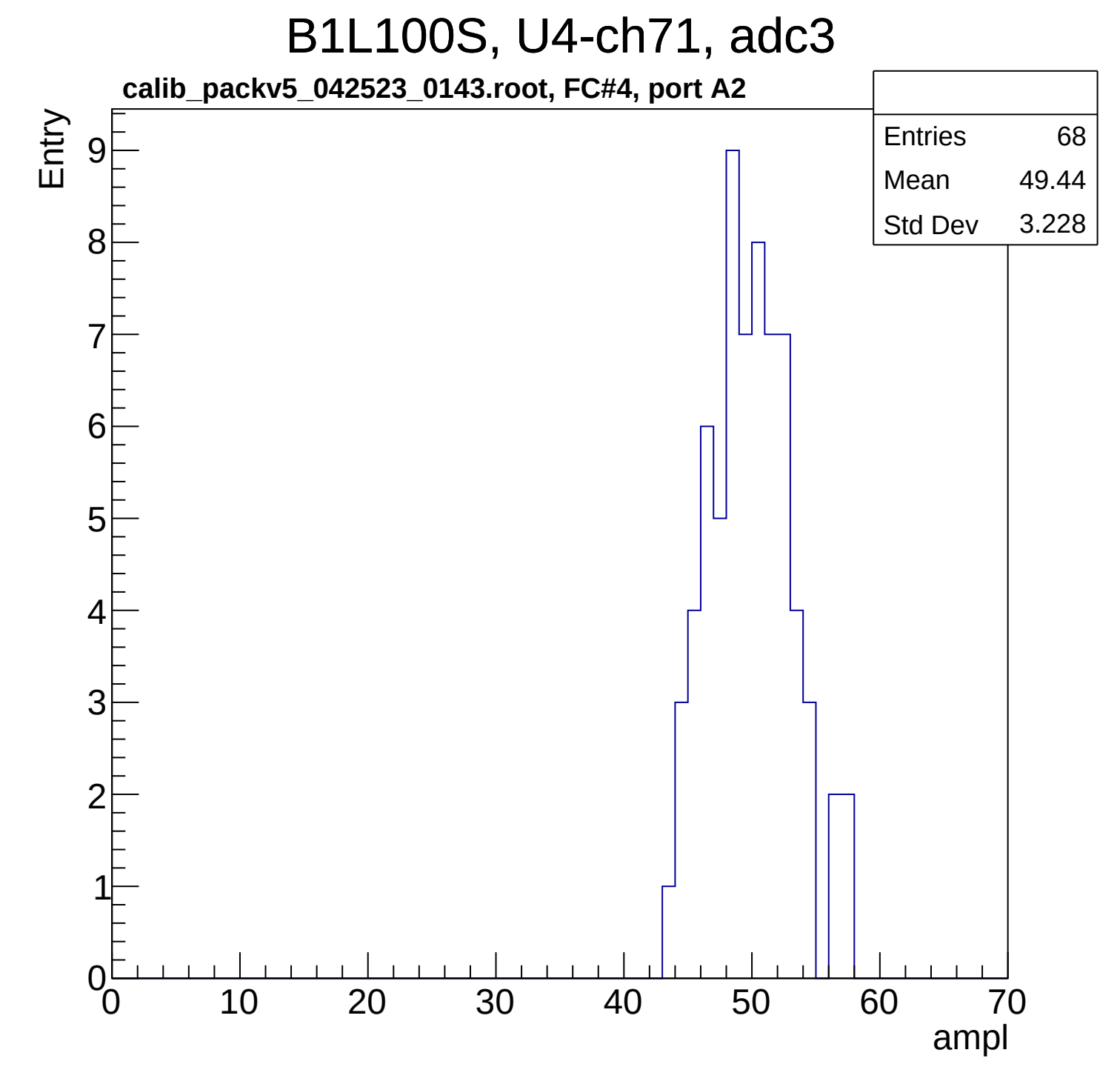

B1L100S, U4-ch70, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 54.44
Std Dev 19.31
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

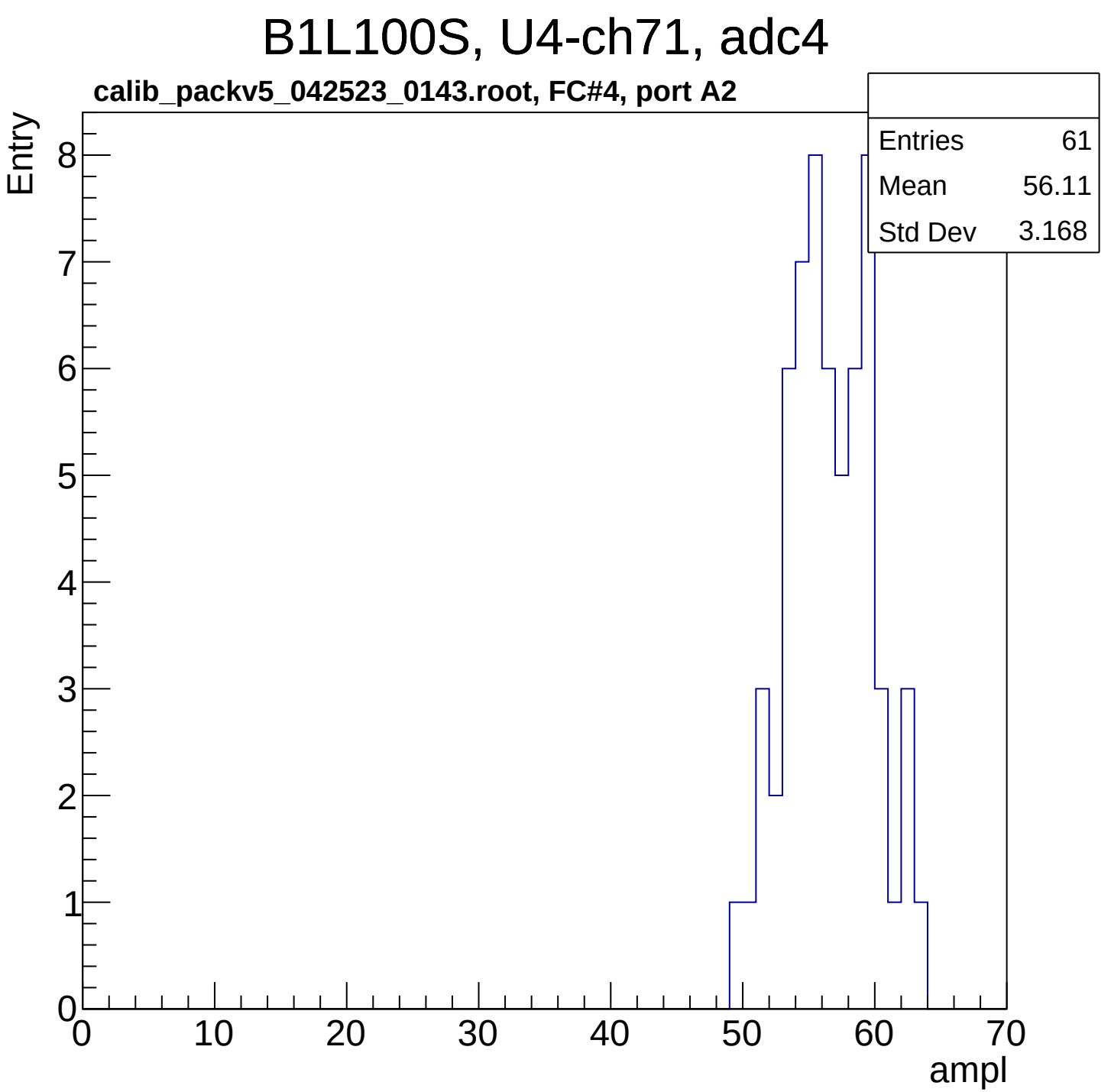

B1L100S, U4-ch70, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

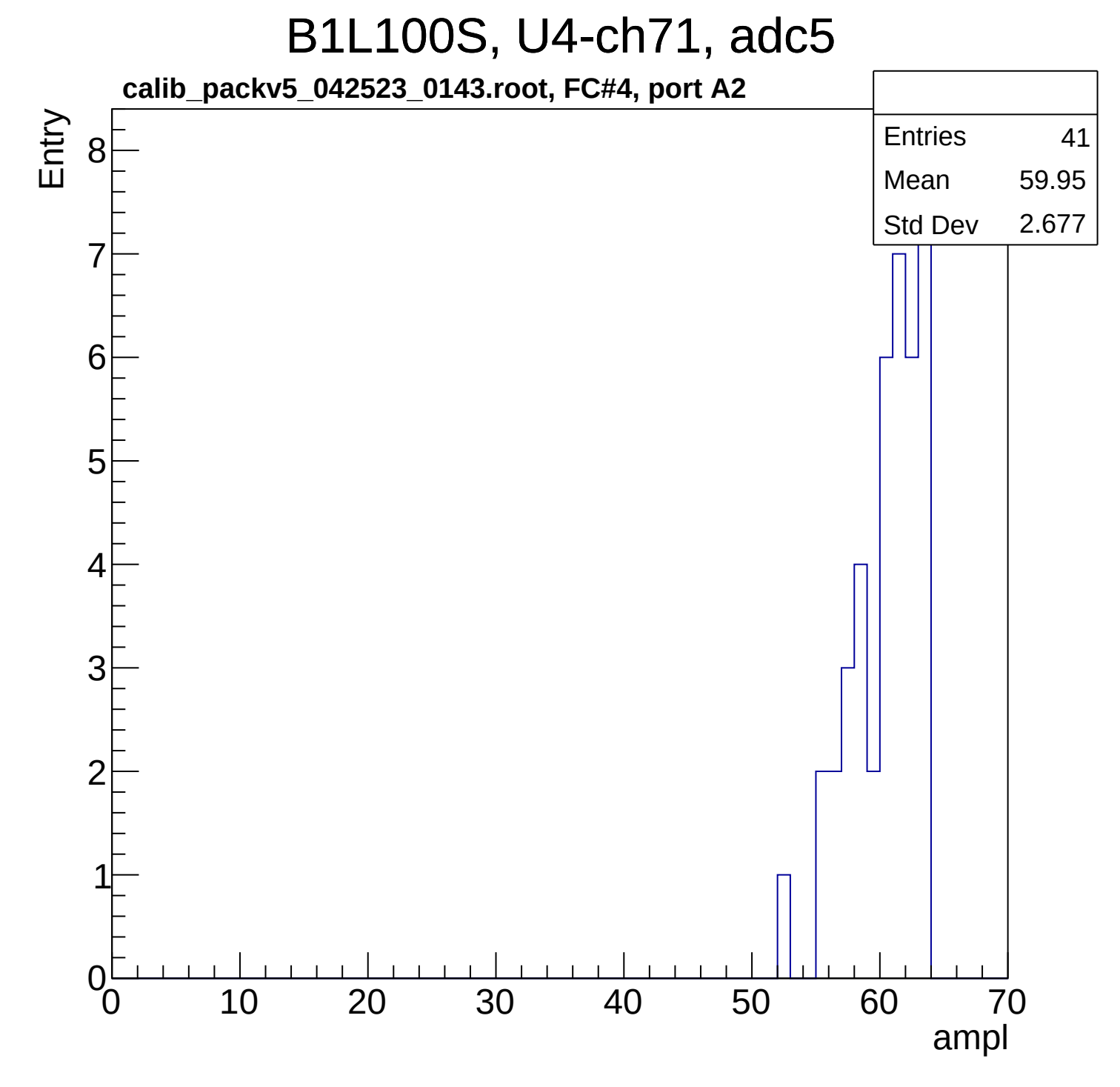

B1L100S, U4-ch71, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 30.22
Std Dev 4.009
Gaus mean : 30.5539
Gaus Width: 3.8877
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

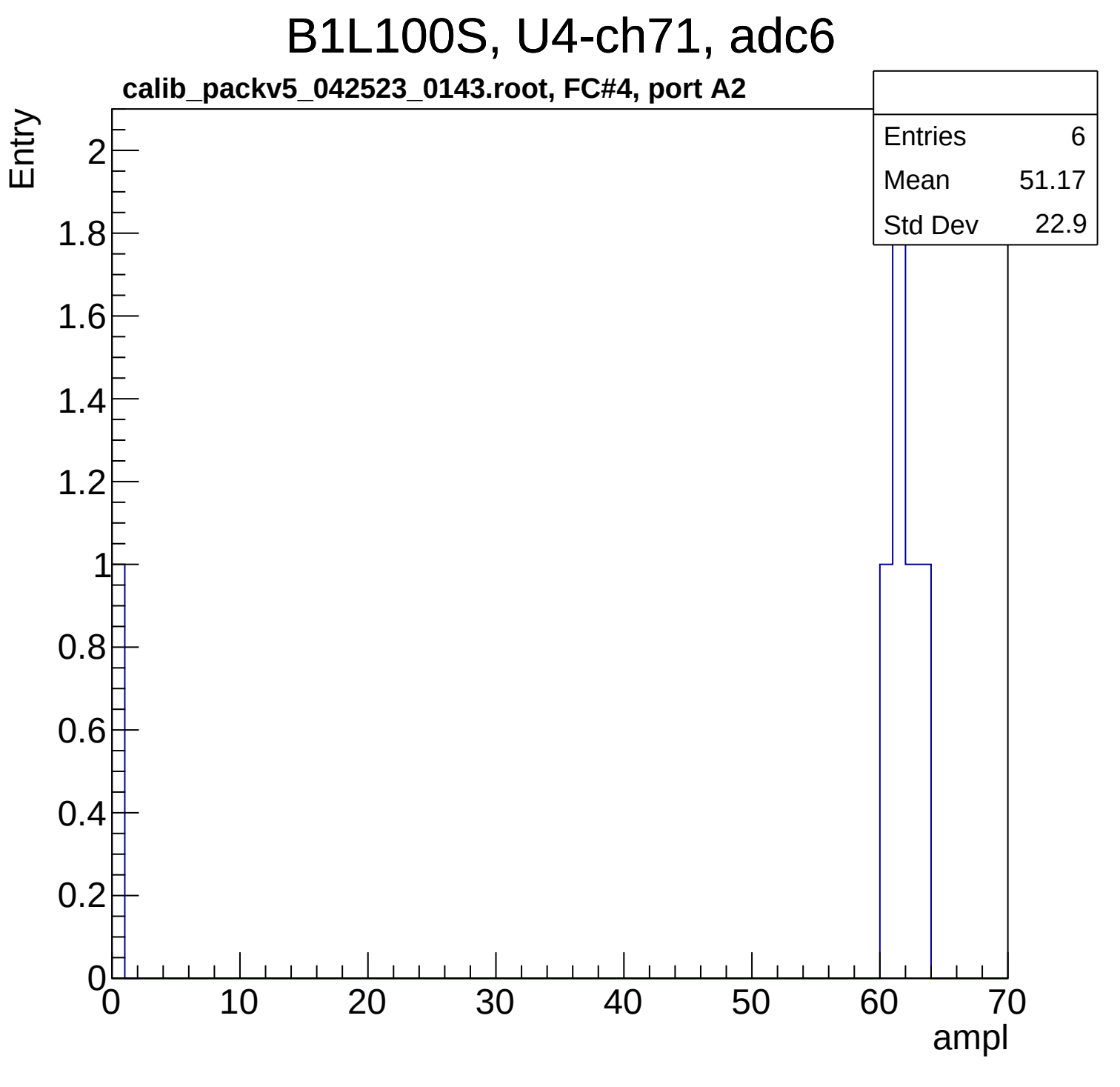

B1L100S, U4-ch71, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 36.28
Std Dev 3.519
Gaus mean : 36.6970
Gaus Width: 3.9642
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

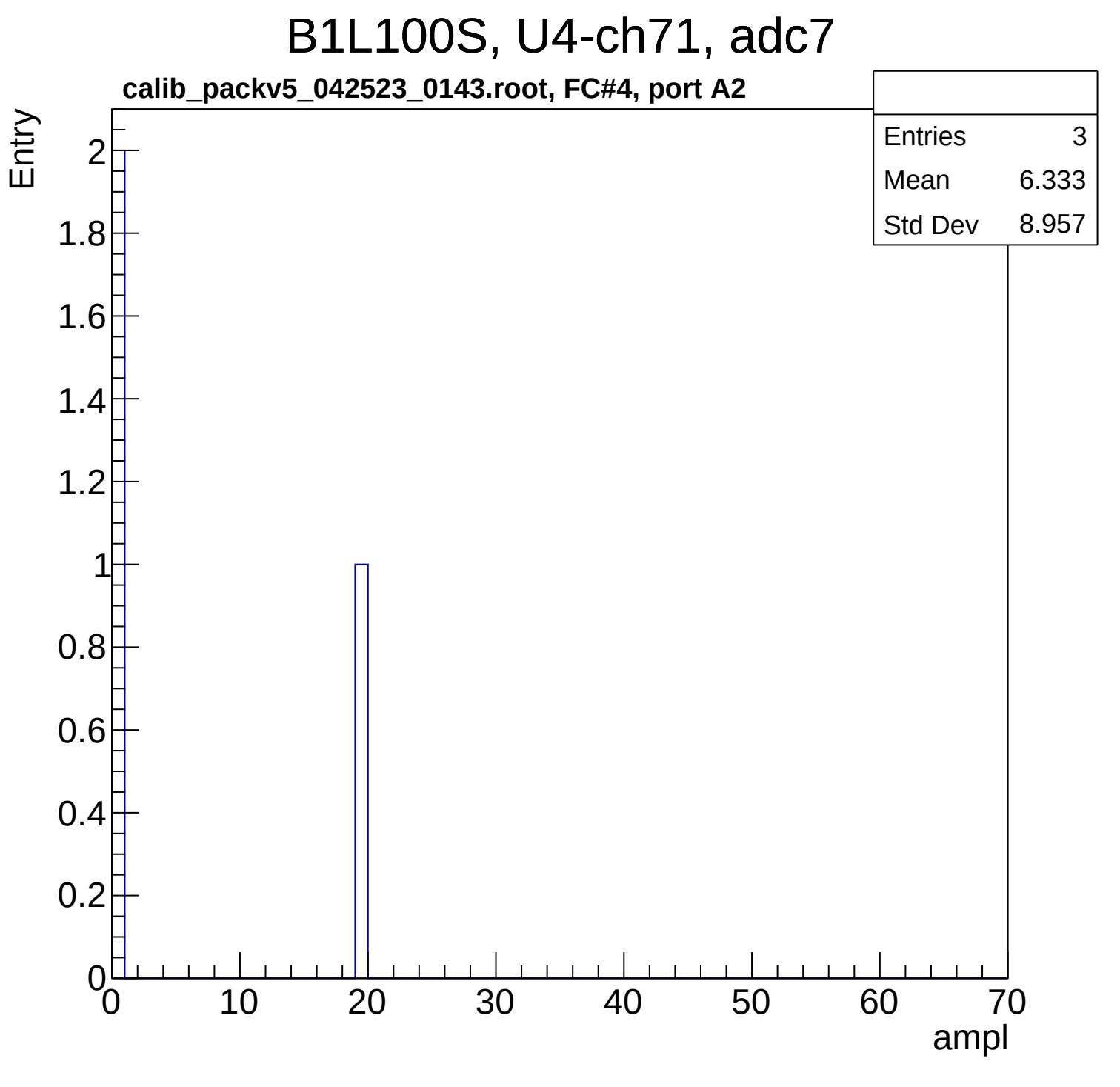

B1L100S, U4-ch71, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 42.52
Std Dev 3.478
Gaus mean : 43.1899
Gaus Width: 3.1765
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

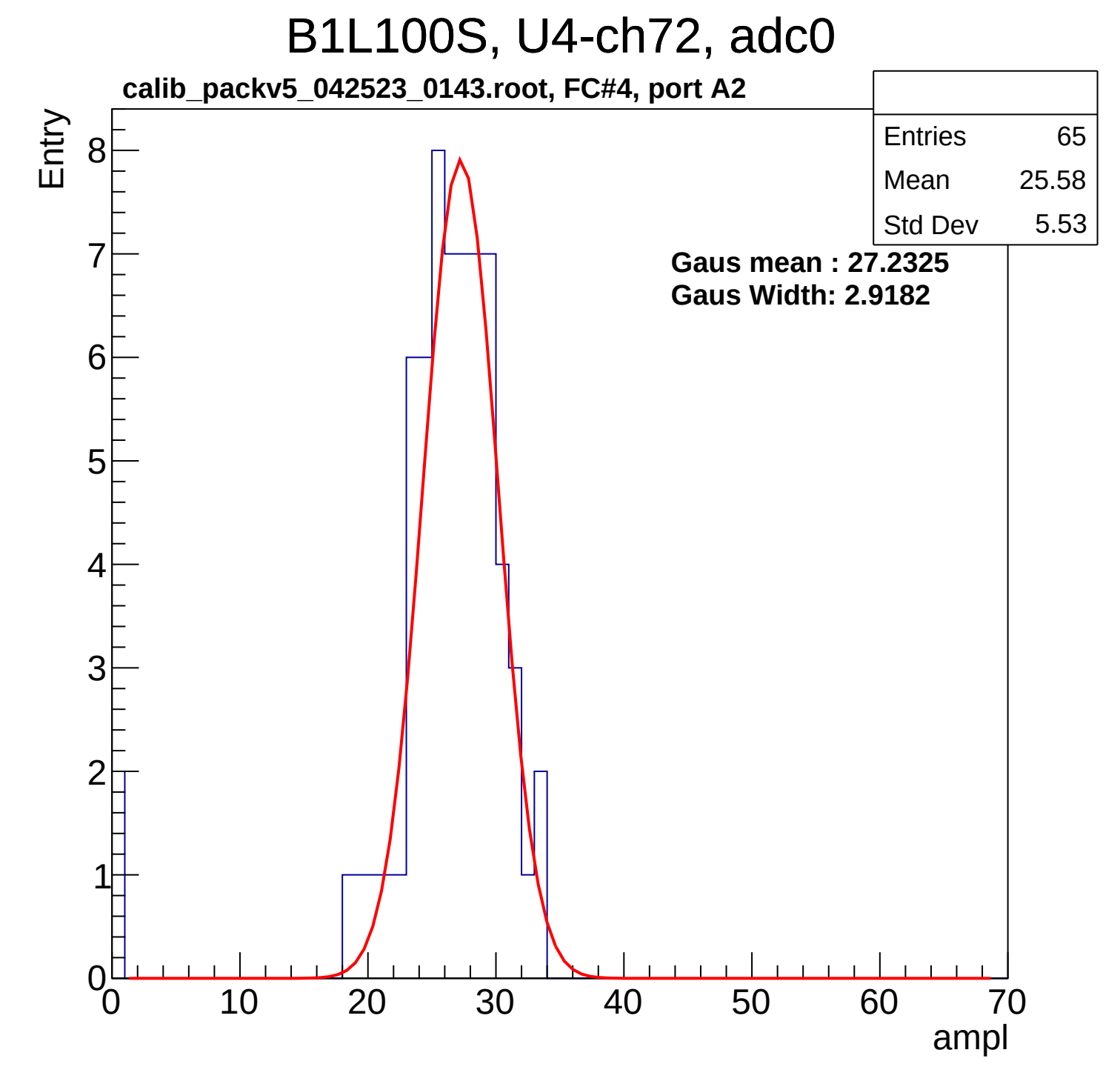

B1L100S, U4-ch71, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 49.44
Std Dev 3.228
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

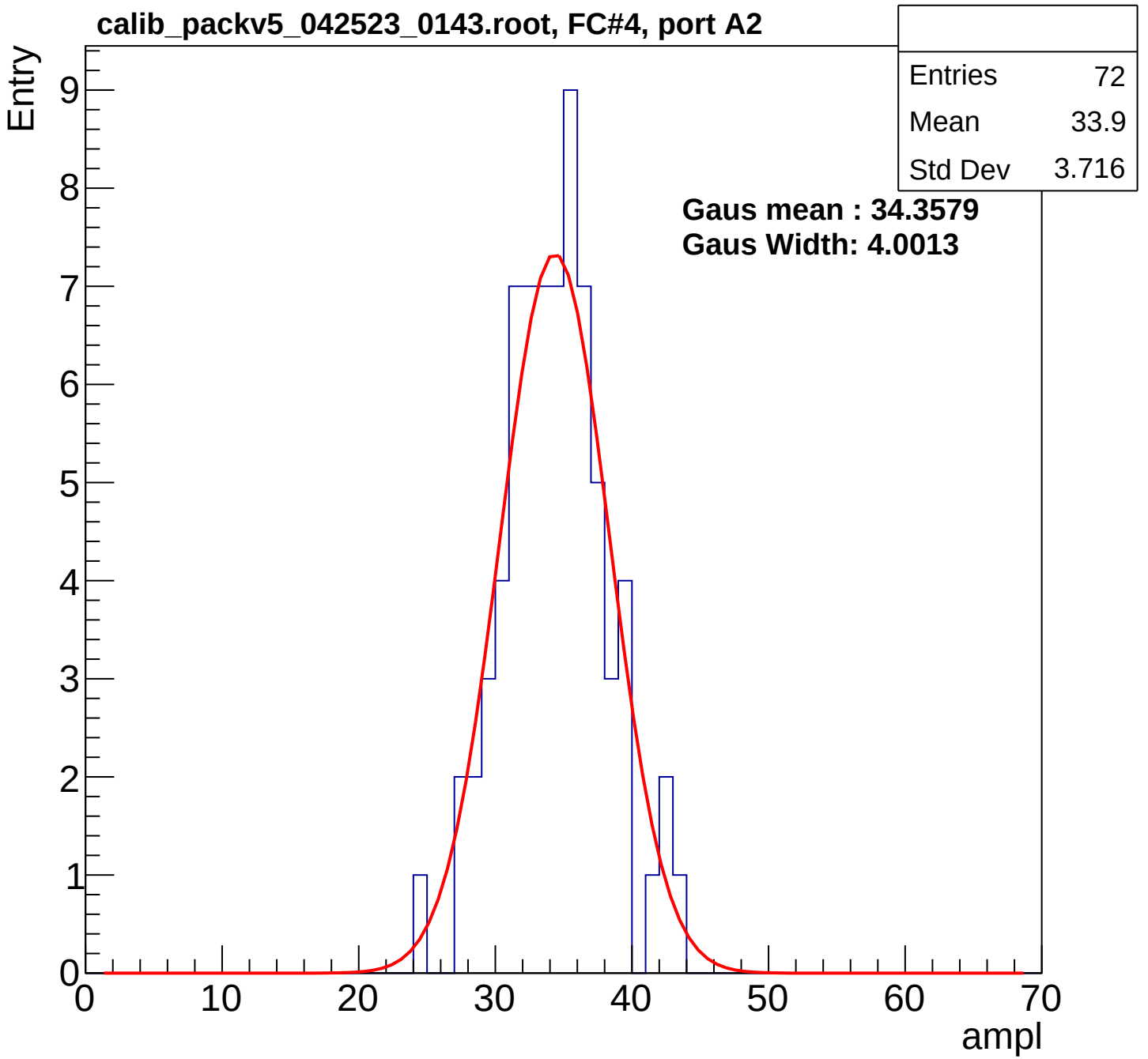

B1L100S, U4-ch71, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 56.11
Std Dev 3.168
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

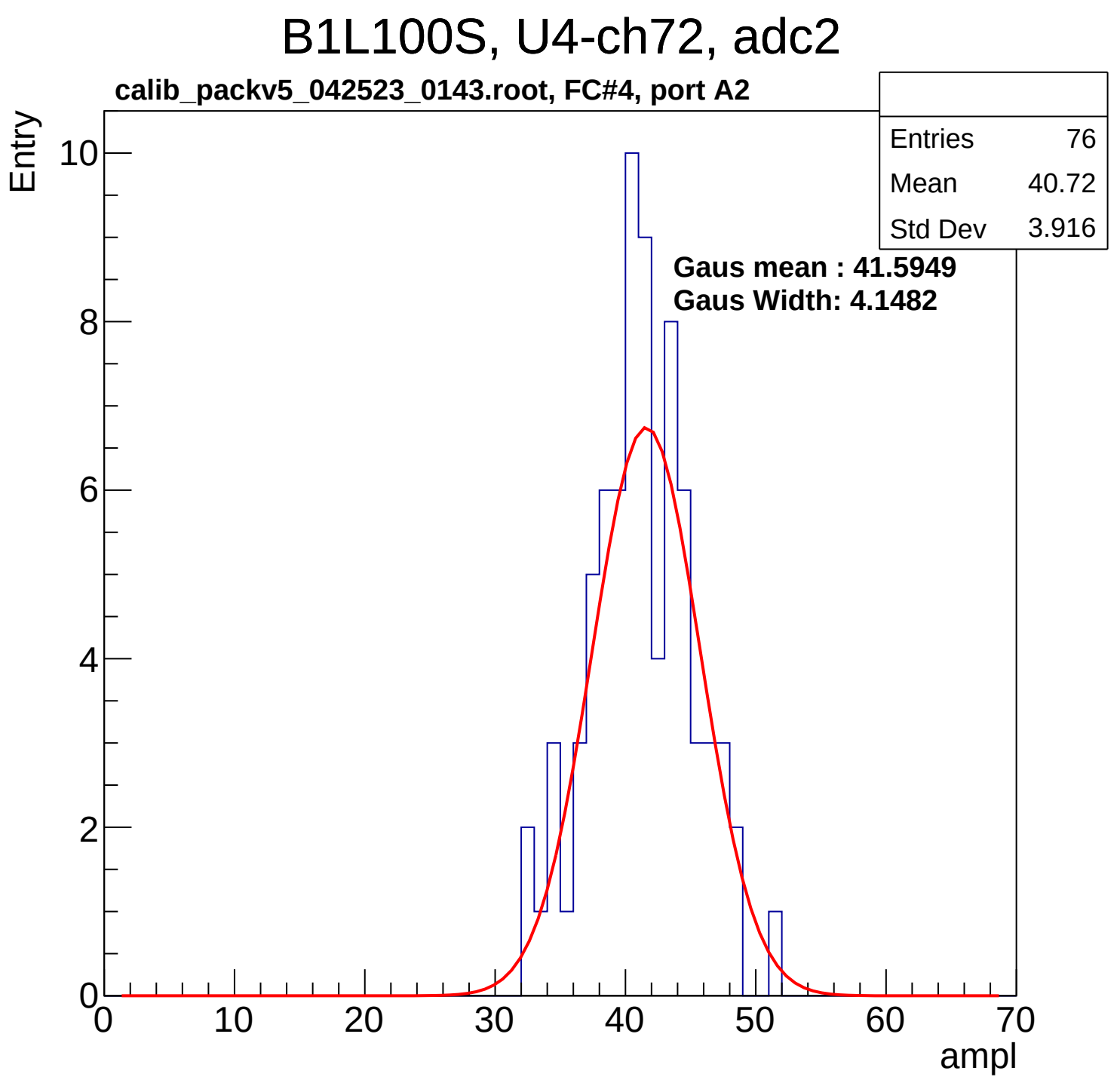

B1L100S, U4-ch71, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 41
Mean 59.95
Std Dev 2.677
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

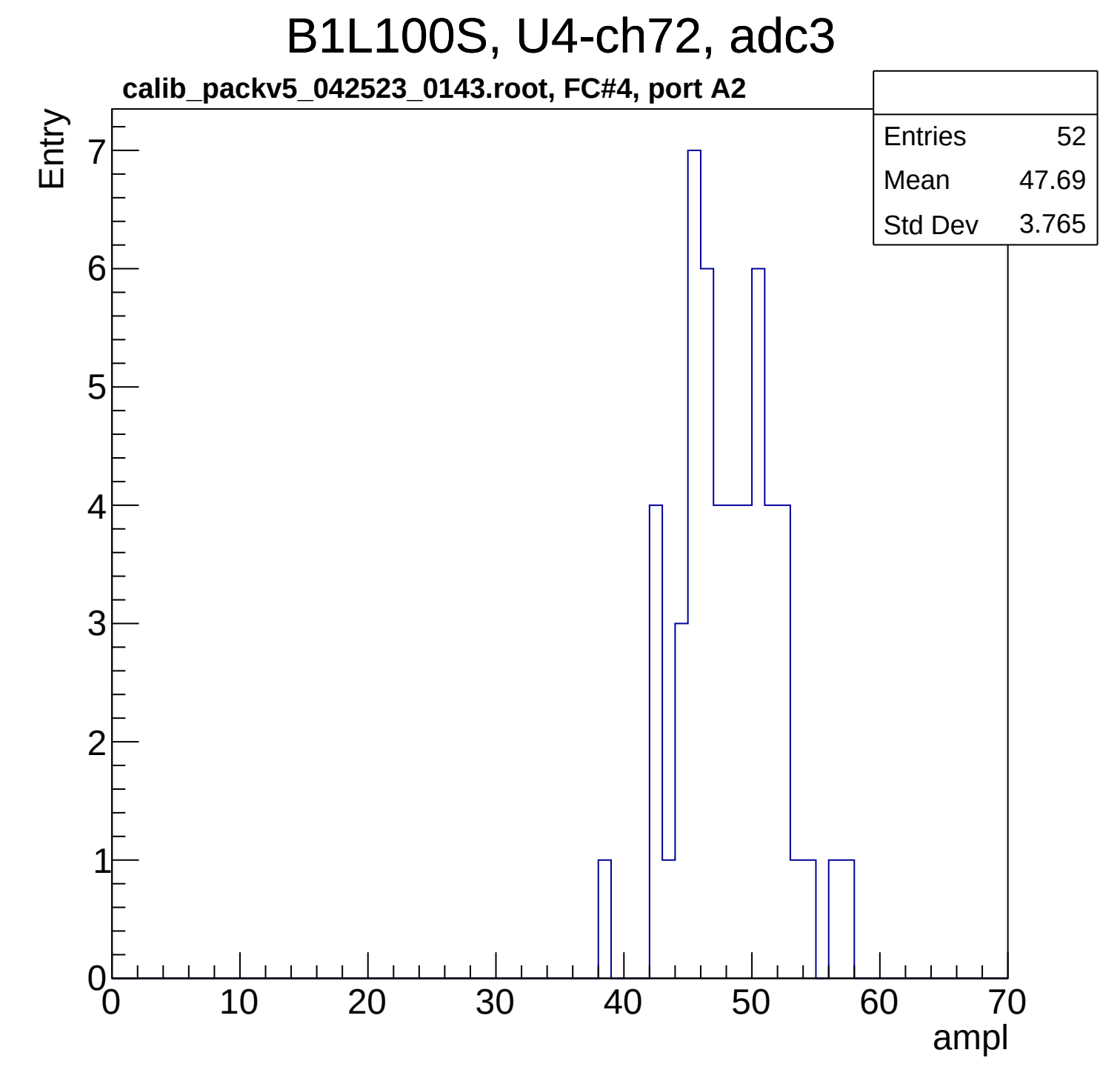

B1L100S, U4-ch71, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 51.17
Std Dev 22.9
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

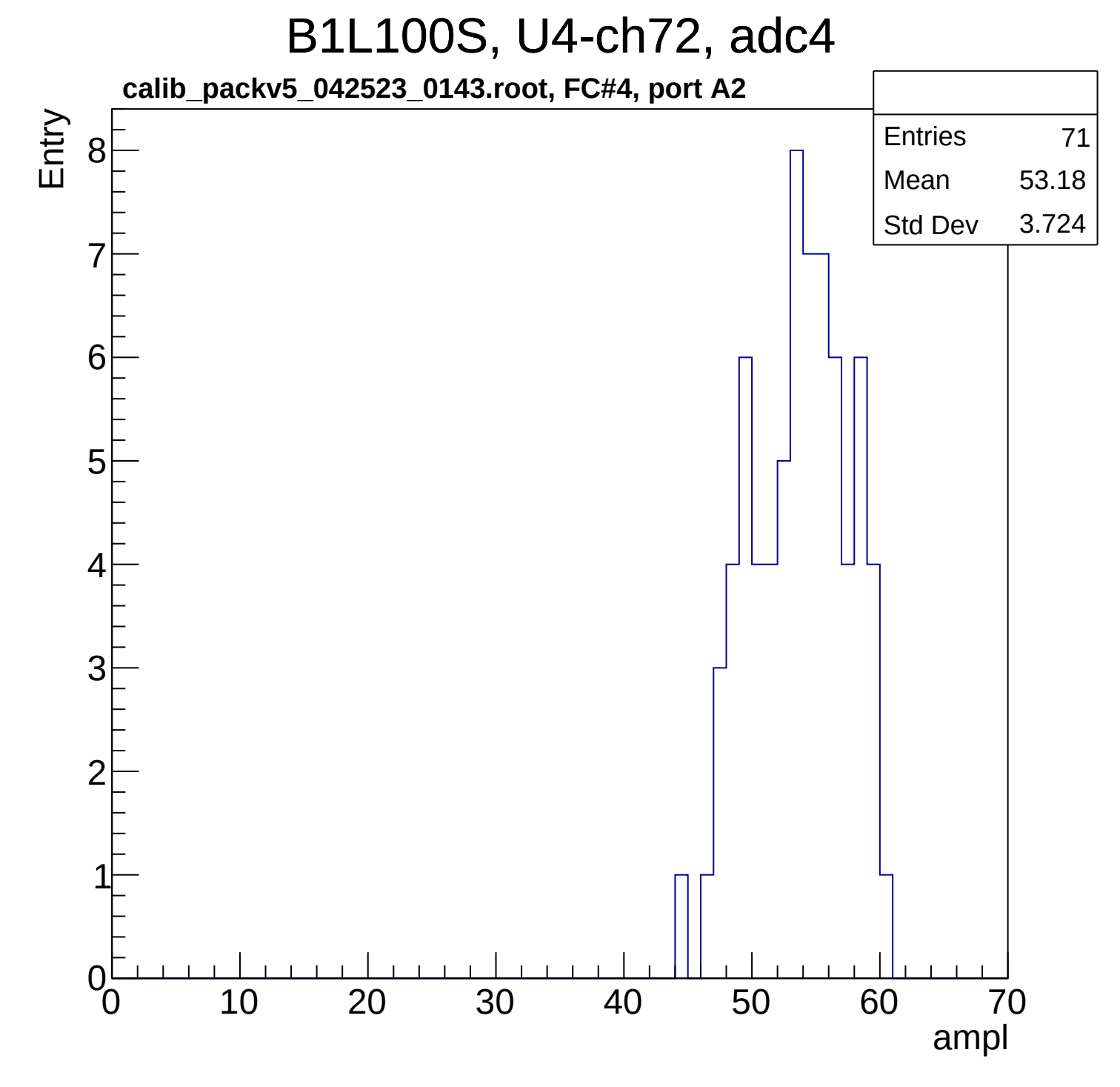

B1L100S, U4-ch71, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 6.333
Std Dev 8.957
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

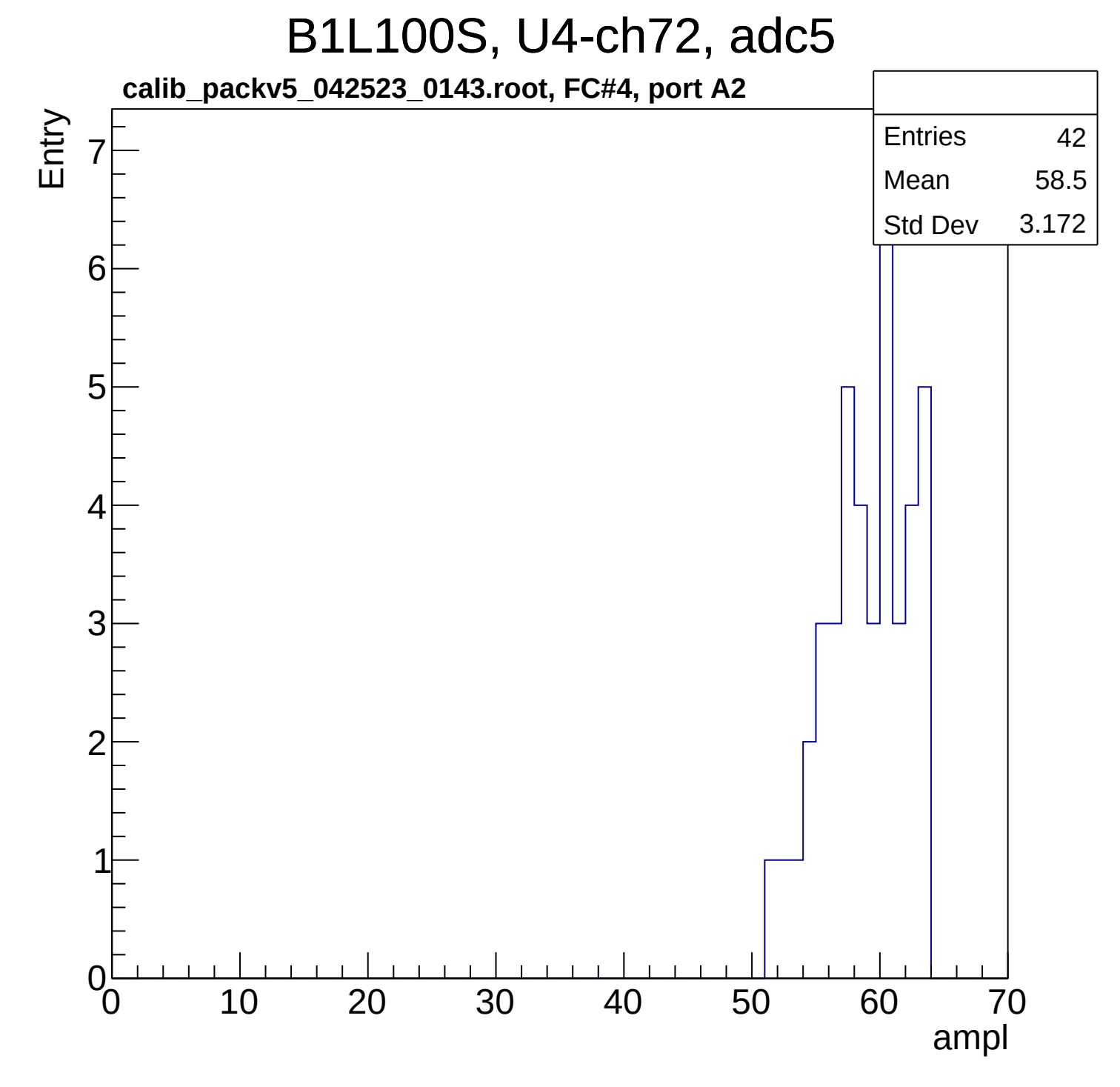

B1L100S, U4-ch72, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 25.58
Std Dev 5.53
Gaus mean : 27.2325
Gaus Width: 2.9182
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

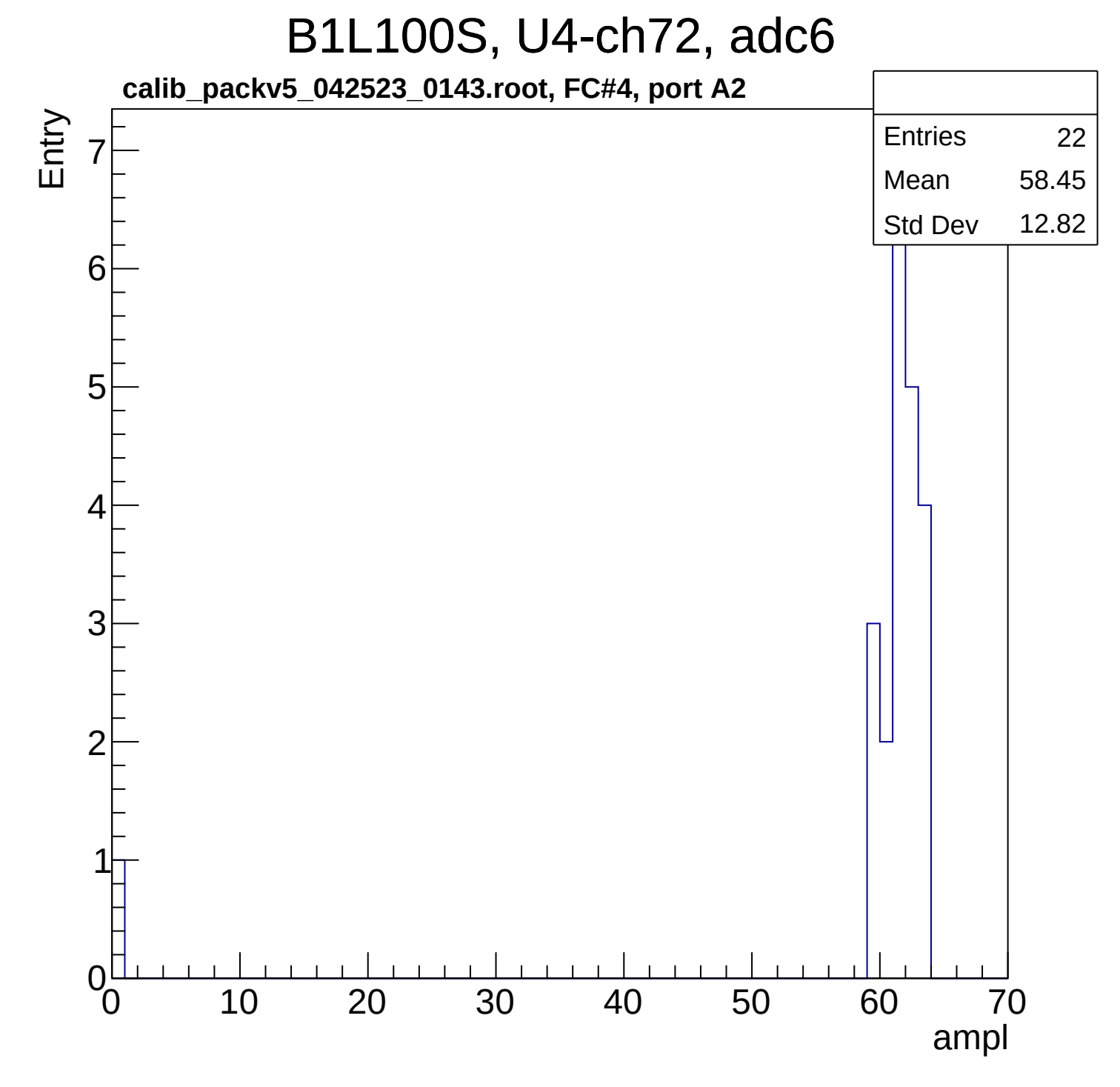

B1L100S, U4-ch72, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 33.9
Std Dev 3.716
Gaus mean : 34.3579
Gaus Width: 4.0013
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

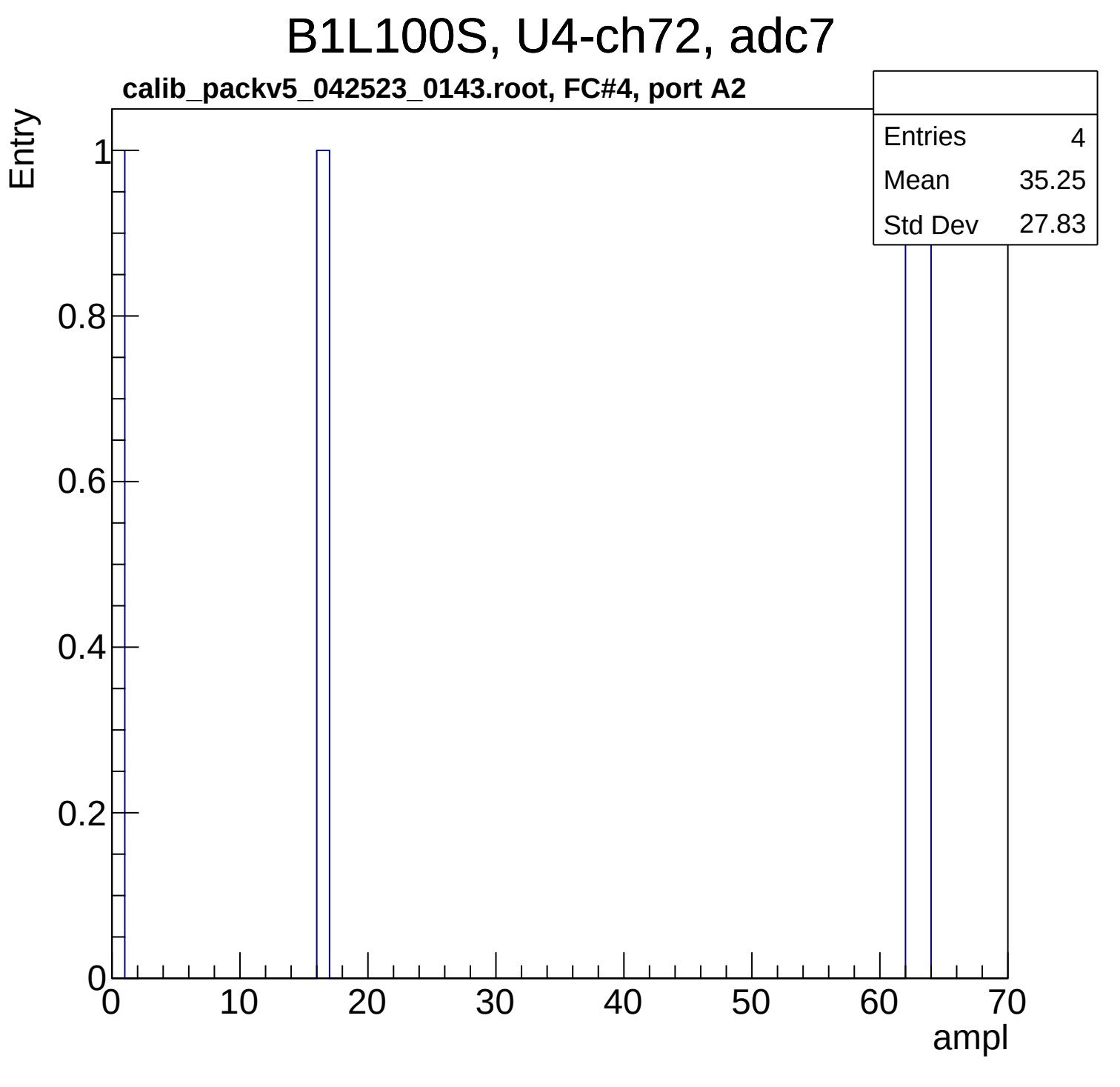

B1L100S, U4-ch72, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 40.72
Std Dev 3.916
Gaus mean : 41.5949
Gaus Width: 4.1482
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

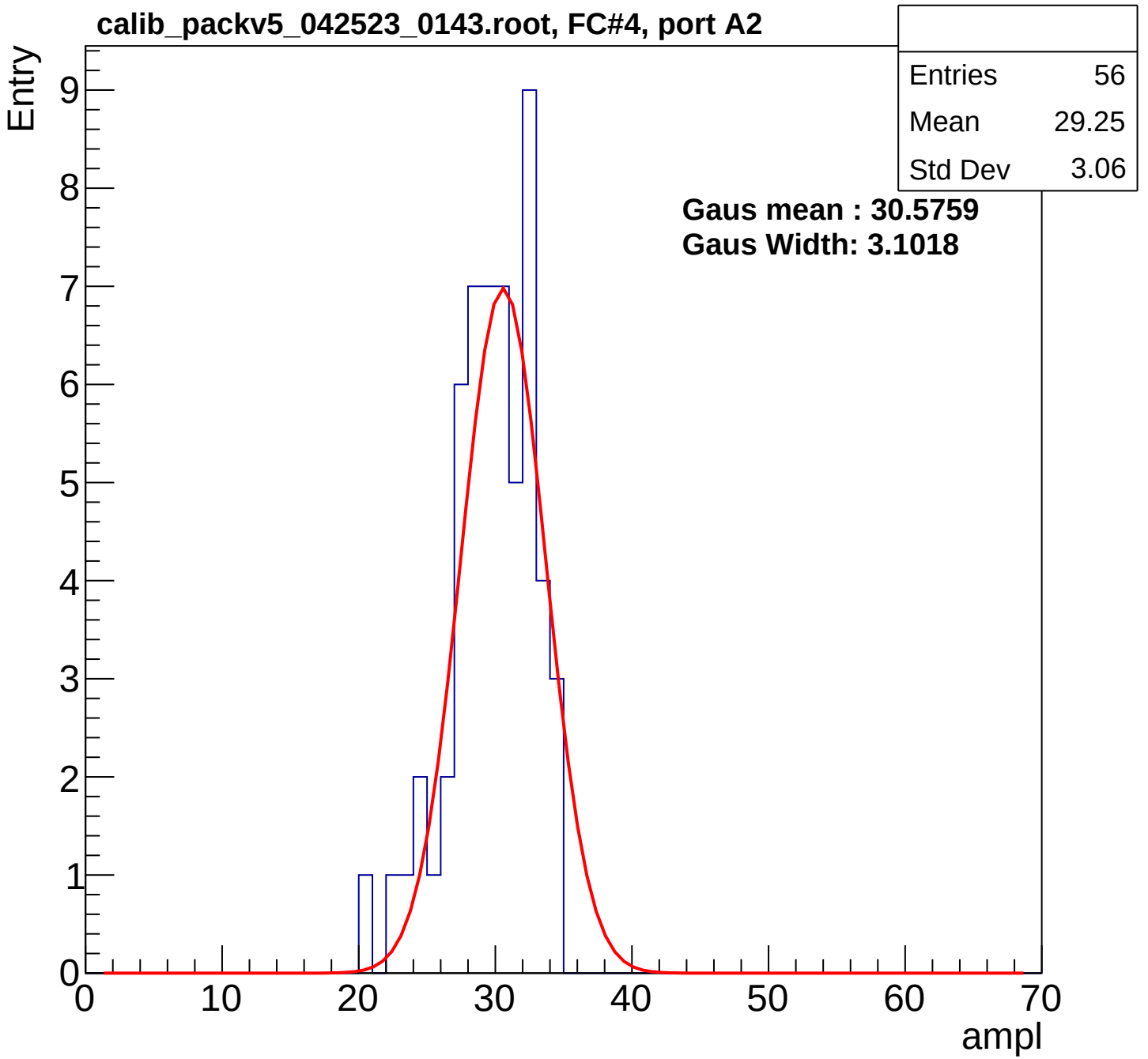

B1L100S, U4-ch72, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 47.69
Std Dev 3.765
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

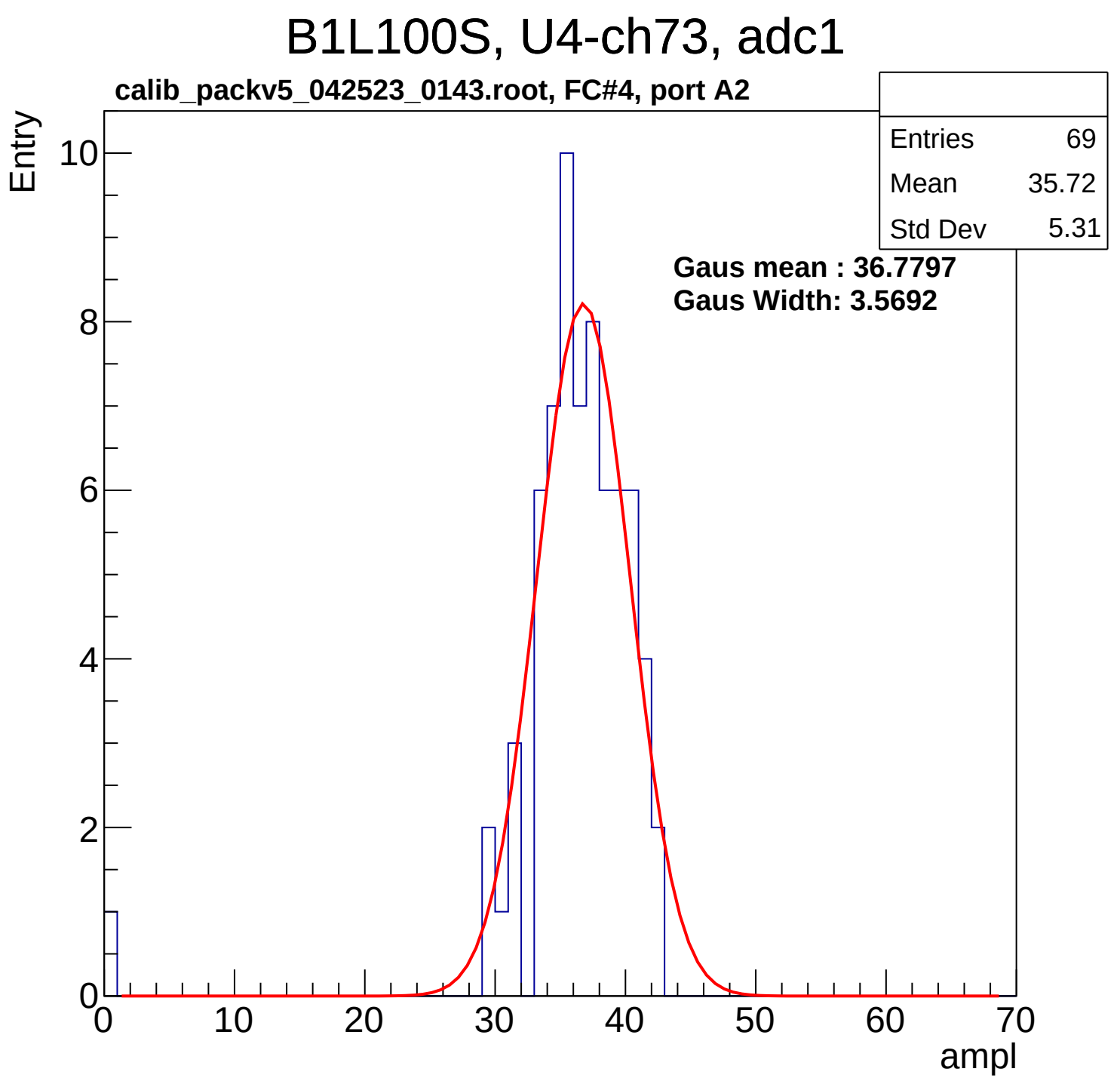

B1L100S, U4-ch72, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 53.18
Std Dev 3.724
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

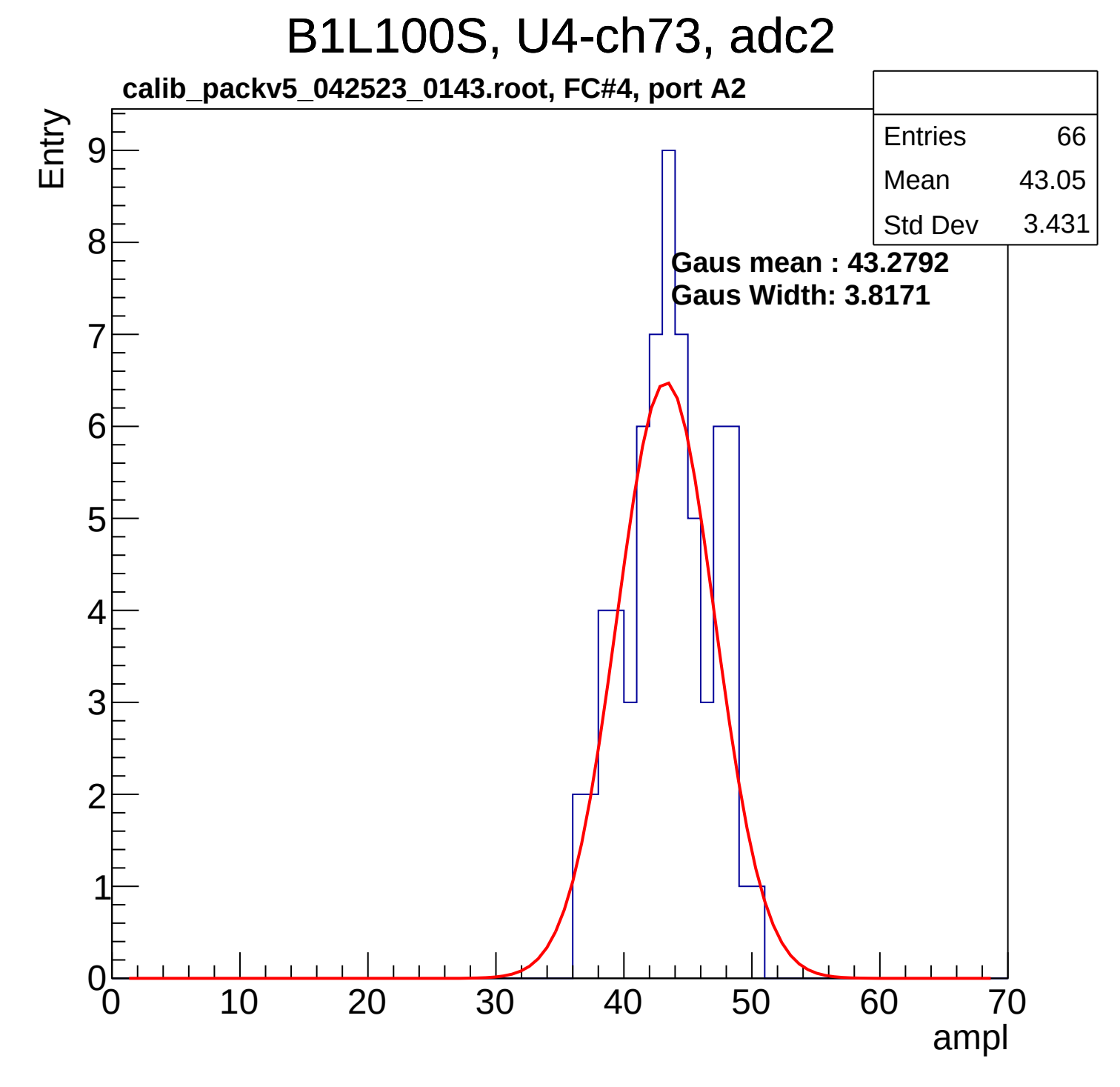

B1L100S, U4-ch72, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 42
Mean 58.5
Std Dev 3.172
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

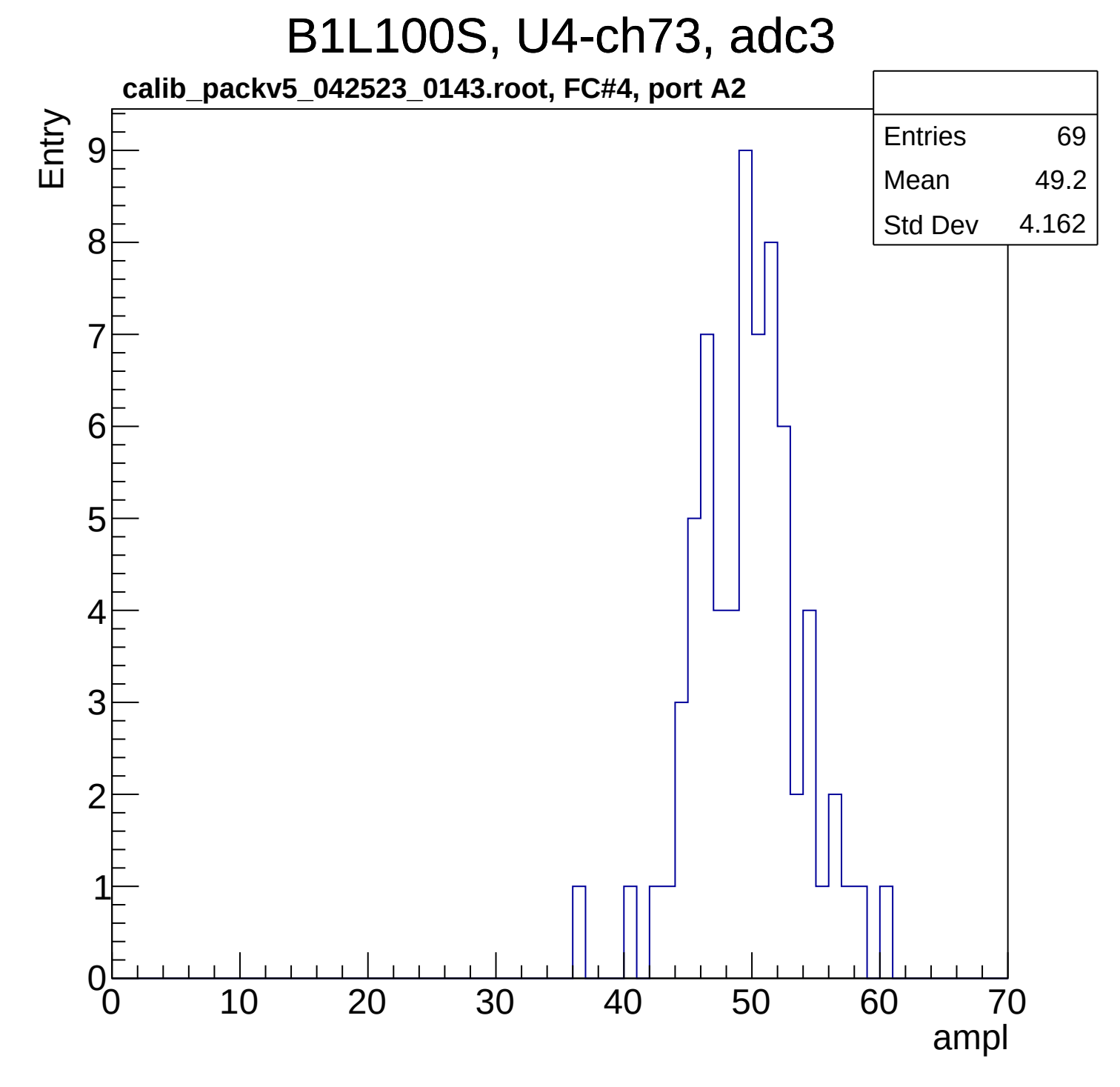

B1L100S, U4-ch72, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 22
Mean 58.45
Std Dev 12.82
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

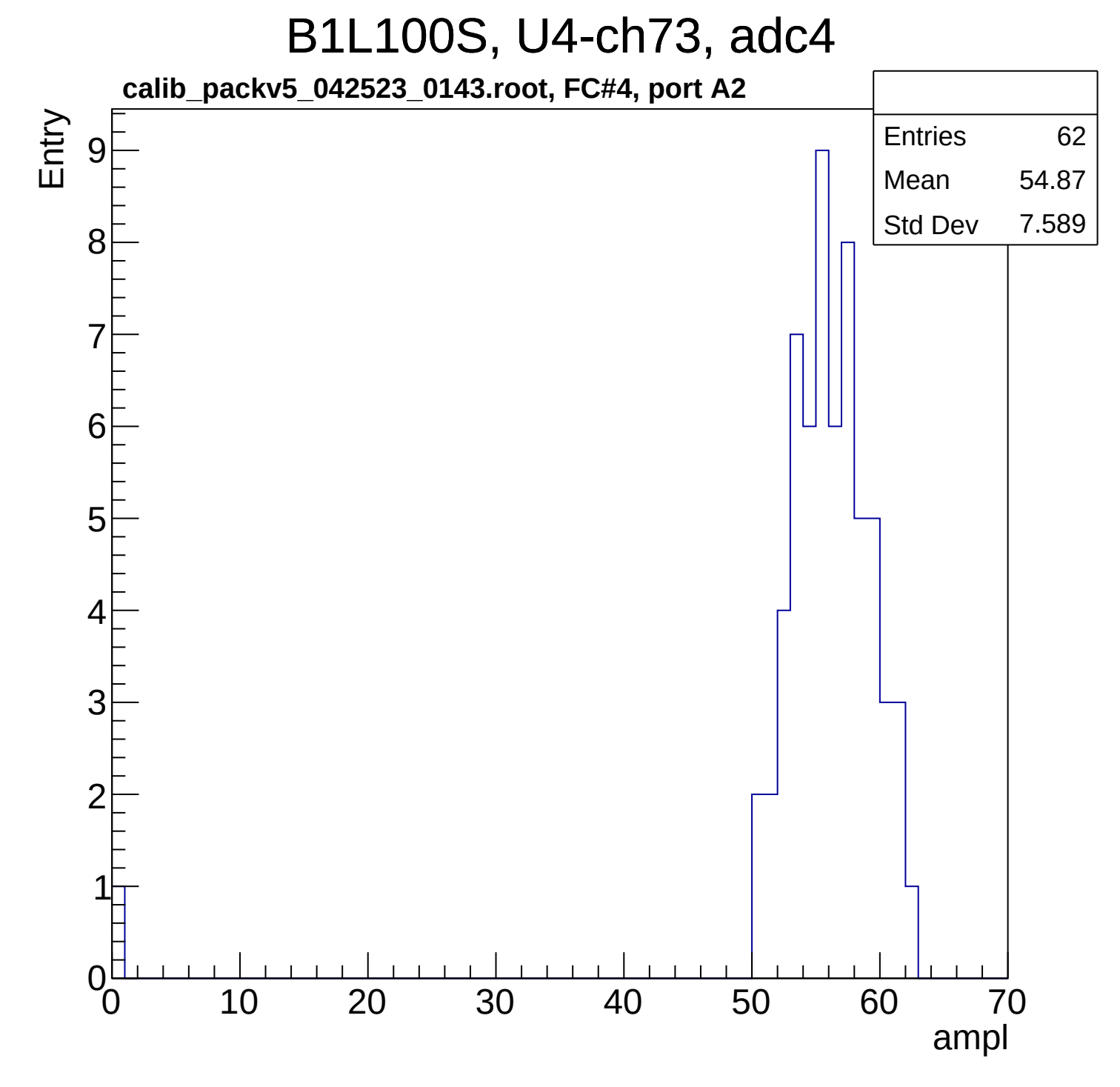

B1L100S, U4-ch72, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 35.25
Std Dev 27.83
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

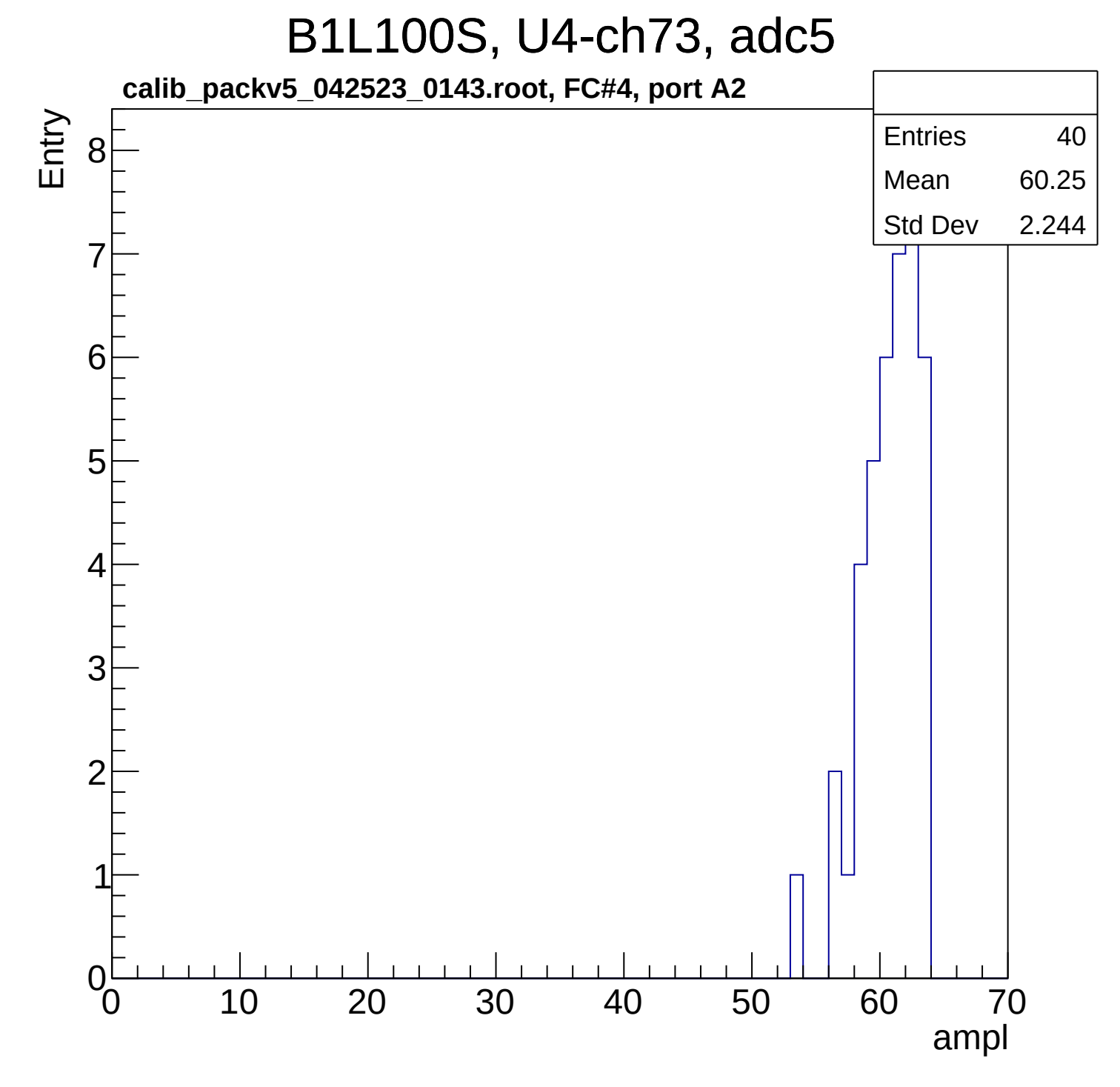

B1L100S, U4-ch73, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 29.25
Std Dev 3.06
Gaus mean : 30.5759
Gaus Width: 3.1018
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

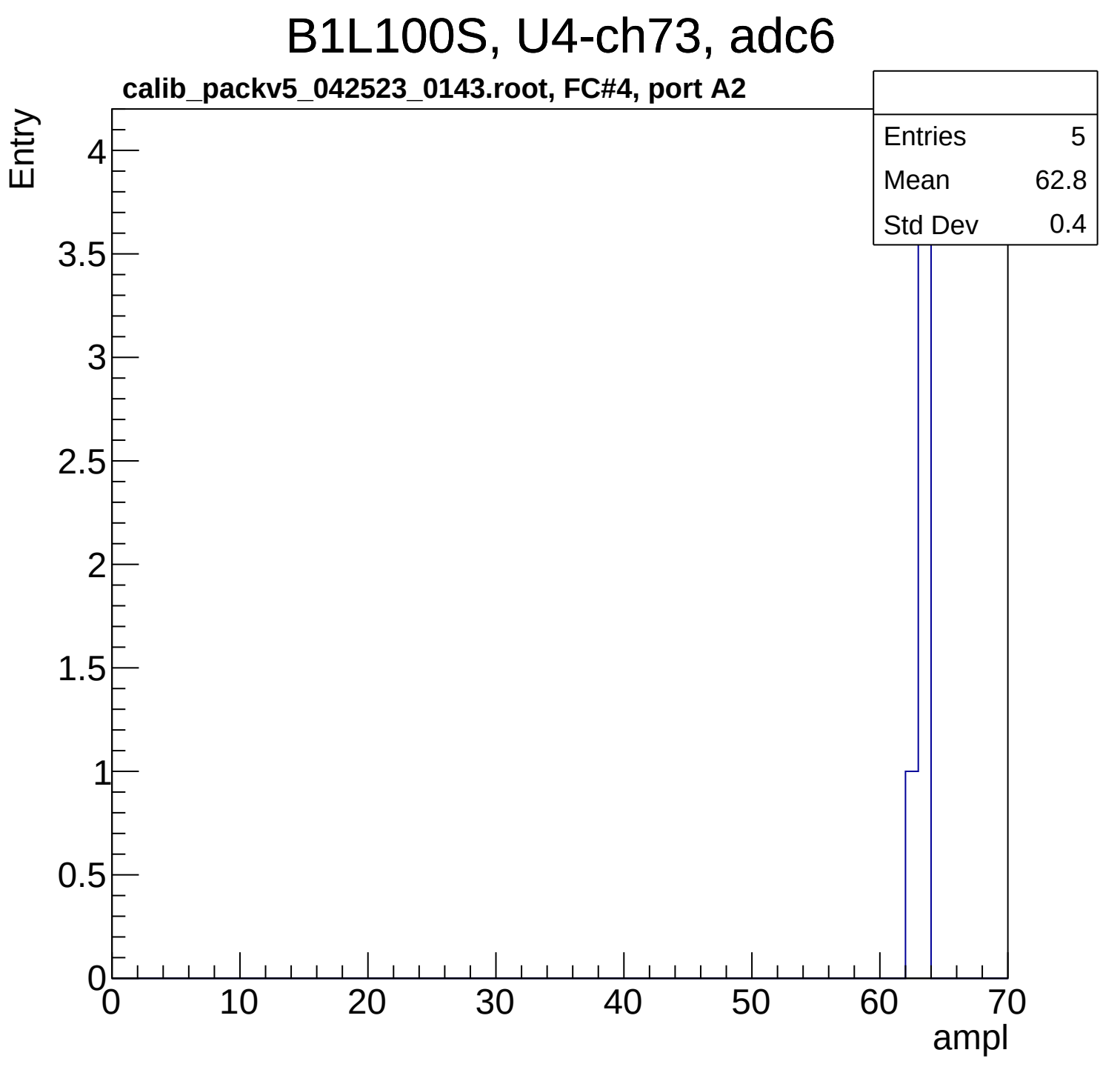

B1L100S, U4-ch73, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 35.72
Std Dev 5.31
Gaus mean : 36.7797
Gaus Width: 3.5692
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

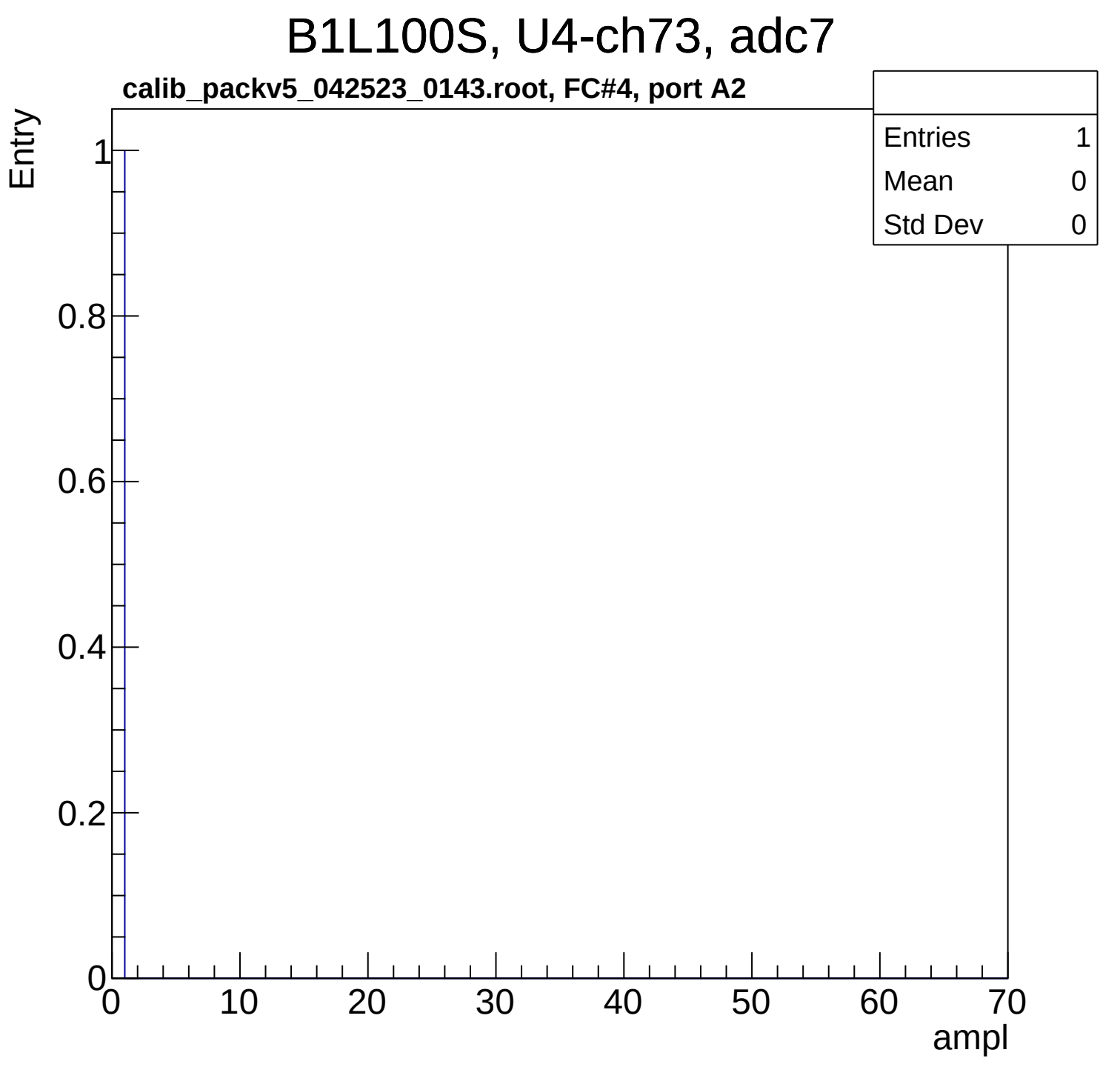

B1L100S, U4-ch73, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 43.05
Std Dev 3.431
Gaus mean : 43.2792
Gaus Width: 3.8171
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

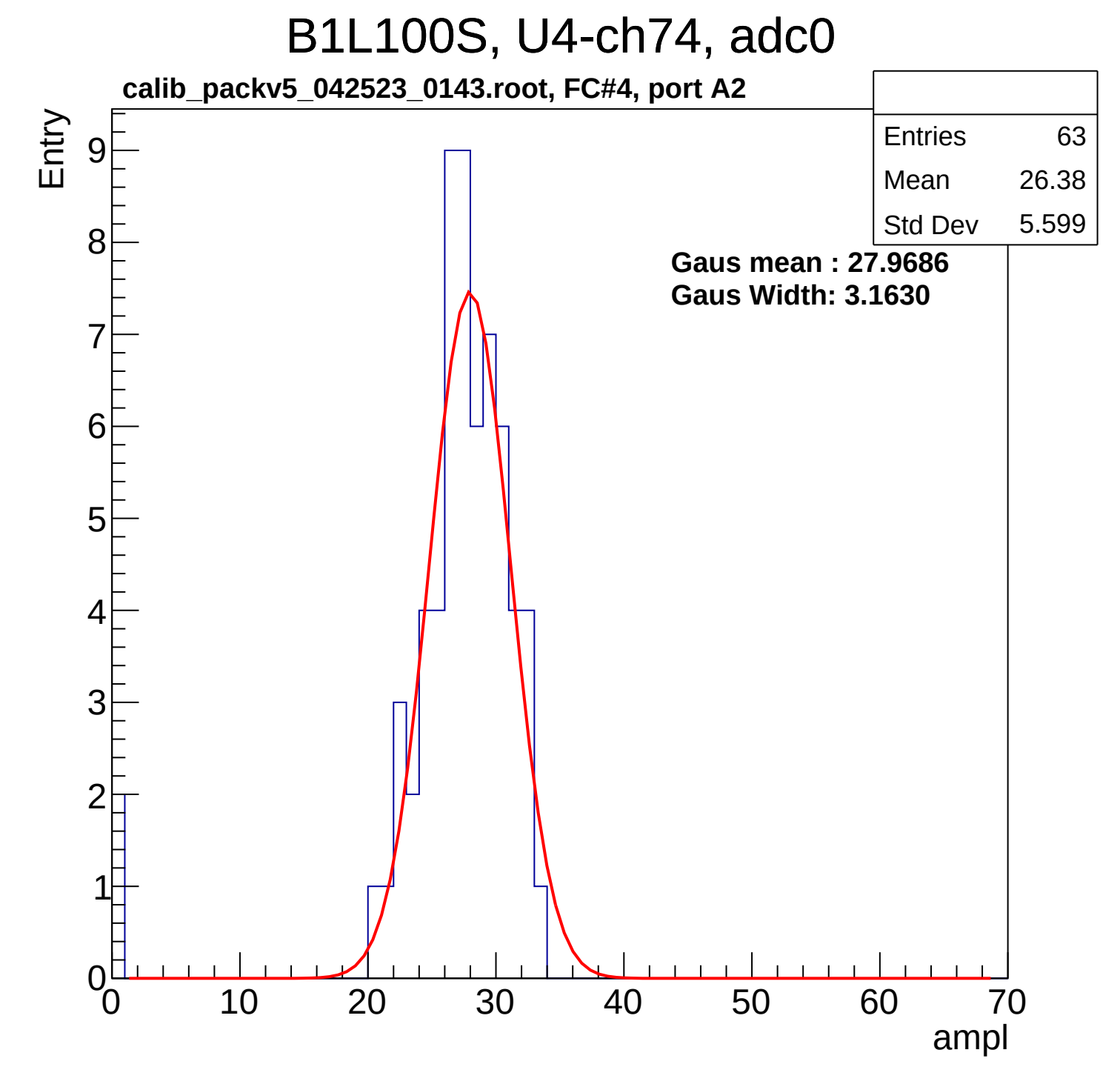

B1L100S, U4-ch73, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 49.2
Std Dev 4.162
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

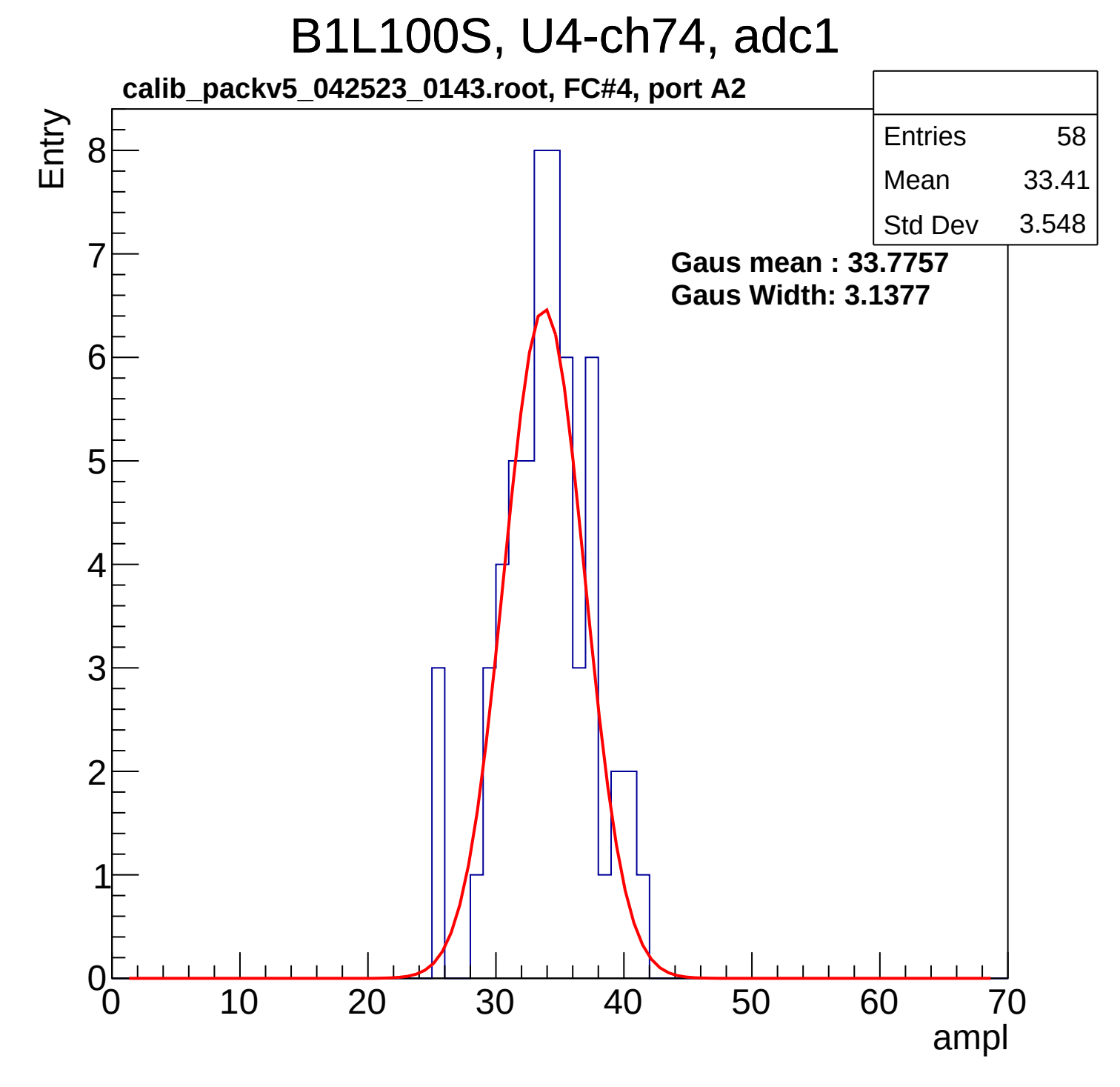

B1L100S, U4-ch73, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 54.87
Std Dev 7.589
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

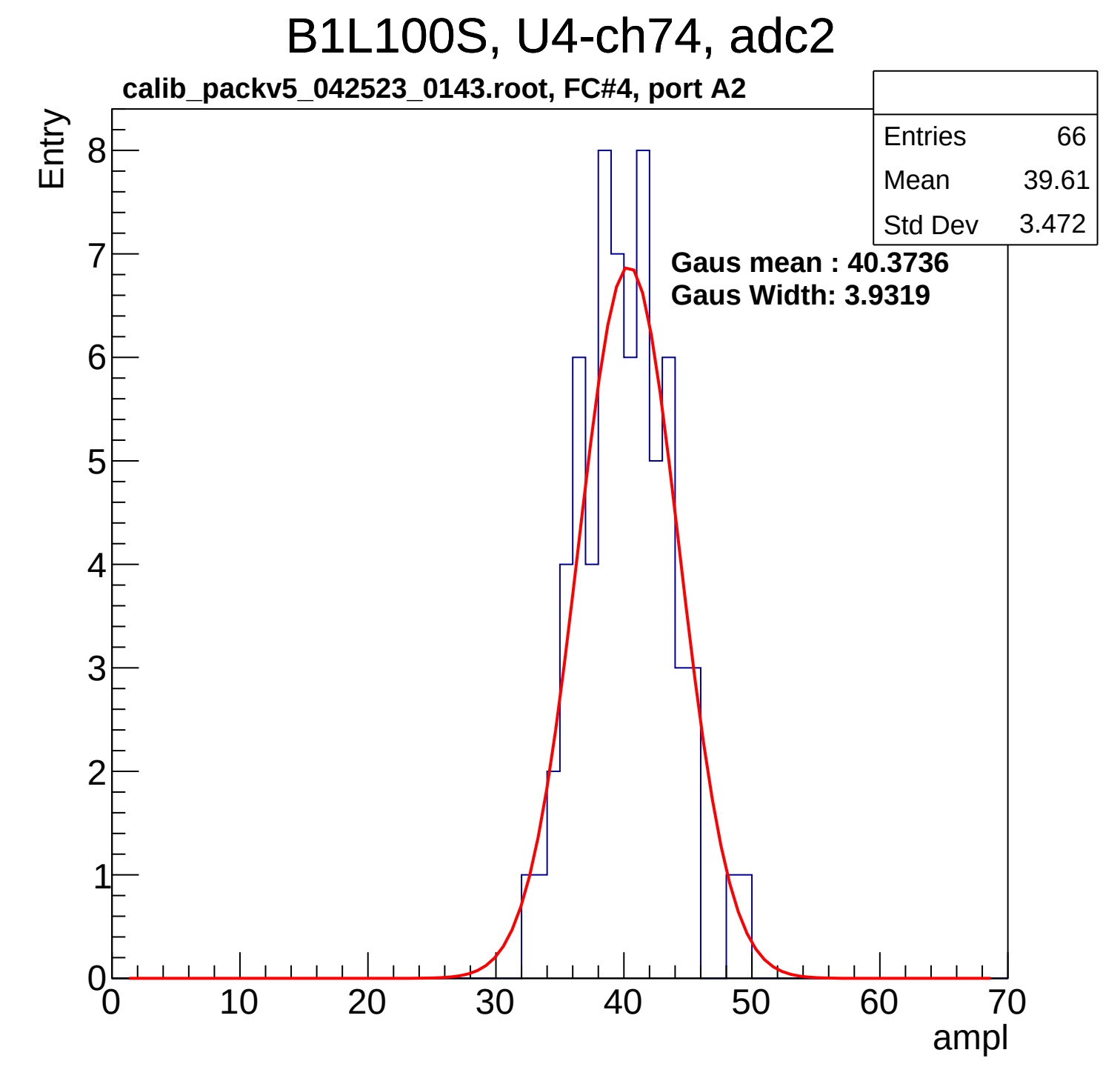

B1L100S, U4-ch73, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 40
Mean 60.25
Std Dev 2.244
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

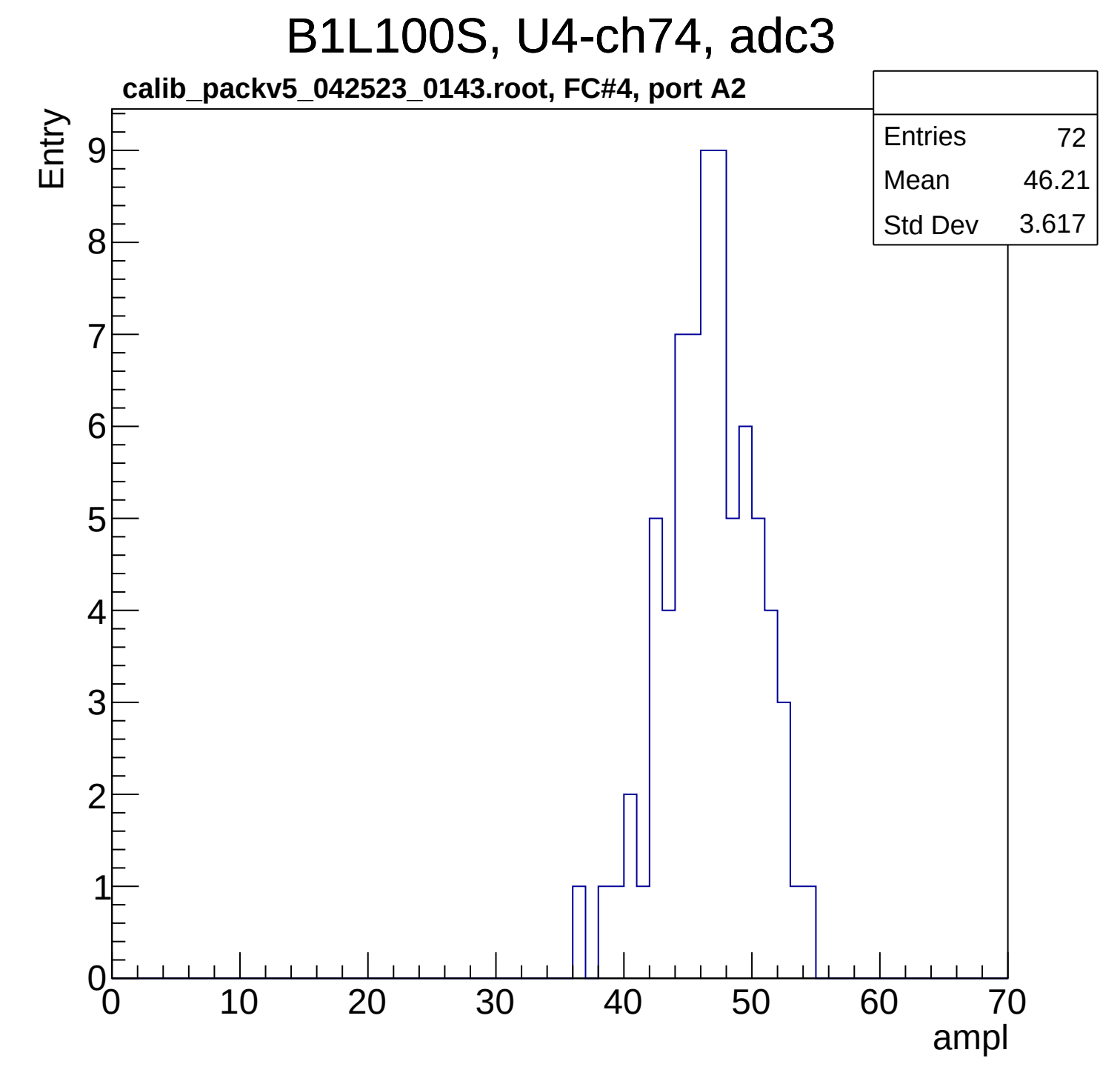

B1L100S, U4-ch73, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 5
Mean 62.8
Std Dev 0.4
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

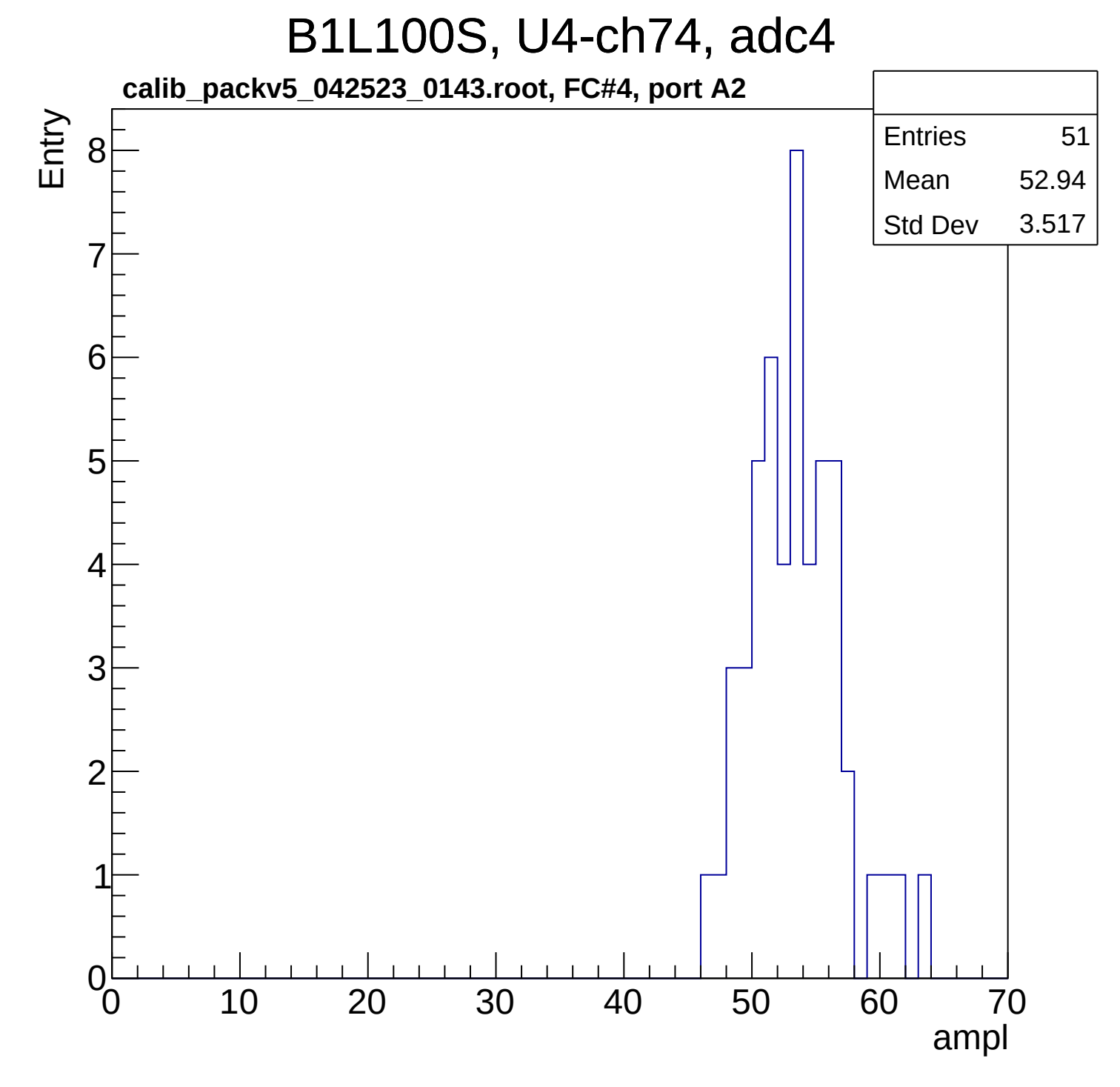

B1L100S, U4-ch73, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

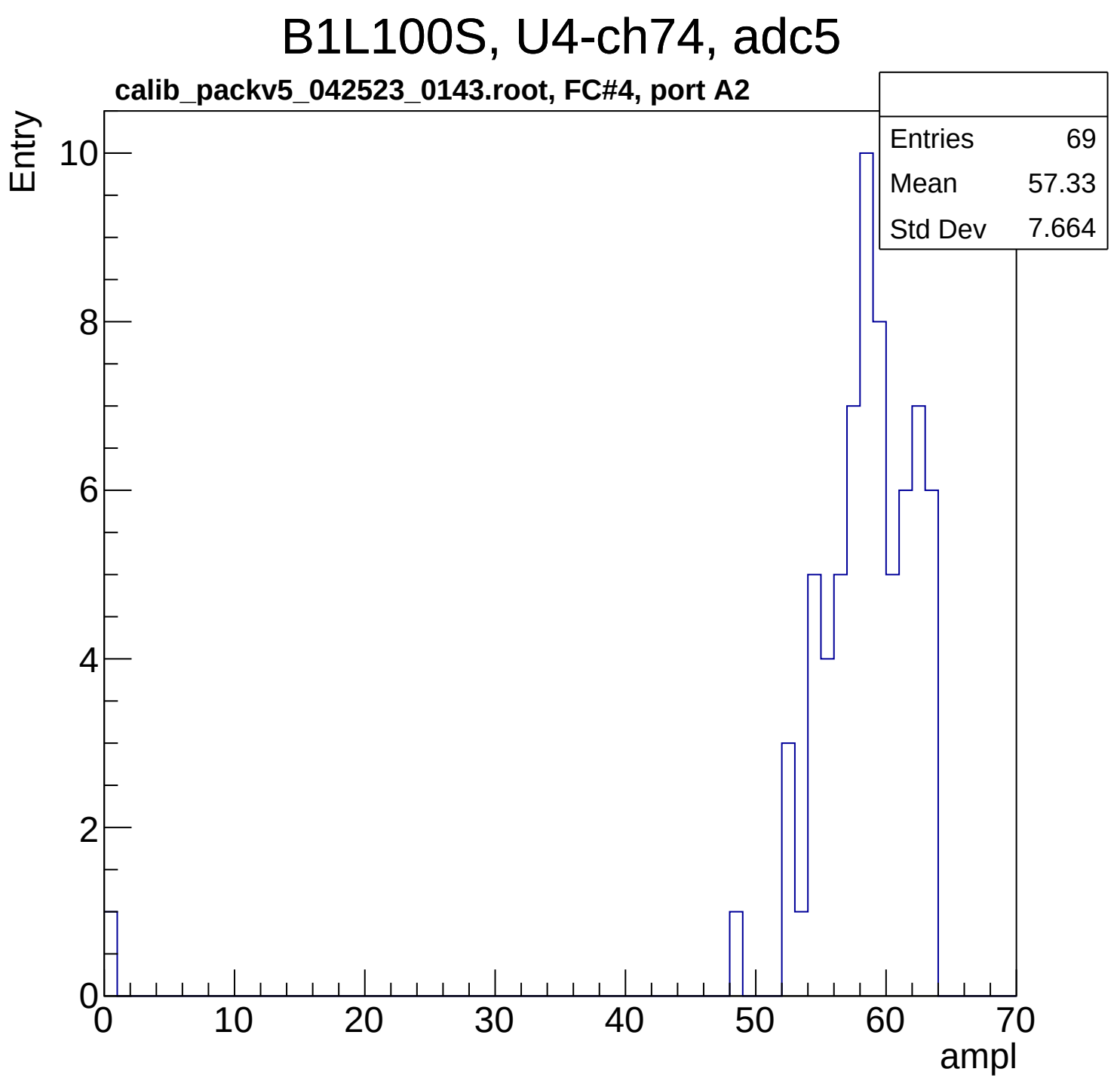

B1L100S, U4-ch74, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 26.38
Std Dev 5.599
Gaus mean : 27.9686
Gaus Width: 3.1630
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

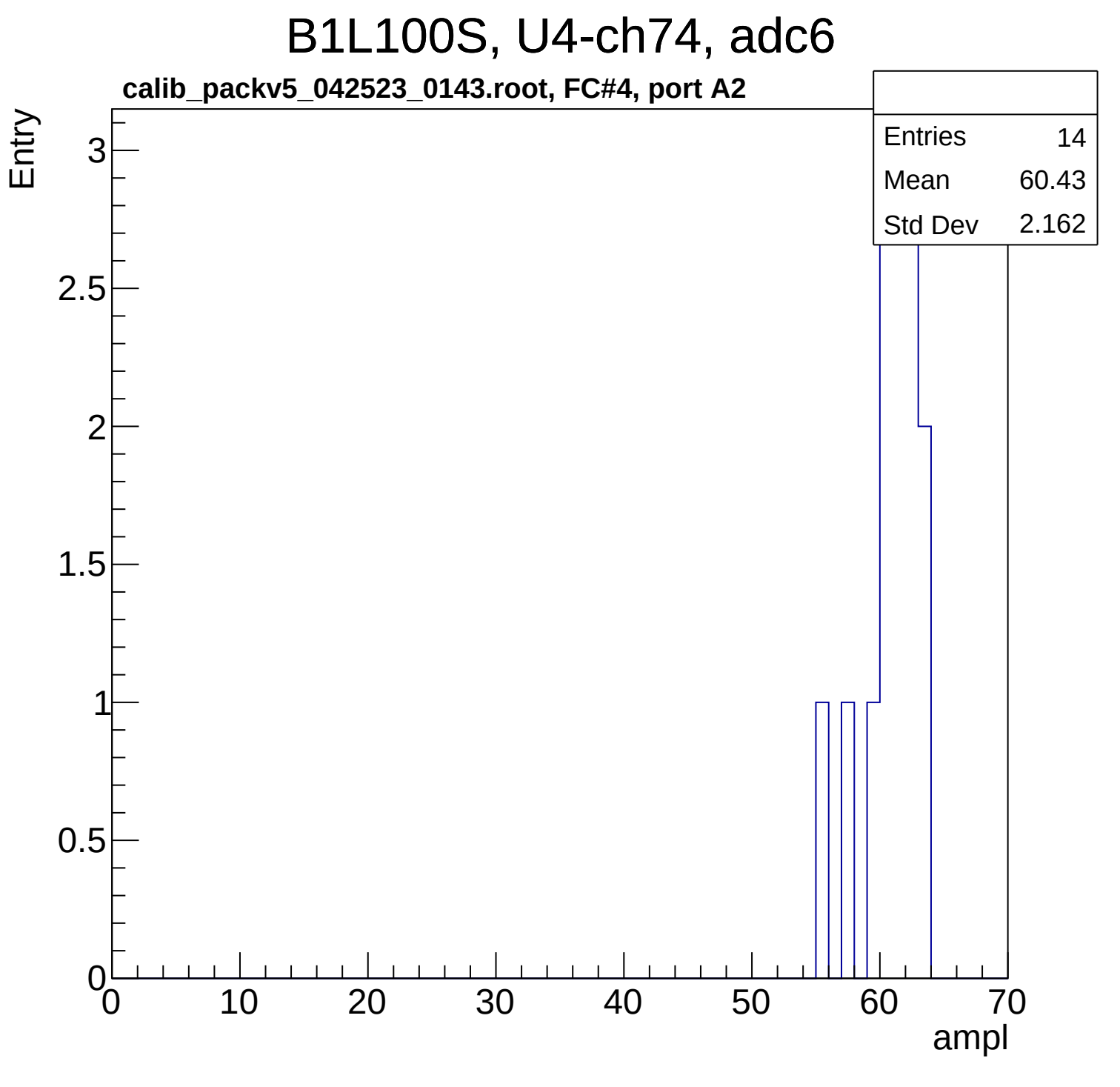

B1L100S, U4-ch74, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 33.41
Std Dev 3.548
Gaus mean : 33.7757
Gaus Width: 3.1377
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

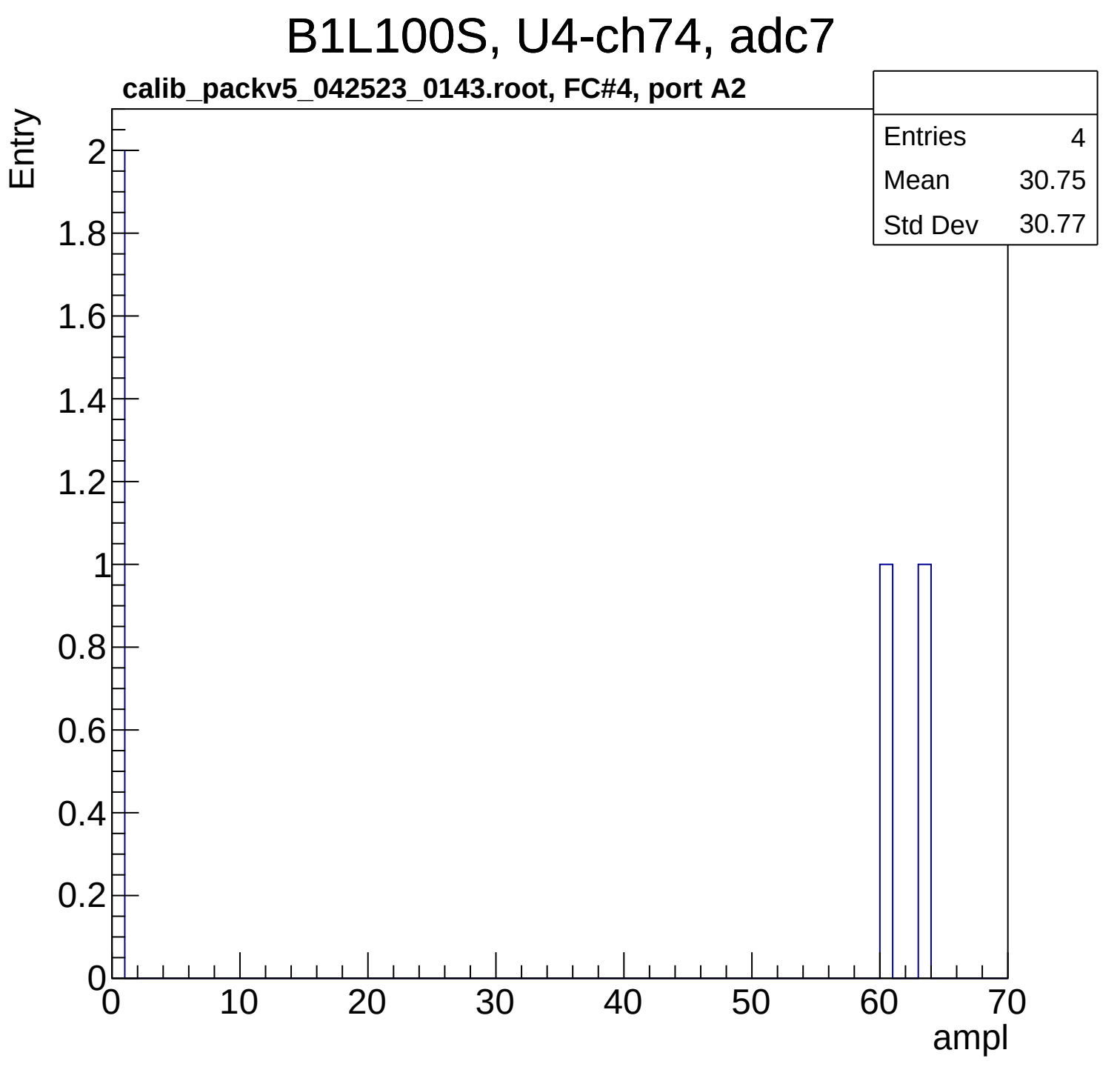

B1L100S, U4-ch74, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 39.61
Std Dev 3.472
Gaus mean : 40.3736
Gaus Width: 3.9319
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

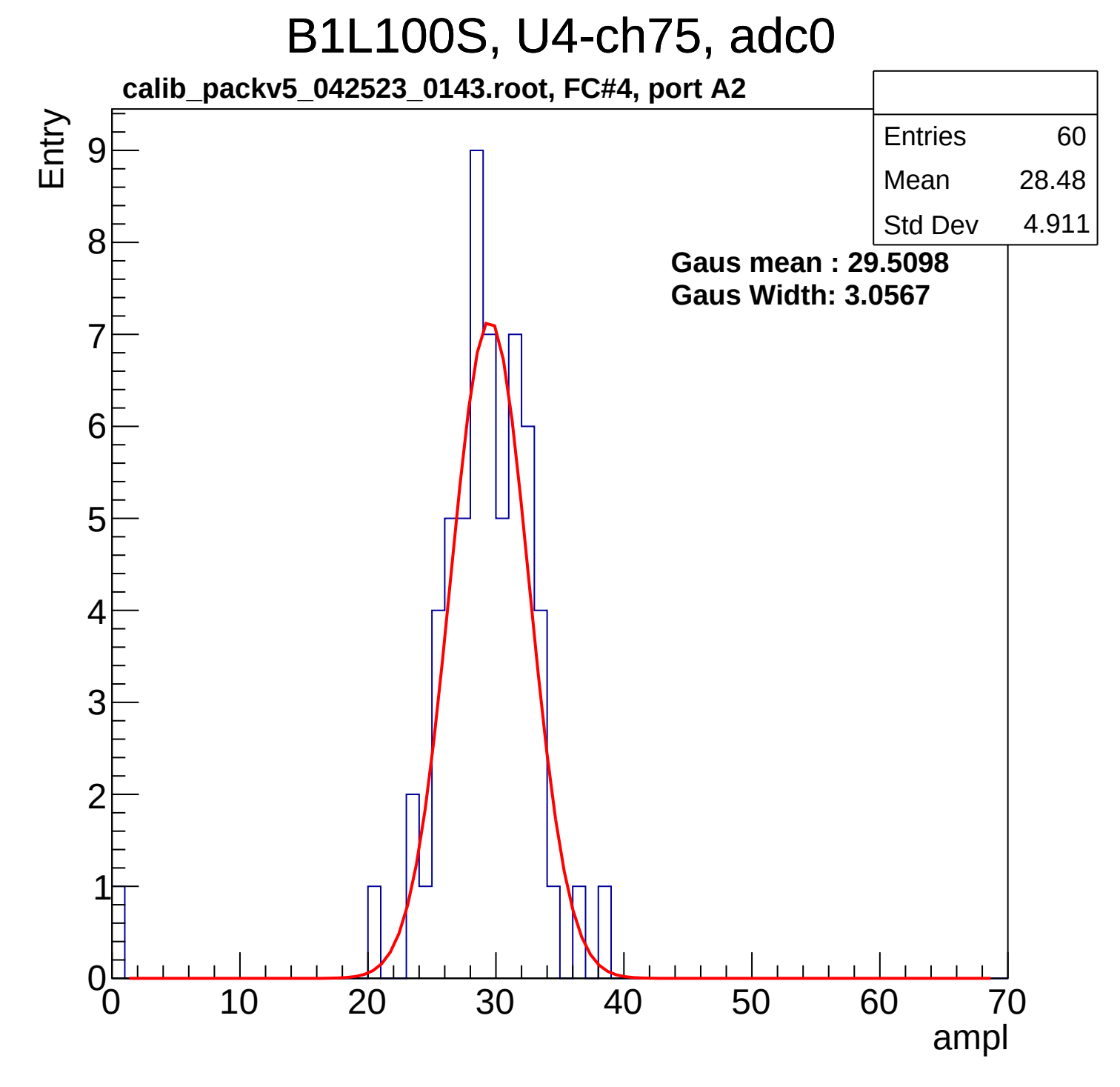

B1L100S, U4-ch74, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 46.21
Std Dev 3.617
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

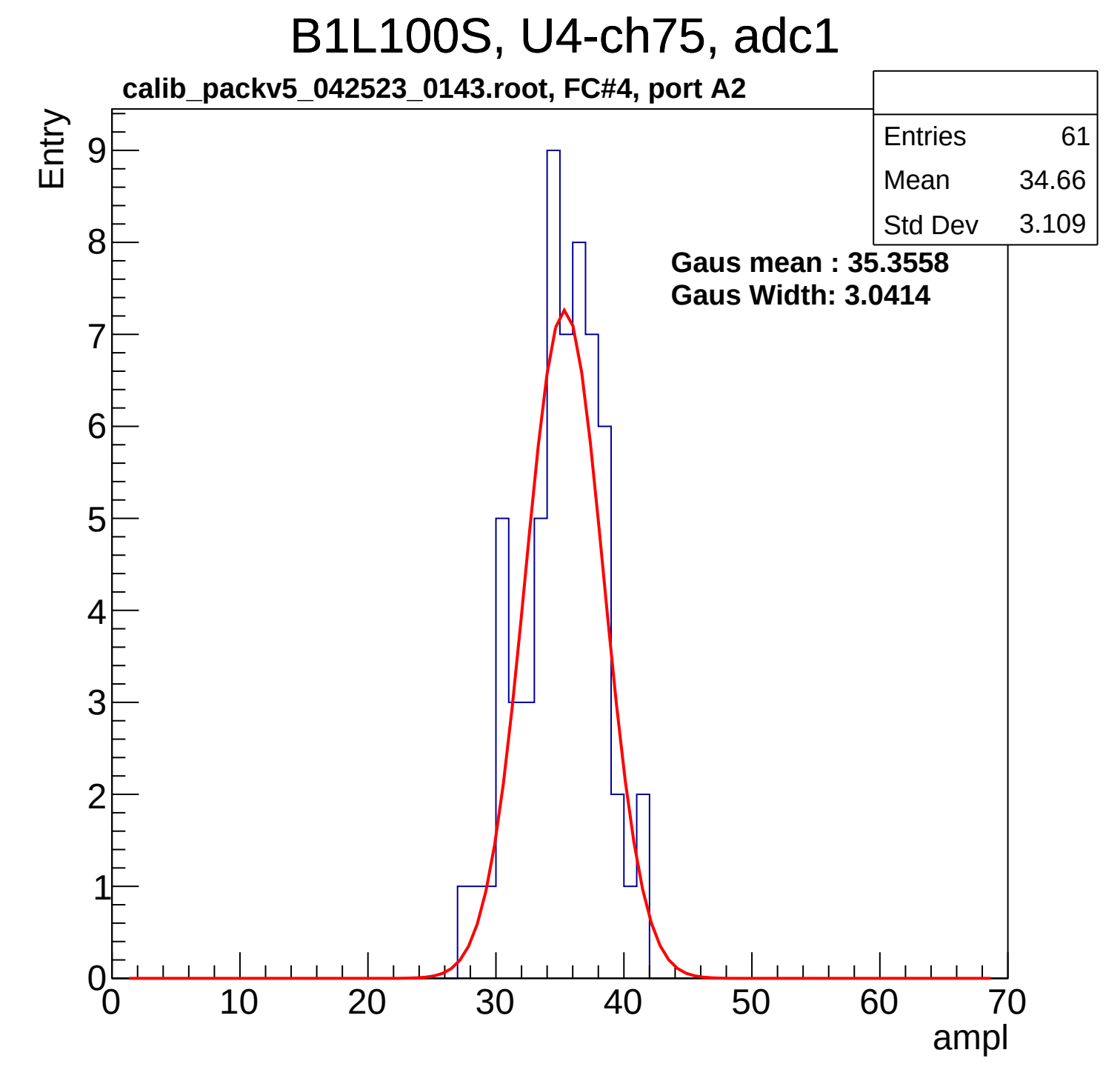

B1L100S, U4-ch74, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 52.94
Std Dev 3.517
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

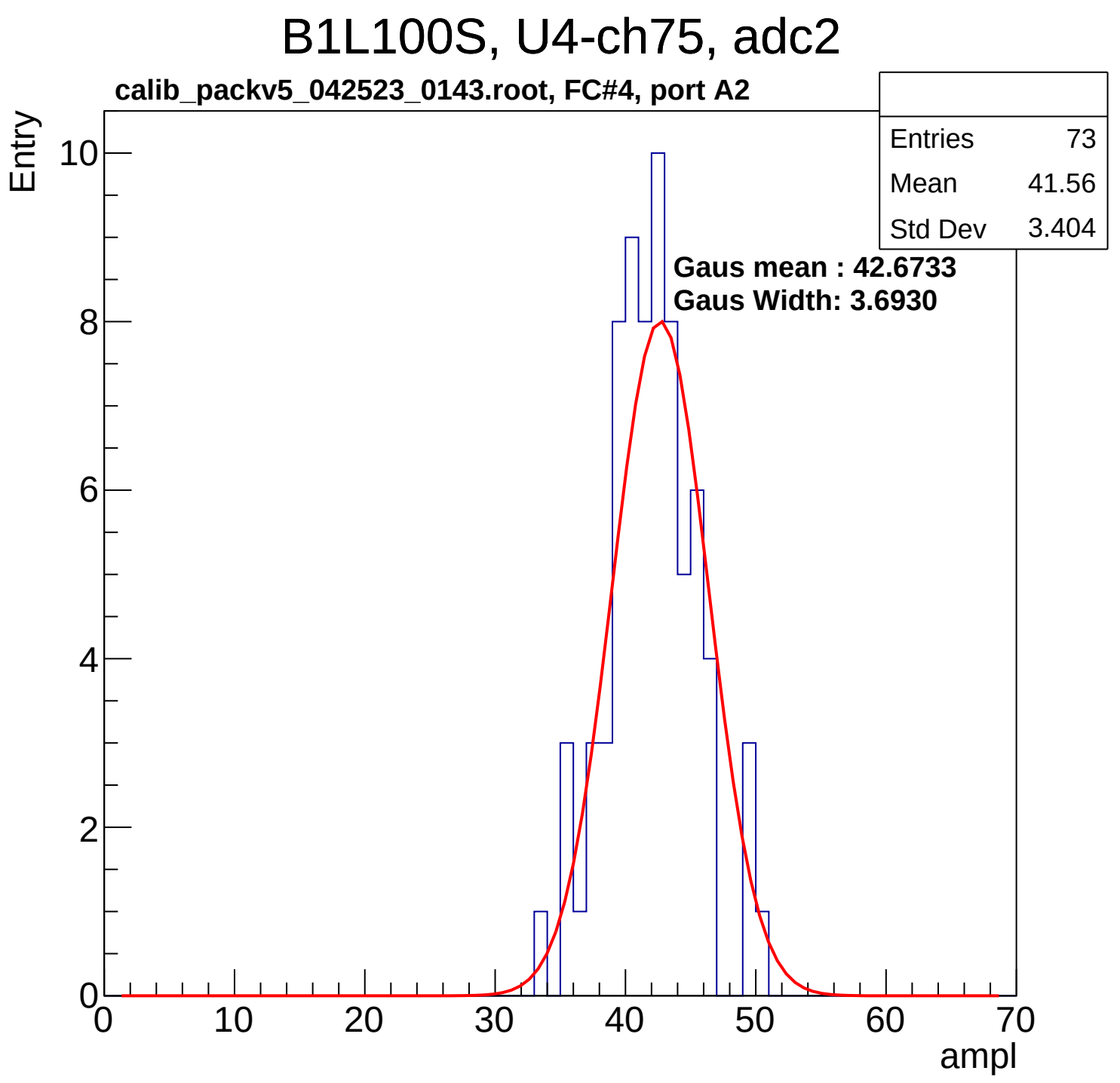

B1L100S, U4-ch74, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 57.33
Std Dev 7.664
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

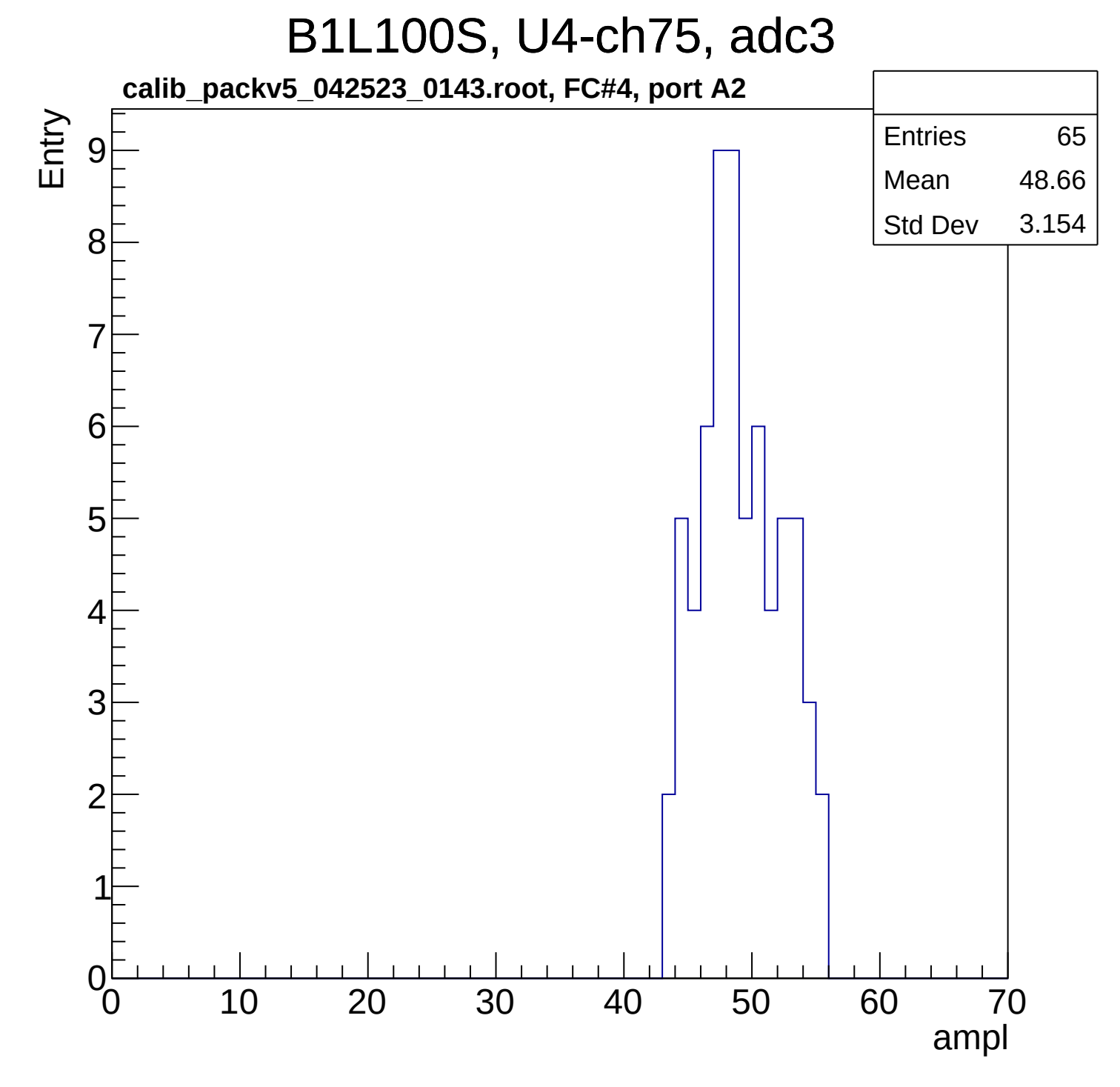

B1L100S, U4-ch74, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 14
Mean 60.43
Std Dev 2.162
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

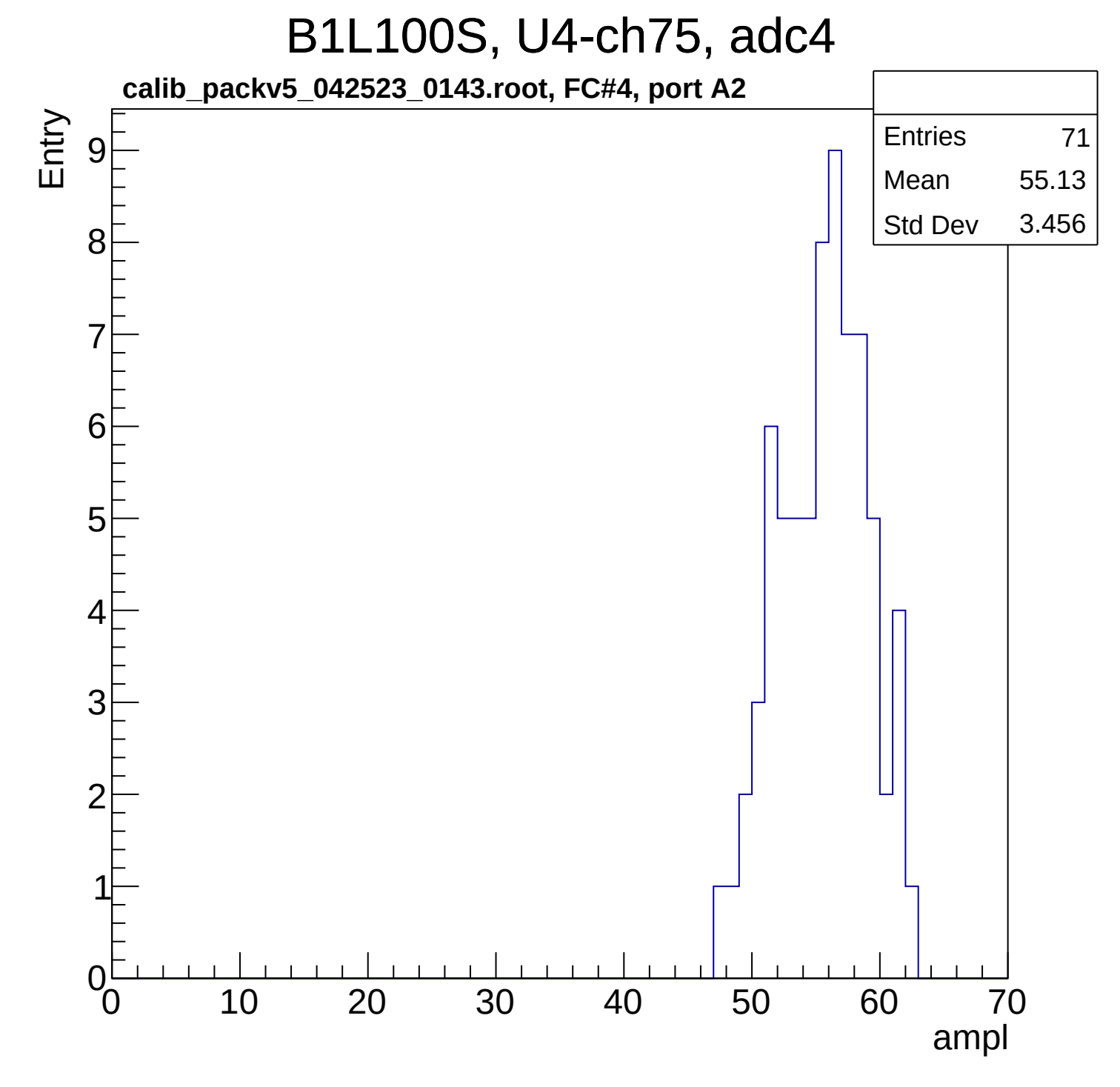

B1L100S, U4-ch74, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 30.75
Std Dev 30.77
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

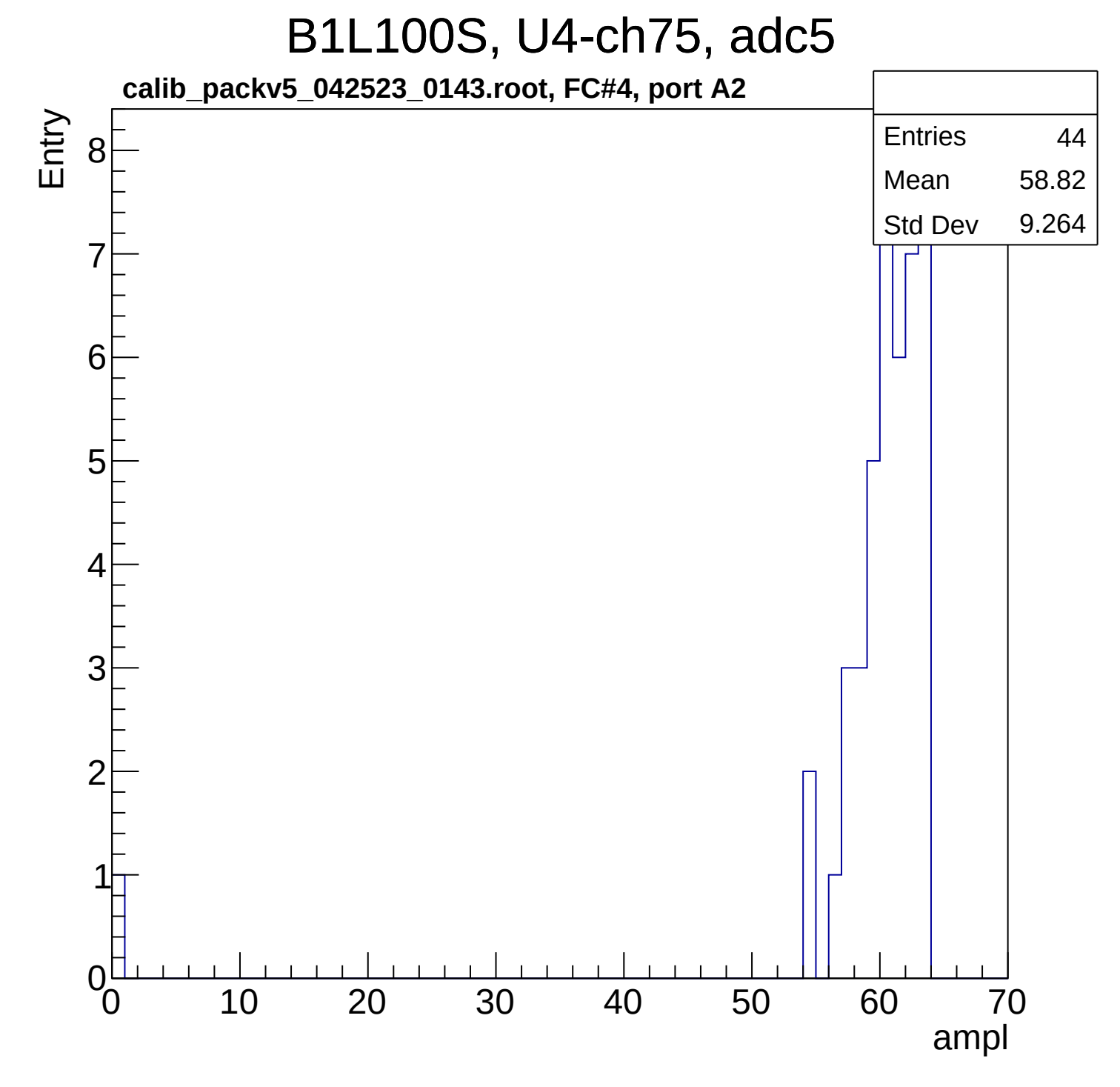

B1L100S, U4-ch75, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 28.48
Std Dev 4.911
Gaus mean : 29.5098
Gaus Width: 3.0567
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

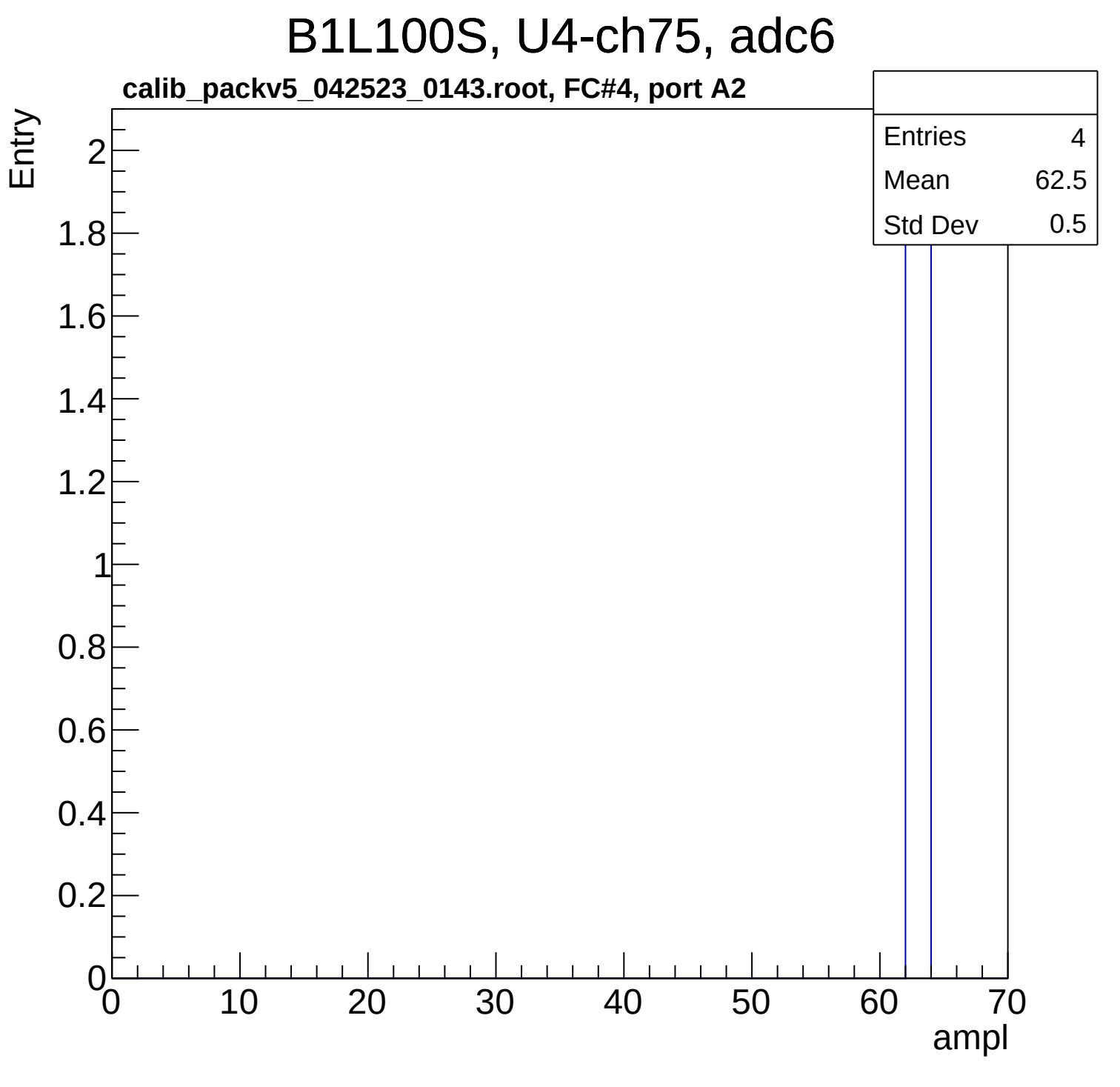

B1L100S, U4-ch75, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 34.66
Std Dev 3.109
Gaus mean : 35.3558
Gaus Width: 3.0414
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

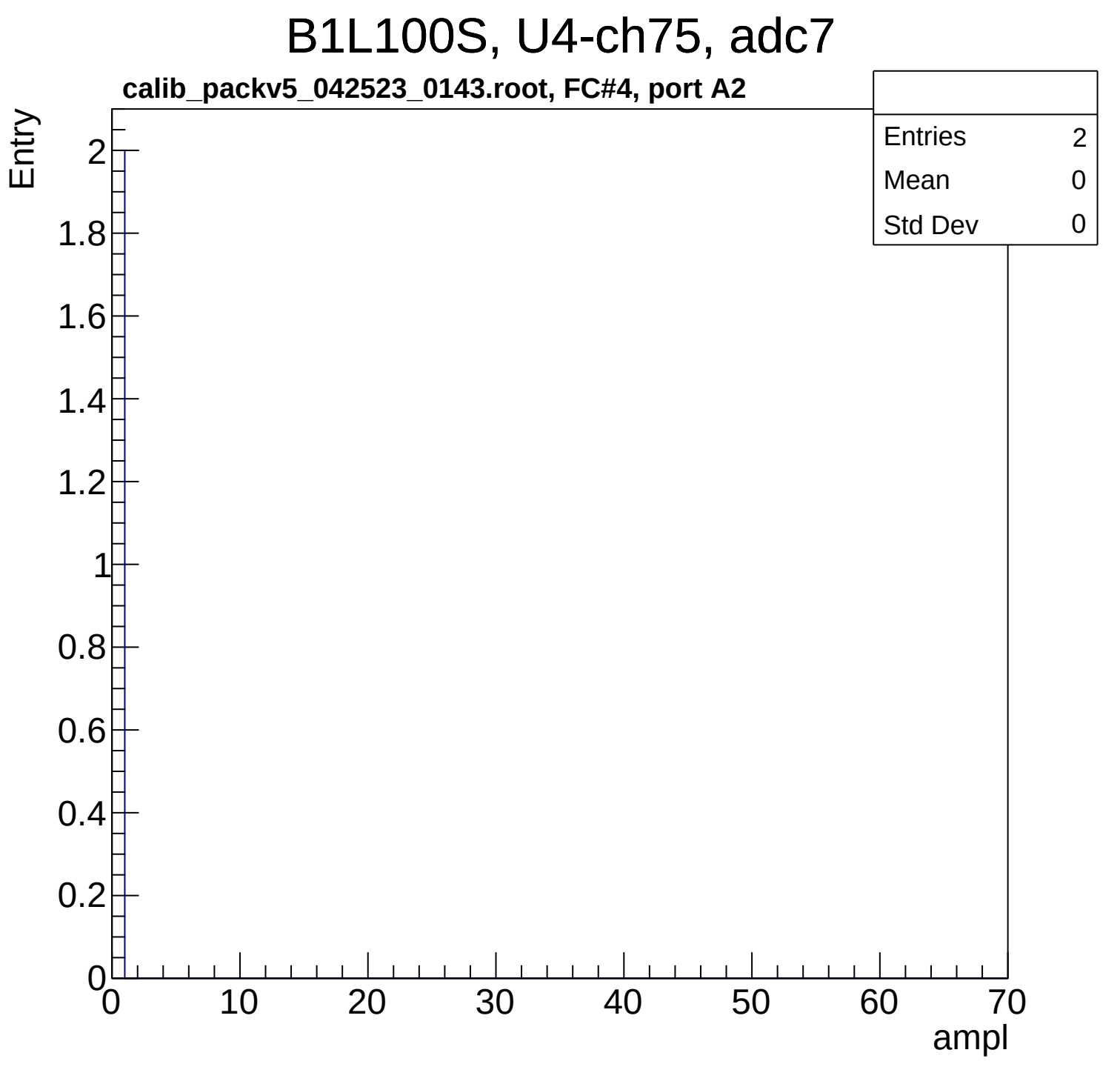

B1L100S, U4-ch75, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 41.56
Std Dev 3.404
Gaus mean : 42.6733
Gaus Width: 3.6930
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

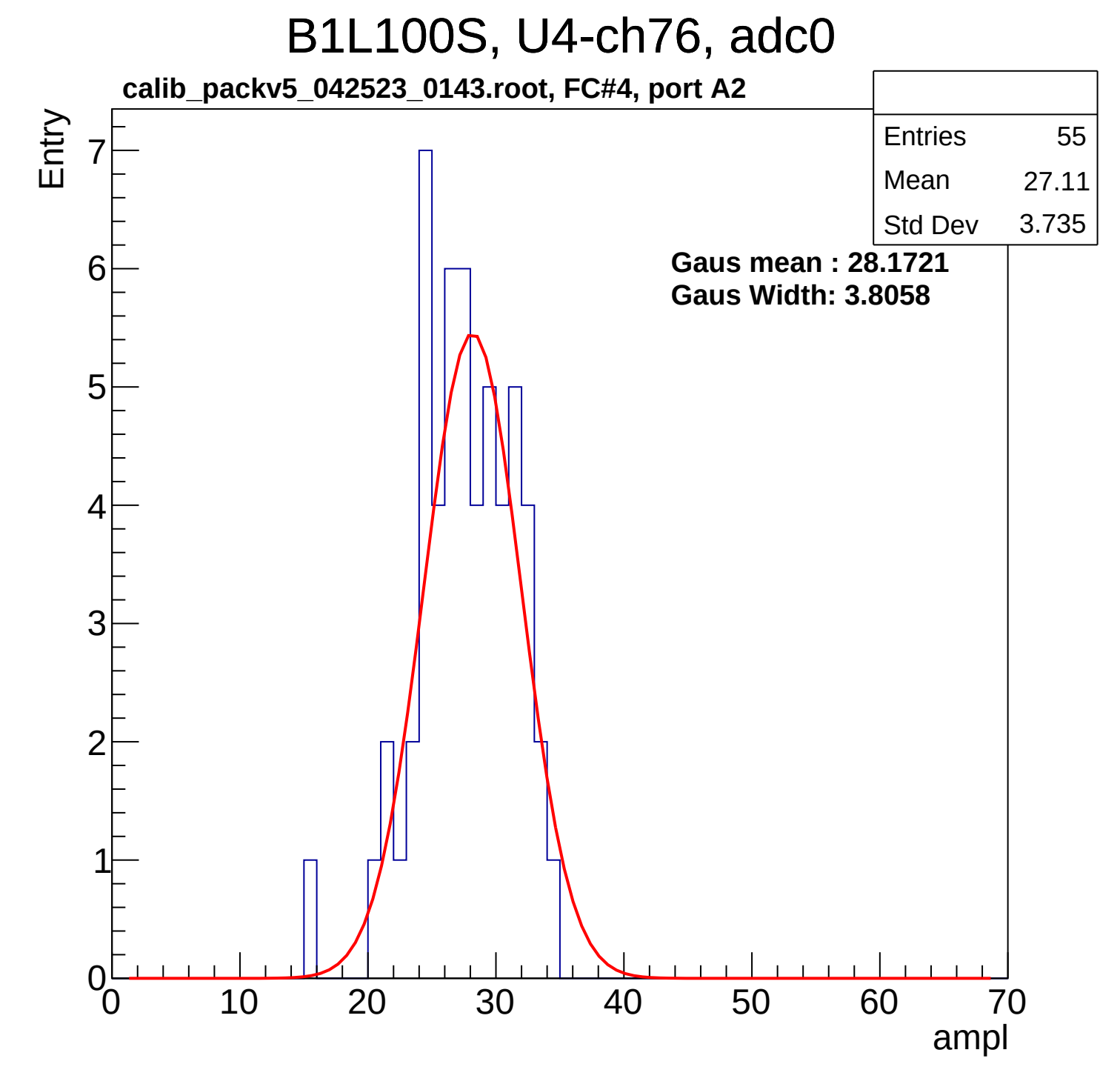

B1L100S, U4-ch75, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 48.66
Std Dev 3.154
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

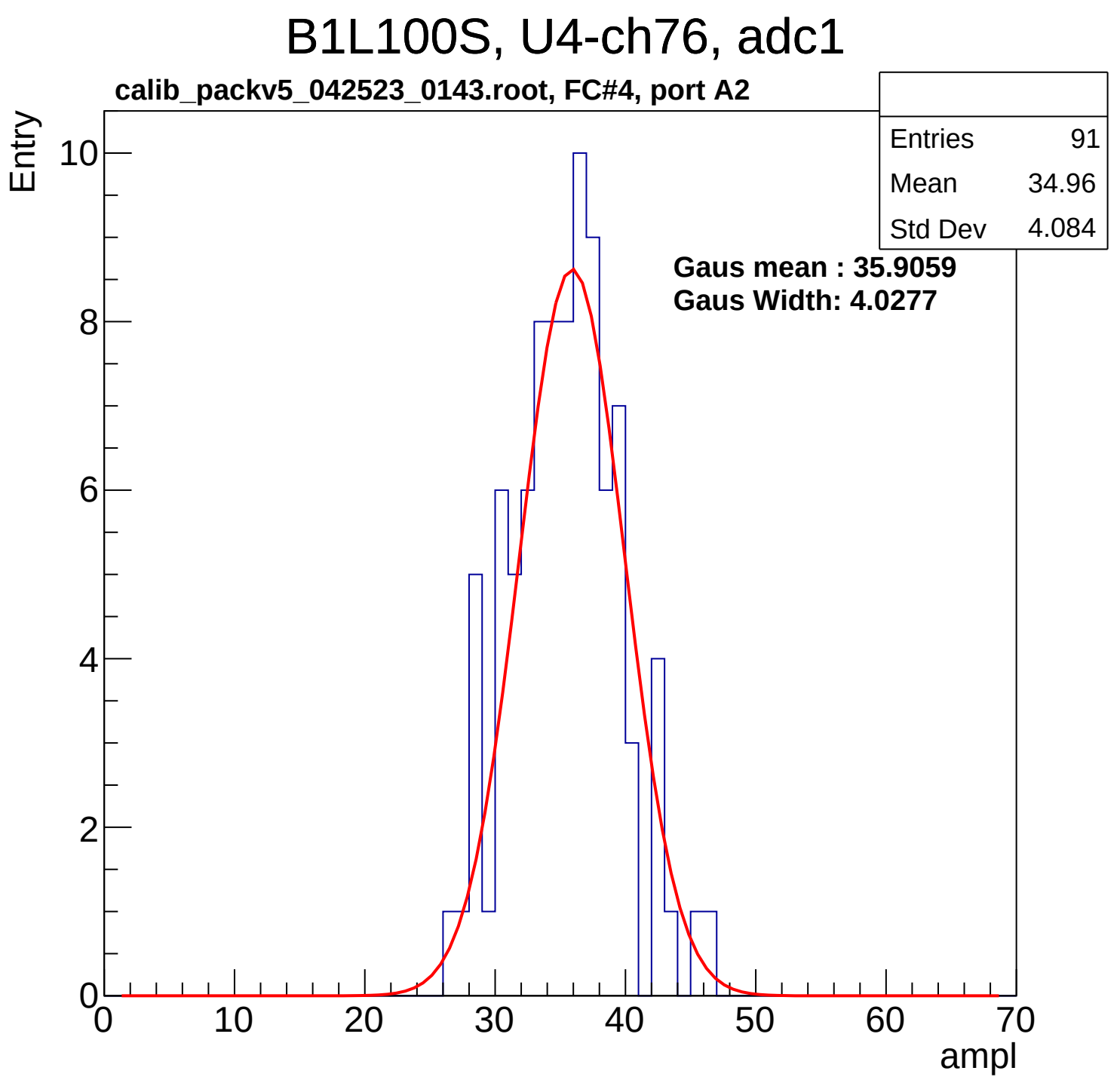

B1L100S, U4-ch75, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 55.13
Std Dev 3.456
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

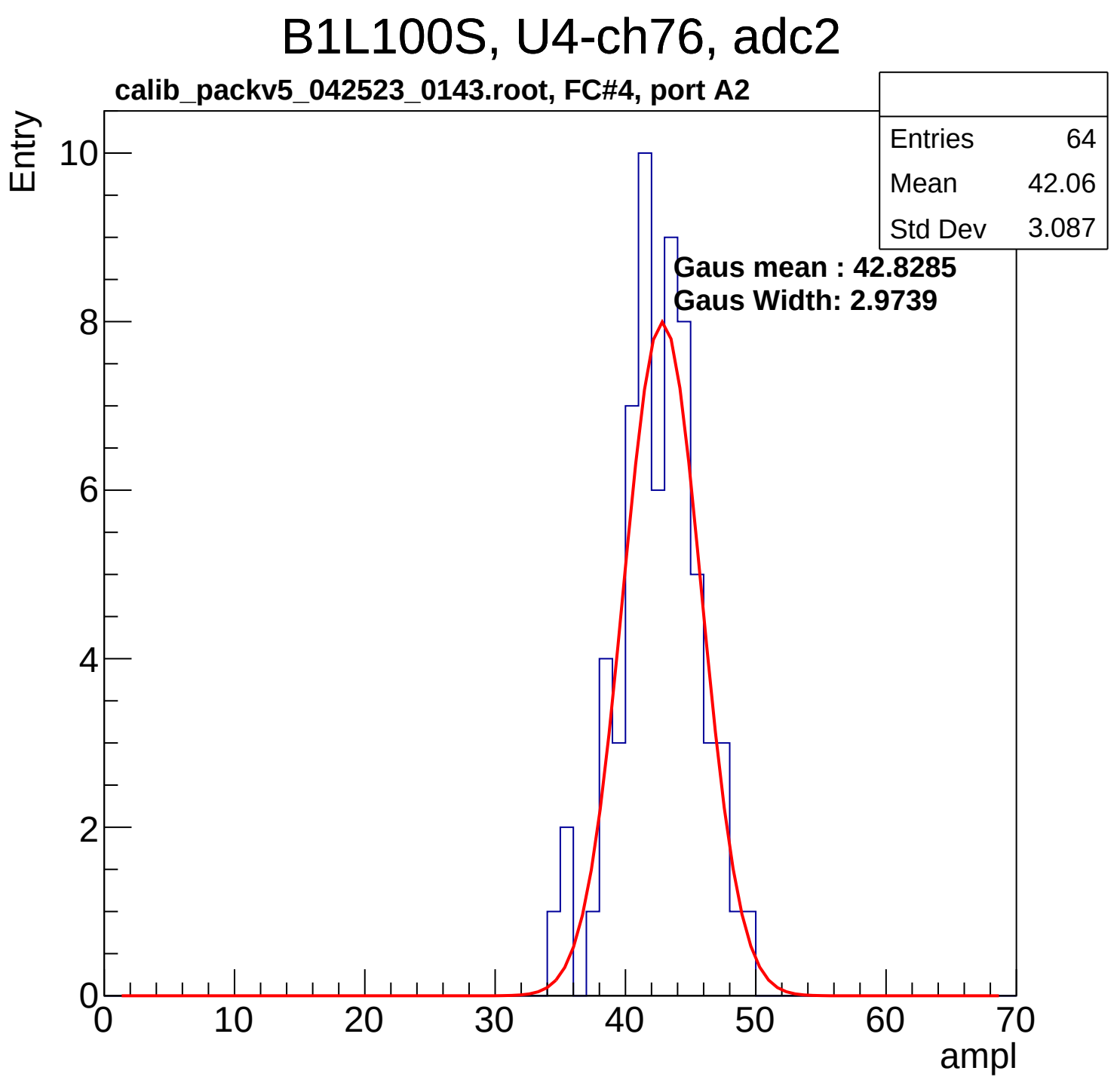

B1L100S, U4-ch75, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 44
Mean 58.82
Std Dev 9.264
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

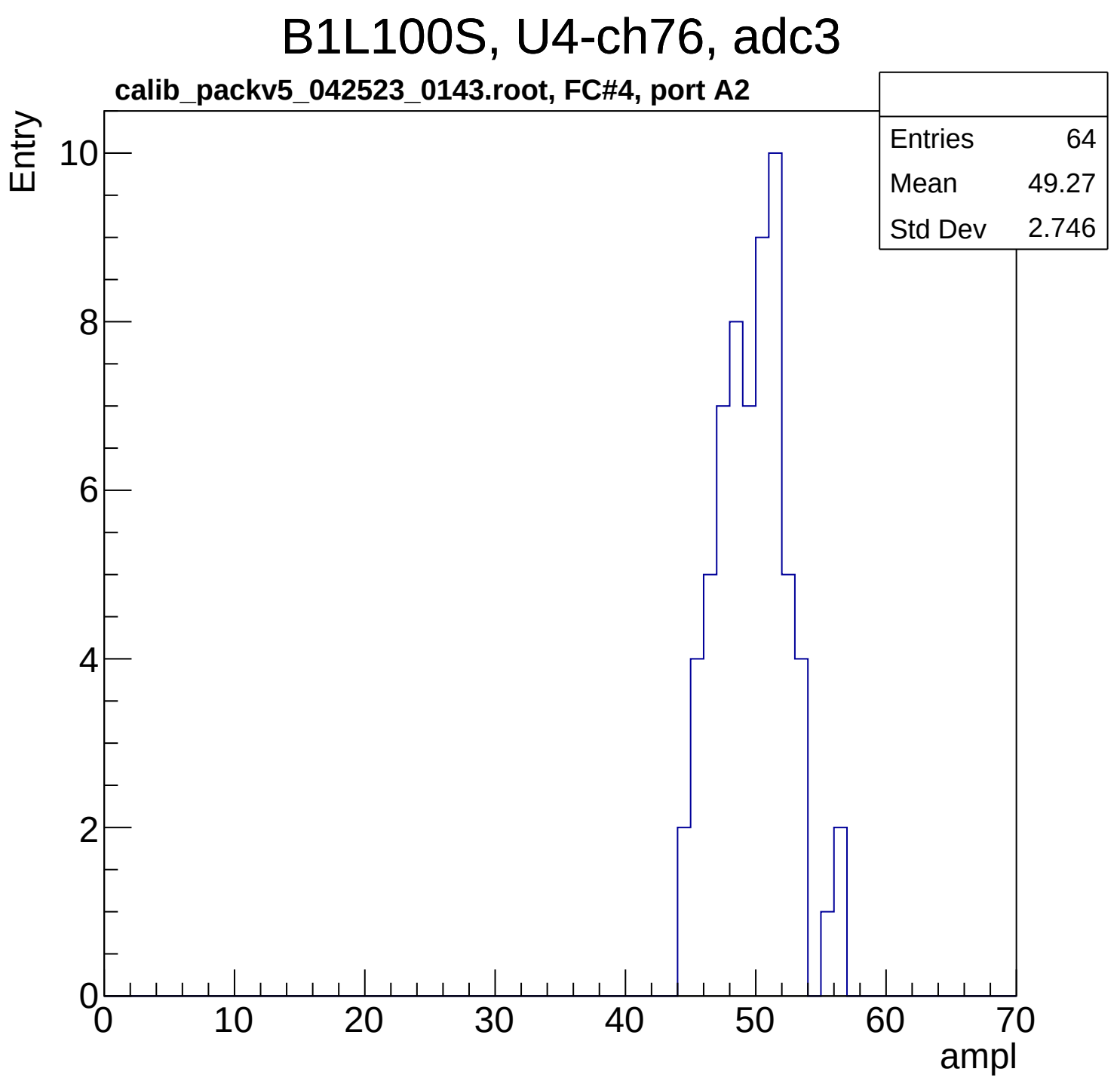

B1L100S, U4-ch75, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 62.5
Std Dev 0.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

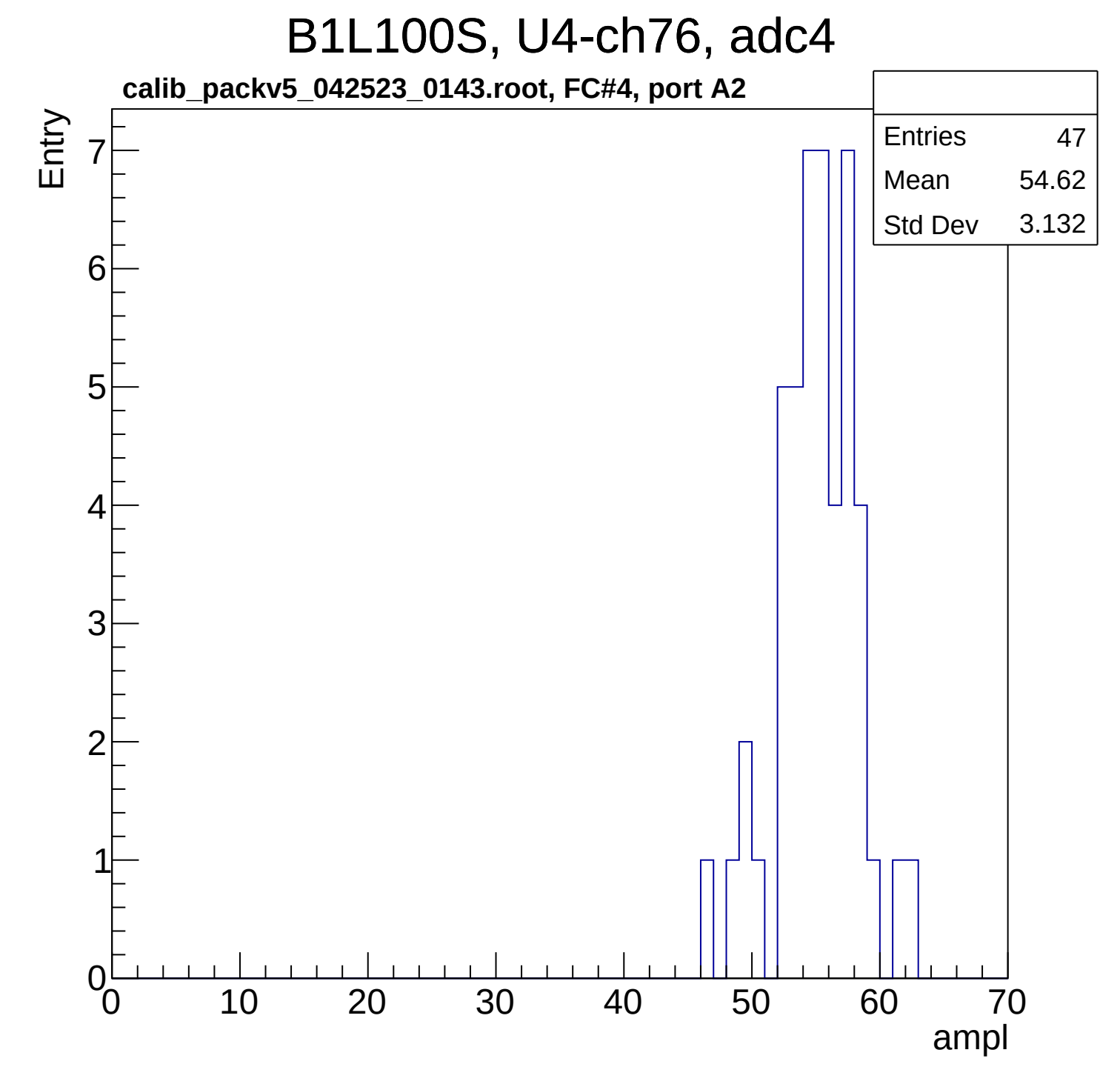

B1L100S, U4-ch75, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

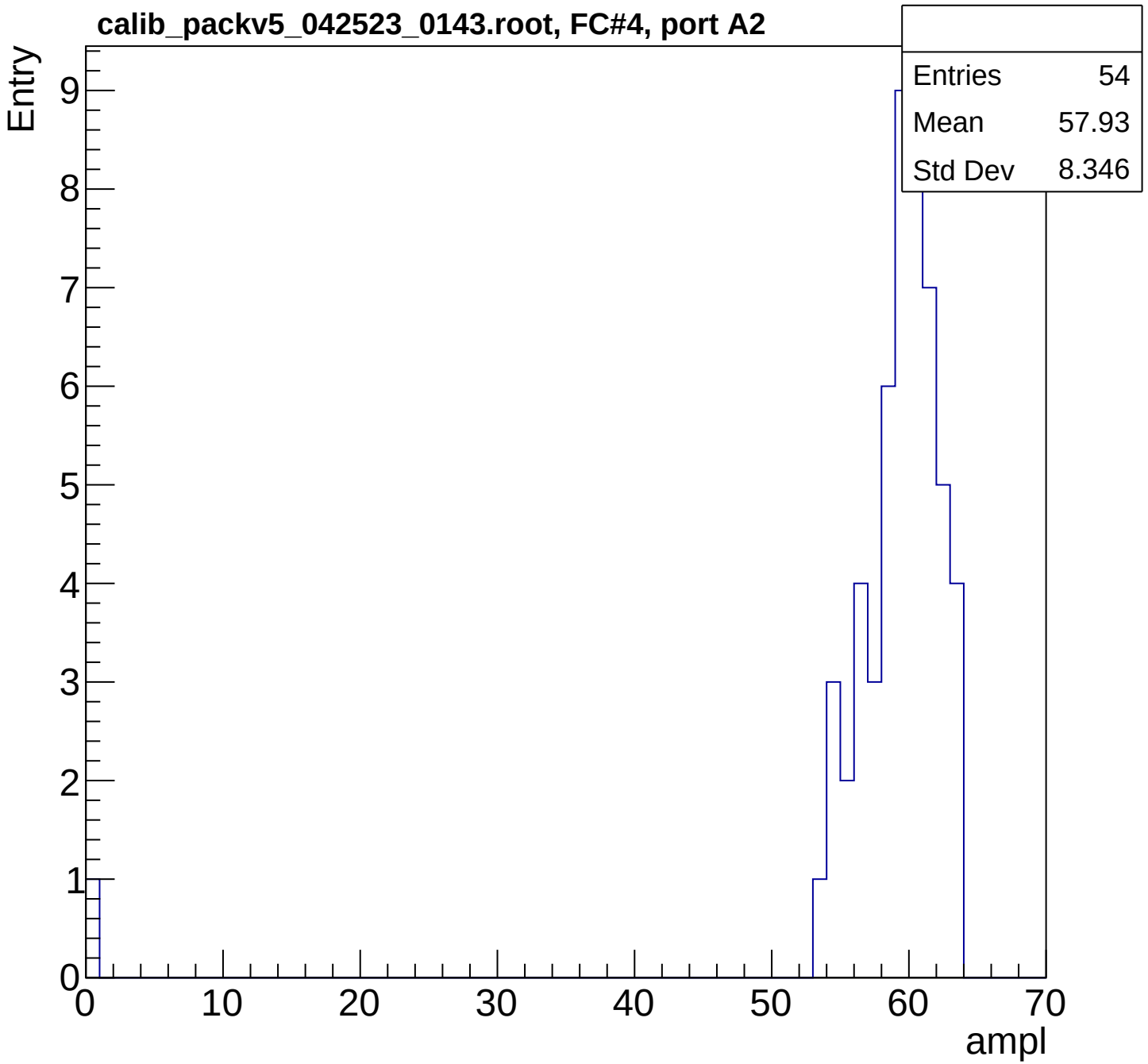

B1L100S, U4-ch76, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 27.11
Std Dev 3.735
Gaus mean : 28.1721
Gaus Width: 3.8058
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

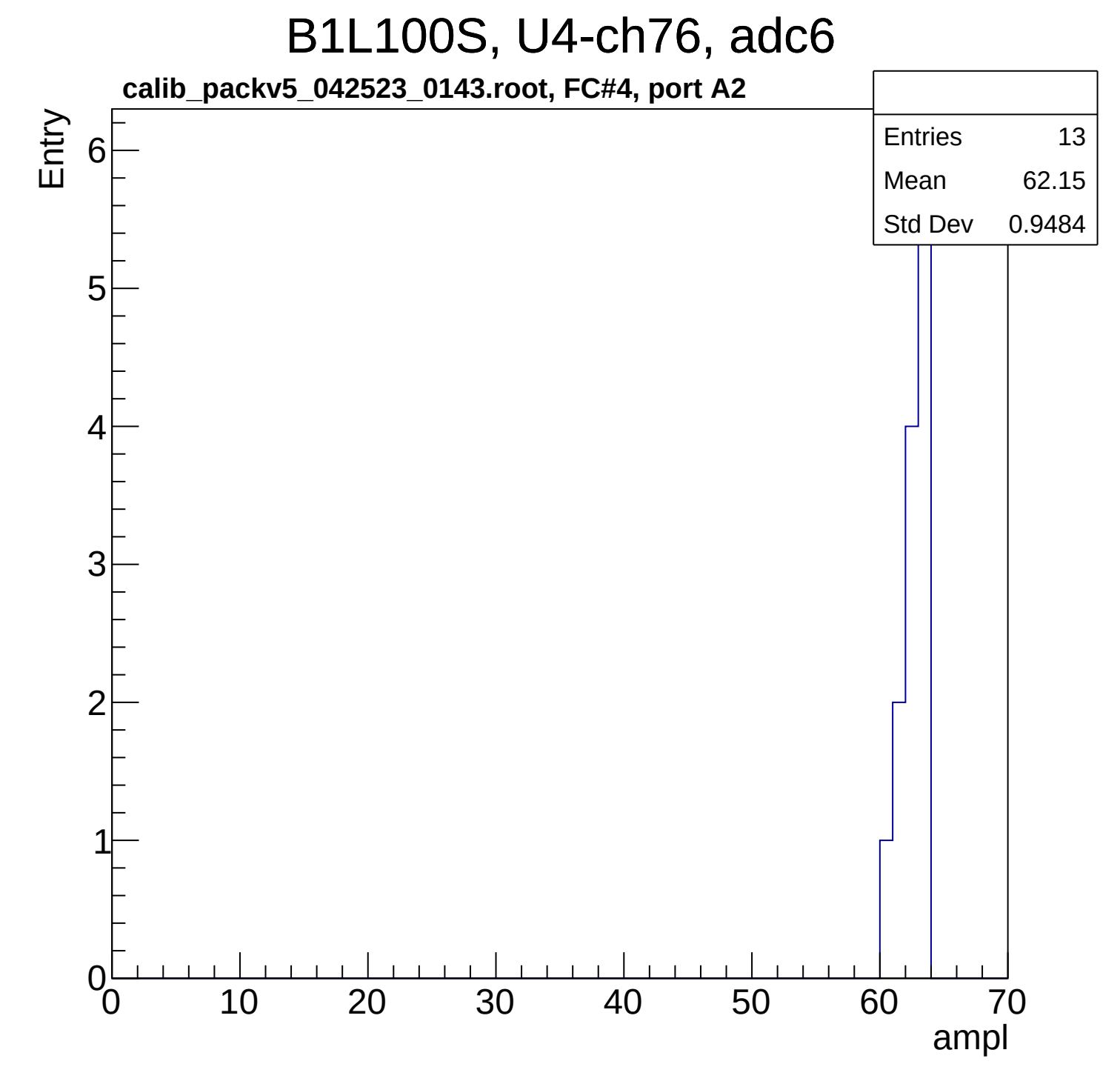

B1L100S, U4-ch76, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 91
Mean 34.96
Std Dev 4.084
Gaus mean : 35.9059
Gaus Width: 4.0277
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

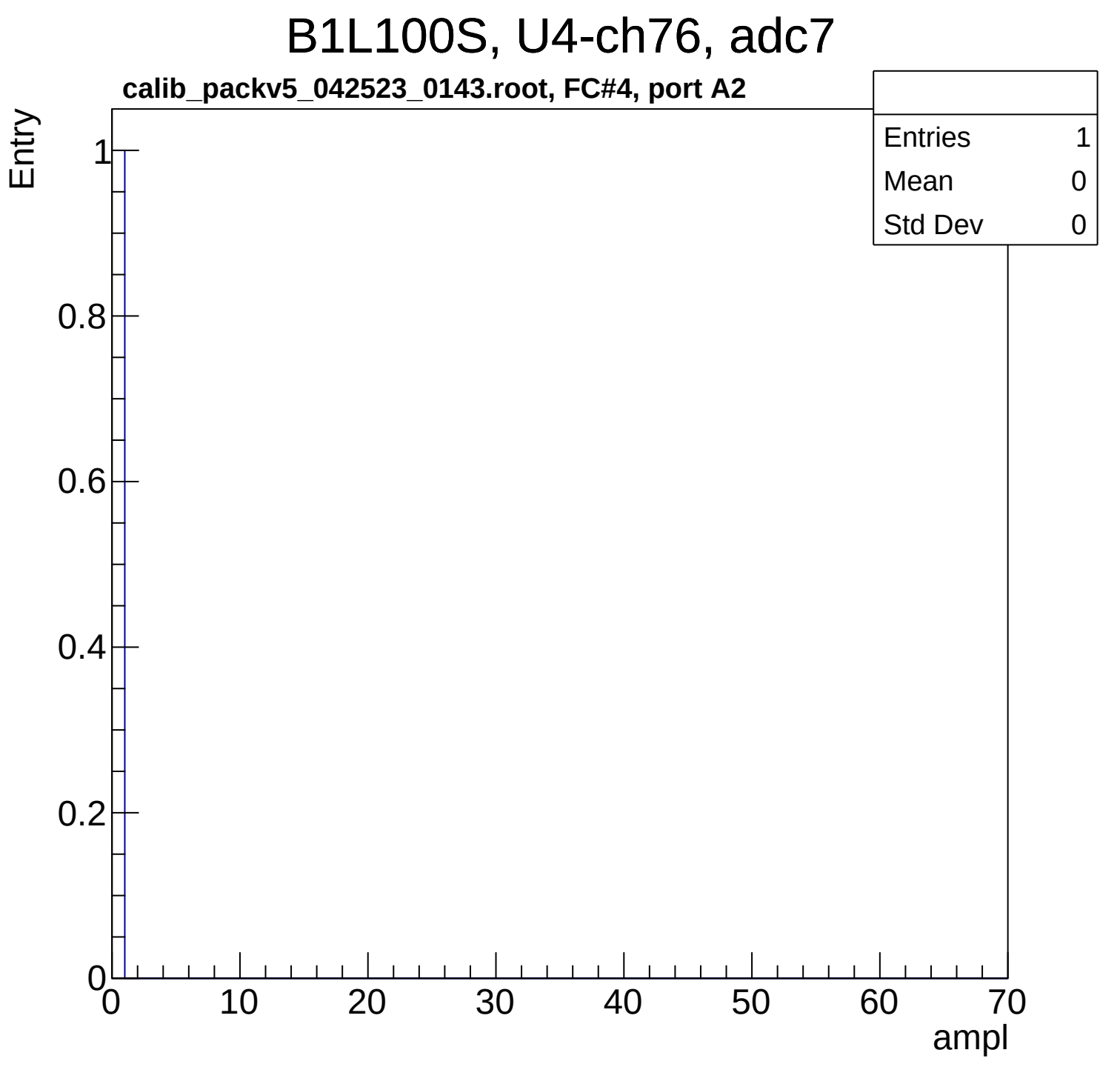

B1L100S, U4-ch76, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 42.06
Std Dev 3.087
Gaus mean : 42.8285
Gaus Width: 2.9739
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

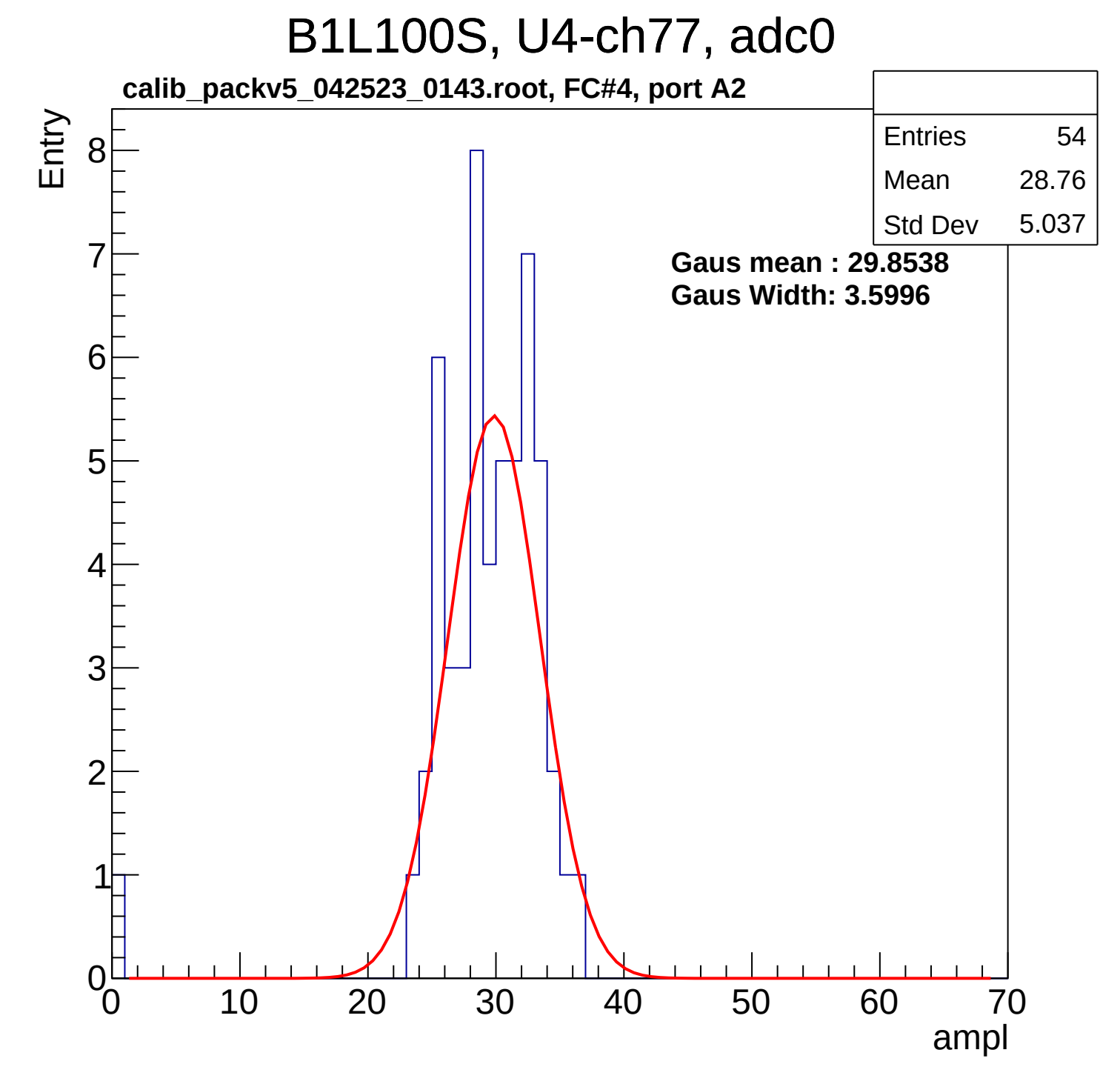

B1L100S, U4-ch76, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 49.27
Std Dev 2.746
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

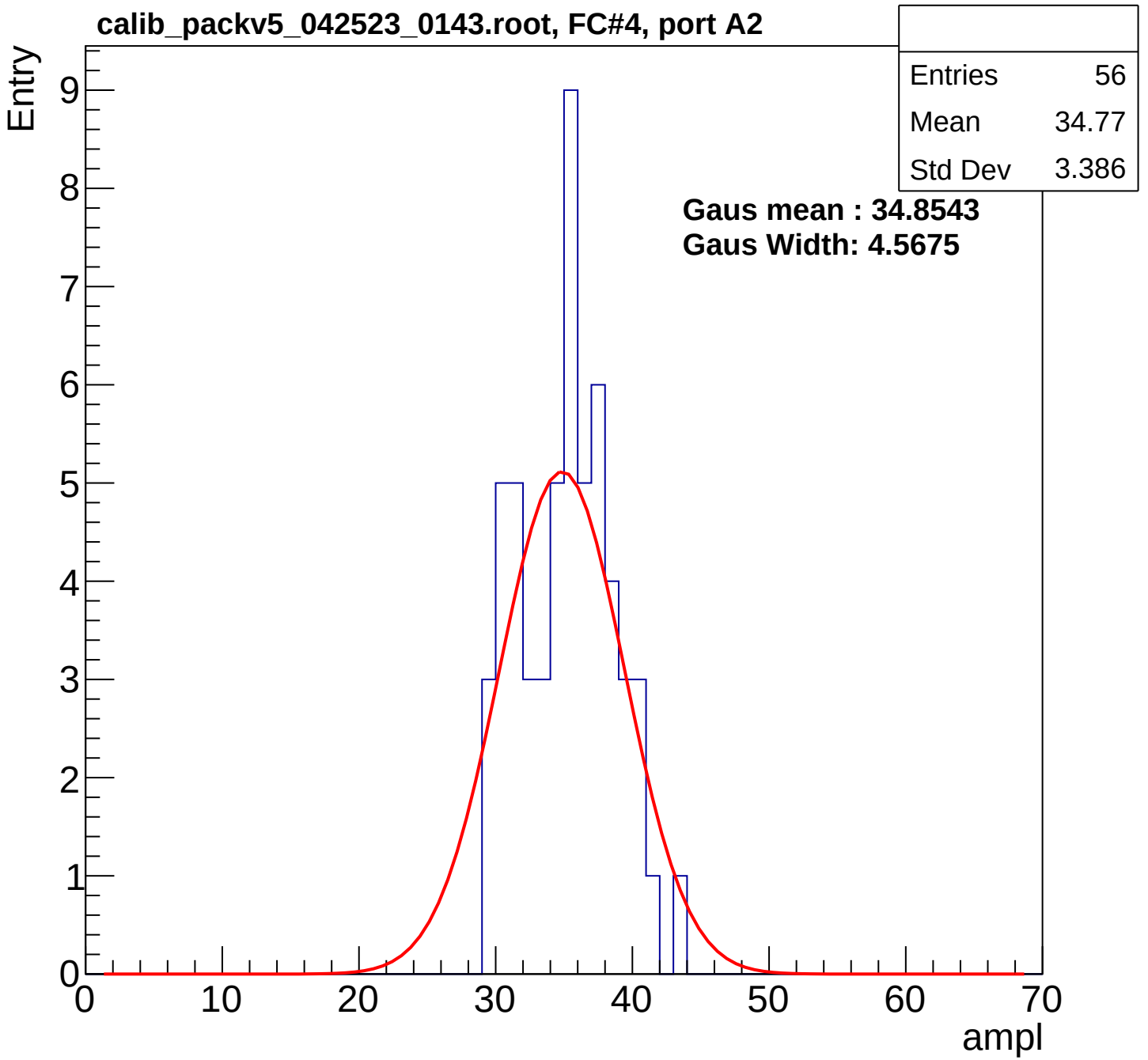

B1L100S, U4-ch76, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 54.62
Std Dev 3.132
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

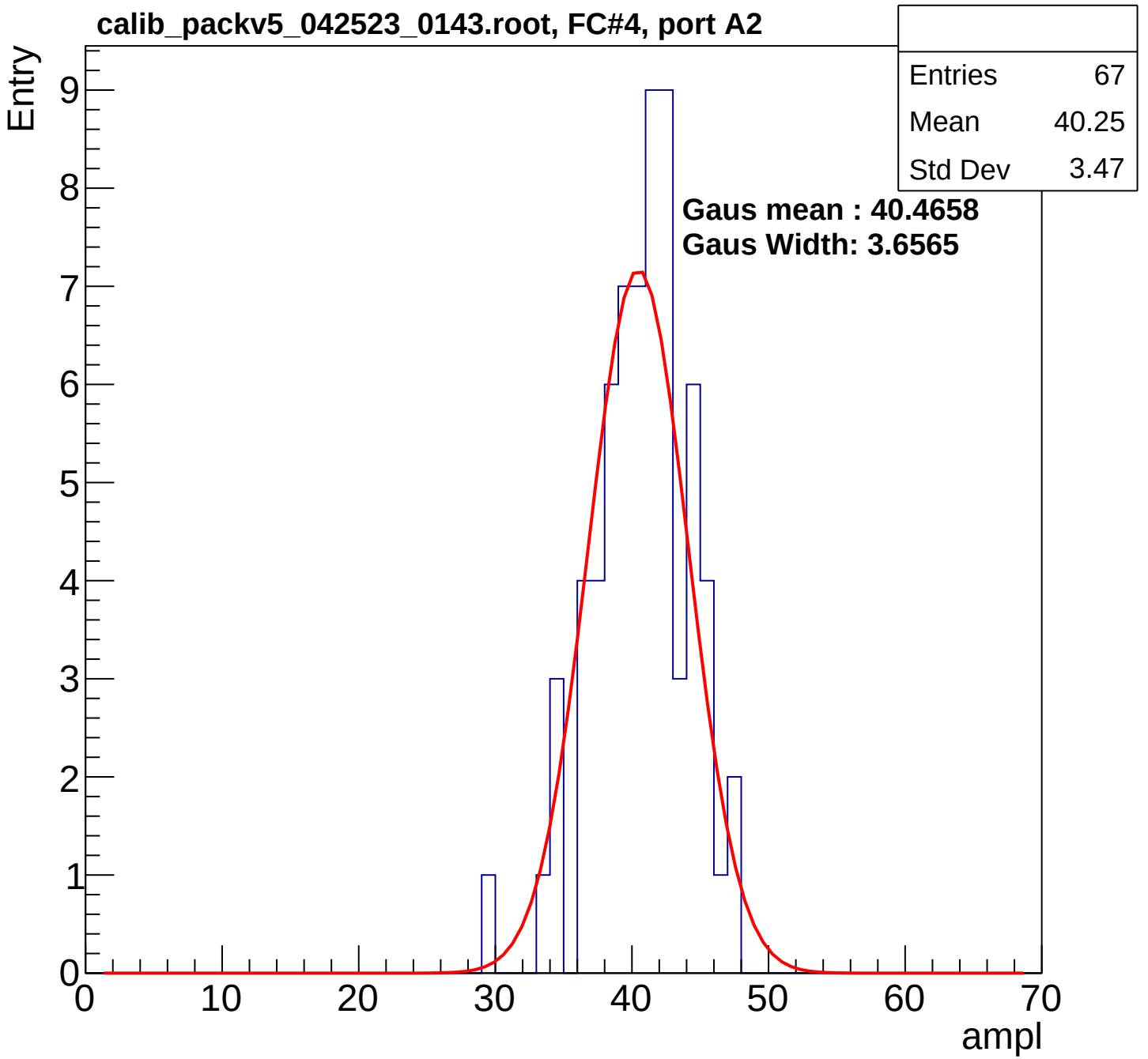

B1L100S, U4-ch76, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 57.93
Std Dev 8.346
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

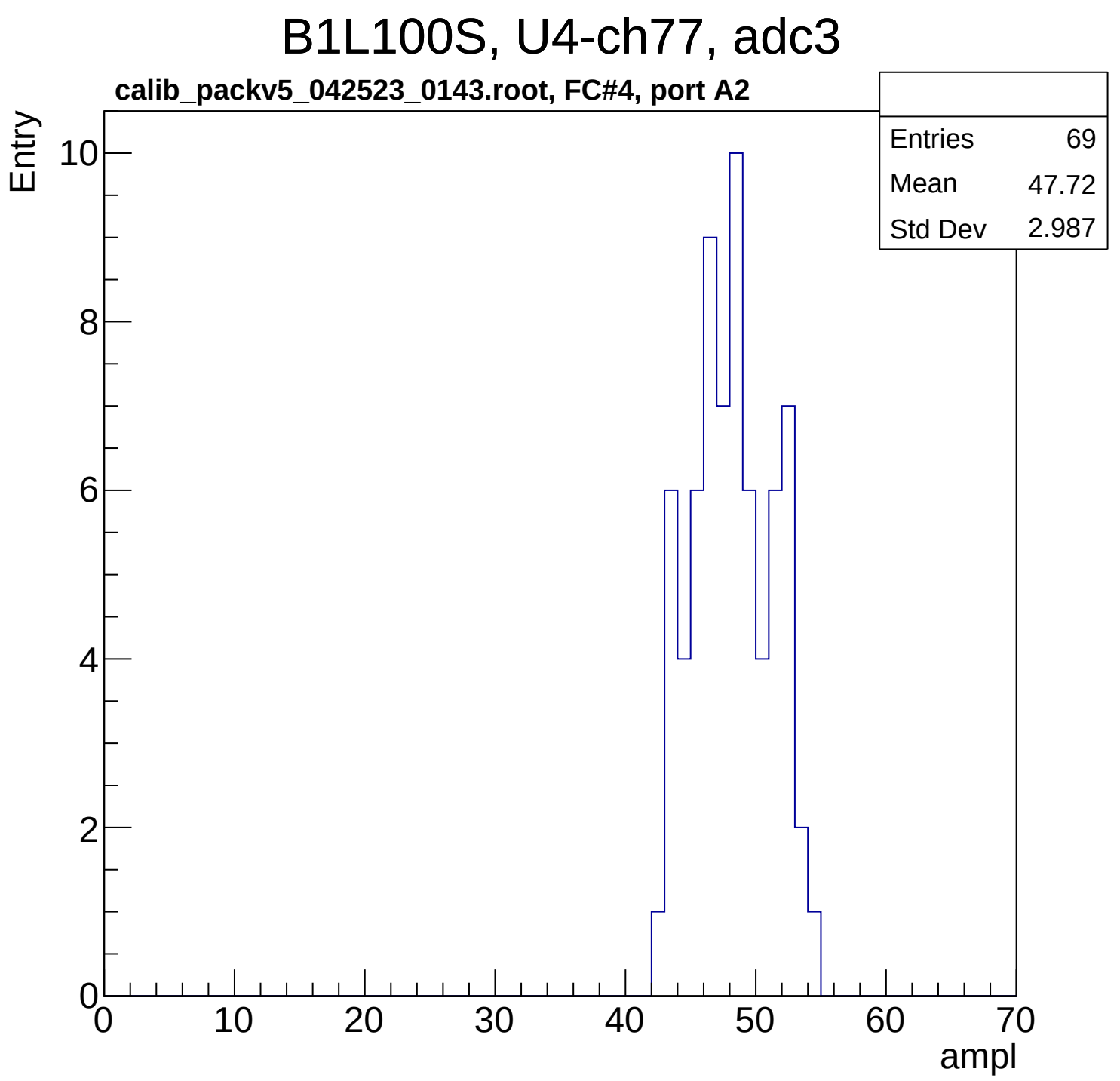

B1L100S, U4-ch76, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 13
Mean 62.15
Std Dev 0.9484
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

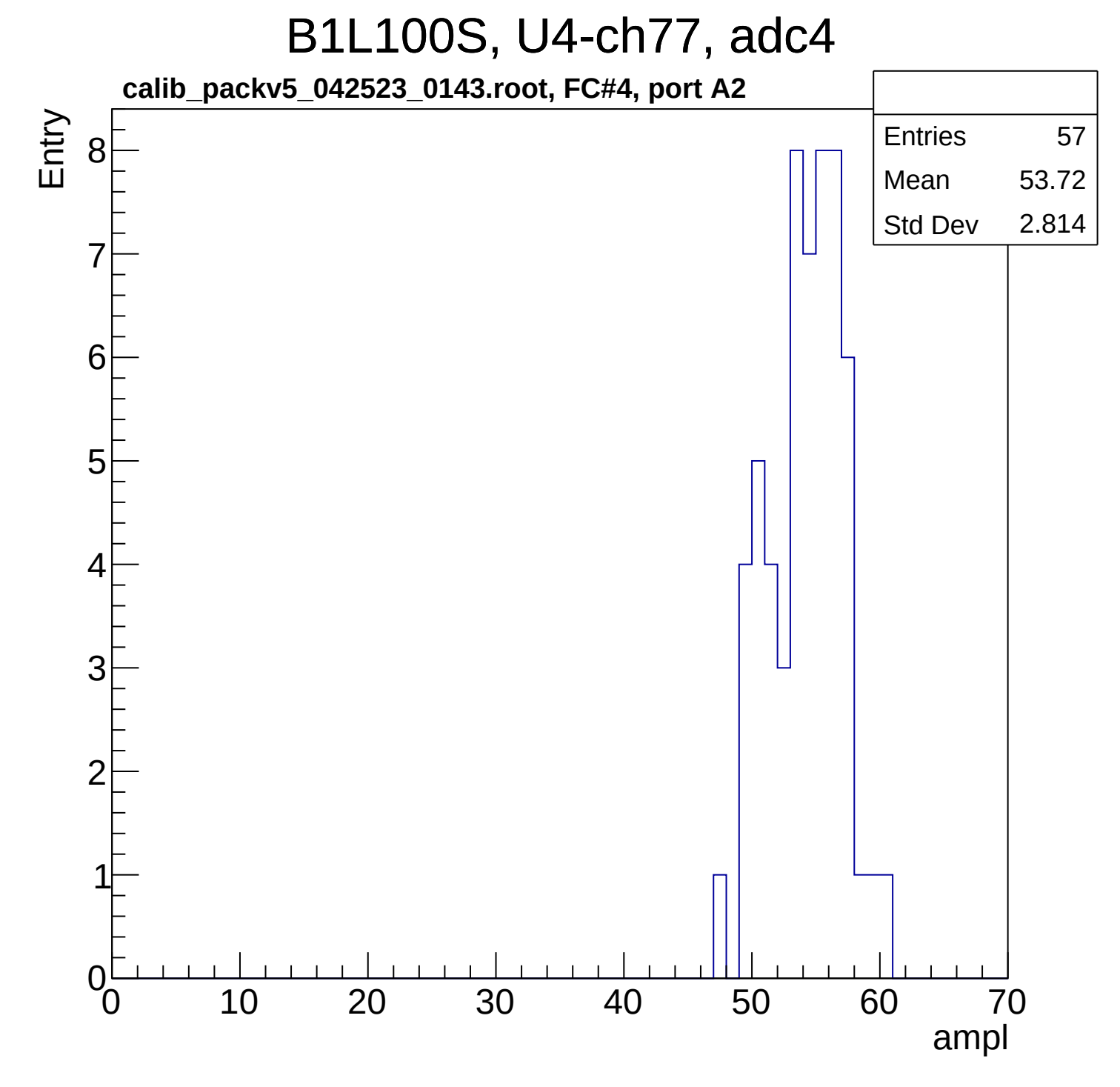

B1L100S, U4-ch76, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

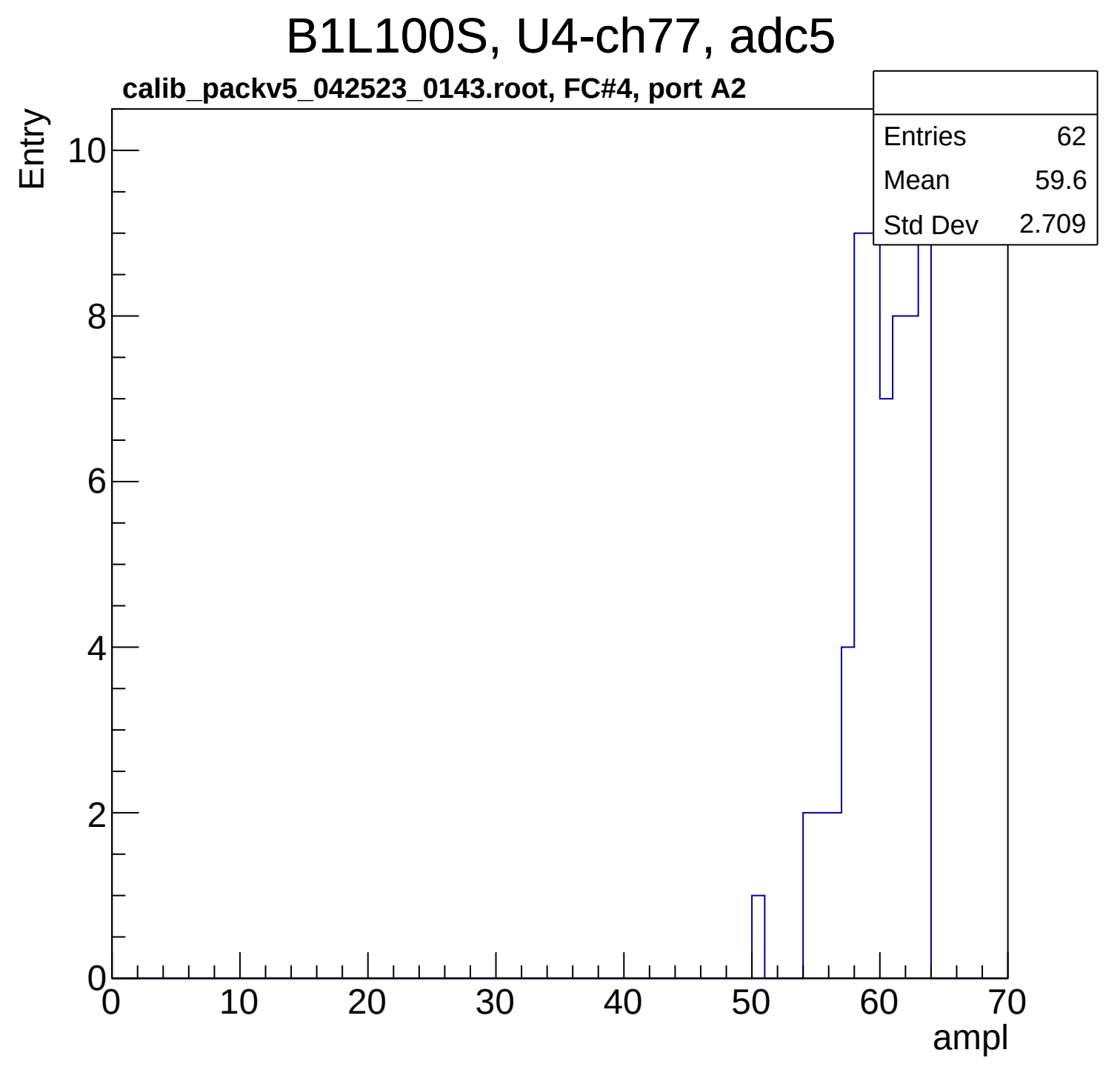

B1L100S, U4-ch77, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 28.76
Std Dev 5.037
Gaus mean : 29.8538
Gaus Width: 3.5996
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

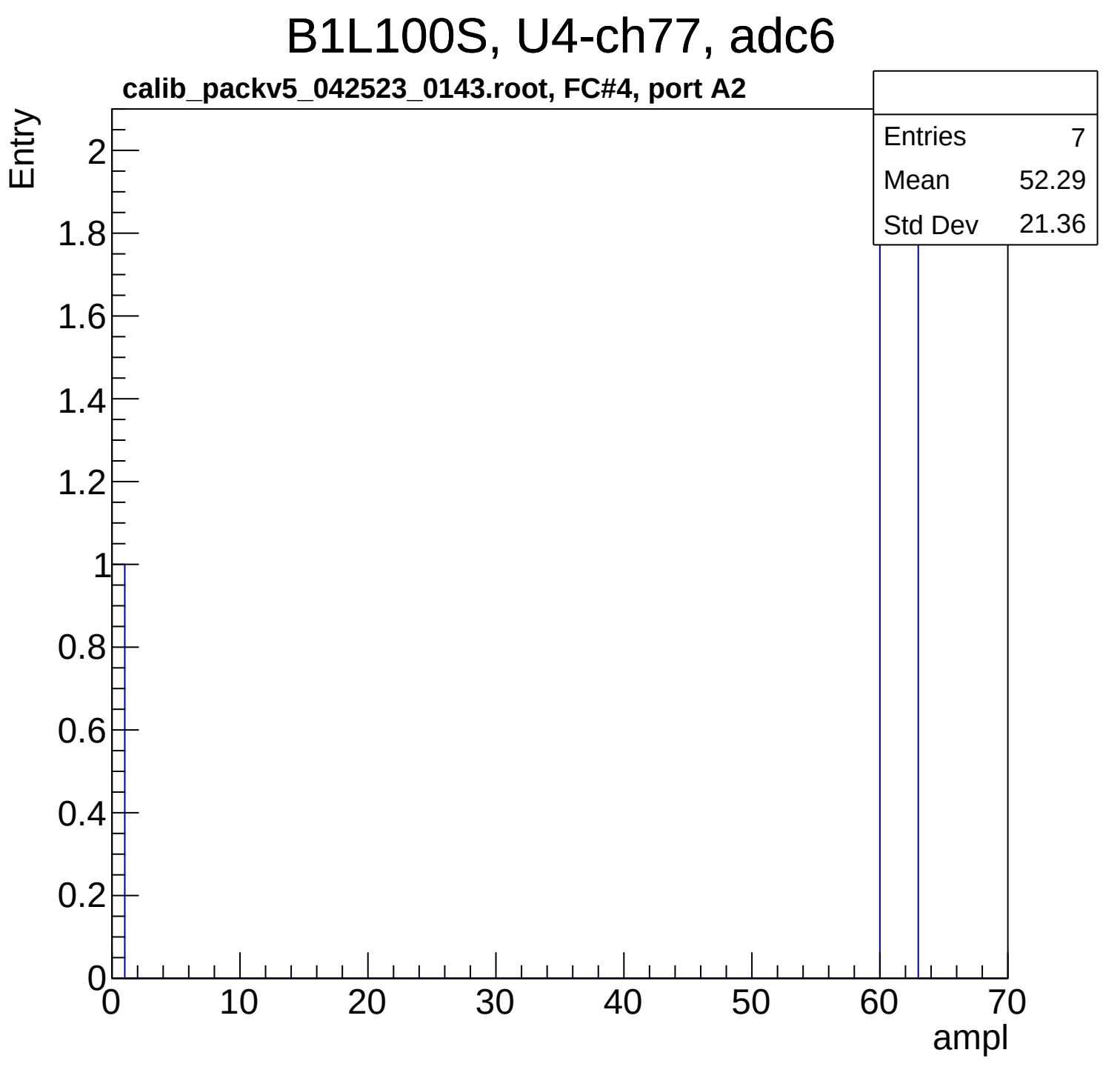

B1L100S, U4-ch77, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 34.77
Std Dev 3.386
Gaus mean : 34.8543
Gaus Width: 4.5675
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

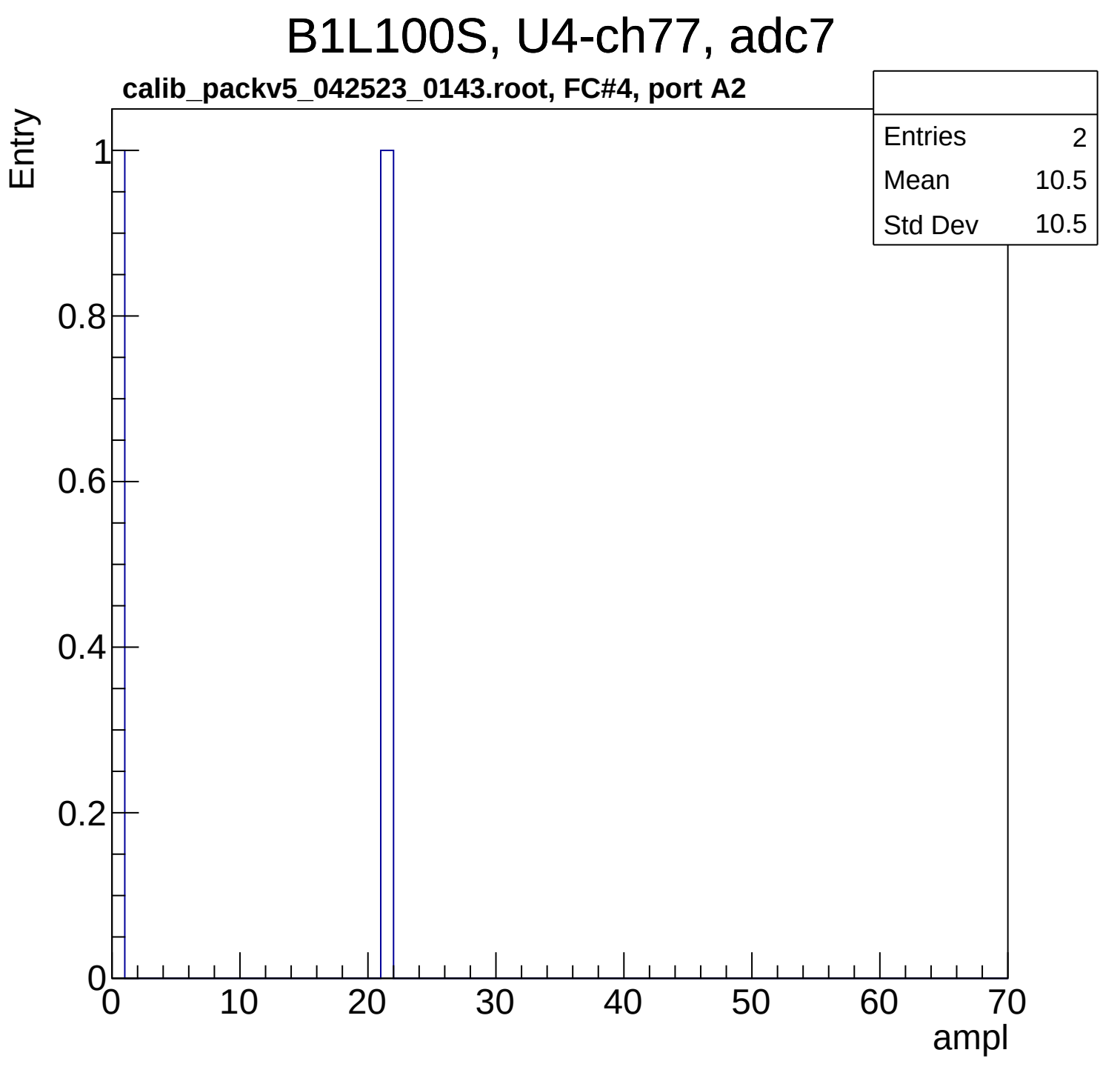

B1L100S, U4-ch77, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 40.25
Std Dev 3.47
Gaus mean : 40.4658
Gaus Width: 3.6565
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

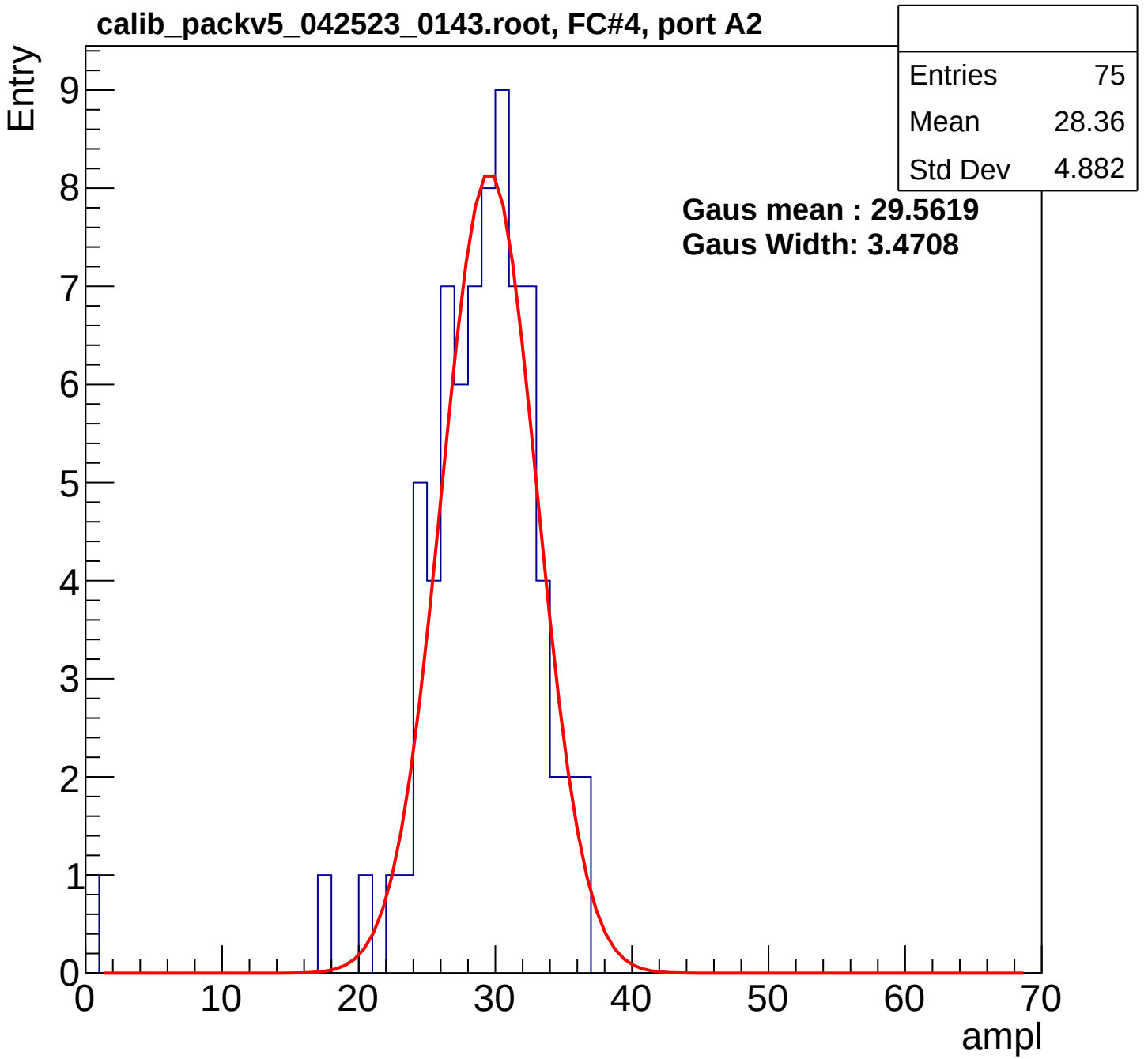

B1L100S, U4-ch77, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 47.72
Std Dev 2.987
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

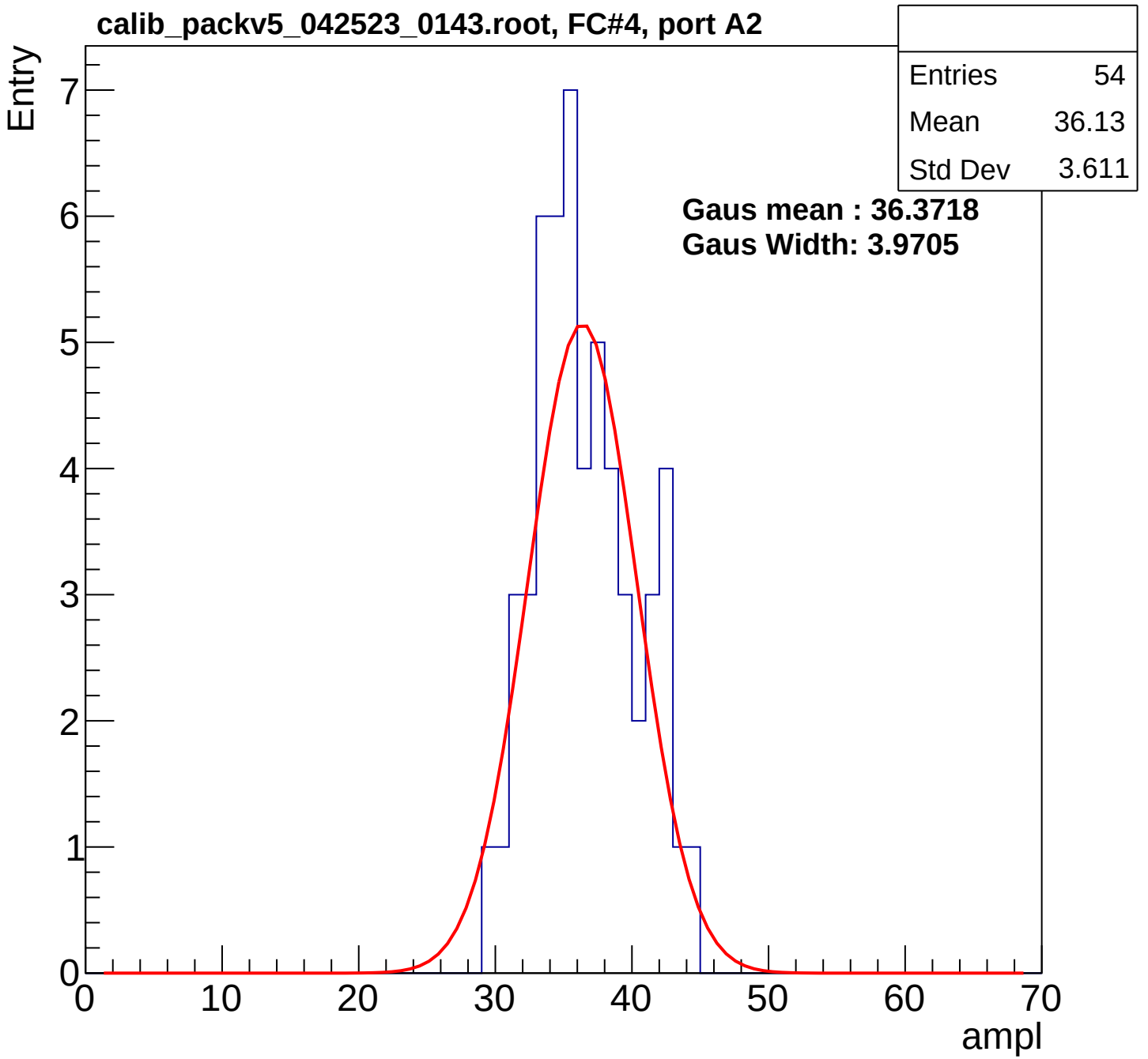

B1L100S, U4-ch77, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 53.72
Std Dev 2.814
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

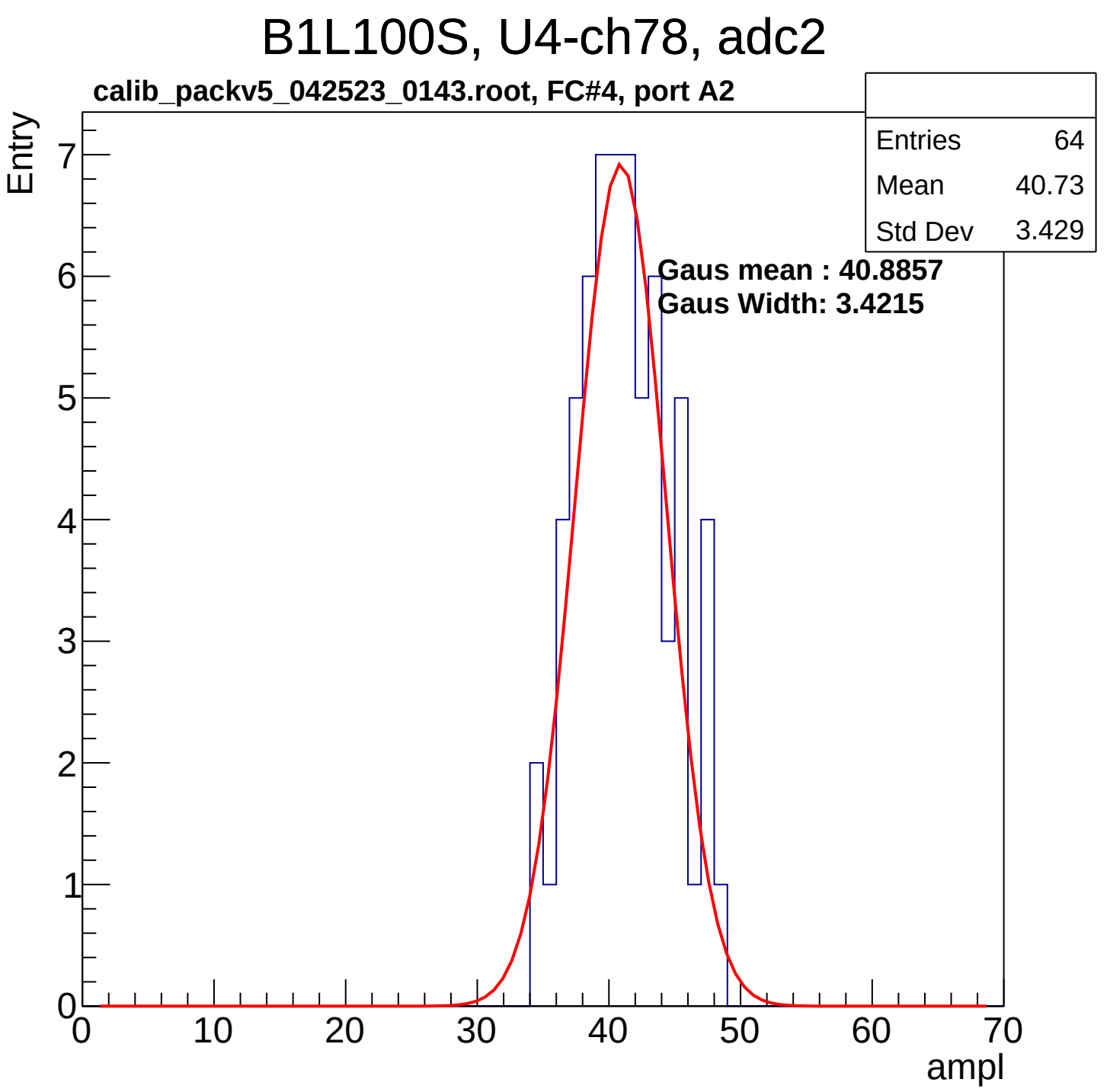

B1L100S, U4-ch77, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 59.6
Std Dev 2.709
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

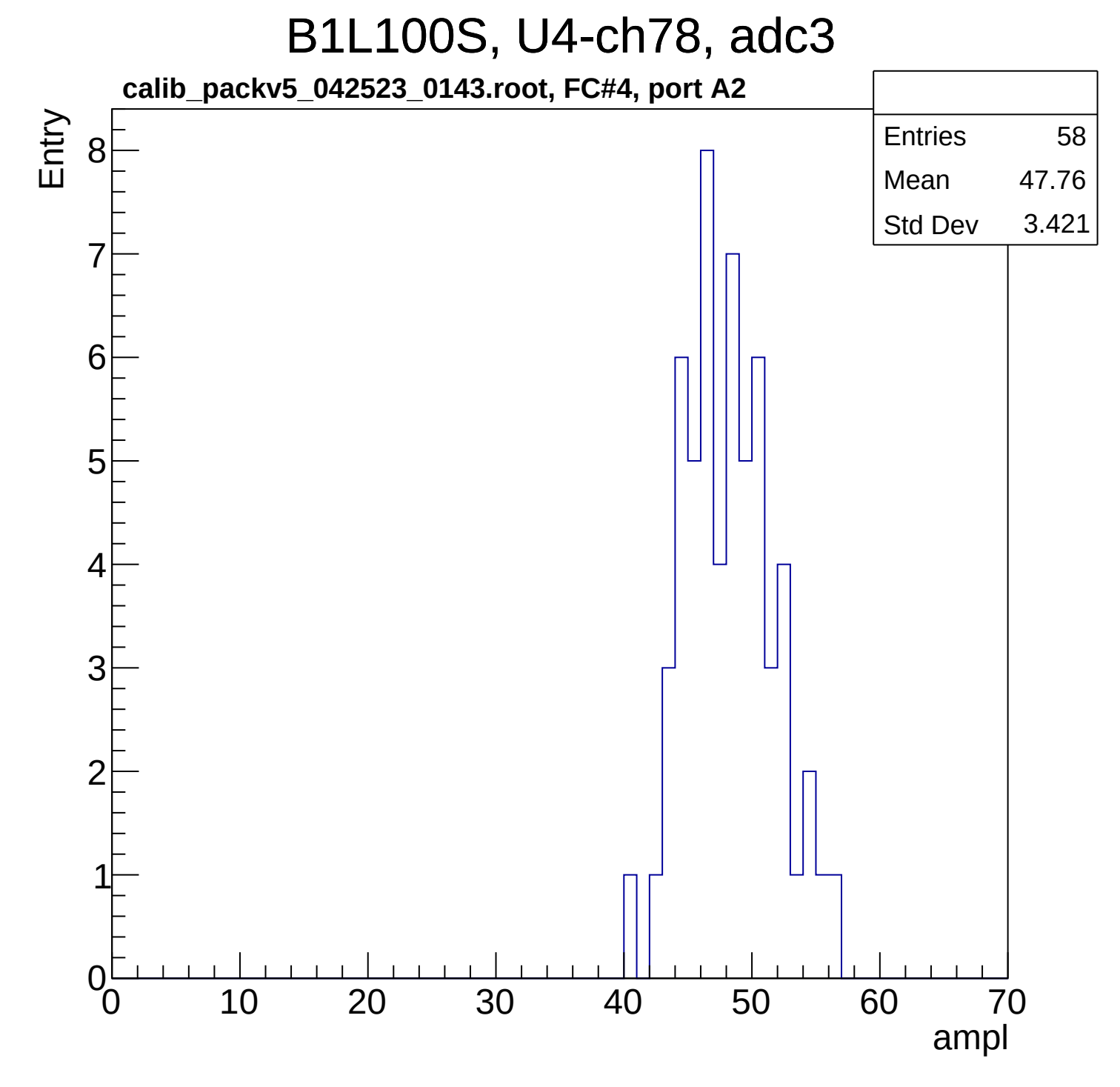

B1L100S, U4-ch77, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 52.29
Std Dev 21.36
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

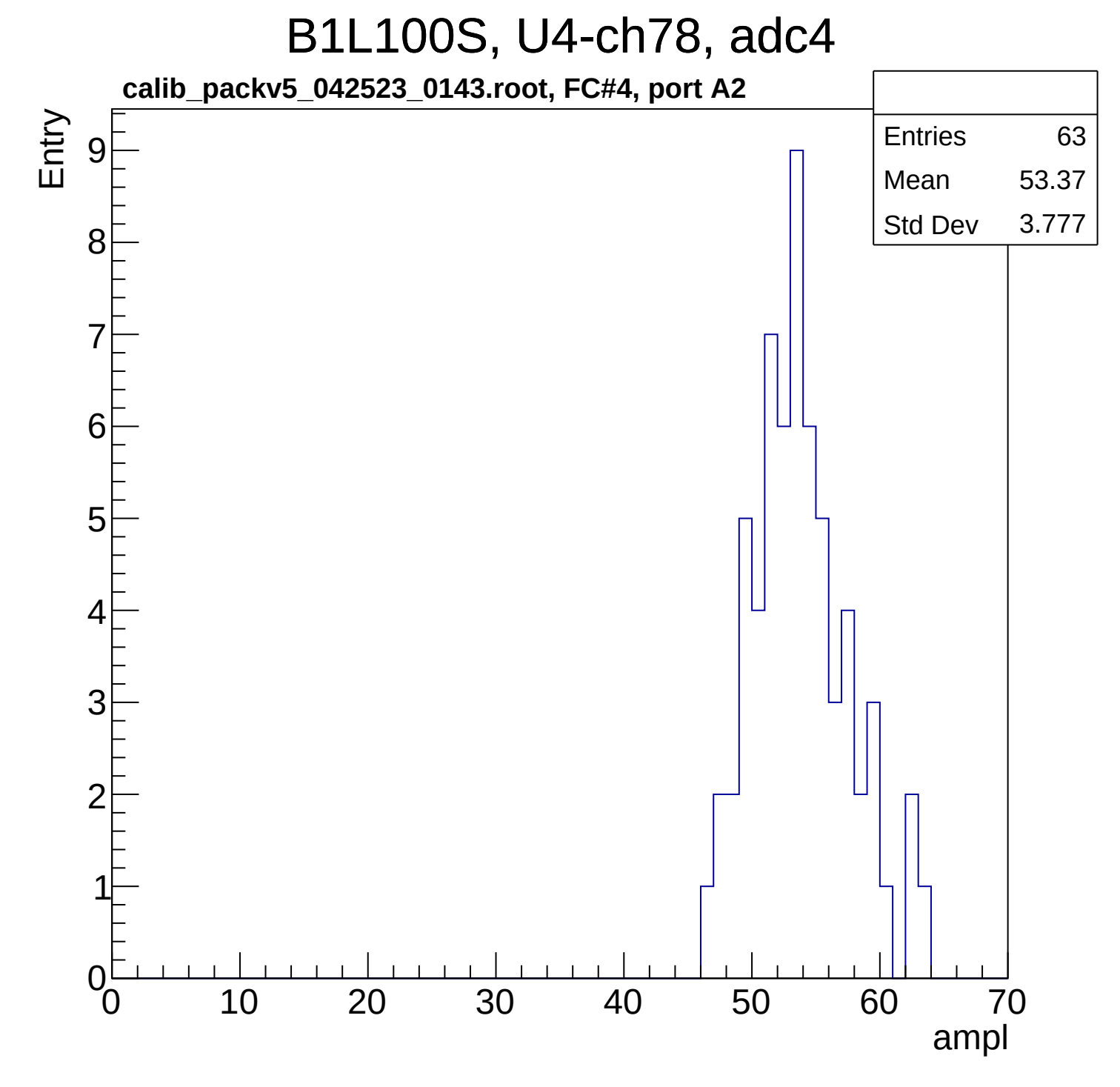

B1L100S, U4-ch77, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 10.5
Std Dev 10.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

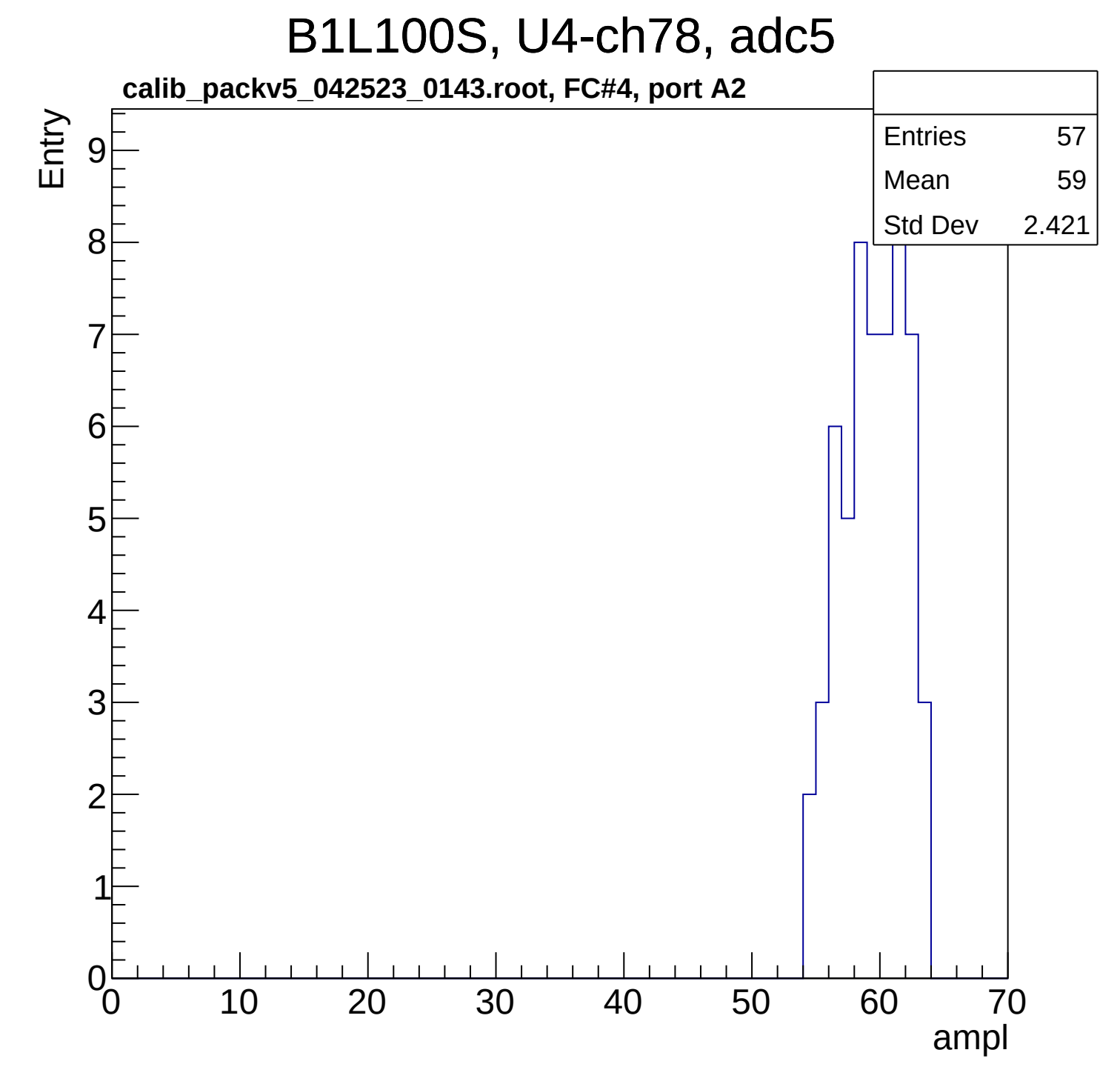

B1L100S, U4-ch78, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 28.36
Std Dev 4.882
Gaus mean : 29.5619
Gaus Width: 3.4708
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

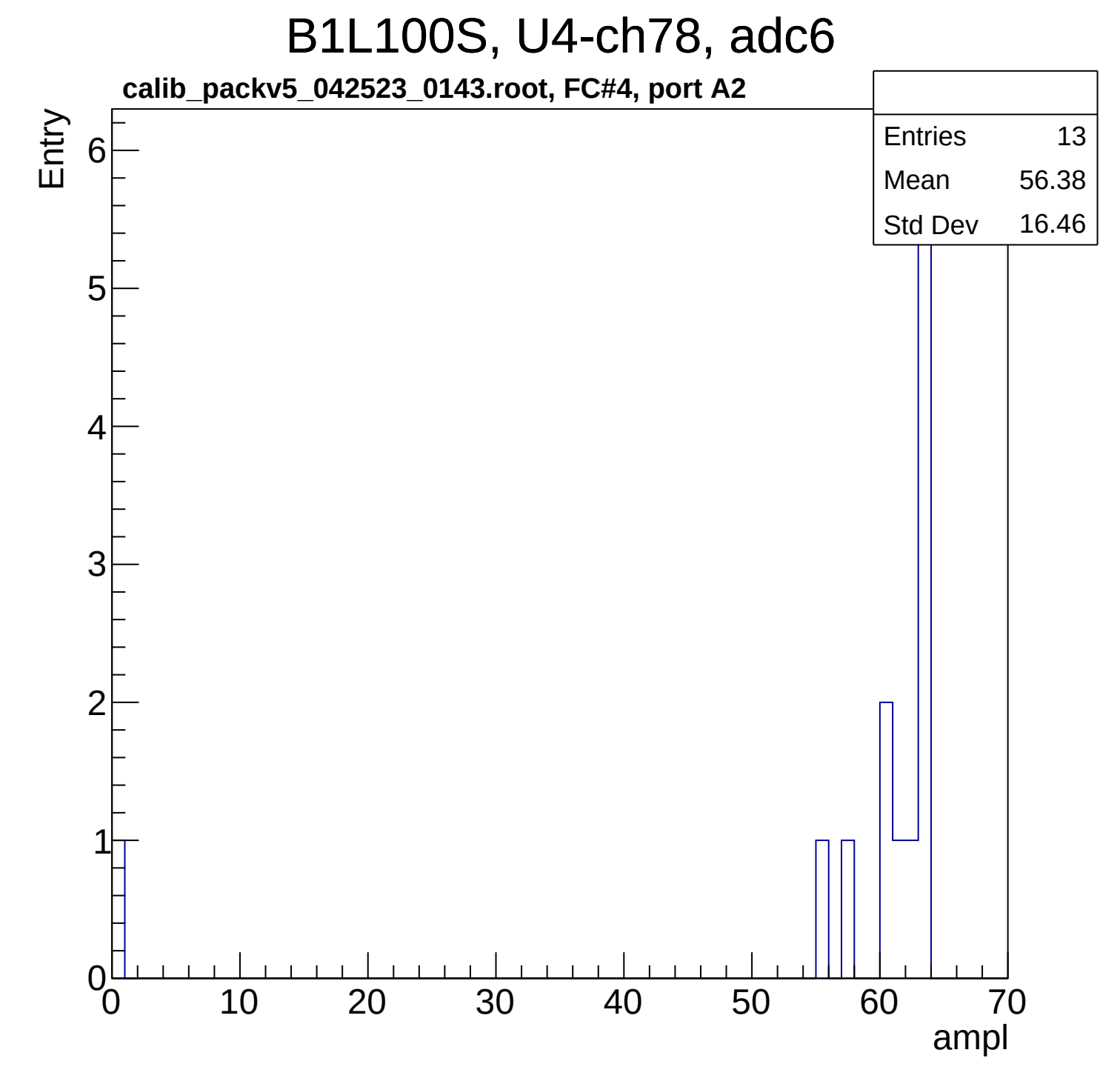

B1L100S, U4-ch78, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 36.13
Std Dev 3.611
Gaus mean : 36.3718
Gaus Width: 3.9705
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

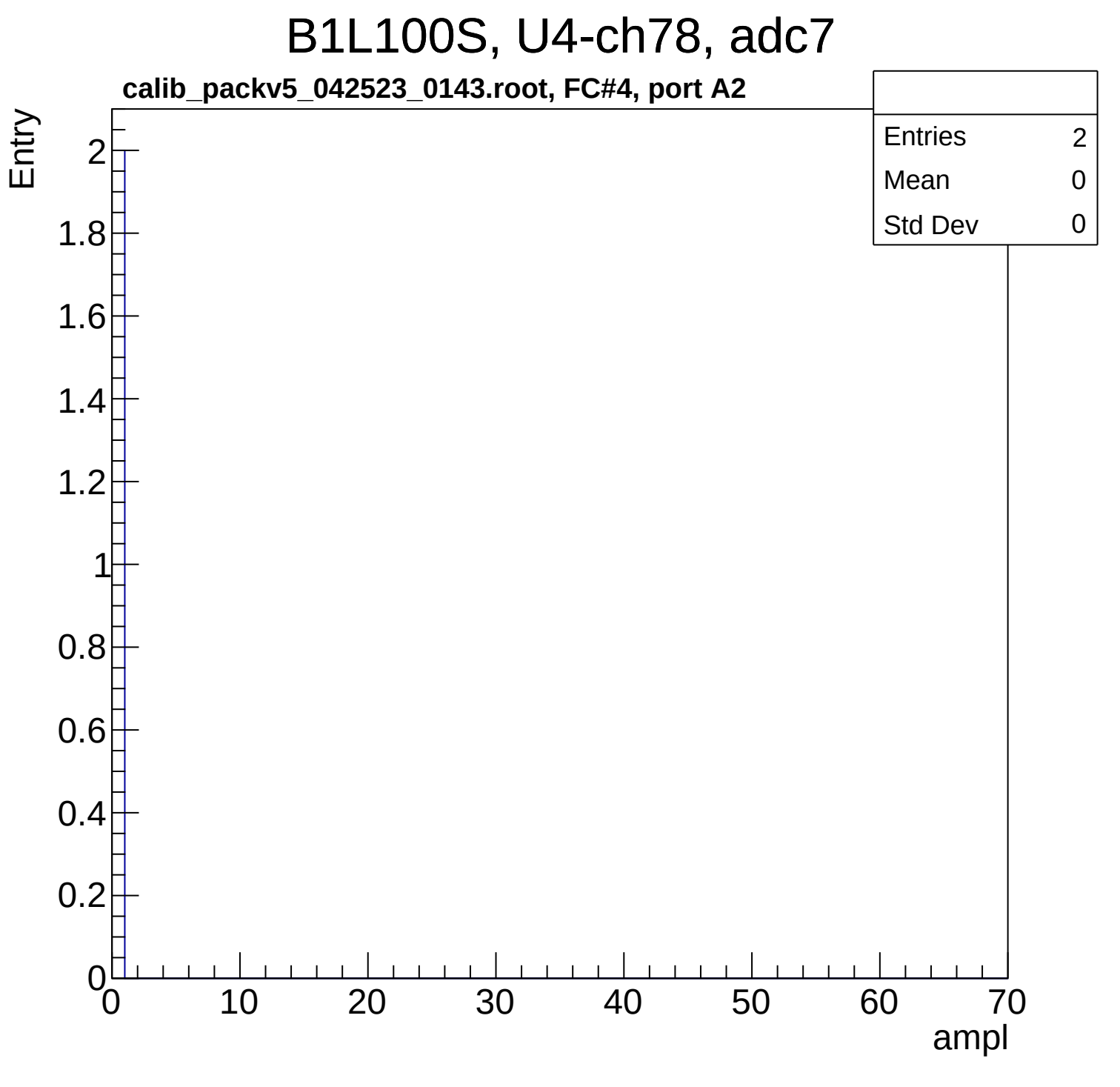

B1L100S, U4-ch78, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 40.73
Std Dev 3.429
Gaus mean : 40.8857
Gaus Width: 3.4215
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

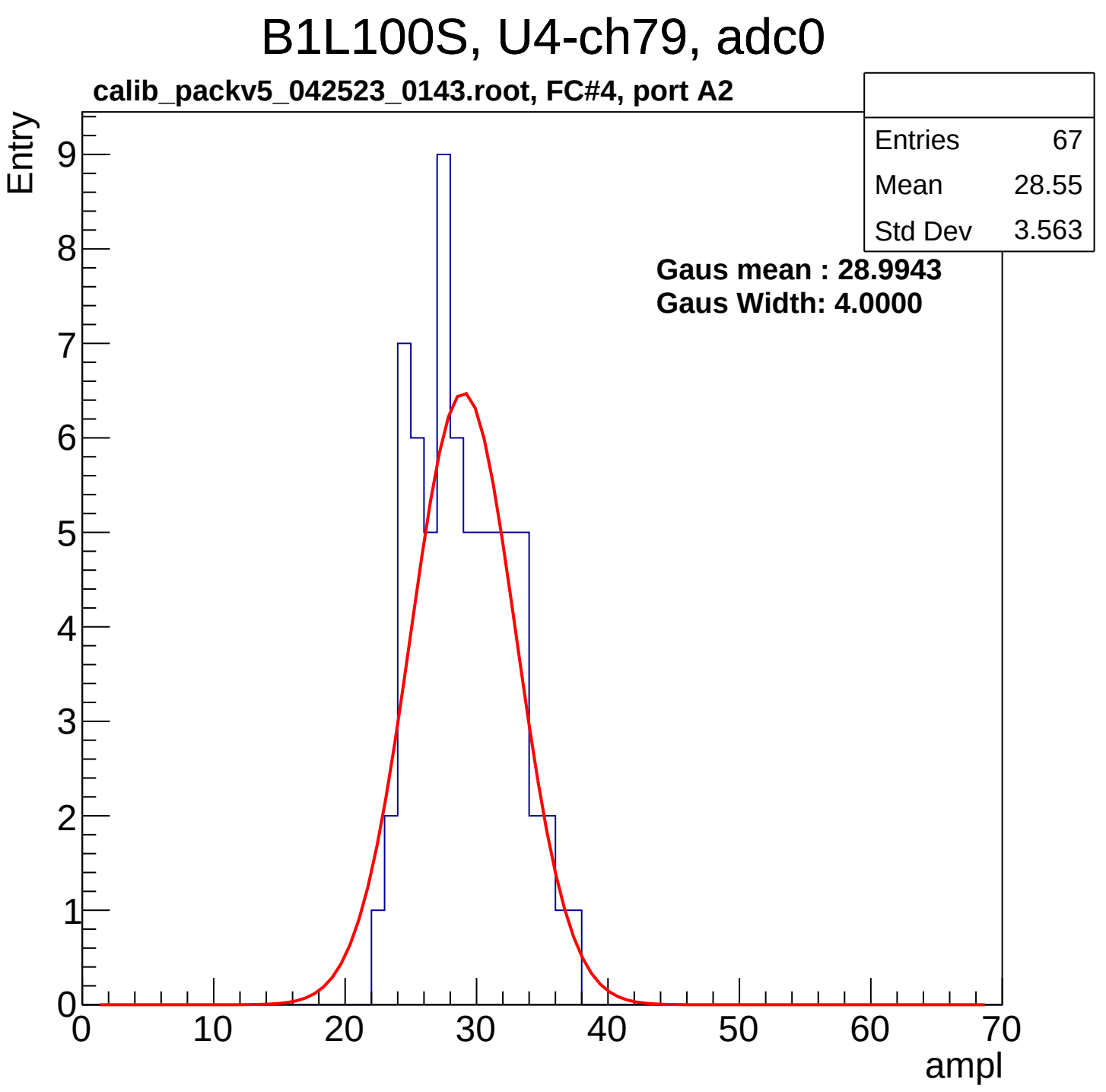

B1L100S, U4-ch78, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 47.76
Std Dev 3.421
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

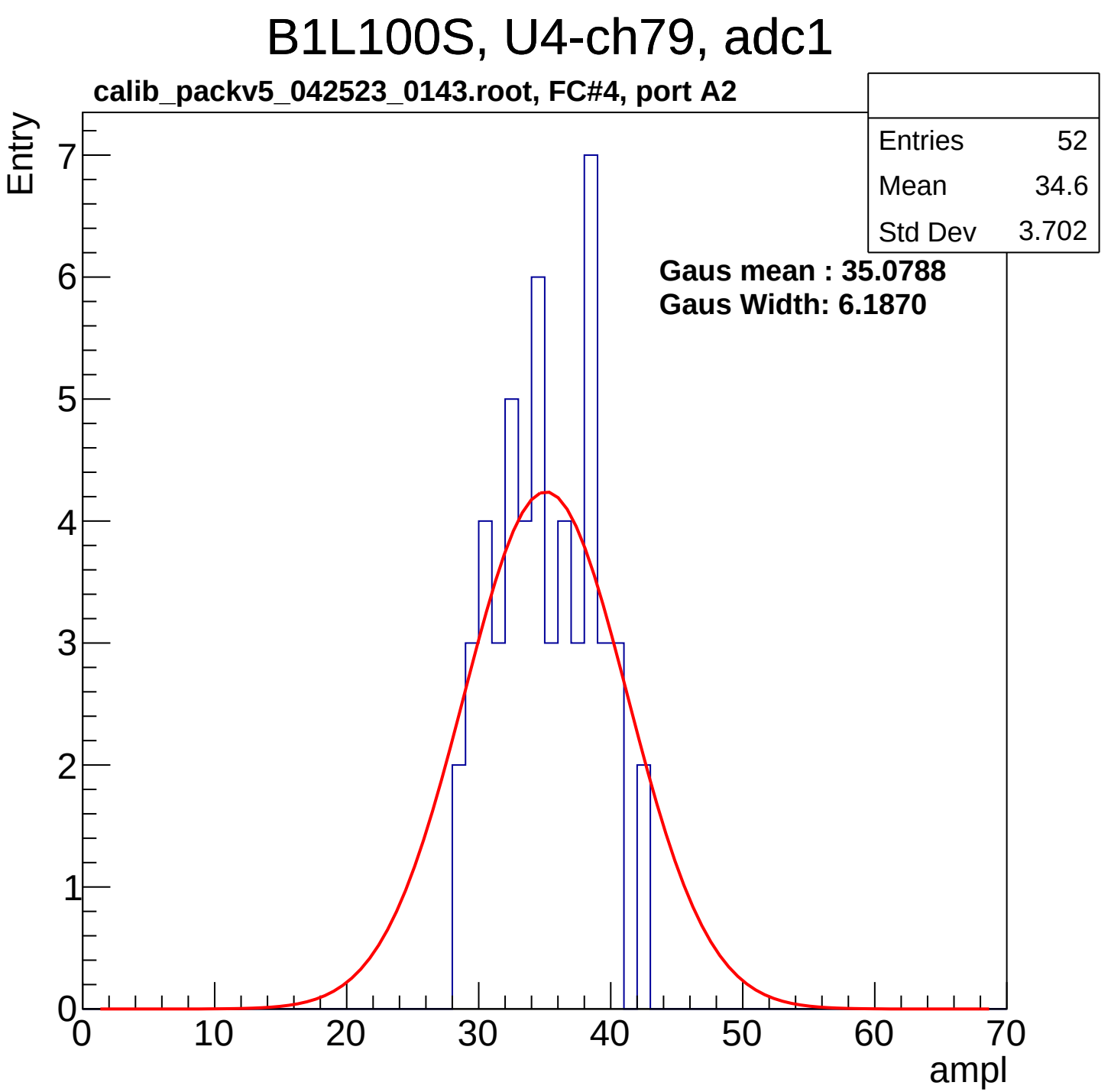

B1L100S, U4-ch78, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 53.37
Std Dev 3.777
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

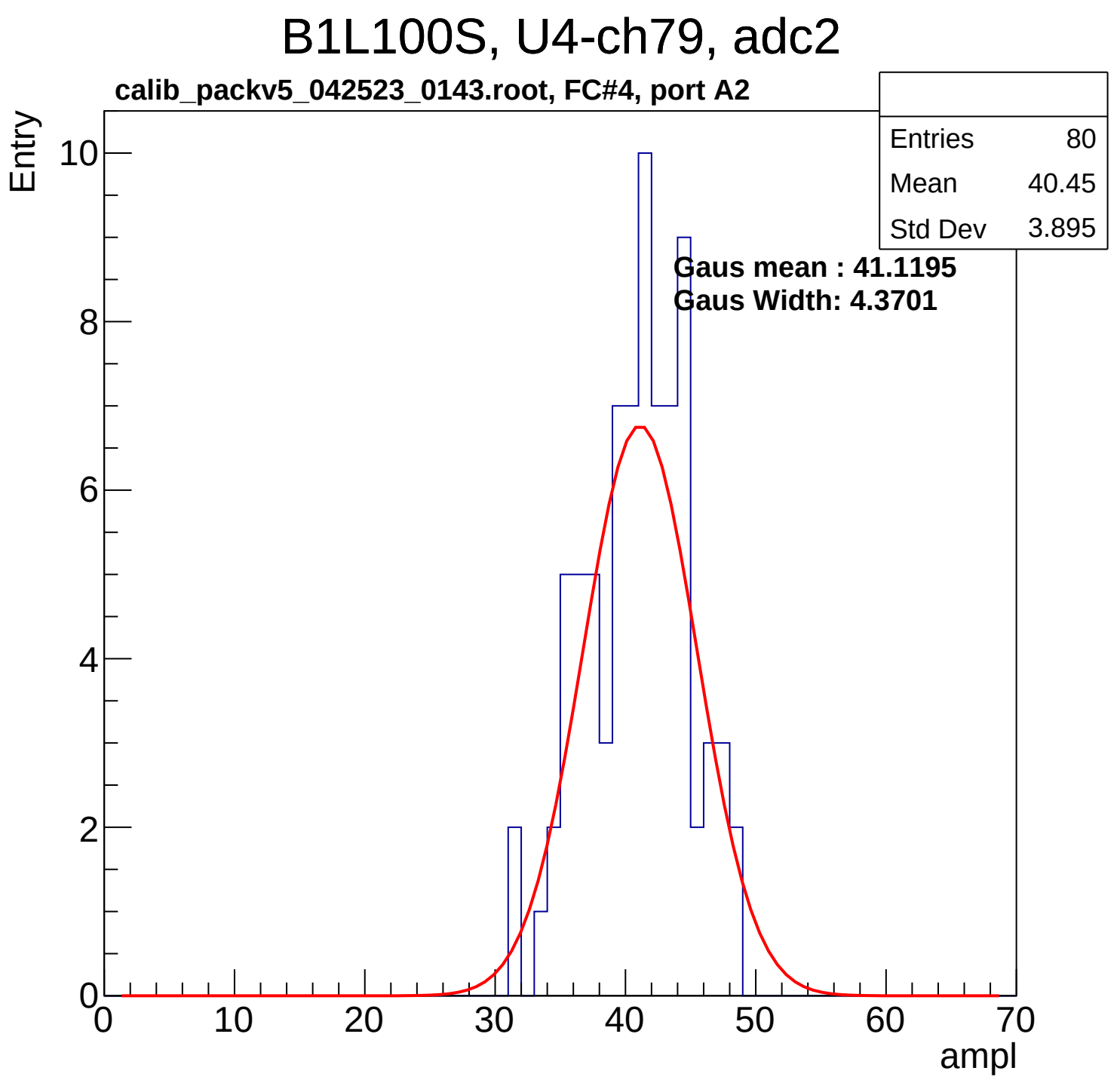

B1L100S, U4-ch78, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 59
Std Dev 2.421
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

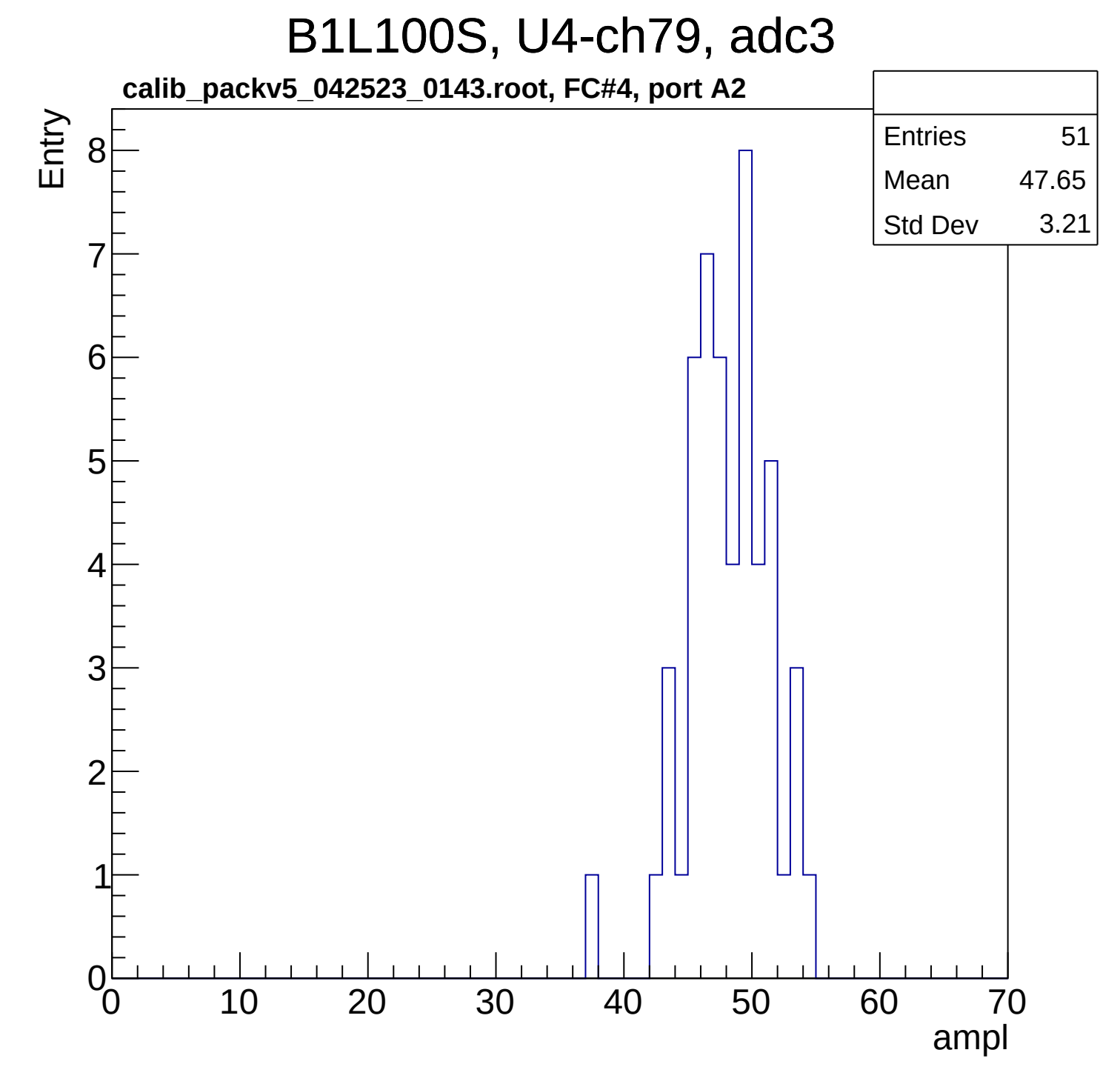

B1L100S, U4-ch78, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 13
Mean 56.38
Std Dev 16.46
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

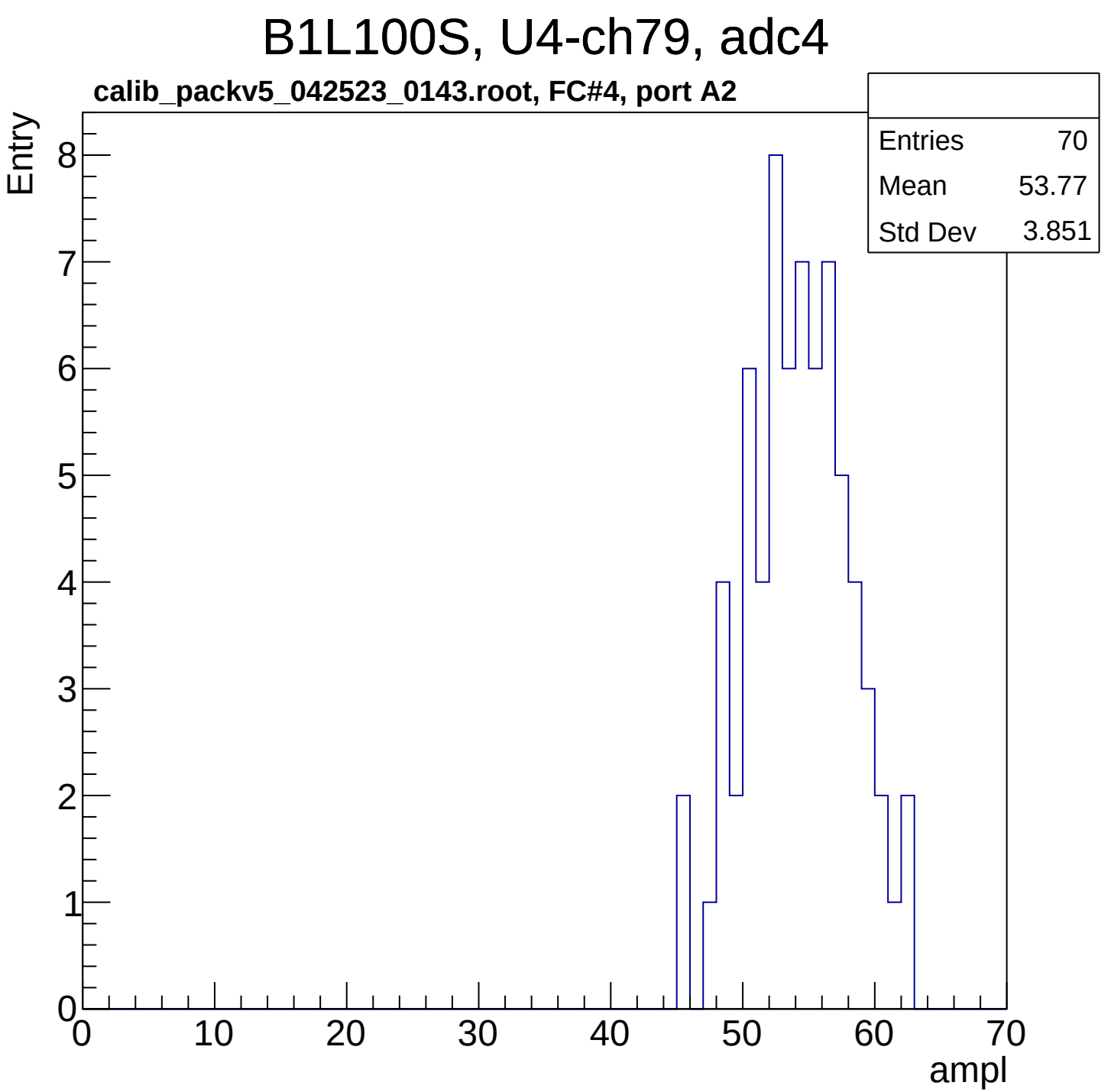

B1L100S, U4-ch78, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

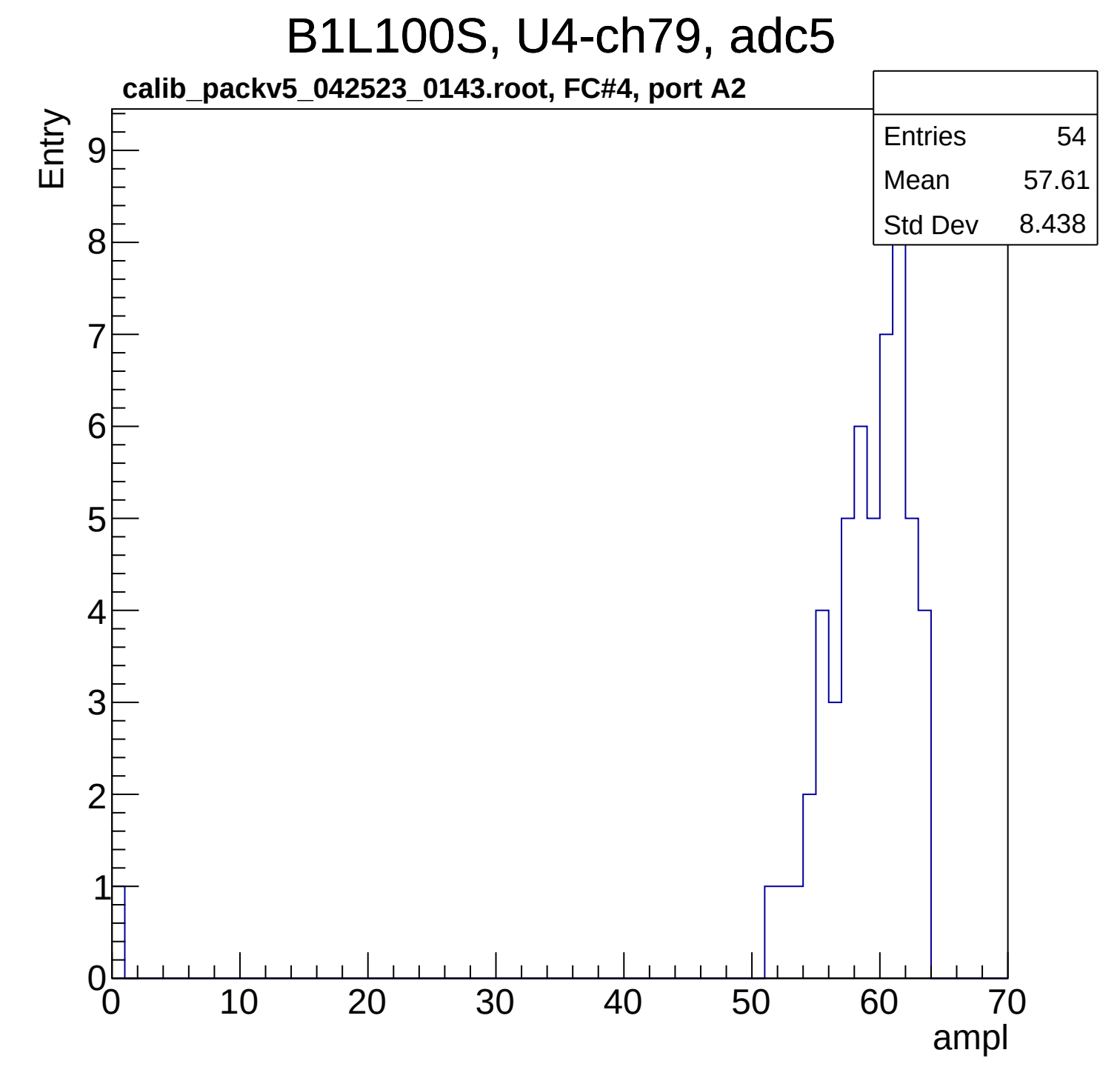

B1L100S, U4-ch79, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 28.55
Std Dev 3.563
Gaus mean : 28.9943
Gaus Width: 4.0000
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

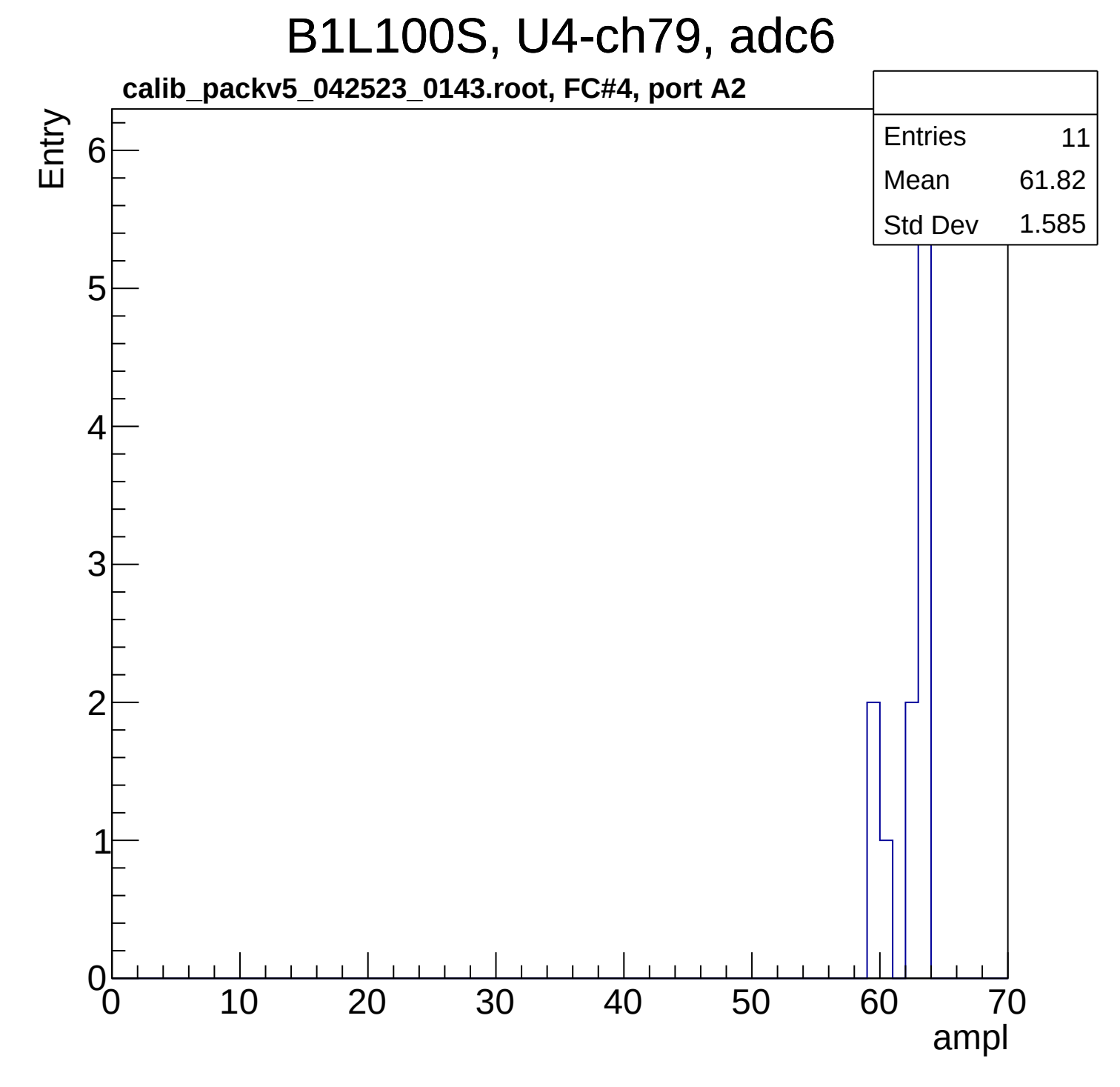

B1L100S, U4-ch79, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 34.6
Std Dev 3.702
Gaus mean : 35.0788
Gaus Width: 6.1870
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

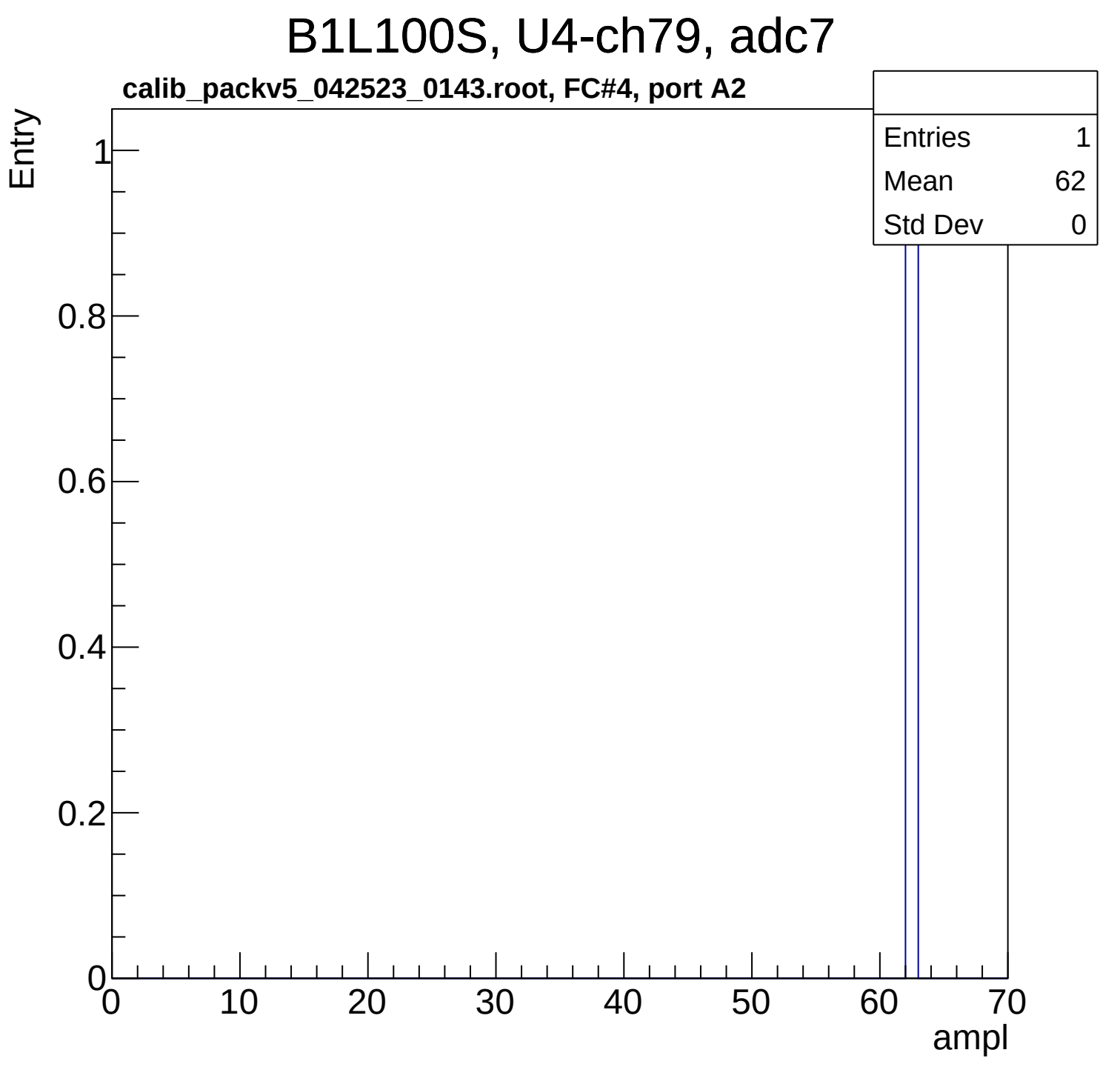

B1L100S, U4-ch79, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 40.45
Std Dev 3.895
Gaus mean : 41.1195
Gaus Width: 4.3701
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

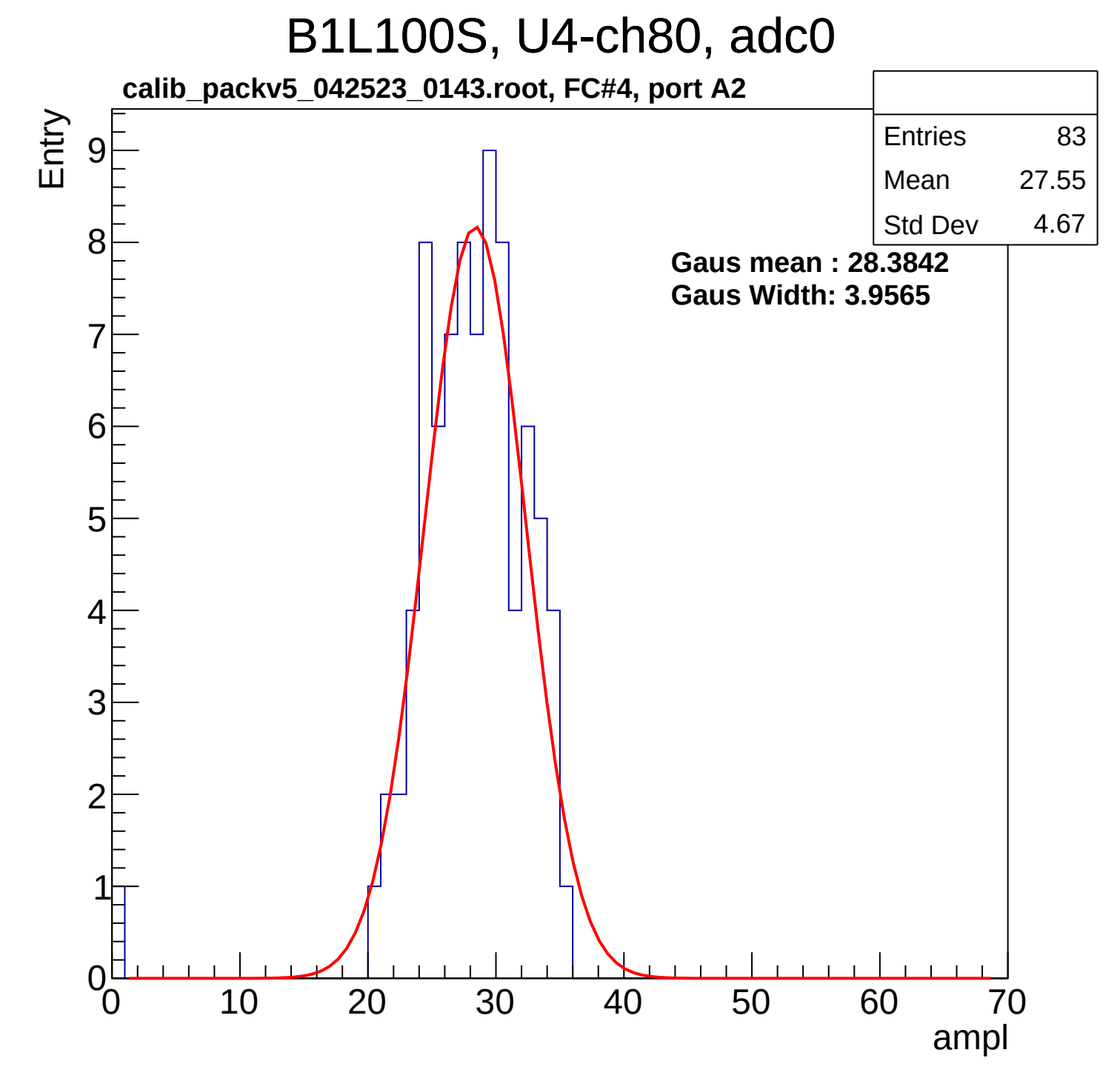

B1L100S, U4-ch79, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 47.65
Std Dev 3.21
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

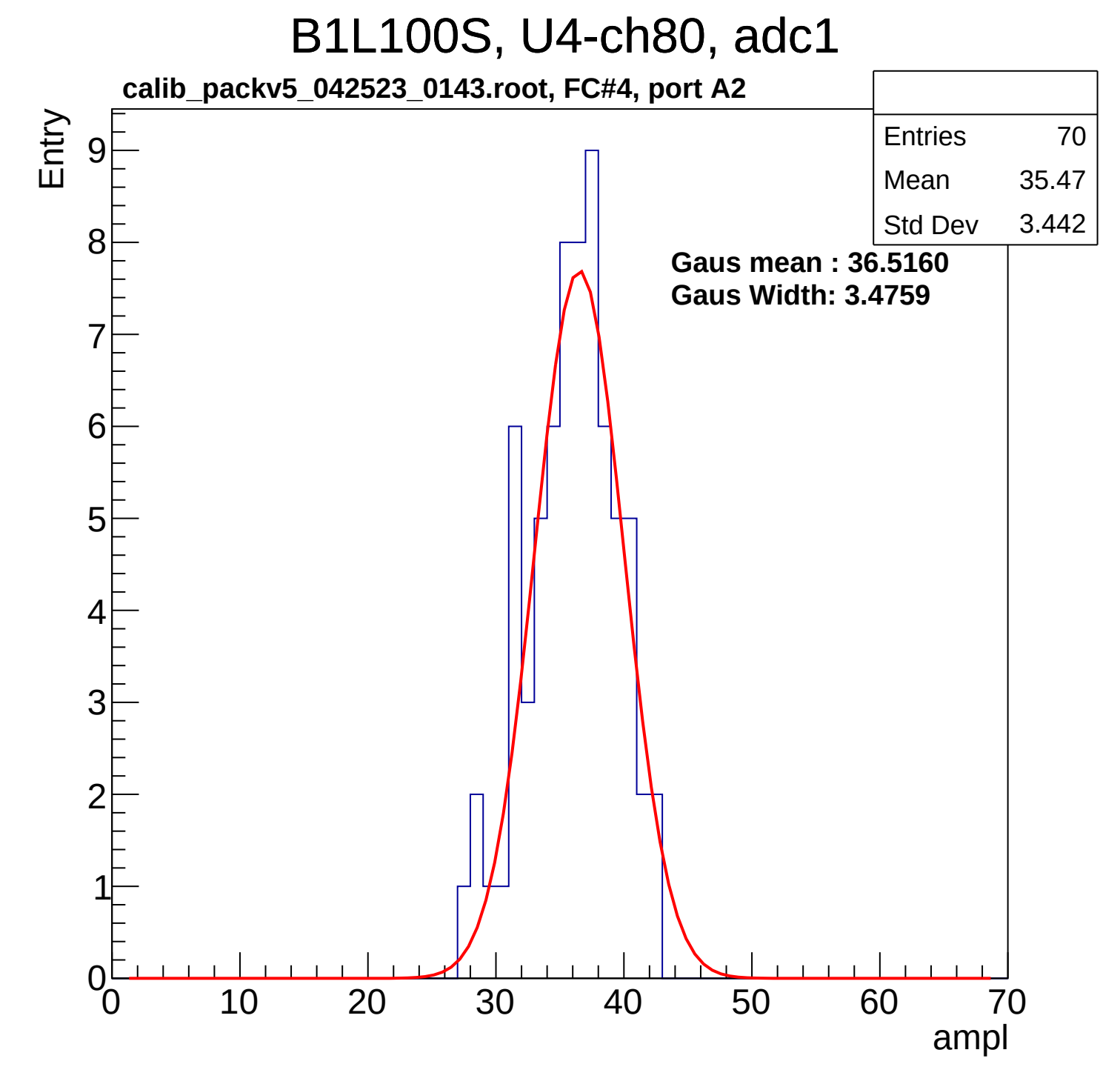

B1L100S, U4-ch79, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 53.77
Std Dev 3.851
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

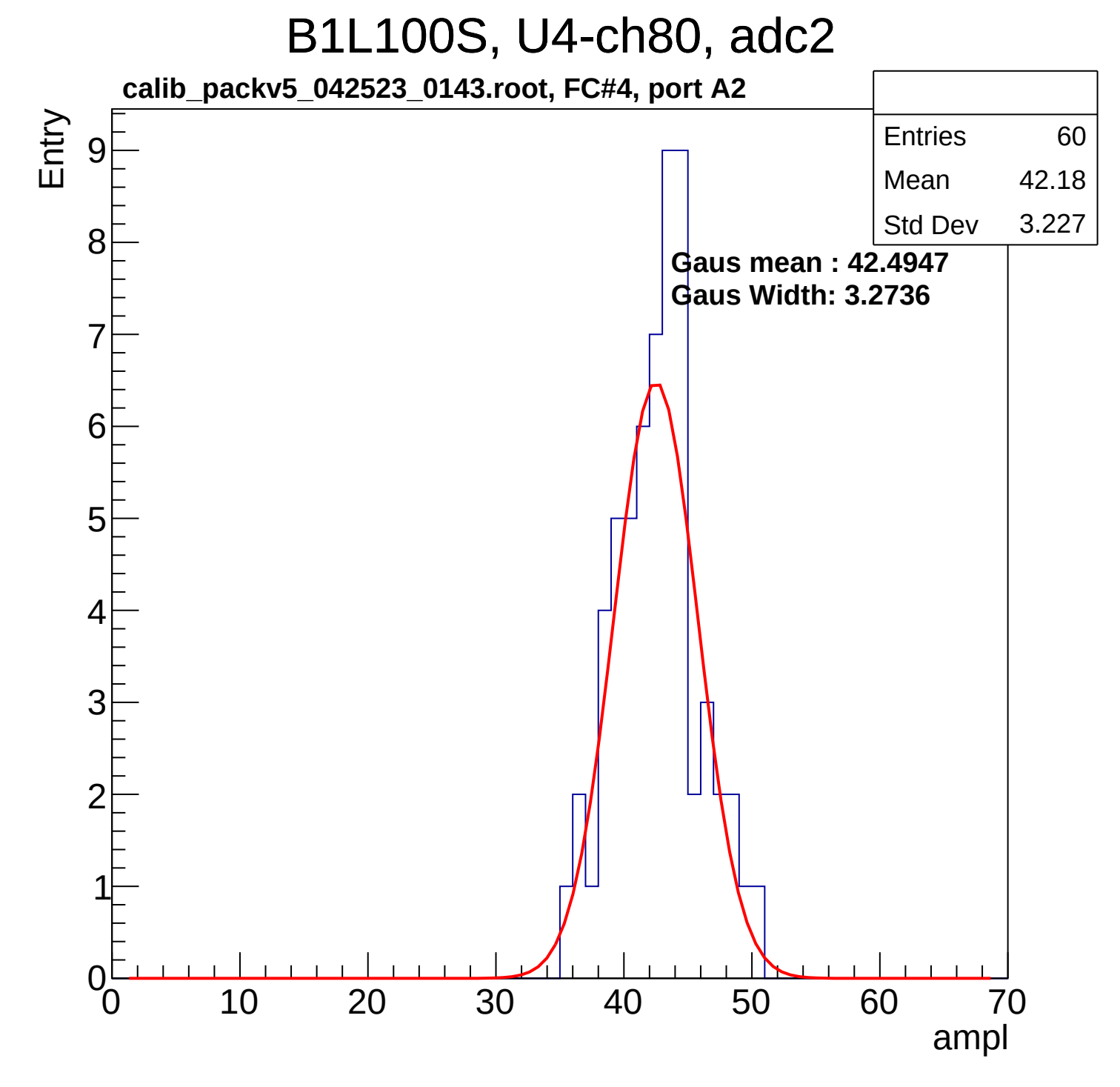

B1L100S, U4-ch79, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 57.61
Std Dev 8.438
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

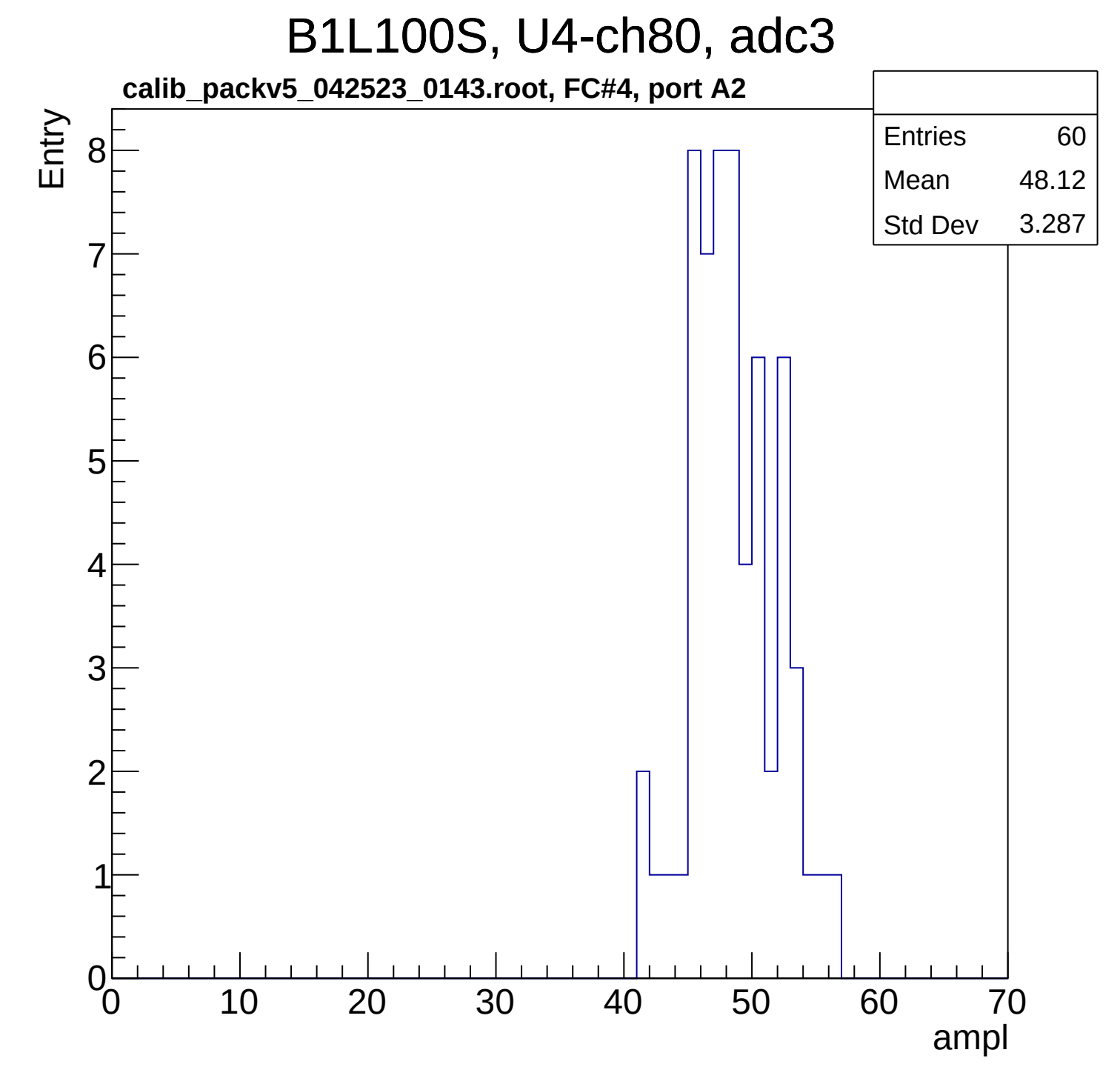

B1L100S, U4-ch79, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 61.82
Std Dev 1.585
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

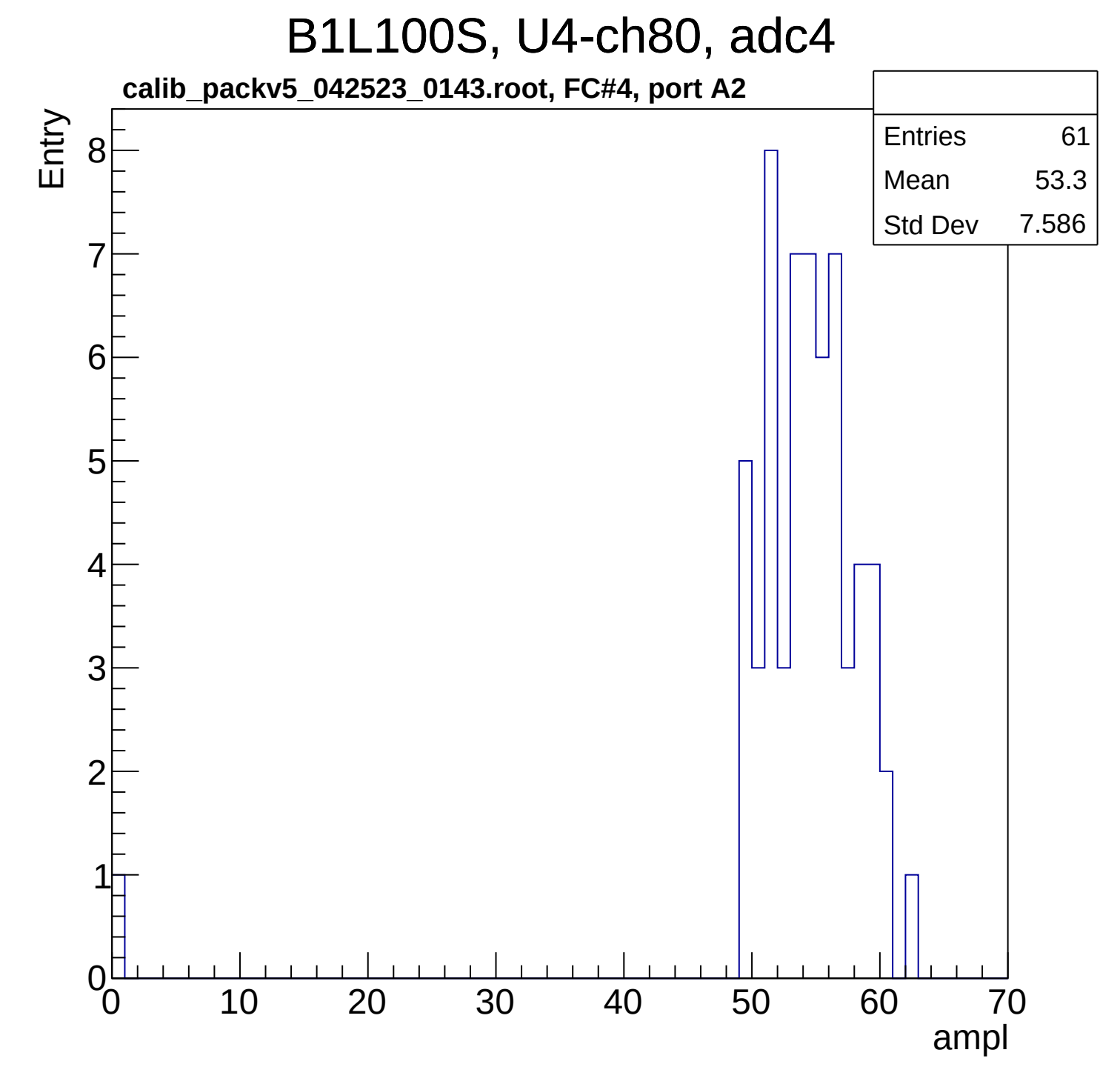

B1L100S, U4-ch79, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

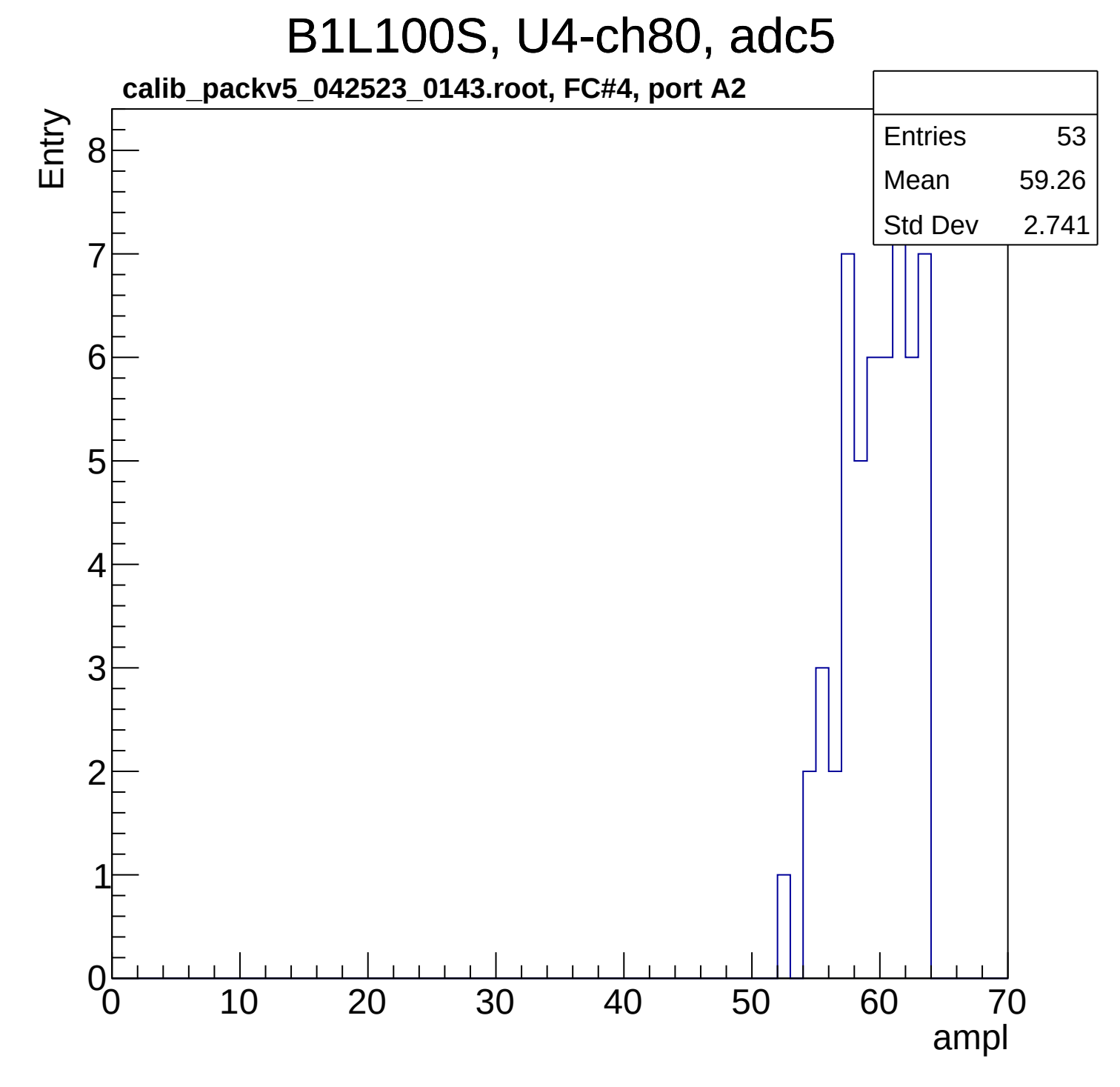

B1L100S, U4-ch80, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 83
Mean 27.55
Std Dev 4.67
Gaus mean : 28.3842
Gaus Width: 3.9565
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

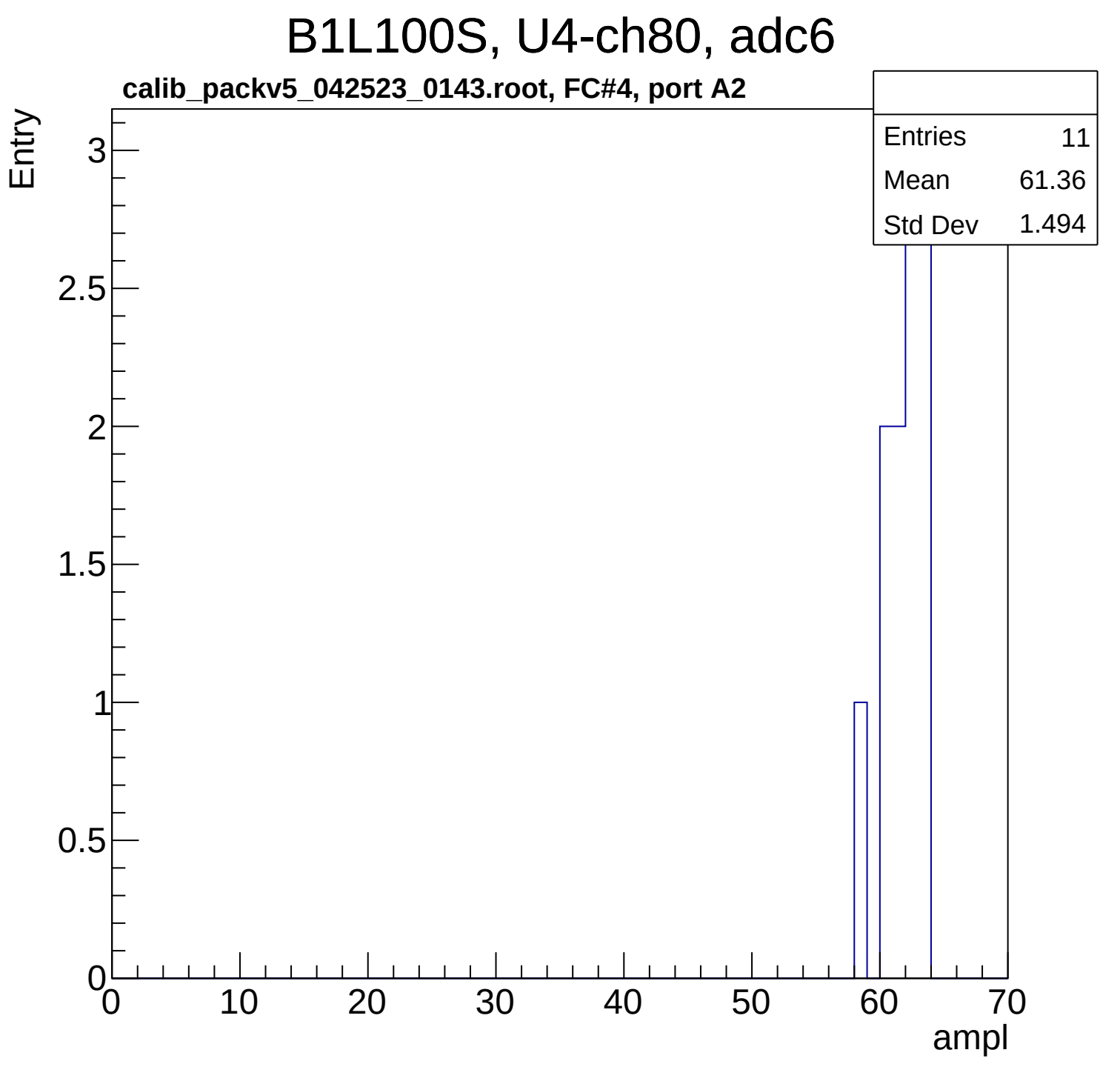

B1L100S, U4-ch80, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 35.47
Std Dev 3.442
Gaus mean : 36.5160
Gaus Width: 3.4759
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

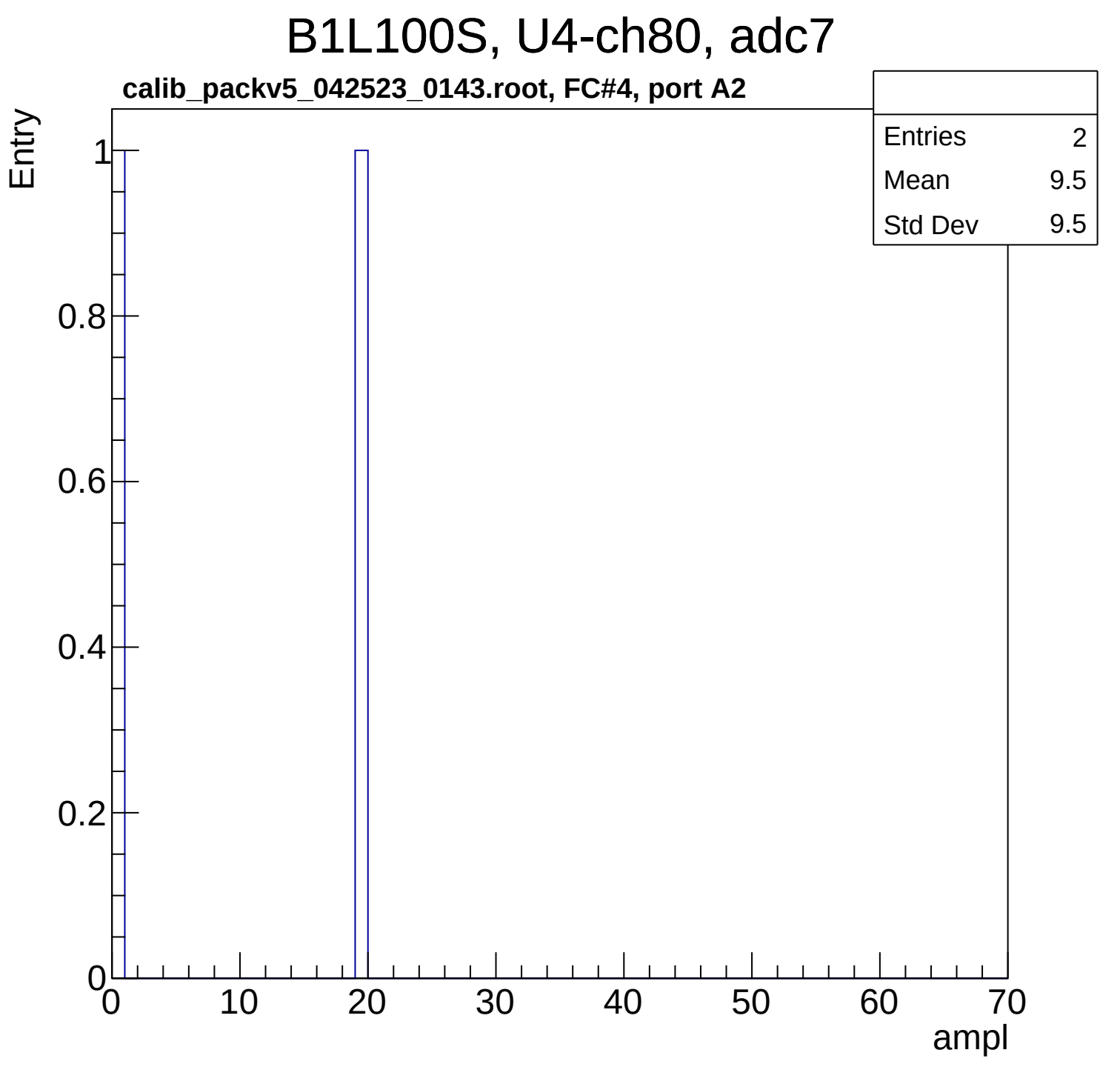

B1L100S, U4-ch80, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 42.18
Std Dev 3.227
Gaus mean : 42.4947
Gaus Width: 3.2736
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

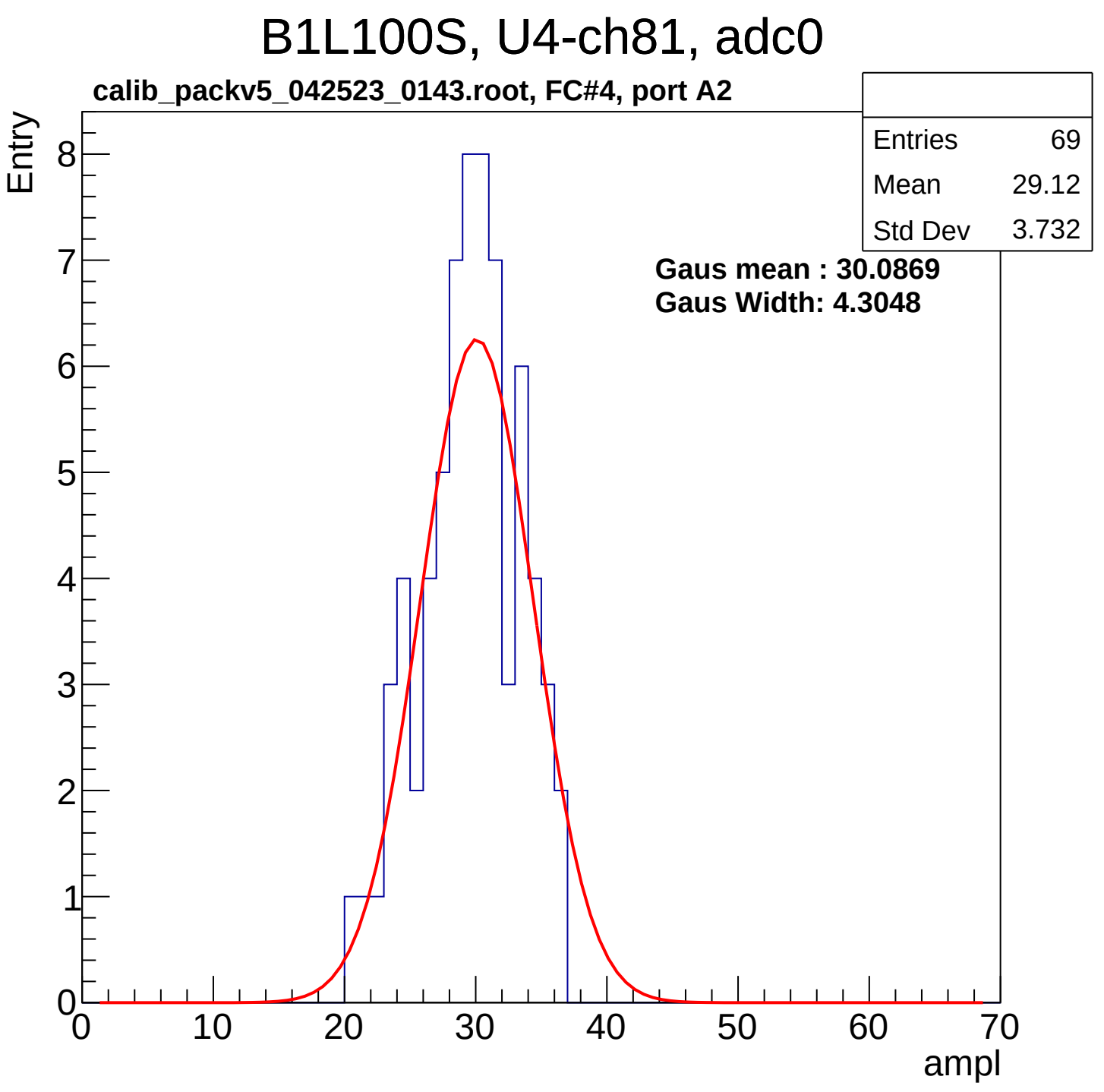

B1L100S, U4-ch80, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 48.12
Std Dev 3.287
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

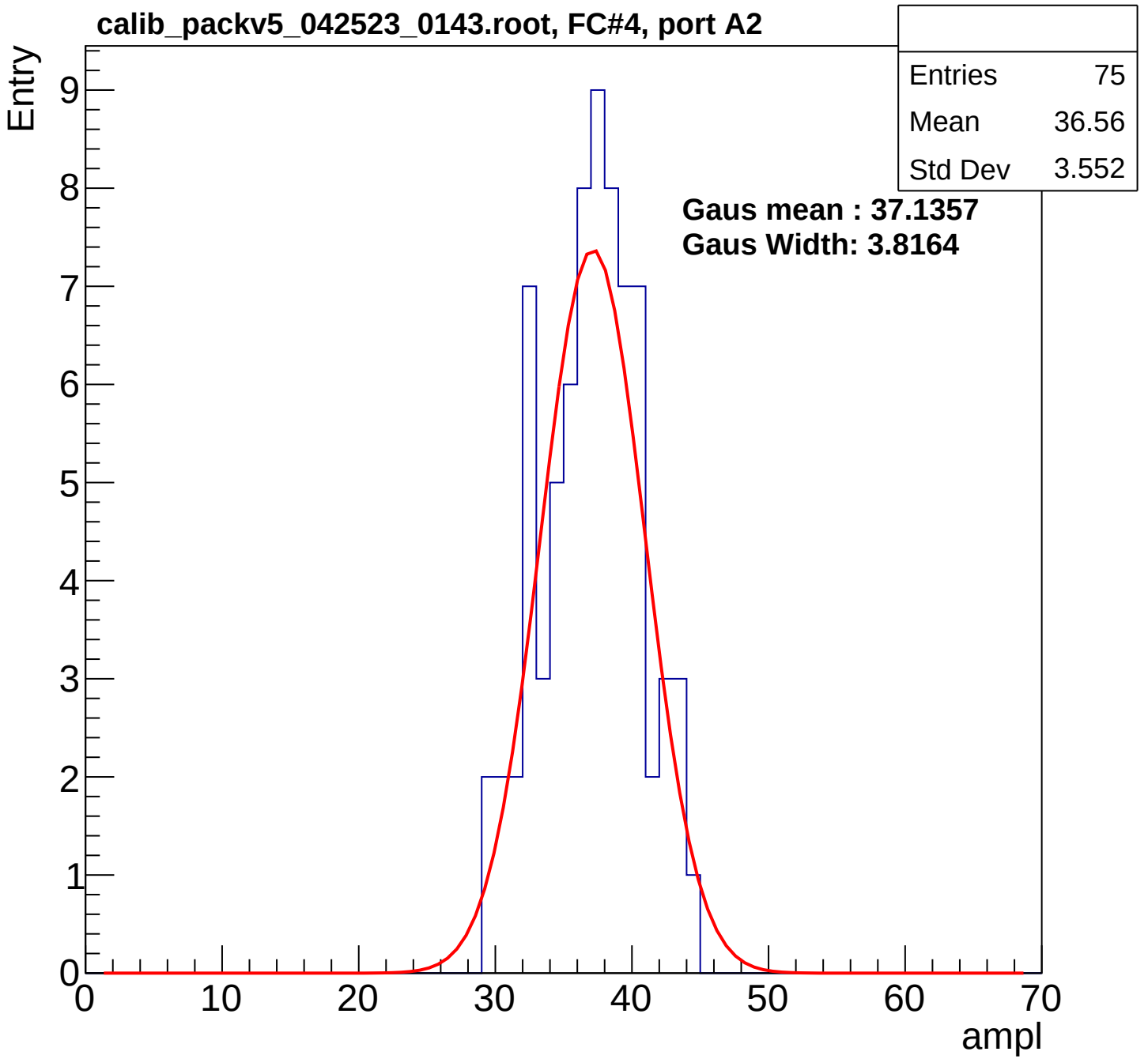

B1L100S, U4-ch80, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 53.3
Std Dev 7.586
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

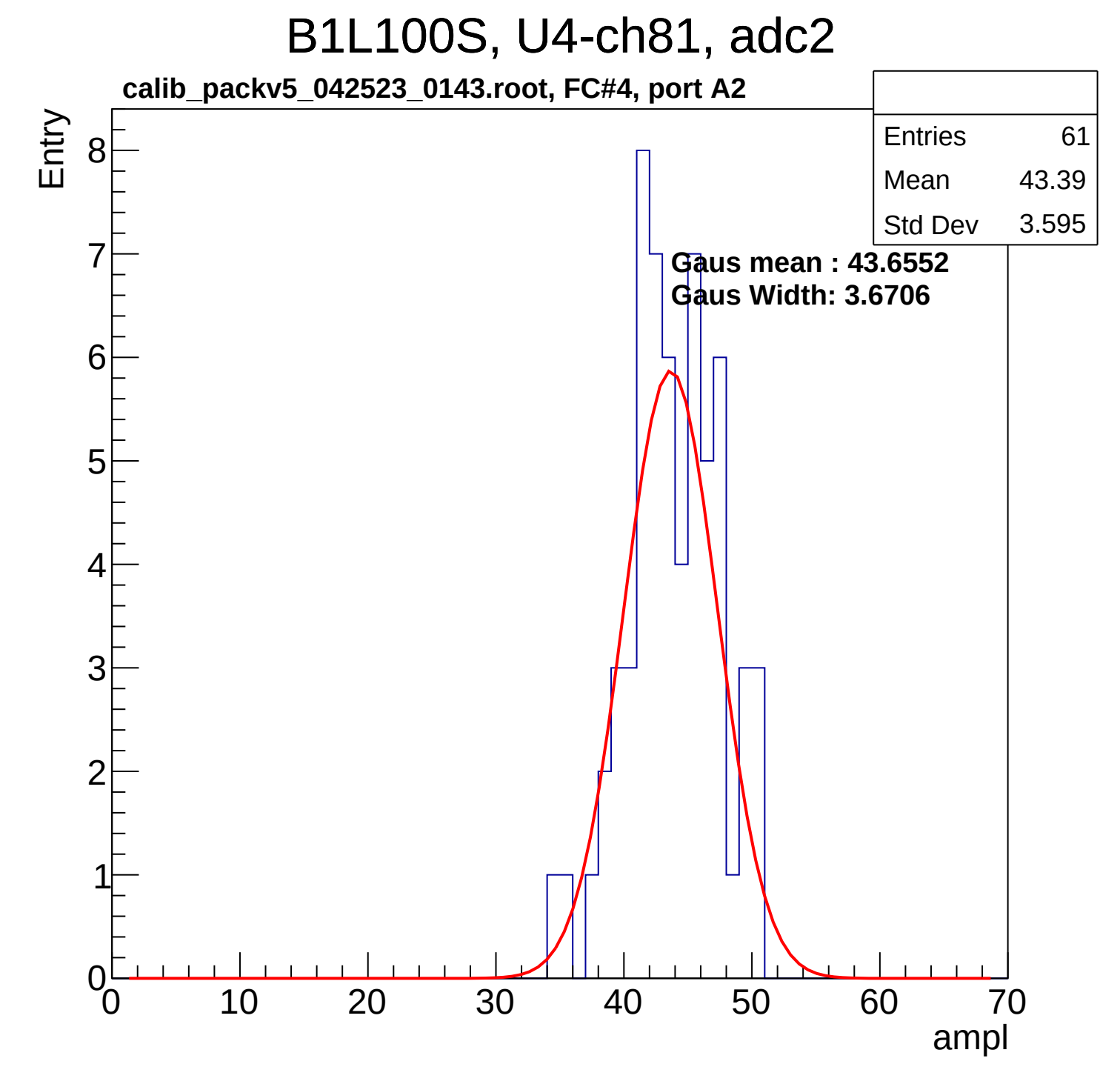

B1L100S, U4-ch80, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 59.26
Std Dev 2.741
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

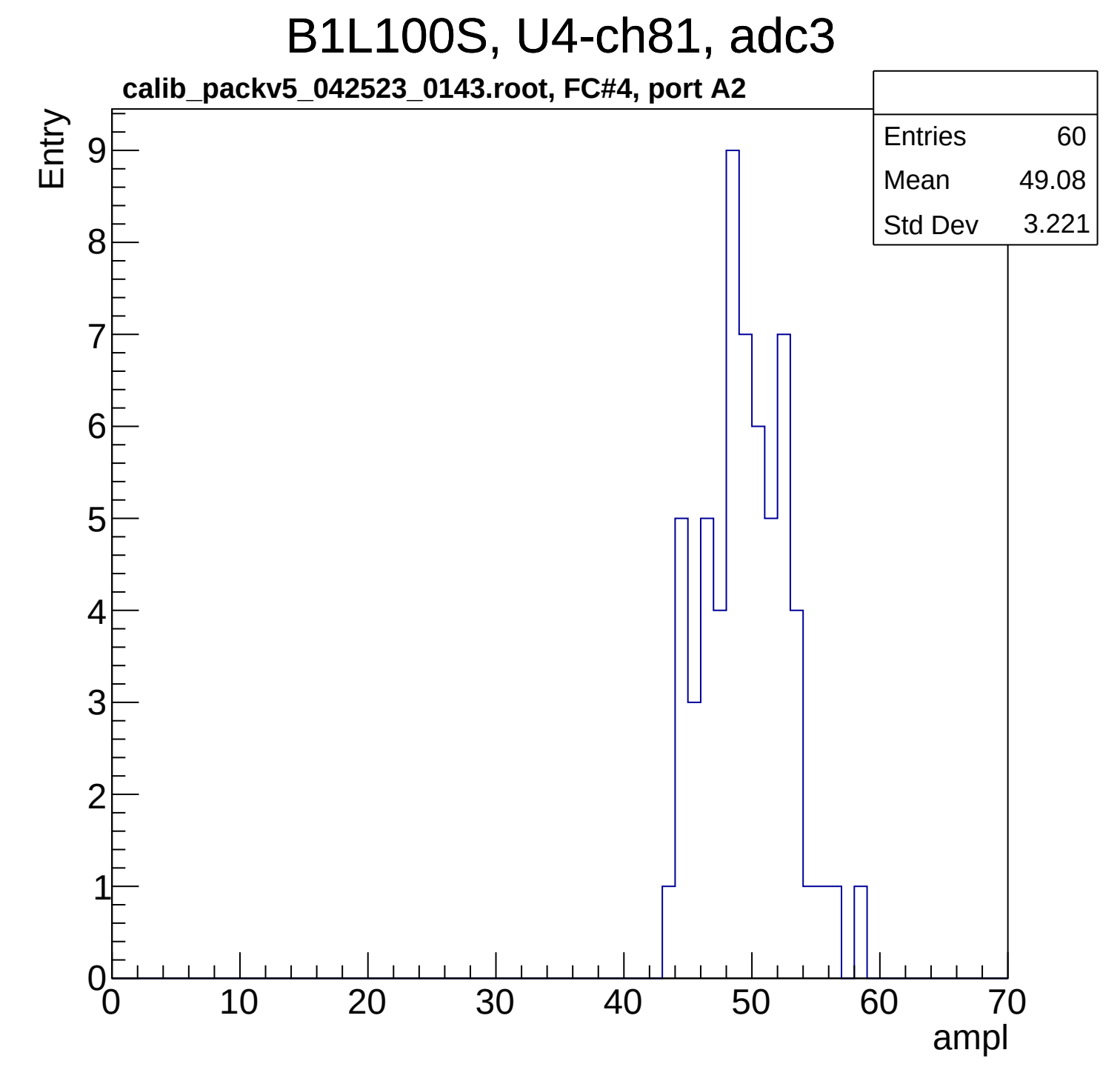

B1L100S, U4-ch80, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 61.36
Std Dev 1.494
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

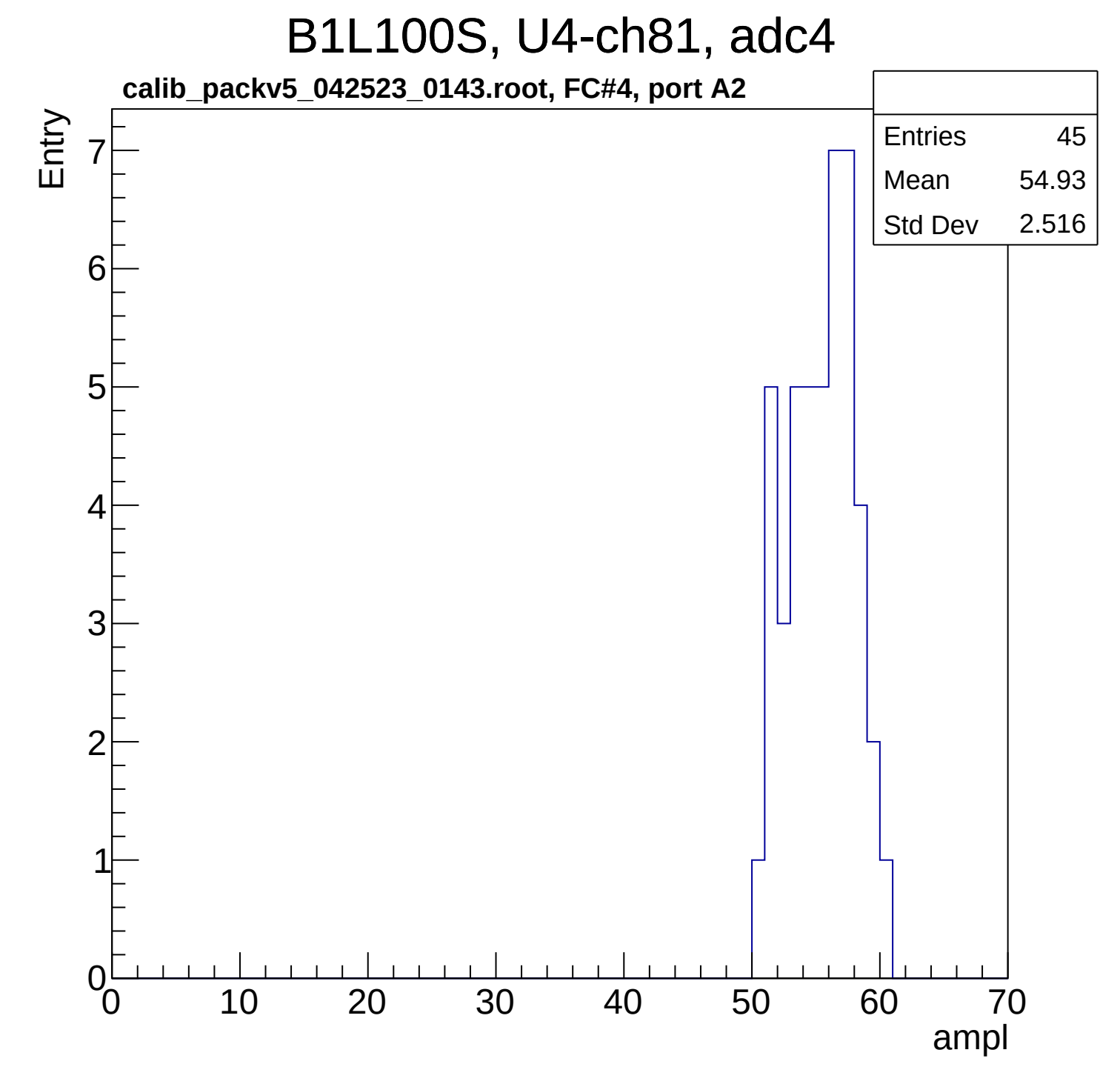

B1L100S, U4-ch80, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 9.5
Std Dev 9.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

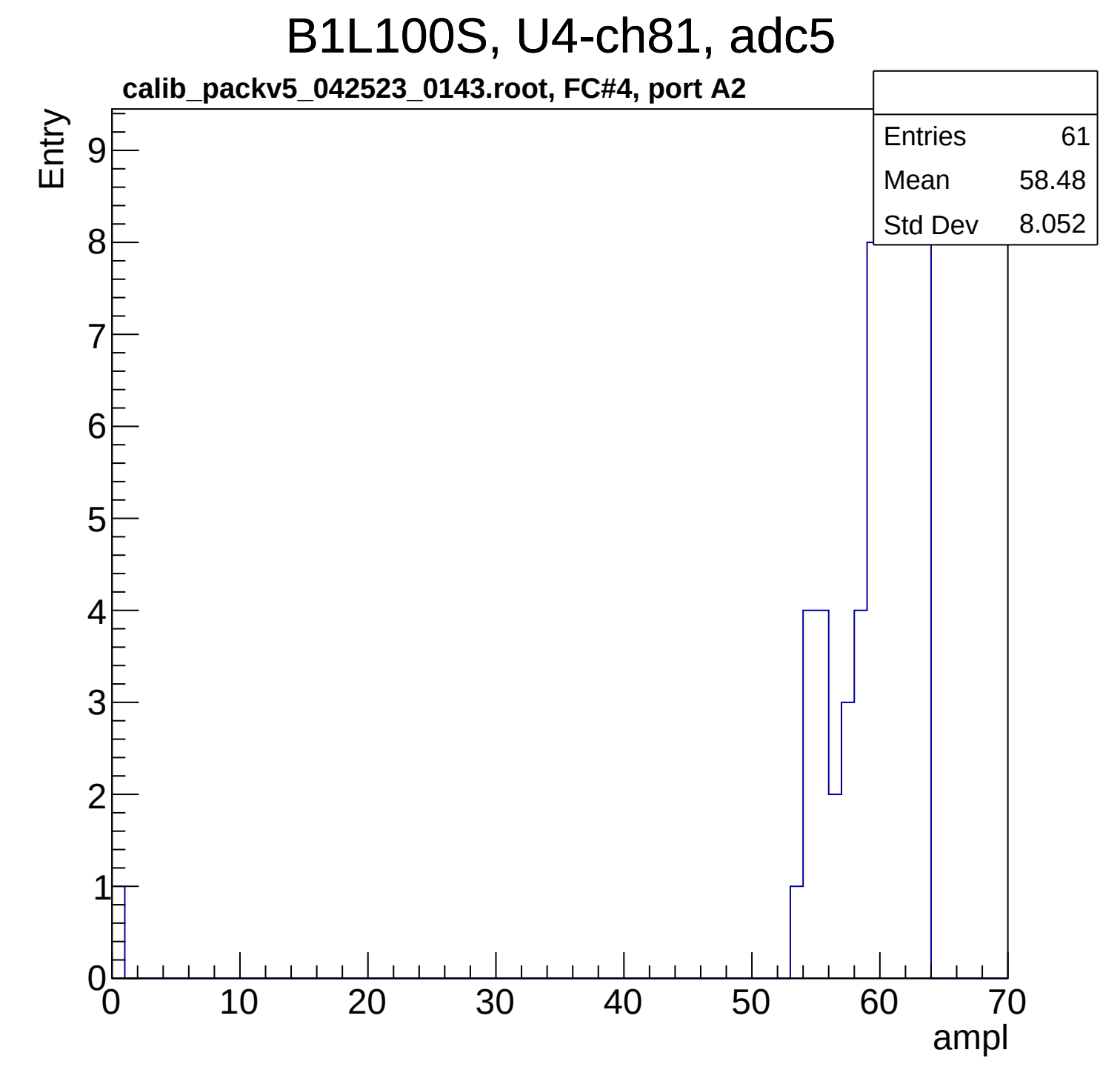

B1L100S, U4-ch81, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 29.12
Std Dev 3.732
Gaus mean : 30.0869
Gaus Width: 4.3048
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

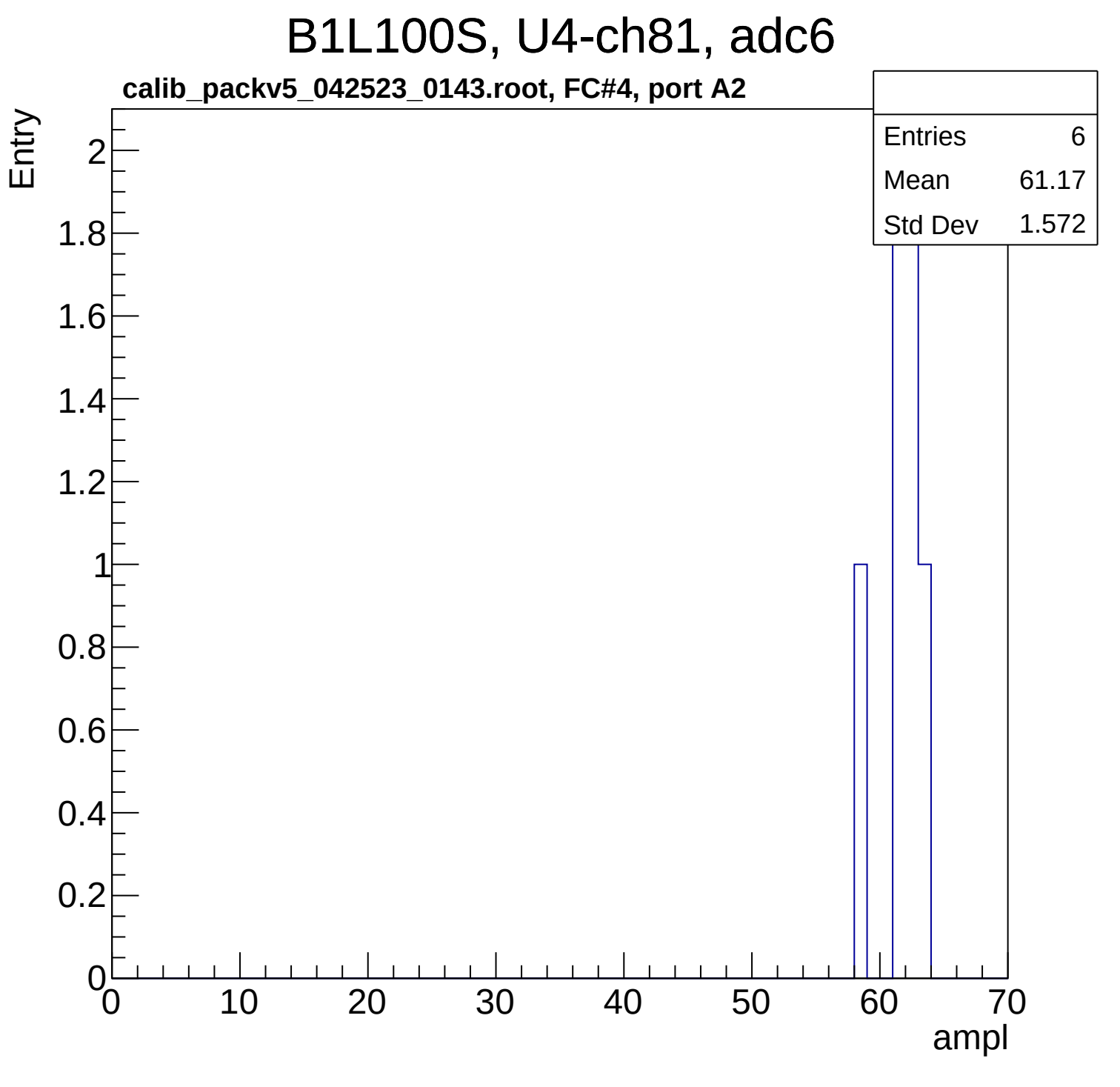

B1L100S, U4-ch81, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 36.56
Std Dev 3.552
Gaus mean : 37.1357
Gaus Width: 3.8164
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

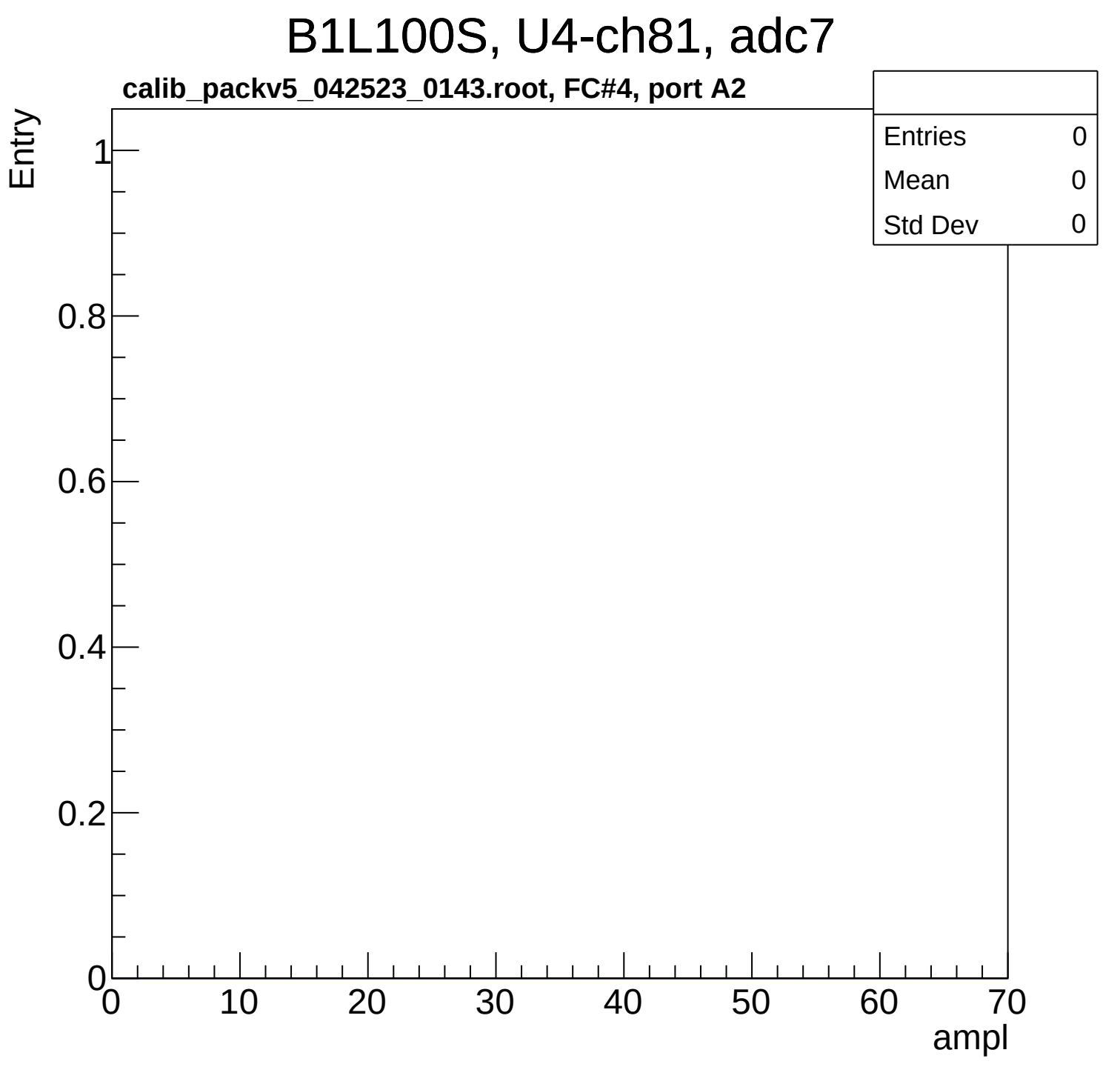

B1L100S, U4-ch81, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 43.39
Std Dev 3.595
Gaus mean : 43.6552
Gaus Width: 3.6706
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

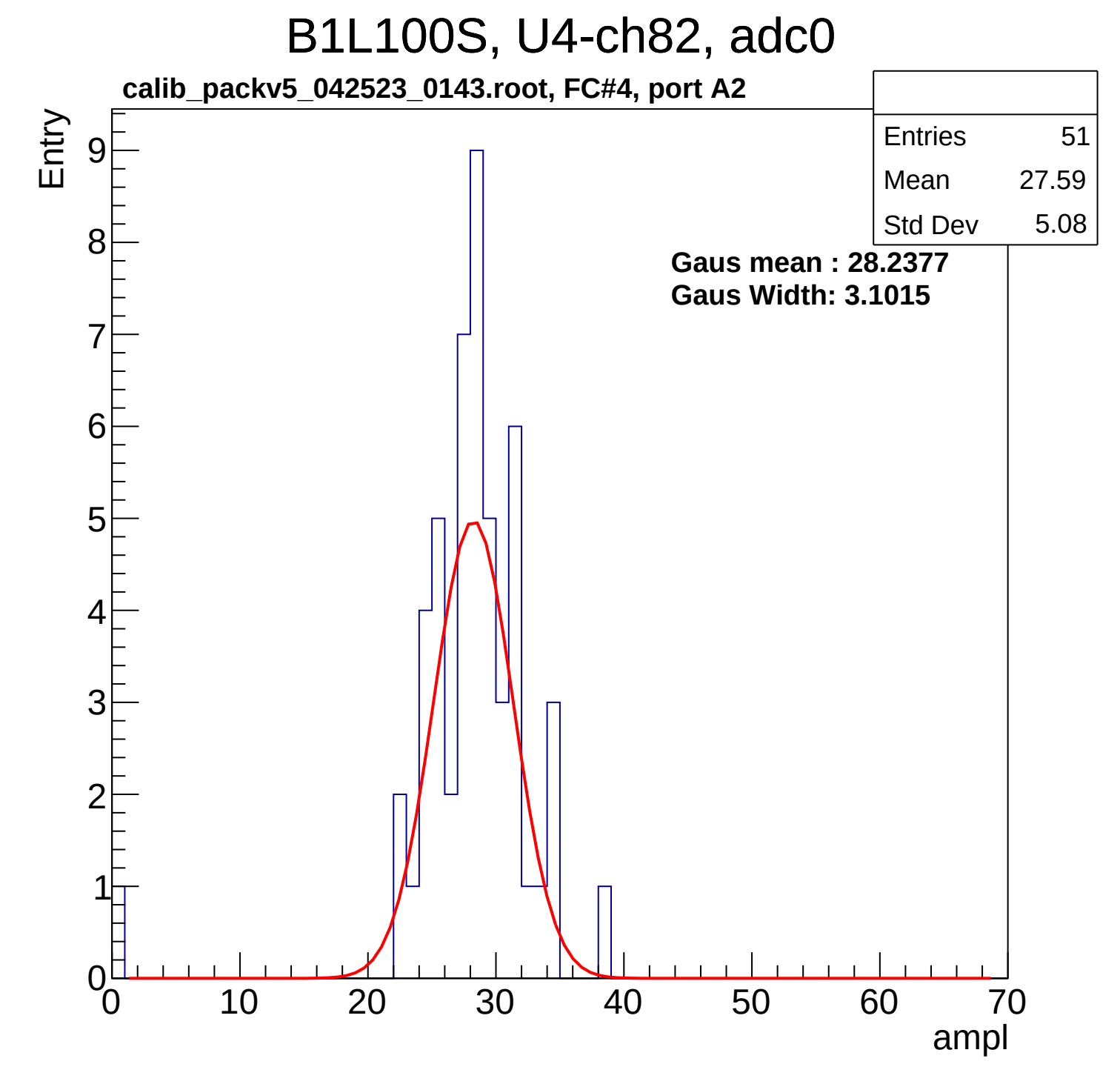

B1L100S, U4-ch81, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 49.08
Std Dev 3.221
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

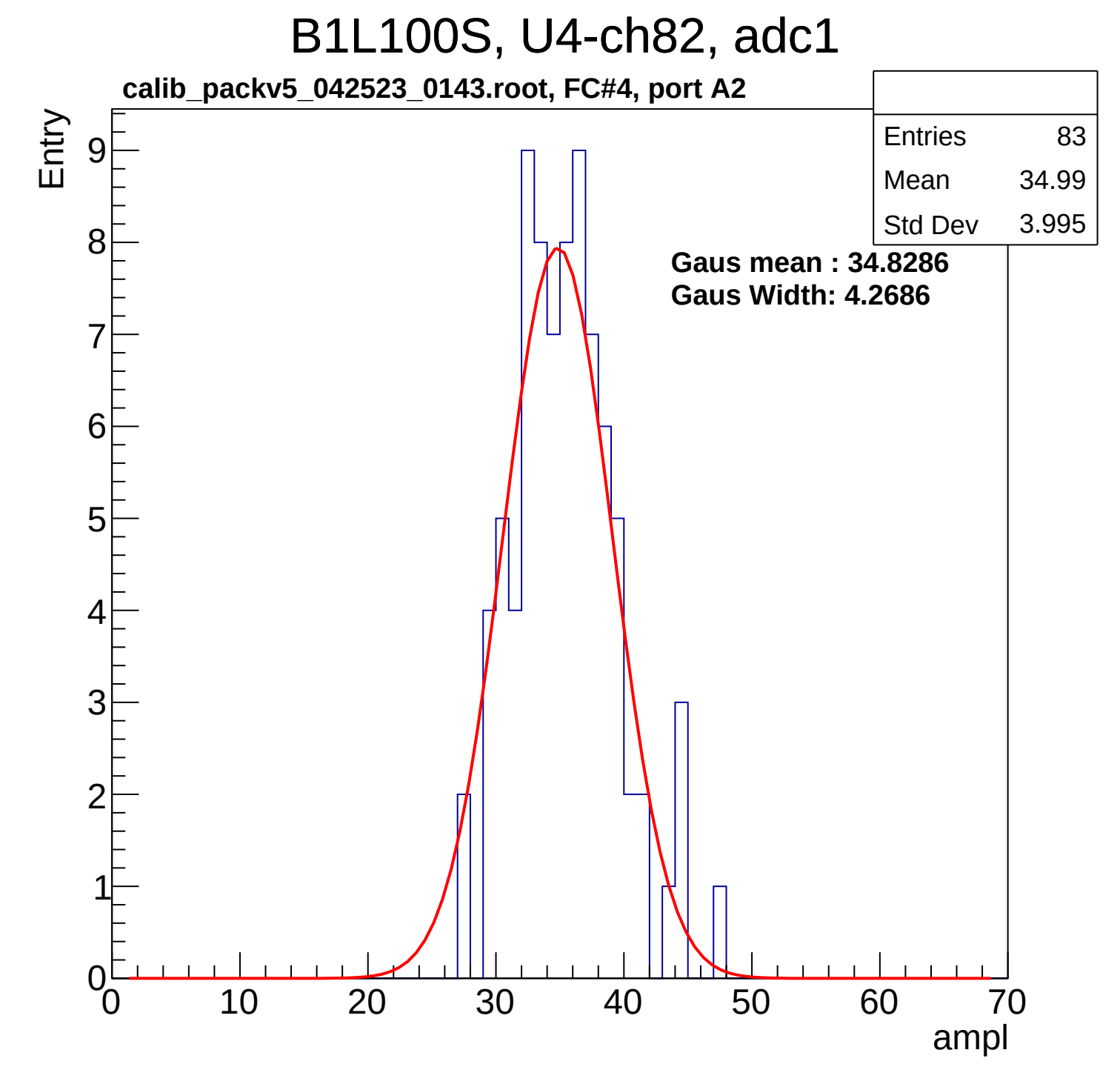

B1L100S, U4-ch81, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 45
Mean 54.93
Std Dev 2.516
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

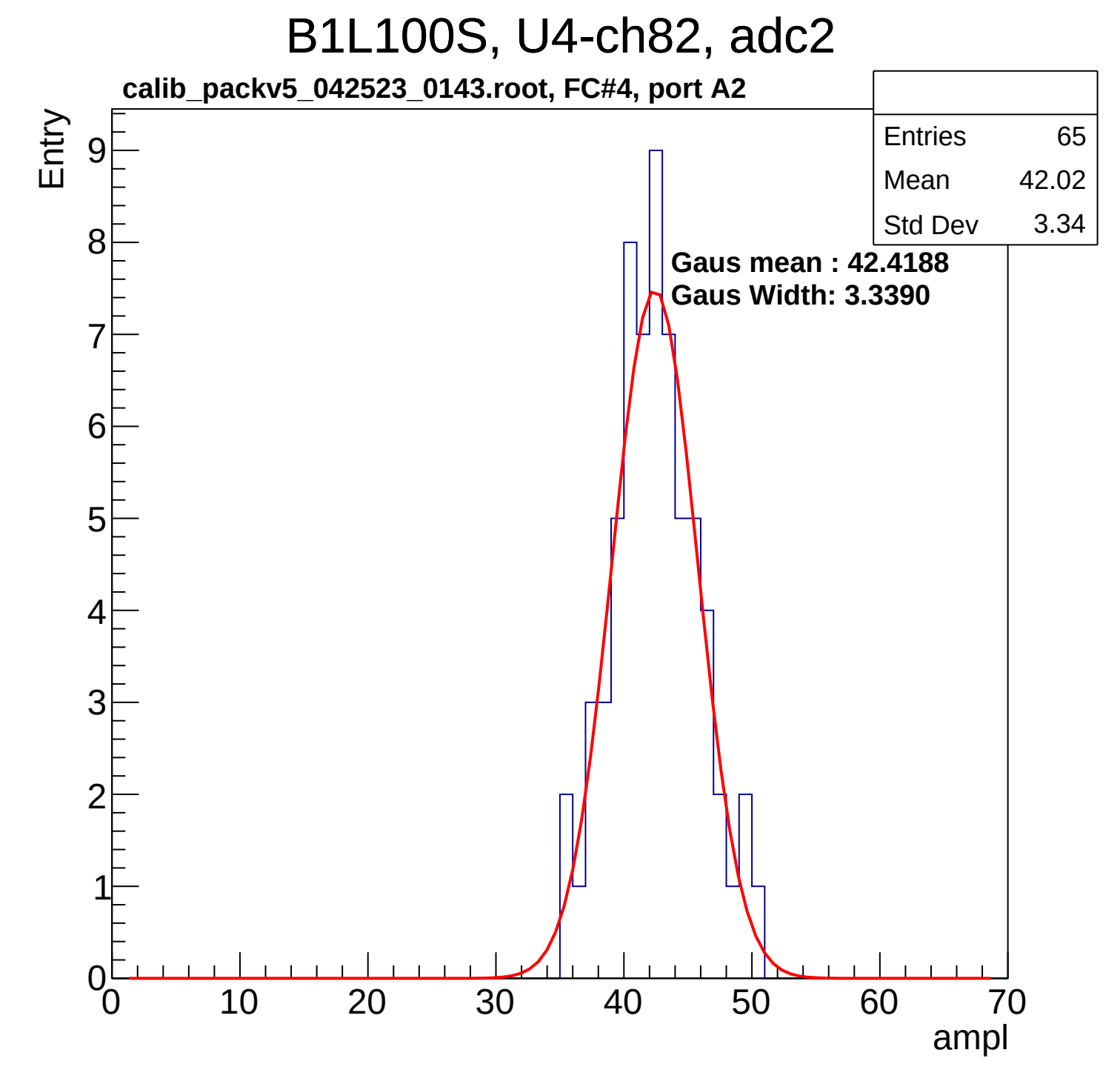

B1L100S, U4-ch81, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 58.48
Std Dev 8.052
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

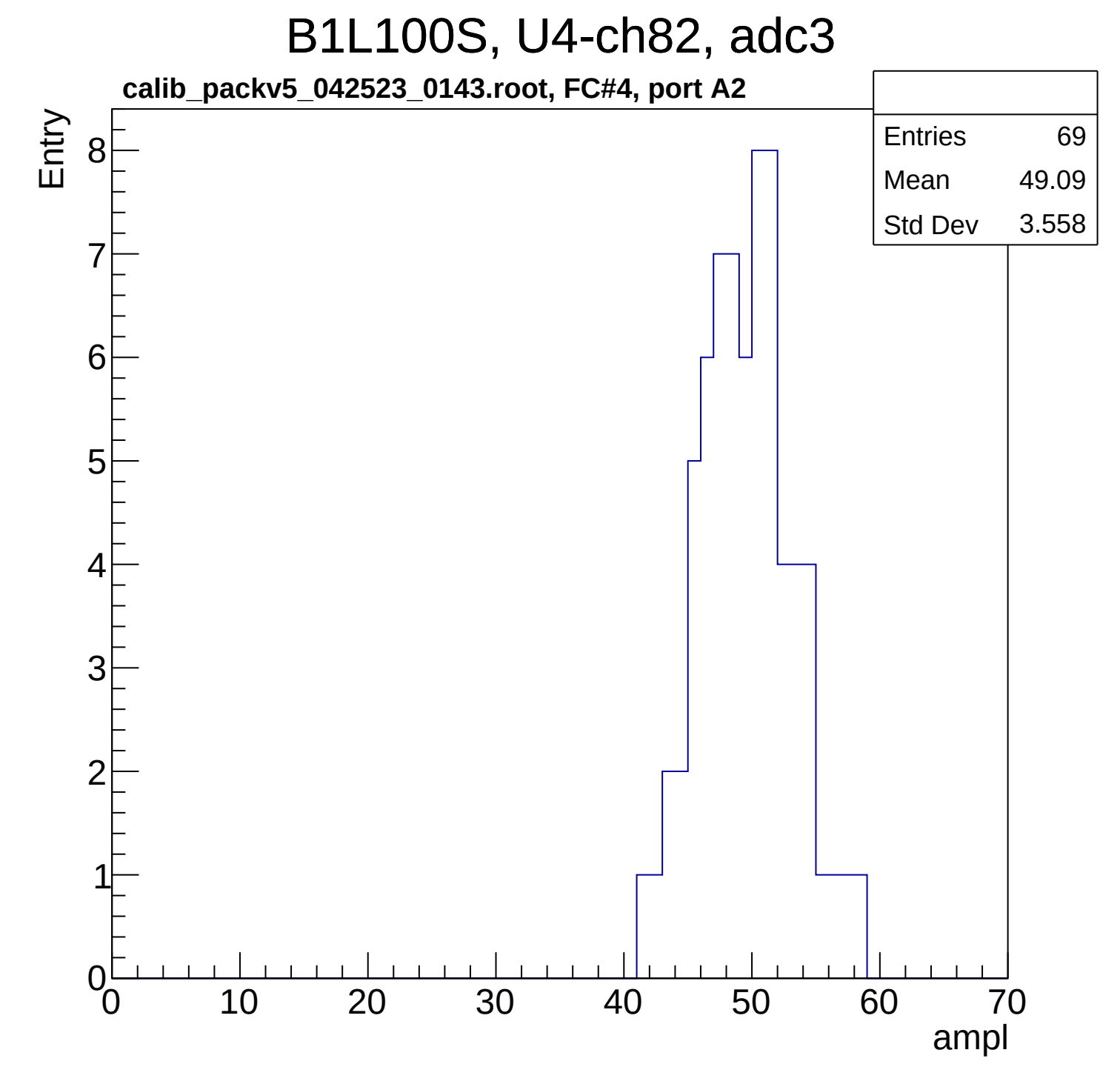

B1L100S, U4-ch81, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 61.17
Std Dev 1.572
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

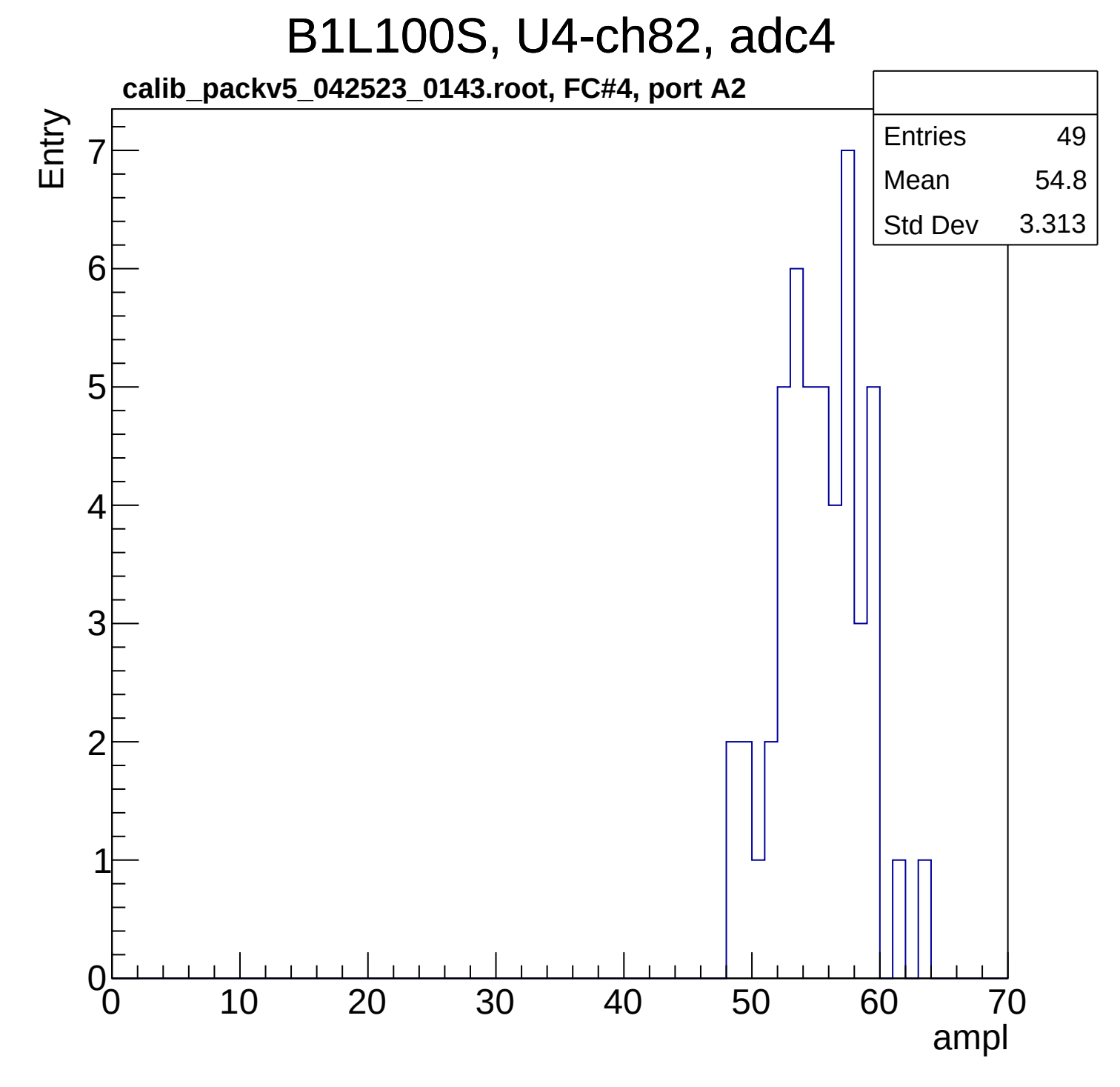

B1L100S, U4-ch81, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

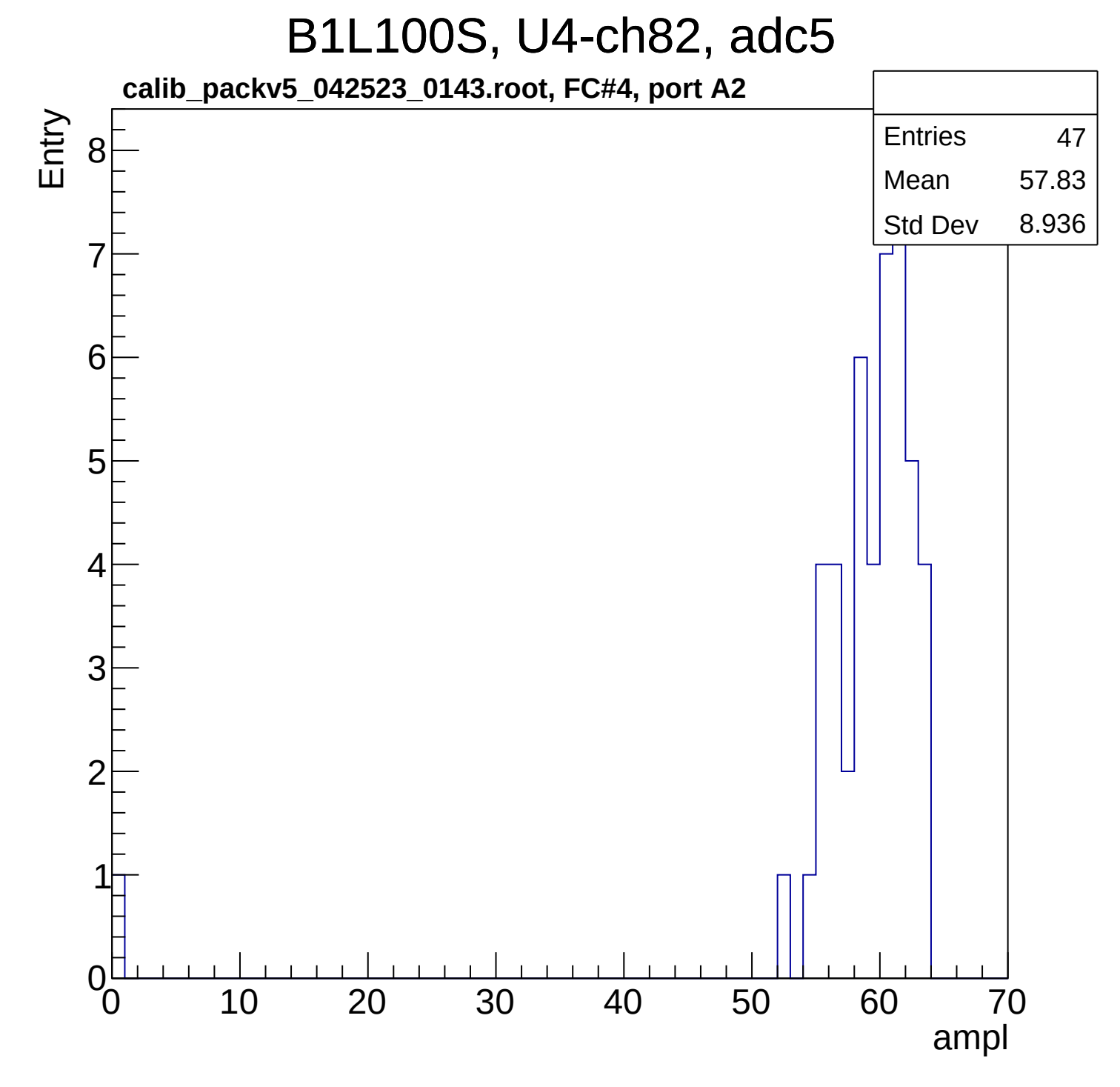

B1L100S, U4-ch82, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 27.59
Std Dev 5.08
Gaus mean : 28.2377
Gaus Width: 3.1015
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

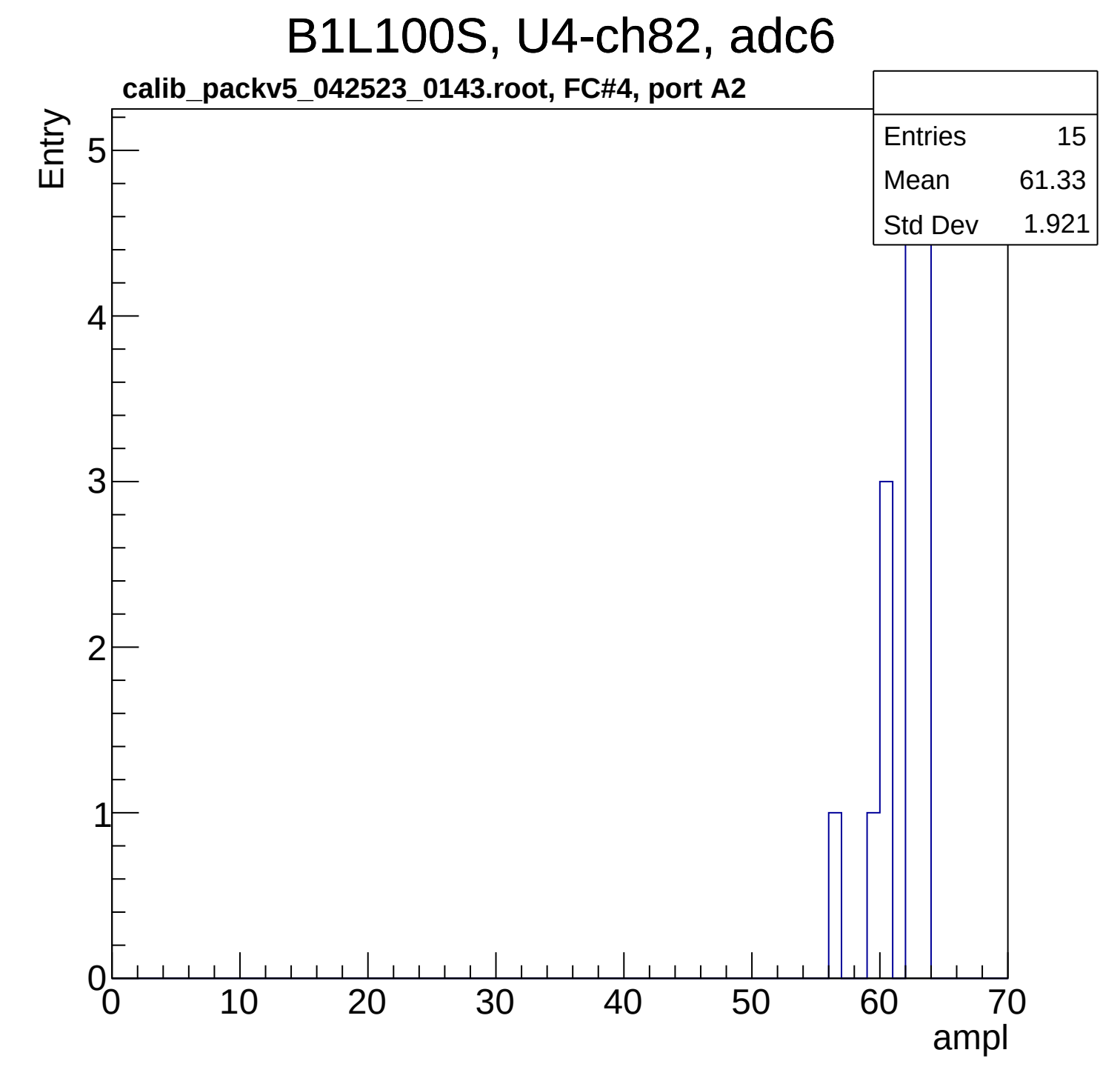

B1L100S, U4-ch82, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 83
Mean 34.99
Std Dev 3.995
Gaus mean : 34.8286
Gaus Width: 4.2686
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

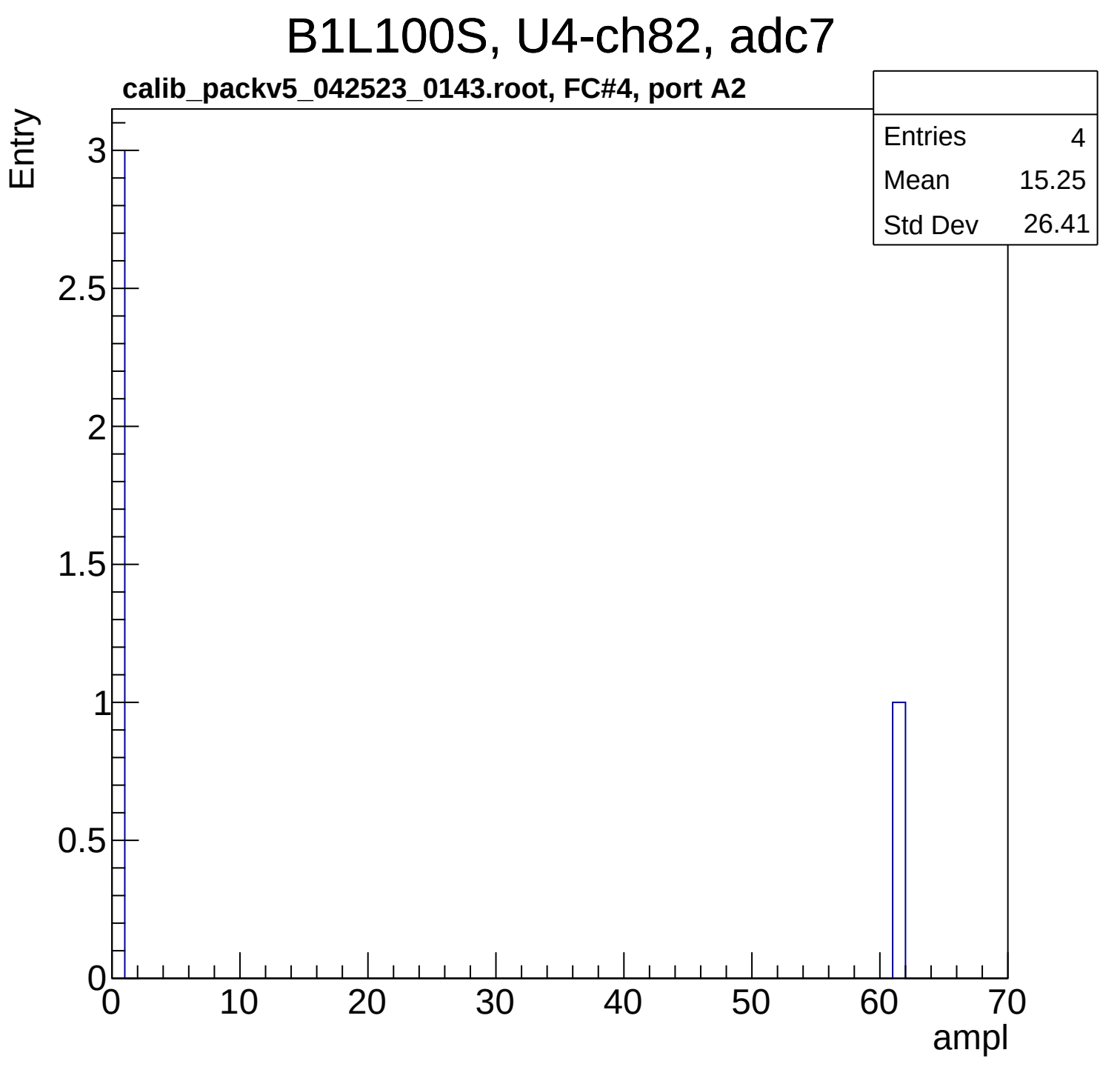

B1L100S, U4-ch82, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 42.02
Std Dev 3.34
Gaus mean : 42.4188
Gaus Width: 3.3390
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

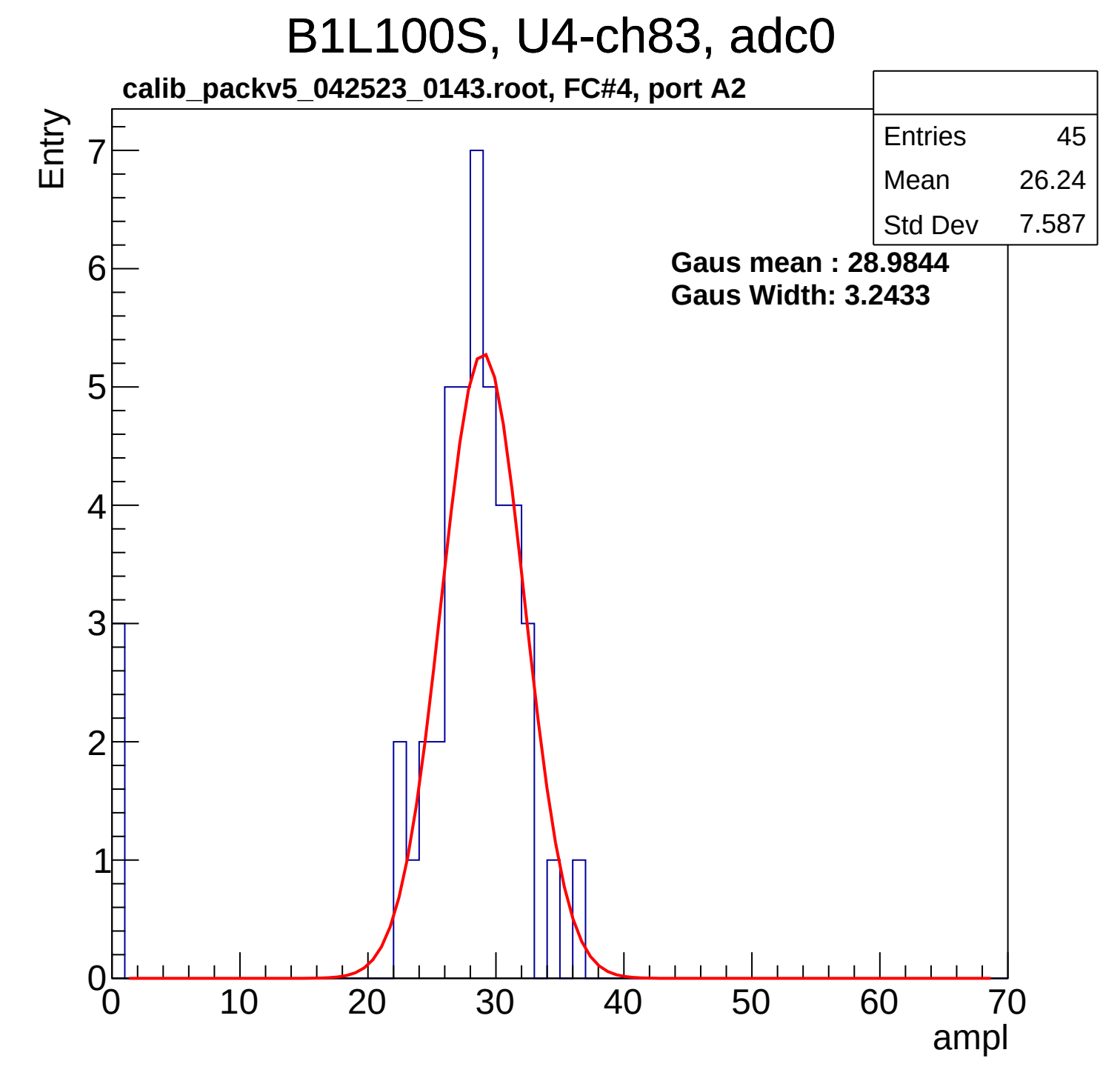

B1L100S, U4-ch82, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 49.09
Std Dev 3.558
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

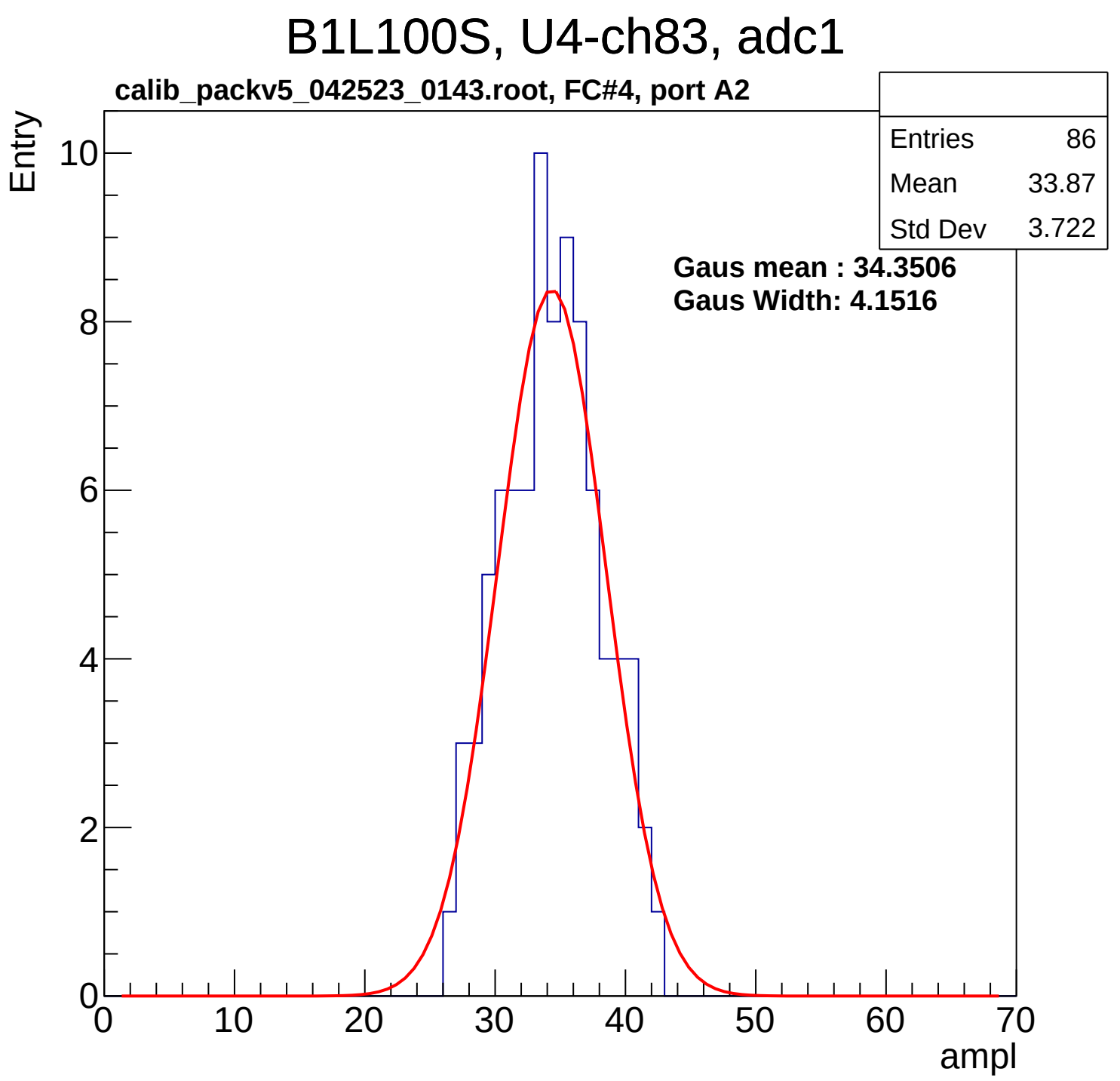

B1L100S, U4-ch82, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 54.8
Std Dev 3.313
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

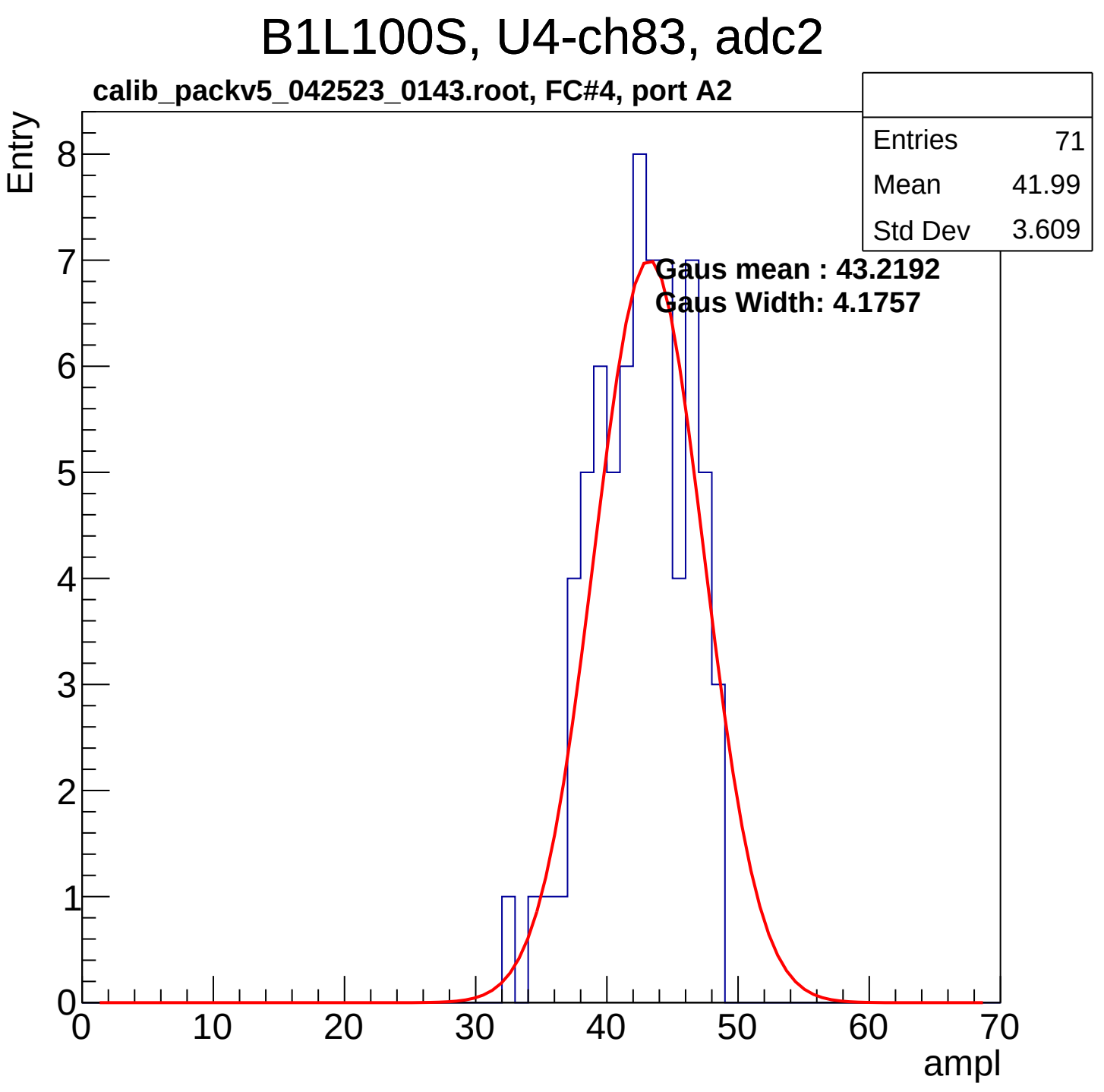

B1L100S, U4-ch82, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 57.83
Std Dev 8.936
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

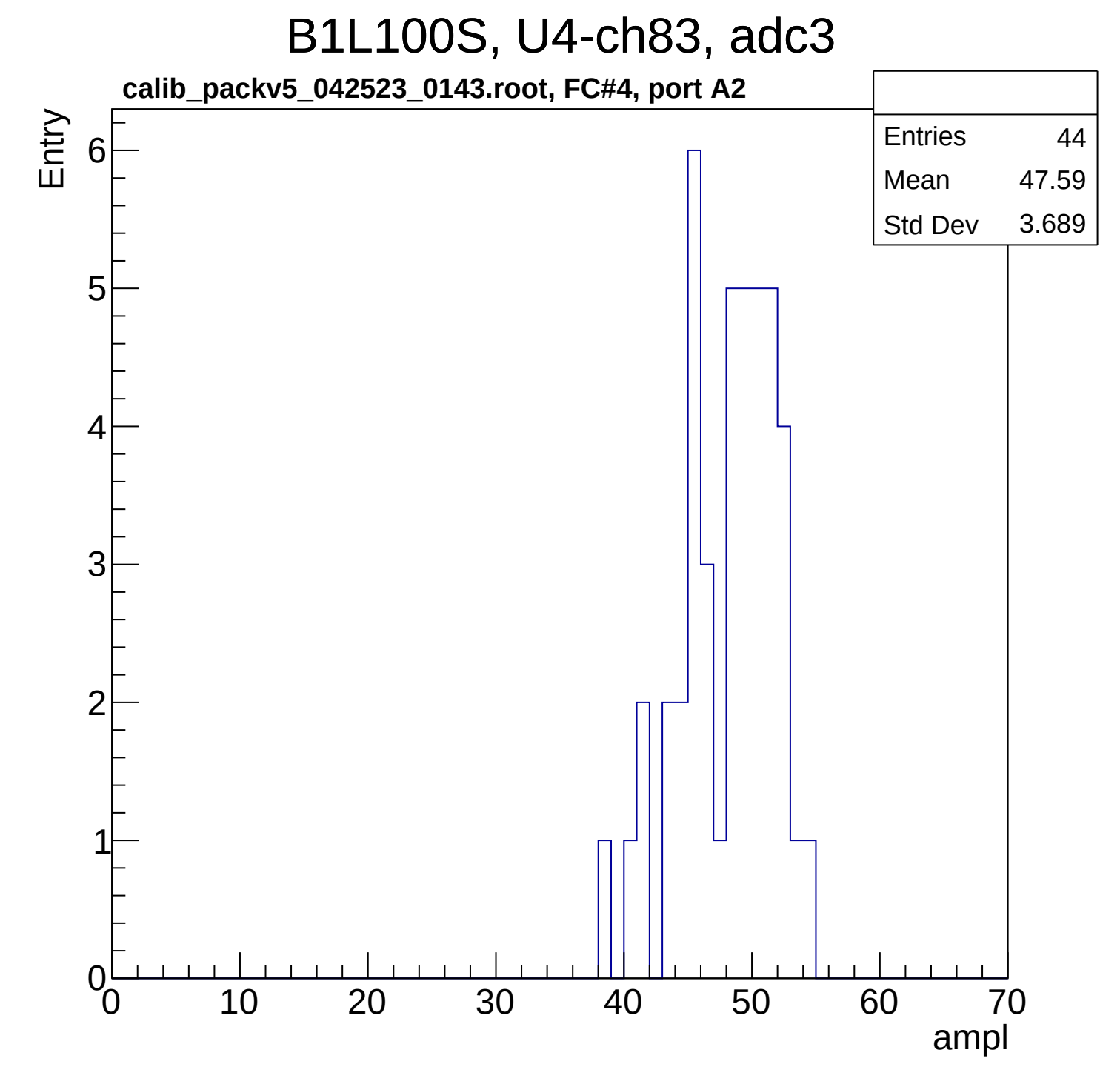

B1L100S, U4-ch82, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 15
Mean 61.33
Std Dev 1.921
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

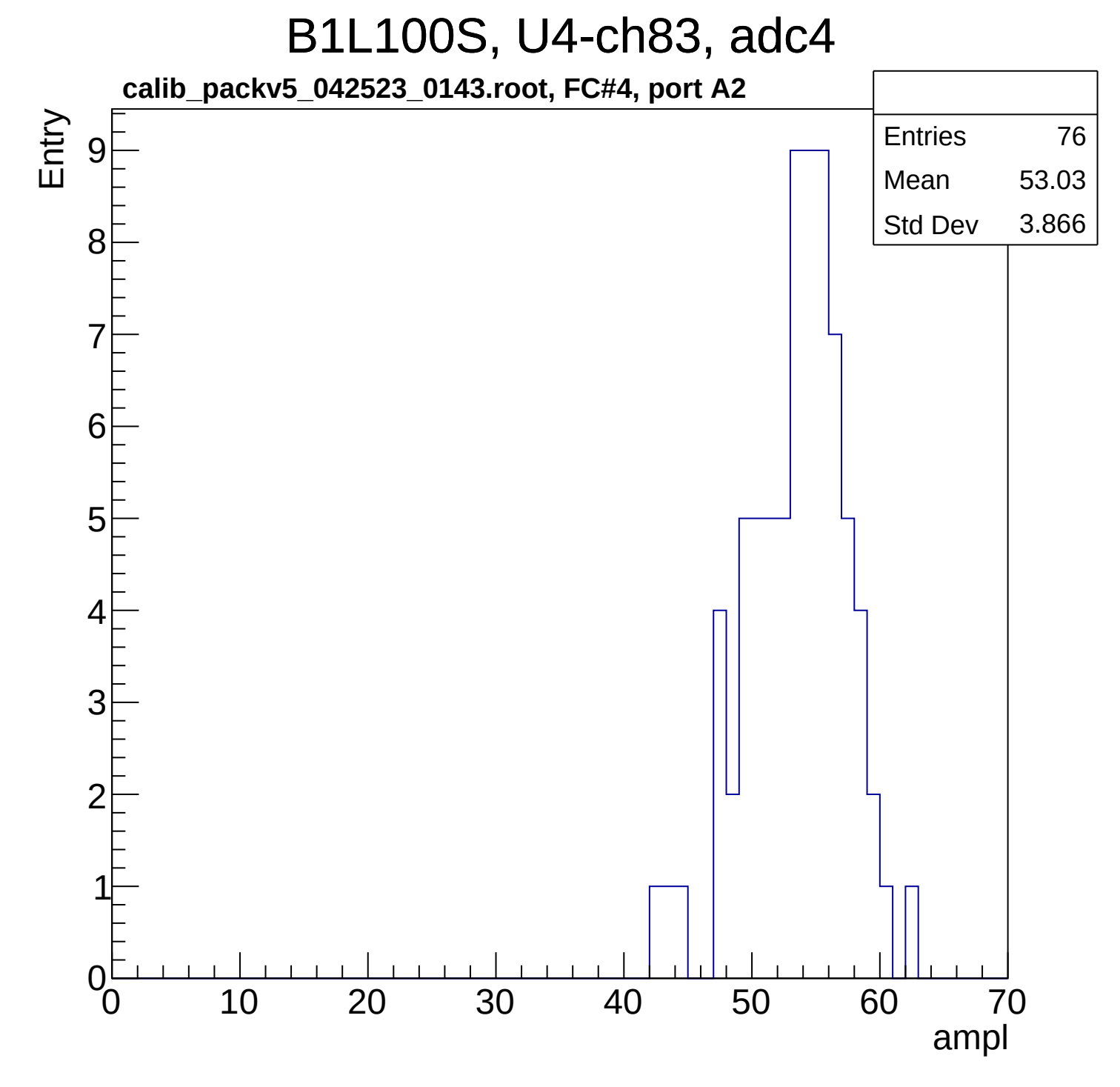

B1L100S, U4-ch82, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 15.25
Std Dev 26.41
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

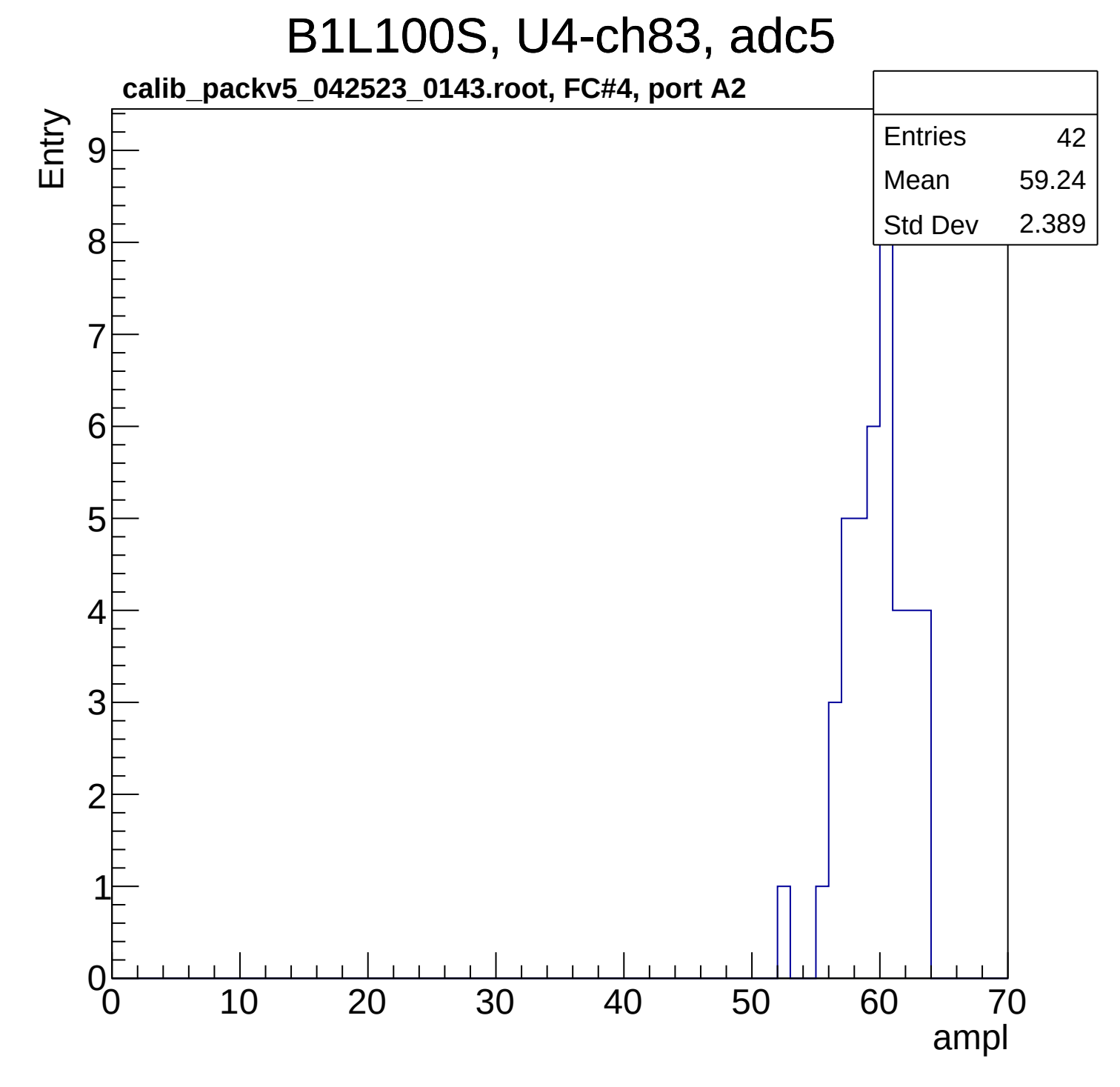

B1L100S, U4-ch83, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 45
Mean 26.24
Std Dev 7.587
Gaus mean : 28.9844
Gaus Width: 3.2433
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

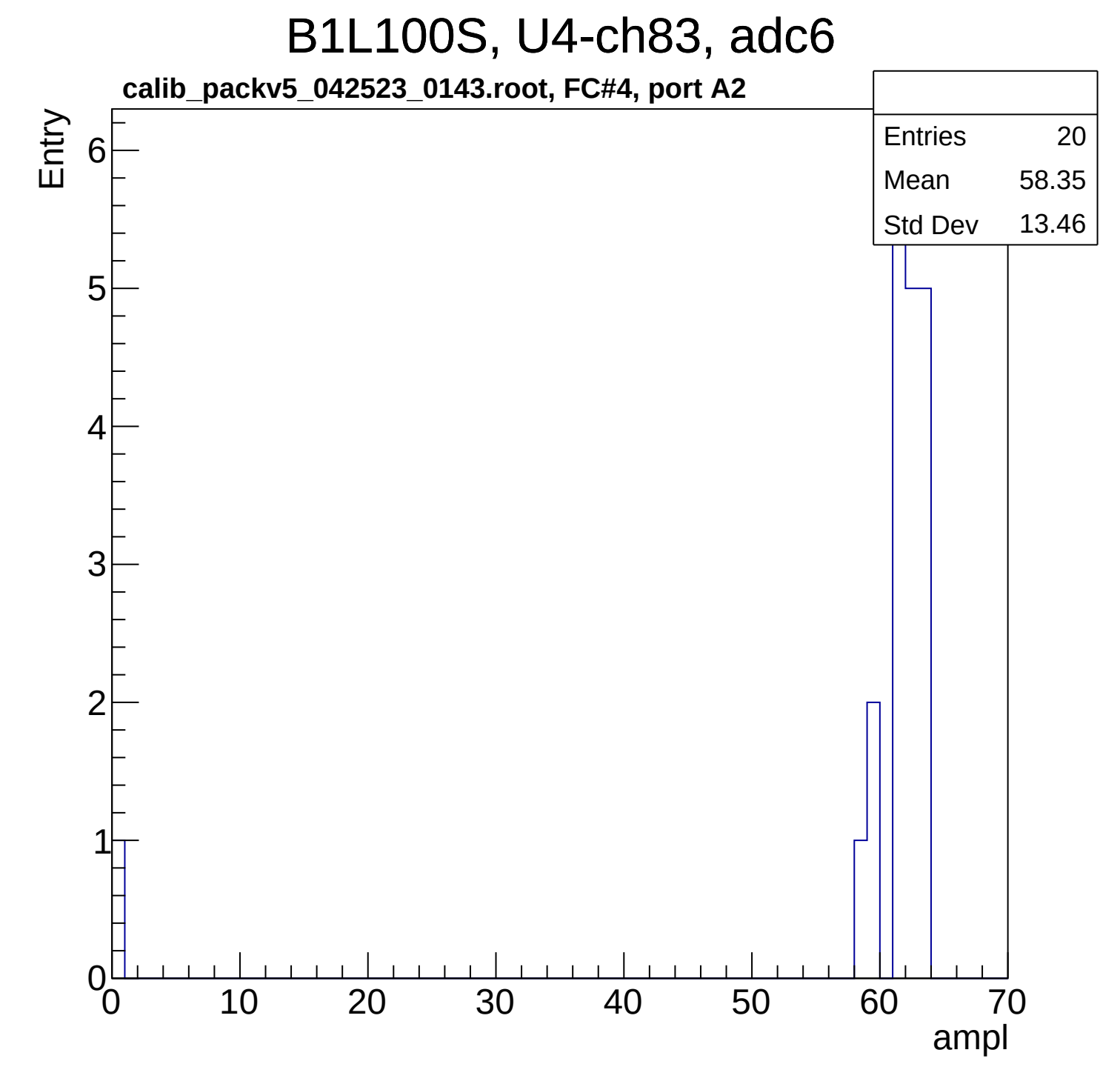

B1L100S, U4-ch83, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 86
Mean 33.87
Std Dev 3.722
Gaus mean : 34.3506
Gaus Width: 4.1516
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

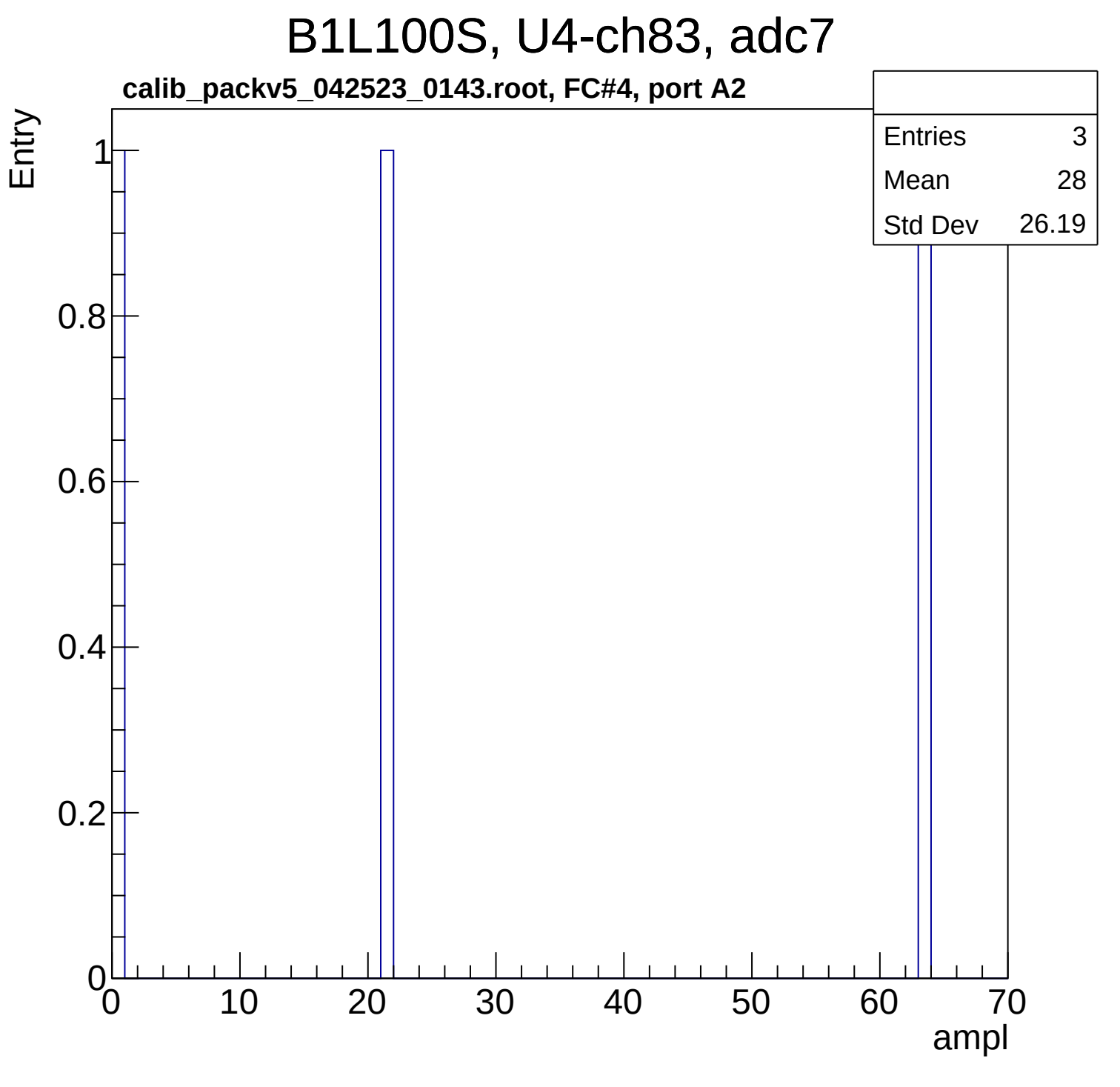

B1L100S, U4-ch83, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 41.99
Std Dev 3.609
Gaus mean : 43.2192
Gaus Width: 4.1757
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

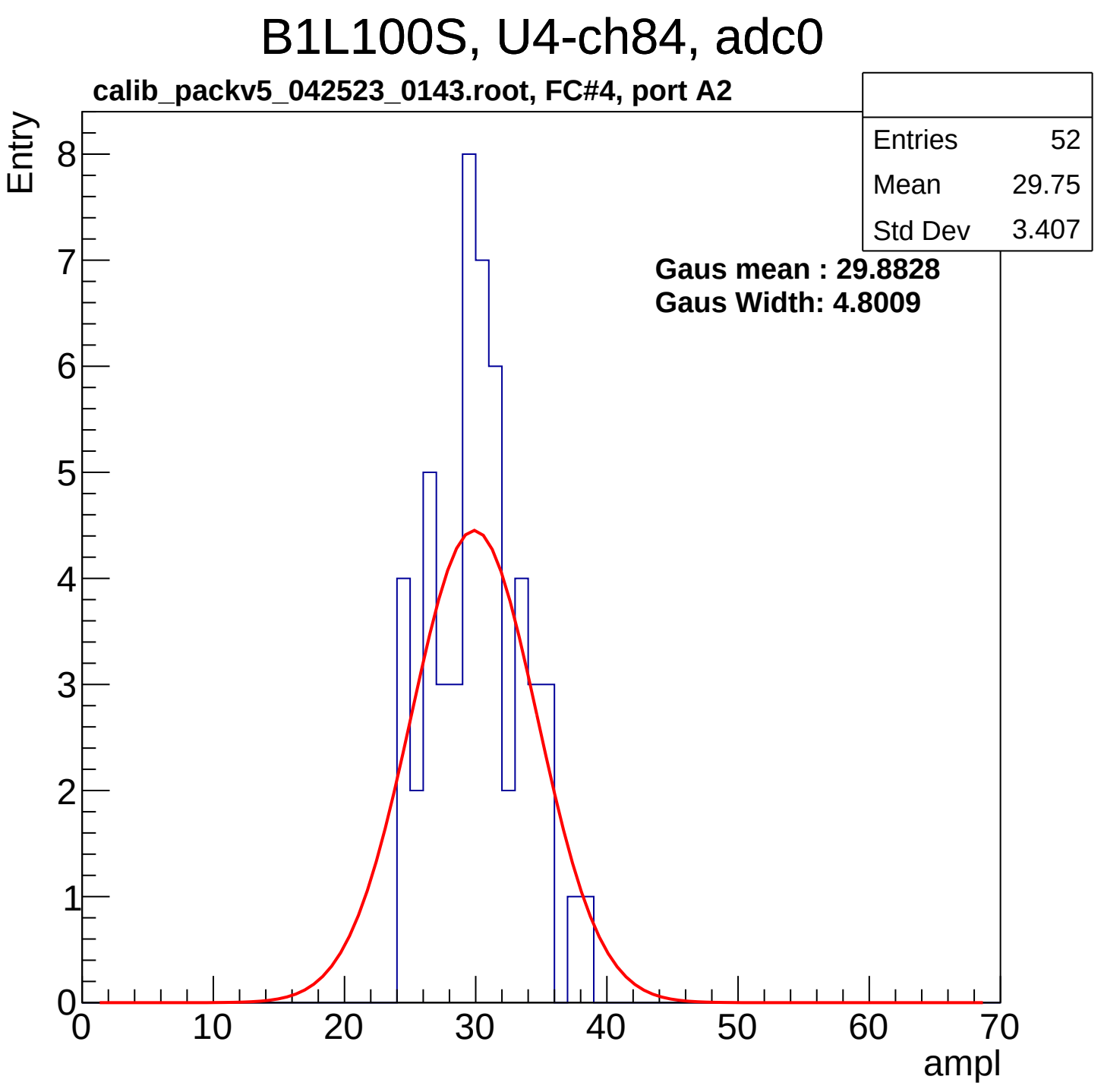

B1L100S, U4-ch83, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 44
Mean 47.59
Std Dev 3.689
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

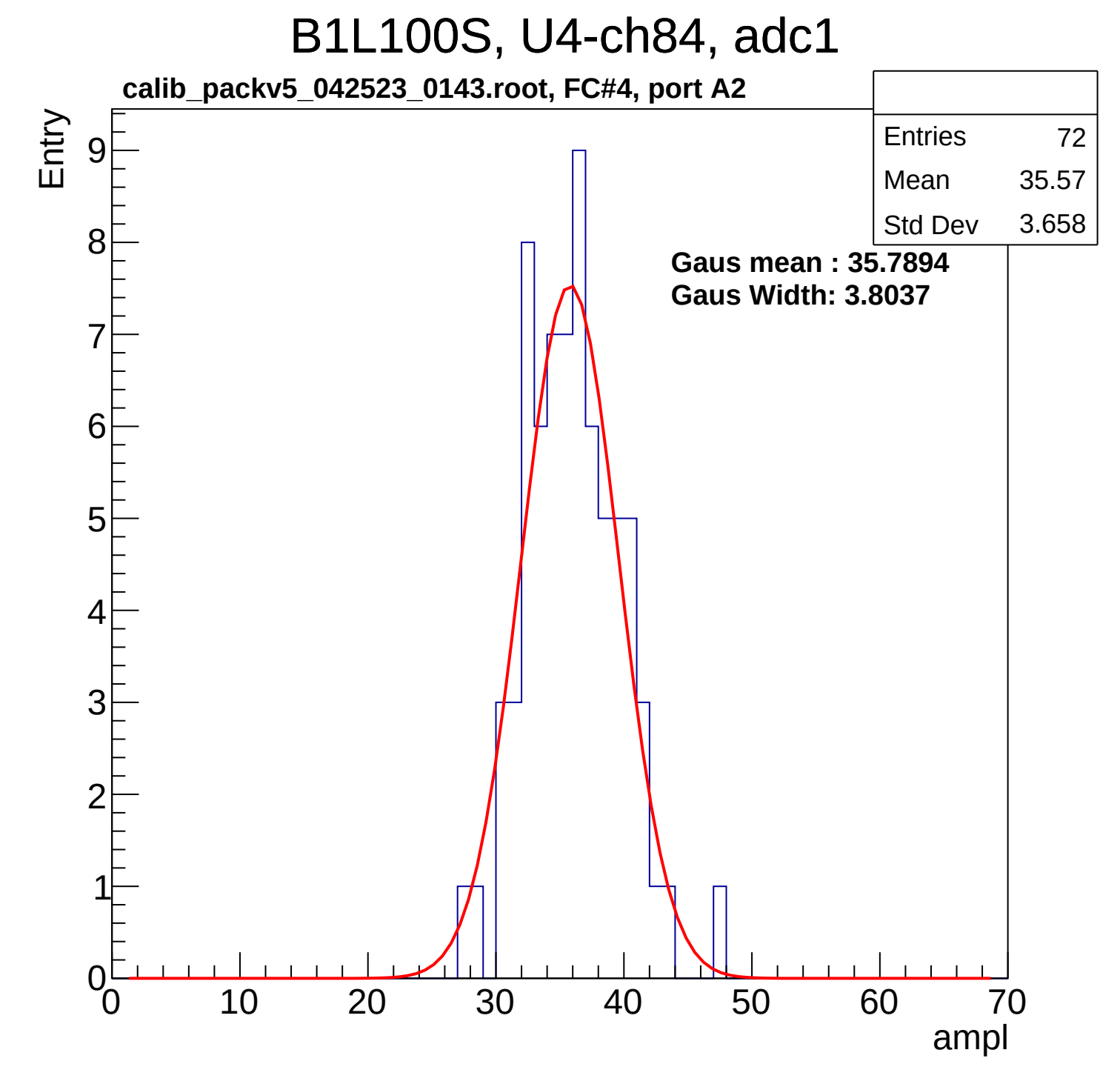

B1L100S, U4-ch83, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 53.03
Std Dev 3.866
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

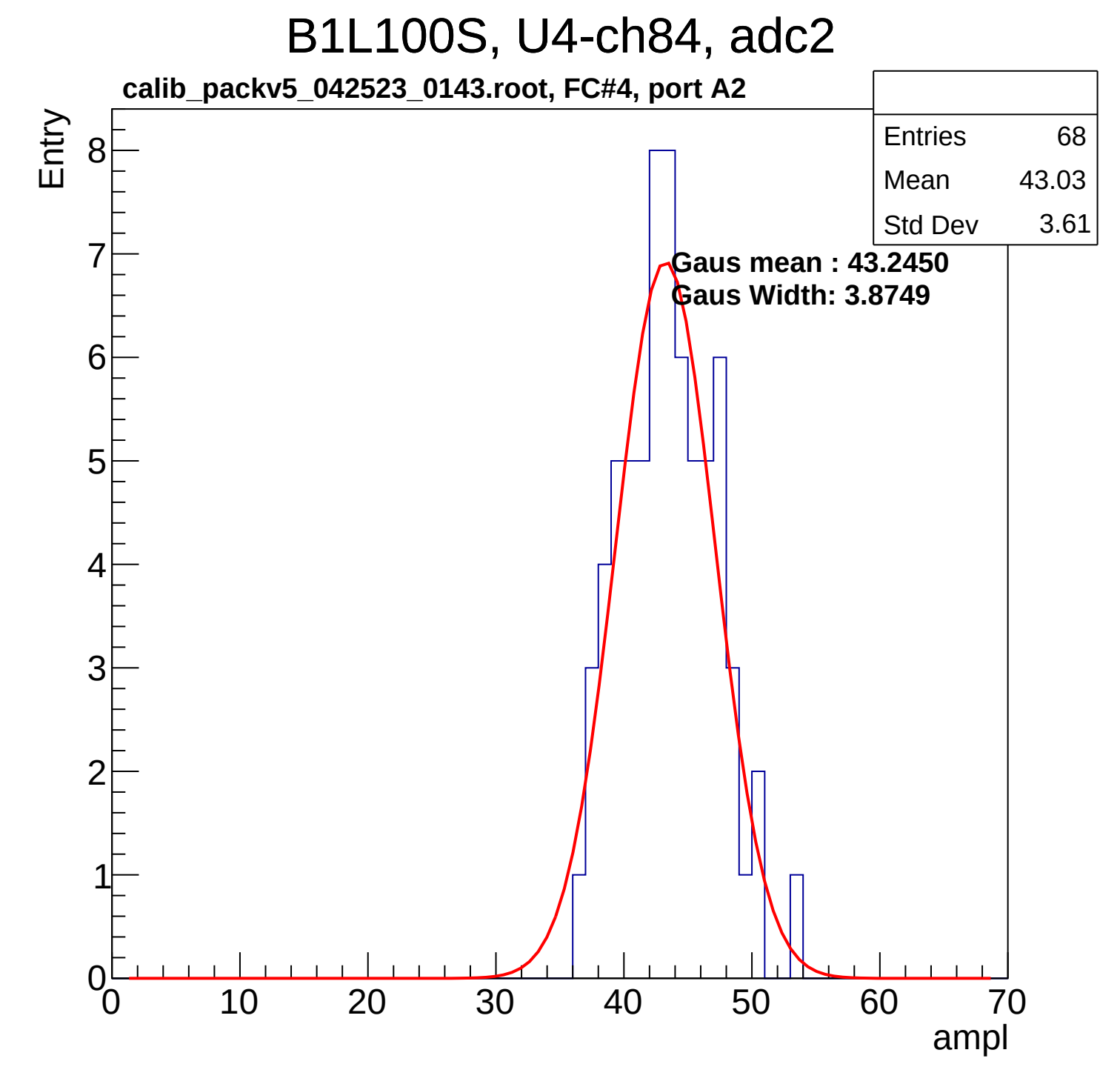

B1L100S, U4-ch83, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 42
Mean 59.24
Std Dev 2.389
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

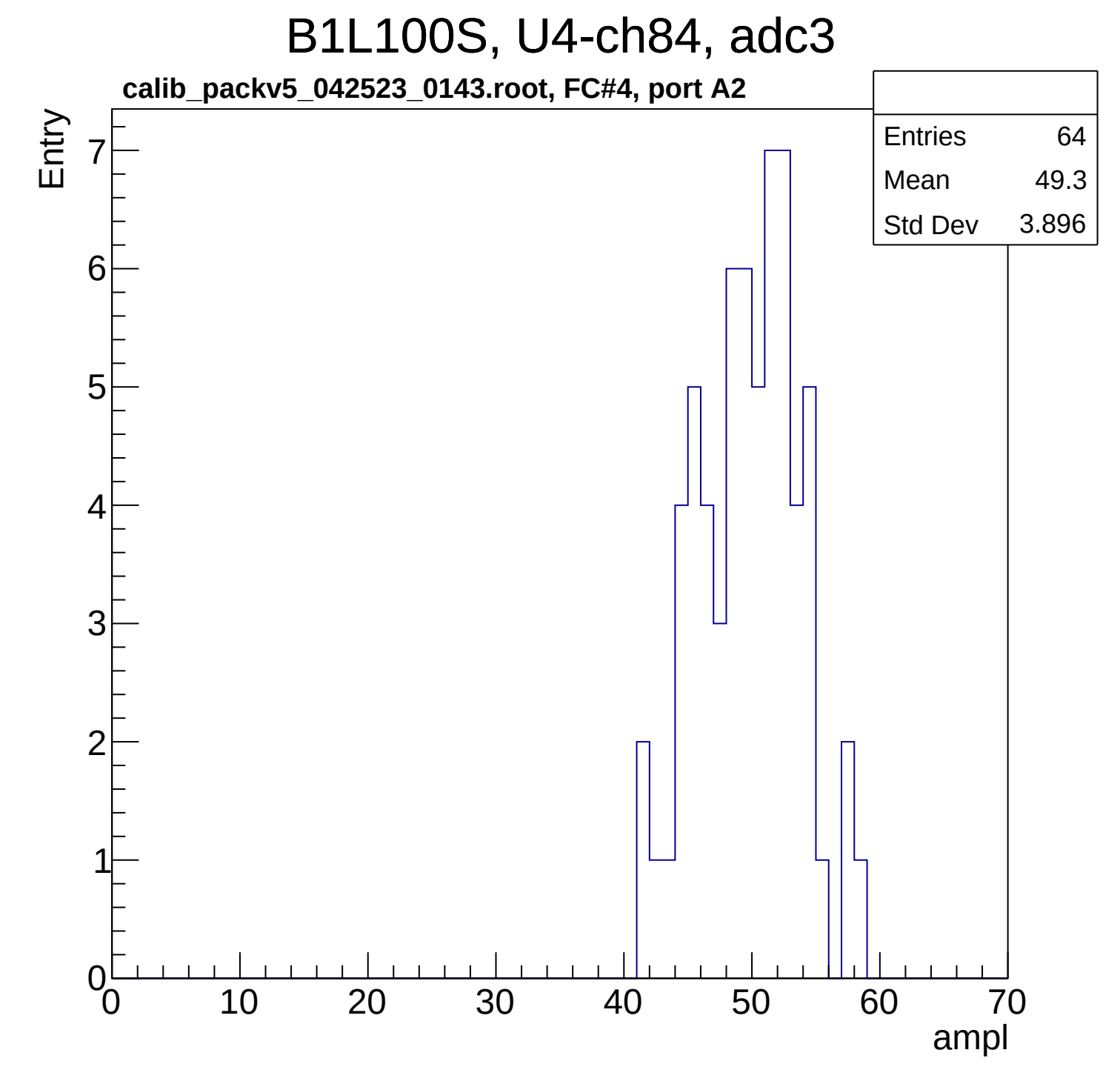

B1L100S, U4-ch83, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 20
Mean 58.35
Std Dev 13.46
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

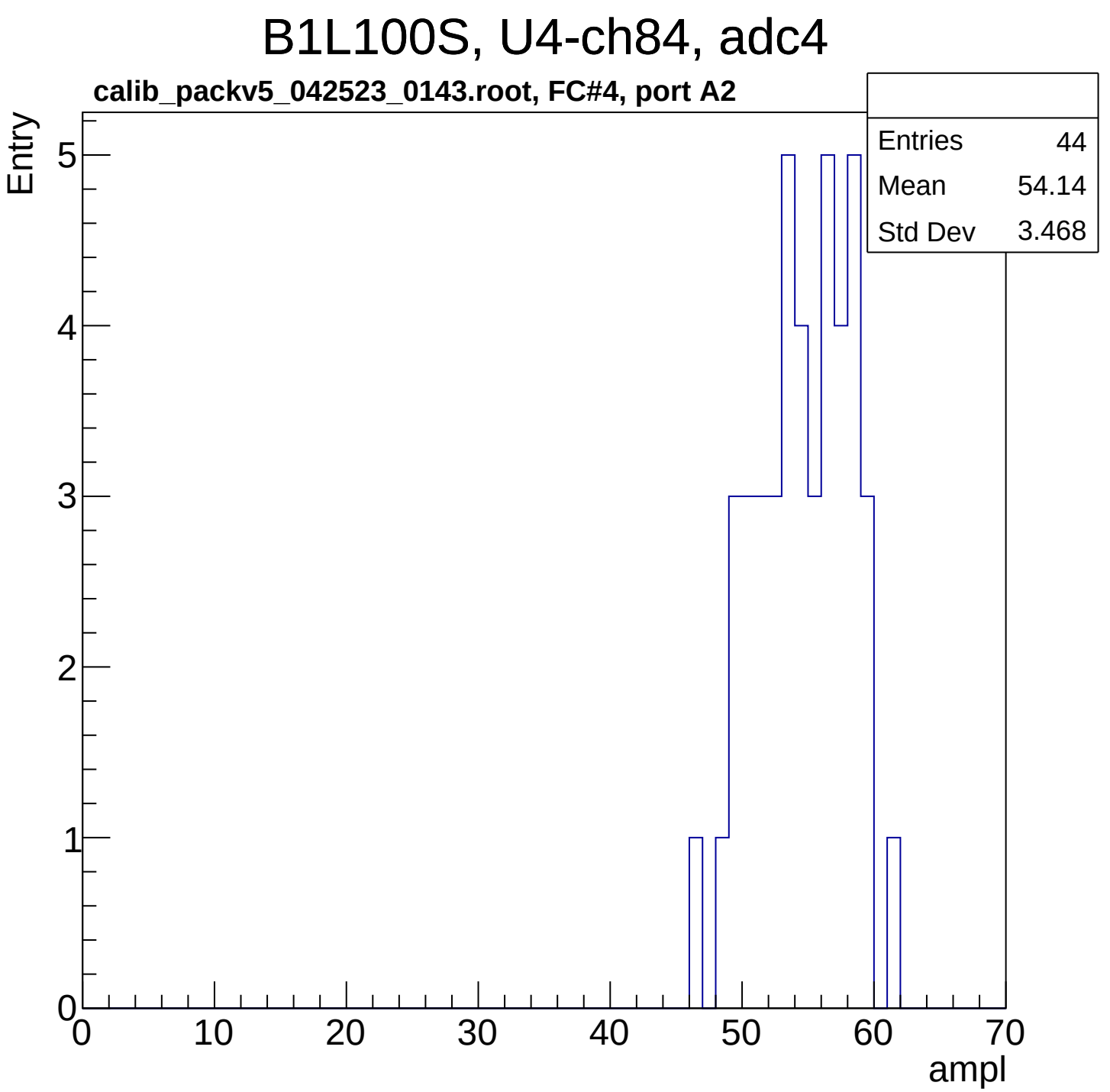

B1L100S, U4-ch83, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 28
Std Dev 26.19
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

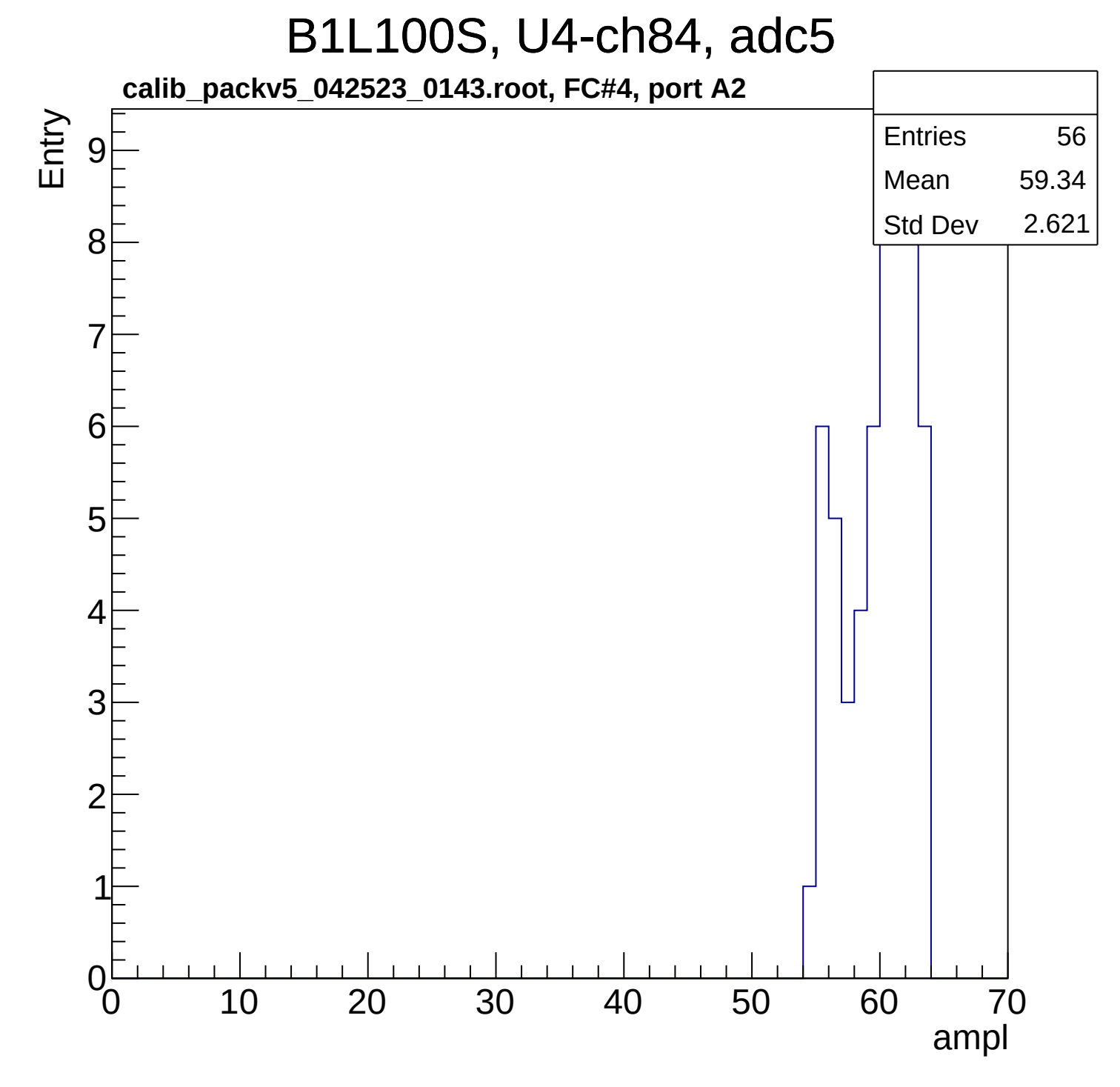

B1L100S, U4-ch84, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 29.75
Std Dev 3.407
Gaus mean : 29.8828
Gaus Width: 4.8009
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

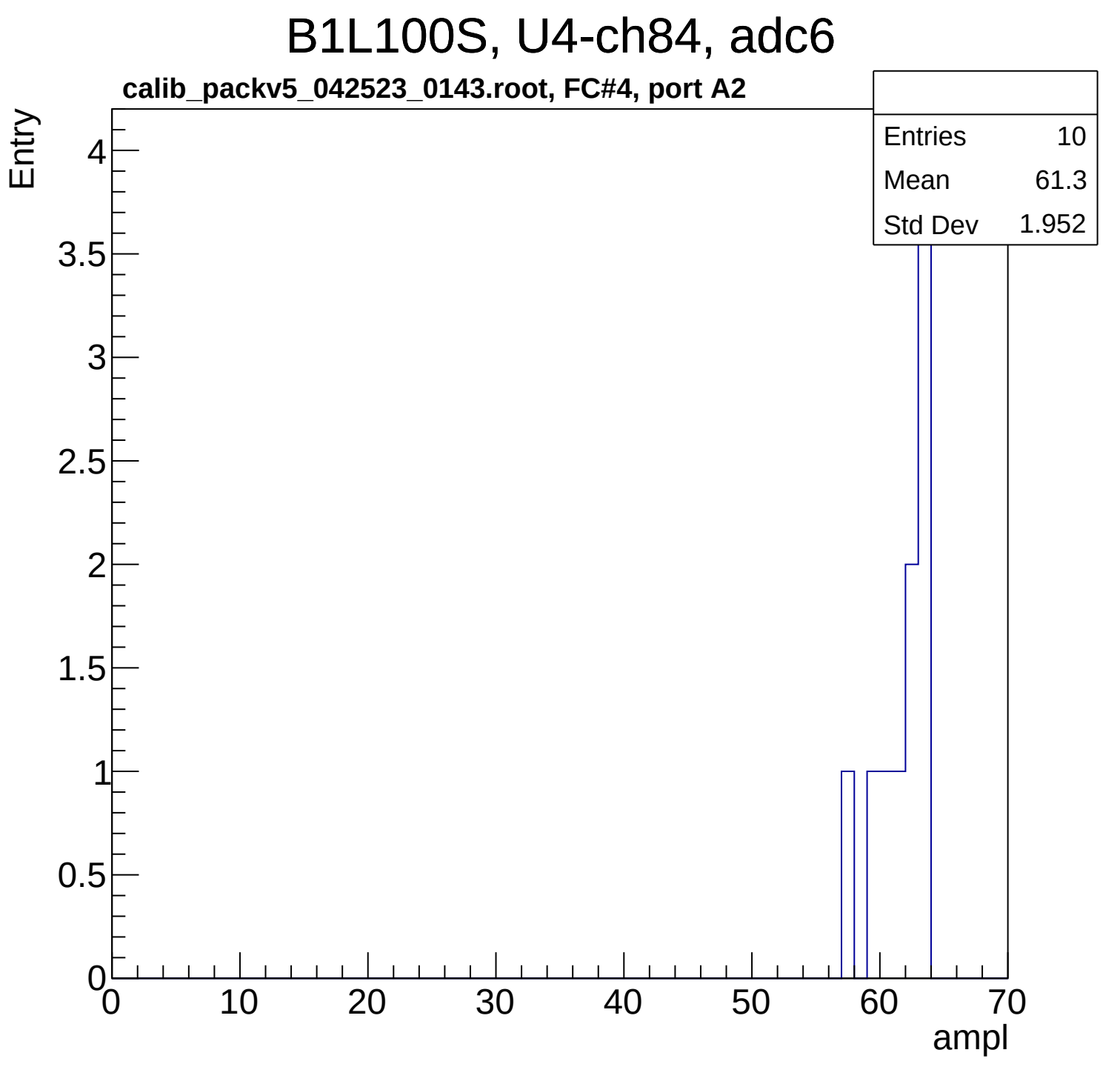

B1L100S, U4-ch84, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 35.57
Std Dev 3.658
Gaus mean : 35.7894
Gaus Width: 3.8037
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

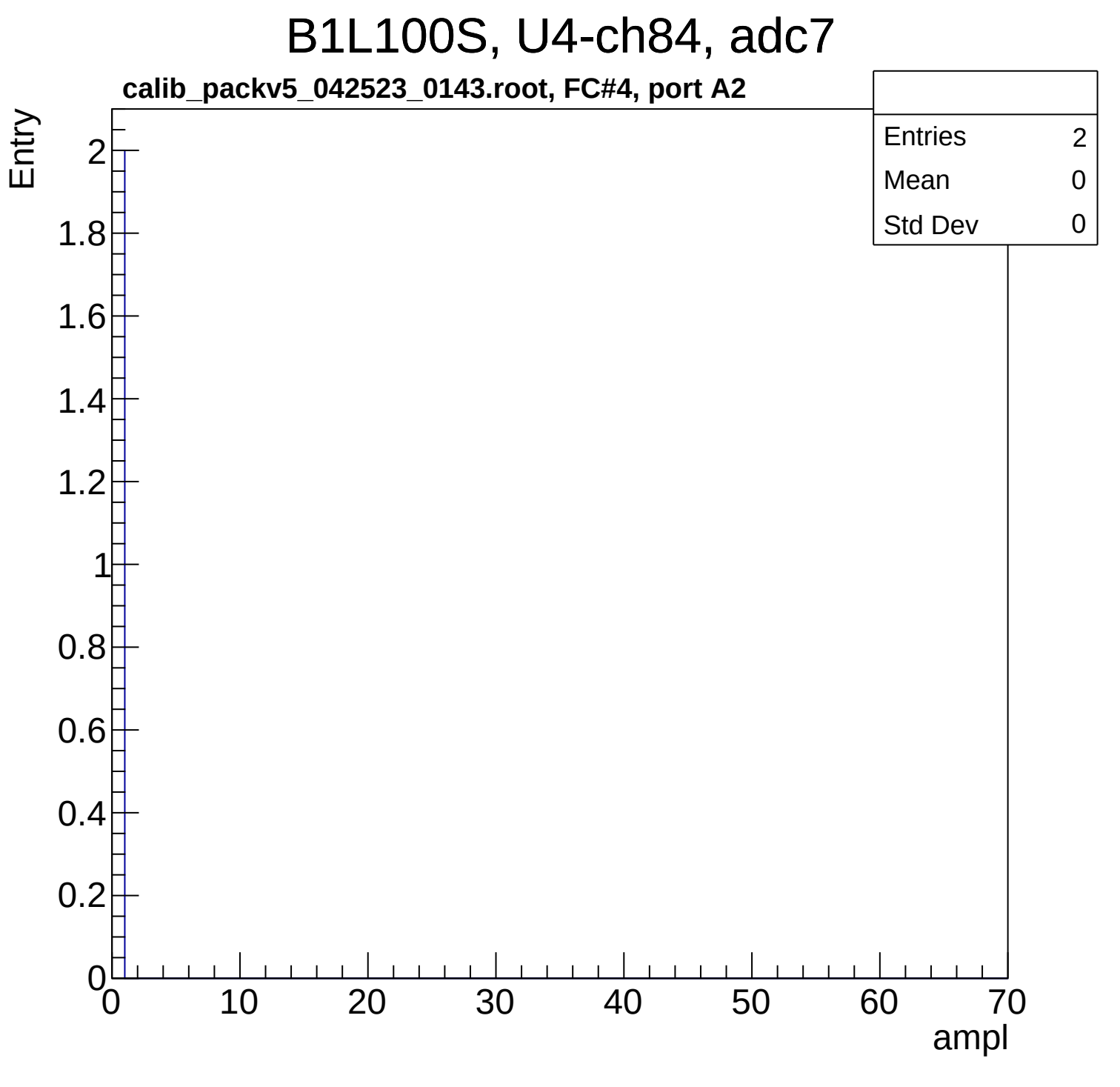

B1L100S, U4-ch84, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 43.03
Std Dev 3.61
Gaus mean : 43.2450
Gaus Width: 3.8749
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

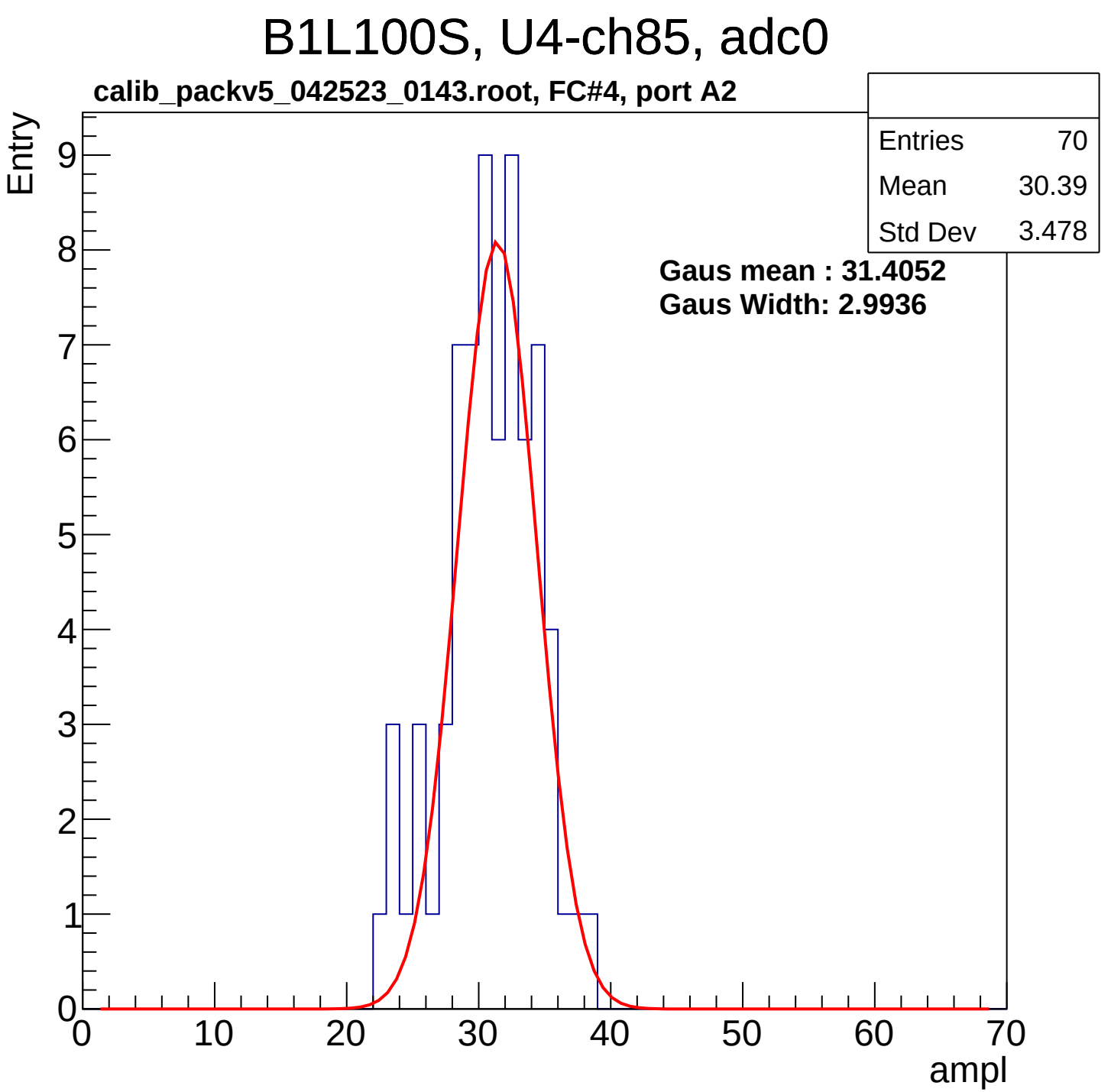

B1L100S, U4-ch84, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 49.3
Std Dev 3.896
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

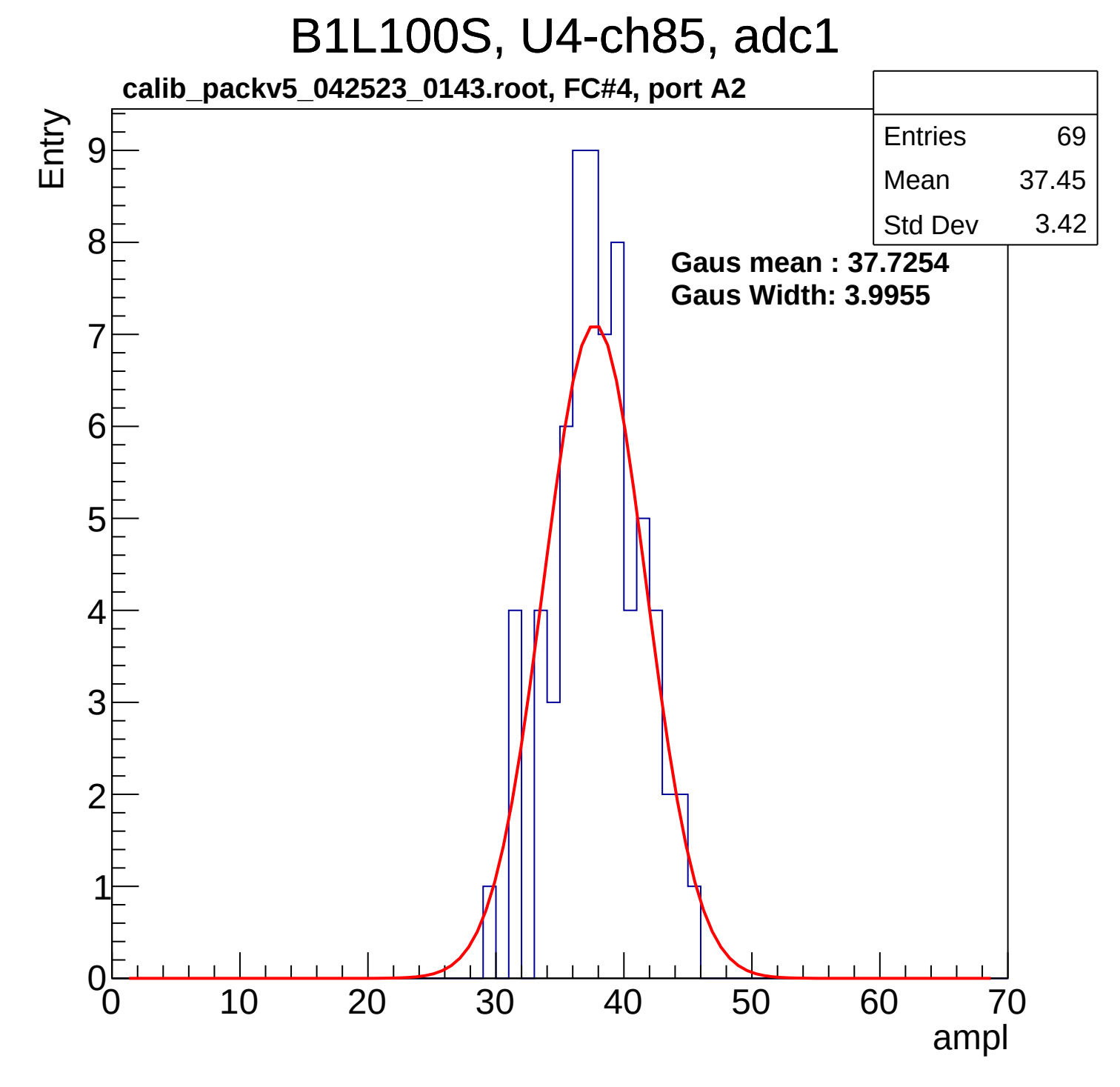

B1L100S, U4-ch84, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 44
Mean 54.14
Std Dev 3.468
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

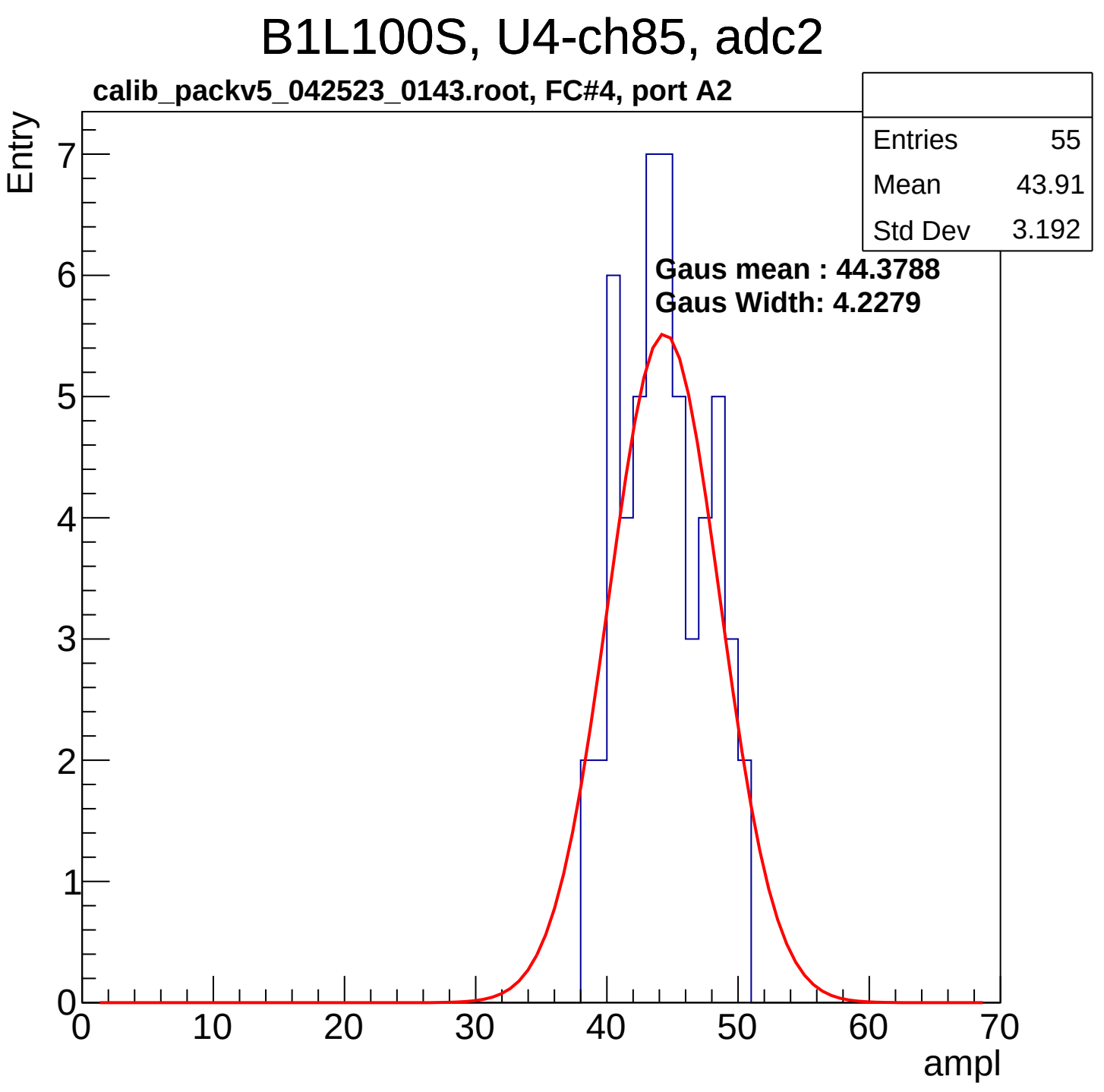

B1L100S, U4-ch84, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 59.34
Std Dev 2.621
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

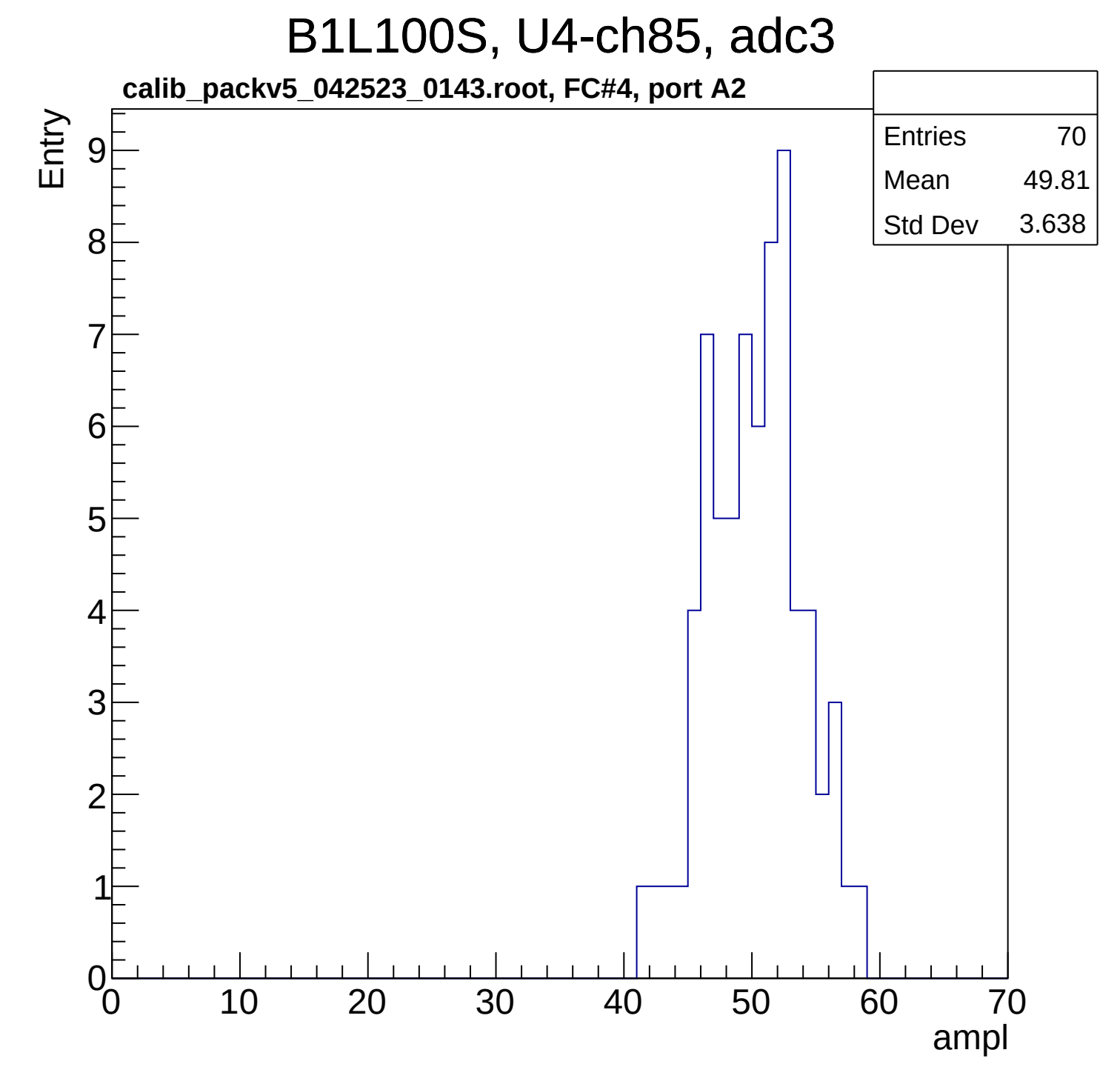

B1L100S, U4-ch84, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 61.3
Std Dev 1.952
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

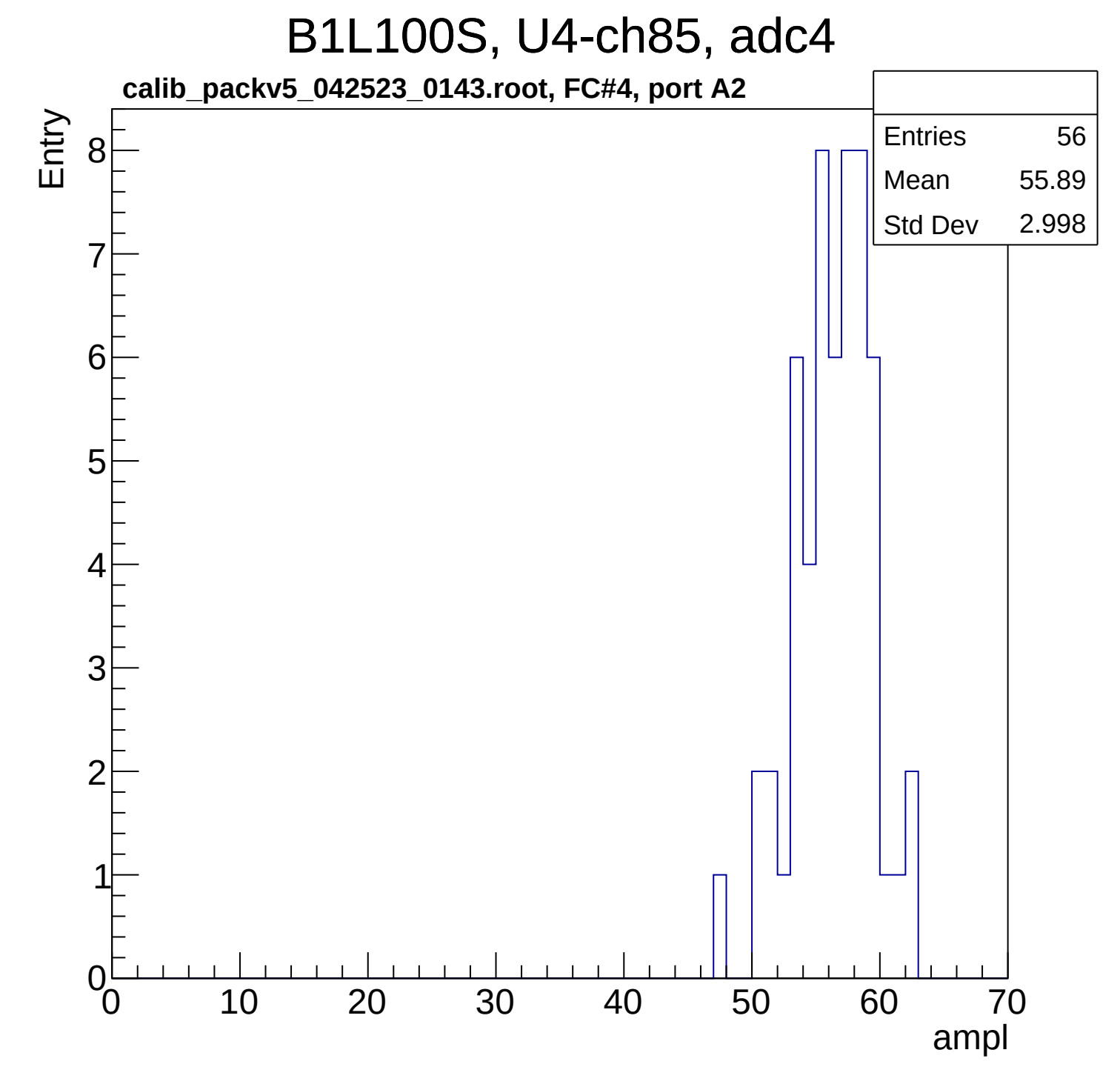

B1L100S, U4-ch84, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

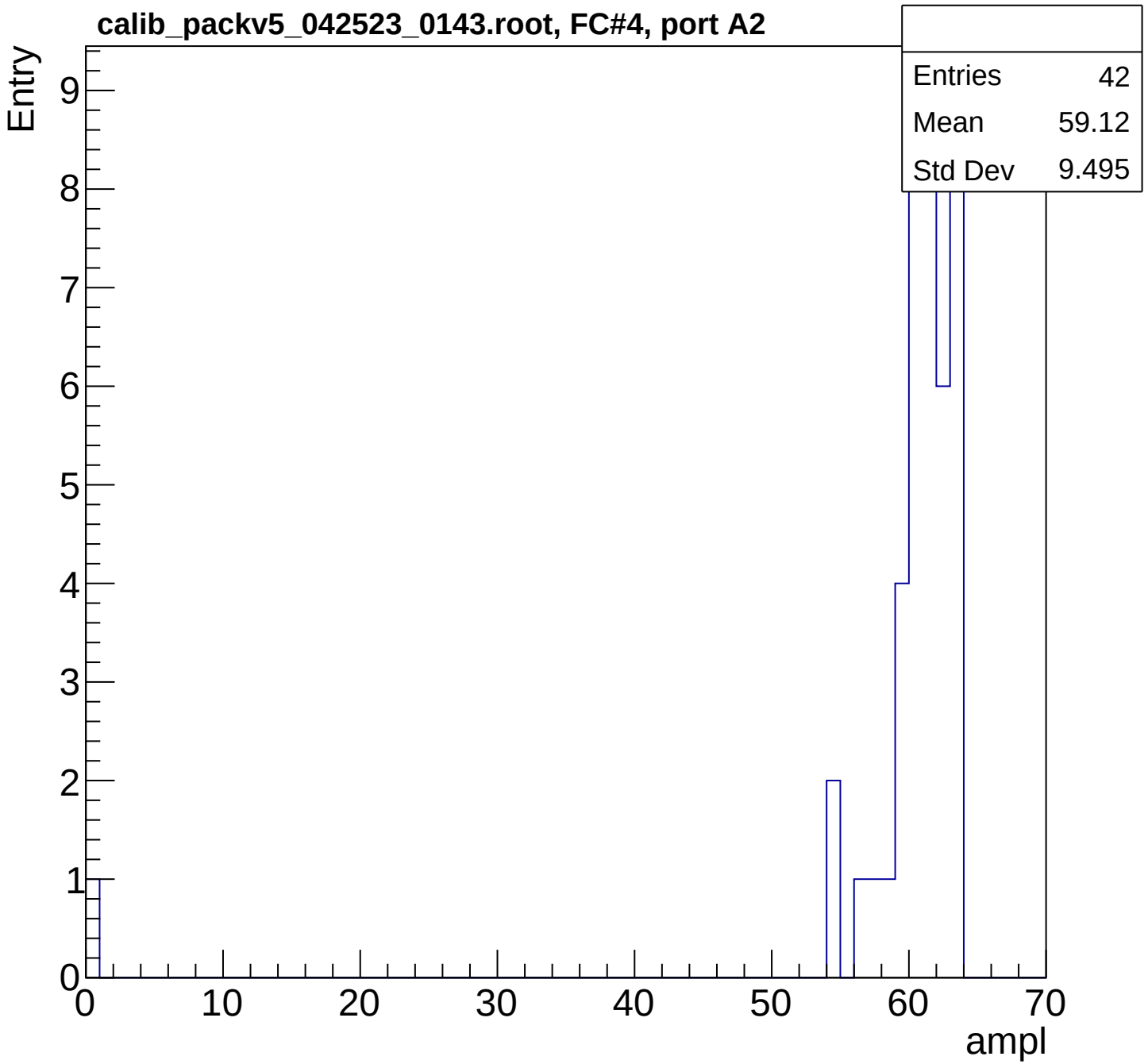

B1L100S, U4-ch85, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 30.39
Std Dev 3.478
Gaus mean : 31.4052
Gaus Width: 2.9936
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

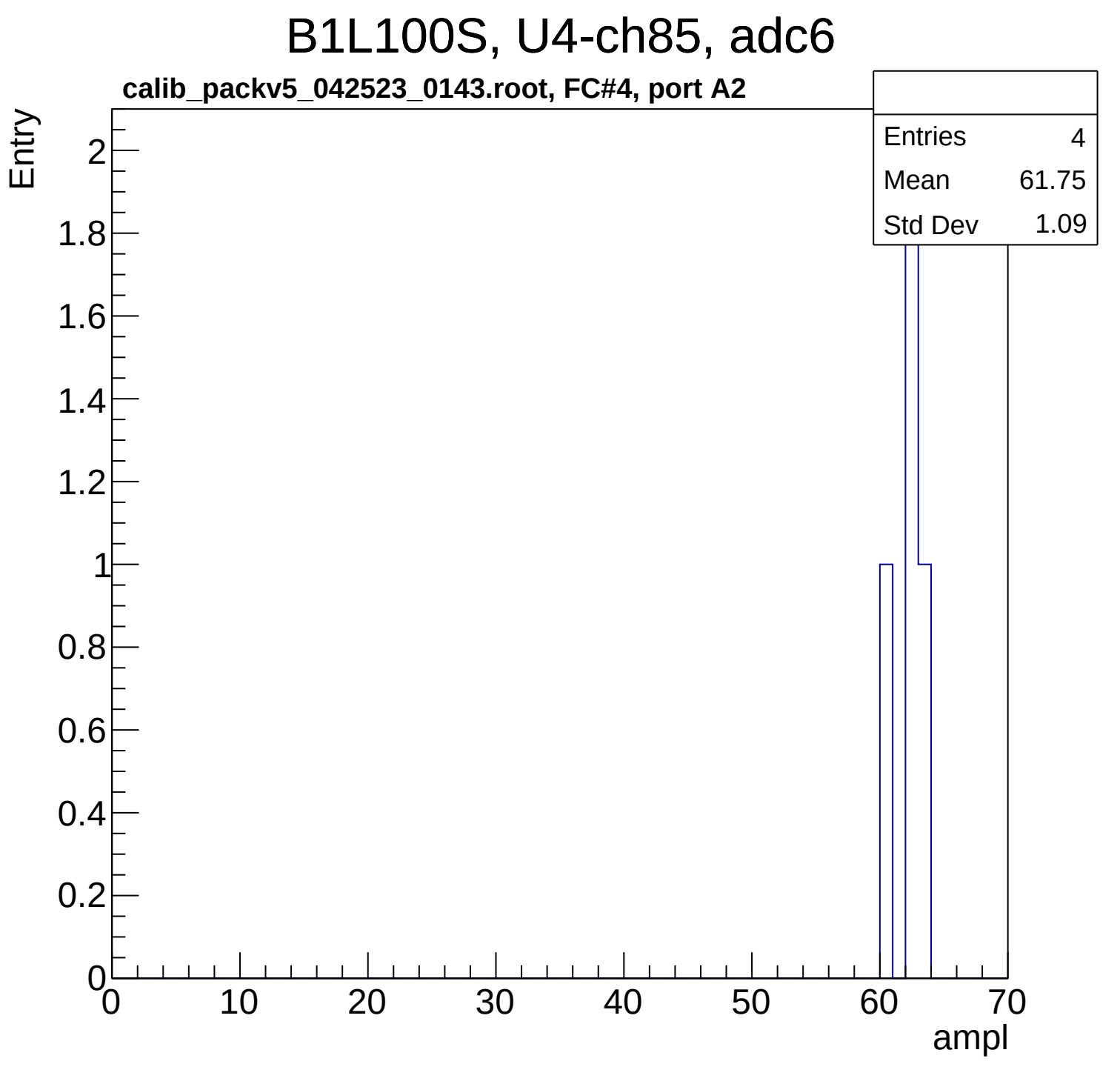

B1L100S, U4-ch85, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 37.45
Std Dev 3.42
Gaus mean : 37.7254
Gaus Width: 3.9955
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

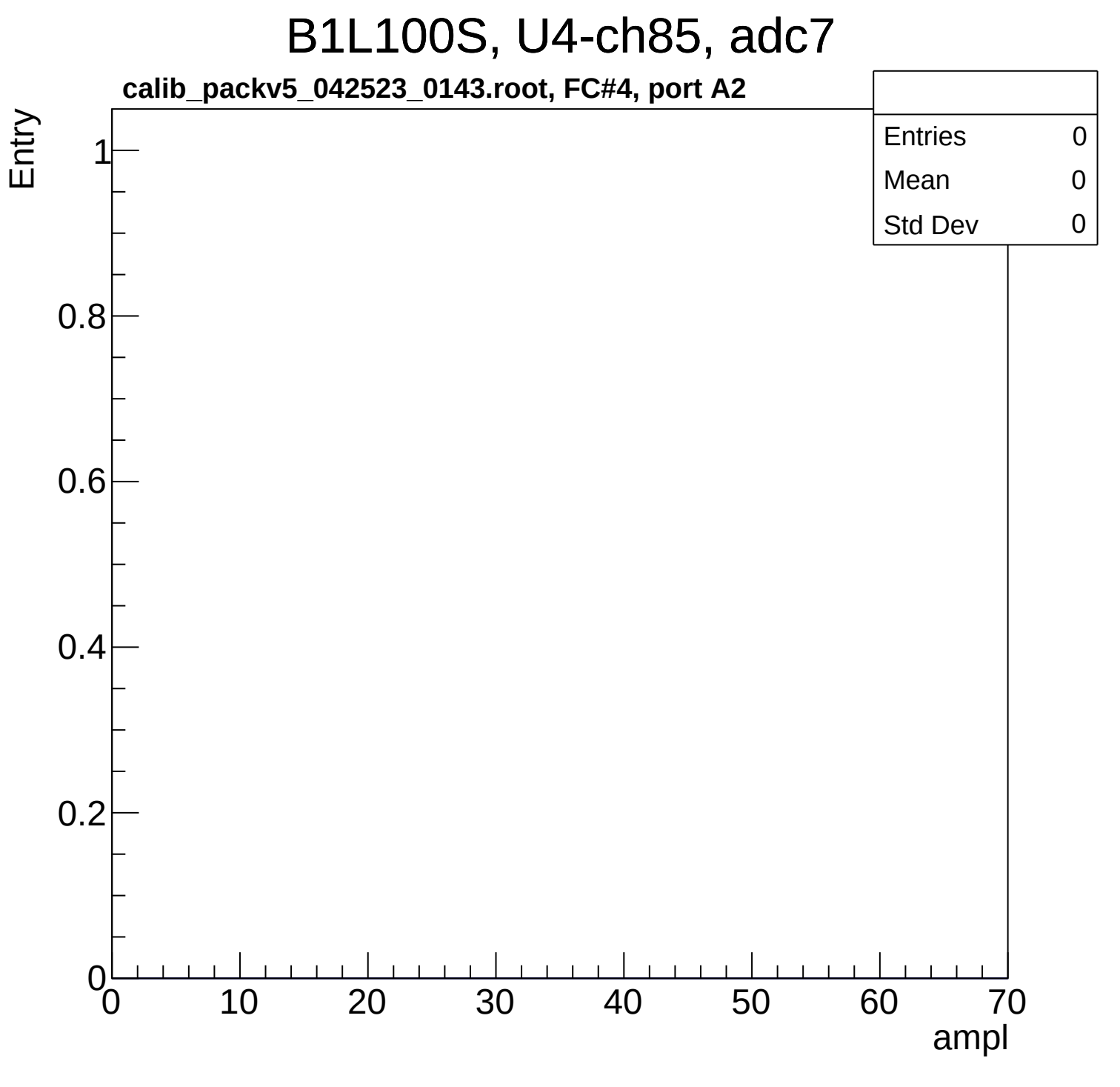

B1L100S, U4-ch85, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 43.91
Std Dev 3.192
Gaus mean : 44.3788
Gaus Width: 4.2279
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

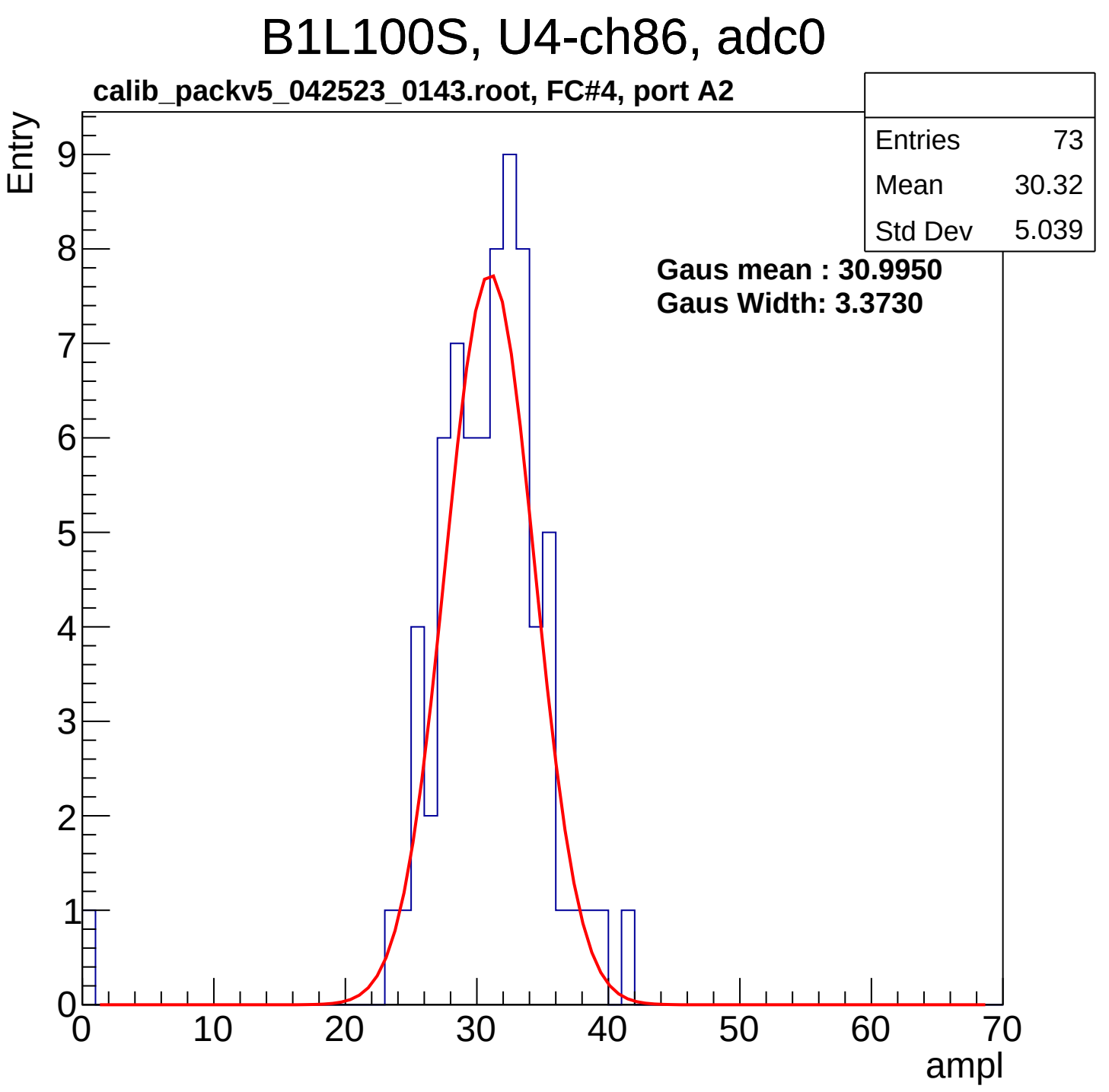

B1L100S, U4-ch85, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 49.81
Std Dev 3.638
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

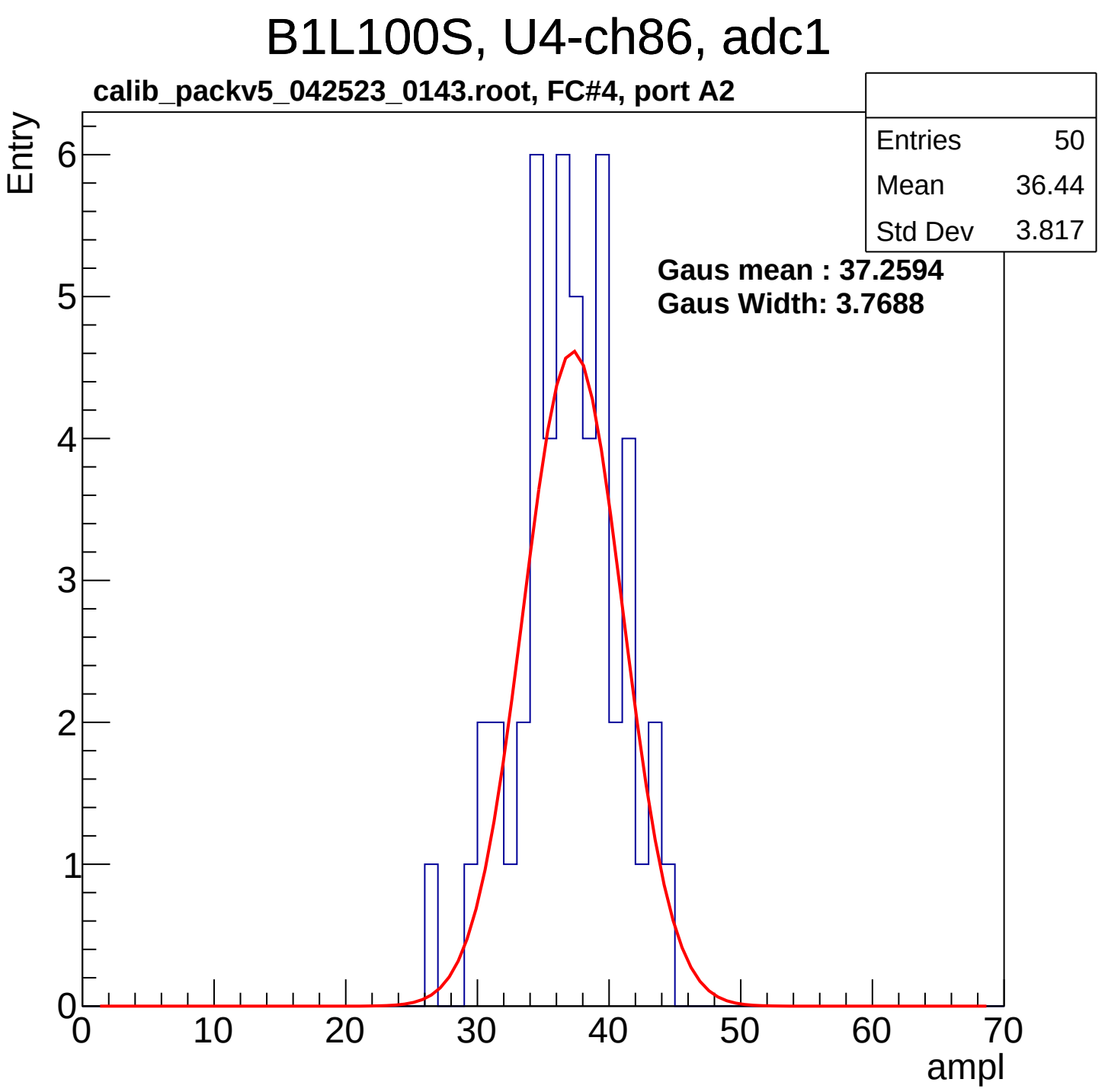

B1L100S, U4-ch85, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 55.89
Std Dev 2.998
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

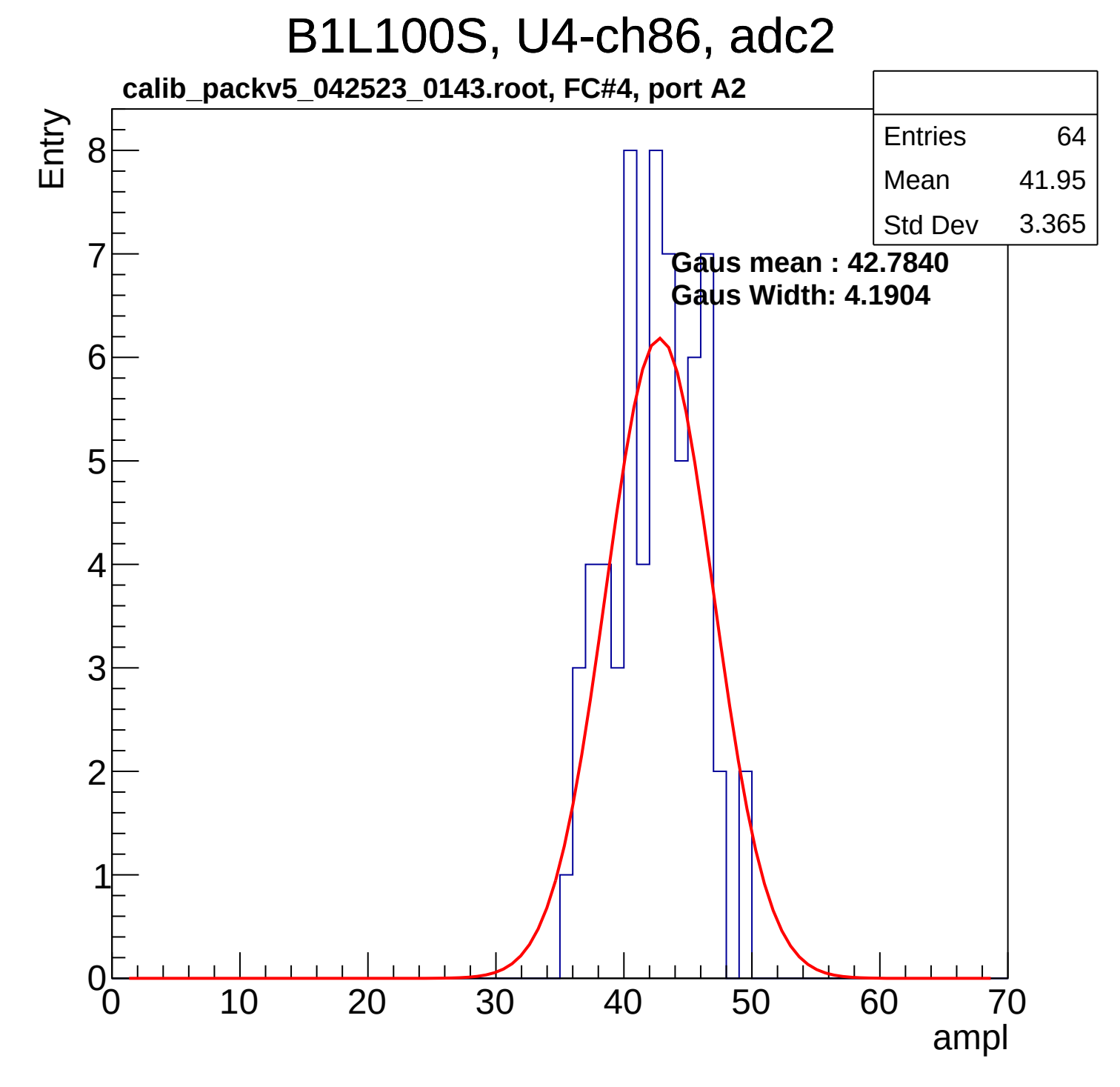

B1L100S, U4-ch85, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 42
Mean 59.12
Std Dev 9.495
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

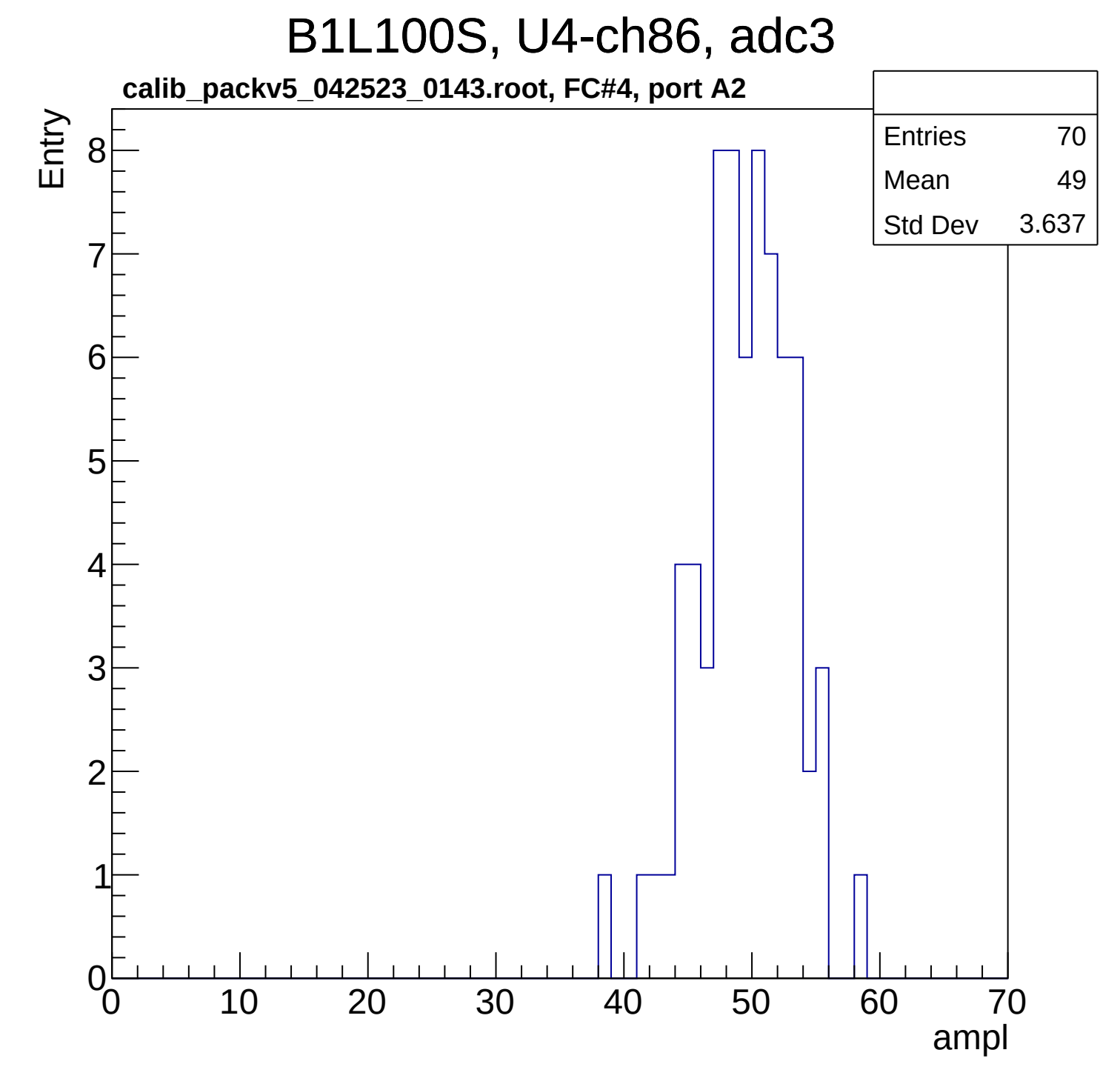

B1L100S, U4-ch85, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 61.75
Std Dev 1.09
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

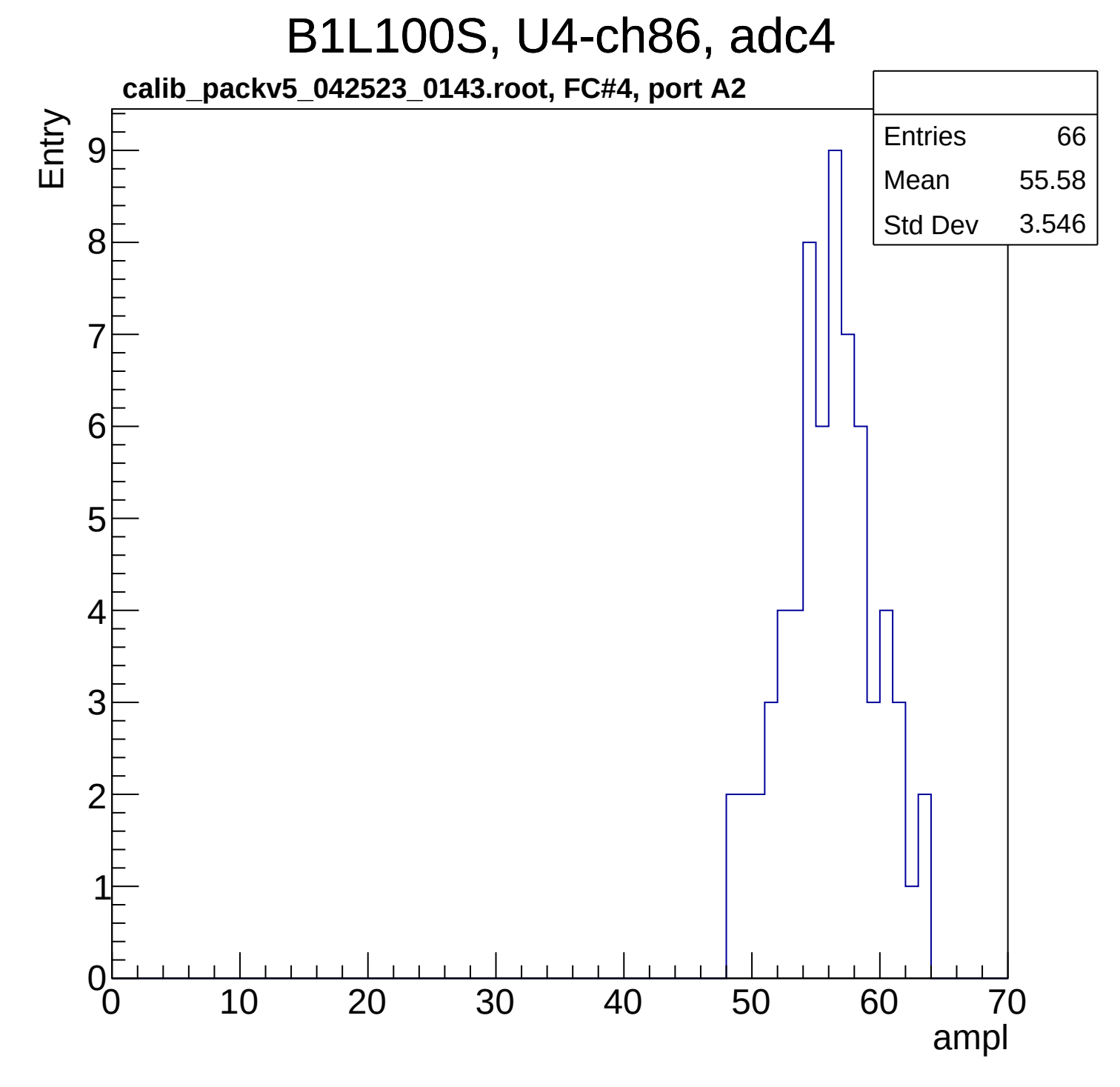

B1L100S, U4-ch85, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

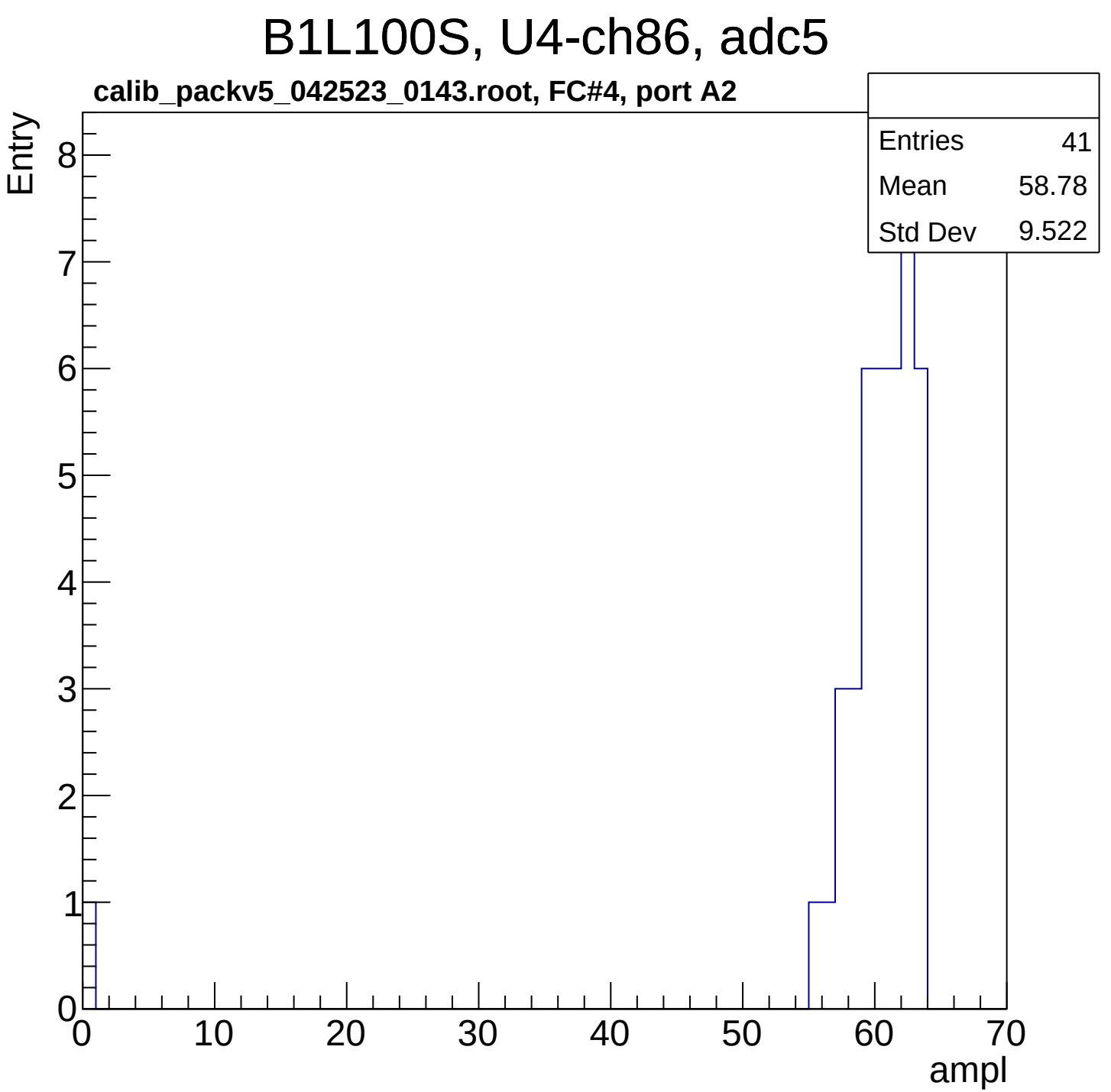

B1L100S, U4-ch86, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 30.32
Std Dev 5.039
Gaus mean : 30.9950
Gaus Width: 3.3730
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

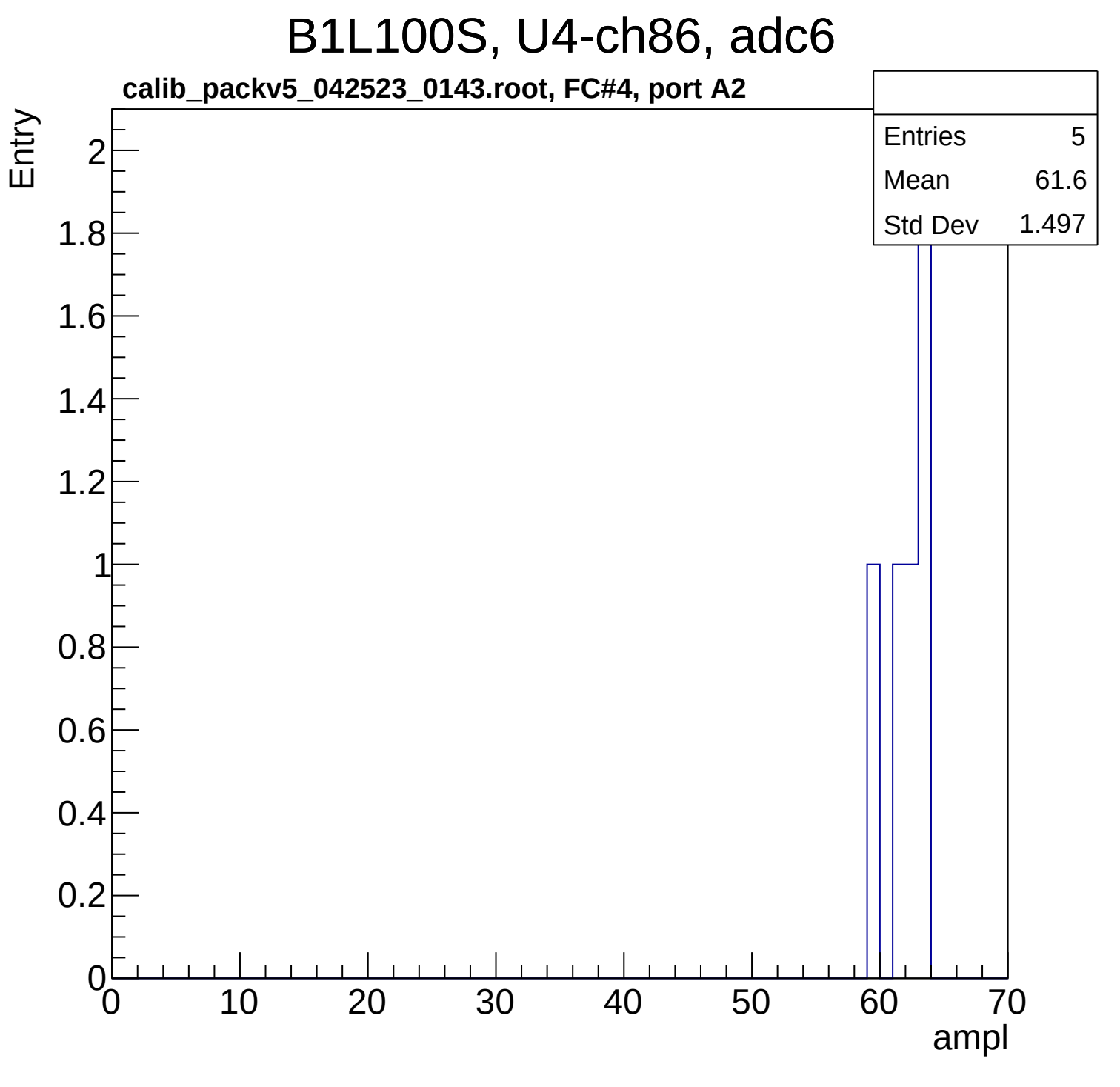

B1L100S, U4-ch86, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 36.44
Std Dev 3.817
Gaus mean : 37.2594
Gaus Width: 3.7688
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

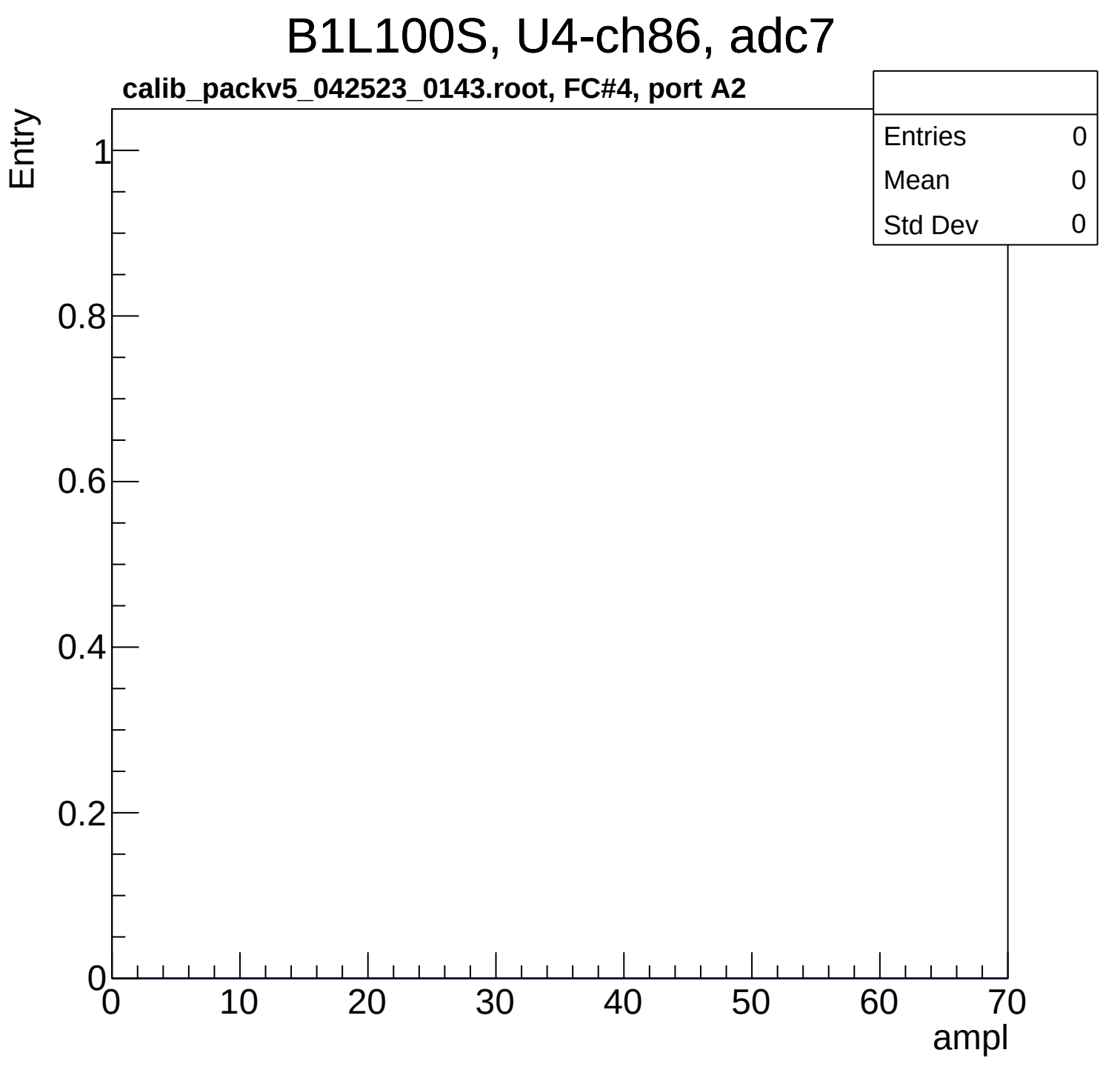

B1L100S, U4-ch86, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 41.95
Std Dev 3.365
Gaus mean : 42.7840
Gaus Width: 4.1904
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

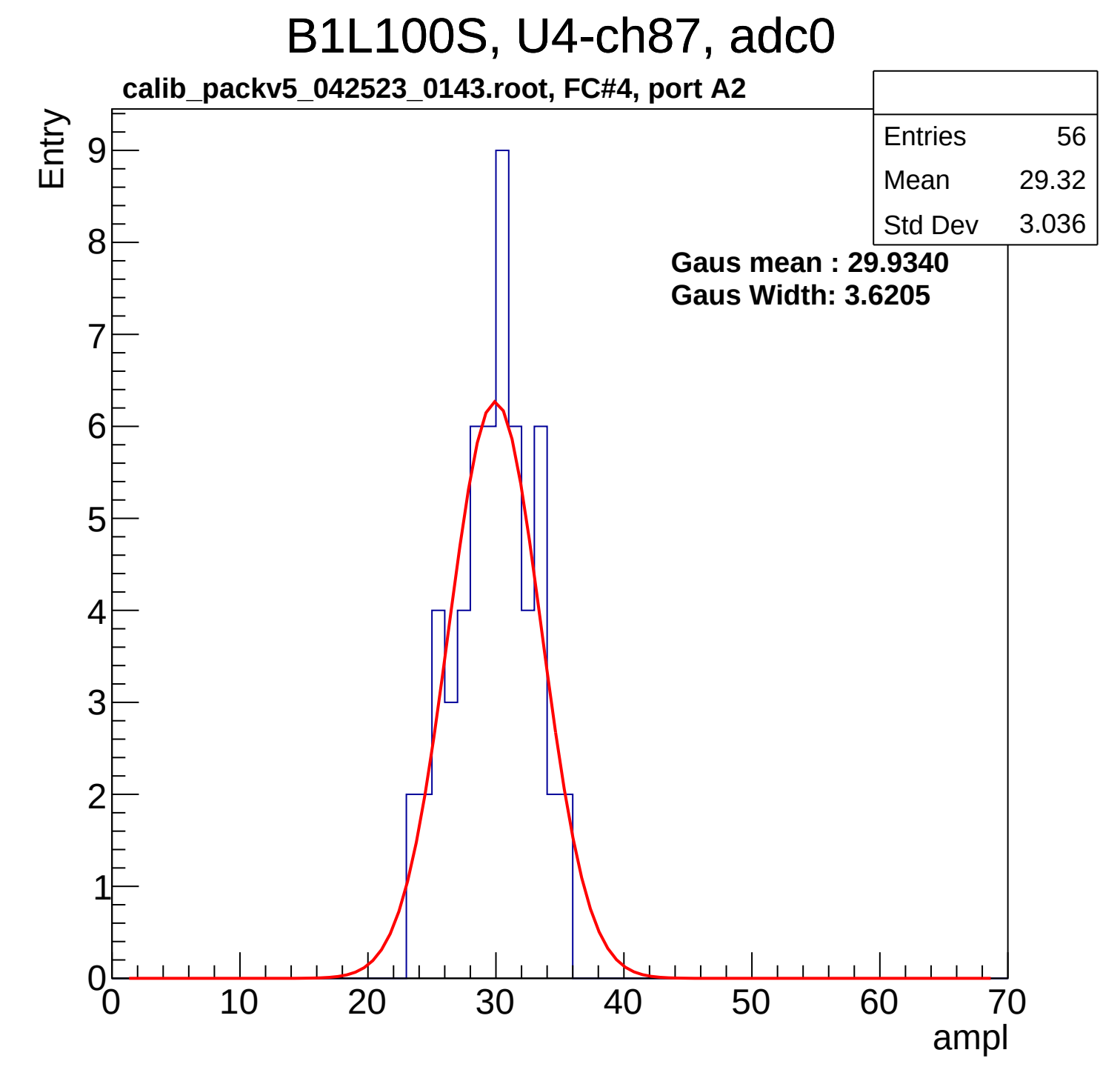

B1L100S, U4-ch86, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 49
Std Dev 3.637
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

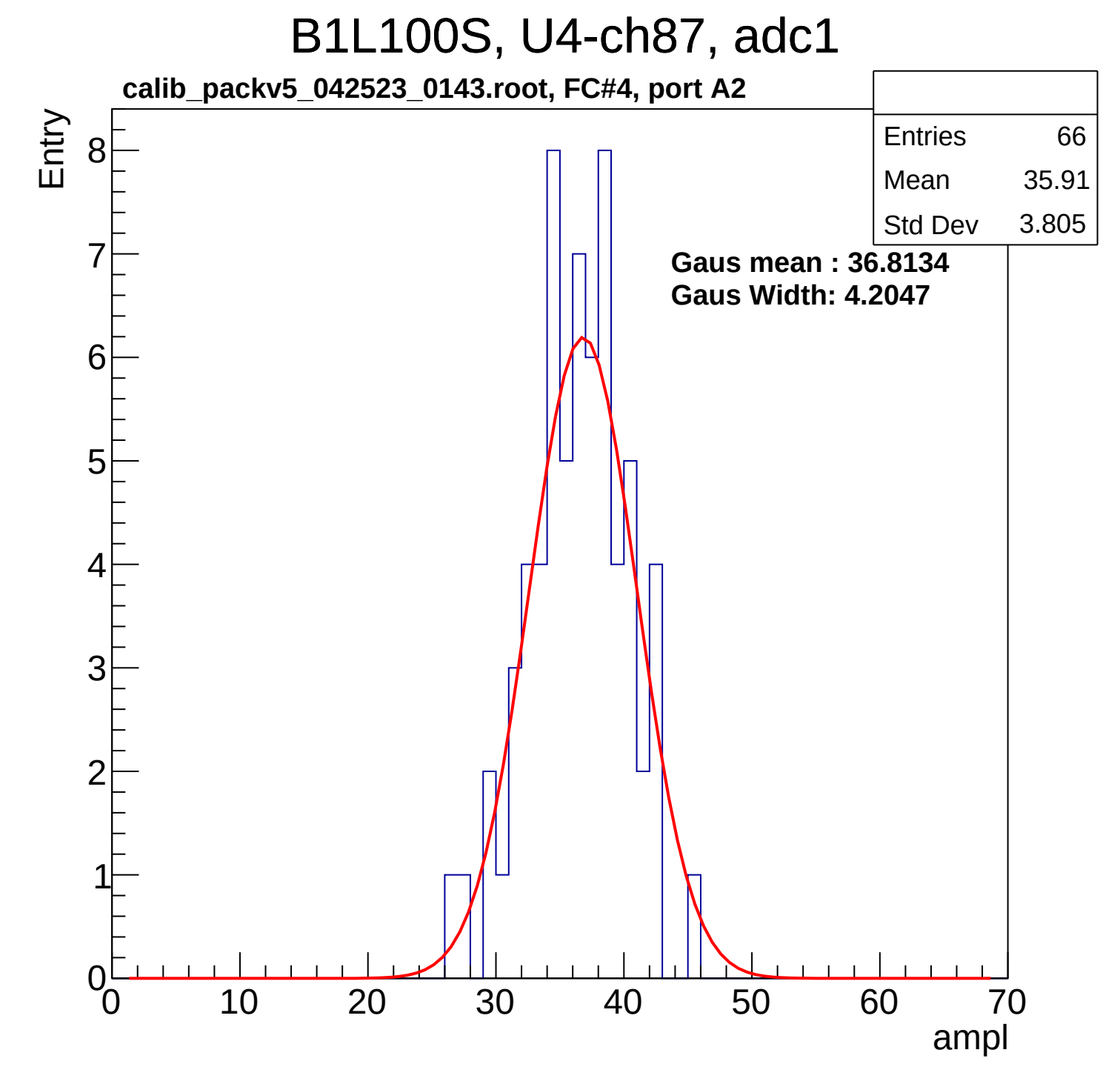

B1L100S, U4-ch86, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 55.58
Std Dev 3.546
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

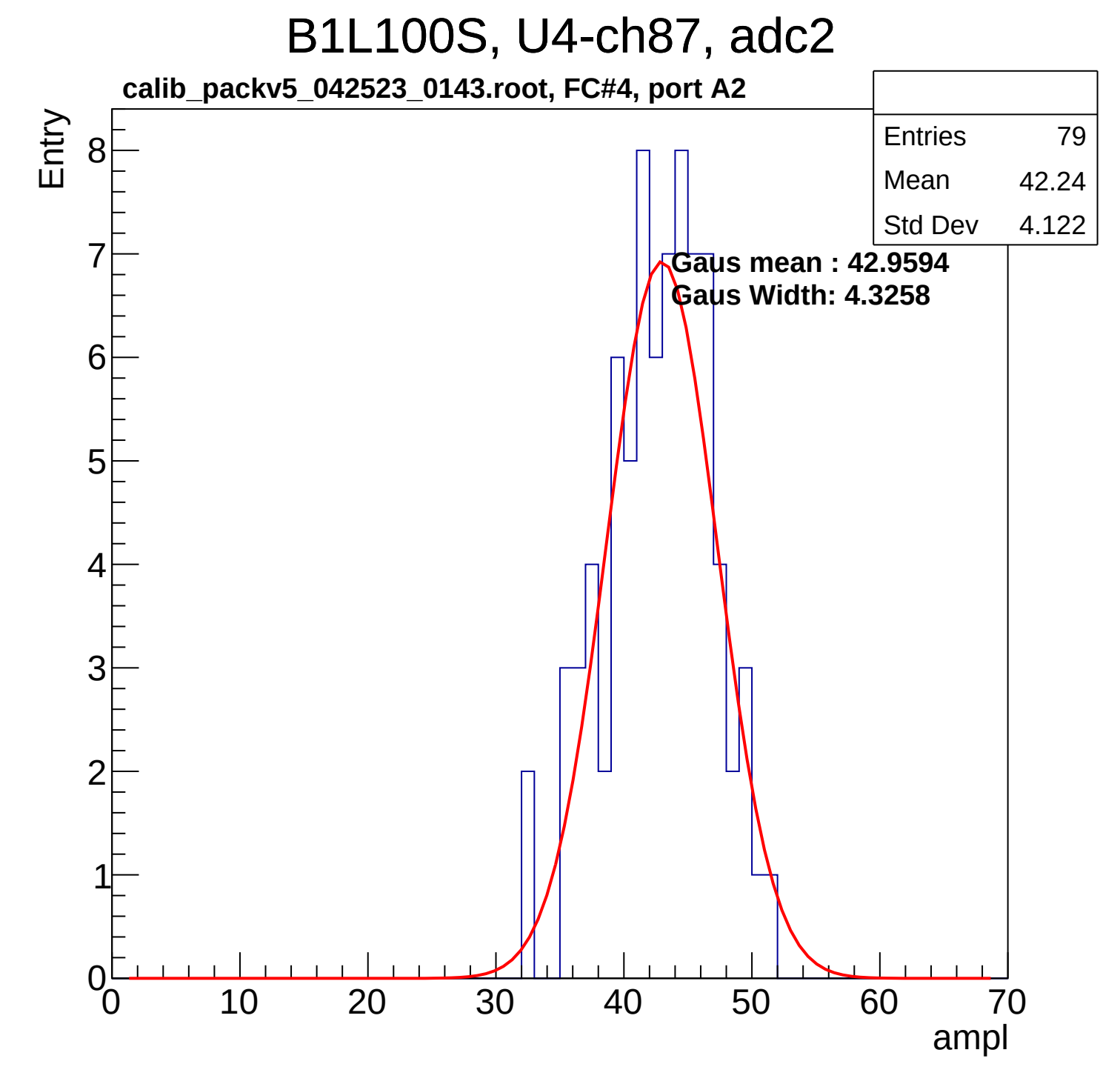

B1L100S, U4-ch86, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 41
Mean 58.78
Std Dev 9.522
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

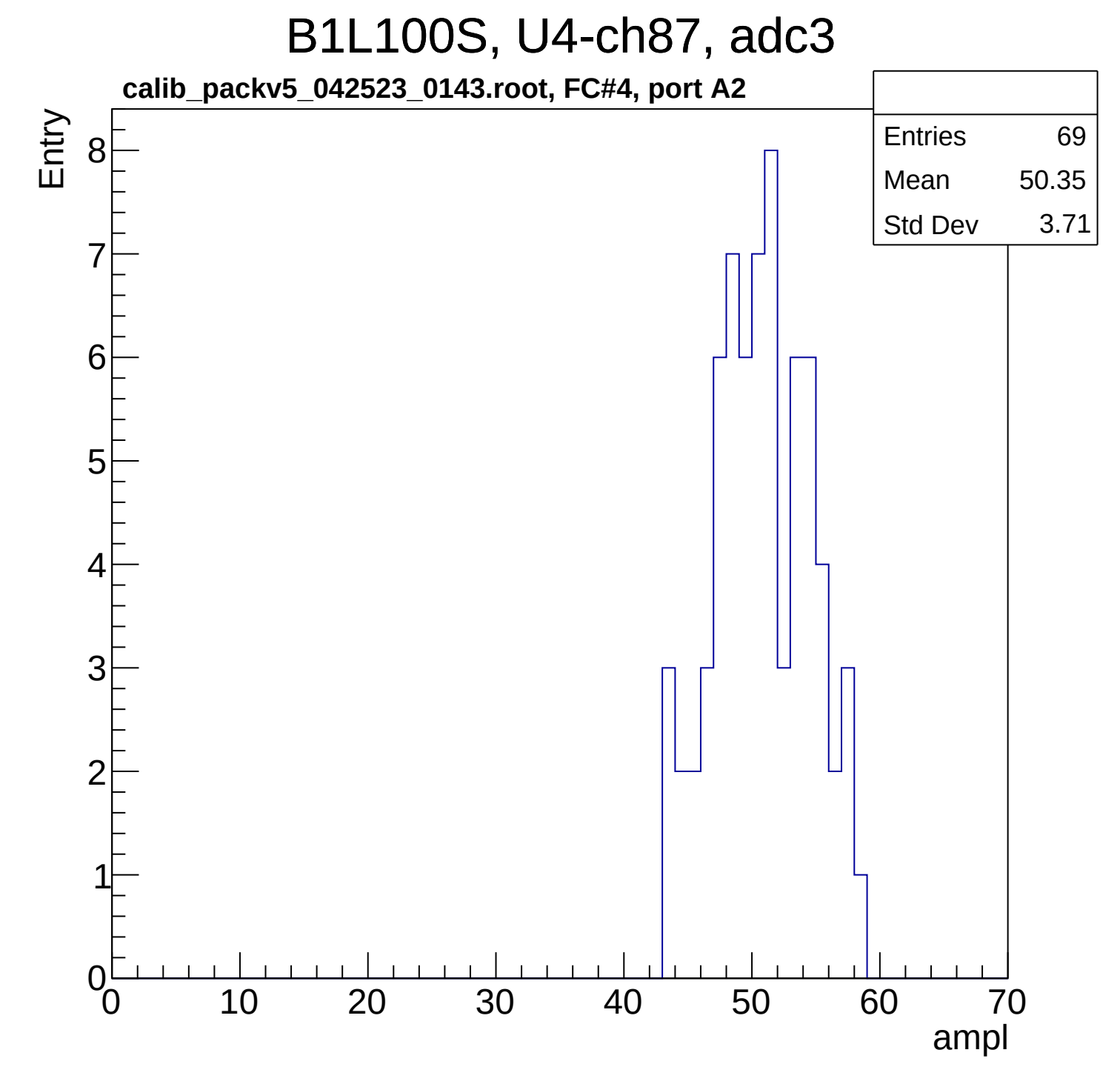

B1L100S, U4-ch86, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 5
Mean 61.6
Std Dev 1.497
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

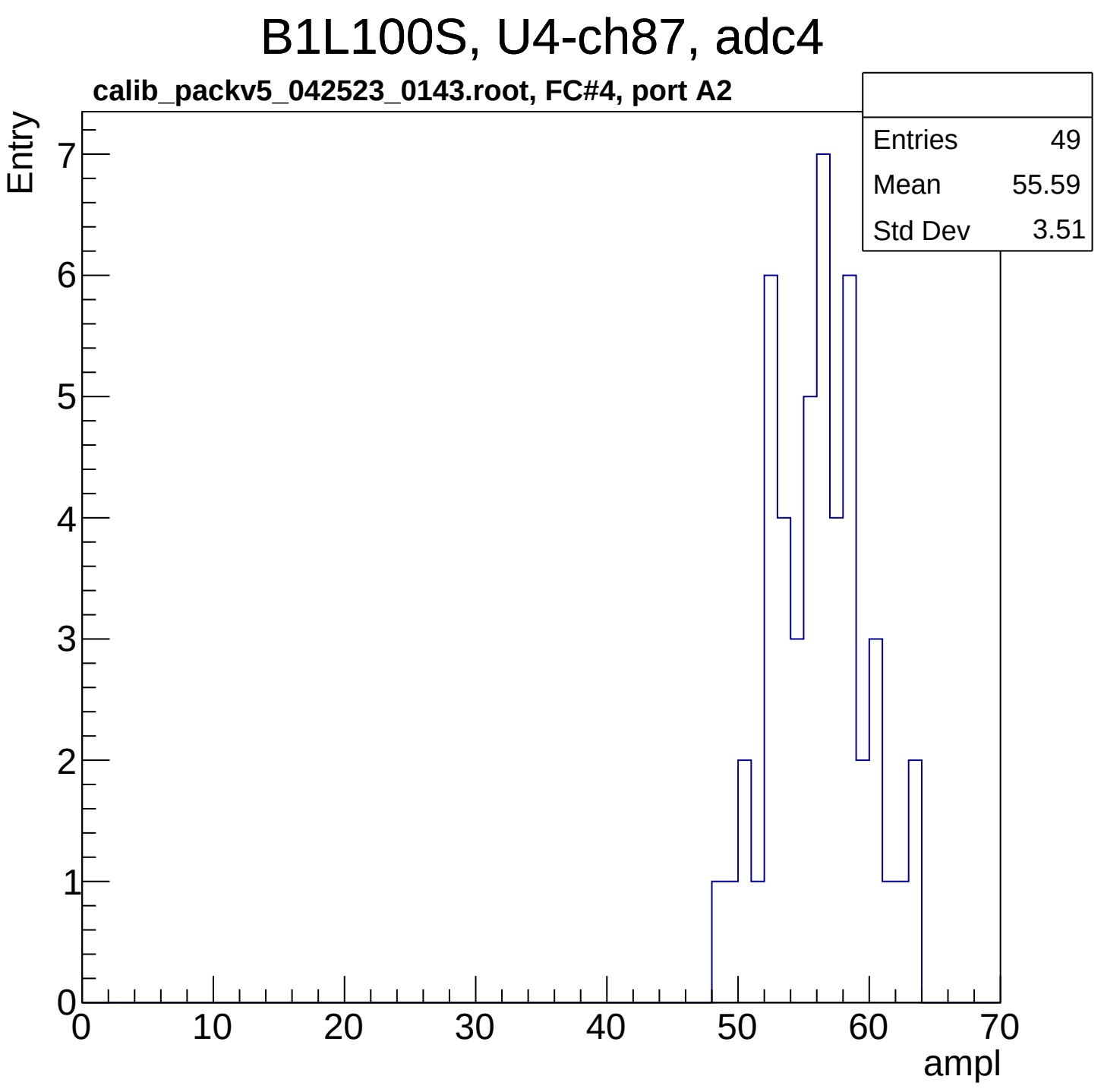

B1L100S, U4-ch86, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

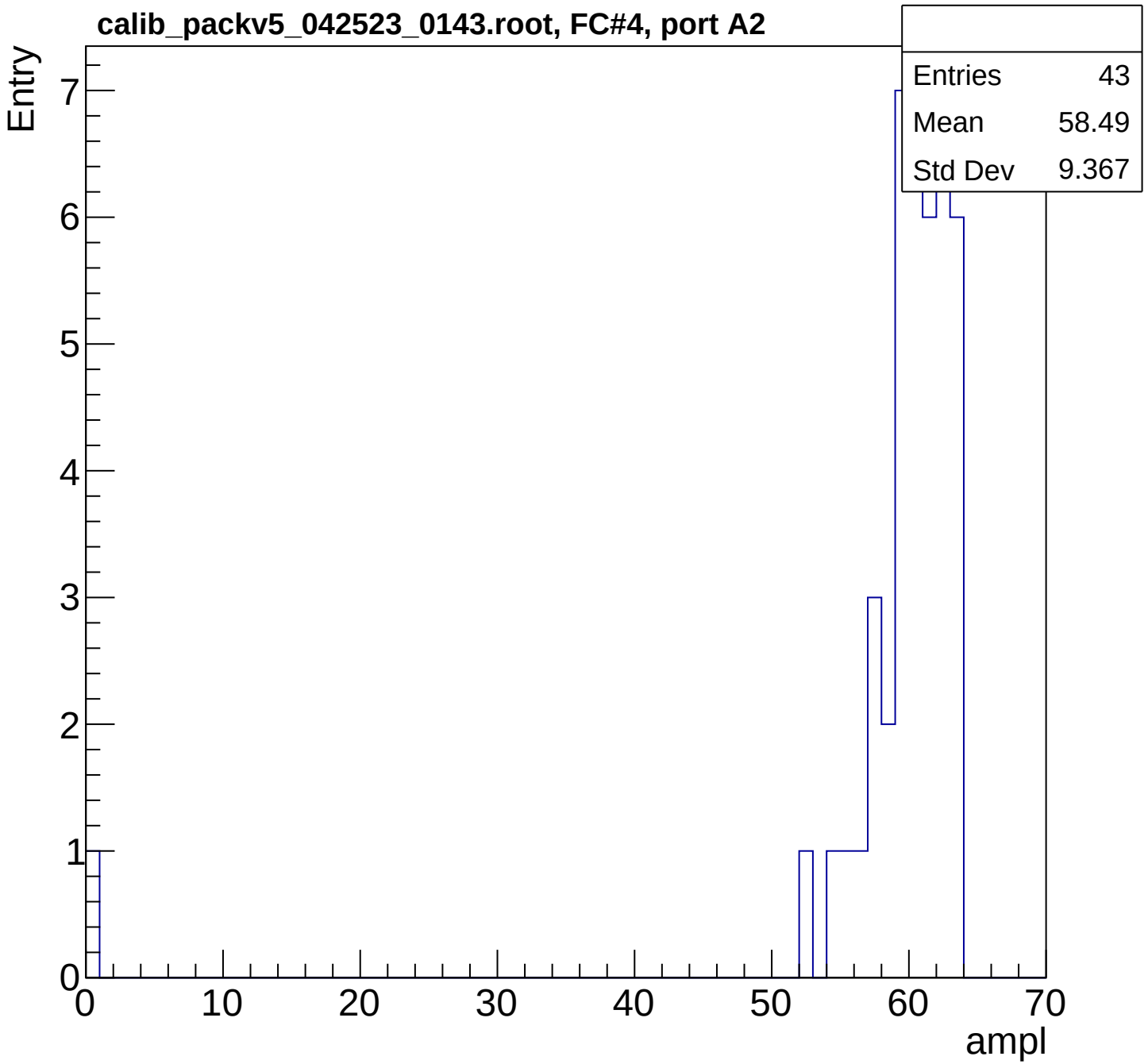

B1L100S, U4-ch87, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 29.32
Std Dev 3.036
Gaus mean : 29.9340
Gaus Width: 3.6205
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

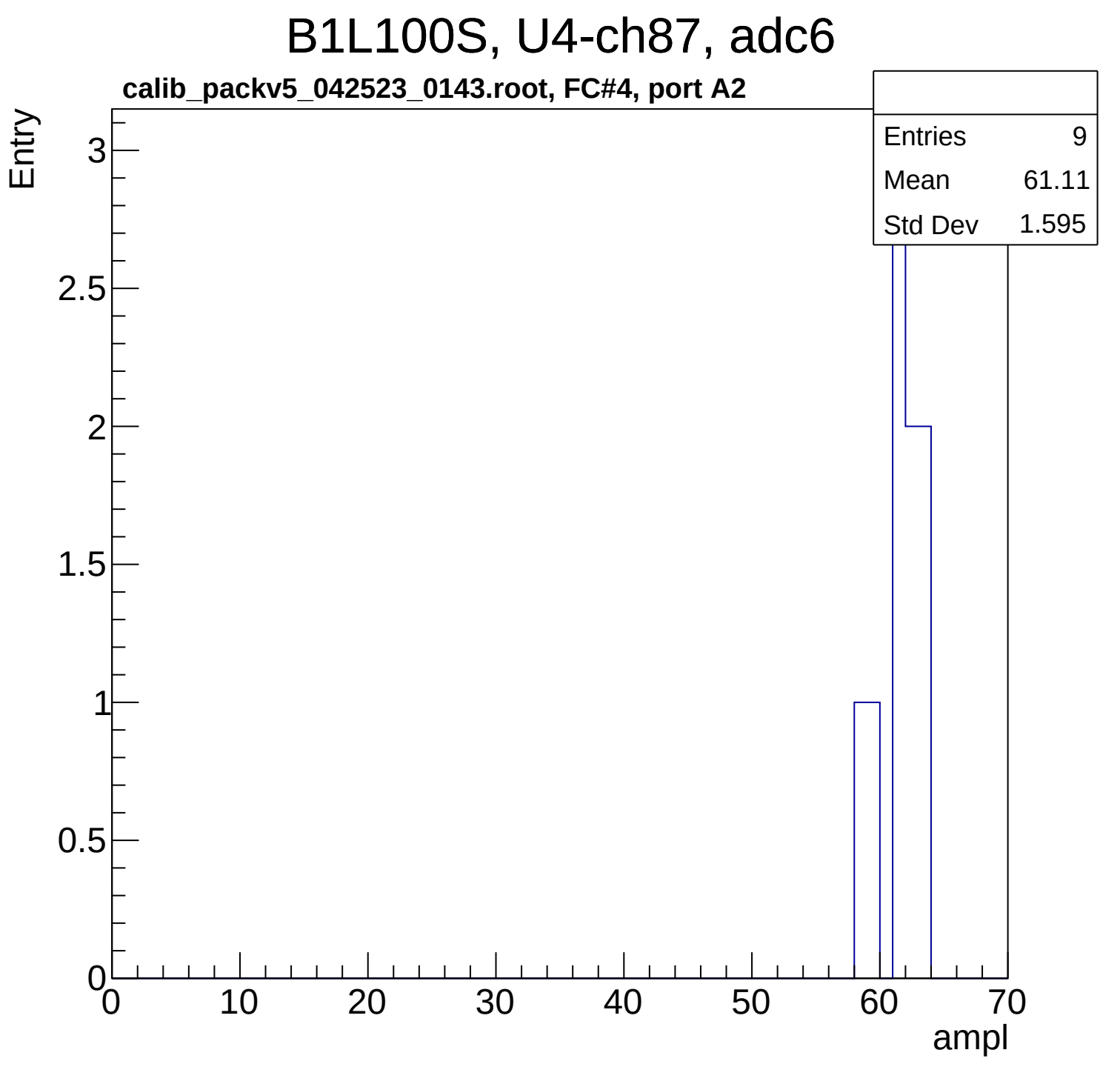

B1L100S, U4-ch87, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 35.91
Std Dev 3.805
Gaus mean : 36.8134
Gaus Width: 4.2047
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

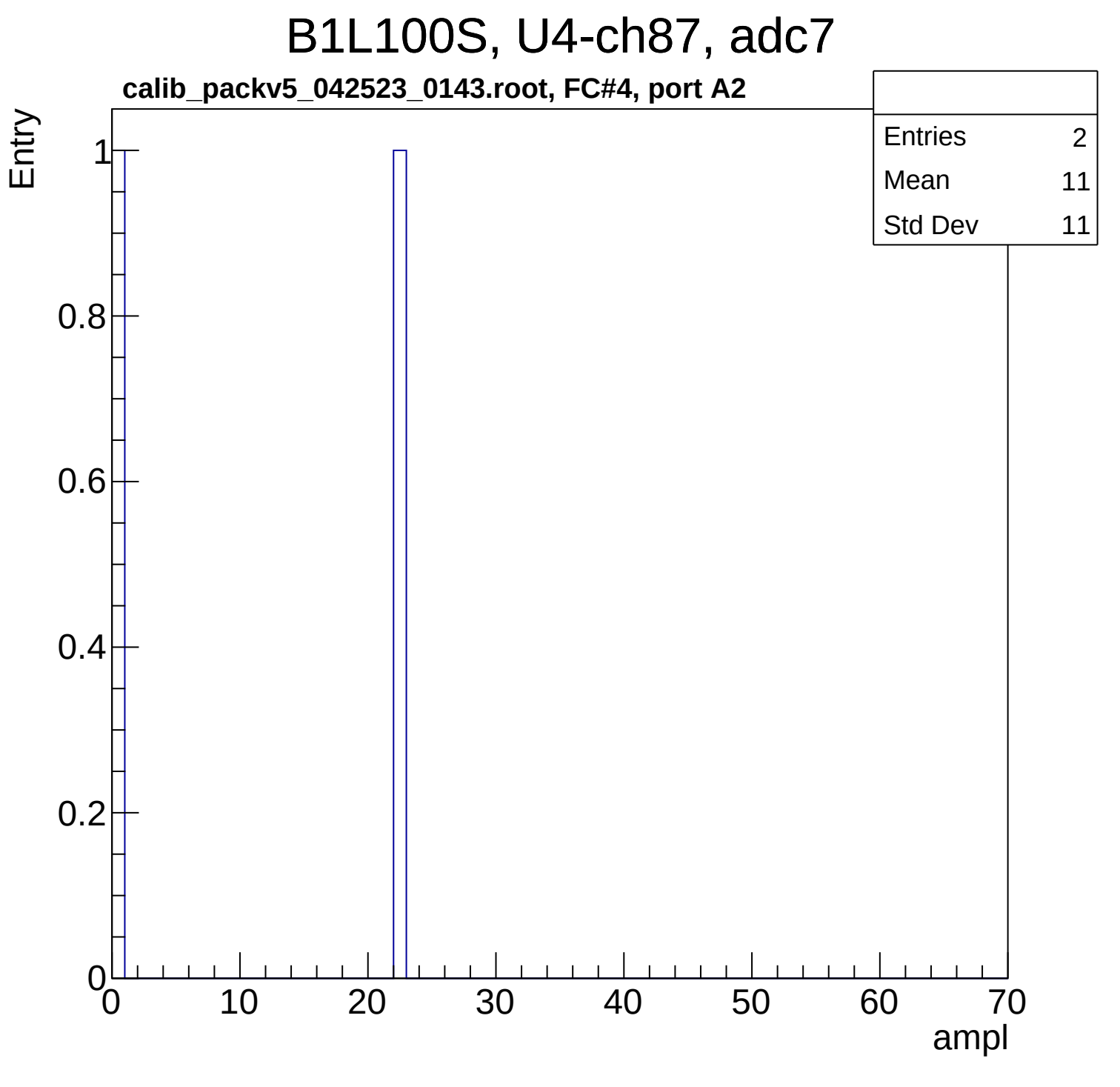

B1L100S, U4-ch87, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 42.24
Std Dev 4.122
Gaus mean : 42.9594
Gaus Width: 4.3258
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

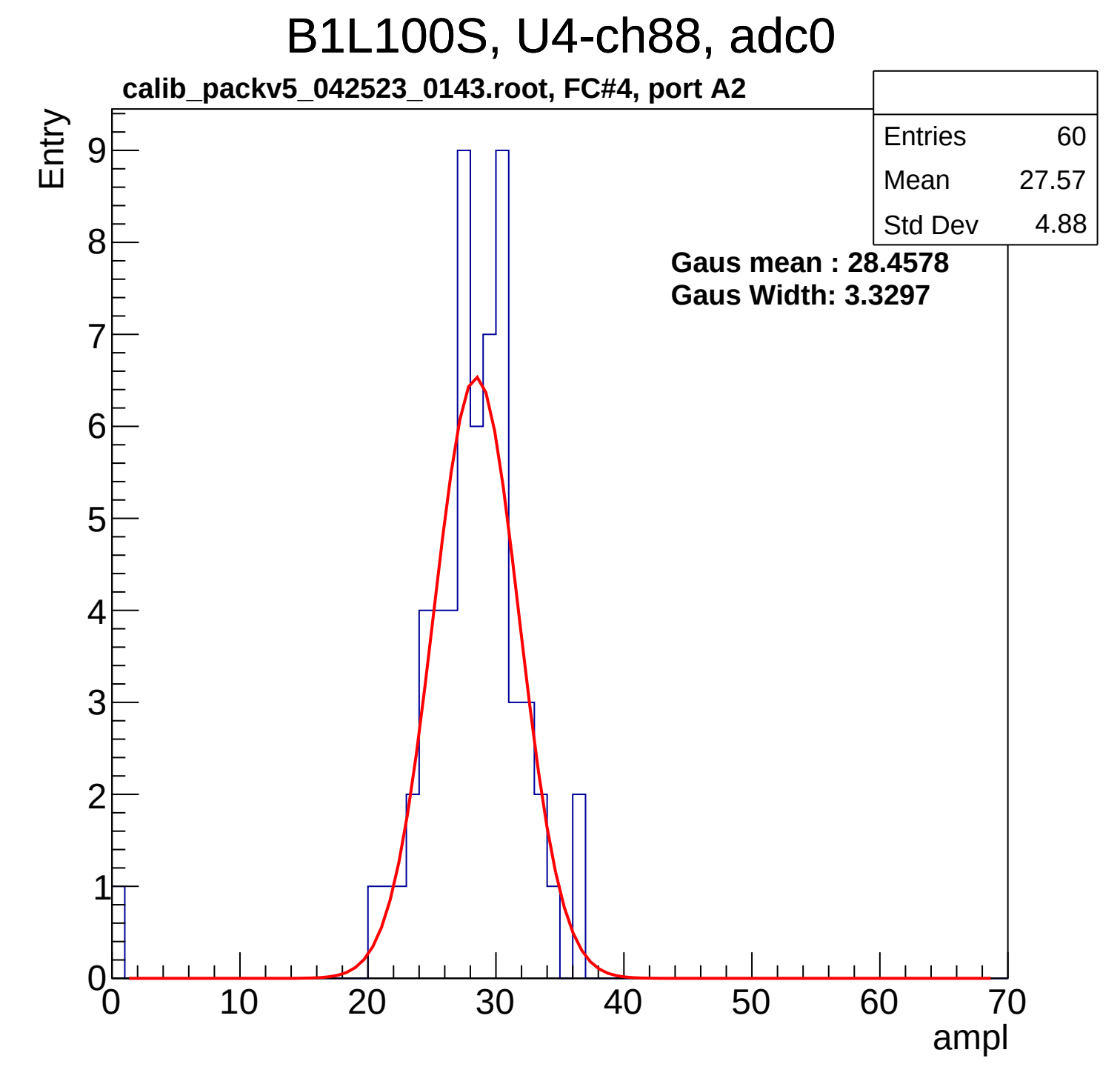

B1L100S, U4-ch87, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 50.35
Std Dev 3.71
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

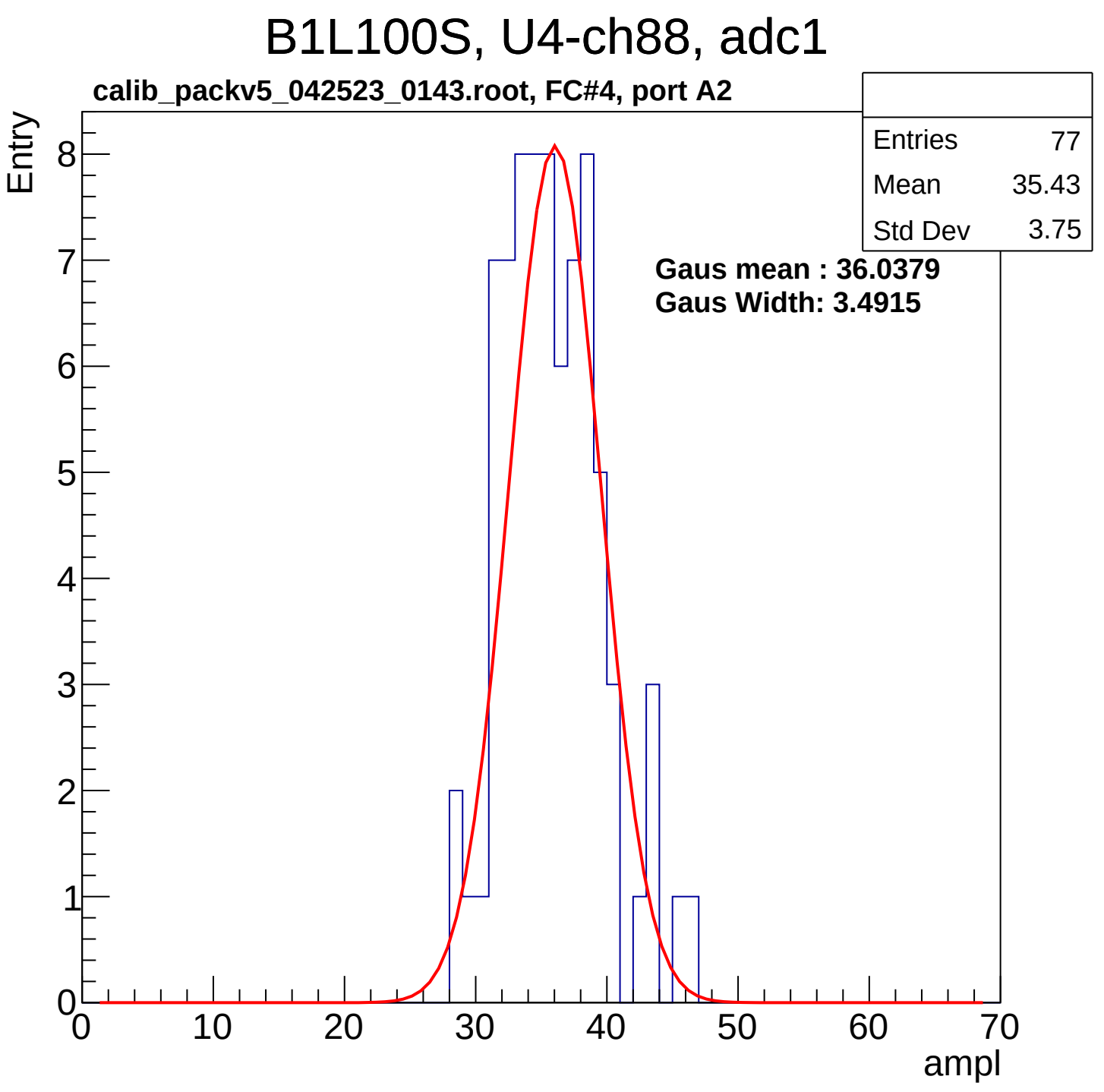

B1L100S, U4-ch87, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 55.59
Std Dev 3.51
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

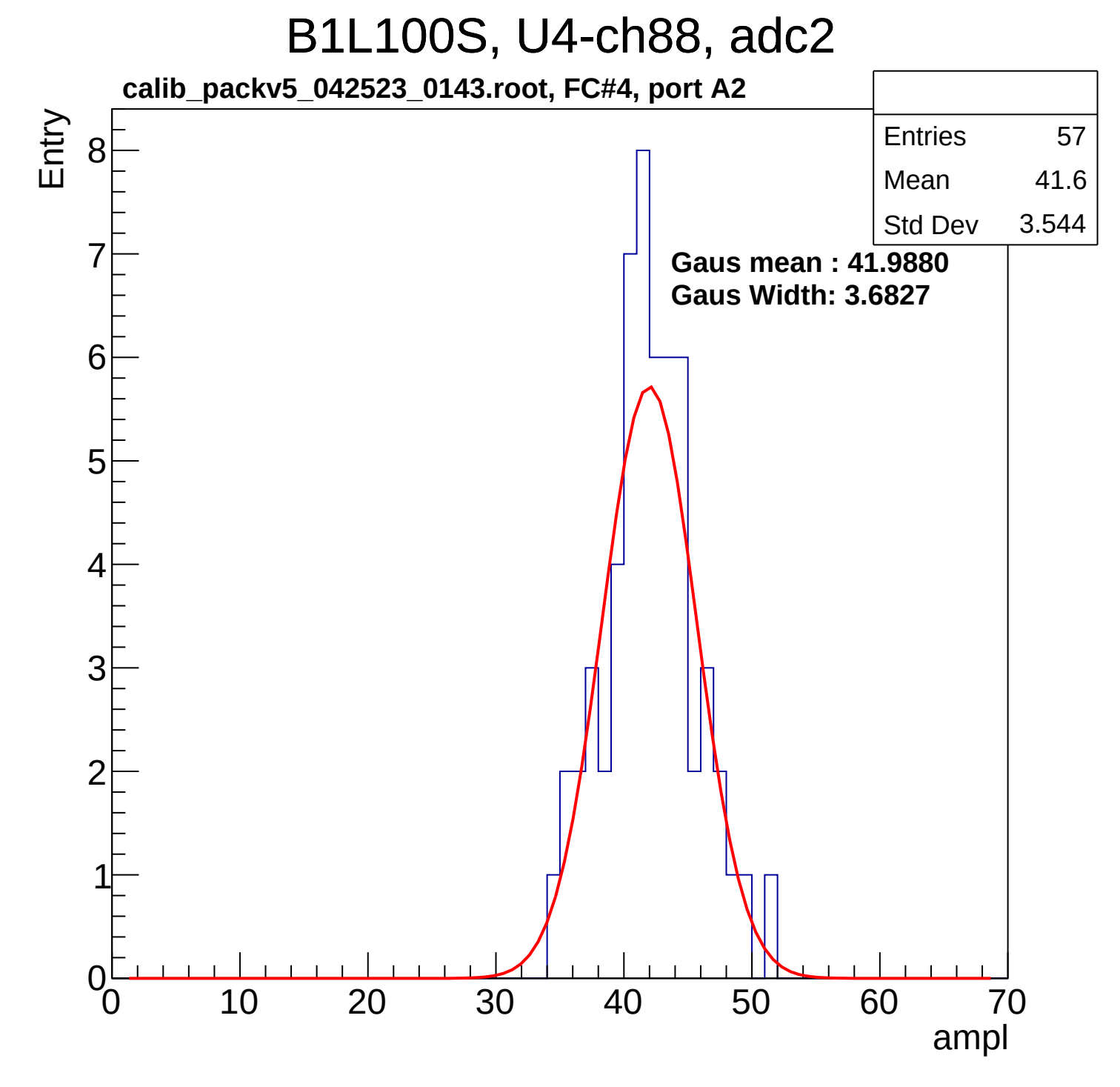

B1L100S, U4-ch87, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 58.49
Std Dev 9.367
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

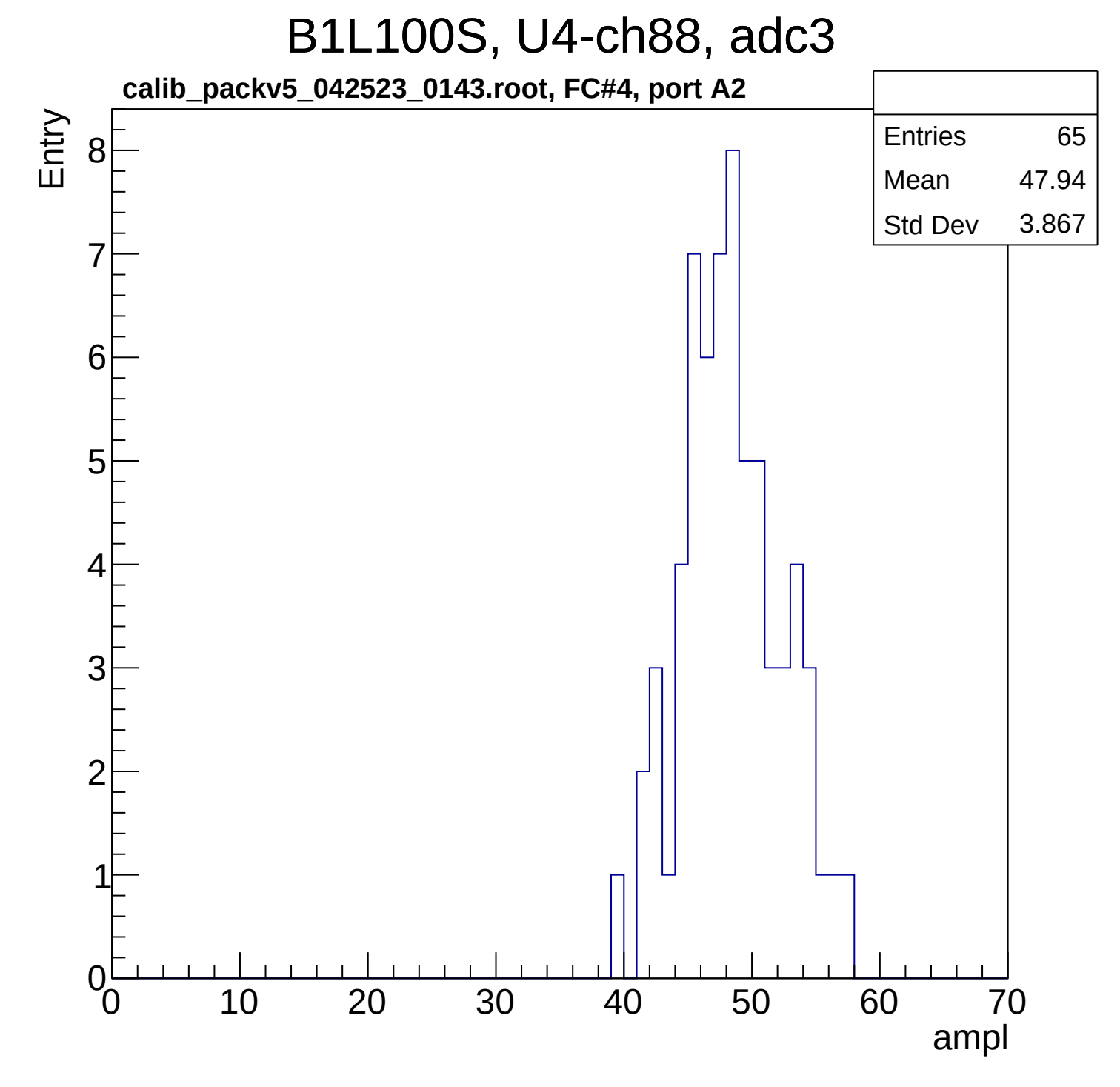

B1L100S, U4-ch87, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 61.11
Std Dev 1.595
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

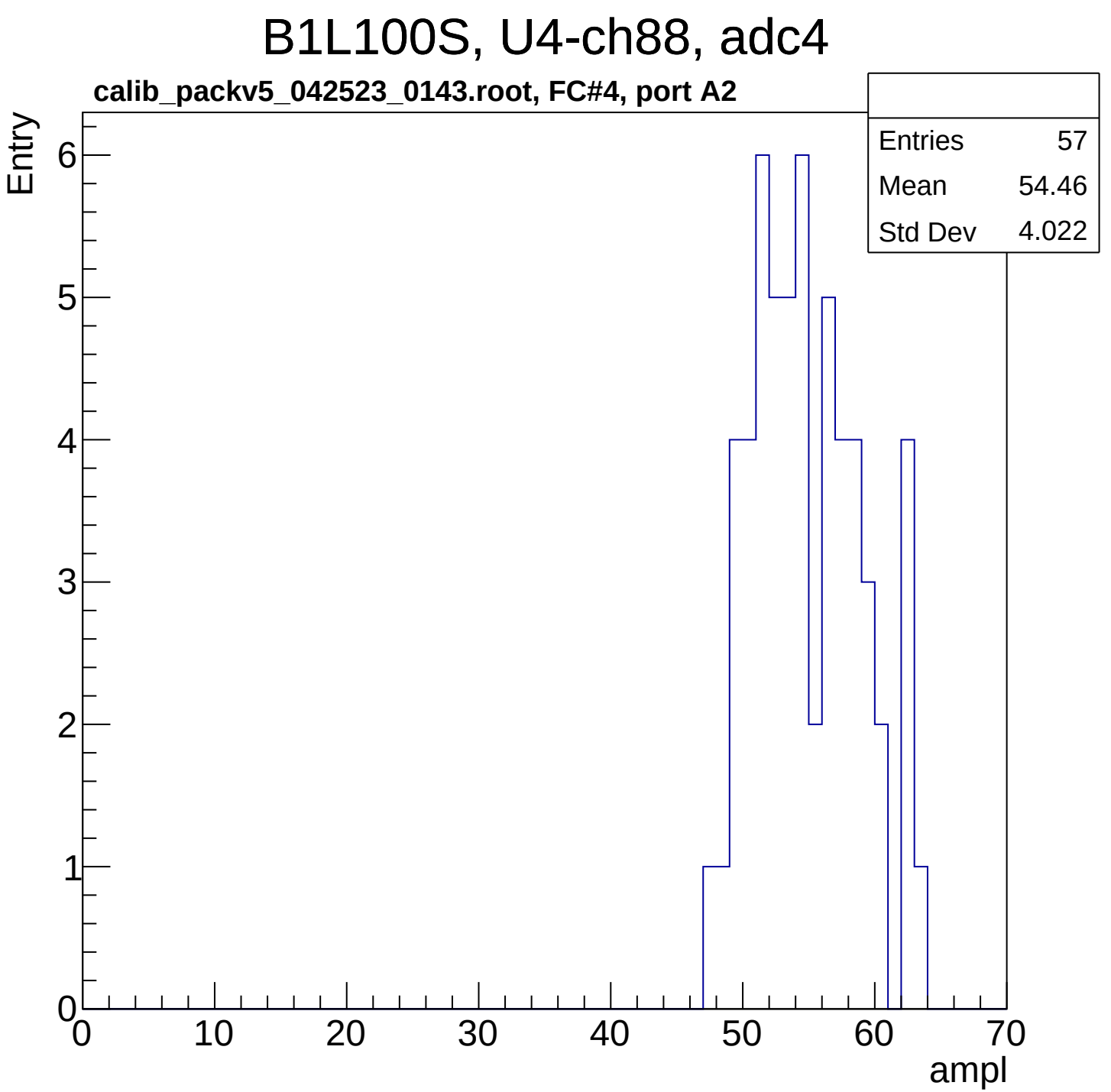

B1L100S, U4-ch87, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 11
Std Dev 11
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

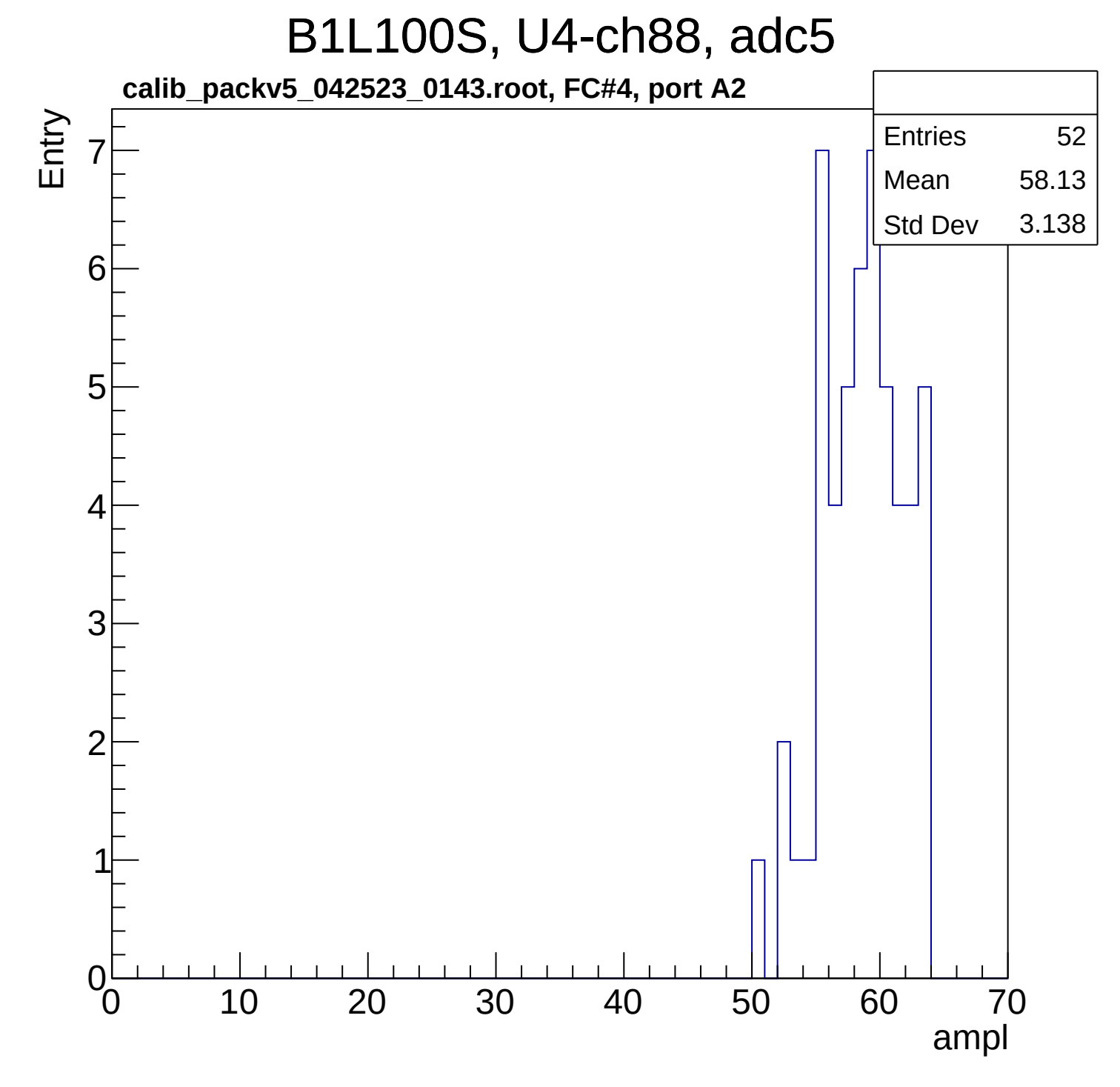

B1L100S, U4-ch88, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 27.57
Std Dev 4.88
Gaus mean : 28.4578
Gaus Width: 3.3297
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

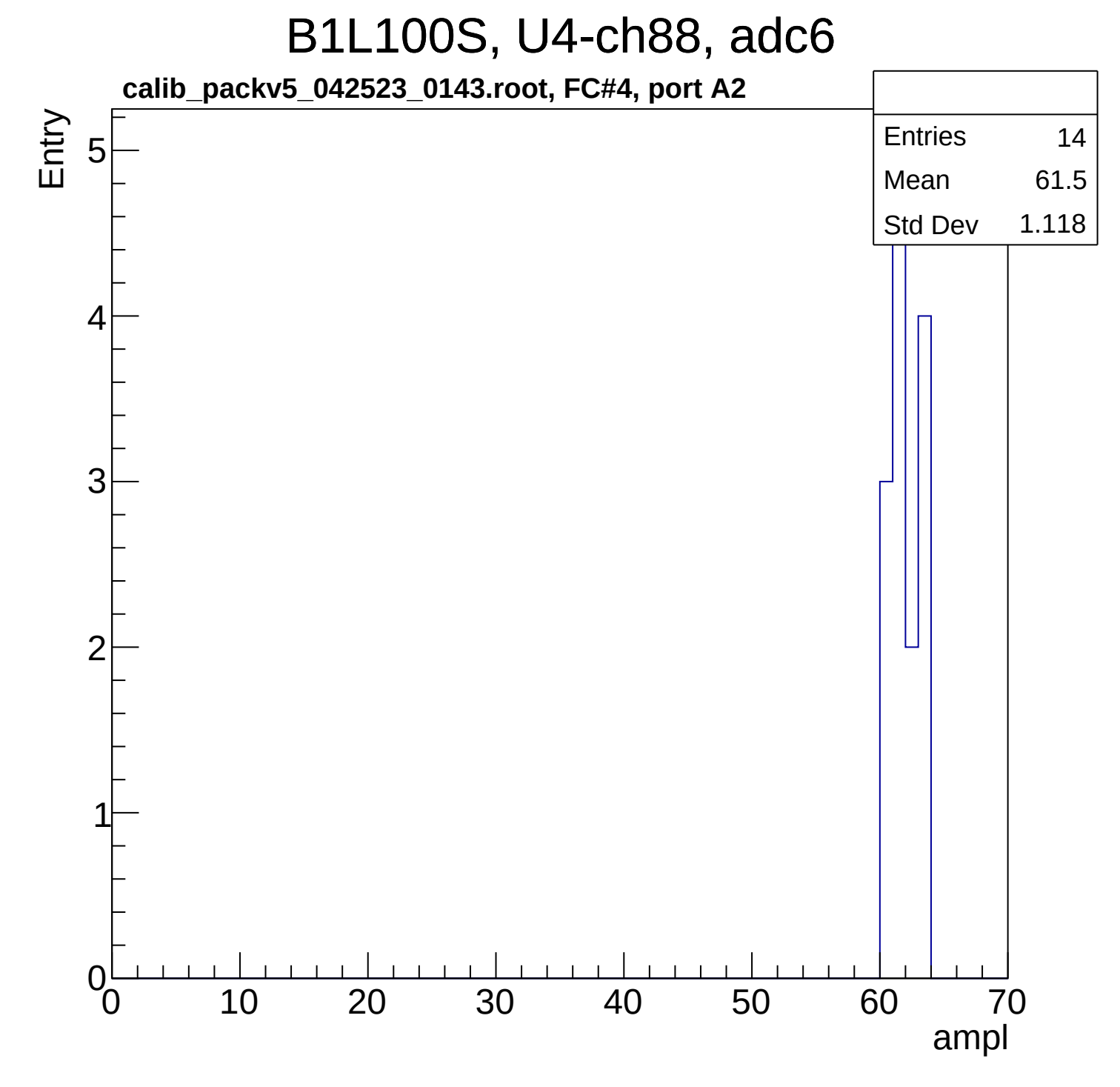

B1L100S, U4-ch88, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 35.43
Std Dev 3.75
Gaus mean : 36.0379
Gaus Width: 3.4915
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

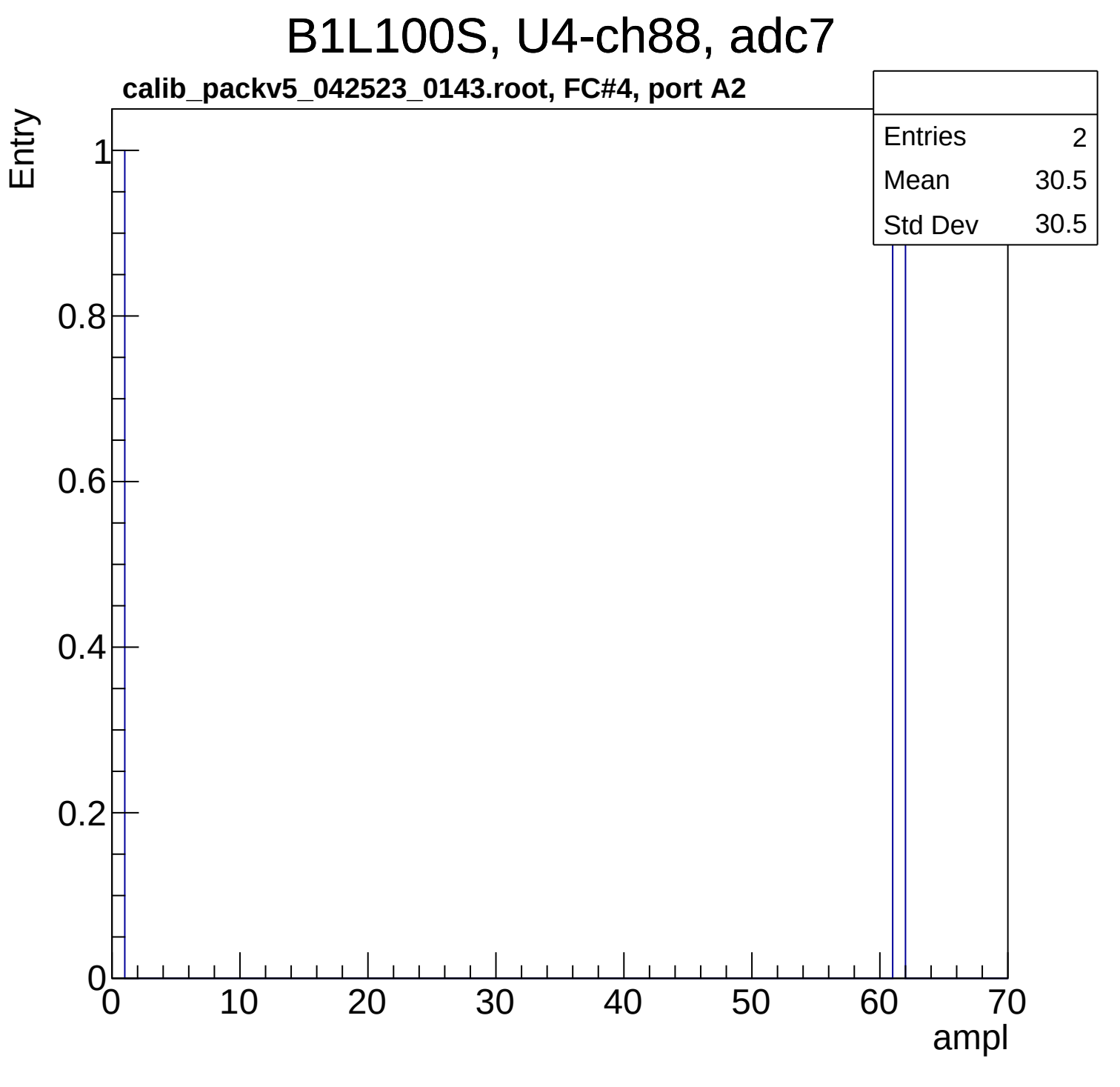

B1L100S, U4-ch88, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 41.6
Std Dev 3.544
Gaus mean : 41.9880
Gaus Width: 3.6827
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

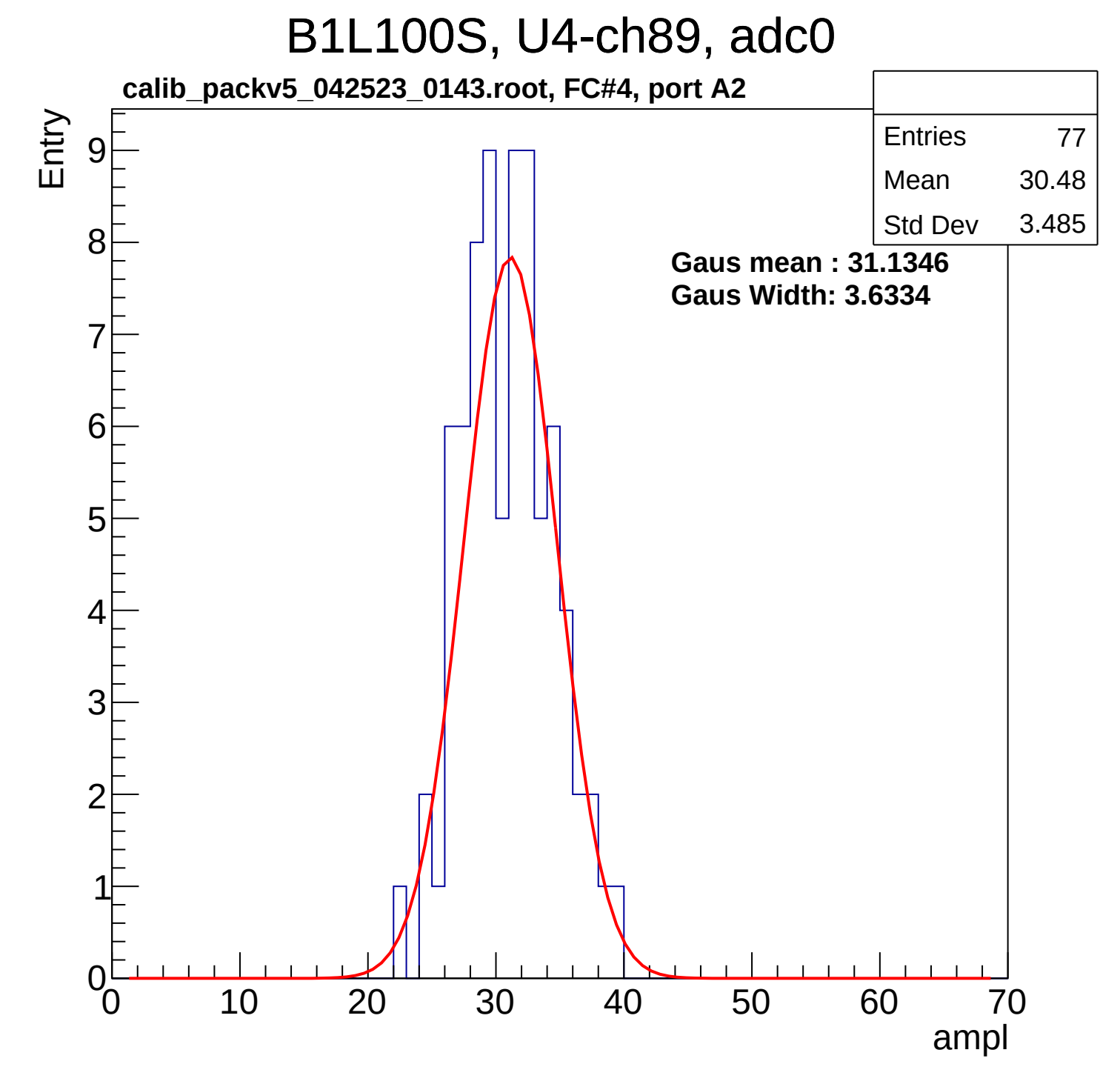

B1L100S, U4-ch88, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 47.94
Std Dev 3.867
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

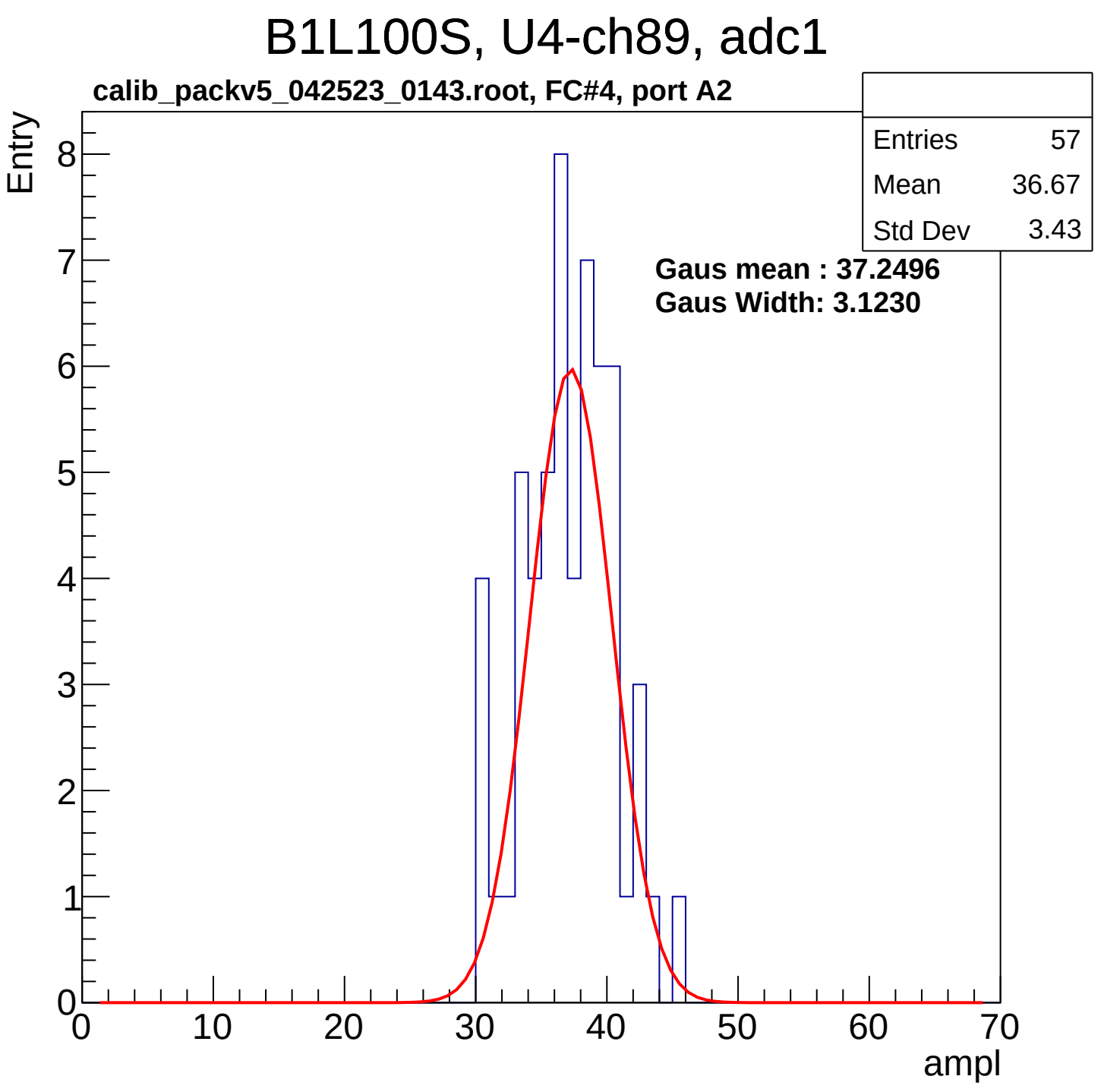

B1L100S, U4-ch88, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 54.46
Std Dev 4.022
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

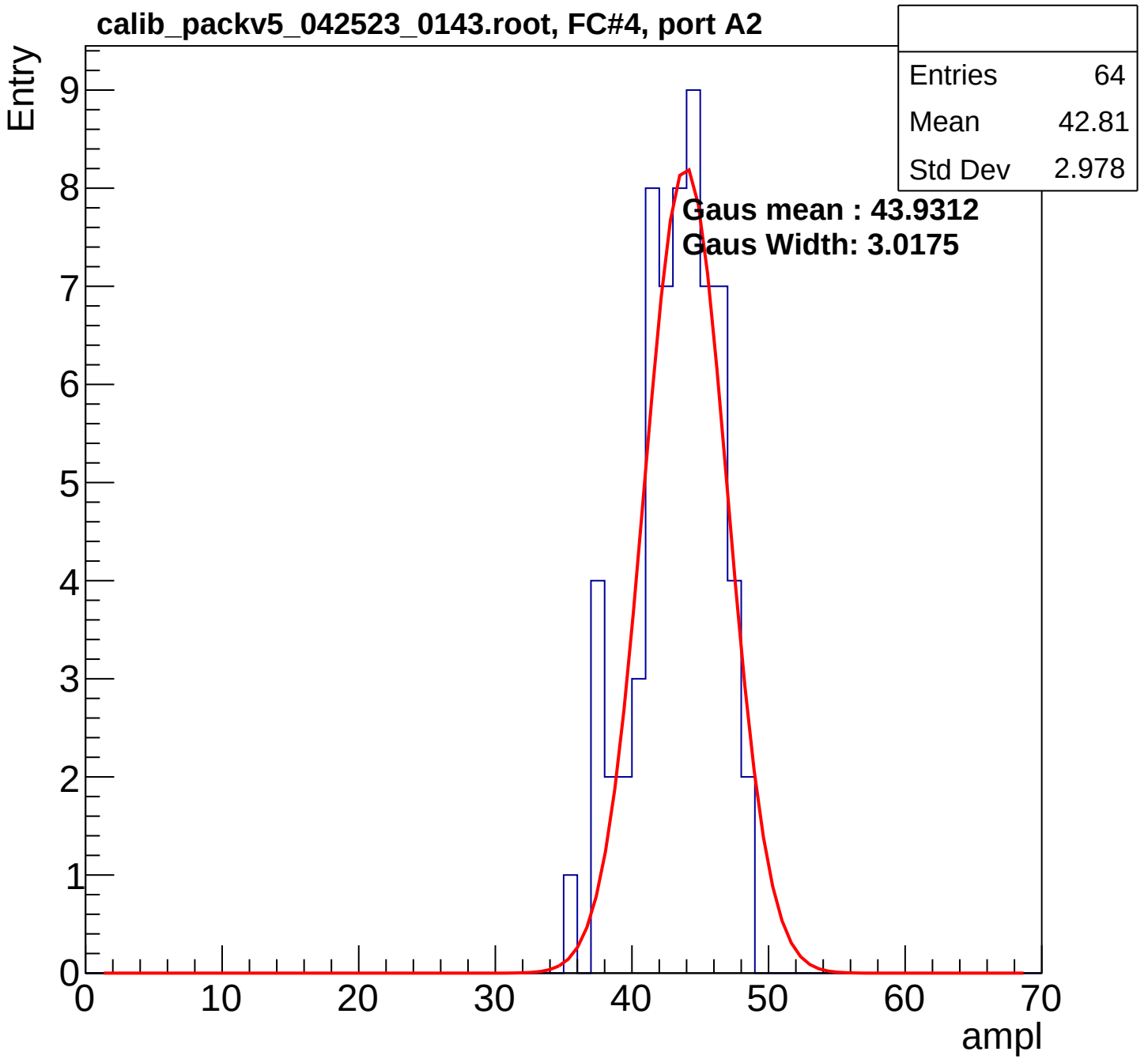

B1L100S, U4-ch88, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 58.13
Std Dev 3.138
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

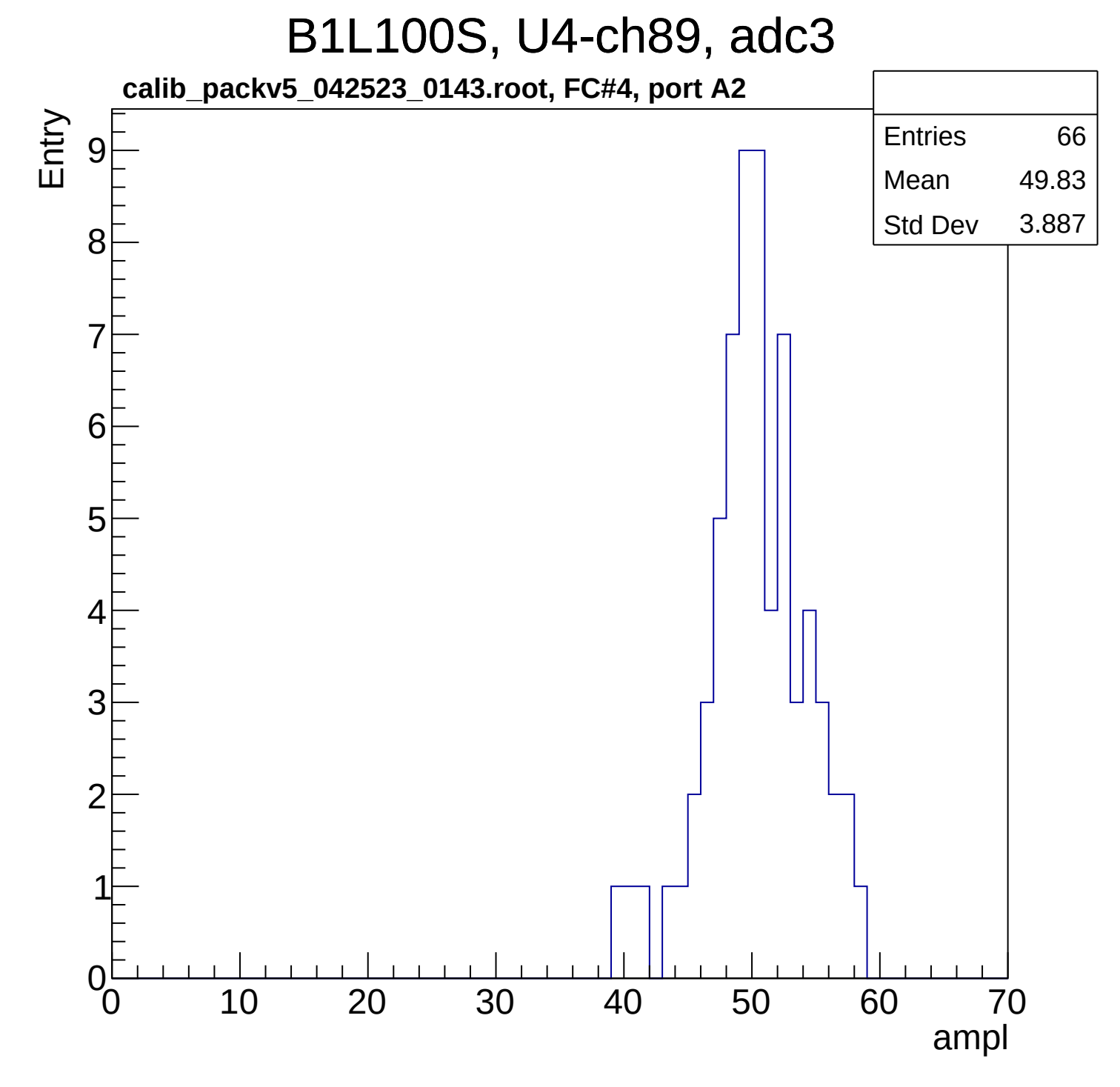

B1L100S, U4-ch88, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 14
Mean 61.5
Std Dev 1.118
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

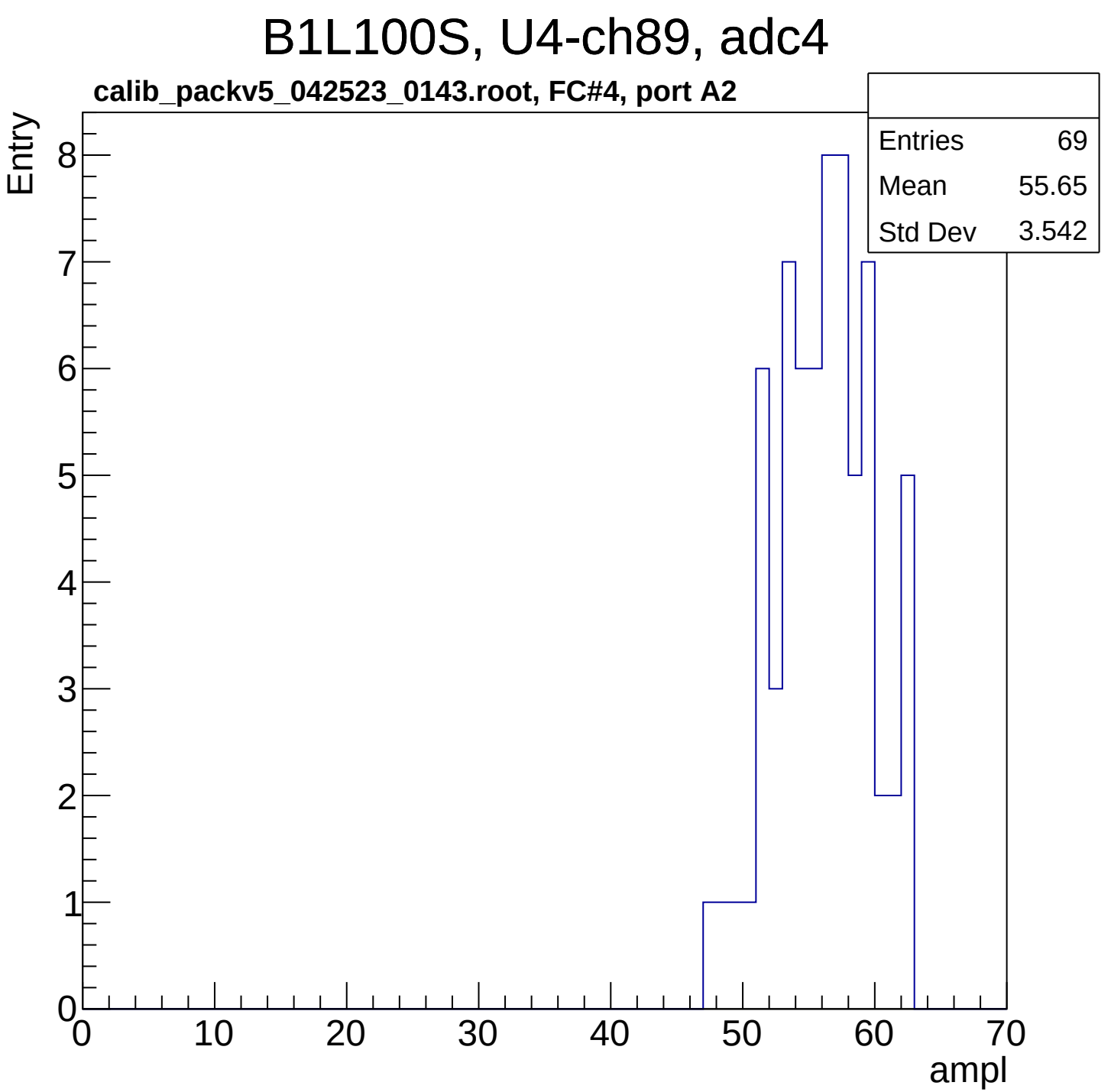

B1L100S, U4-ch88, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 30.5
Std Dev 30.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

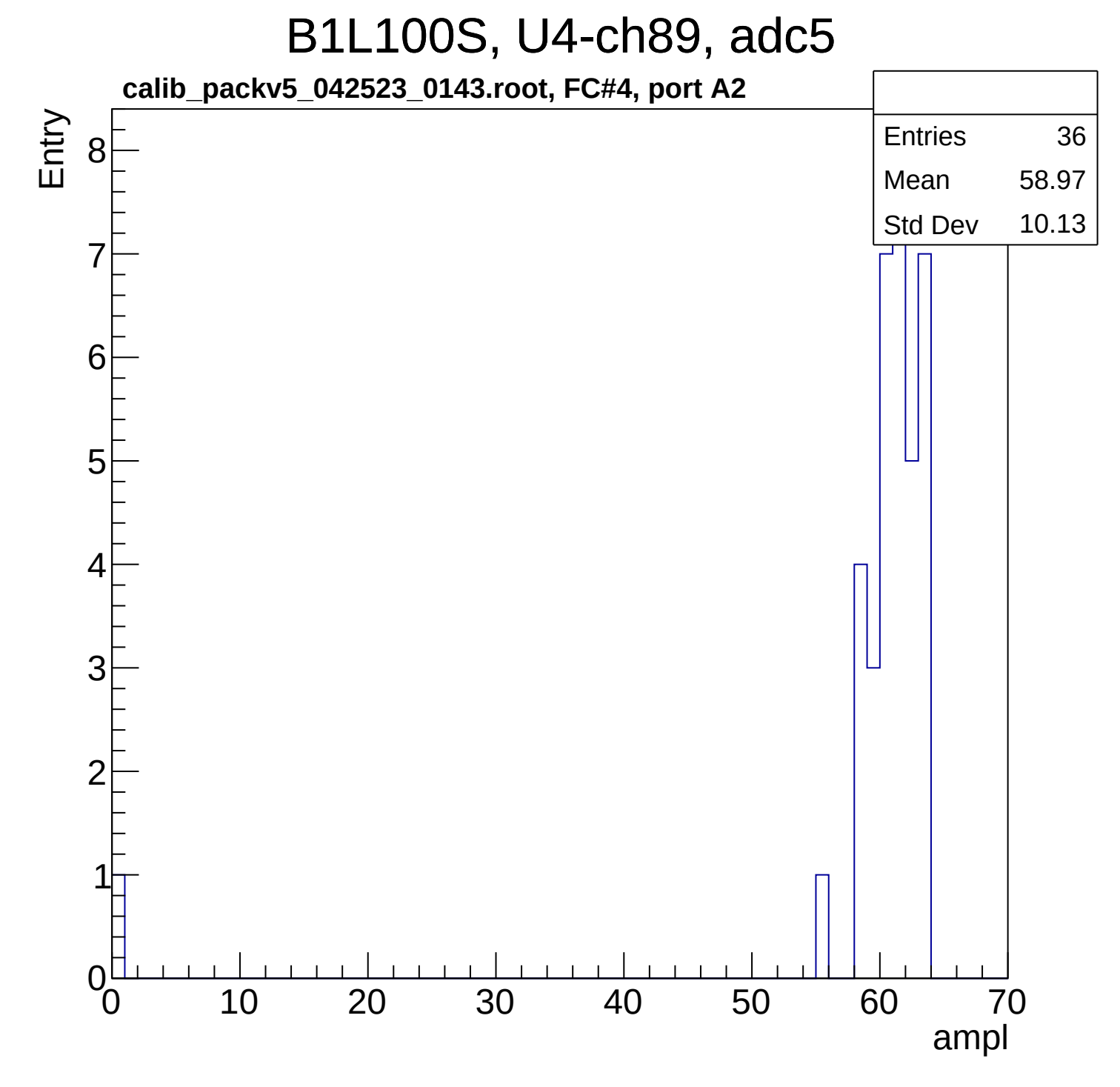

B1L100S, U4-ch89, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 30.48
Std Dev 3.485
Gaus mean : 31.1346
Gaus Width: 3.6334
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

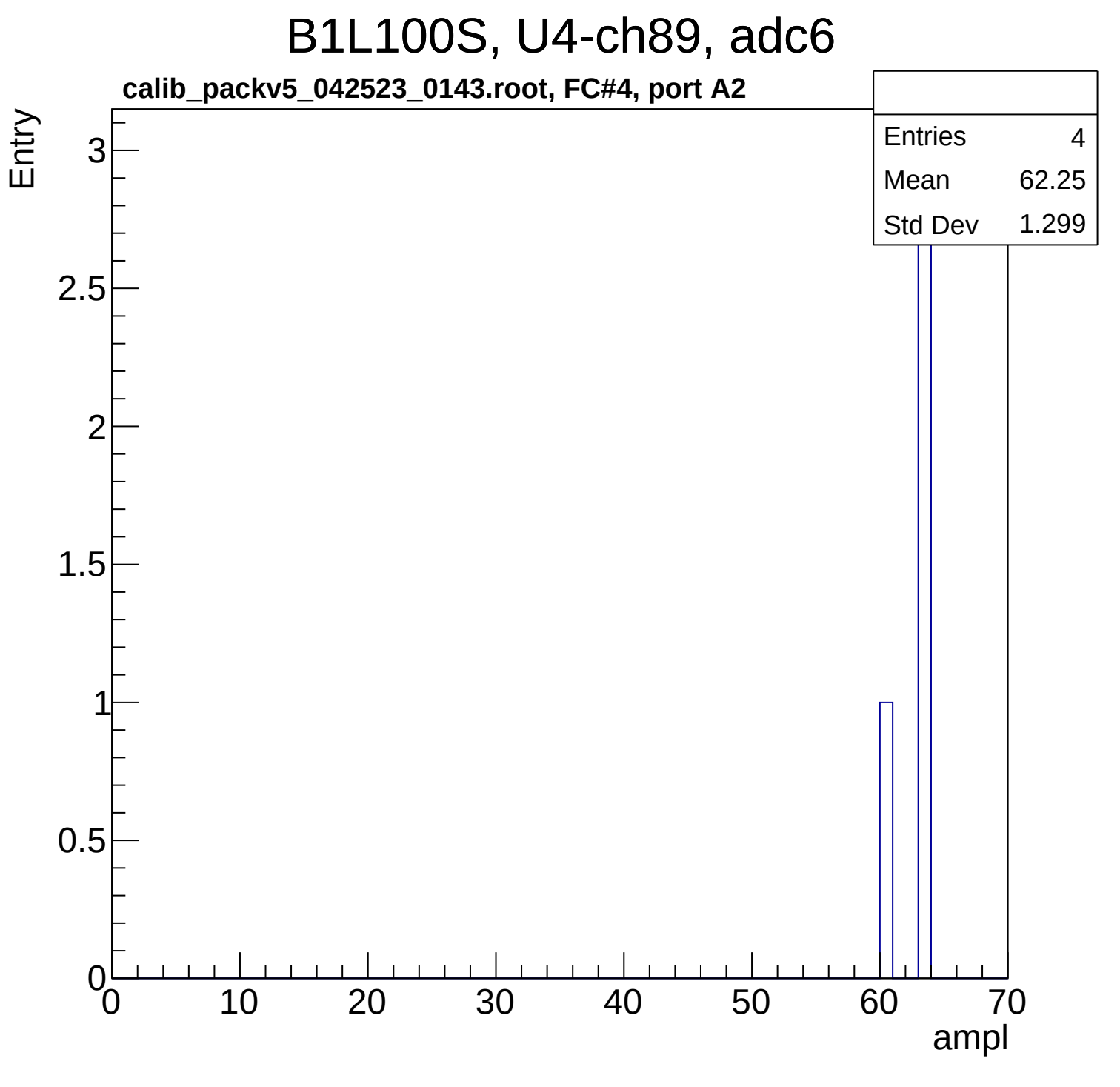

B1L100S, U4-ch89, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 36.67
Std Dev 3.43
Gaus mean : 37.2496
Gaus Width: 3.1230
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

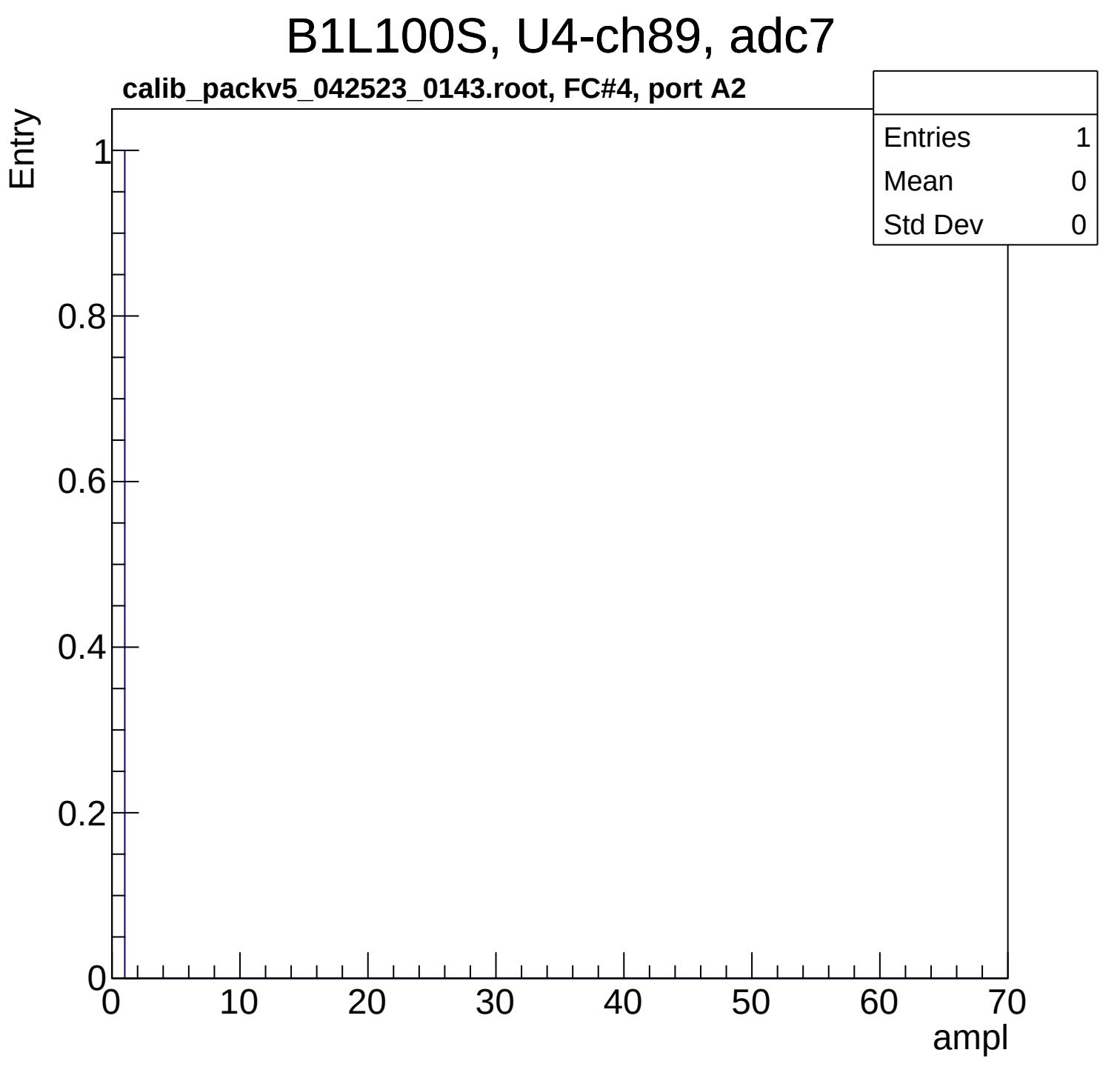

B1L100S, U4-ch89, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 42.81
Std Dev 2.978
Gaus mean : 43.9312
Gaus Width: 3.0175
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

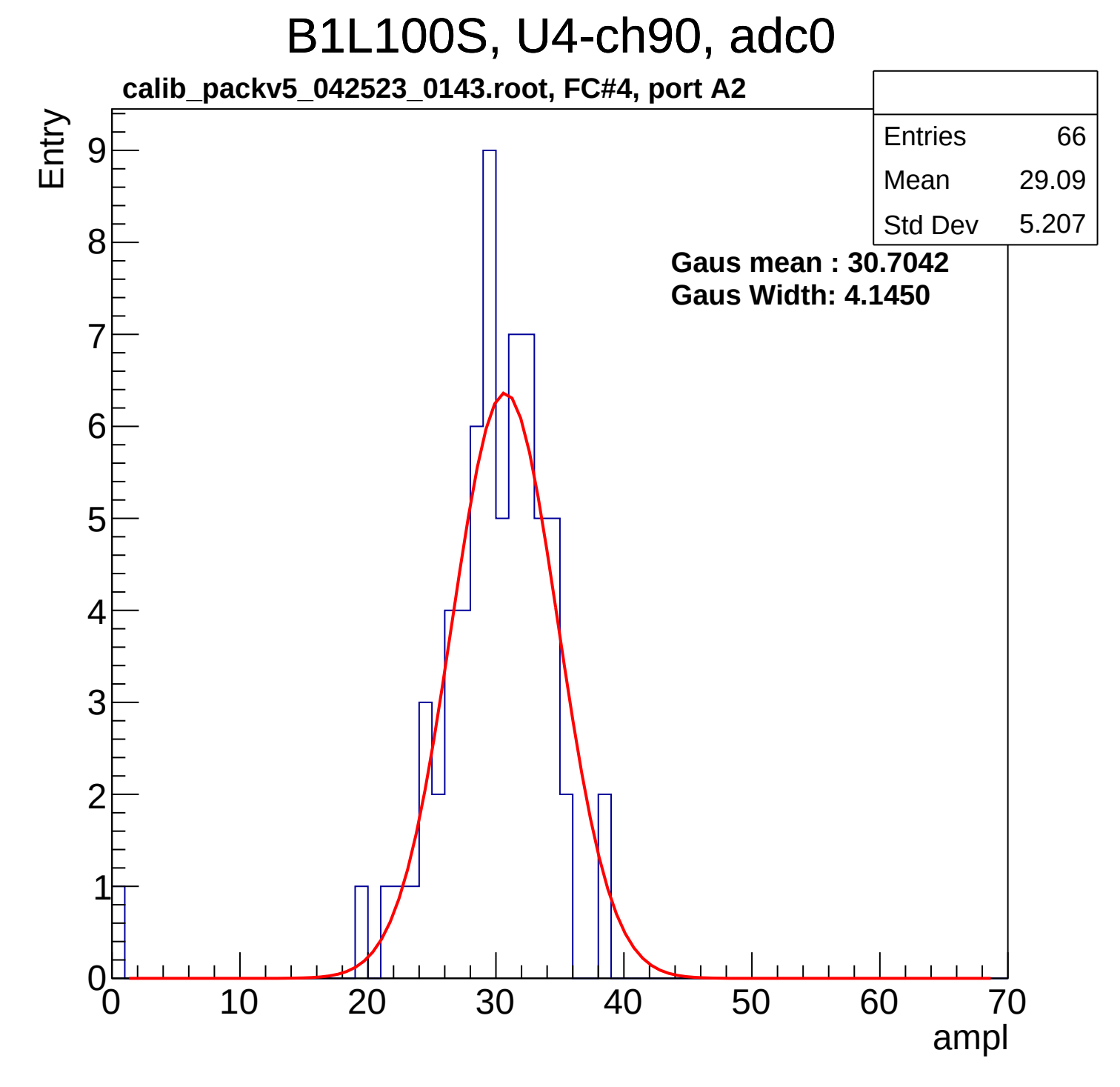

B1L100S, U4-ch89, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 49.83
Std Dev 3.887
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

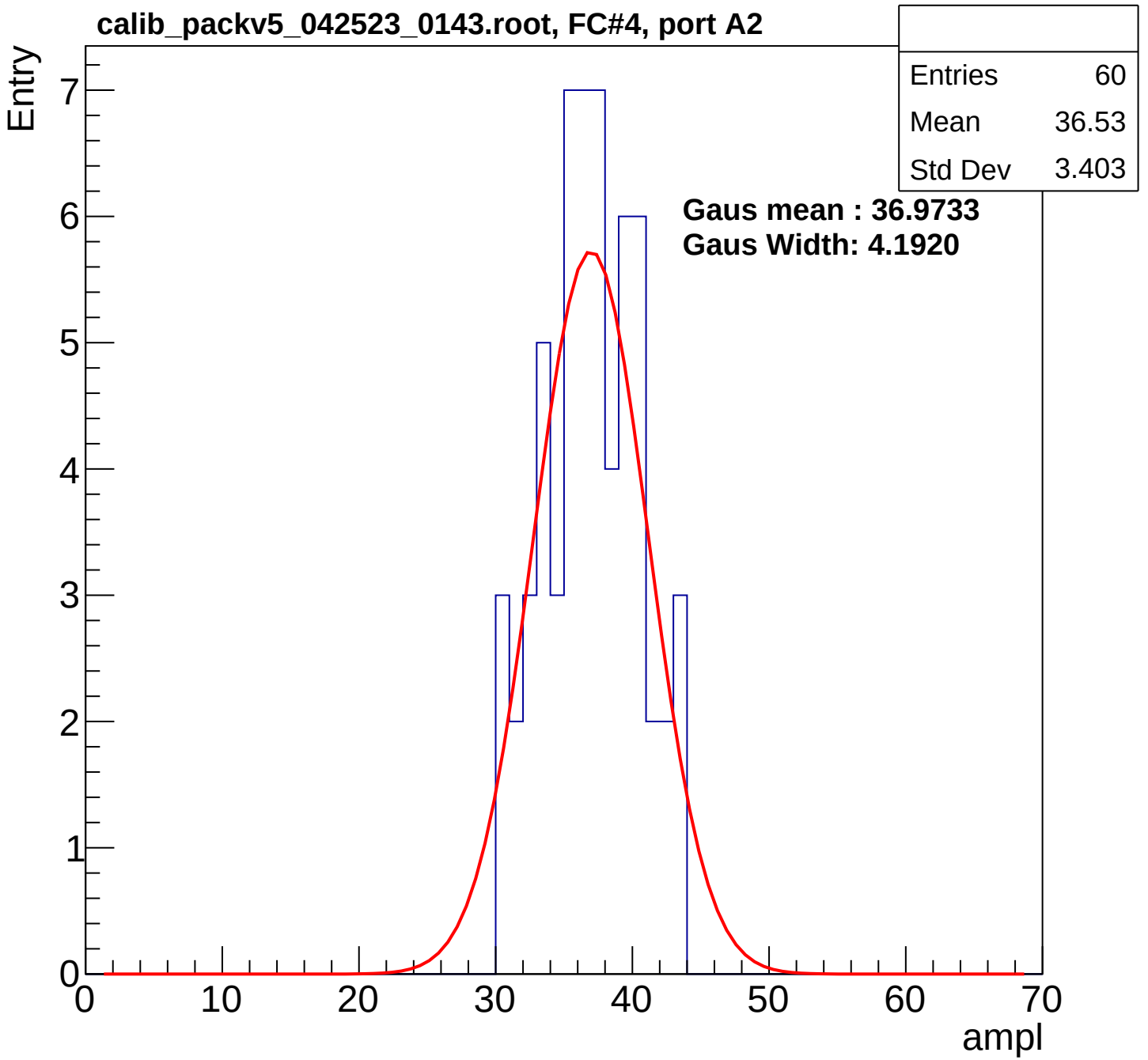

B1L100S, U4-ch89, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 55.65
Std Dev 3.542
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

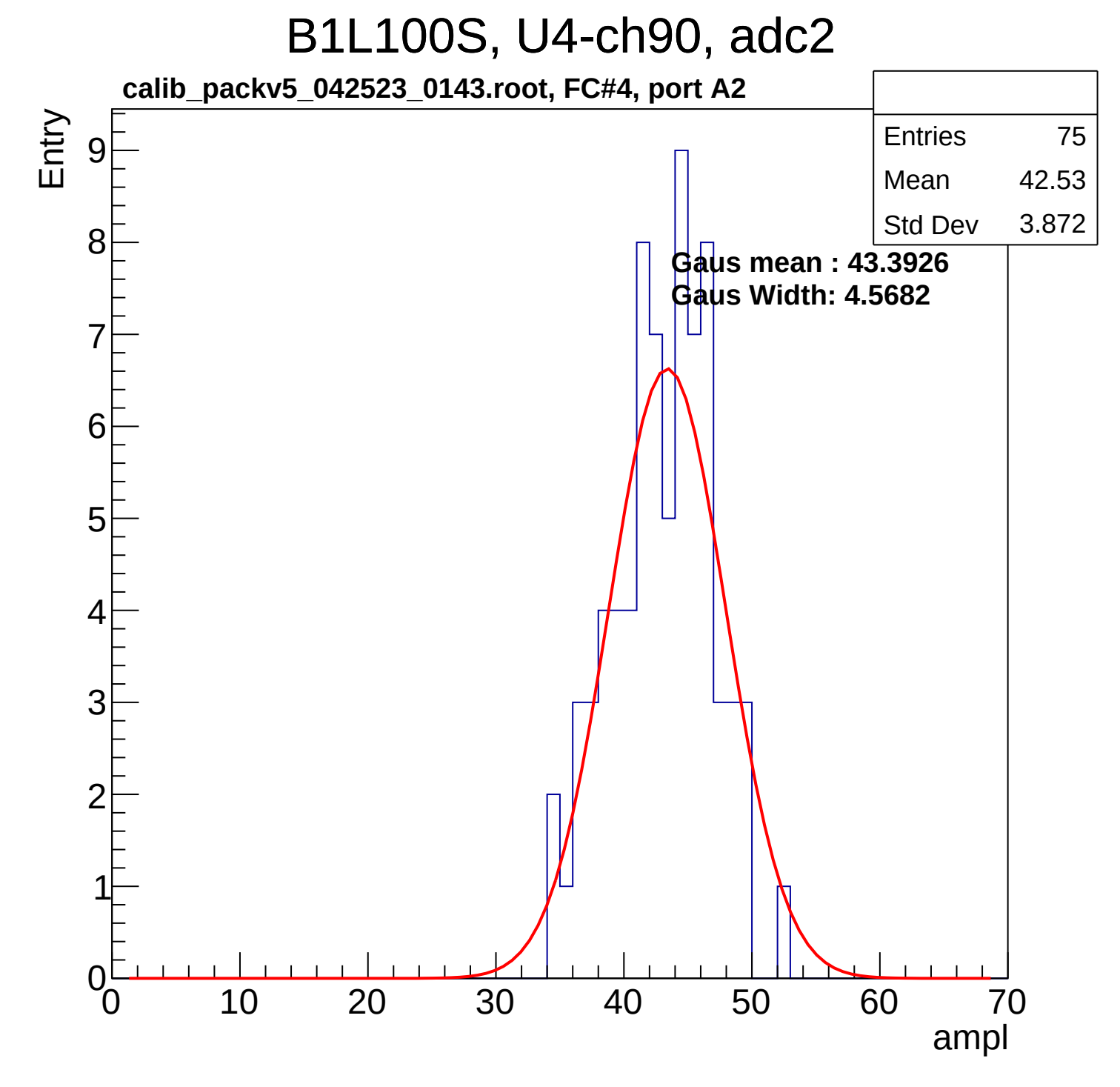

B1L100S, U4-ch89, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 36
Mean 58.97
Std Dev 10.13
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

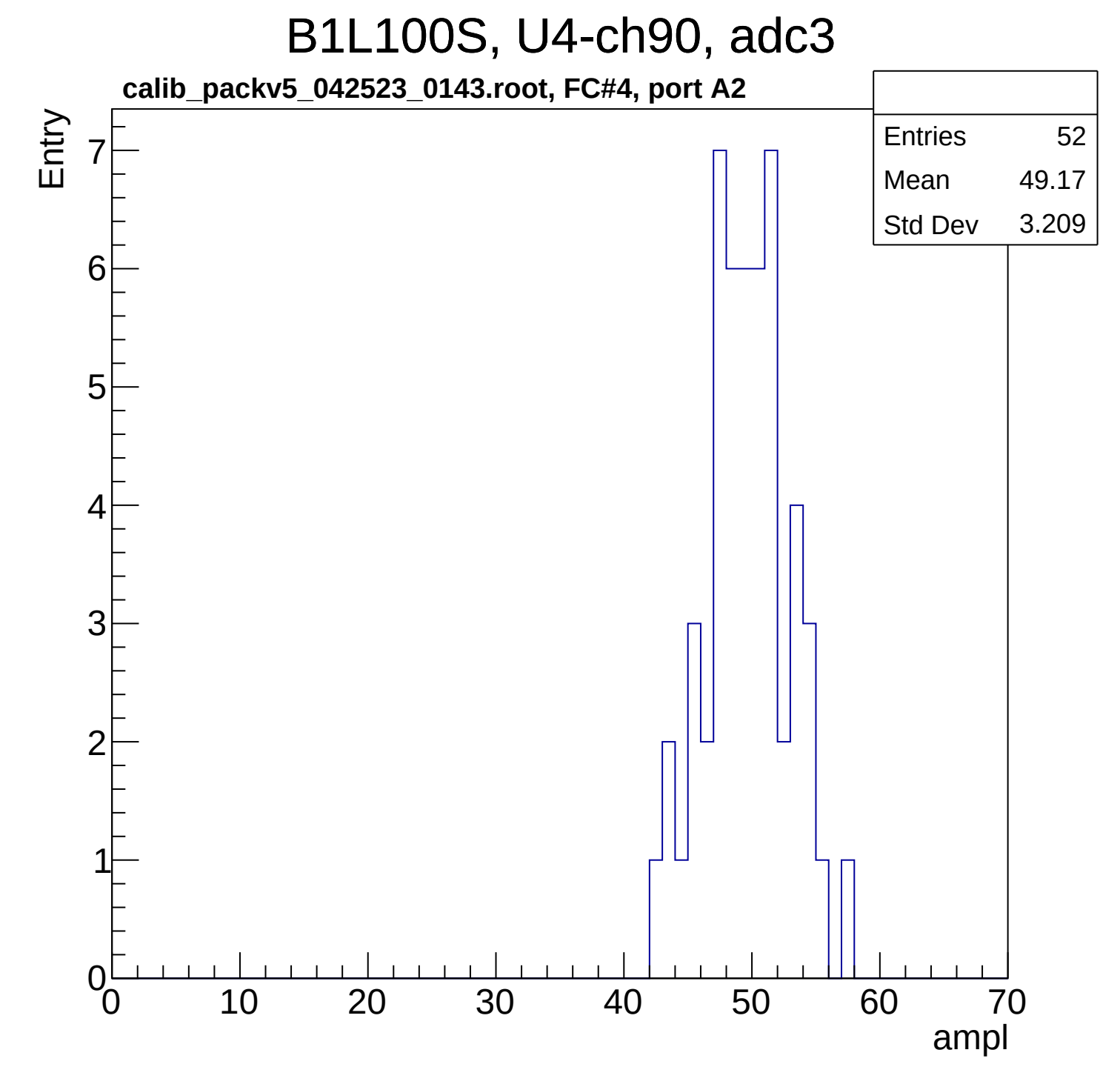

B1L100S, U4-ch89, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 62.25
Std Dev 1.299
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

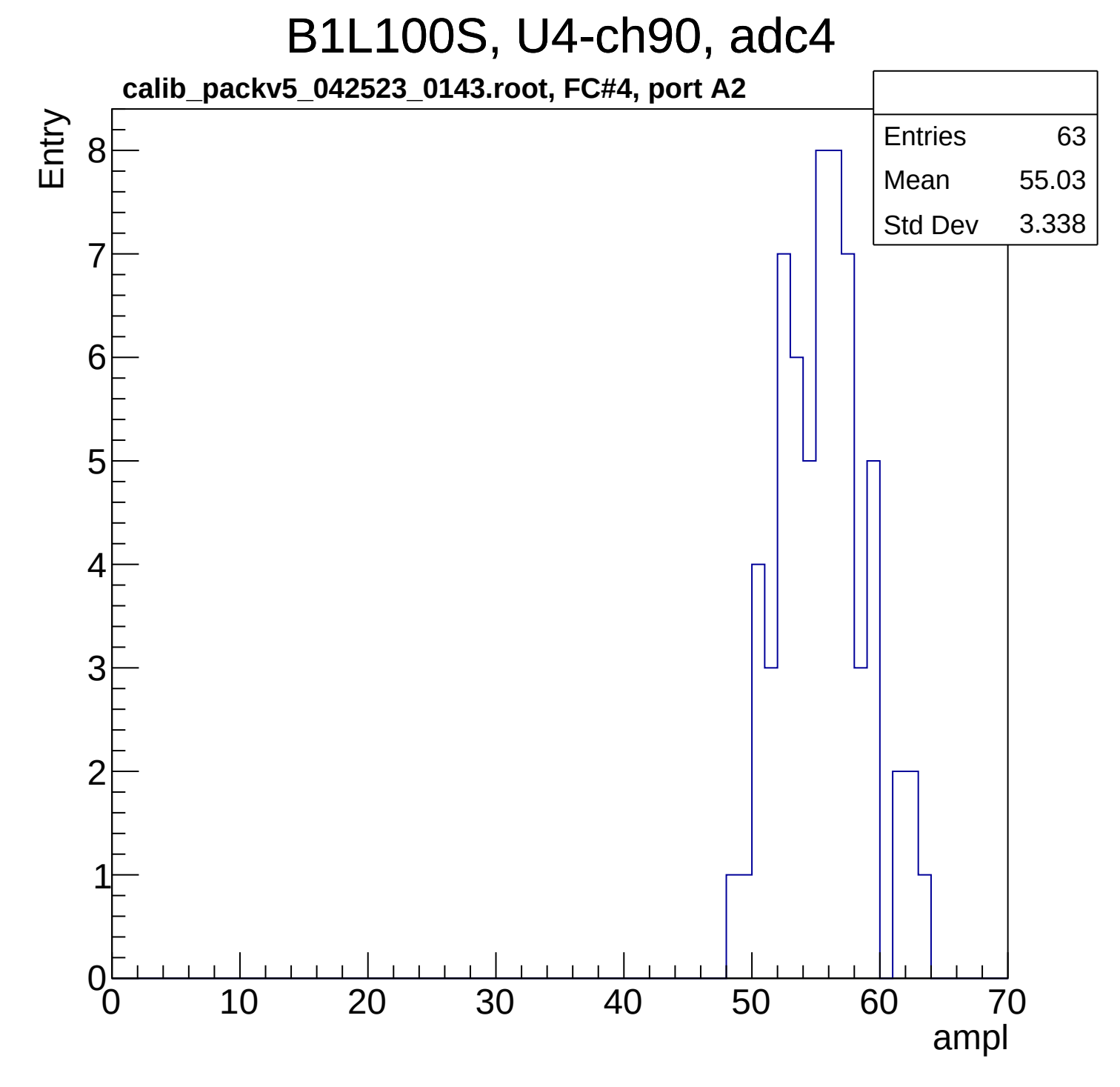

B1L100S, U4-ch89, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

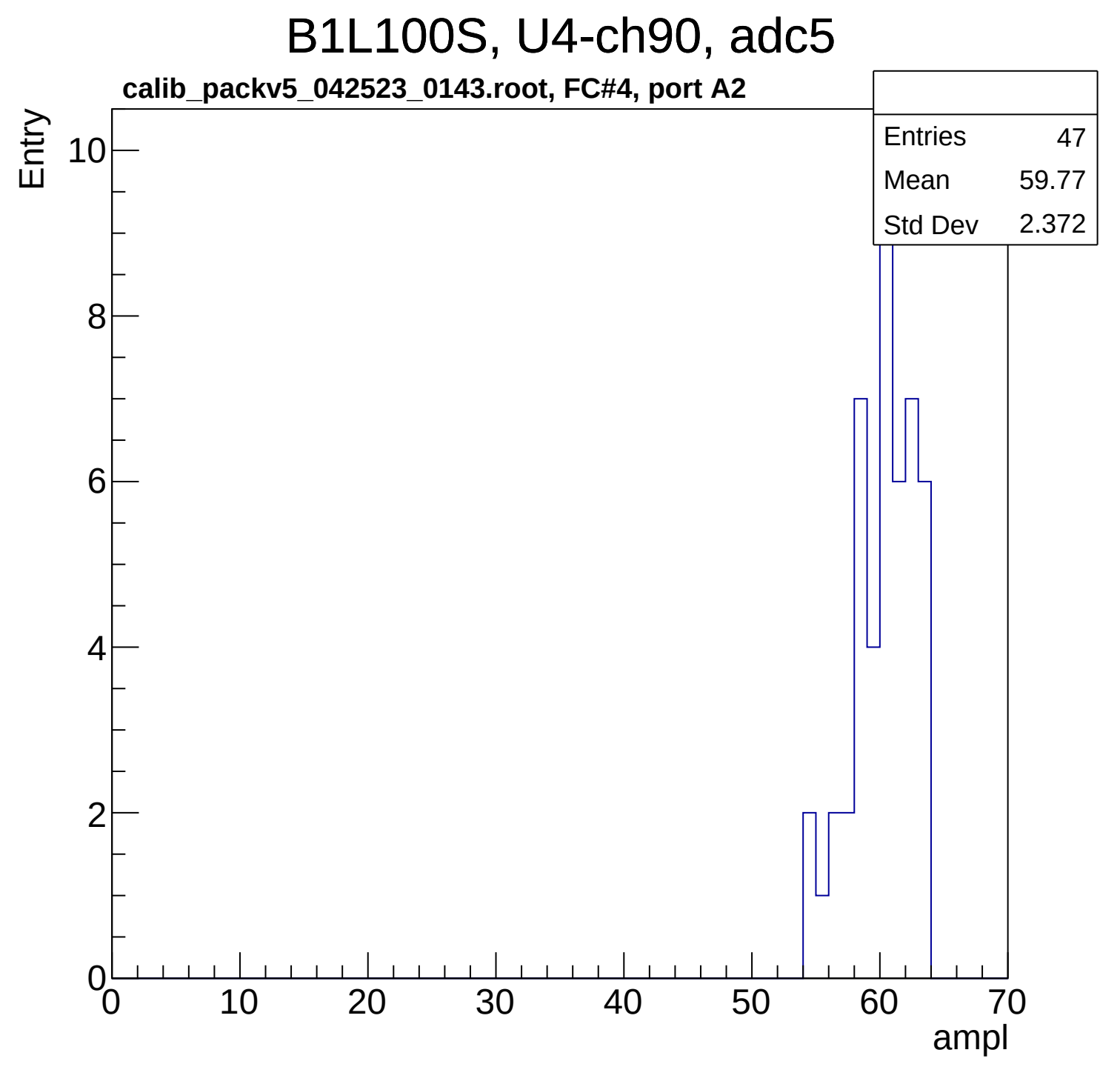

B1L100S, U4-ch90, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 29.09
Std Dev 5.207
Gaus mean : 30.7042
Gaus Width: 4.1450
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

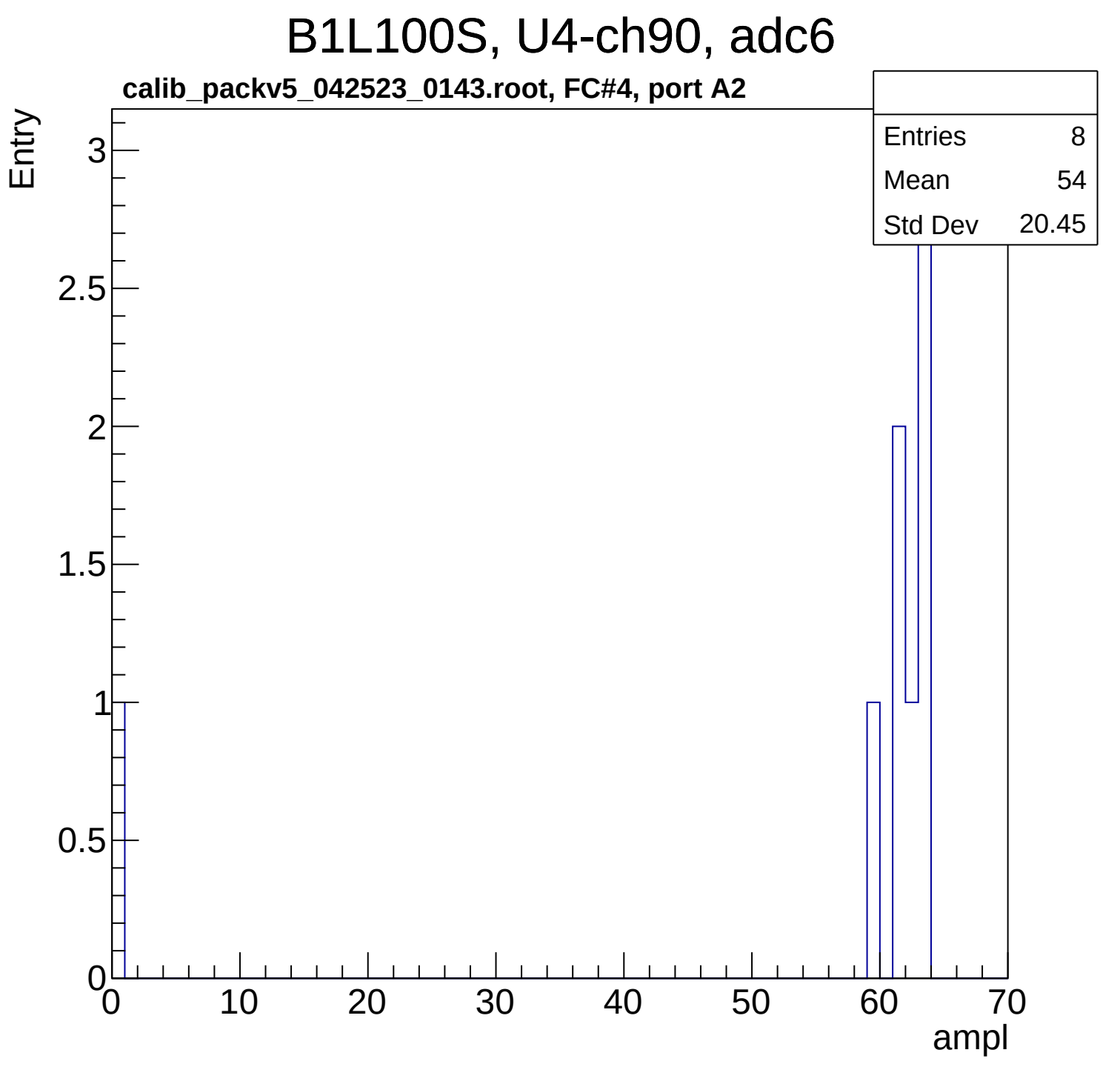

B1L100S, U4-ch90, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 36.53
Std Dev 3.403
Gaus mean : 36.9733
Gaus Width: 4.1920
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

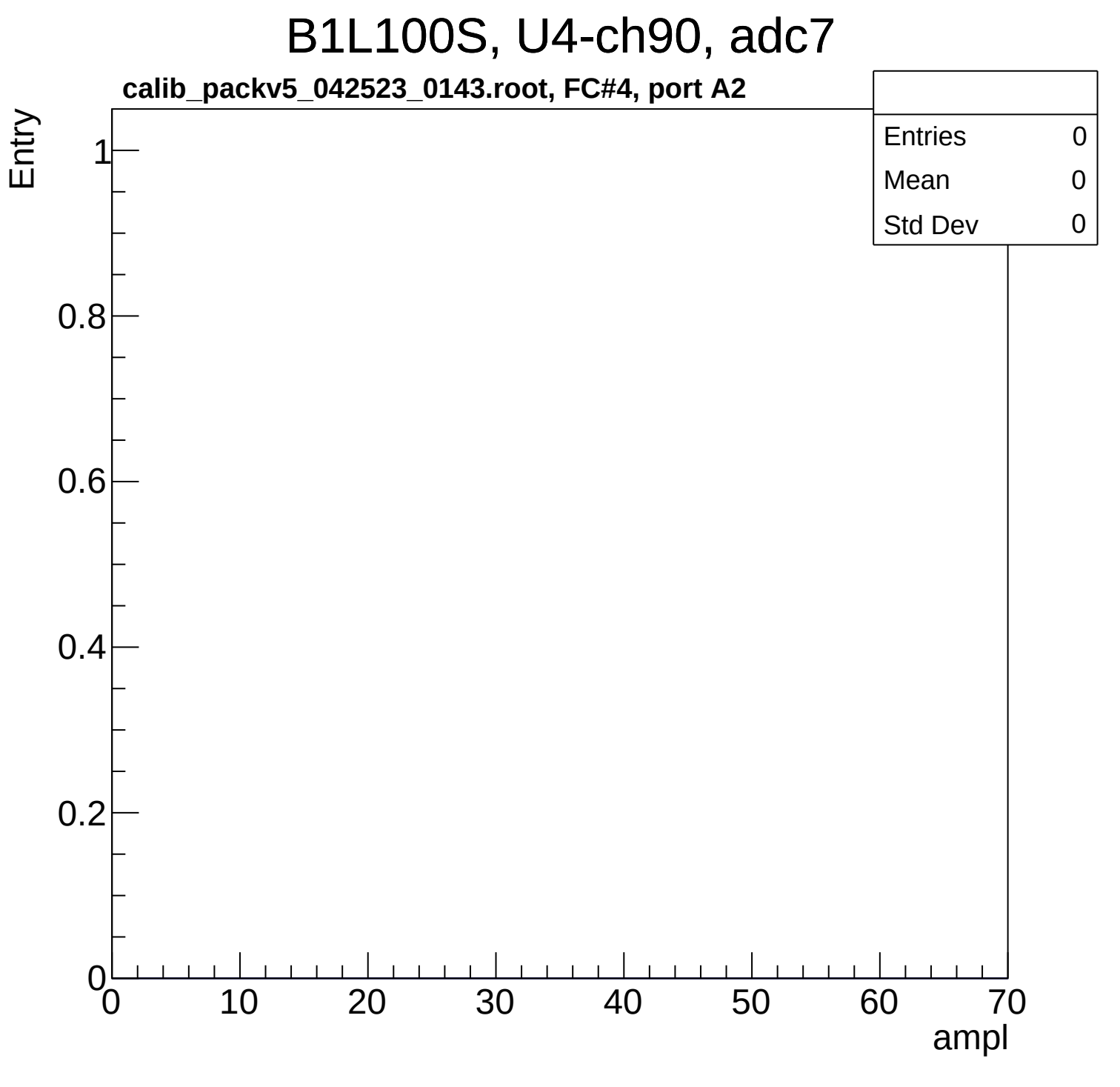

B1L100S, U4-ch90, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 42.53
Std Dev 3.872
Gaus mean : 43.3926
Gaus Width: 4.5682
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

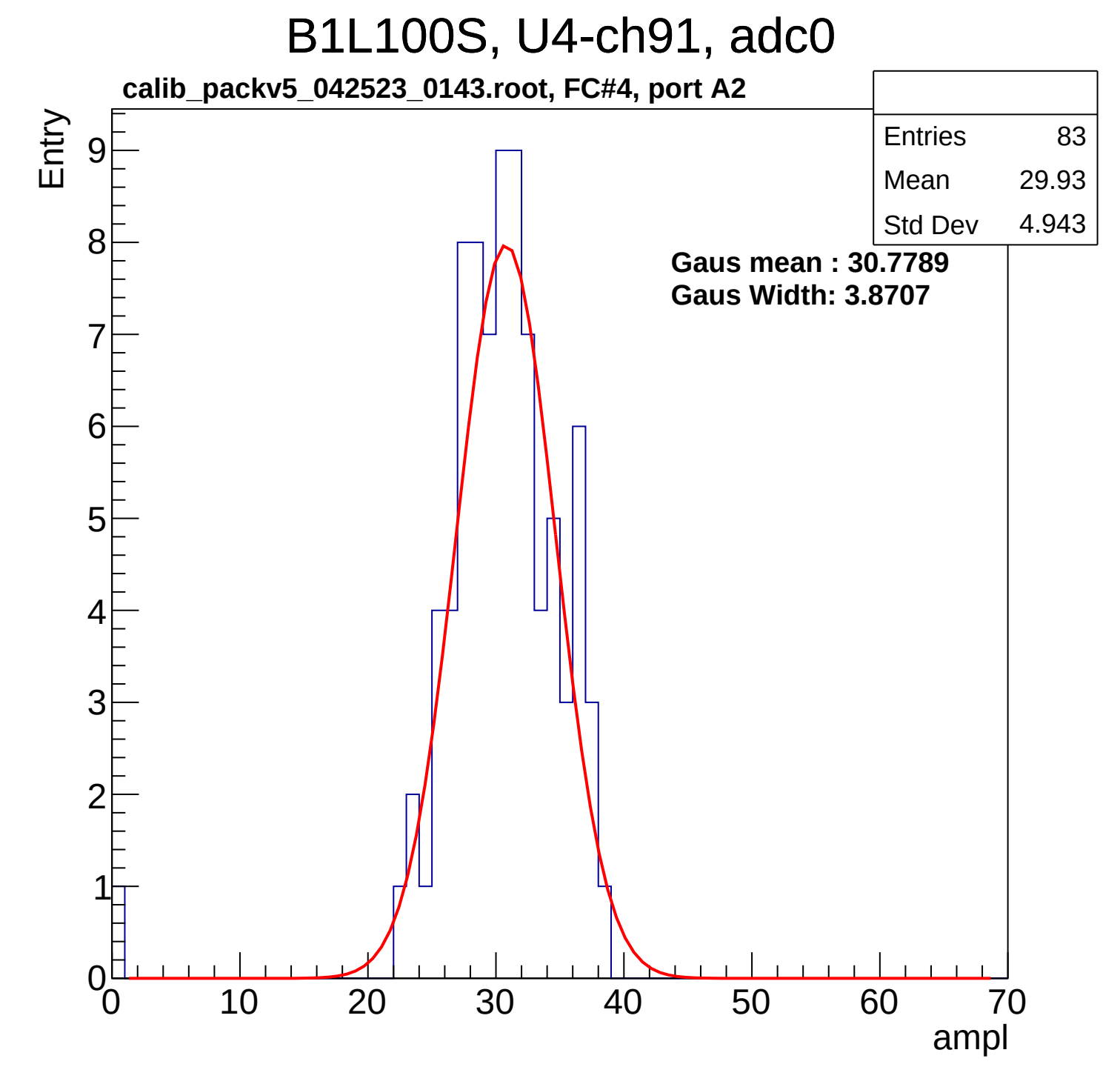

B1L100S, U4-ch90, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 49.17
Std Dev 3.209
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

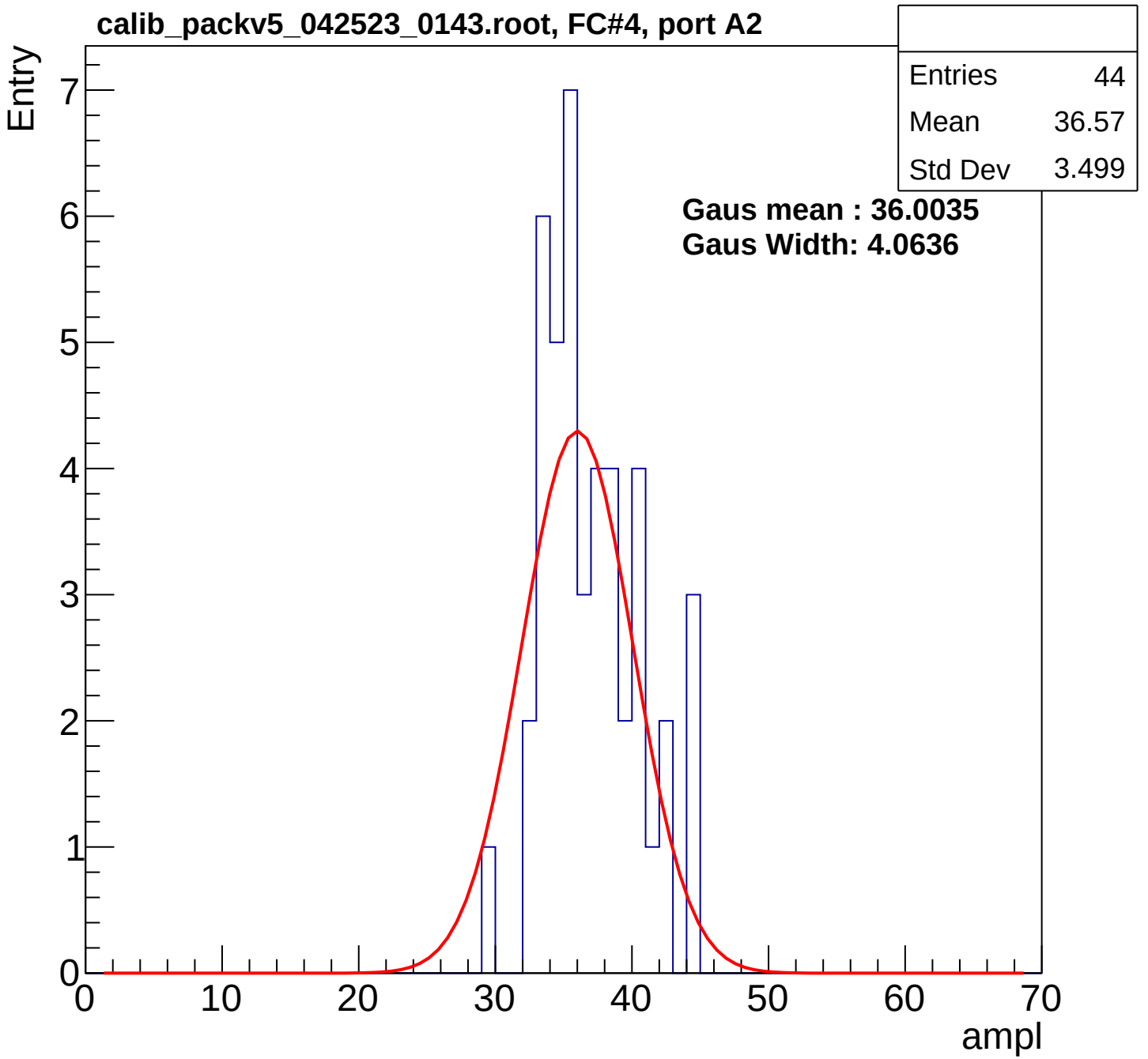

B1L100S, U4-ch90, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 55.03
Std Dev 3.338
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

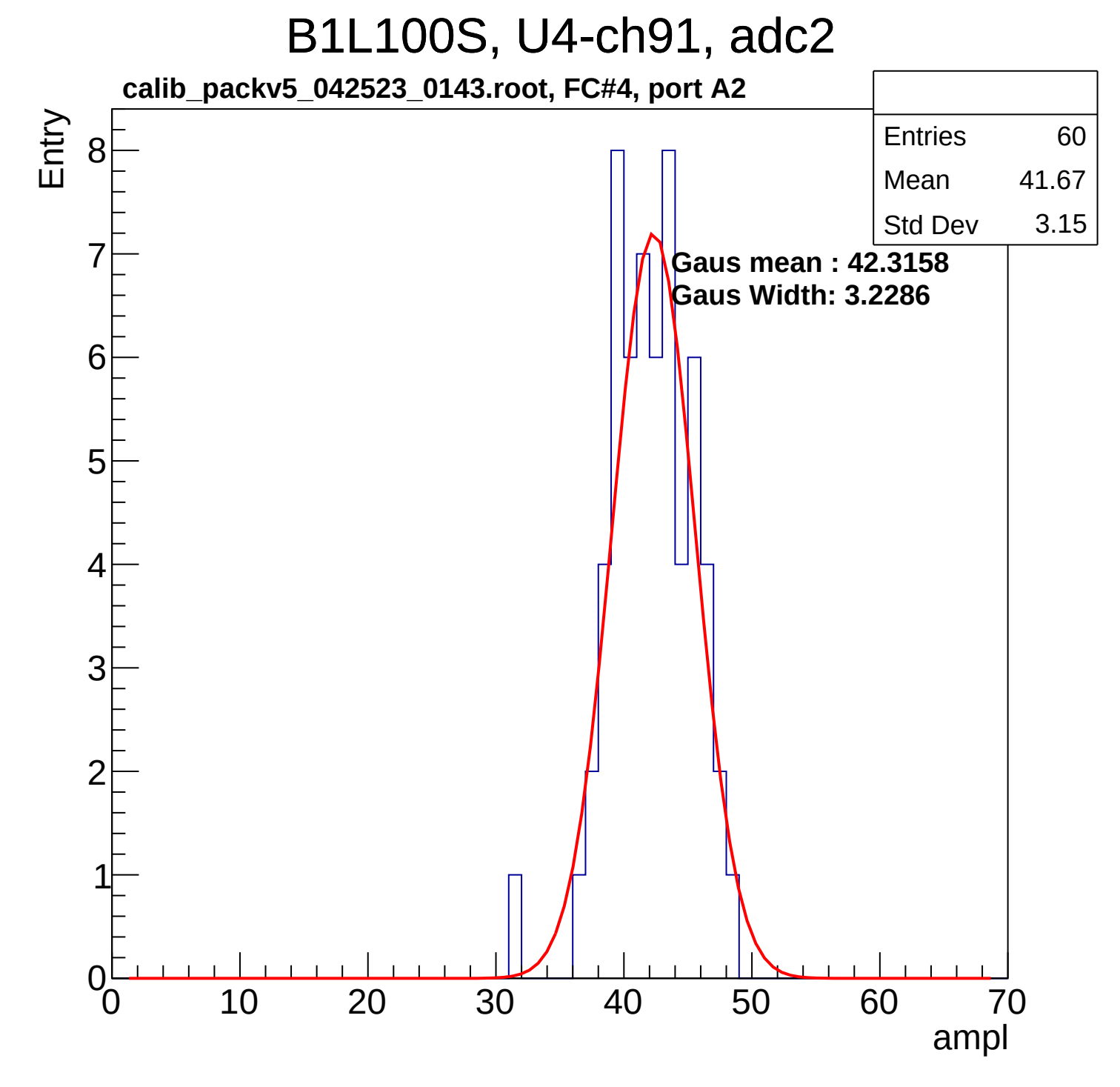

B1L100S, U4-ch90, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 59.77
Std Dev 2.372
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

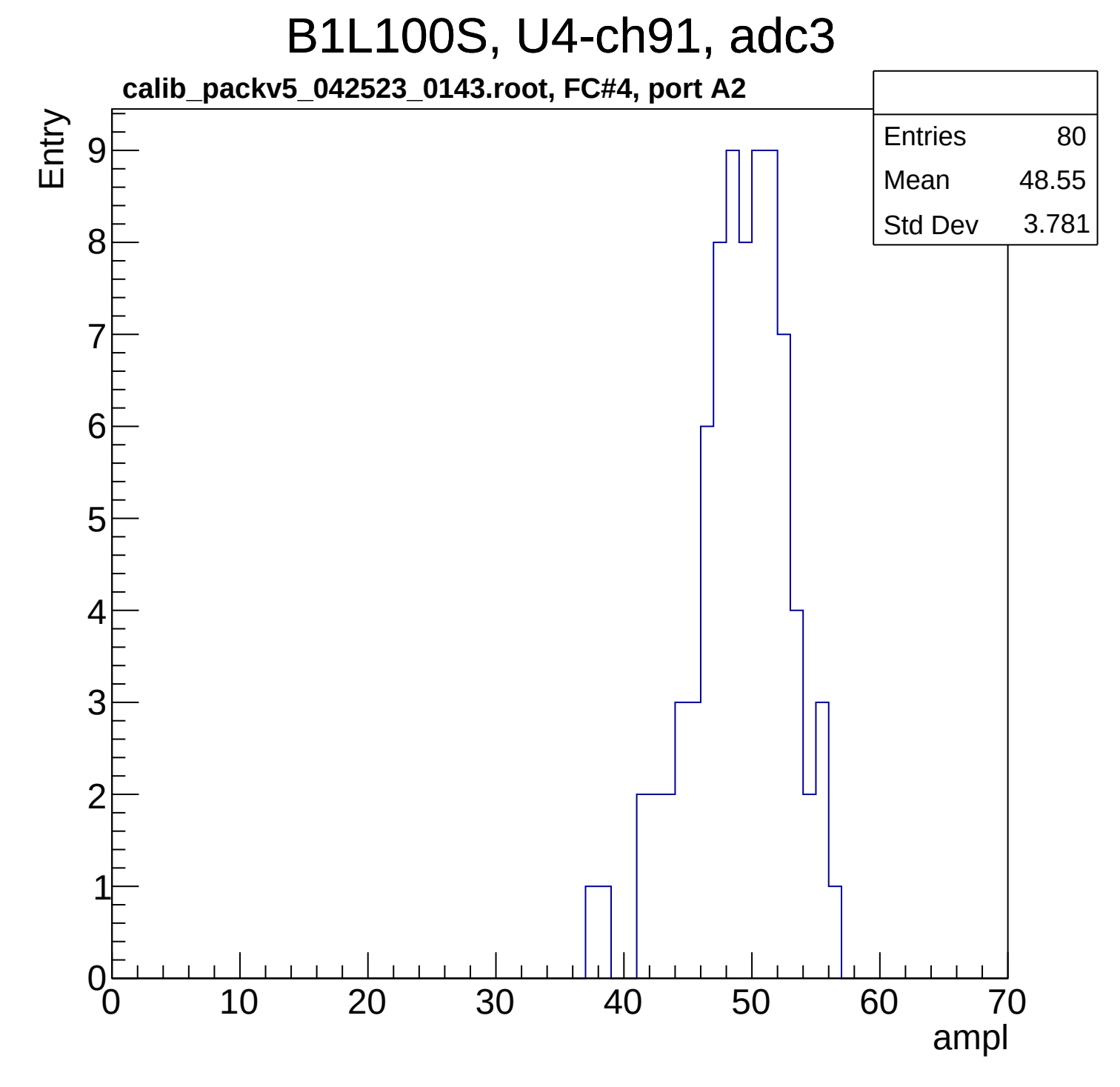

B1L100S, U4-ch90, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 8
Mean 54
Std Dev 20.45
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

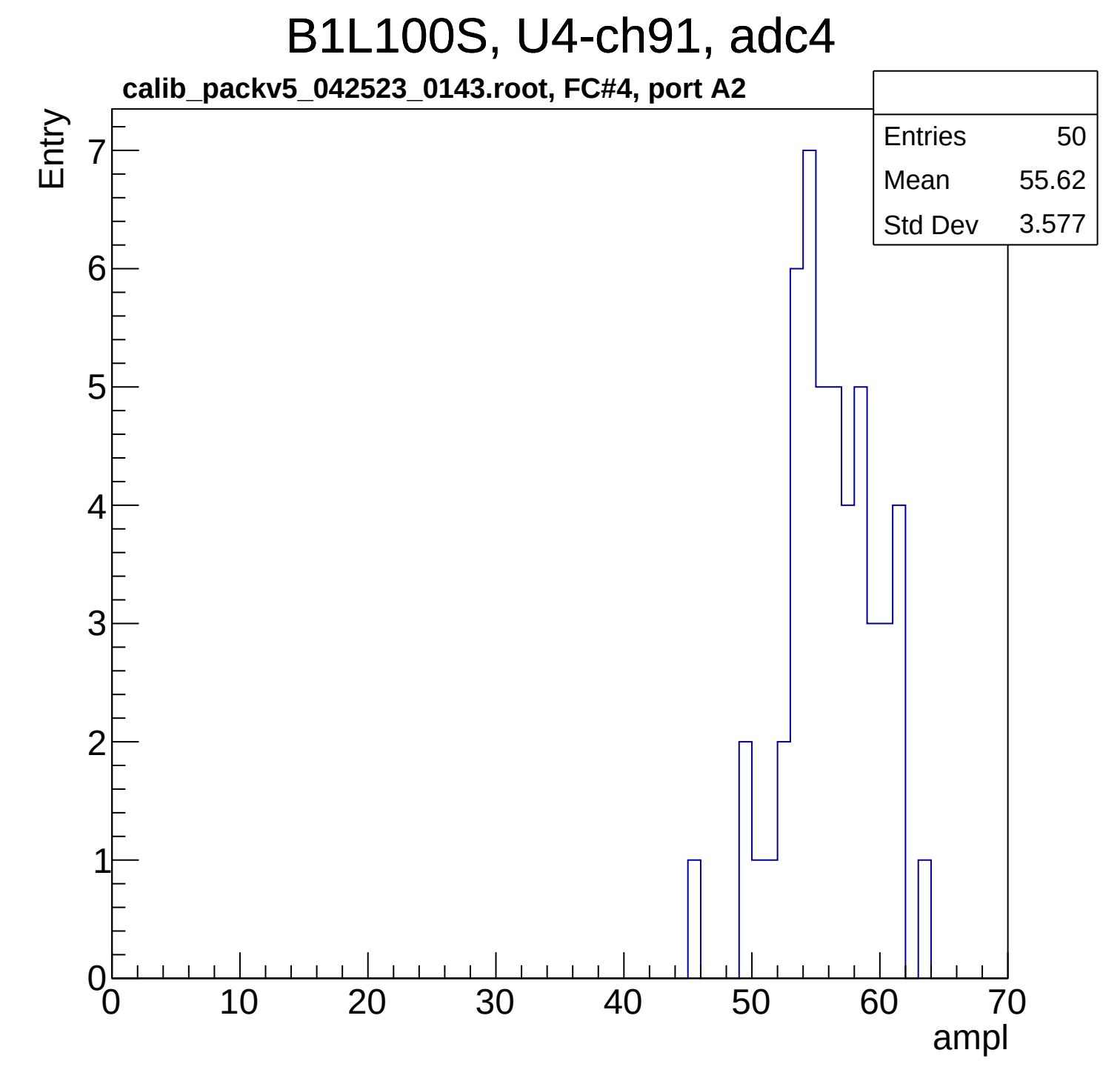

B1L100S, U4-ch90, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

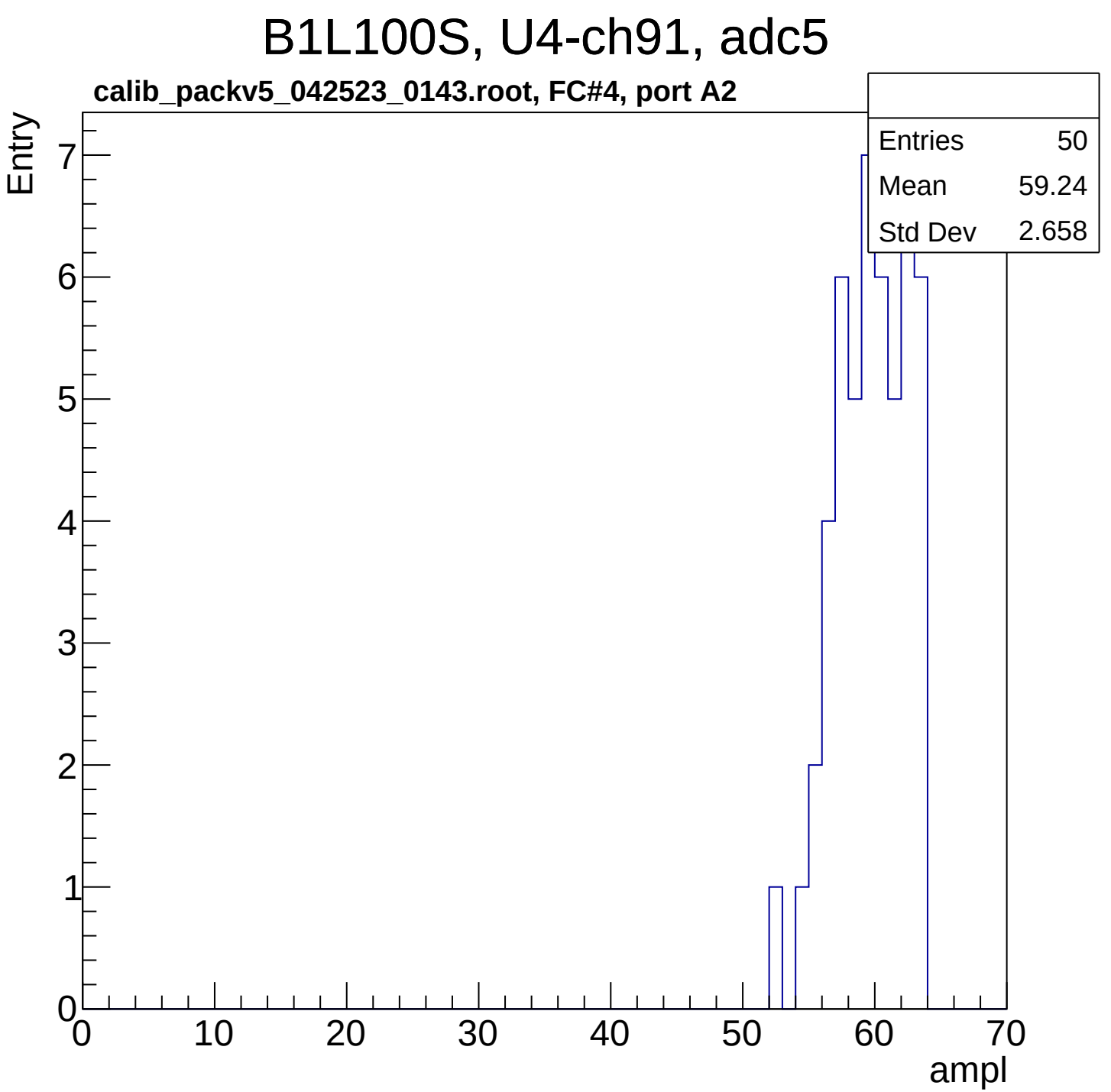

B1L100S, U4-ch91, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 83
Mean 29.93
Std Dev 4.943
Gaus mean : 30.7789
Gaus Width: 3.8707
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

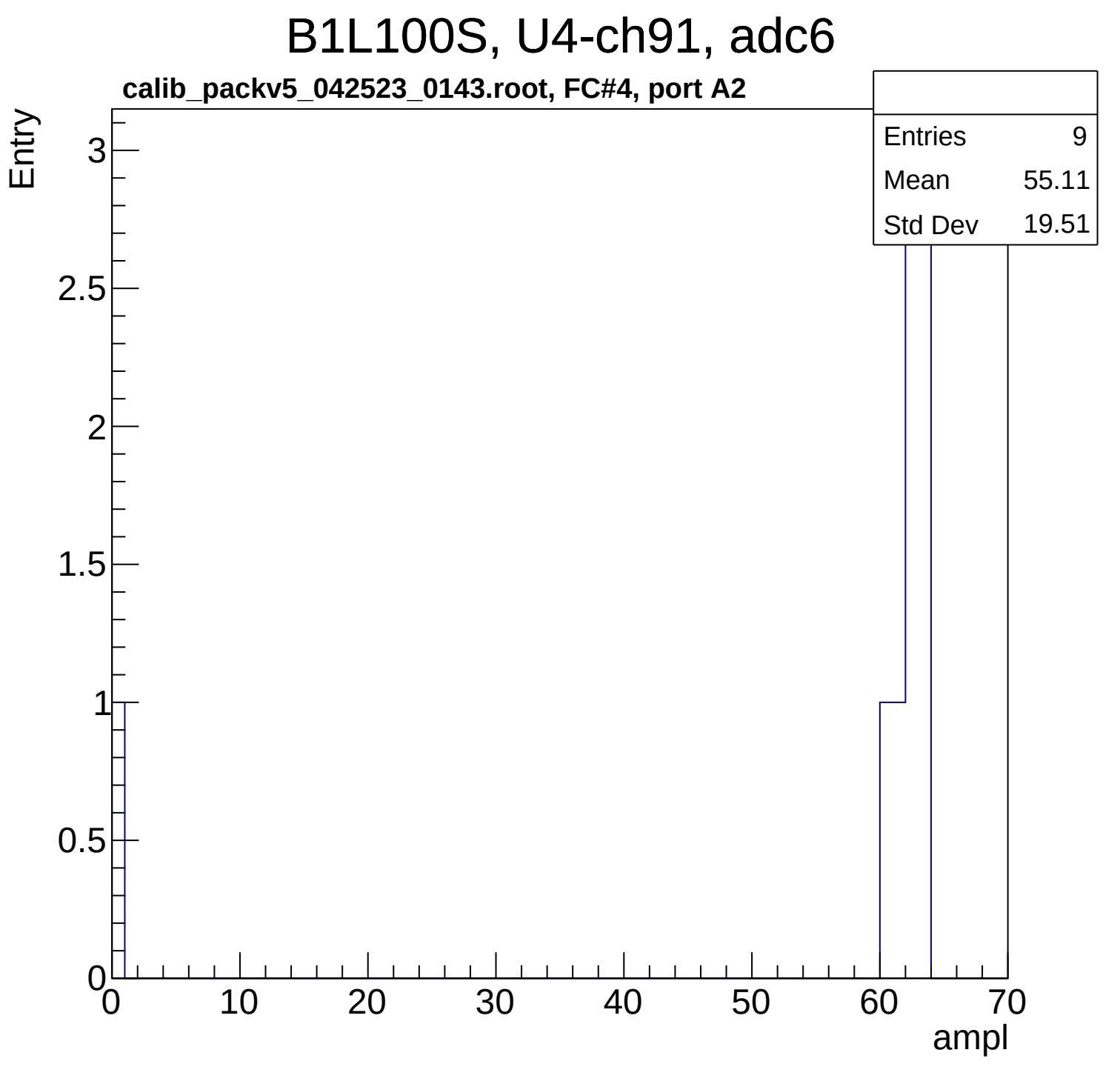

B1L100S, U4-ch91, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 44
Mean 36.57
Std Dev 3.499
Gaus mean : 36.0035
Gaus Width: 4.0636
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

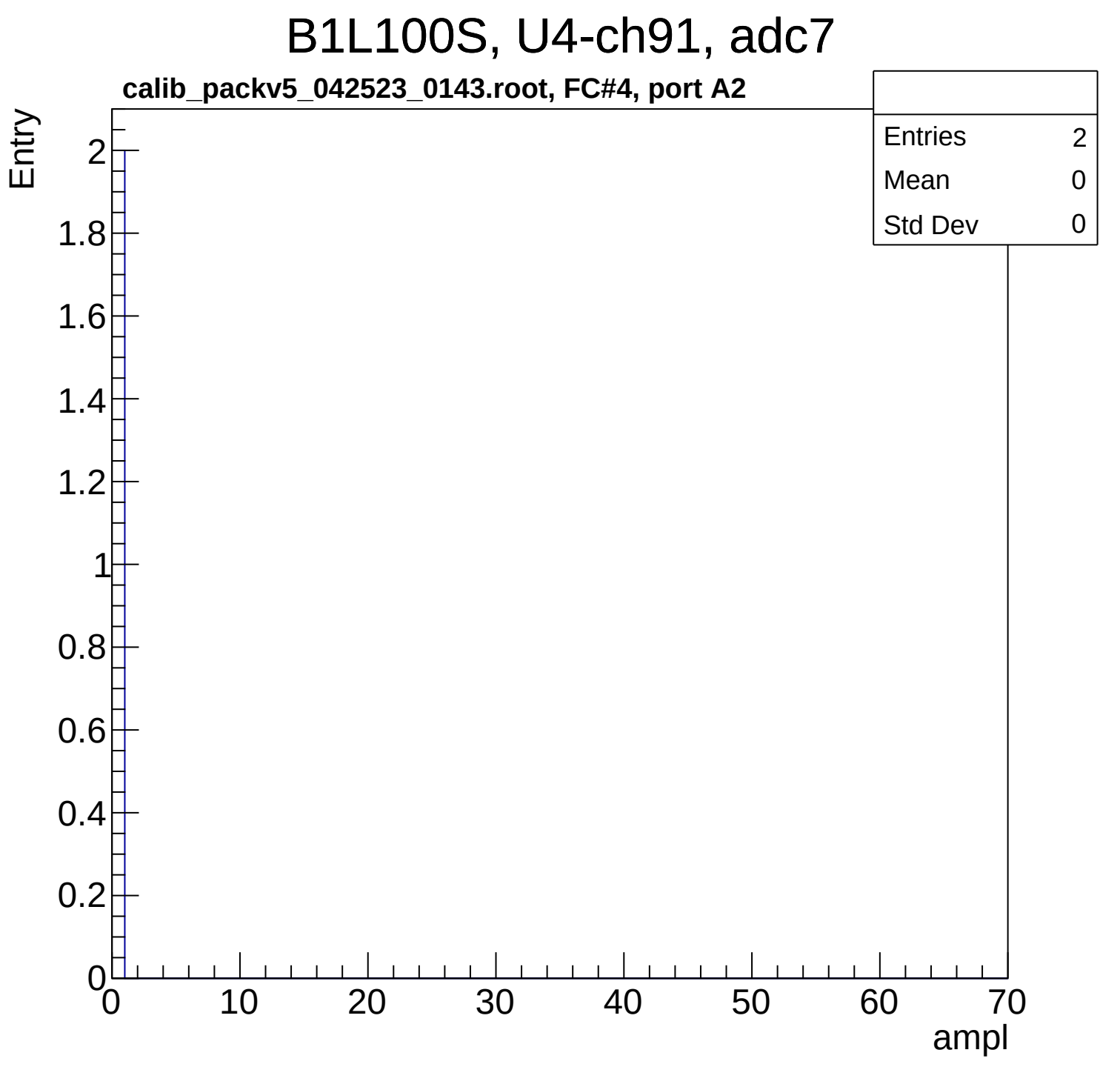

B1L100S, U4-ch91, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 41.67
Std Dev 3.15
Gaus mean : 42.3158
Gaus Width: 3.2286
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

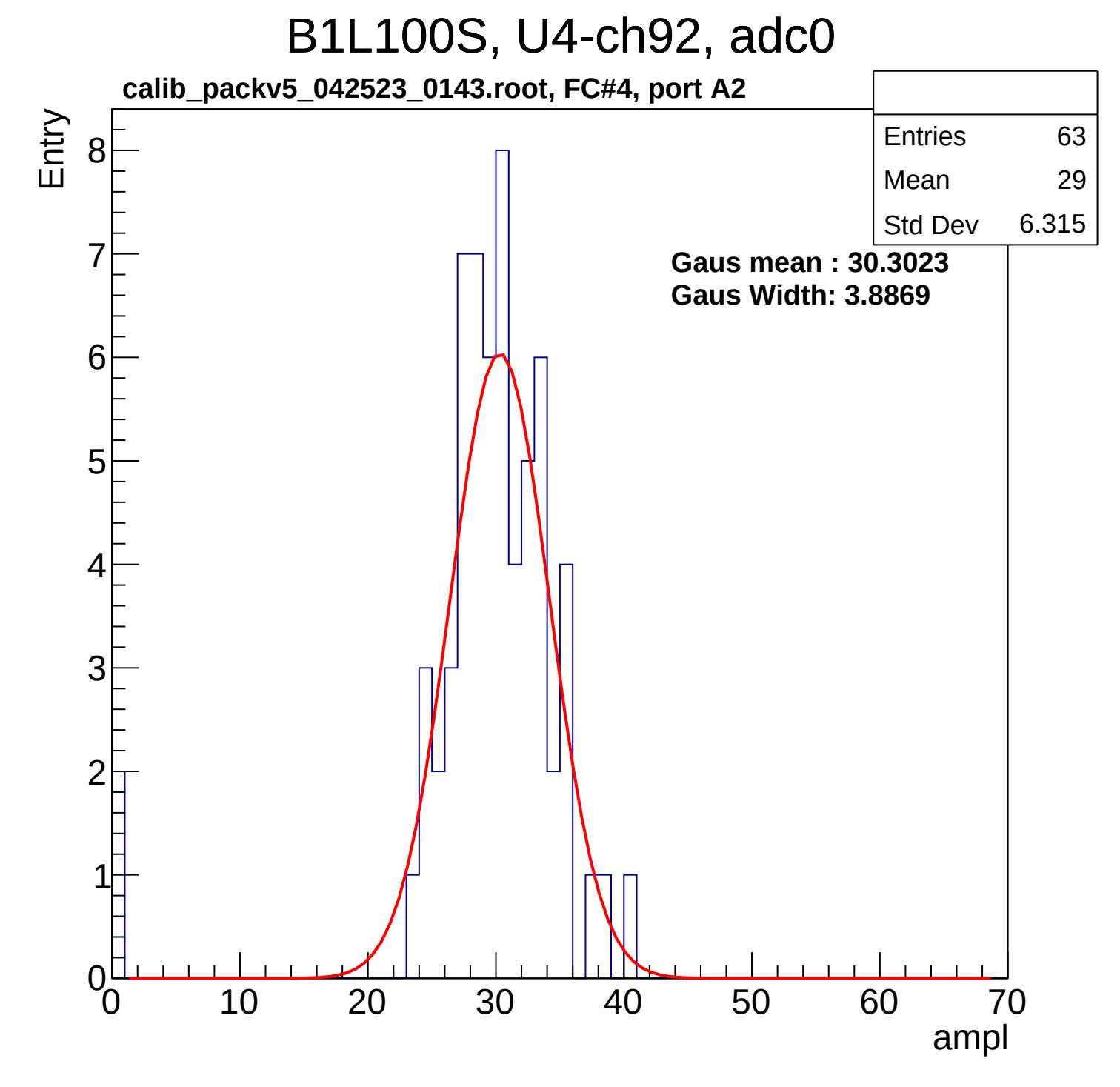

B1L100S, U4-ch91, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 48.55
Std Dev 3.781
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

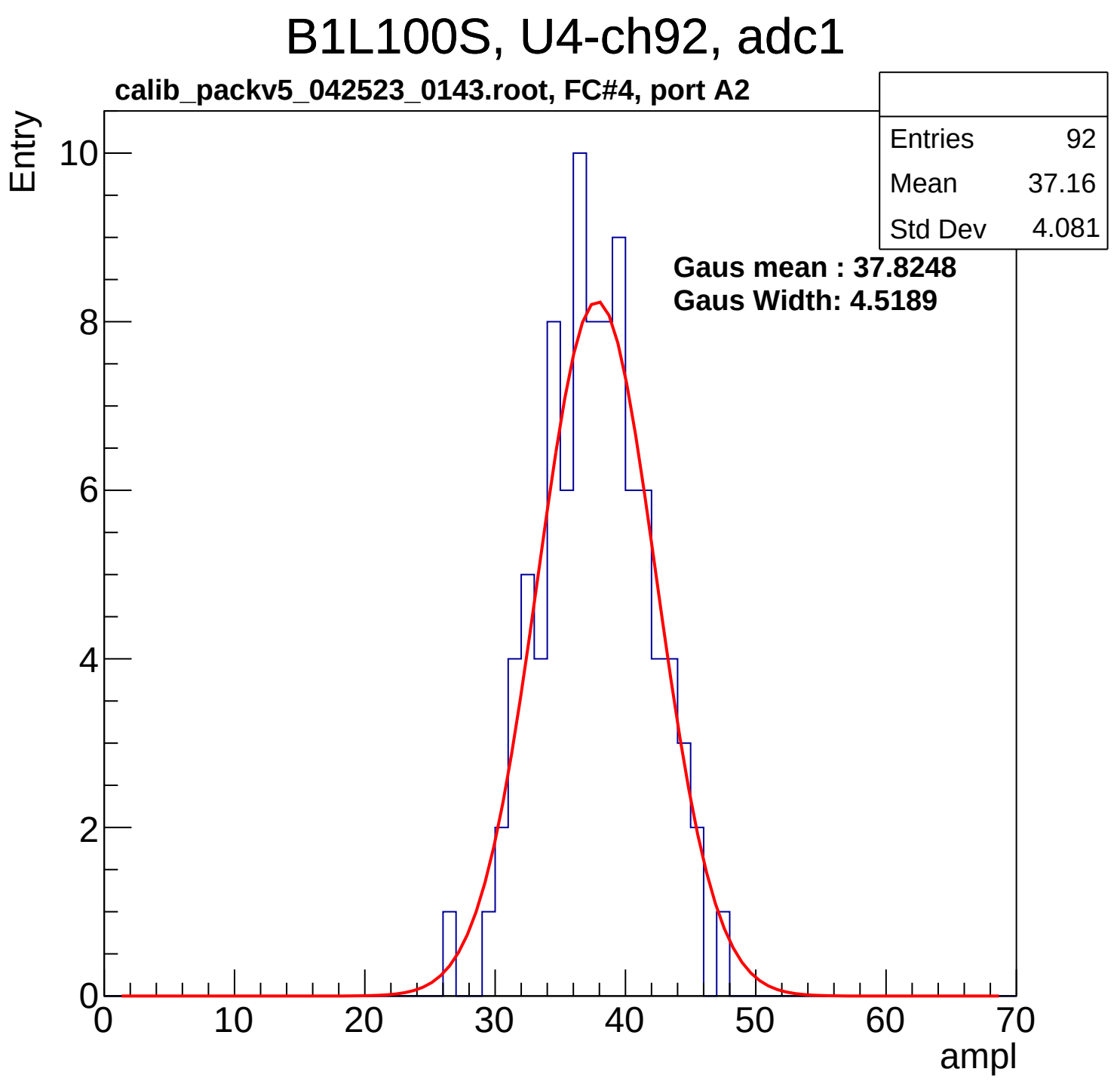

B1L100S, U4-ch91, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 55.62
Std Dev 3.577
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

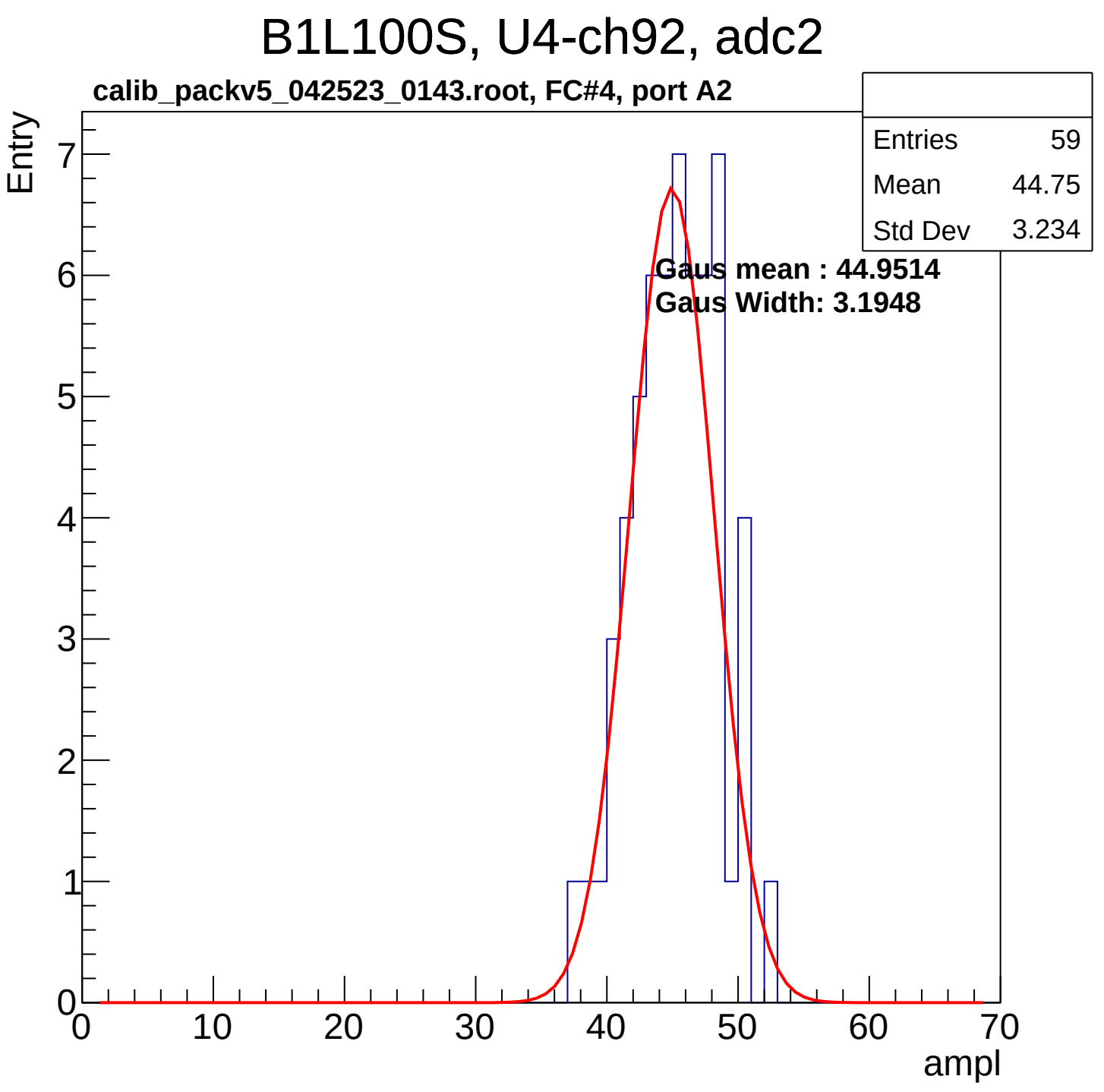

B1L100S, U4-ch91, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 59.24
Std Dev 2.658
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

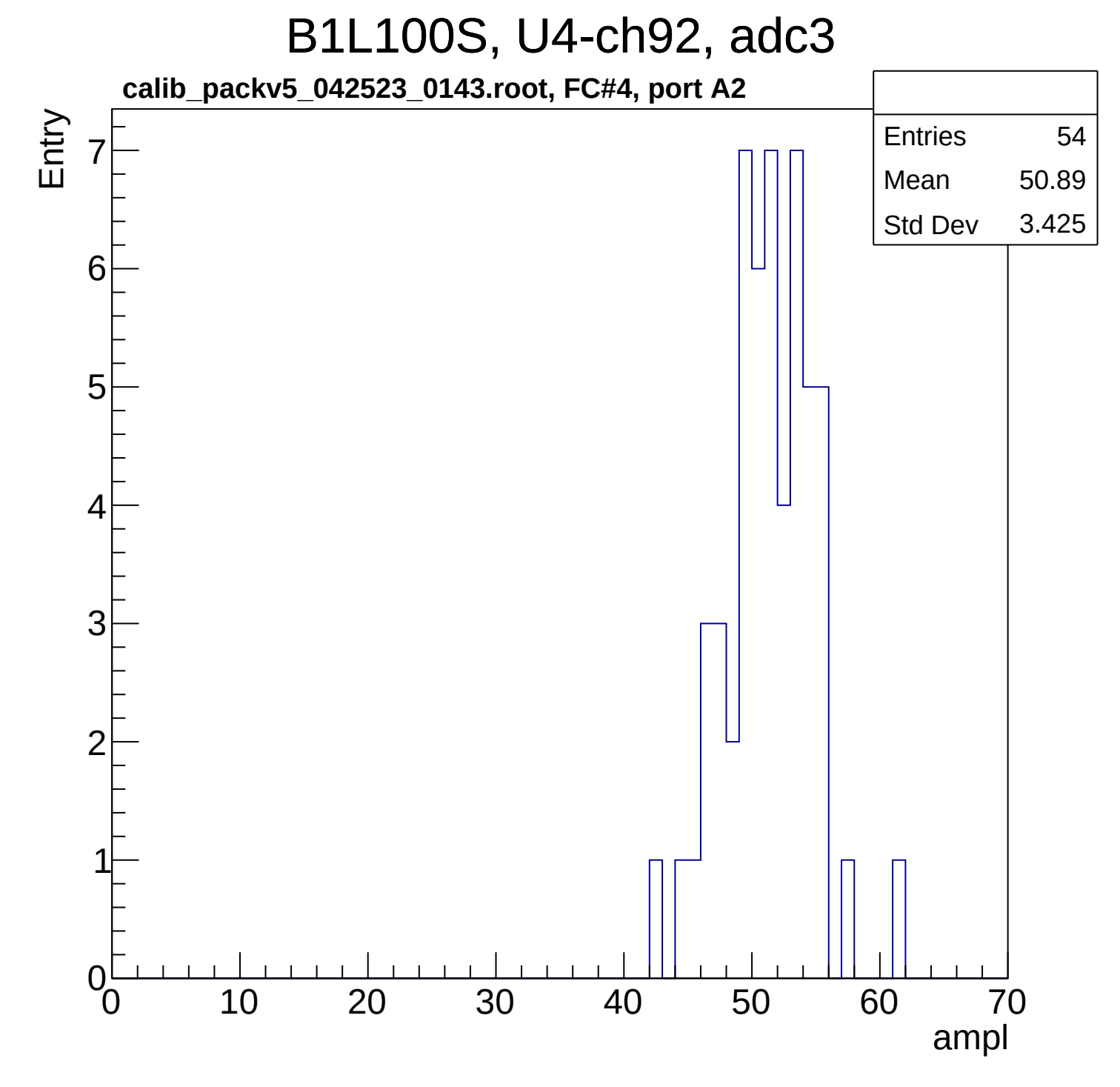

B1L100S, U4-ch91, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 55.11
Std Dev 19.51
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

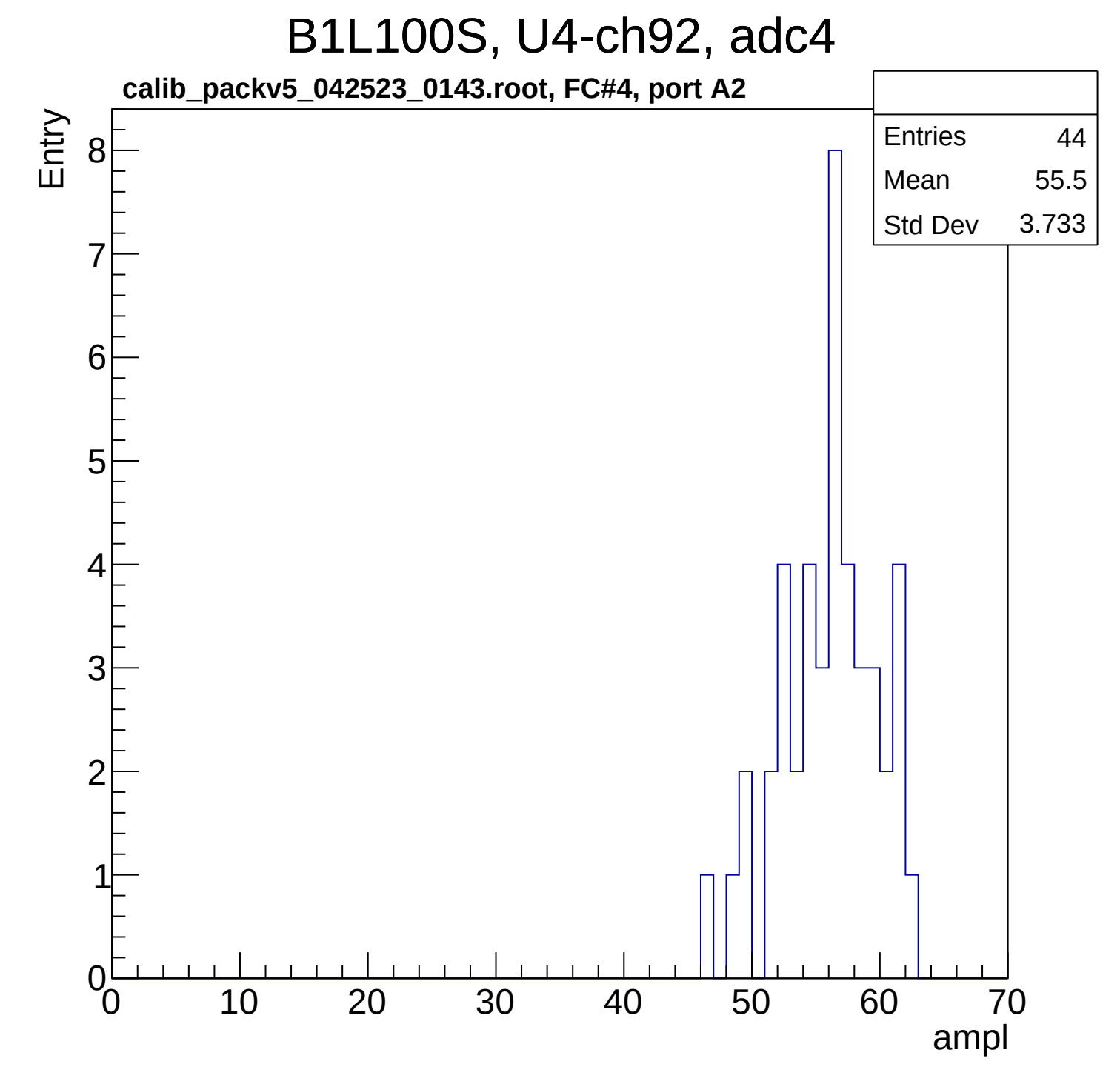

B1L100S, U4-ch91, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

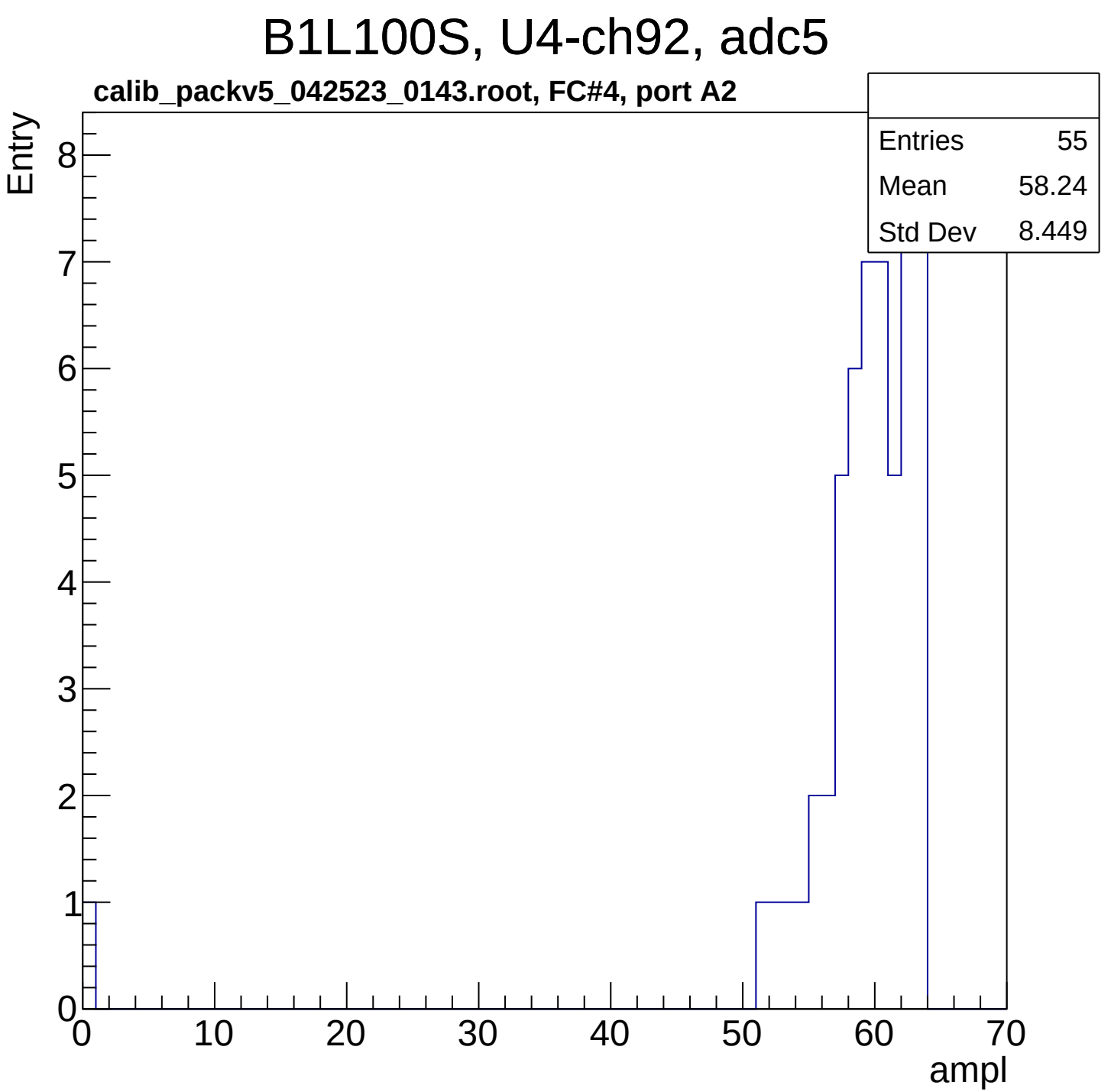

B1L100S, U4-ch92, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 29
Std Dev 6.315
Gaus mean : 30.3023
Gaus Width: 3.8869
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

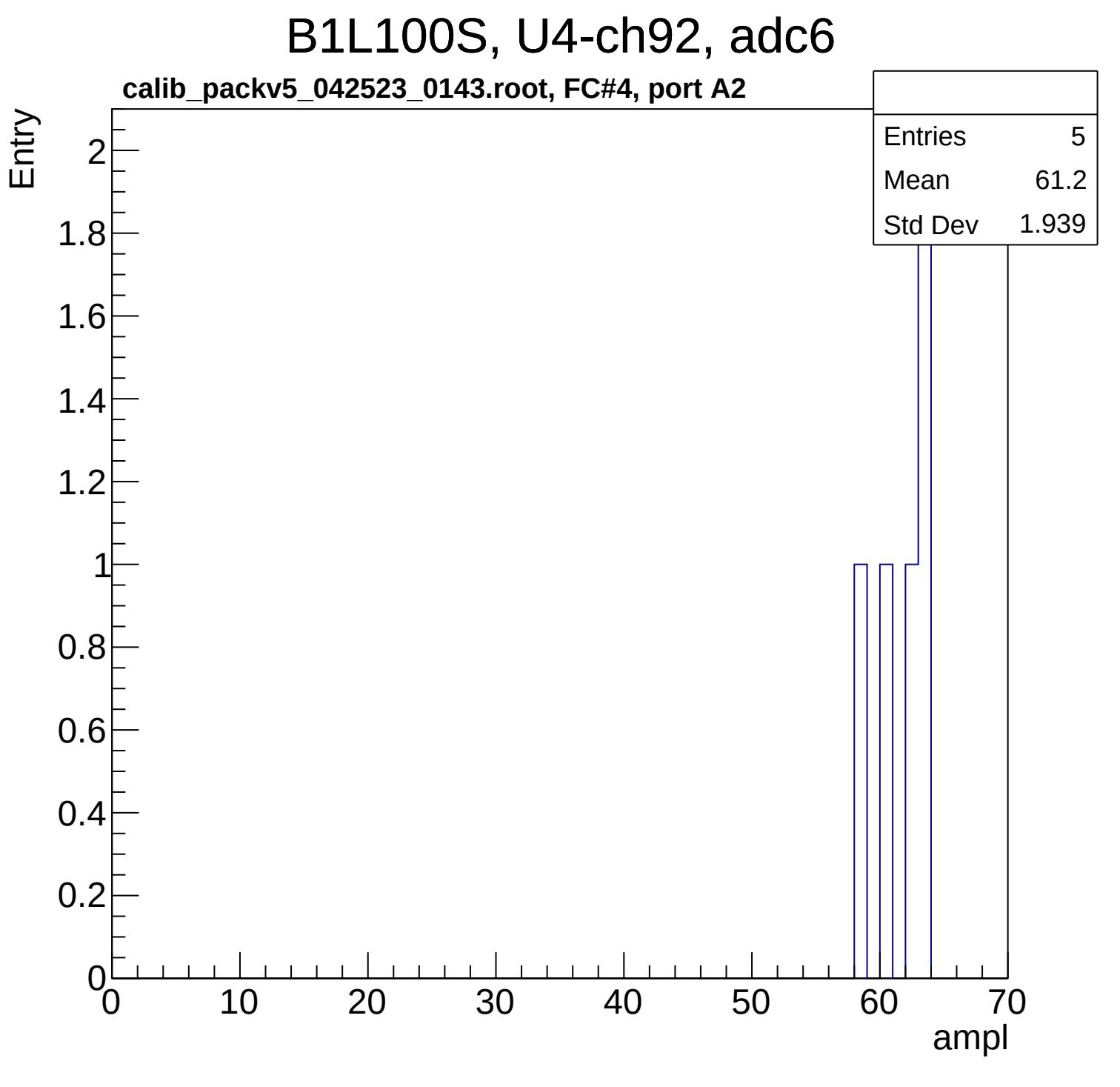

B1L100S, U4-ch92, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 92
Mean 37.16
Std Dev 4.081
Gaus mean : 37.8248
Gaus Width: 4.5189
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

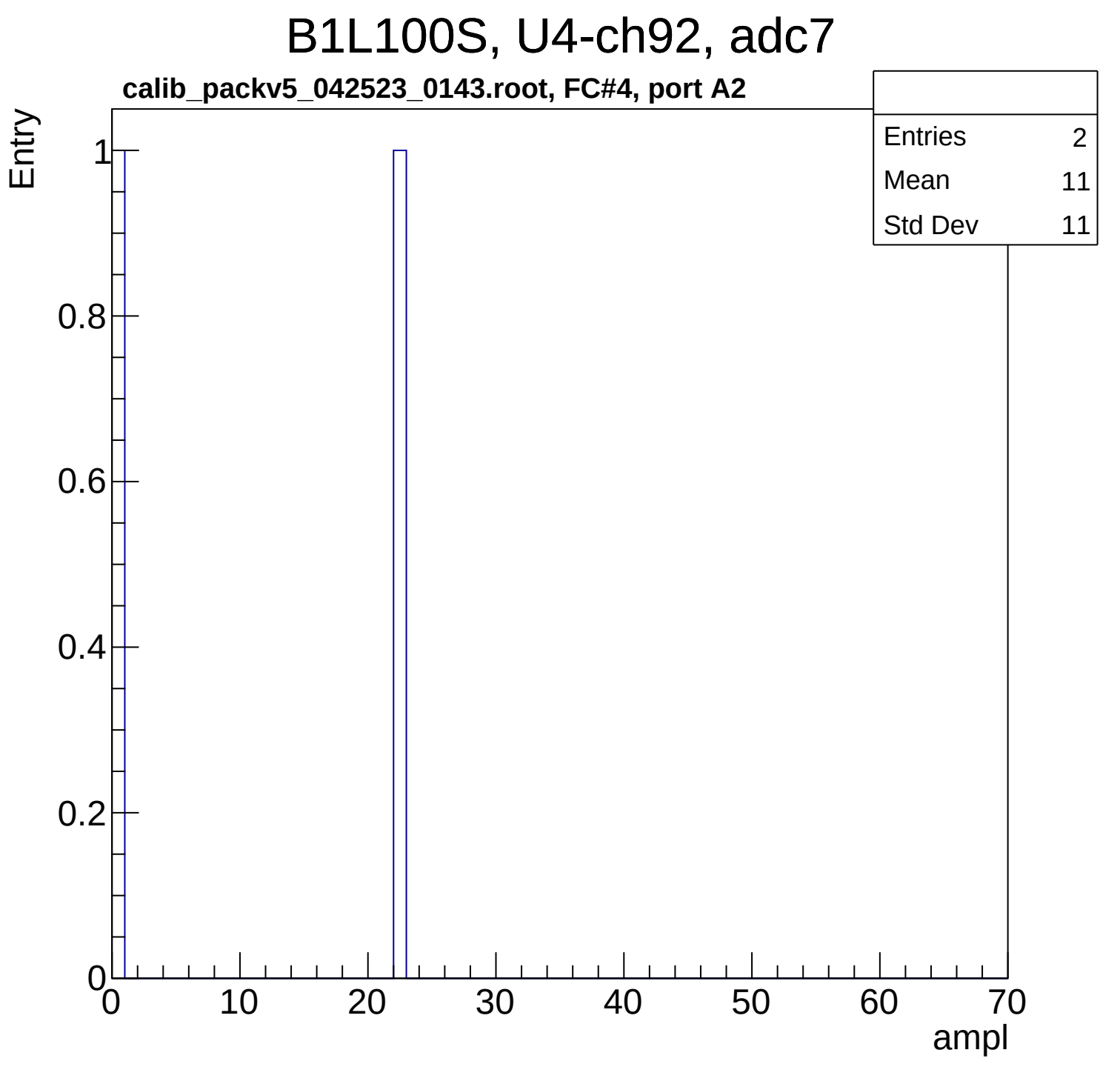

B1L100S, U4-ch92, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 44.75
Std Dev 3.234
Gaus mean : 44.9514
Gaus Width: 3.1948
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

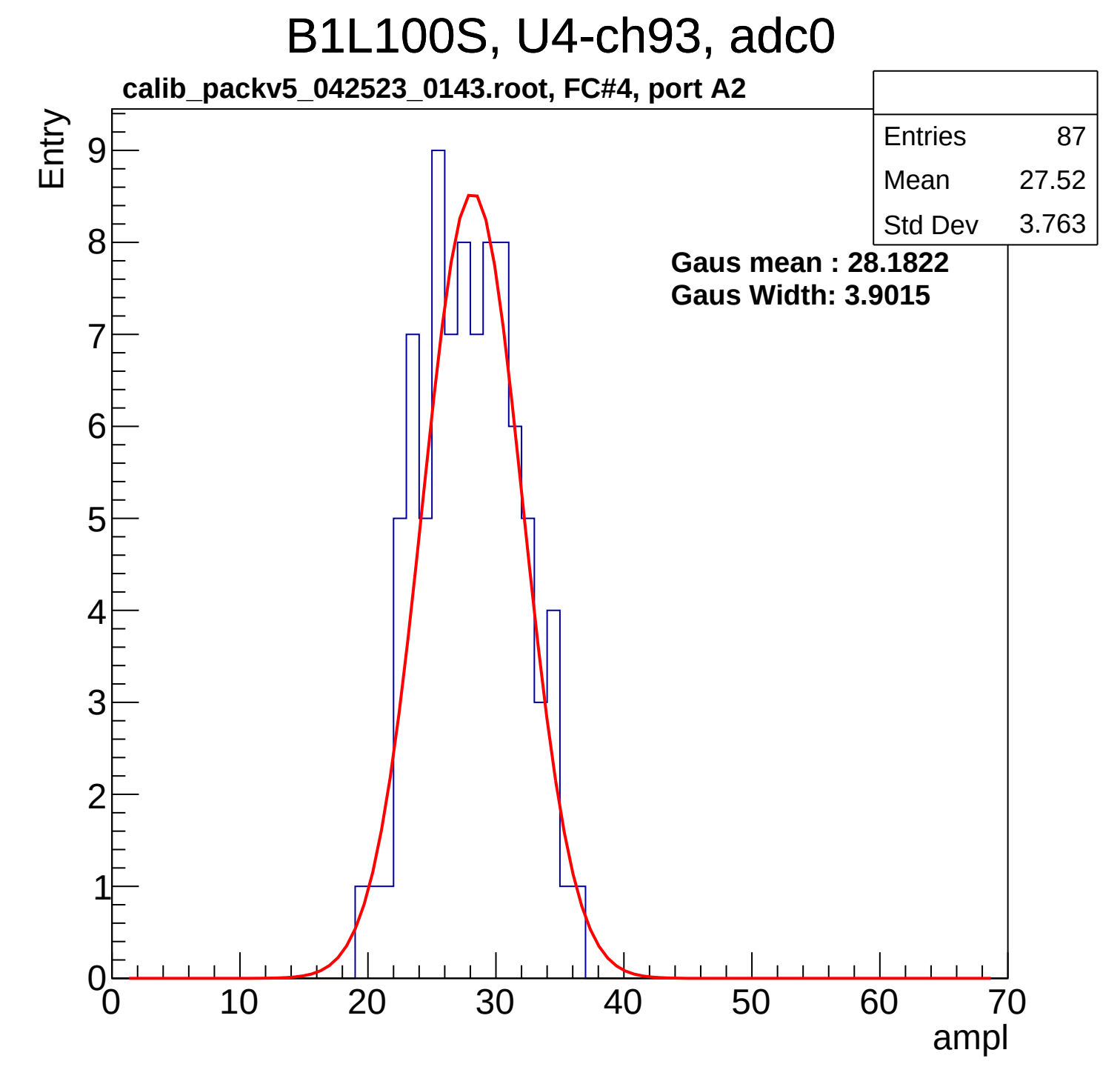

B1L100S, U4-ch92, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 50.89
Std Dev 3.425
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

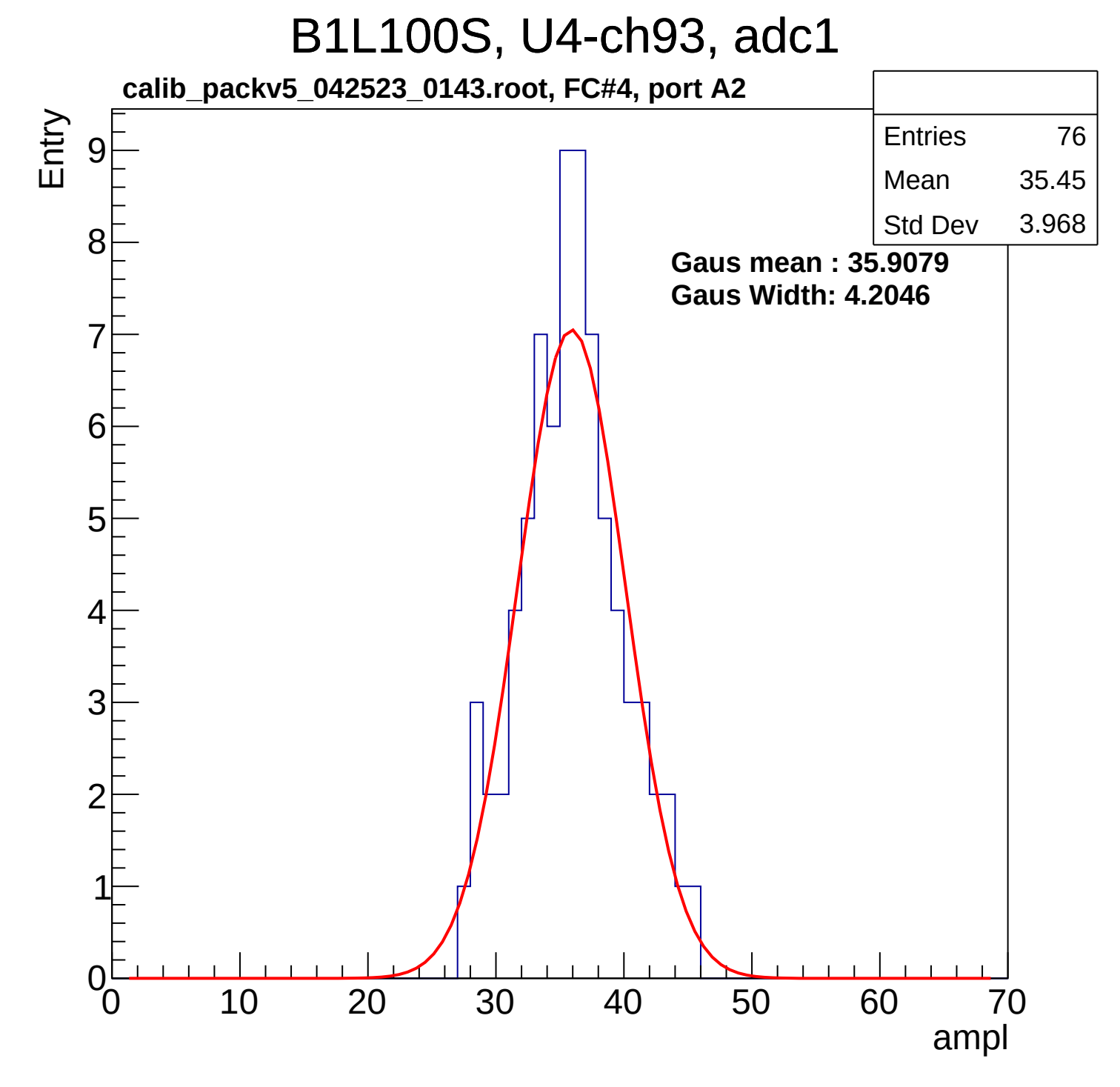

B1L100S, U4-ch92, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 44
Mean 55.5
Std Dev 3.733
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

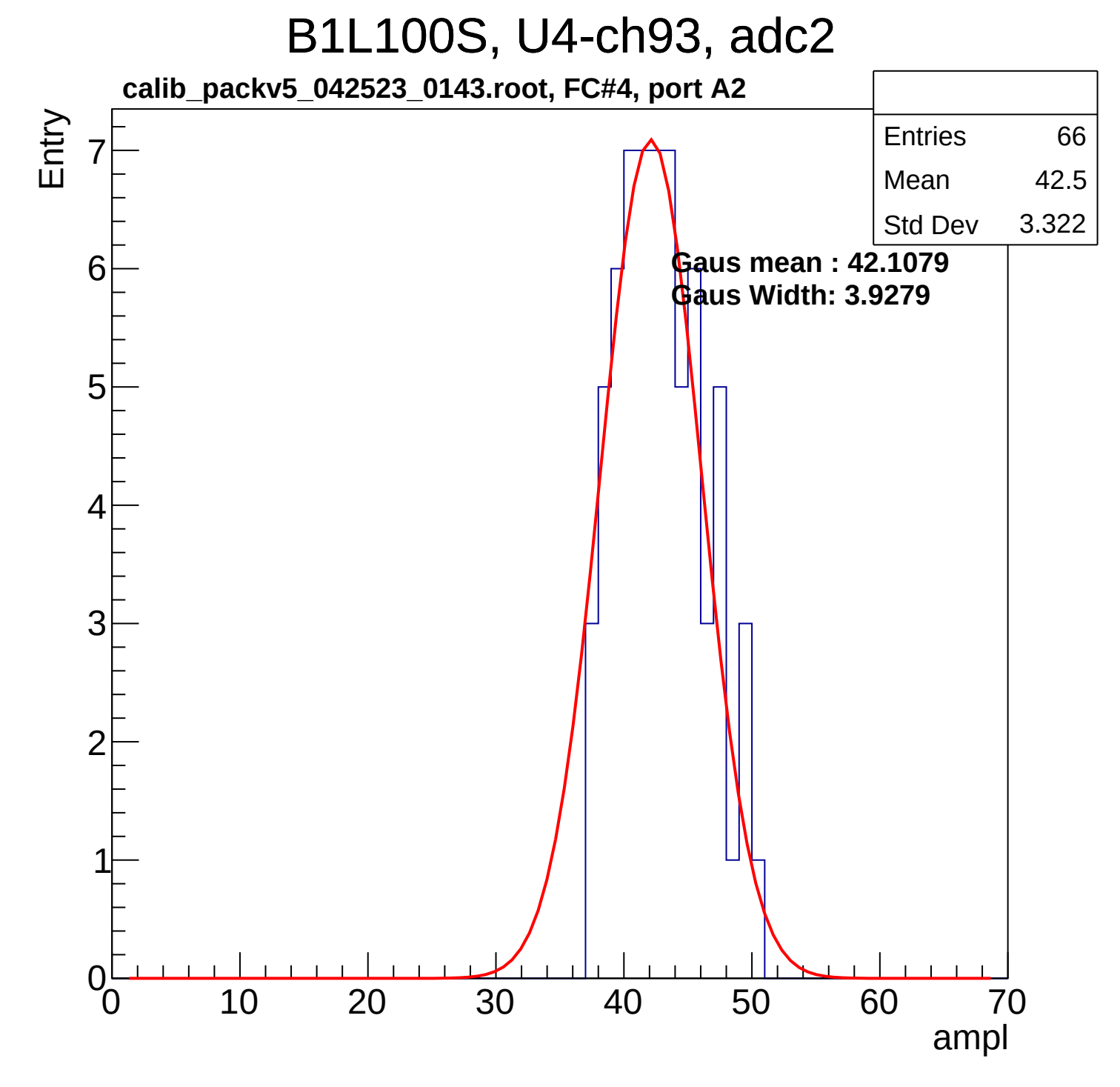

B1L100S, U4-ch92, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 58.24
Std Dev 8.449
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

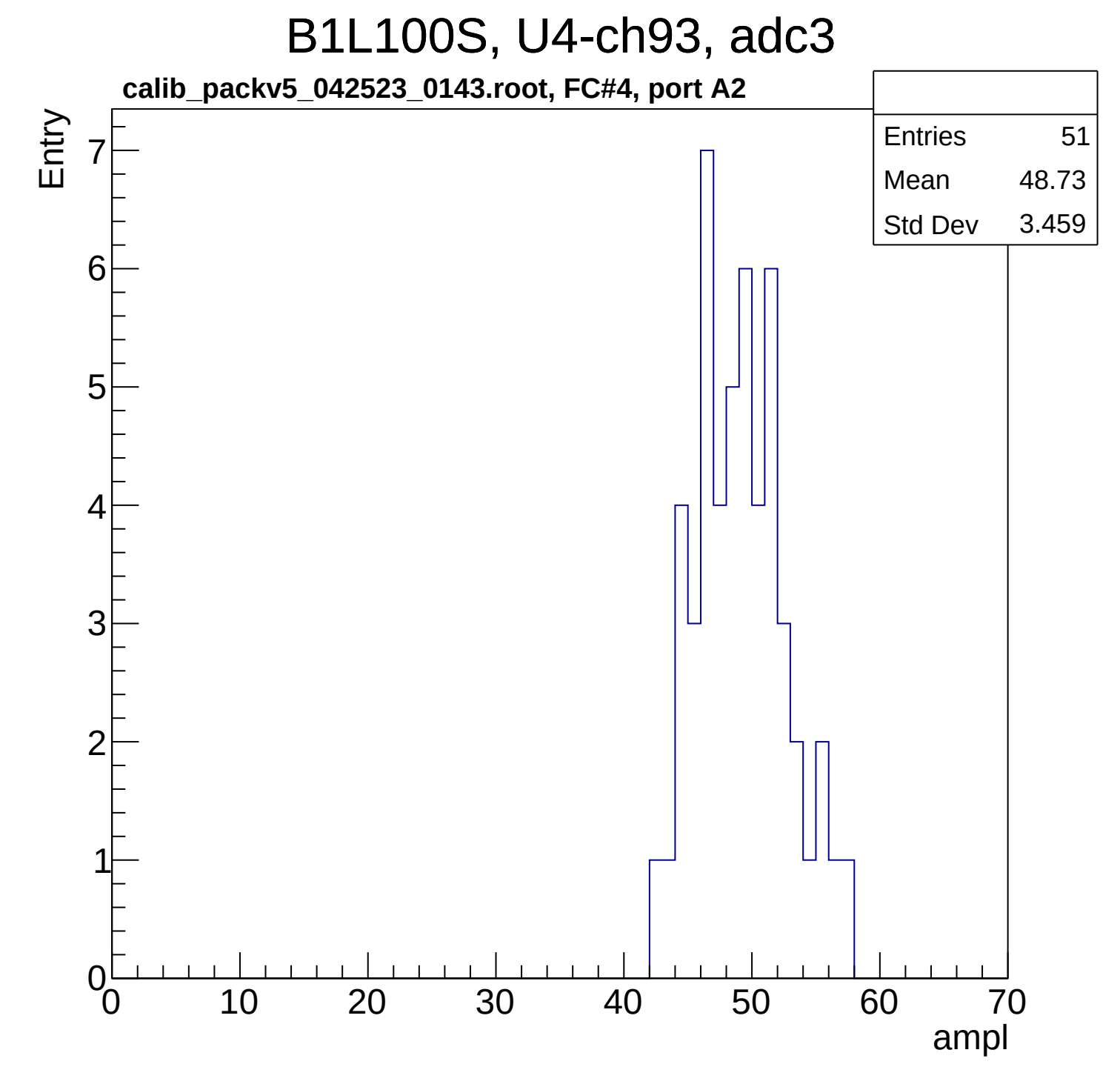

B1L100S, U4-ch92, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 5
Mean 61.2
Std Dev 1.939
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

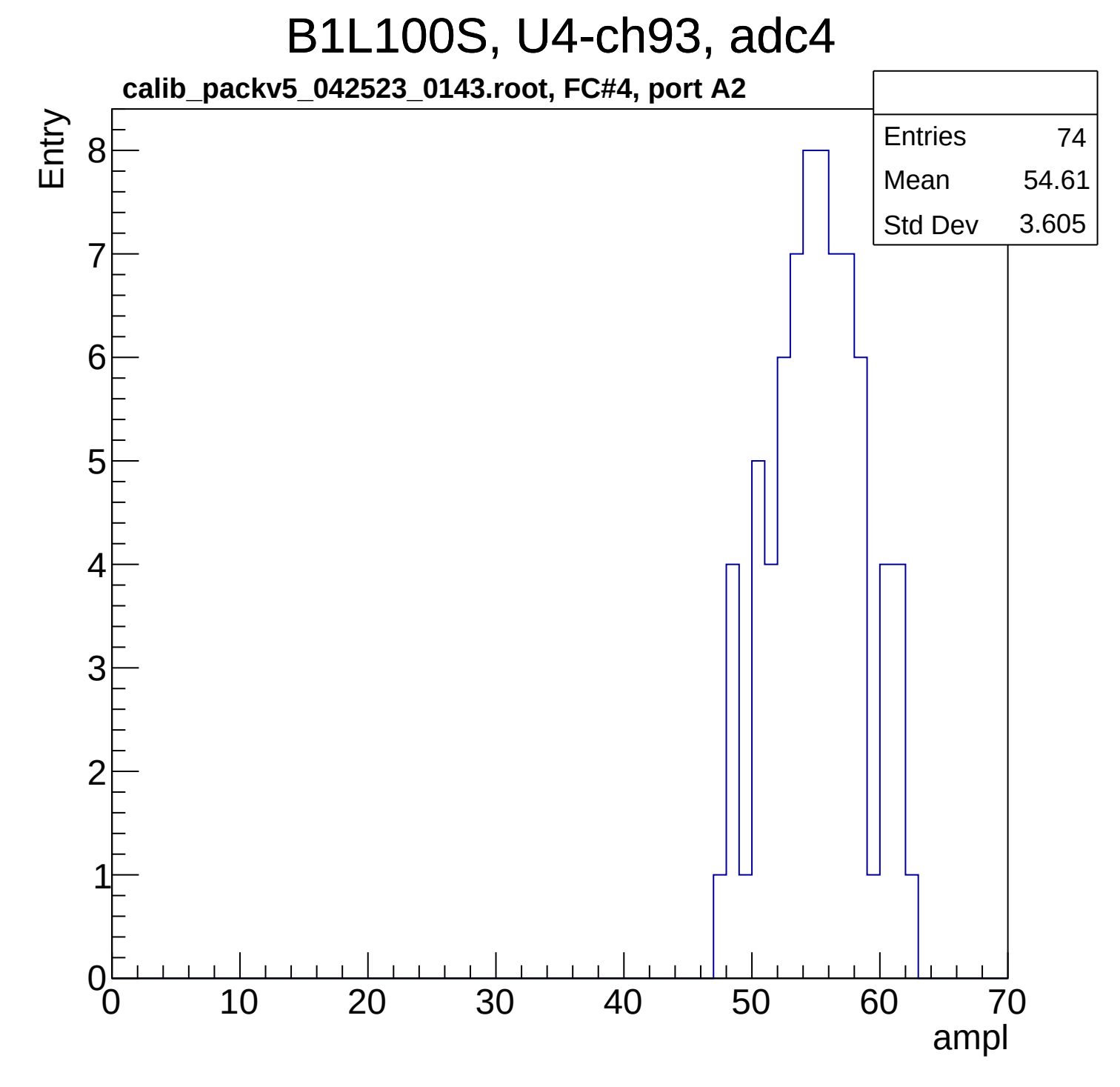

B1L100S, U4-ch92, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 11
Std Dev 11
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

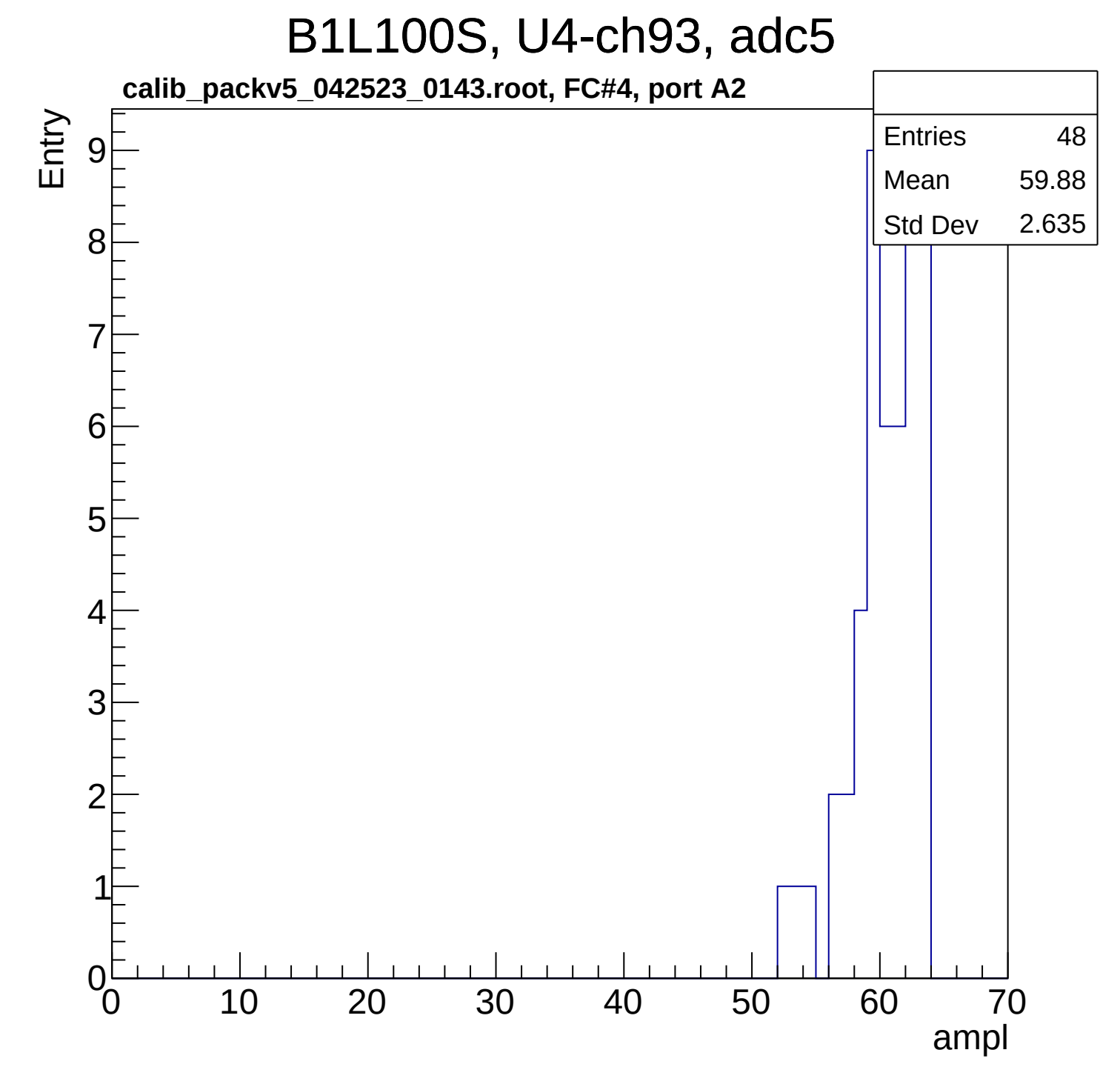

B1L100S, U4-ch93, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 87
Mean 27.52
Std Dev 3.763
Gaus mean : 28.1822
Gaus Width: 3.9015
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

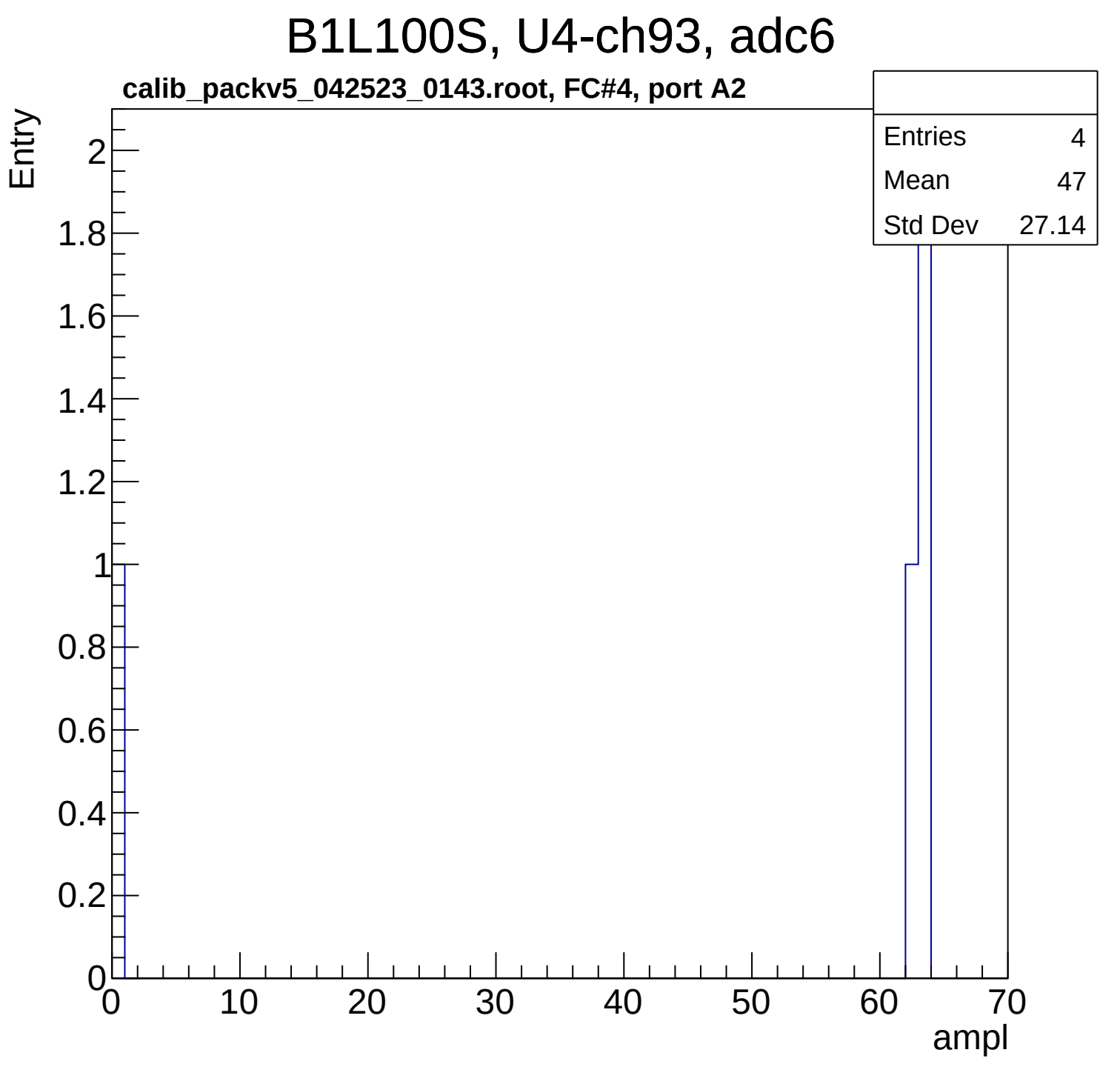

B1L100S, U4-ch93, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 35.45
Std Dev 3.968
Gaus mean : 35.9079
Gaus Width: 4.2046
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

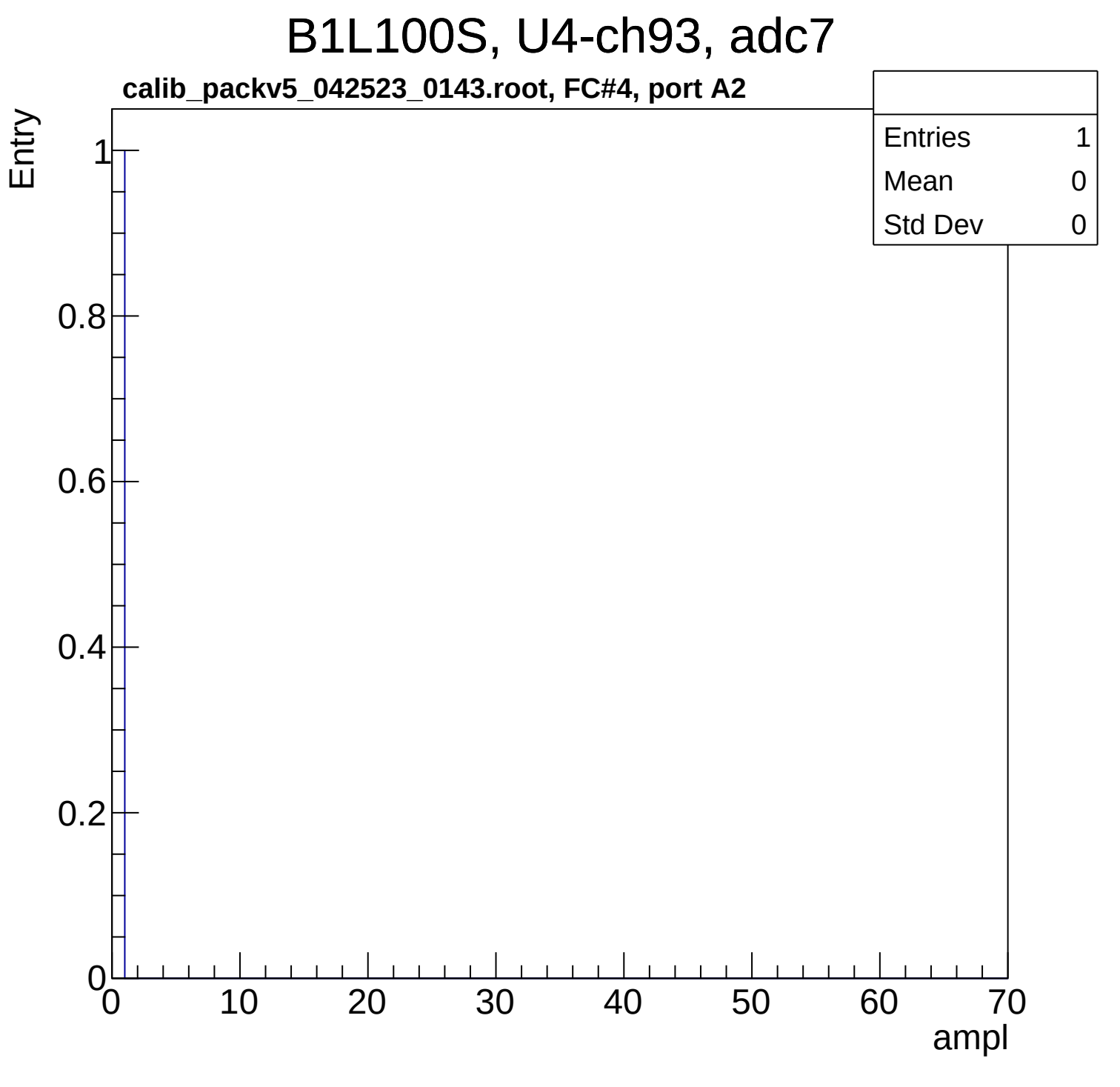

B1L100S, U4-ch93, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 42.5
Std Dev 3.322
Gaus mean : 42.1079
Gaus Width: 3.9279
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

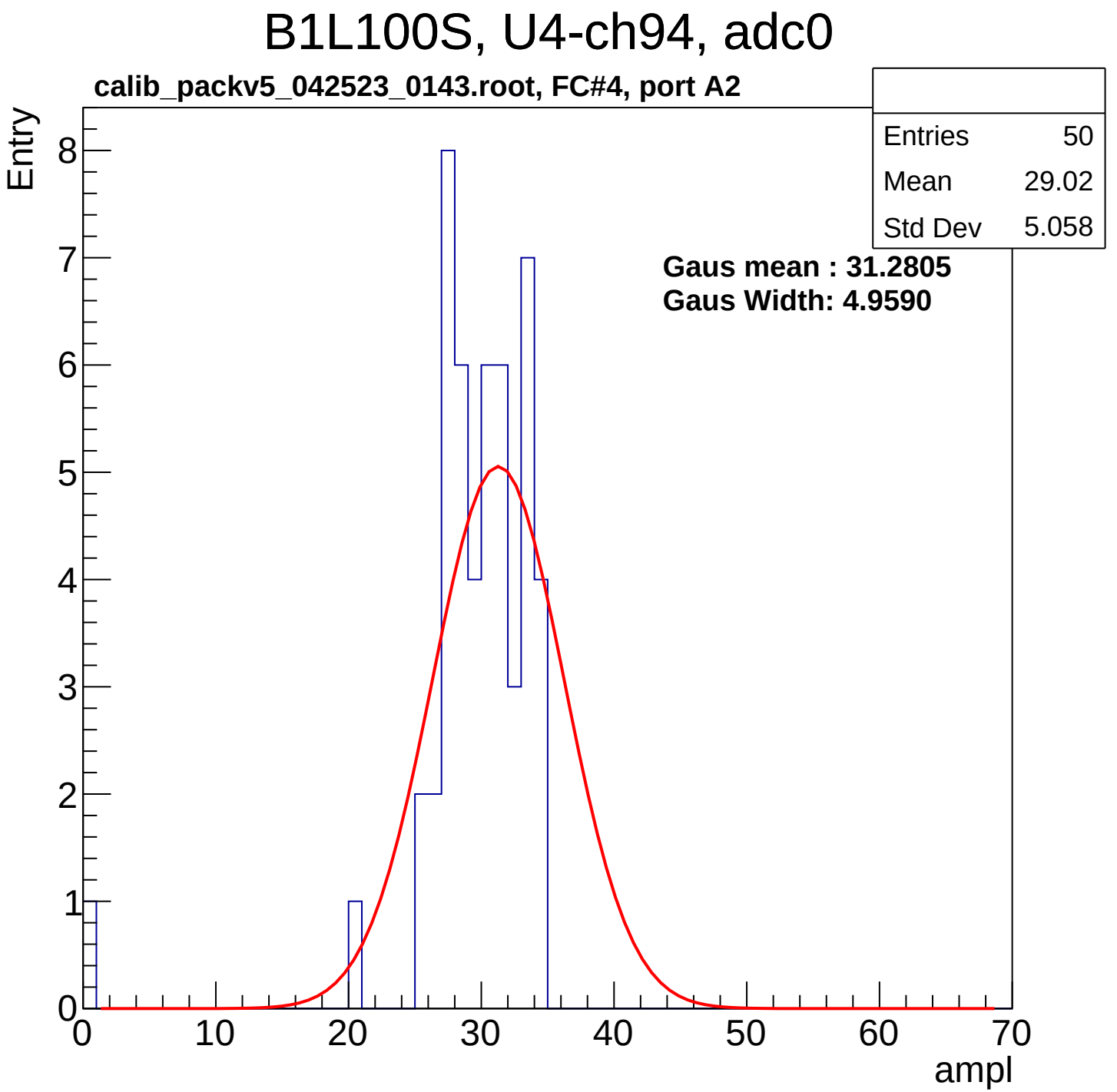

B1L100S, U4-ch93, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 48.73
Std Dev 3.459
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

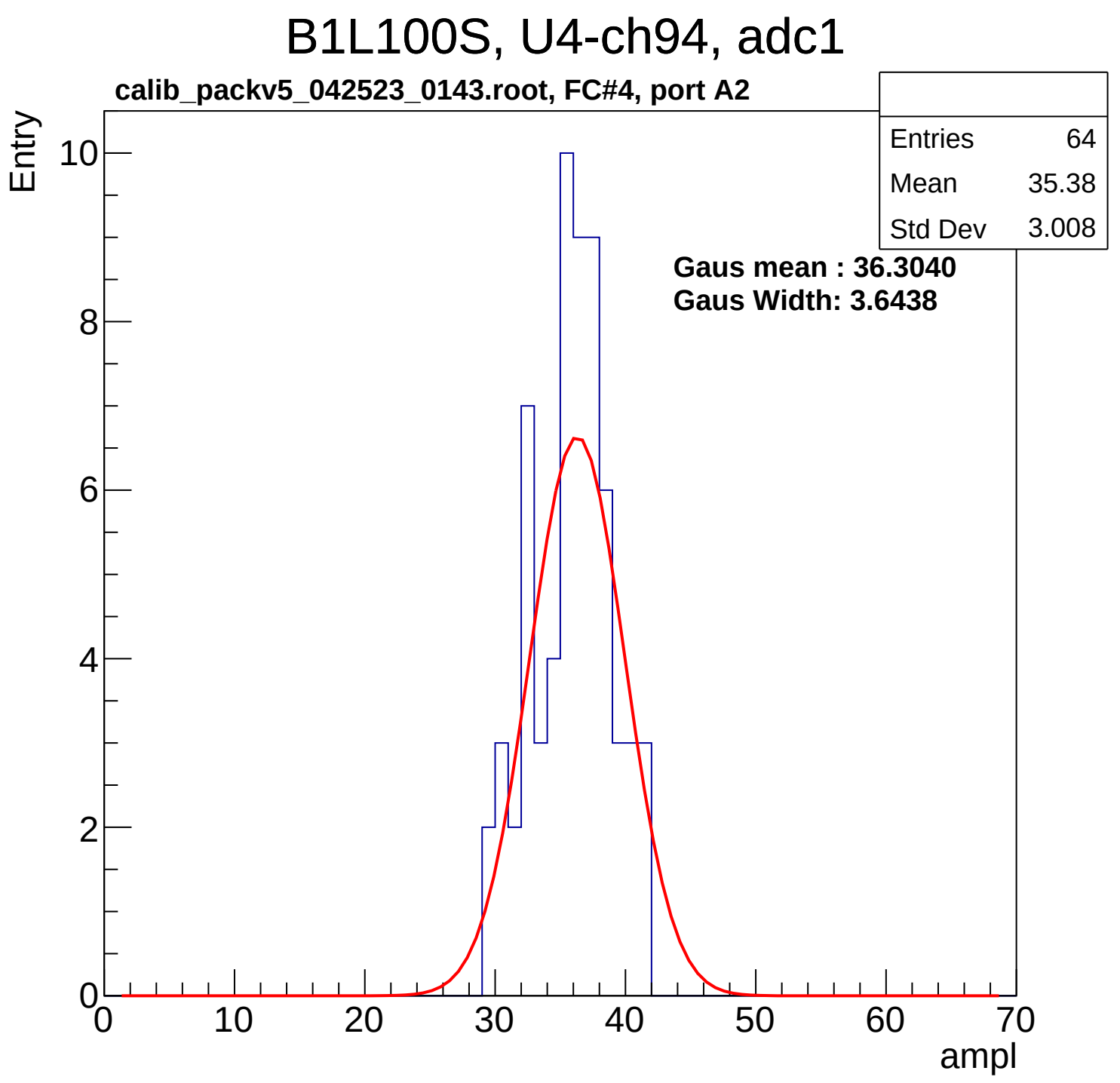

B1L100S, U4-ch93, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 54.61
Std Dev 3.605
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

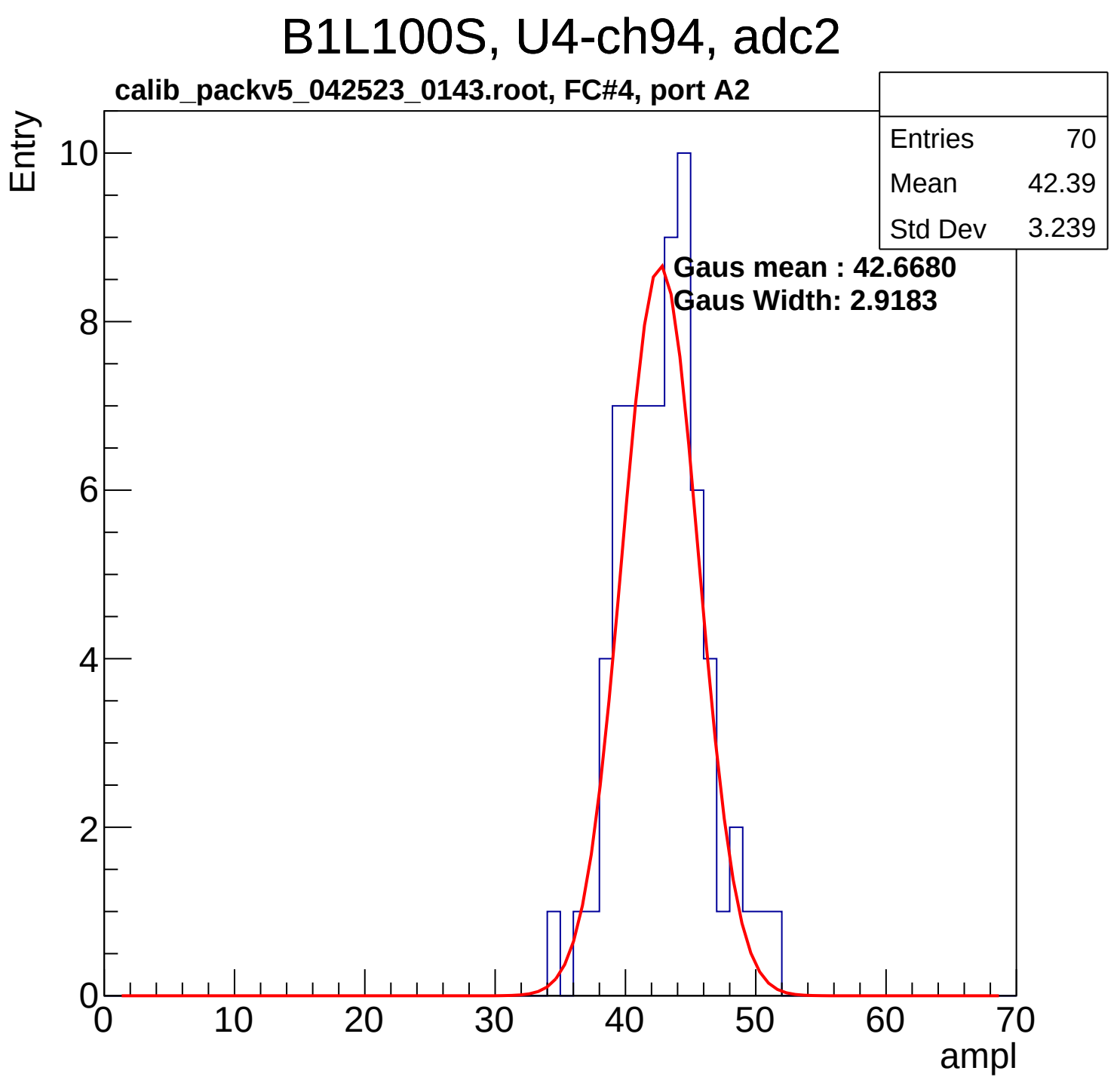

B1L100S, U4-ch93, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 59.88
Std Dev 2.635
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

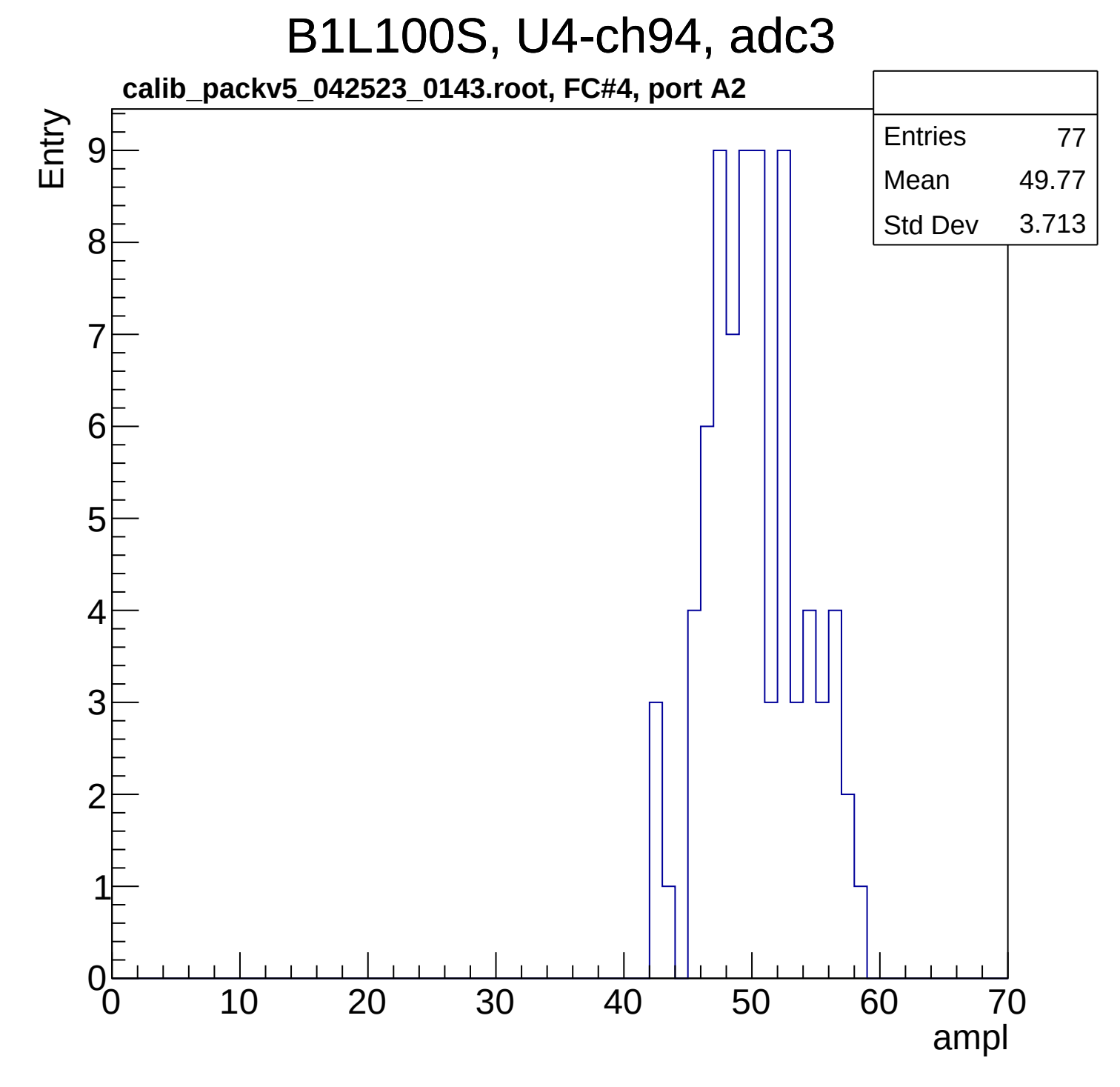

B1L100S, U4-ch93, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 47
Std Dev 27.14
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

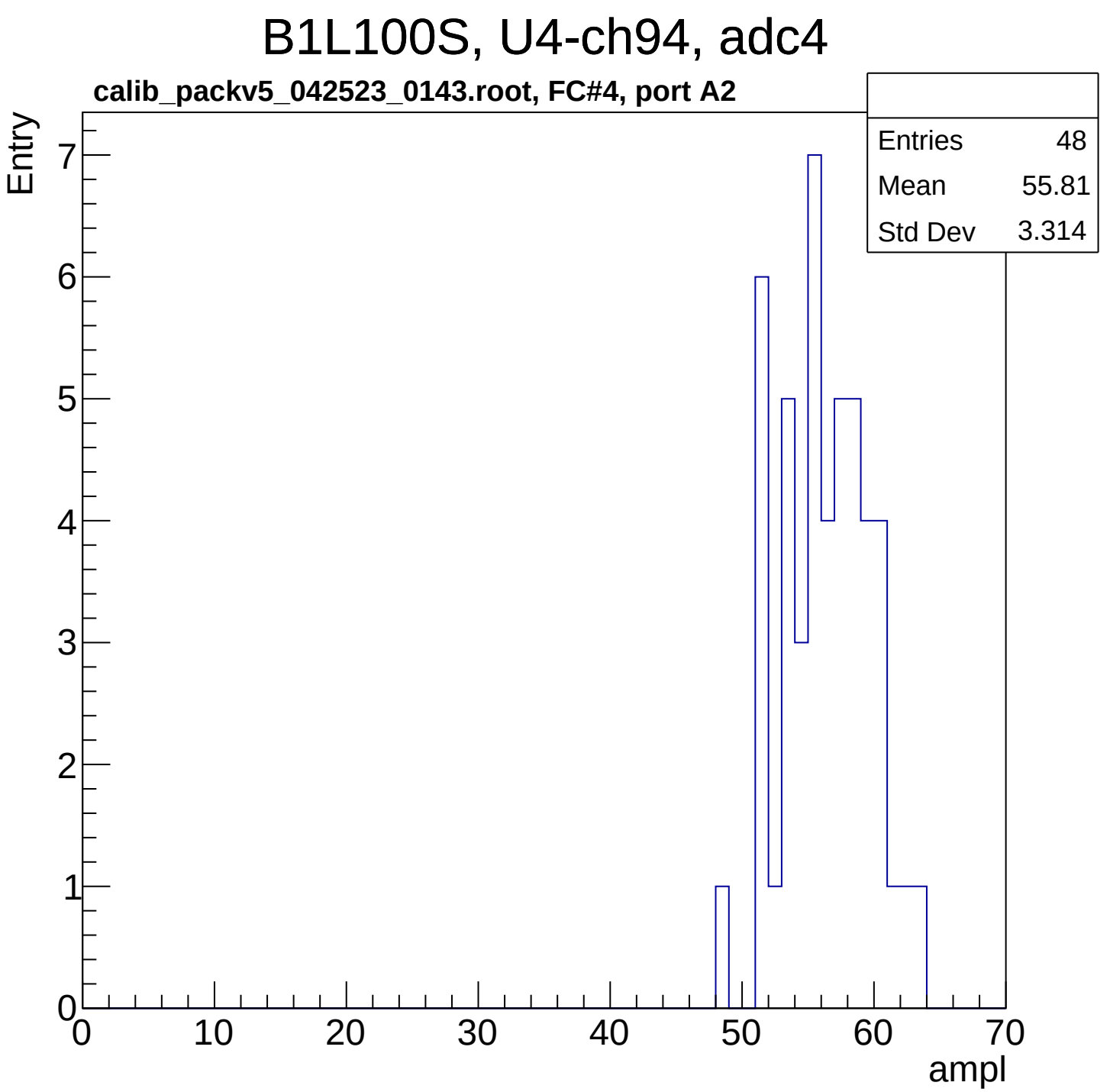

B1L100S, U4-ch93, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

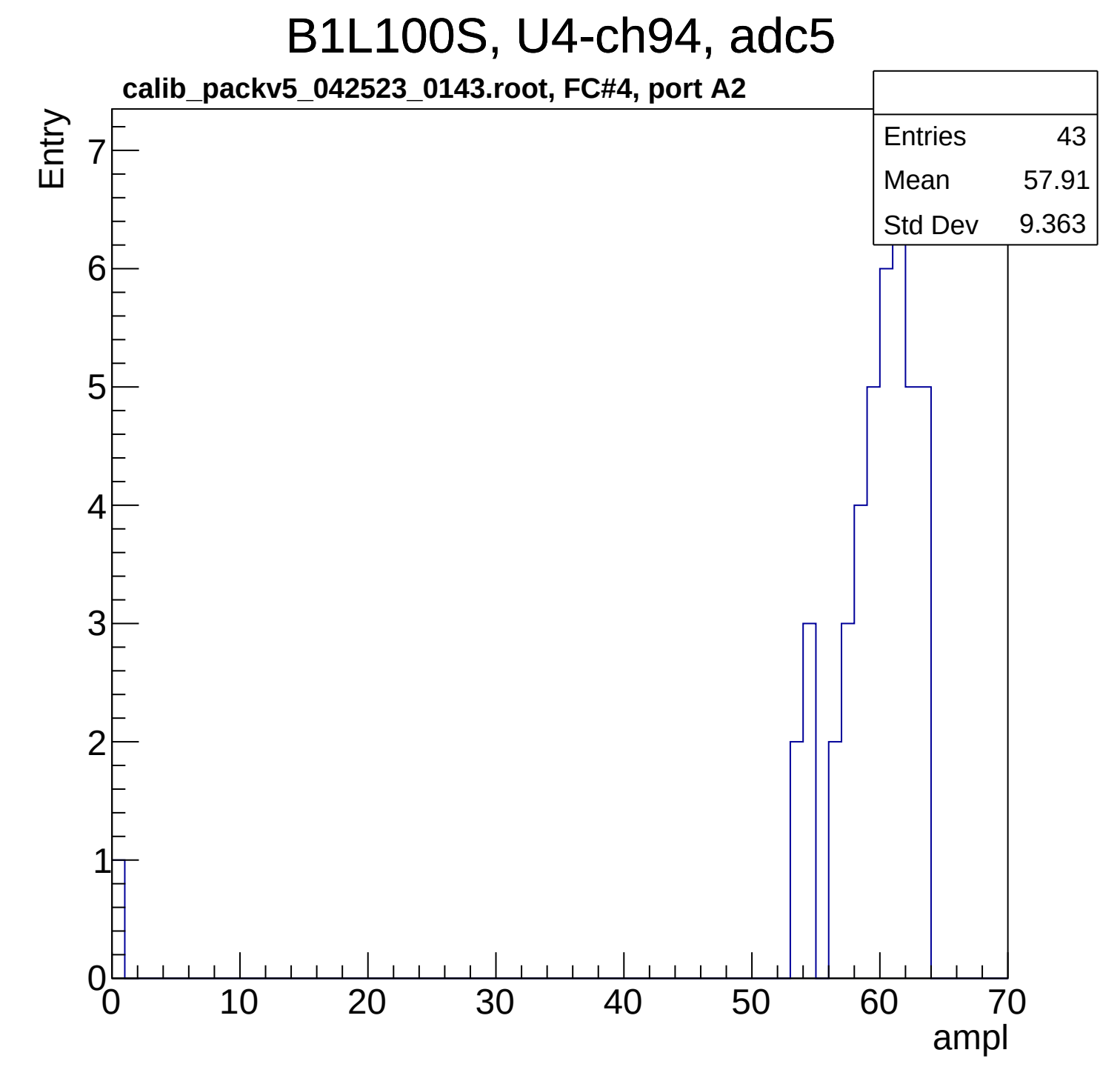

B1L100S, U4-ch94, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 29.02
Std Dev 5.058
Gaus mean : 31.2805
Gaus Width: 4.9590
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

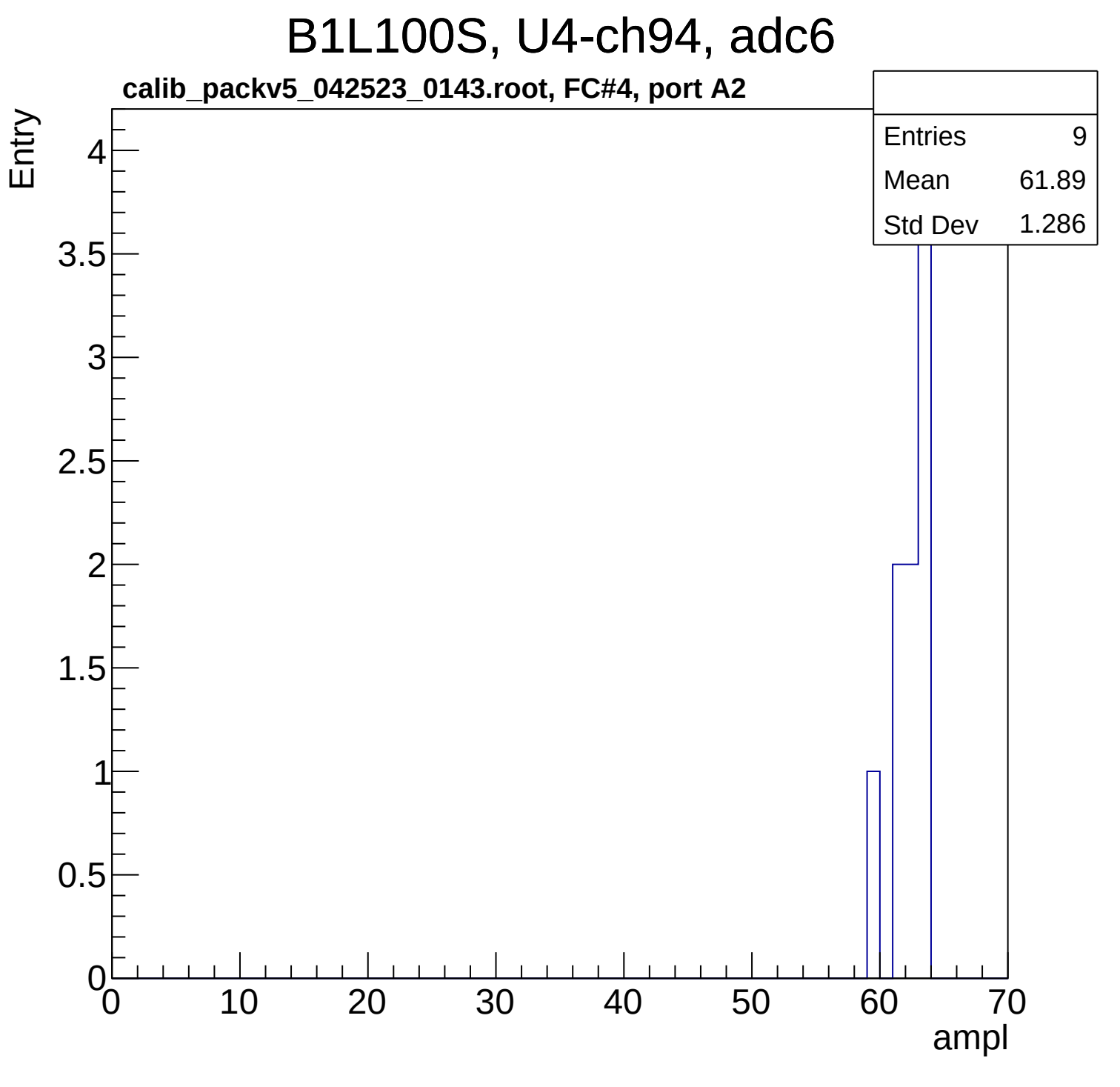

B1L100S, U4-ch94, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 35.38
Std Dev 3.008
Gaus mean : 36.3040
Gaus Width: 3.6438
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

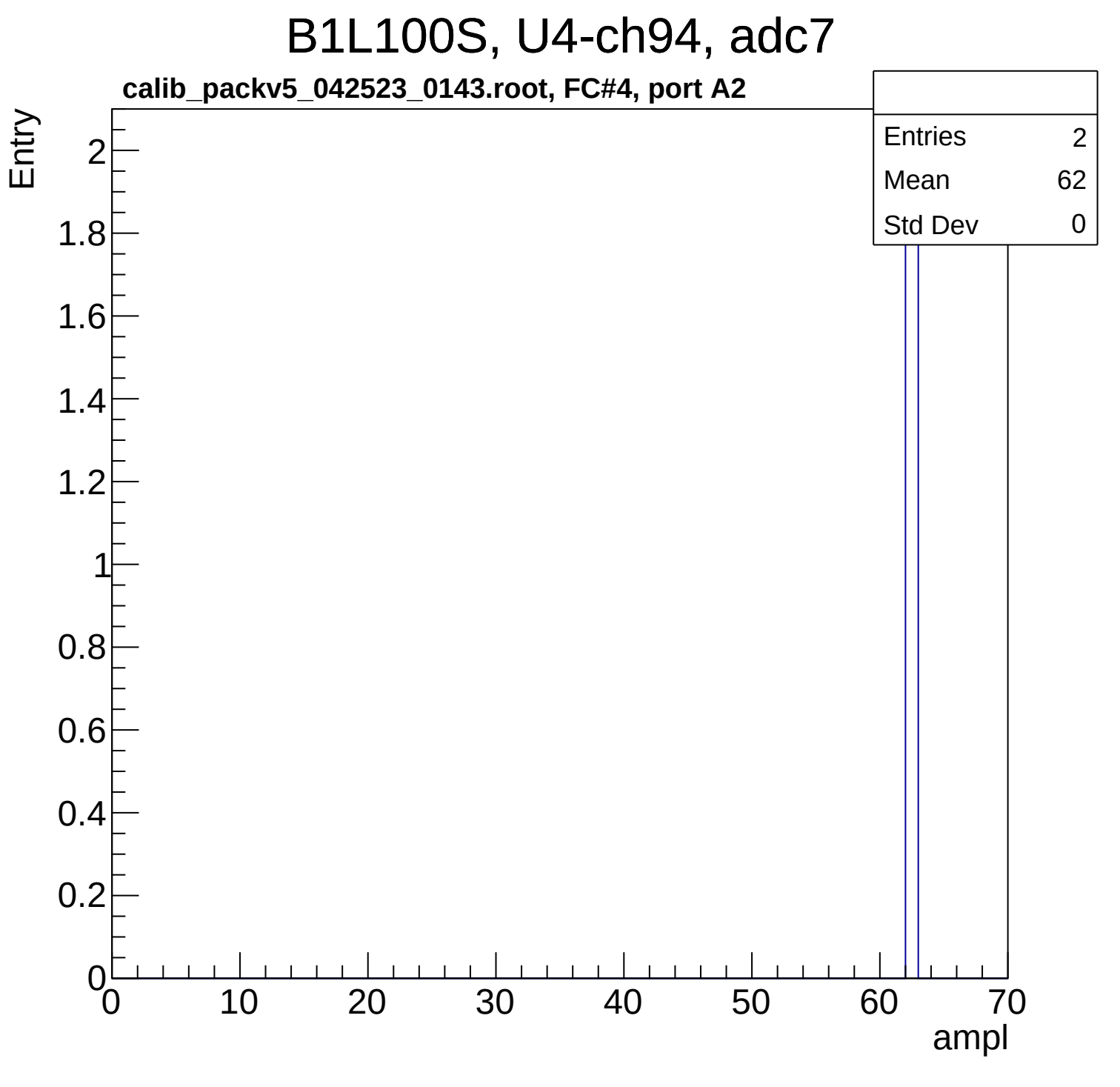

B1L100S, U4-ch94, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 42.39
Std Dev 3.239
Gaus mean : 42.6680
Gaus Width: 2.9183
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

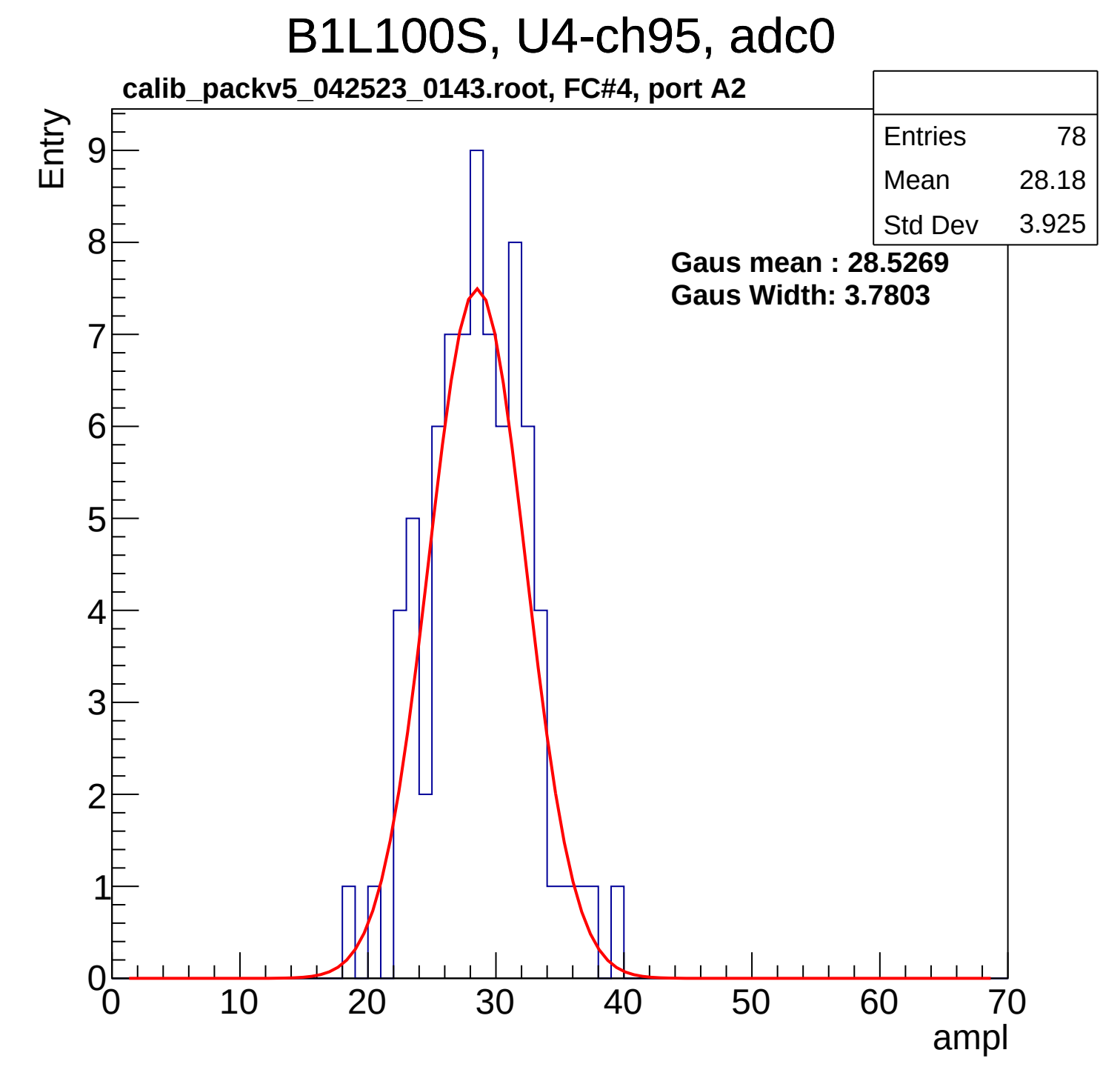

B1L100S, U4-ch94, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 49.77
Std Dev 3.713
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

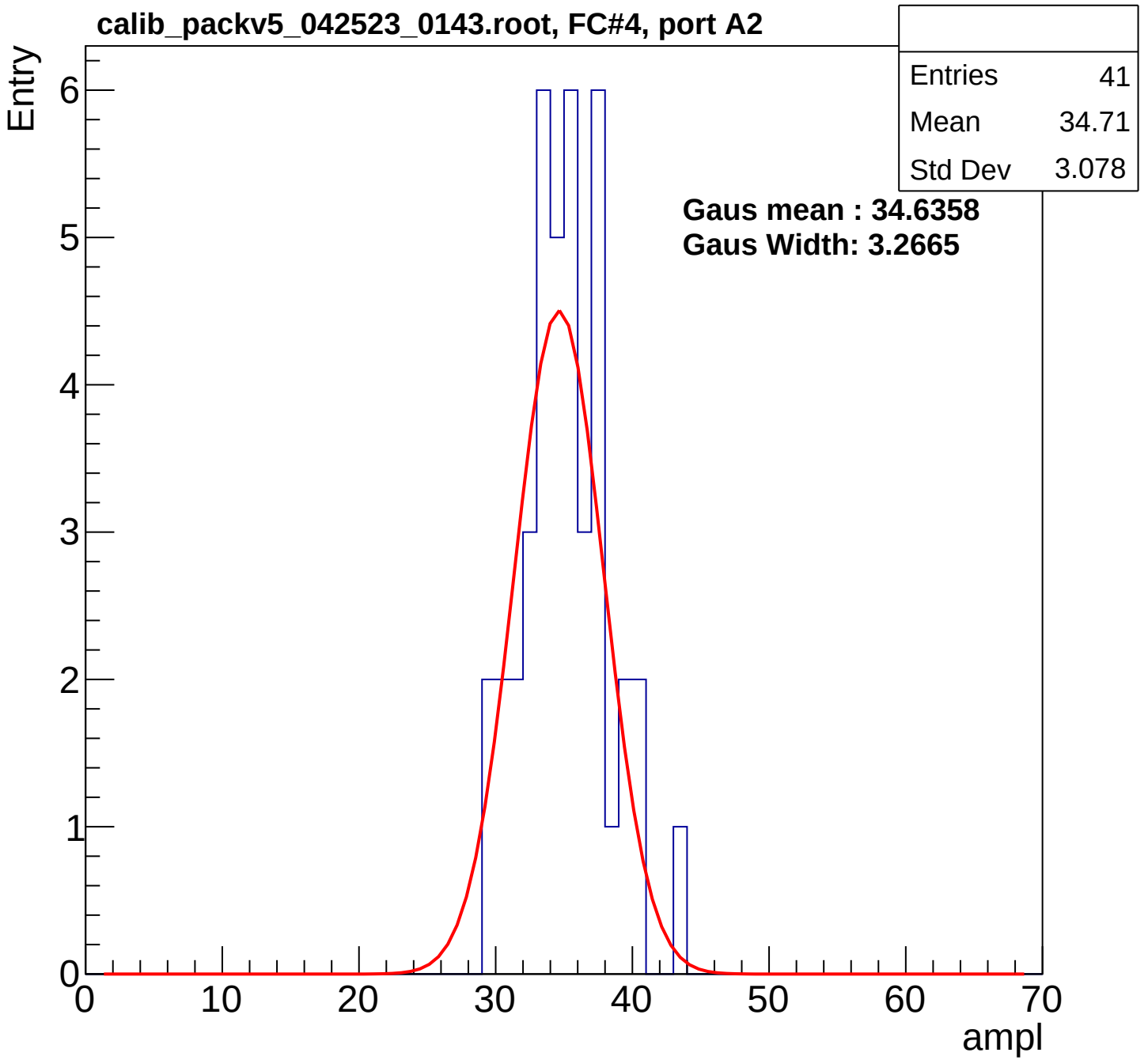

B1L100S, U4-ch94, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 55.81
Std Dev 3.314
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

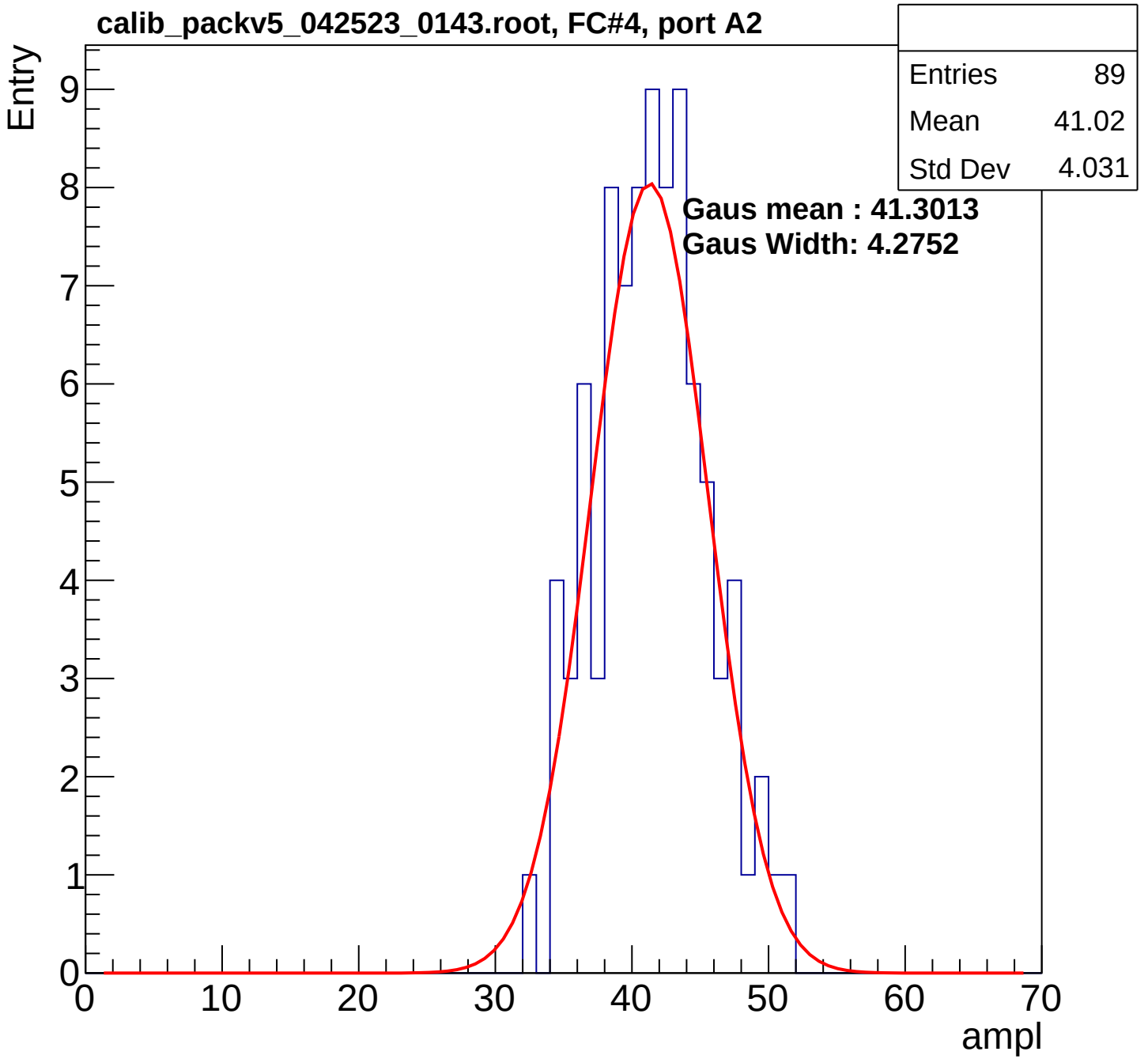

B1L100S, U4-ch94, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 57.91
Std Dev 9.363
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

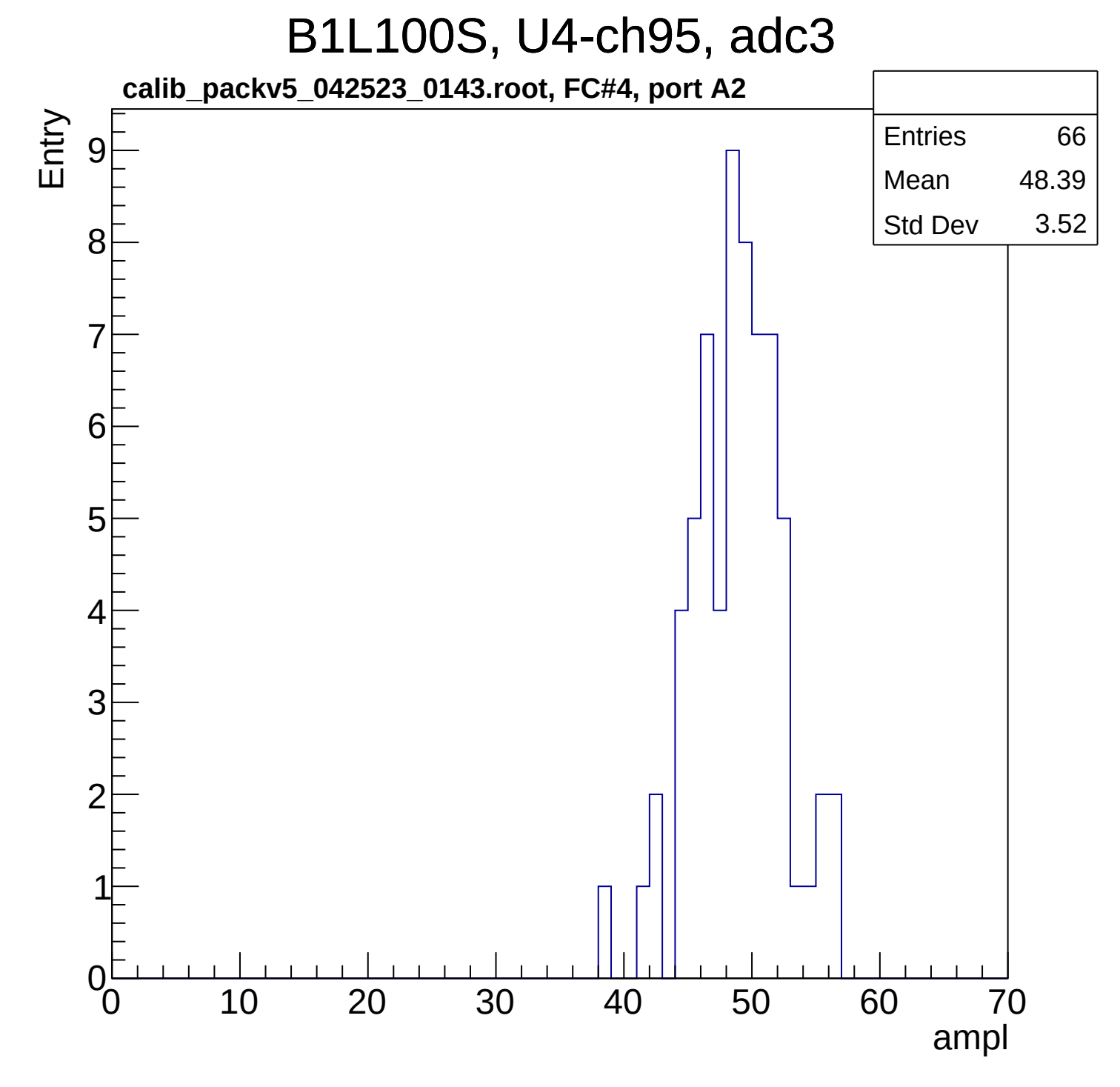

B1L100S, U4-ch94, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 61.89
Std Dev 1.286
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

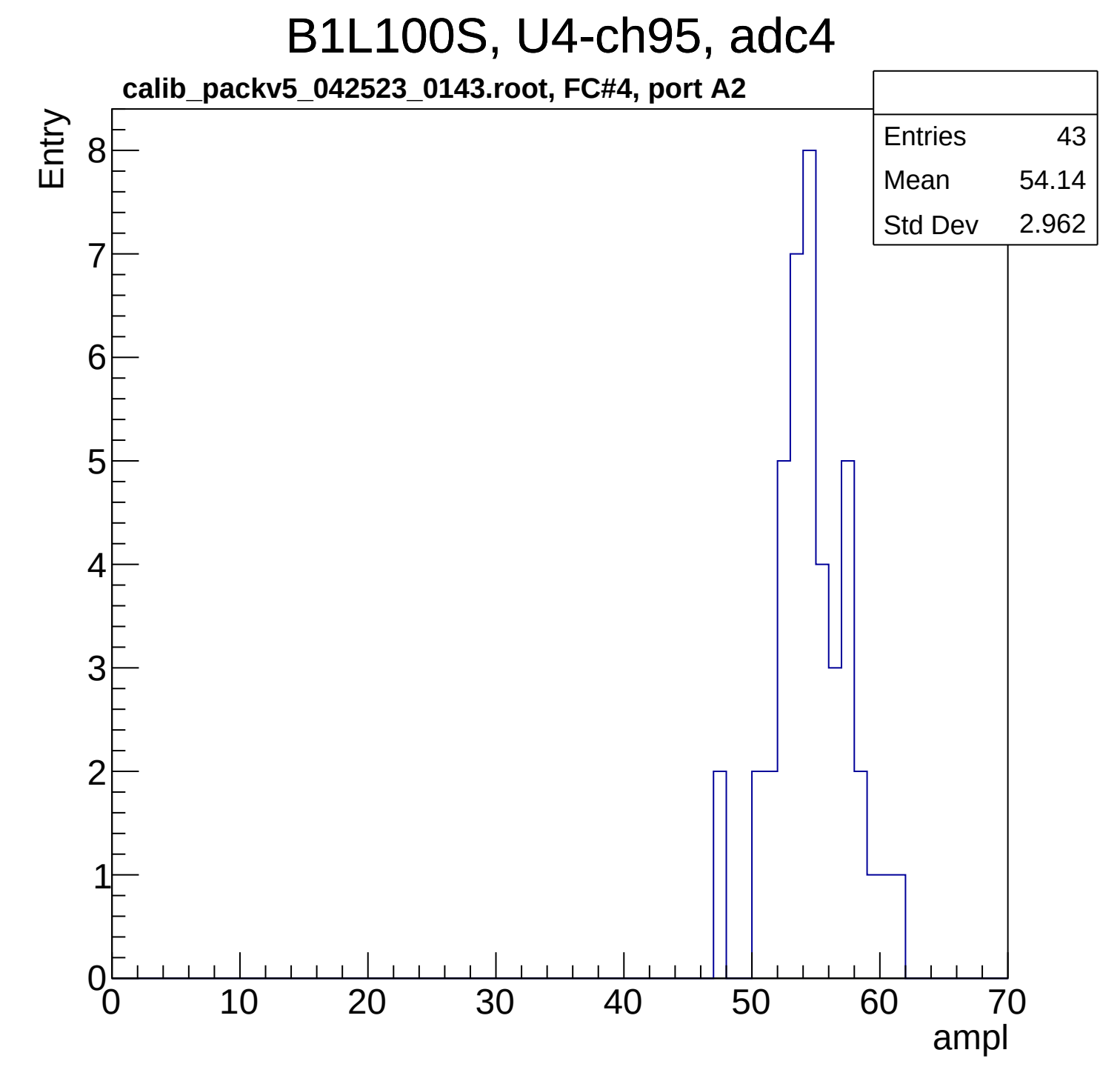

B1L100S, U4-ch94, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 62
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

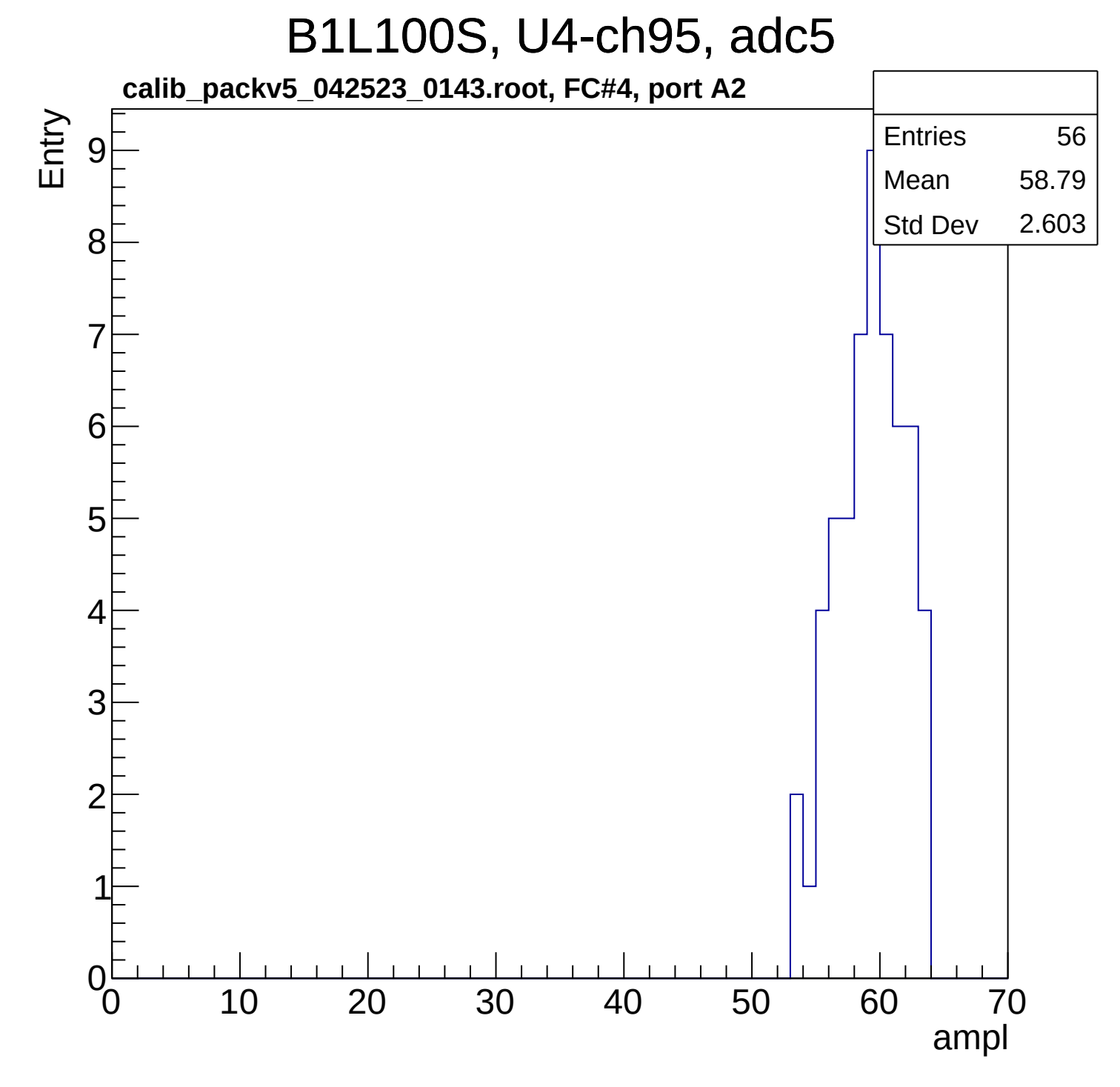

B1L100S, U4-ch95, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 28.18
Std Dev 3.925
Gaus mean : 28.5269
Gaus Width: 3.7803
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

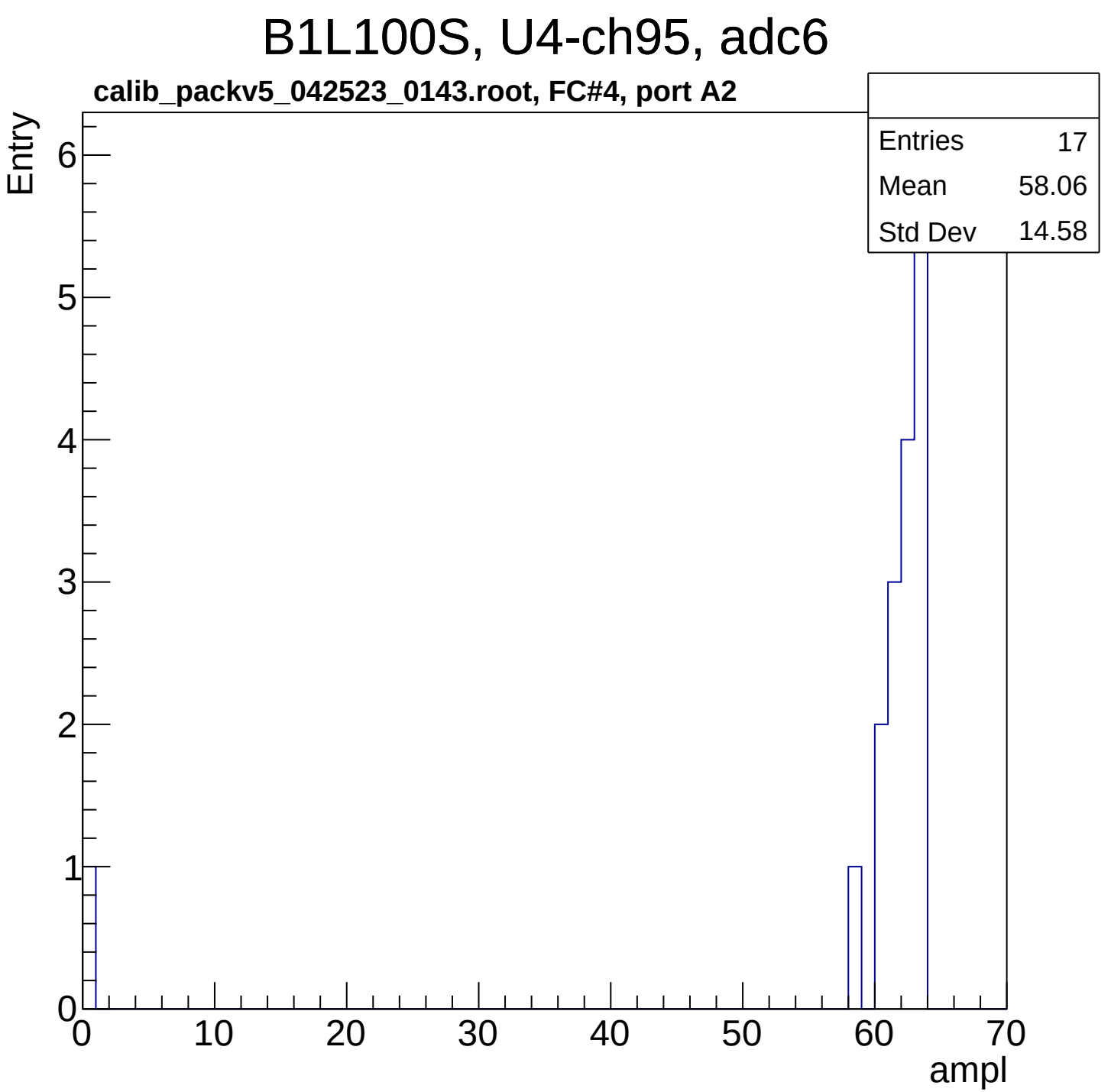

B1L100S, U4-ch95, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 41
Mean 34.71
Std Dev 3.078
Gaus mean : 34.6358
Gaus Width: 3.2665
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

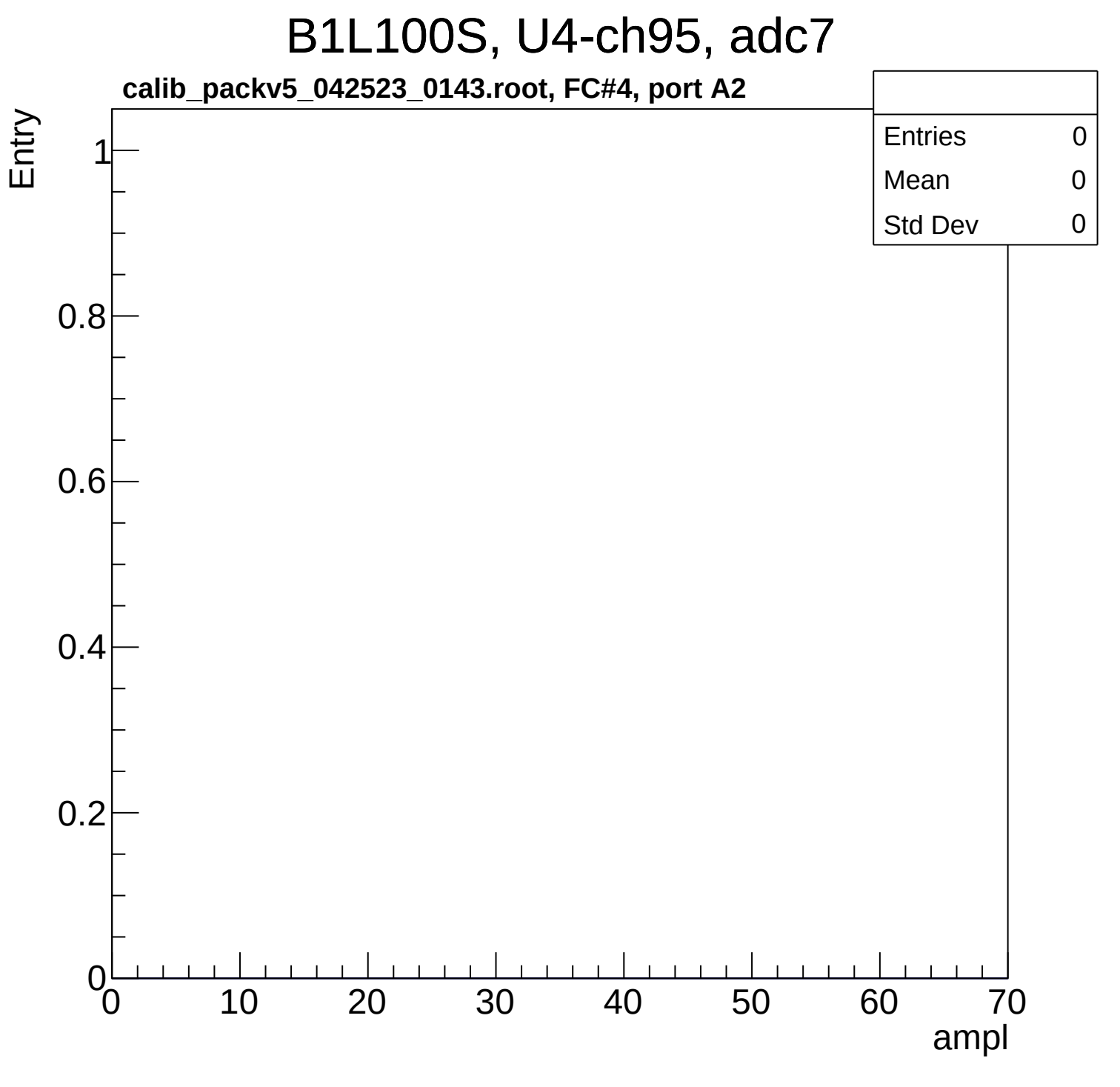

B1L100S, U4-ch95, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 89
Mean 41.02
Std Dev 4.031
Gaus mean : 41.3013
Gaus Width: 4.2752
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

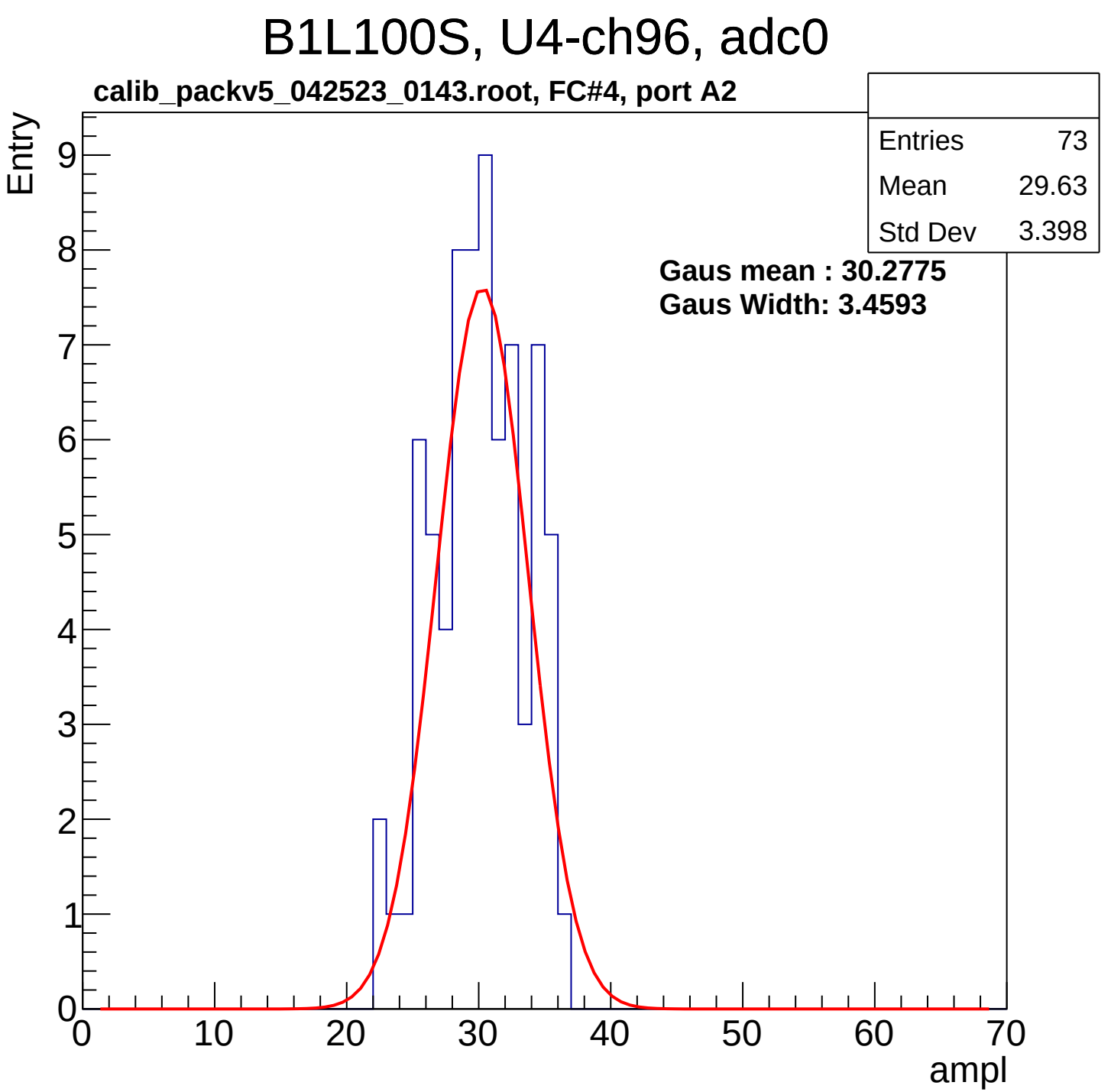

B1L100S, U4-ch95, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 48.39
Std Dev 3.52
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

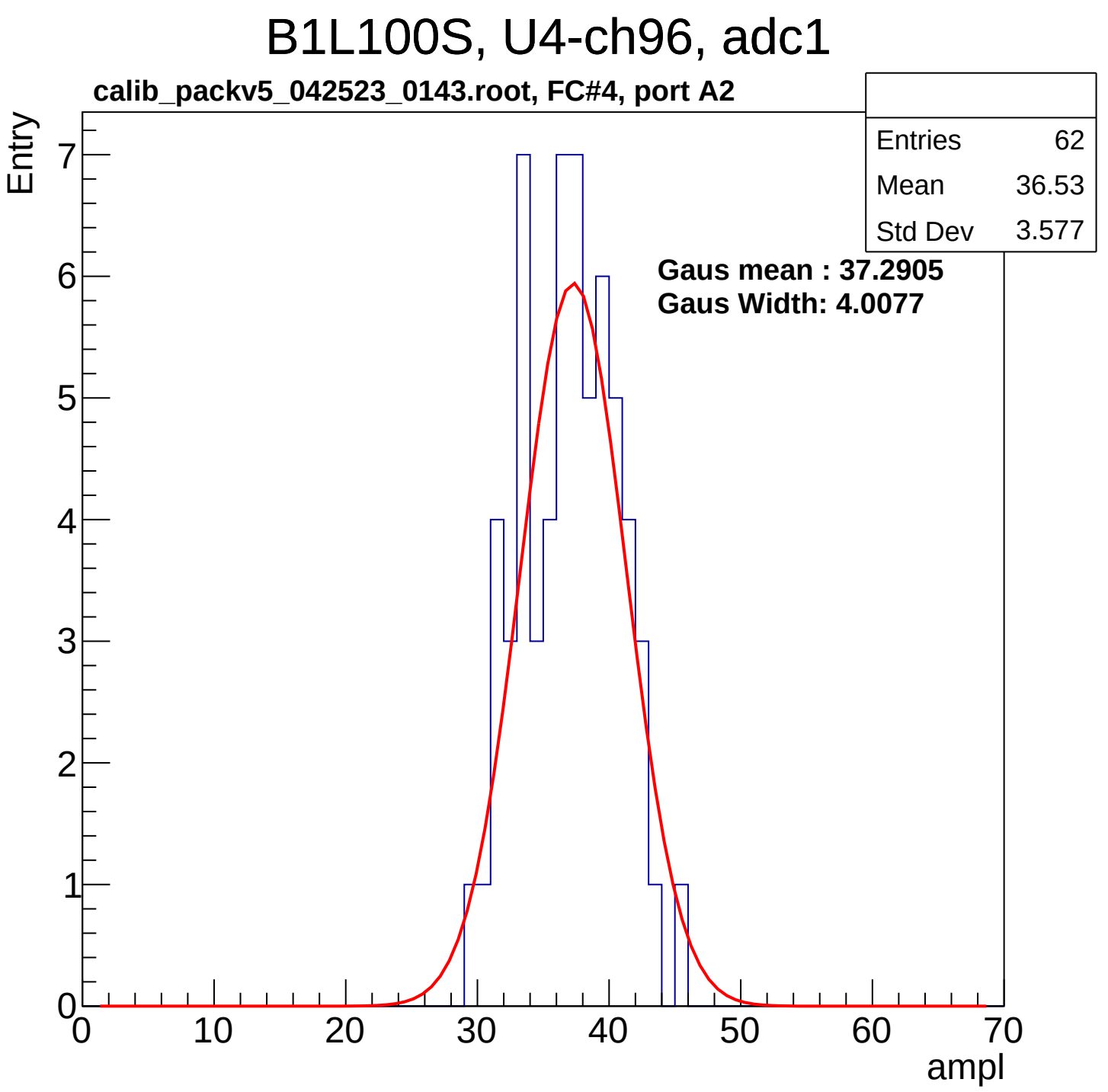

B1L100S, U4-ch95, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 54.14
Std Dev 2.962
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

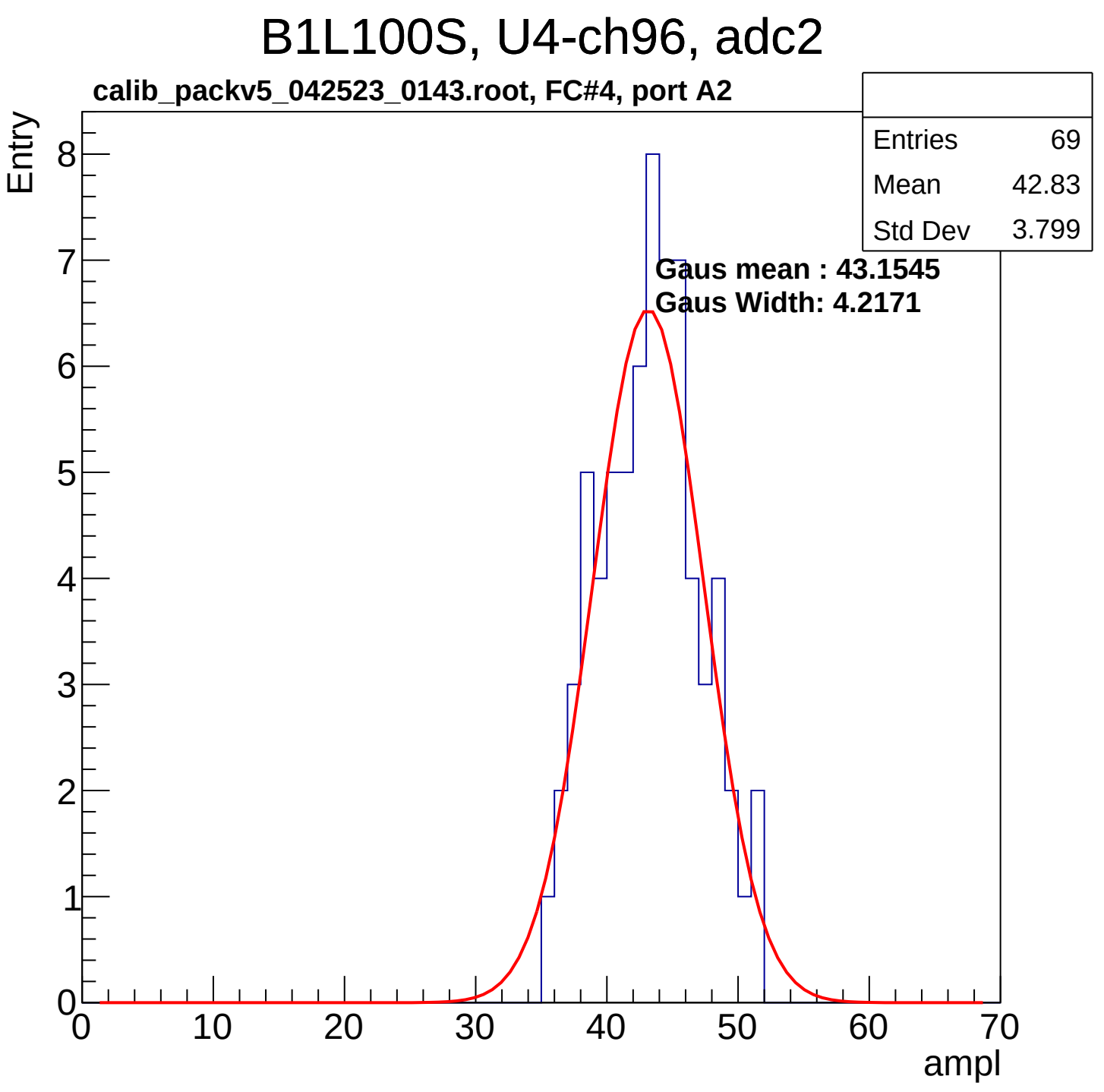

B1L100S, U4-ch95, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 58.79
Std Dev 2.603
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

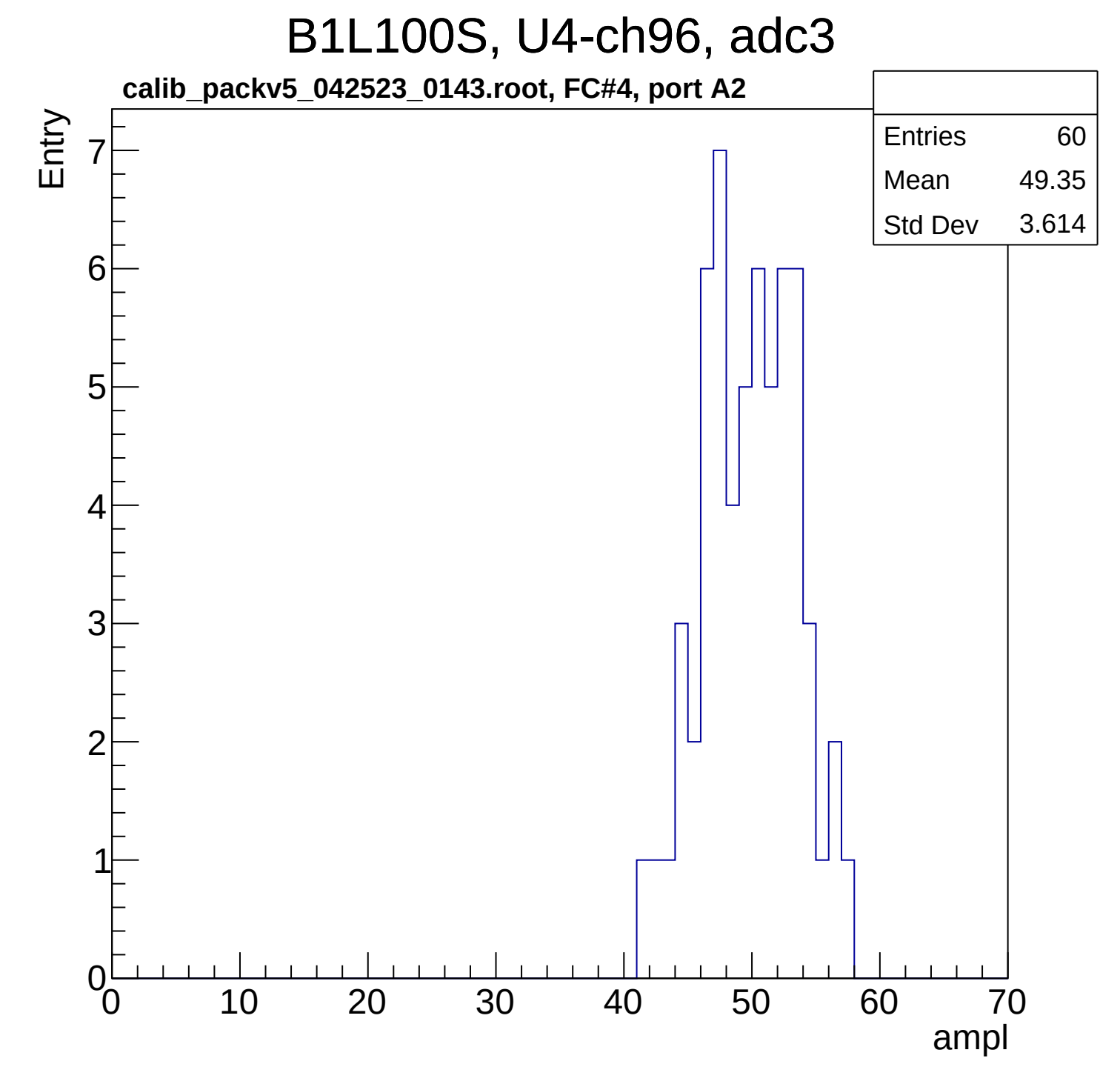

B1L100S, U4-ch95, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 17
Mean 58.06
Std Dev 14.58
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

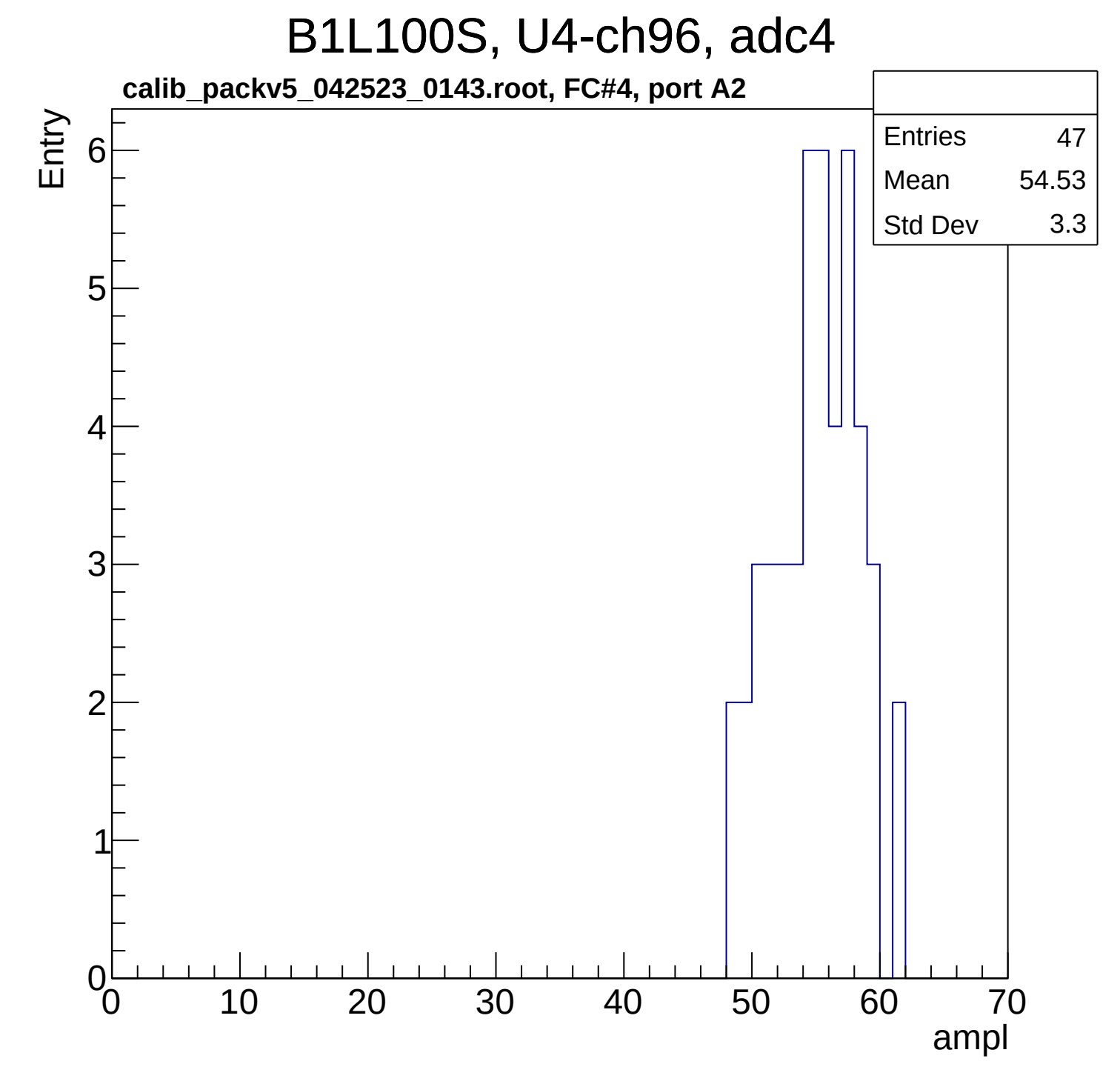

B1L100S, U4-ch95, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

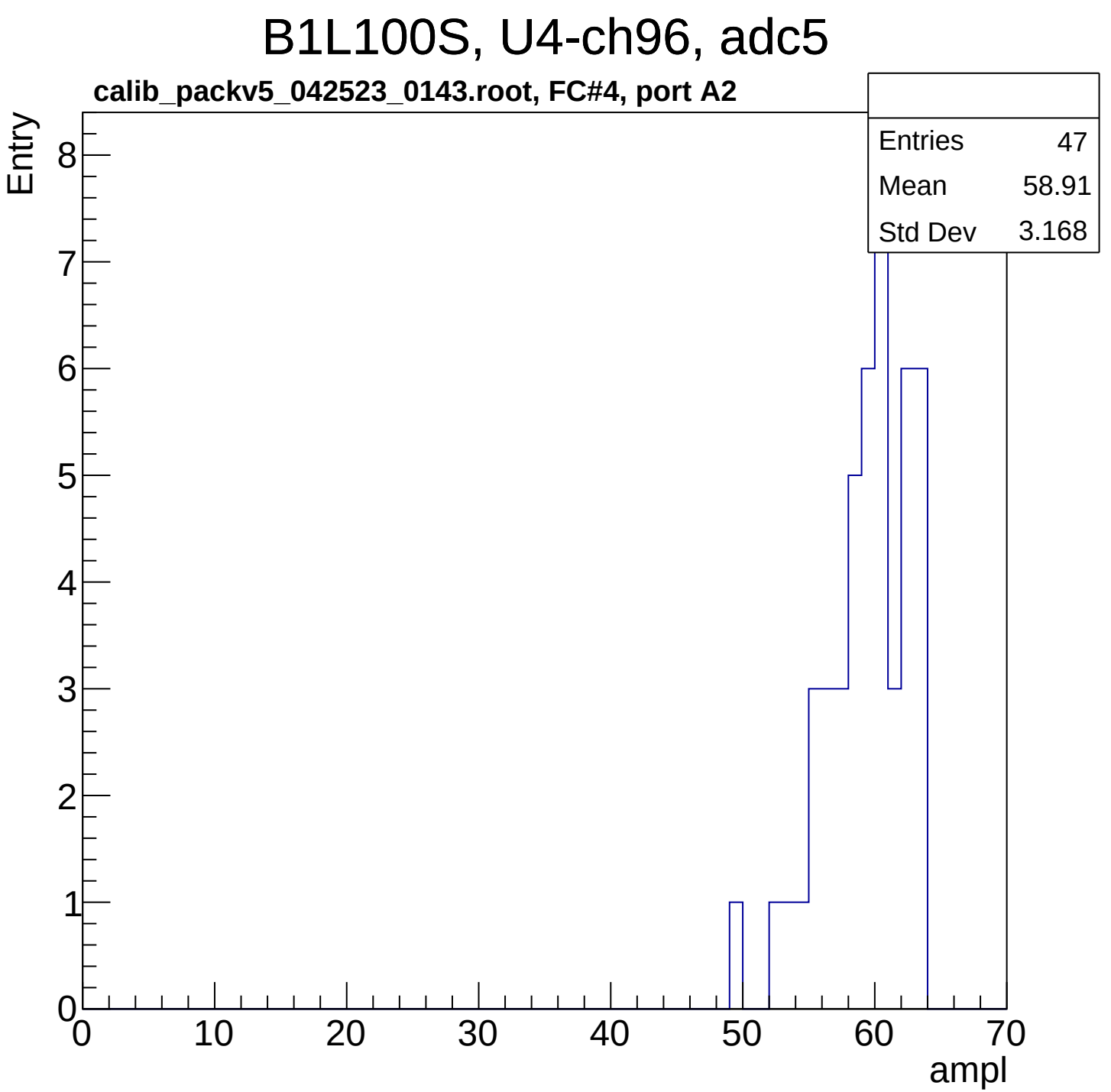

B1L100S, U4-ch96, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 29.63
Std Dev 3.398
Gaus mean : 30.2775
Gaus Width: 3.4593
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

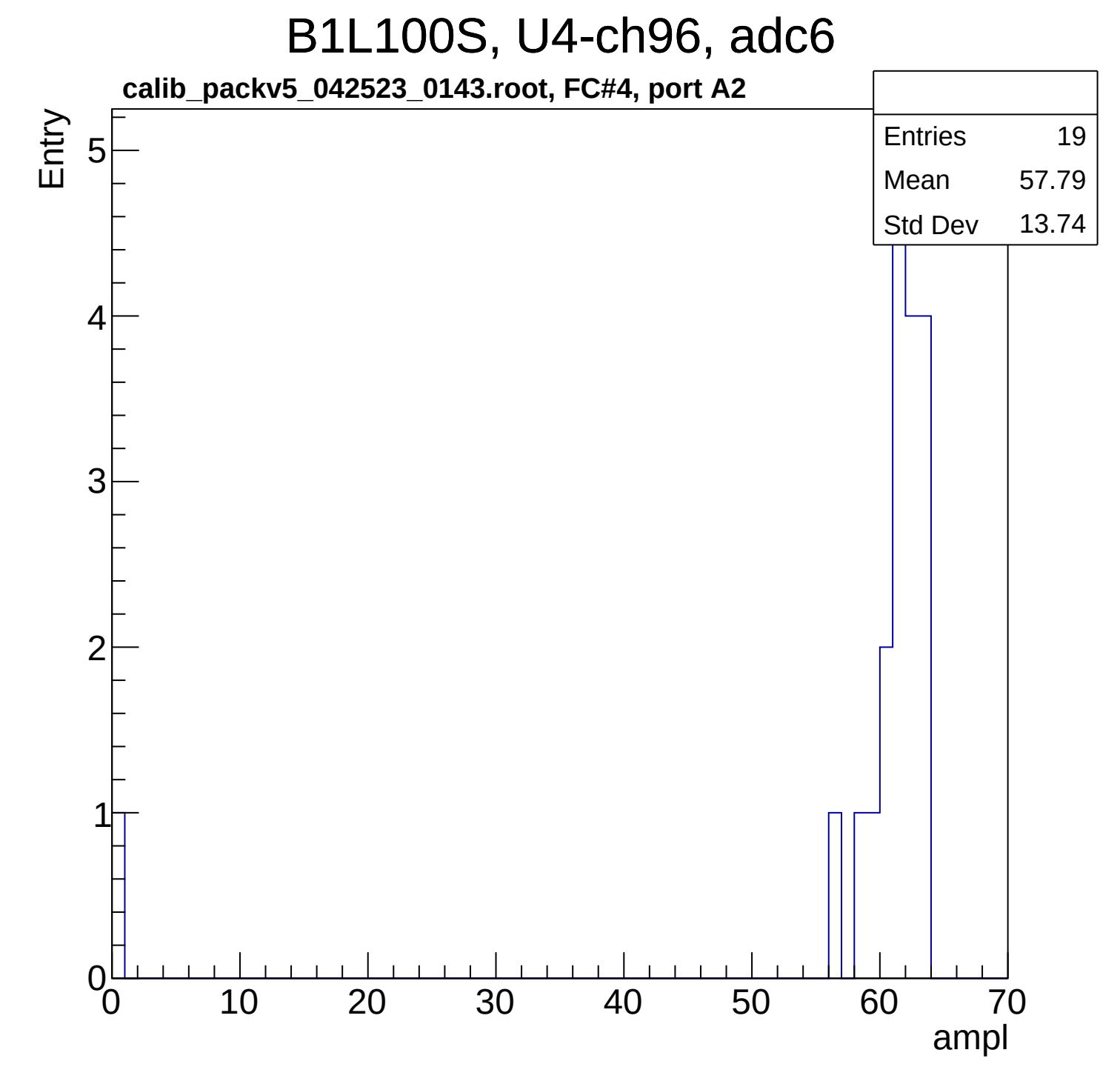

B1L100S, U4-ch96, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 36.53
Std Dev 3.577
Gaus mean : 37.2905
Gaus Width: 4.0077
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

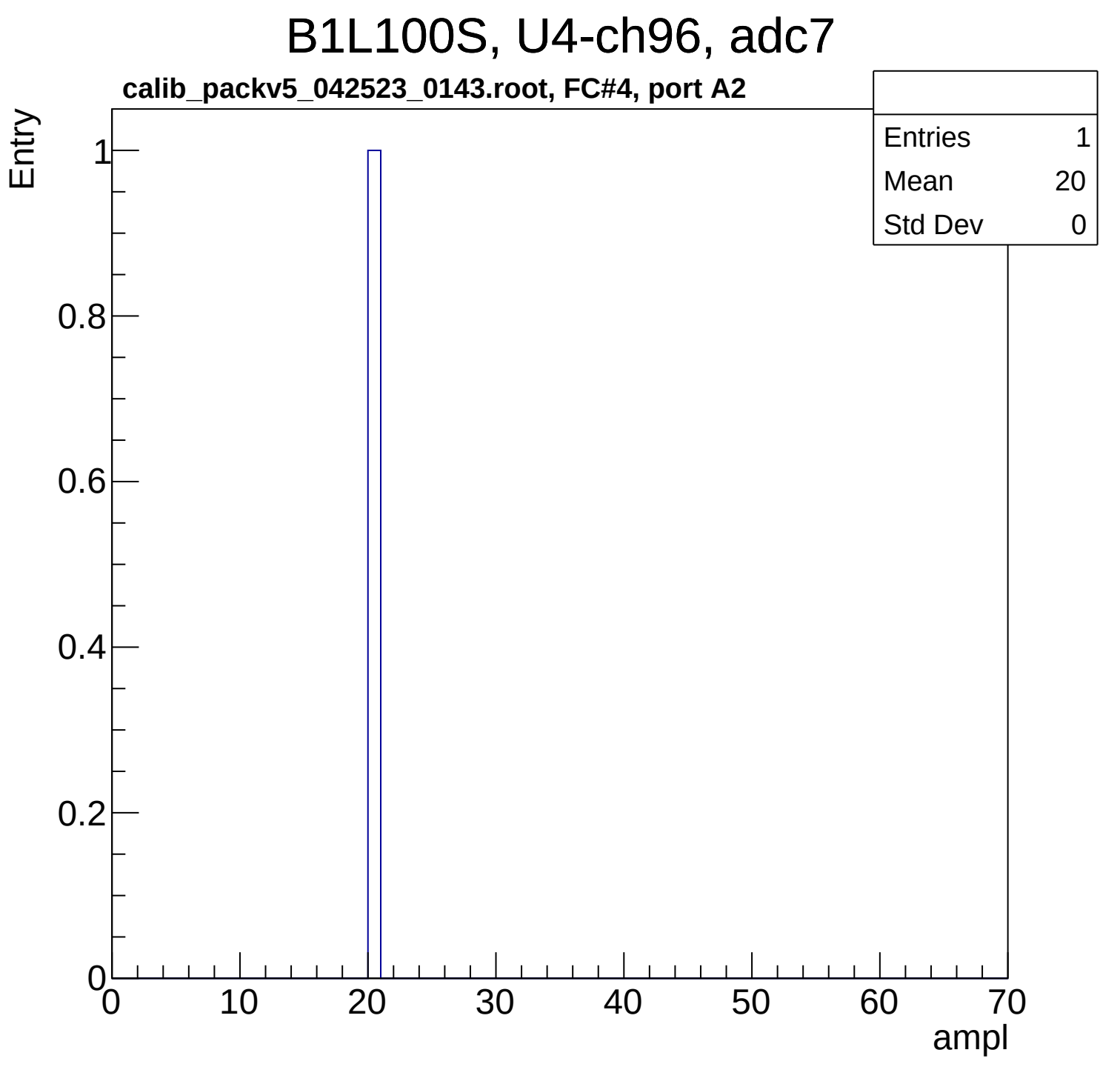

B1L100S, U4-ch96, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 42.83
Std Dev 3.799
Gaus mean : 43.1545
Gaus Width: 4.2171
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

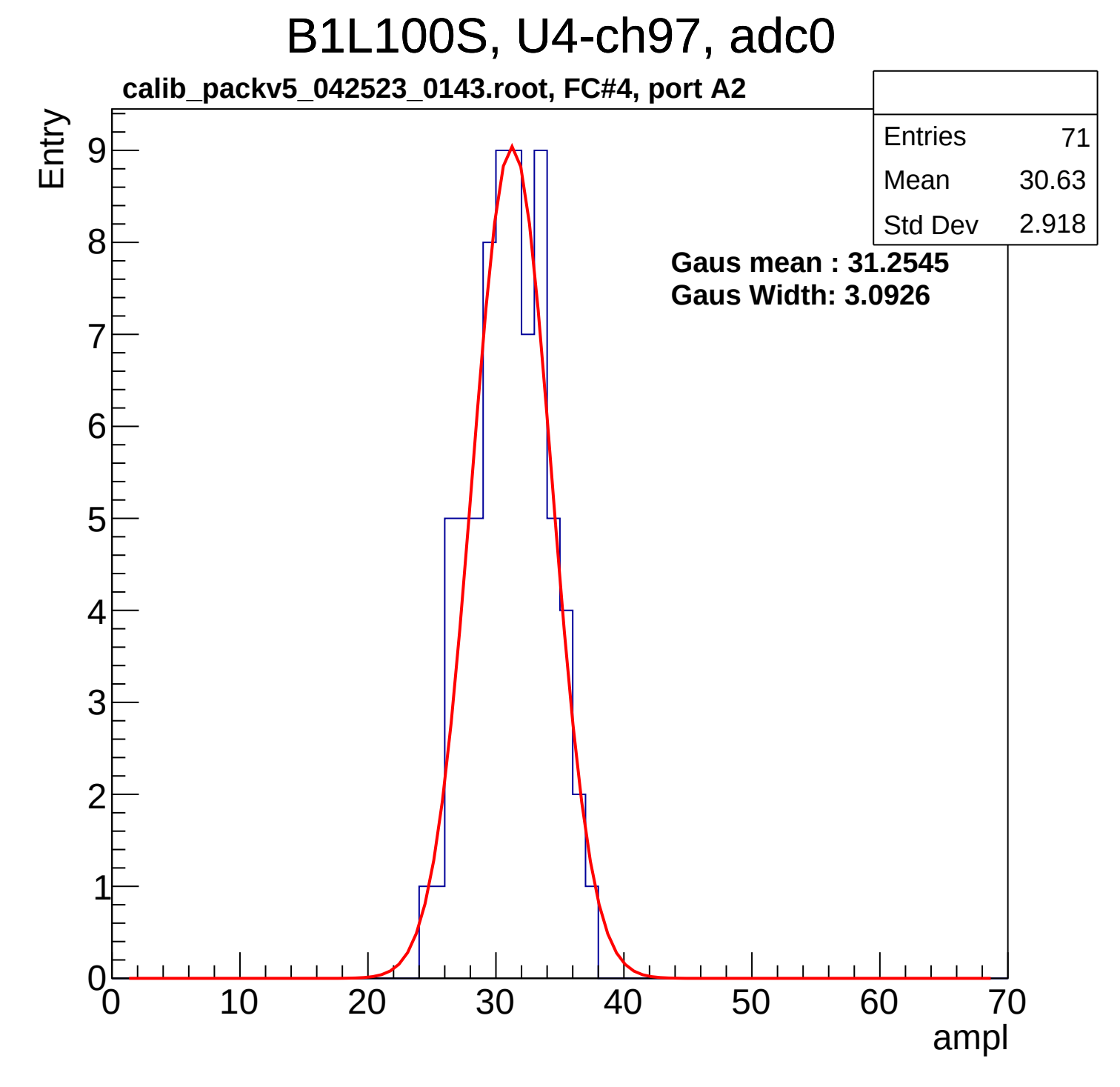

B1L100S, U4-ch96, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 49.35
Std Dev 3.614
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

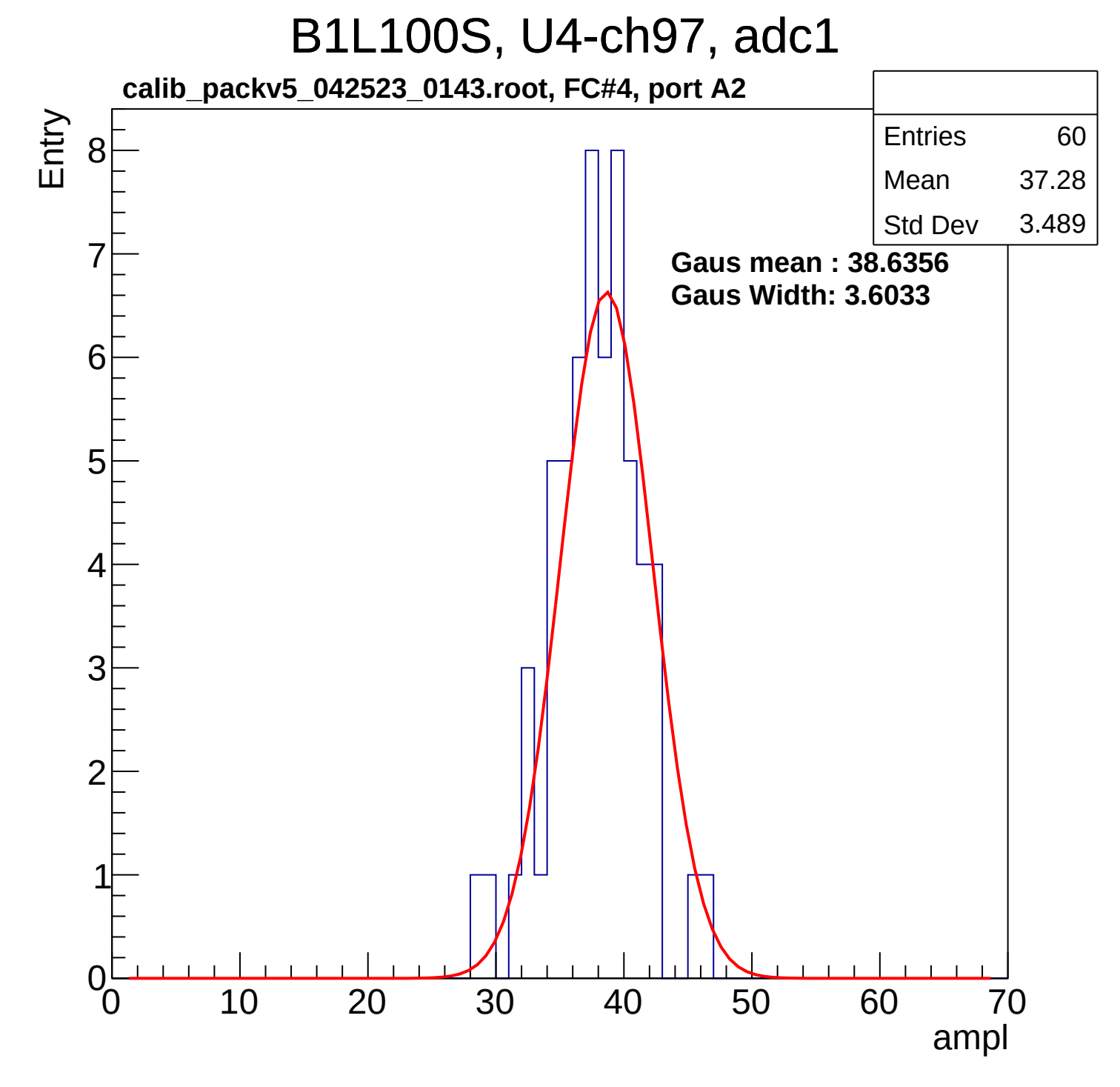

B1L100S, U4-ch96, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 54.53
Std Dev 3.3
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

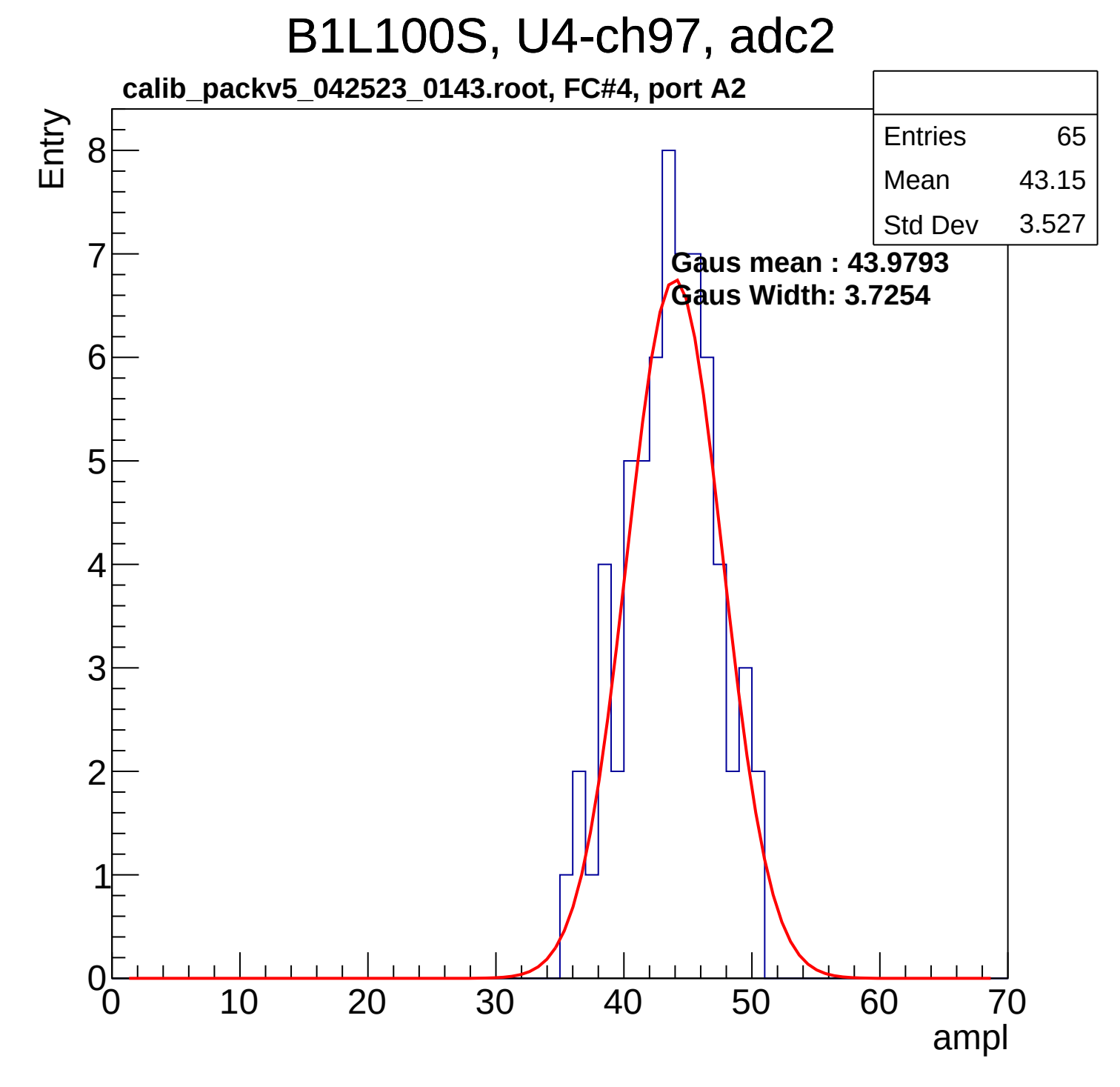

B1L100S, U4-ch96, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 58.91
Std Dev 3.168
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

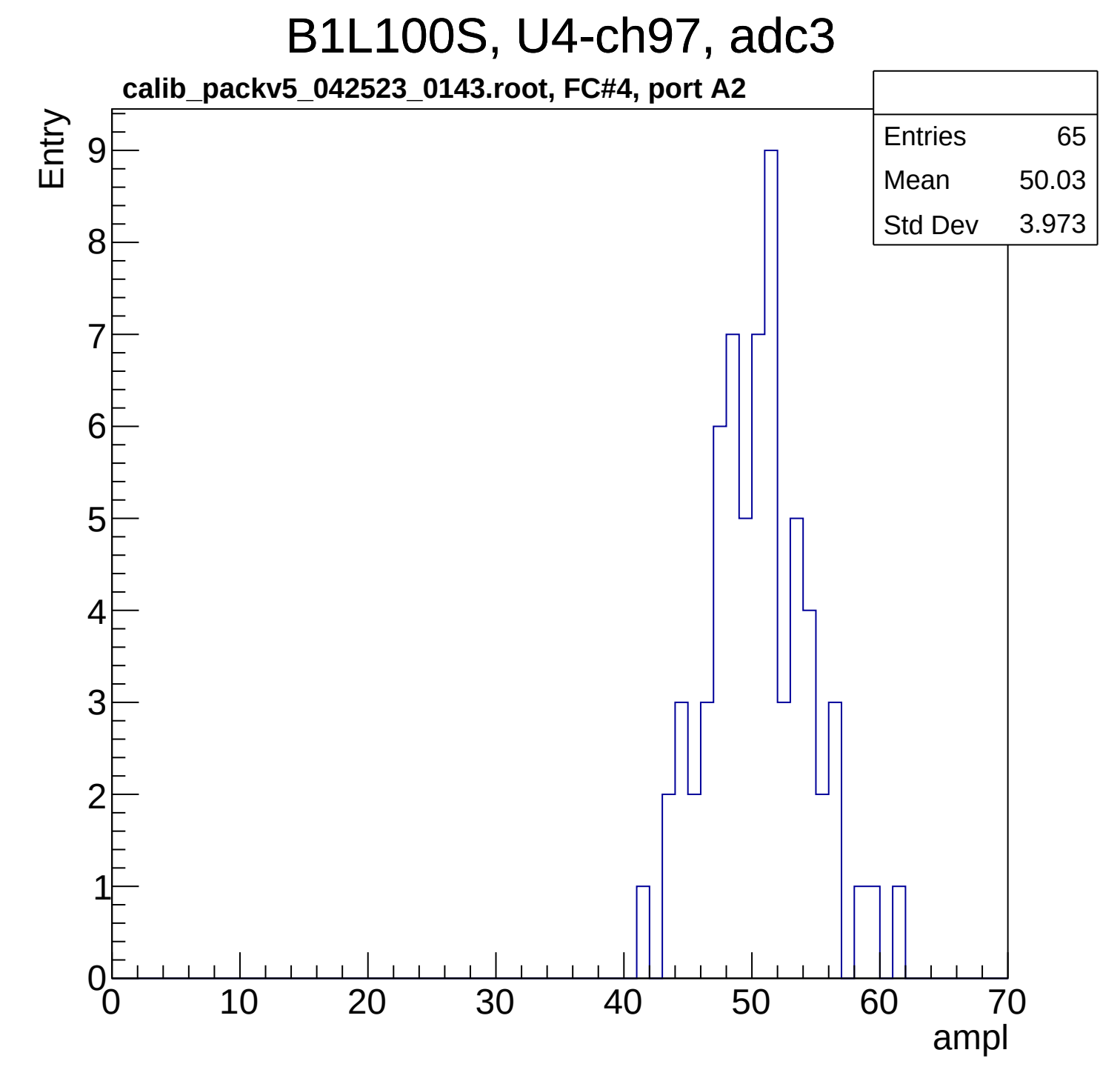

B1L100S, U4-ch96, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 19
Mean 57.79
Std Dev 13.74
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

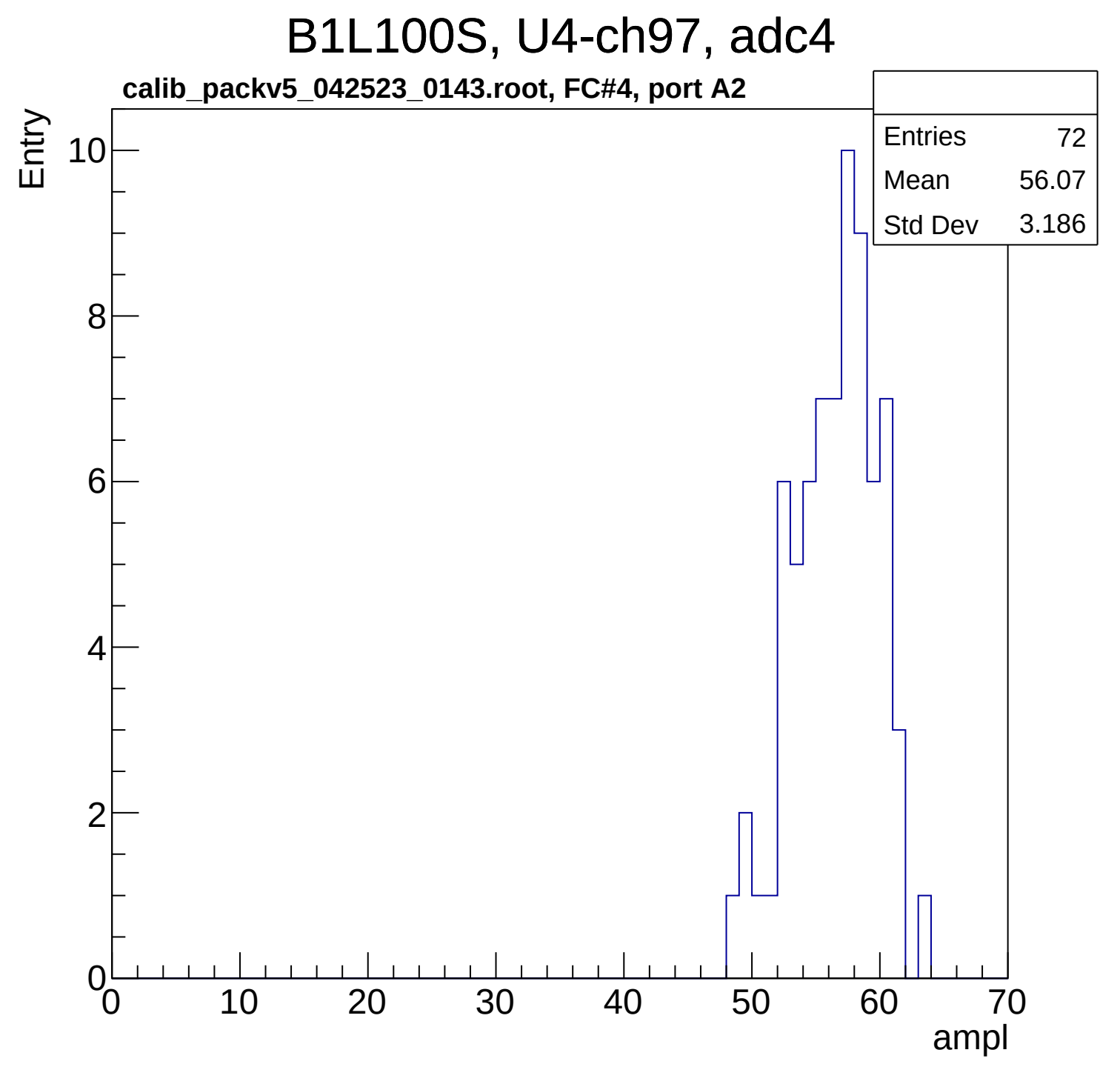

B1L100S, U4-ch96, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 20
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

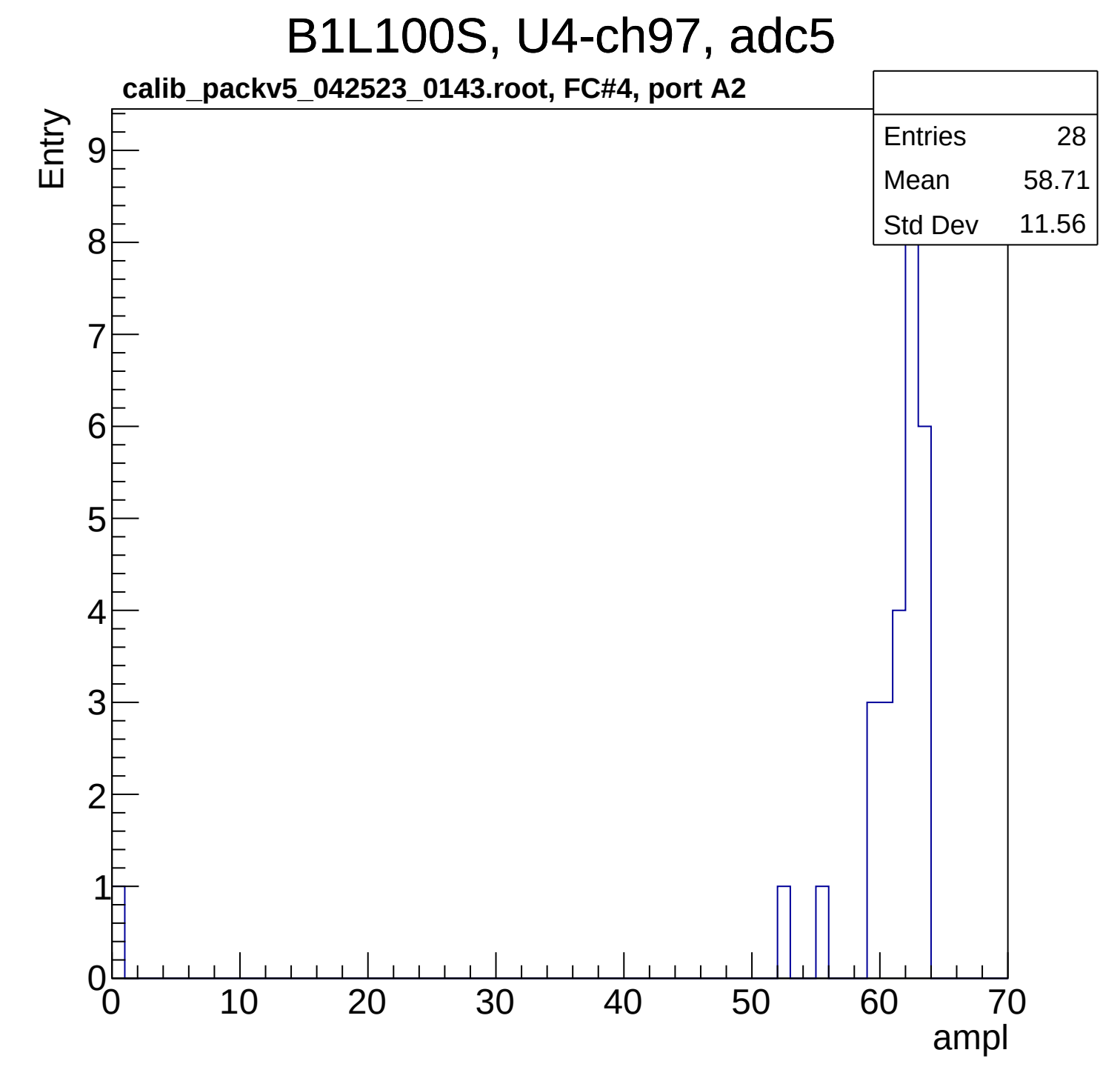

B1L100S, U4-ch97, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 30.63
Std Dev 2.918
Gaus mean : 31.2545
Gaus Width: 3.0926
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

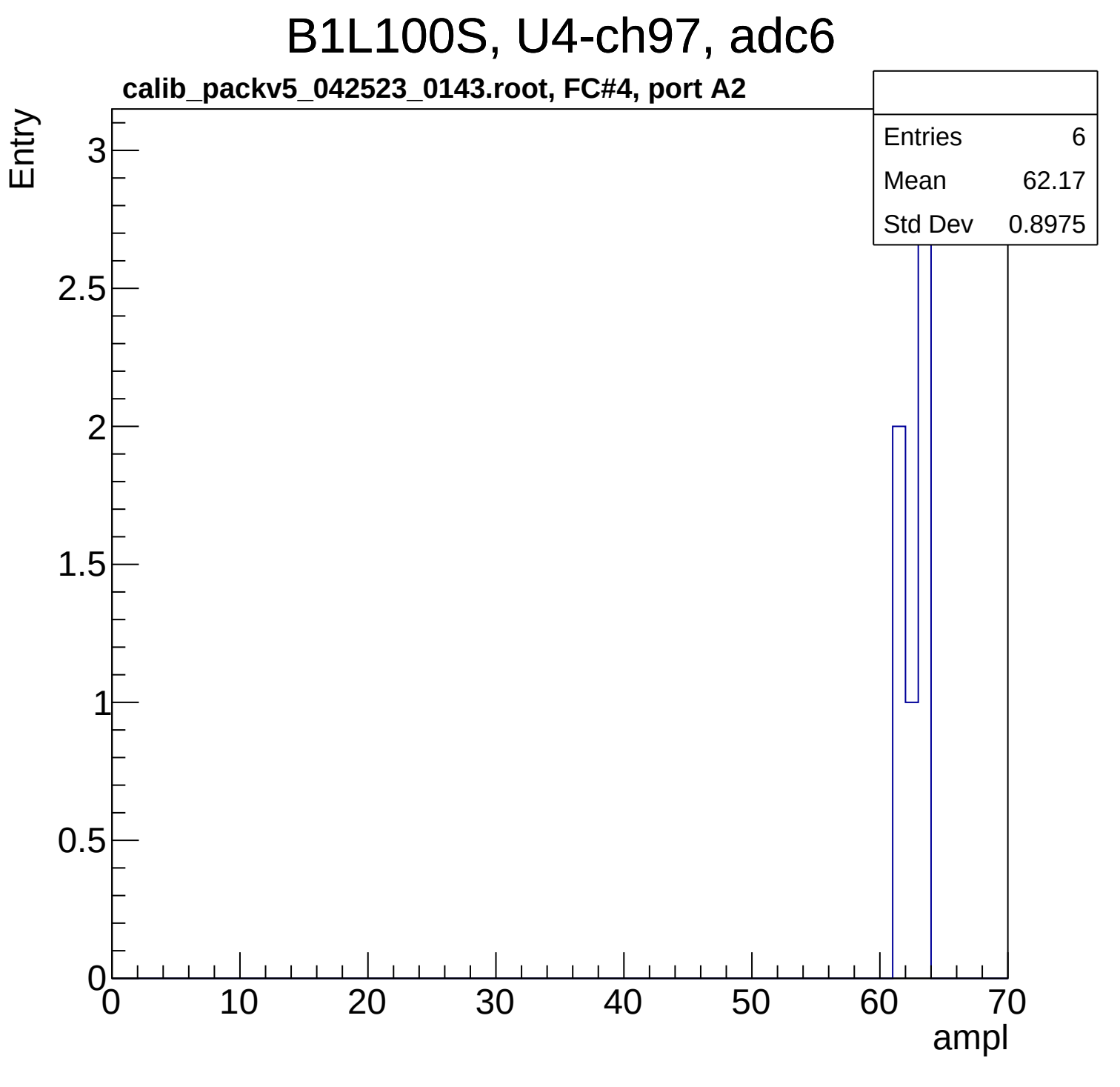

B1L100S, U4-ch97, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 37.28
Std Dev 3.489
Gaus mean : 38.6356
Gaus Width: 3.6033
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

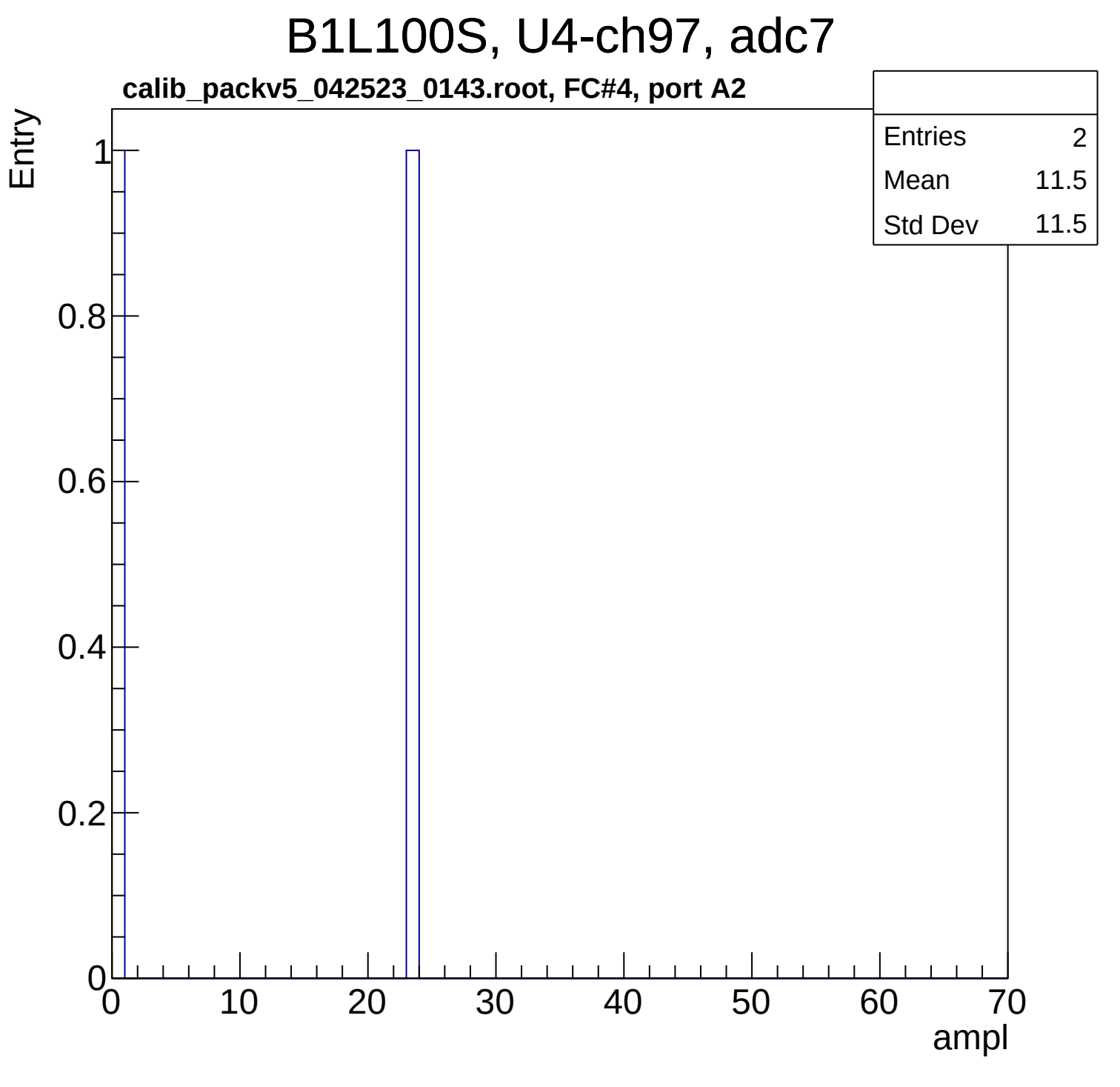

B1L100S, U4-ch97, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 43.15
Std Dev 3.527
Gaus mean : 43.9793
Gaus Width: 3.7254
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

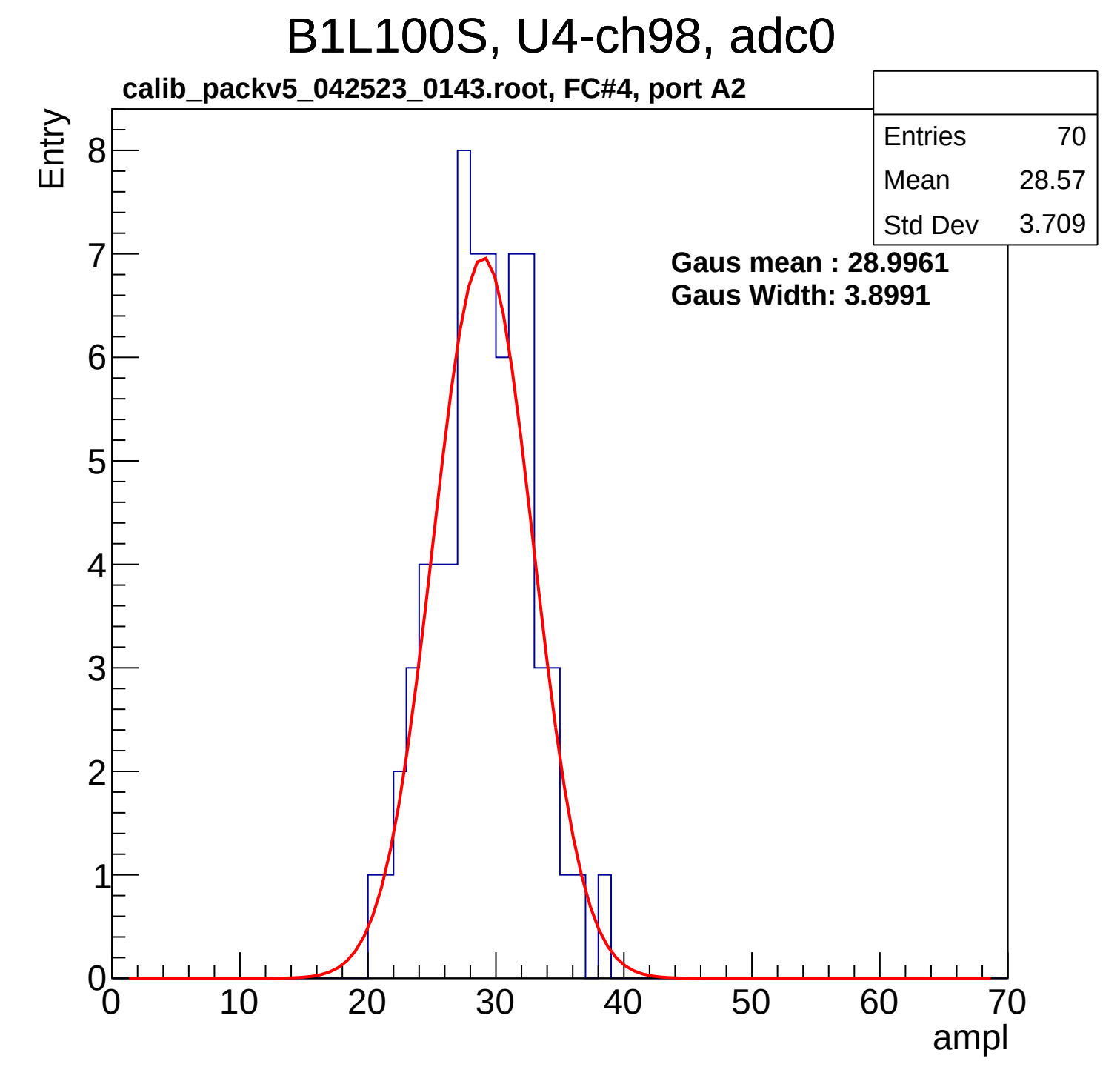

B1L100S, U4-ch97, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 50.03
Std Dev 3.973
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

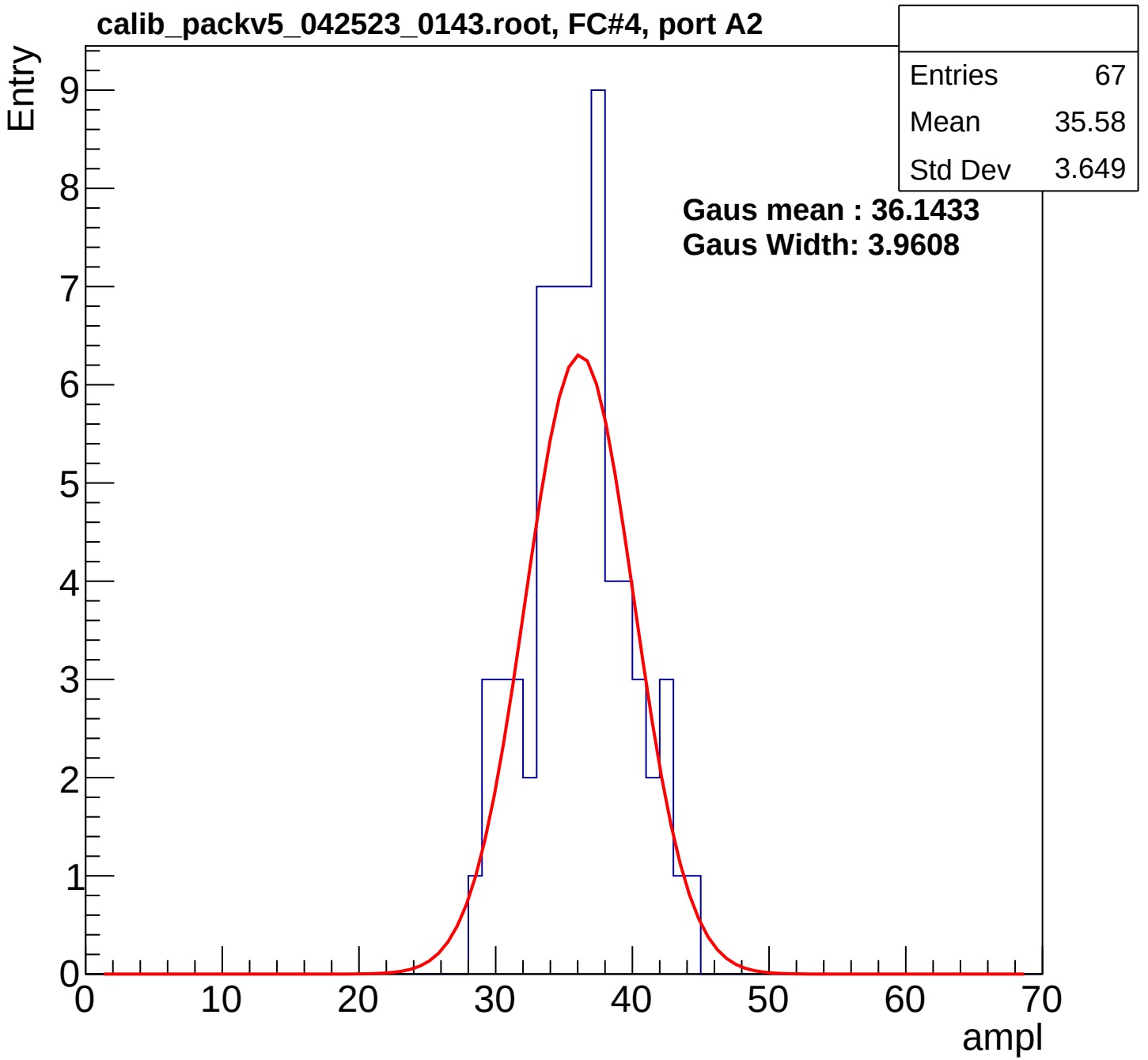

B1L100S, U4-ch97, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 56.07
Std Dev 3.186
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

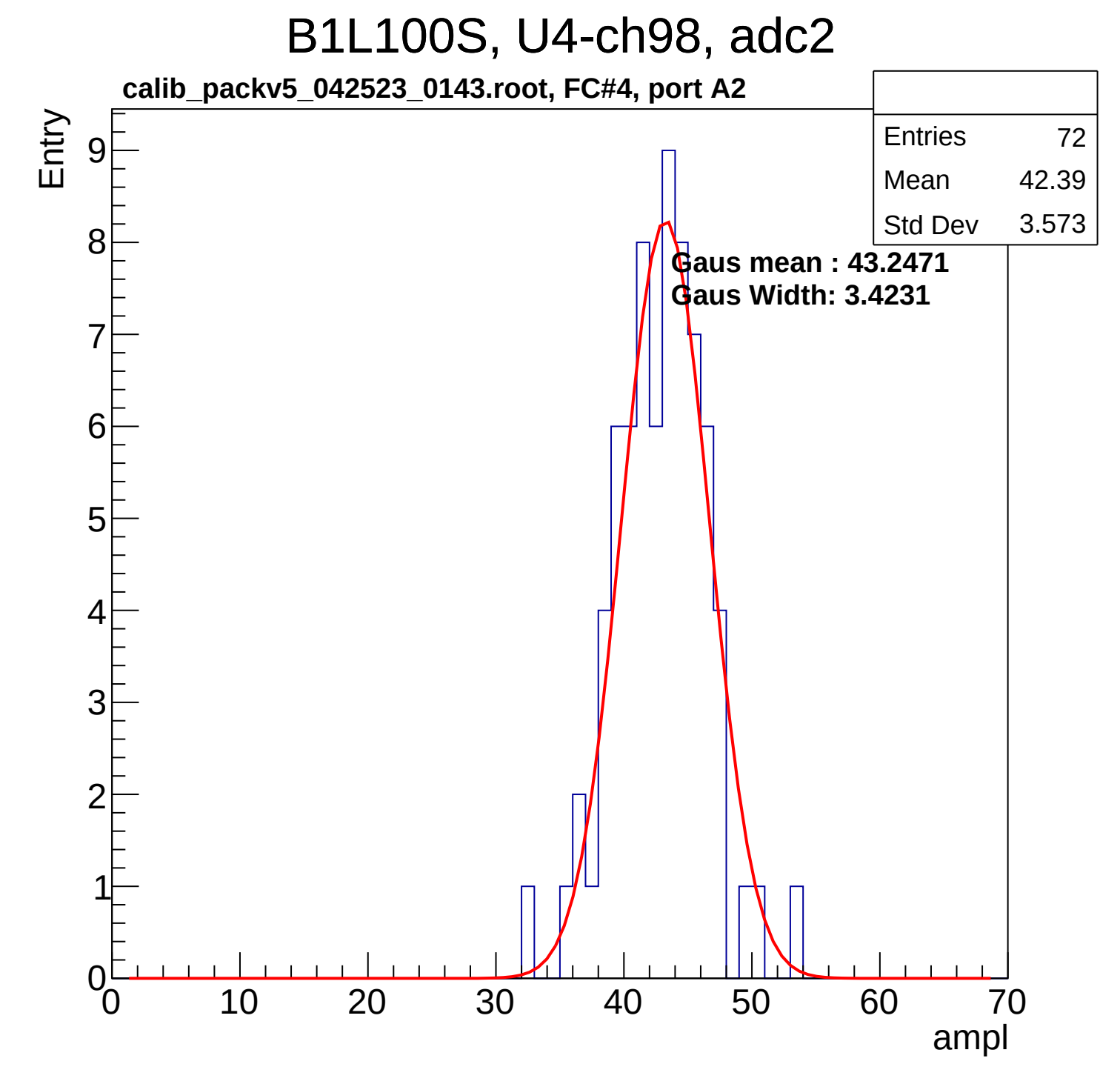

B1L100S, U4-ch97, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 28
Mean 58.71
Std Dev 11.56
Entry
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70
ampl

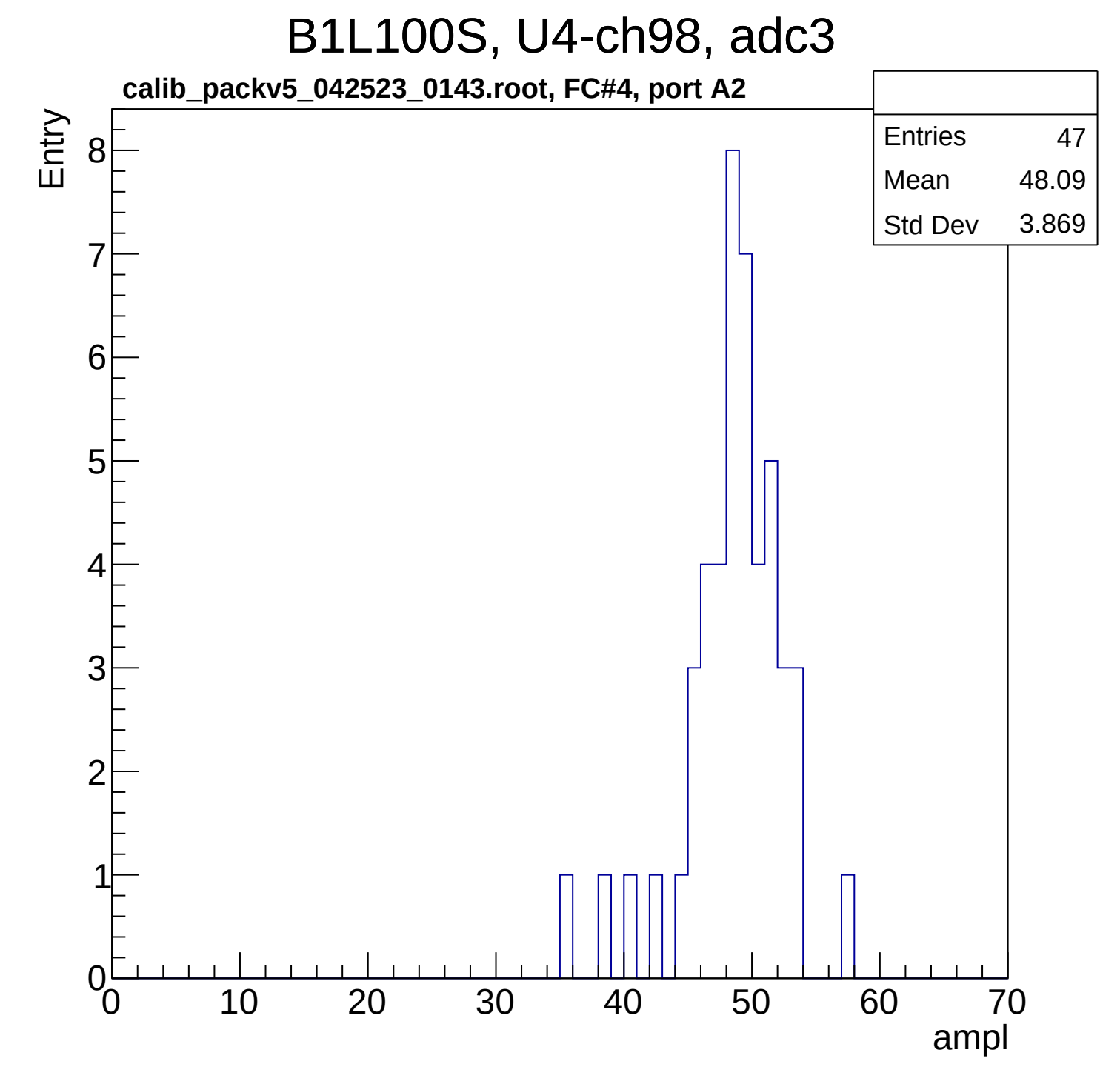

B1L100S, U4-ch97, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 62.17
Std Dev 0.8975
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

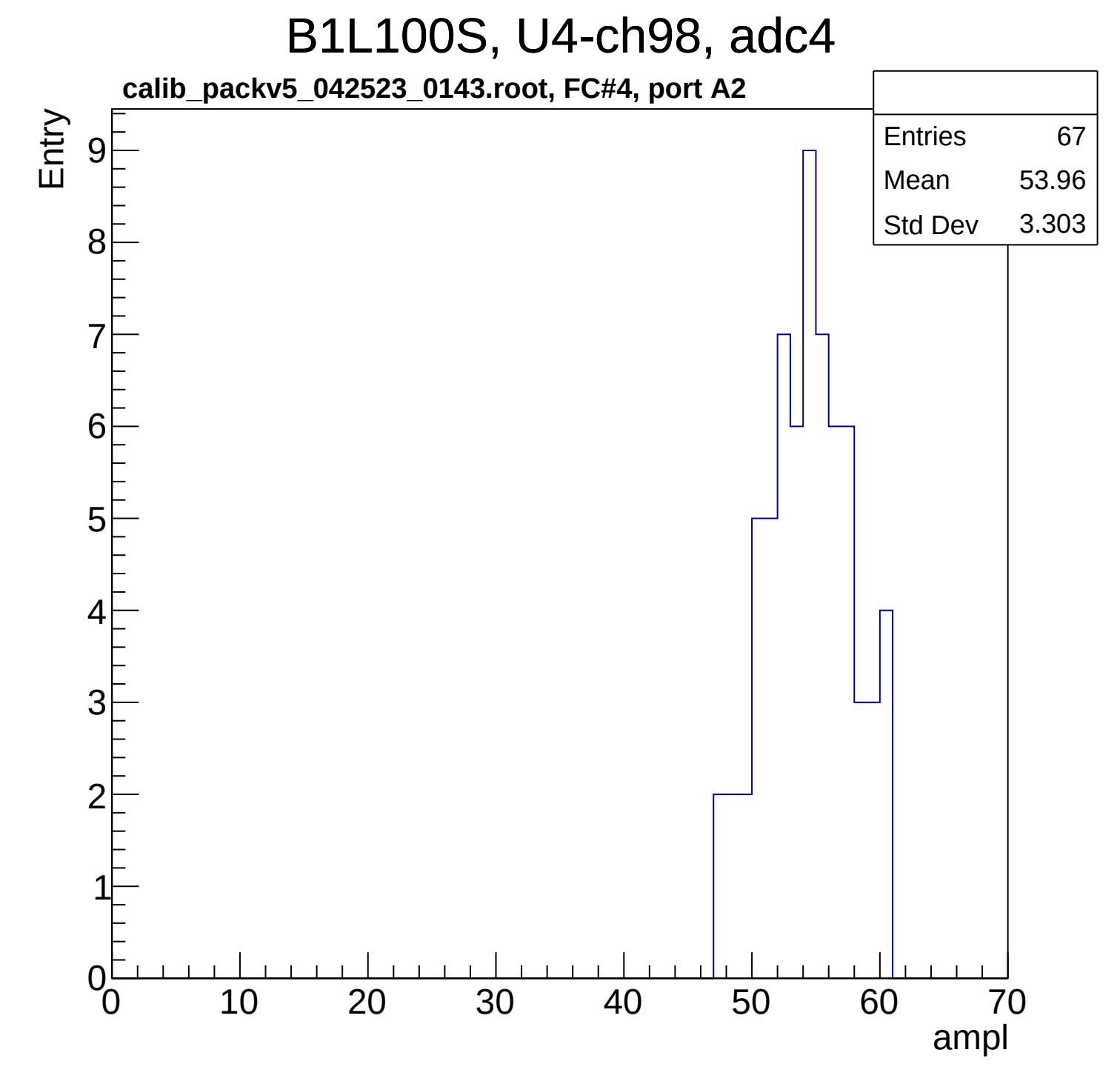

B1L100S, U4-ch97, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 11.5
Std Dev 11.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

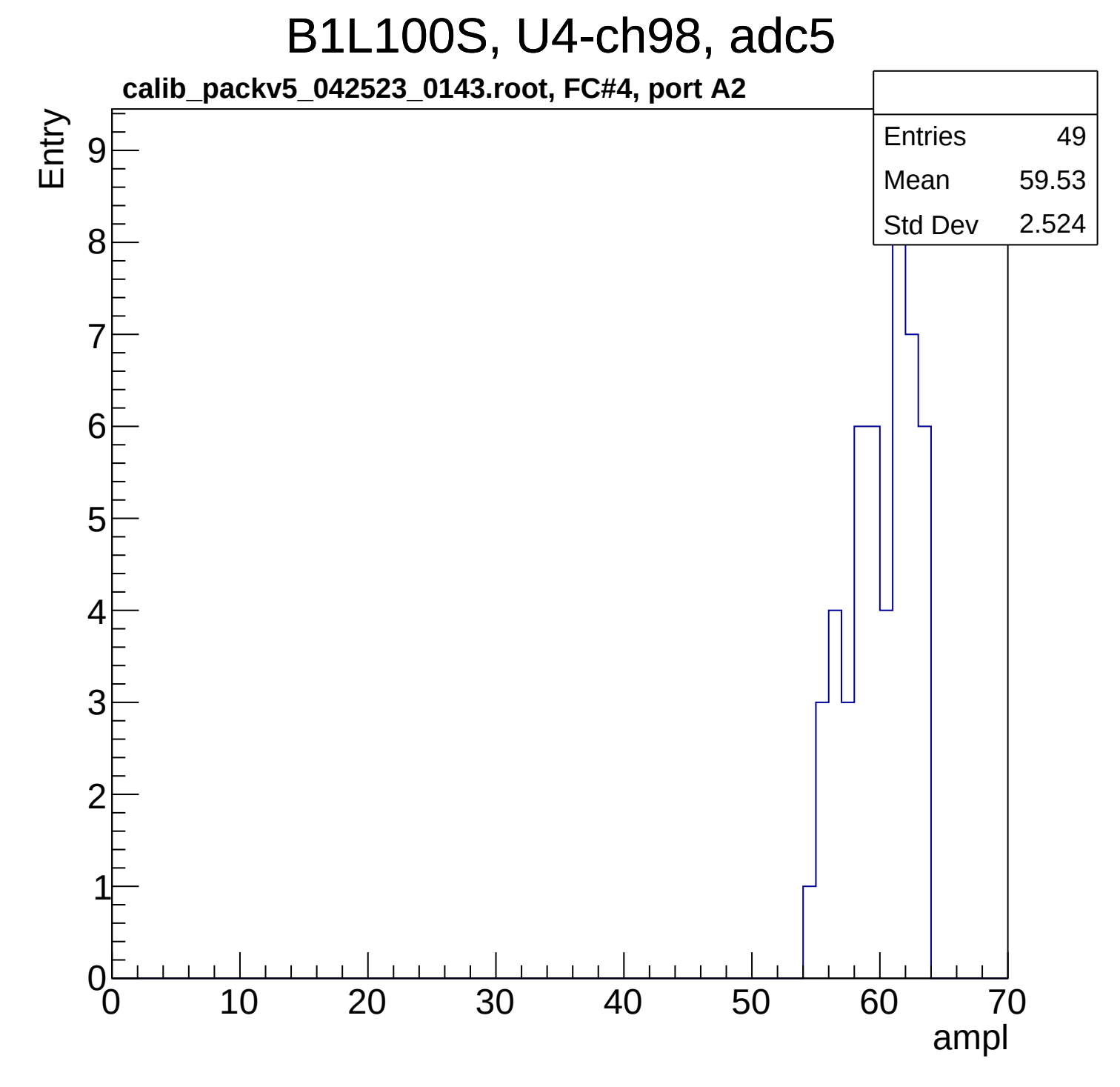

B1L100S, U4-ch98, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 28.57
Std Dev 3.709
Gaus mean : 28.9961
Gaus Width: 3.8991
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

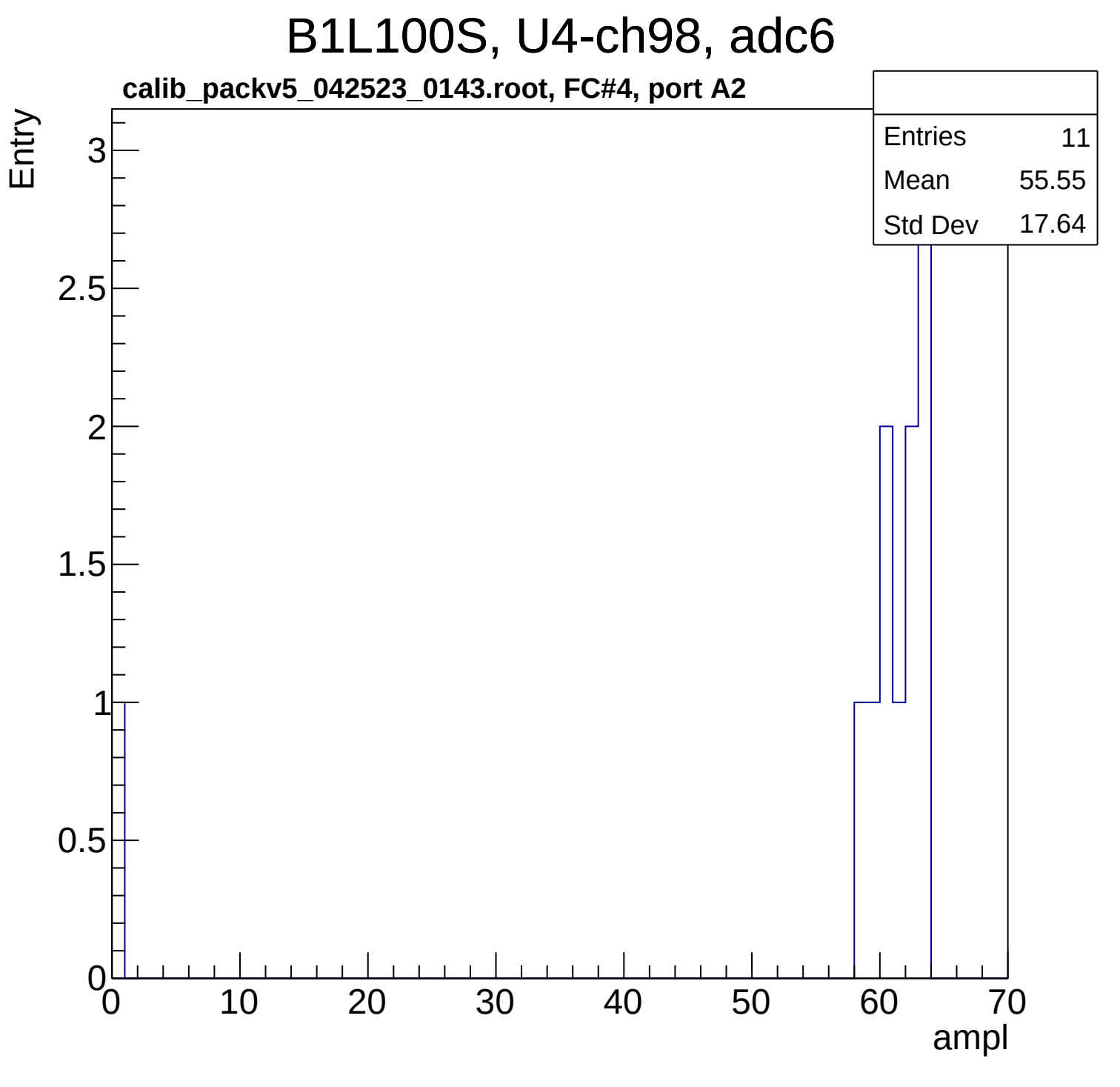

B1L100S, U4-ch98, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 35.58
Std Dev 3.649
Gaus mean : 36.1433
Gaus Width: 3.9608
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

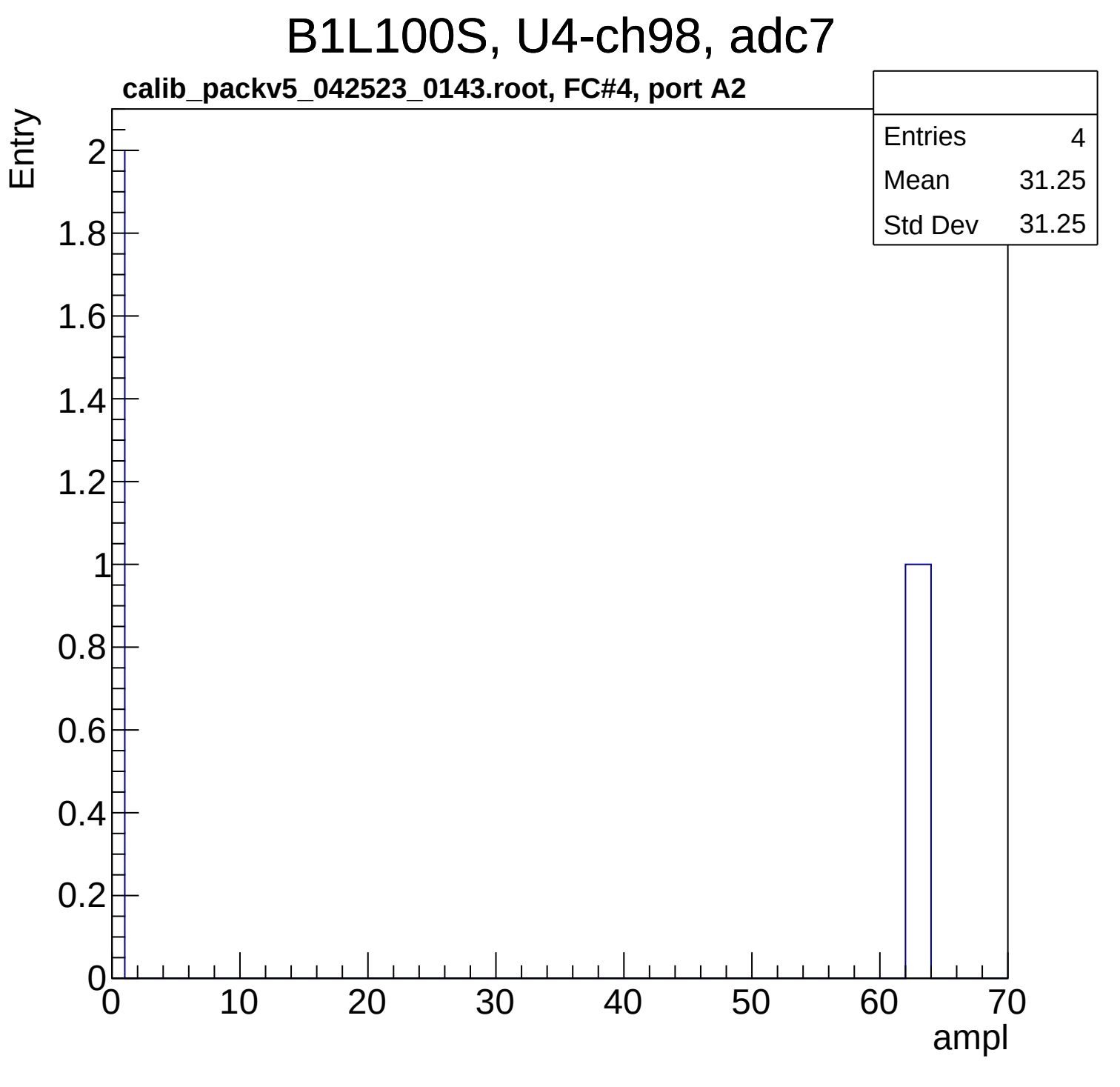

B1L100S, U4-ch98, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 42.39
Std Dev 3.573
Gaus mean : 43.2471
Gaus Width: 3.4231
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

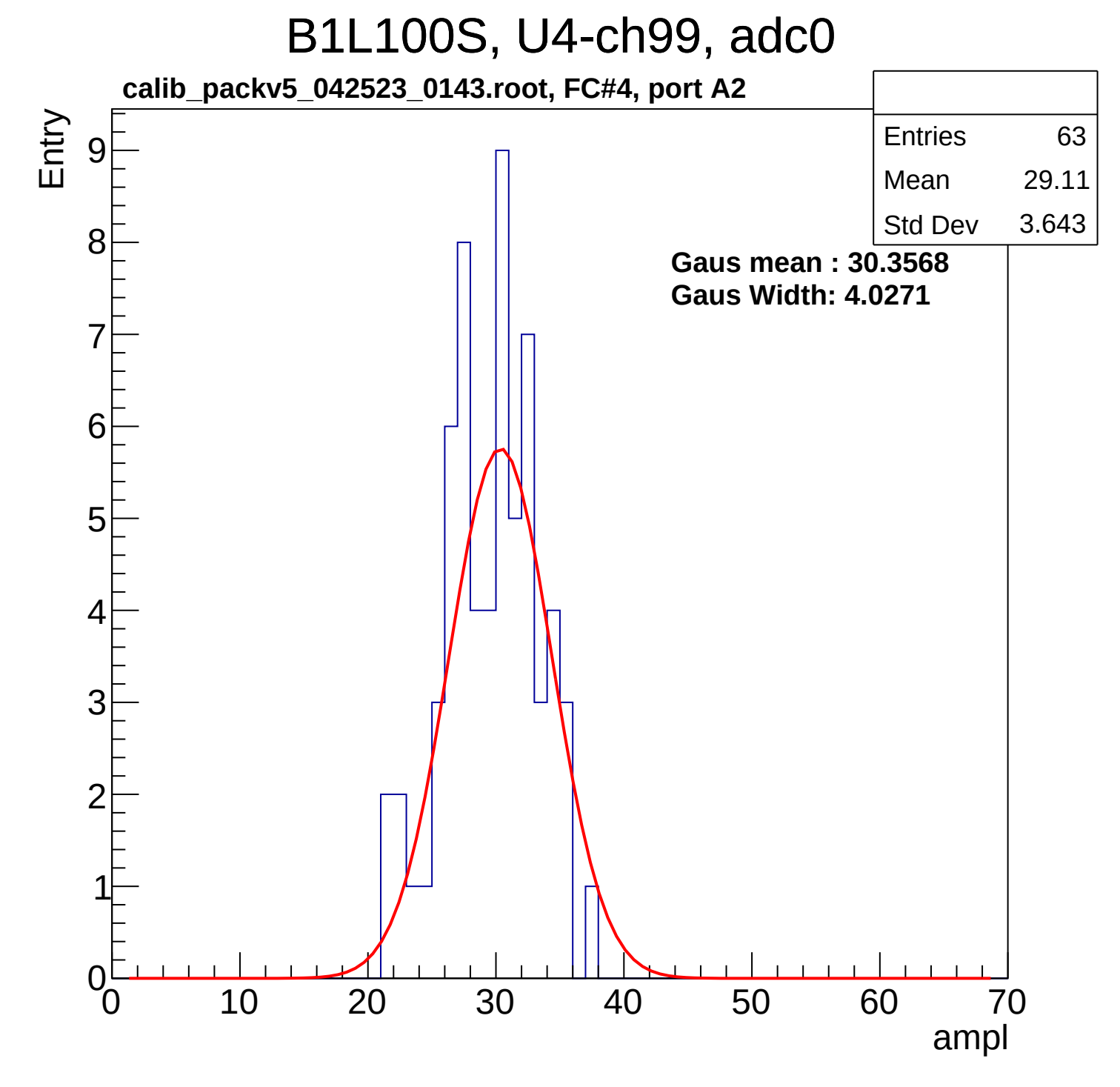

B1L100S, U4-ch98, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 48.09
Std Dev 3.869
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

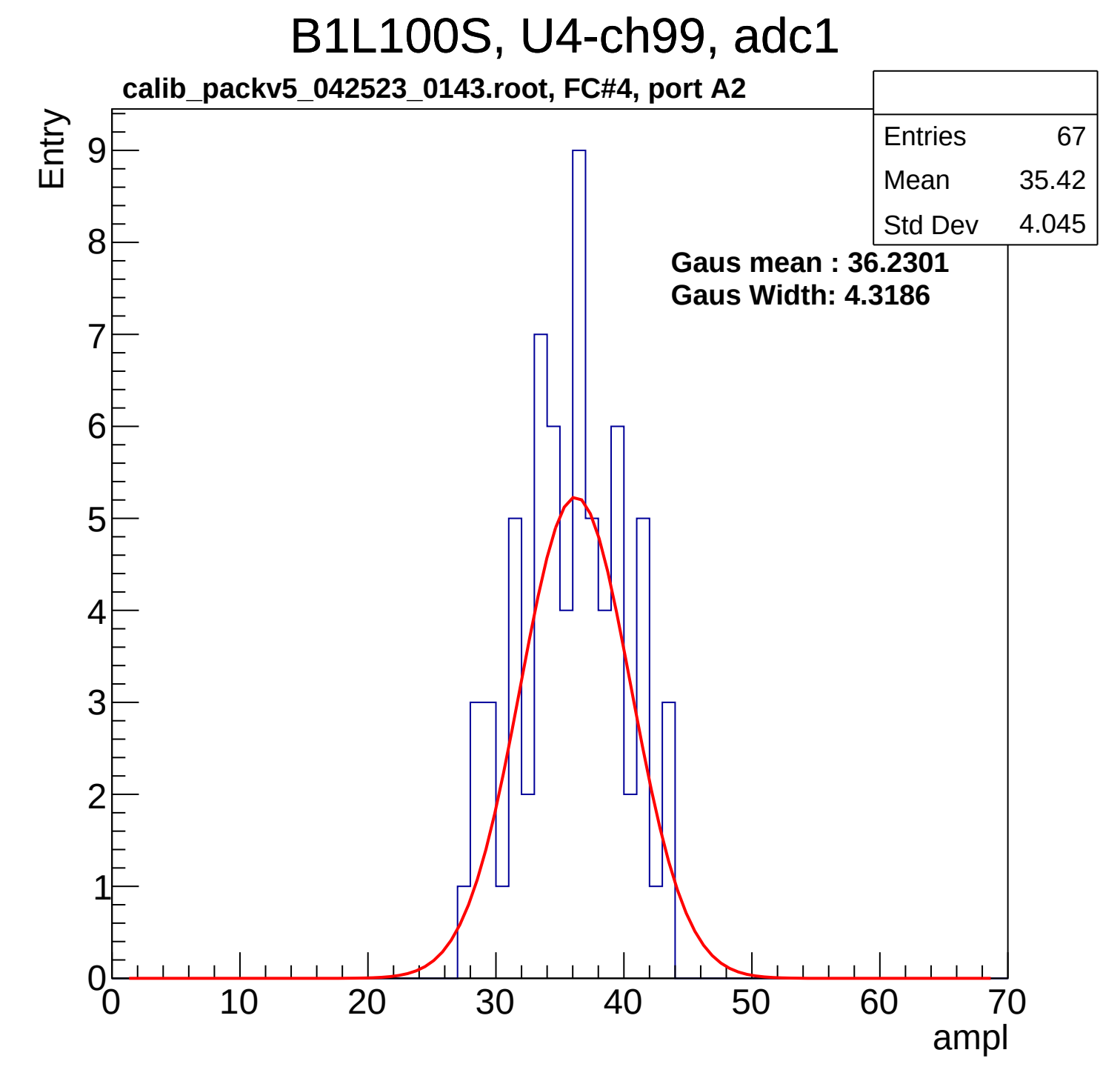

B1L100S, U4-ch98, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 53.96
Std Dev 3.303
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

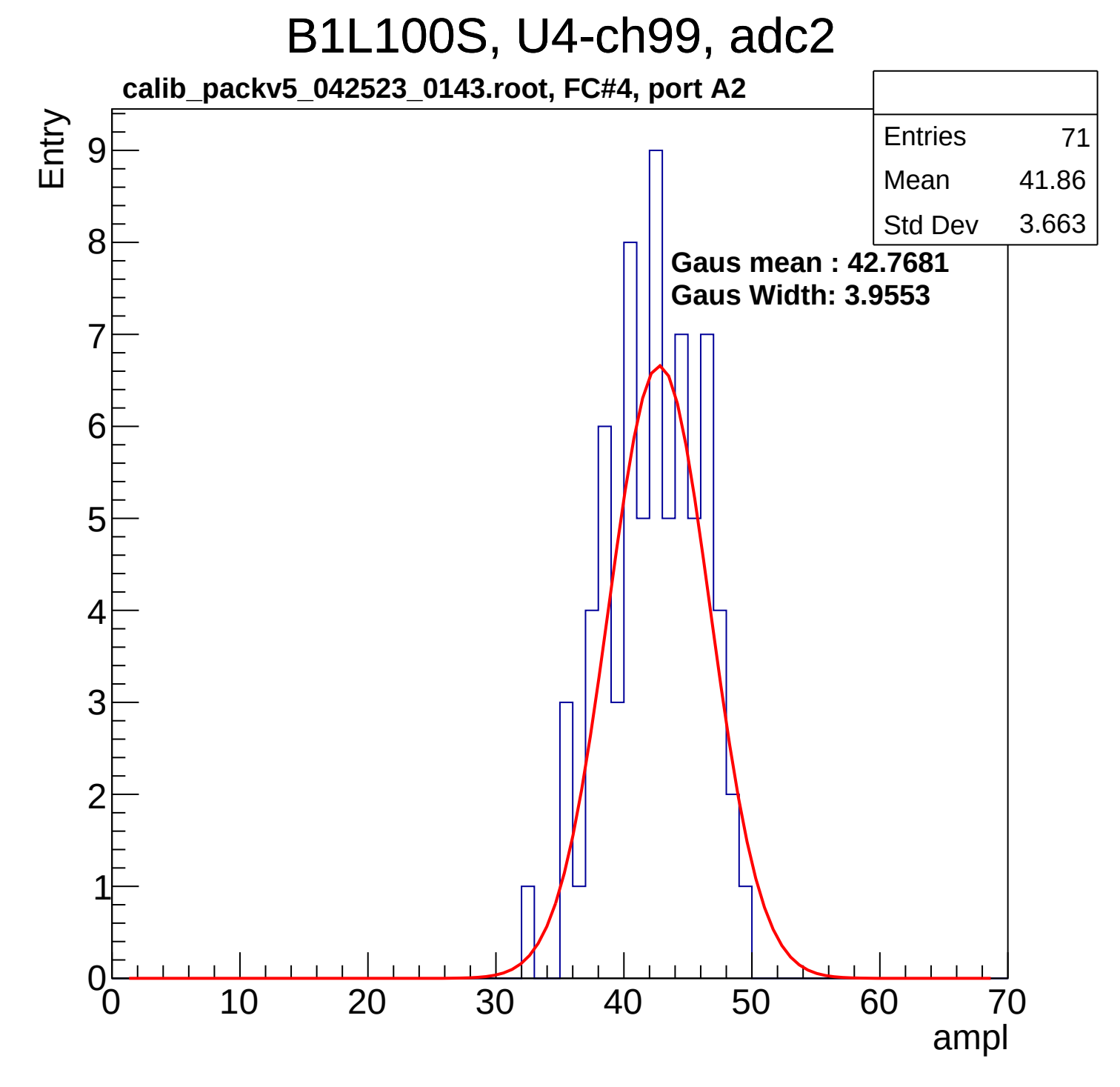

B1L100S, U4-ch98, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 59.53
Std Dev 2.524
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

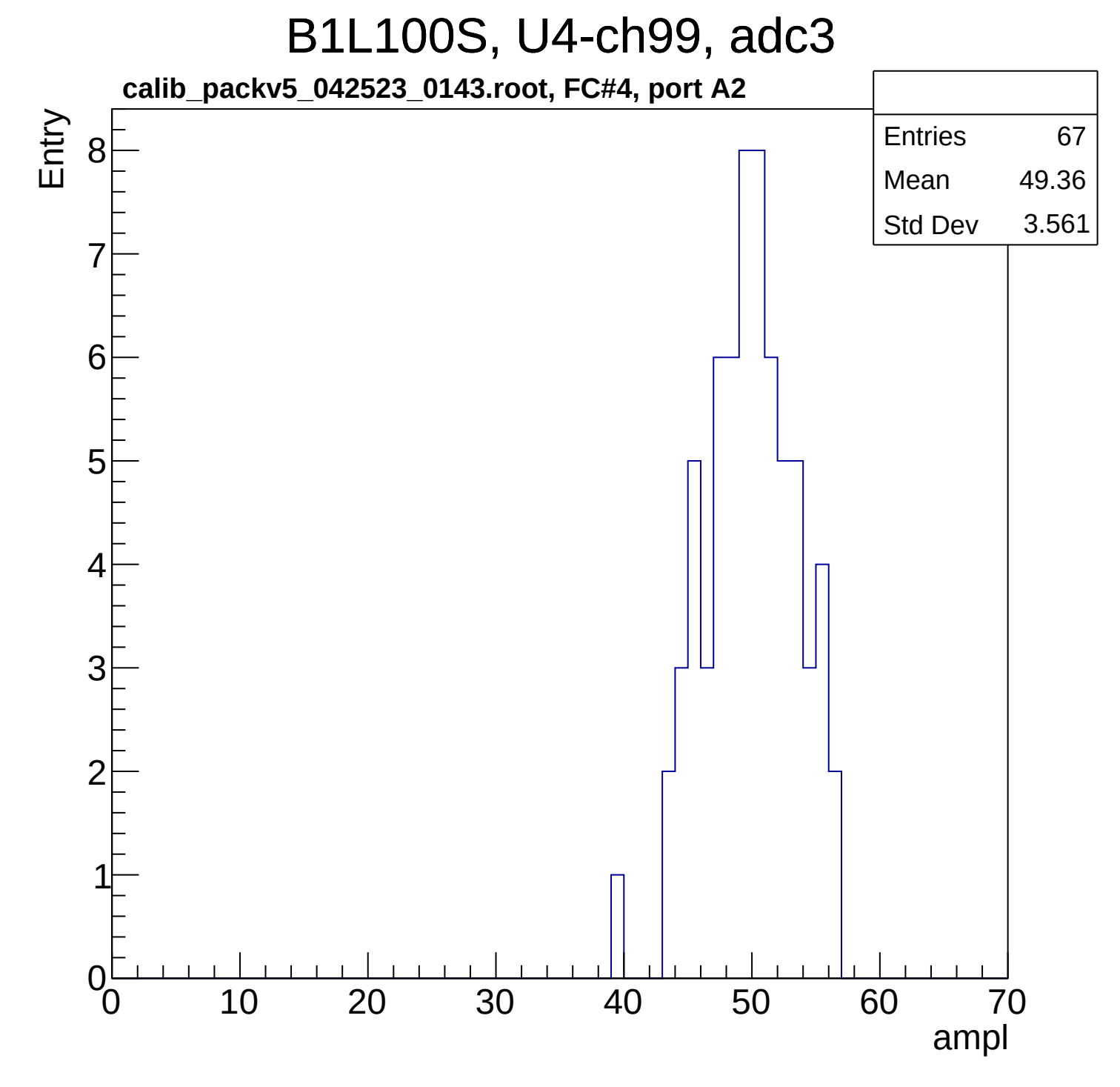

B1L100S, U4-ch98, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 55.55
Std Dev 17.64
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

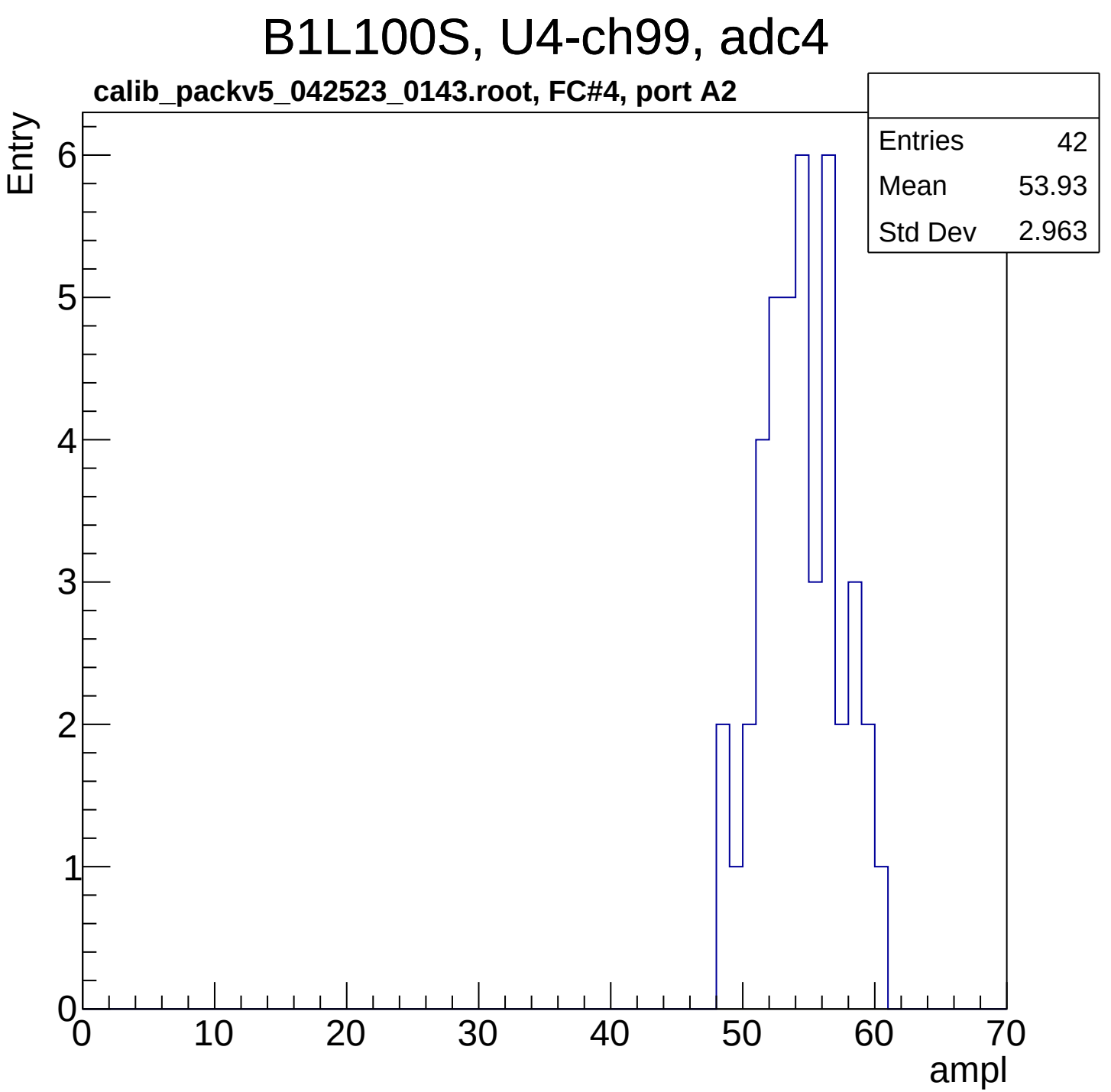

B1L100S, U4-ch98, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 31.25
Std Dev 31.25
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

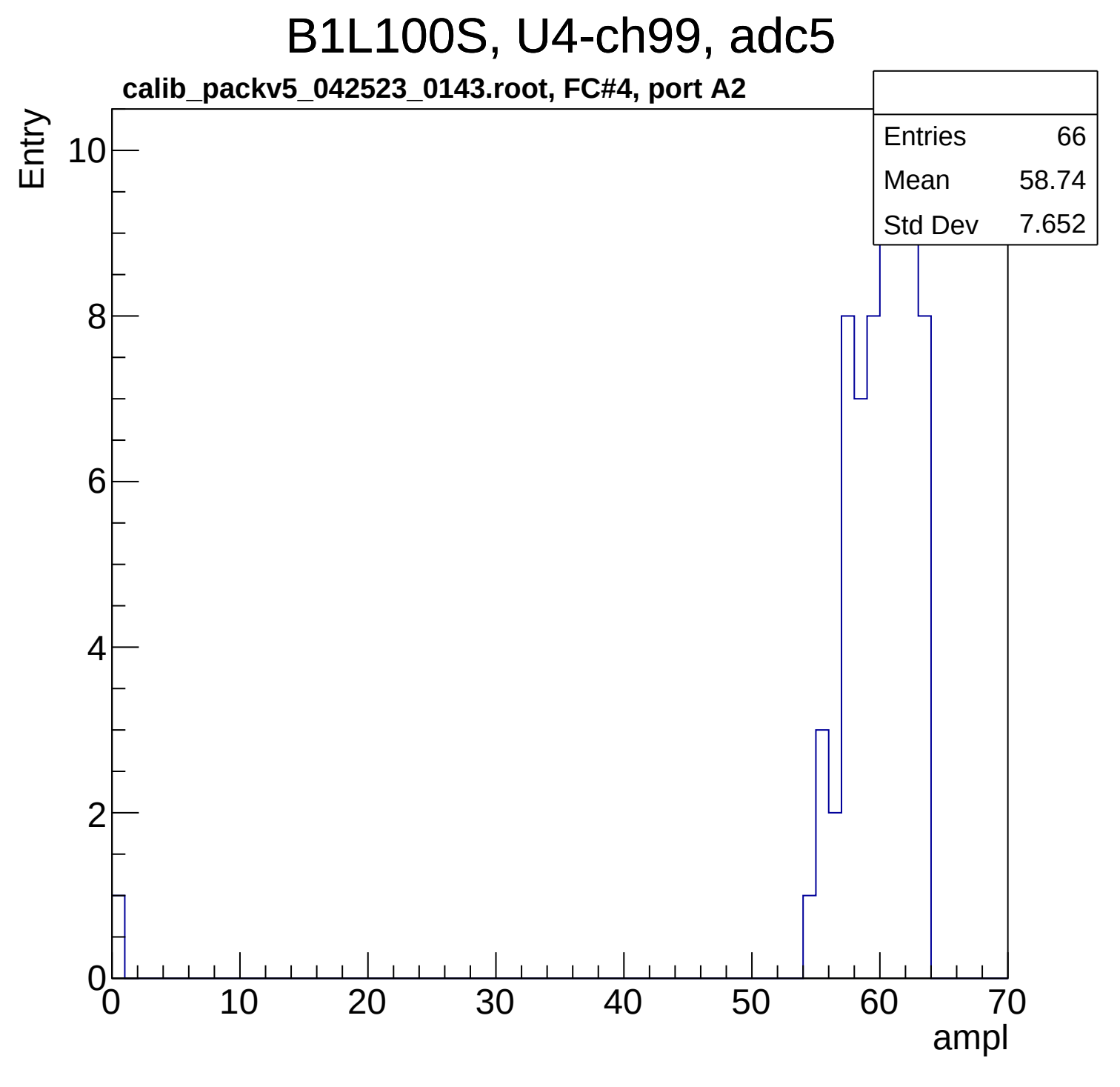

B1L100S, U4-ch99, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 29.11
Std Dev 3.643
Gaus mean : 30.3568
Gaus Width: 4.0271
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

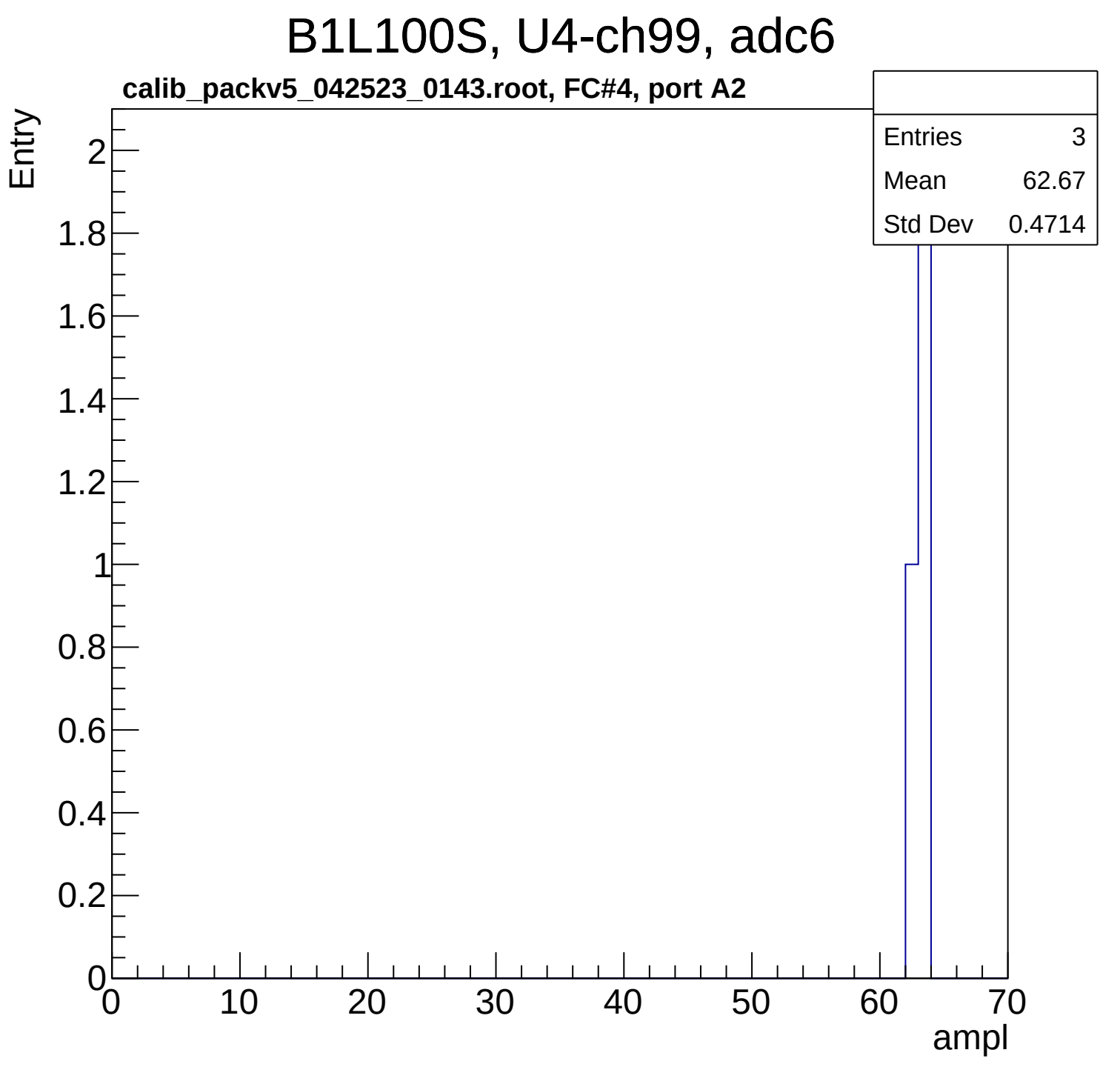

B1L100S, U4-ch99, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 35.42
Std Dev 4.045
Gaus mean : 36.2301
Gaus Width: 4.3186
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

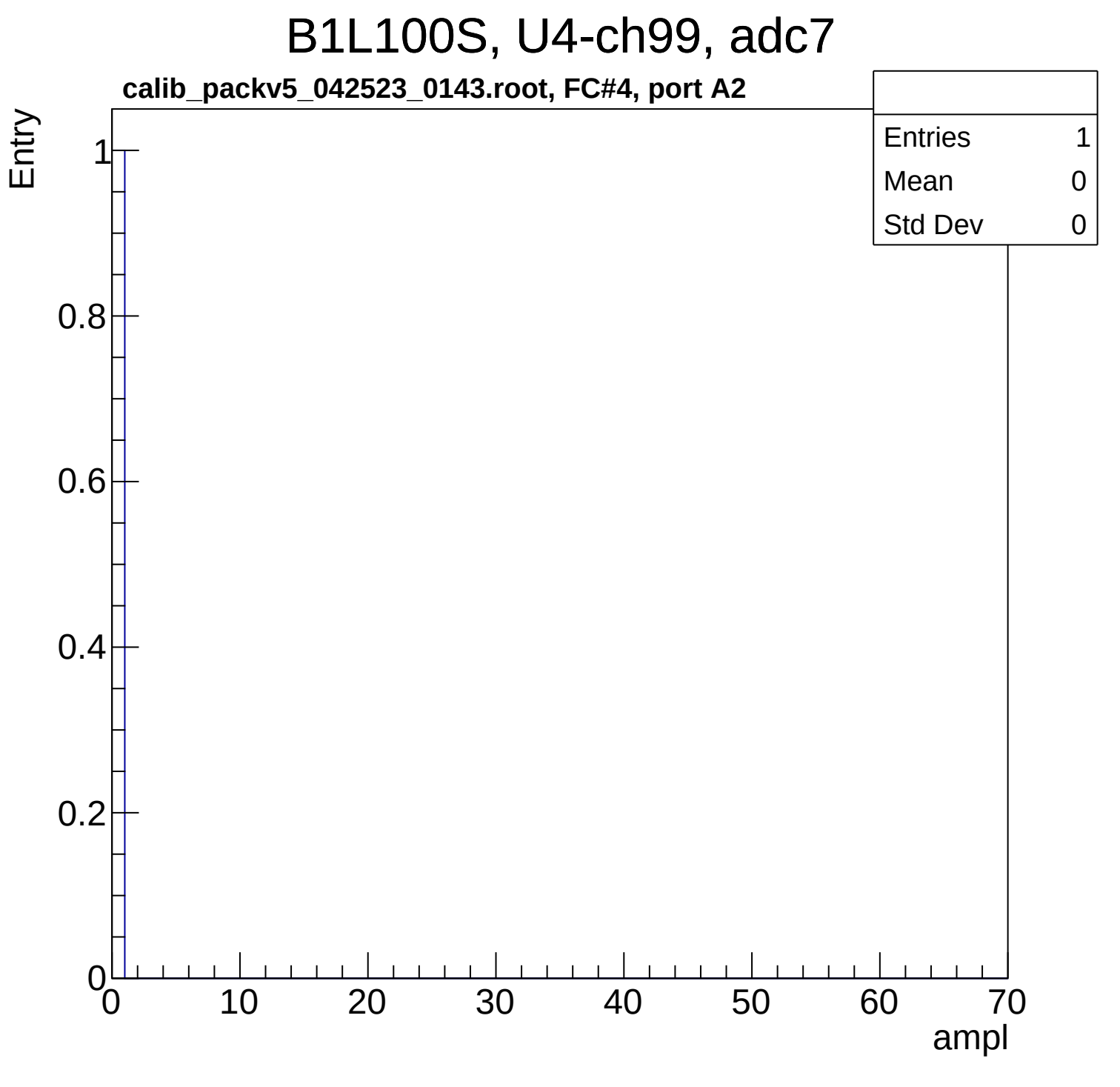

B1L100S, U4-ch99, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 41.86
Std Dev 3.663
Gaus mean : 42.7681
Gaus Width: 3.9553
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

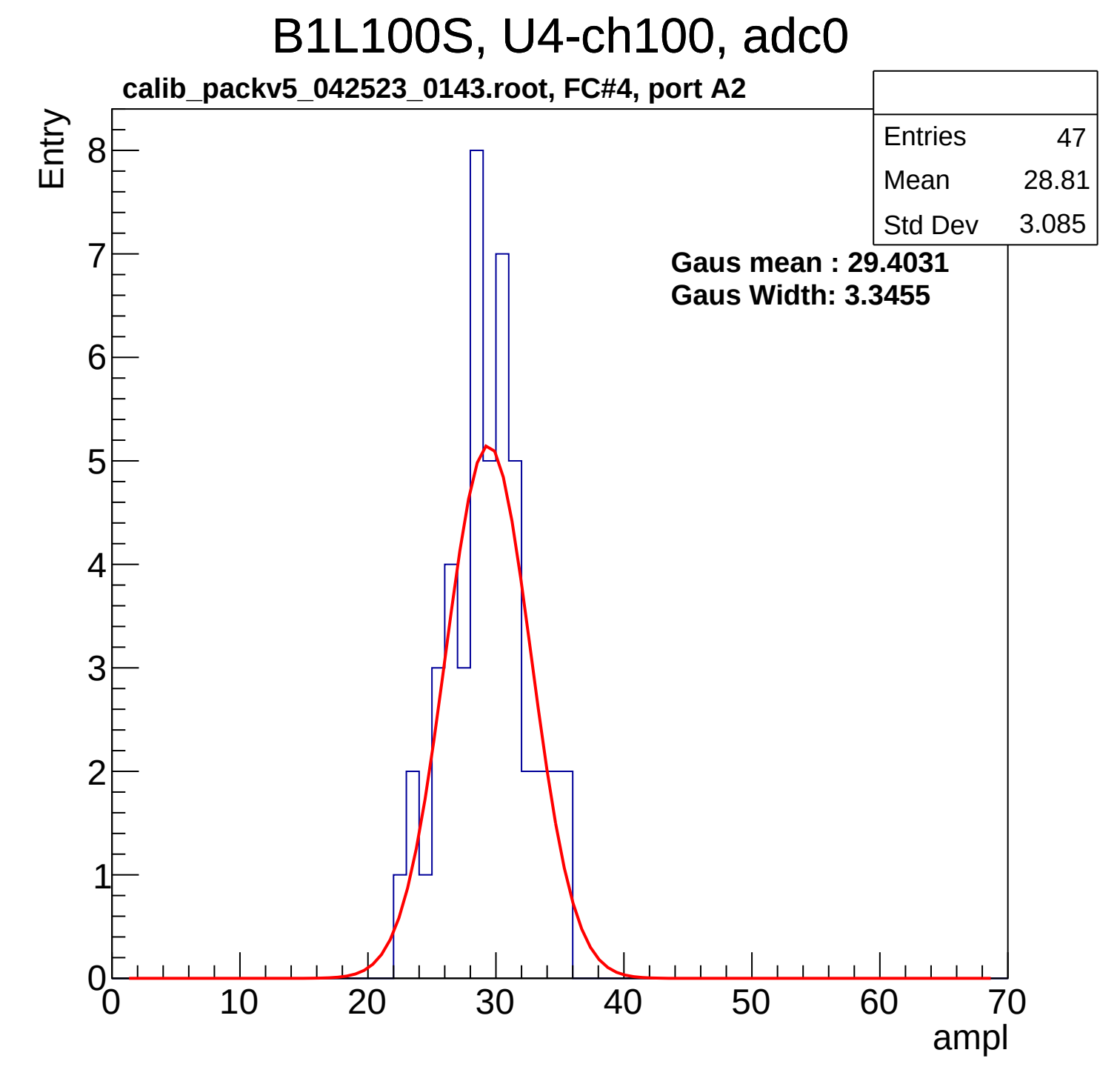

B1L100S, U4-ch99, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 49.36
Std Dev 3.561
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

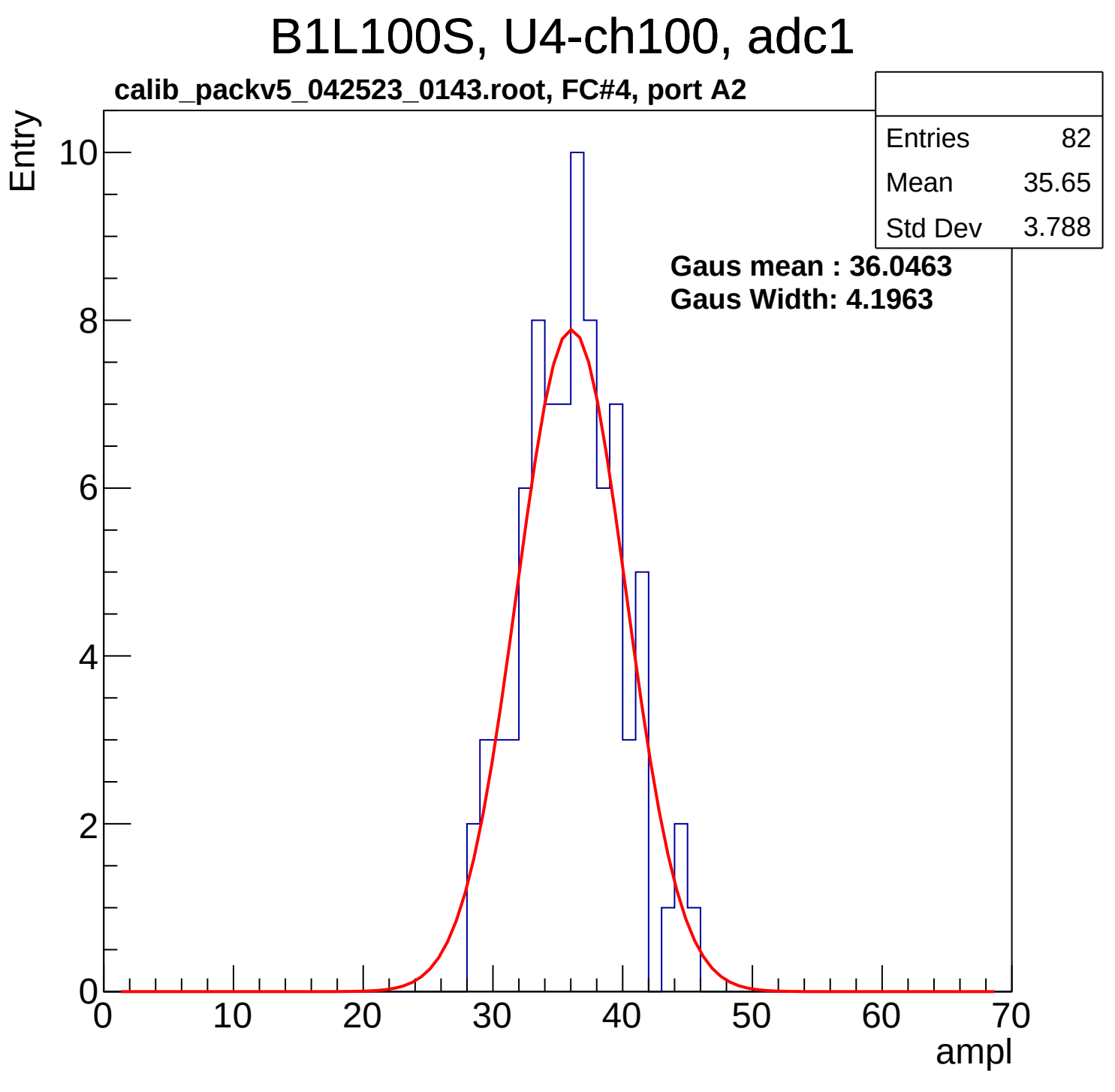

B1L100S, U4-ch99, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 42
Mean 53.93
Std Dev 2.963
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

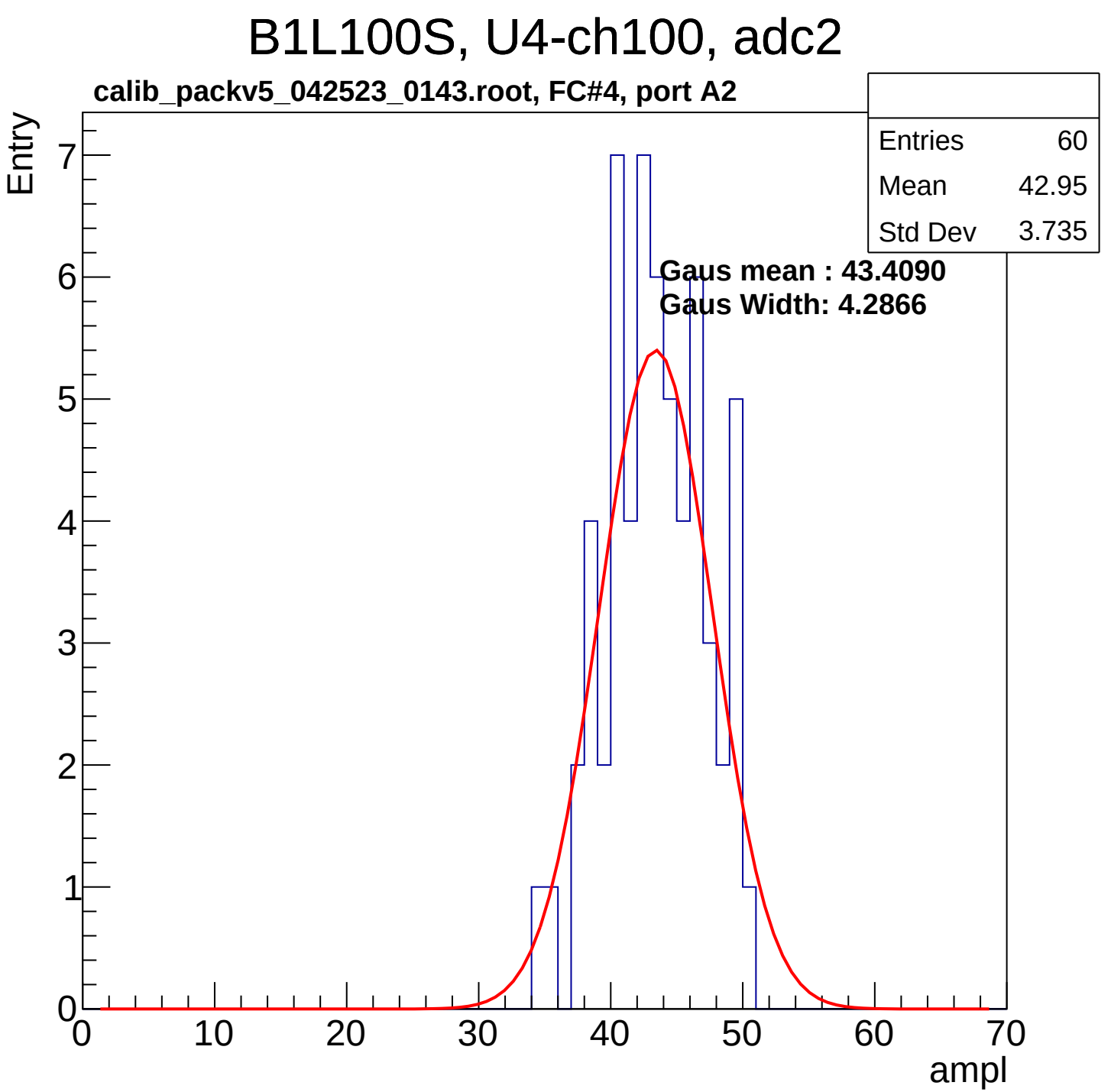

B1L100S, U4-ch99, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 58.74
Std Dev 7.652
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

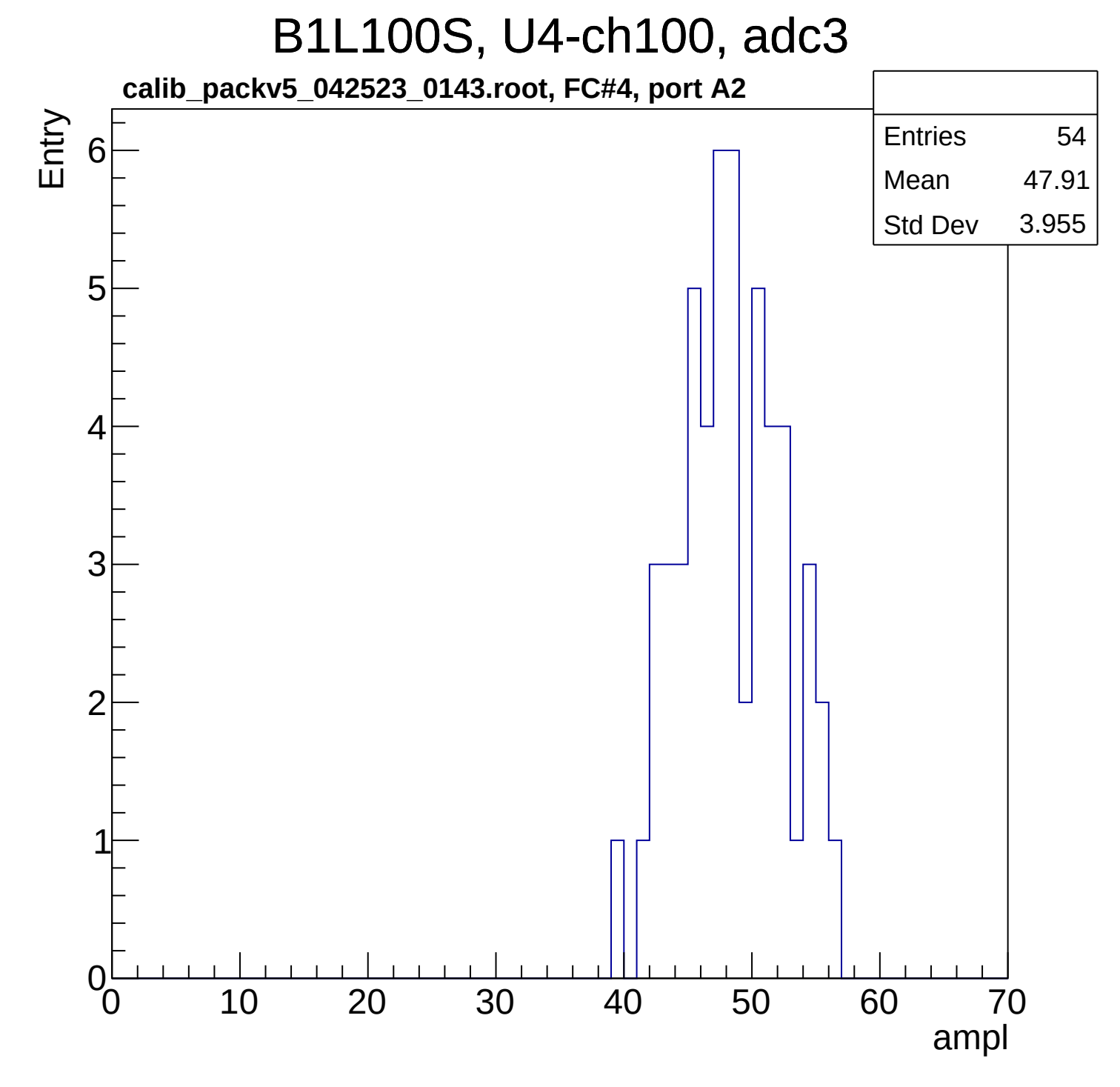

B1L100S, U4-ch99, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

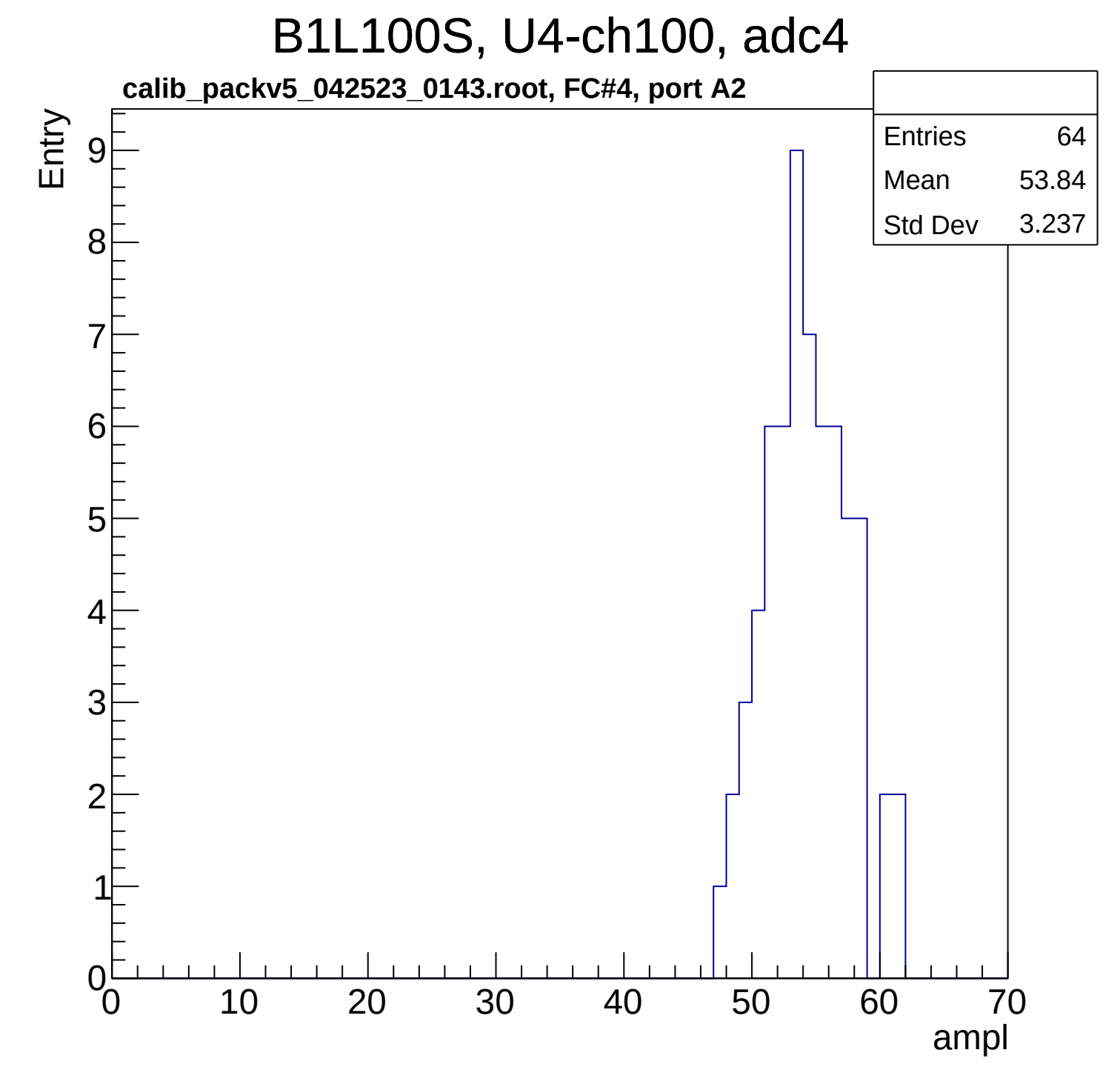

B1L100S, U4-ch99, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

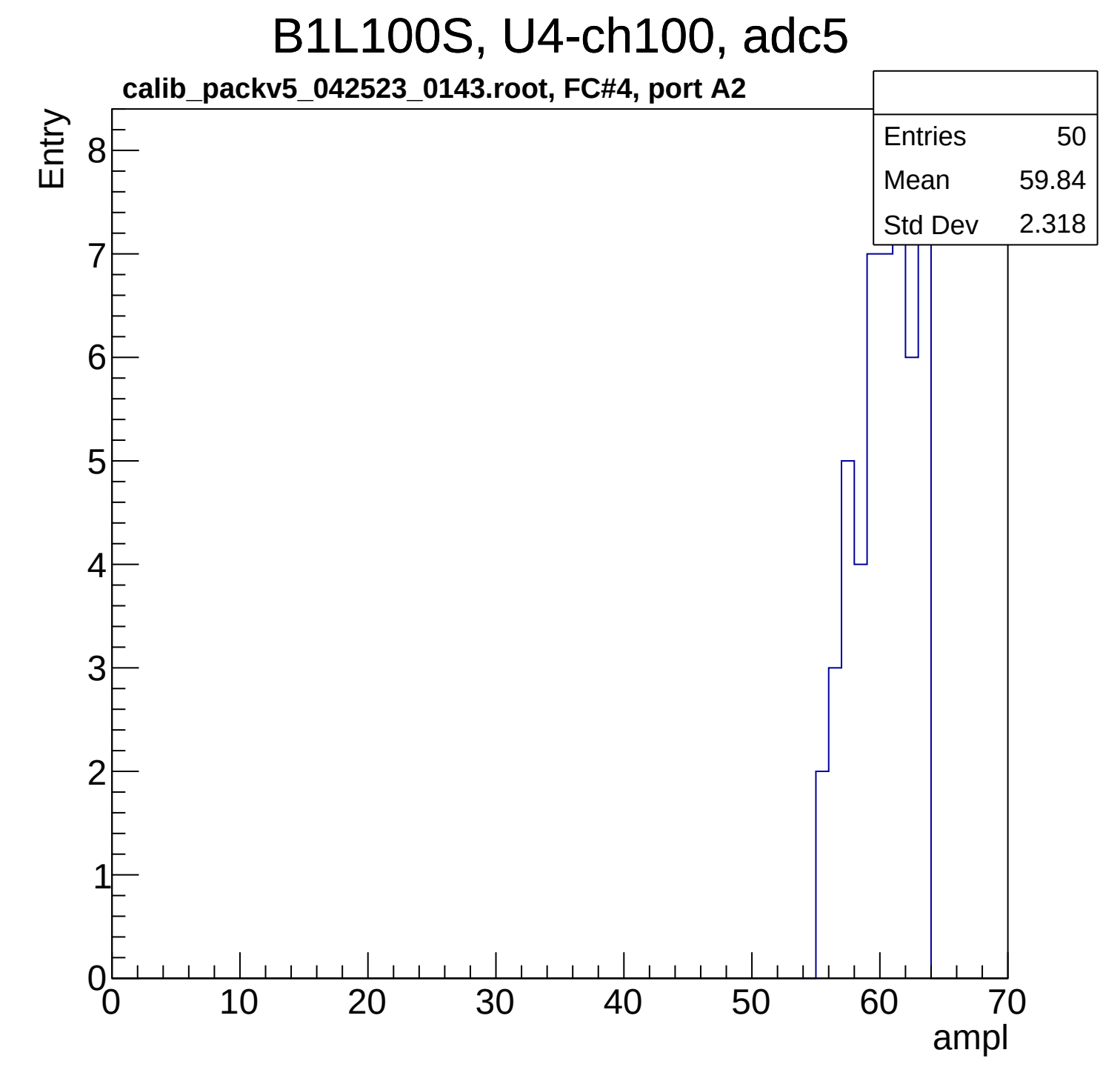

B1L100S, U4-ch100, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 28.81
Std Dev 3.085
Gaus mean : 29.4031
Gaus Width: 3.3455
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

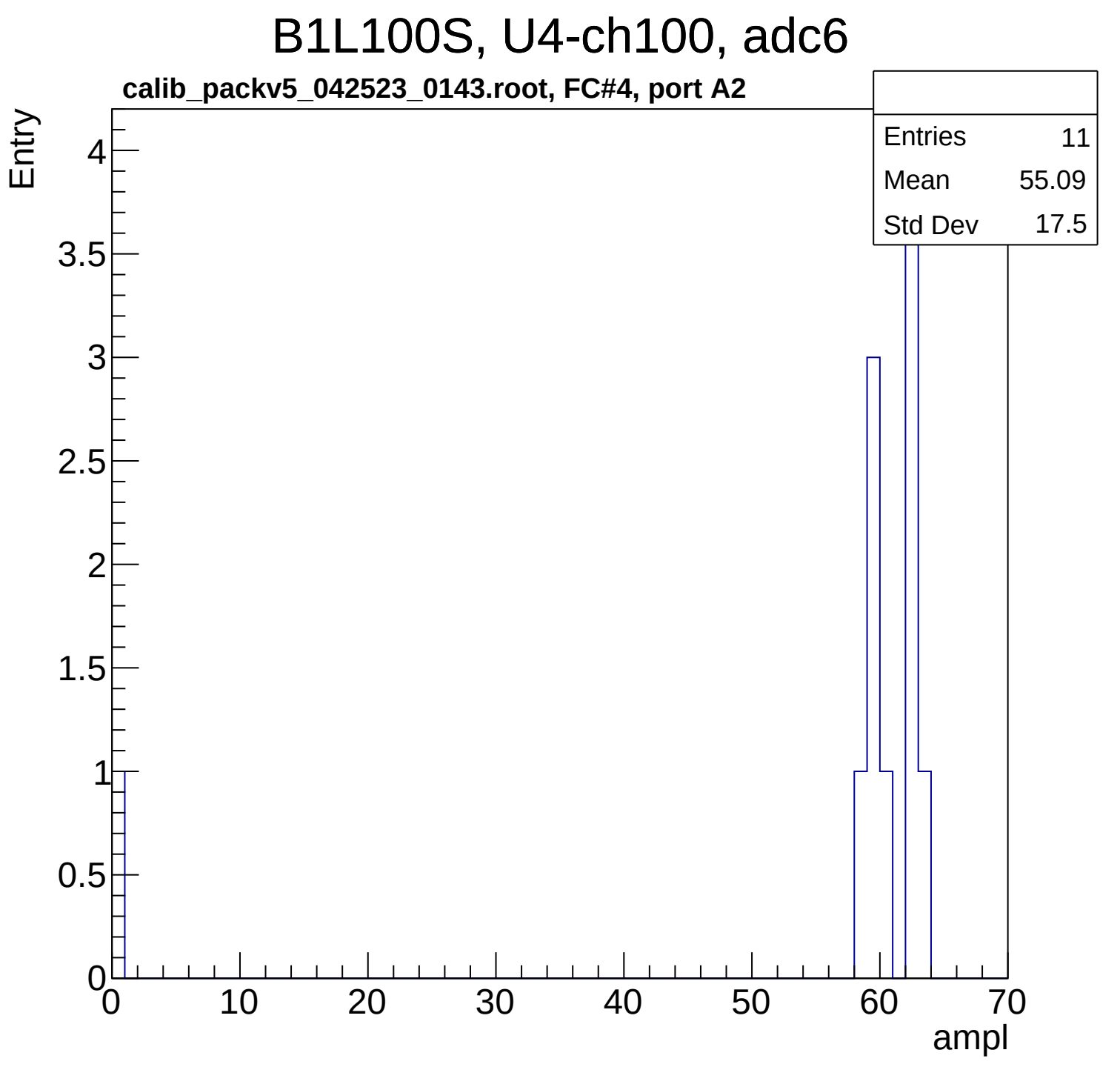

B1L100S, U4-ch100, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 35.65
Std Dev 3.788
Gaus mean : 36.0463
Gaus Width: 4.1963
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

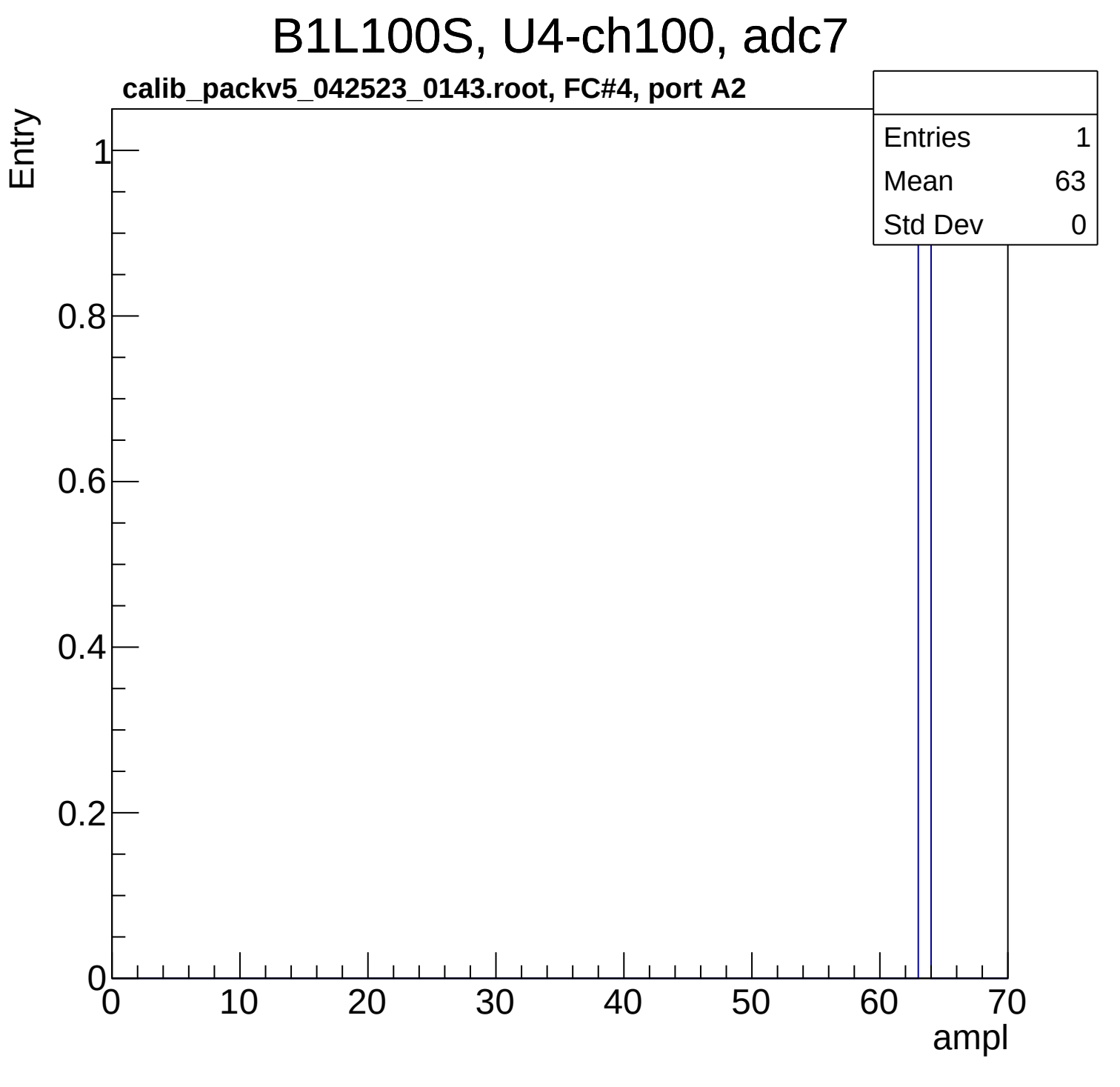

B1L100S, U4-ch100, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 42.95
Std Dev 3.735
Gaus mean : 43.4090
Gaus Width: 4.2866
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

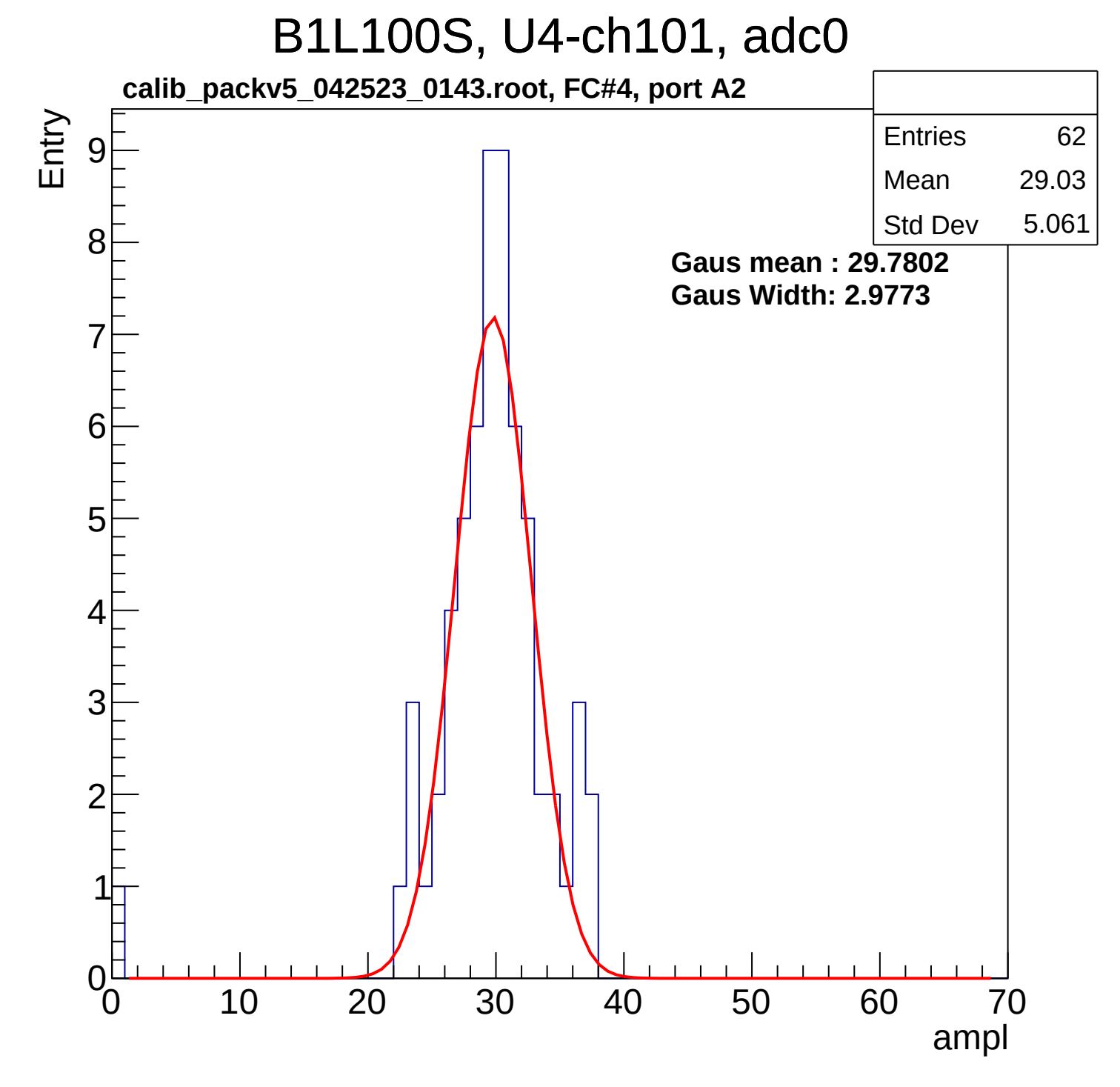

B1L100S, U4-ch100, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 47.91
Std Dev 3.955
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

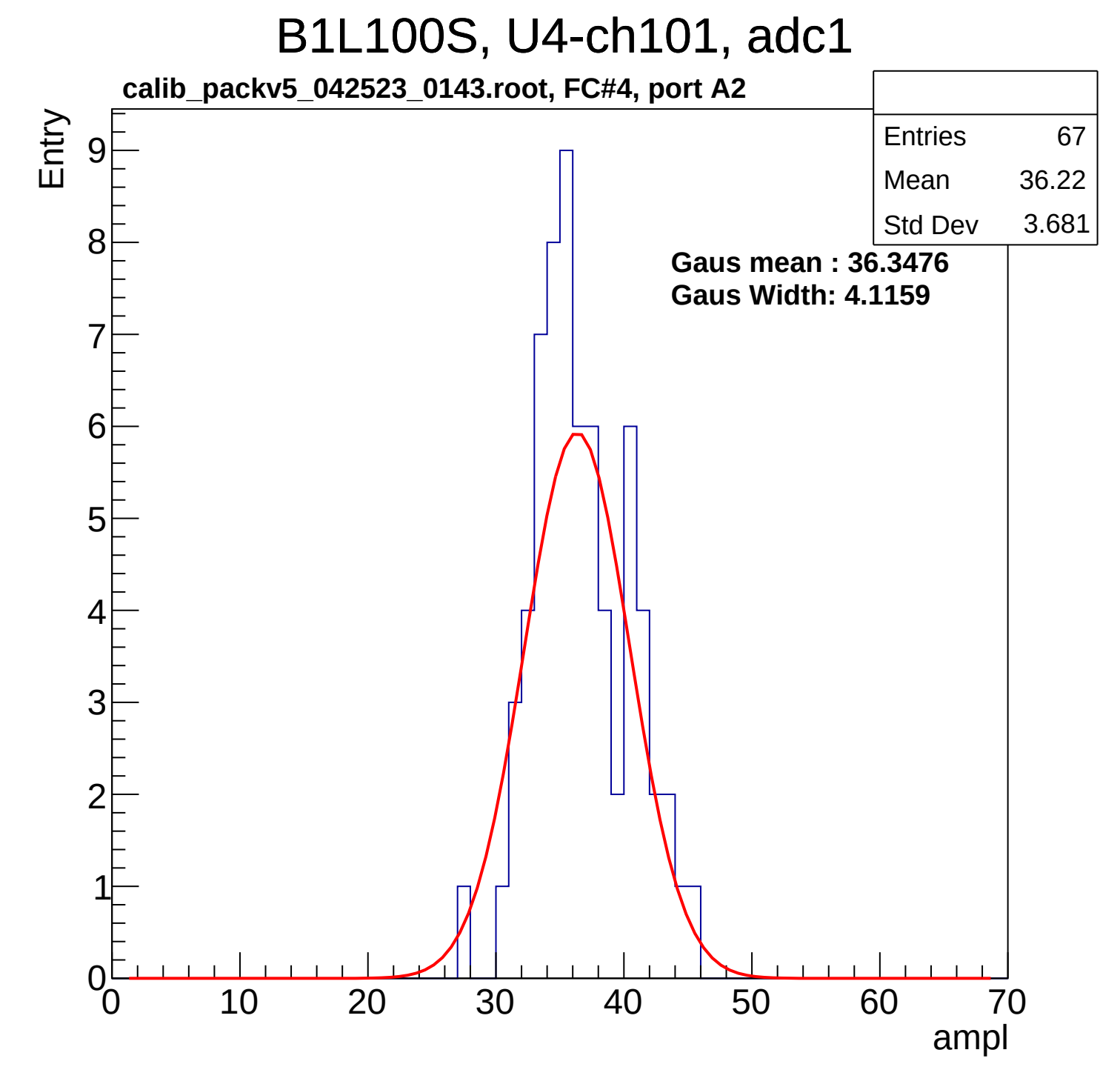

B1L100S, U4-ch100, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 53.84
Std Dev 3.237
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

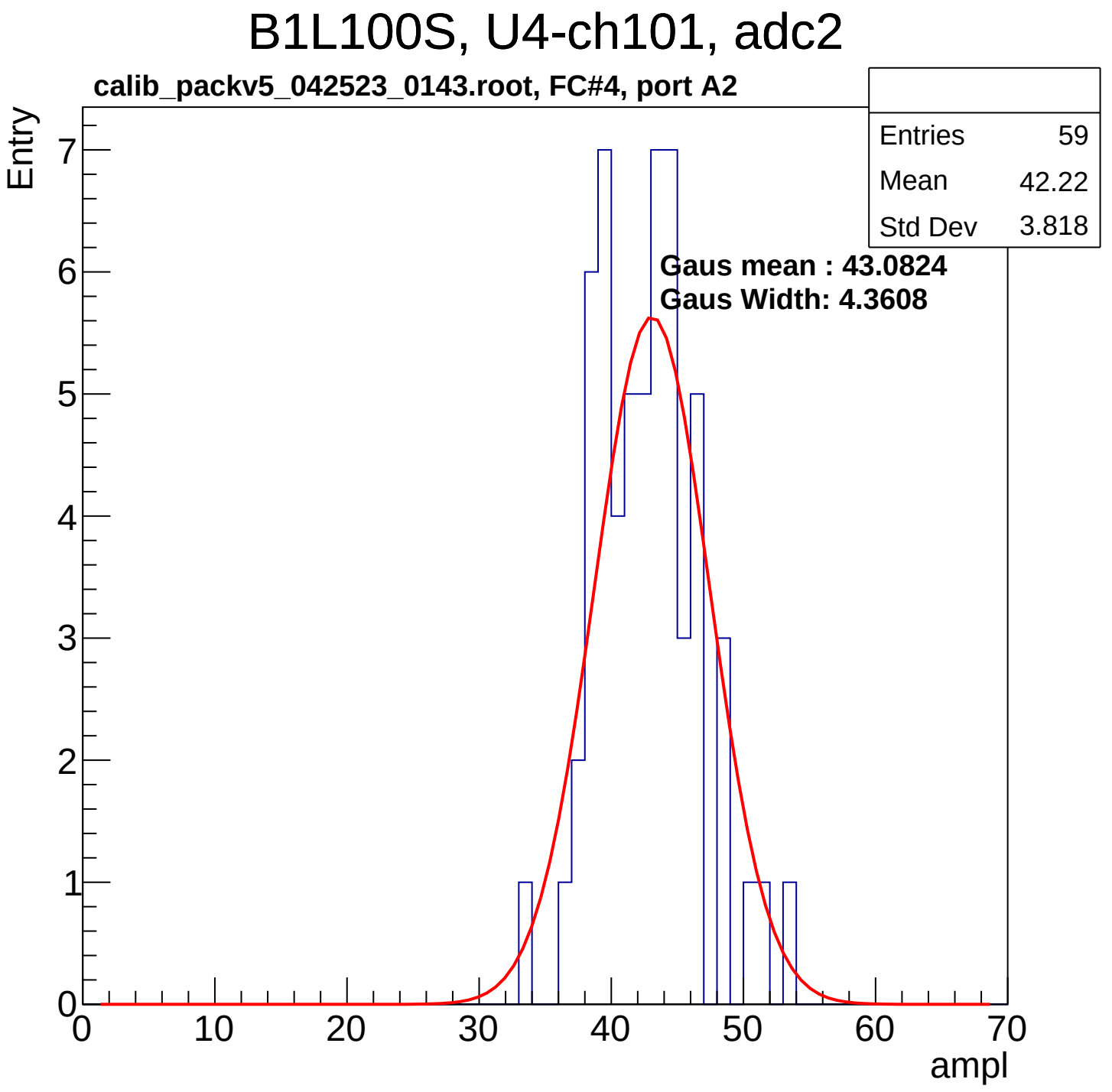

B1L100S, U4-ch100, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 59.84
Std Dev 2.318
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

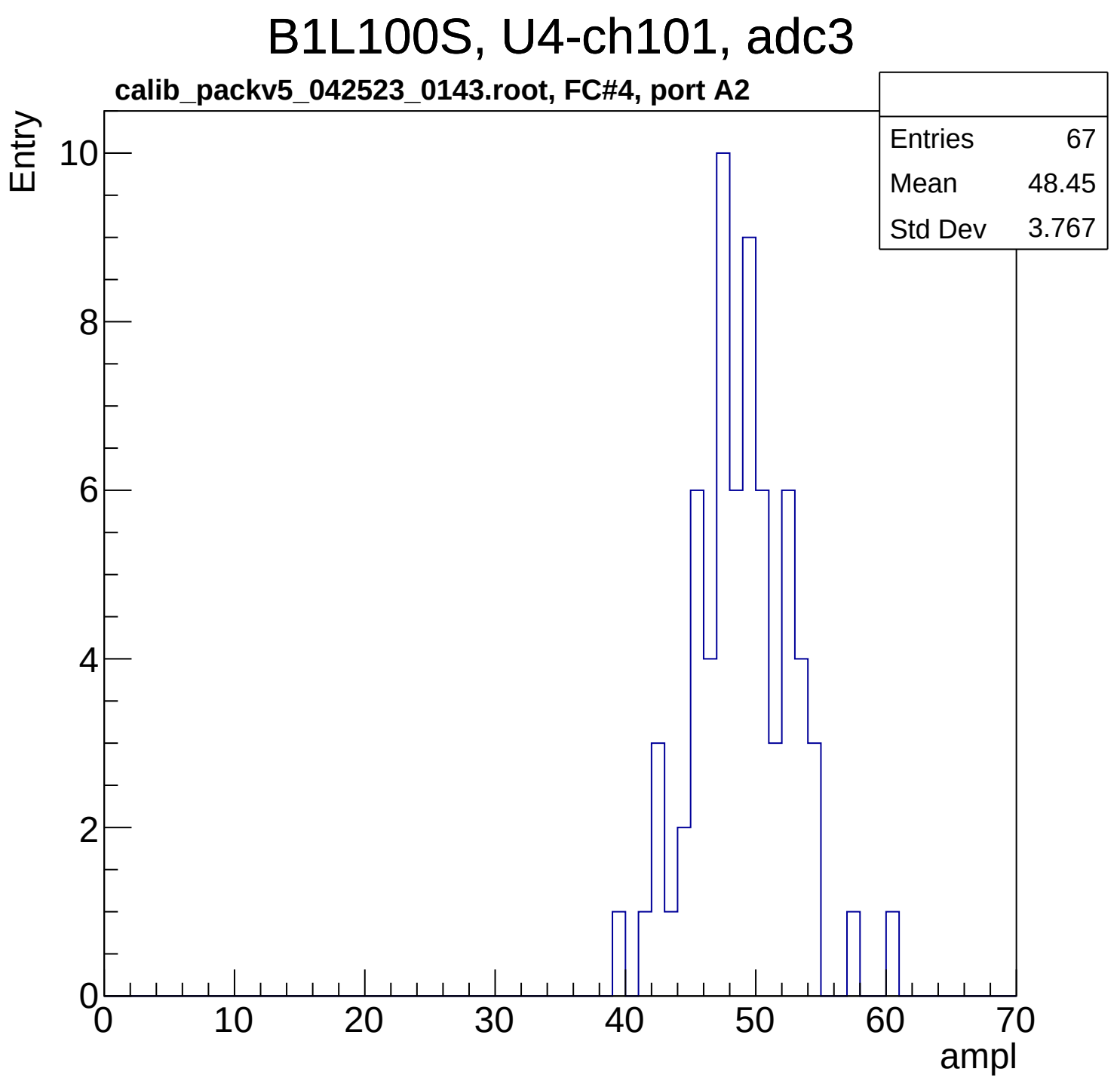

B1L100S, U4-ch100, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 55.09
Std Dev 17.5
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

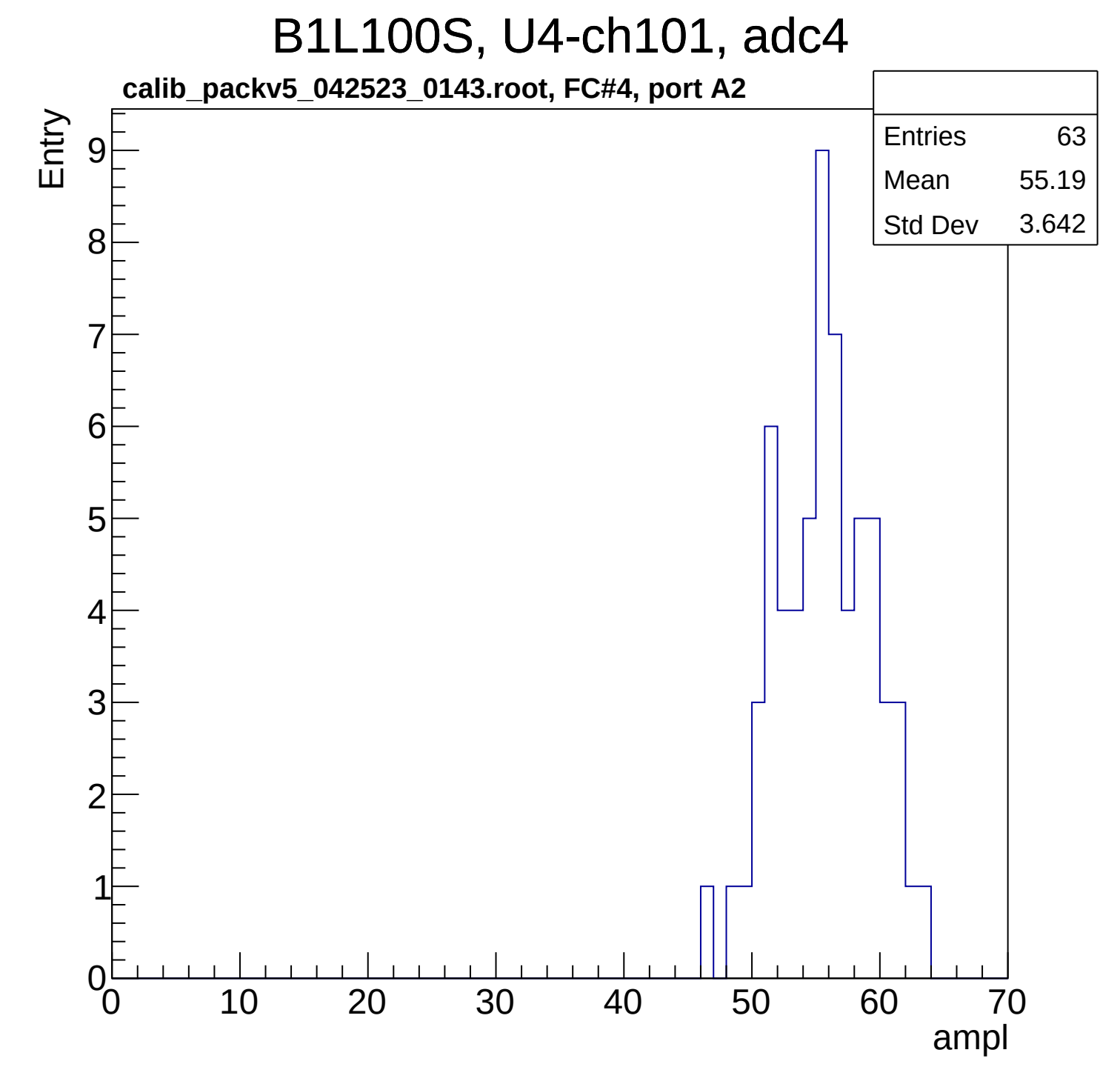

B1L100S, U4-ch100, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

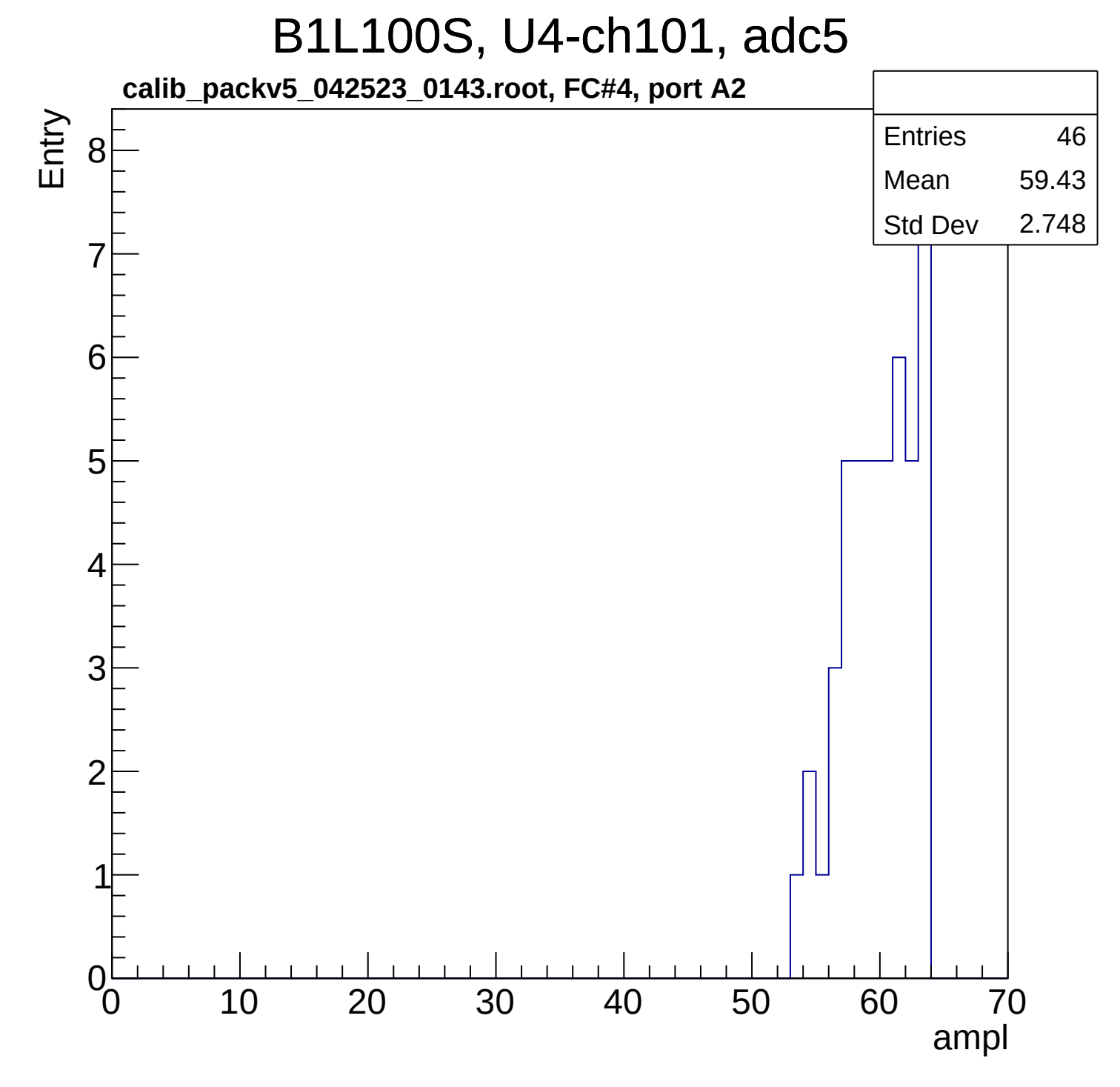

B1L100S, U4-ch101, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 29.03
Std Dev 5.061
Gaus mean : 29.7802
Gaus Width: 2.9773
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

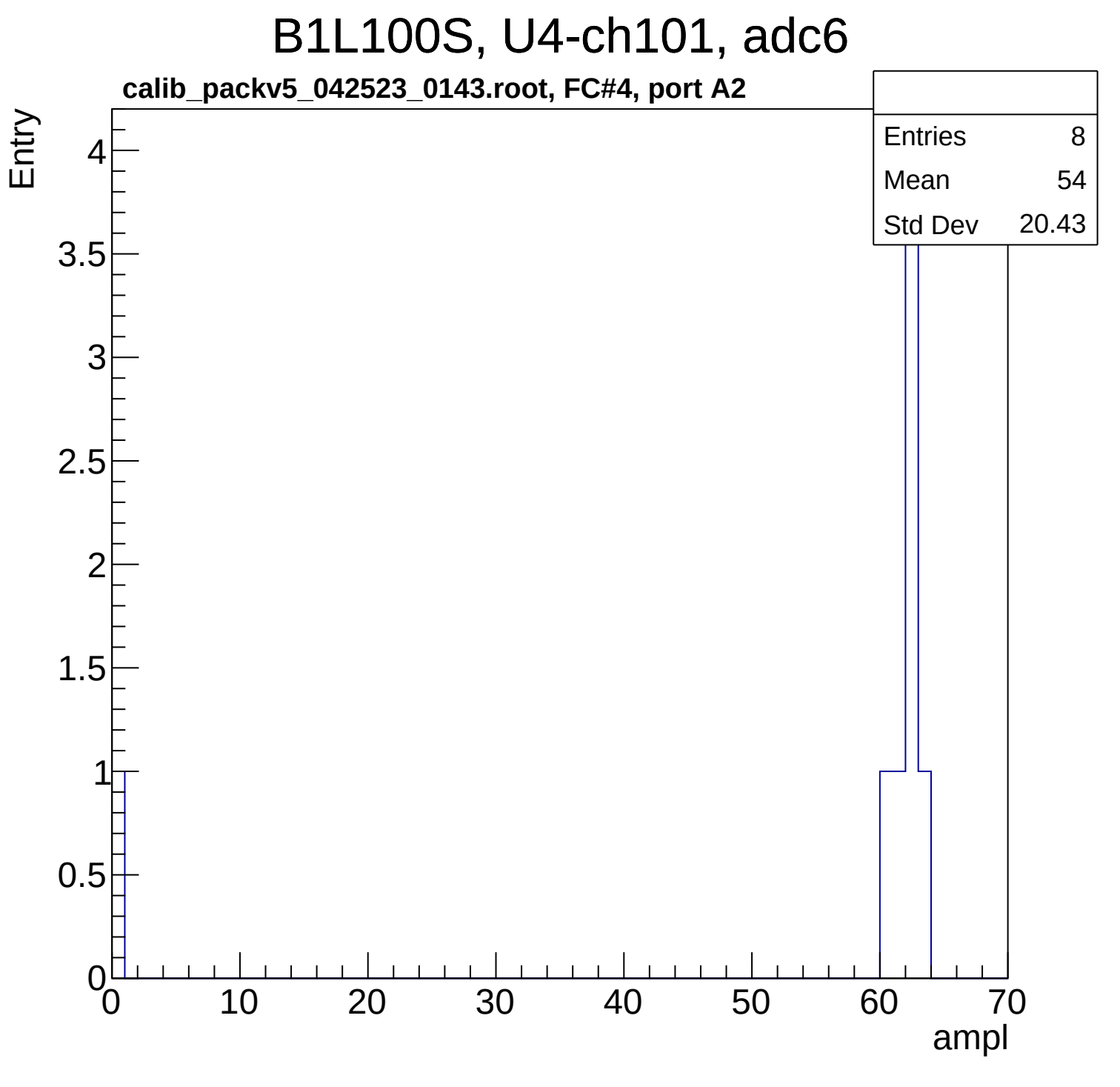

B1L100S, U4-ch101, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 36.22
Std Dev 3.681
Gaus mean : 36.3476
Gaus Width: 4.1159
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

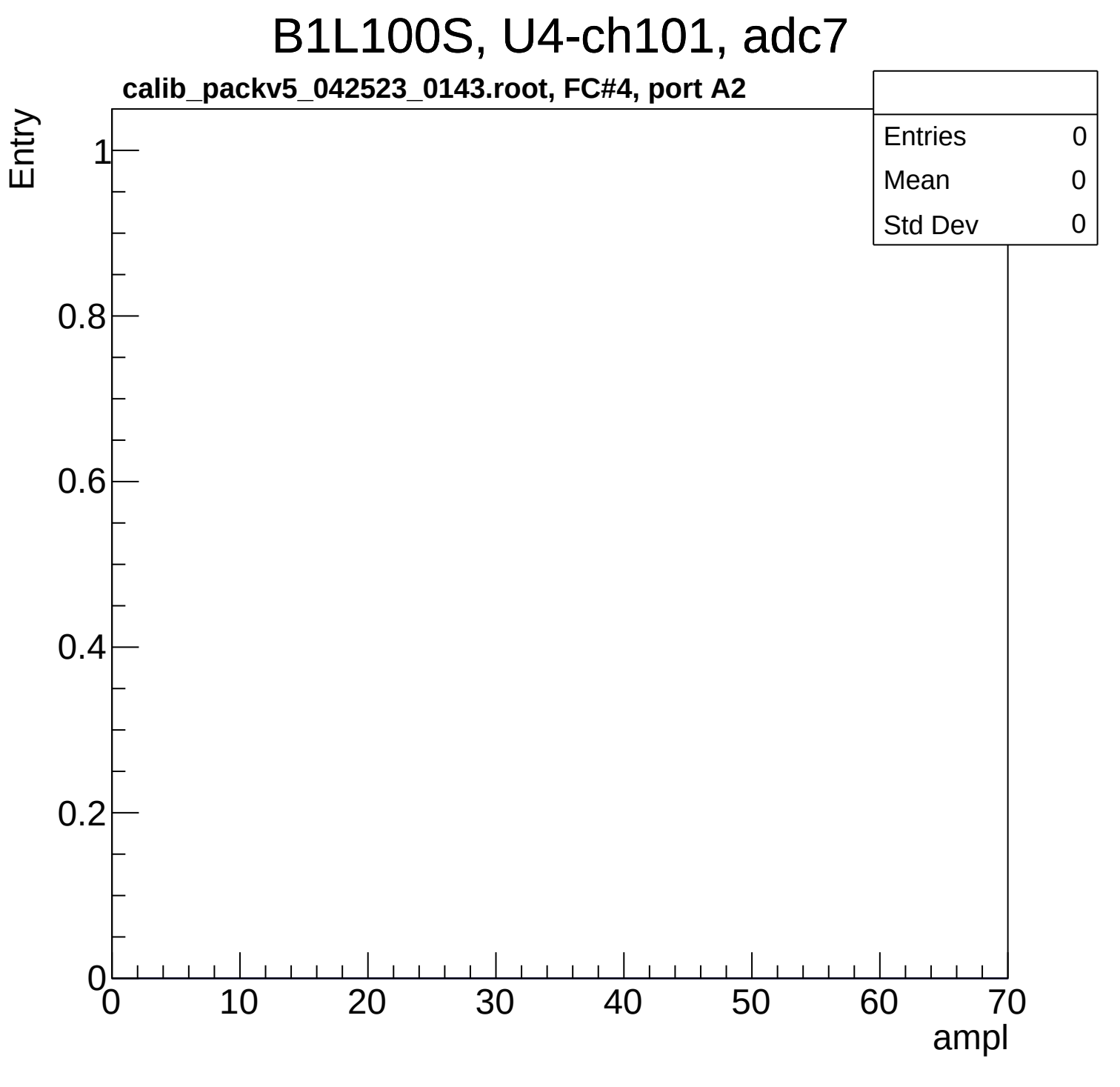

B1L100S, U4-ch101, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 42.22
Std Dev 3.818
Gaus mean : 43.0824
Gaus Width: 4.3608
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

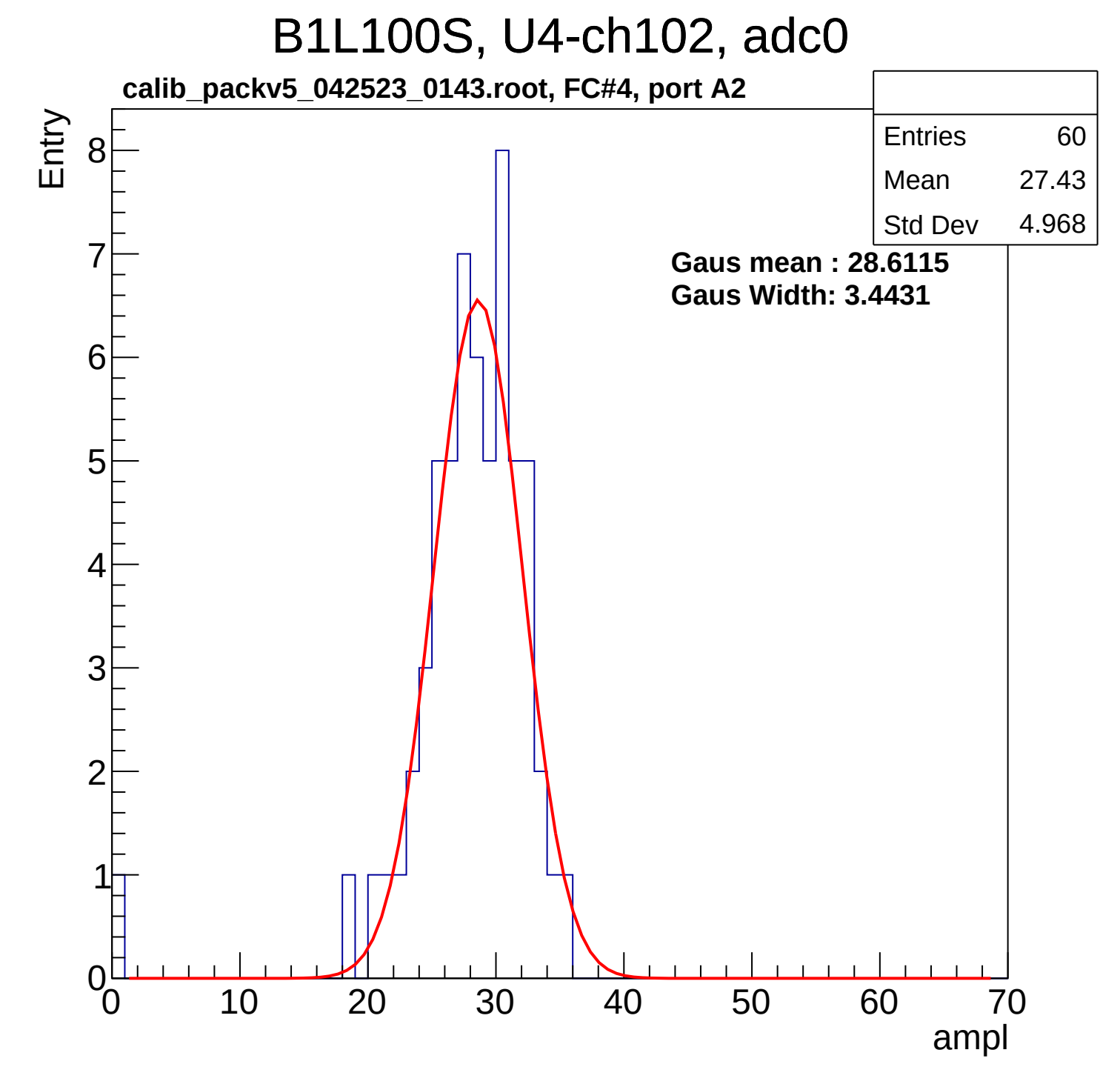

B1L100S, U4-ch101, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 48.45
Std Dev 3.767
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

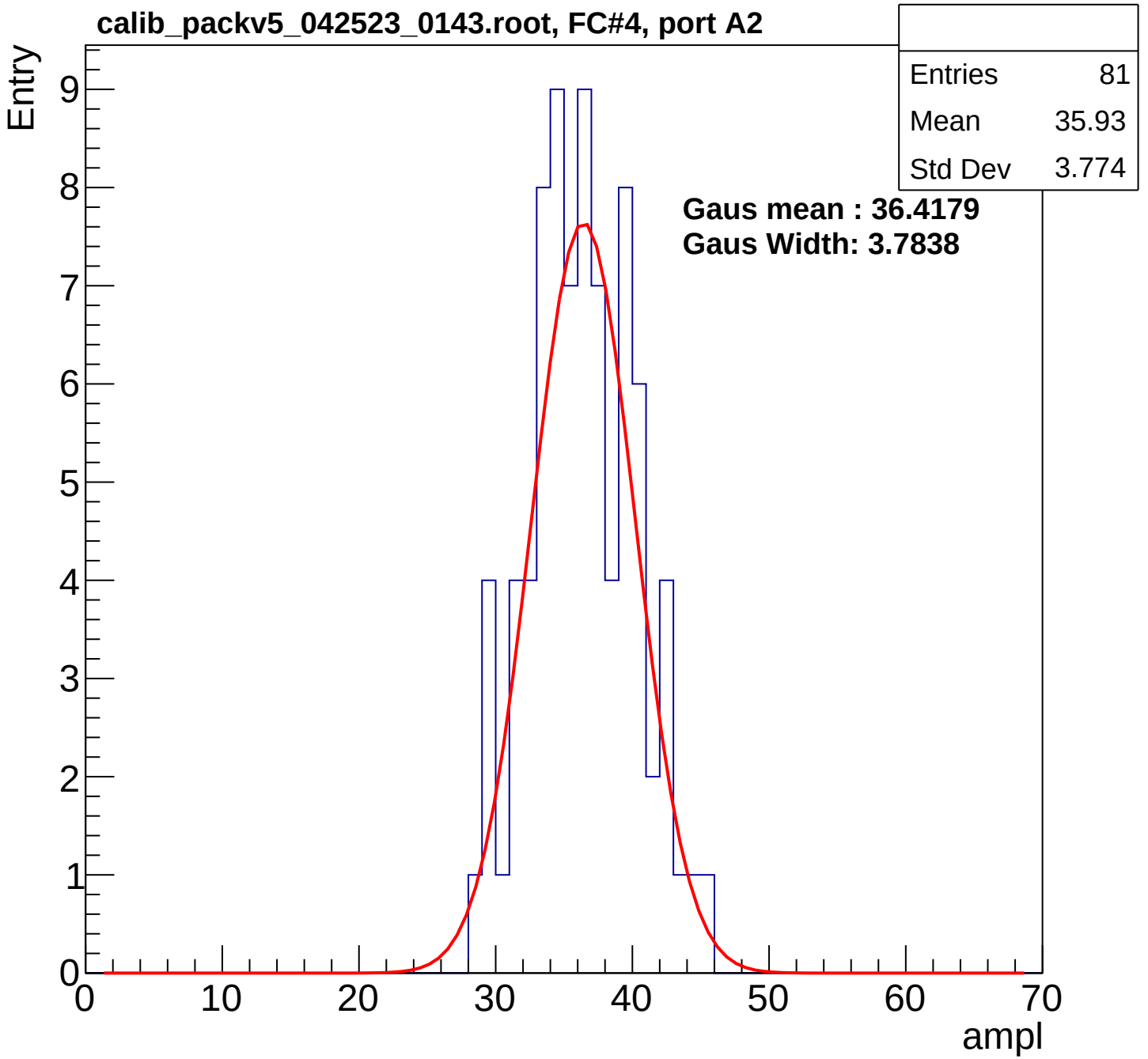

B1L100S, U4-ch101, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 55.19
Std Dev 3.642
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

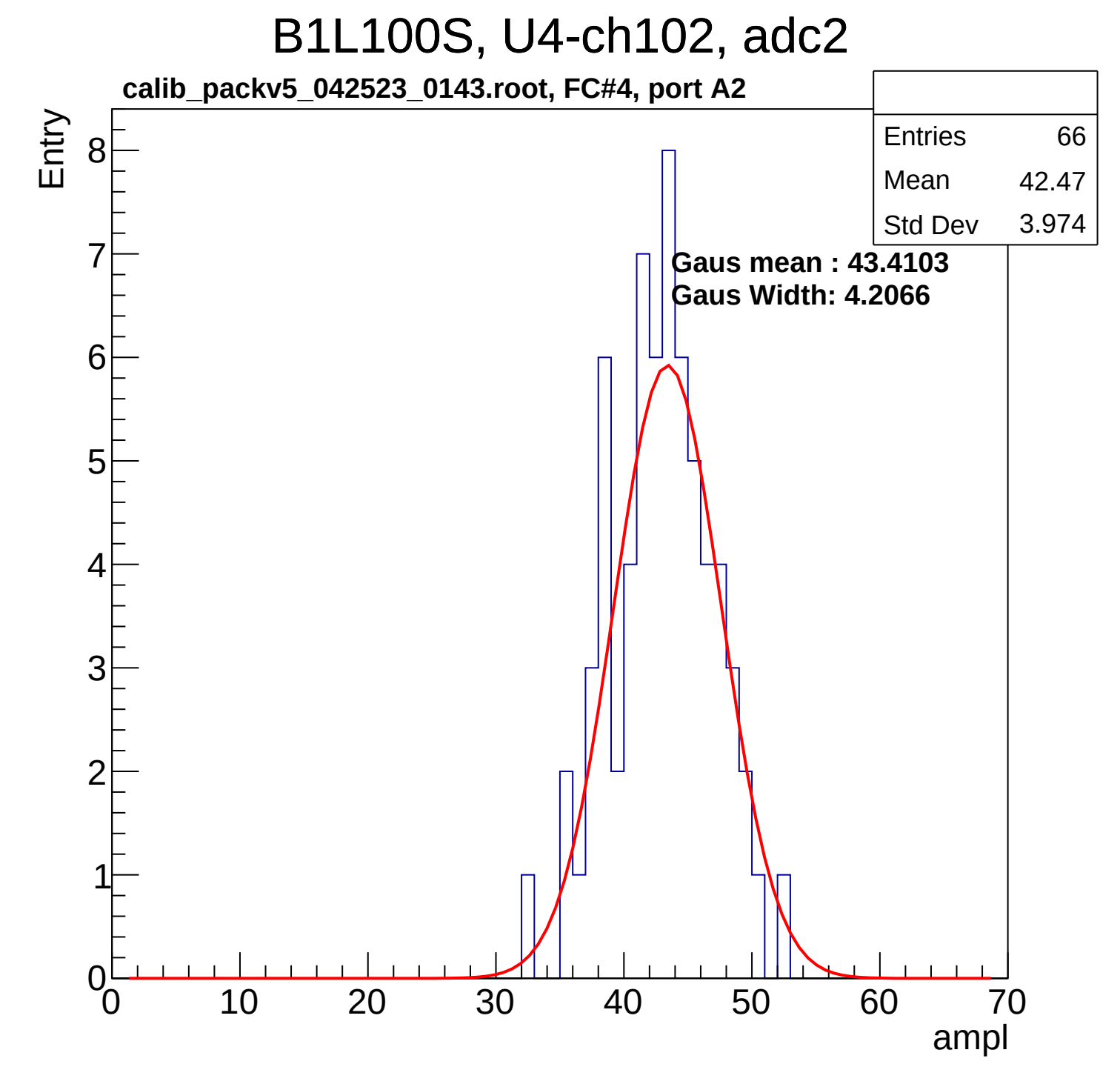

B1L100S, U4-ch101, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 59.43
Std Dev 2.748
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

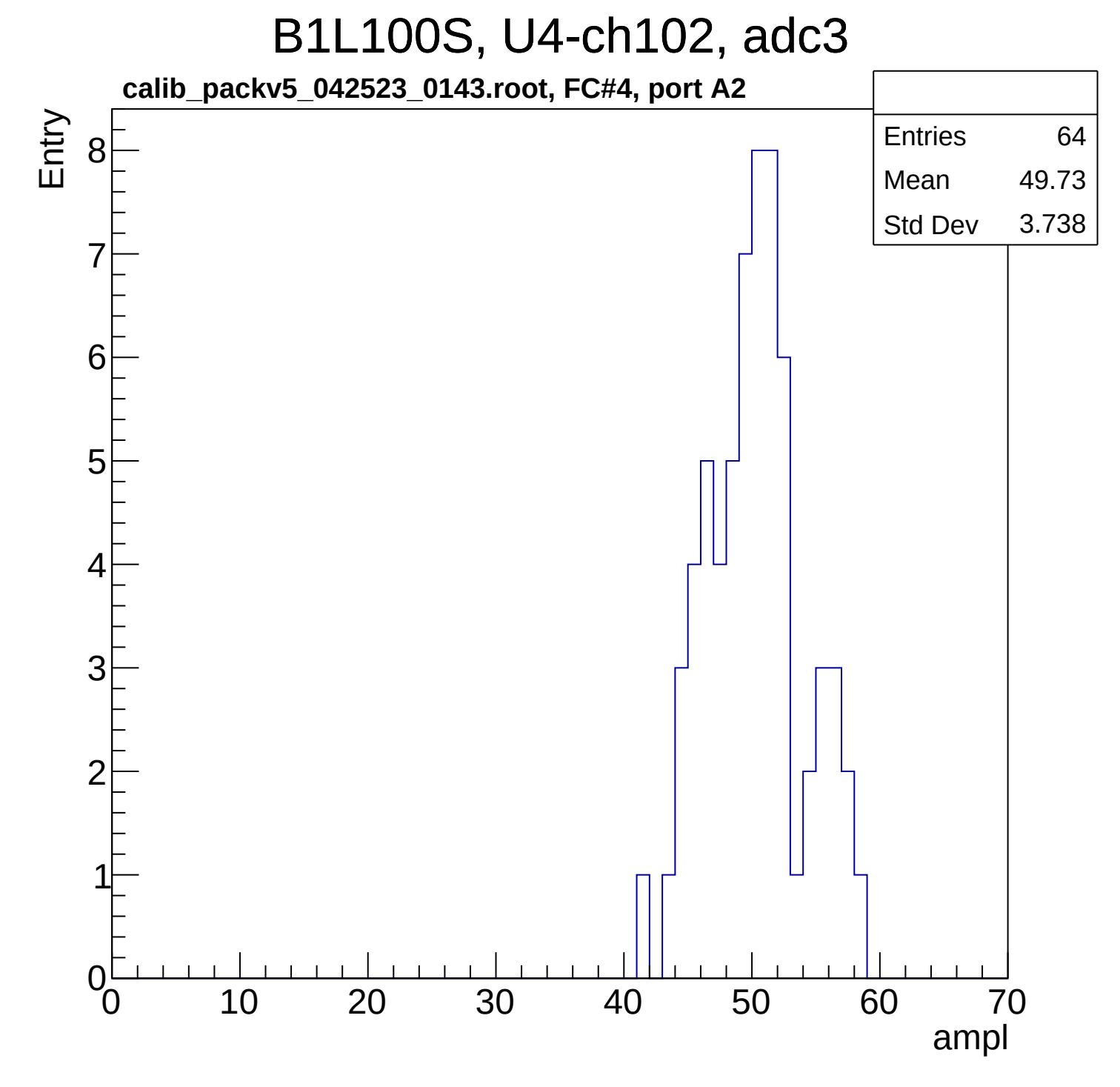

B1L100S, U4-ch101, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 8
Mean 54
Std Dev 20.43
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

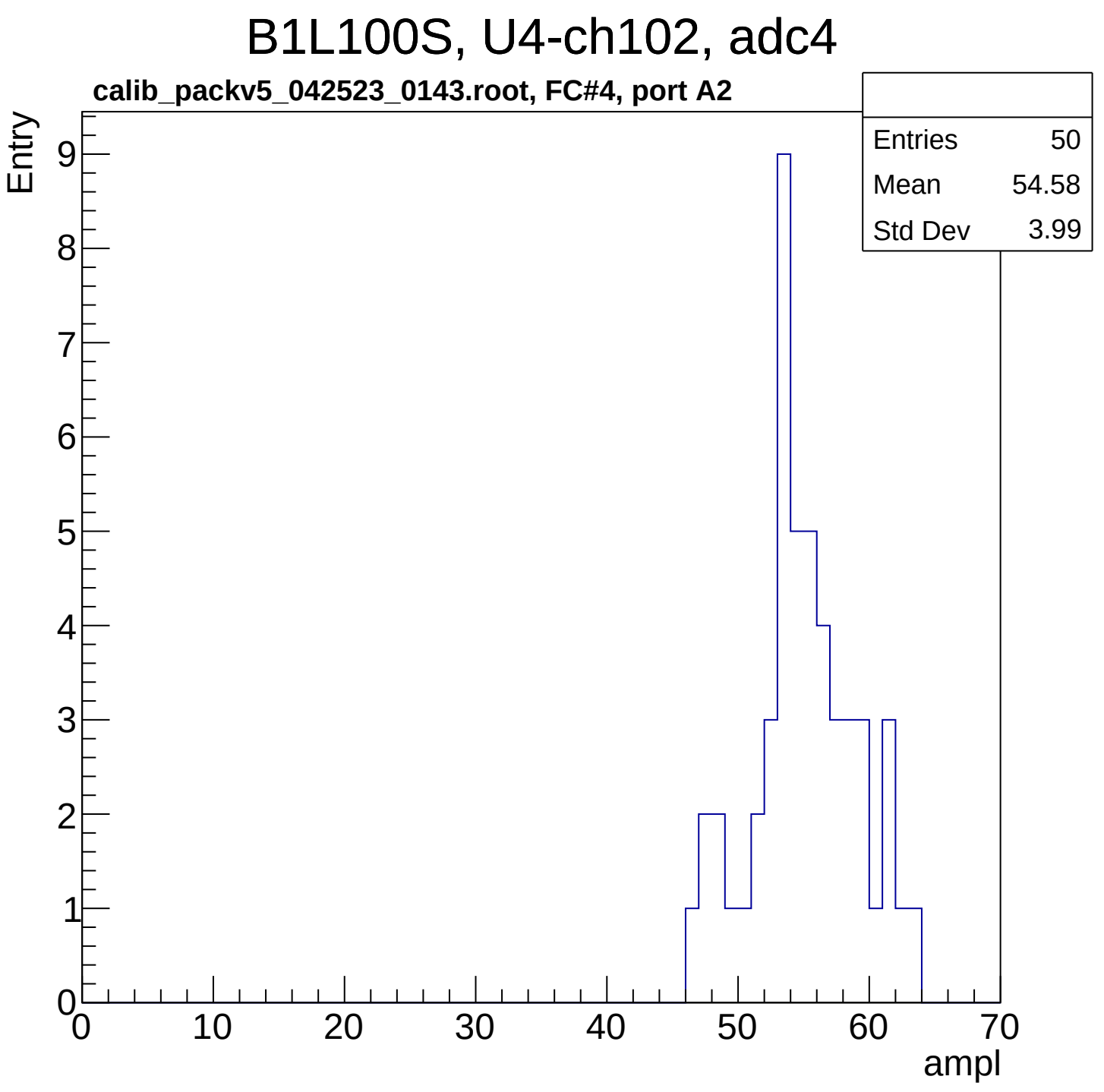

B1L100S, U4-ch101, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

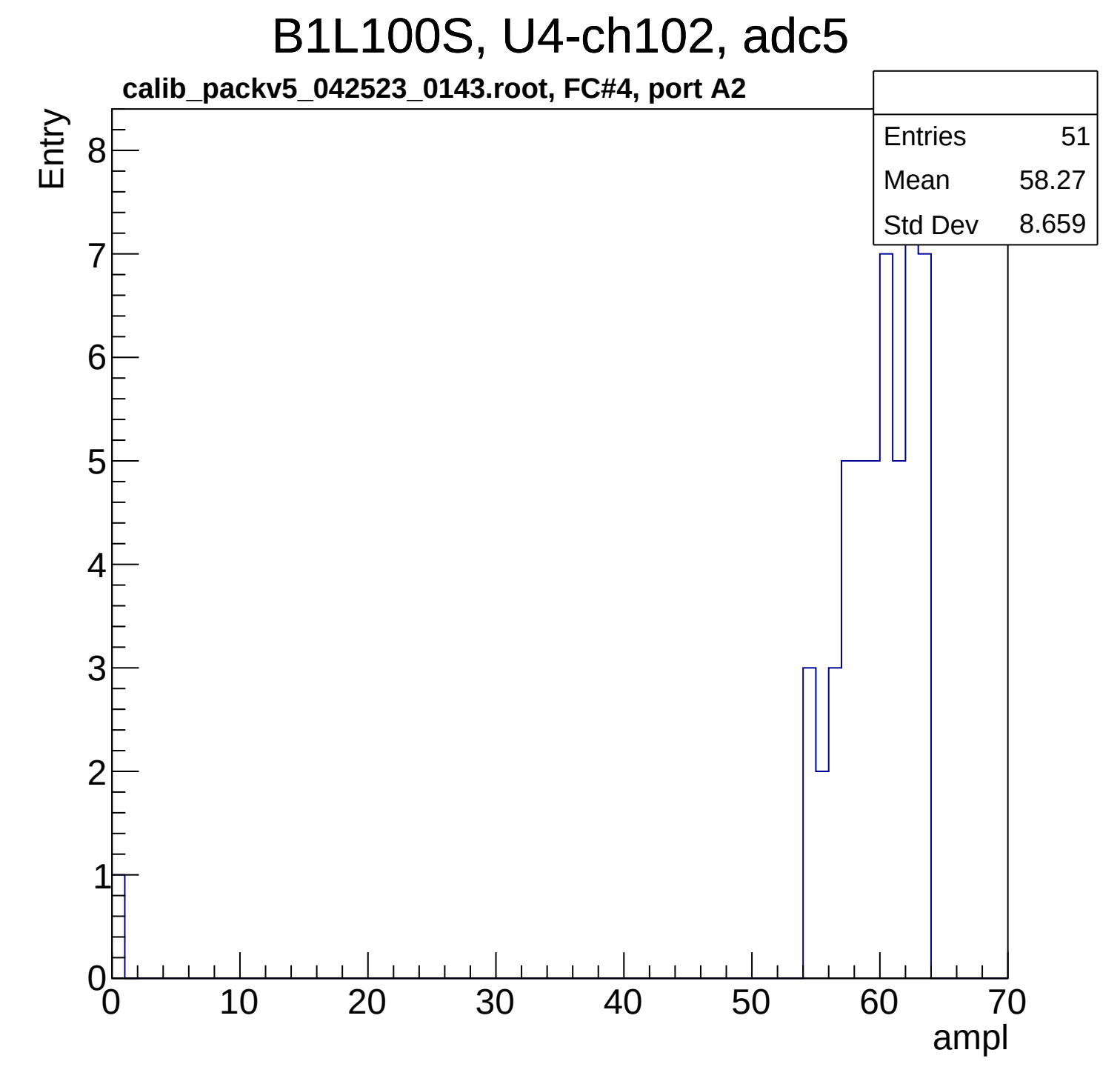

B1L100S, U4-ch102, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 27.43
Std Dev 4.968
Gaus mean : 28.6115
Gaus Width: 3.4431
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

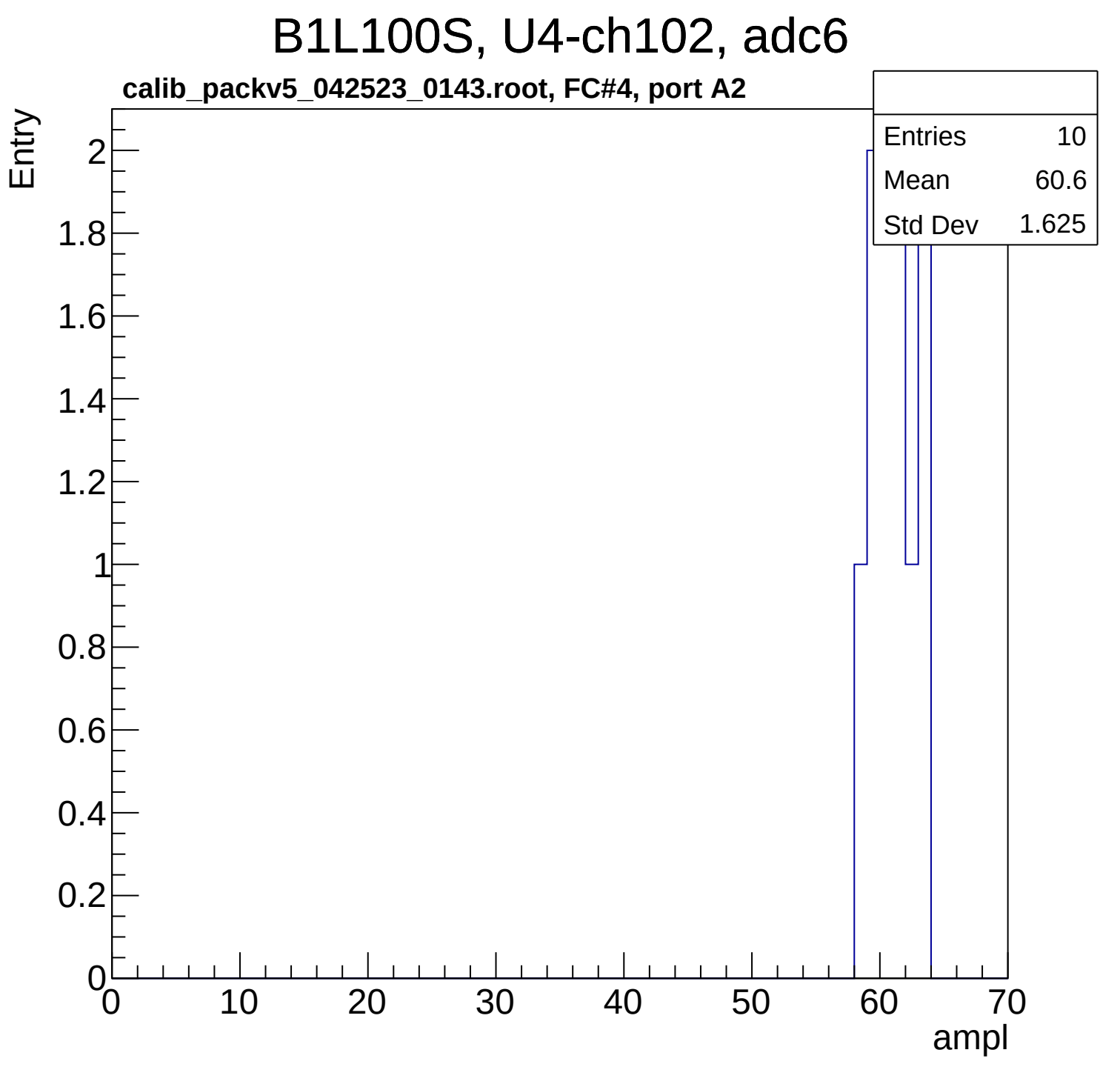

B1L100S, U4-ch102, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 35.93
Std Dev 3.774
Gaus mean : 36.4179
Gaus Width: 3.7838
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

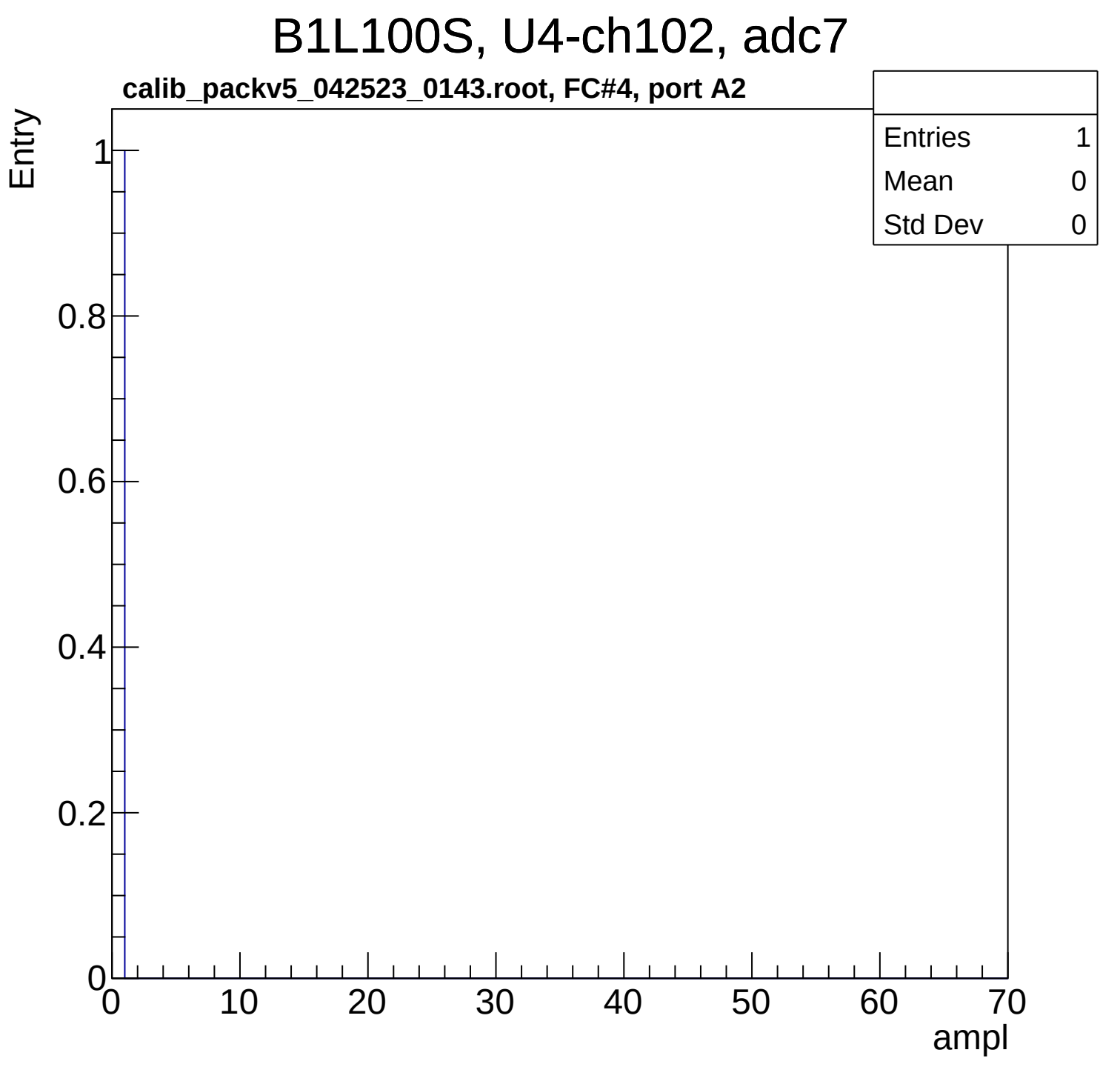

B1L100S, U4-ch102, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 42.47
Std Dev 3.974
Gaus mean : 43.4103
Gaus Width: 4.2066
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

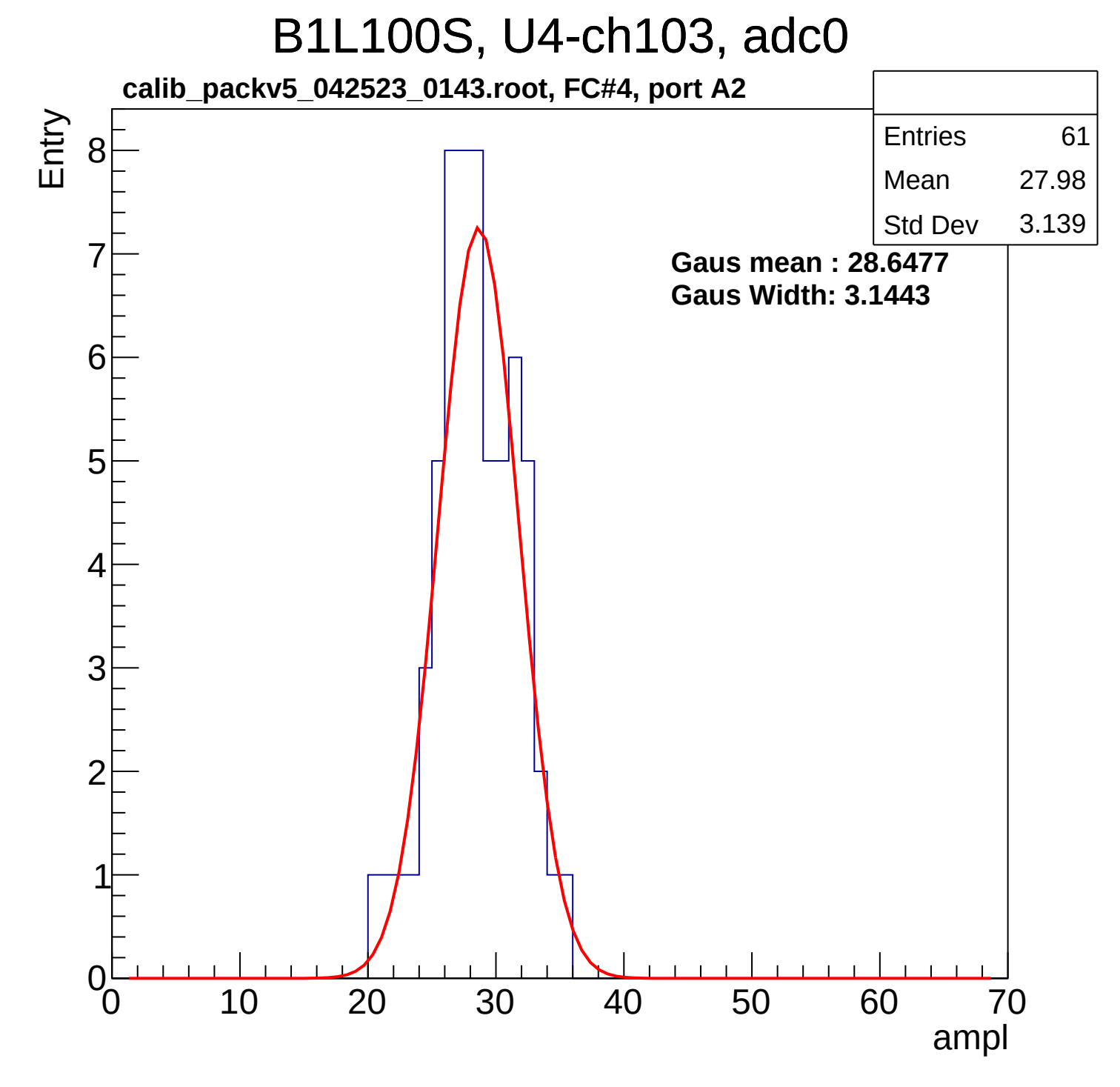

B1L100S, U4-ch102, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 49.73
Std Dev 3.738
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

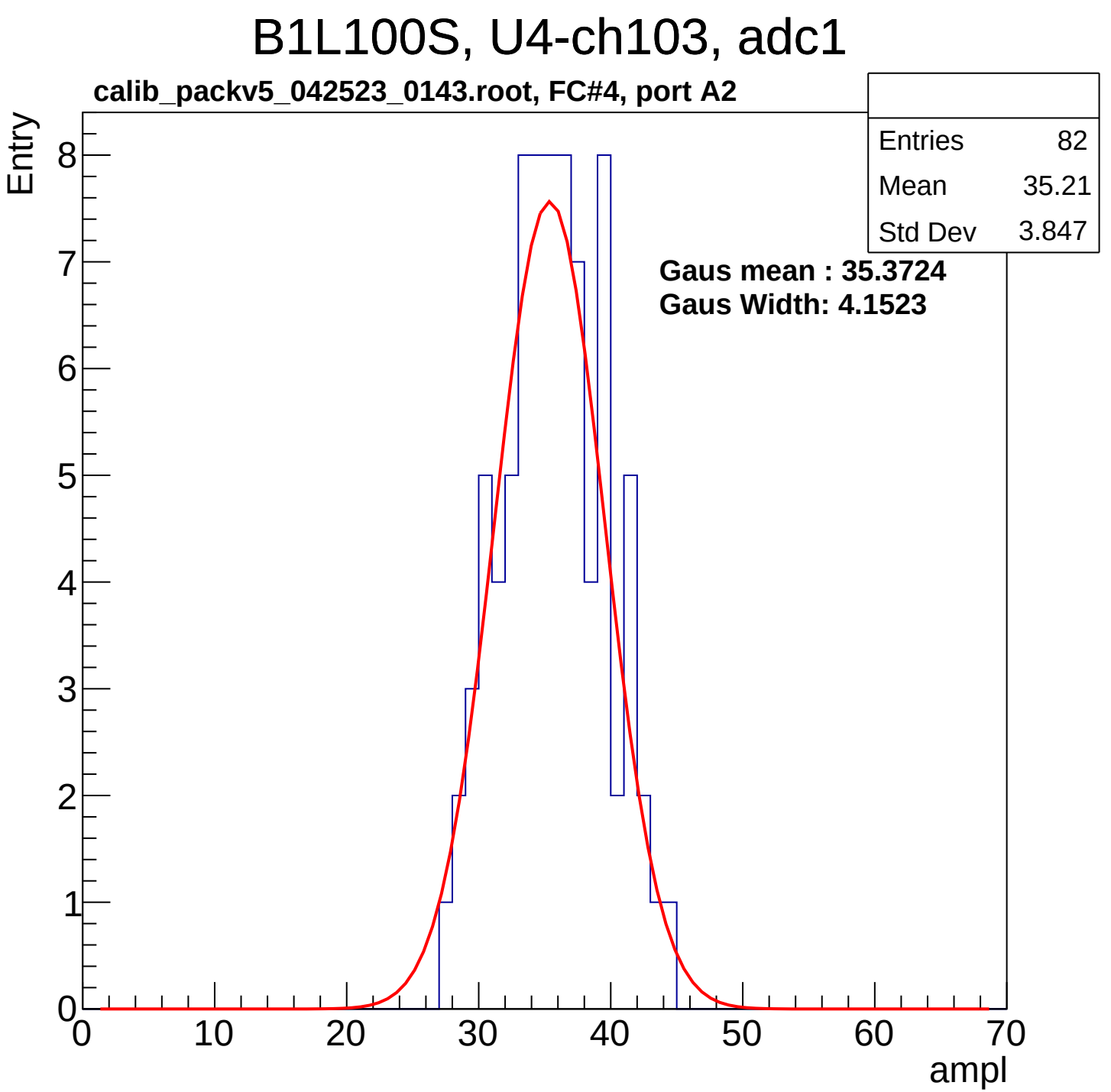

B1L100S, U4-ch102, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 54.58
Std Dev 3.99
Entry
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70
ampl

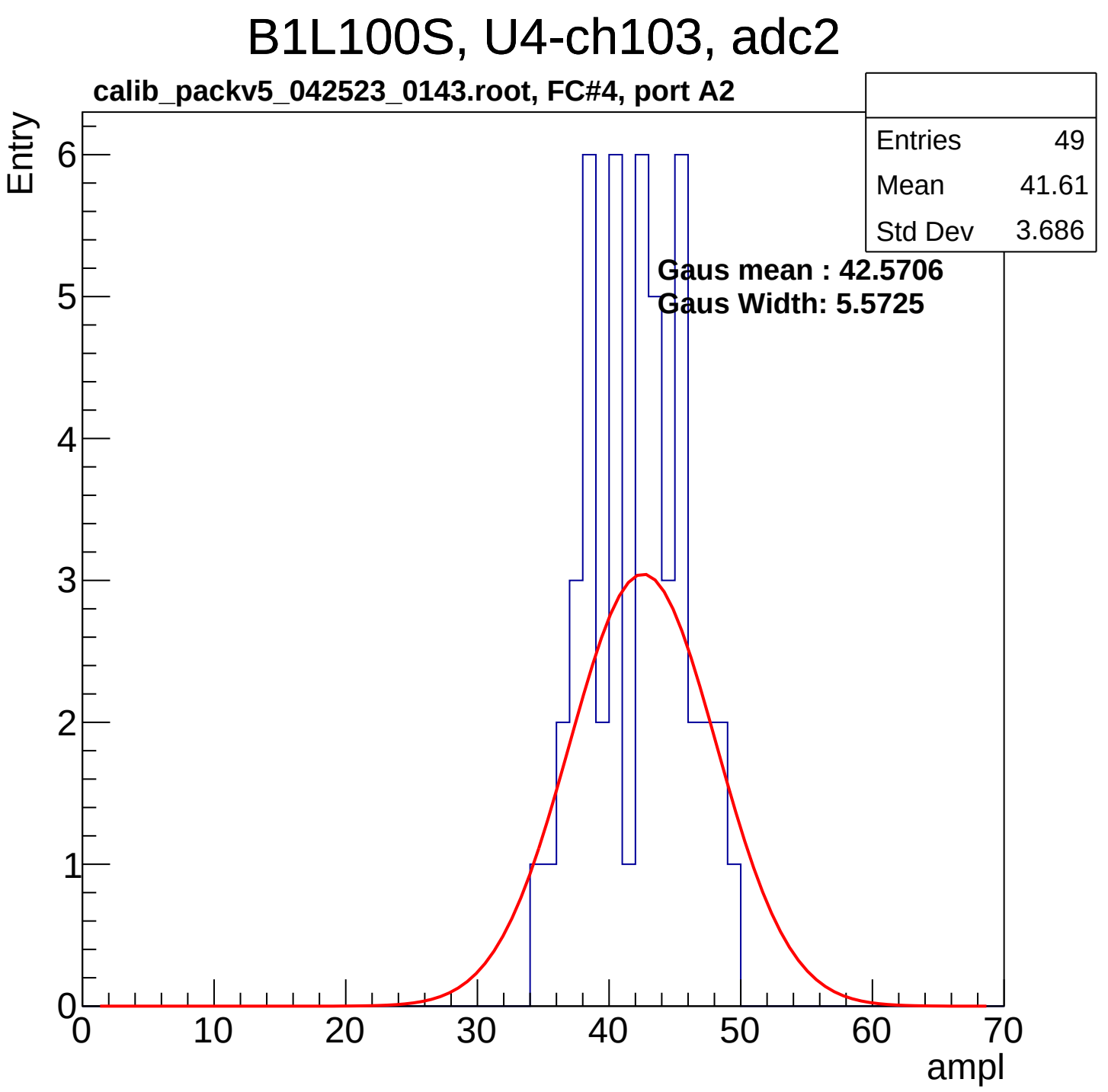

B1L100S, U4-ch102, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 58.27
Std Dev 8.659
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

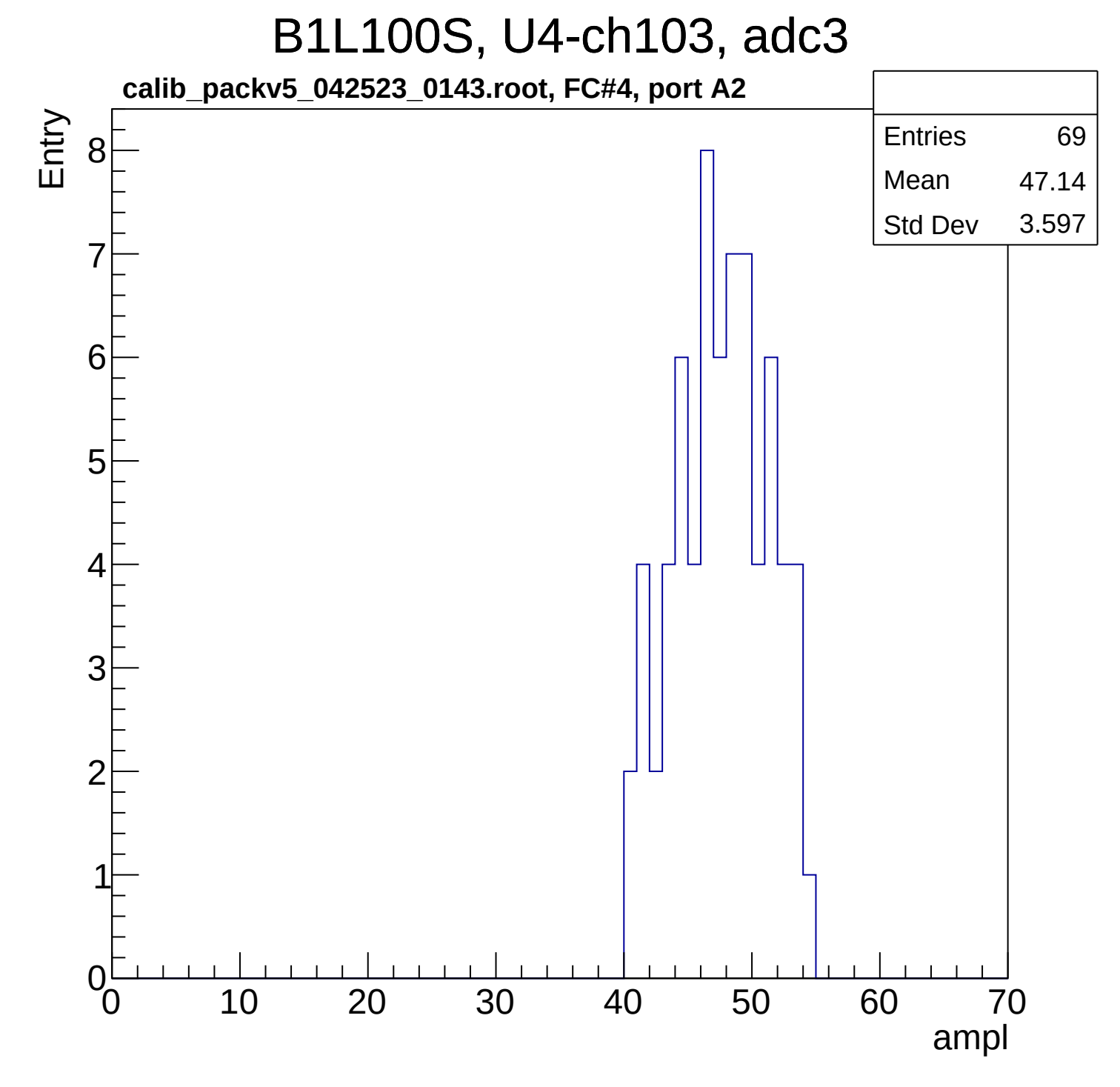

B1L100S, U4-ch102, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 60.6
Std Dev 1.625
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

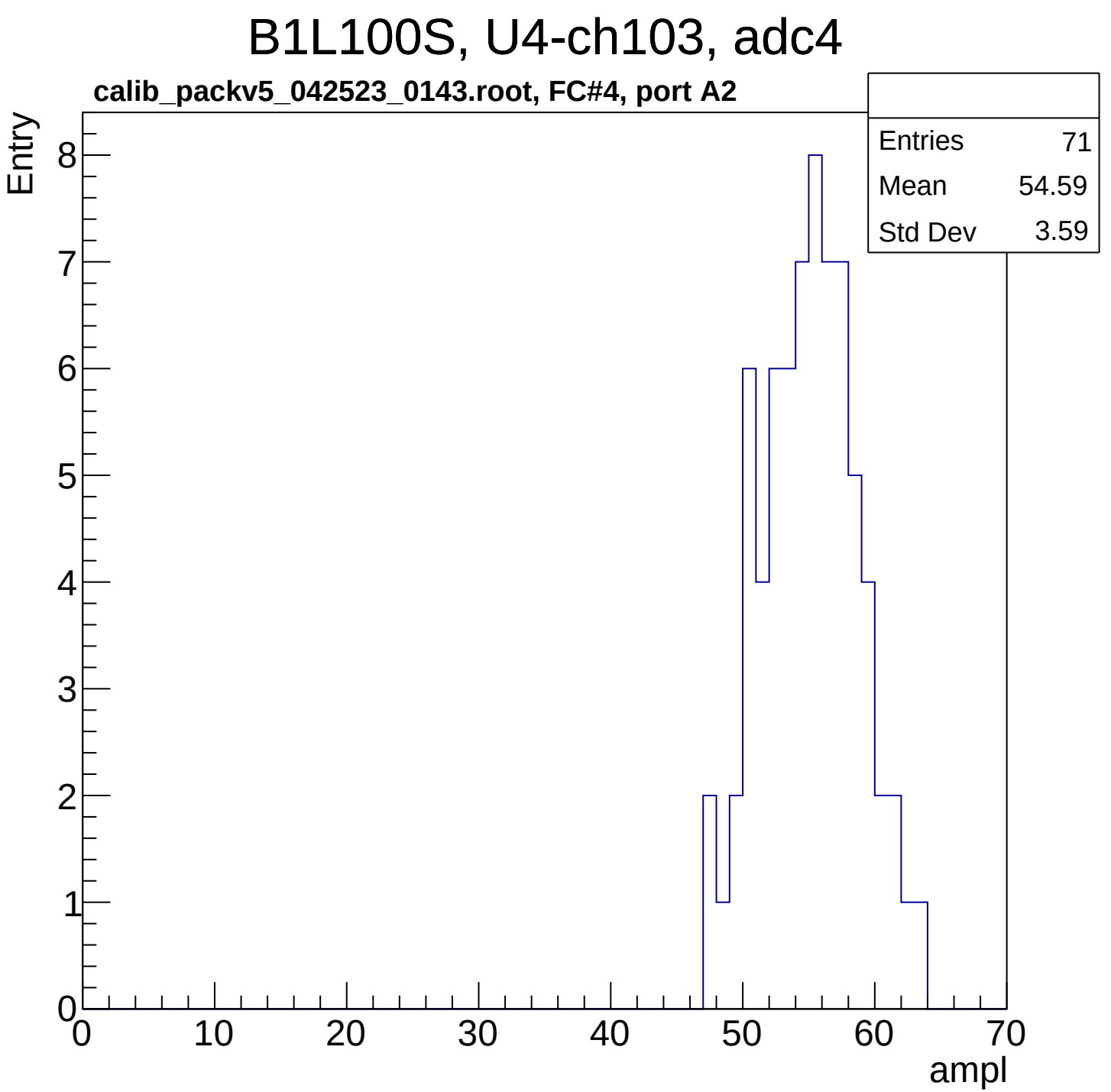

B1L100S, U4-ch102, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

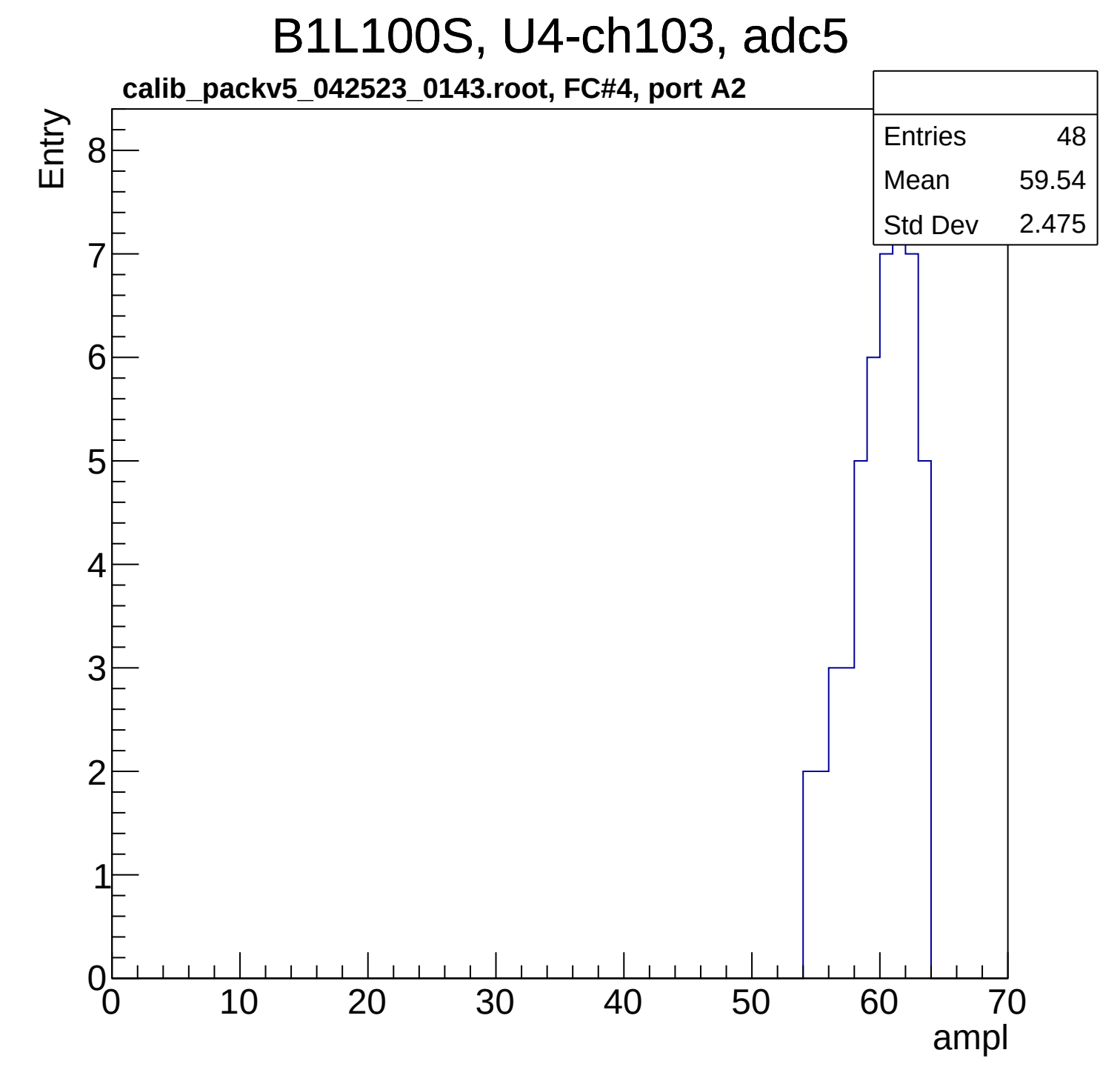

B1L100S, U4-ch103, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 27.98
Std Dev 3.139
Gaus mean : 28.6477
Gaus Width: 3.1443
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

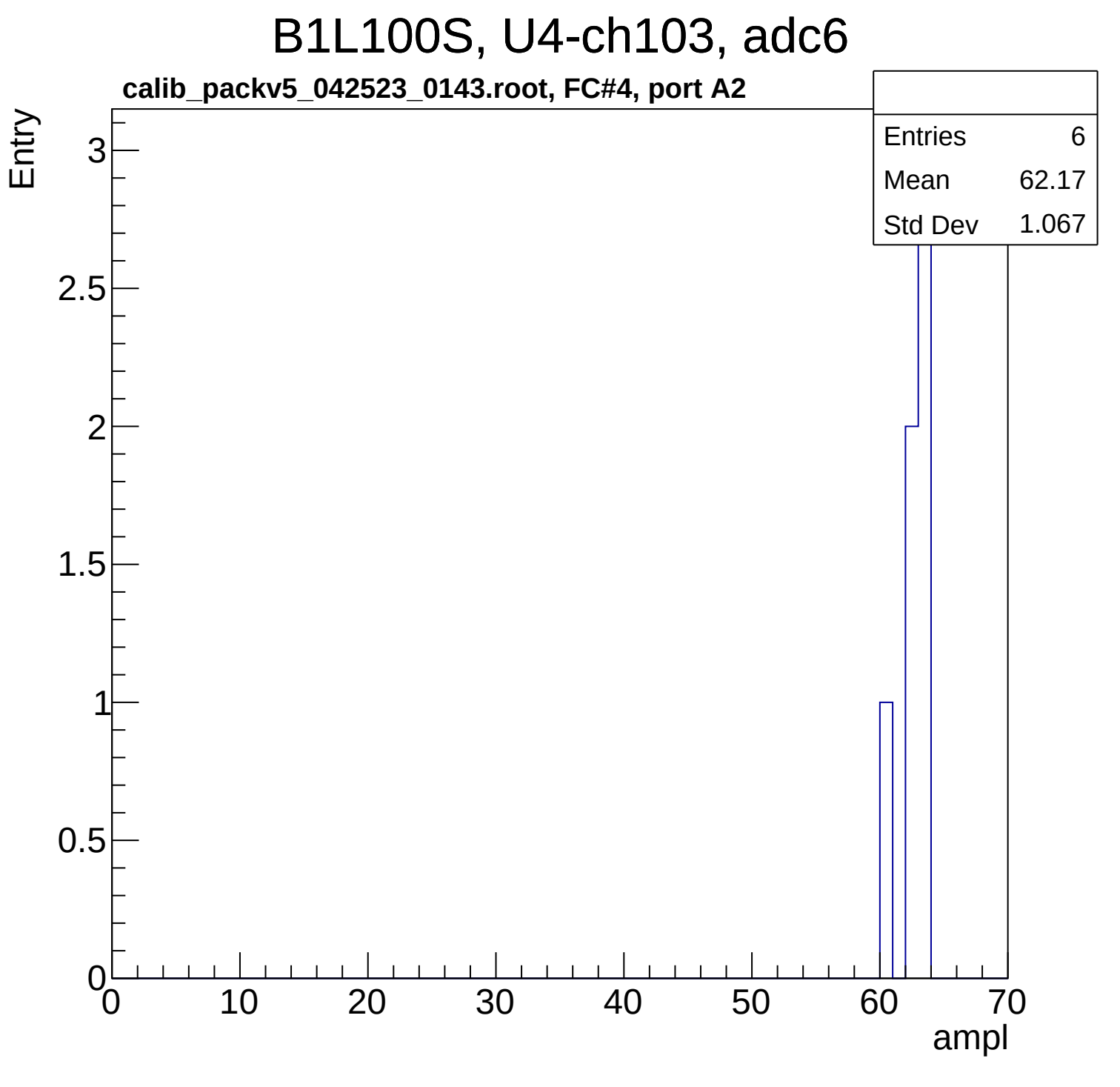

B1L100S, U4-ch103, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 35.21
Std Dev 3.847
Gaus mean : 35.3724
Gaus Width: 4.1523
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

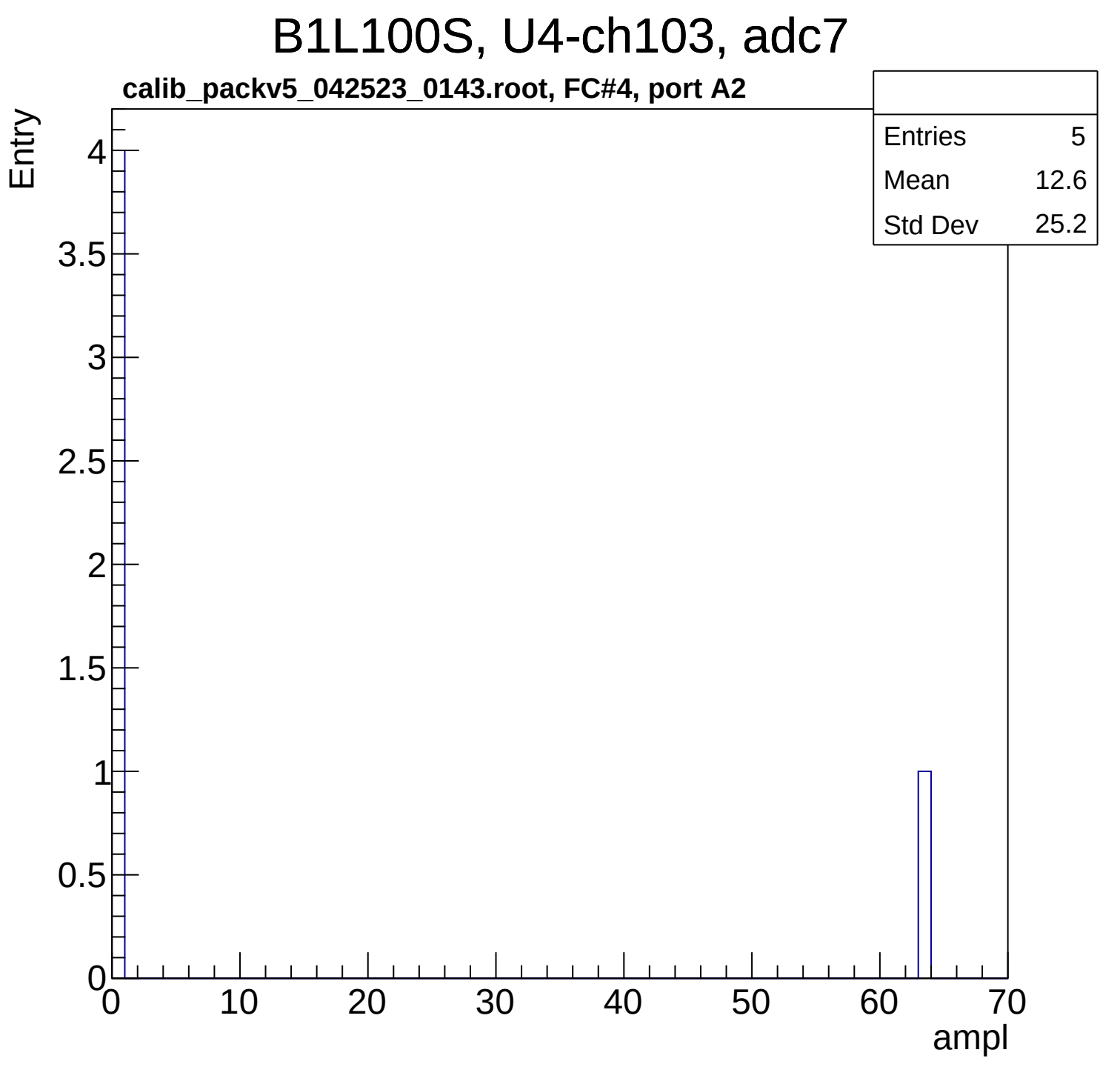

B1L100S, U4-ch103, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 41.61
Std Dev 3.686
Gaus mean : 42.5706
Gaus Width: 5.5725
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

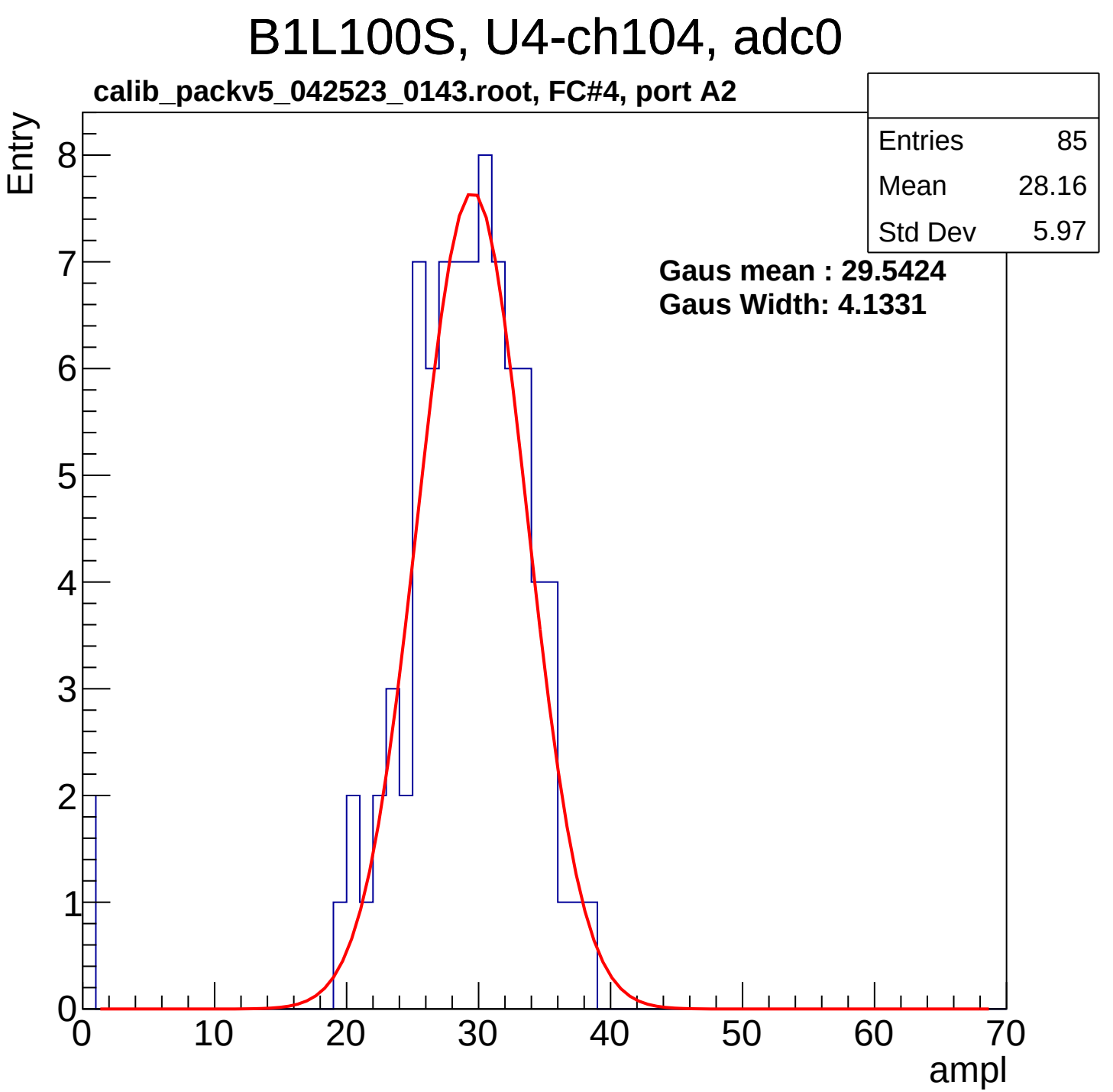

B1L100S, U4-ch103, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 47.14
Std Dev 3.597
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

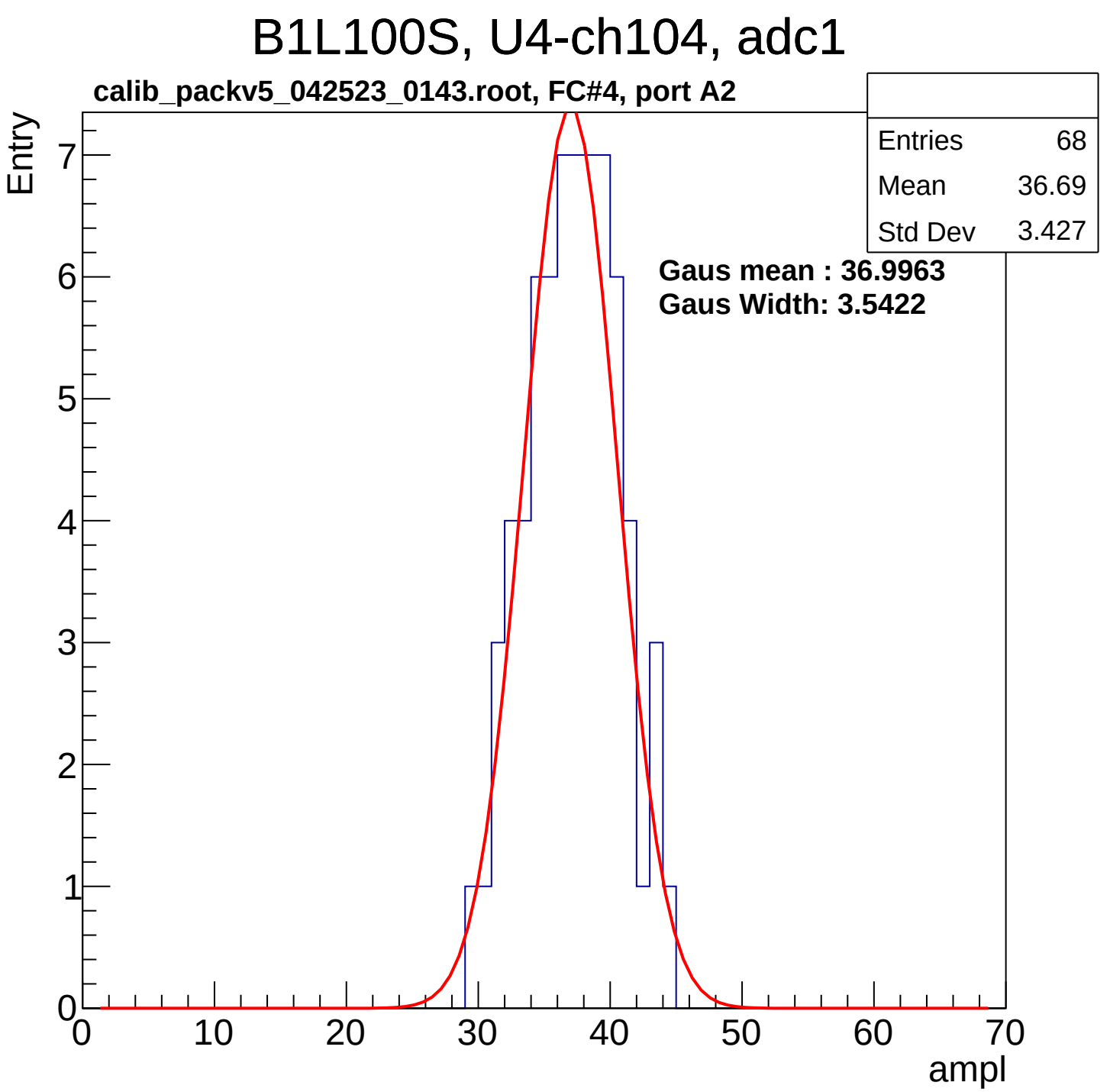

B1L100S, U4-ch103, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 54.59
Std Dev 3.59
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

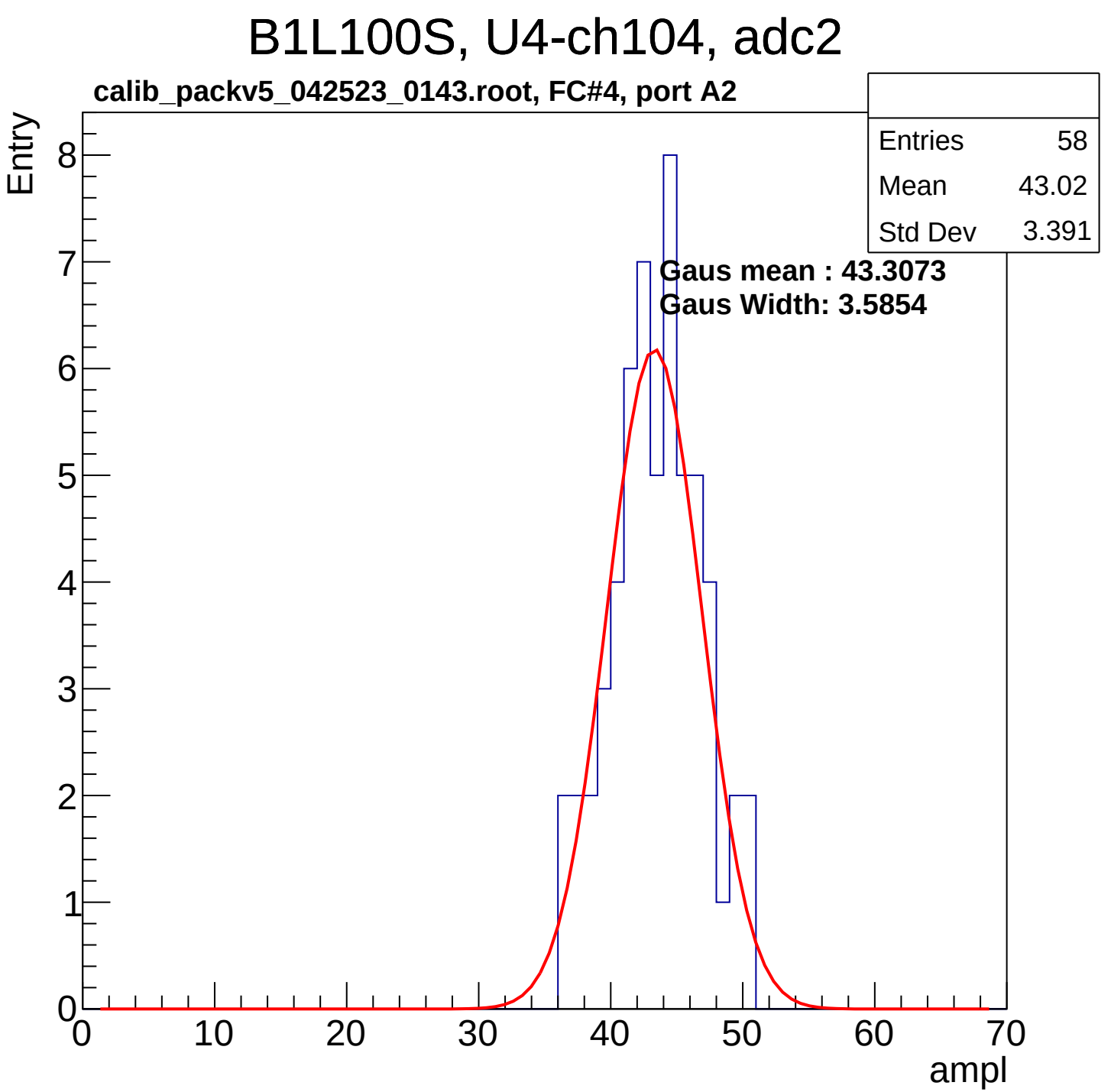

B1L100S, U4-ch103, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 59.54
Std Dev 2.475
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

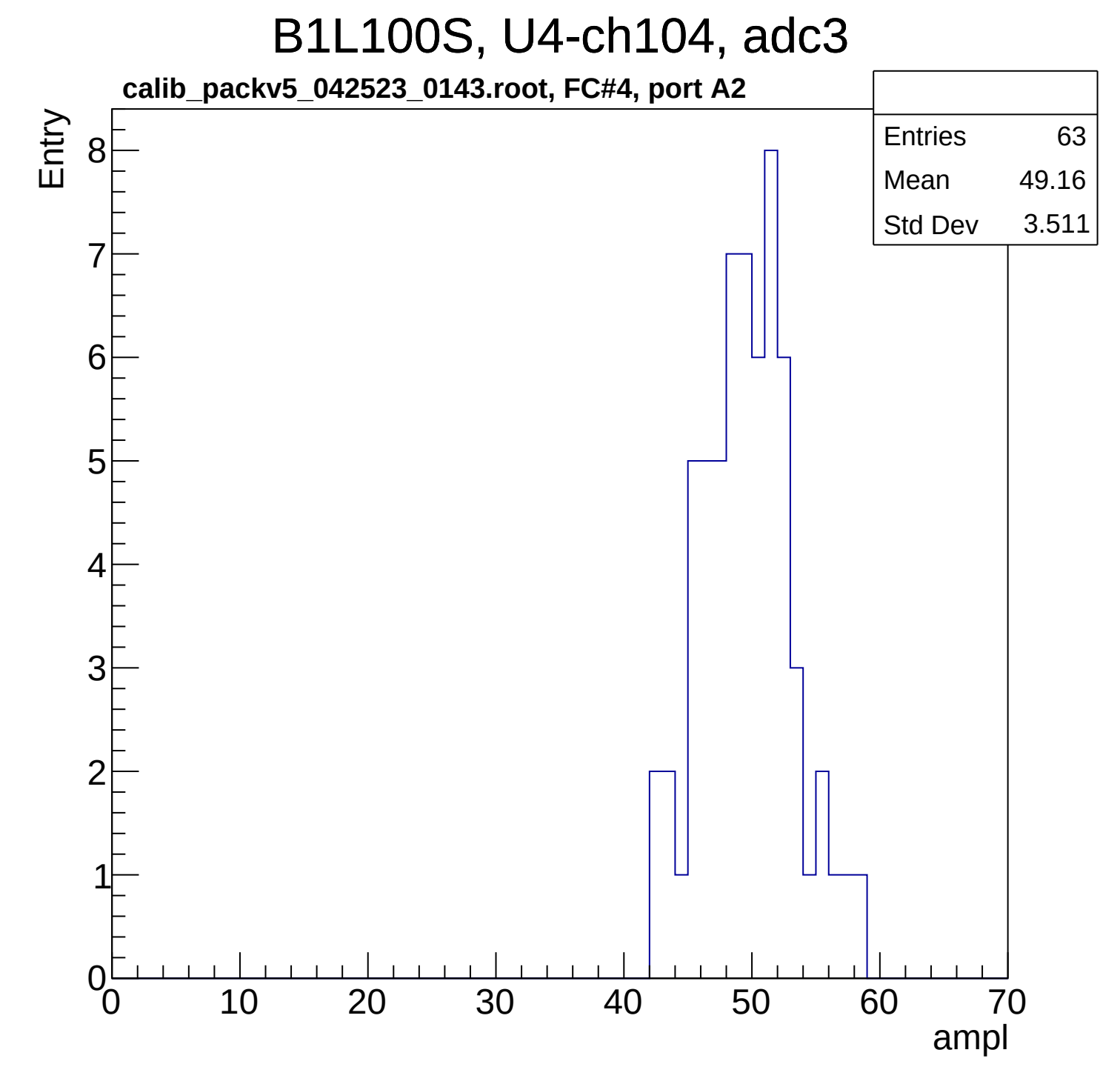

B1L100S, U4-ch103, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 62.17
Std Dev 1.067
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

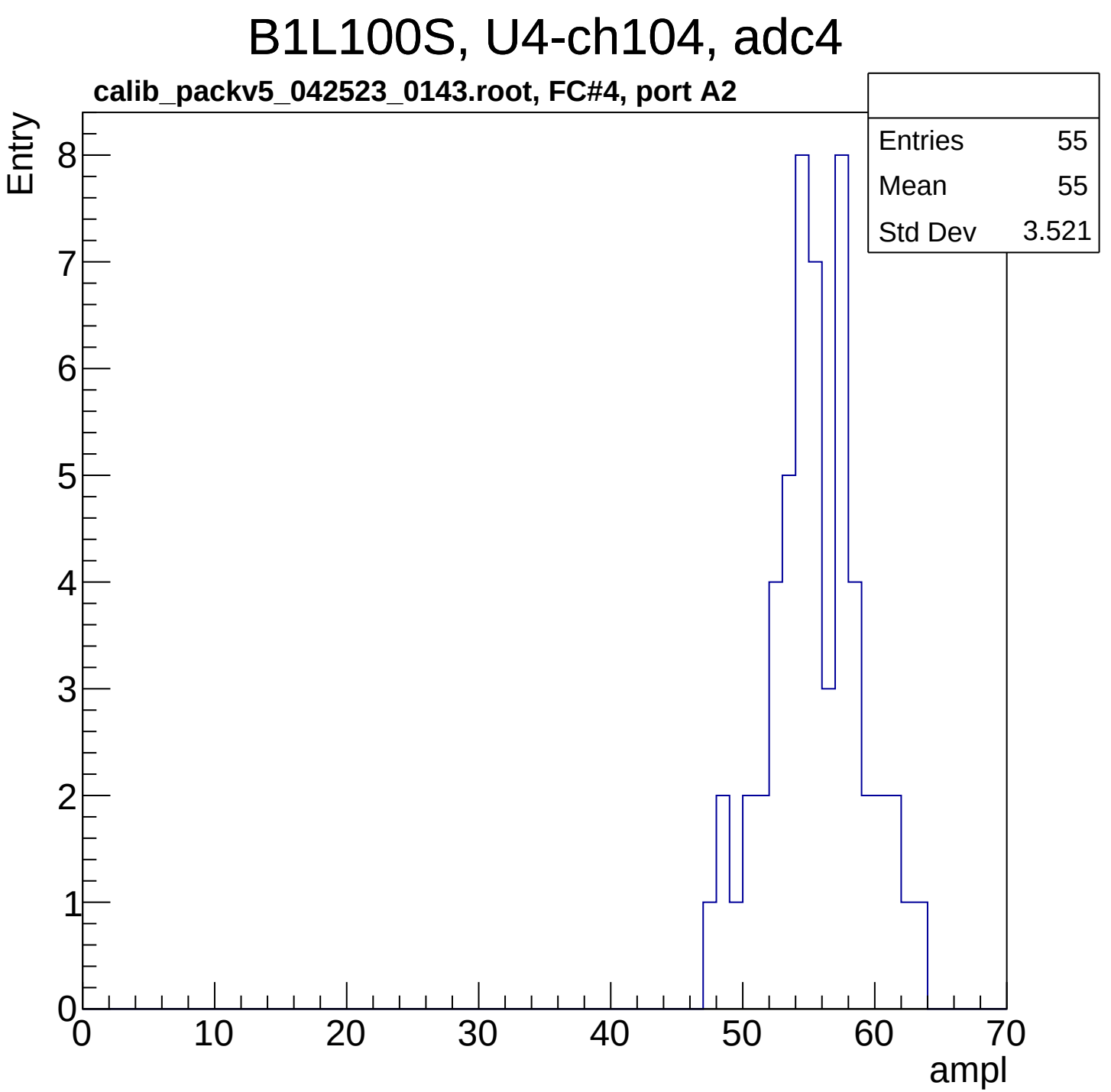

B1L100S, U4-ch103, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 5
Mean 12.6
Std Dev 25.2
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

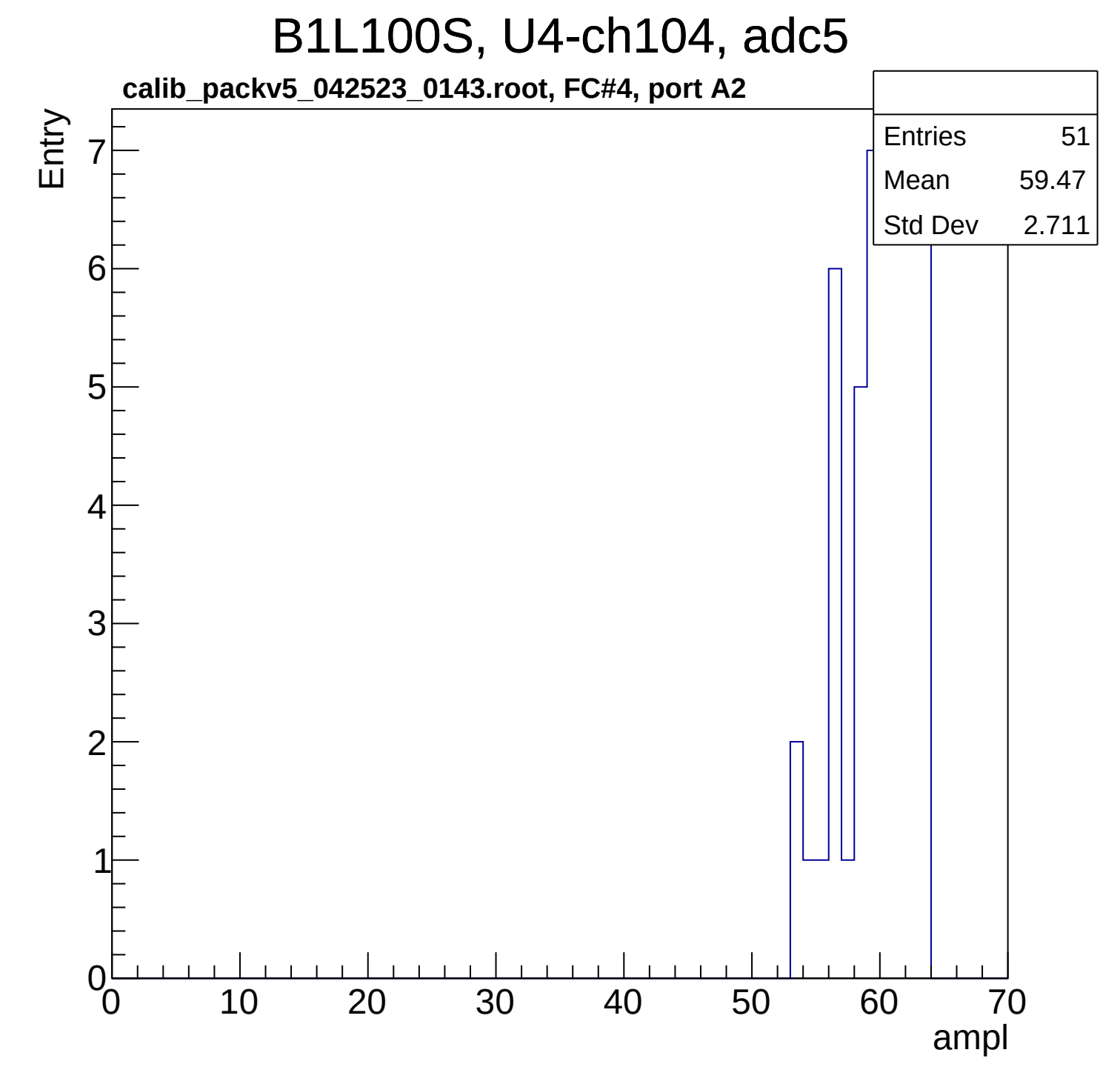

B1L100S, U4-ch104, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 85
Mean 28.16
Std Dev 5.97
Gaus mean : 29.5424
Gaus Width: 4.1331
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

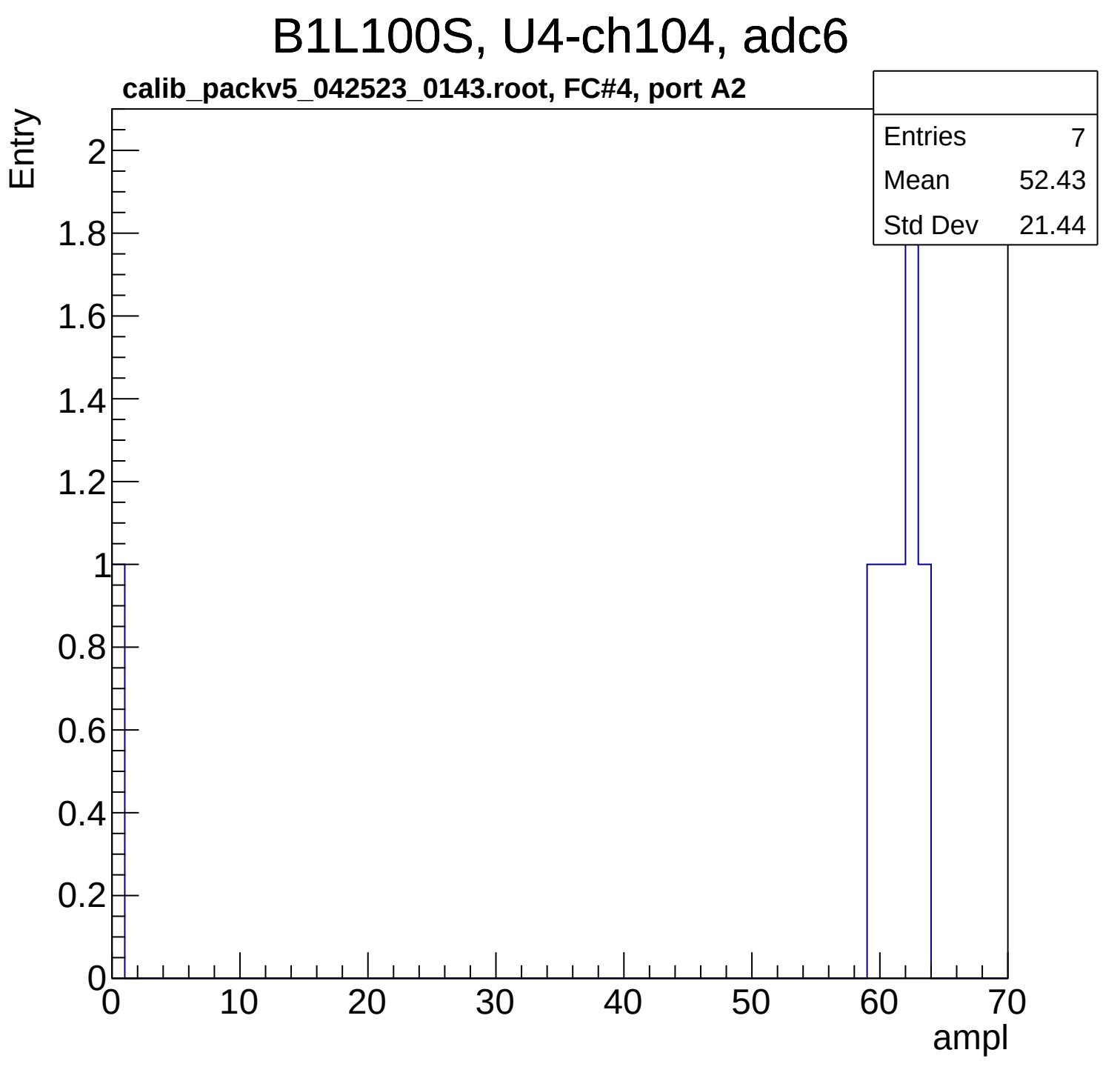

B1L100S, U4-ch104, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 36.69
Std Dev 3.427
Gaus mean : 36.9963
Gaus Width: 3.5422
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

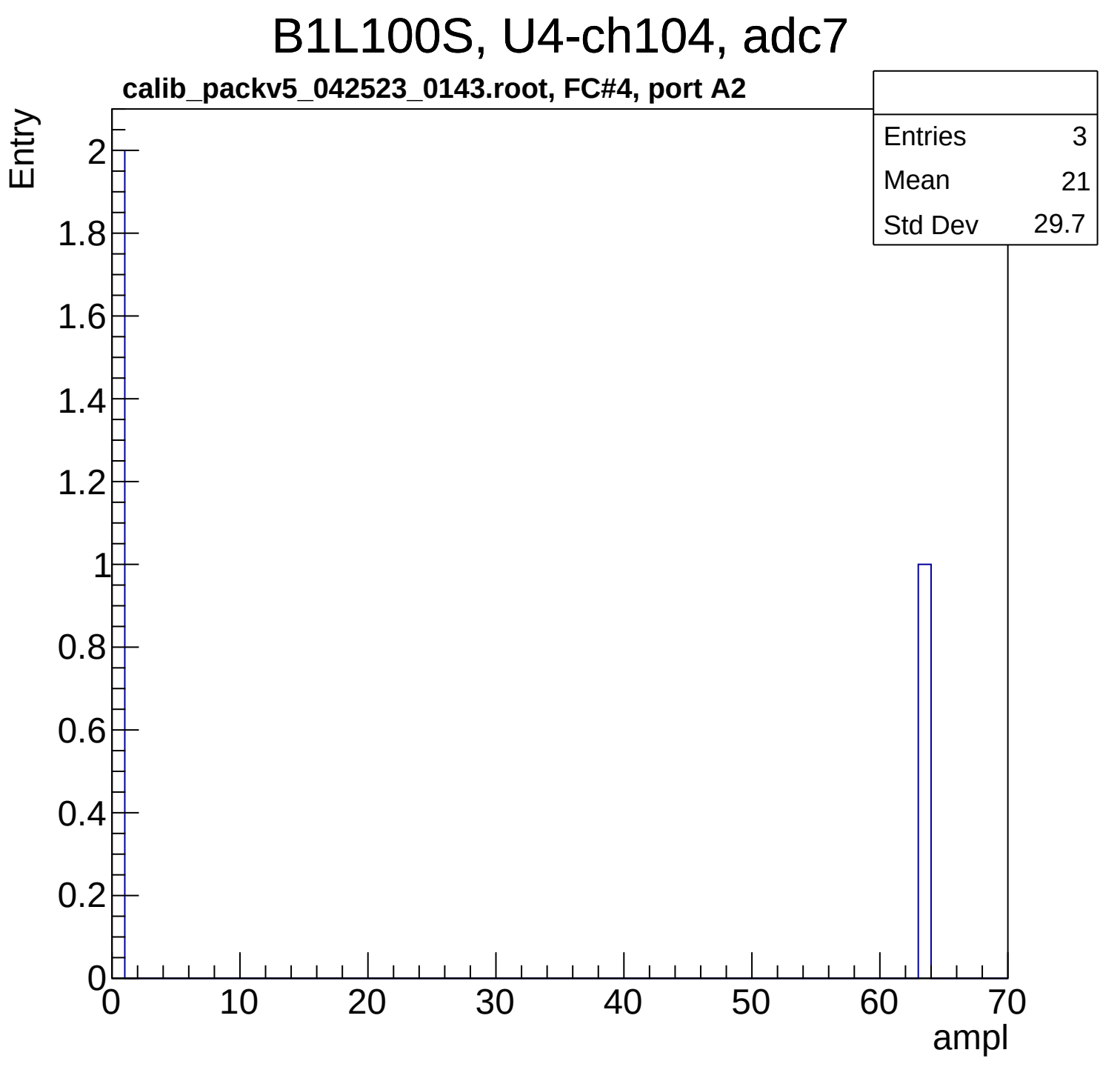

B1L100S, U4-ch104, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 43.02
Std Dev 3.391
Gaus mean : 43.3073
Gaus Width: 3.5854
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

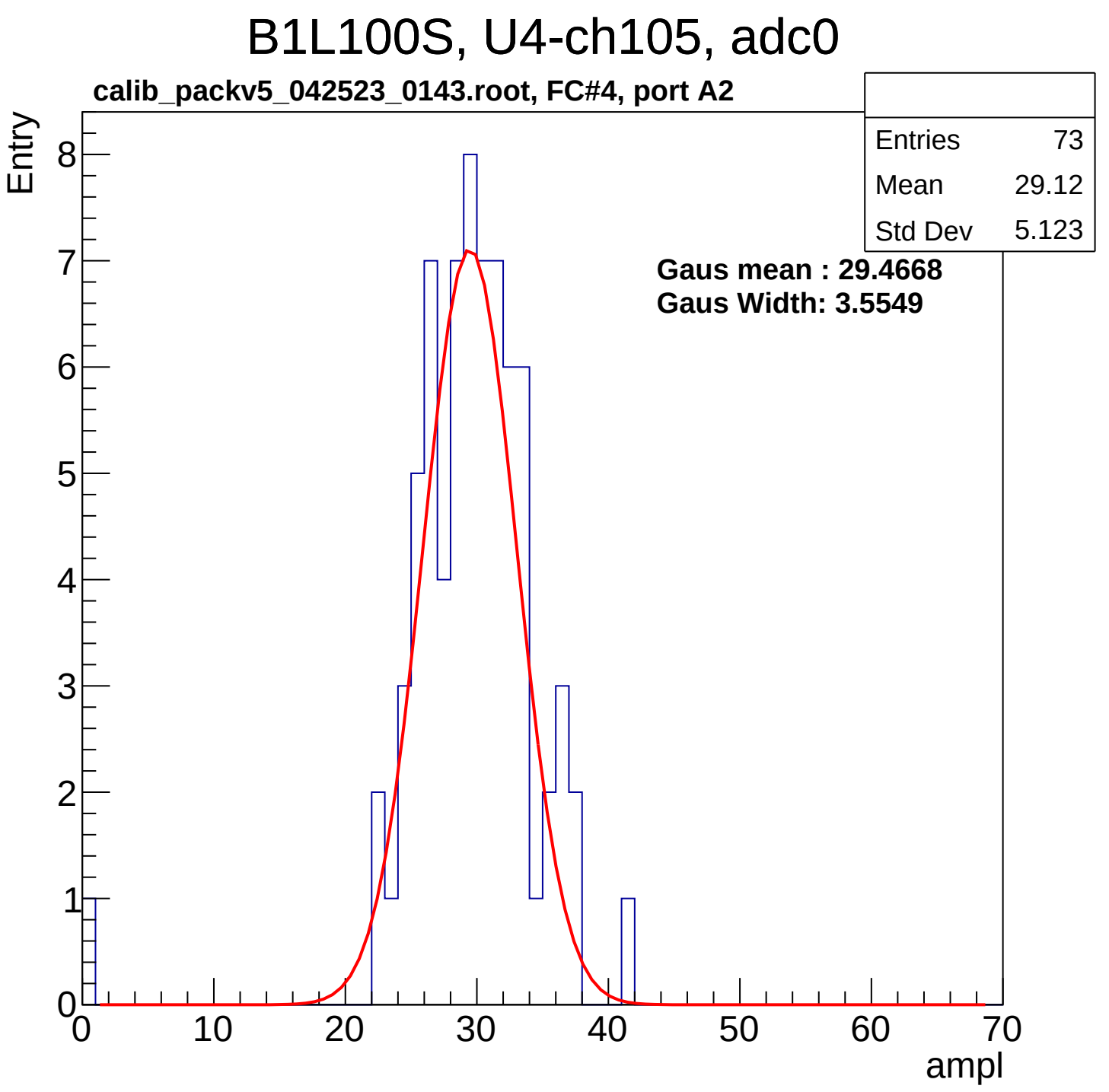

B1L100S, U4-ch104, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 49.16
Std Dev 3.511
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

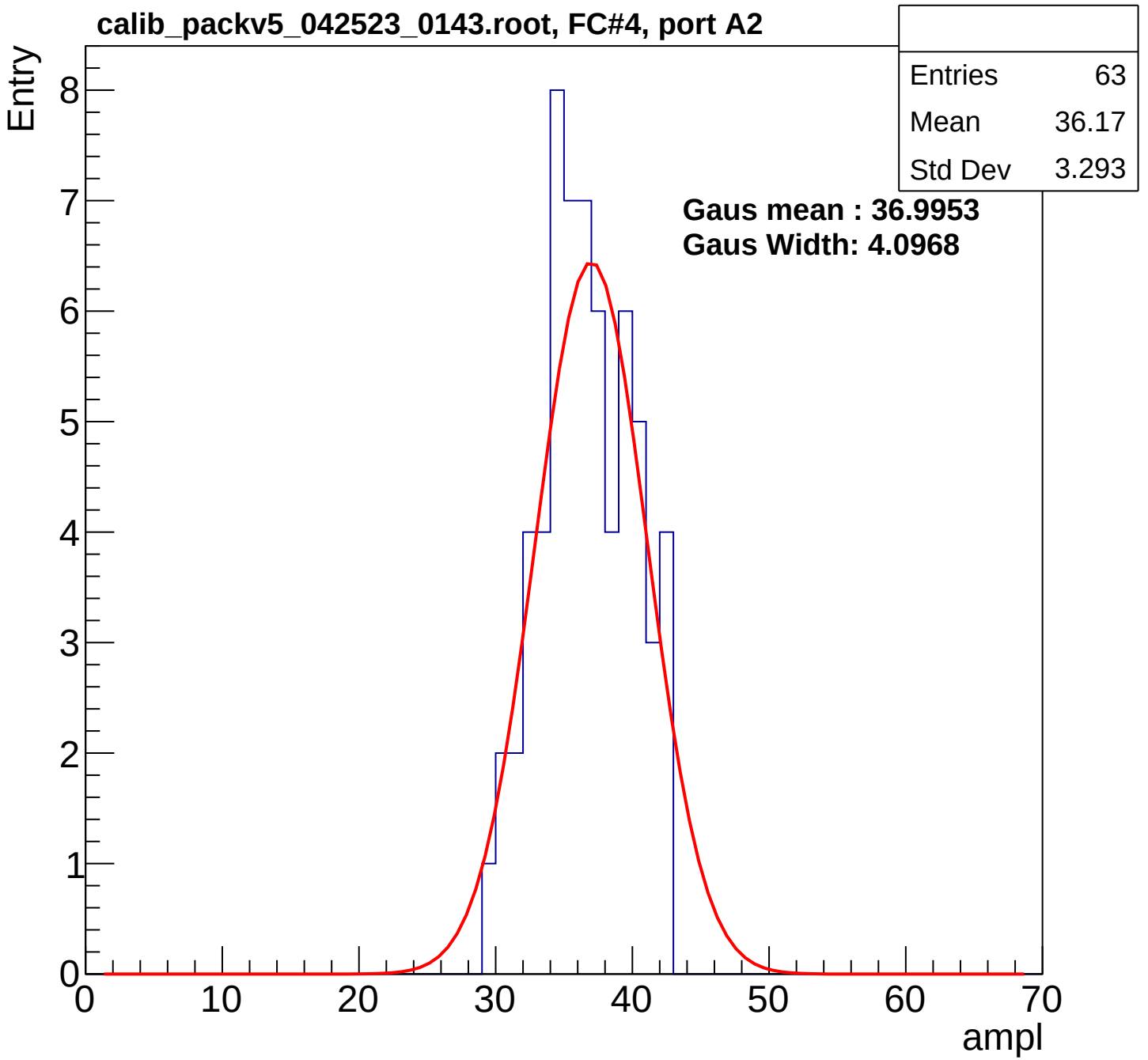

B1L100S, U4-ch104, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 55
Std Dev 3.521
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

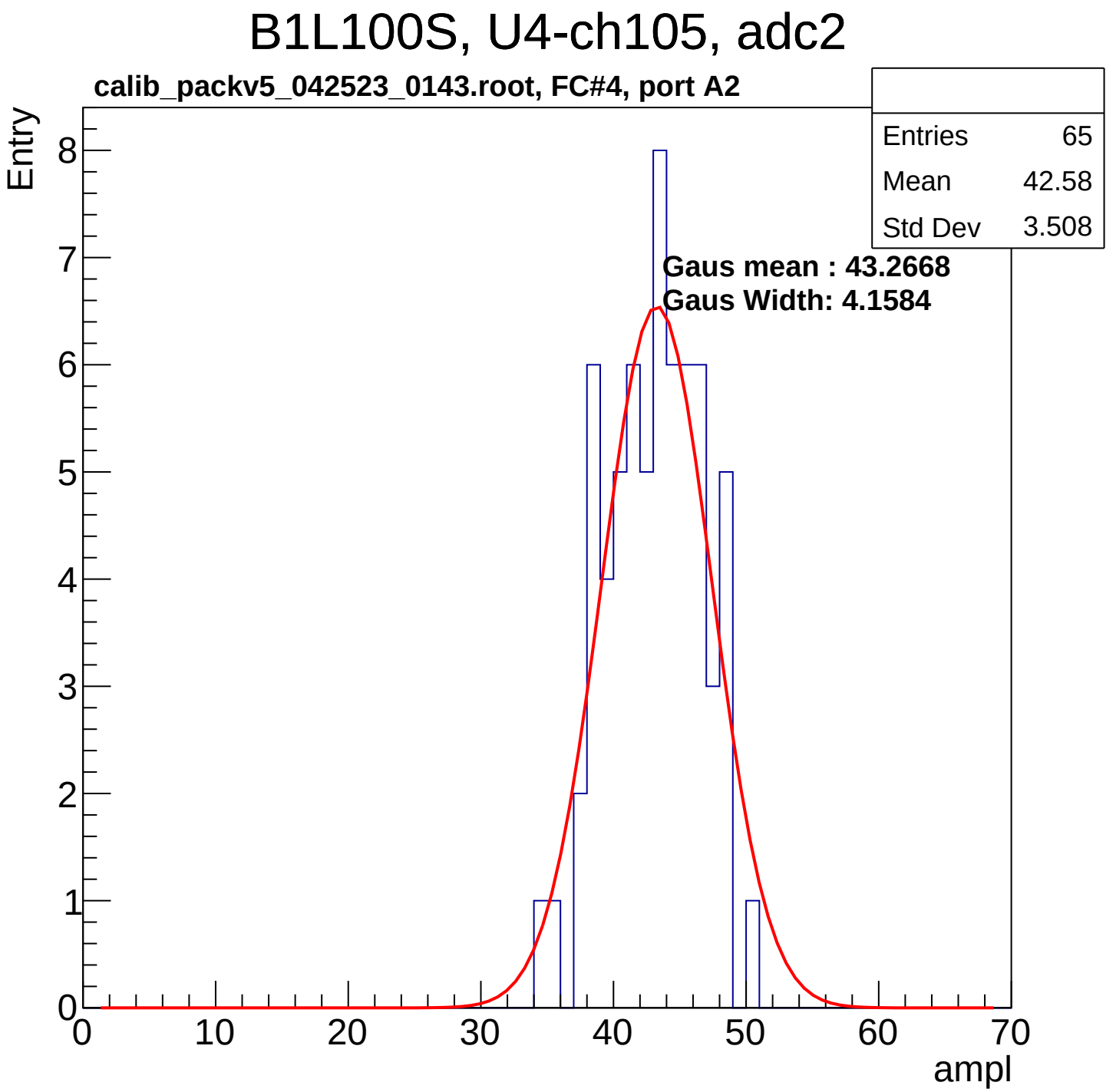

B1L100S, U4-ch104, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 59.47
Std Dev 2.711
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

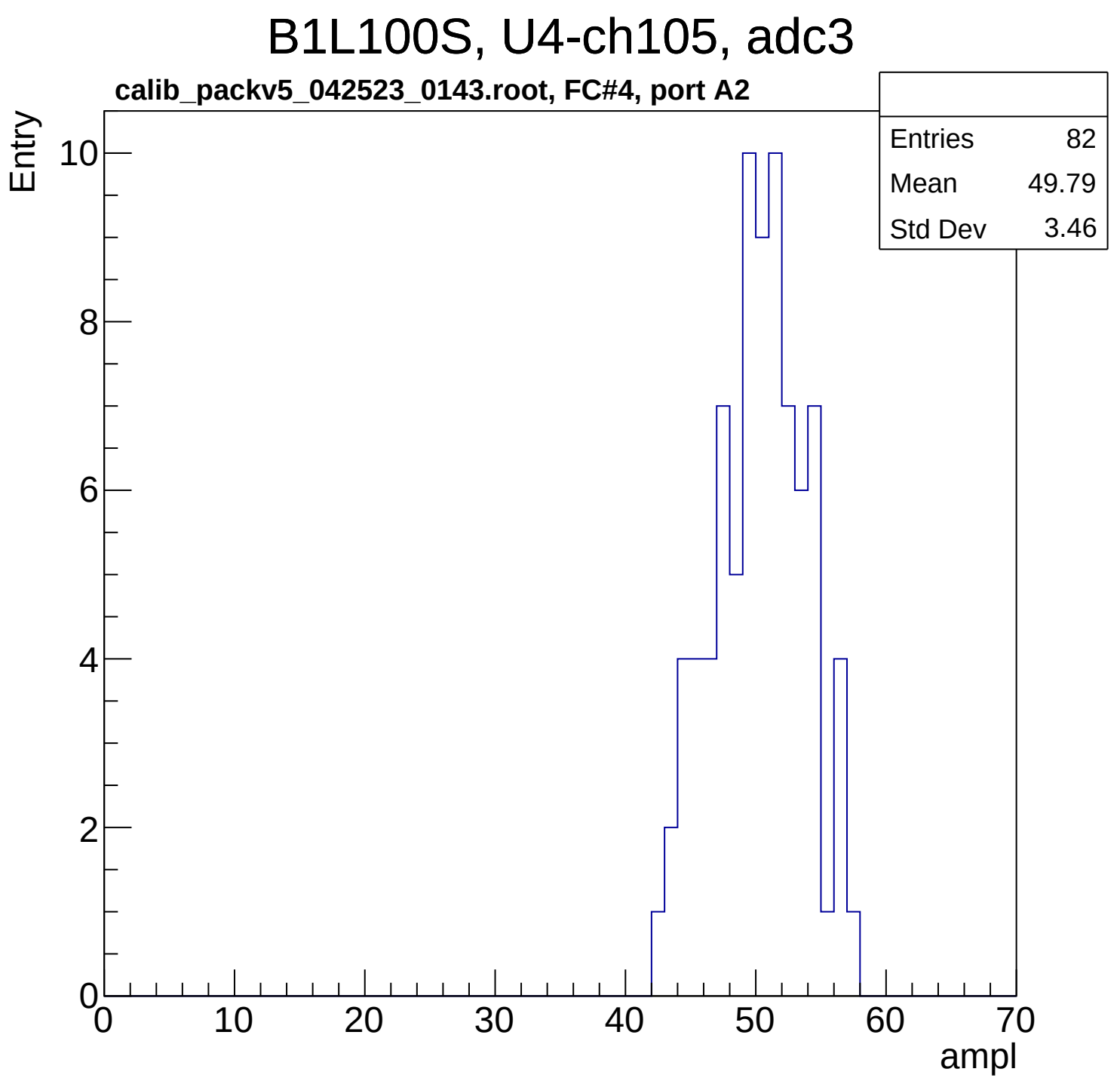

B1L100S, U4-ch104, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 52.43
Std Dev 21.44
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

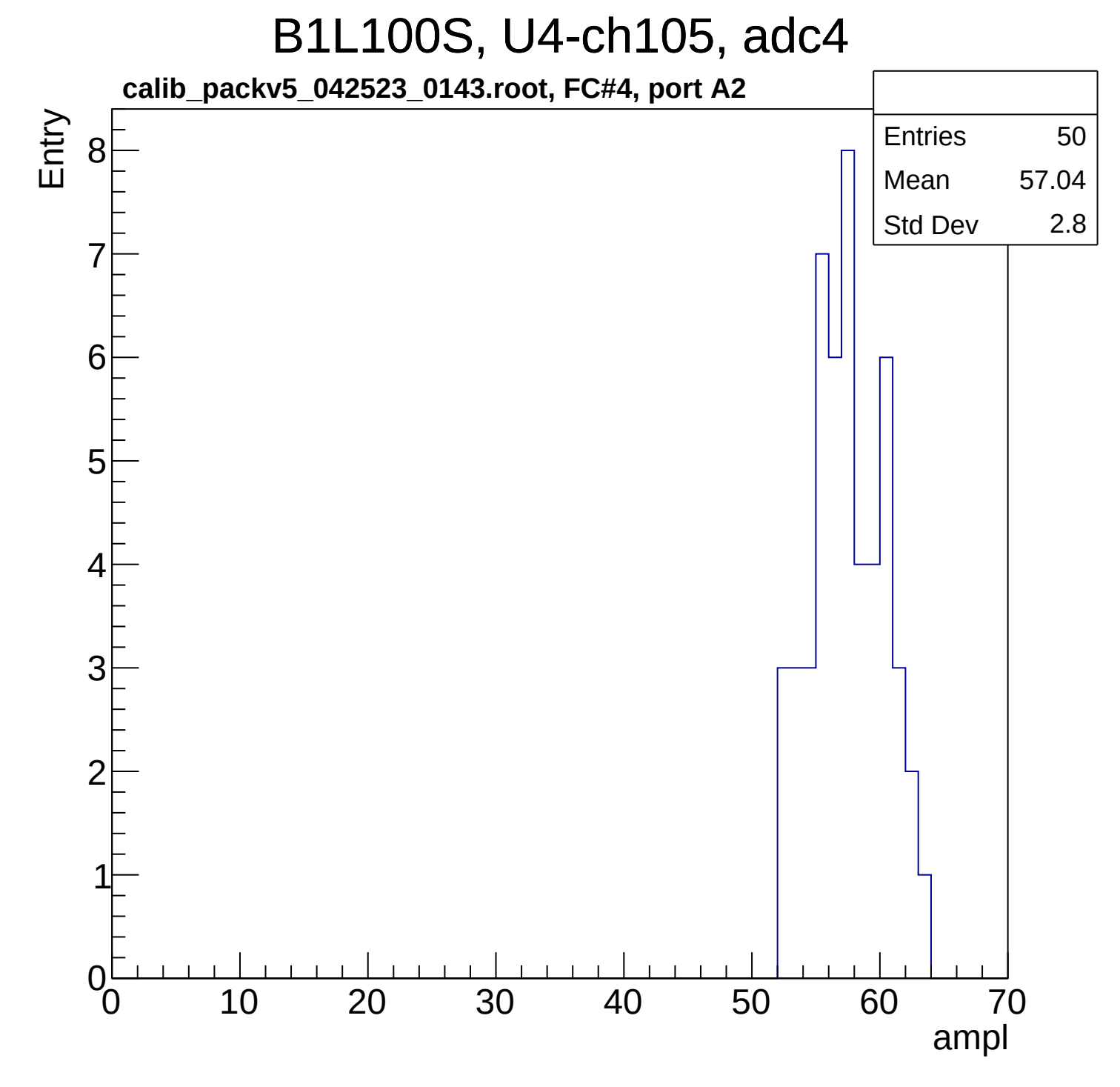

B1L100S, U4-ch104, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 21
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

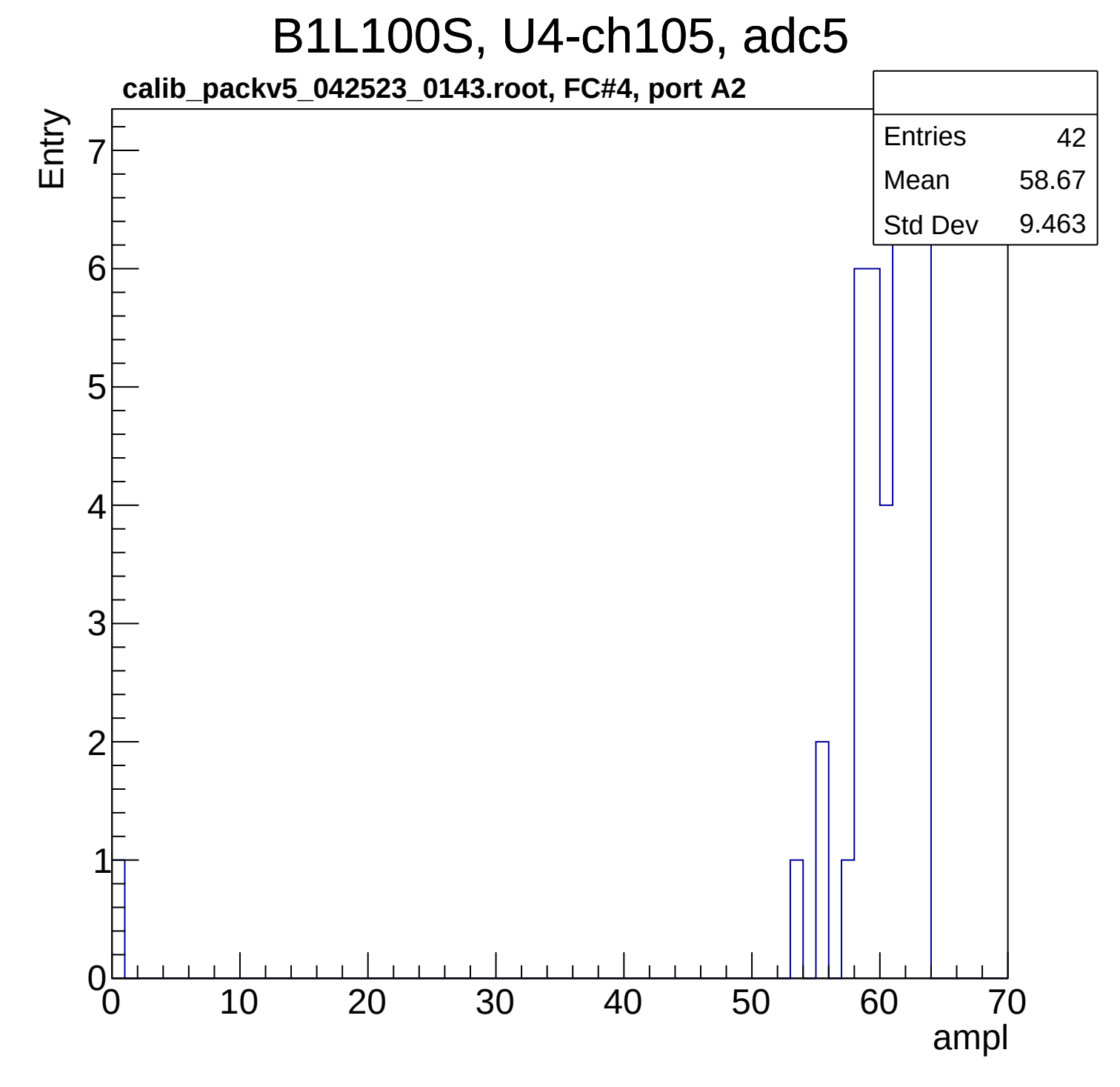

B1L100S, U4-ch105, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 29.12
Std Dev 5.123
Gaus mean : 29.4668
Gaus Width: 3.5549
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

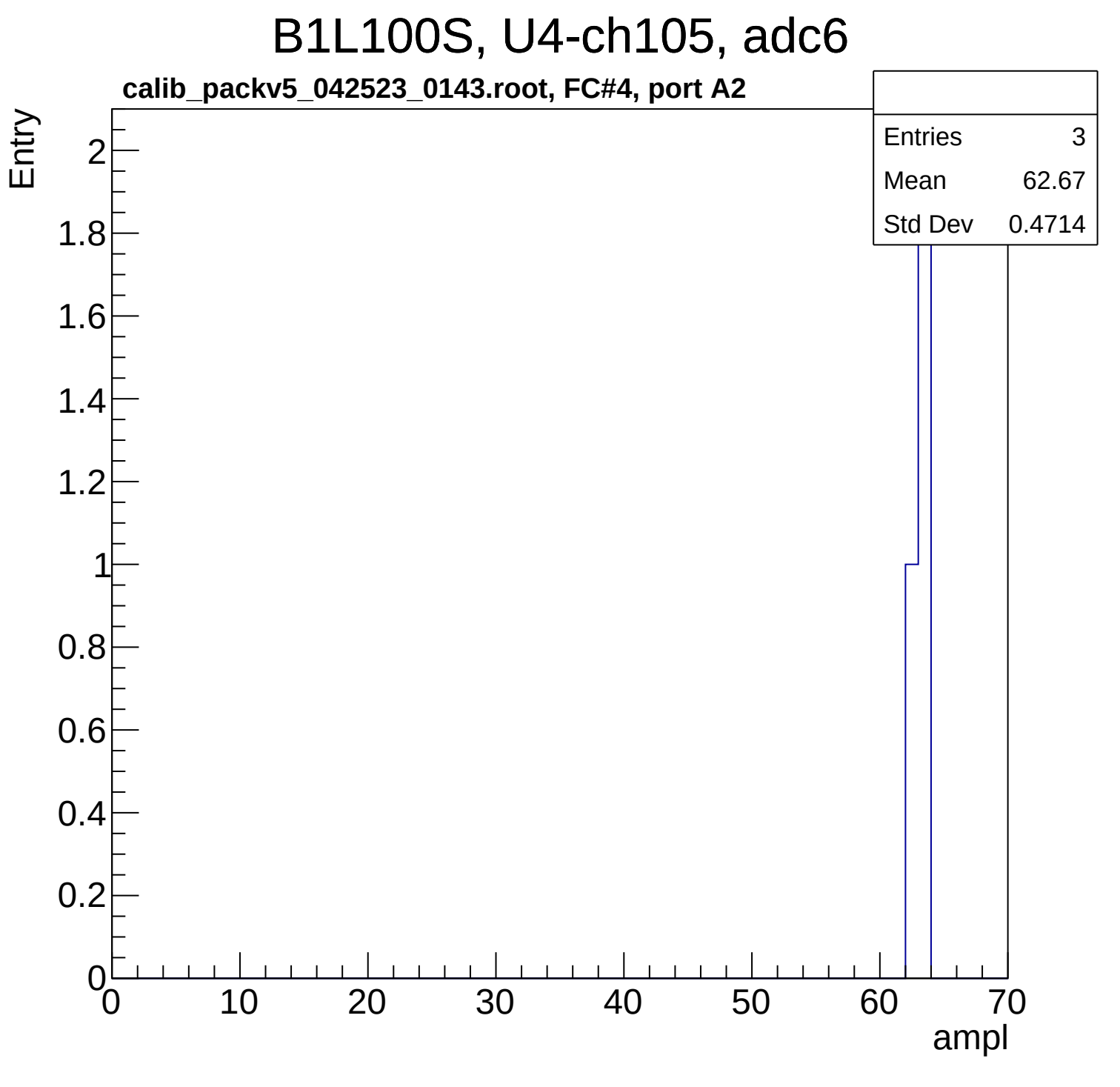

B1L100S, U4-ch105, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 36.17
Std Dev 3.293
Gaus mean : 36.9953
Gaus Width: 4.0968
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

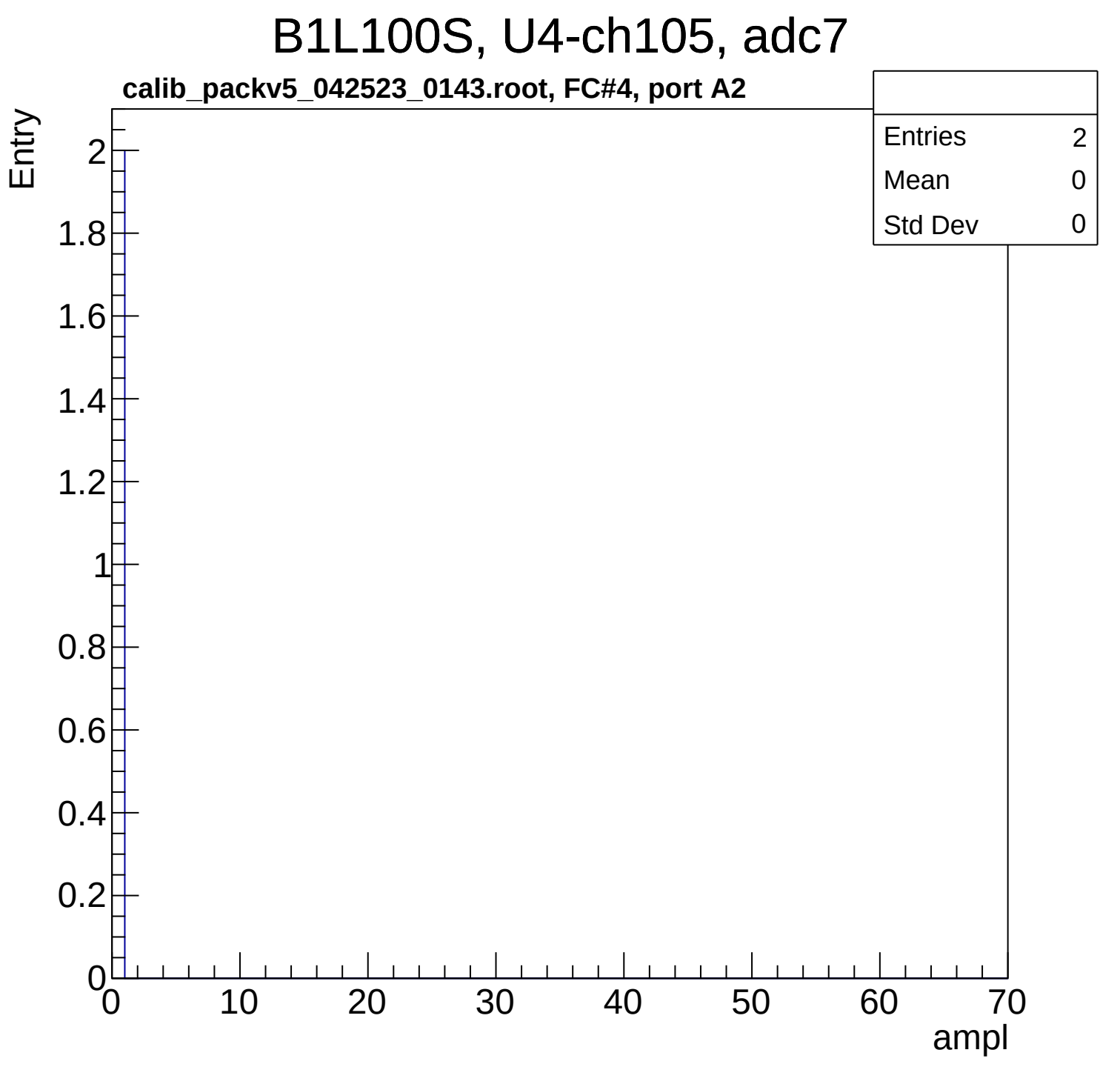

B1L100S, U4-ch105, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 42.58
Std Dev 3.508
Gaus mean : 43.2668
Gaus Width: 4.1584
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

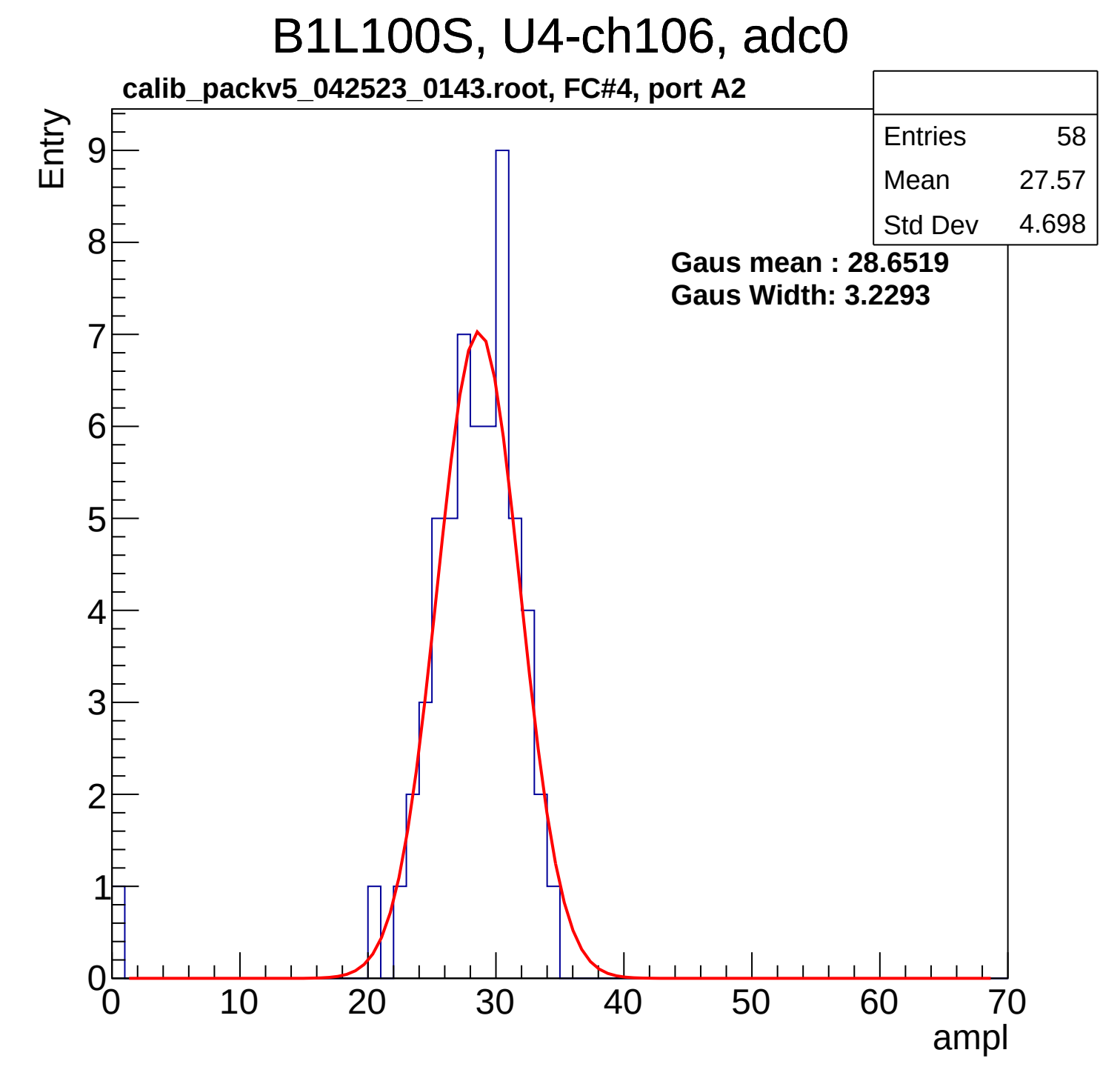

B1L100S, U4-ch105, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 49.79
Std Dev 3.46
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

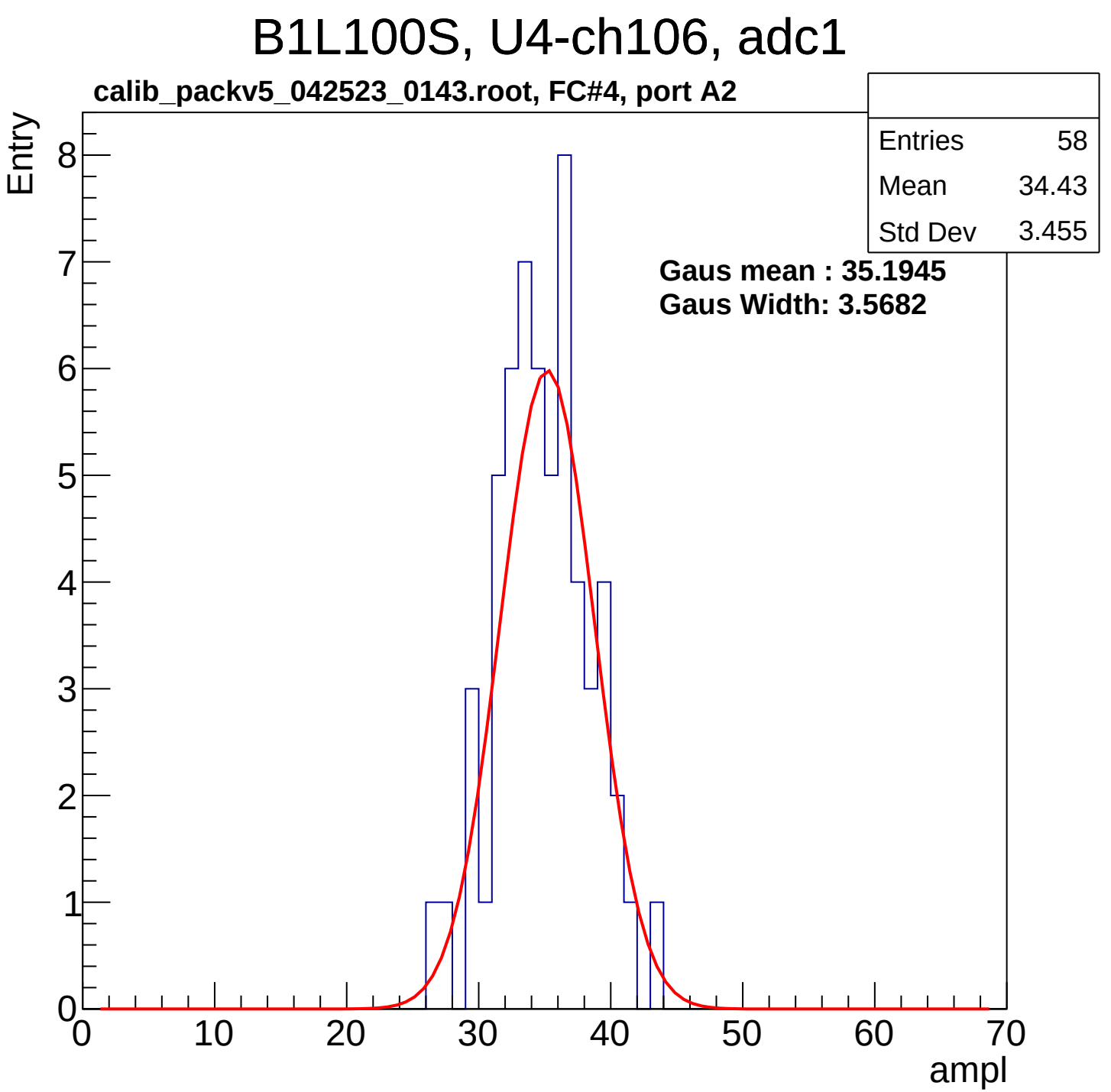

B1L100S, U4-ch105, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 57.04
Std Dev 2.8
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

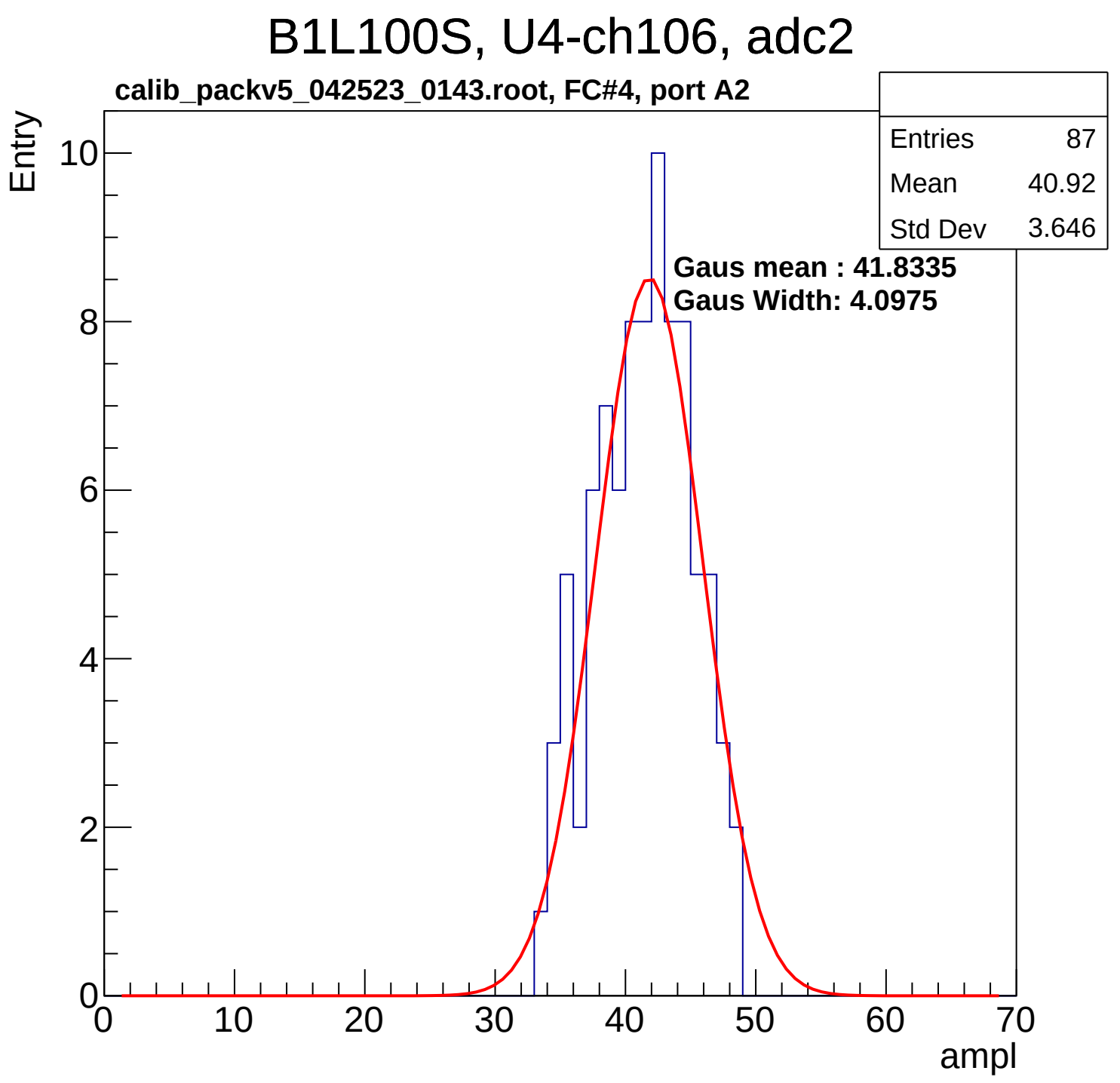

B1L100S, U4-ch105, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 42
Mean 58.67
Std Dev 9.463
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

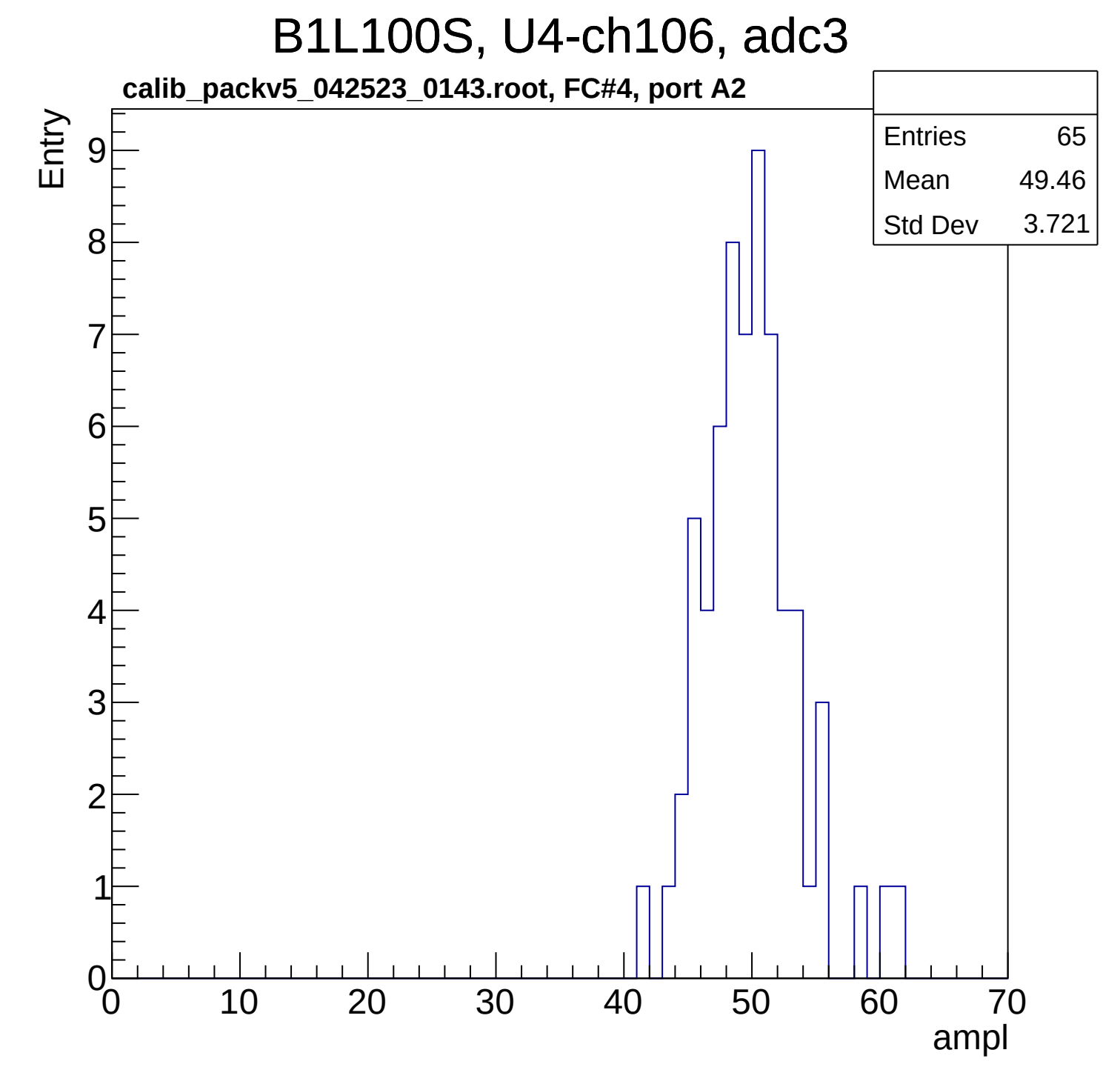

B1L100S, U4-ch105, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

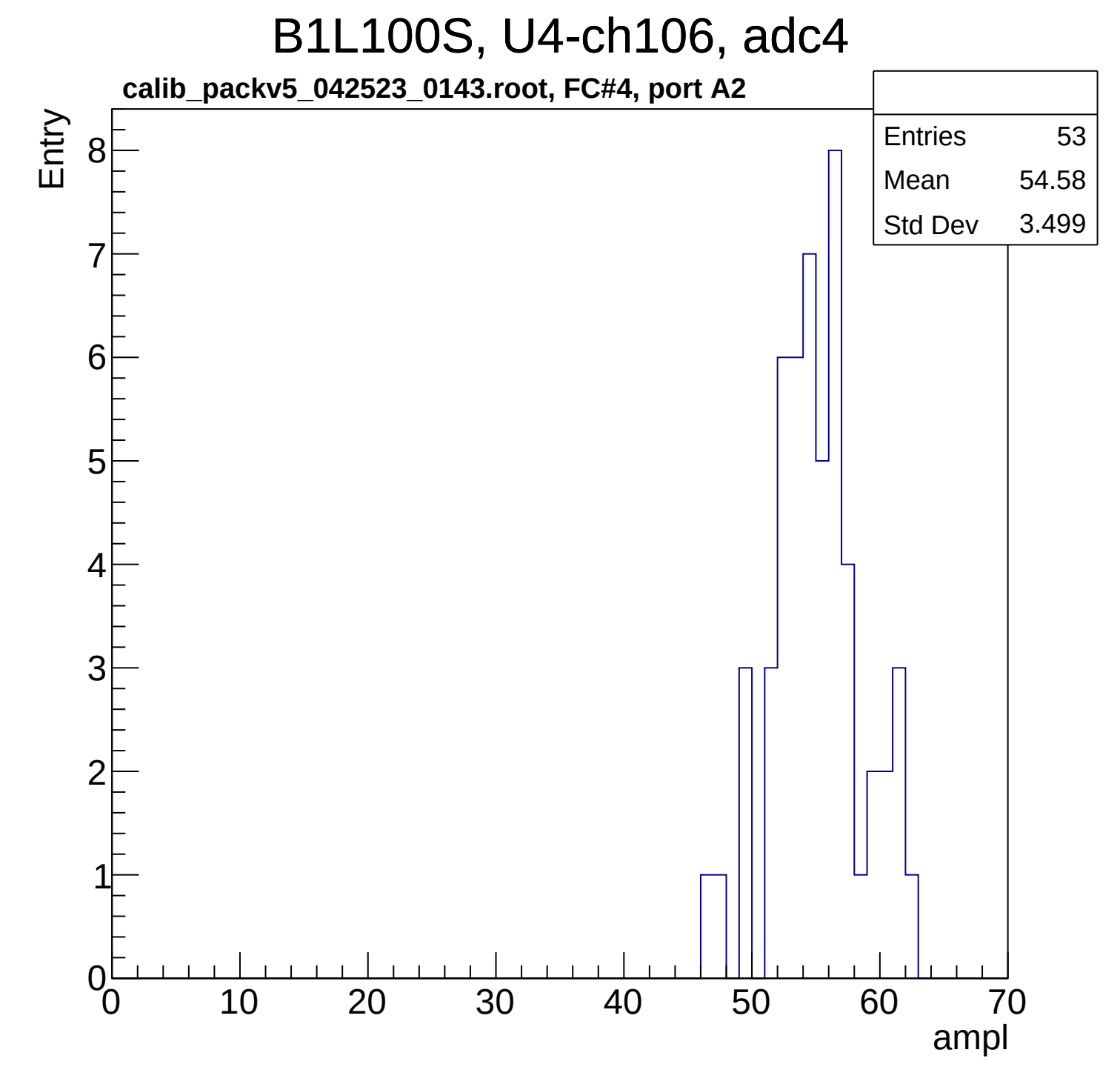

B1L100S, U4-ch105, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

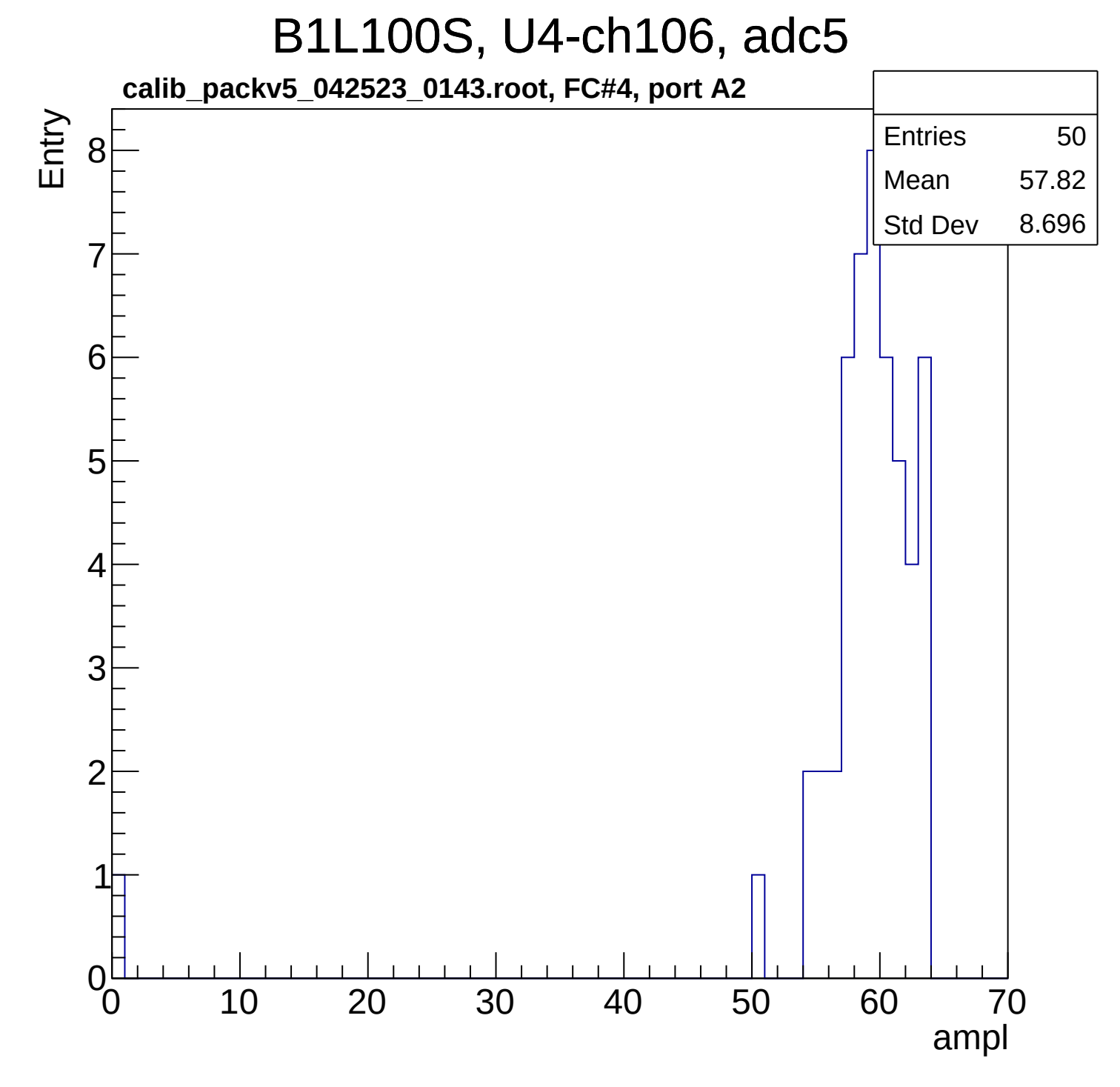

B1L100S, U4-ch106, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 27.57
Std Dev 4.698
Gaus mean : 28.6519
Gaus Width: 3.2293
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

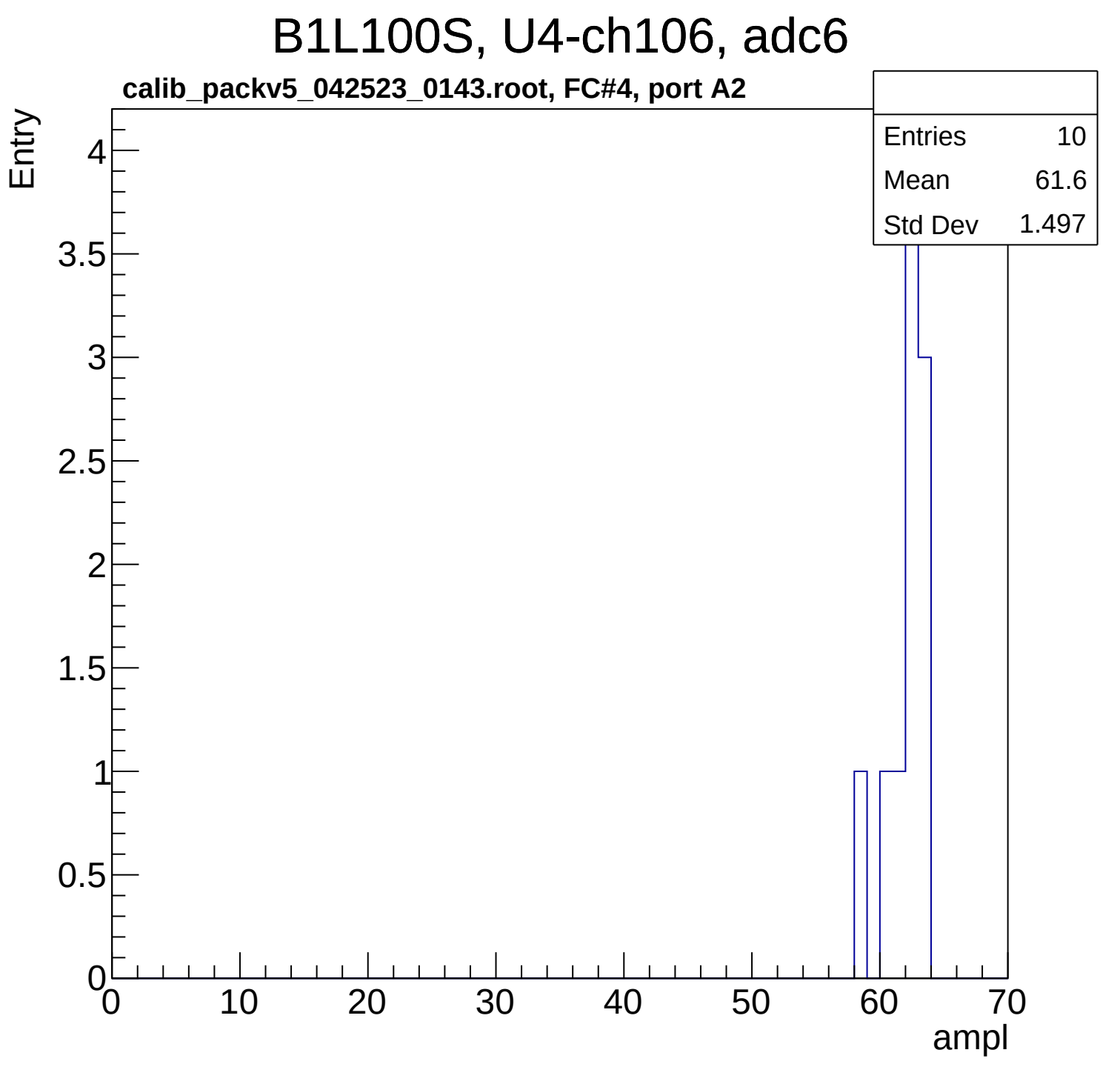

B1L100S, U4-ch106, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 34.43
Std Dev 3.455
Gaus mean : 35.1945
Gaus Width: 3.5682
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

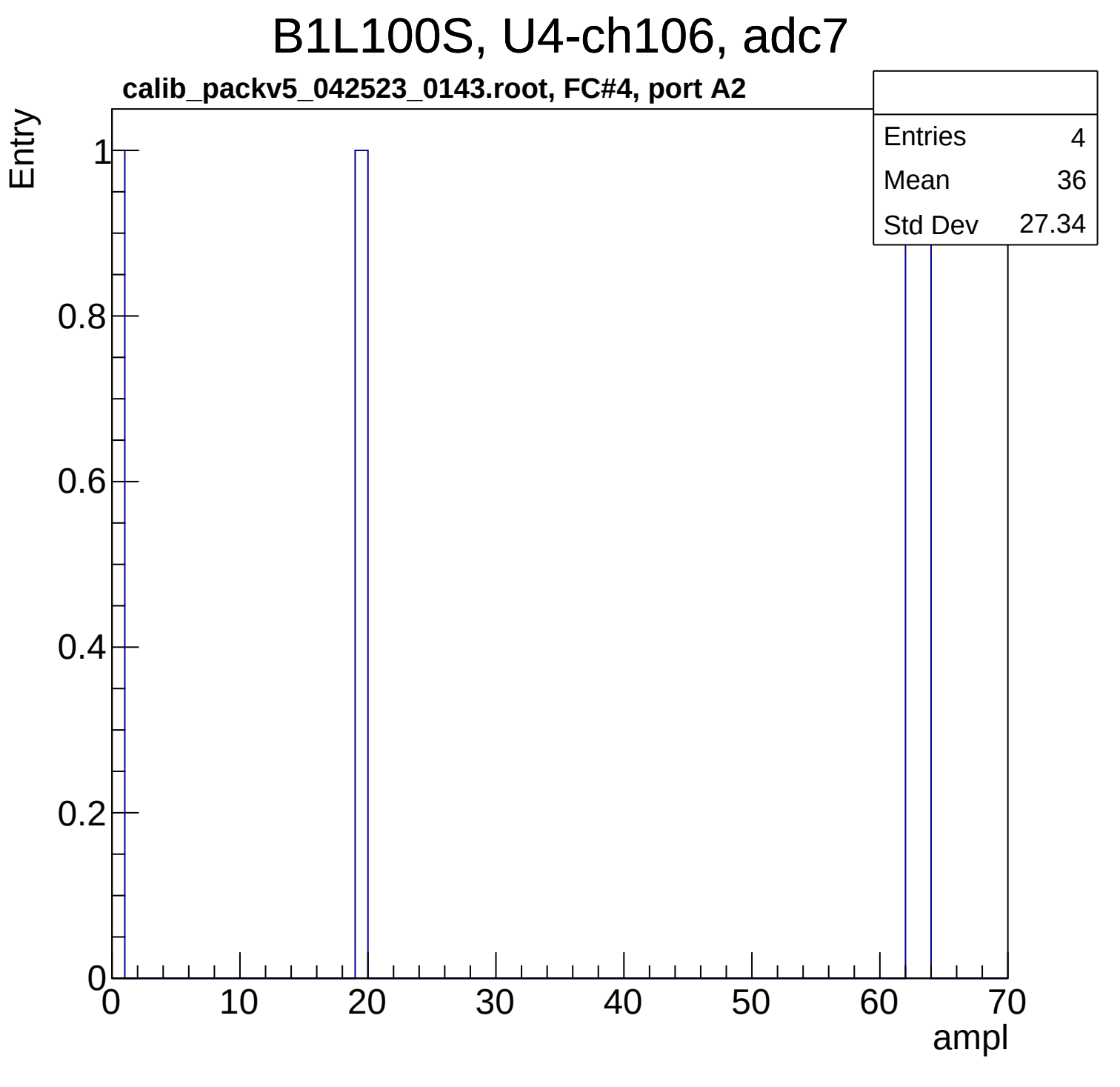

B1L100S, U4-ch106, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 87
Mean 40.92
Std Dev 3.646
Gaus mean : 41.8335
Gaus Width: 4.0975
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

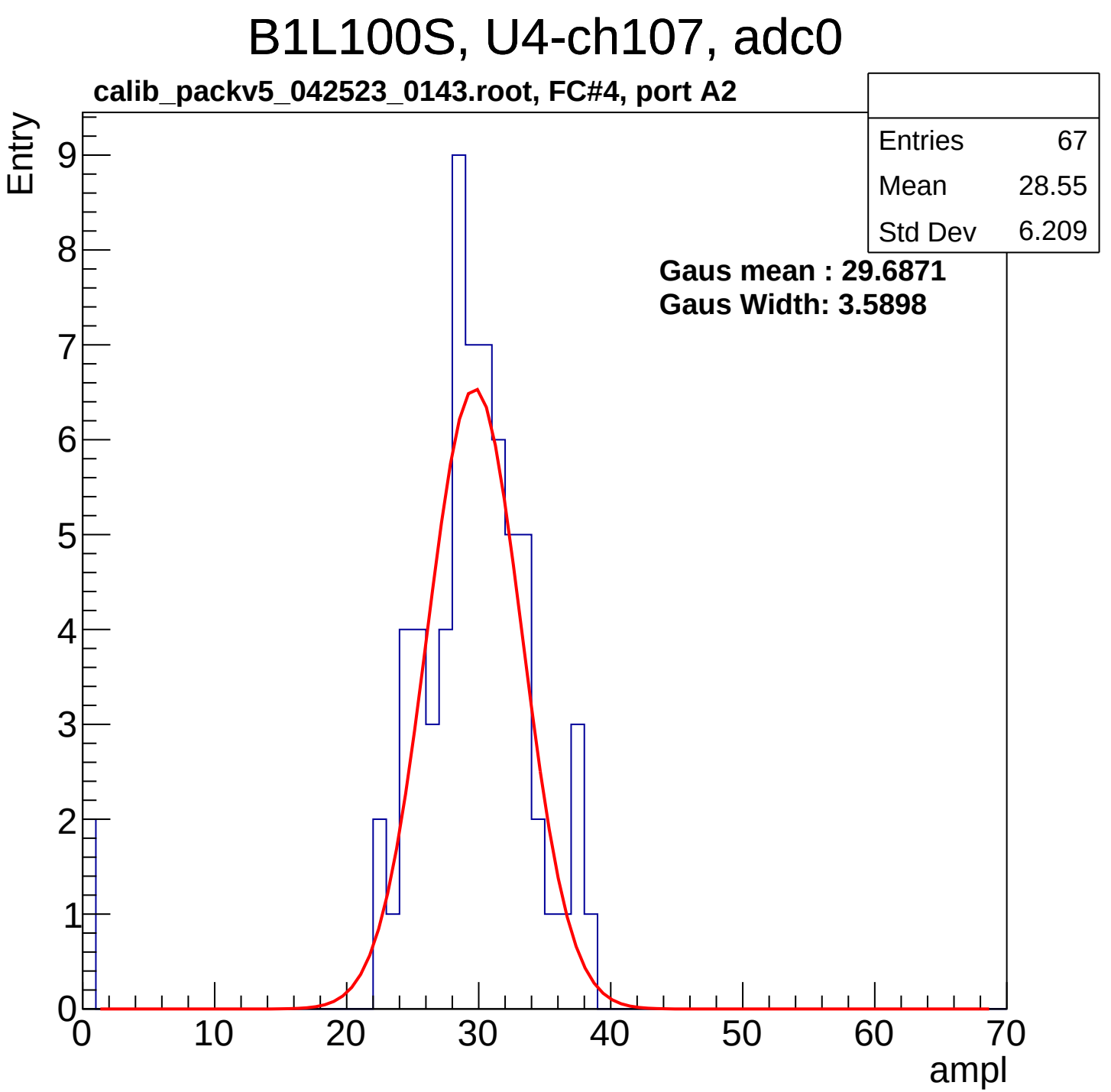

B1L100S, U4-ch106, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 49.46
Std Dev 3.721
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

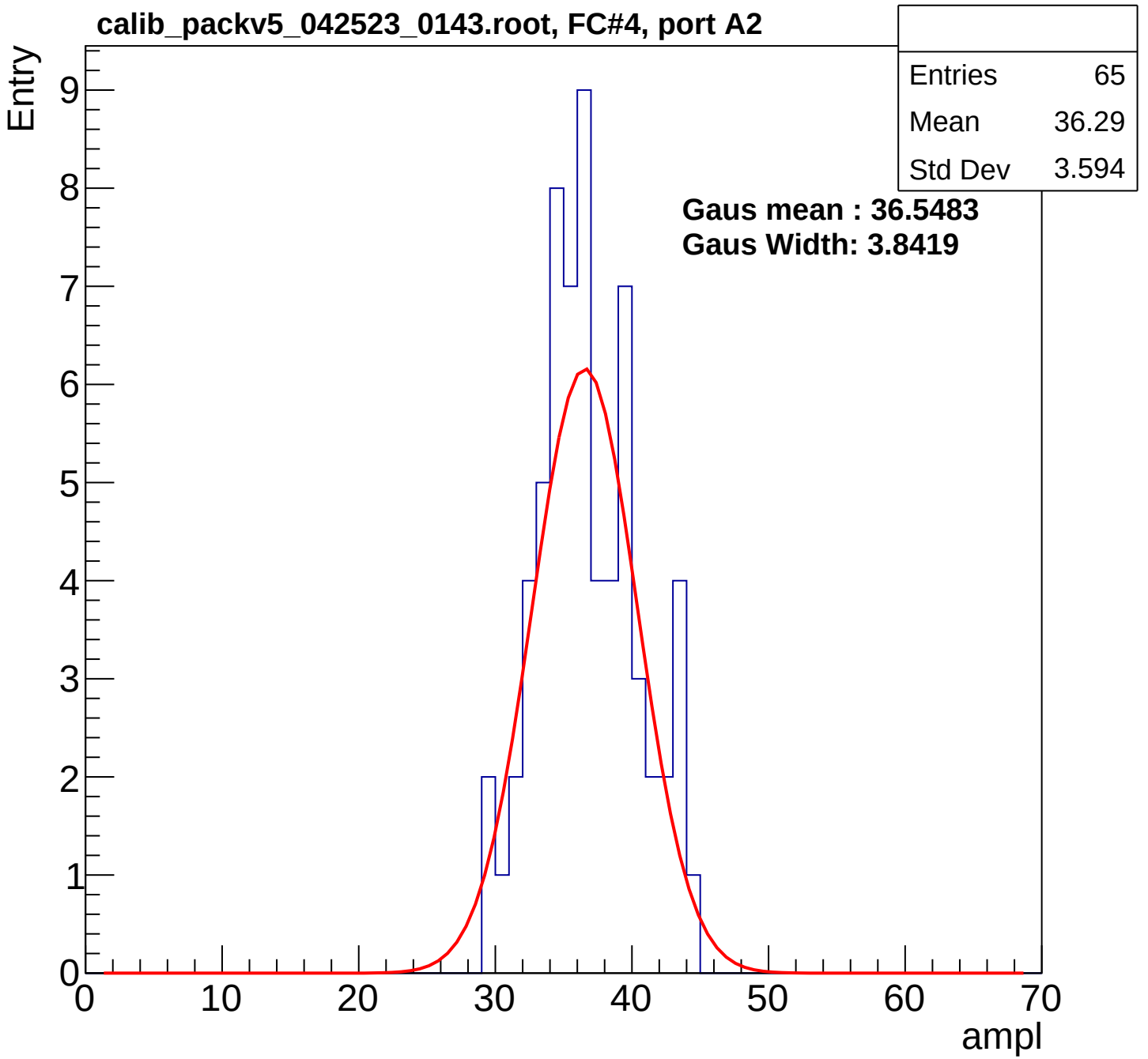

B1L100S, U4-ch106, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 54.58
Std Dev 3.499
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

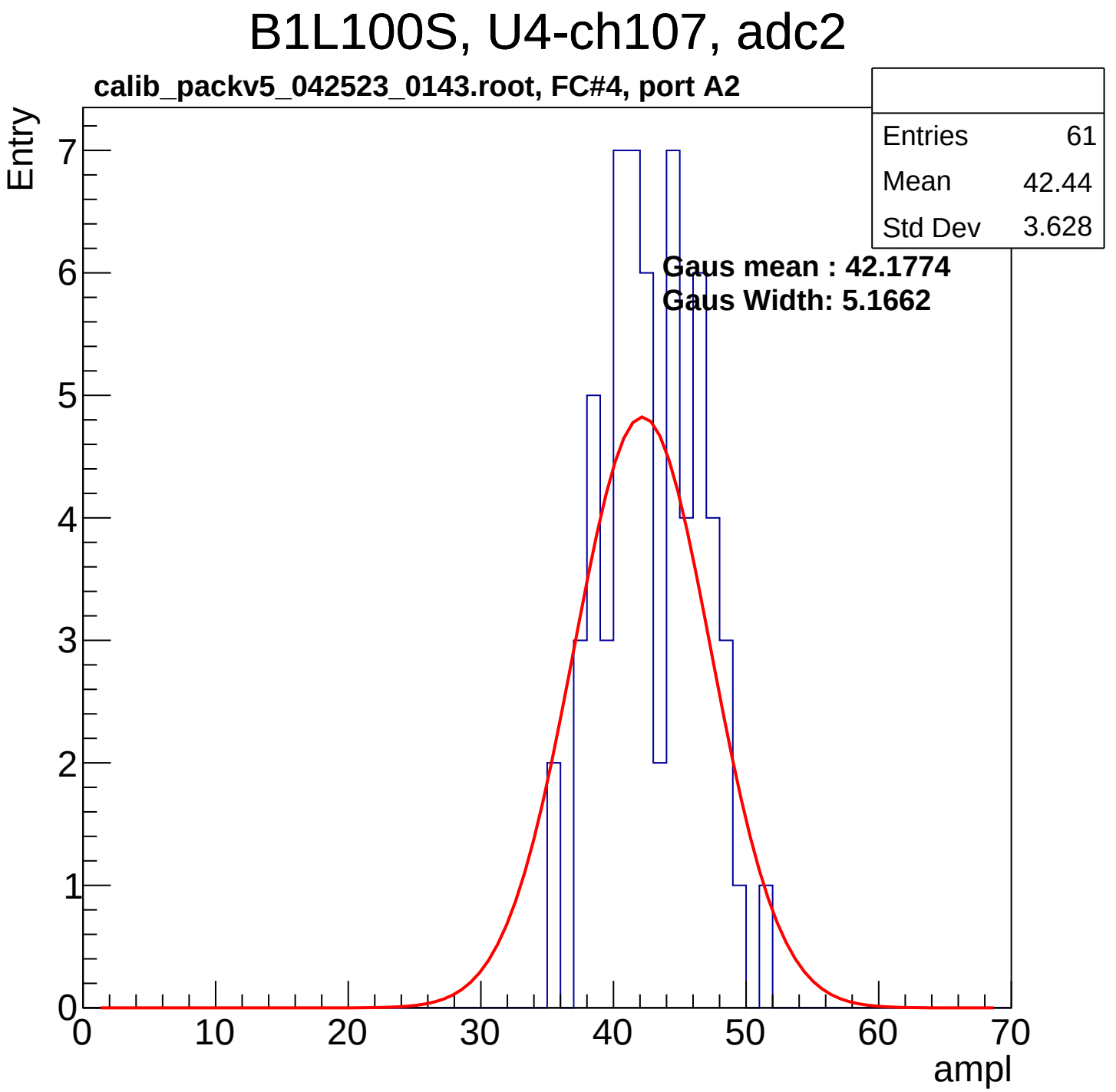

B1L100S, U4-ch106, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 57.82
Std Dev 8.696
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

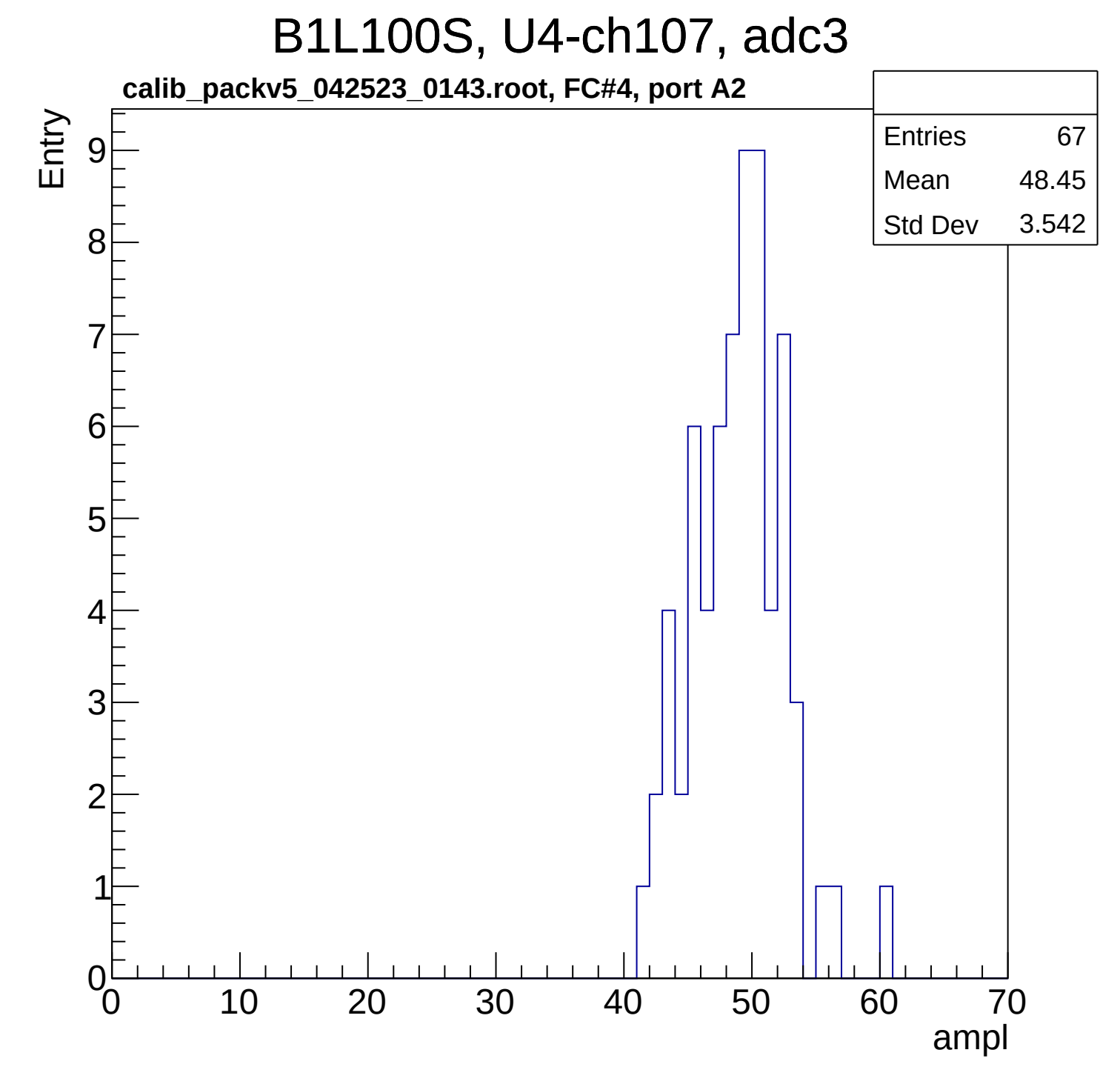

B1L100S, U4-ch106, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 61.6
Std Dev 1.497
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

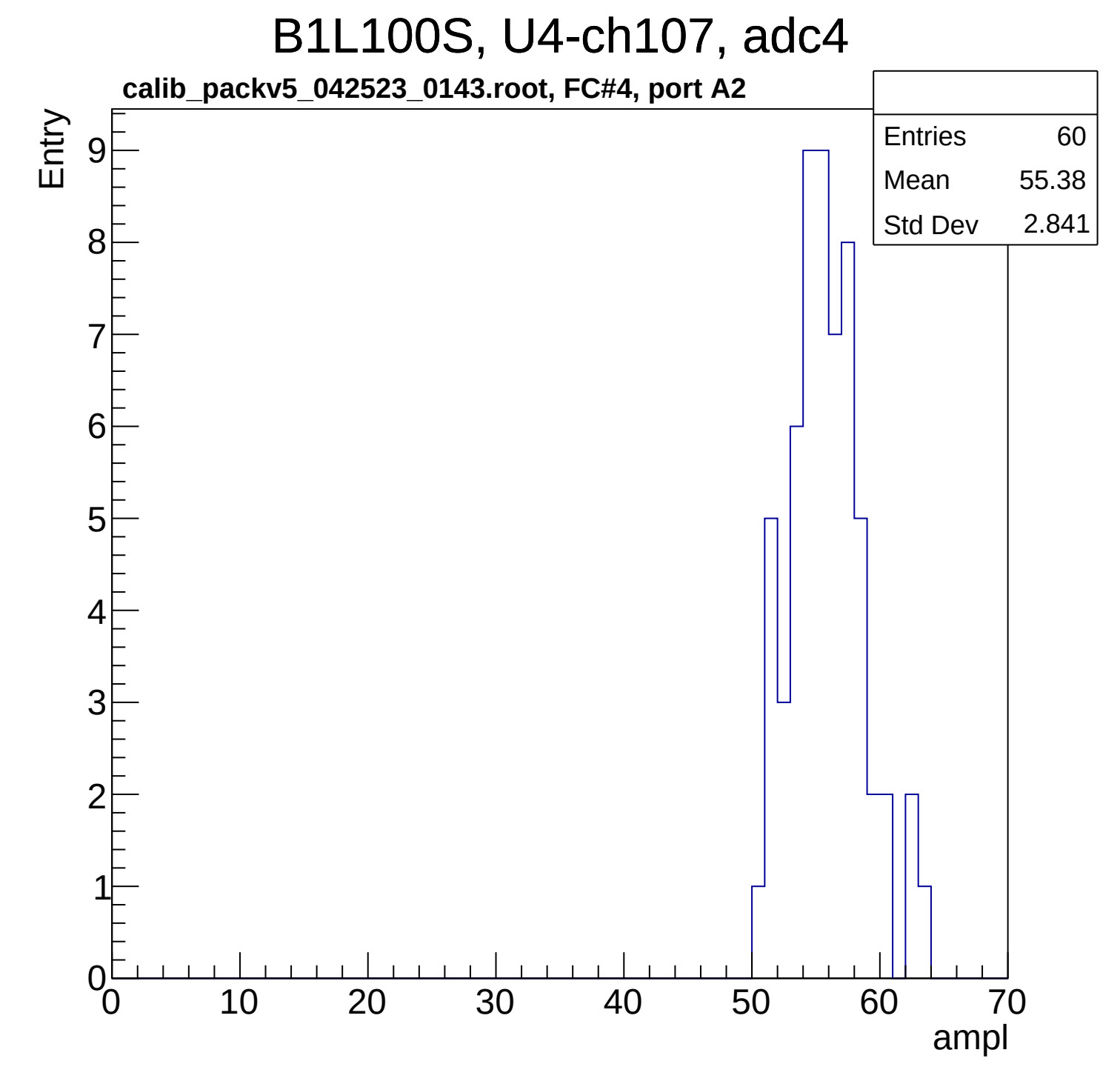

B1L100S, U4-ch106, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 36
Std Dev 27.34
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

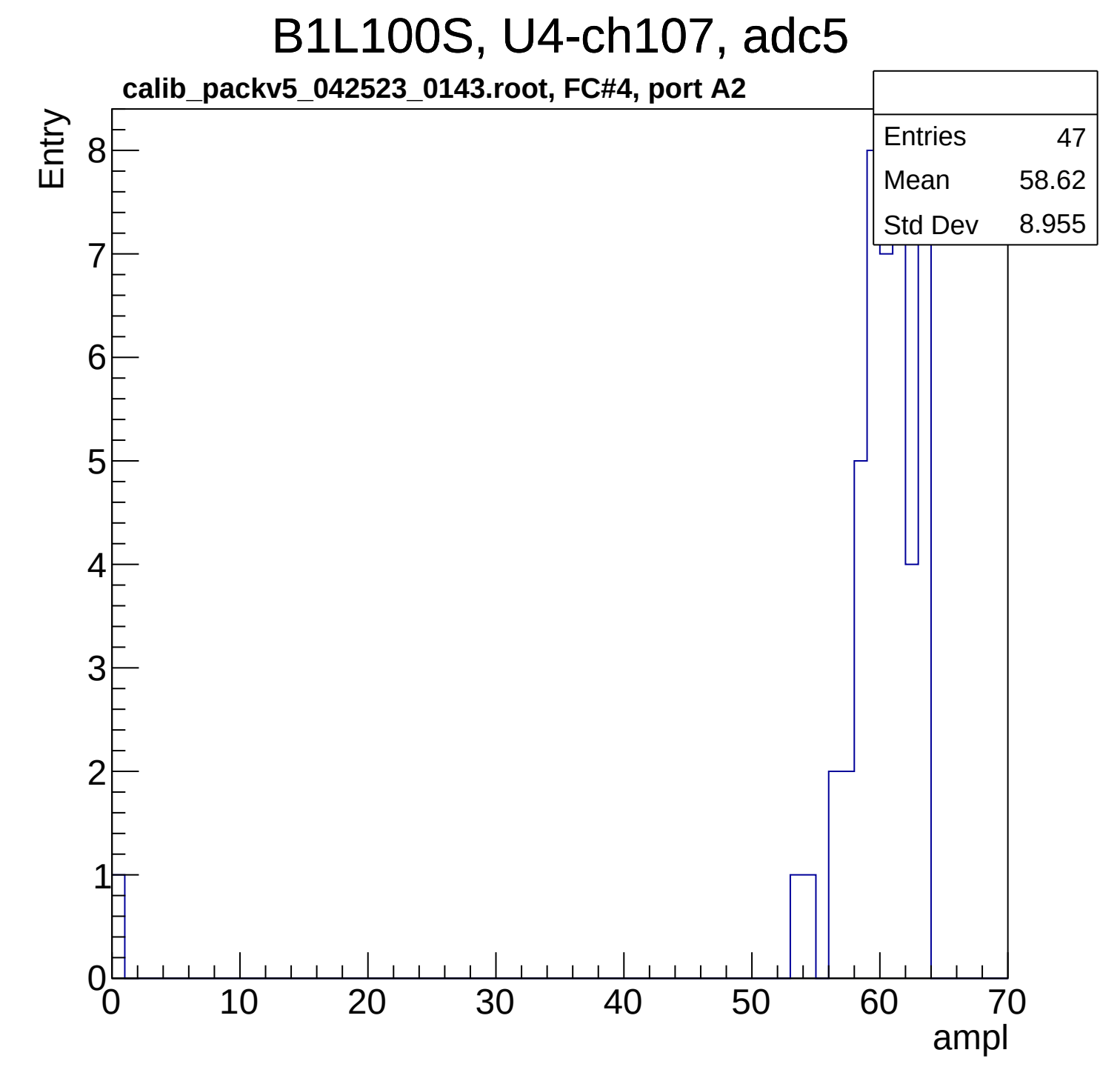

B1L100S, U4-ch107, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 28.55
Std Dev 6.209
Gaus mean : 29.6871
Gaus Width: 3.5898
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

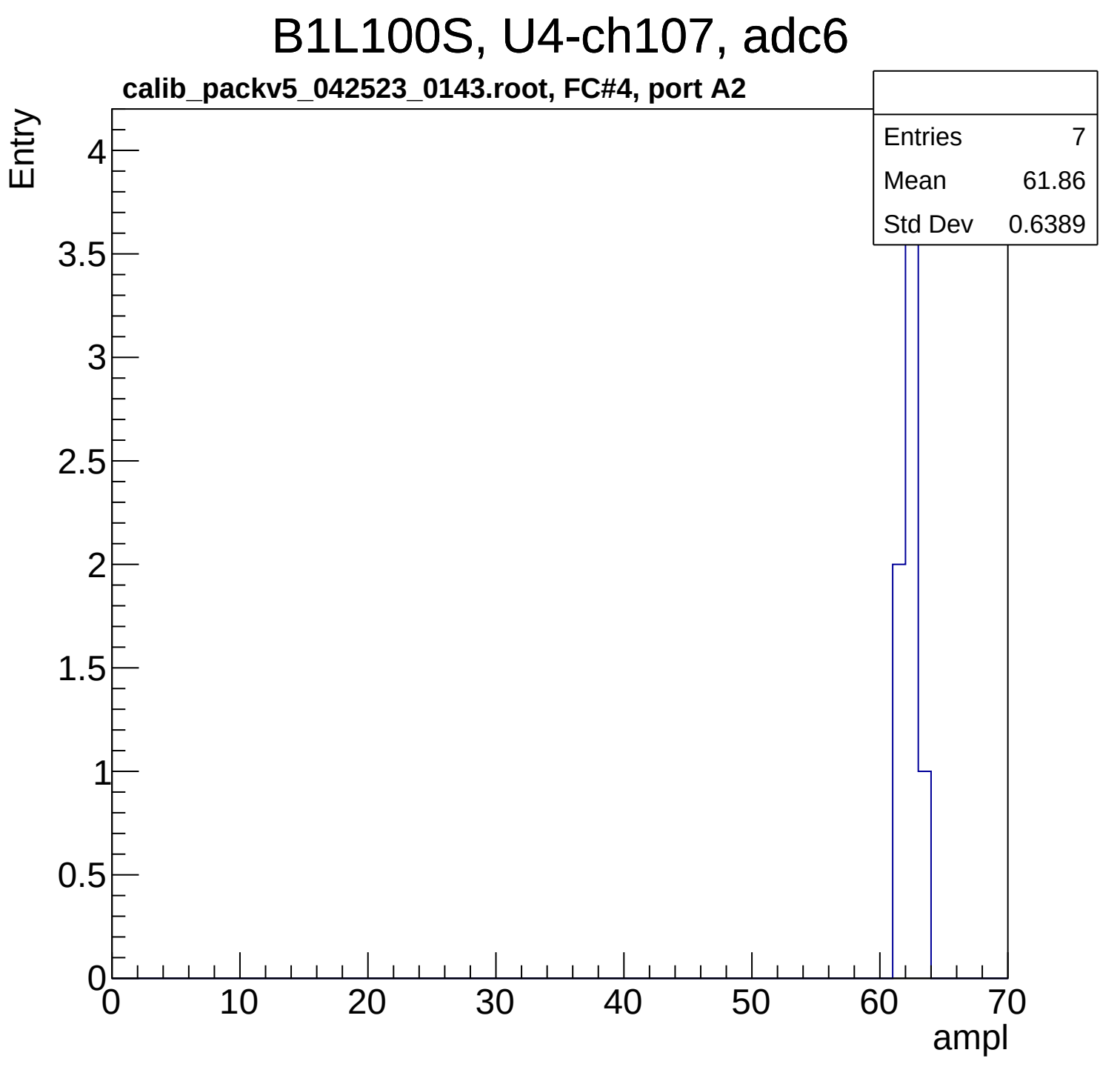

B1L100S, U4-ch107, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 36.29
Std Dev 3.594
Gaus mean : 36.5483
Gaus Width: 3.8419
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

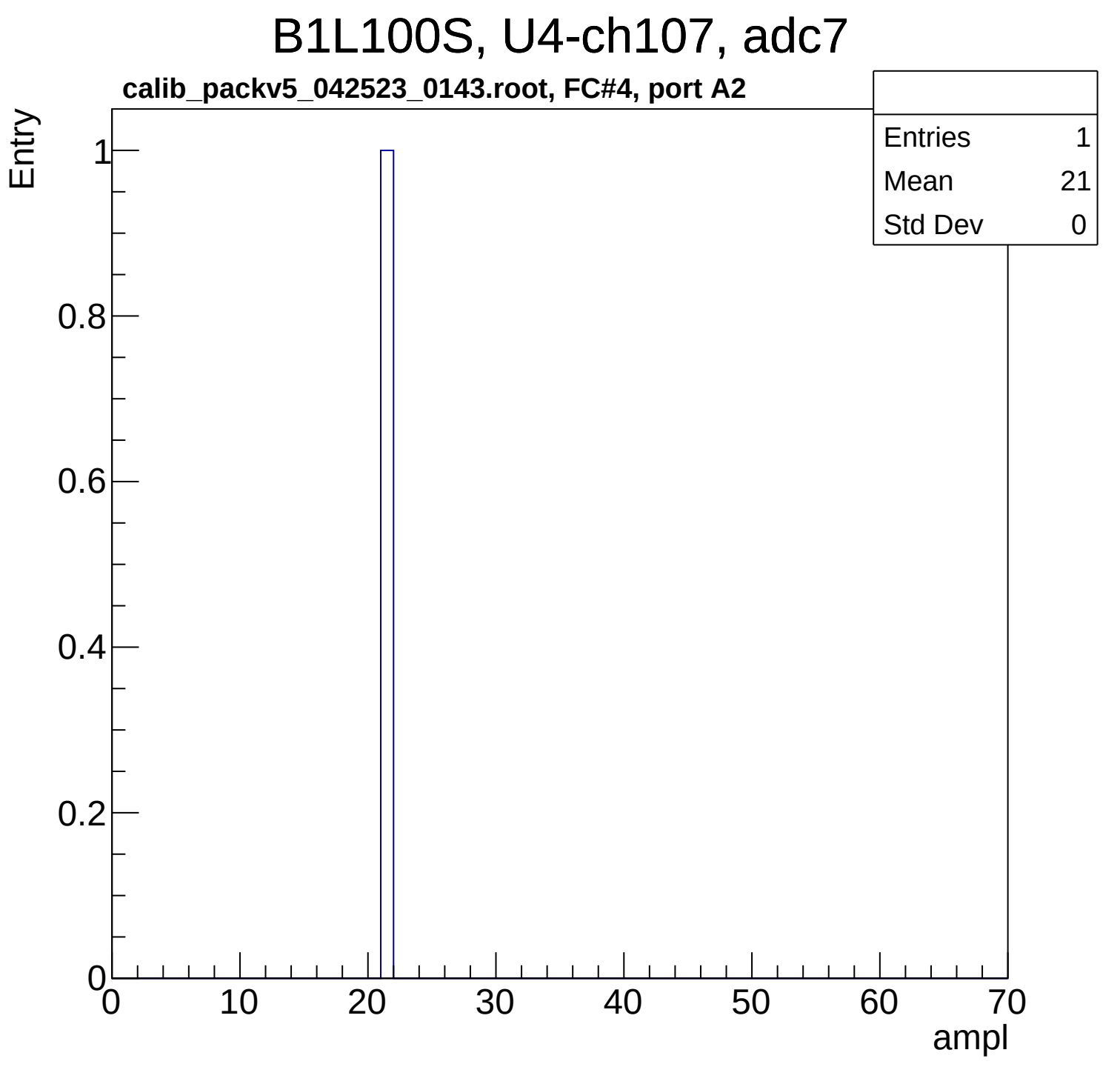

B1L100S, U4-ch107, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 42.44
Std Dev 3.628
Gaus mean : 42.1774
Gaus Width: 5.1662
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

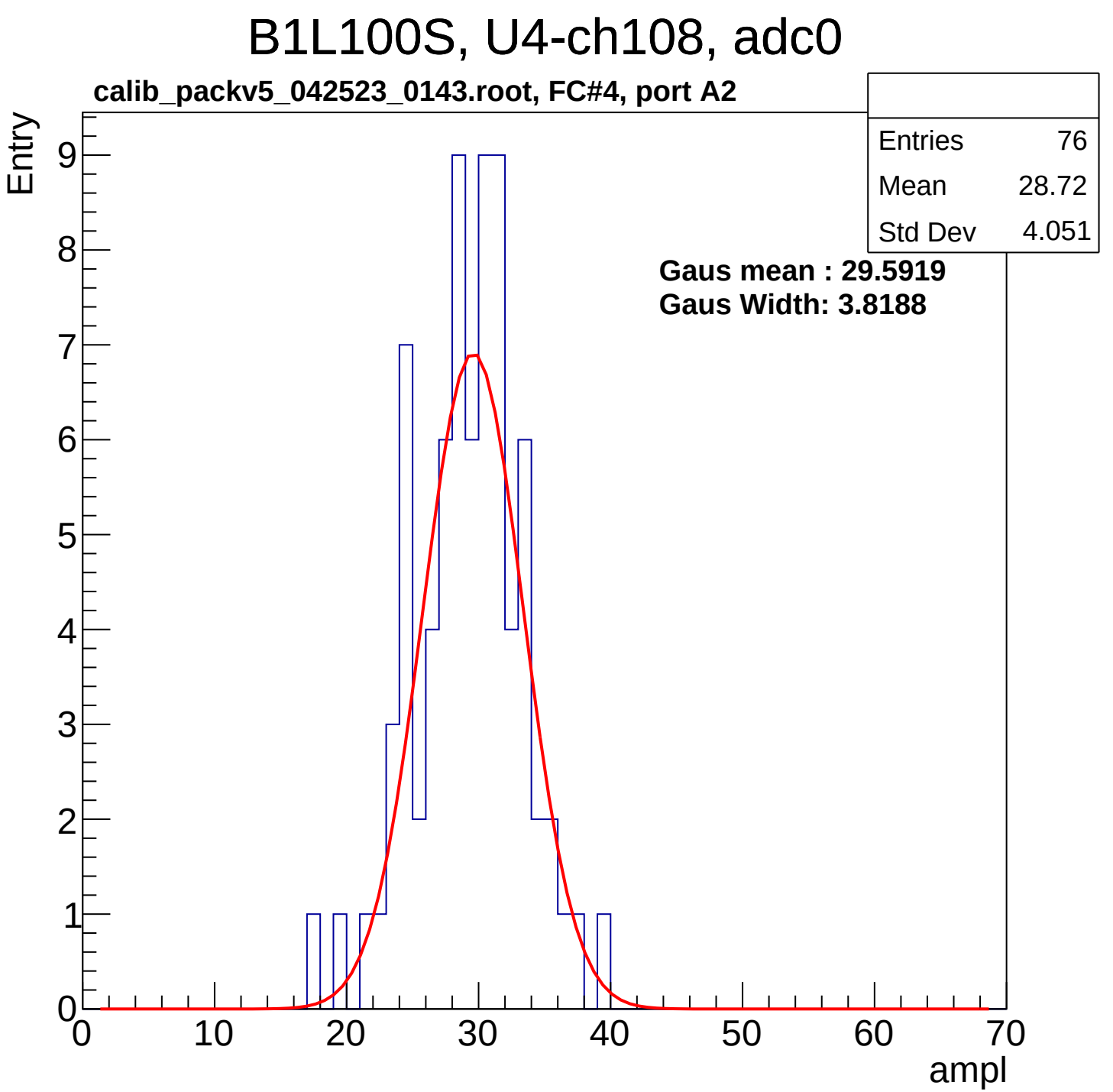

B1L100S, U4-ch107, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 48.45
Std Dev 3.542
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

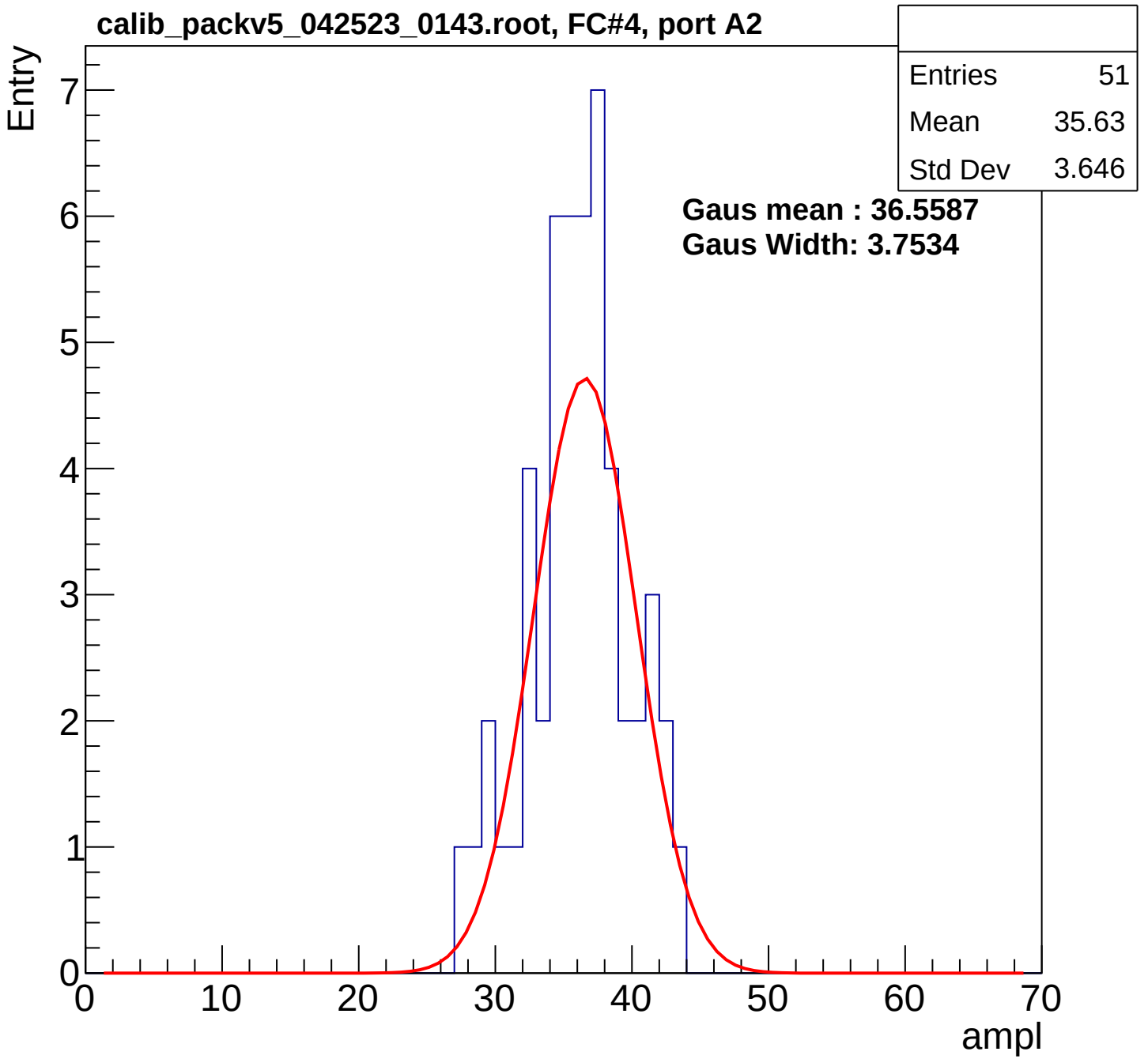

B1L100S, U4-ch107, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 55.38
Std Dev 2.841
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

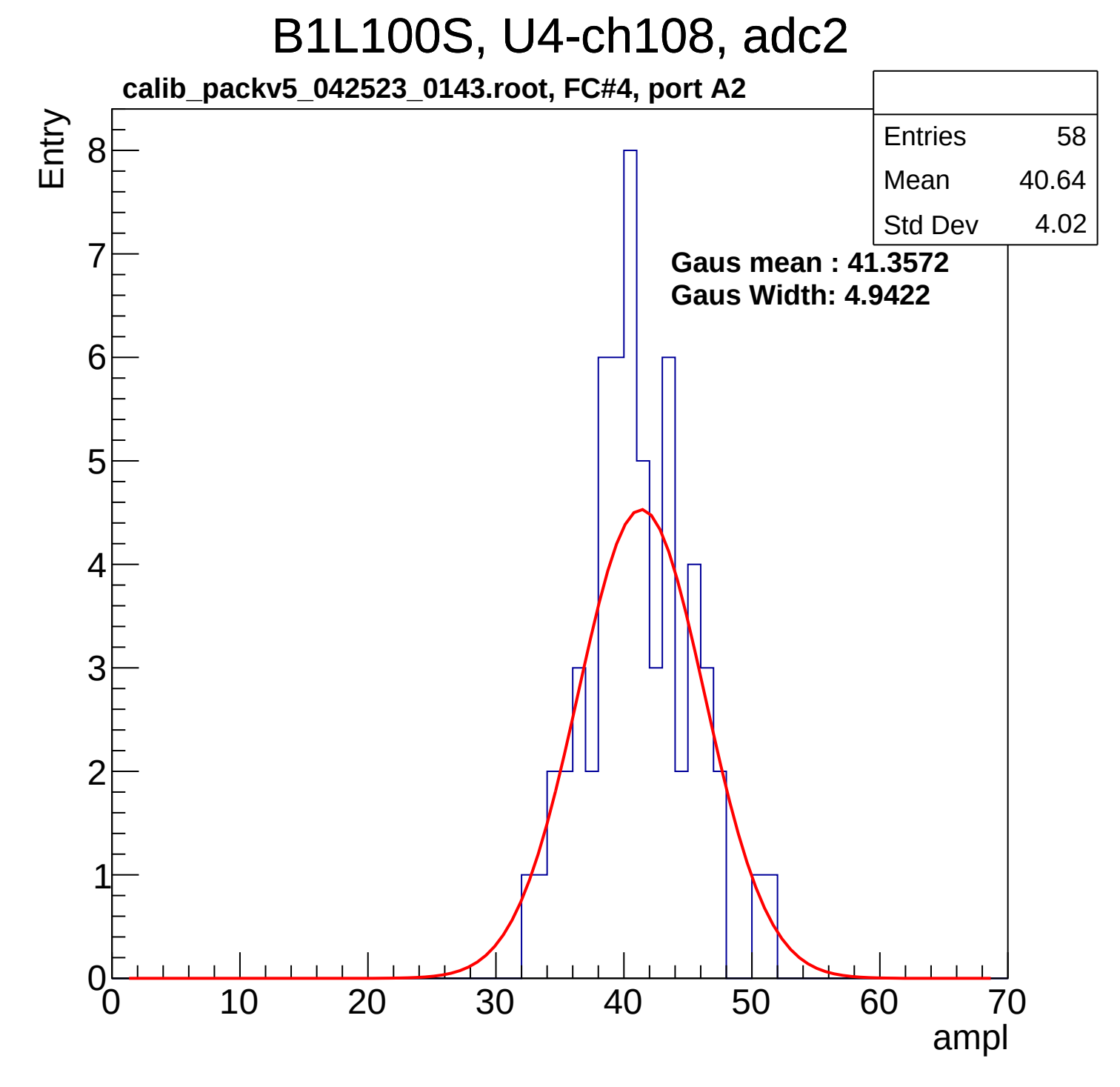

B1L100S, U4-ch107, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 58.62
Std Dev 8.955
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

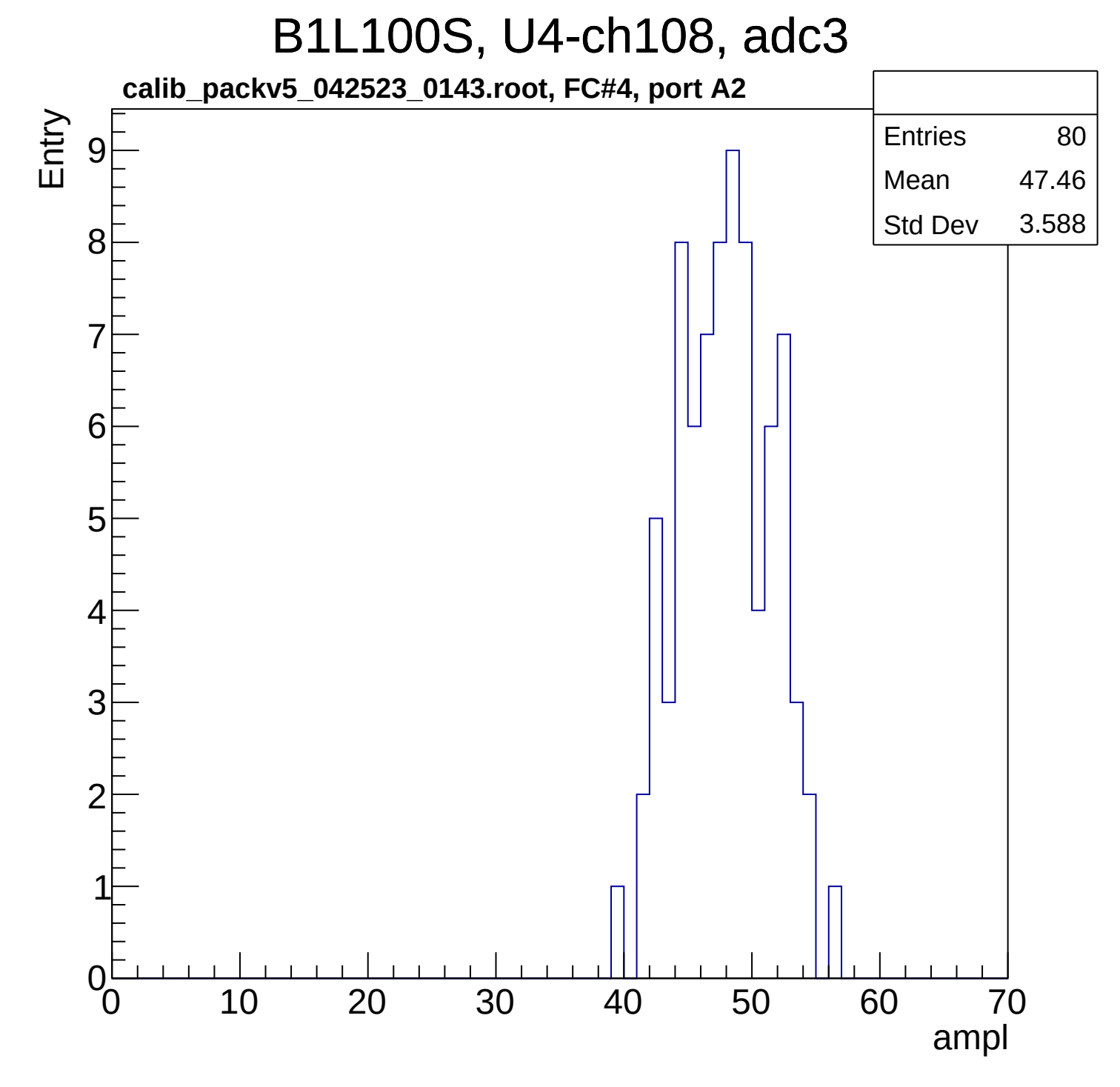

B1L100S, U4-ch107, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 61.86
Std Dev 0.6389
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

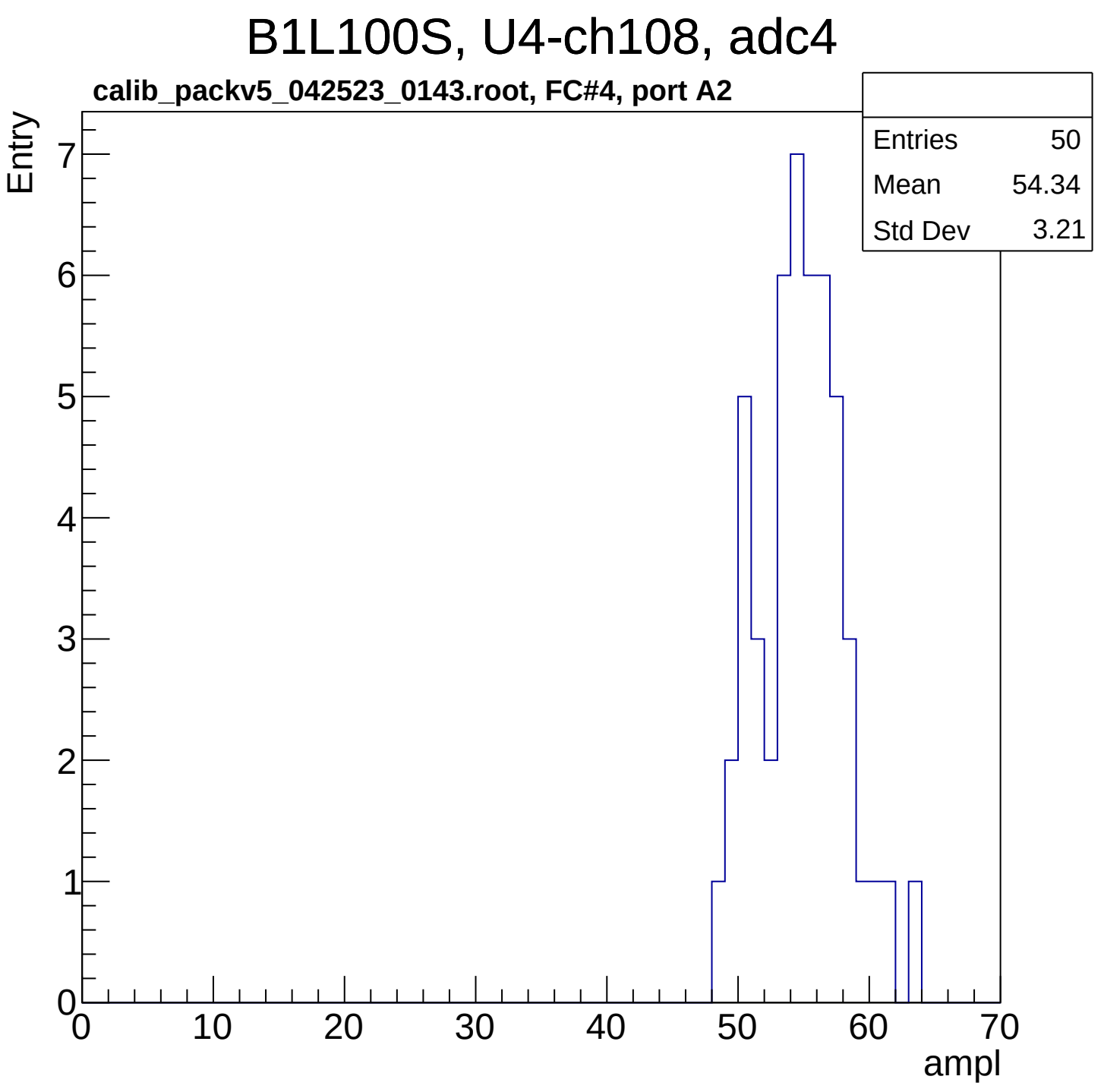

B1L100S, U4-ch107, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 21
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

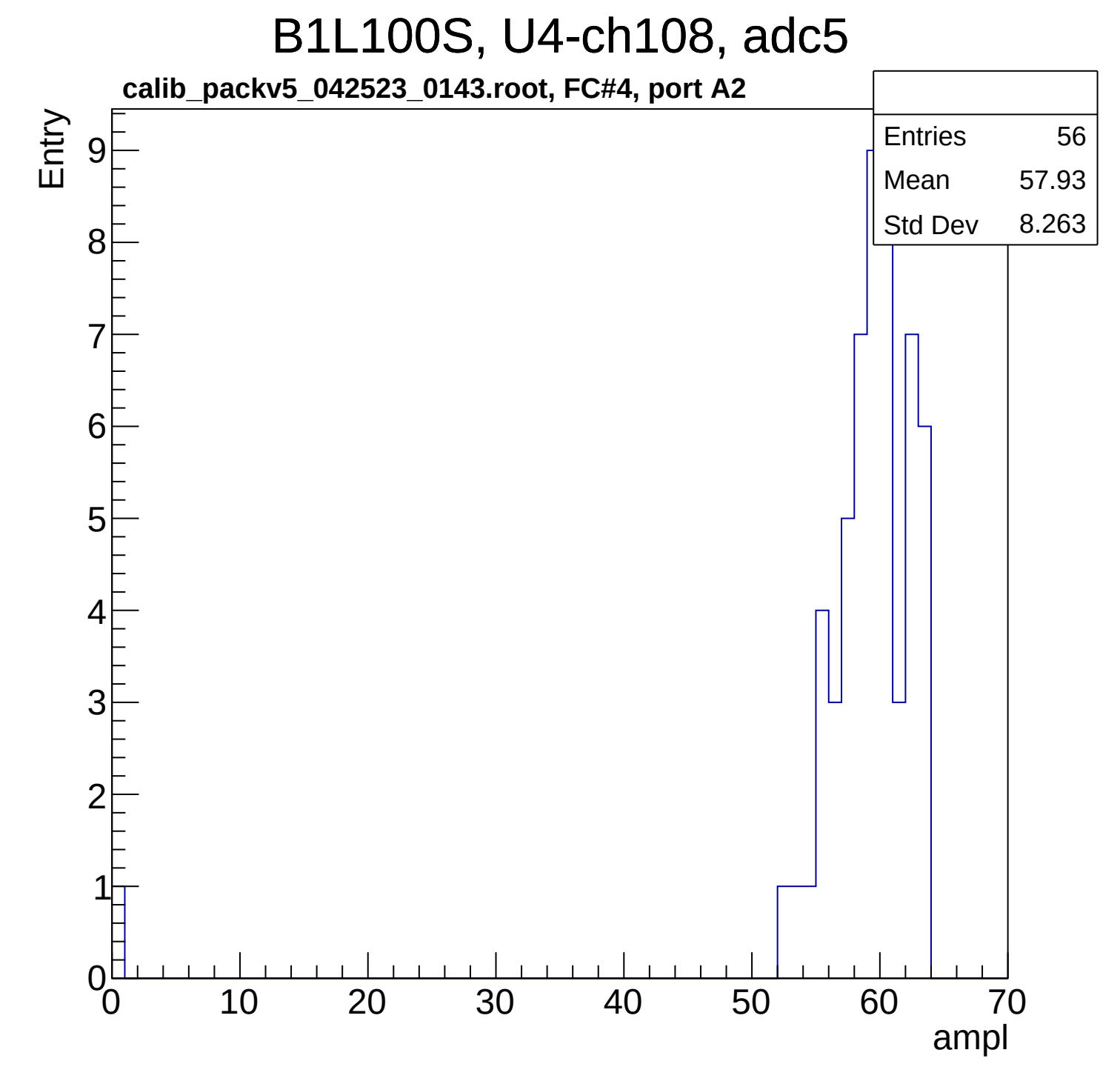

B1L100S, U4-ch108, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 28.72
Std Dev 4.051
Gaus mean : 29.5919
Gaus Width: 3.8188
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

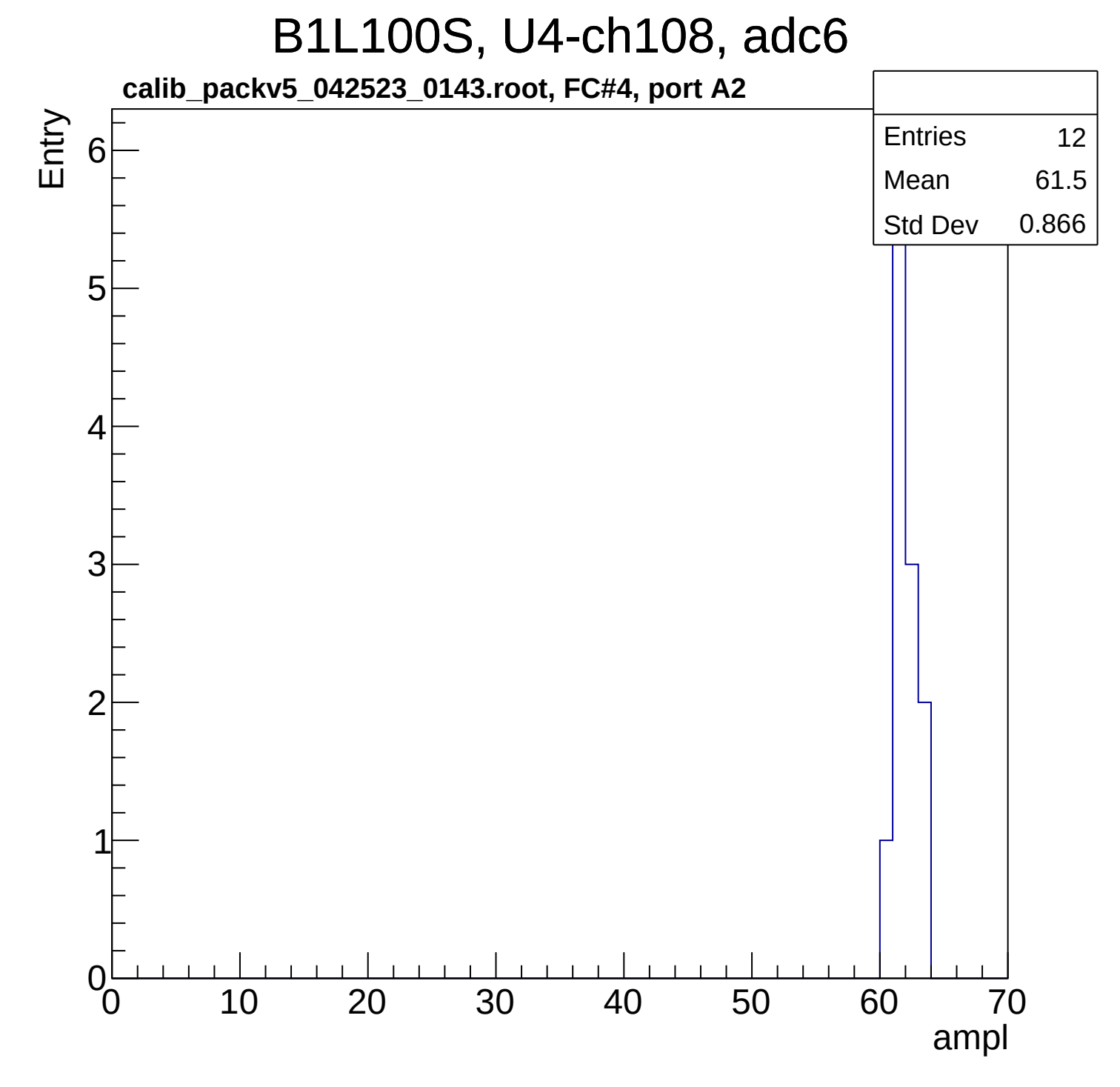

B1L100S, U4-ch108, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 35.63
Std Dev 3.646
Gaus mean : 36.5587
Gaus Width: 3.7534
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

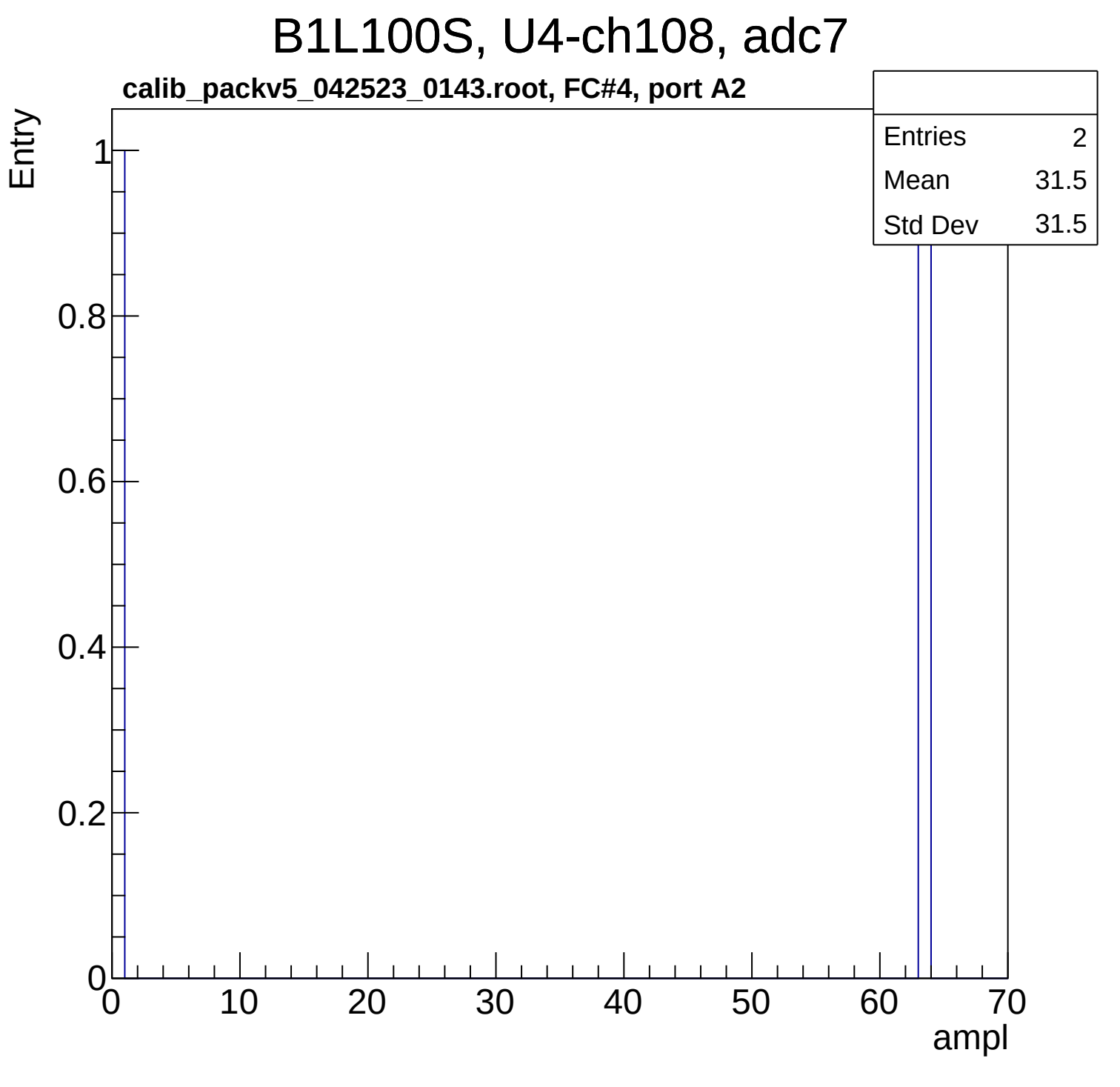

B1L100S, U4-ch108, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 40.64
Std Dev 4.02
Gaus mean : 41.3572
Gaus Width: 4.9422
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

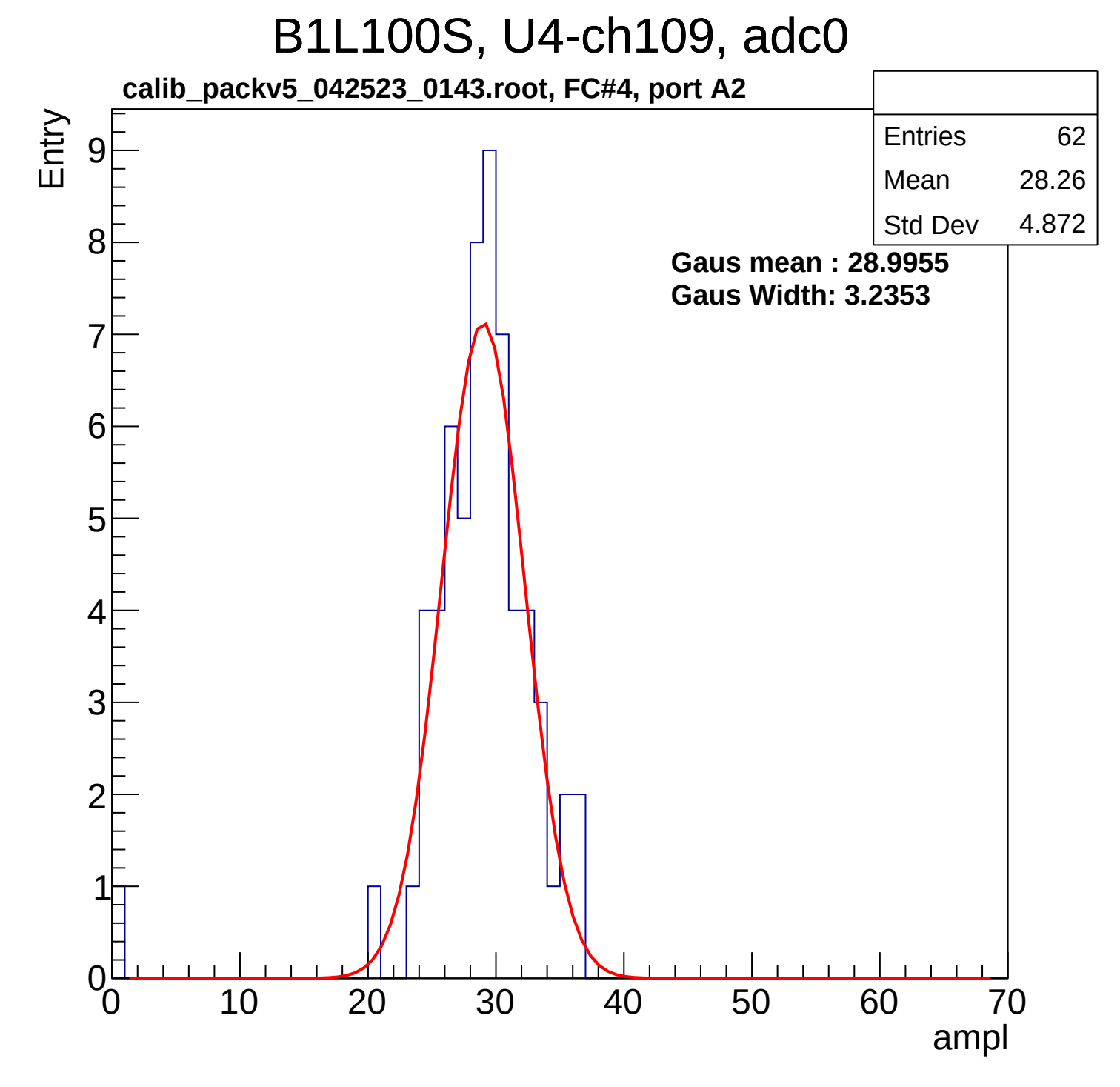

B1L100S, U4-ch108, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 47.46
Std Dev 3.588
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

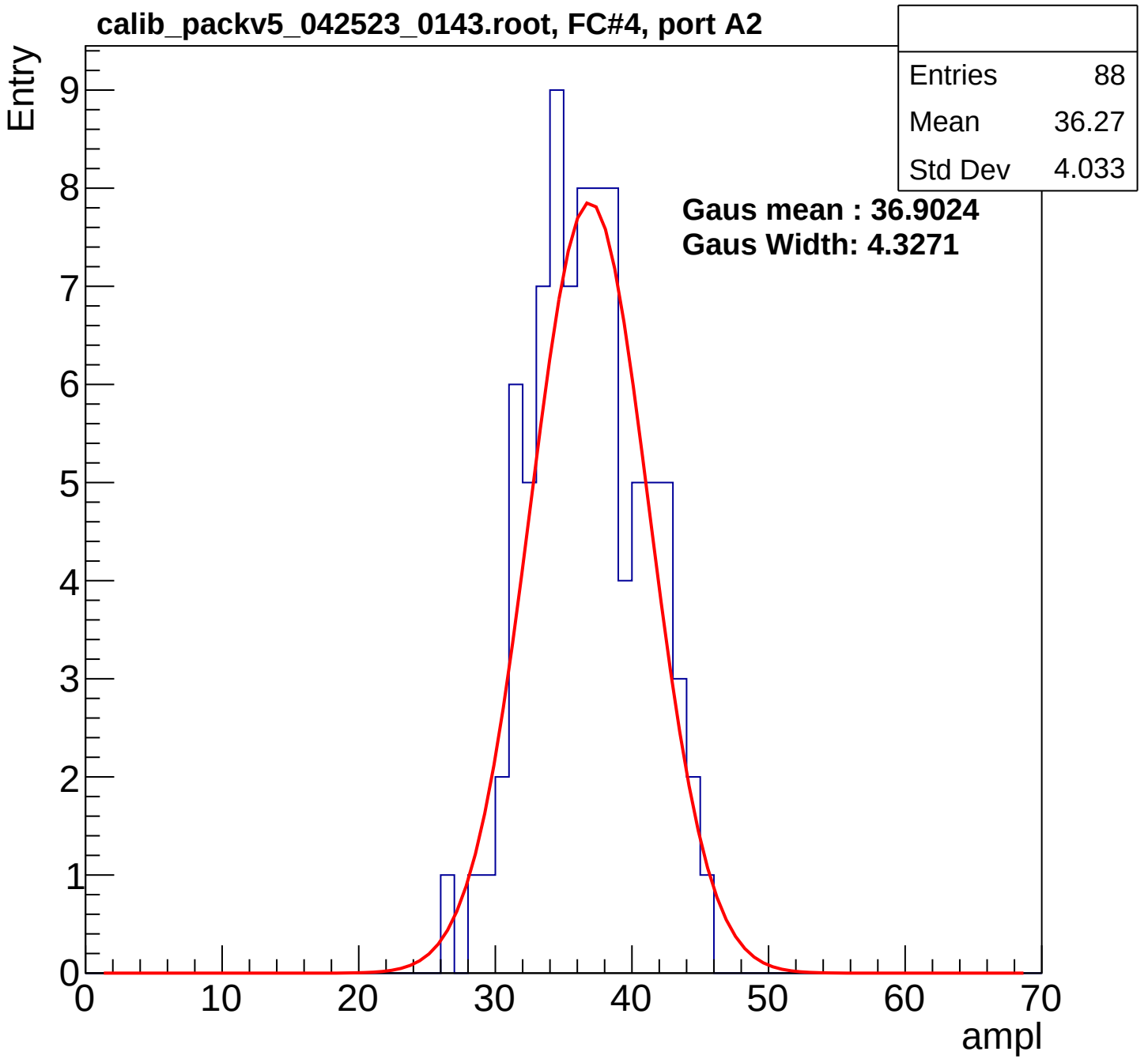

B1L100S, U4-ch108, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 54.34
Std Dev 3.21
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

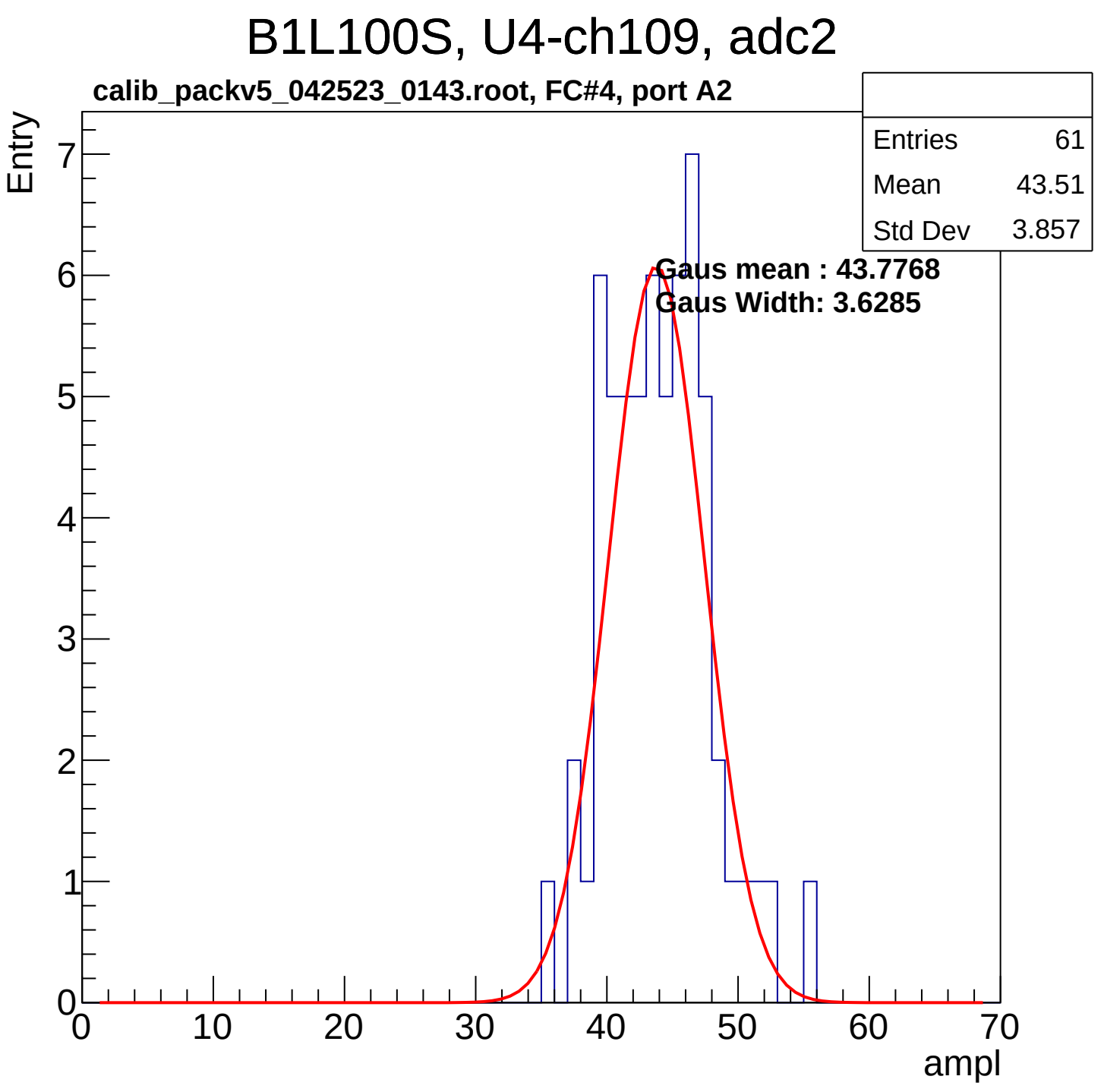

B1L100S, U4-ch108, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 57.93
Std Dev 8.263
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

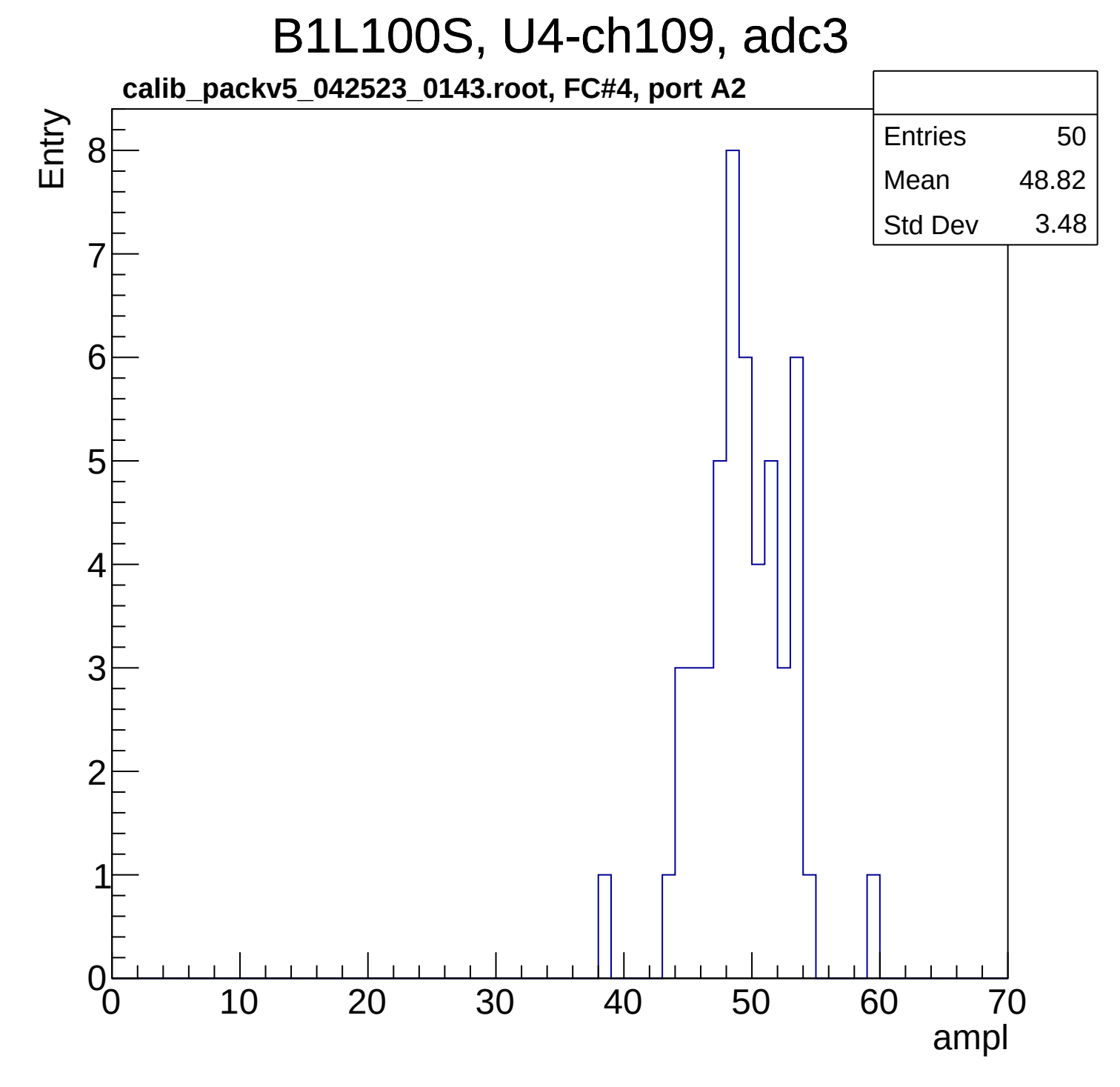

B1L100S, U4-ch108, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 12
Mean 61.5
Std Dev 0.866
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

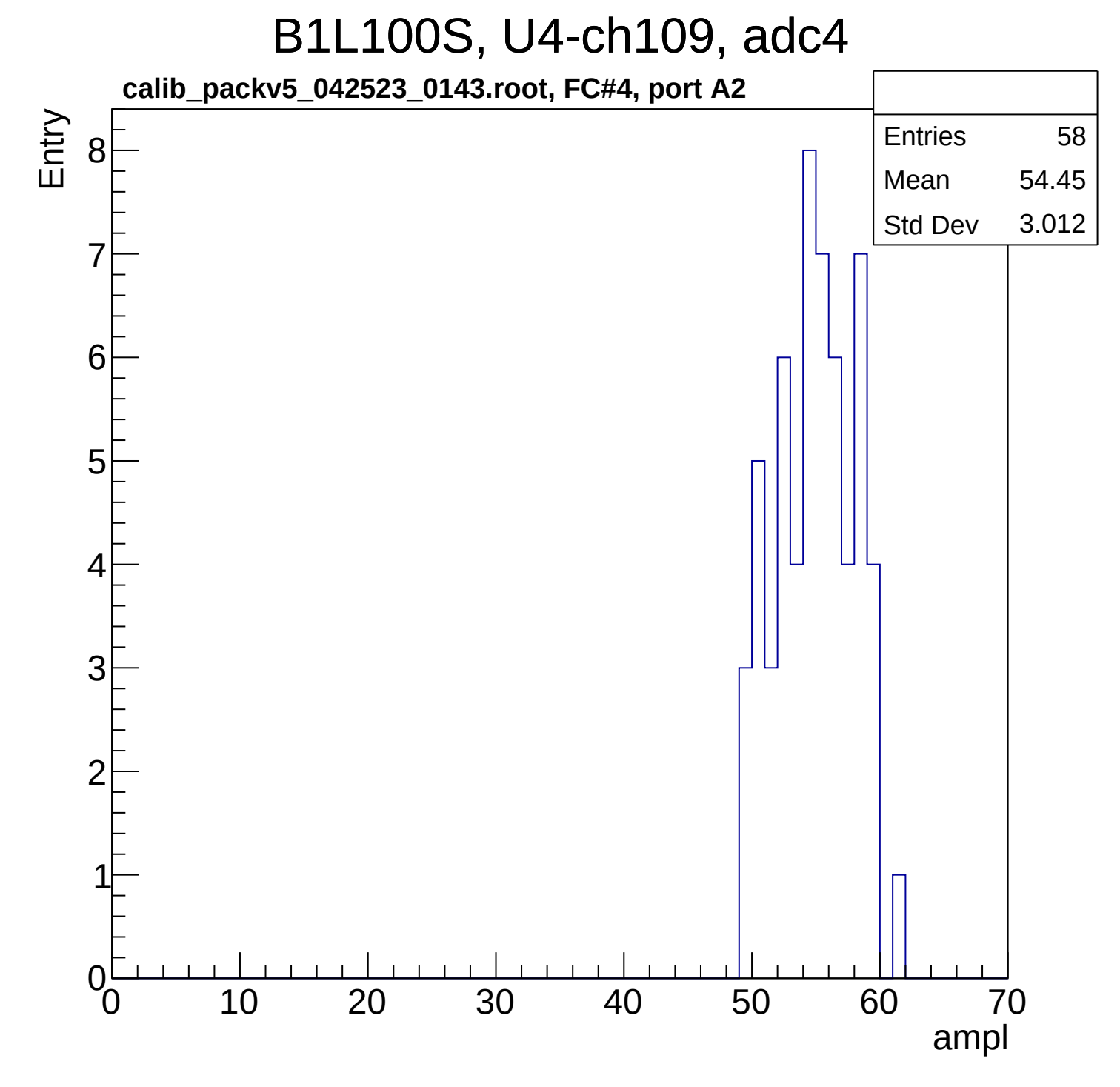

B1L100S, U4-ch108, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

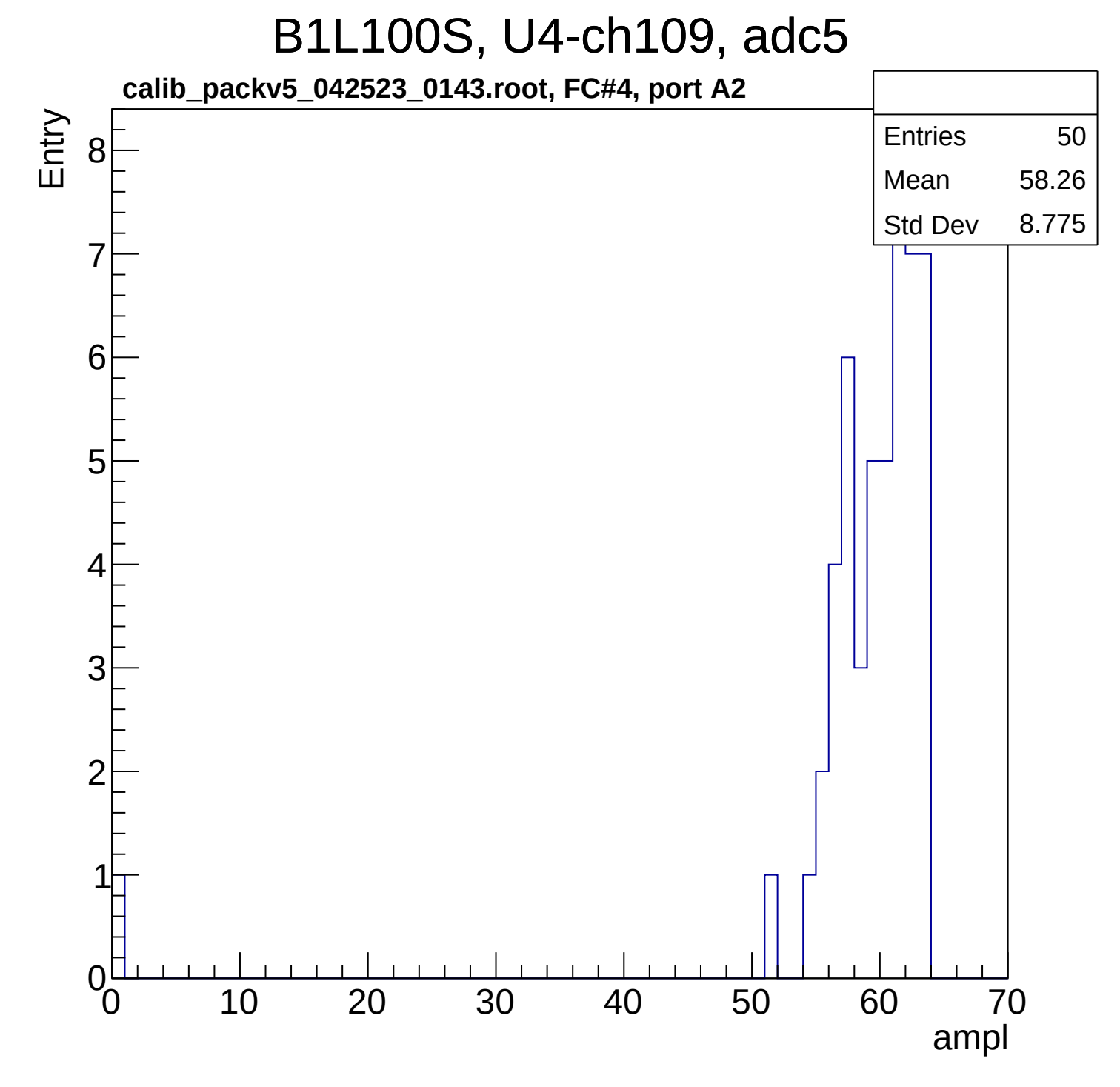

B1L100S, U4-ch109, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 28.26
Std Dev 4.872
Gaus mean : 28.9955
Gaus Width: 3.2353
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

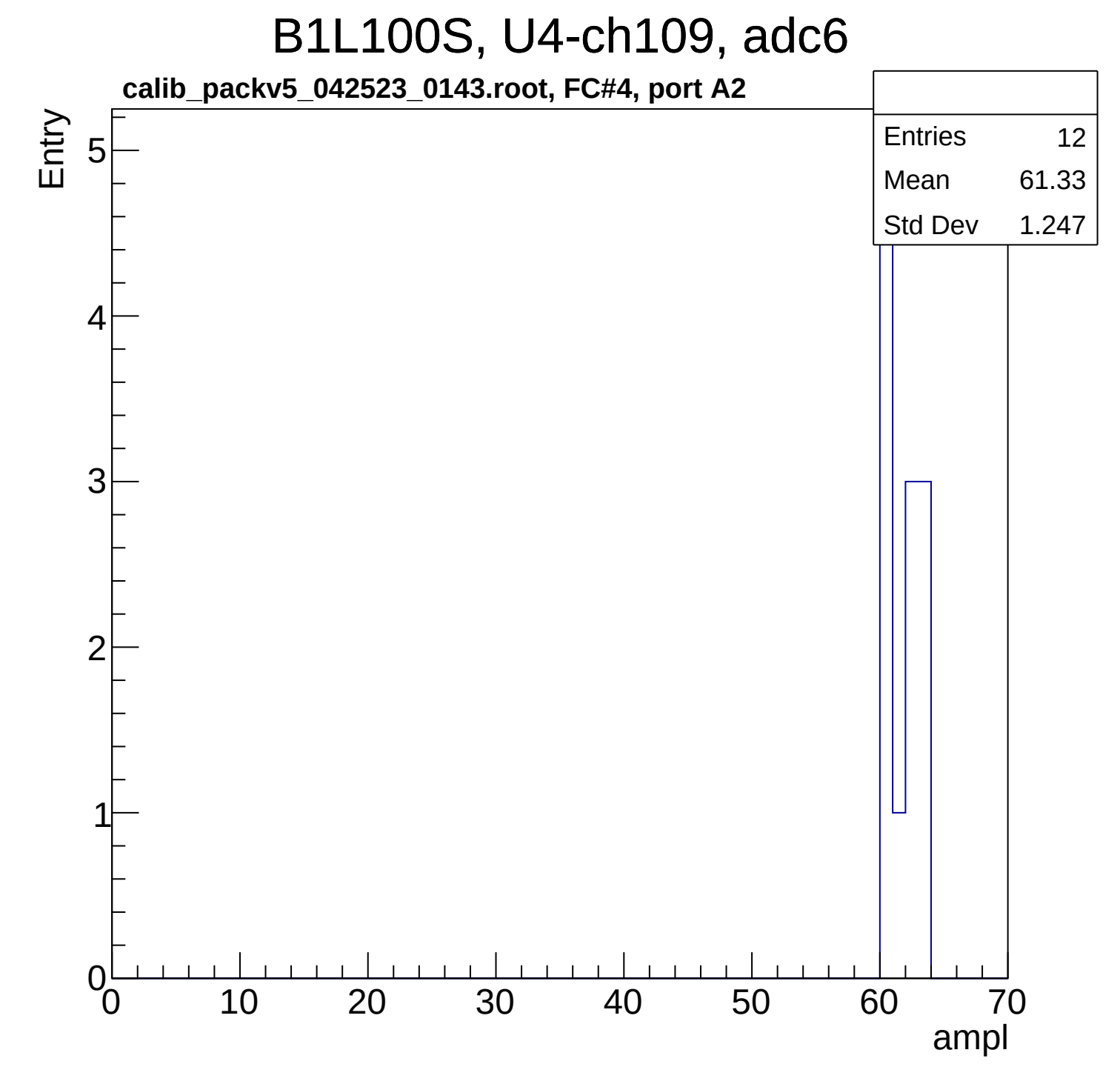

B1L100S, U4-ch109, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 88
Mean 36.27
Std Dev 4.033
Gaus mean : 36.9024
Gaus Width: 4.3271
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

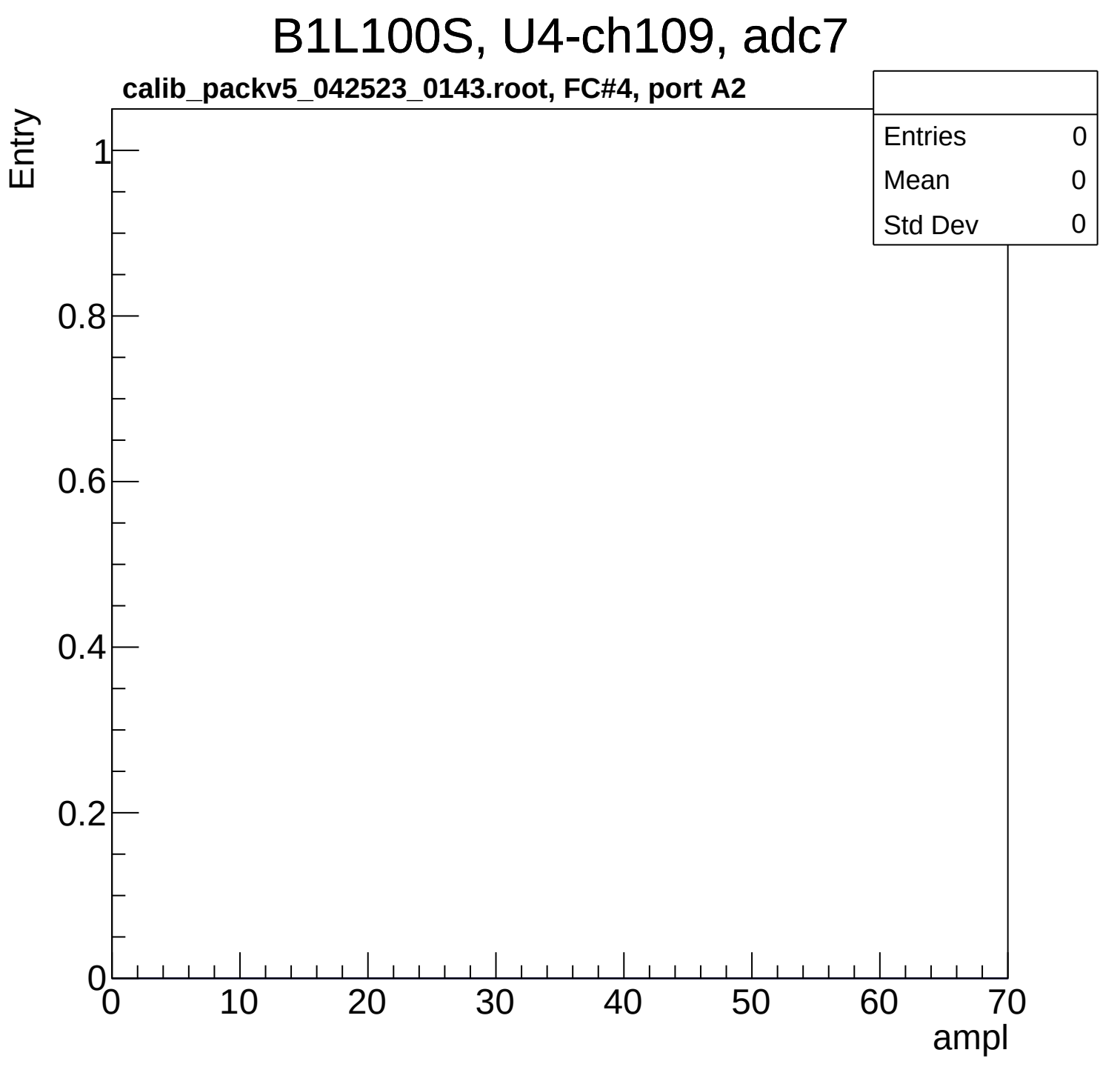

B1L100S, U4-ch109, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 43.51
Std Dev 3.857
Gaus mean : 43.7768
Gaus Width: 3.6285
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

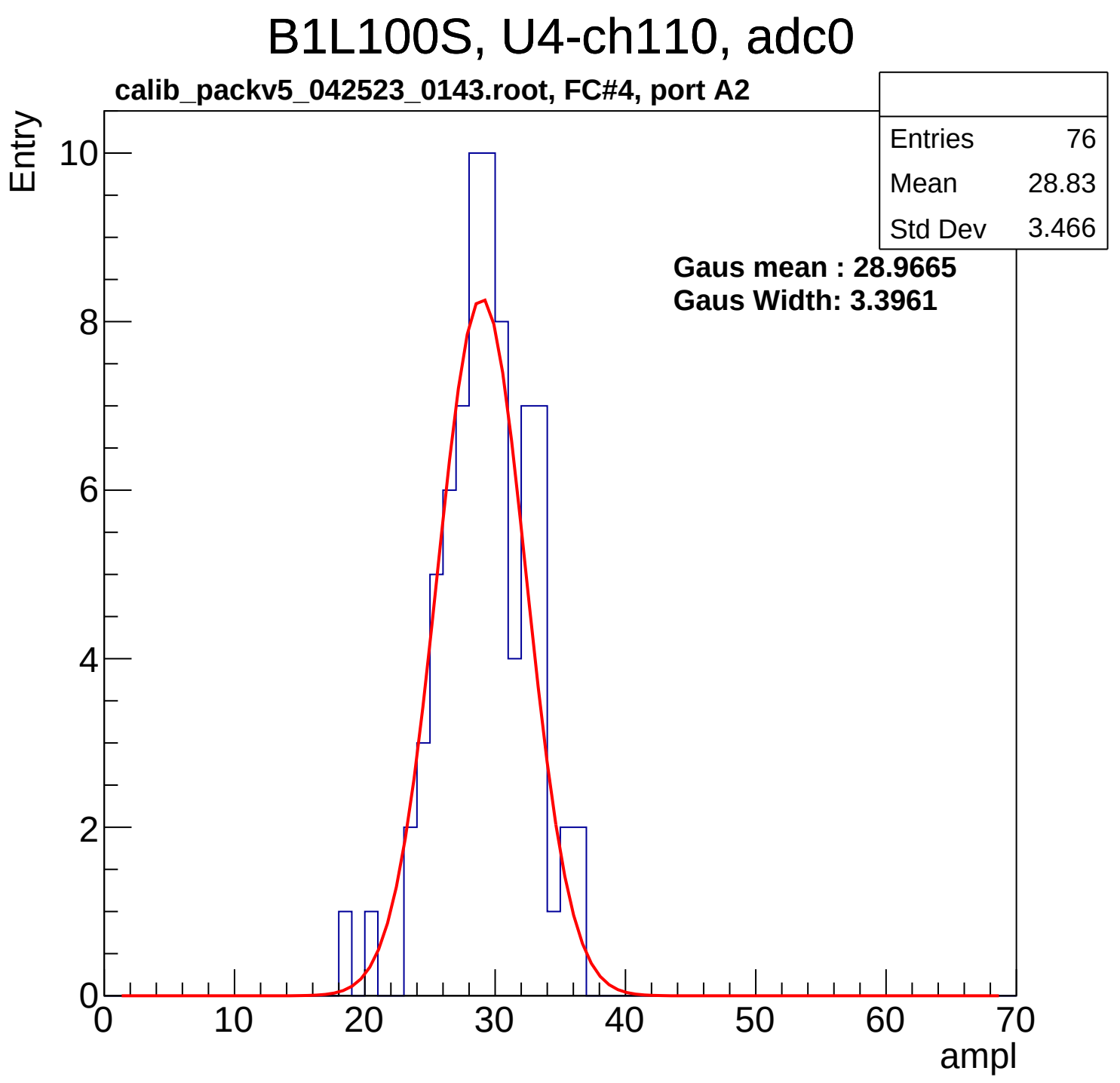

B1L100S, U4-ch109, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 48.82
Std Dev 3.48
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

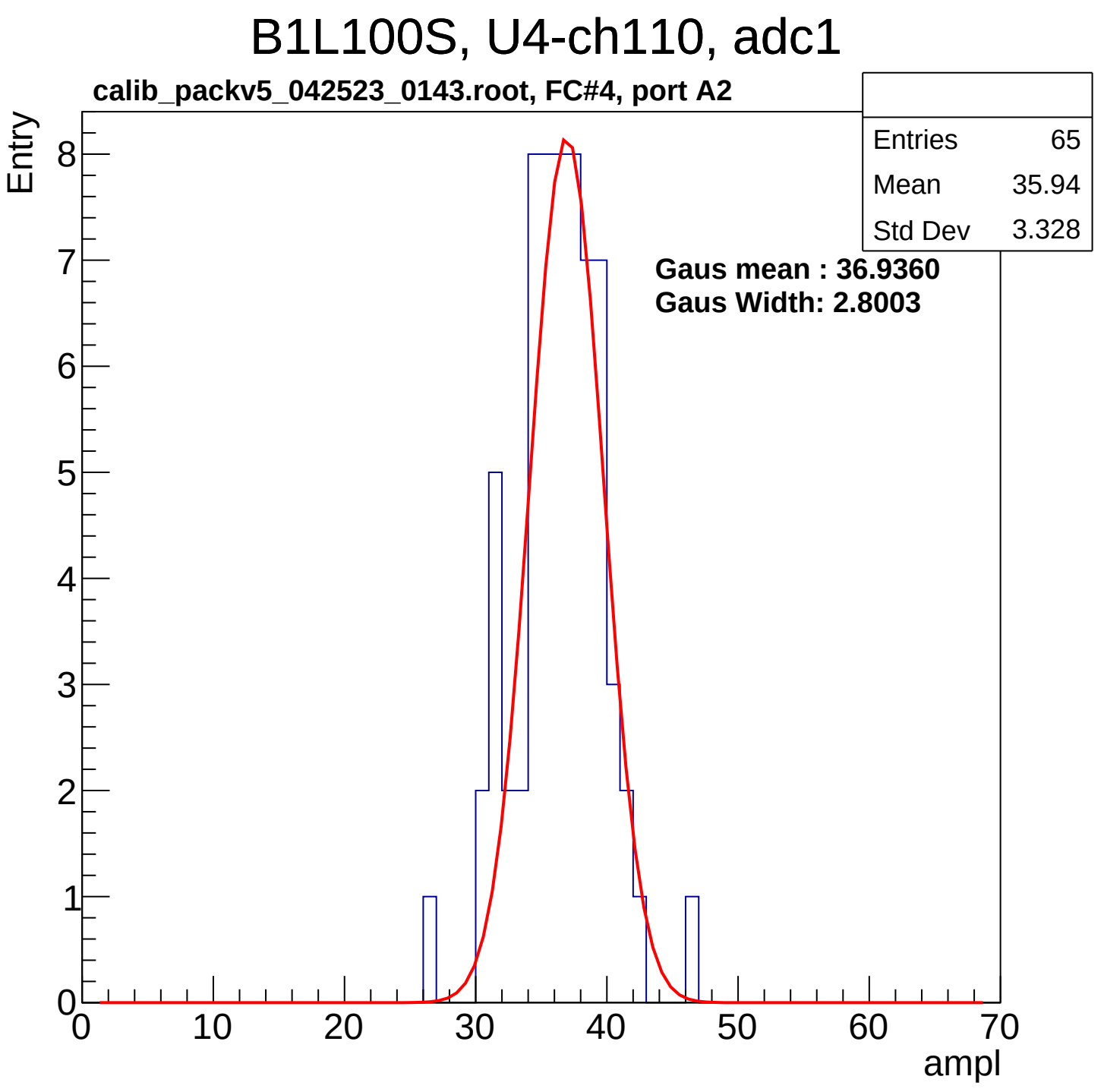

B1L100S, U4-ch109, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 54.45
Std Dev 3.012
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

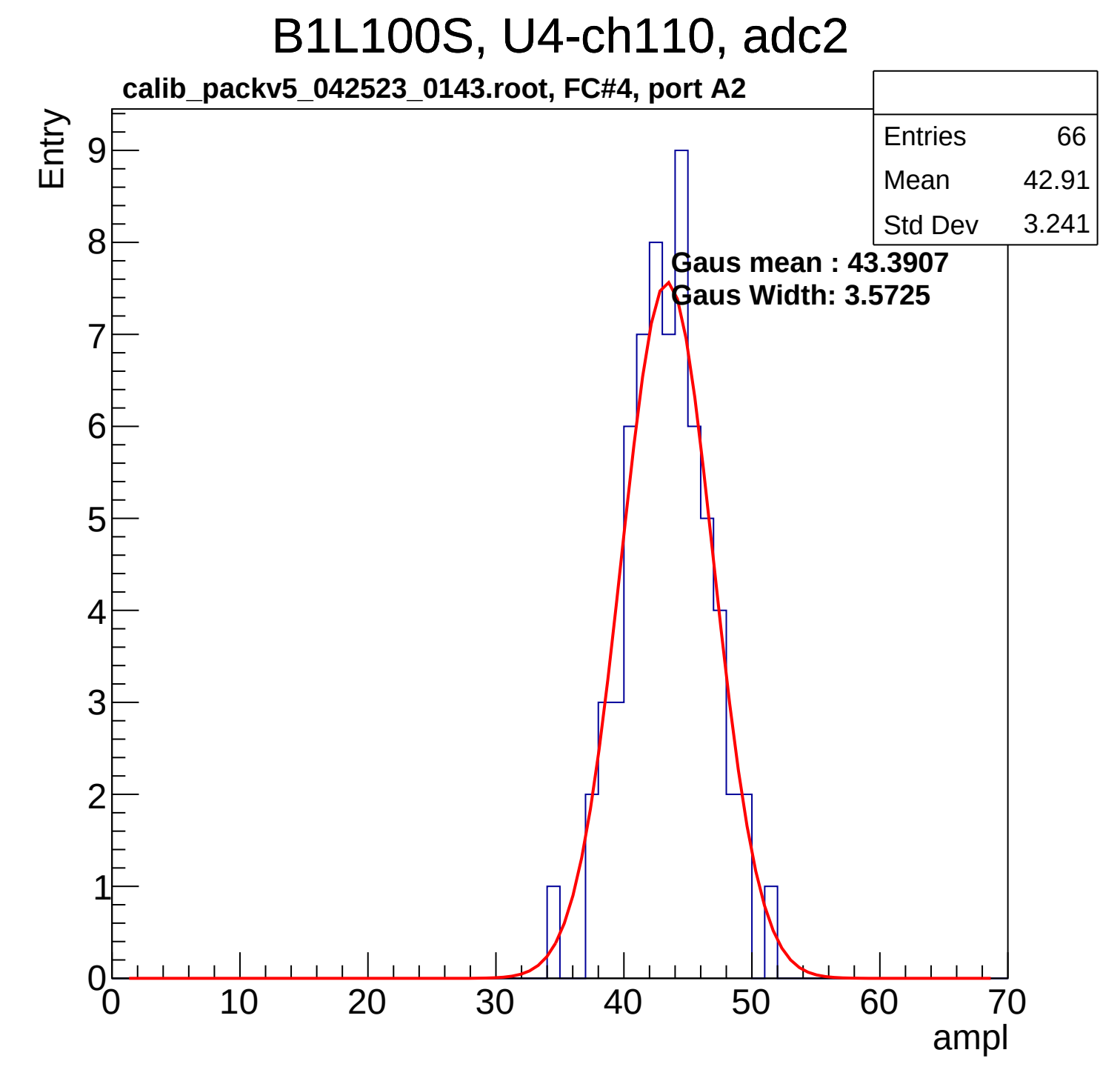

B1L100S, U4-ch109, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 58.26
Std Dev 8.775
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

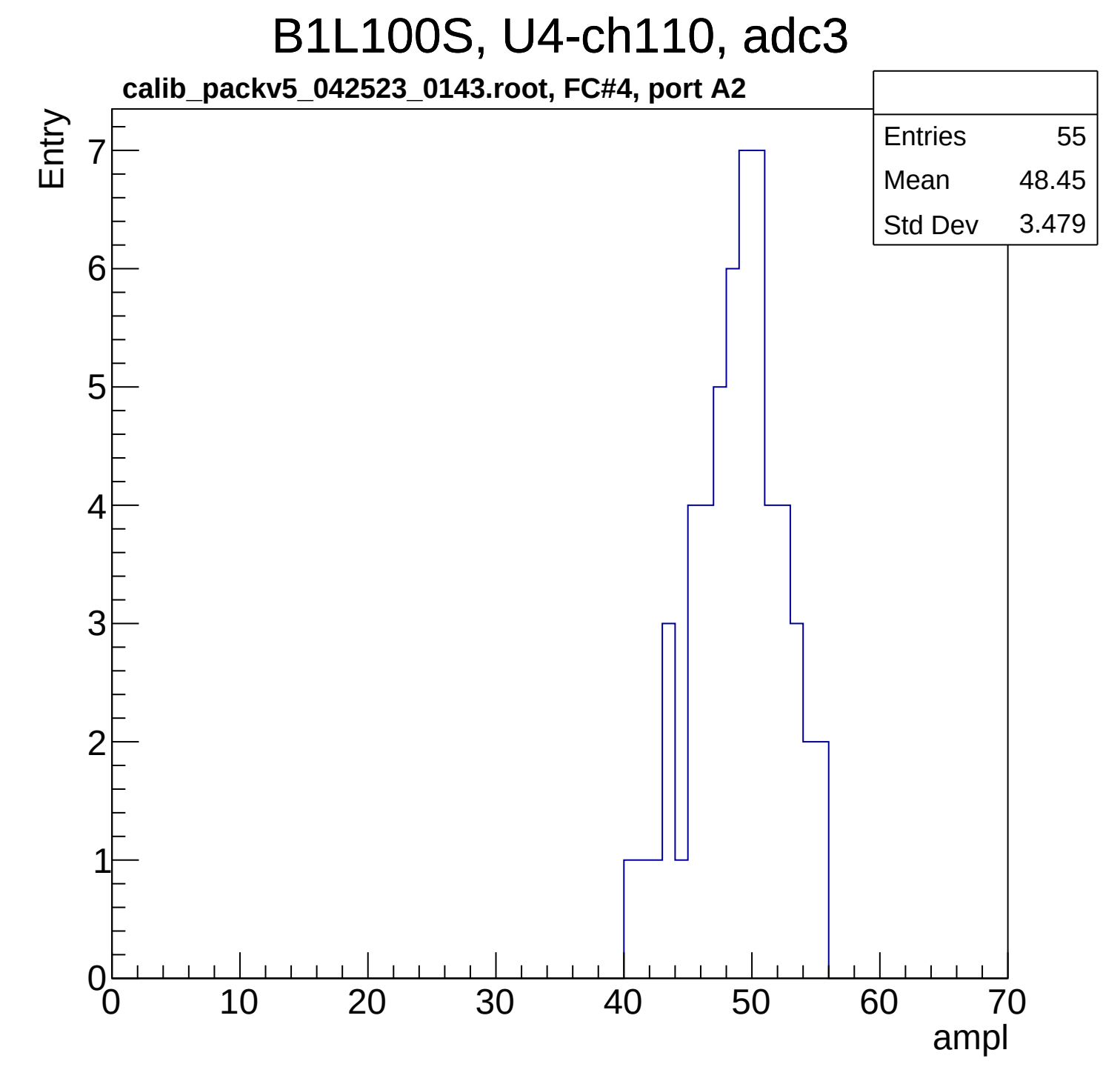

B1L100S, U4-ch109, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 12
Mean 61.33
Std Dev 1.247
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

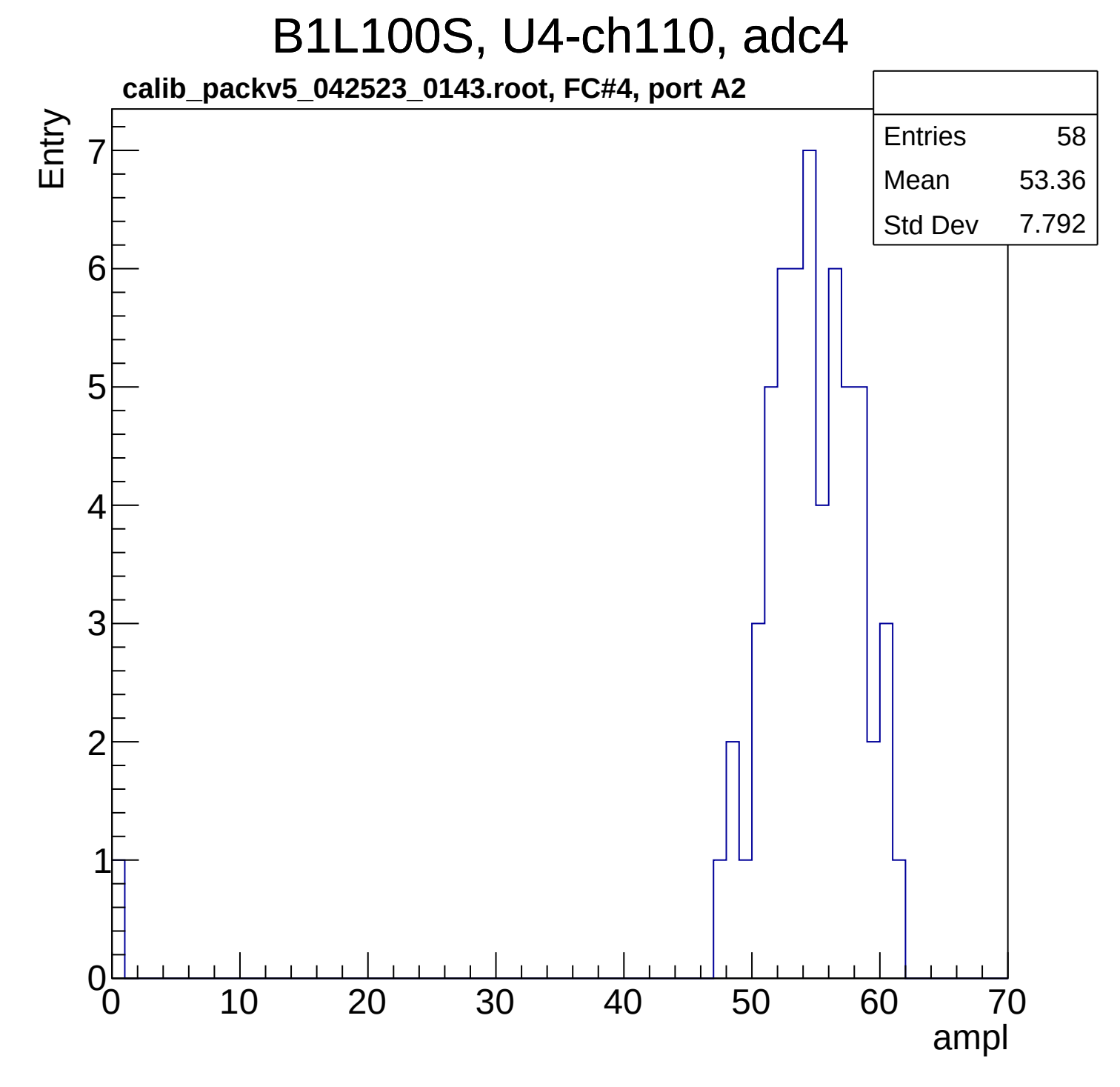

B1L100S, U4-ch109, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

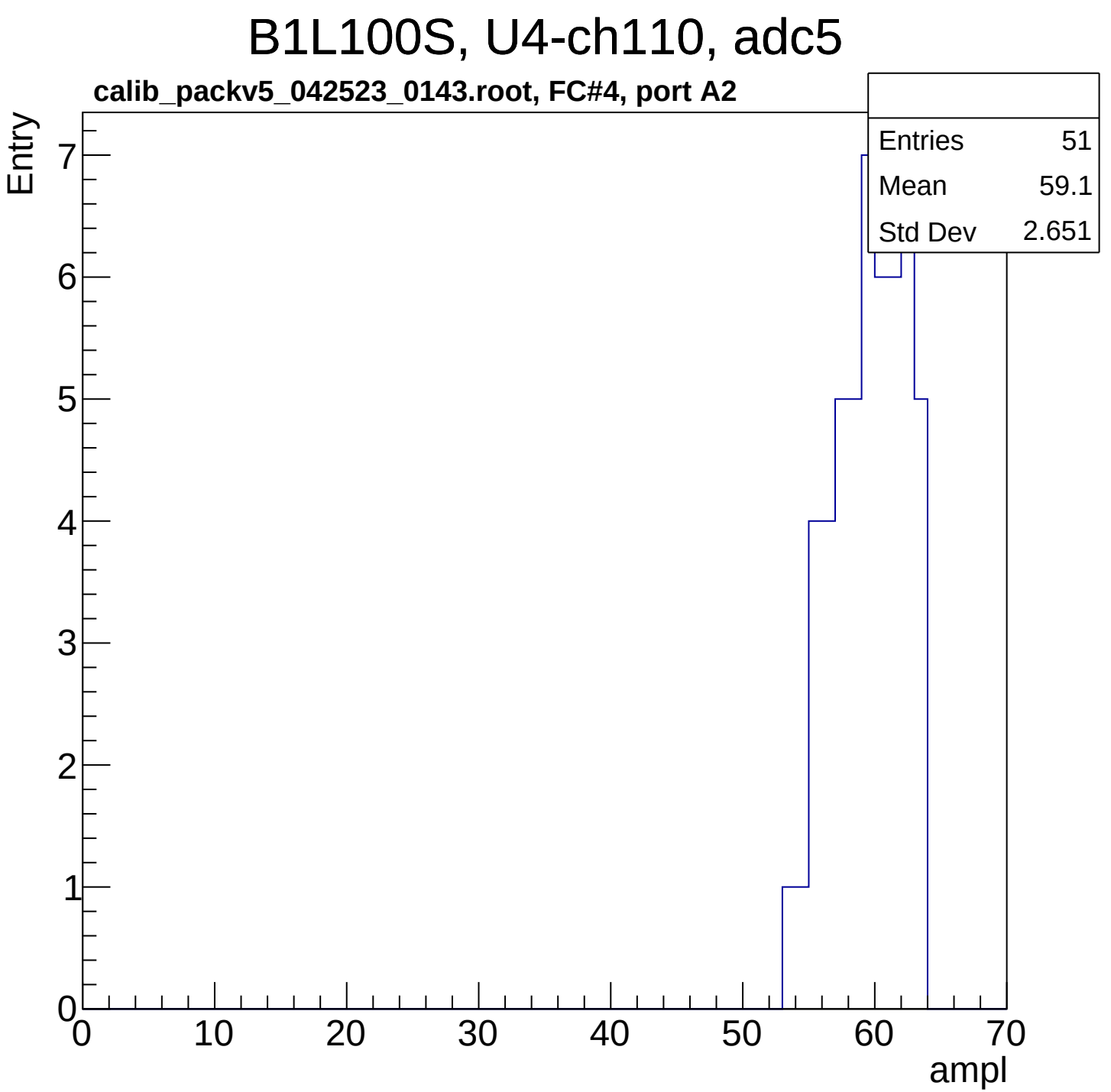

B1L100S, U4-ch110, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 28.83
Std Dev 3.466
Gaus mean : 28.9665
Gaus Width: 3.3961
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

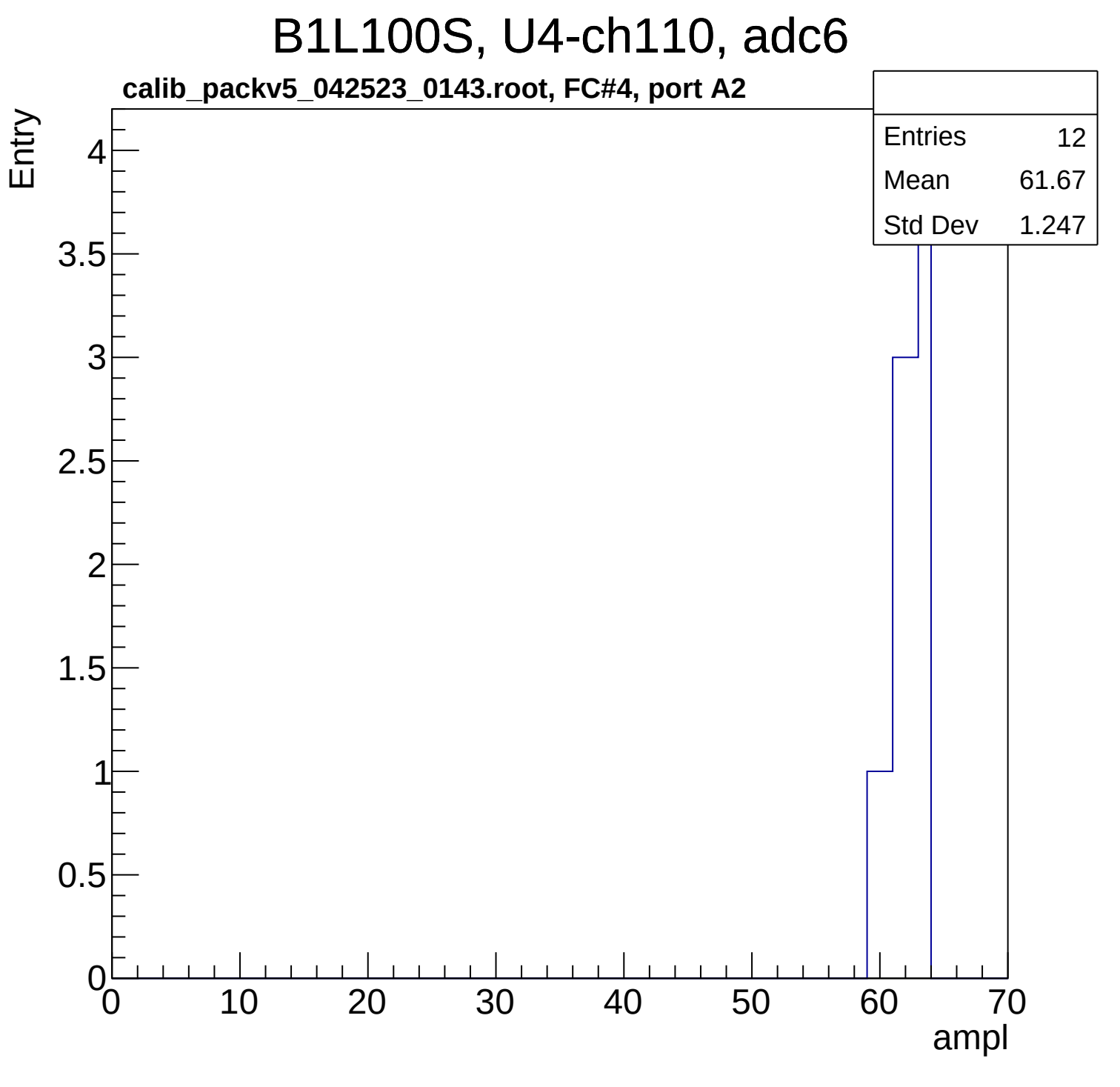

B1L100S, U4-ch110, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 35.94
Std Dev 3.328
Gaus mean : 36.9360
Gaus Width: 2.8003
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

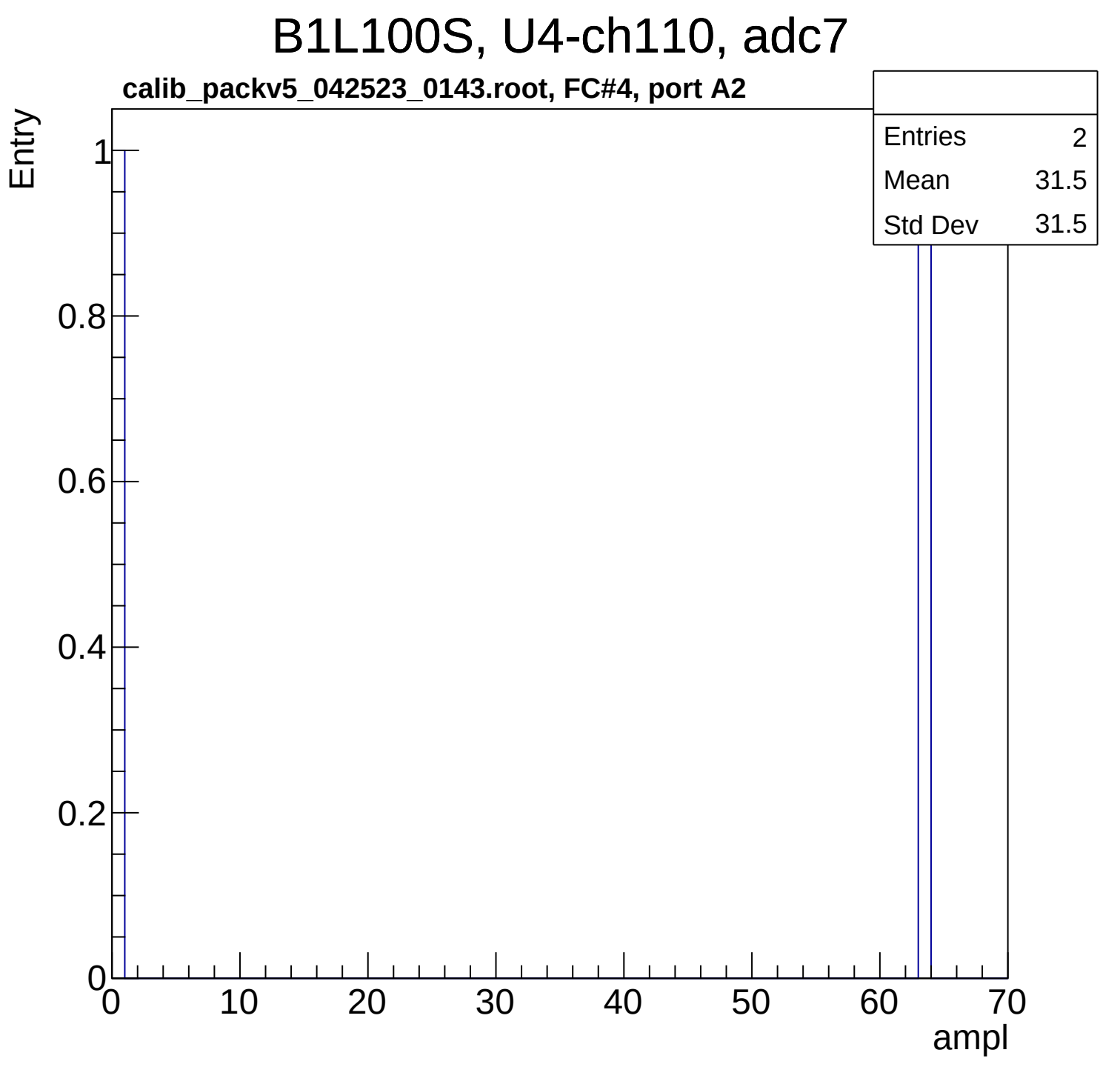

B1L100S, U4-ch110, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 42.91
Std Dev 3.241
Gaus mean : 43.3907
Gaus Width: 3.5725
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

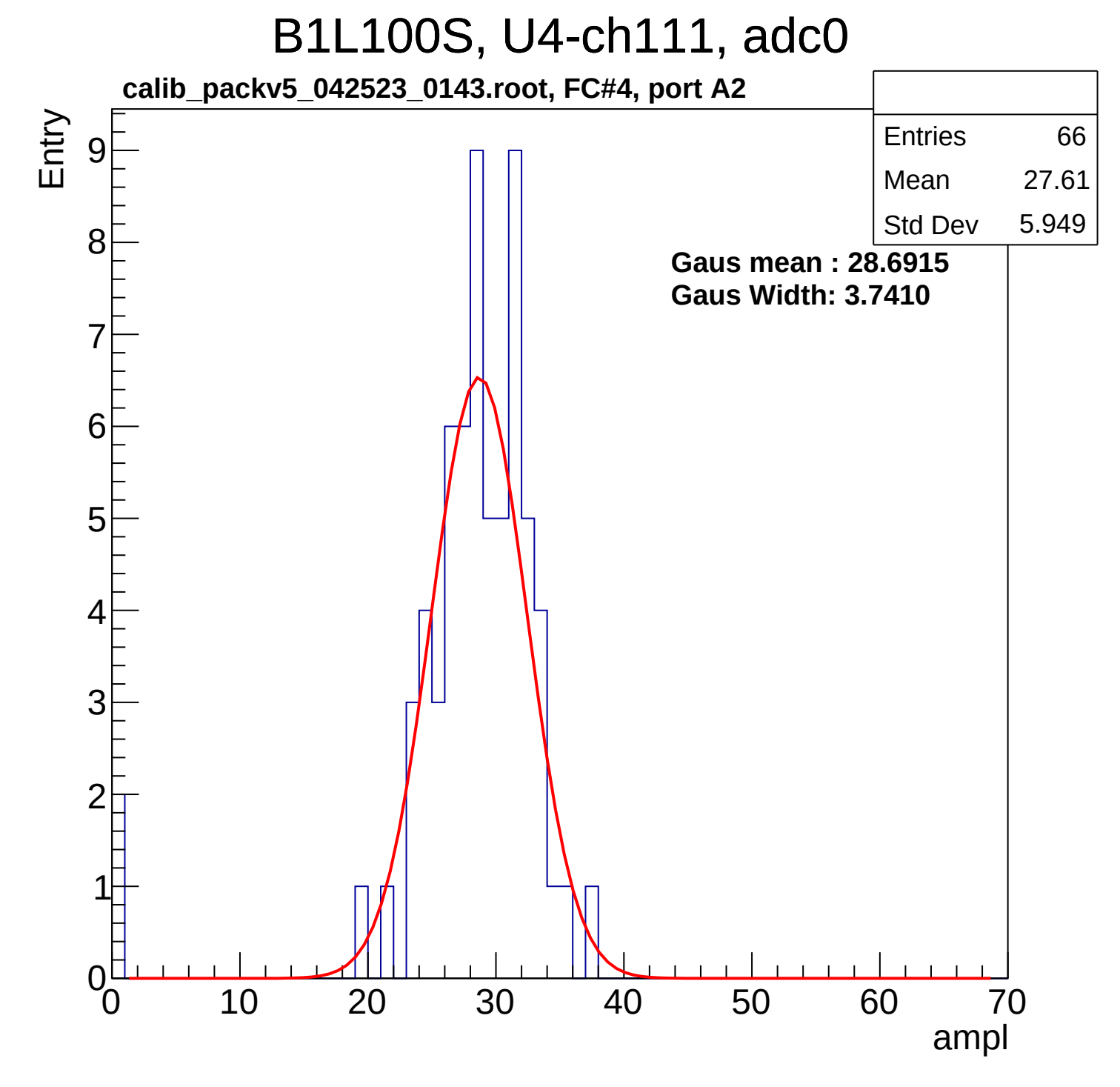

B1L100S, U4-ch110, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 48.45
Std Dev 3.479
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

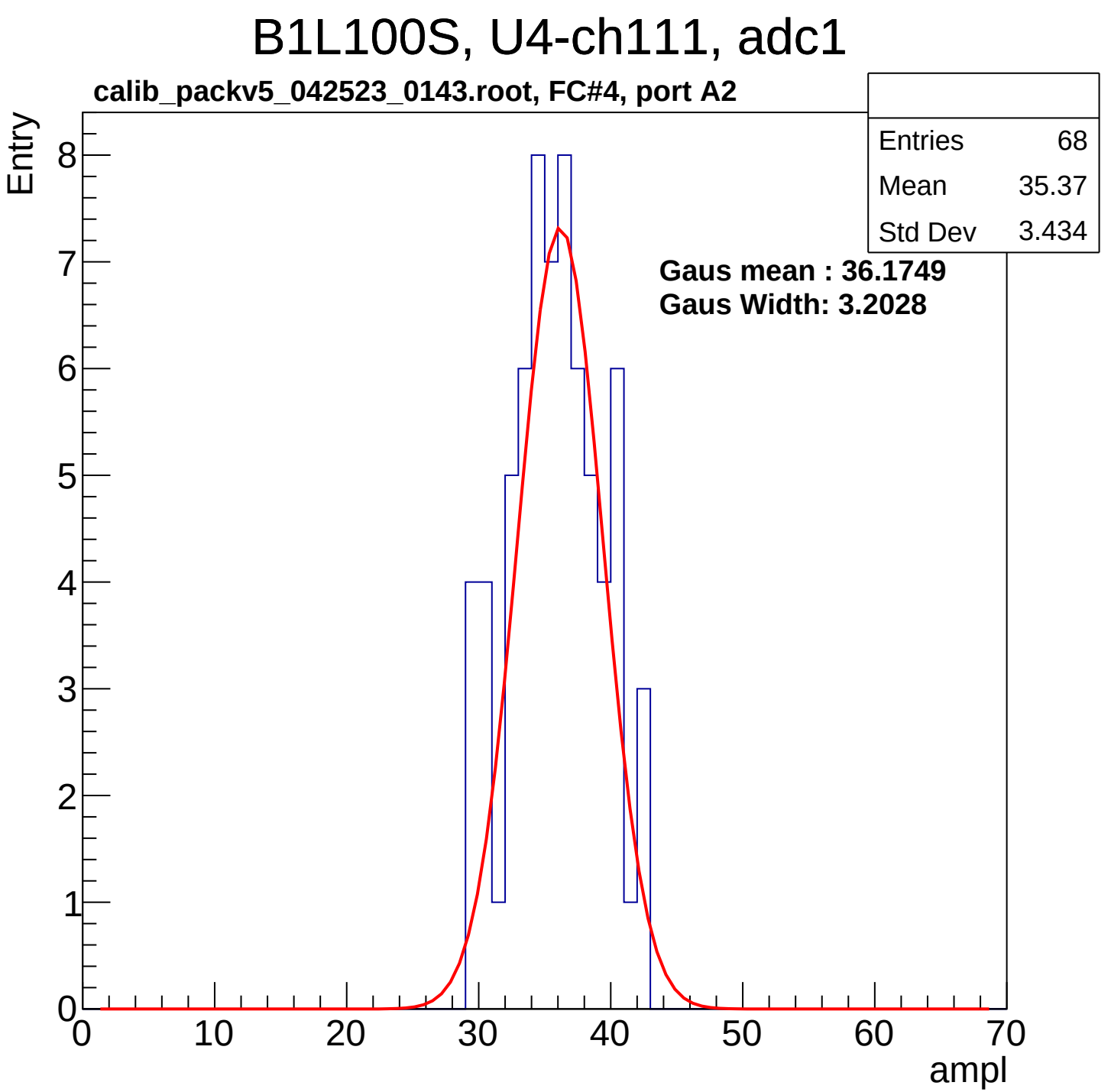

B1L100S, U4-ch110, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 53.36
Std Dev 7.792
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

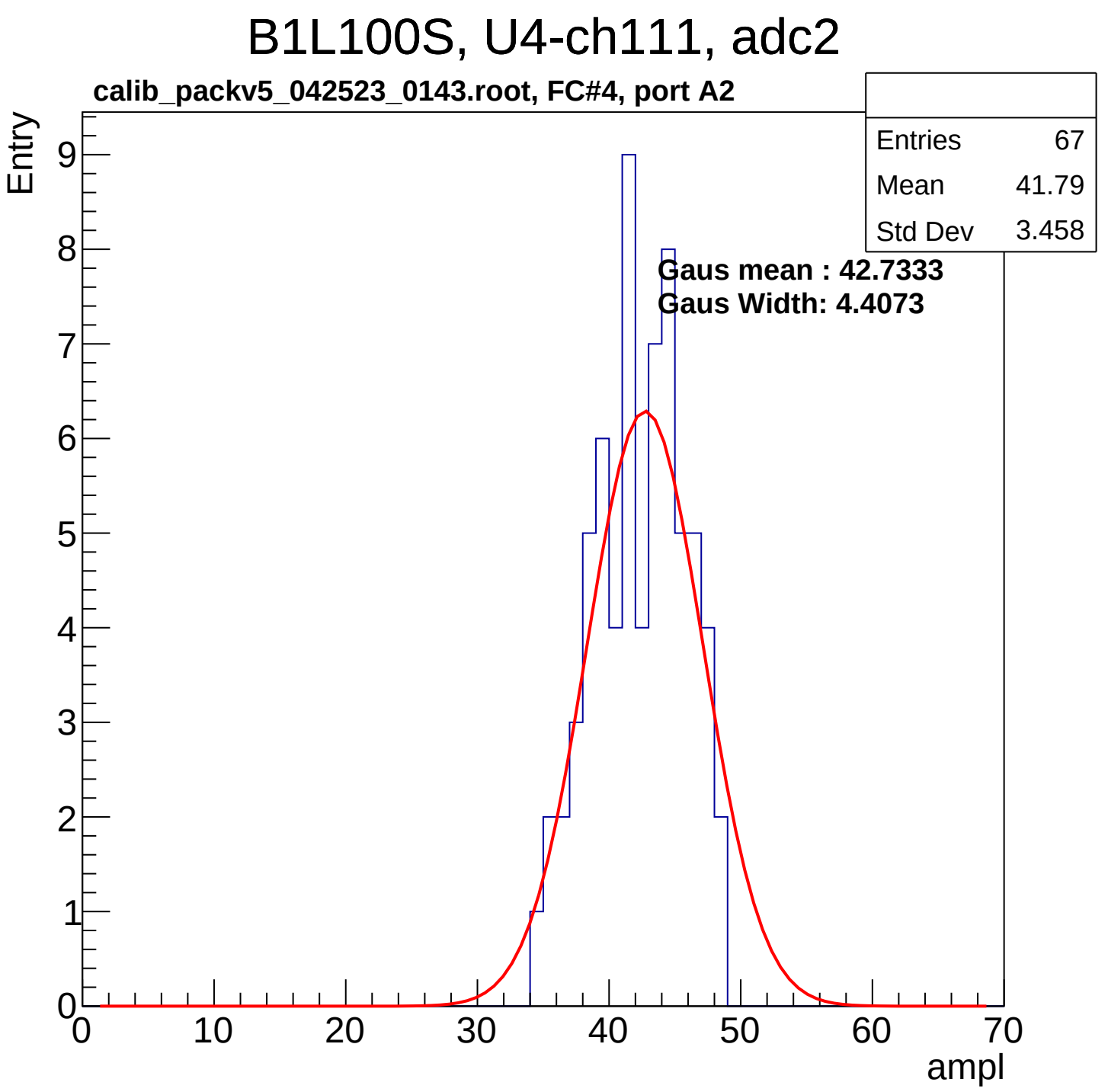

B1L100S, U4-ch110, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 59.1
Std Dev 2.651
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

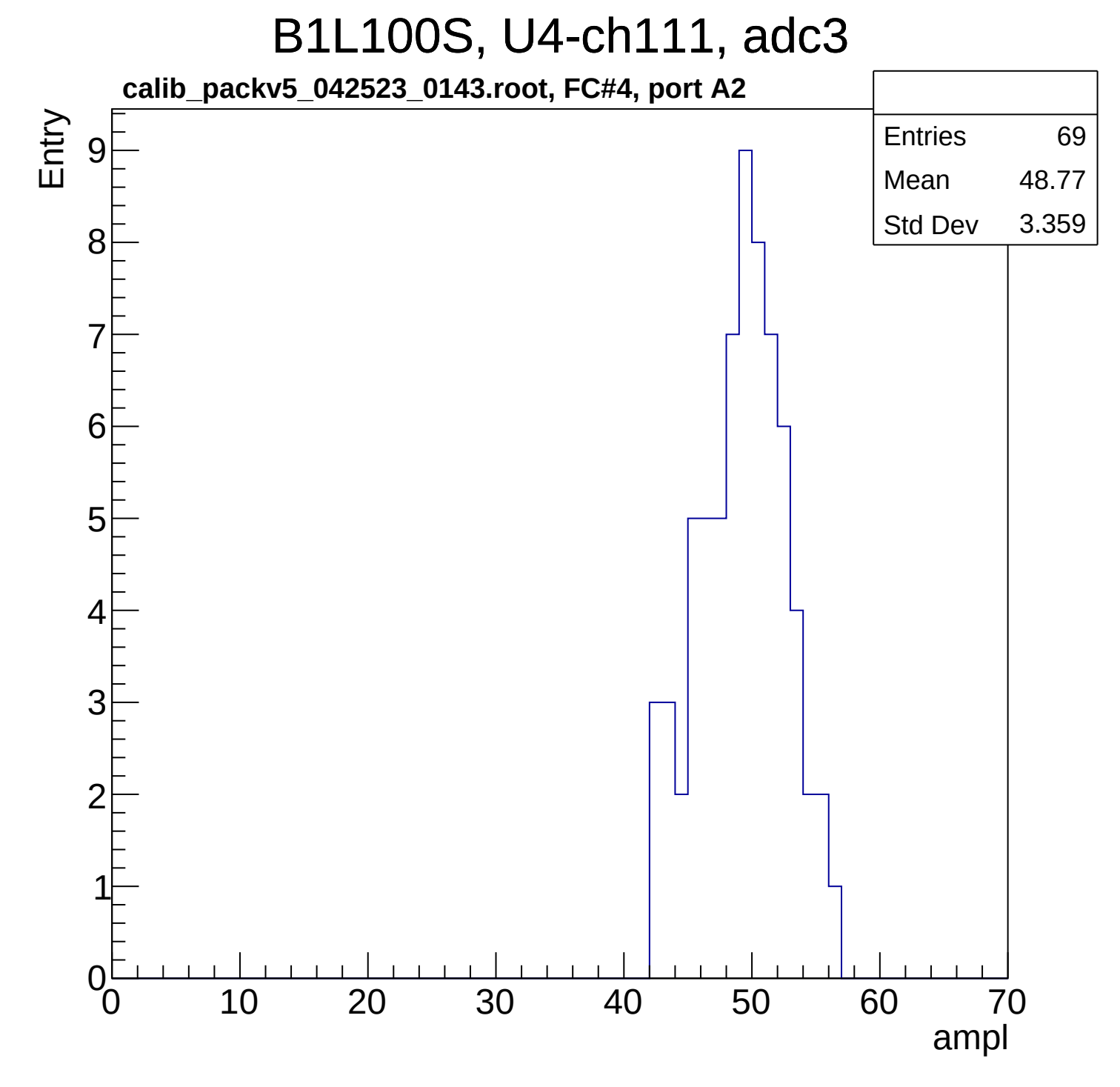

B1L100S, U4-ch110, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 12
Mean 61.67
Std Dev 1.247
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

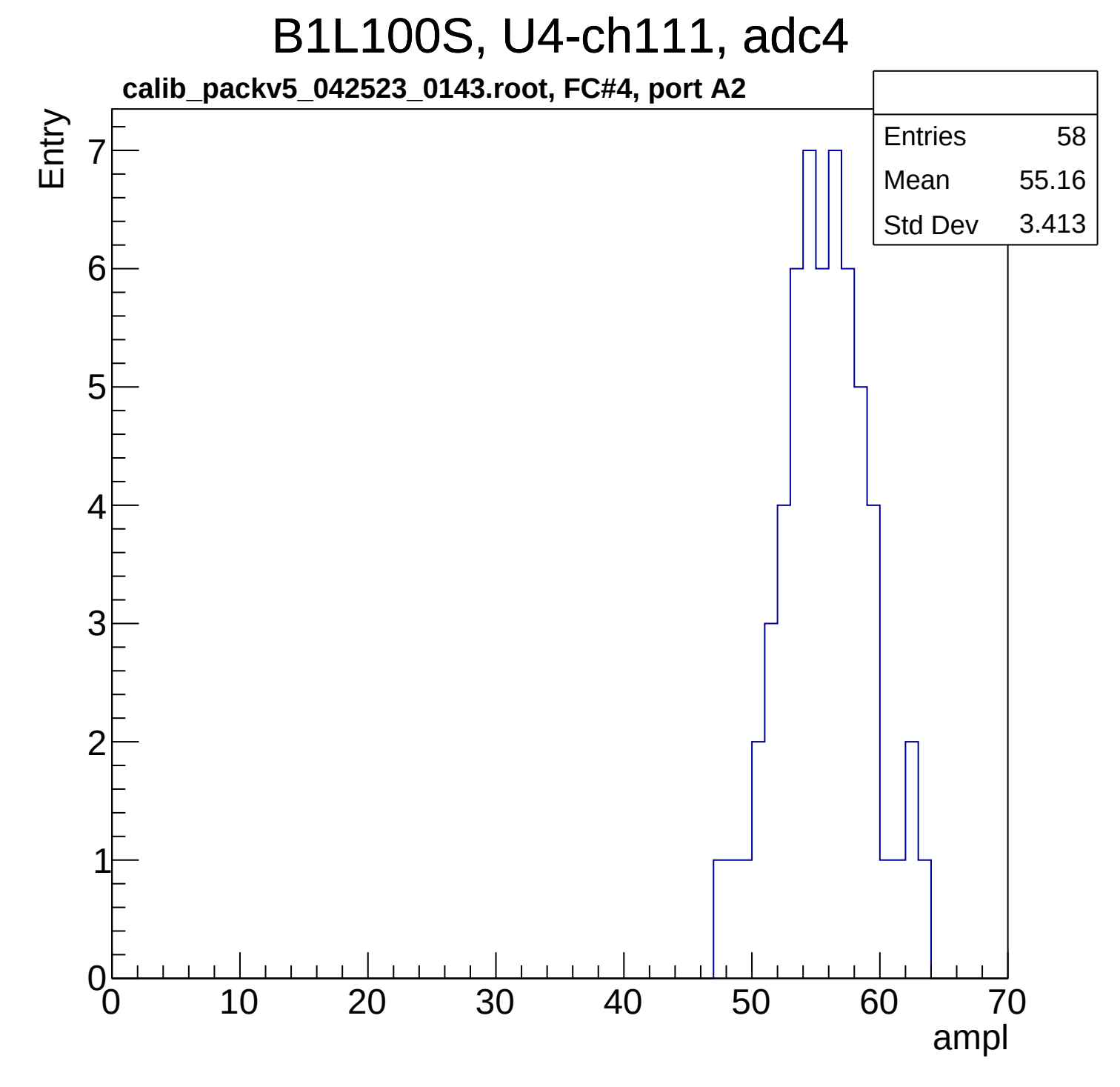

B1L100S, U4-ch110, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

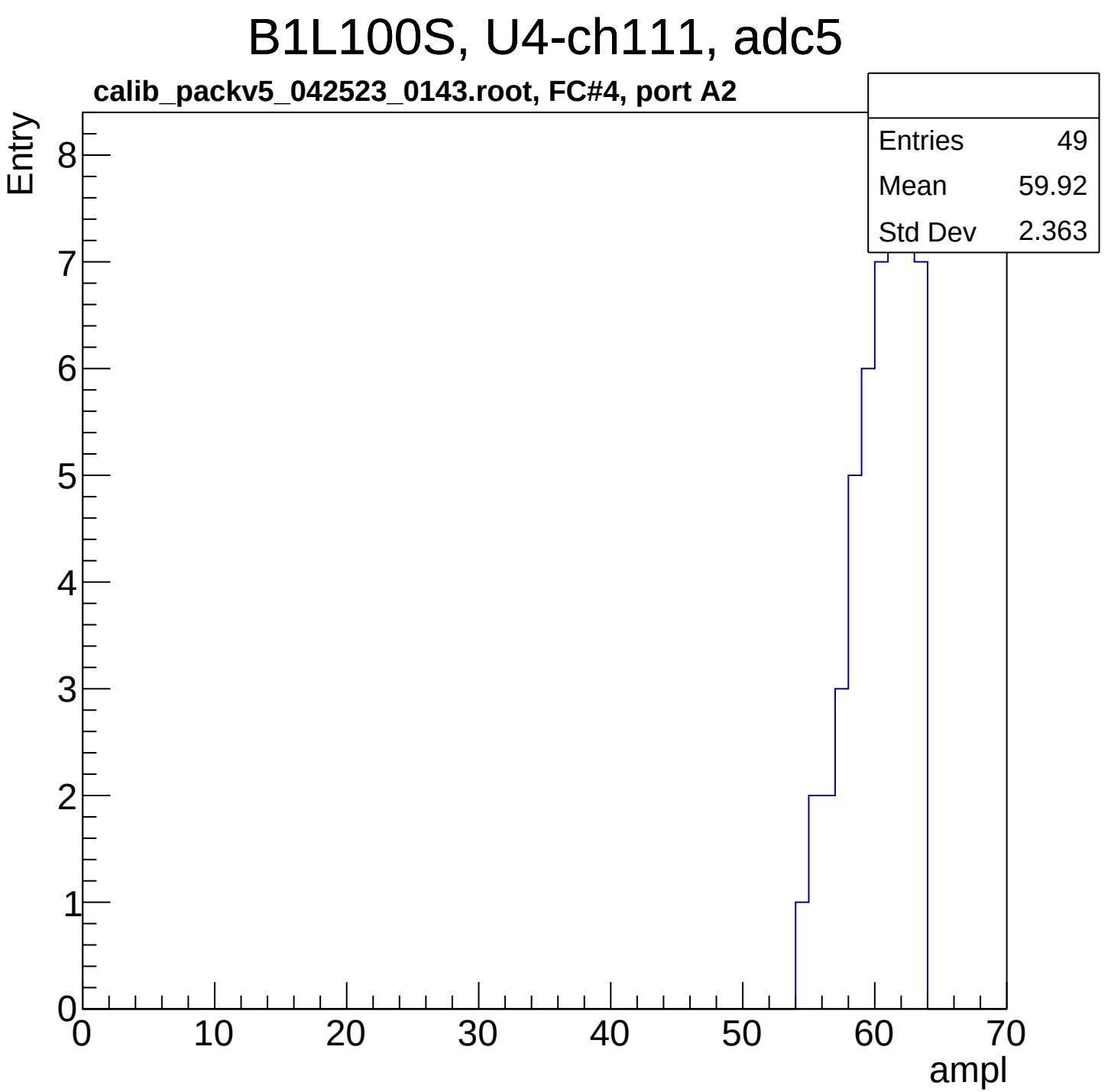

B1L100S, U4-ch111, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 27.61
Std Dev 5.949
Gaus mean : 28.6915
Gaus Width: 3.7410
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

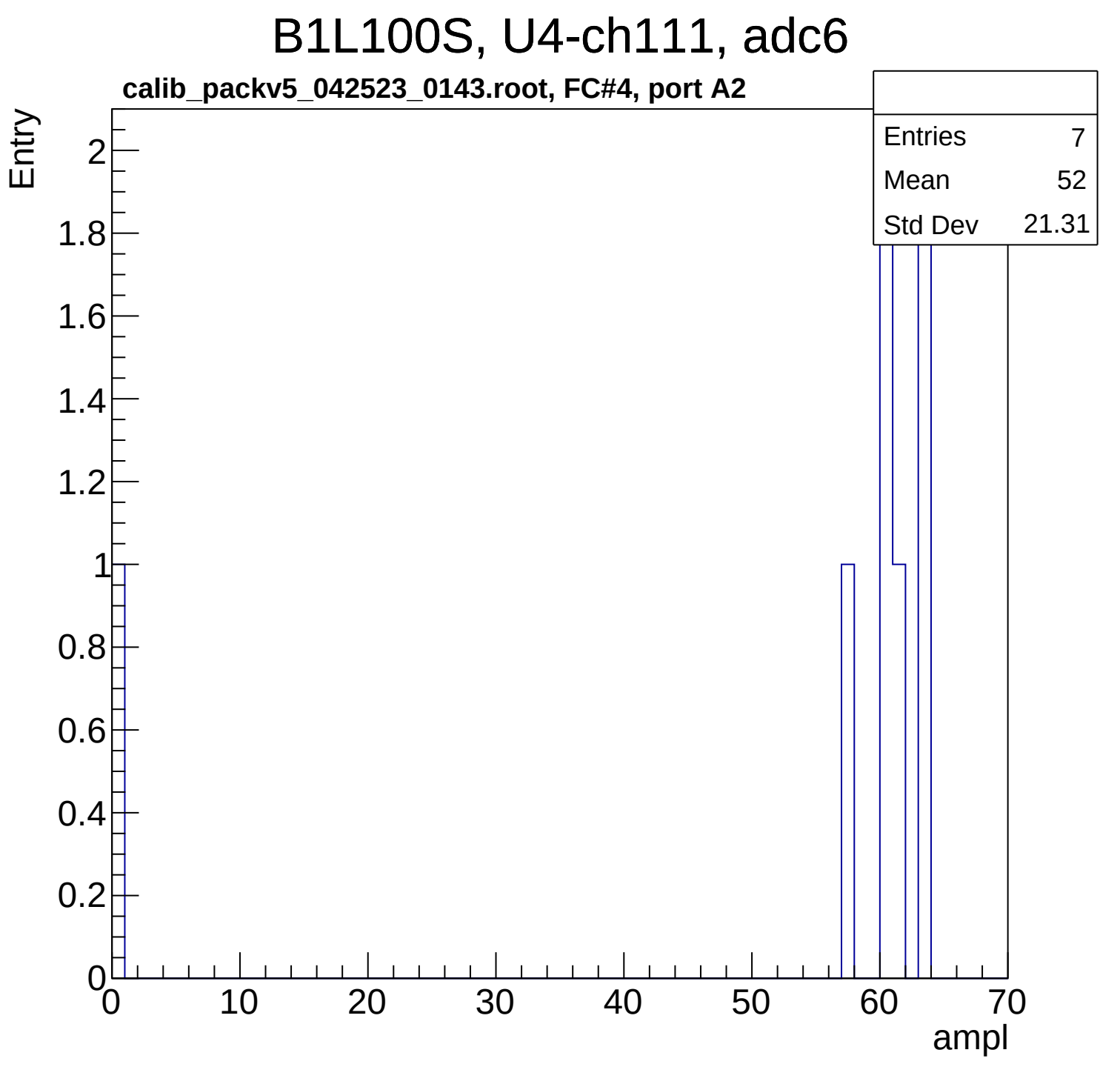

B1L100S, U4-ch111, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 35.37
Std Dev 3.434
Gaus mean : 36.1749
Gaus Width: 3.2028
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

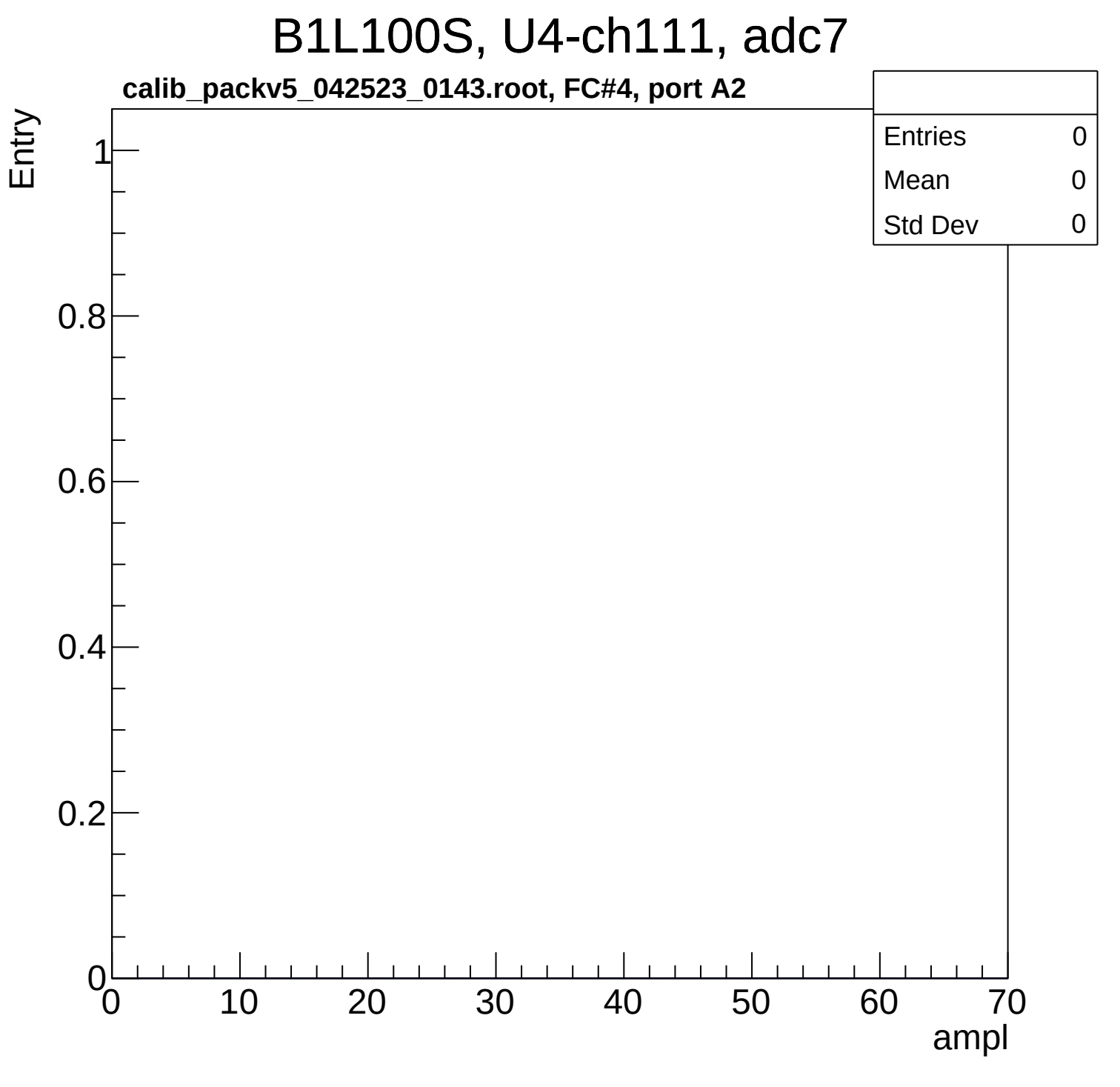

B1L100S, U4-ch111, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 41.79
Std Dev 3.458
Gaus mean : 42.7333
Gaus Width: 4.4073
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

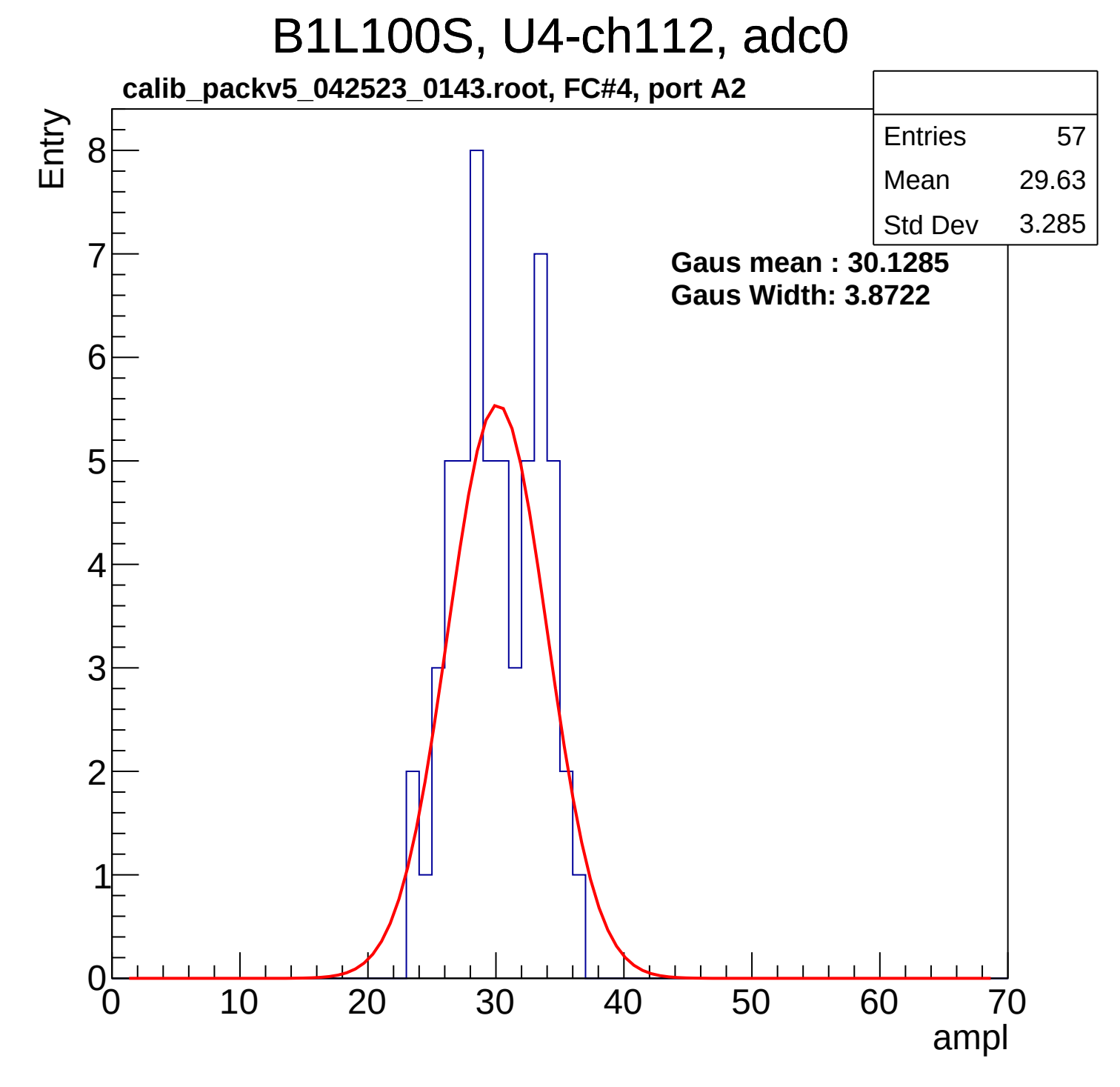

B1L100S, U4-ch111, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 48.77
Std Dev 3.359
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

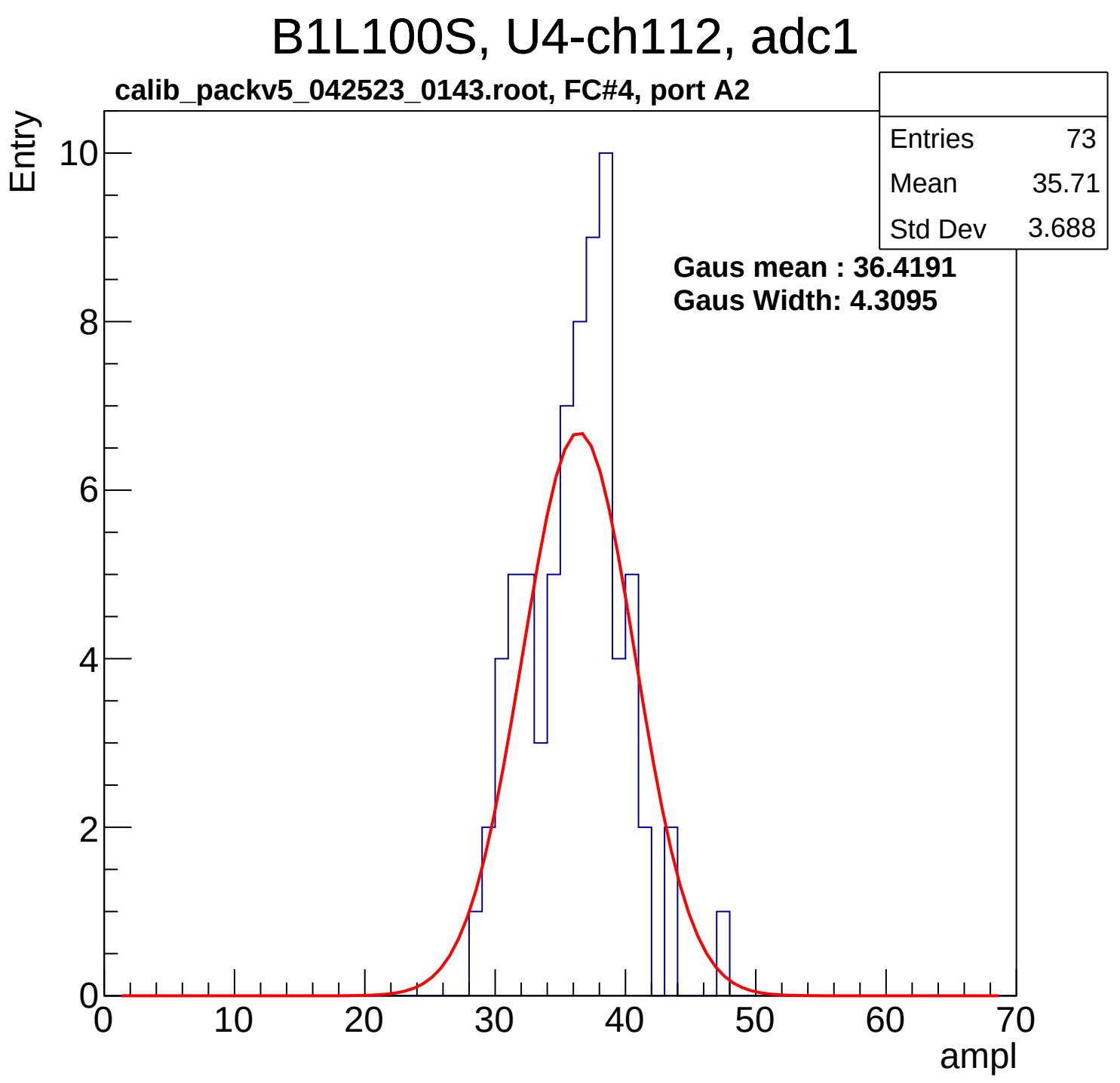

B1L100S, U4-ch111, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 55.16
Std Dev 3.413
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

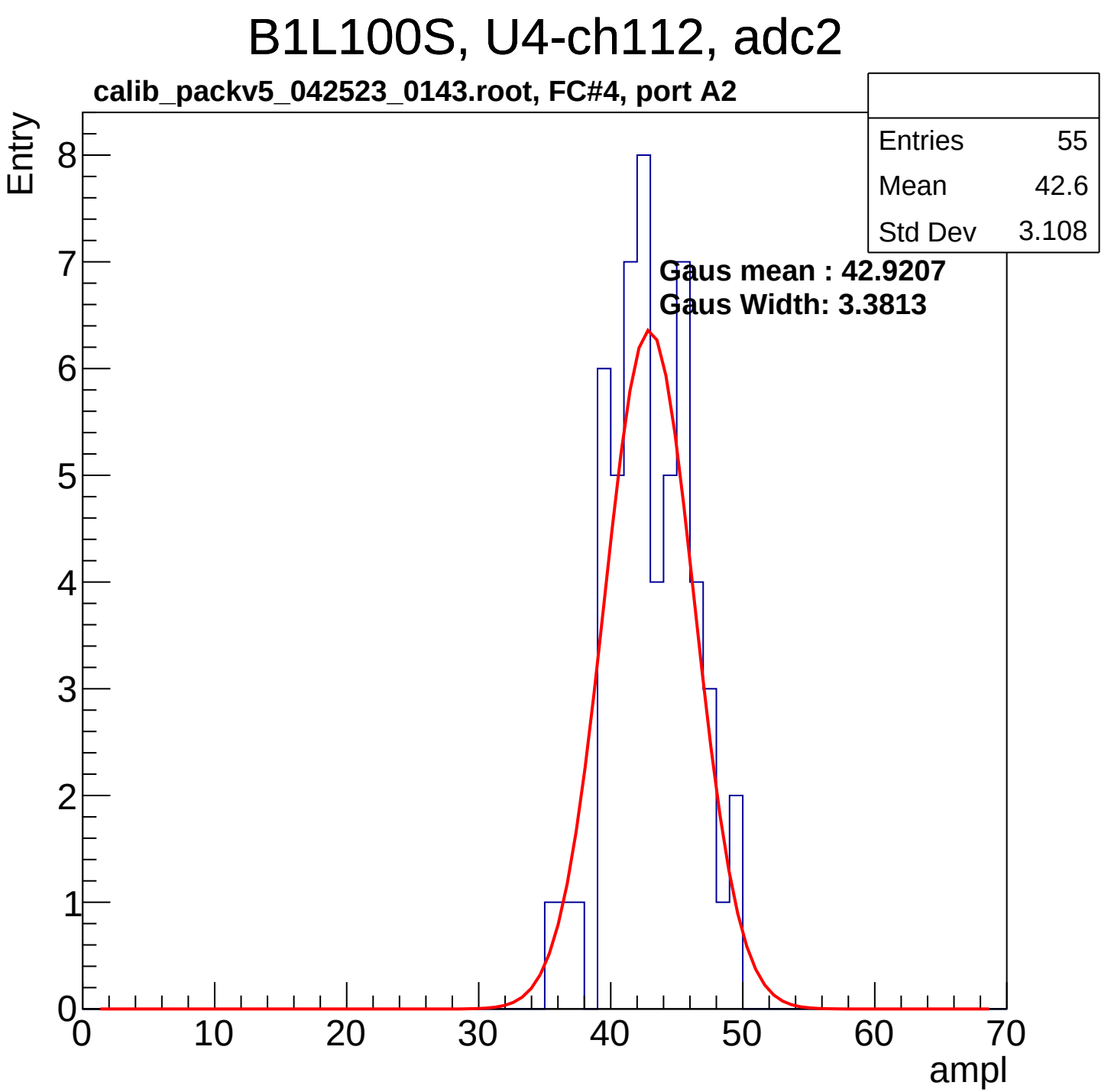

B1L100S, U4-ch111, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 59.92
Std Dev 2.363
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

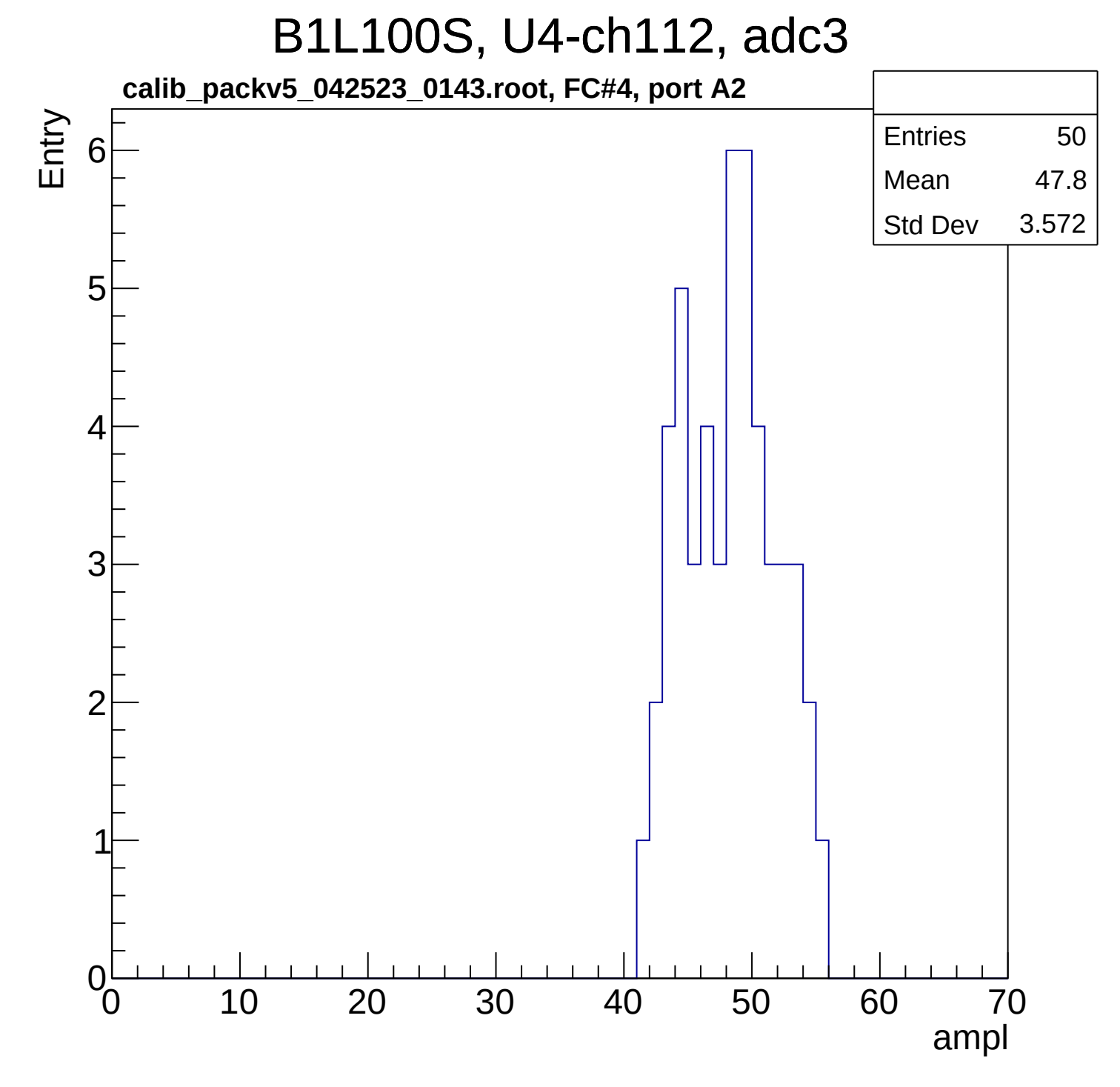

B1L100S, U4-ch111, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 52
Std Dev 21.31
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

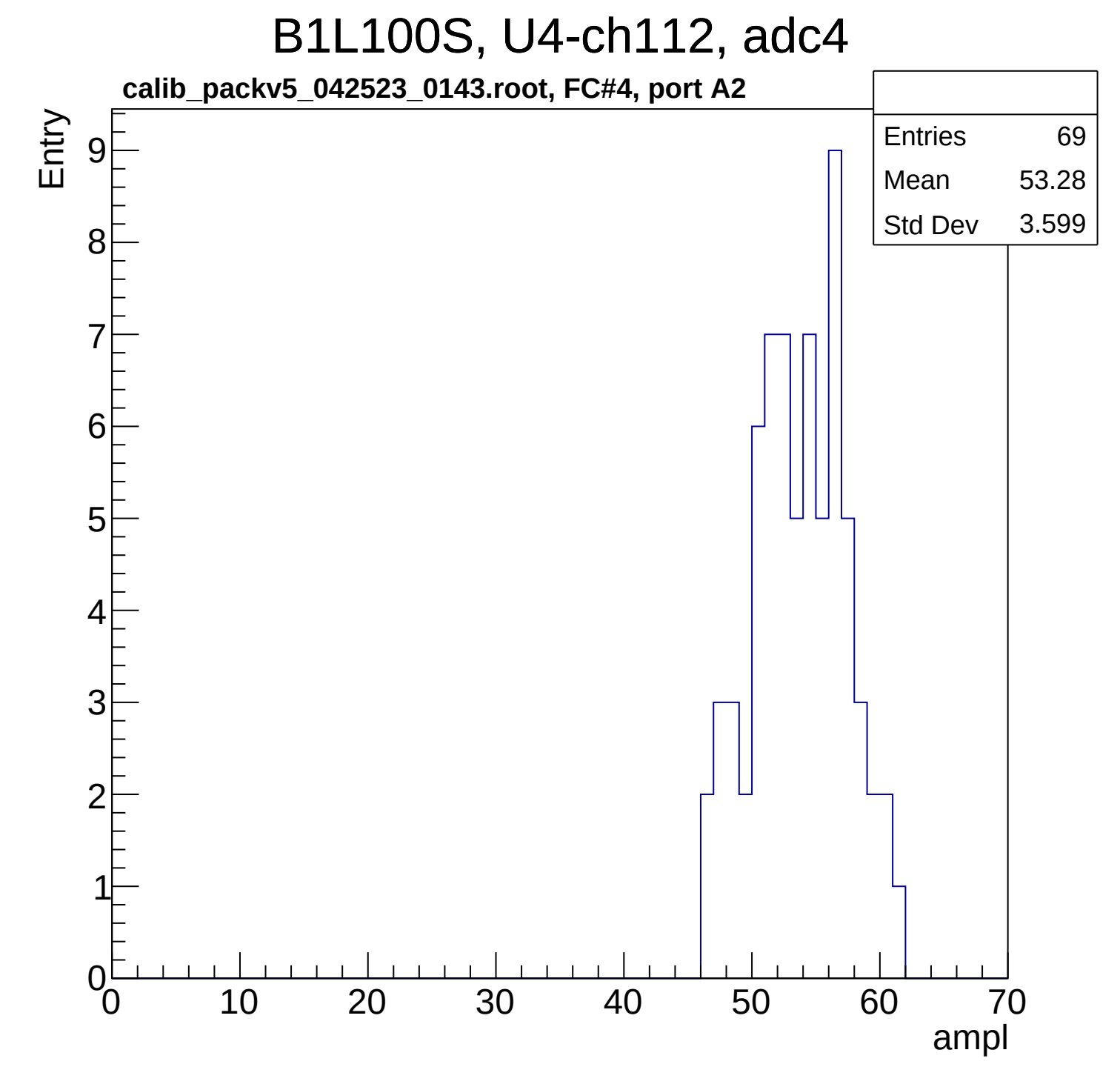

B1L100S, U4-ch111, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

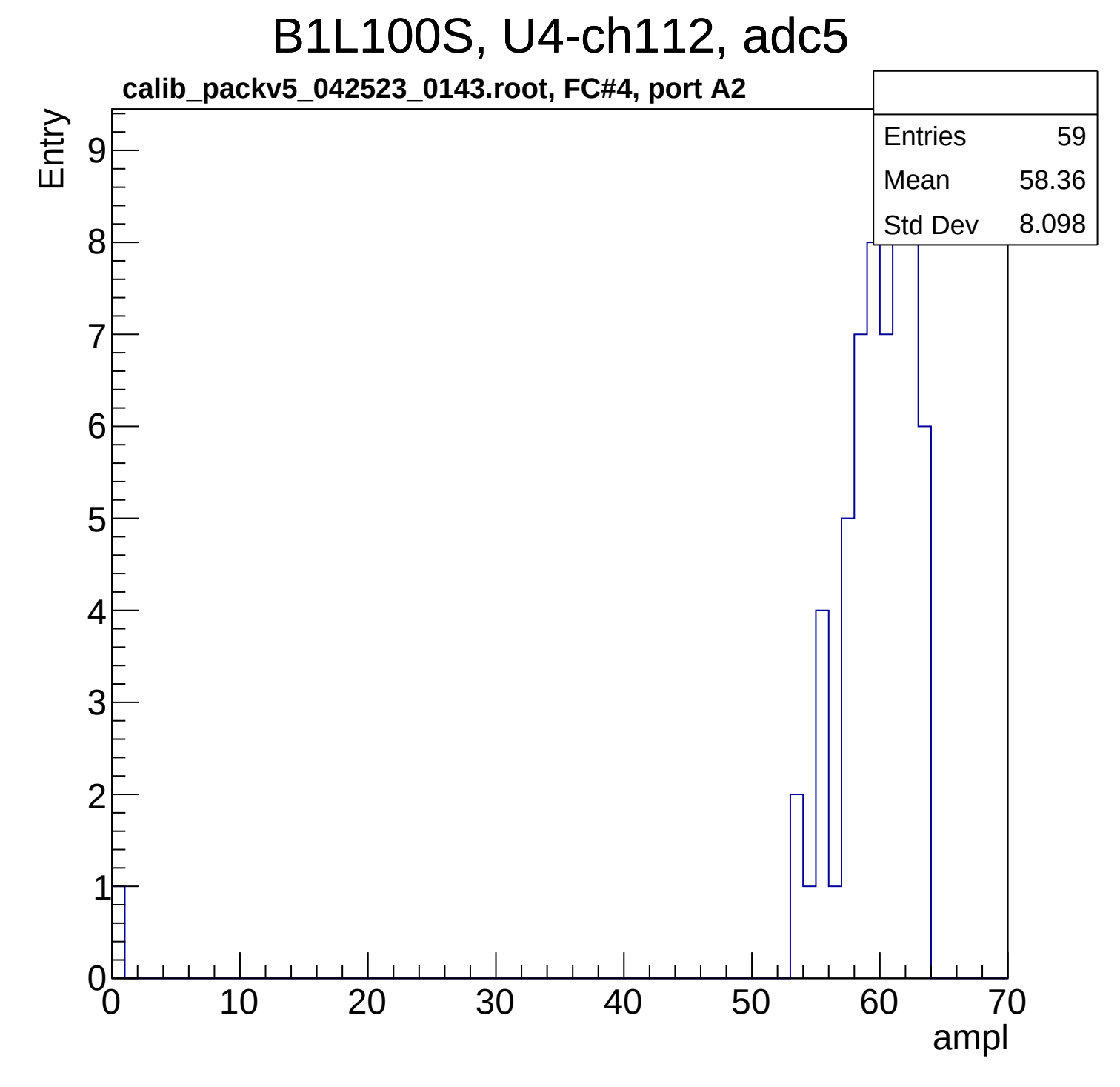

B1L100S, U4-ch112, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 29.63
Std Dev 3.285
Gaus mean : 30.1285
Gaus Width: 3.8722
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

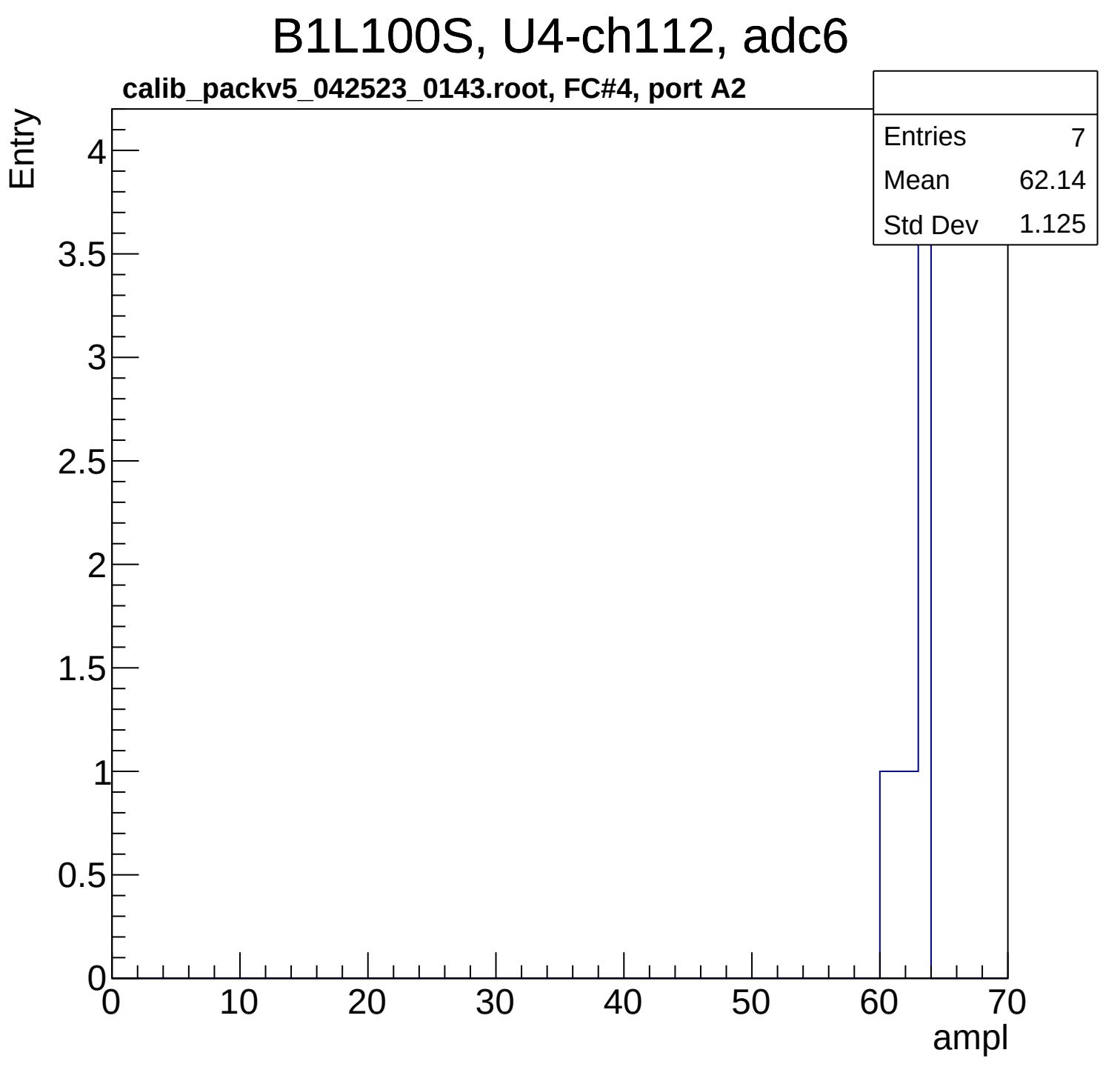

B1L100S, U4-ch112, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 35.71
Std Dev 3.688
Gaus mean : 36.4191
Gaus Width: 4.3095
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

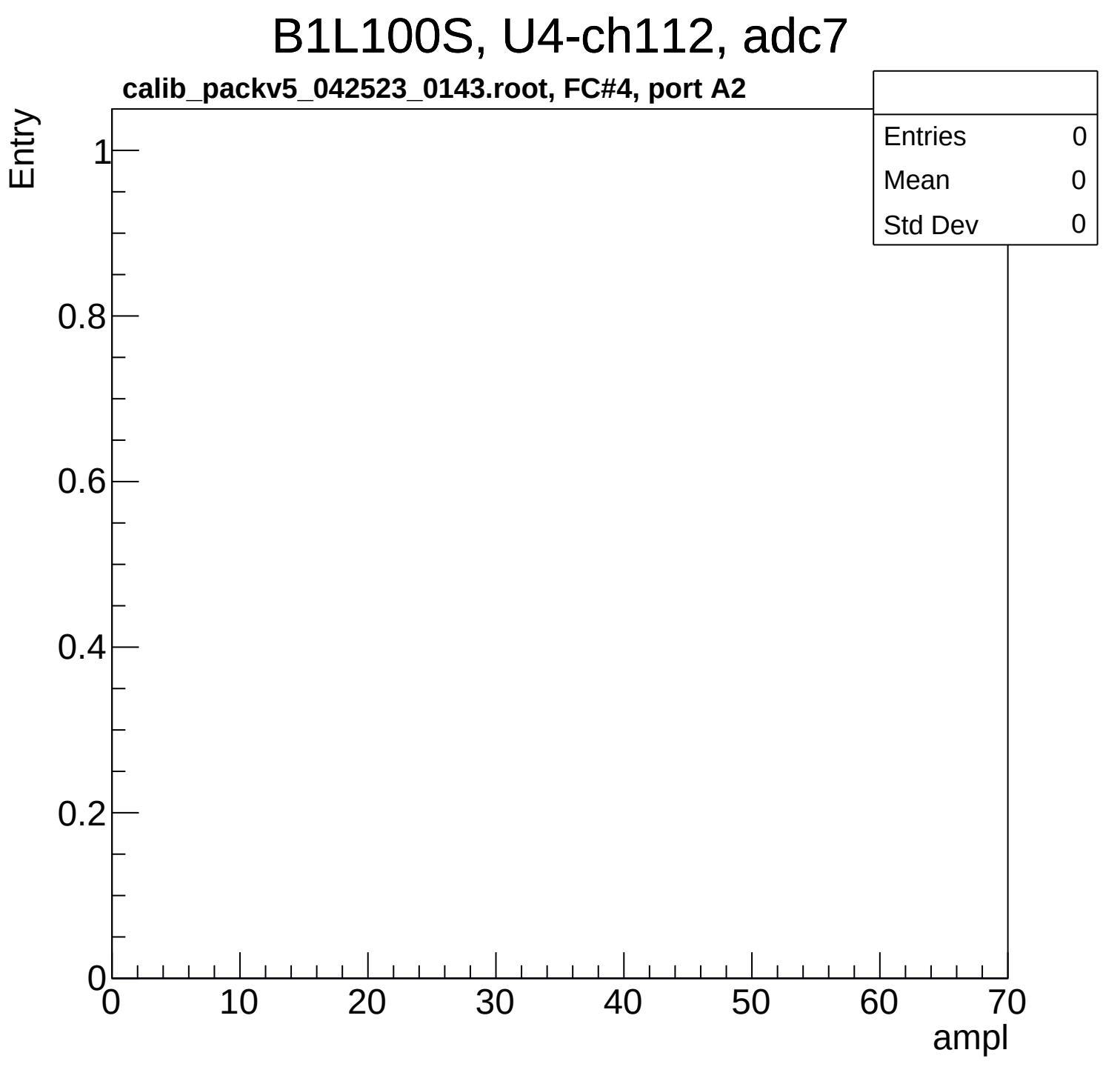

B1L100S, U4-ch112, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 42.6
Std Dev 3.108
Gaus mean : 42.9207
Gaus Width: 3.3813
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

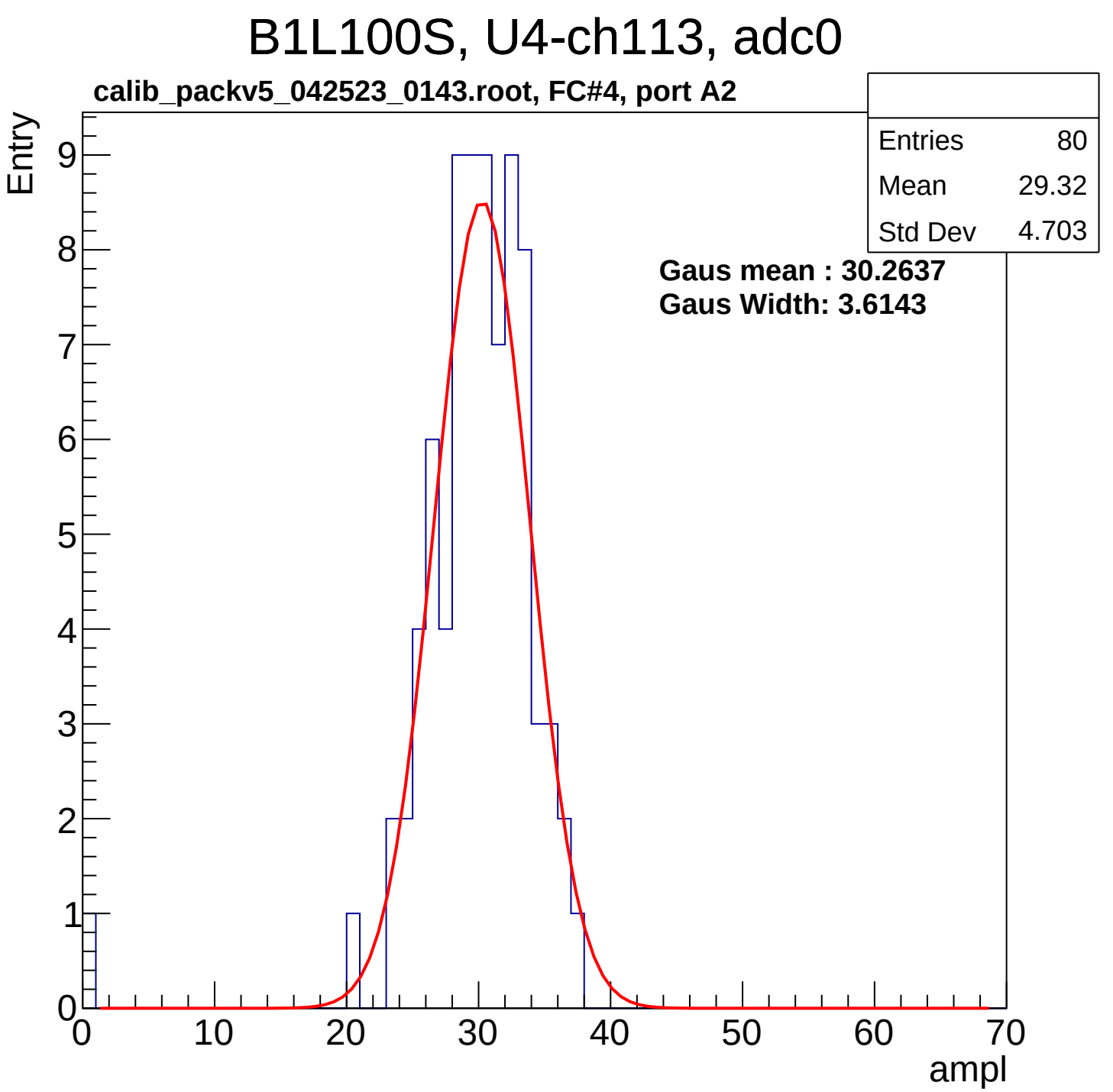

B1L100S, U4-ch112, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 47.8
Std Dev 3.572
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

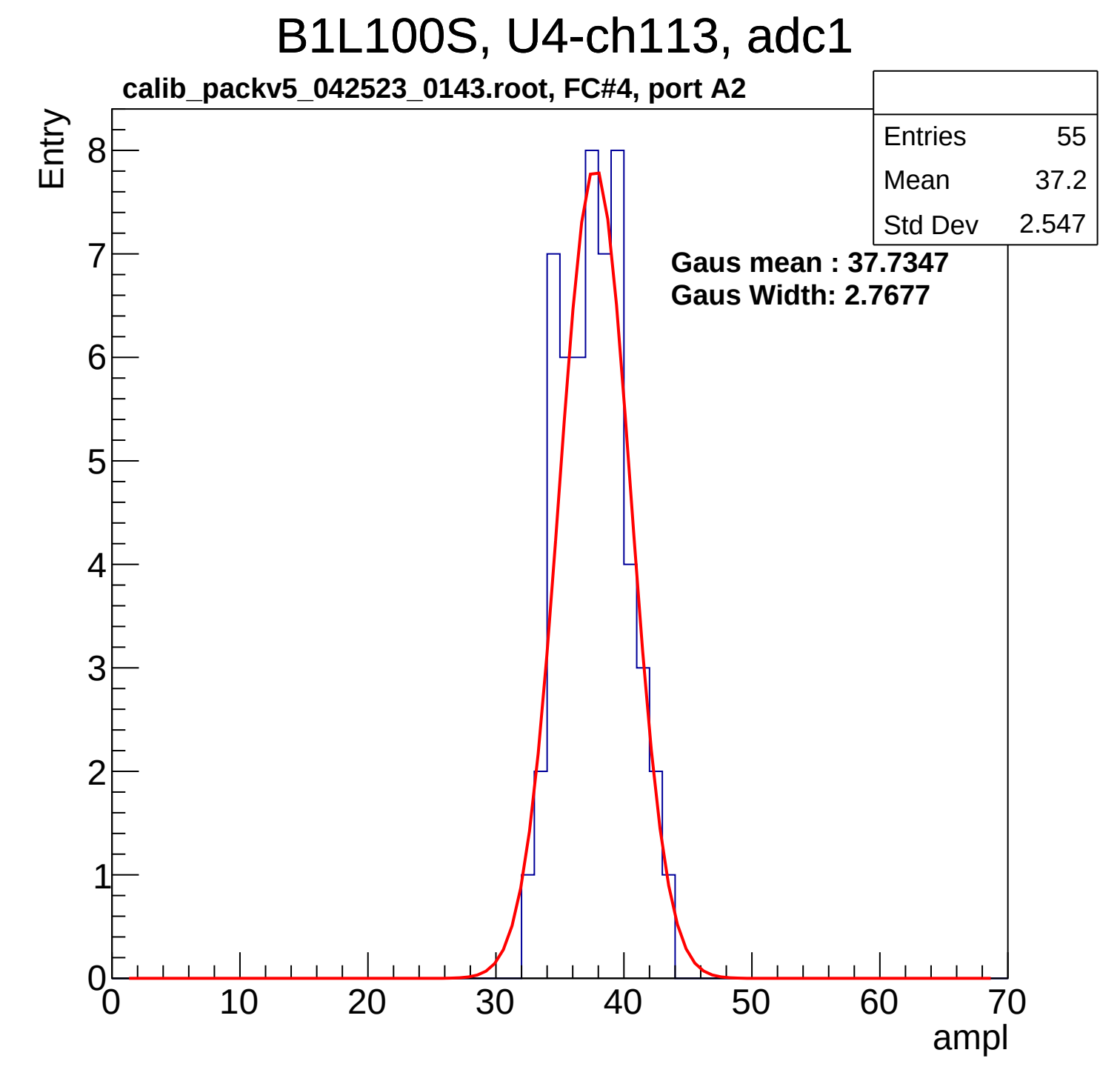

B1L100S, U4-ch112, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 53.28
Std Dev 3.599
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

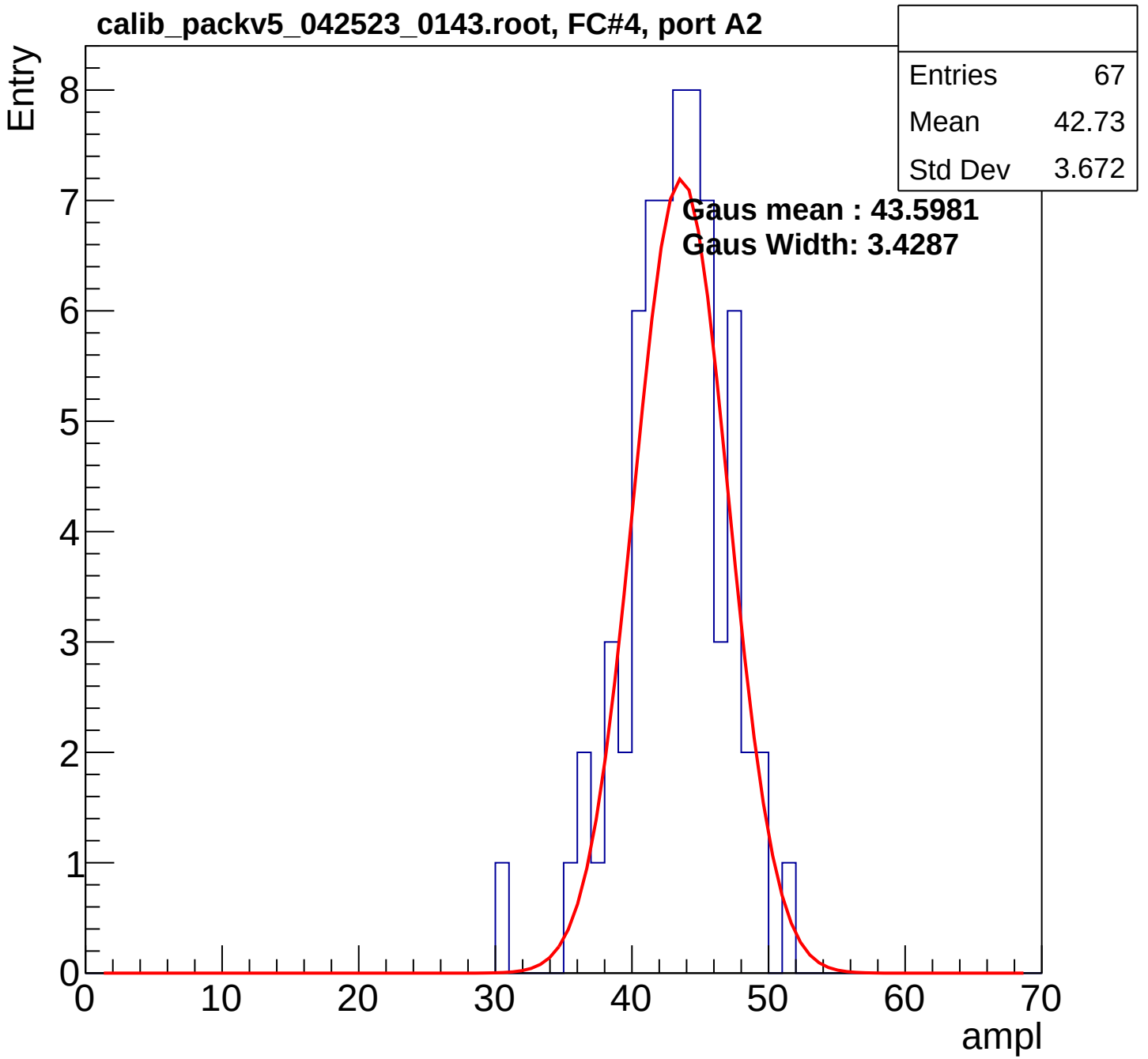

B1L100S, U4-ch112, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 58.36
Std Dev 8.098
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

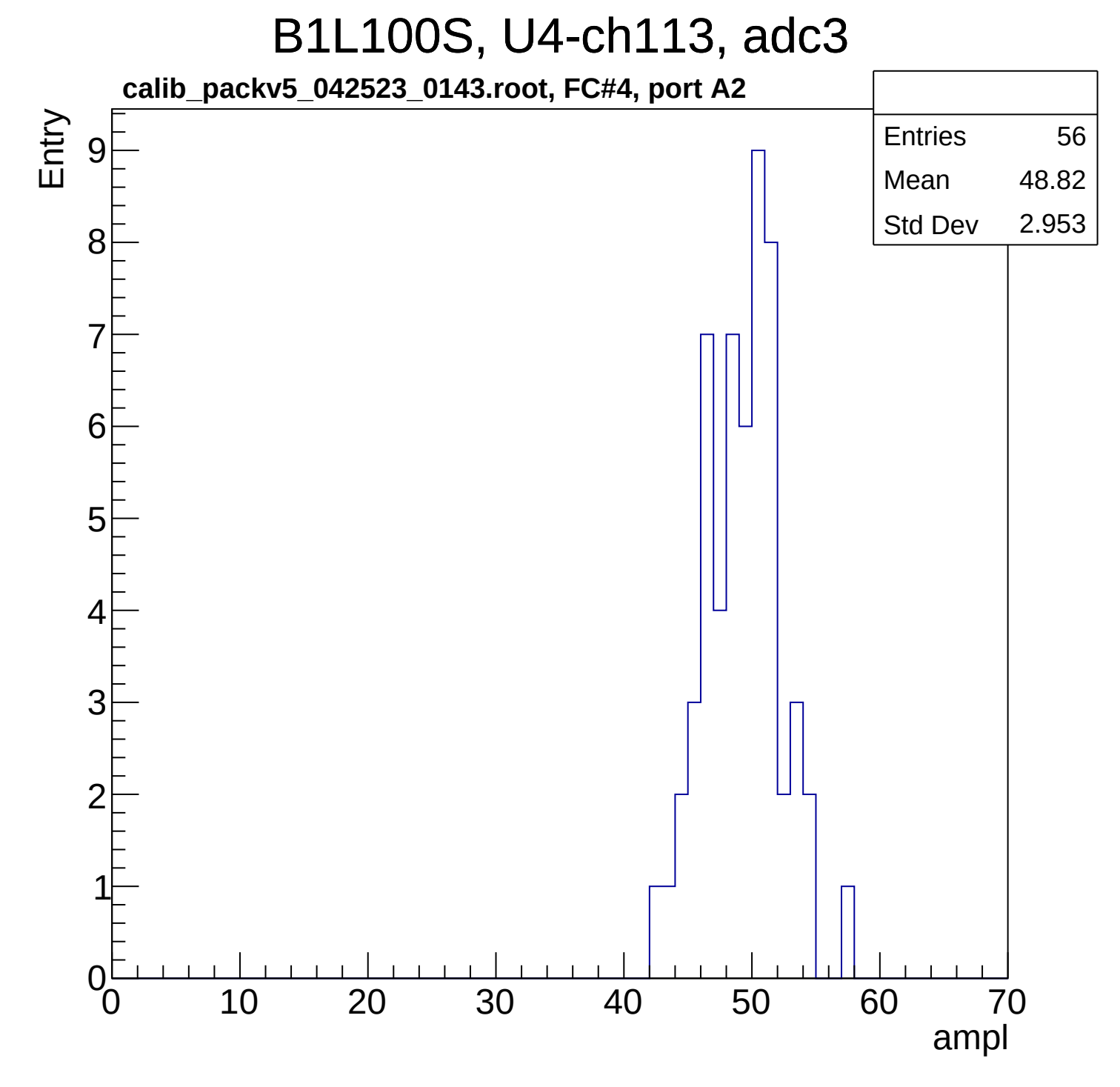

B1L100S, U4-ch112, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 62.14
Std Dev 1.125
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

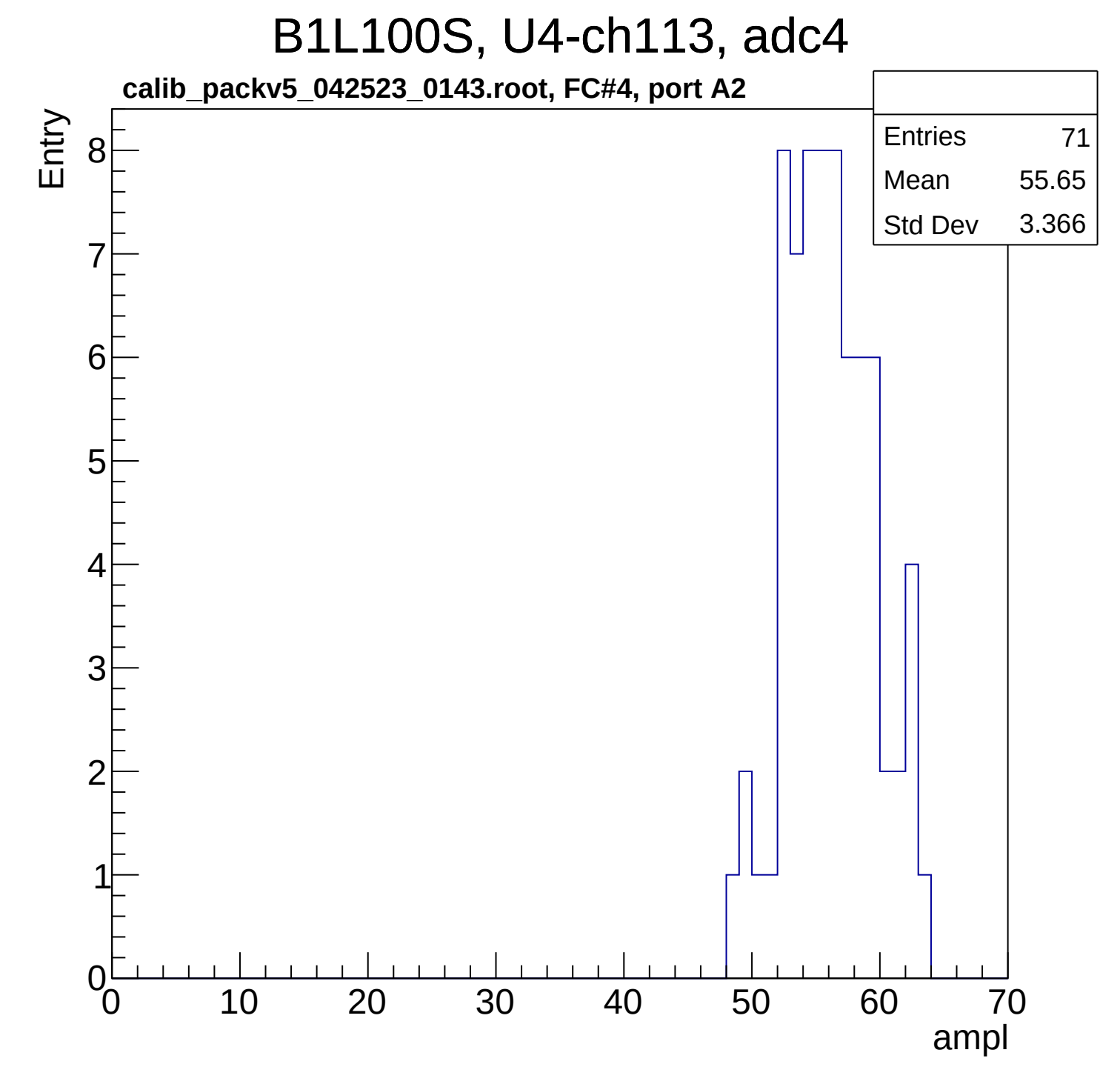

B1L100S, U4-ch112, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

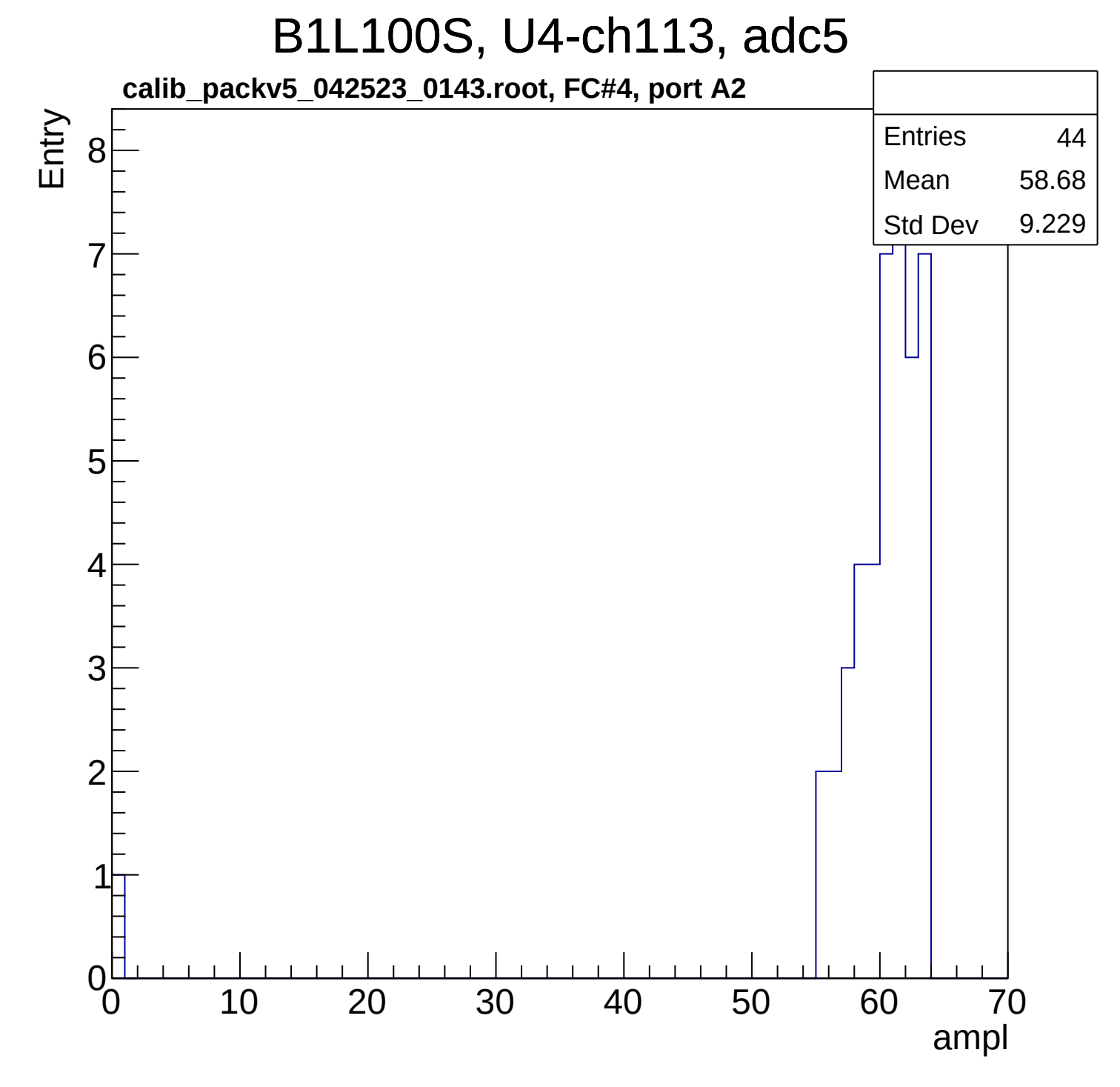

B1L100S, U4-ch113, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 29.32
Std Dev 4.703
Gaus mean : 30.2637
Gaus Width: 3.6143
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

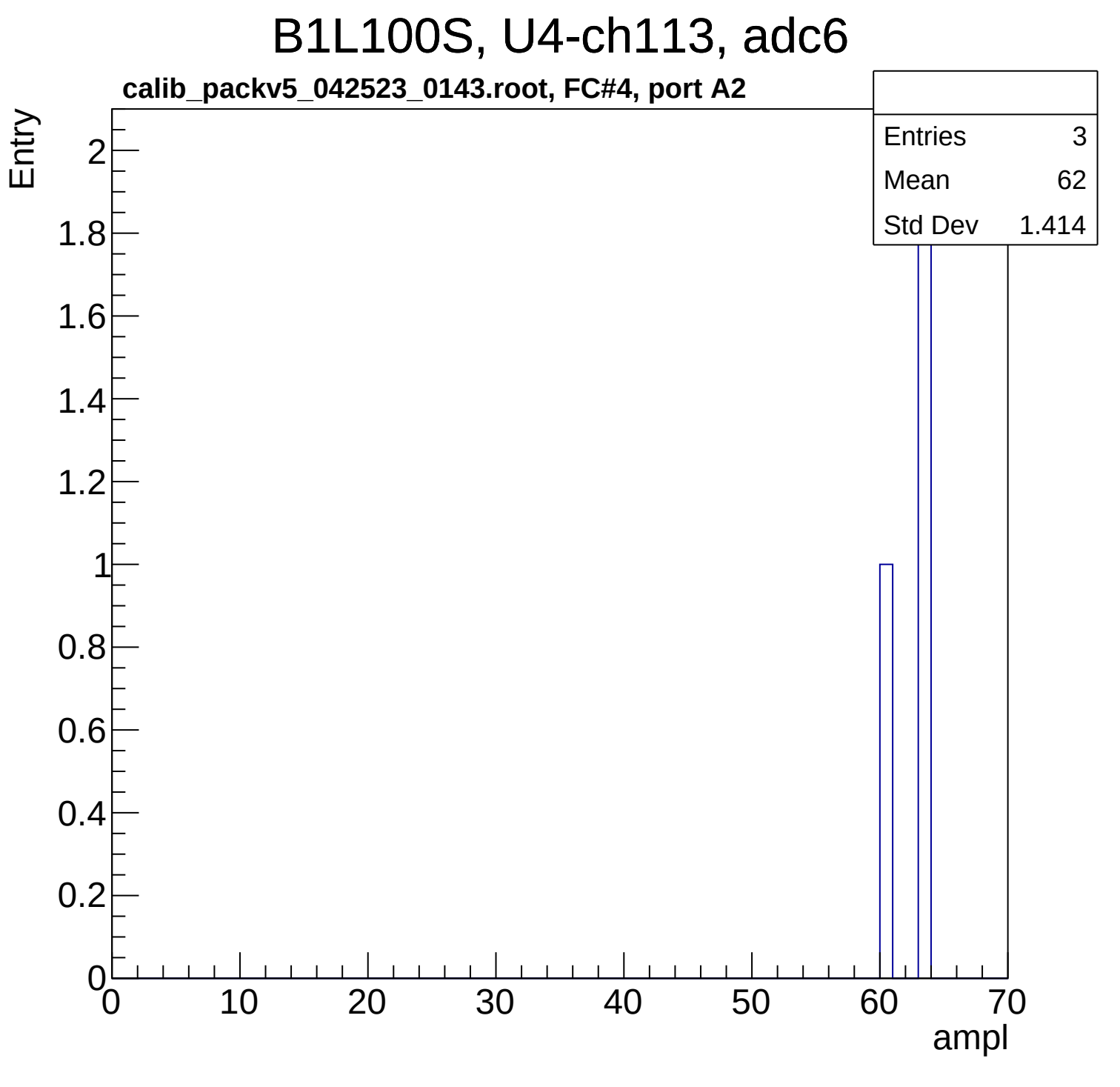

B1L100S, U4-ch113, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 37.2
Std Dev 2.547
Gaus mean : 37.7347
Gaus Width: 2.7677
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

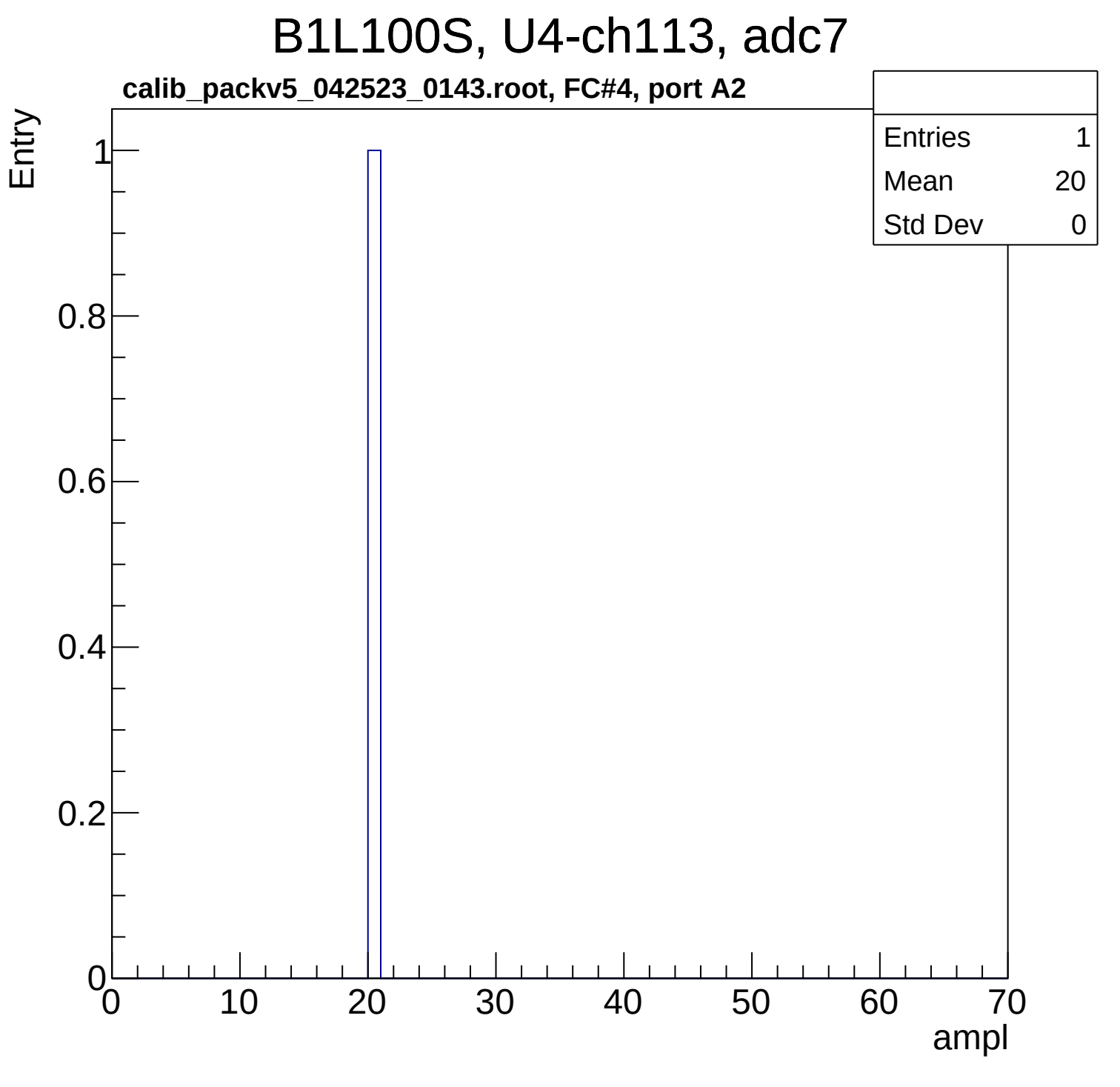

B1L100S, U4-ch113, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 42.73
Std Dev 3.672
Gaus mean : 43.5981
Gaus Width: 3.4287
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

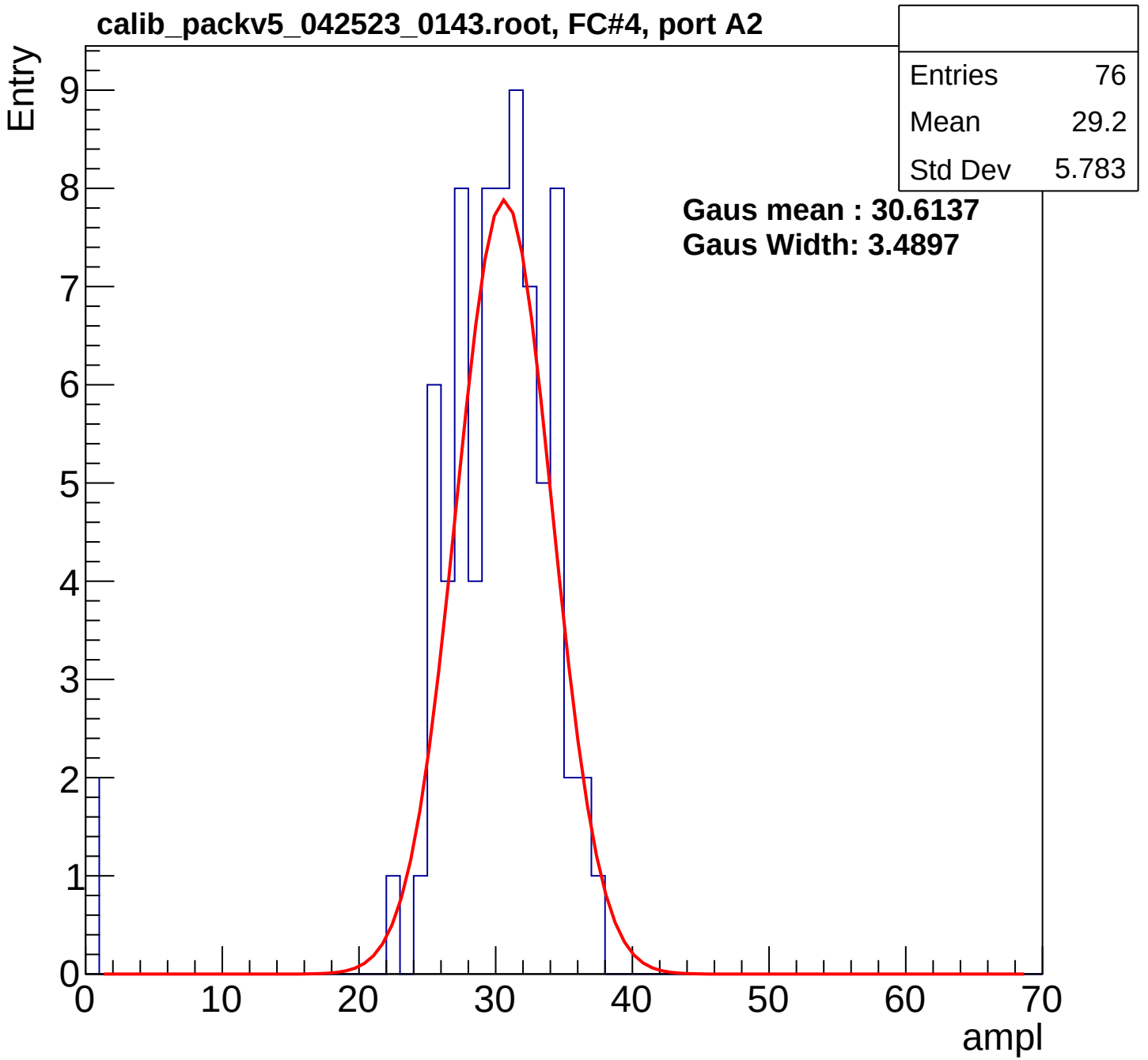

B1L100S, U4-ch113, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 48.82
Std Dev 2.953
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

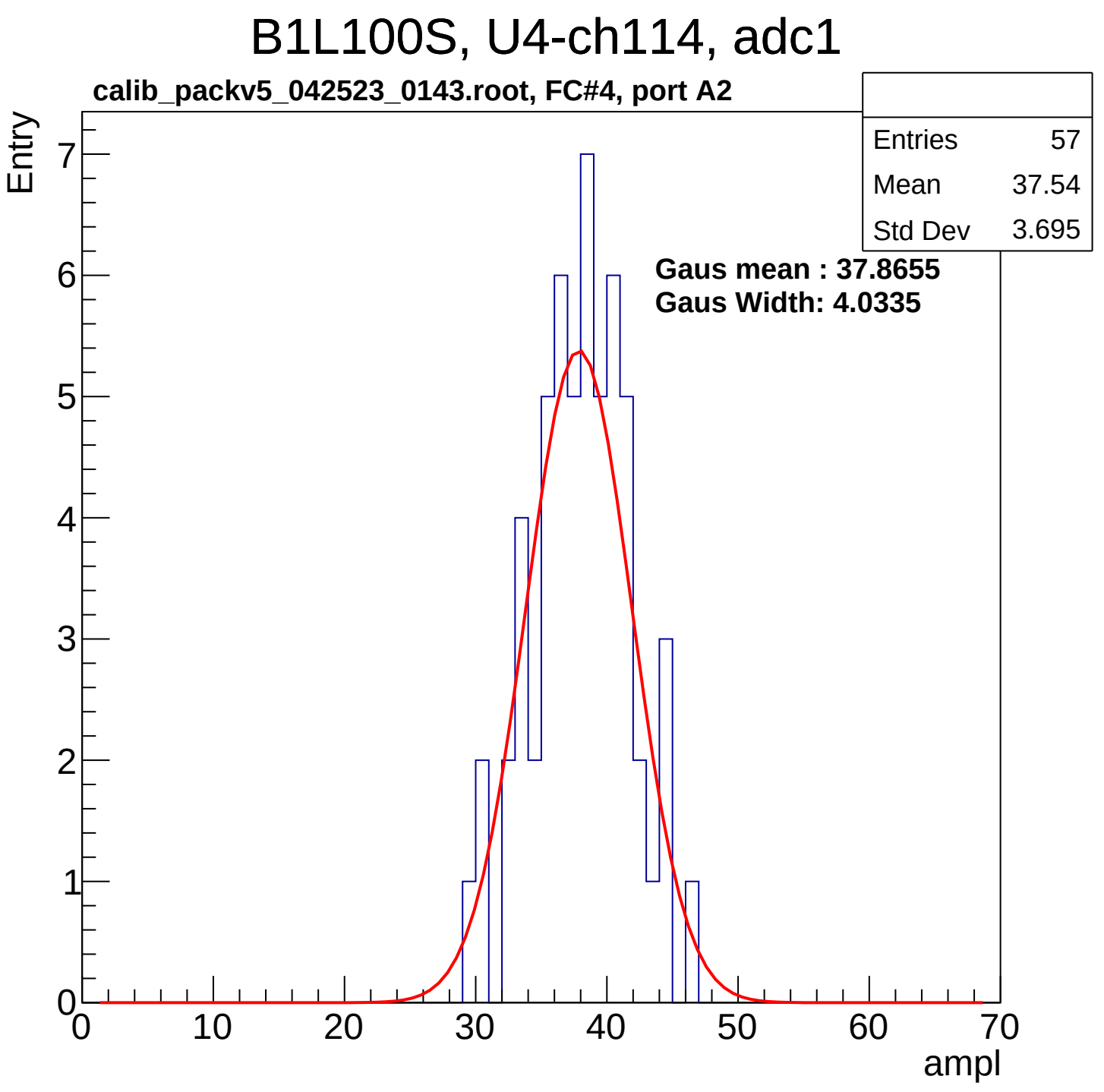

B1L100S, U4-ch113, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 55.65
Std Dev 3.366
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

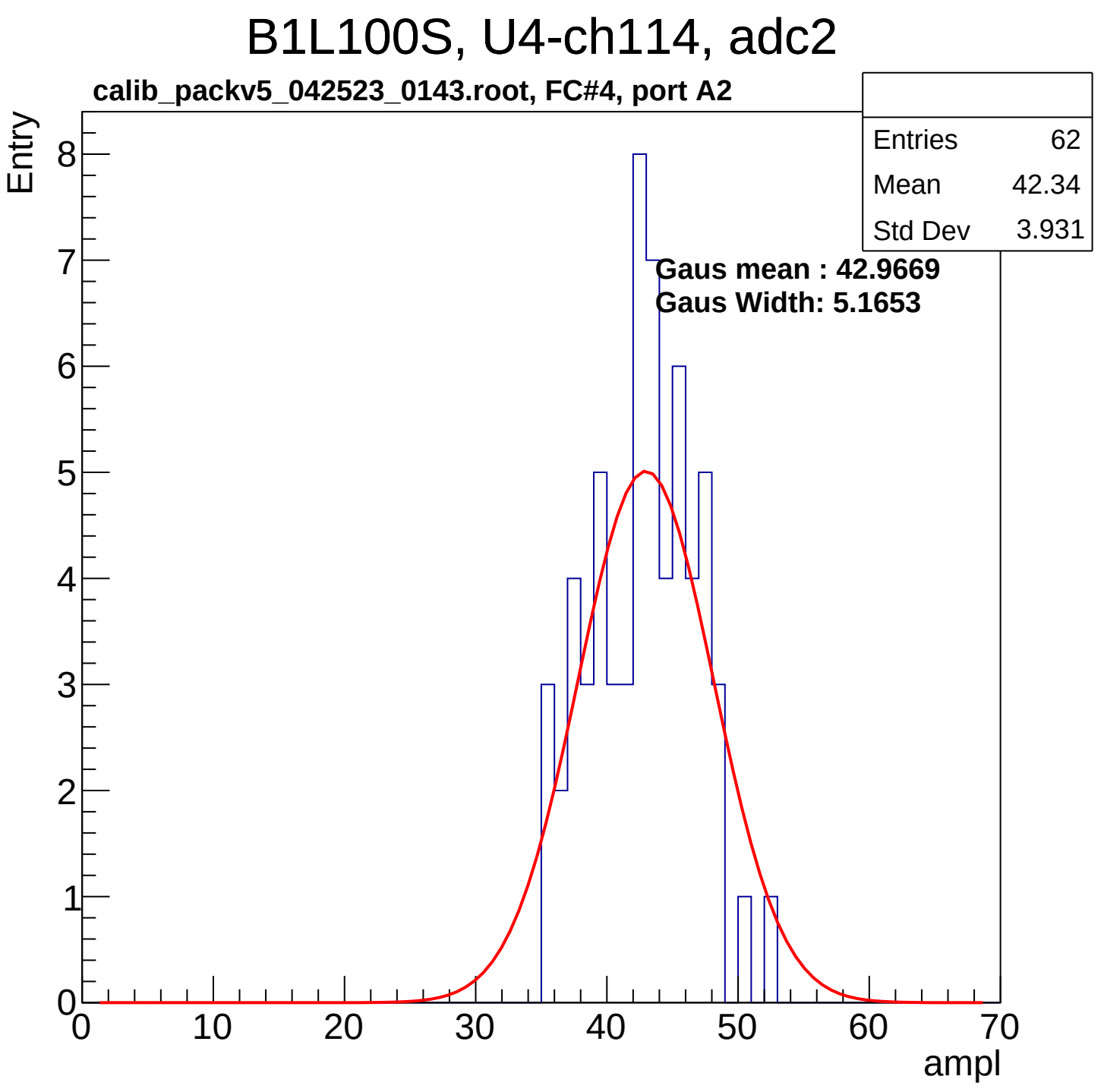

B1L100S, U4-ch113, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 44
Mean 58.68
Std Dev 9.229
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

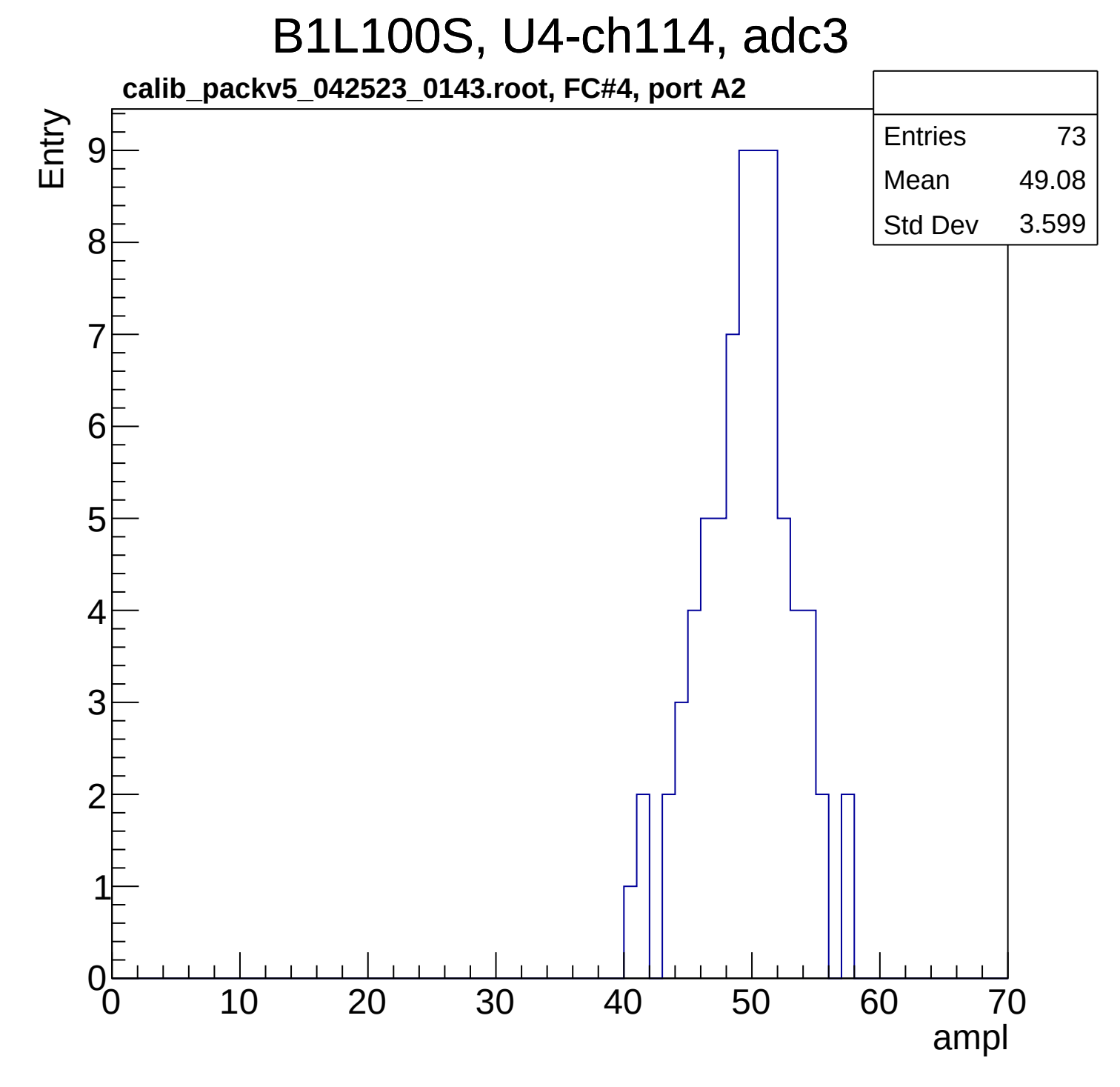

B1L100S, U4-ch113, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 62
Std Dev 1.414
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

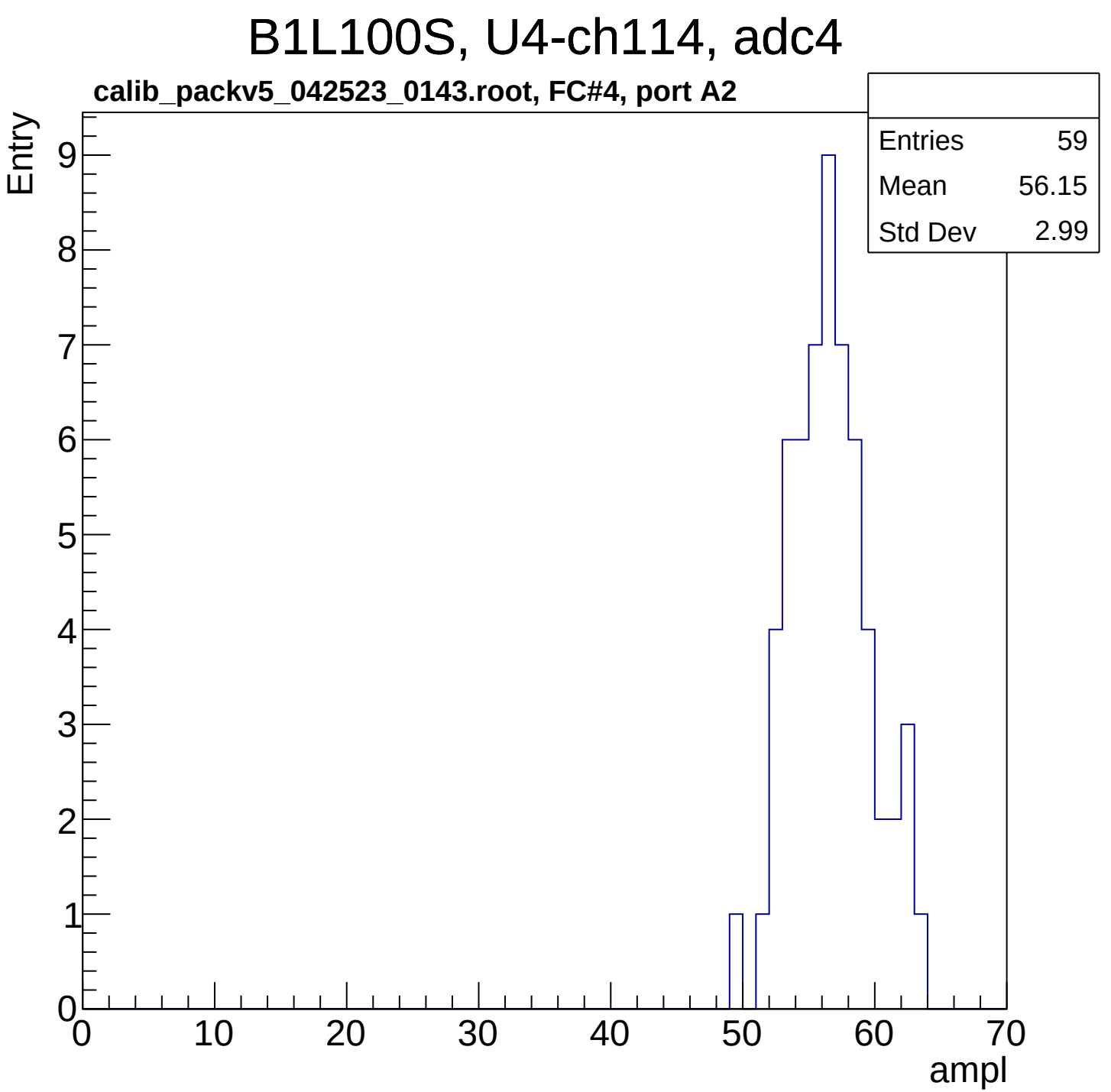

B1L100S, U4-ch113, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 20
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

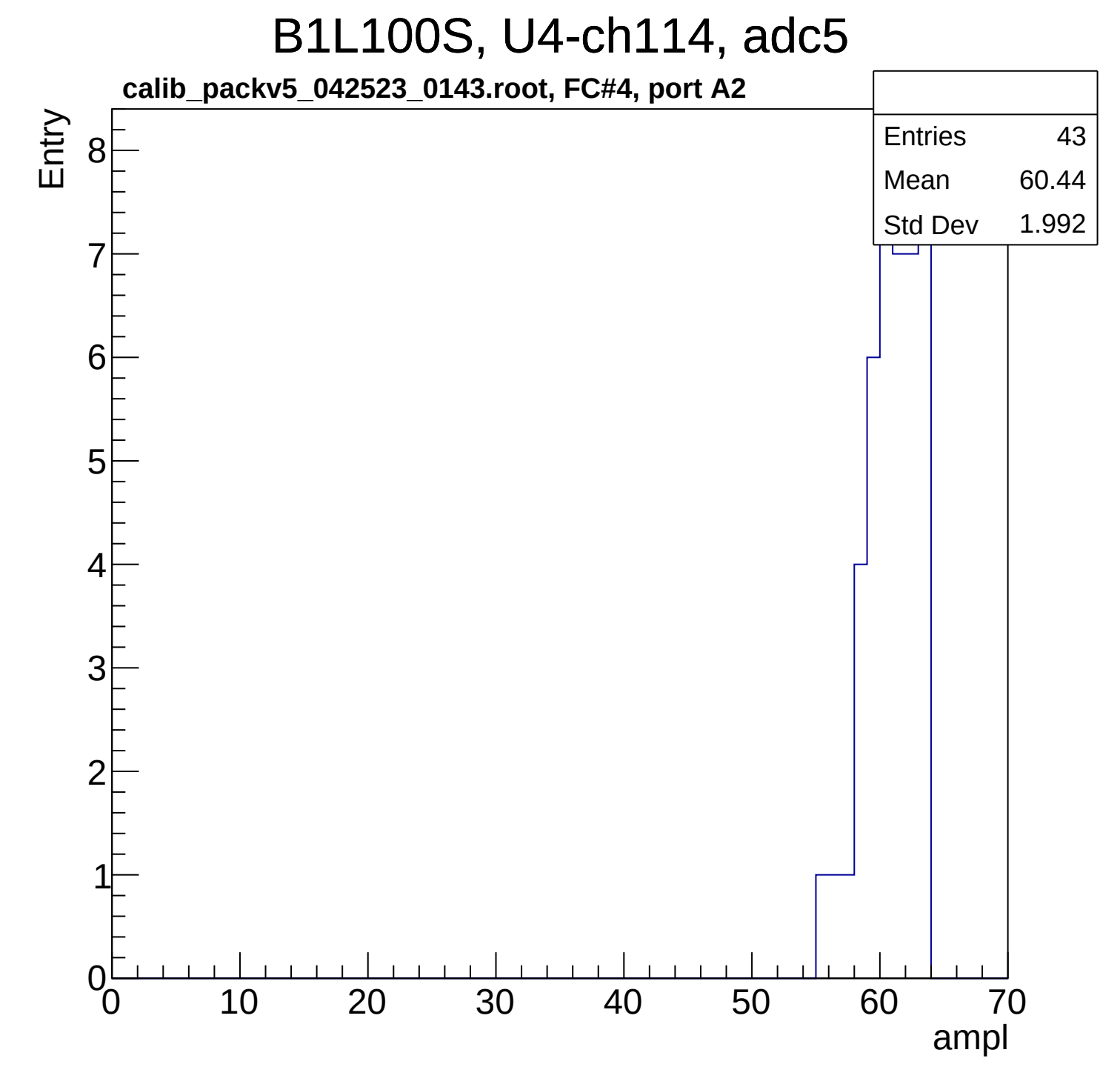

B1L100S, U4-ch114, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 29.2
Std Dev 5.783
Gaus mean : 30.6137
Gaus Width: 3.4897
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

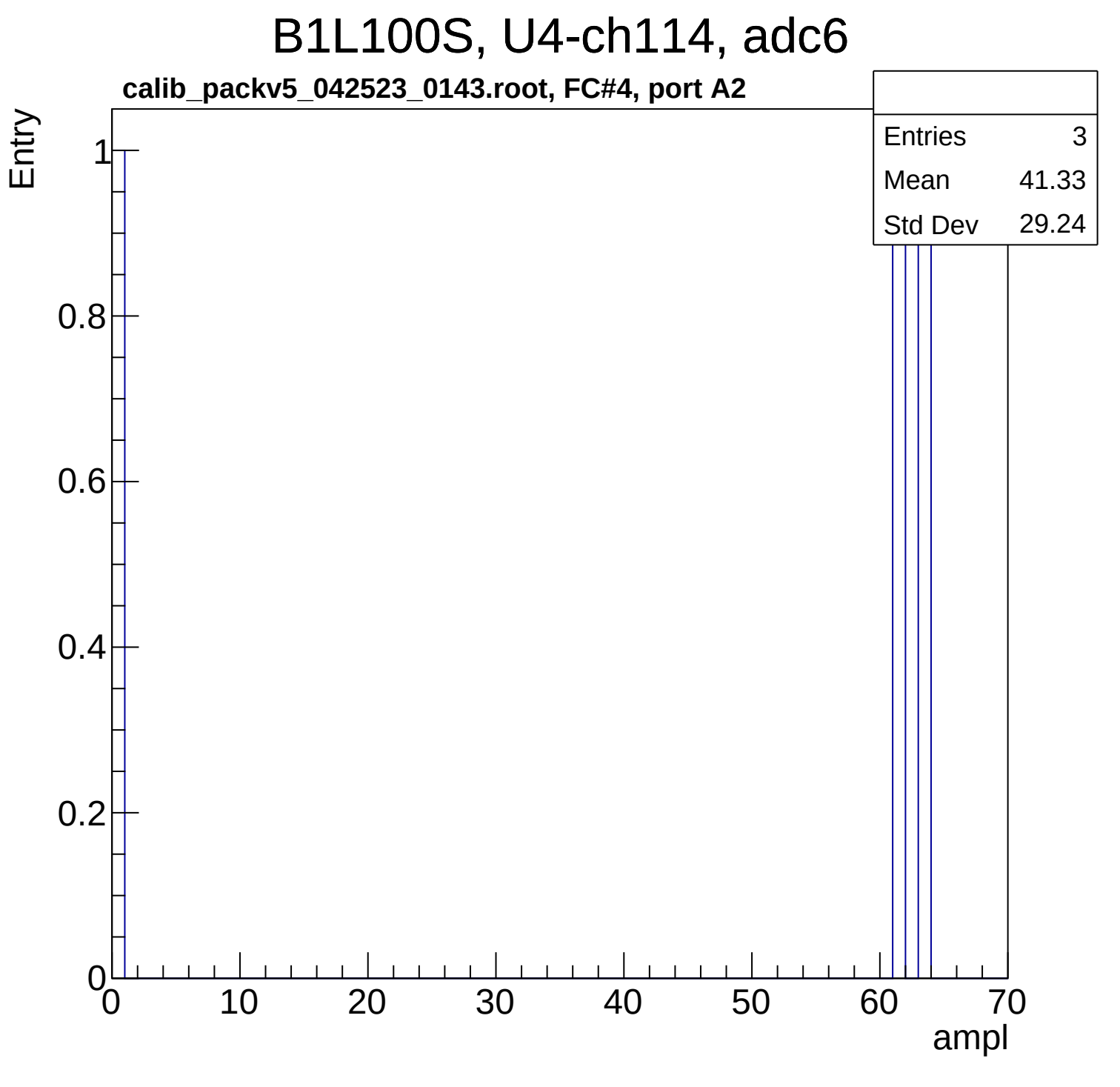

B1L100S, U4-ch114, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 37.54
Std Dev 3.695
Gaus mean : 37.8655
Gaus Width: 4.0335
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

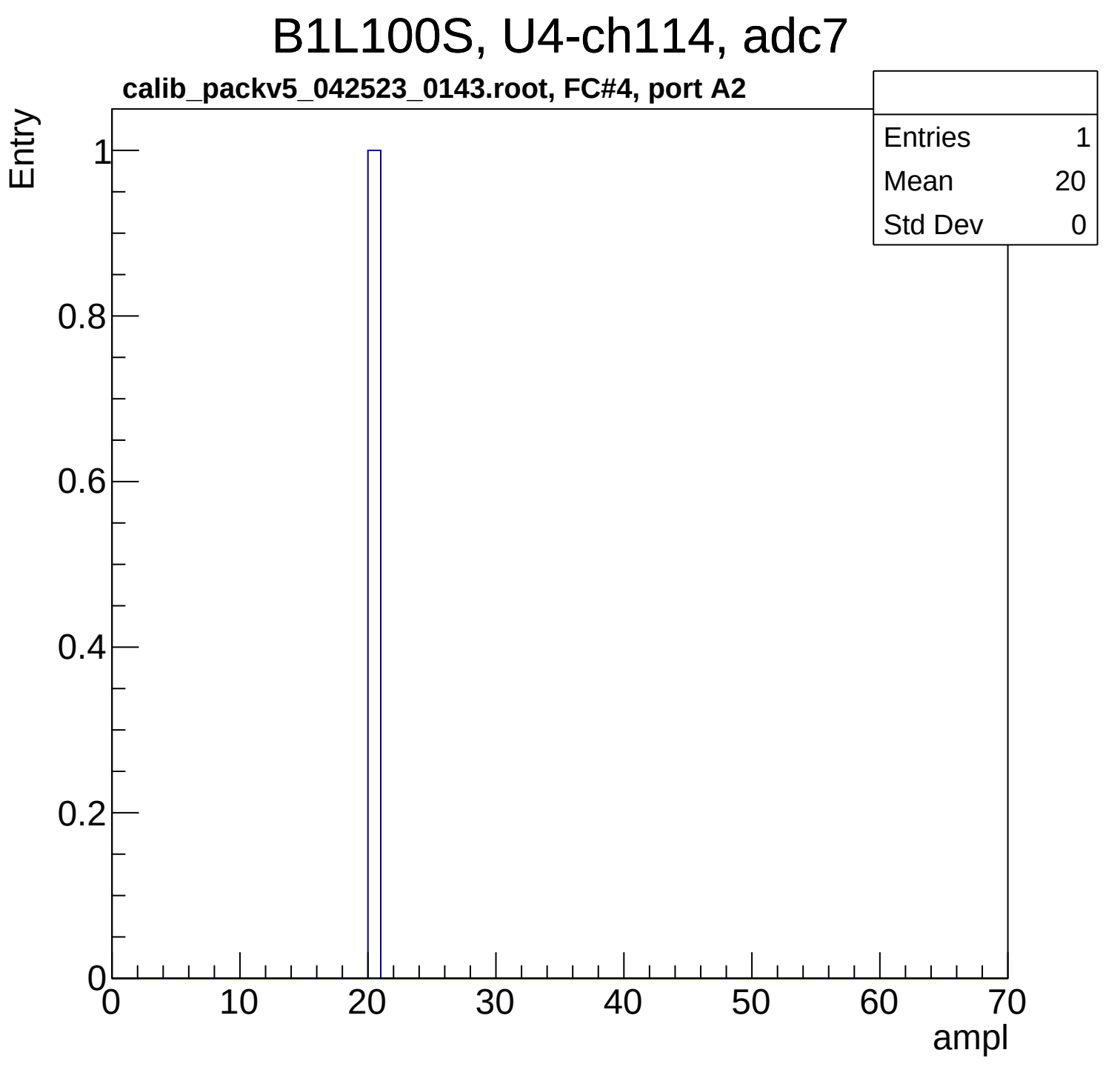

B1L100S, U4-ch114, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 42.34
Std Dev 3.931
Gaus mean : 42.9669
Gaus Width: 5.1653
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

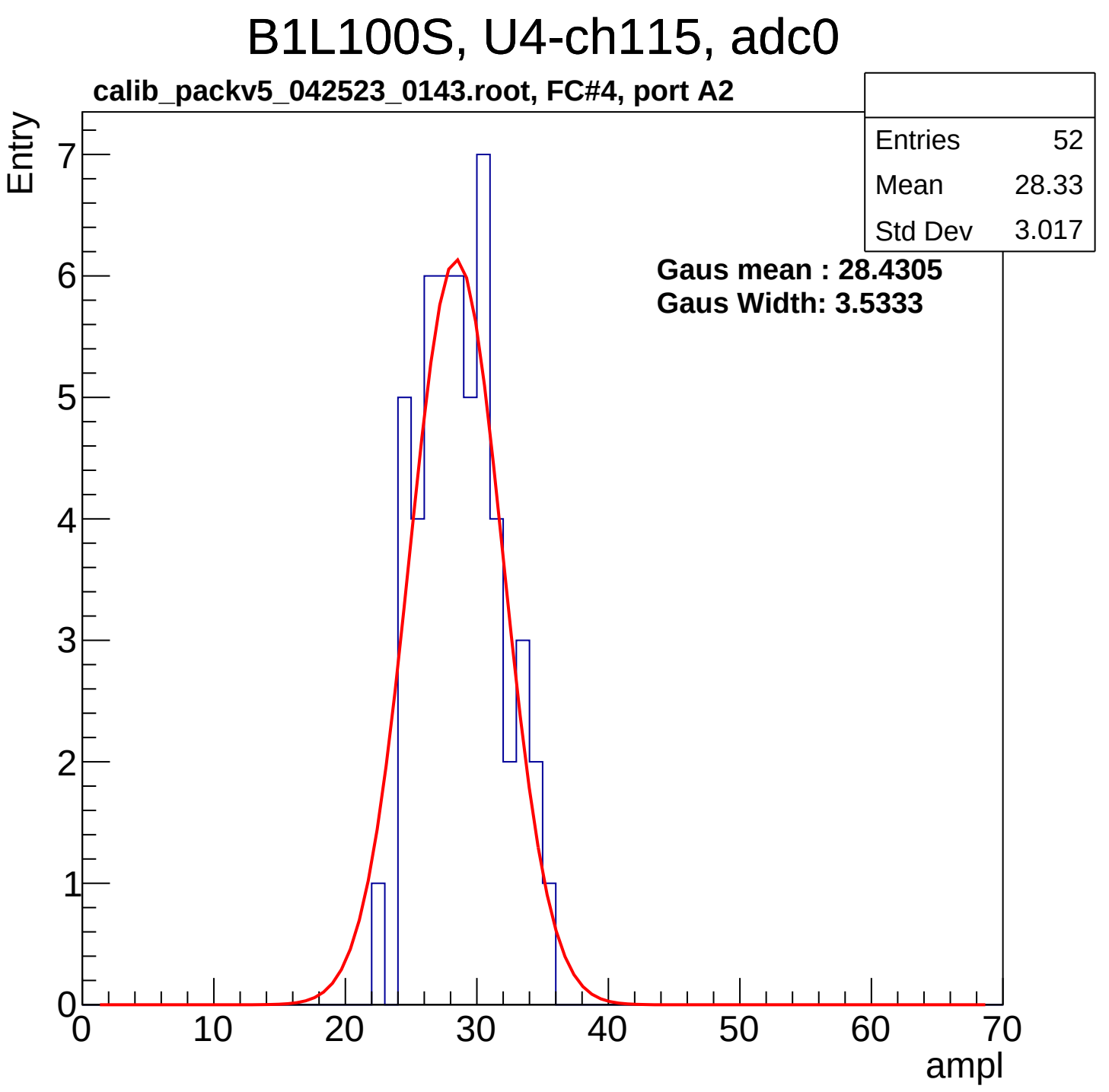

B1L100S, U4-ch114, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 49.08
Std Dev 3.599
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

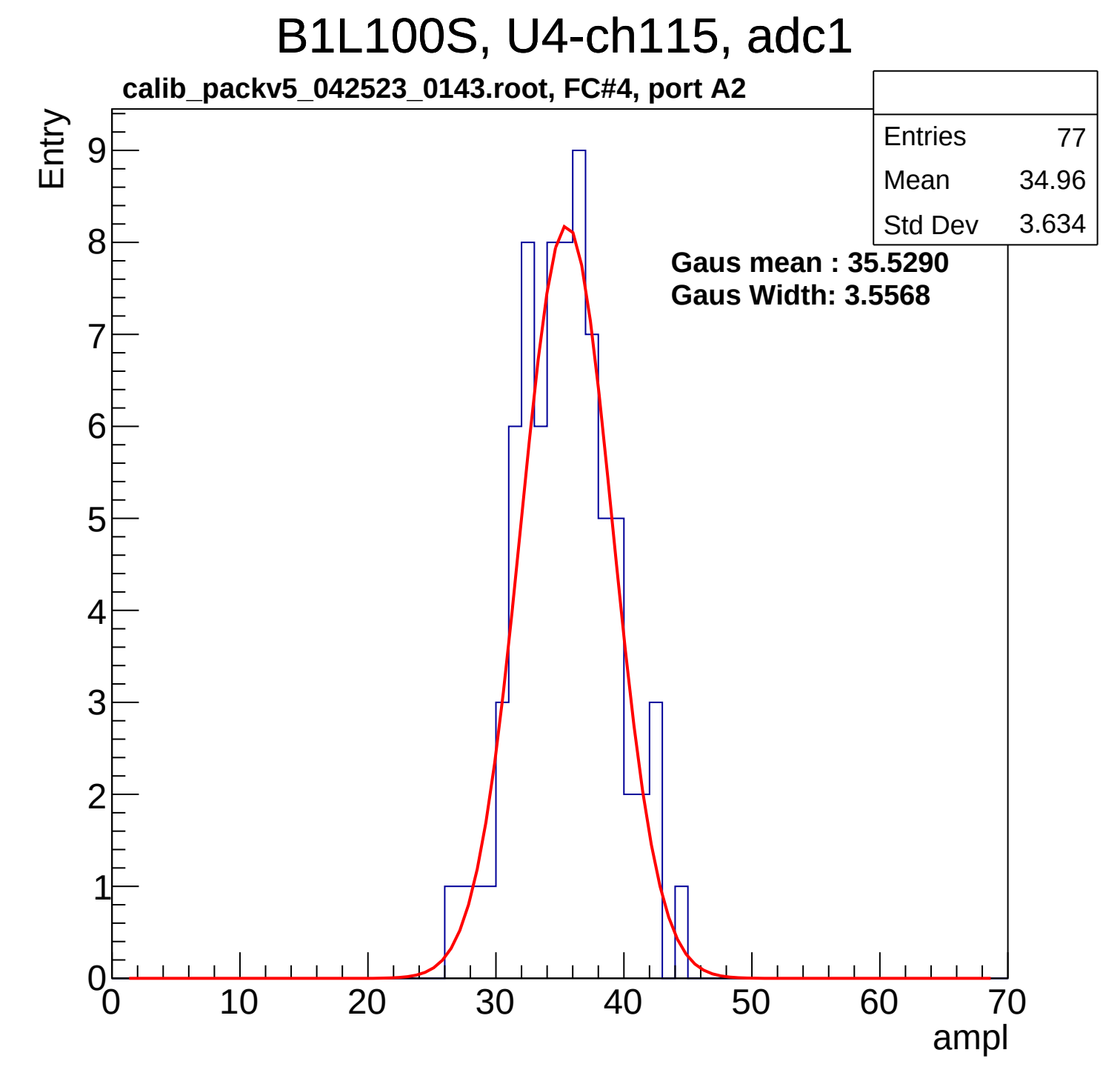

B1L100S, U4-ch114, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 56.15
Std Dev 2.99
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

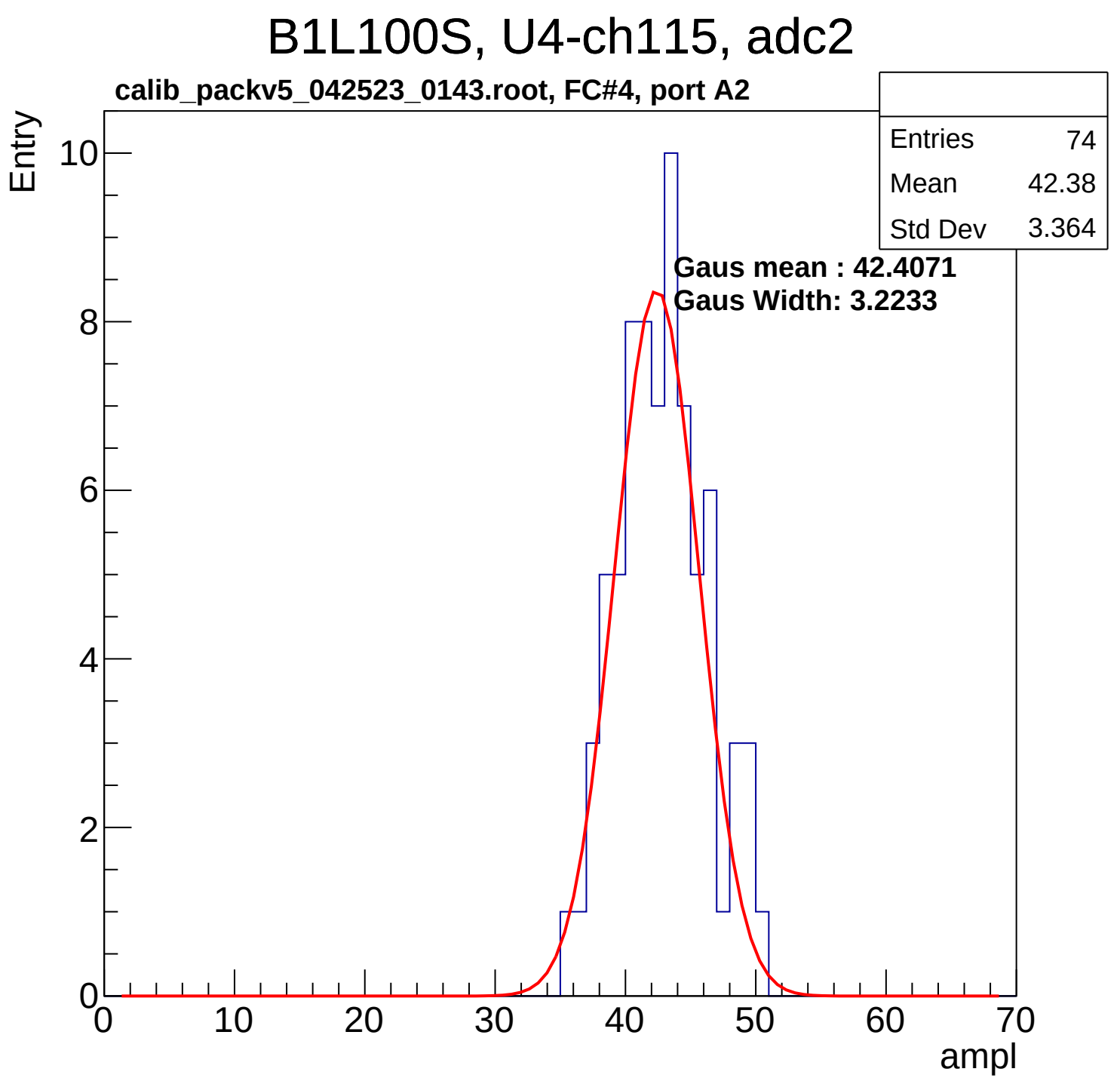

B1L100S, U4-ch114, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 60.44
Std Dev 1.992
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

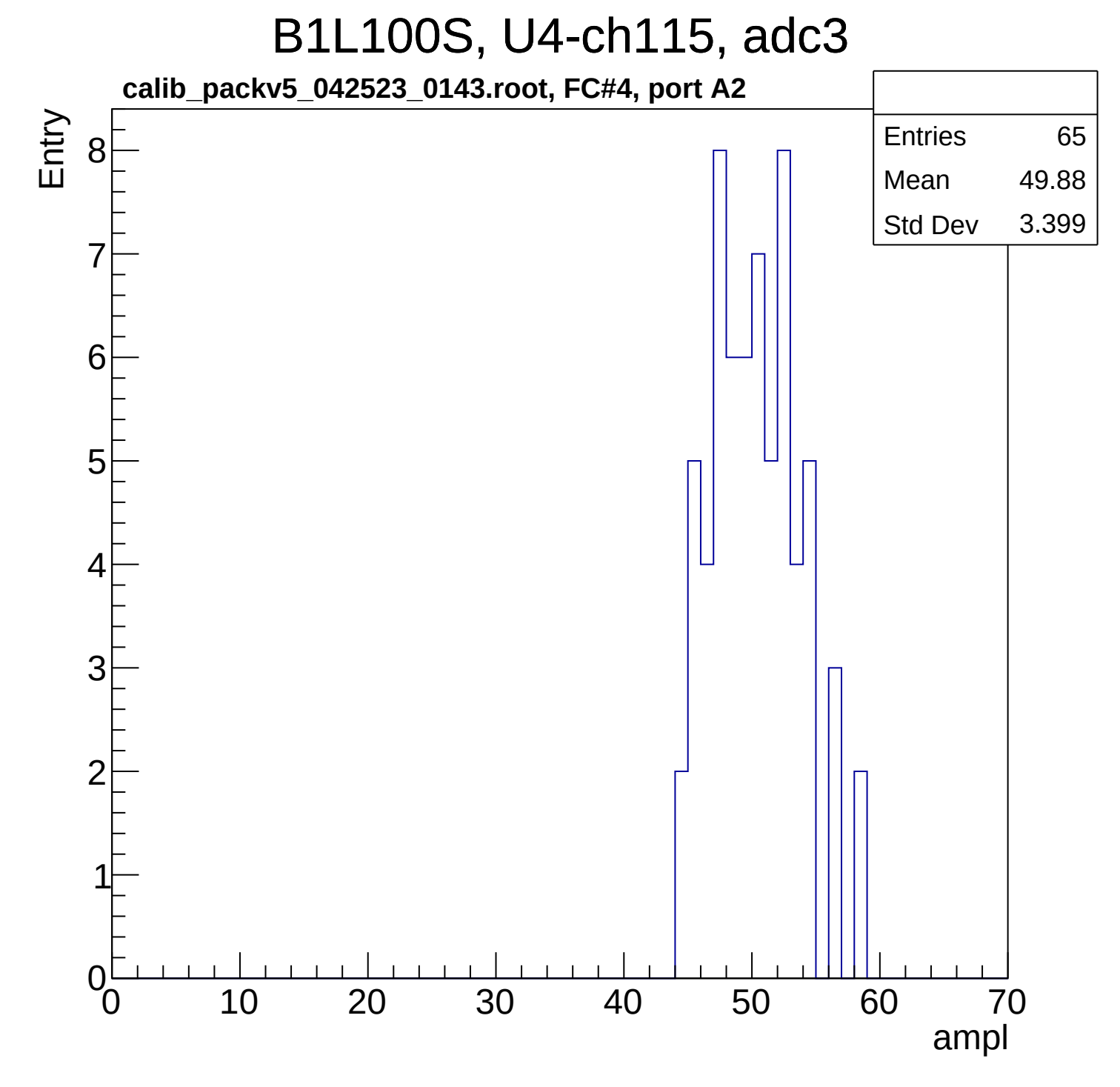

B1L100S, U4-ch114, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 41.33
Std Dev 29.24
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

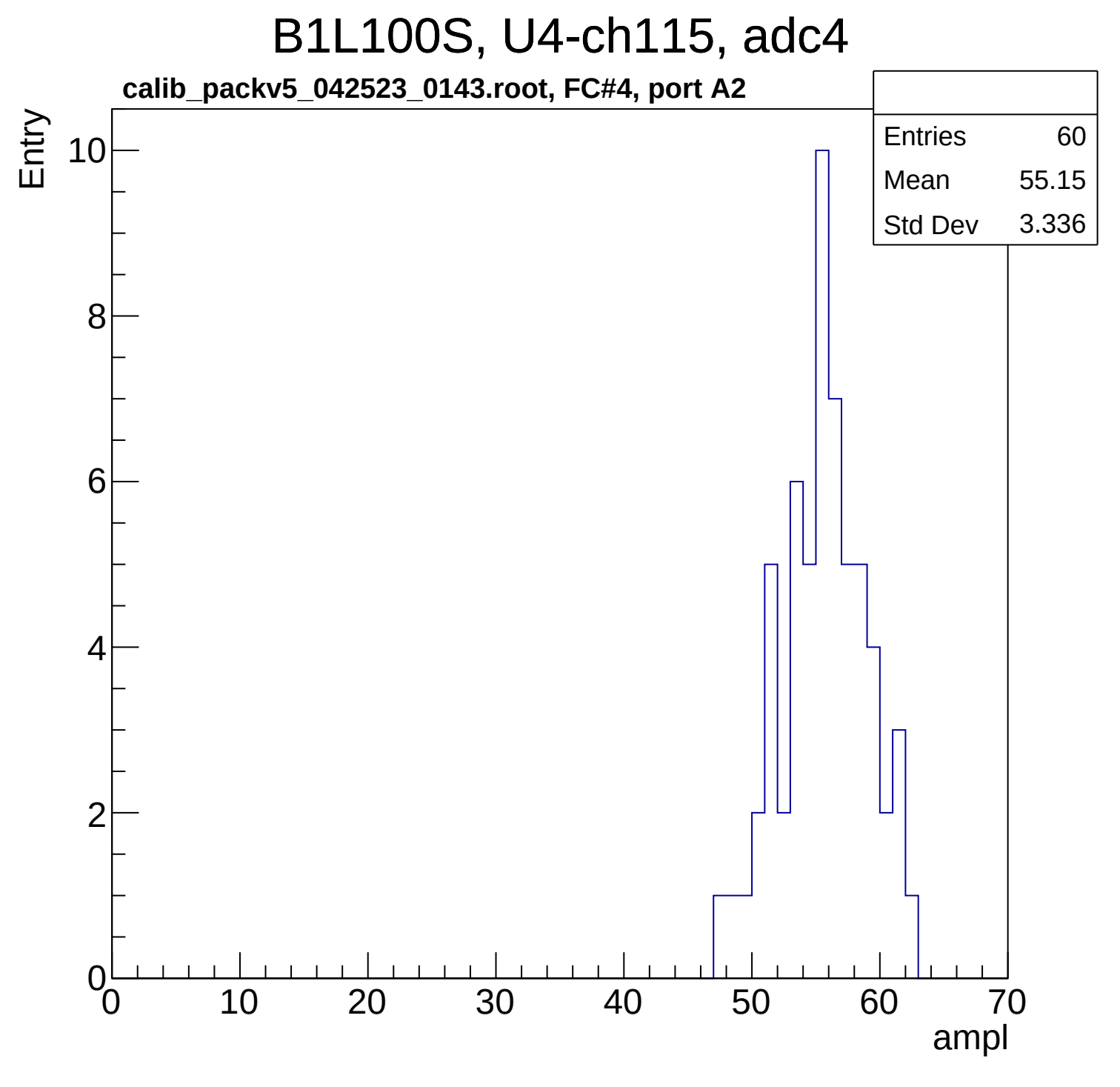

B1L100S, U4-ch114, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 20
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

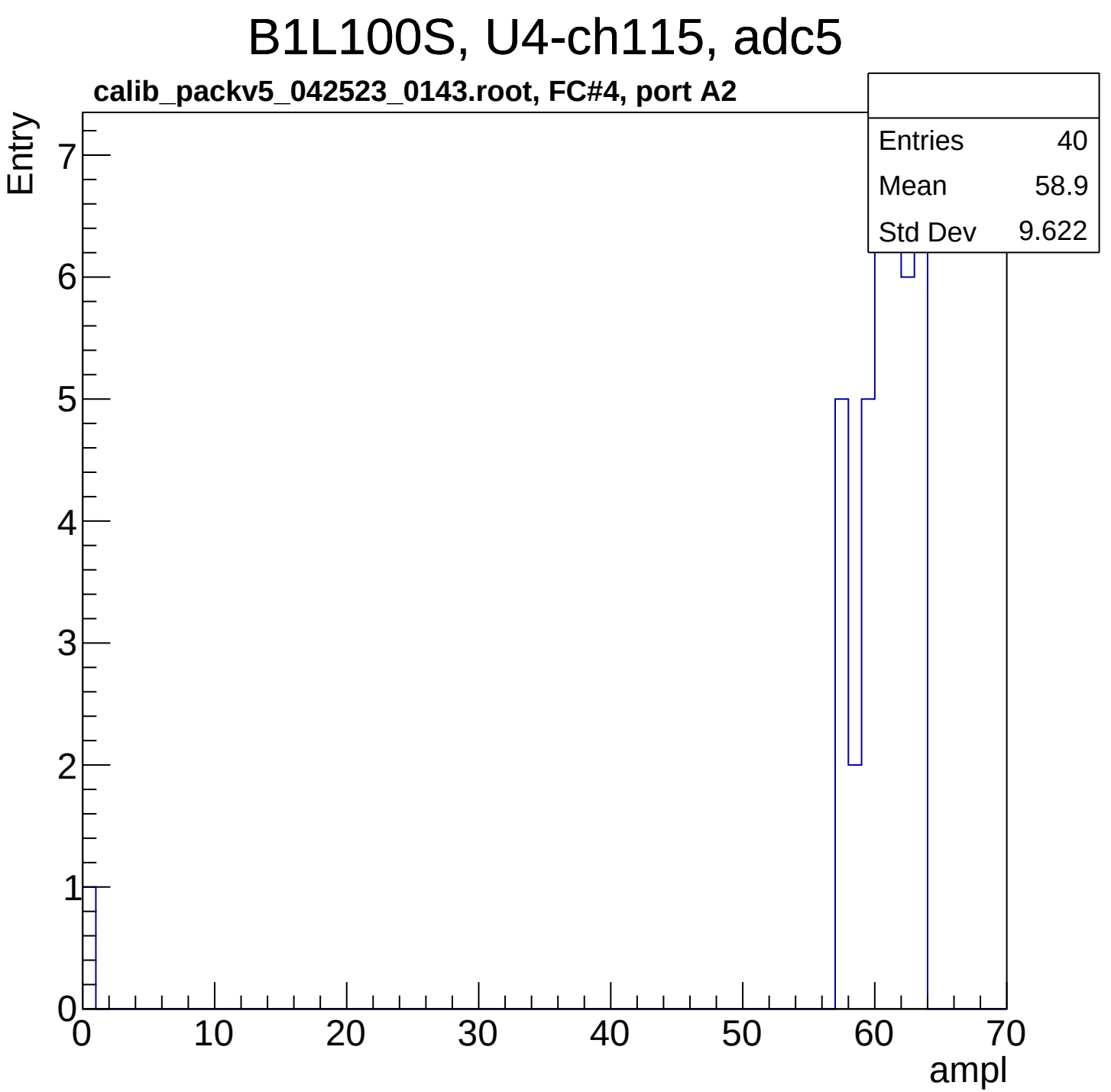

B1L100S, U4-ch115, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 28.33
Std Dev 3.017
Gaus mean : 28.4305
Gaus Width: 3.5333
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

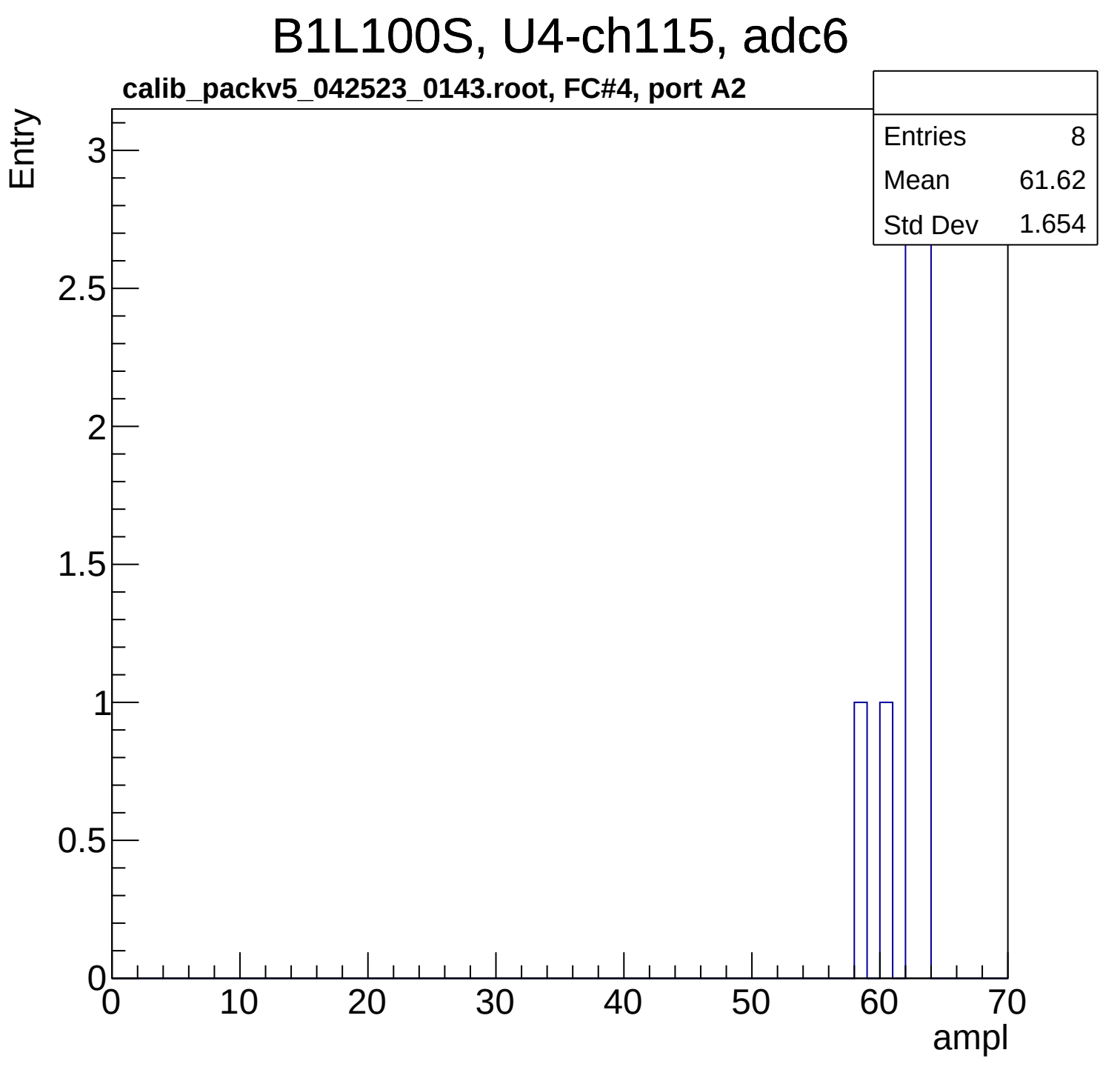

B1L100S, U4-ch115, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 34.96
Std Dev 3.634
Gaus mean : 35.5290
Gaus Width: 3.5568
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

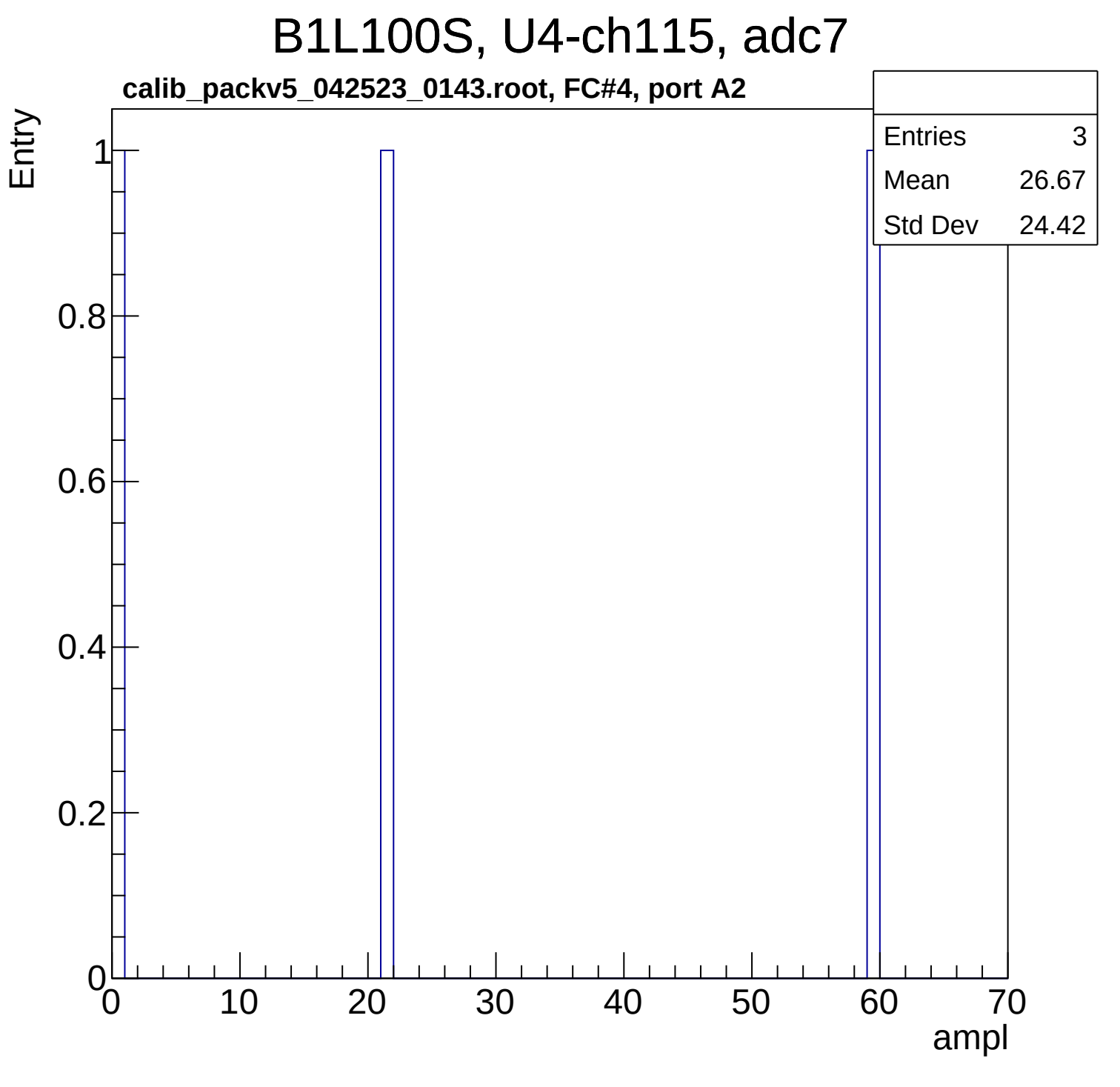

B1L100S, U4-ch115, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 42.38
Std Dev 3.364
Gaus mean : 42.4071
Gaus Width: 3.2233
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

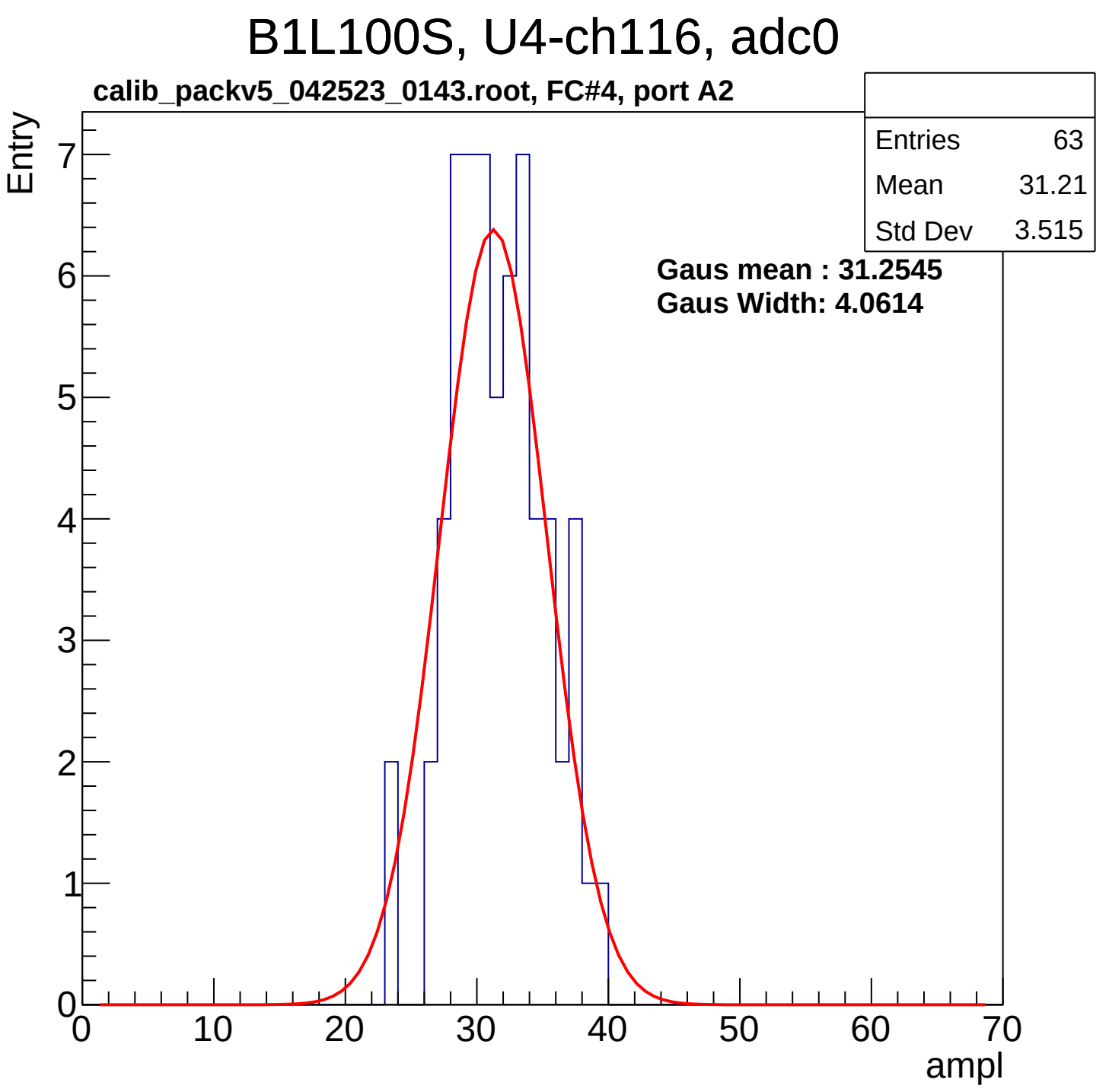

B1L100S, U4-ch115, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 49.88
Std Dev 3.399
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

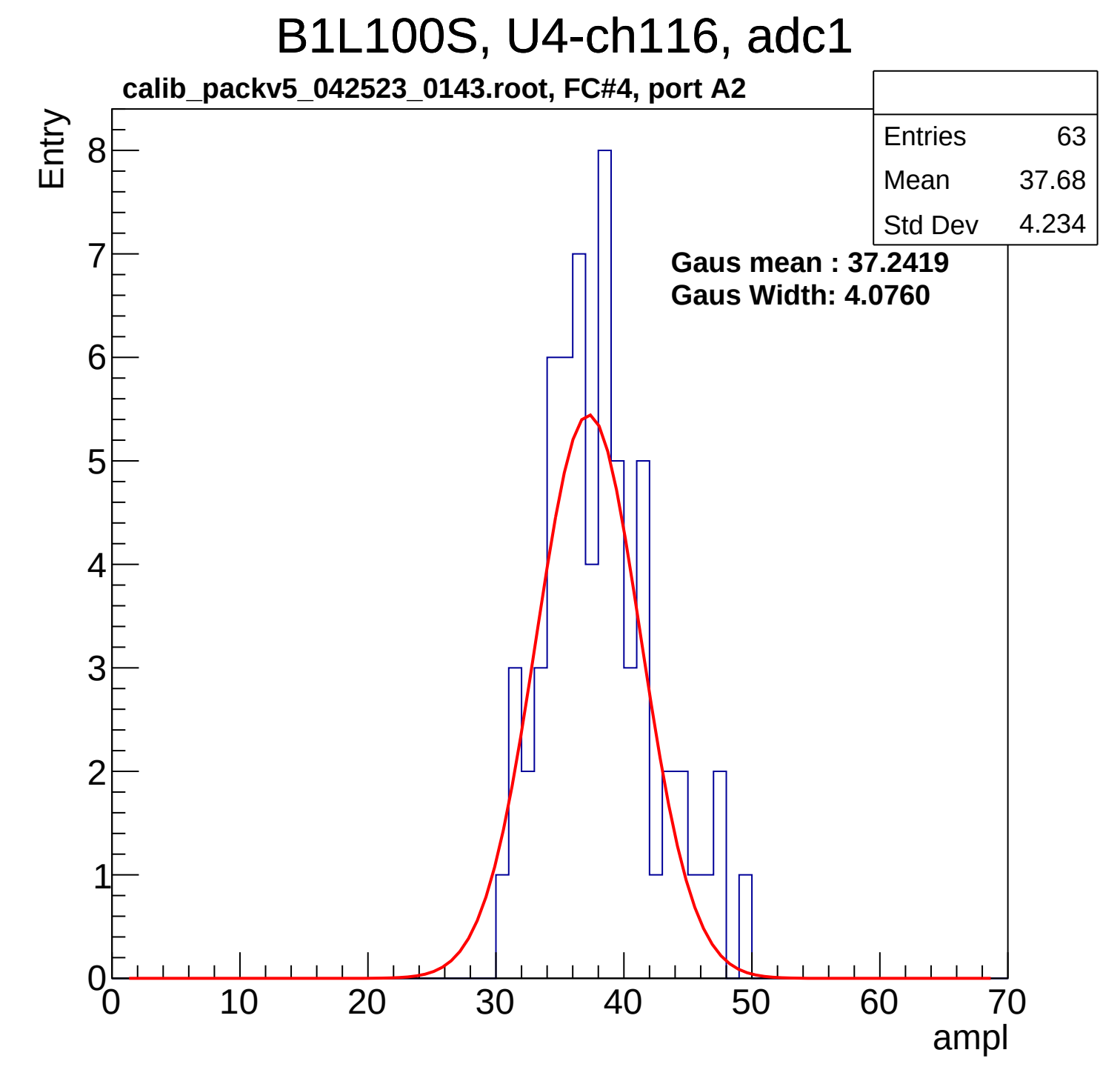

B1L100S, U4-ch115, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 55.15
Std Dev 3.336
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

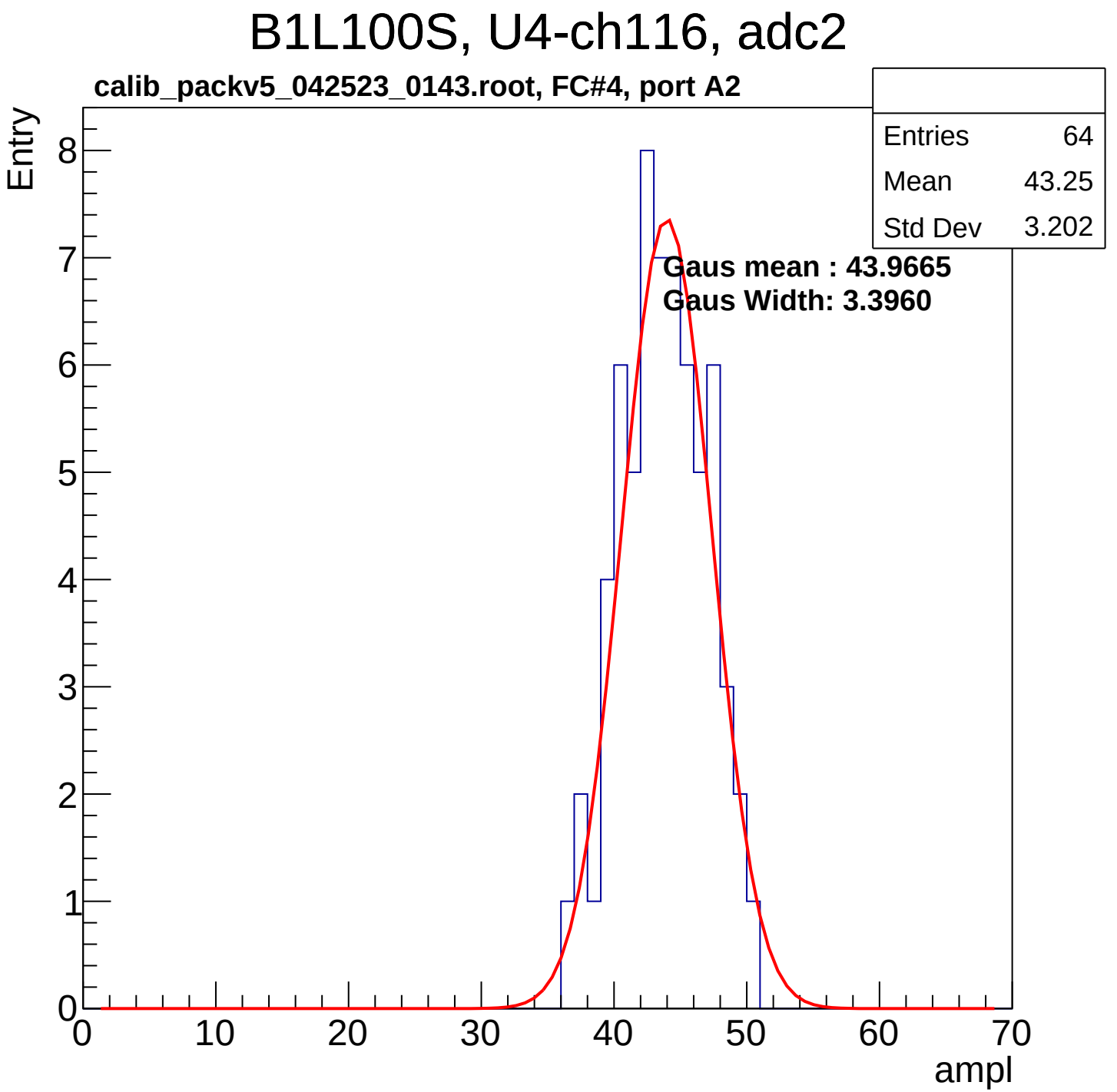

B1L100S, U4-ch115, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 40
Mean 58.9
Std Dev 9.622
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

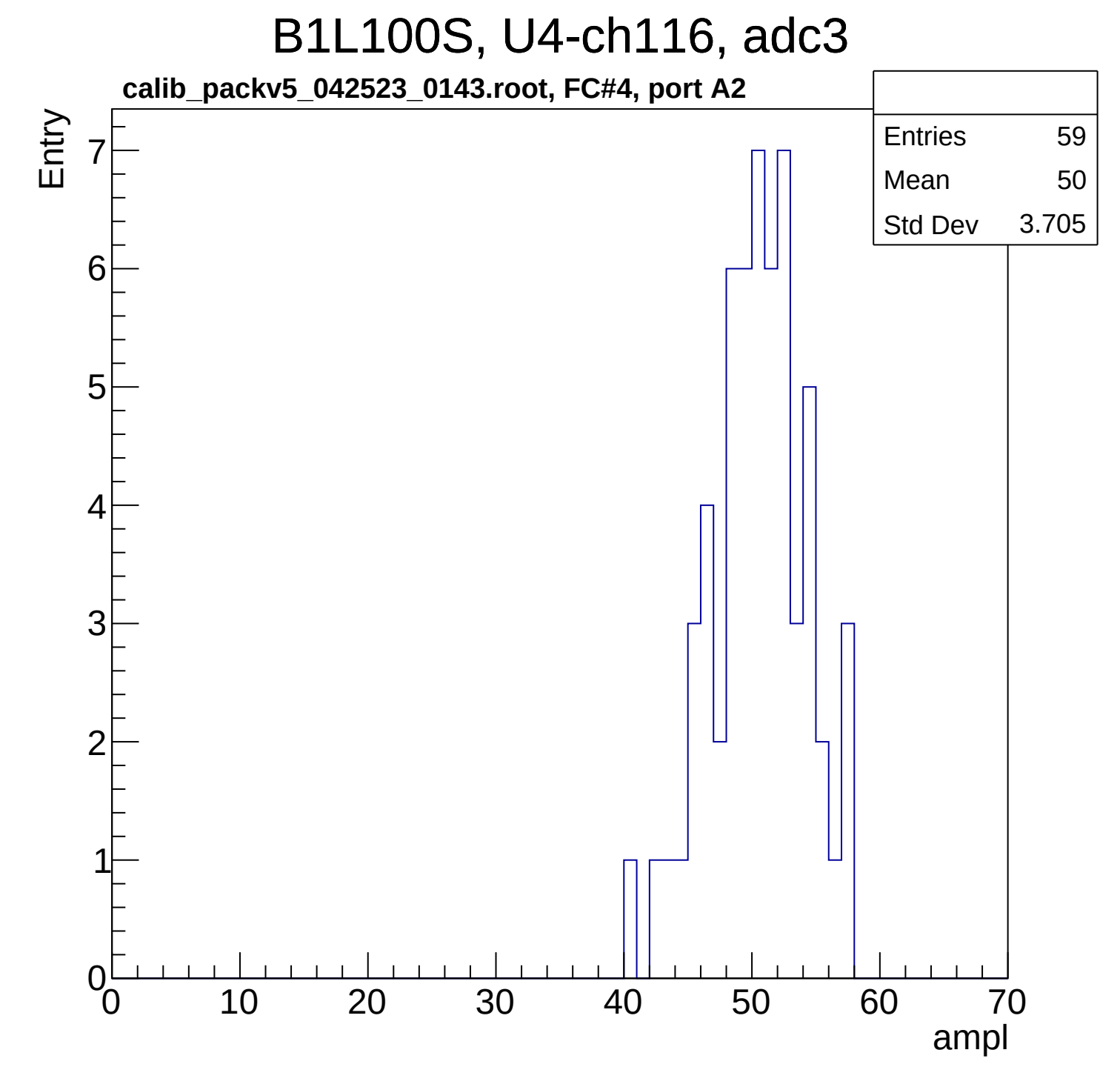

B1L100S, U4-ch115, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 8
Mean 61.62
Std Dev 1.654
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

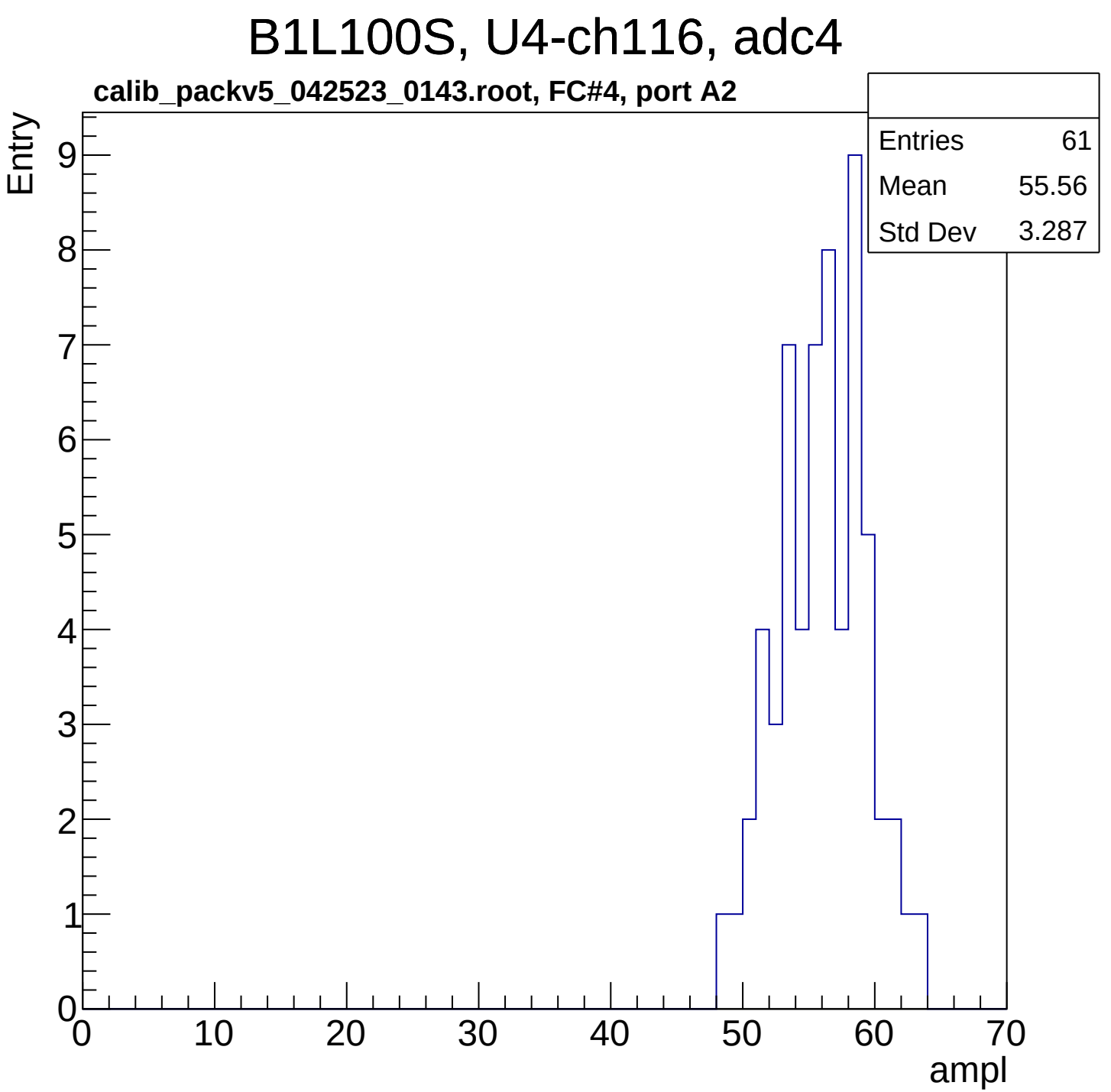

B1L100S, U4-ch115, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 26.67
Std Dev 24.42
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

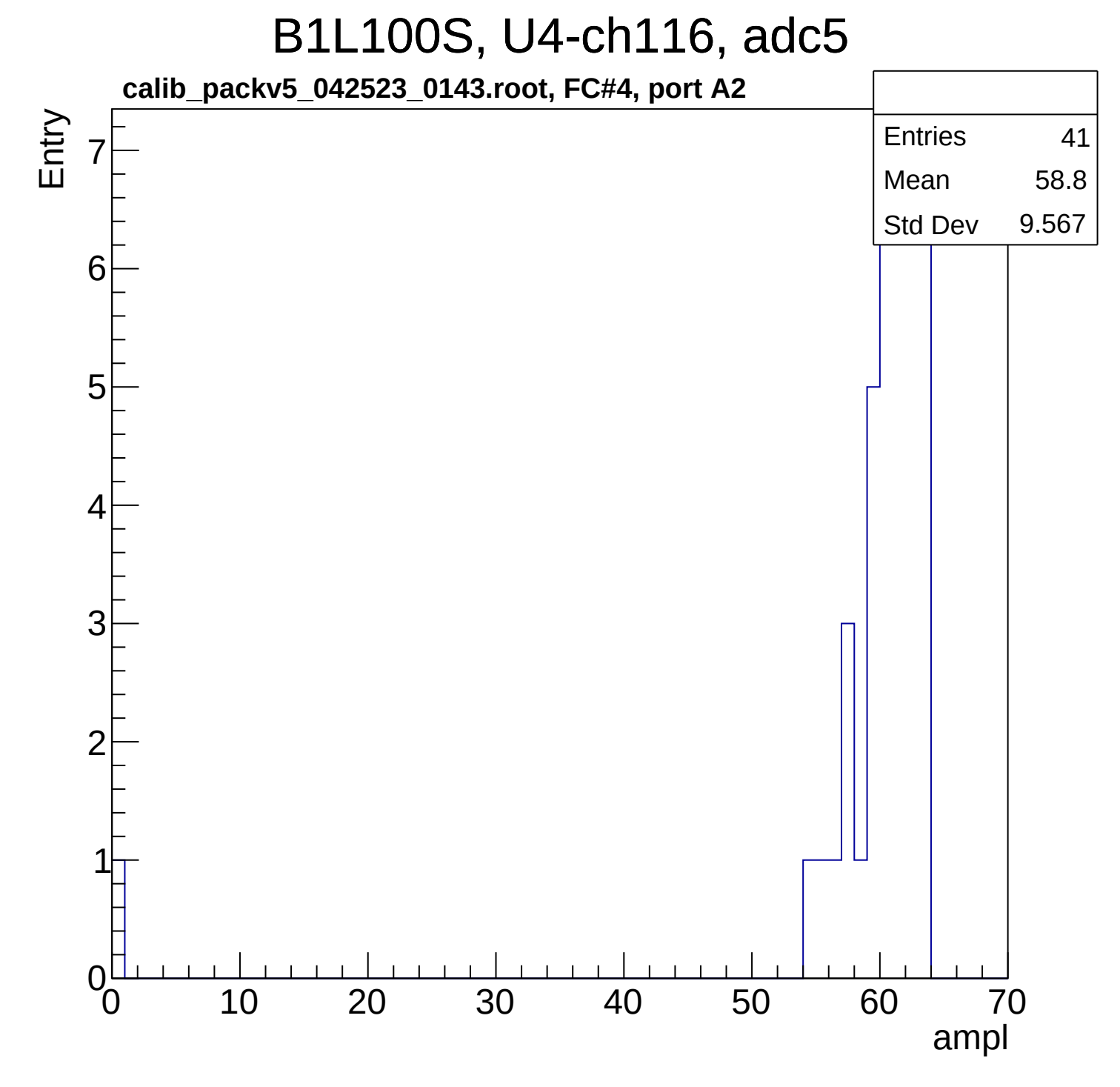

B1L100S, U4-ch116, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 31.21
Std Dev 3.515
Gaus mean : 31.2545
Gaus Width: 4.0614
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

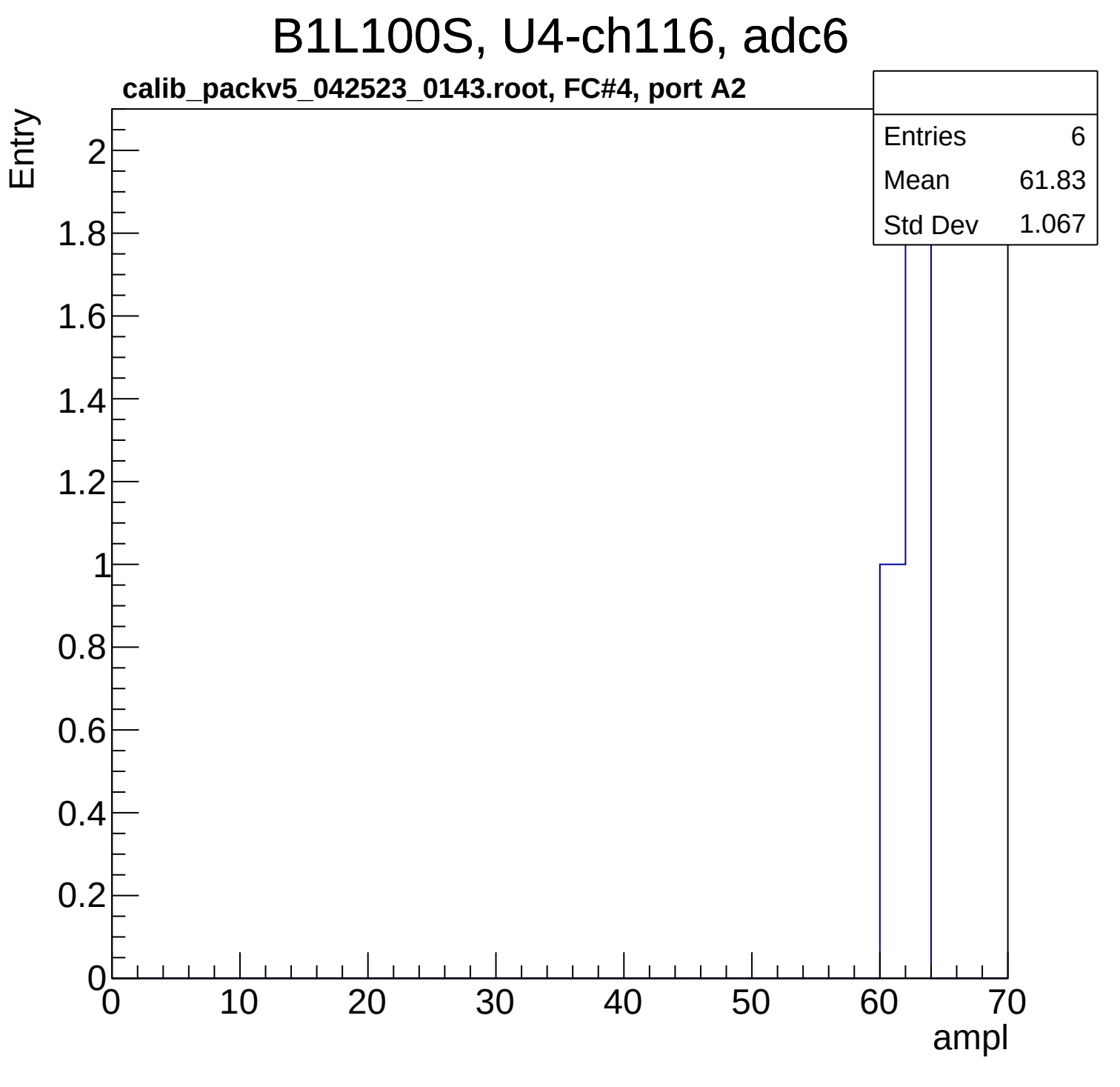

B1L100S, U4-ch116, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 37.68
Std Dev 4.234
Gaus mean : 37.2419
Gaus Width: 4.0760
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

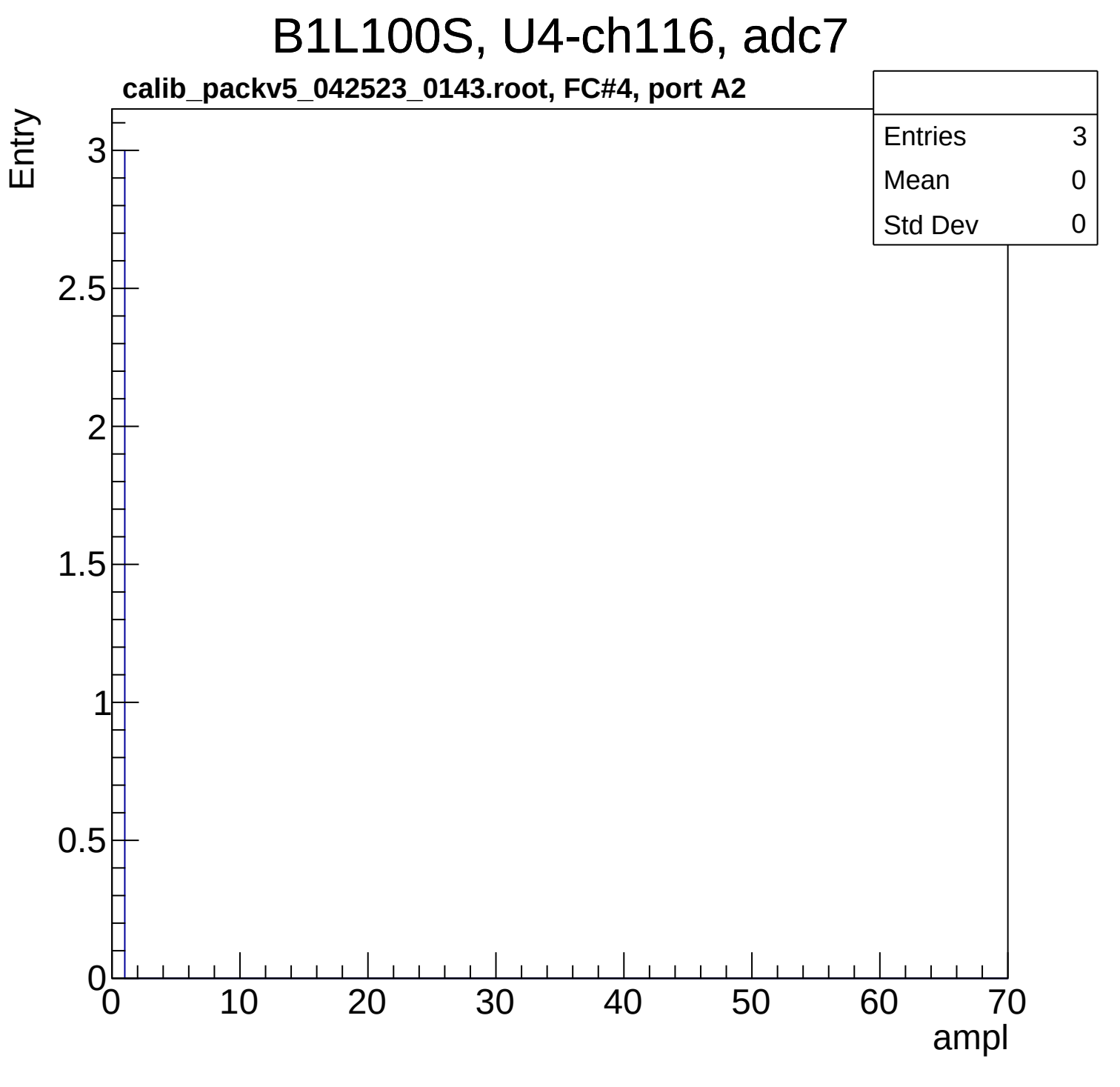

B1L100S, U4-ch116, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 43.25
Std Dev 3.202
Gaus mean : 43.9665
Gaus Width: 3.3960
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

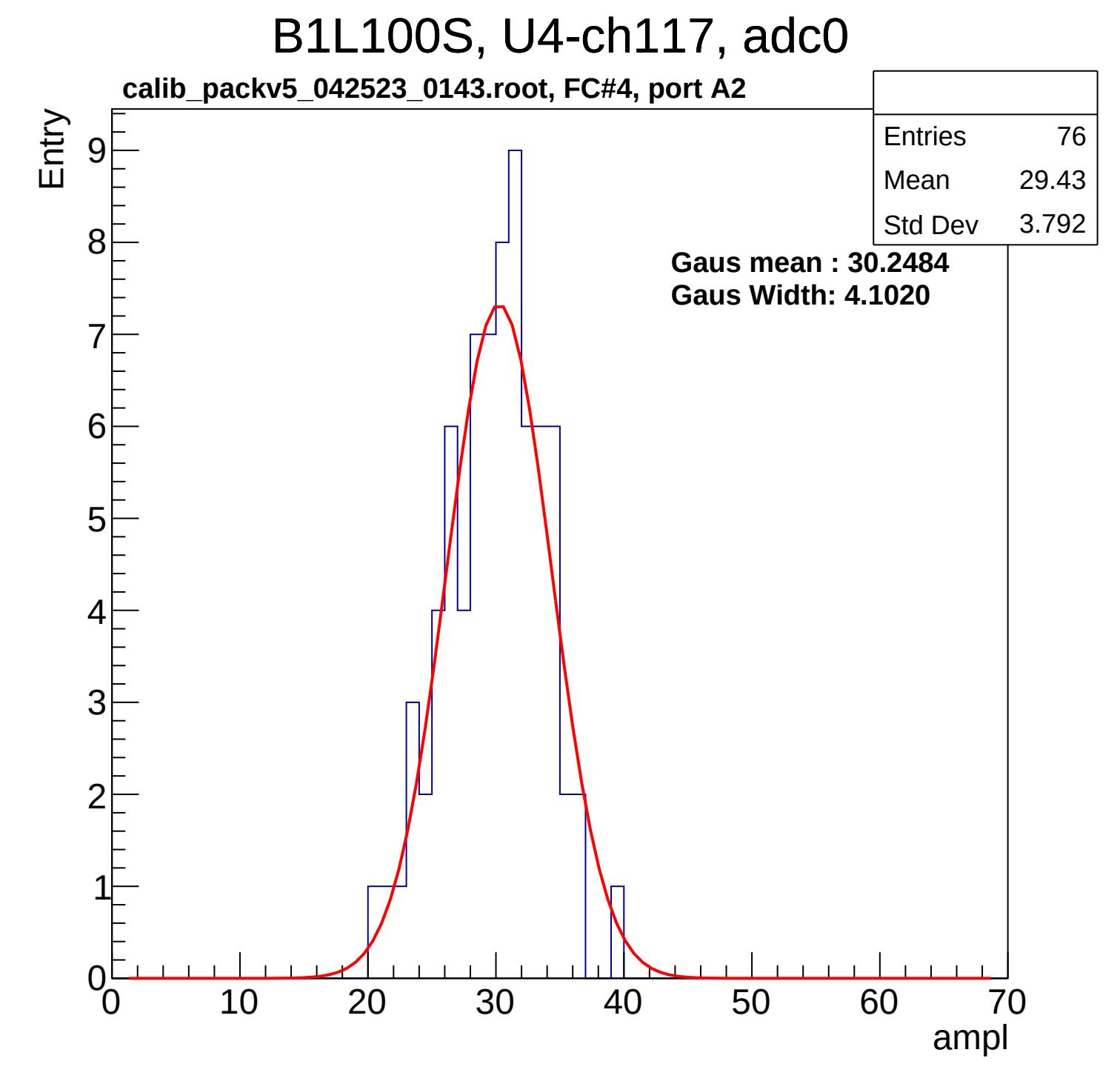

B1L100S, U4-ch116, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 50
Std Dev 3.705
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

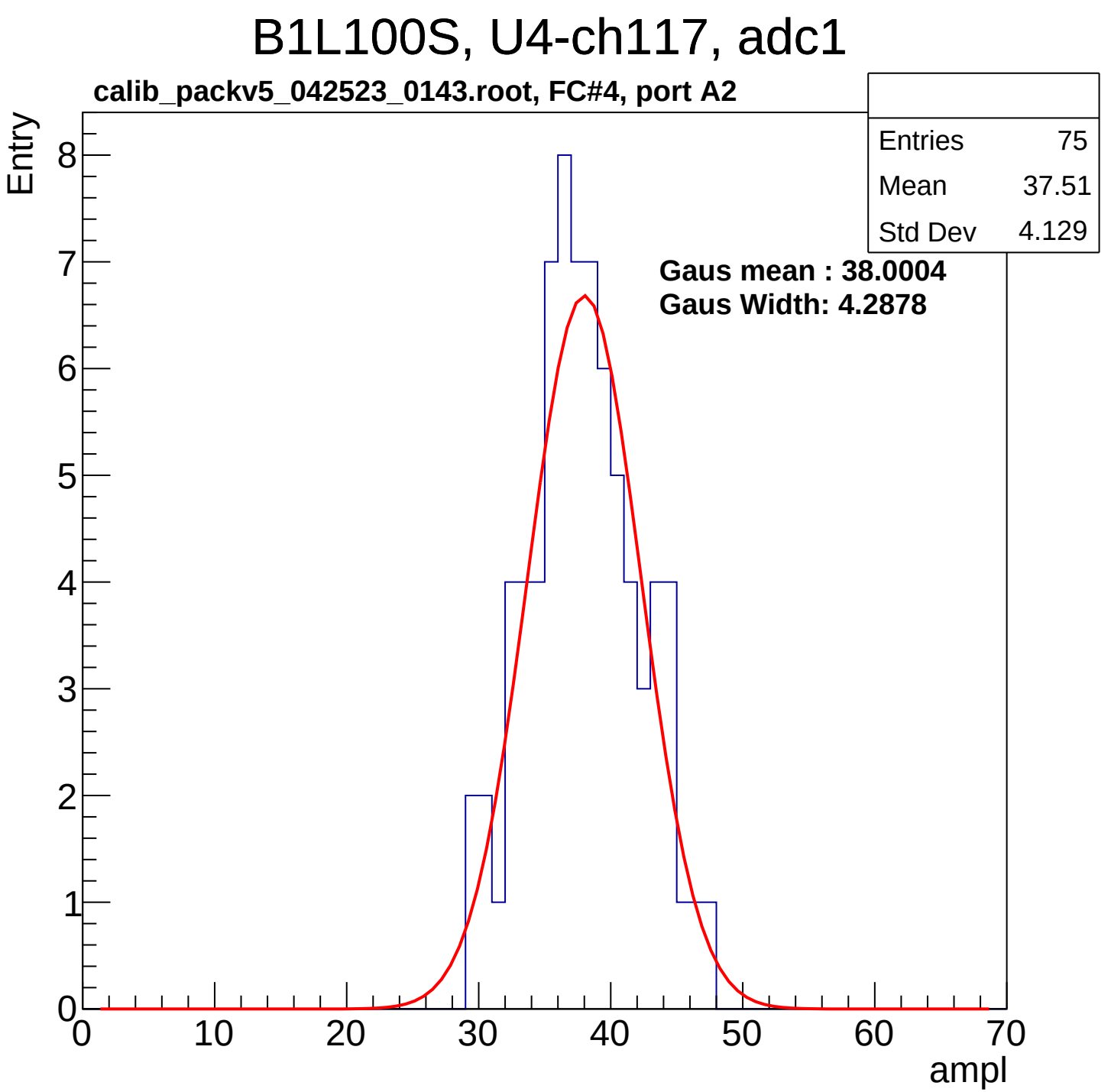

B1L100S, U4-ch116, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 55.56
Std Dev 3.287
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

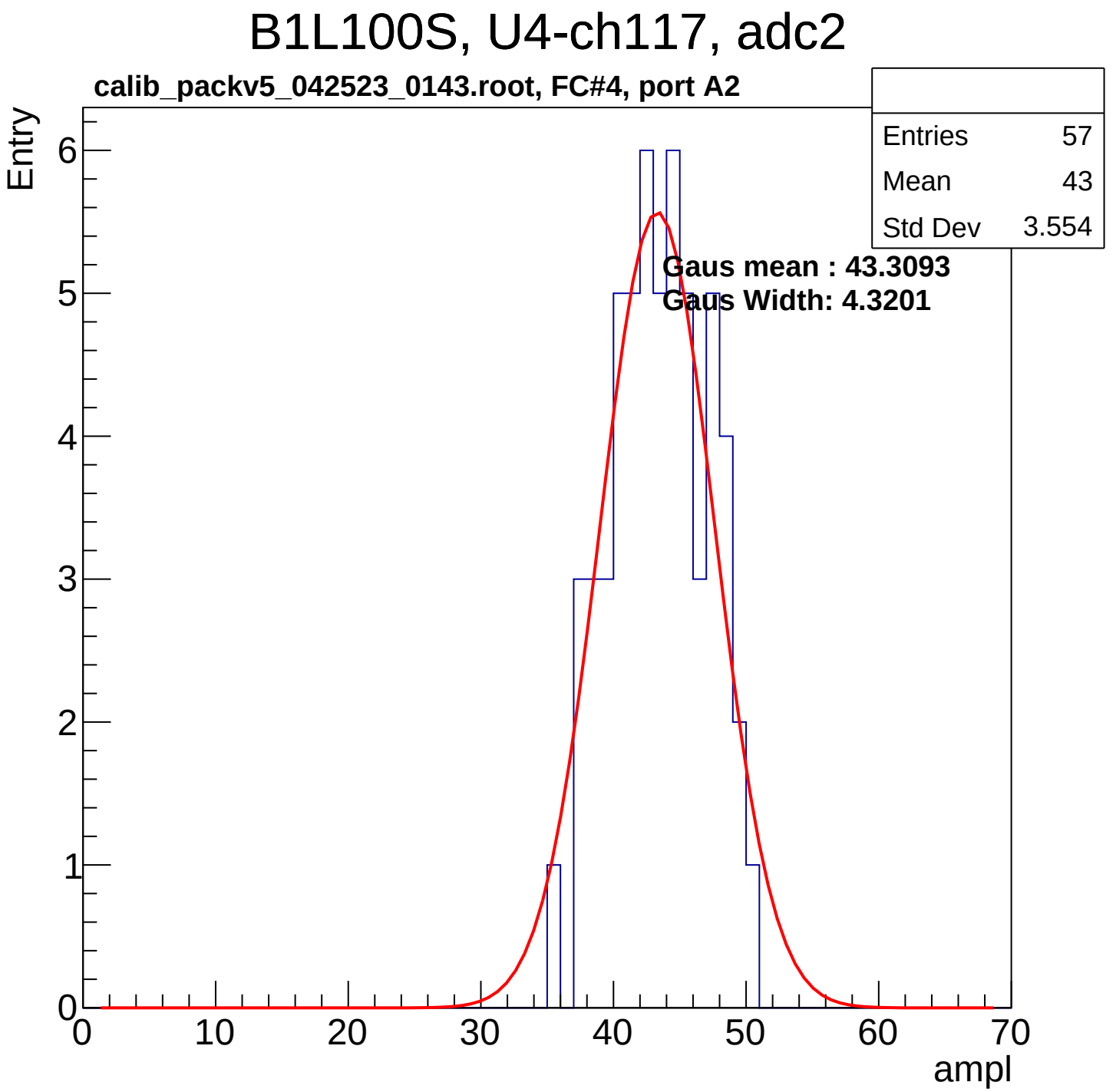

B1L100S, U4-ch116, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 41
Mean 58.8
Std Dev 9.567
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

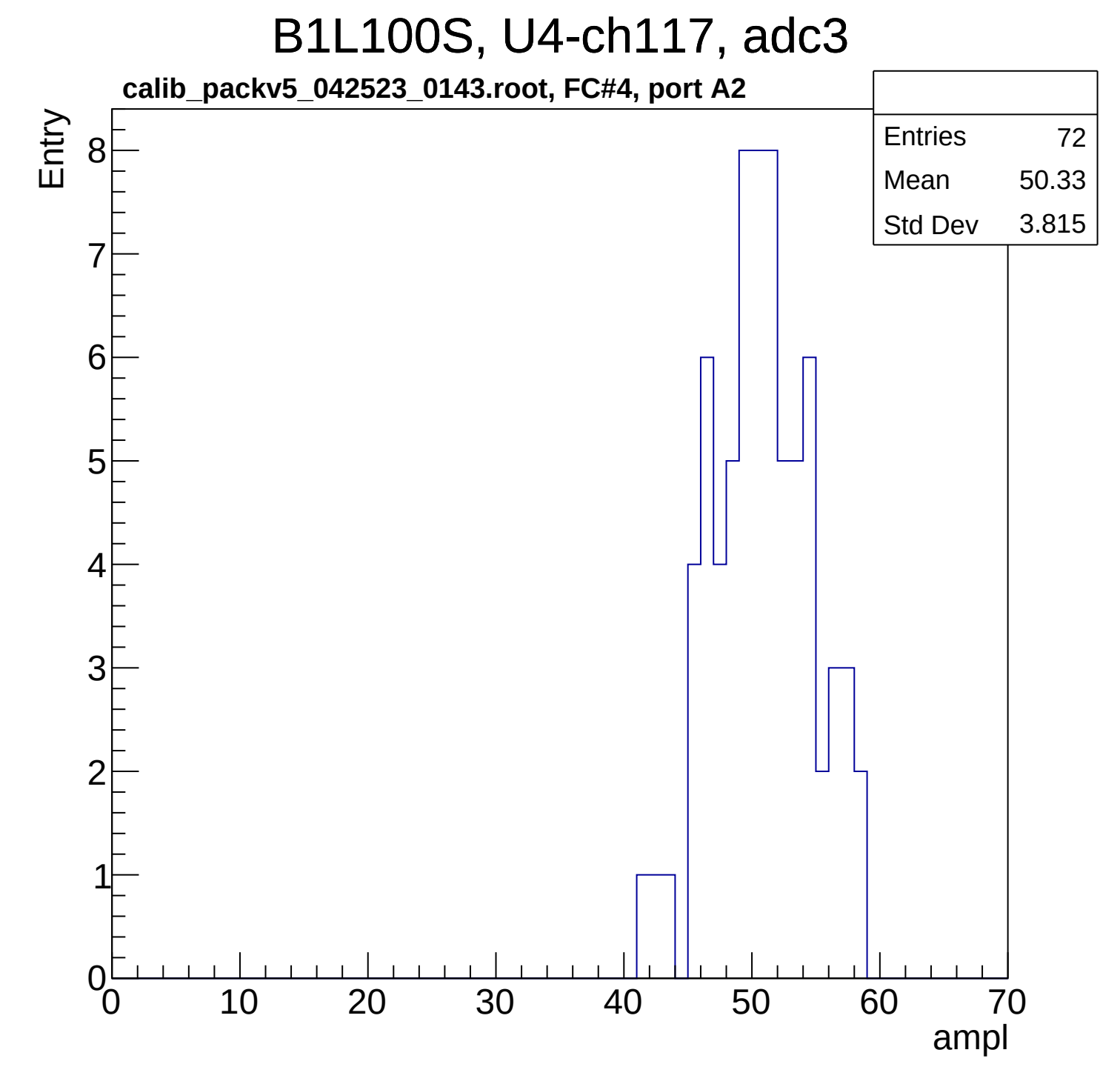

B1L100S, U4-ch116, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 61.83
Std Dev 1.067
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

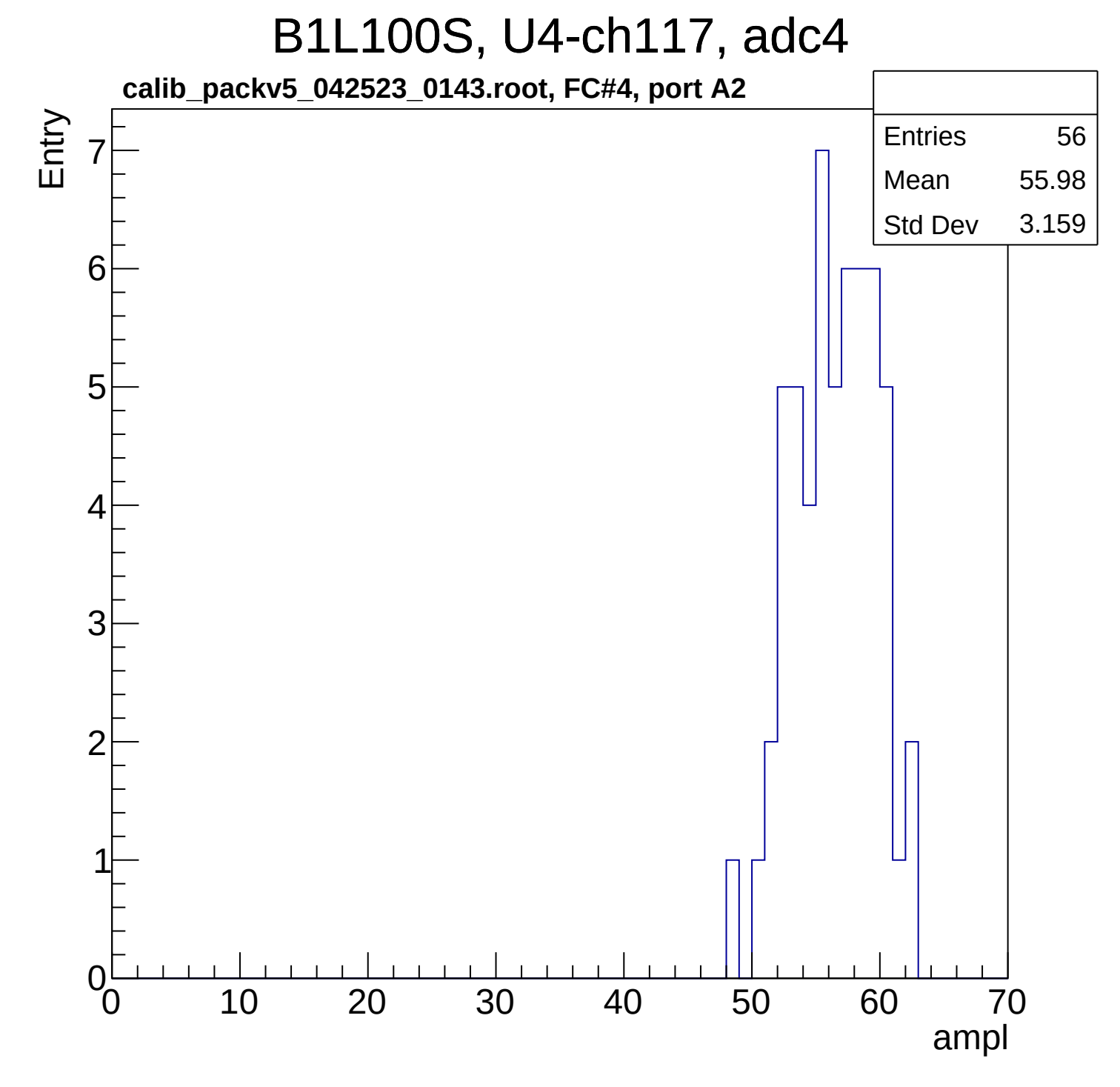

B1L100S, U4-ch116, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 0
Std Dev 0
Entry
3
2.5
2
1.5
1
0.5
0
0
10
20
30
40
50
60
70
ampl

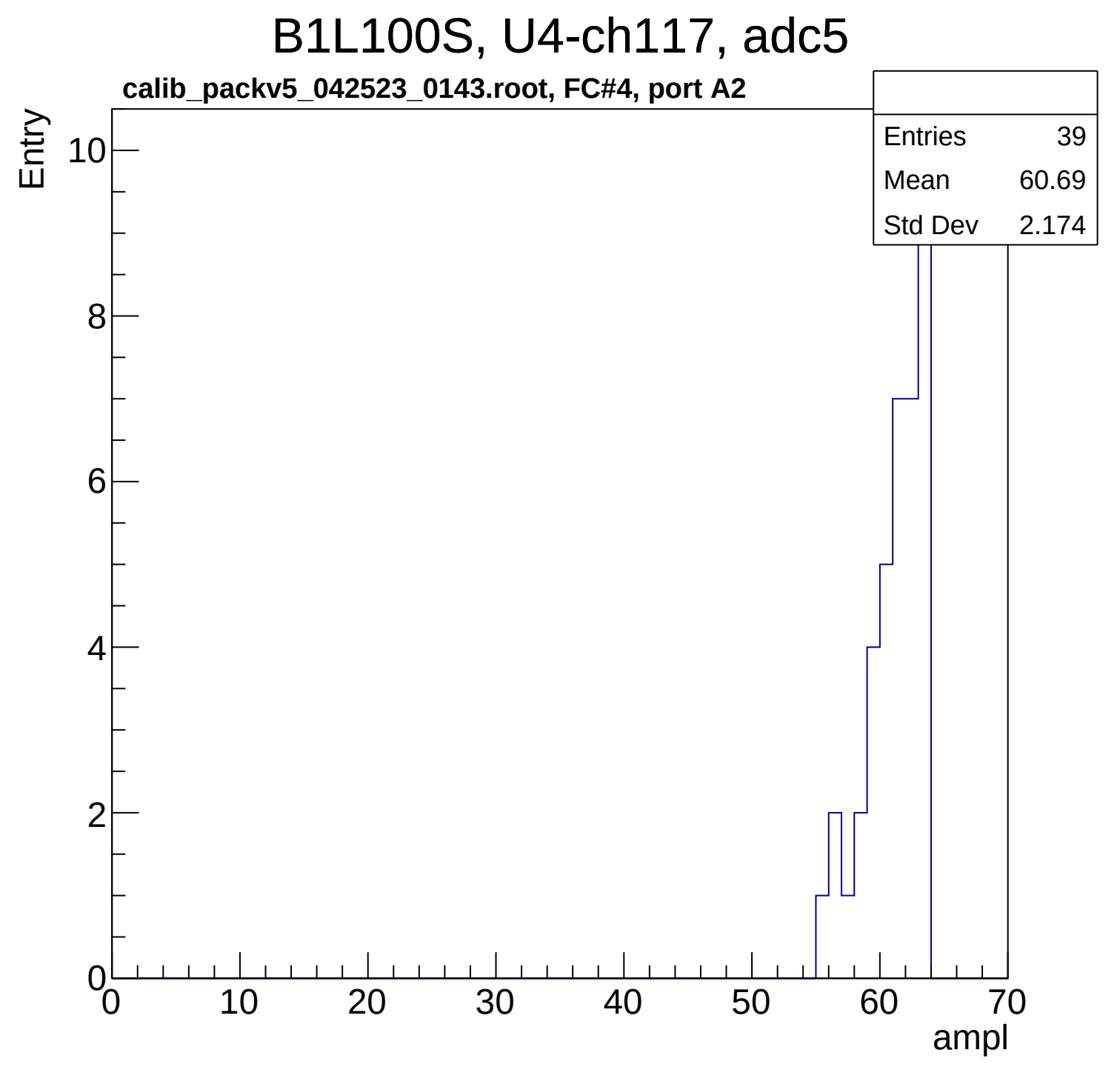

B1L100S, U4-ch117, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 29.43
Std Dev 3.792
Gaus mean : 30.2484
Gaus Width: 4.1020
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

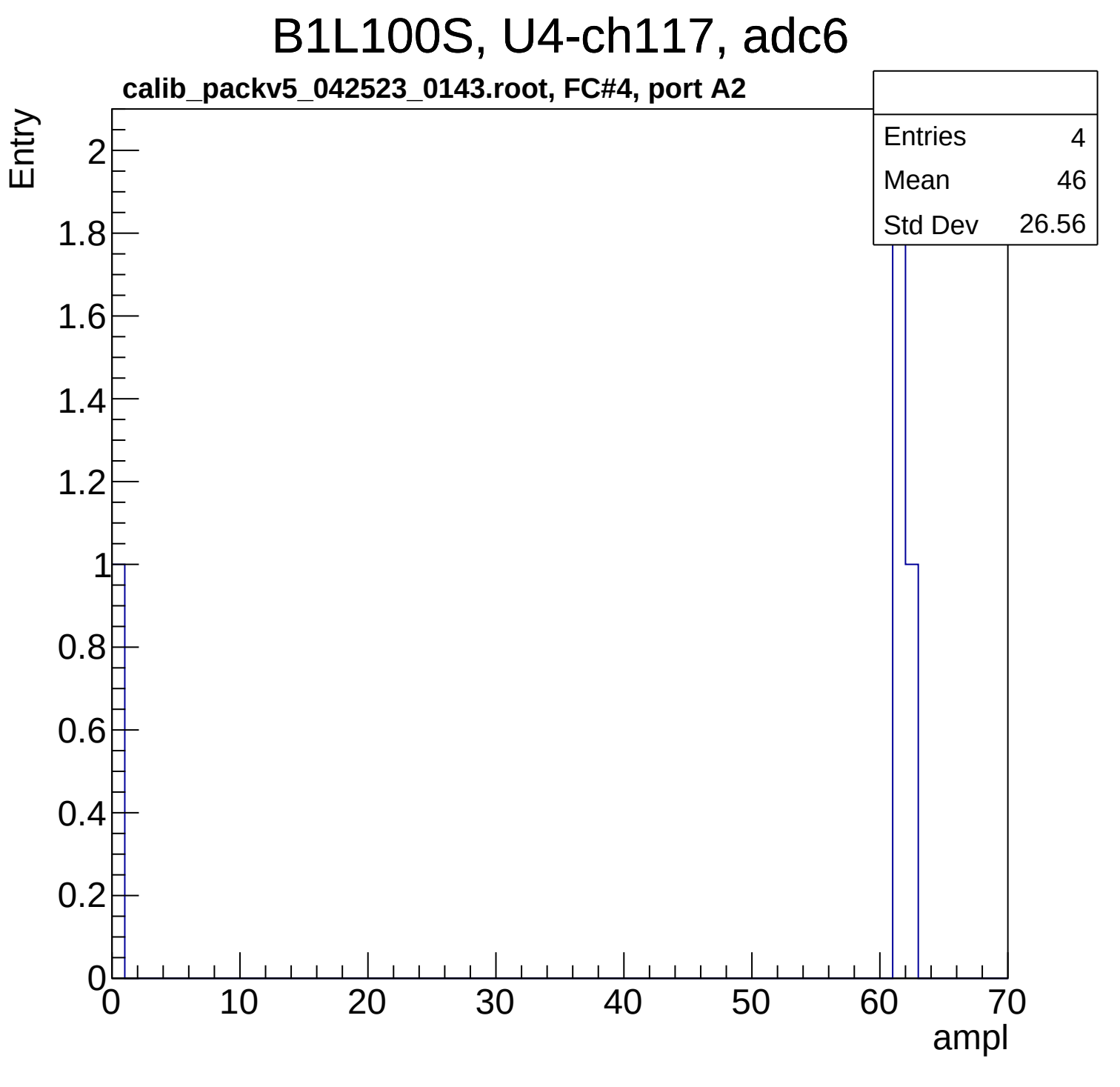

B1L100S, U4-ch117, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 37.51
Std Dev 4.129
Gaus mean : 38.0004
Gaus Width: 4.2878
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

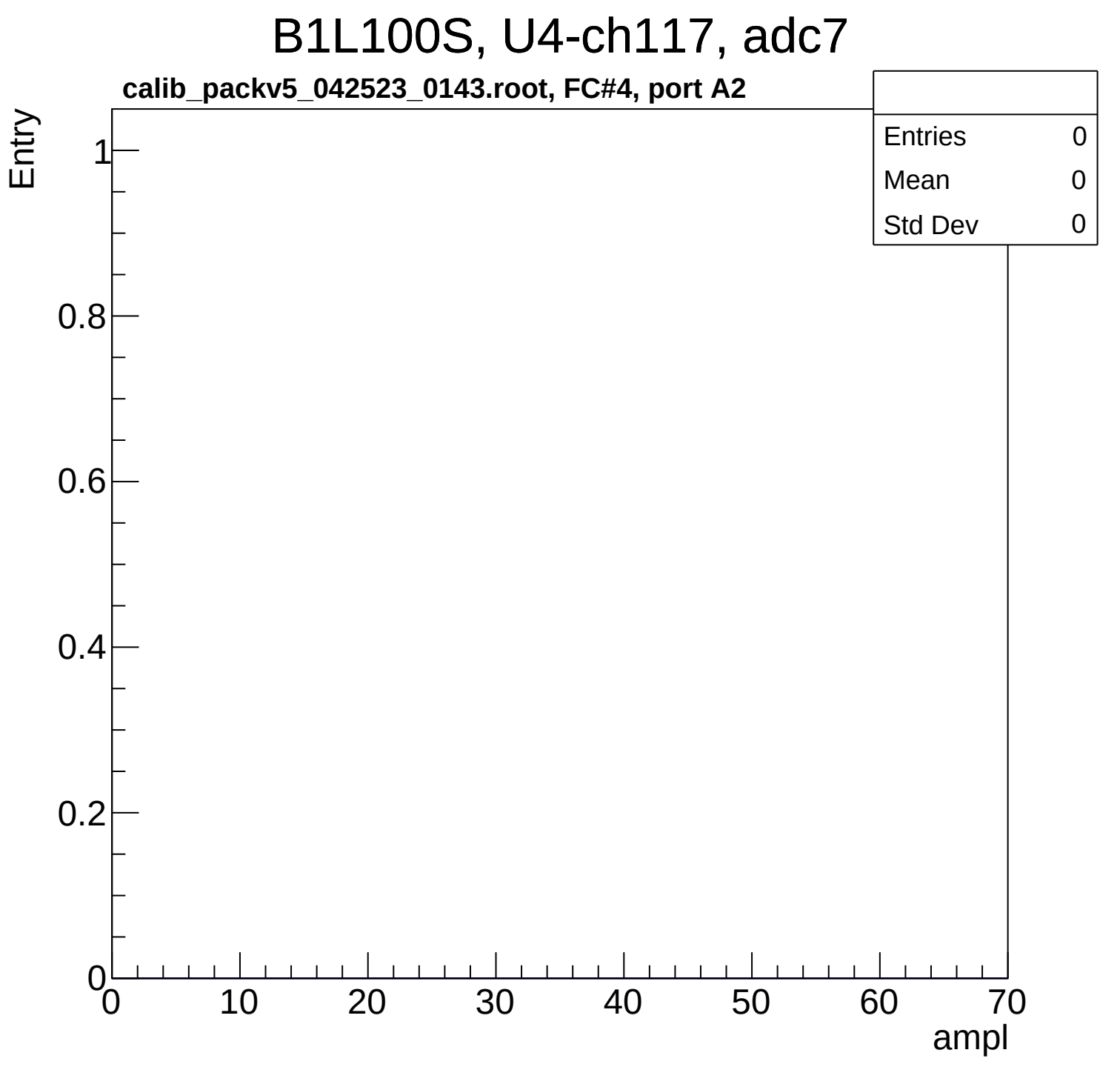

B1L100S, U4-ch117, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 43
Std Dev 3.554
Gaus mean : 43.3093
Gaus Width: 4.3201
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

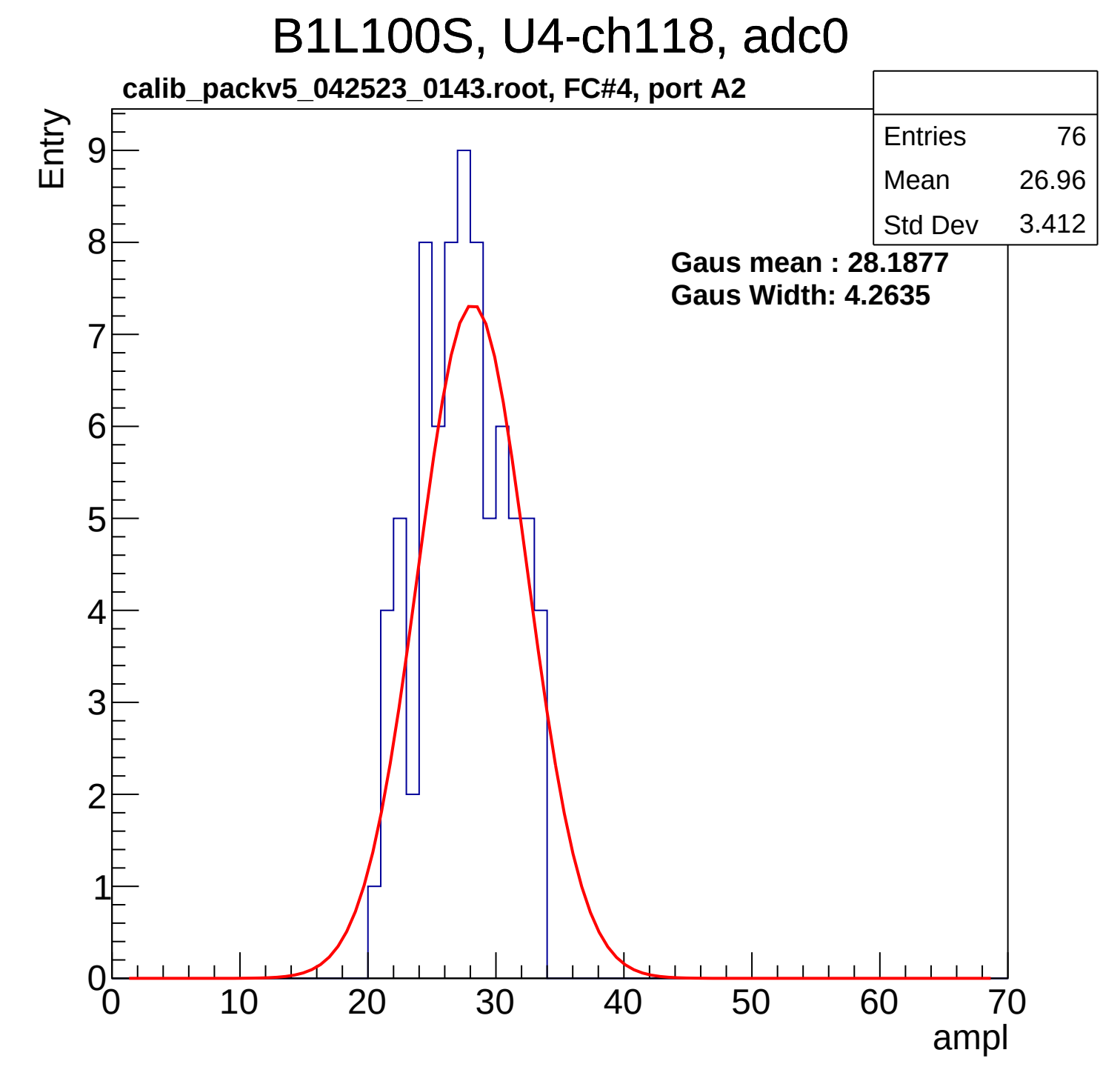

B1L100S, U4-ch117, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 50.33
Std Dev 3.815
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

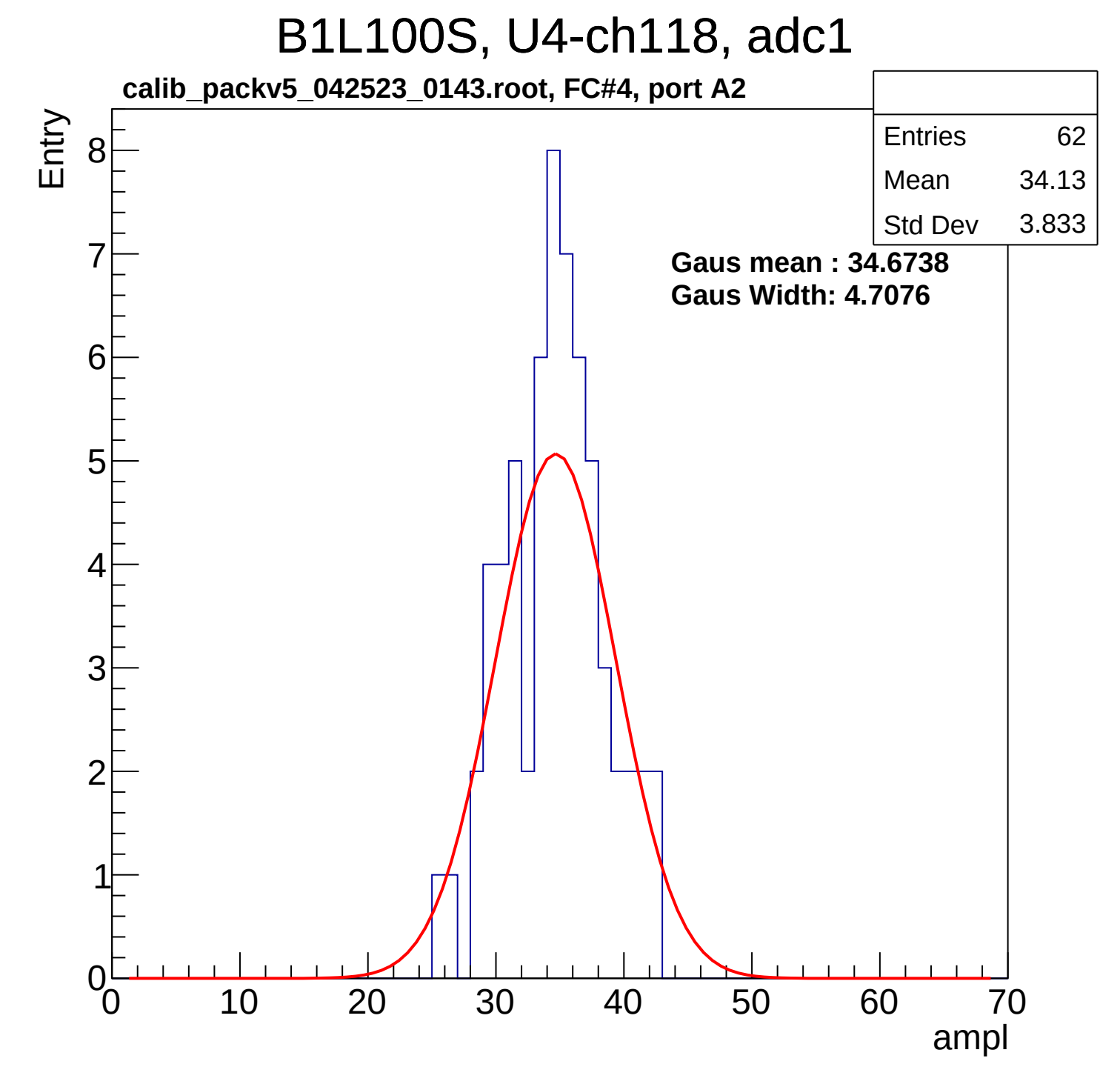

B1L100S, U4-ch117, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 55.98
Std Dev 3.159
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

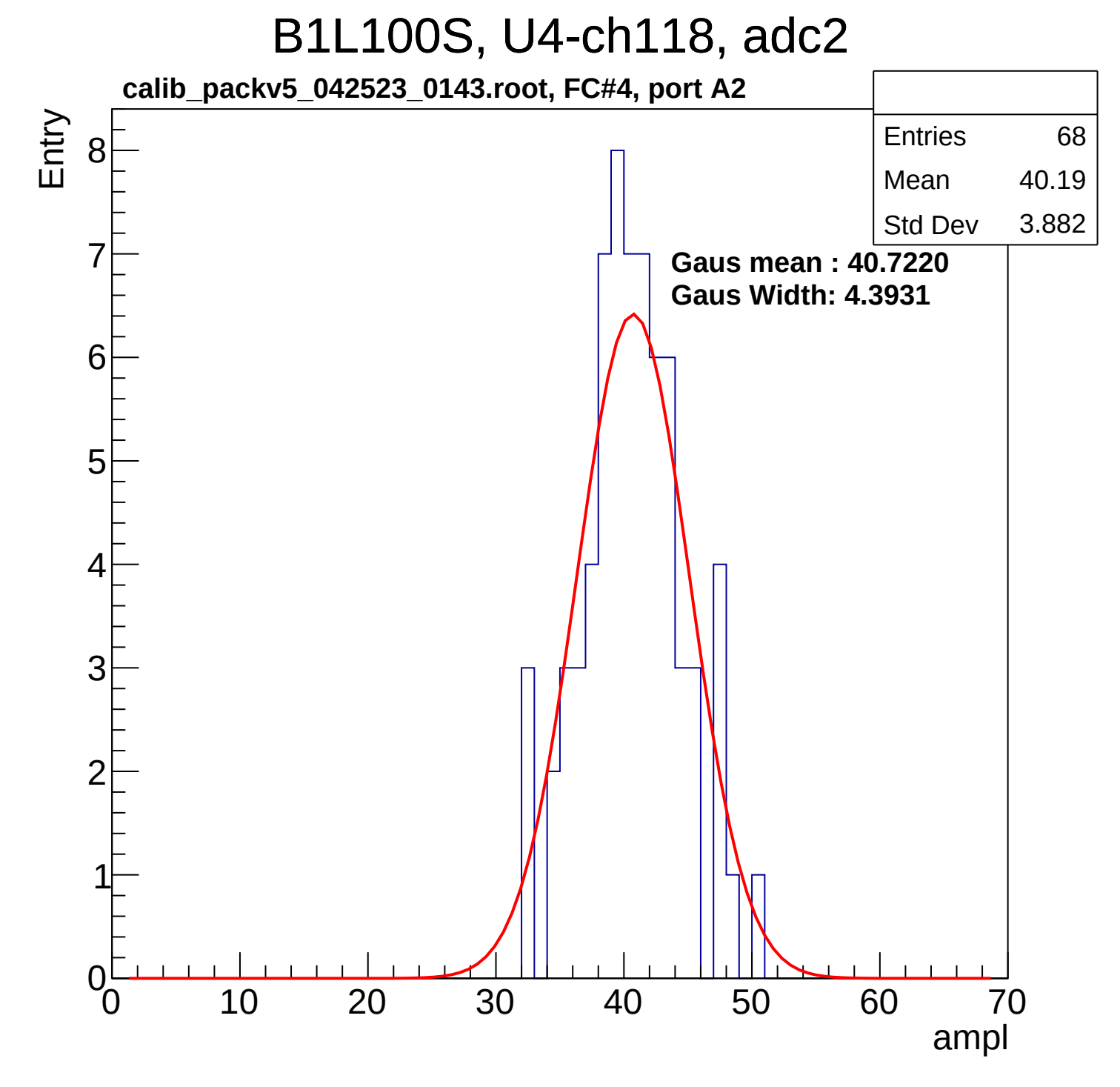

B1L100S, U4-ch117, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 39
Mean 60.69
Std Dev 2.174
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

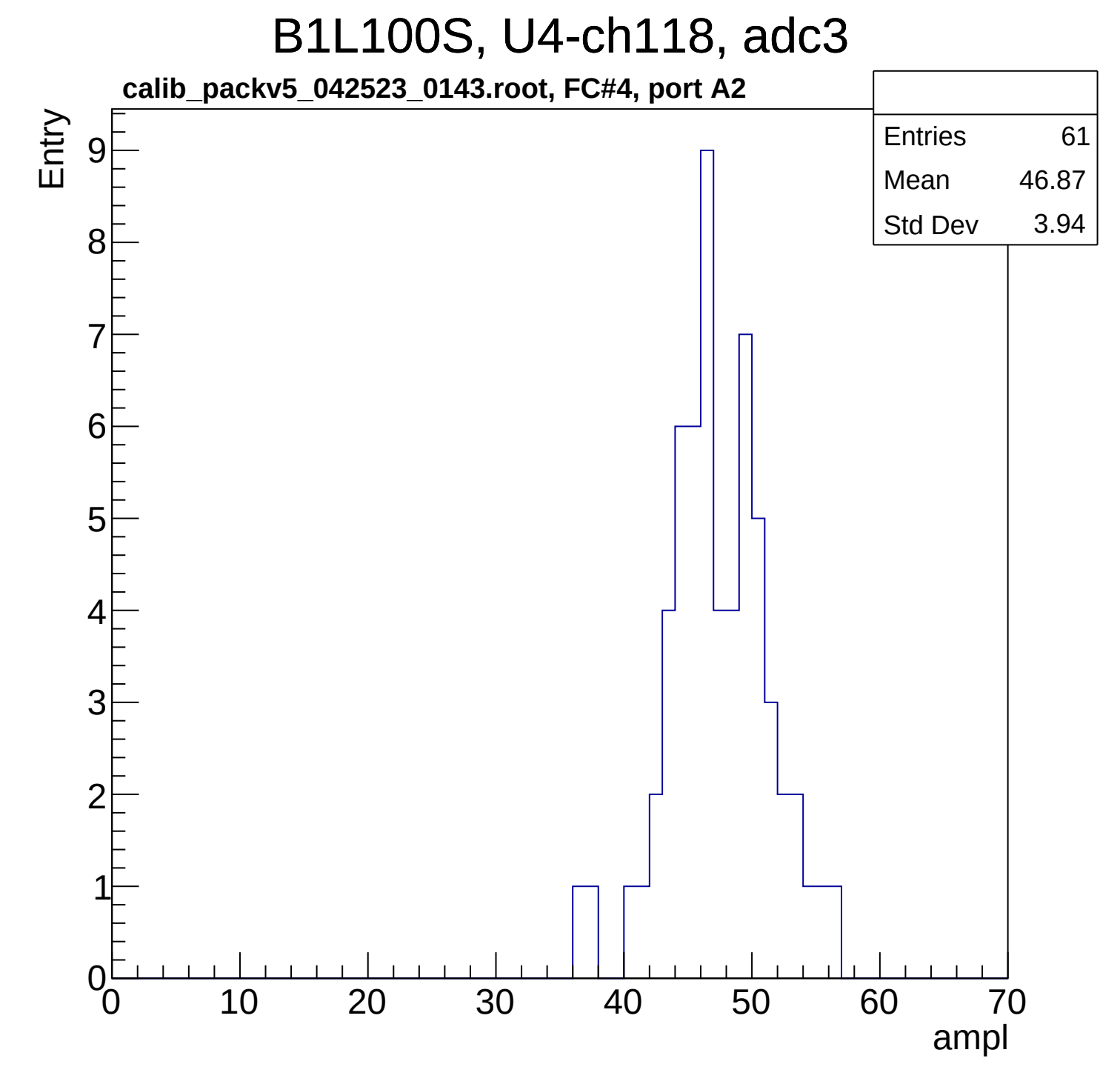

B1L100S, U4-ch117, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 46
Std Dev 26.56
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

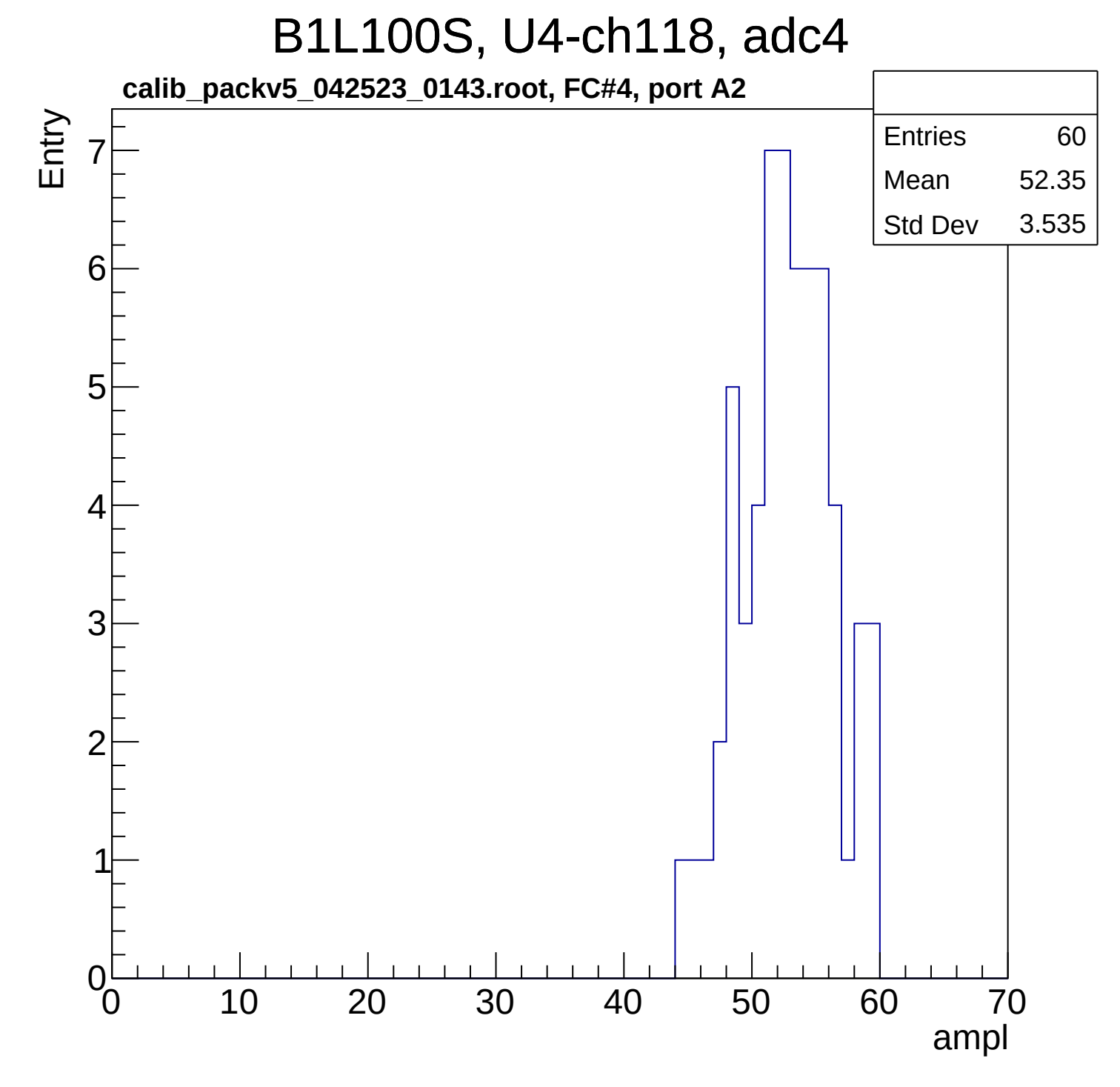

B1L100S, U4-ch117, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

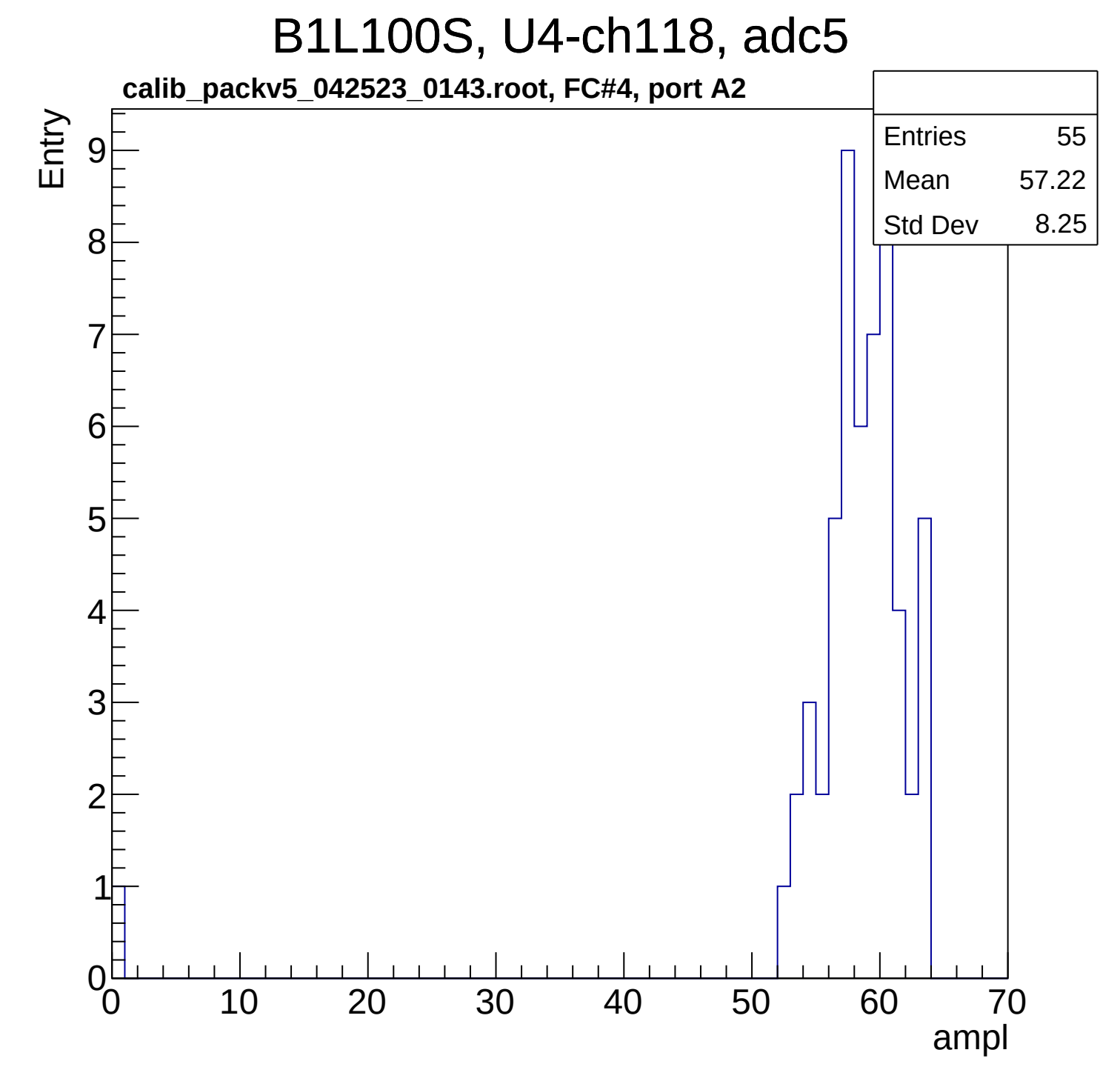

B1L100S, U4-ch118, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 26.96
Std Dev 3.412
Gaus mean : 28.1877
Gaus Width: 4.2635
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

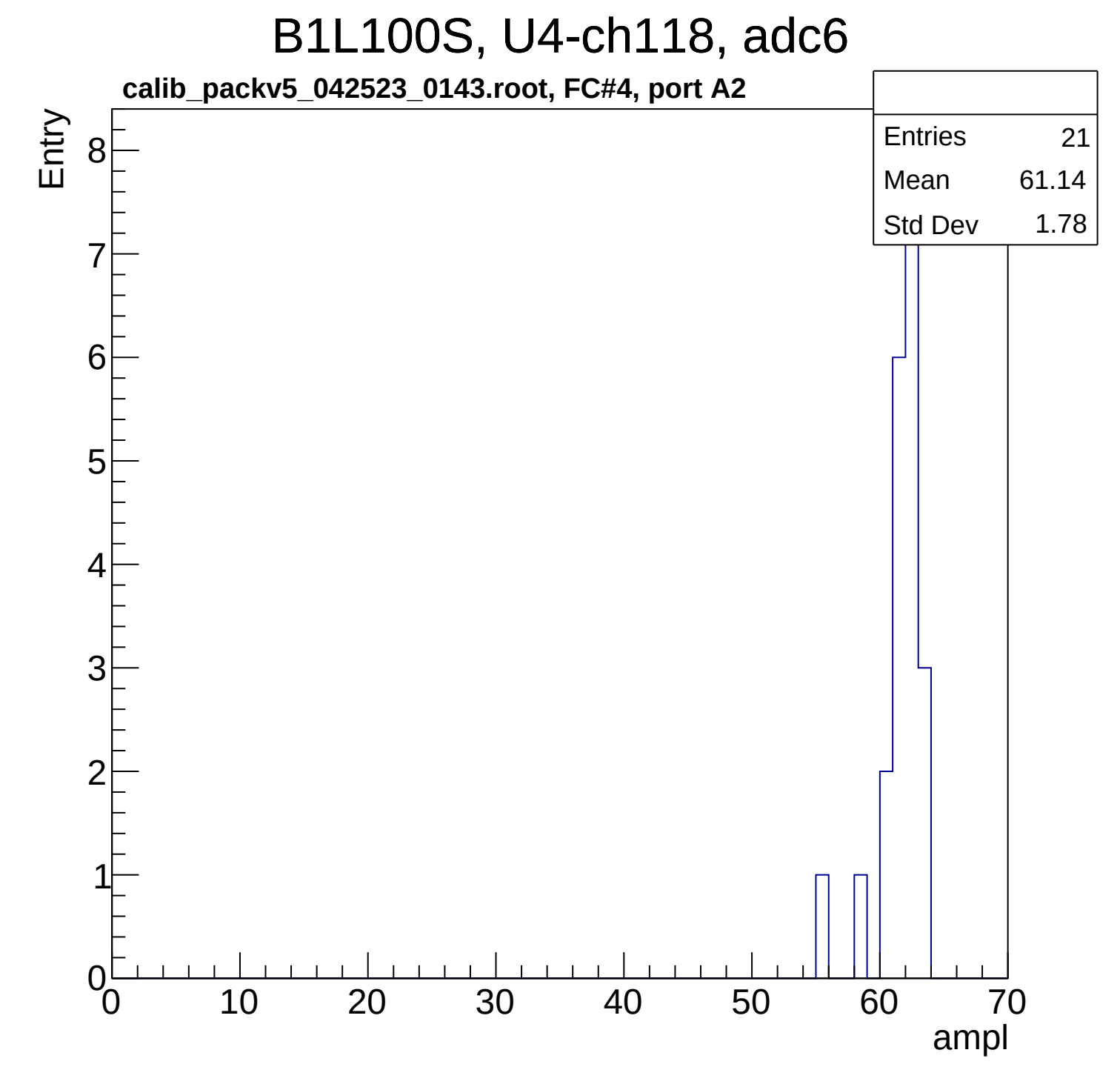

B1L100S, U4-ch118, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 34.13
Std Dev 3.833
Gaus mean : 34.6738
Gaus Width: 4.7076
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

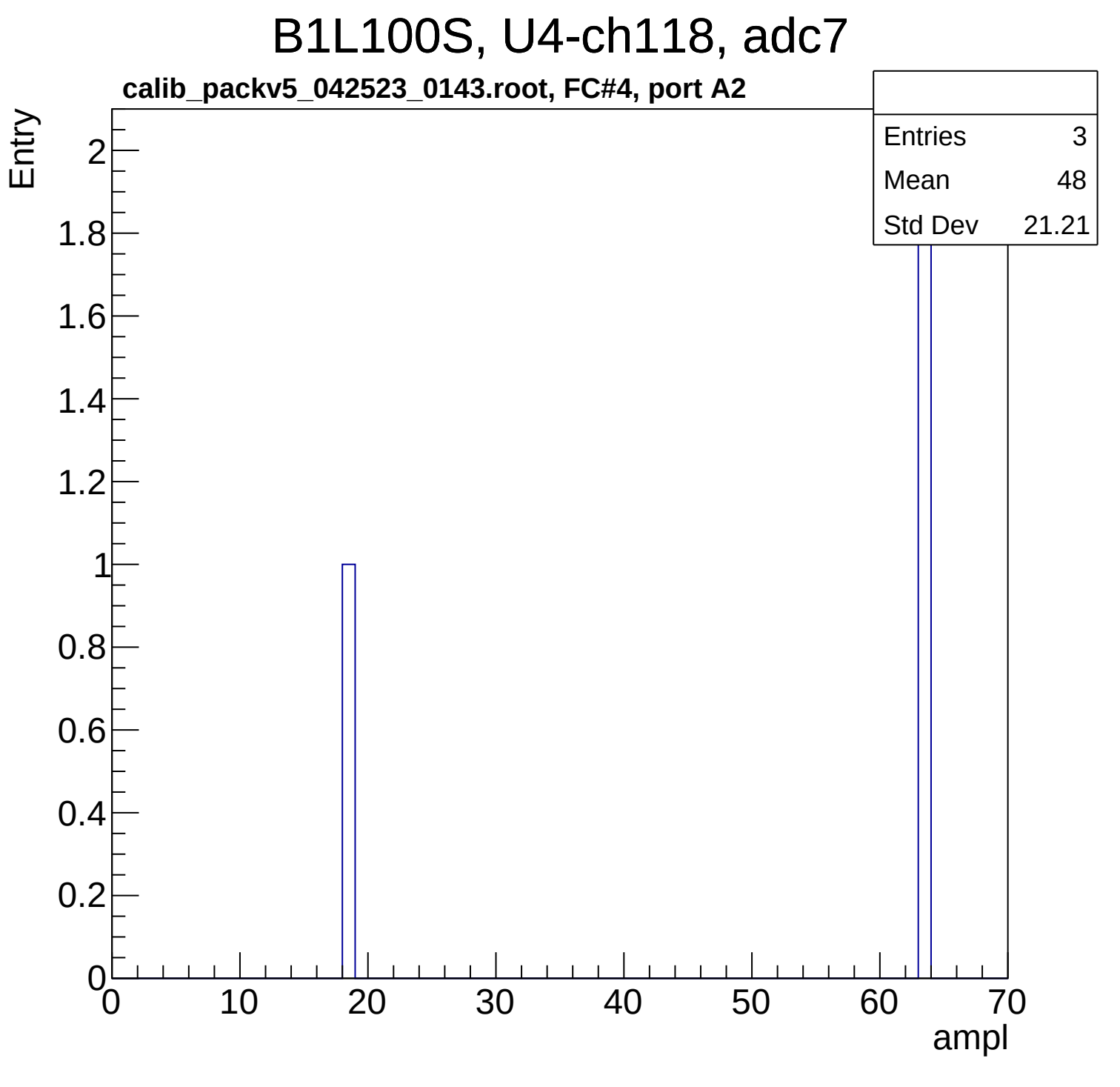

B1L100S, U4-ch118, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 40.19
Std Dev 3.882
Gaus mean : 40.7220
Gaus Width: 4.3931
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

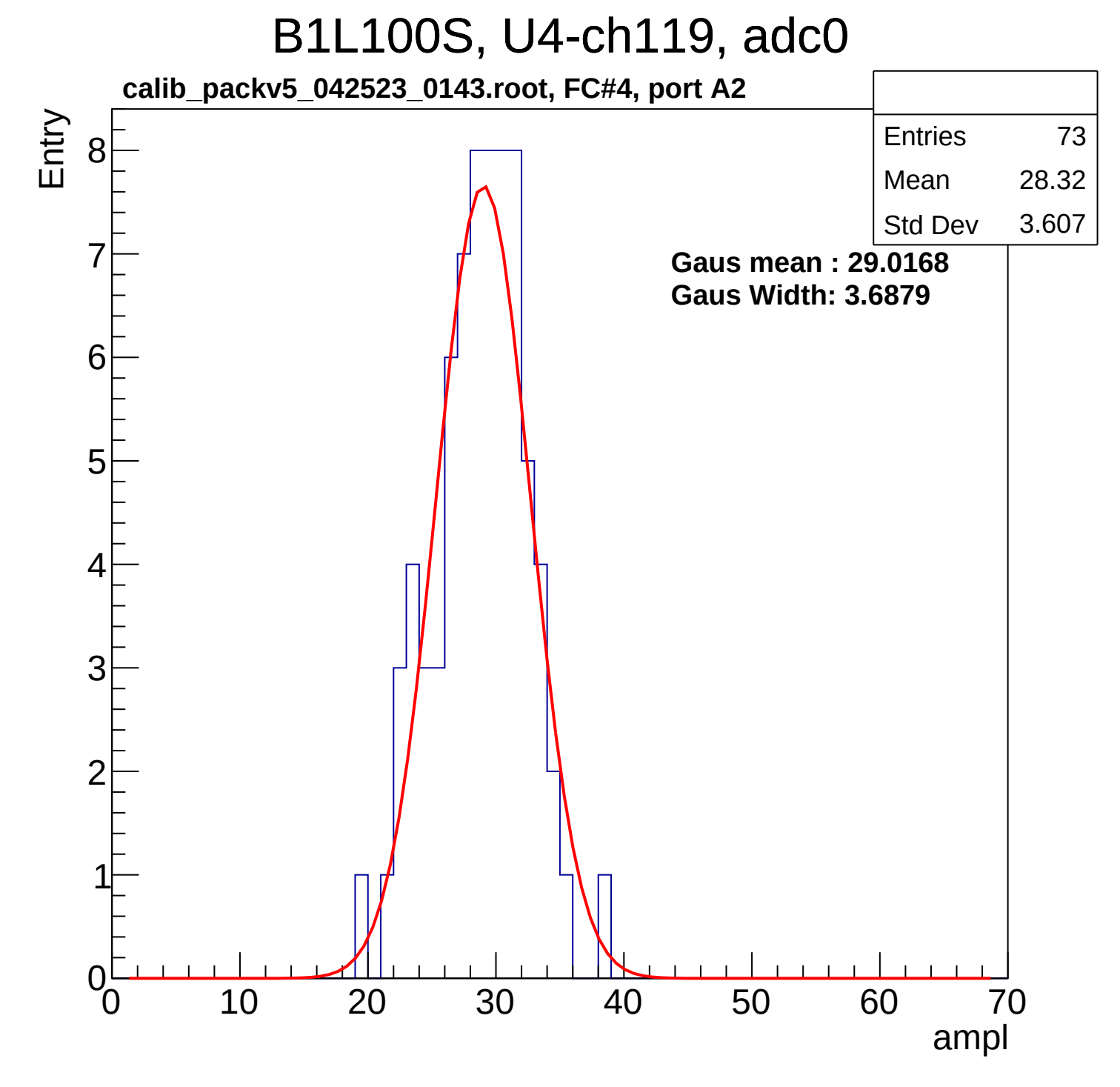

B1L100S, U4-ch118, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 46.87
Std Dev 3.94
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

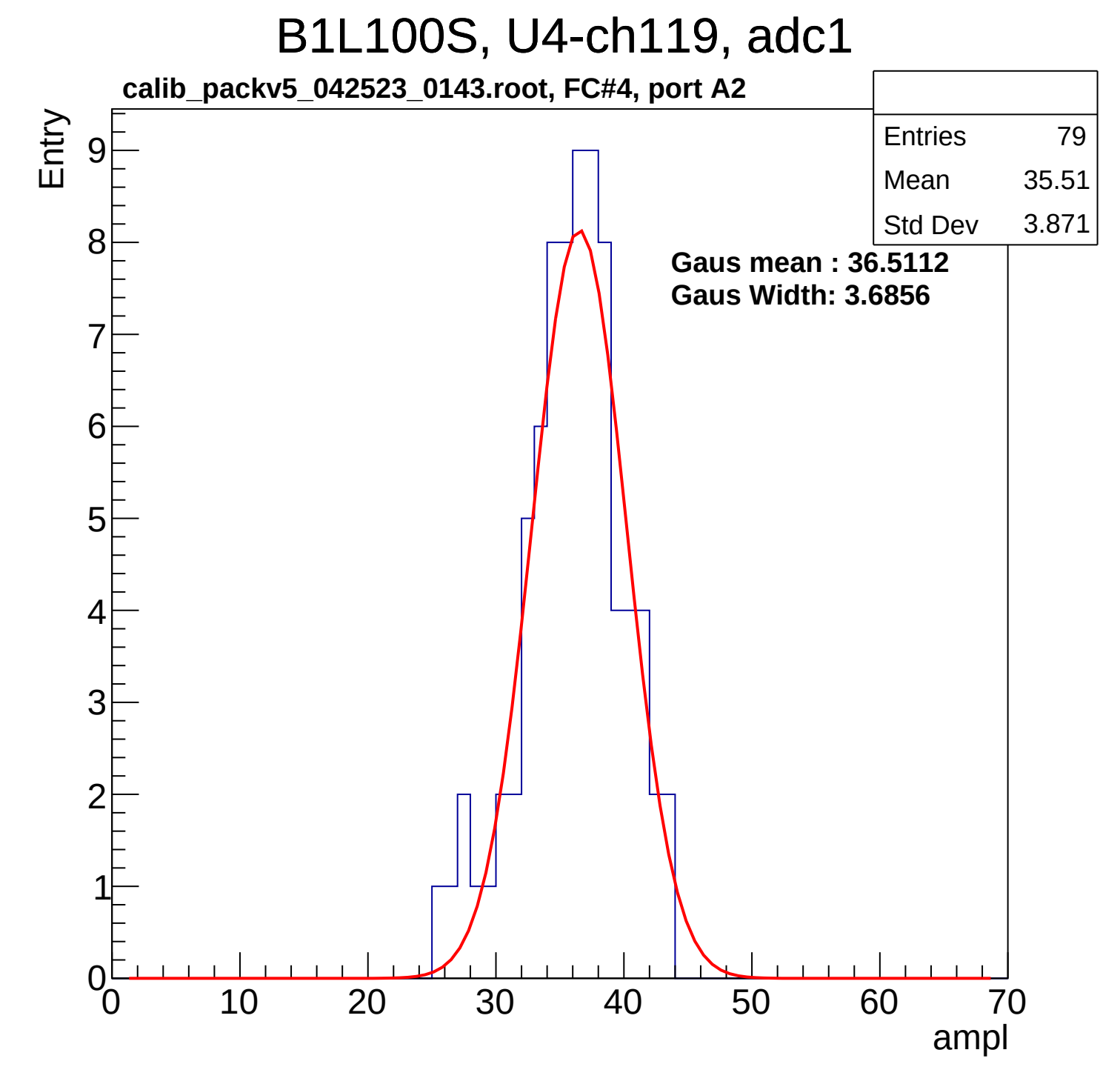

B1L100S, U4-ch118, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 52.35
Std Dev 3.535
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

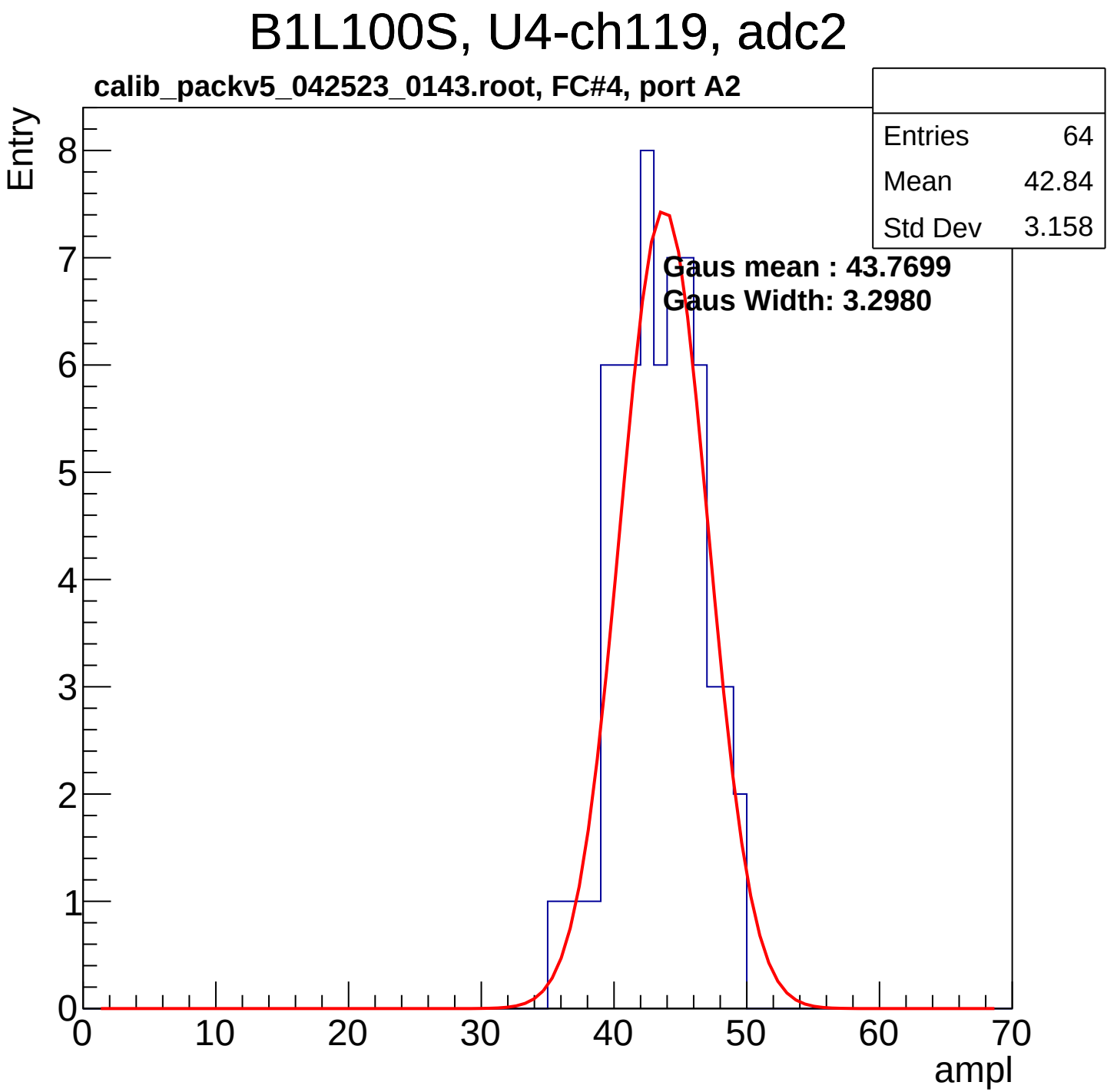

B1L100S, U4-ch118, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 57.22
Std Dev 8.25
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

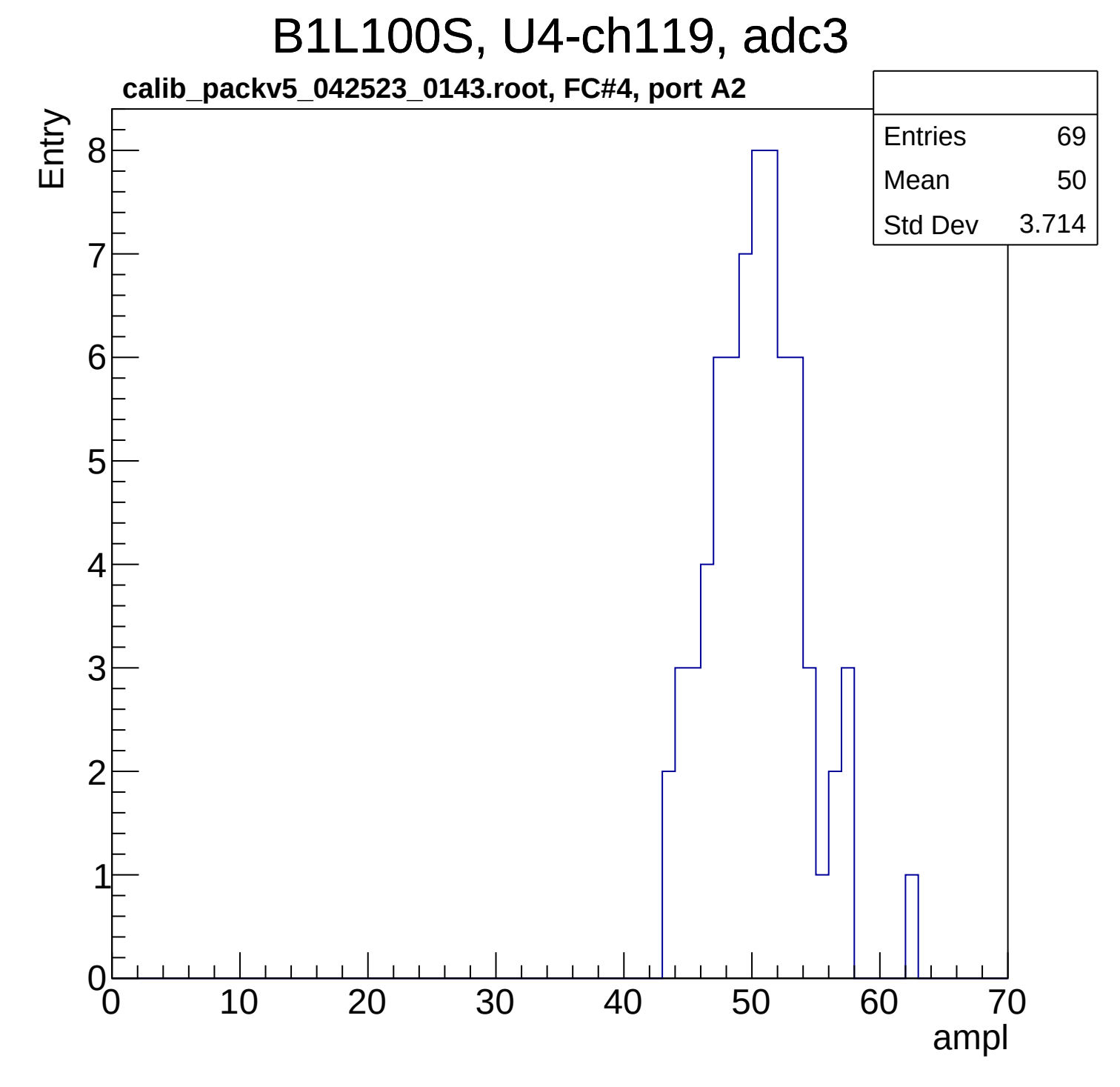

B1L100S, U4-ch118, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 21
Mean 61.14
Std Dev 1.78
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

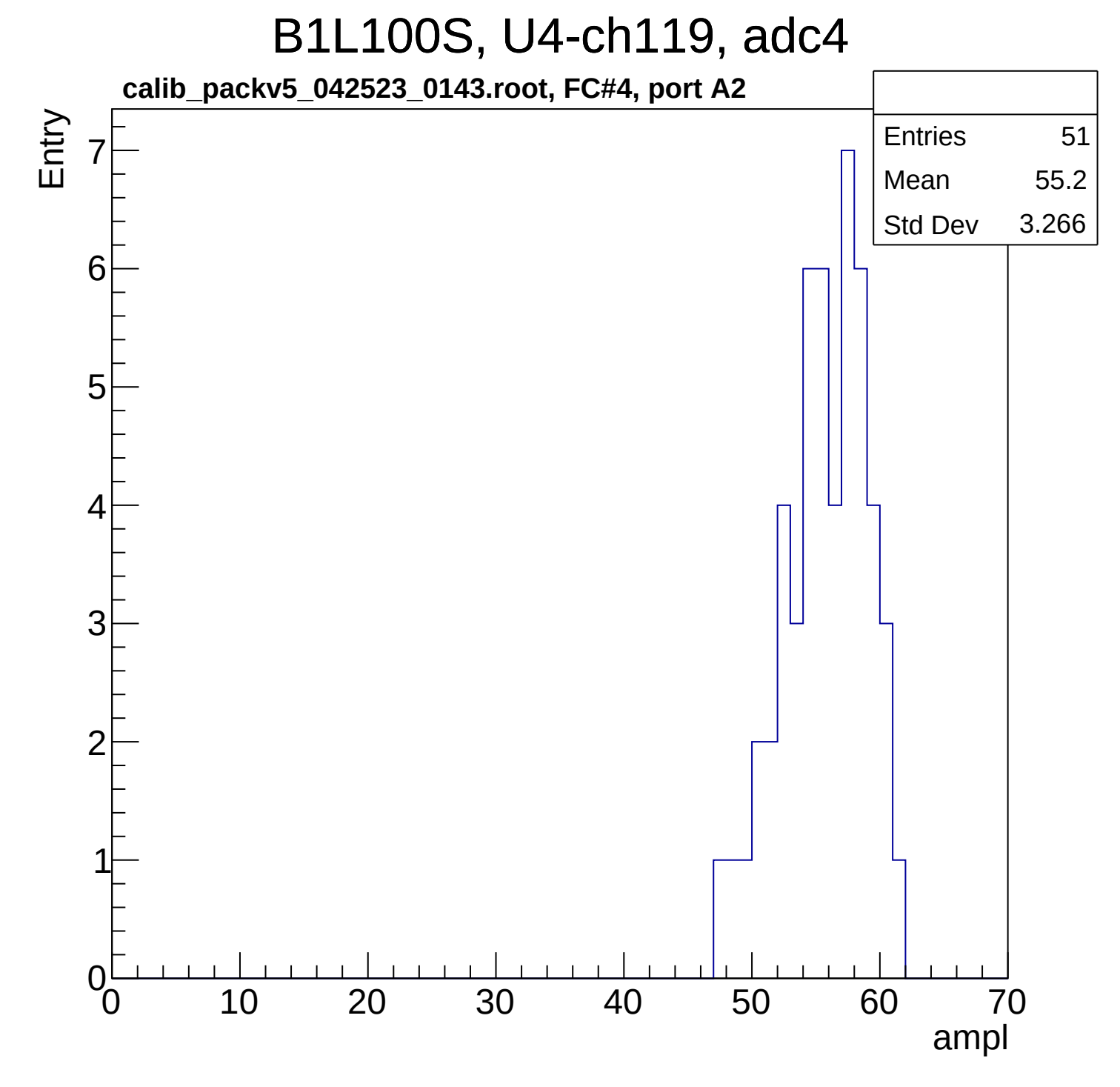

B1L100S, U4-ch118, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 48
Std Dev 21.21
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

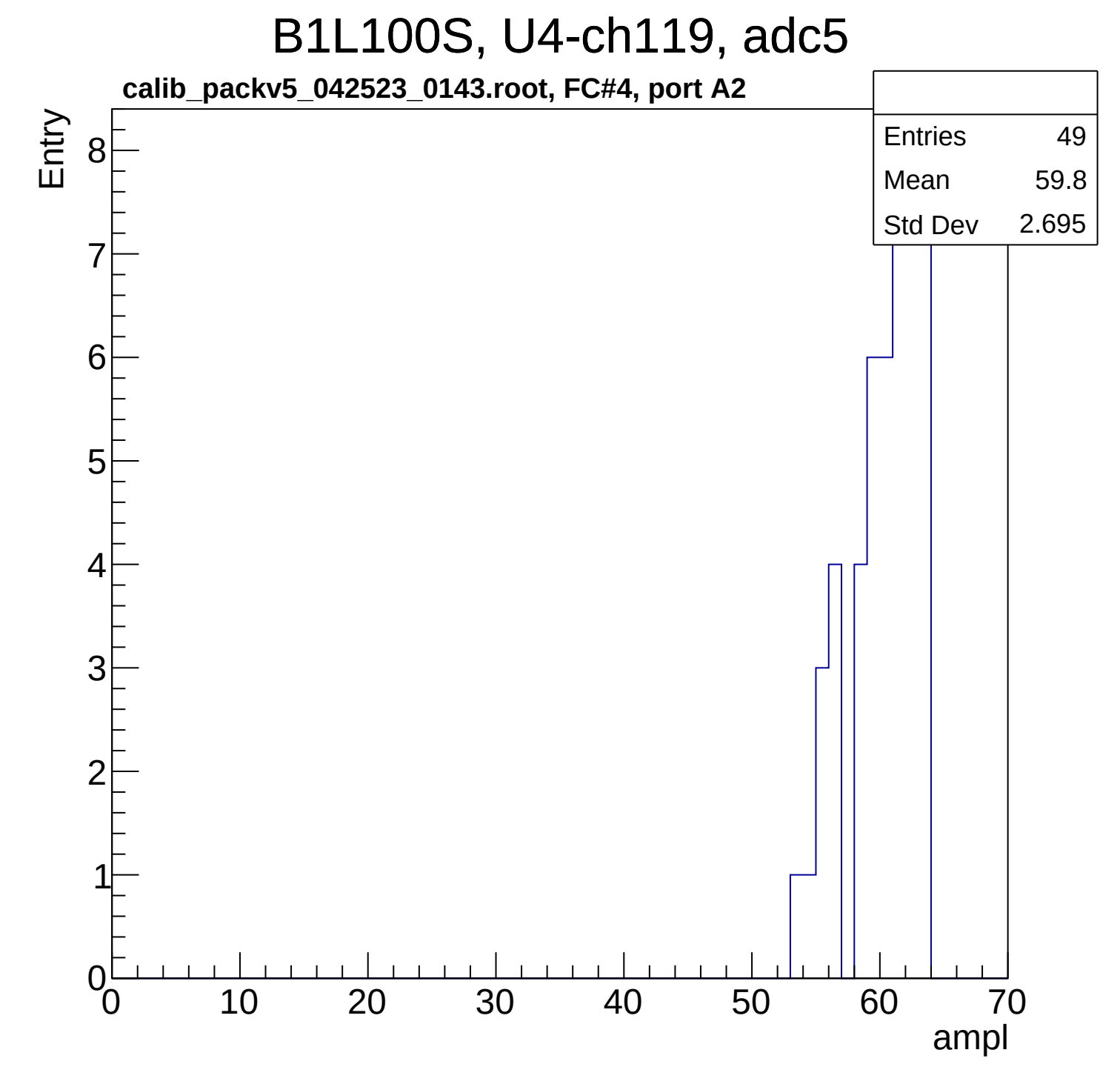

B1L100S, U4-ch119, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 28.32
Std Dev 3.607
Gaus mean : 29.0168
Gaus Width: 3.6879
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

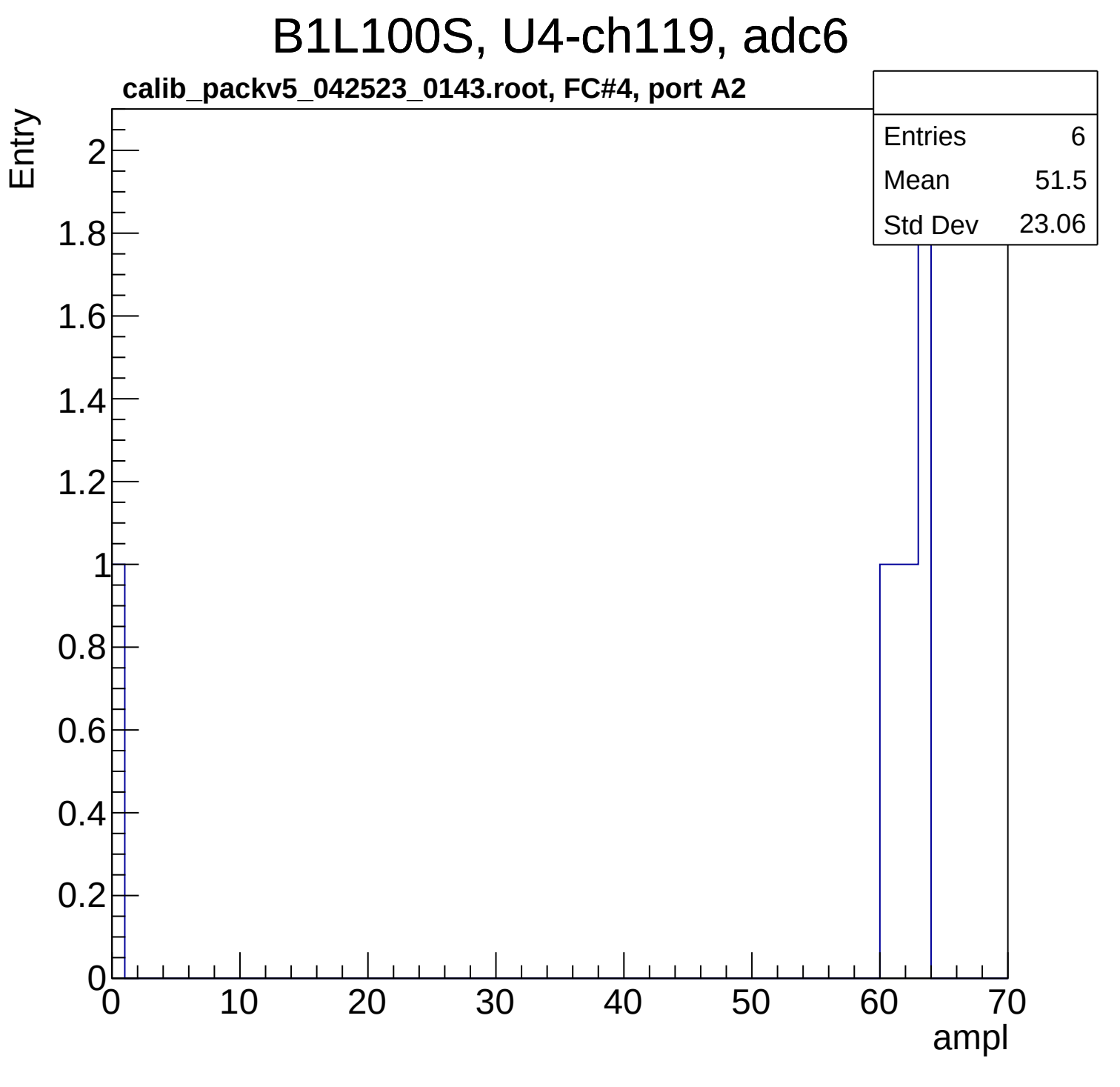

B1L100S, U4-ch119, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 35.51
Std Dev 3.871
Gaus mean : 36.5112
Gaus Width: 3.6856
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

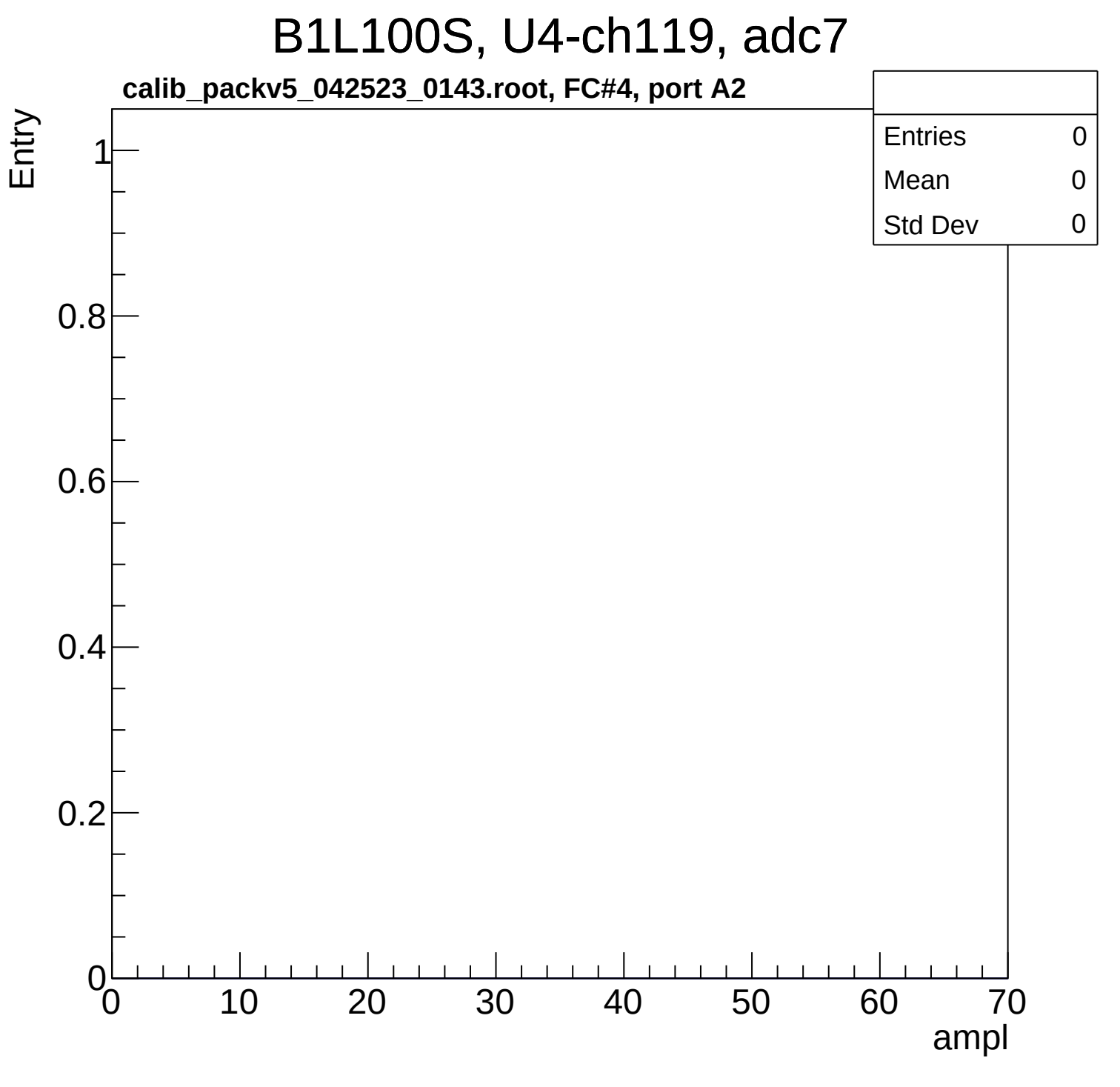

B1L100S, U4-ch119, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 42.84
Std Dev 3.158
Gaus mean : 43.7699
Gaus Width: 3.2980
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

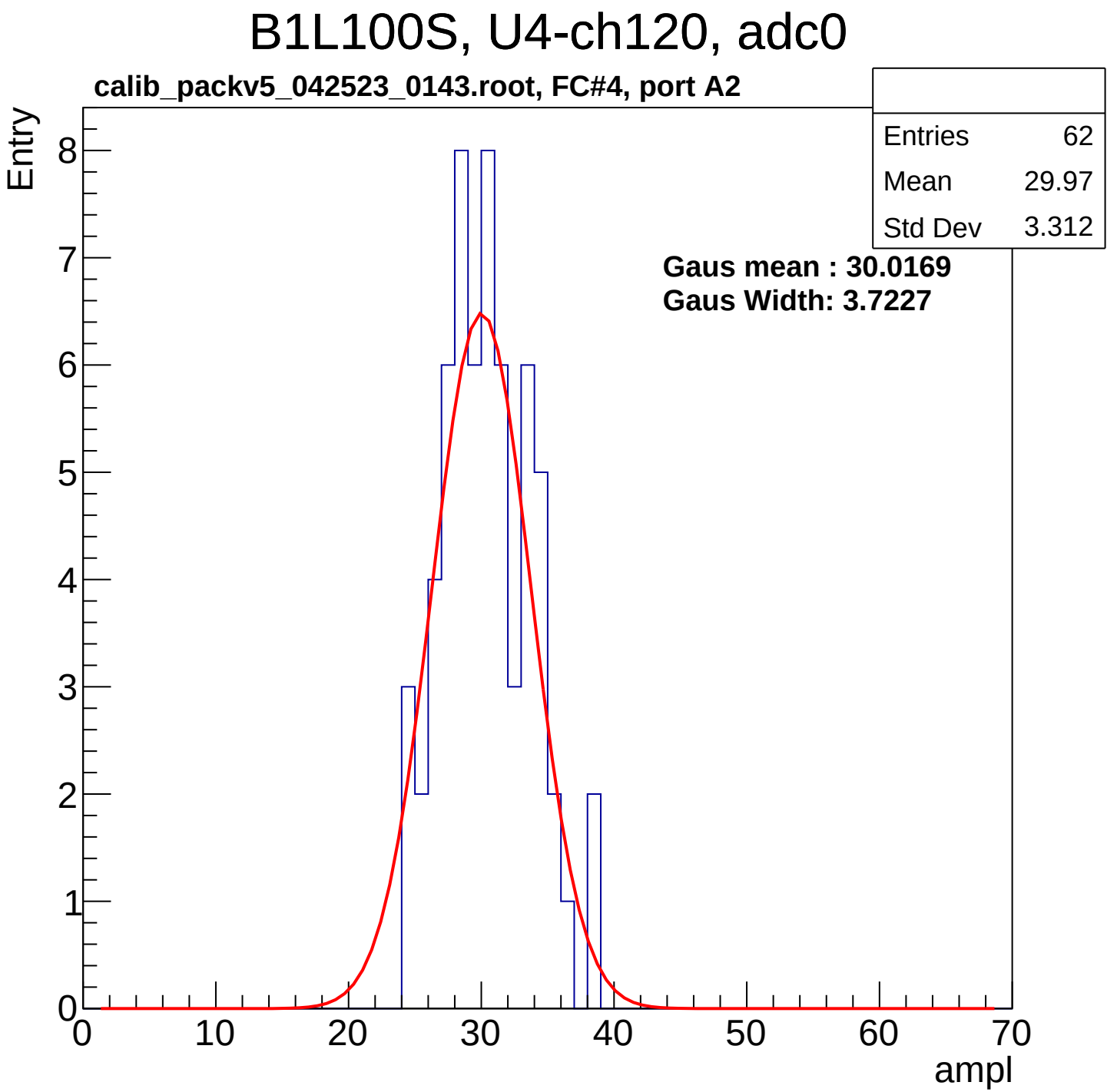

B1L100S, U4-ch119, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 50
Std Dev 3.714
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

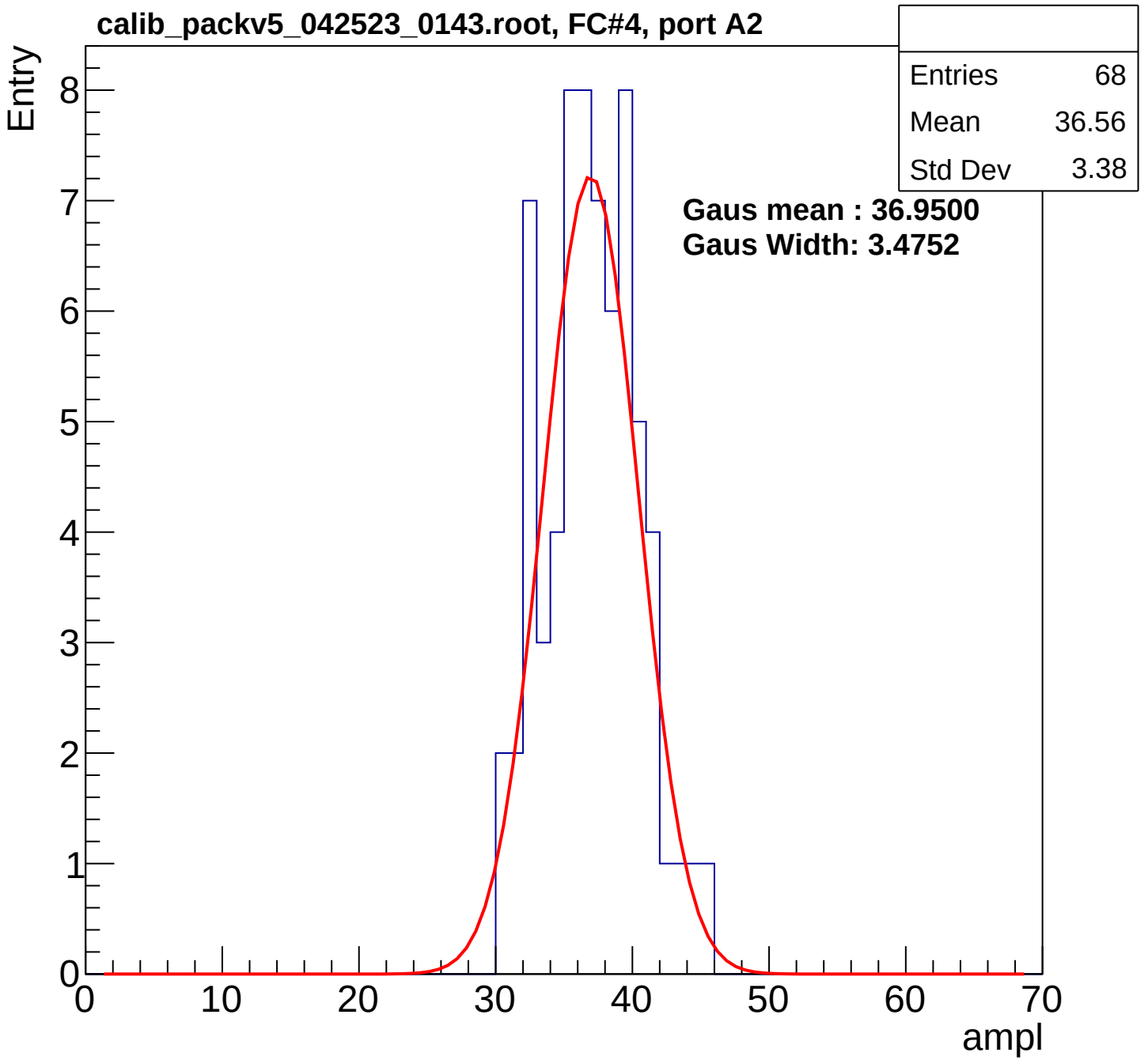

B1L100S, U4-ch119, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 55.2
Std Dev 3.266
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

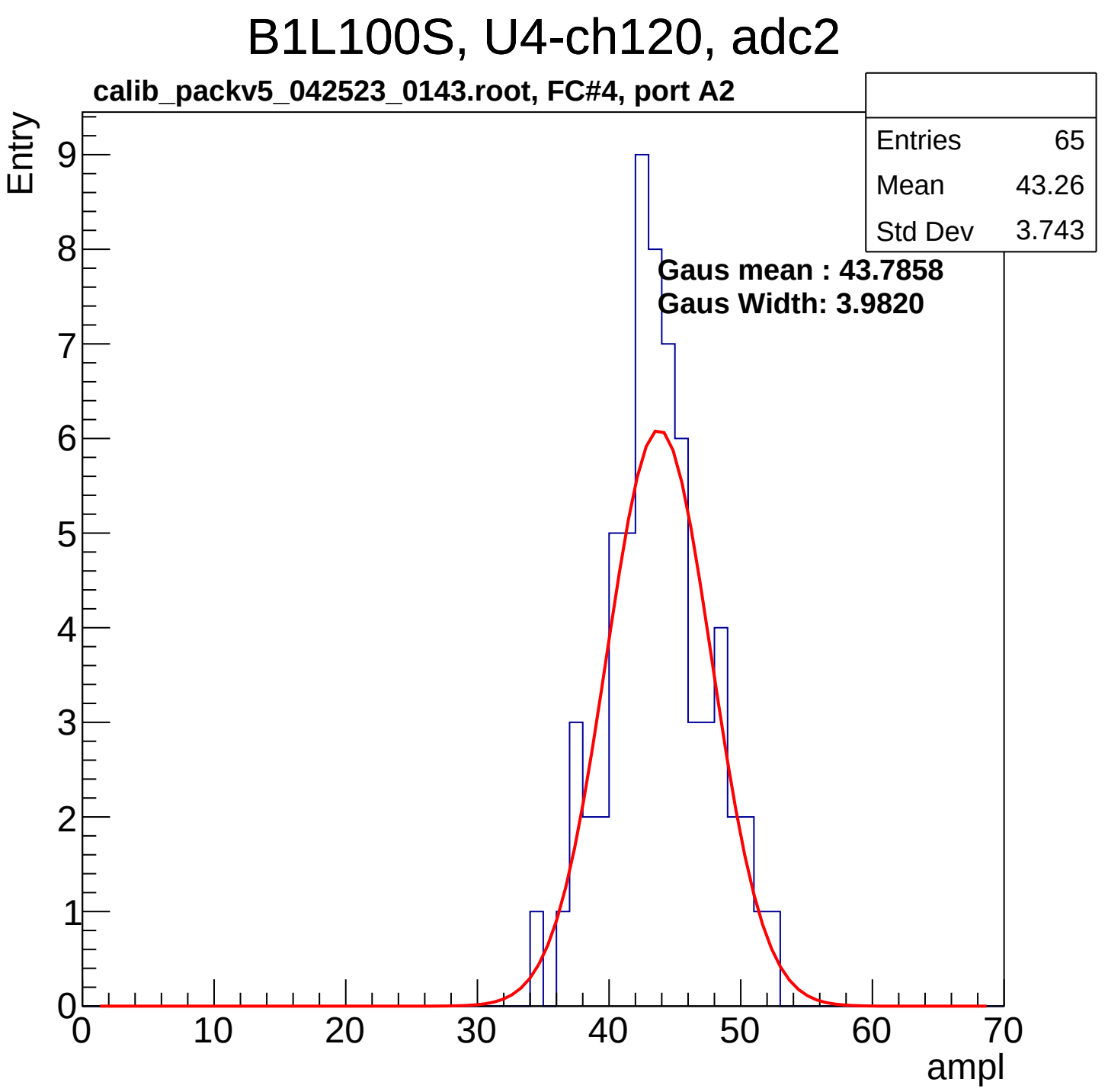

B1L100S, U4-ch119, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 59.8
Std Dev 2.695
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

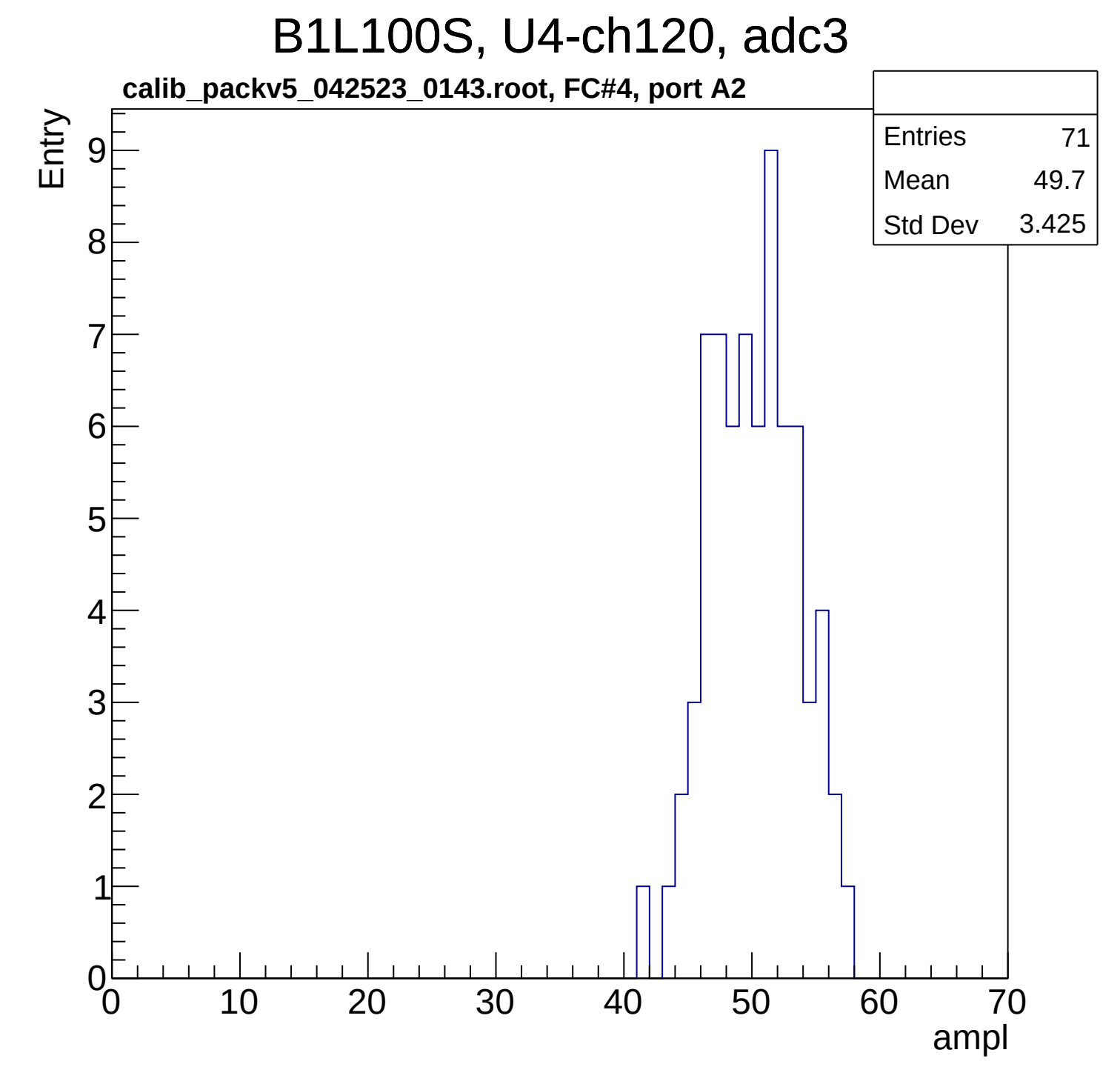

B1L100S, U4-ch119, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 51.5
Std Dev 23.06
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

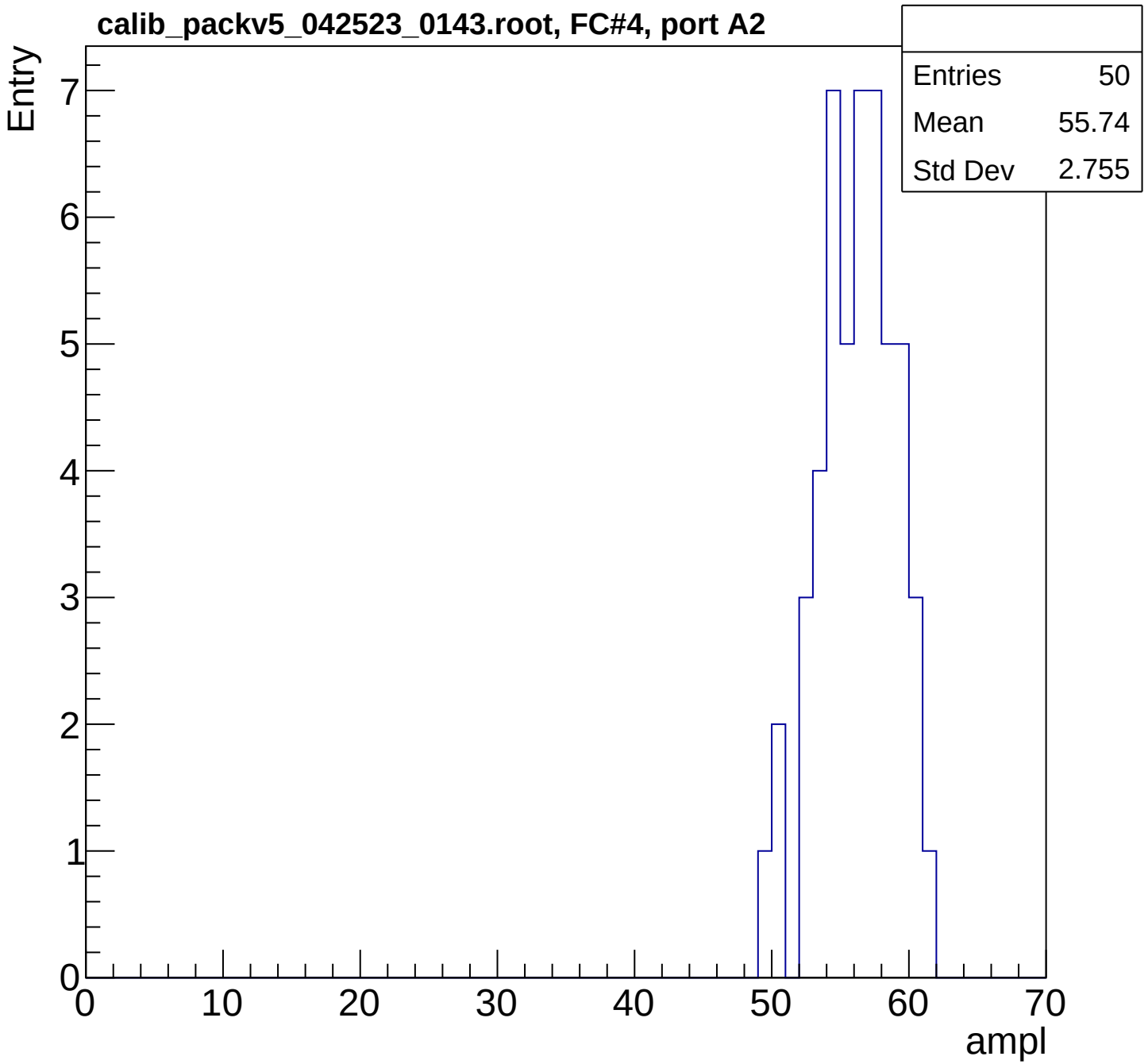

B1L100S, U4-ch119, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

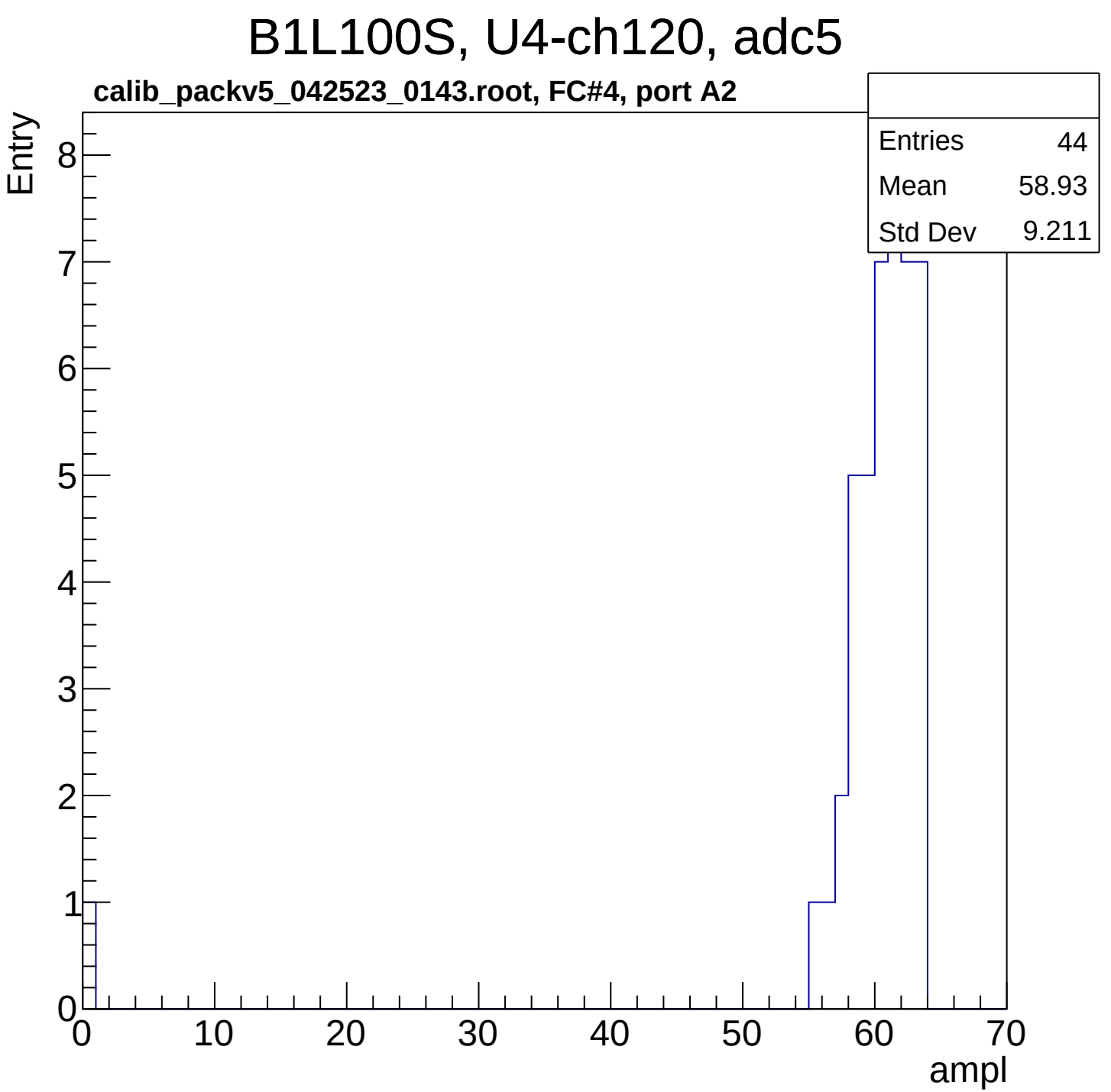

B1L100S, U4-ch120, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 29.97
Std Dev 3.312
Gaus mean : 30.0169
Gaus Width: 3.7227
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

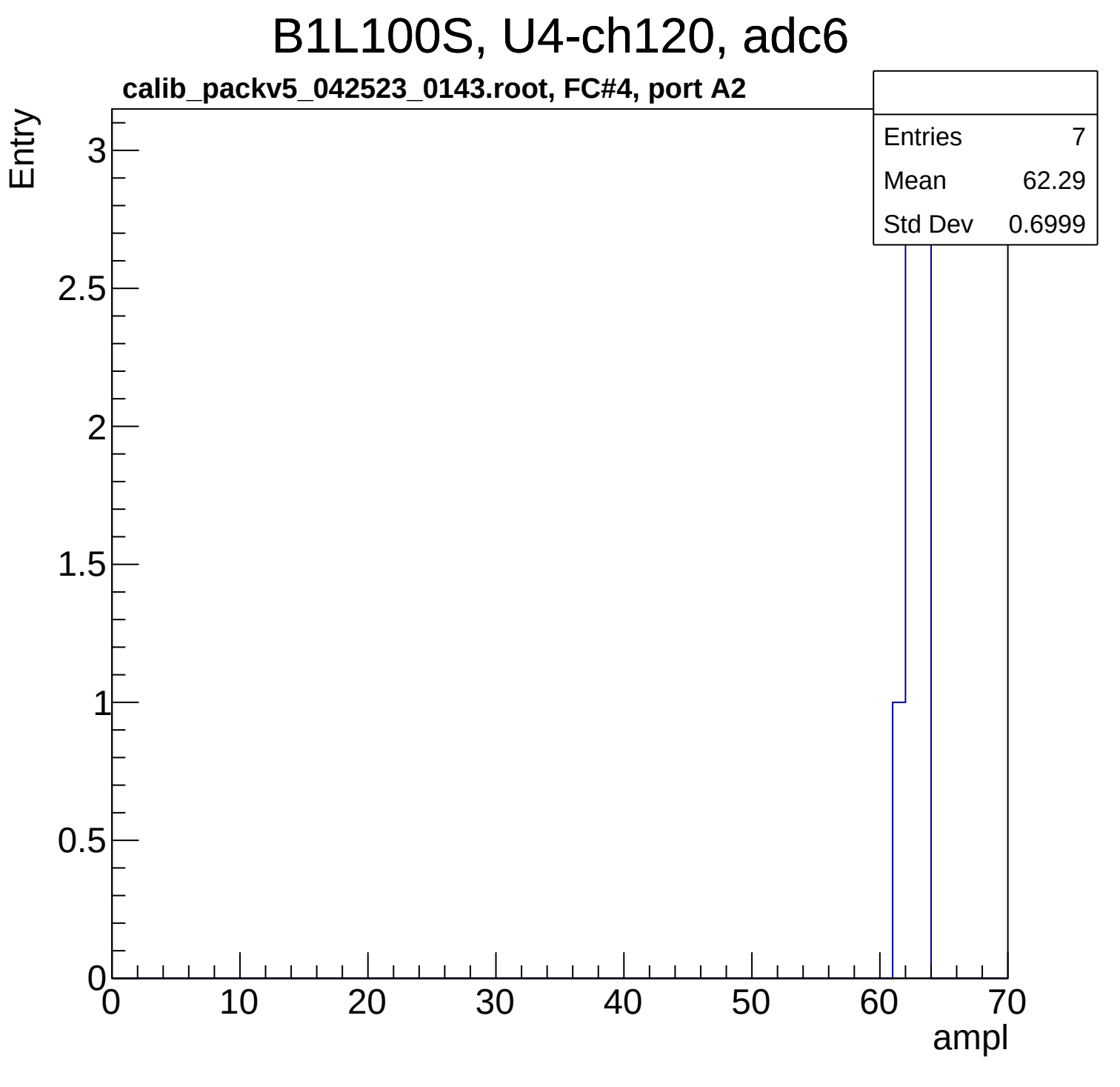

B1L100S, U4-ch120, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 36.56
Std Dev 3.38
Gaus mean : 36.9500
Gaus Width: 3.4752
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

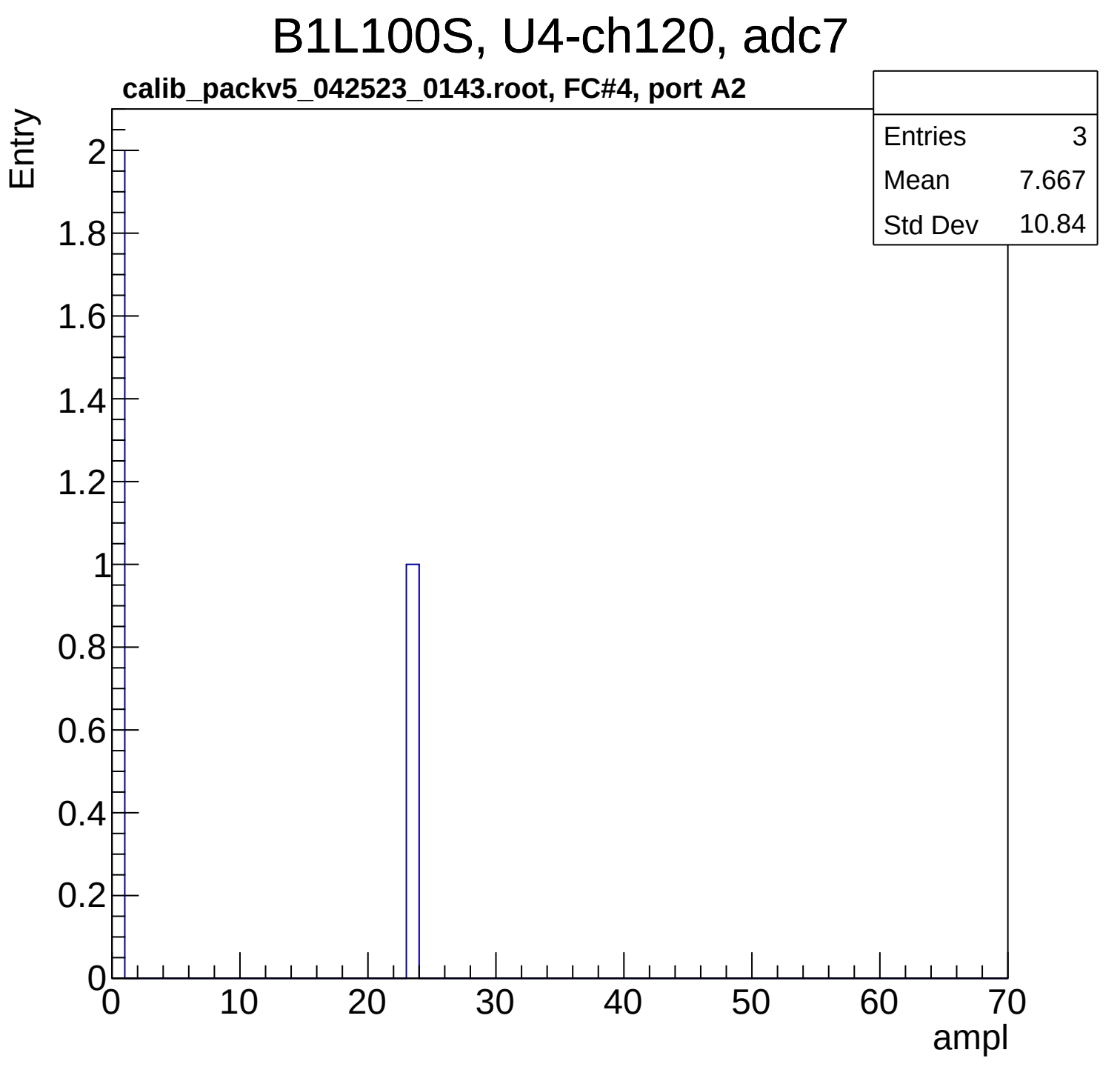

B1L100S, U4-ch120, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 43.26
Std Dev 3.743
Gaus mean : 43.7858
Gaus Width: 3.9820
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

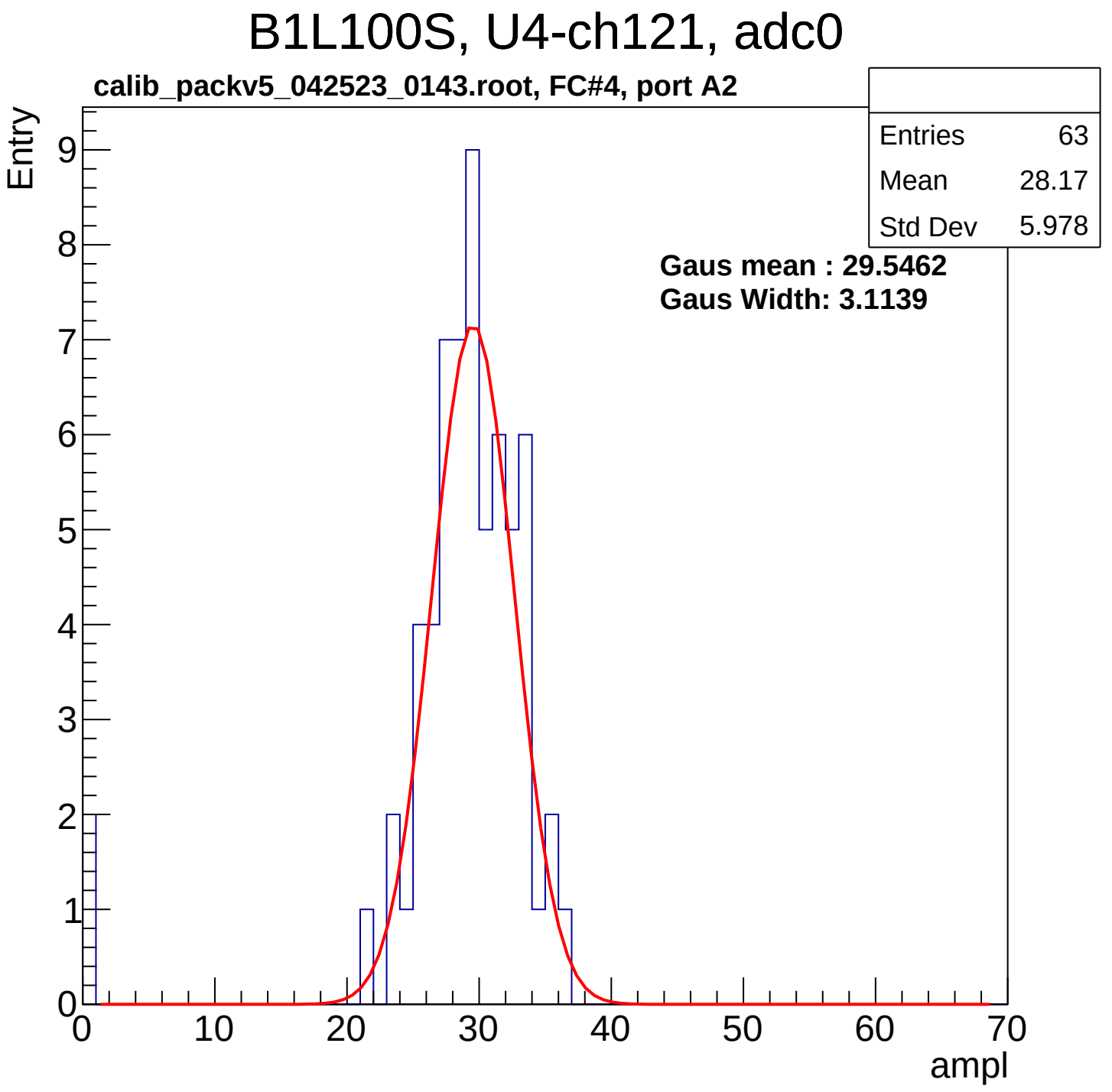

B1L100S, U4-ch120, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 49.7
Std Dev 3.425
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

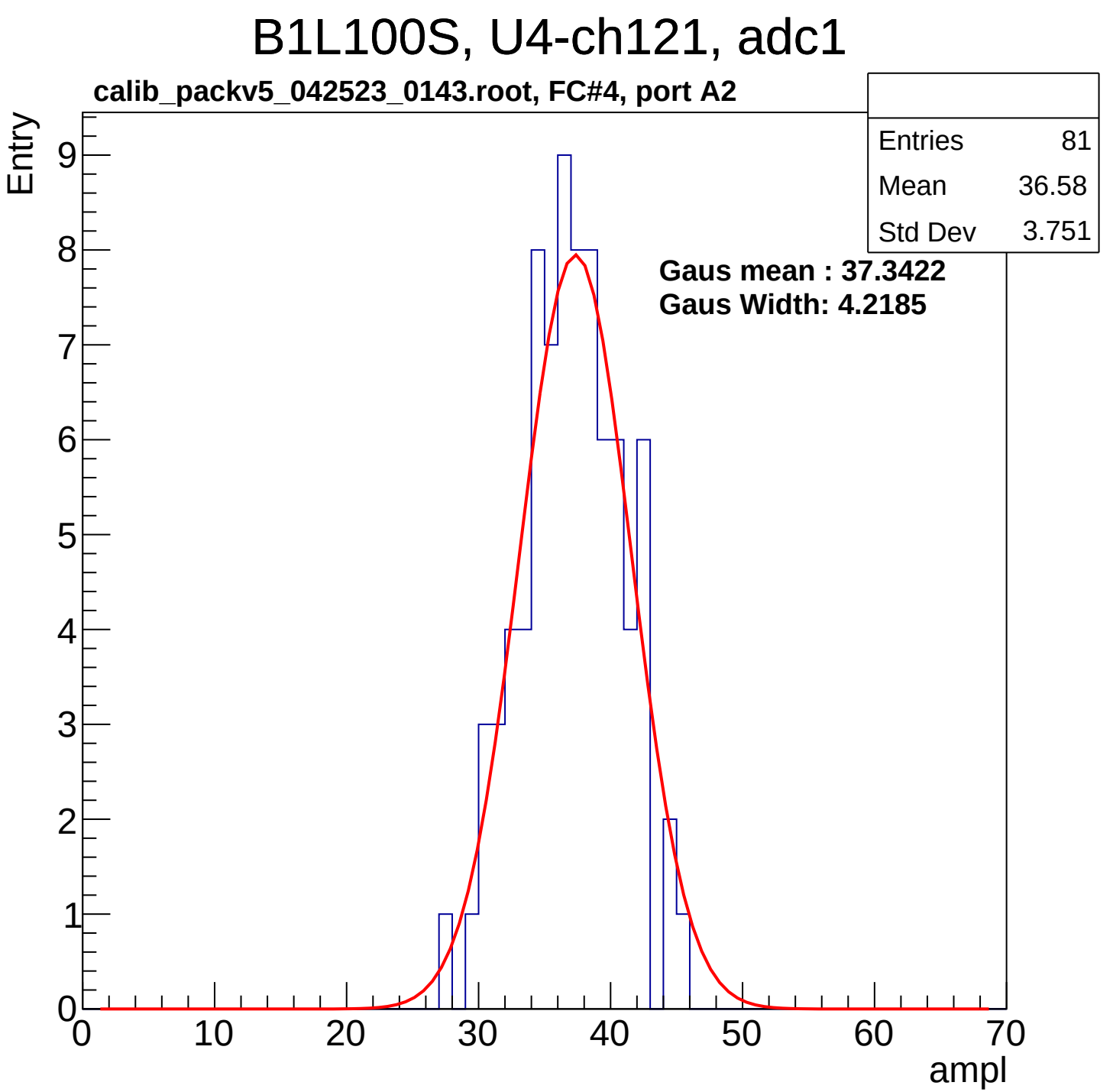

B1L100S, U4-ch120, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 55.74
Std Dev 2.755
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

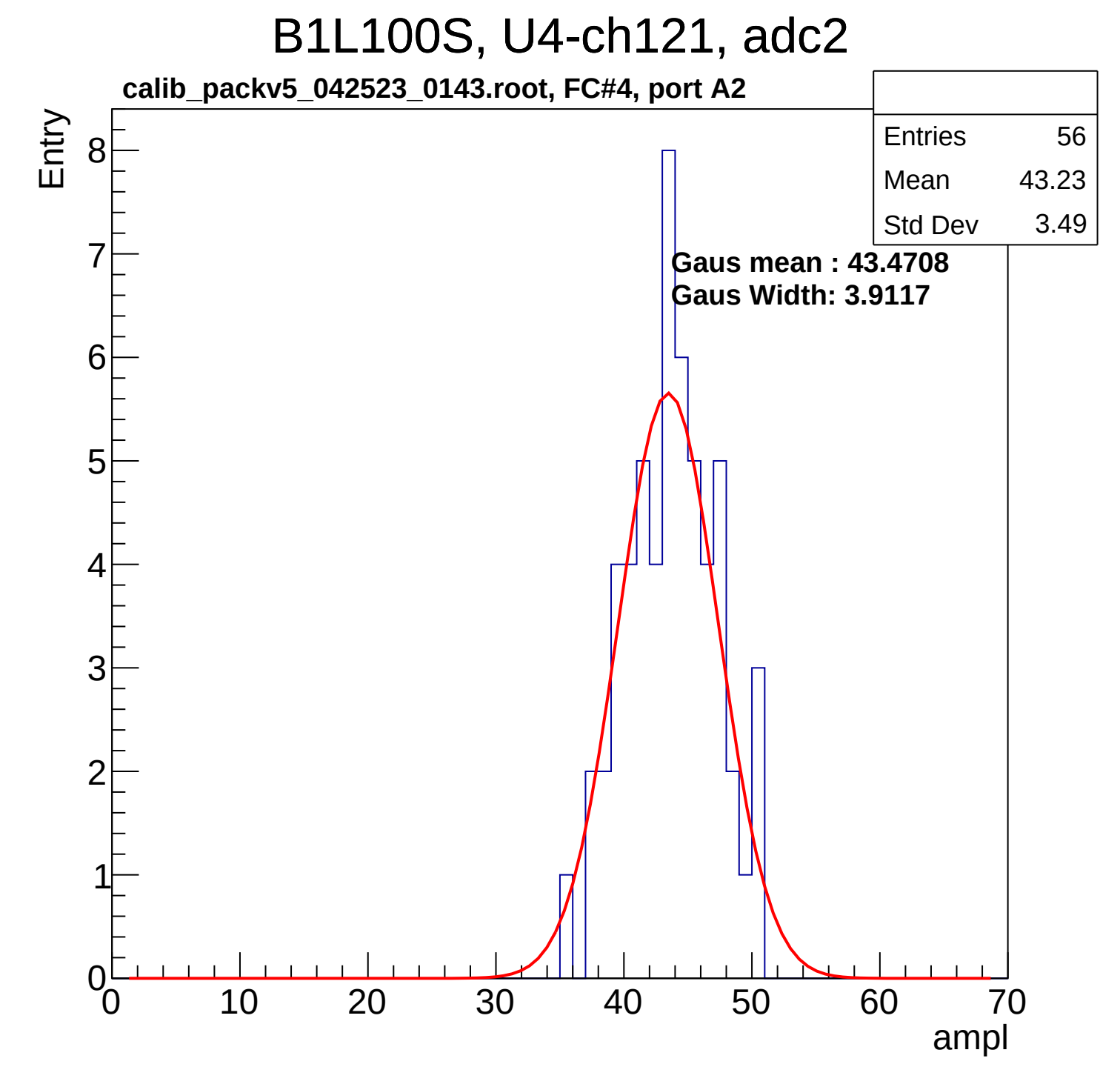

B1L100S, U4-ch120, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 44
Mean 58.93
Std Dev 9.211
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

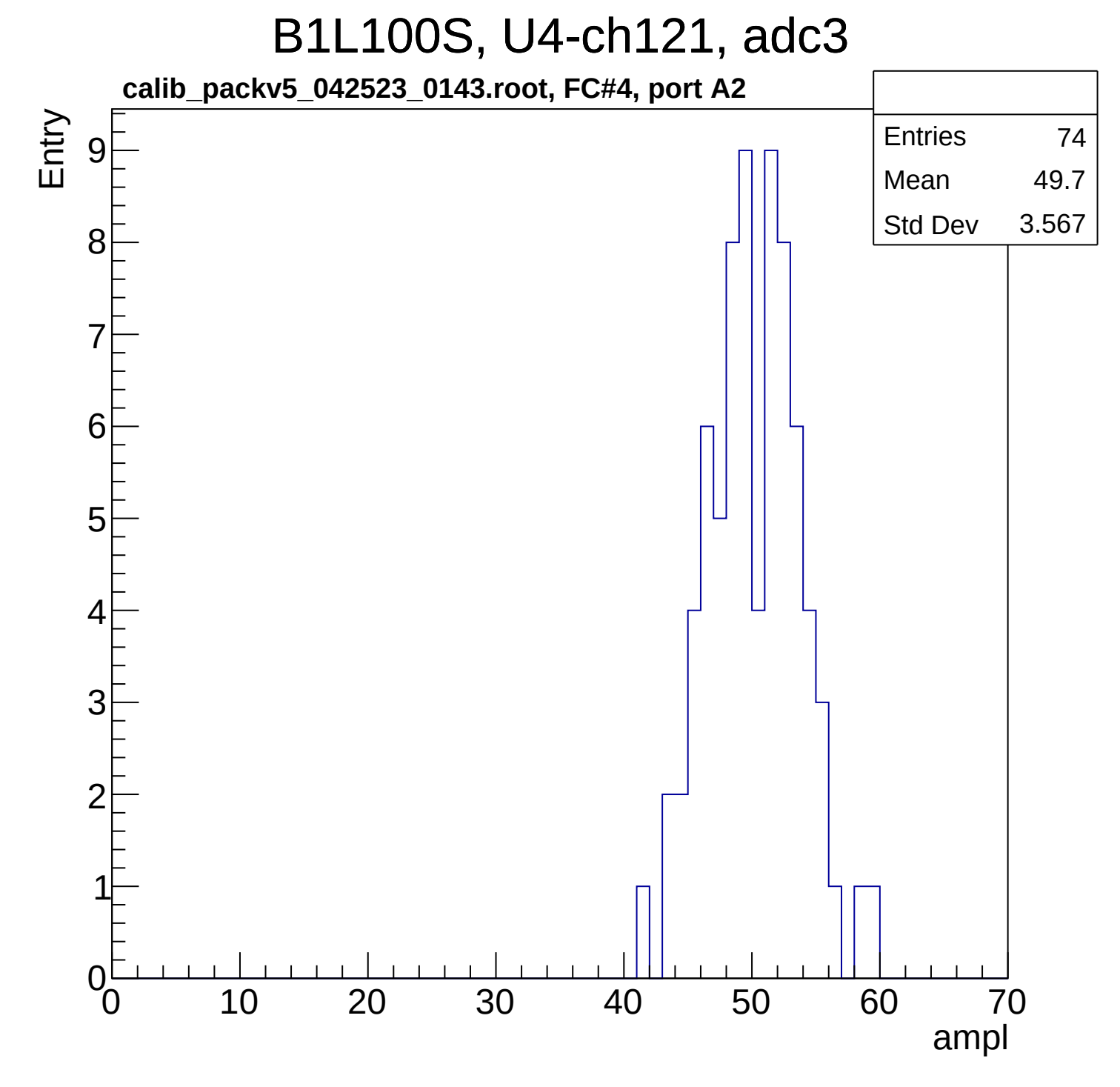

B1L100S, U4-ch120, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 62.29
Std Dev 0.6999
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

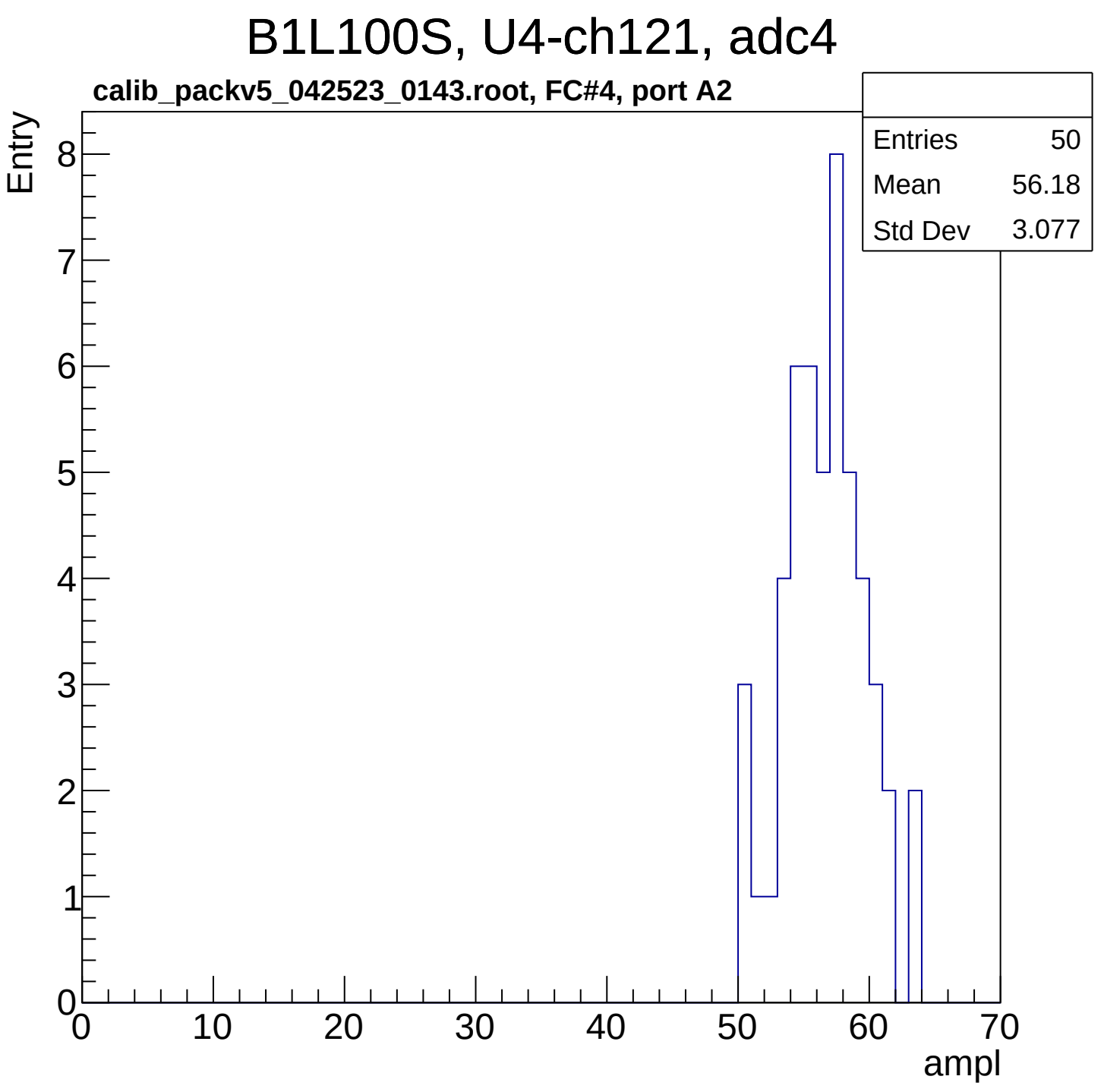

B1L100S, U4-ch120, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 7.667
Std Dev 10.84
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

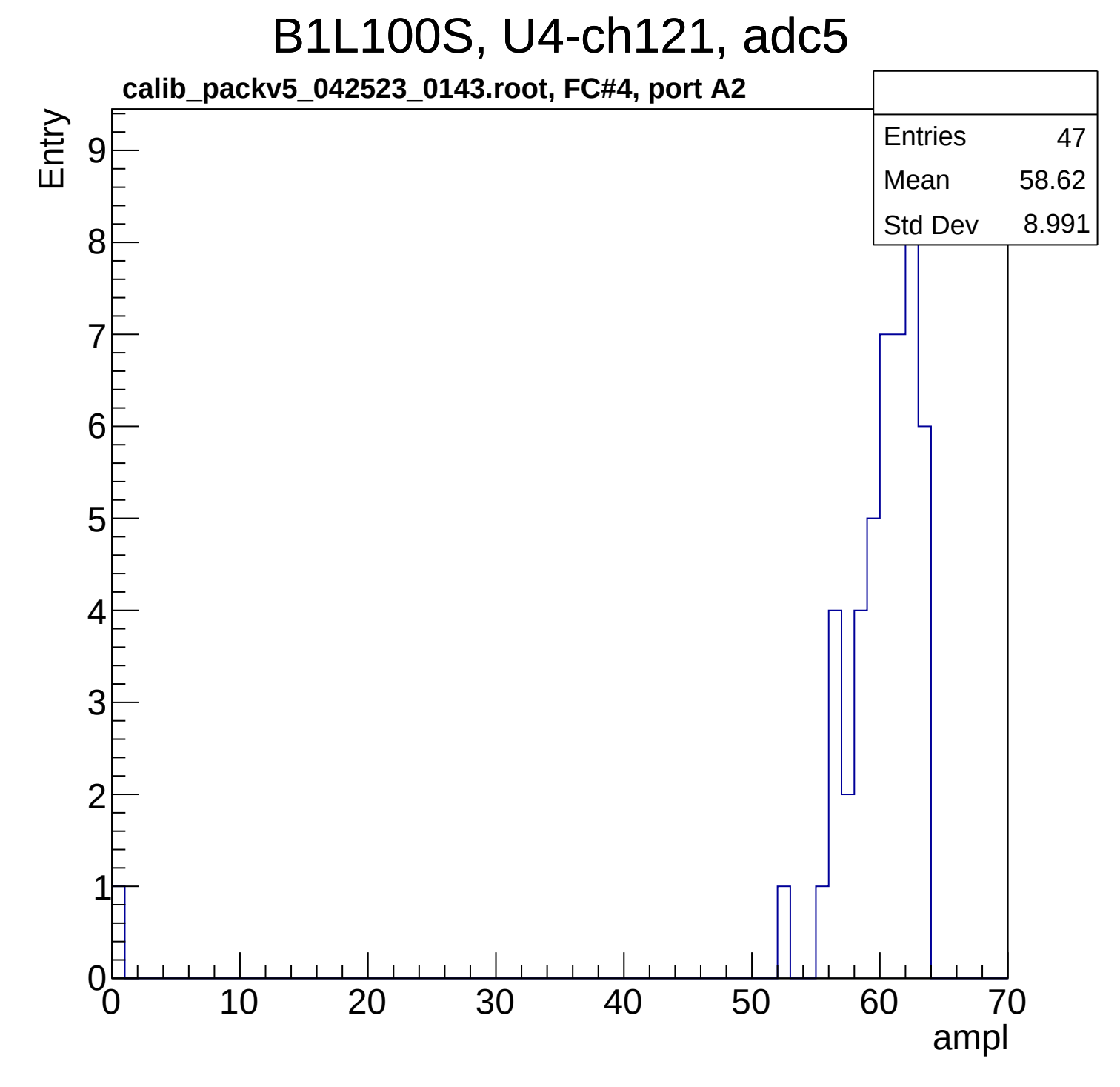

B1L100S, U4-ch121, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 28.17
Std Dev 5.978
Gaus mean : 29.5462
Gaus Width: 3.1139
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

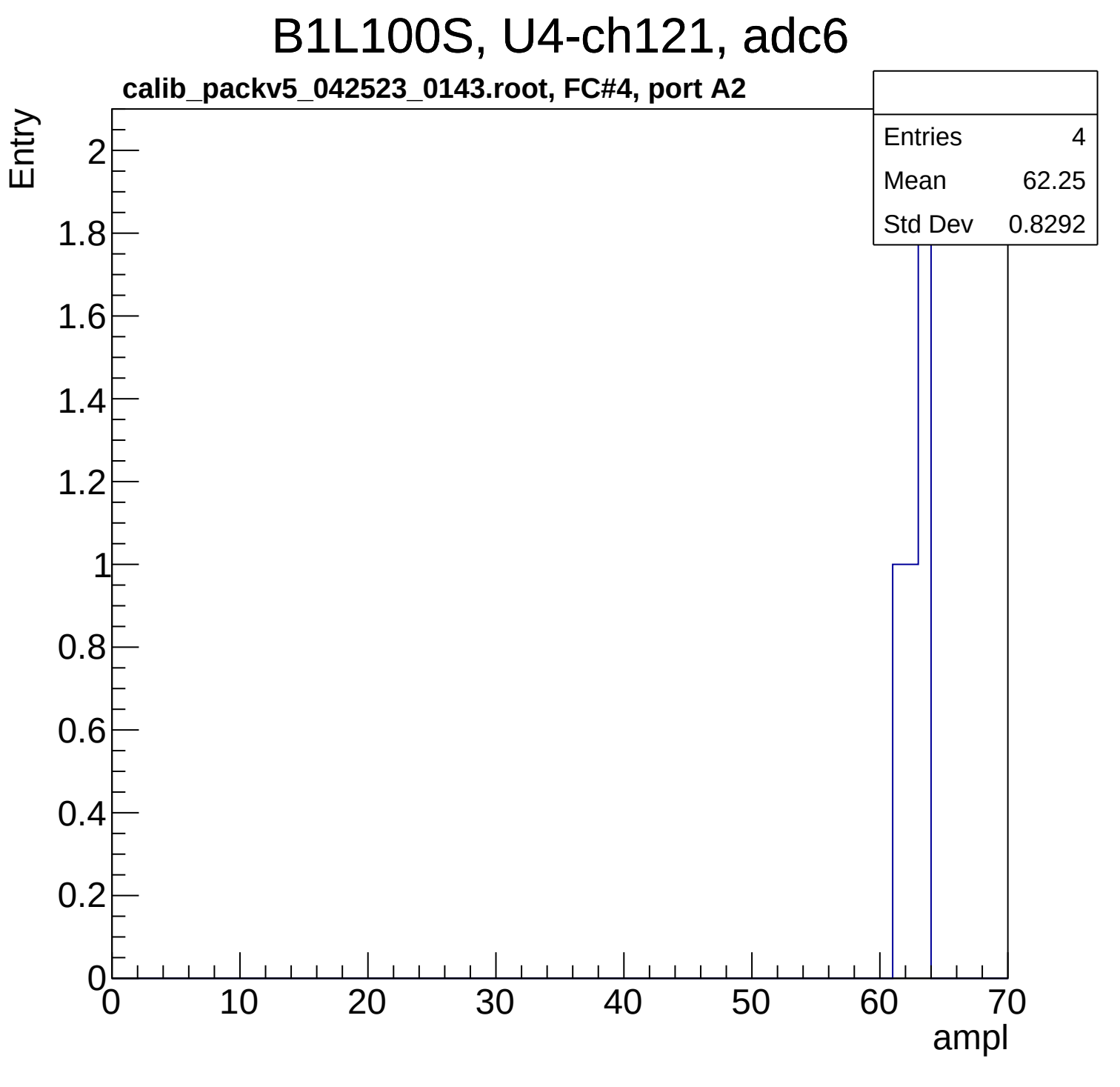

B1L100S, U4-ch121, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 36.58
Std Dev 3.751
Gaus mean : 37.3422
Gaus Width: 4.2185
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

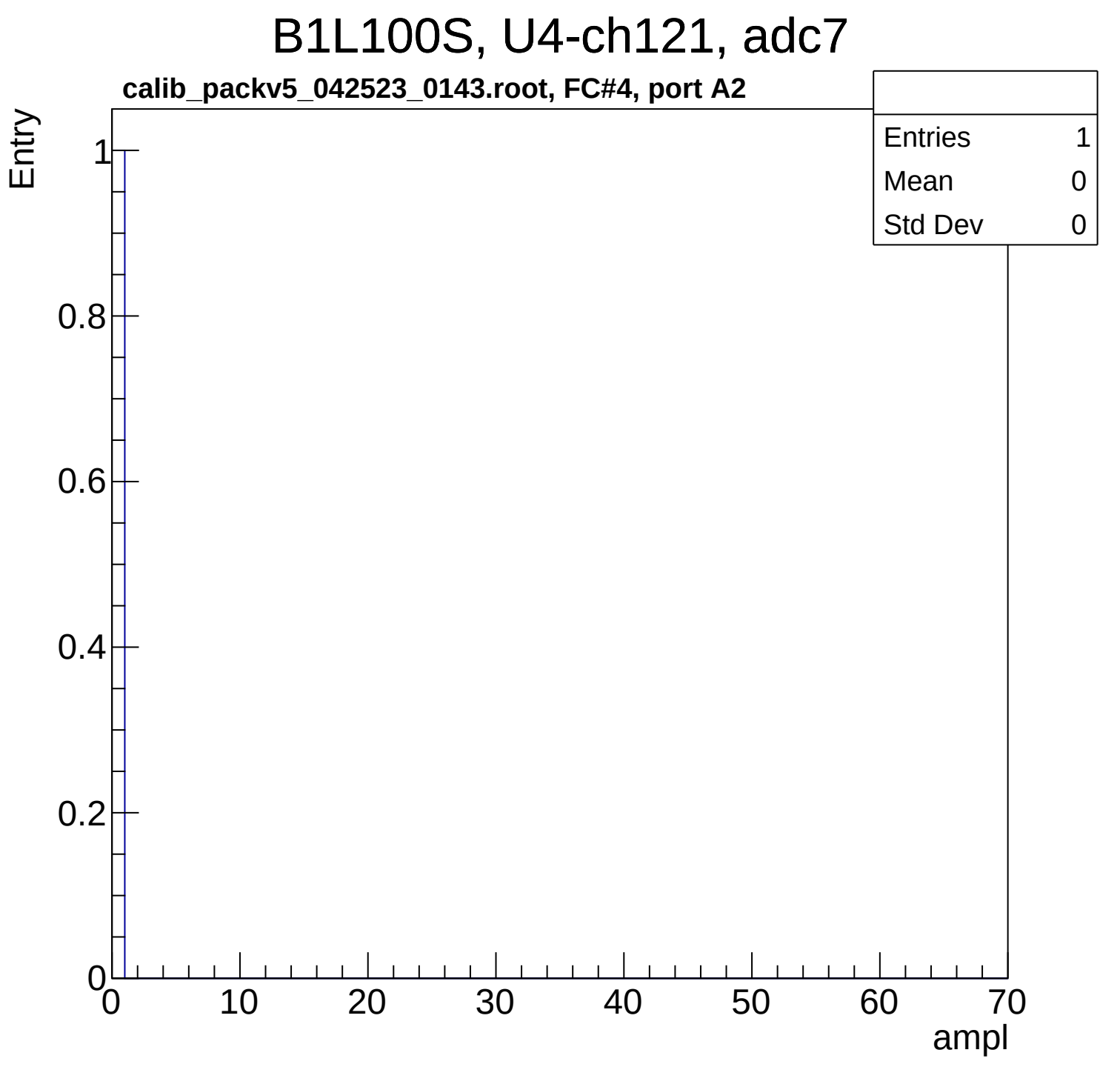

B1L100S, U4-ch121, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 43.23
Std Dev 3.49
Gaus mean : 43.4708
Gaus Width: 3.9117
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

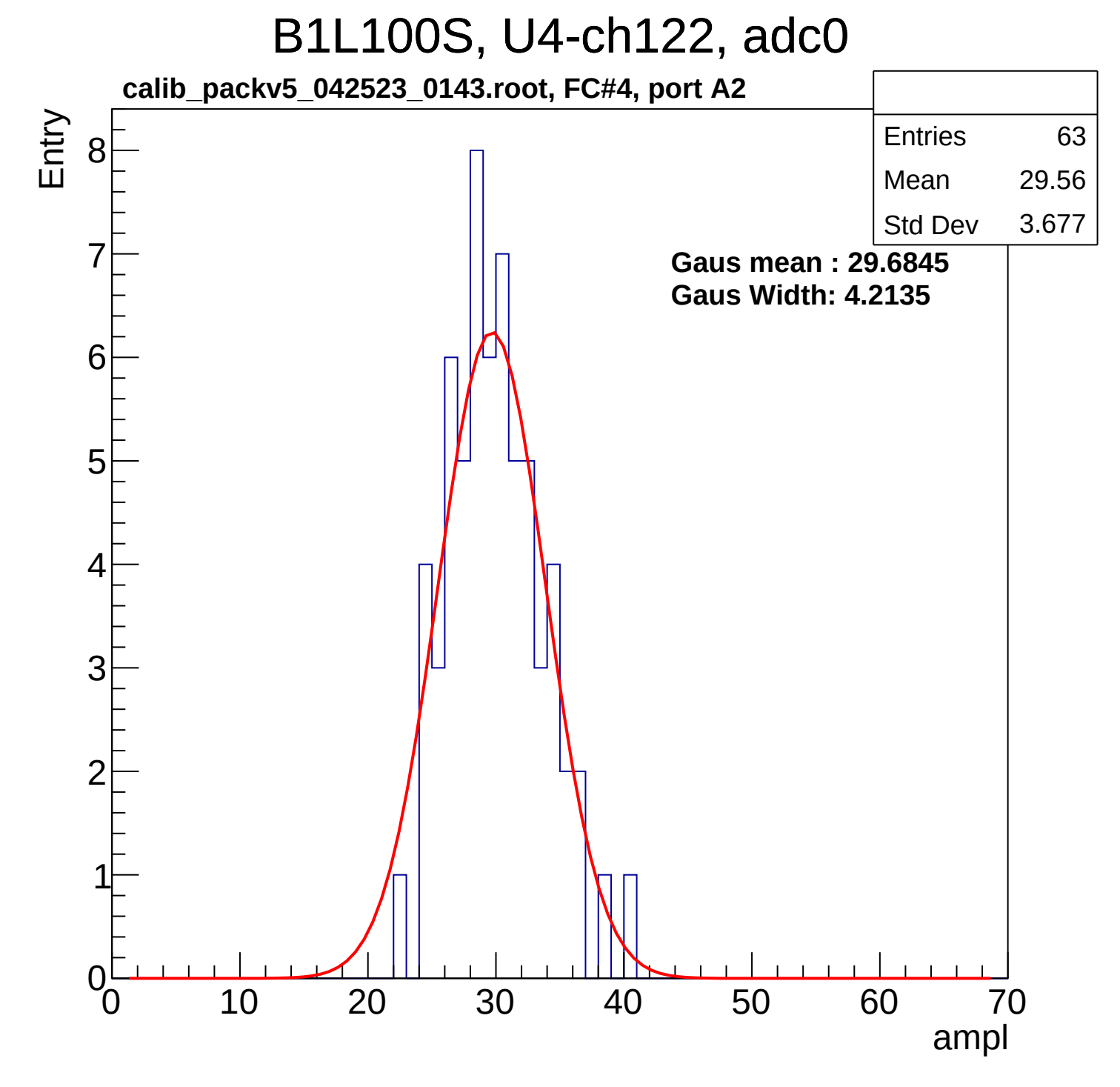

B1L100S, U4-ch121, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 49.7
Std Dev 3.567
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

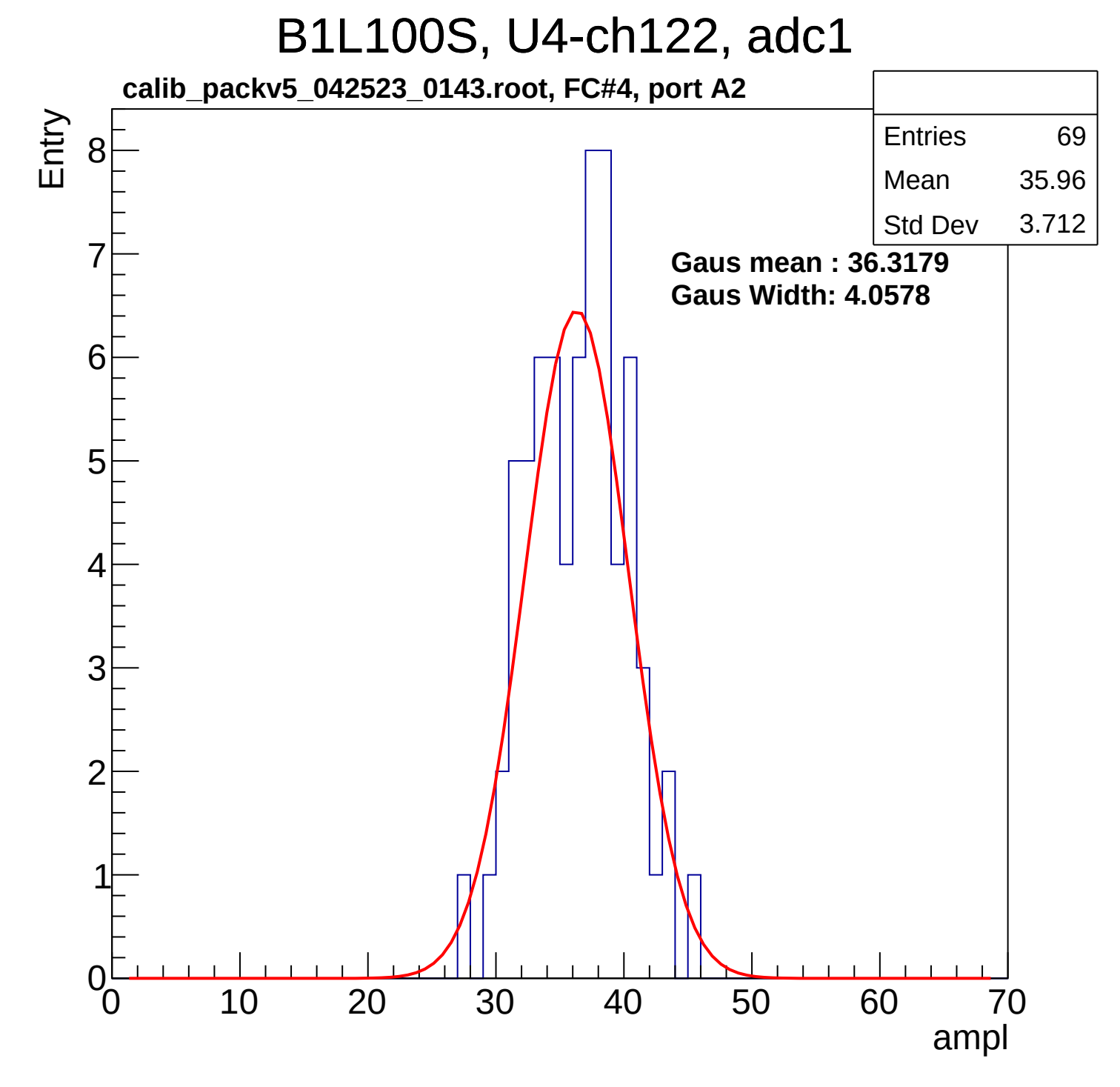

B1L100S, U4-ch121, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 56.18
Std Dev 3.077
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

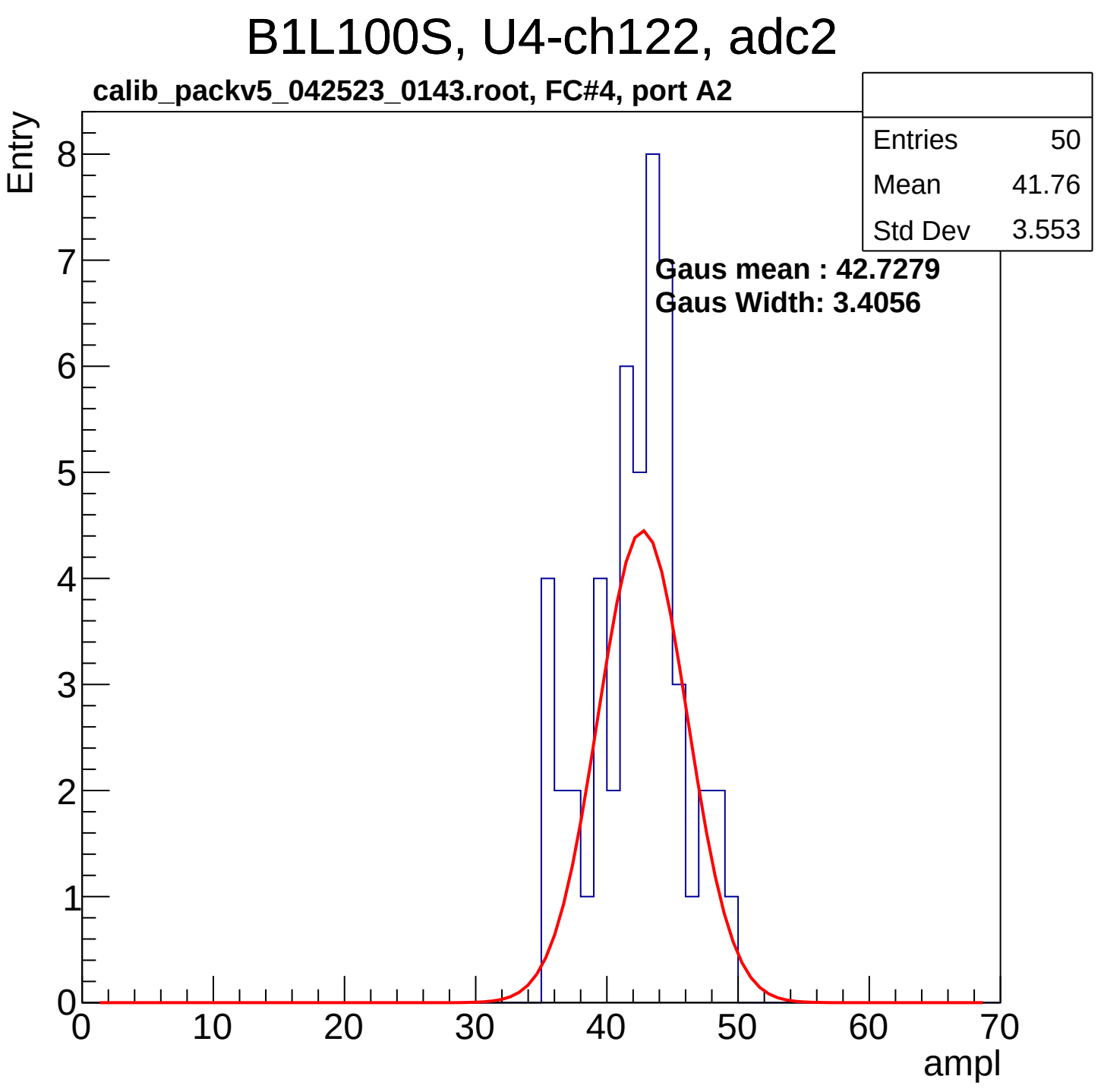

B1L100S, U4-ch121, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 58.62
Std Dev 8.991
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

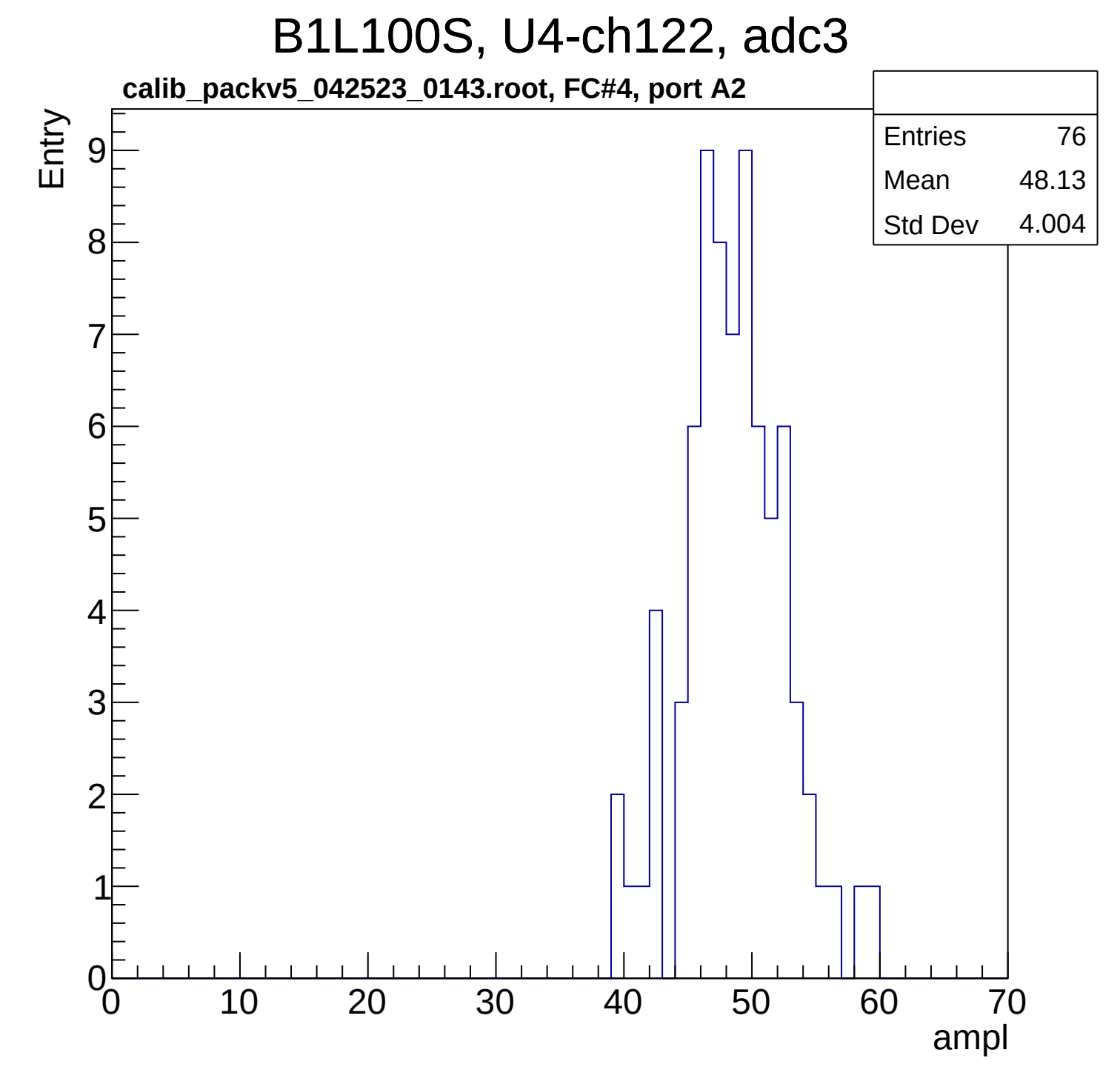

B1L100S, U4-ch121, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

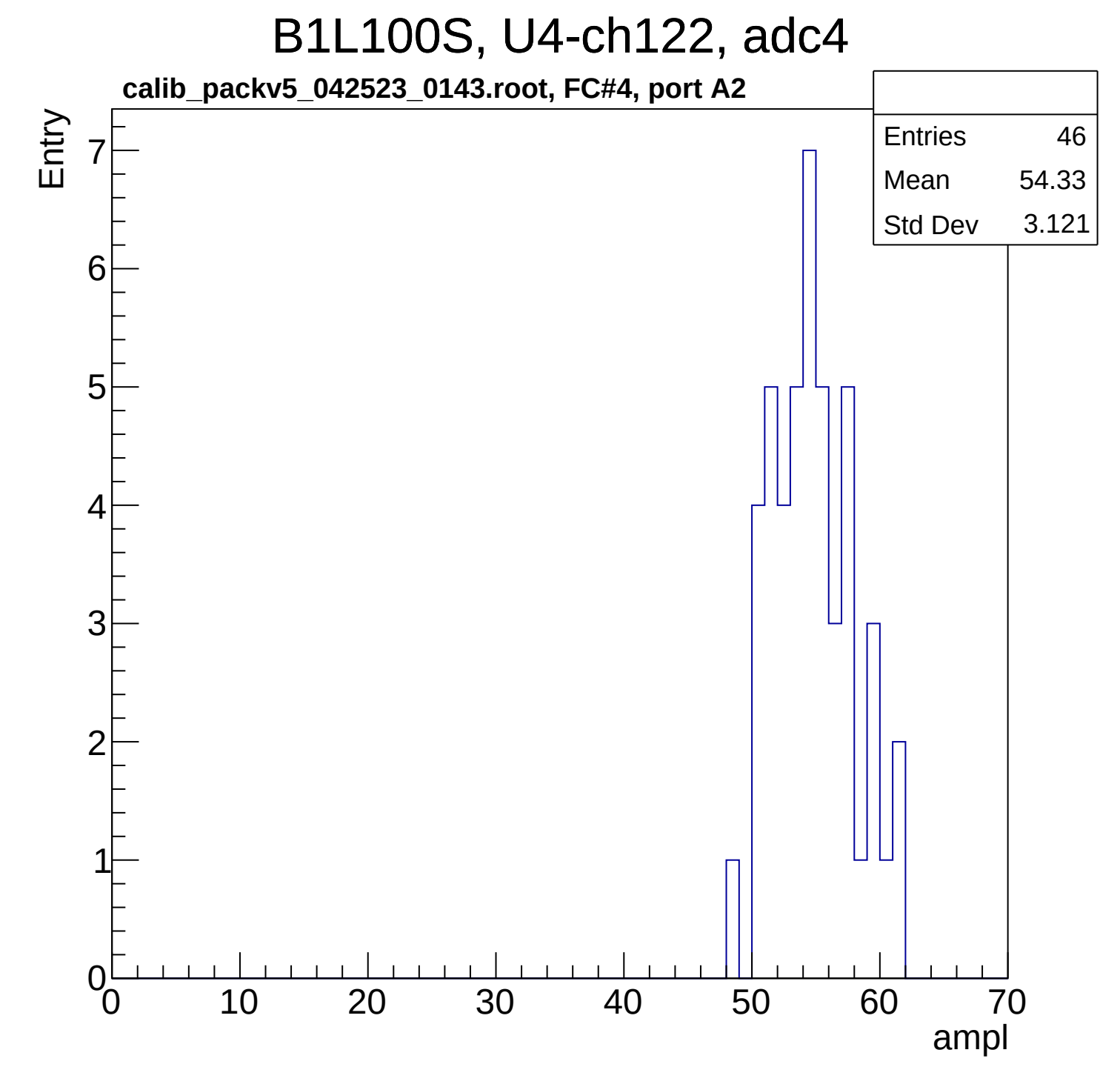

B1L100S, U4-ch121, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

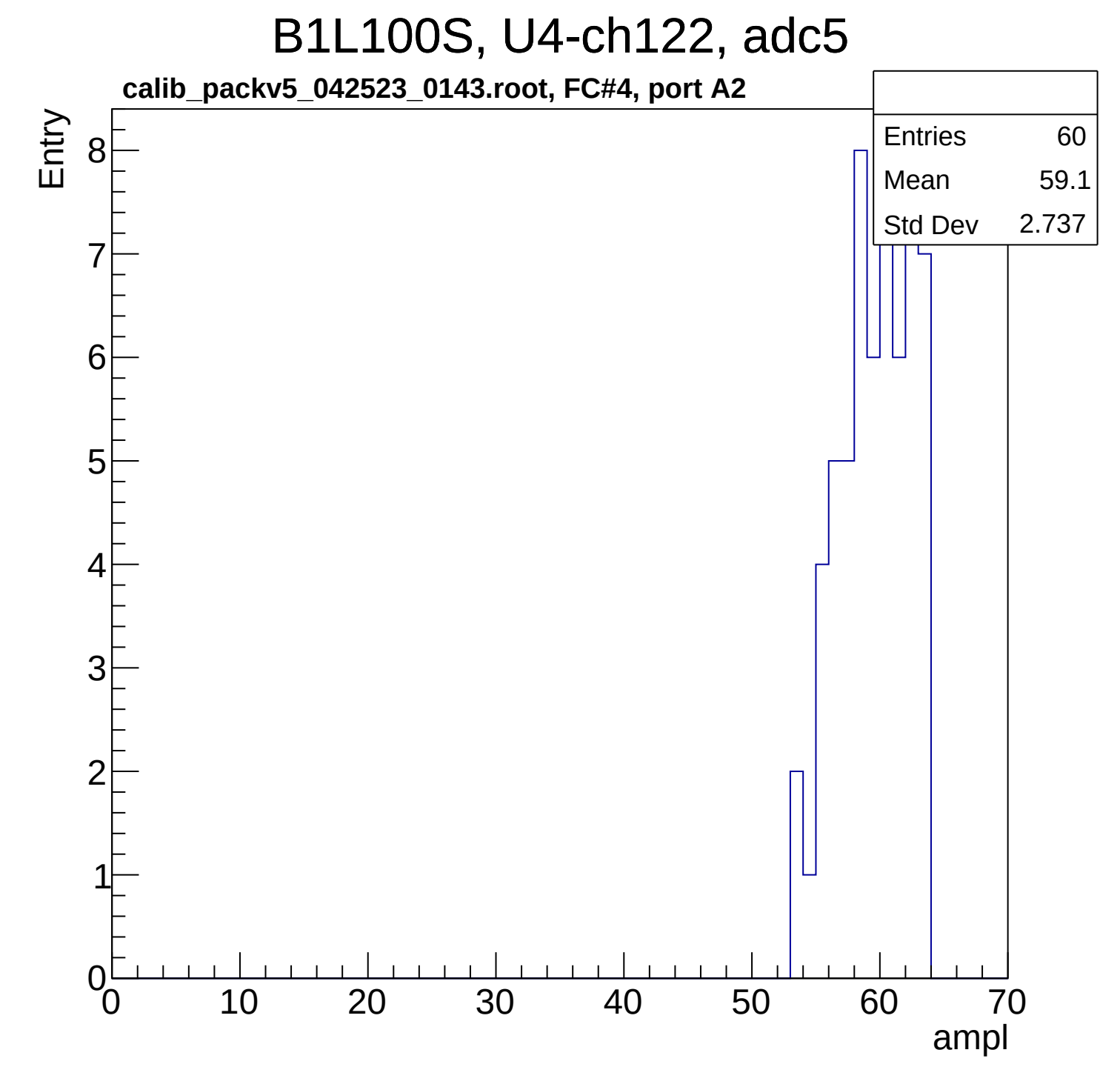

B1L100S, U4-ch122, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 29.56
Std Dev 3.677
Gaus mean : 29.6845
Gaus Width: 4.2135
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

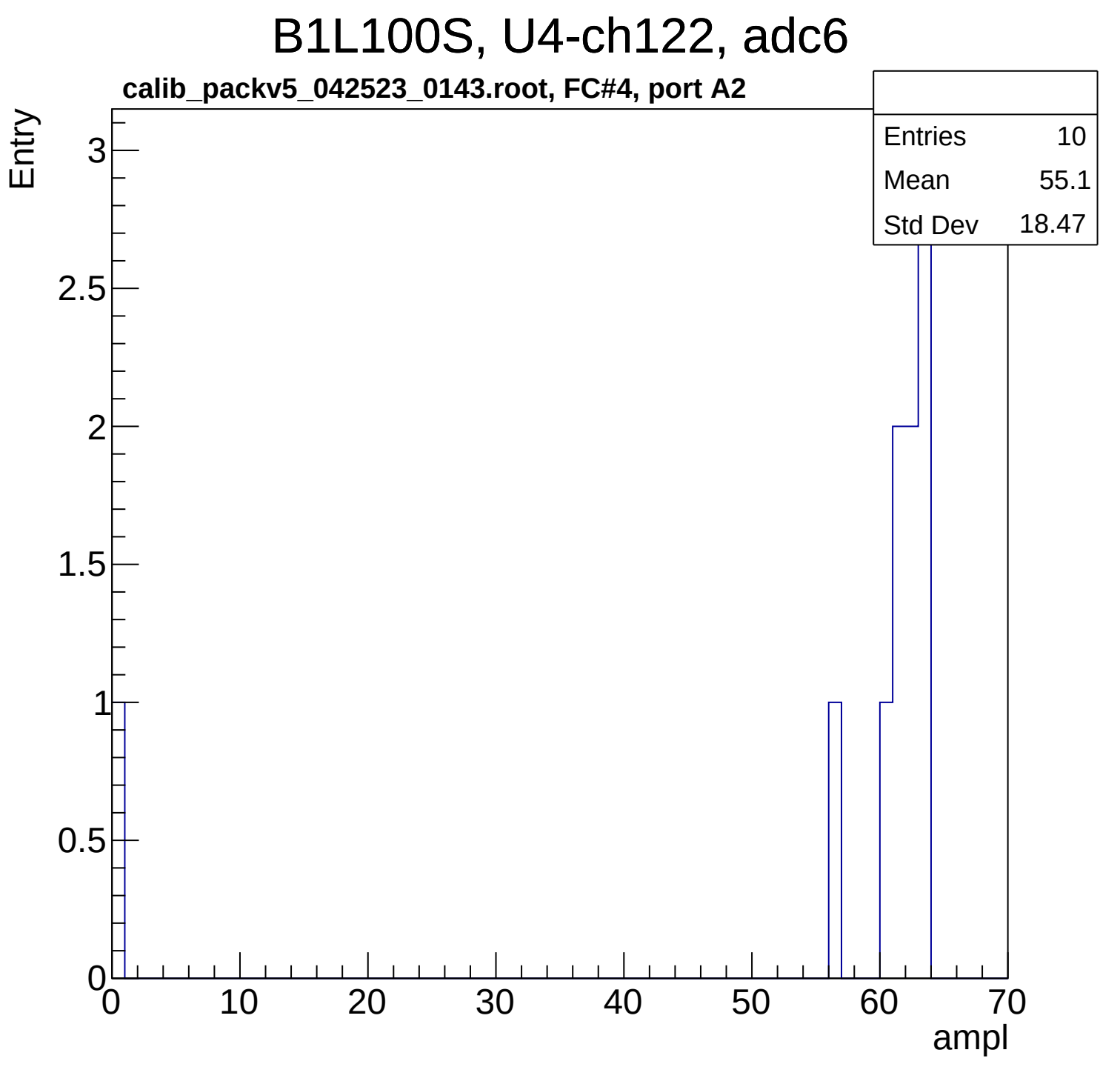

B1L100S, U4-ch122, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 35.96
Std Dev 3.712
Gaus mean : 36.3179
Gaus Width: 4.0578
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

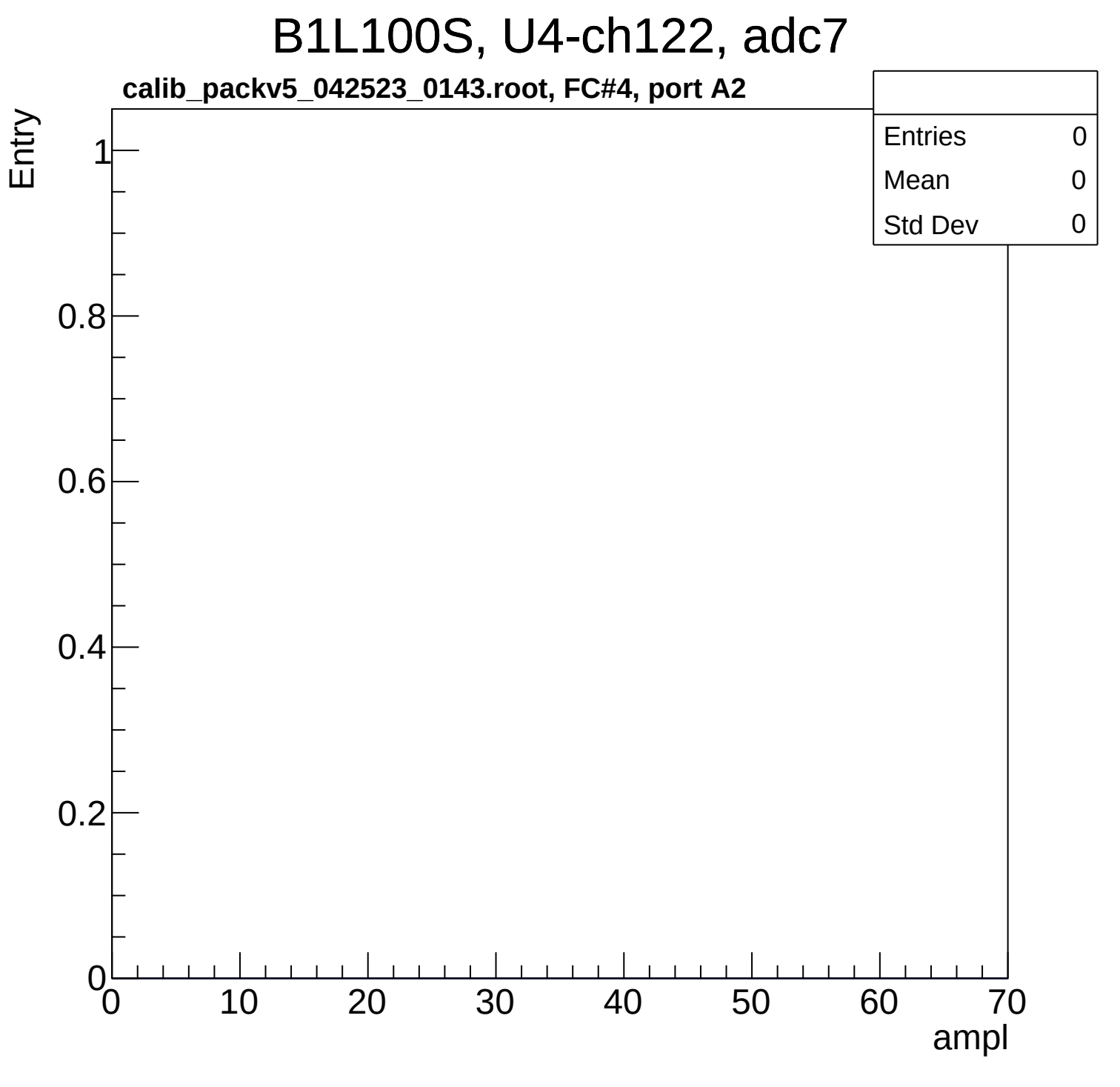

B1L100S, U4-ch122, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 41.76
Std Dev 3.553
Gaus mean : 42.7279
Gaus Width: 3.4056
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

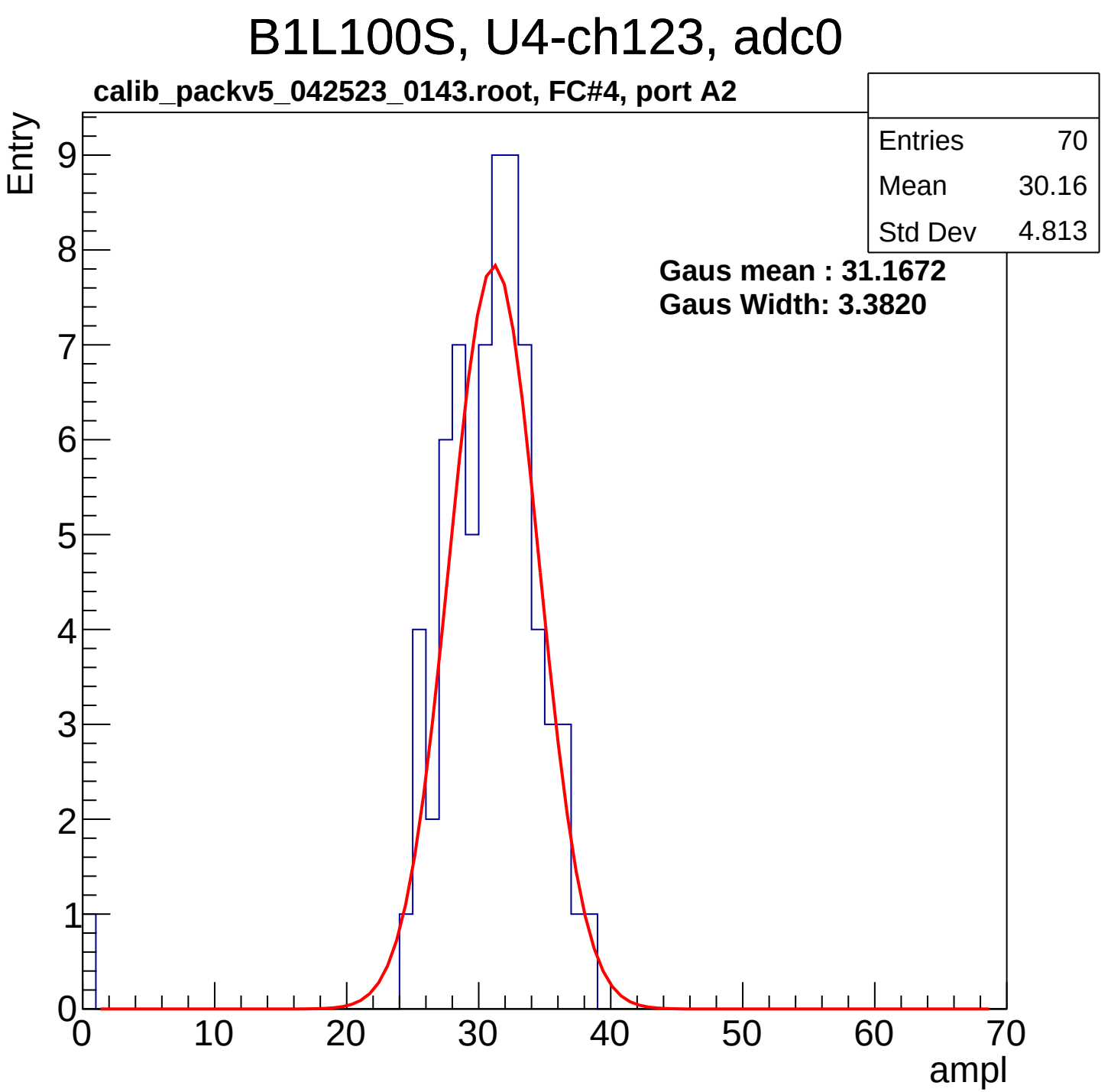

B1L100S, U4-ch122, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 48.13
Std Dev 4.004
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

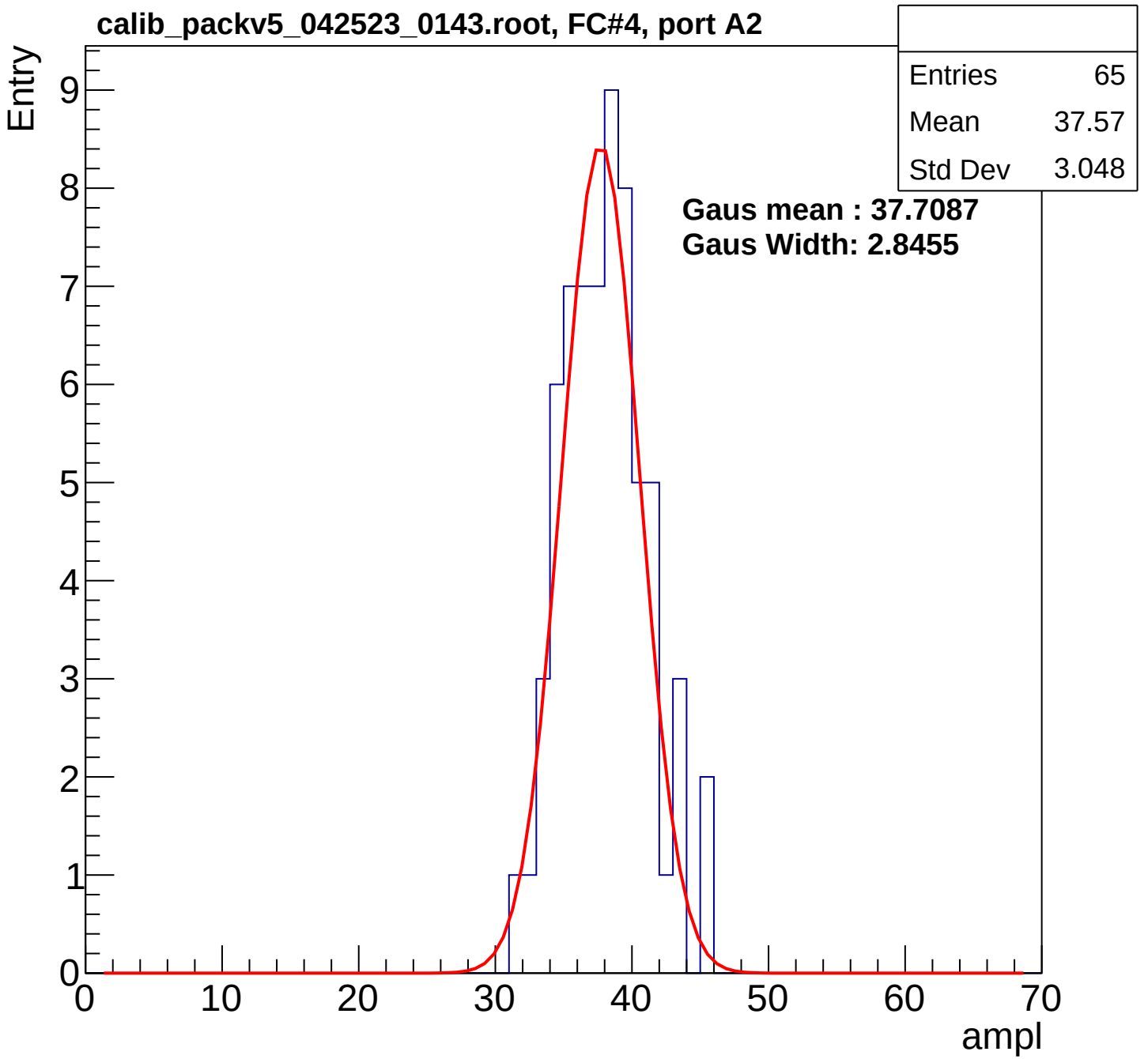

B1L100S, U4-ch122, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 54.33
Std Dev 3.121
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

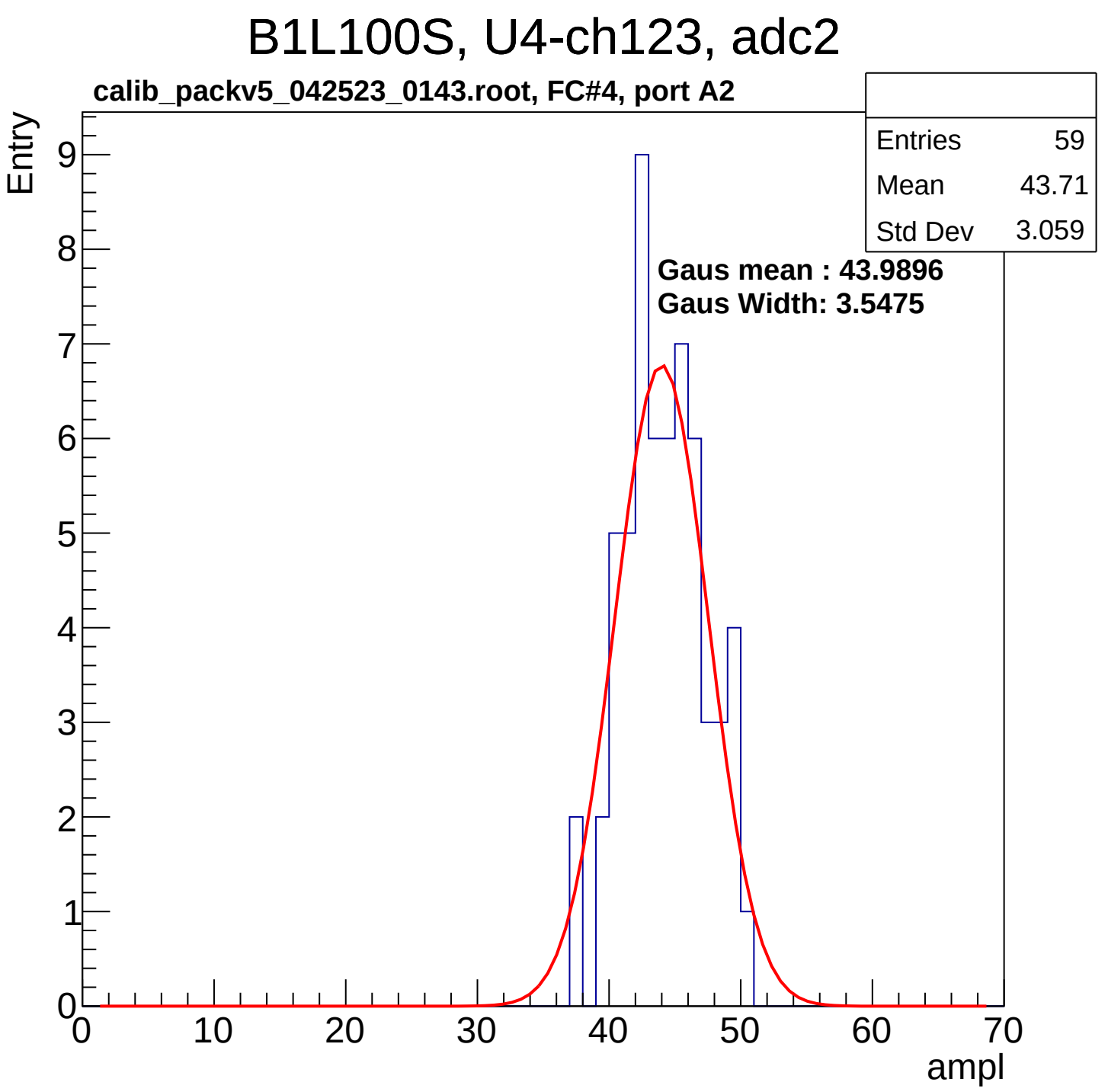

B1L100S, U4-ch122, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 59.1
Std Dev 2.737
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

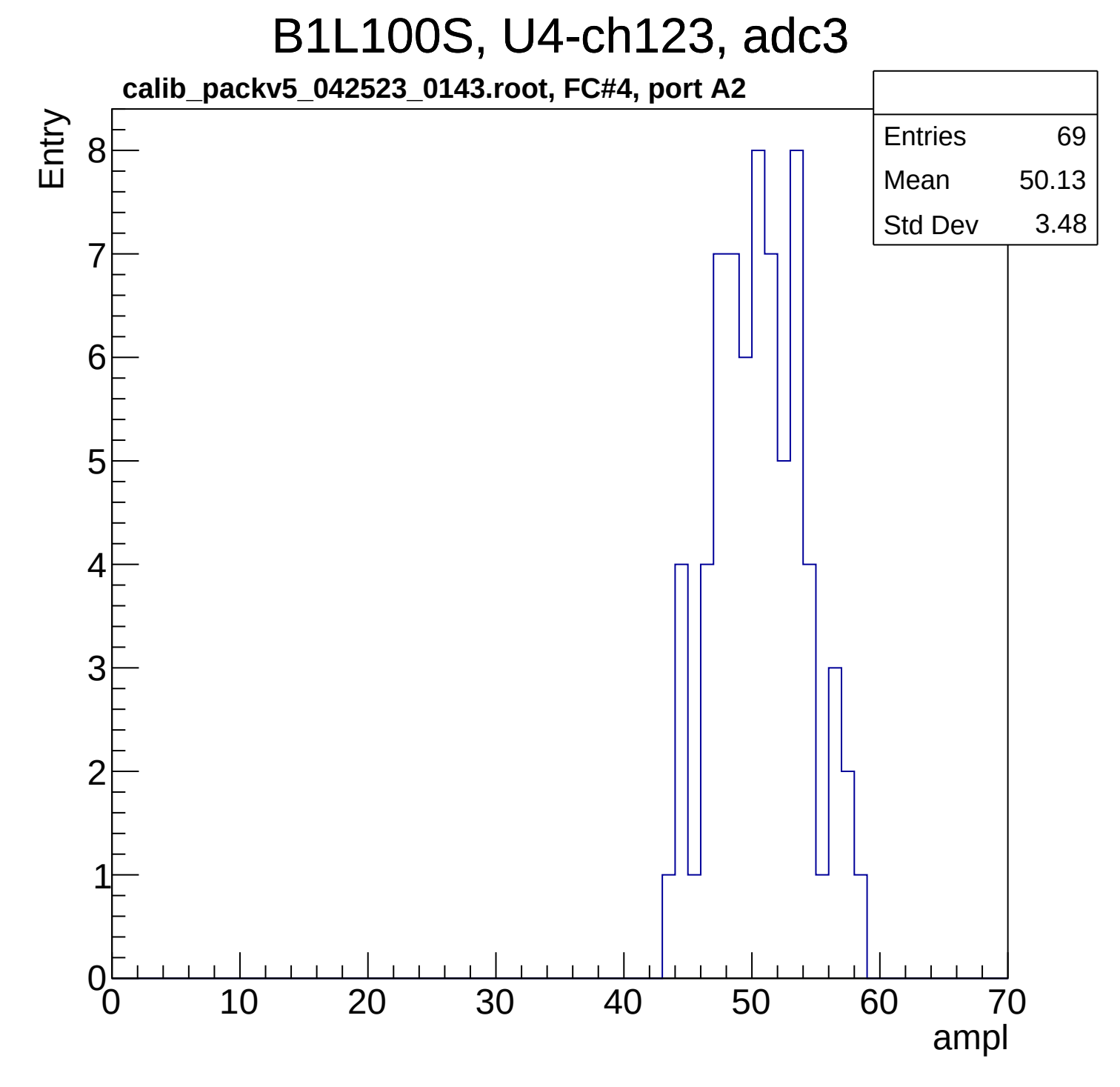

B1L100S, U4-ch122, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 55.1
Std Dev 18.47
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

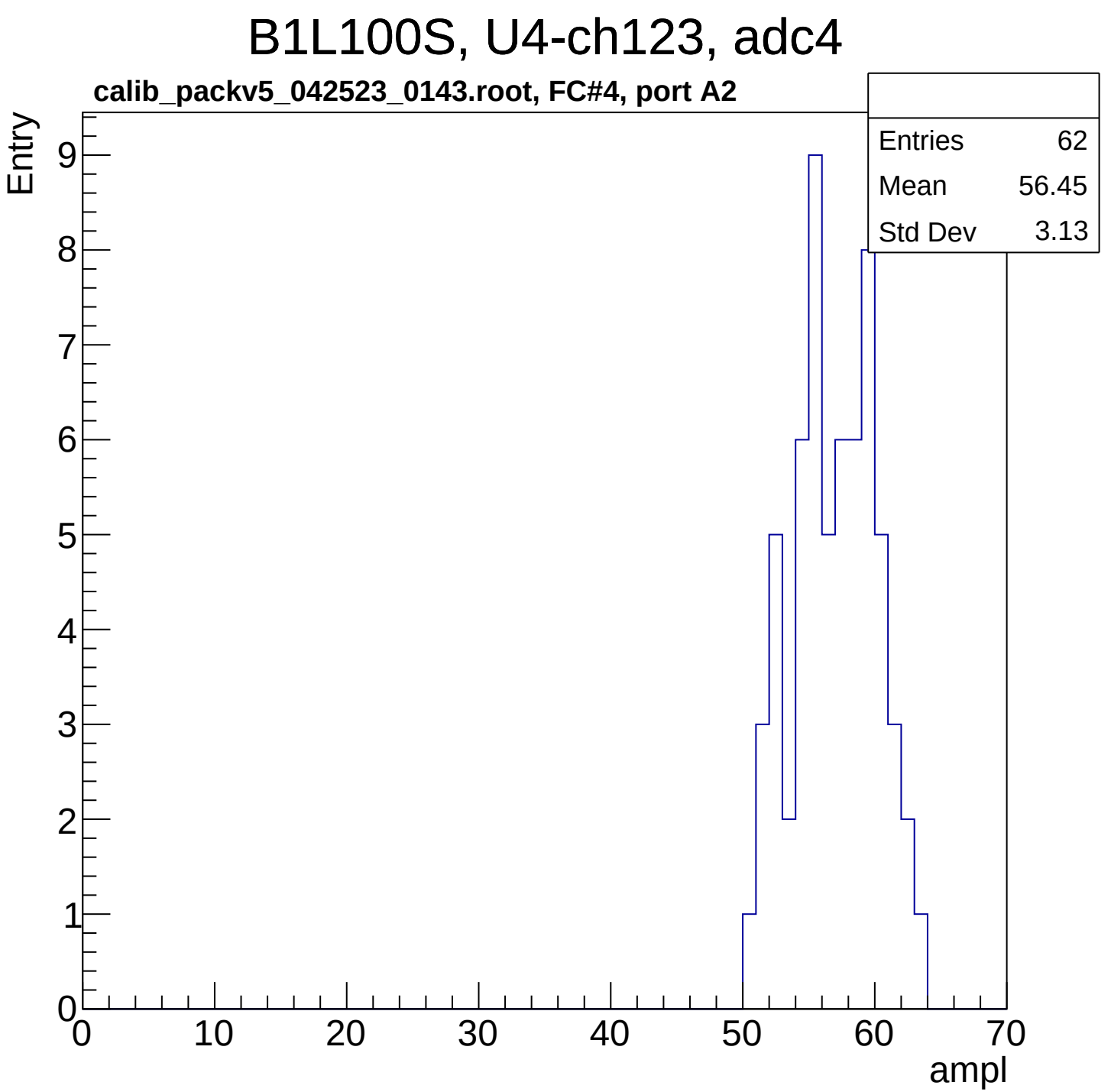

B1L100S, U4-ch122, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

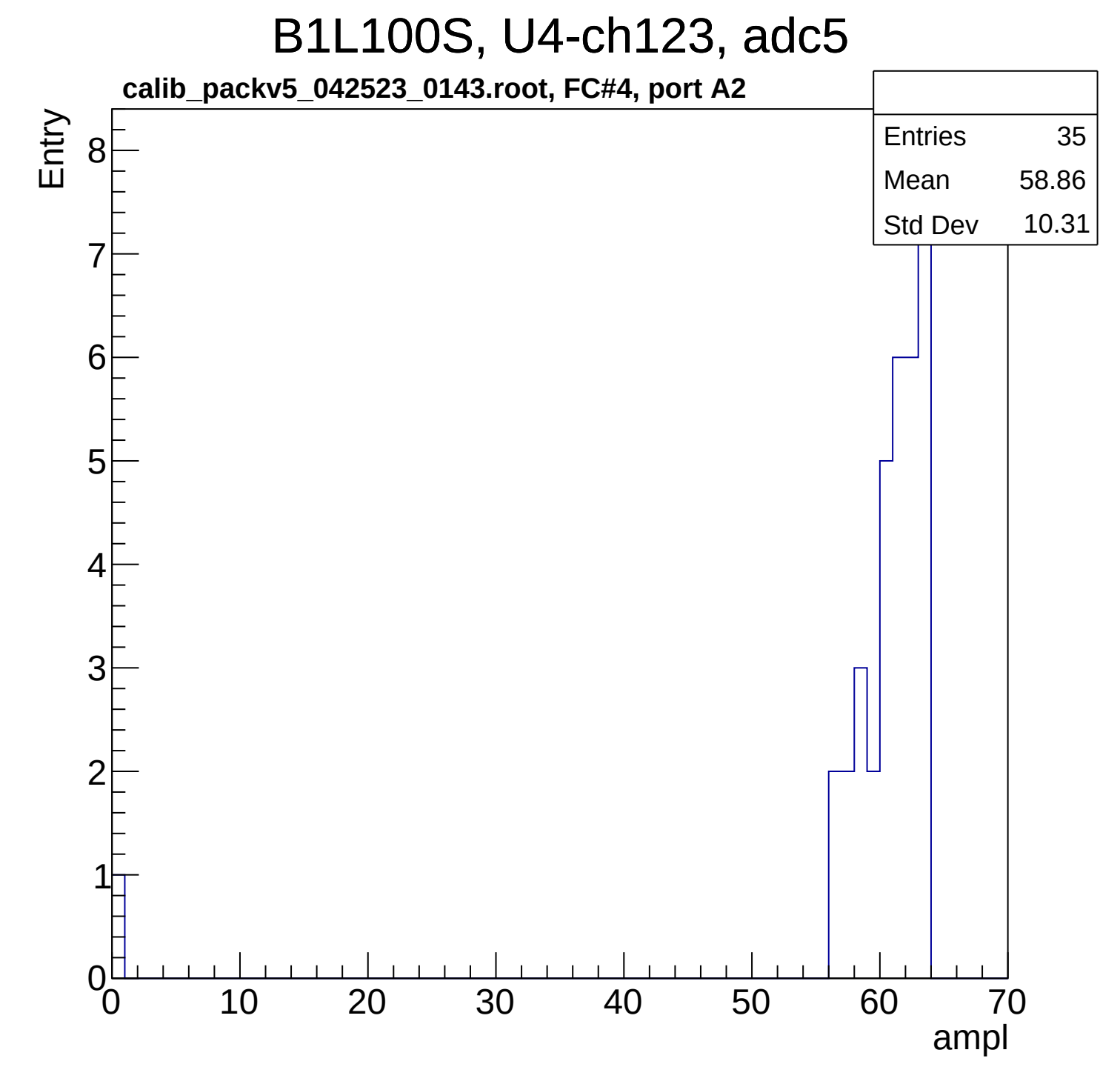

B1L100S, U4-ch123, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 30.16
Std Dev 4.813
Gaus mean : 31.1672
Gaus Width: 3.3820
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

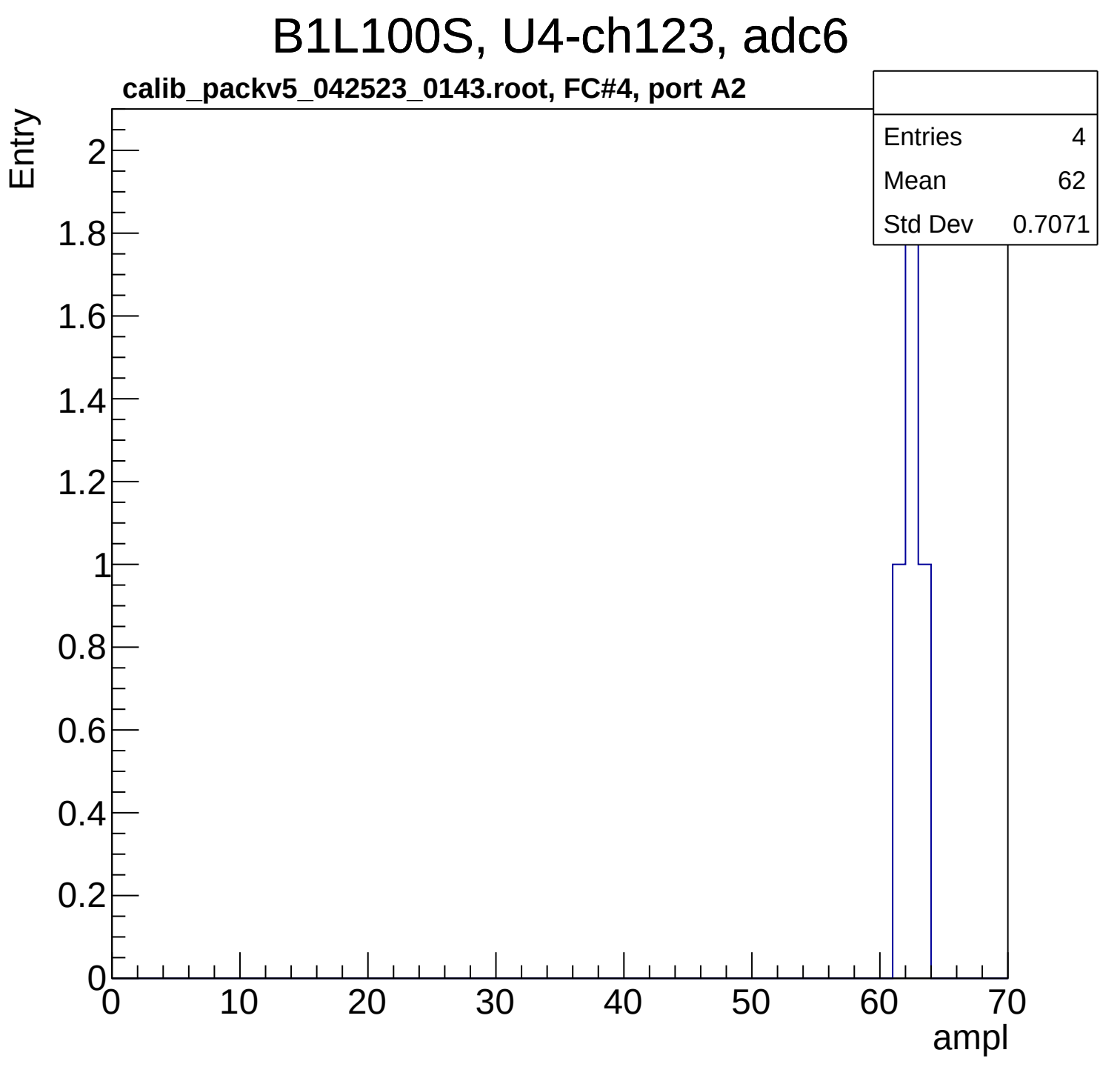

B1L100S, U4-ch123, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 37.57
Std Dev 3.048
Gaus mean : 37.7087
Gaus Width: 2.8455
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

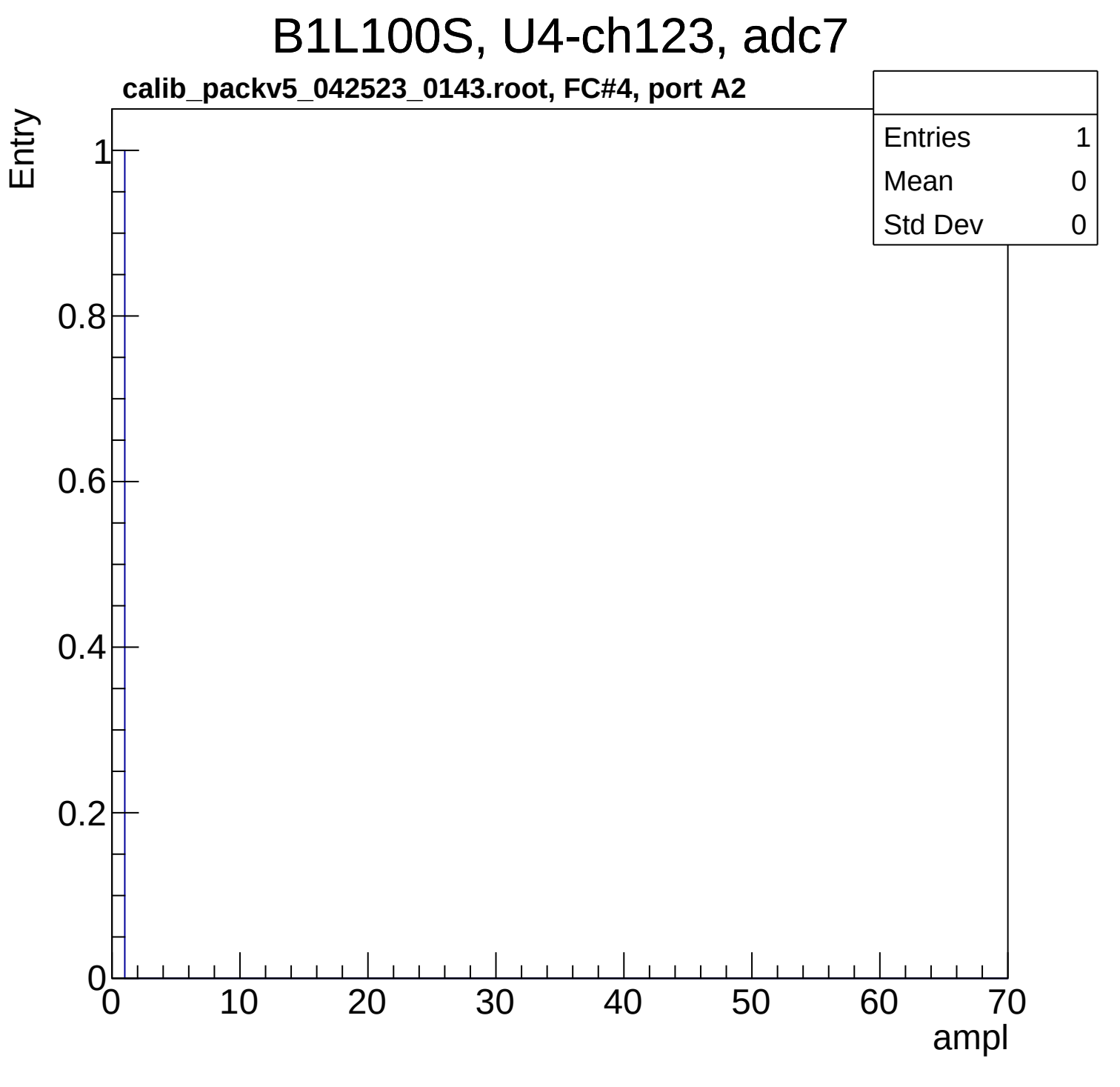

B1L100S, U4-ch123, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 43.71
Std Dev 3.059
Gaus mean : 43.9896
Gaus Width: 3.5475
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

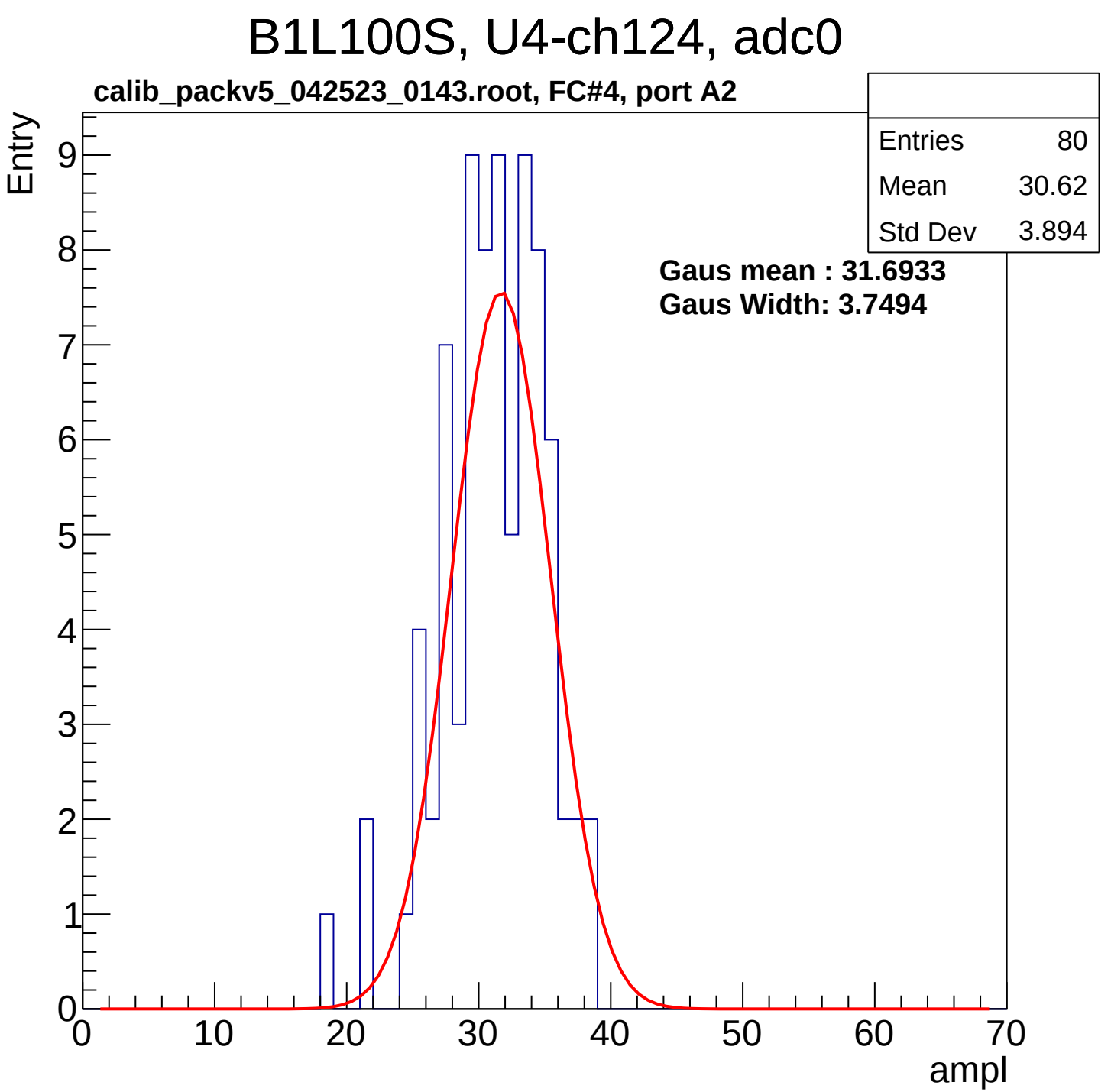

B1L100S, U4-ch123, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 50.13
Std Dev 3.48
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

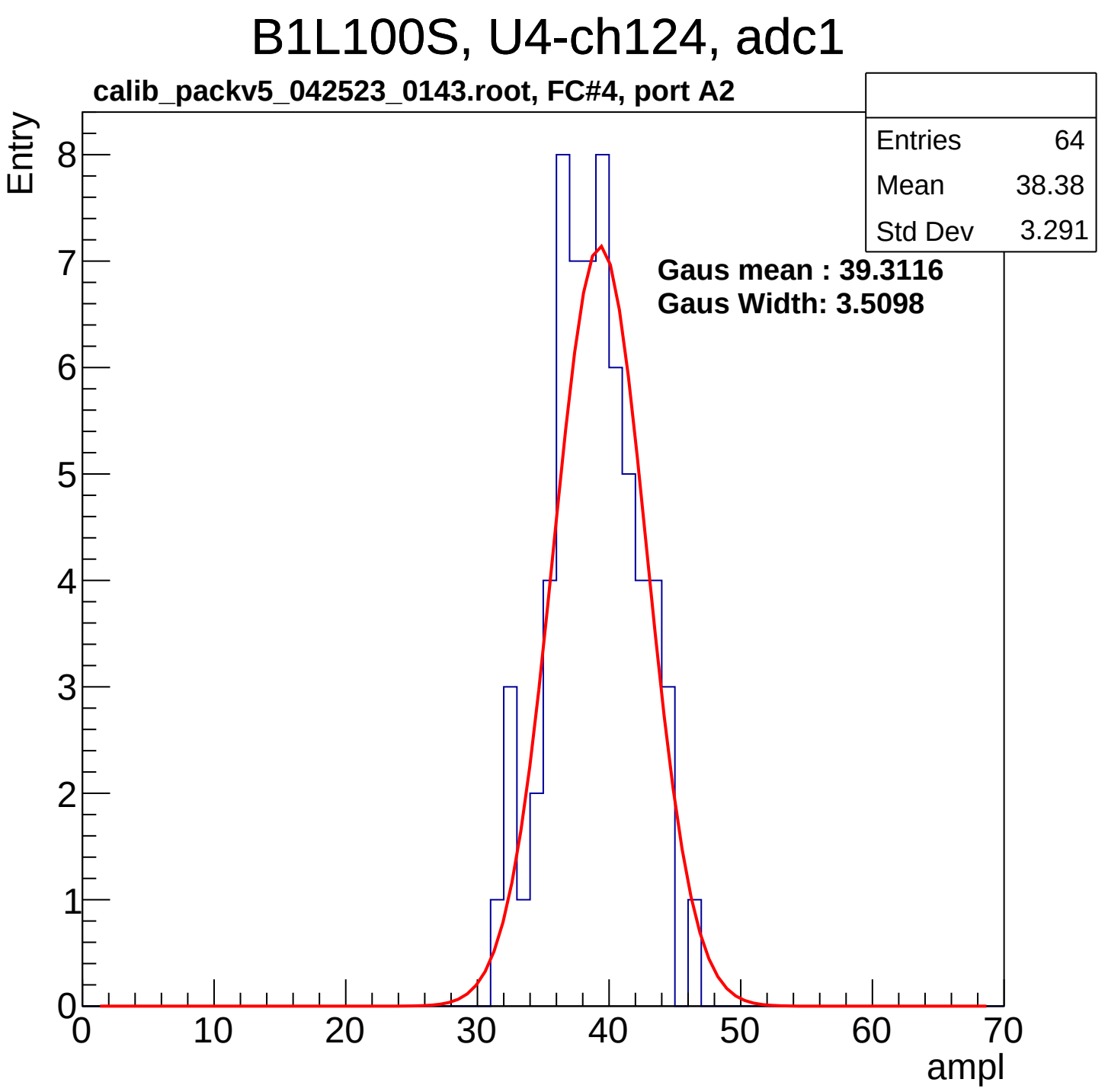

B1L100S, U4-ch123, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 56.45
Std Dev 3.13
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

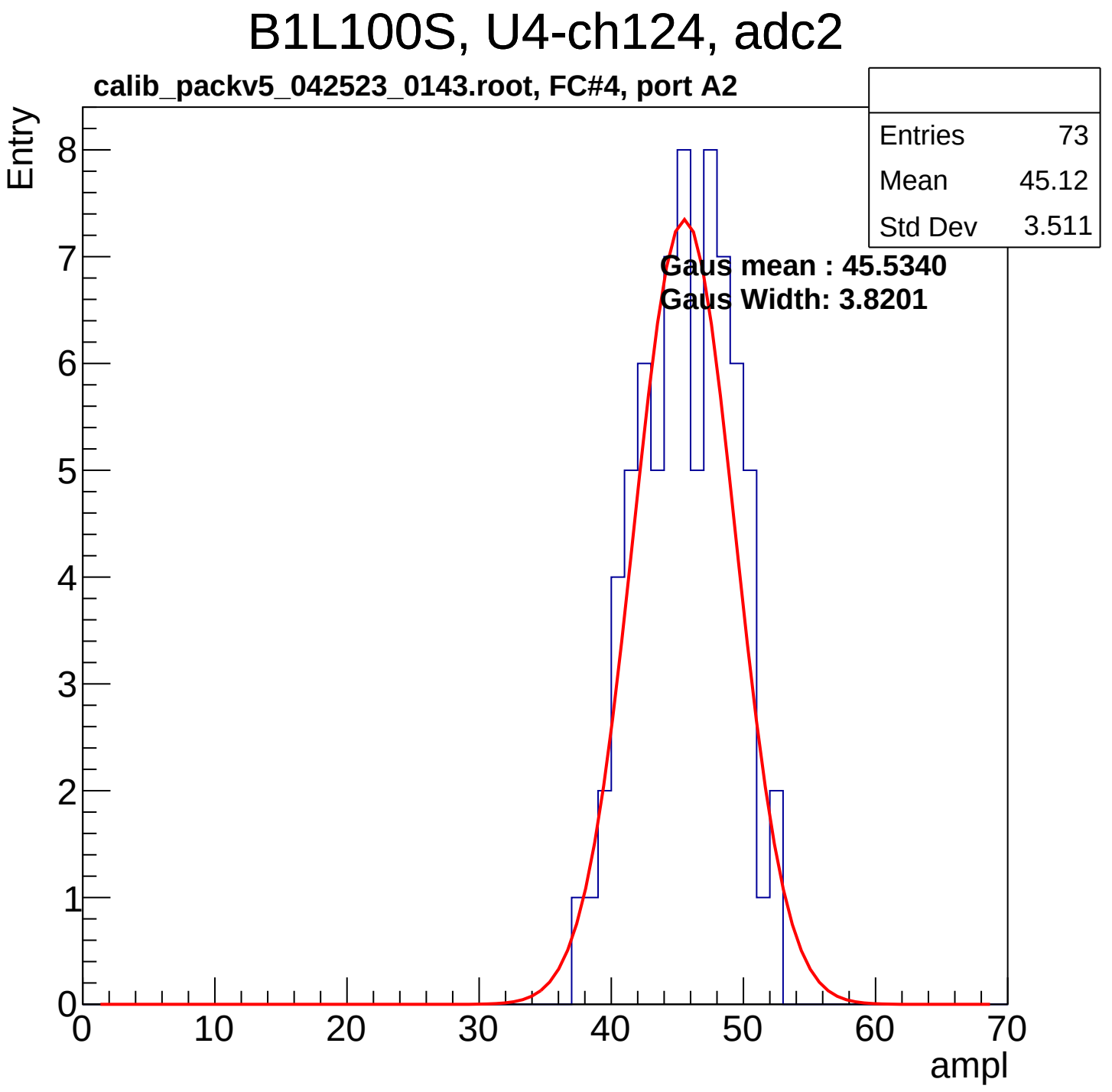

B1L100S, U4-ch123, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 35
Mean 58.86
Std Dev 10.31
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

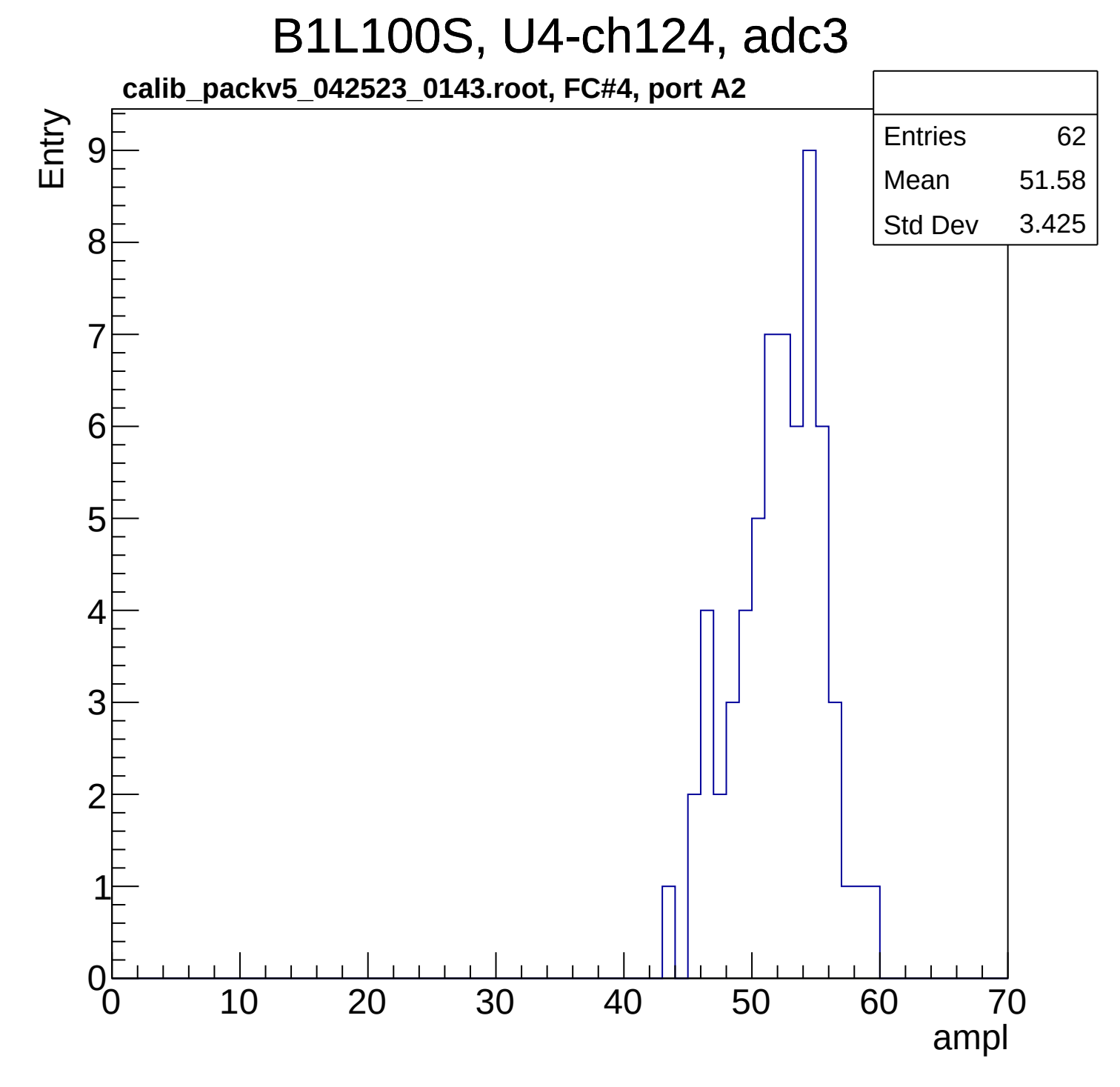

B1L100S, U4-ch123, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 62
Std Dev 0.7071
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

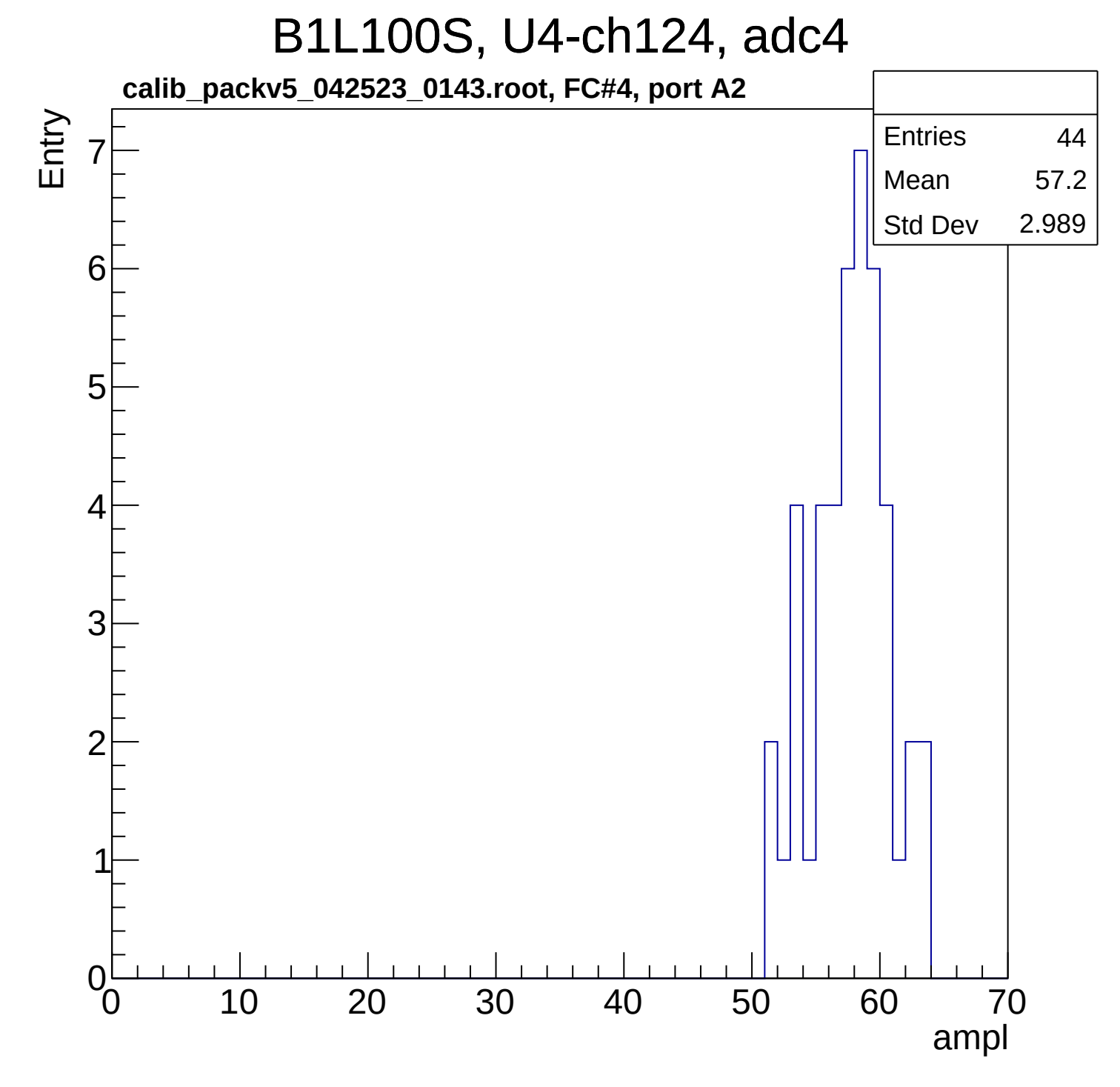

B1L100S, U4-ch123, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

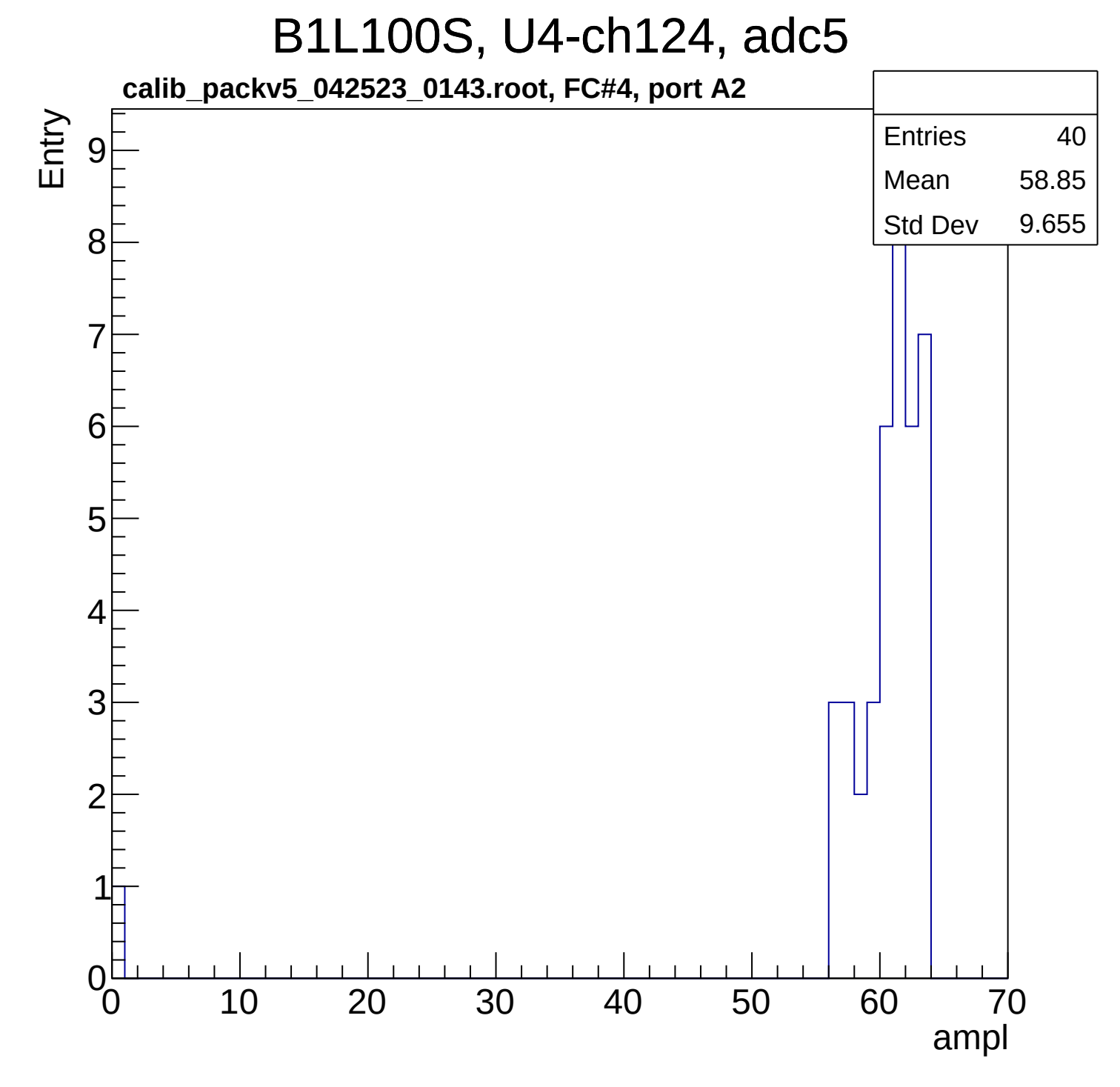

B1L100S, U4-ch124, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 30.62
Std Dev 3.894
Gaus mean : 31.6933
Gaus Width: 3.7494
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

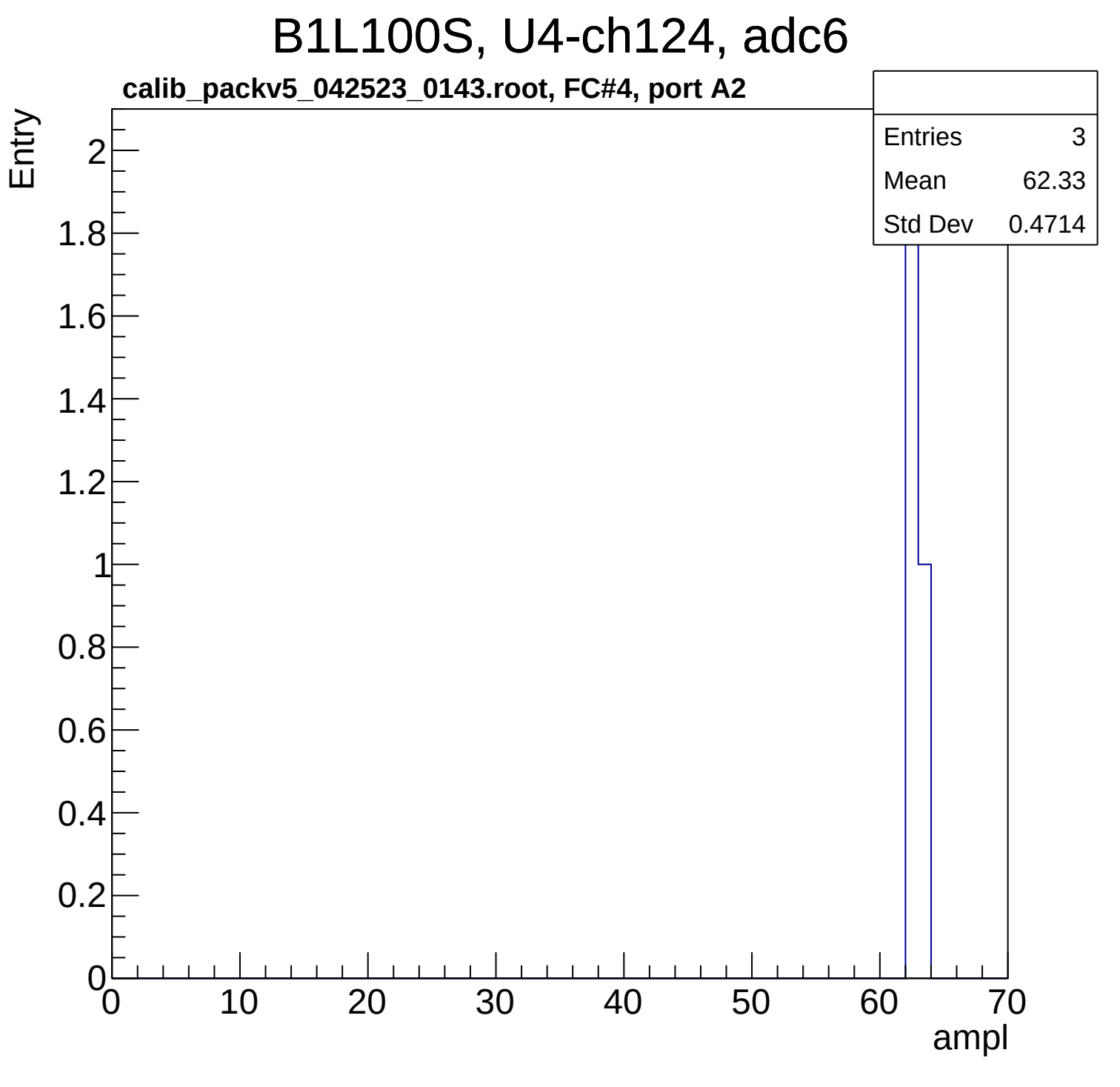

B1L100S, U4-ch124, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 38.38
Std Dev 3.291
Gaus mean : 39.3116
Gaus Width: 3.5098
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

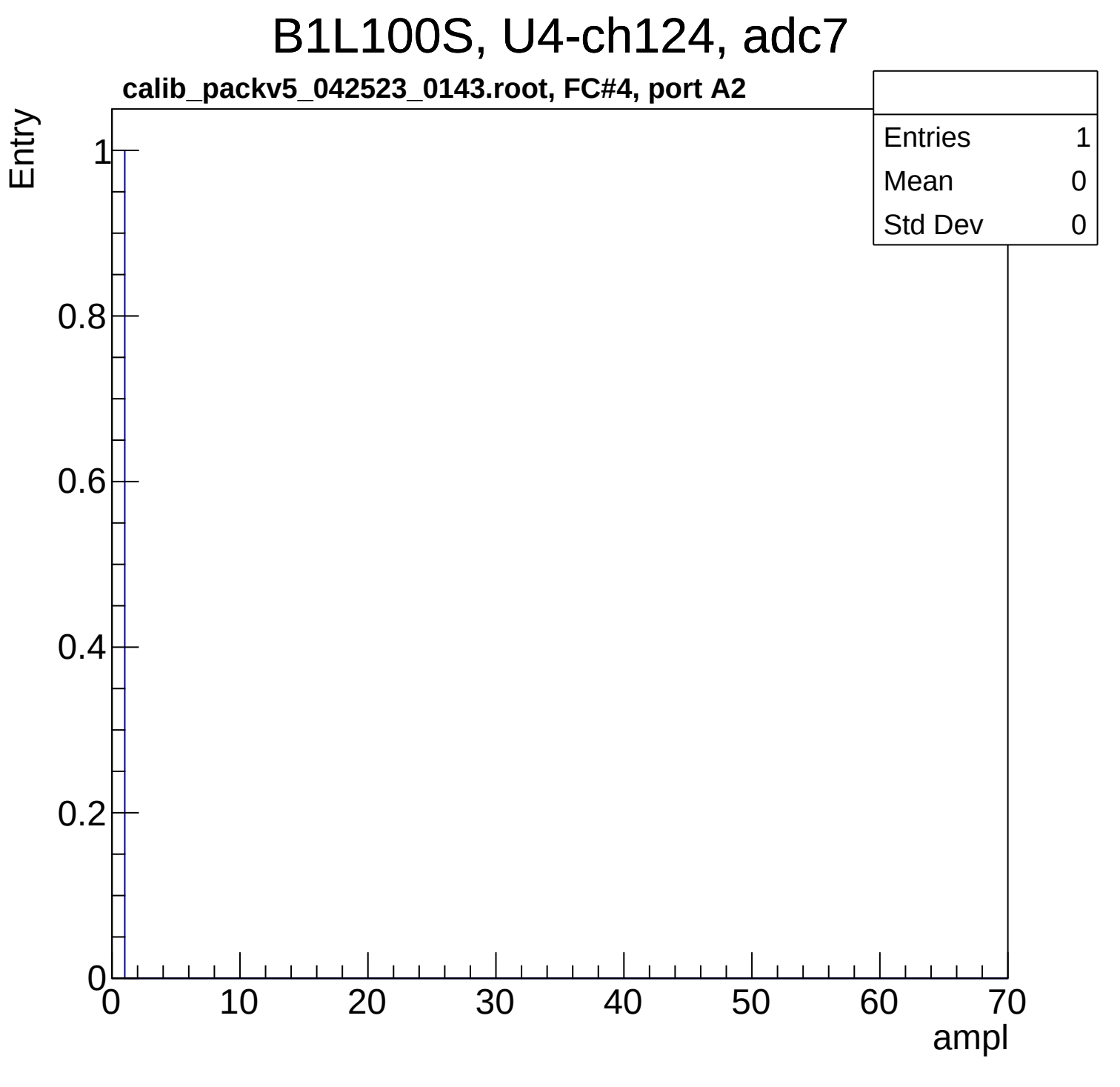

B1L100S, U4-ch124, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 45.12
Std Dev 3.511
Gaus mean : 45.5340
Gaus Width: 3.8201
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

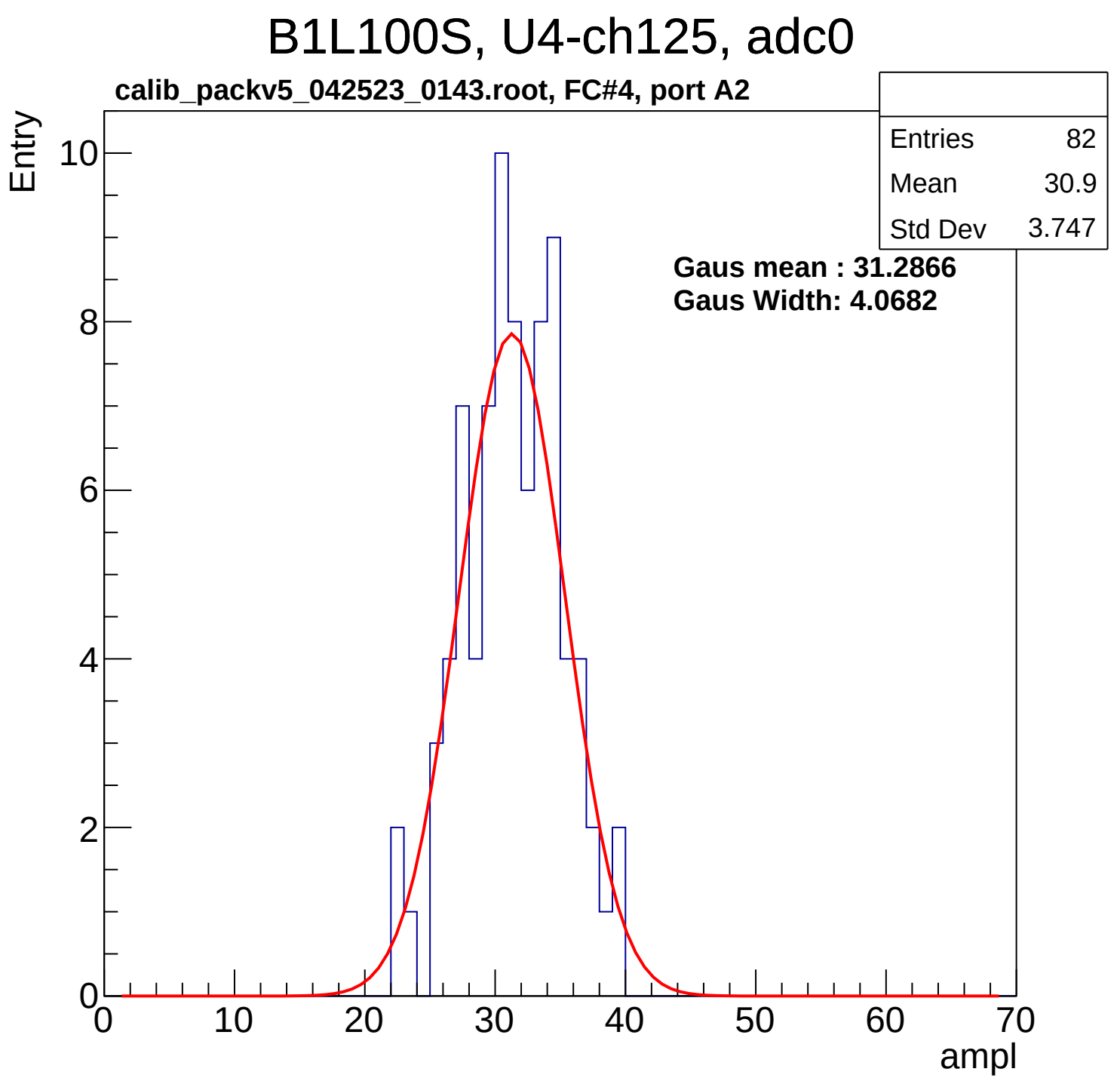

B1L100S, U4-ch124, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 51.58
Std Dev 3.425
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

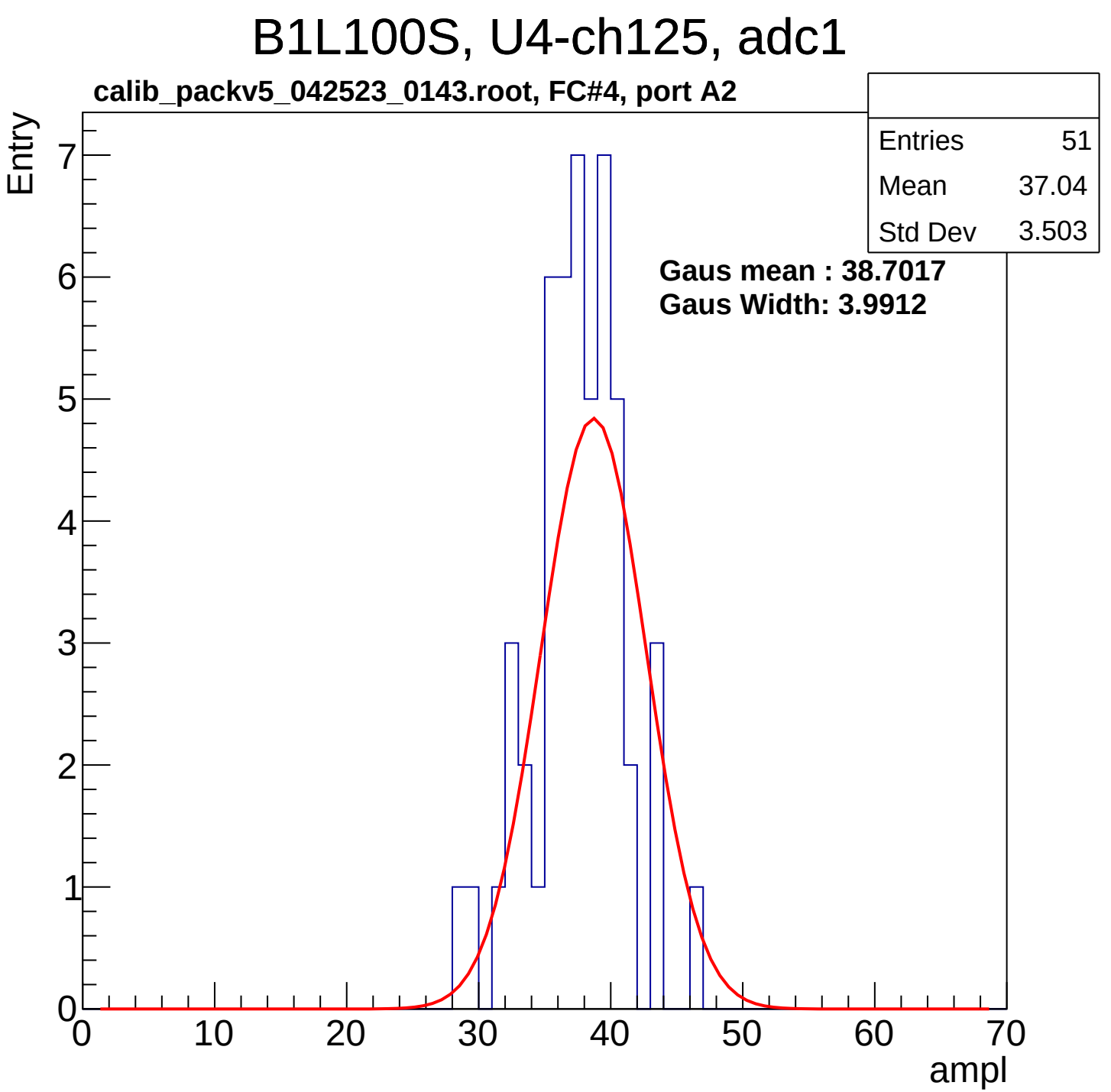

B1L100S, U4-ch124, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 44
Mean 57.2
Std Dev 2.989
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

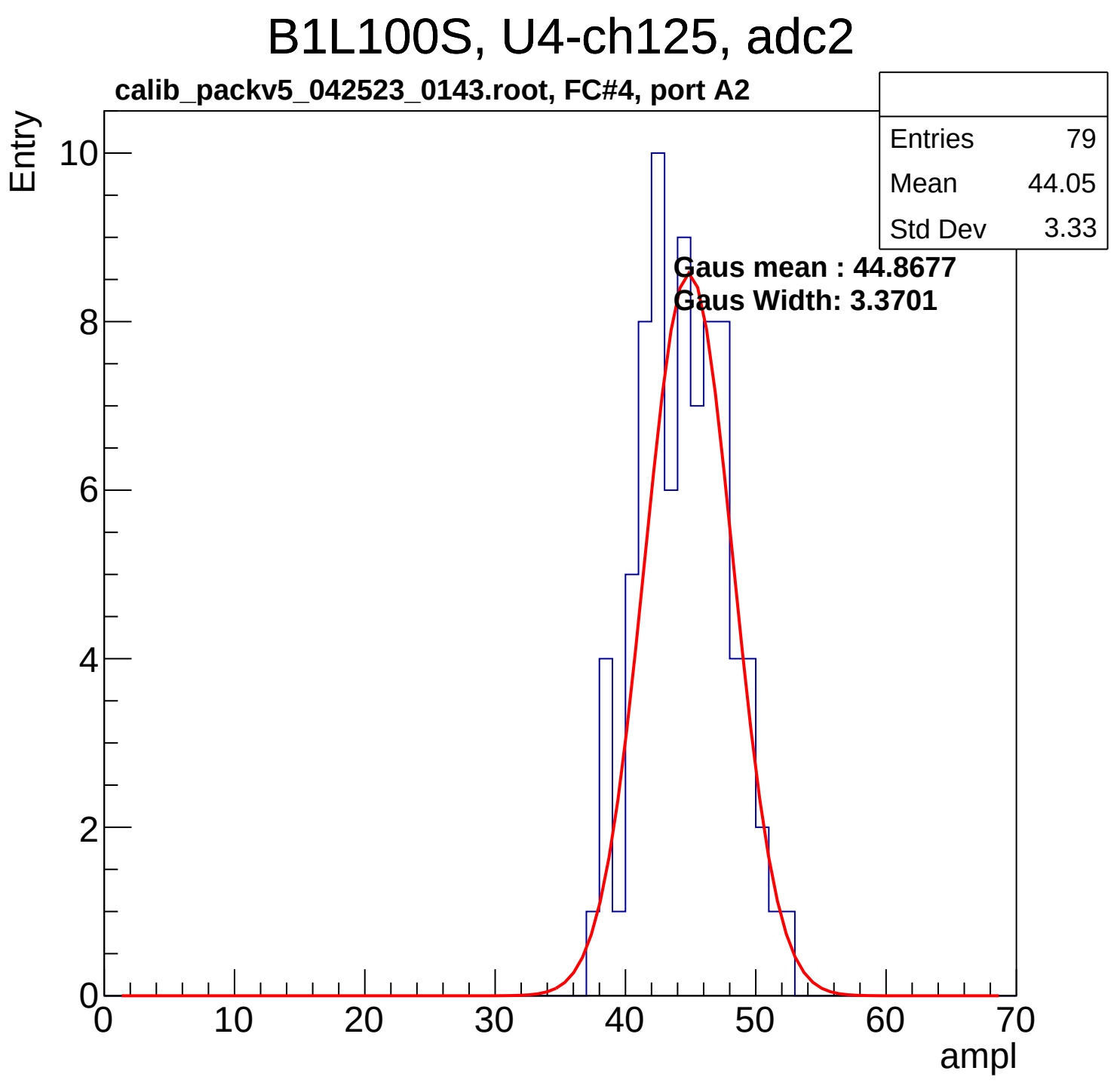

B1L100S, U4-ch124, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 40
Mean 58.85
Std Dev 9.655
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

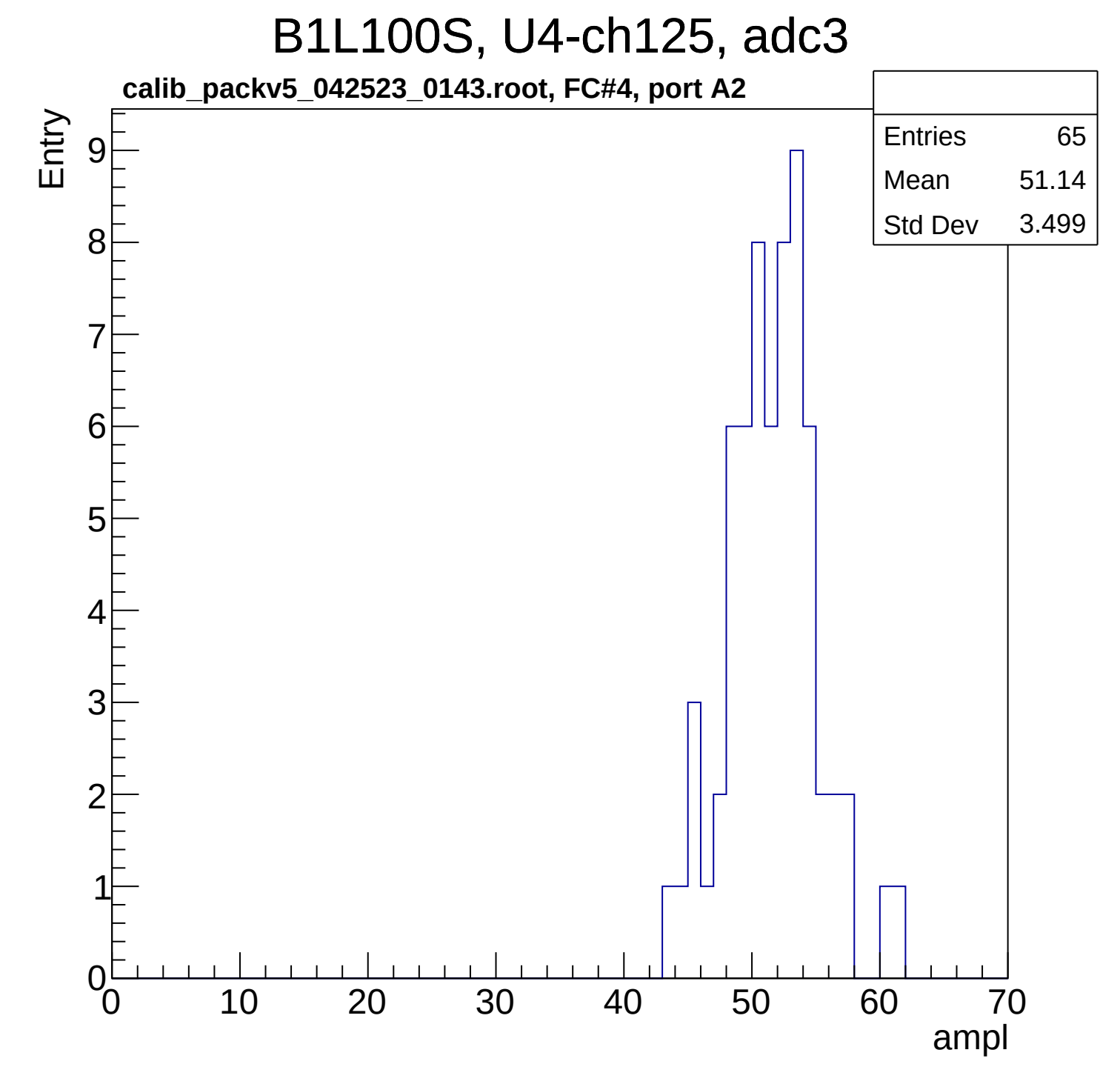

B1L100S, U4-ch124, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

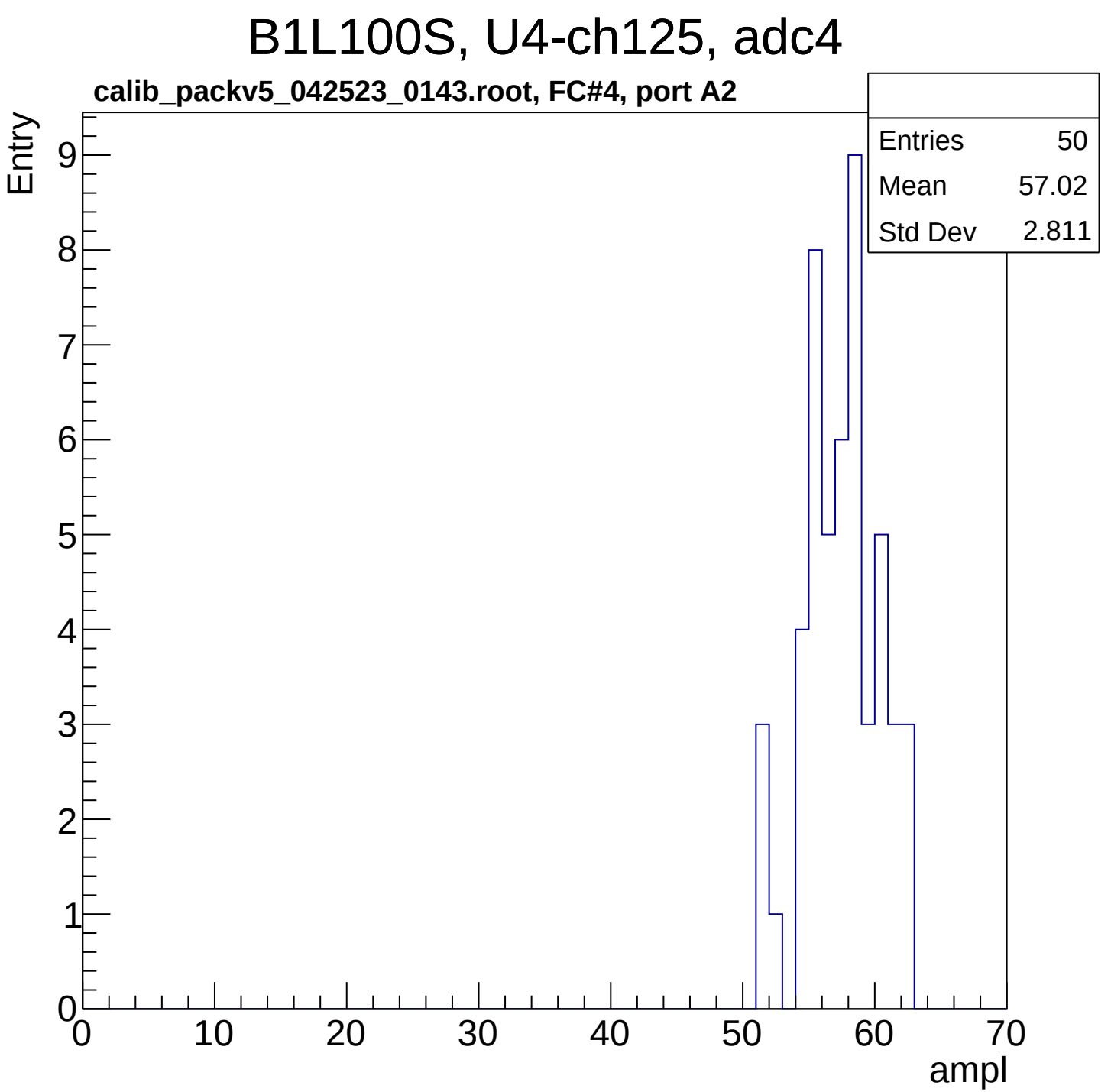

B1L100S, U4-ch124, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

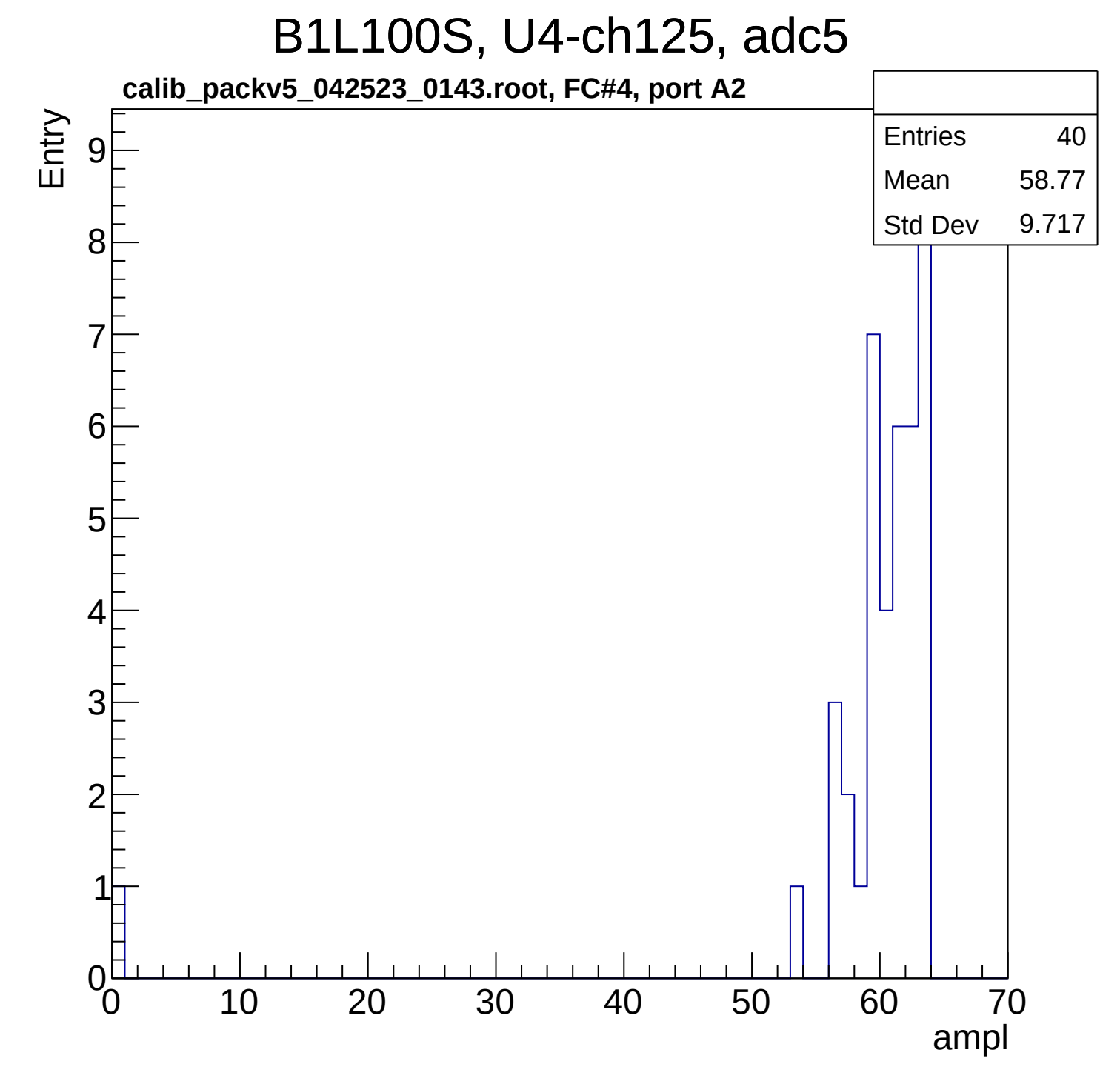

B1L100S, U4-ch125, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 30.9
Std Dev 3.747
Gaus mean : 31.2866
Gaus Width: 4.0682
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

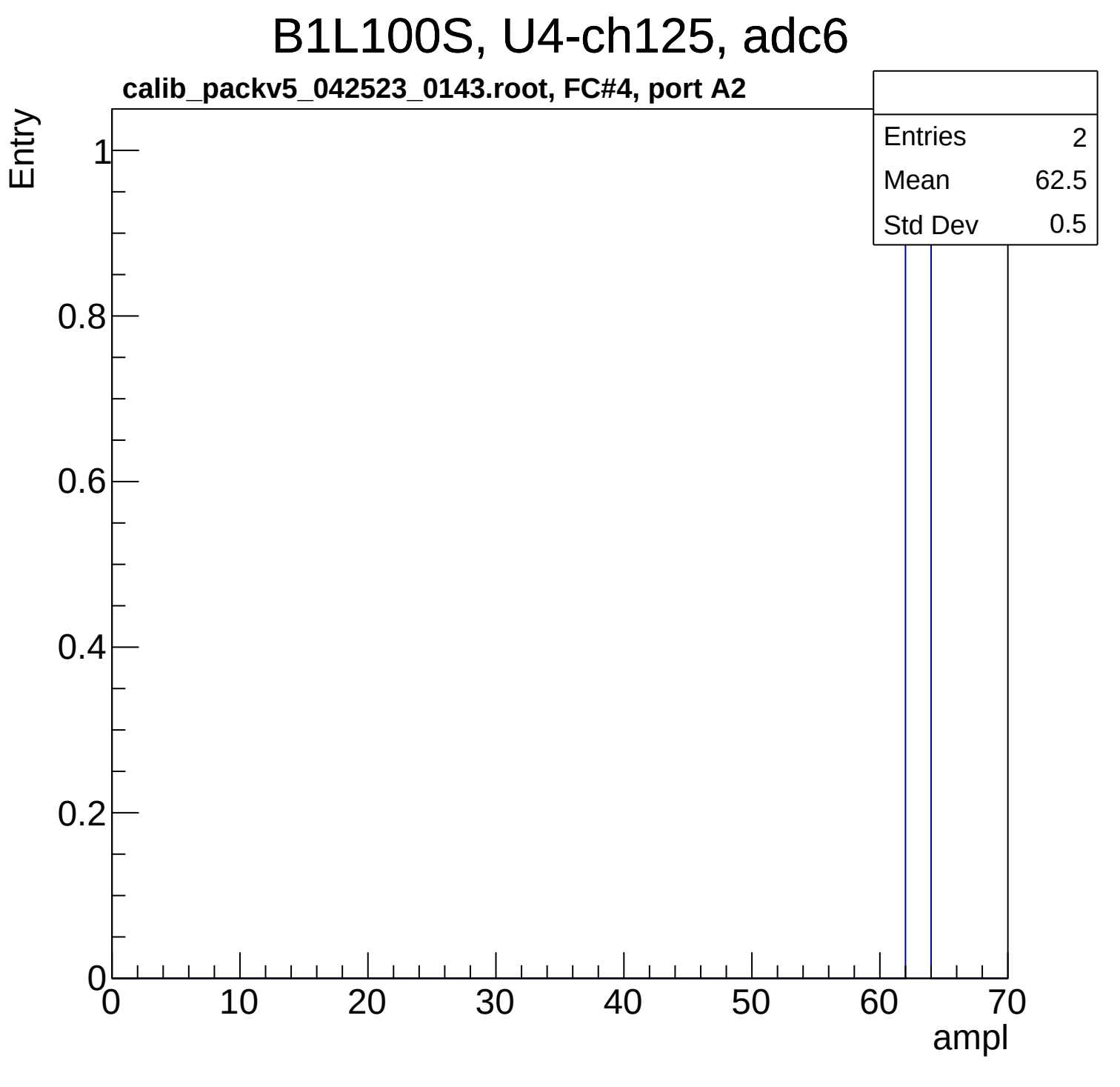

B1L100S, U4-ch125, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 37.04
Std Dev 3.503
Gaus mean : 38.7017
Gaus Width: 3.9912
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

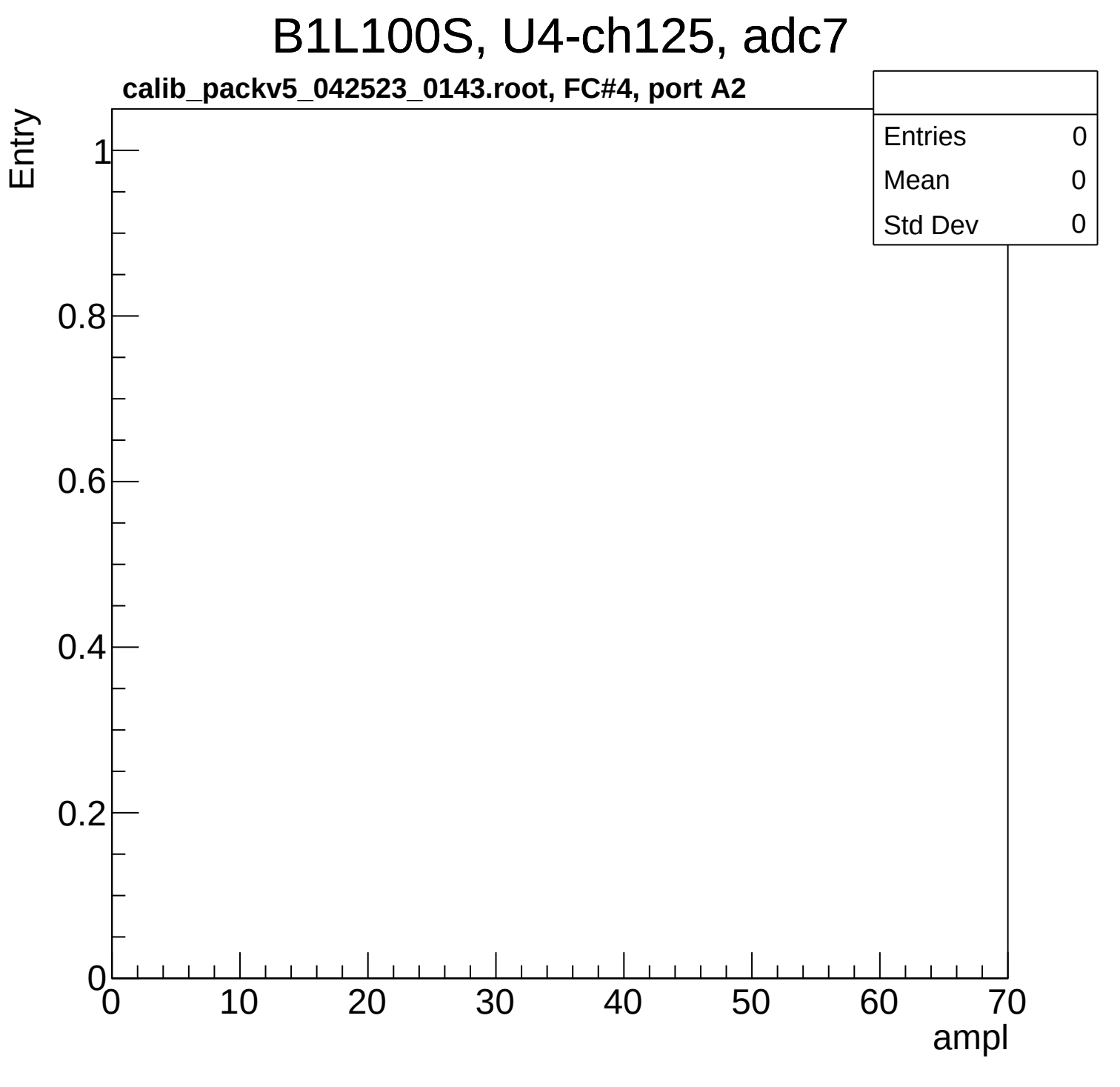

B1L100S, U4-ch125, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 44.05
Std Dev 3.33
Gaus mean : 44.8677
Gaus Width: 3.3701
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

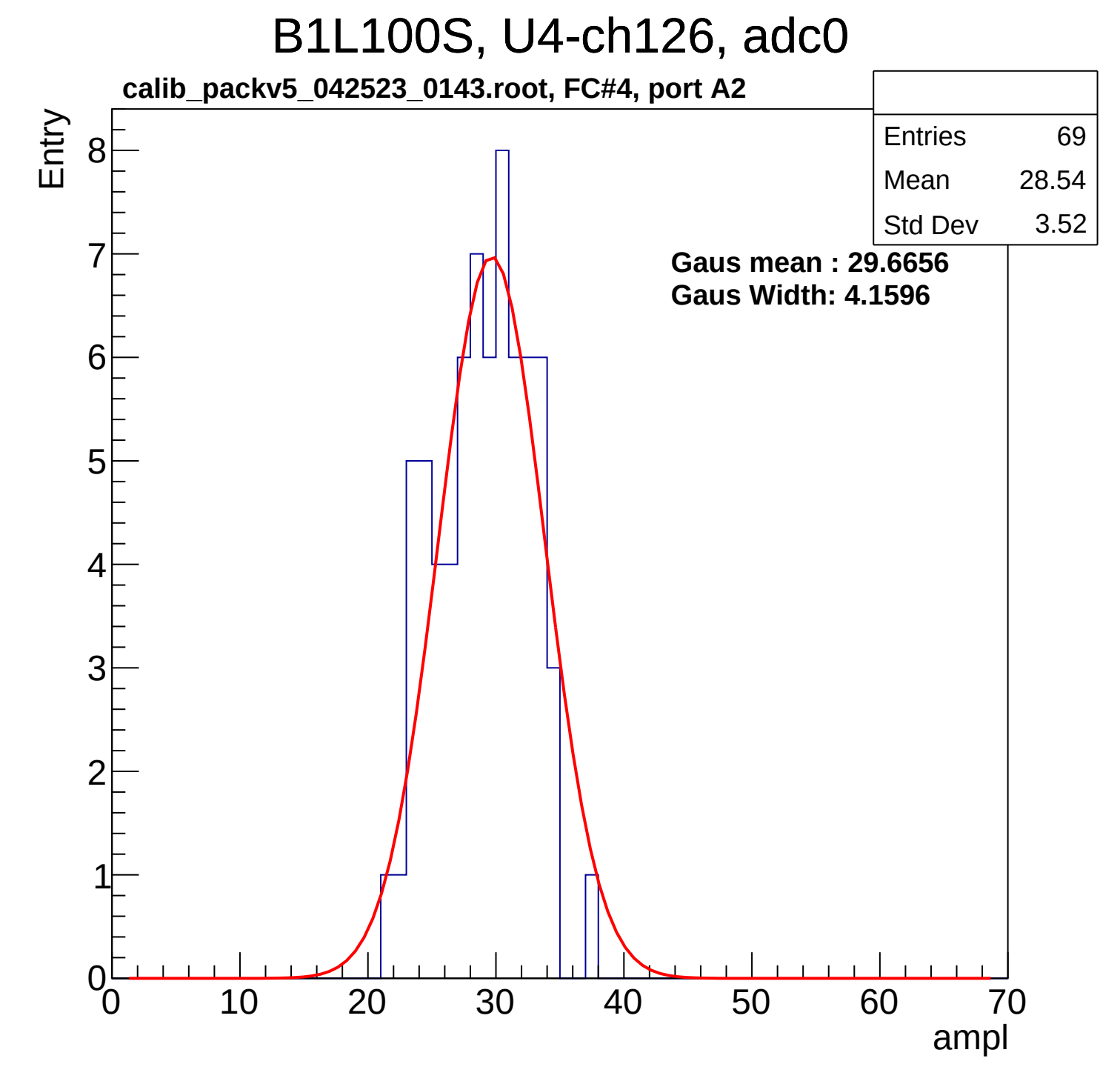

B1L100S, U4-ch125, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 51.14
Std Dev 3.499
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

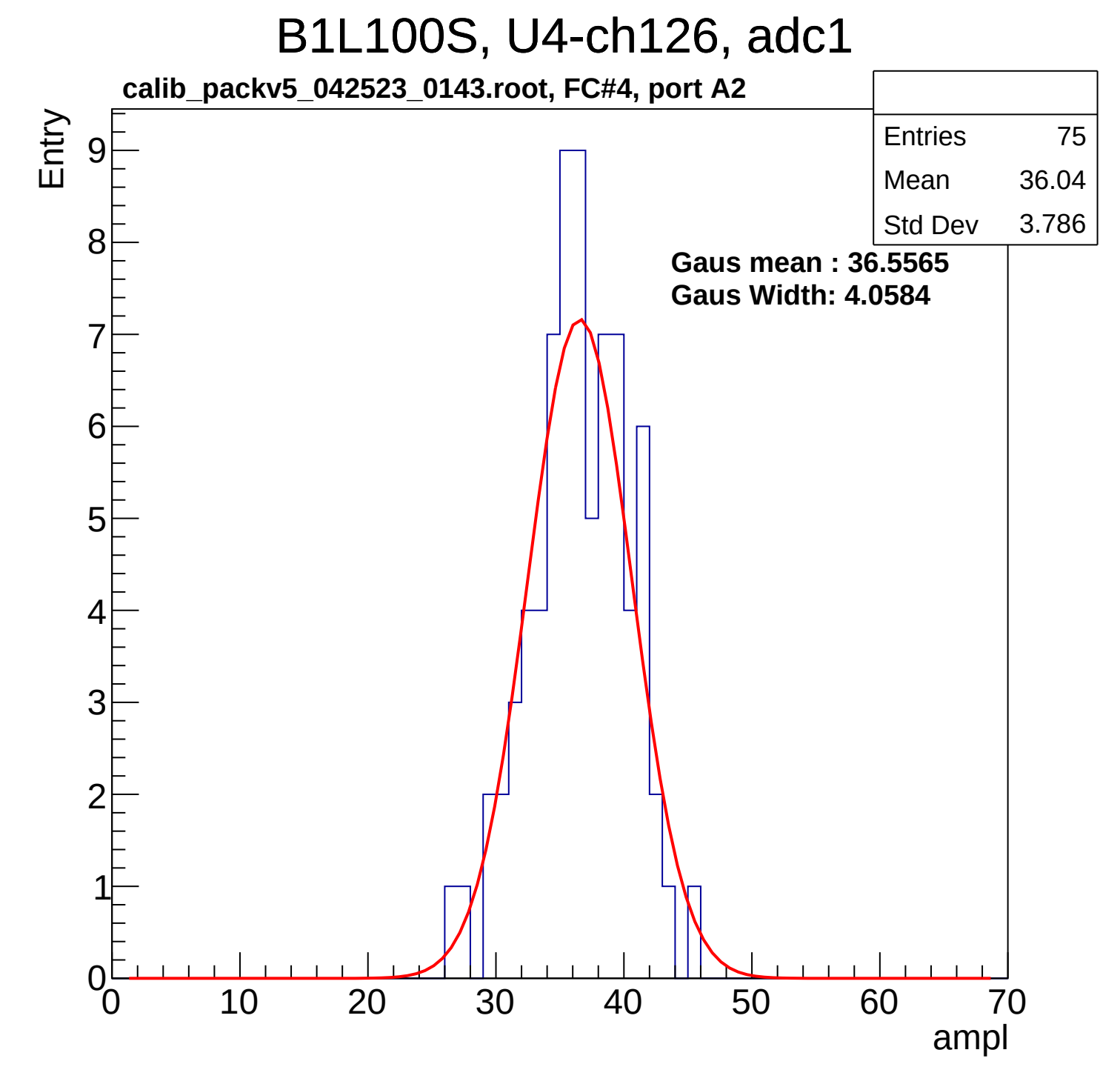

B1L100S, U4-ch125, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 57.02
Std Dev 2.811
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

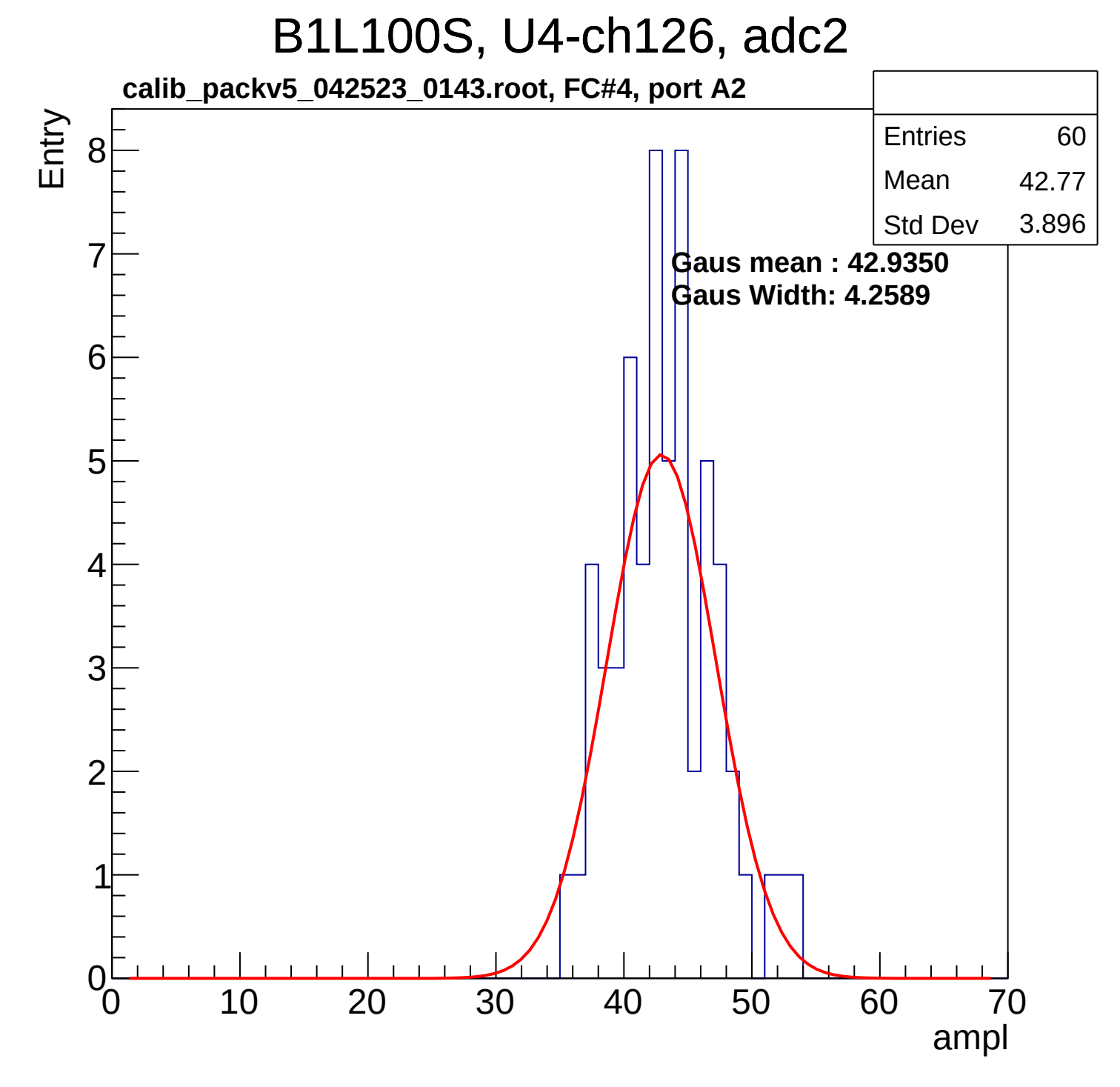

B1L100S, U4-ch125, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 40
Mean 58.77
Std Dev 9.717
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

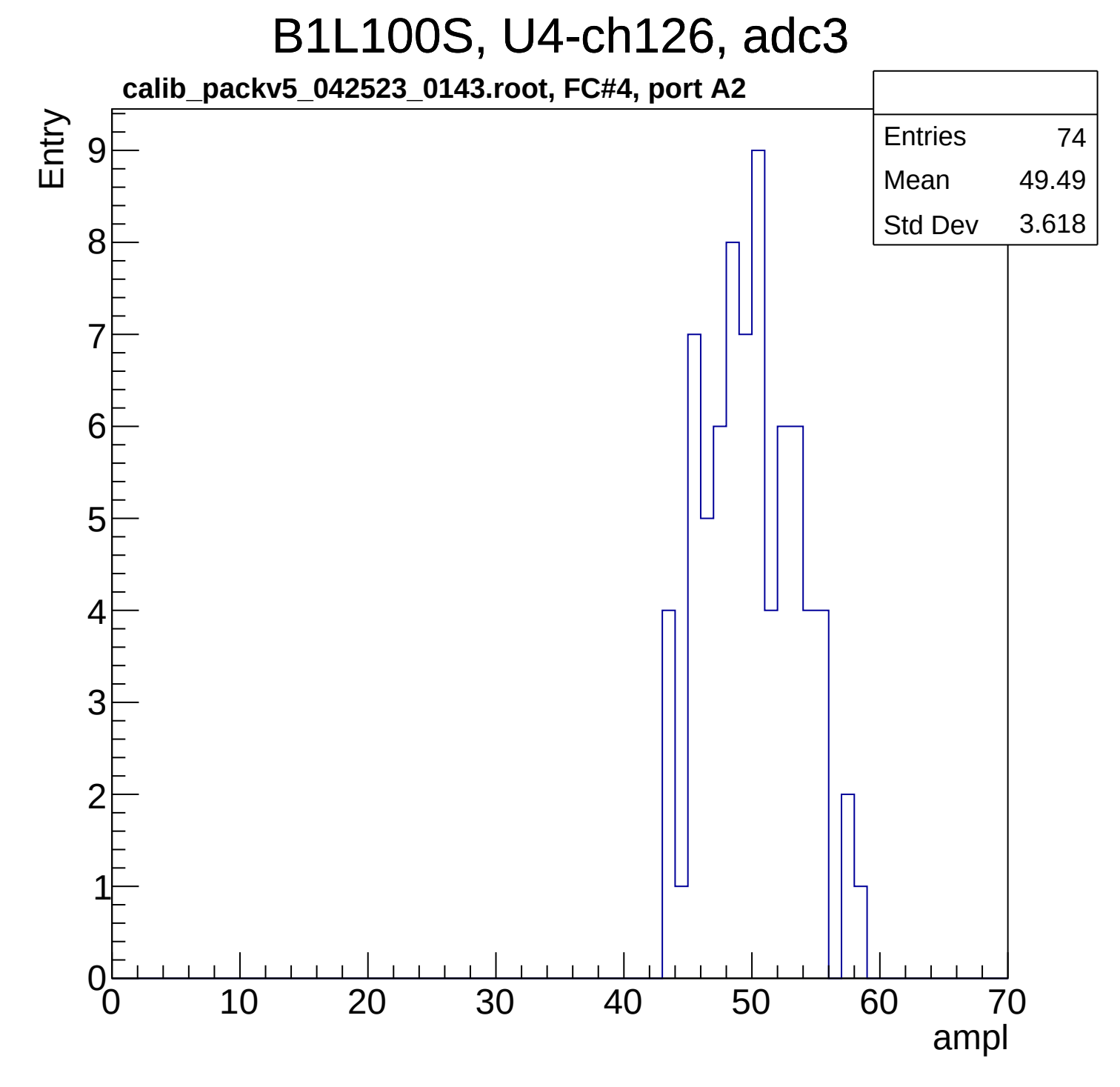

B1L100S, U4-ch125, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

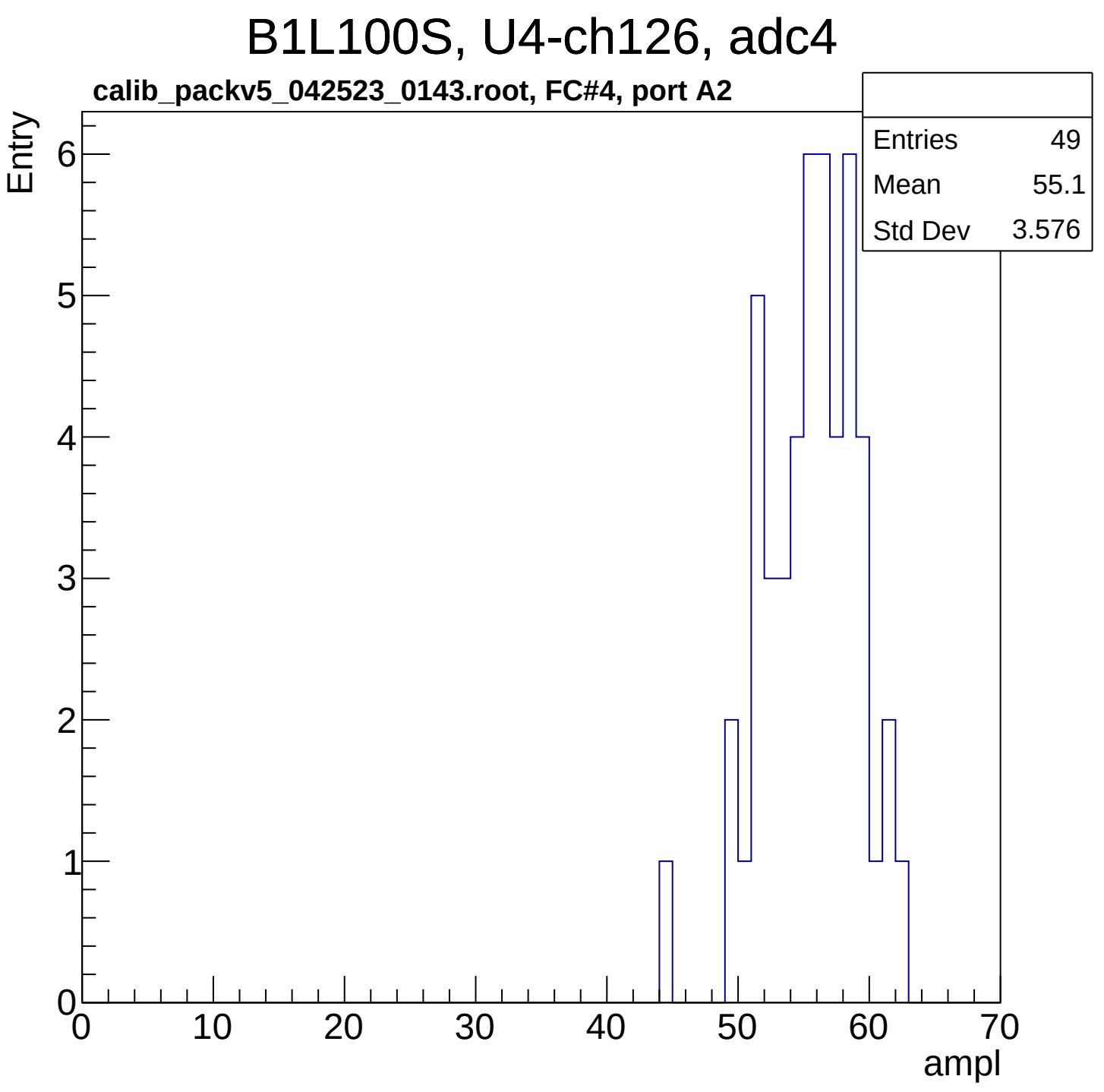

B1L100S, U4-ch125, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

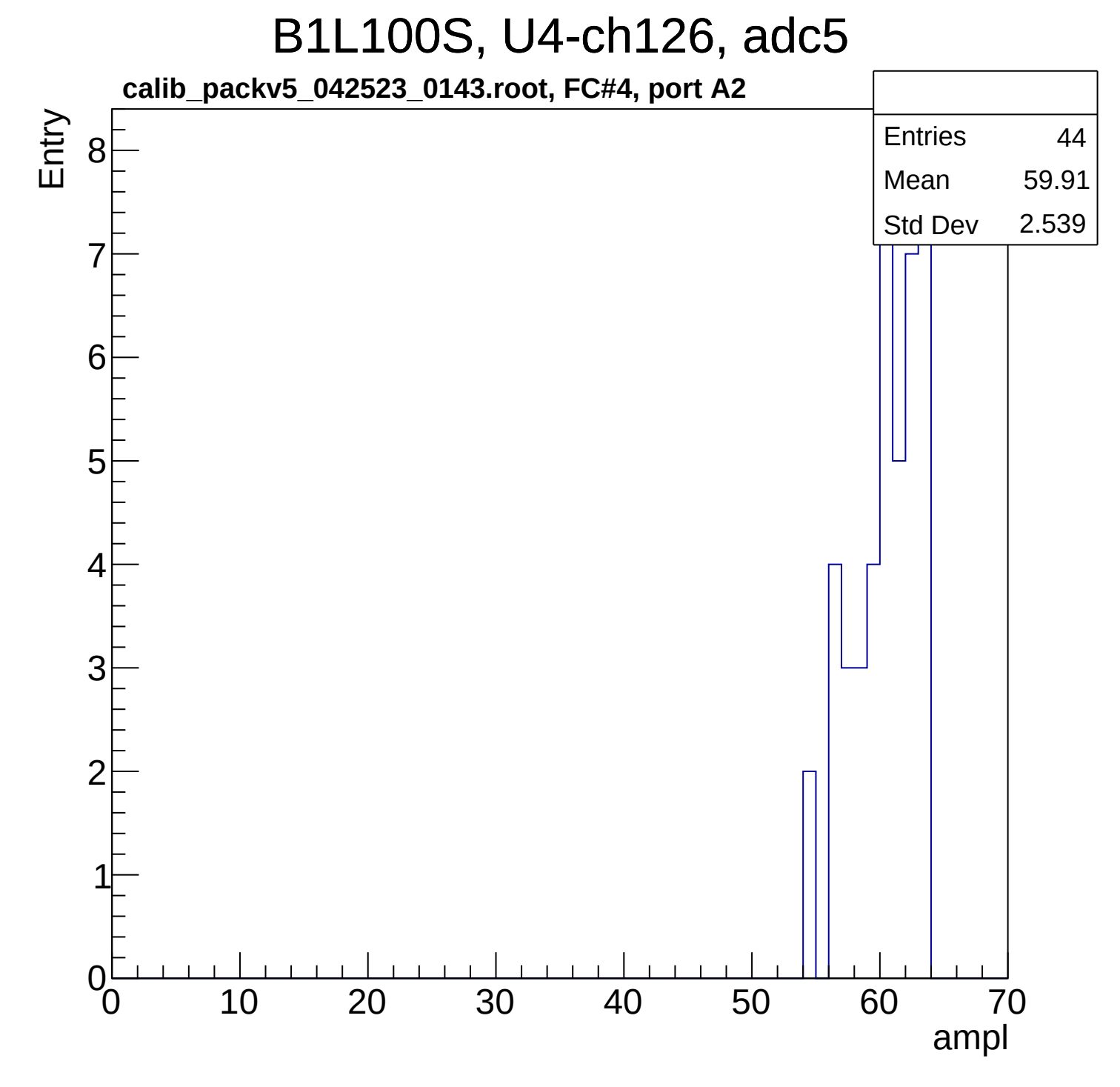

B1L100S, U4-ch126, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 28.54
Std Dev 3.52
Gaus mean : 29.6656
Gaus Width: 4.1596
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

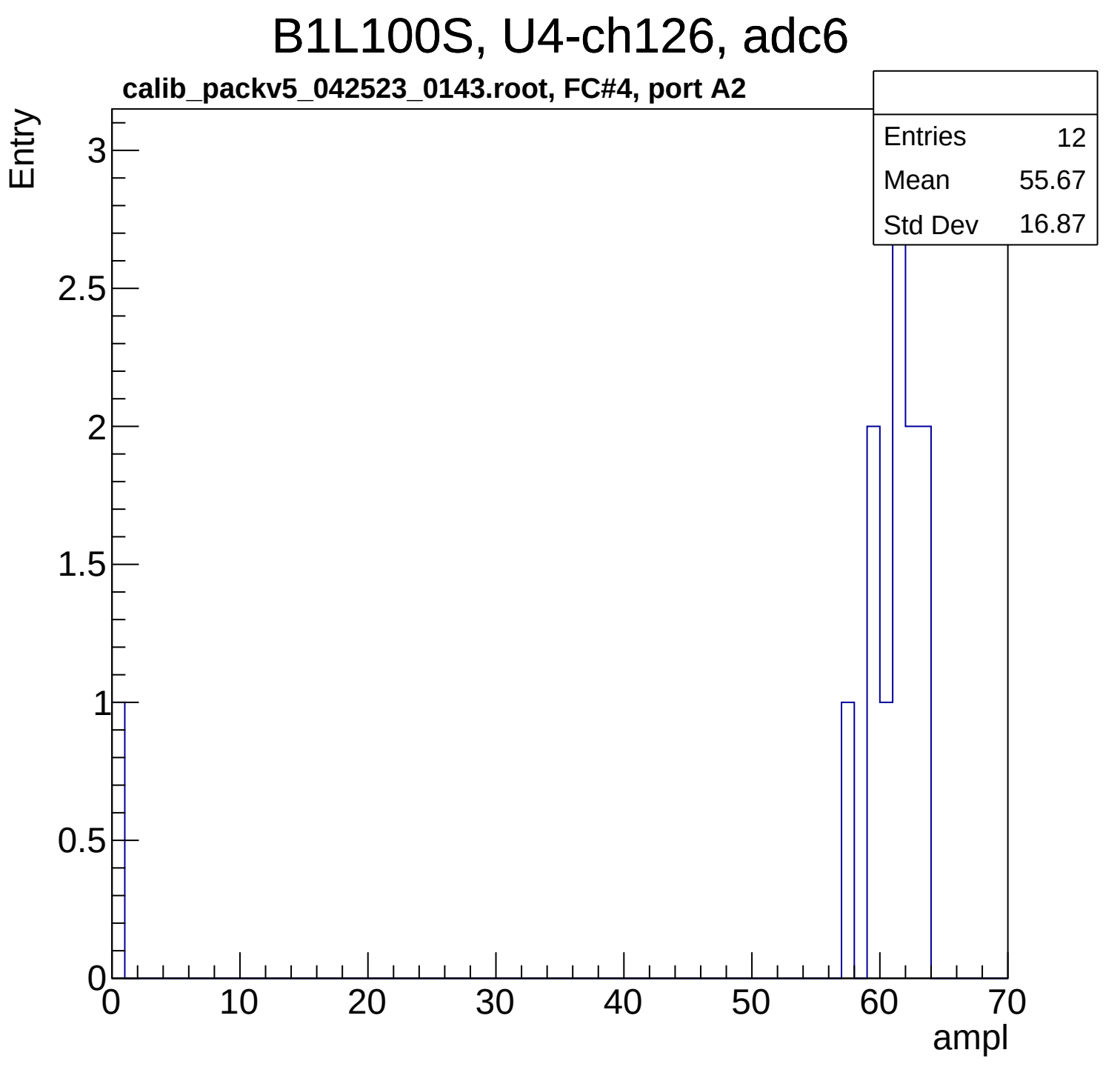

B1L100S, U4-ch126, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 36.04
Std Dev 3.786
Gaus mean : 36.5565
Gaus Width: 4.0584
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

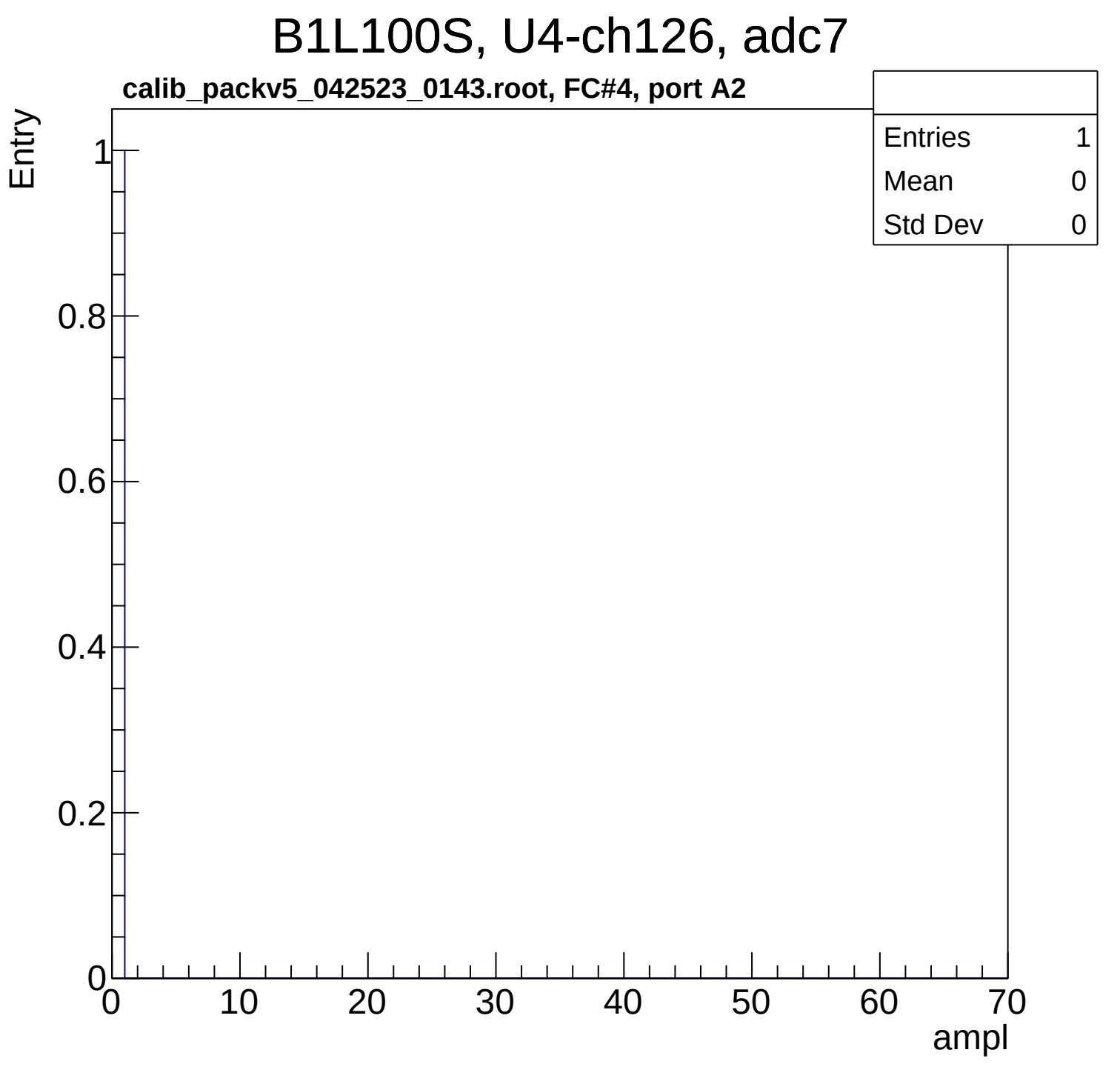

B1L100S, U4-ch126, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 42.77
Std Dev 3.896
Gaus mean : 42.9350
Gaus Width: 4.2589
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

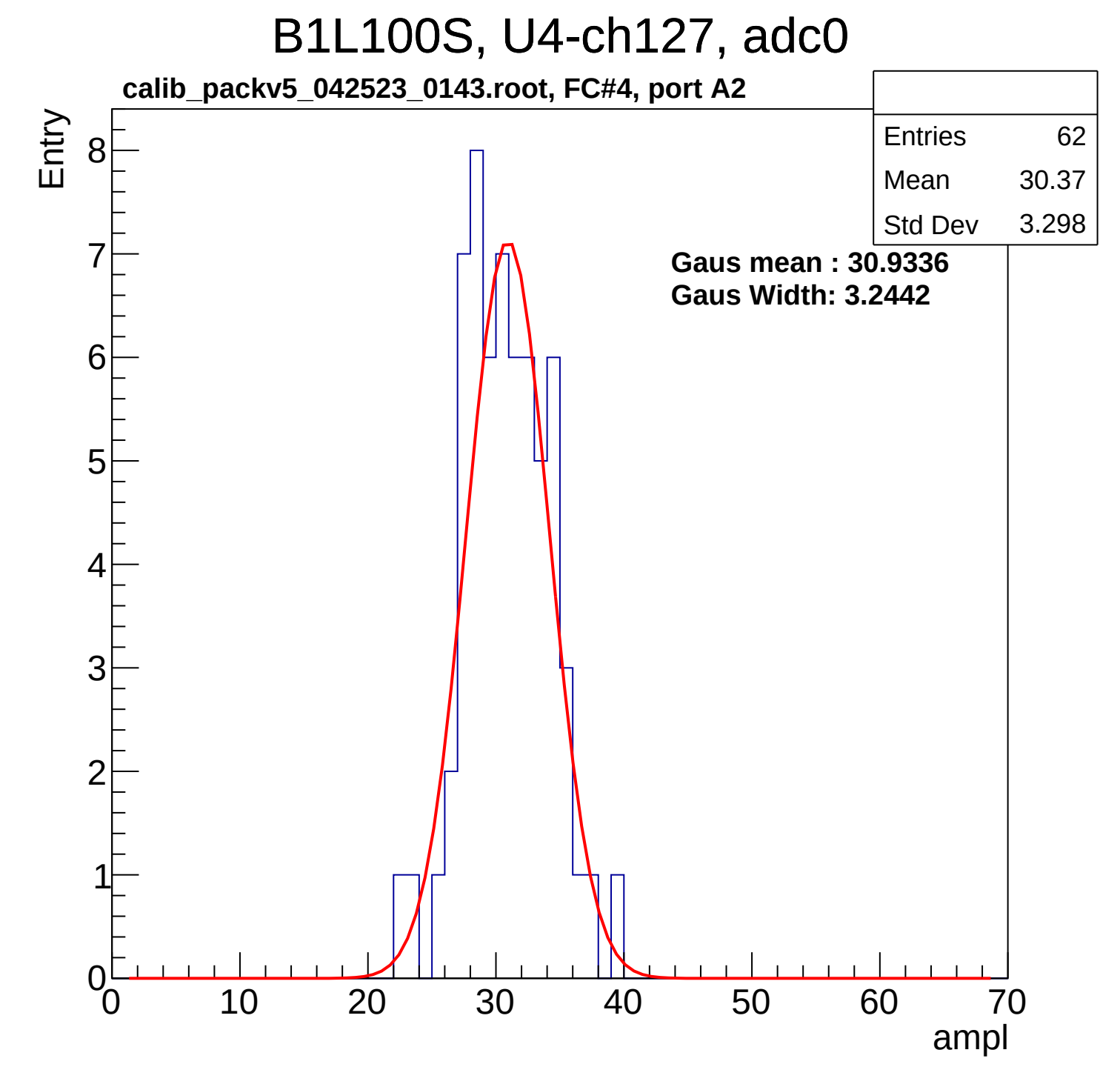

B1L100S, U4-ch126, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 49.49
Std Dev 3.618
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

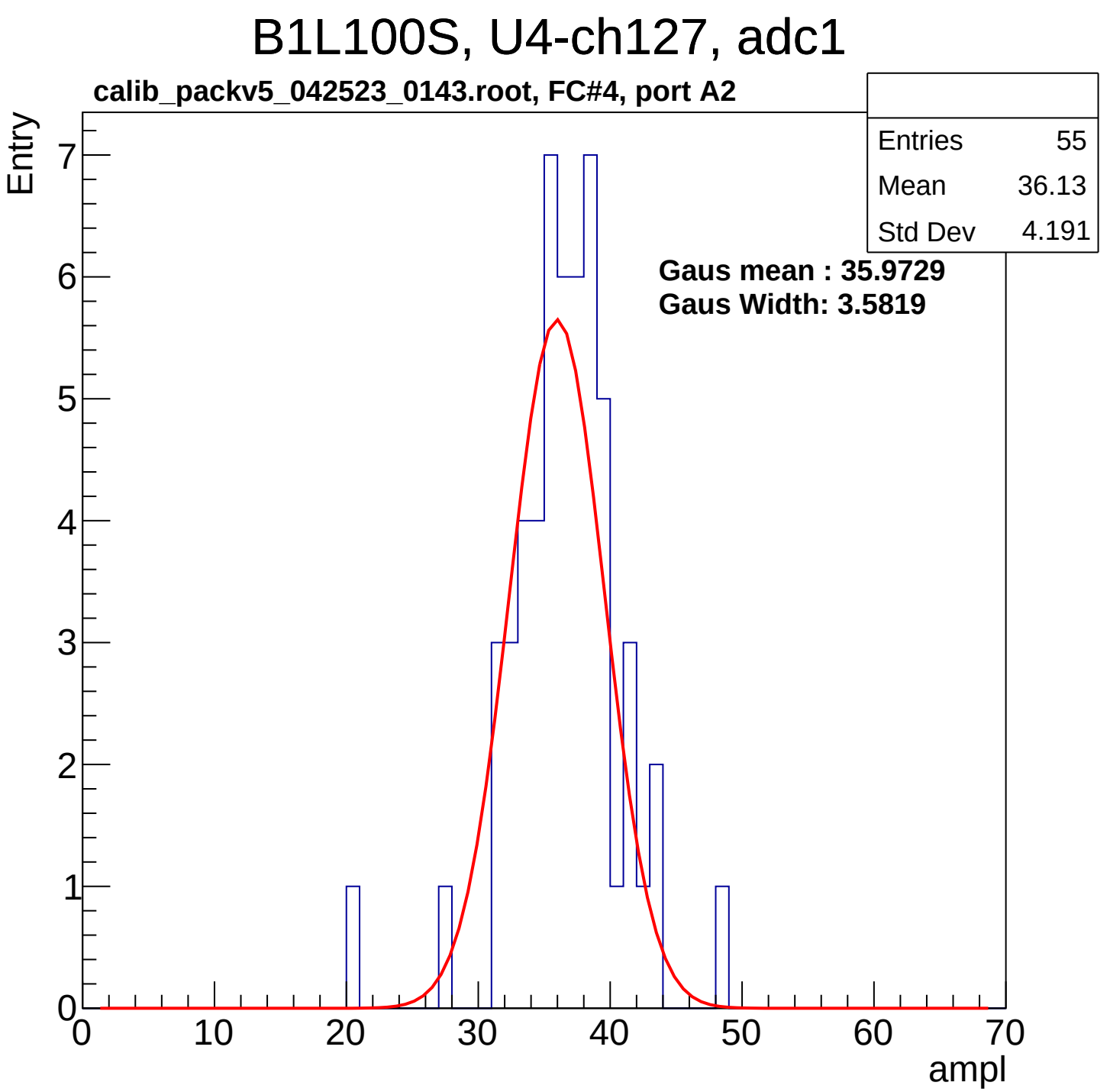

B1L100S, U4-ch126, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 55.1
Std Dev 3.576
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

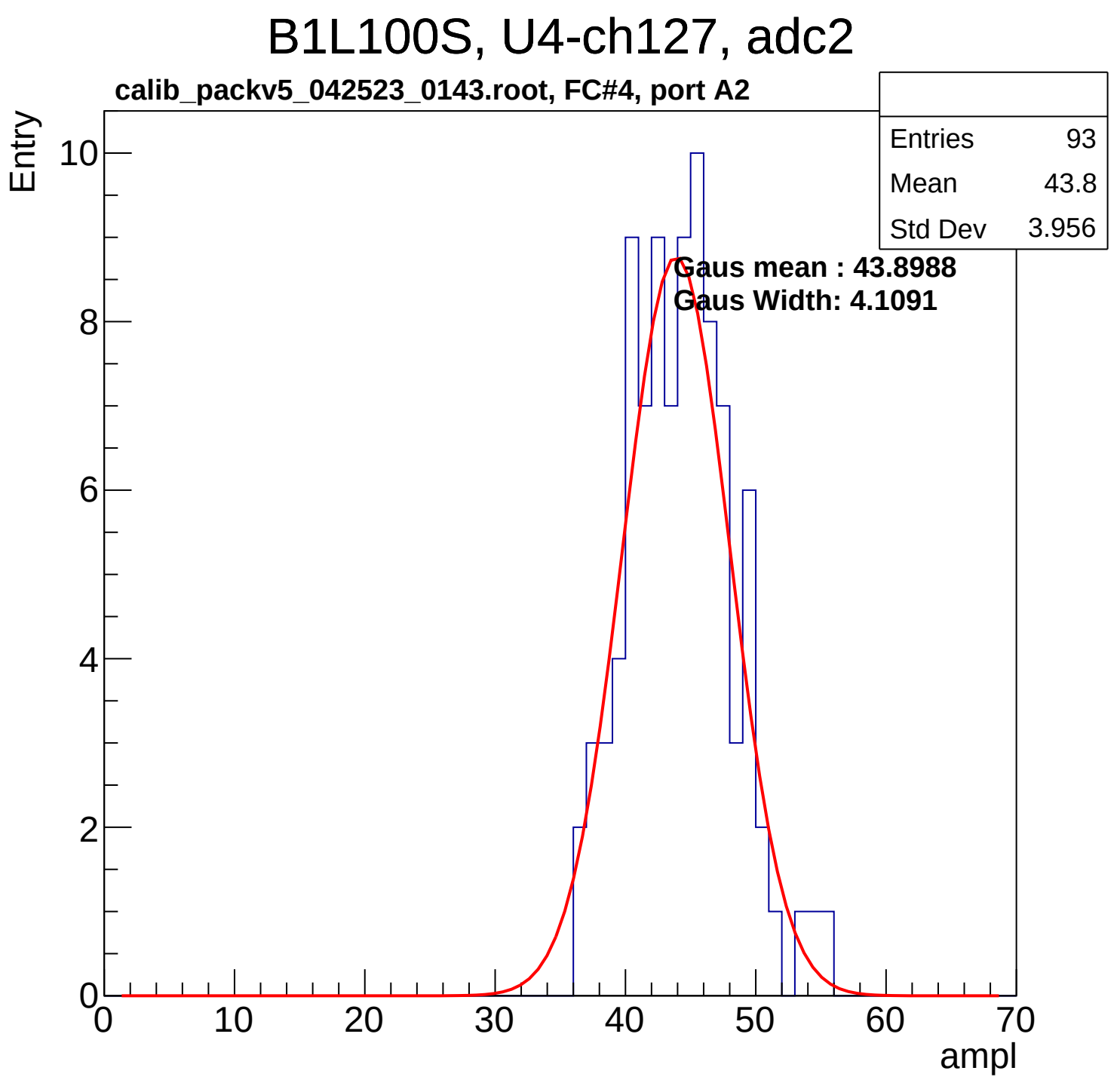

B1L100S, U4-ch126, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 44
Mean 59.91
Std Dev 2.539
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

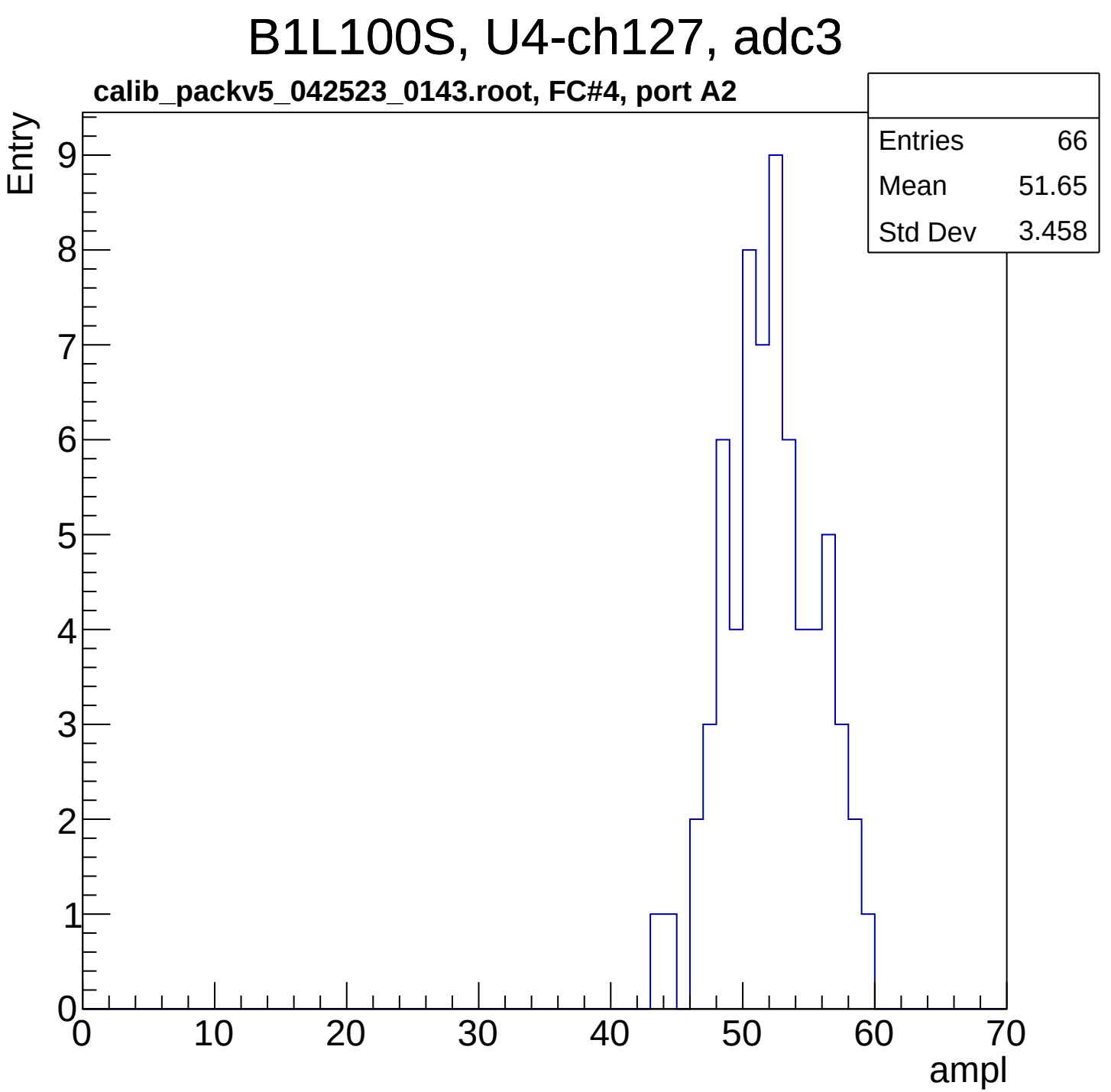

B1L100S, U4-ch126, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 12
Mean 55.67
Std Dev 16.87
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

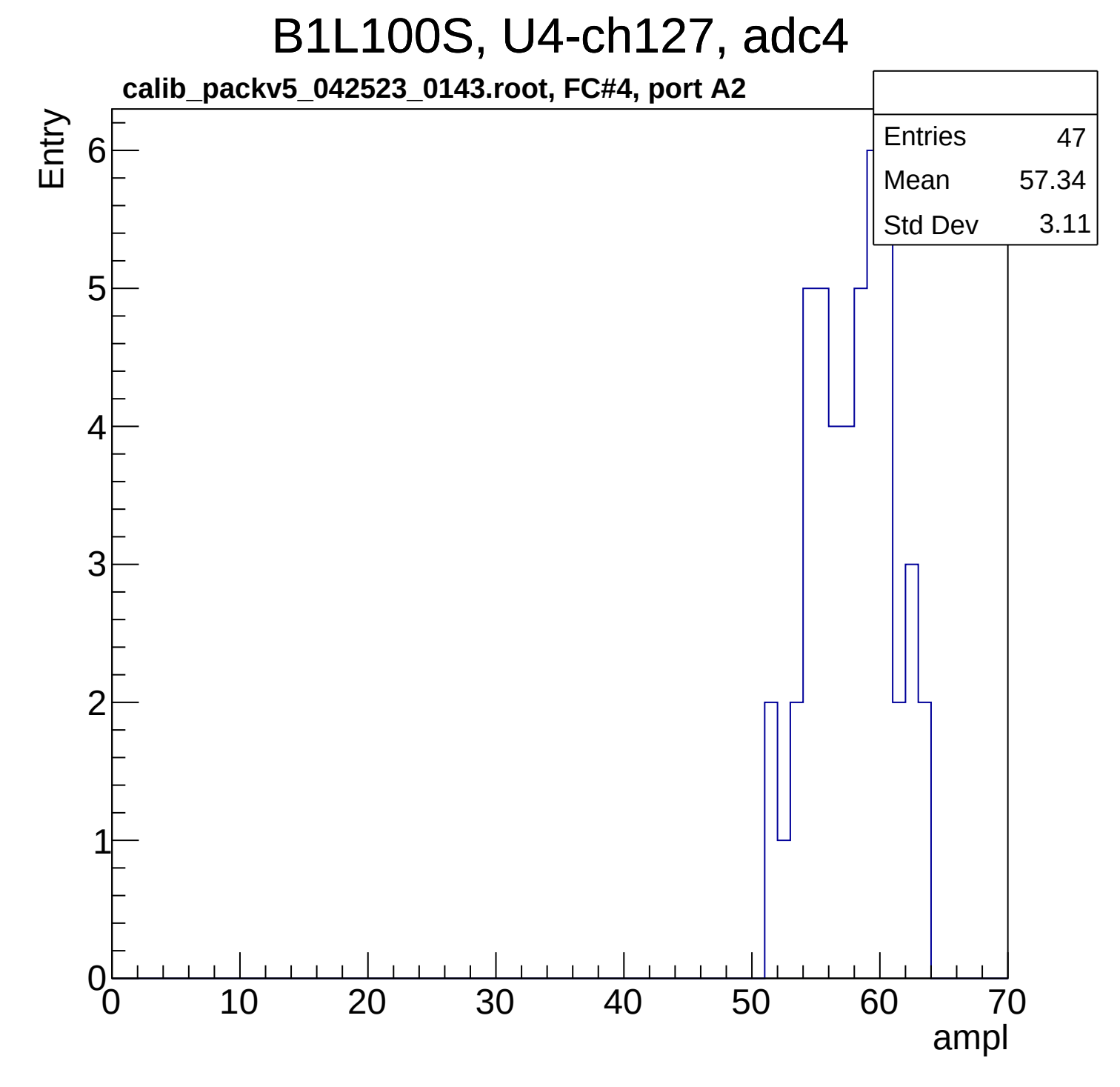

B1L100S, U4-ch126, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

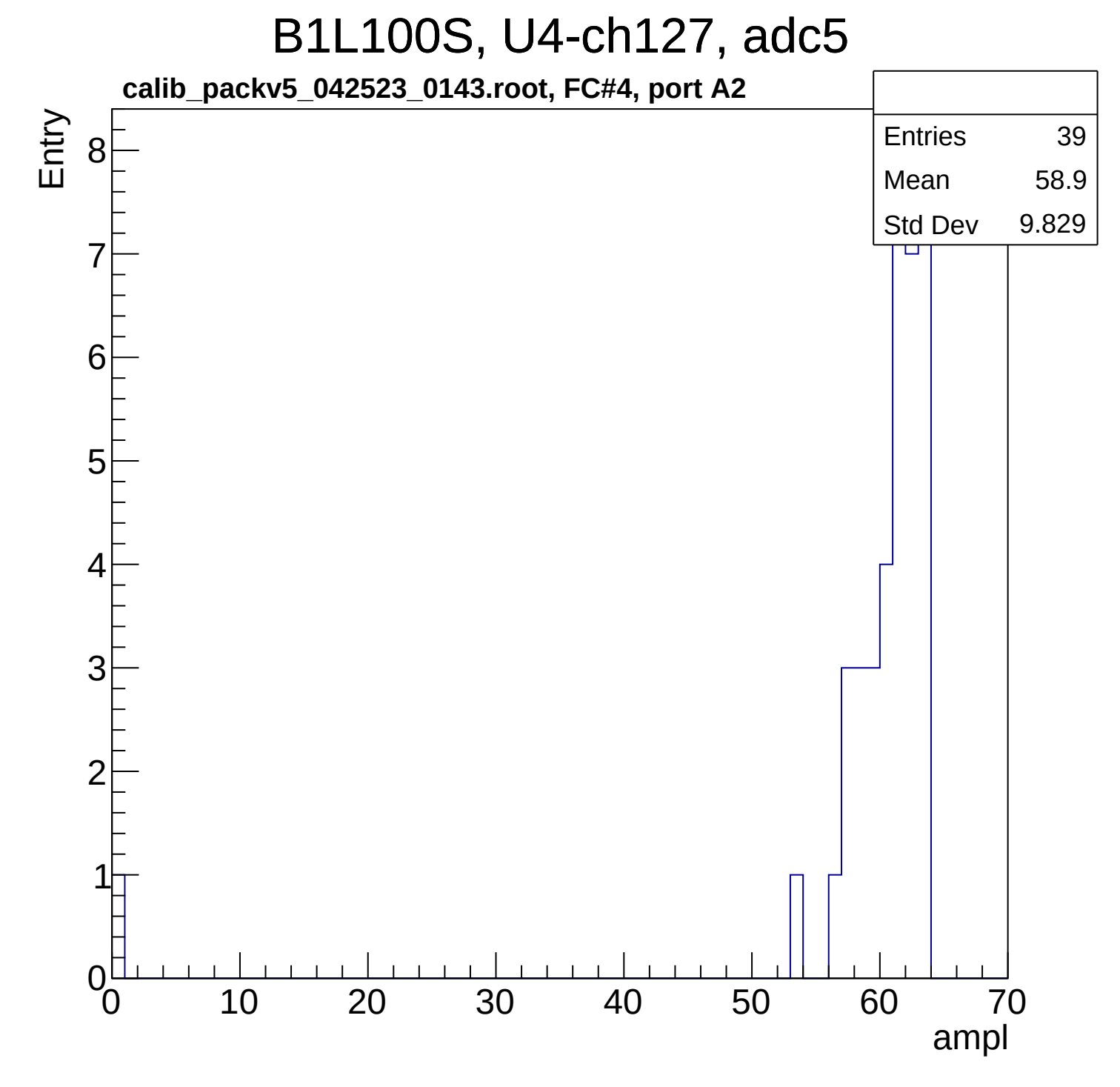

B1L100S, U4-ch127, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 30.37
Std Dev 3.298
Gaus mean : 30.9336
Gaus Width: 3.2442
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

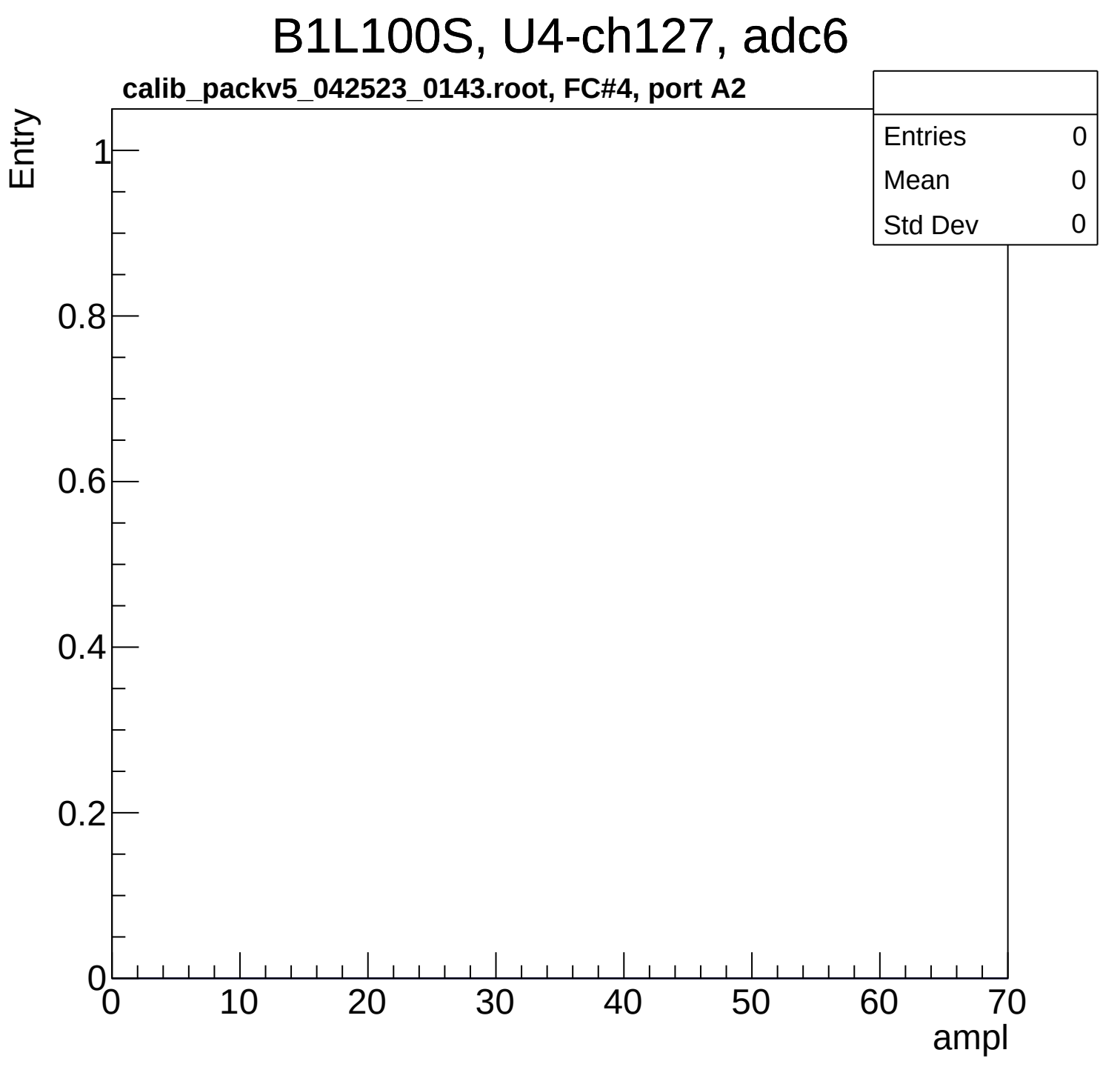

B1L100S, U4-ch127, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 36.13
Std Dev 4.191
Gaus mean : 35.9729
Gaus Width: 3.5819
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

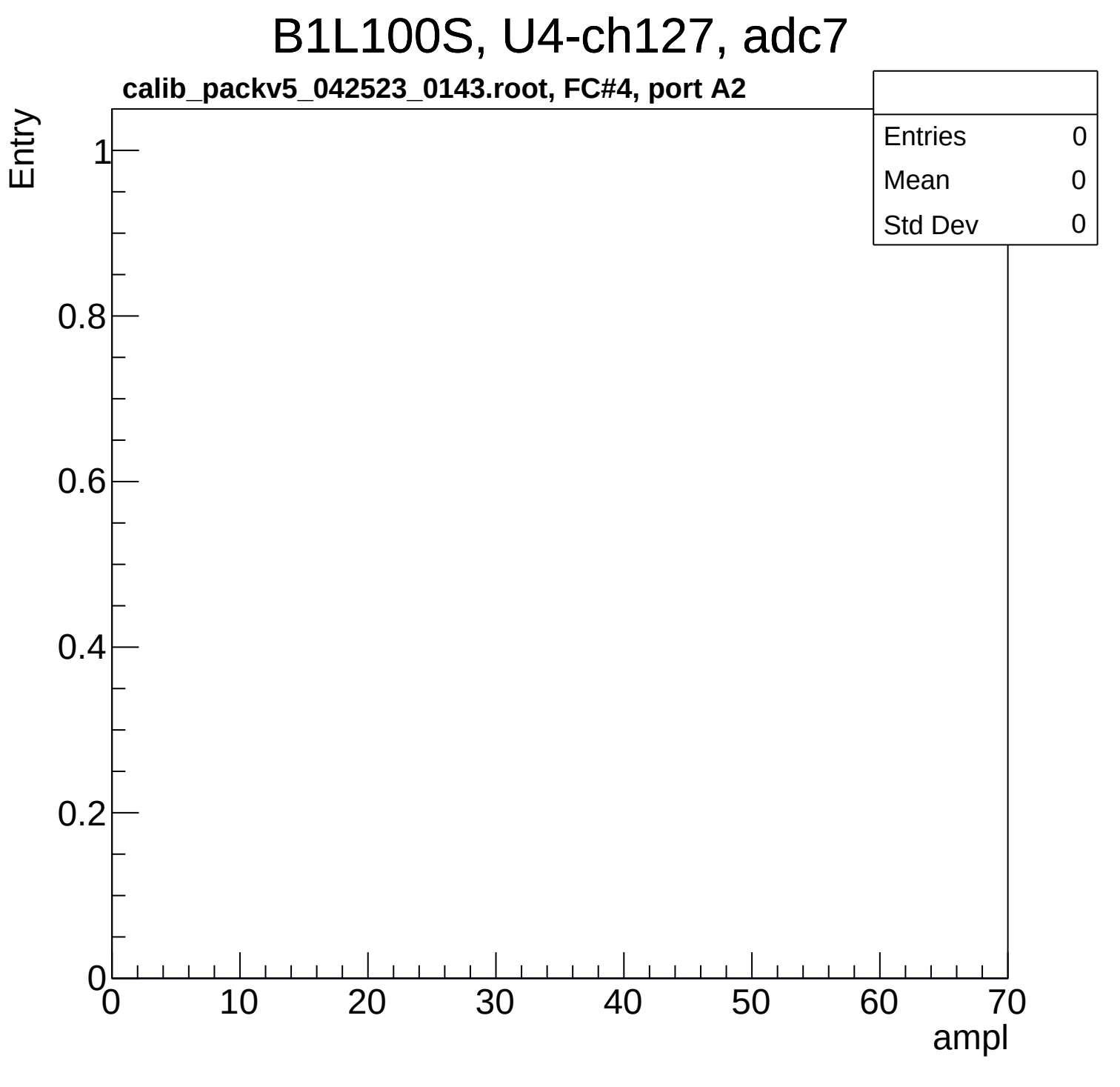

B1L100S, U4-ch127, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 93
Mean 43.8
Std Dev 3.956
Gaus mean : 43.8988
Gaus Width: 4.1091
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

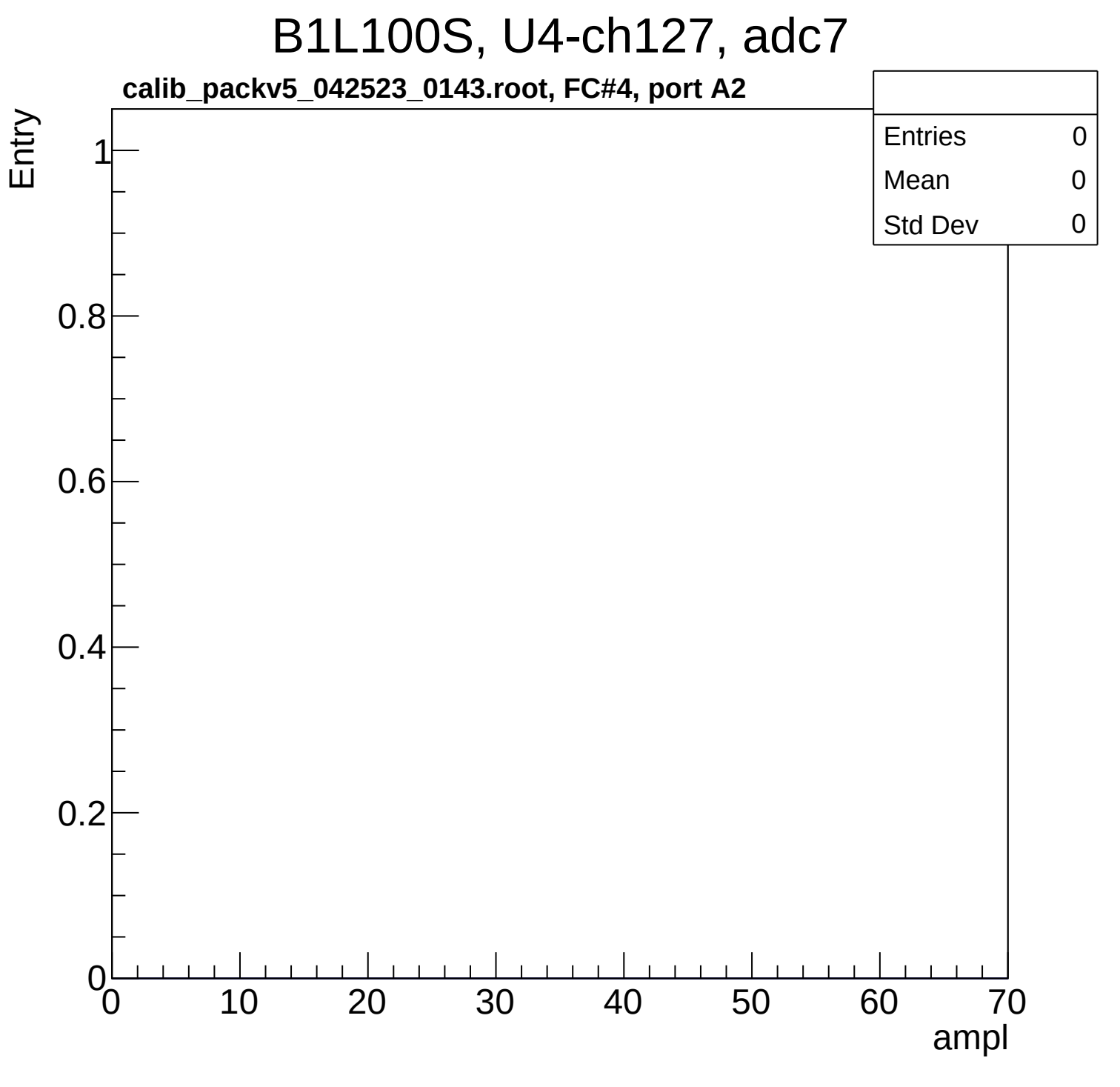

B1L100S, U4-ch127, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 51.65
Std Dev 3.458
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70


B1L100S, U4-ch127, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 57.34
Std Dev 3.11
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70


B1L100S, U4-ch127, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 39
Mean 58.9
Std Dev 9.829
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U4-ch127, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U4-ch127, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U4-ch127, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl