



# B1L102S, U8-ch0, adc0

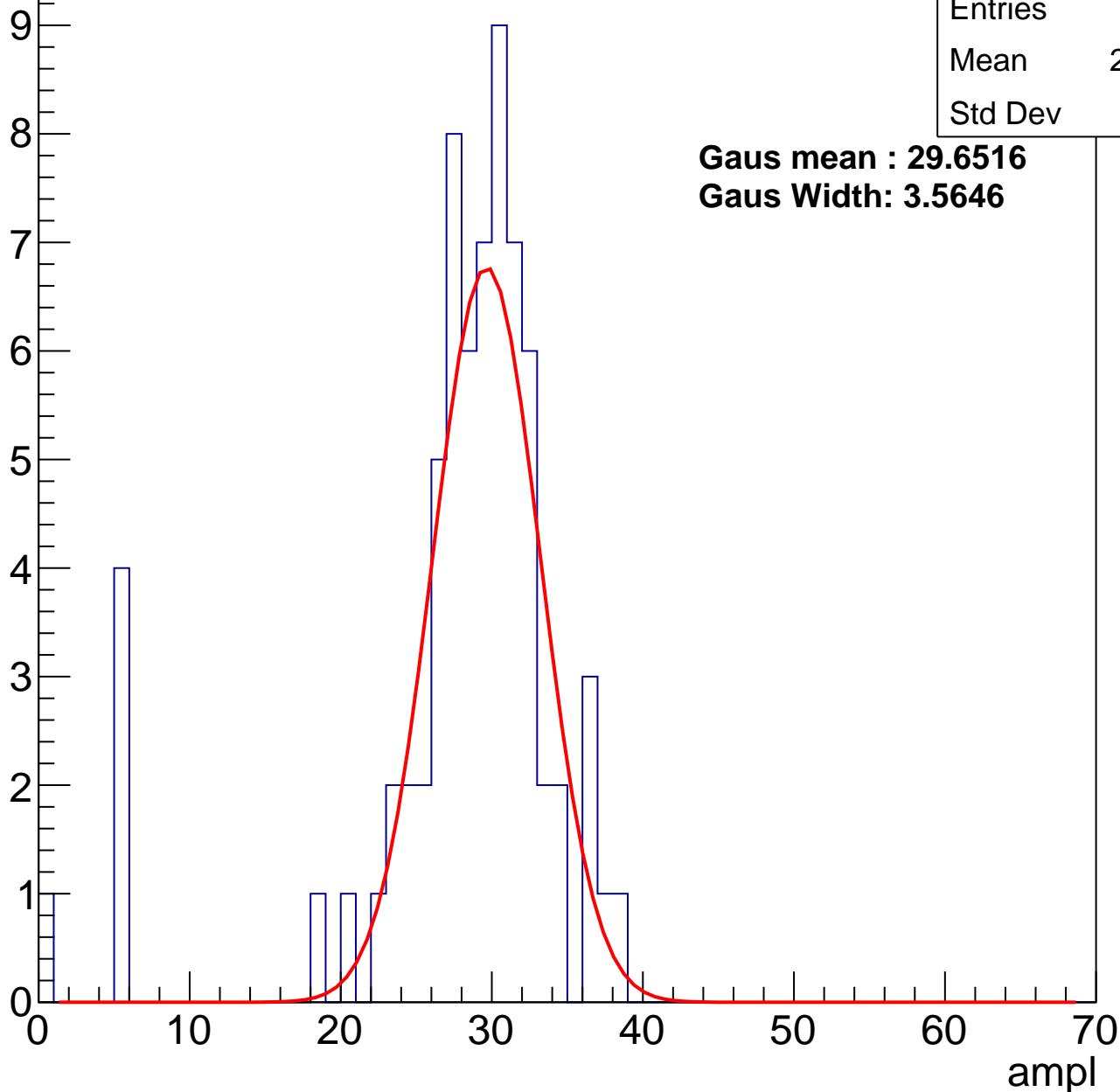
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	27.28
Std Dev	7.4

**Gaus mean : 29.6516**

**Gaus Width: 3.5646**



# B1L102S, U8-ch0, adc1

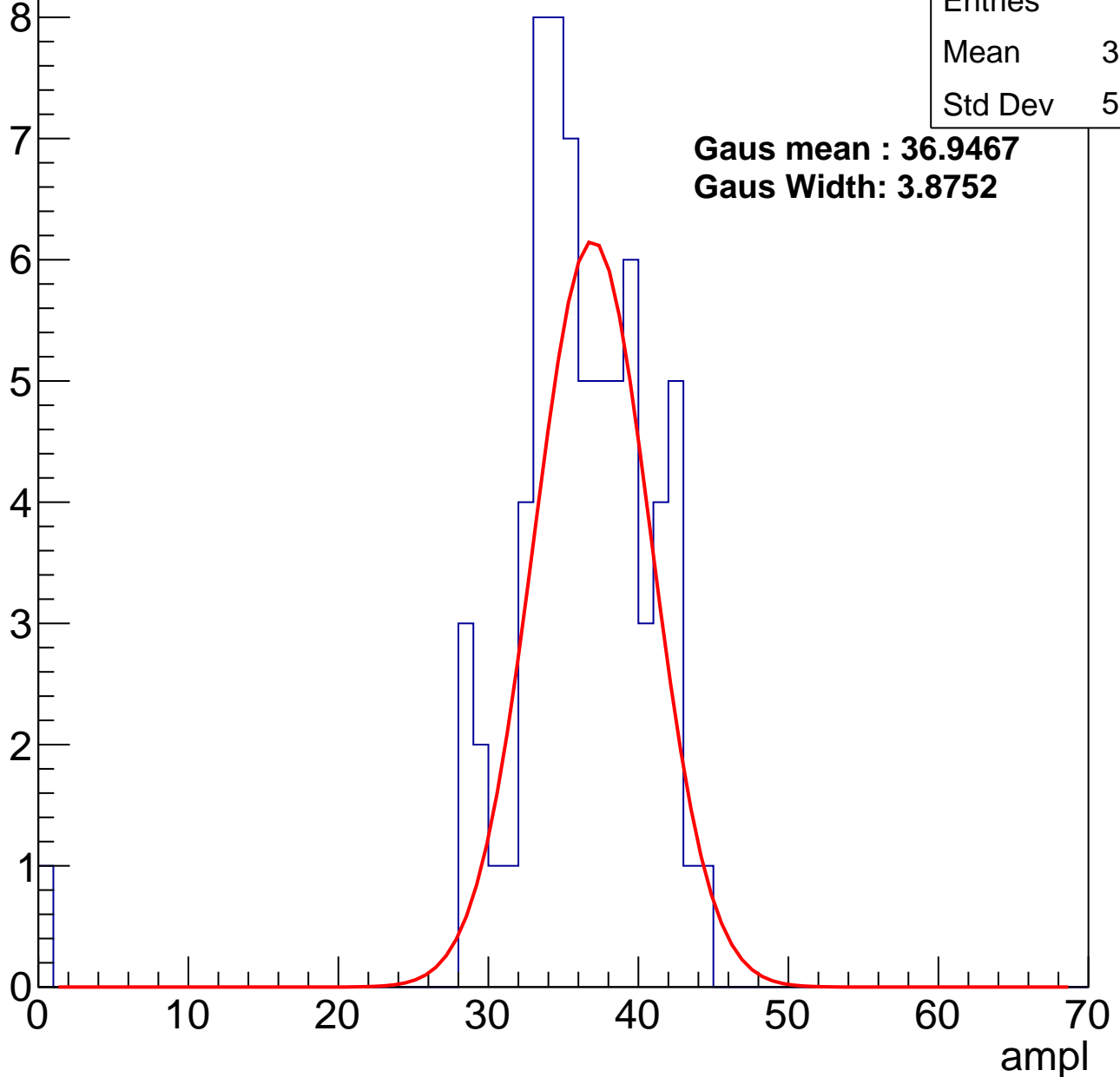
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	35.46
Std Dev	5.759

**Gaus mean : 36.9467**

**Gaus Width: 3.8752**



# B1L102S, U8-ch0, adc2

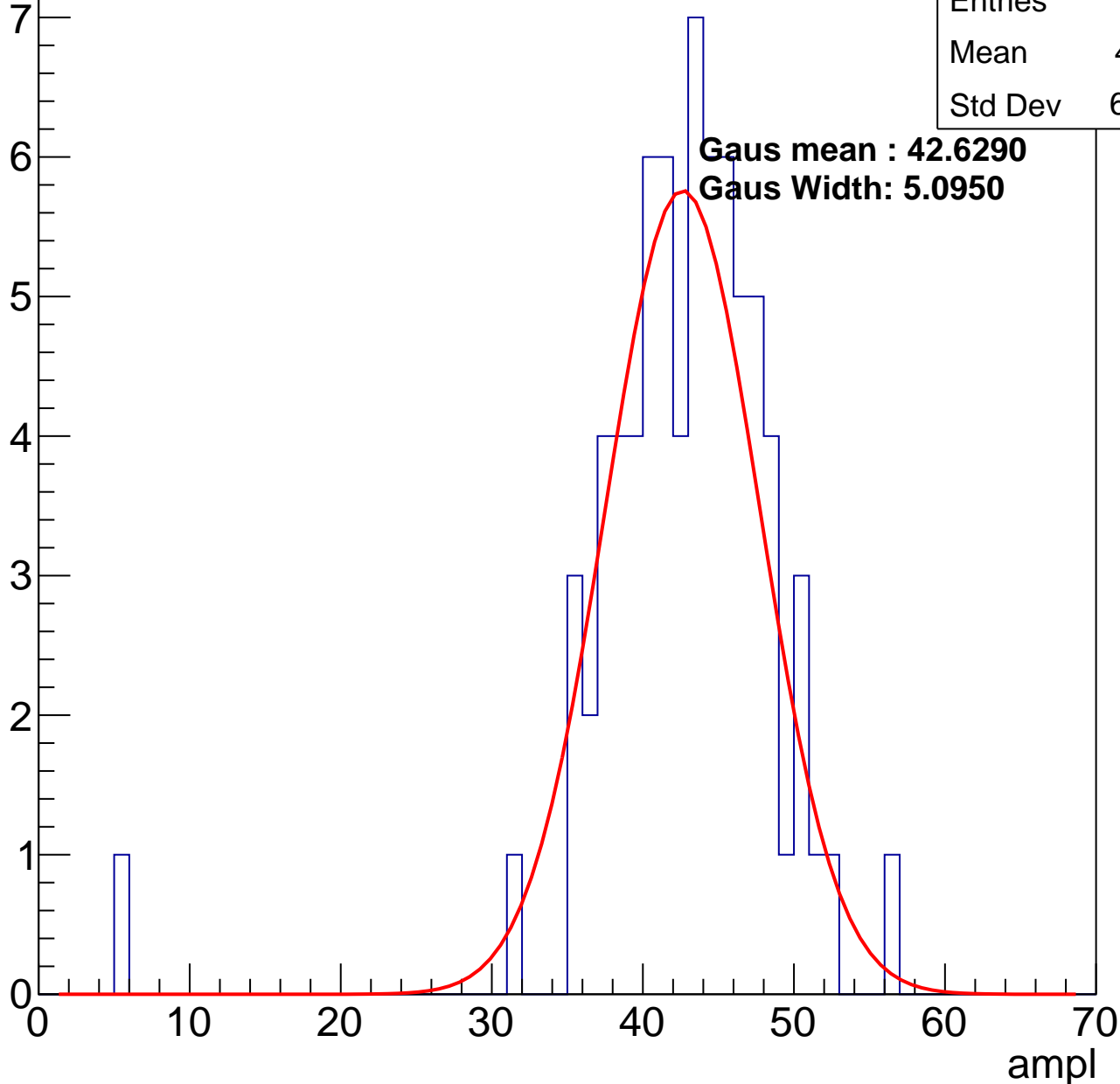
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	42.31
Std Dev	6.308

**Gaus mean : 42.6290**

**Gaus Width: 5.0950**

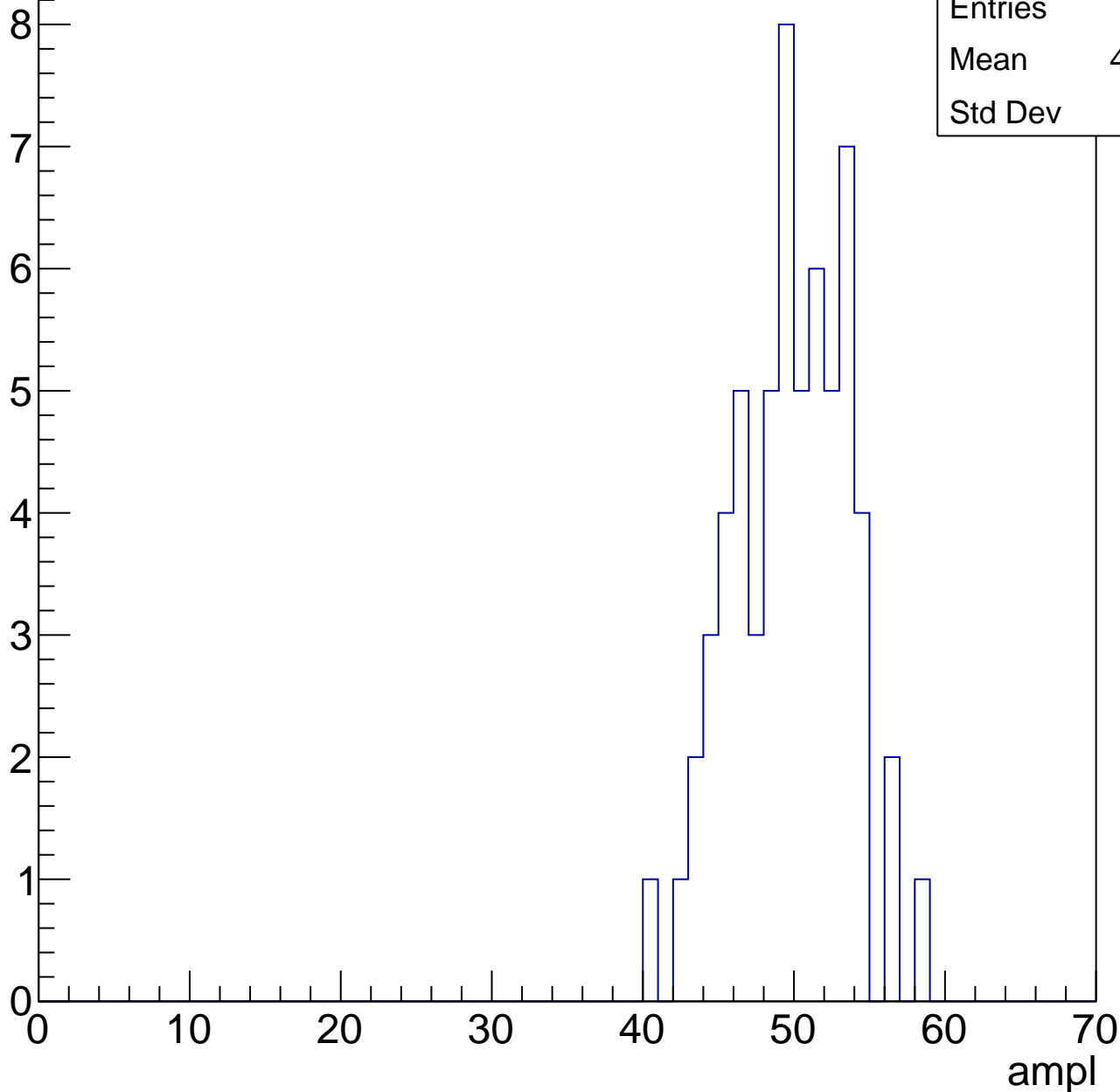


# B1L102S, U8-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

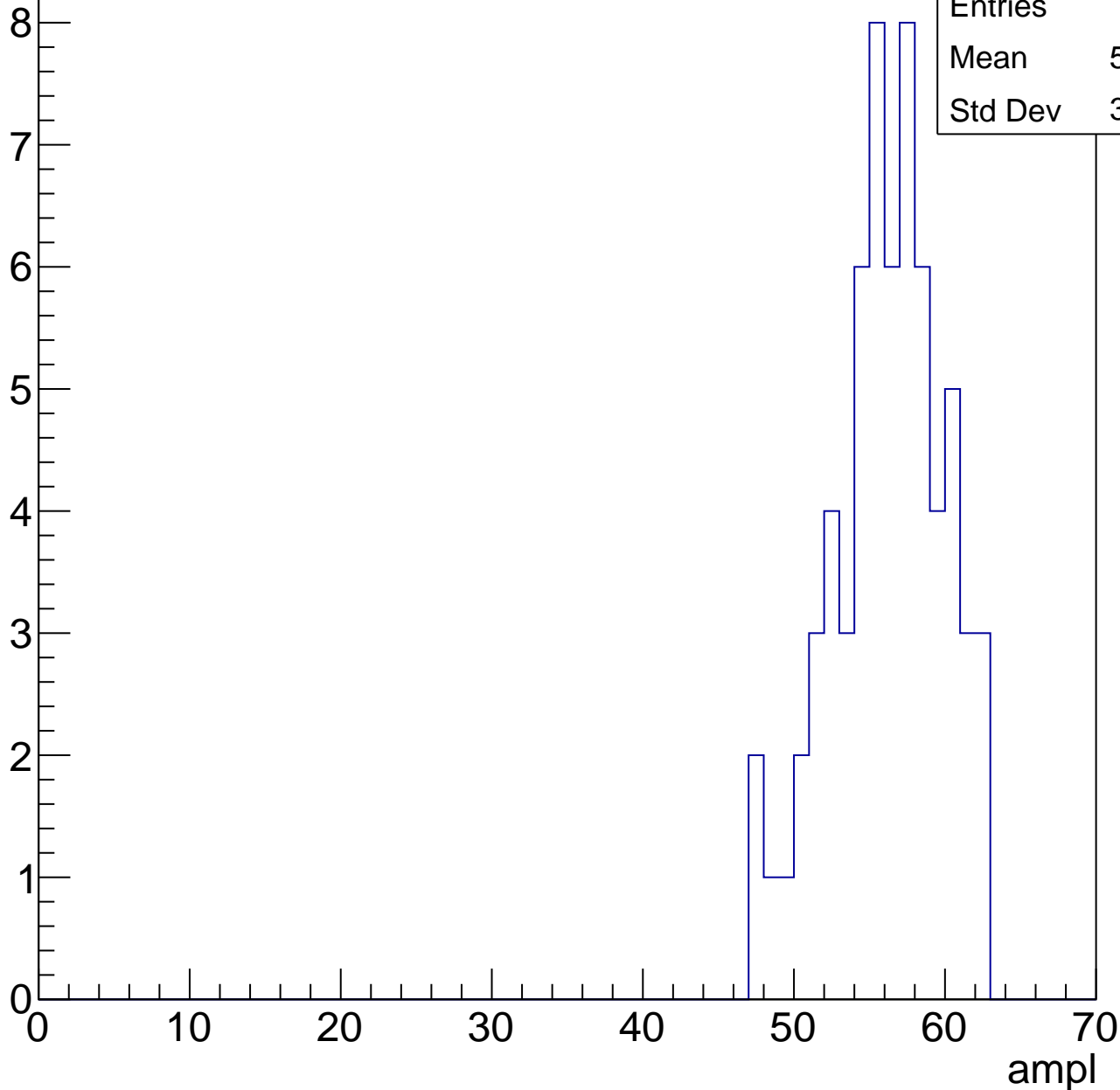
Entries	62
Mean	49.29
Std Dev	3.73



# B1L102S, U8-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

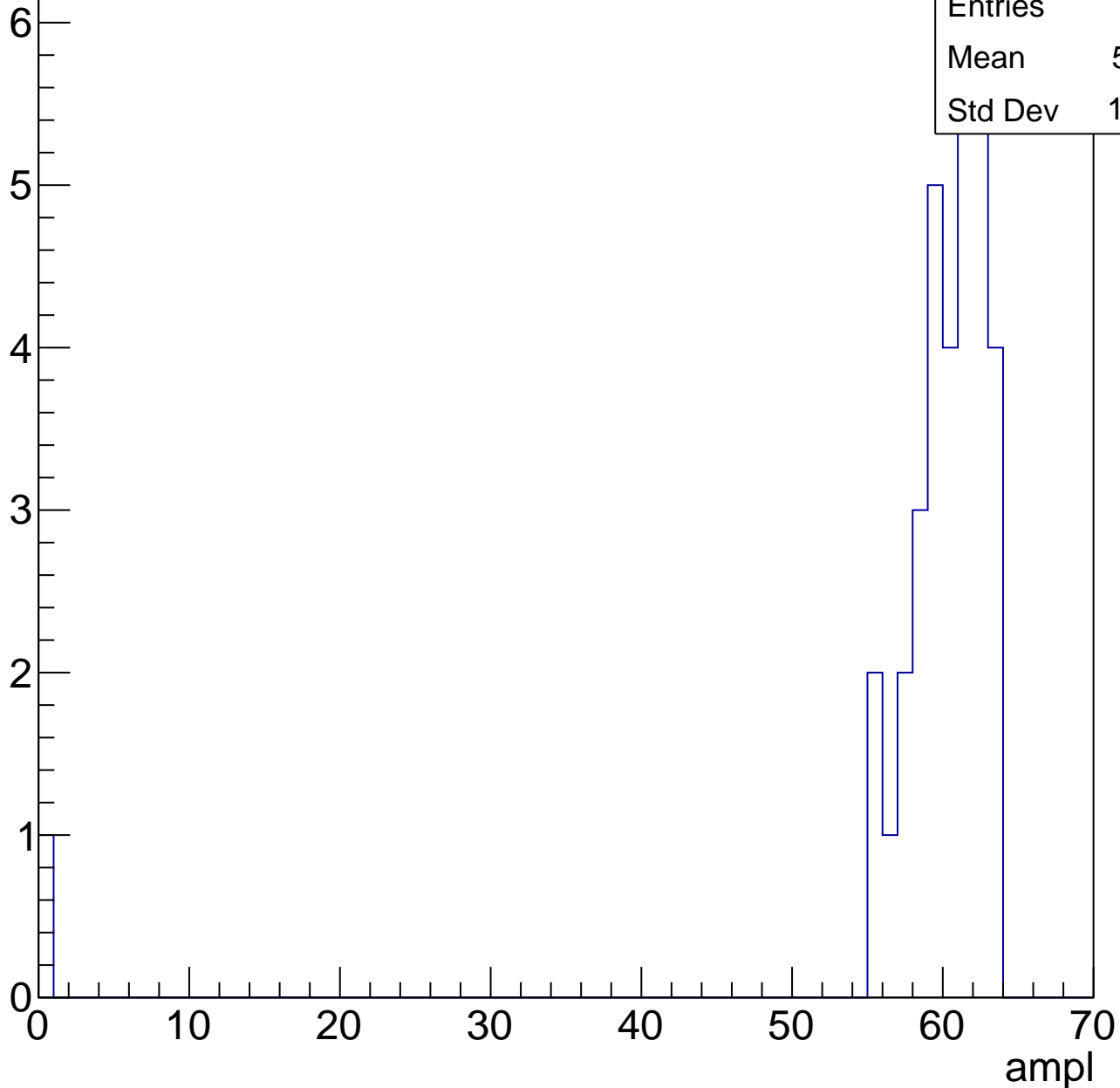
Entry



# B1L102S, U8-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

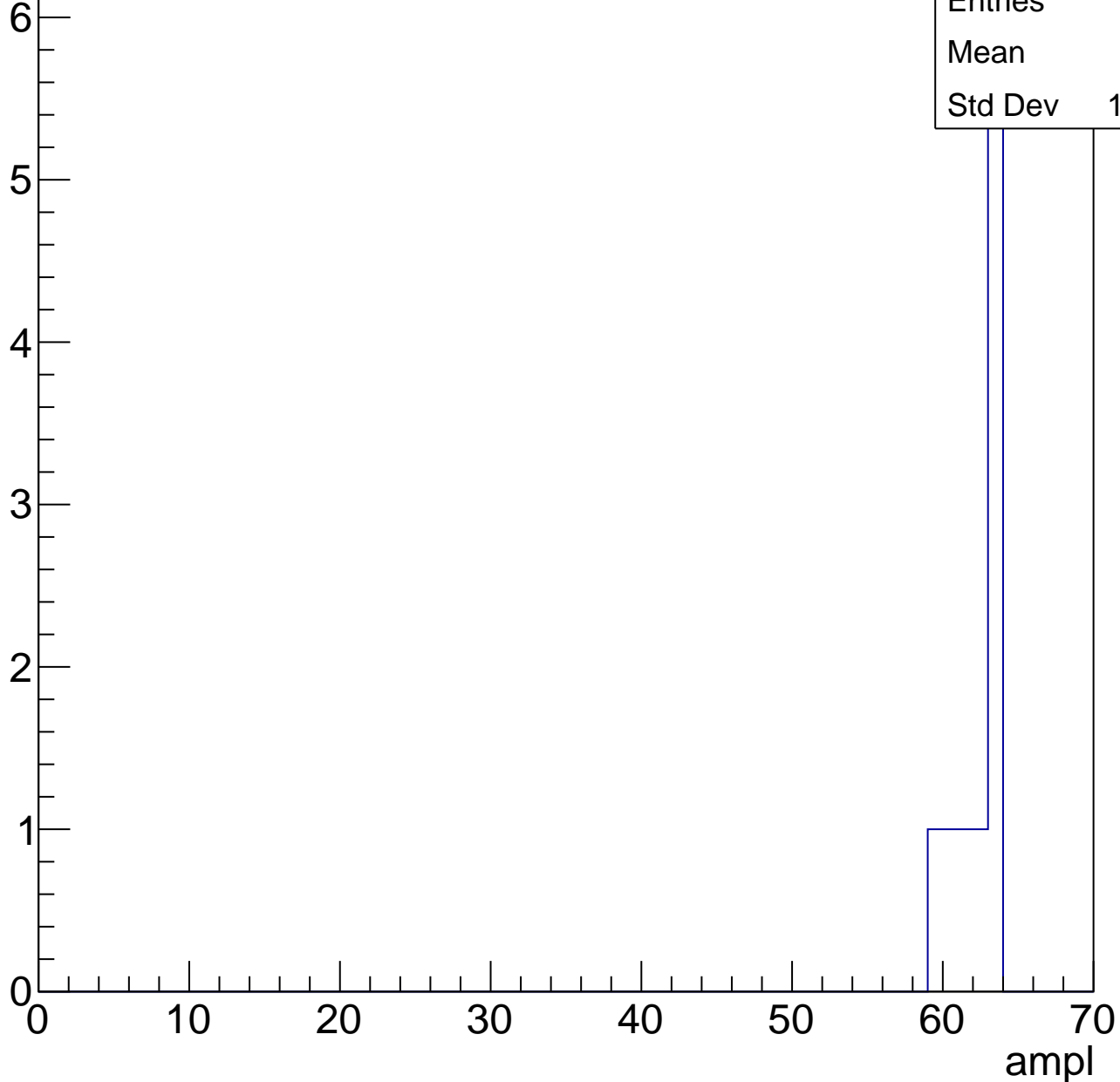
Entry



# B1L102S, U8-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

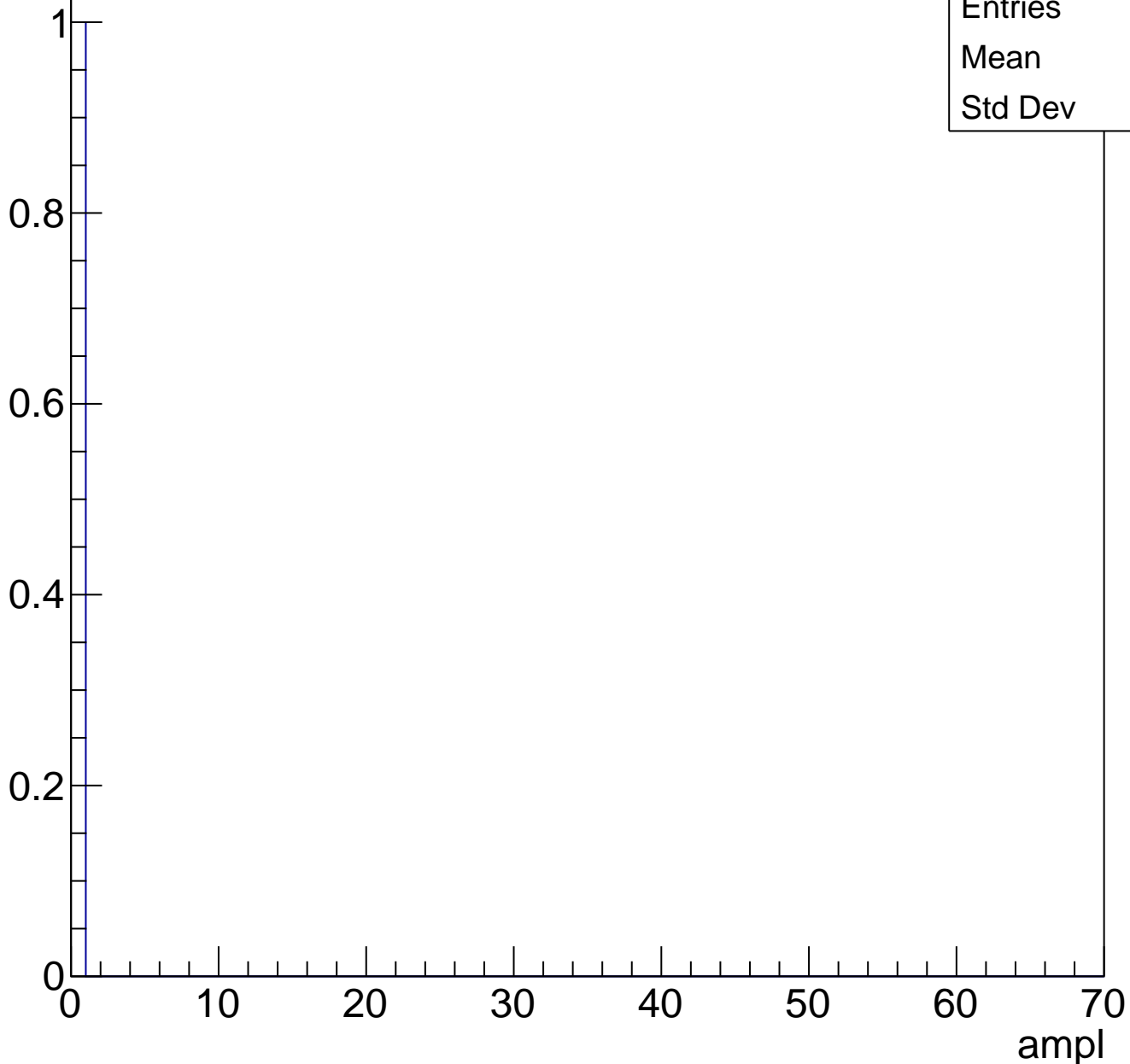




# B1L102S, U8-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch1, adc0

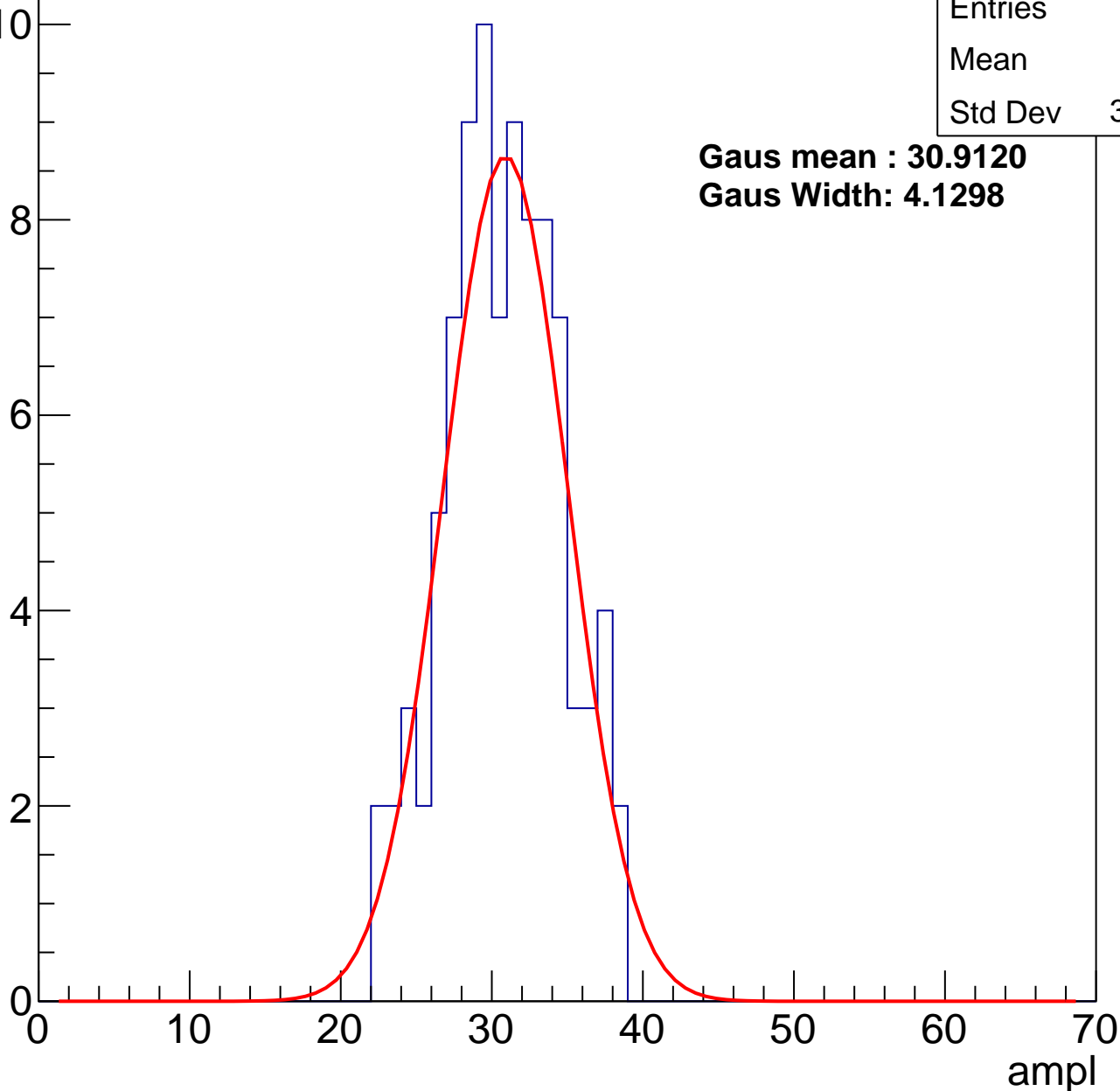
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	91
Mean	30.3
Std Dev	3.775

**Gaus mean : 30.9120**

**Gaus Width: 4.1298**



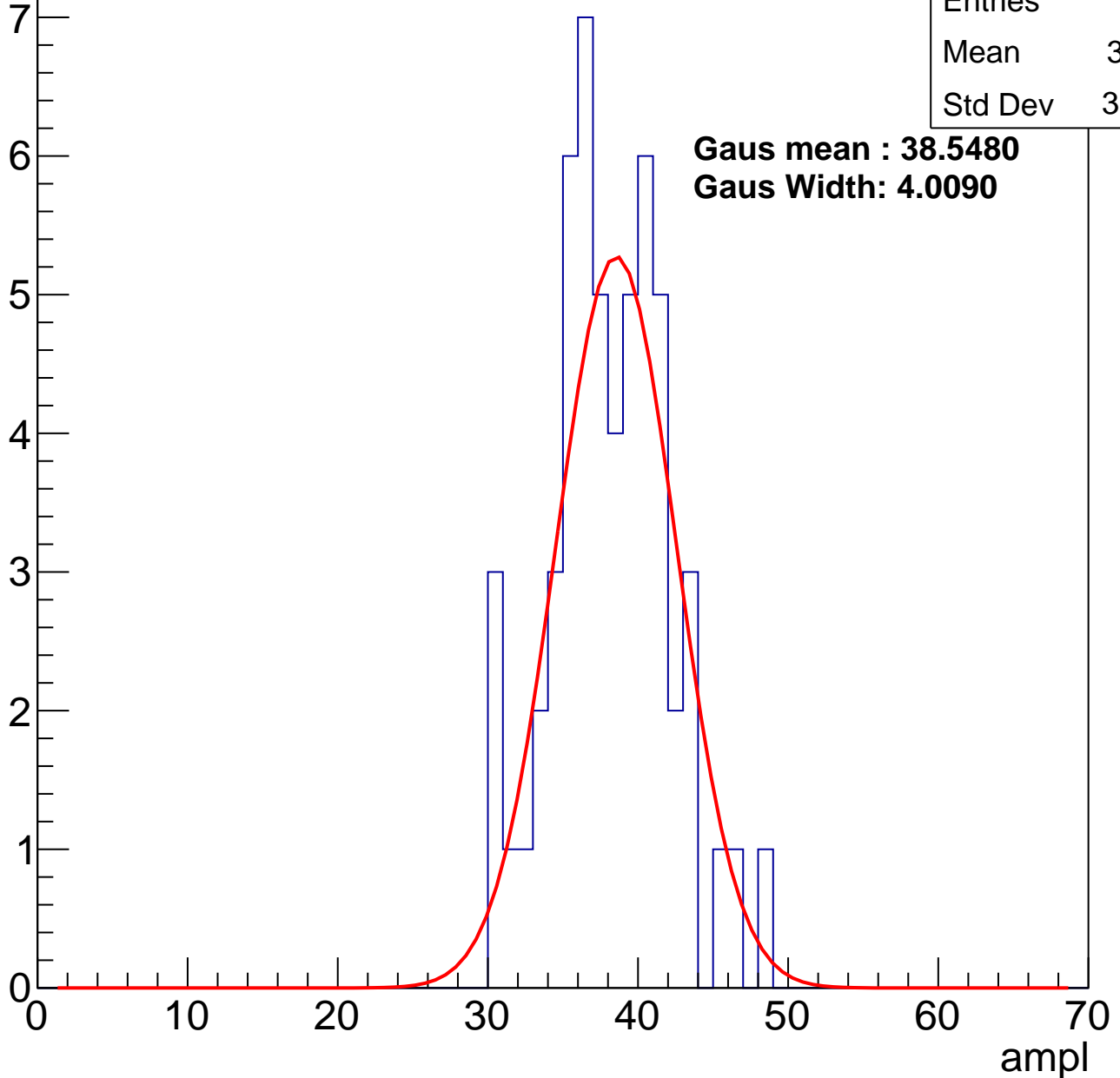
# B1L102S, U8-ch1, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	37.71
Std Dev	3.899

**Gaus mean : 38.5480**  
**Gaus Width: 4.0090**



# B1L102S, U8-ch1, adc2

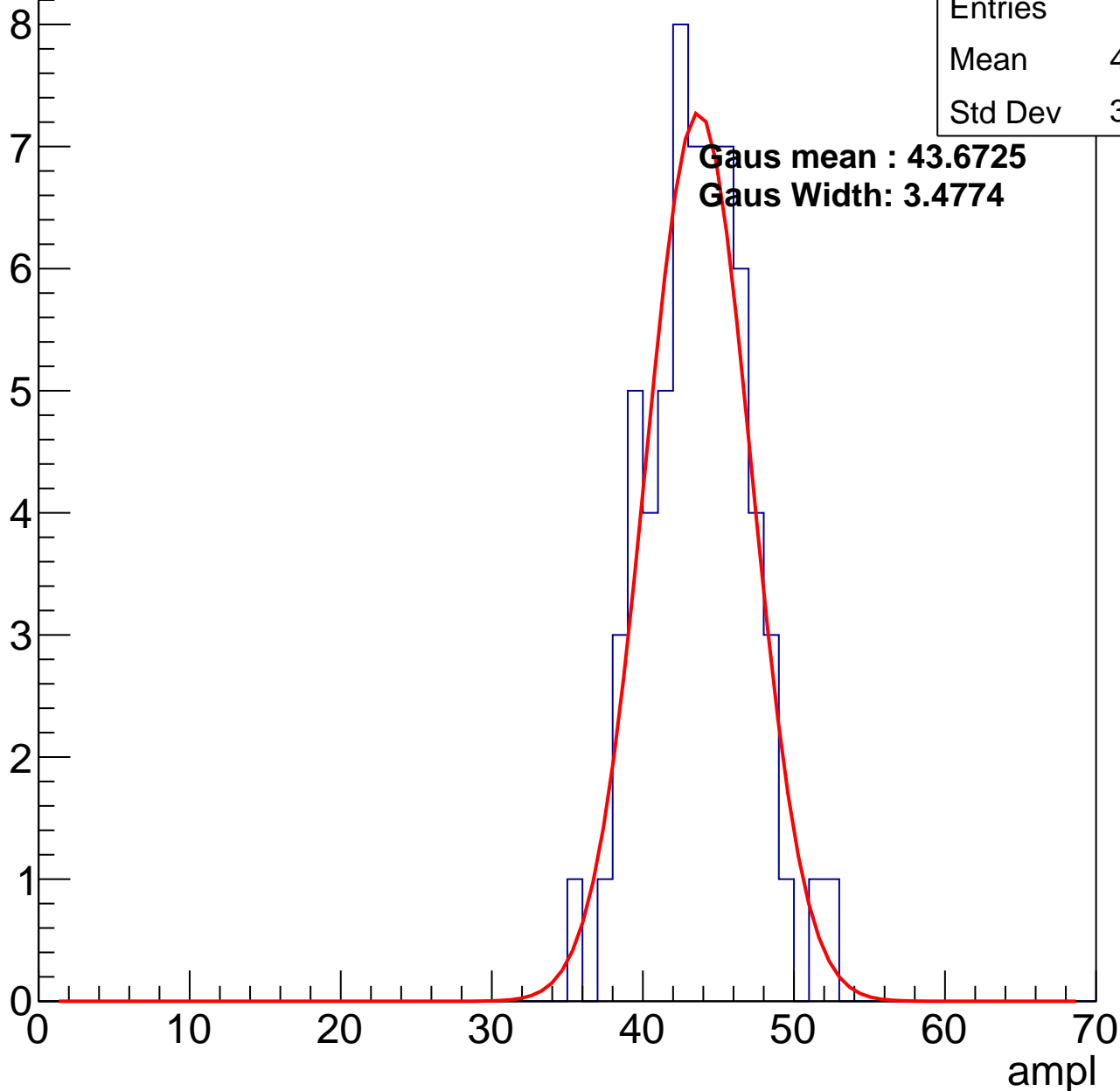
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	43.22
Std Dev	3.366

**Gaus mean : 43.6725**

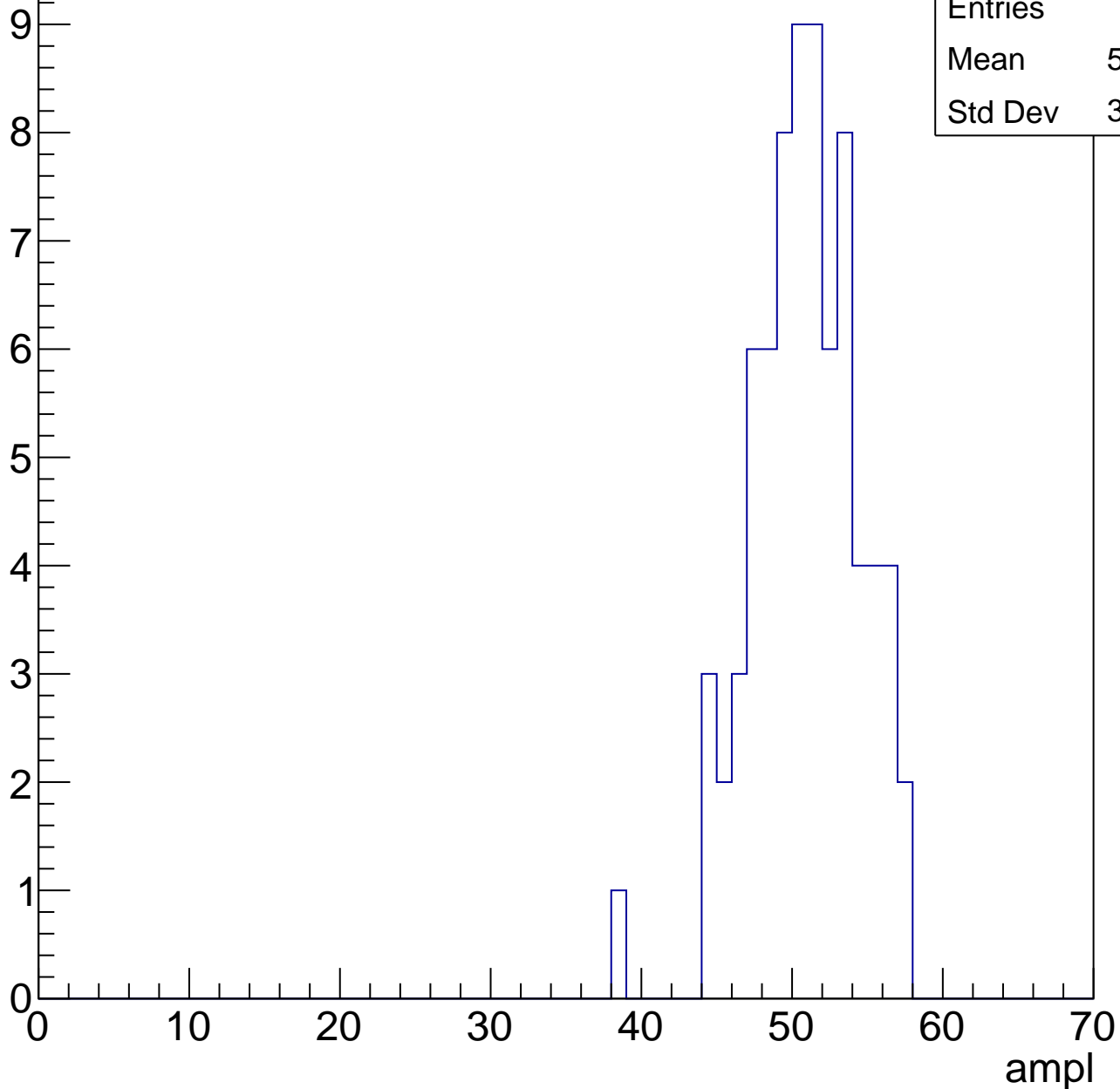
**Gaus Width: 3.4774**



# B1L102S, U8-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



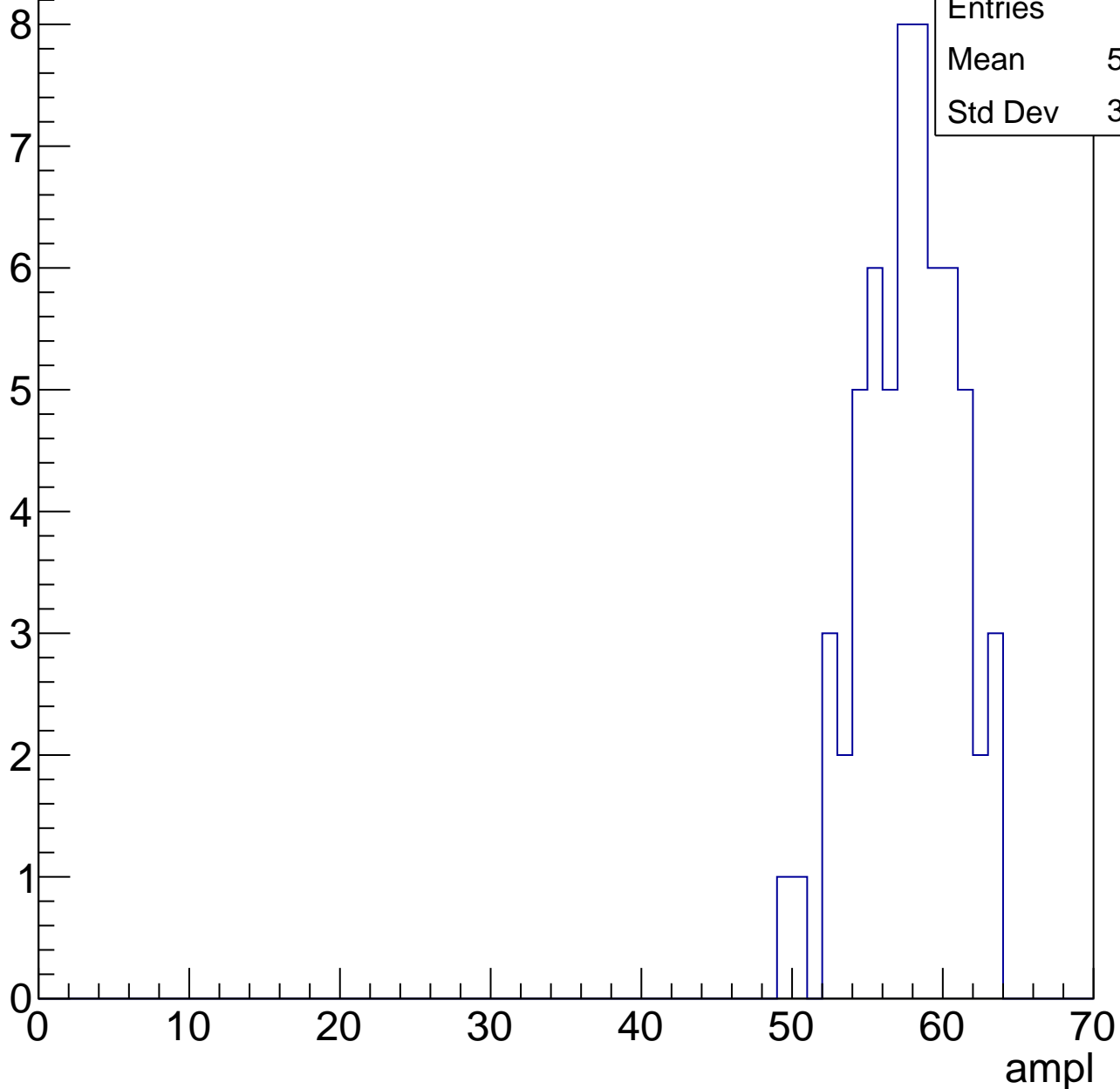
Entries	75
Mean	50.39
Std Dev	3.532

# B1L102S, U8-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	57.26
Std Dev	3.172

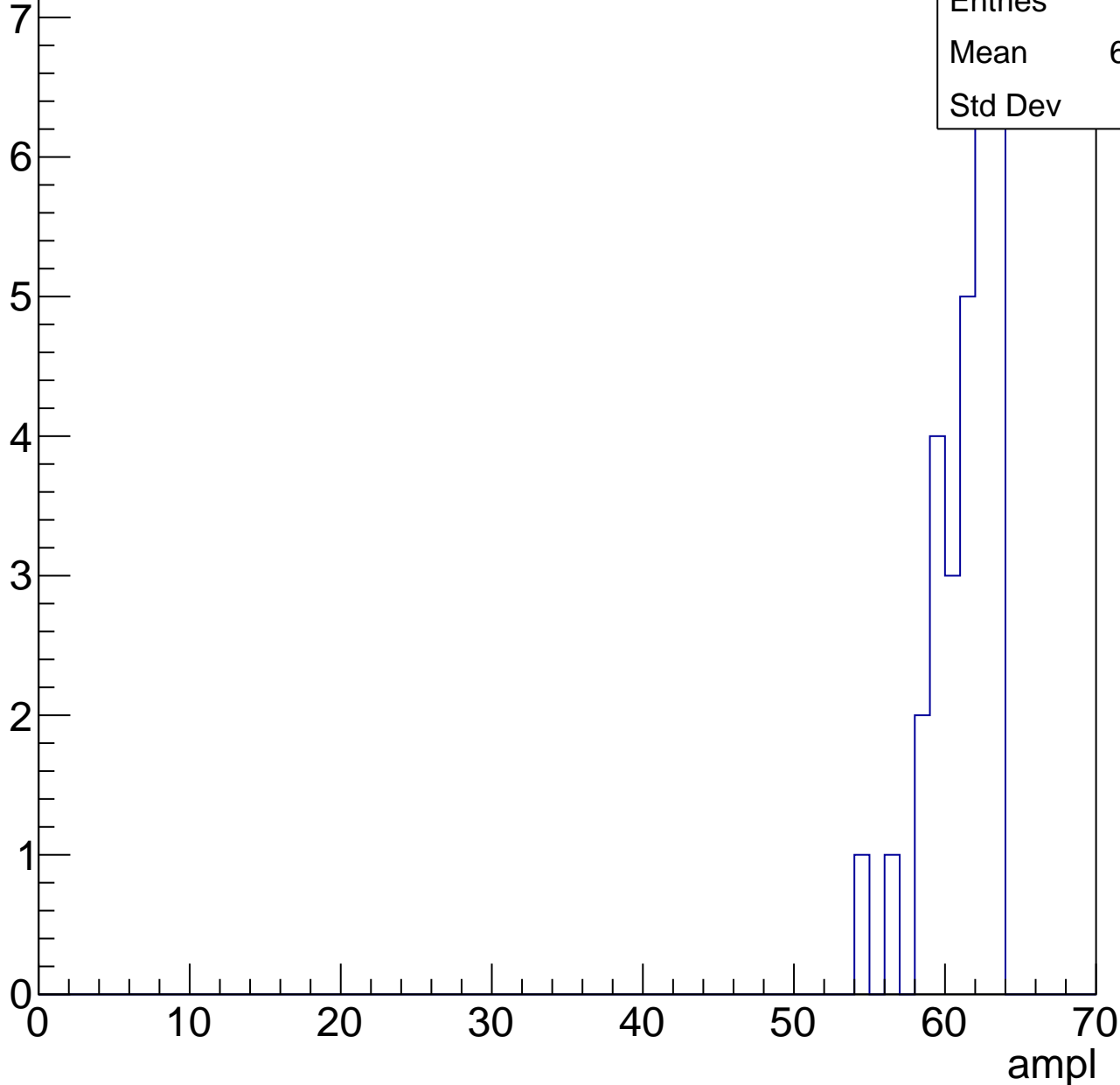


# B1L102S, U8-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

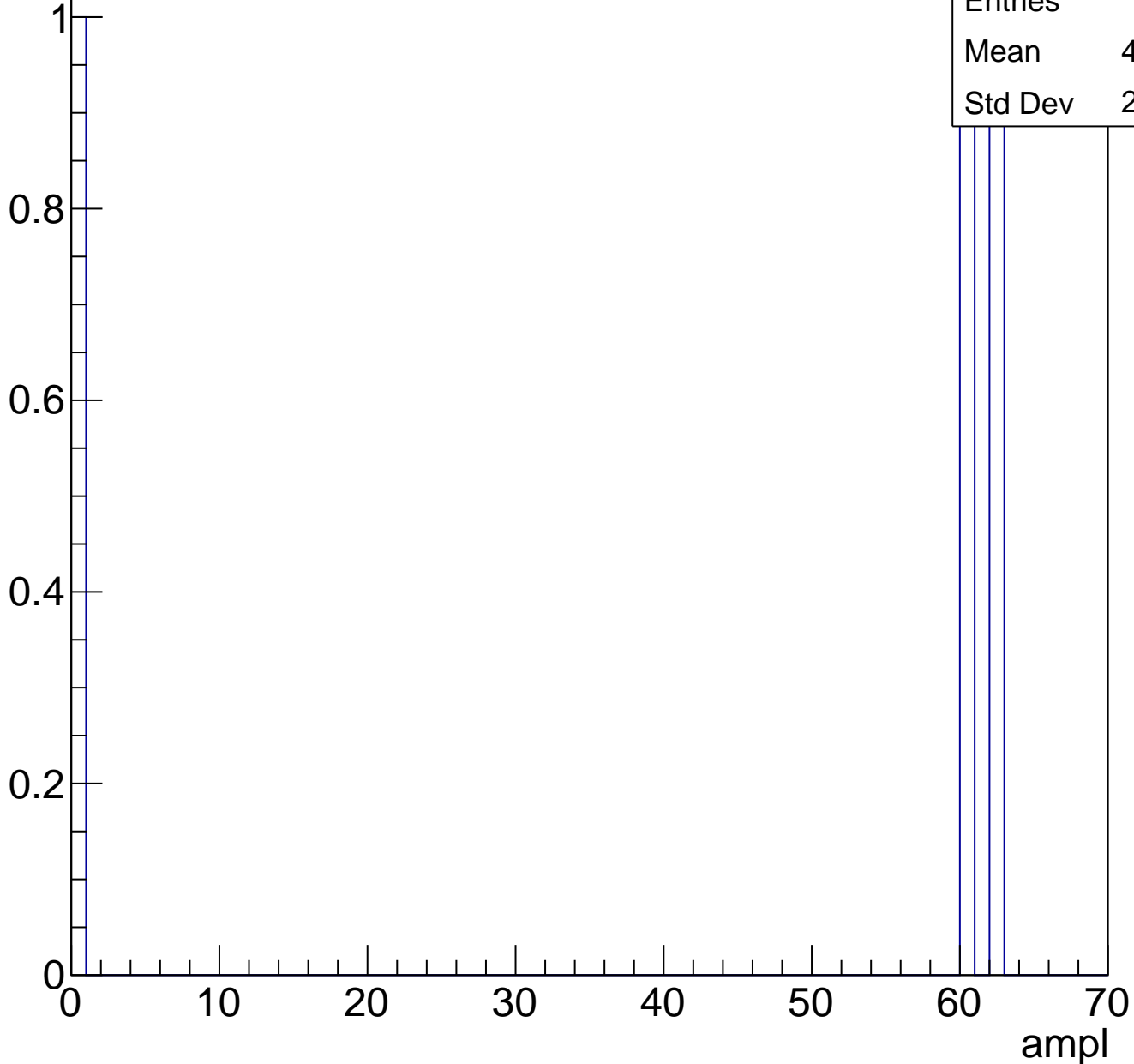
Entries	30
Mean	60.73
Std Dev	2.19



# B1L102S, U8-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch2, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	89
Mean	30.15
Std Dev	3.779

**Gaus mean : 30.3896**

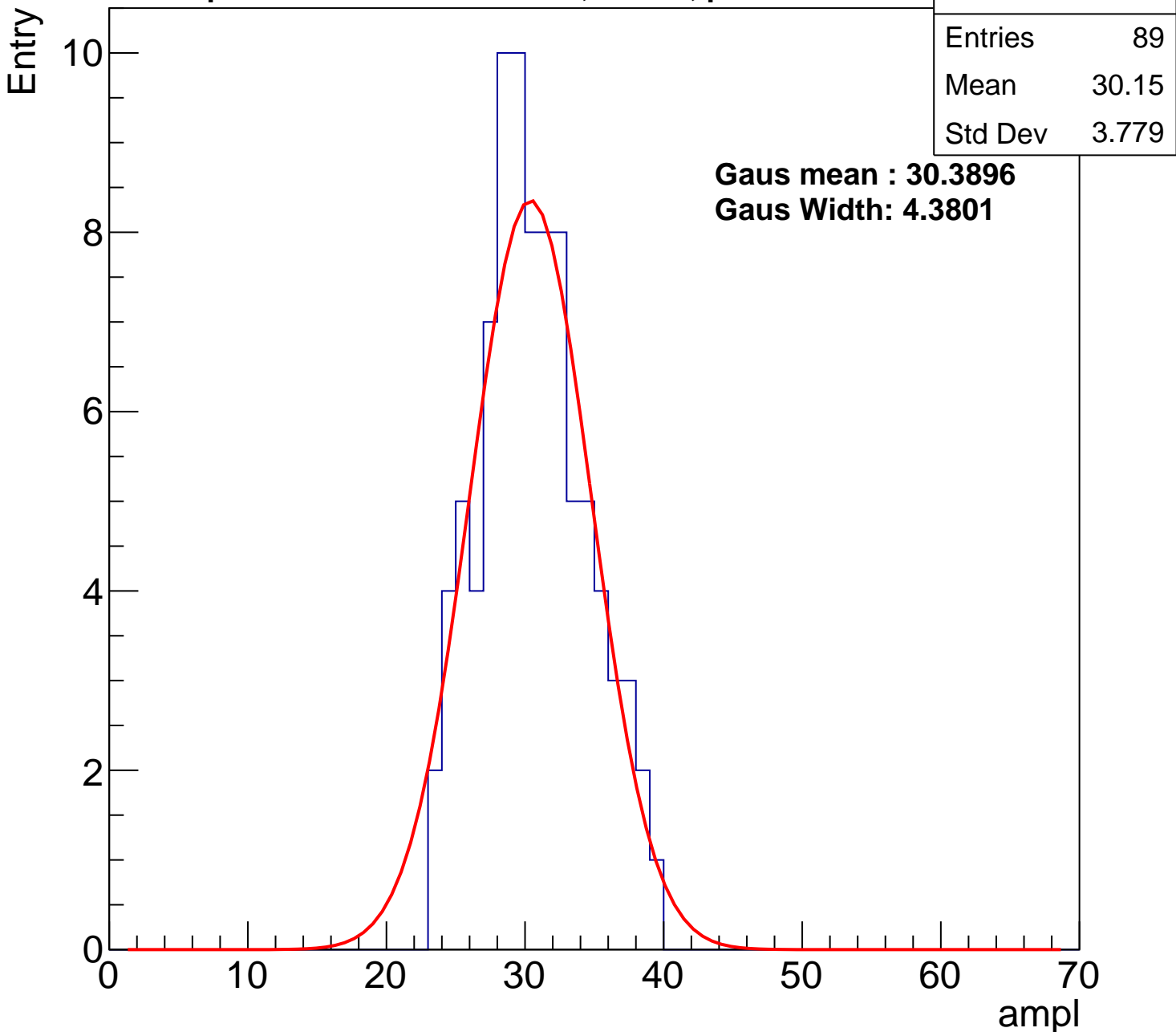
**Gaus Width: 4.3801**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



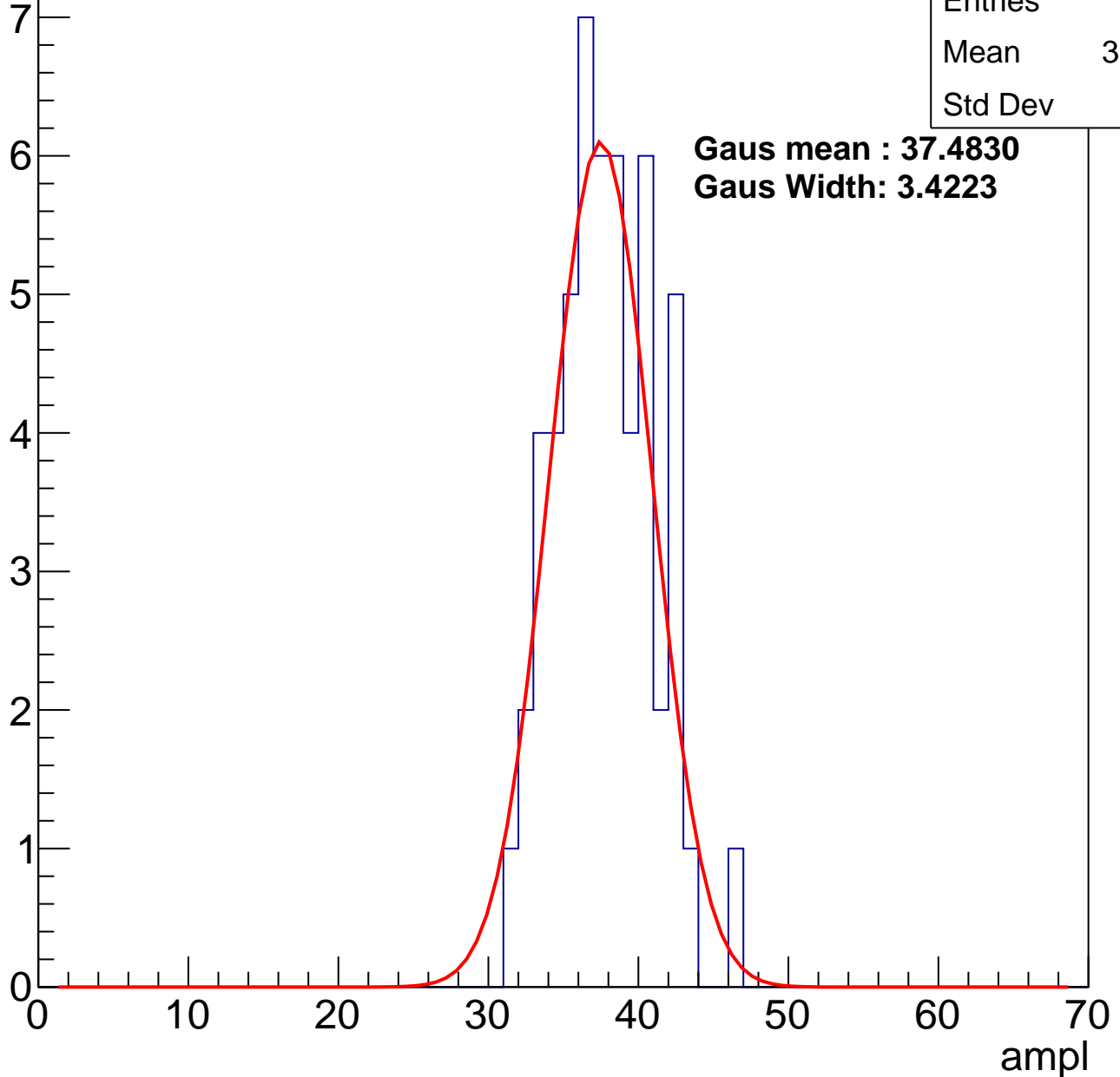
# B1L102S, U8-ch2, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	37.35
Std Dev	3.21

**Gaus mean : 37.4830**  
**Gaus Width: 3.4223**



# B1L102S, U8-ch2, adc2

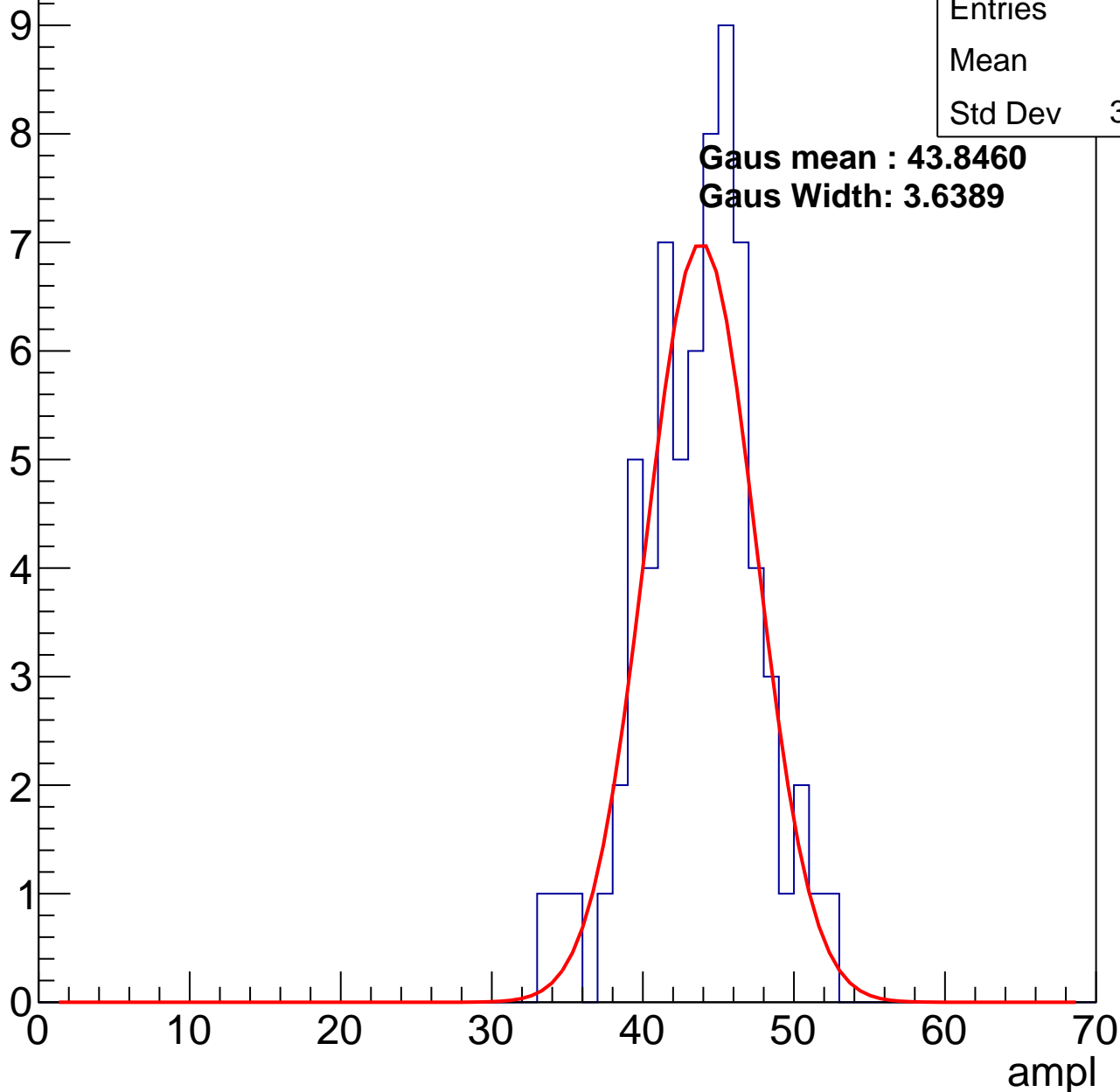
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	43.3
Std Dev	3.804

**Gaus mean : 43.8460**

**Gaus Width: 3.6389**

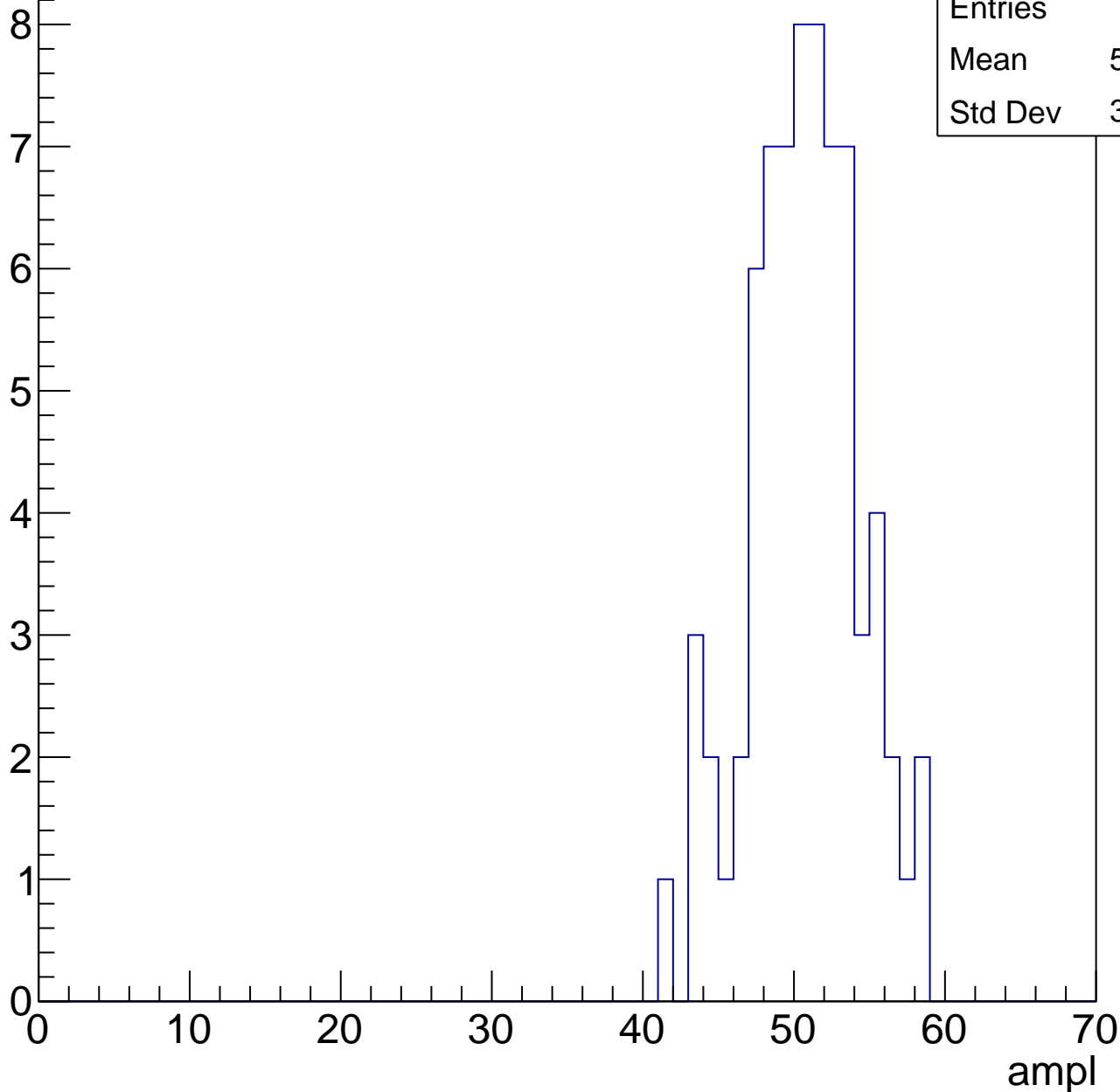


# B1L102S, U8-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	50.23
Std Dev	3.635

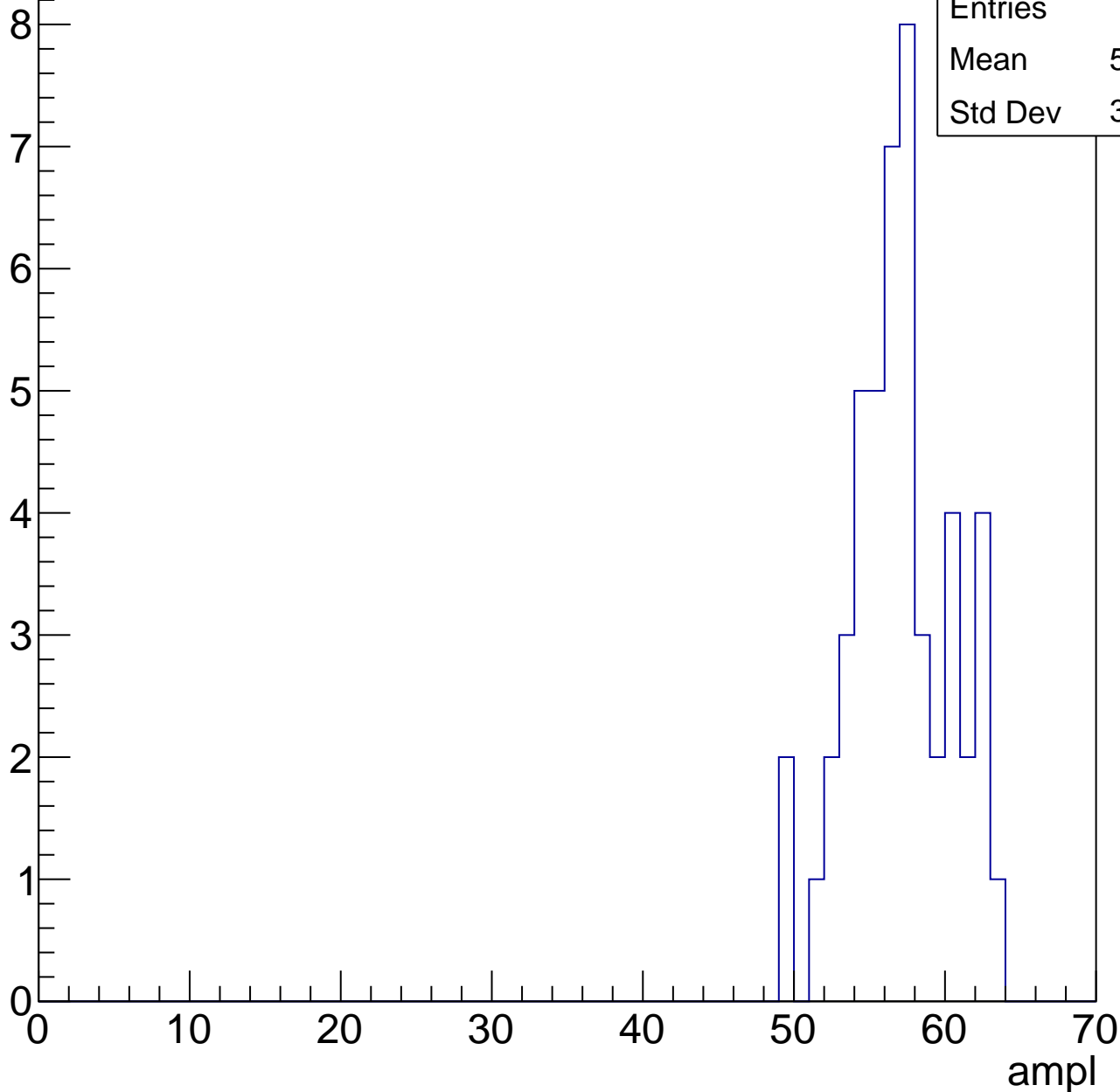


# B1L102S, U8-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	56.53
Std Dev	3.314



# B1L102S, U8-ch2, adc5

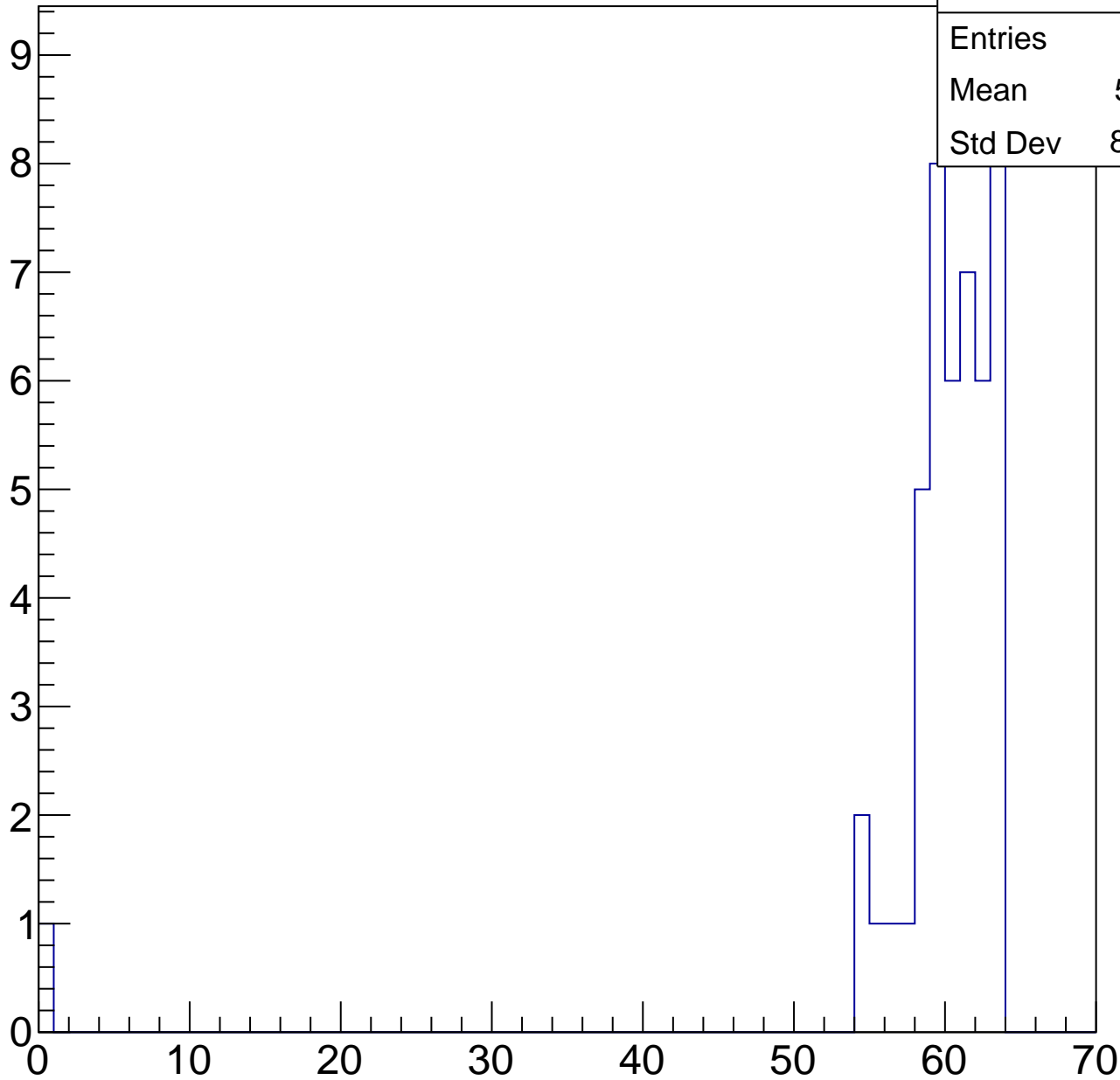
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	47
Mean	58.81
Std Dev	8.986

ampl



# B1L102S, U8-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	21
Std Dev	0

ampl

# B1L102S, U8-ch3, adc0

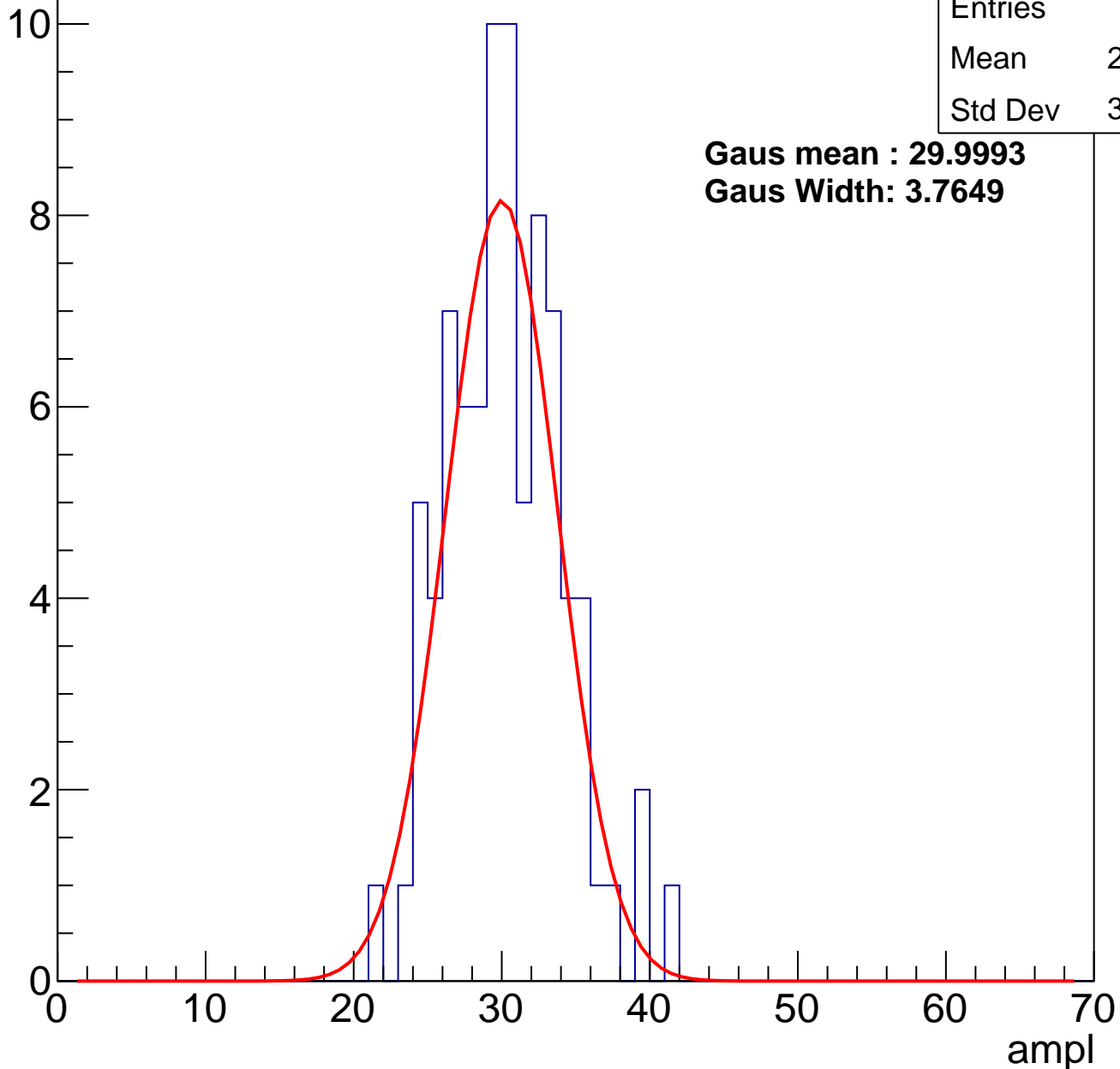
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	83
Mean	29.83
Std Dev	3.865

**Gaus mean : 29.9993**

**Gaus Width: 3.7649**

Entry



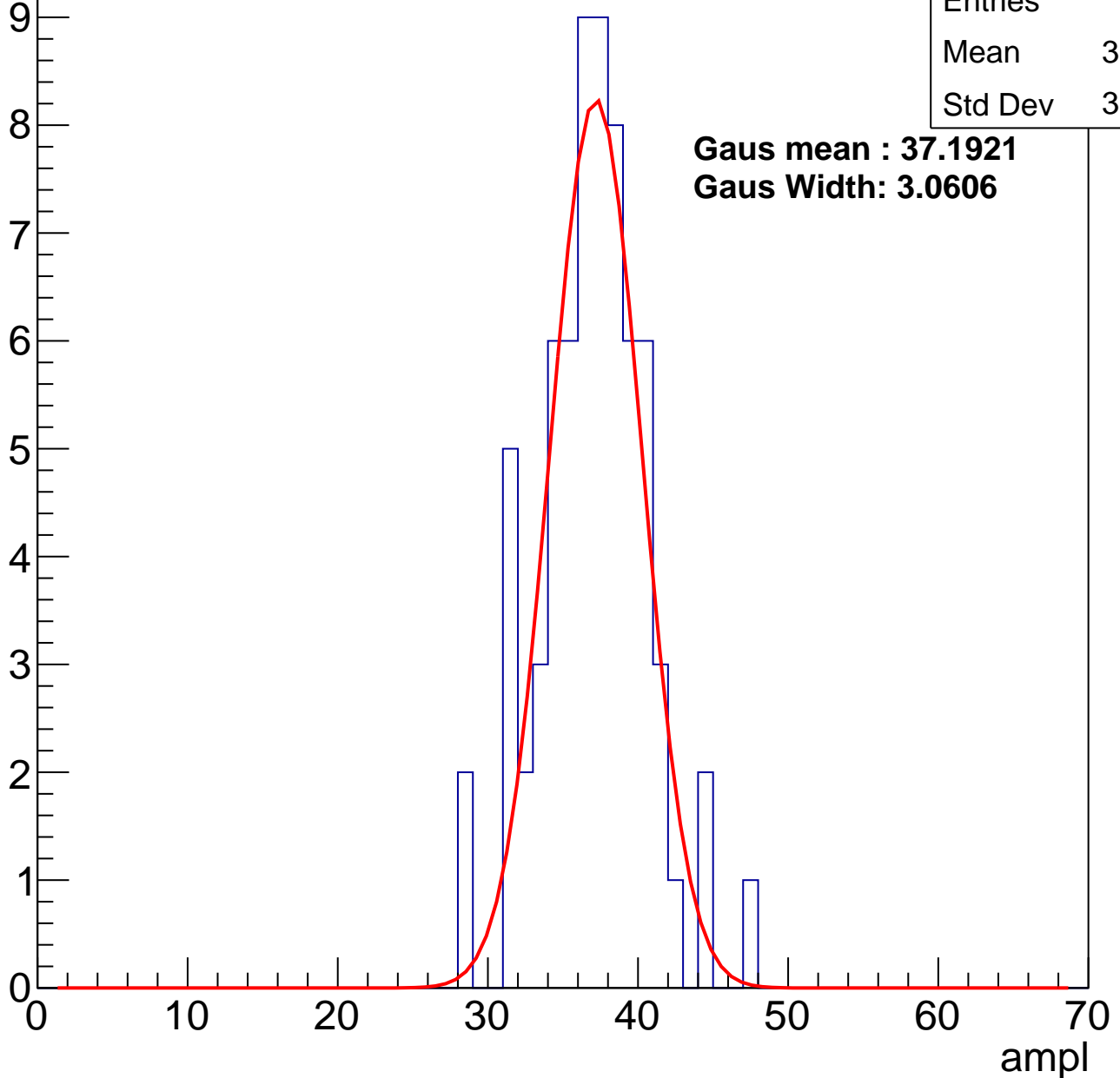
# B1L102S, U8-ch3, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	36.57
Std Dev	3.553

**Gaus mean : 37.1921**  
**Gaus Width: 3.0606**



# B1L102S, U8-ch3, adc2

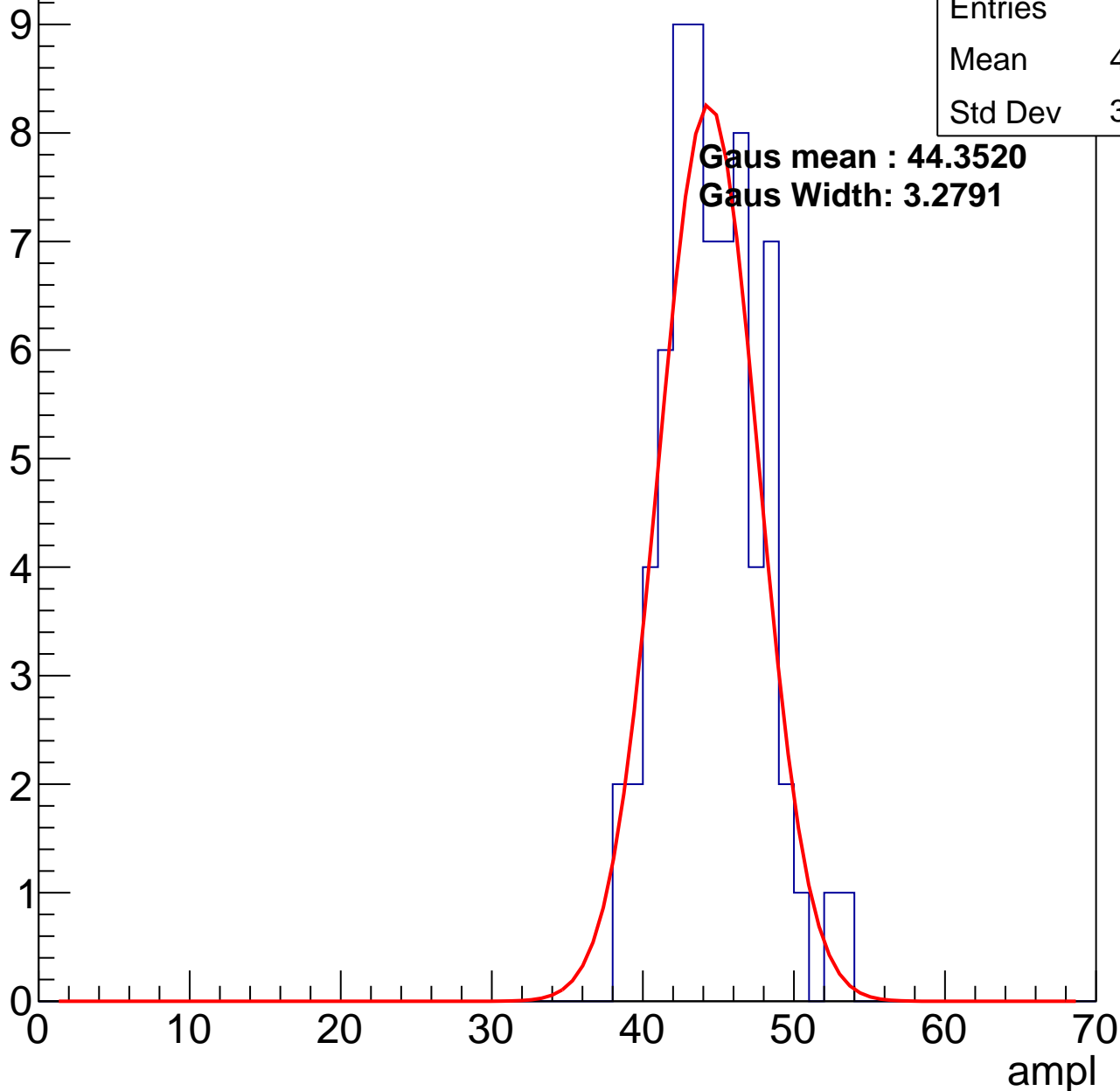
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	44.19
Std Dev	3.164

**Gaus mean : 44.3520**

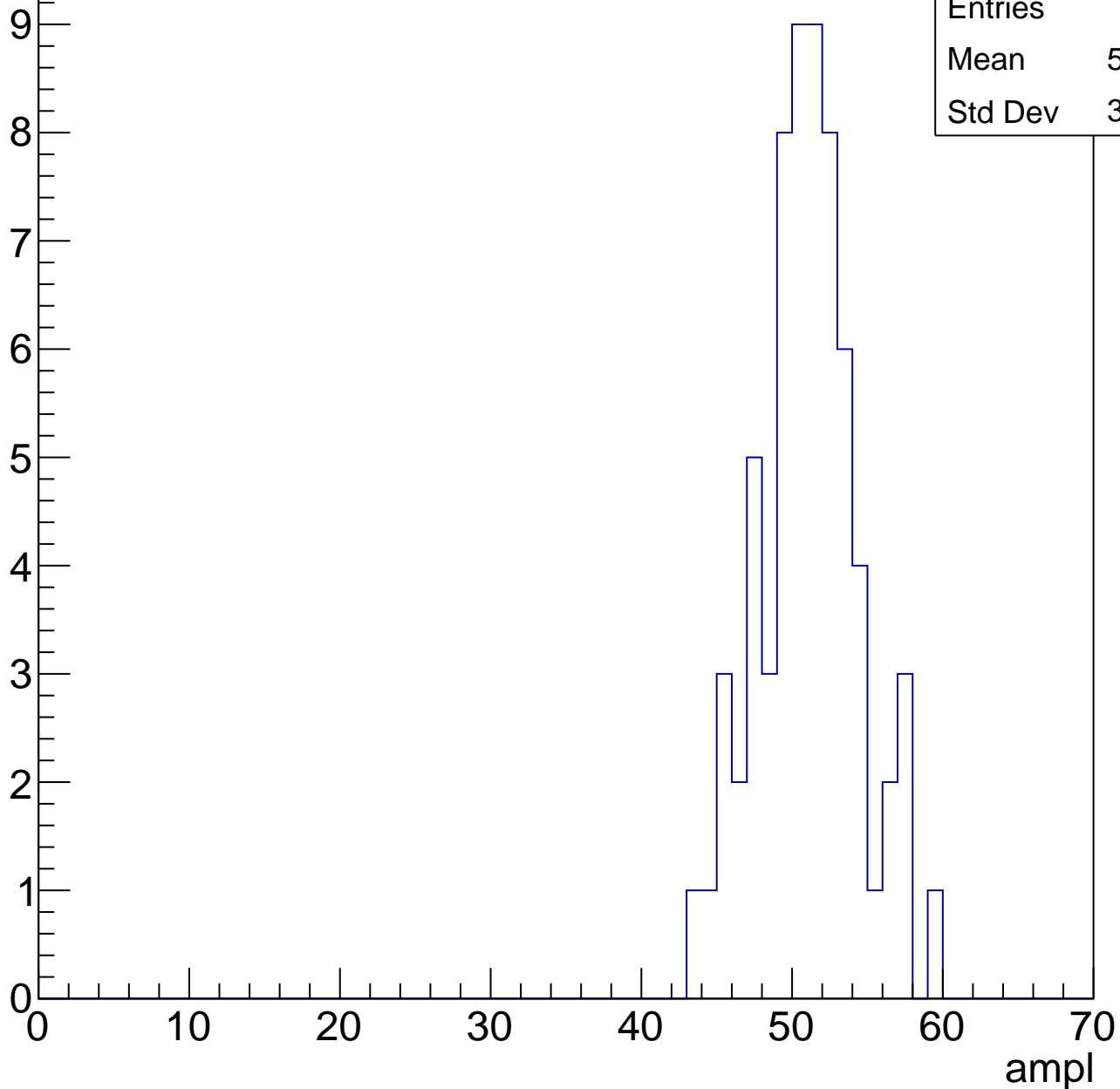
**Gaus Width: 3.2791**



# B1L102S, U8-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



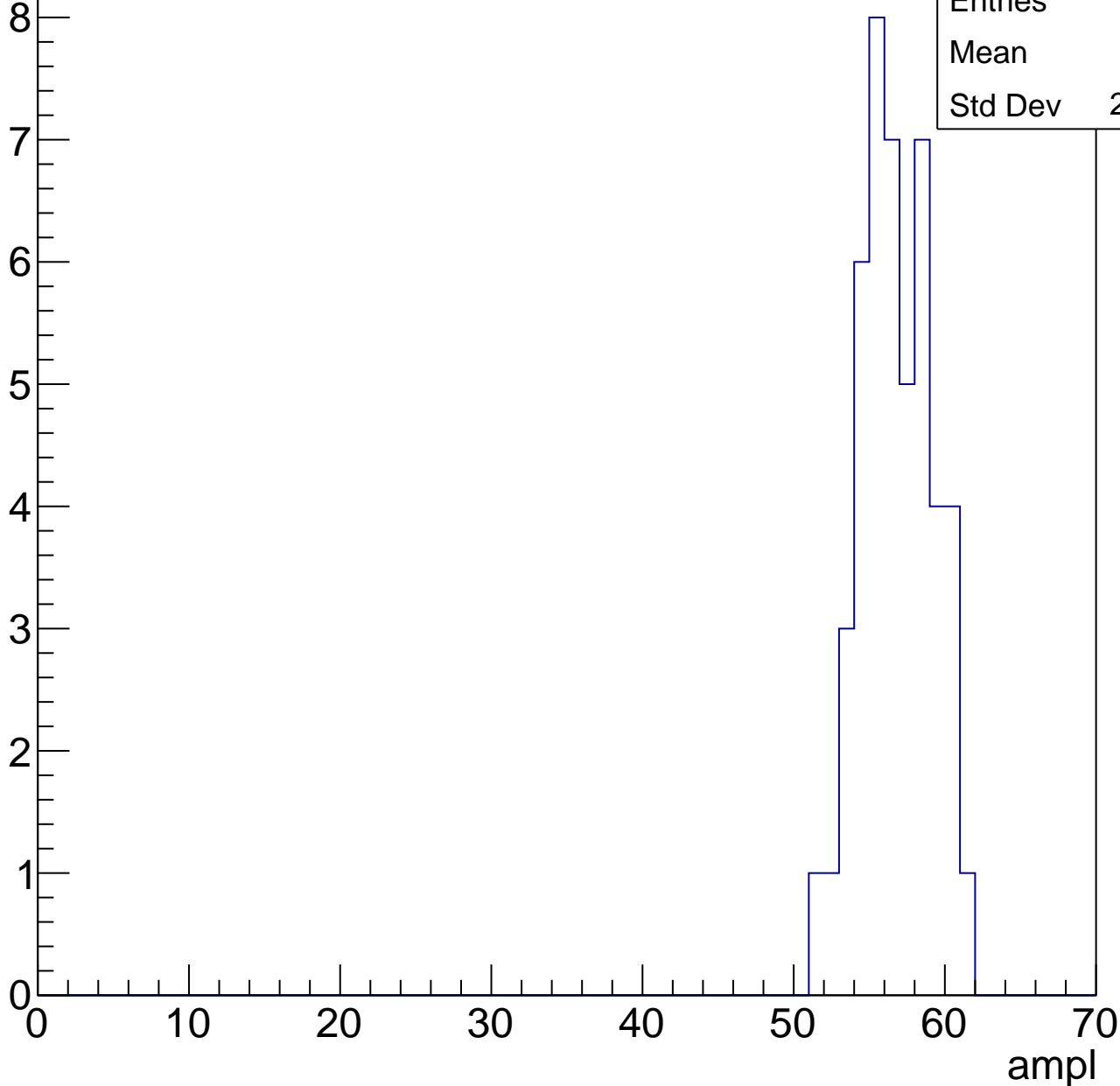
Entries	66
Mean	50.62
Std Dev	3.293

# B1L102S, U8-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

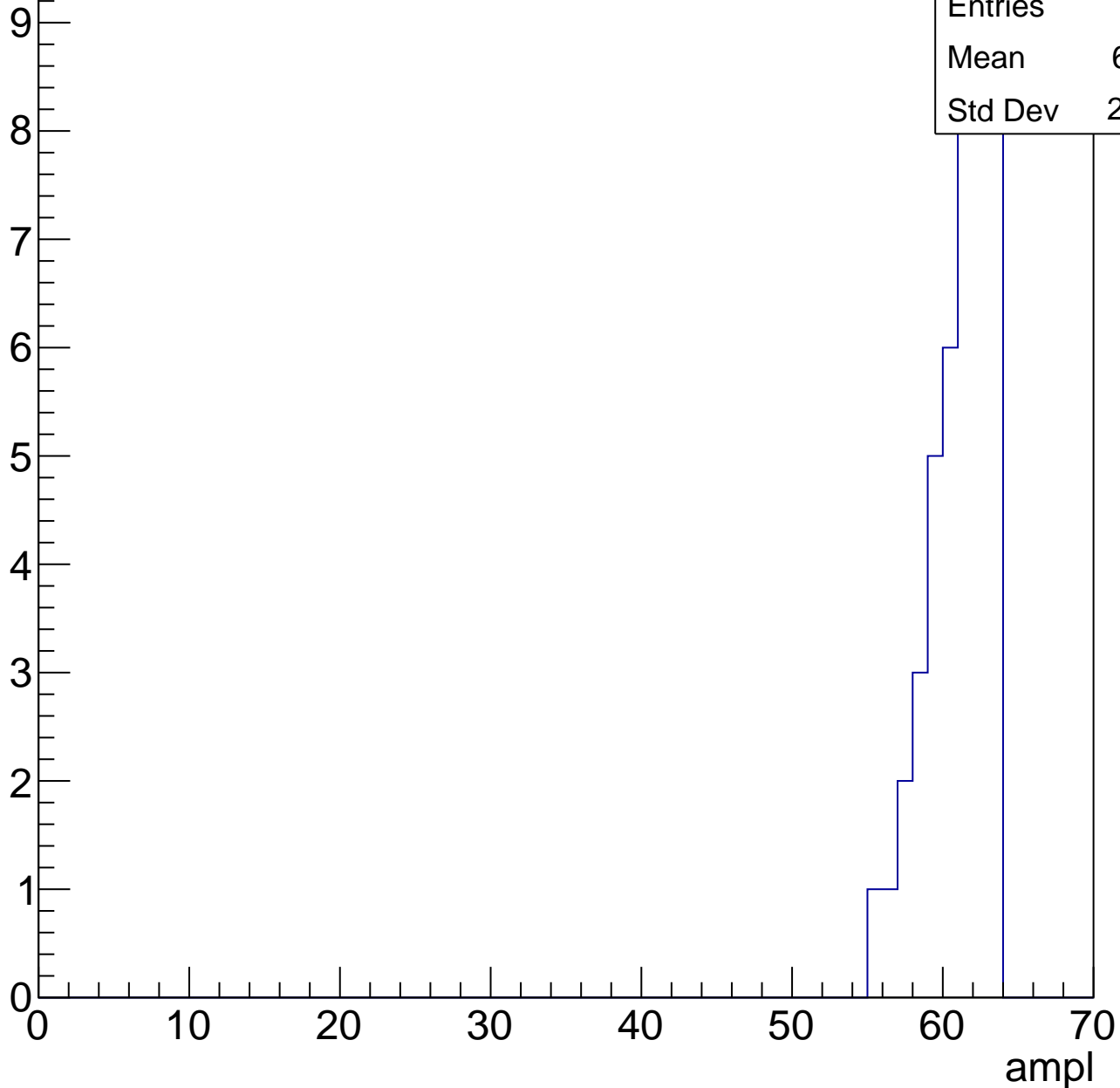
Entries	47
Mean	56.3
Std Dev	2.324



# B1L102S, U8-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch4, adc0

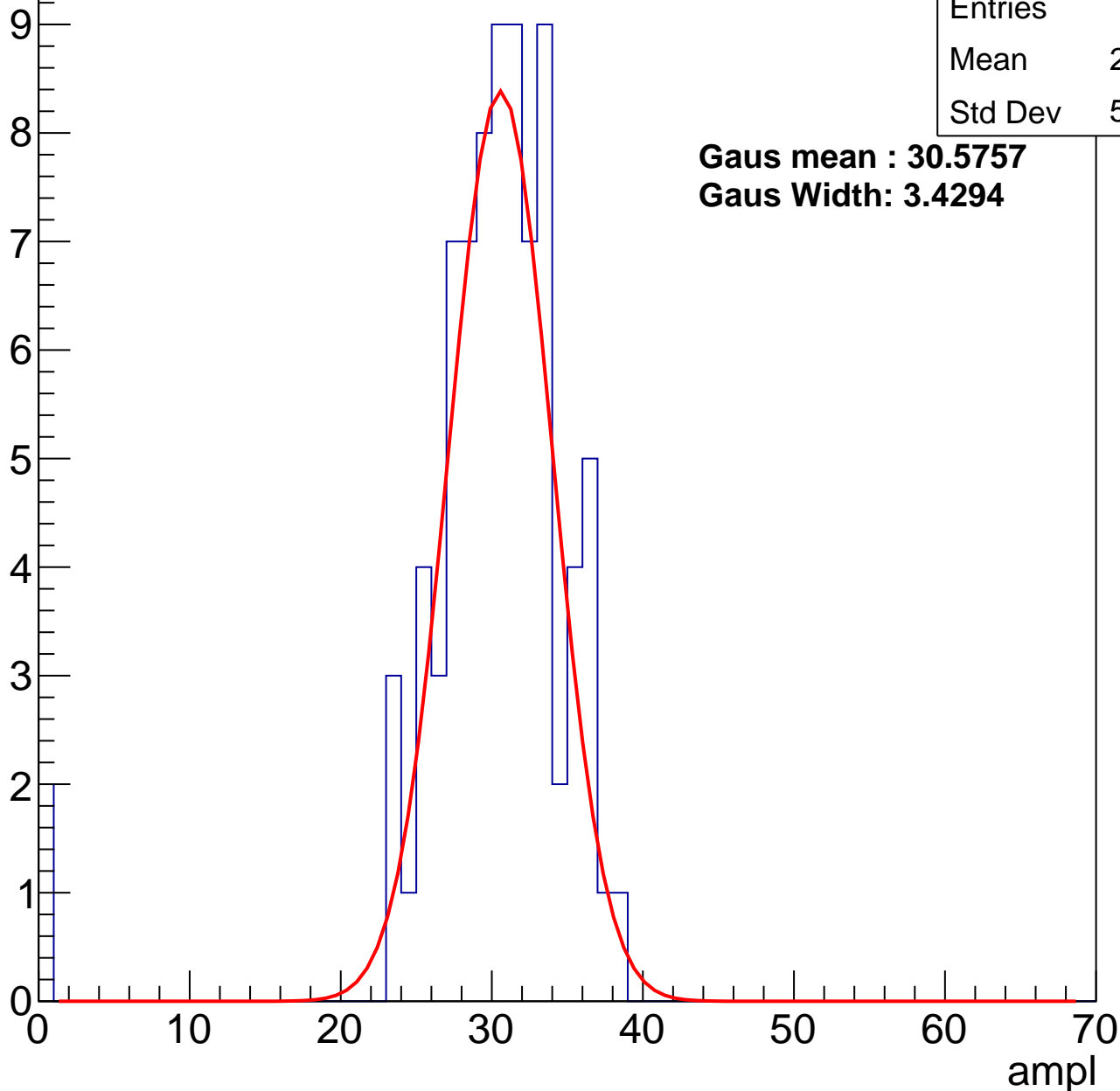
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	29.52
Std Dev	5.796

**Gaus mean : 30.5757**

**Gaus Width: 3.4294**



# B1L102S, U8-ch4, adc1

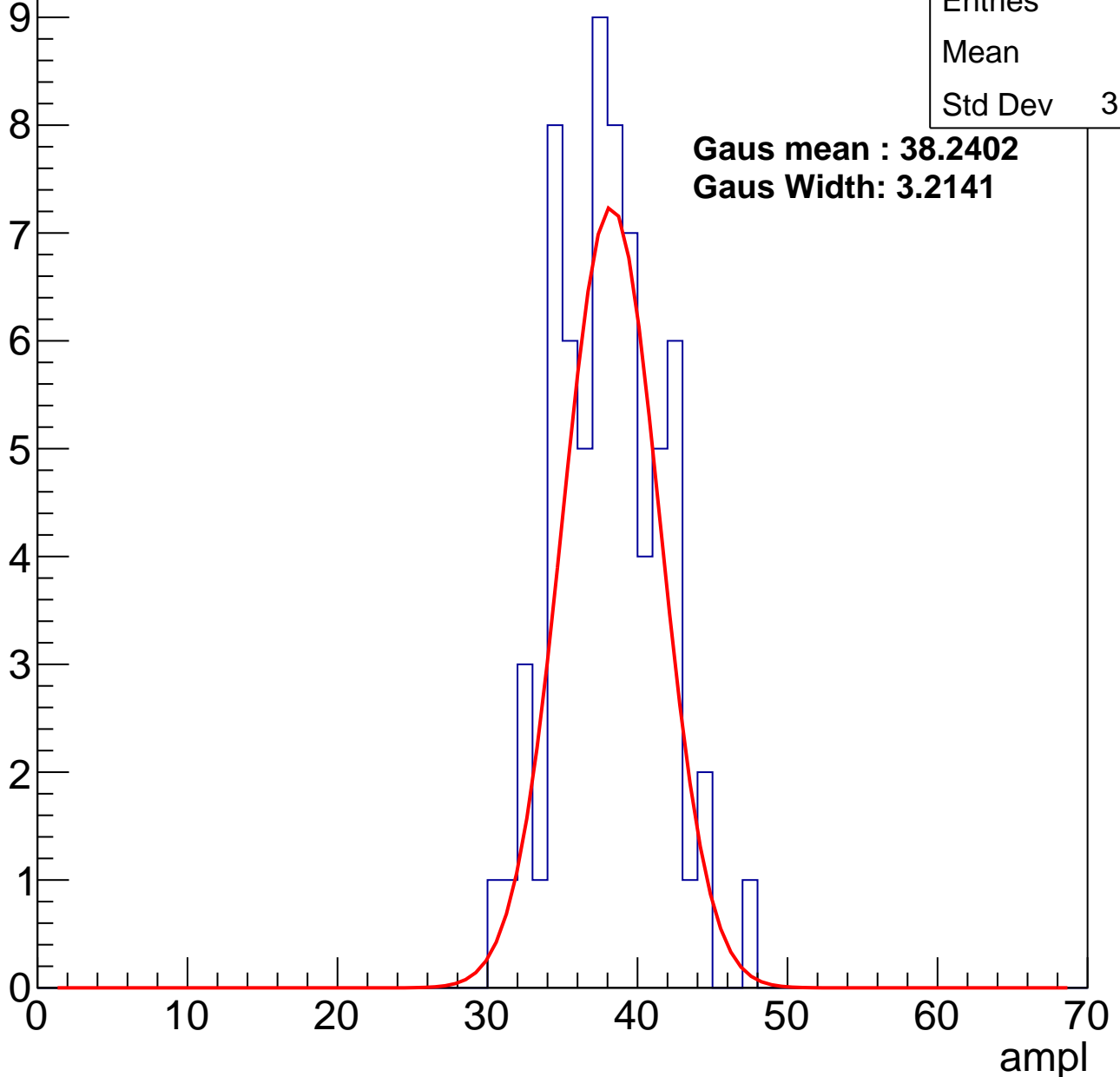
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	37.6
Std Dev	3.405

**Gaus mean : 38.2402**

**Gaus Width: 3.2141**



# B1L102S, U8-ch4, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	80
Mean	45.15
Std Dev	3.702

**Gaus mean : 45.4677**

**Gaus Width: 3.8030**

Entry

10

8

6

4

2

0

0

10

20

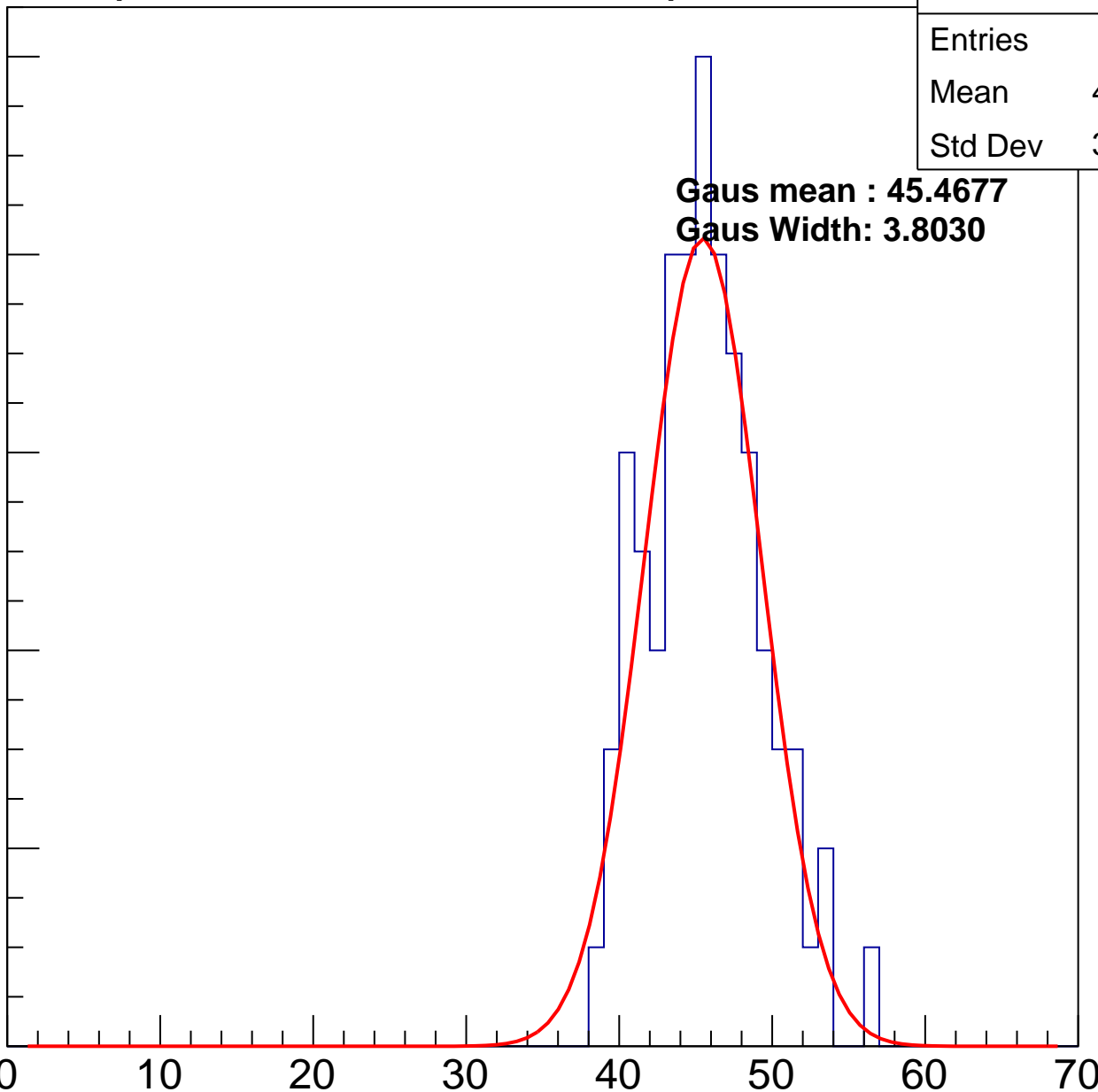
30

40

50

60

ampl

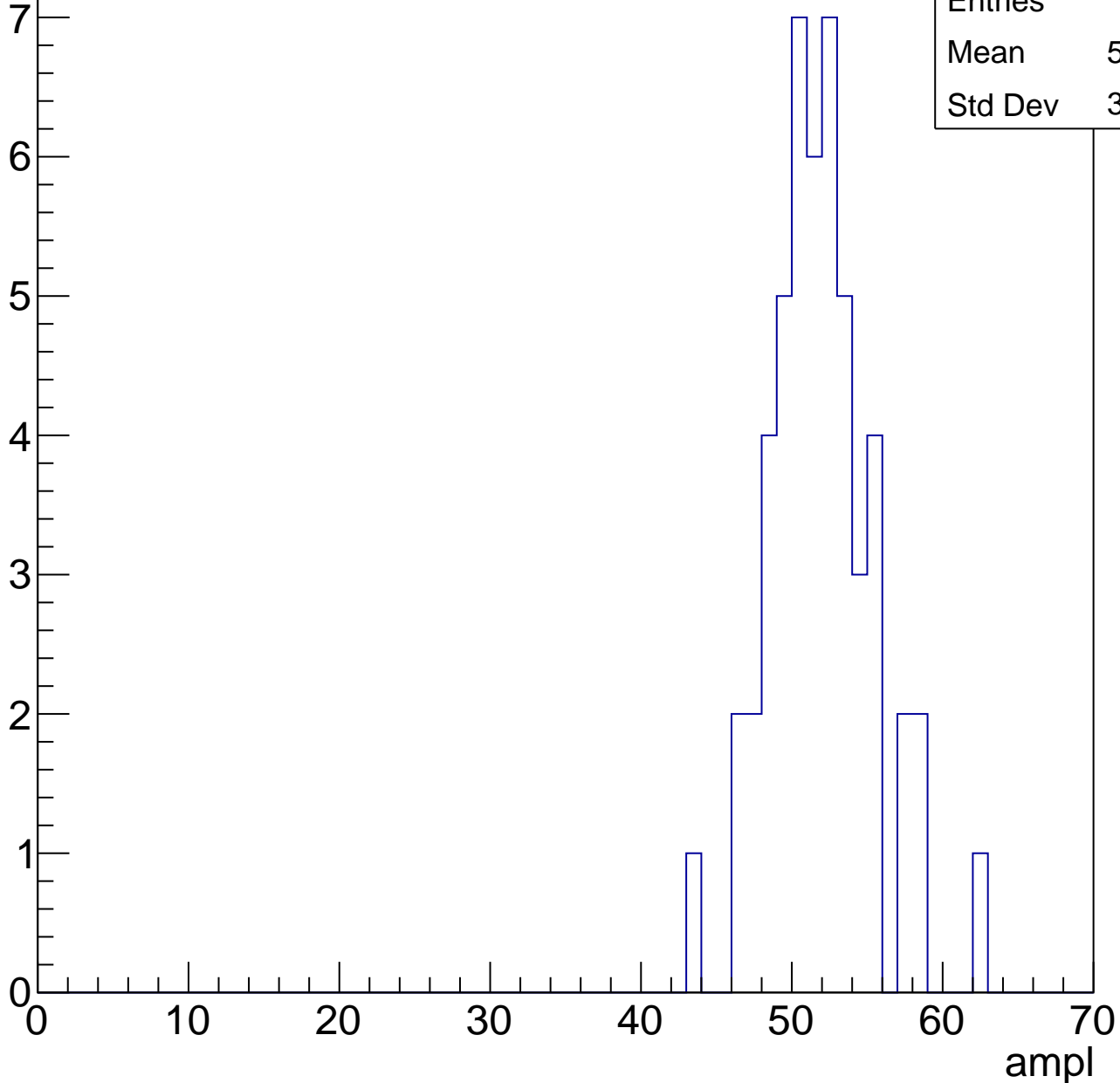


# B1L102S, U8-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	51.47
Std Dev	3.449

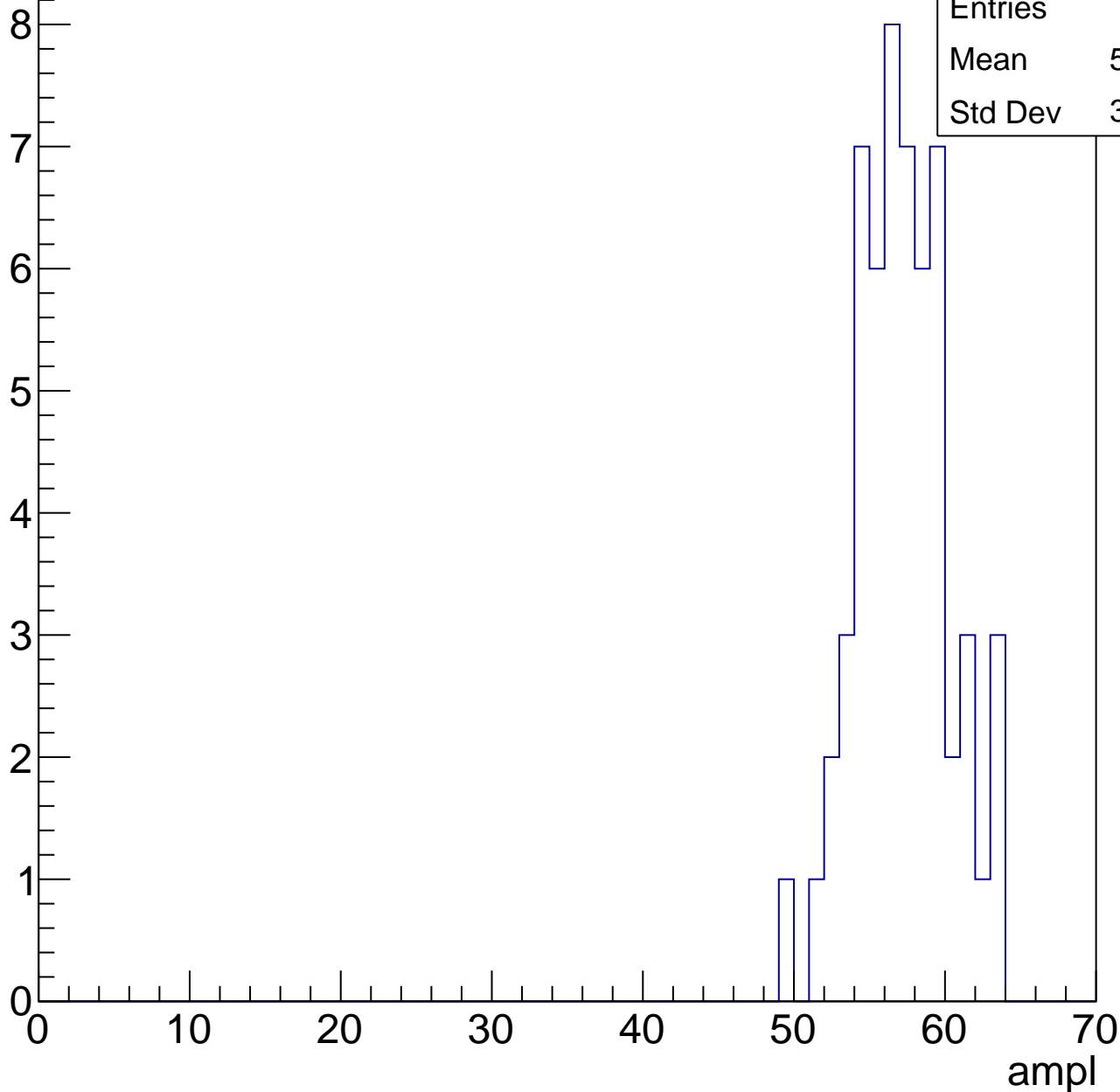


# B1L102S, U8-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	56.72
Std Dev	3.025



# B1L102S, U8-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

7

6

5

4

3

2

1

0

0

1

2

3

4

5

6

7

8

9

10

10

20

30

40

50

60

70

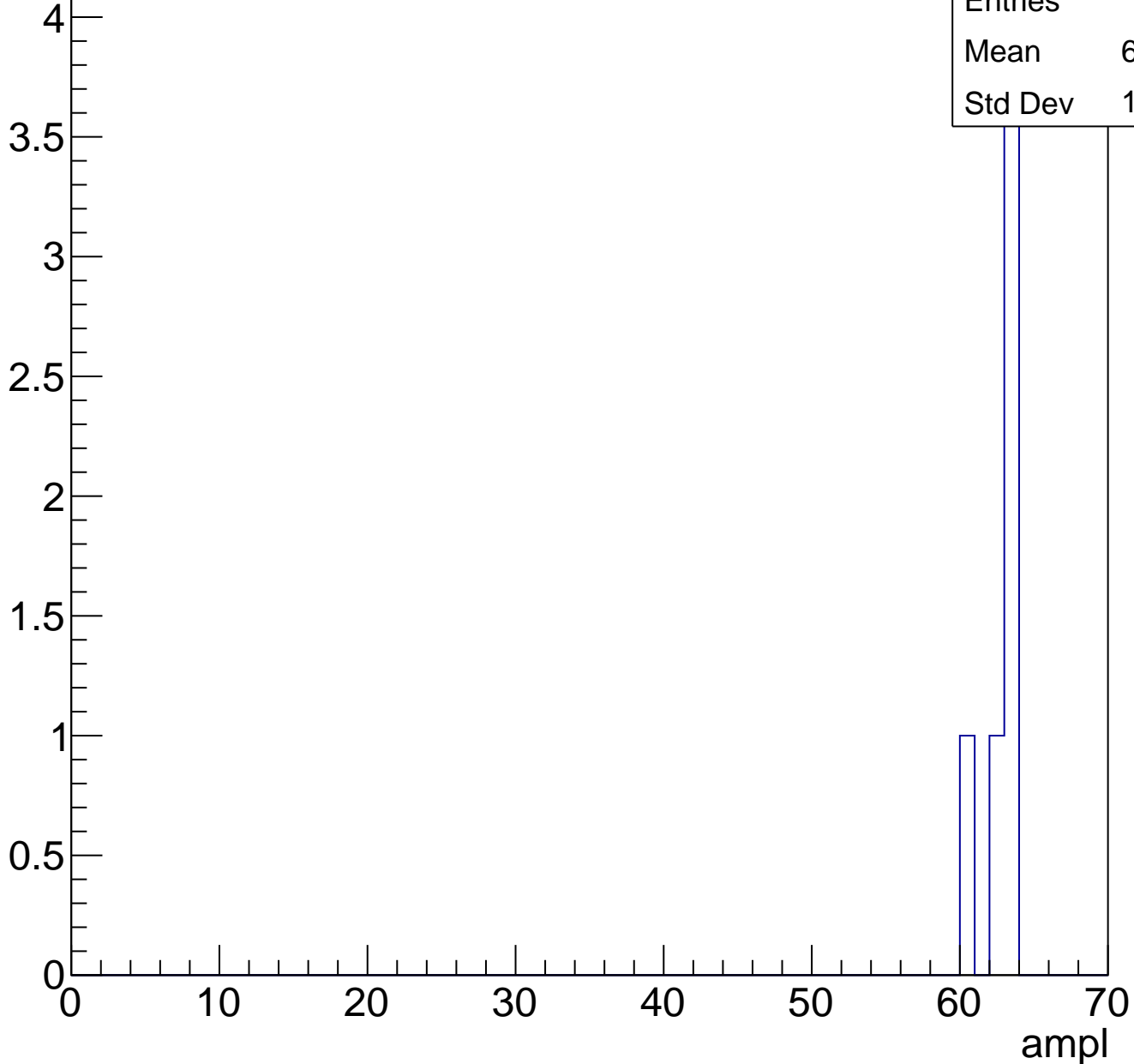
ampl

Entries	32
Mean	58.62
Std Dev	10.66

# B1L102S, U8-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch5, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	72
Mean	29.62
Std Dev	3.048

**Gaus mean : 30.0081**

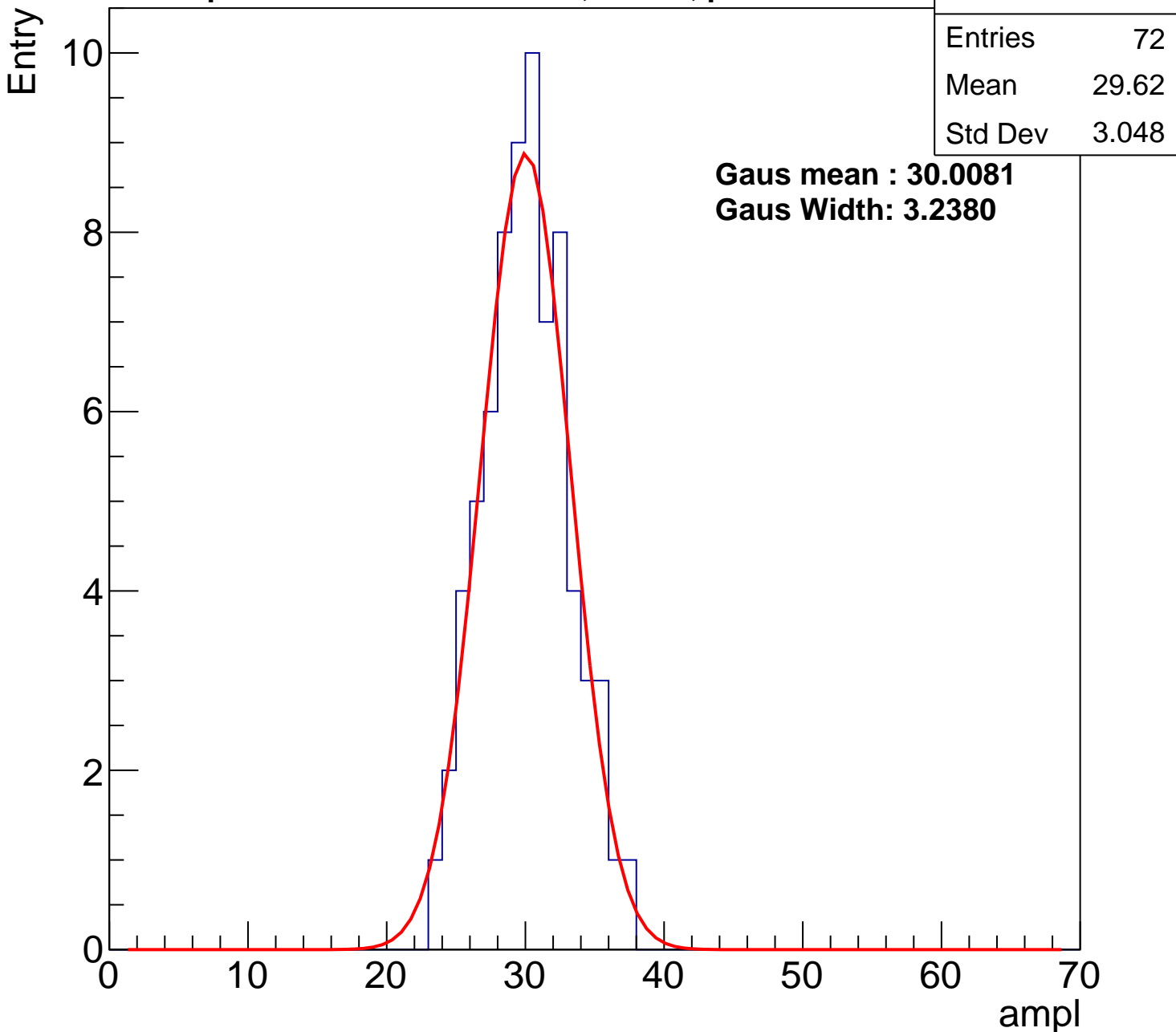
**Gaus Width: 3.2380**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



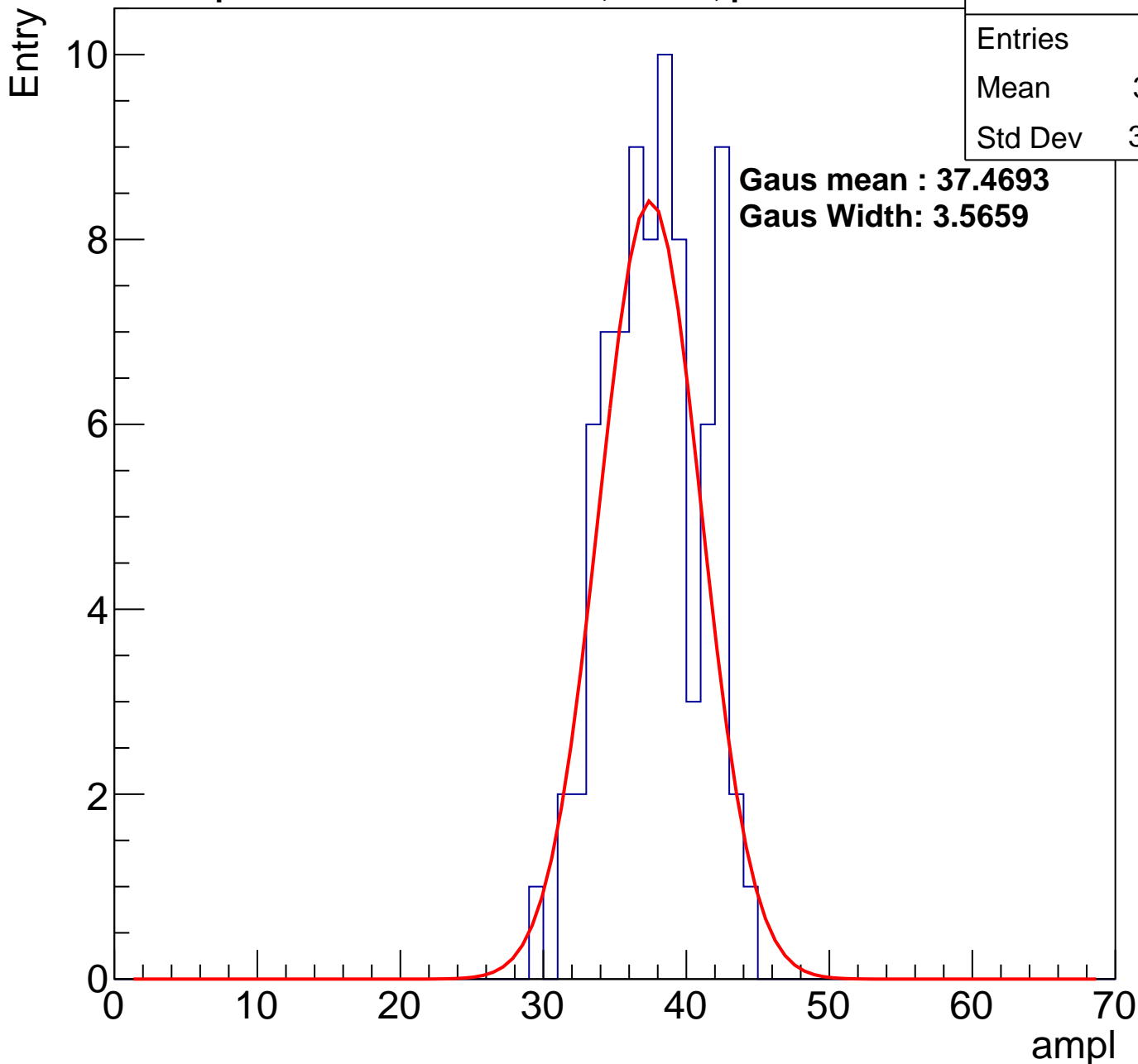
# B1L102S, U8-ch5, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	81
Mean	37.31
Std Dev	3.306

**Gaus mean : 37.4693**

**Gaus Width: 3.5659**



# B1L102S, U8-ch5, adc2

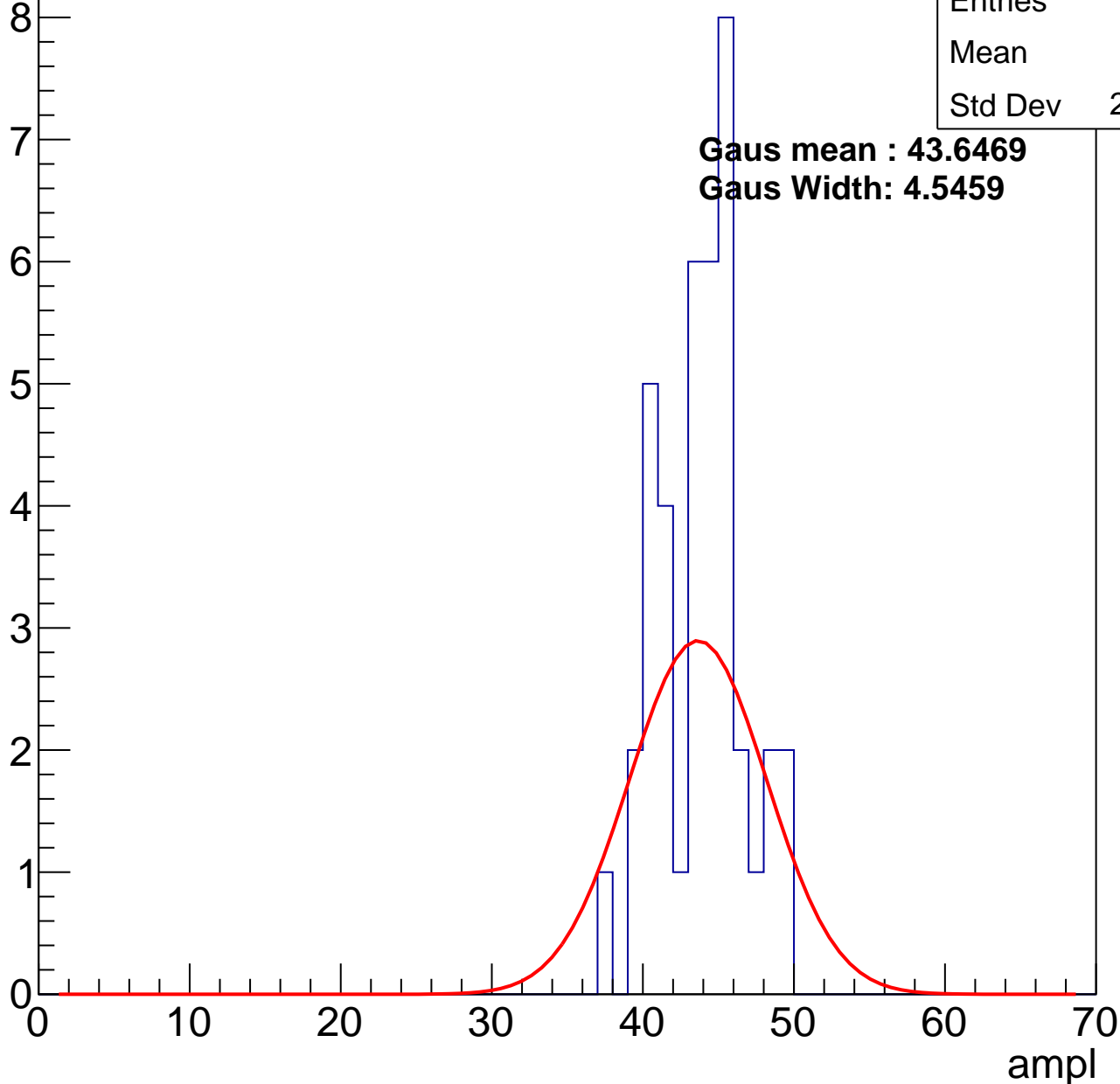
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	43.4
Std Dev	2.818

**Gaus mean : 43.6469**

**Gaus Width: 4.5459**

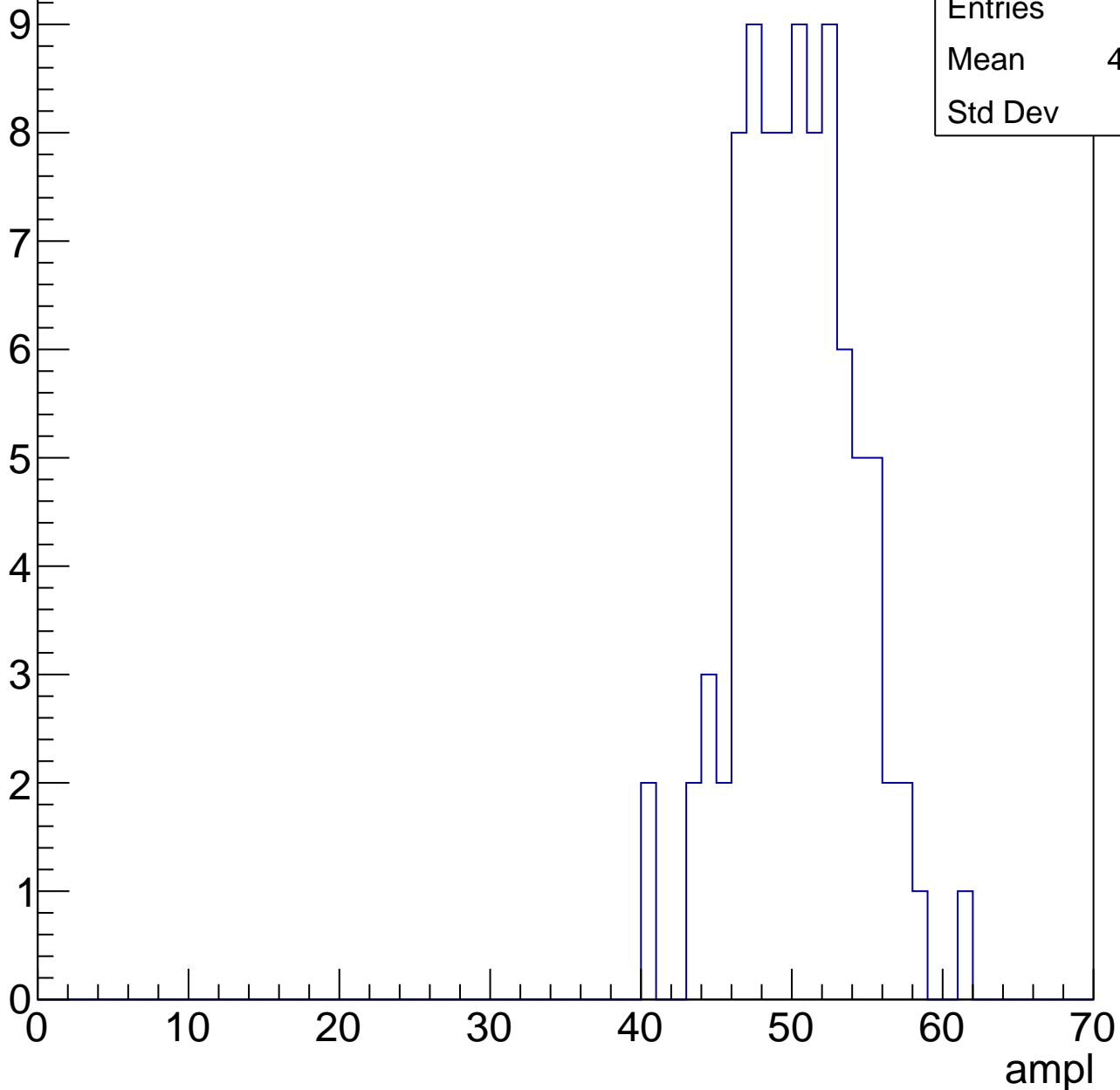


# B1L102S, U8-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	90
Mean	49.88
Std Dev	3.89

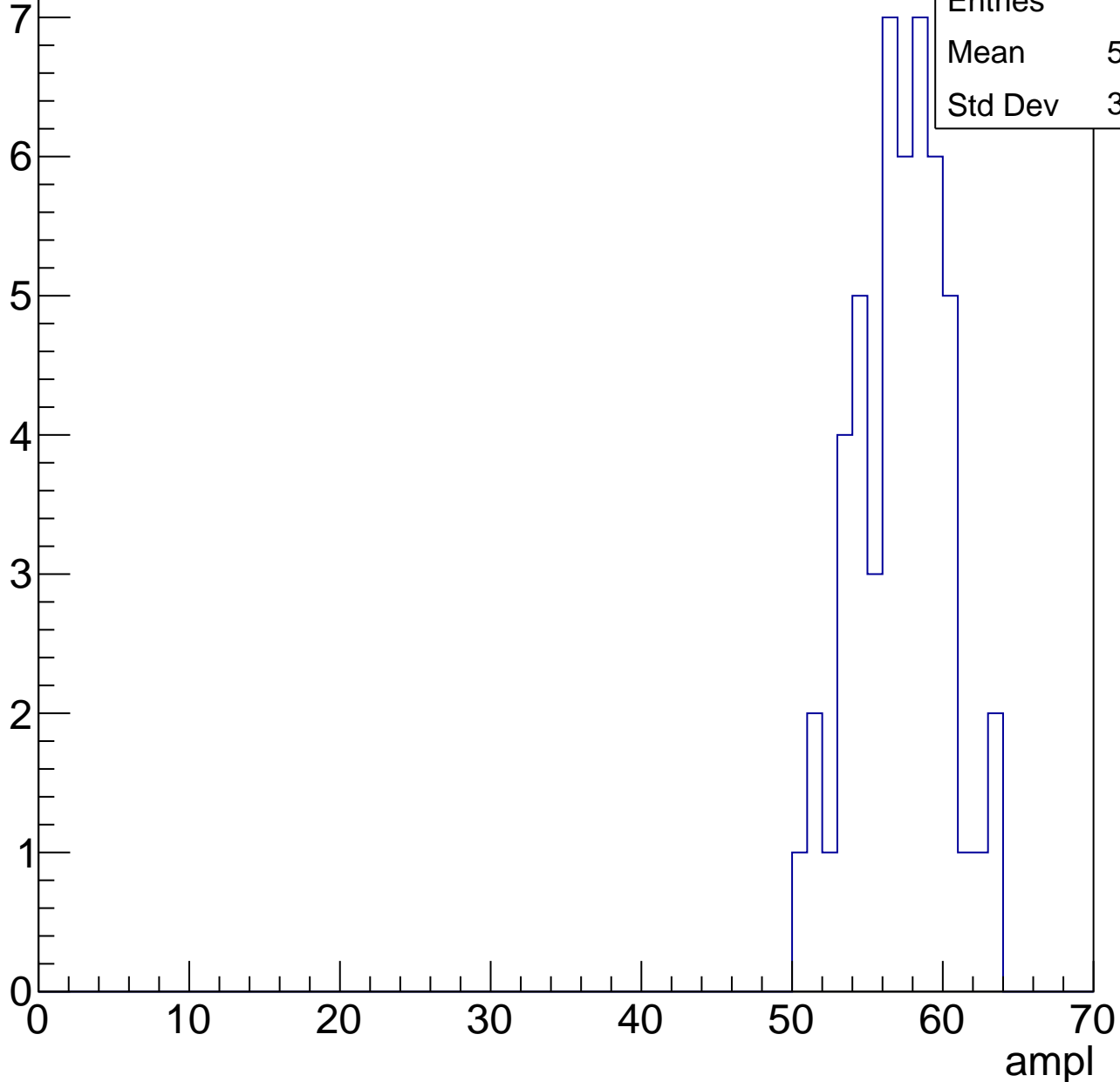


# B1L102S, U8-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

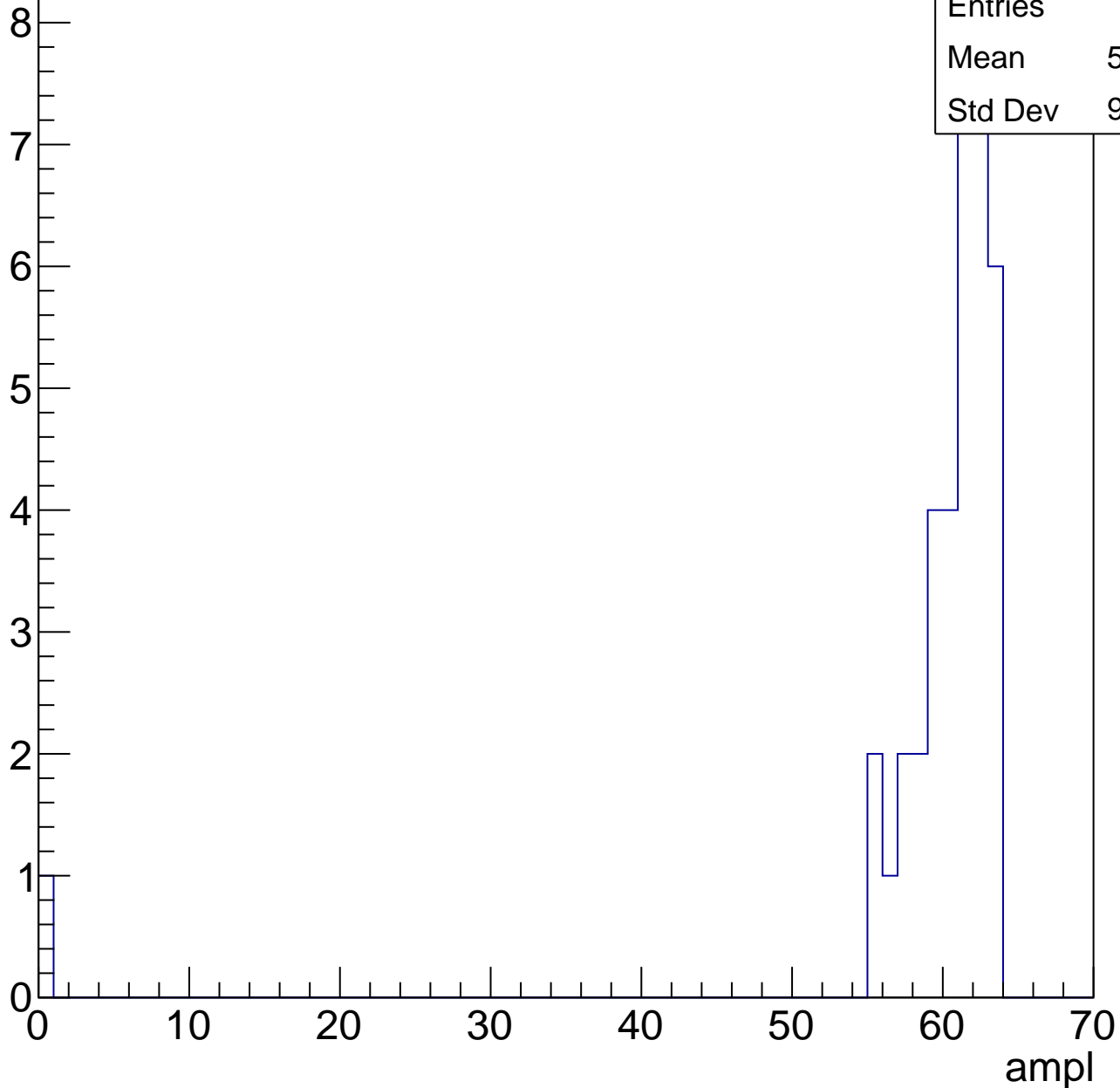
Entries	51
Mean	56.75
Std Dev	3.002



# B1L102S, U8-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	62
Std Dev	1.225

ampl

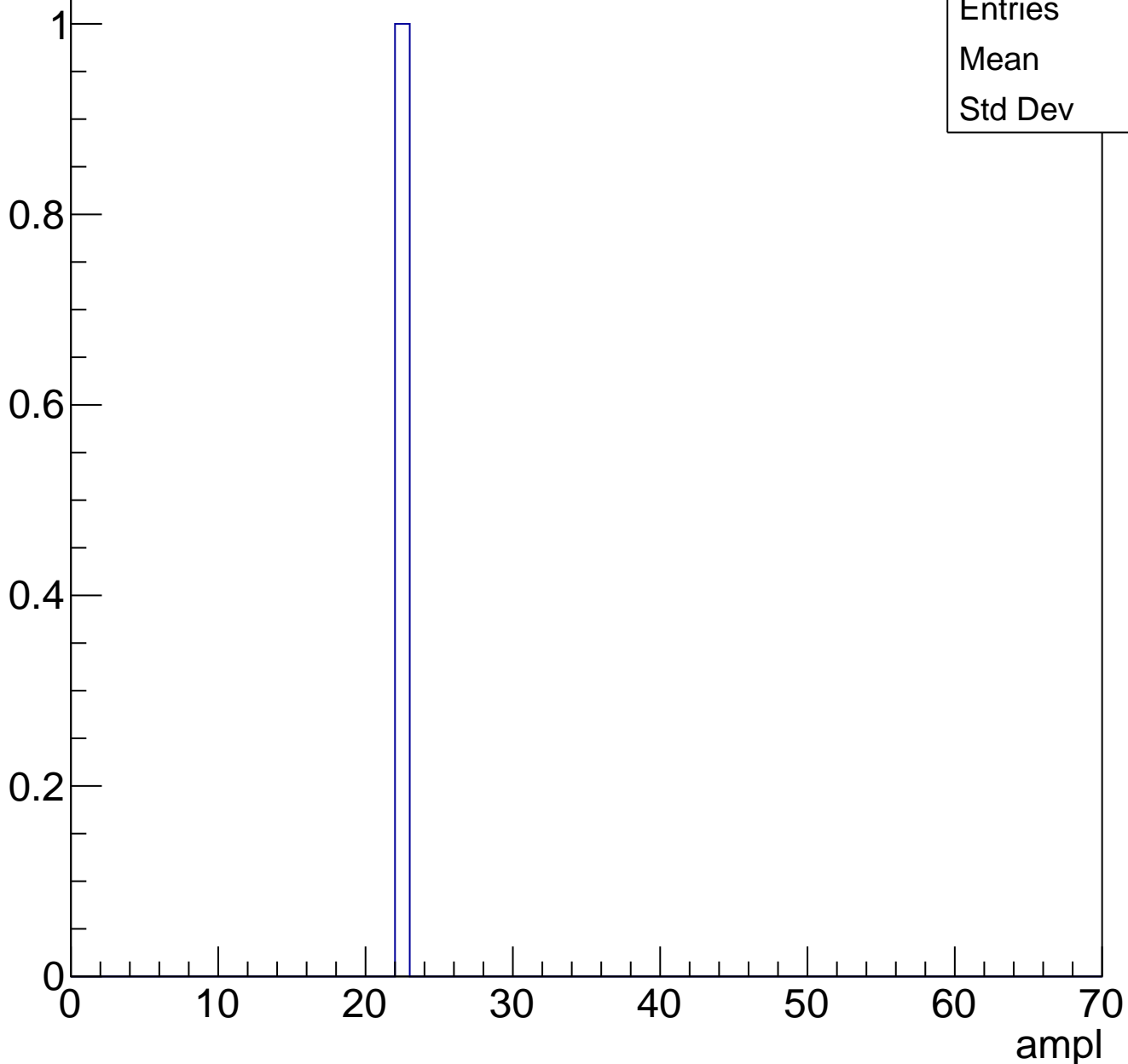
0 10 20 30 40 50 60 70



# B1L102S, U8-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	22
Std Dev	0

# B1L102S, U8-ch6, adc0

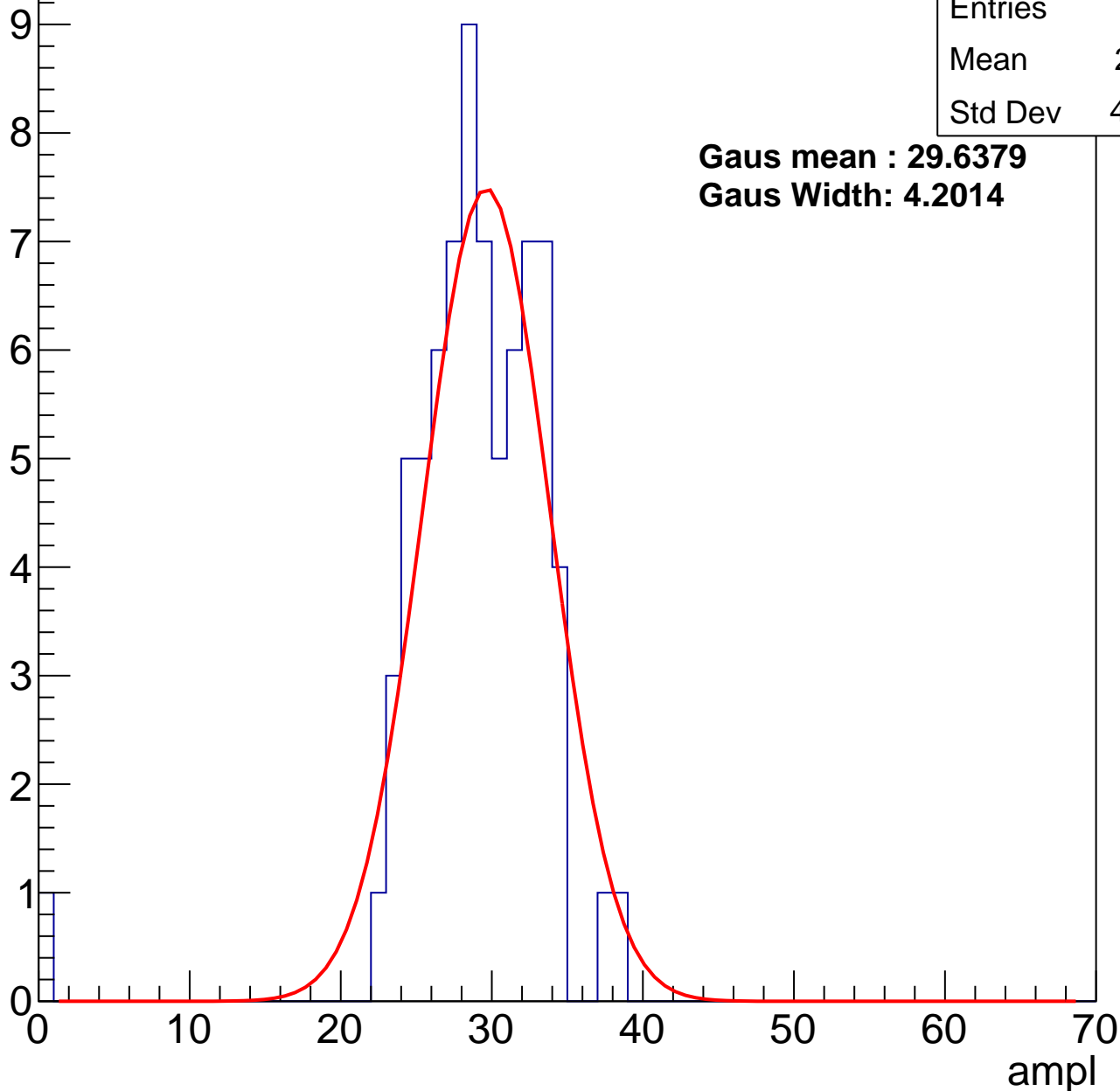
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	28.51
Std Dev	4.795

**Gaus mean : 29.6379**

**Gaus Width: 4.2014**



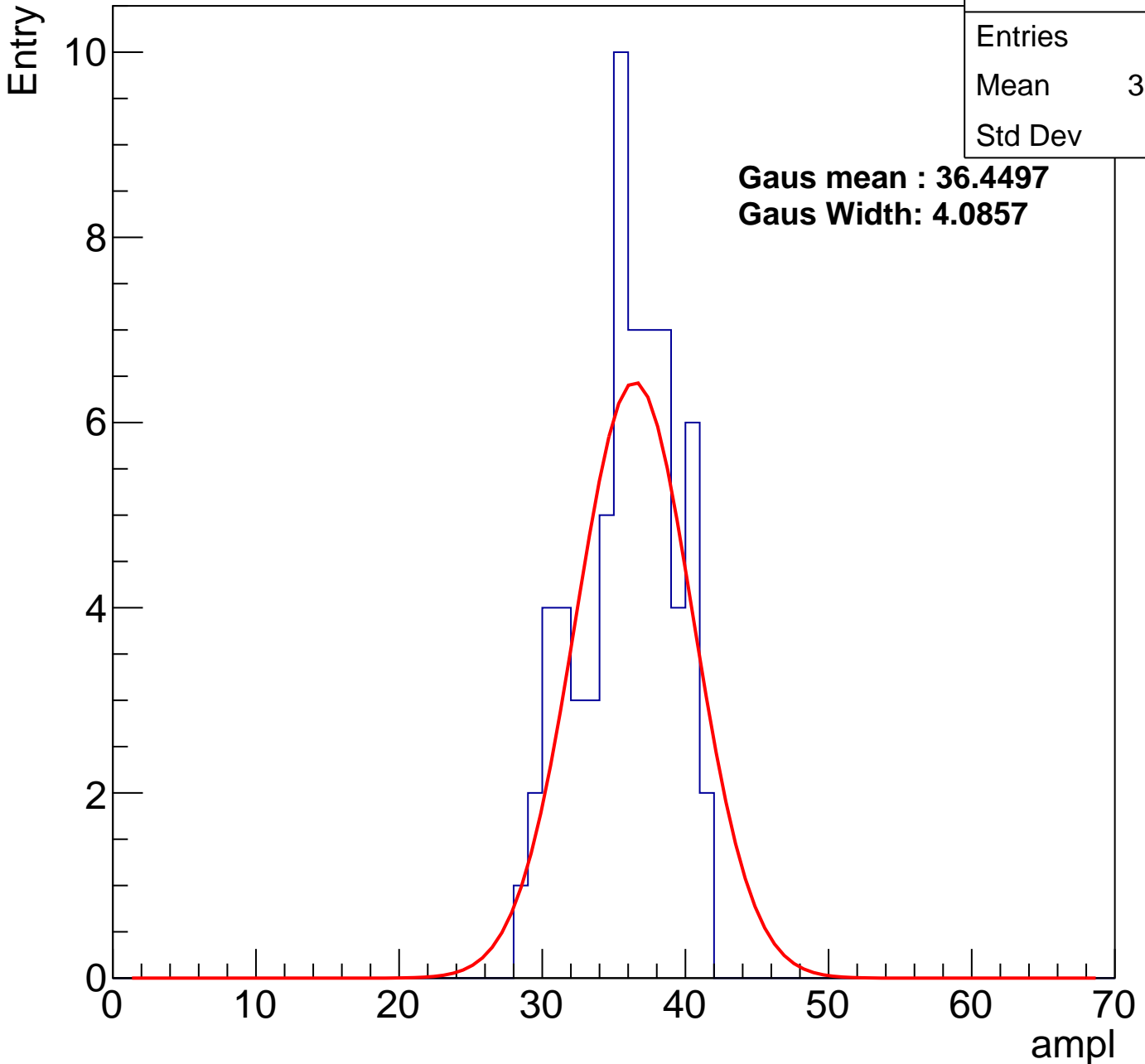
# B1L102S, U8-ch6, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	65
Mean	35.38
Std Dev	3.29

**Gaus mean : 36.4497**

**Gaus Width: 4.0857**



# B1L102S, U8-ch6, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	79
Mean	42.97
Std Dev	3.628

**Gaus mean : 43.4437**

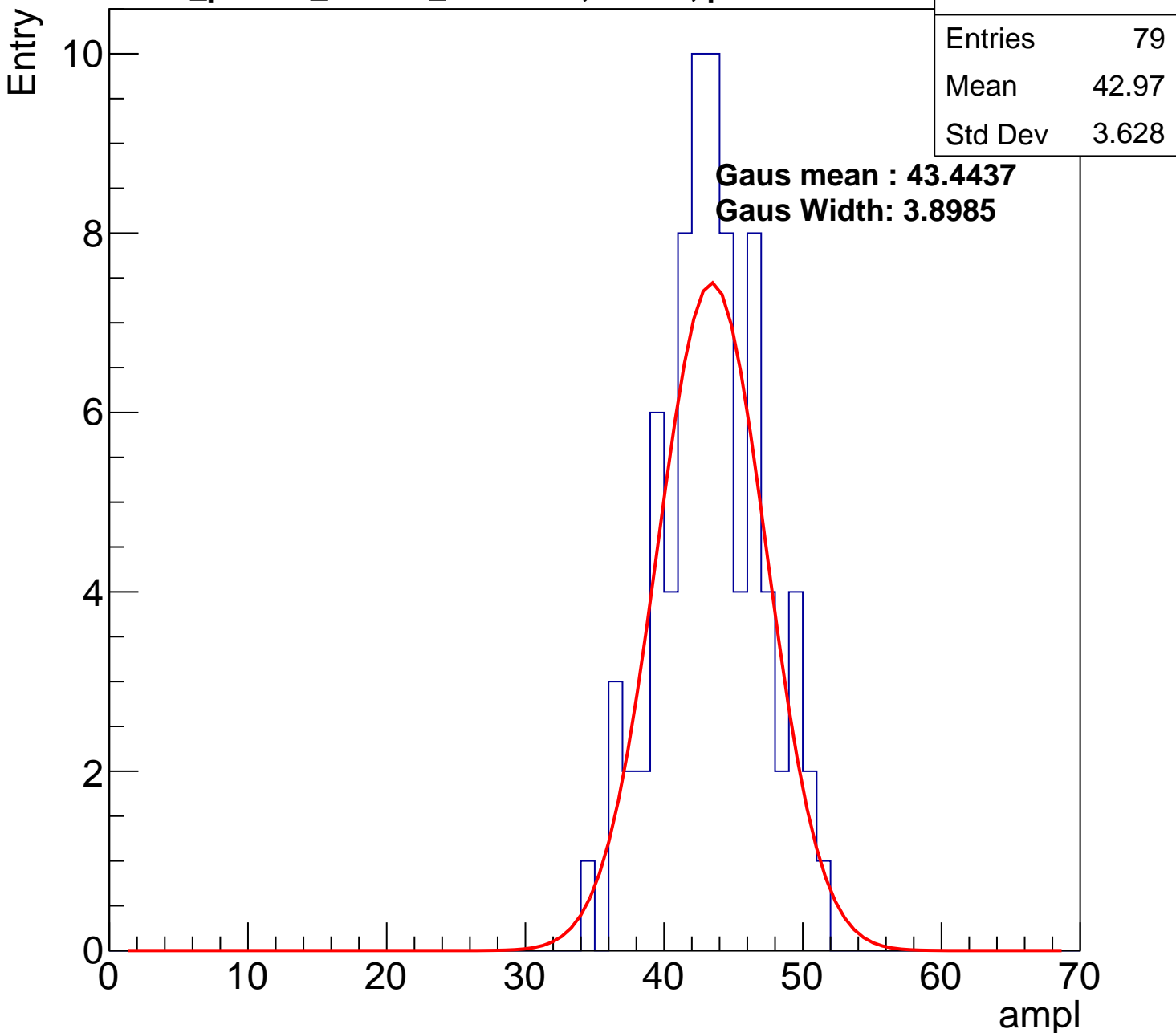
**Gaus Width: 3.8985**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U8-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

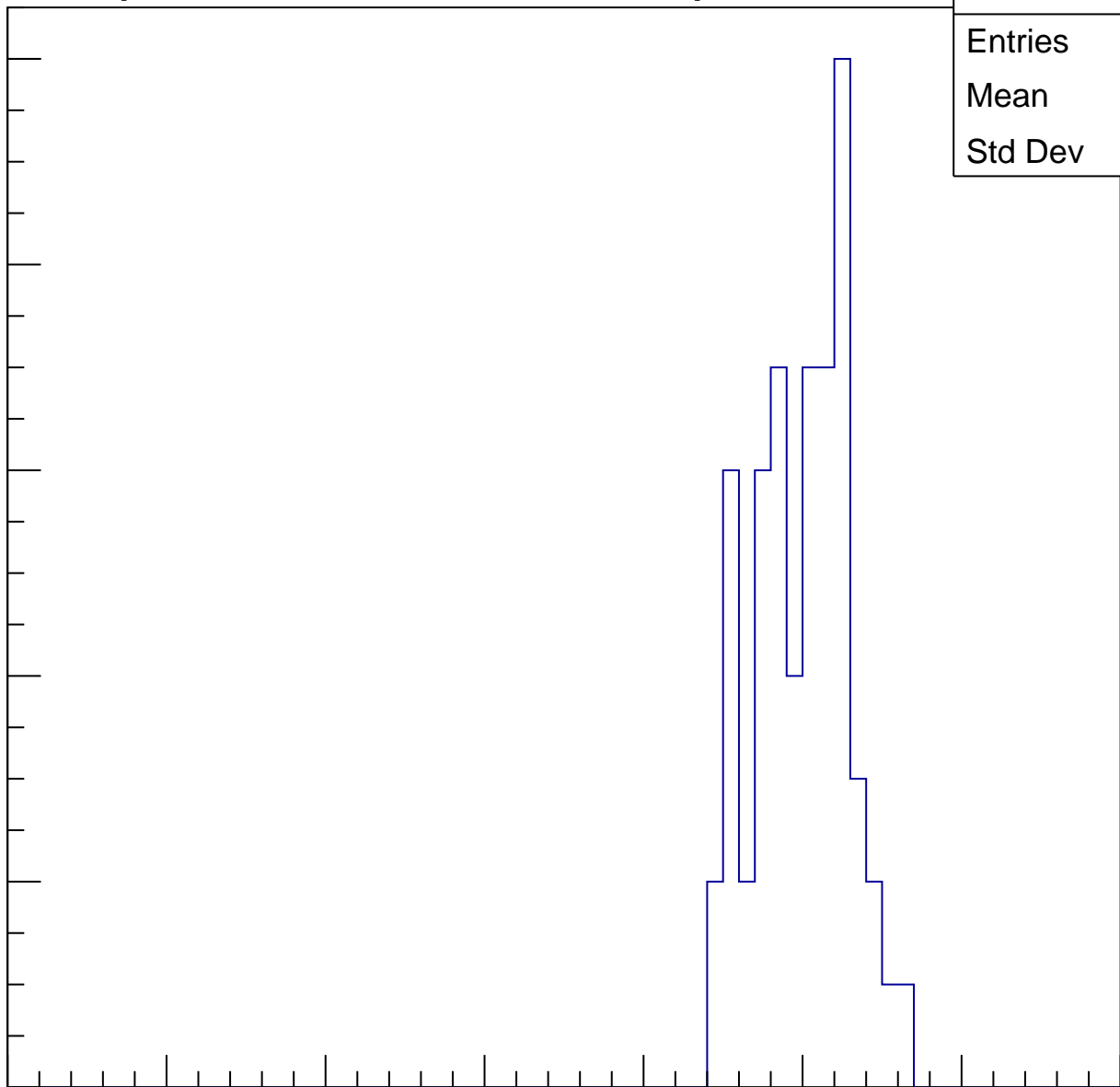
Entries	58
Mean	49.47
Std Dev	2.908

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

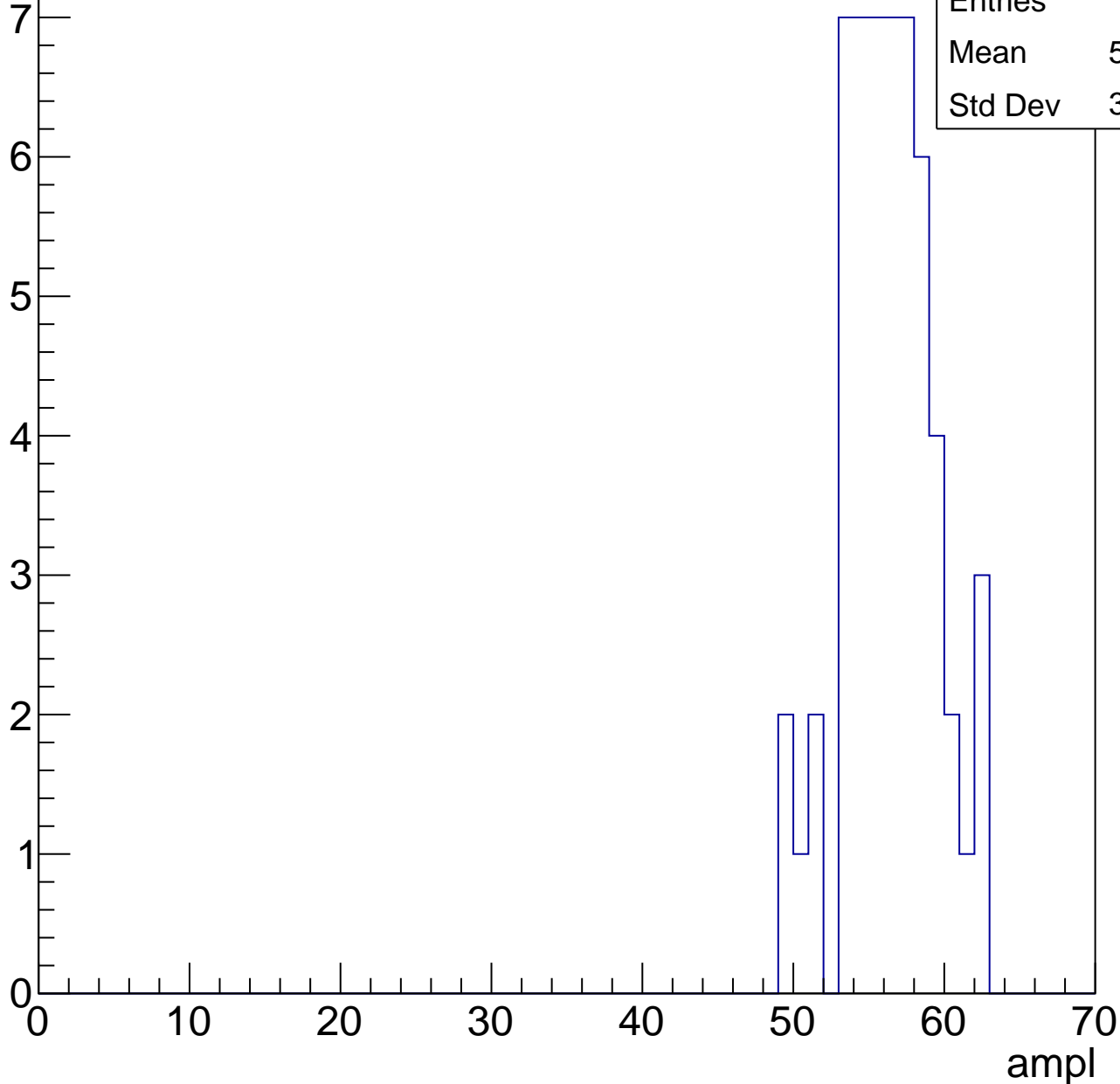


# B1L102S, U8-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	55.82
Std Dev	3.024

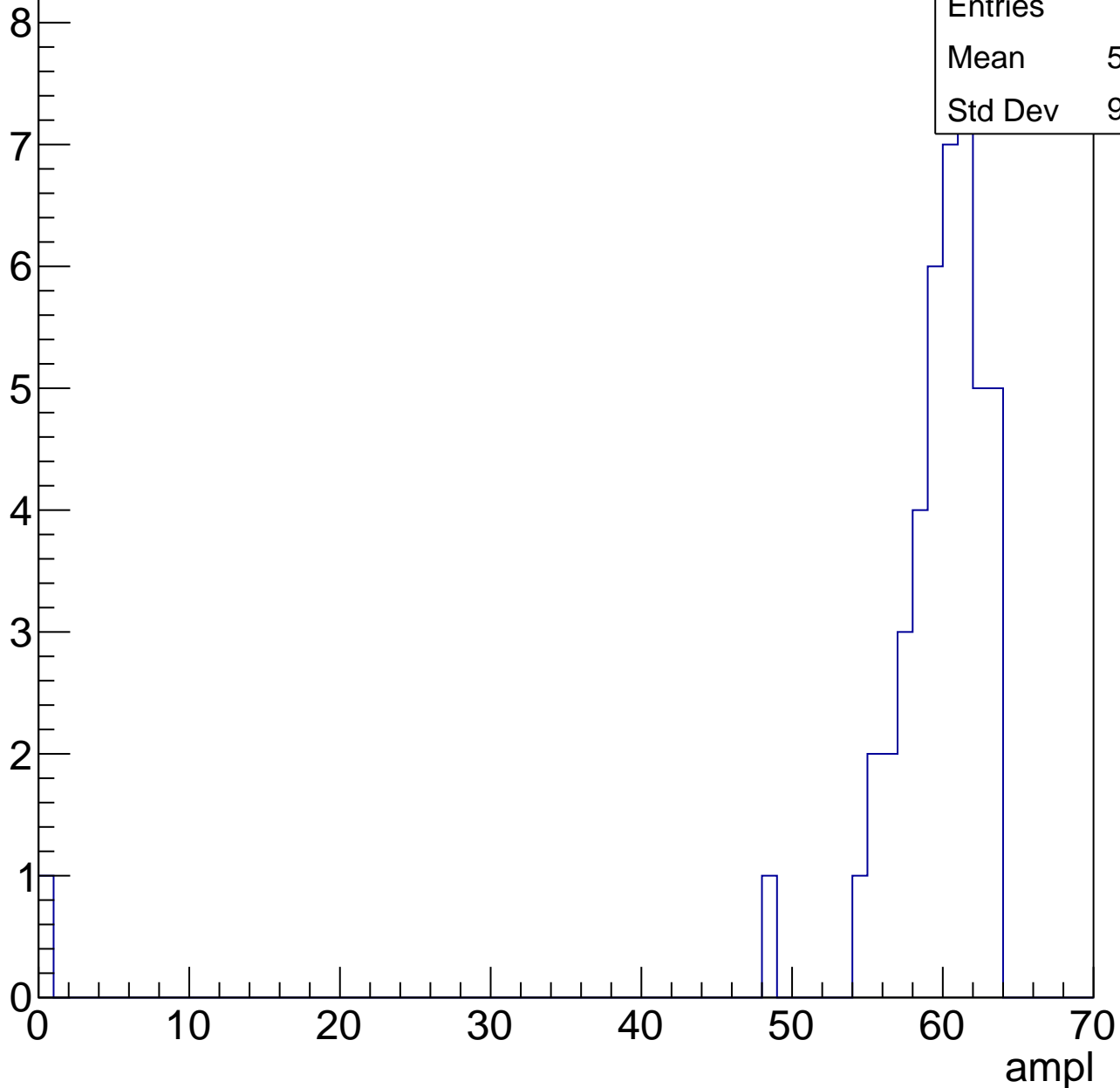


# B1L102S, U8-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	58.09
Std Dev	9.213

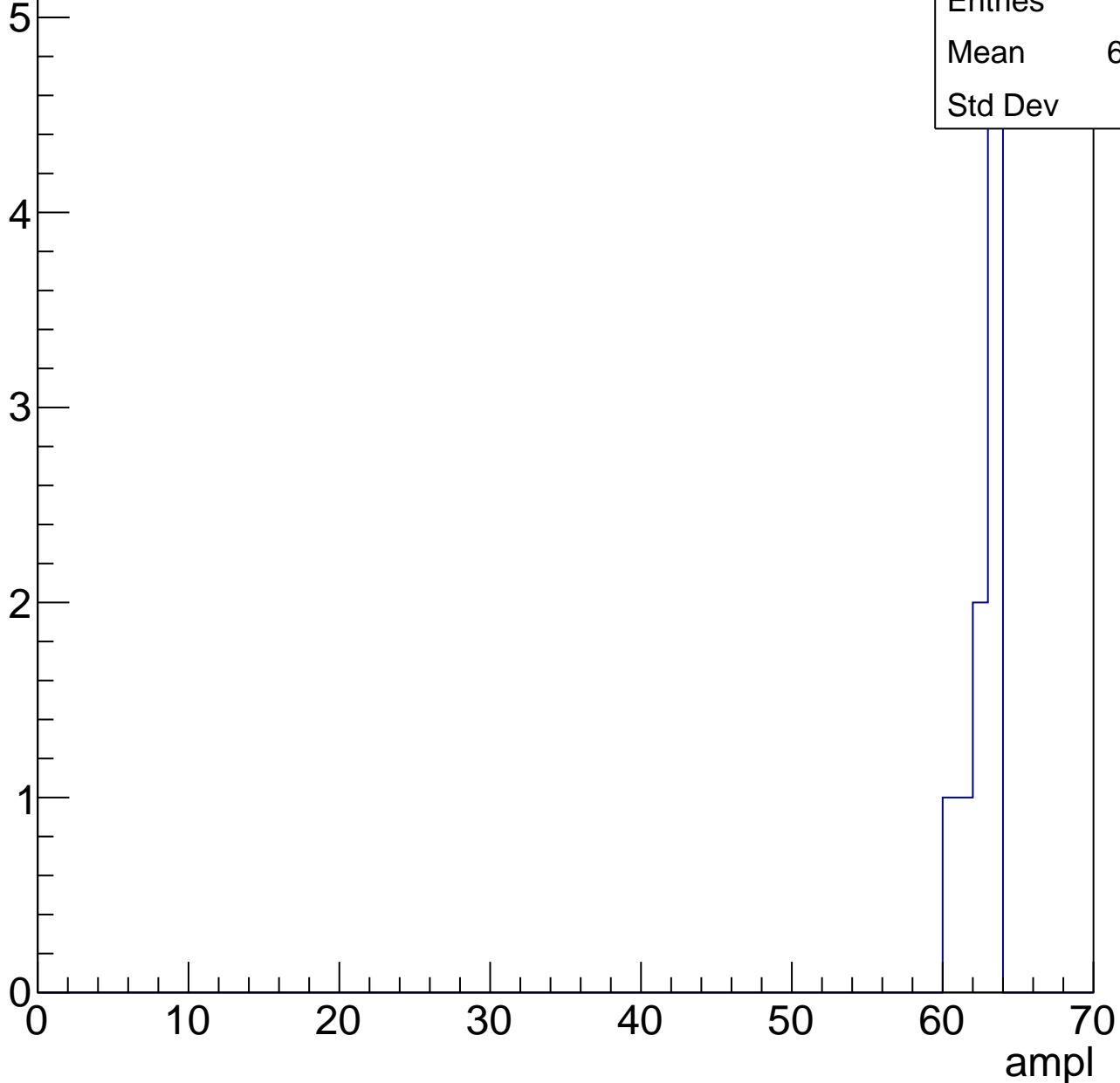


# B1L102S, U8-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	9
Mean	62.22
Std Dev	1.03





# B1L102S, U8-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch7, adc0

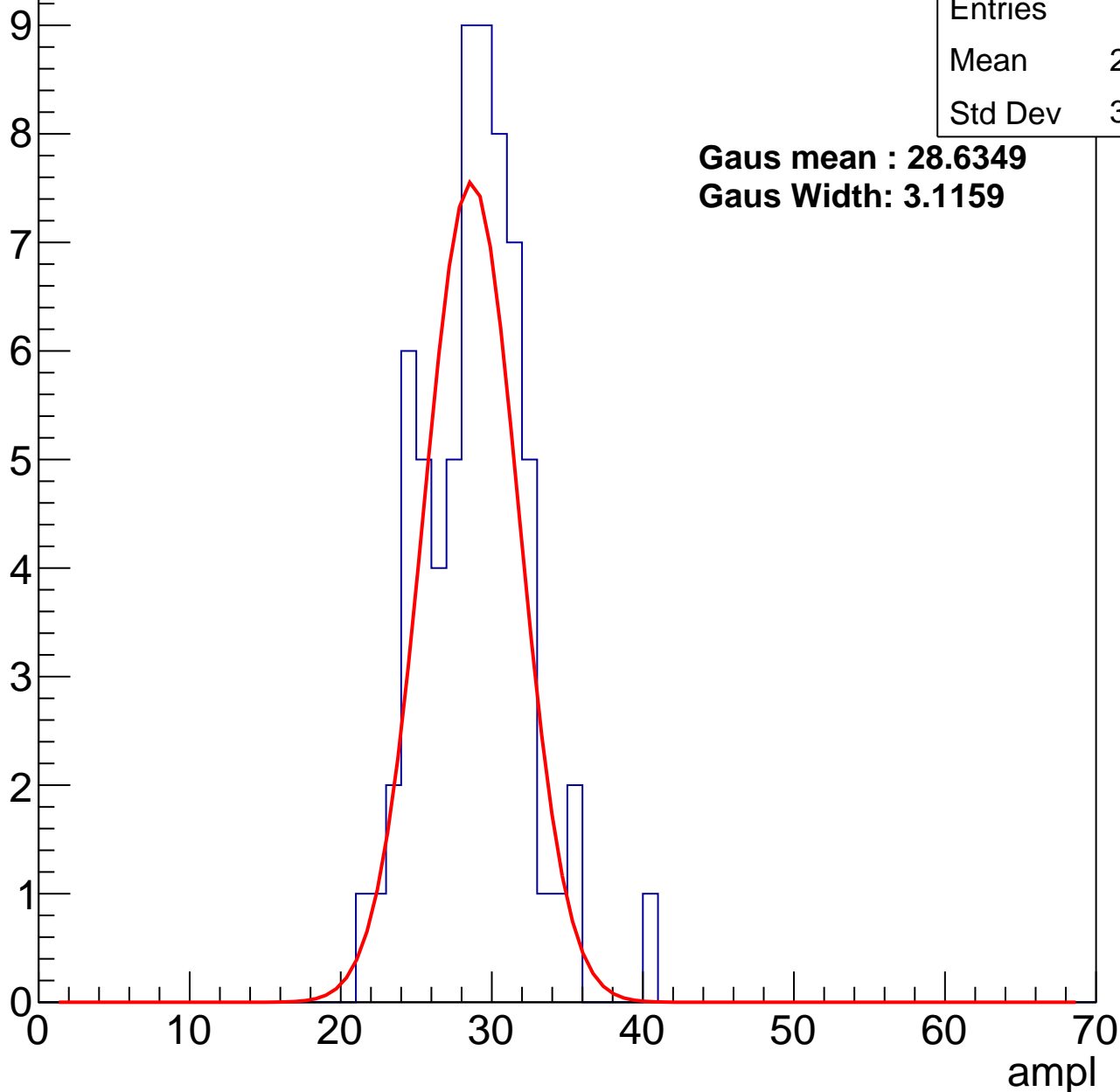
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	28.42
Std Dev	3.395

**Gaus mean : 28.6349**

**Gaus Width: 3.1159**



# B1L102S, U8-ch7, adc1

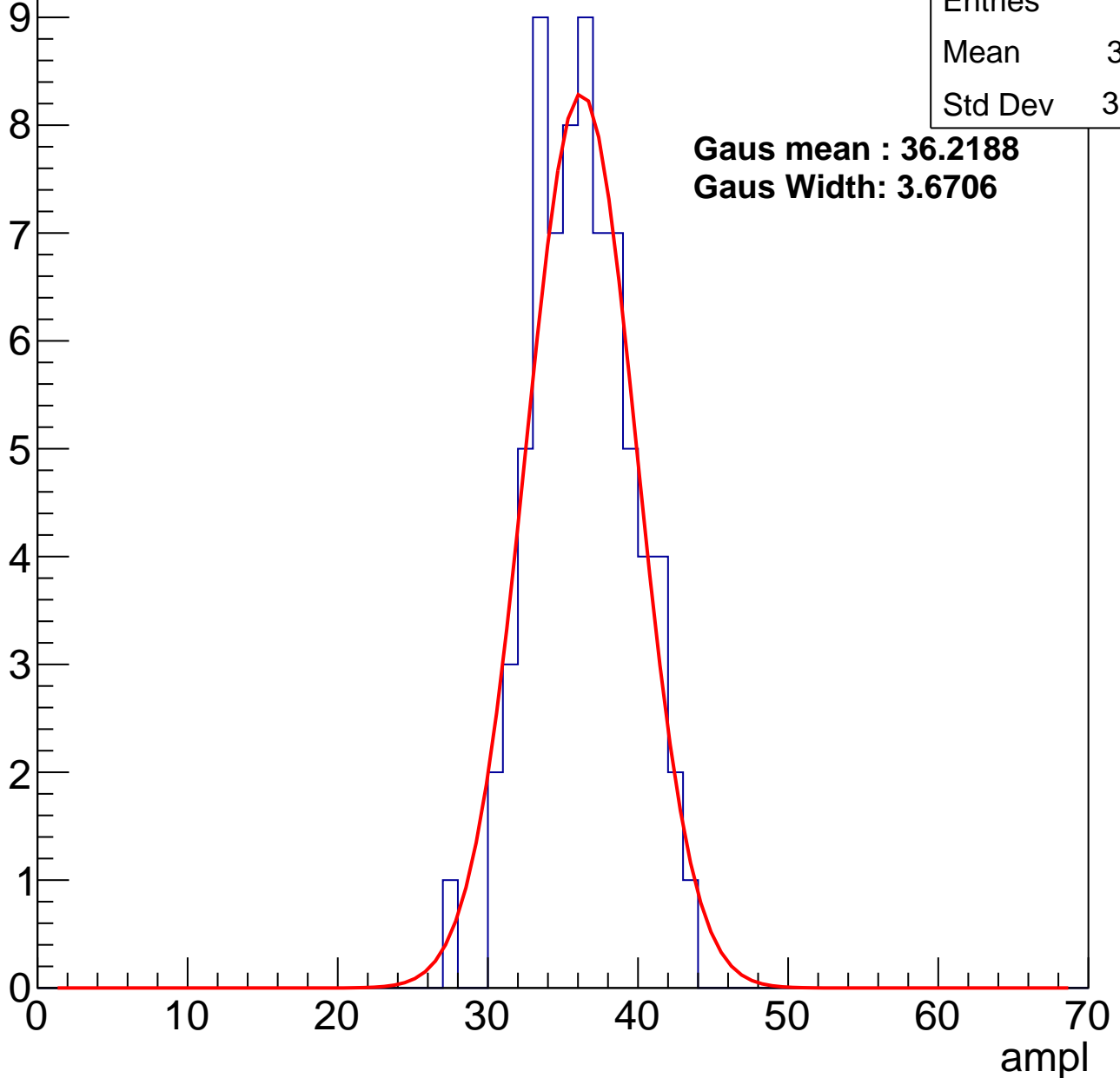
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	35.81
Std Dev	3.262

**Gaus mean : 36.2188**

**Gaus Width: 3.6706**



# B1L102S, U8-ch7, adc2

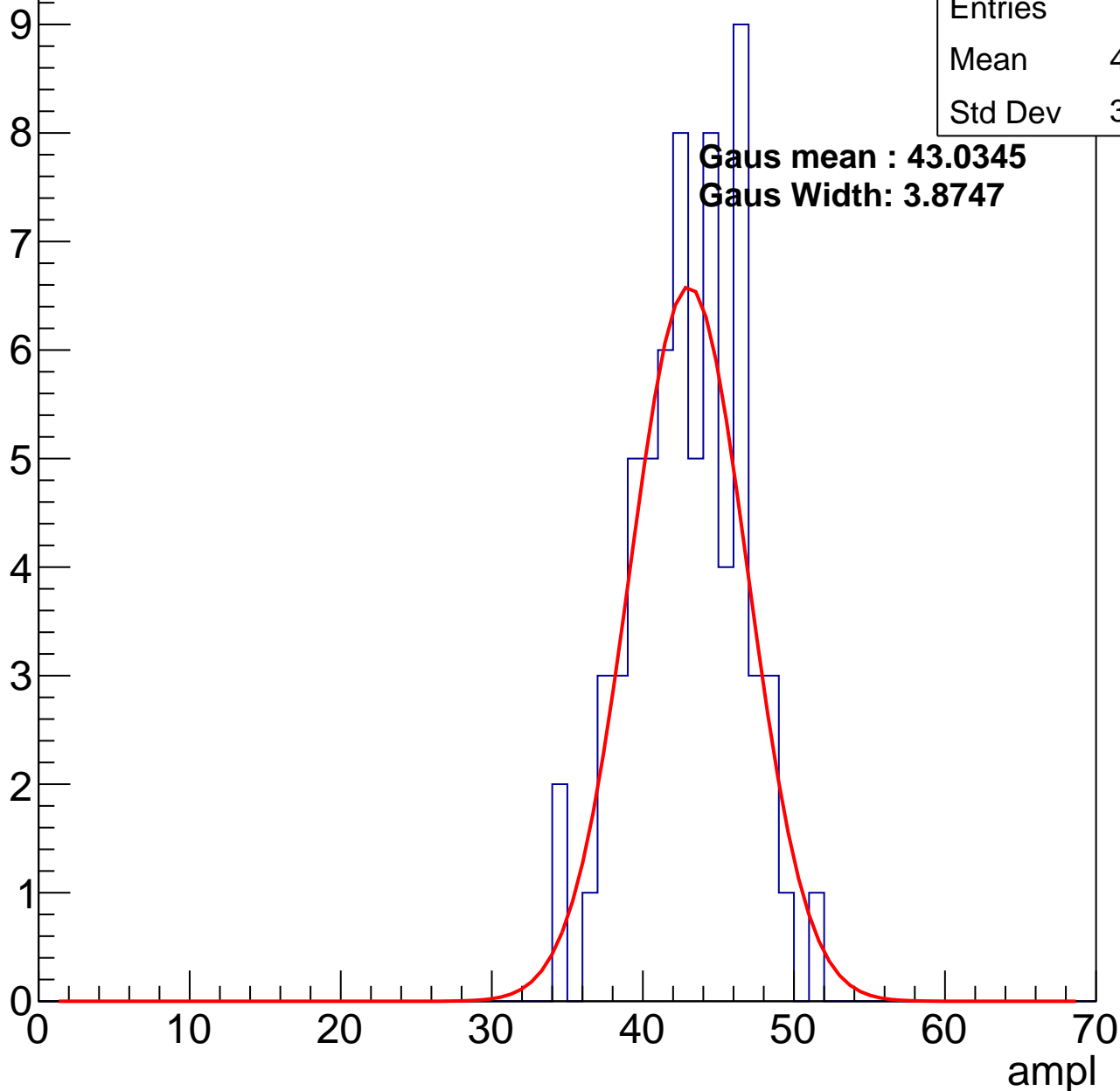
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	42.57
Std Dev	3.596

**Gaus mean : 43.0345**

**Gaus Width: 3.8747**

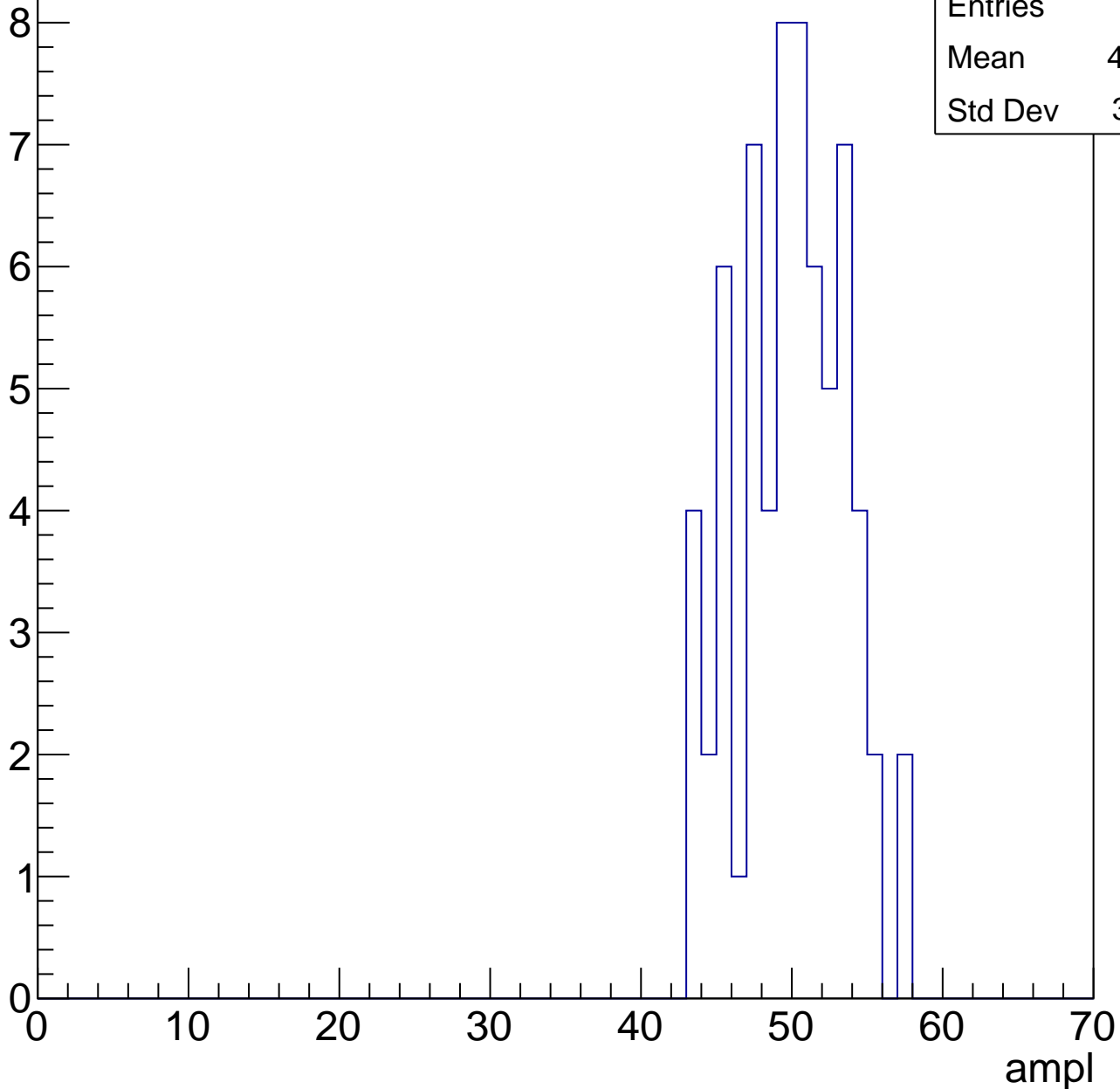


# B1L102S, U8-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	49.48
Std Dev	3.491

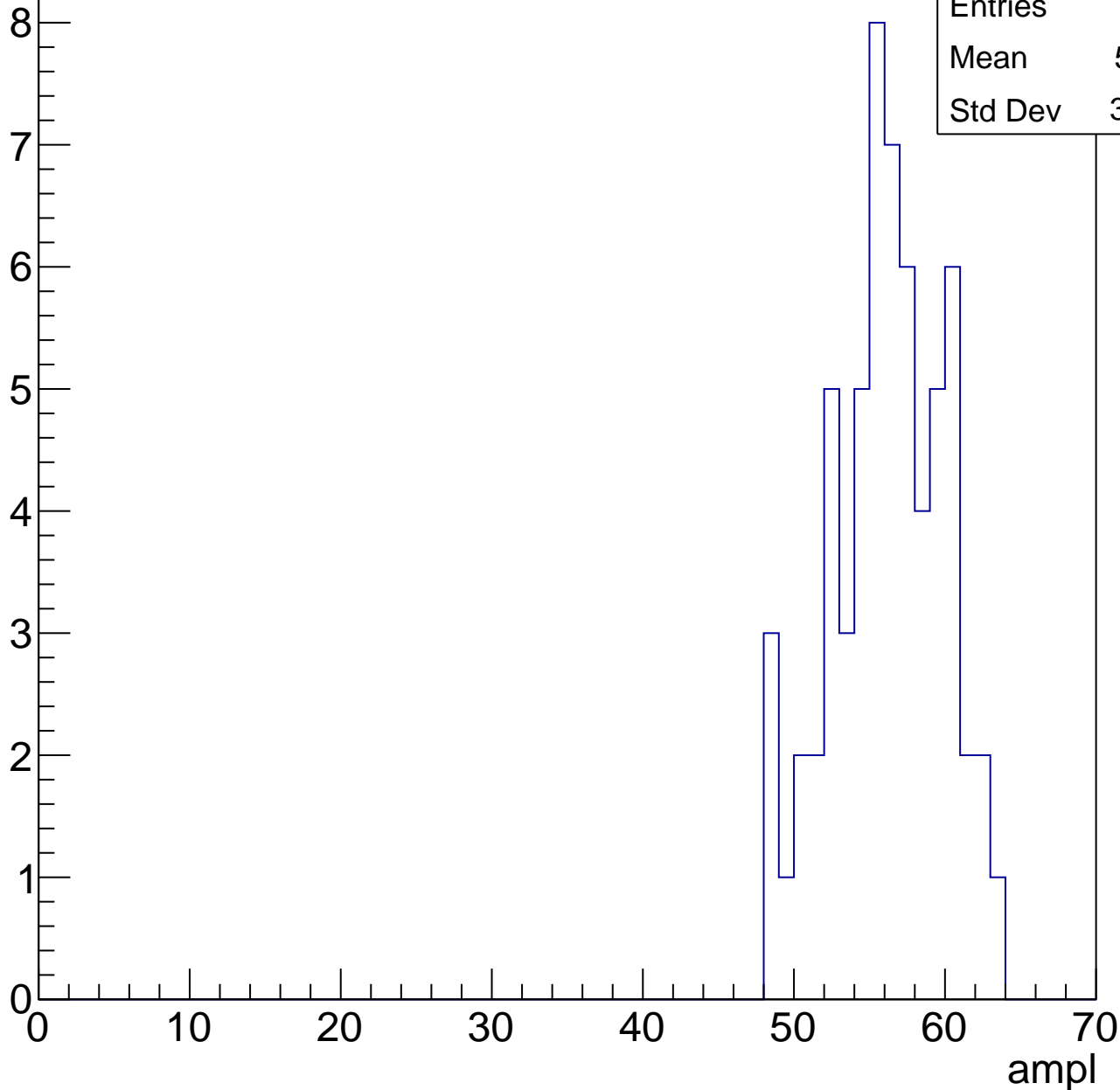


# B1L102S, U8-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	55.71
Std Dev	3.652

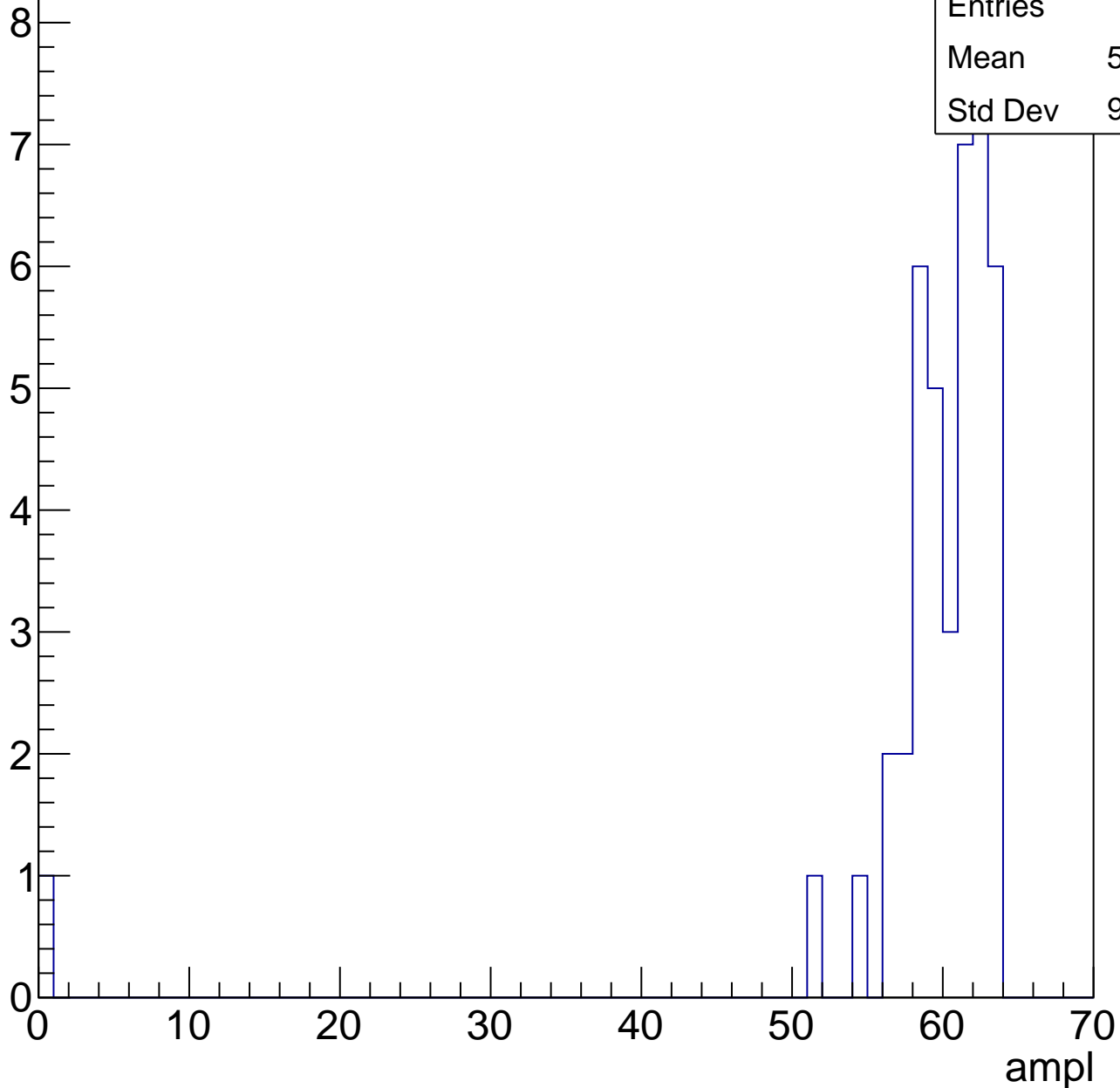


# B1L102S, U8-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

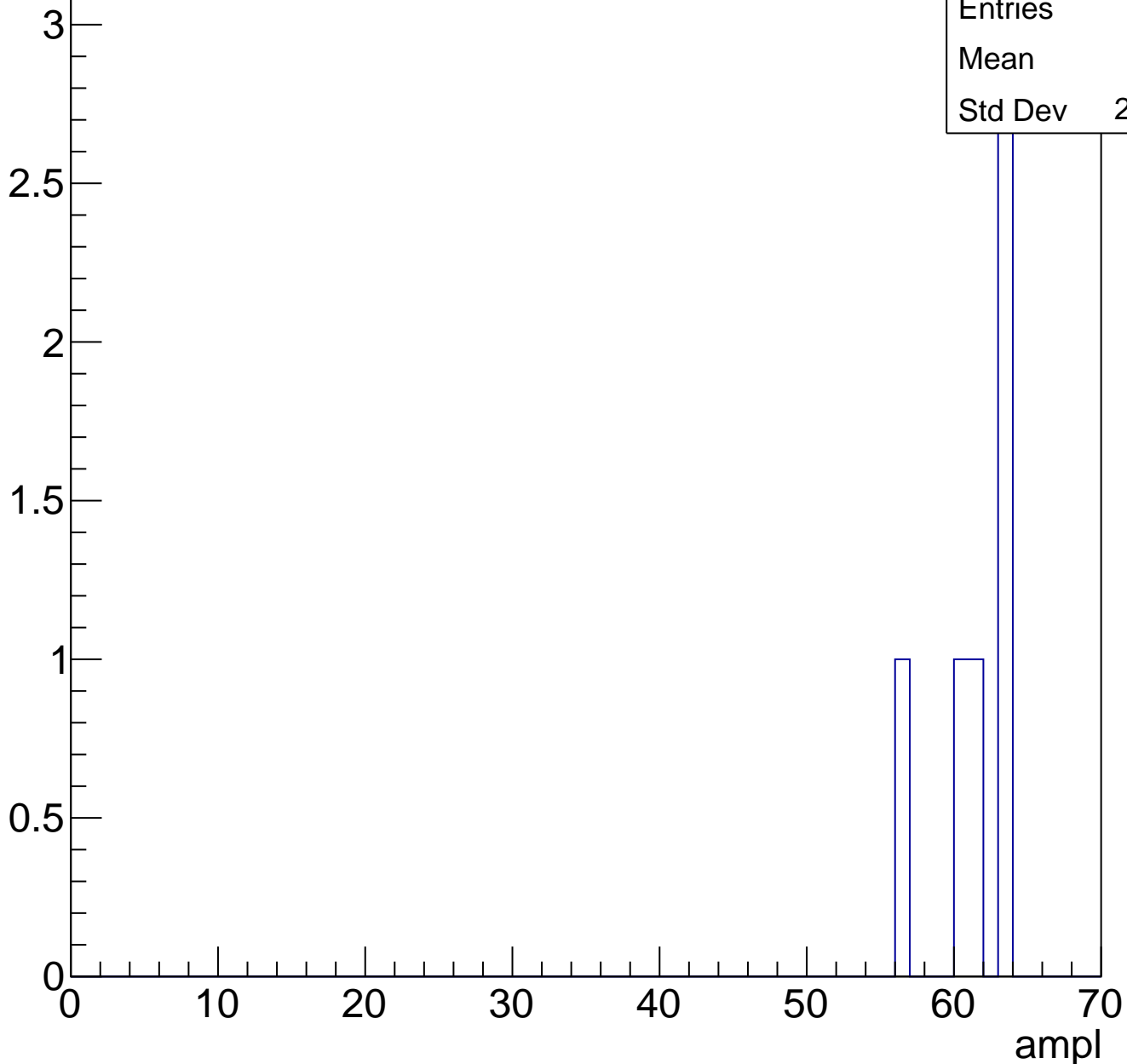
Entries	42
Mean	58.45
Std Dev	9.497



# B1L102S, U8-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U8-ch8, adc0

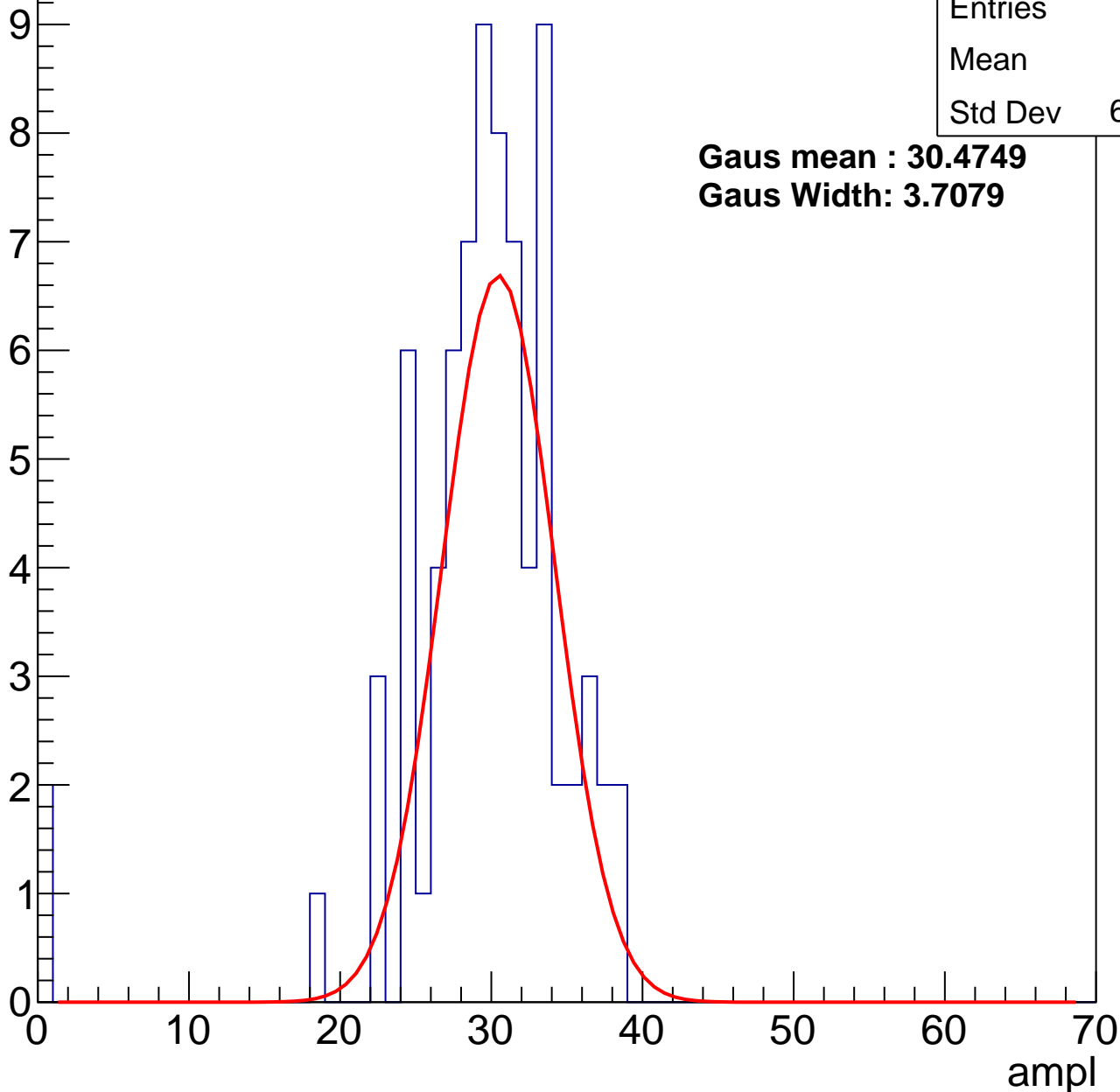
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	28.9
Std Dev	6.157

**Gaus mean : 30.4749**

**Gaus Width: 3.7079**



# B1L102S, U8-ch8, adc1

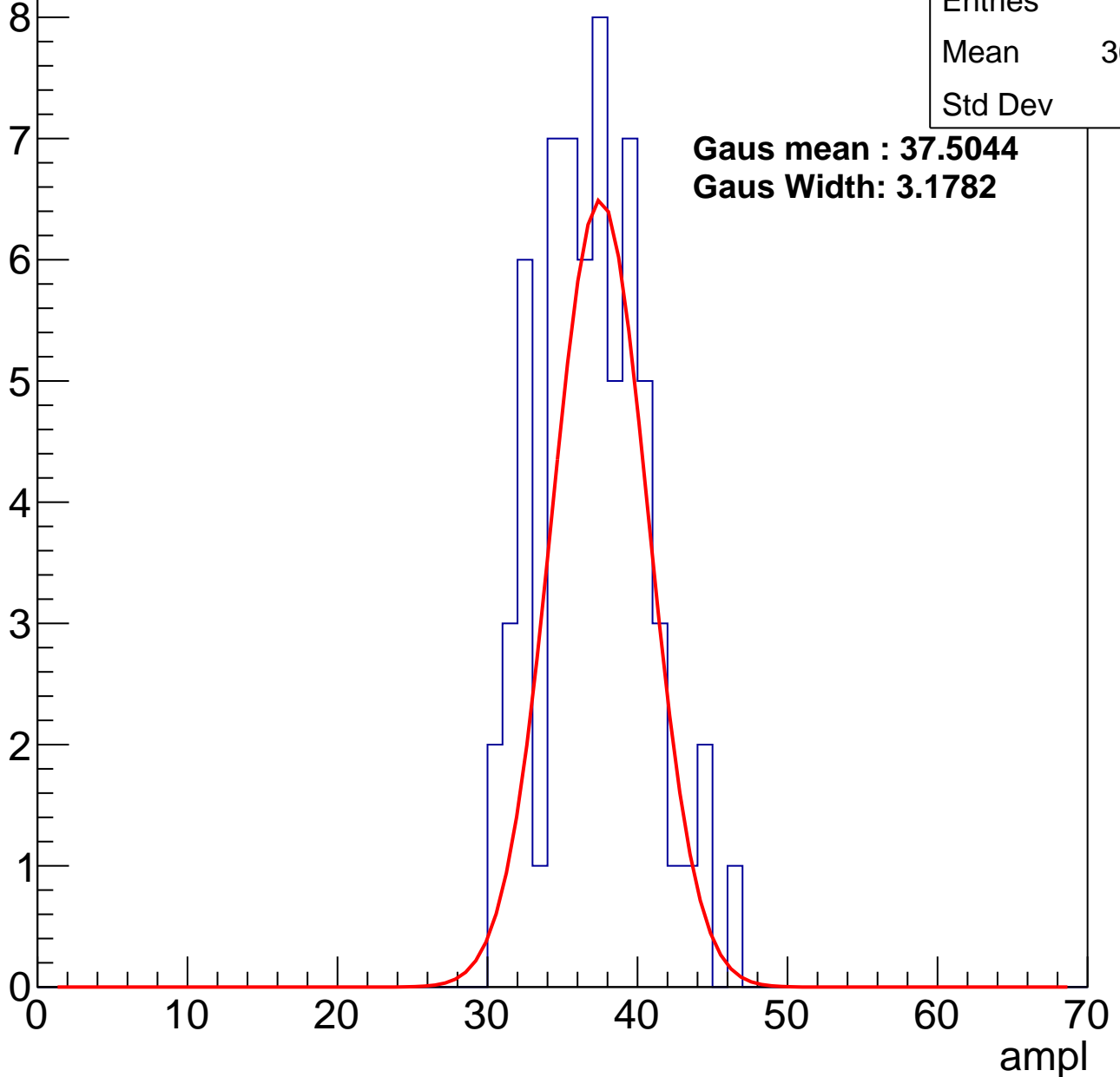
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	36.58
Std Dev	3.56

**Gaus mean : 37.5044**

**Gaus Width: 3.1782**



# B1L102S, U8-ch8, adc2

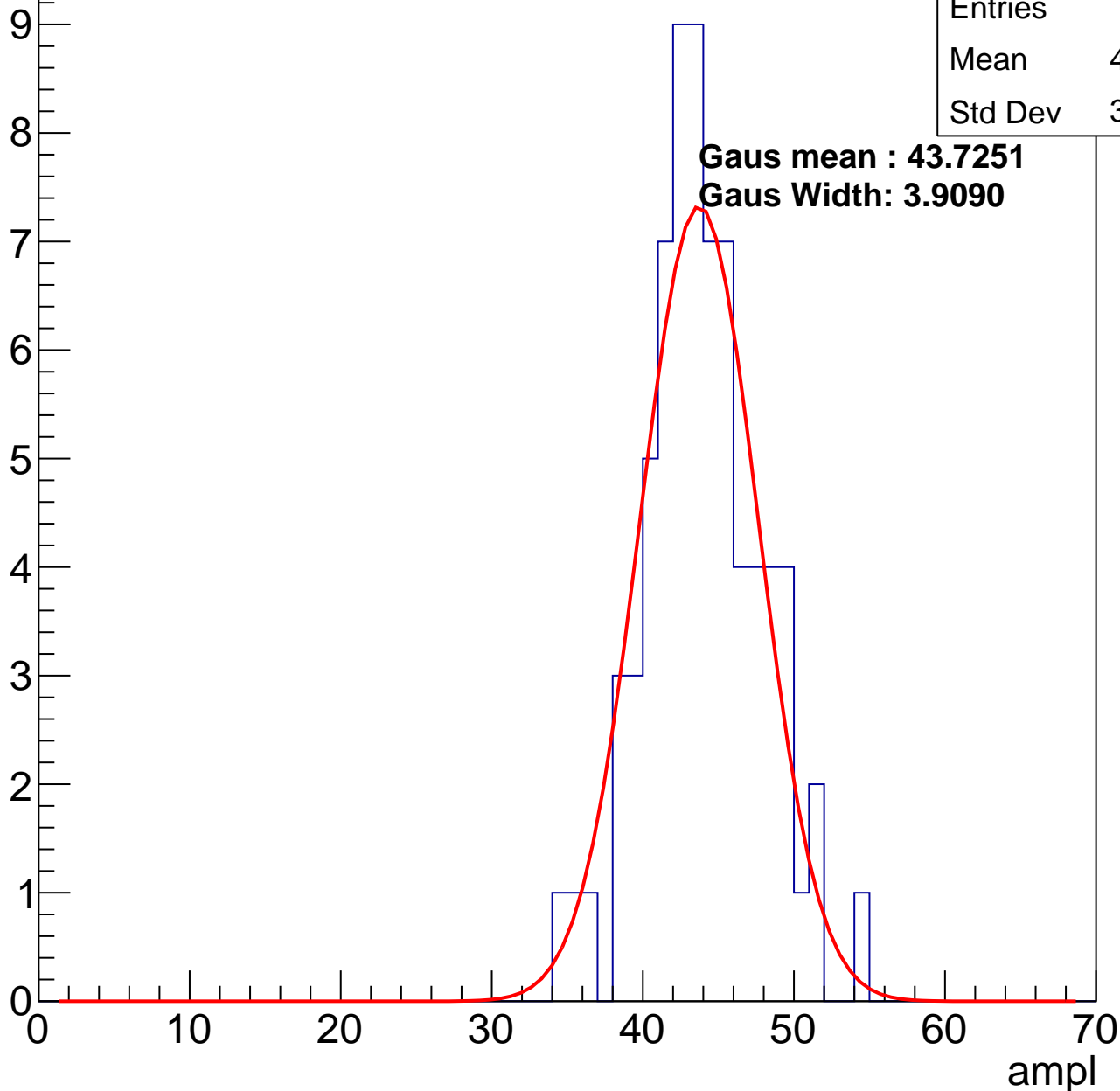
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	43.52
Std Dev	3.804

**Gaus mean : 43.7251**

**Gaus Width: 3.9090**

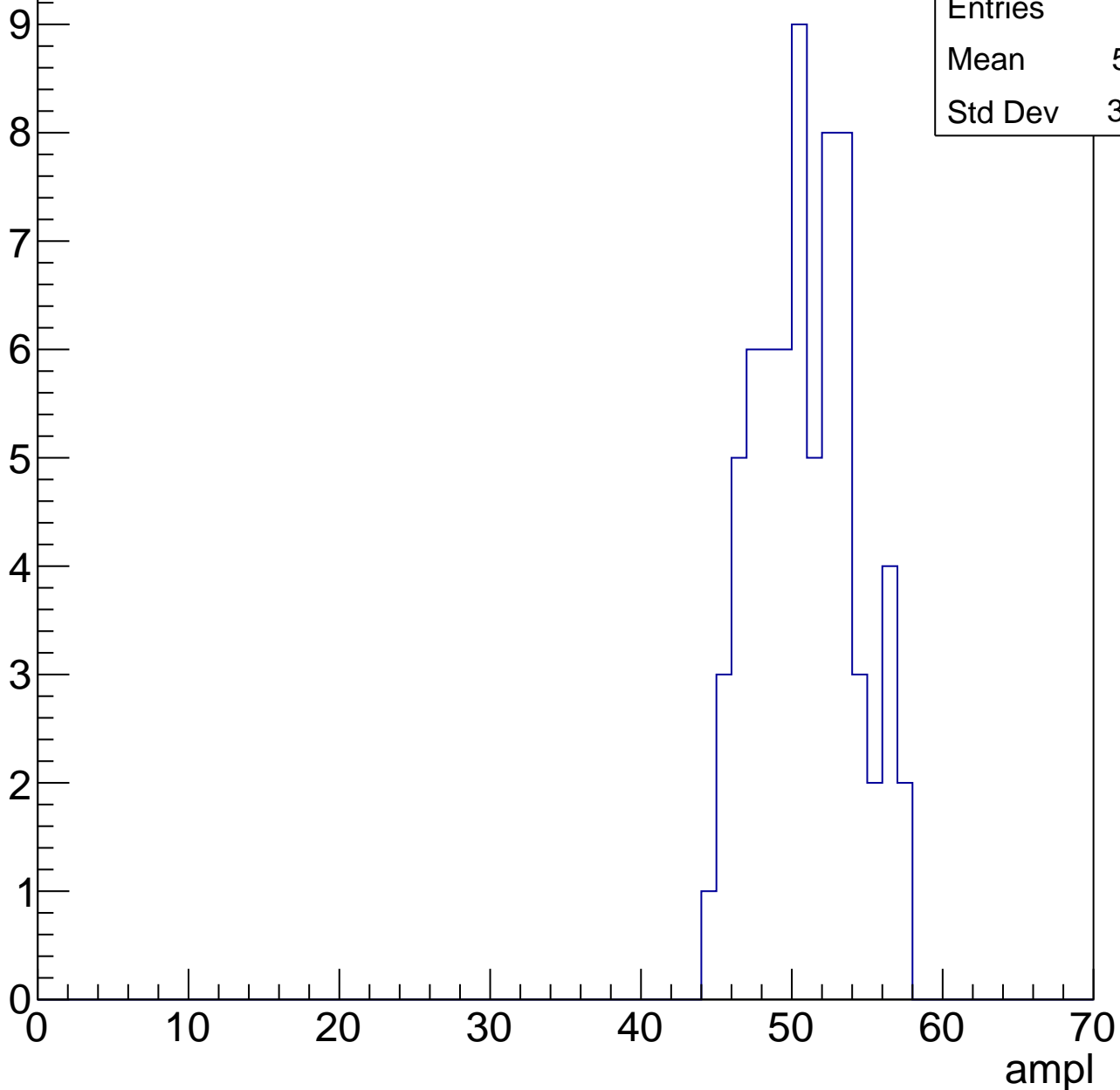


# B1L102S, U8-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	50.41
Std Dev	3.237

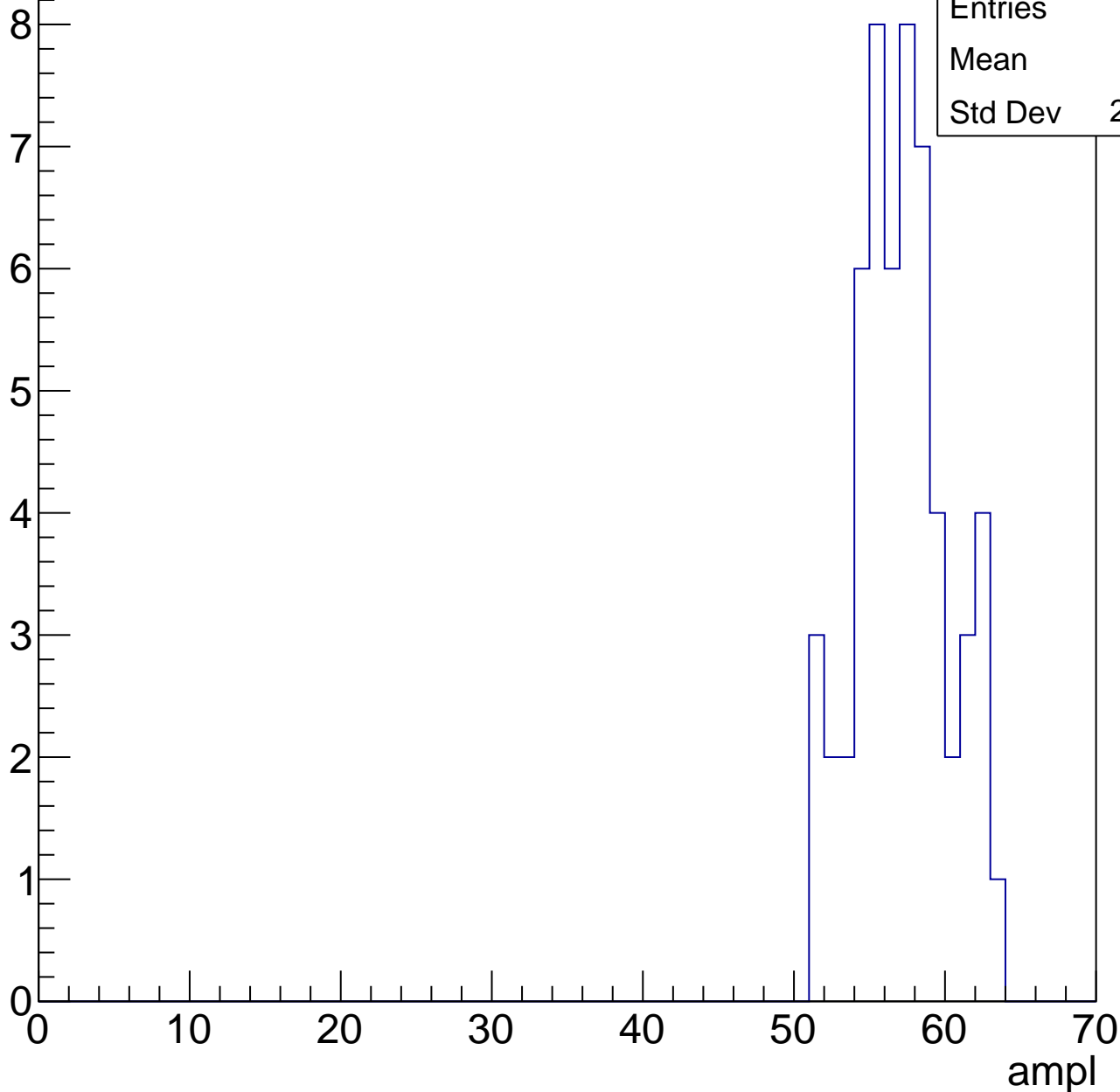


# B1L102S, U8-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

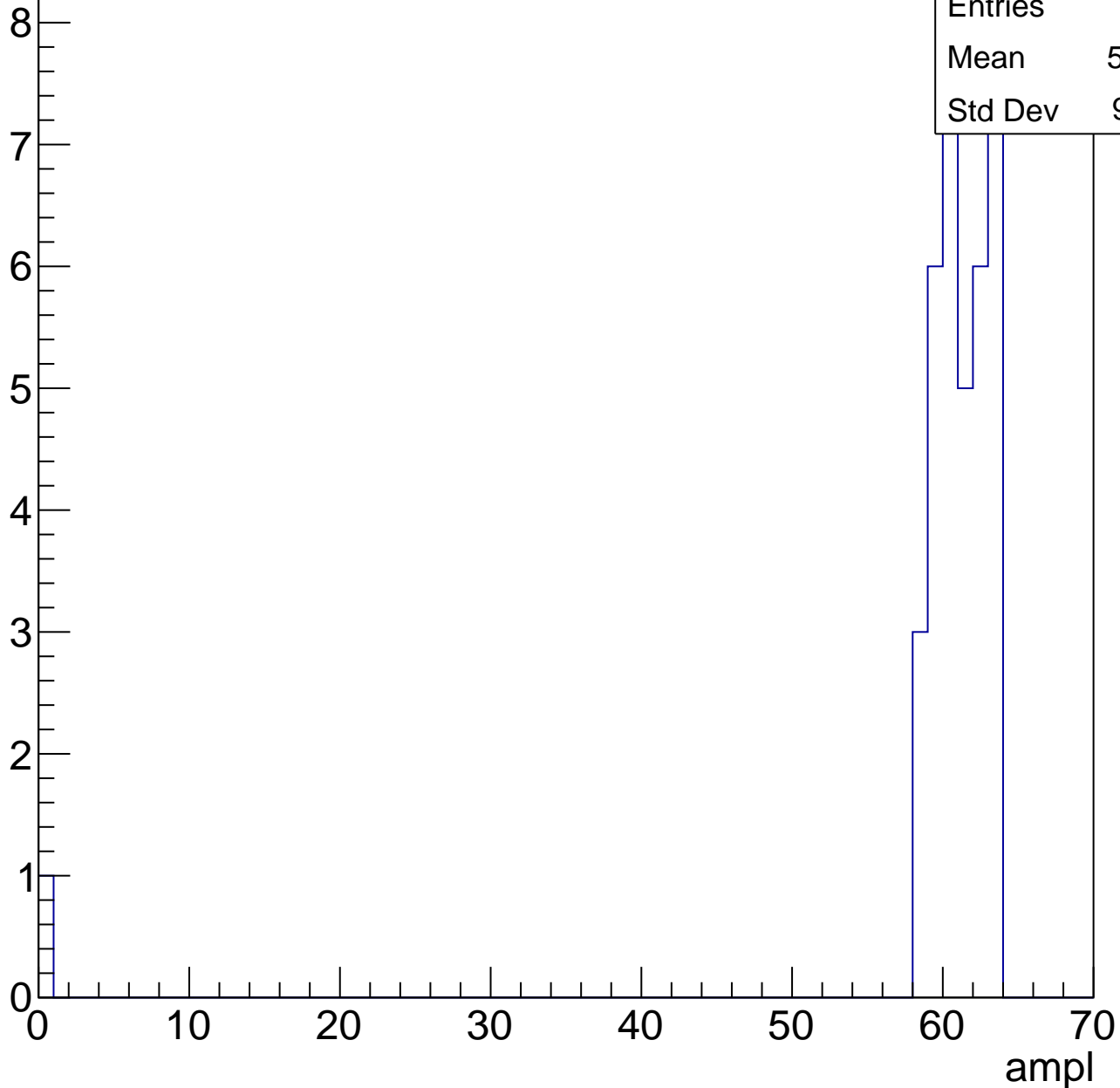
Entries	56
Mean	56.7
Std Dev	2.994



# B1L102S, U8-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	61.67
Std Dev	0.9428

ampl

0 10 20 30 40 50 60 70



# B1L102S, U8-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

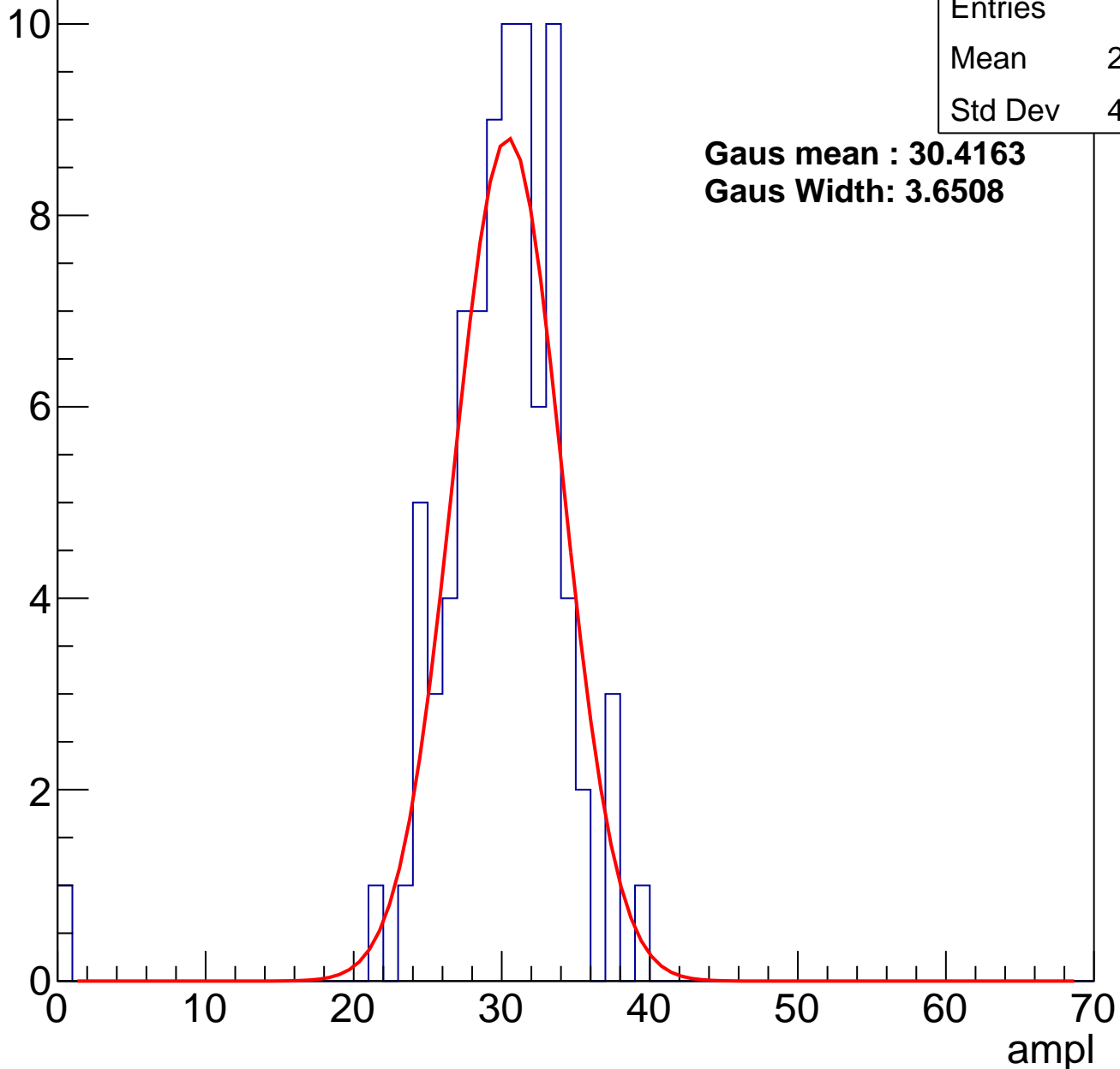
# B1L102S, U8-ch9, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	84
Mean	29.49
Std Dev	4.747

**Gaus mean : 30.4163**  
**Gaus Width: 3.6508**

Entry



# B1L102S, U8-ch9, adc1

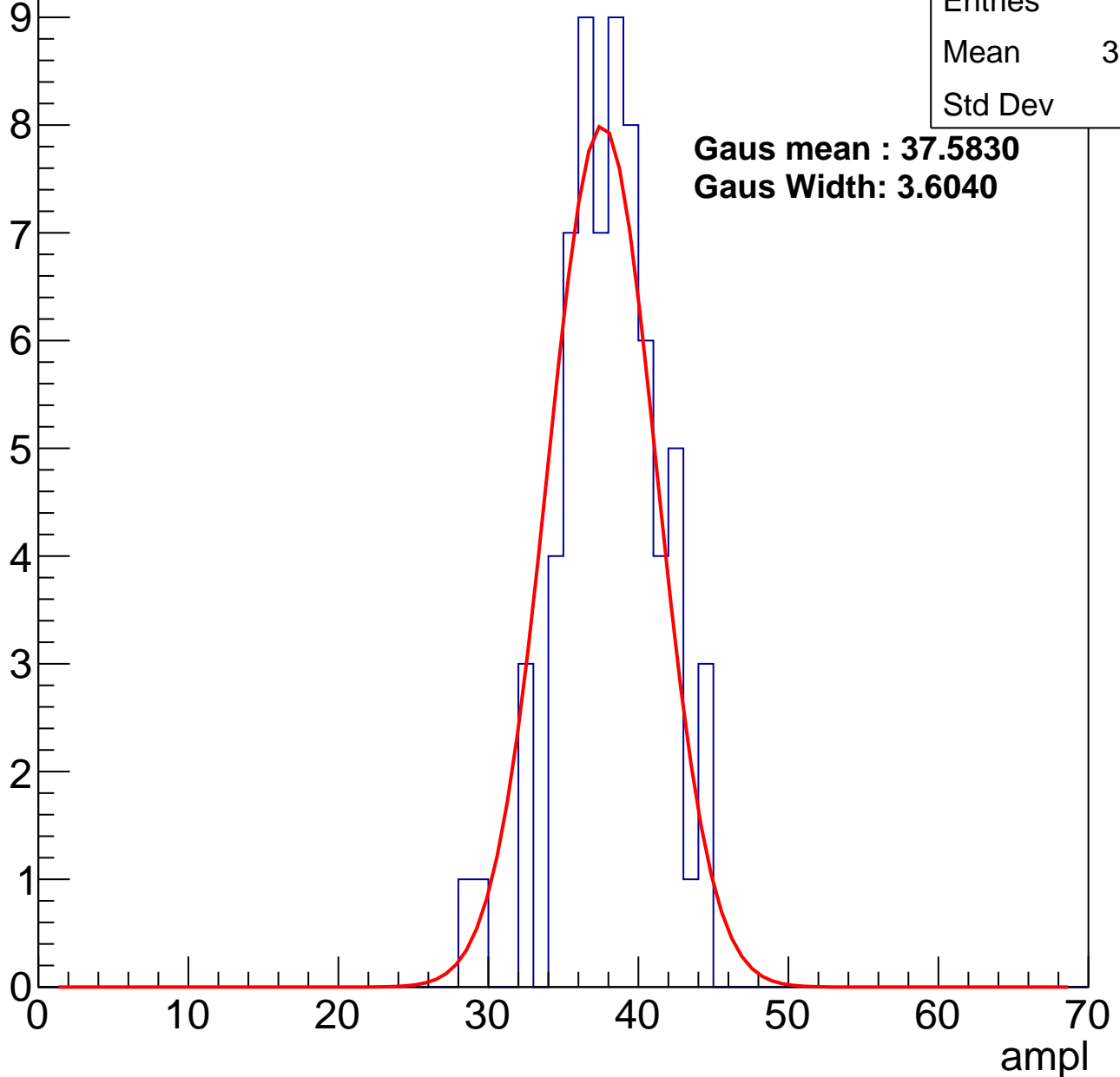
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	37.65
Std Dev	3.28

**Gaus mean : 37.5830**

**Gaus Width: 3.6040**



# B1L102S, U8-ch9, adc2

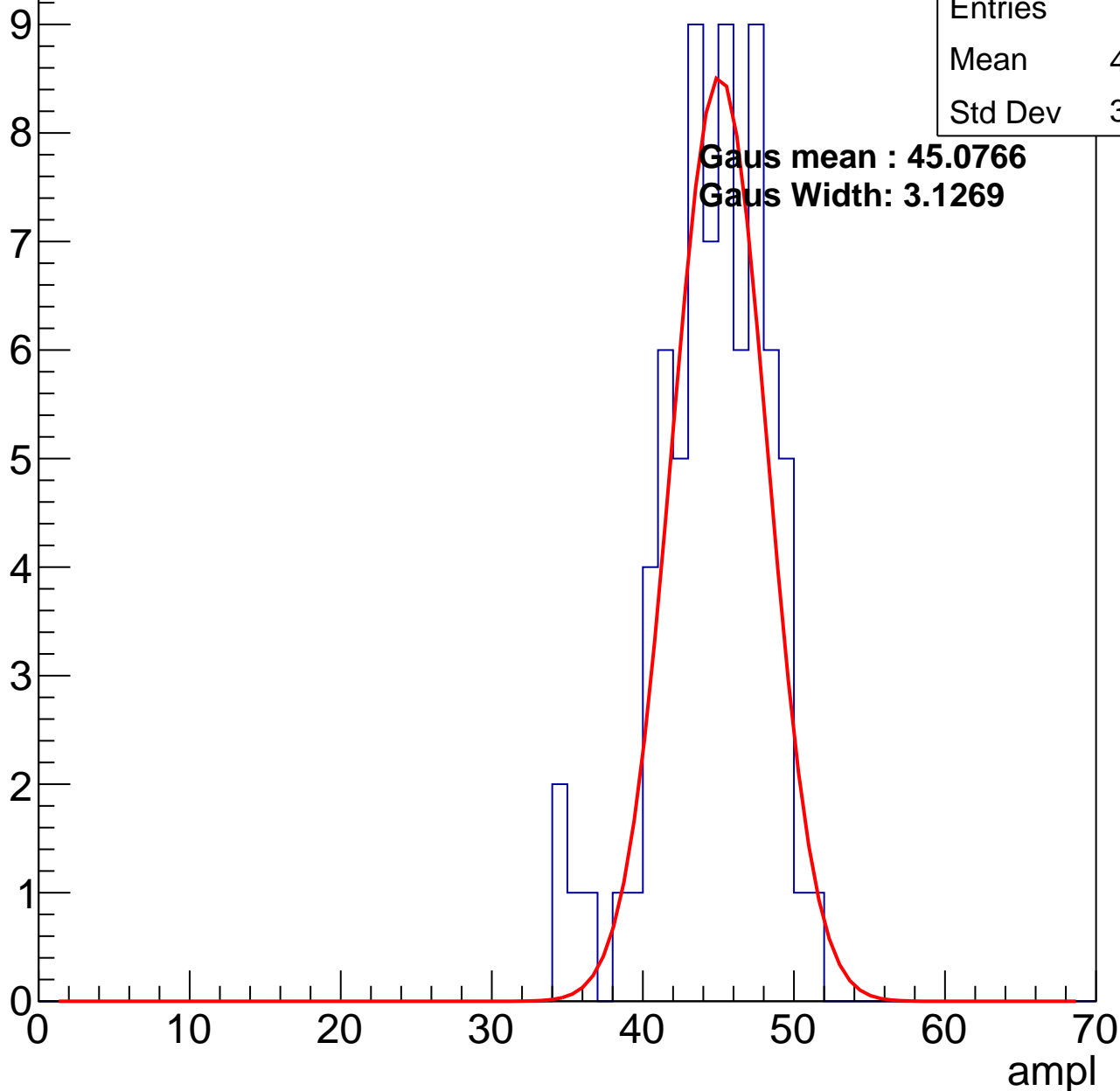
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	44.12
Std Dev	3.624

**Gaus mean : 45.0766**

**Gaus Width: 3.1269**

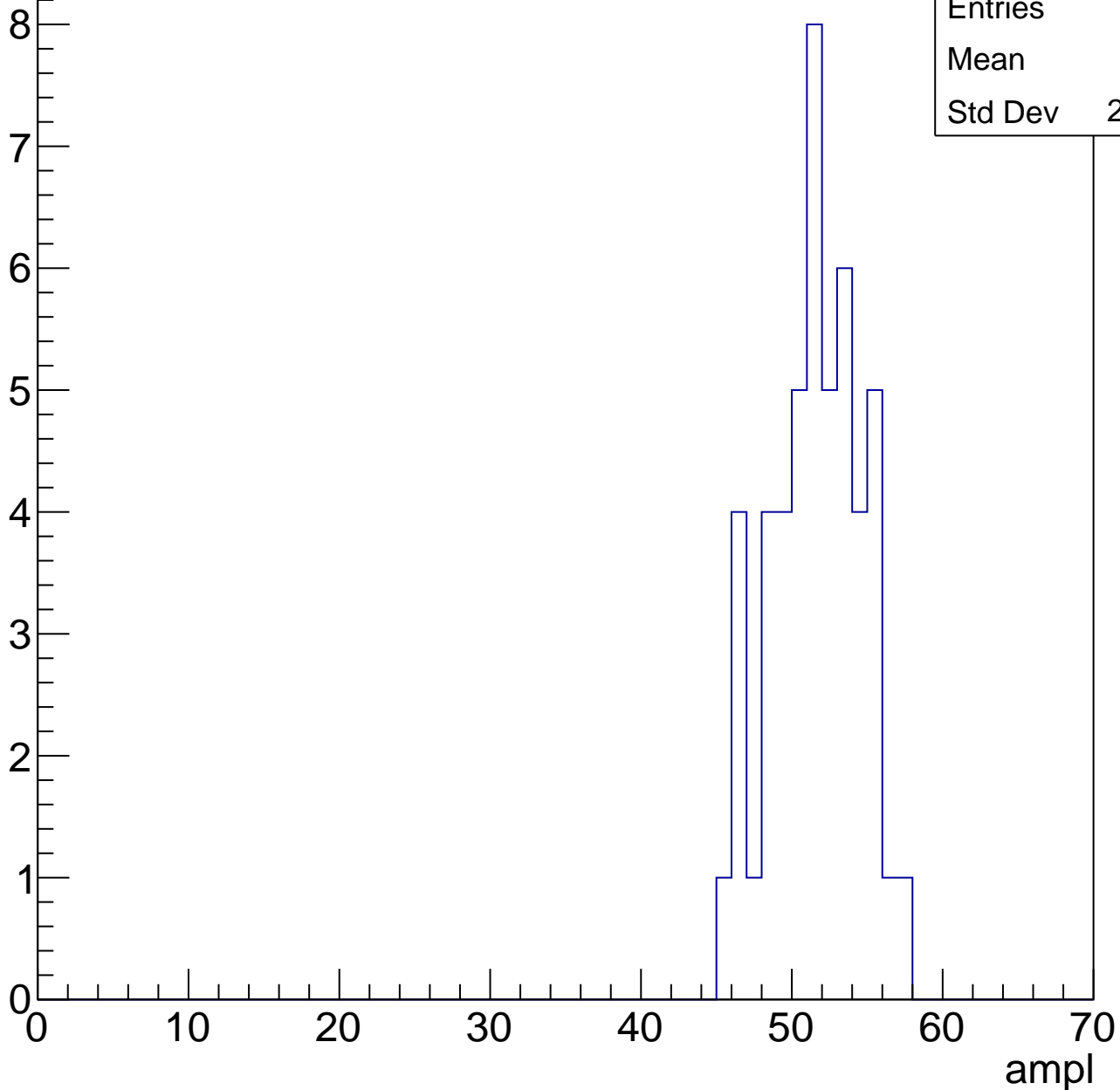


# B1L102S, U8-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	51.1
Std Dev	2.908

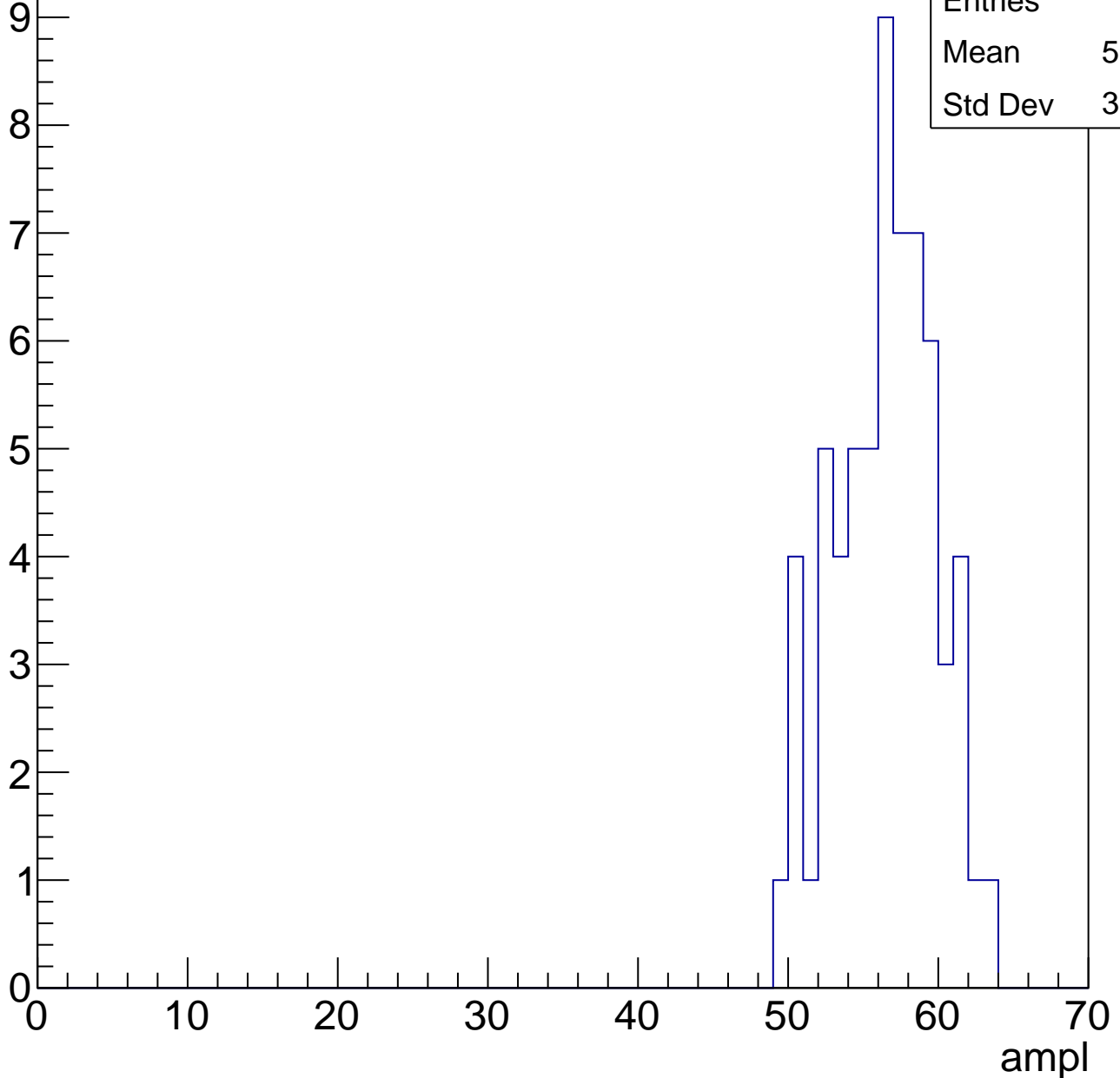


# B1L102S, U8-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	56.02
Std Dev	3.288

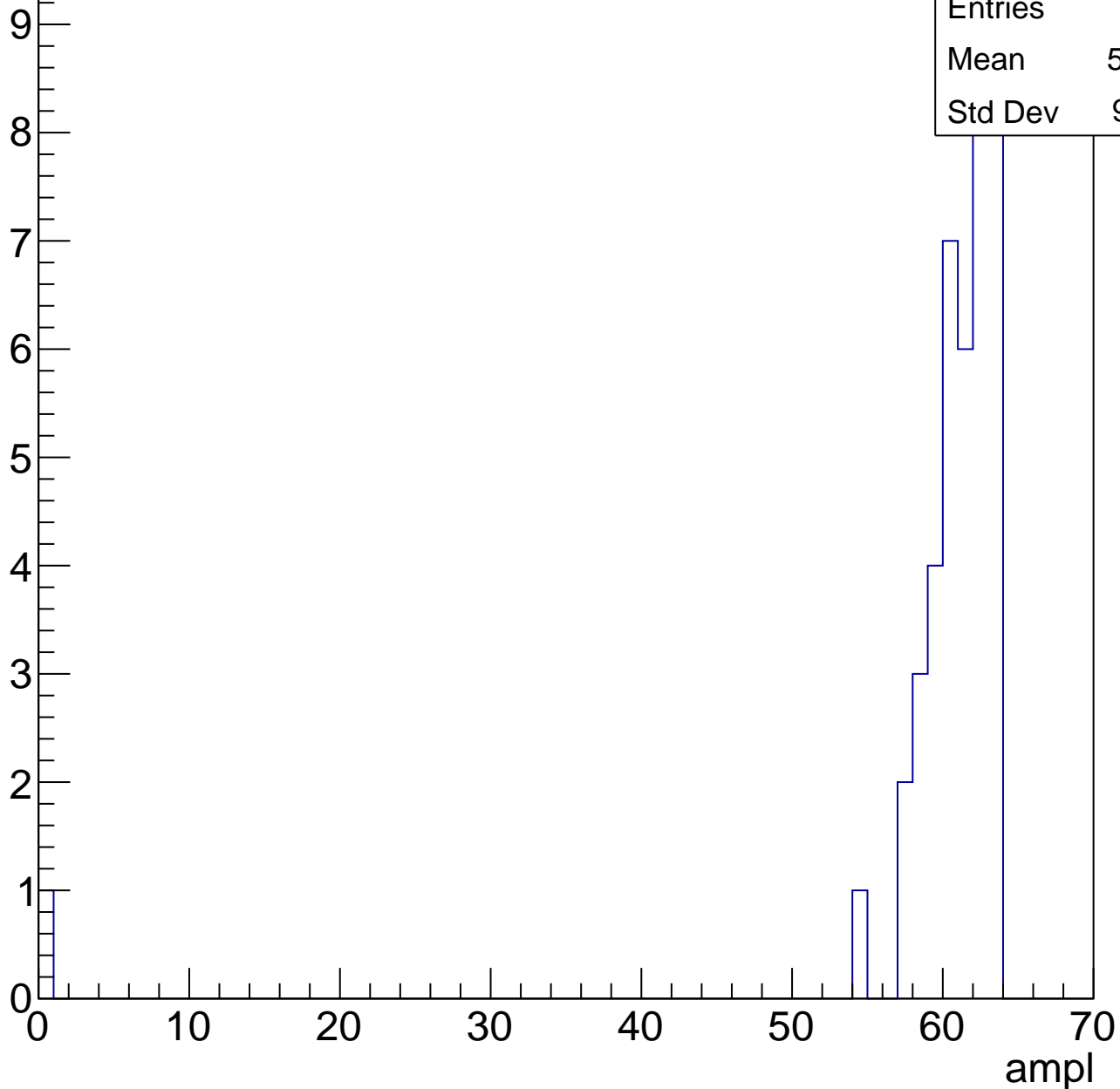


# B1L102S, U8-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	41
Mean	59.17
Std Dev	9.571



# B1L102S, U8-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch10, adc0

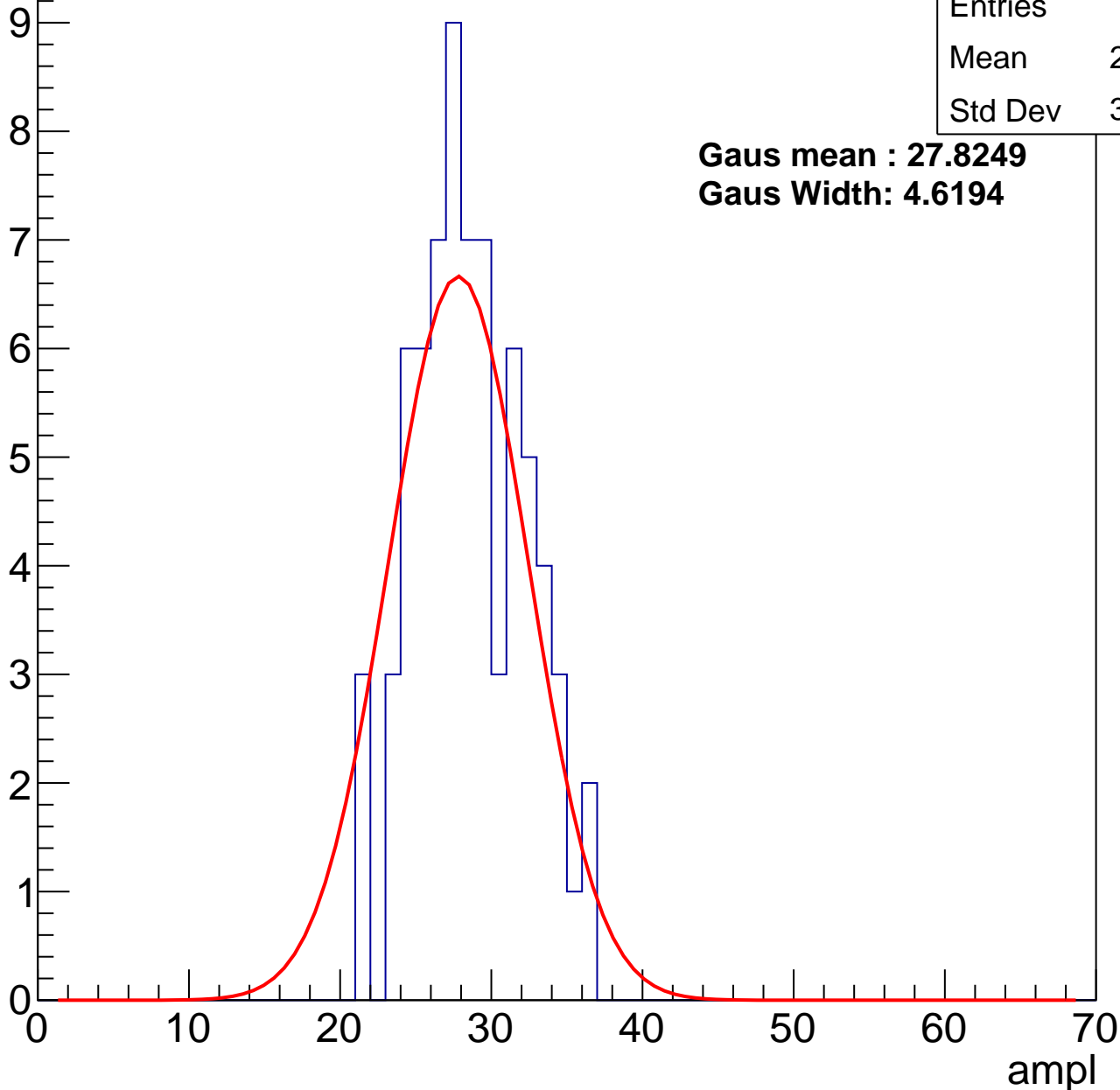
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	28.15
Std Dev	3.623

**Gaus mean : 27.8249**

**Gaus Width: 4.6194**



# B1L102S, U8-ch10, adc1

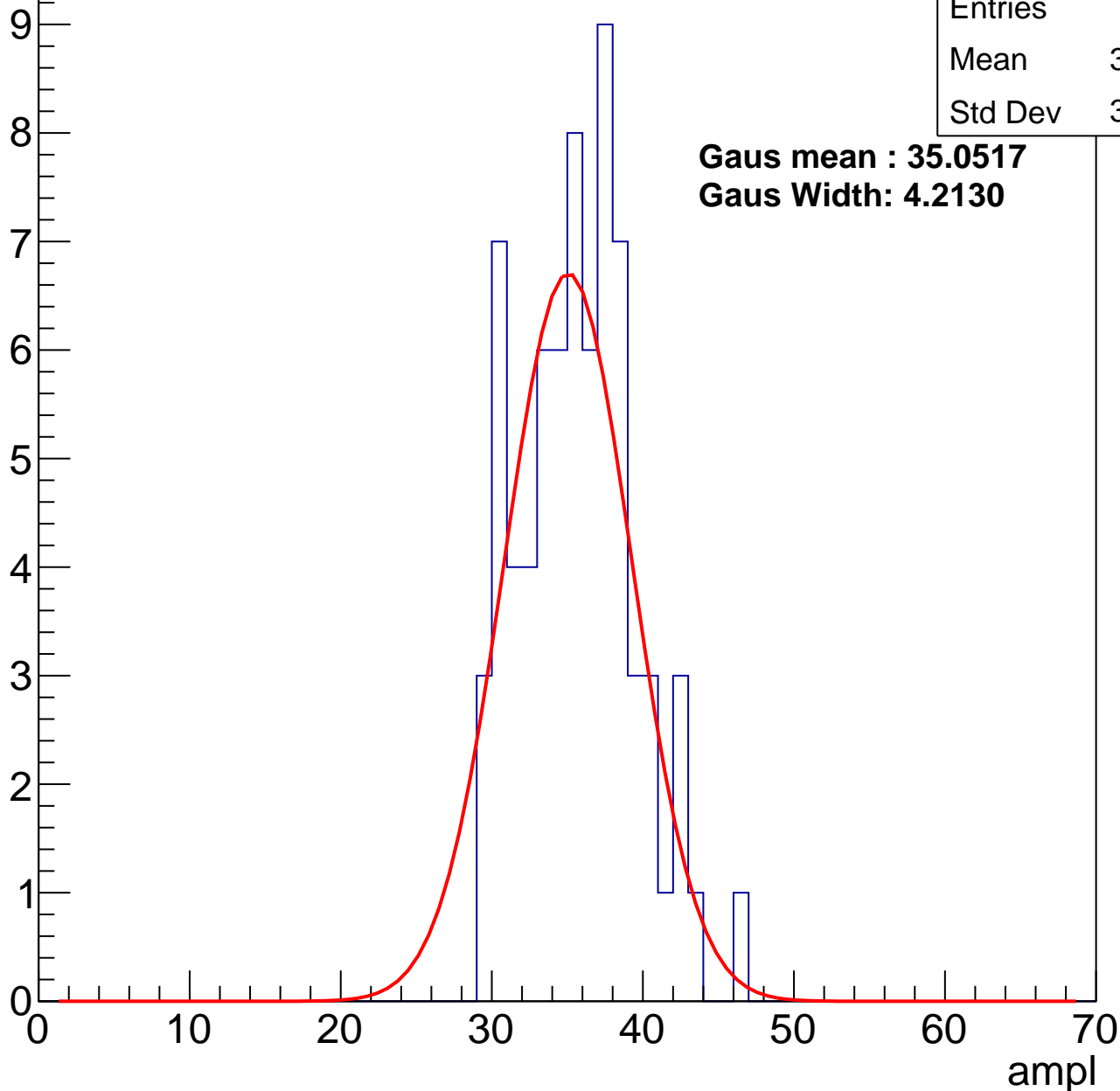
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	35.26
Std Dev	3.734

**Gaus mean : 35.0517**

**Gaus Width: 4.2130**



# B1L102S, U8-ch10, adc2

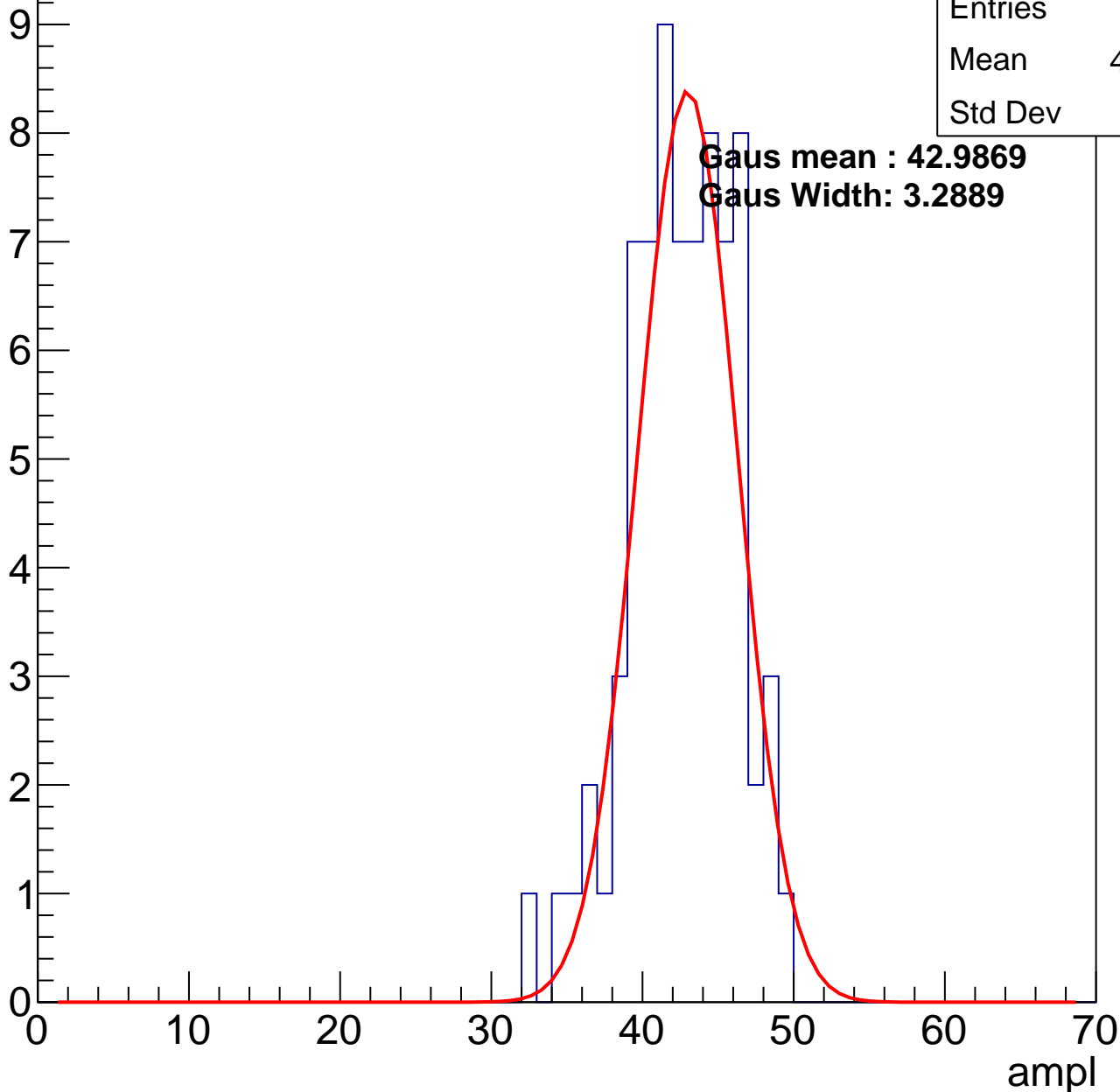
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	42.17
Std Dev	3.45

**Gaus mean : 42.9869**

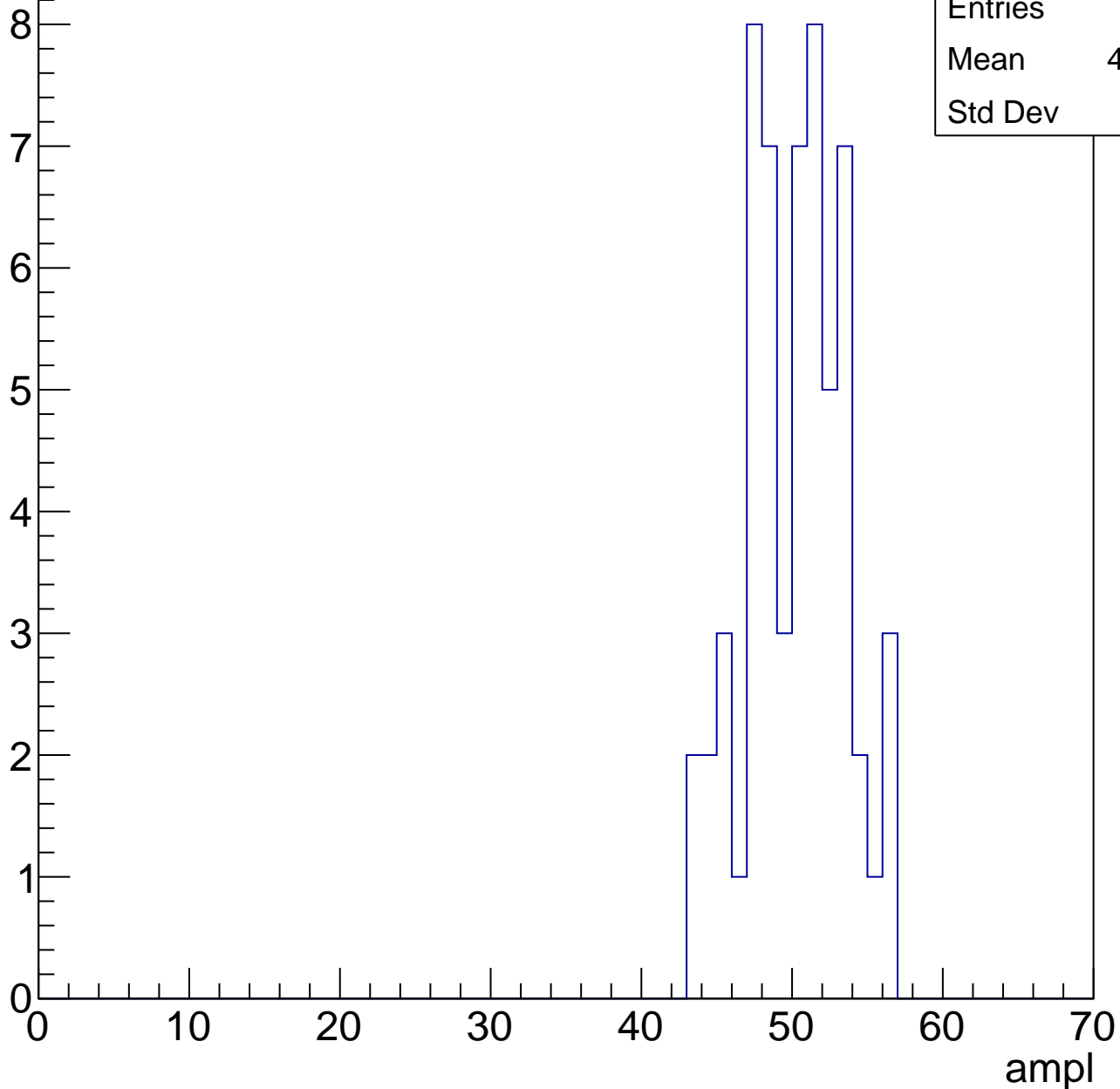
**Gaus Width: 3.2889**



# B1L102S, U8-ch10, adc3

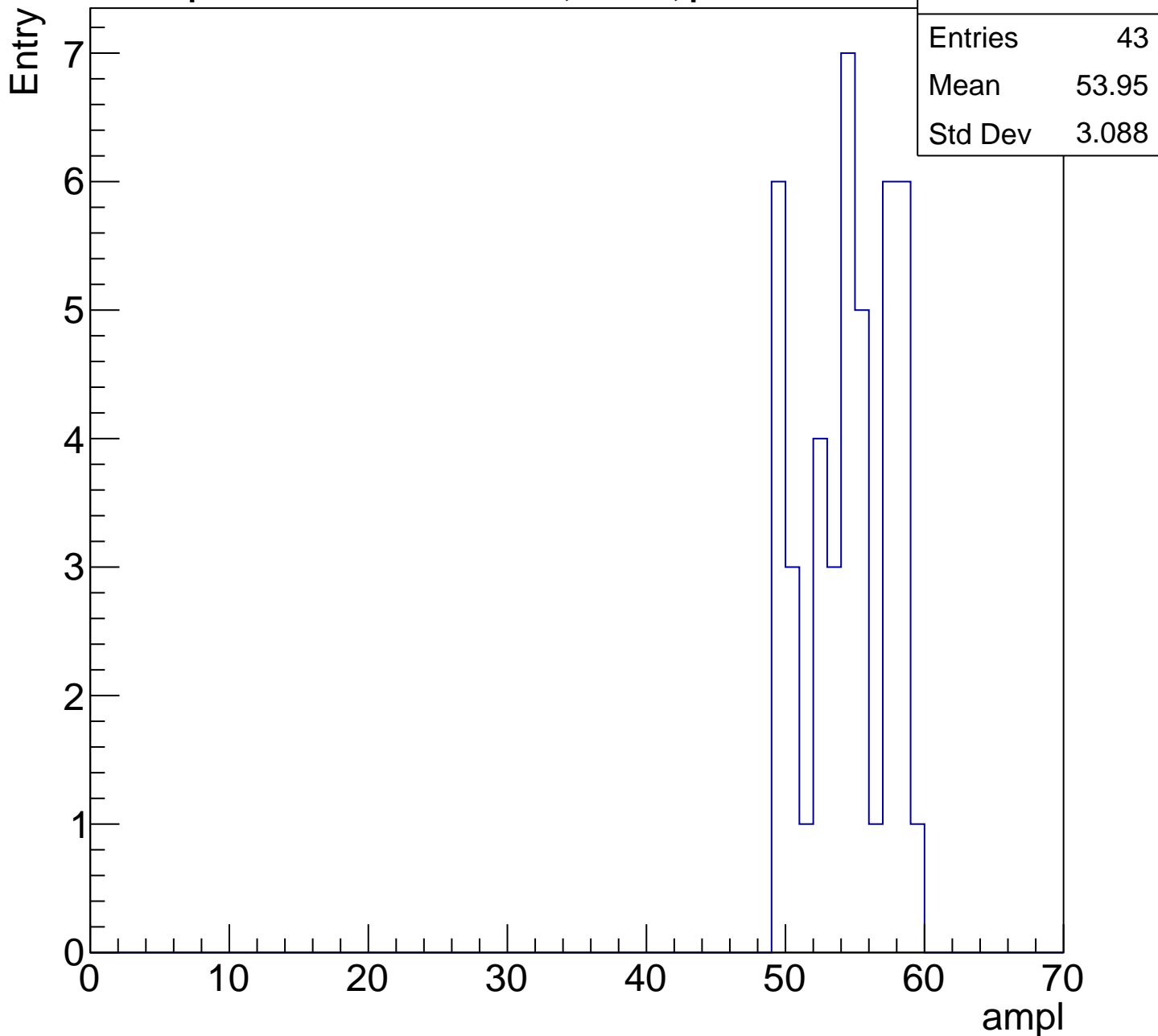
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



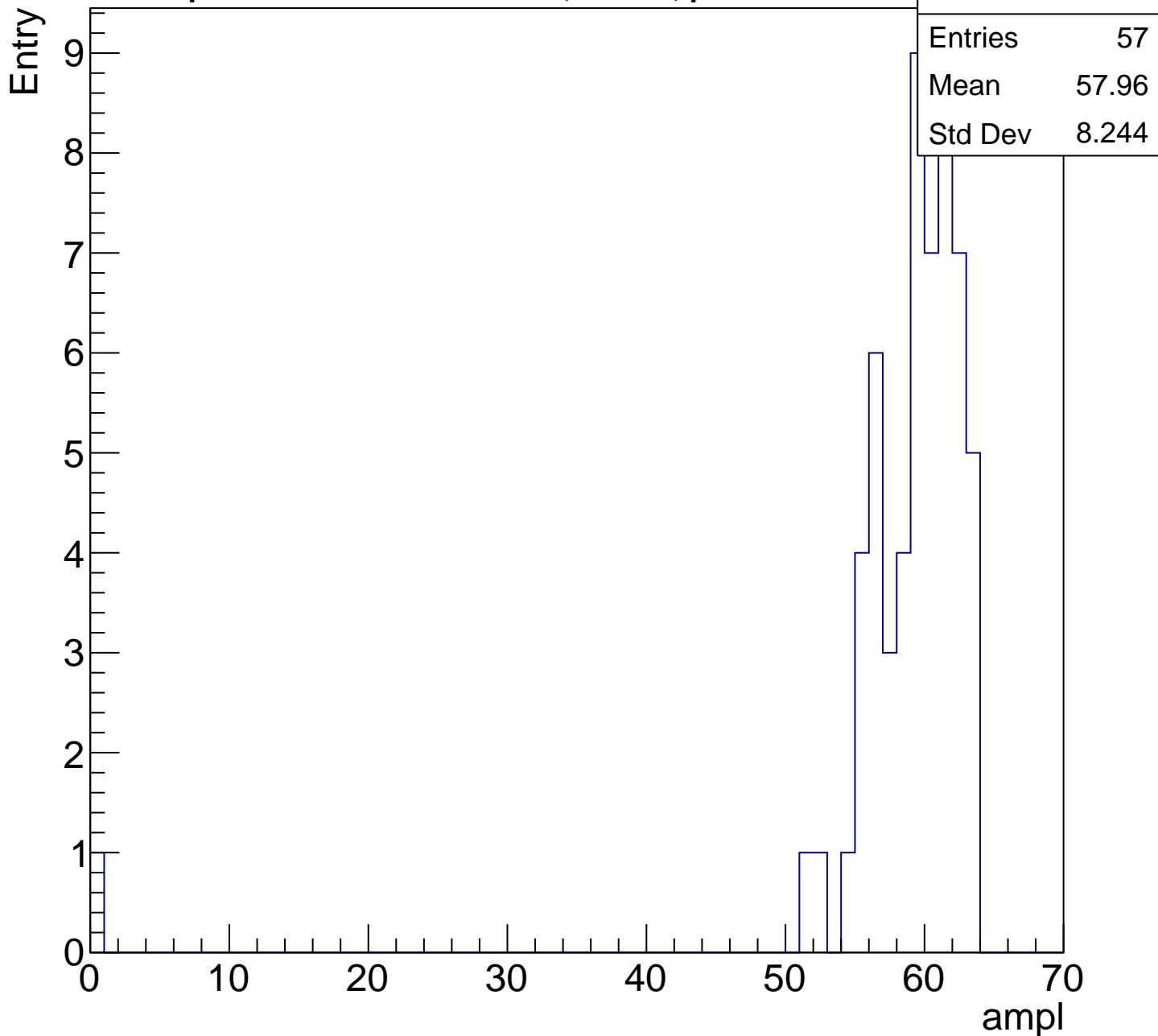
# B1L102S, U8-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U8-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

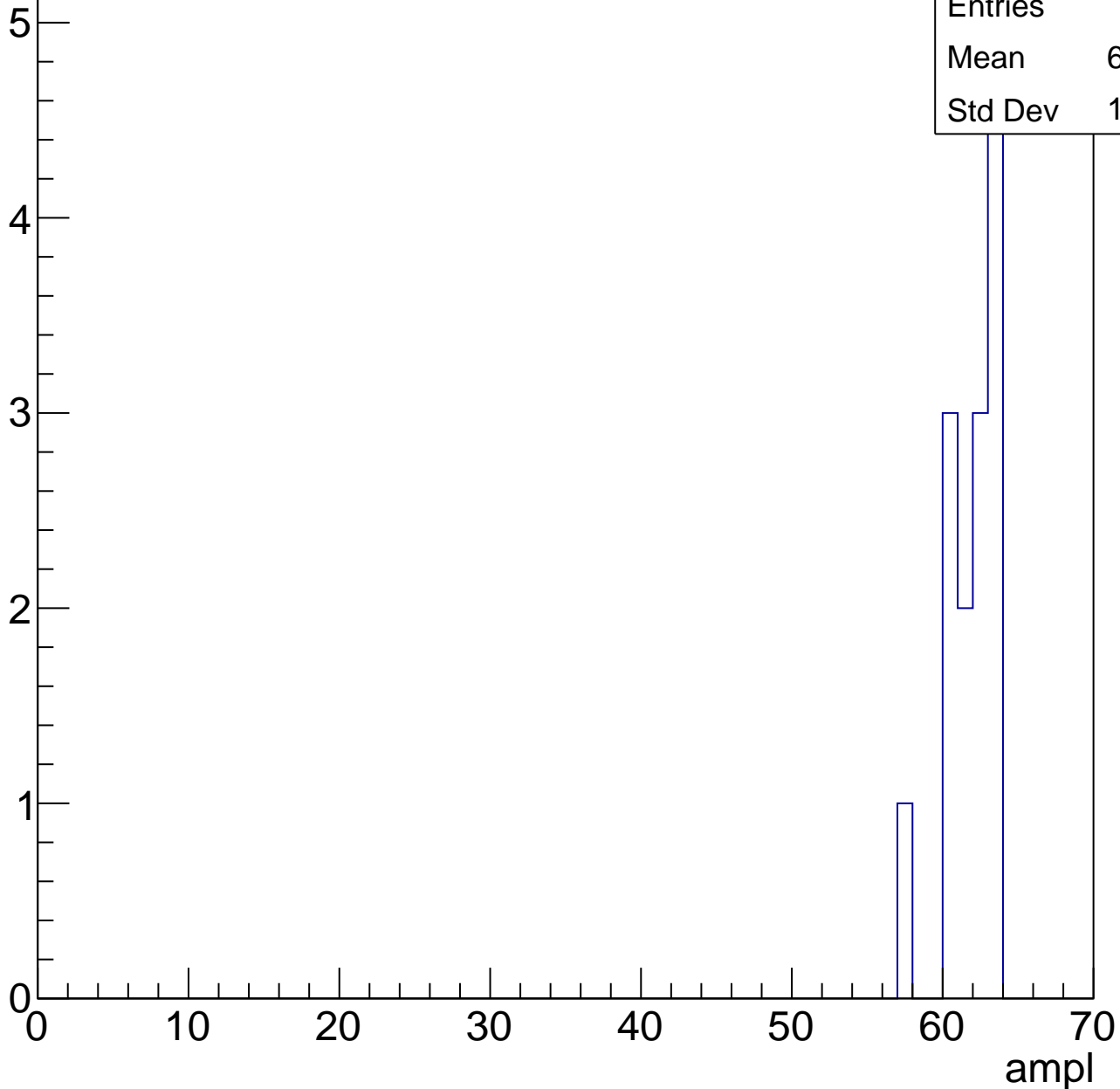


# B1L102S, U8-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	14
Mean	61.43
Std Dev	1.678





# B1L102S, U8-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch11, adc0

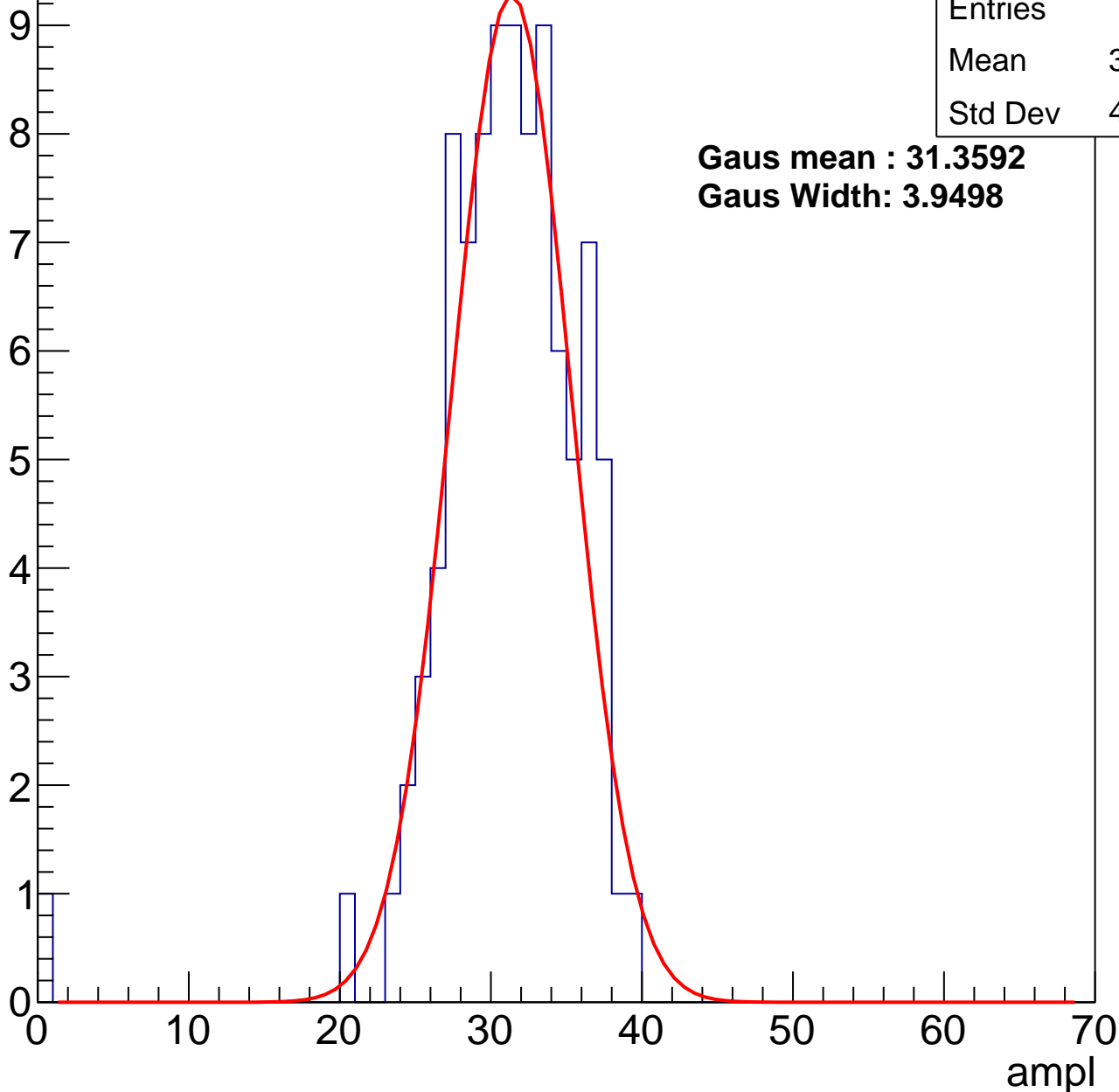
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	95
Mean	30.62
Std Dev	4.938

**Gaus mean : 31.3592**

**Gaus Width: 3.9498**



# B1L102S, U8-ch11, adc1

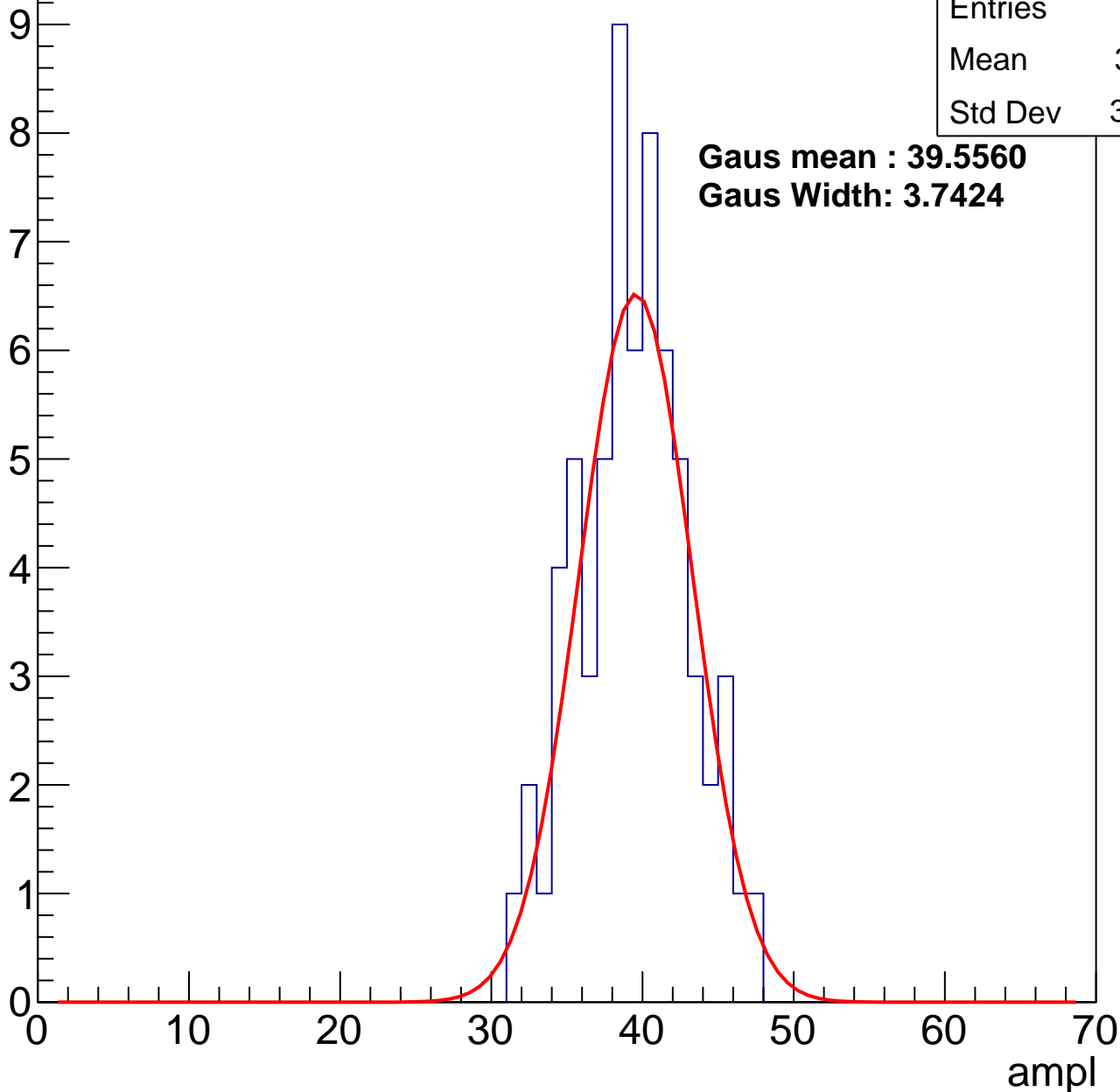
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	38.91
Std Dev	3.572

**Gaus mean : 39.5560**

**Gaus Width: 3.7424**



# B1L102S, U8-ch11, adc2

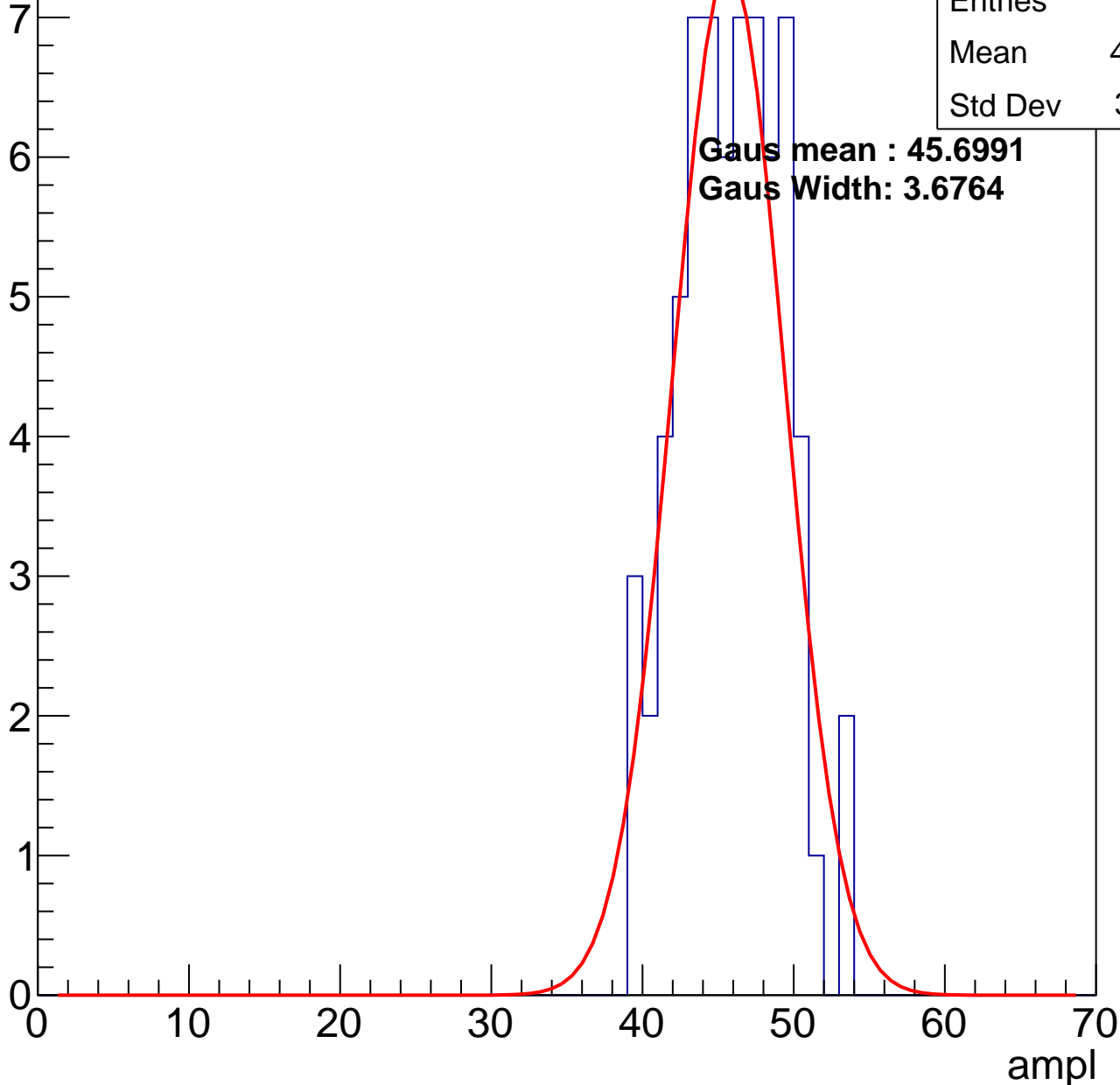
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	45.43
Std Dev	3.331

**Gaus mean : 45.6991**

**Gaus Width: 3.6764**

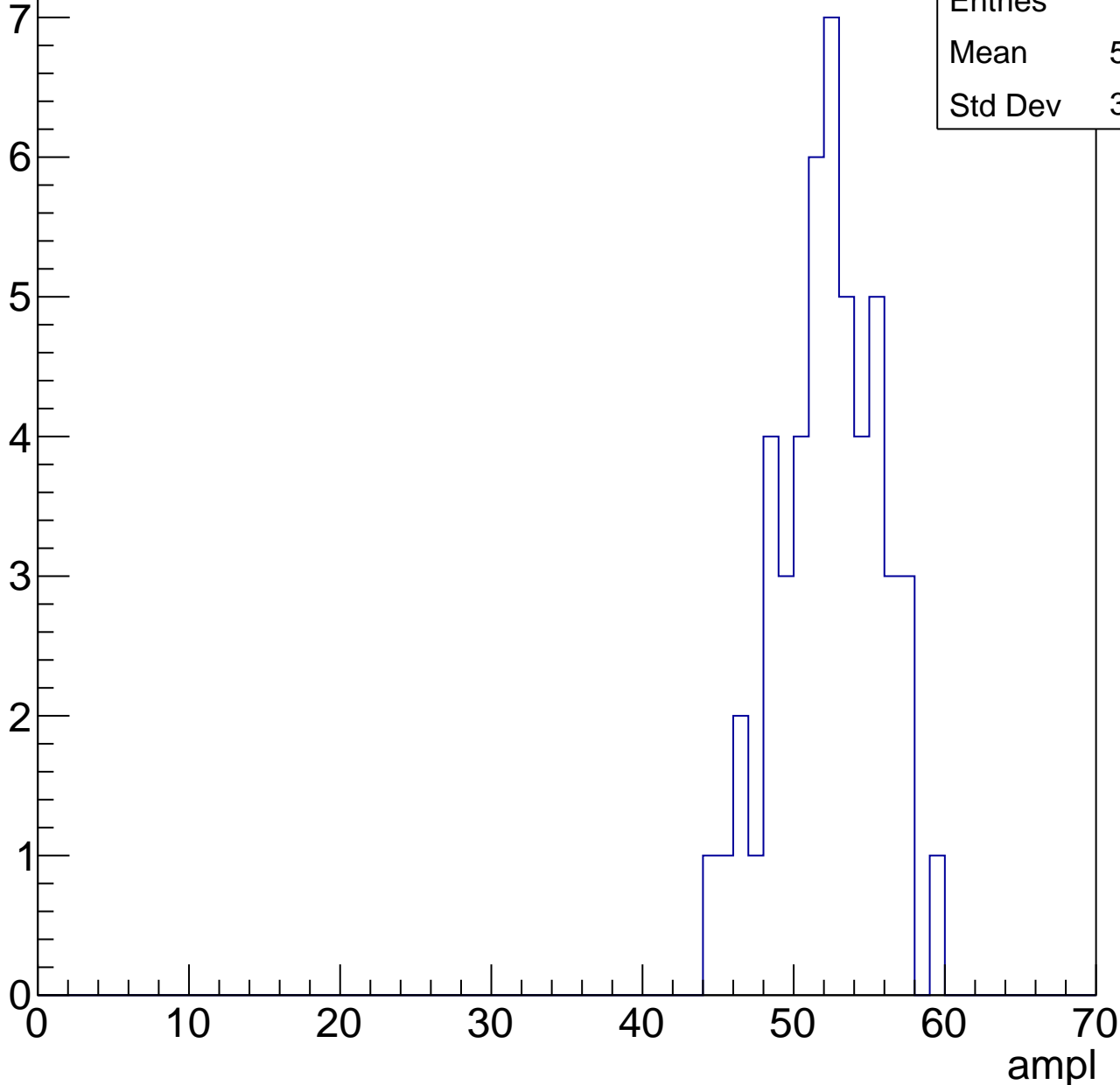


# B1L102S, U8-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	51.82
Std Dev	3.345

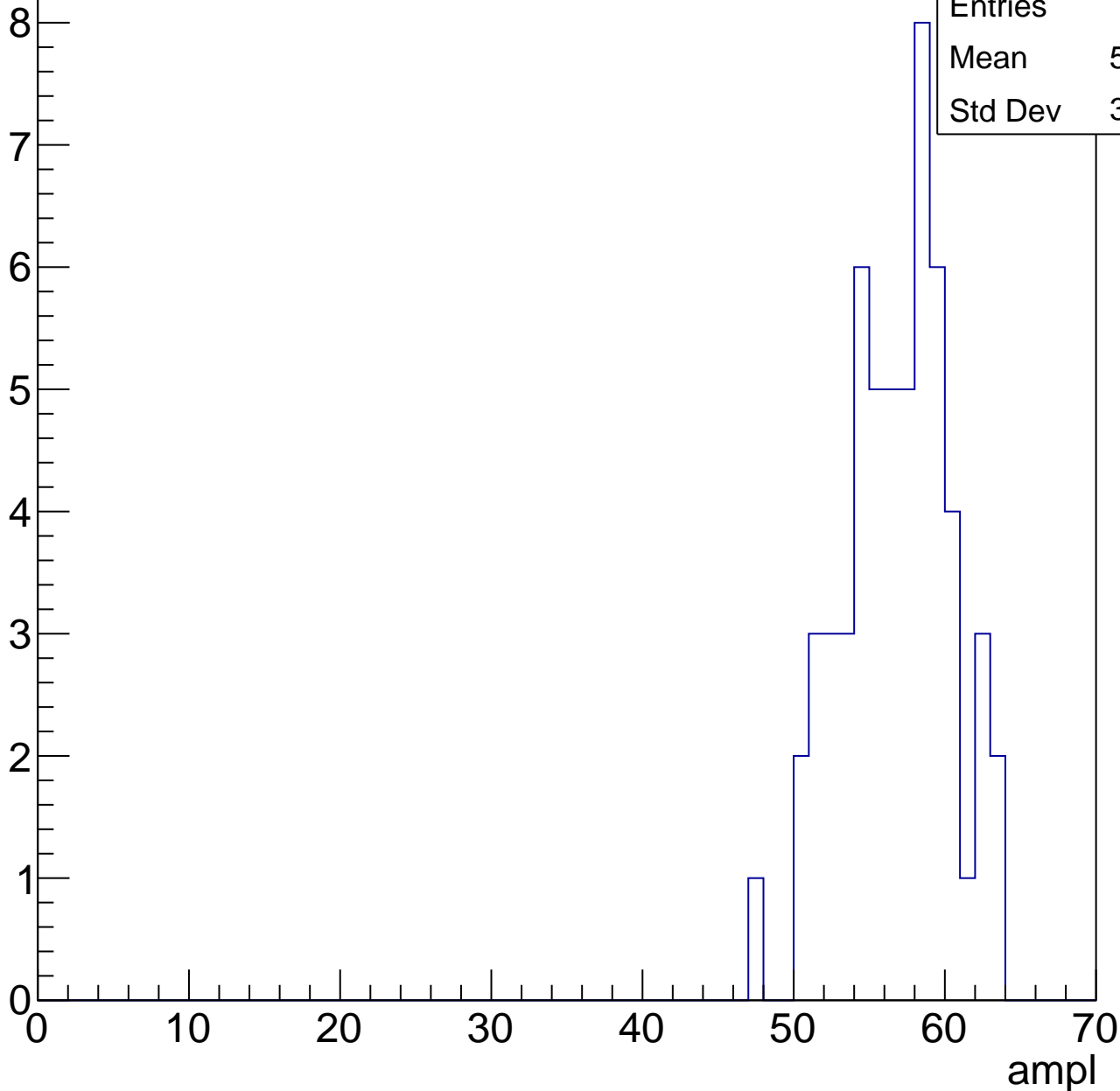


# B1L102S, U8-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	56.32
Std Dev	3.535



# B1L102S, U8-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	38
Mean	59
Std Dev	9.897

ampl

0

10

20

30

40

50

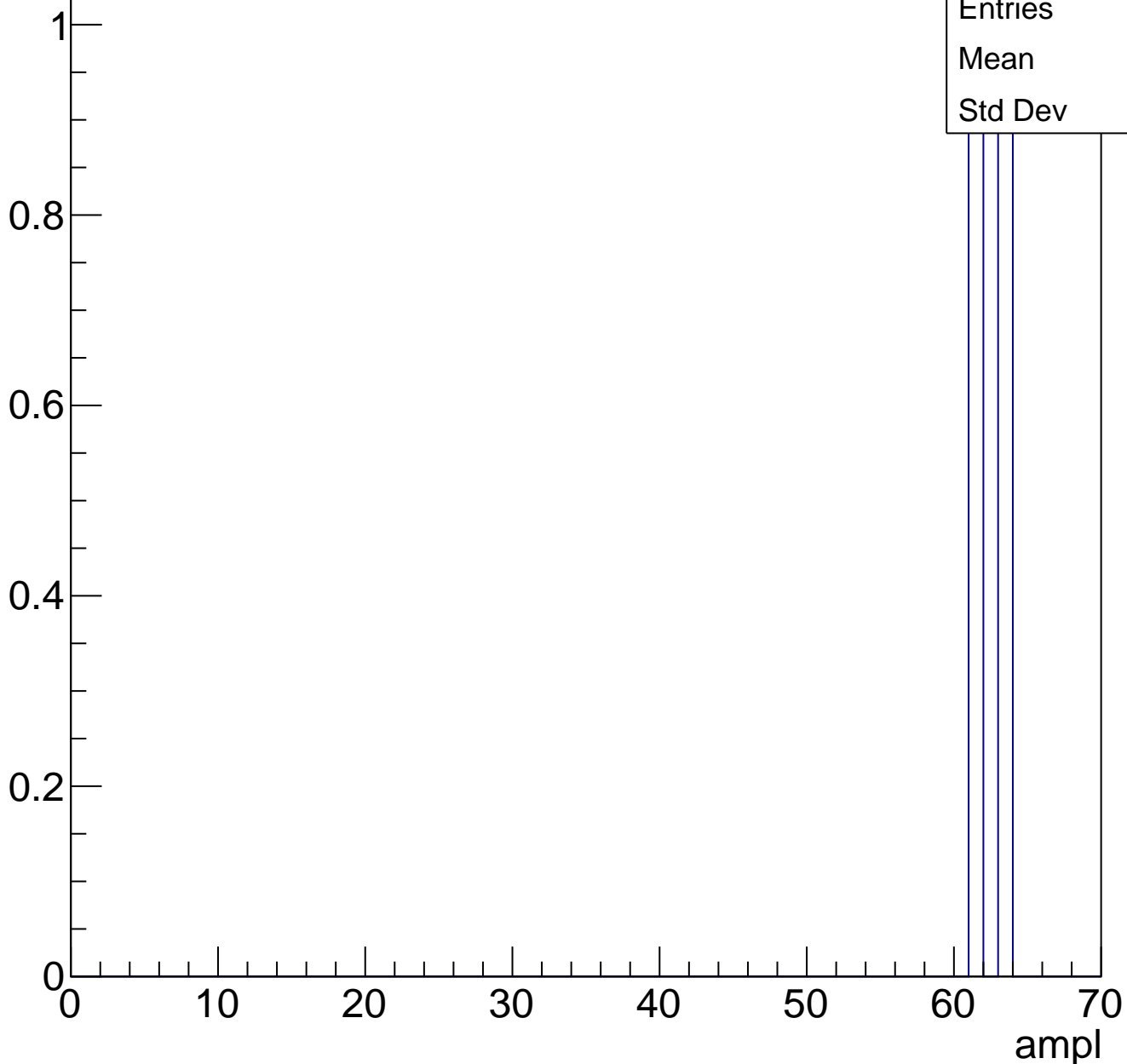
60

70

# B1L102S, U8-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U8-ch12, adc0

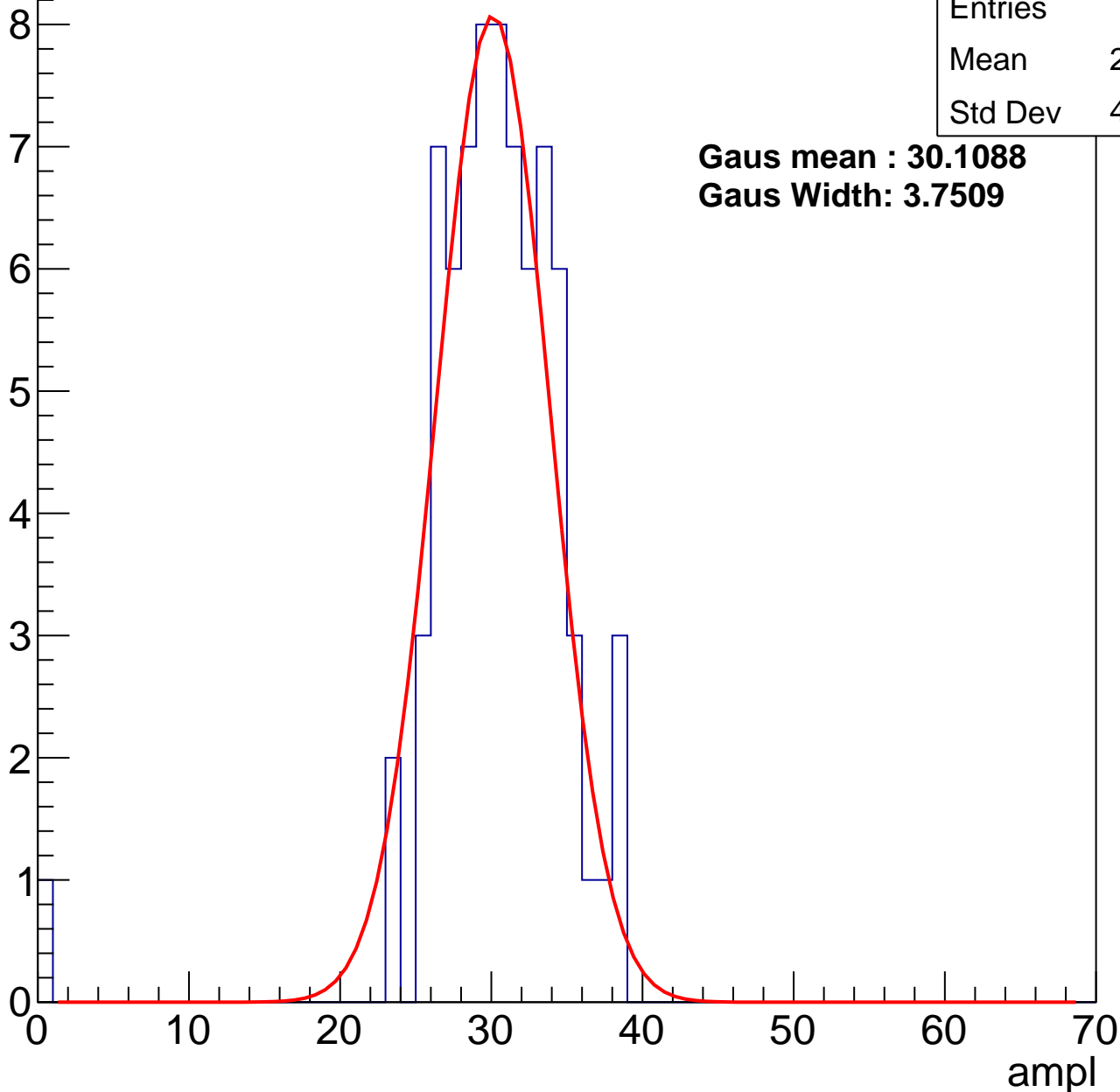
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	29.86
Std Dev	4.887

**Gaus mean : 30.1088**

**Gaus Width: 3.7509**



# B1L102S, U8-ch12, adc1

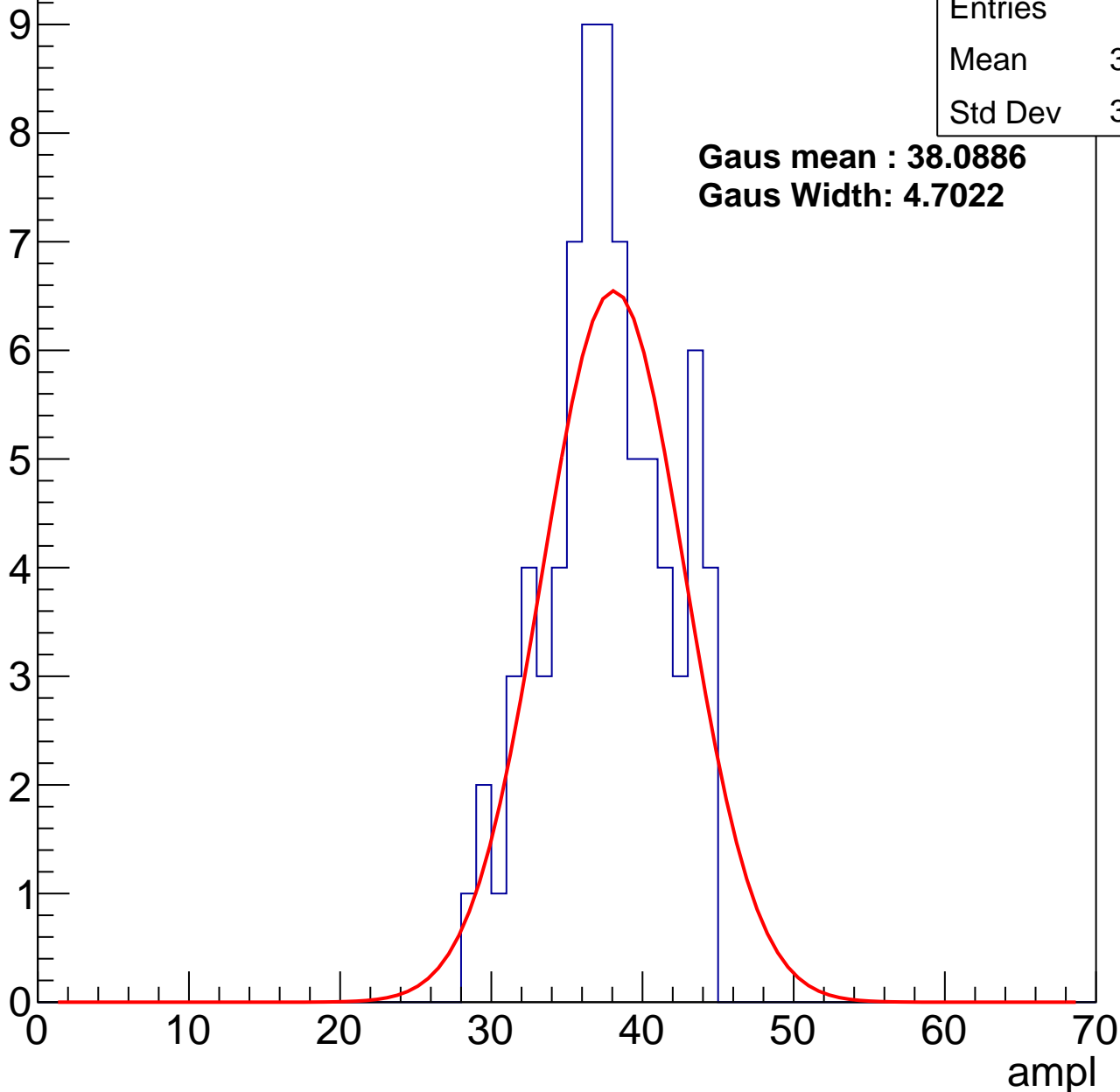
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	37.13
Std Dev	3.962

**Gaus mean : 38.0886**

**Gaus Width: 4.7022**



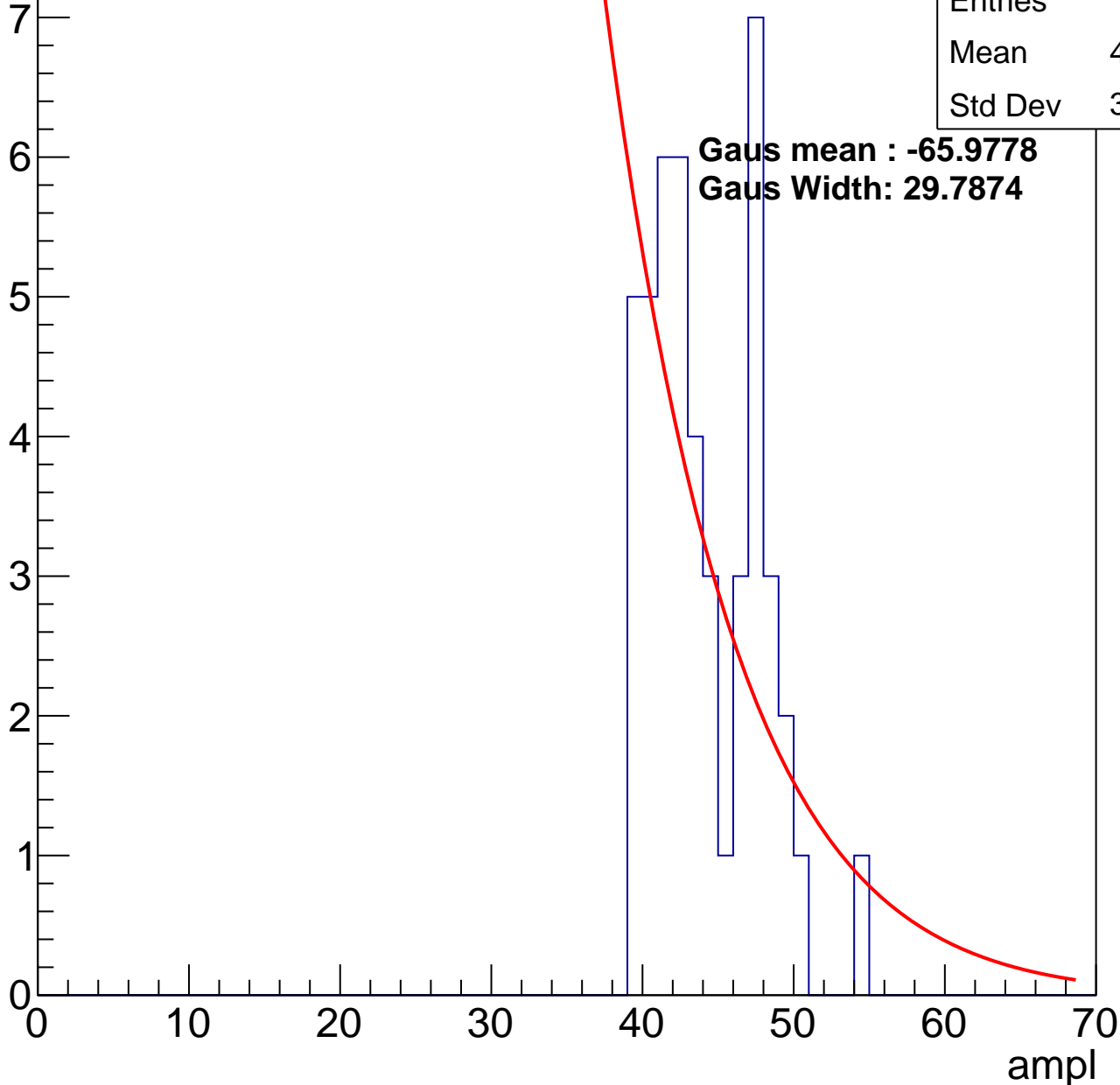
# B1L102S, U8-ch12, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	43.72
Std Dev	3.553

**Gaus mean : -65.9778**  
**Gaus Width: 29.7874**

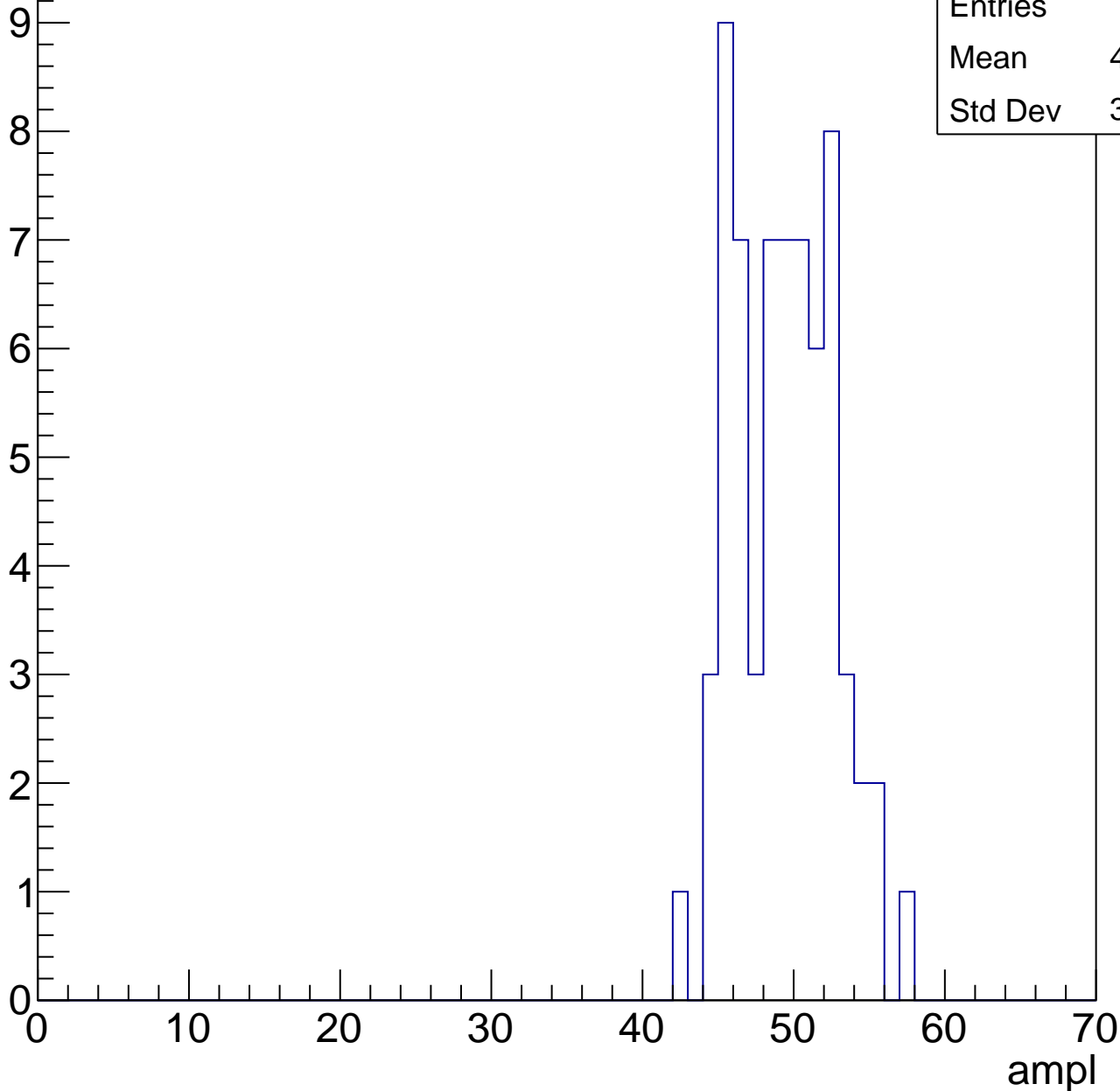


# B1L102S, U8-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

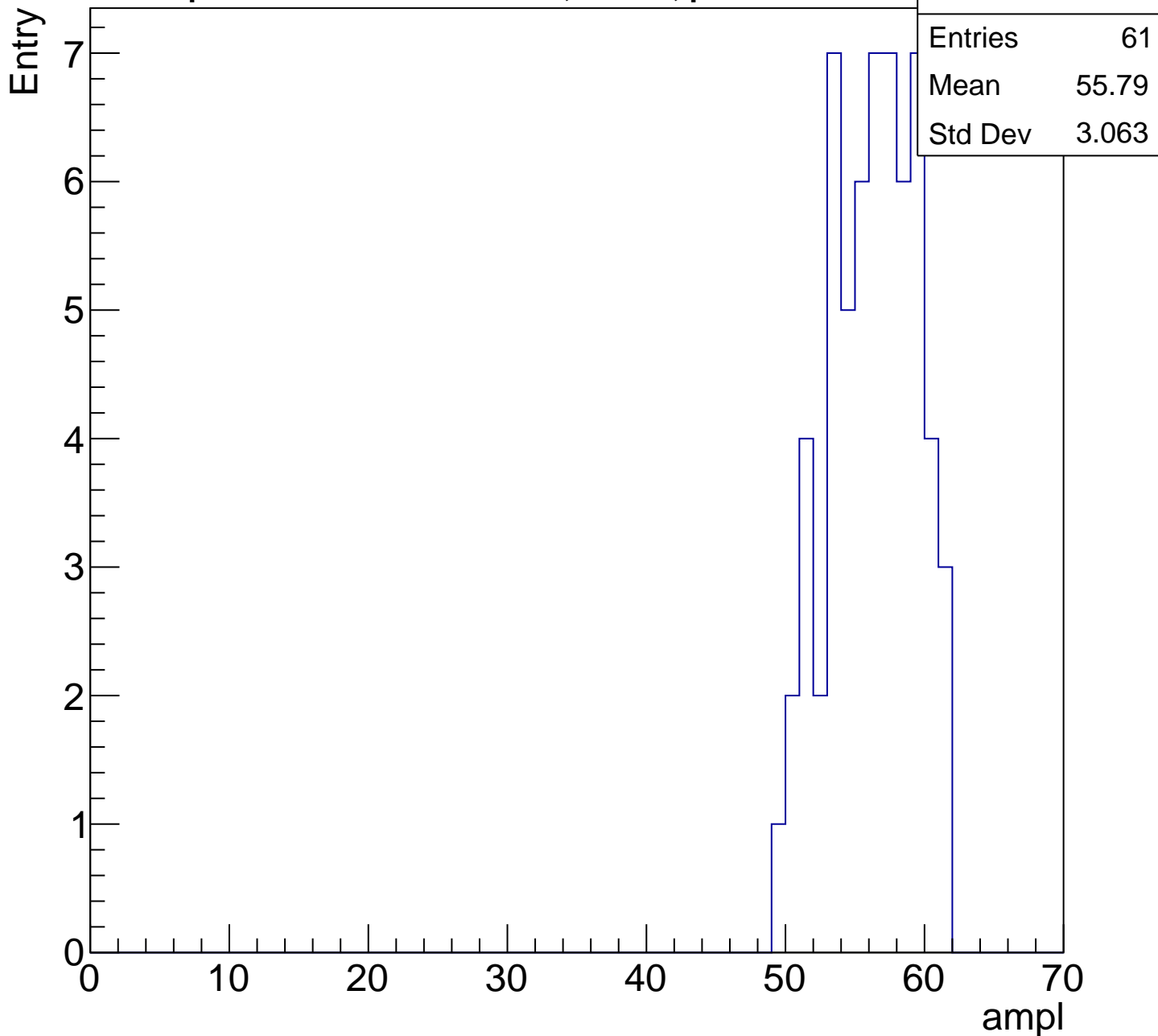
Entry

Entries	66
Mean	48.89
Std Dev	3.225



# B1L102S, U8-ch12, adc4

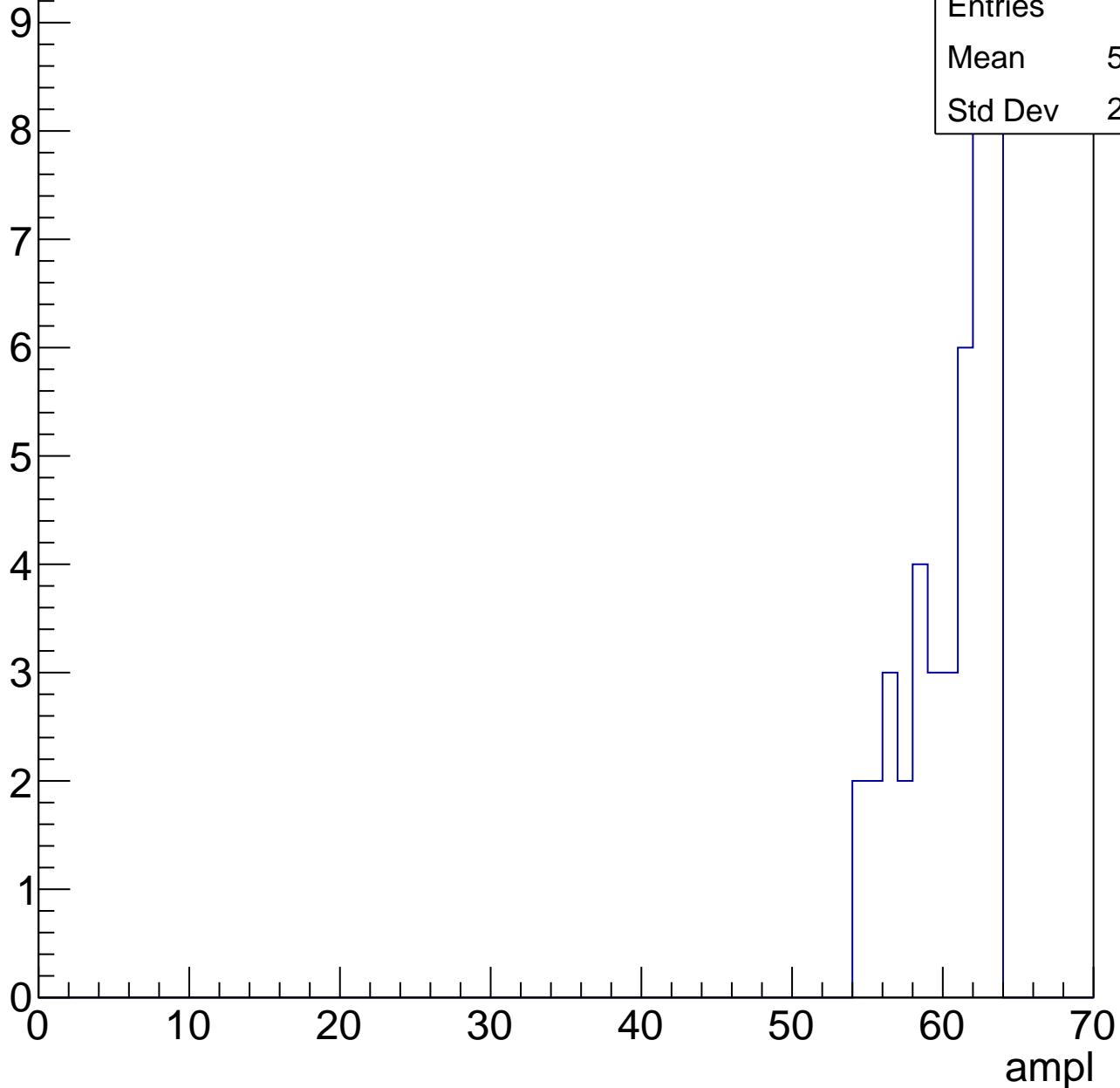
calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U8-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

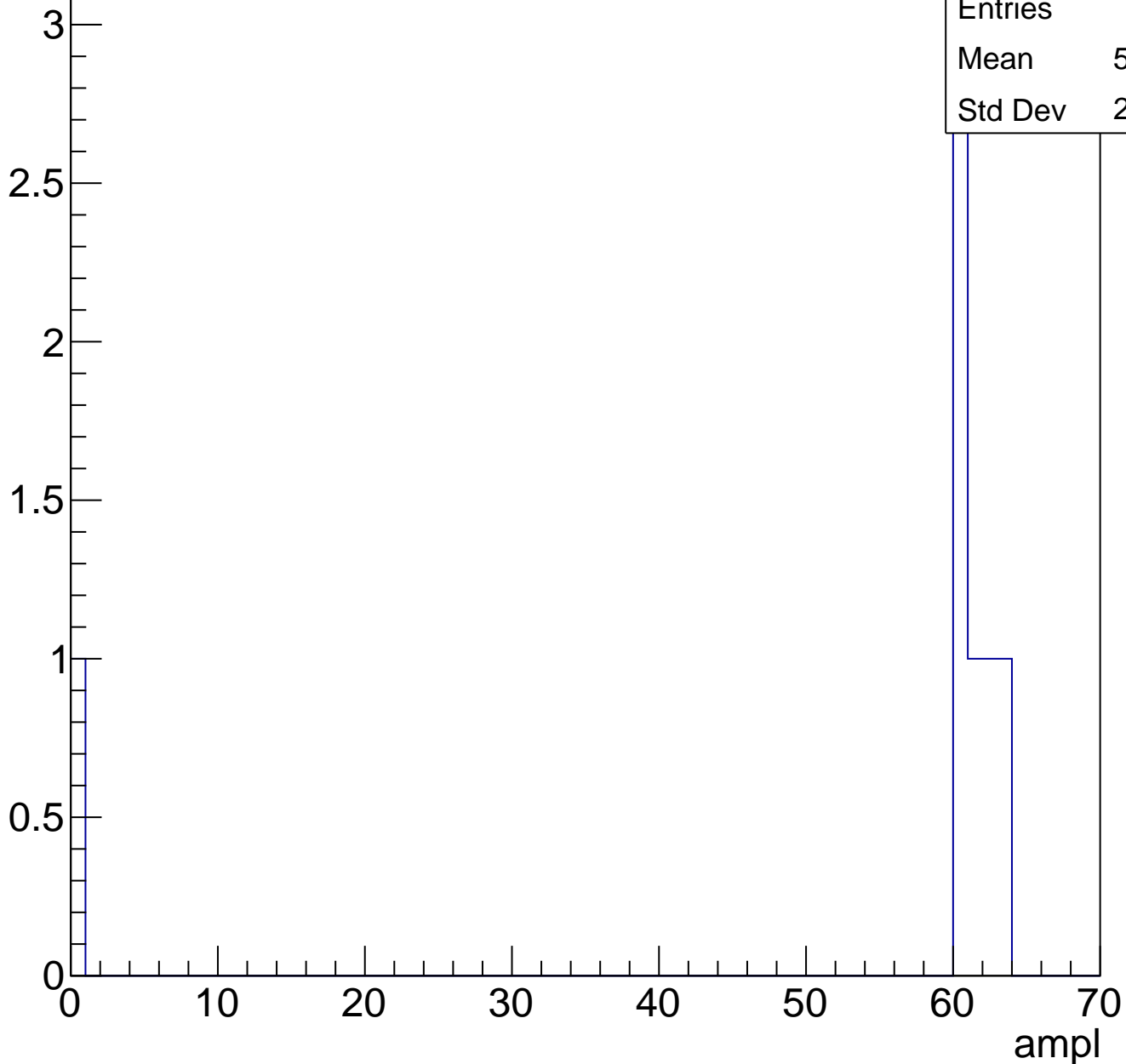
Entry



# B1L102S, U8-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	7
Mean	52.29
Std Dev	21.37



# B1L102S, U8-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch13, adc0

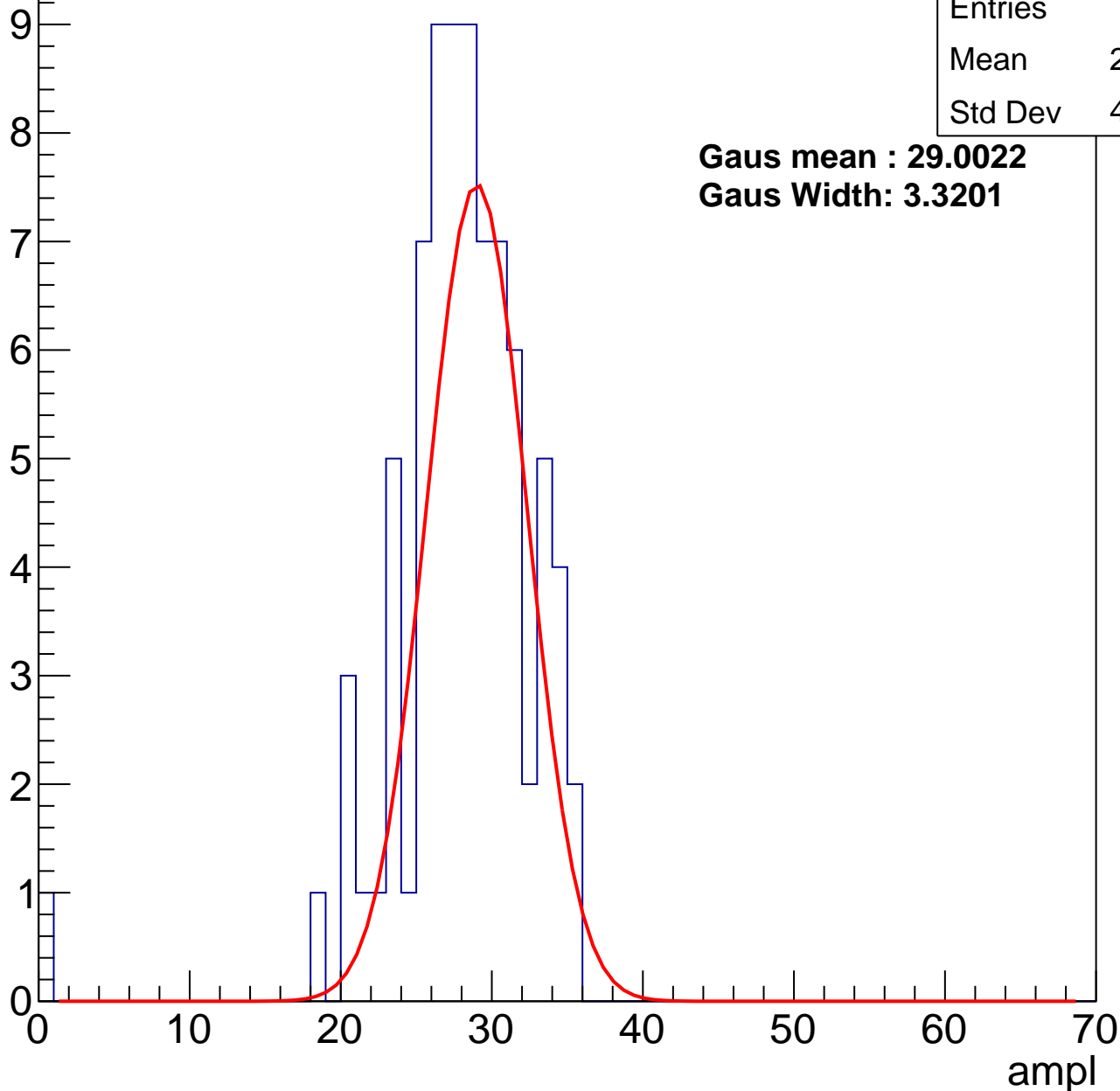
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	27.48
Std Dev	4.842

**Gaus mean : 29.0022**

**Gaus Width: 3.3201**



# B1L102S, U8-ch13, adc1

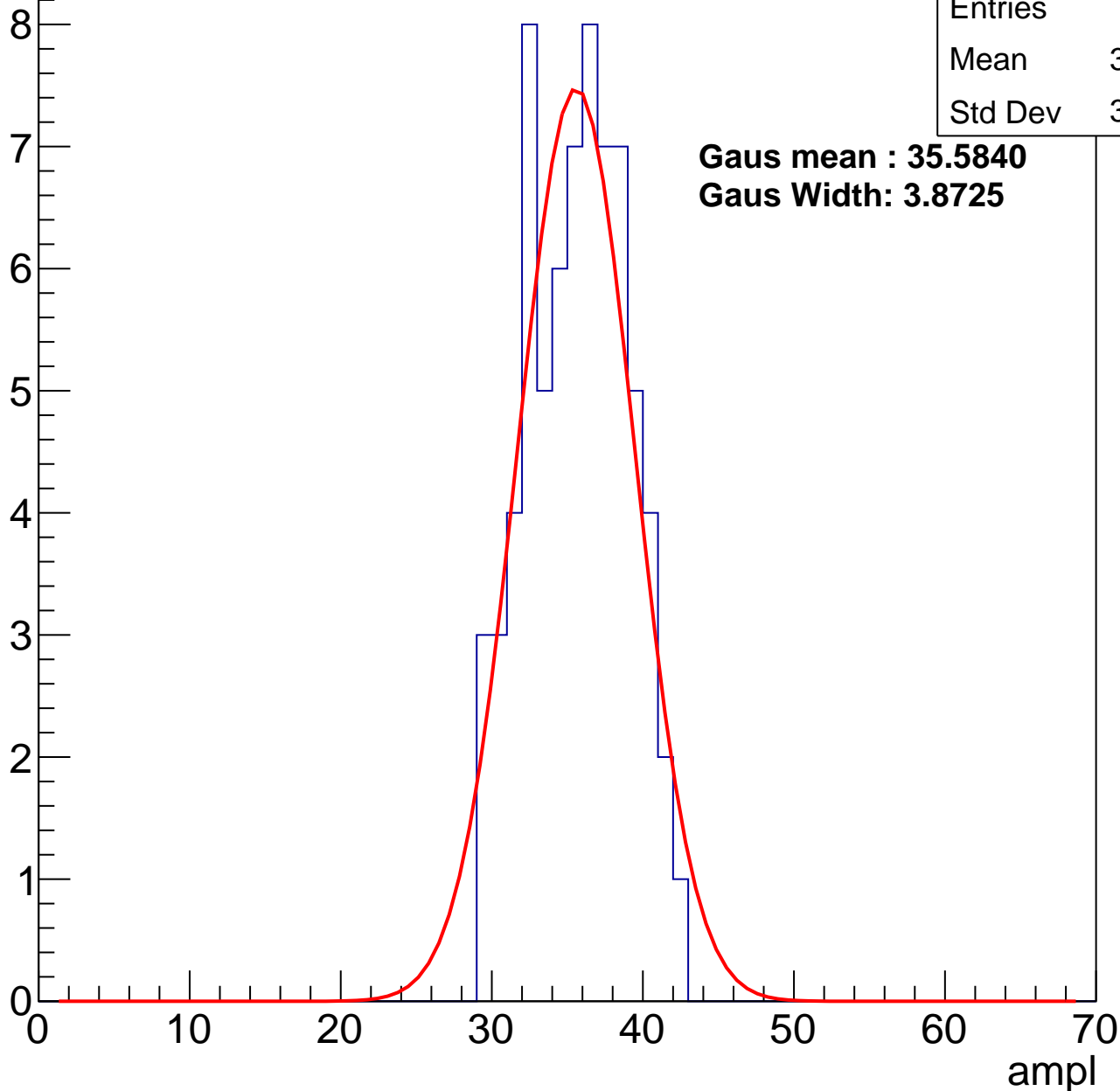
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	35.19
Std Dev	3.257

**Gaus mean : 35.5840**

**Gaus Width: 3.8725**



# B1L102S, U8-ch13, adc2

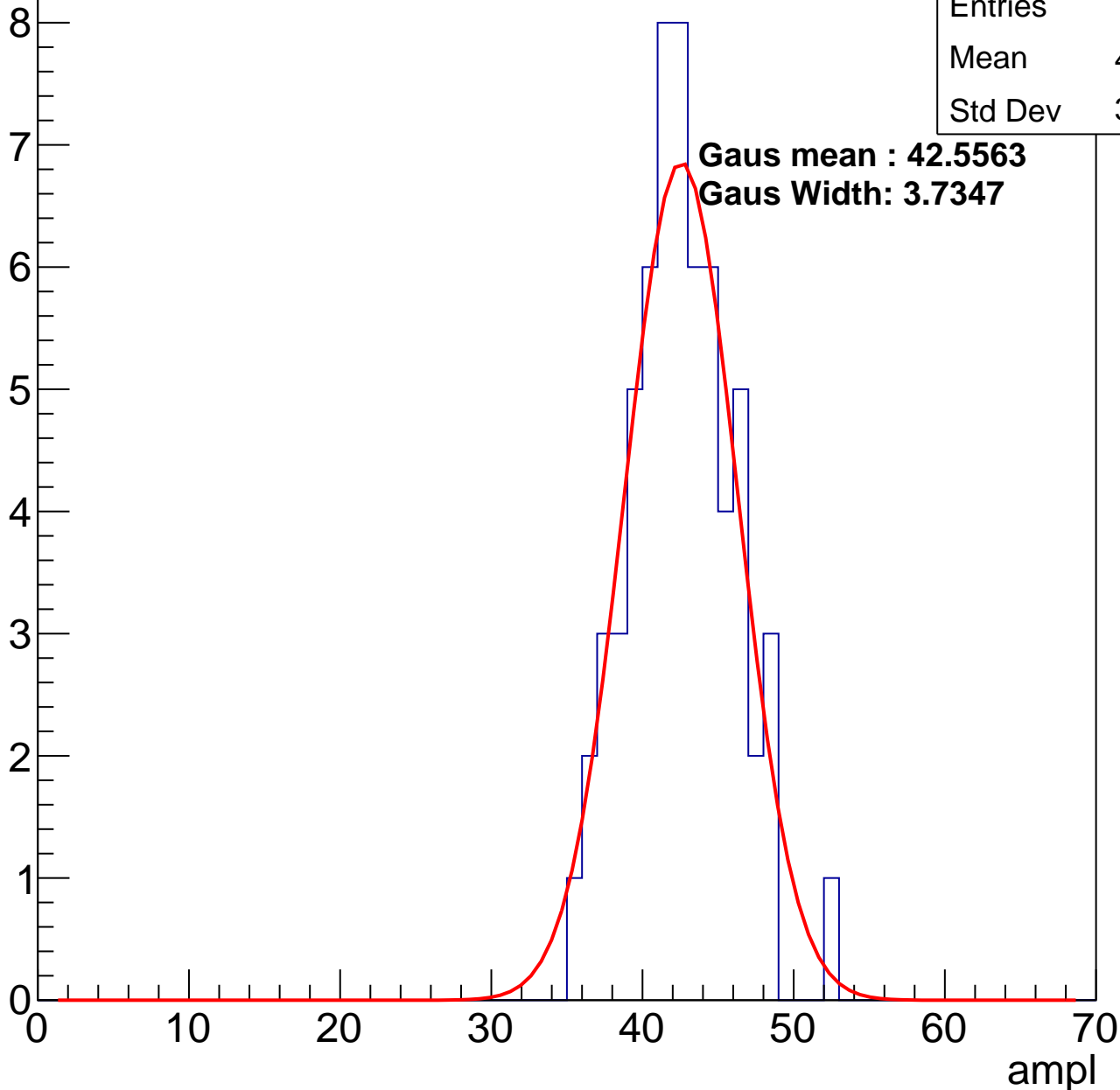
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	42.11
Std Dev	3.391

**Gaus mean : 42.5563**

**Gaus Width: 3.7347**

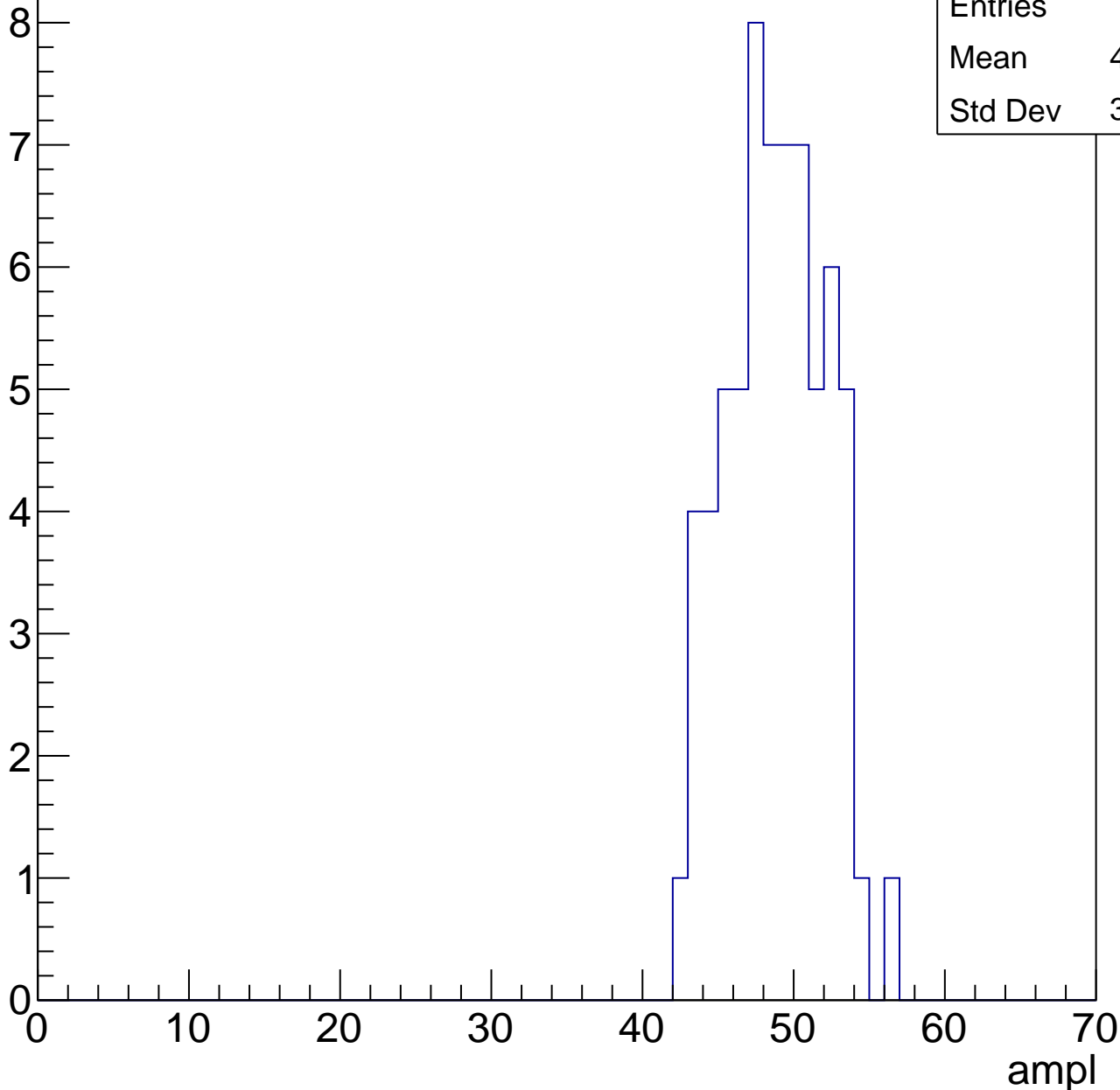


# B1L102S, U8-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	48.36
Std Dev	3.175

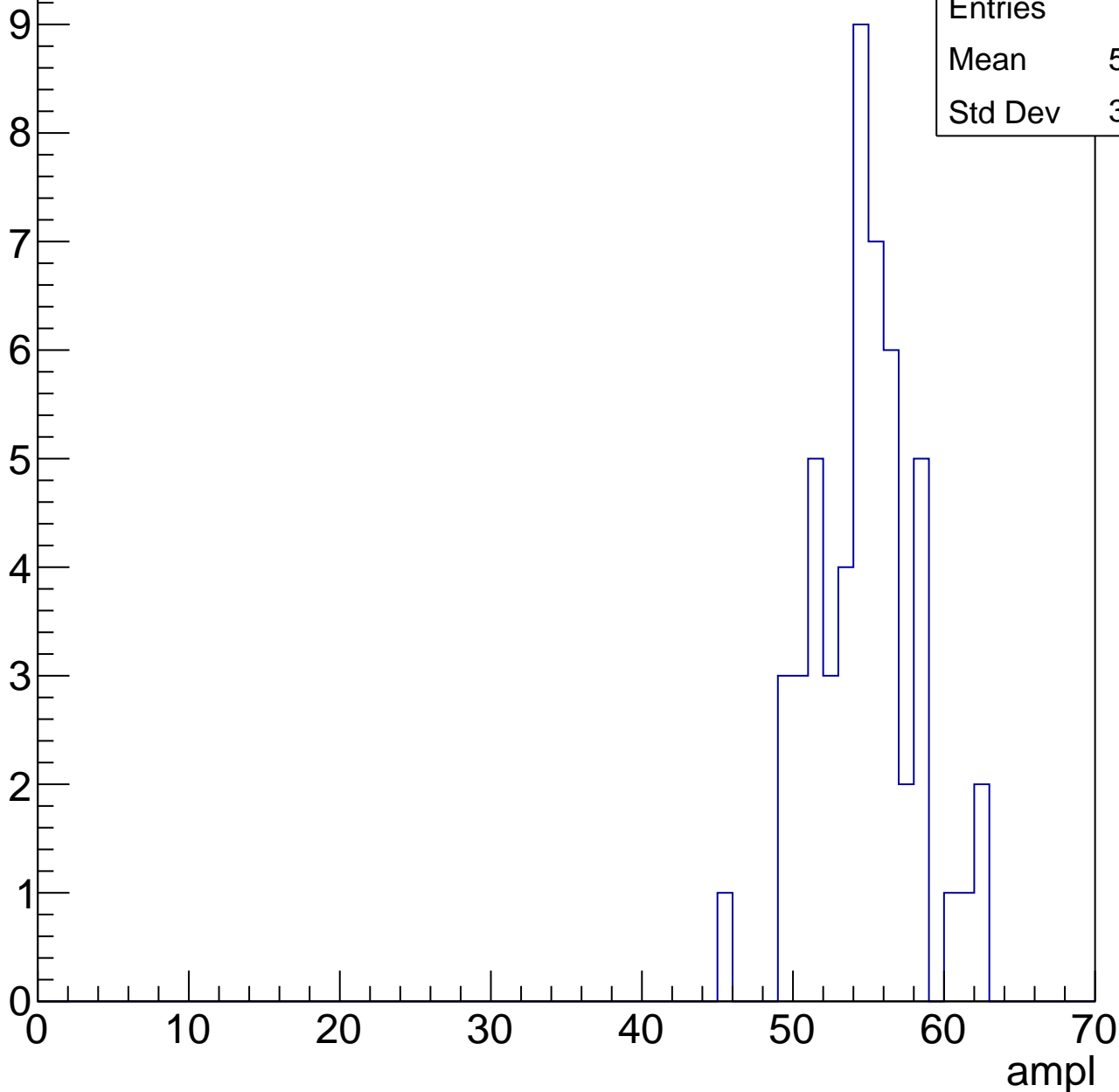


# B1L102S, U8-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	54.25
Std Dev	3.407

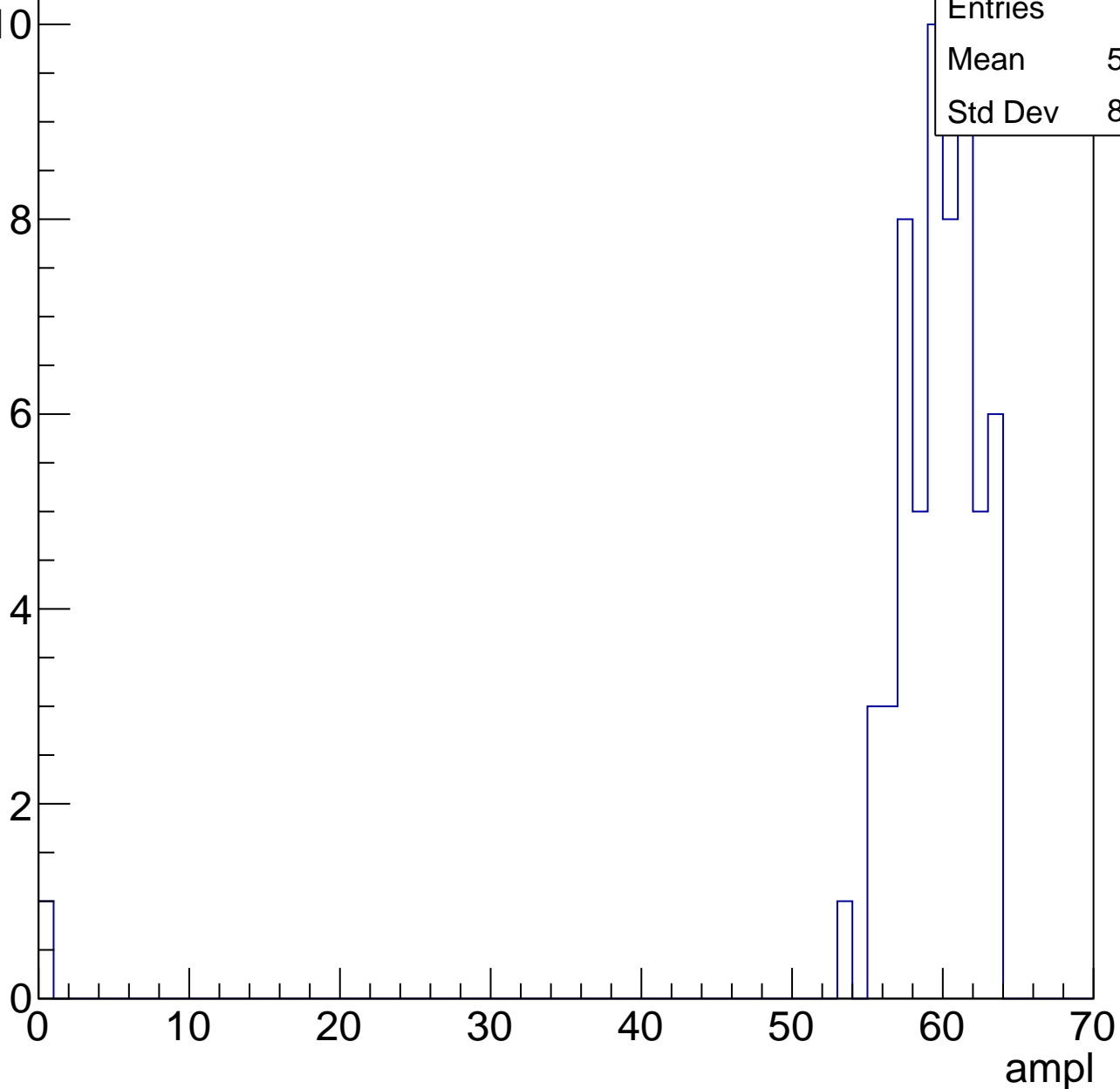


# B1L102S, U8-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

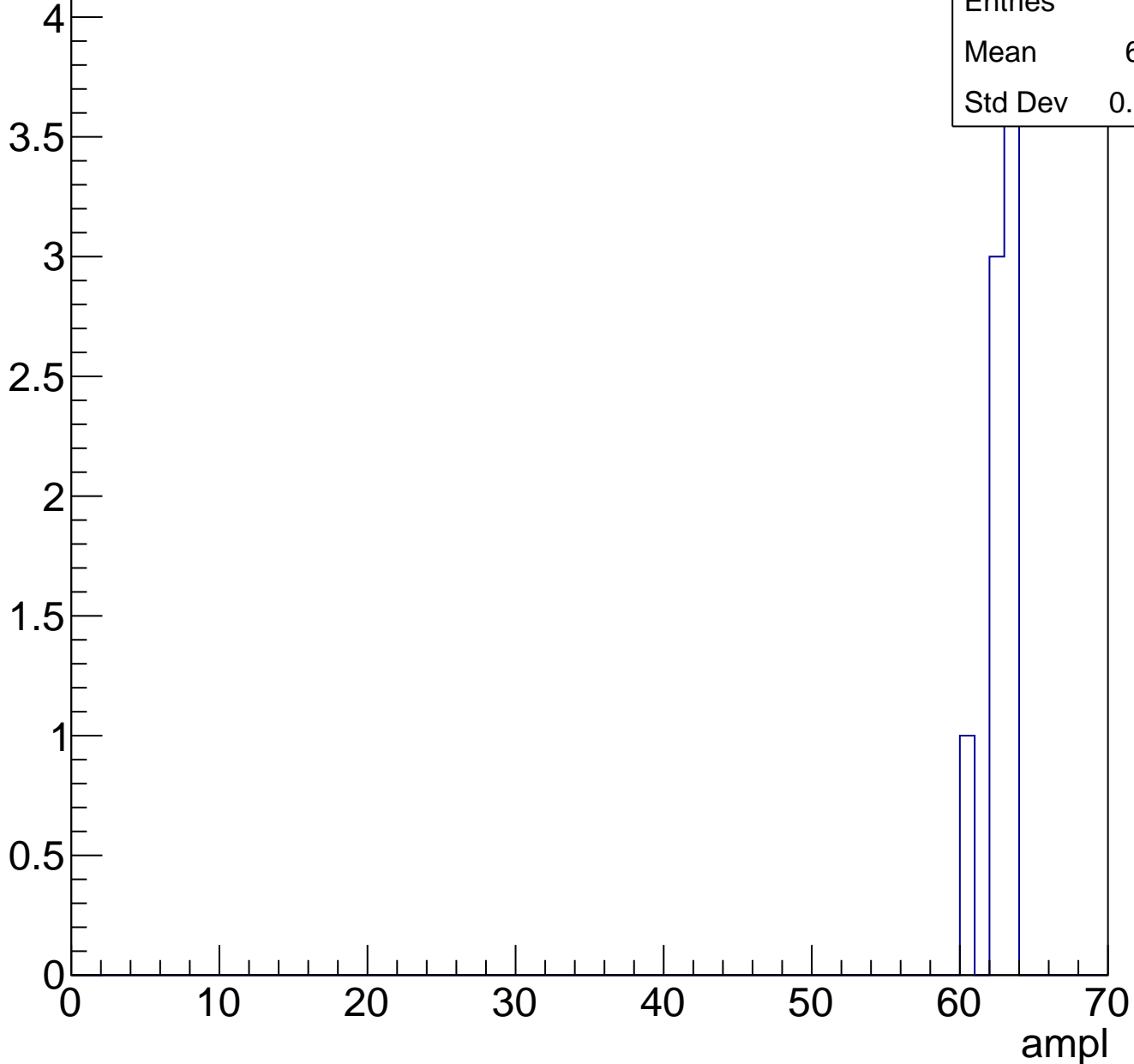
Entries	59
Mean	58.29
Std Dev	8.009



# B1L102S, U8-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U8-ch14, adc0

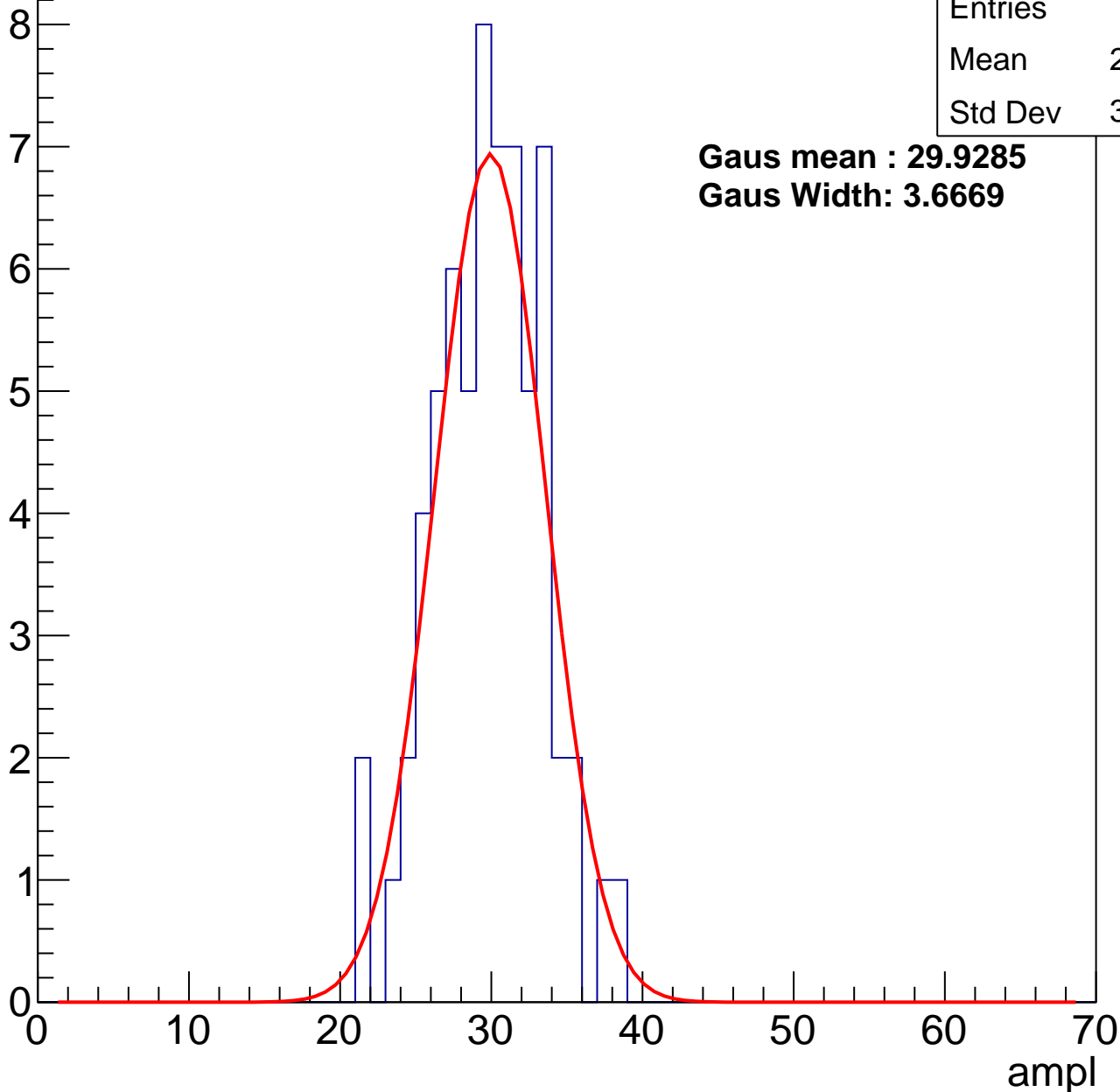
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	29.35
Std Dev	3.515

**Gaus mean : 29.9285**

**Gaus Width: 3.6669**



# B1L102S, U8-ch14, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	36.42
Std Dev	3.435

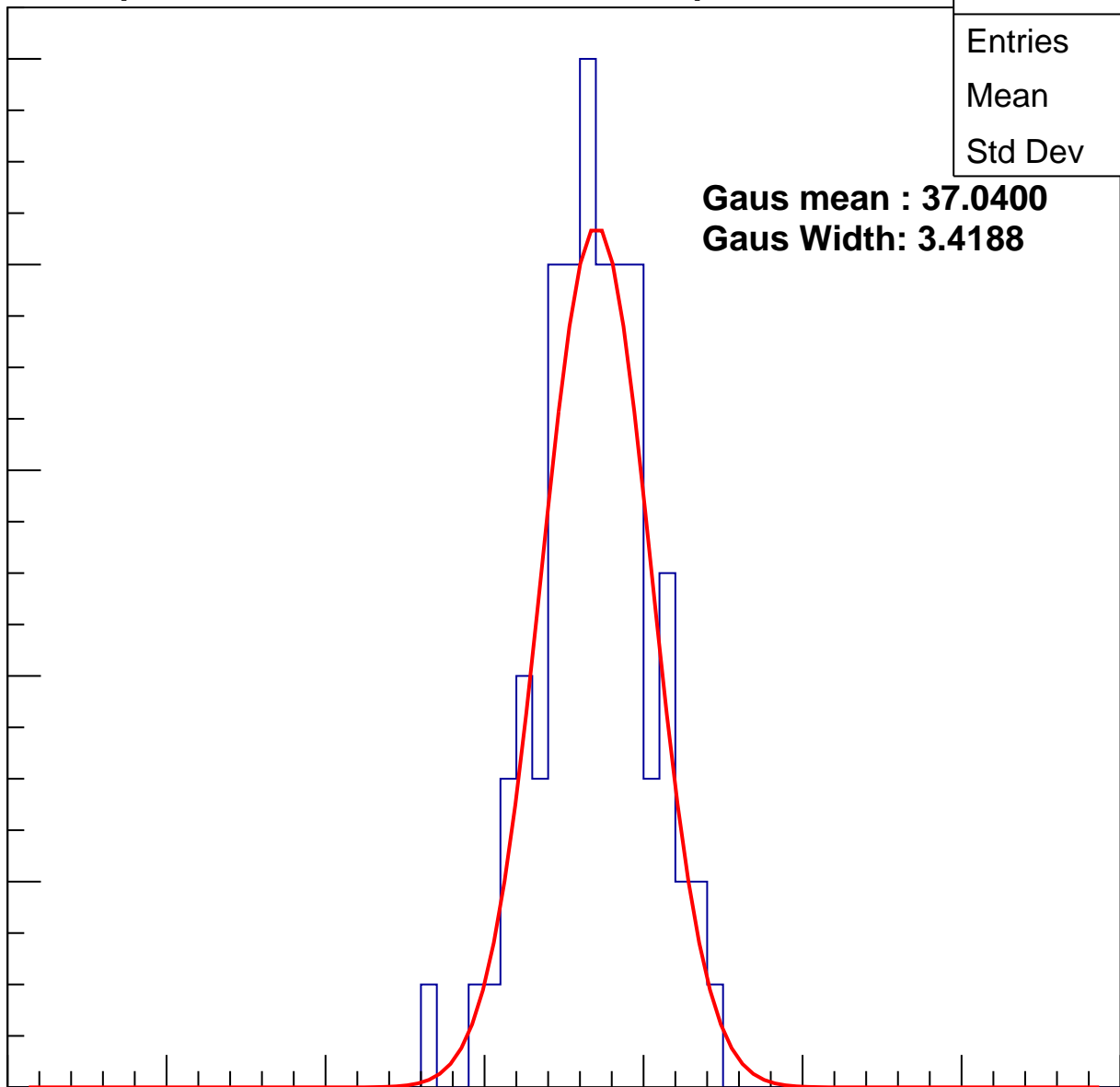
**Gaus mean : 37.0400**

**Gaus Width: 3.4188**

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L102S, U8-ch14, adc2

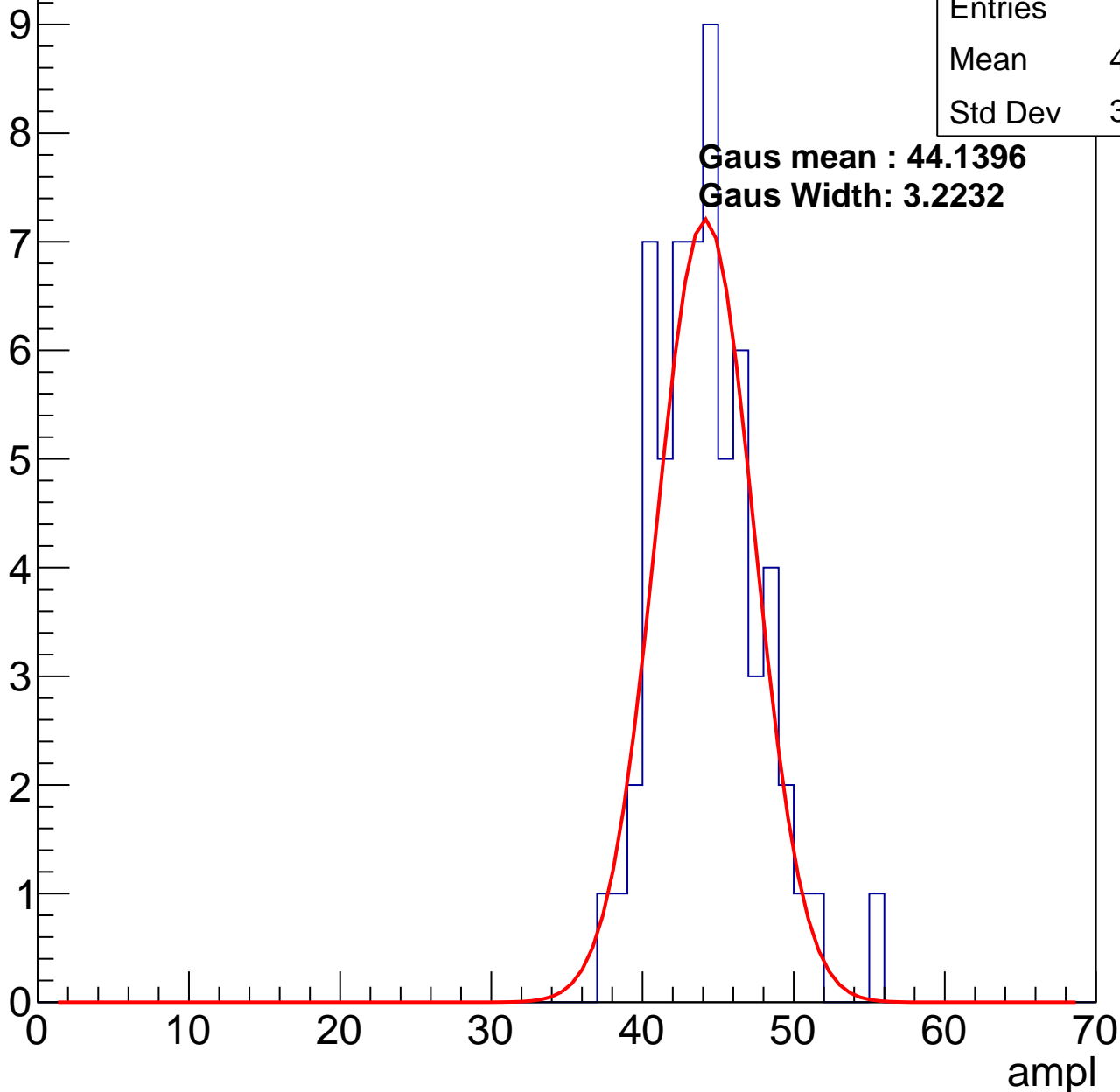
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	43.82
Std Dev	3.363

**Gaus mean : 44.1396**

**Gaus Width: 3.2232**

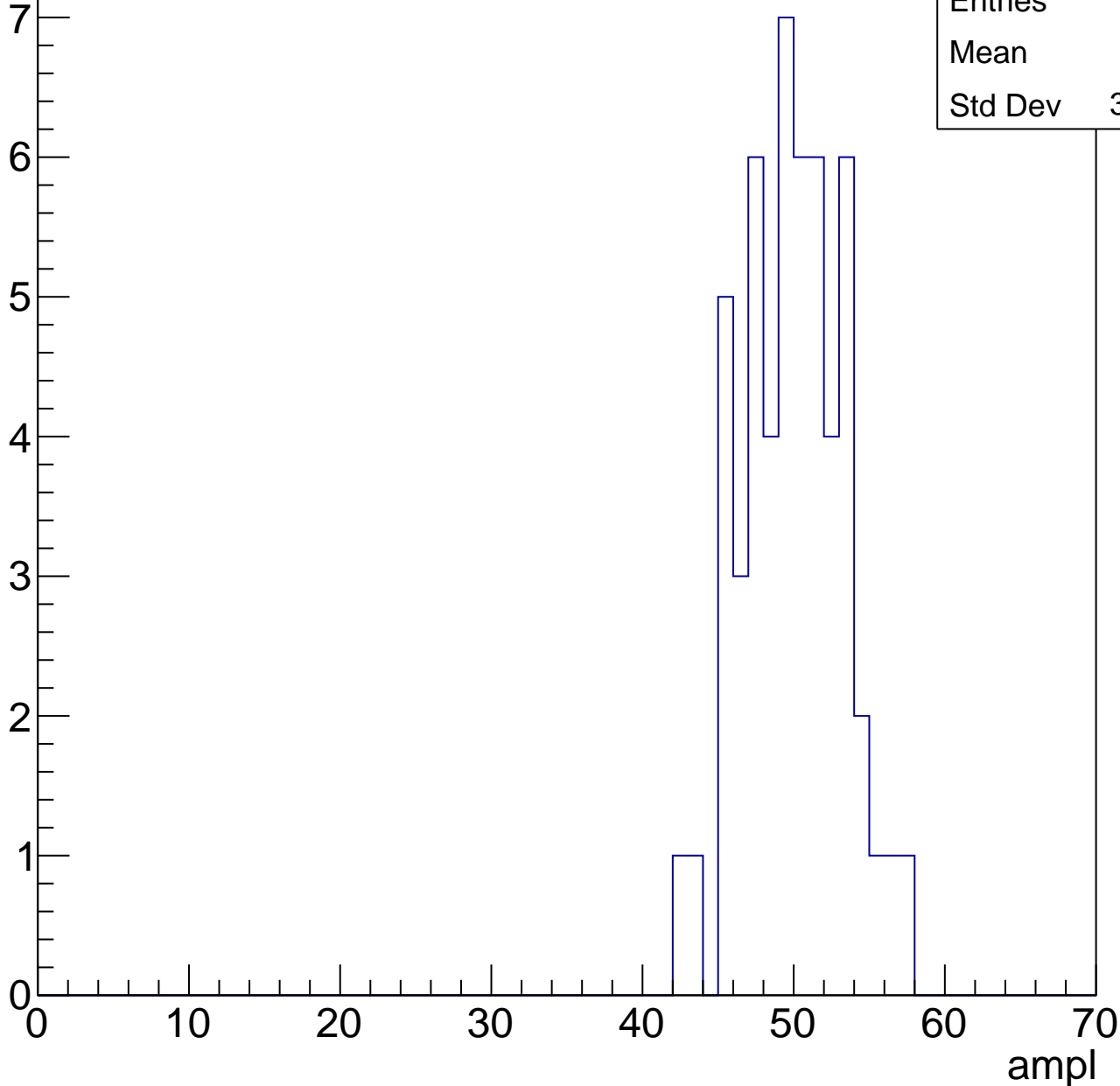


# B1L102S, U8-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	49.5
Std Dev	3.242

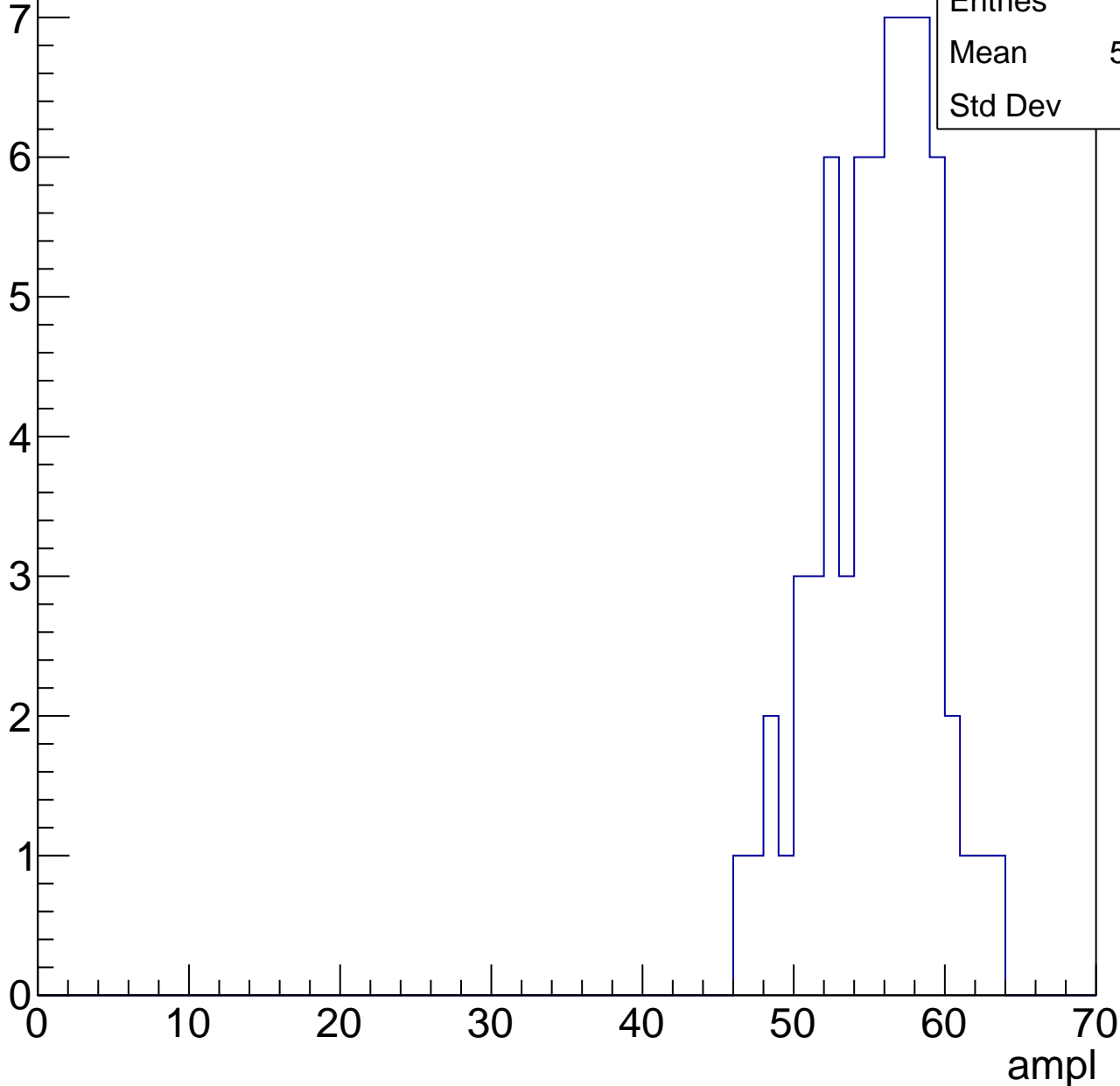


# B1L102S, U8-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	55.05
Std Dev	3.68



# B1L102S, U8-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	50
Mean	58.72
Std Dev	8.796

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

7

8

9

# B1L102S, U8-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch15, adc0

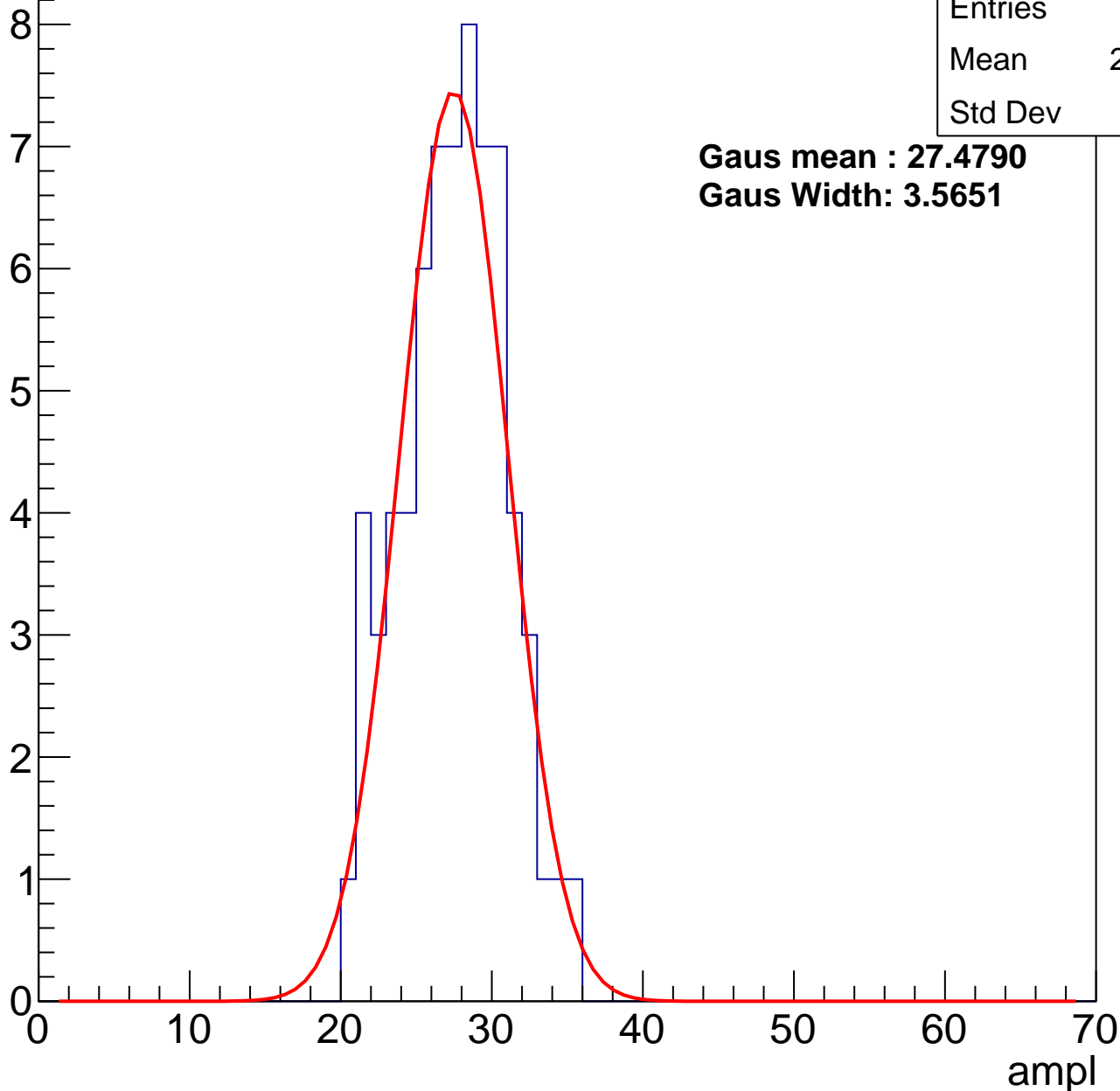
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	27.03
Std Dev	3.4

**Gaus mean : 27.4790**

**Gaus Width: 3.5651**



# B1L102S, U8-ch15, adc1

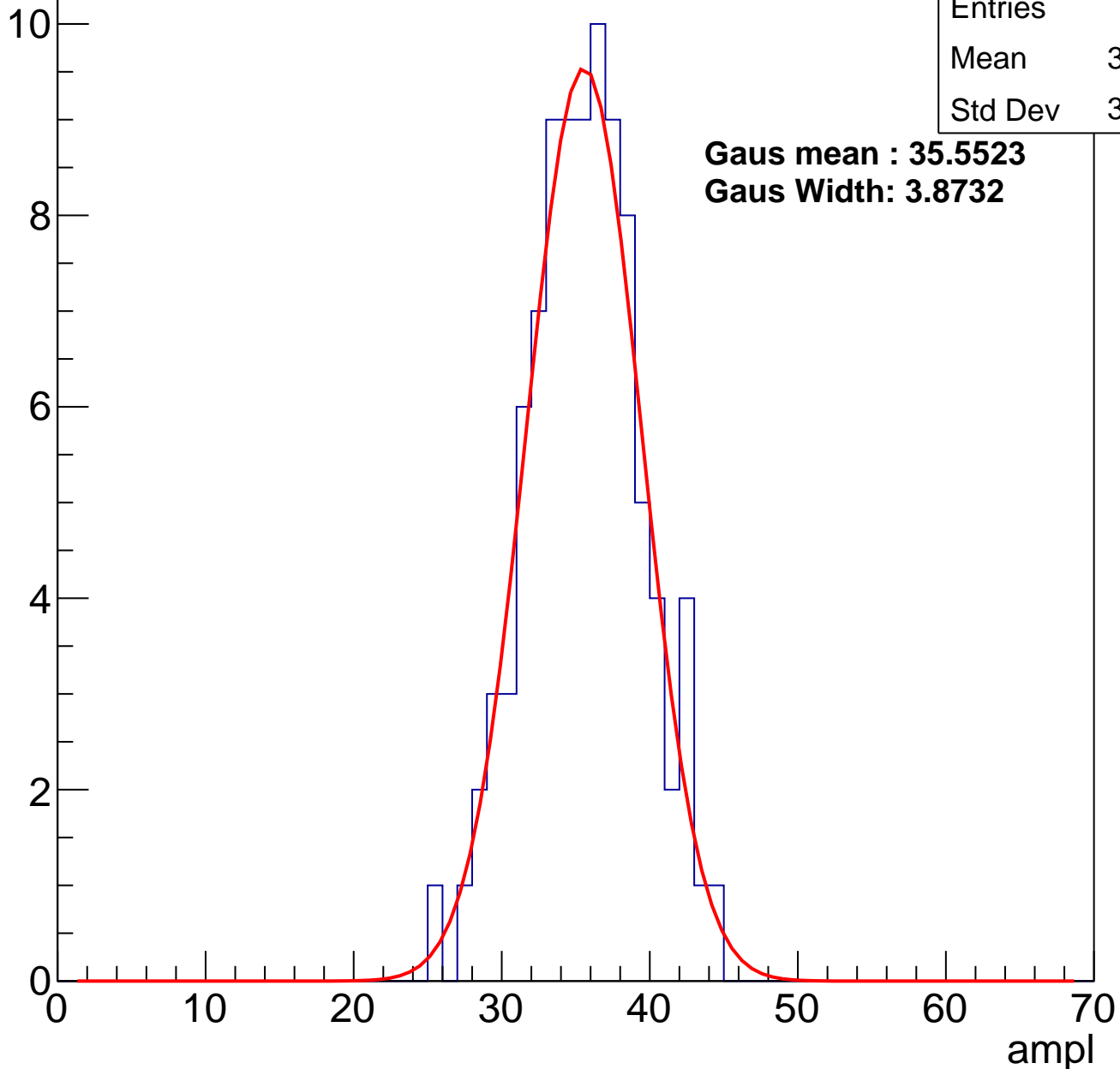
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	94
Mean	35.13
Std Dev	3.802

**Gaus mean : 35.5523**

**Gaus Width: 3.8732**

Entry



# B1L102S, U8-ch15, adc2

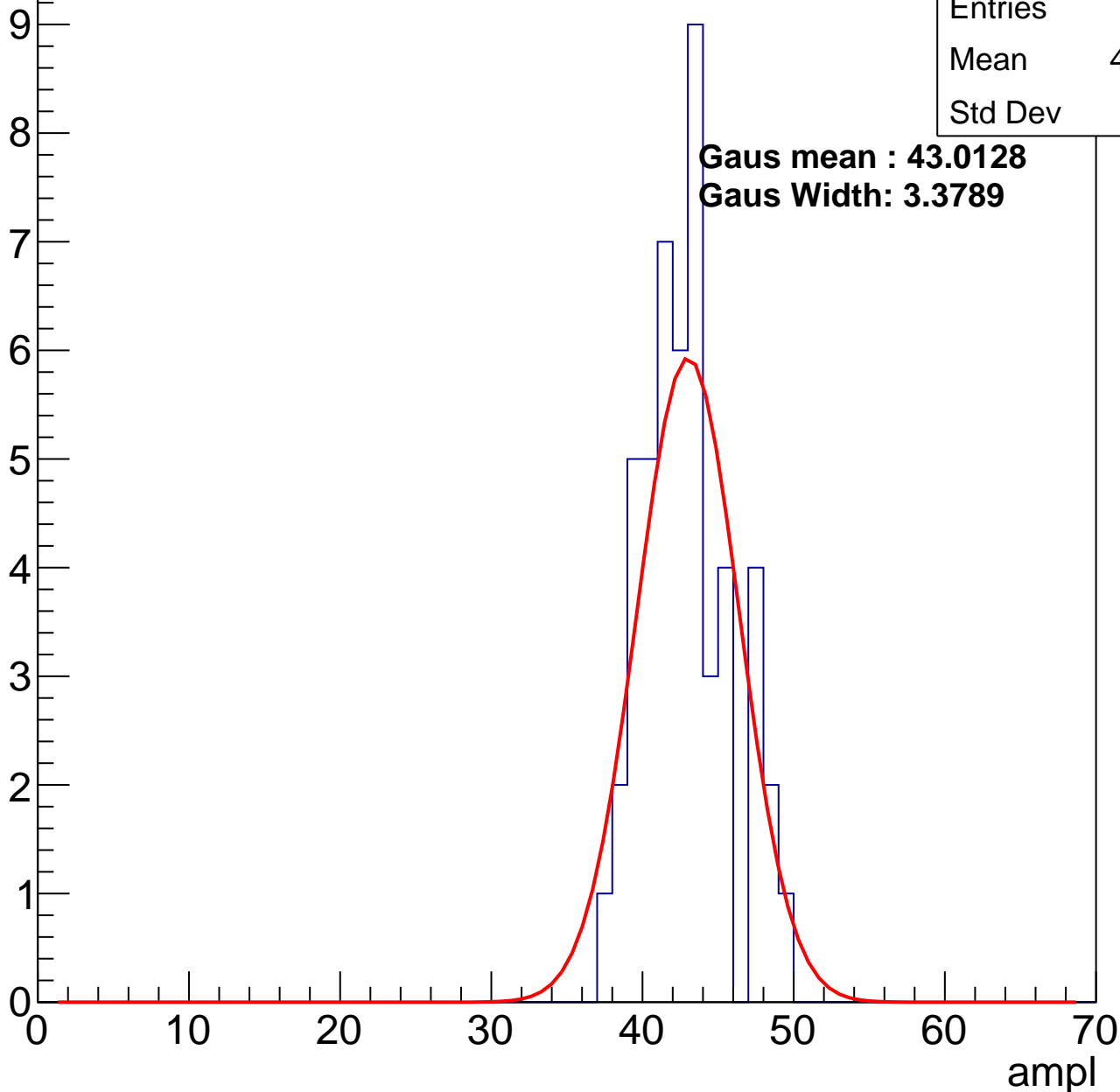
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	42.43
Std Dev	2.85

**Gaus mean : 43.0128**

**Gaus Width: 3.3789**

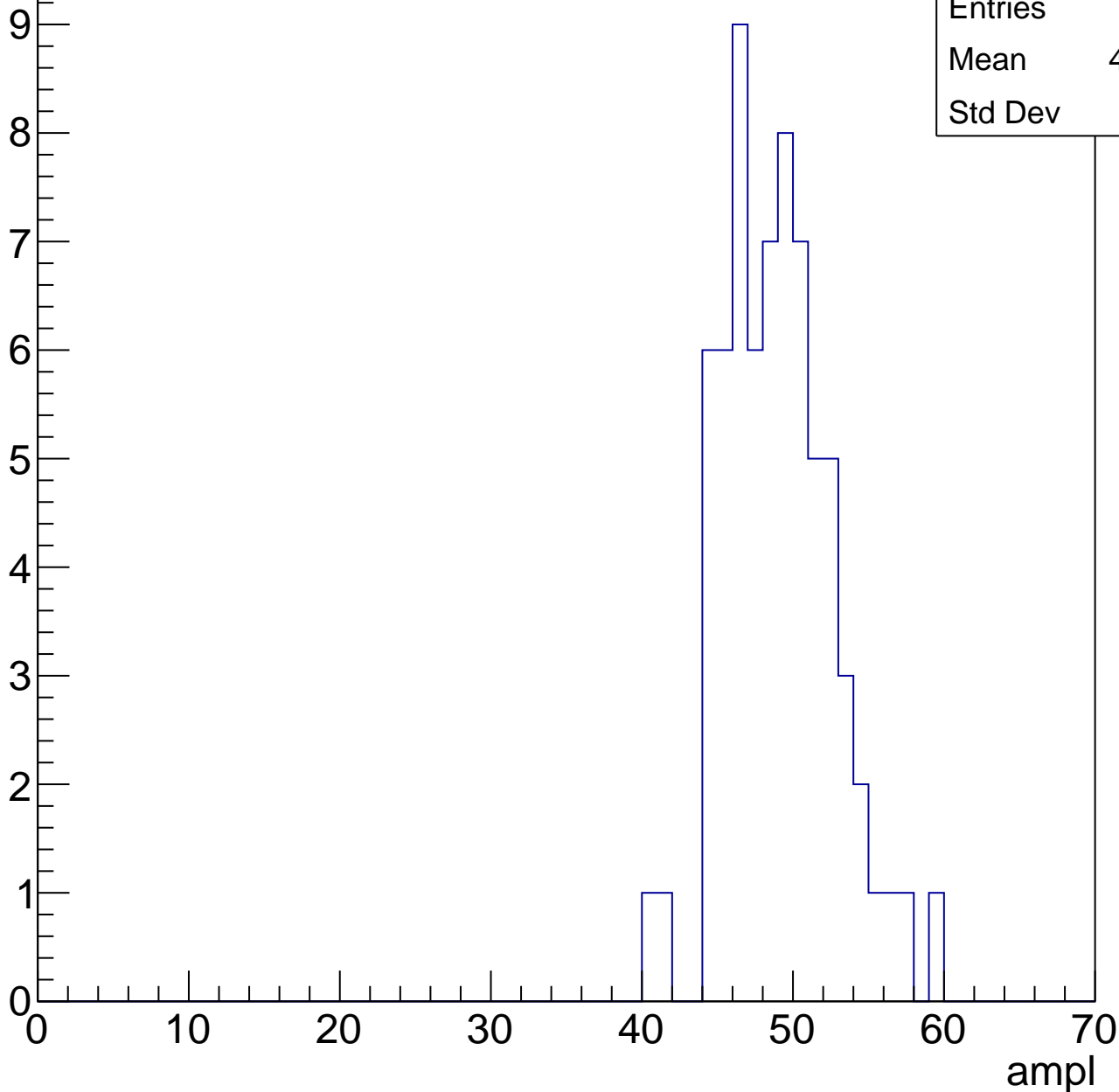


# B1L102S, U8-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

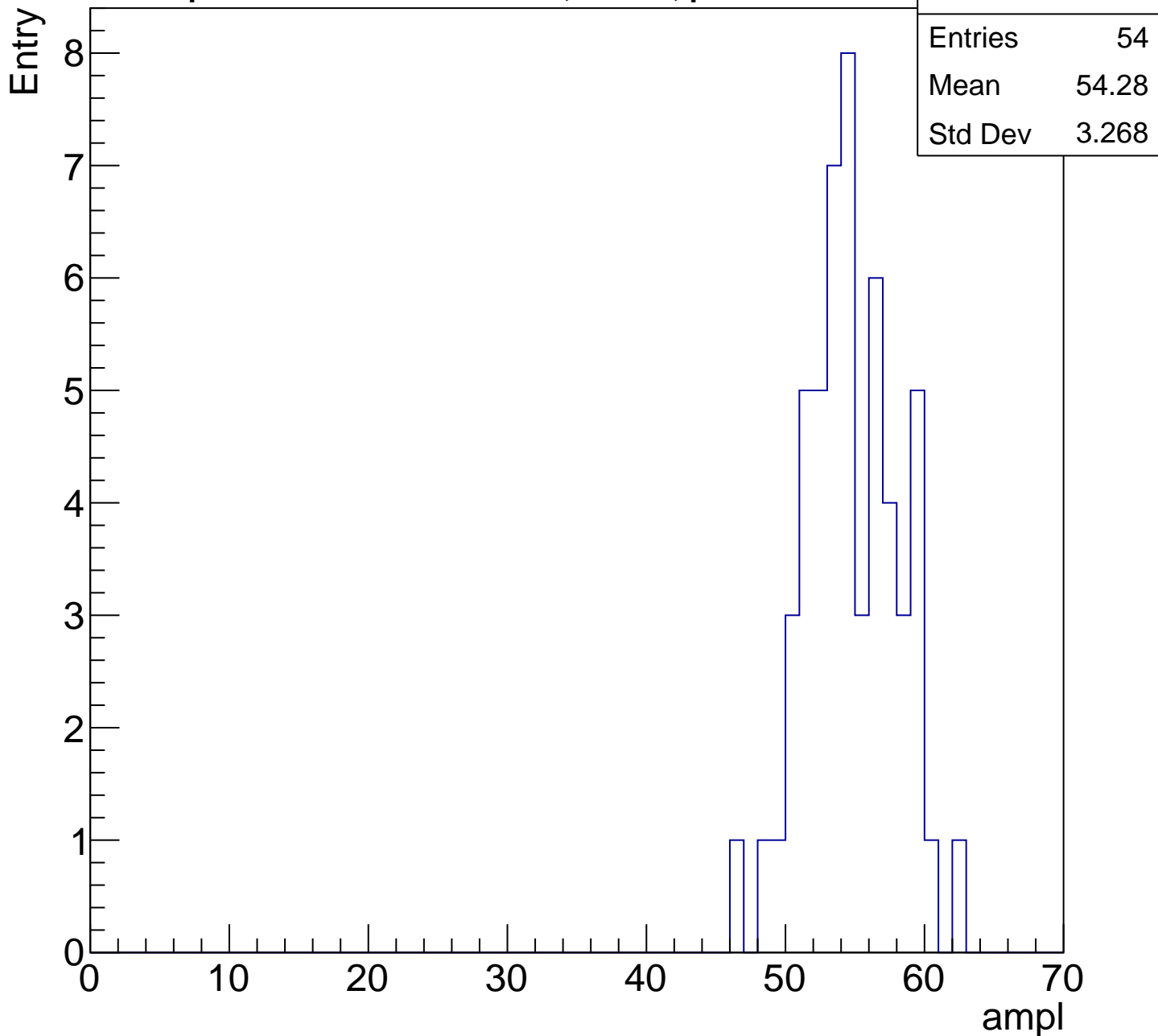
Entry

Entries	70
Mean	48.54
Std Dev	3.6



# B1L102S, U8-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

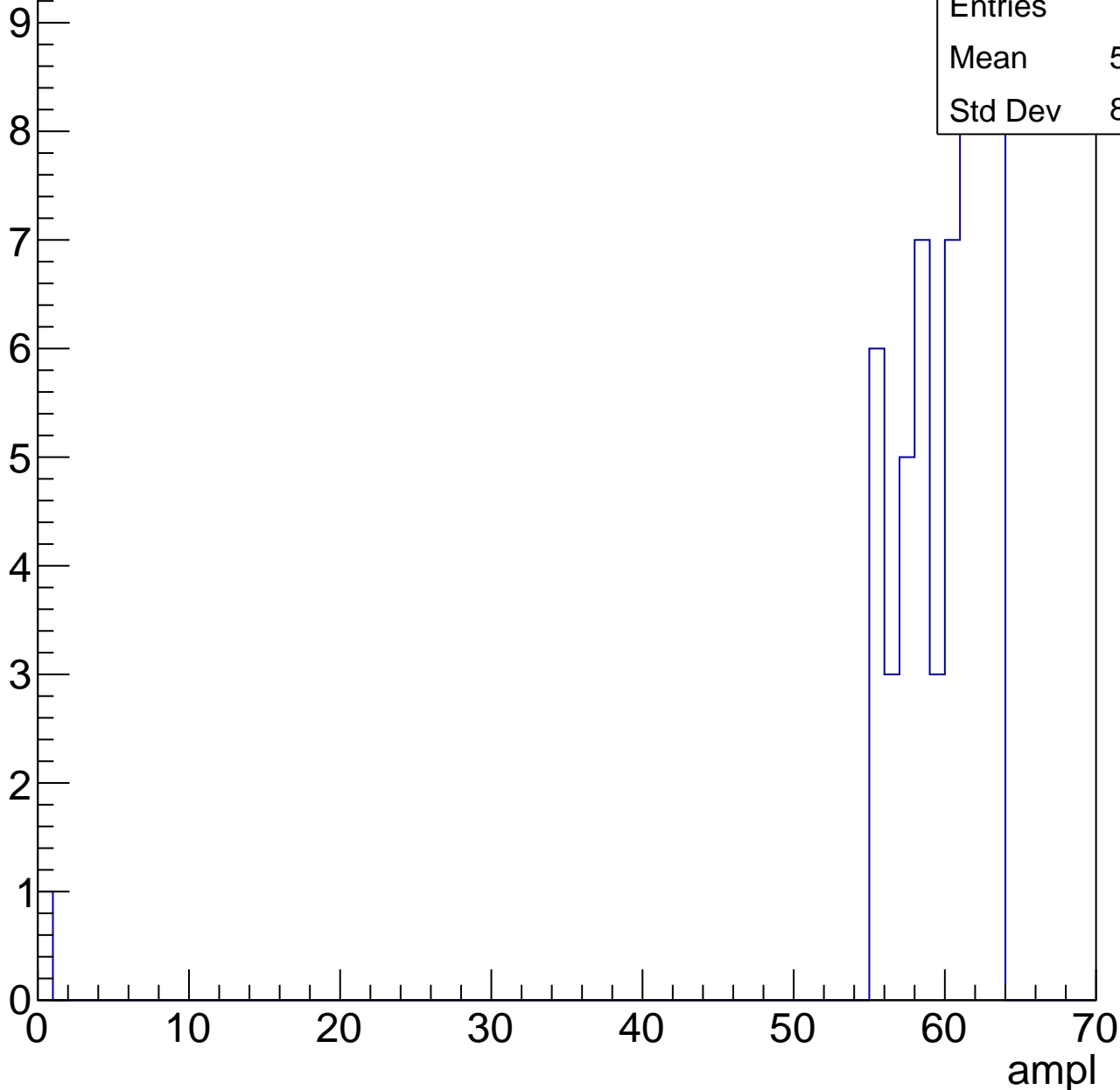


# B1L102S, U8-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	58.54
Std Dev	8.244



# B1L102S, U8-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

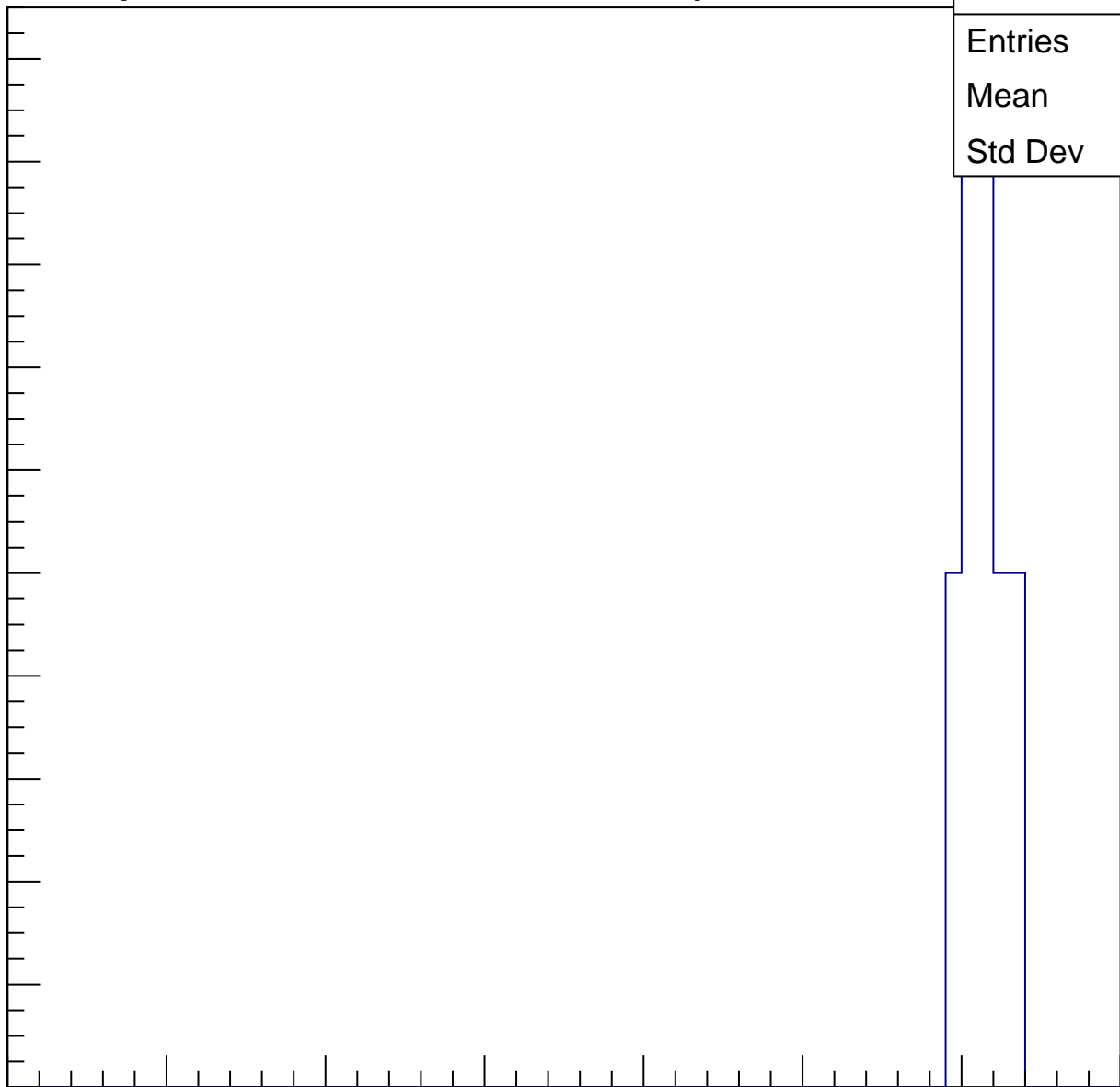
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	60.86
Std Dev	1.245

0 10 20 30 40 50 60 70

ampl





# B1L102S, U8-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch16, adc0

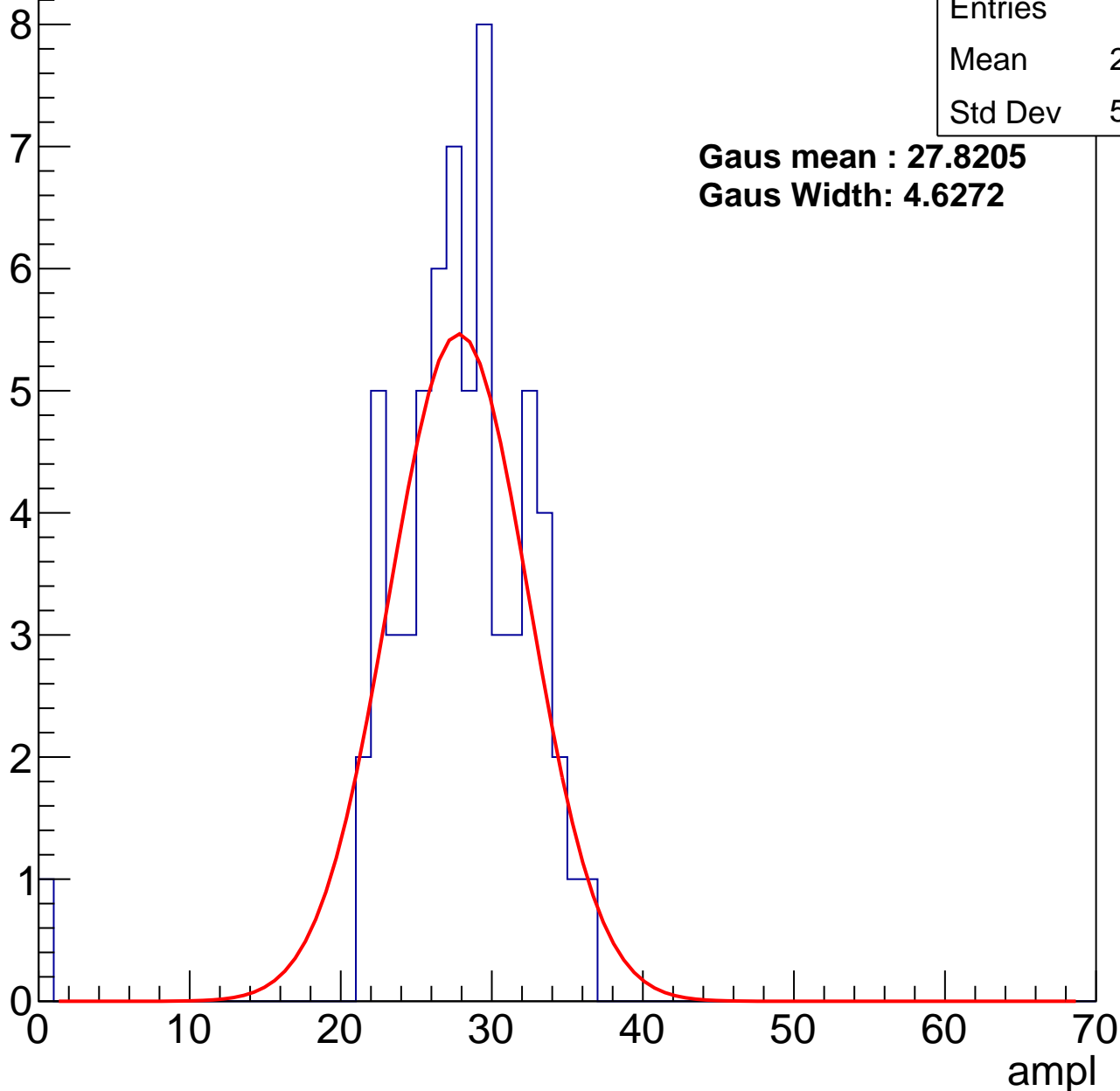
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	27.33
Std Dev	5.068

**Gaus mean : 27.8205**

**Gaus Width: 4.6272**



# B1L102S, U8-ch16, adc1

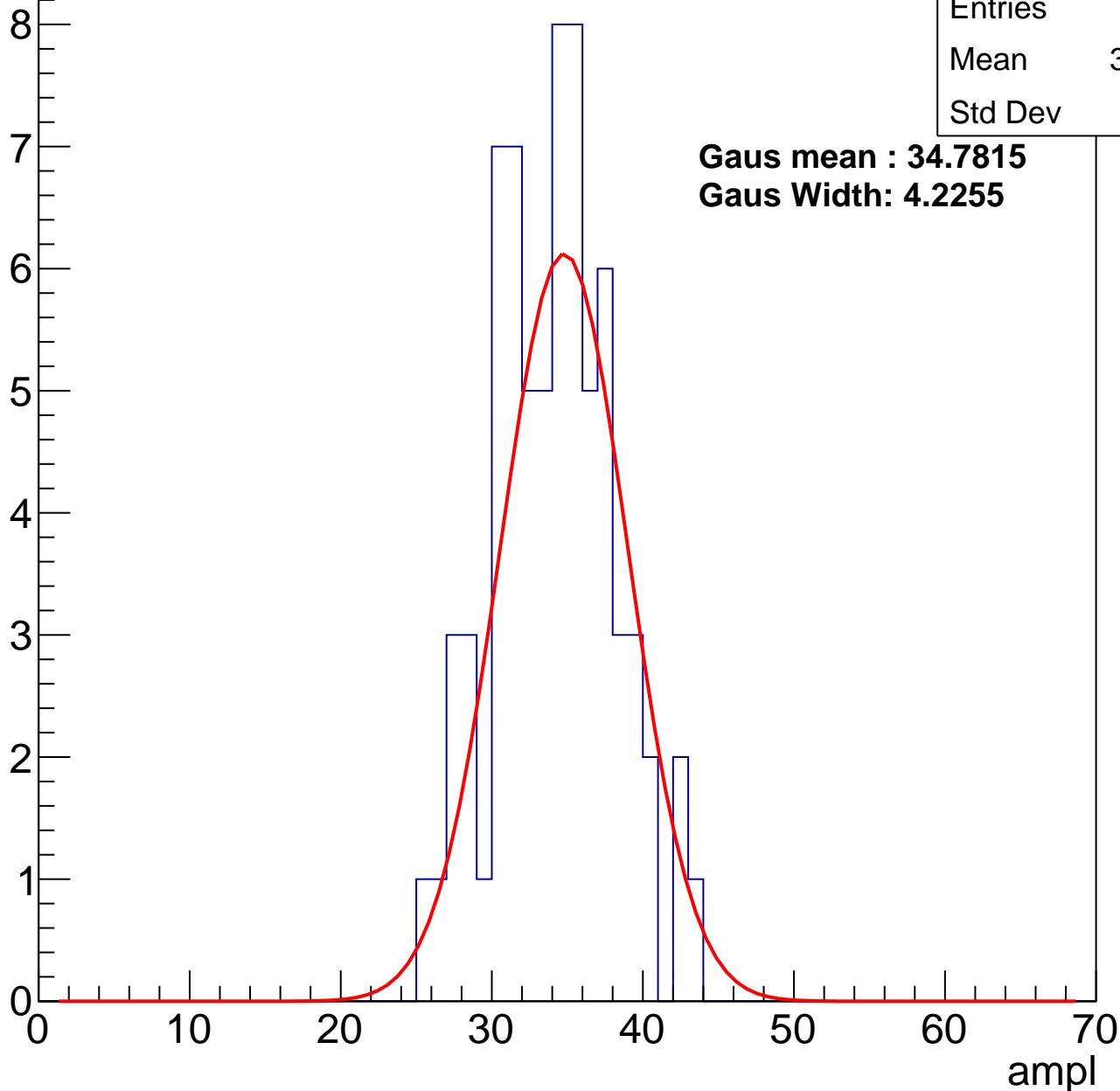
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	33.65
Std Dev	3.94

**Gaus mean : 34.7815**

**Gaus Width: 4.2255**



# B1L102S, U8-ch16, adc2

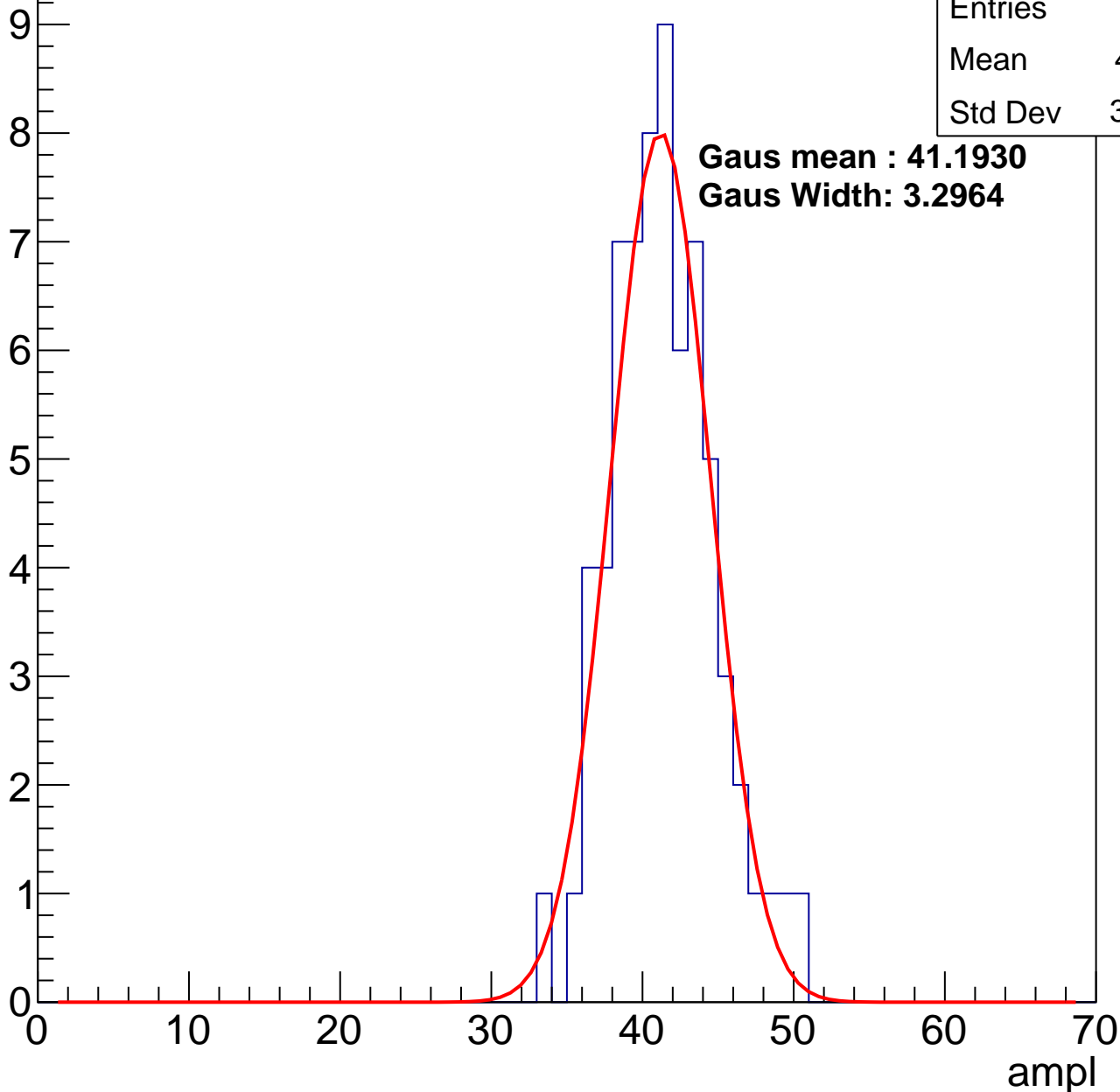
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	40.91
Std Dev	3.364

**Gaus mean : 41.1930**

**Gaus Width: 3.2964**

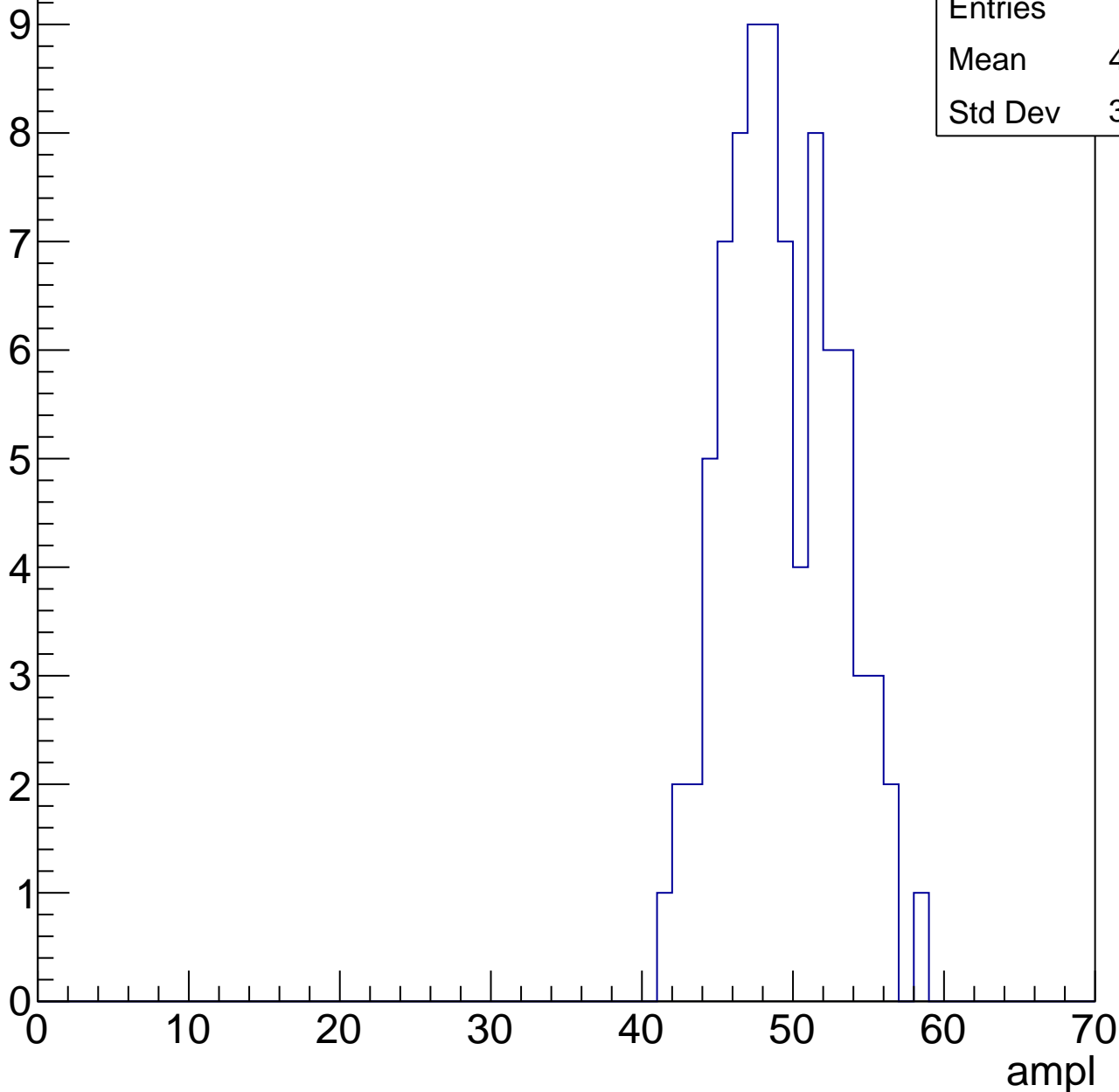


# B1L102S, U8-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	83
Mean	48.76
Std Dev	3.692

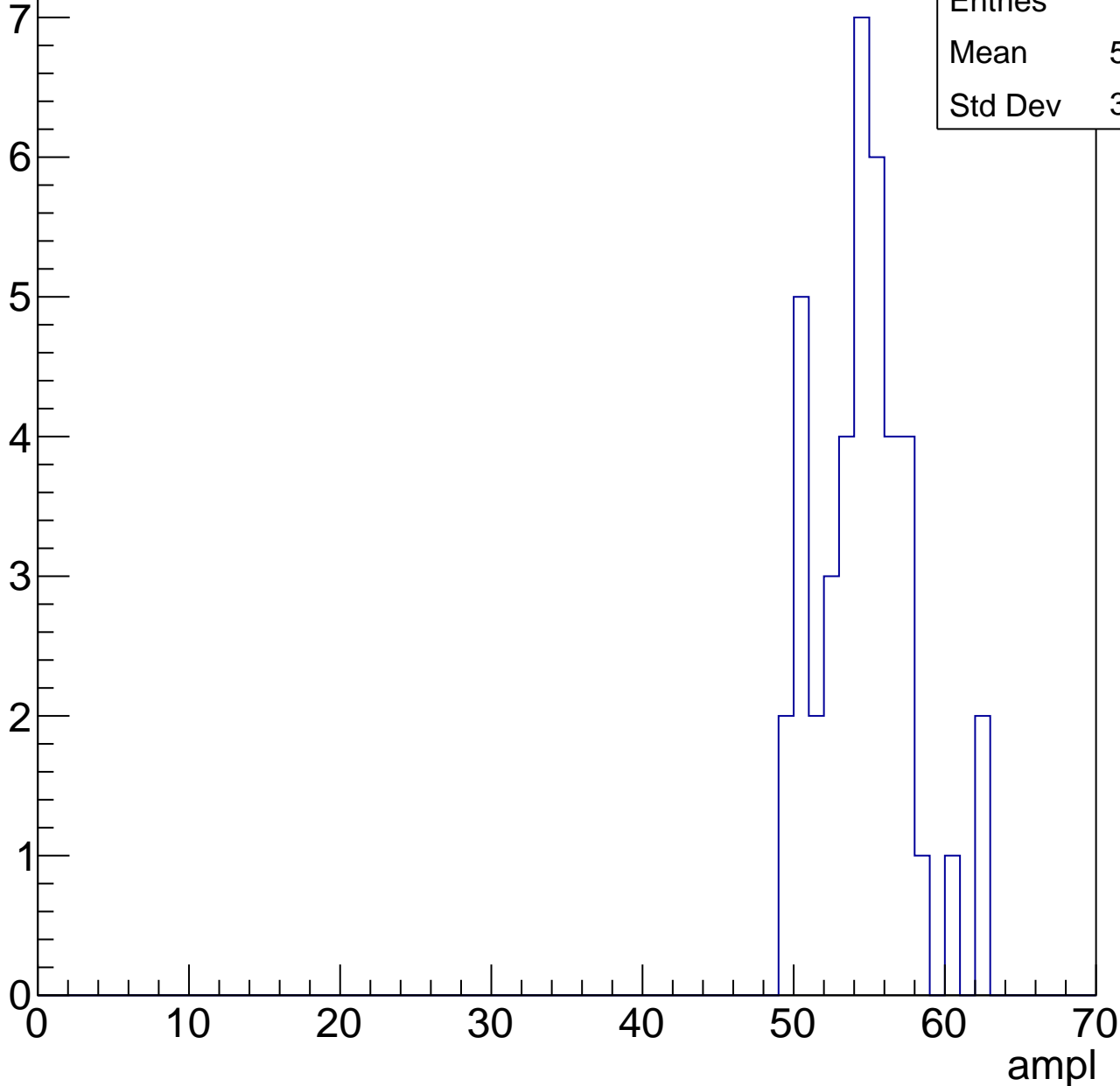


# B1L102S, U8-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	41
Mean	54.15
Std Dev	3.128

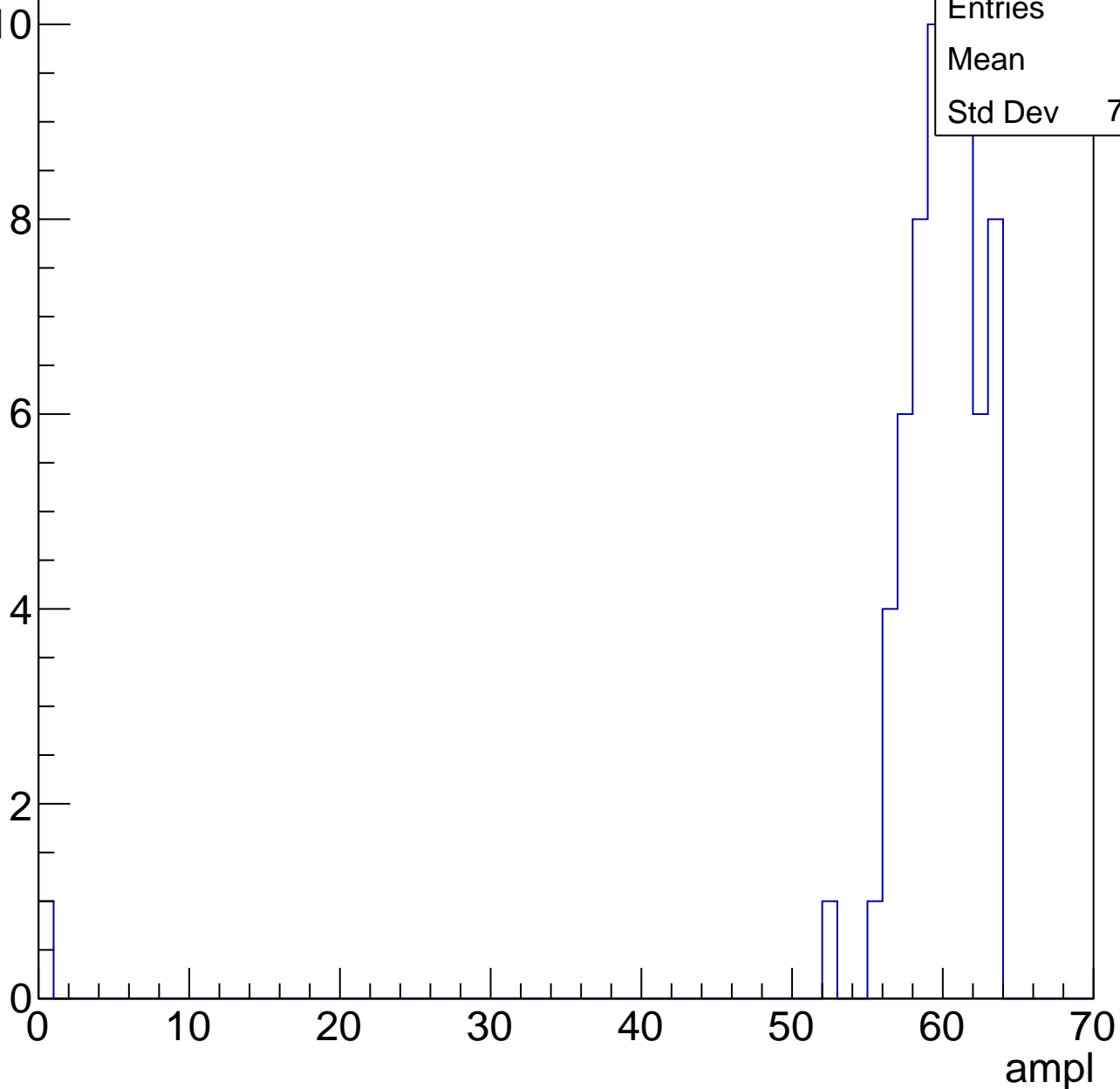


# B1L102S, U8-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	58.6
Std Dev	7.798



# B1L102S, U8-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	62.2
Std Dev	0.7483

ampl

0 10 20 30 40 50 60 70



# B1L102S, U8-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch17, adc0

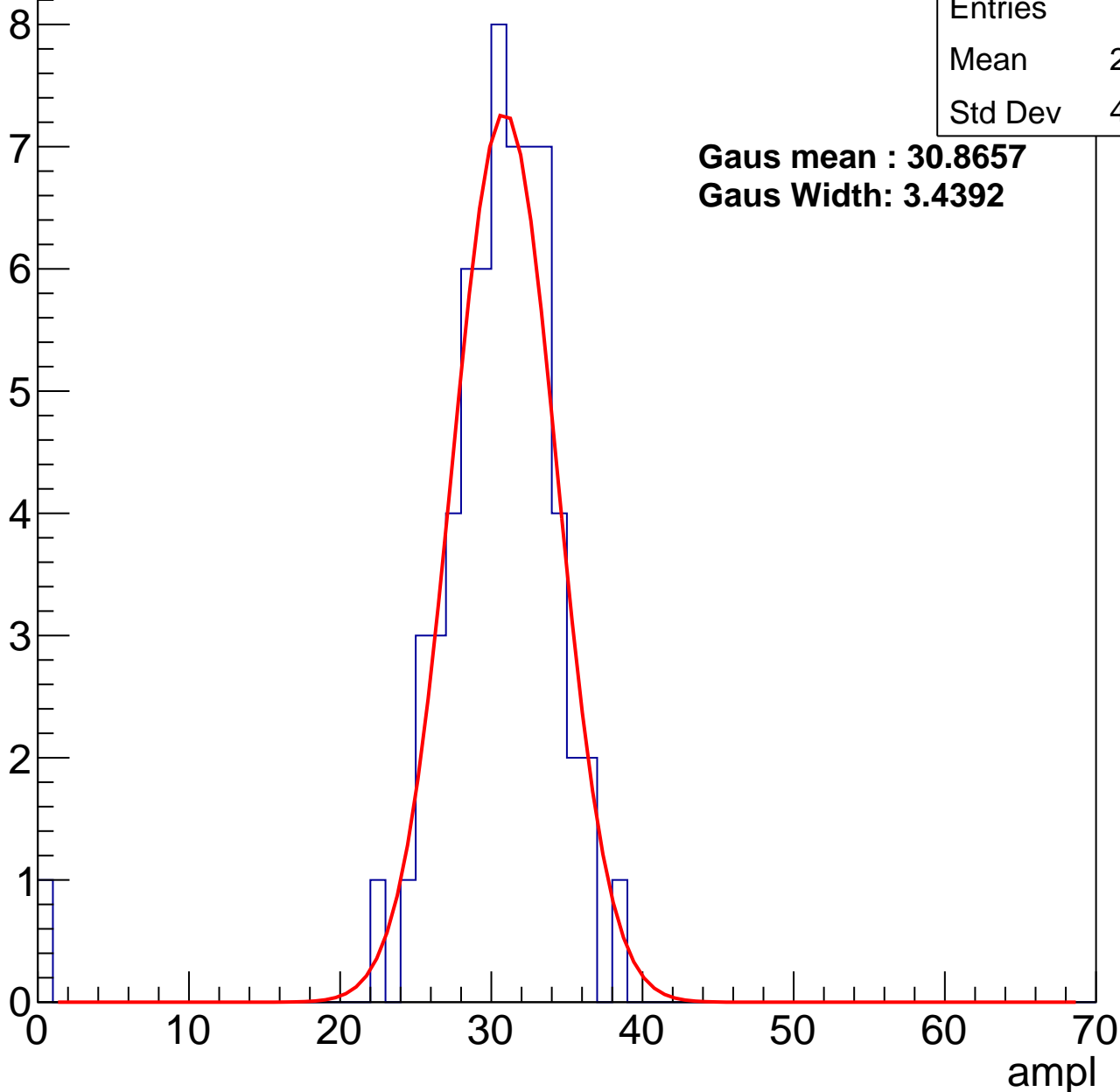
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	29.79
Std Dev	4.935

**Gaus mean : 30.8657**

**Gaus Width: 3.4392**



# B1L102S, U8-ch17, adc1

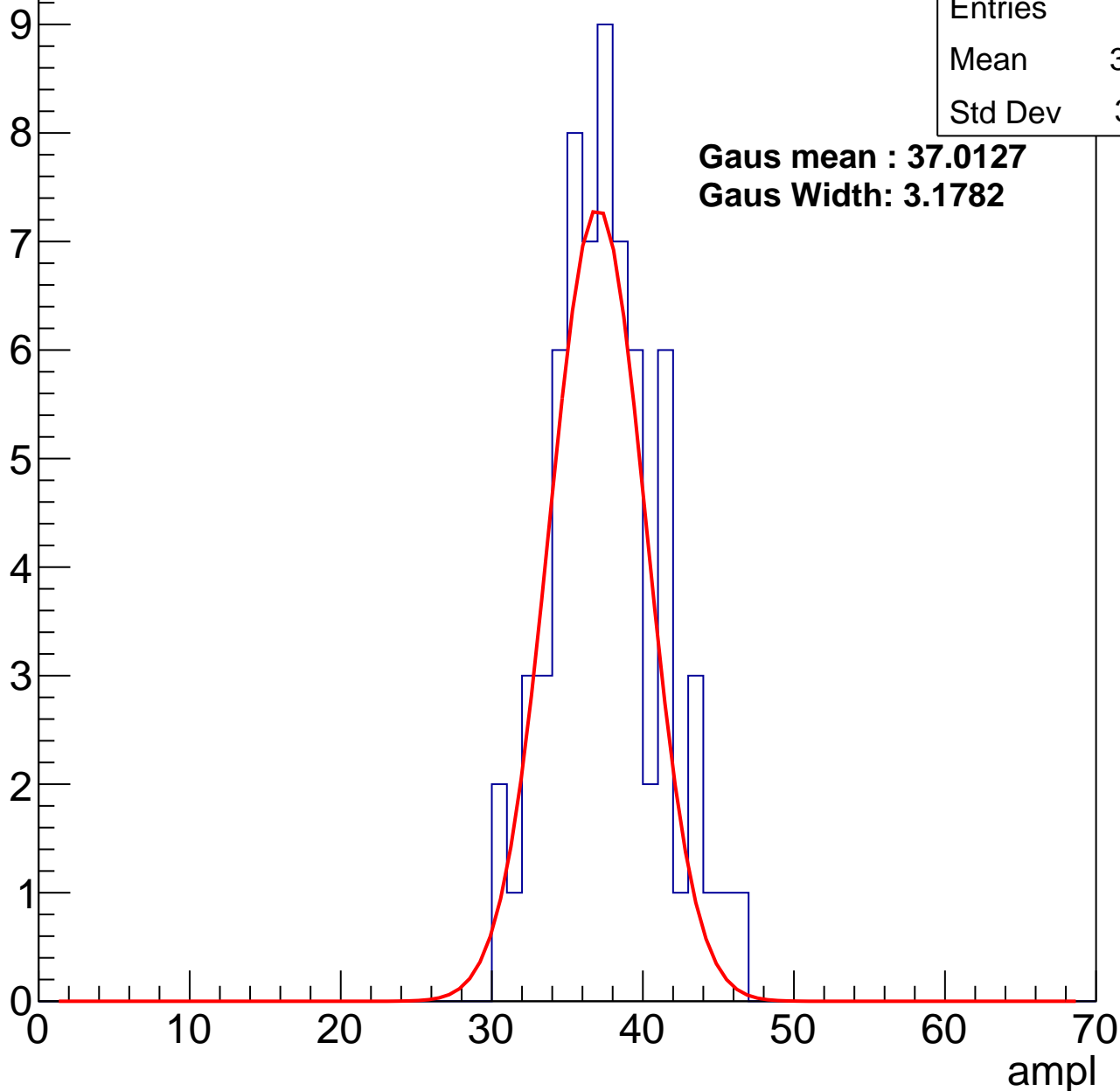
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	37.12
Std Dev	3.501

**Gaus mean : 37.0127**

**Gaus Width: 3.1782**



# B1L102S, U8-ch17, adc2

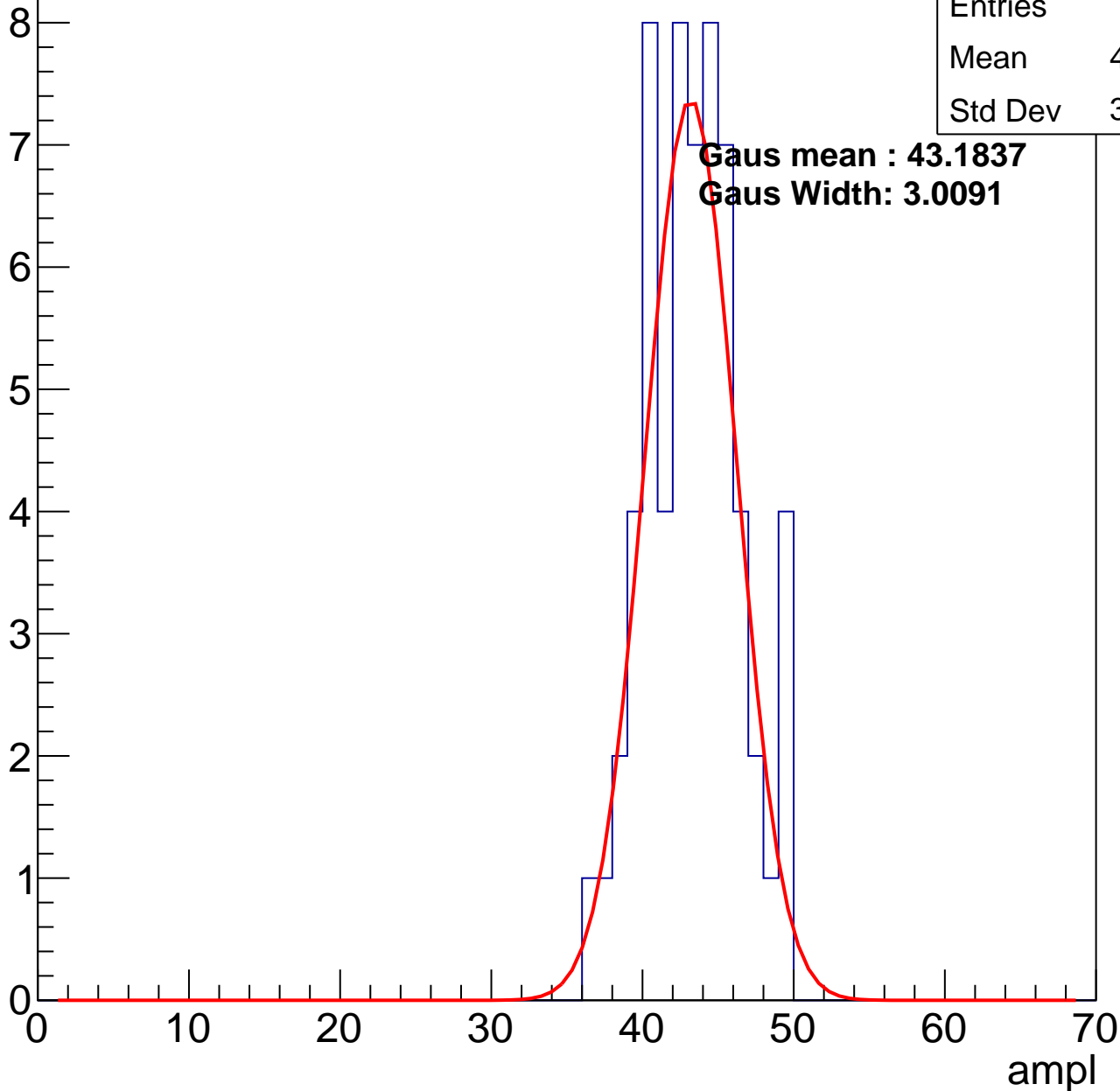
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	42.87
Std Dev	3.049

**Gaus mean : 43.1837**

**Gaus Width: 3.0091**

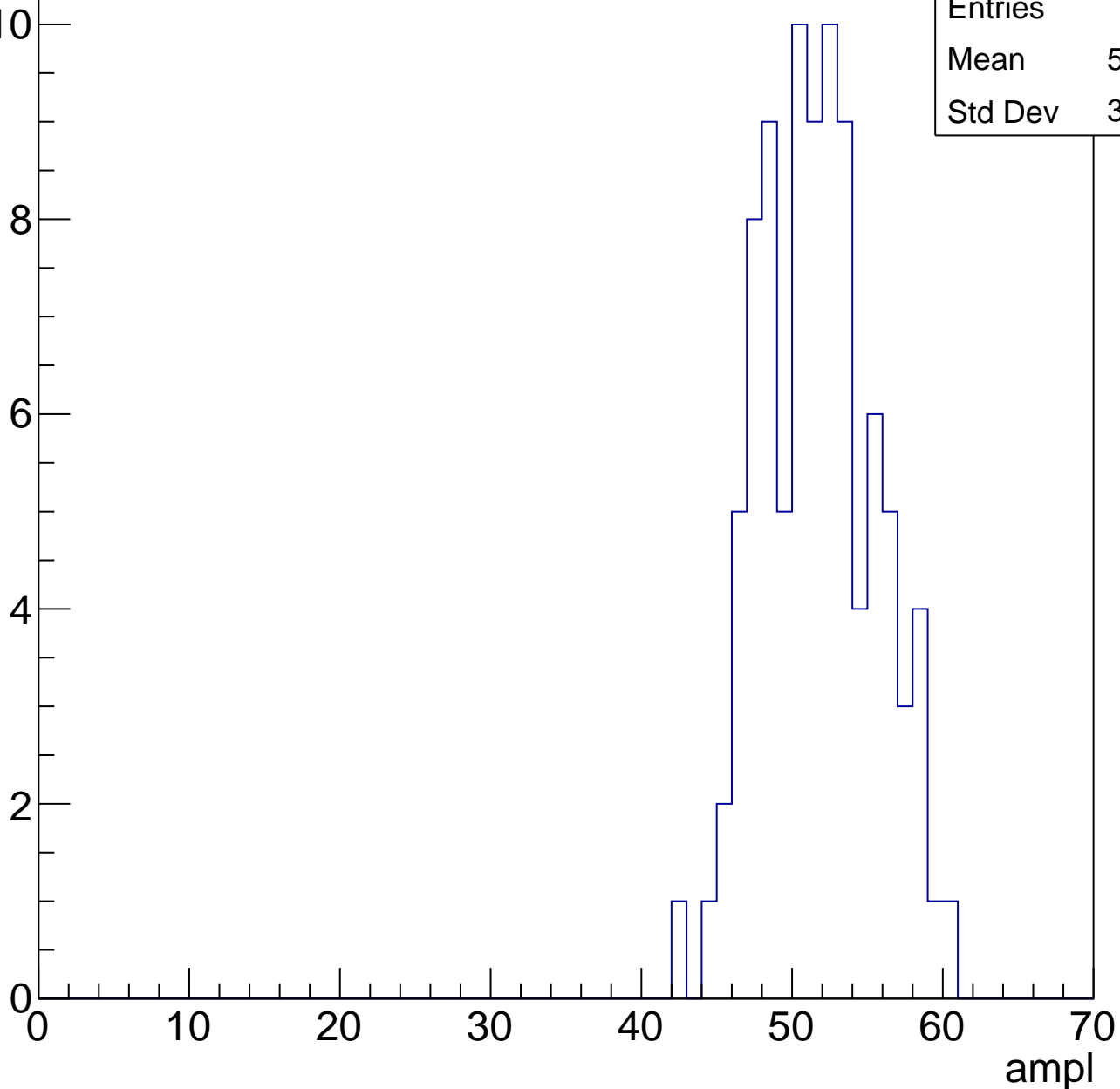


# B1L102S, U8-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	93
Mean	51.22
Std Dev	3.758

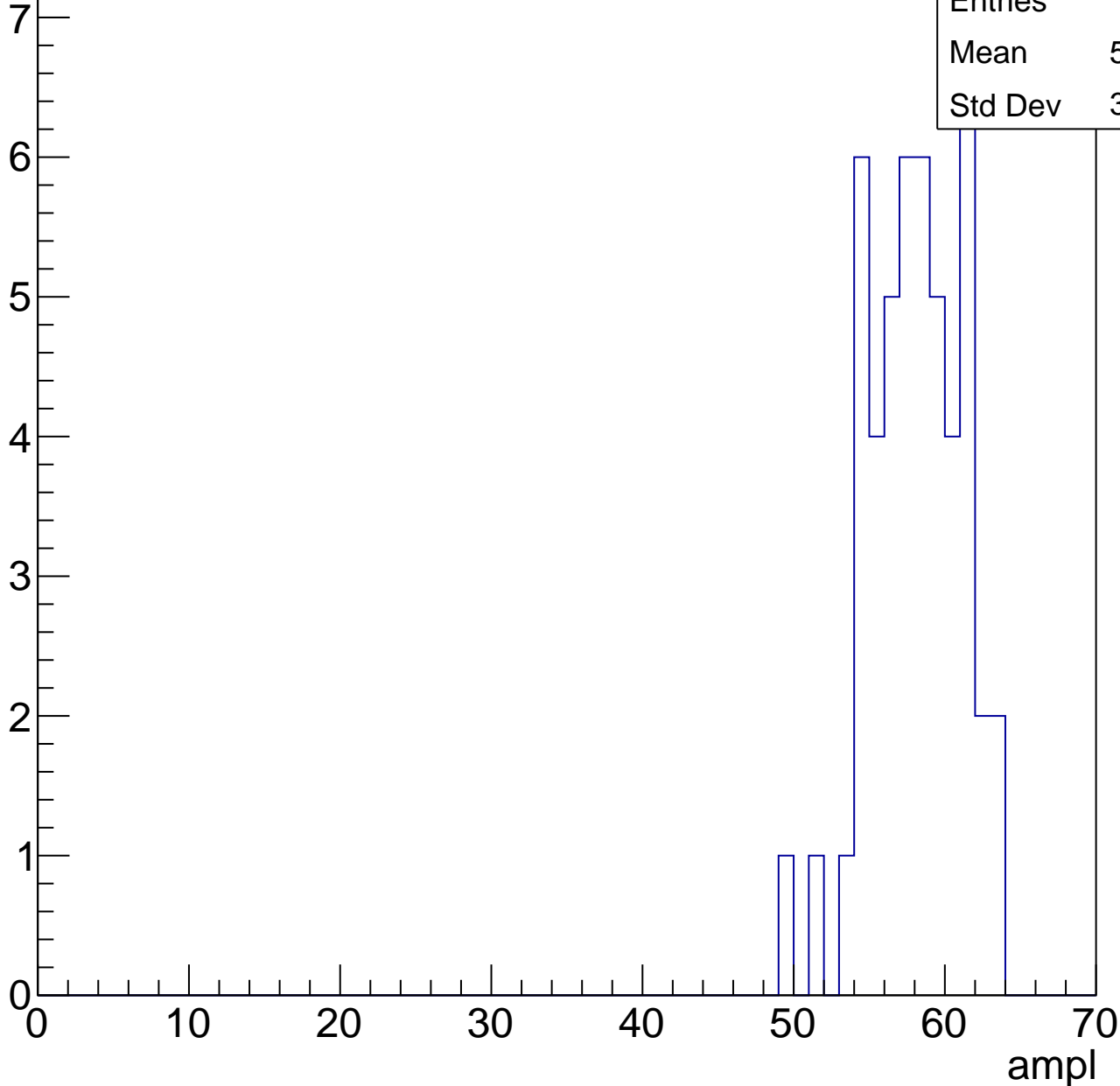


# B1L102S, U8-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	57.58
Std Dev	3.067

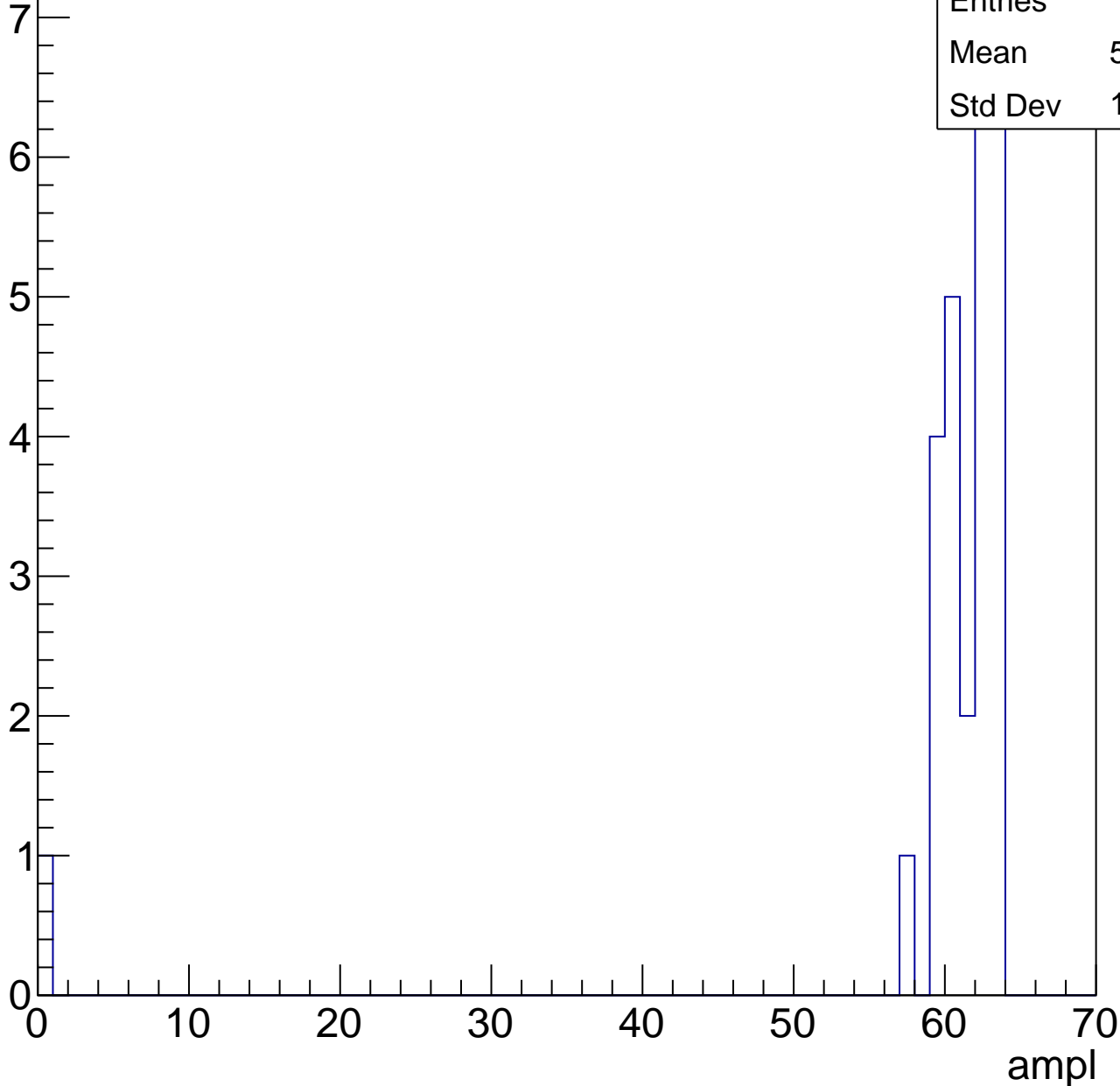


# B1L102S, U8-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	27
Mean	58.89
Std Dev	11.66



# B1L102S, U8-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch18, adc0

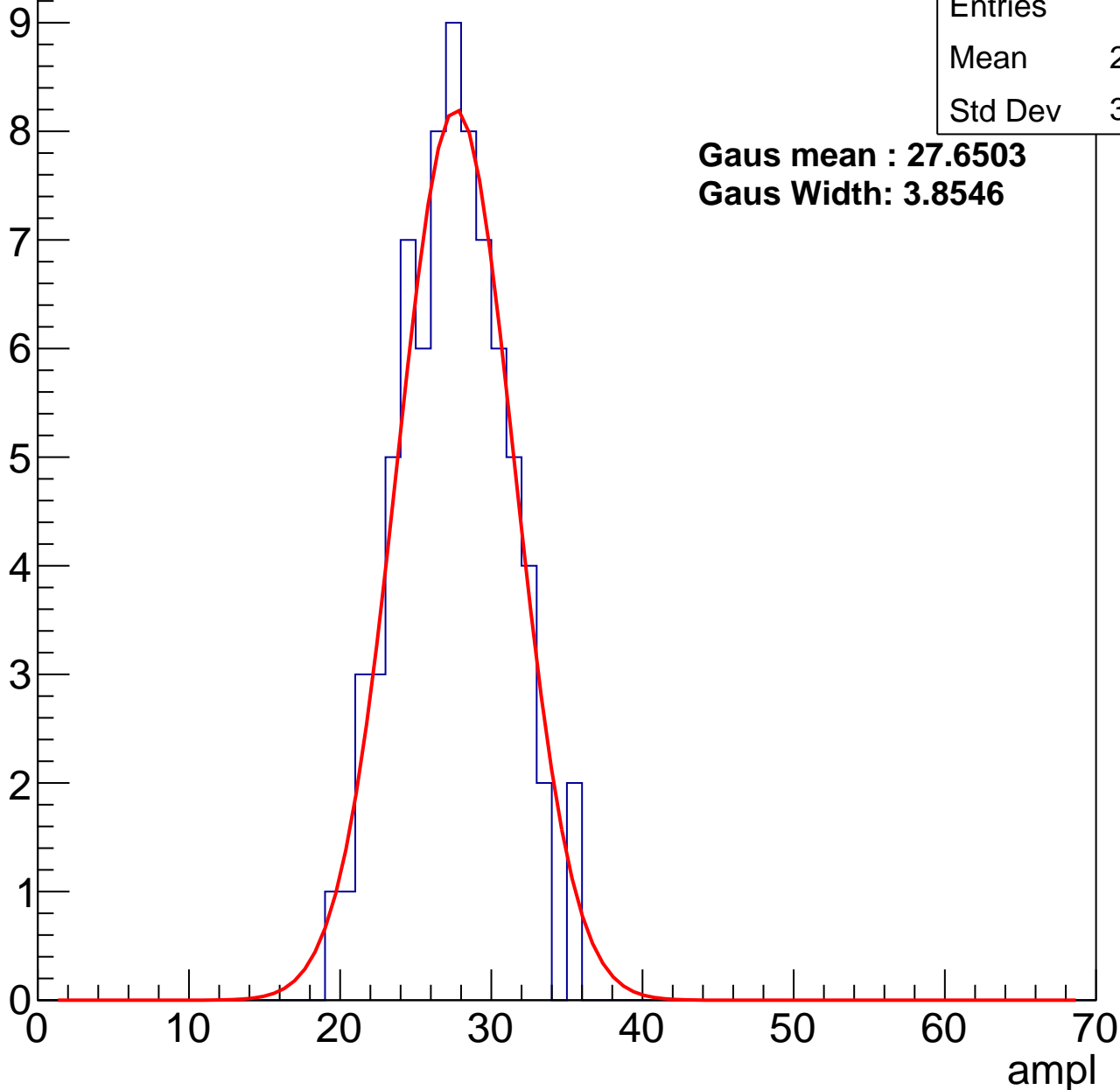
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	26.99
Std Dev	3.496

**Gaus mean : 27.6503**

**Gaus Width: 3.8546**



# B1L102S, U8-ch18, adc1

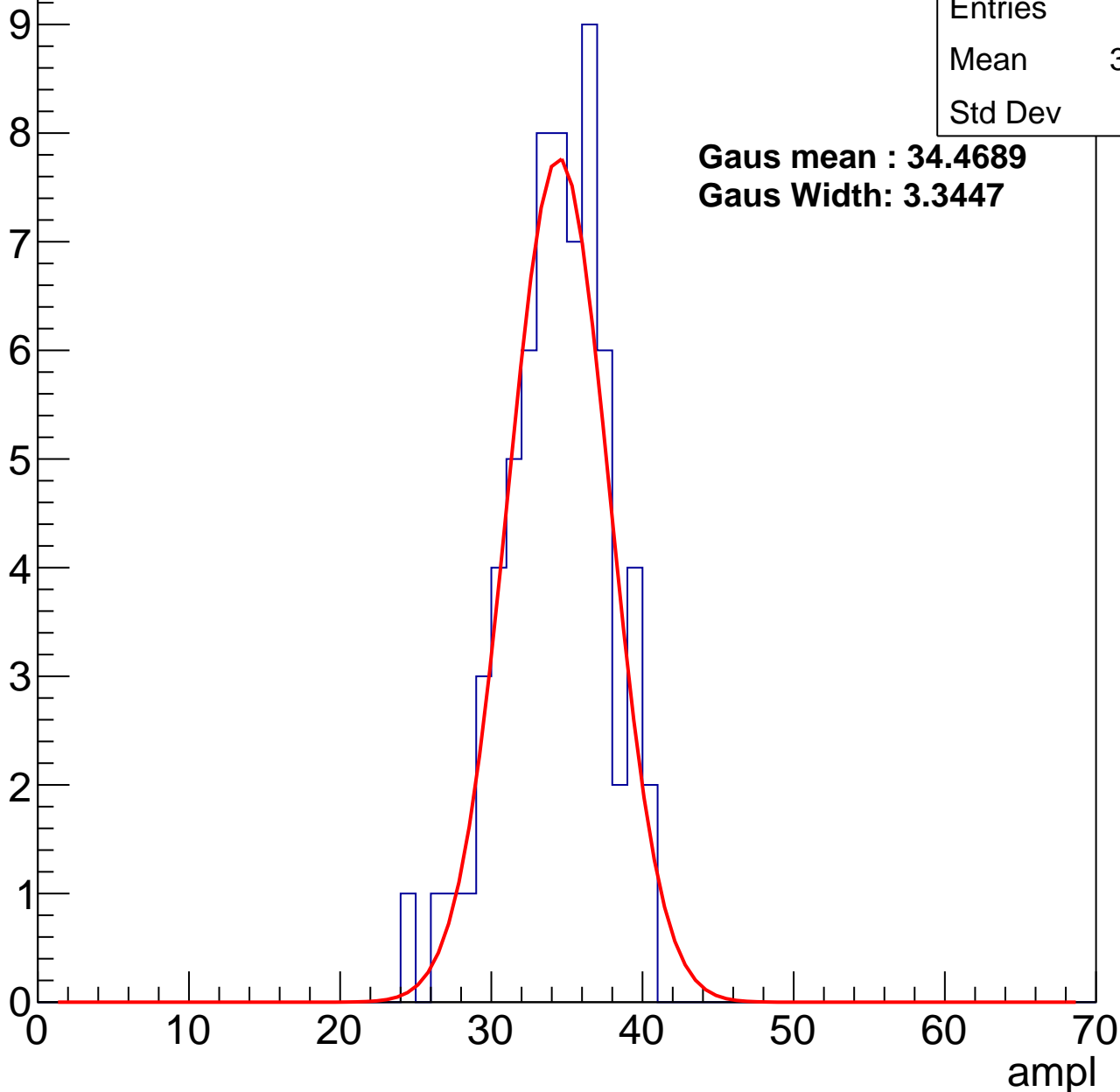
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	33.79
Std Dev	3.35

**Gaus mean : 34.4689**

**Gaus Width: 3.3447**



# B1L102S, U8-ch18, adc2

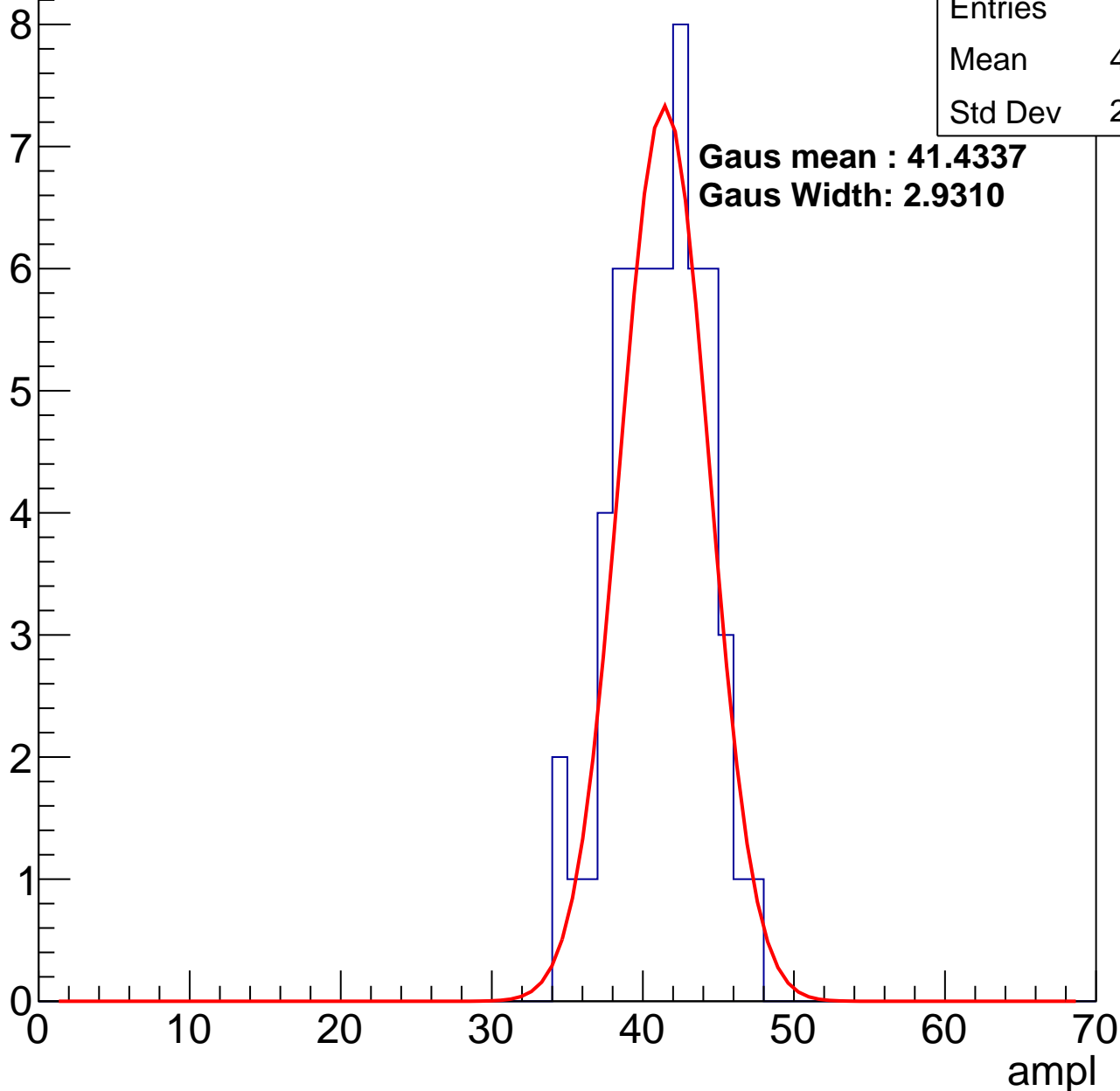
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	40.72
Std Dev	2.954

**Gaus mean : 41.4337**

**Gaus Width: 2.9310**



# B1L102S, U8-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

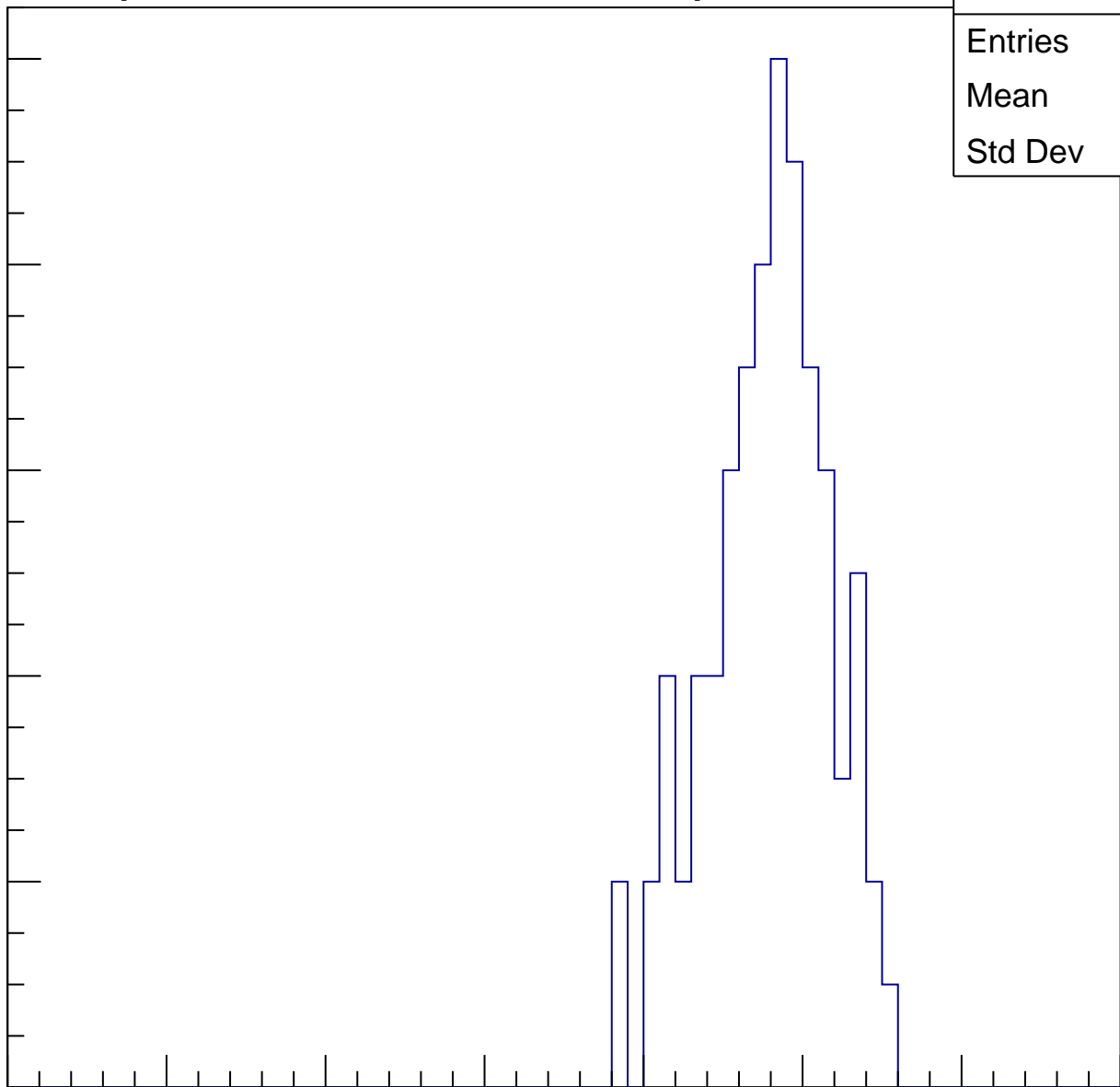
Entries	82
Mean	47.33
Std Dev	3.822

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

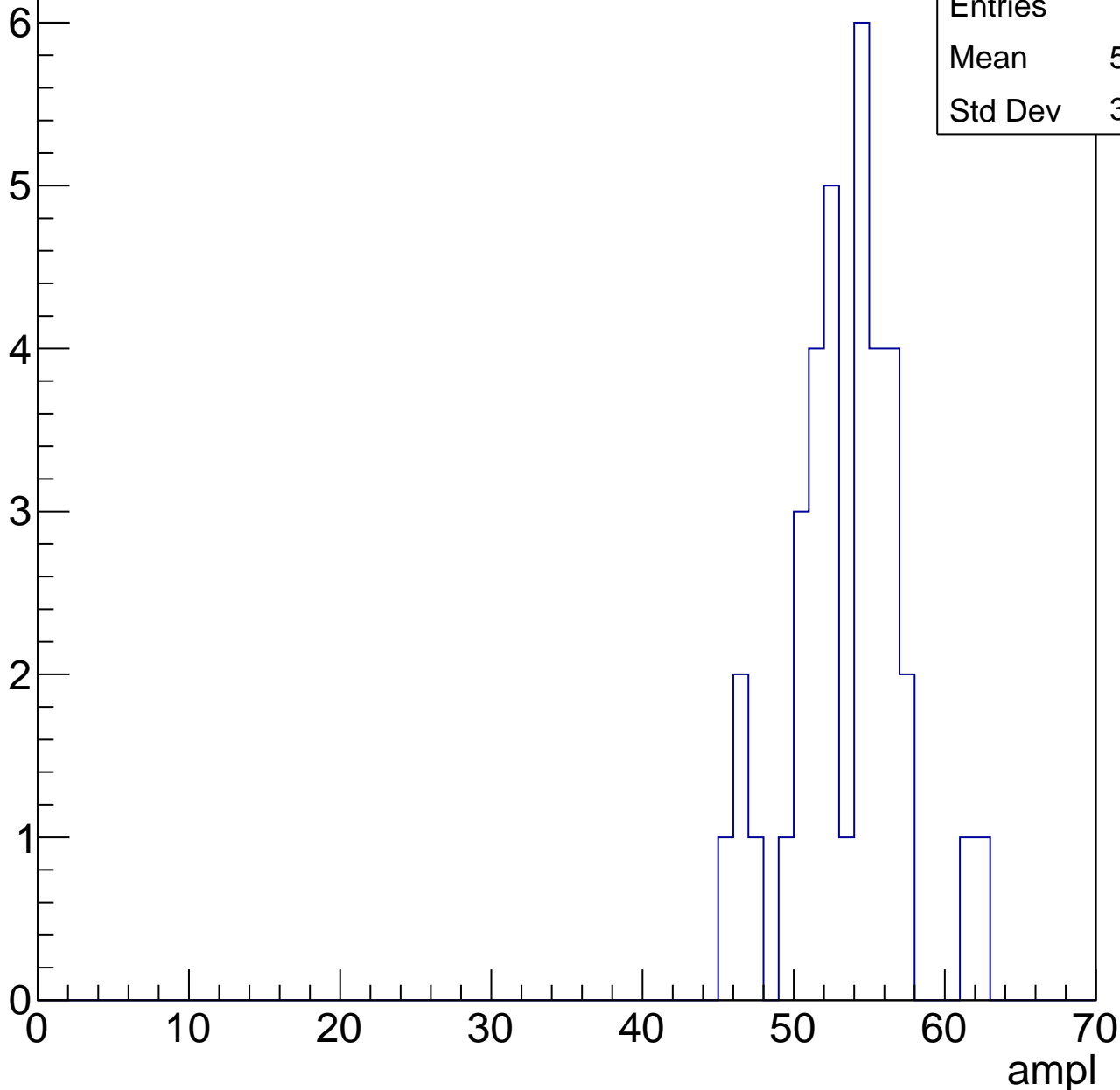


# B1L102S, U8-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	36
Mean	52.92
Std Dev	3.715



# B1L102S, U8-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

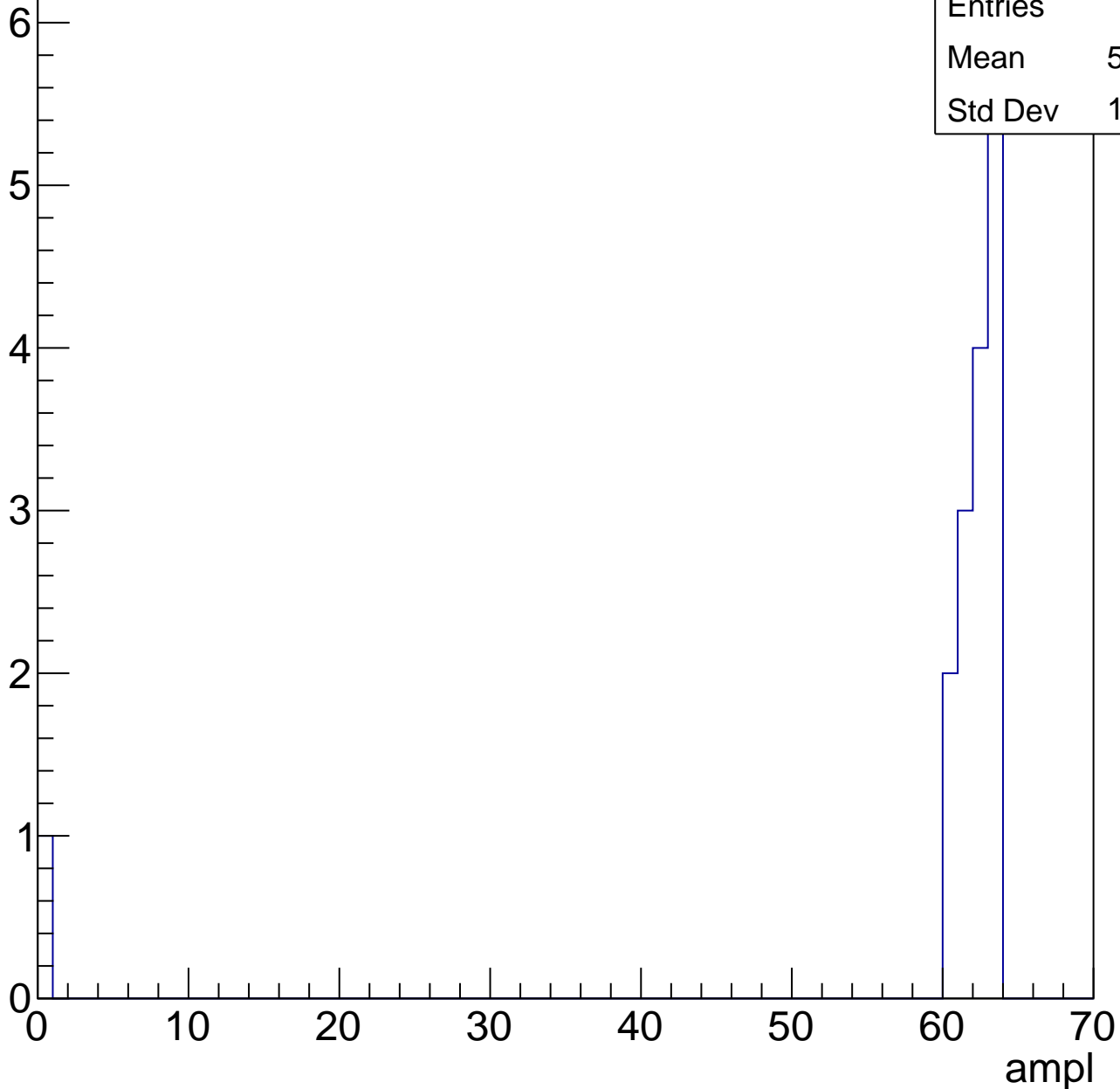
Entries	69
Mean	58.07
Std Dev	2.799

# B1L102S, U8-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	16
Mean	58.06
Std Dev	15.03

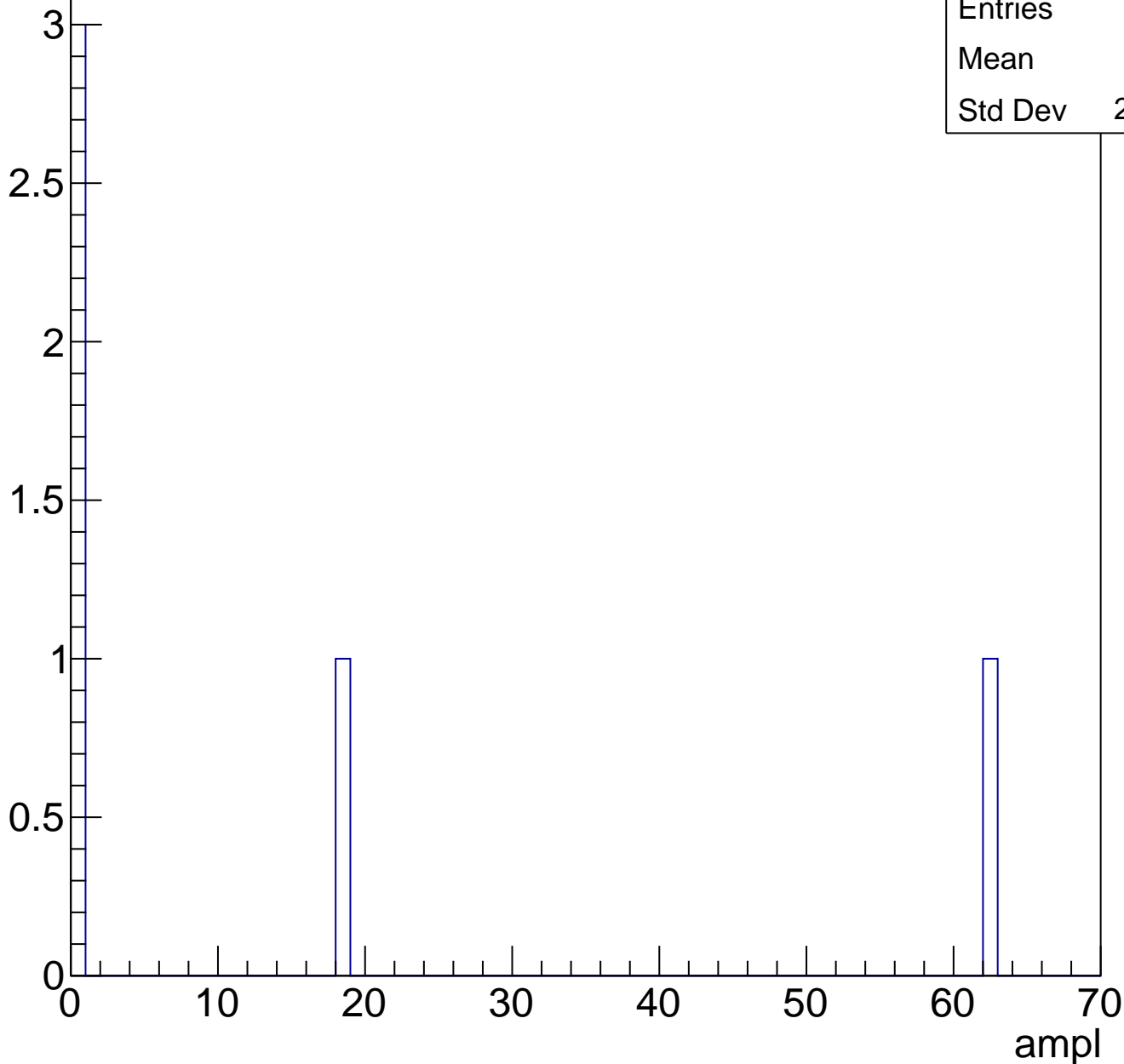




# B1L102S, U8-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

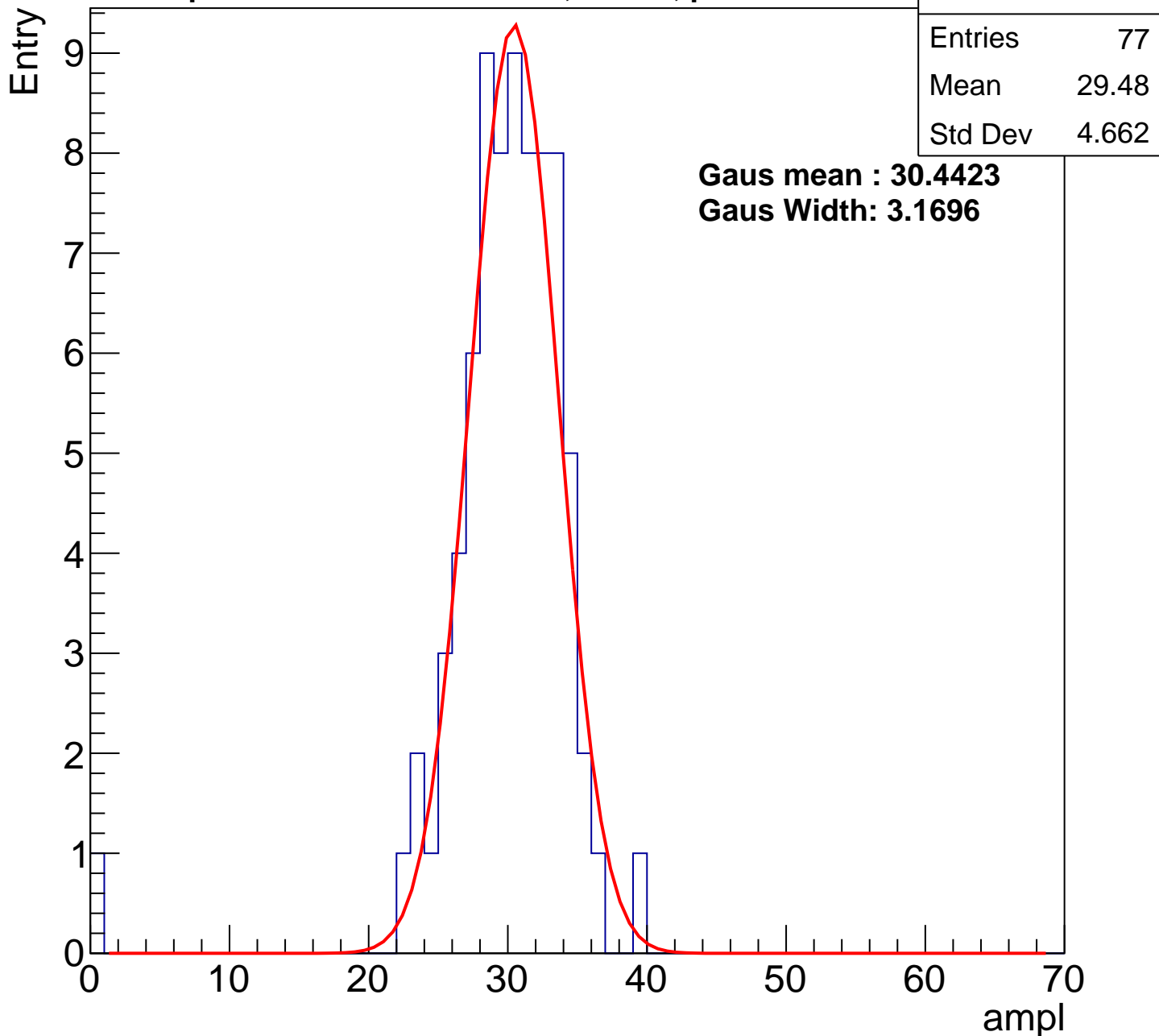
Entry



Entries	5
Mean	16
Std Dev	24.03

# B1L102S, U8-ch19, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U8-ch19, adc1

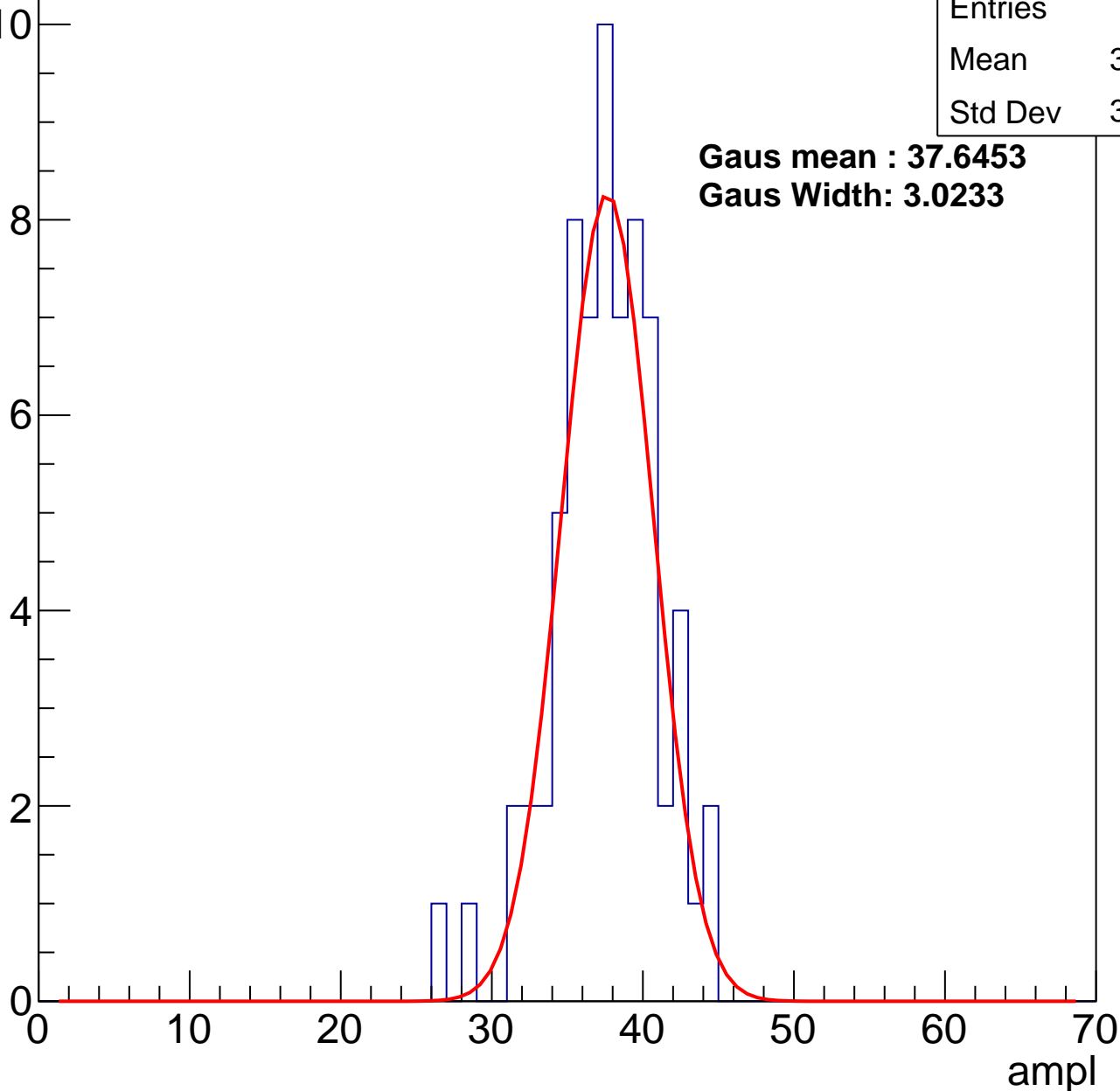
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	37.06
Std Dev	3.422

**Gaus mean : 37.6453**

**Gaus Width: 3.0233**



# B1L102S, U8-ch19, adc2

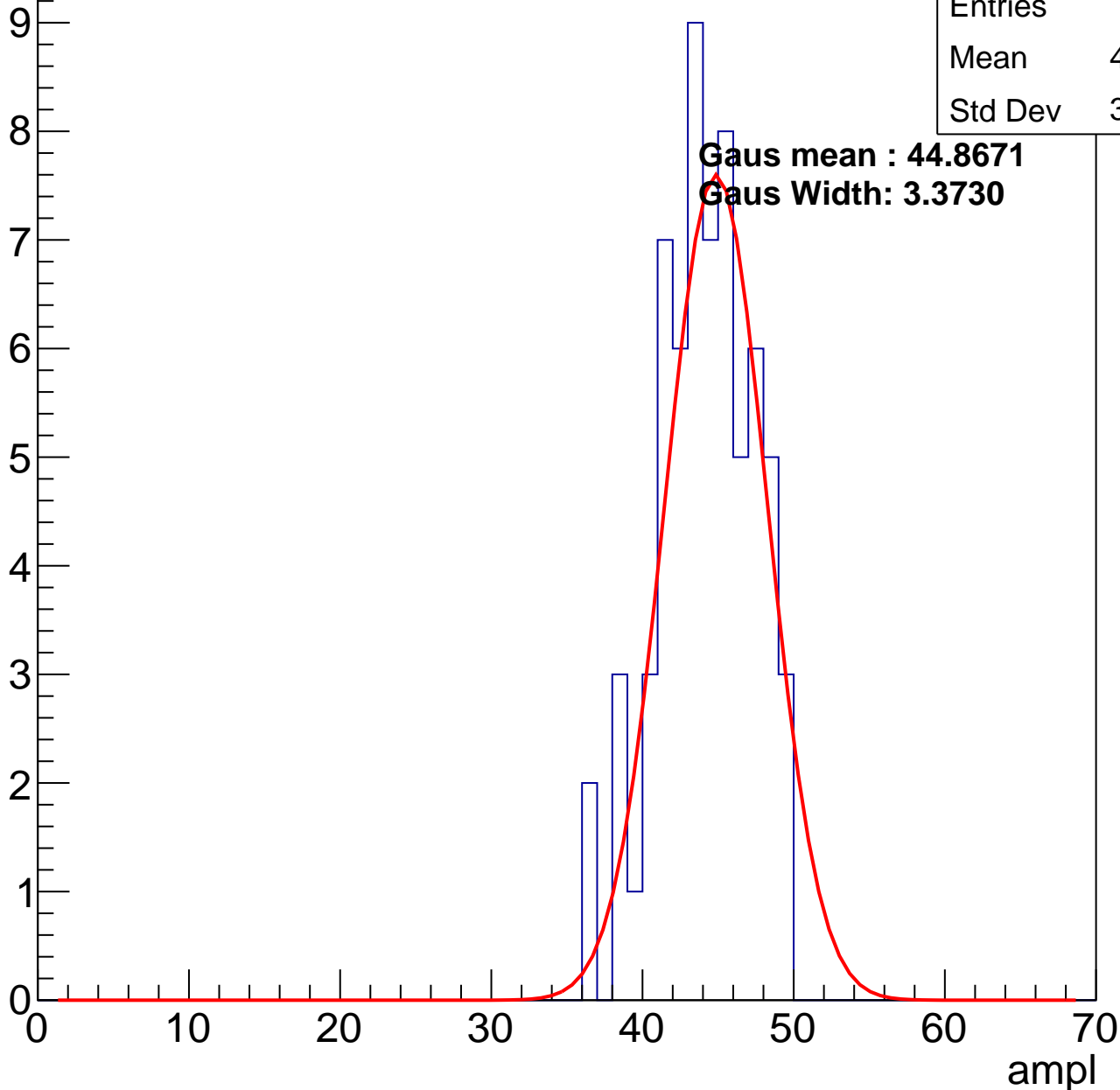
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	43.66
Std Dev	3.124

**Gaus mean : 44.8671**

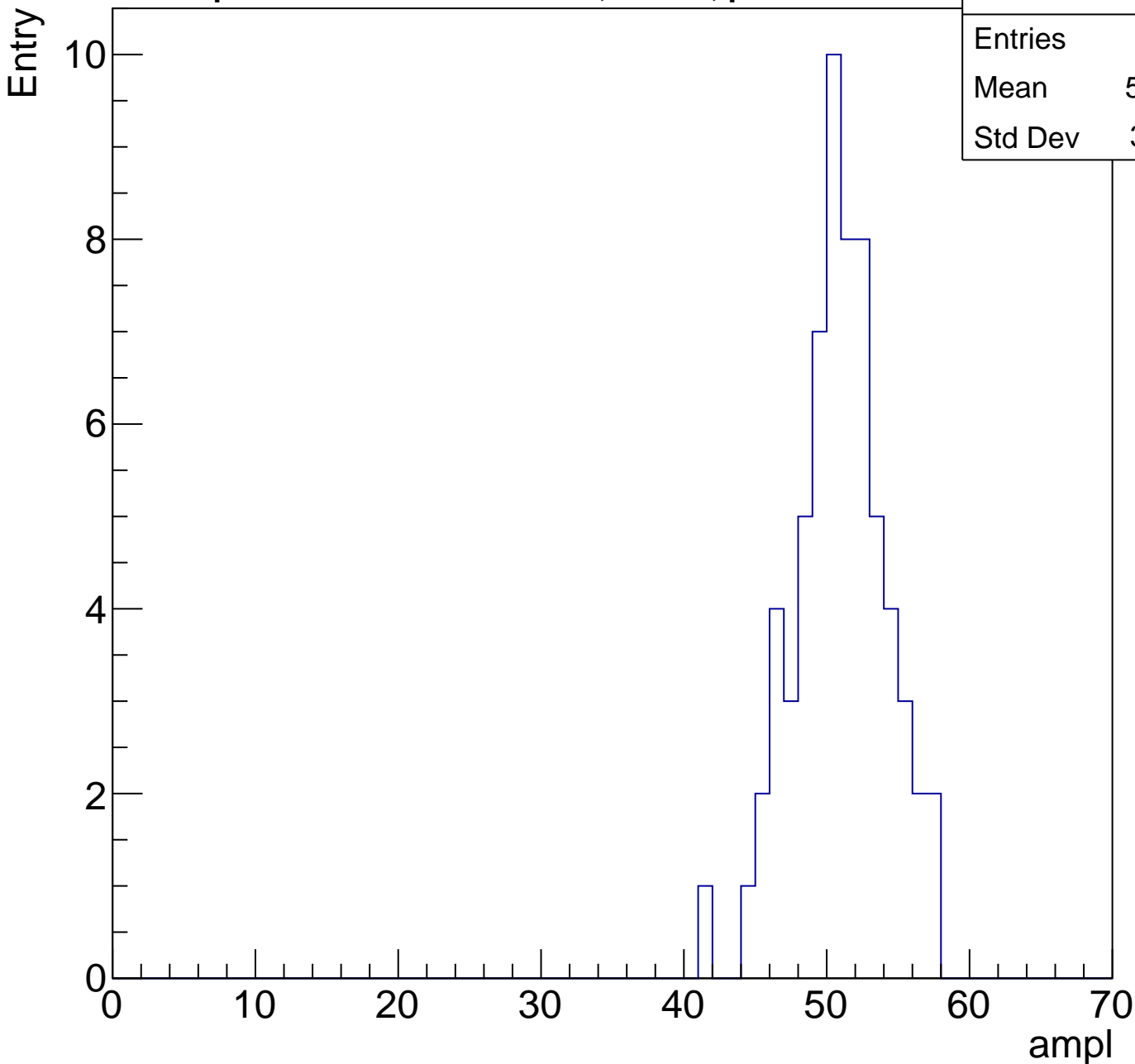
**Gaus Width: 3.3730**



# B1L102S, U8-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	65
Mean	50.45
Std Dev	3.201

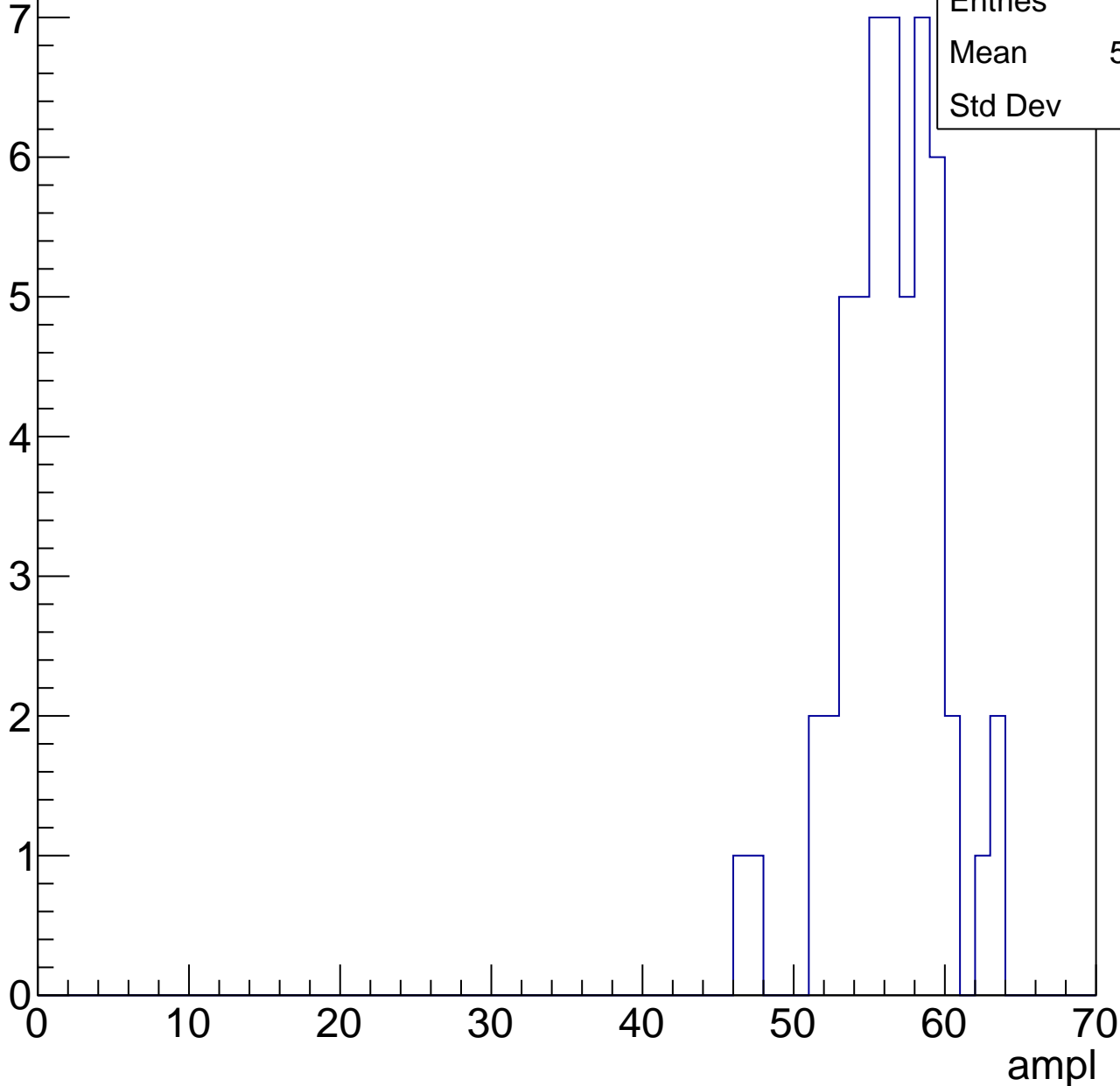


# B1L102S, U8-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	55.92
Std Dev	3.33

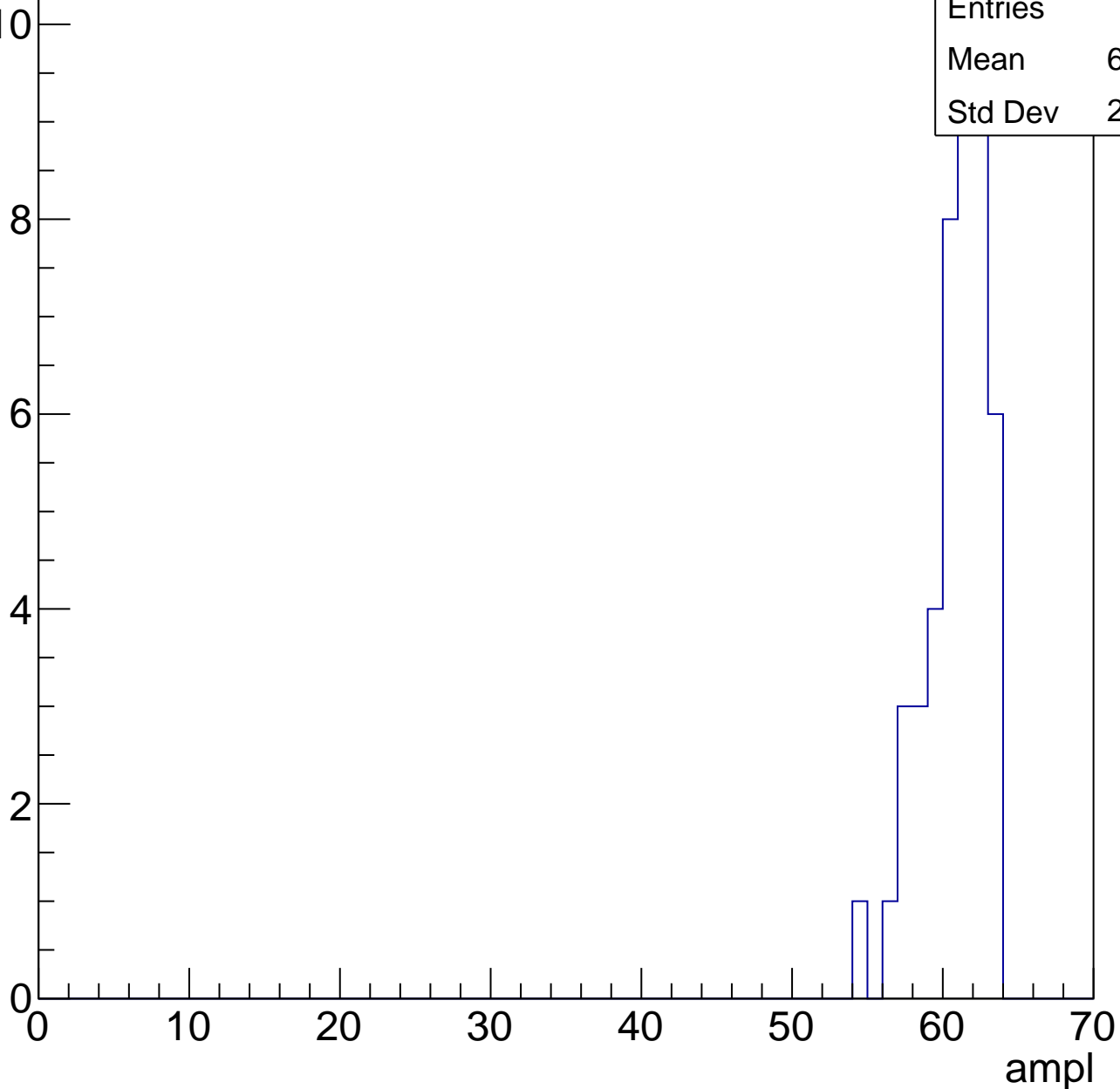


# B1L102S, U8-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	60.38
Std Dev	2.047



# B1L102S, U8-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch20, adc0

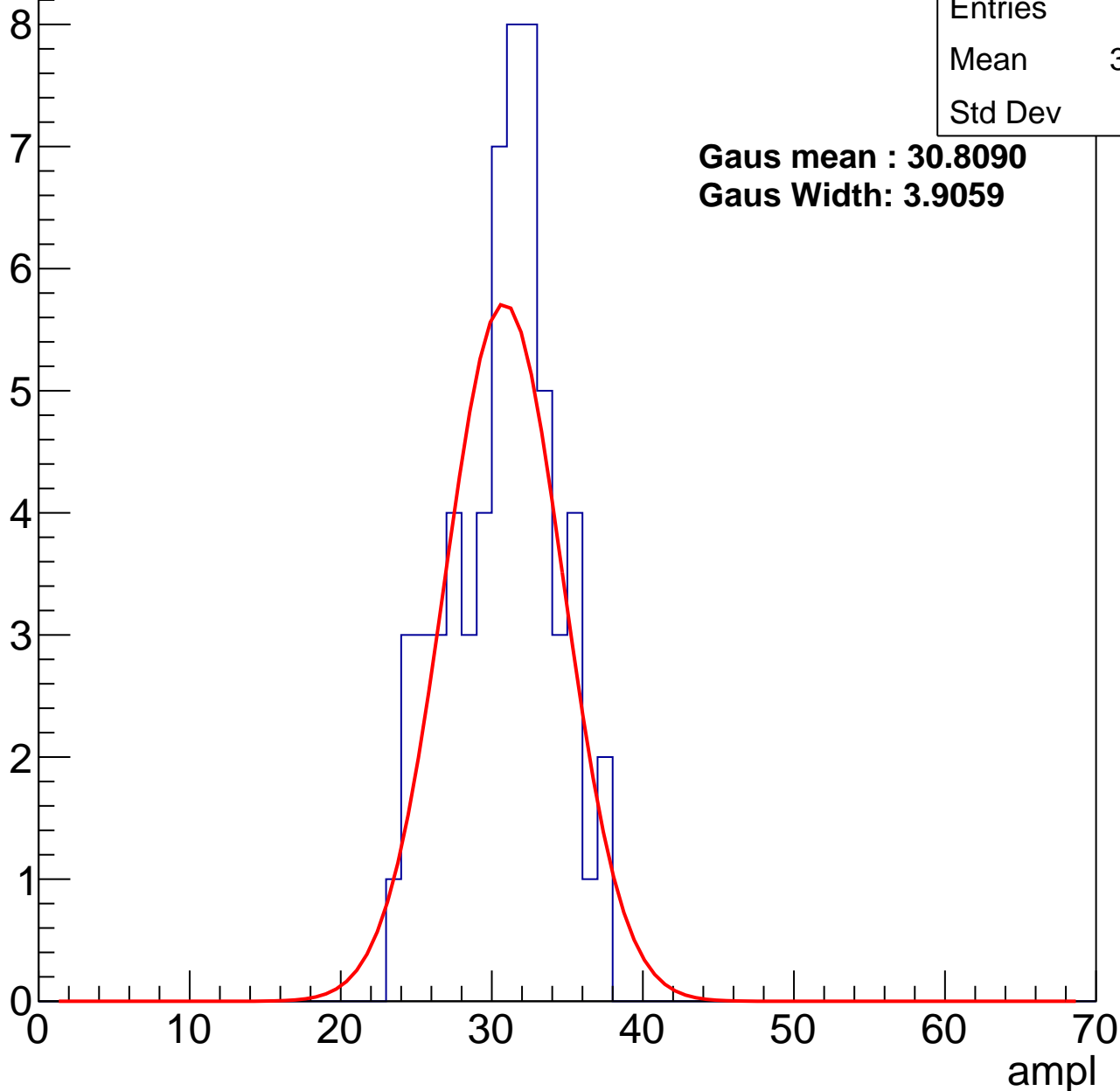
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	30.29
Std Dev	3.43

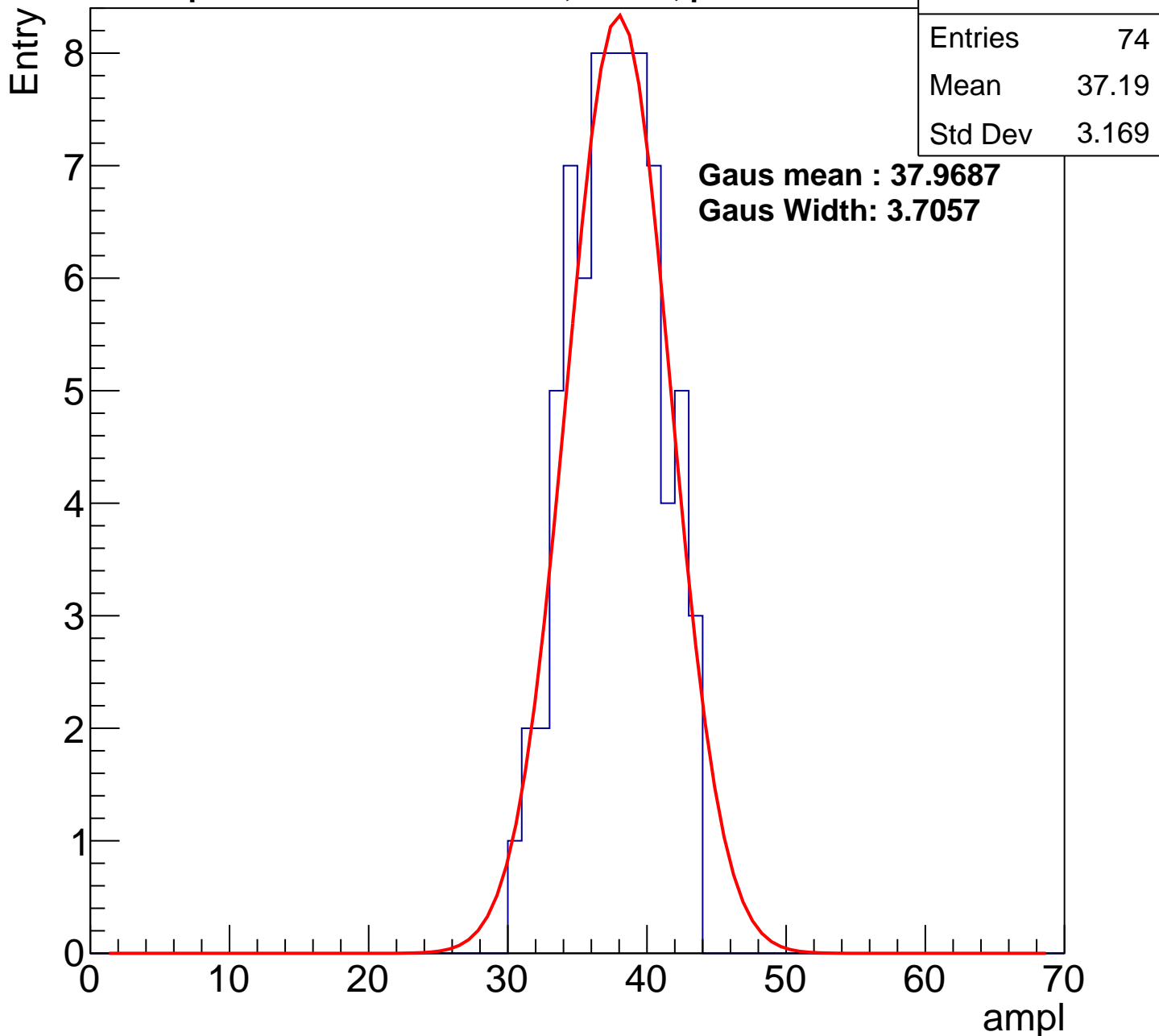
**Gaus mean : 30.8090**

**Gaus Width: 3.9059**



# B1L102S, U8-ch20, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U8-ch20, adc2

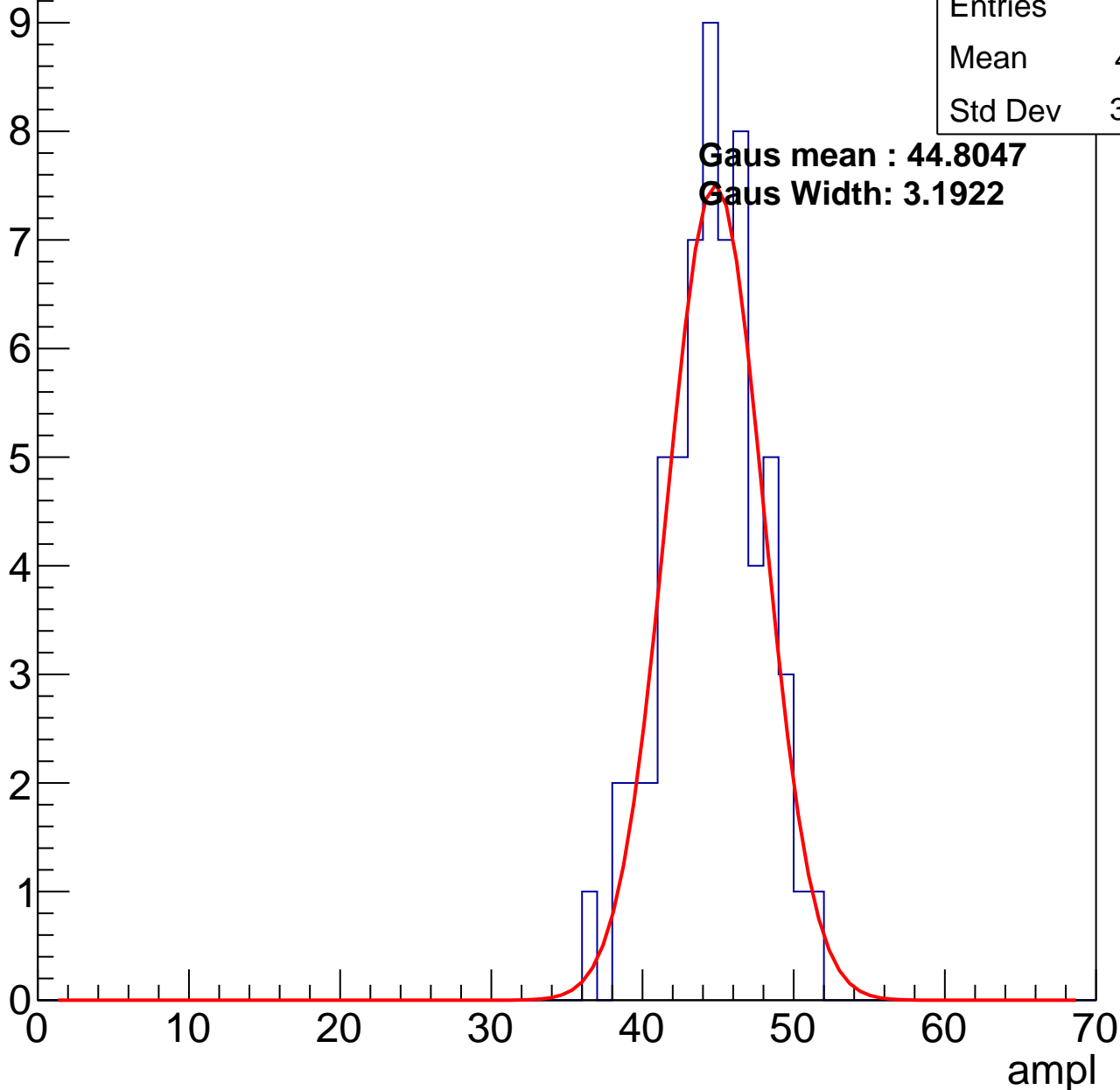
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	44.21
Std Dev	3.117

**Gaus mean : 44.8047**

**Gaus Width: 3.1922**

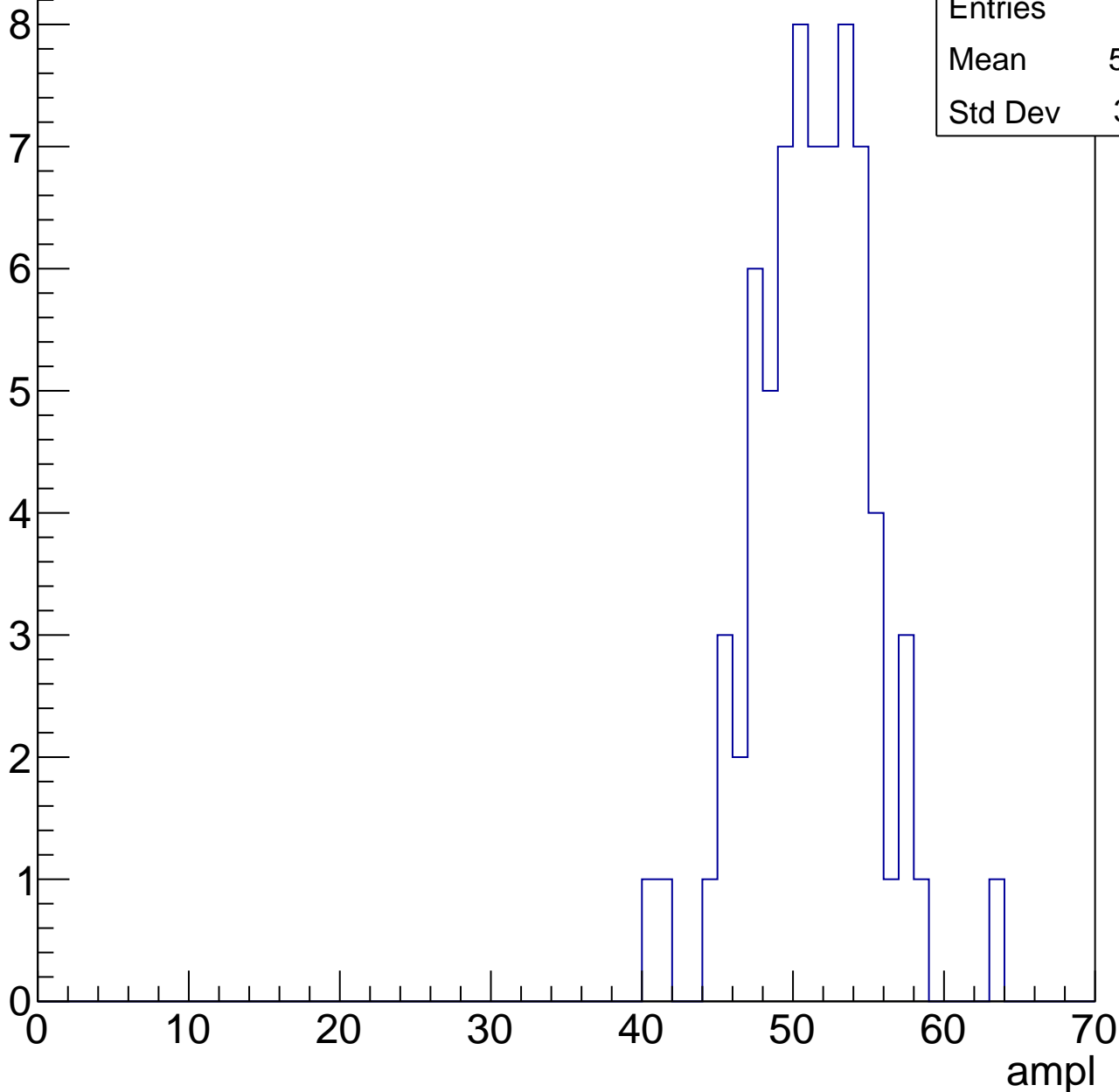


# B1L102S, U8-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	50.79
Std Dev	3.871

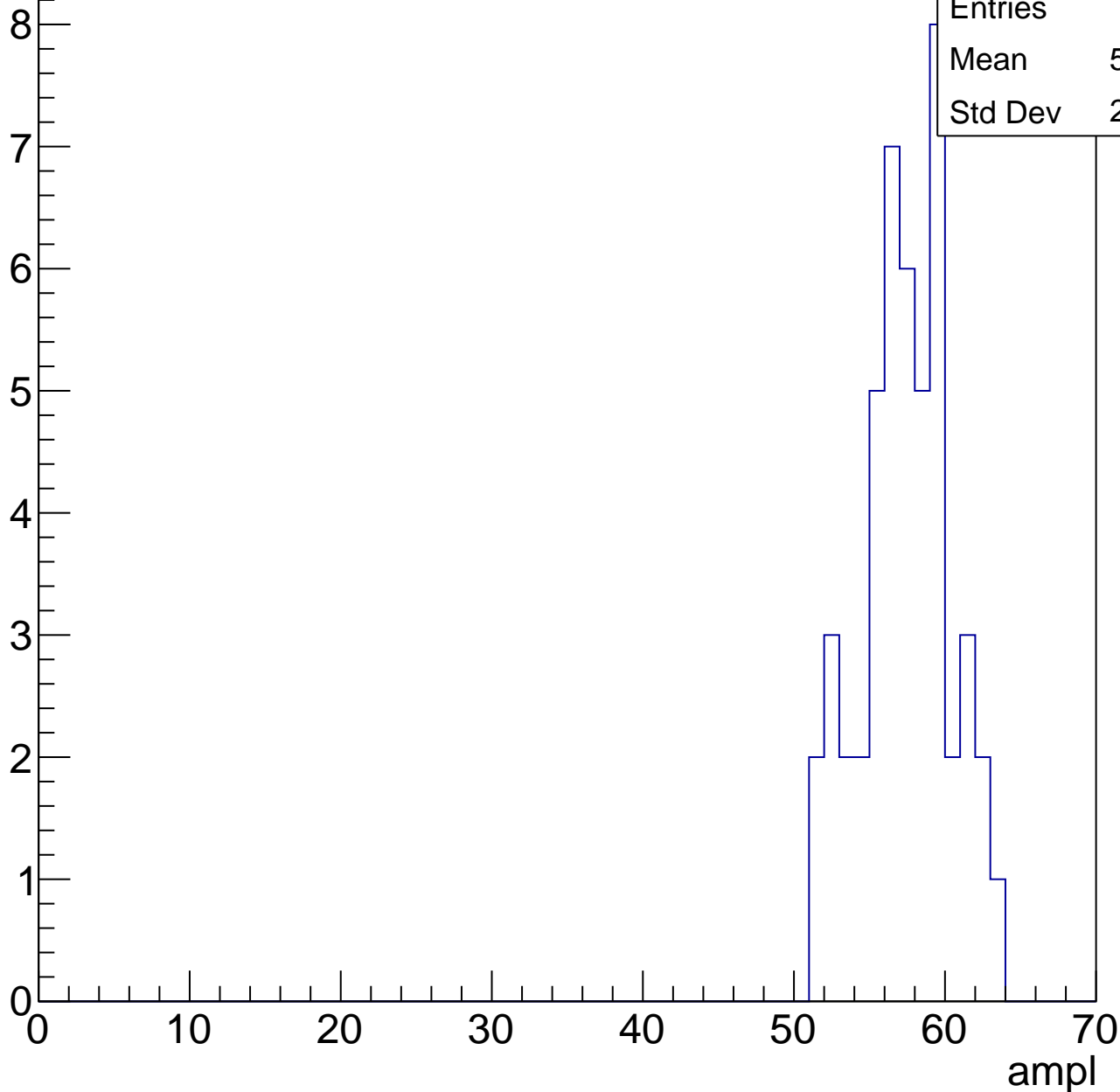


# B1L102S, U8-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	56.94
Std Dev	2.933

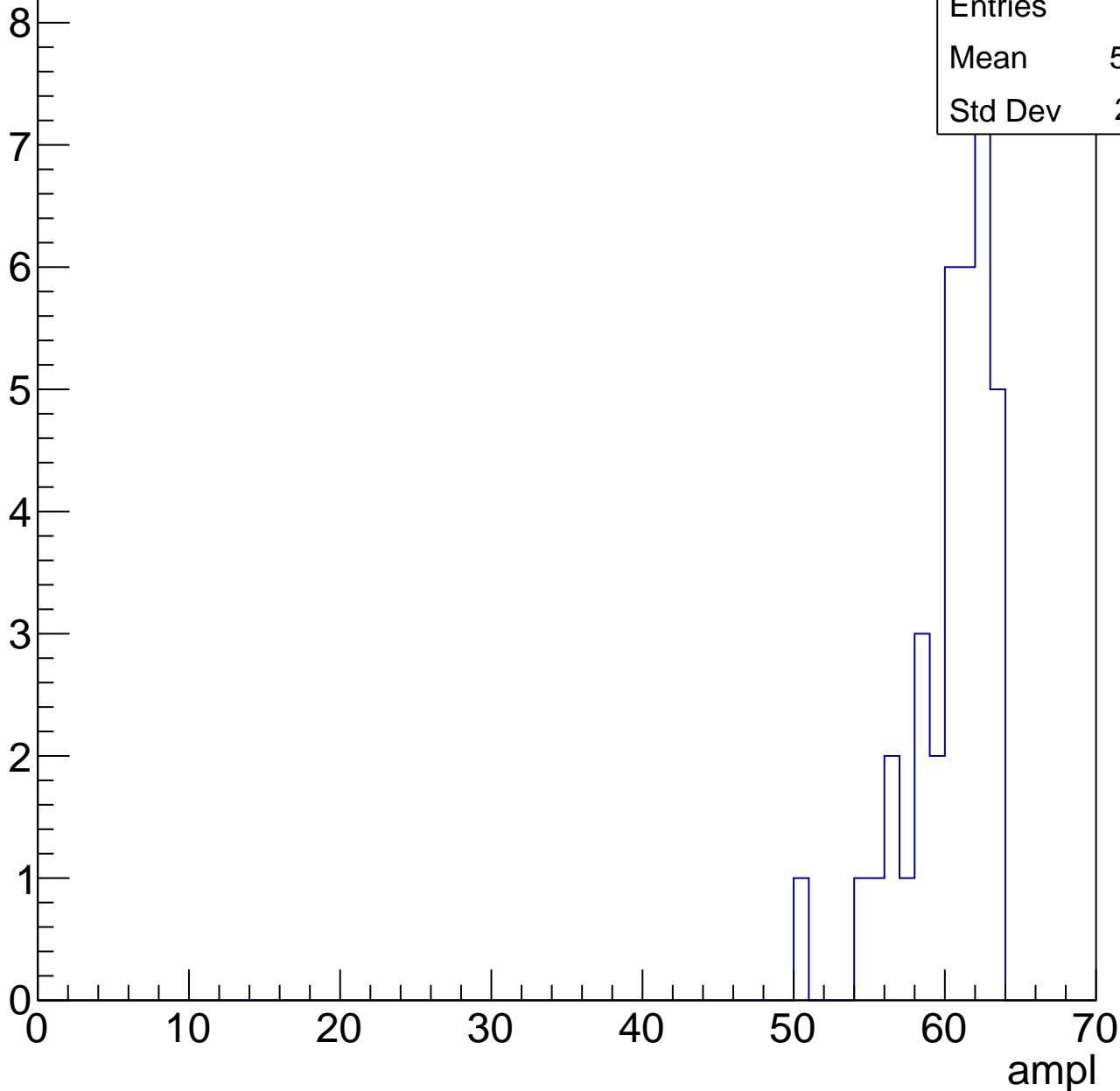


# B1L102S, U8-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

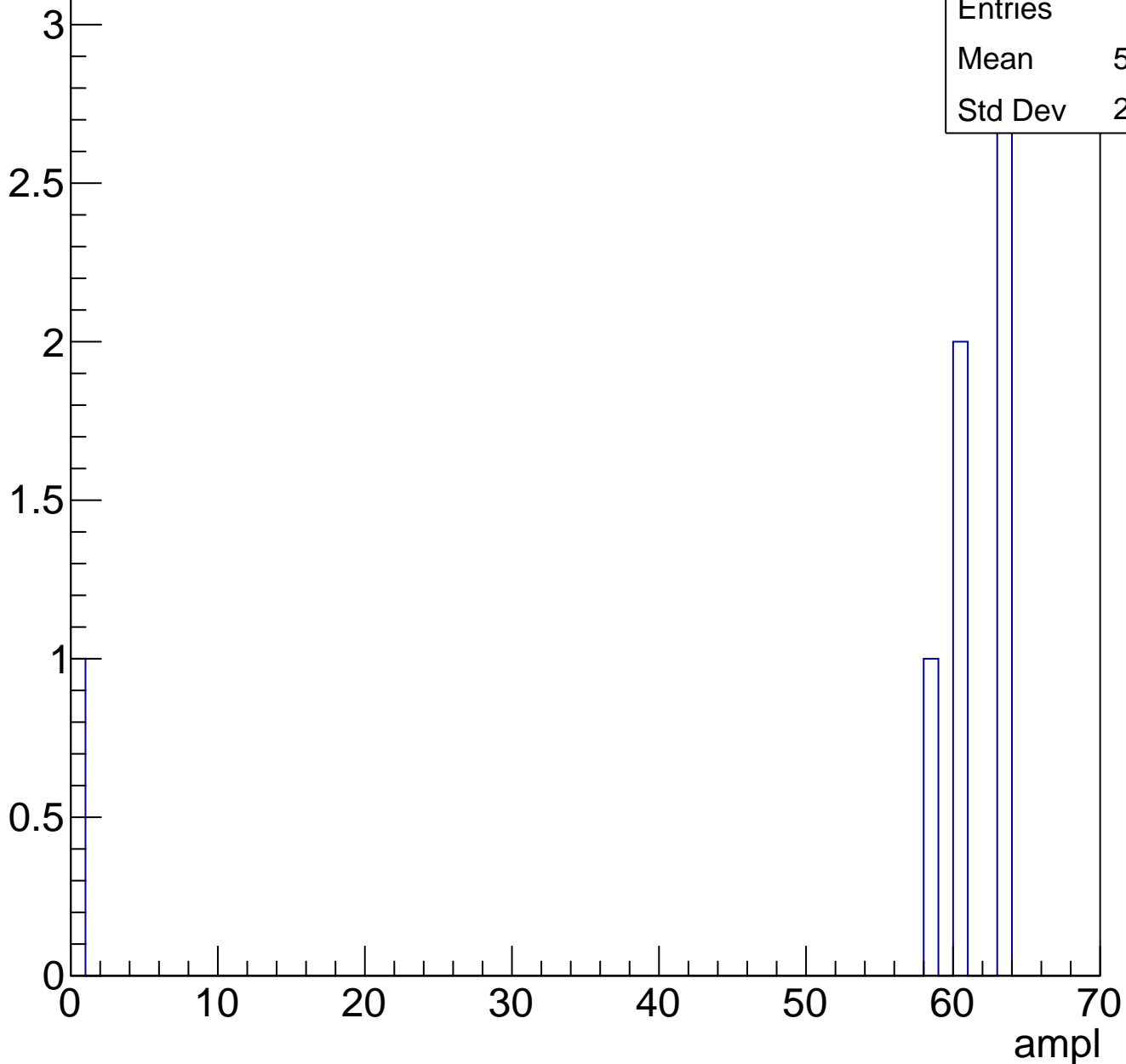
Entries	36
Mean	59.92
Std Dev	2.881



# B1L102S, U8-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

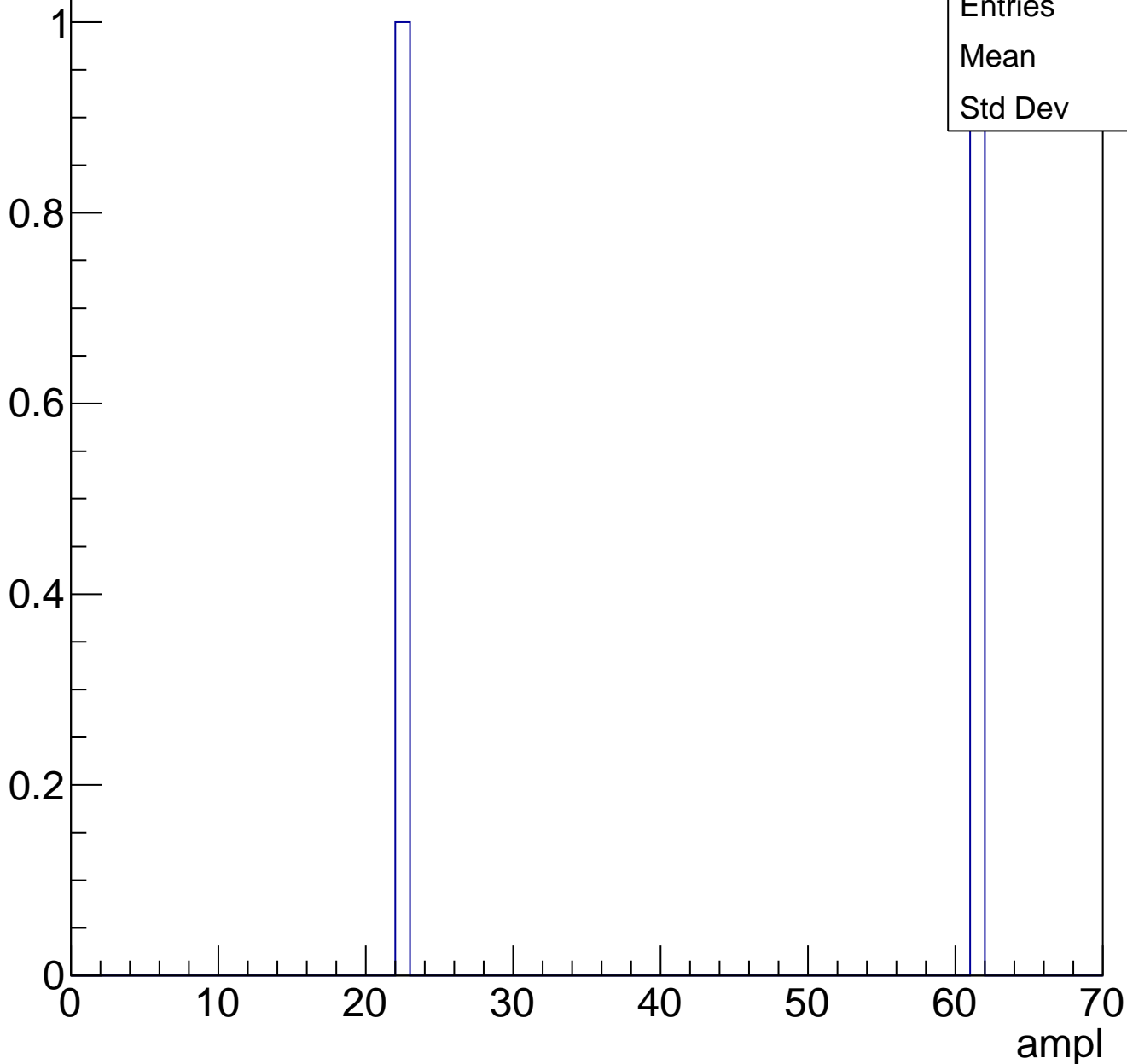




# B1L102S, U8-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch21, adc0

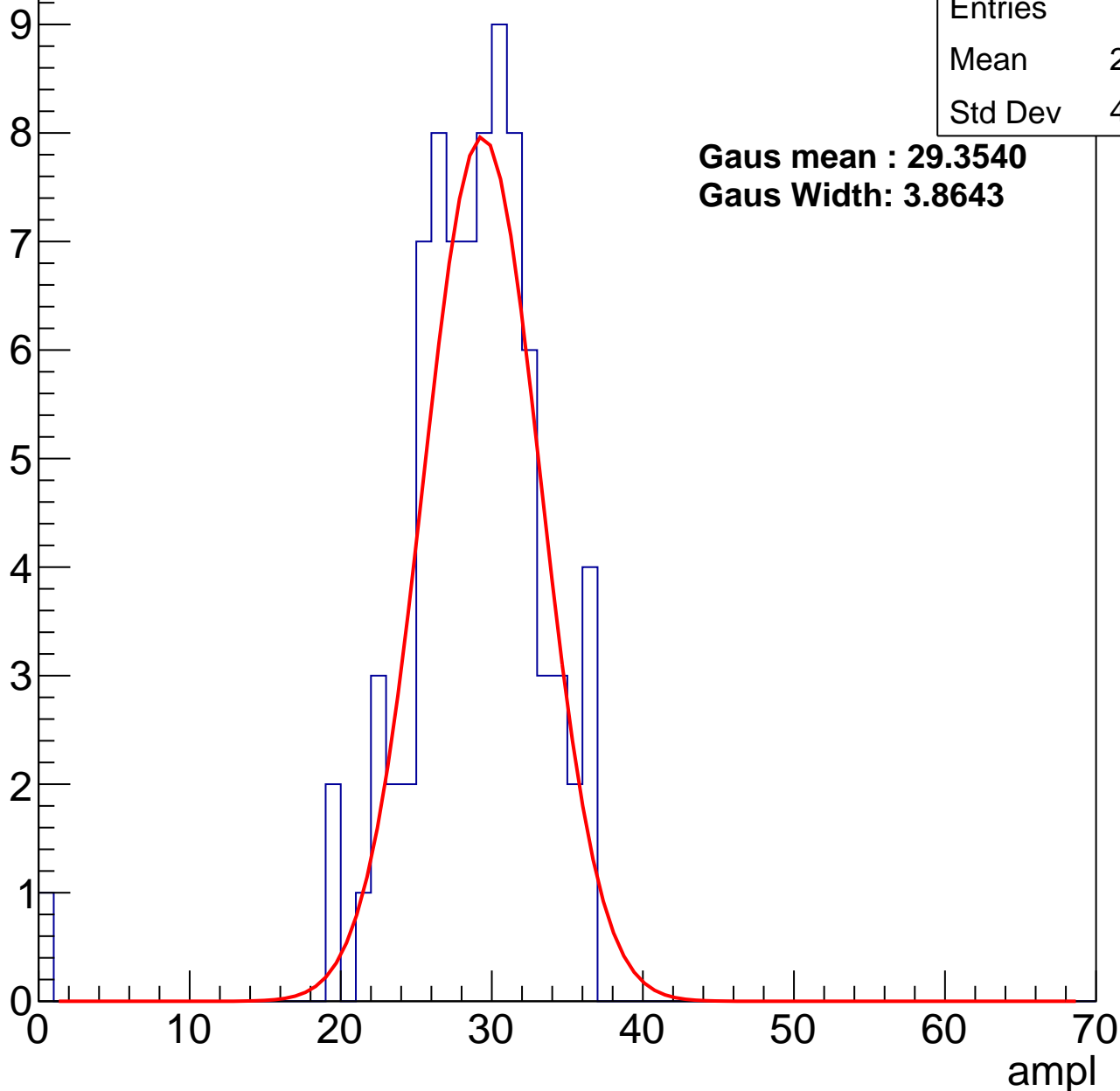
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	83
Mean	28.24
Std Dev	4.947

**Gaus mean : 29.3540**

**Gaus Width: 3.8643**



# B1L102S, U8-ch21, adc1

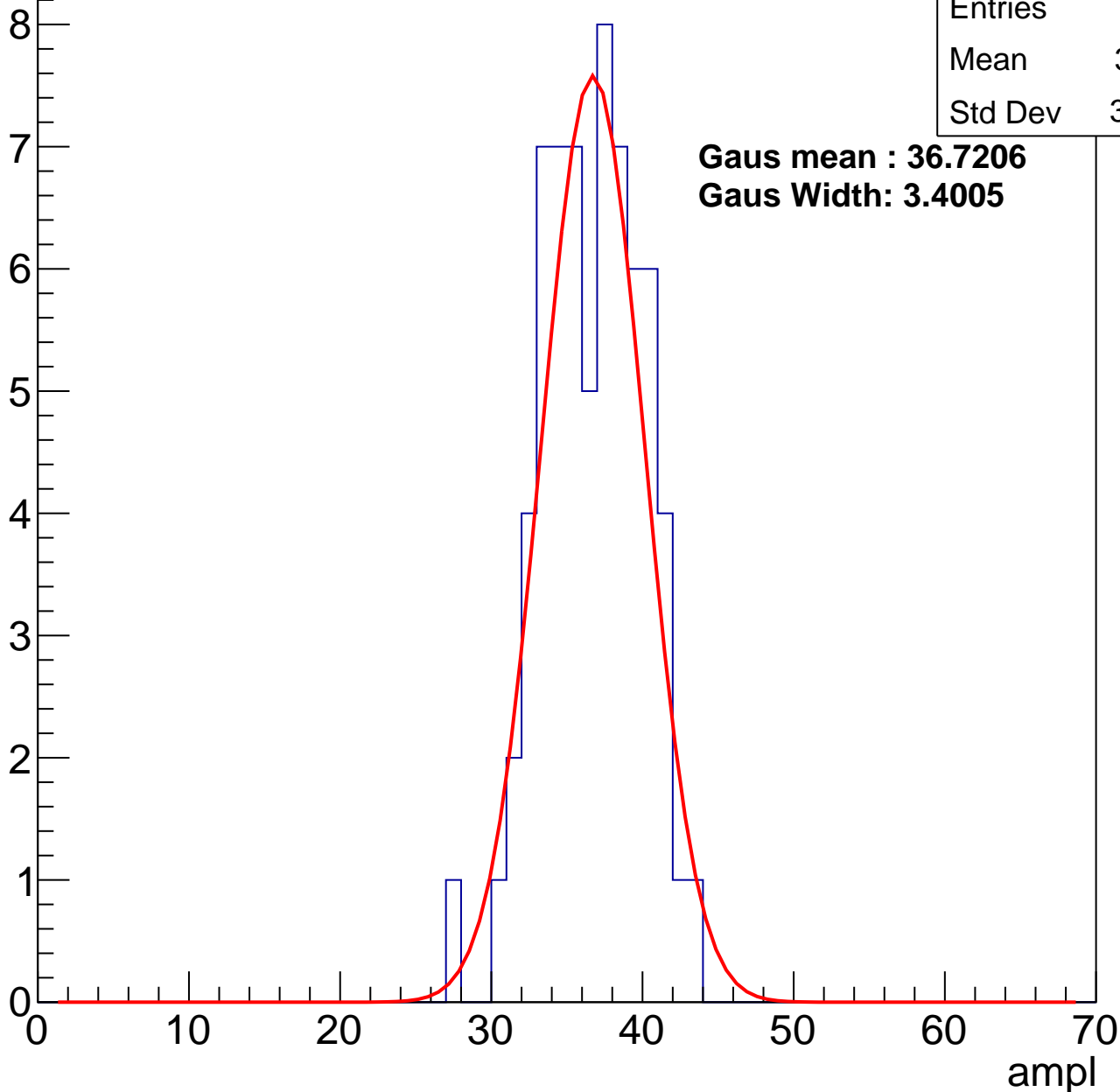
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	36.21
Std Dev	3.226

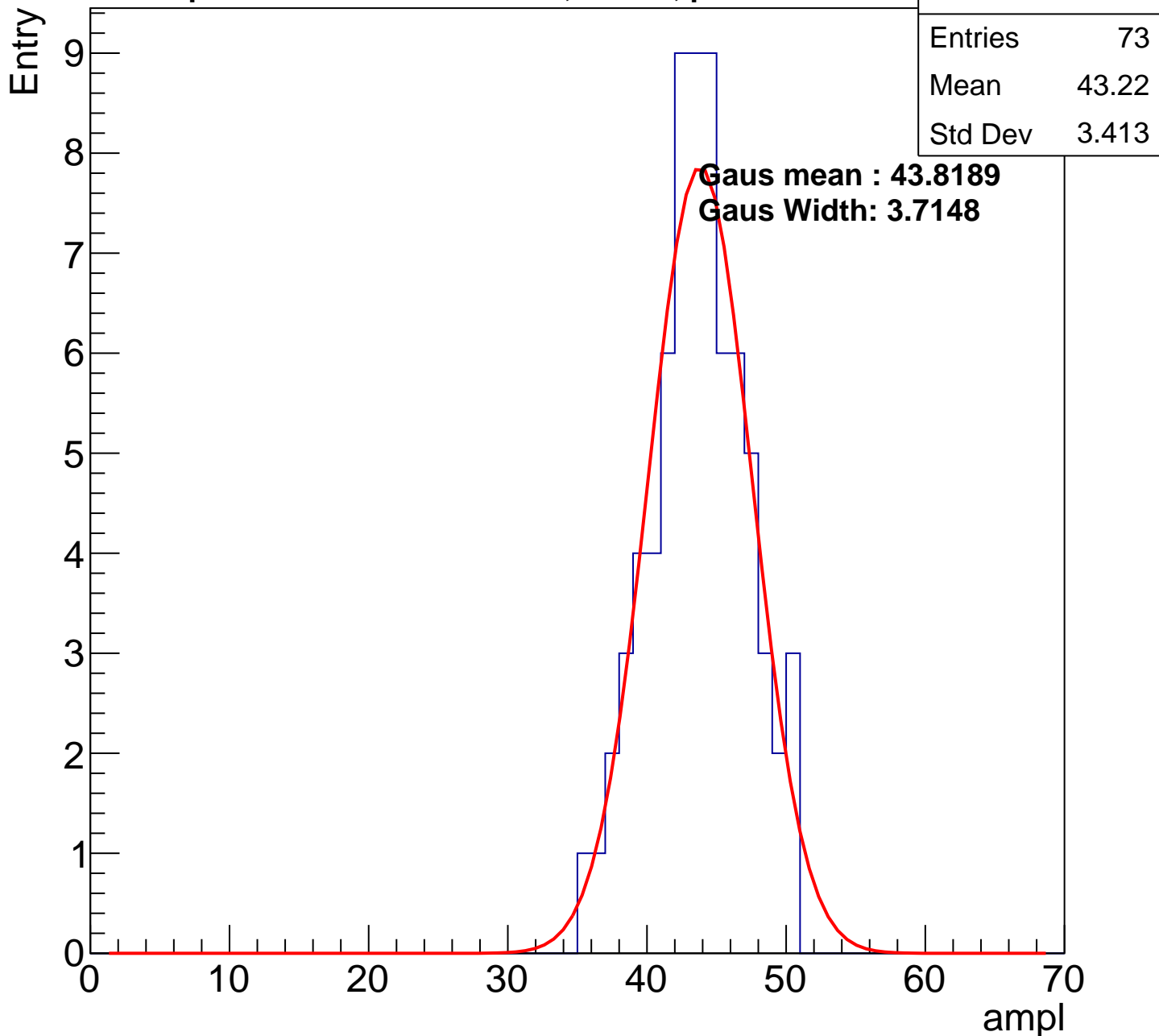
**Gaus mean : 36.7206**

**Gaus Width: 3.4005**



# B1L102S, U8-ch21, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U8-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

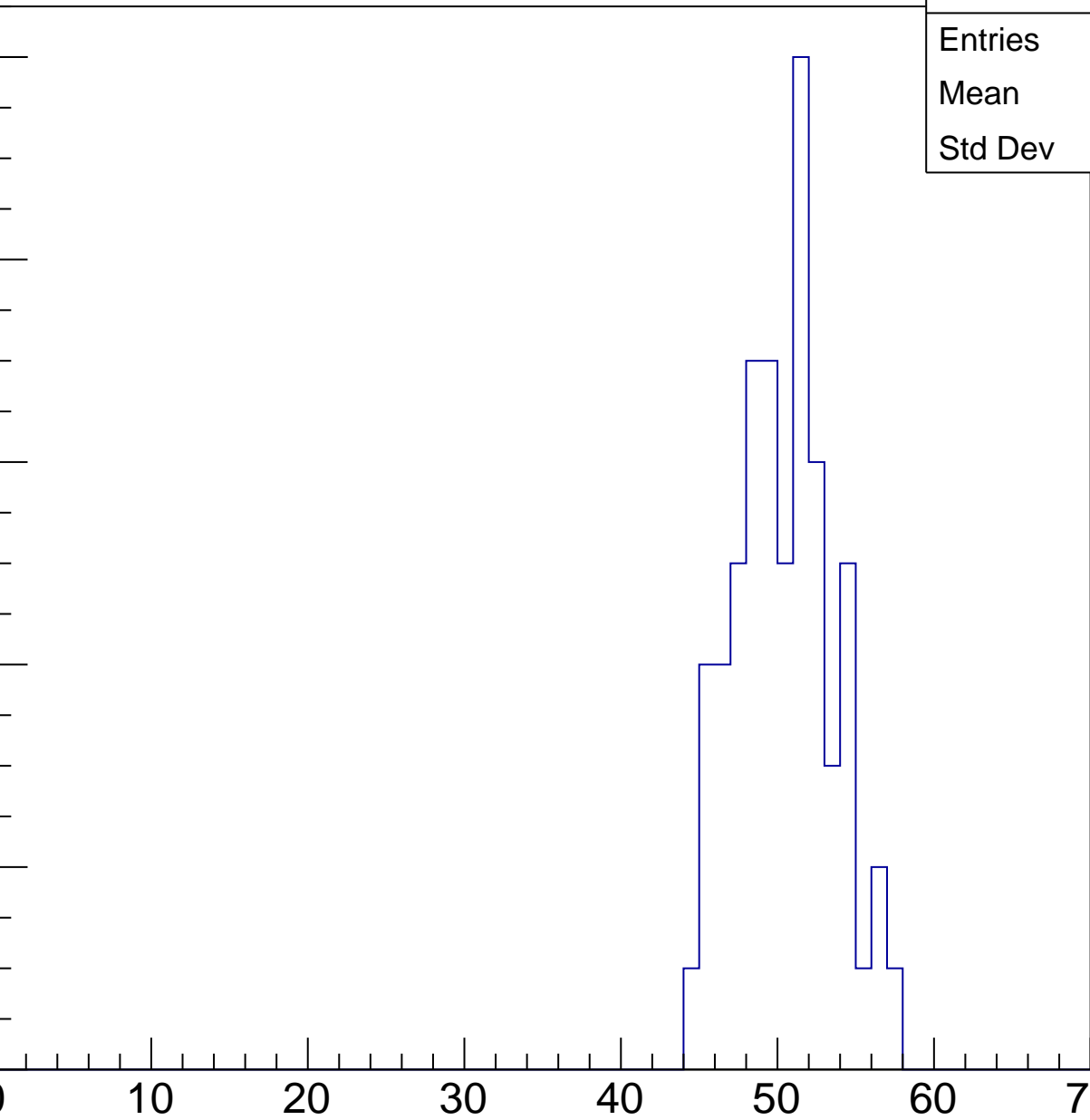
Entries	61
Mean	49.95
Std Dev	3.048

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

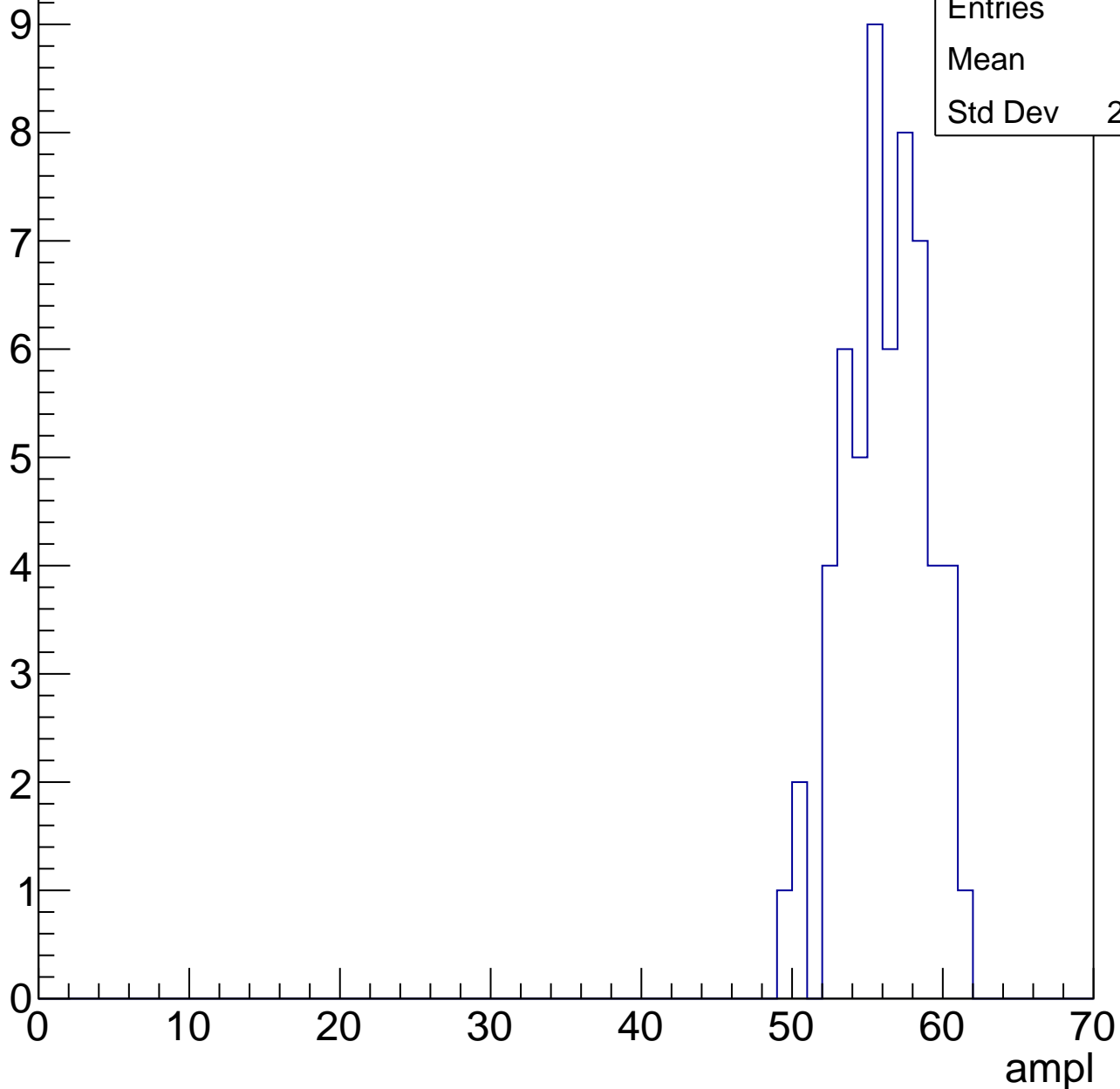
ampl



# B1L102S, U8-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

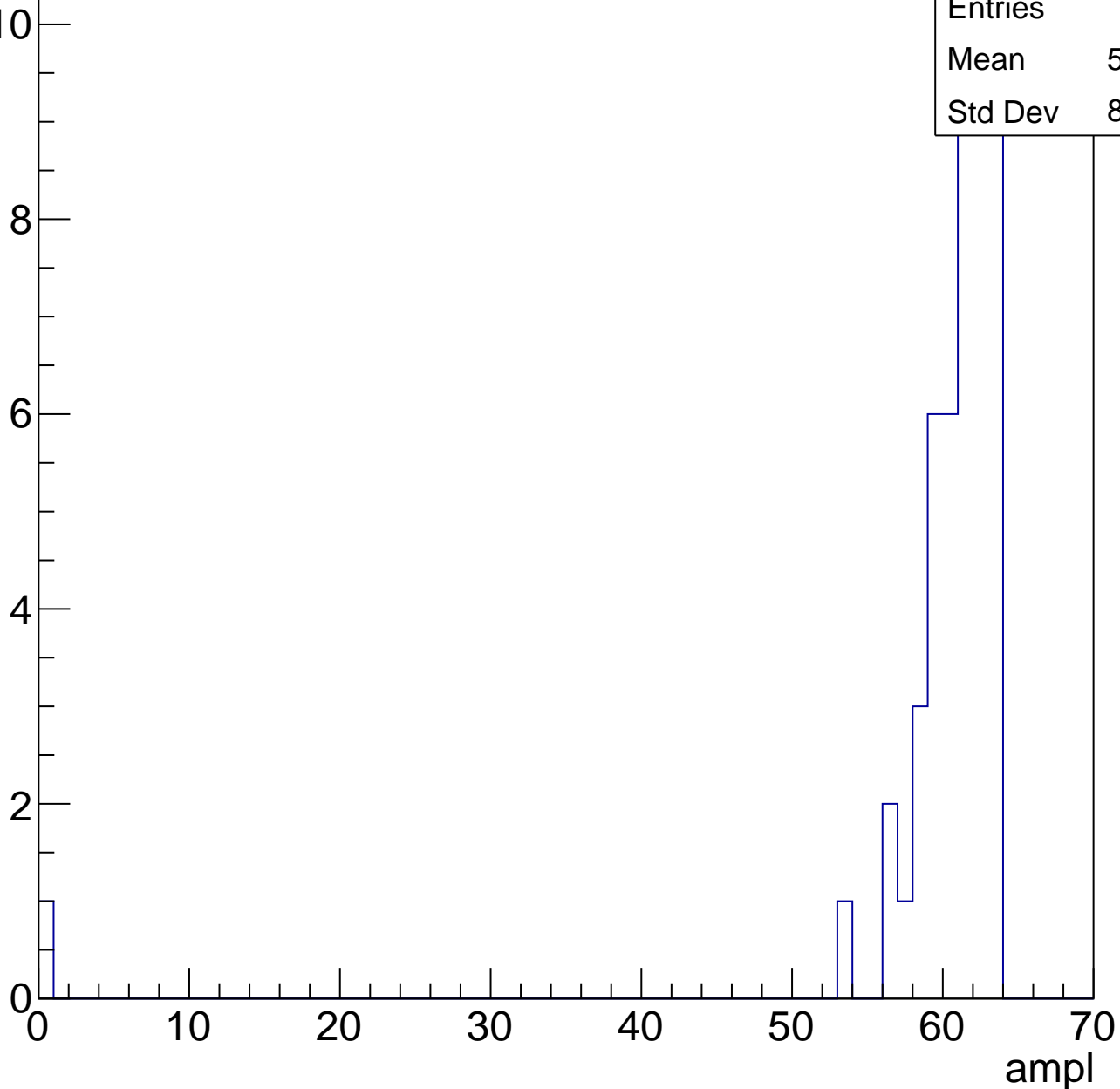


# B1L102S, U8-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	59.37
Std Dev	8.838



# B1L102S, U8-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L102S, U8-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch22, adc0

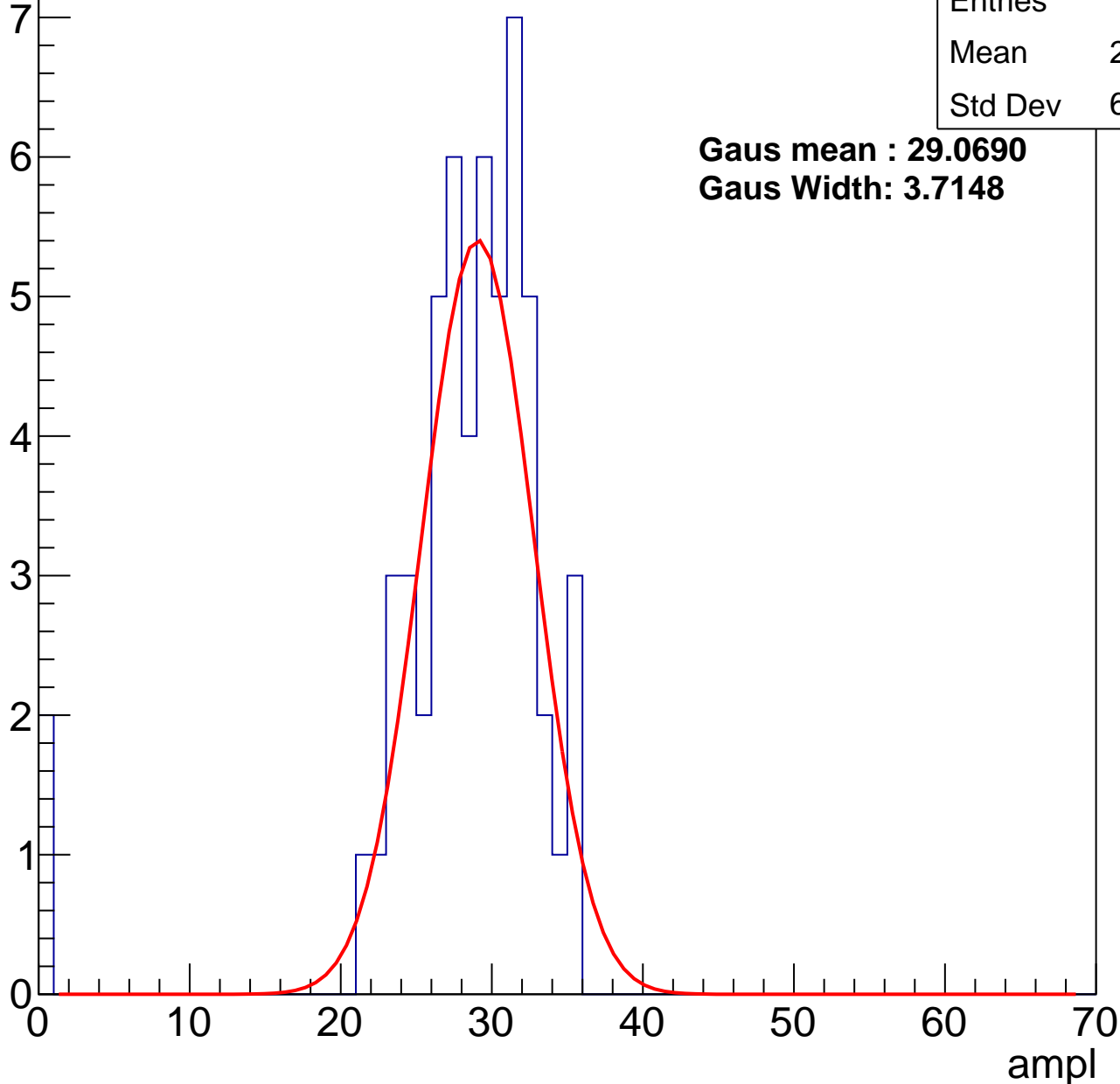
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	27.57
Std Dev	6.284

**Gaus mean : 29.0690**

**Gaus Width: 3.7148**



# B1L102S, U8-ch22, adc1

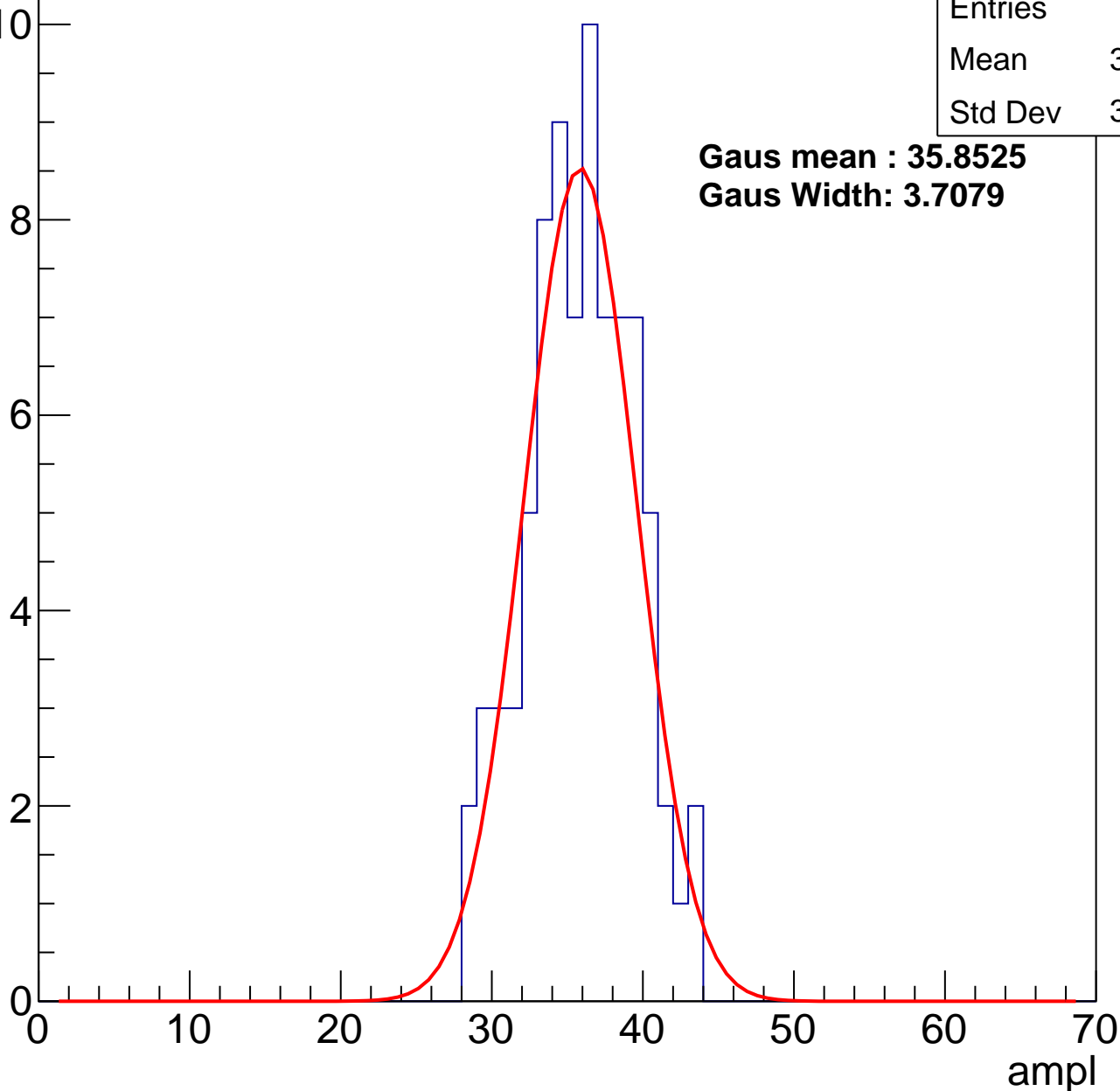
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	81
Mean	35.42
Std Dev	3.492

**Gaus mean : 35.8525**

**Gaus Width: 3.7079**



# B1L102S, U8-ch22, adc2

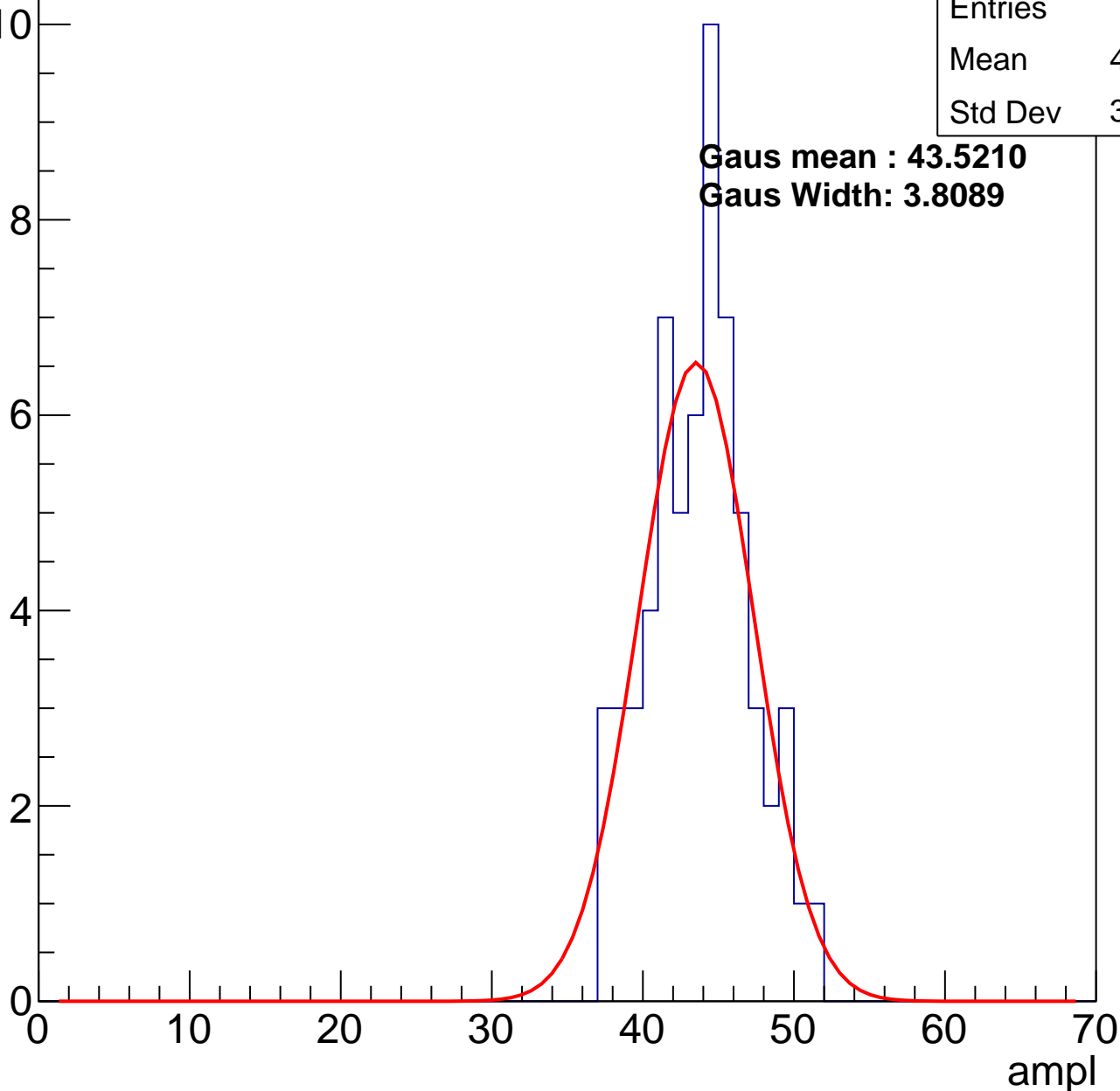
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	43.29
Std Dev	3.326

**Gaus mean : 43.5210**

**Gaus Width: 3.8089**

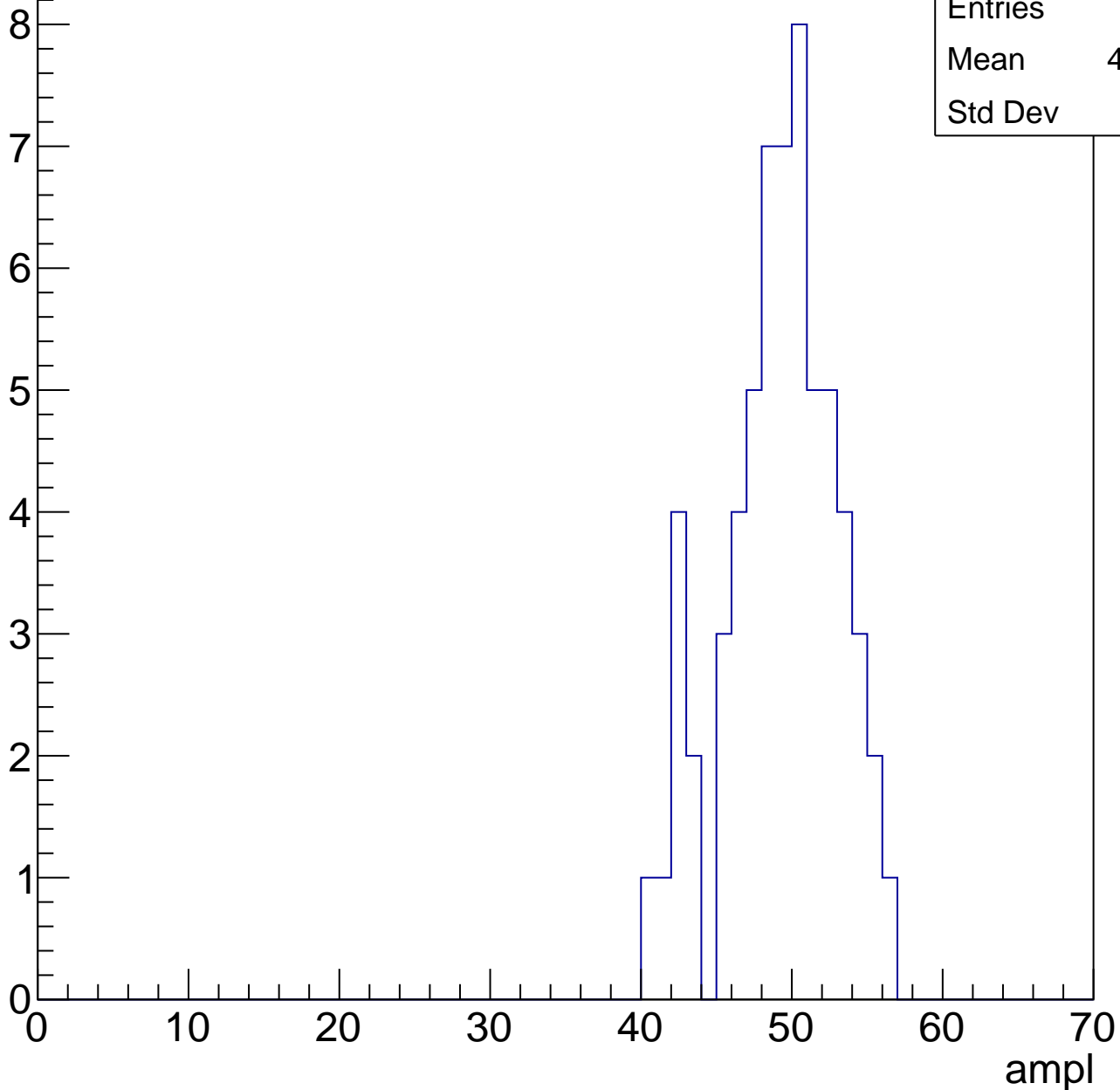


# B1L102S, U8-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	48.76
Std Dev	3.71

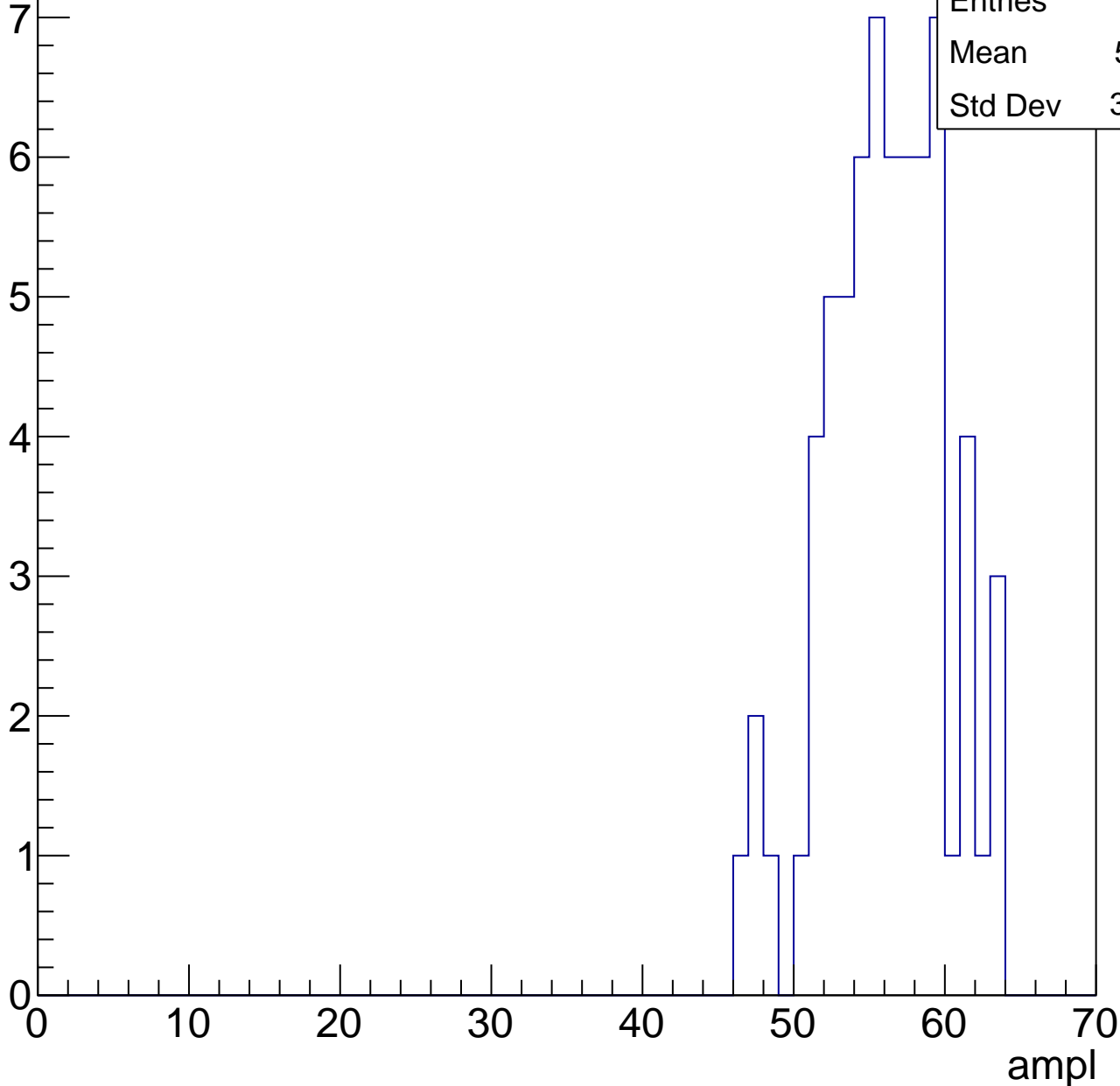


# B1L102S, U8-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

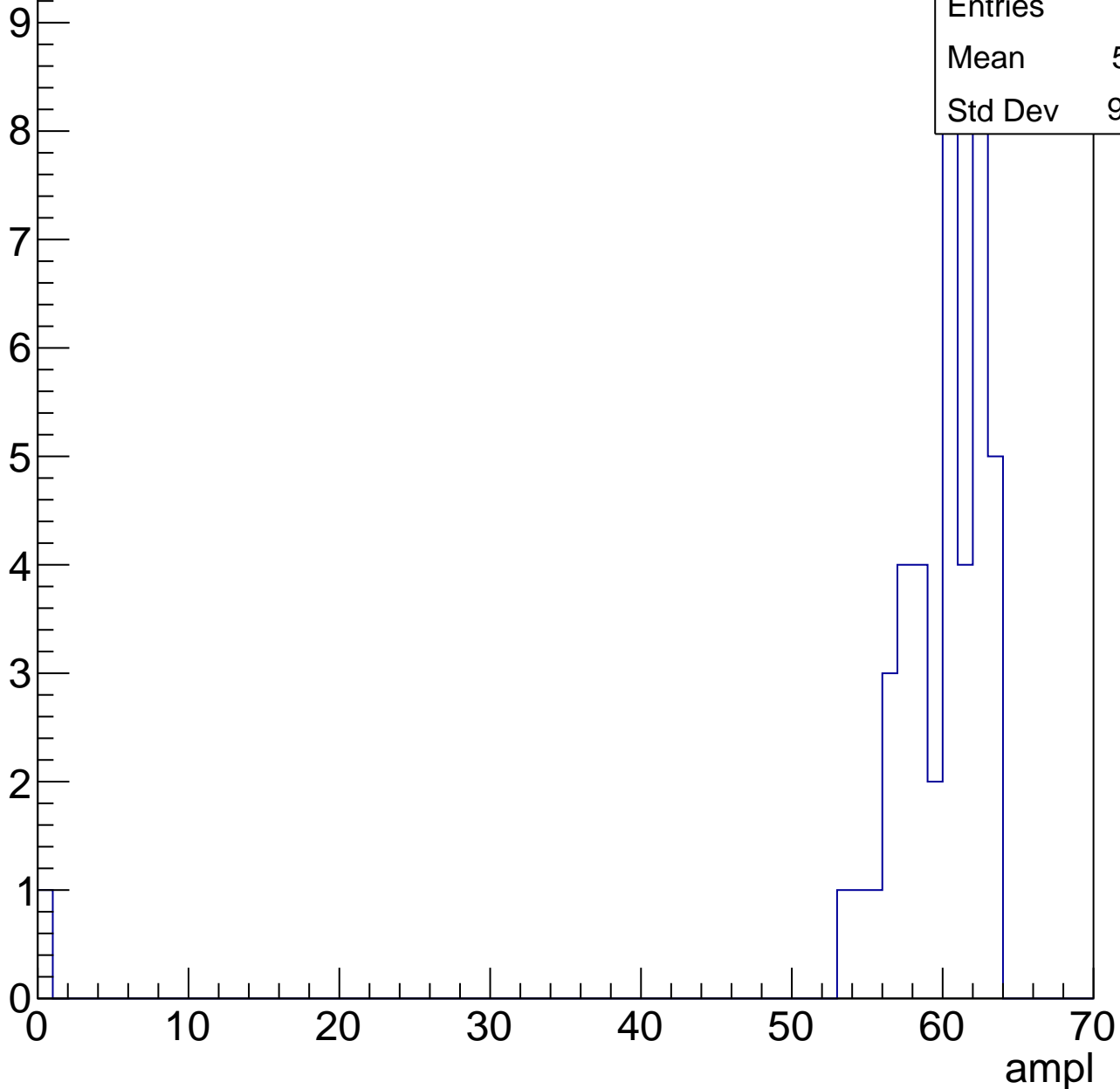
Entries	66
Mean	55.61
Std Dev	3.892



# B1L102S, U8-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.5
Std Dev	1.384

ampl

0 10 20 30 40 50 60 70



# B1L102S, U8-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch23, adc0

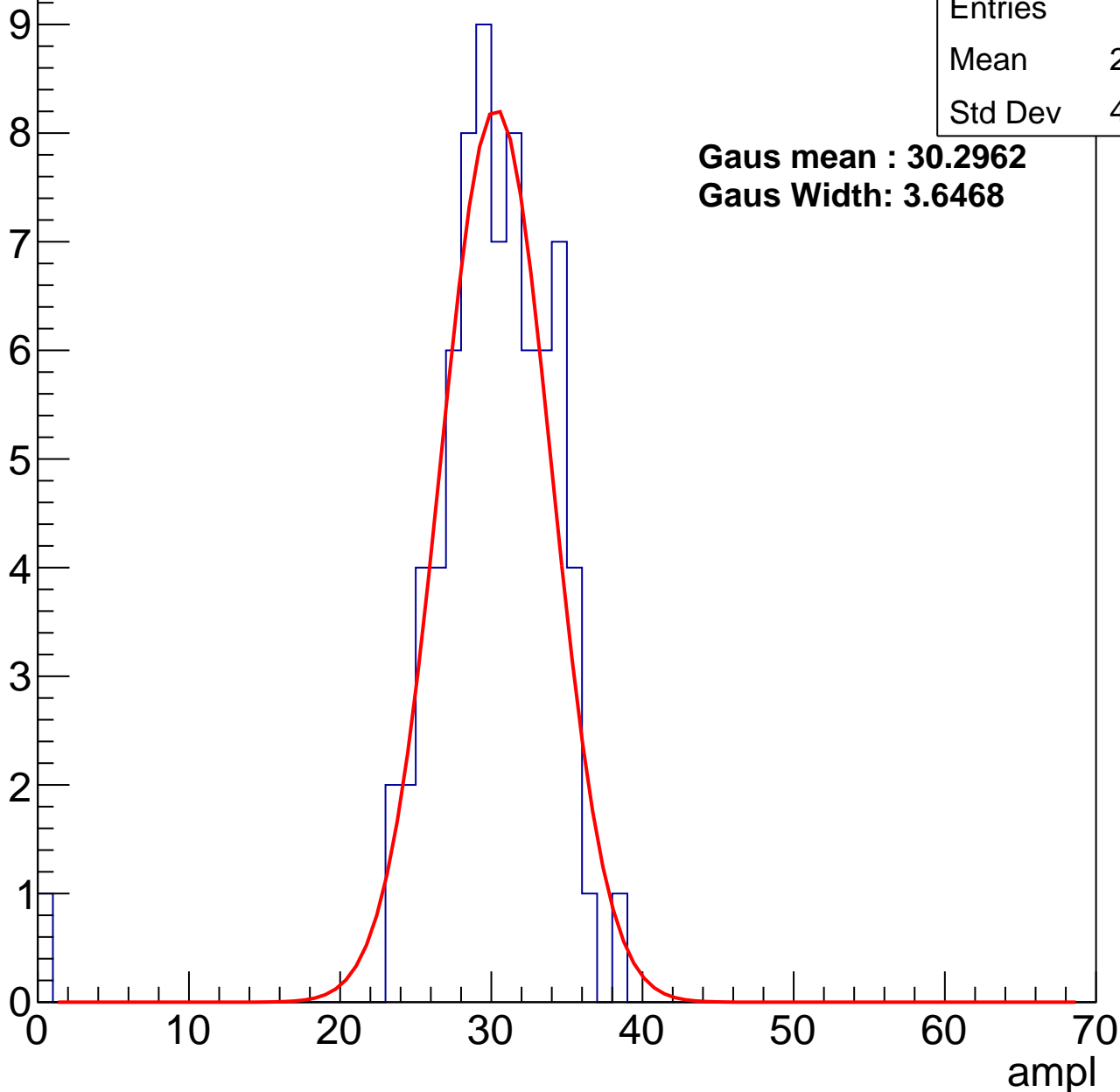
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	29.54
Std Dev	4.745

**Gaus mean : 30.2962**

**Gaus Width: 3.6468**



# B1L102S, U8-ch23, adc1

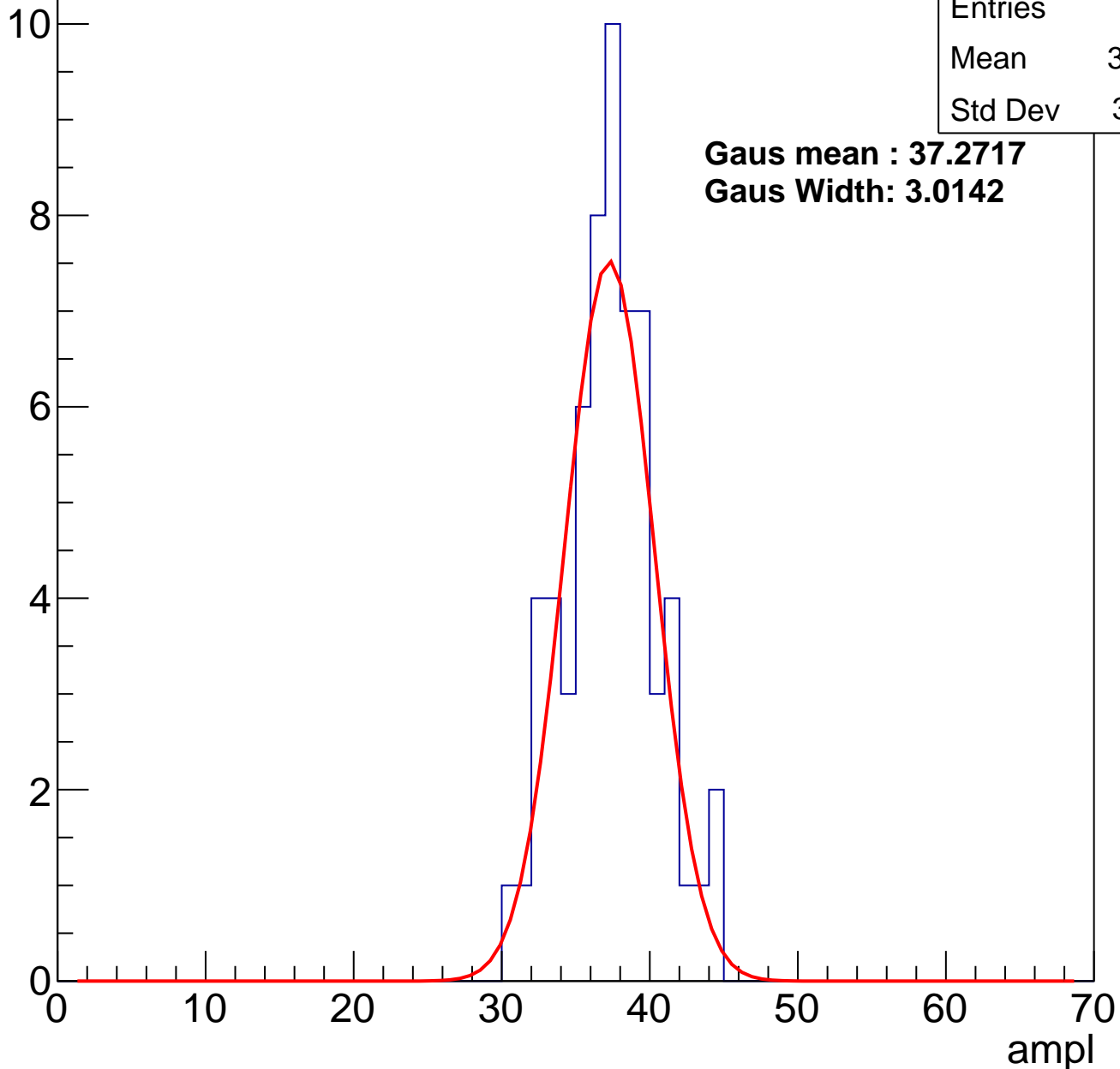
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	62
Mean	36.89
Std Dev	3.091

**Gaus mean : 37.2717**

**Gaus Width: 3.0142**

Entry



# B1L102S, U8-ch23, adc2

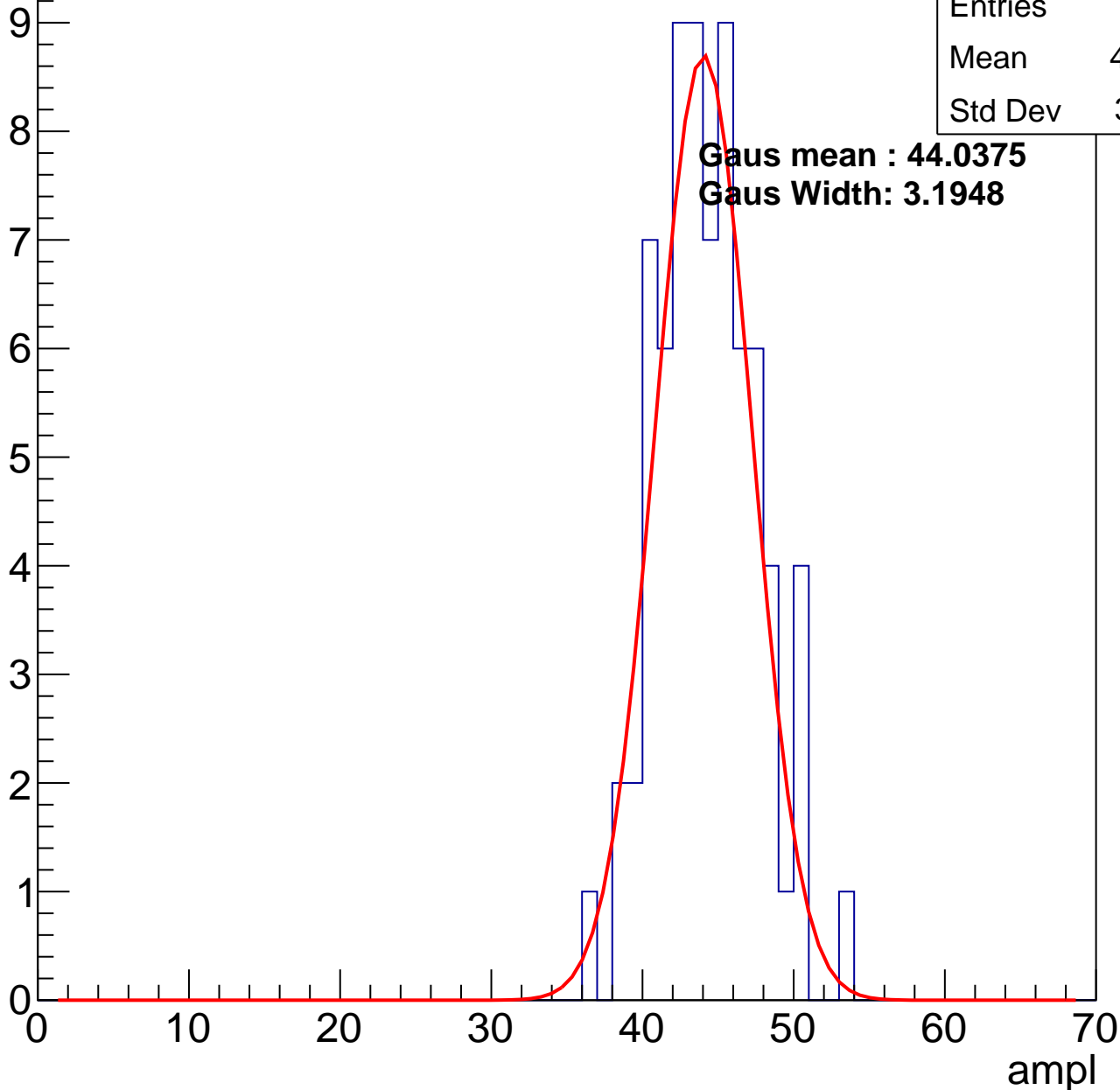
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	43.86
Std Dev	3.281

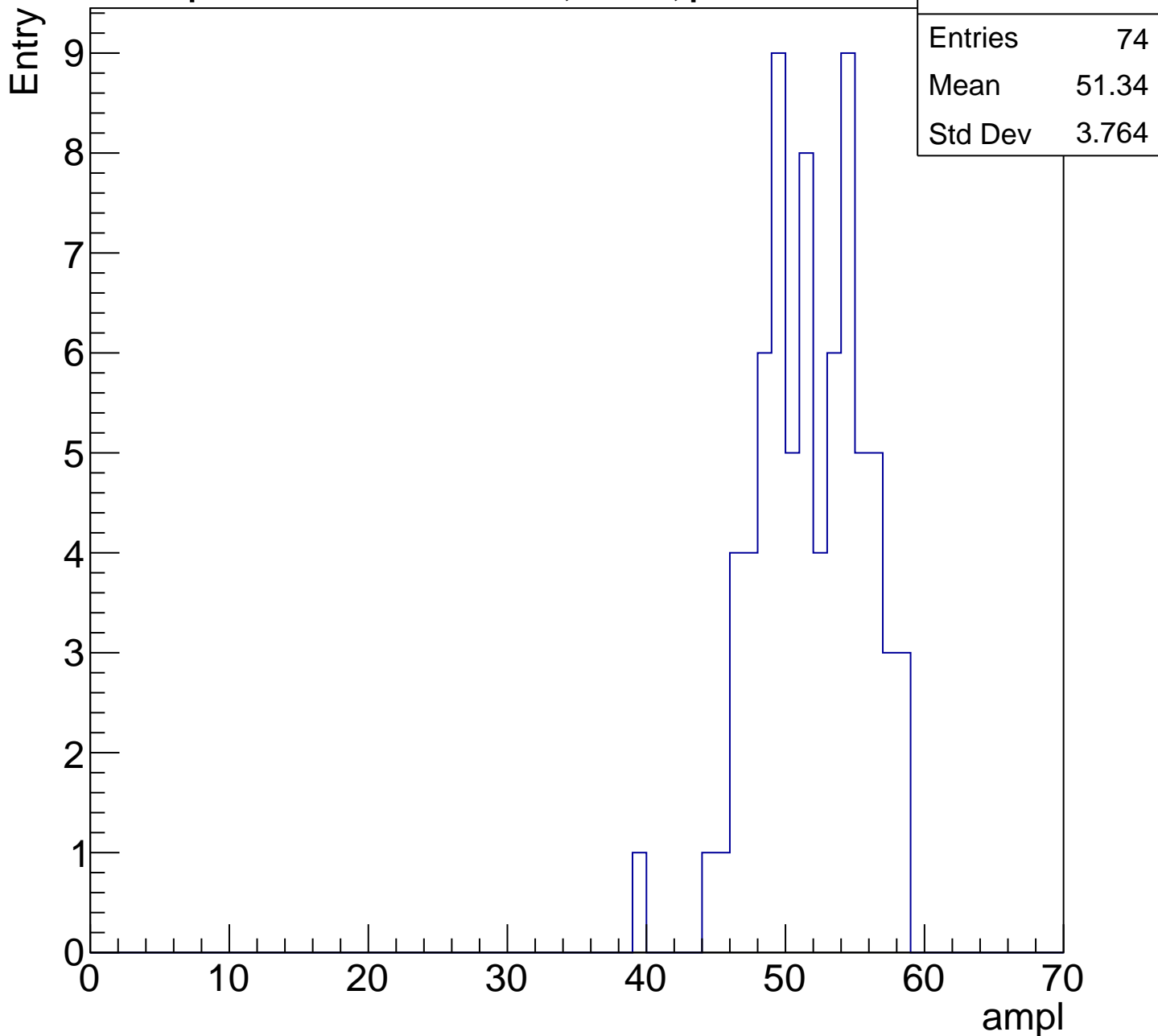
**Gaus mean : 44.0375**

**Gaus Width: 3.1948**



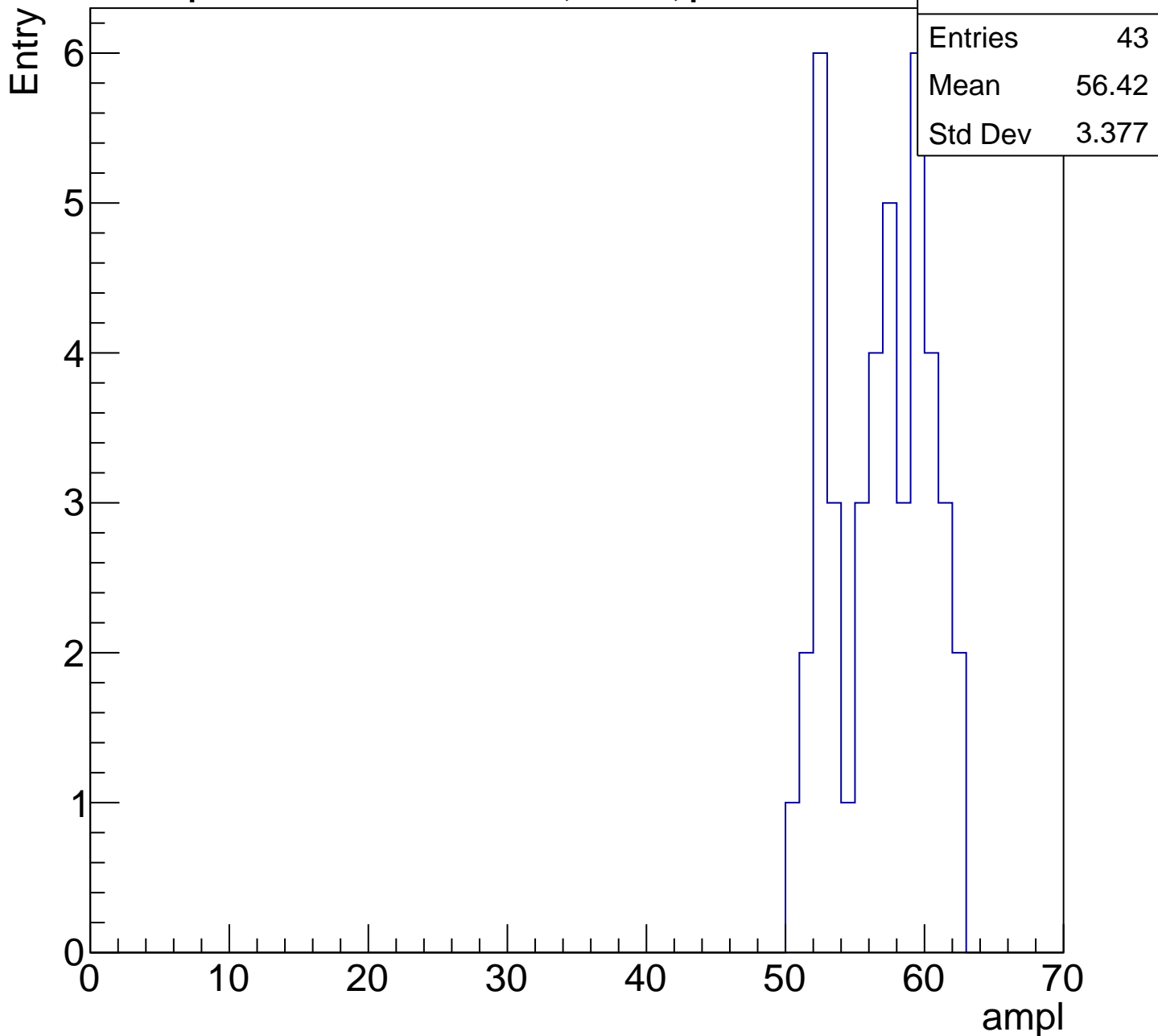
# B1L102S, U8-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U8-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

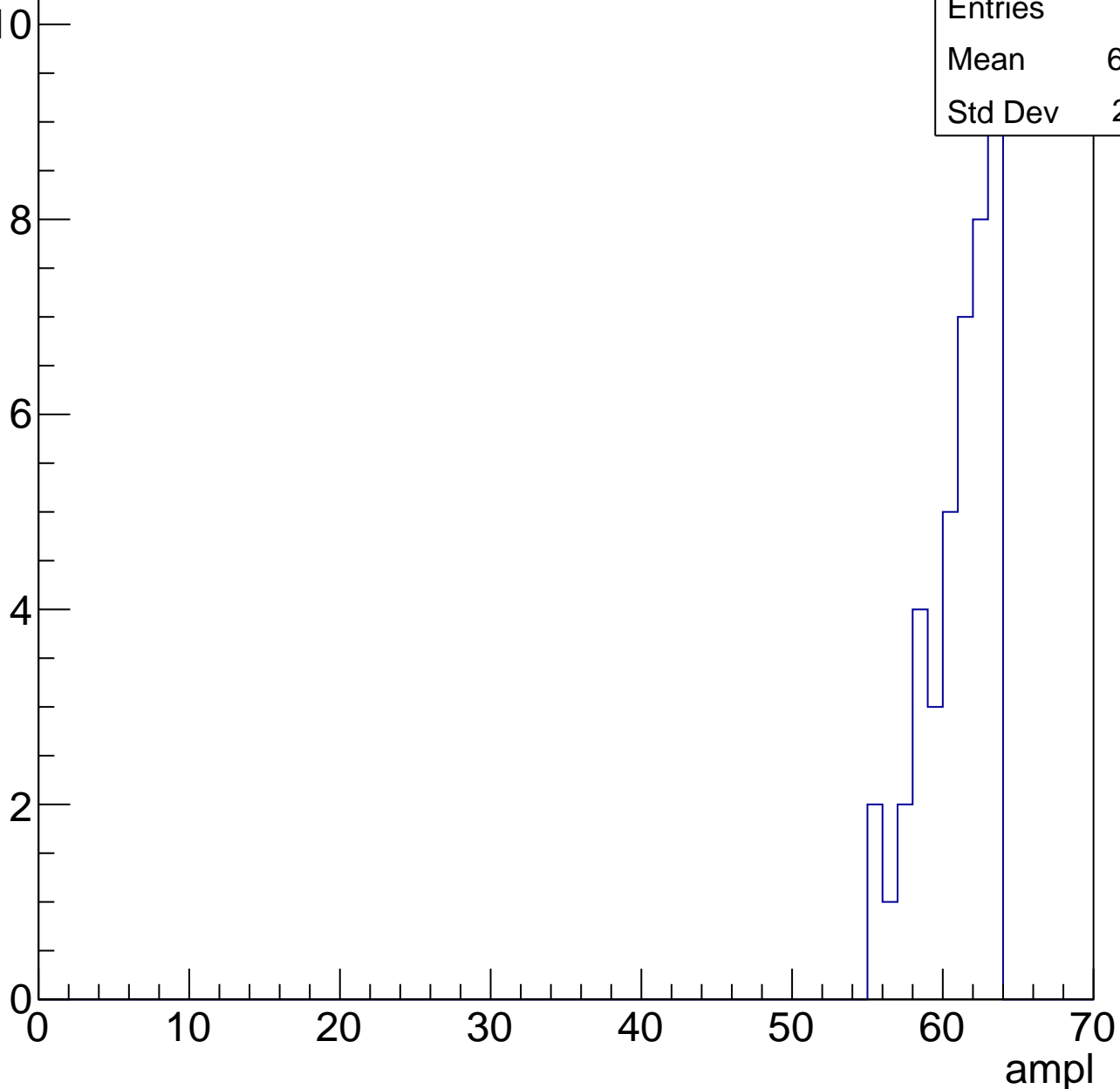


# B1L102S, U8-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

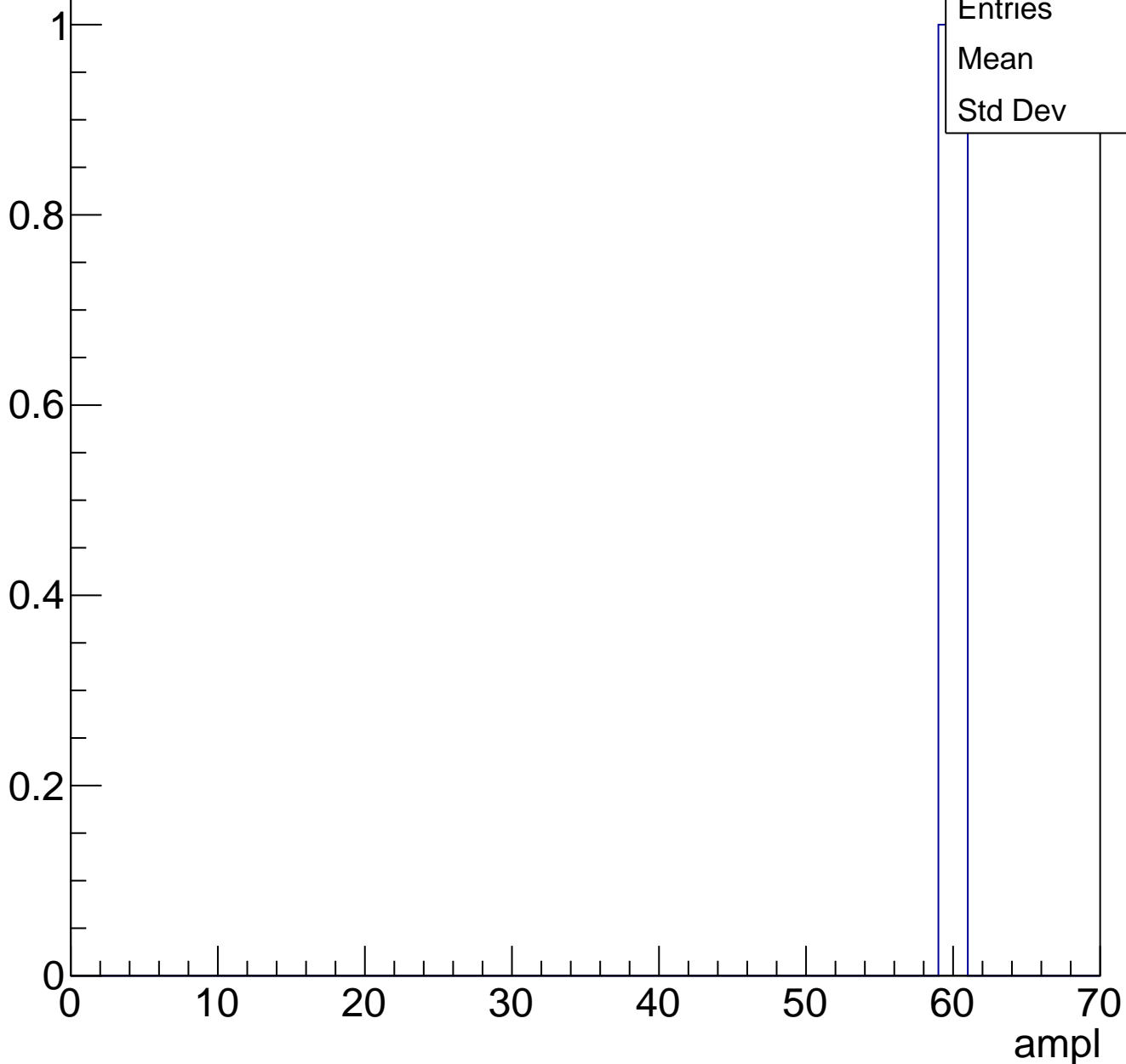
Entries	42
Mean	60.52
Std Dev	2.291



# B1L102S, U8-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	7
Std Dev	9.899

# B1L102S, U8-ch24, adc0

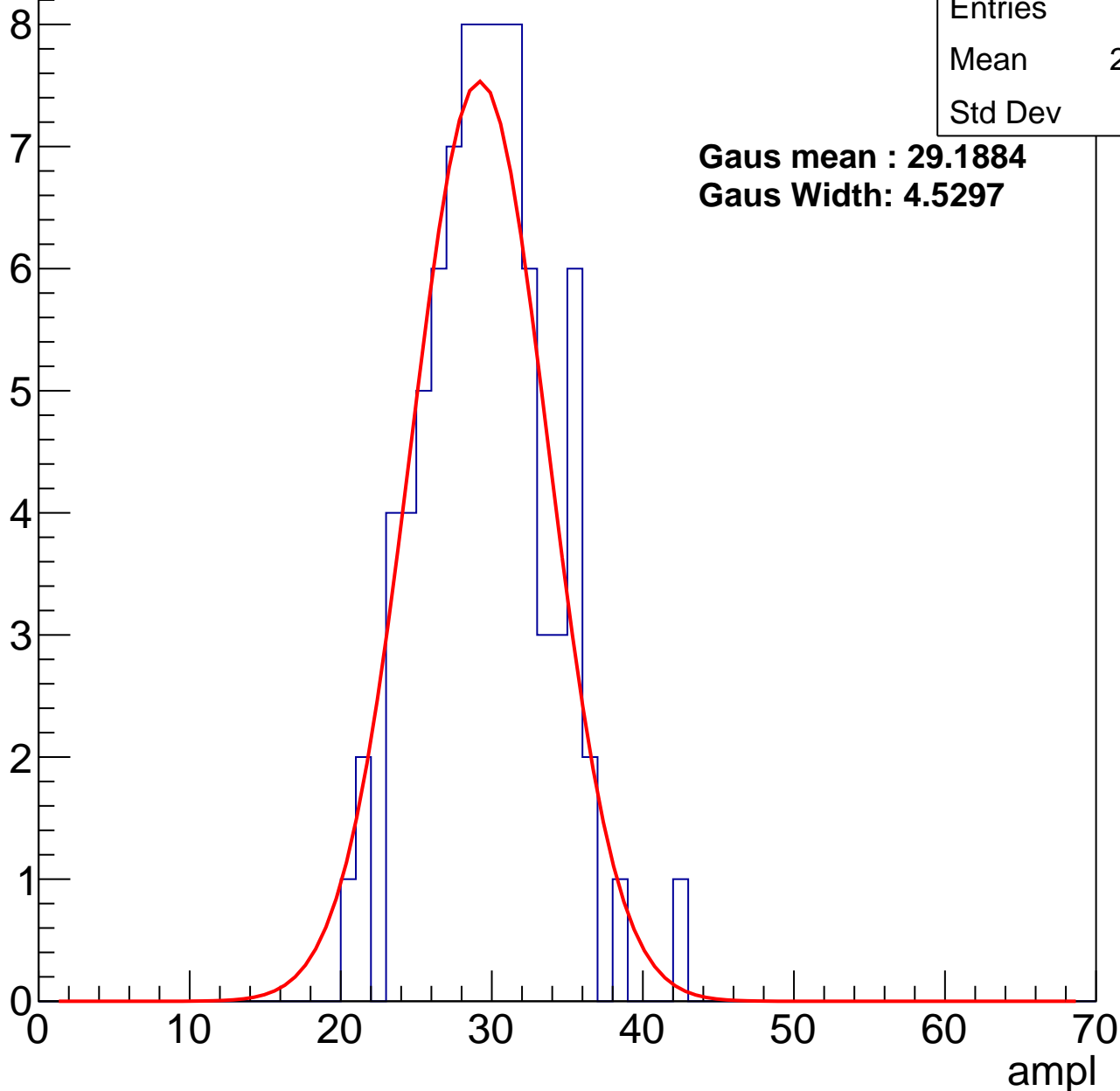
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	83
Mean	29.14
Std Dev	4.11

**Gaus mean : 29.1884**

**Gaus Width: 4.5297**



# B1L102S, U8-ch24, adc1

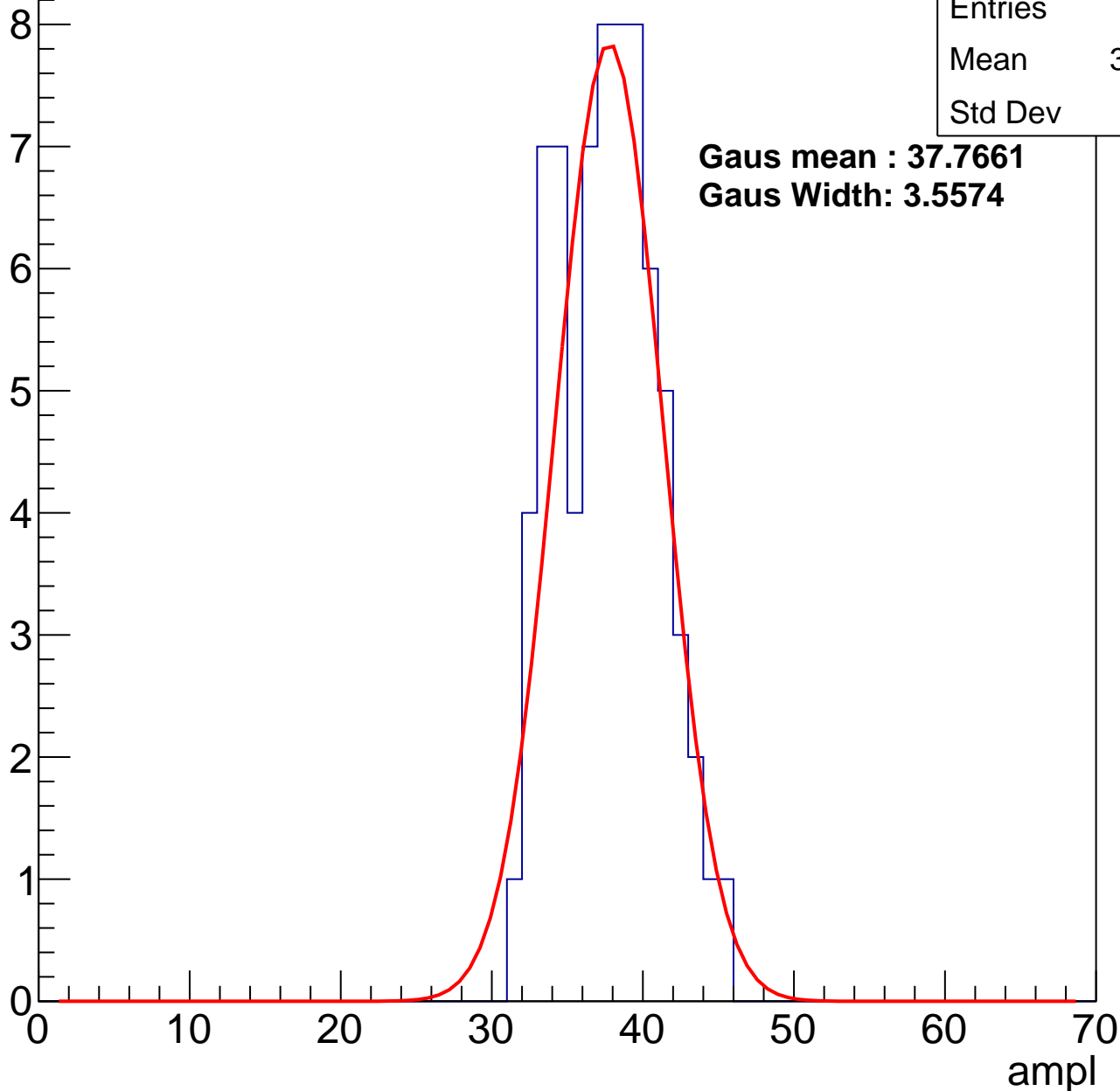
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	37.19
Std Dev	3.26

**Gaus mean : 37.7661**

**Gaus Width: 3.5574**



# B1L102S, U8-ch24, adc2

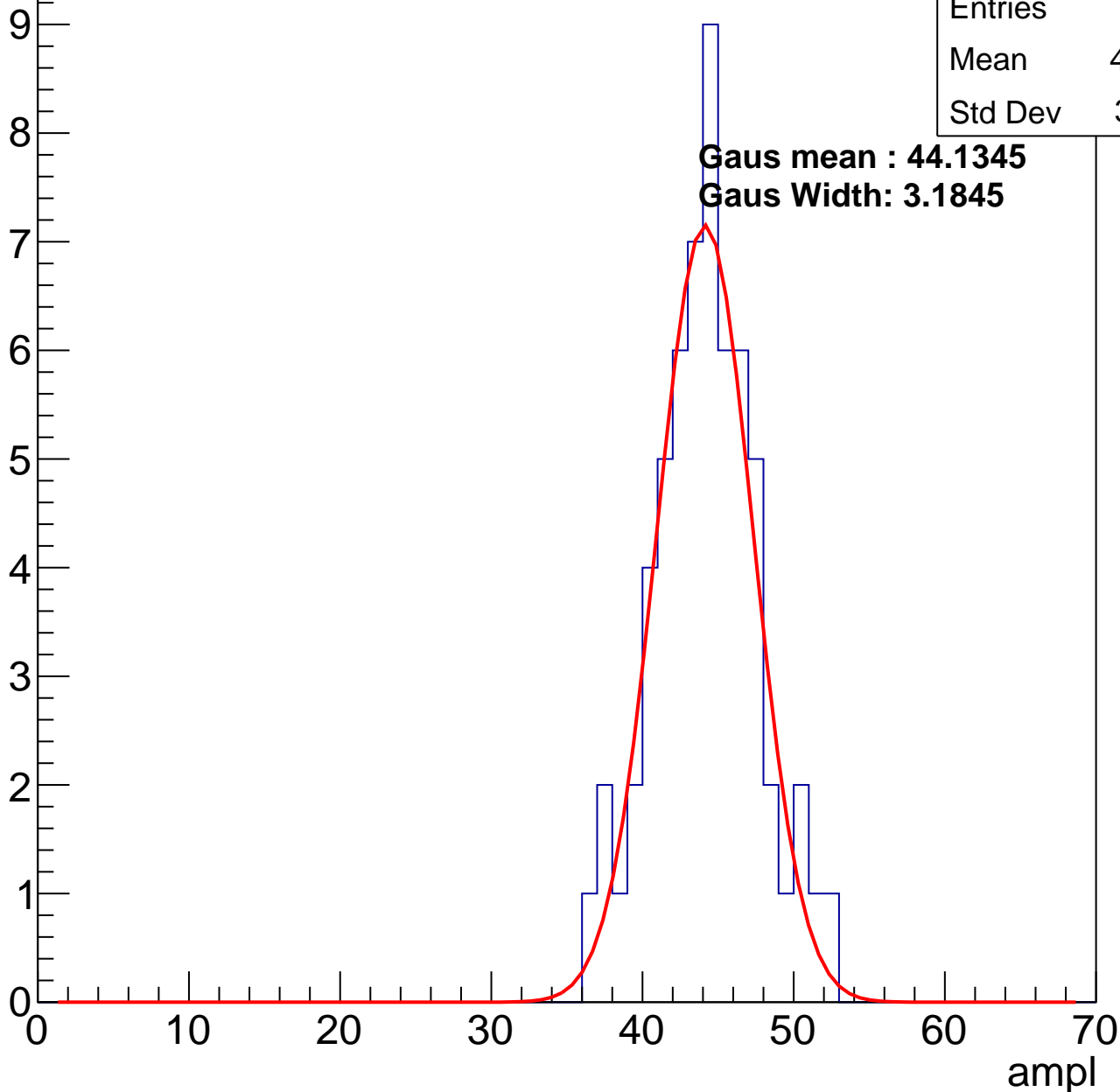
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	43.75
Std Dev	3.391

**Gaus mean : 44.1345**

**Gaus Width: 3.1845**

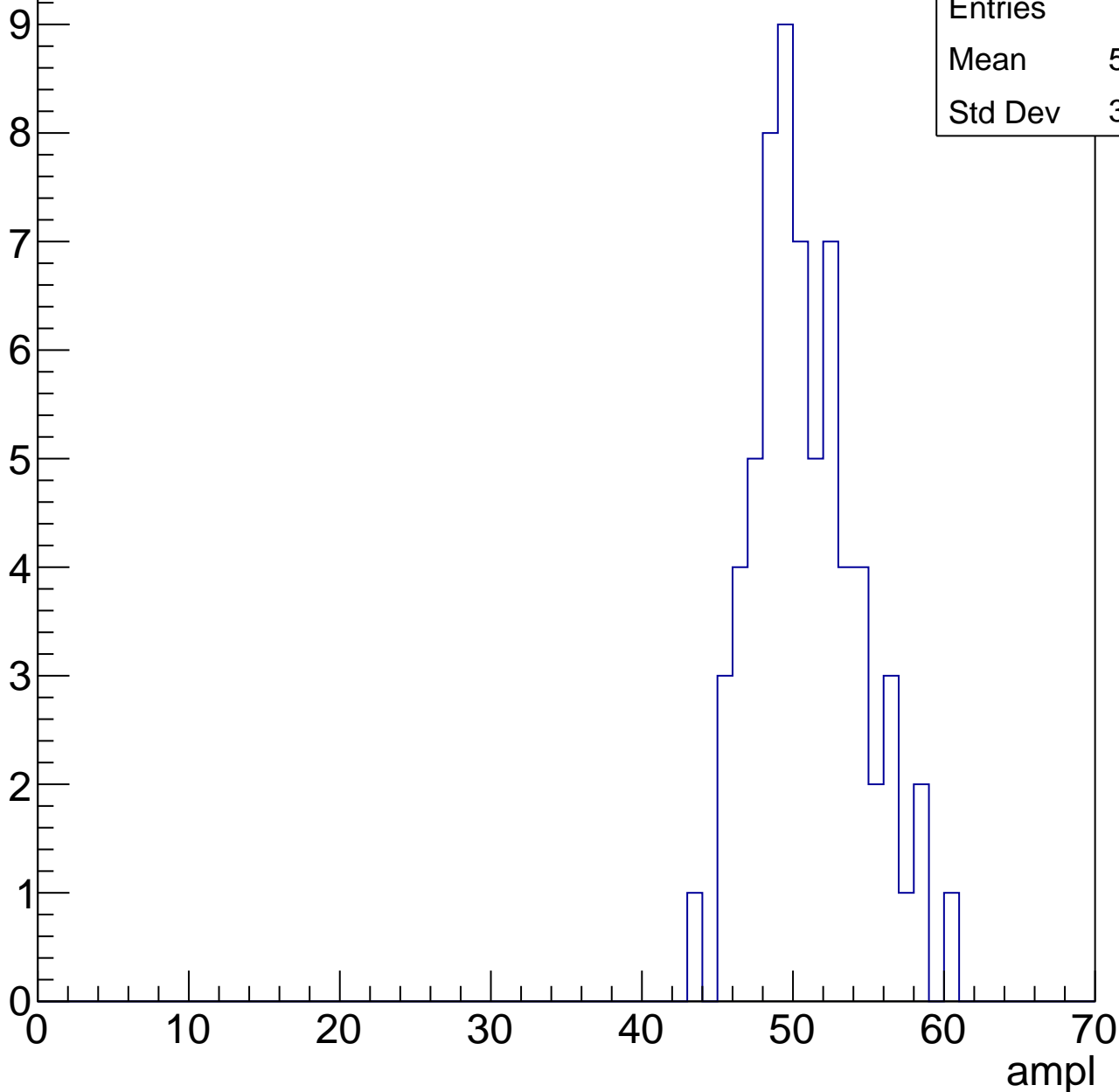


# B1L102S, U8-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

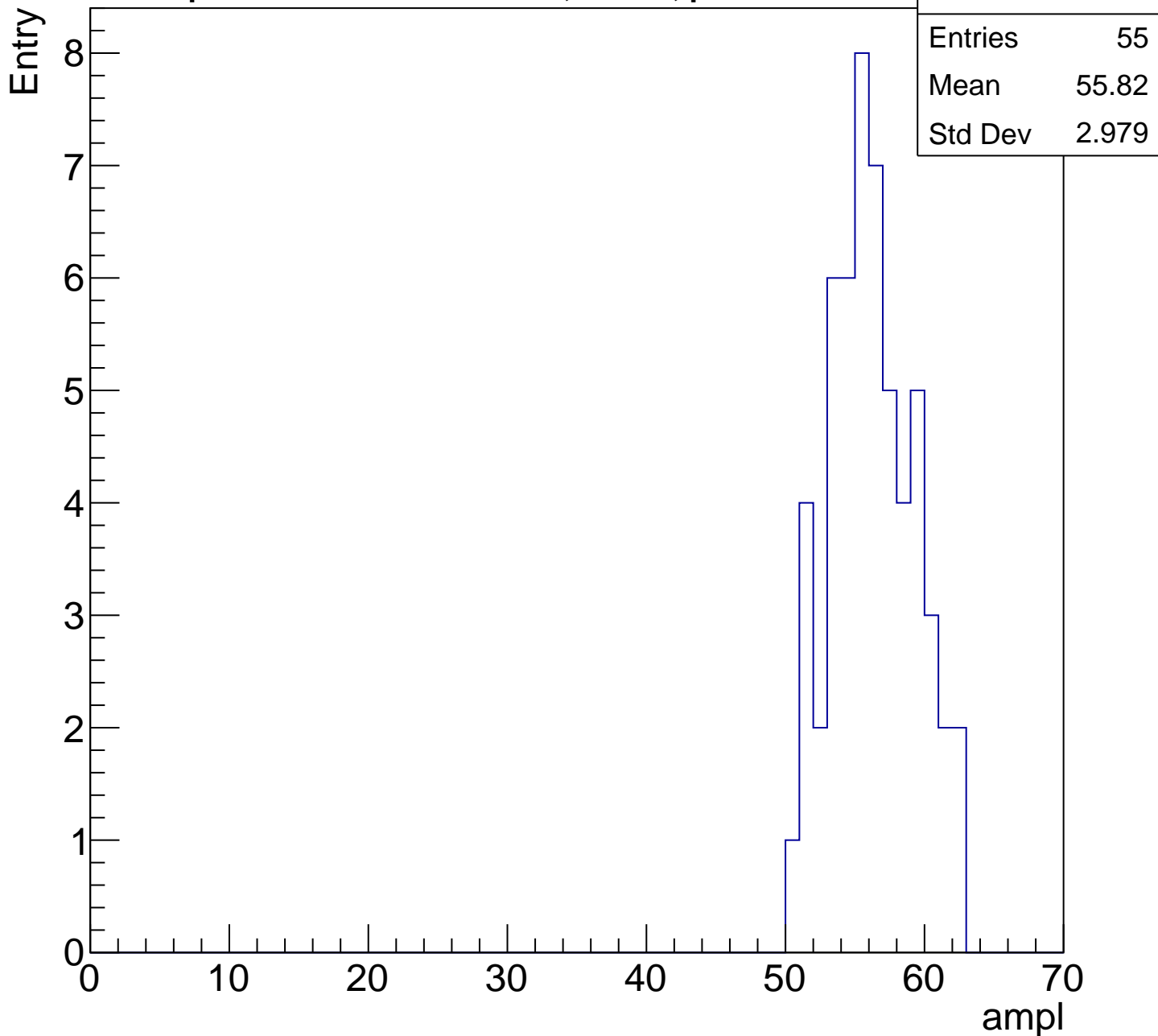
Entry

Entries	66
Mean	50.45
Std Dev	3.543



# B1L102S, U8-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

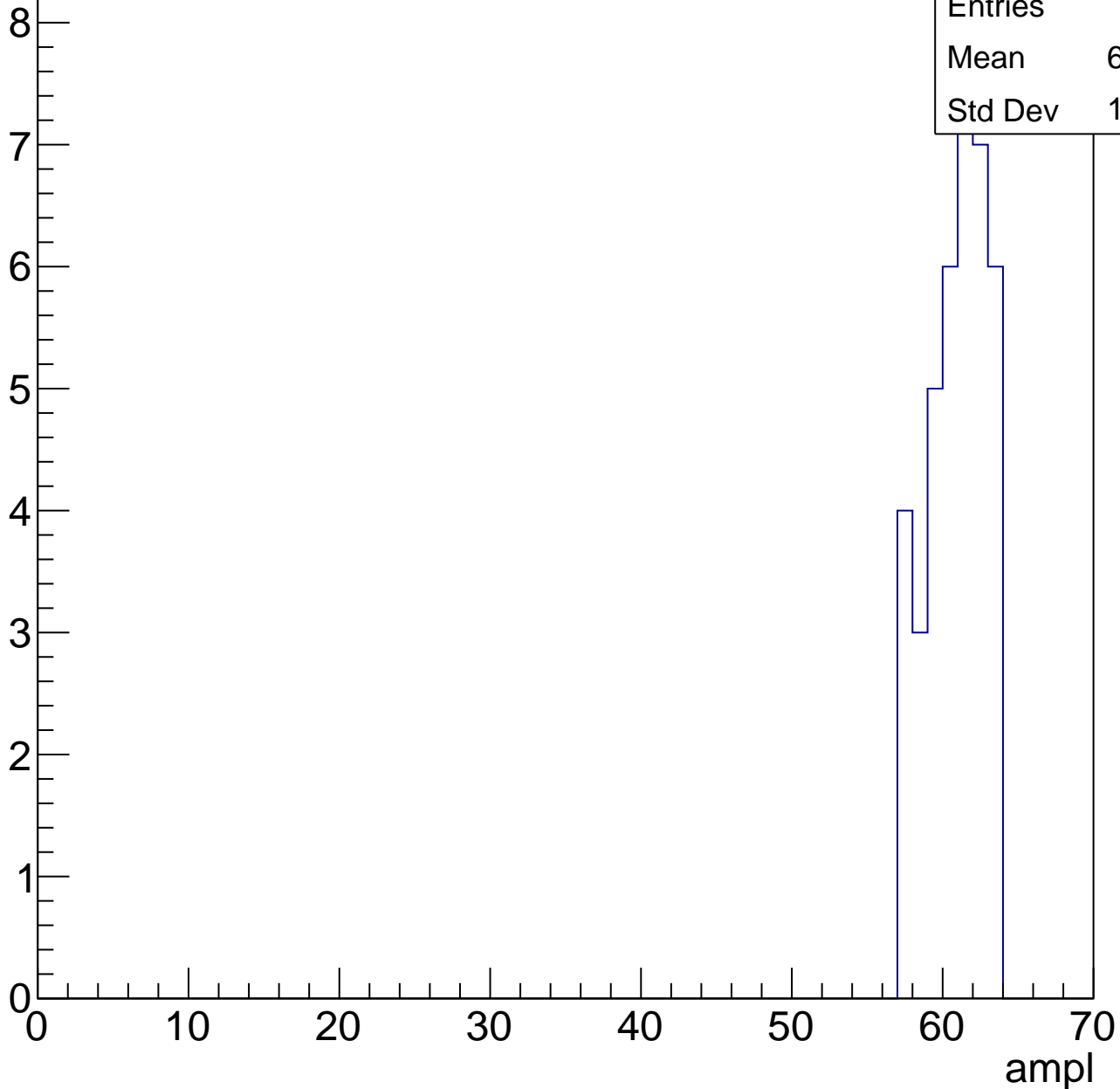


# B1L102S, U8-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

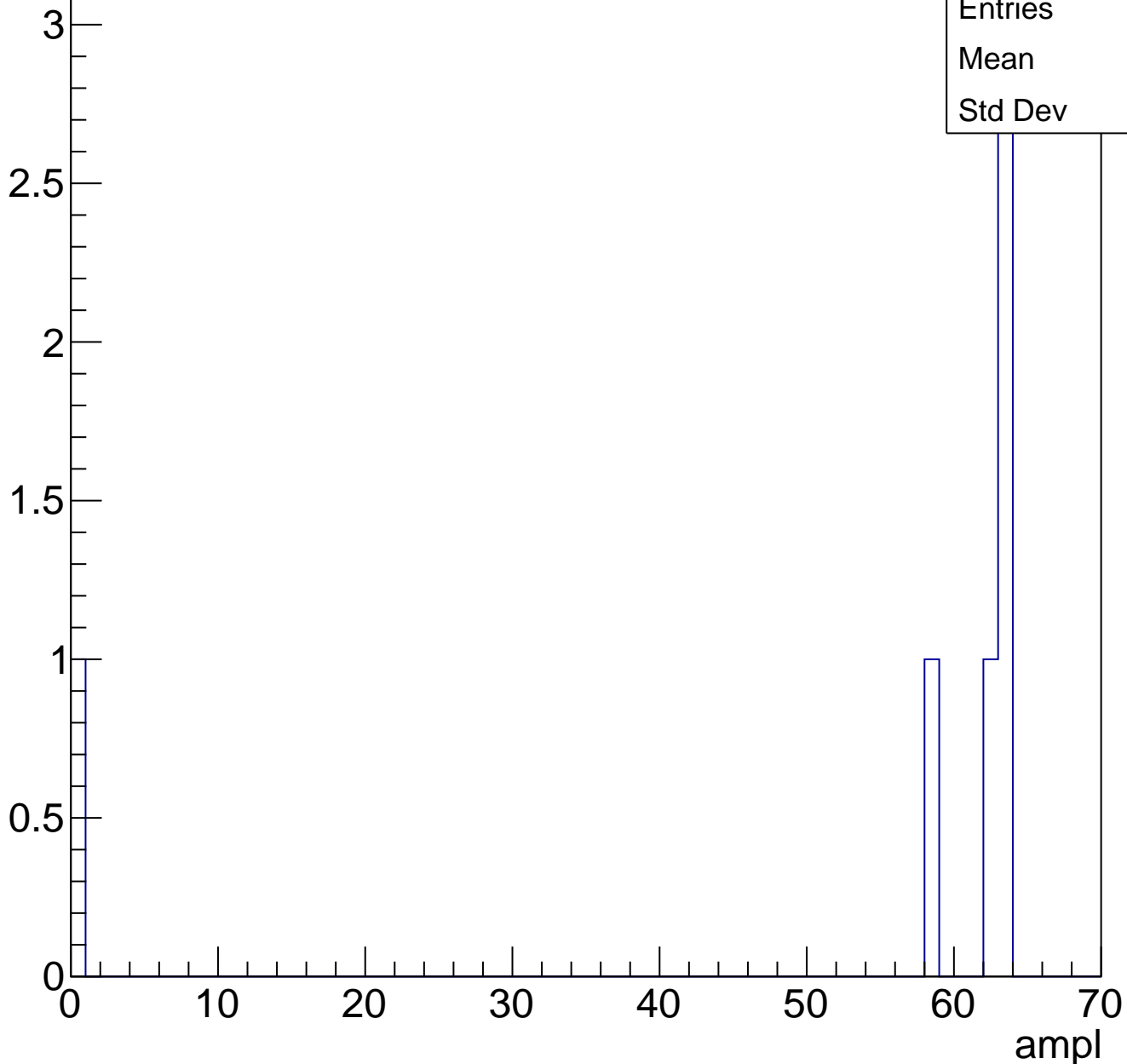
Entries	39
Mean	60.44
Std Dev	1.865



# B1L102S, U8-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

1

Mean

63

Std Dev

0

# B1L102S, U8-ch25, adc0

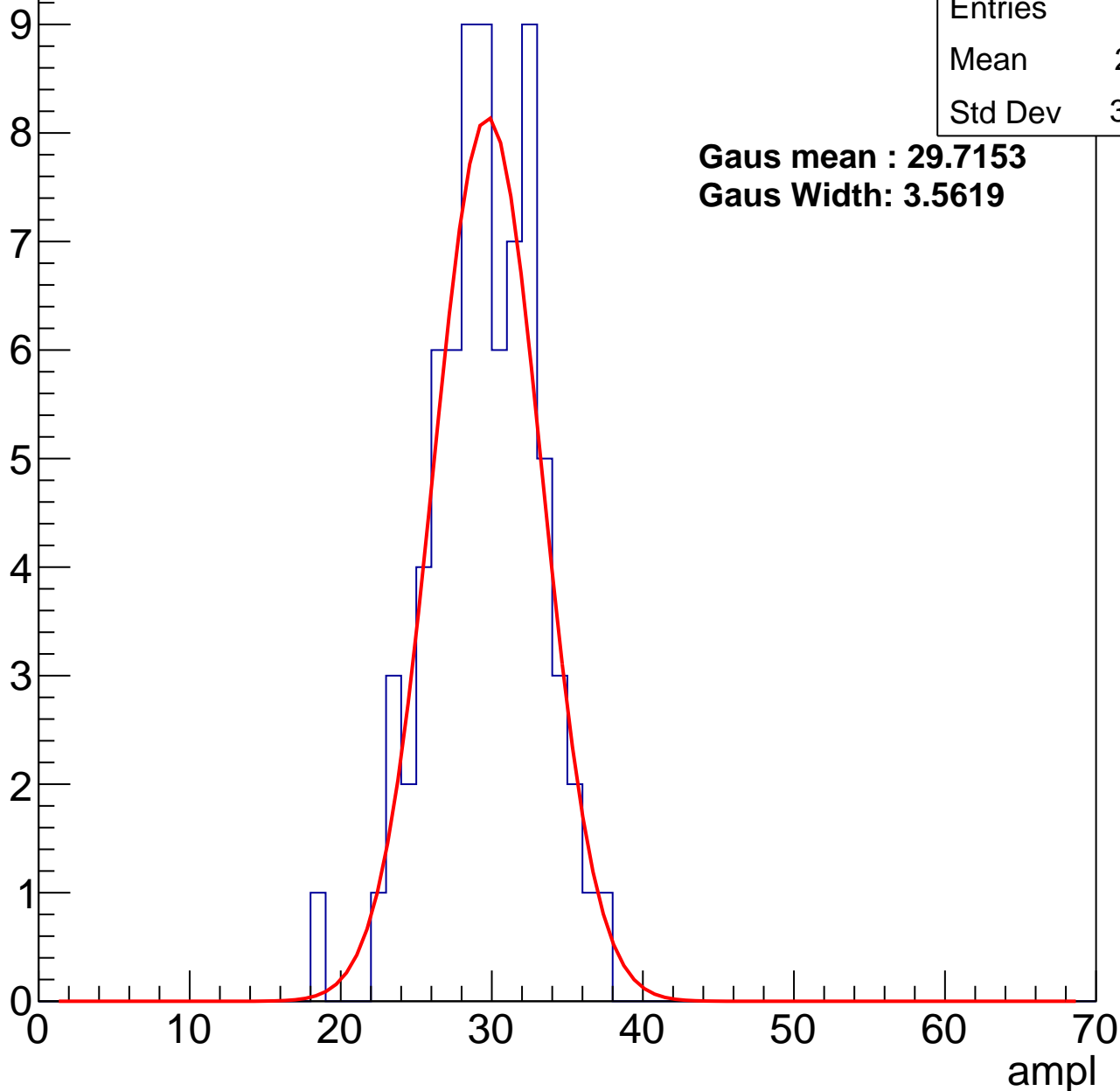
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	29.11
Std Dev	3.527

**Gaus mean : 29.7153**

**Gaus Width: 3.5619**



# B1L102S, U8-ch25, adc1

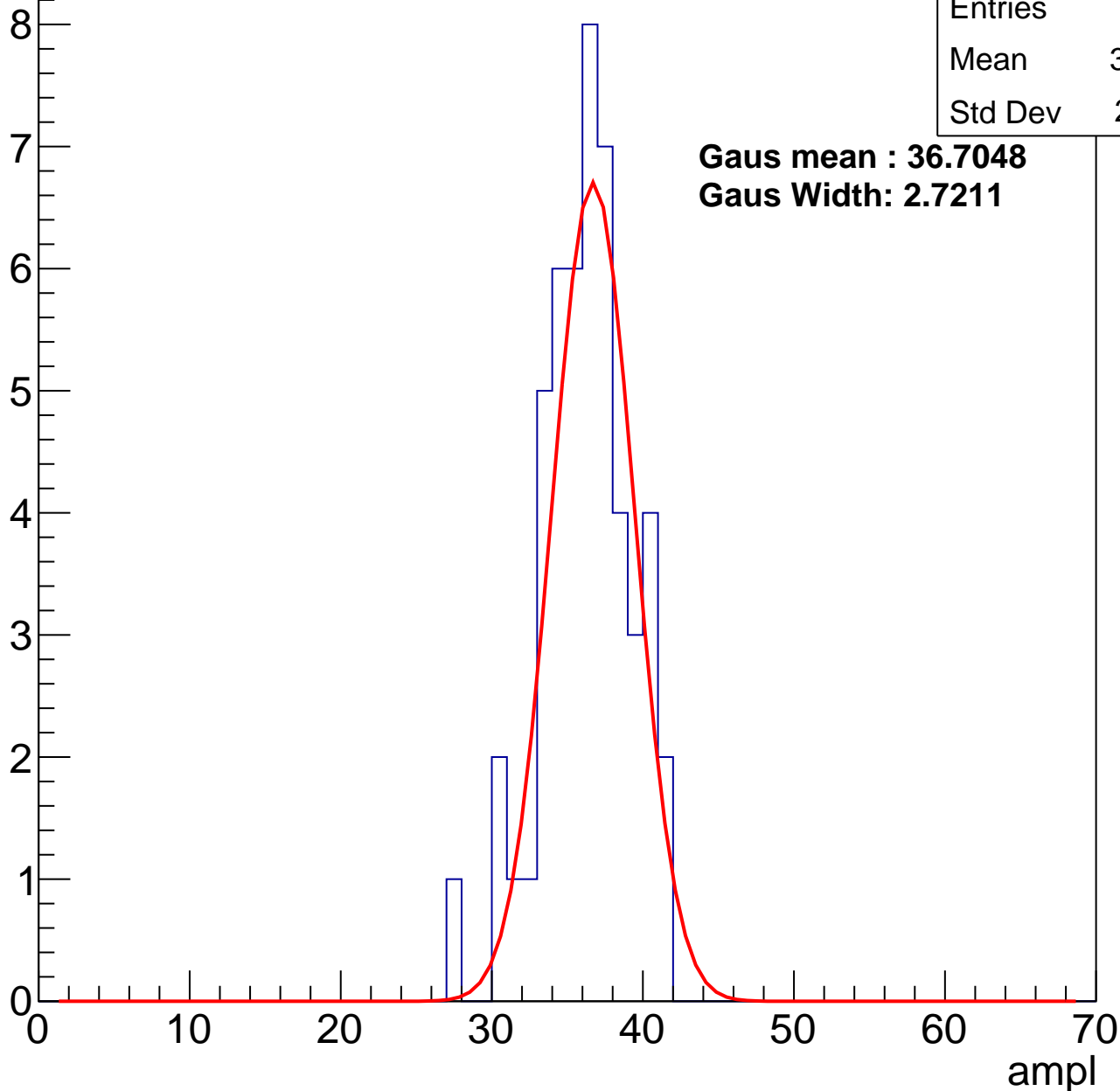
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	35.74
Std Dev	2.931

**Gaus mean : 36.7048**

**Gaus Width: 2.7211**



# B1L102S, U8-ch25, adc2

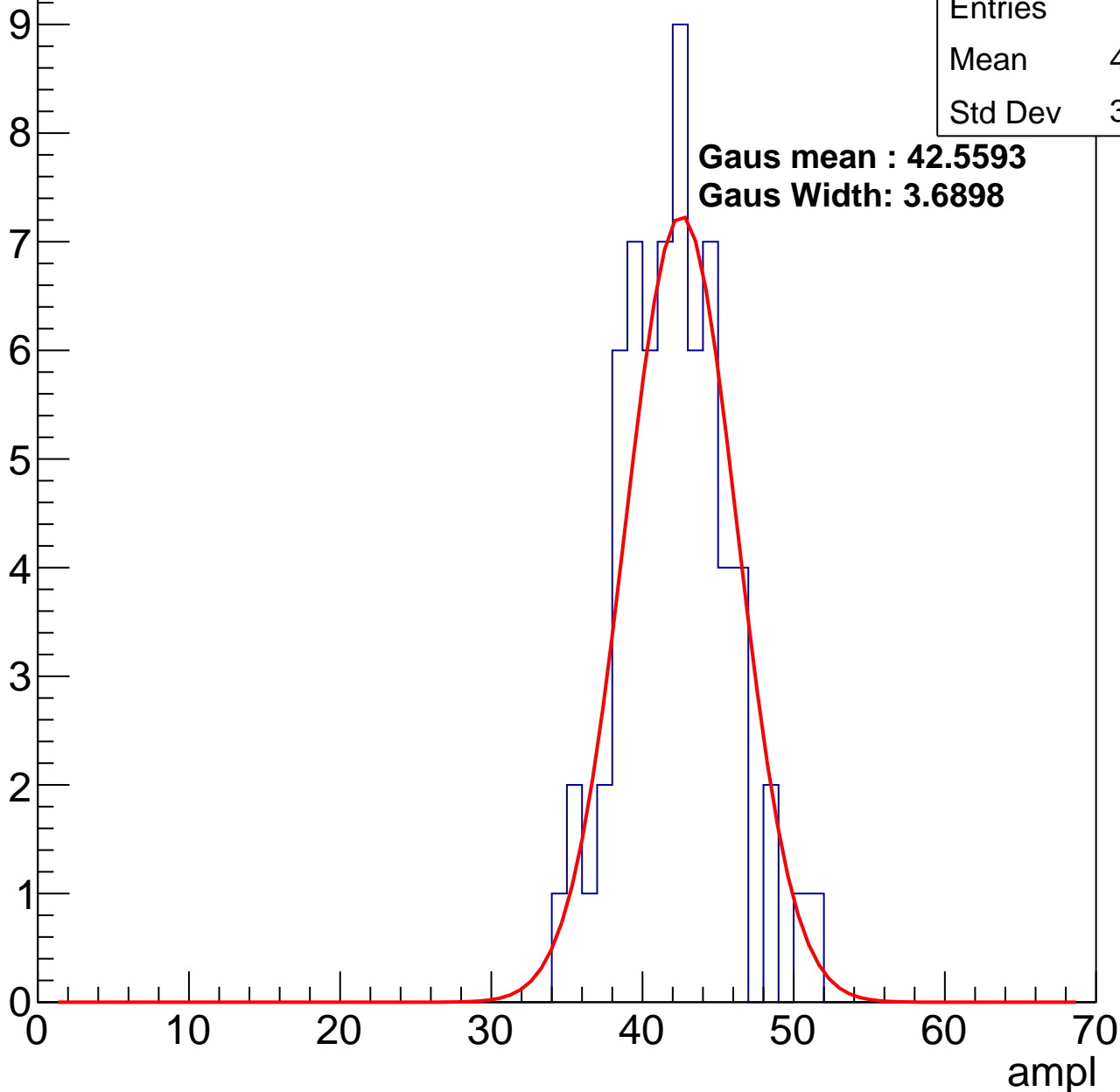
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	41.62
Std Dev	3.437

**Gaus mean : 42.5593**

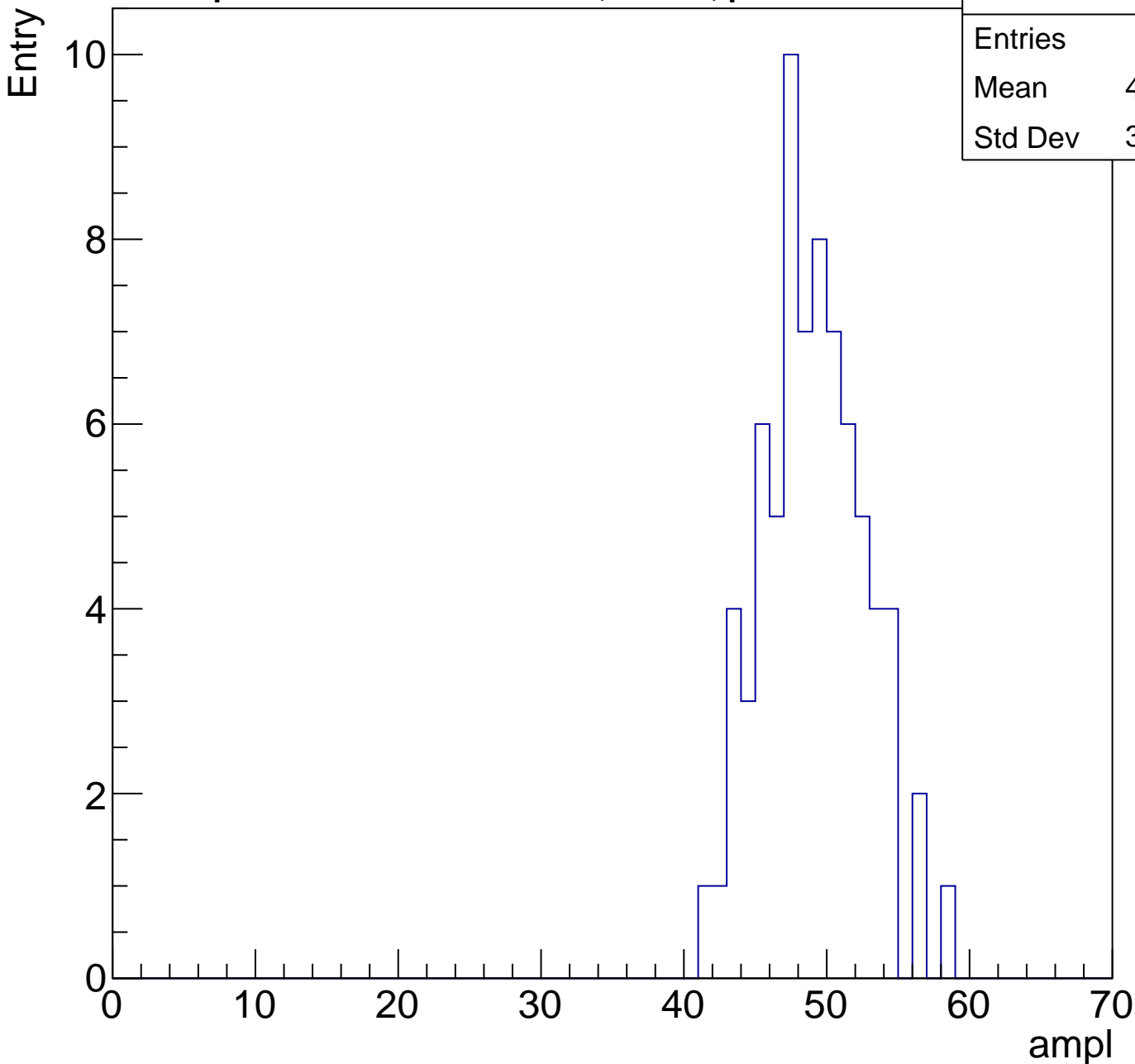
**Gaus Width: 3.6898**



# B1L102S, U8-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

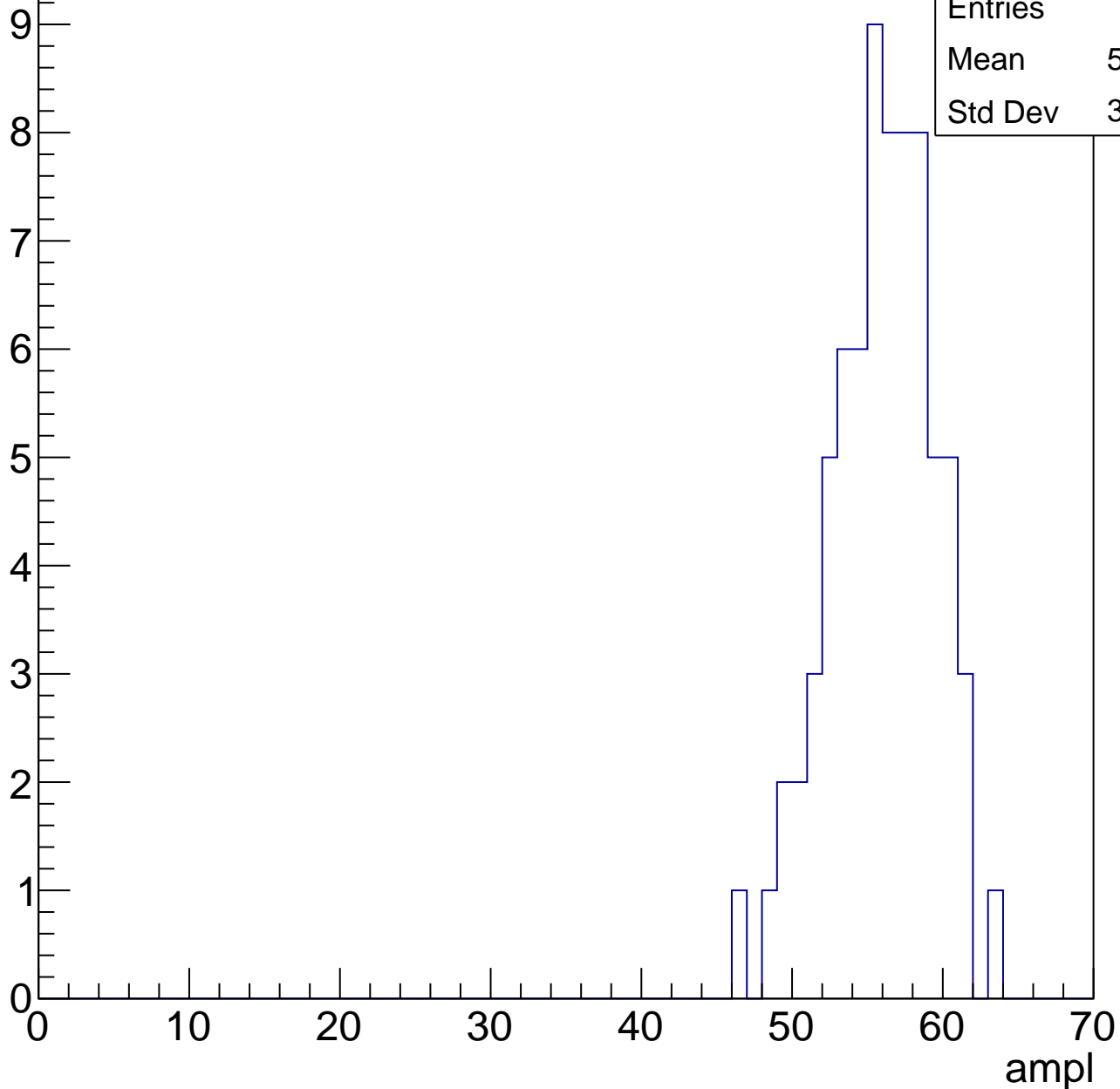
Entries	74
Mean	48.64
Std Dev	3.543



# B1L102S, U8-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



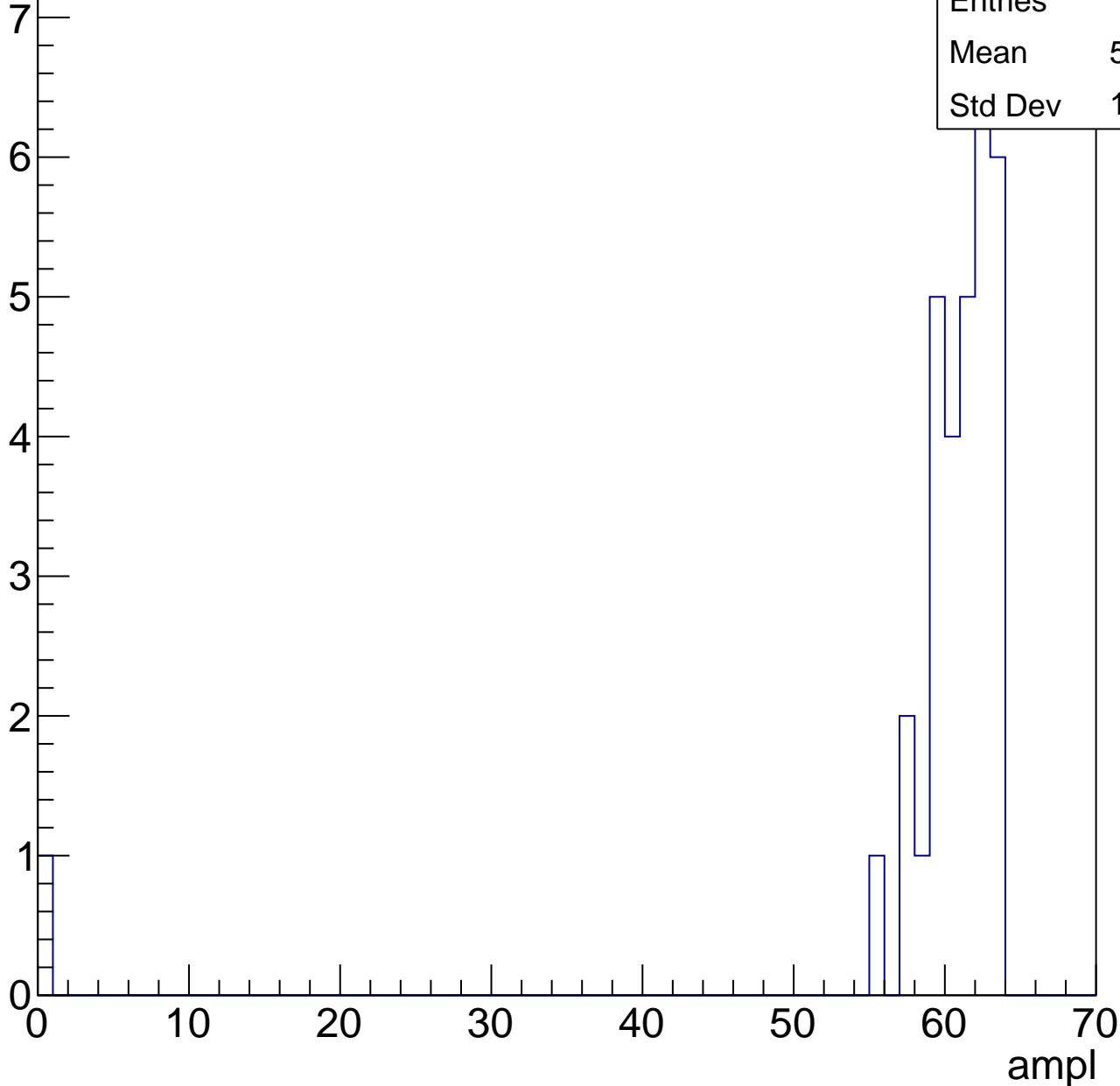
Entries	73
Mean	55.49
Std Dev	3.405

# B1L102S, U8-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	32
Mean	58.72
Std Dev	10.73



# B1L102S, U8-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

9

Mean

61.89

Std Dev

0.9938



# B1L102S, U8-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U8-ch26, adc0

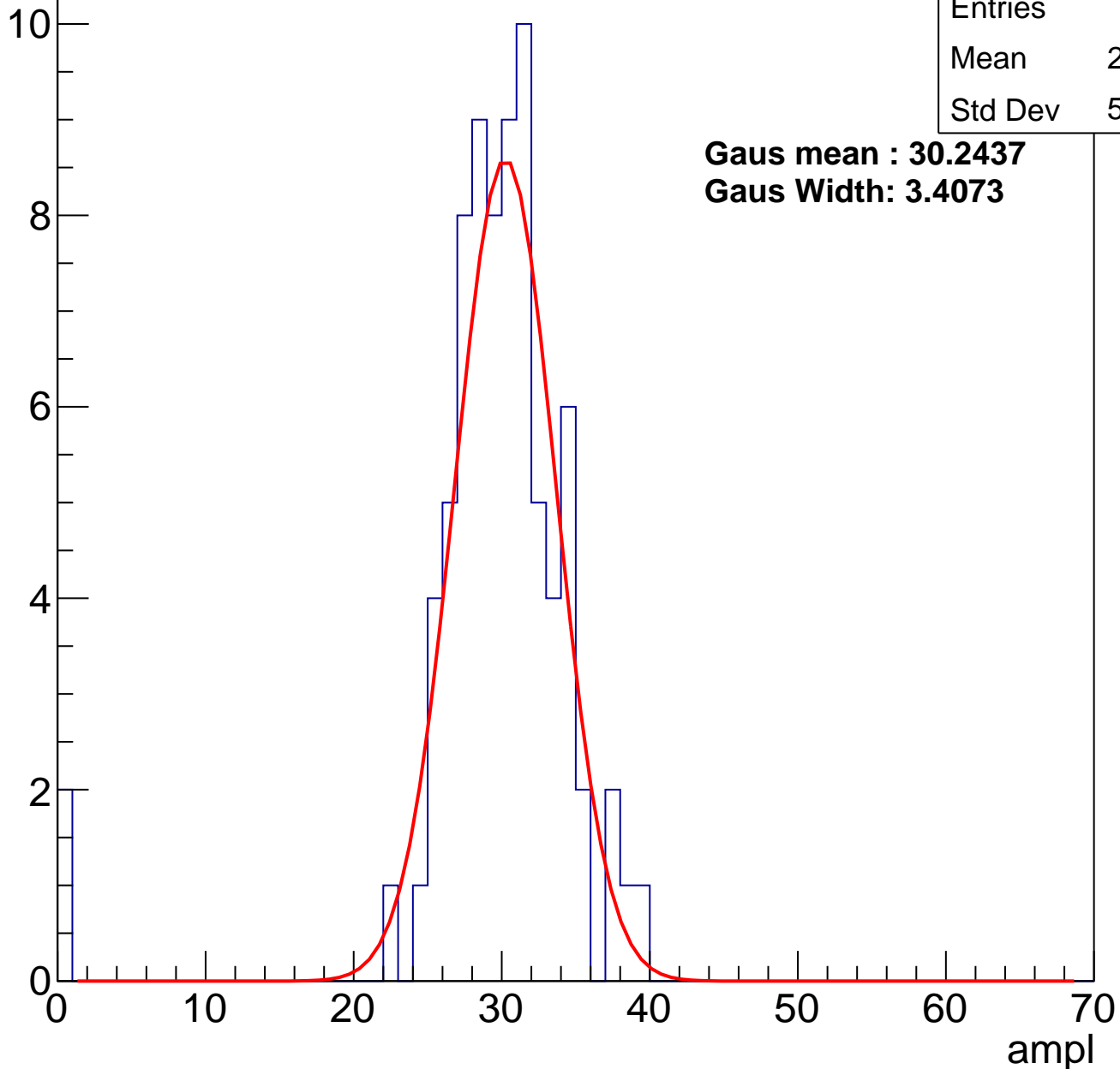
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	78
Mean	29.14
Std Dev	5.766

**Gaus mean : 30.2437**

**Gaus Width: 3.4073**

Entry



# B1L102S, U8-ch26, adc1

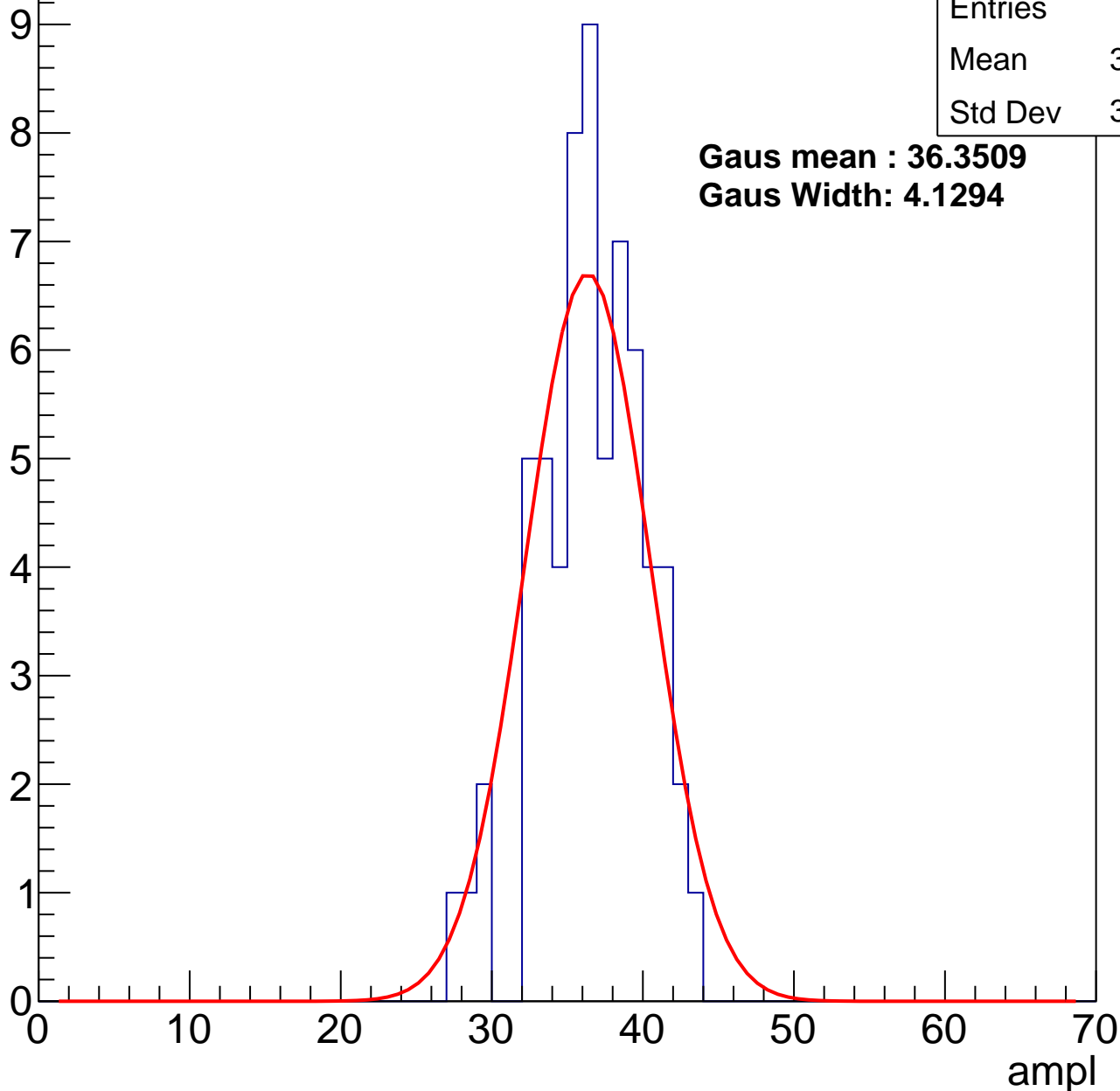
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	36.16
Std Dev	3.452

**Gaus mean : 36.3509**

**Gaus Width: 4.1294**

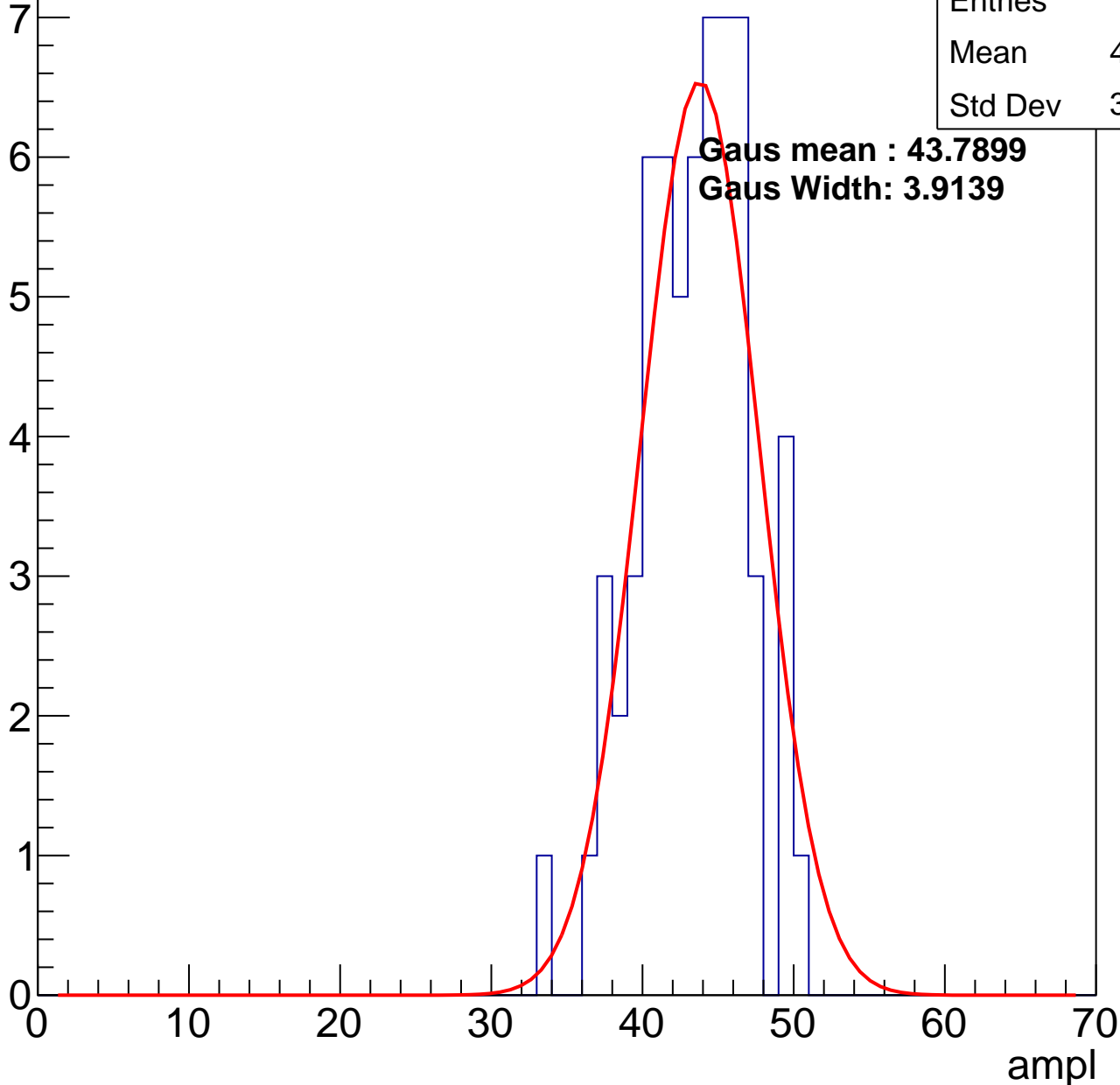


# B1L102S, U8-ch26, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

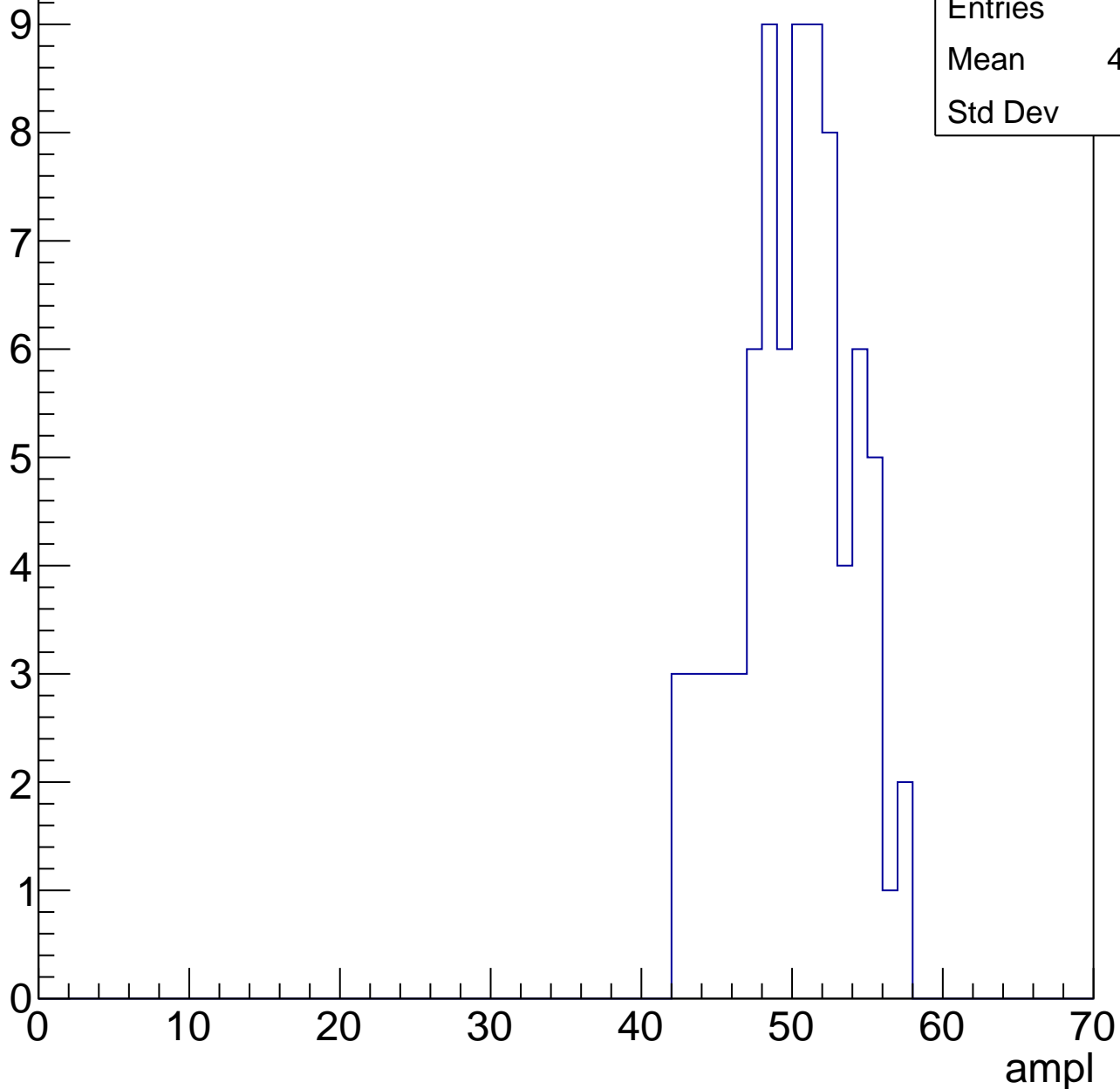
Entries	62
Mean	42.89
Std Dev	3.538



# B1L102S, U8-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

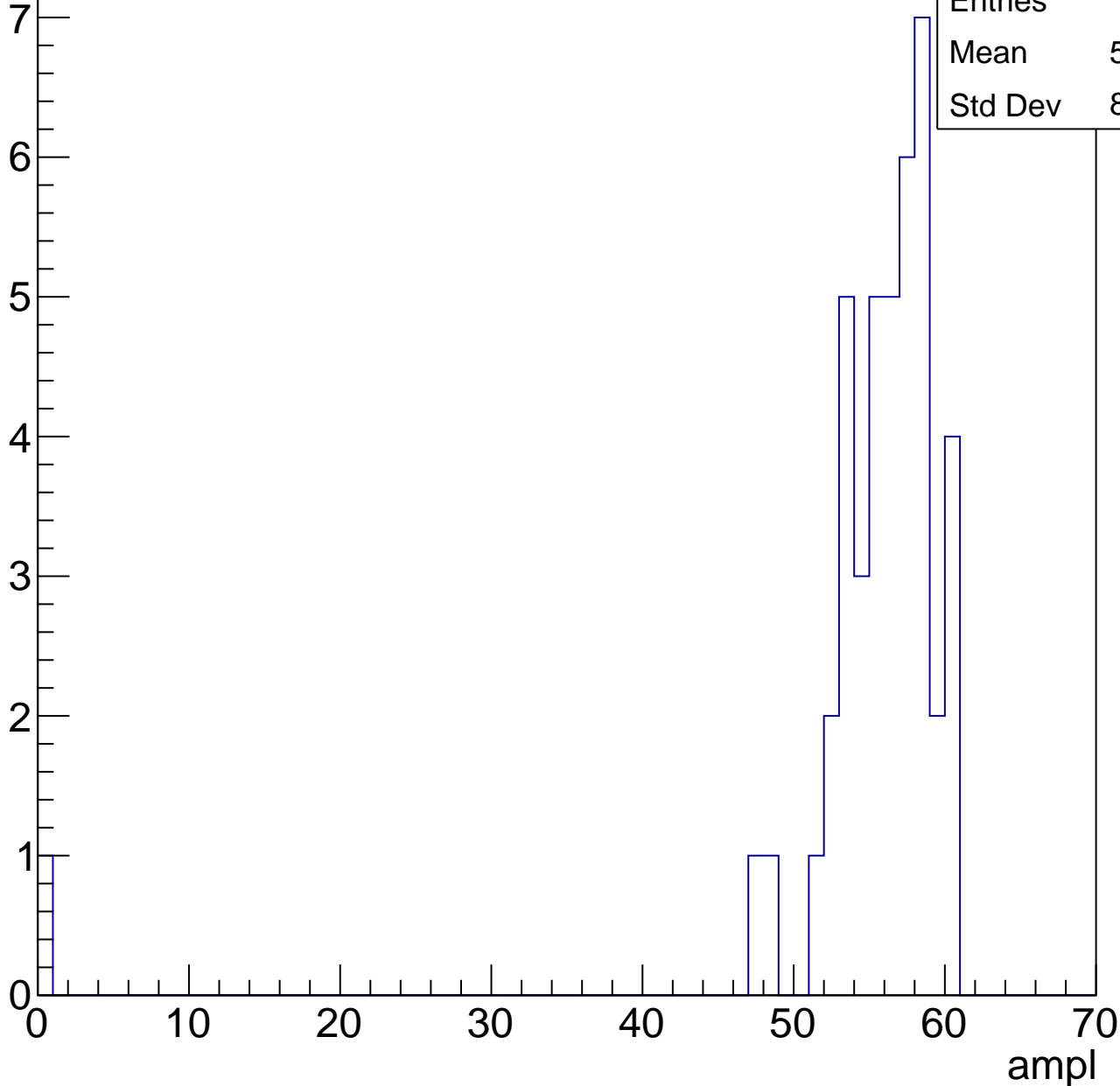


# B1L102S, U8-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	43
Mean	54.37
Std Dev	8.895

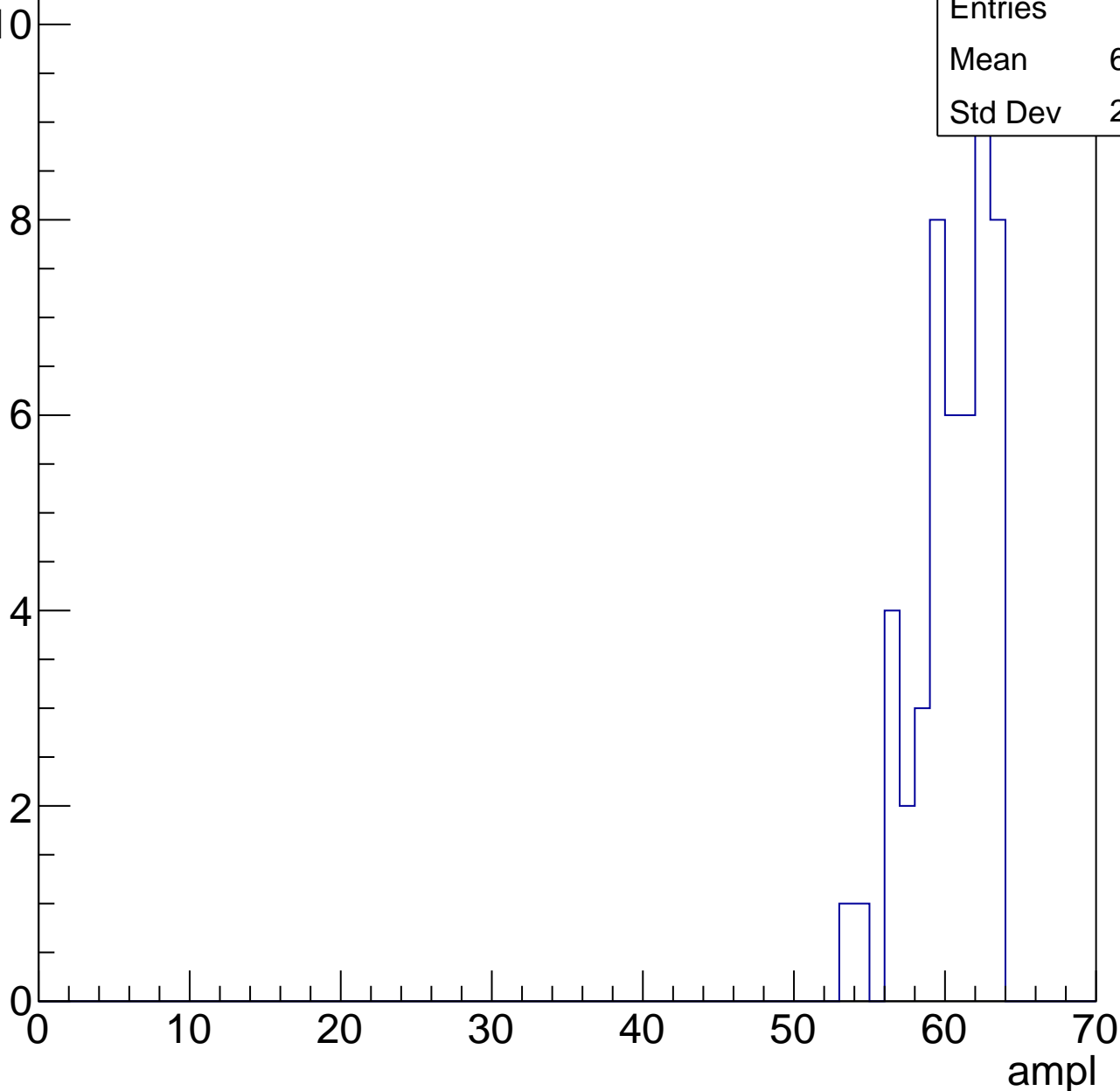


# B1L102S, U8-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

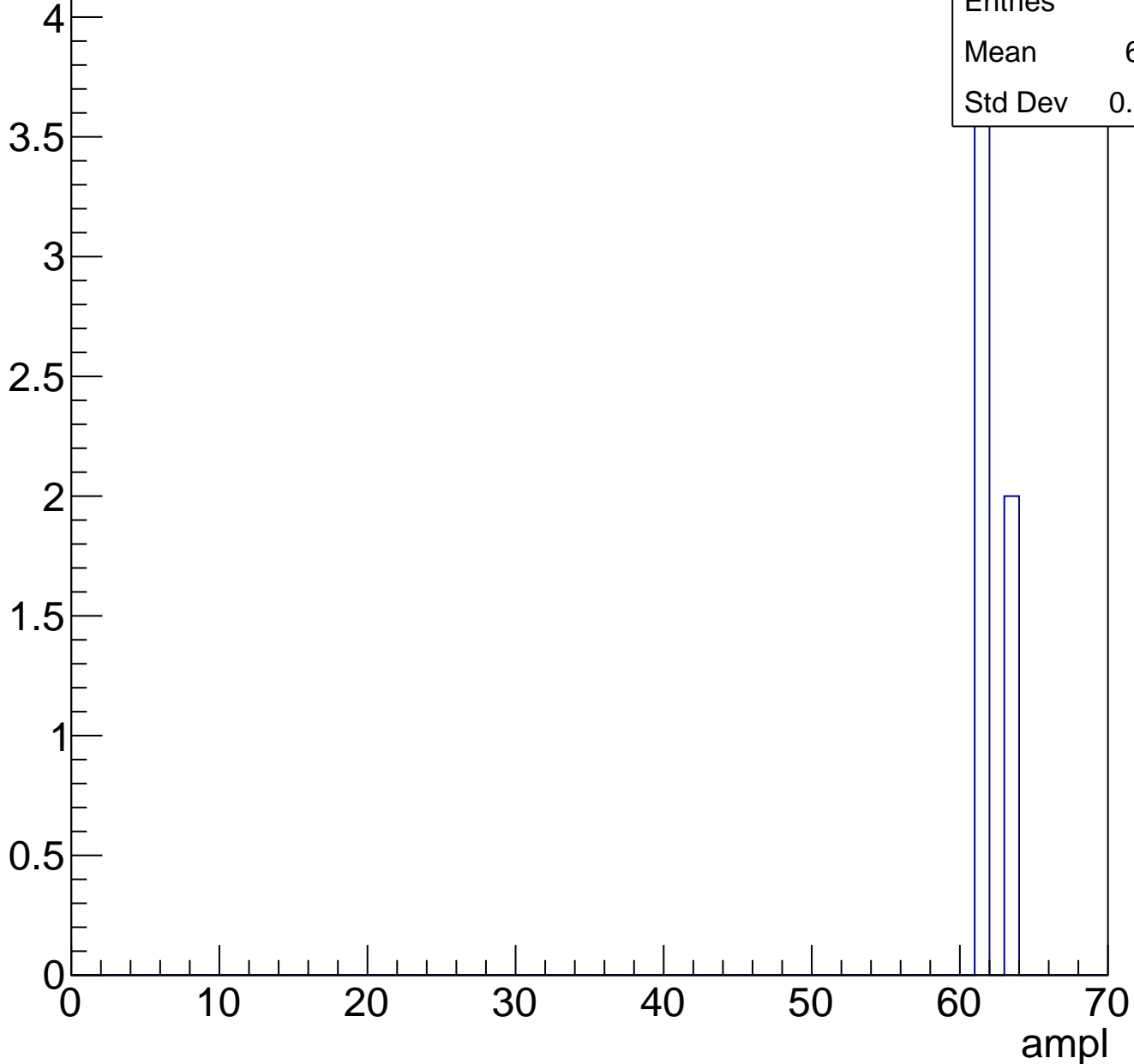
Entries	49
Mean	60.02
Std Dev	2.495



# B1L102S, U8-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch27, adc0

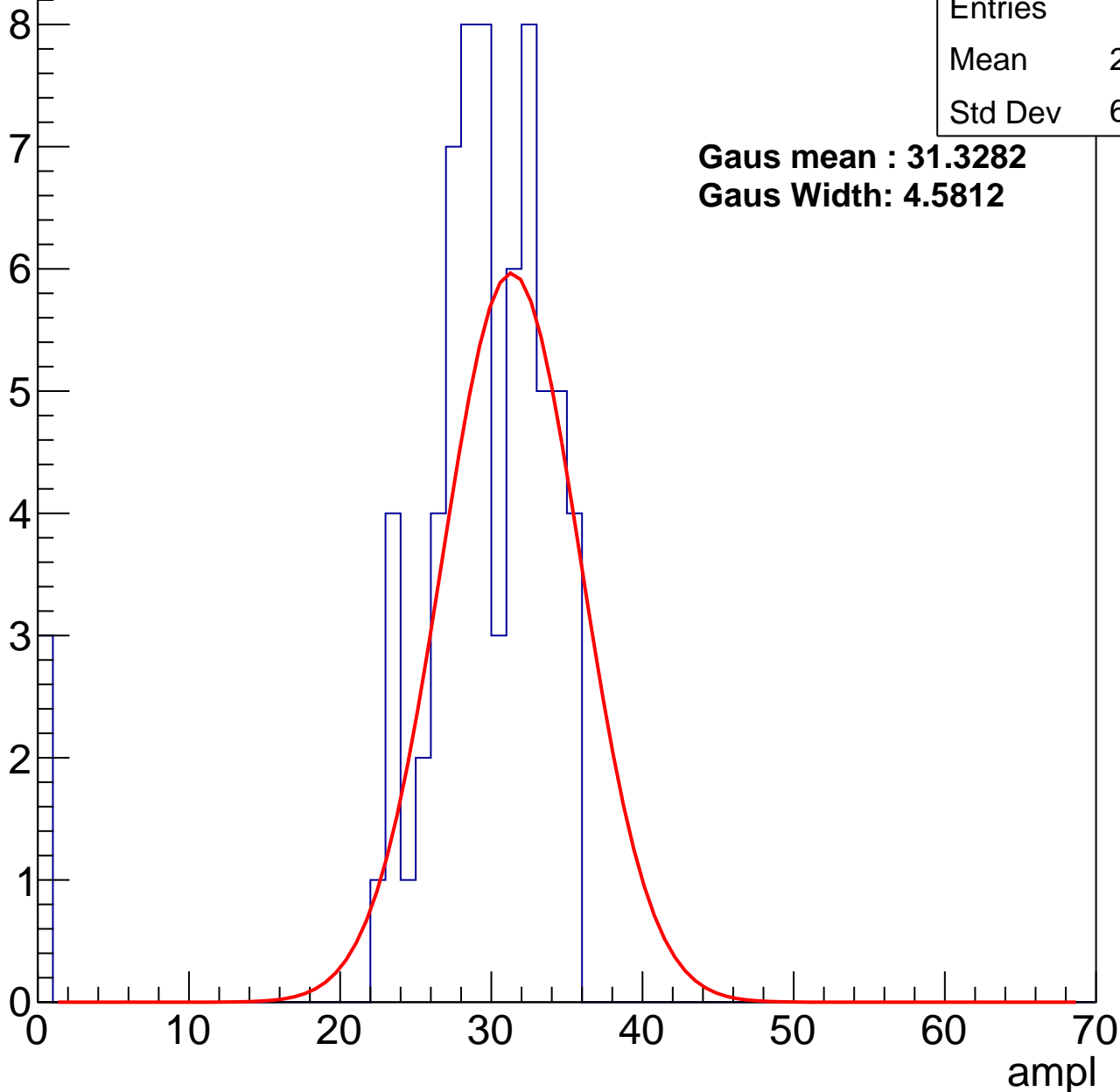
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	28.17
Std Dev	6.859

**Gaus mean : 31.3282**

**Gaus Width: 4.5812**



# B1L102S, U8-ch27, adc1

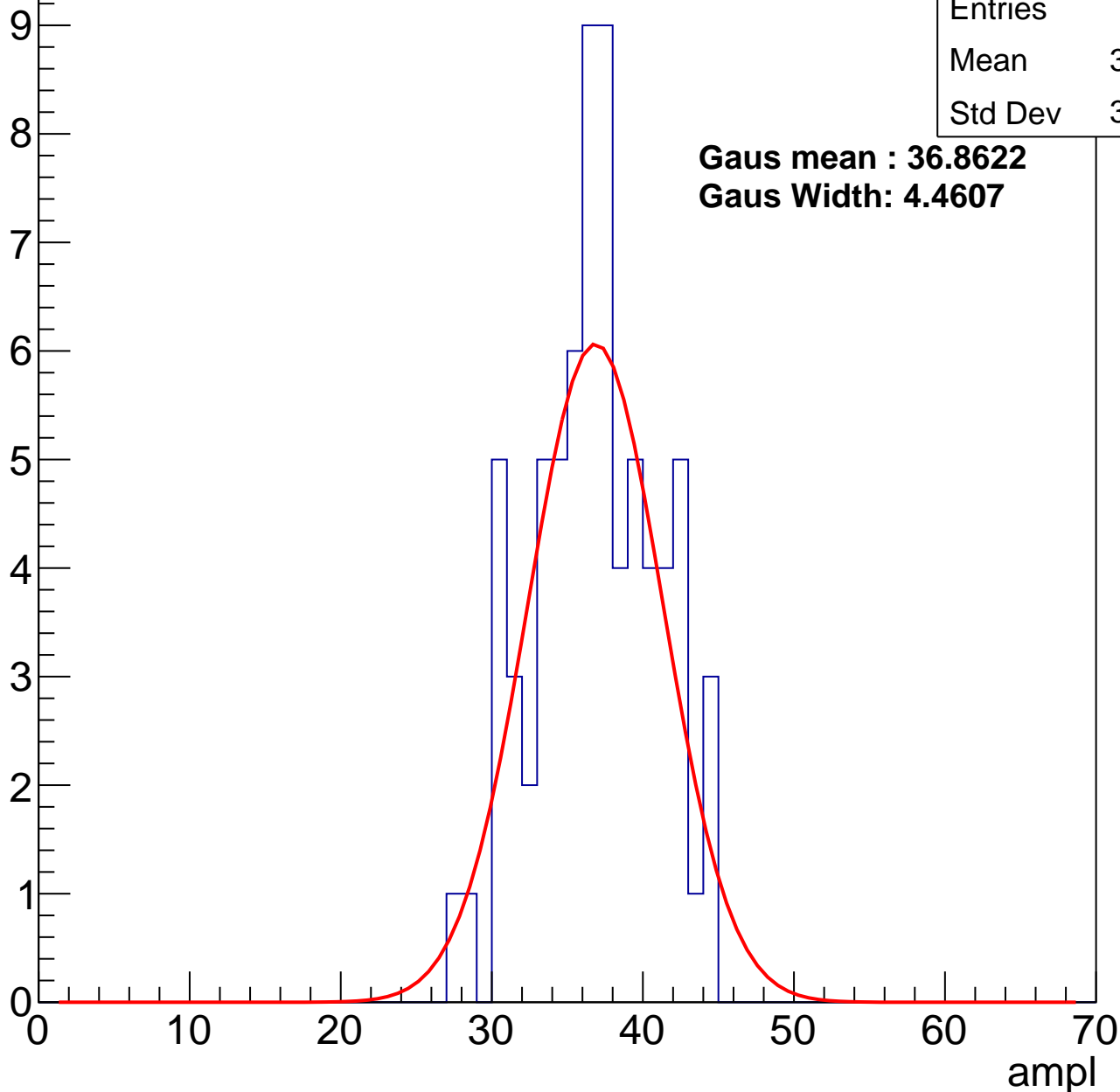
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	36.39
Std Dev	3.992

**Gaus mean : 36.8622**

**Gaus Width: 4.4607**



# B1L102S, U8-ch27, adc2

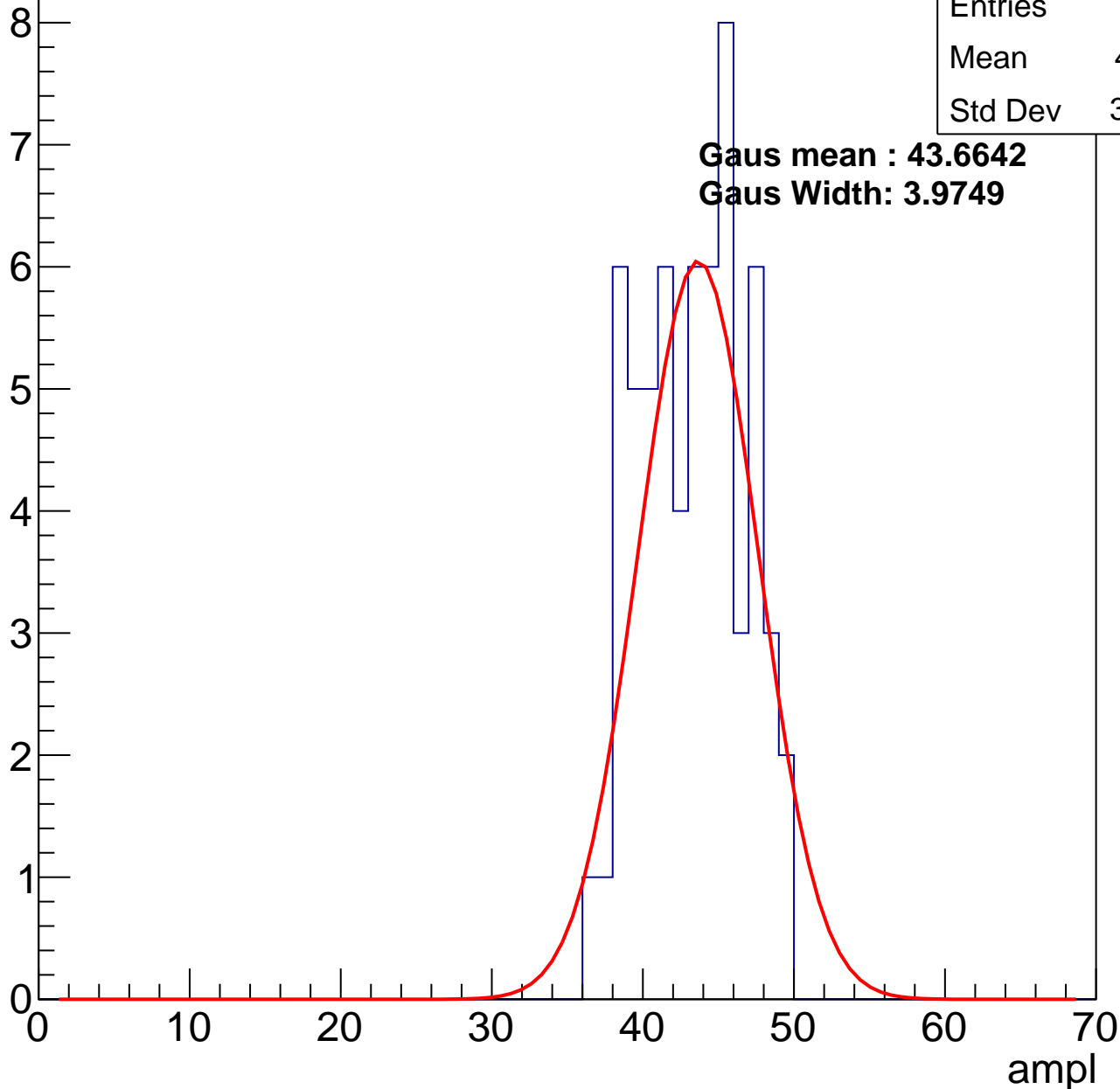
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	42.81
Std Dev	3.345

**Gaus mean : 43.6642**

**Gaus Width: 3.9749**

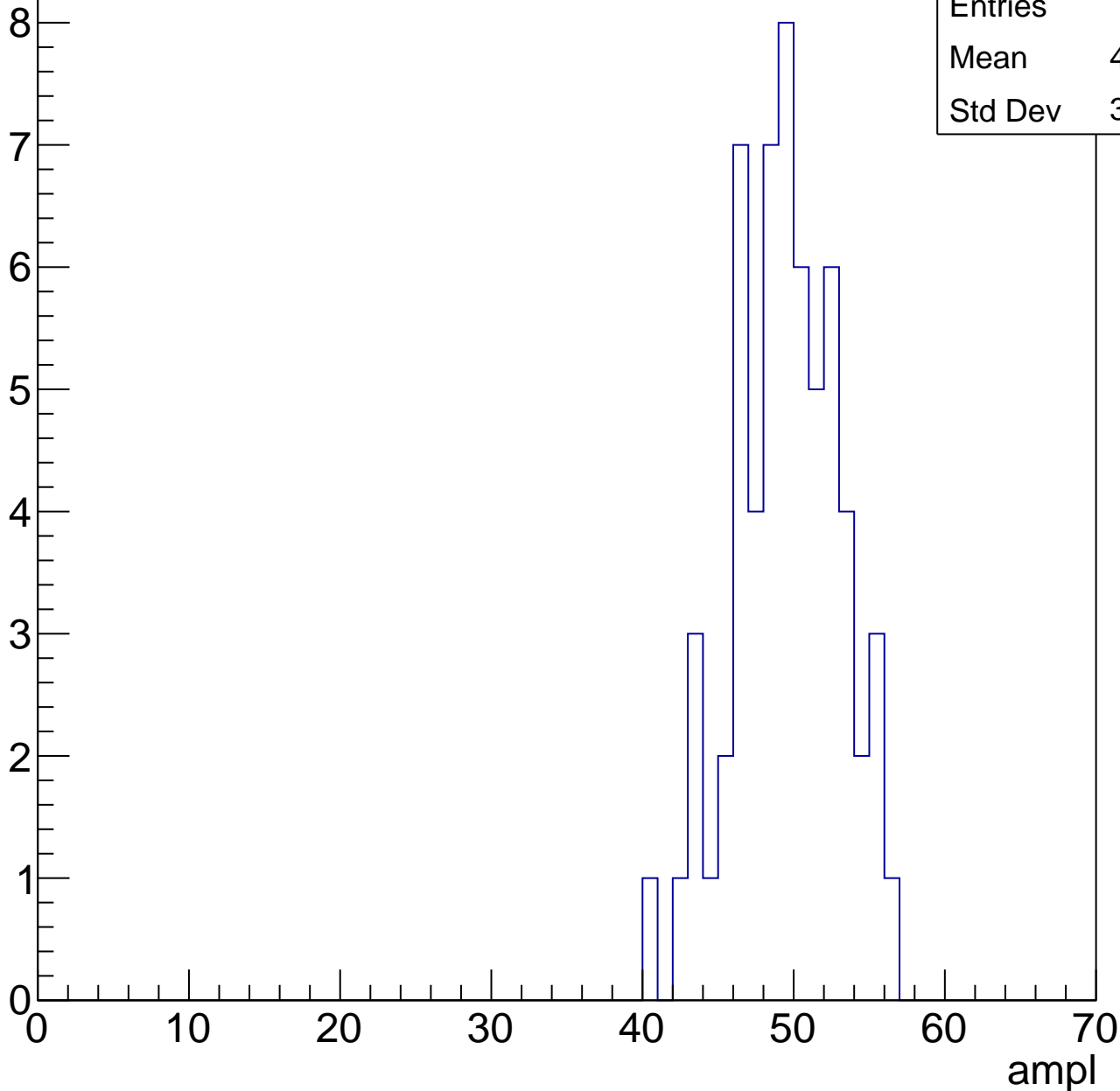


# B1L102S, U8-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

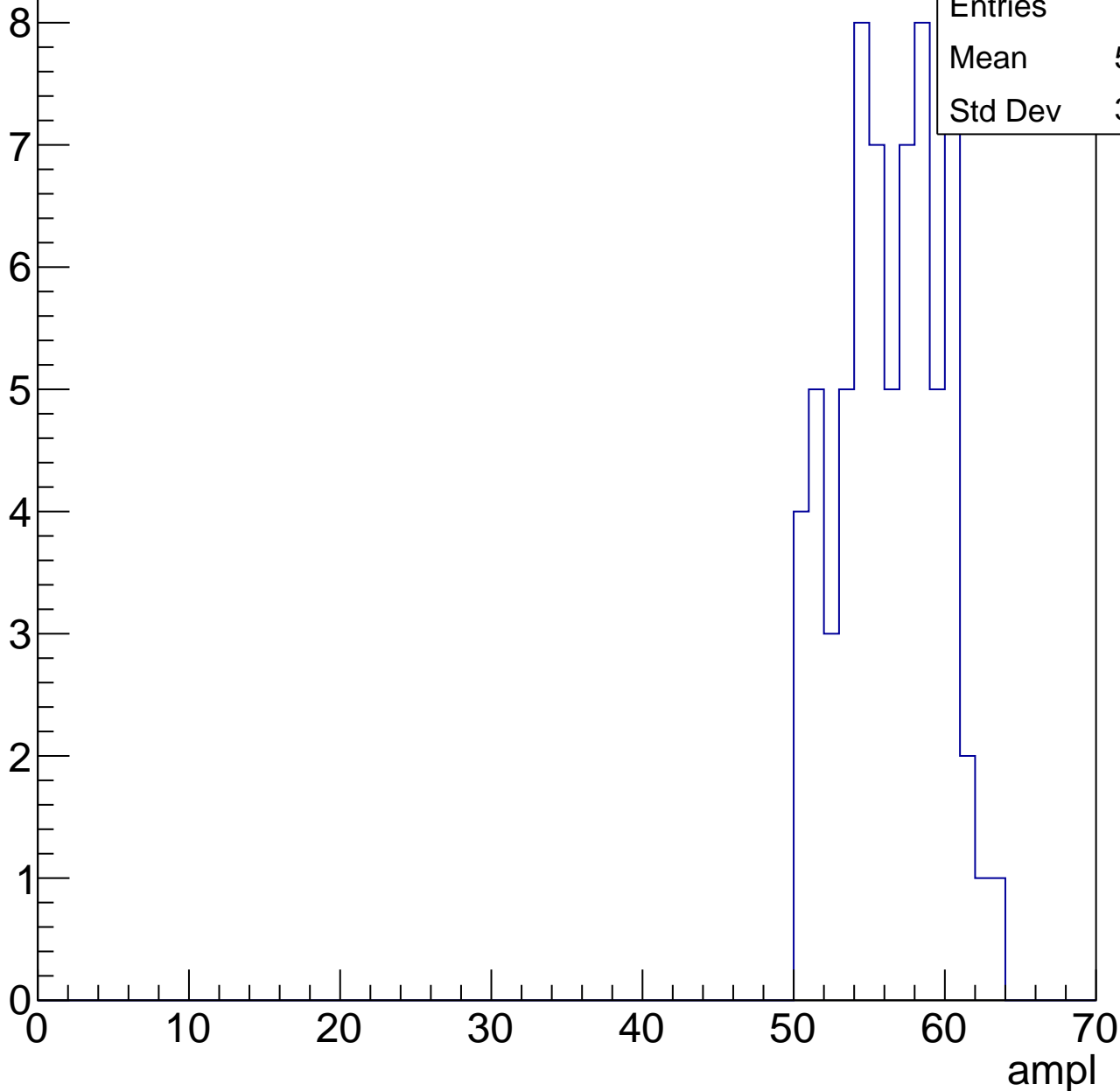
Entries	61
Mean	49.03
Std Dev	3.464



# B1L102S, U8-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

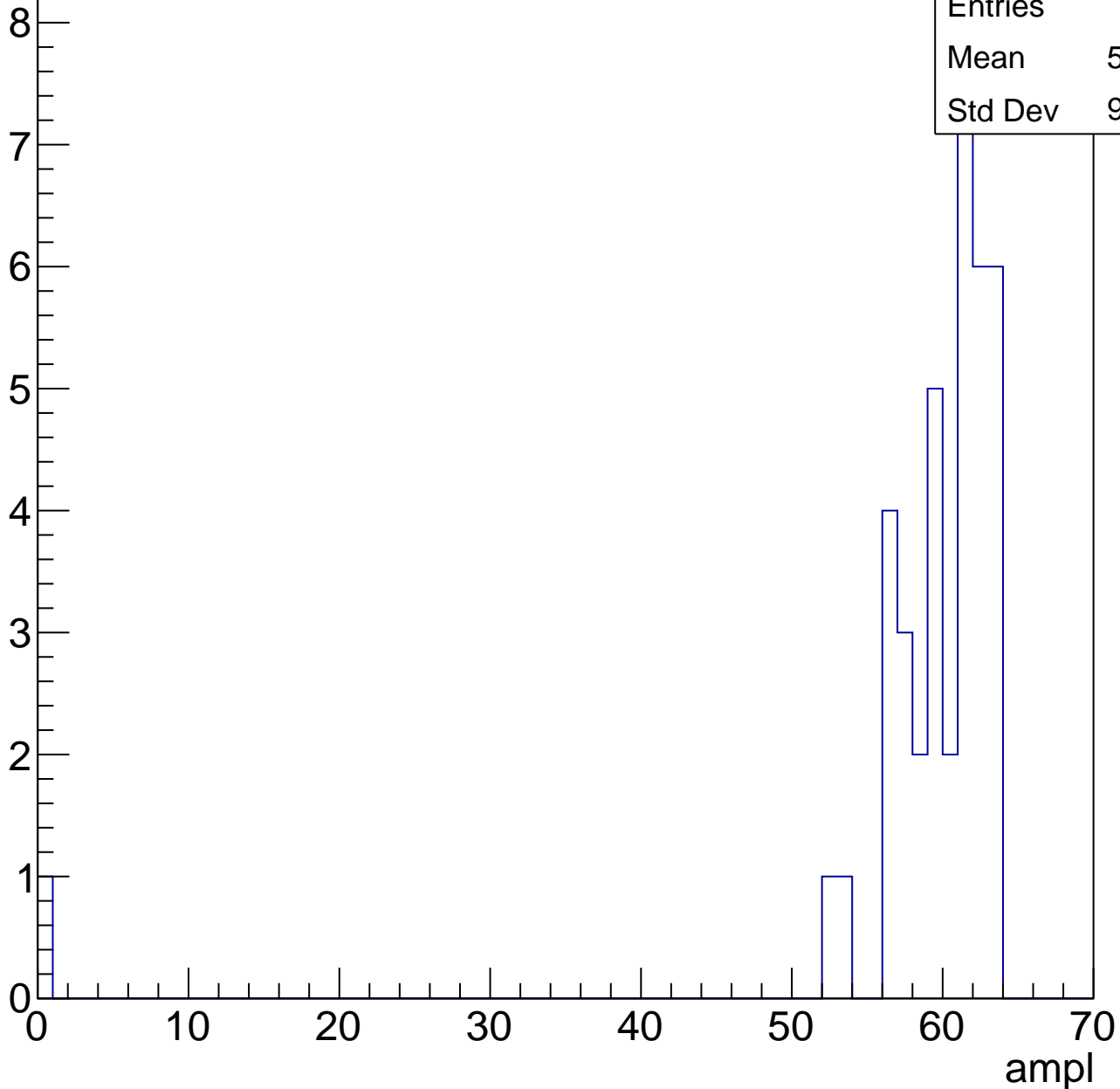


# B1L102S, U8-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	39
Mean	58.18
Std Dev	9.837



# B1L102S, U8-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch28, adc0

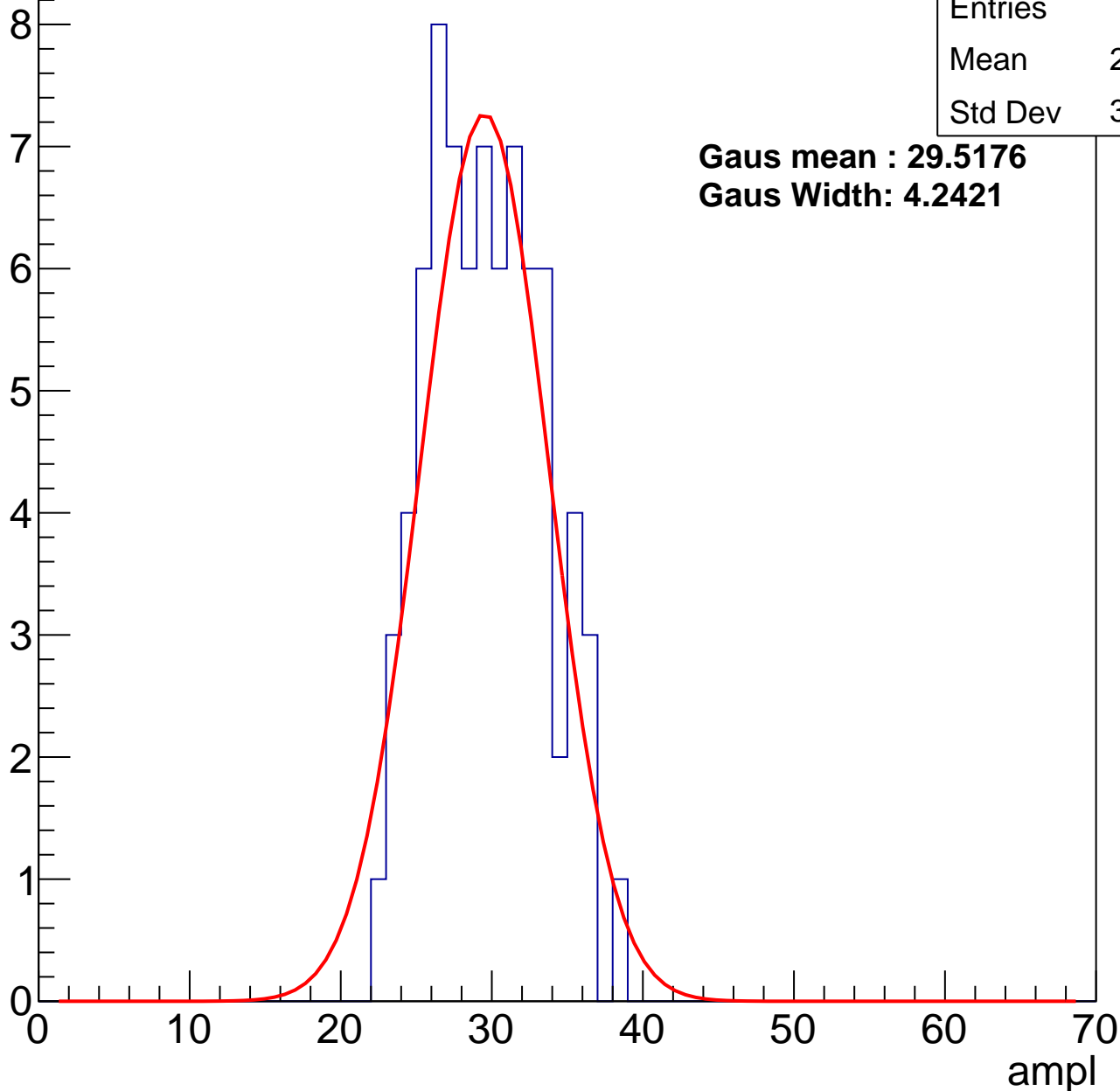
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	29.17
Std Dev	3.715

**Gaus mean : 29.5176**

**Gaus Width: 4.2421**



# B1L102S, U8-ch28, adc1

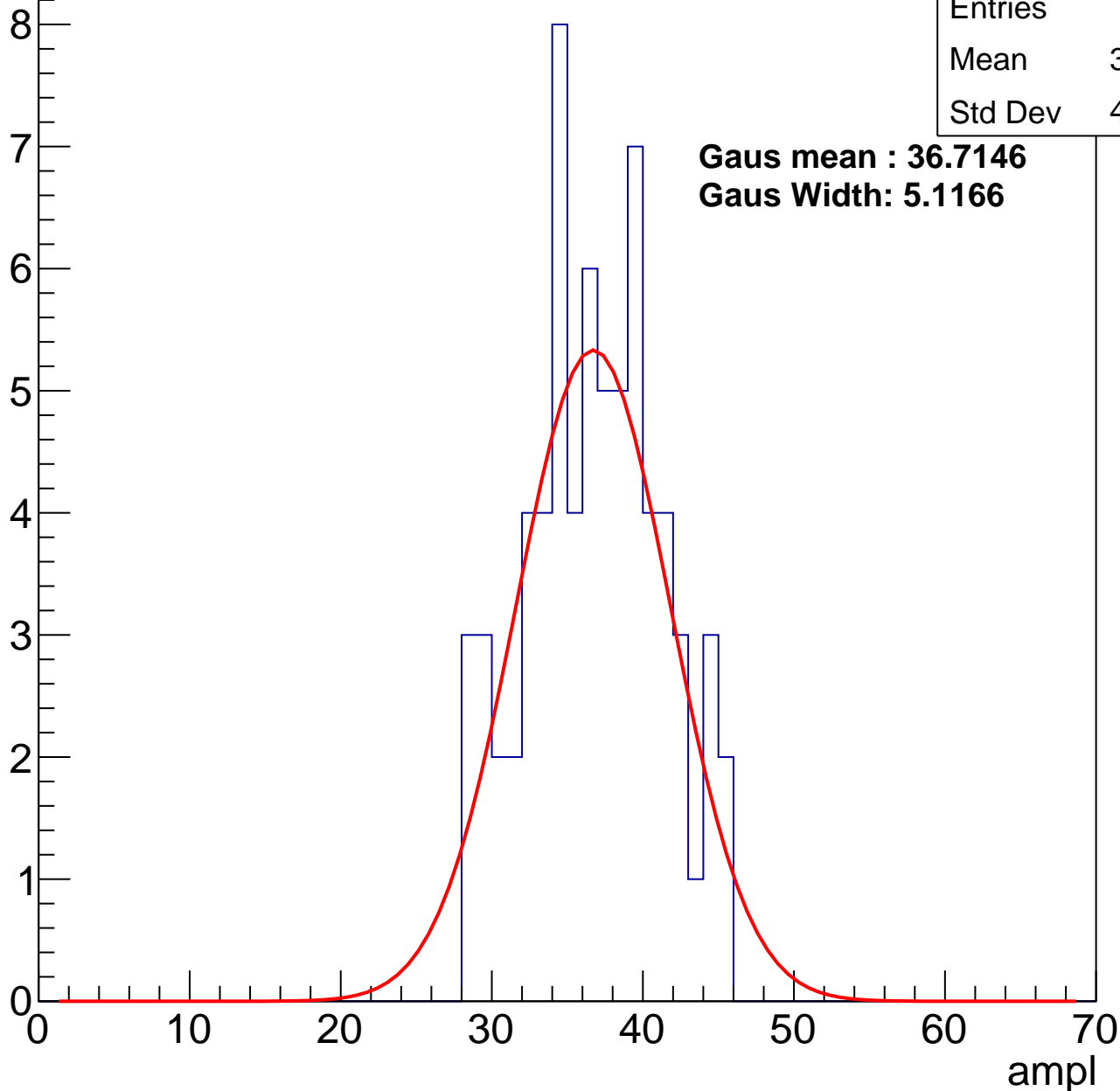
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	36.34
Std Dev	4.394

**Gaus mean : 36.7146**

**Gaus Width: 5.1166**



# B1L102S, U8-ch28, adc2

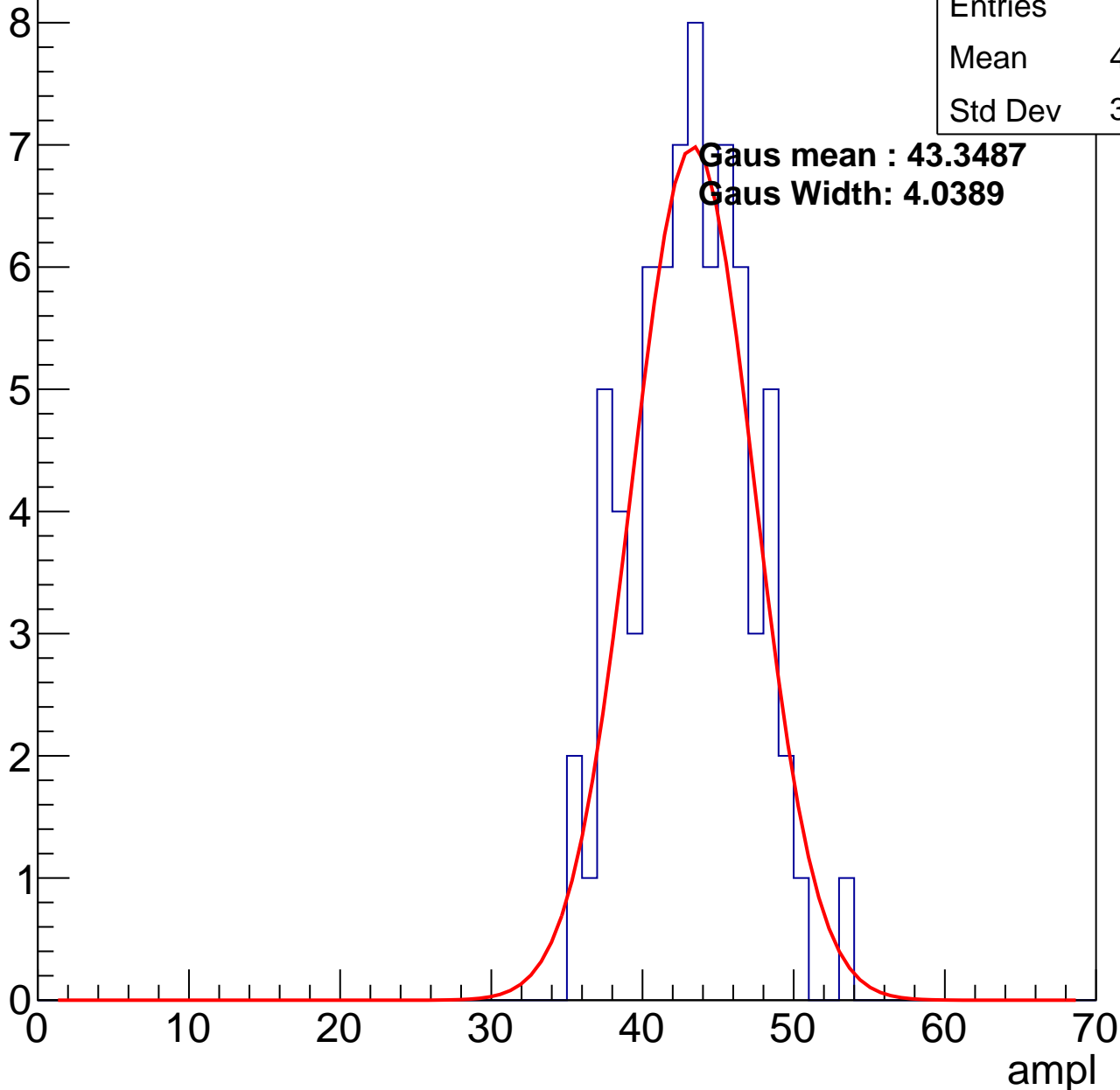
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	42.75
Std Dev	3.824

**Gaus mean : 43.3487**

**Gaus Width: 4.0389**

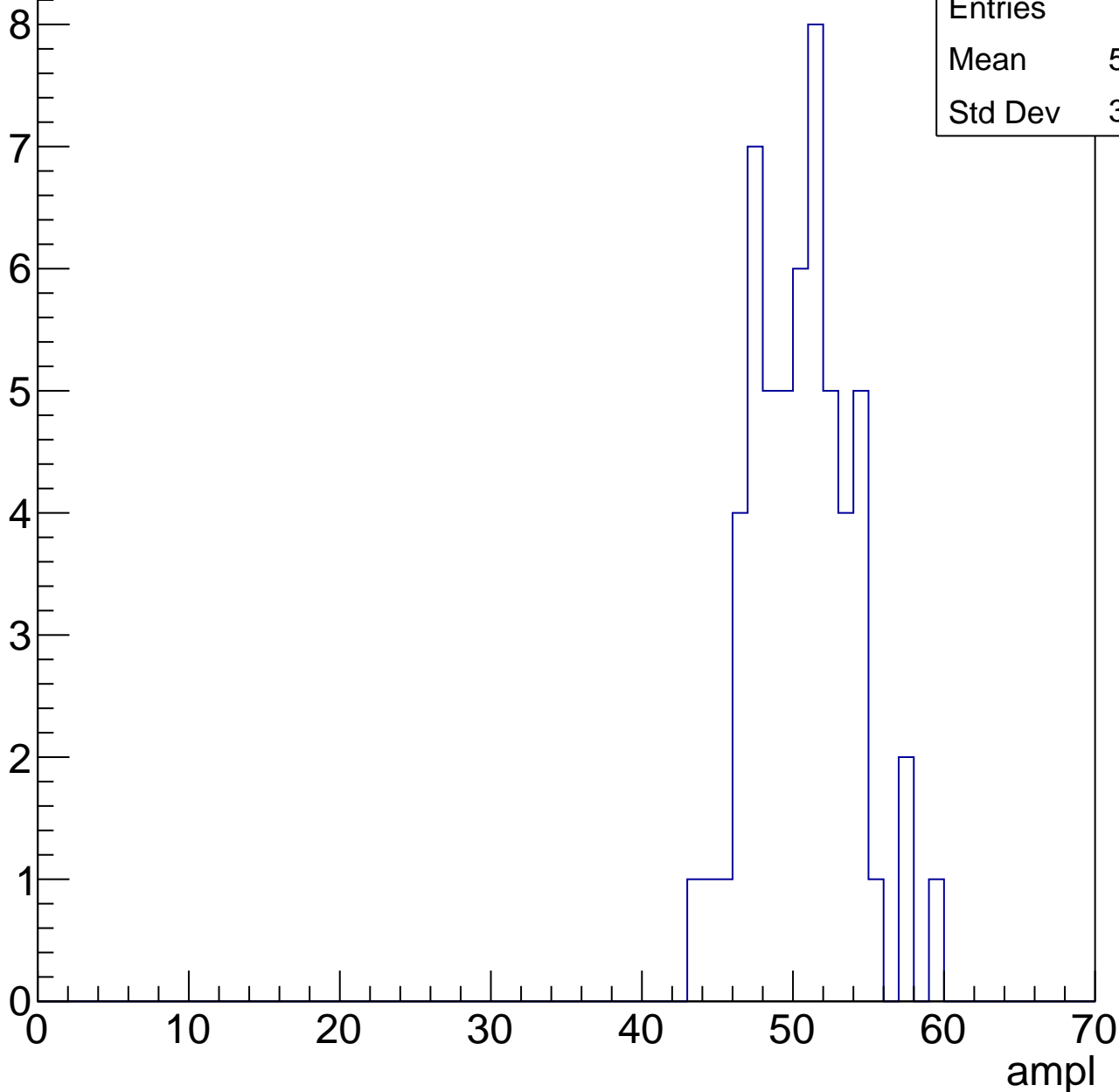


# B1L102S, U8-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

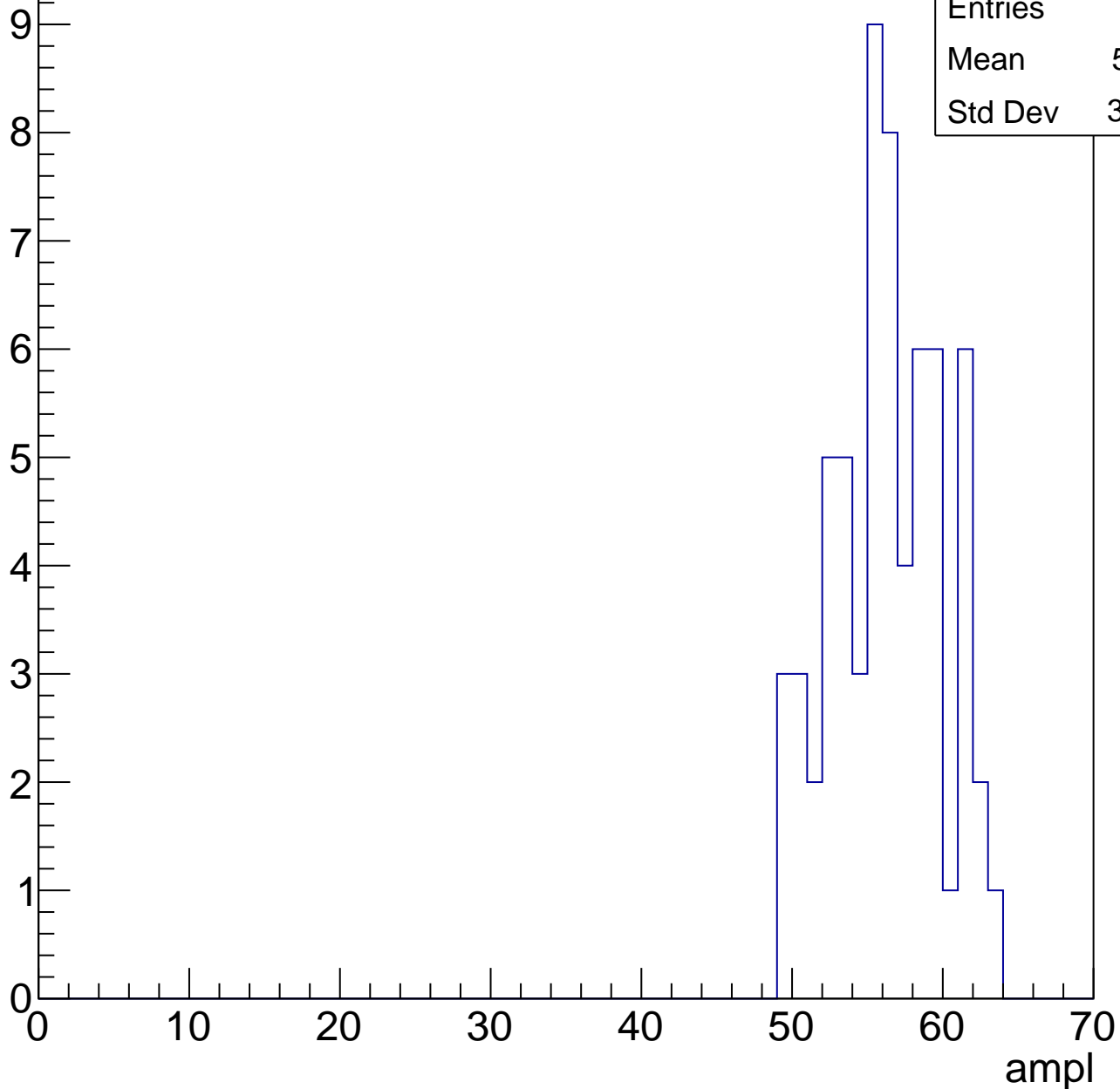
Entries	56
Mean	50.14
Std Dev	3.297



# B1L102S, U8-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



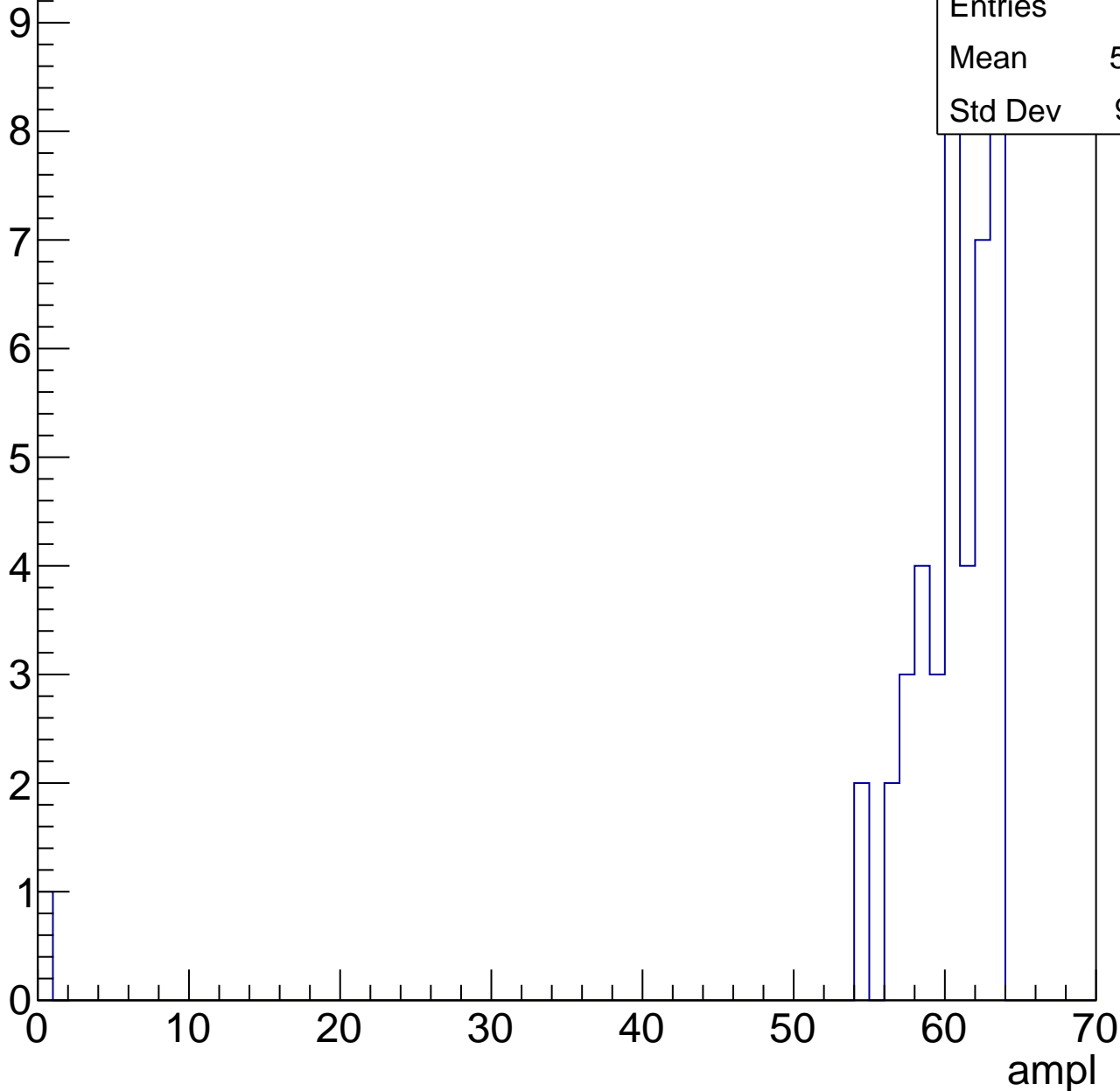
Entries	64
Mean	55.81
Std Dev	3.575

# B1L102S, U8-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	43
Mean	58.65
Std Dev	9.371



# B1L102S, U8-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

3

Mean

60.67

Std Dev

2.625



# B1L102S, U8-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch29, adc0

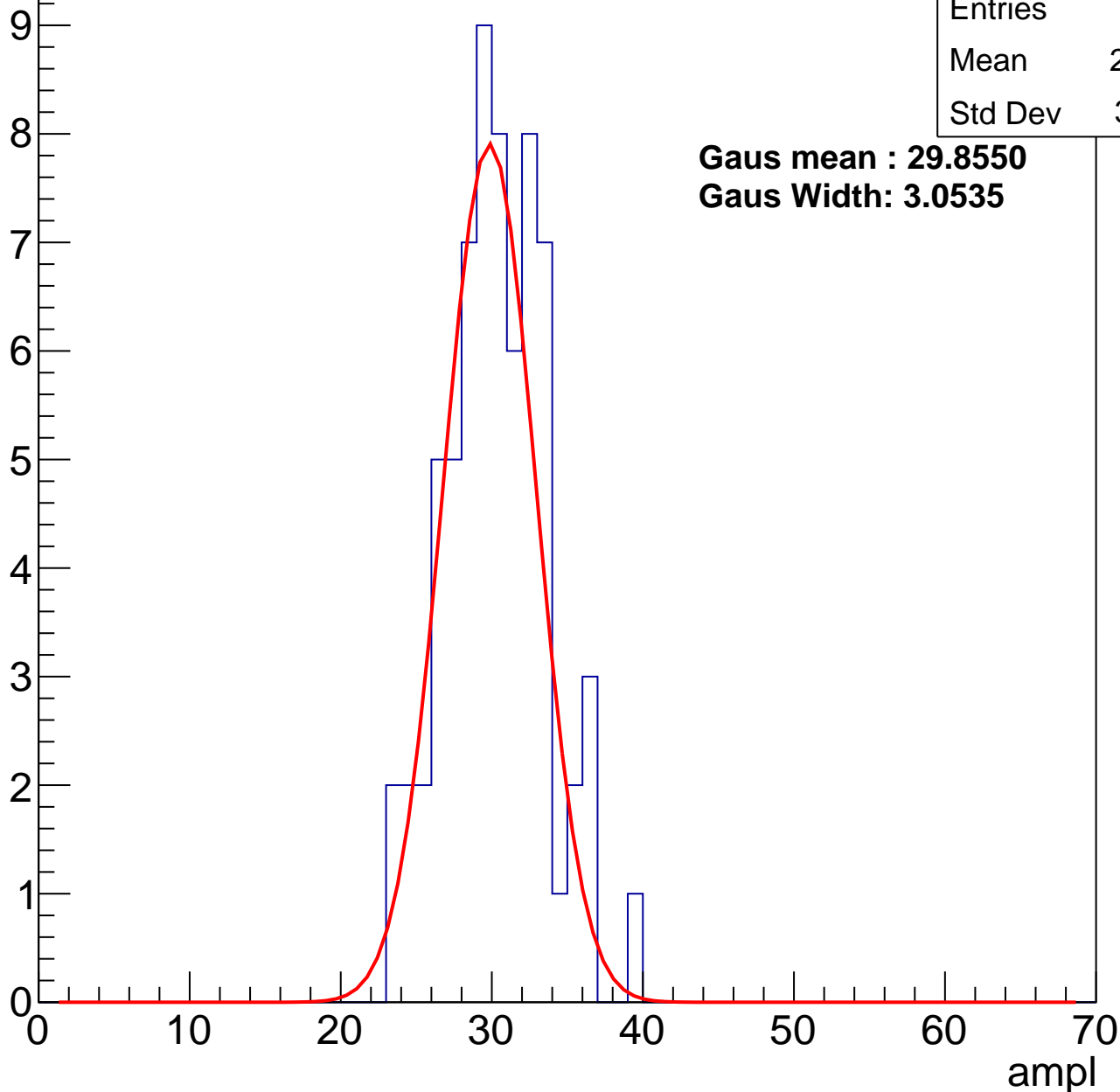
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	29.85
Std Dev	3.291

**Gaus mean : 29.8550**

**Gaus Width: 3.0535**



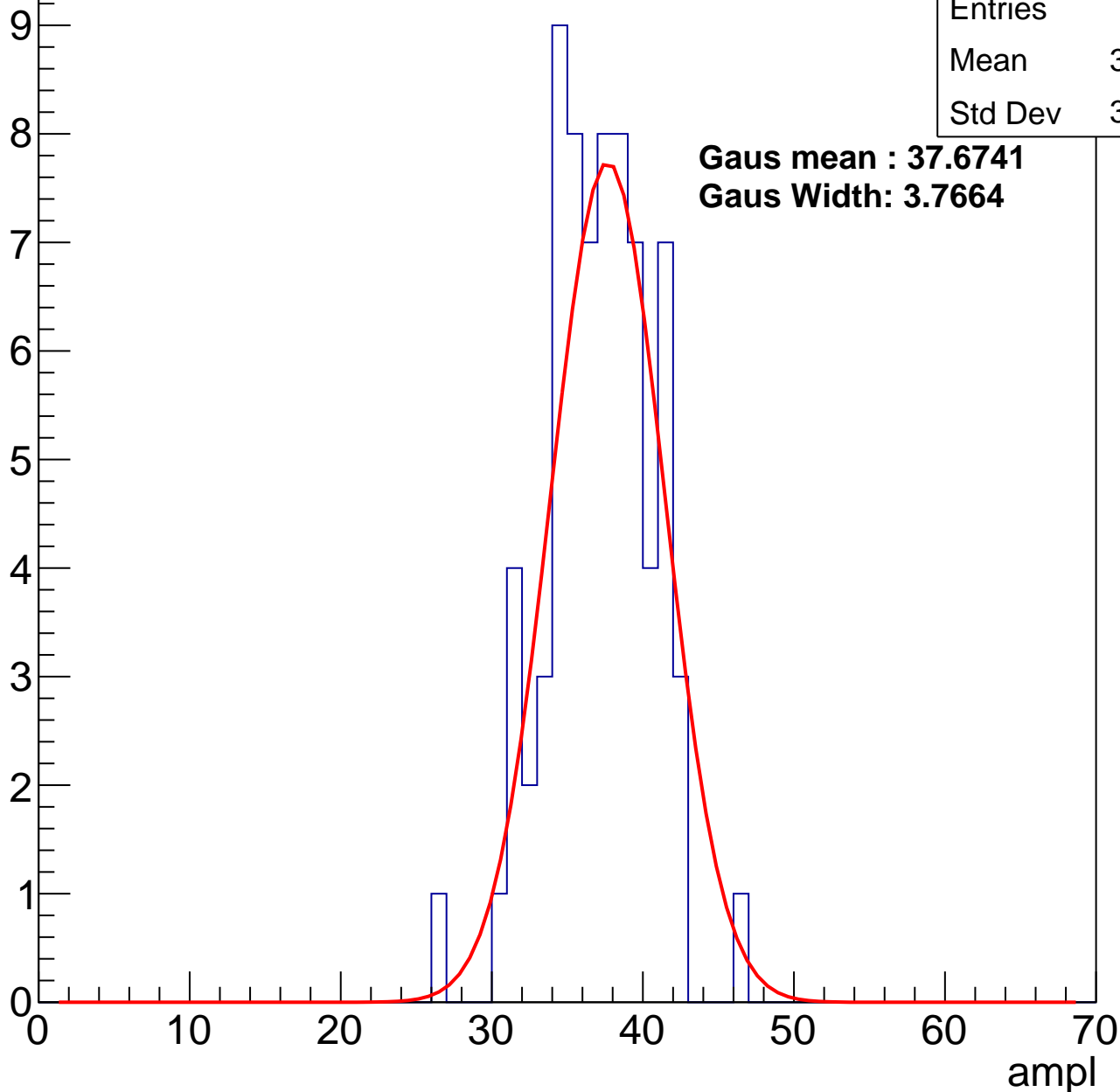
# B1L102S, U8-ch29, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	36.62
Std Dev	3.435

**Gaus mean : 37.6741**  
**Gaus Width: 3.7664**



# B1L102S, U8-ch29, adc2

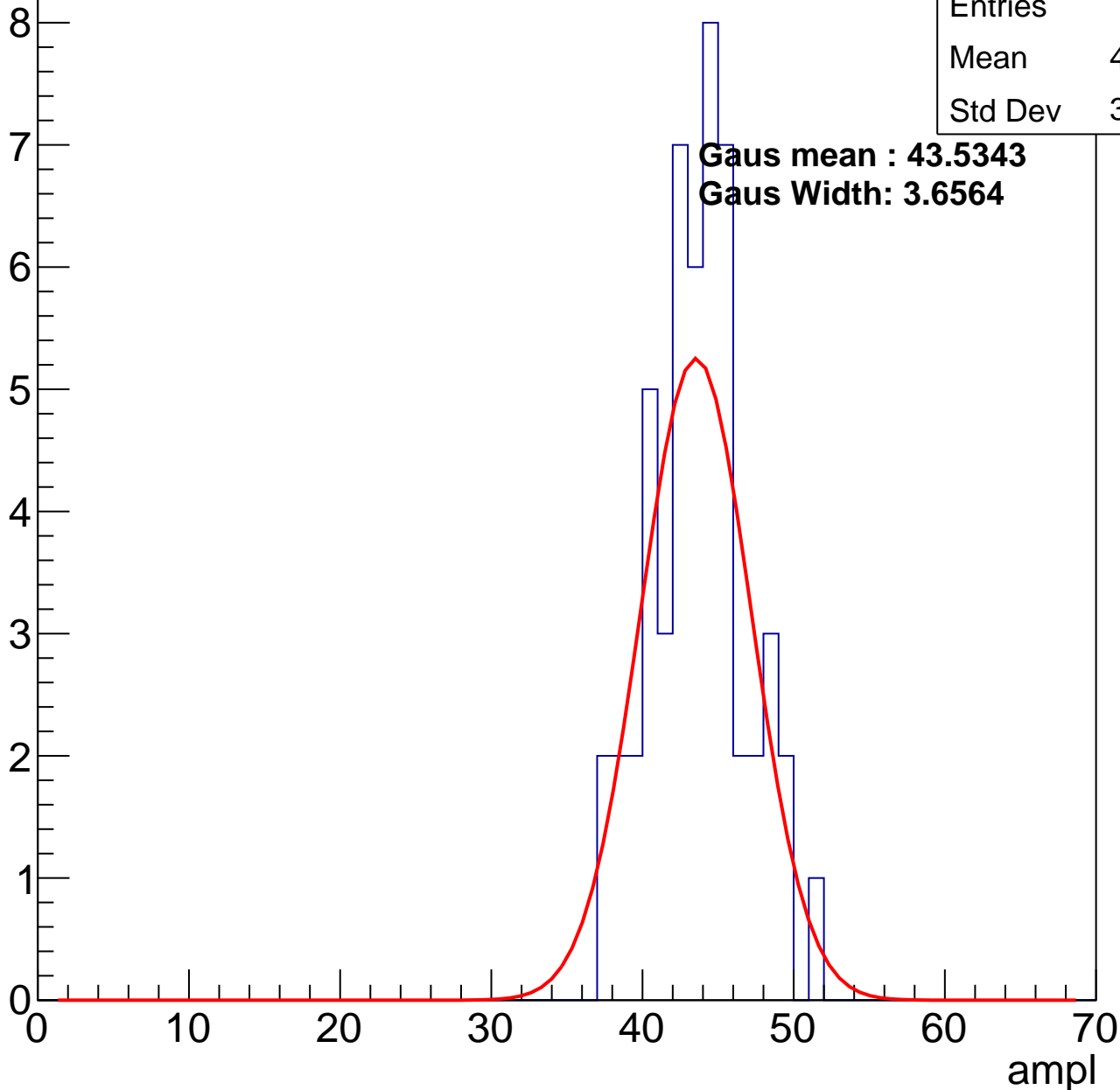
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	43.25
Std Dev	3.137

**Gaus mean : 43.5343**

**Gaus Width: 3.6564**

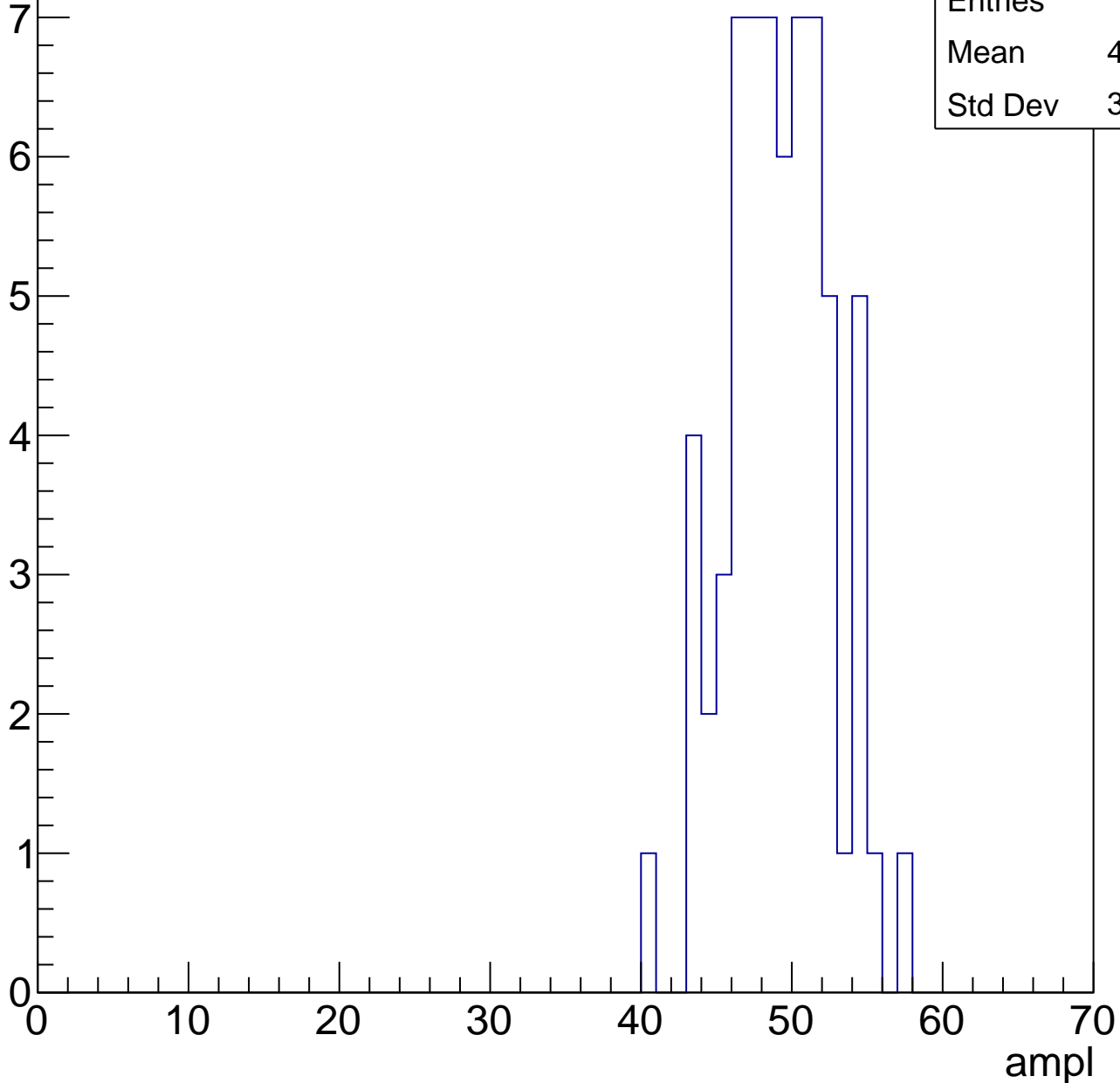


# B1L102S, U8-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	48.72
Std Dev	3.393

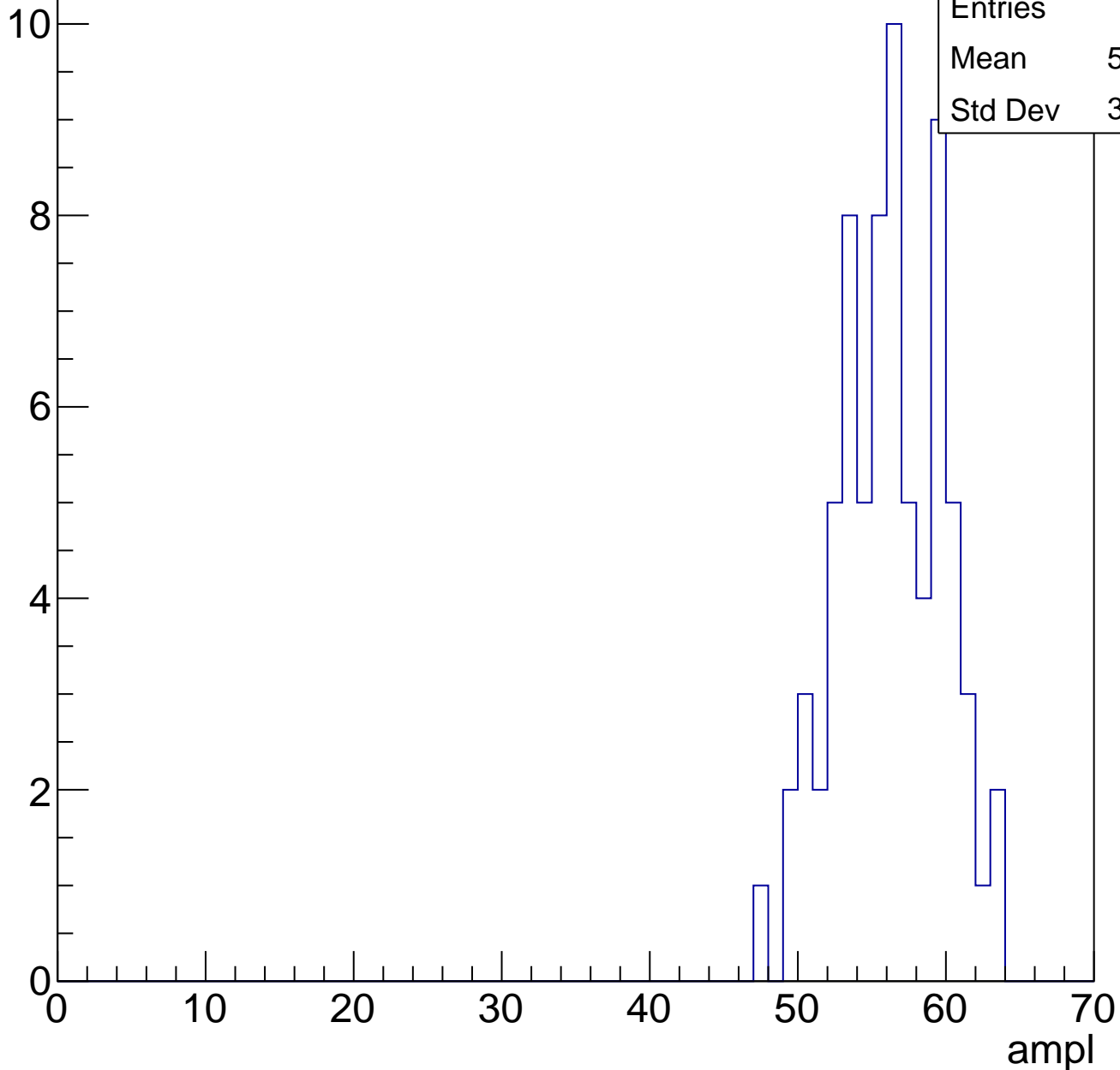


# B1L102S, U8-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	73
Mean	55.75
Std Dev	3.518

Entry

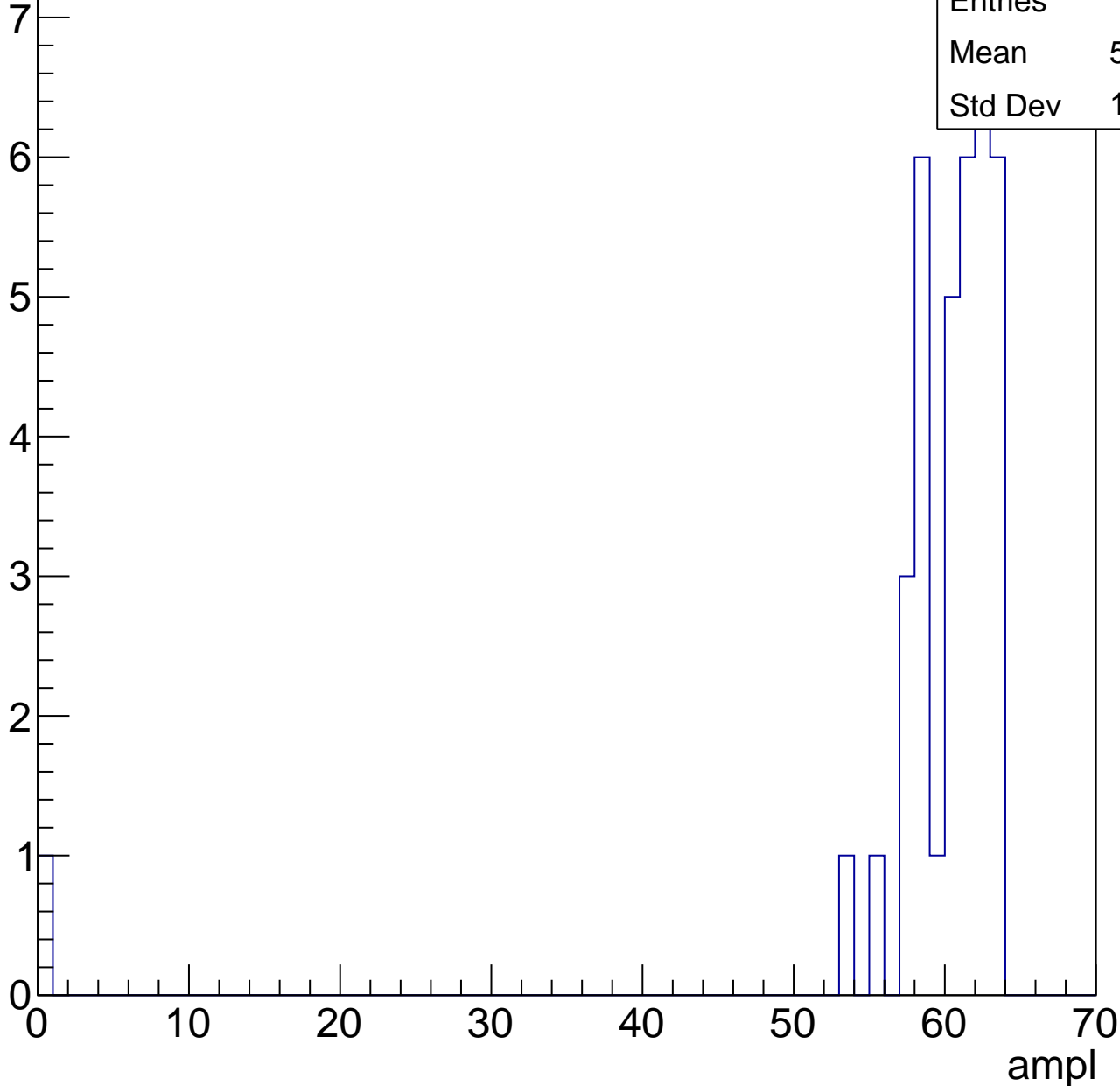


# B1L102S, U8-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	37
Mean	58.49
Std Dev	10.04



# B1L102S, U8-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

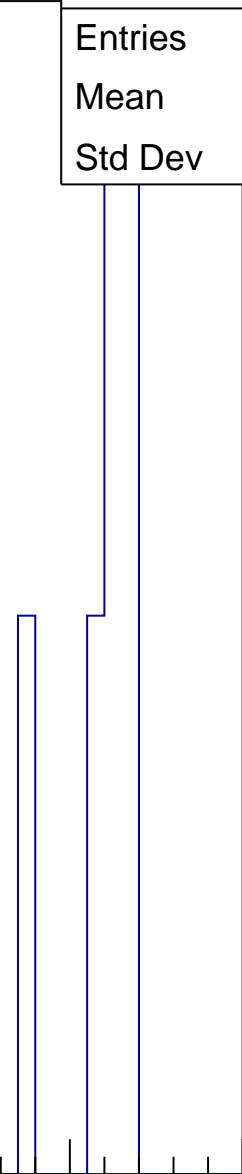
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.33
Std Dev	2.055

0 10 20 30 40 50 60 70

ampl





# B1L102S, U8-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch30, adc0

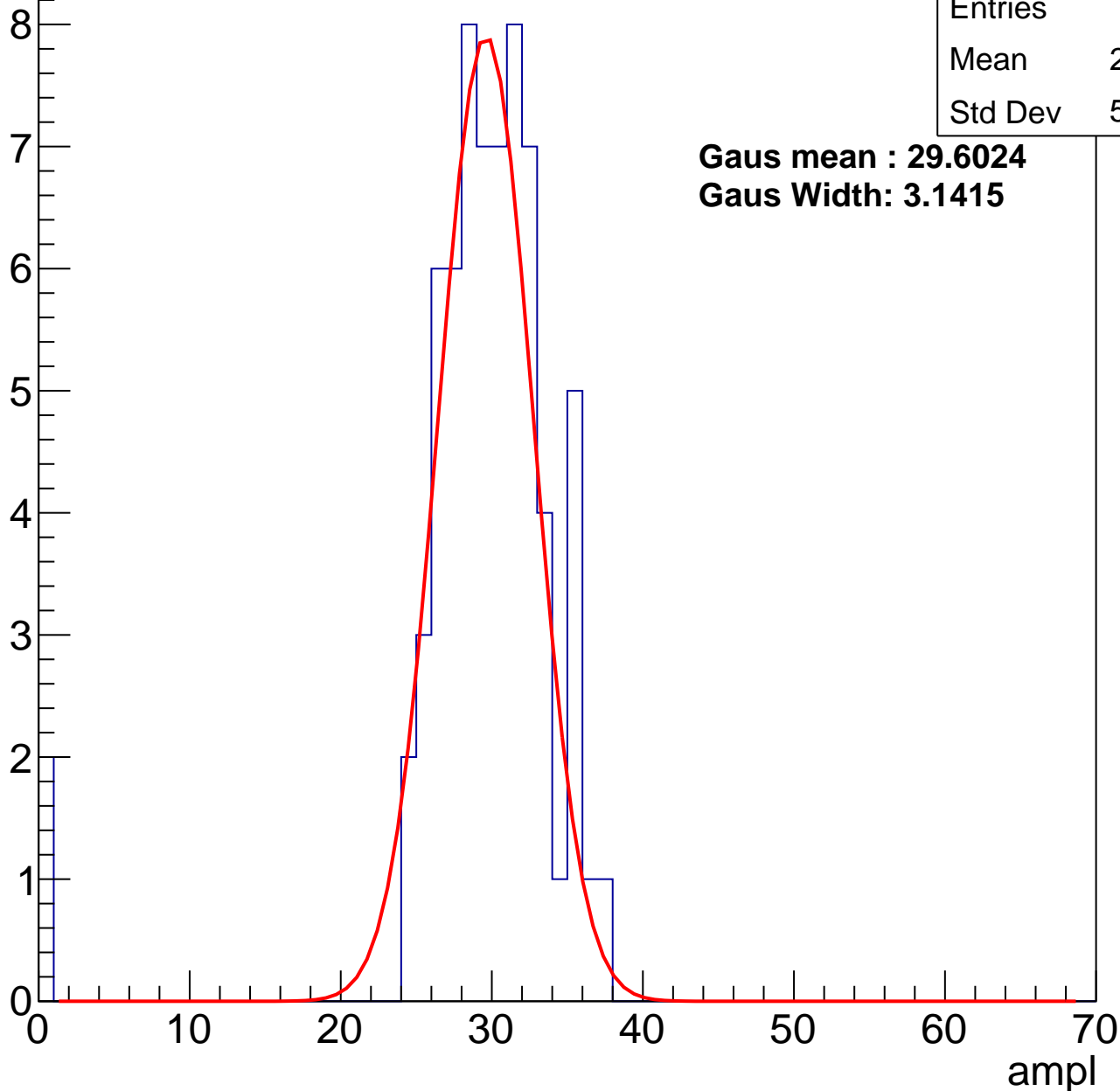
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	28.88
Std Dev	5.877

**Gaus mean : 29.6024**

**Gaus Width: 3.1415**



# B1L102S, U8-ch30, adc1

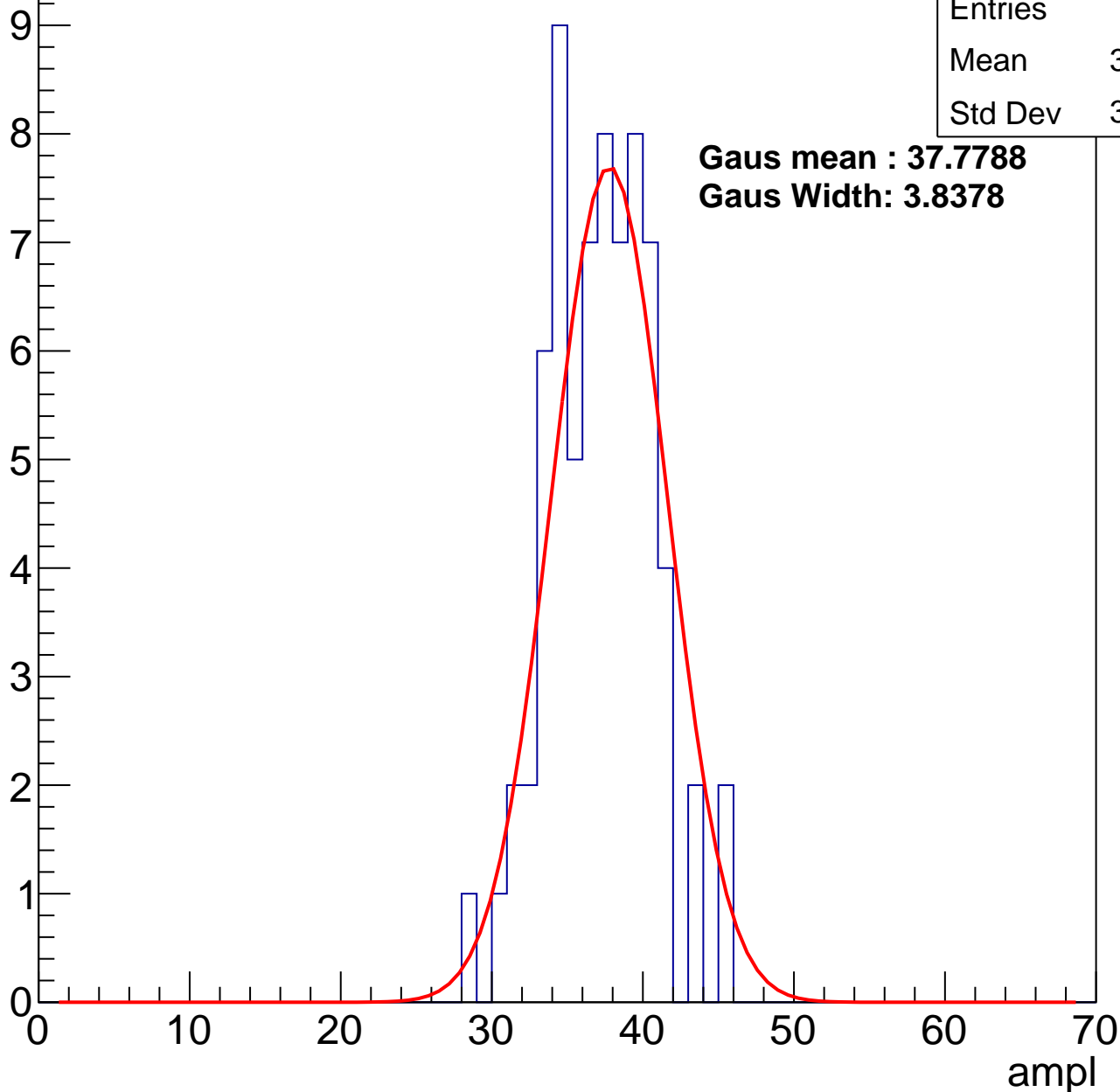
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	36.75
Std Dev	3.393

**Gaus mean : 37.7788**

**Gaus Width: 3.8378**



# B1L102S, U8-ch30, adc2

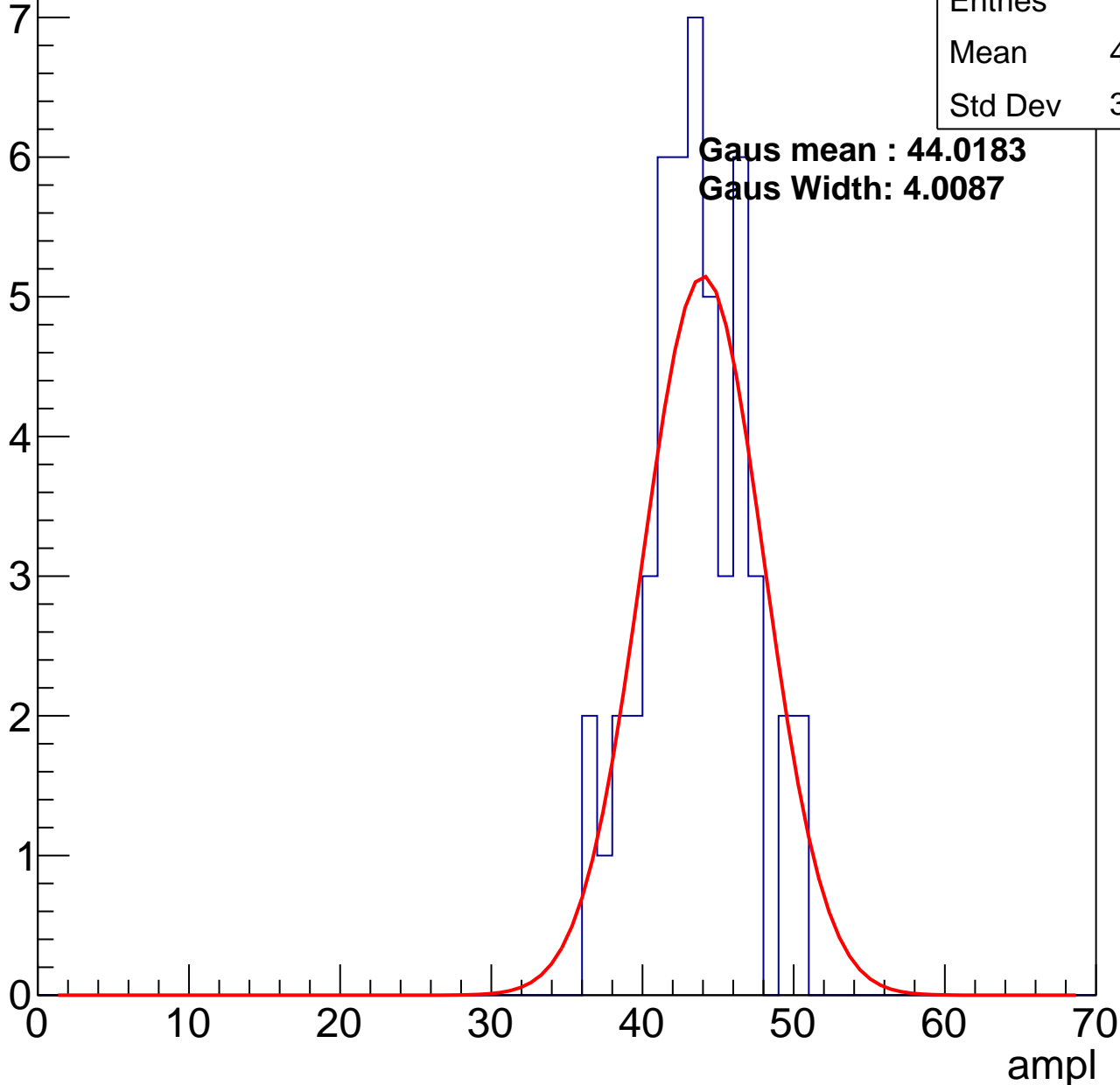
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	43.04
Std Dev	3.352

**Gaus mean : 44.0183**

**Gaus Width: 4.0087**

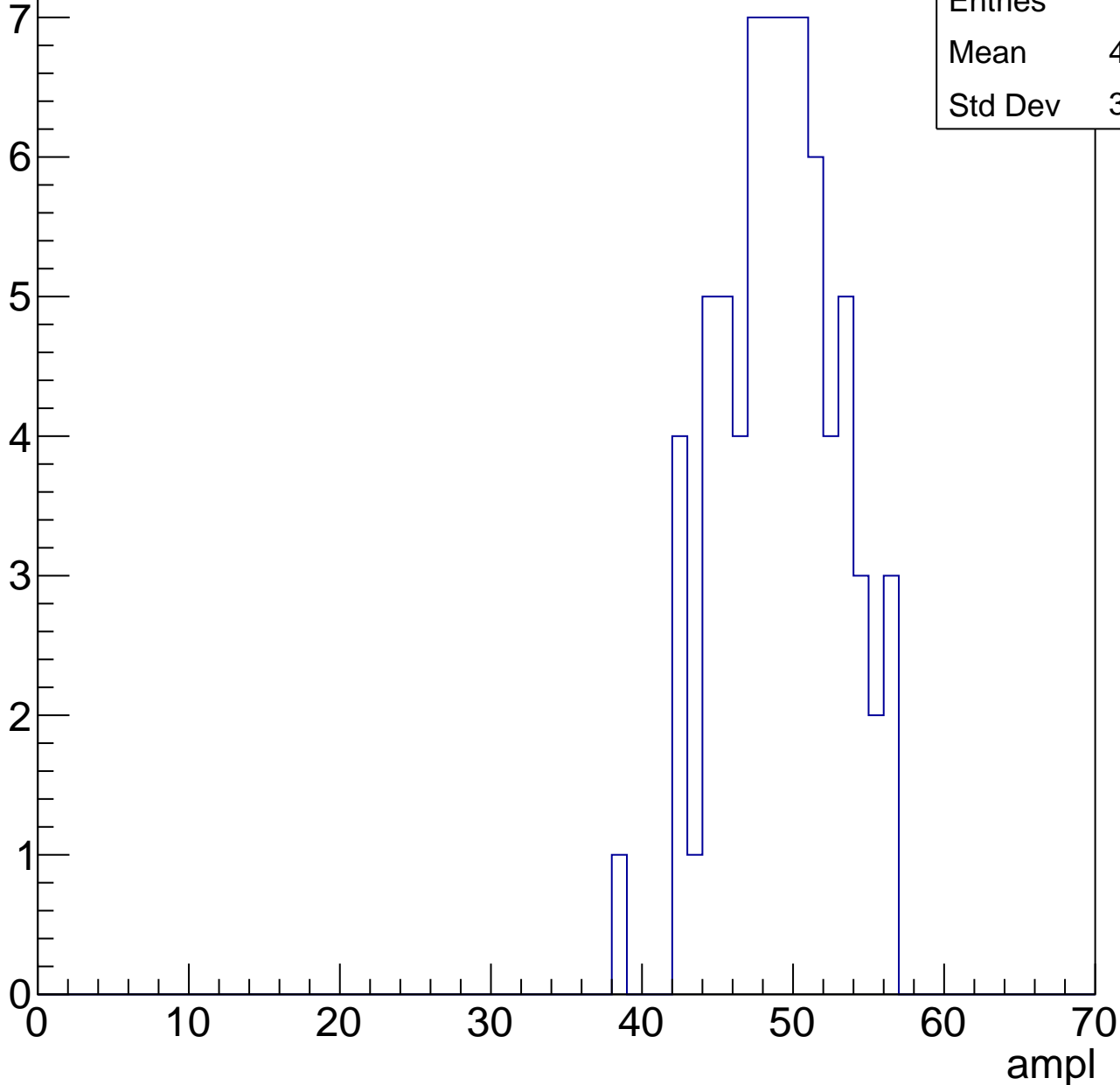


# B1L102S, U8-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

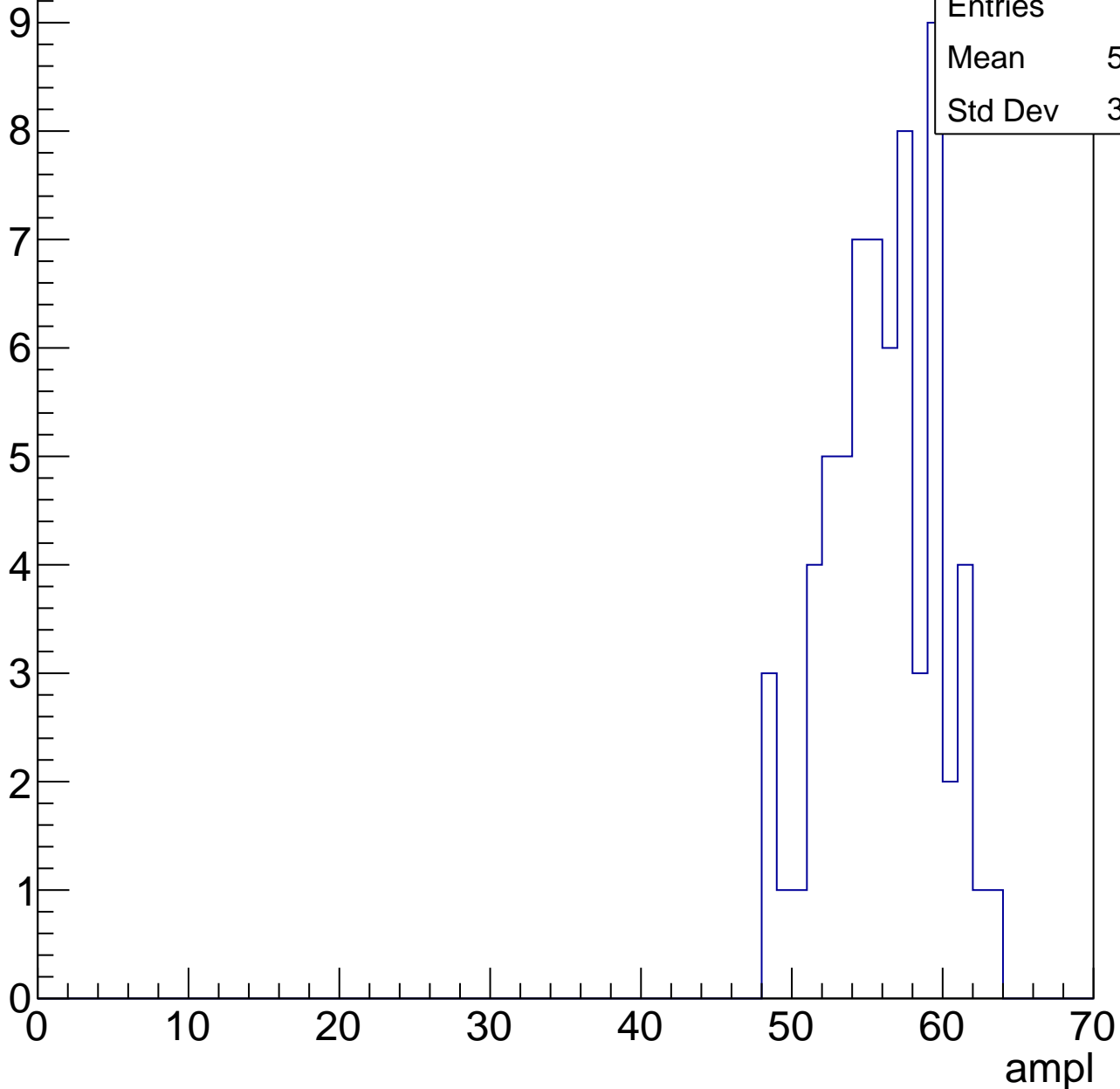
Entries	71
Mean	48.66
Std Dev	3.867



# B1L102S, U8-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

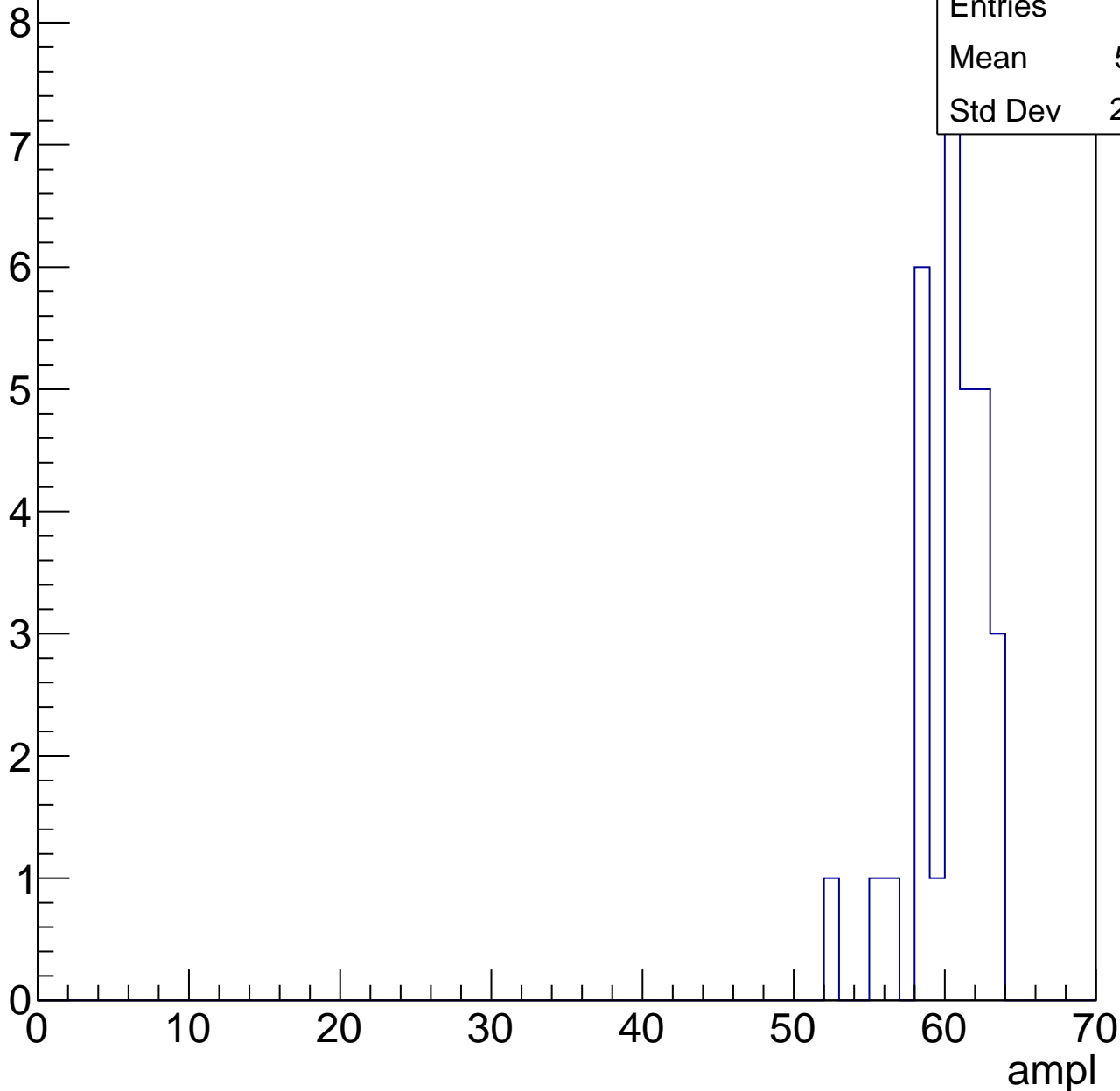


# B1L102S, U8-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	31
Mean	59.81
Std Dev	2.415

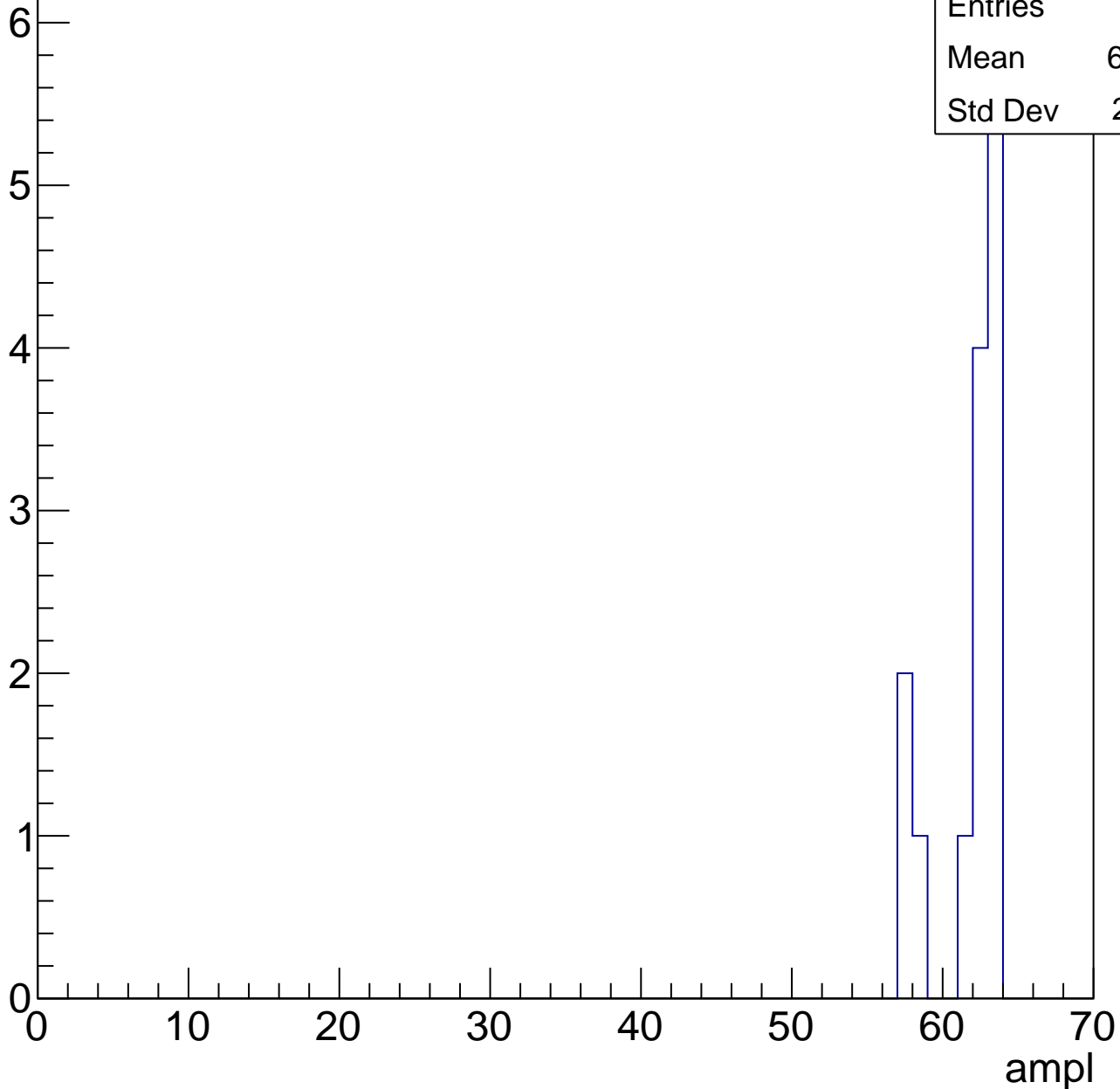


# B1L102S, U8-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	14
Mean	61.36
Std Dev	2.191





# B1L102S, U8-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch31, adc0

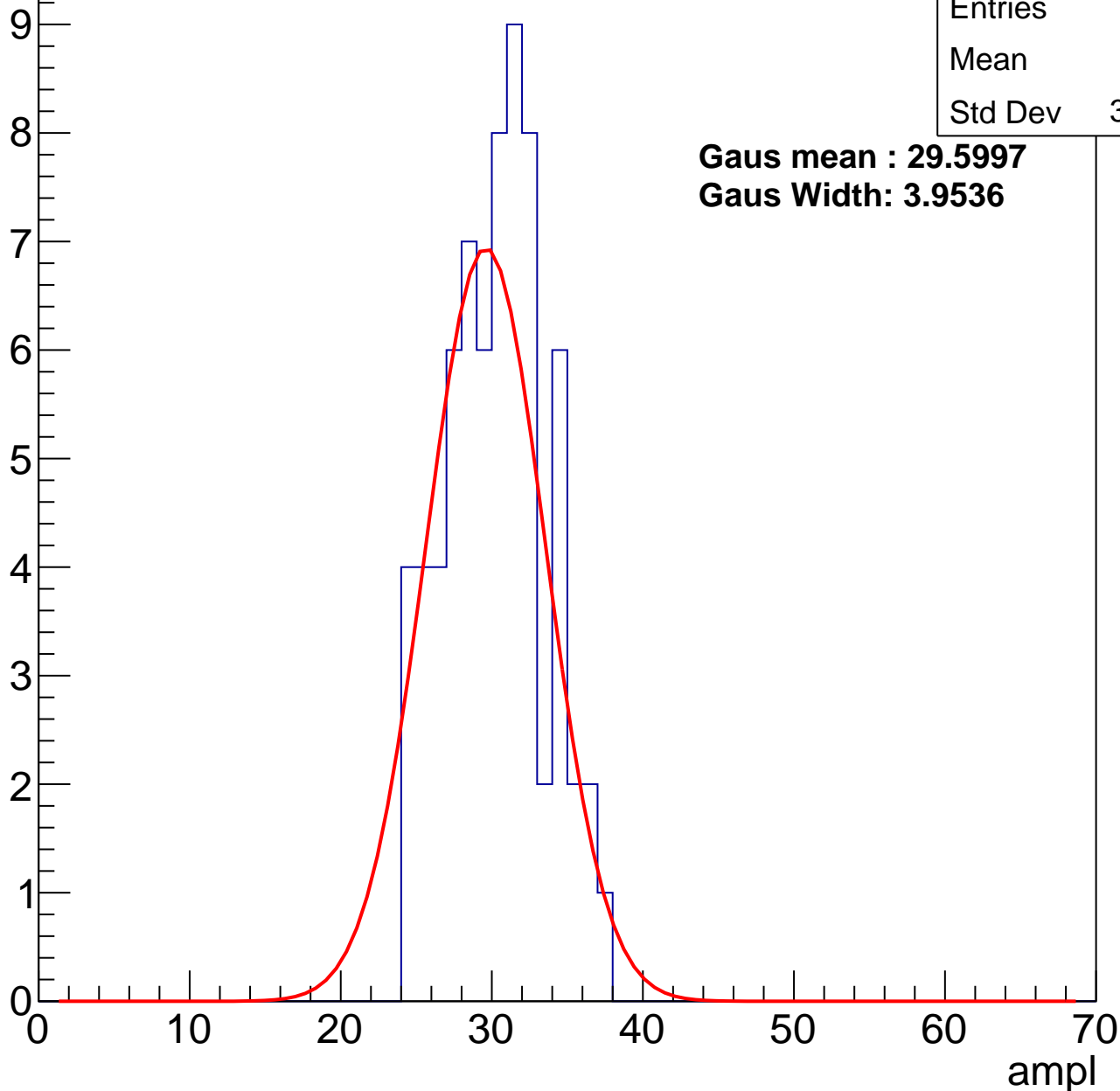
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	29.8
Std Dev	3.228

**Gaus mean : 29.5997**

**Gaus Width: 3.9536**



# B1L102S, U8-ch31, adc1

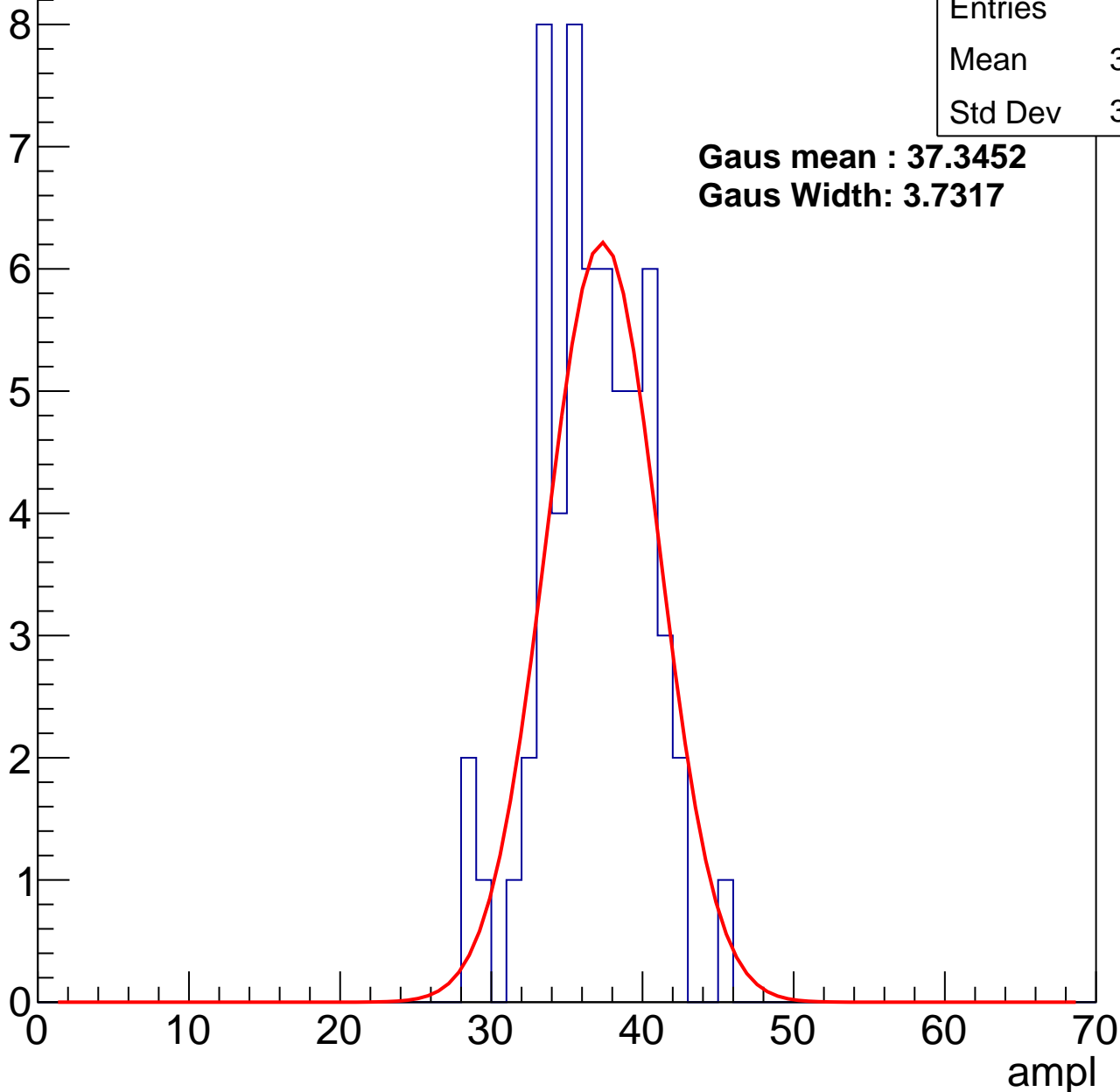
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	36.25
Std Dev	3.467

**Gaus mean : 37.3452**

**Gaus Width: 3.7317**



# B1L102S, U8-ch31, adc2

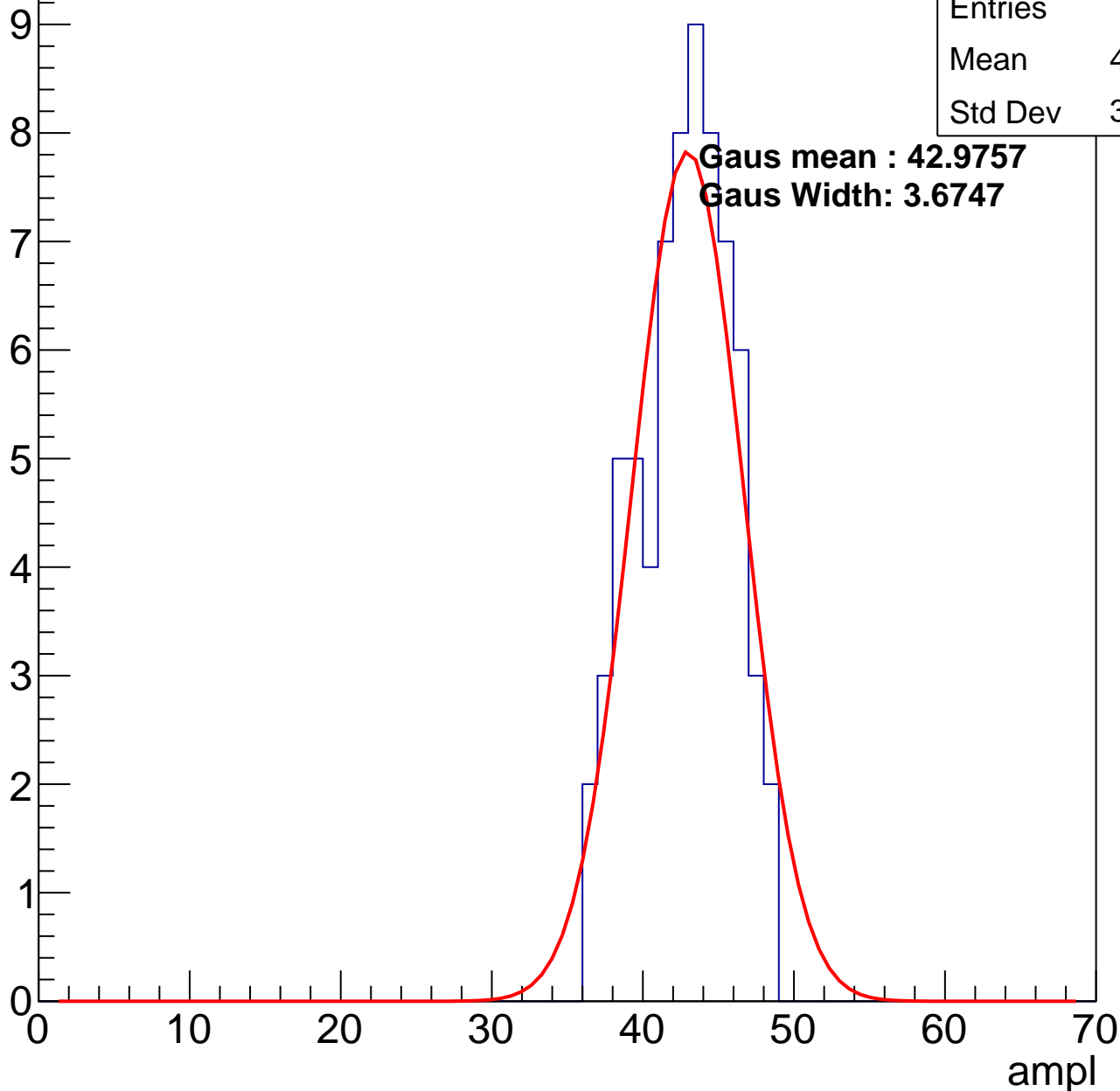
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	42.29
Std Dev	3.036

**Gaus mean : 42.9757**

**Gaus Width: 3.6747**

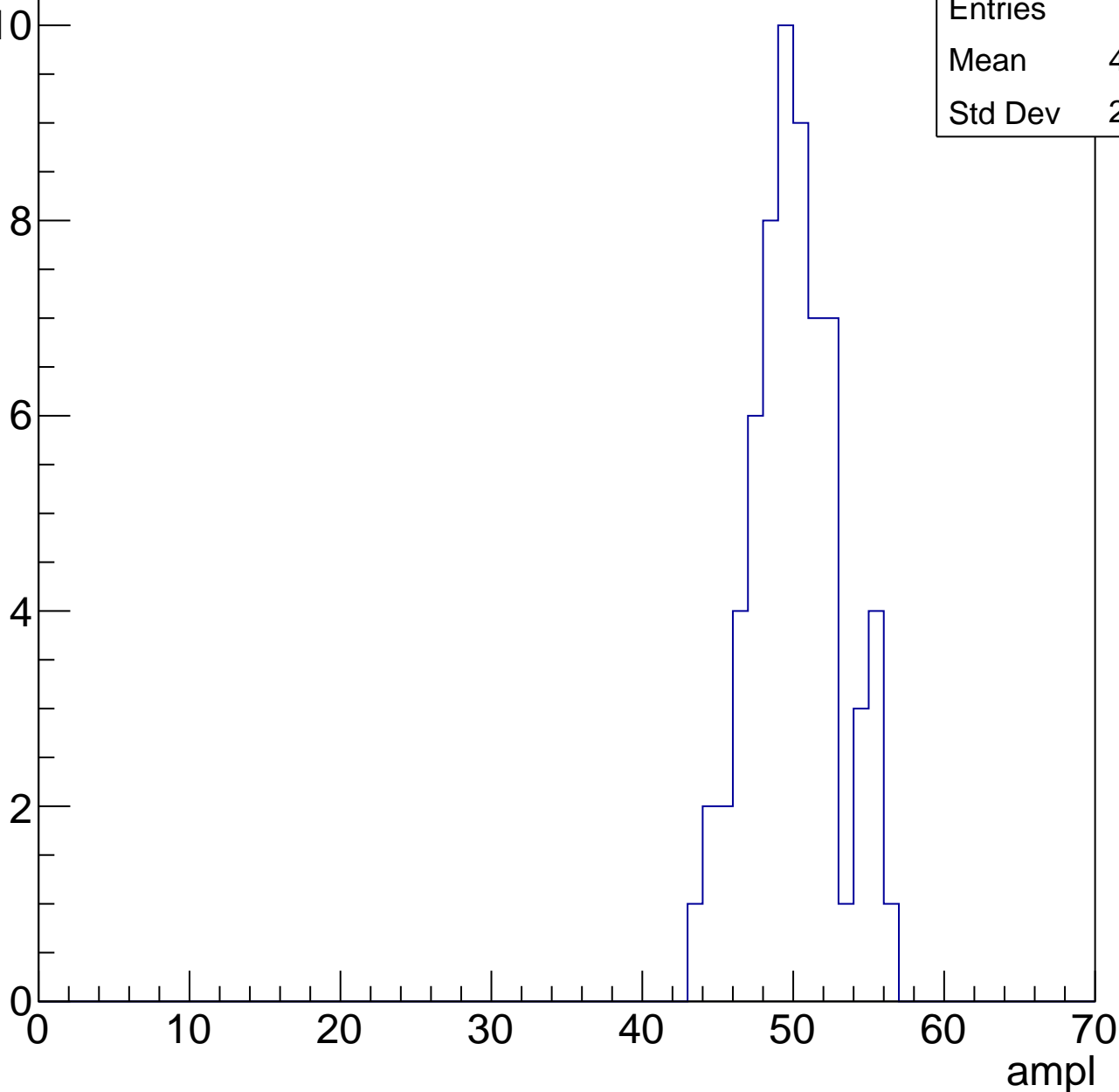


# B1L102S, U8-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	49.58
Std Dev	2.903

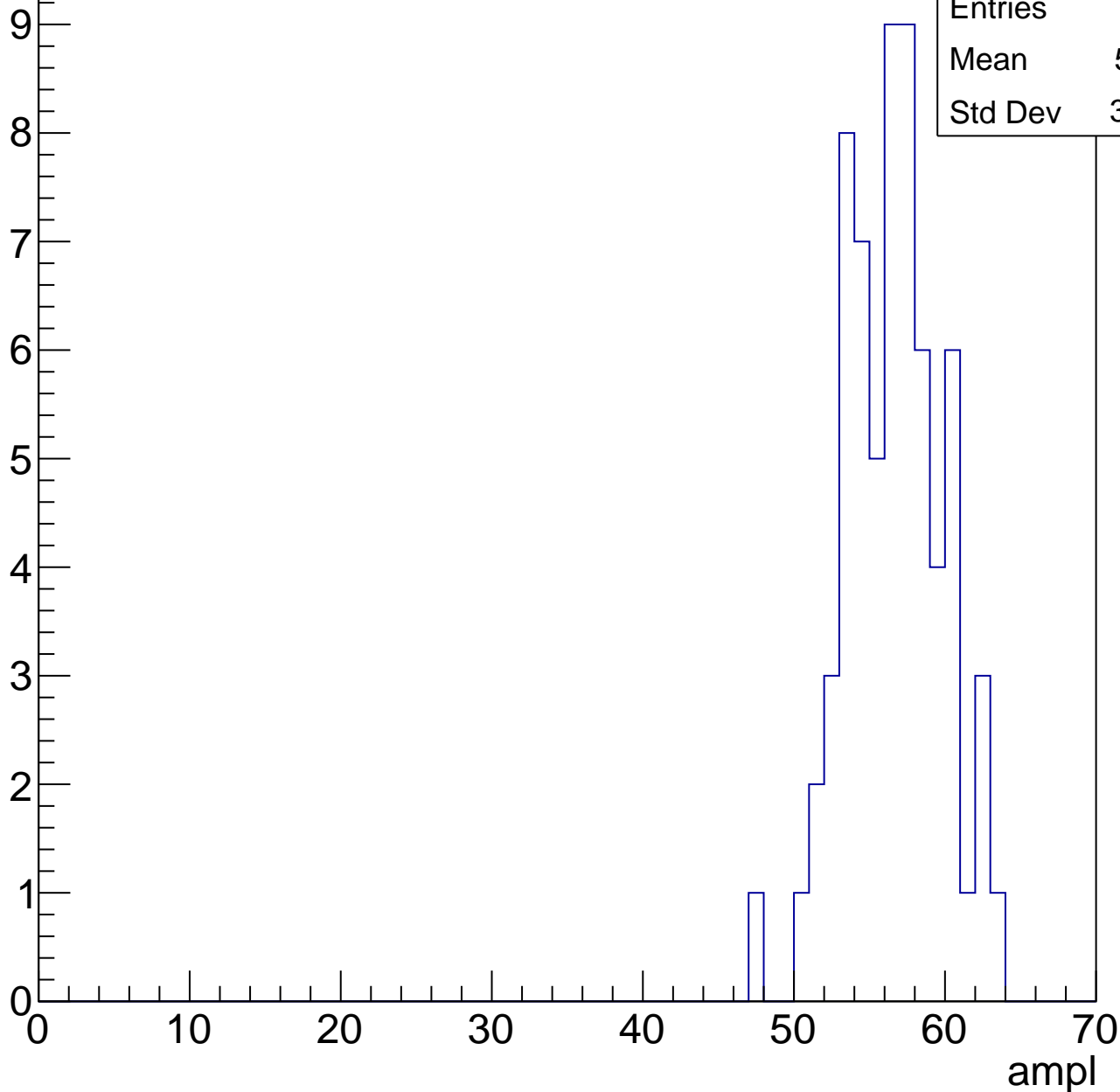


# B1L102S, U8-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	56.11
Std Dev	3.177

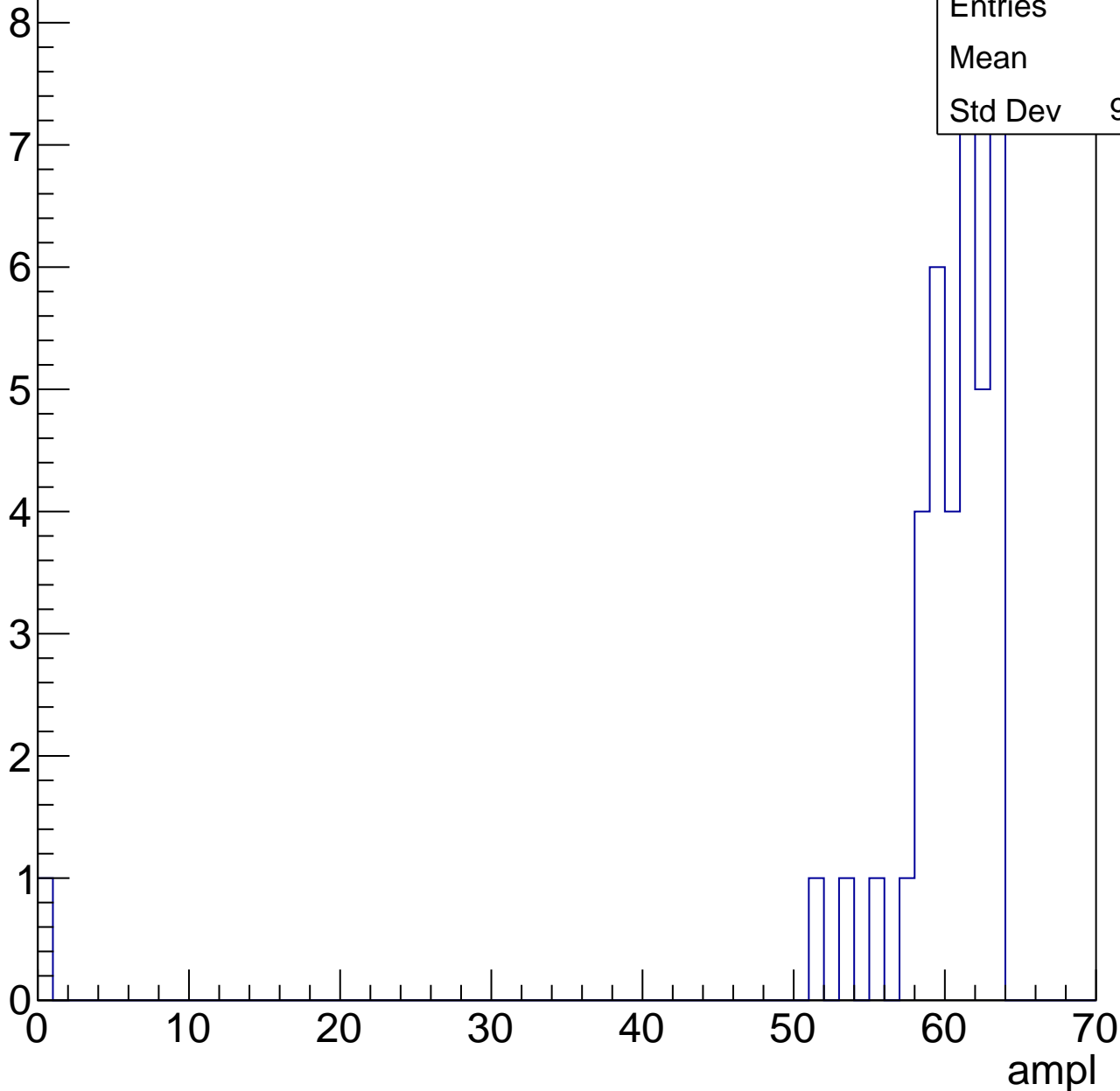


# B1L102S, U8-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	58.6
Std Dev	9.757



# B1L102S, U8-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

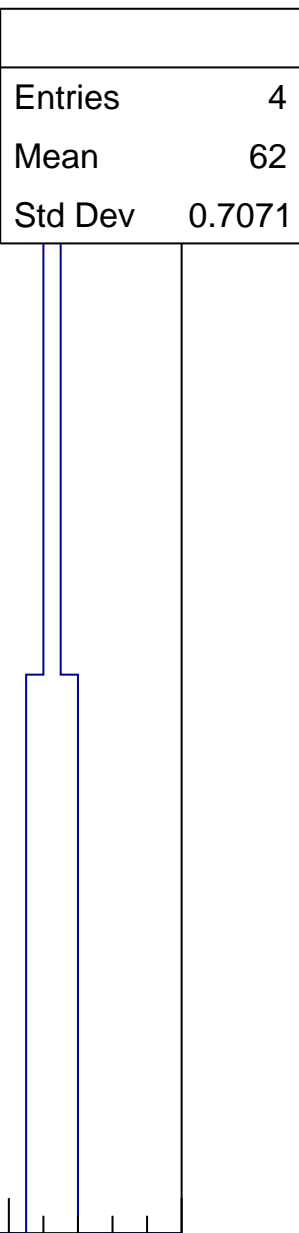
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	62
Std Dev	0.7071

0 10 20 30 40 50 60 70

ampl





# B1L102S, U8-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	22
Std Dev	0

# B1L102S, U8-ch32, adc0

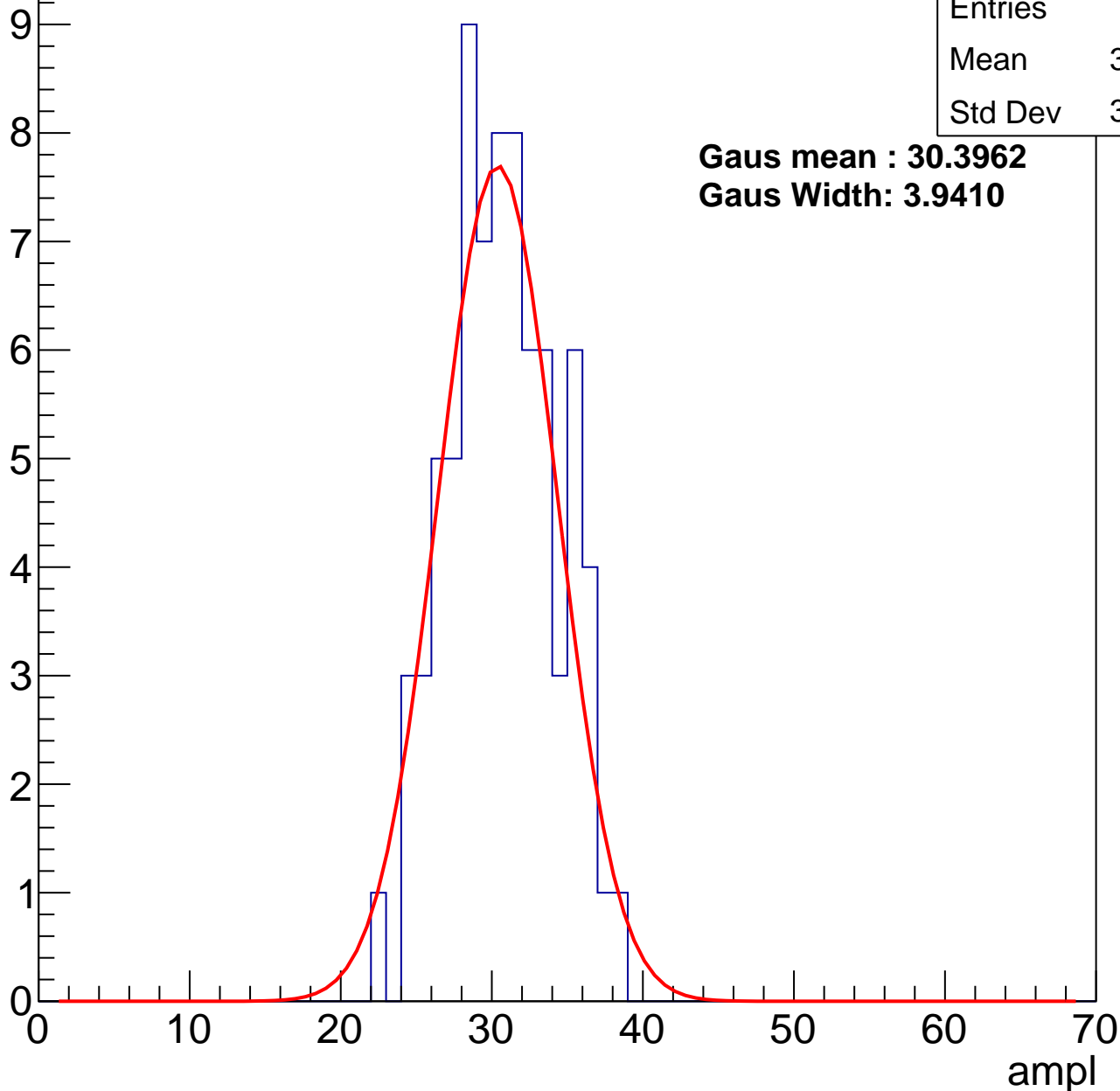
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	30.24
Std Dev	3.539

**Gaus mean : 30.3962**

**Gaus Width: 3.9410**



# B1L102S, U8-ch32, adc1

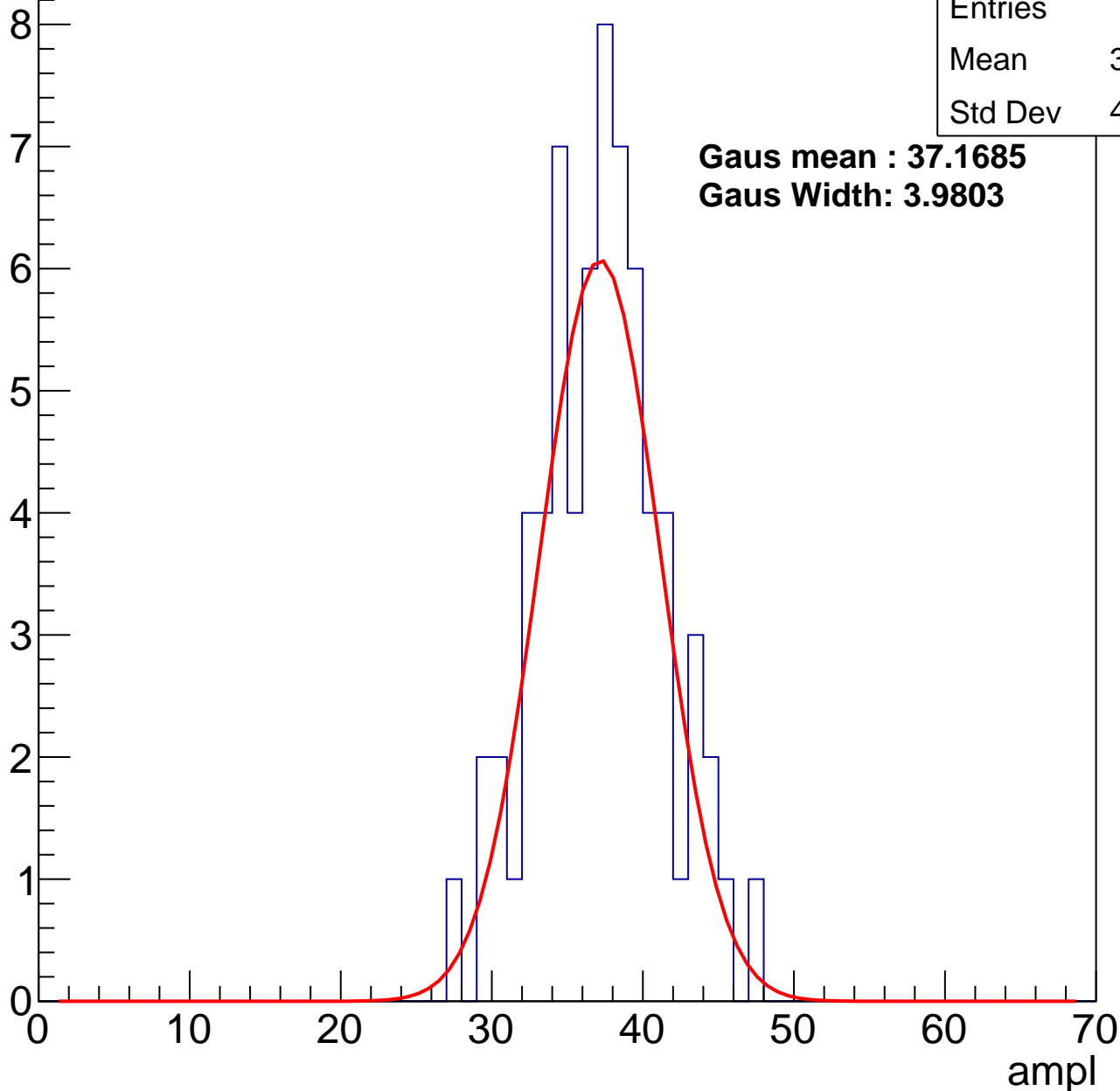
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	36.78
Std Dev	4.083

**Gaus mean : 37.1685**

**Gaus Width: 3.9803**



# B1L102S, U8-ch32, adc2

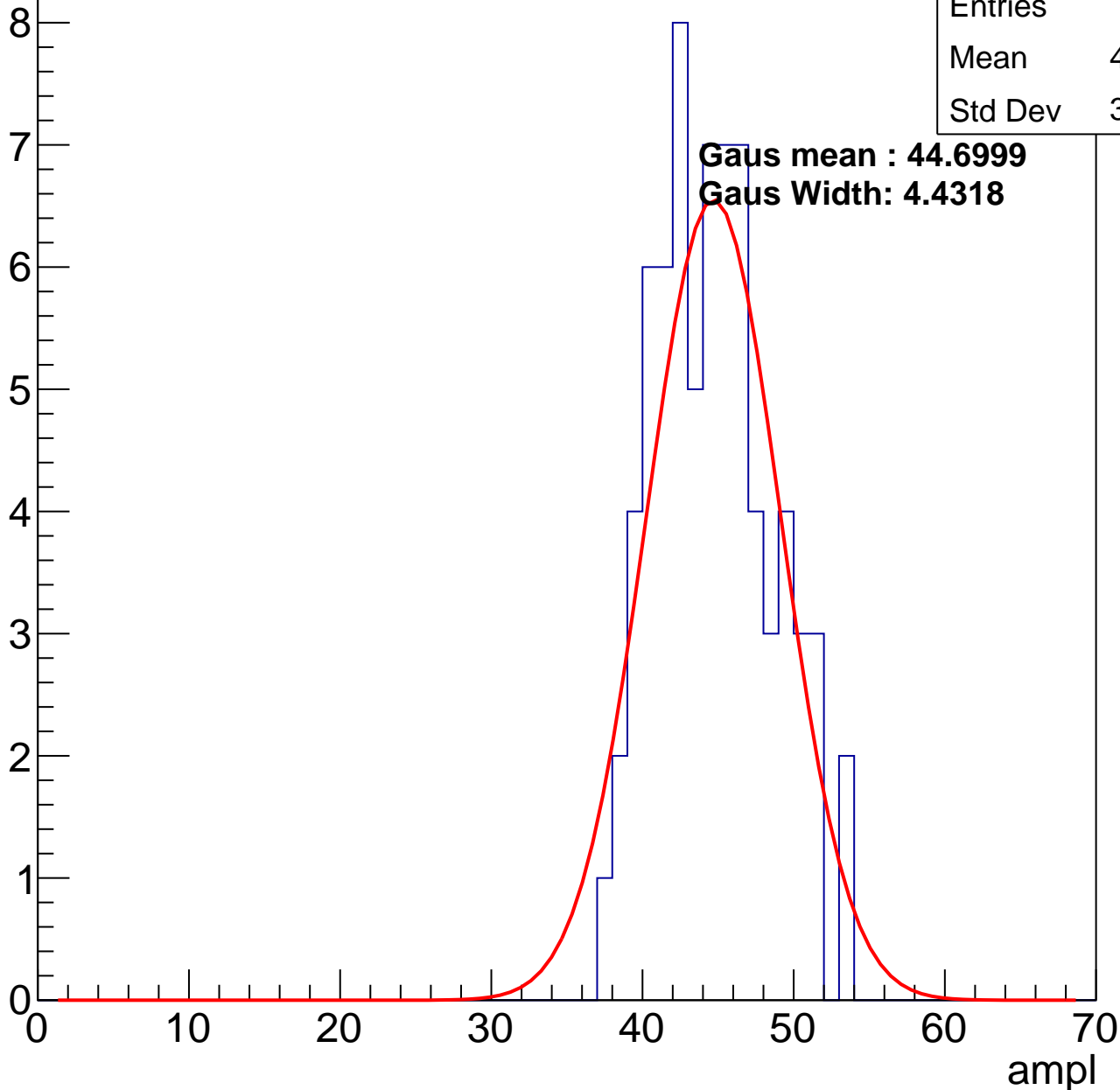
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	44.28
Std Dev	3.798

**Gaus mean : 44.6999**

**Gaus Width: 4.4318**

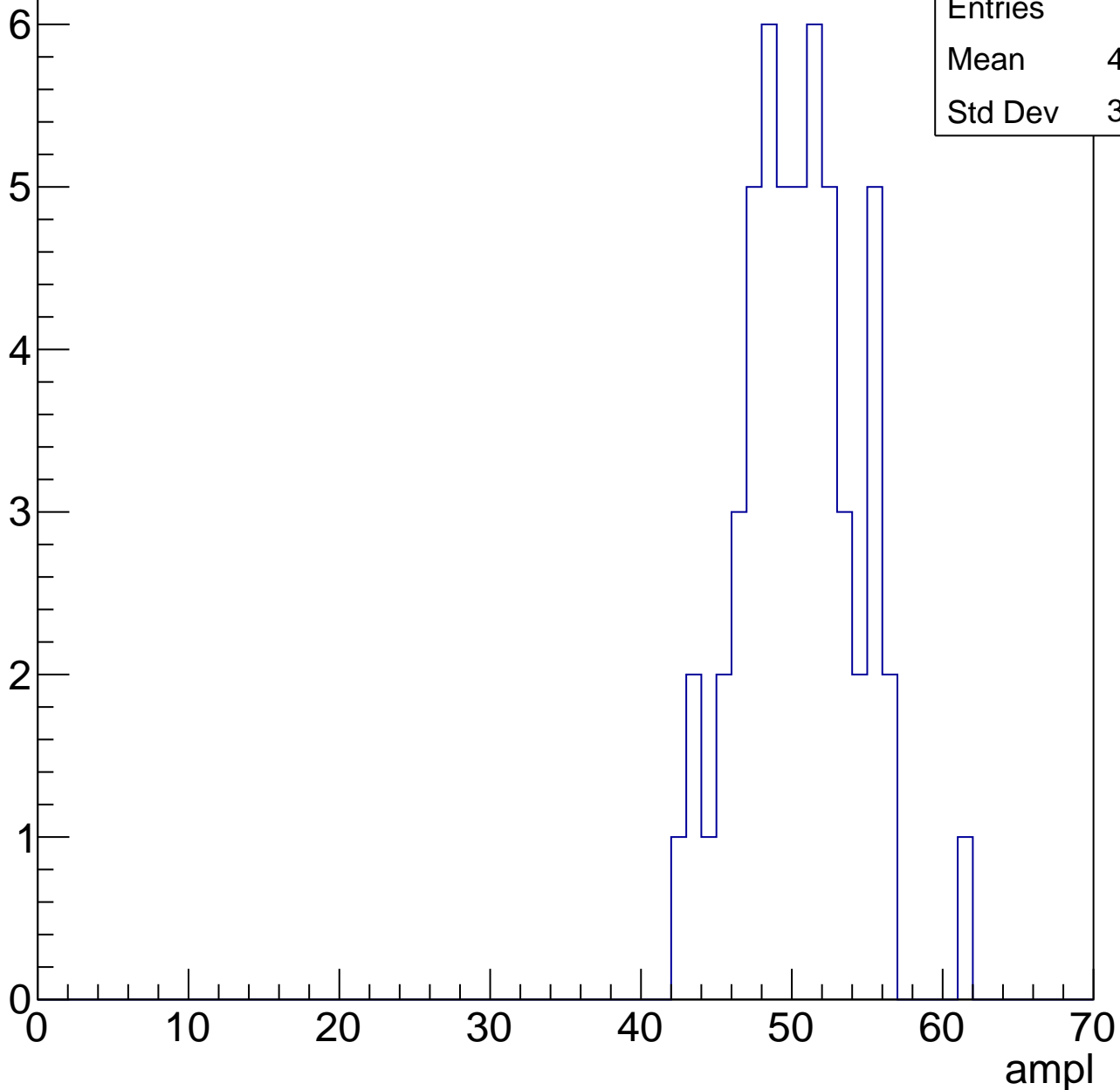


# B1L102S, U8-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	49.98
Std Dev	3.783

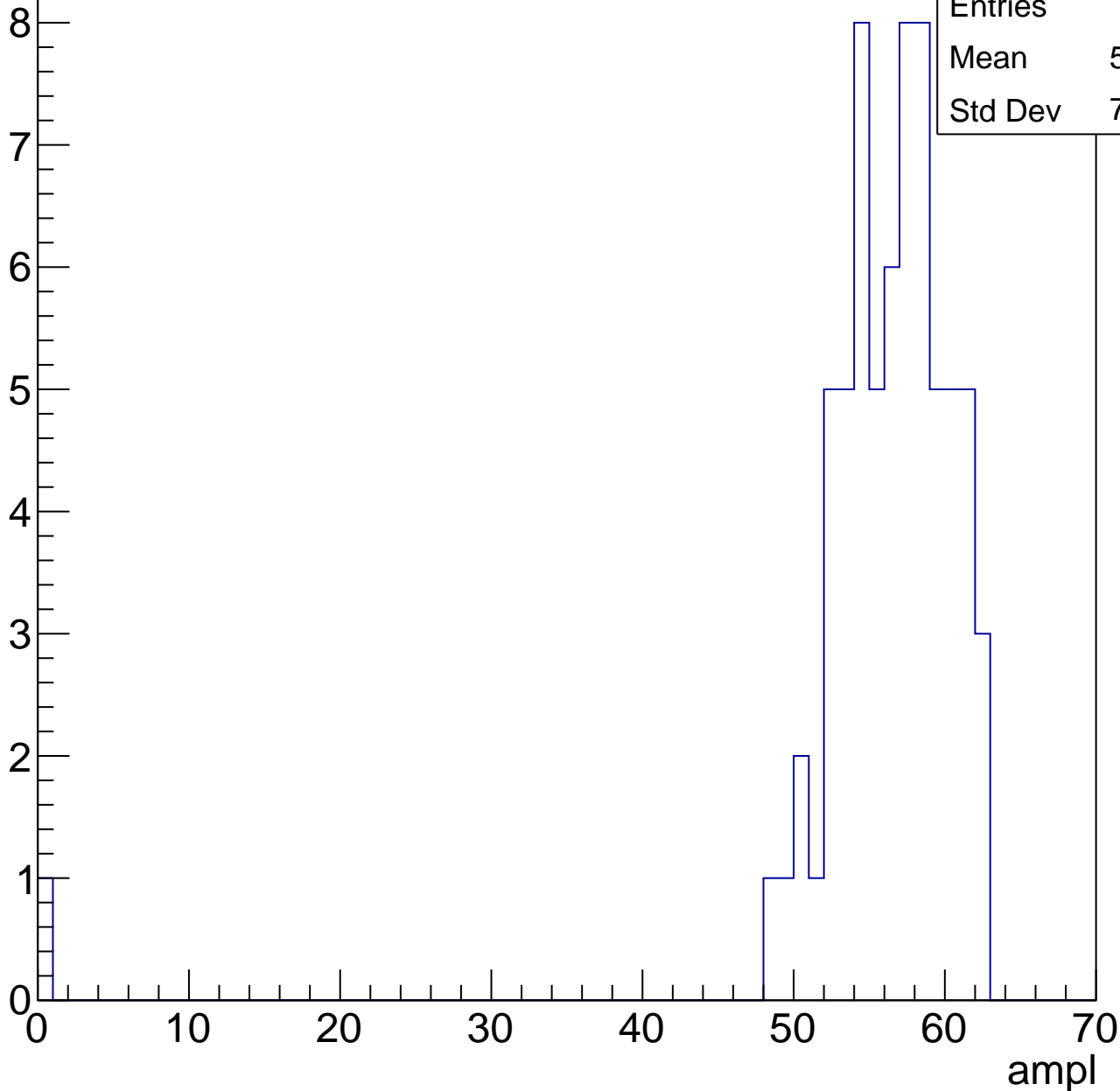


# B1L102S, U8-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	55.39
Std Dev	7.499

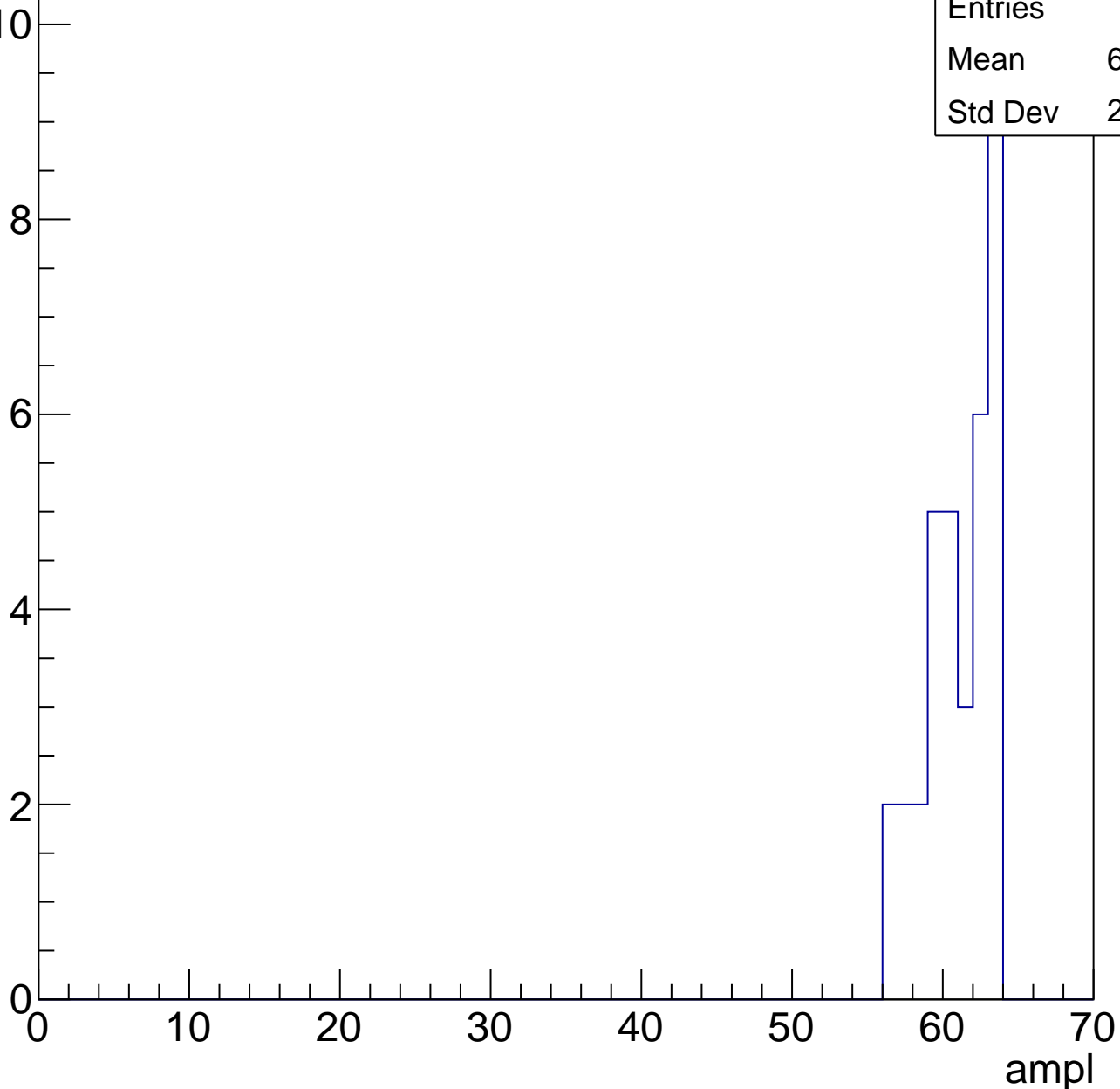


# B1L102S, U8-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

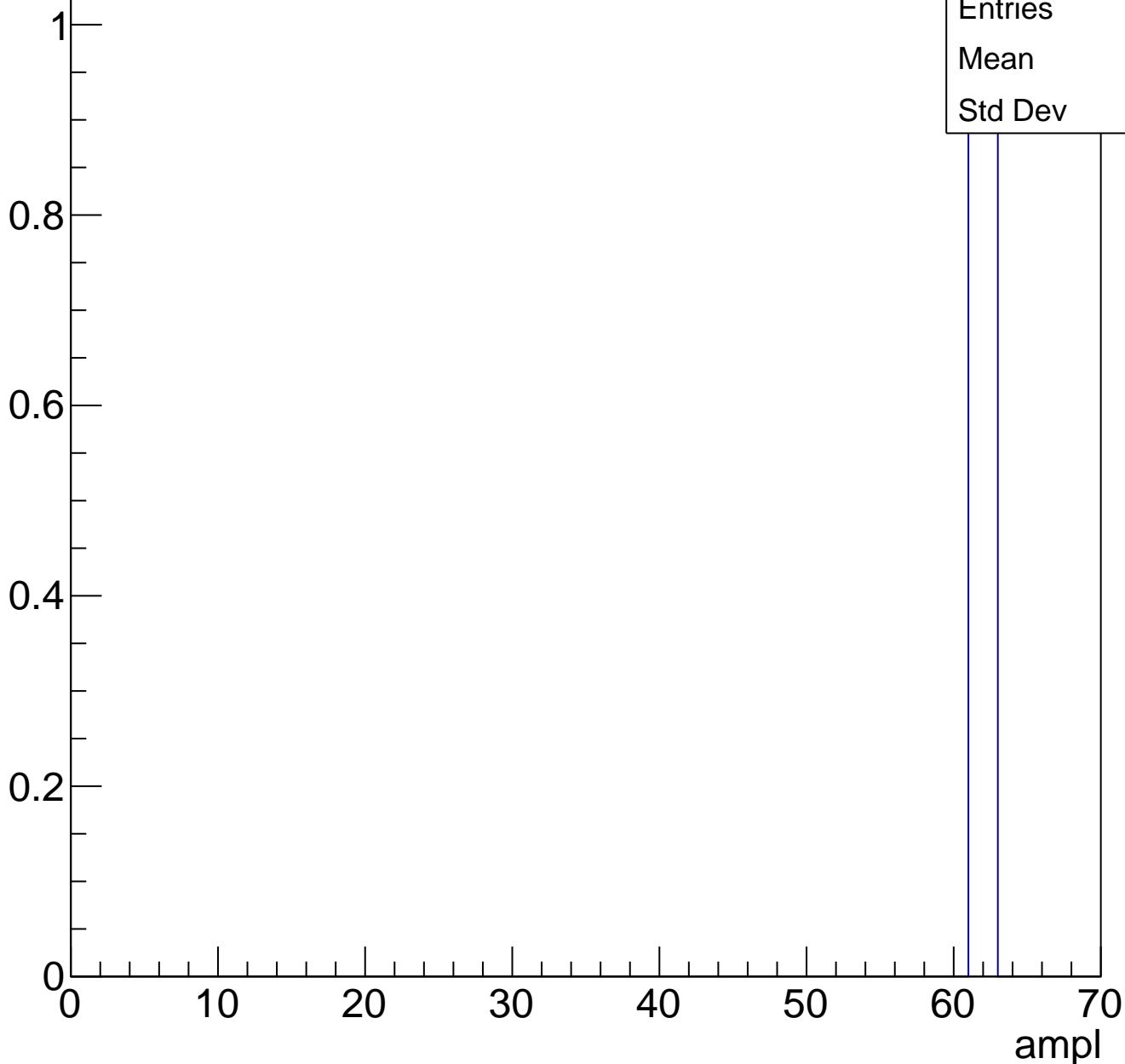
Entries	35
Mean	60.63
Std Dev	2.179



# B1L102S, U8-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch33, adc0

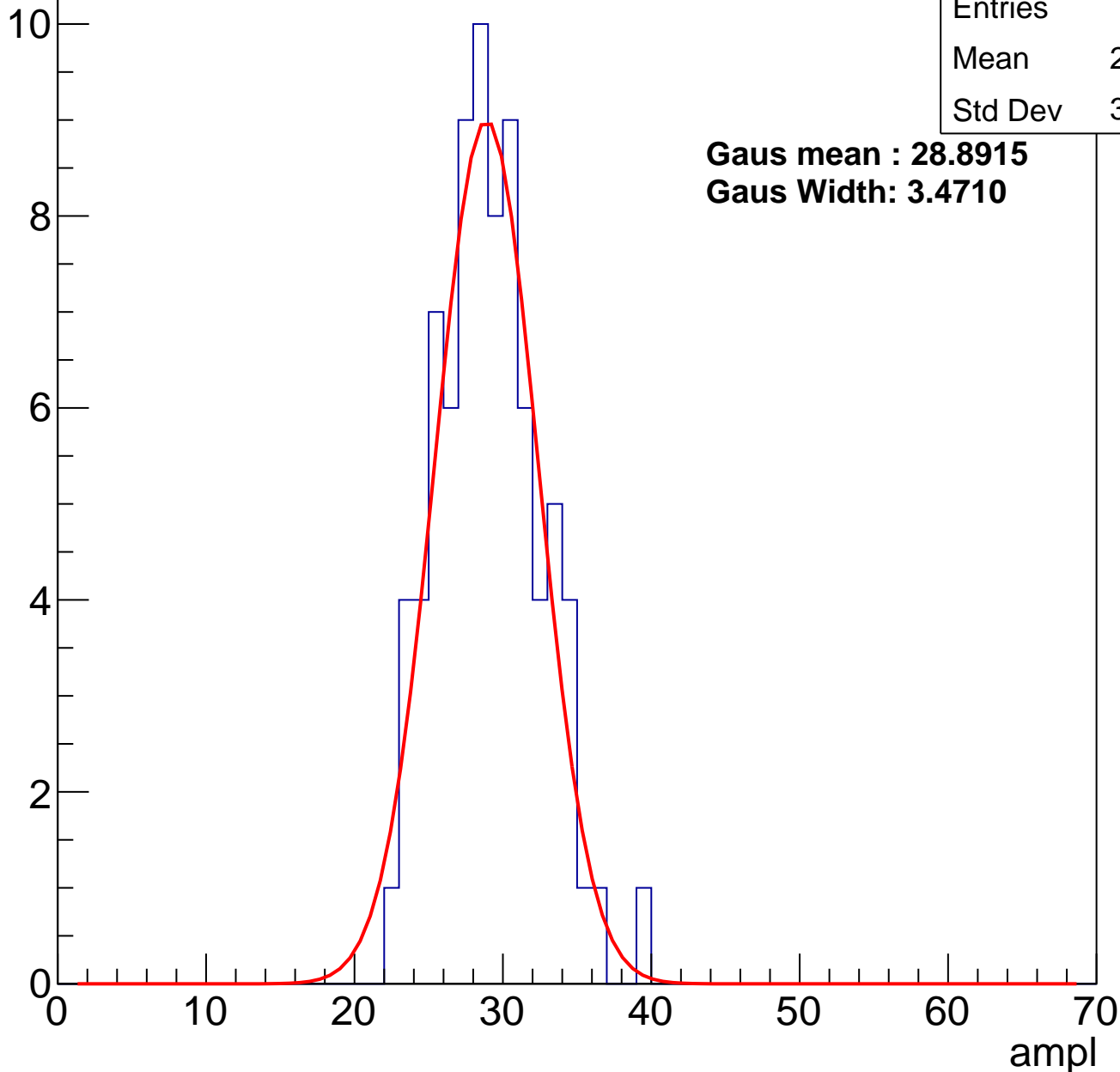
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	80
Mean	28.64
Std Dev	3.407

**Gaus mean : 28.8915**

**Gaus Width: 3.4710**

Entry



# B1L102S, U8-ch33, adc1

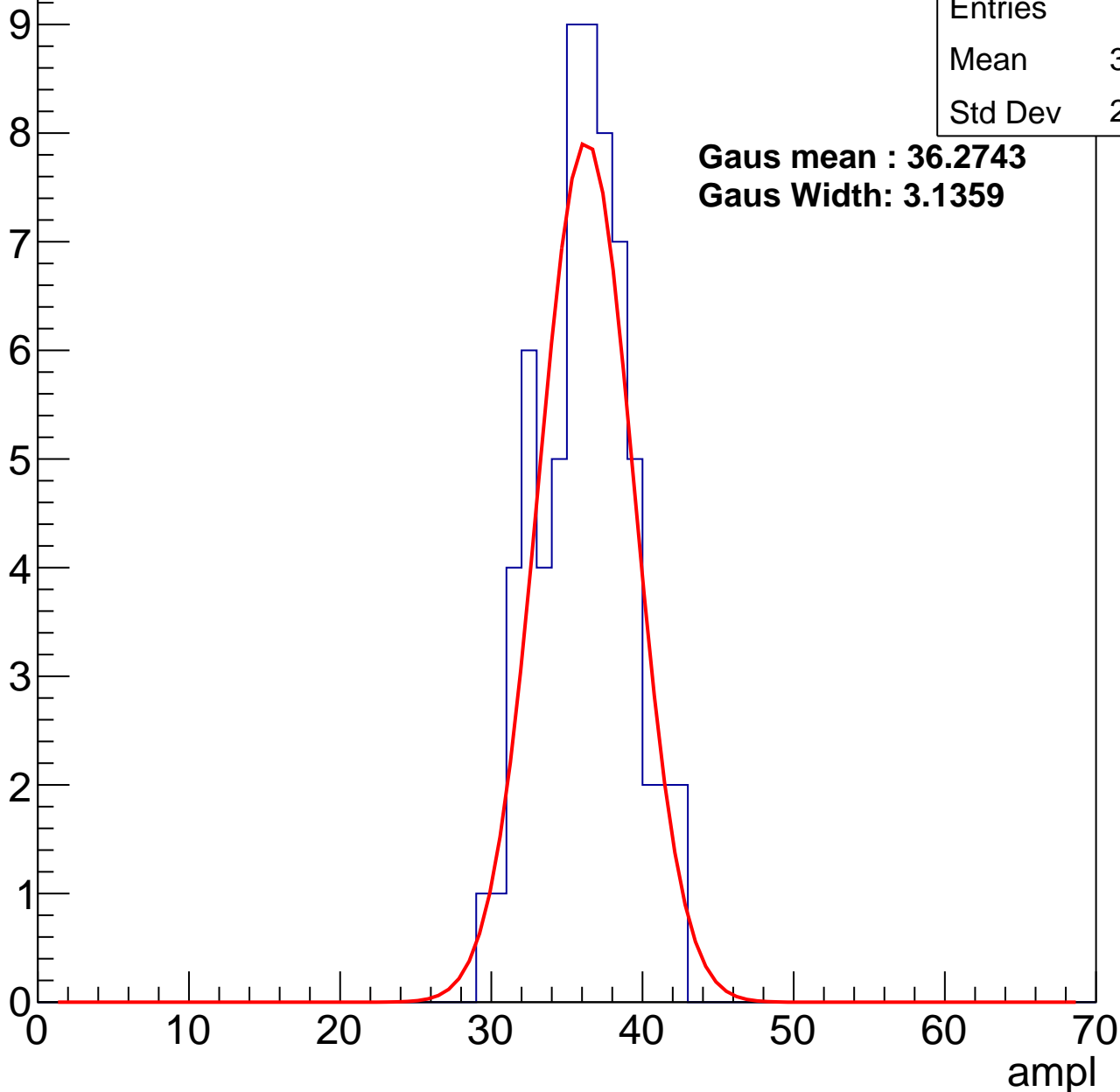
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	35.68
Std Dev	2.972

**Gaus mean : 36.2743**

**Gaus Width: 3.1359**



# B1L102S, U8-ch33, adc2

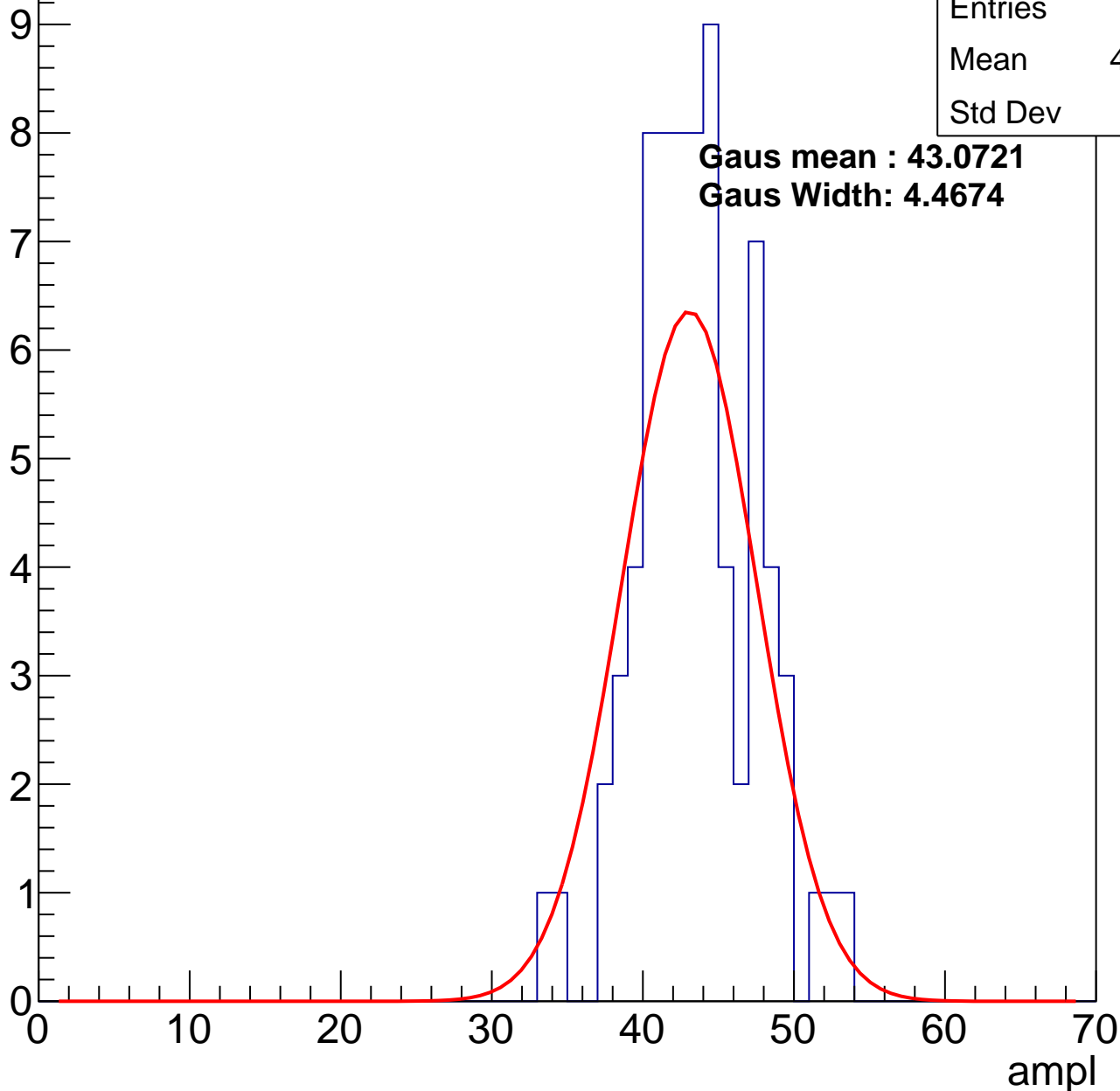
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	43.08
Std Dev	3.85

**Gaus mean : 43.0721**

**Gaus Width: 4.4674**

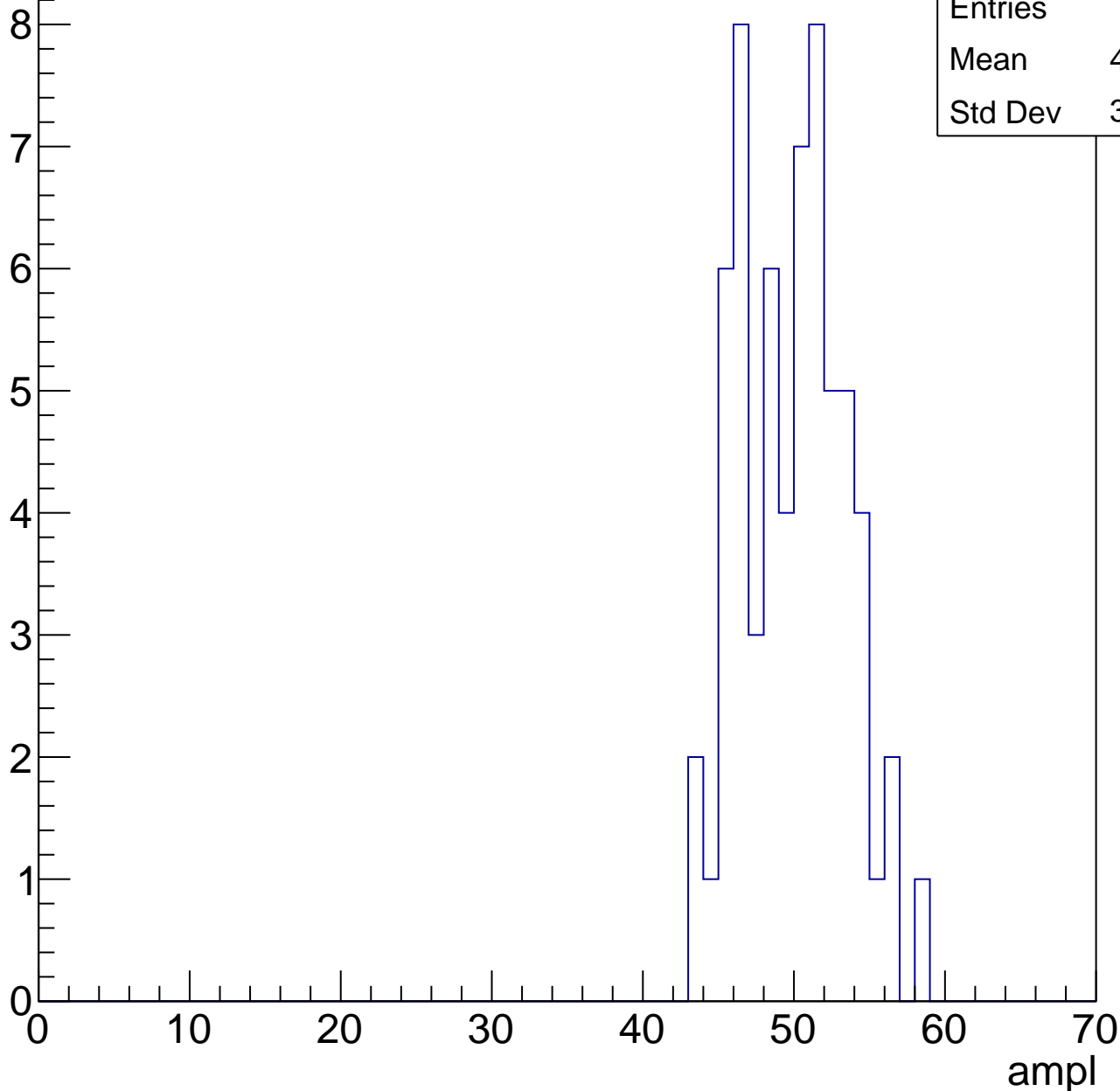


# B1L102S, U8-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

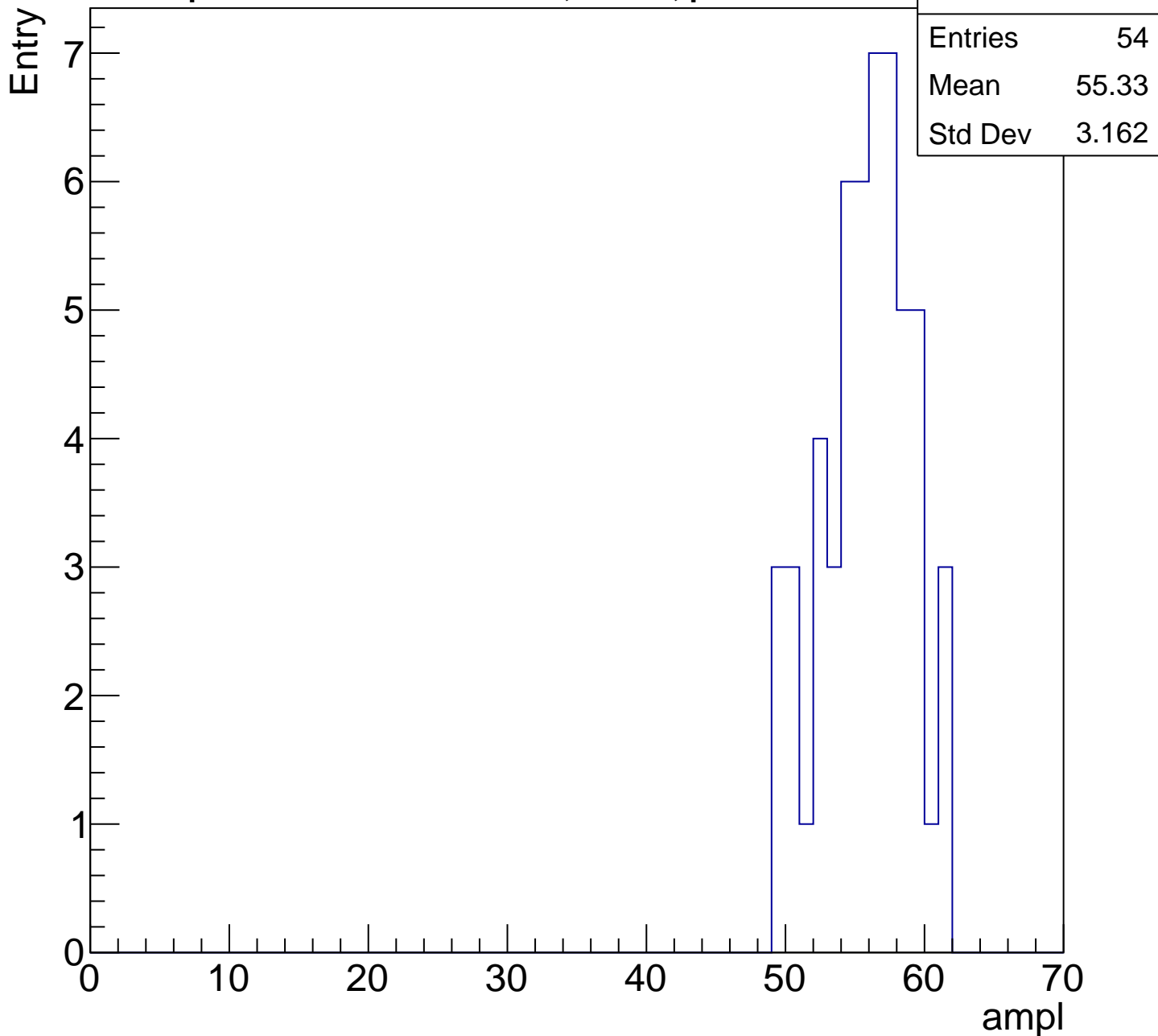
Entry

Entries	63
Mean	49.48
Std Dev	3.445



# B1L102S, U8-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

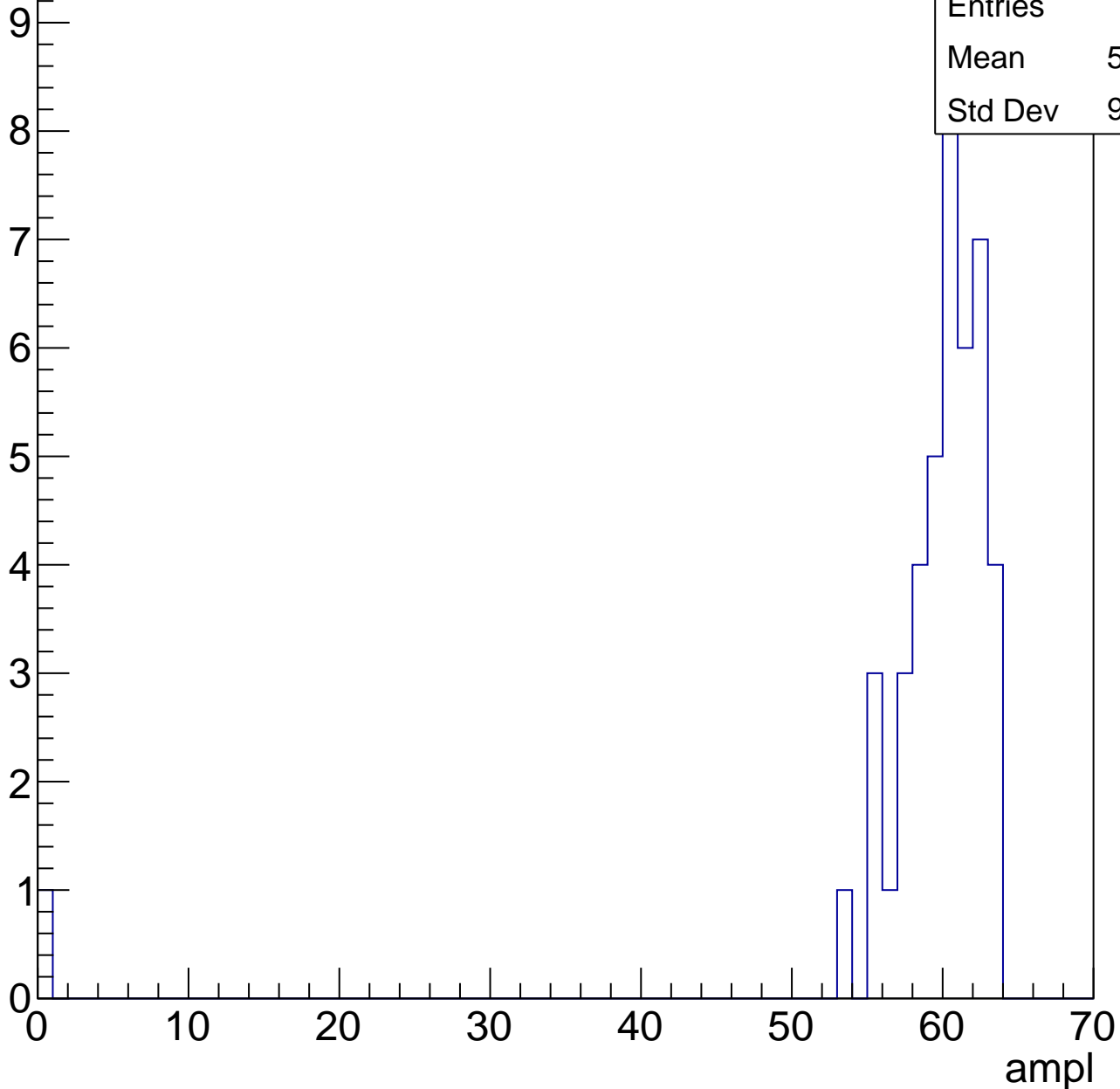


# B1L102S, U8-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	44
Mean	58.27
Std Dev	9.203

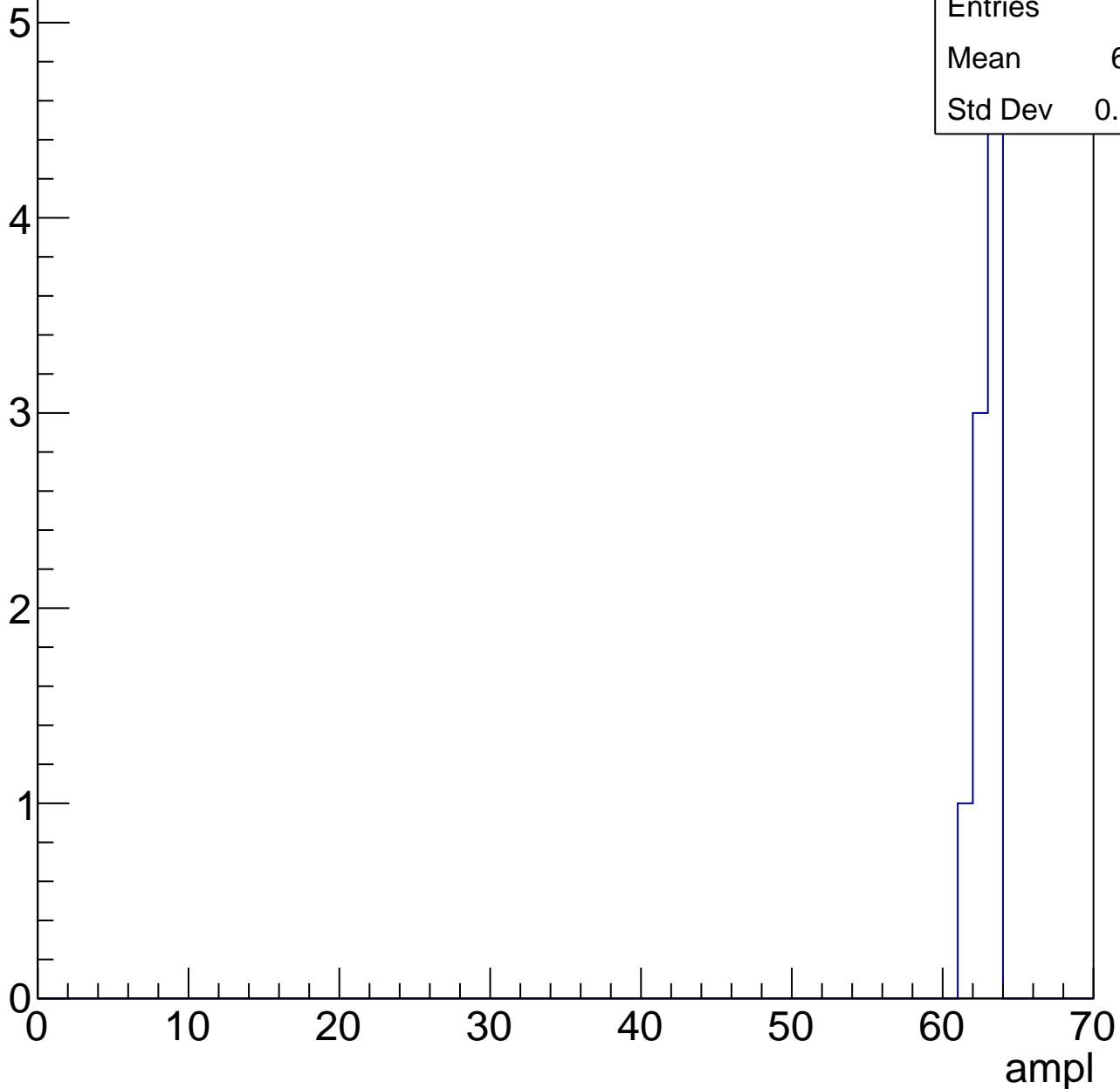


# B1L102S, U8-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	9
Mean	62.44
Std Dev	0.6849

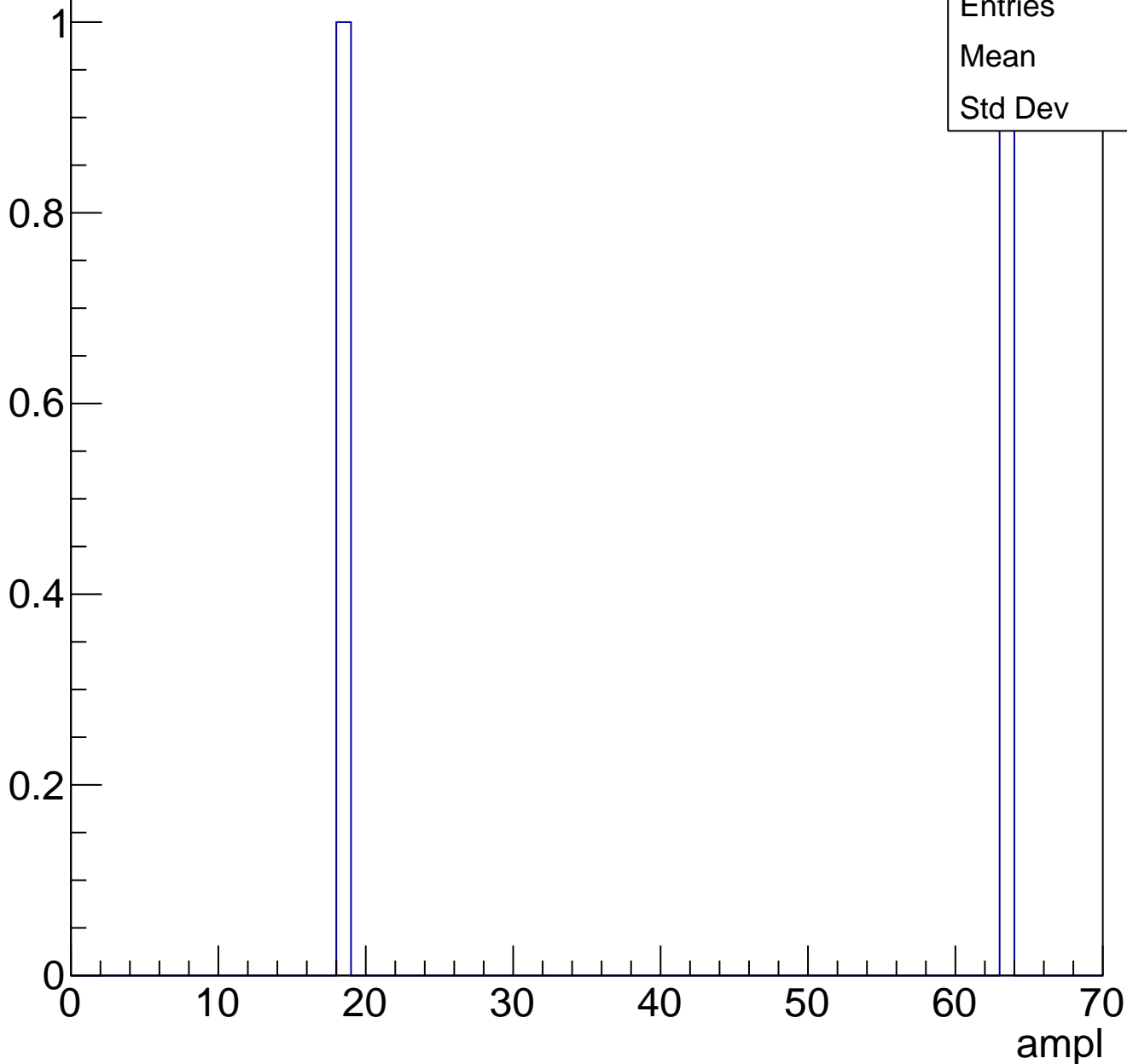




# B1L102S, U8-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch34, adc0

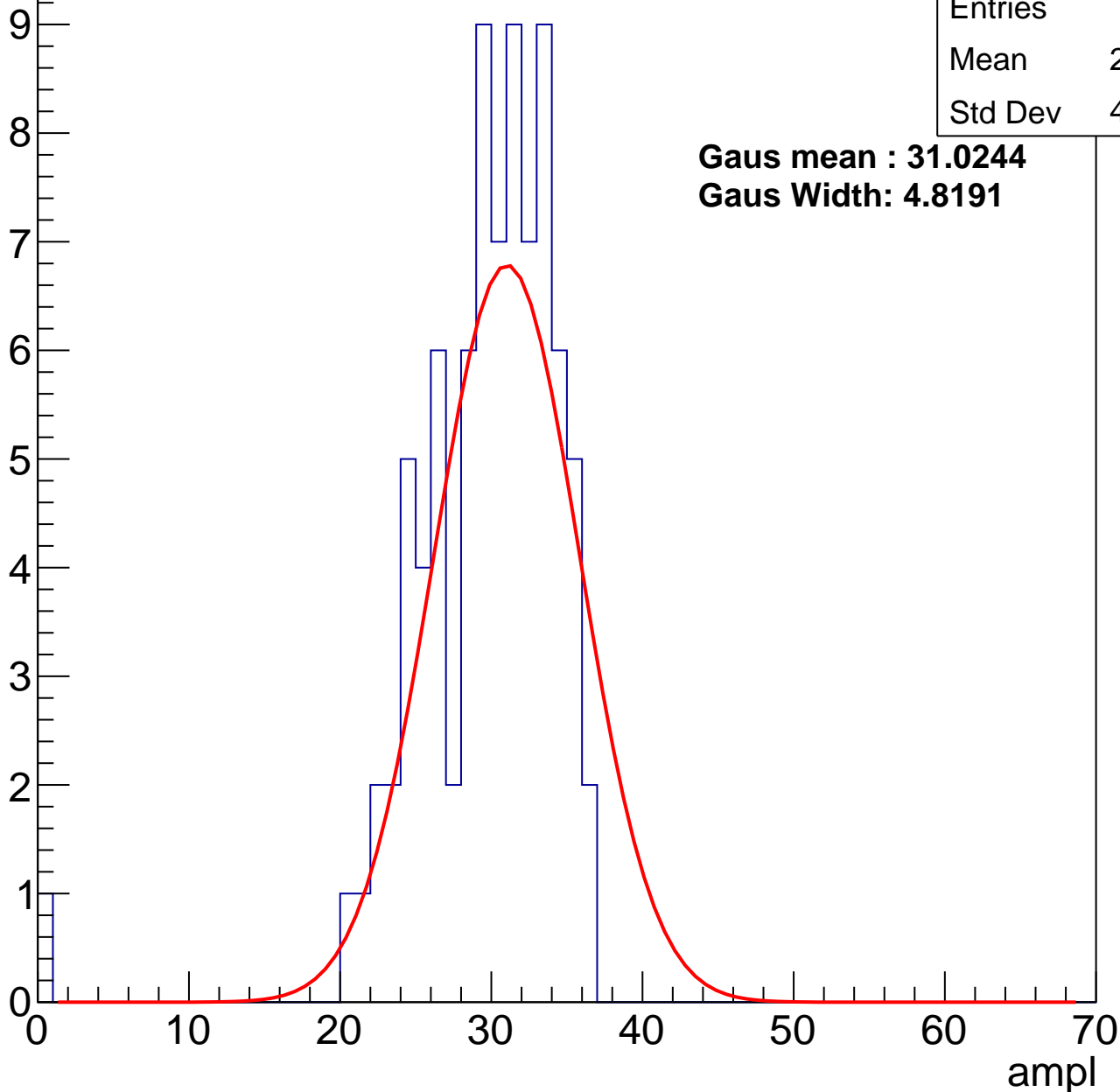
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	29.18
Std Dev	4.986

**Gaus mean : 31.0244**

**Gaus Width: 4.8191**



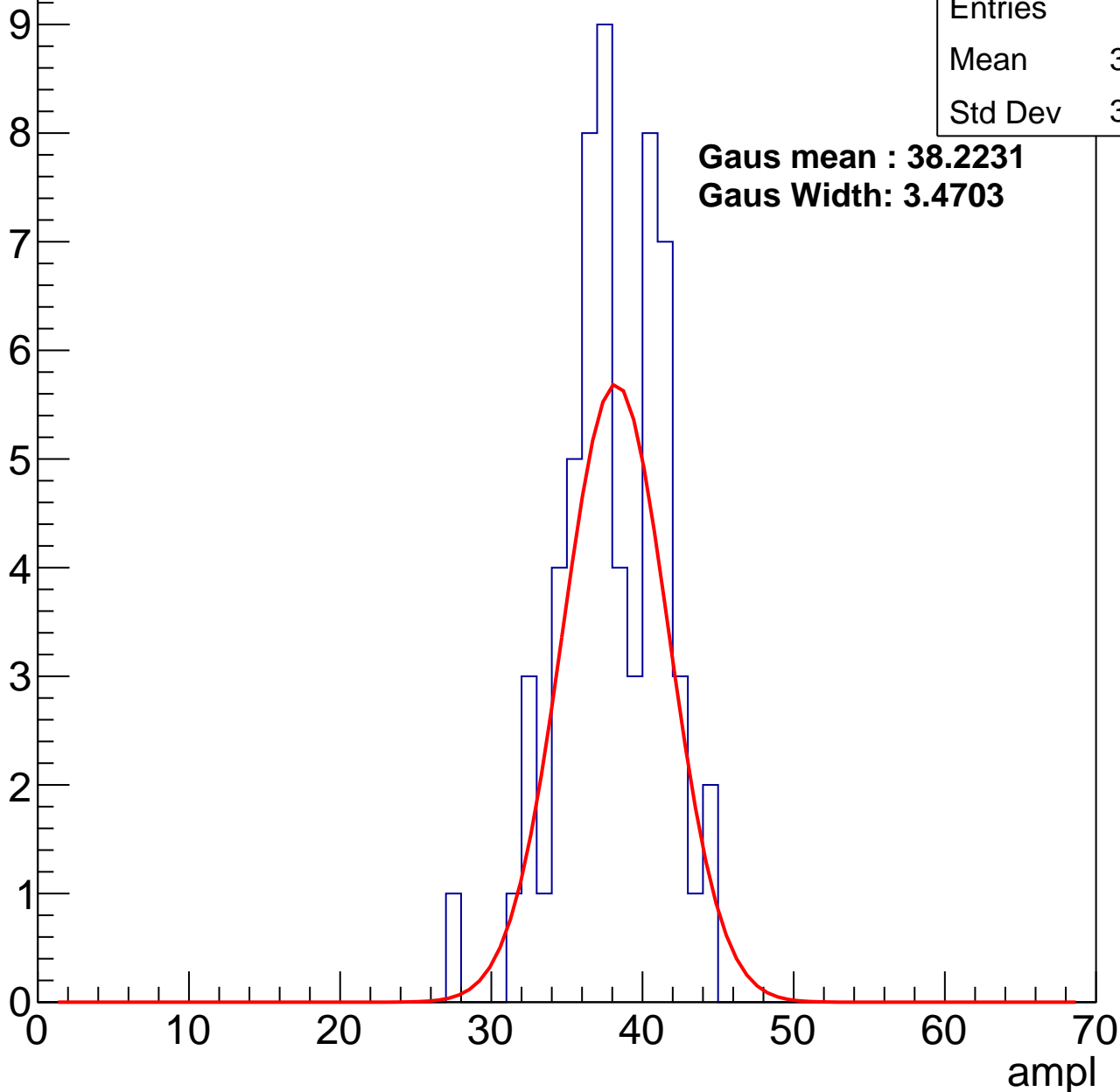
# B1L102S, U8-ch34, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	37.53
Std Dev	3.374

**Gaus mean : 38.2231**  
**Gaus Width: 3.4703**



# B1L102S, U8-ch34, adc2

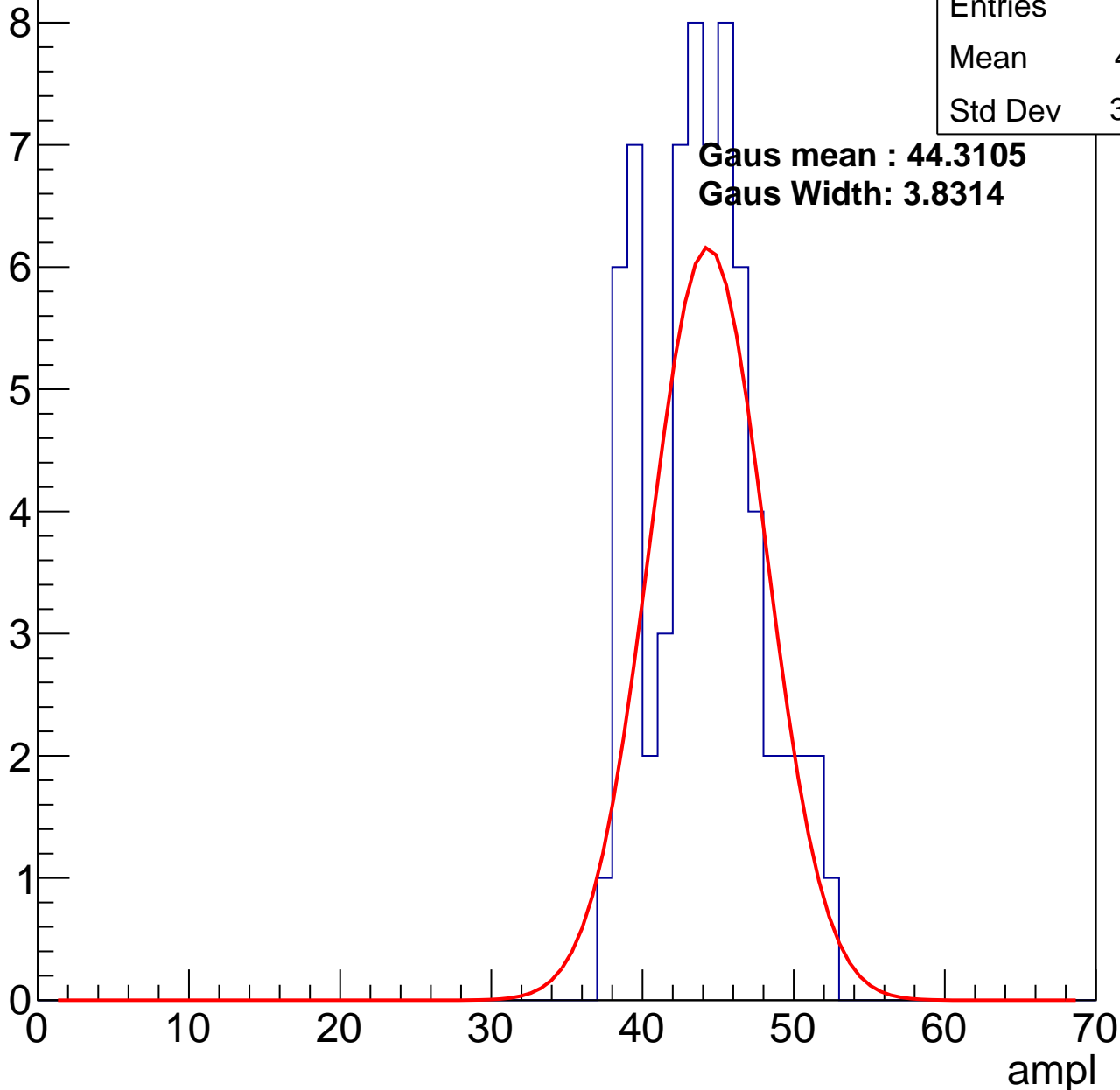
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	43.51
Std Dev	3.644

**Gaus mean : 44.3105**

**Gaus Width: 3.8314**

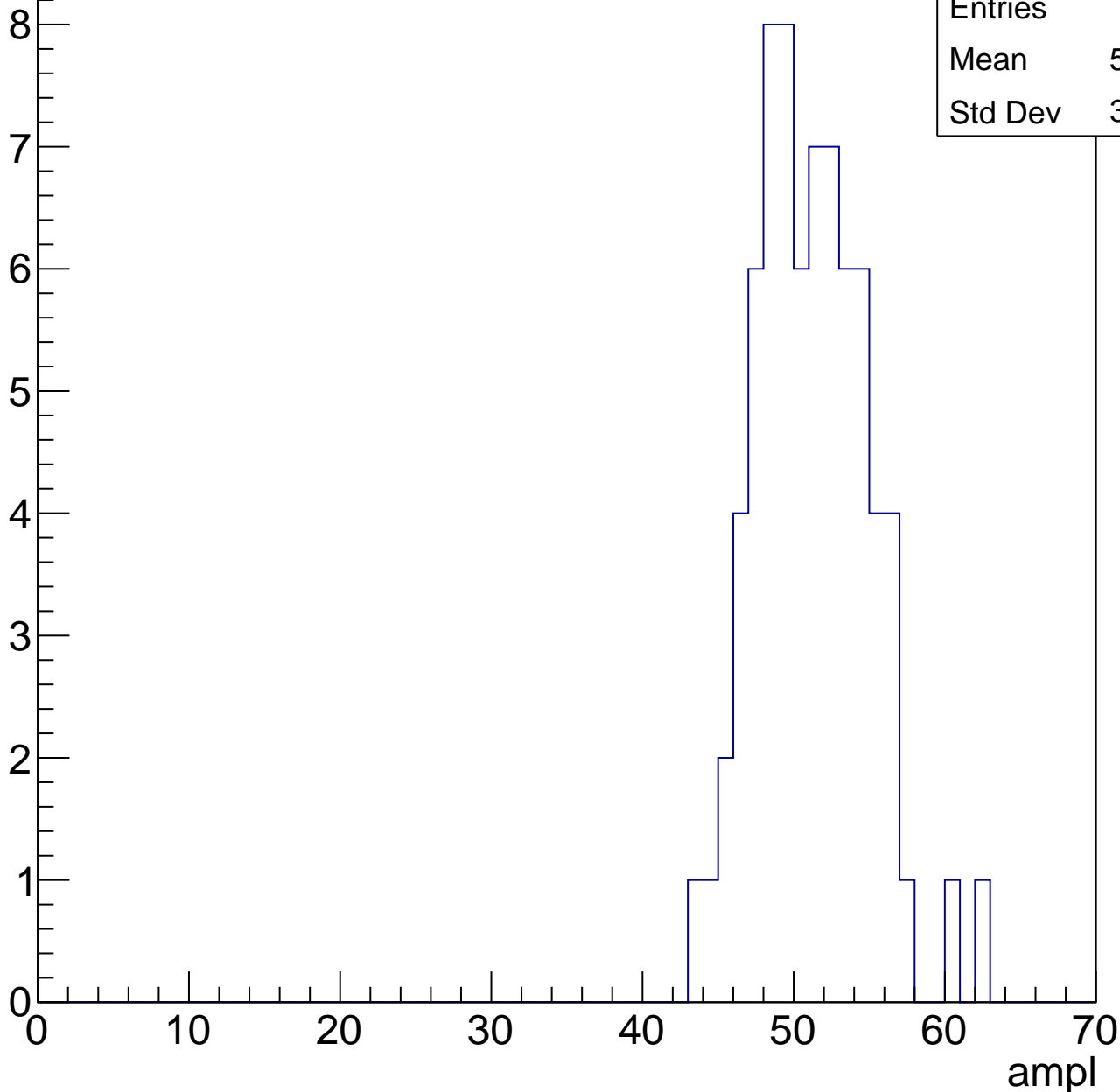


# B1L102S, U8-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	50.75
Std Dev	3.652

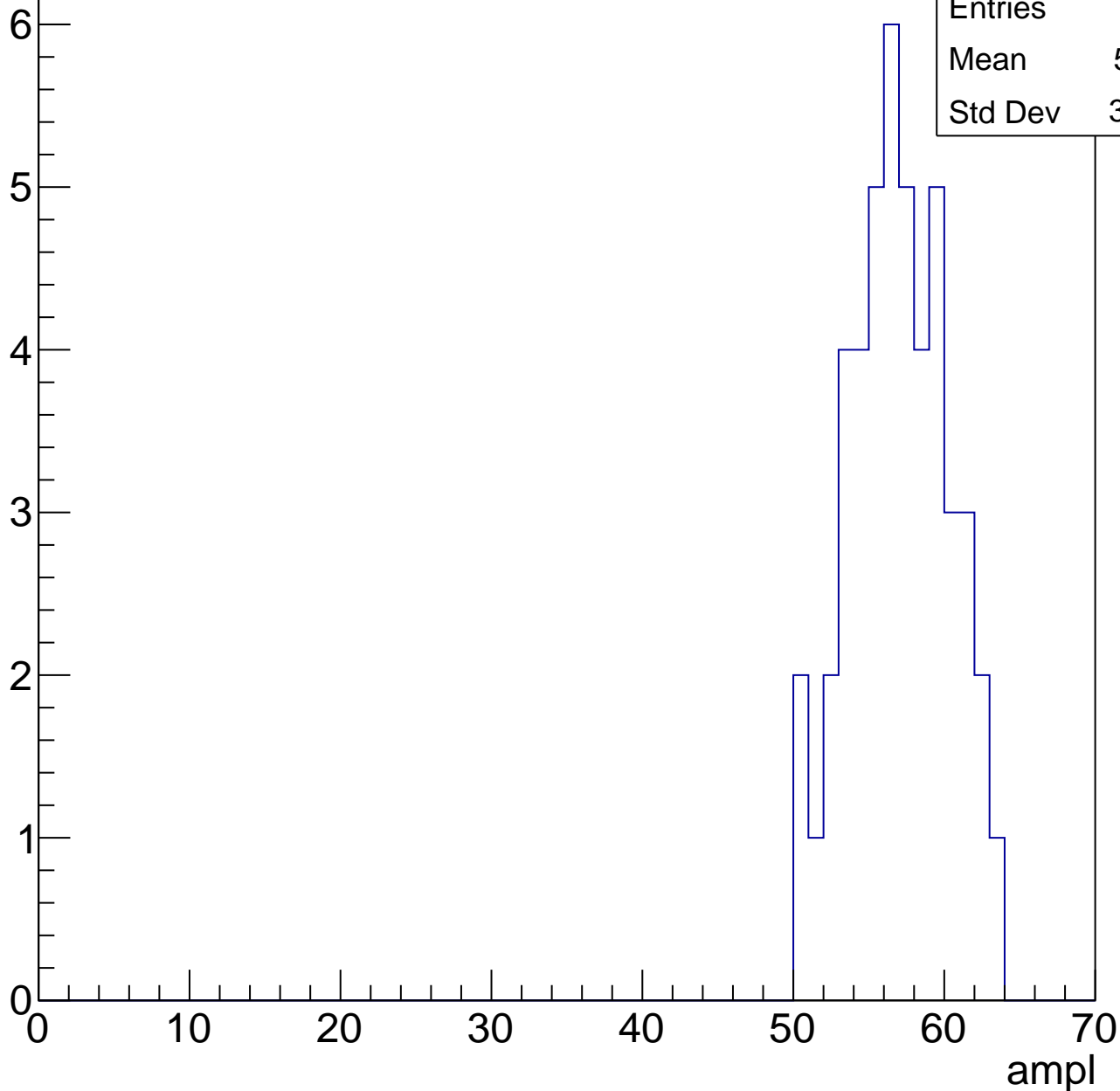


# B1L102S, U8-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	56.51
Std Dev	3.208

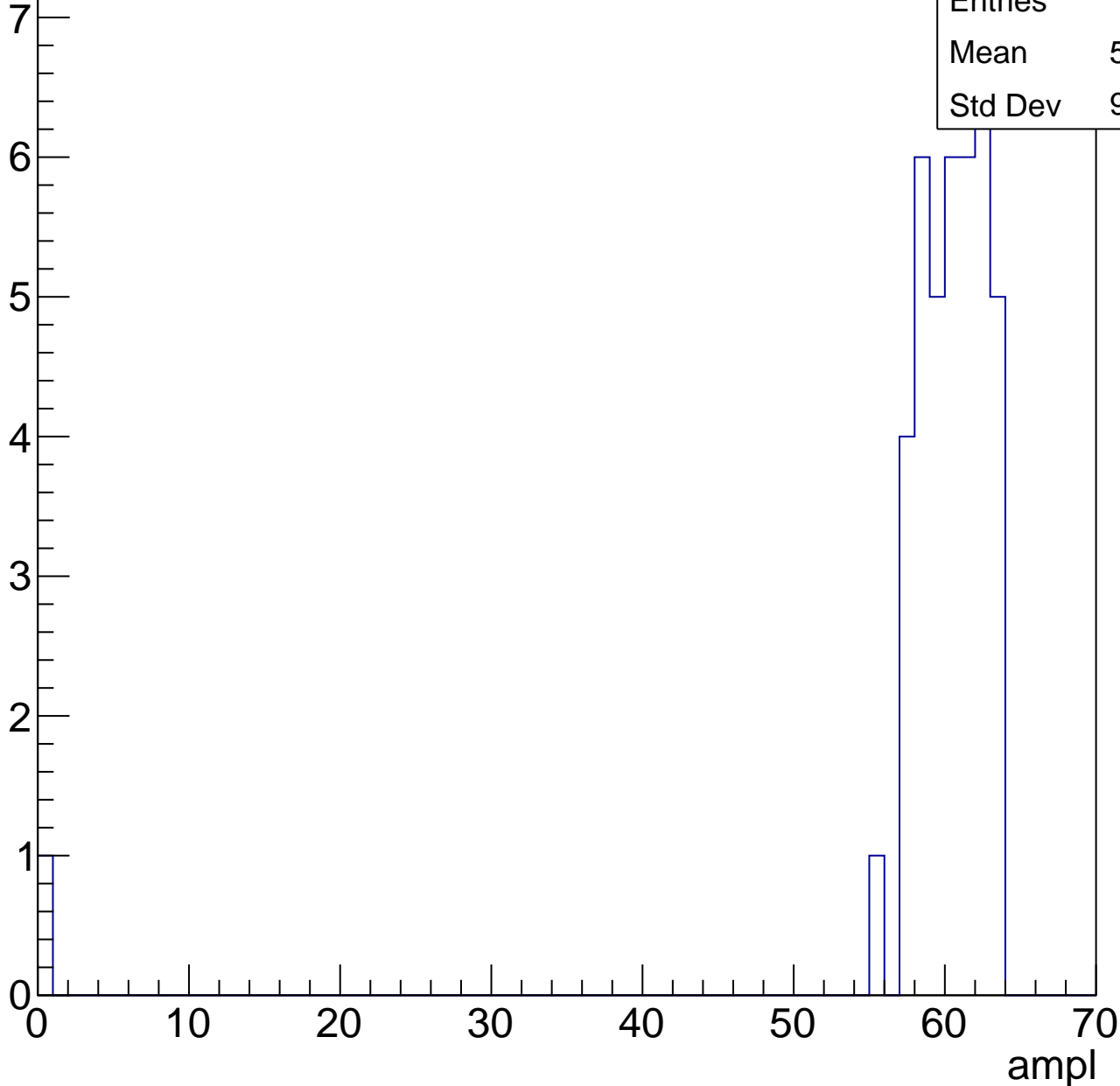


# B1L102S, U8-ch34, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

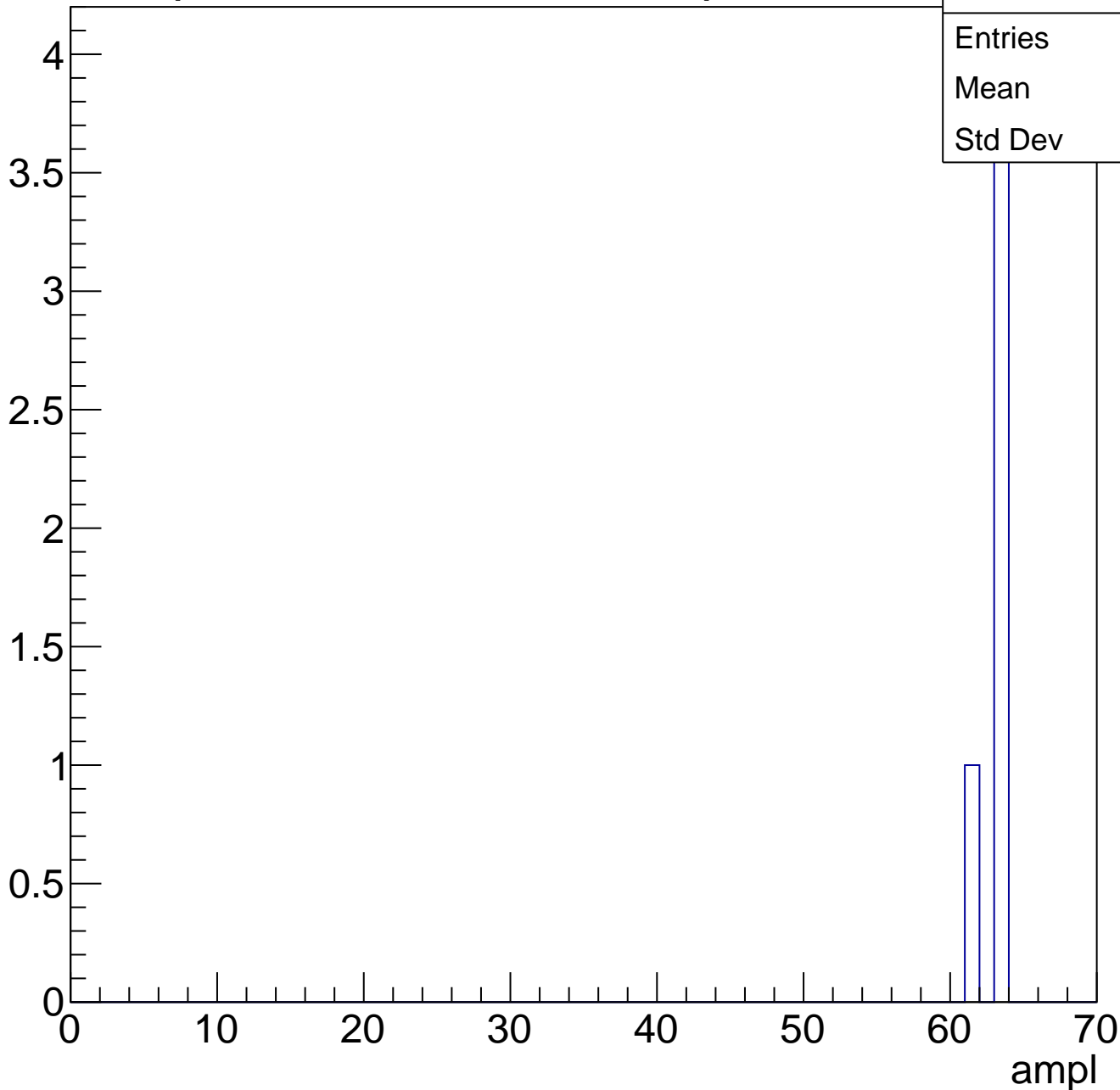
Entries	41
Mean	58.56
Std Dev	9.479



# B1L102S, U8-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch35, adc0

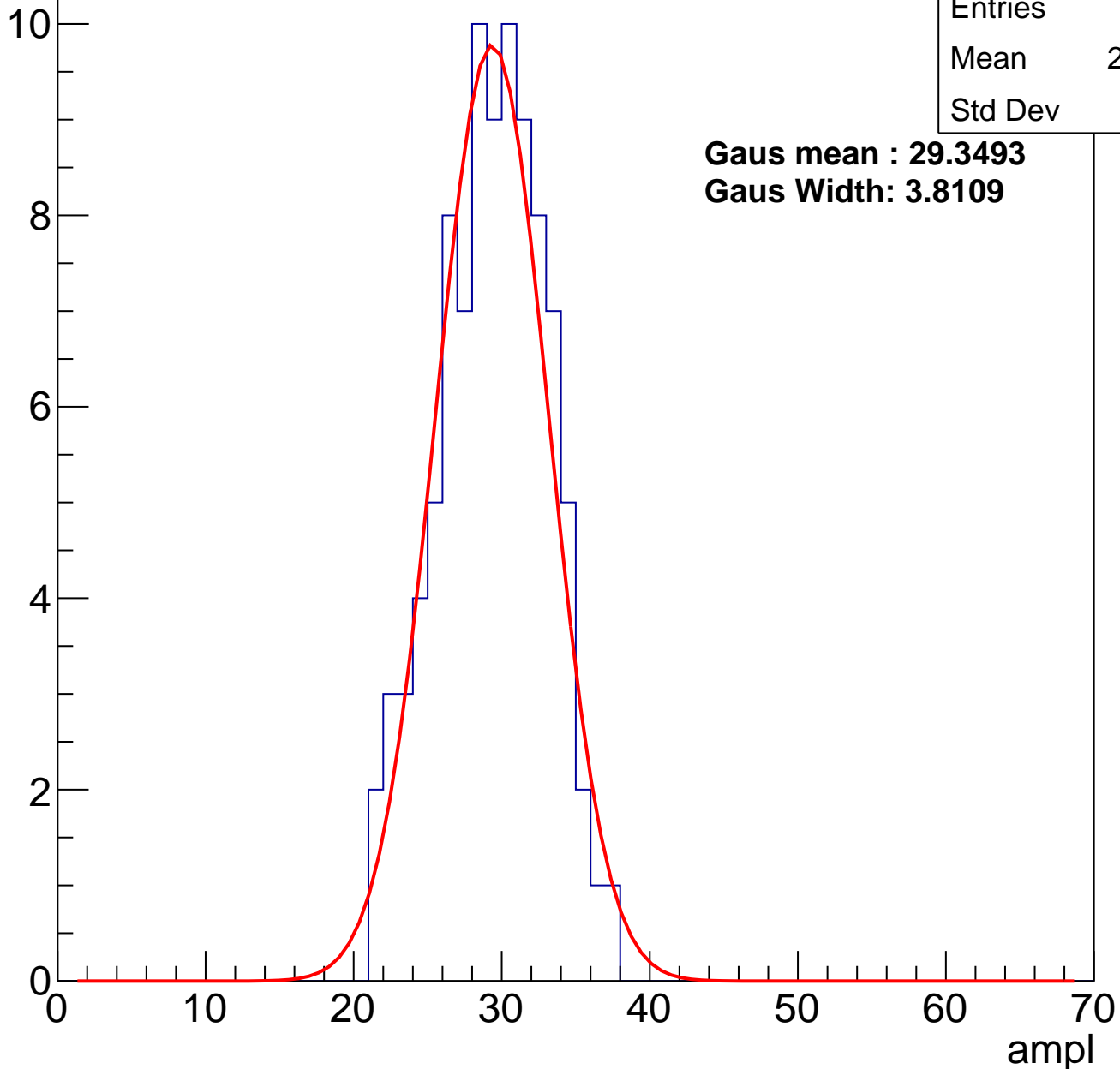
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	94
Mean	28.88
Std Dev	3.59

**Gaus mean : 29.3493**

**Gaus Width: 3.8109**

Entry



# B1L102S, U8-ch35, adc1

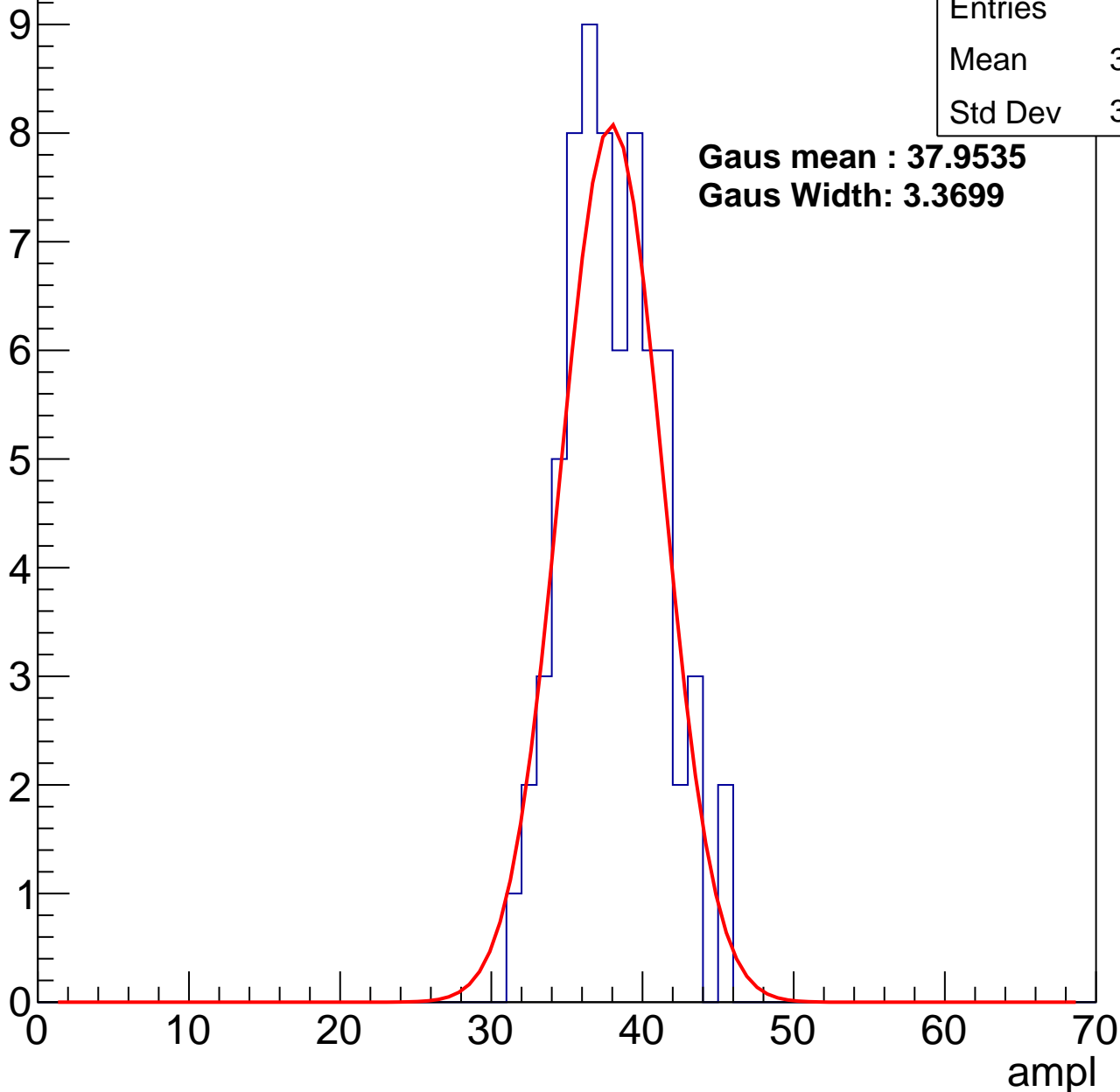
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	37.58
Std Dev	3.118

**Gaus mean : 37.9535**

**Gaus Width: 3.3699**



# B1L102S, U8-ch35, adc2

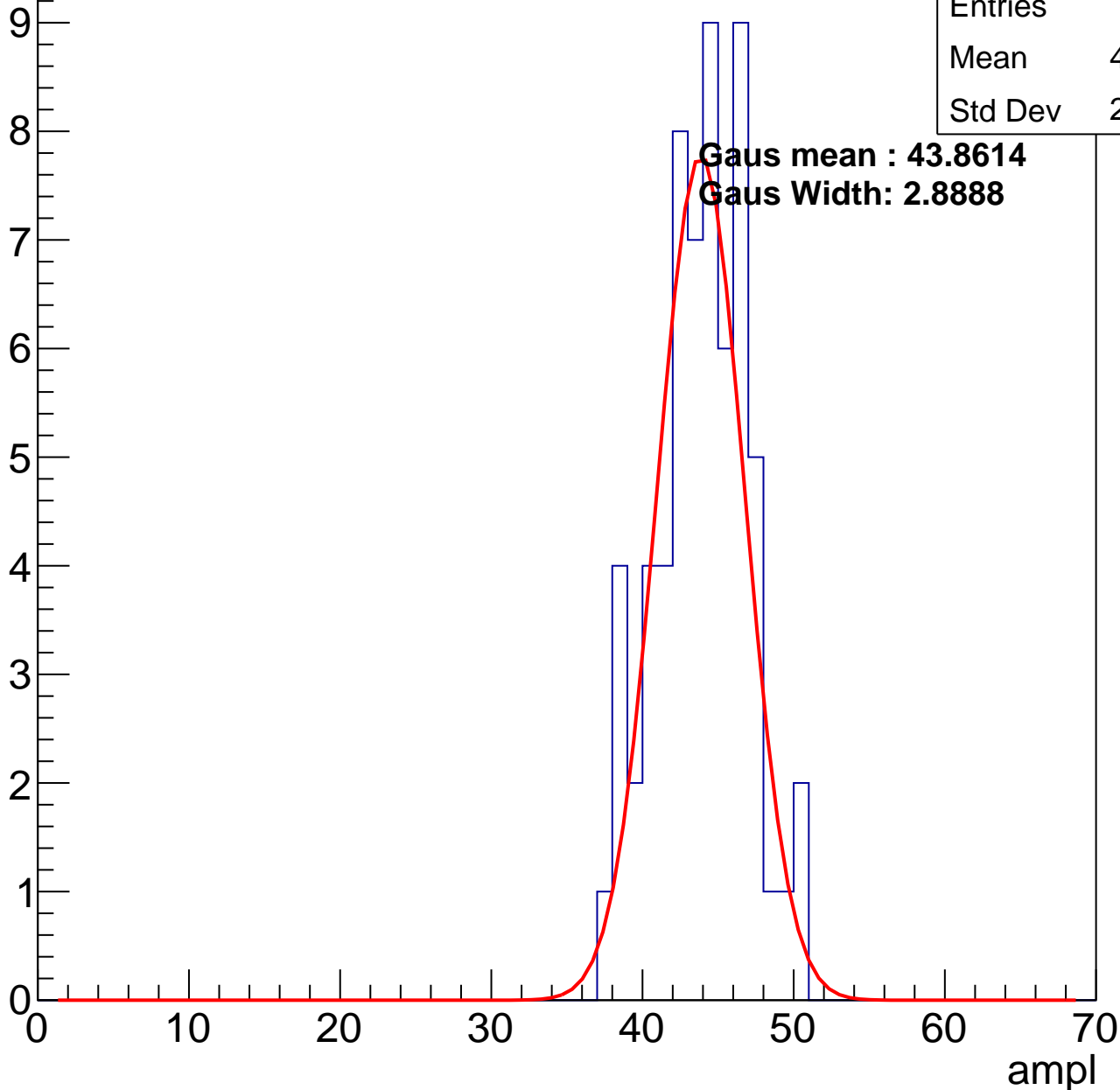
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	43.49
Std Dev	2.997

**Gaus mean : 43.8614**

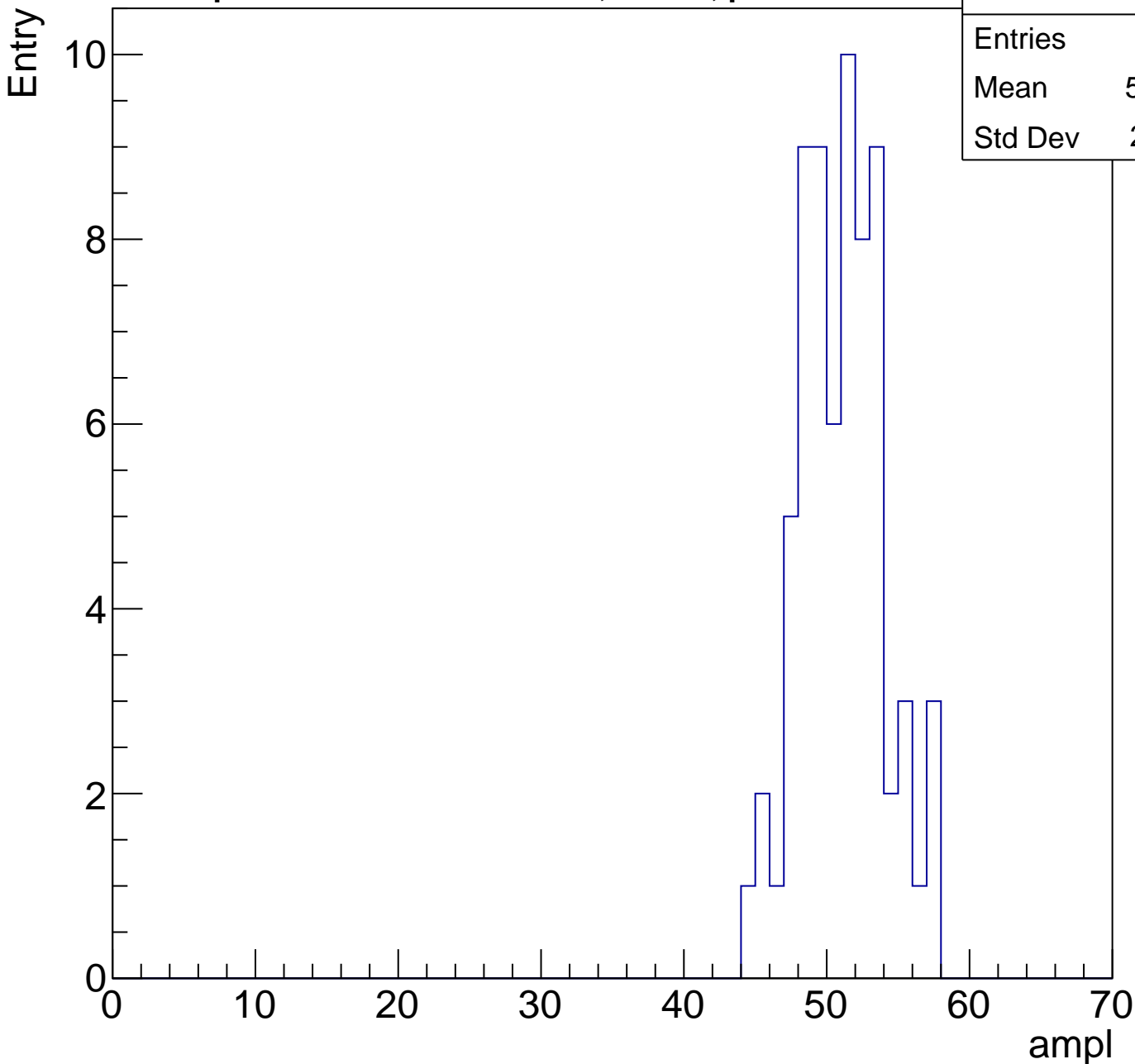
**Gaus Width: 2.8888**



# B1L102S, U8-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	69
Mean	50.59
Std Dev	2.901

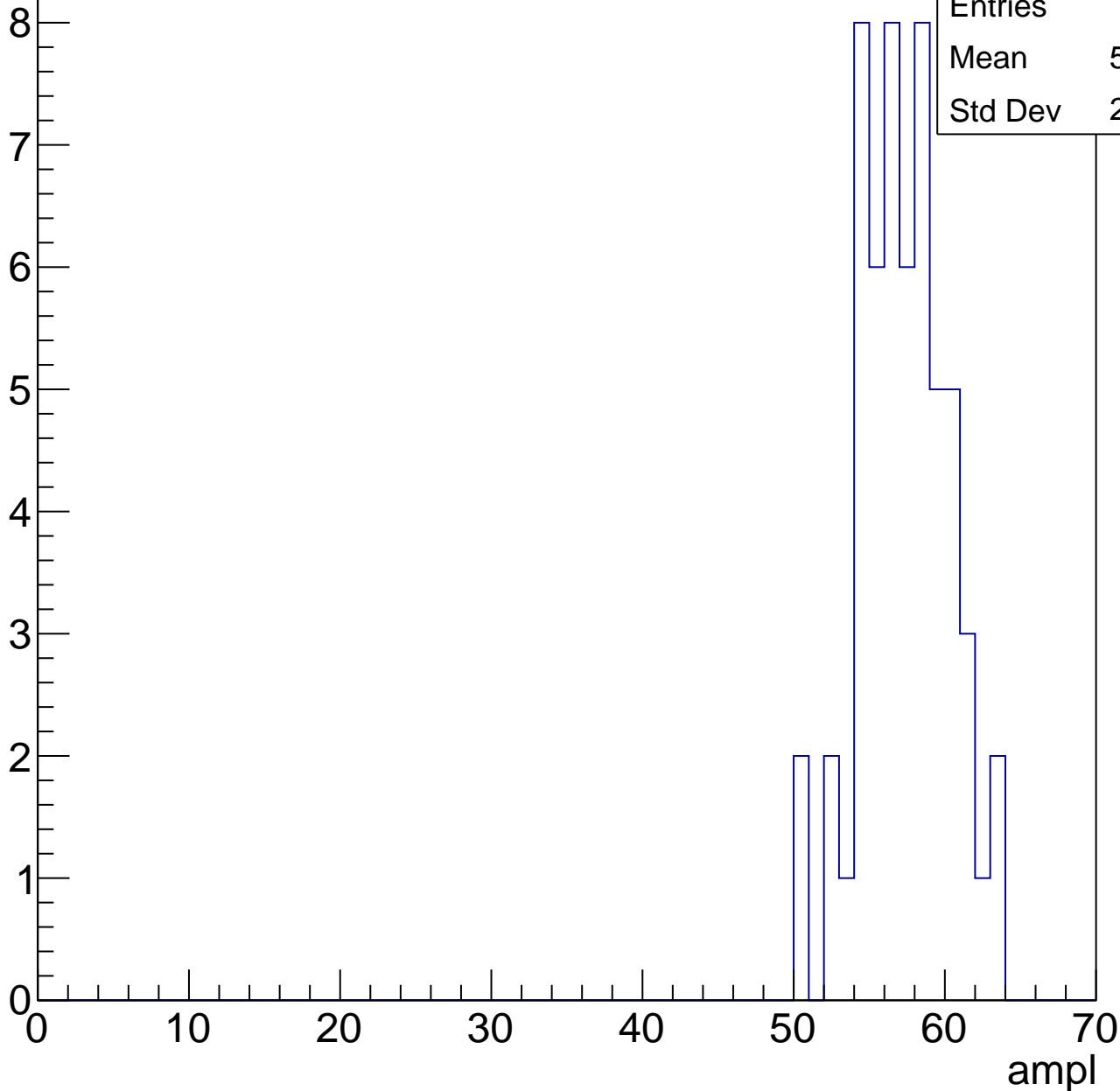


# B1L102S, U8-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	56.82
Std Dev	2.915

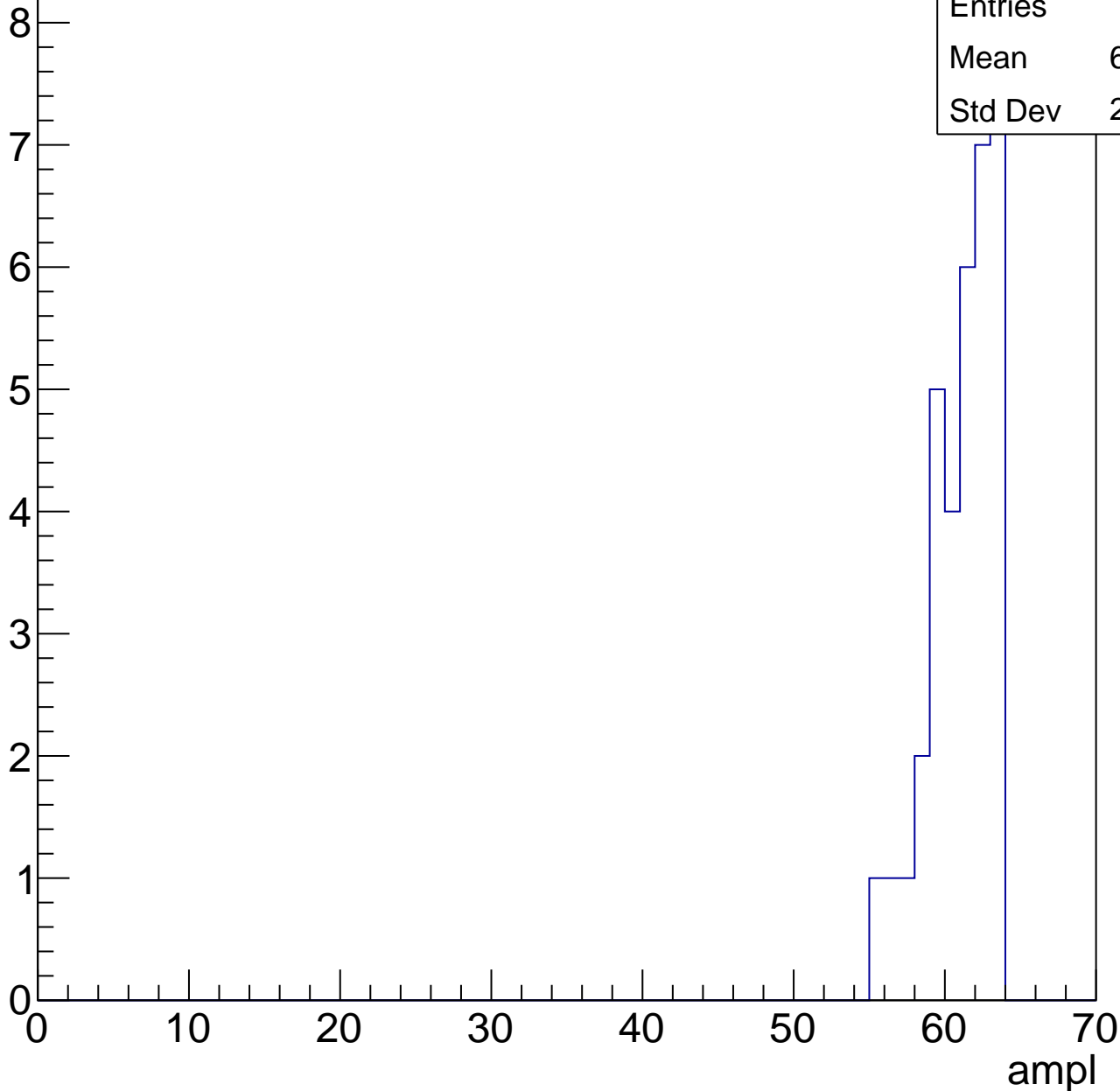


# B1L102S, U8-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

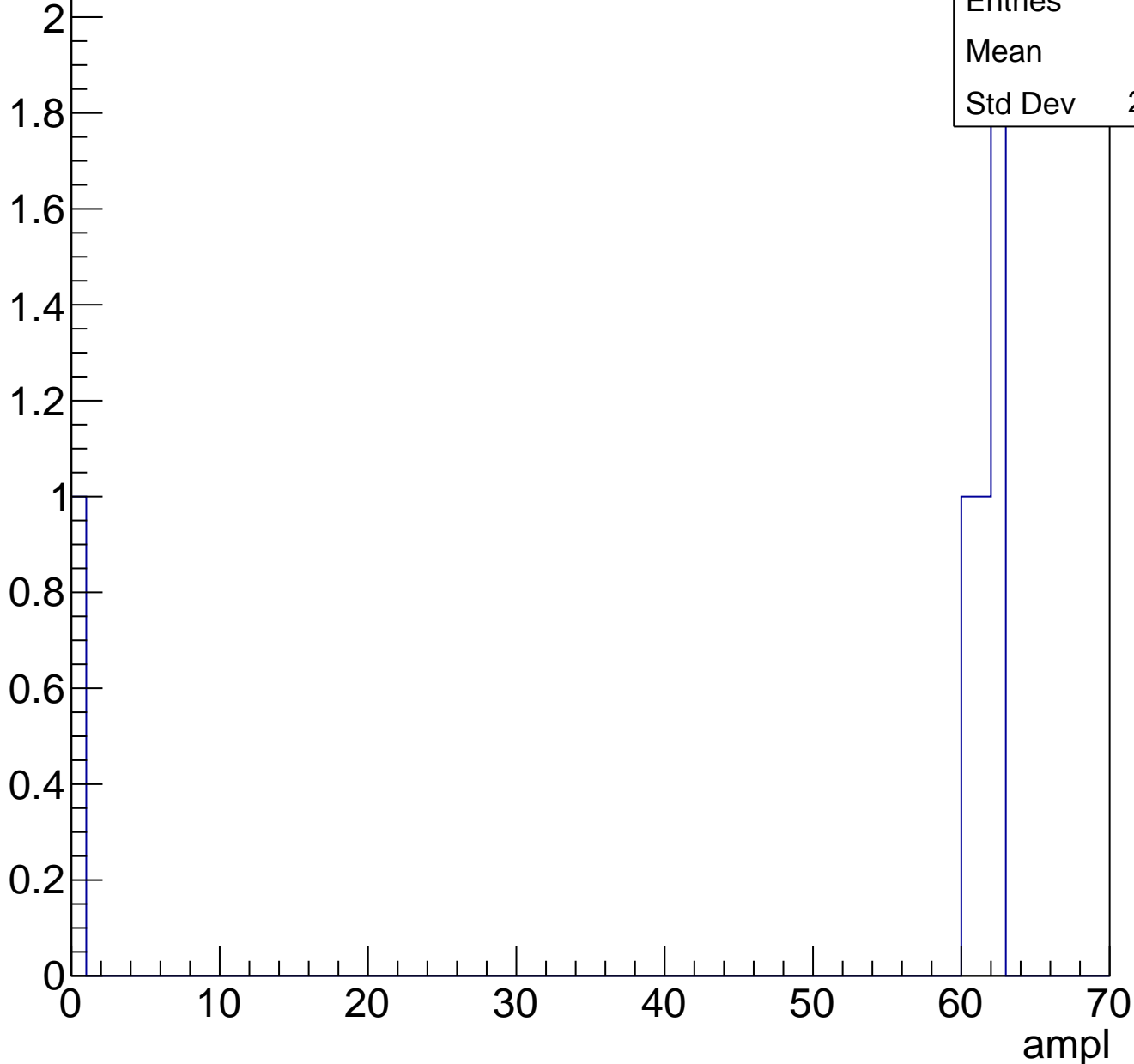
Entries	35
Mean	60.66
Std Dev	2.097



# B1L102S, U8-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	10.5
Std Dev	10.5

# B1L102S, U8-ch36, adc0

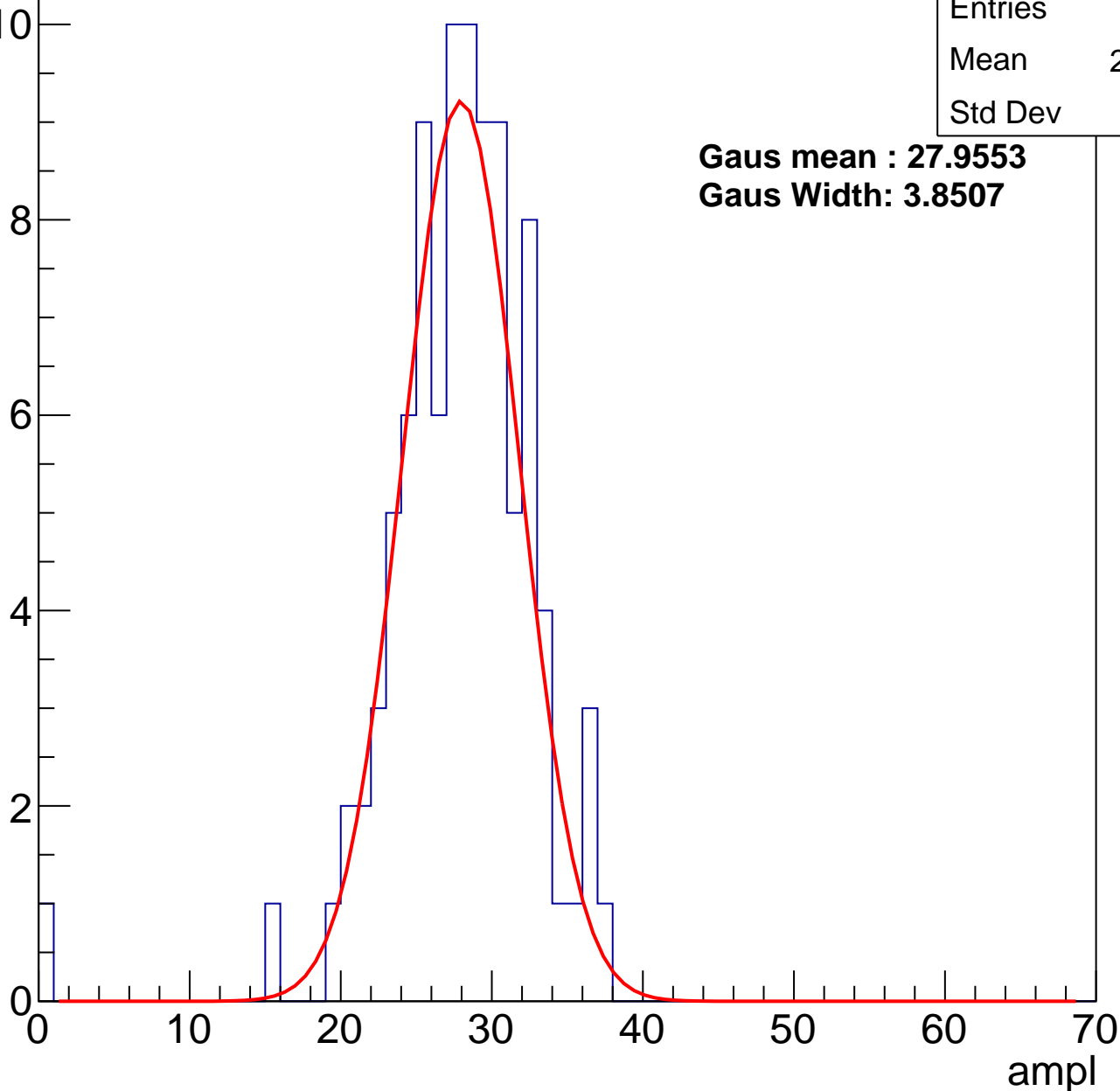
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	97
Mean	27.42
Std Dev	4.92

**Gaus mean : 27.9553**

**Gaus Width: 3.8507**



# B1L102S, U8-ch36, adc1

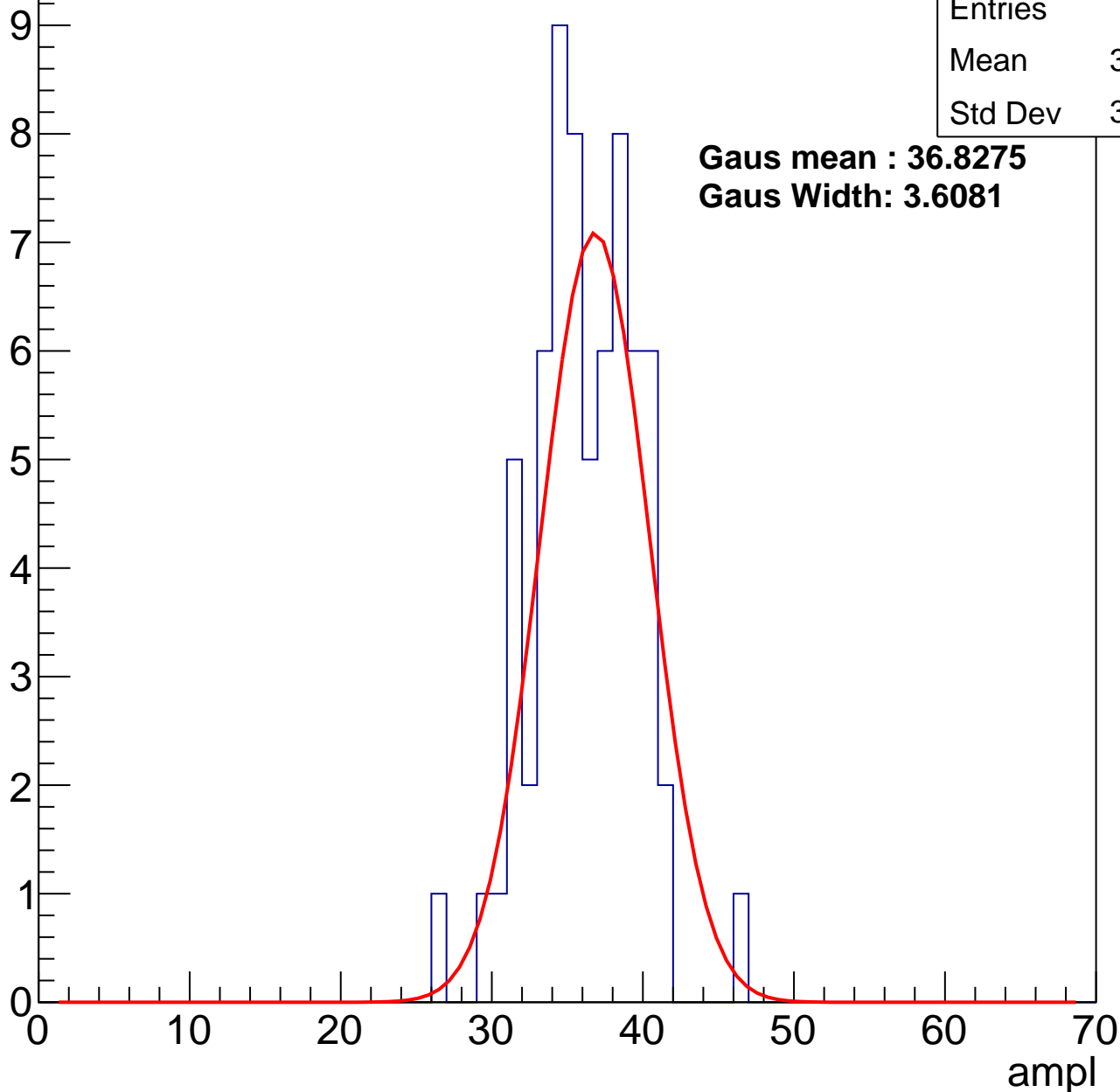
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	35.76
Std Dev	3.399

**Gaus mean : 36.8275**

**Gaus Width: 3.6081**



# B1L102S, U8-ch36, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	82
Mean	43.72
Std Dev	3.726

**Gaus mean : 44.1430**

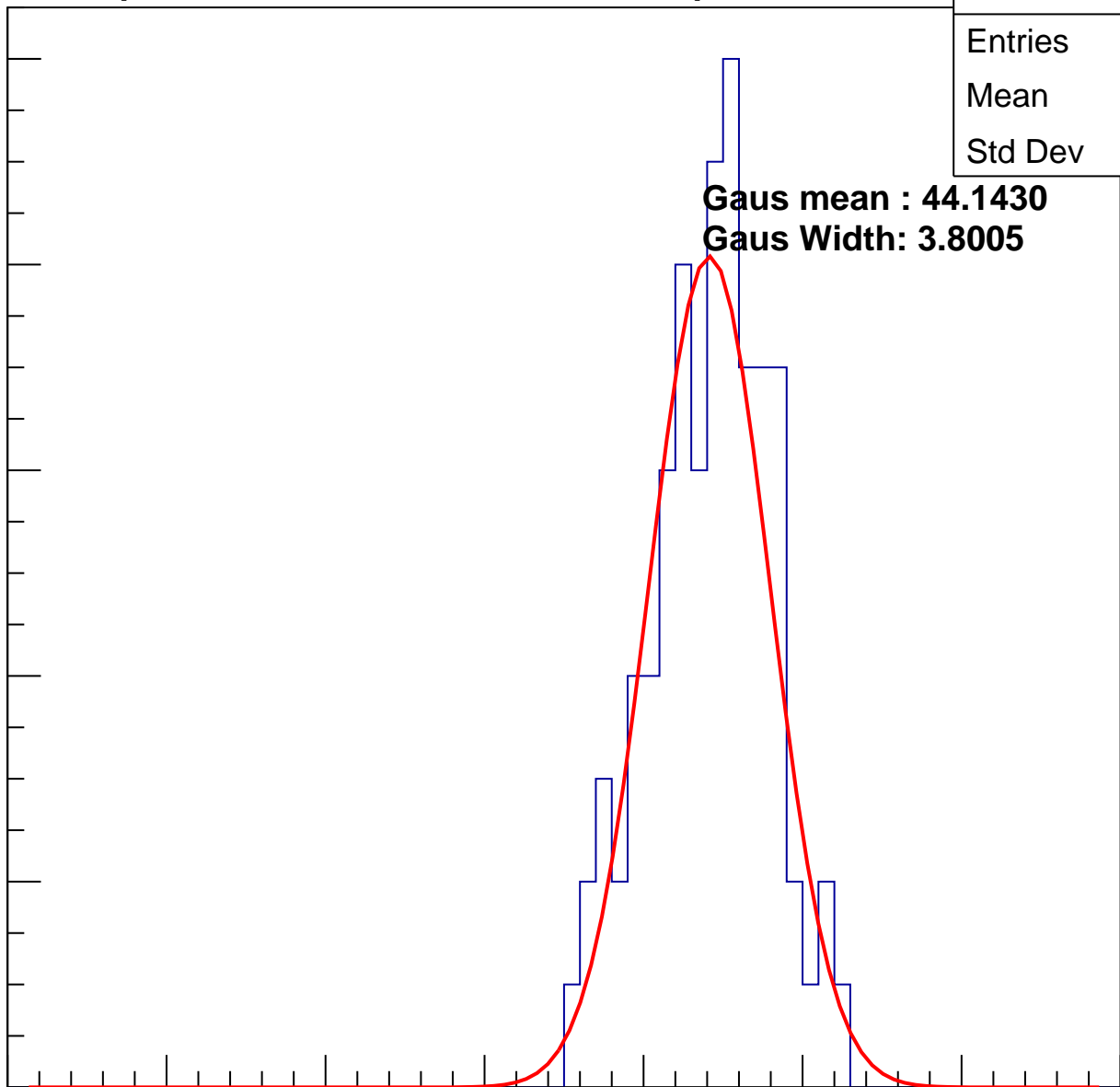
**Gaus Width: 3.8005**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

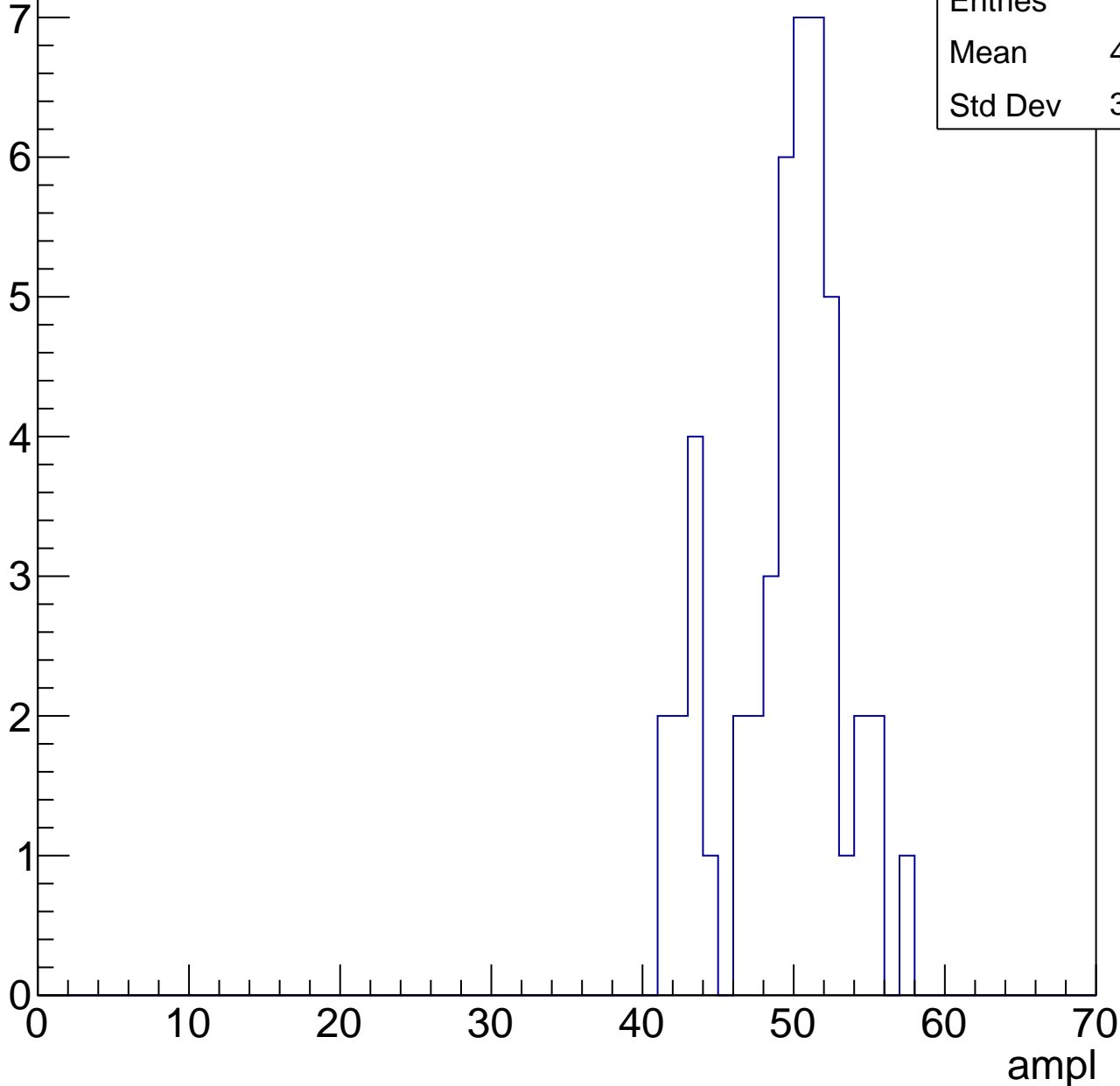


# B1L102S, U8-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

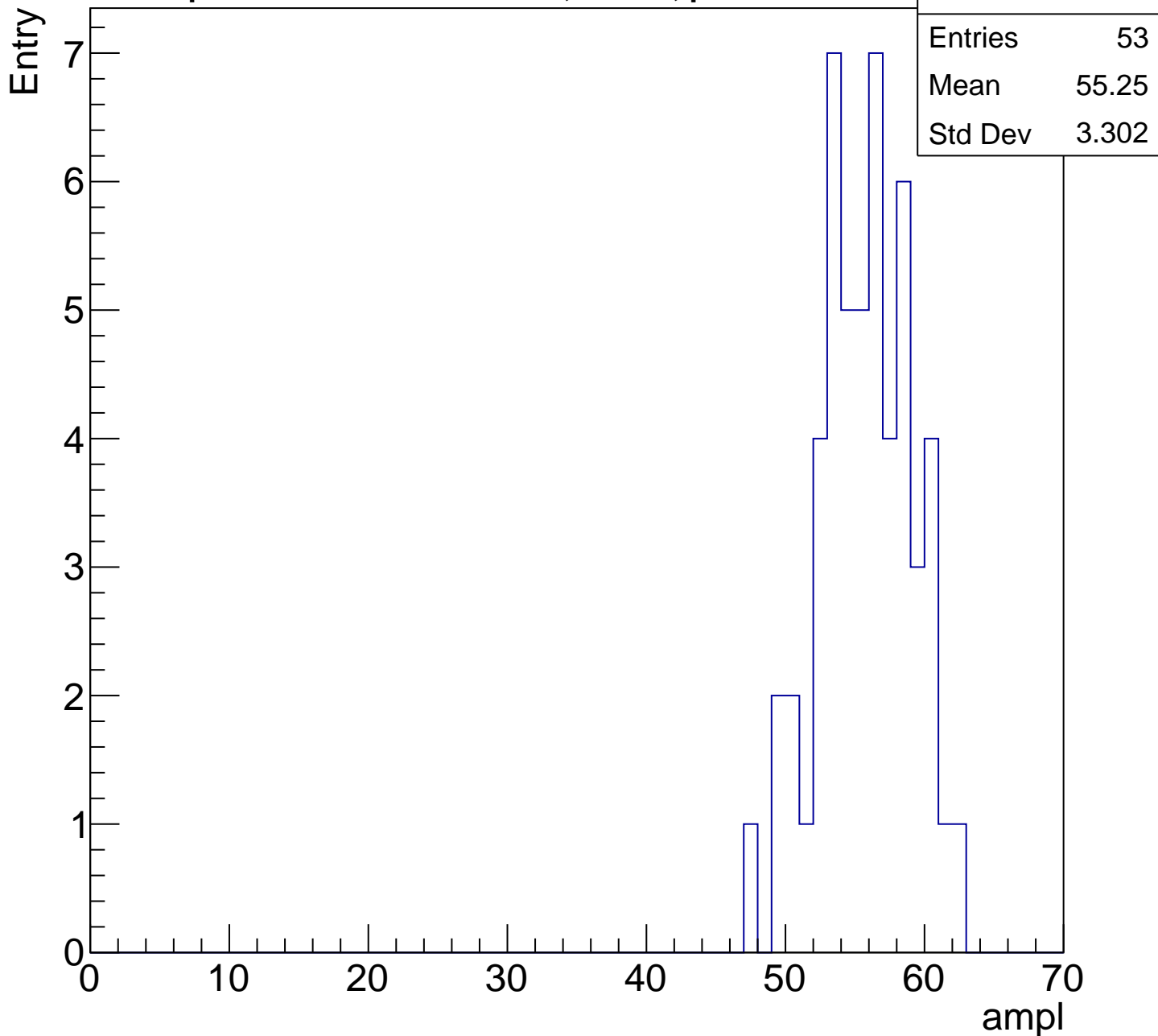
Entry

Entries	47
Mean	48.96
Std Dev	3.875



# B1L102S, U8-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

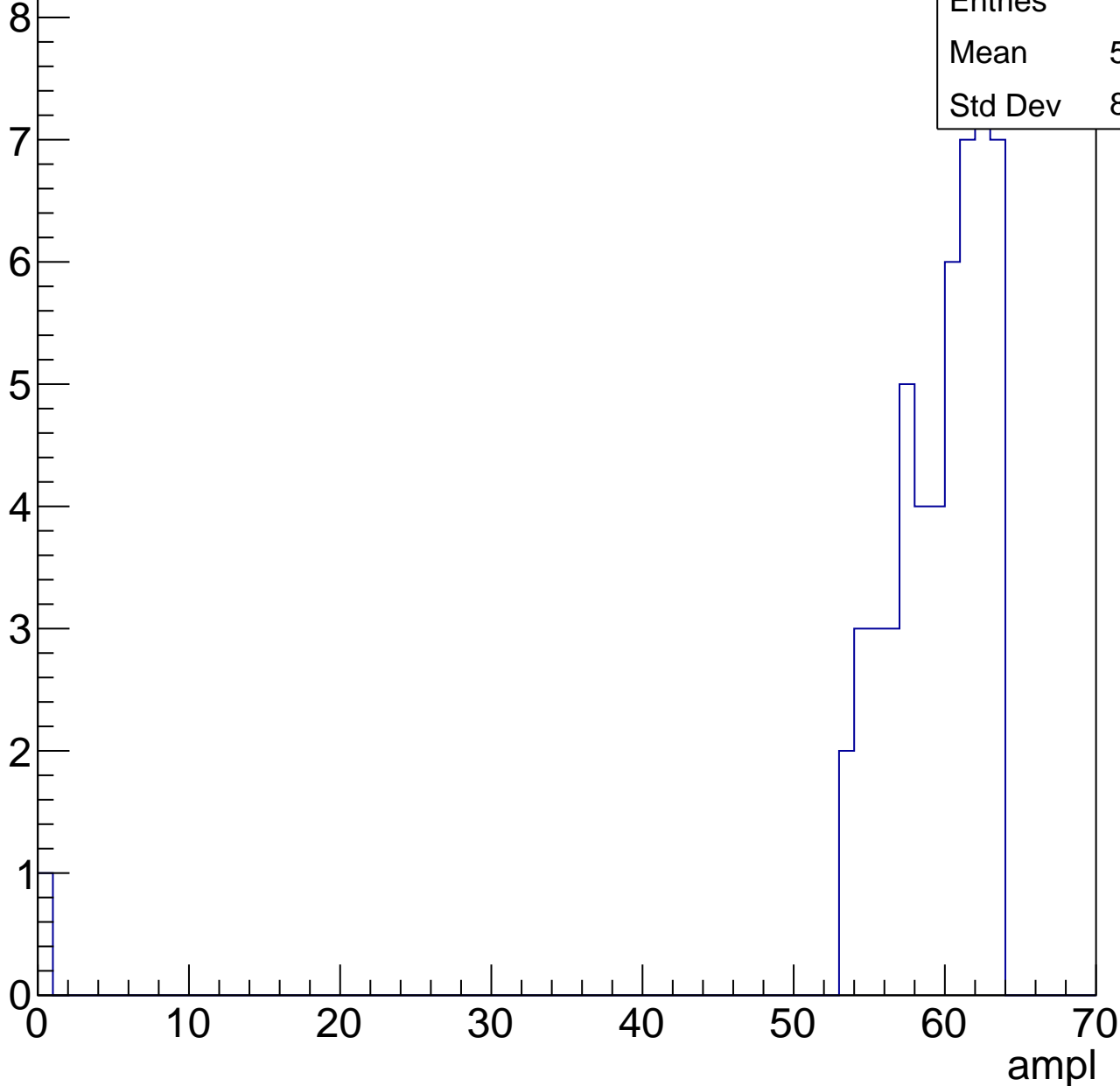


# B1L102S, U8-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	58.08
Std Dev	8.578



# B1L102S, U8-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries	9
Mean	61.11
Std Dev	1.663



# B1L102S, U8-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch37, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	71
Mean	28.49
Std Dev	4.062

**Gaus mean : 29.8322**

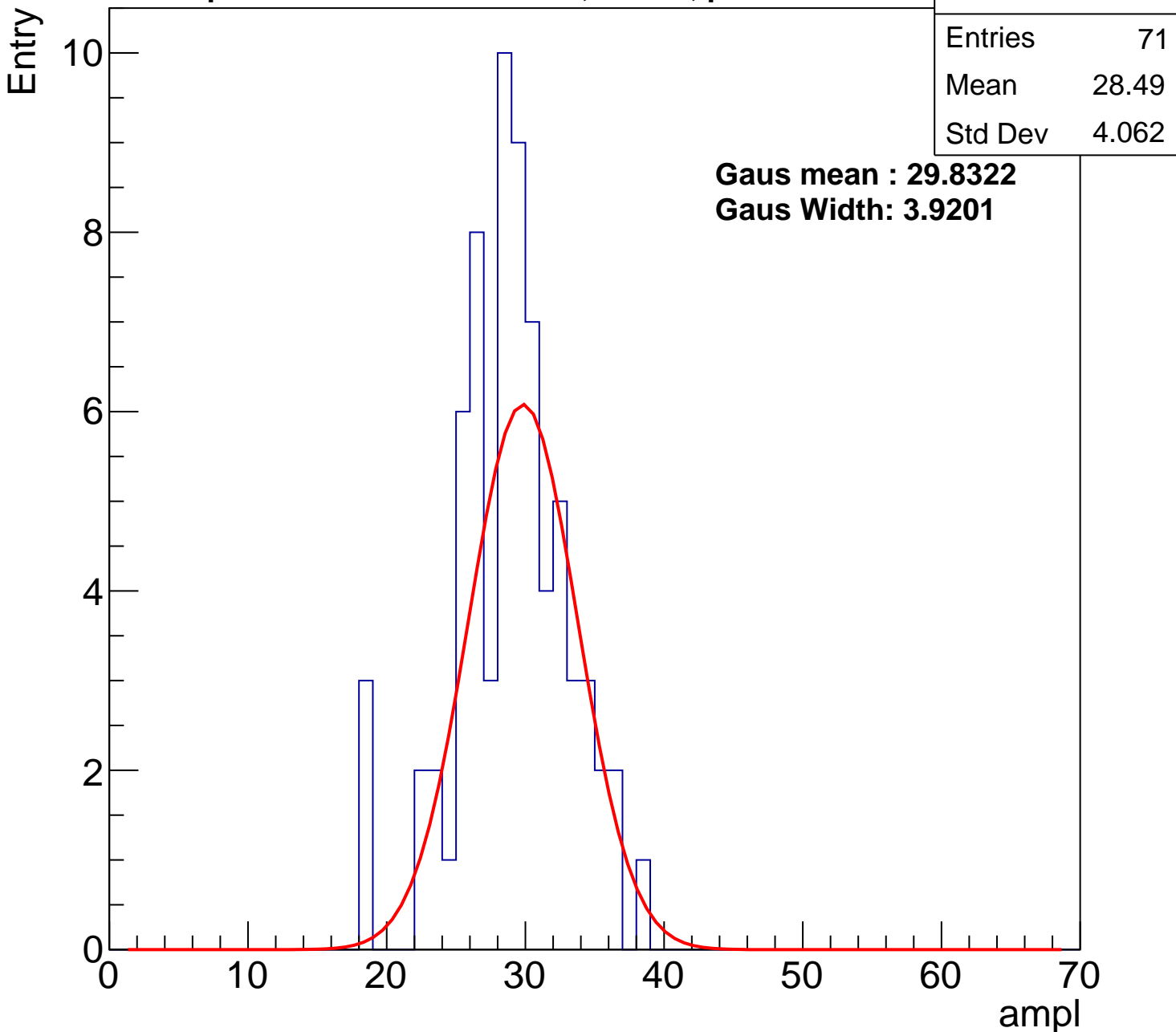
**Gaus Width: 3.9201**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U8-ch37, adc1

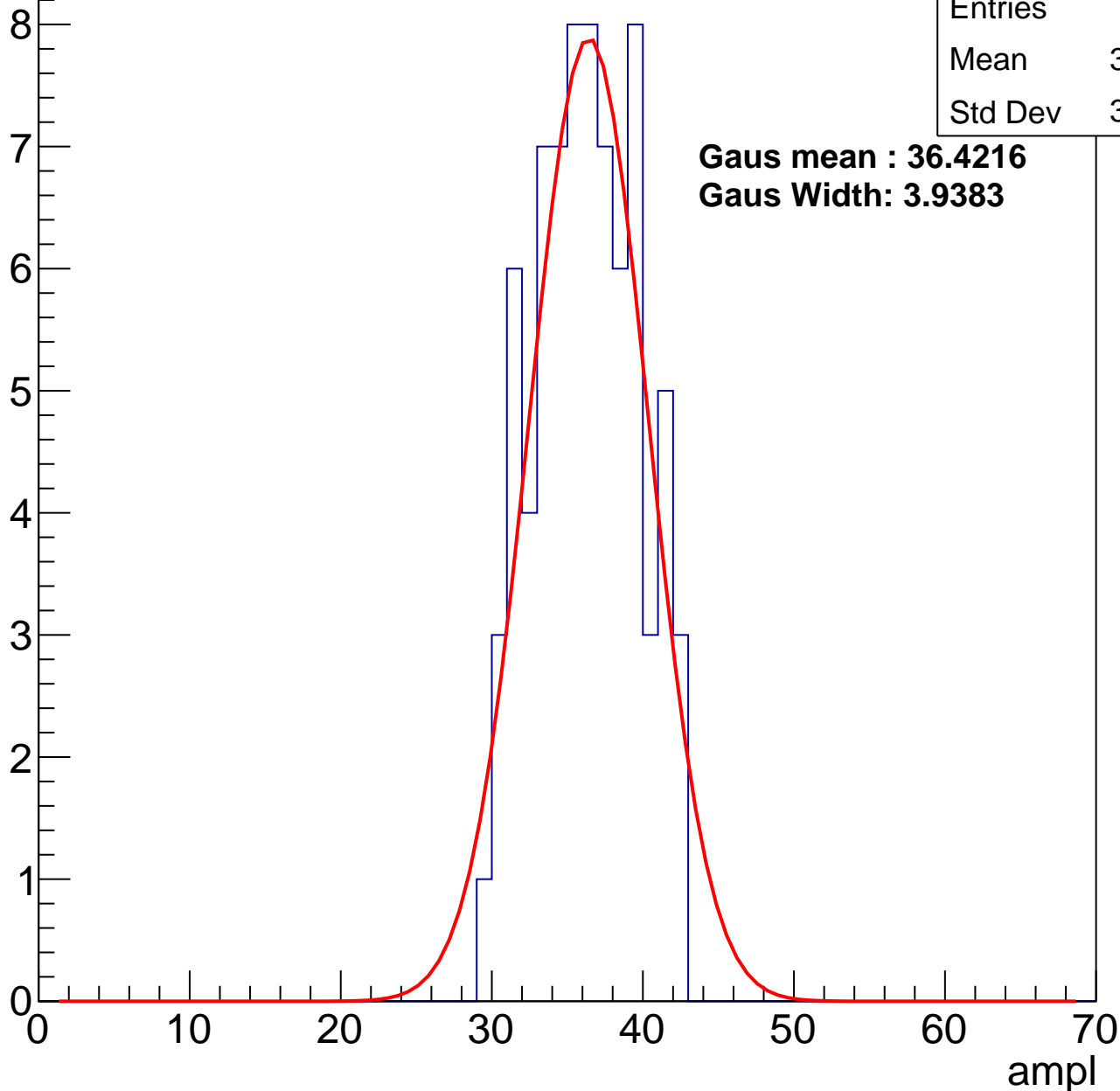
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	35.79
Std Dev	3.346

**Gaus mean : 36.4216**

**Gaus Width: 3.9383**



# B1L102S, U8-ch37, adc2

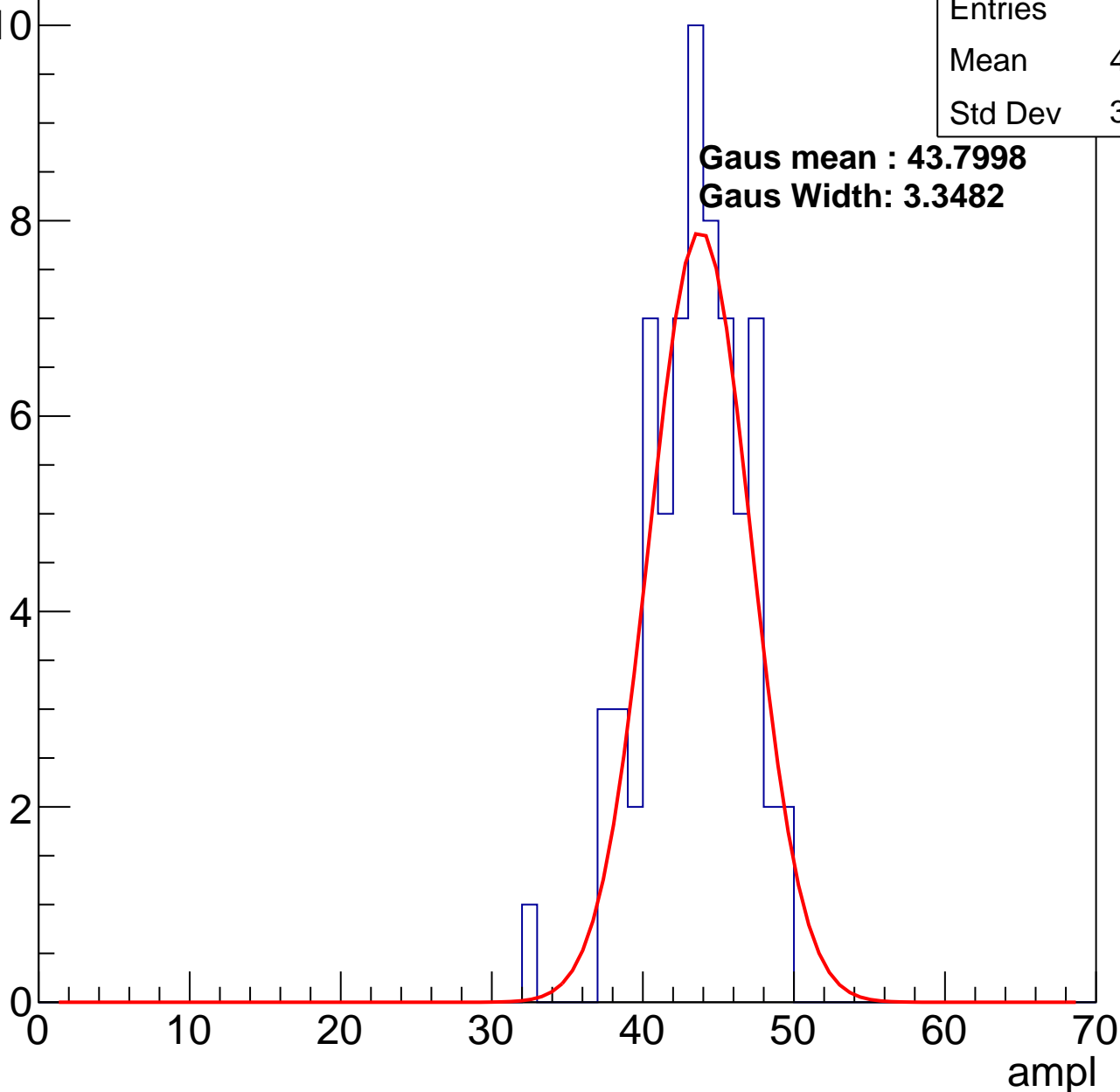
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	42.96
Std Dev	3.277

**Gaus mean : 43.7998**

**Gaus Width: 3.3482**

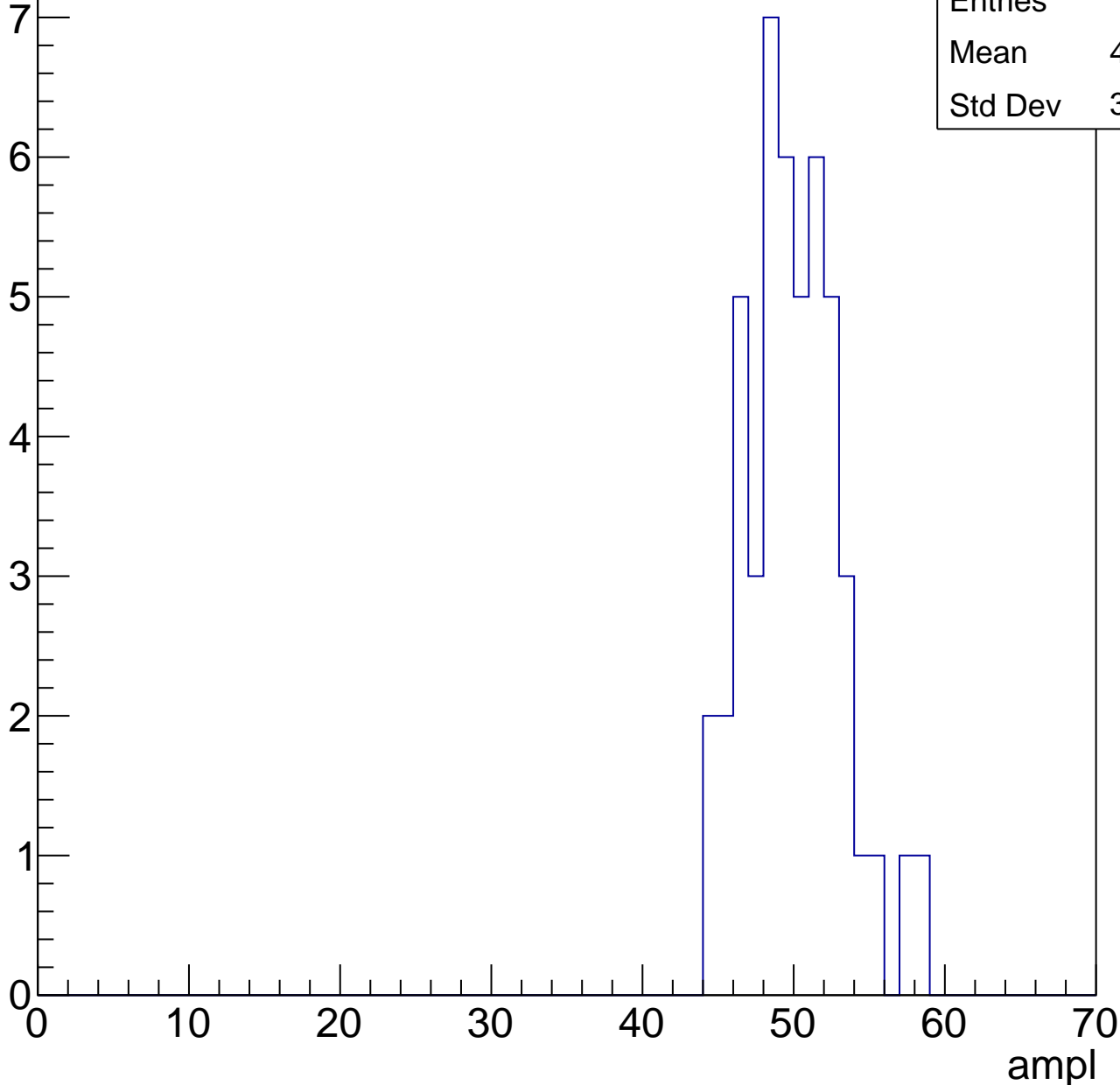


# B1L102S, U8-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

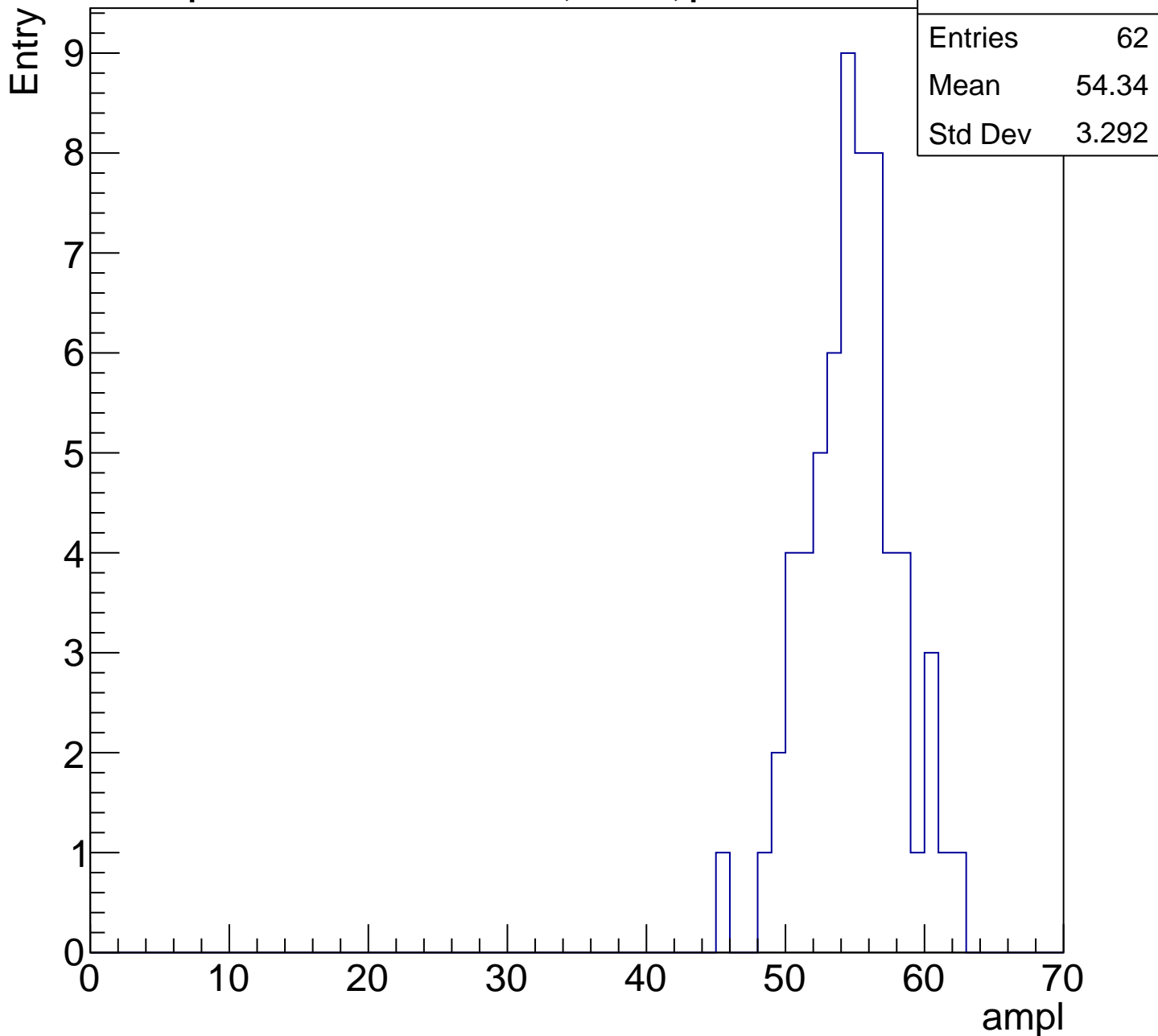
Entry

Entries	48
Mean	49.54
Std Dev	3.095



# B1L102S, U8-ch37, adc4

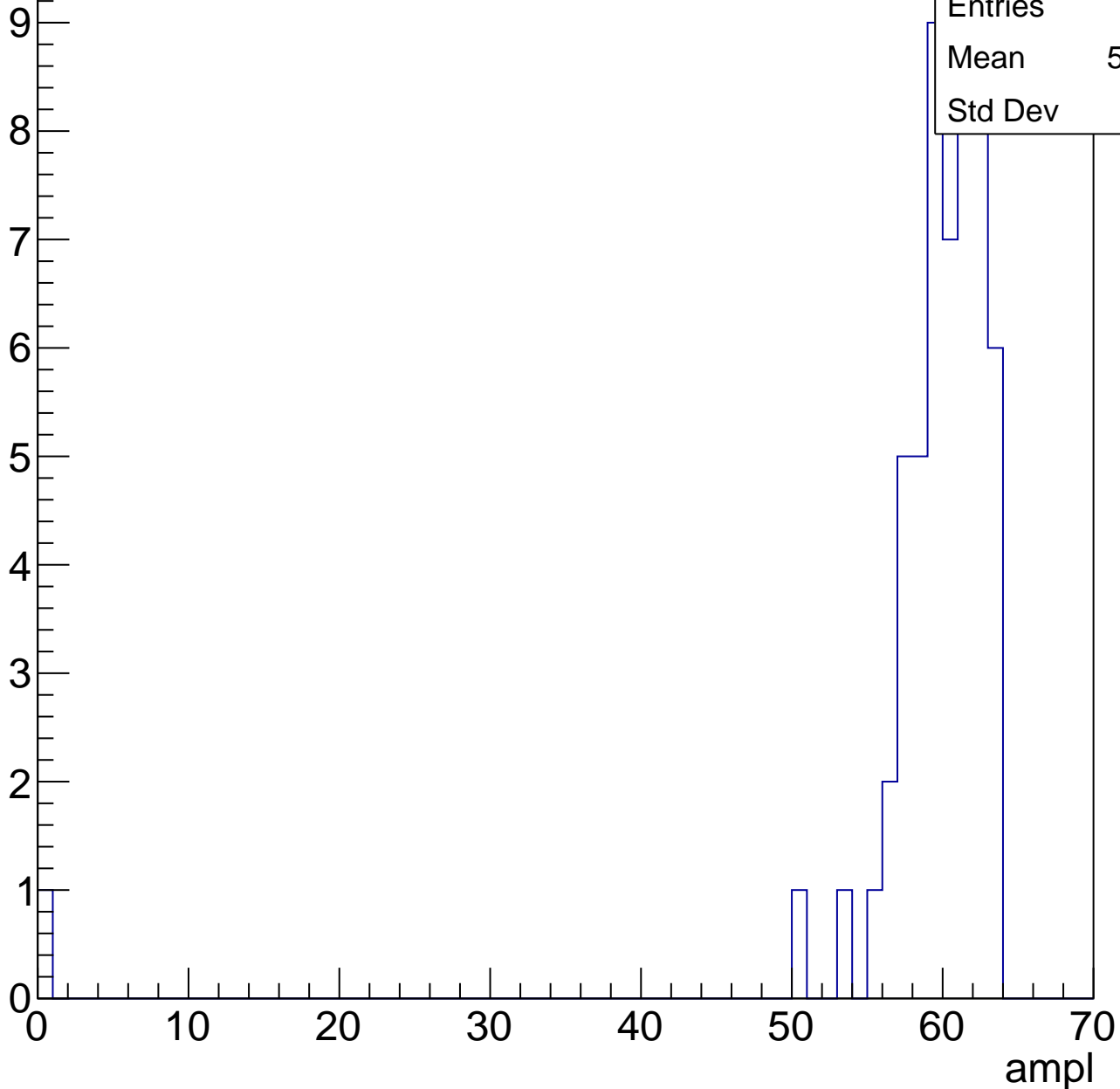
calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U8-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch38, adc0

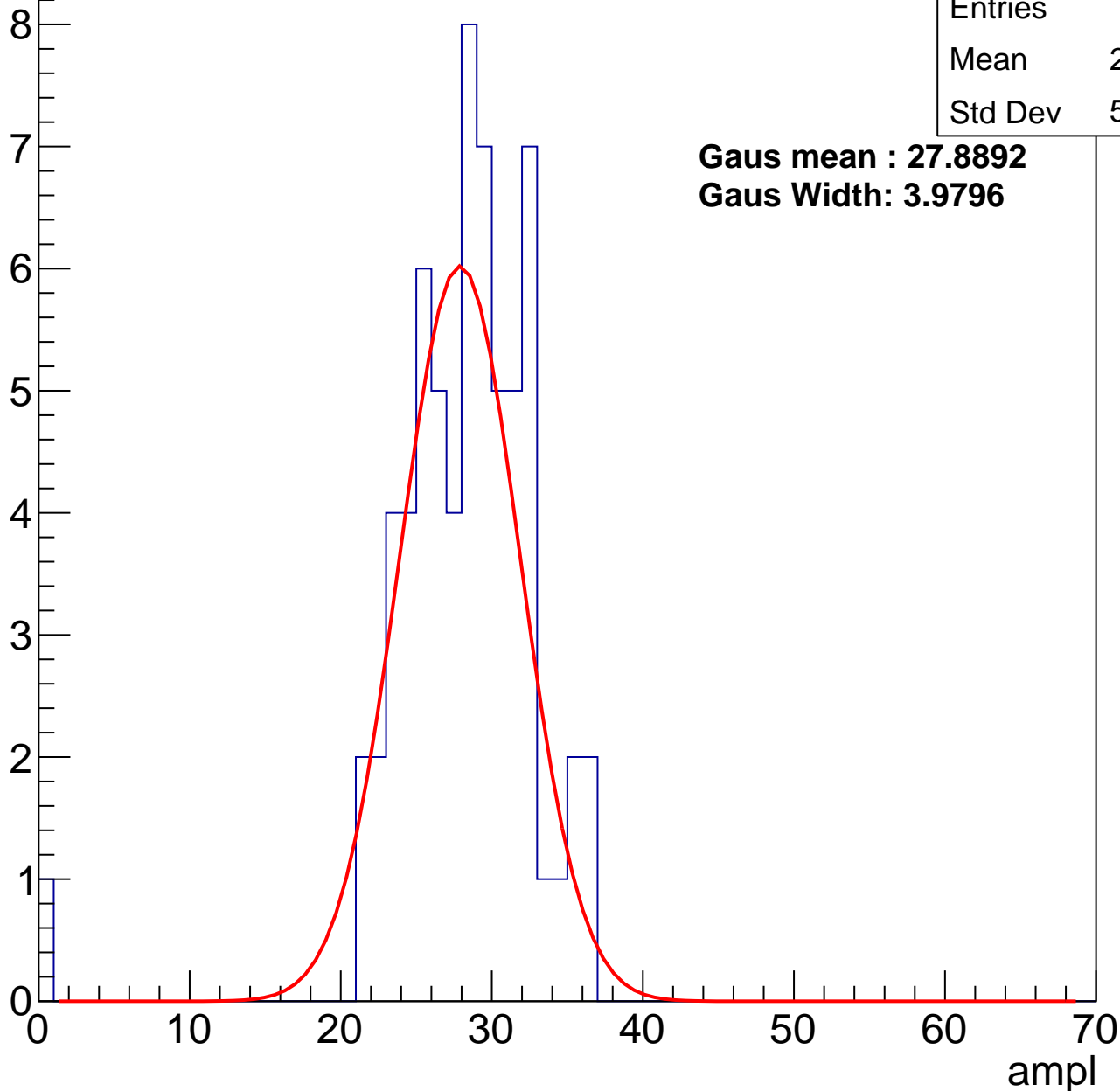
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	27.68
Std Dev	5.016

**Gaus mean : 27.8892**

**Gaus Width: 3.9796**



# B1L102S, U8-ch38, adc1

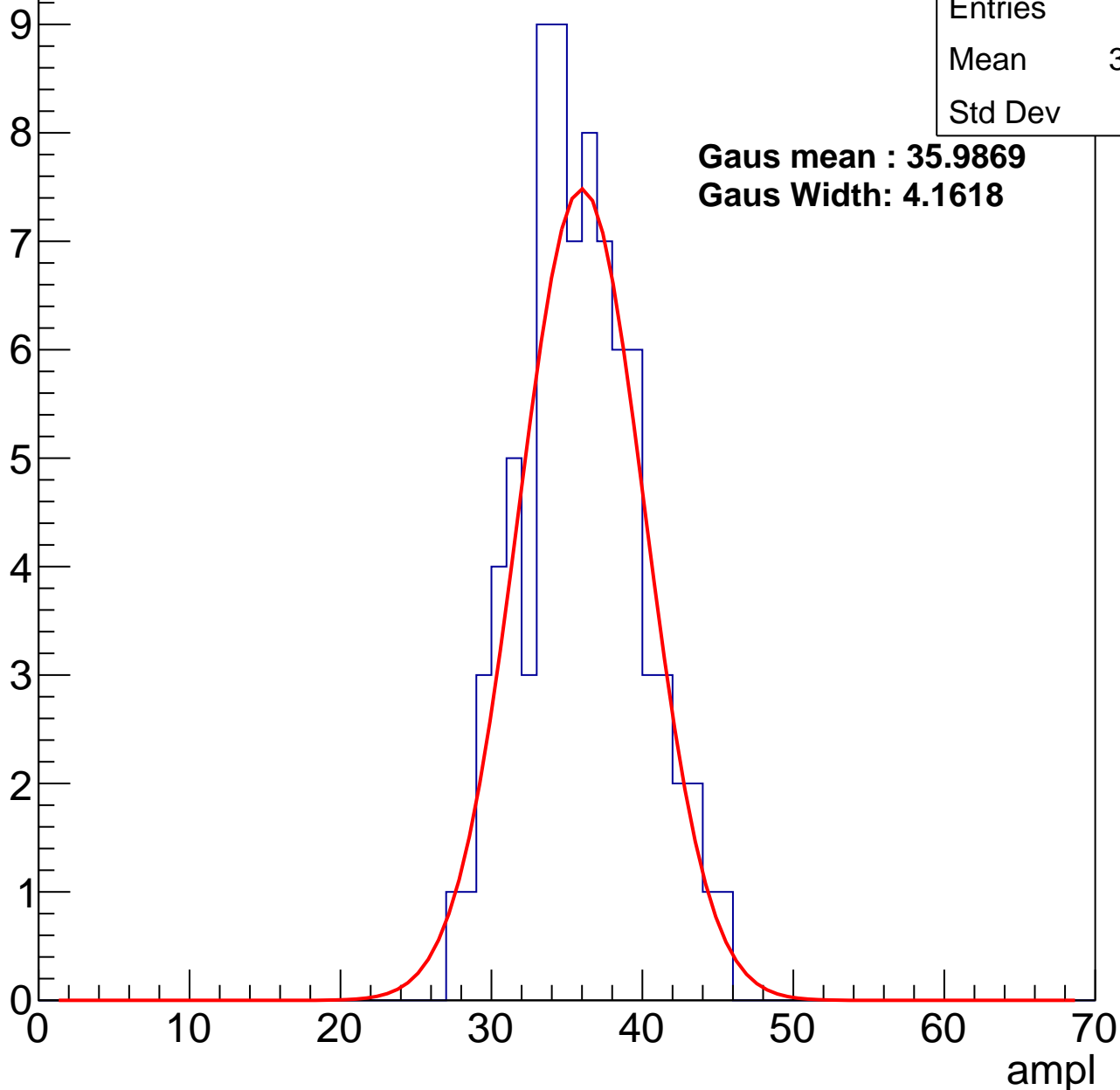
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	81
Mean	35.46
Std Dev	3.9

**Gaus mean : 35.9869**

**Gaus Width: 4.1618**



# B1L102S, U8-ch38, adc2

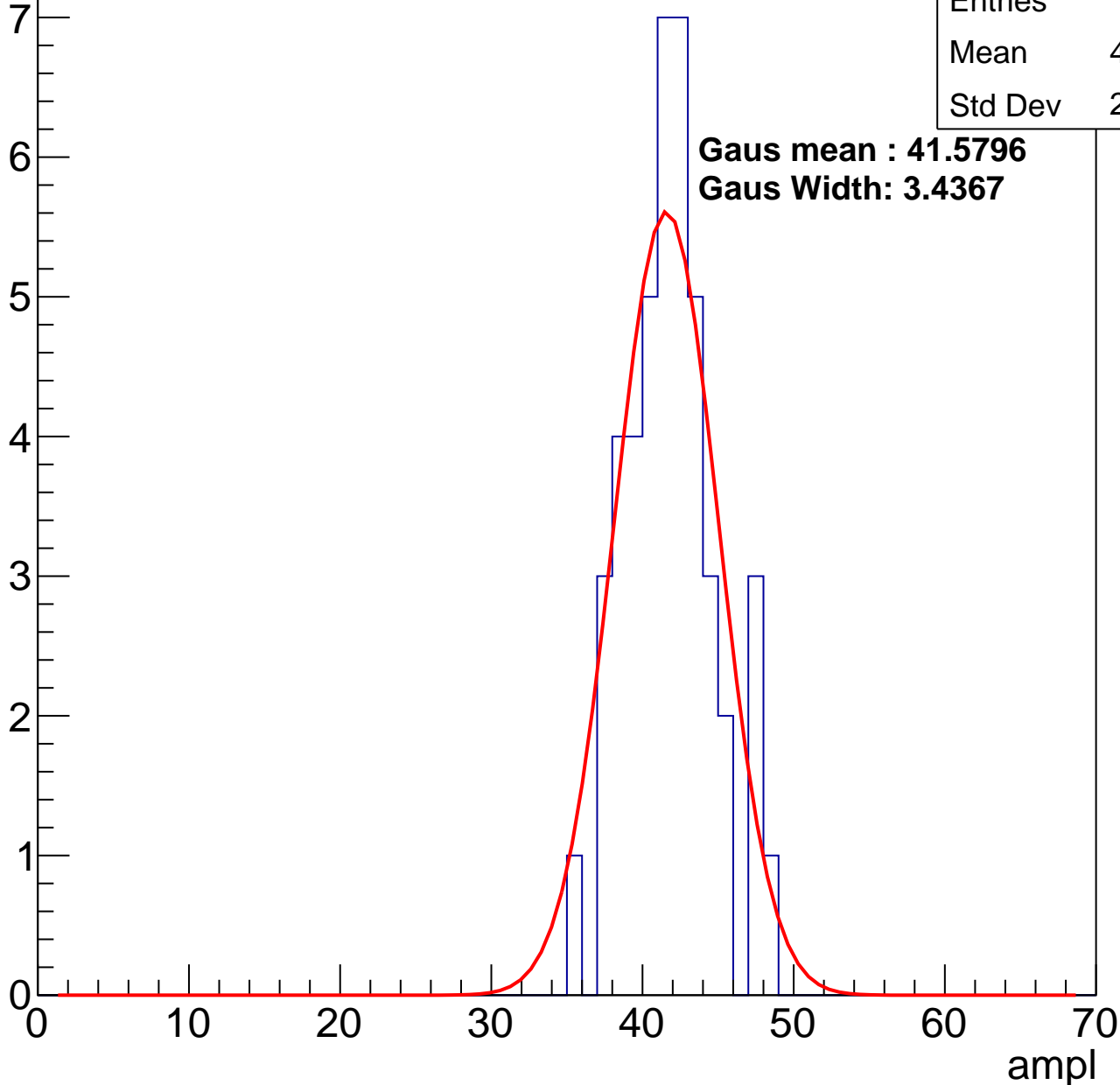
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	41.36
Std Dev	2.899

**Gaus mean : 41.5796**

**Gaus Width: 3.4367**

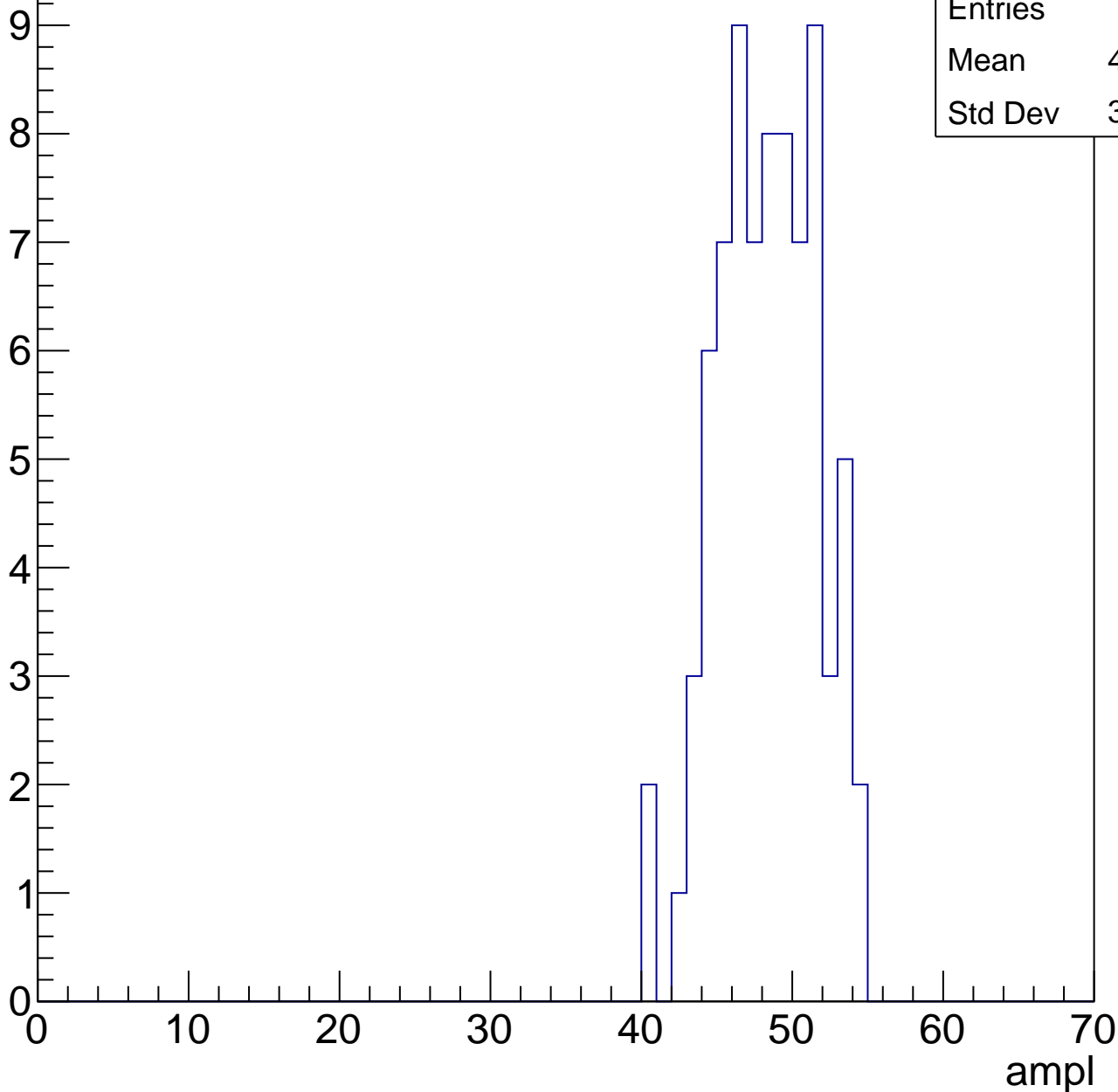


# B1L102S, U8-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	47.88
Std Dev	3.227

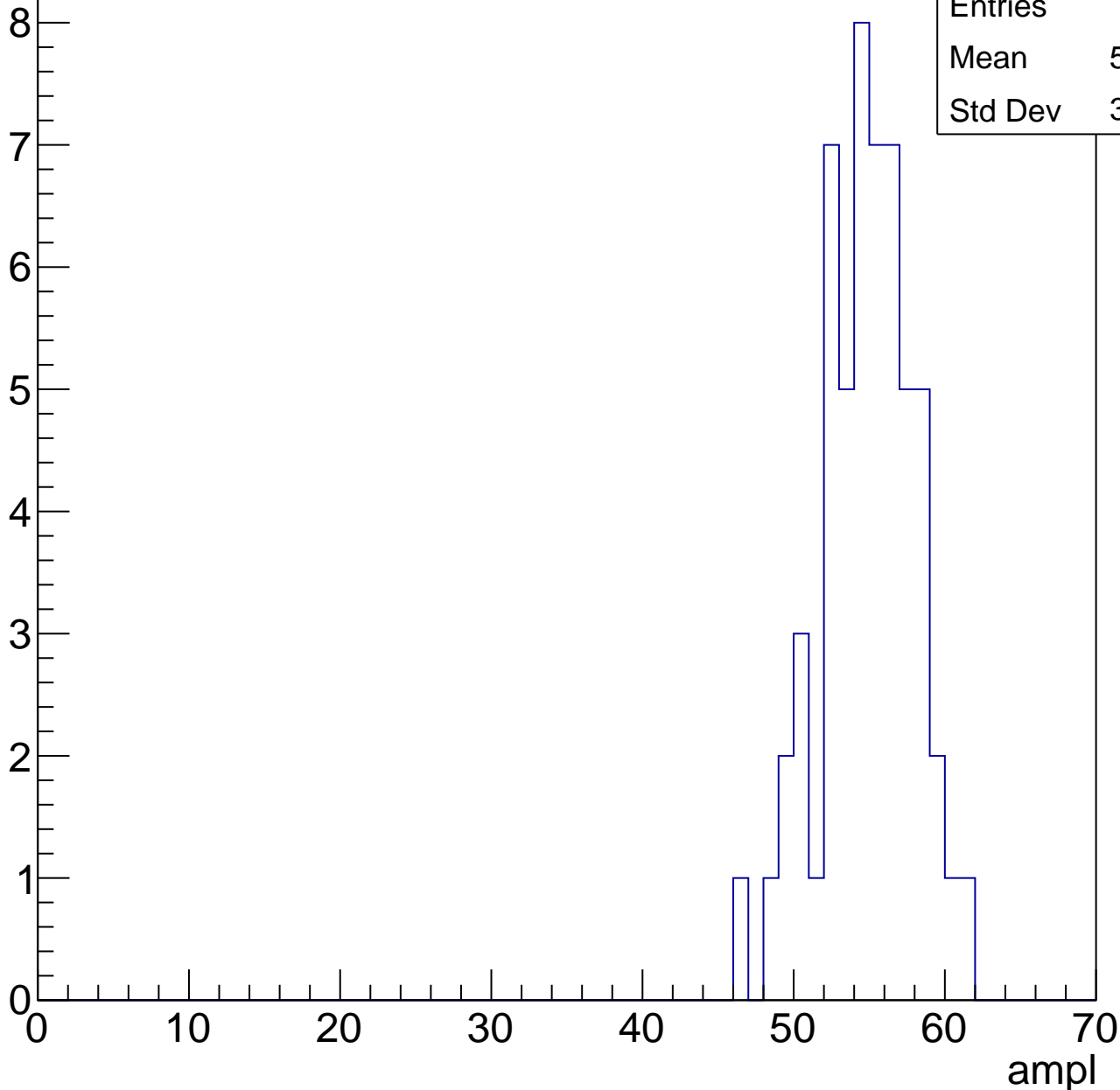


# B1L102S, U8-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

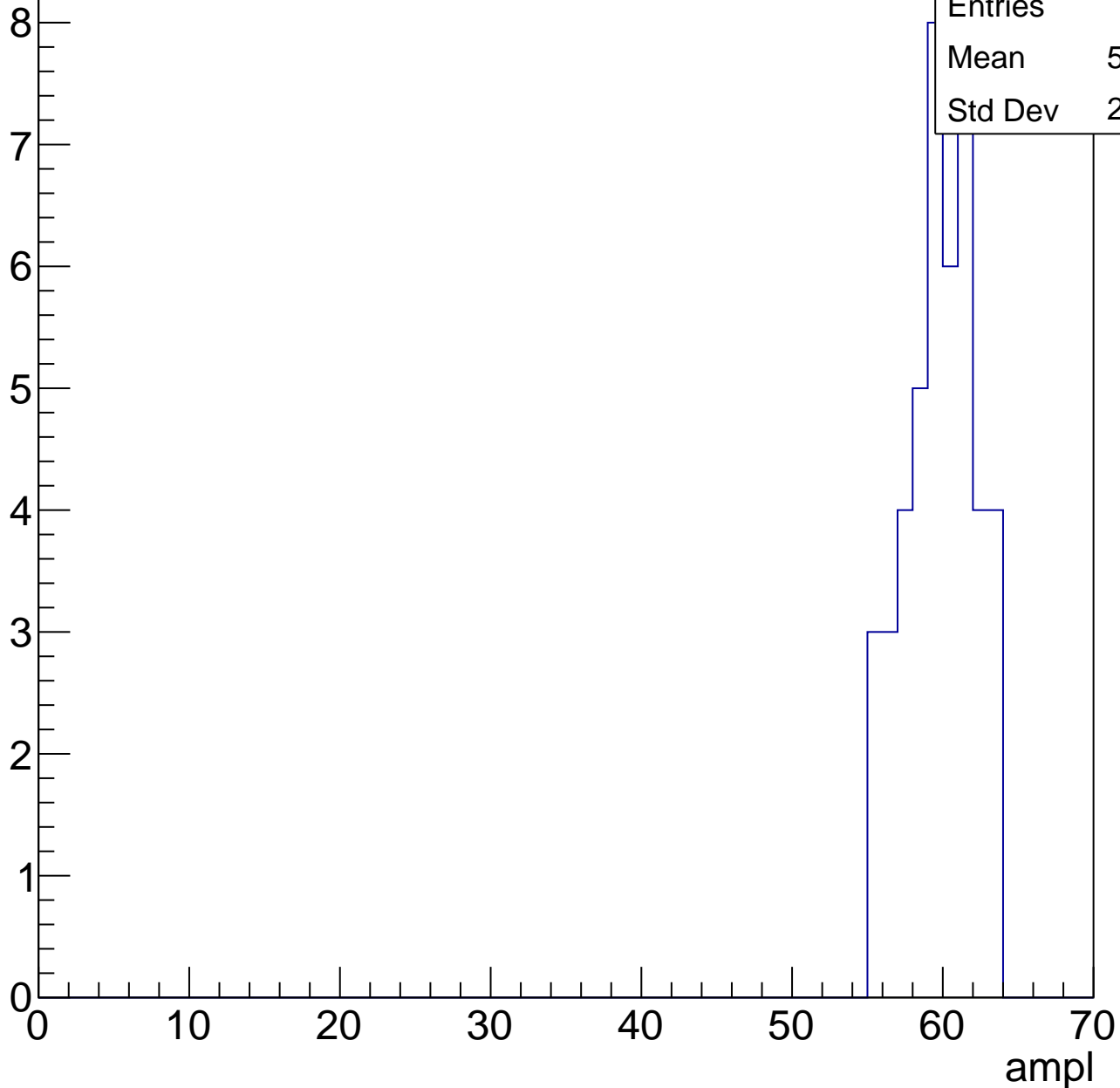
Entries	56
Mean	54.38
Std Dev	3.068



# B1L102S, U8-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



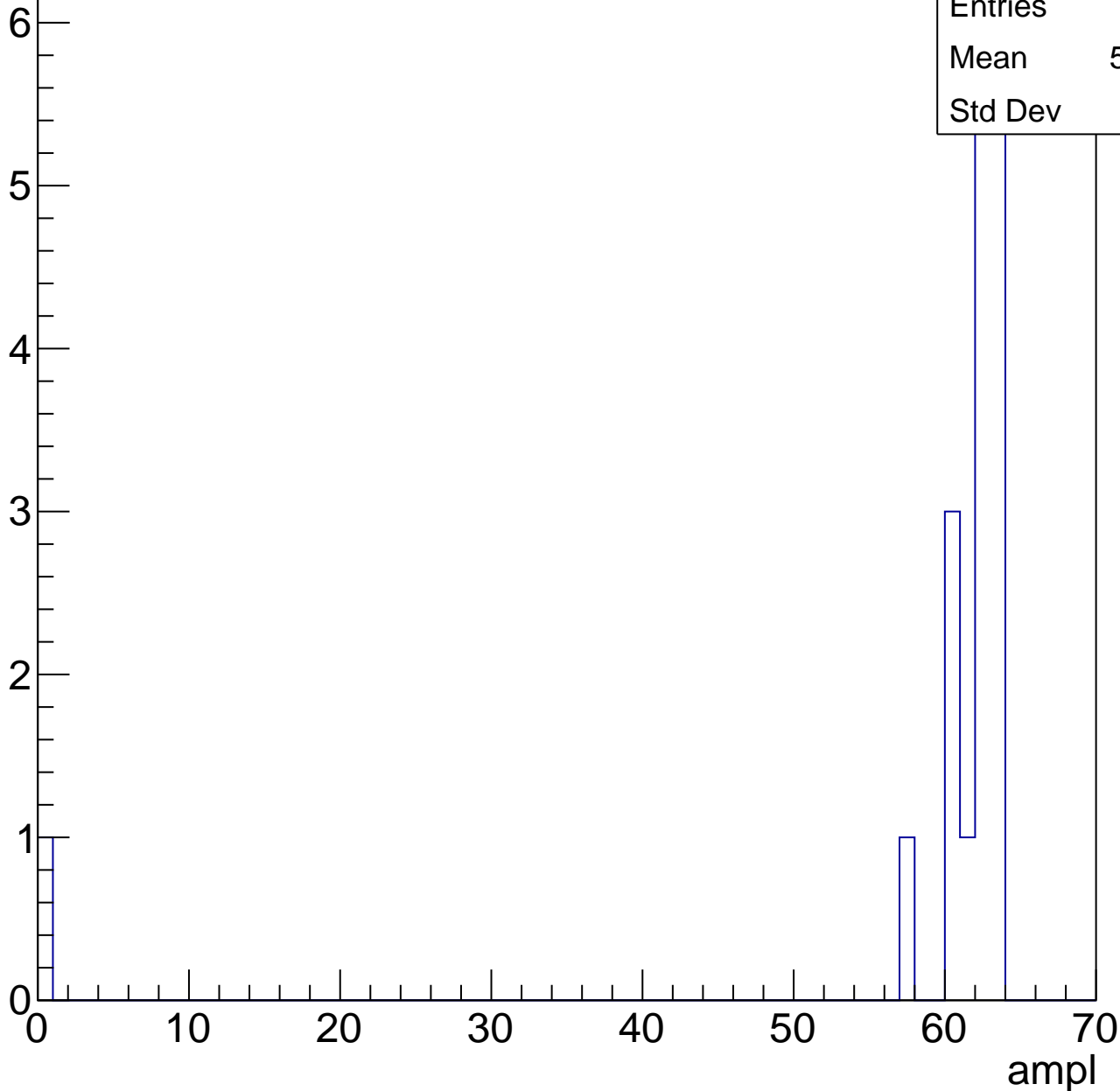
Entries	45
Mean	59.36
Std Dev	2.252

# B1L102S, U8-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	18
Mean	58.22
Std Dev	14.2





# B1L102S, U8-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch39, adc0

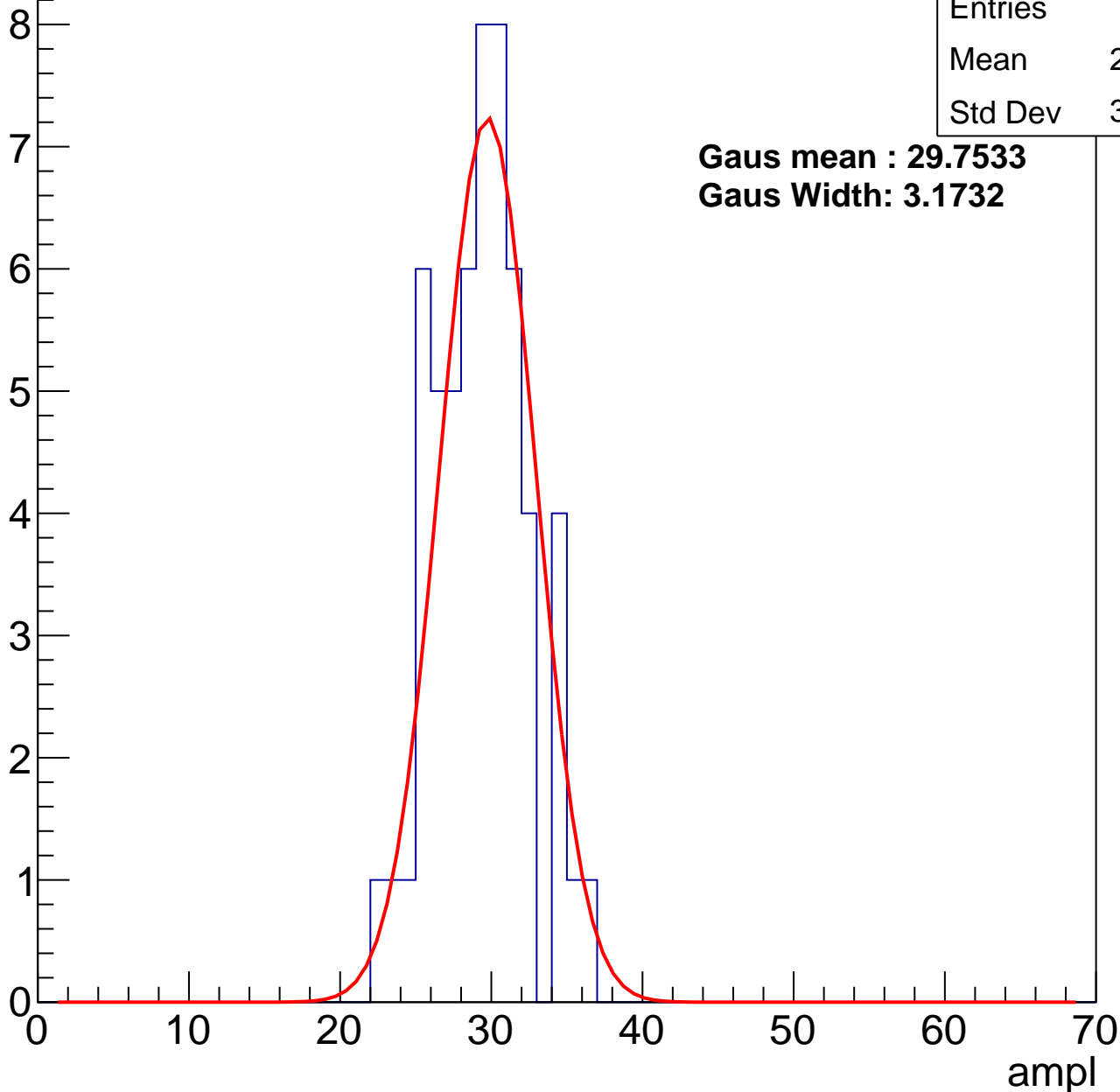
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	28.86
Std Dev	3.046

**Gaus mean : 29.7533**

**Gaus Width: 3.1732**

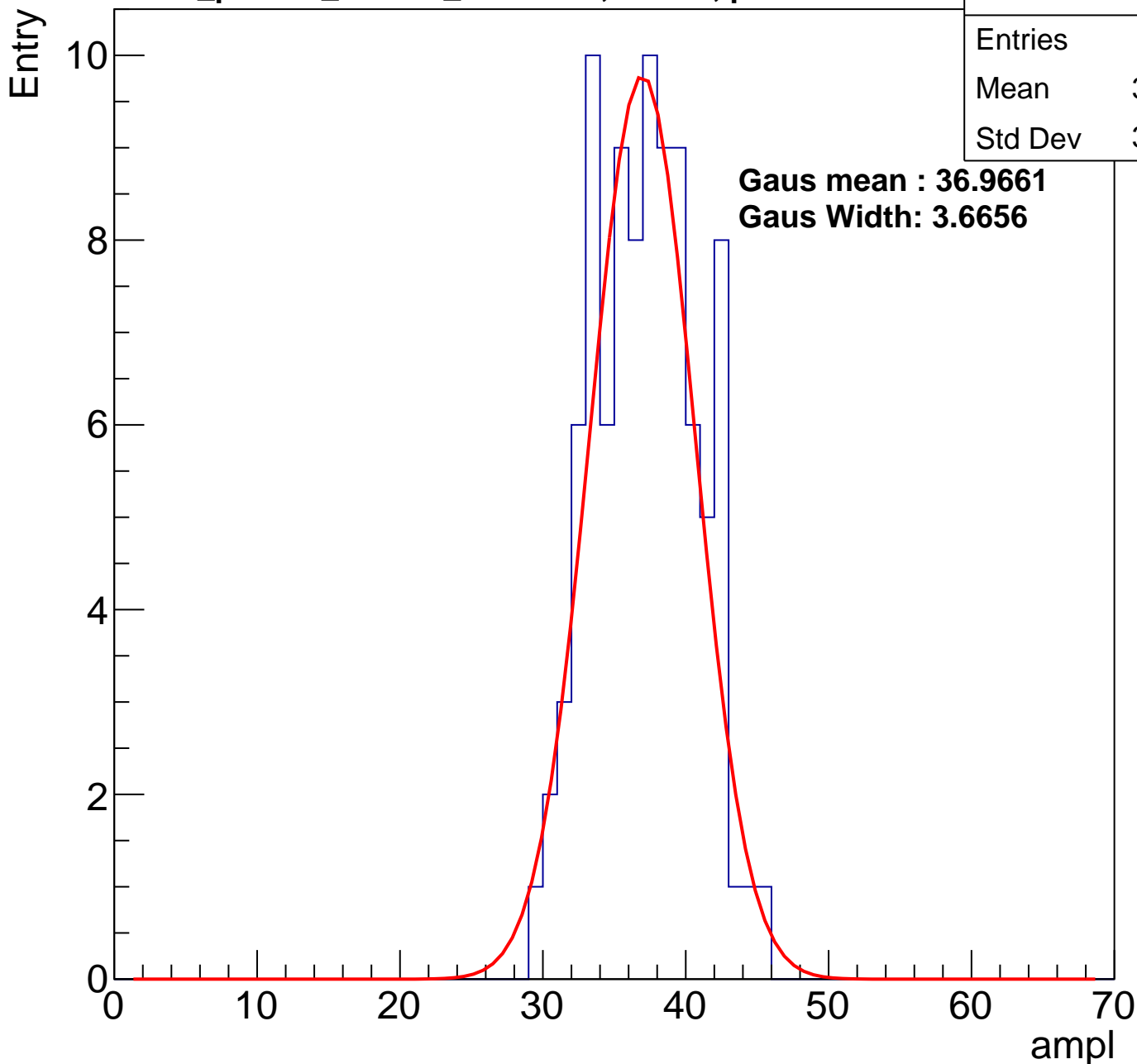


# B1L102S, U8-ch39, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	95
Mean	36.71
Std Dev	3.551

**Gaus mean : 36.9661**  
**Gaus Width: 3.6656**



# B1L102S, U8-ch39, adc2

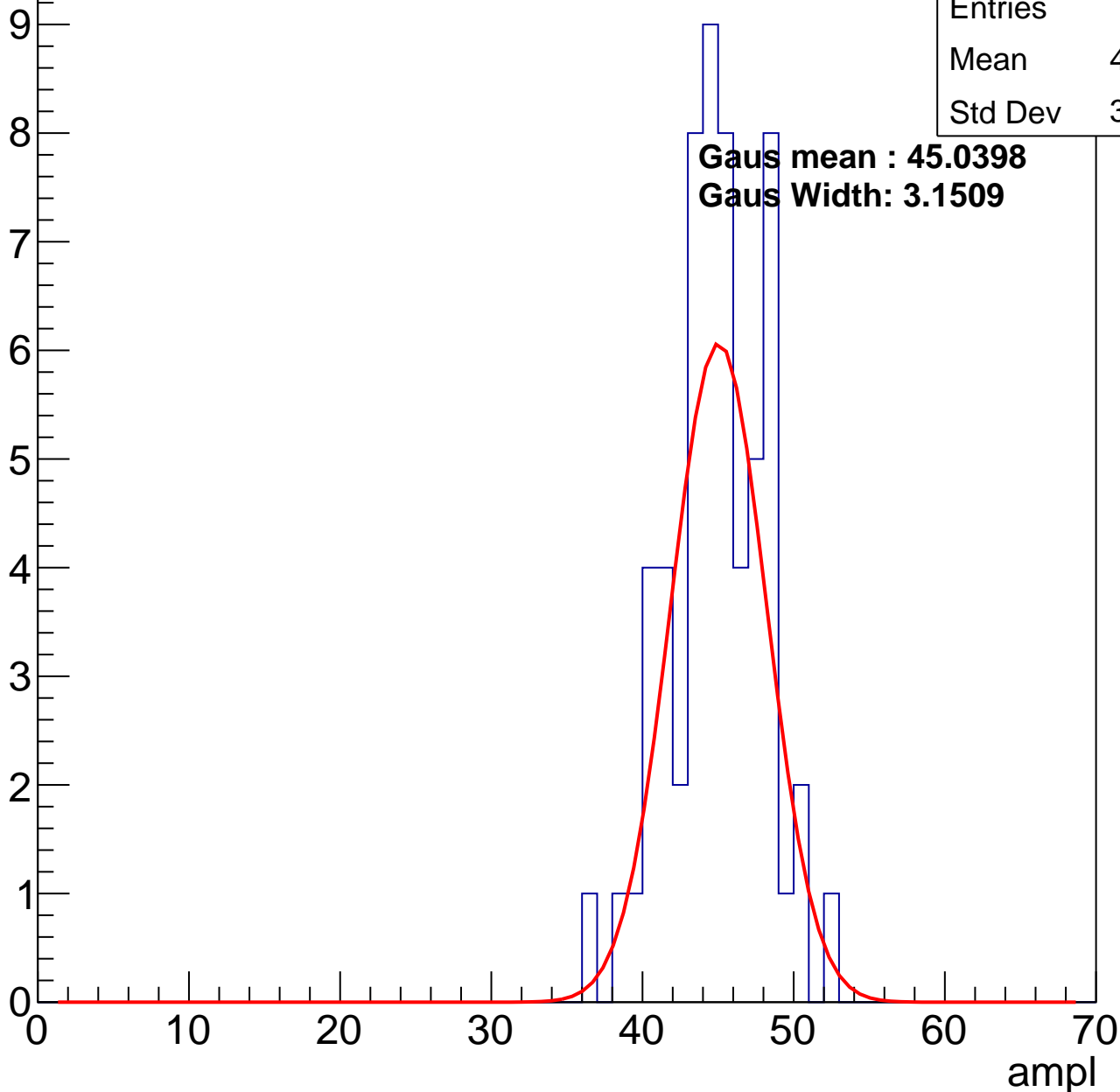
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	44.49
Std Dev	3.148

**Gaus mean : 45.0398**

**Gaus Width: 3.1509**

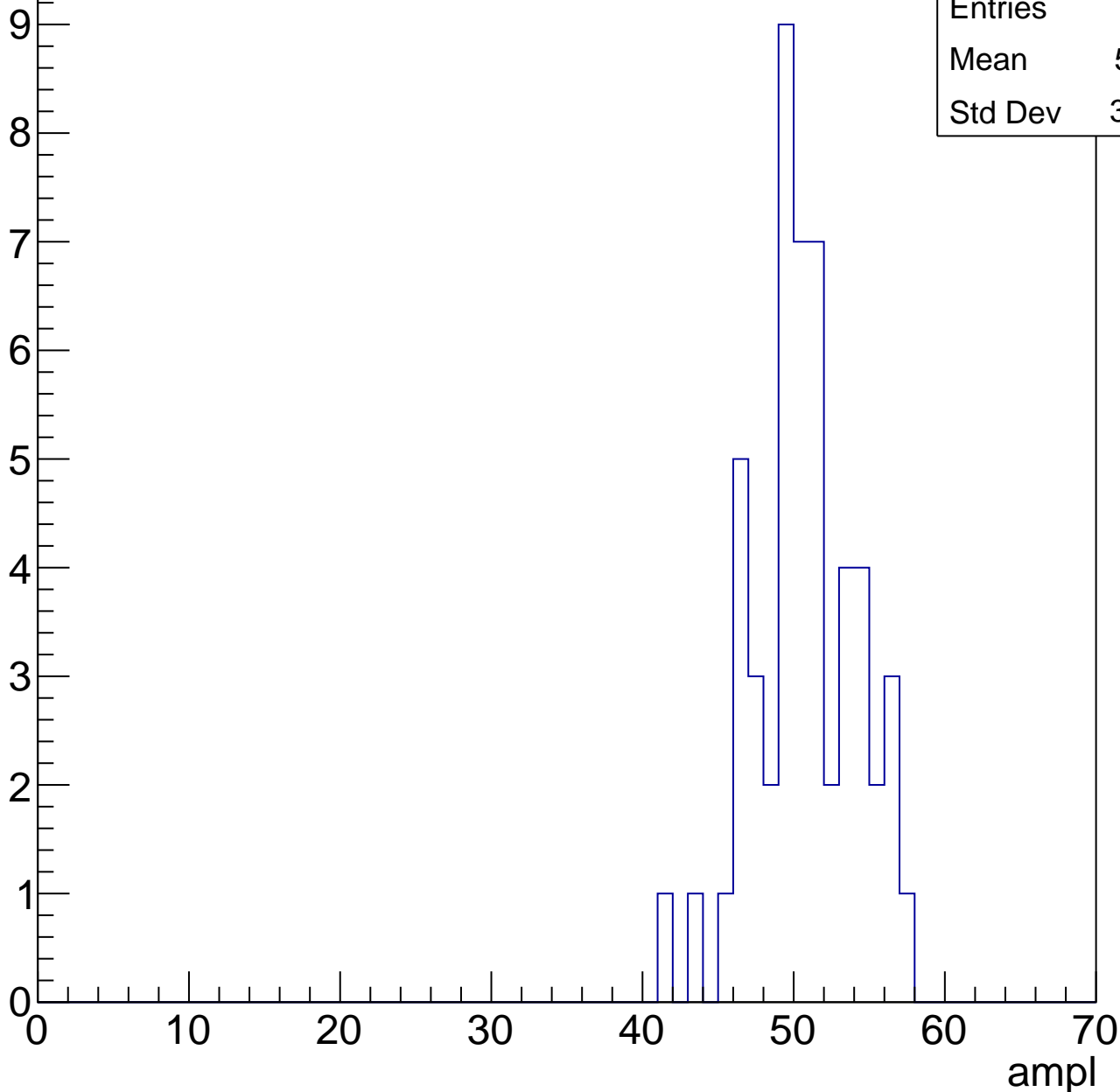


# B1L102S, U8-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	50.21
Std Dev	3.393

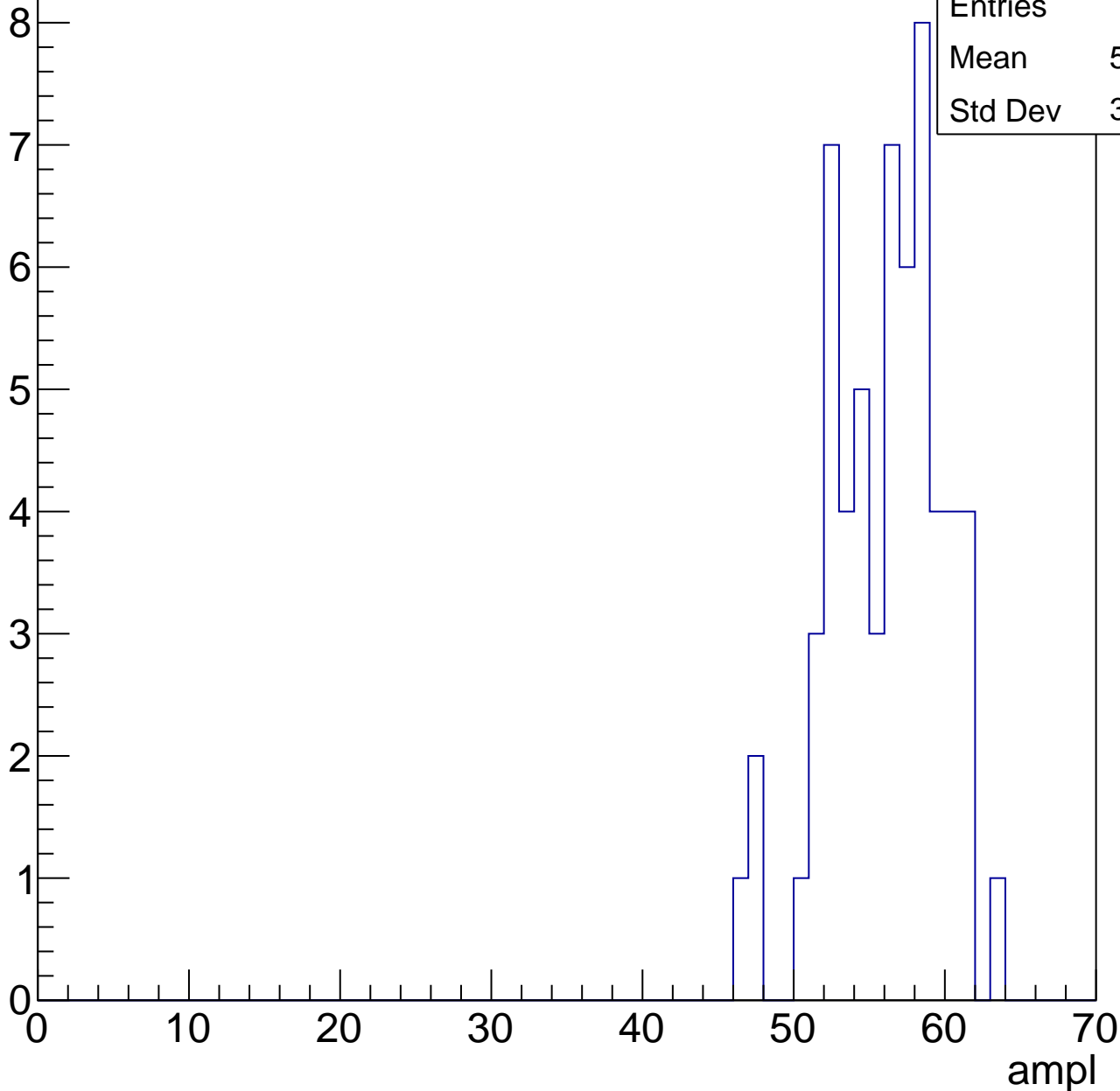


# B1L102S, U8-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	55.58
Std Dev	3.698

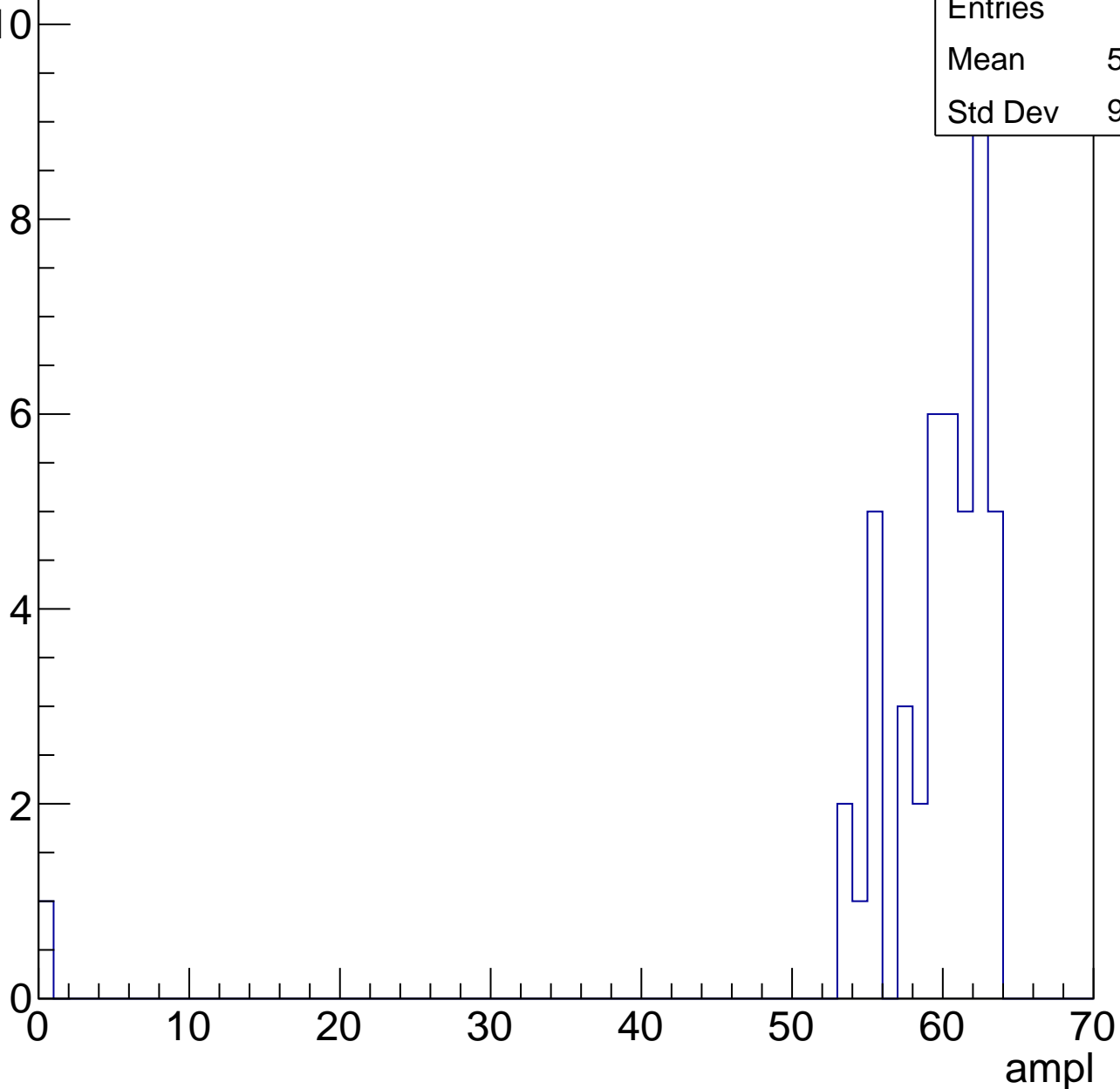


# B1L102S, U8-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

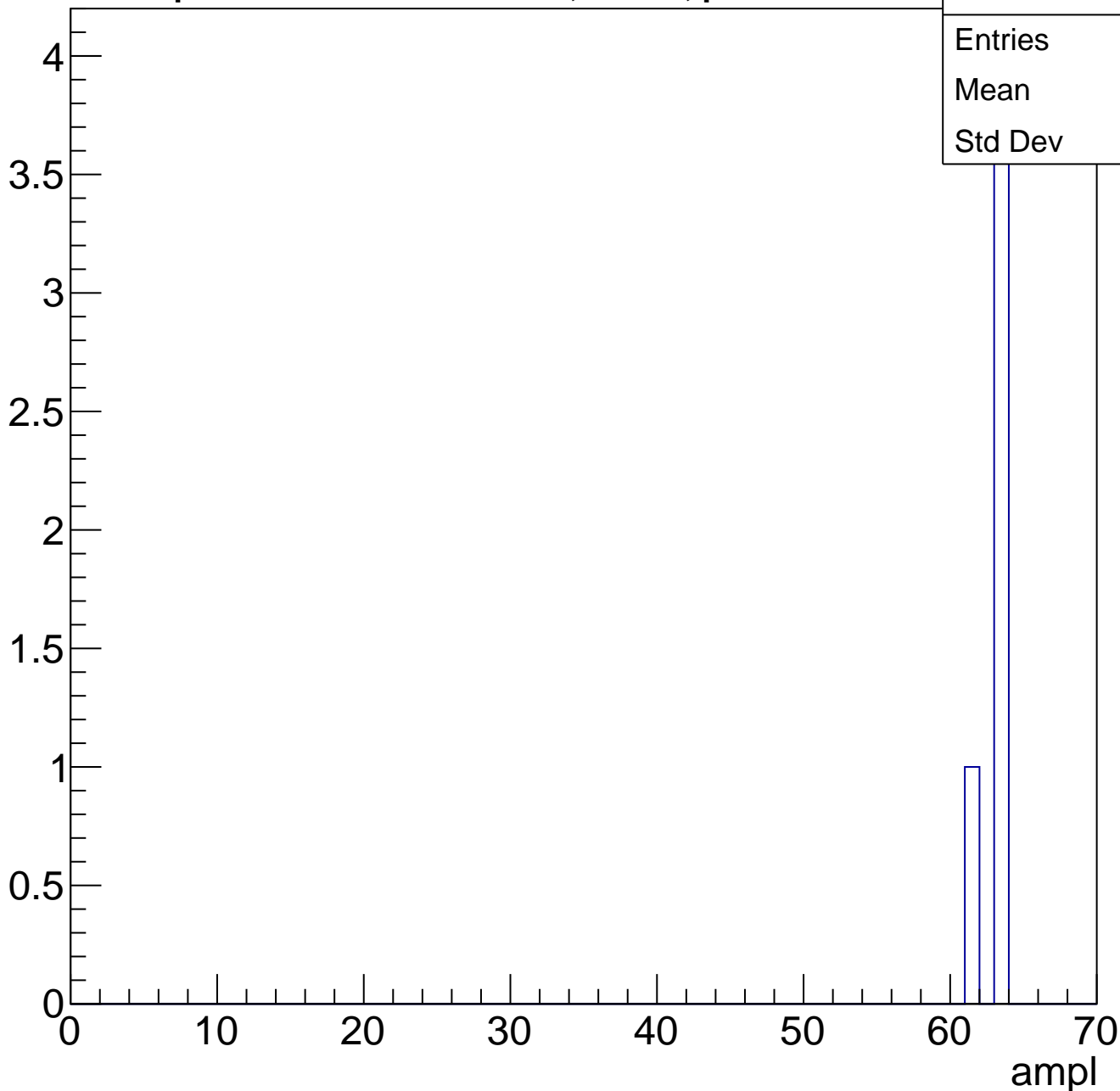
Entries	46
Mean	58.17
Std Dev	9.133



# B1L102S, U8-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch40, adc0

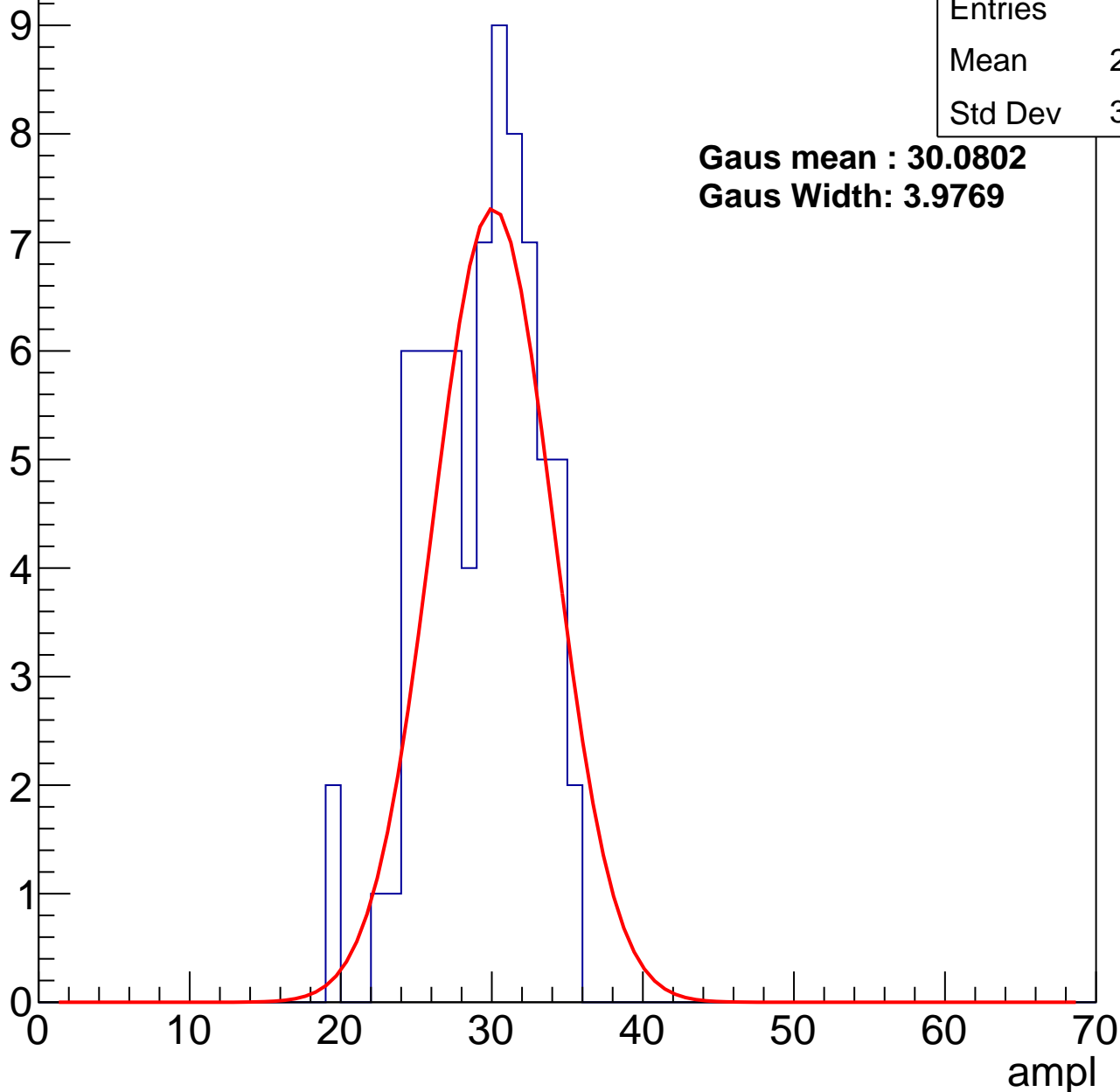
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	28.76
Std Dev	3.633

**Gaus mean : 30.0802**

**Gaus Width: 3.9769**



# B1L102S, U8-ch40, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	52
Mean	35.69
Std Dev	2.978

**Gaus mean : 35.9928**

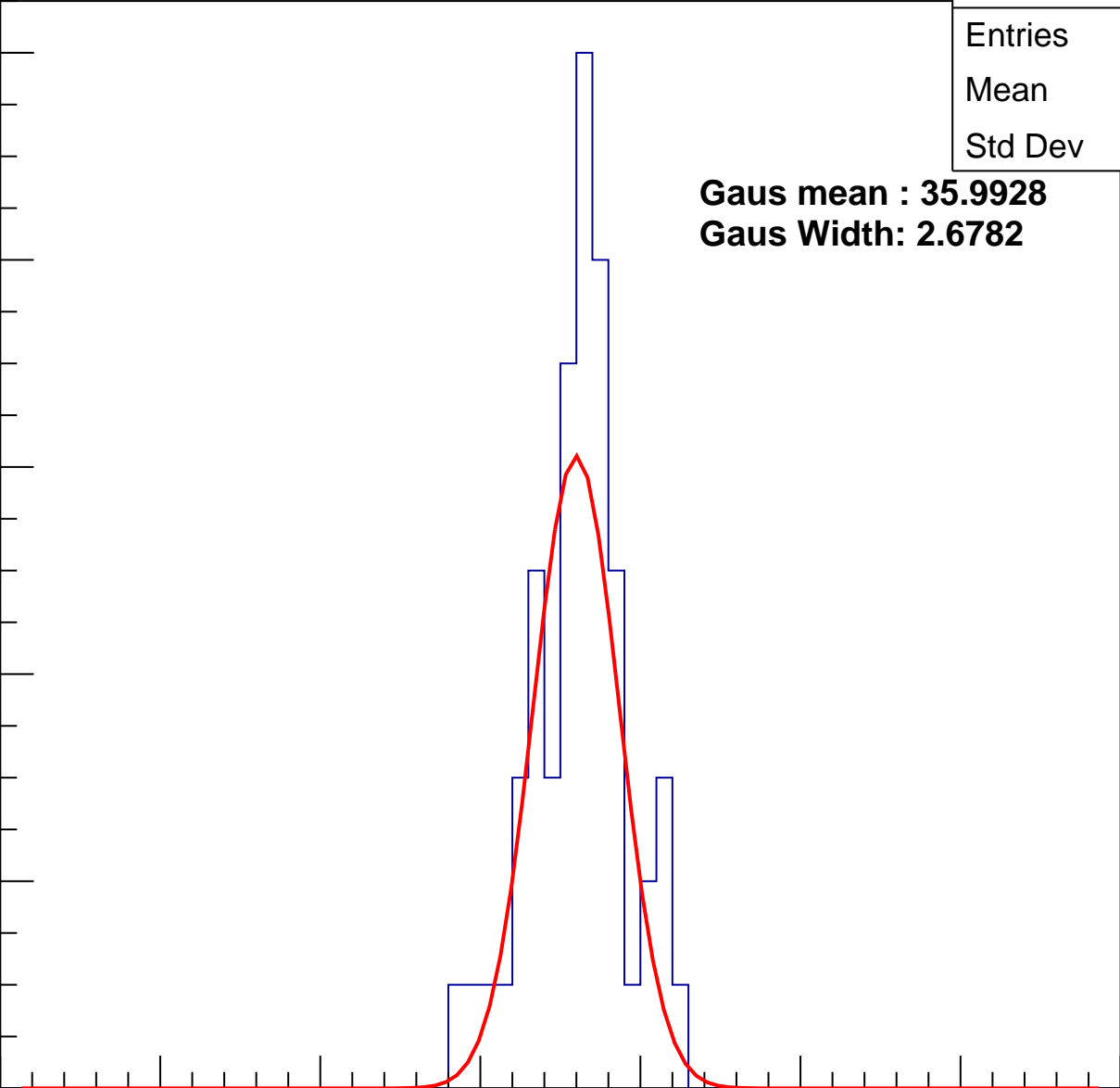
**Gaus Width: 2.6782**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U8-ch40, adc2

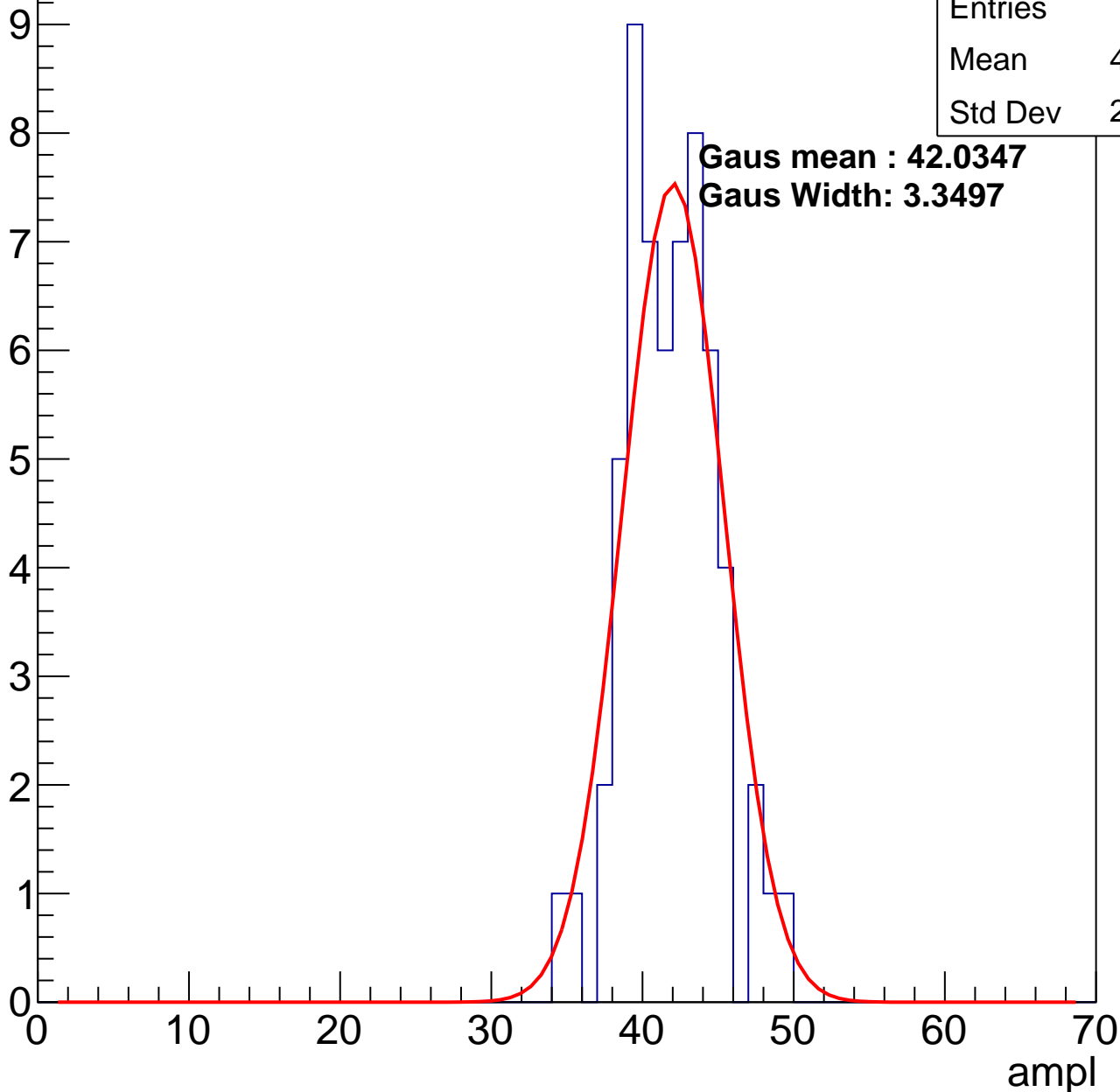
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	41.38
Std Dev	2.995

**Gaus mean : 42.0347**

**Gaus Width: 3.3497**



# B1L102S, U8-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

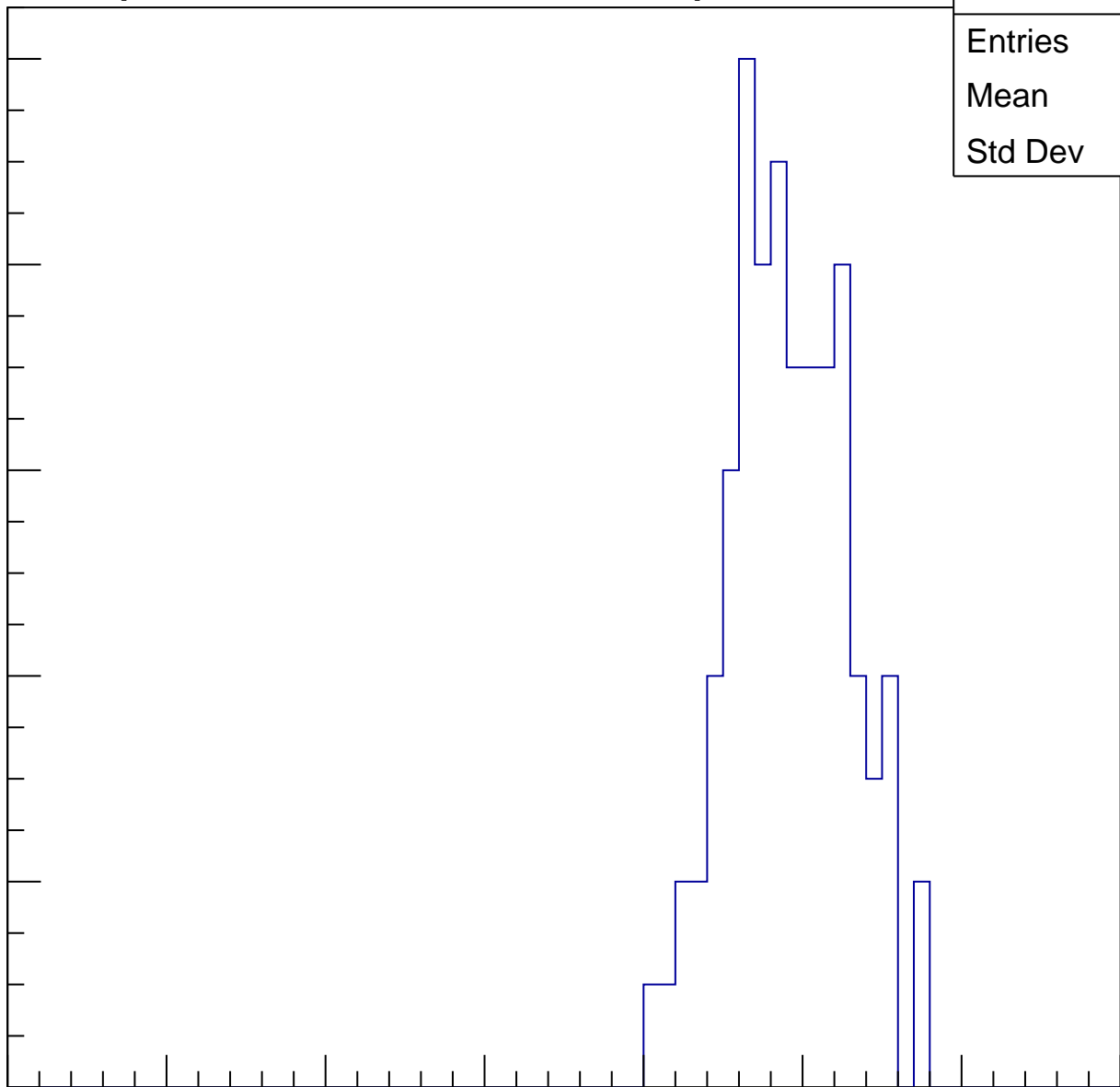
Entry

10  
8  
6  
4  
2  
0

Entries	85
Mean	48.69
Std Dev	3.682

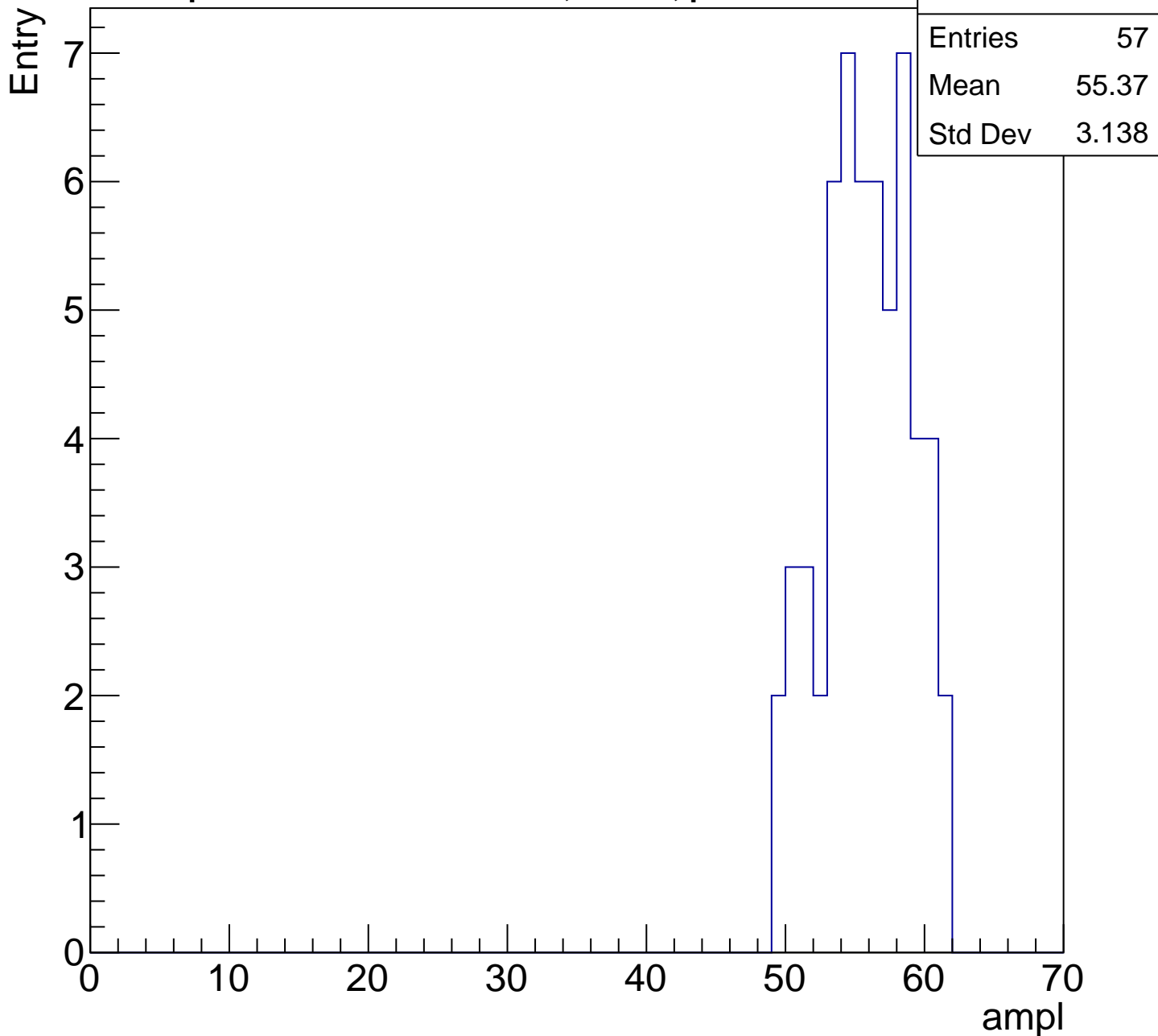
ampl

0 10 20 30 40 50 60 70



# B1L102S, U8-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

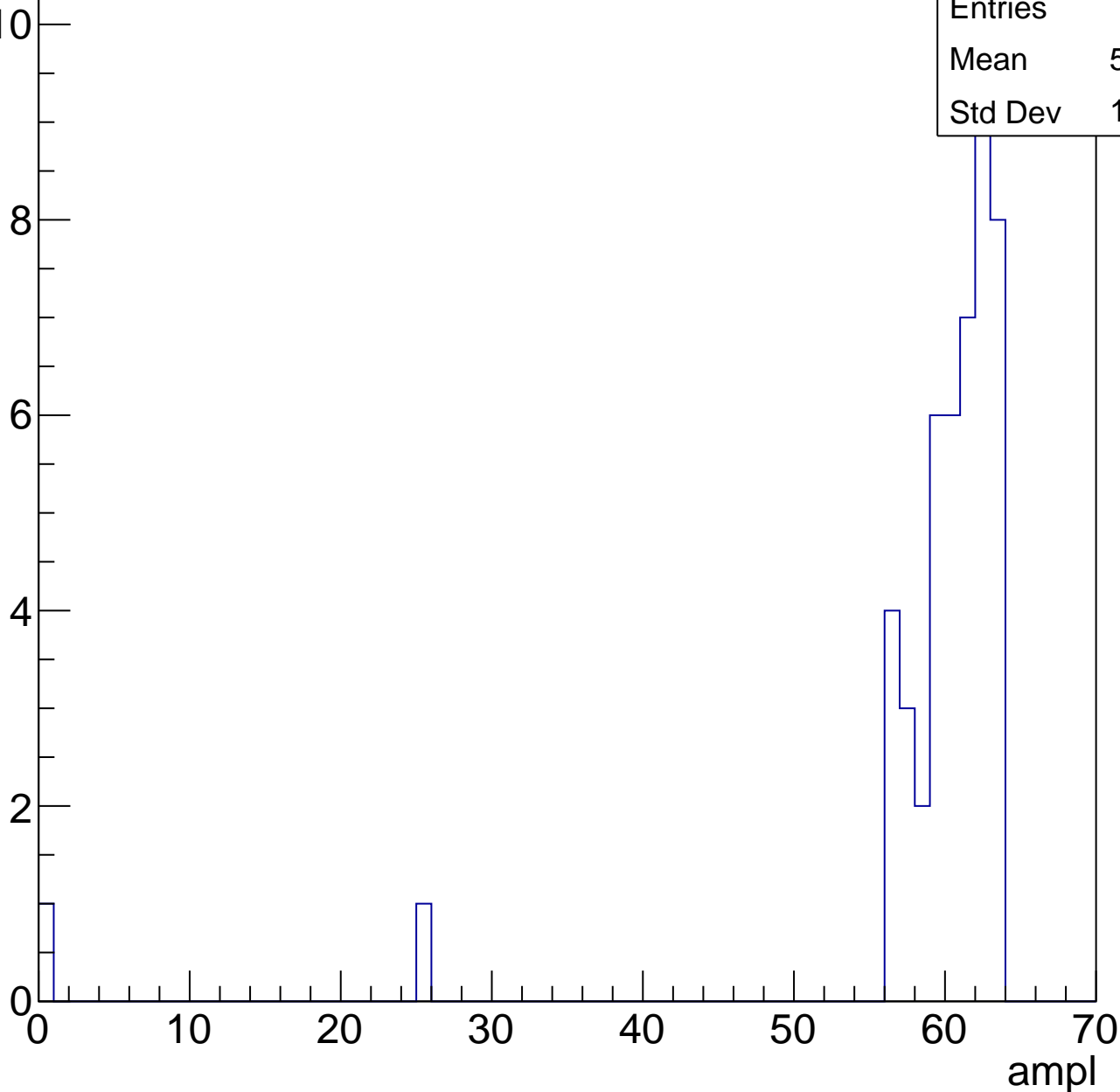


# B1L102S, U8-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

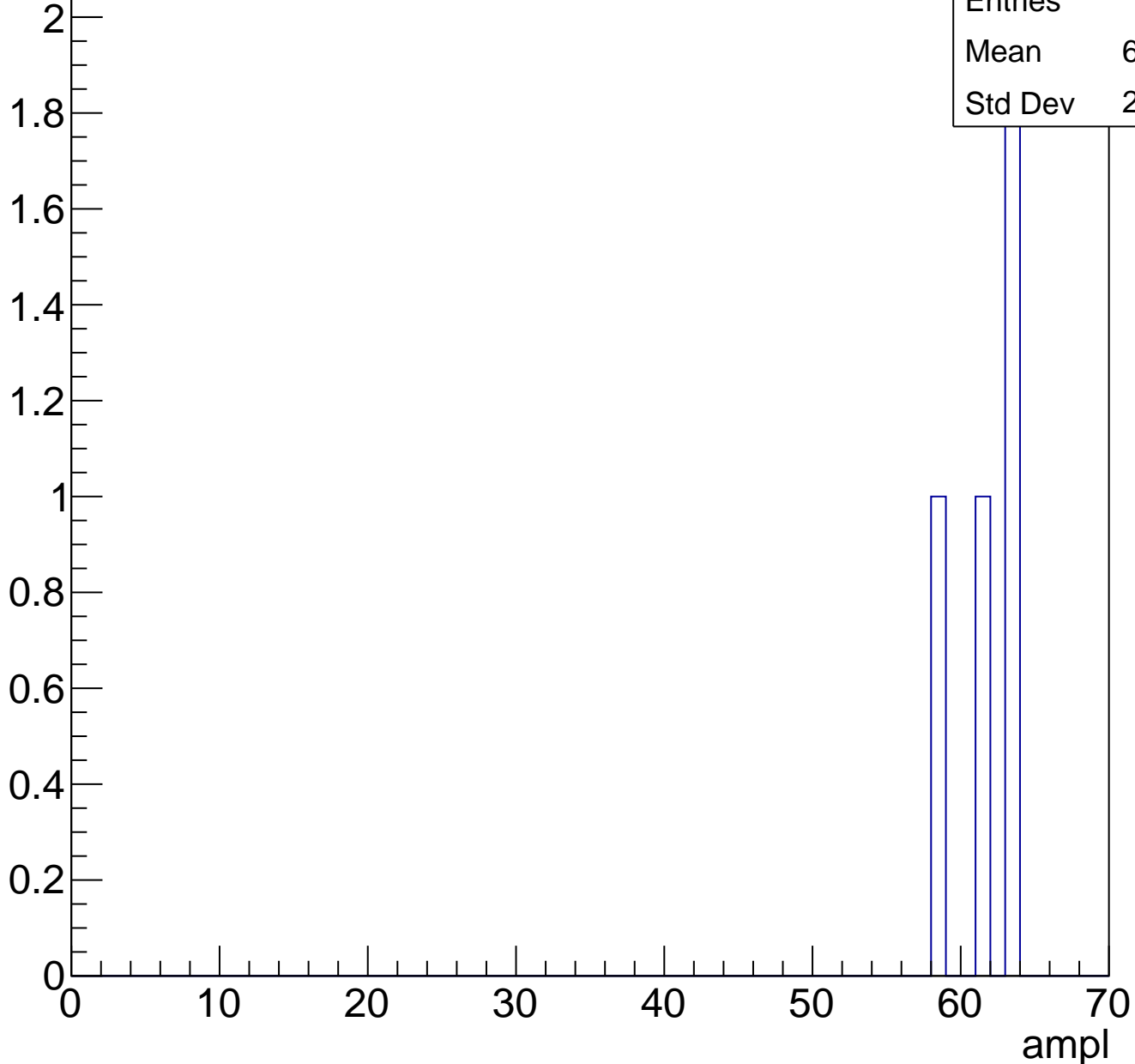
Entries	48
Mean	58.35
Std Dev	10.12



# B1L102S, U8-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch41, adc0

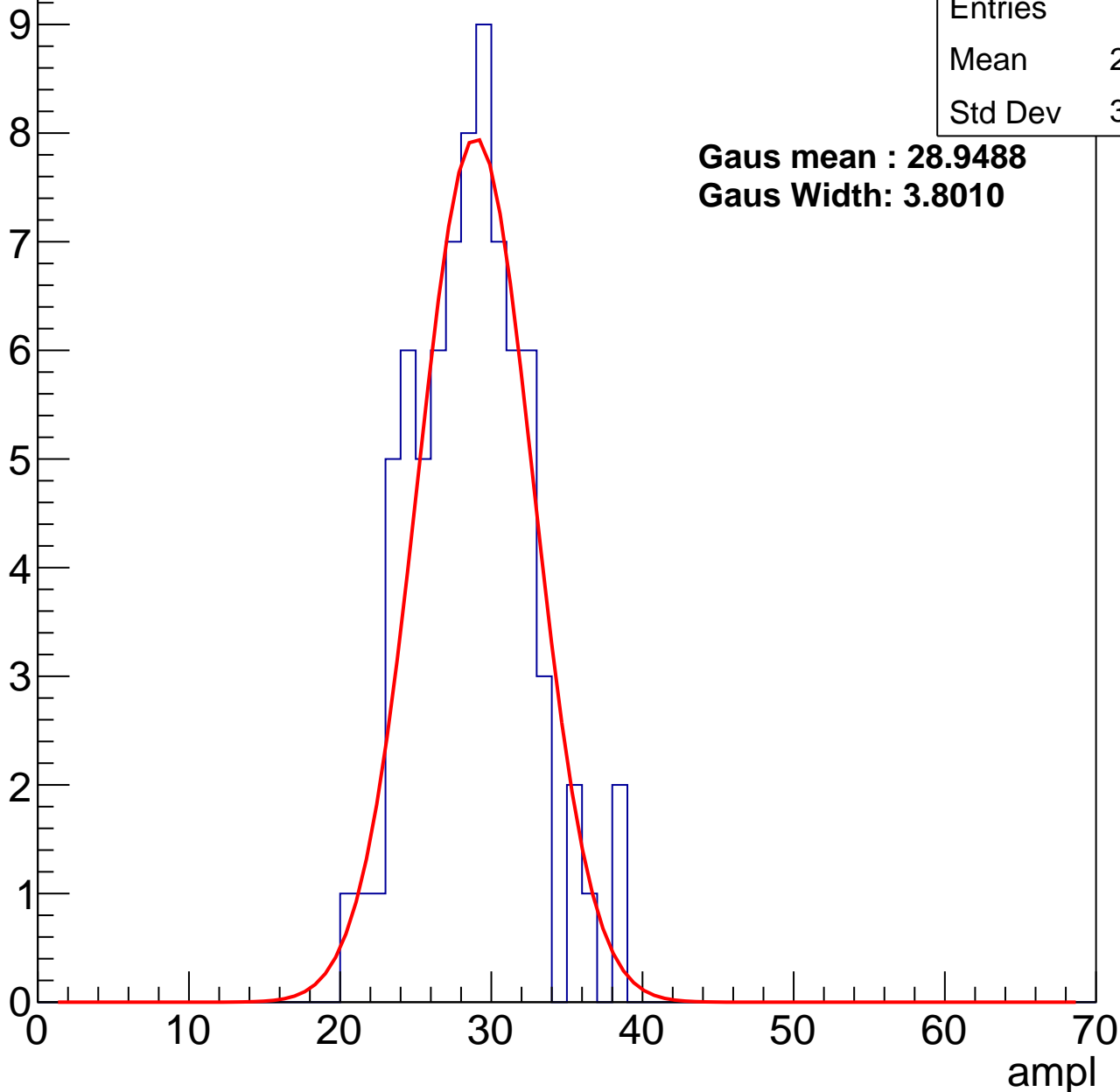
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	28.24
Std Dev	3.745

**Gaus mean : 28.9488**

**Gaus Width: 3.8010**



# B1L102S, U8-ch41, adc1

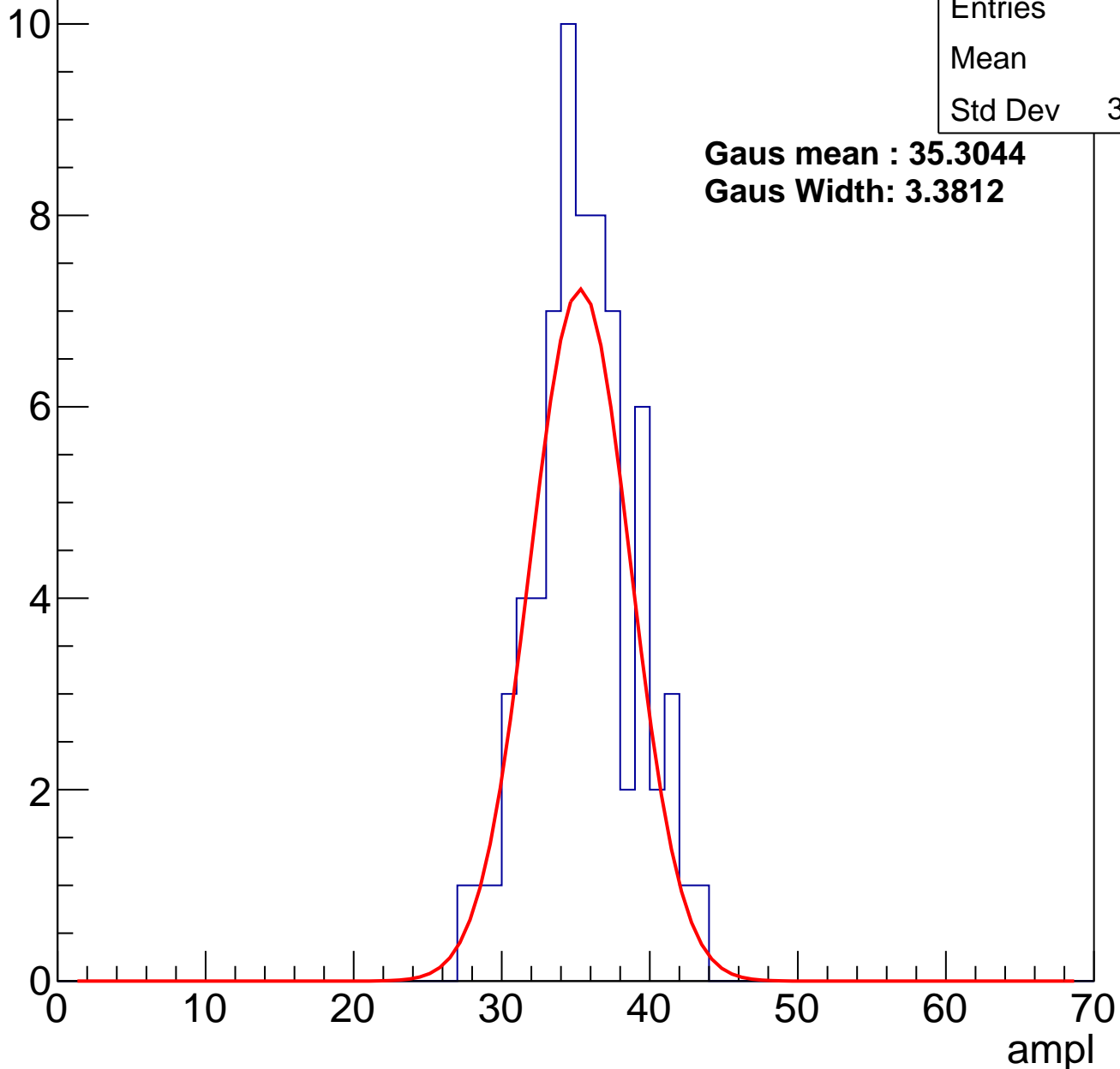
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	69
Mean	35.1
Std Dev	3.367

**Gaus mean : 35.3044**

**Gaus Width: 3.3812**

Entry

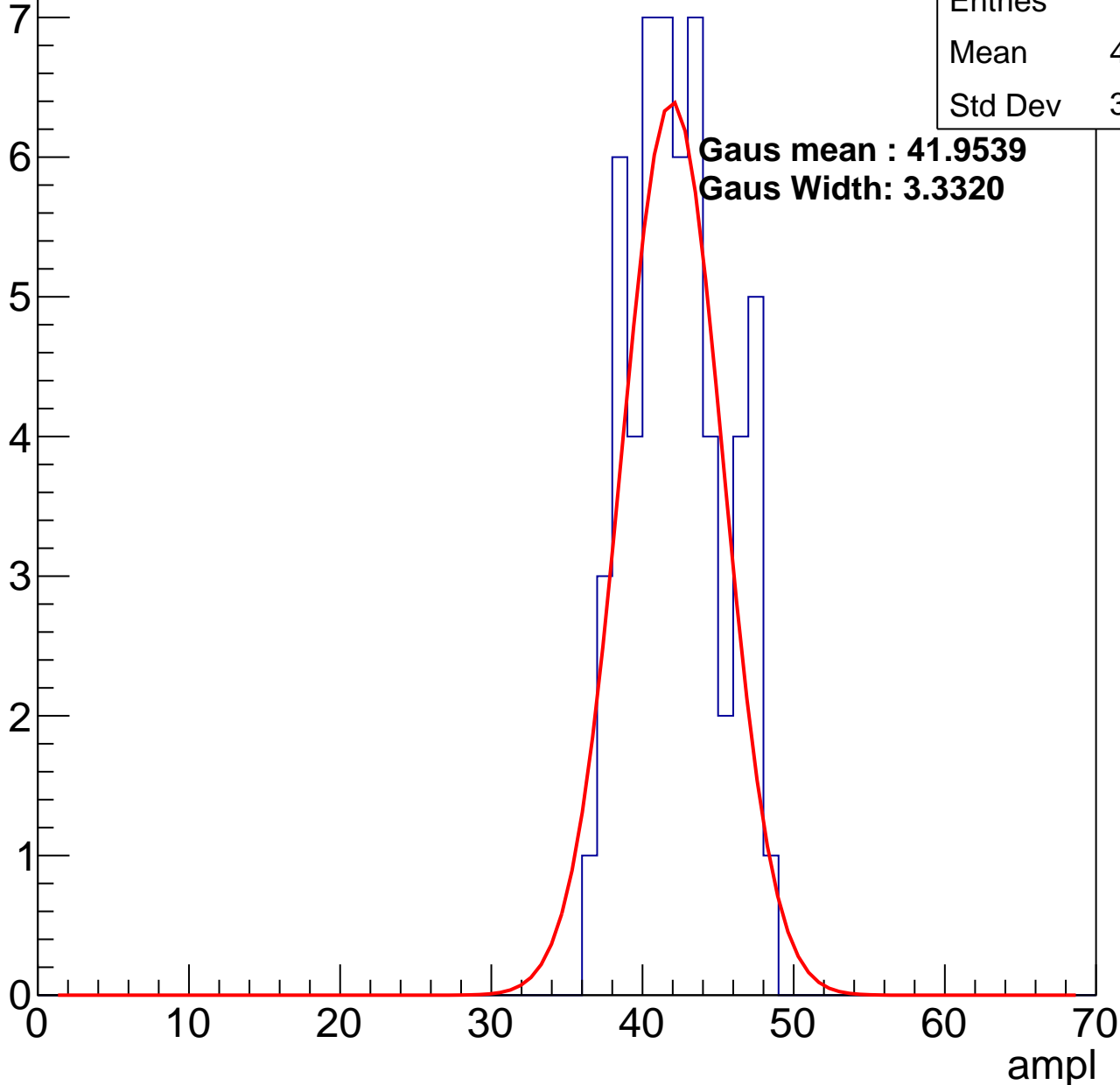


# B1L102S, U8-ch41, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

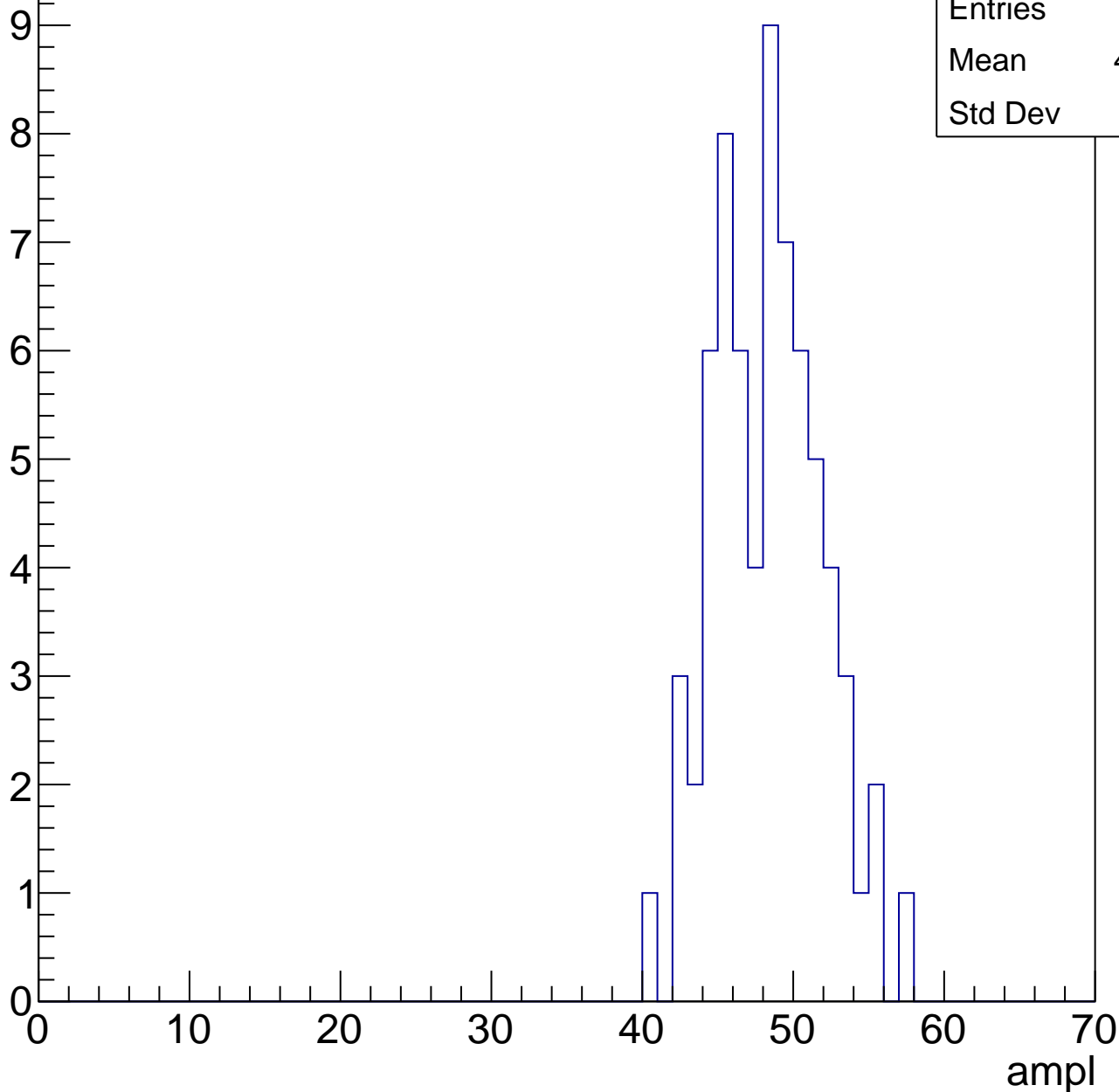
Entries	57
Mean	41.82
Std Dev	3.084



# B1L102S, U8-ch41, adc3

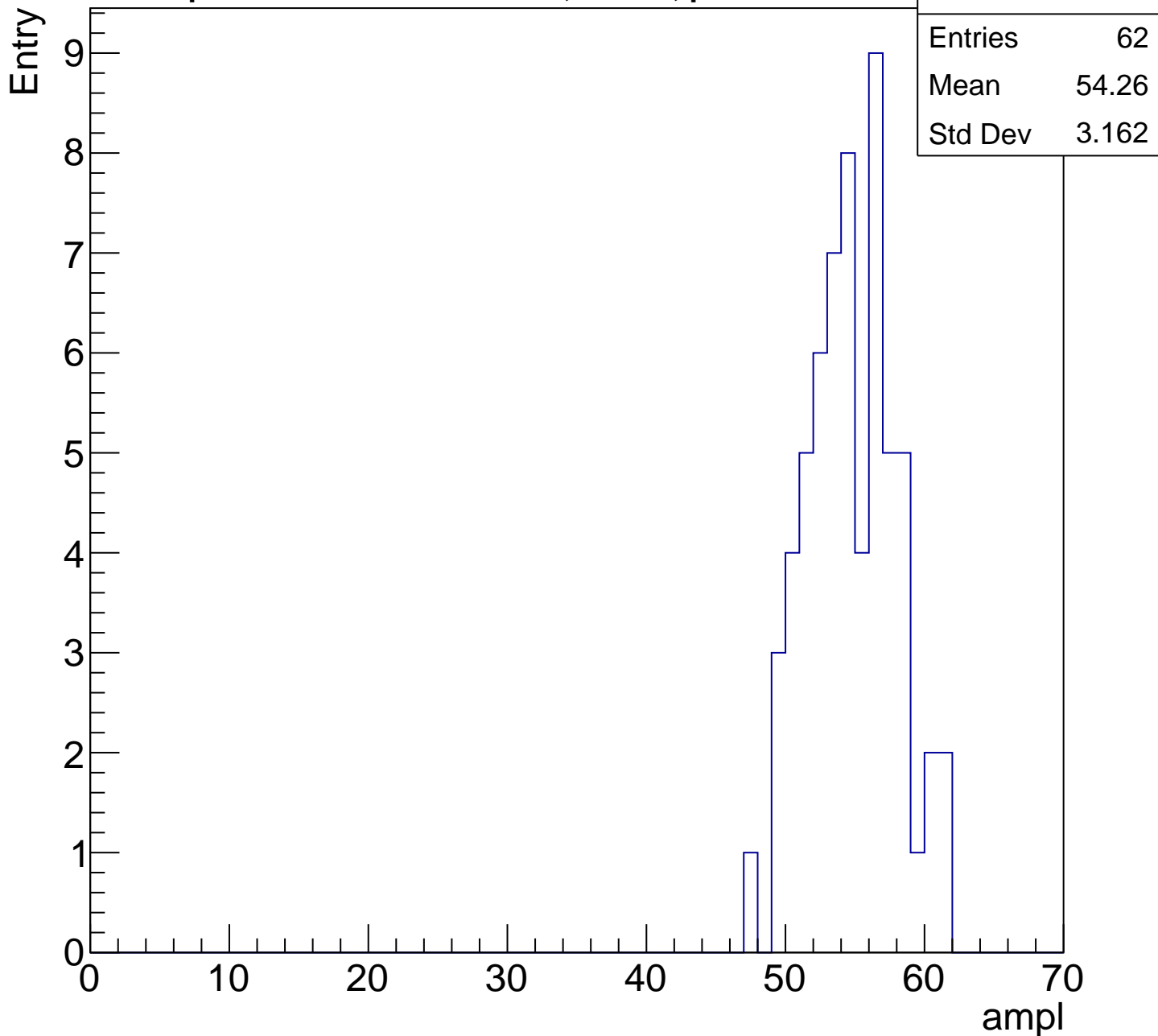
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U8-ch41, adc5

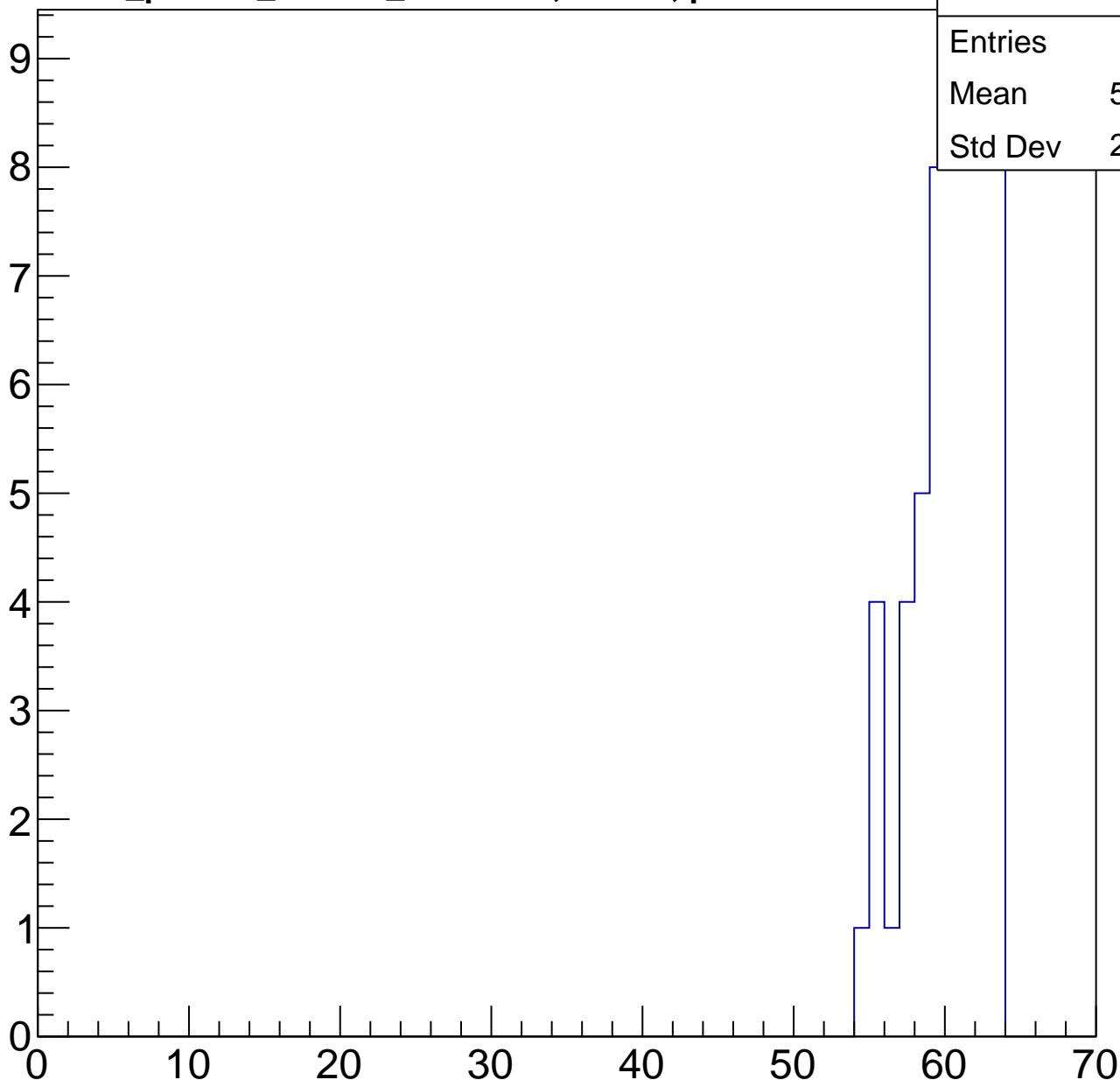
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	56
Mean	59.82
Std Dev	2.428

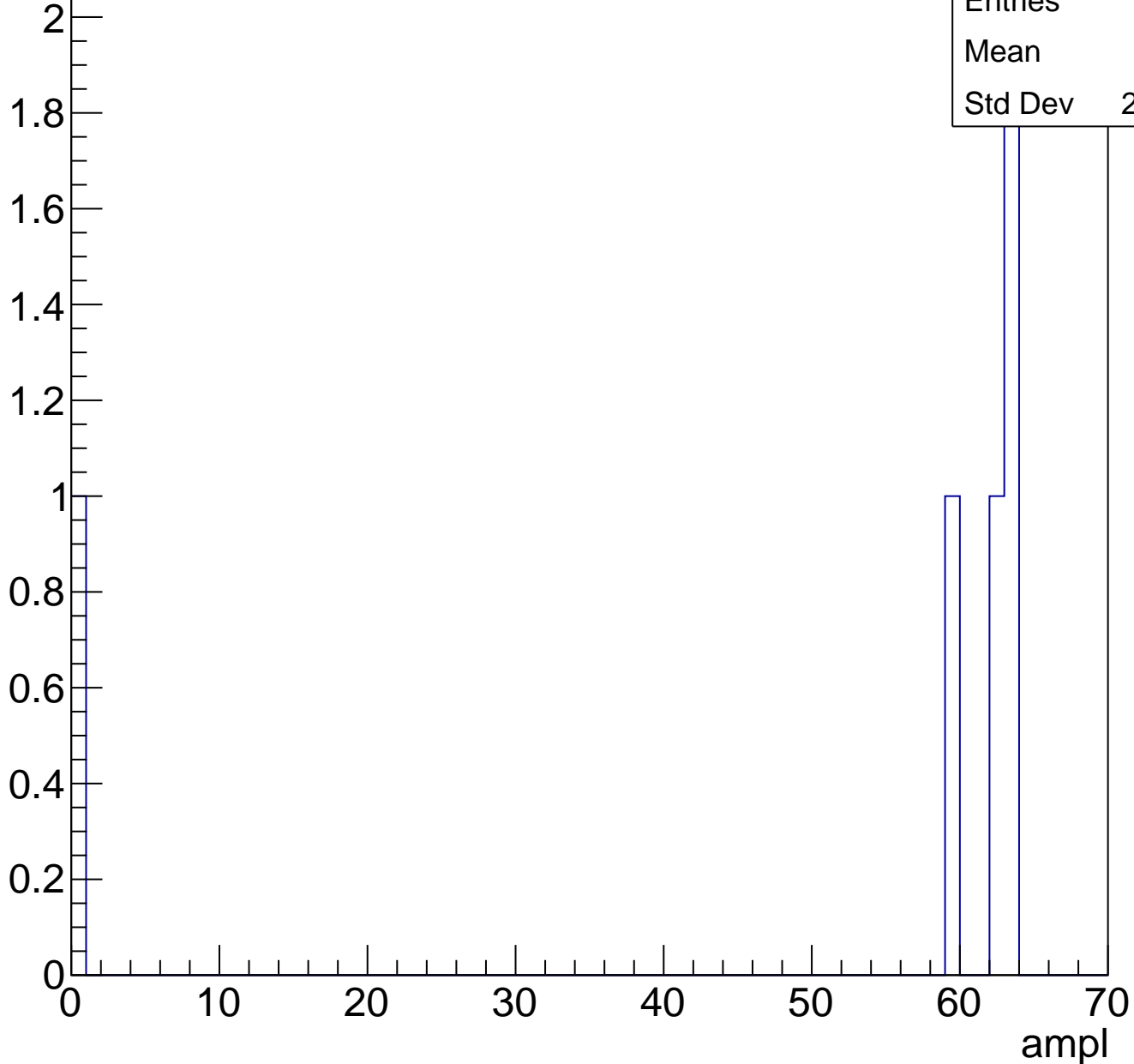
ampl



# B1L102S, U8-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch42, adc0

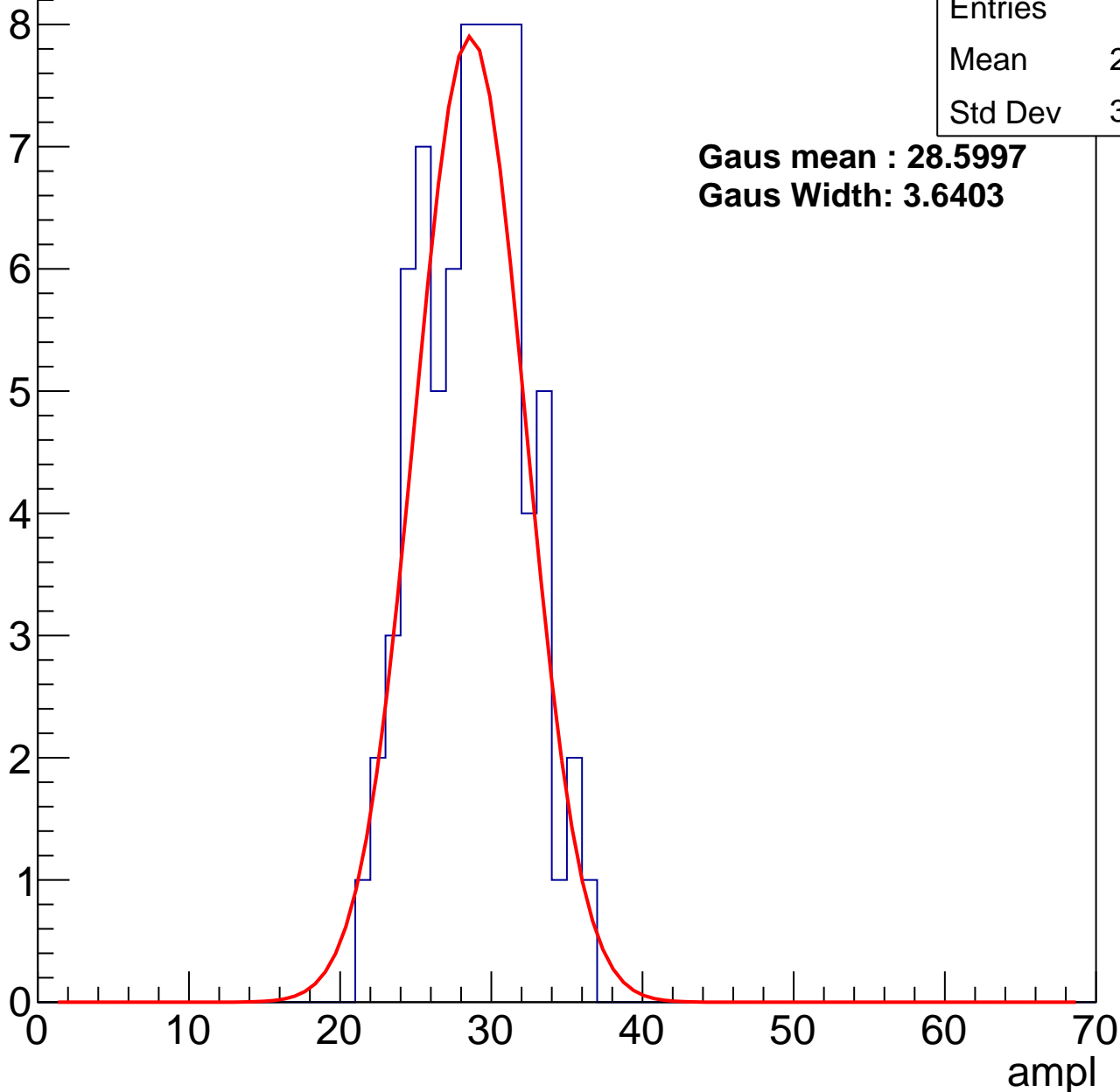
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	28.29
Std Dev	3.413

**Gaus mean : 28.5997**

**Gaus Width: 3.6403**



# B1L102S, U8-ch42, adc1

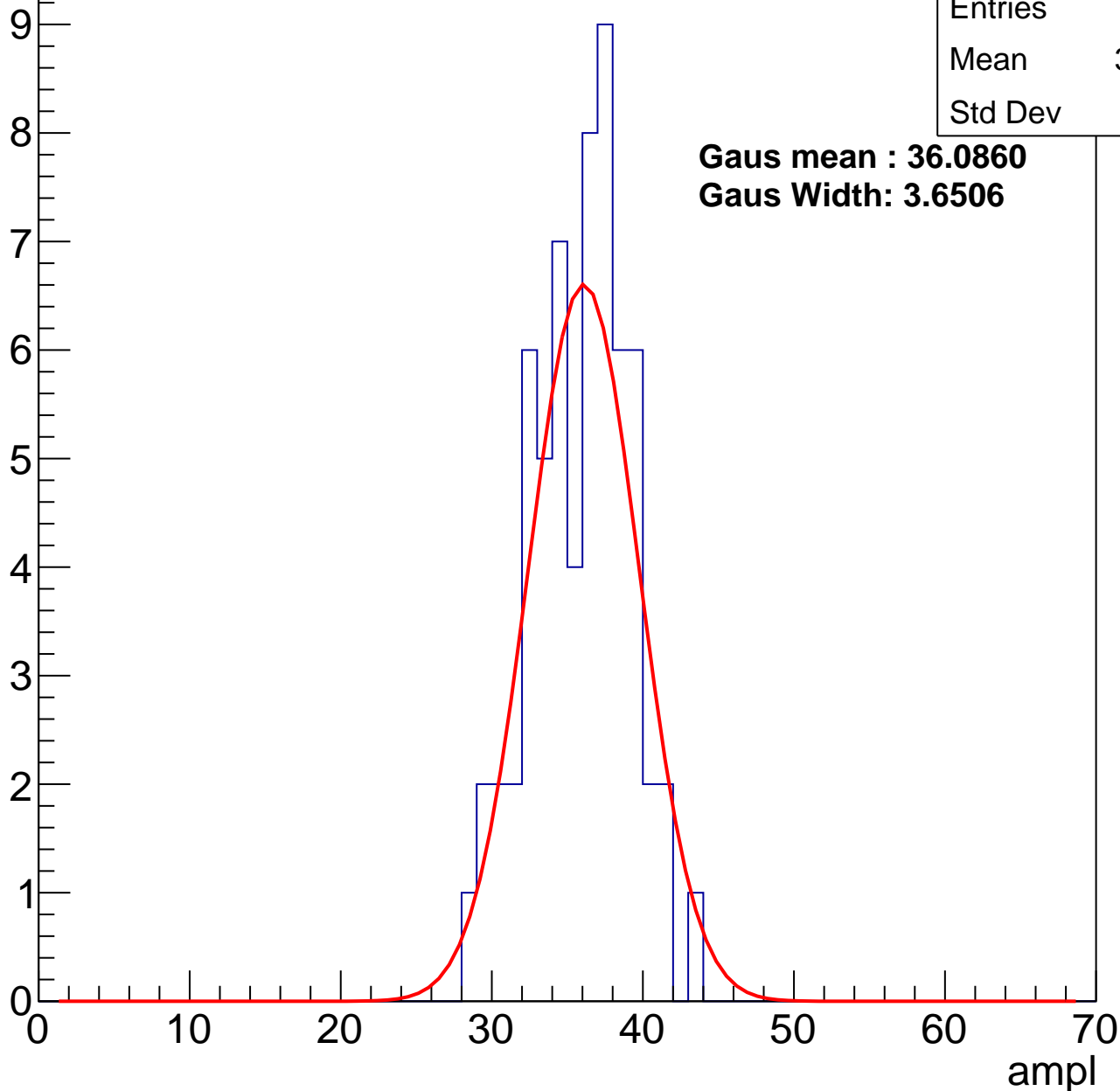
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	35.41
Std Dev	3.22

**Gaus mean : 36.0860**

**Gaus Width: 3.6506**



# B1L102S, U8-ch42, adc2

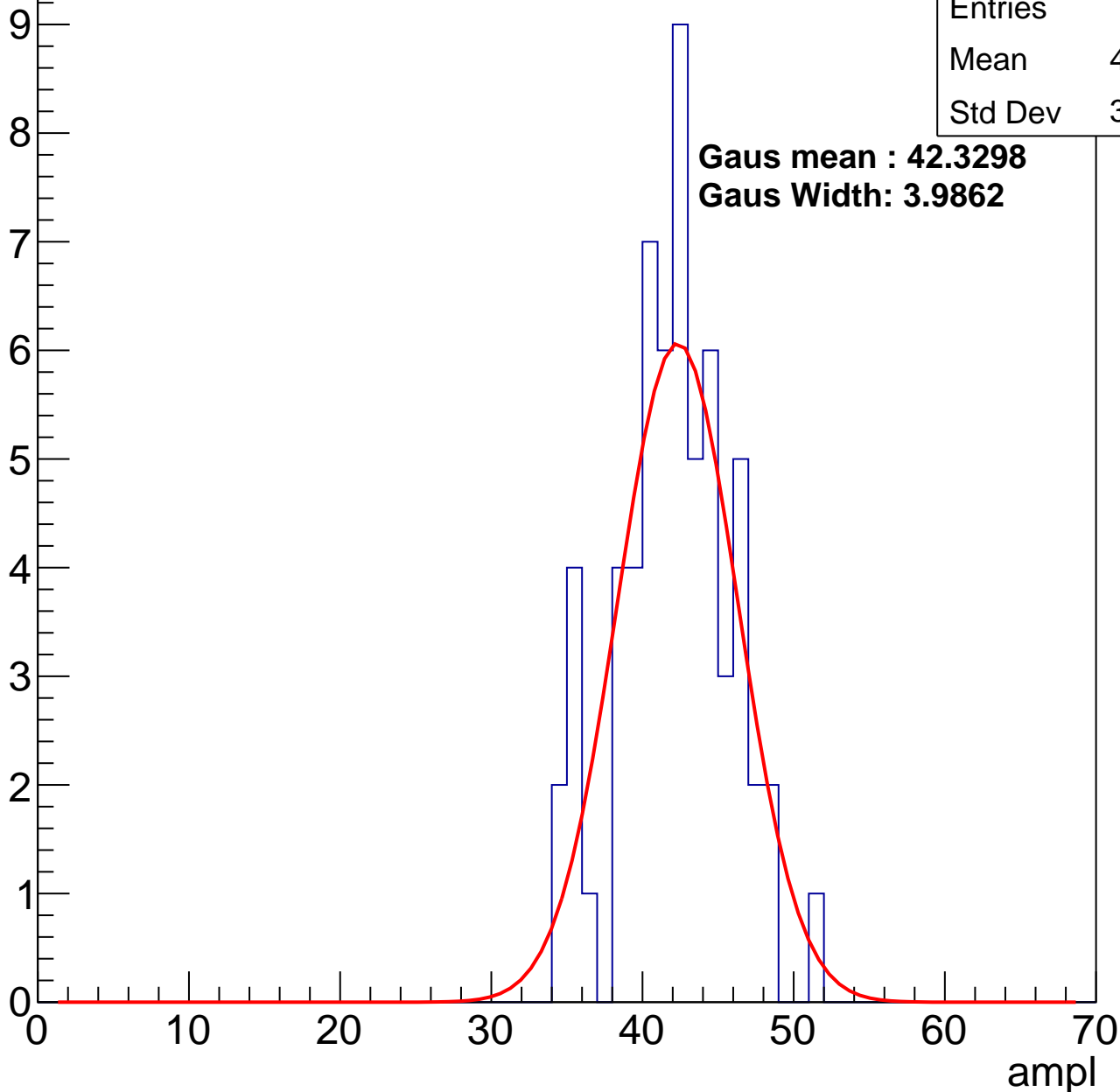
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	41.66
Std Dev	3.679

**Gaus mean : 42.3298**

**Gaus Width: 3.9862**

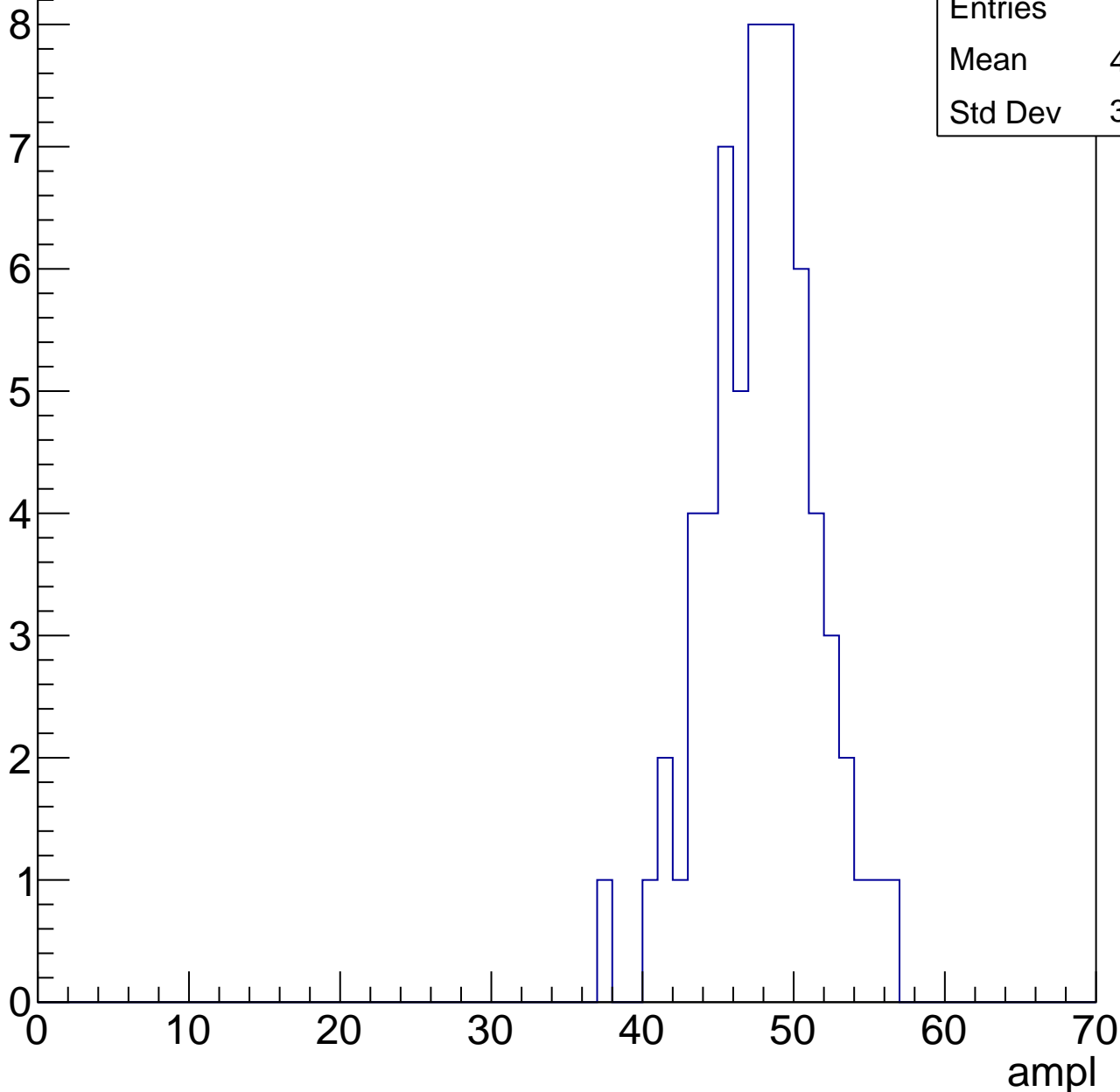


# B1L102S, U8-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	47.42
Std Dev	3.596



# B1L102S, U8-ch42, adc4

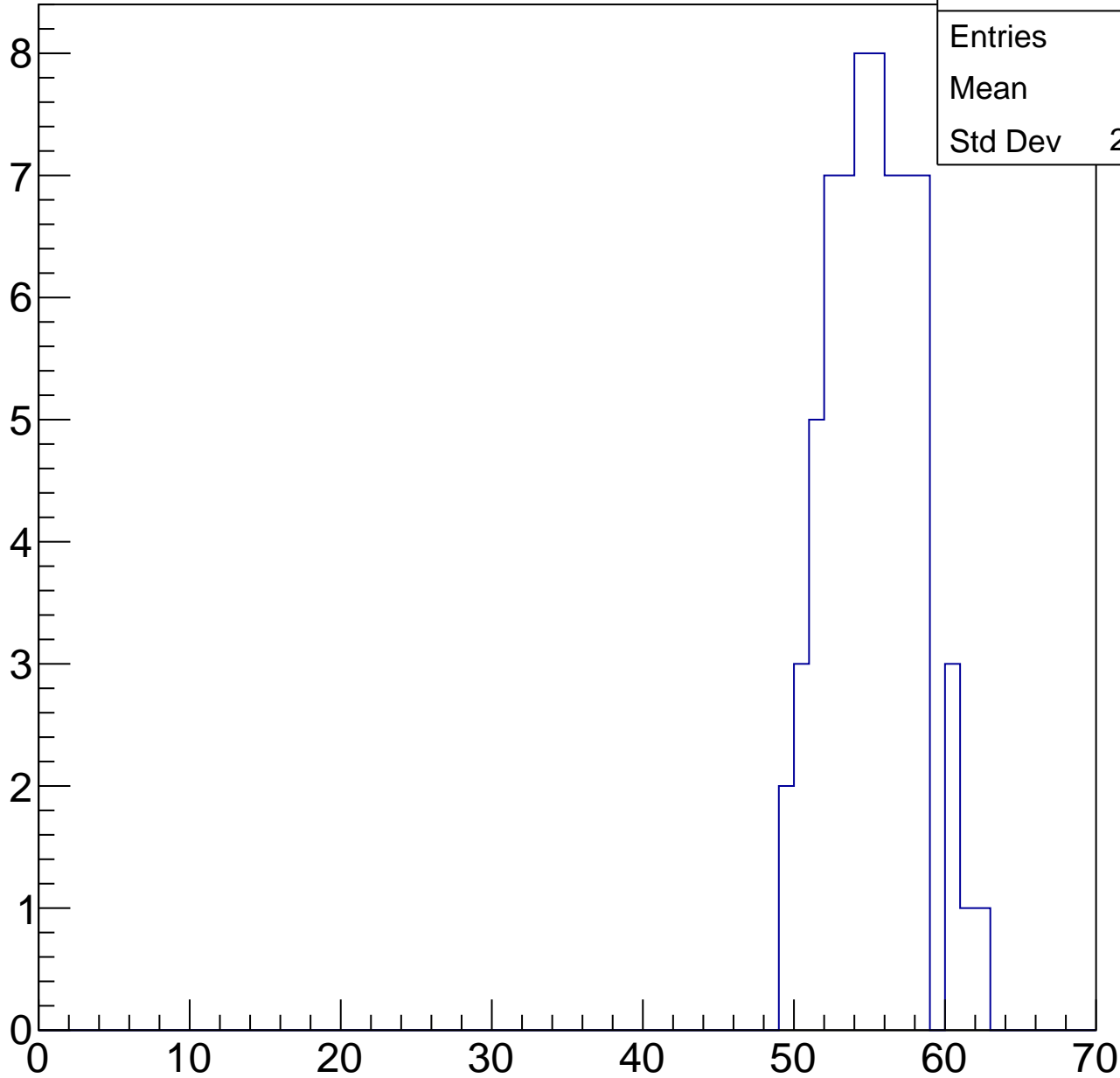
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	66
Mean	54.7
Std Dev	2.959

ampl

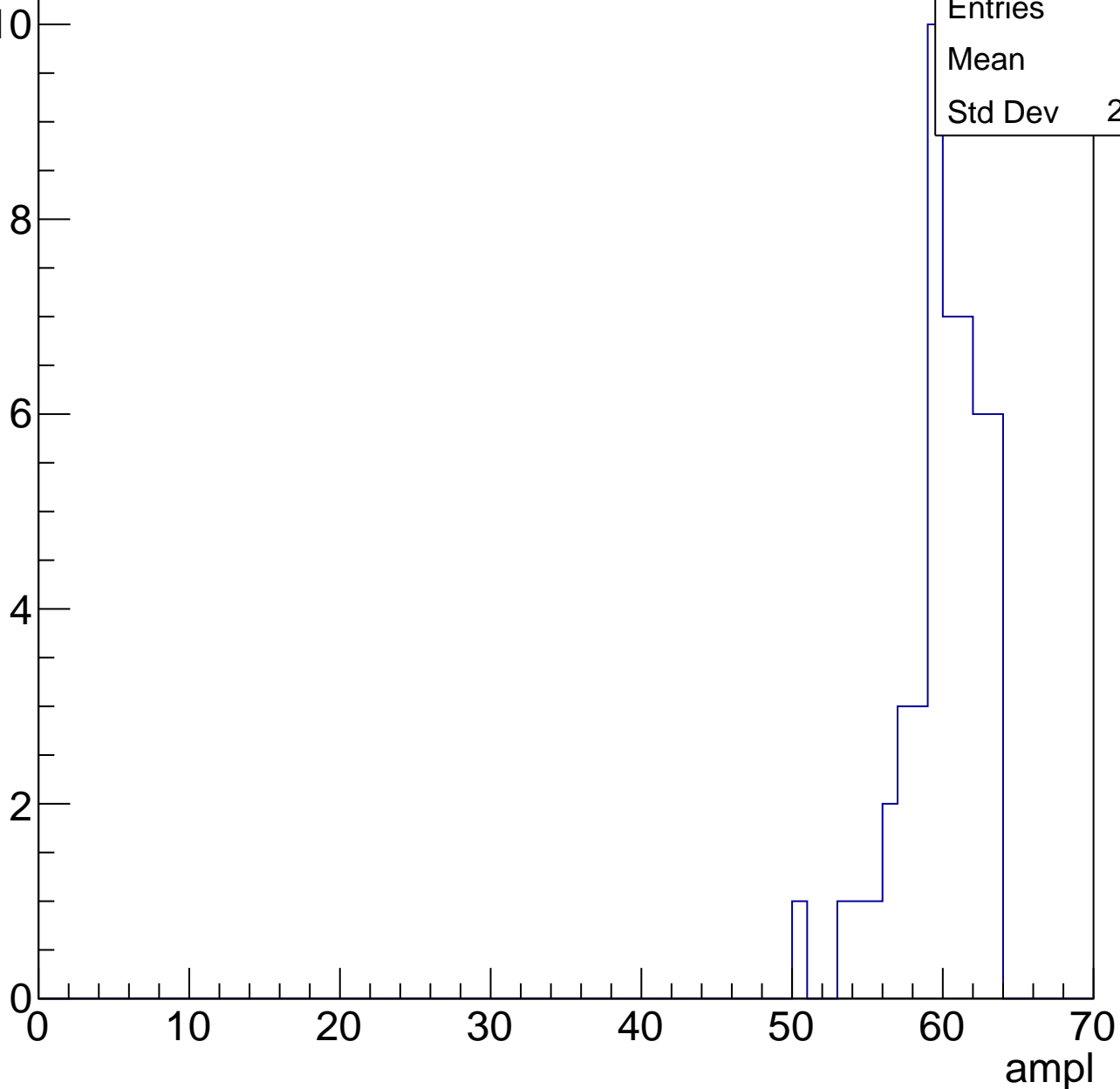


# B1L102S, U8-ch42, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	59.5
Std Dev	2.754



# B1L102S, U8-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3

2.5

2

1.5

1

0.5

0

Entries

9

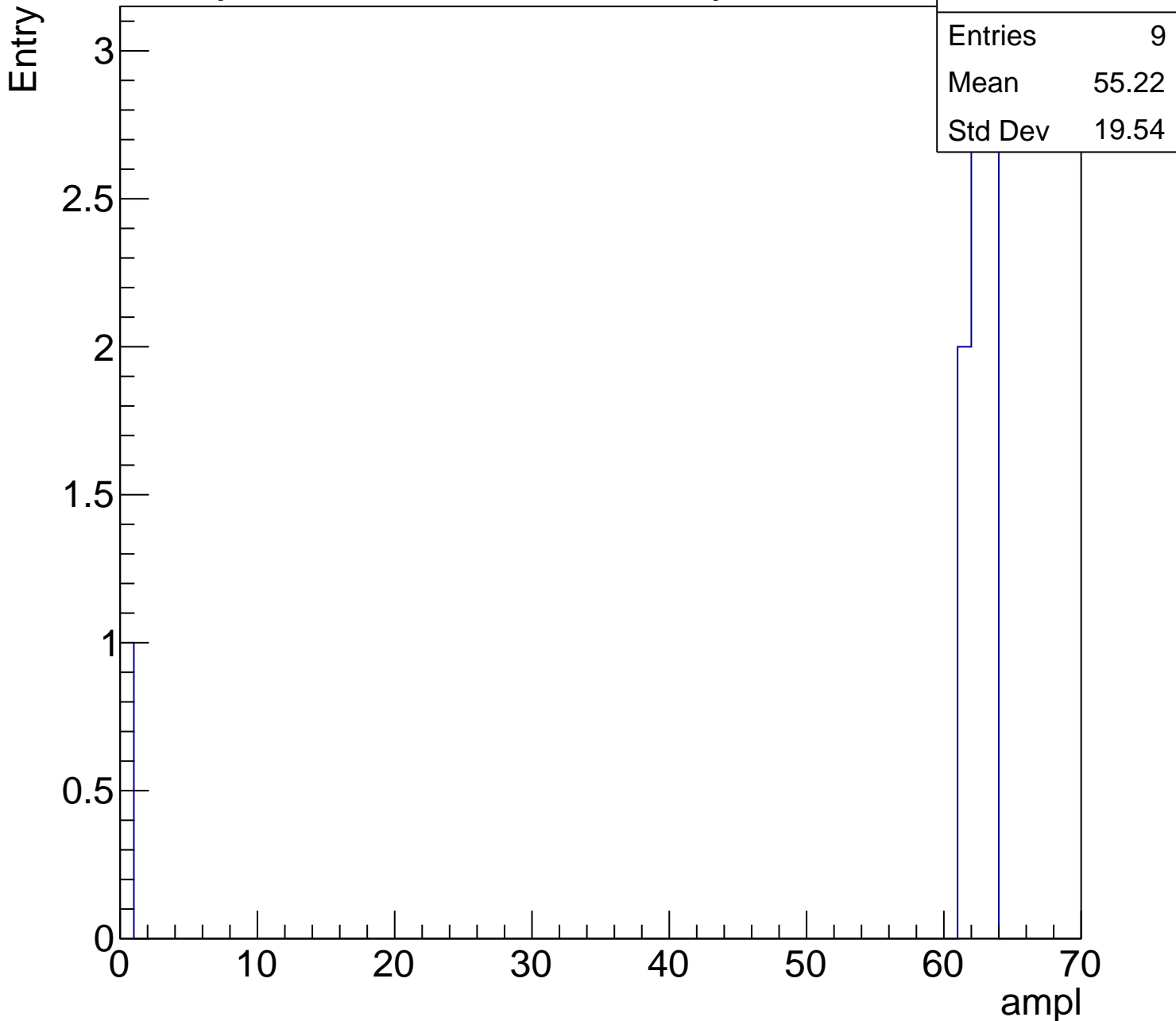
Mean

55.22

Std Dev

19.54

ampl





# B1L102S, U8-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L102S, U8-ch43, adc0

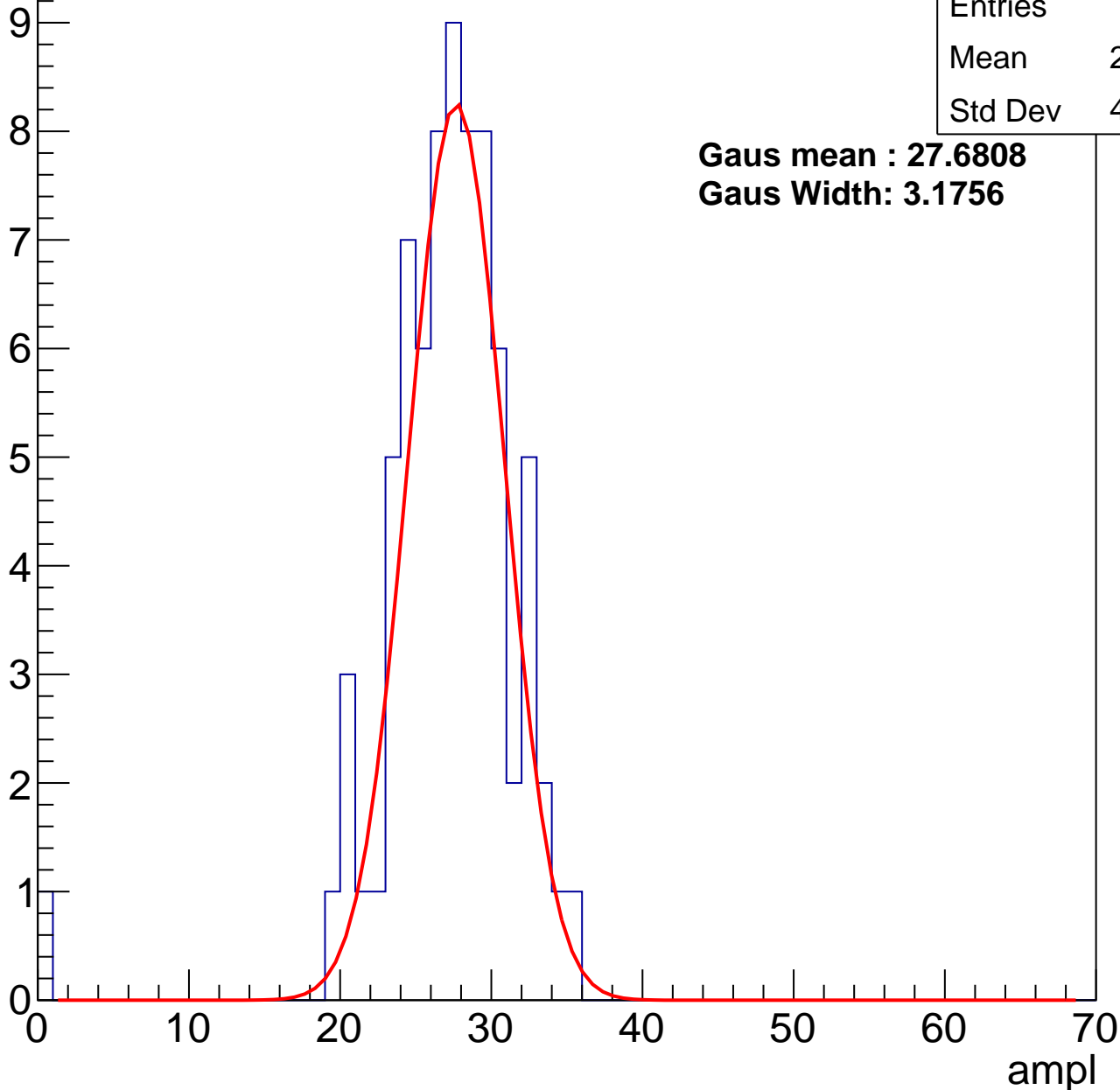
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	26.65
Std Dev	4.623

**Gaus mean : 27.6808**

**Gaus Width: 3.1756**



# B1L102S, U8-ch43, adc1

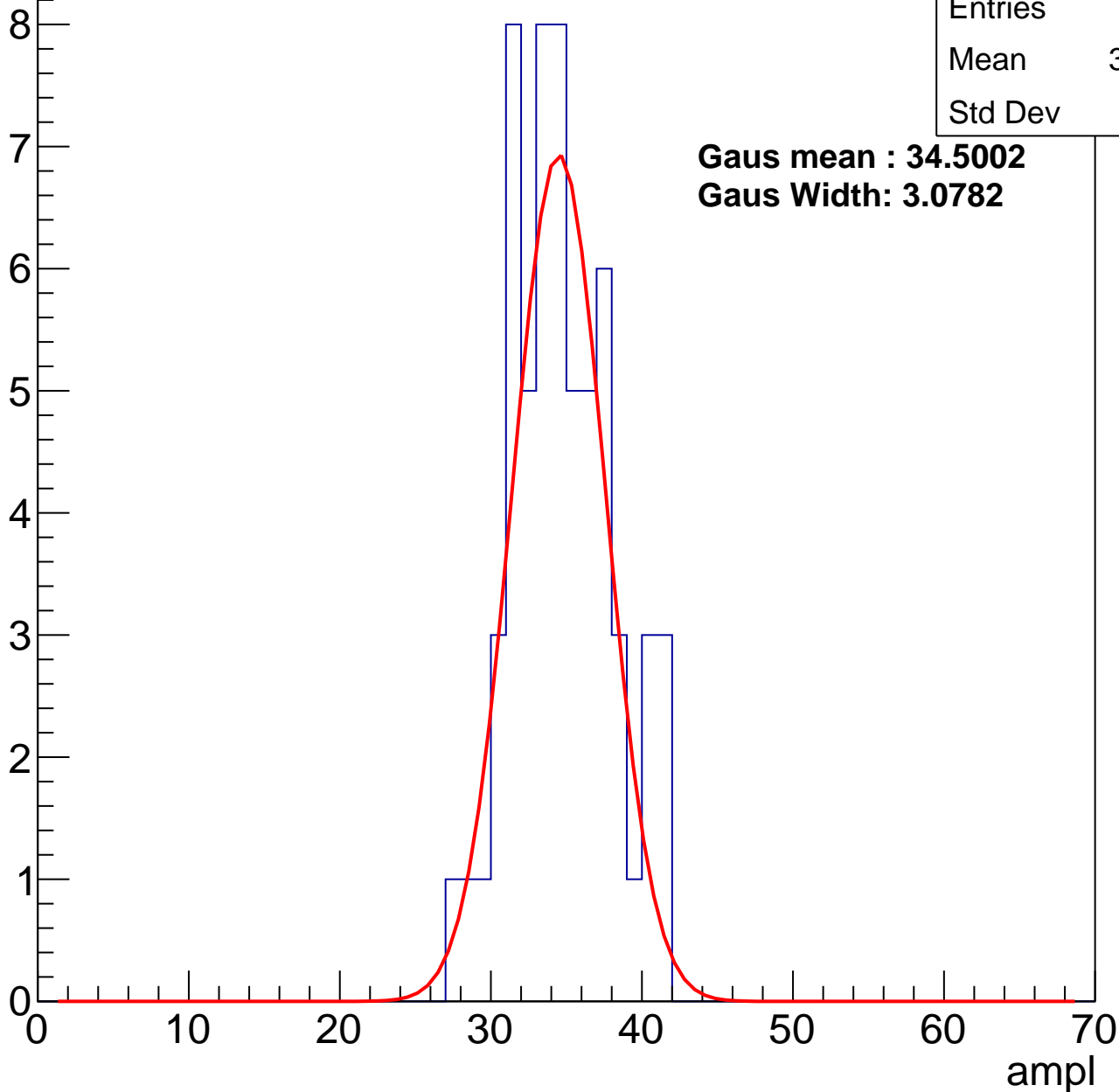
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	34.28
Std Dev	3.29

**Gaus mean : 34.5002**

**Gaus Width: 3.0782**



# B1L102S, U8-ch43, adc2

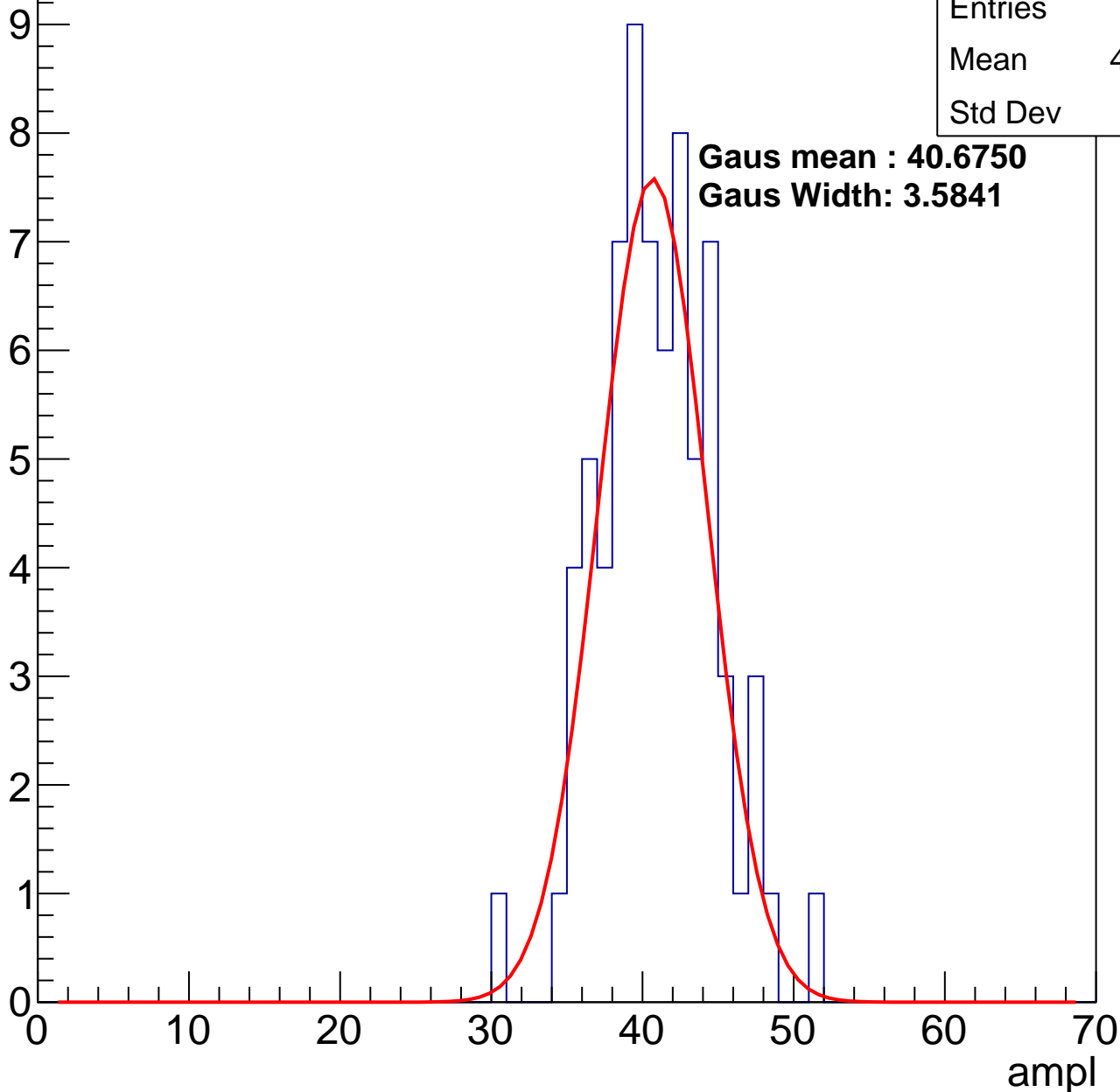
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	40.48
Std Dev	3.72

**Gaus mean : 40.6750**

**Gaus Width: 3.5841**

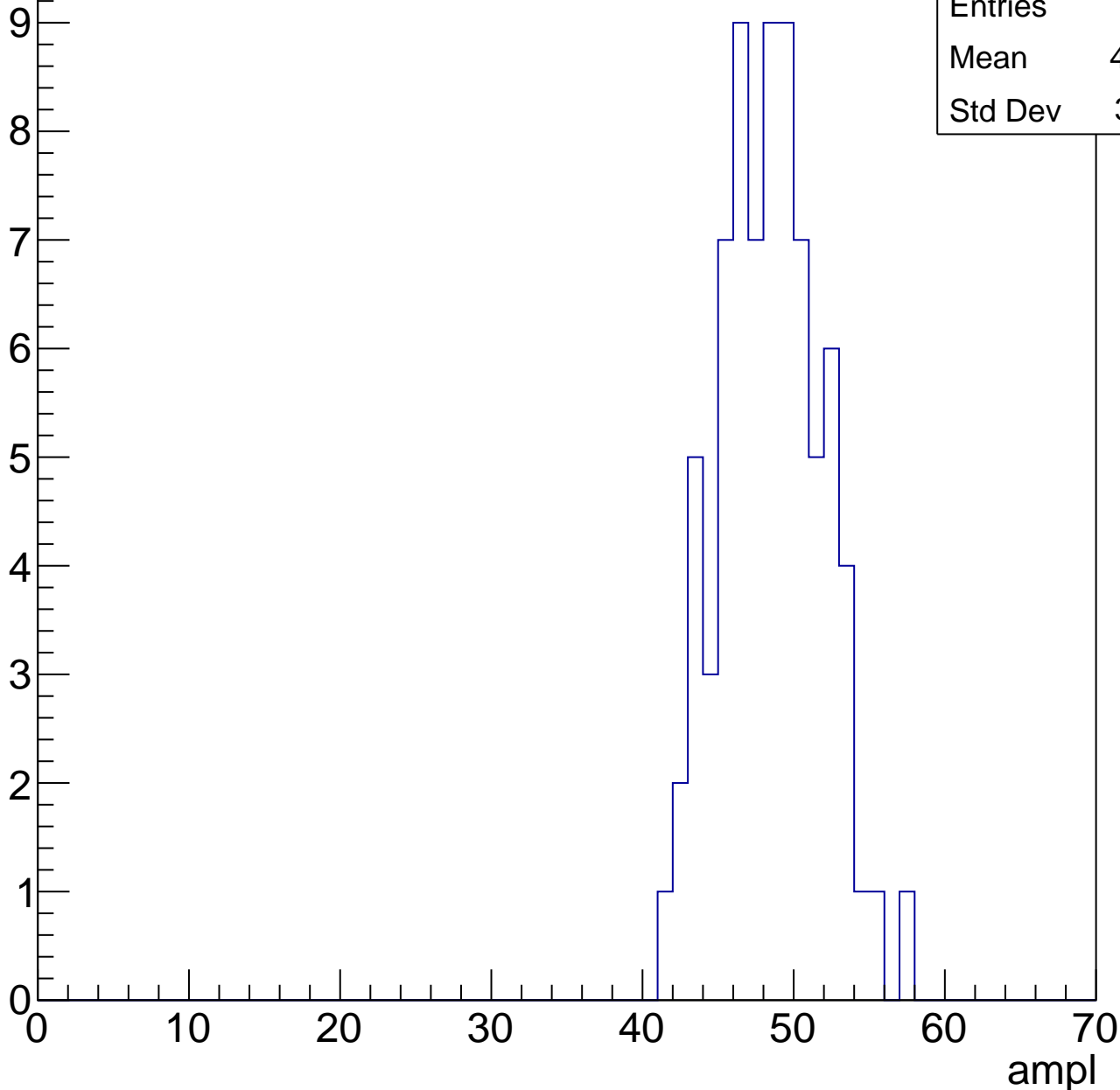


# B1L102S, U8-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	48.03
Std Dev	3.311

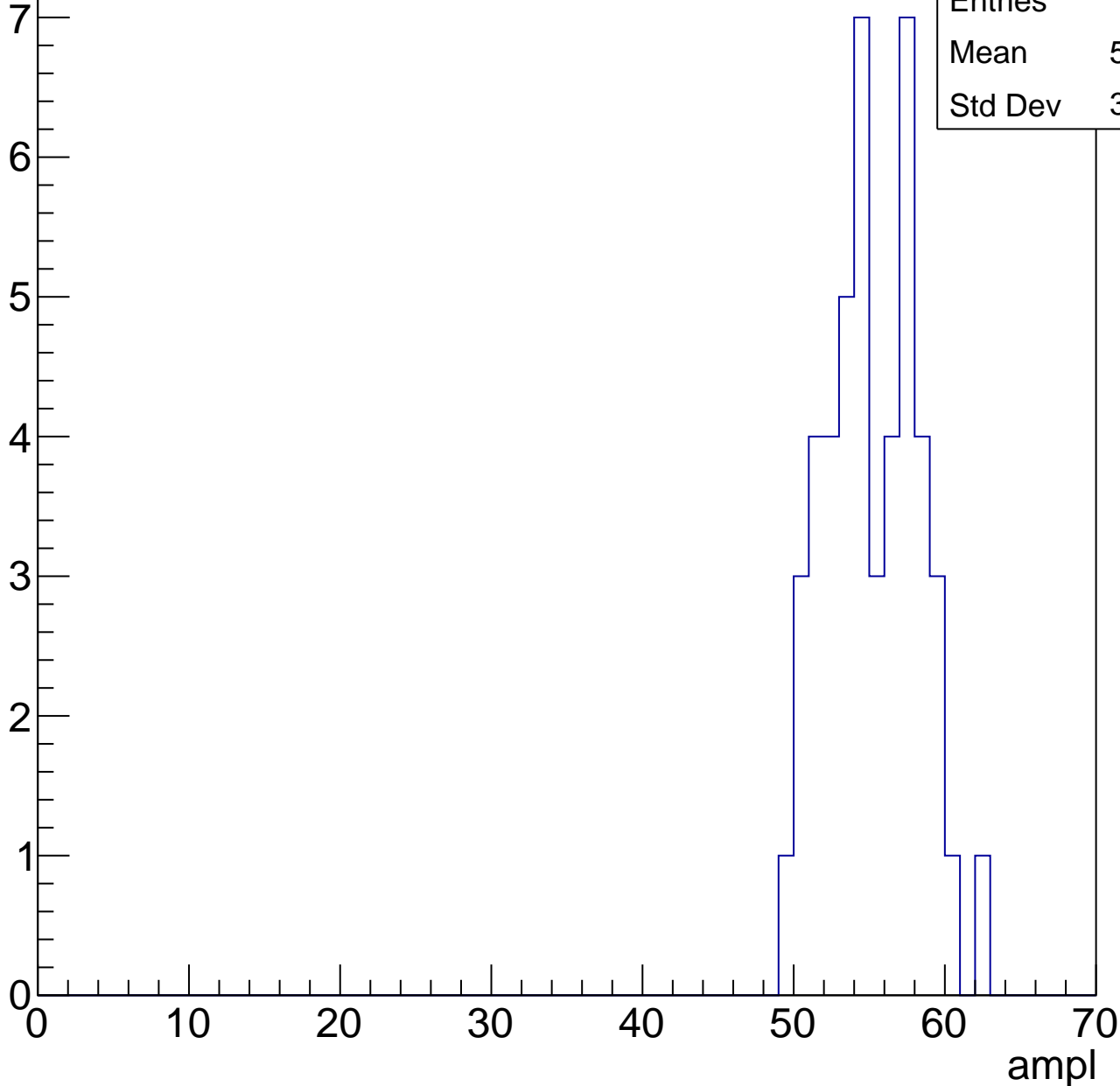


# B1L102S, U8-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	54.74
Std Dev	3.007

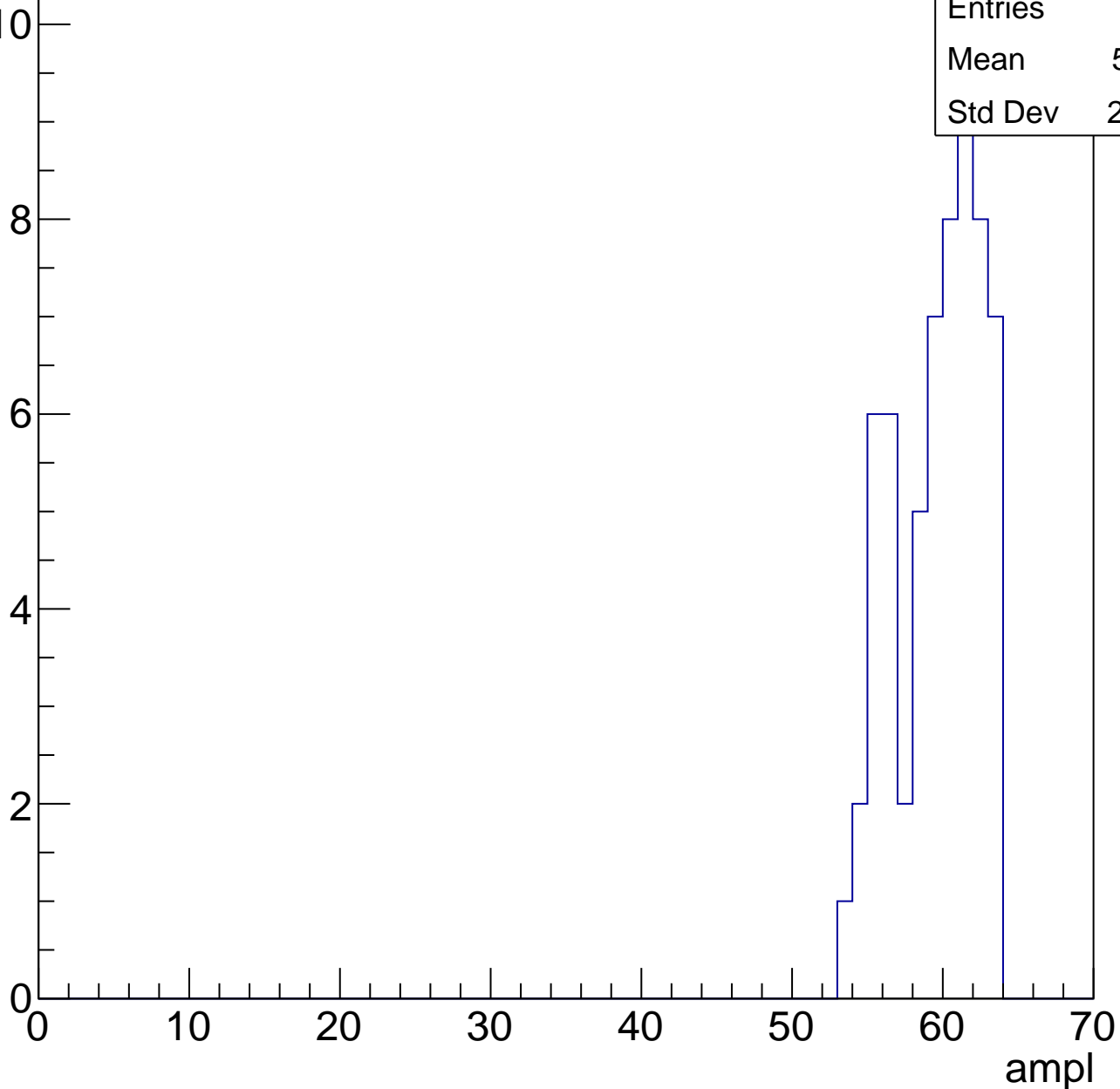


# B1L102S, U8-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

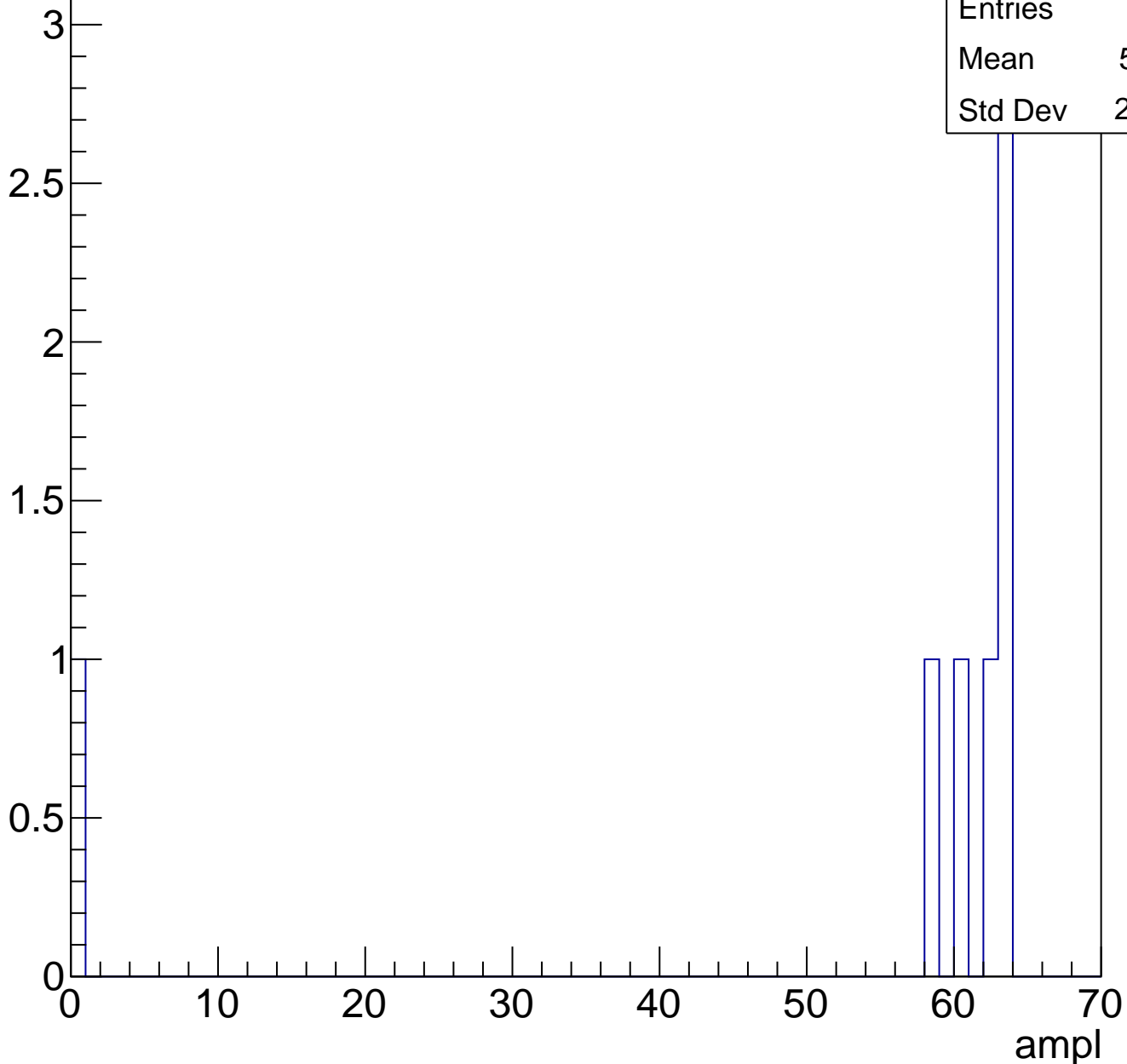
Entries	62
Mean	59.21
Std Dev	2.777



# B1L102S, U8-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	7
Mean	52.71
Std Dev	21.59



# B1L102S, U8-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch44, adc0

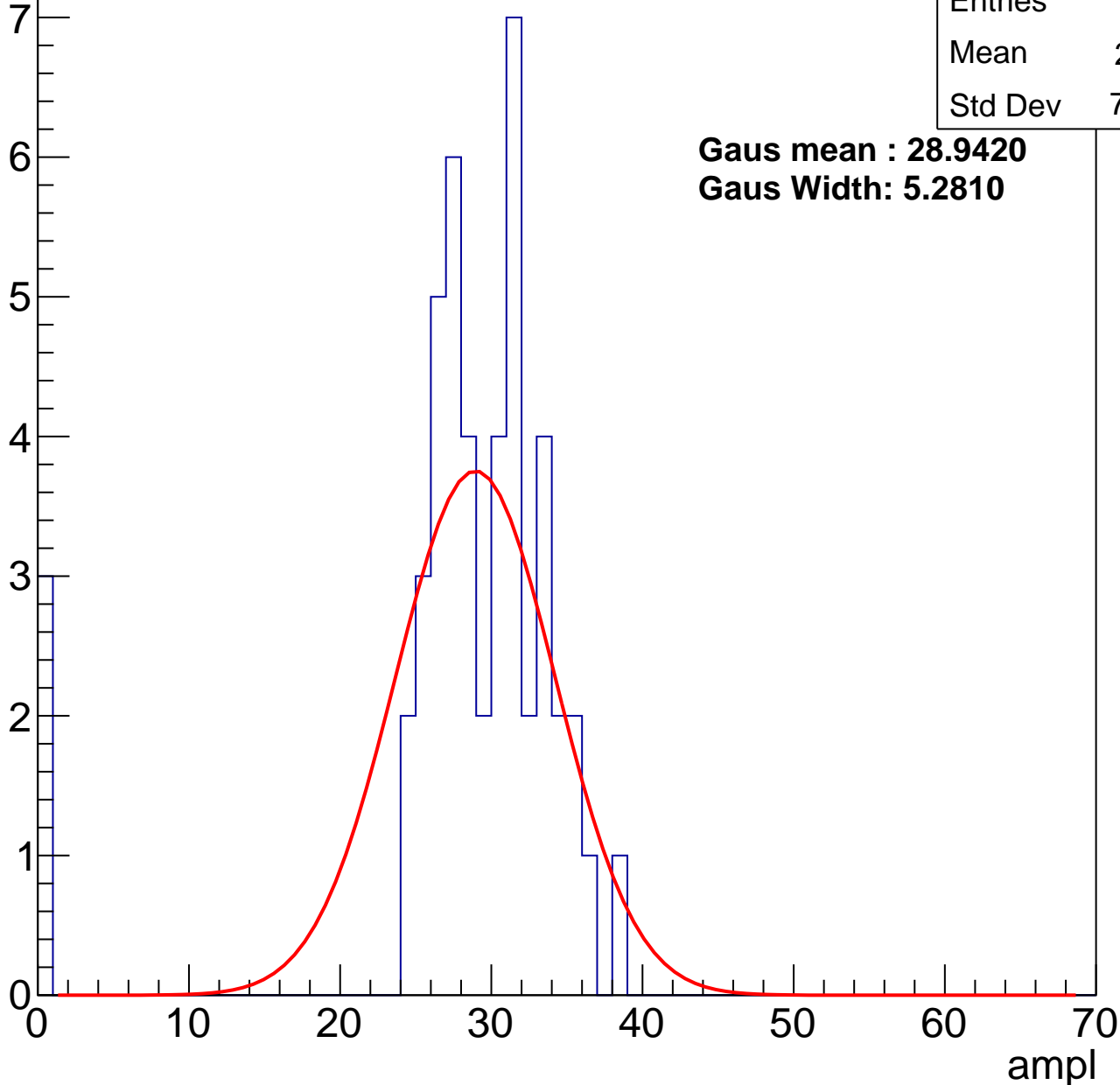
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	27.71
Std Dev	7.879

**Gaus mean : 28.9420**

**Gaus Width: 5.2810**



# B1L102S, U8-ch44, adc1

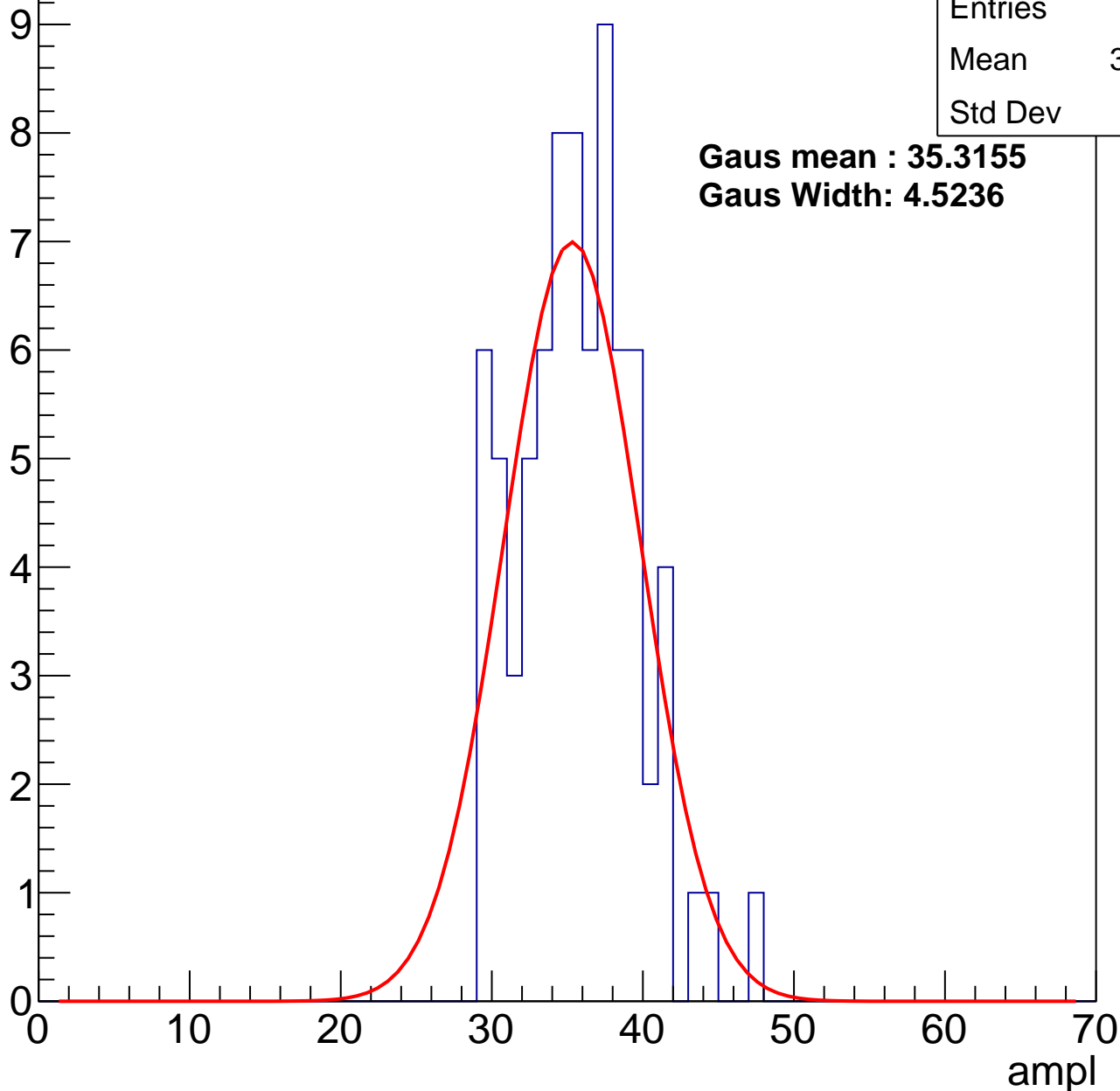
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	35.27
Std Dev	3.84

**Gaus mean : 35.3155**

**Gaus Width: 4.5236**



# B1L102S, U8-ch44, adc2

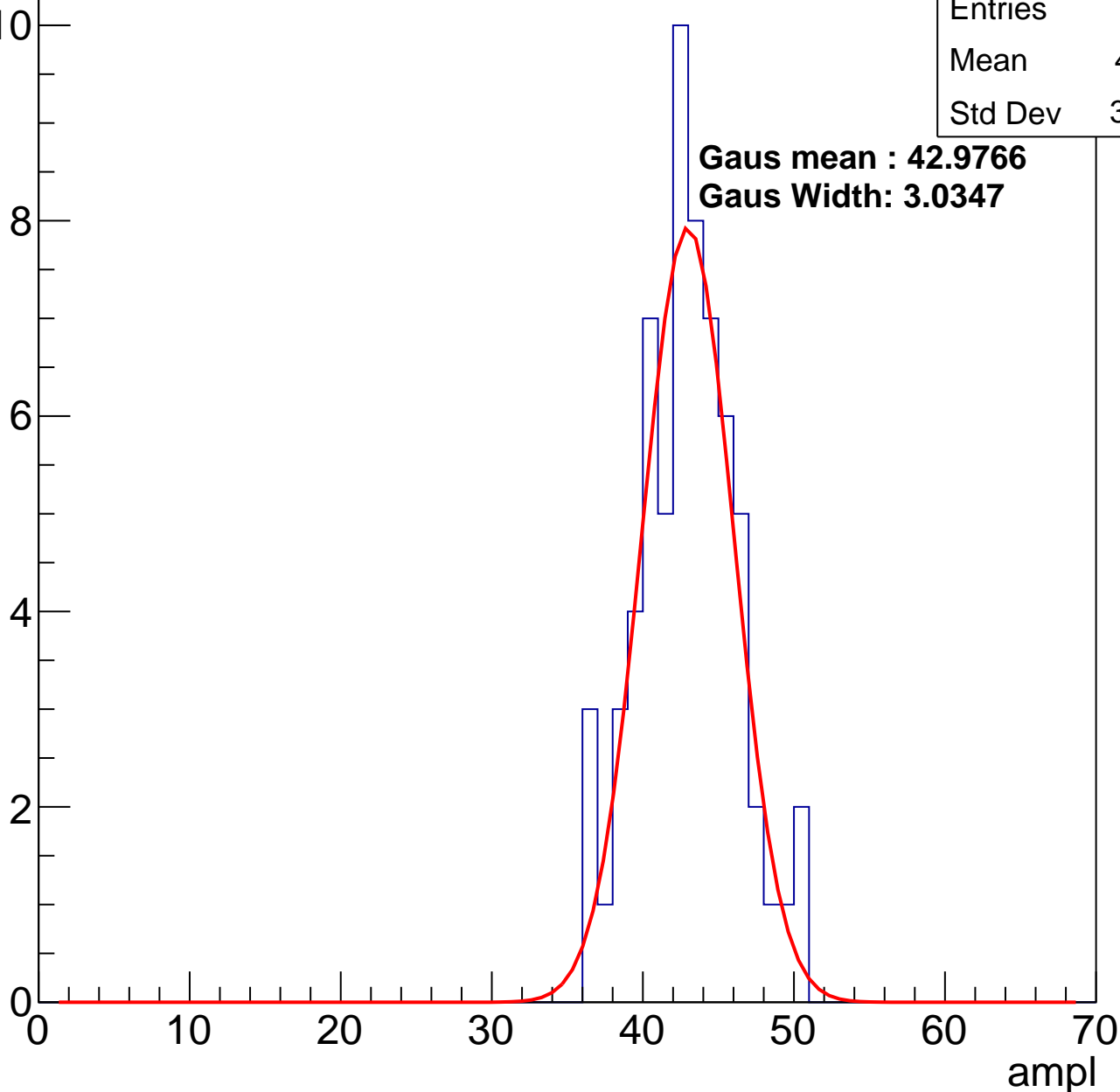
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	42.51
Std Dev	3.202

**Gaus mean : 42.9766**

**Gaus Width: 3.0347**

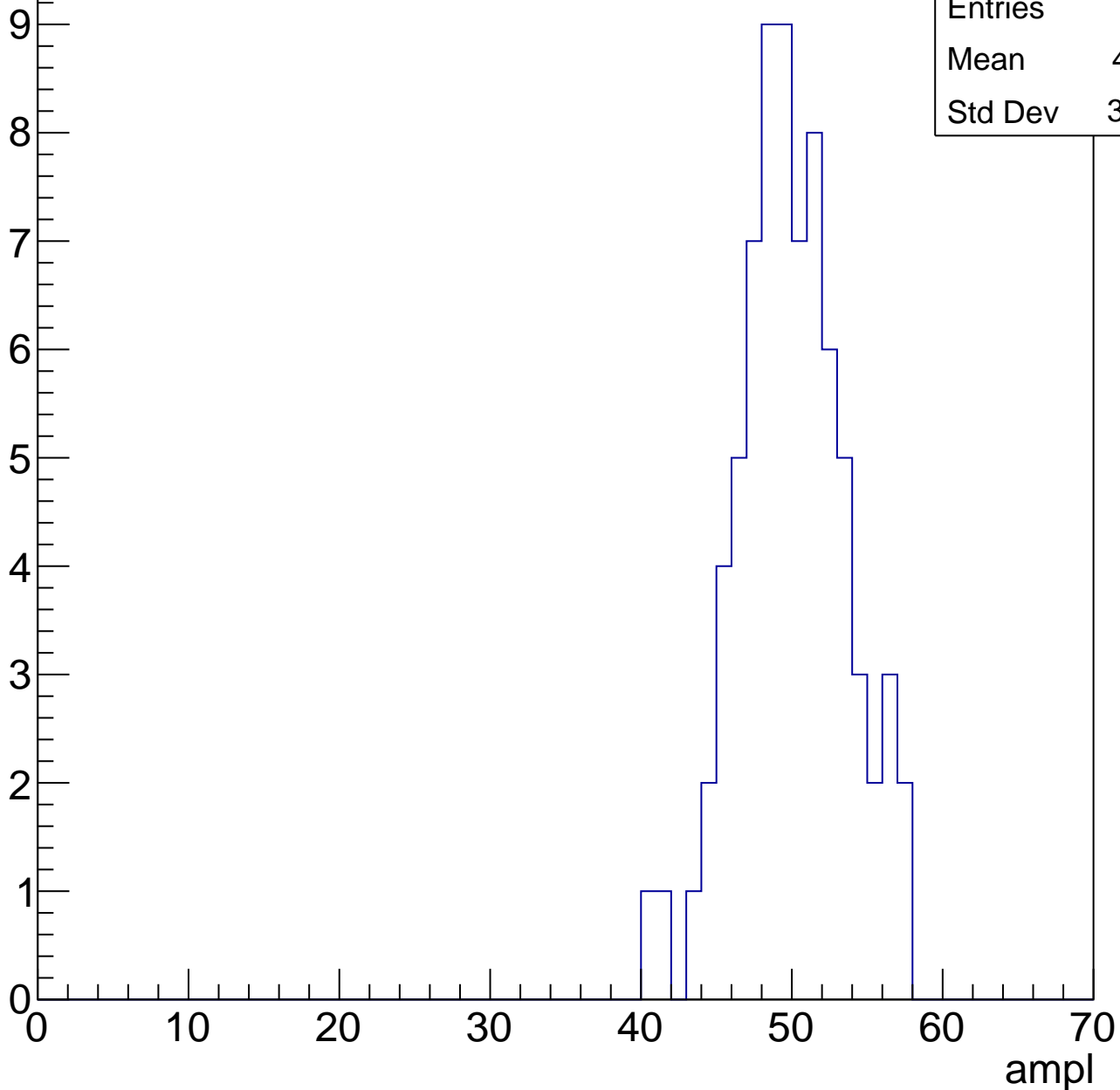


# B1L102S, U8-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	49.51
Std Dev	3.564

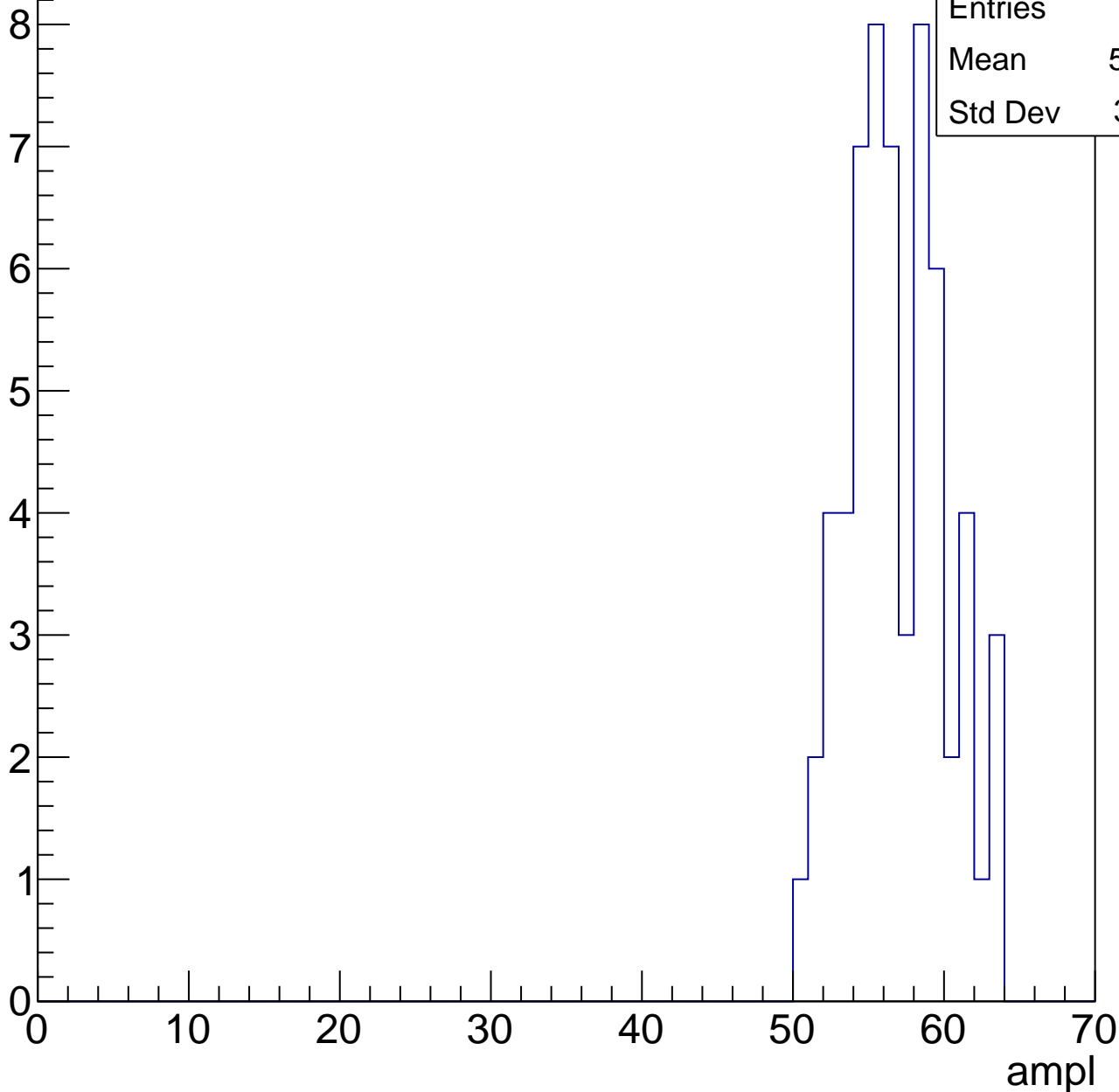


# B1L102S, U8-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	56.43
Std Dev	3.201

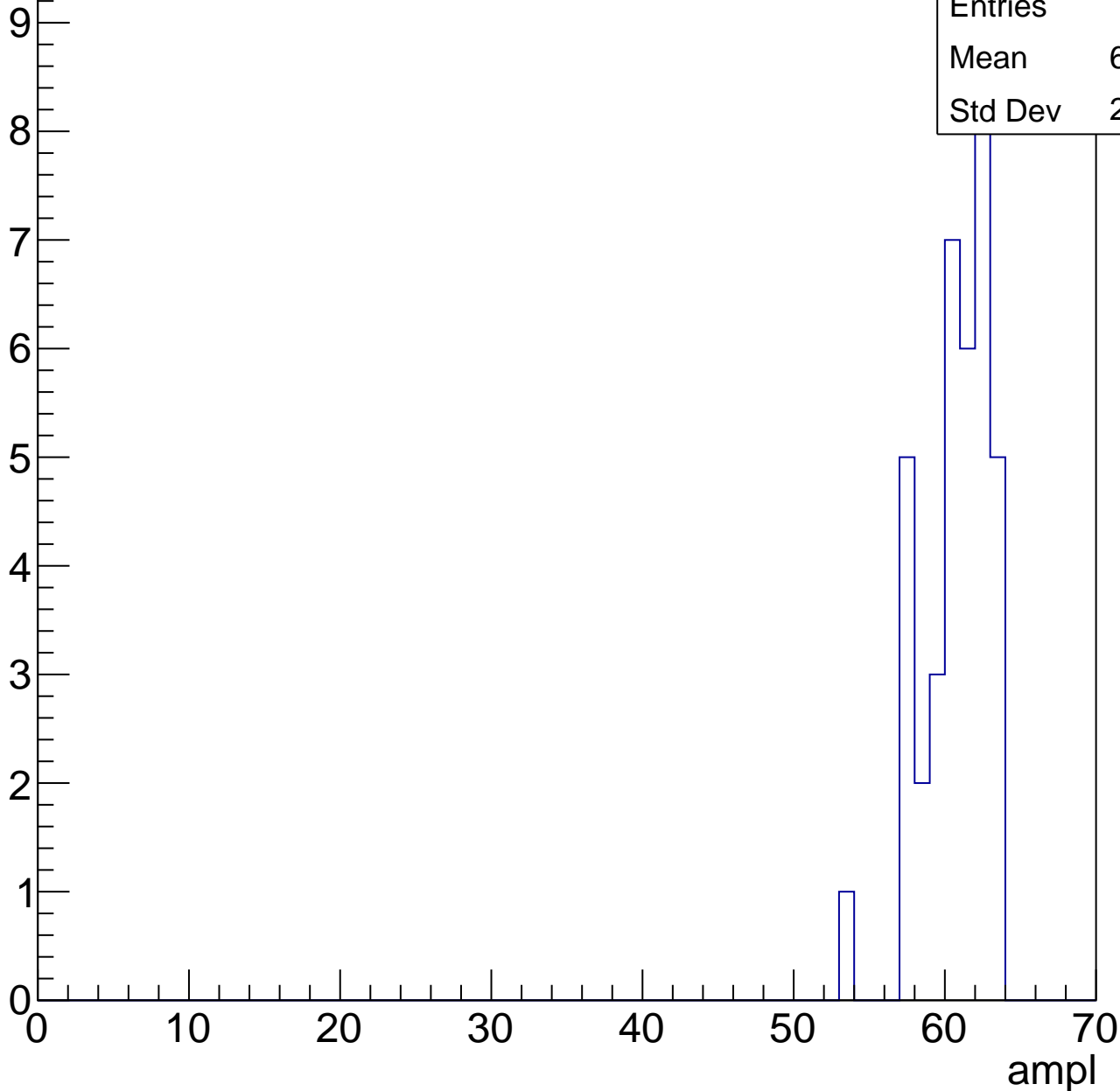


# B1L102S, U8-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

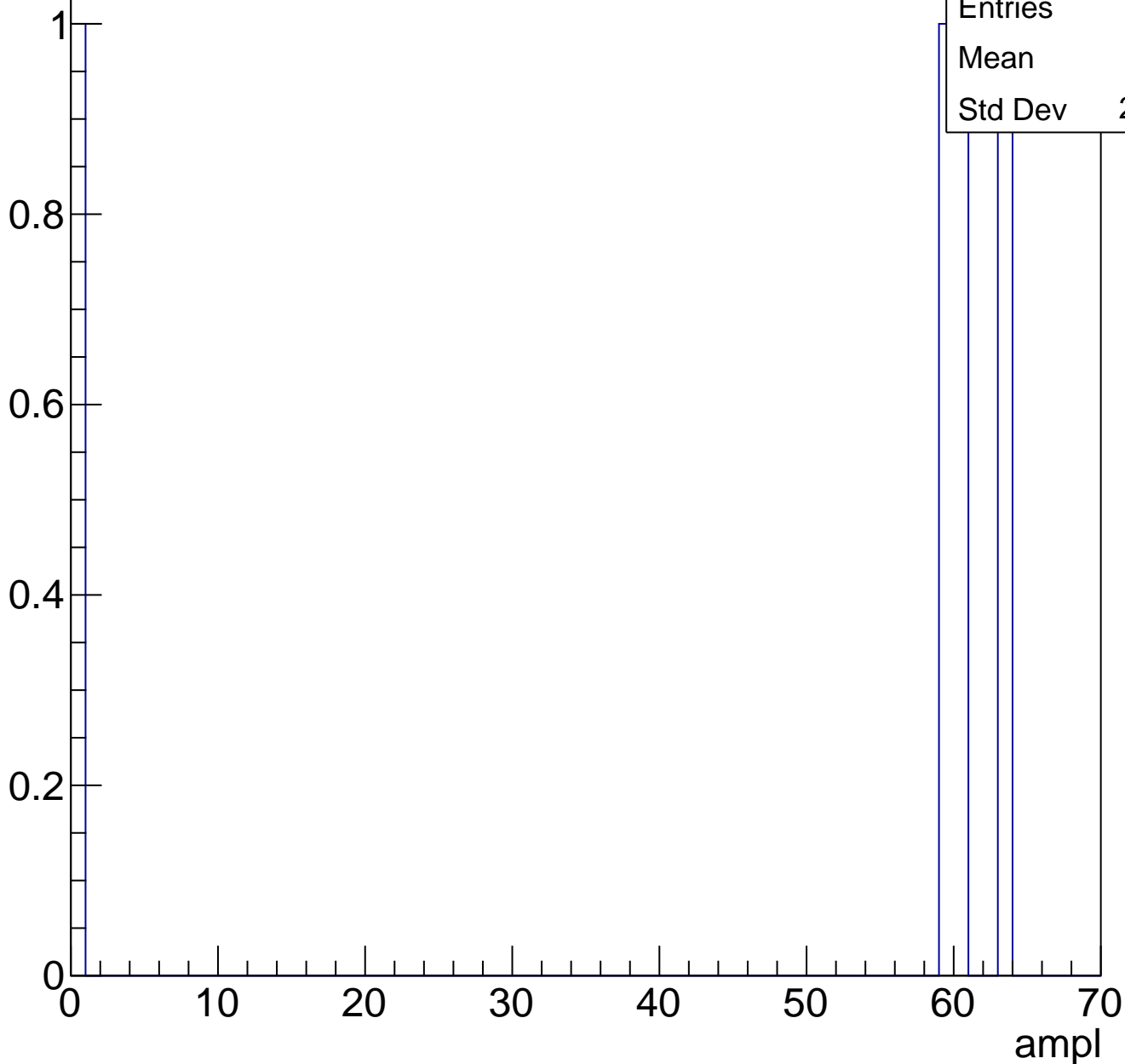
Entries	38
Mean	60.26
Std Dev	2.232



# B1L102S, U8-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch45, adc0

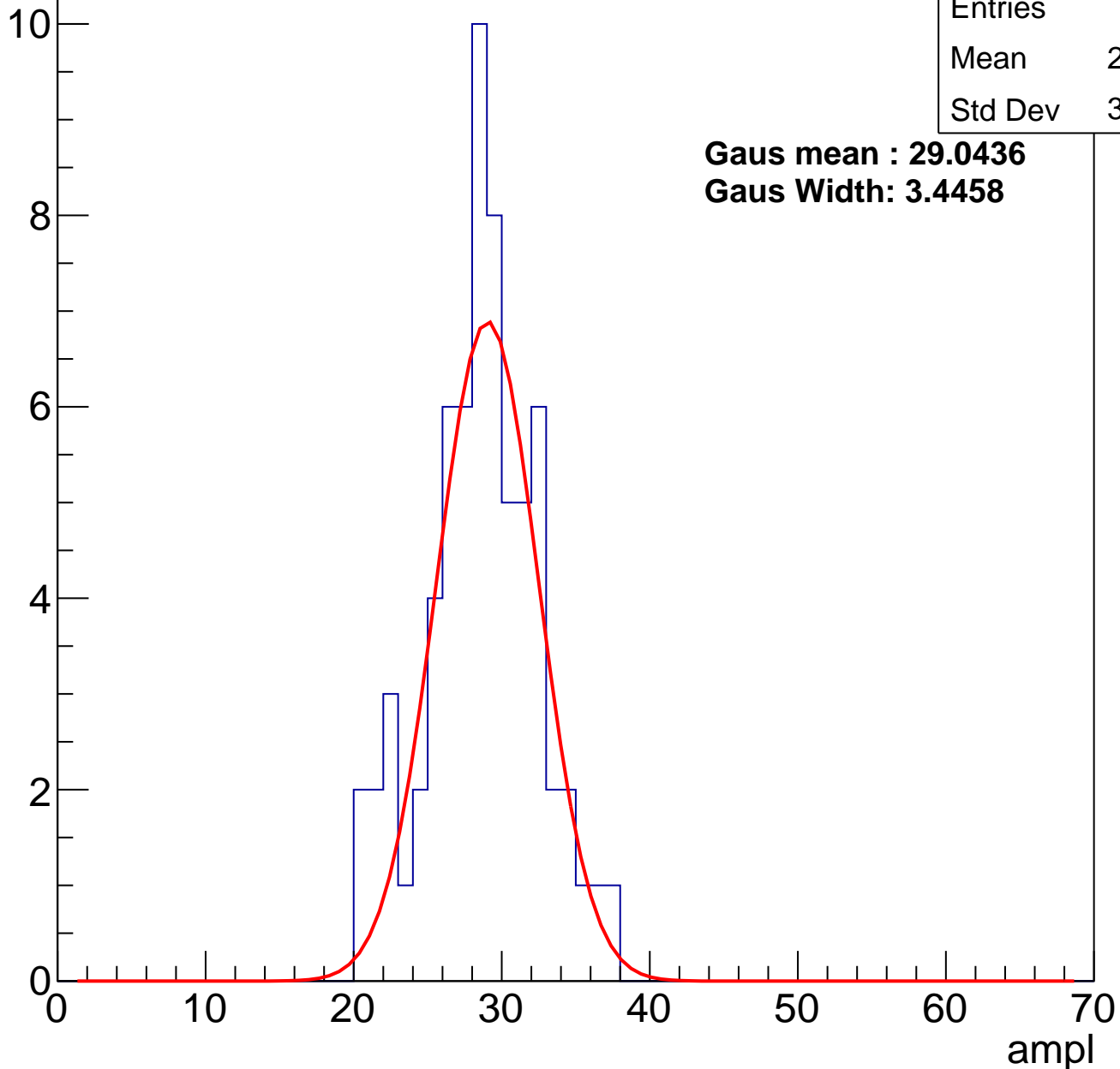
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	67
Mean	28.18
Std Dev	3.745

**Gaus mean : 29.0436**

**Gaus Width: 3.4458**

Entry



# B1L102S, U8-ch45, adc1

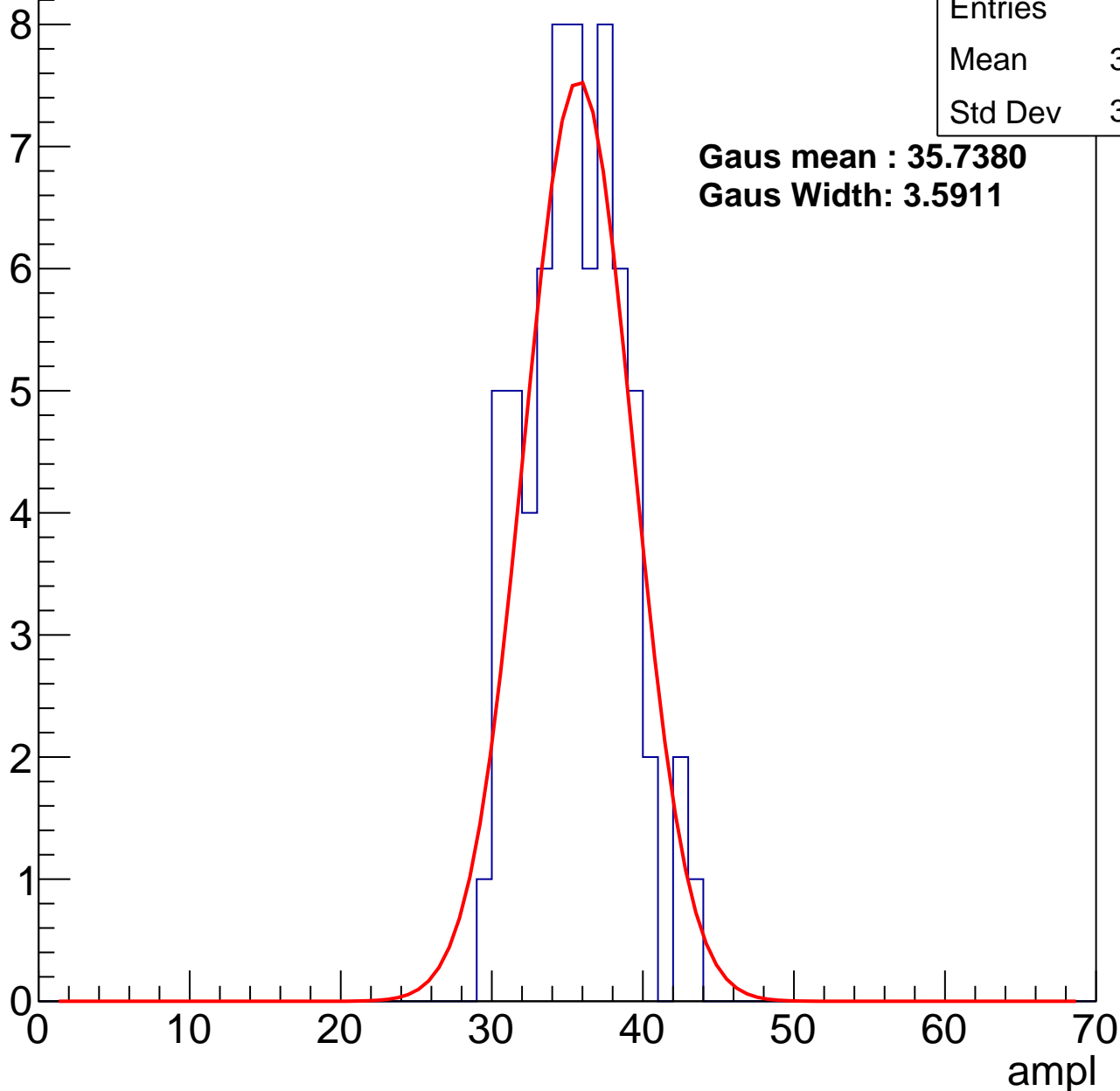
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	35.13
Std Dev	3.213

**Gaus mean : 35.7380**

**Gaus Width: 3.5911**



# B1L102S, U8-ch45, adc2

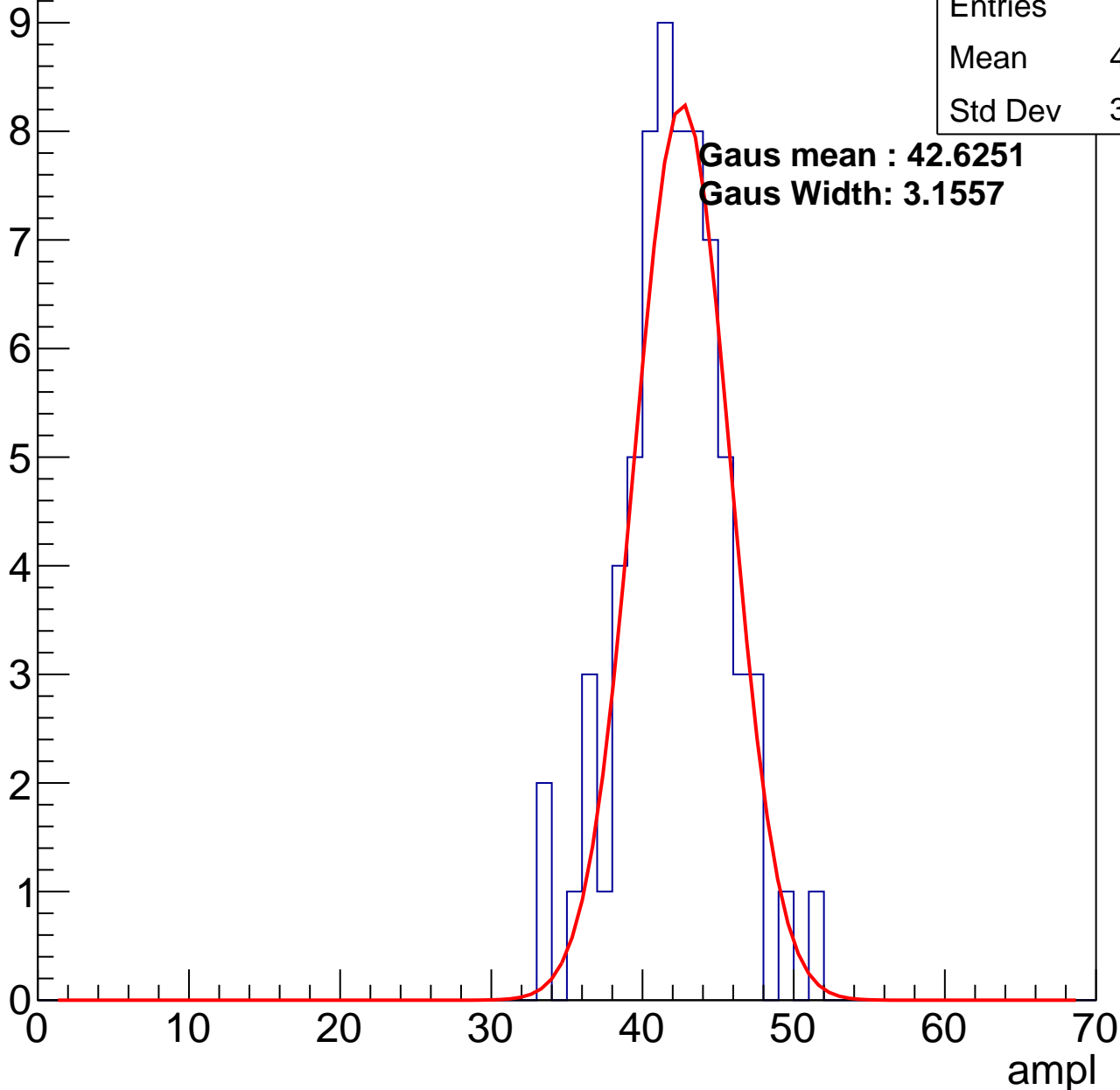
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	41.65
Std Dev	3.447

**Gaus mean : 42.6251**

**Gaus Width: 3.1557**

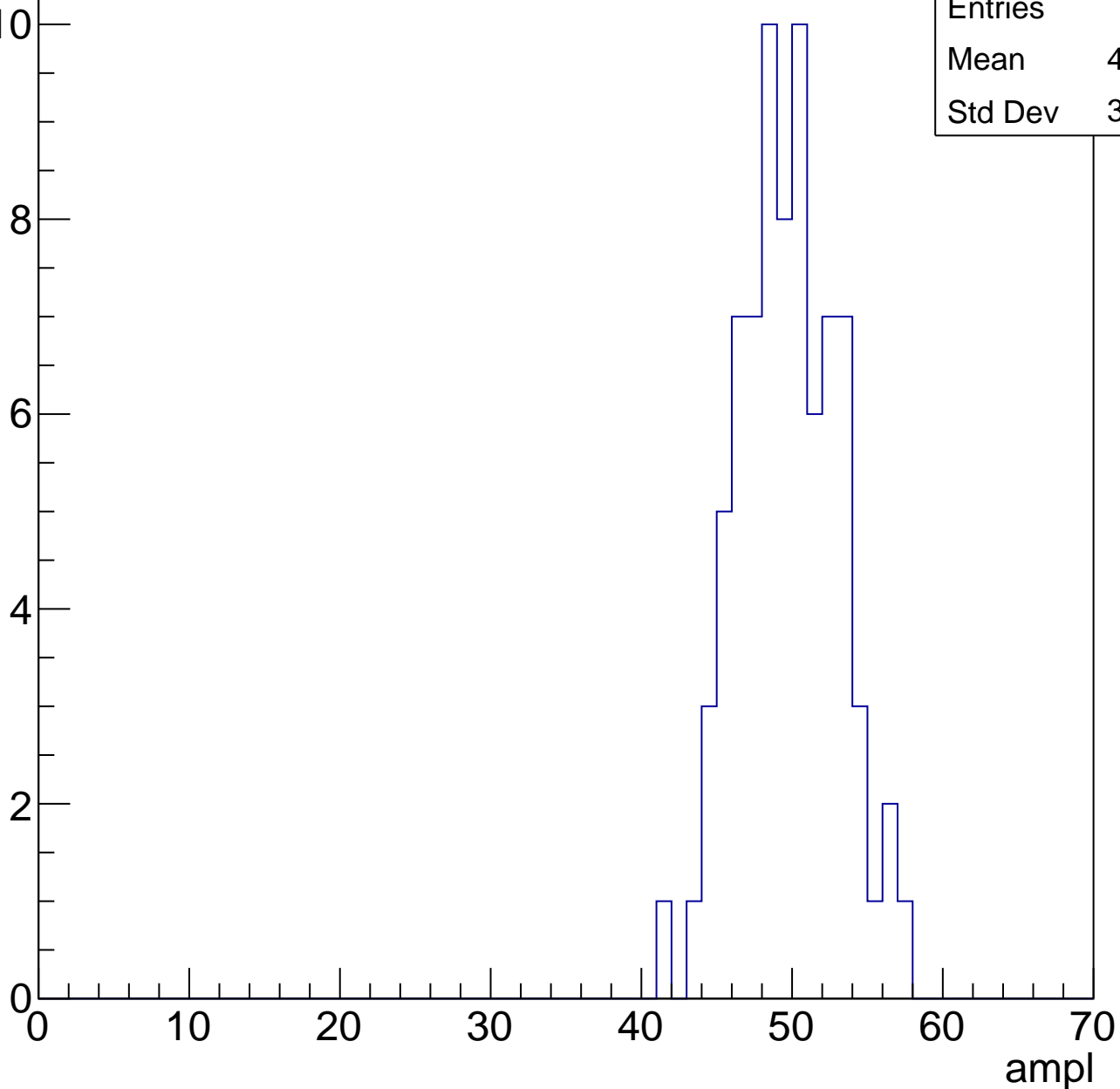


# B1L102S, U8-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	49.25
Std Dev	3.247

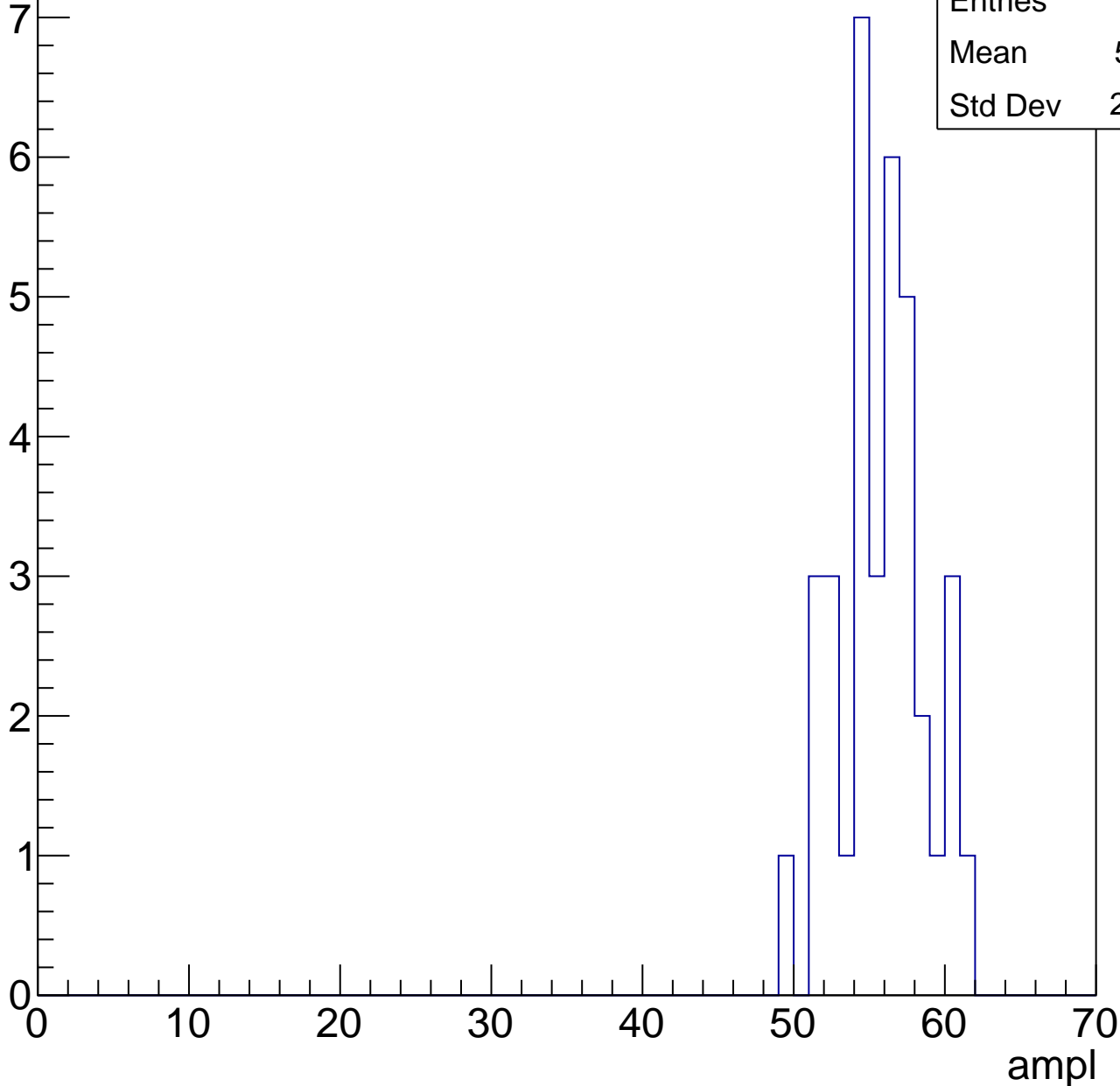


# B1L102S, U8-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	36
Mean	55.31
Std Dev	2.836



# B1L102S, U8-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

10

8

6

4

2

0

Entries	62
Mean	59.31
Std Dev	2.631

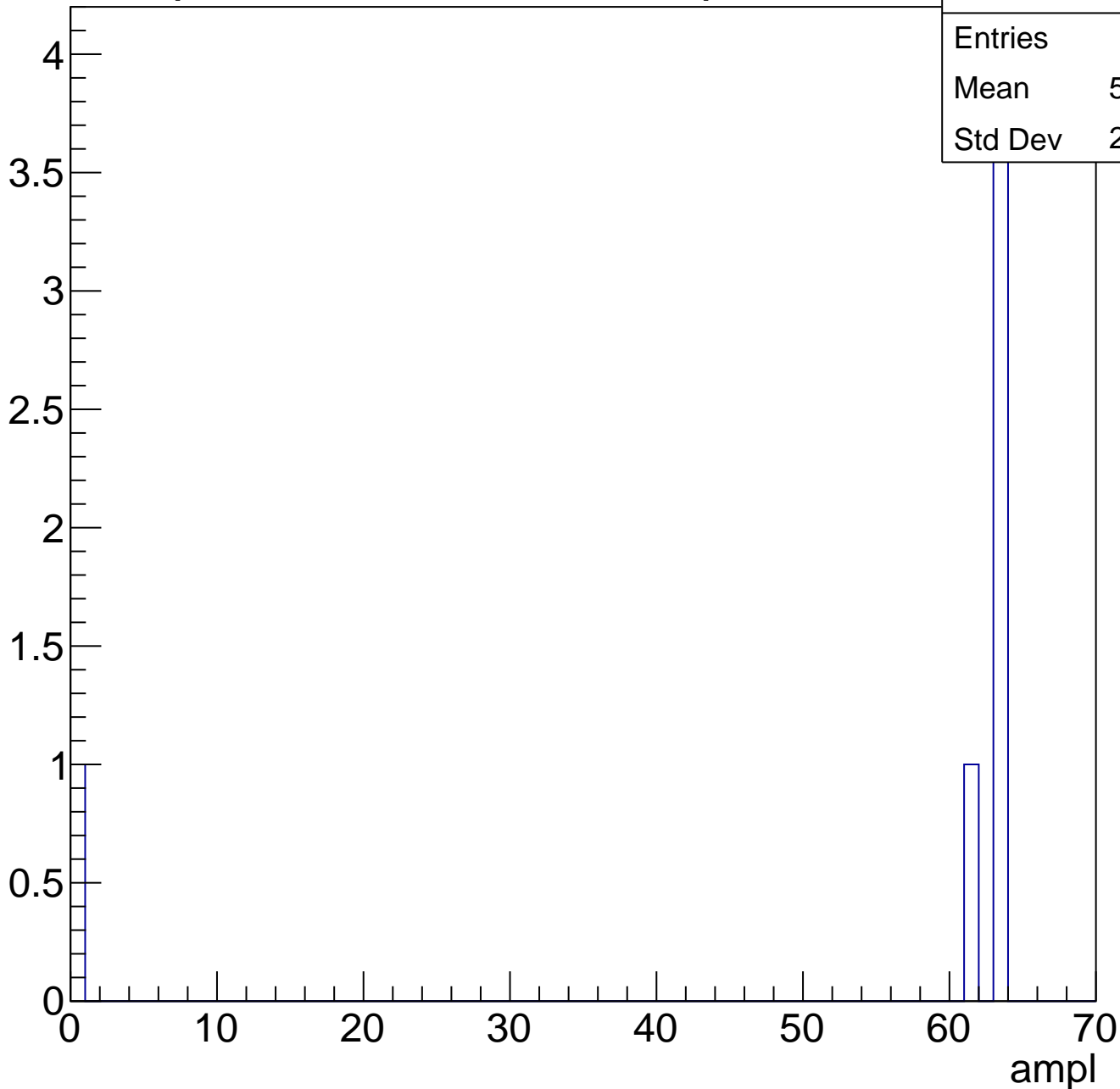
ampl

0 10 20 30 40 50 60 70

# B1L102S, U8-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch46, adc0

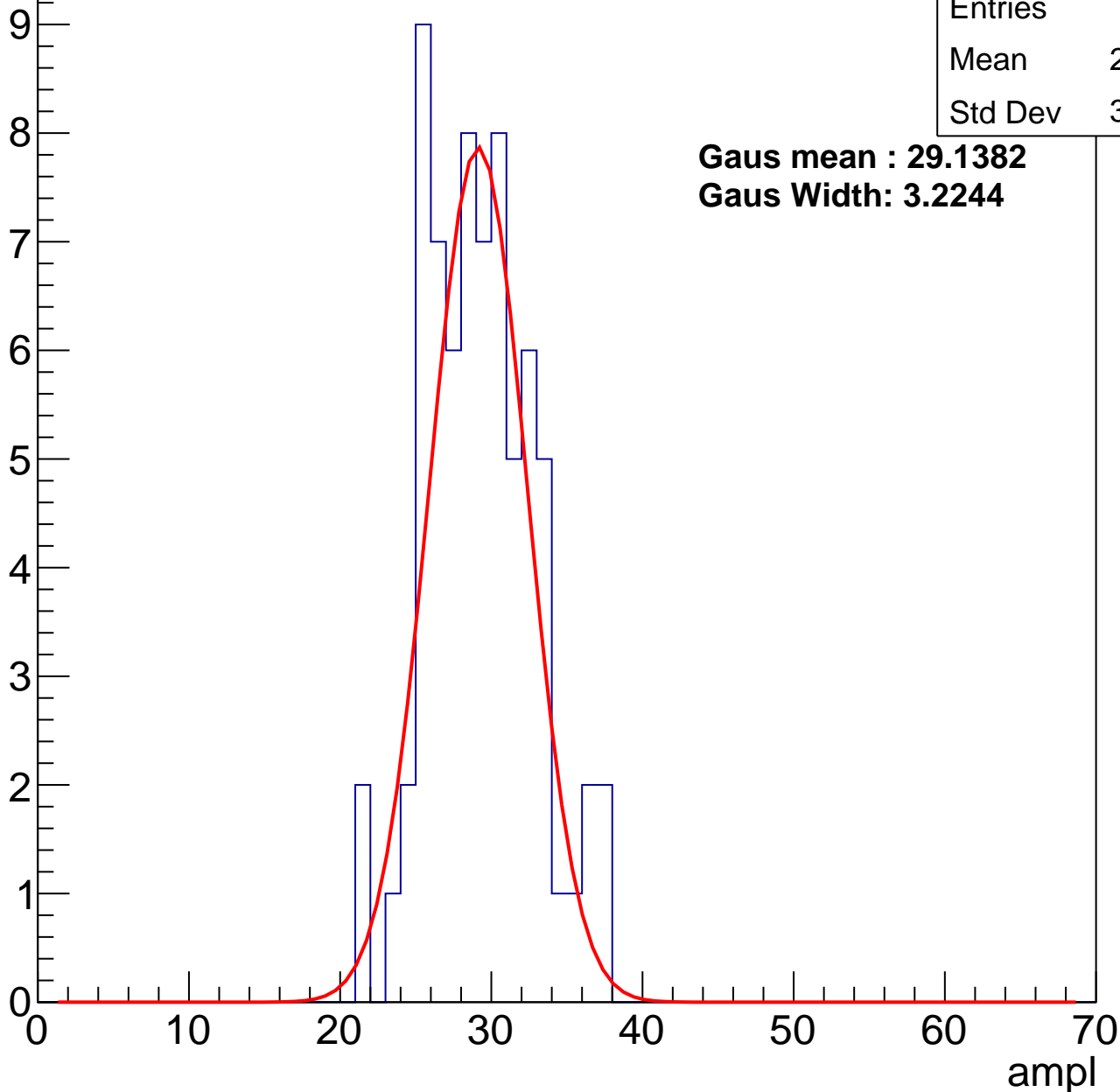
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	28.83
Std Dev	3.536

**Gaus mean : 29.1382**

**Gaus Width: 3.2244**



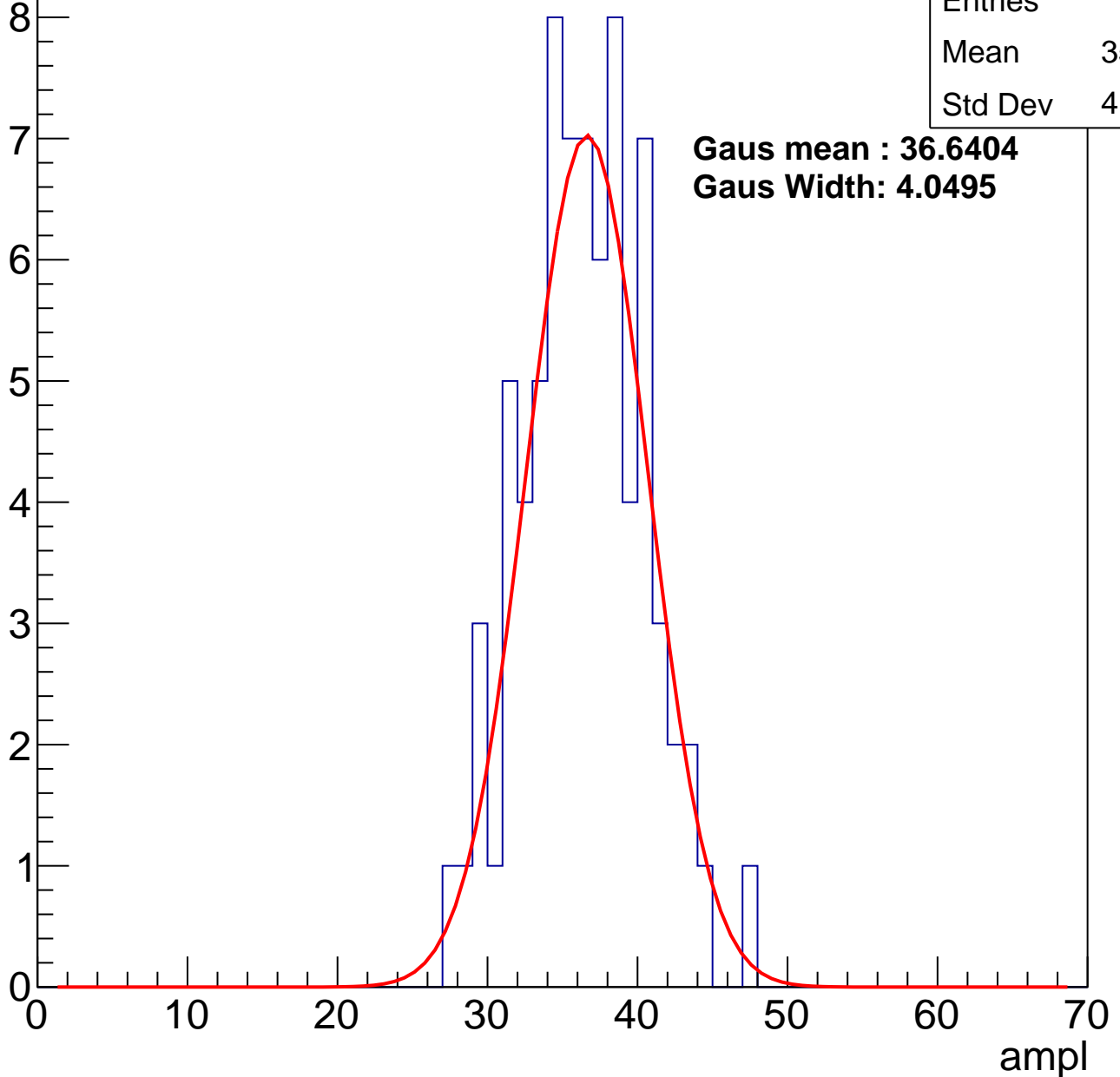
# B1L102S, U8-ch46, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	35.99
Std Dev	4.002

**Gaus mean : 36.6404**  
**Gaus Width: 4.0495**



# B1L102S, U8-ch46, adc2

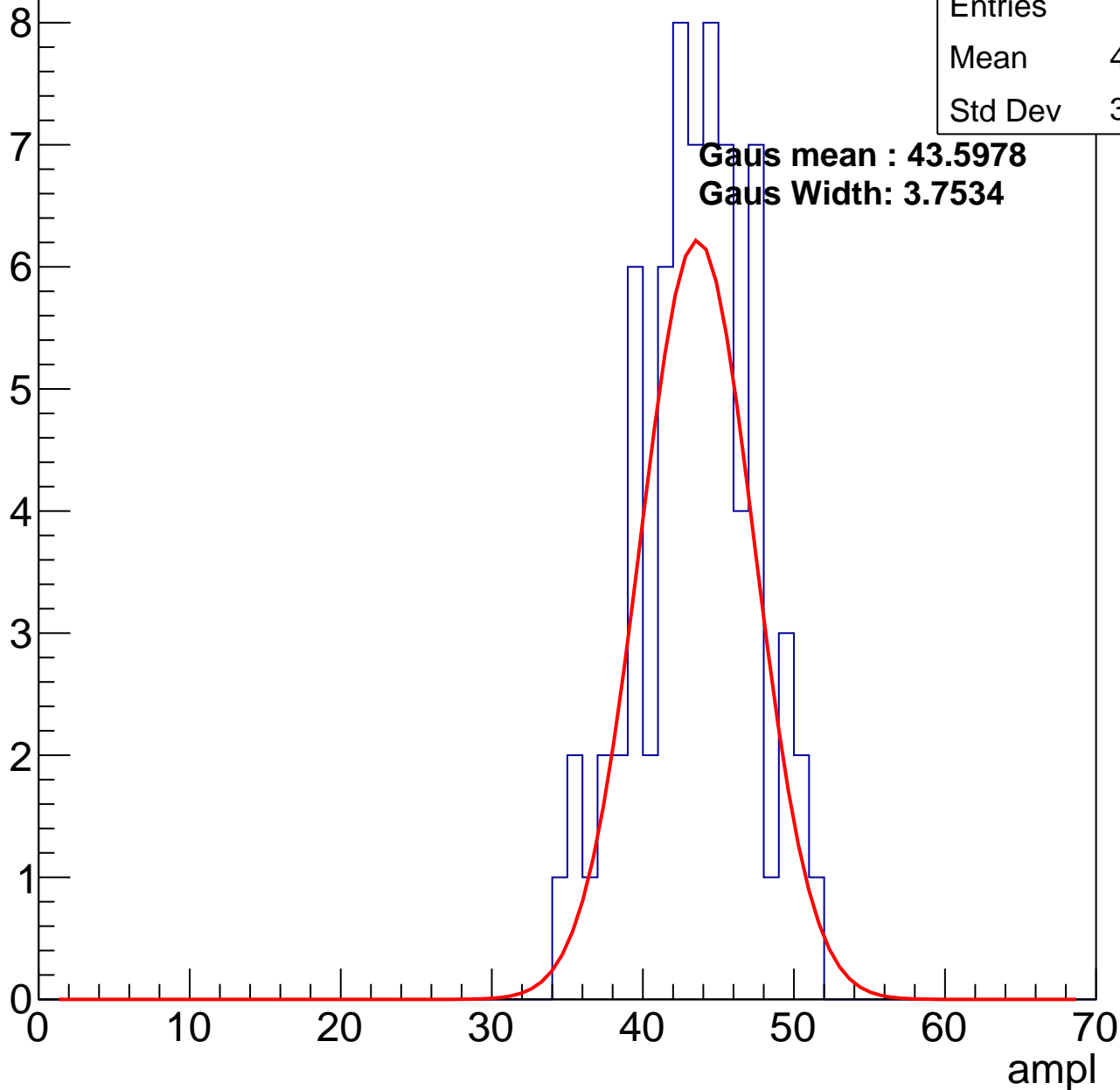
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	43.04
Std Dev	3.789

**Gaus mean : 43.5978**

**Gaus Width: 3.7534**

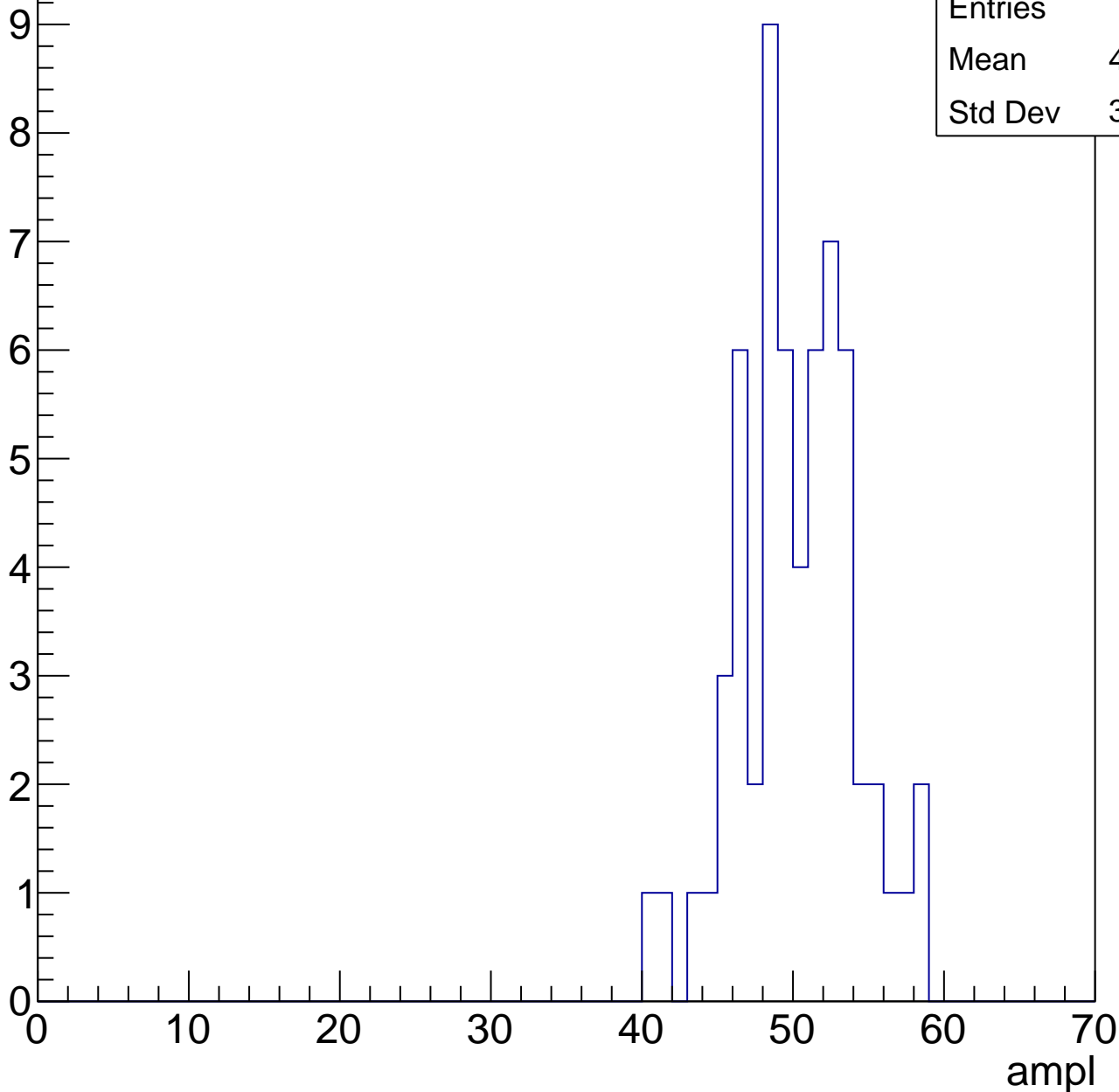


# B1L102S, U8-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

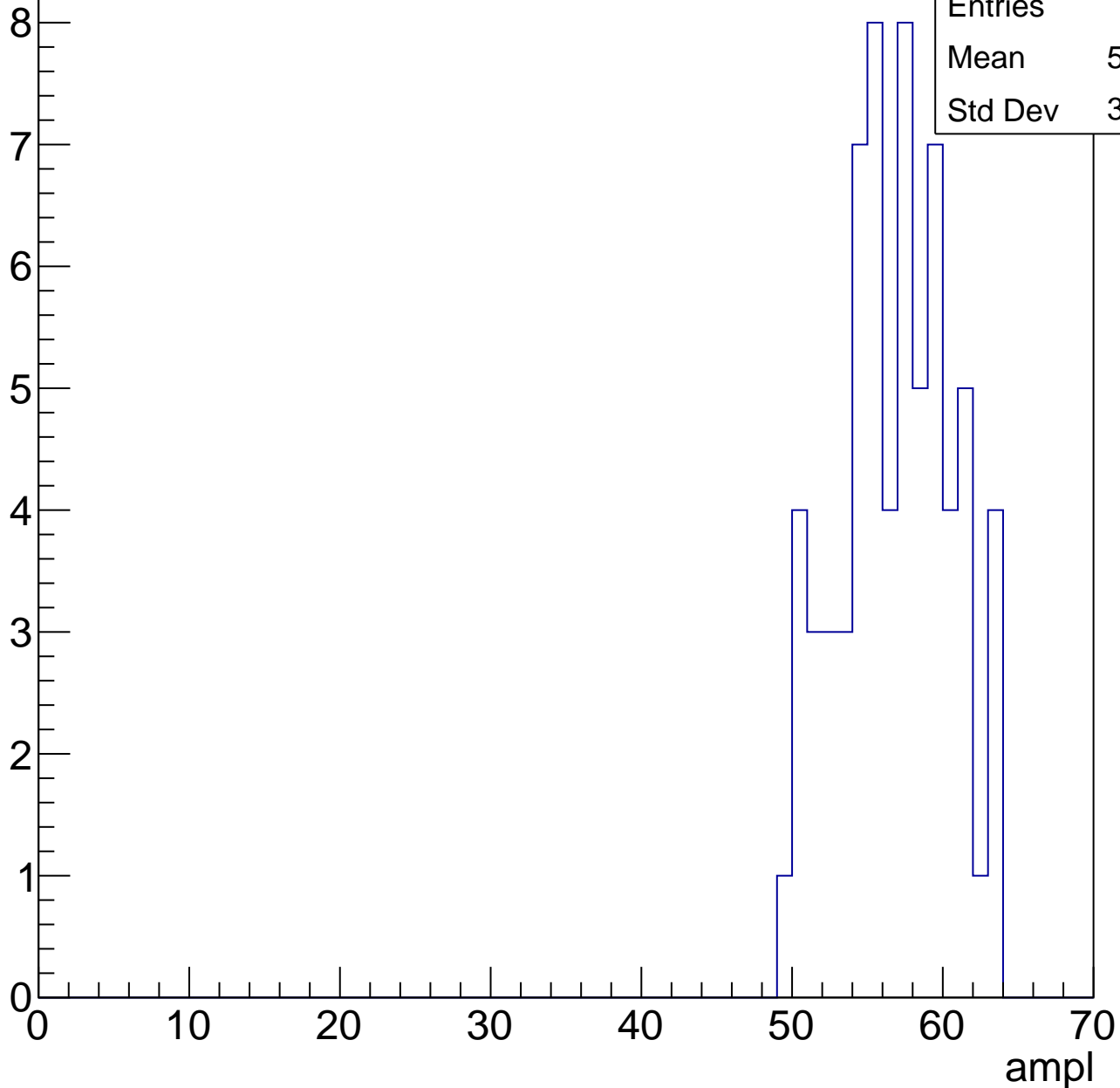
Entries	61
Mean	49.74
Std Dev	3.789



# B1L102S, U8-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



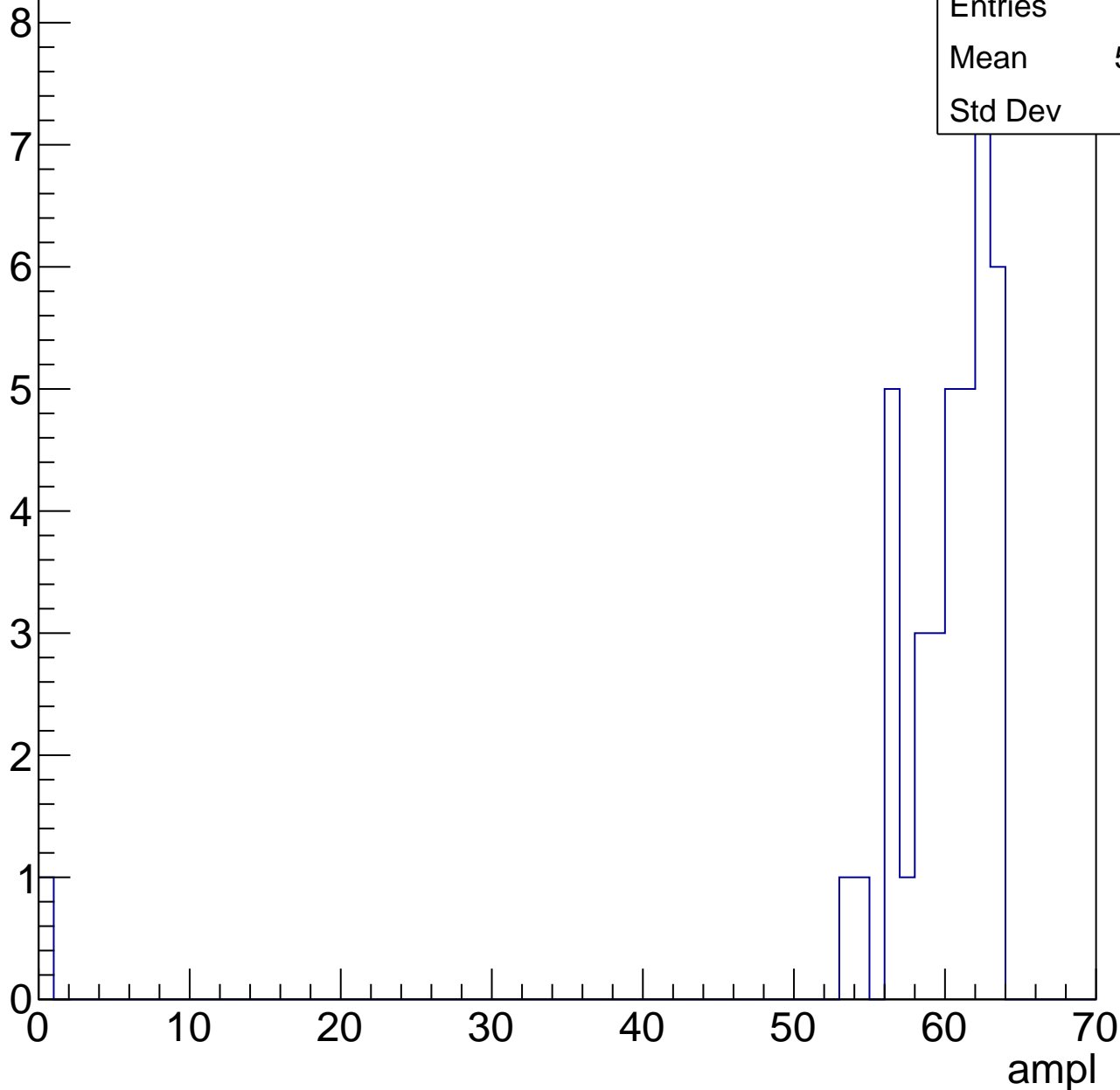
Entries	67
Mean	56.37
Std Dev	3.628

# B1L102S, U8-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	39
Mean	58.31
Std Dev	9.83



# B1L102S, U8-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch47, adc0

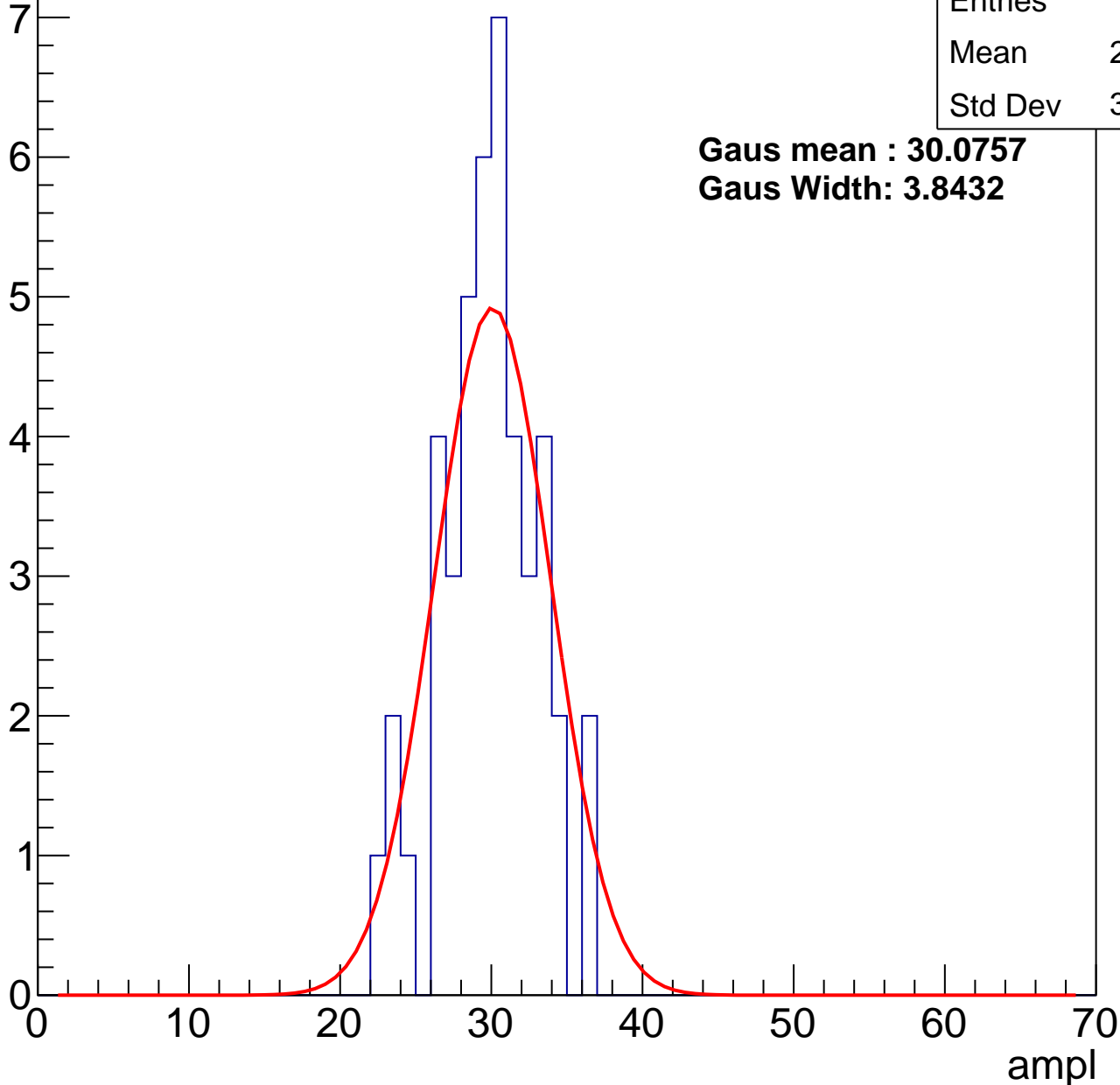
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	44
Mean	29.39
Std Dev	3.214

**Gaus mean : 30.0757**

**Gaus Width: 3.8432**



# B1L102S, U8-ch47, adc1

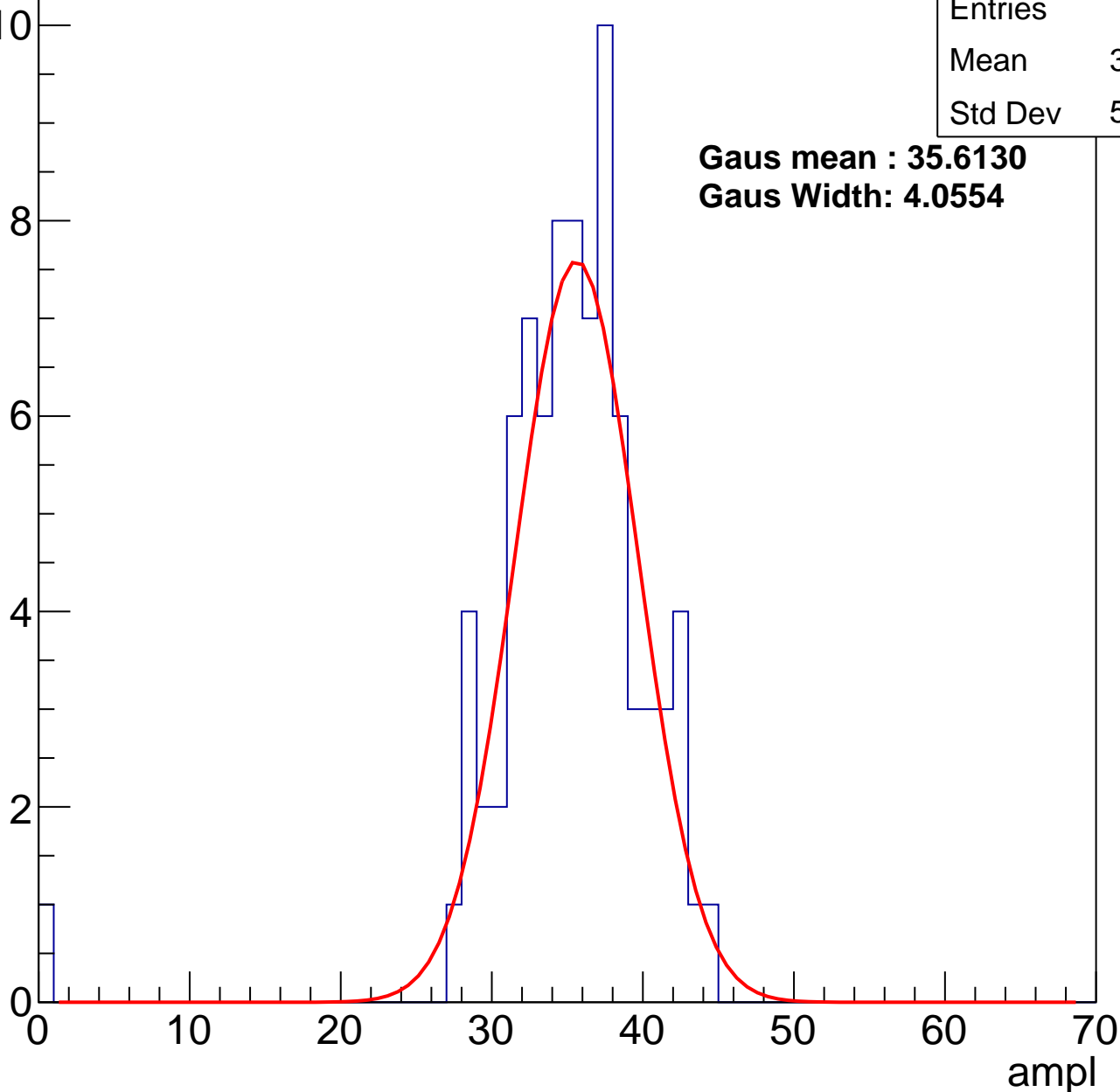
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	83
Mean	34.72
Std Dev	5.449

**Gaus mean : 35.6130**

**Gaus Width: 4.0554**



# B1L102S, U8-ch47, adc2

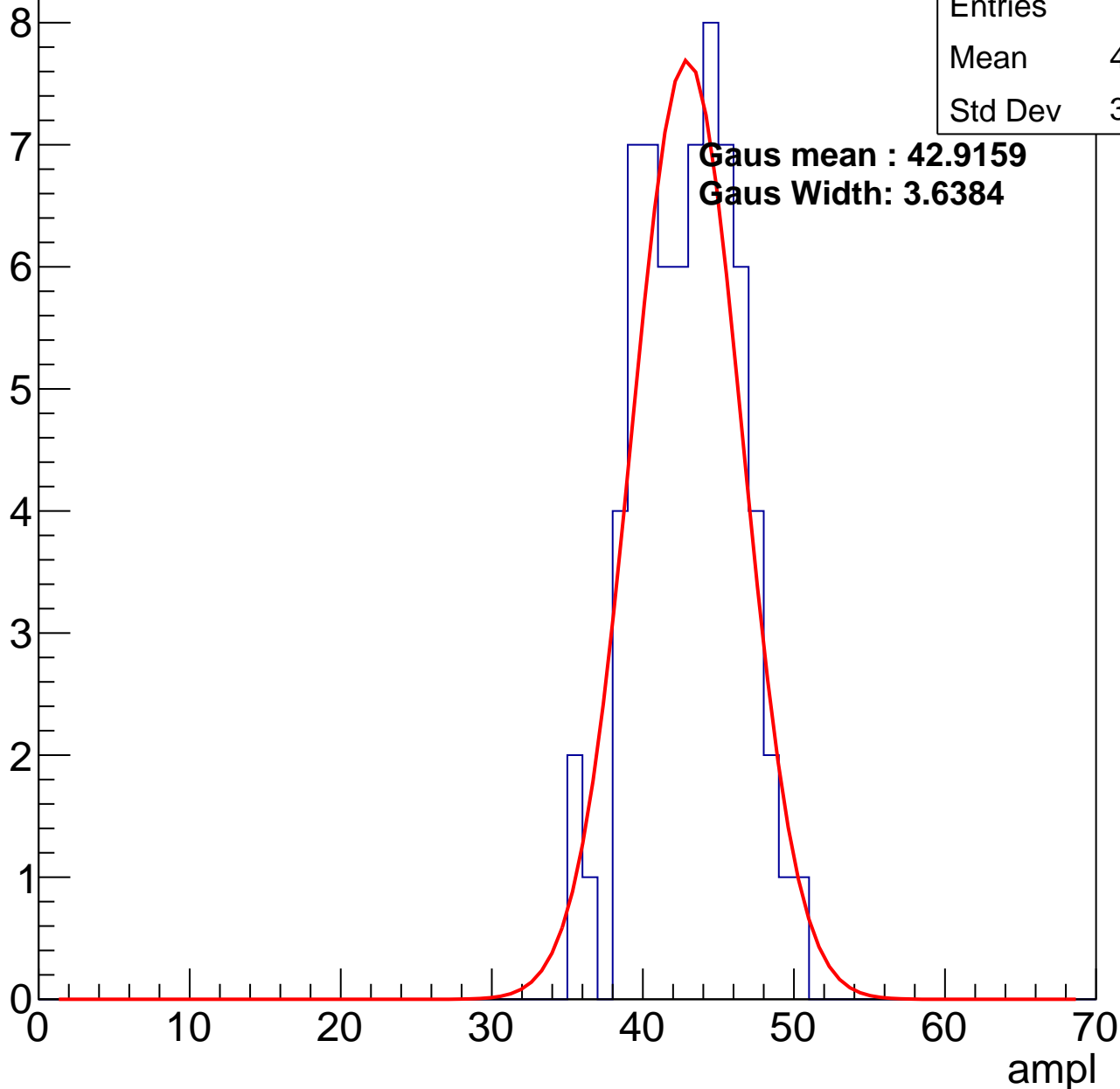
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	42.55
Std Dev	3.312

**Gaus mean : 42.9159**

**Gaus Width: 3.6384**

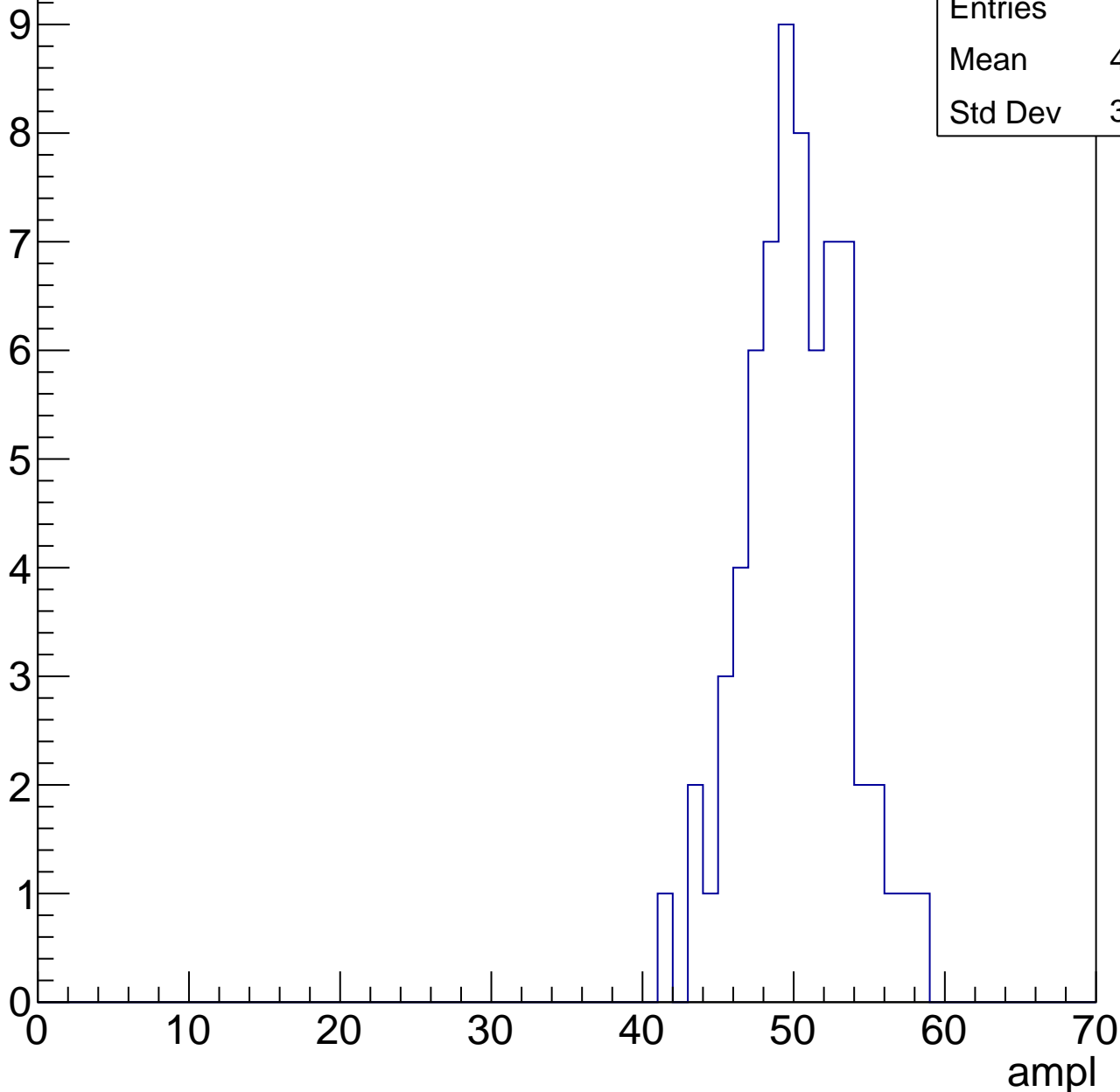


# B1L102S, U8-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	49.69
Std Dev	3.357

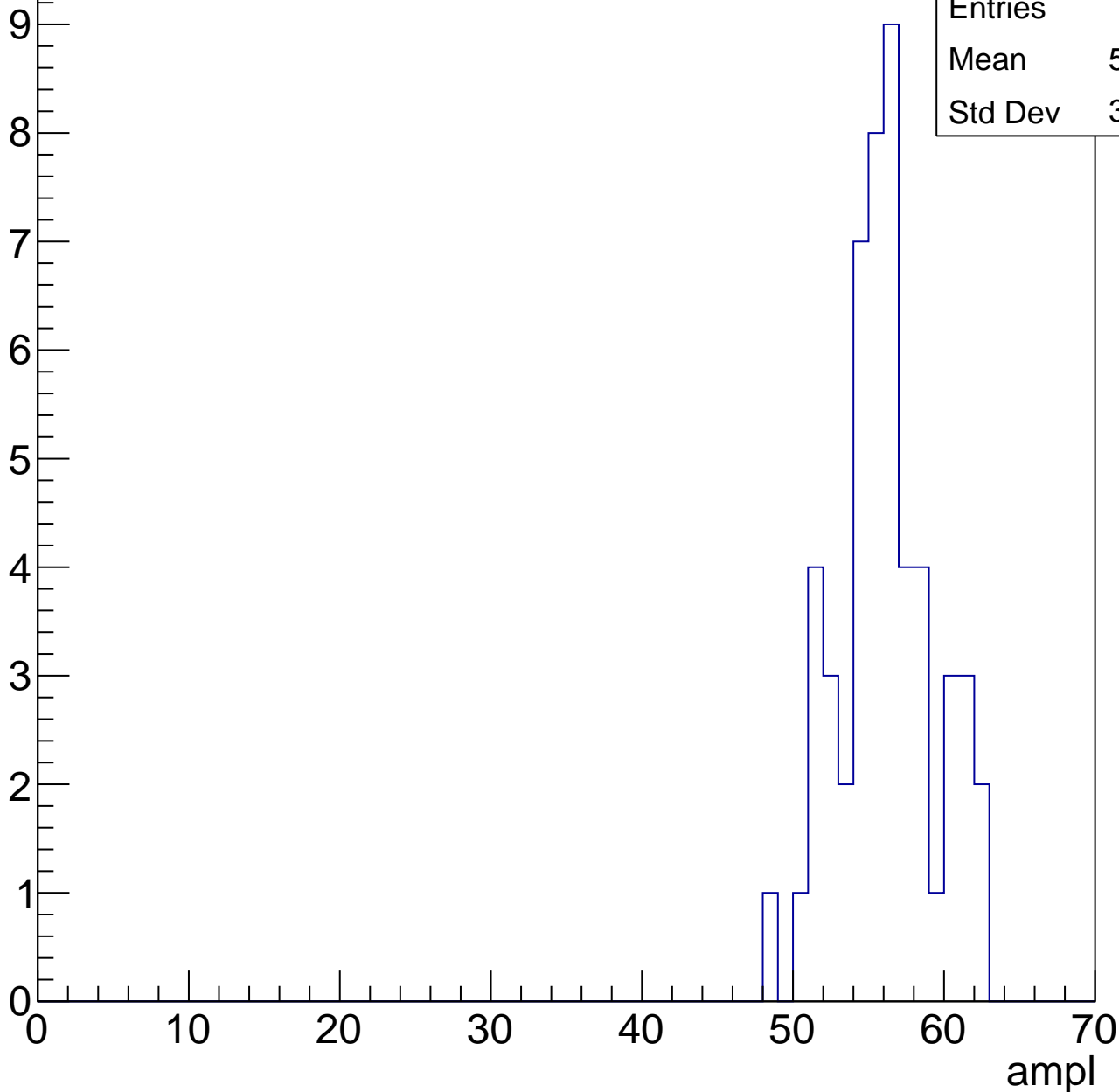


# B1L102S, U8-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	55.62
Std Dev	3.157



# B1L102S, U8-ch47, adc5

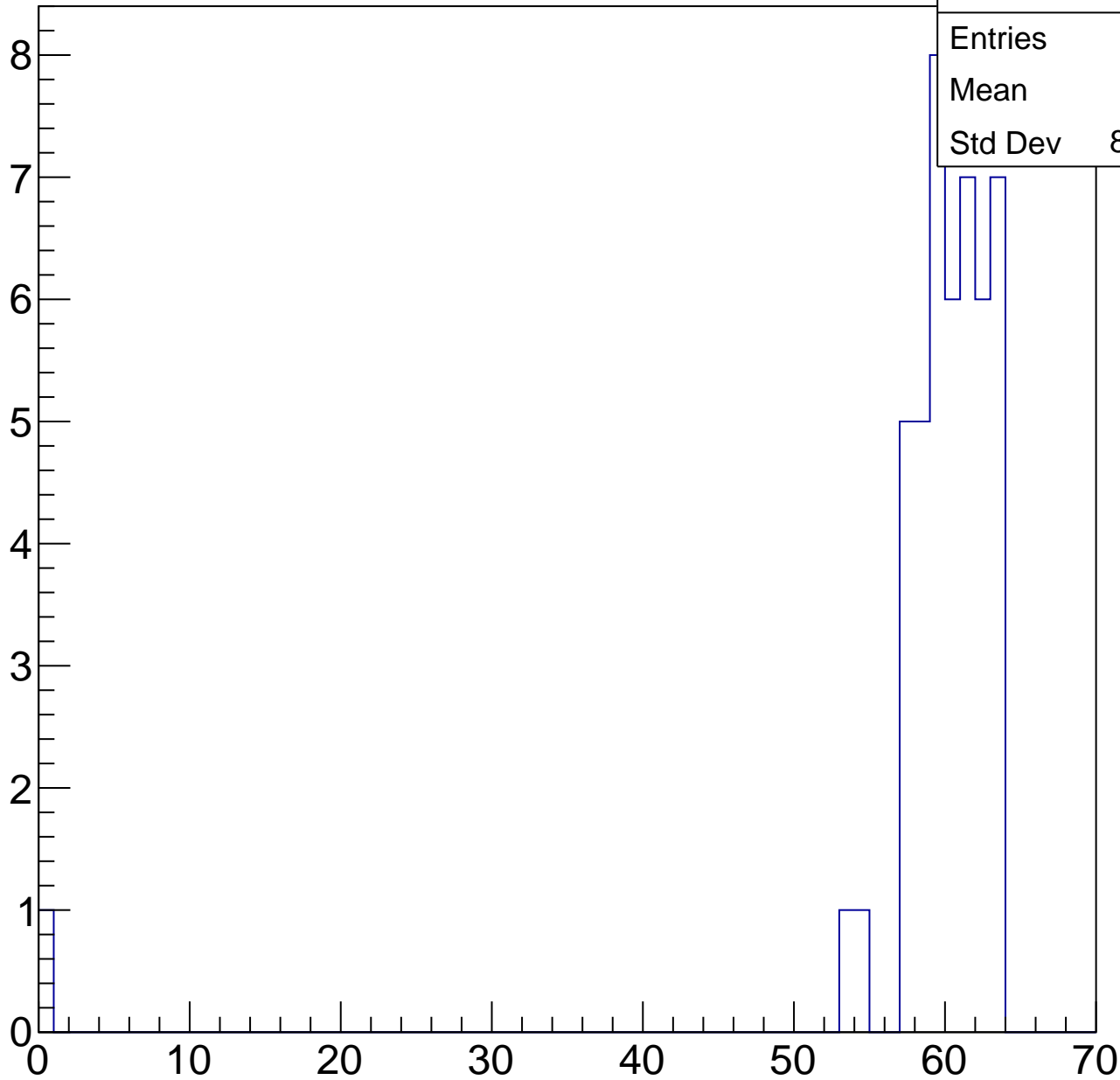
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	47
Mean	58.6
Std Dev	8.943

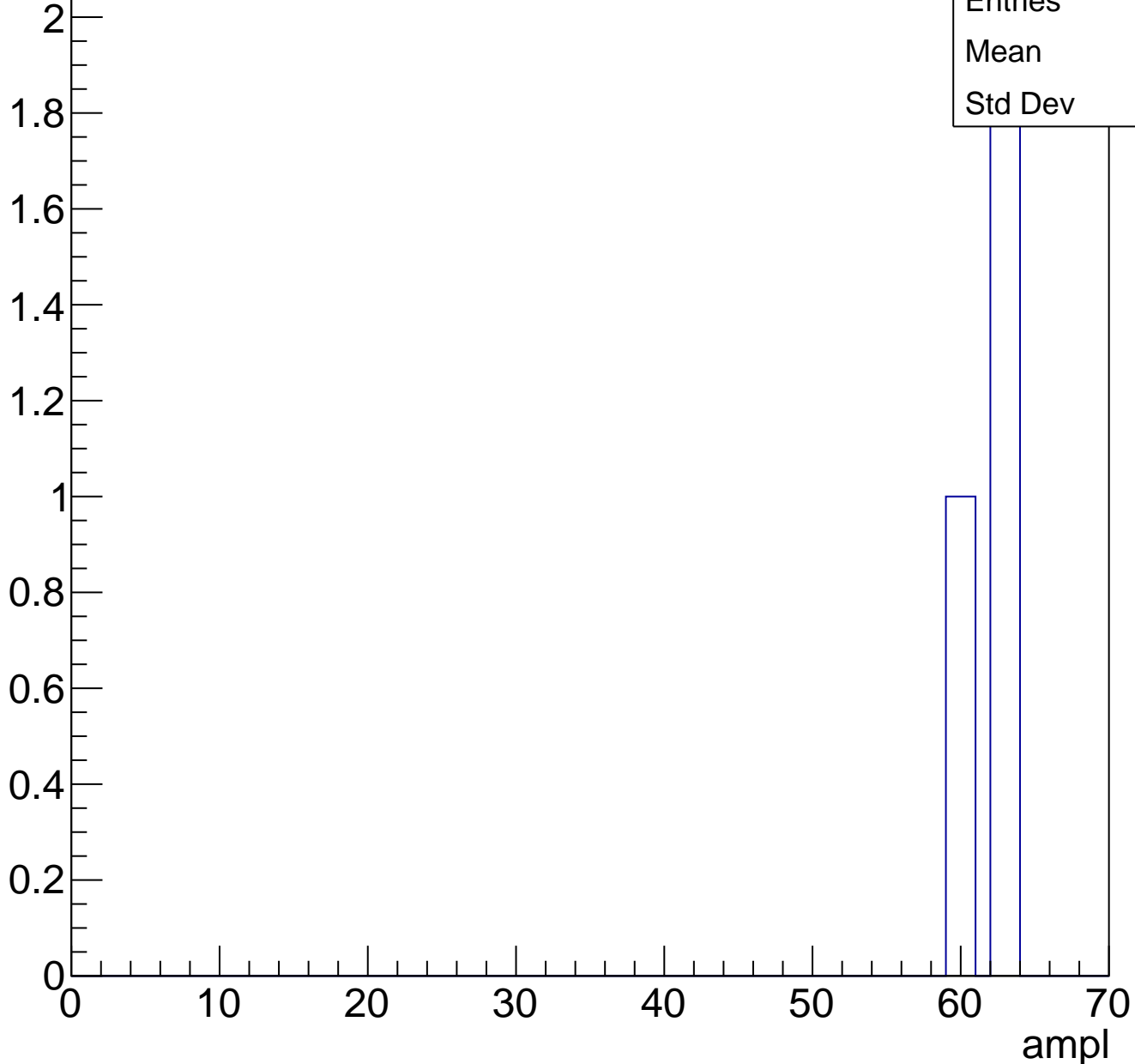
ampl



# B1L102S, U8-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch48, adc0

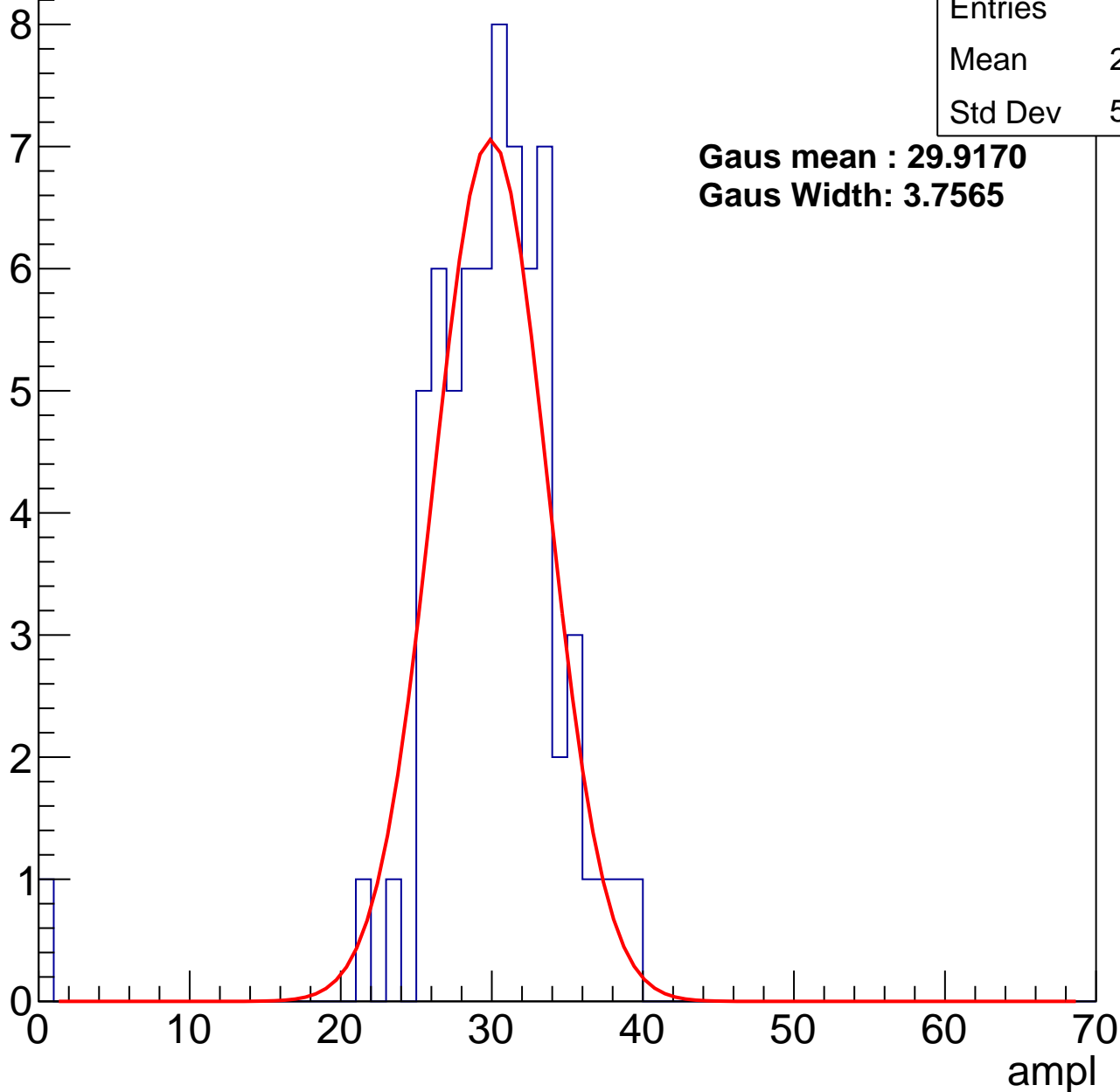
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	29.49
Std Dev	5.057

**Gaus mean : 29.9170**

**Gaus Width: 3.7565**



# B1L102S, U8-ch48, adc1

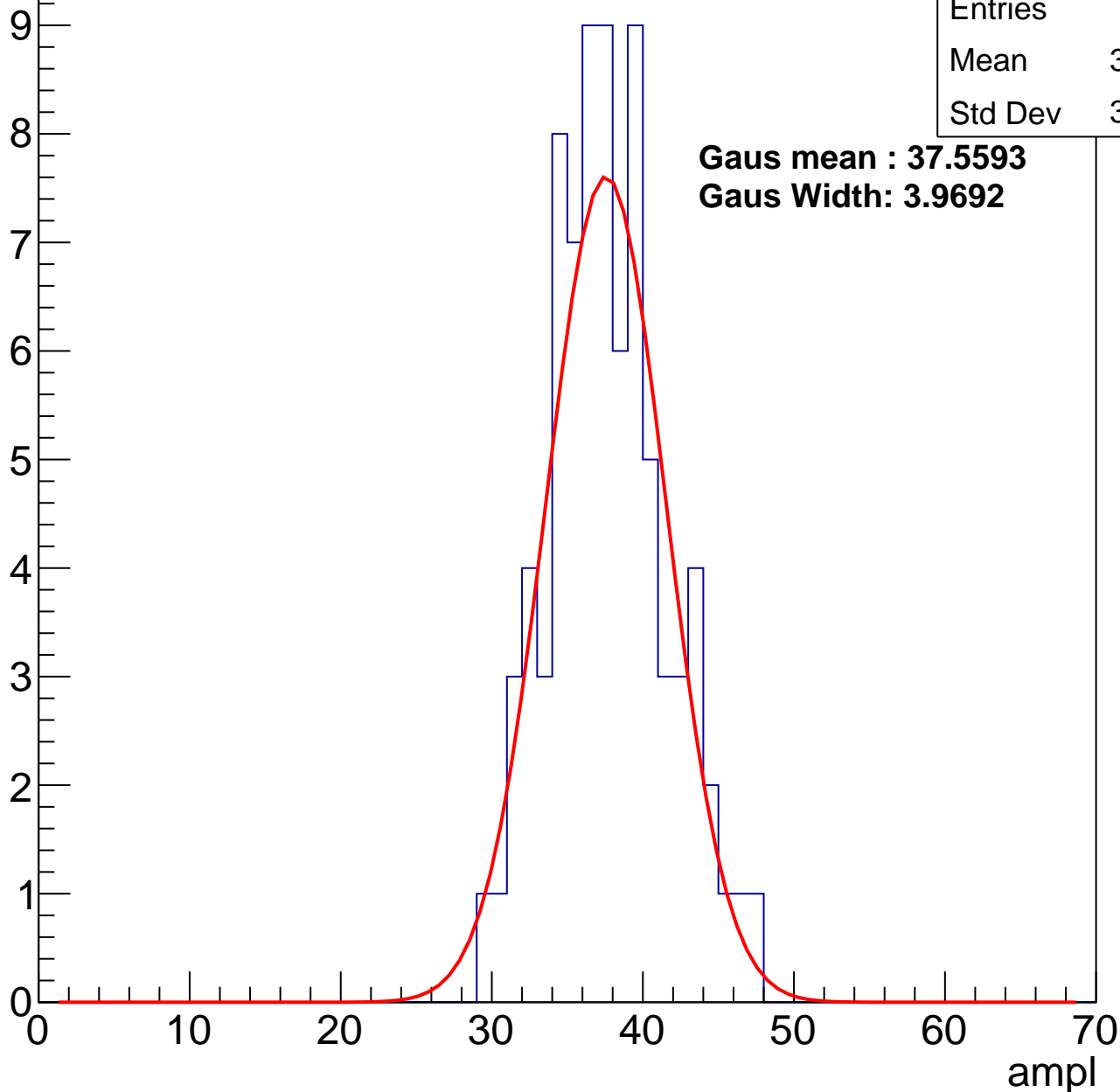
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	37.24
Std Dev	3.825

**Gaus mean : 37.5593**

**Gaus Width: 3.9692**



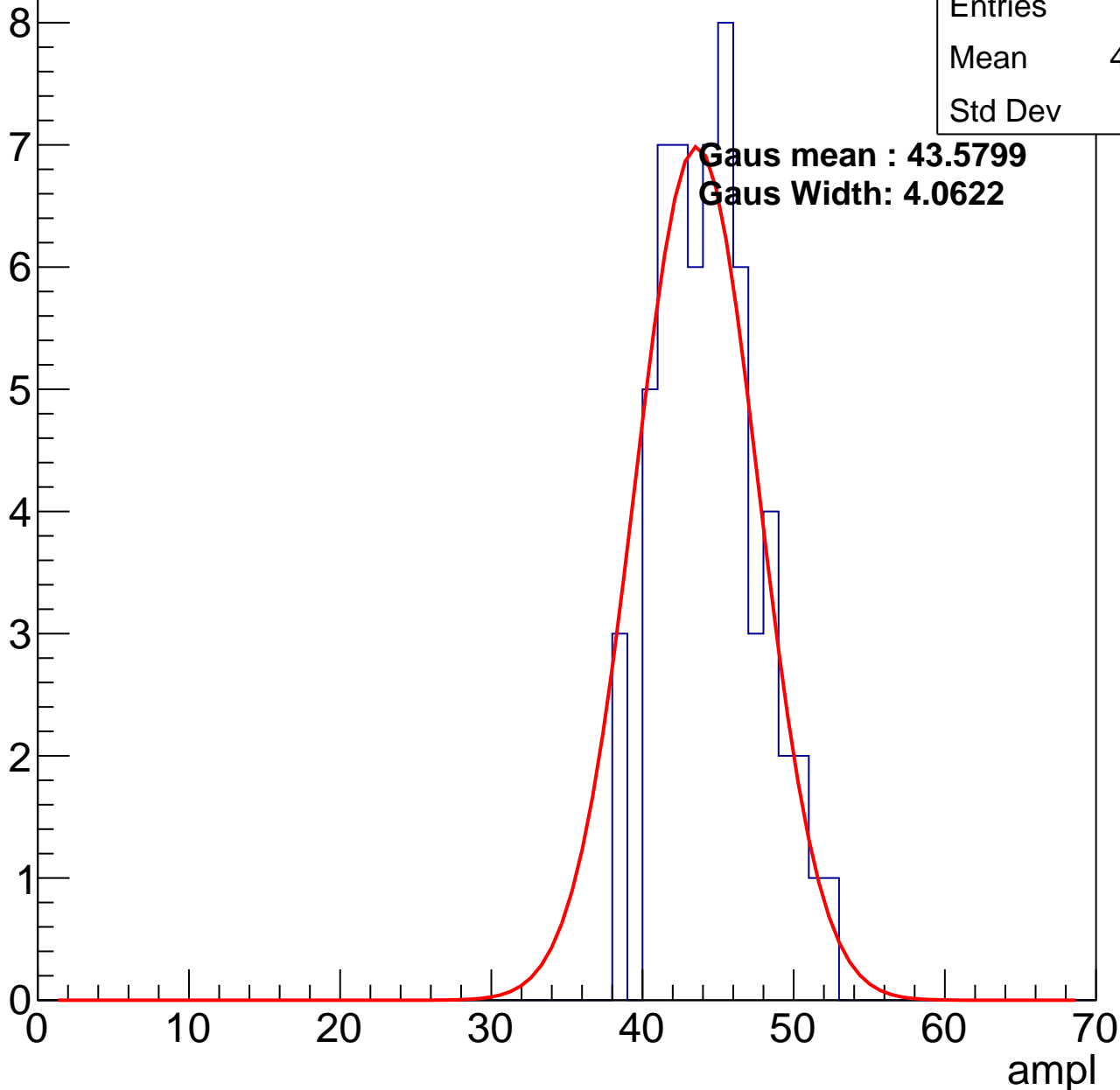
# B1L102S, U8-ch48, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	44.05
Std Dev	3.22

**Gaus mean : 43.5799**  
**Gaus Width: 4.0622**

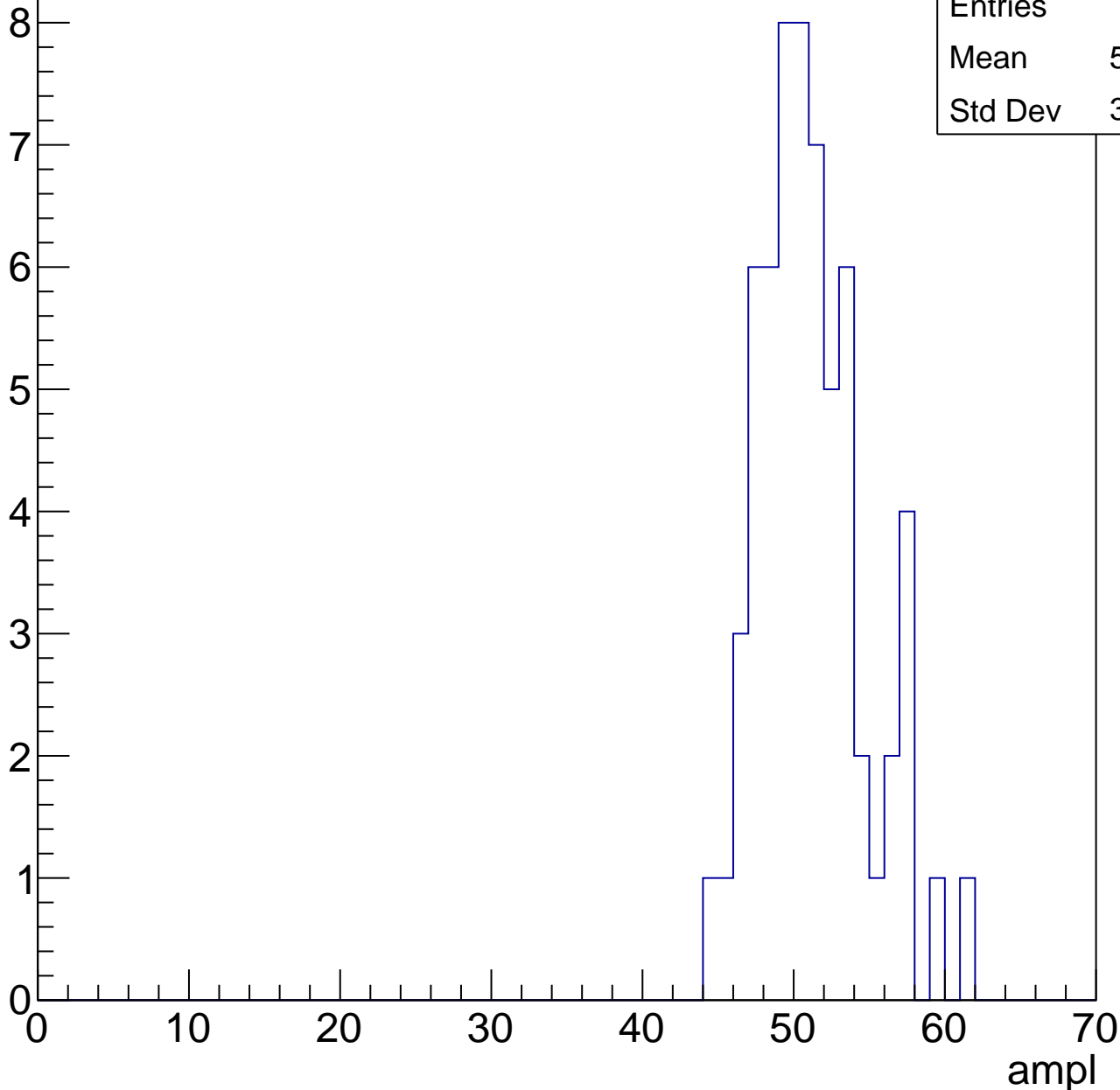


# B1L102S, U8-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	50.76
Std Dev	3.518

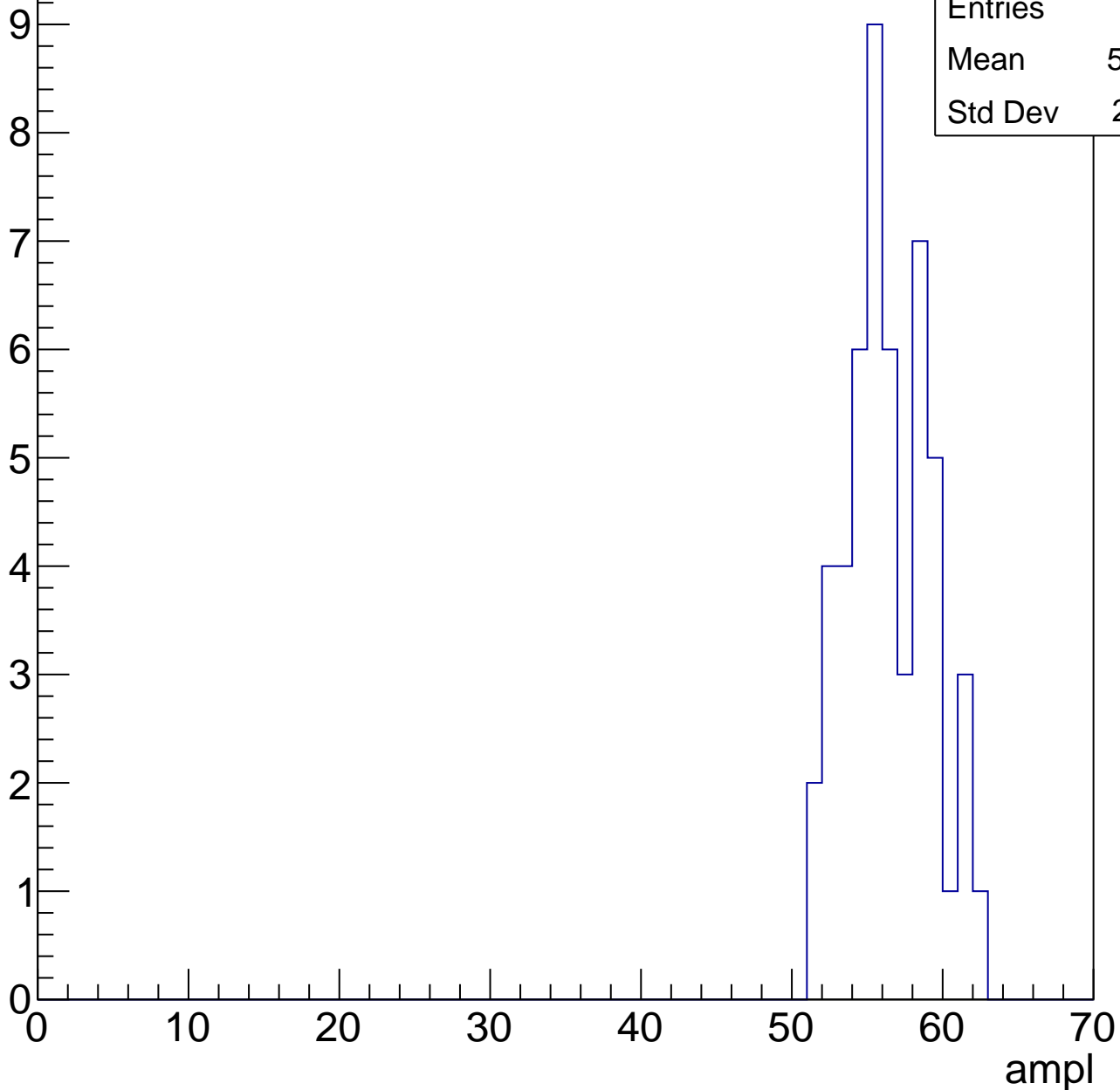


# B1L102S, U8-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	55.96
Std Dev	2.751

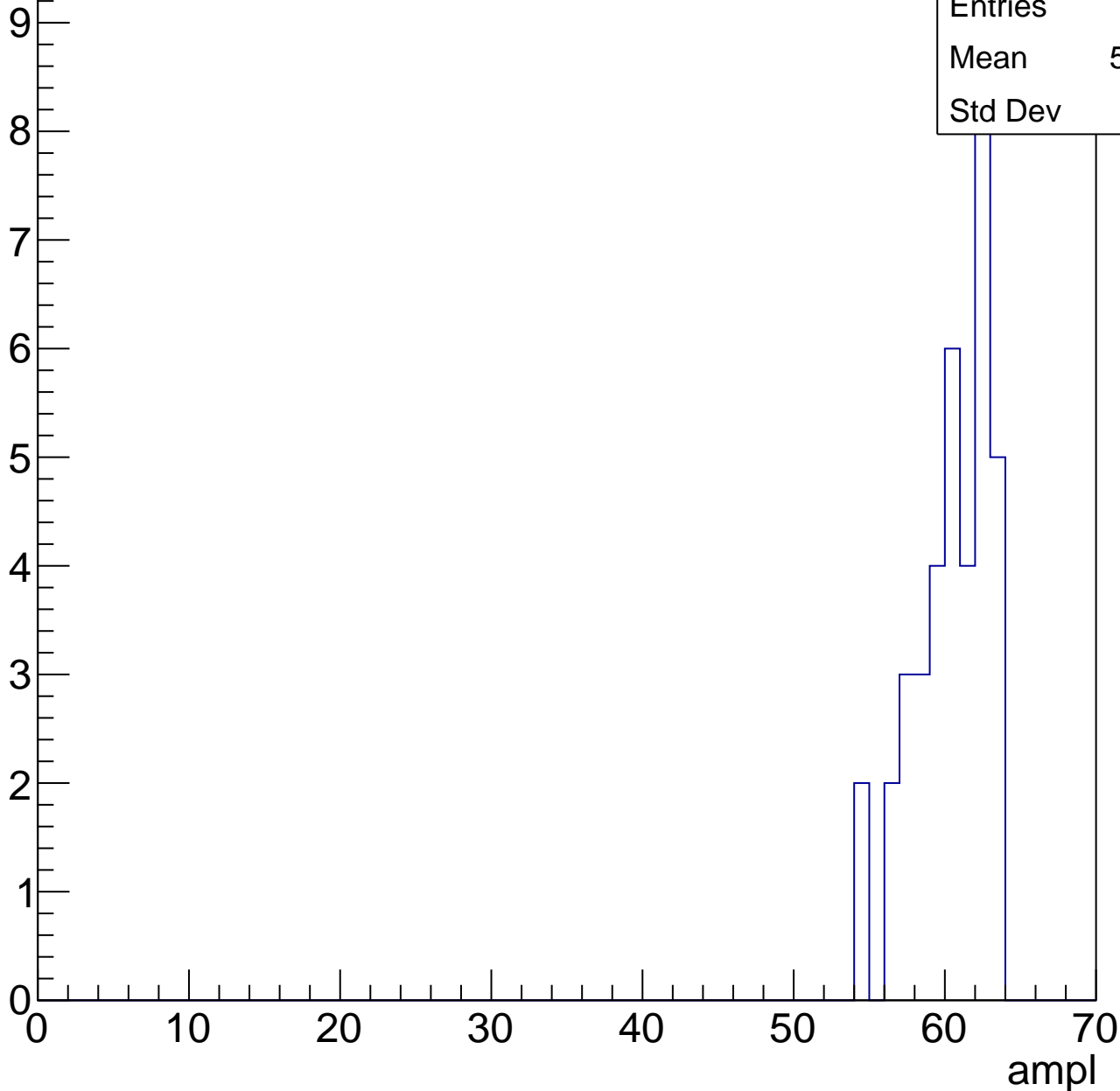


# B1L102S, U8-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	38
Mean	59.95
Std Dev	2.47

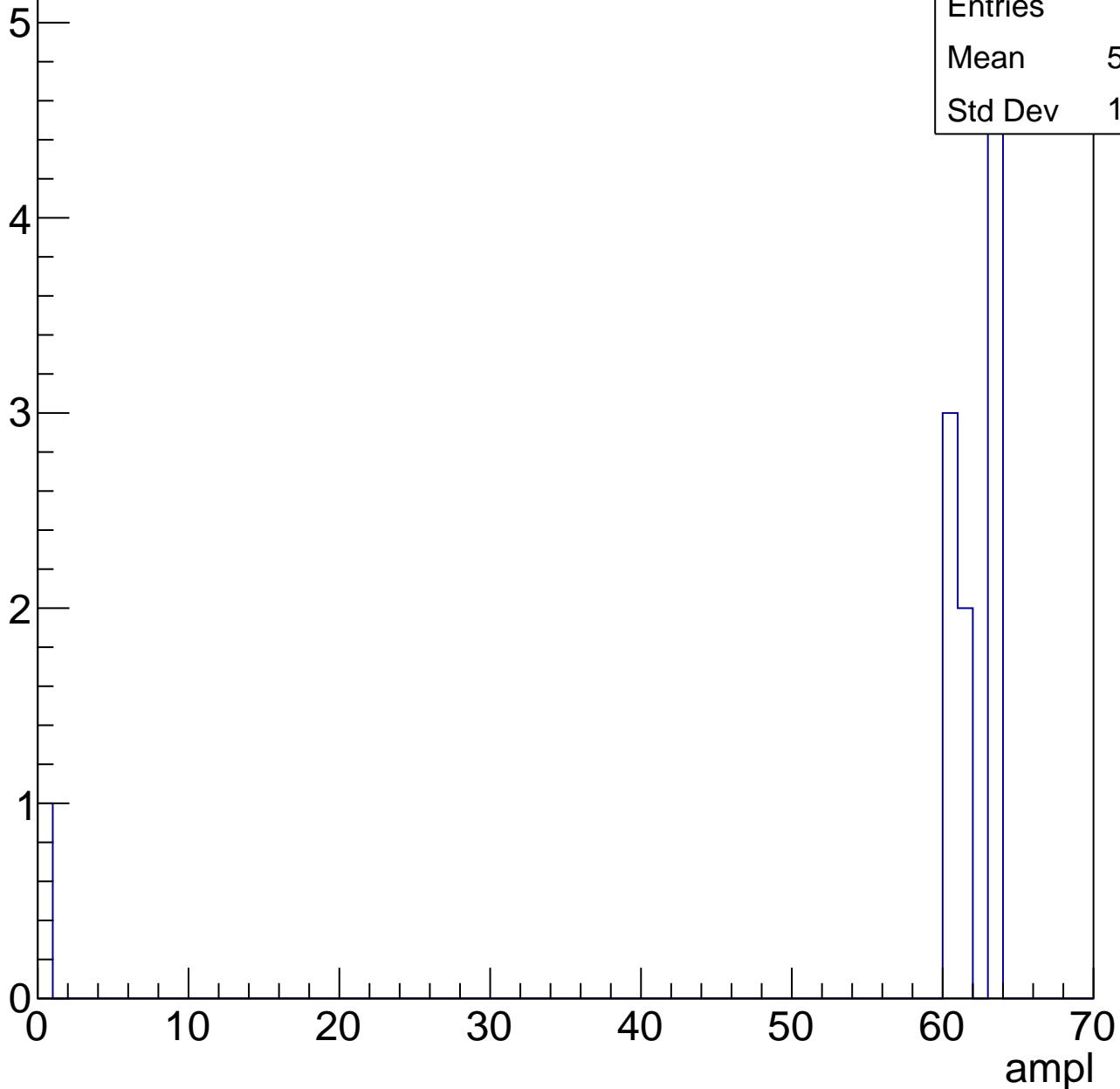


# B1L102S, U8-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	11
Mean	56.09
Std Dev	17.78





# B1L102S, U8-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch49, adc0

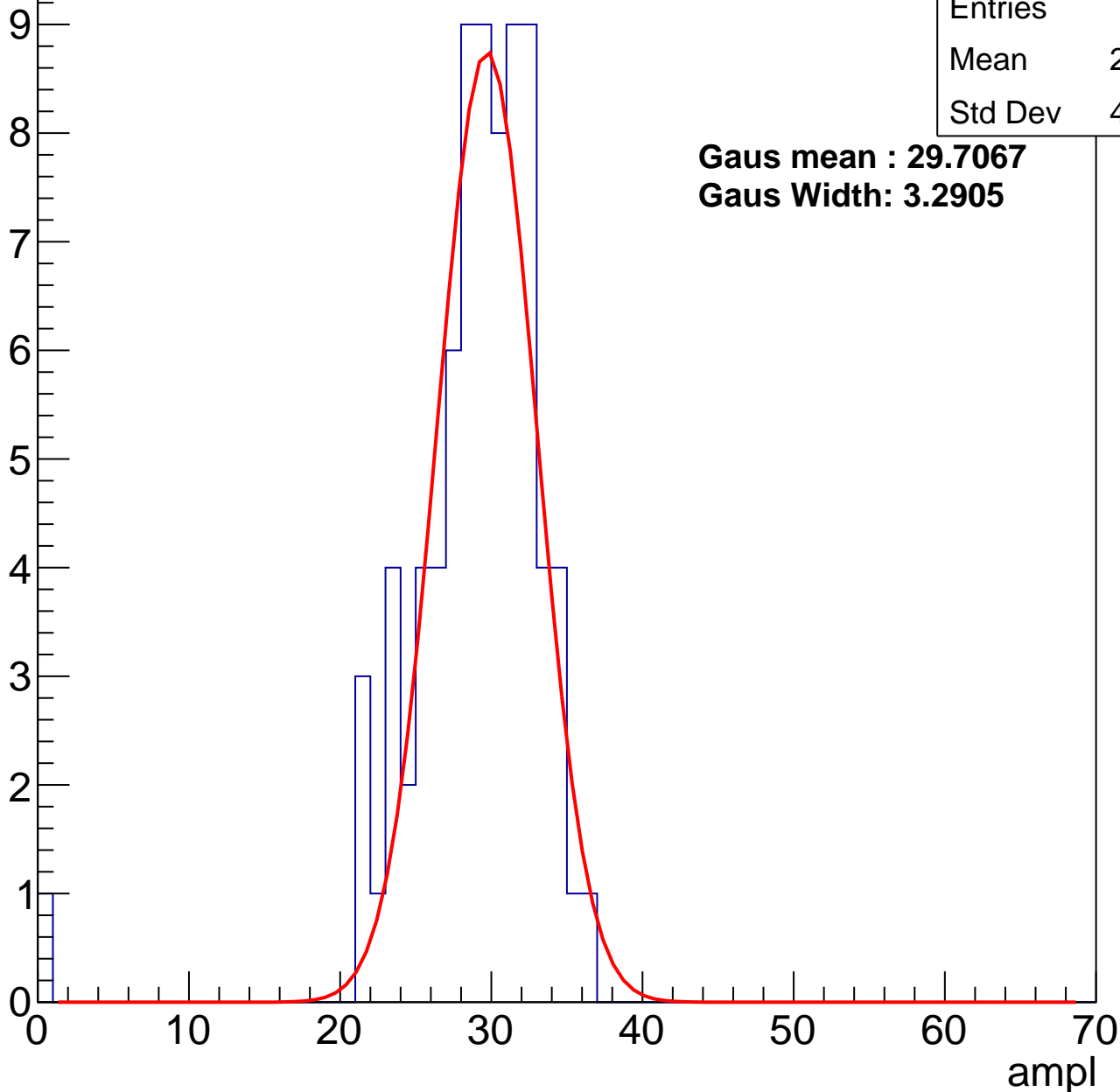
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	28.48
Std Dev	4.722

**Gaus mean : 29.7067**

**Gaus Width: 3.2905**



# B1L102S, U8-ch49, adc1

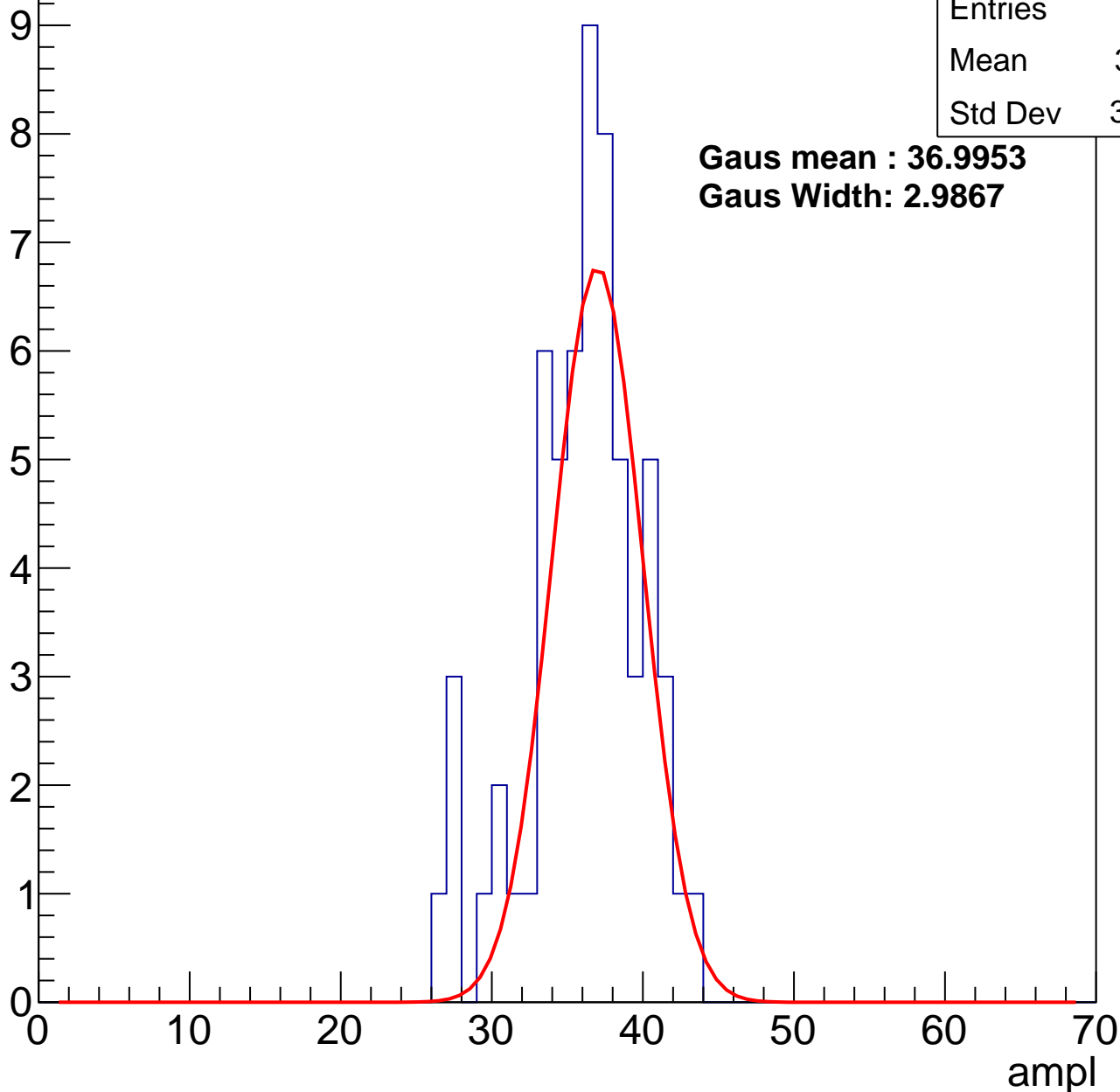
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	35.61
Std Dev	3.778

**Gaus mean : 36.9953**

**Gaus Width: 2.9867**



# B1L102S, U8-ch49, adc2

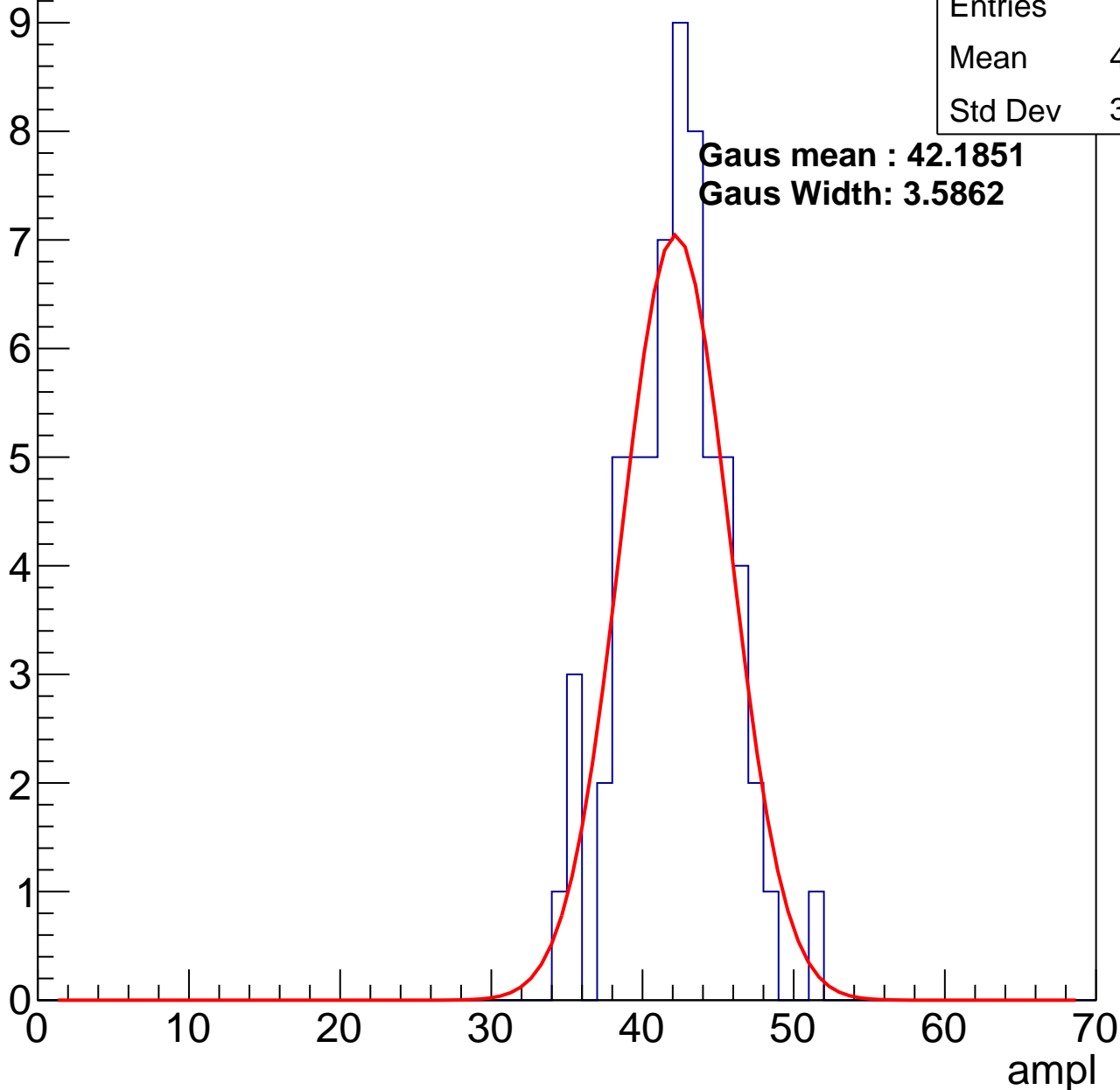
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	41.73
Std Dev	3.363

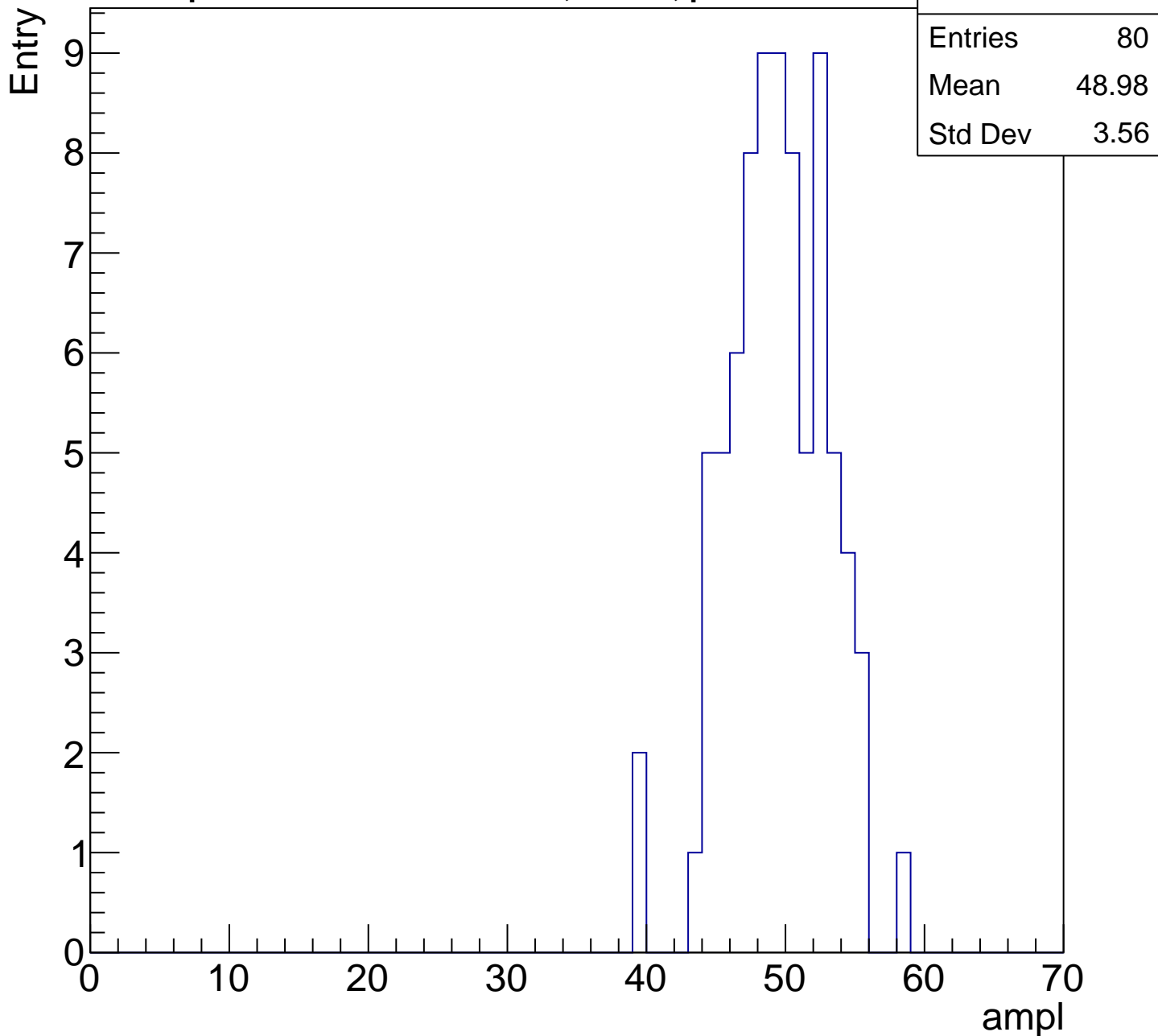
**Gaus mean : 42.1851**

**Gaus Width: 3.5862**



# B1L102S, U8-ch49, adc3

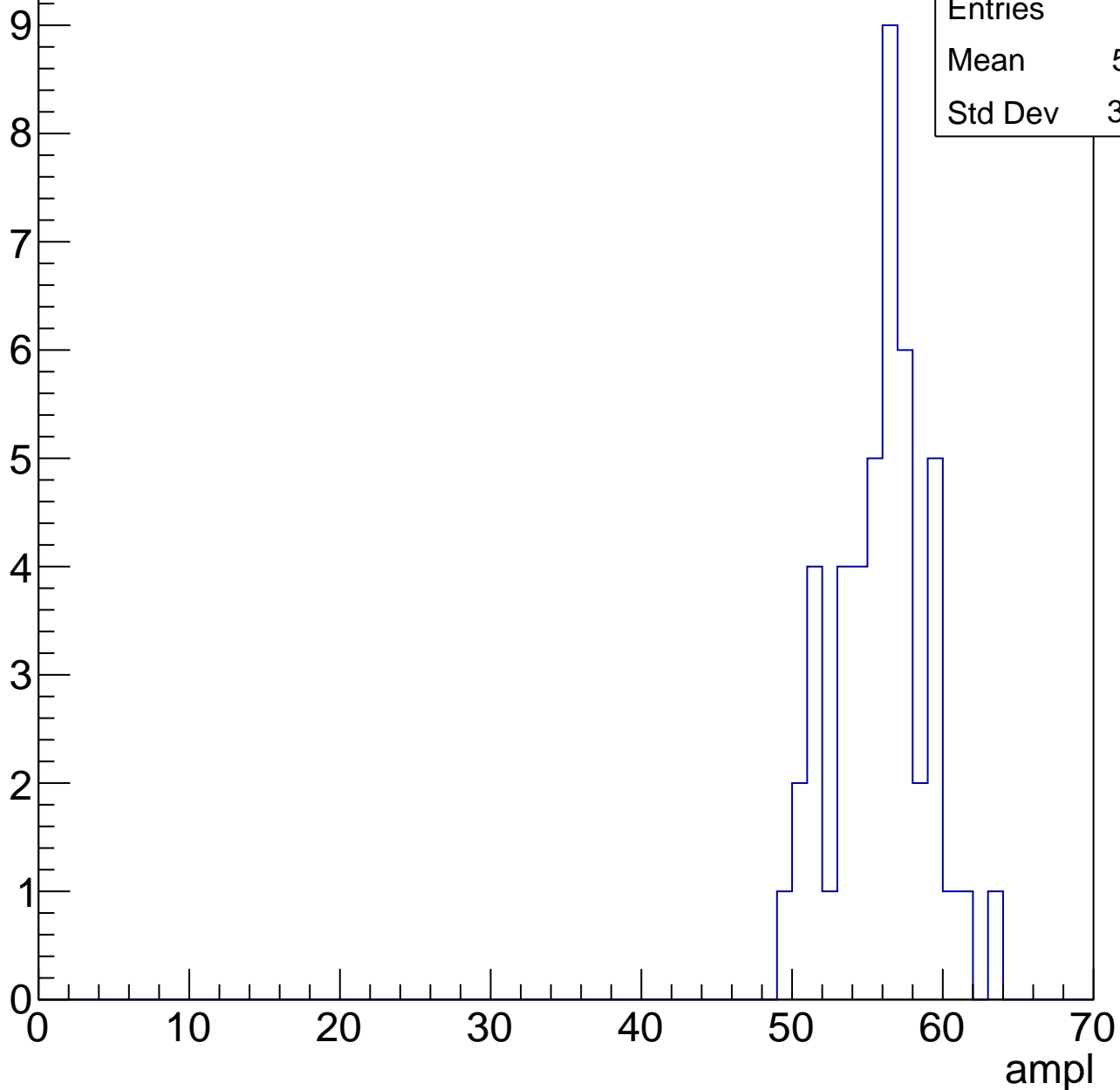
calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U8-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

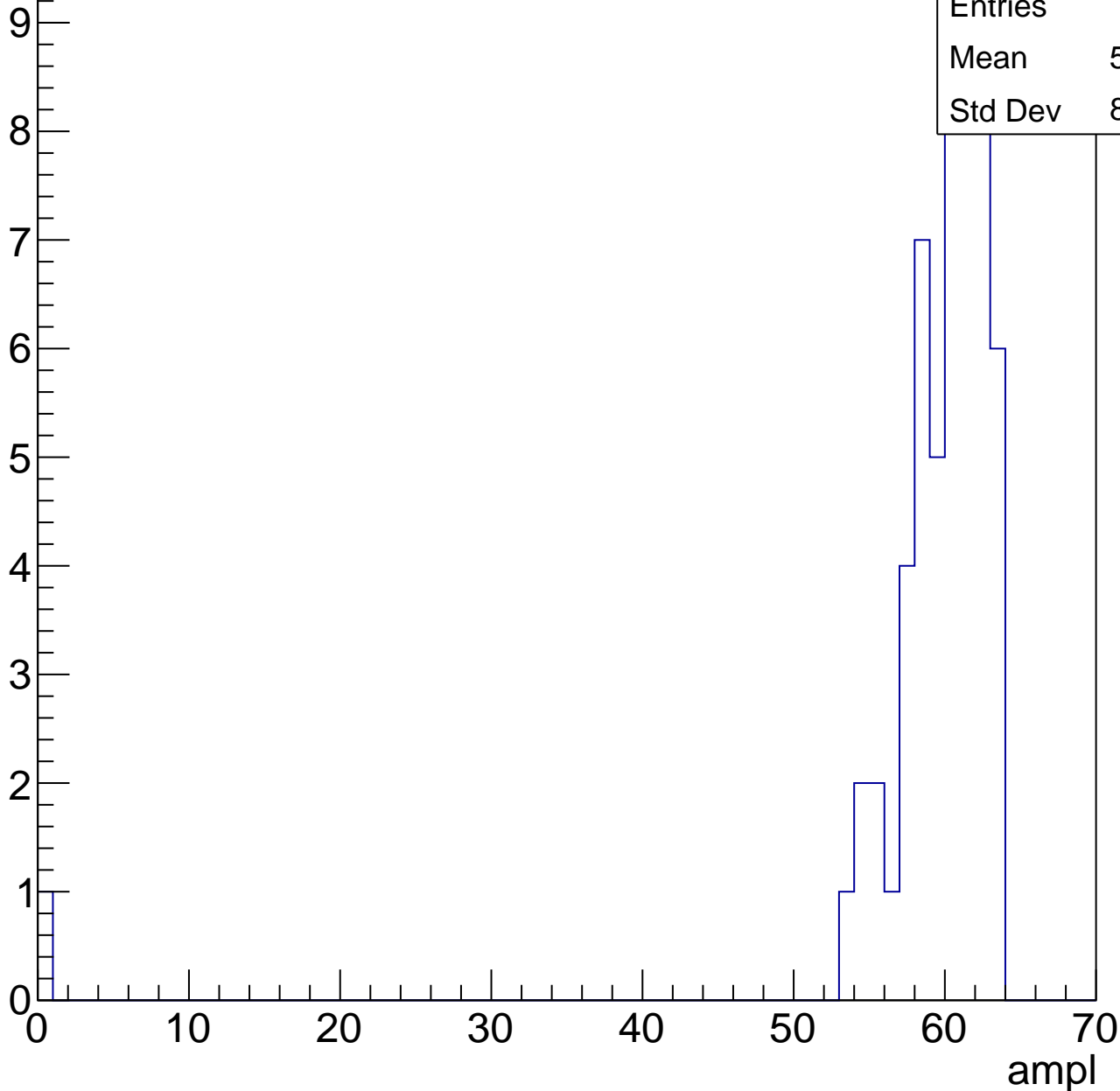


# B1L102S, U8-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	58.52
Std Dev	8.428



# B1L102S, U8-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch50, adc0

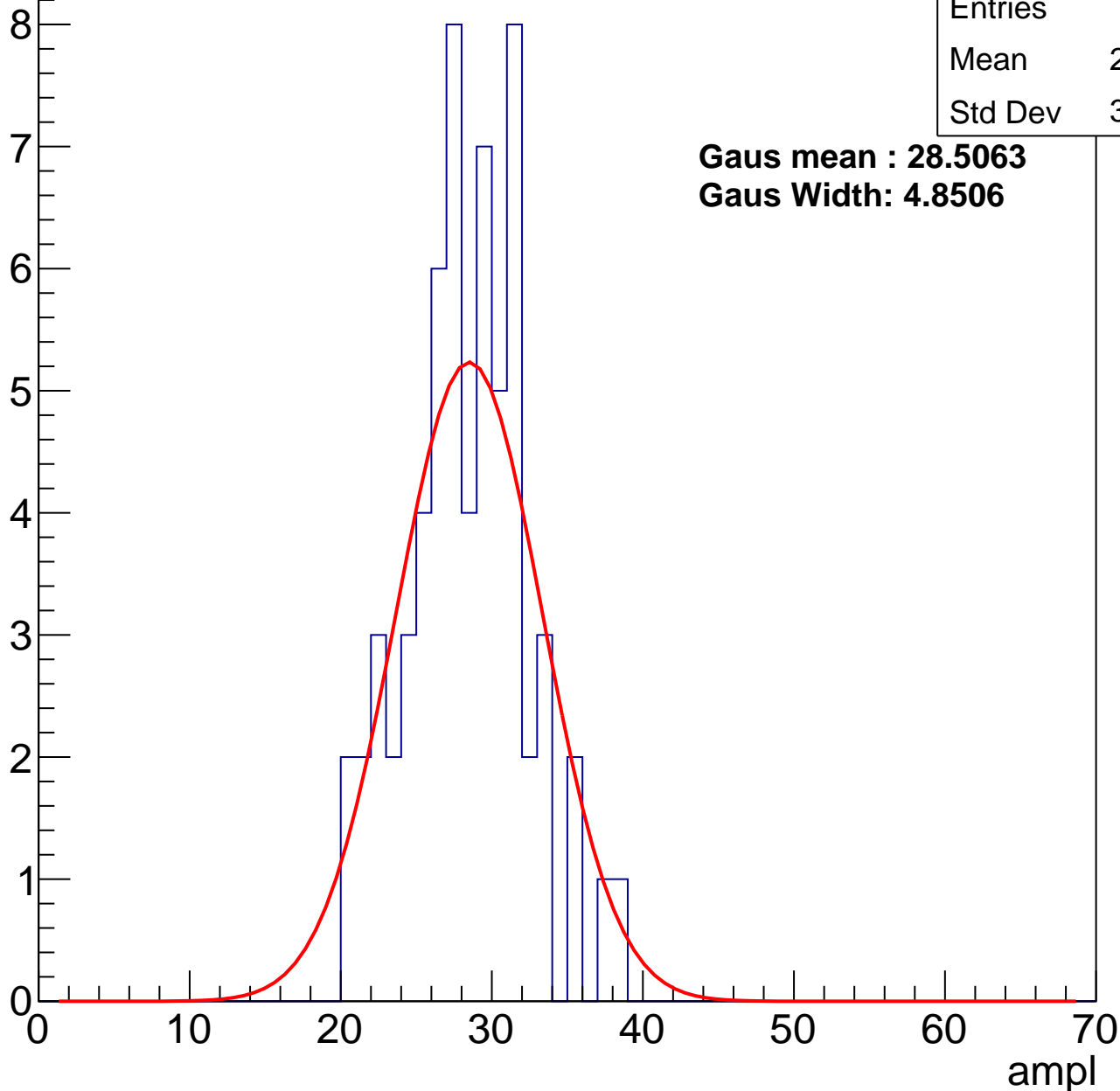
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	27.92
Std Dev	3.953

**Gaus mean : 28.5063**

**Gaus Width: 4.8506**



# B1L102S, U8-ch50, adc1

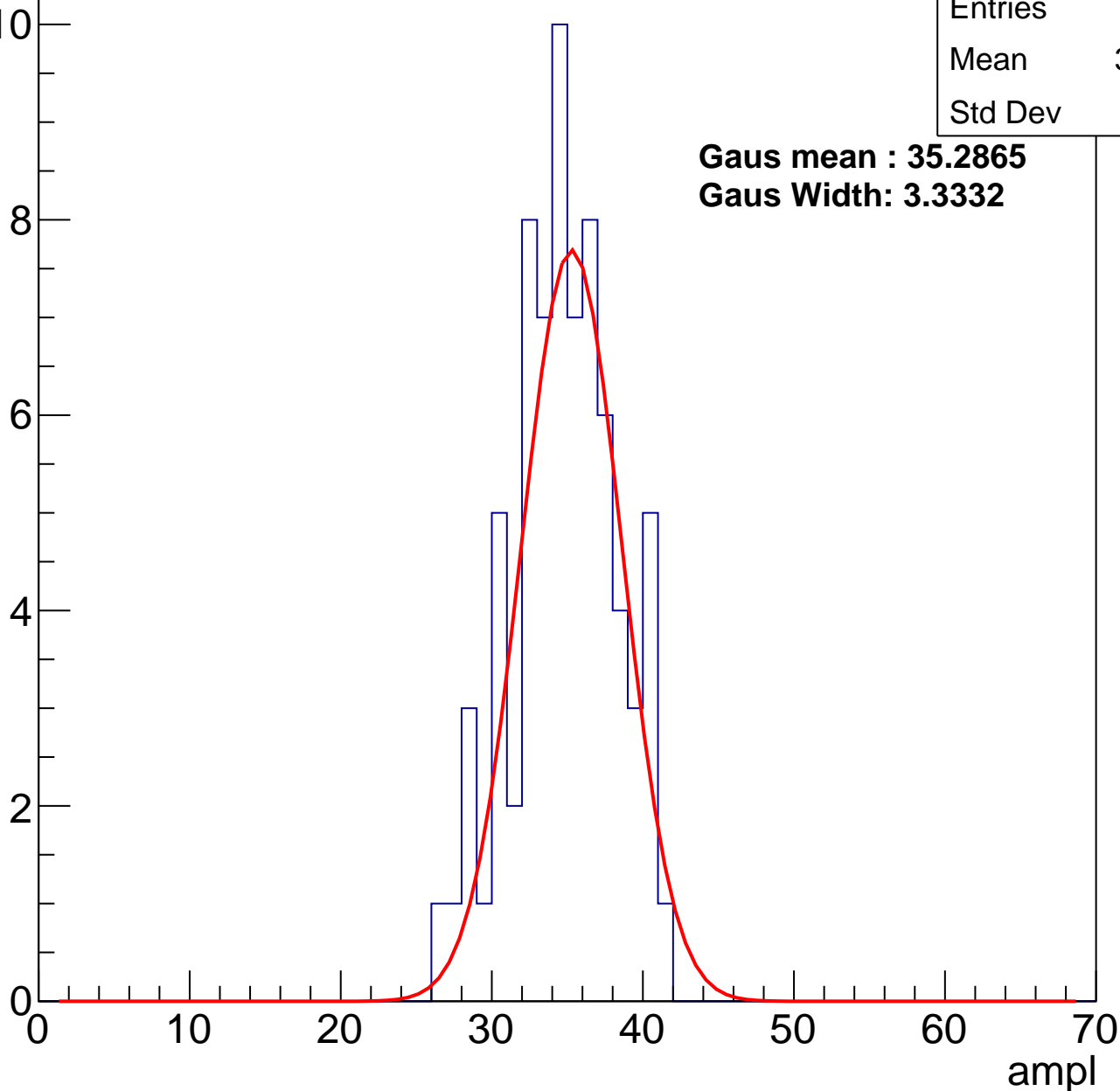
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	34.31
Std Dev	3.41

**Gaus mean : 35.2865**

**Gaus Width: 3.3332**



# B1L102S, U8-ch50, adc2

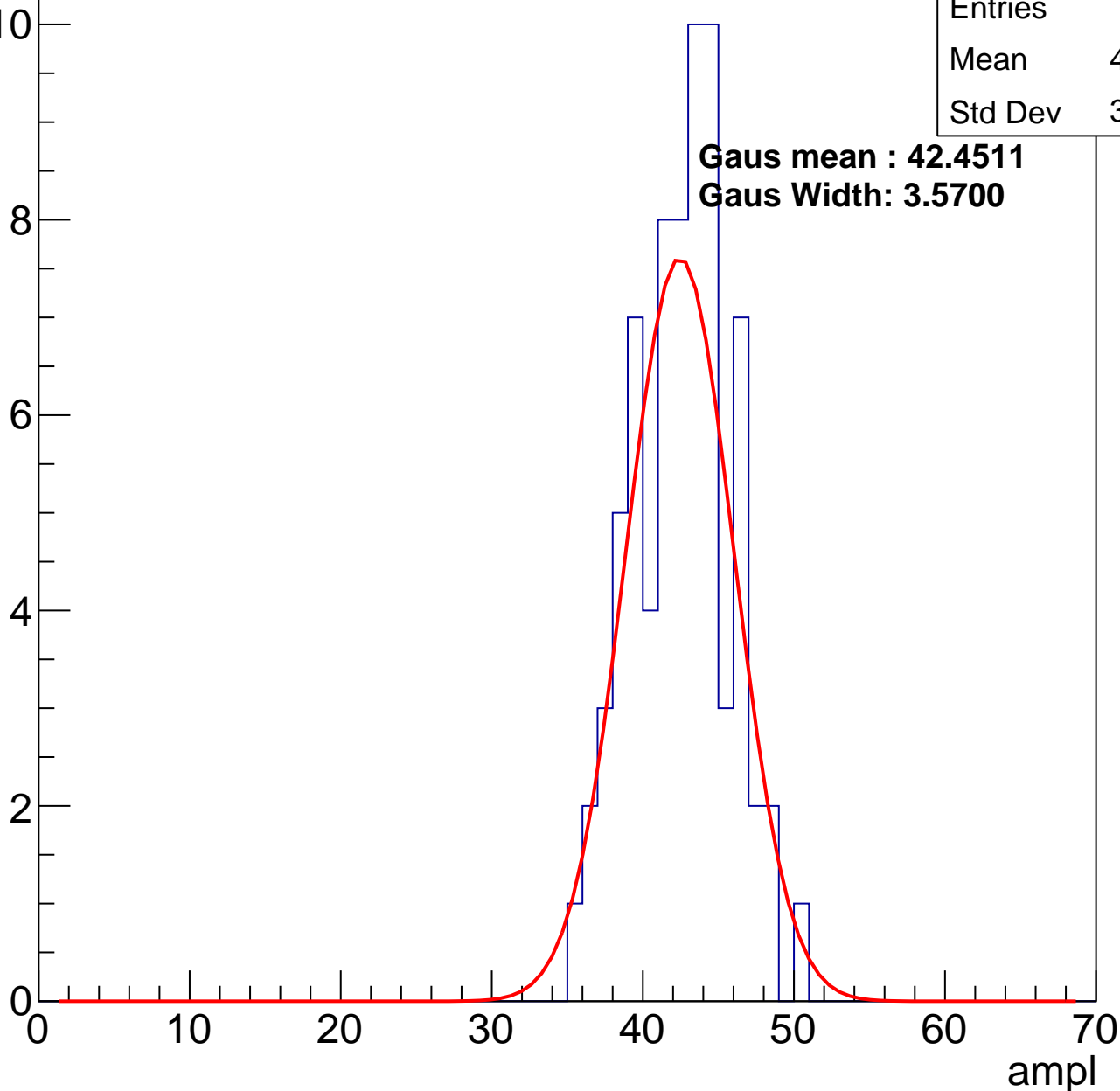
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	42.08
Std Dev	3.178

**Gaus mean : 42.4511**

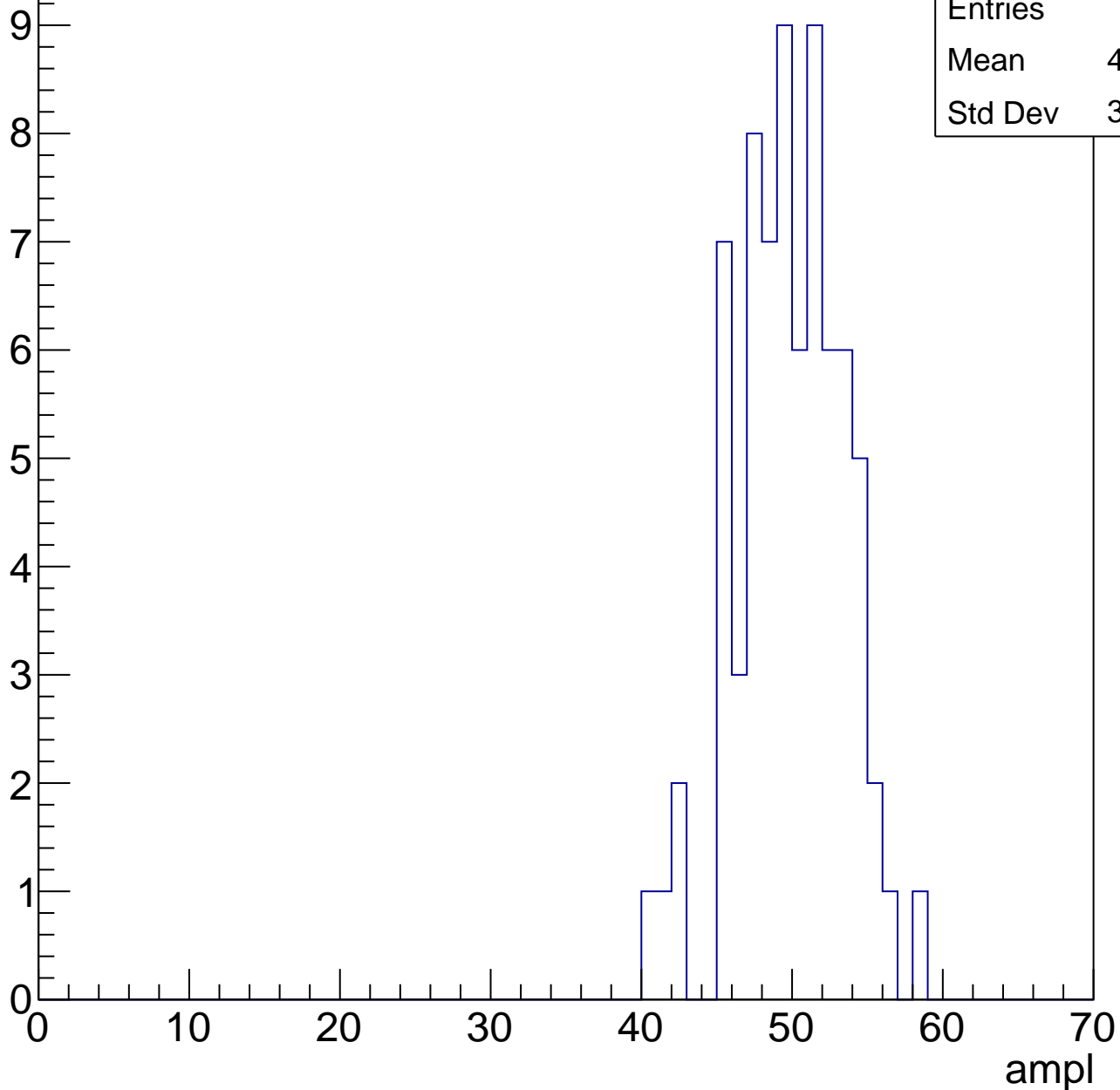
**Gaus Width: 3.5700**



# B1L102S, U8-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

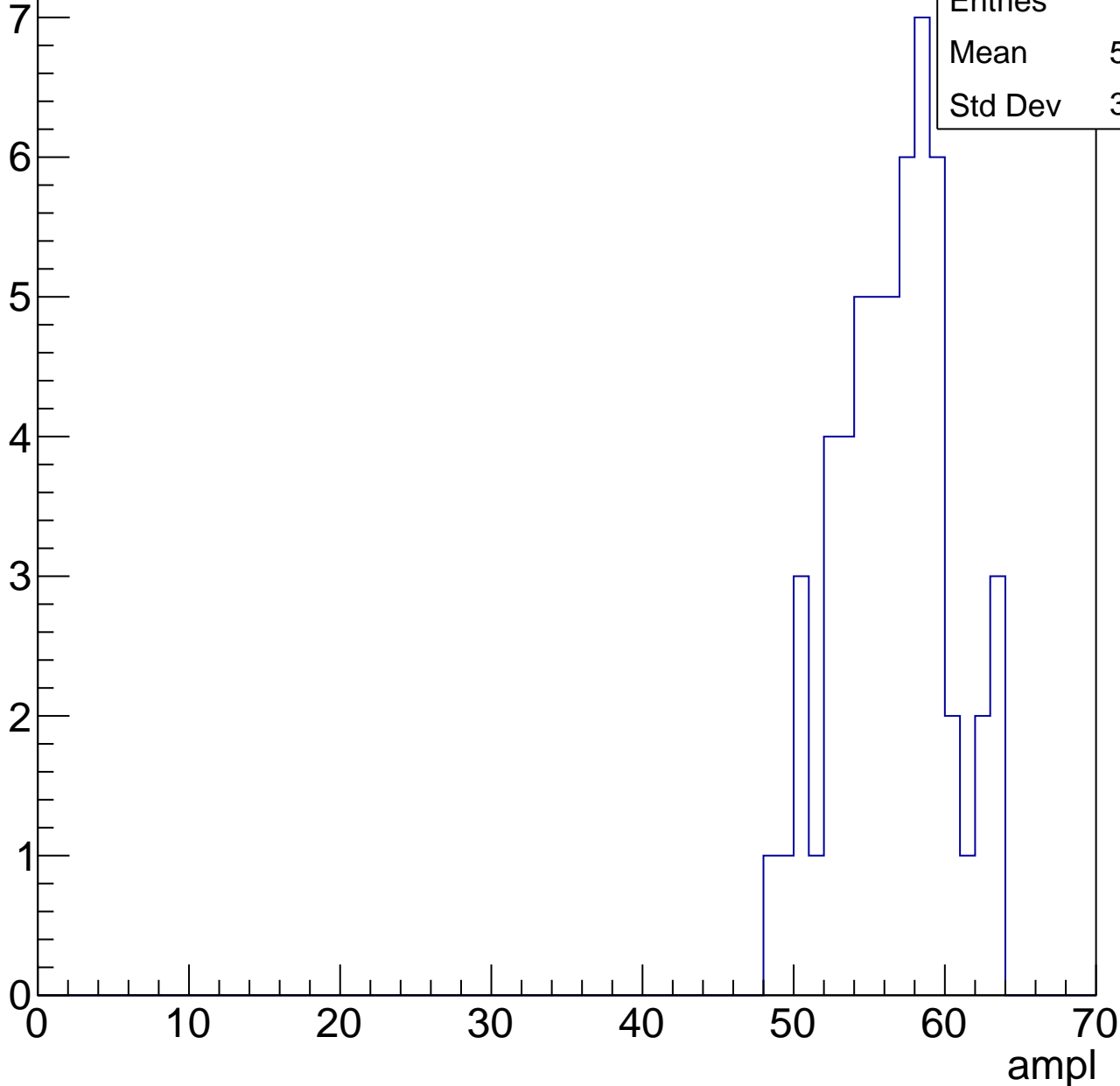


# B1L102S, U8-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

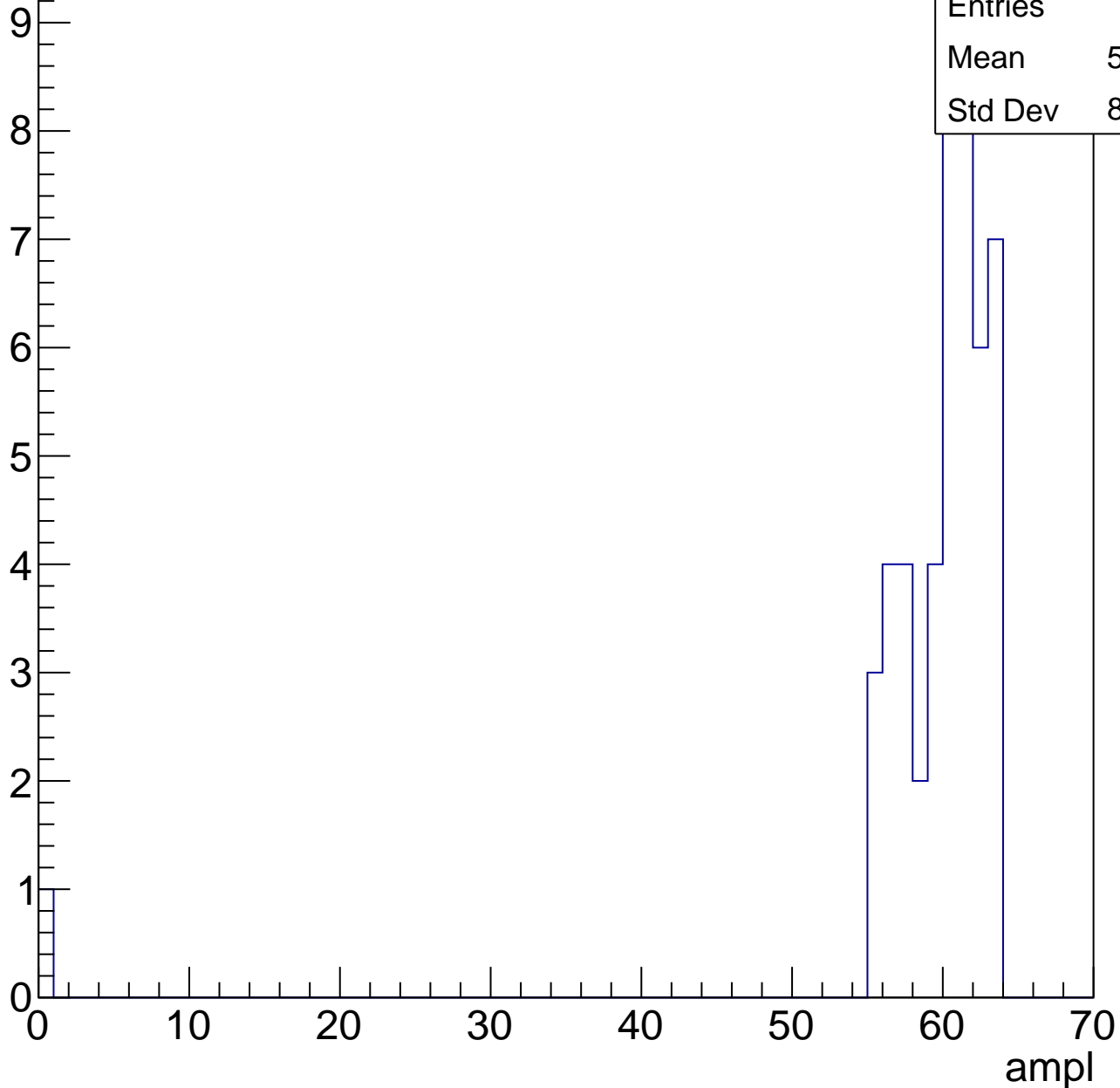
Entries	56
Mean	56.05
Std Dev	3.622



# B1L102S, U8-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch51, adc0

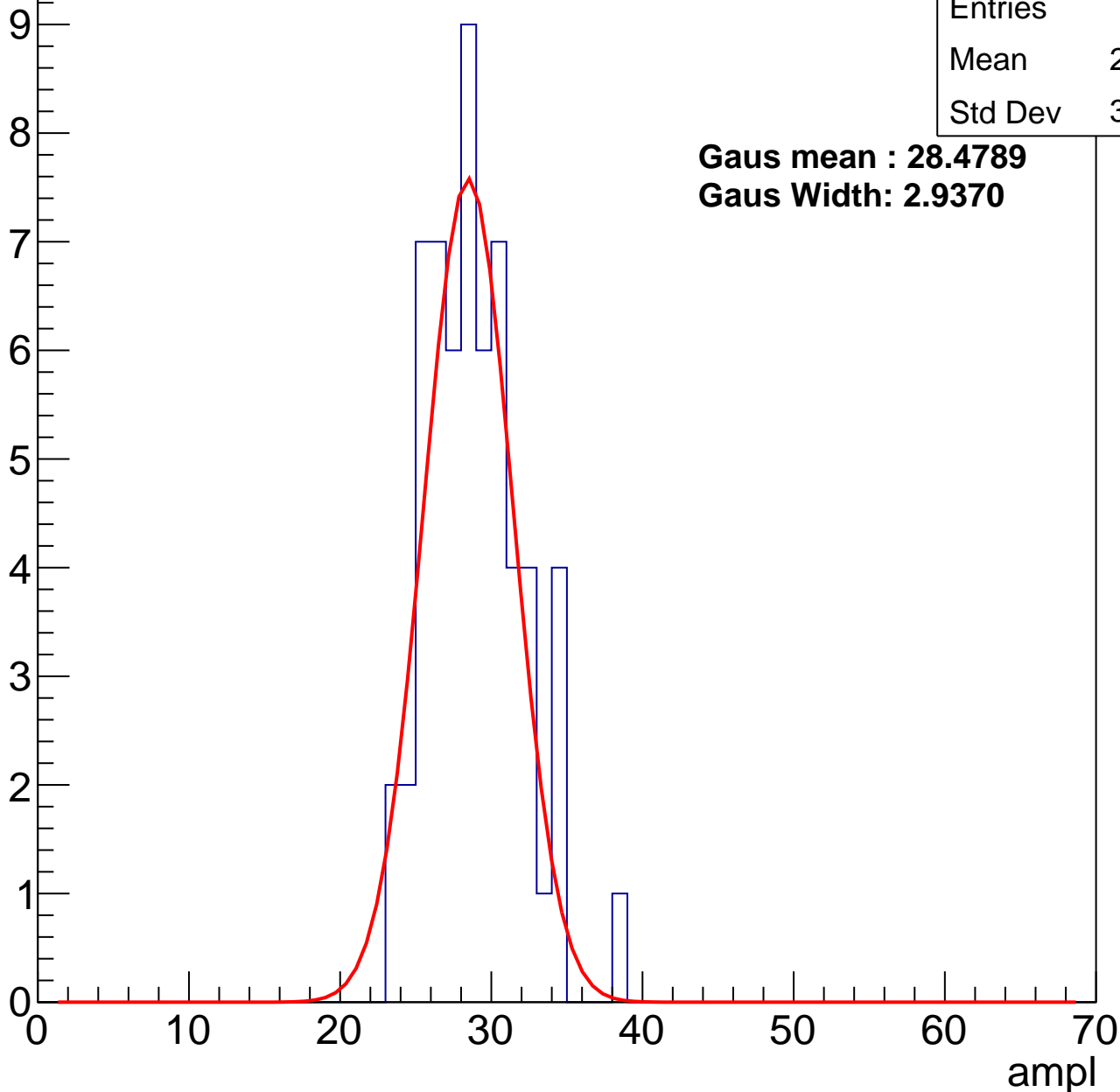
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	28.47
Std Dev	3.079

**Gaus mean : 28.4789**

**Gaus Width: 2.9370**



# B1L102S, U8-ch51, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	80
Mean	35.51
Std Dev	3.421

**Gaus mean : 36.3953**

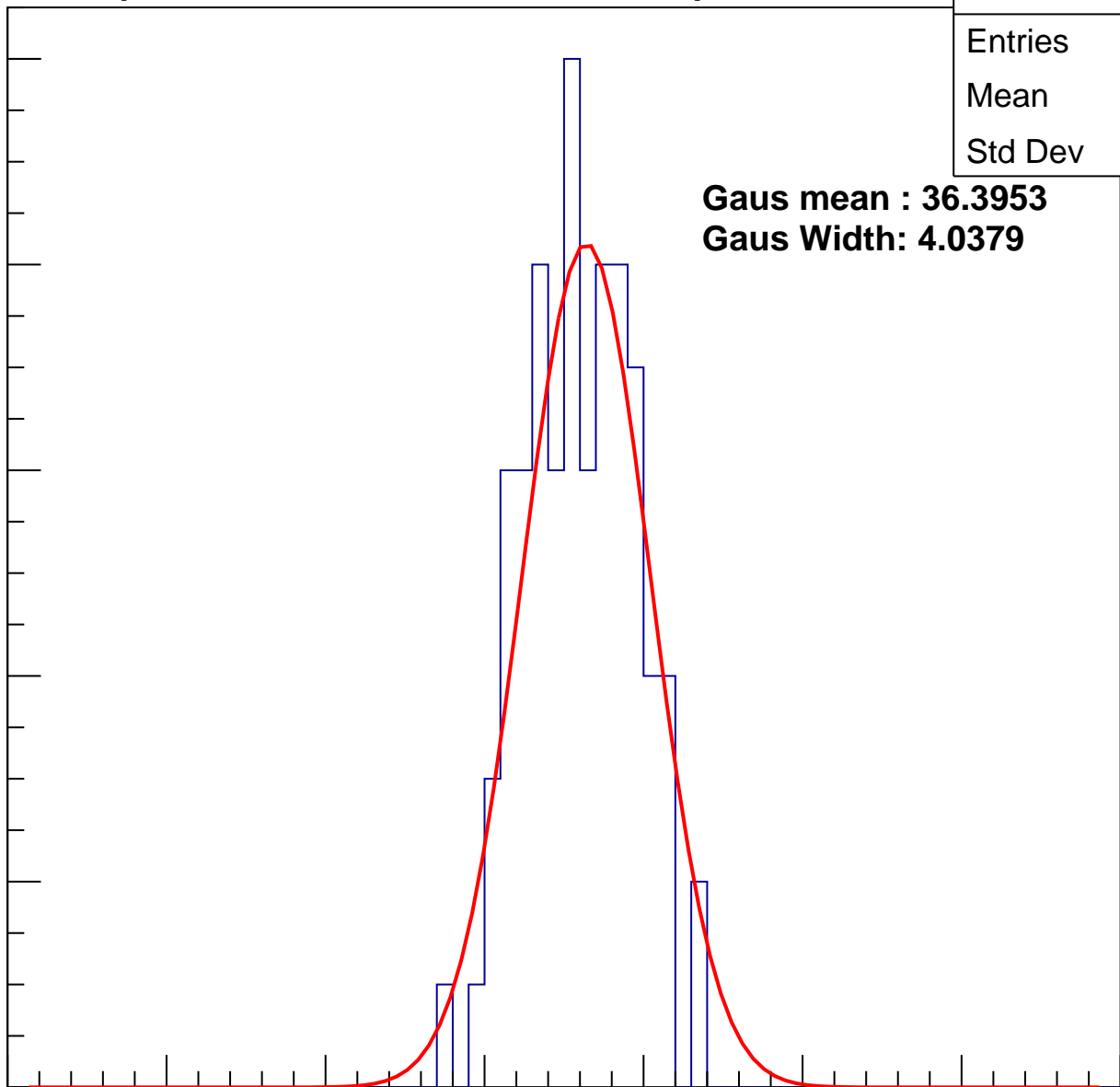
**Gaus Width: 4.0379**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L102S, U8-ch51, adc2

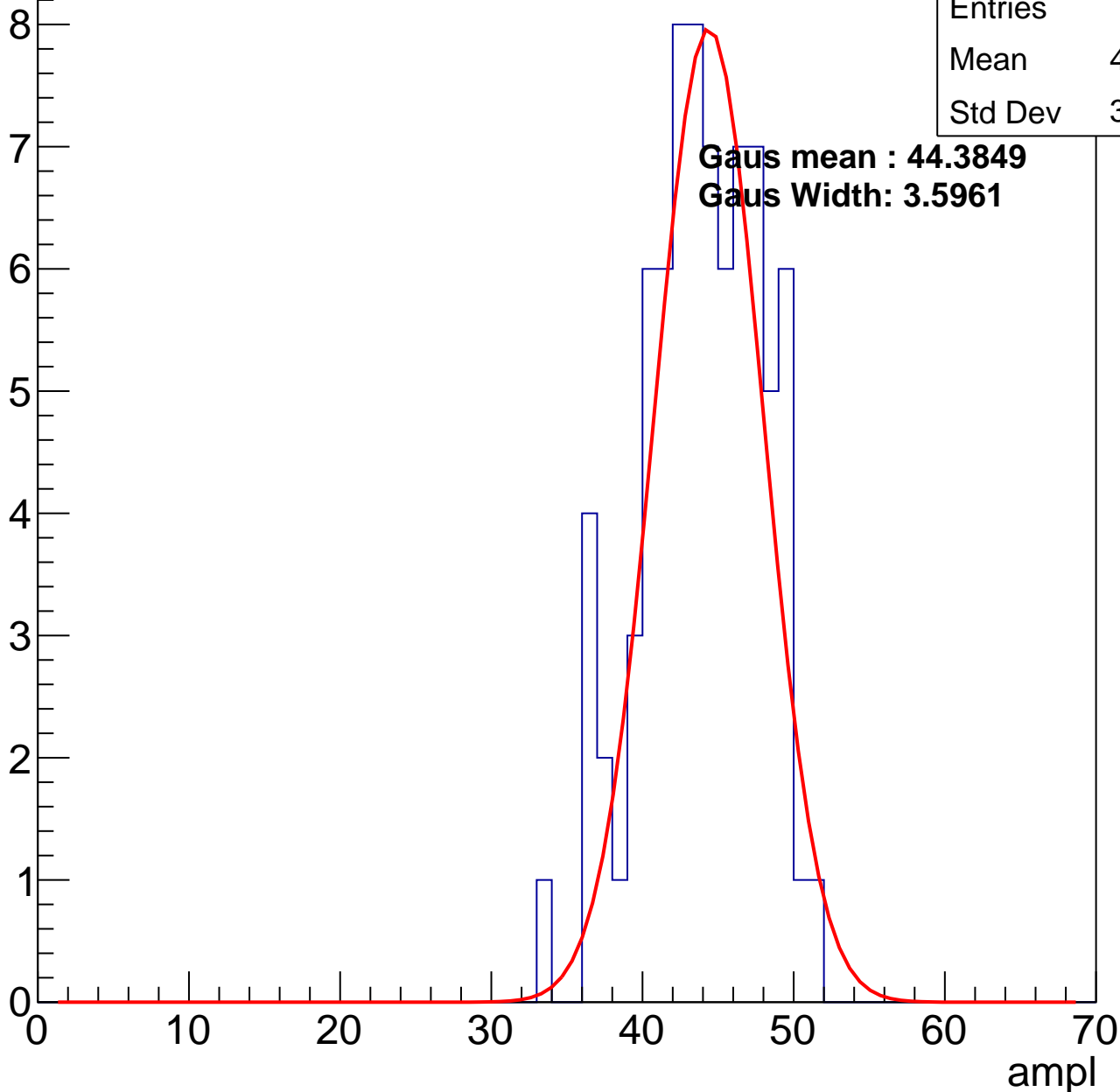
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	43.49
Std Dev	3.845

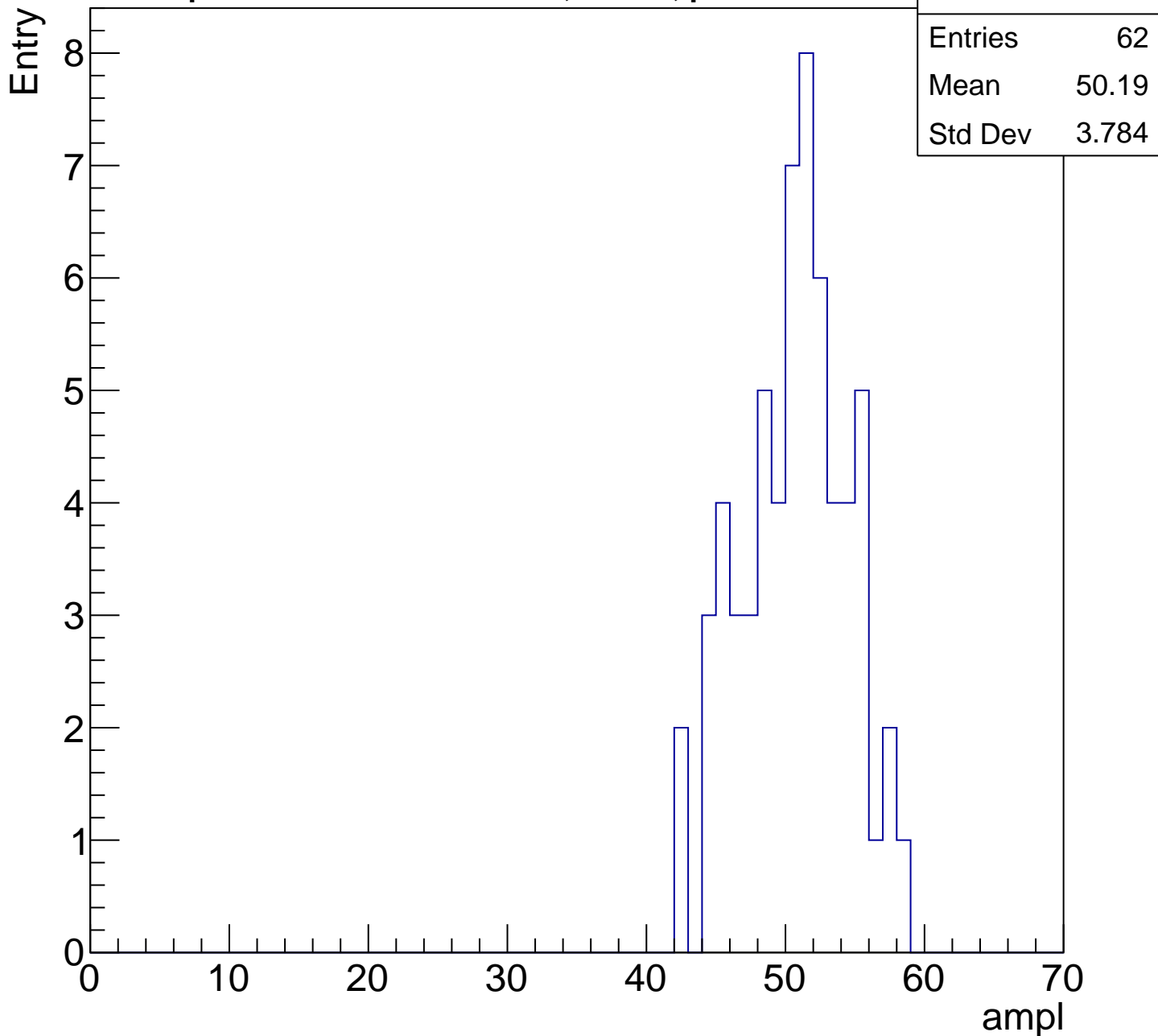
**Gaus mean : 44.3849**

**Gaus Width: 3.5961**



# B1L102S, U8-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

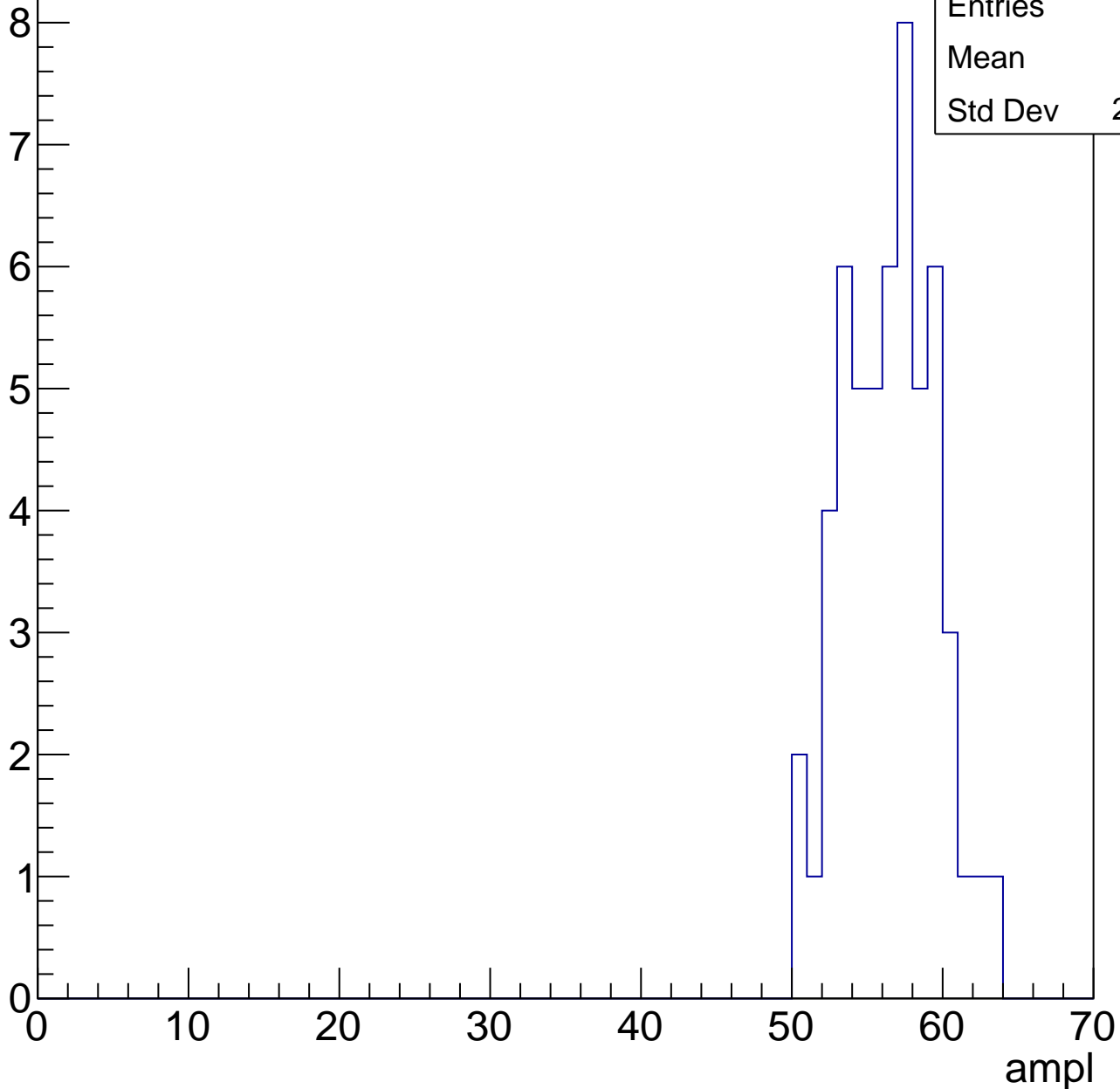


# B1L102S, U8-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	56
Std Dev	2.981

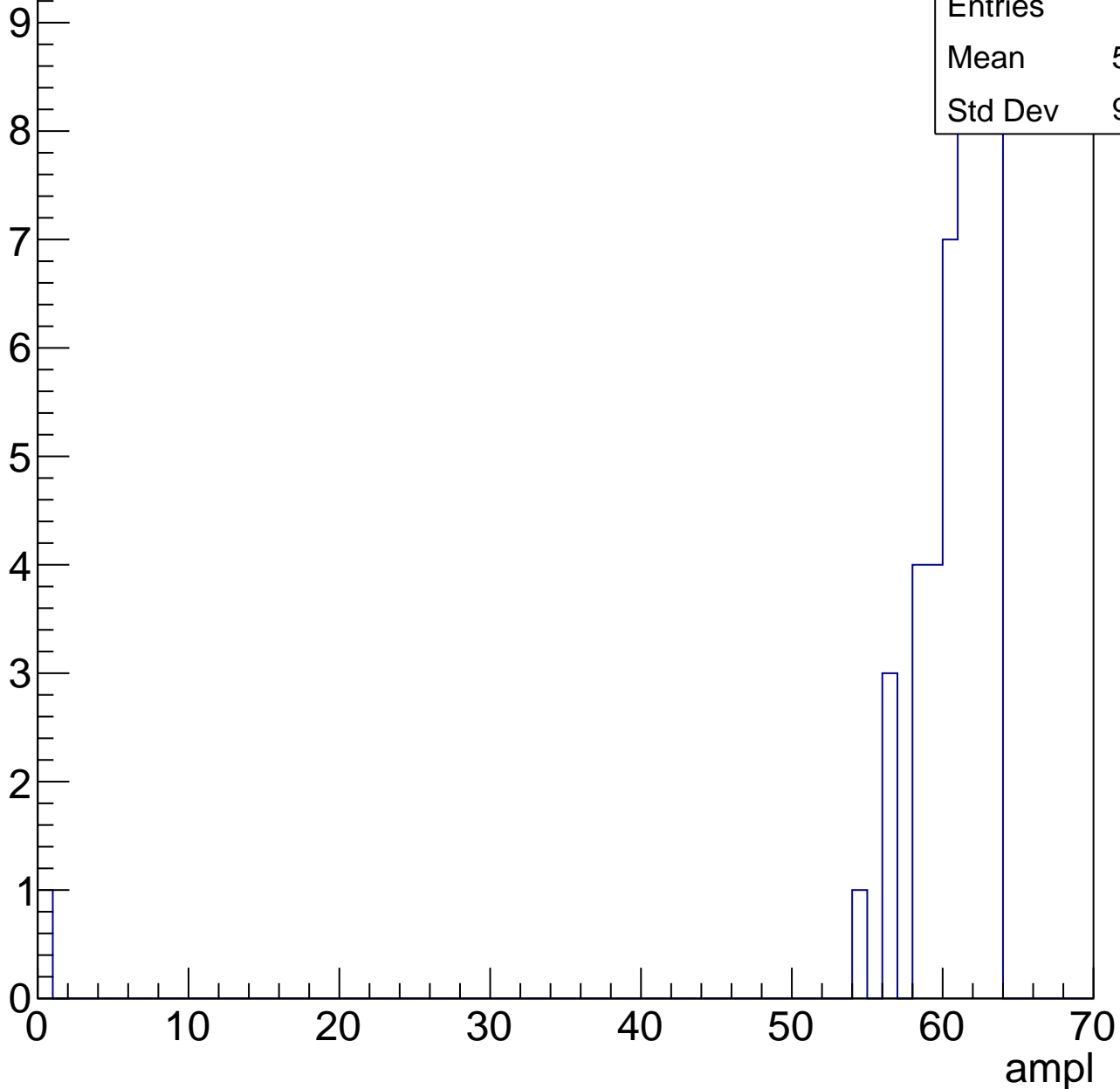


# B1L102S, U8-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

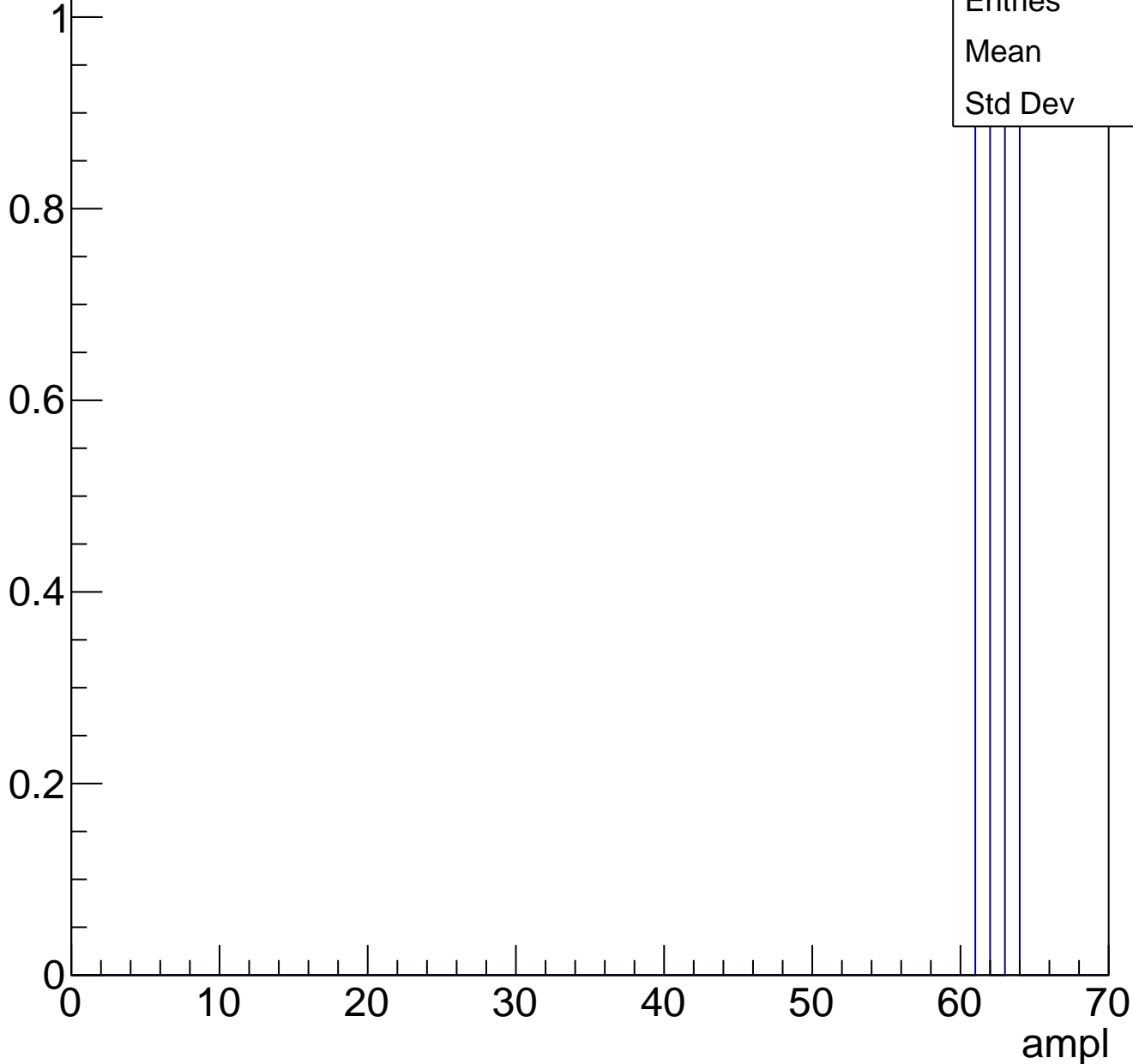
Entries	45
Mean	59.11
Std Dev	9.171



# B1L102S, U8-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch52, adc0

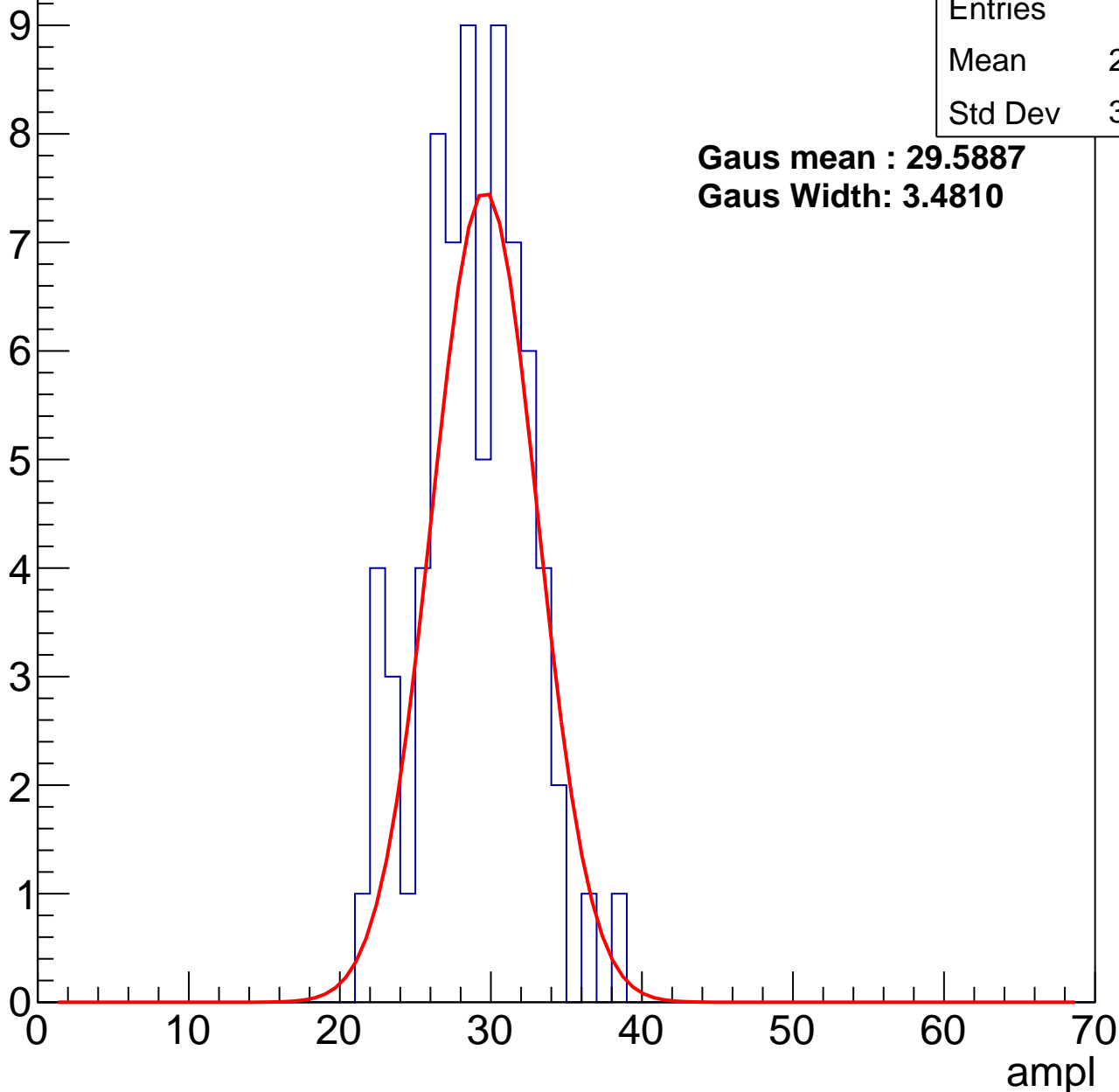
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	28.46
Std Dev	3.496

**Gaus mean : 29.5887**

**Gaus Width: 3.4810**



# B1L102S, U8-ch52, adc1

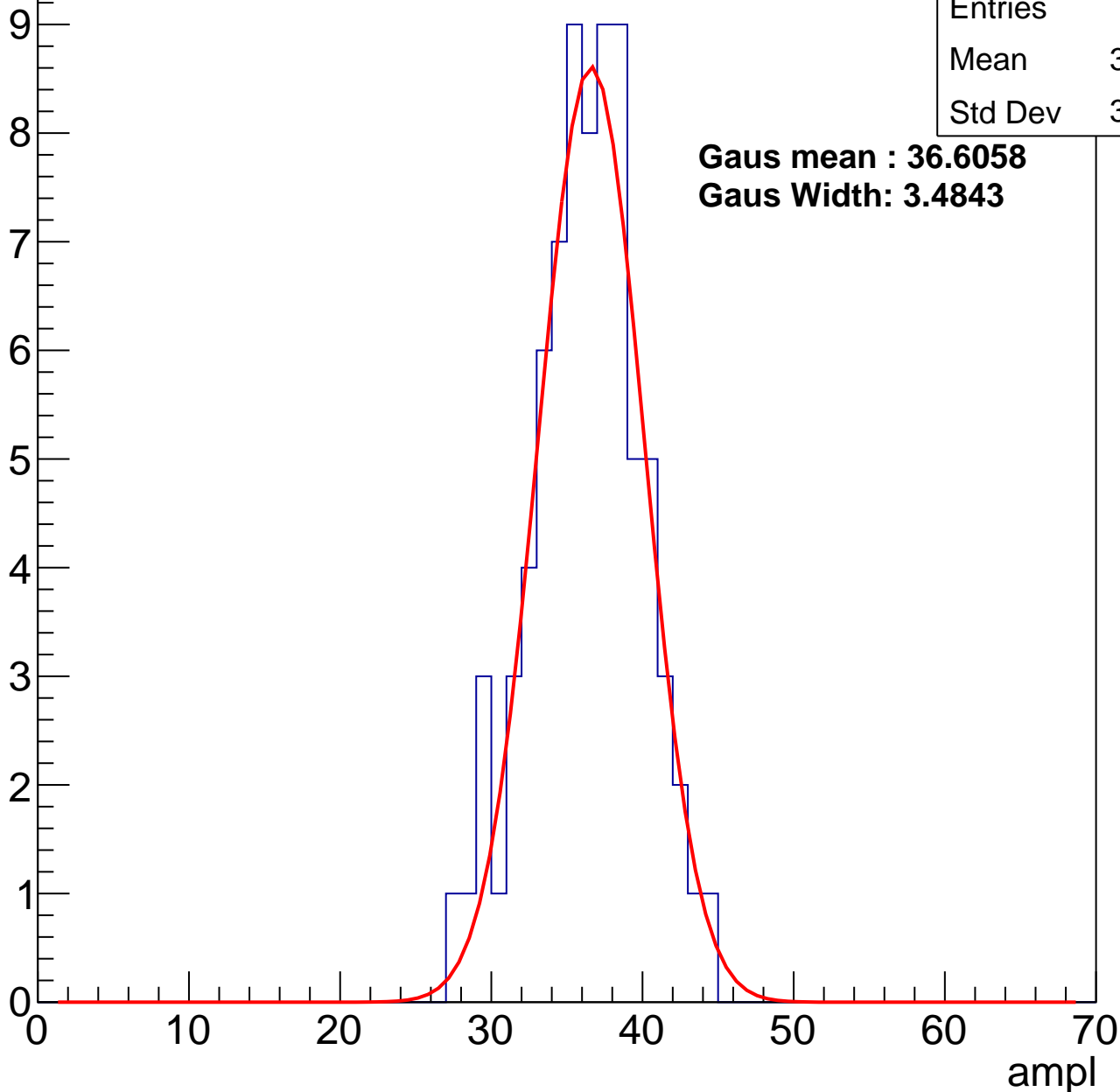
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	35.85
Std Dev	3.556

**Gaus mean : 36.6058**

**Gaus Width: 3.4843**



# B1L102S, U8-ch52, adc2

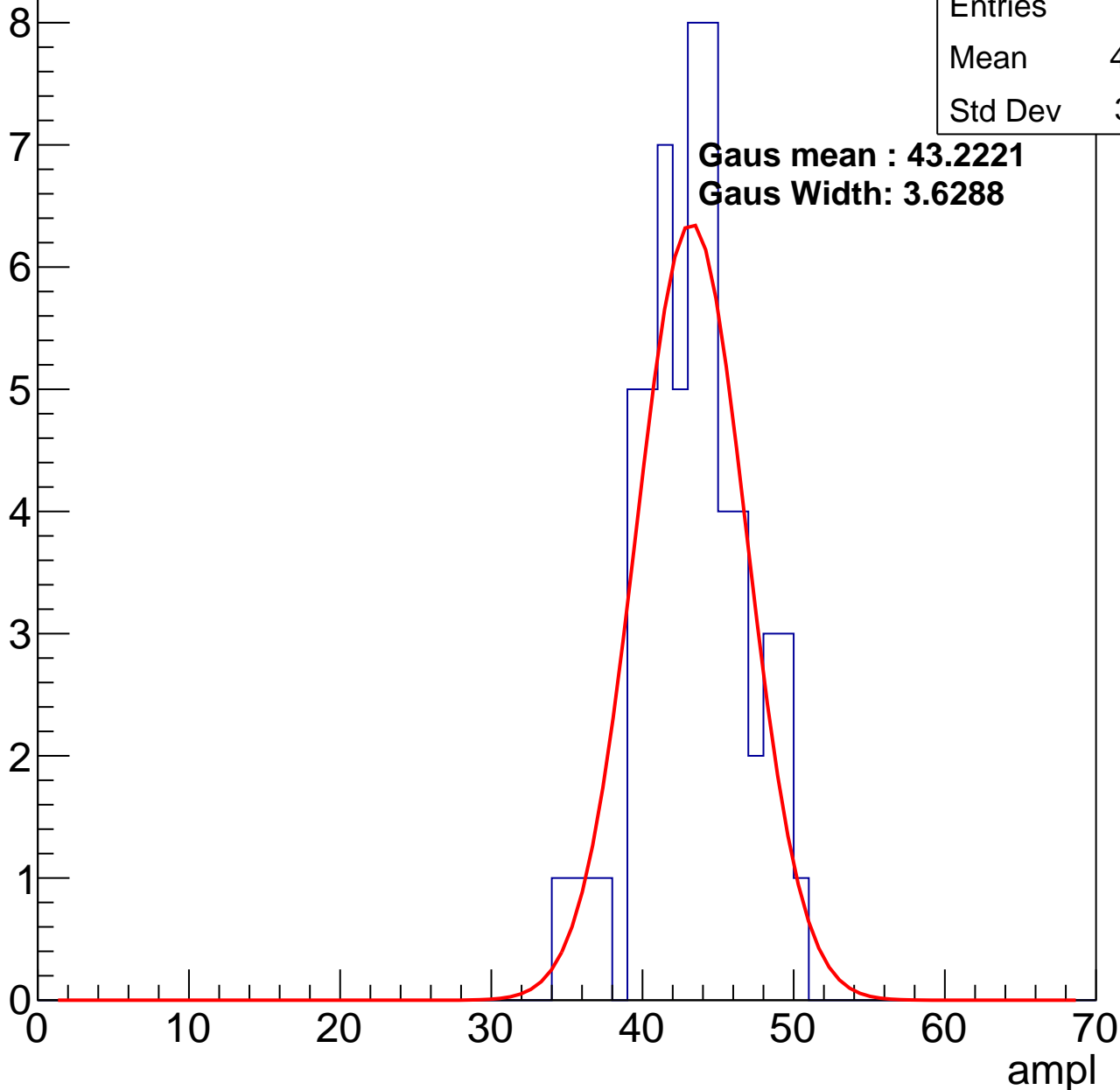
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	42.86
Std Dev	3.471

**Gaus mean : 43.2221**

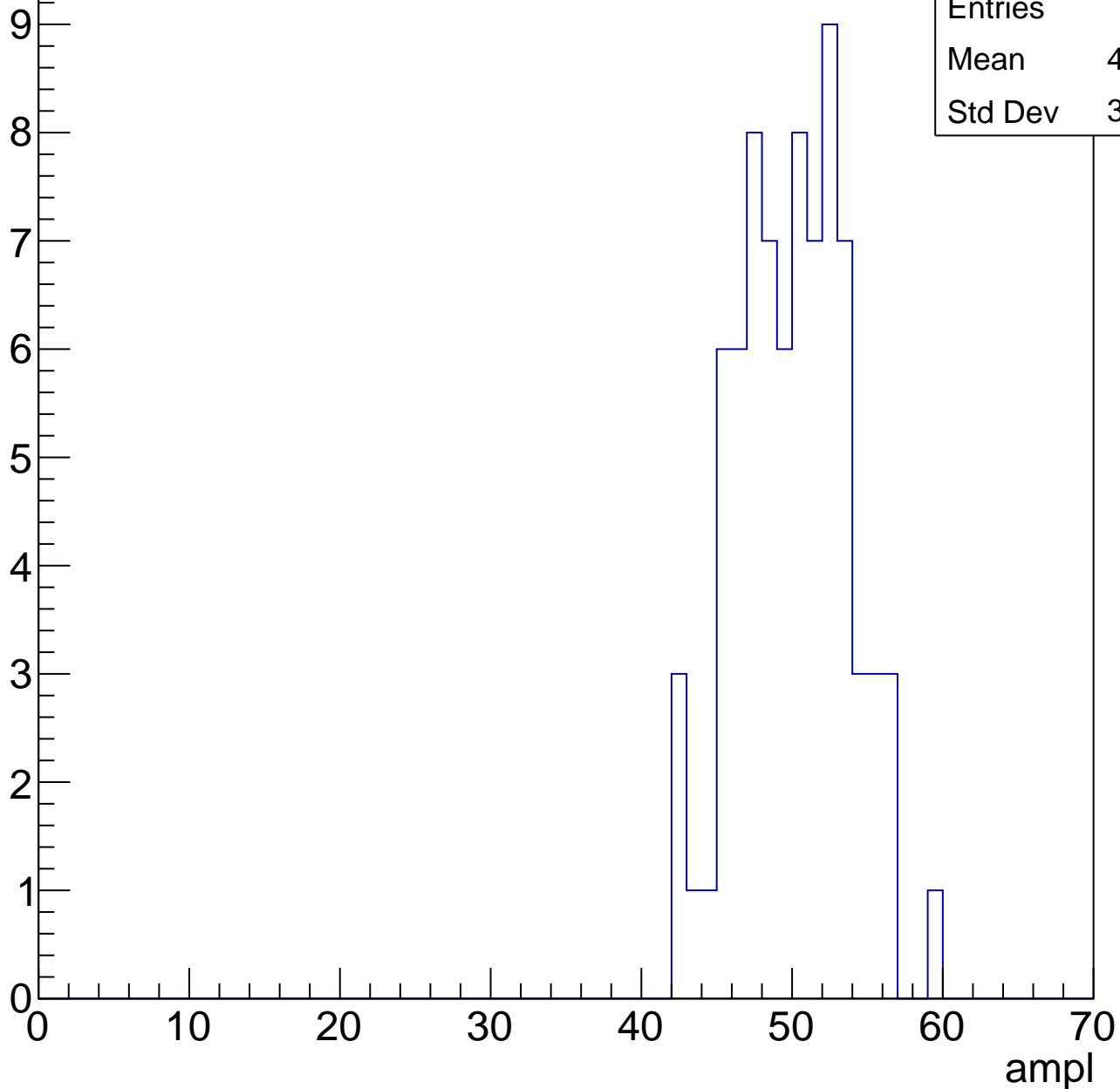
**Gaus Width: 3.6288**



# B1L102S, U8-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



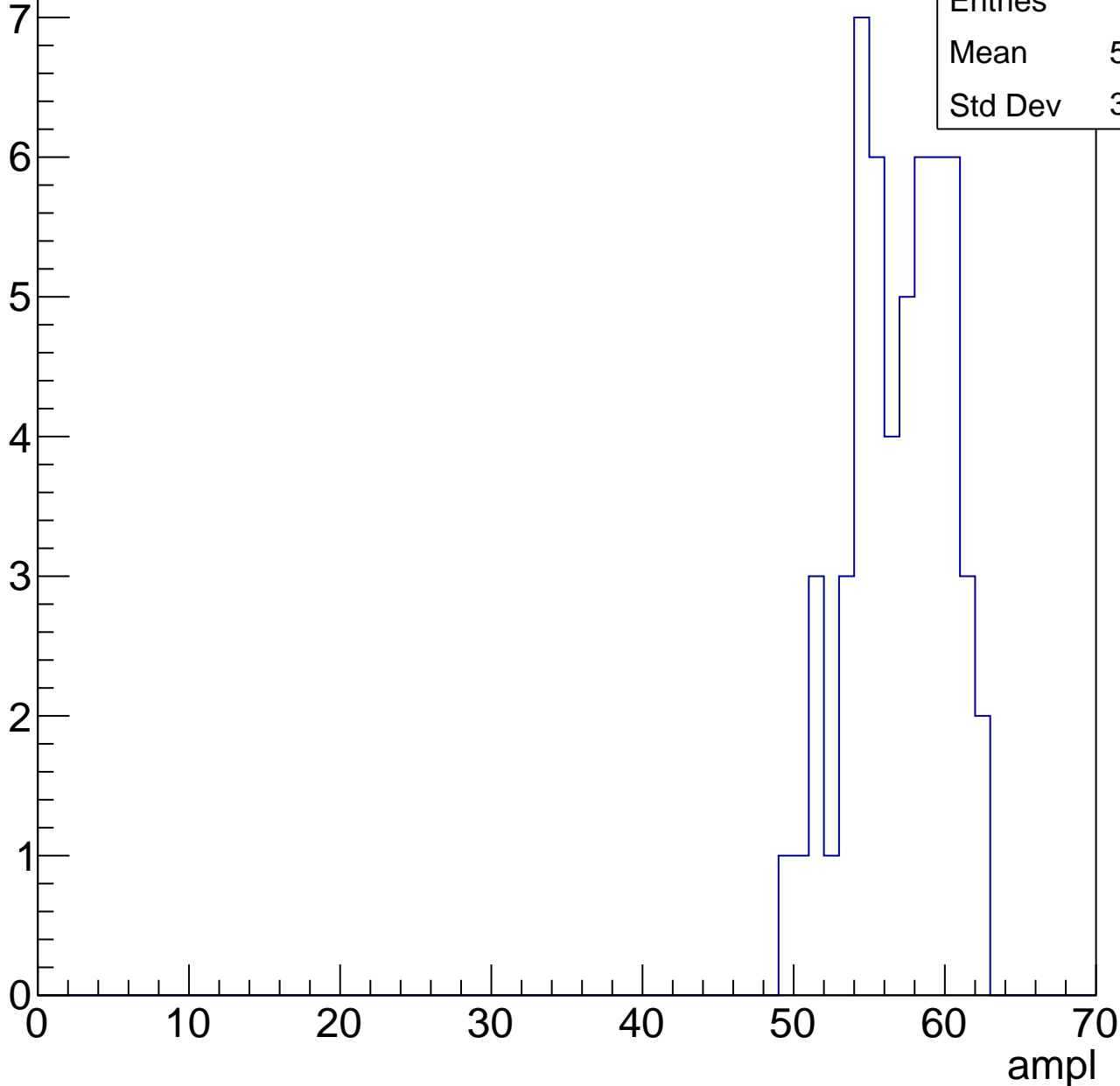
Entries	79
Mean	49.56
Std Dev	3.613

# B1L102S, U8-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	56.46
Std Dev	3.196

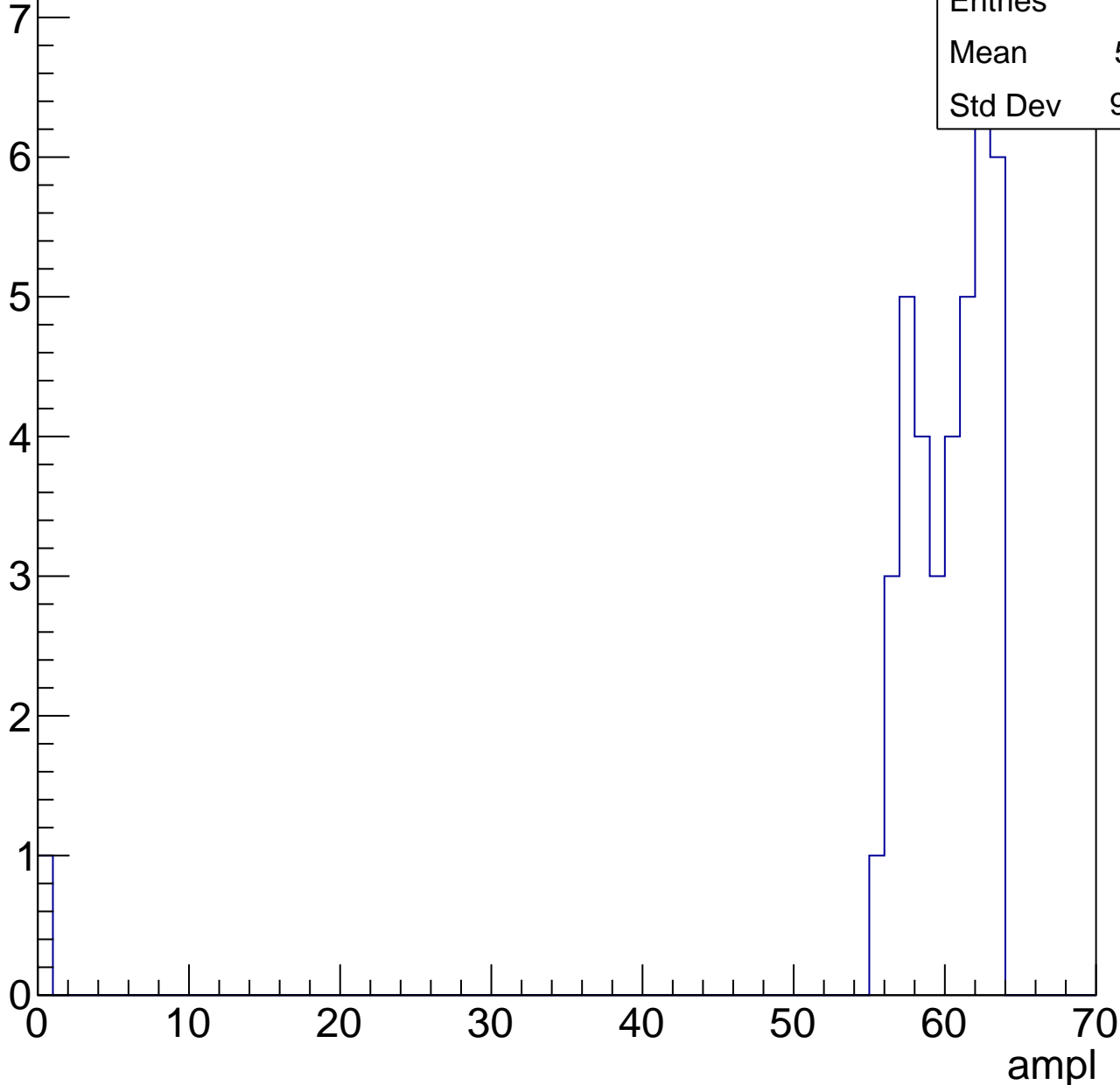


# B1L102S, U8-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

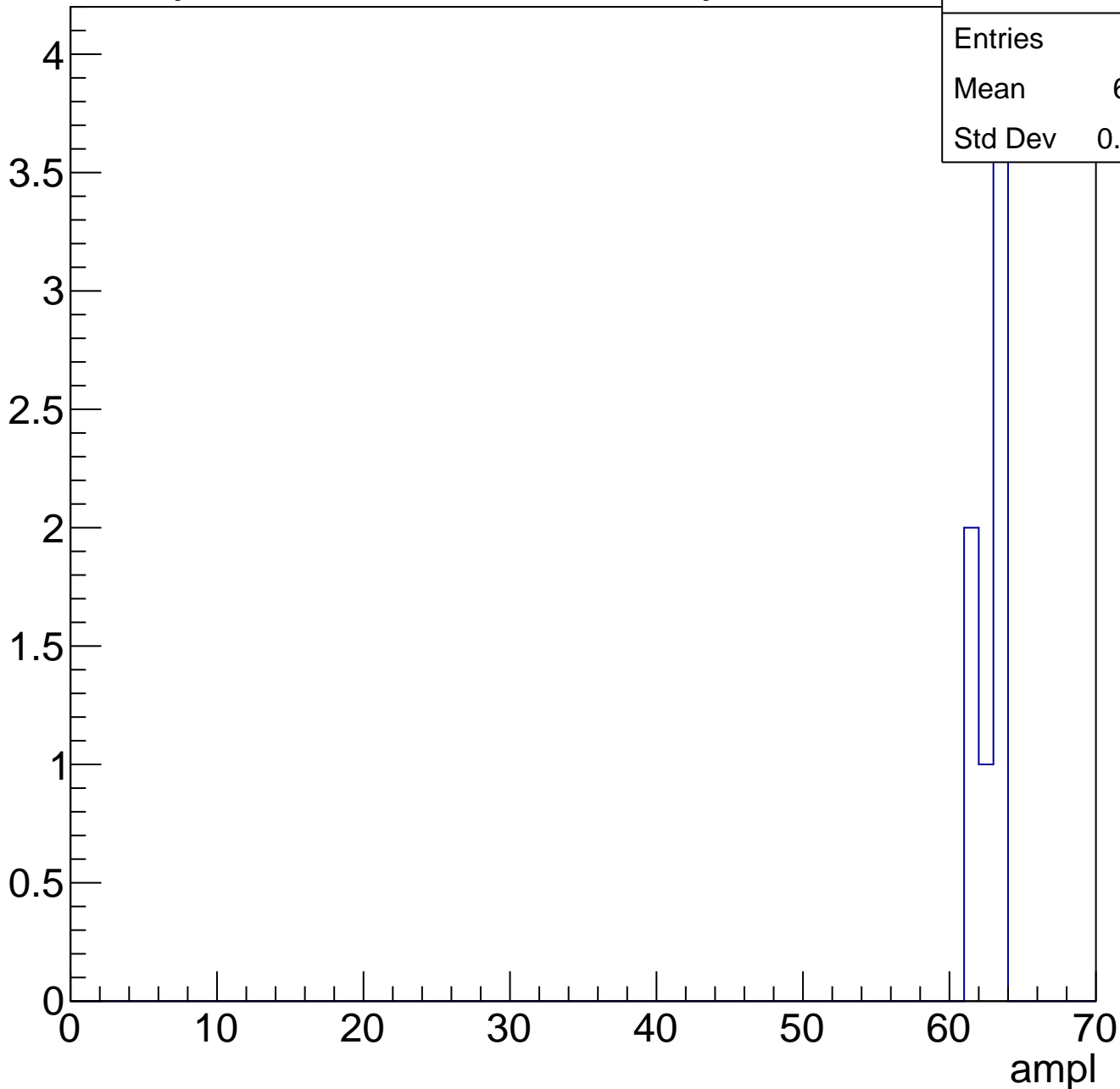
Entries	39
Mean	58.31
Std Dev	9.756



# B1L102S, U8-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch53, adc0

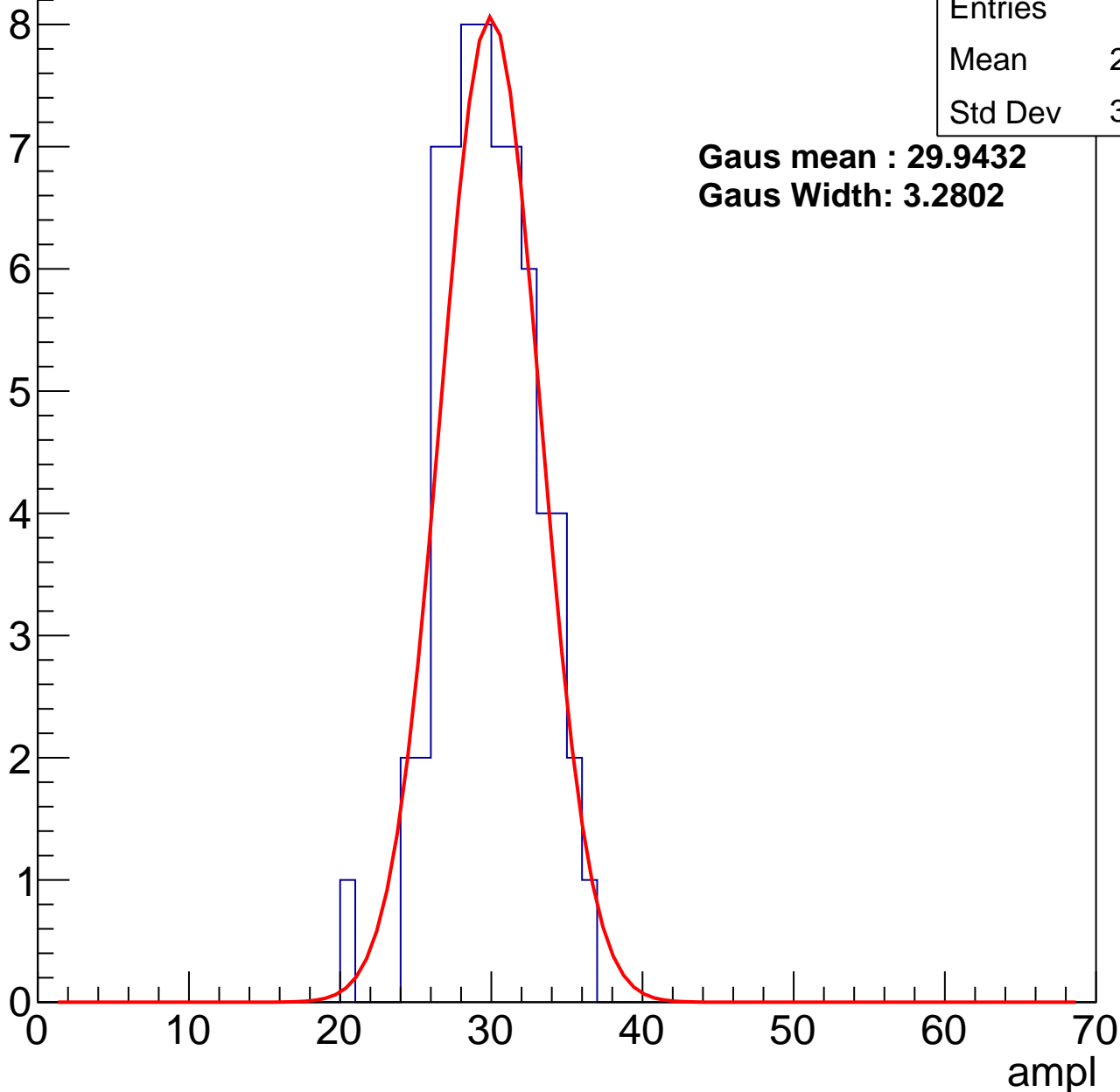
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	29.36
Std Dev	3.083

**Gaus mean : 29.9432**

**Gaus Width: 3.2802**



# B1L102S, U8-ch53, adc1

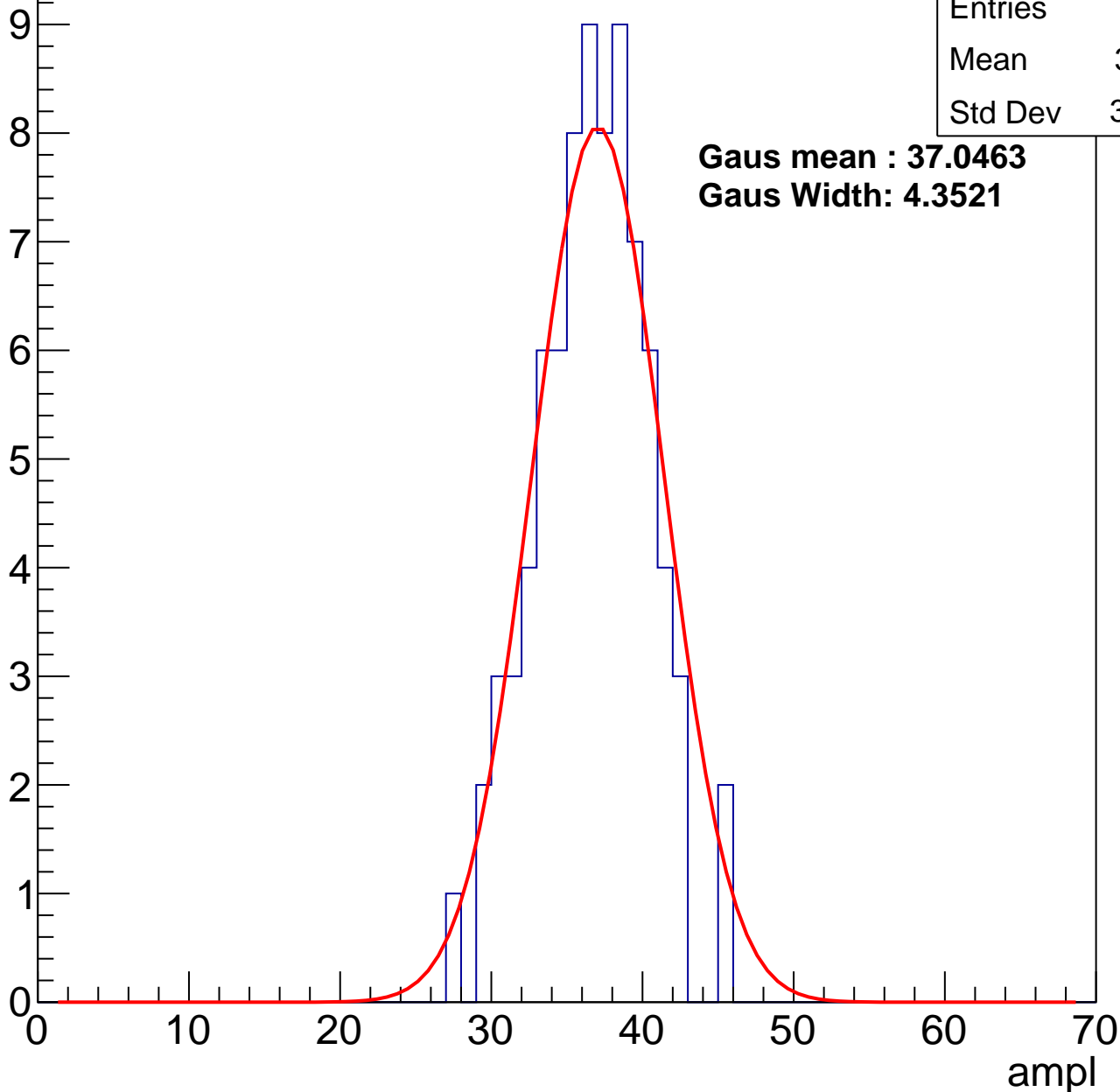
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	81
Mean	36.21
Std Dev	3.654

**Gaus mean : 37.0463**

**Gaus Width: 4.3521**



# B1L102S, U8-ch53, adc2

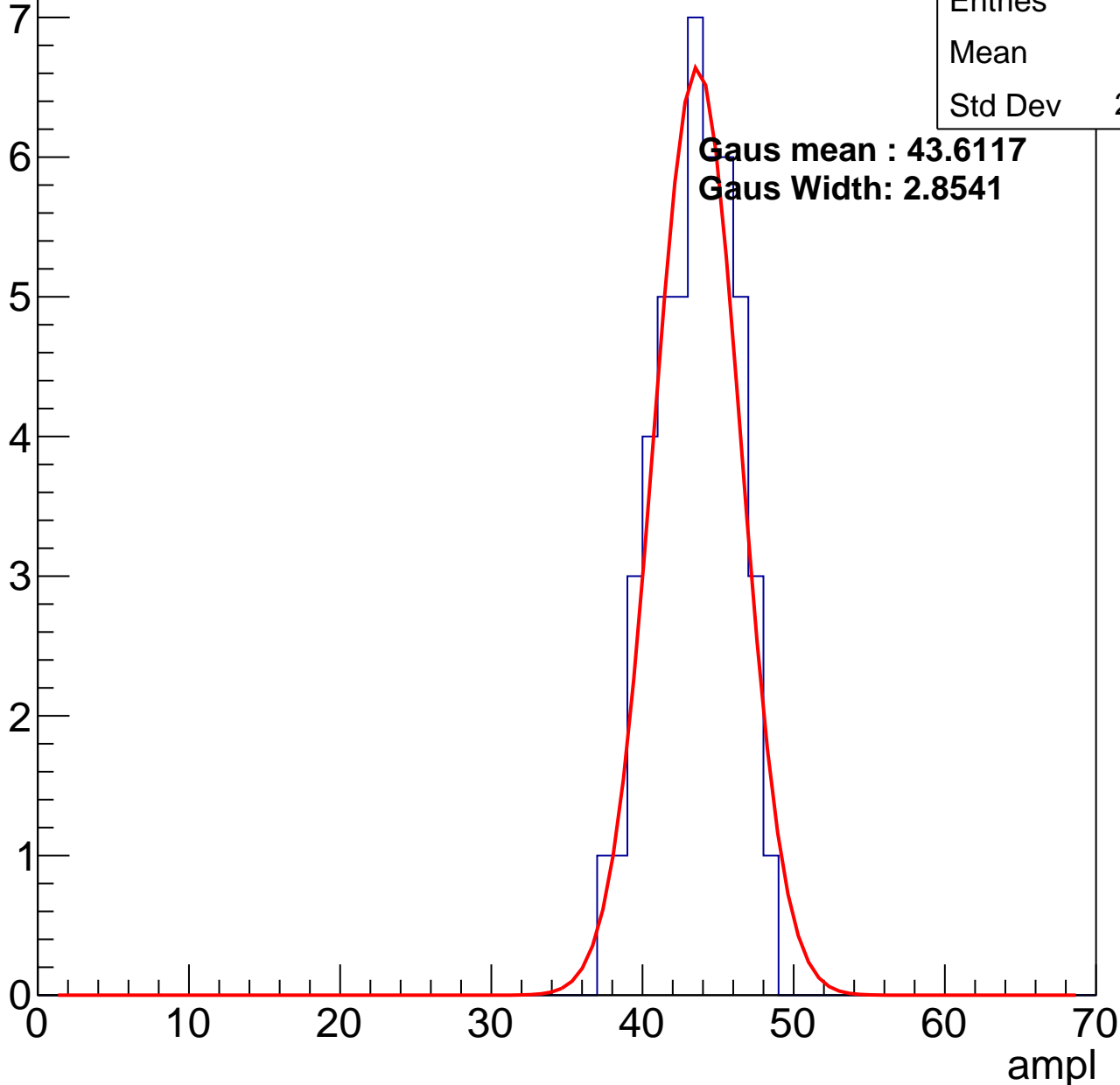
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	43
Std Dev	2.601

**Gaus mean : 43.6117**

**Gaus Width: 2.8541**

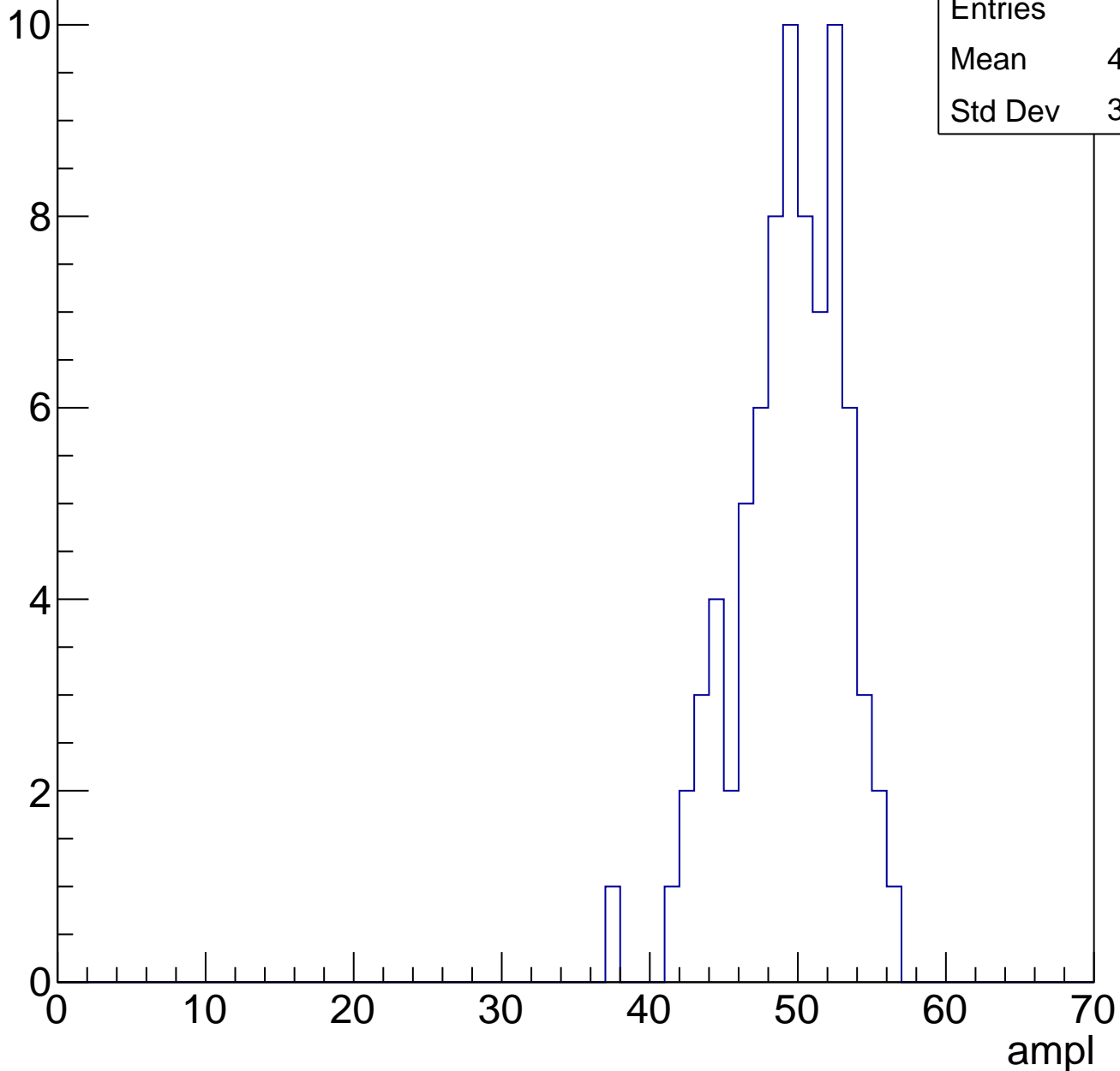


# B1L102S, U8-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	79
Mean	48.94
Std Dev	3.629

Entry

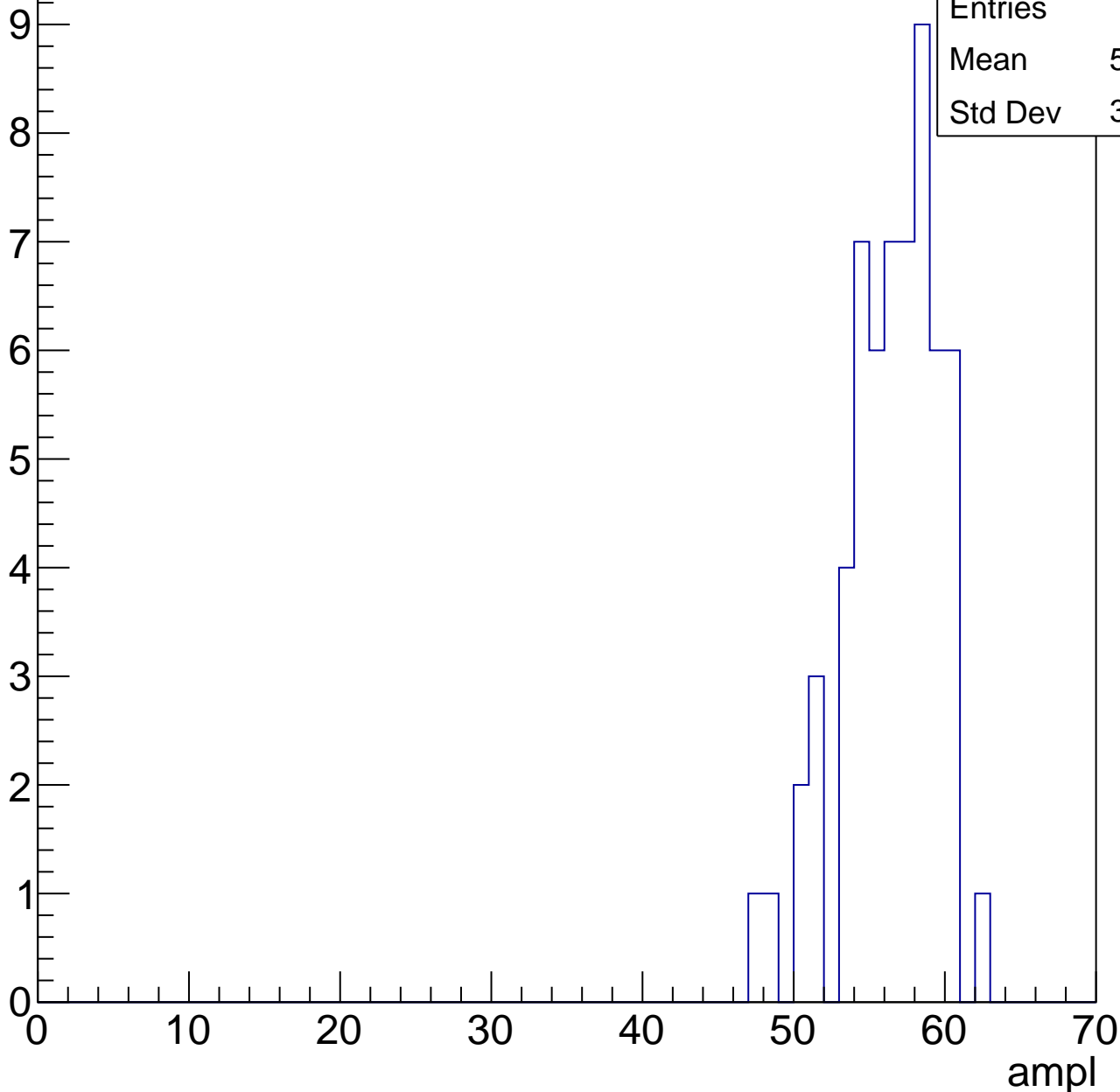


# B1L102S, U8-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	55.95
Std Dev	3.138



# B1L102S, U8-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	40
Mean	58.77
Std Dev	9.691

ampl

0 10 20 30 40 50 60 70

1

2

3

4

5

6

7

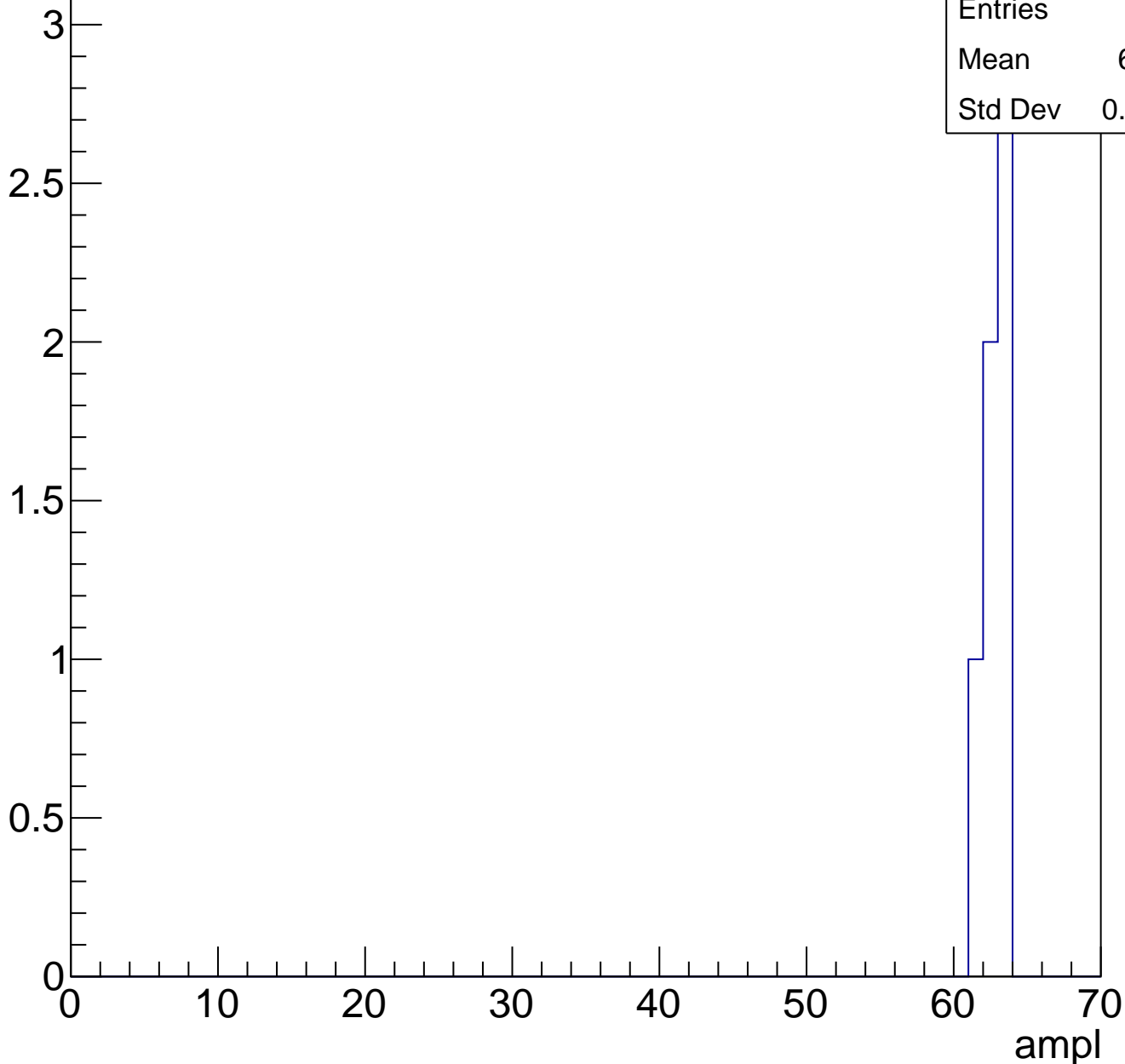
8

9

# B1L102S, U8-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch54, adc0

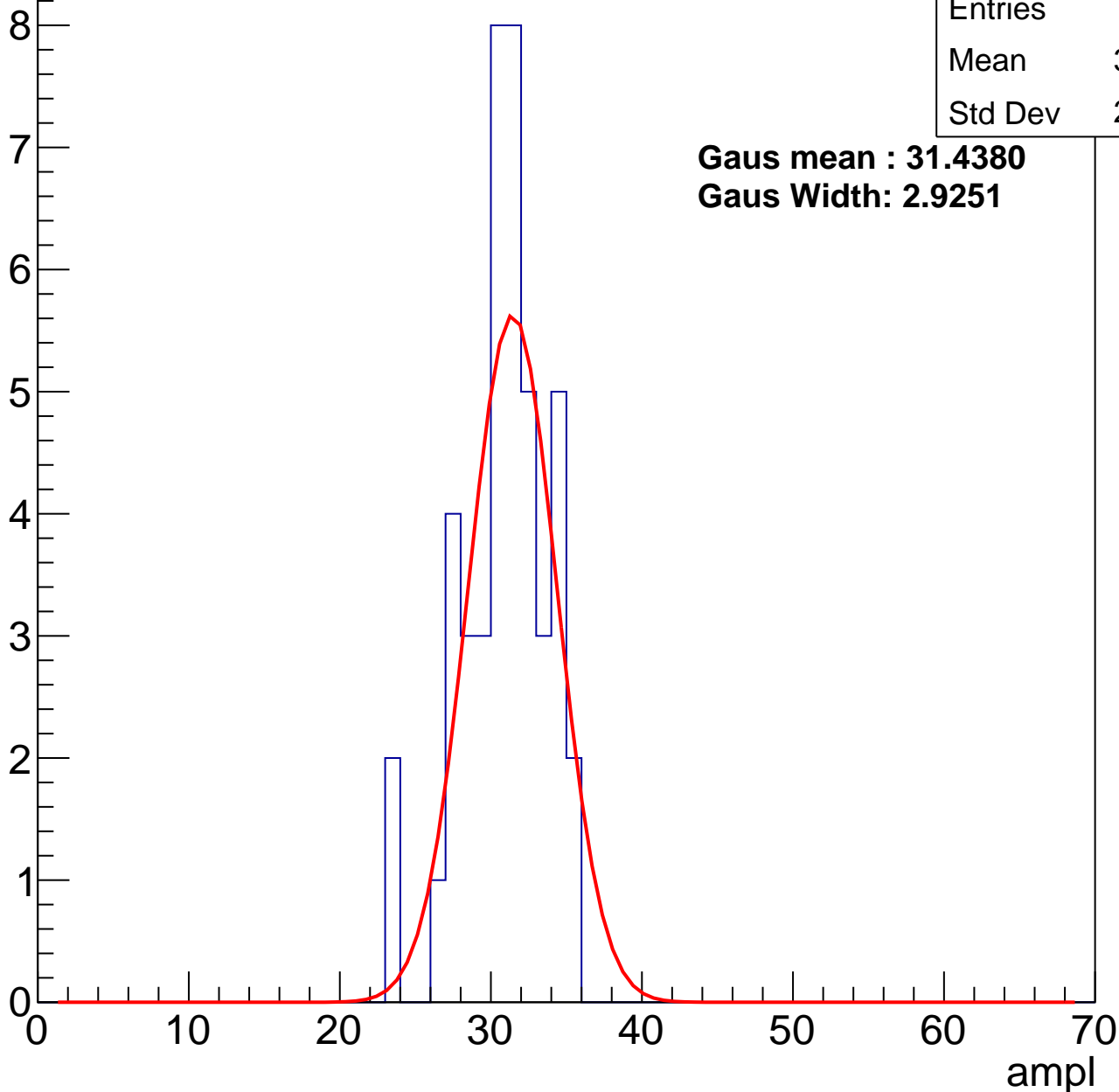
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	44
Mean	30.41
Std Dev	2.791

**Gaus mean : 31.4380**

**Gaus Width: 2.9251**



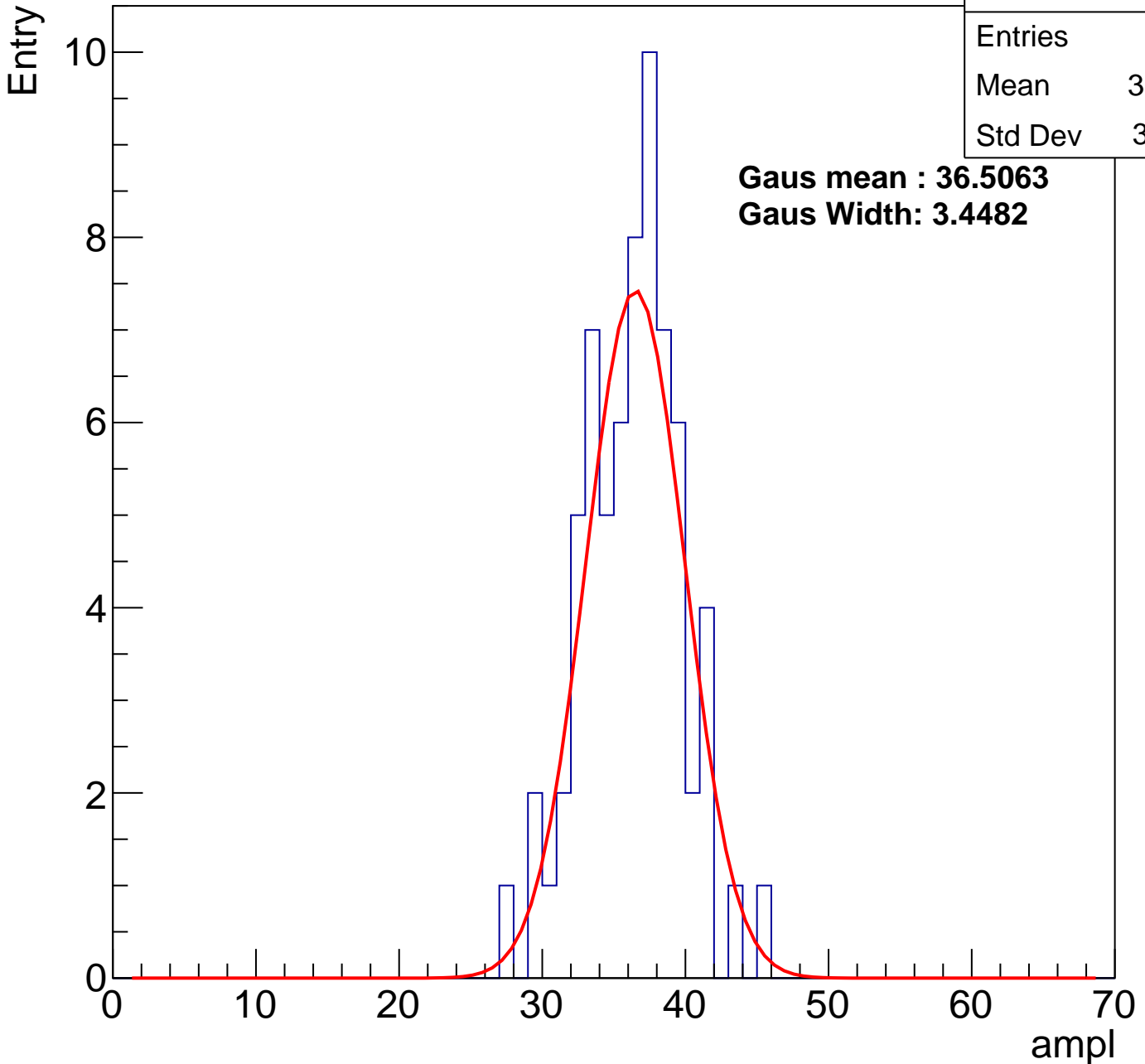
# B1L102S, U8-ch54, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	68
Mean	35.85
Std Dev	3.401

**Gaus mean : 36.5063**

**Gaus Width: 3.4482**



# B1L102S, U8-ch54, adc2

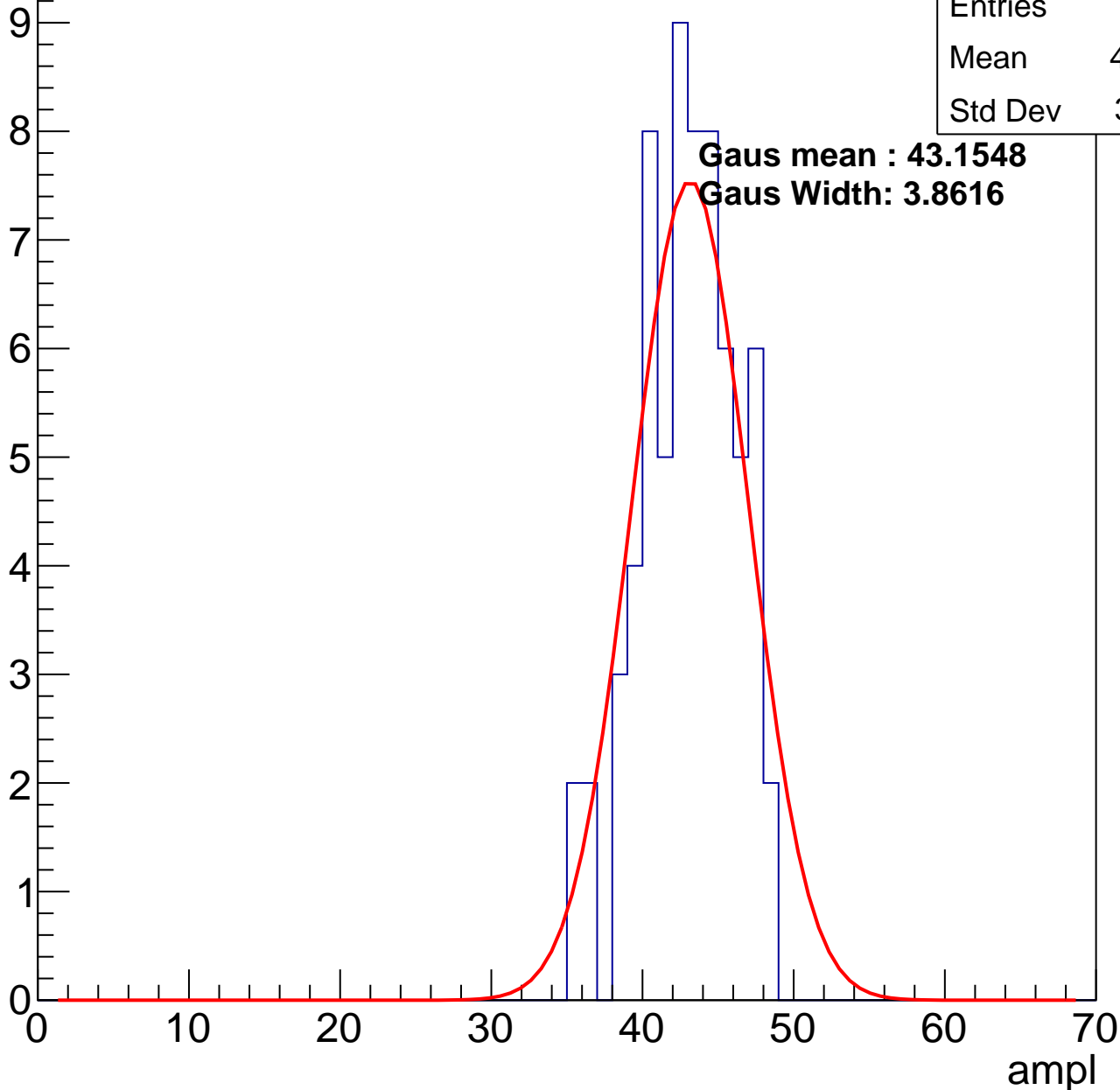
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	42.49
Std Dev	3.141

**Gaus mean : 43.1548**

**Gaus Width: 3.8616**

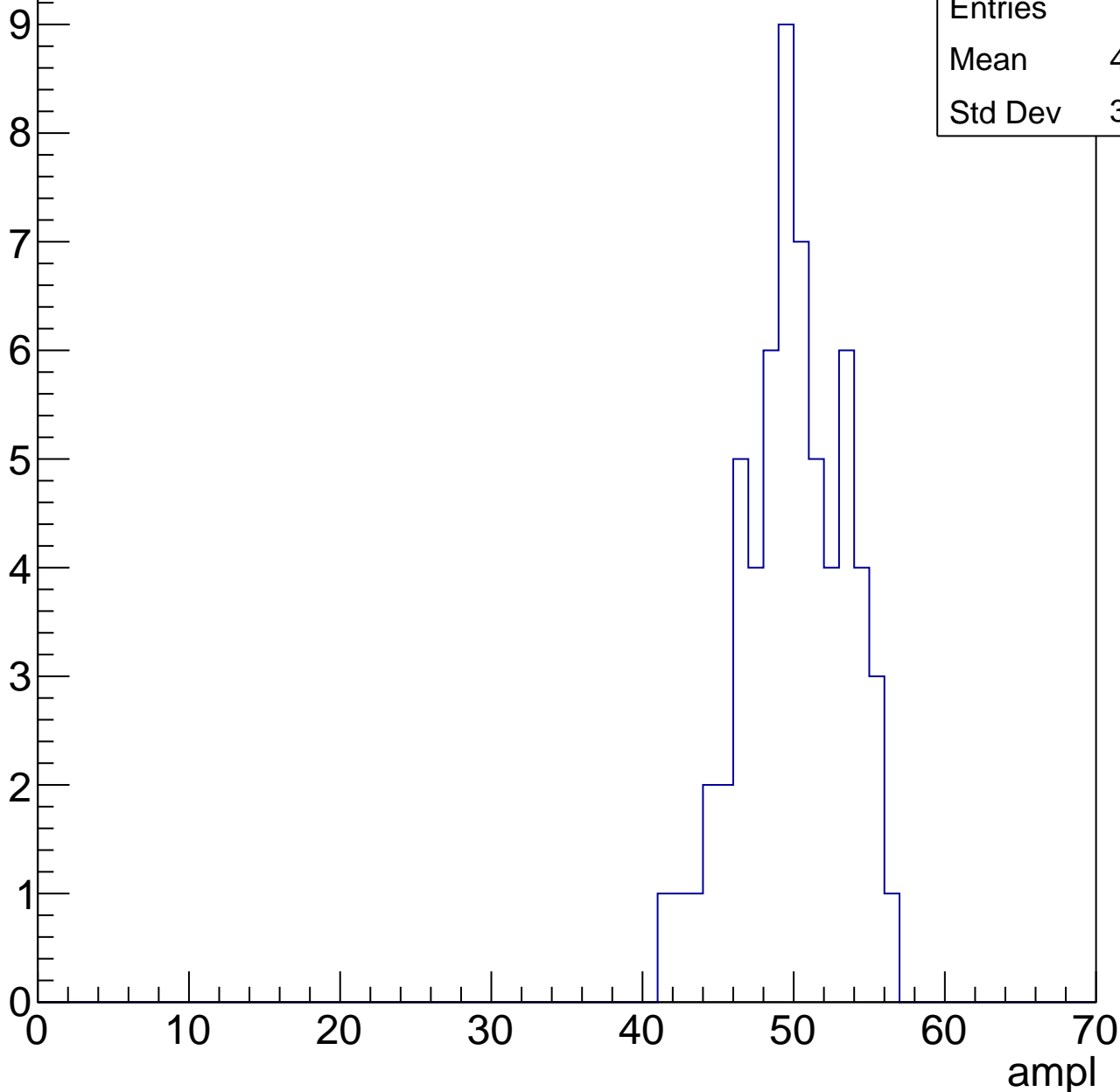


# B1L102S, U8-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	49.49
Std Dev	3.386

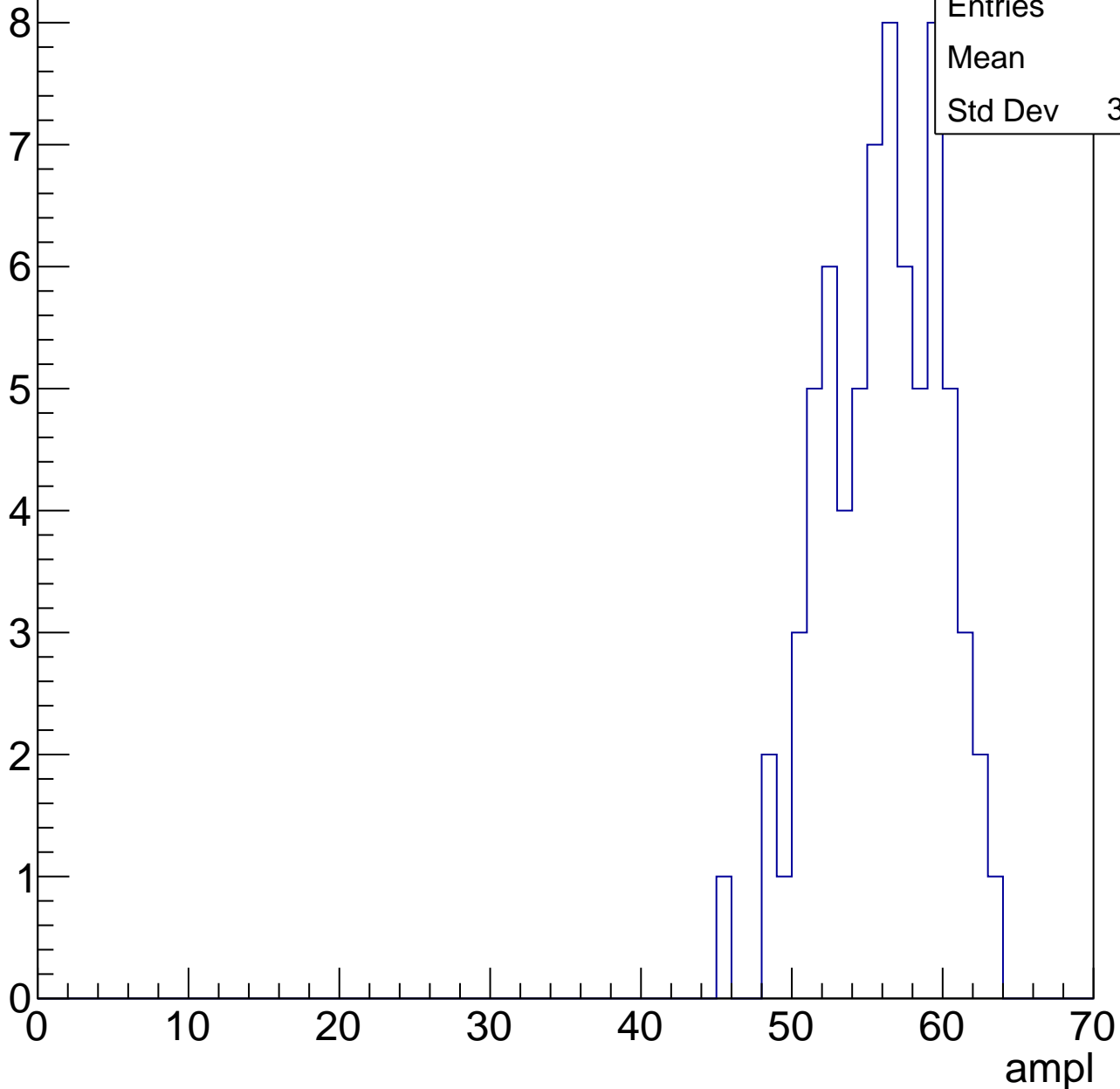


# B1L102S, U8-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	55.5
Std Dev	3.812

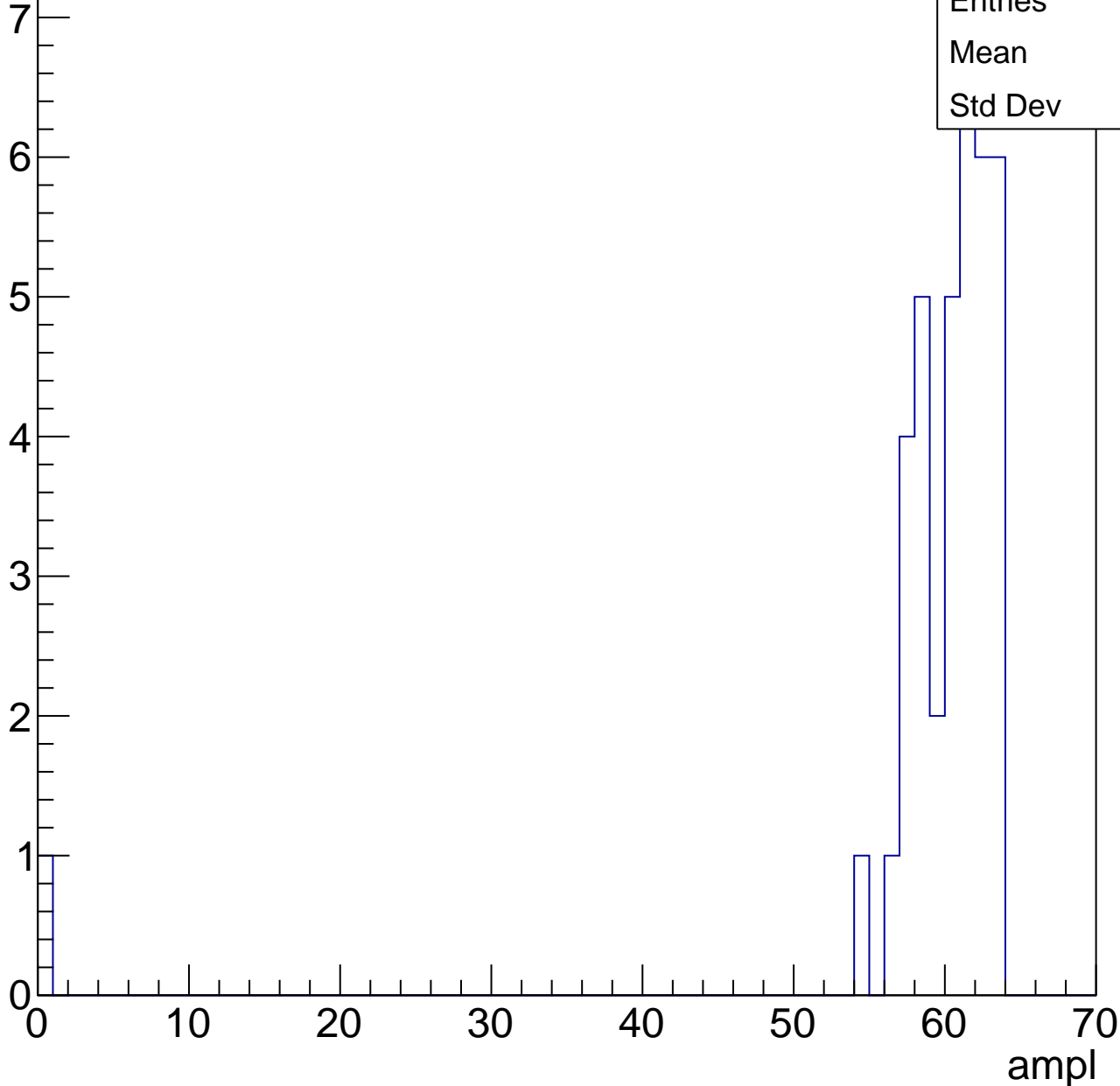


# B1L102S, U8-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	38
Mean	58.5
Std Dev	9.88



# B1L102S, U8-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	10
Std Dev	10

# B1L102S, U8-ch55, adc0

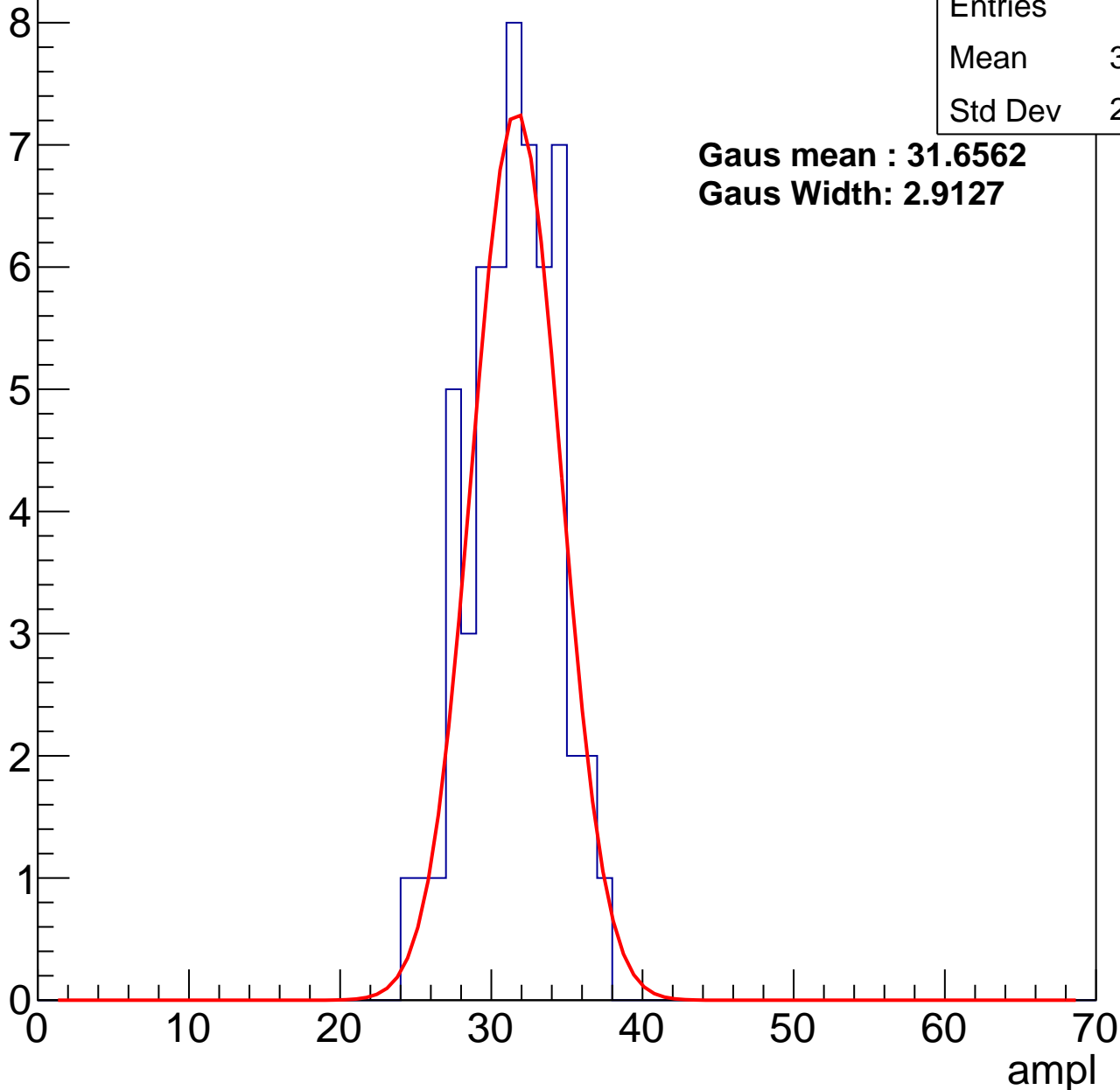
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	30.98
Std Dev	2.863

**Gaus mean : 31.6562**

**Gaus Width: 2.9127**



# B1L102S, U8-ch55, adc1

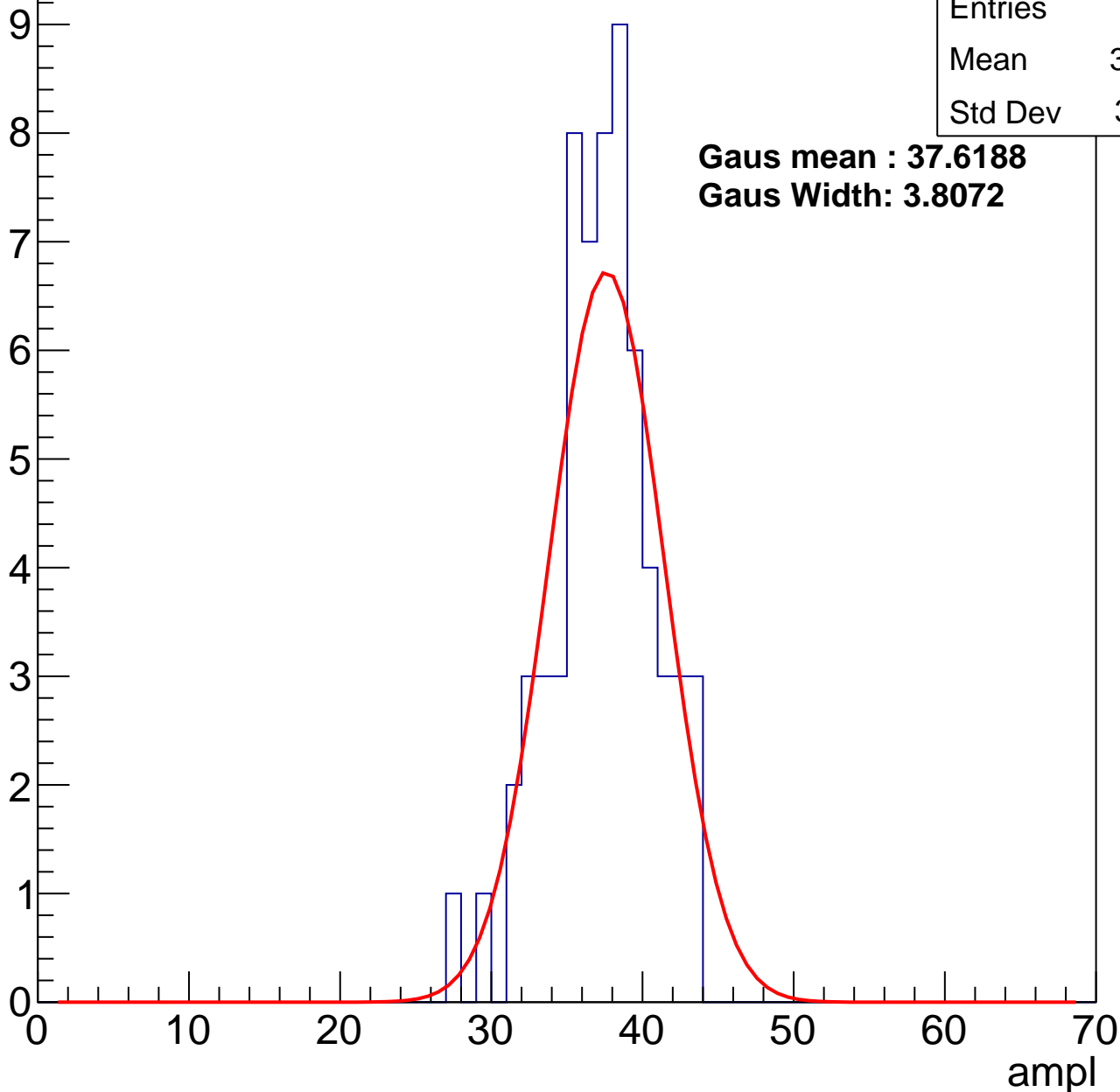
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	36.83
Std Dev	3.361

**Gaus mean : 37.6188**

**Gaus Width: 3.8072**



# B1L102S, U8-ch55, adc2

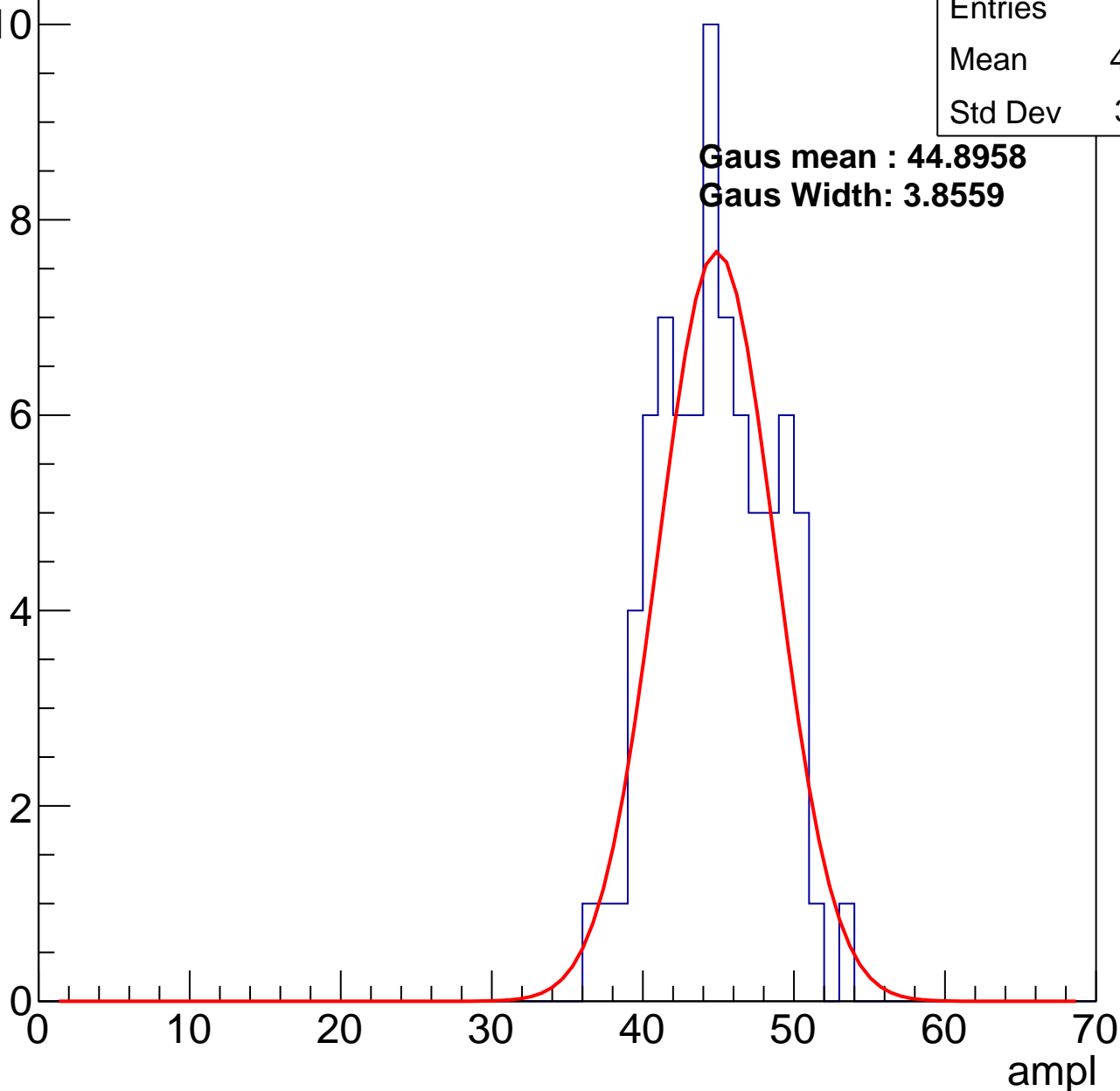
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	44.33
Std Dev	3.661

**Gaus mean : 44.8958**

**Gaus Width: 3.8559**

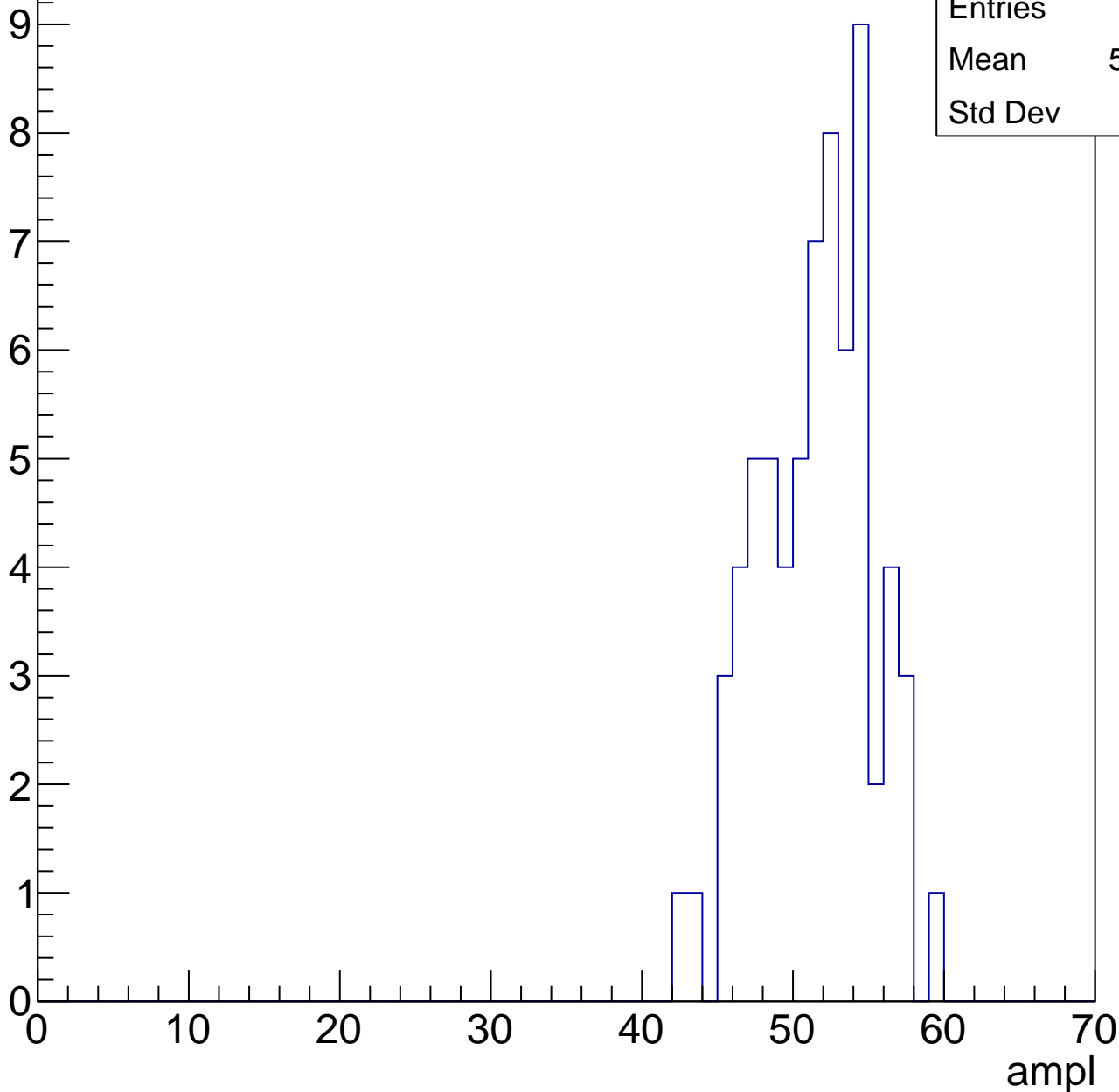


# B1L102S, U8-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	50.97
Std Dev	3.67

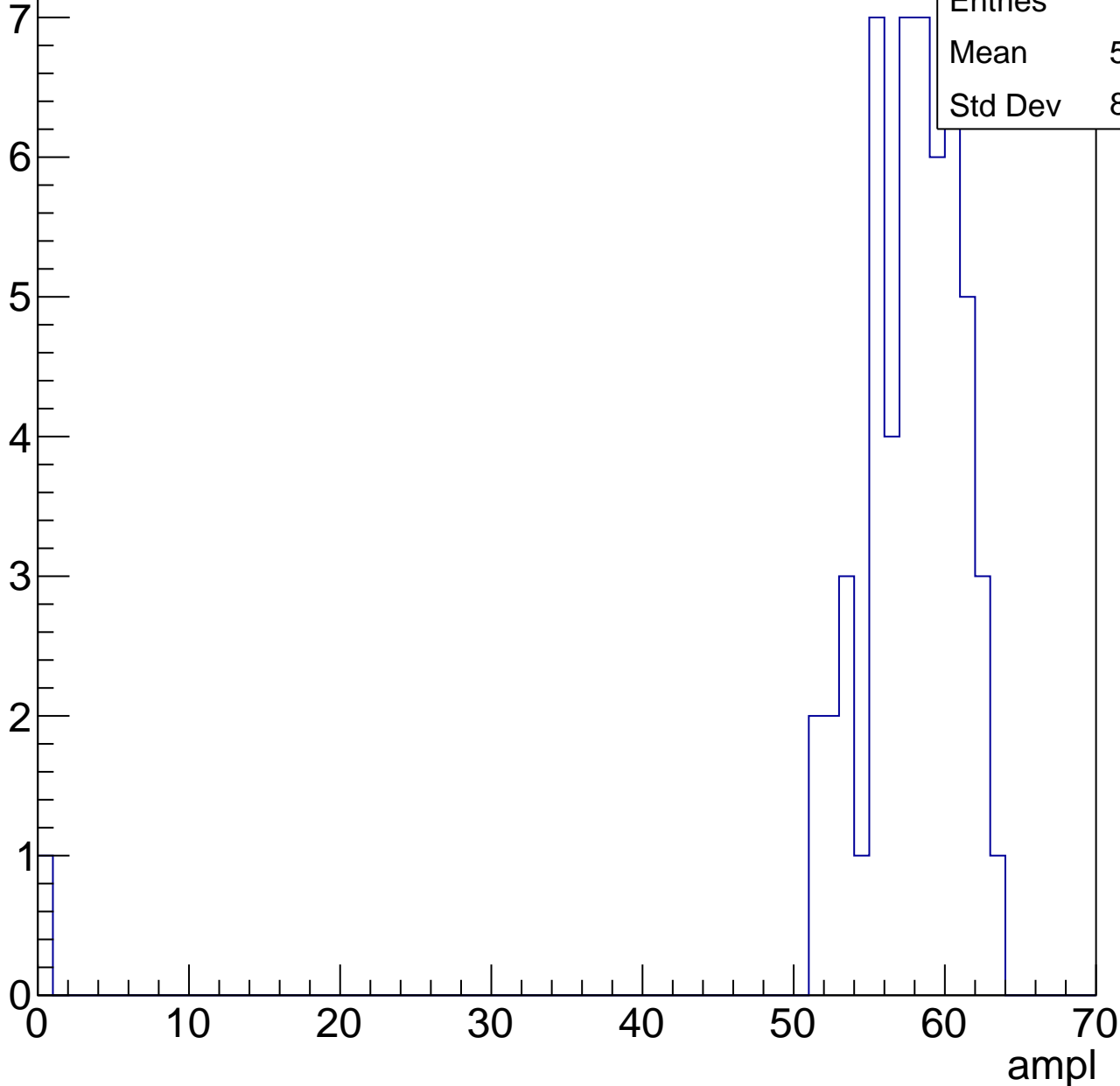


# B1L102S, U8-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	56.45
Std Dev	8.159

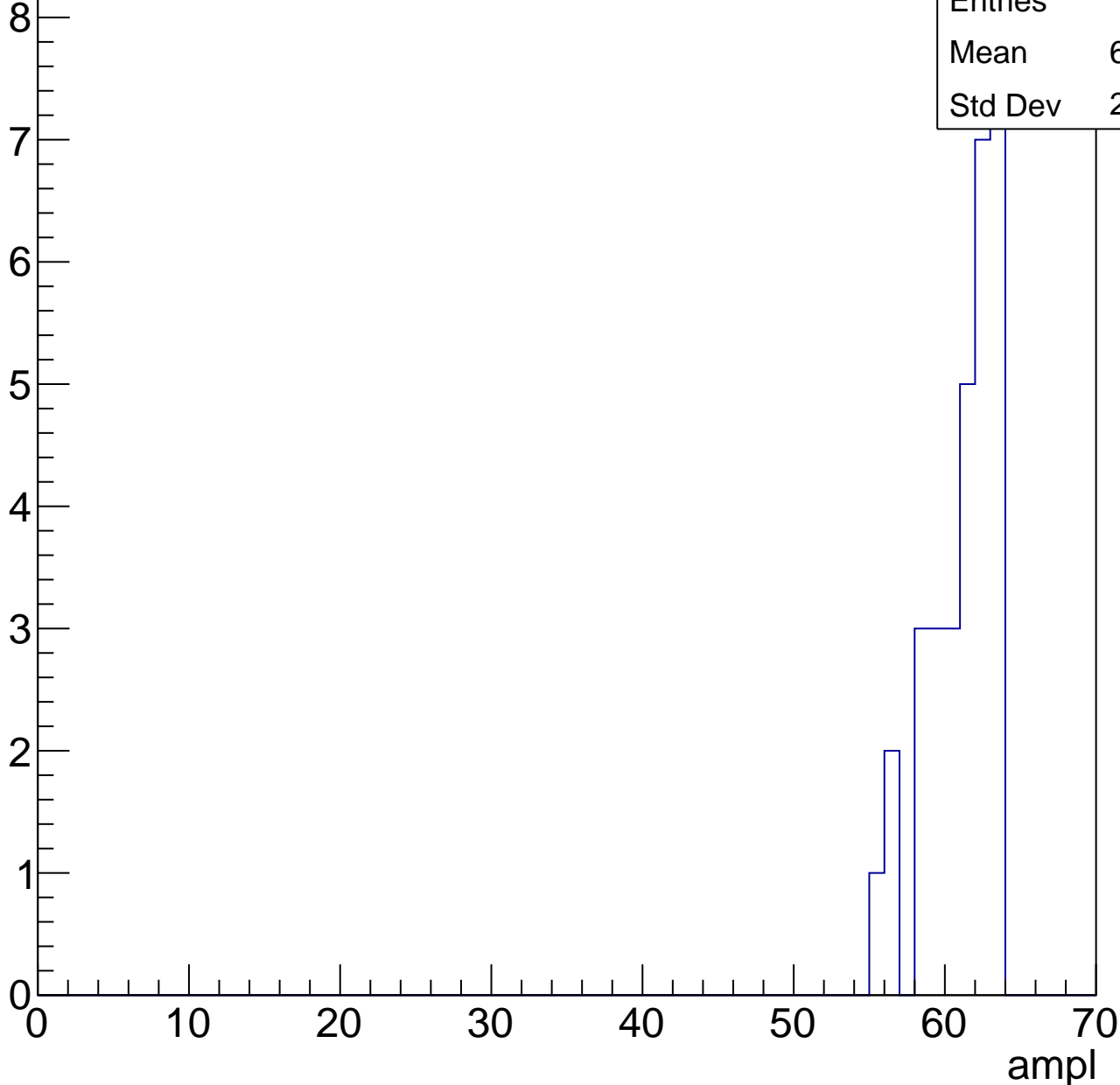


# B1L102S, U8-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

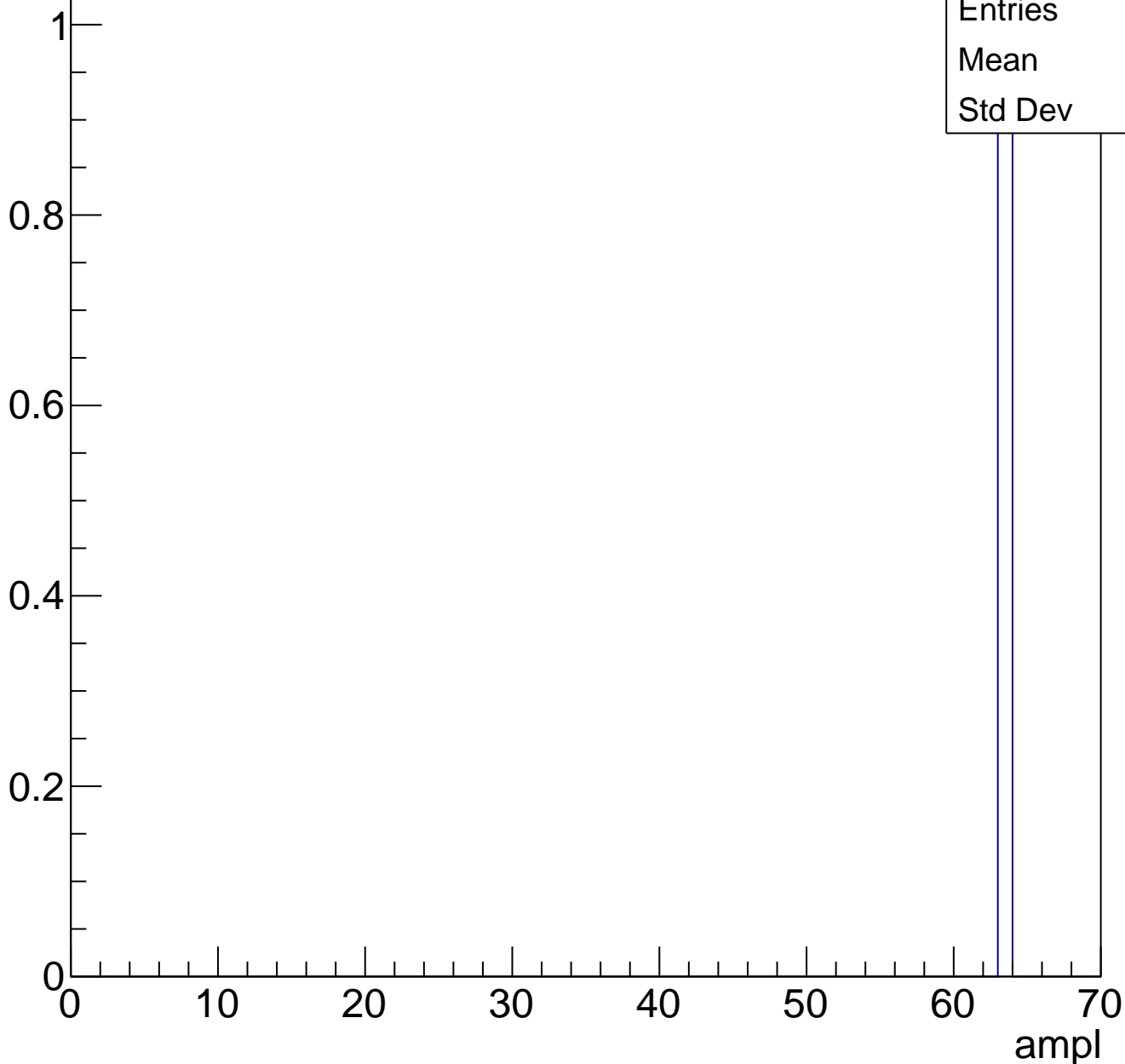
Entries	32
Mean	60.66
Std Dev	2.258



# B1L102S, U8-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U8-ch56, adc0

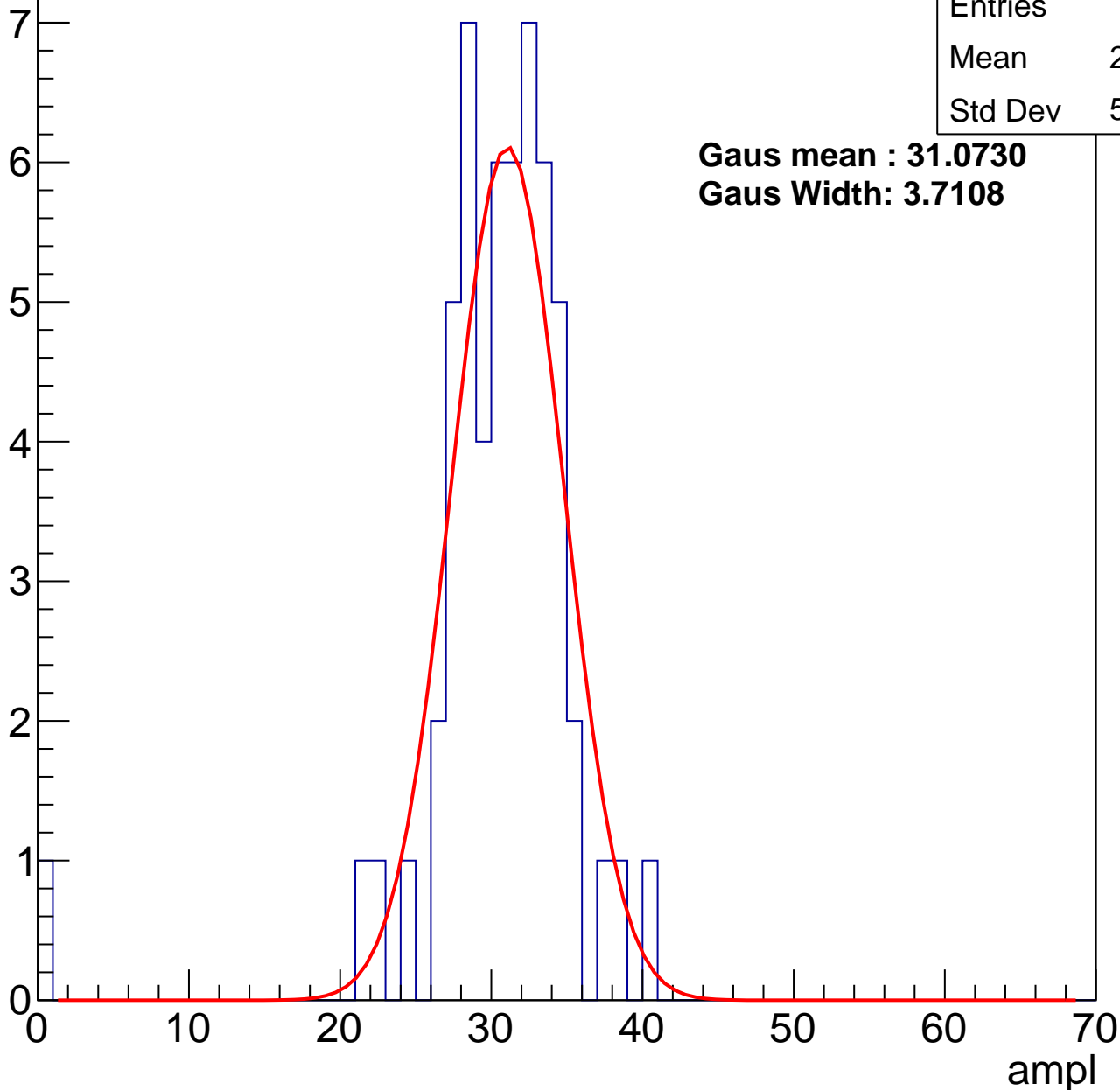
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	29.98
Std Dev	5.333

**Gaus mean : 31.0730**

**Gaus Width: 3.7108**



# B1L102S, U8-ch56, adc1

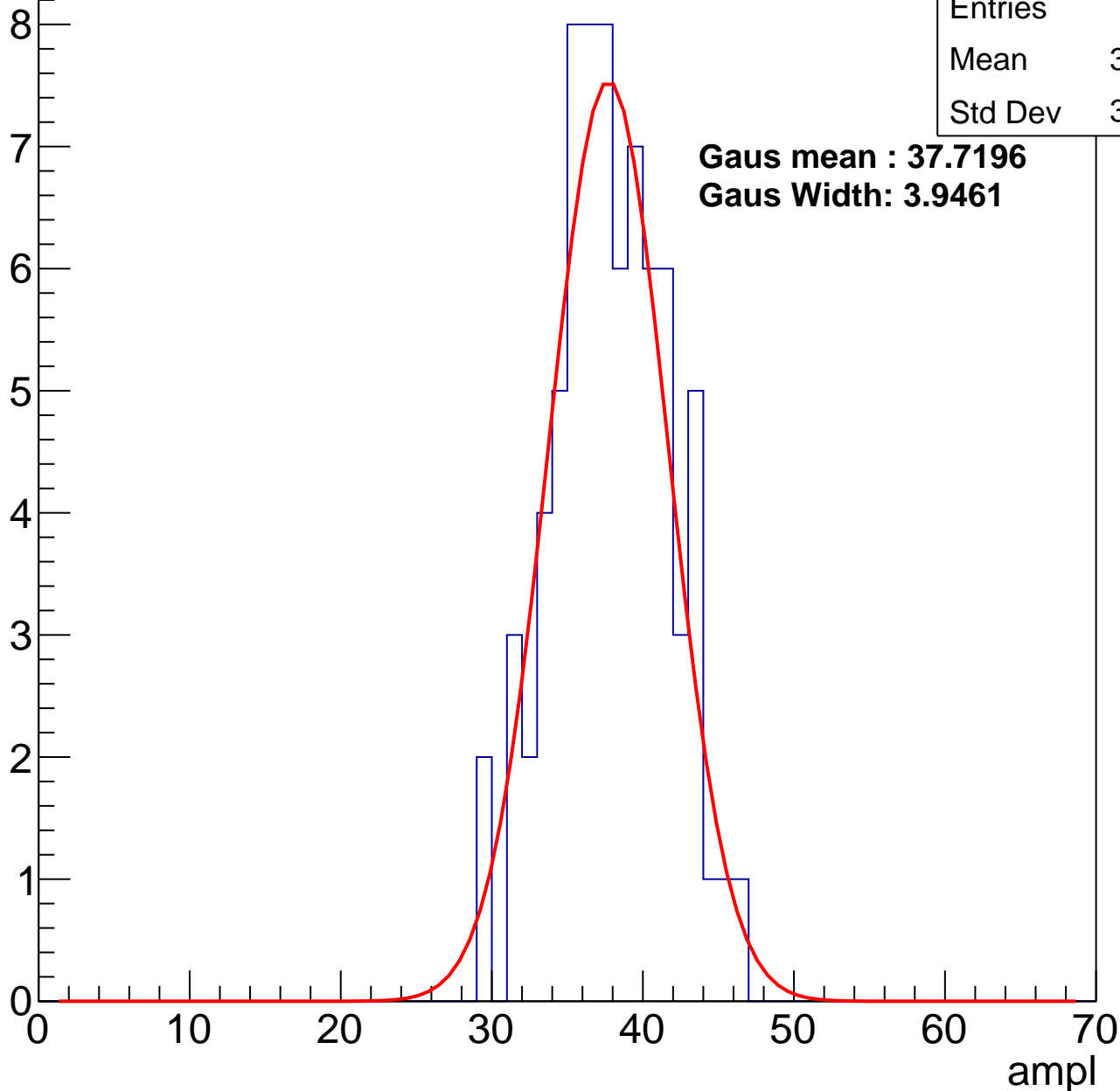
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	37.42
Std Dev	3.725

**Gaus mean : 37.7196**

**Gaus Width: 3.9461**



# B1L102S, U8-ch56, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	70
Mean	44.17
Std Dev	3.66

**Gaus mean : 44.6229**

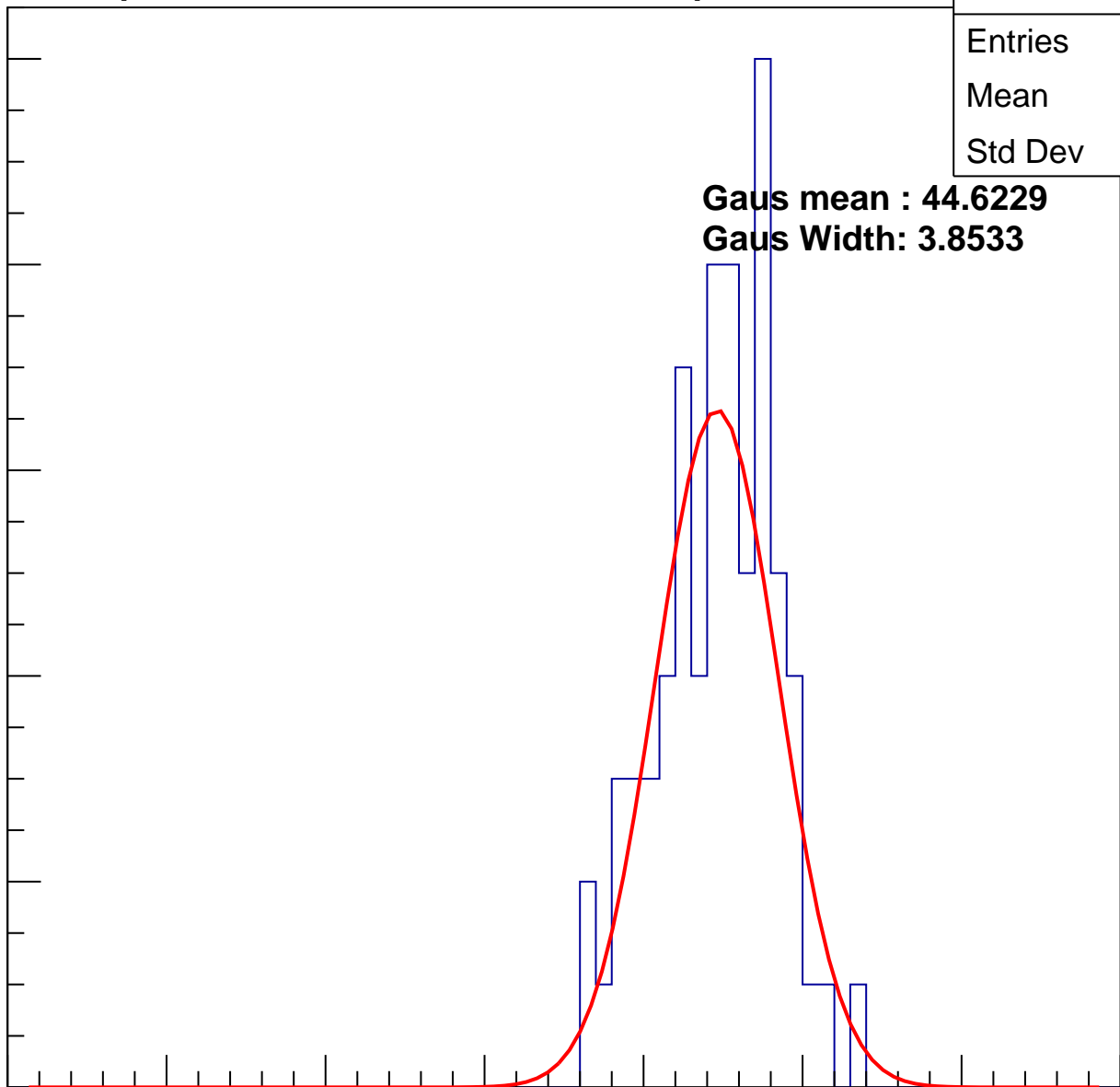
**Gaus Width: 3.8533**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

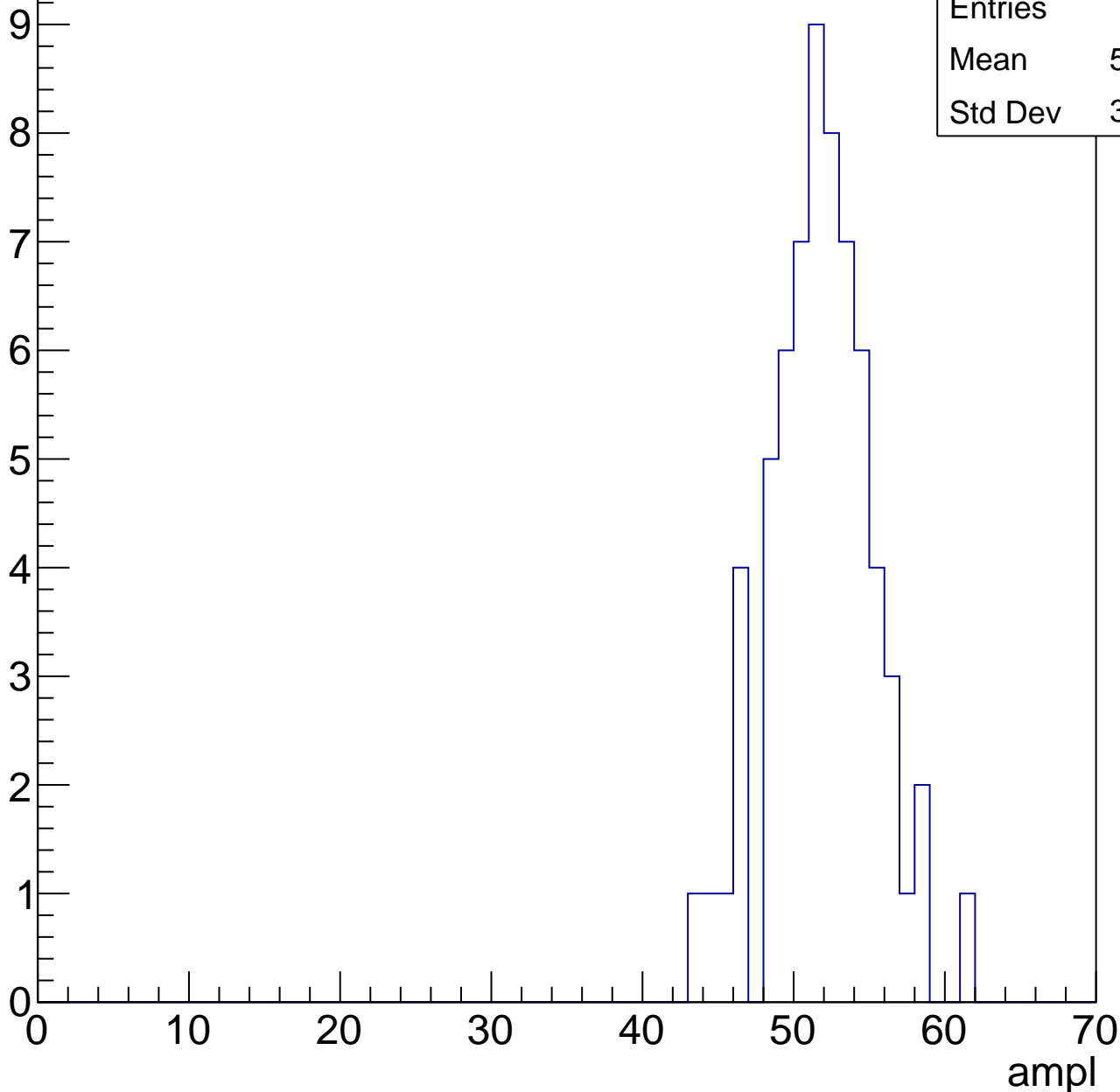


# B1L102S, U8-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	51.39
Std Dev	3.433

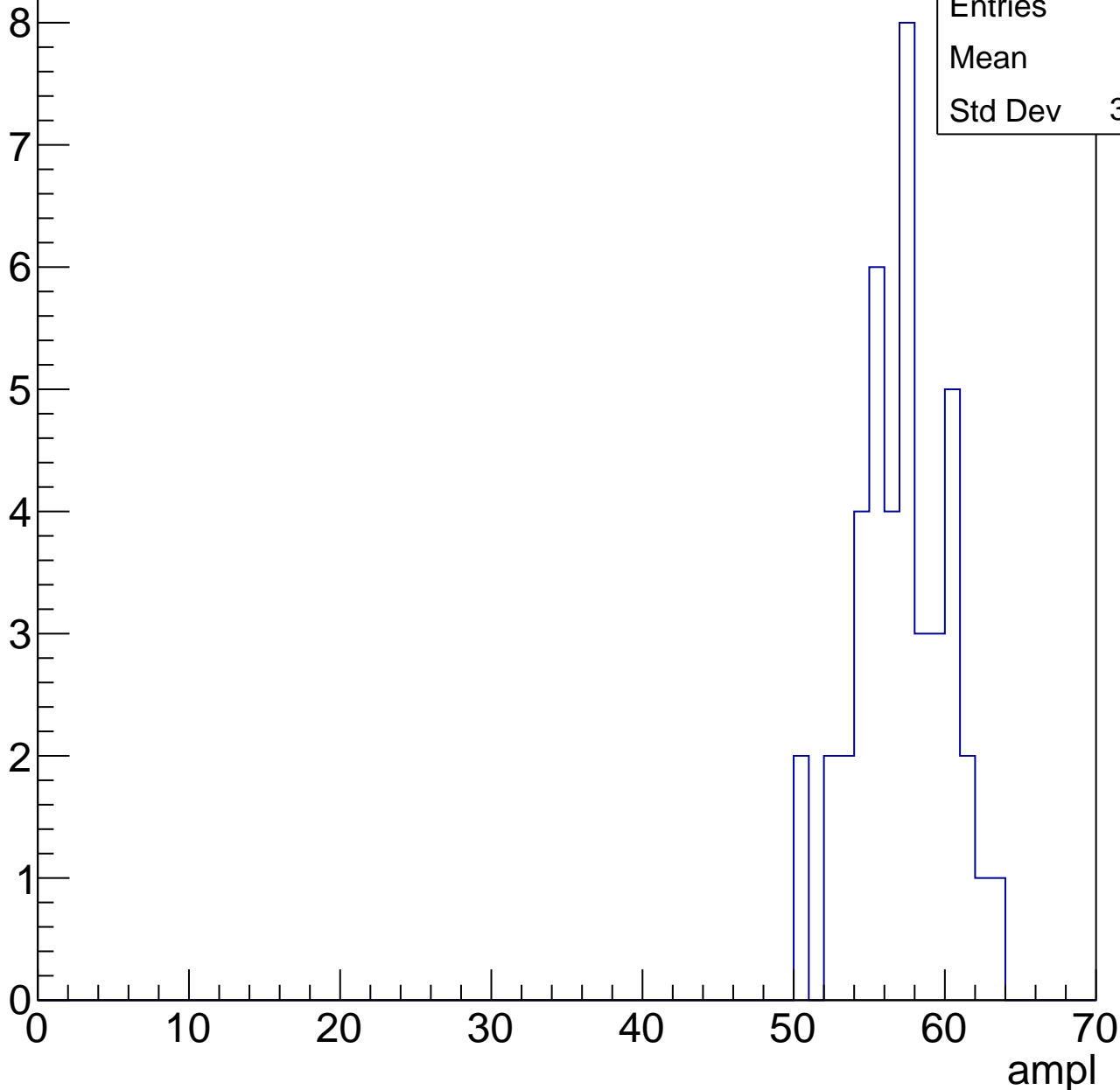


# B1L102S, U8-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	43
Mean	56.6
Std Dev	3.013

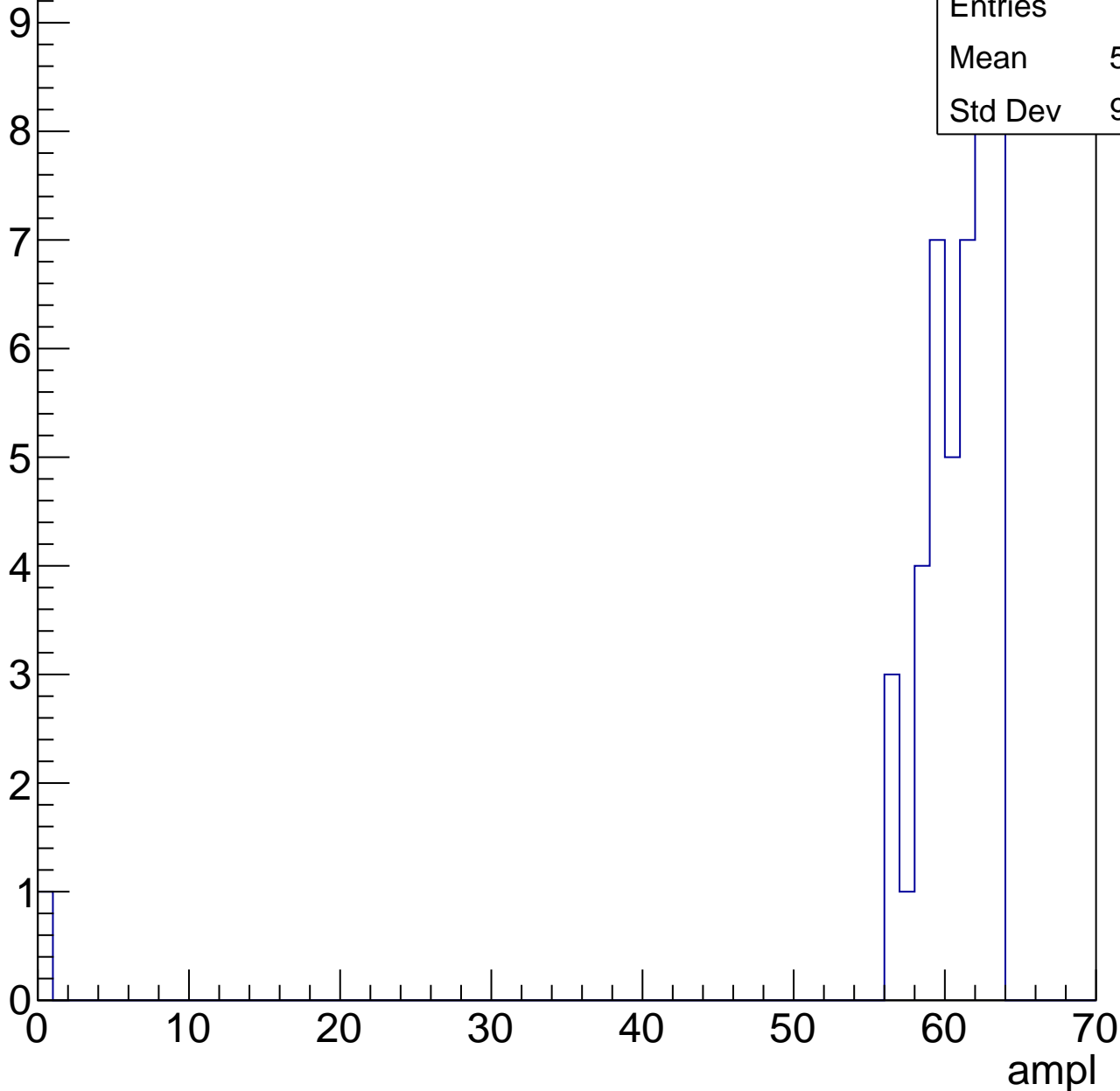


# B1L102S, U8-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

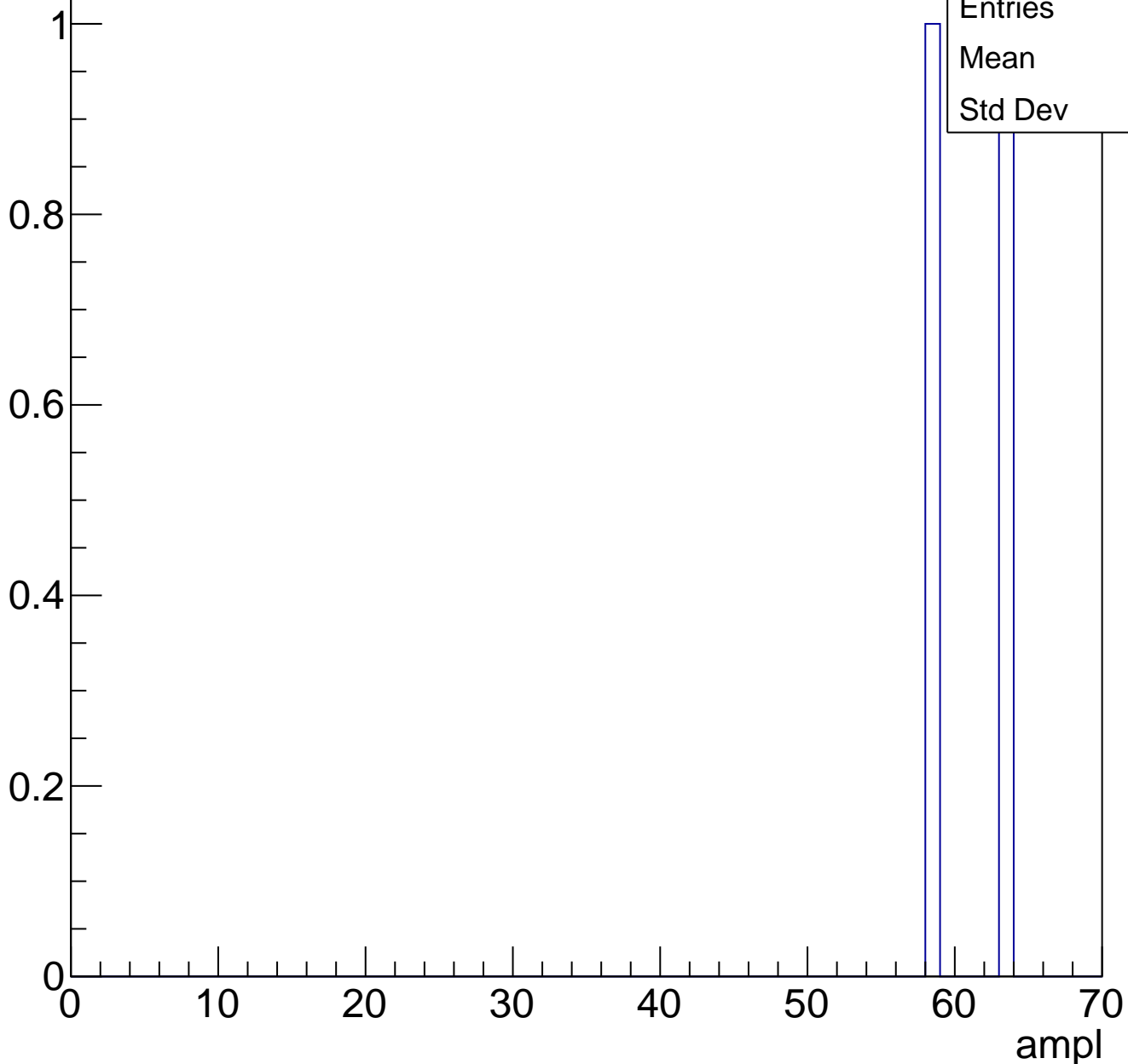
Entries	45
Mean	59.09
Std Dev	9.138



# B1L102S, U8-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch57, adc0

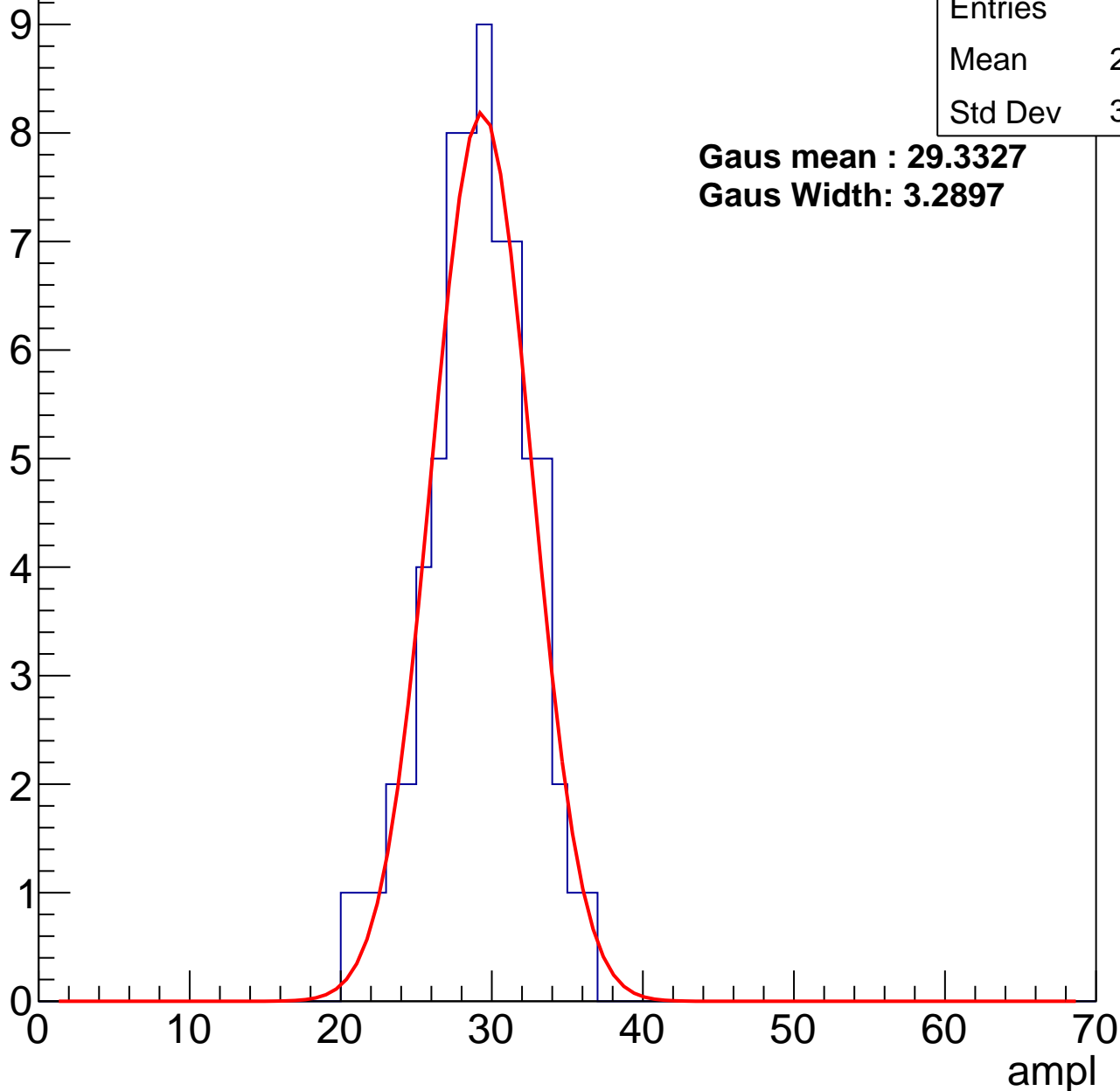
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	28.68
Std Dev	3.303

**Gaus mean : 29.3327**

**Gaus Width: 3.2897**



# B1L102S, U8-ch57, adc1

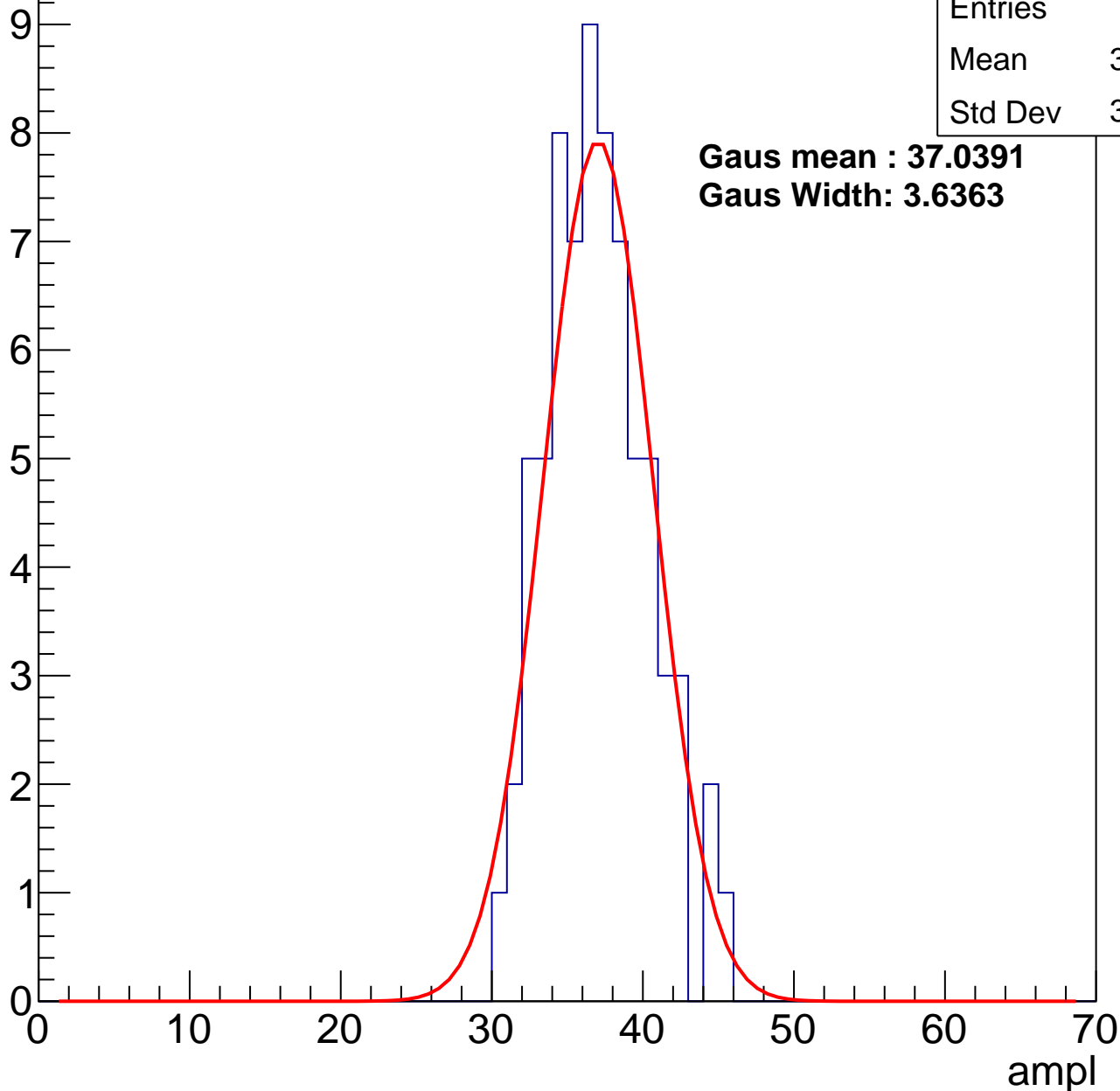
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	36.58
Std Dev	3.313

**Gaus mean : 37.0391**

**Gaus Width: 3.6363**



# B1L102S, U8-ch57, adc2

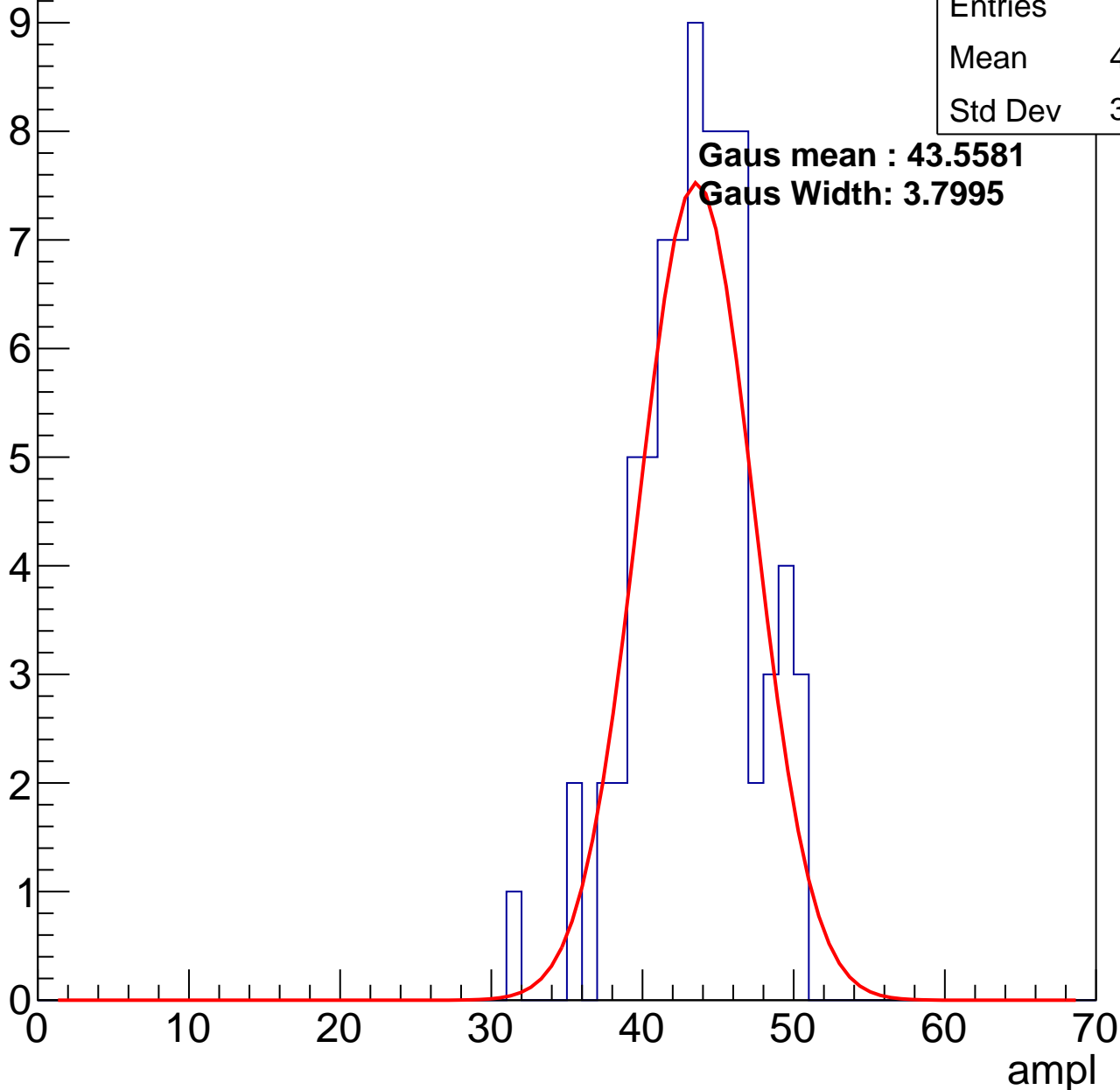
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	43.13
Std Dev	3.739

**Gaus mean : 43.5581**

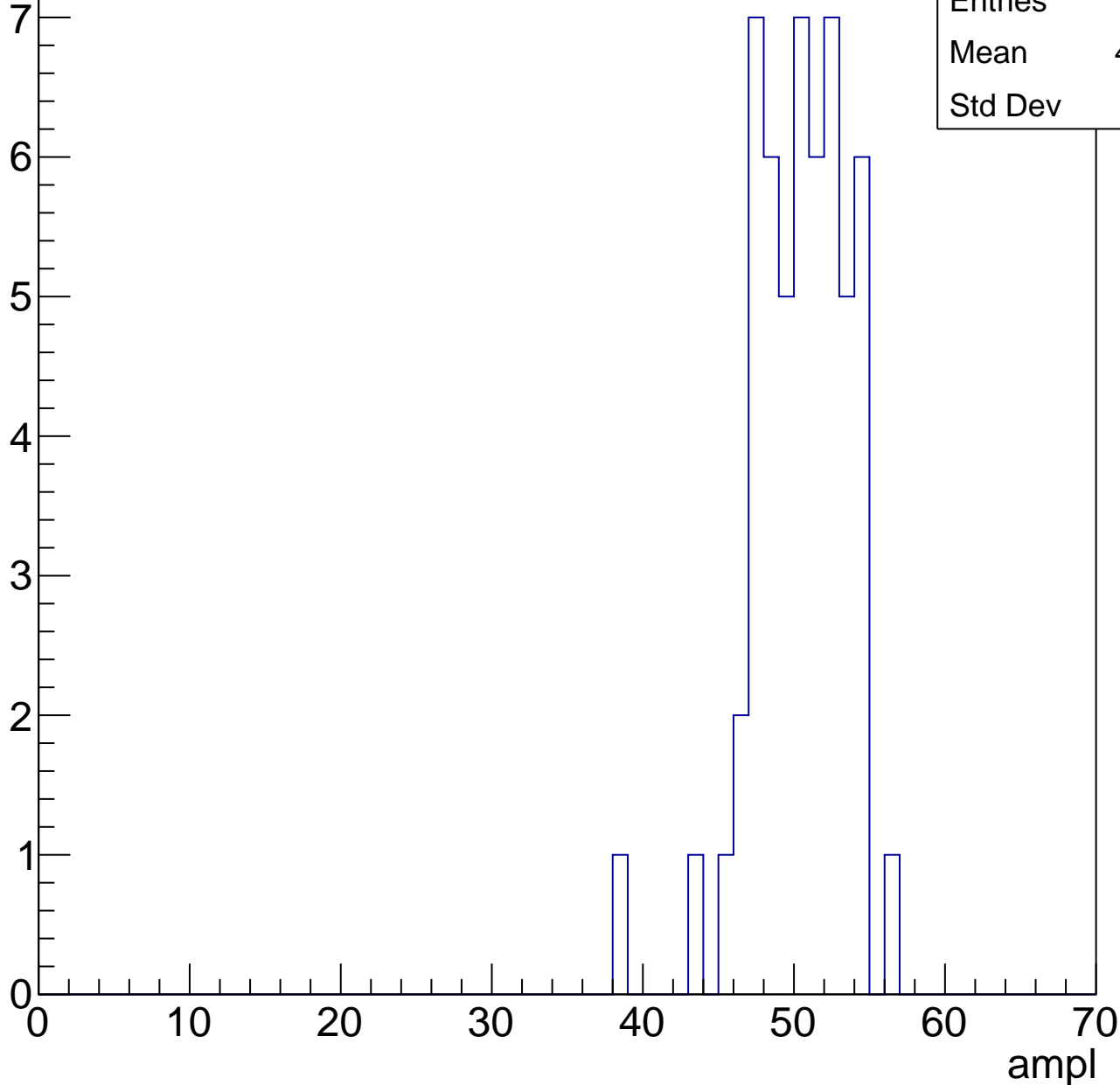
**Gaus Width: 3.7995**



# B1L102S, U8-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

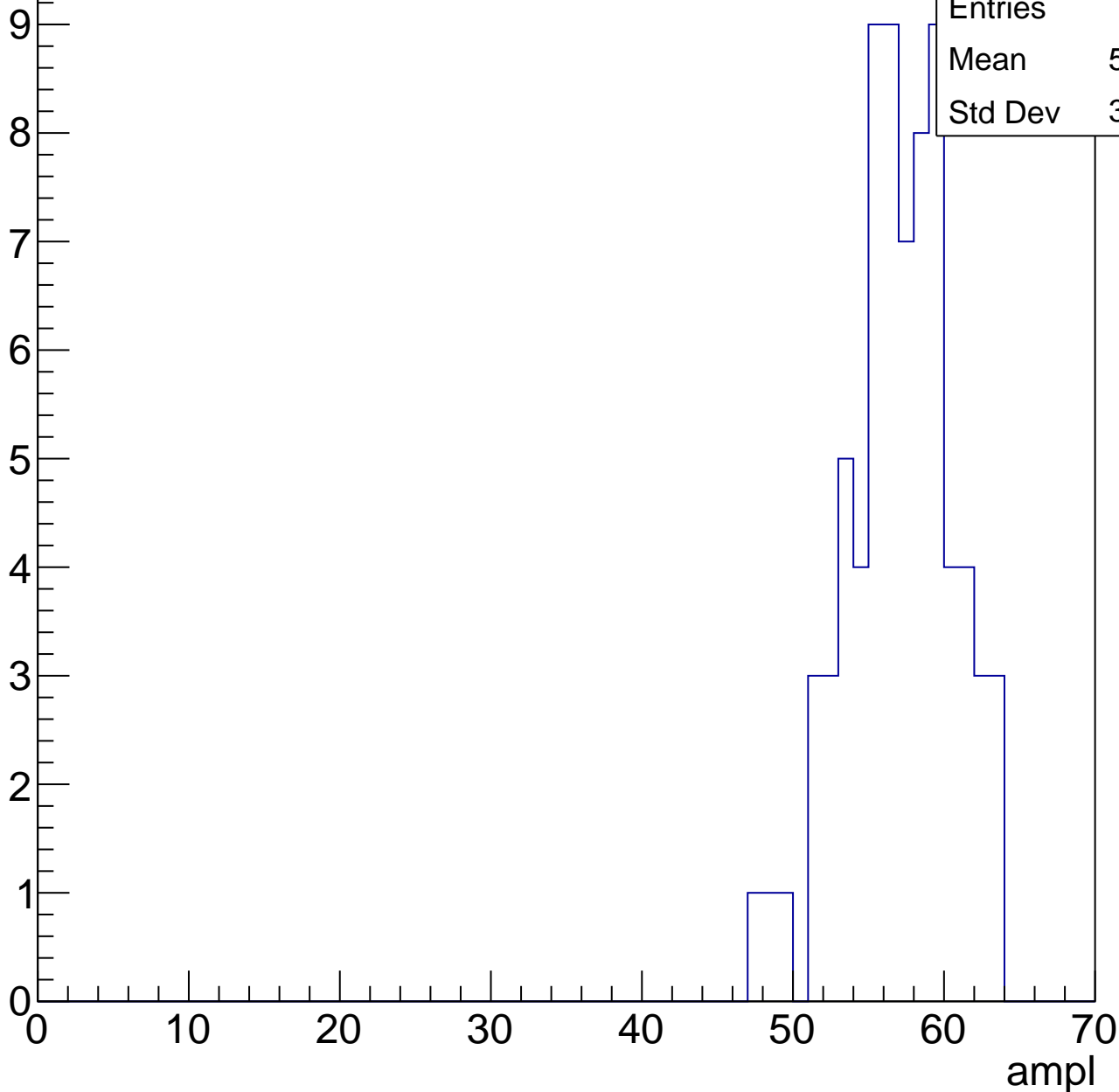


# B1L102S, U8-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	56.57
Std Dev	3.492

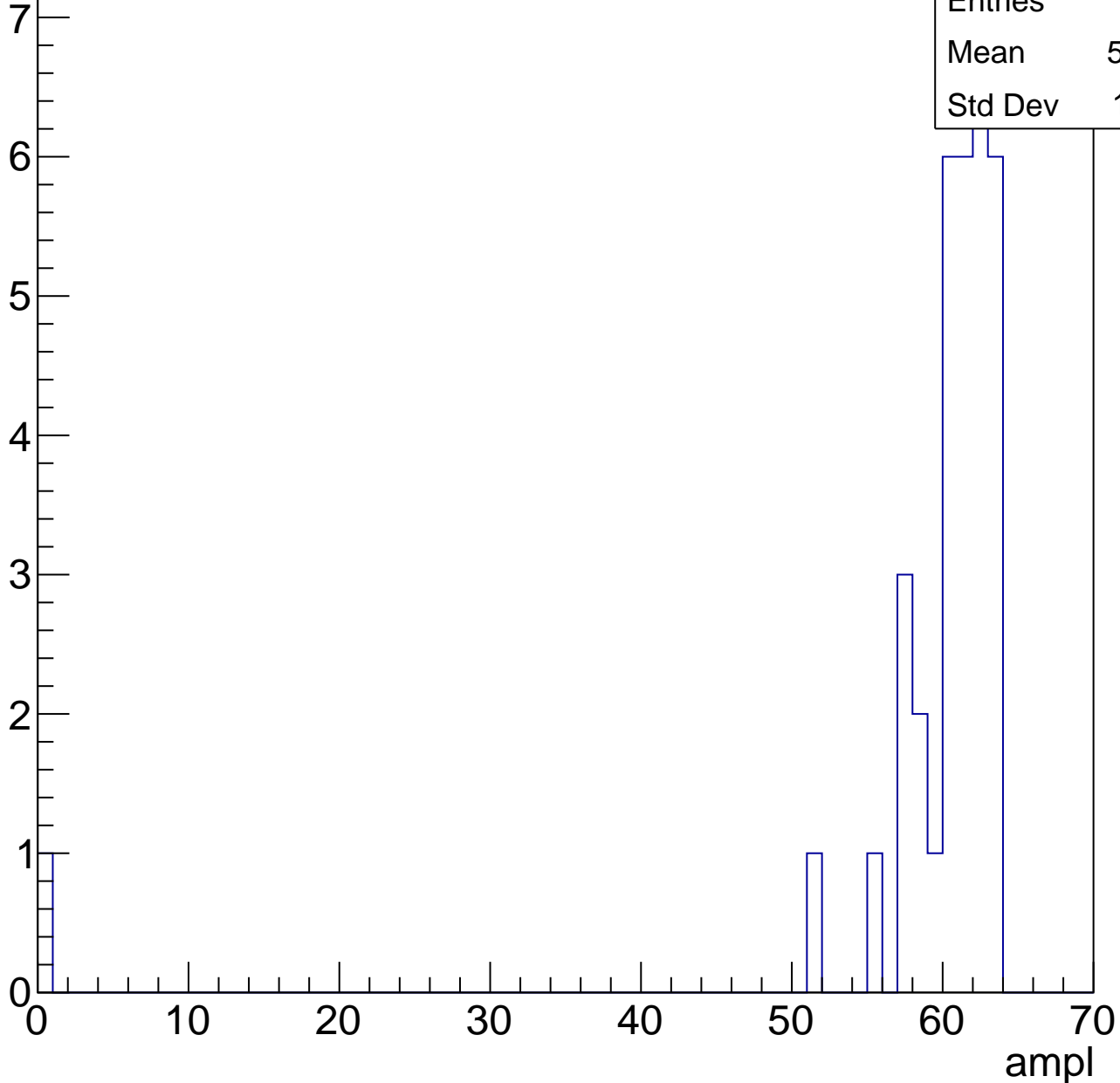


# B1L102S, U8-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	34
Mean	58.53
Std Dev	10.51



# B1L102S, U8-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U8-ch58, adc0

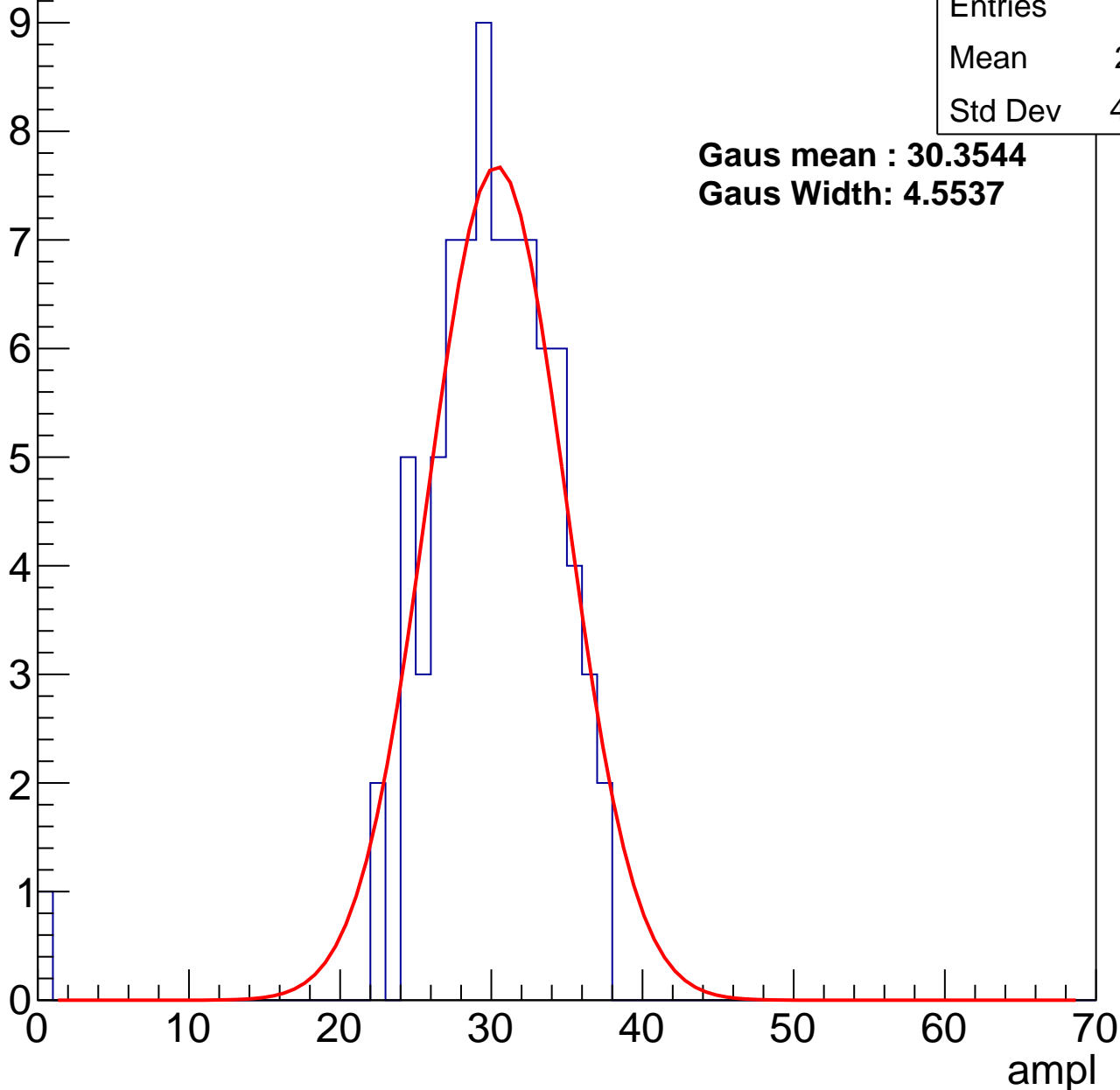
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	81
Mean	29.51
Std Dev	4.887

**Gaus mean : 30.3544**

**Gaus Width: 4.5537**



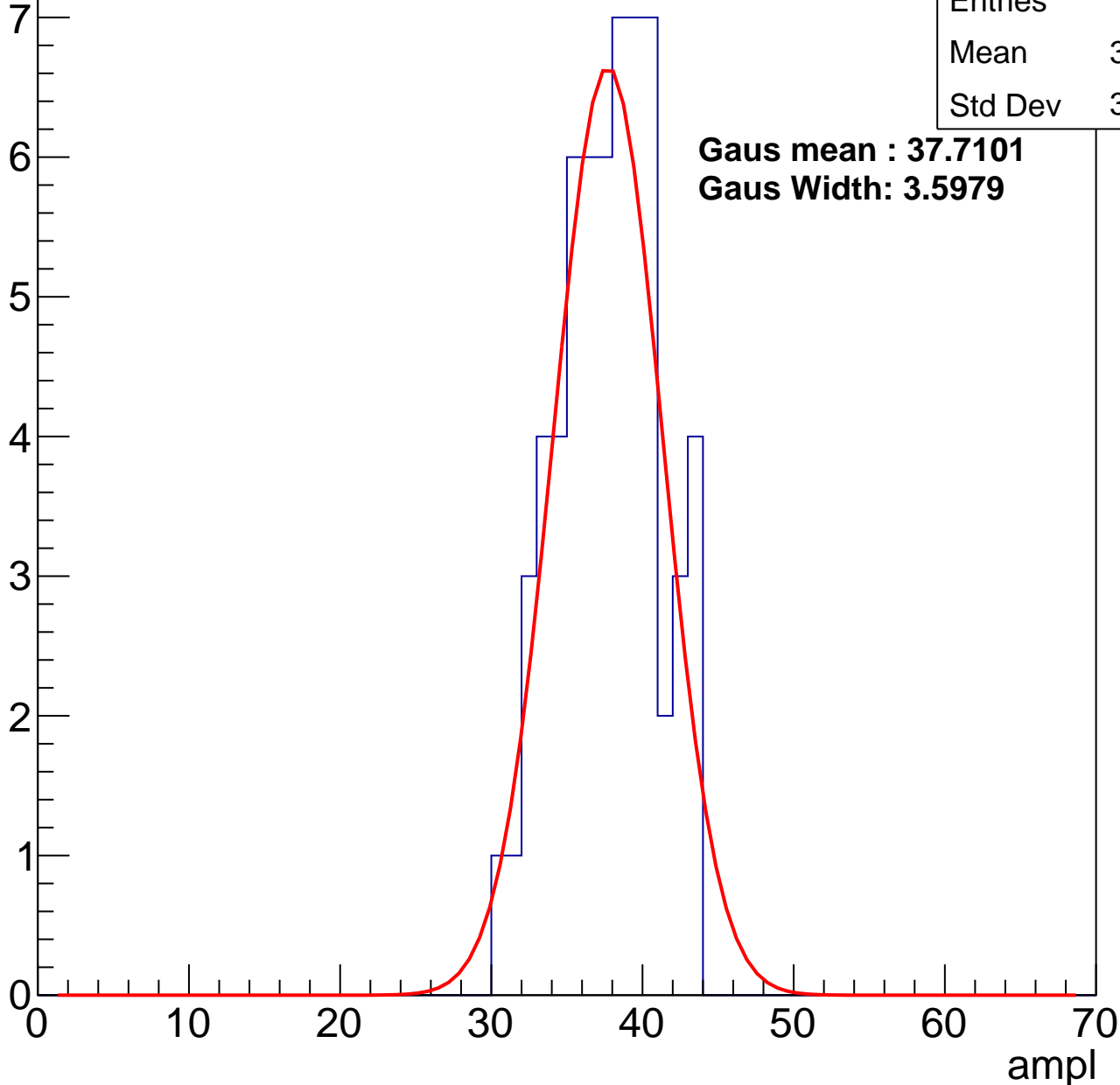
# B1L102S, U8-ch58, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	37.25
Std Dev	3.227

**Gaus mean : 37.7101**  
**Gaus Width: 3.5979**



# B1L102S, U8-ch58, adc2

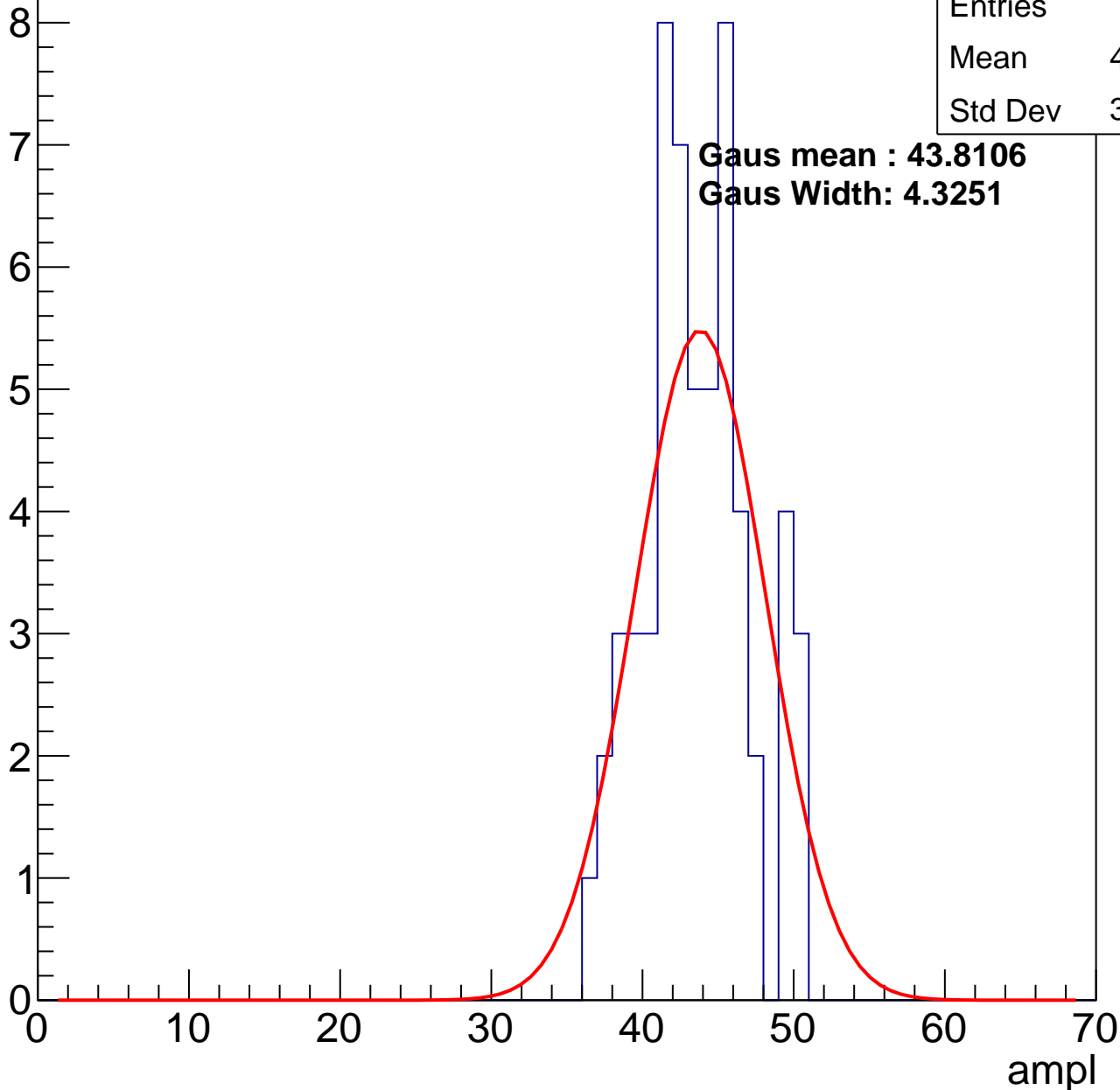
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	43.14
Std Dev	3.486

**Gaus mean : 43.8106**

**Gaus Width: 4.3251**

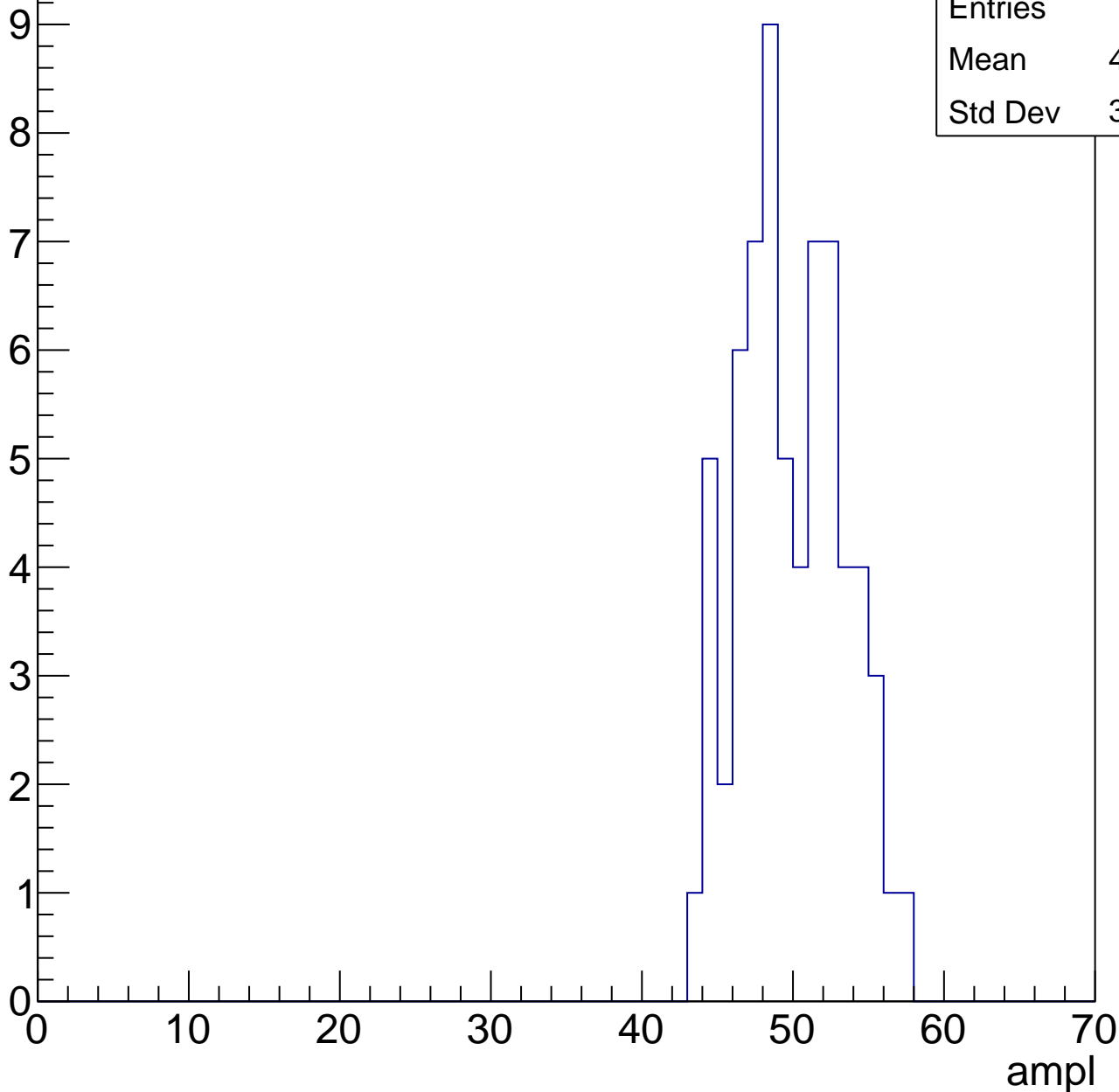


# B1L102S, U8-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

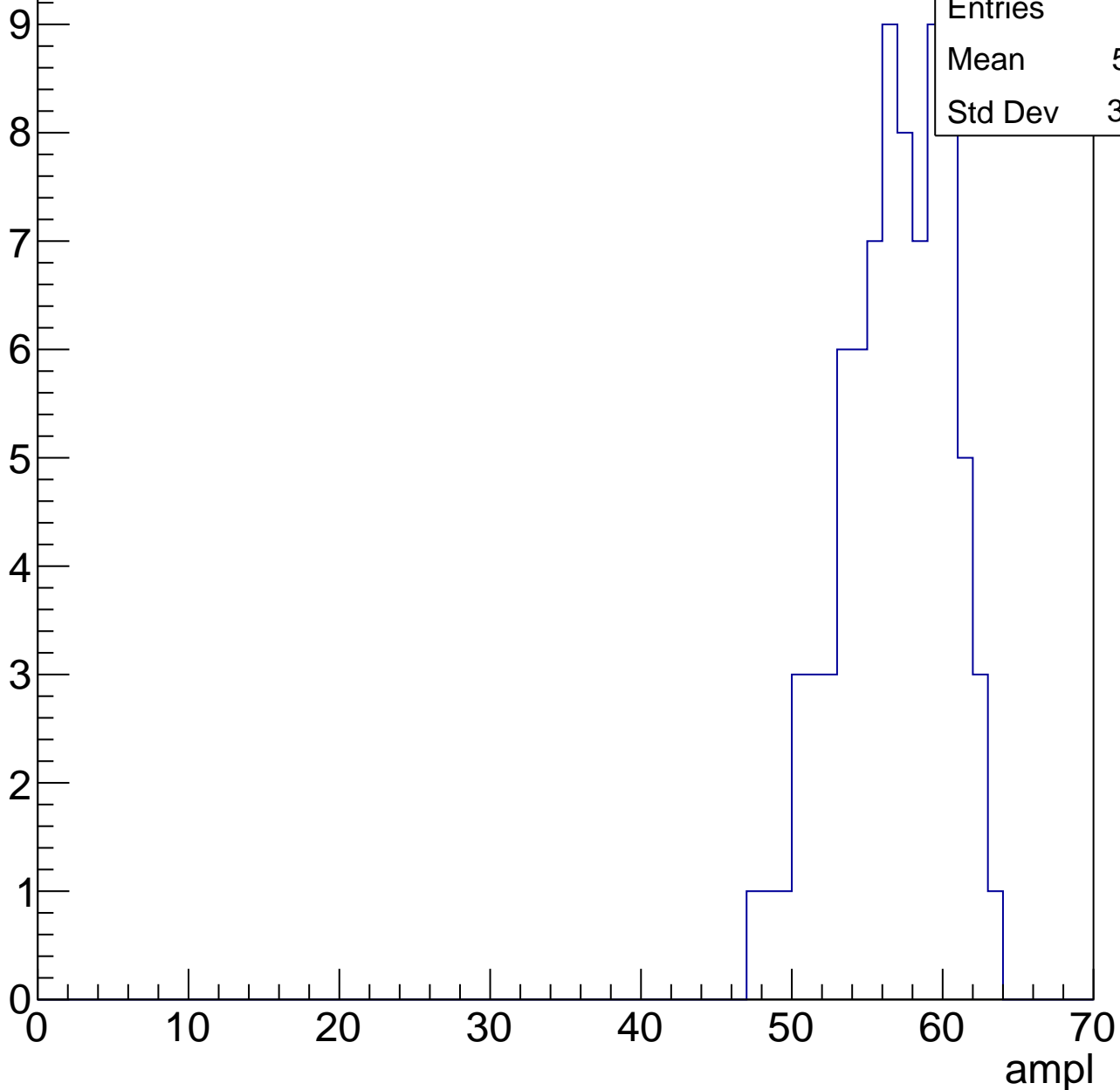
Entries	66
Mean	49.42
Std Dev	3.376



# B1L102S, U8-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



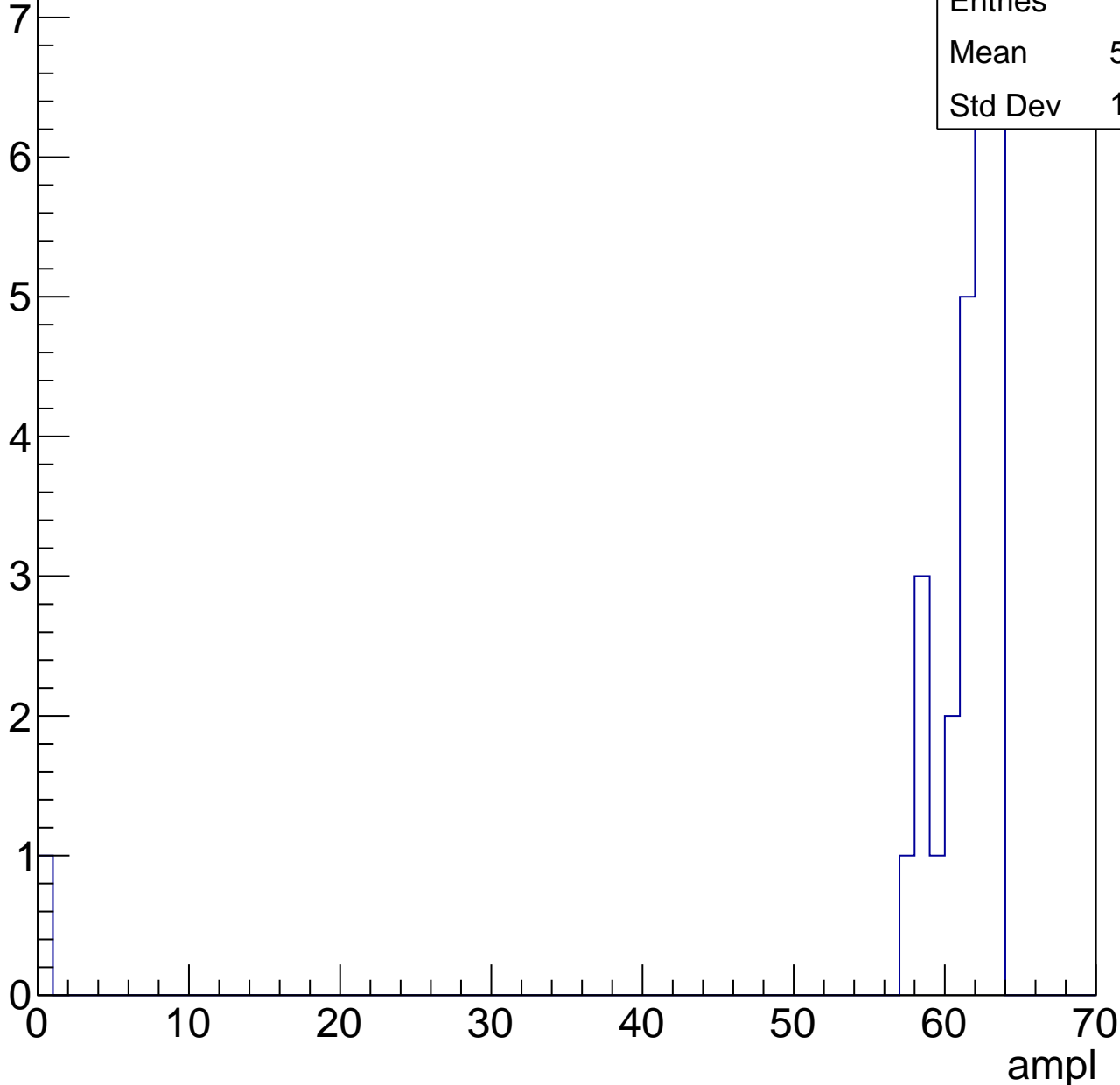
Entries	81
Mean	56.31
Std Dev	3.565

# B1L102S, U8-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	27
Mean	58.89
Std Dev	11.68



# B1L102S, U8-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

0 10 20 30 40 50 60 70

ampl



# B1L102S, U8-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch59, adc0

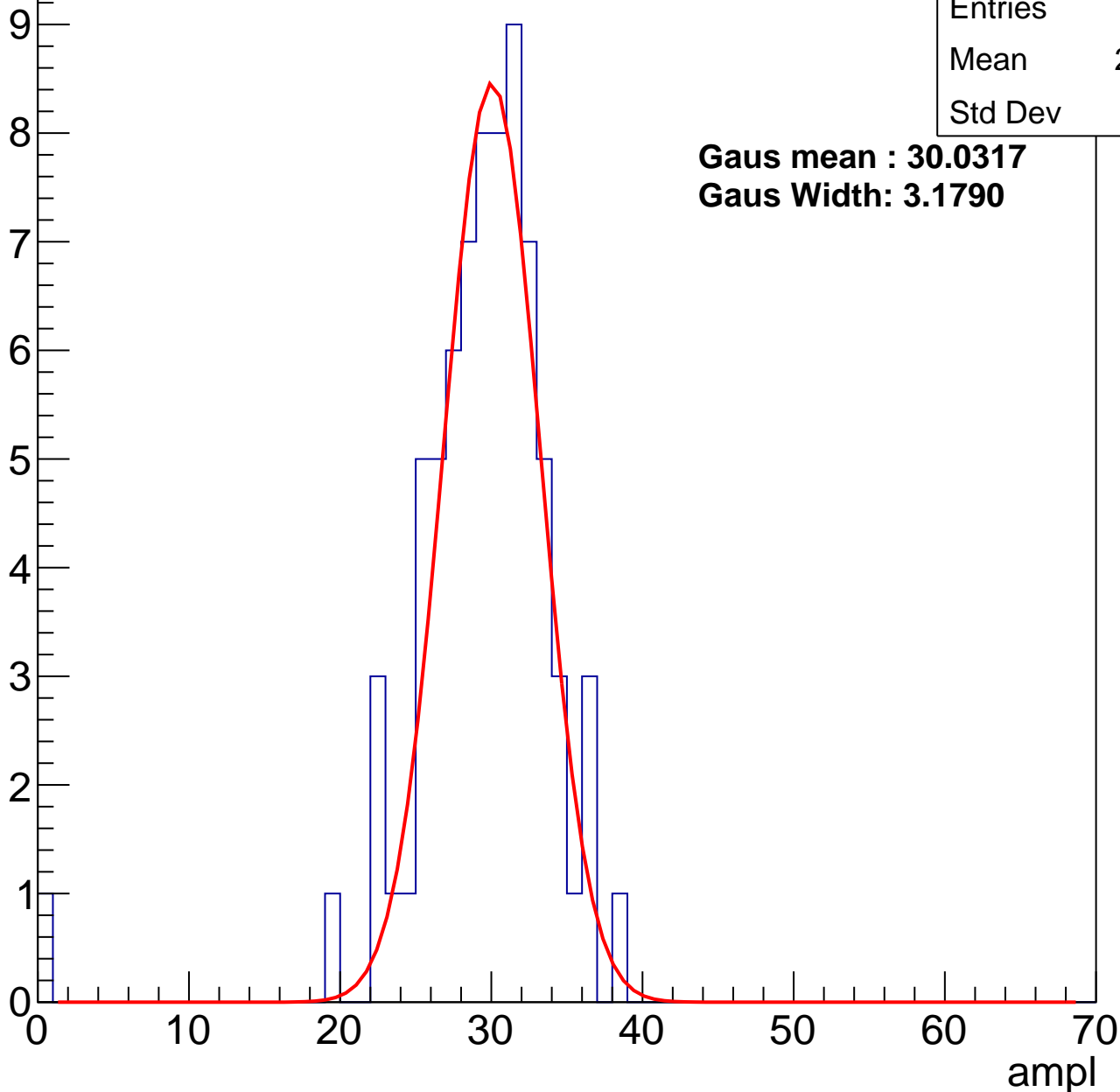
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	28.91
Std Dev	4.94

**Gaus mean : 30.0317**

**Gaus Width: 3.1790**



# B1L102S, U8-ch59, adc1

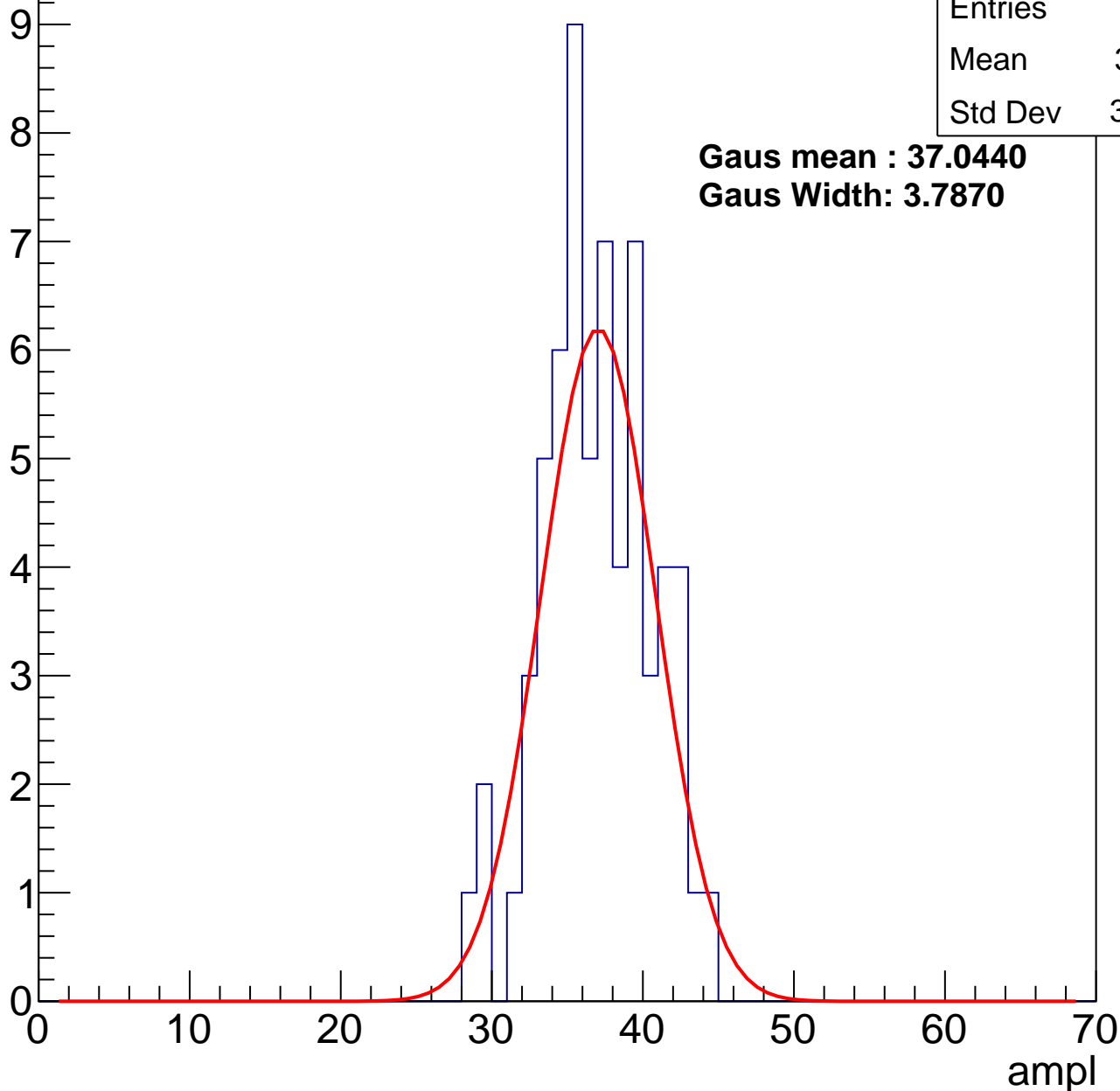
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	36.51
Std Dev	3.536

**Gaus mean : 37.0440**

**Gaus Width: 3.7870**



# B1L102S, U8-ch59, adc2

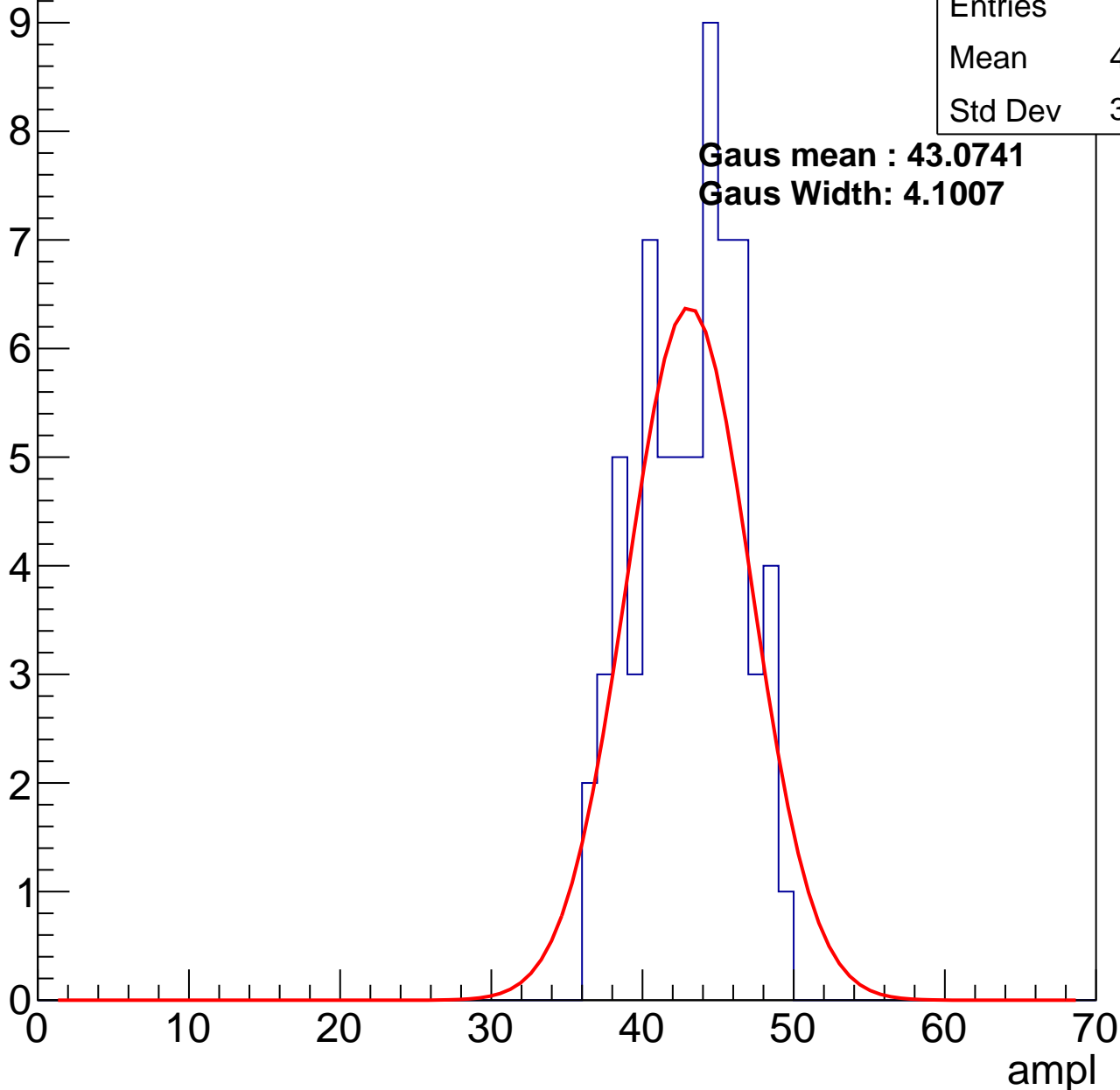
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	42.65
Std Dev	3.355

**Gaus mean : 43.0741**

**Gaus Width: 4.1007**

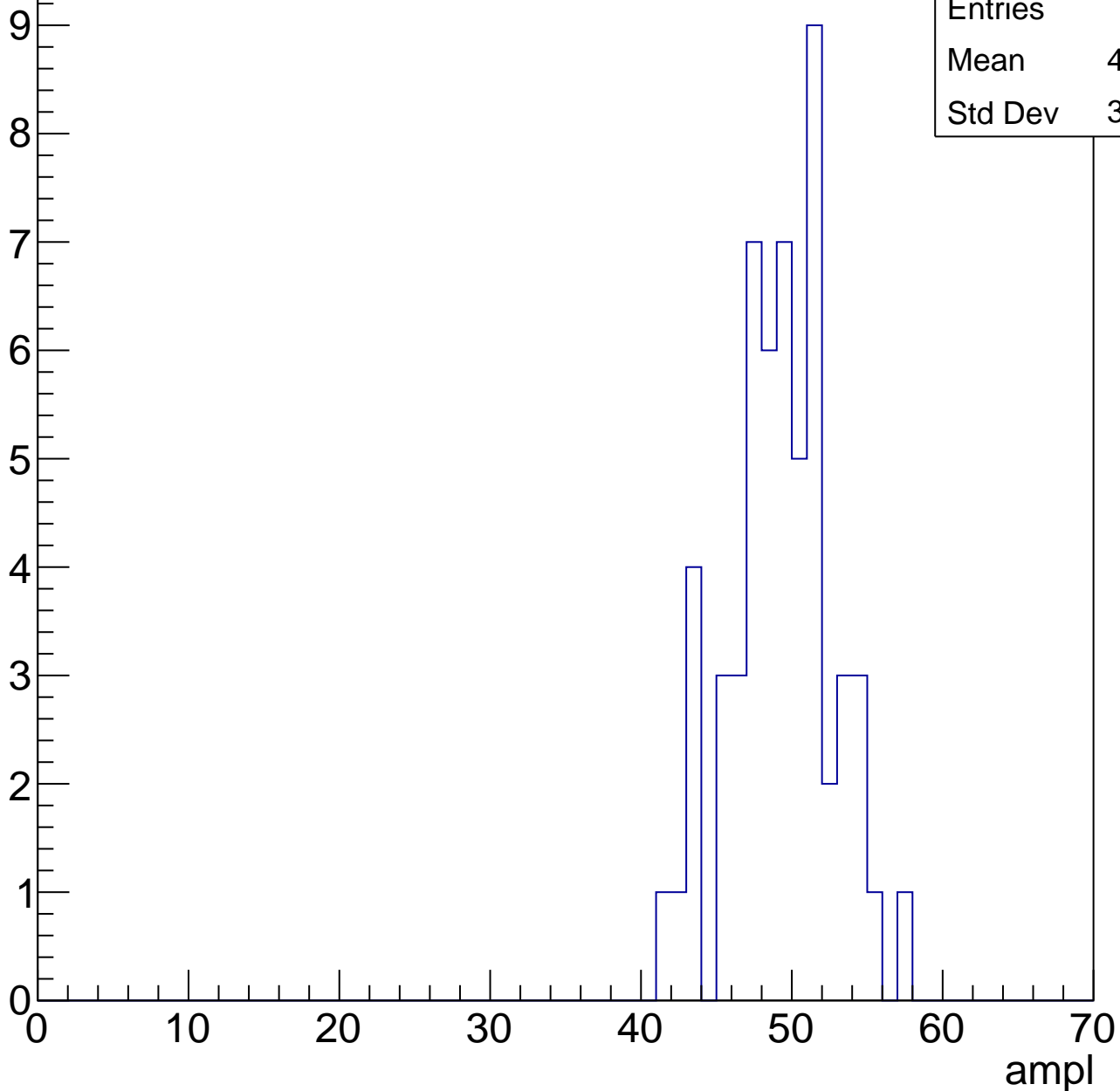


# B1L102S, U8-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

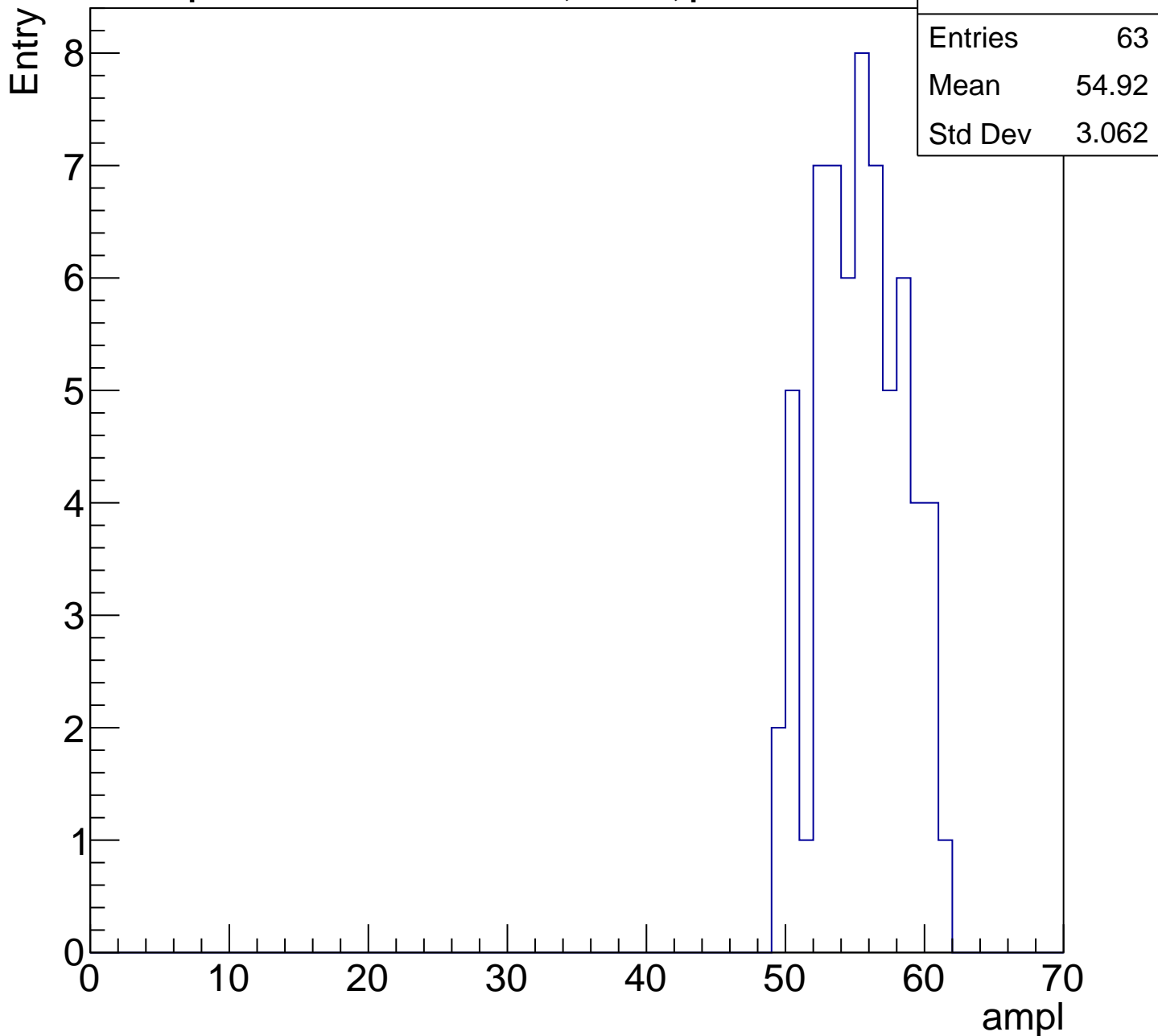
Entry

Entries	56
Mean	48.82
Std Dev	3.397



# B1L102S, U8-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

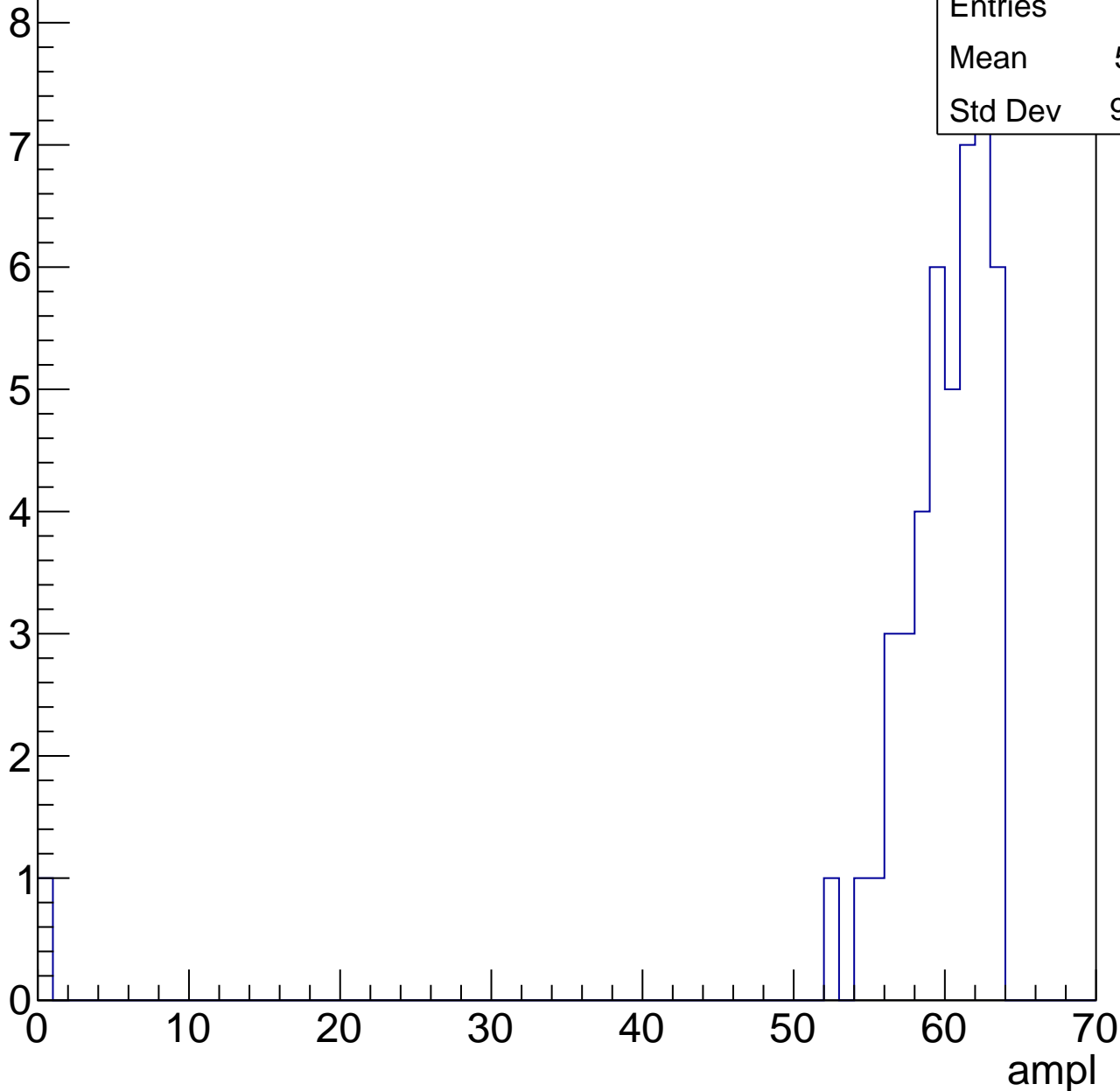


# B1L102S, U8-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

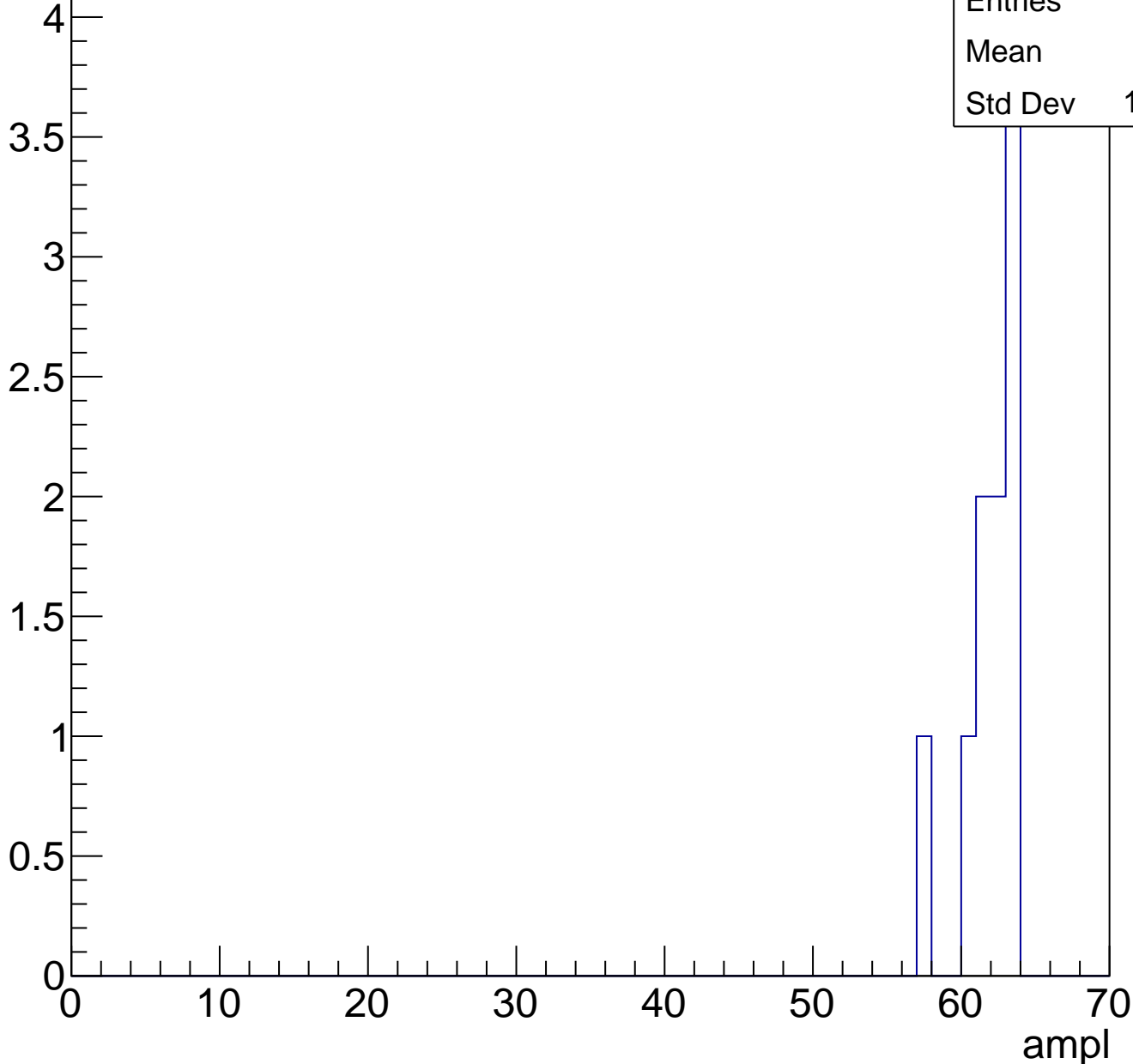
Entries	46
Mean	58.41
Std Dev	9.088



# B1L102S, U8-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U8-ch60, adc0

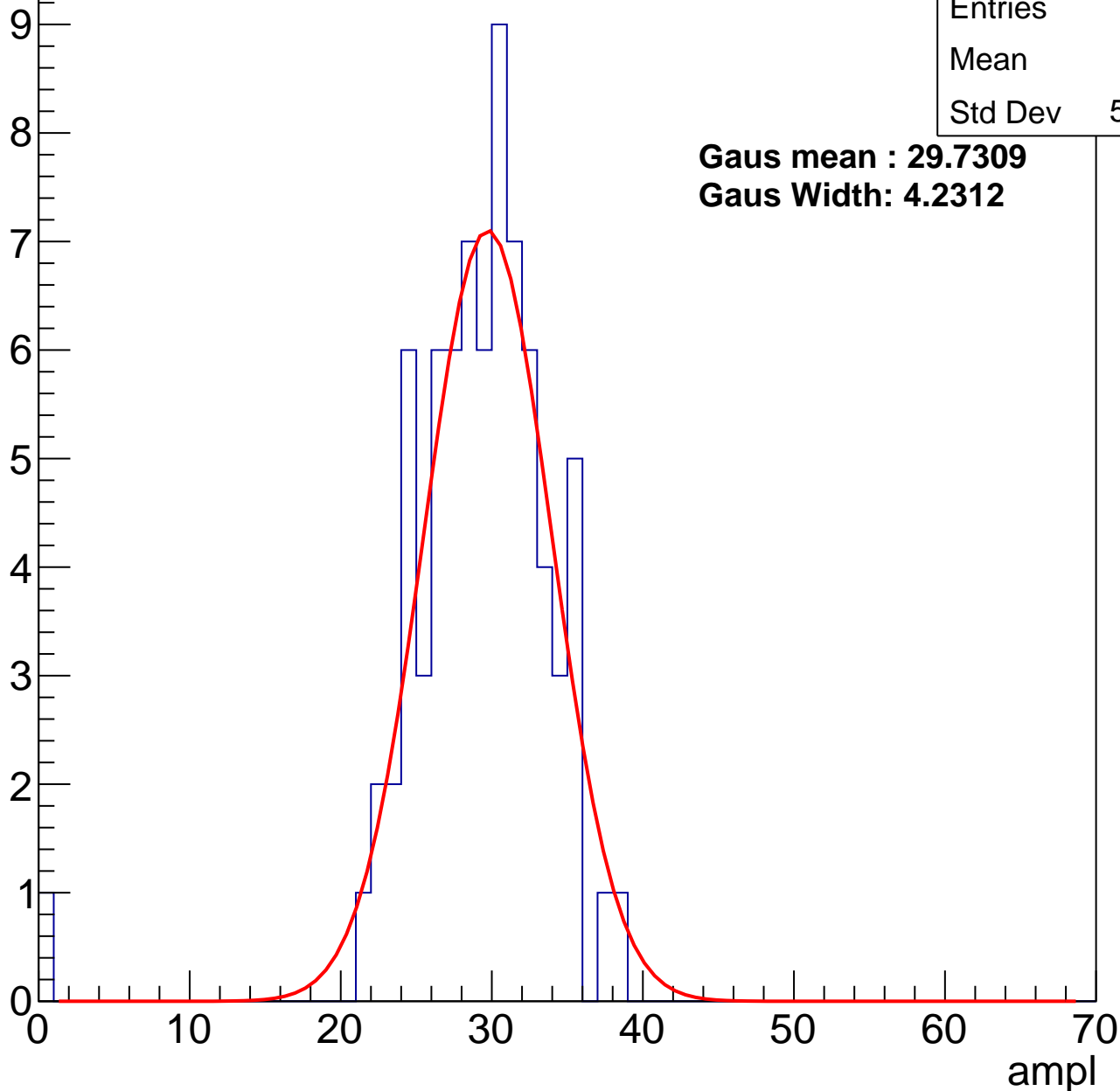
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	28.7
Std Dev	5.008

**Gaus mean : 29.7309**

**Gaus Width: 4.2312**



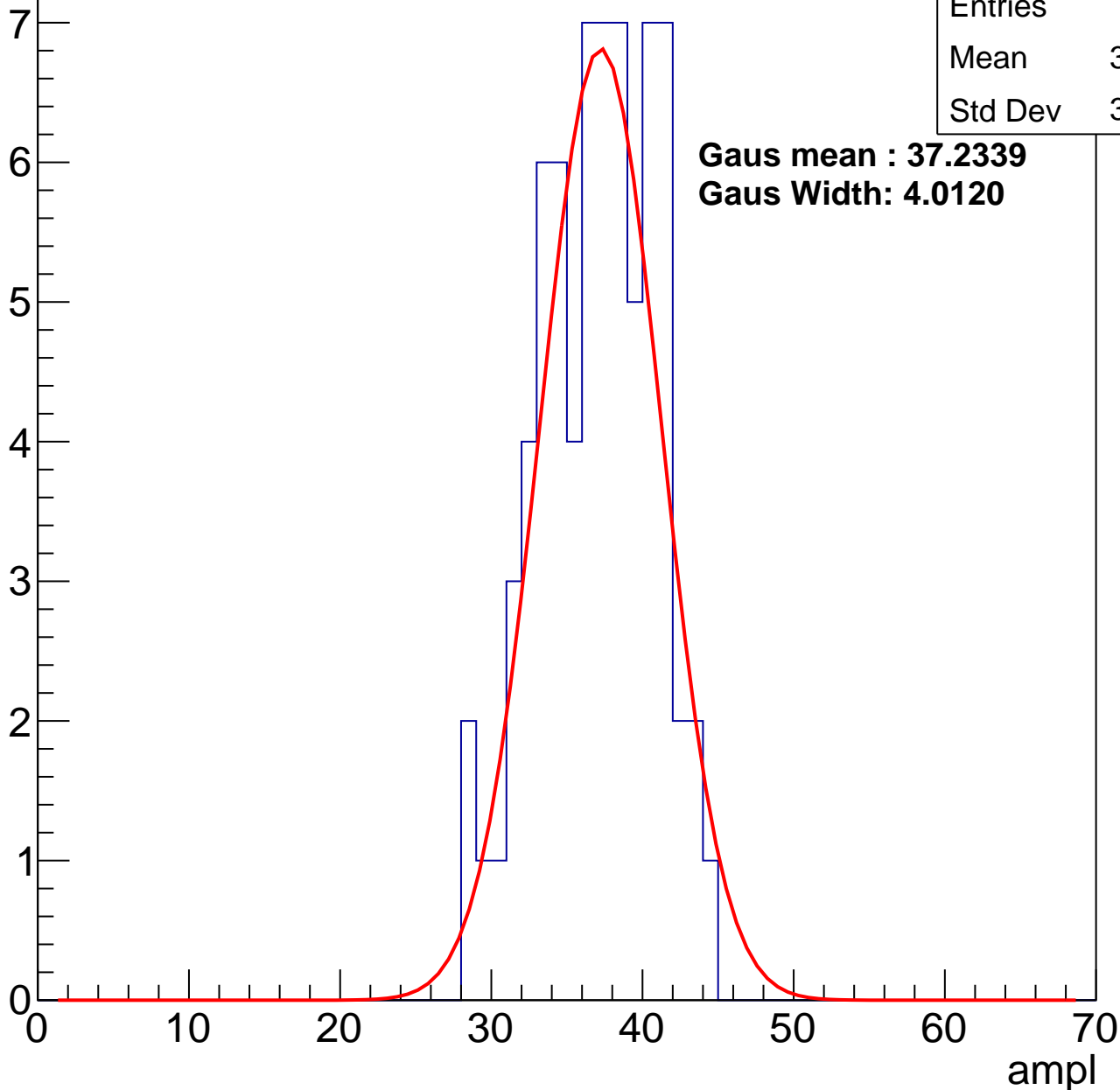
# B1L102S, U8-ch60, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	36.54
Std Dev	3.753

**Gaus mean : 37.2339**  
**Gaus Width: 4.0120**



# B1L102S, U8-ch60, adc2

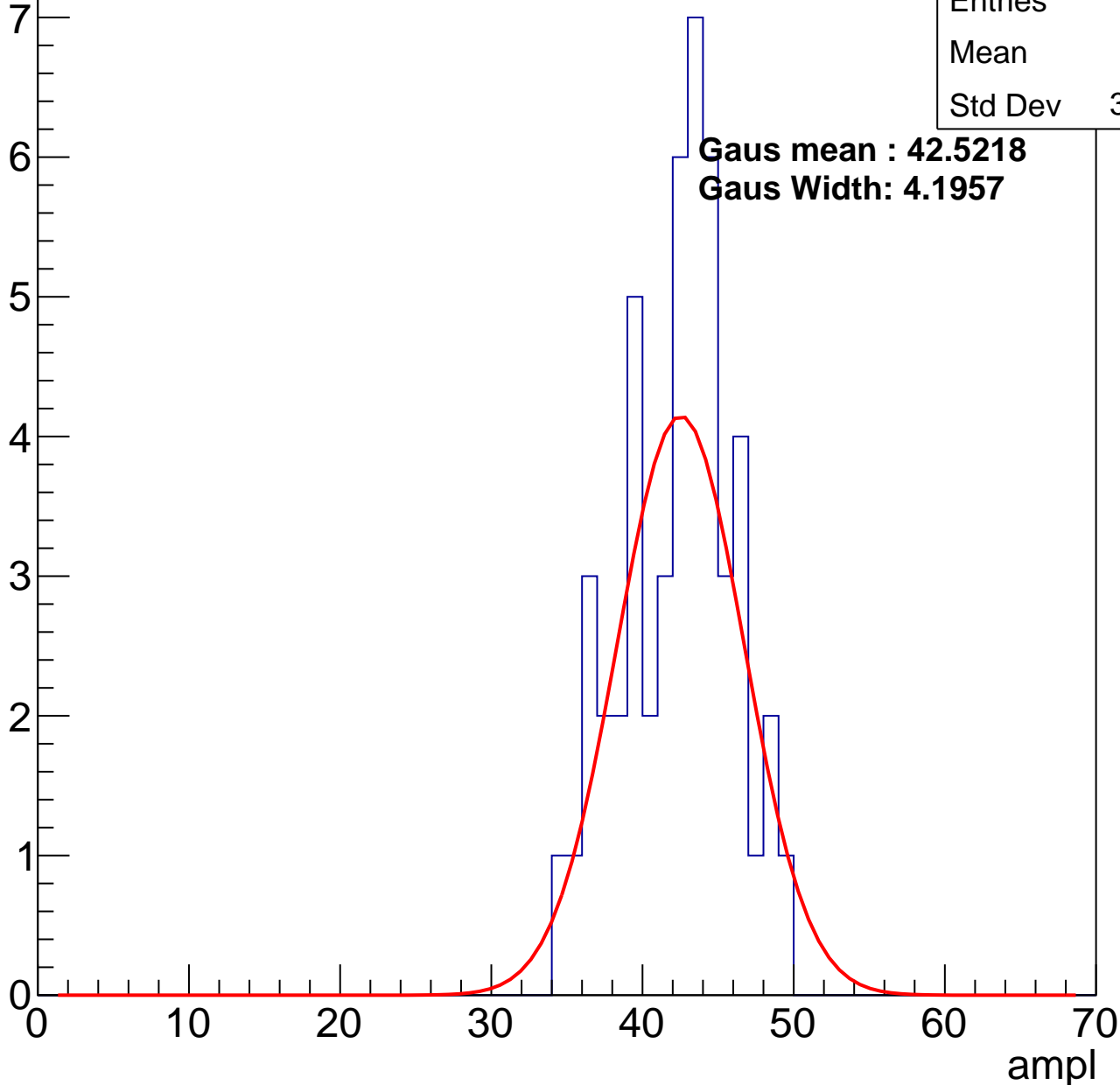
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	41.9
Std Dev	3.576

**Gaus mean : 42.5218**

**Gaus Width: 4.1957**

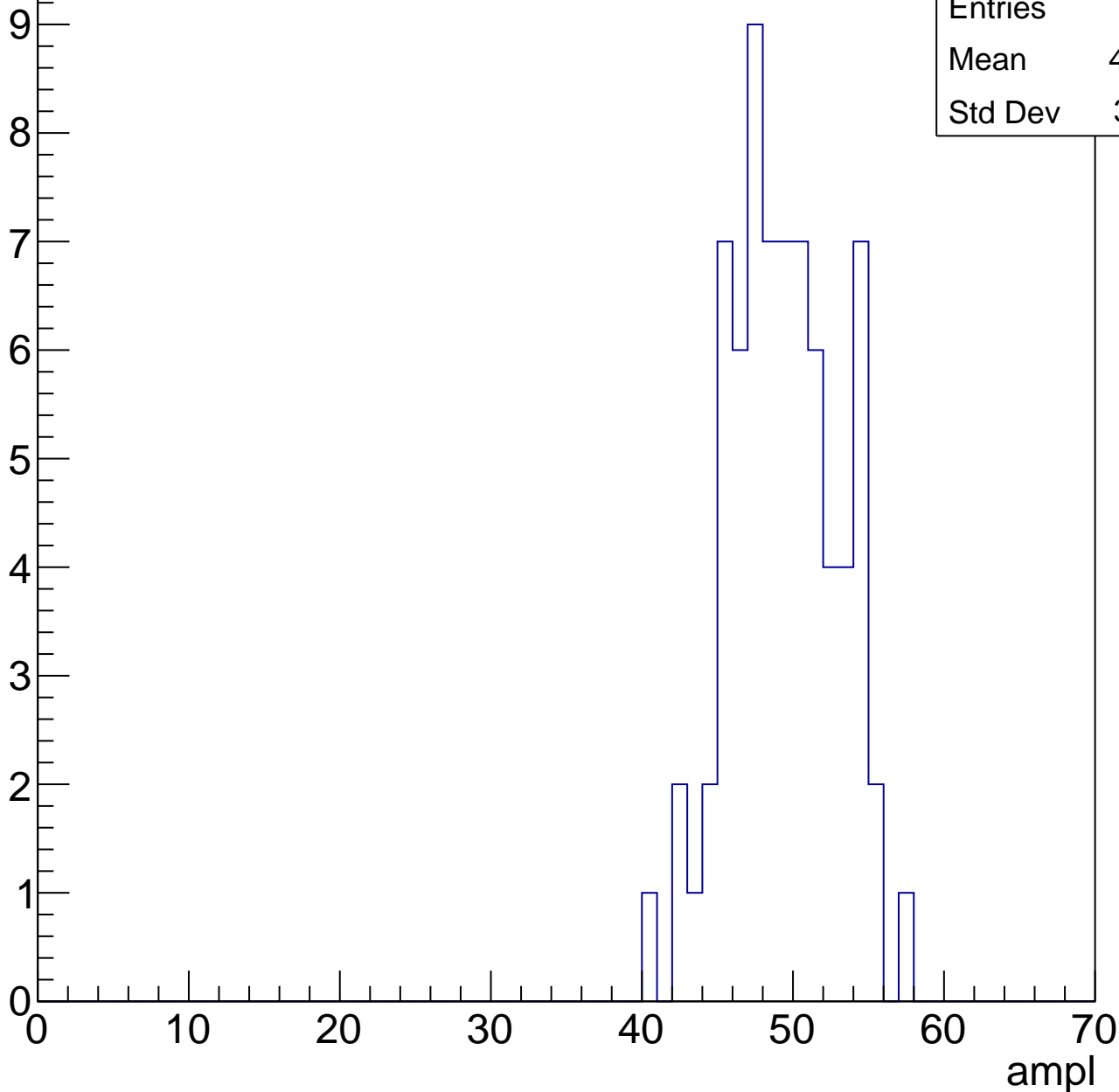


# B1L102S, U8-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	48.89
Std Dev	3.541

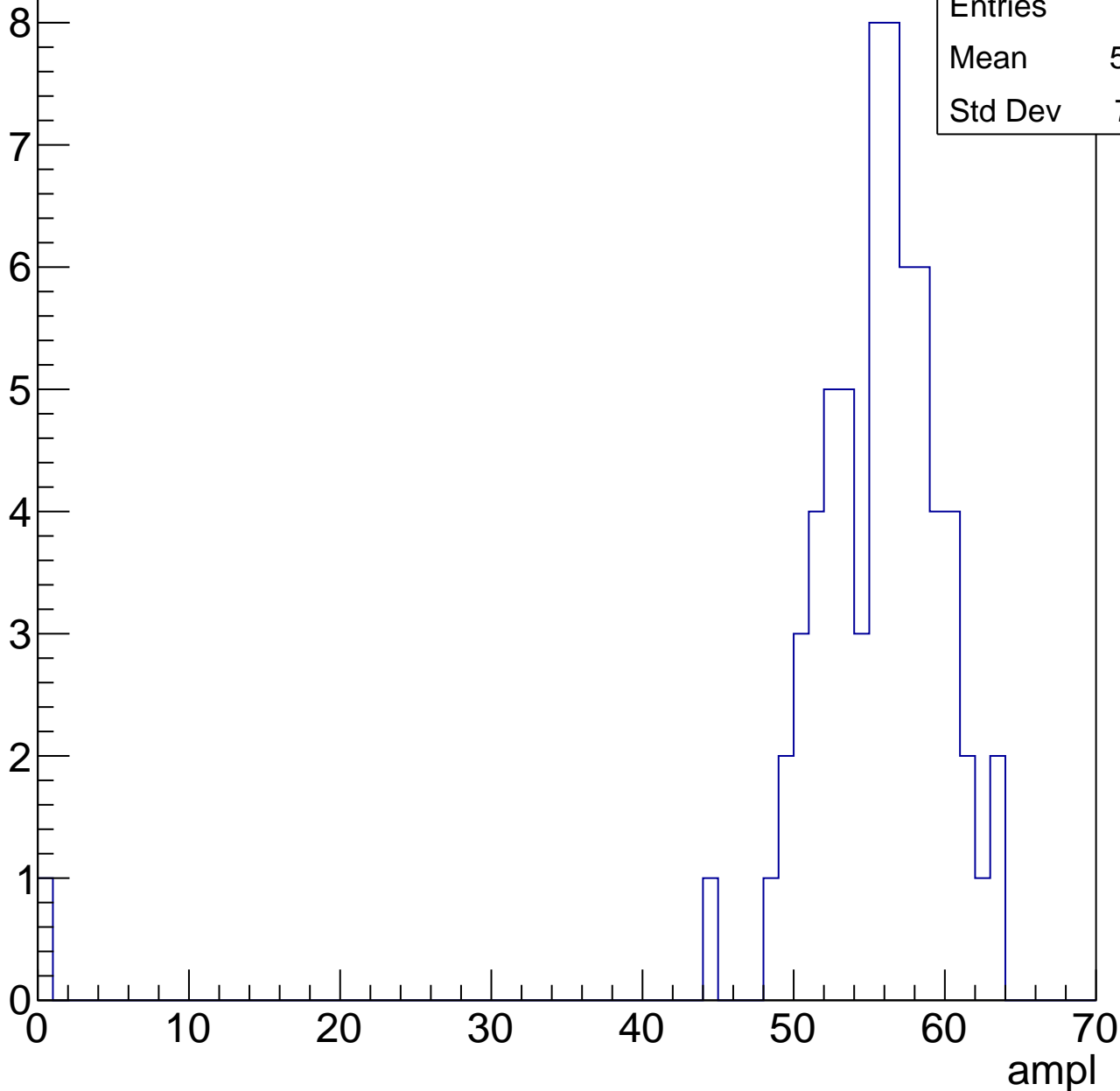


# B1L102S, U8-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	54.47
Std Dev	7.741

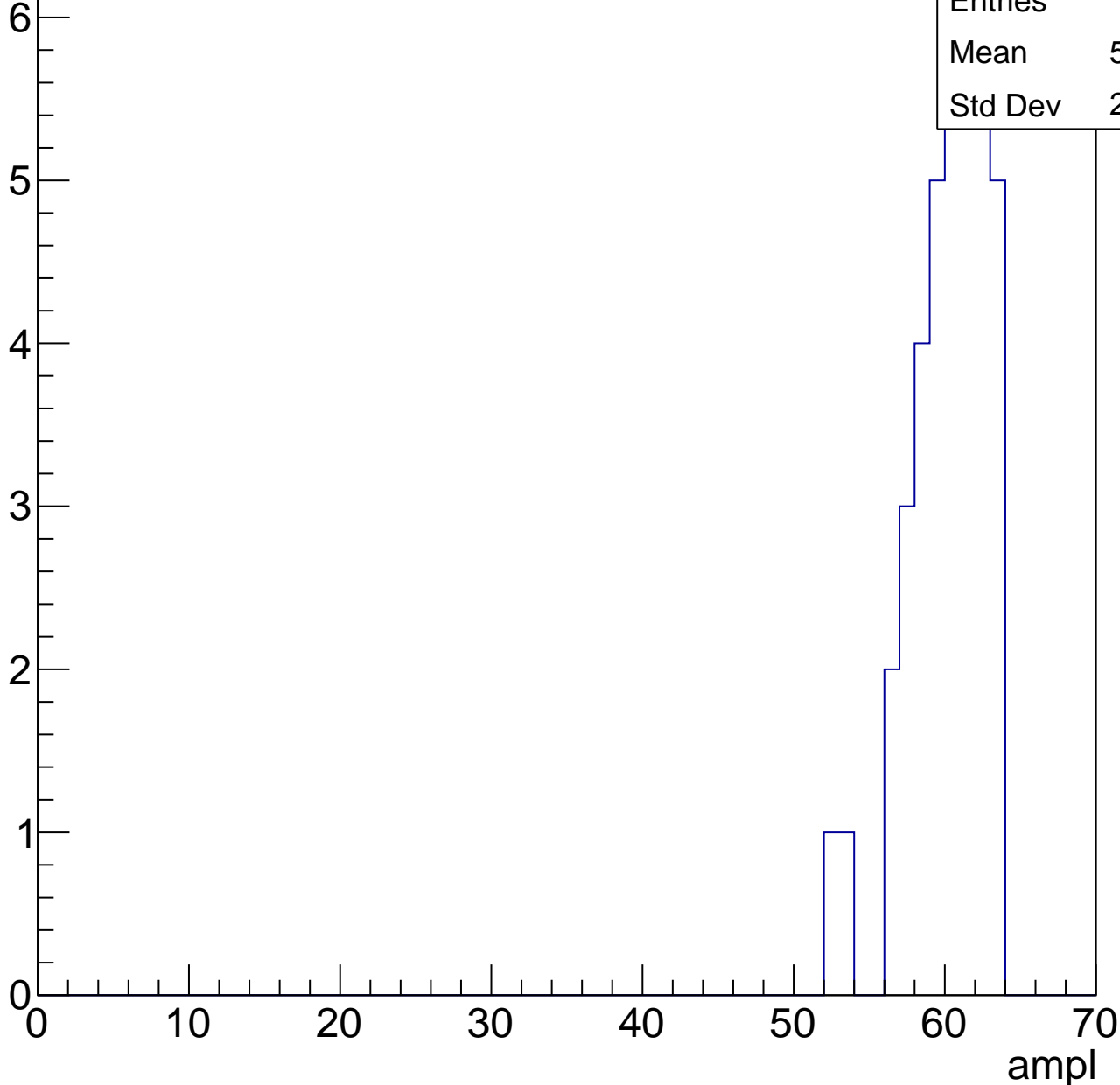


# B1L102S, U8-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

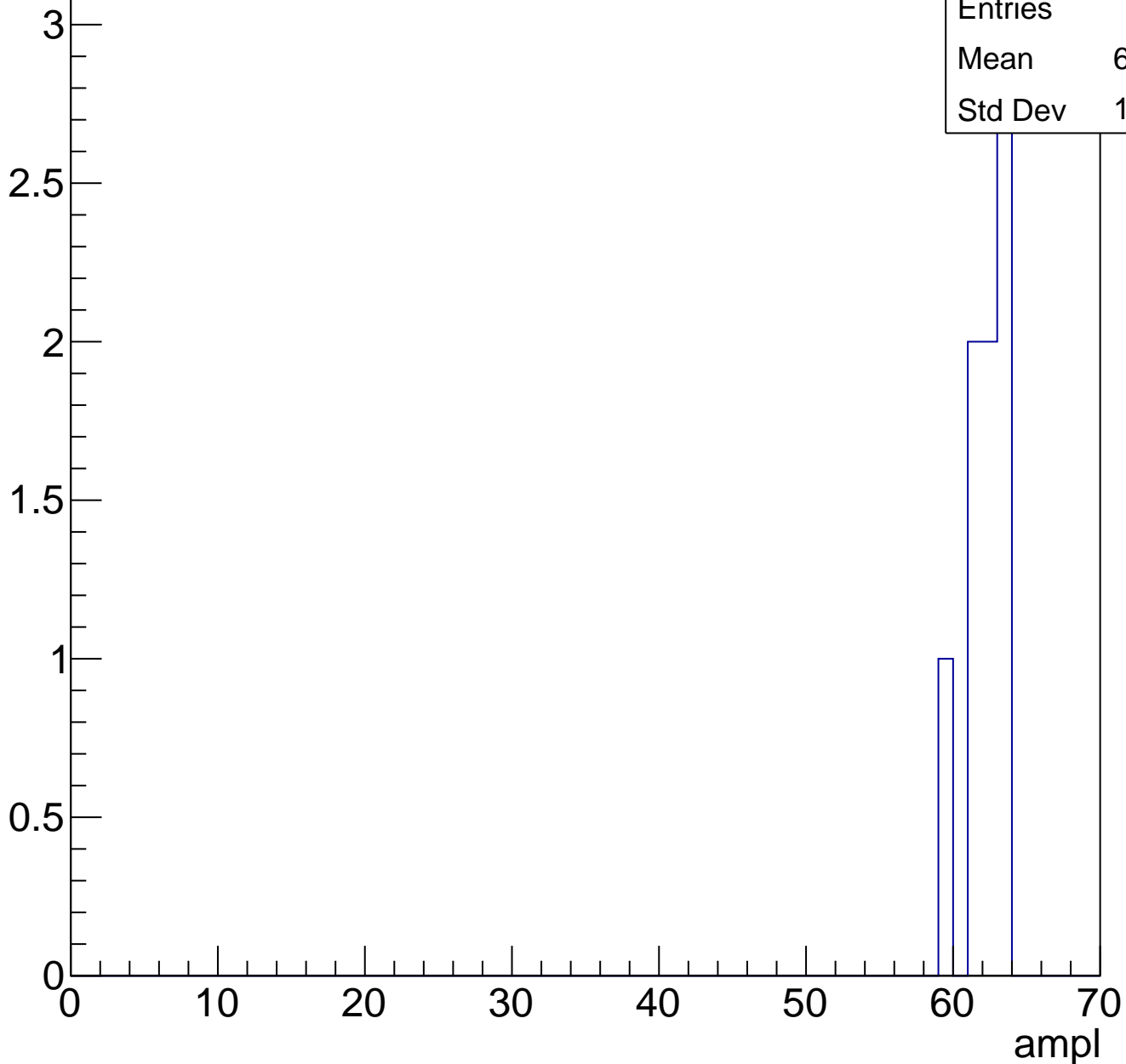
Entries	39
Mean	59.69
Std Dev	2.603



# B1L102S, U8-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

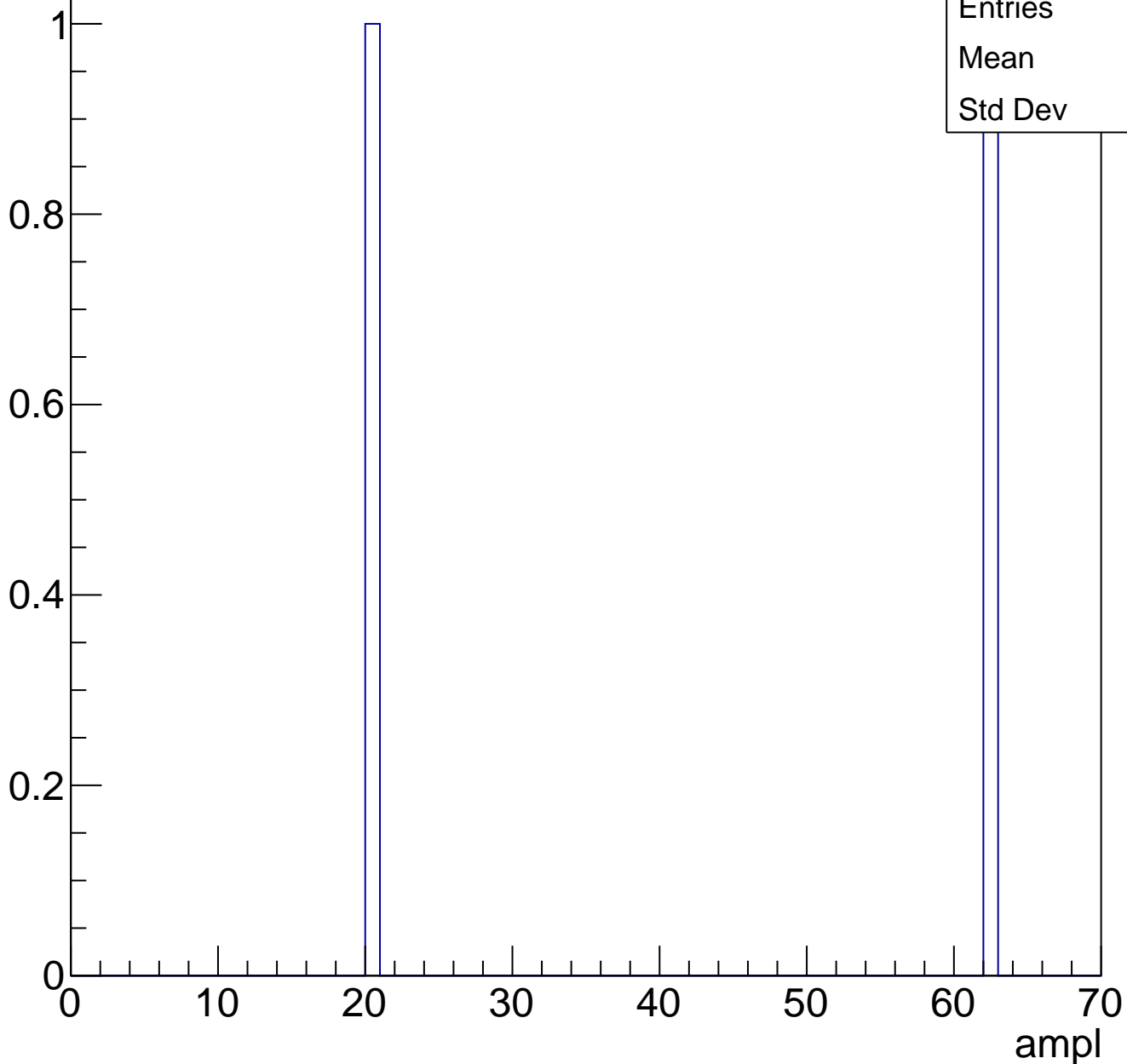




# B1L102S, U8-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	41
Std Dev	21

# B1L102S, U8-ch61, adc0

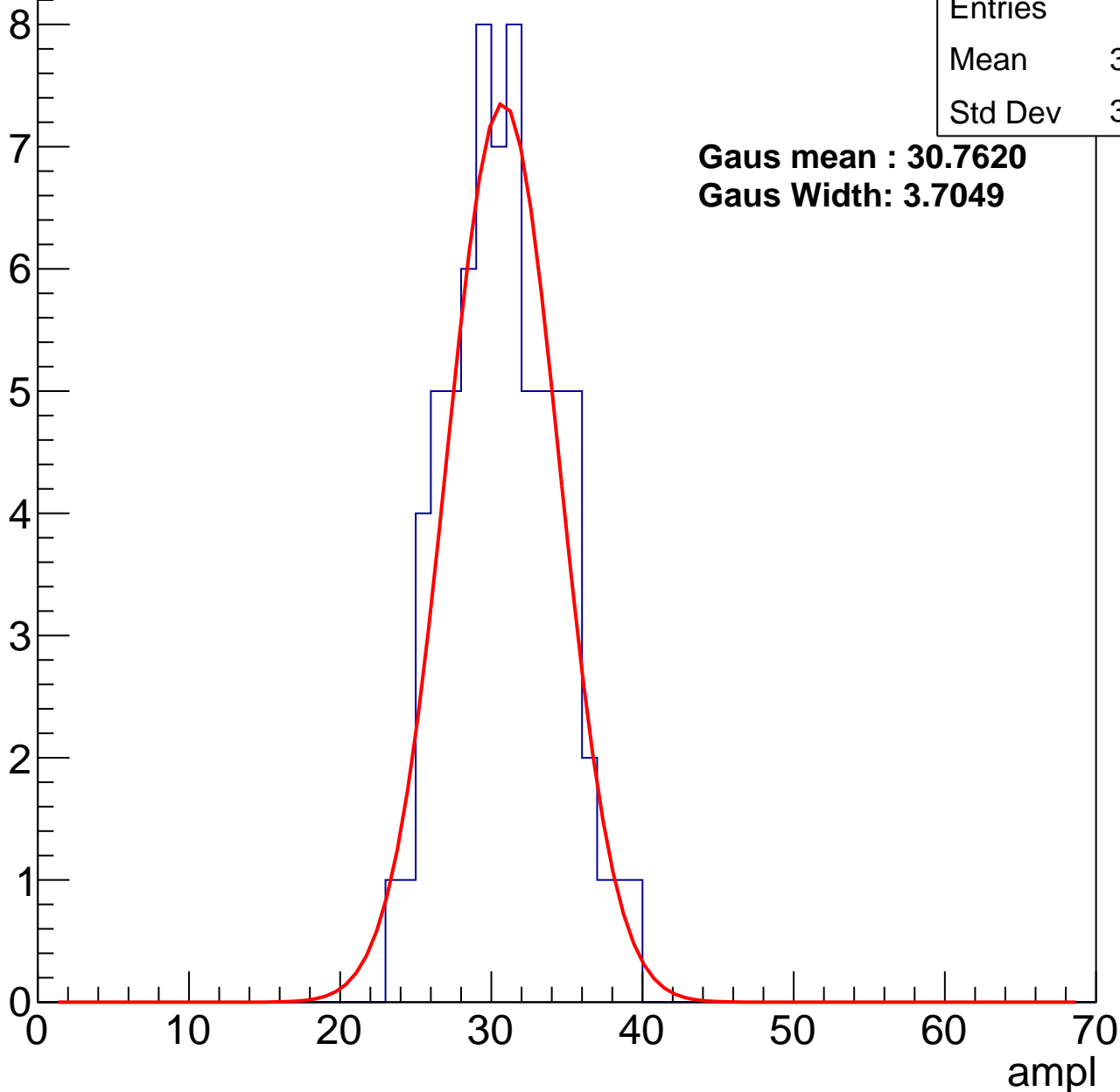
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	30.37
Std Dev	3.538

**Gaus mean : 30.7620**

**Gaus Width: 3.7049**



# B1L102S, U8-ch61, adc1

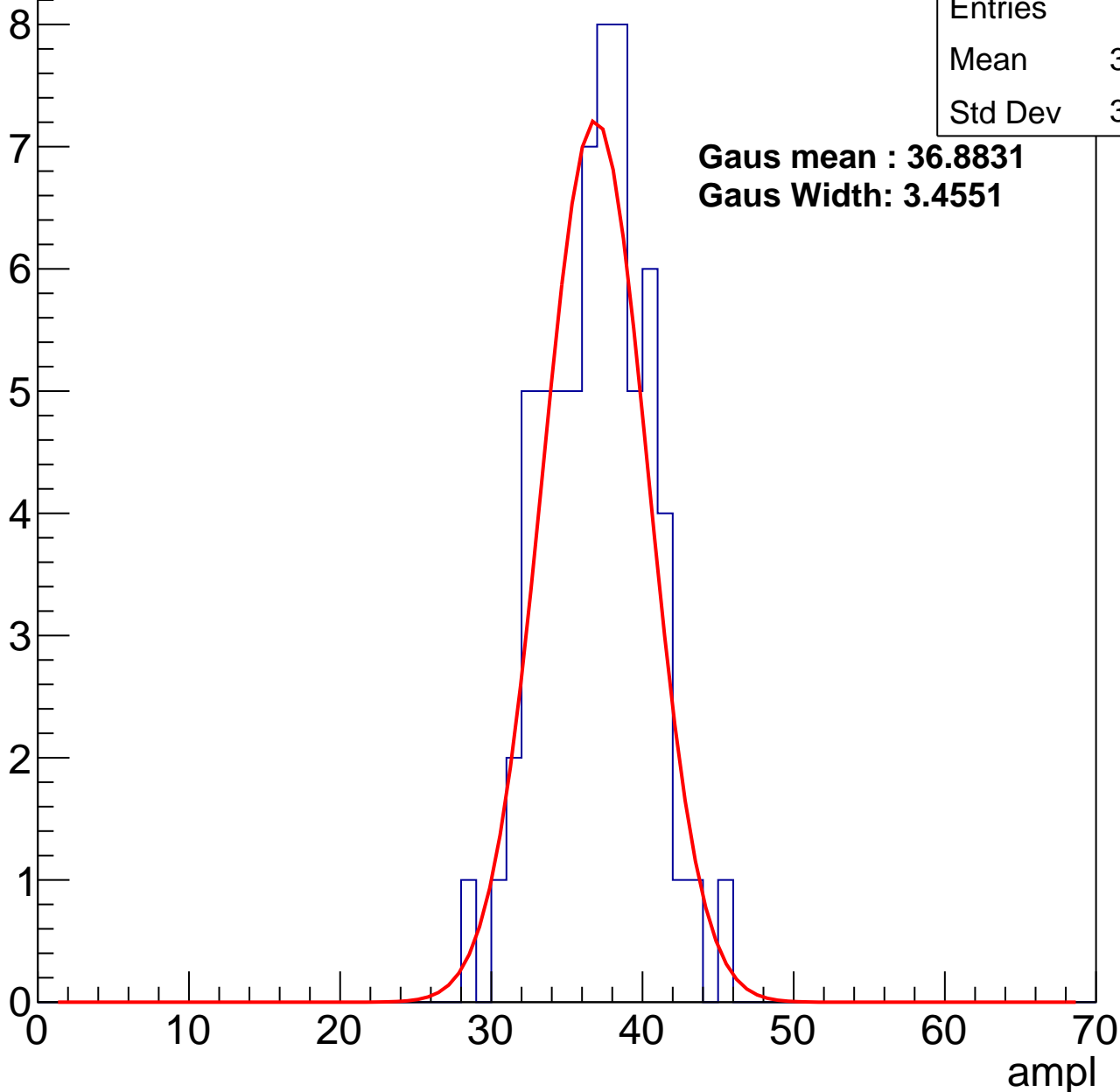
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	36.48
Std Dev	3.356

**Gaus mean : 36.8831**

**Gaus Width: 3.4551**



# B1L102S, U8-ch61, adc2

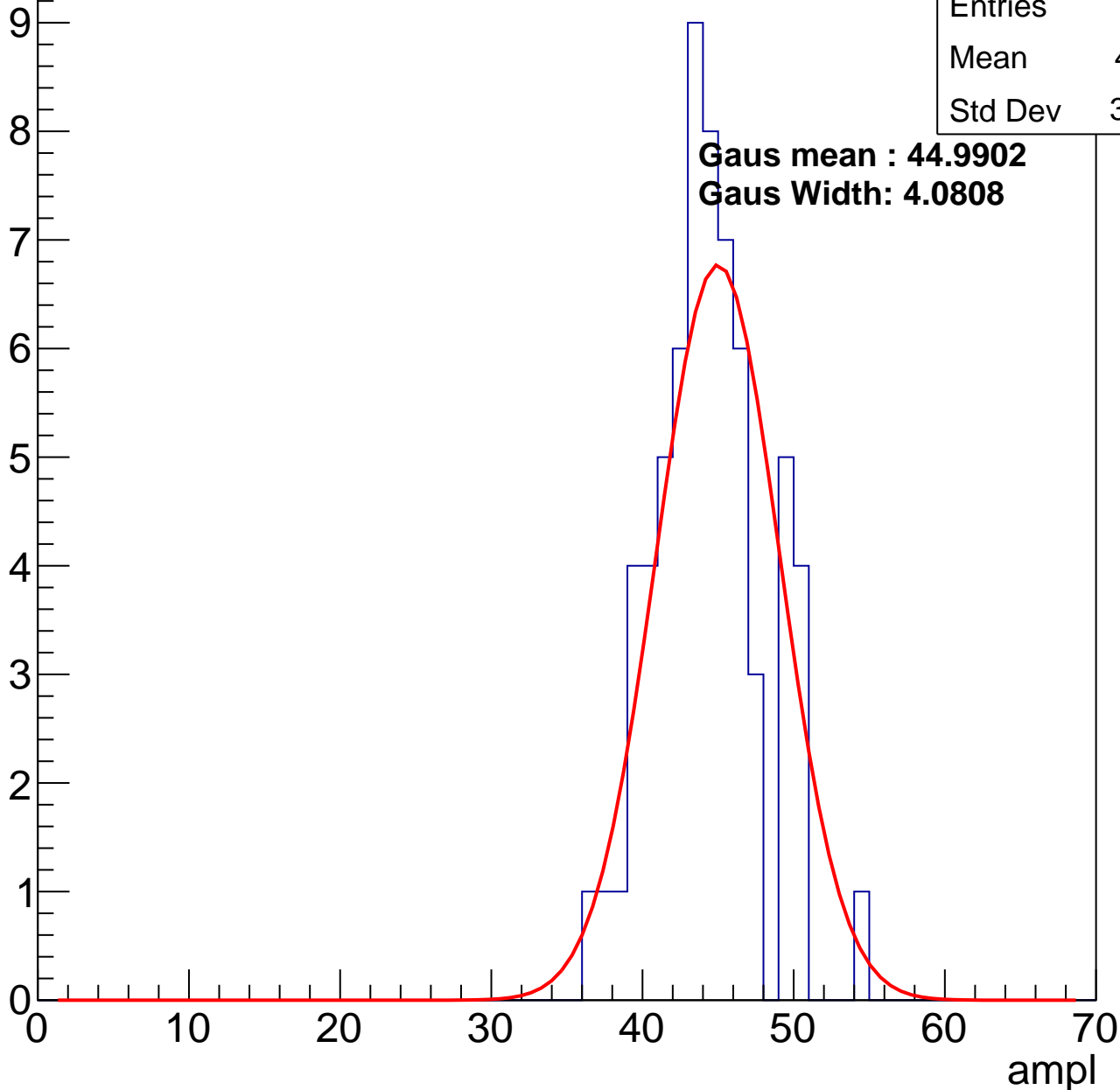
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	43.91
Std Dev	3.546

**Gaus mean : 44.9902**

**Gaus Width: 4.0808**



# B1L102S, U8-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	77
Mean	50.1
Std Dev	3.843

Entry

10

8

6

4

2

0

0

10

20

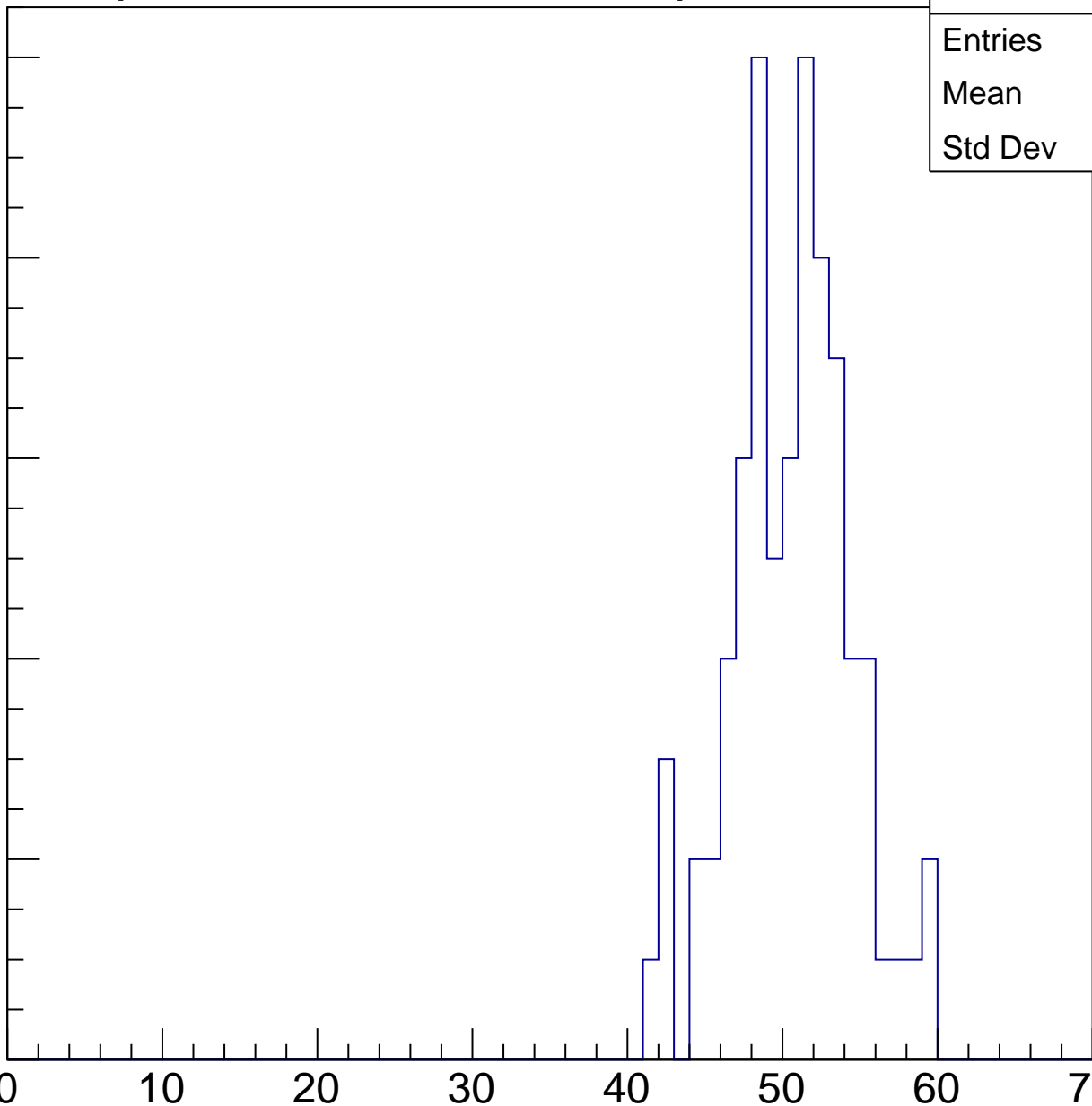
30

40

50

60

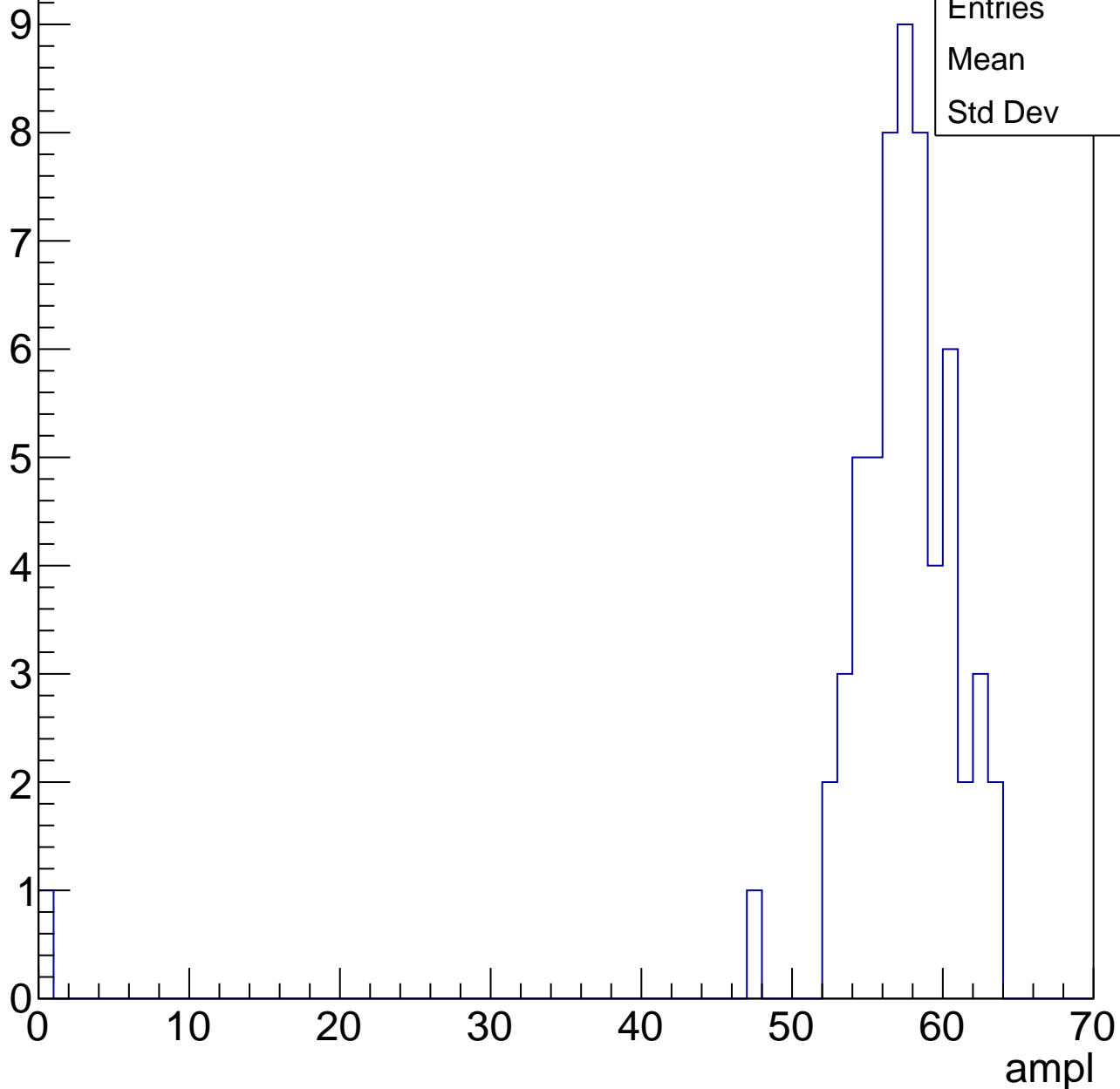
ampl



# B1L102S, U8-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

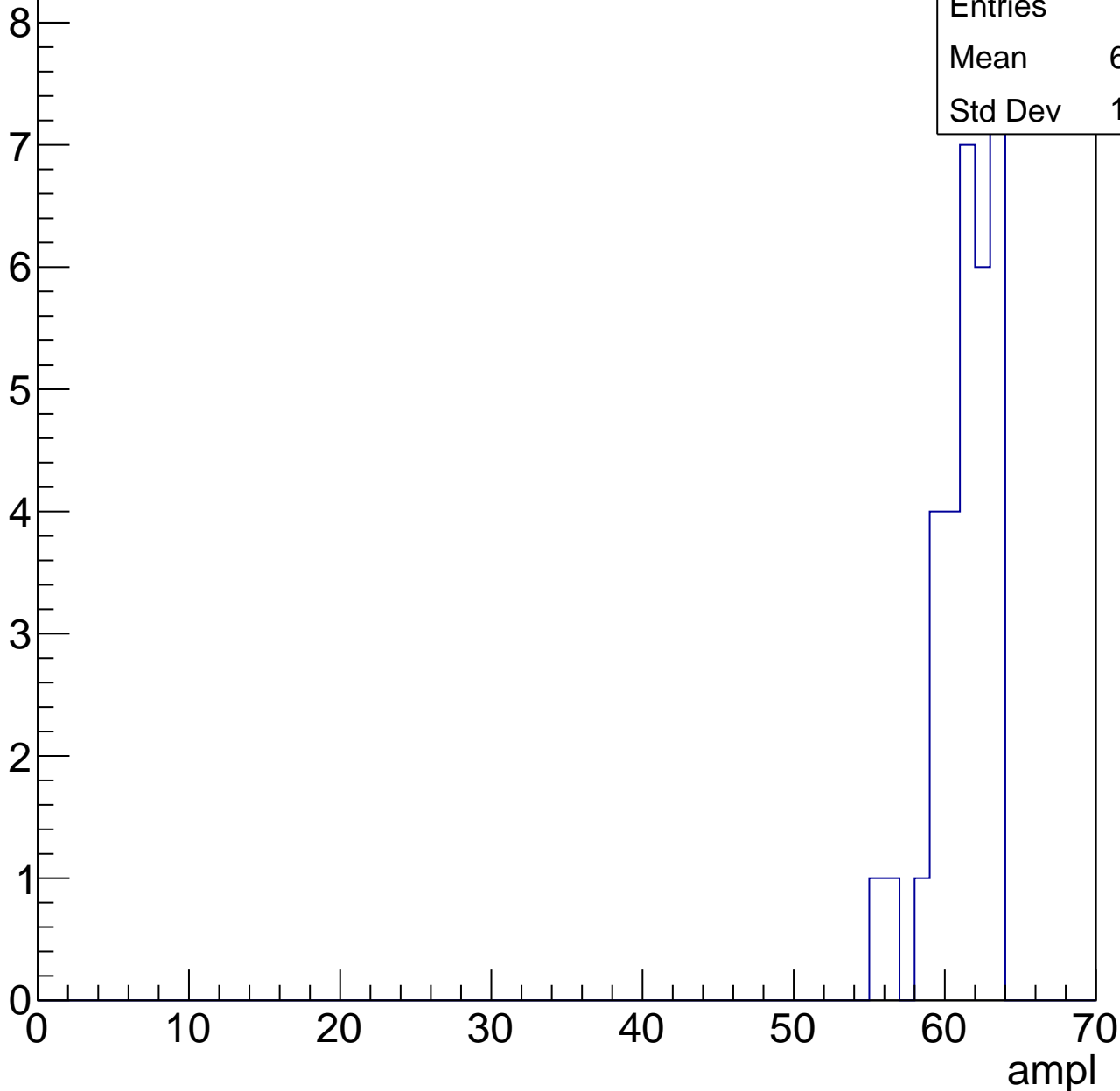


# B1L102S, U8-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

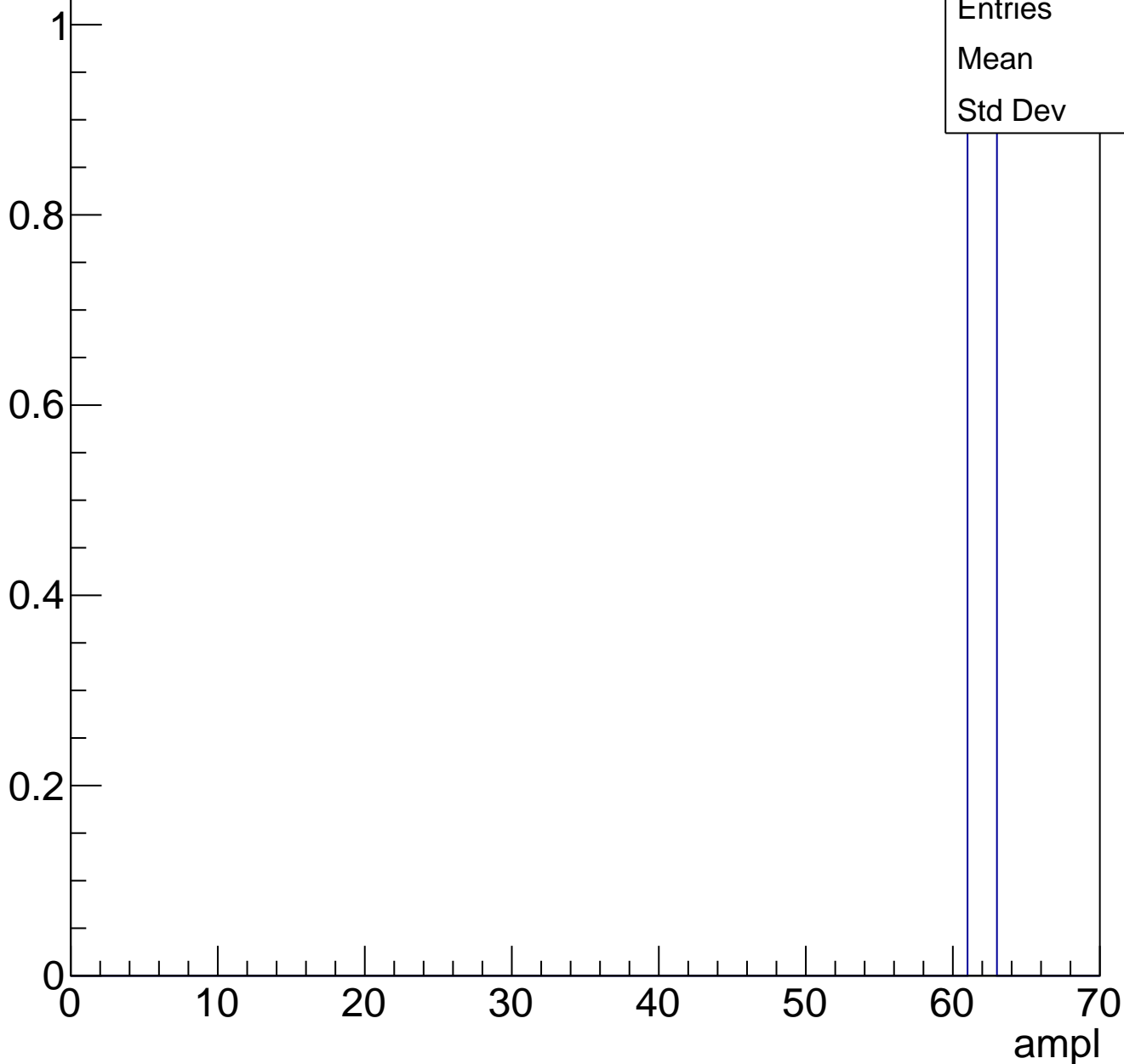
Entries	32
Mean	60.88
Std Dev	1.996



# B1L102S, U8-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch62, adc0

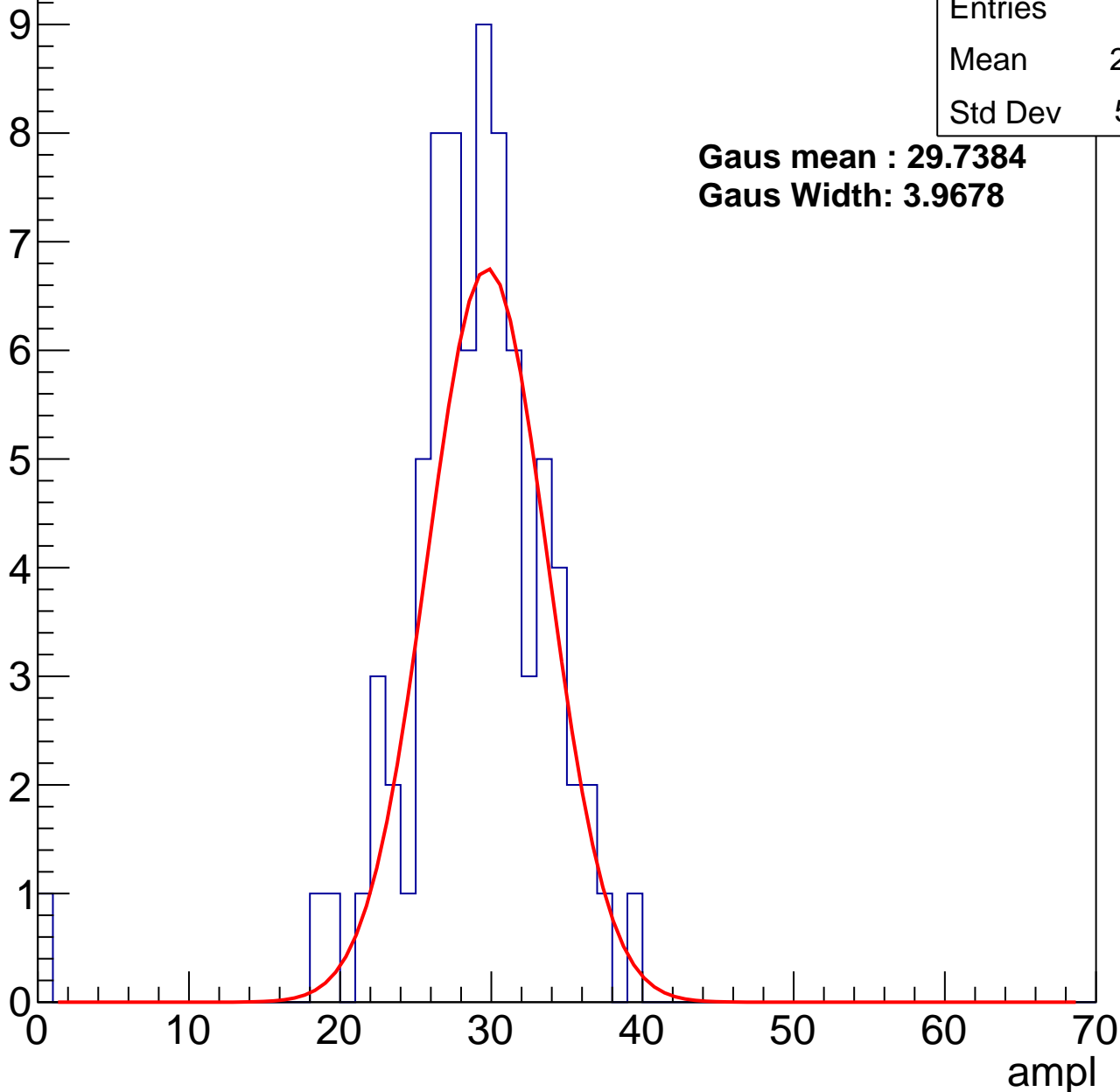
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	28.37
Std Dev	5.191

**Gaus mean : 29.7384**

**Gaus Width: 3.9678**



# B1L102S, U8-ch62, adc1

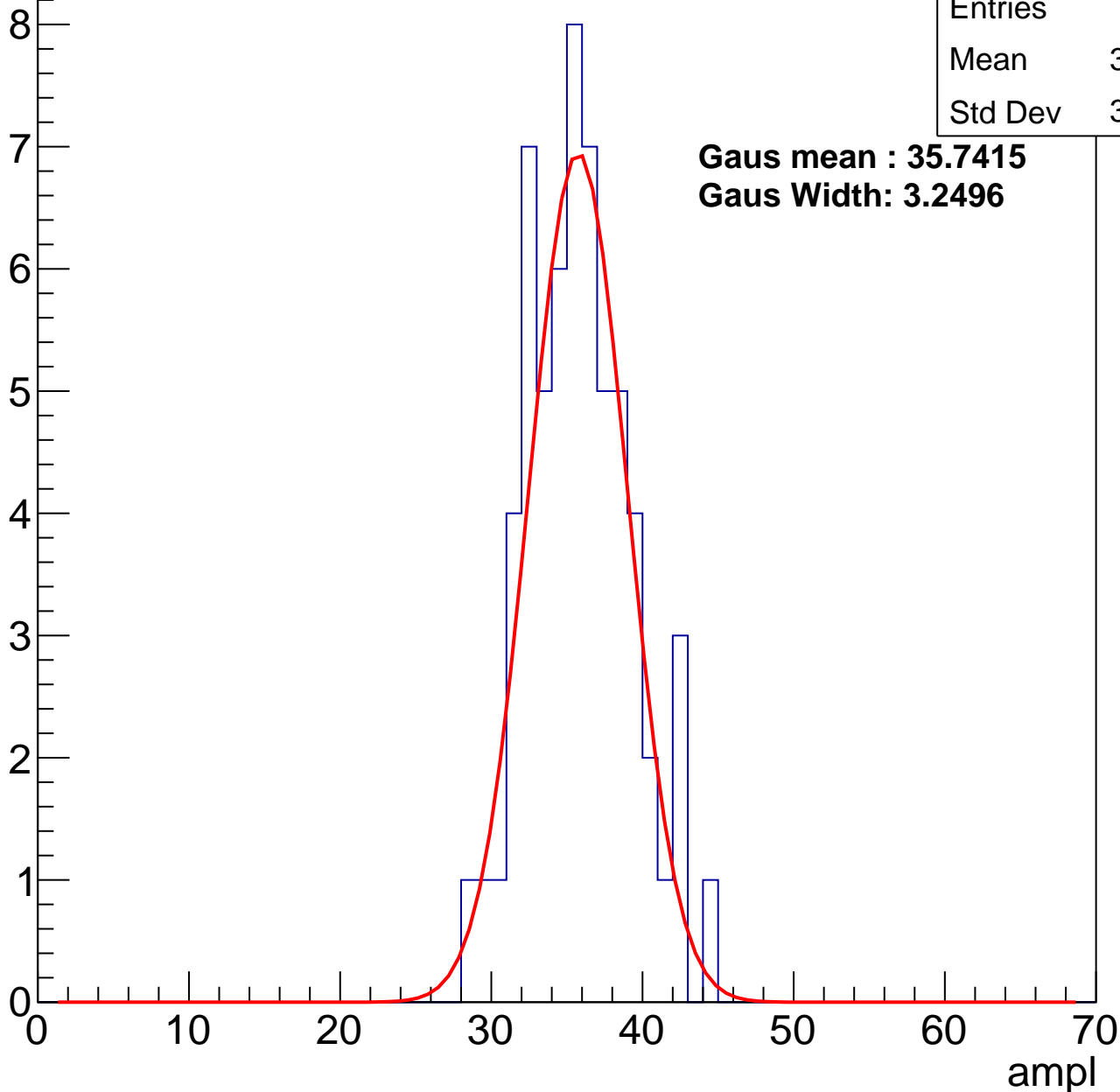
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	35.38
Std Dev	3.398

**Gaus mean : 35.7415**

**Gaus Width: 3.2496**



# B1L102S, U8-ch62, adc2

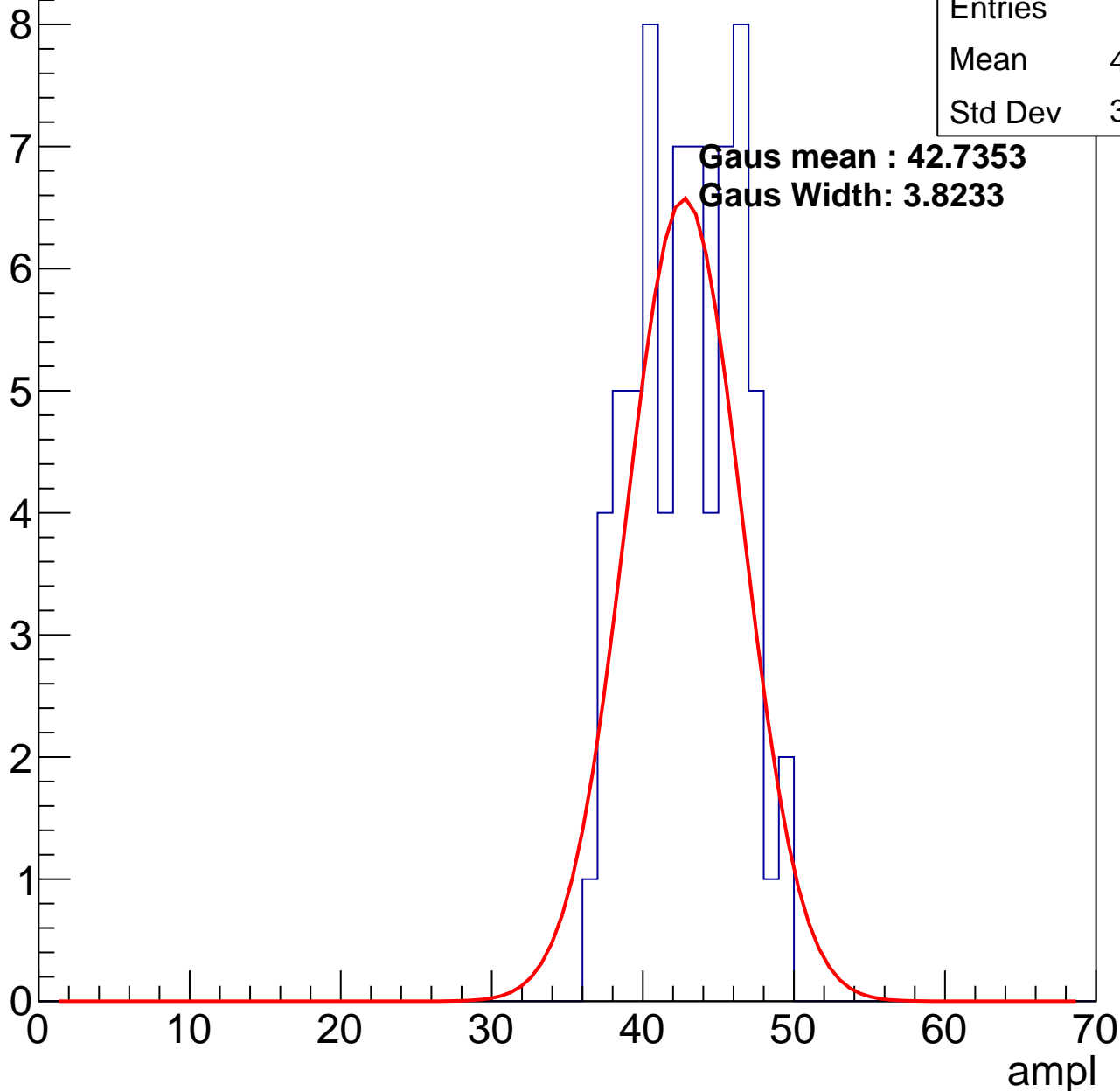
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	42.47
Std Dev	3.332

**Gaus mean : 42.7353**

**Gaus Width: 3.8233**

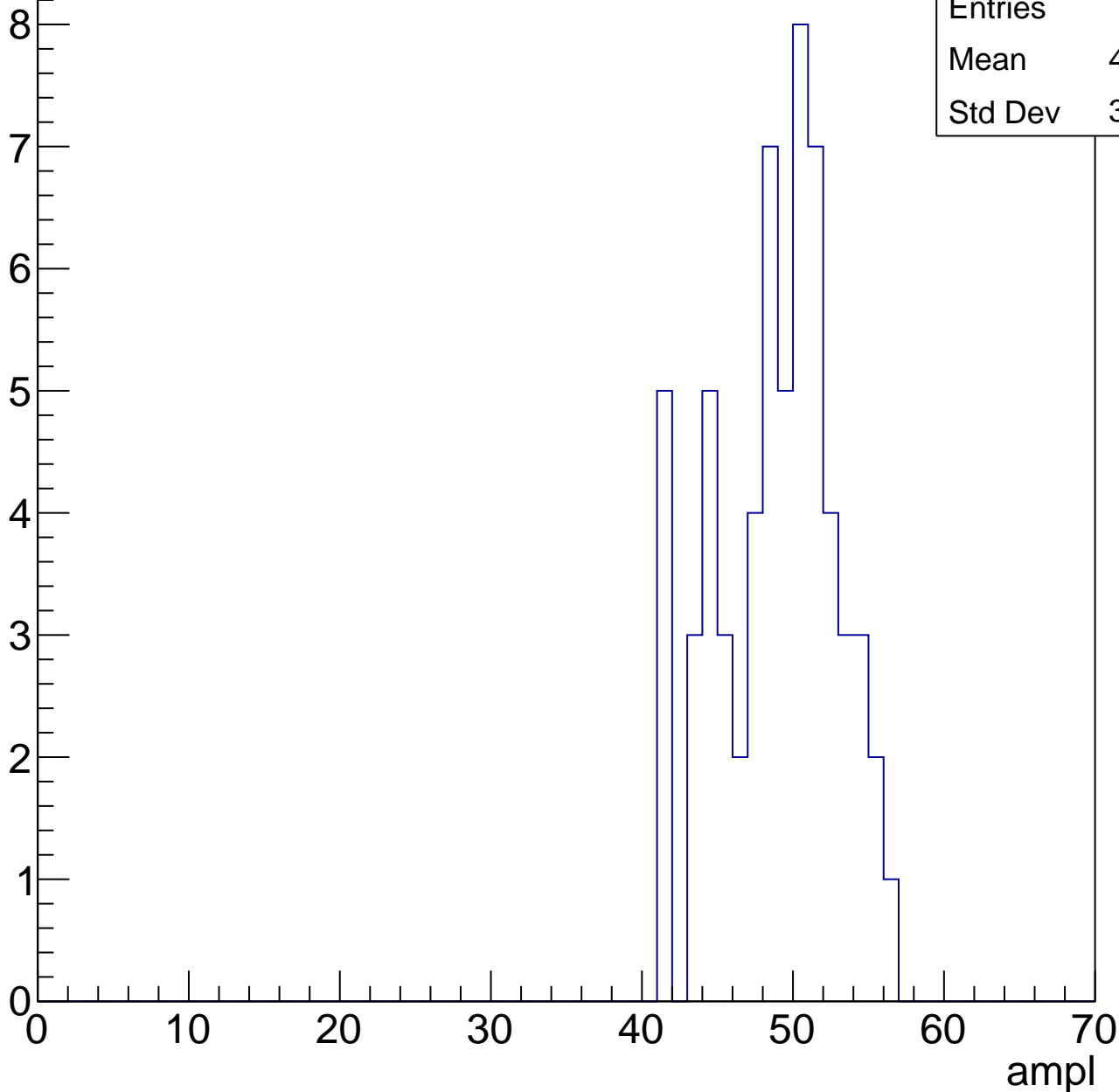


# B1L102S, U8-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

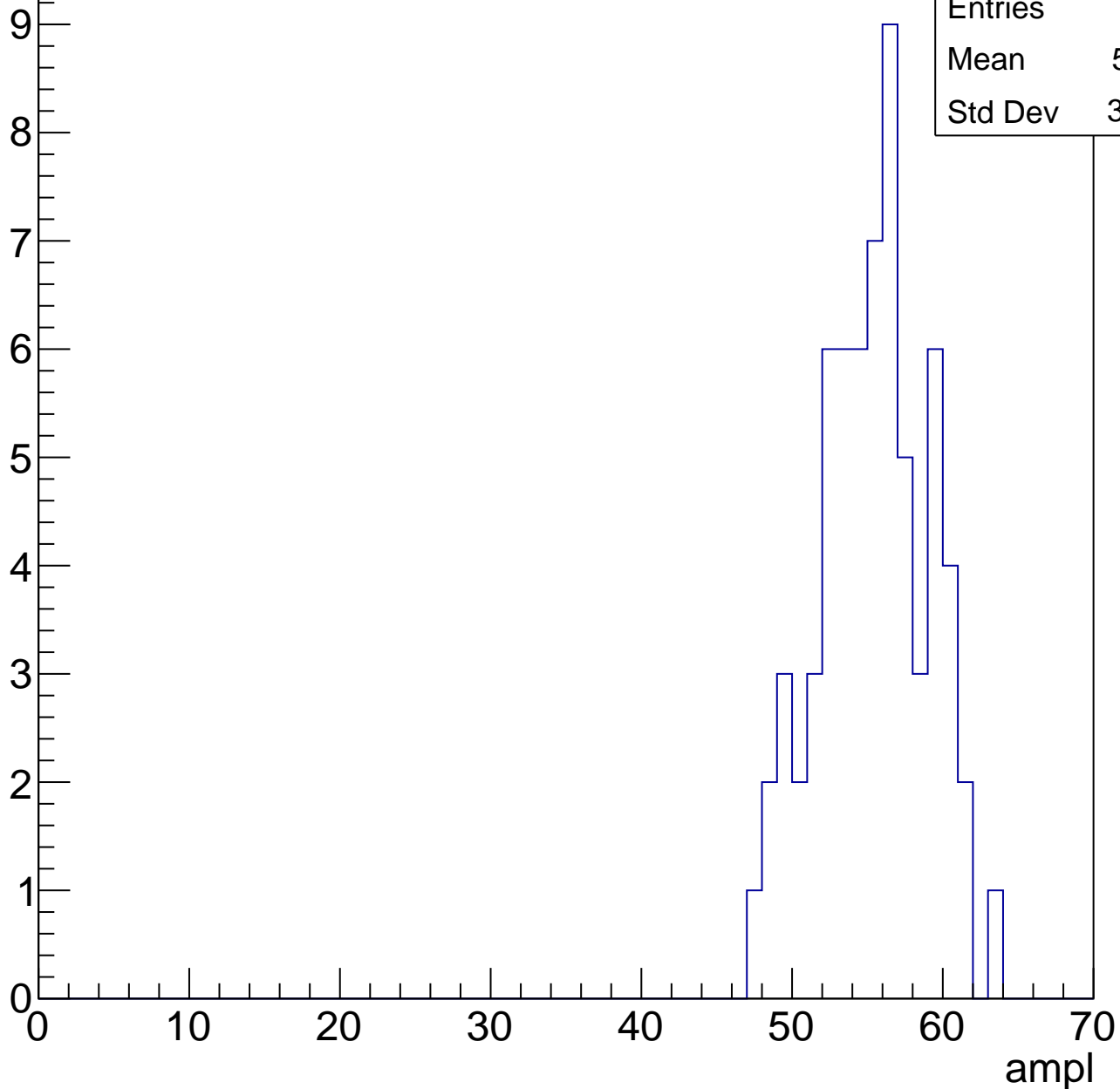
Entries	62
Mean	48.42
Std Dev	3.888



# B1L102S, U8-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

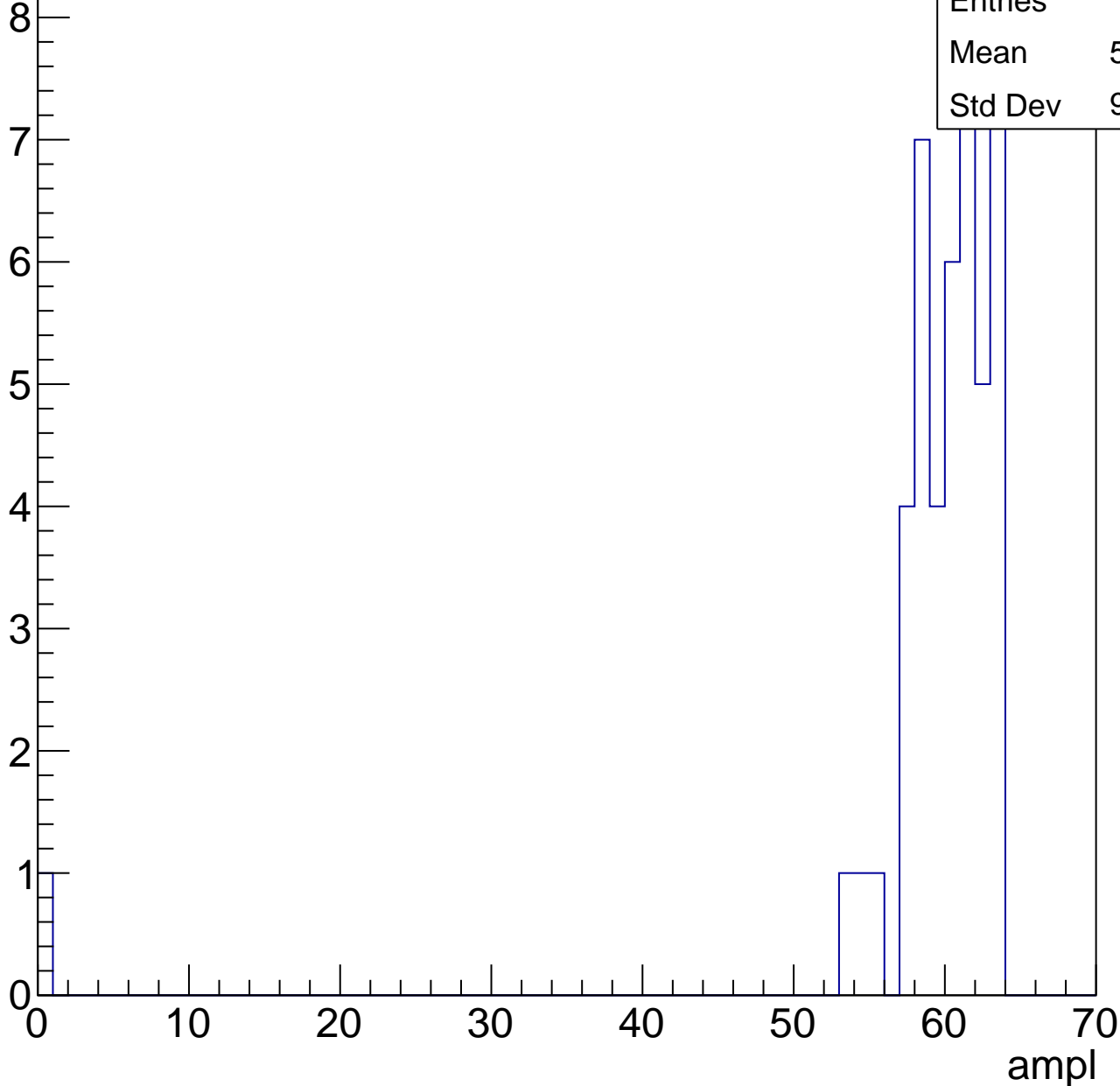


# B1L102S, U8-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	58.57
Std Dev	9.069

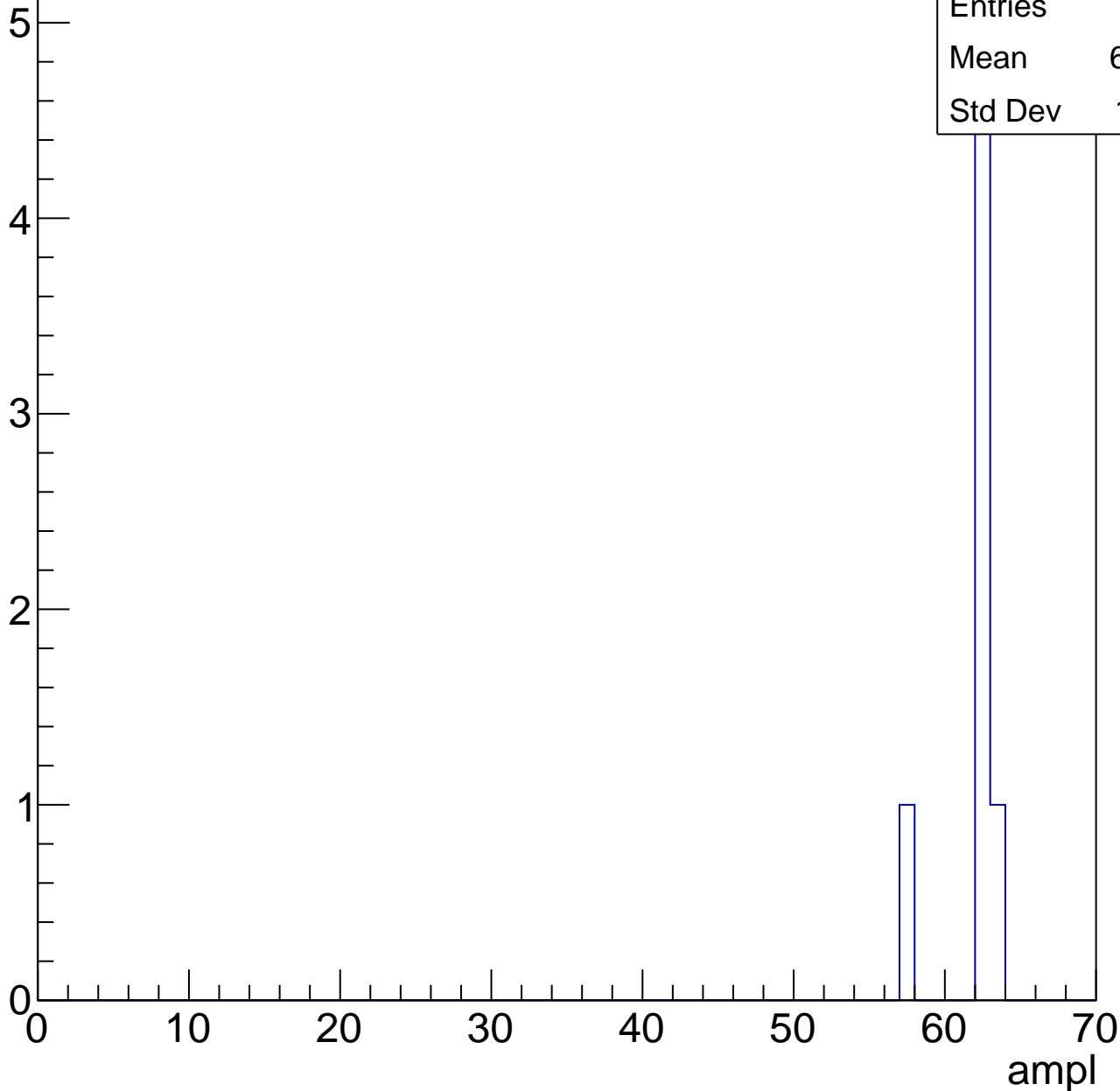


# B1L102S, U8-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	7
Mean	61.43
Std Dev	1.841





# B1L102S, U8-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch63, adc0

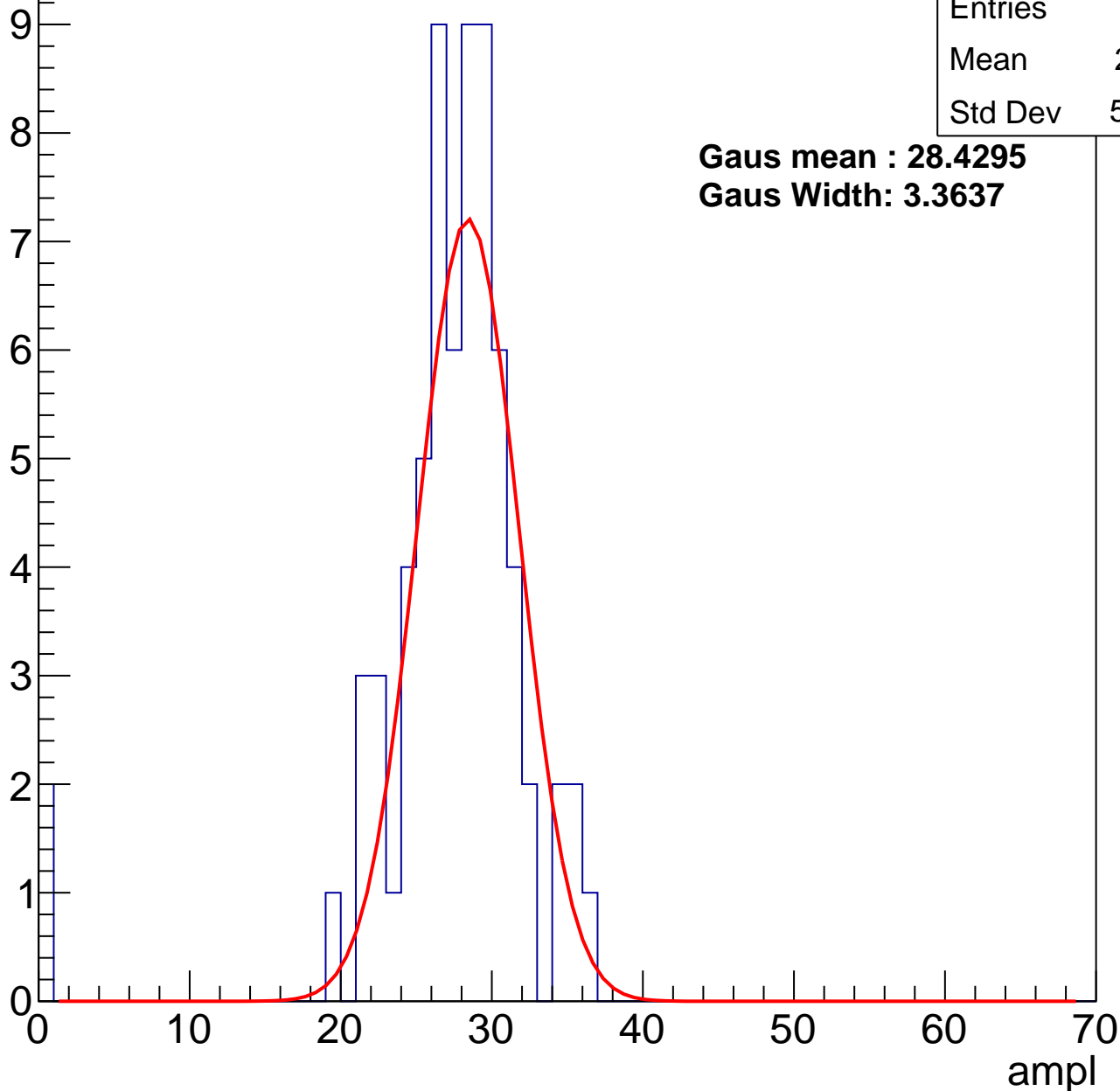
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	26.71
Std Dev	5.774

**Gaus mean : 28.4295**

**Gaus Width: 3.3637**



# B1L102S, U8-ch63, adc1

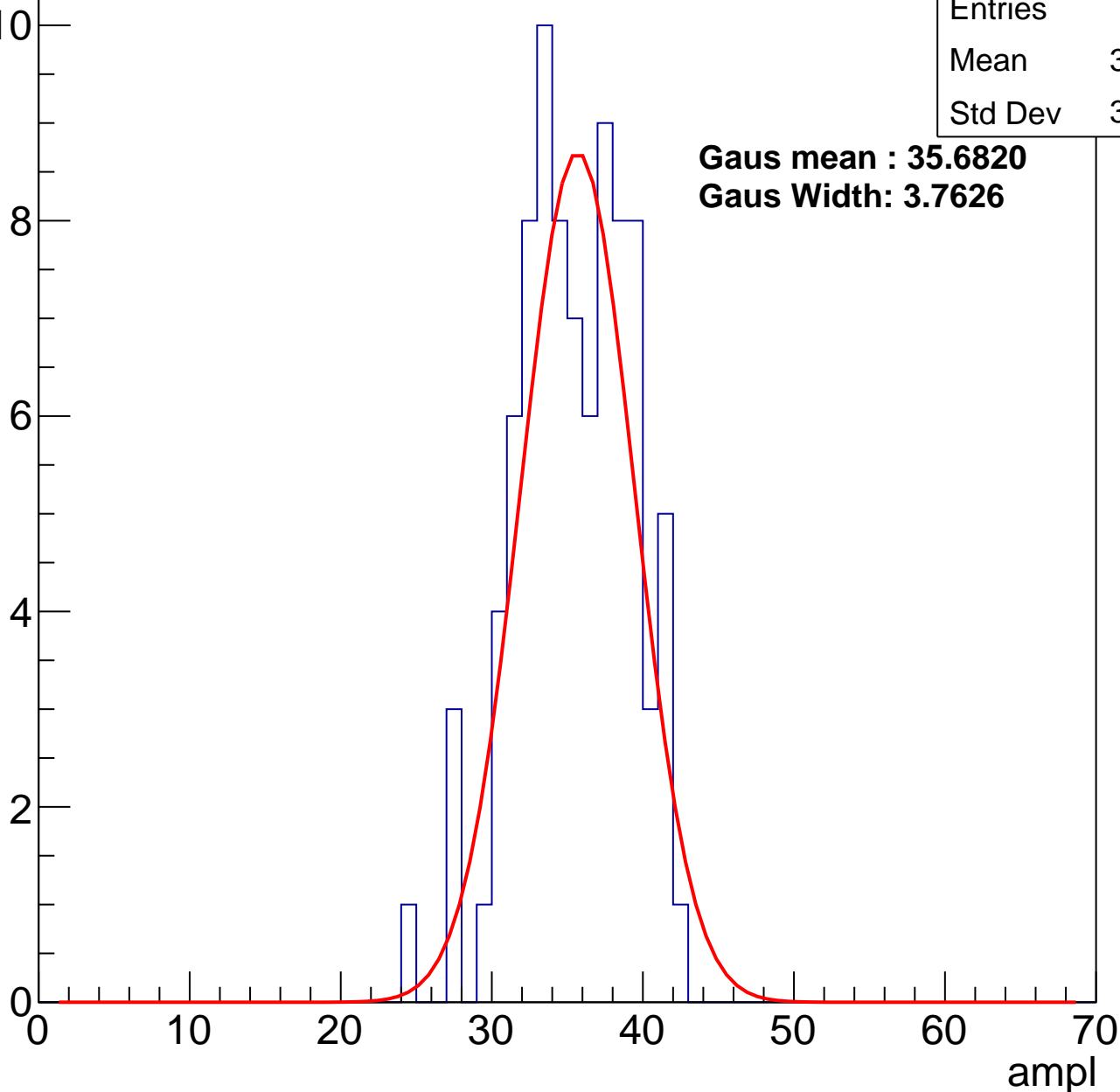
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	88
Mean	34.94
Std Dev	3.709

**Gaus mean : 35.6820**

**Gaus Width: 3.7626**

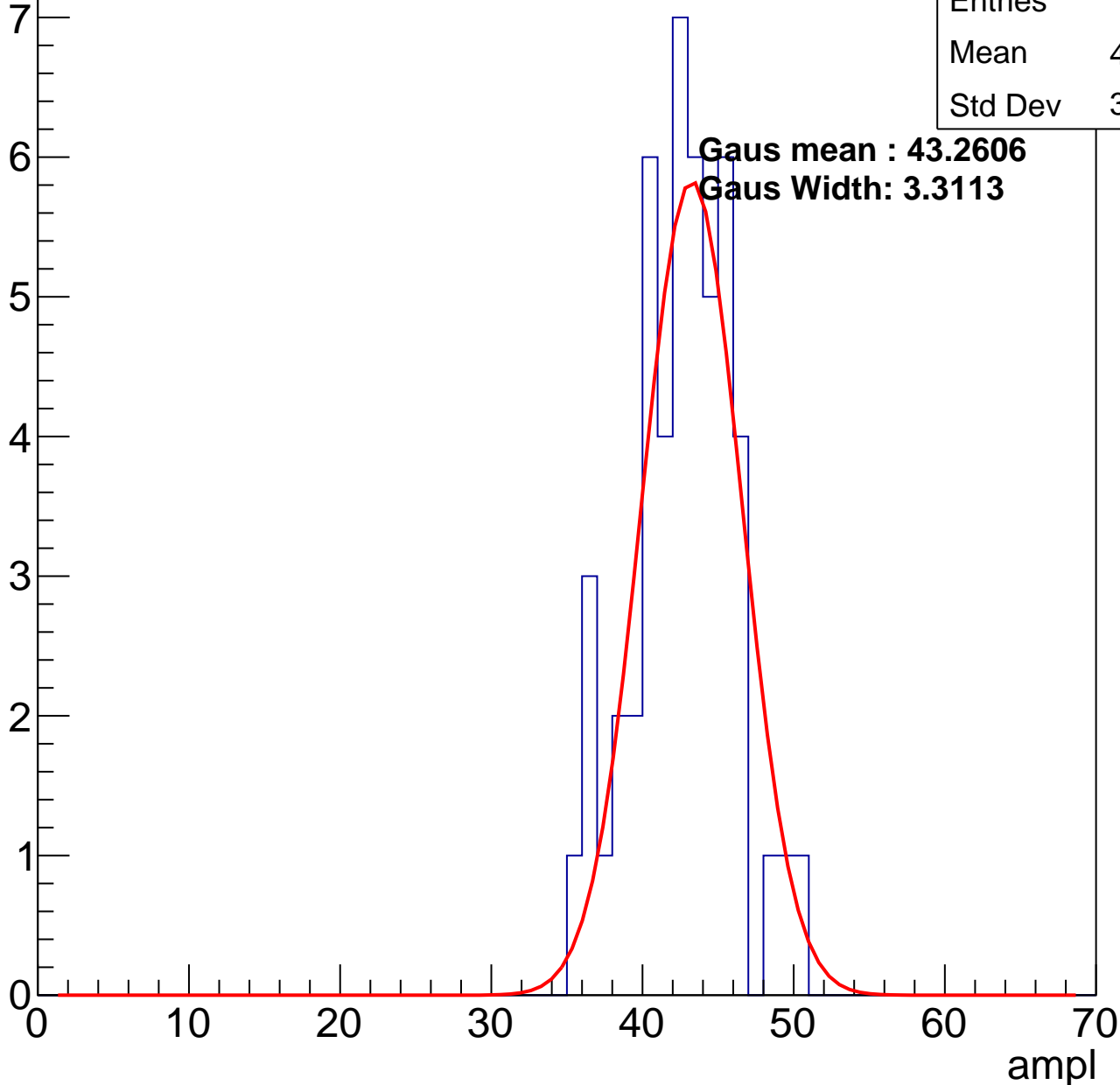


# B1L102S, U8-ch63, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	42.22
Std Dev	3.318



# B1L102S, U8-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

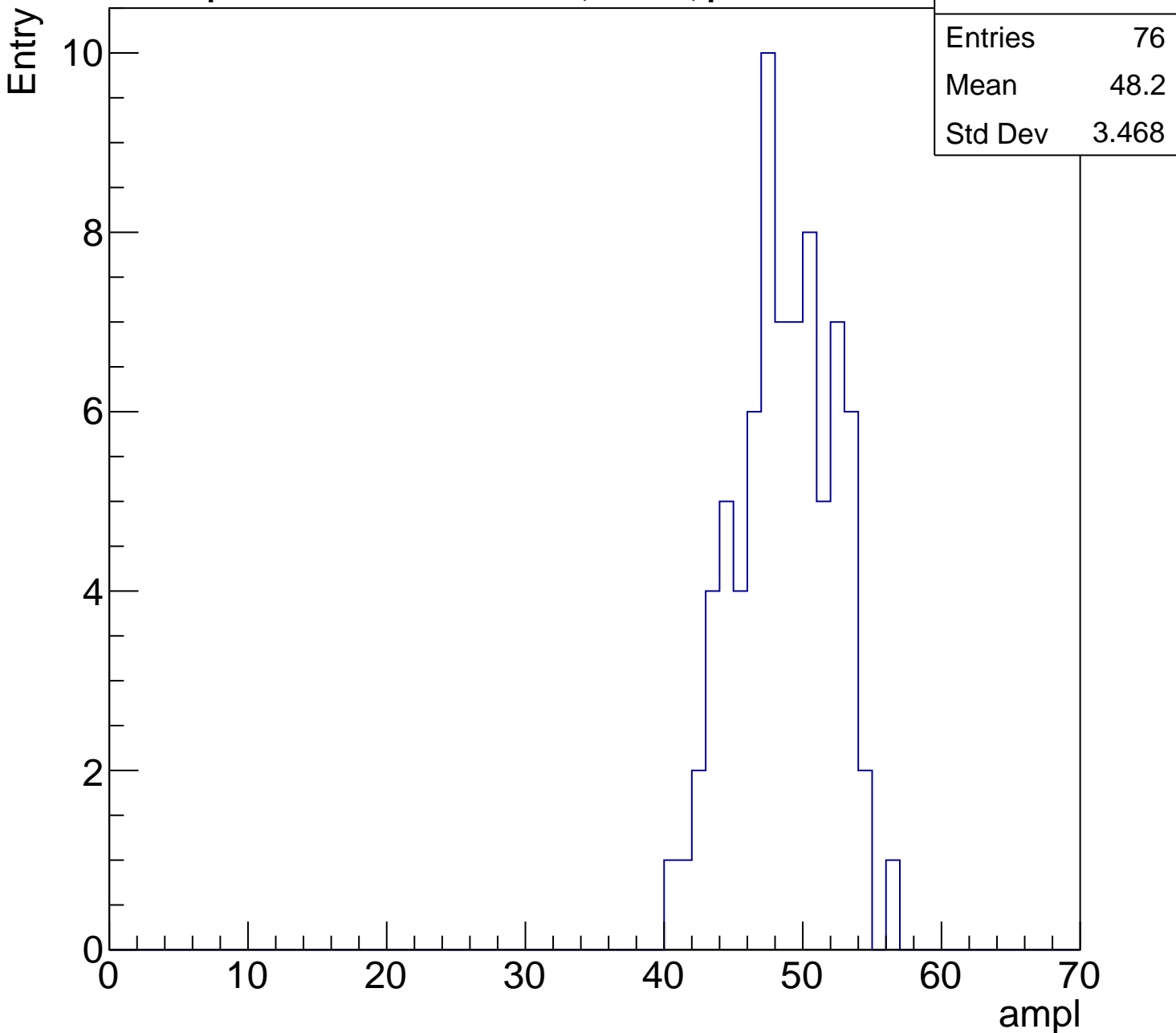
Entries	76
Mean	48.2
Std Dev	3.468

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

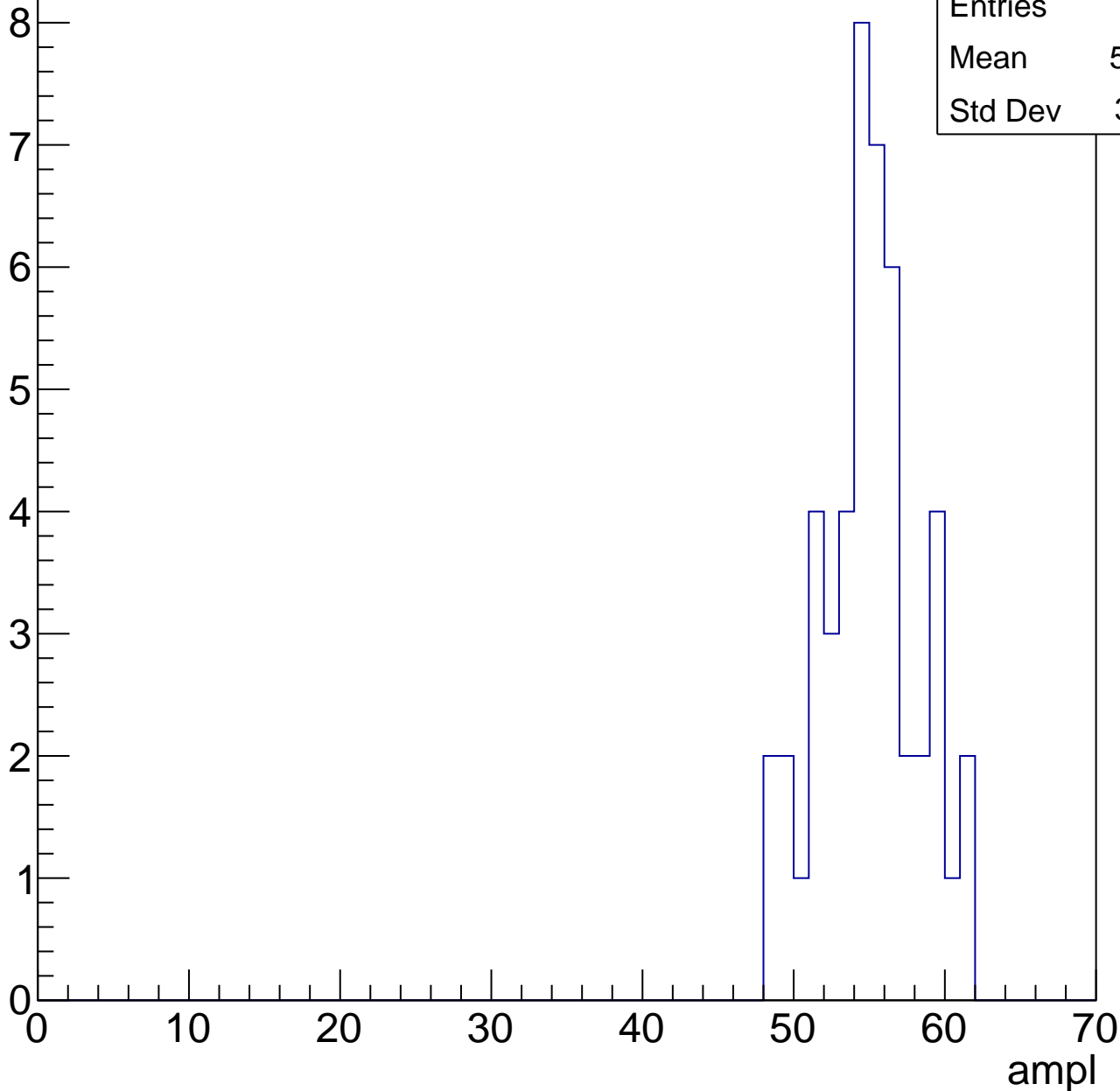


# B1L102S, U8-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	54.52
Std Dev	3.201

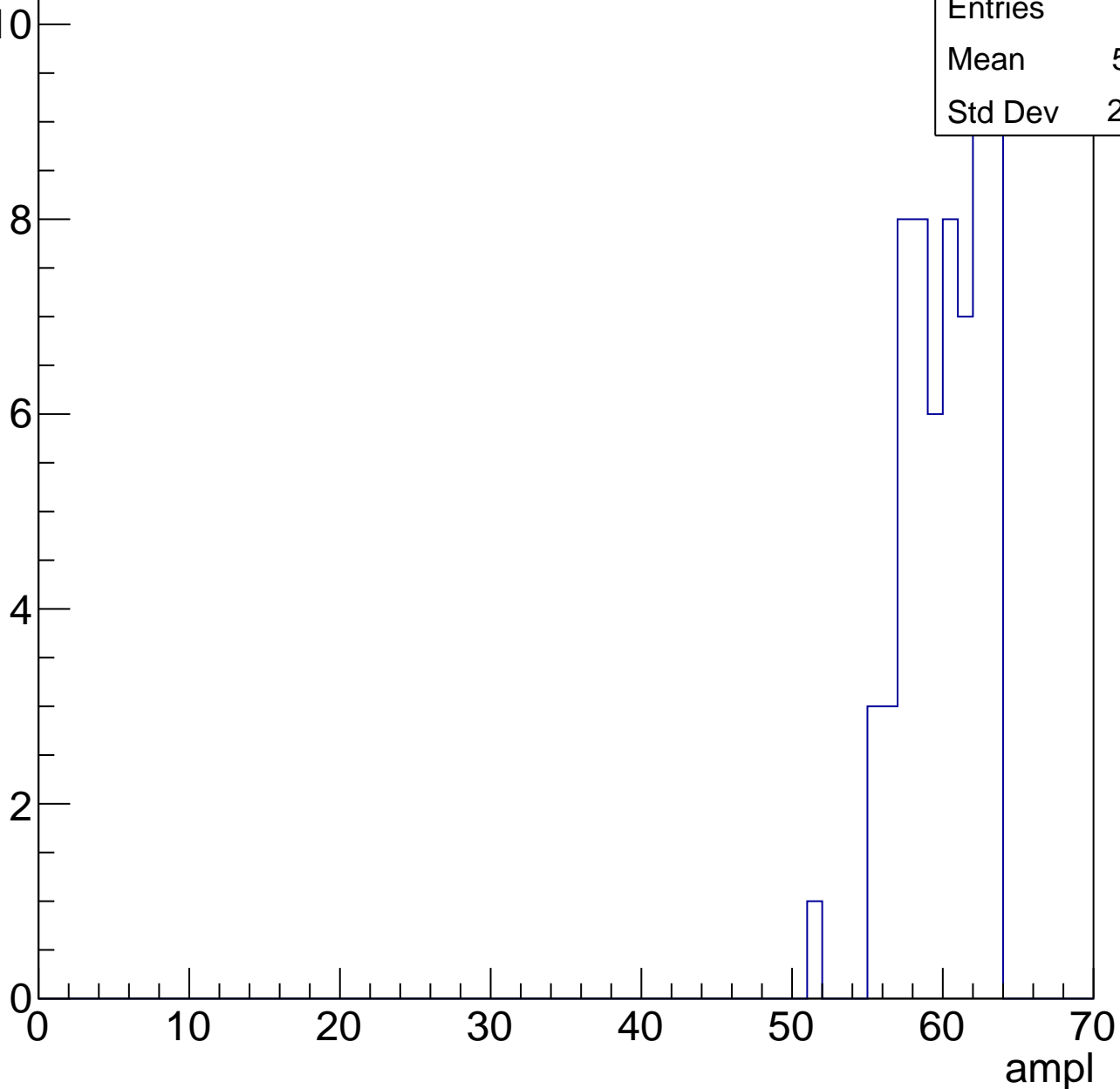


# B1L102S, U8-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

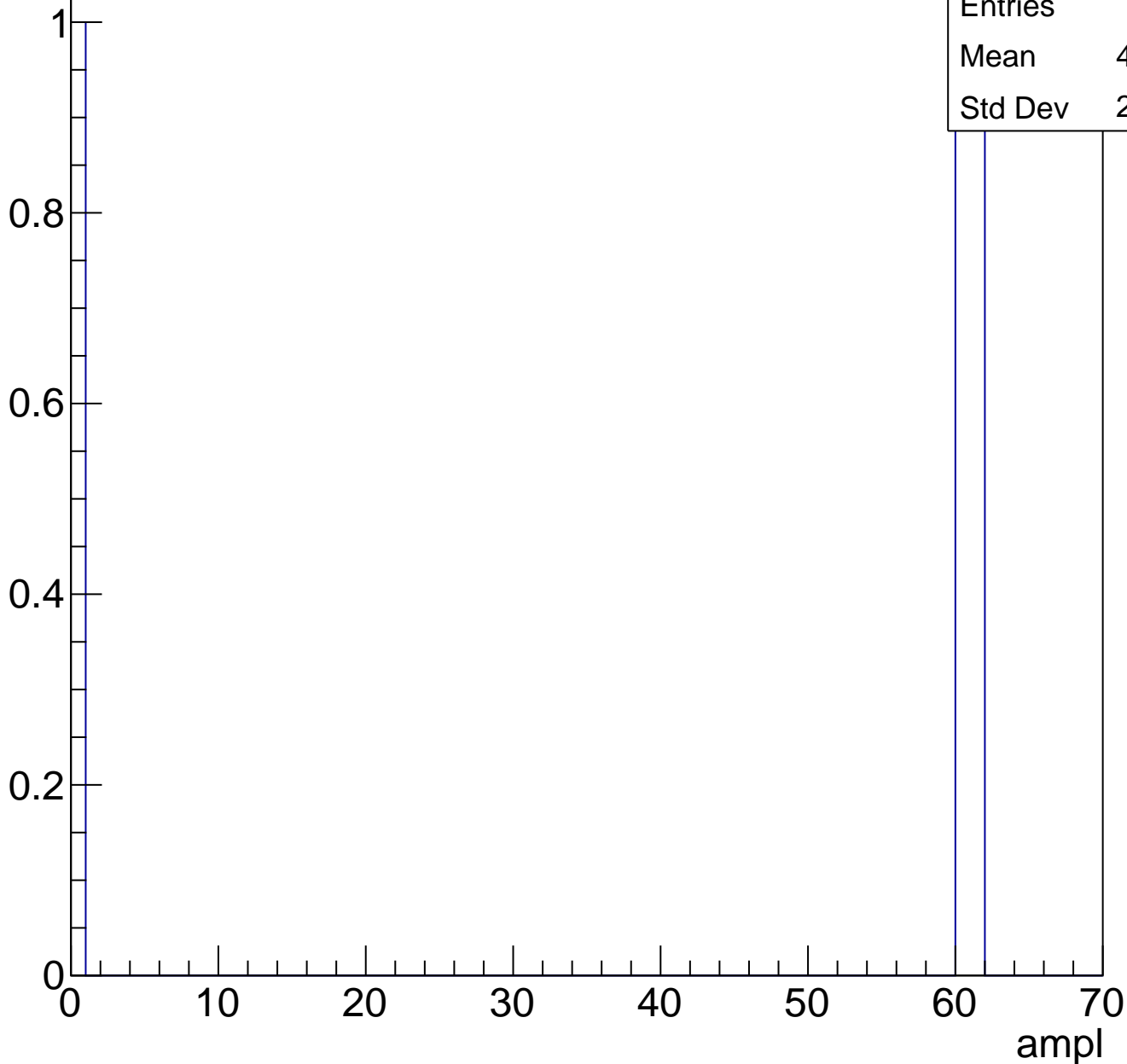
Entries	64
Mean	59.61
Std Dev	2.626



# B1L102S, U8-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch64, adc0

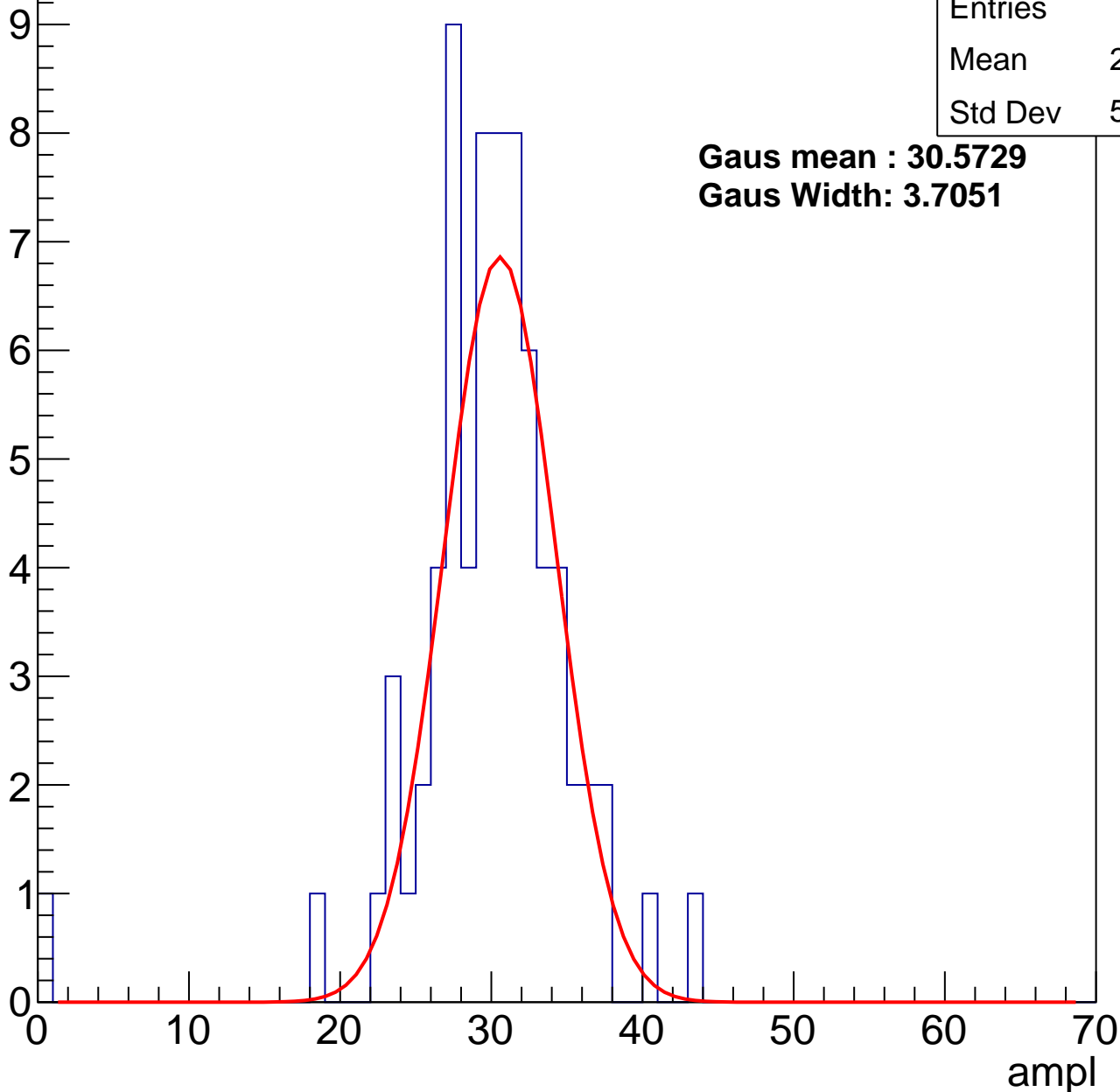
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	29.46
Std Dev	5.413

**Gaus mean : 30.5729**

**Gaus Width: 3.7051**



# B1L102S, U8-ch64, adc1

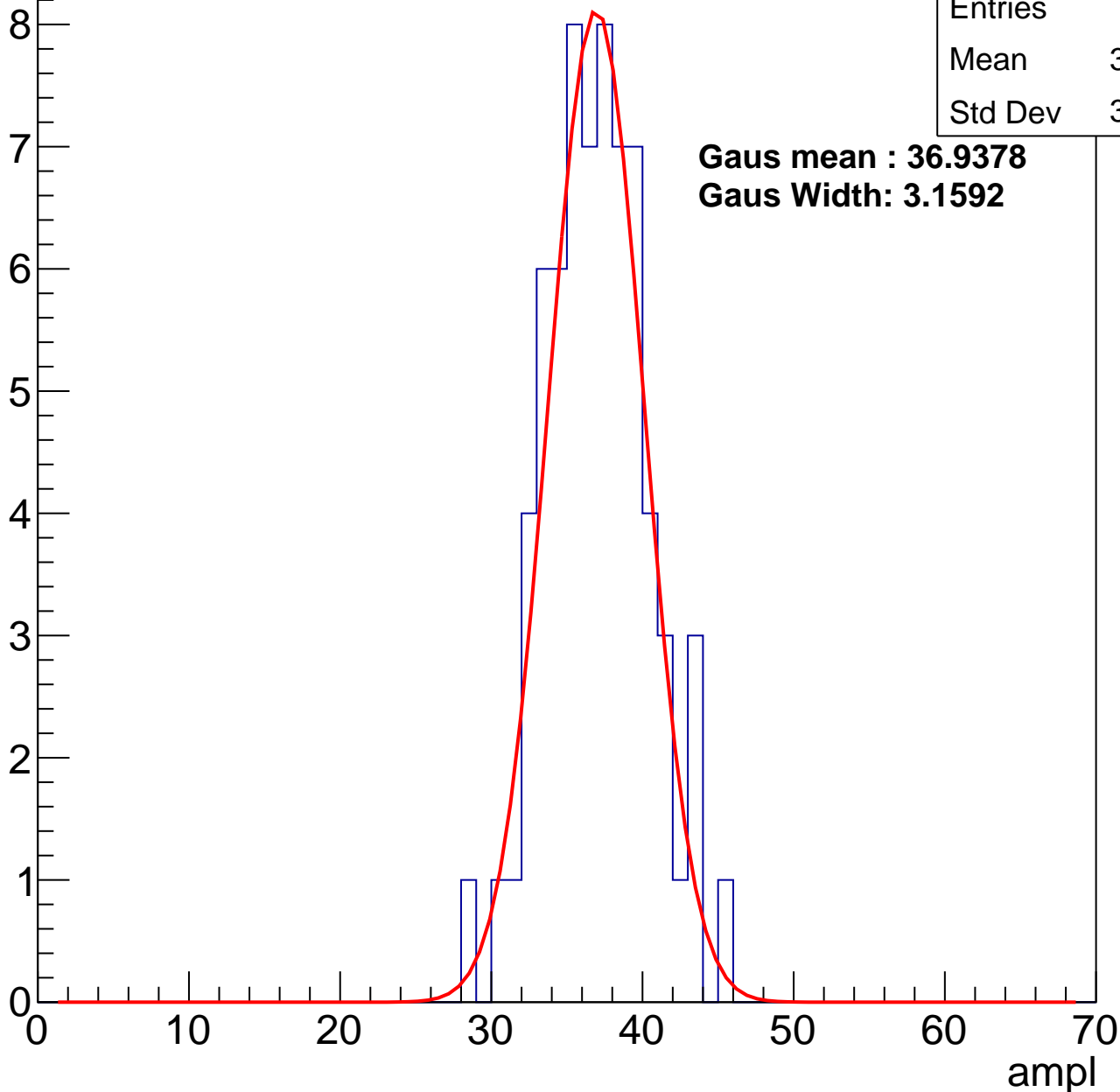
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	36.54
Std Dev	3.336

**Gaus mean : 36.9378**

**Gaus Width: 3.1592**



# B1L102S, U8-ch64, adc2

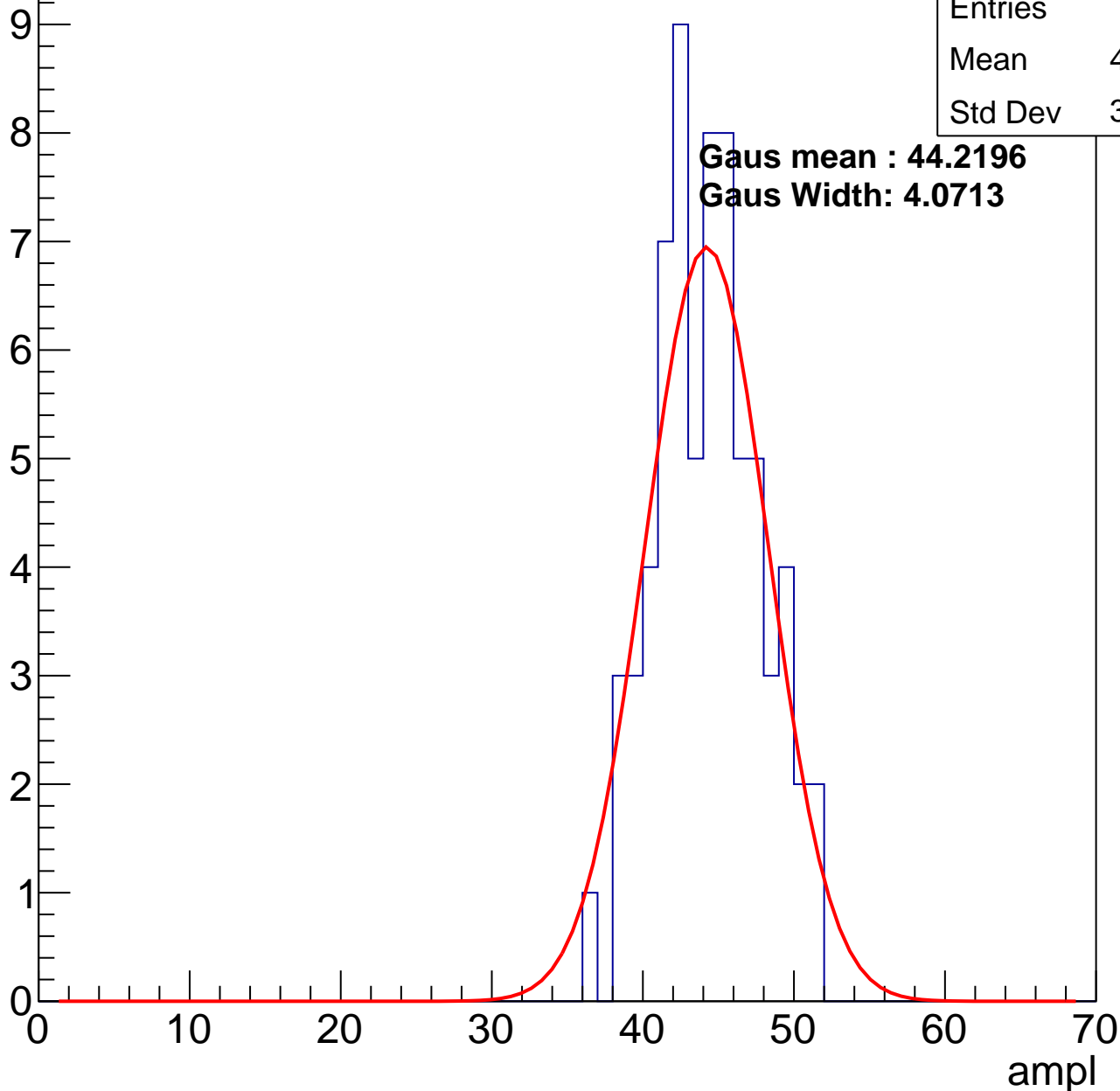
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	43.86
Std Dev	3.415

**Gaus mean : 44.2196**

**Gaus Width: 4.0713**

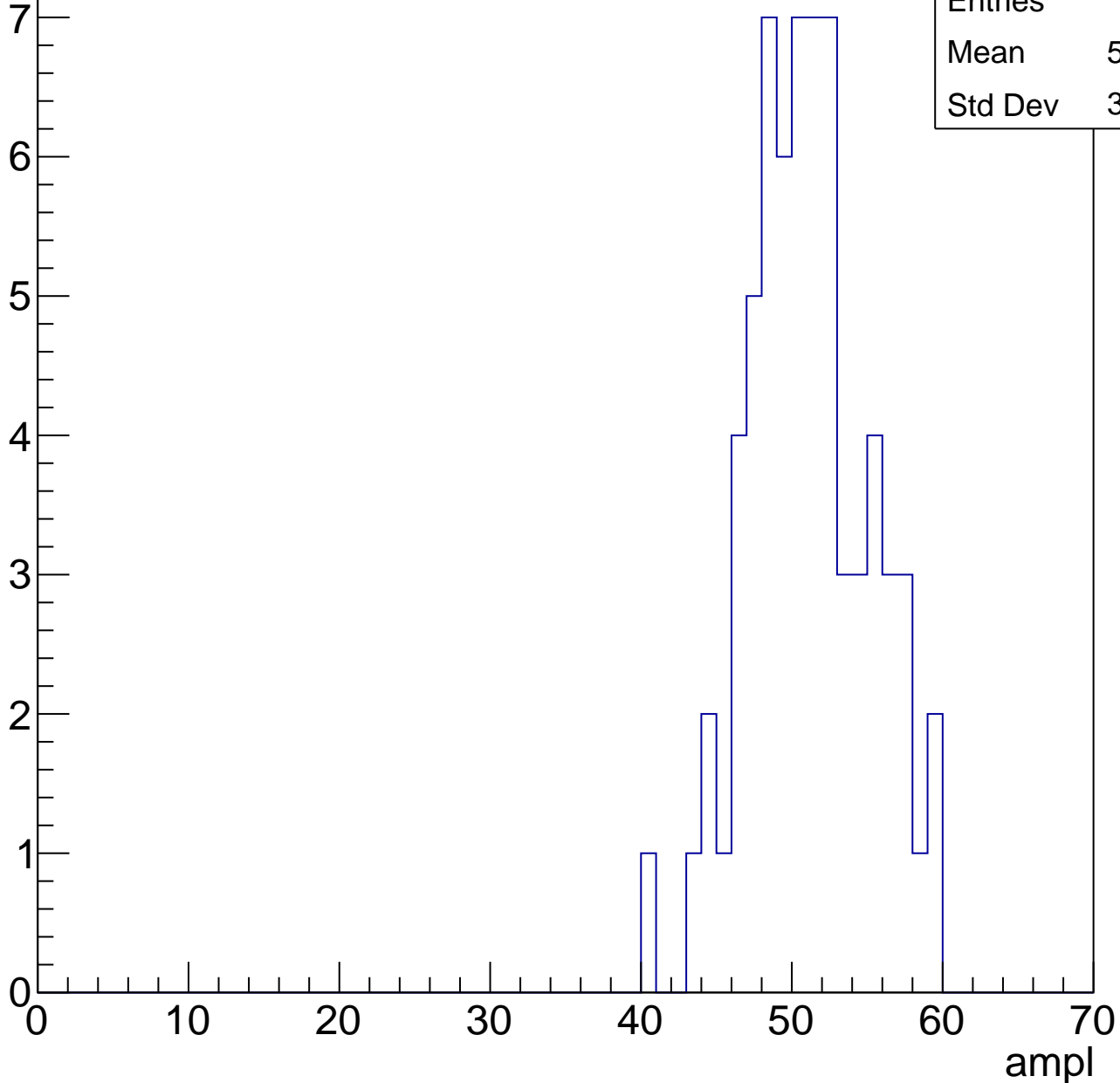


# B1L102S, U8-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	50.63
Std Dev	3.966



# B1L102S, U8-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

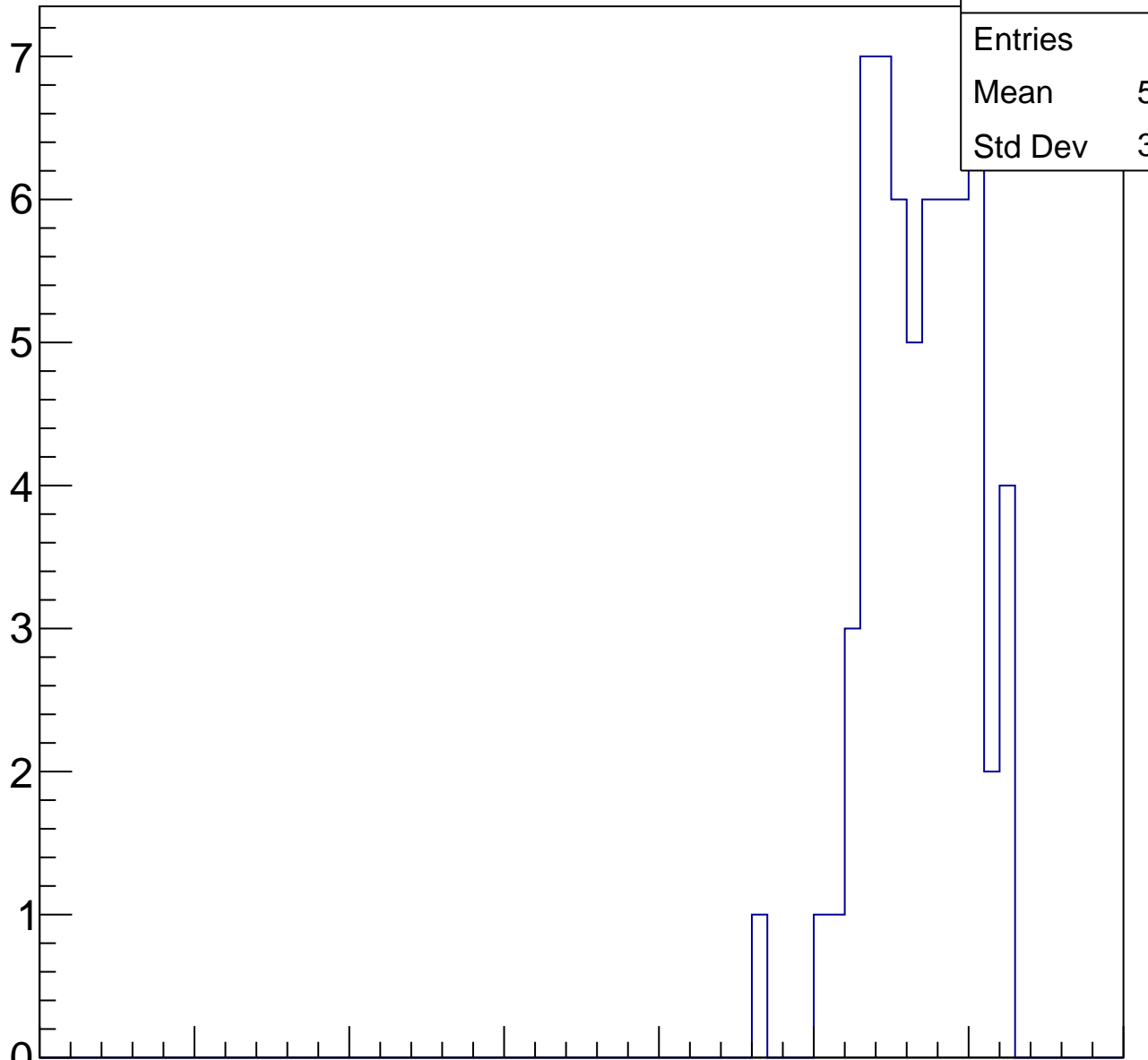
Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	62
Mean	56.39
Std Dev	3.328

ampl

0 10 20 30 40 50 60 70



# B1L102S, U8-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	34
Mean	59
Std Dev	10.47

ampl

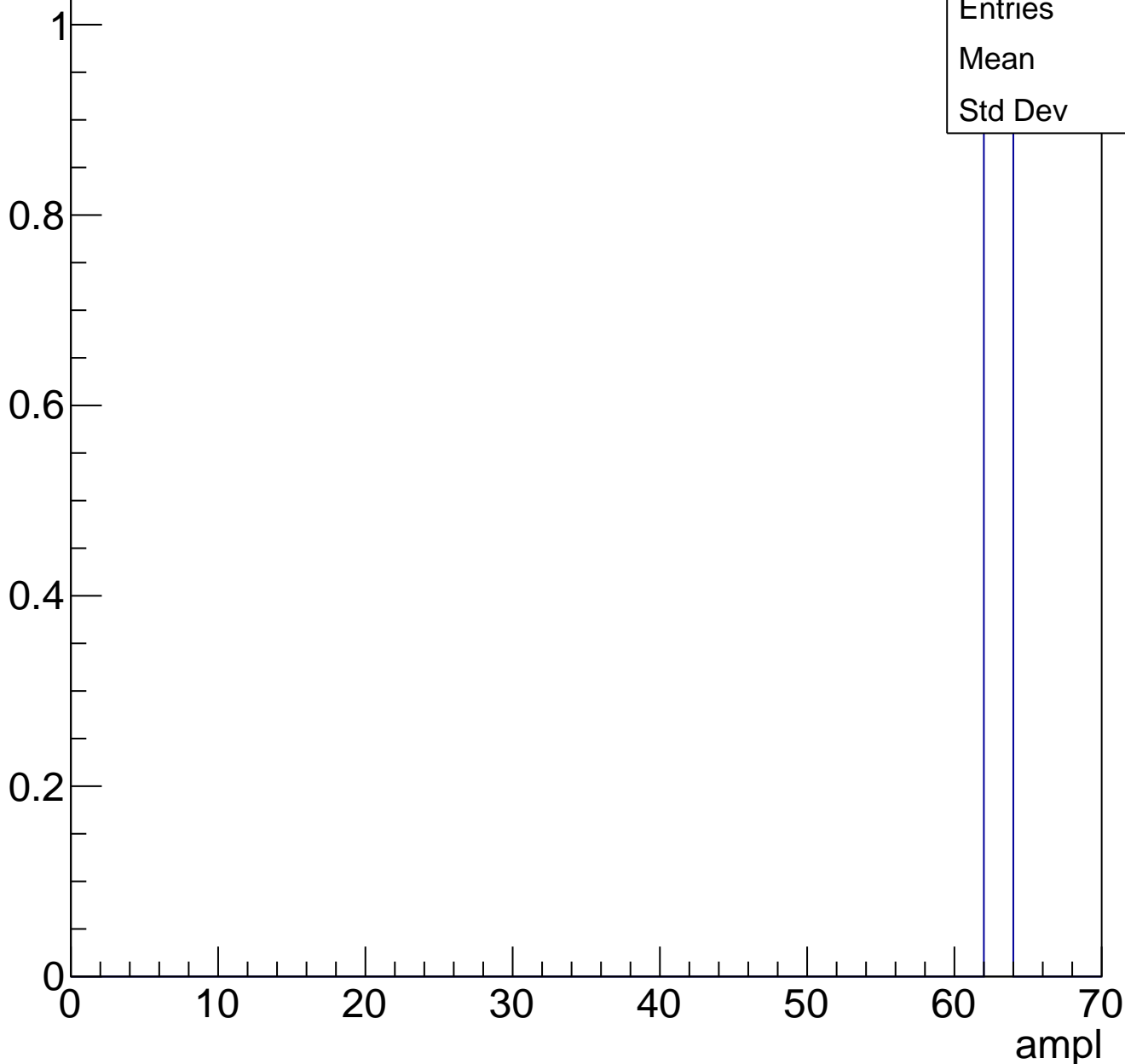
0 10 20 30 40 50 60 70

0 1 2 3 4 5 6 7 8 9

# B1L102S, U8-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch65, adc0

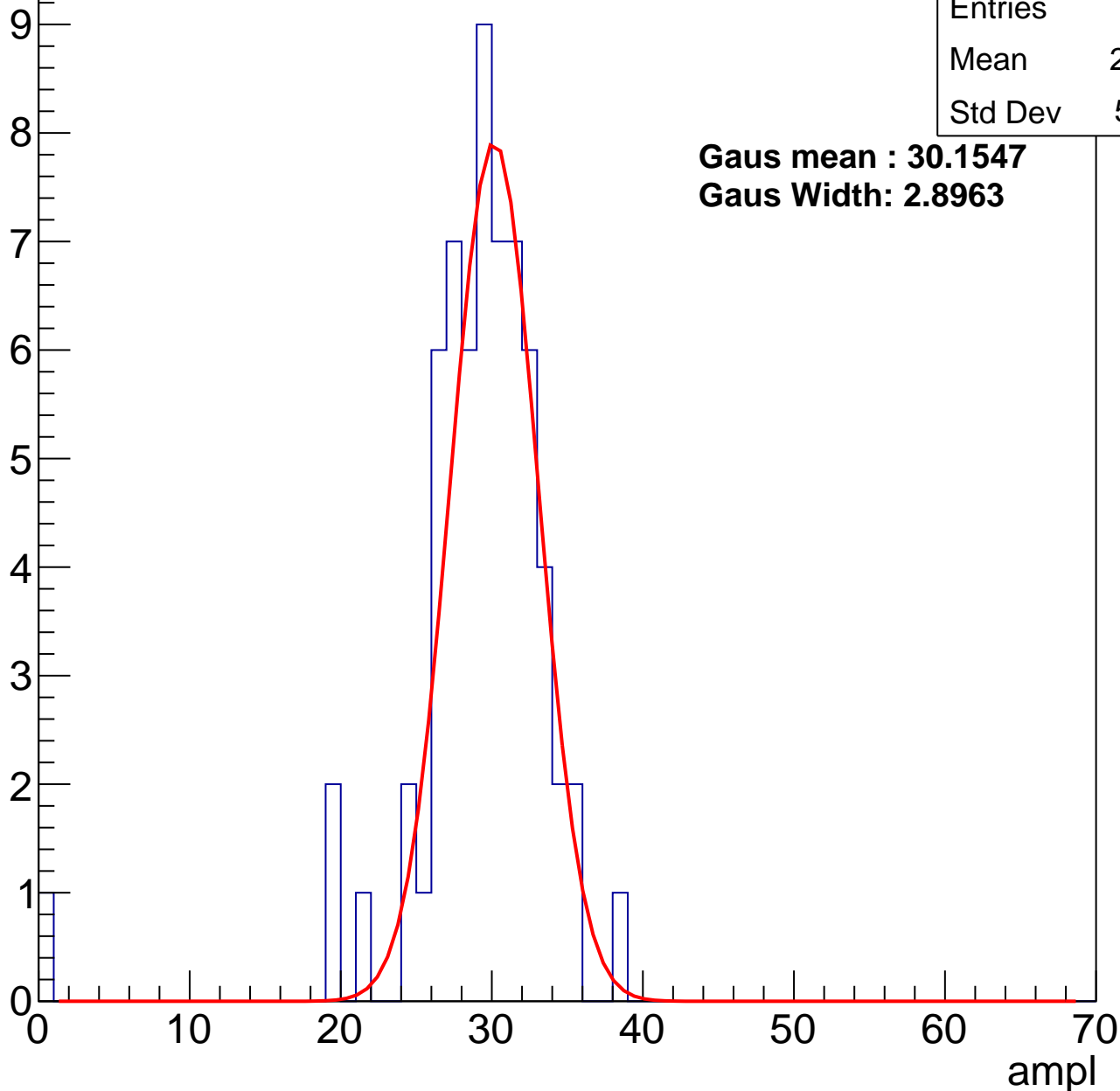
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	28.64
Std Dev	5.011

**Gaus mean : 30.1547**

**Gaus Width: 2.8963**



# B1L102S, U8-ch65, adc1

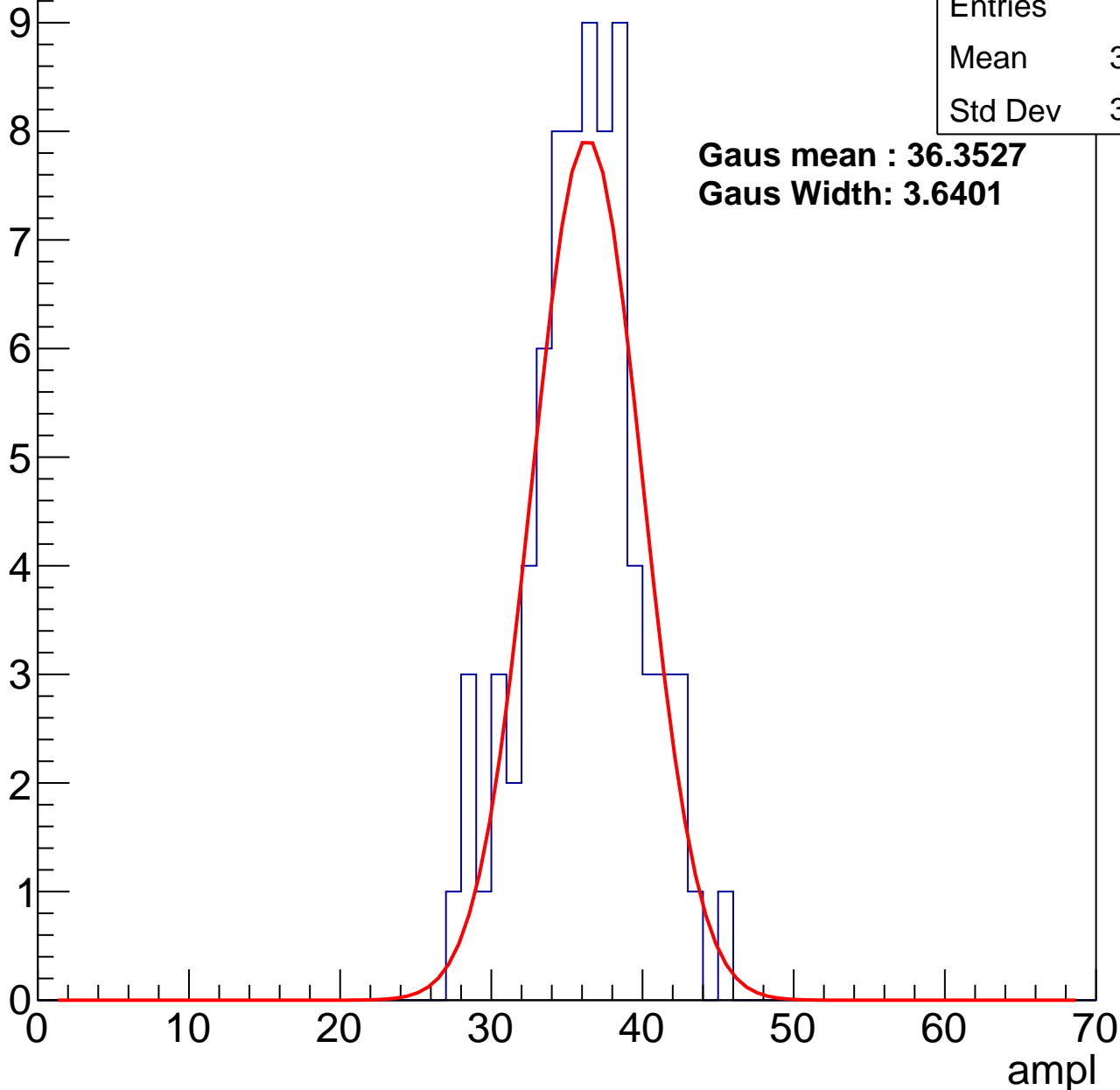
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	35.65
Std Dev	3.727

**Gaus mean : 36.3527**

**Gaus Width: 3.6401**



# B1L102S, U8-ch65, adc2

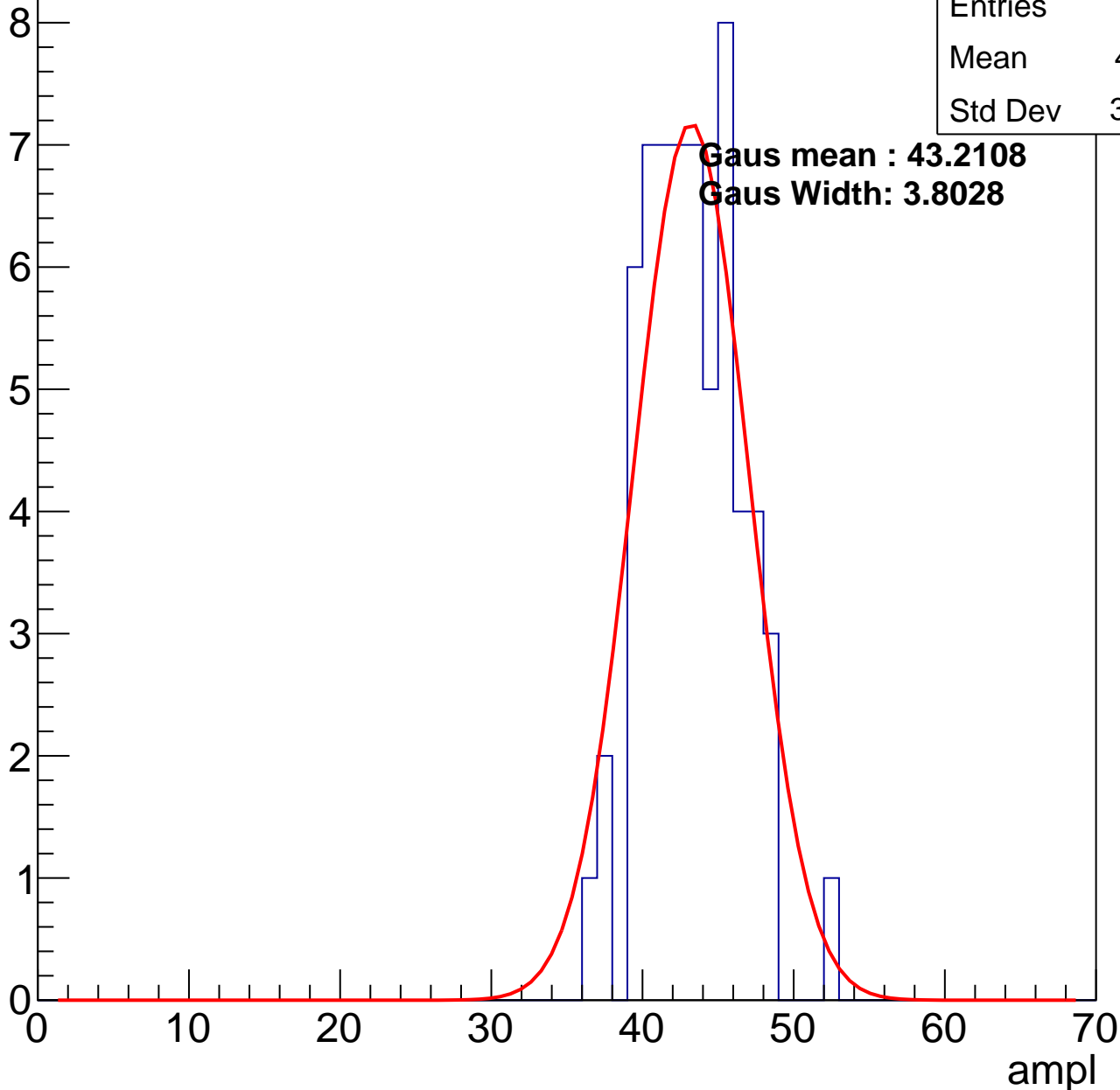
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	42.81
Std Dev	3.126

**Gaus mean : 43.2108**

**Gaus Width: 3.8028**



# B1L102S, U8-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

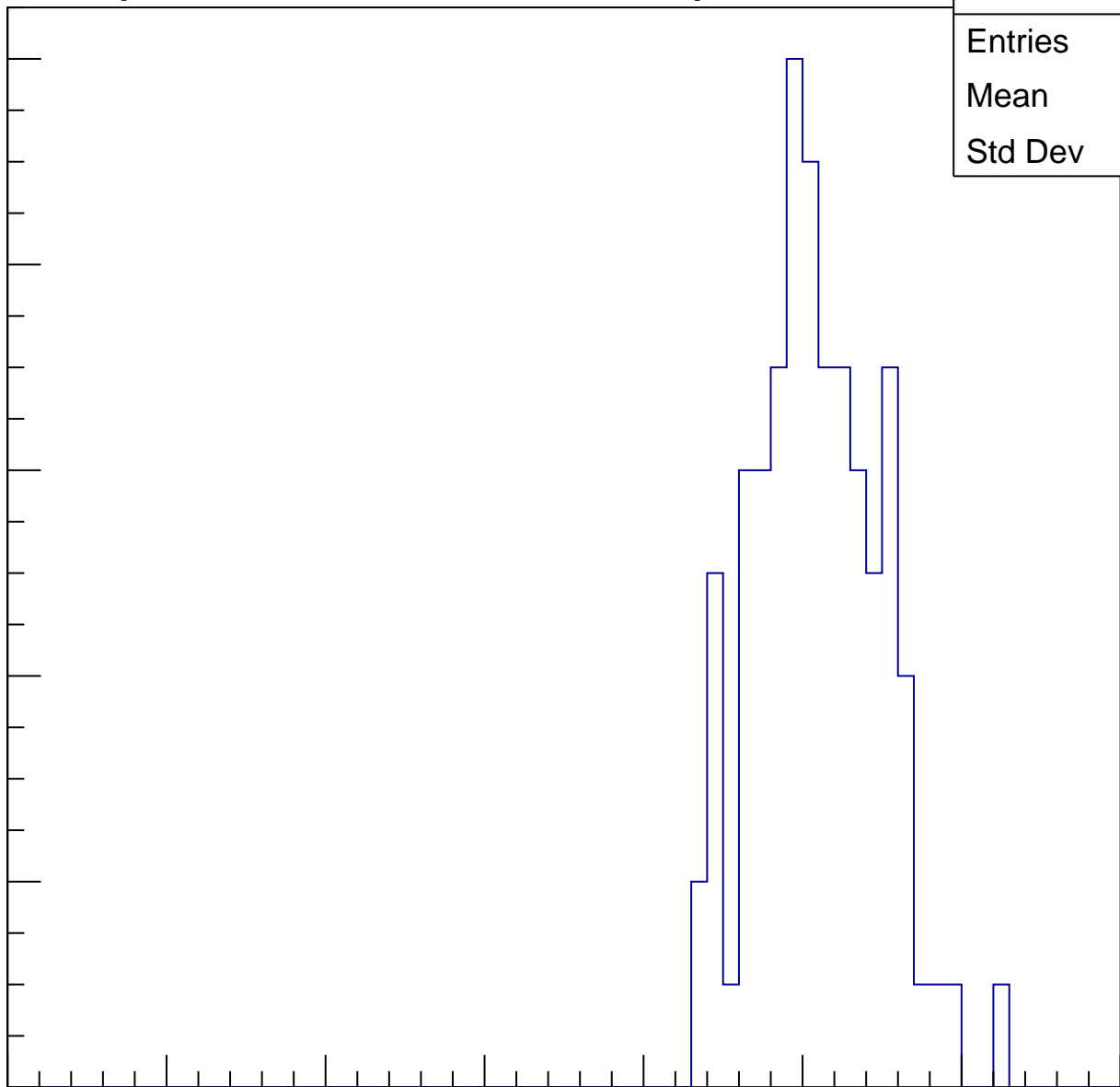
Entries	86
Mean	50.45
Std Dev	3.887

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

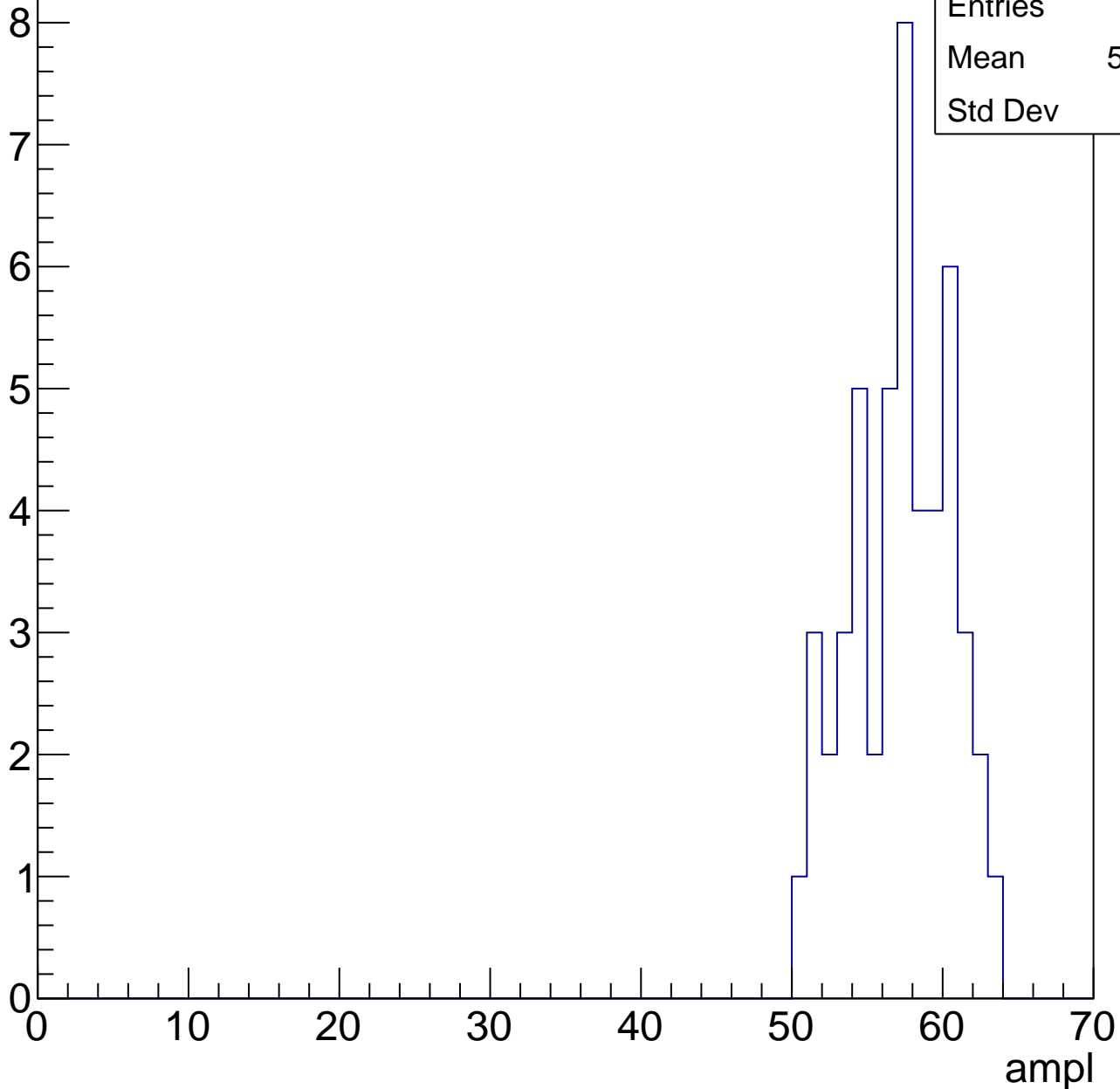


# B1L102S, U8-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	56.73
Std Dev	3.25

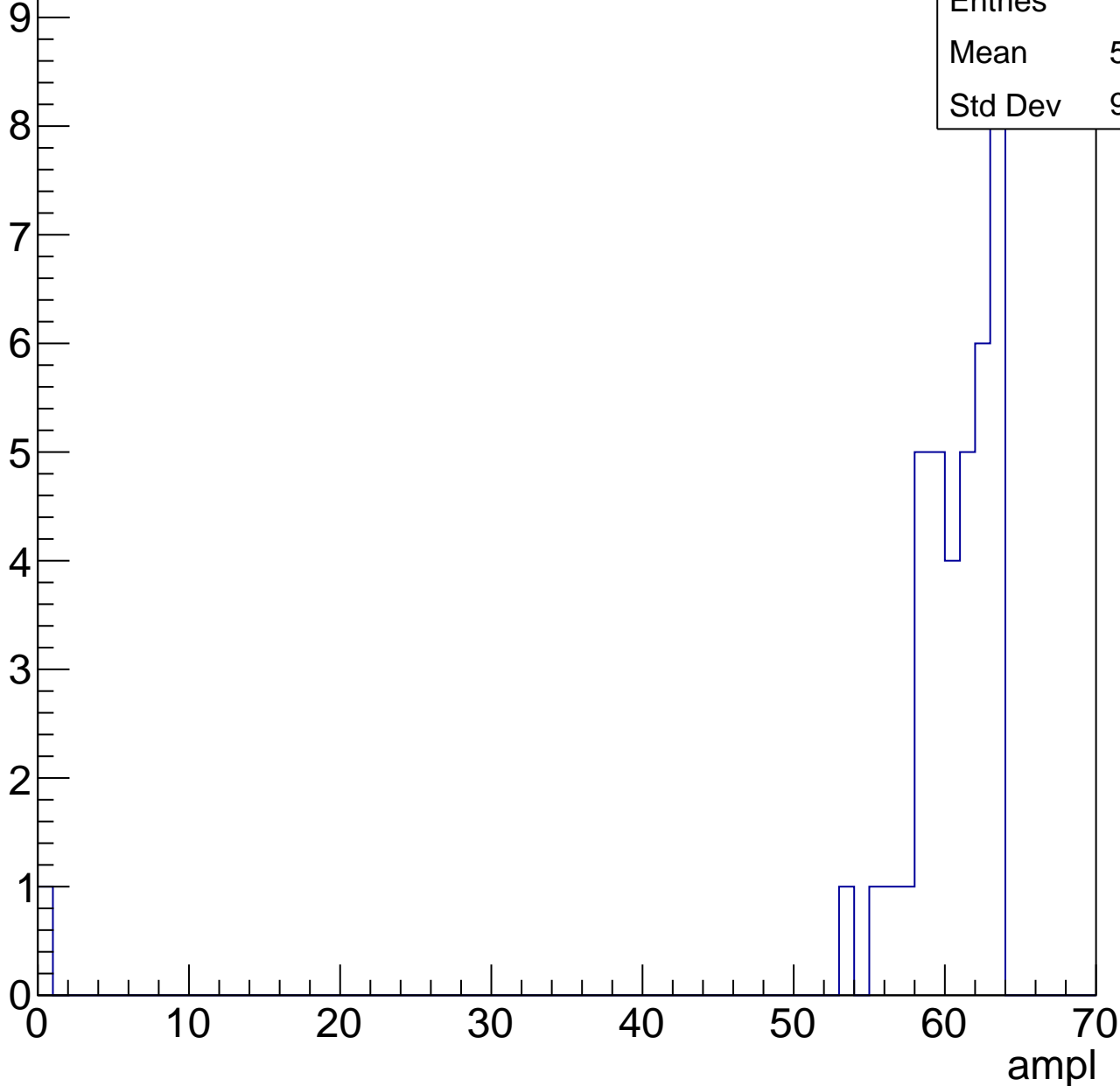


# B1L102S, U8-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

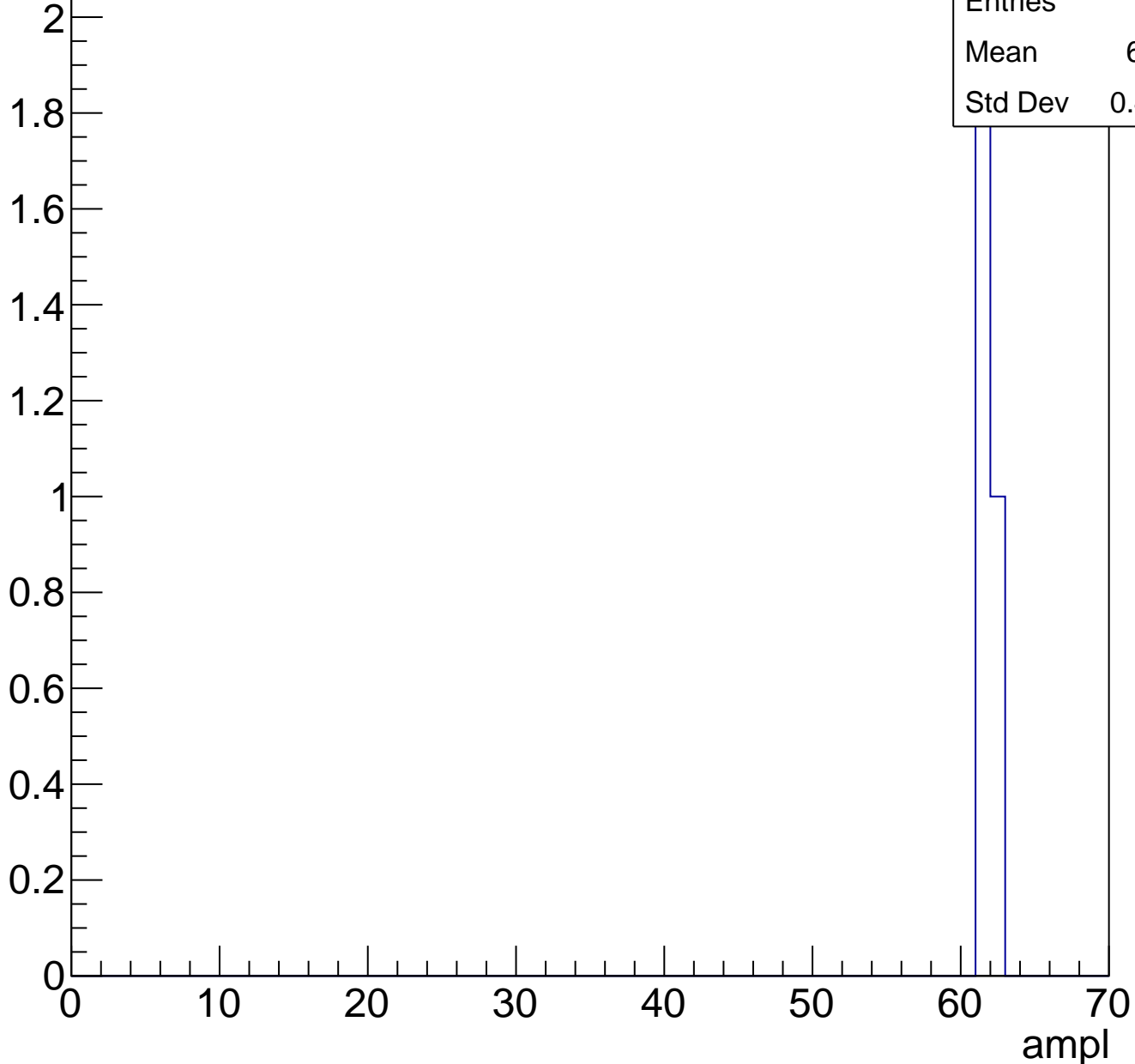
Entries	39
Mean	58.72
Std Dev	9.832



# B1L102S, U8-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U8-ch66, adc0

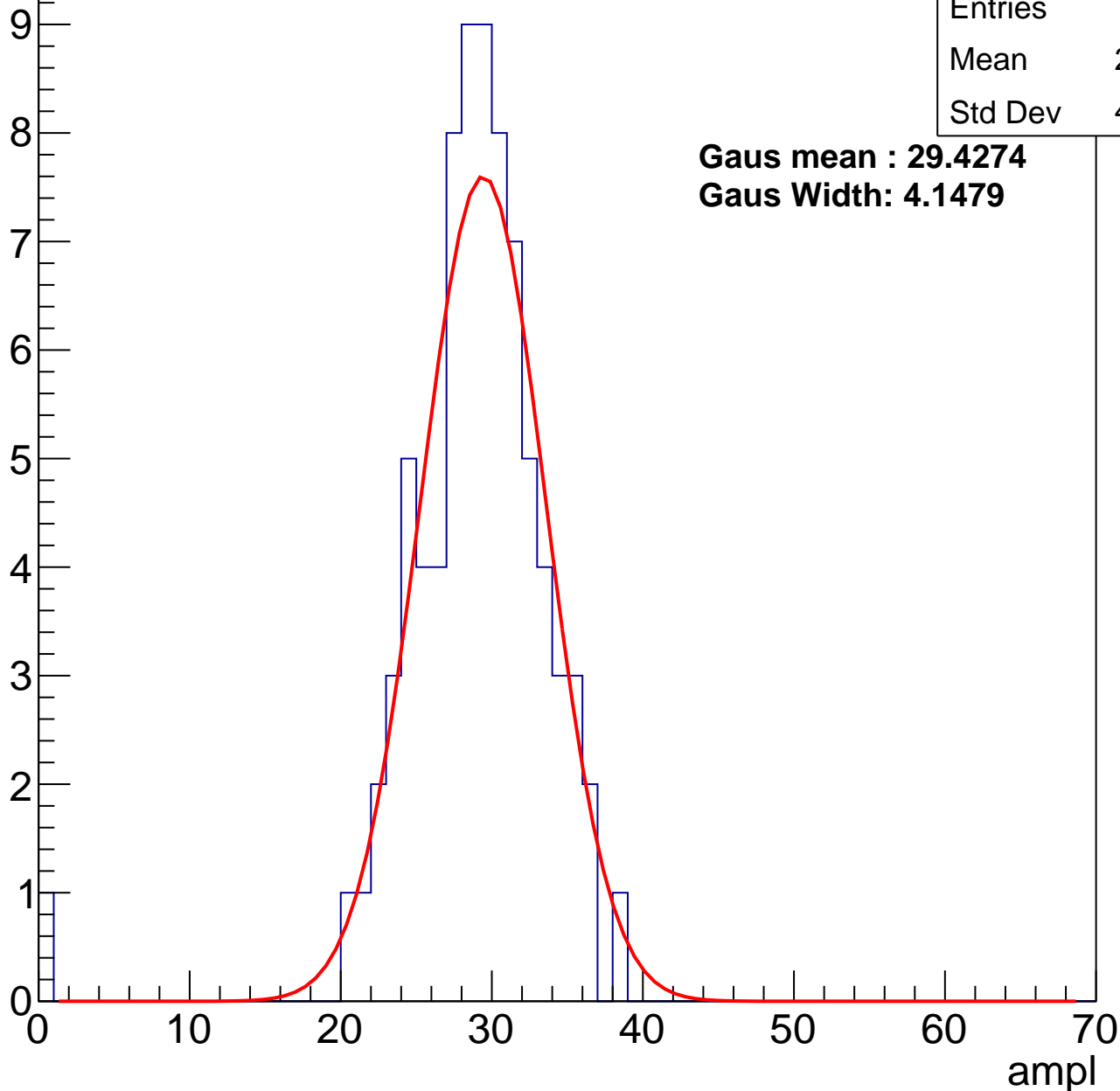
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	28.41
Std Dev	4.921

**Gaus mean : 29.4274**

**Gaus Width: 4.1479**



# B1L102S, U8-ch66, adc1

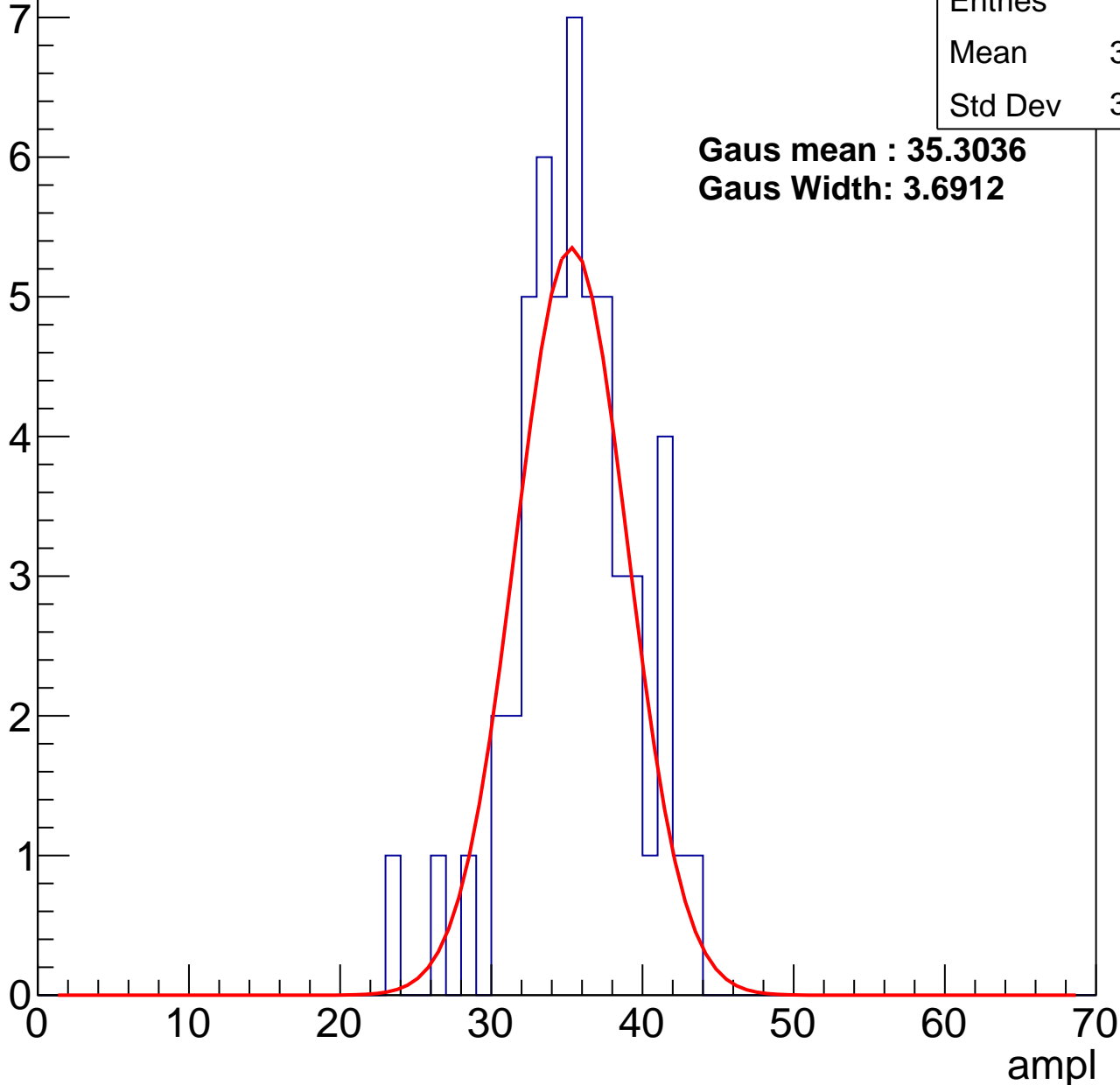
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	35.04
Std Dev	3.914

**Gaus mean : 35.3036**

**Gaus Width: 3.6912**



# B1L102S, U8-ch66, adc2

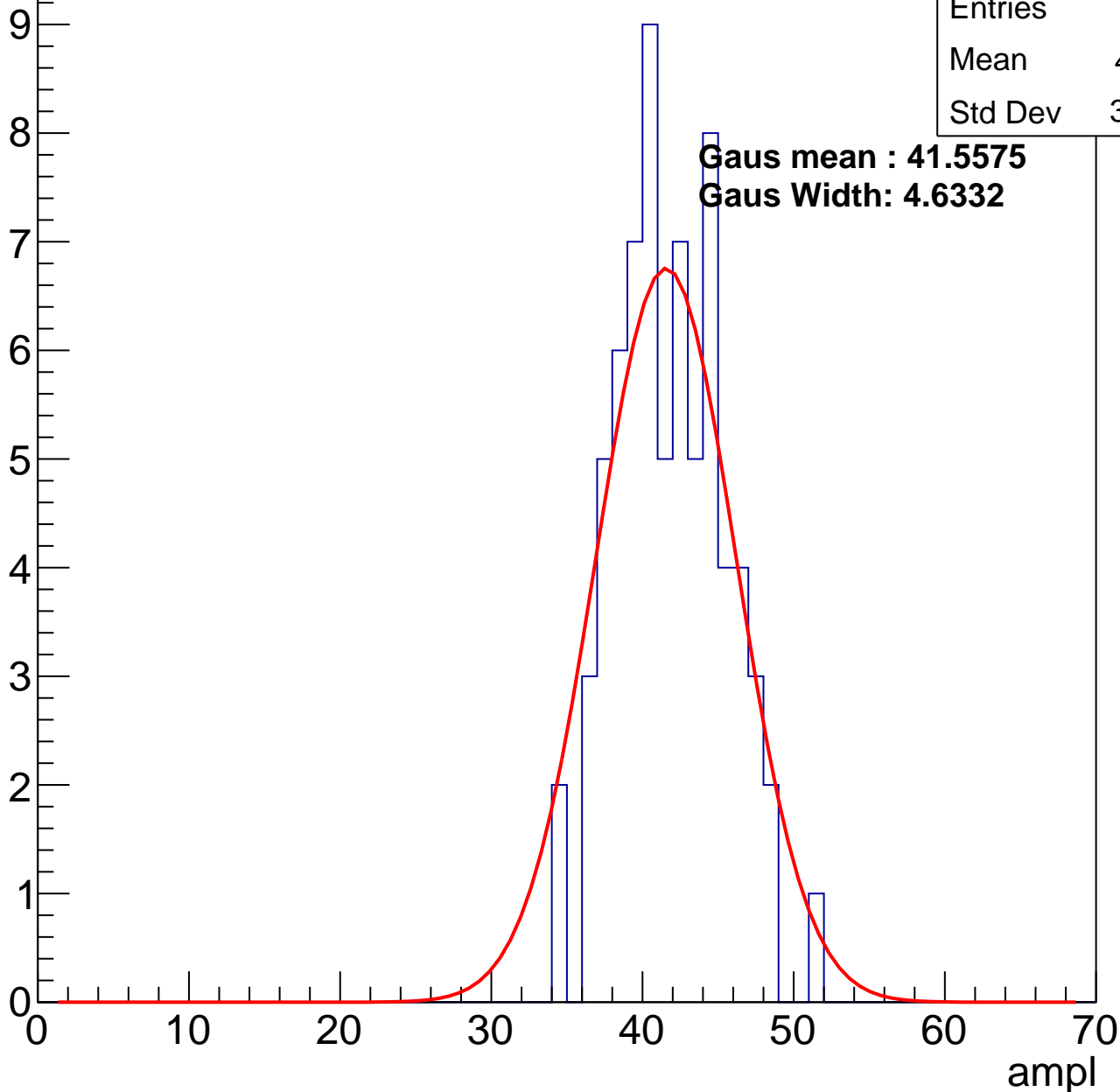
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	41.41
Std Dev	3.563

**Gaus mean : 41.5575**

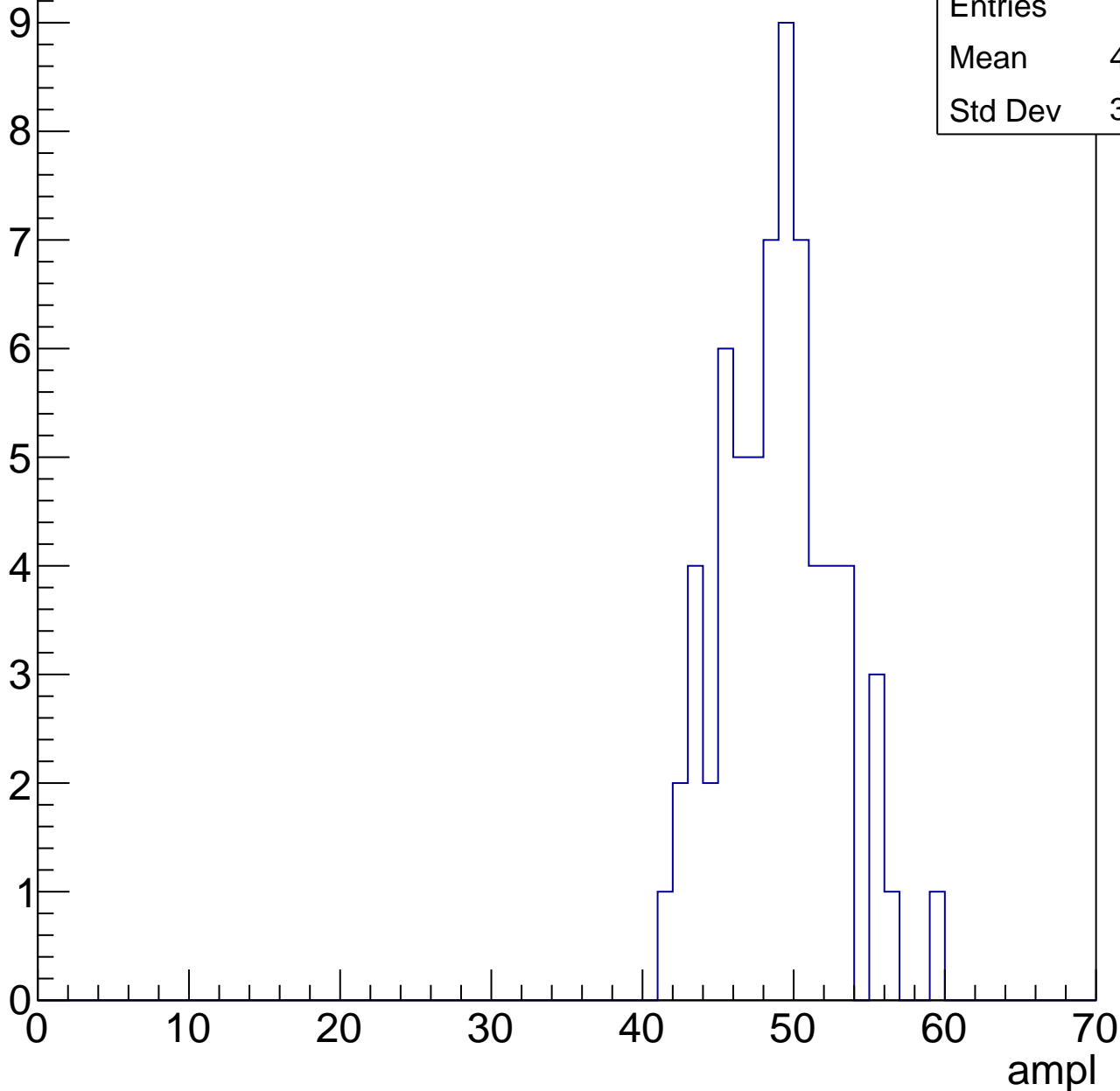
**Gaus Width: 4.6332**



# B1L102S, U8-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

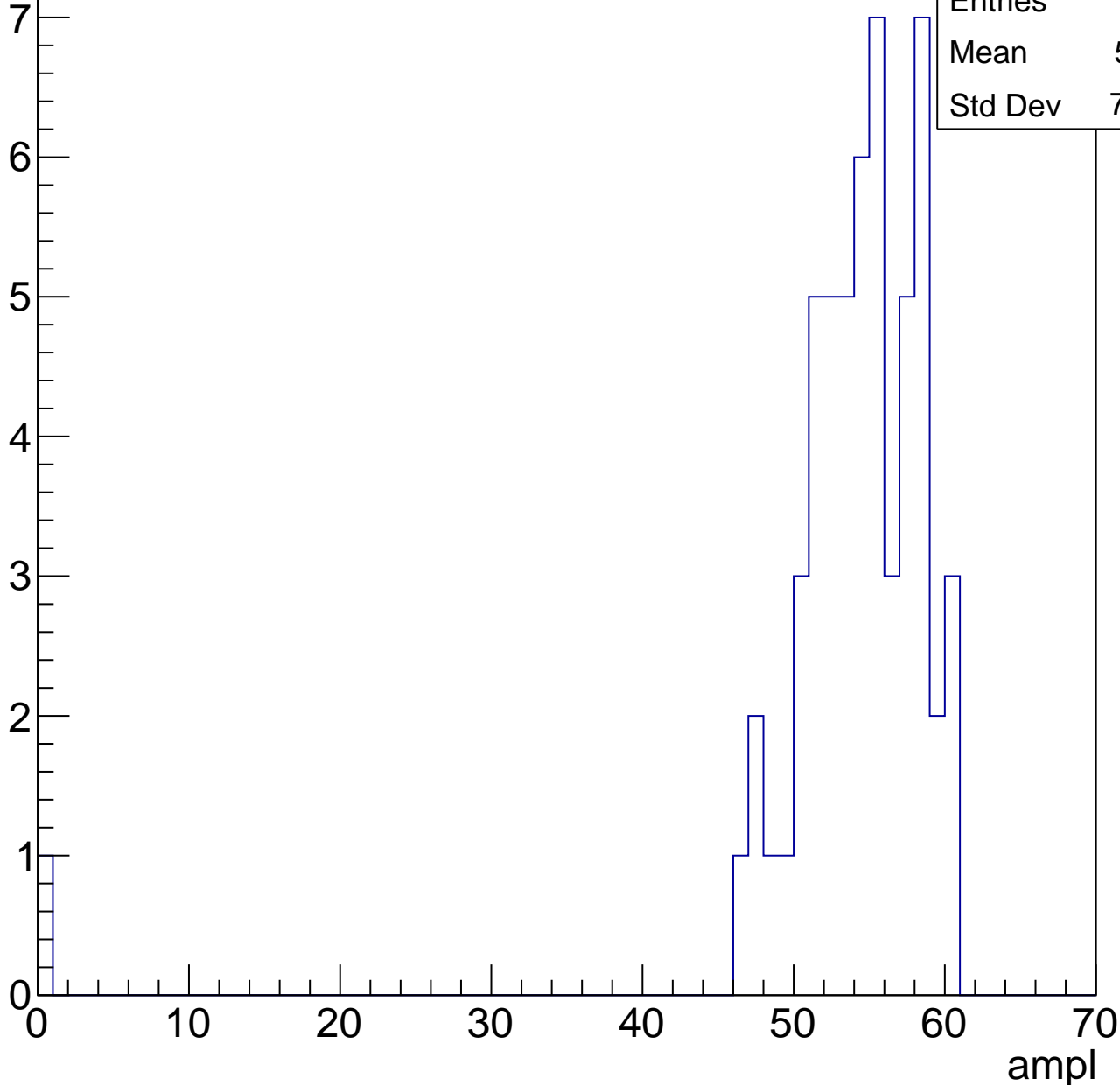


# B1L102S, U8-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	53.21
Std Dev	7.898

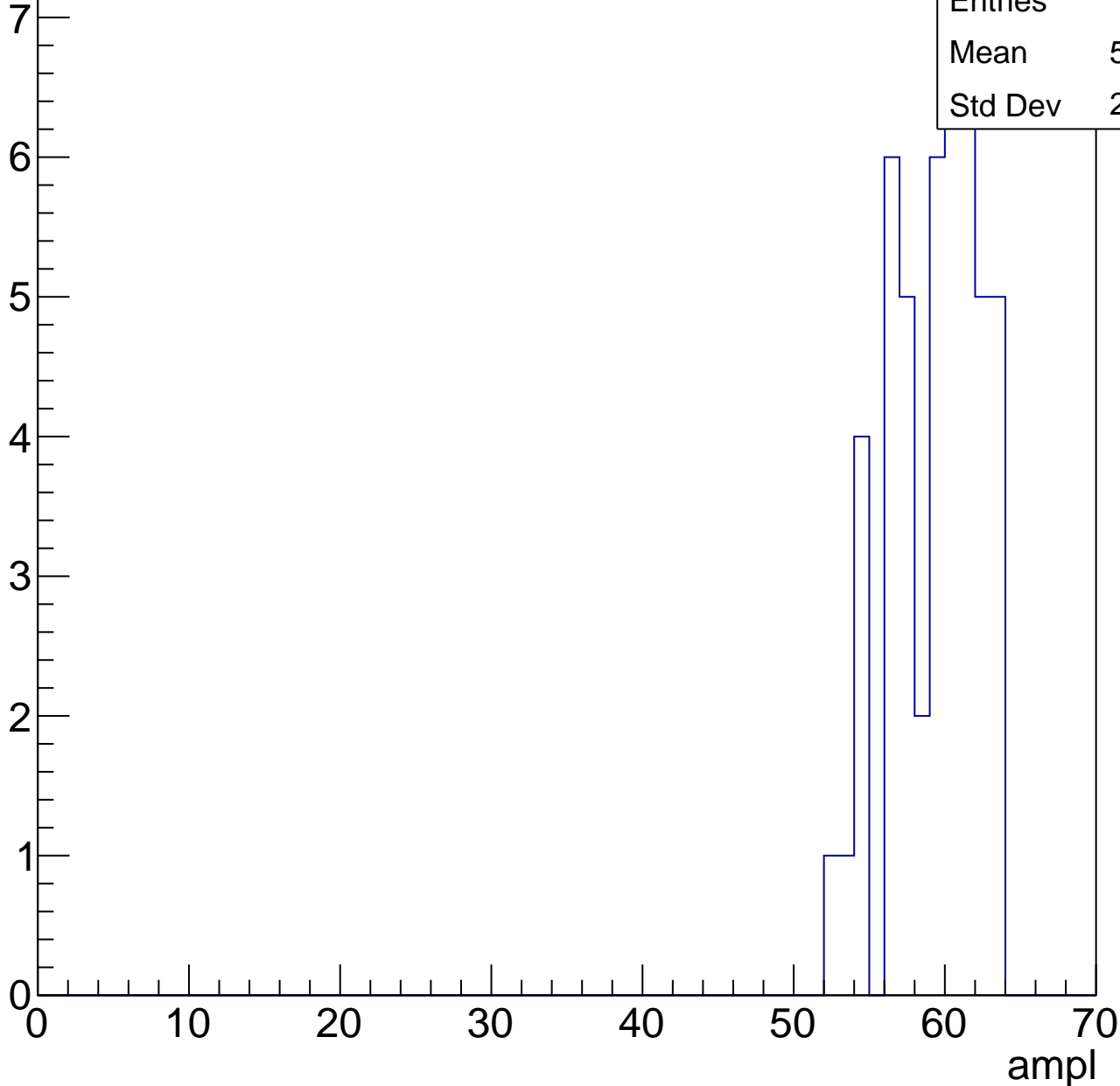


# B1L102S, U8-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	58.86
Std Dev	2.928

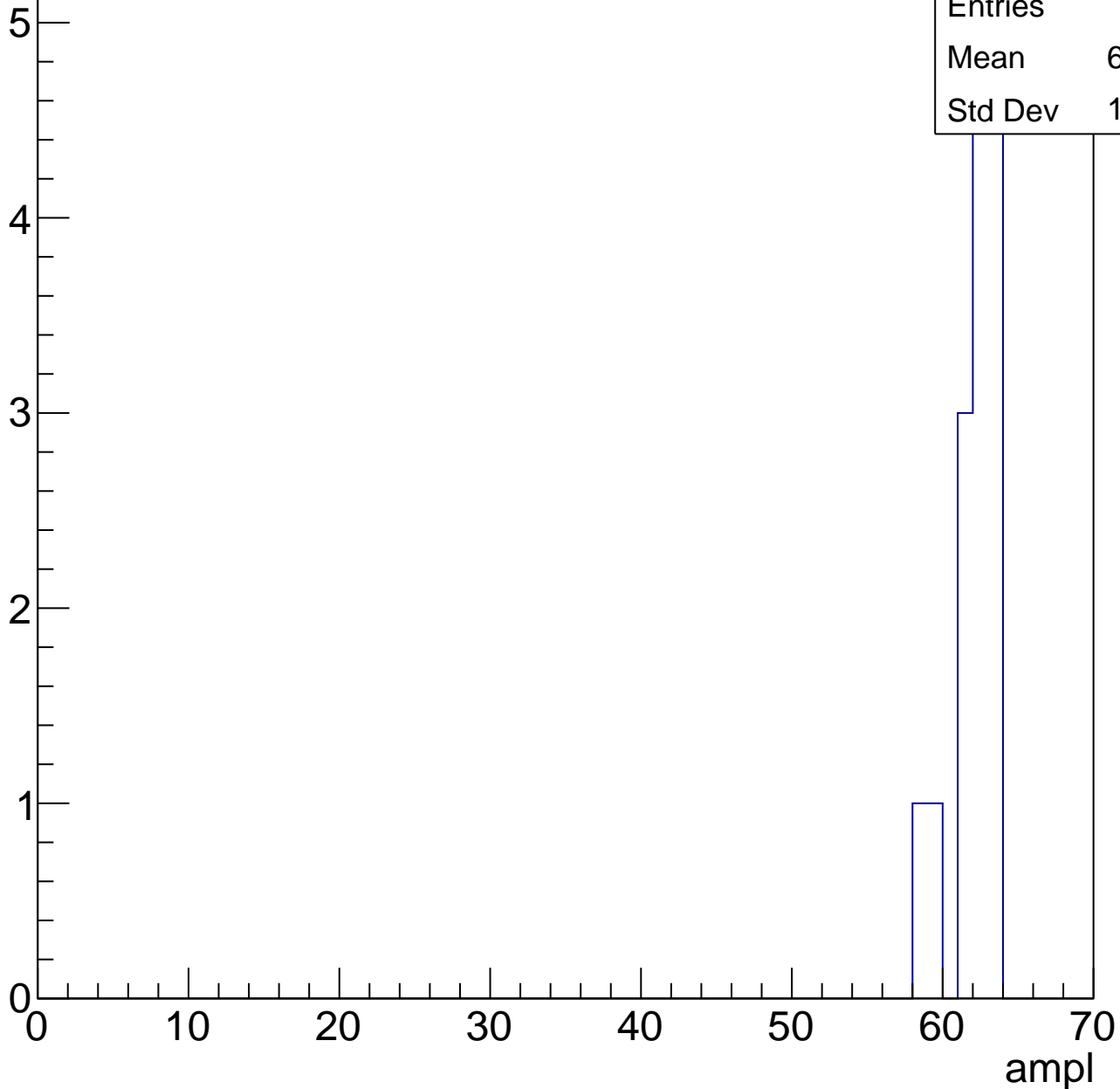


# B1L102S, U8-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	15
Mean	61.67
Std Dev	1.445





# B1L102S, U8-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U8-ch67, adc0

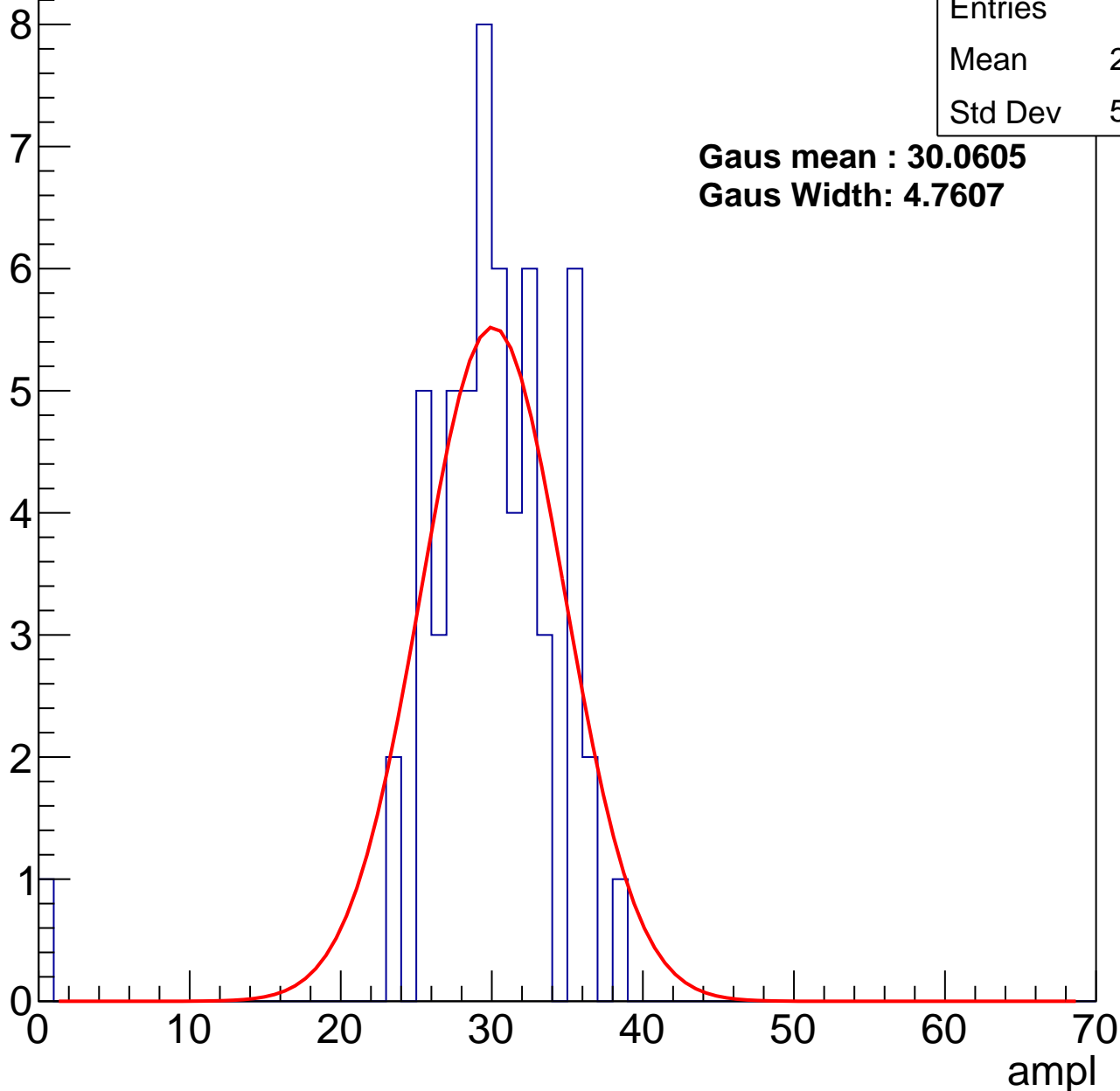
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	29.32
Std Dev	5.229

**Gaus mean : 30.0605**

**Gaus Width: 4.7607**



# B1L102S, U8-ch67, adc1

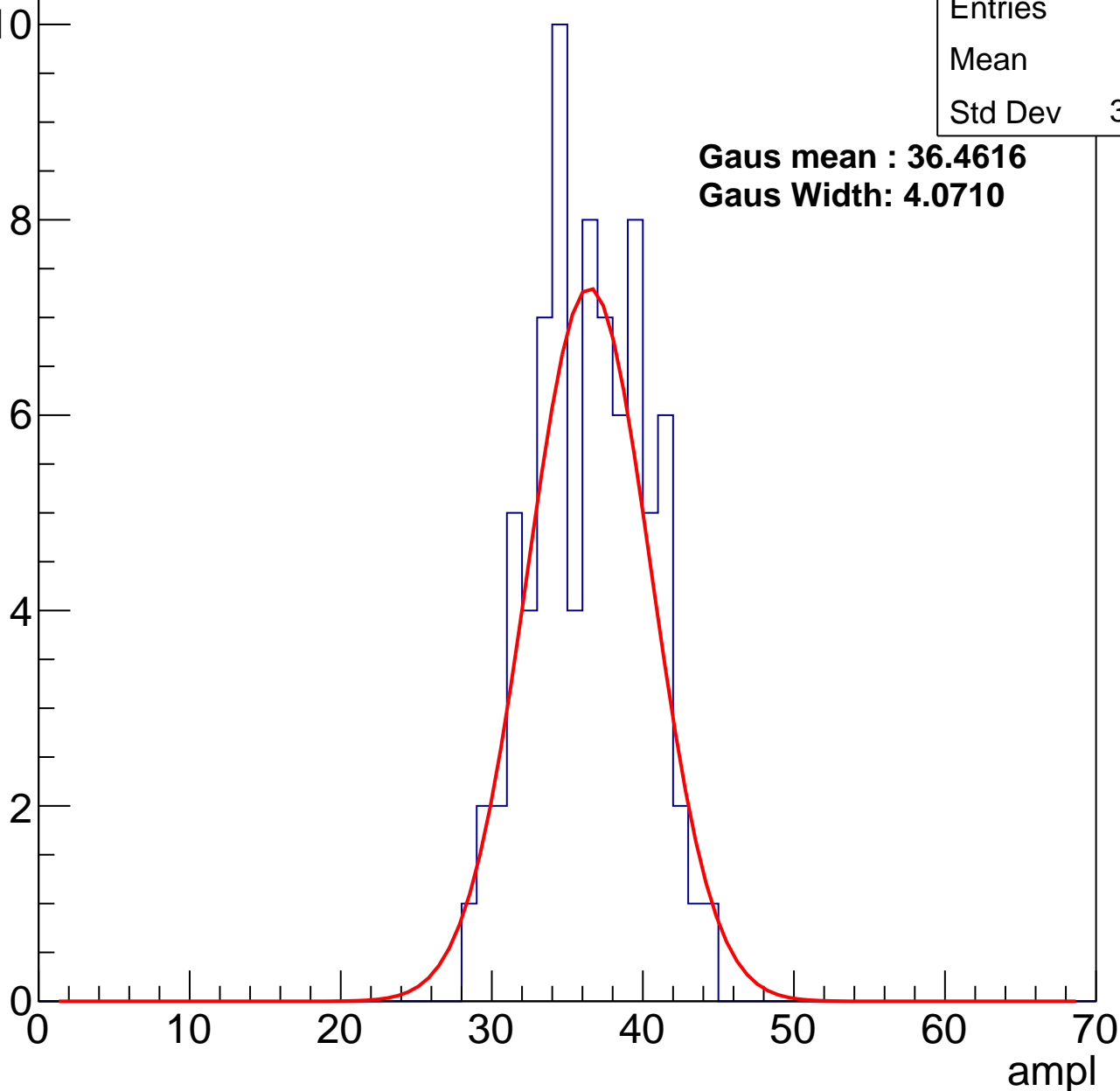
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	36
Std Dev	3.642

**Gaus mean : 36.4616**

**Gaus Width: 4.0710**



# B1L102S, U8-ch67, adc2

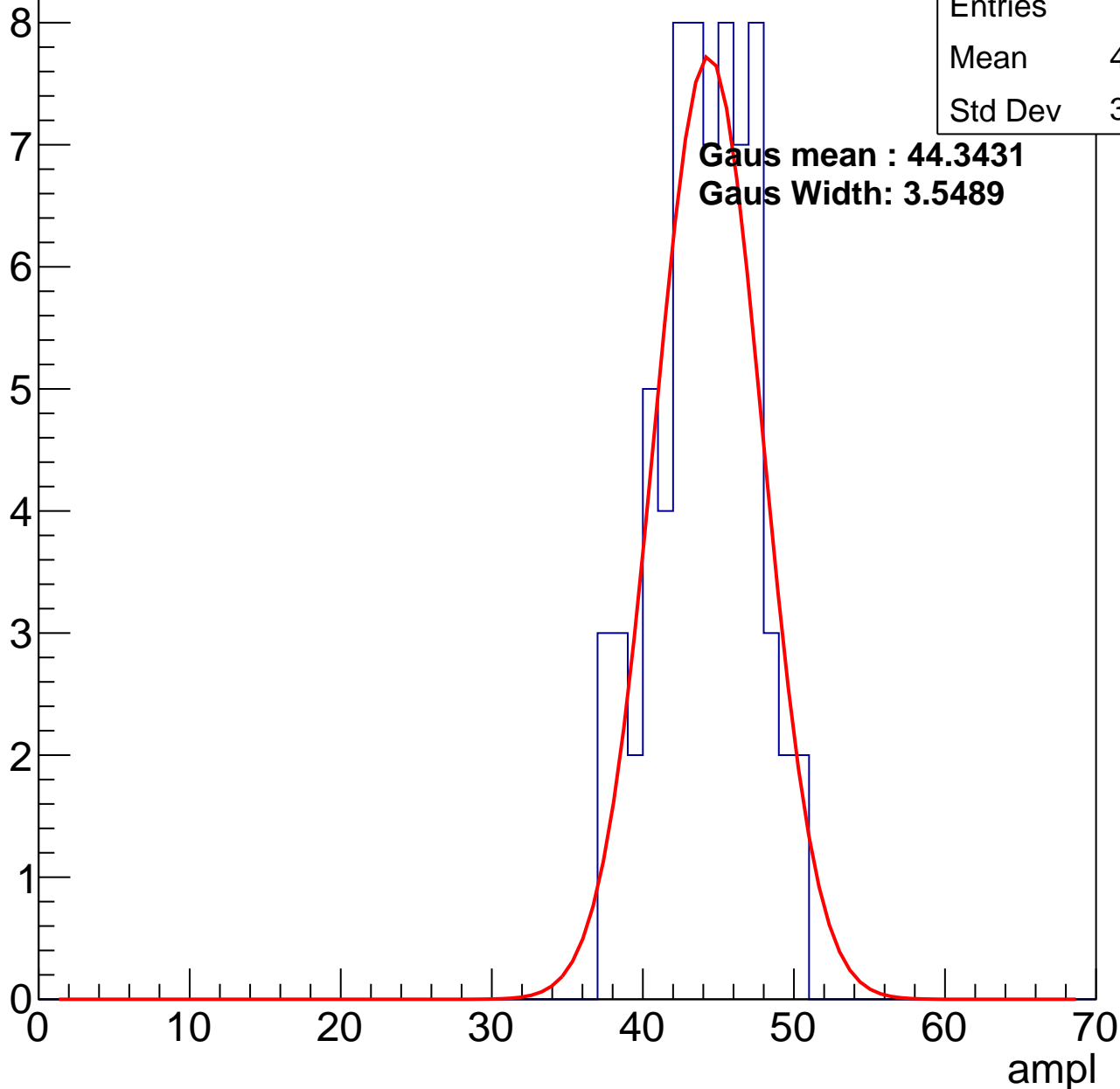
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	43.64
Std Dev	3.229

**Gaus mean : 44.3431**

**Gaus Width: 3.5489**

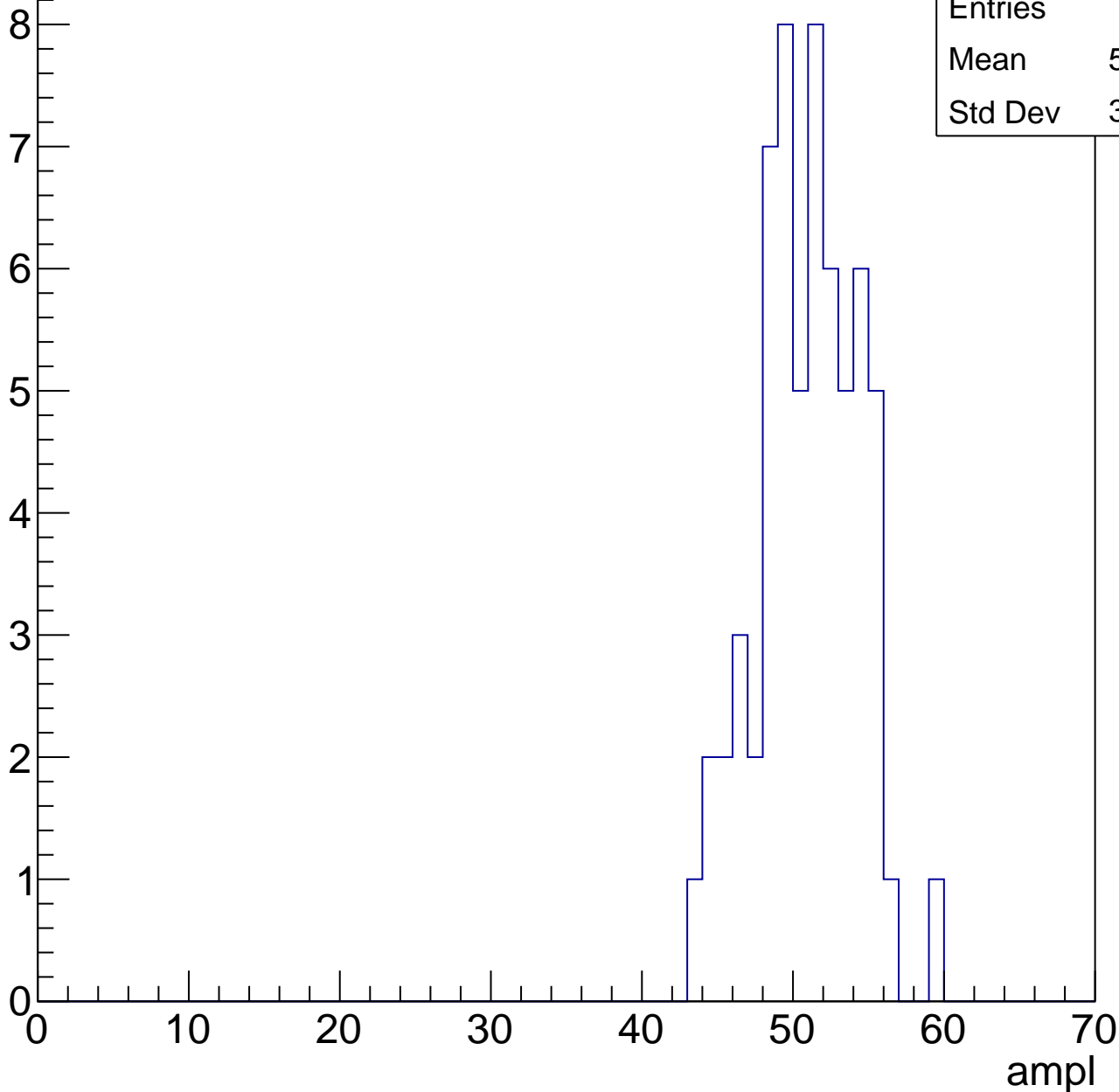


# B1L102S, U8-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

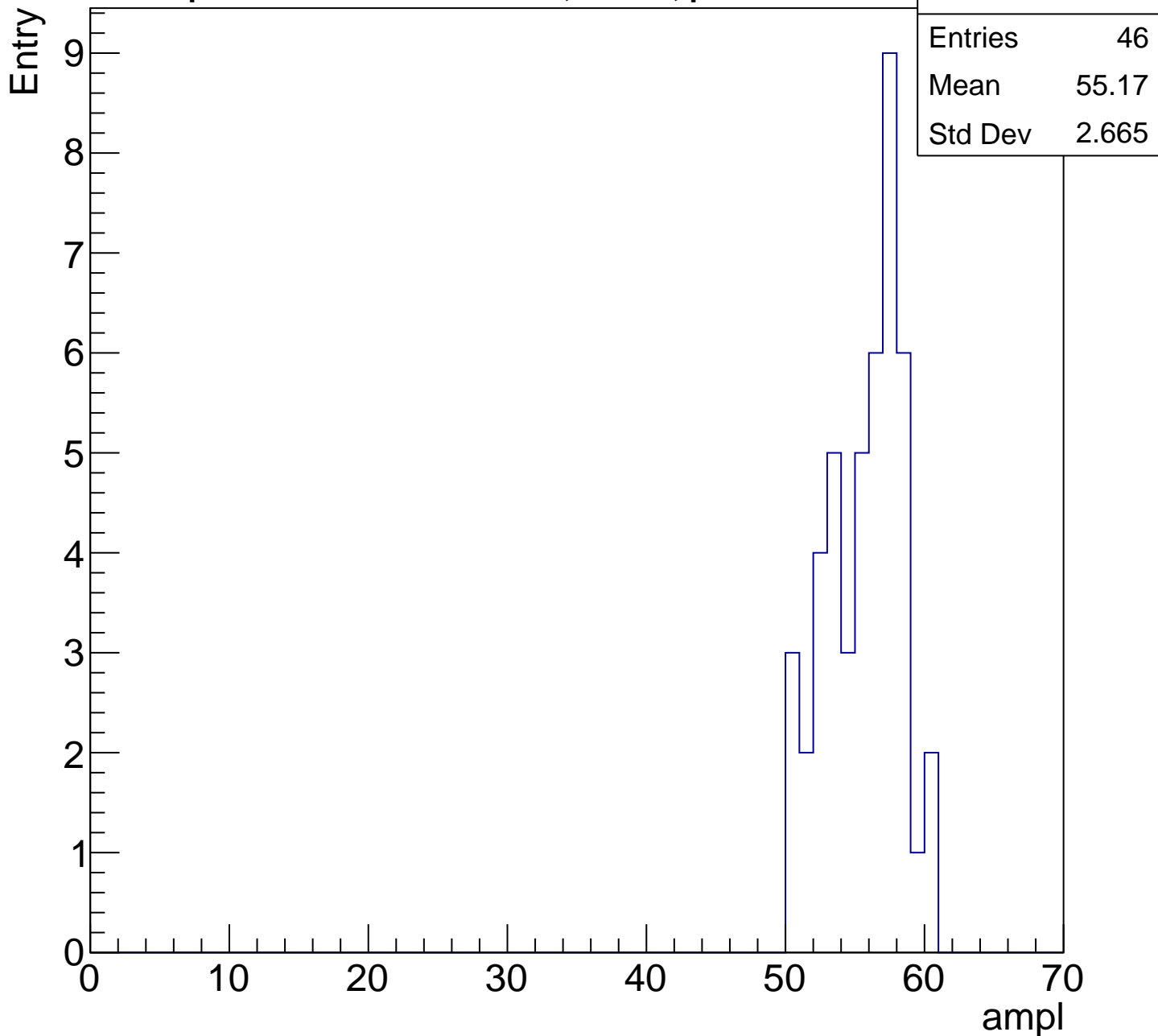
Entry

Entries	62
Mean	50.48
Std Dev	3.296



# B1L102S, U8-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

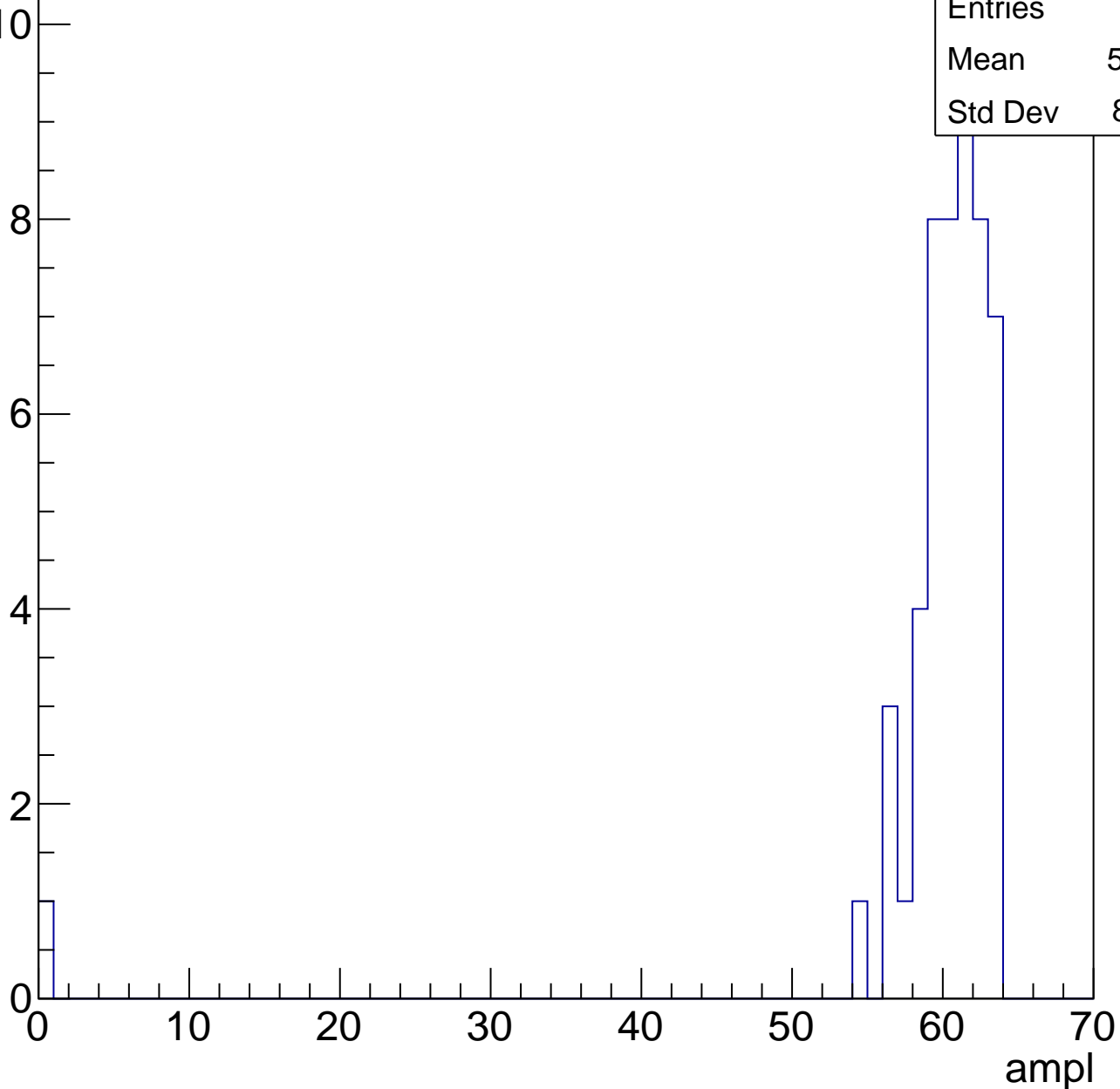


# B1L102S, U8-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	59.02
Std Dev	8.601



# B1L102S, U8-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch68, adc0

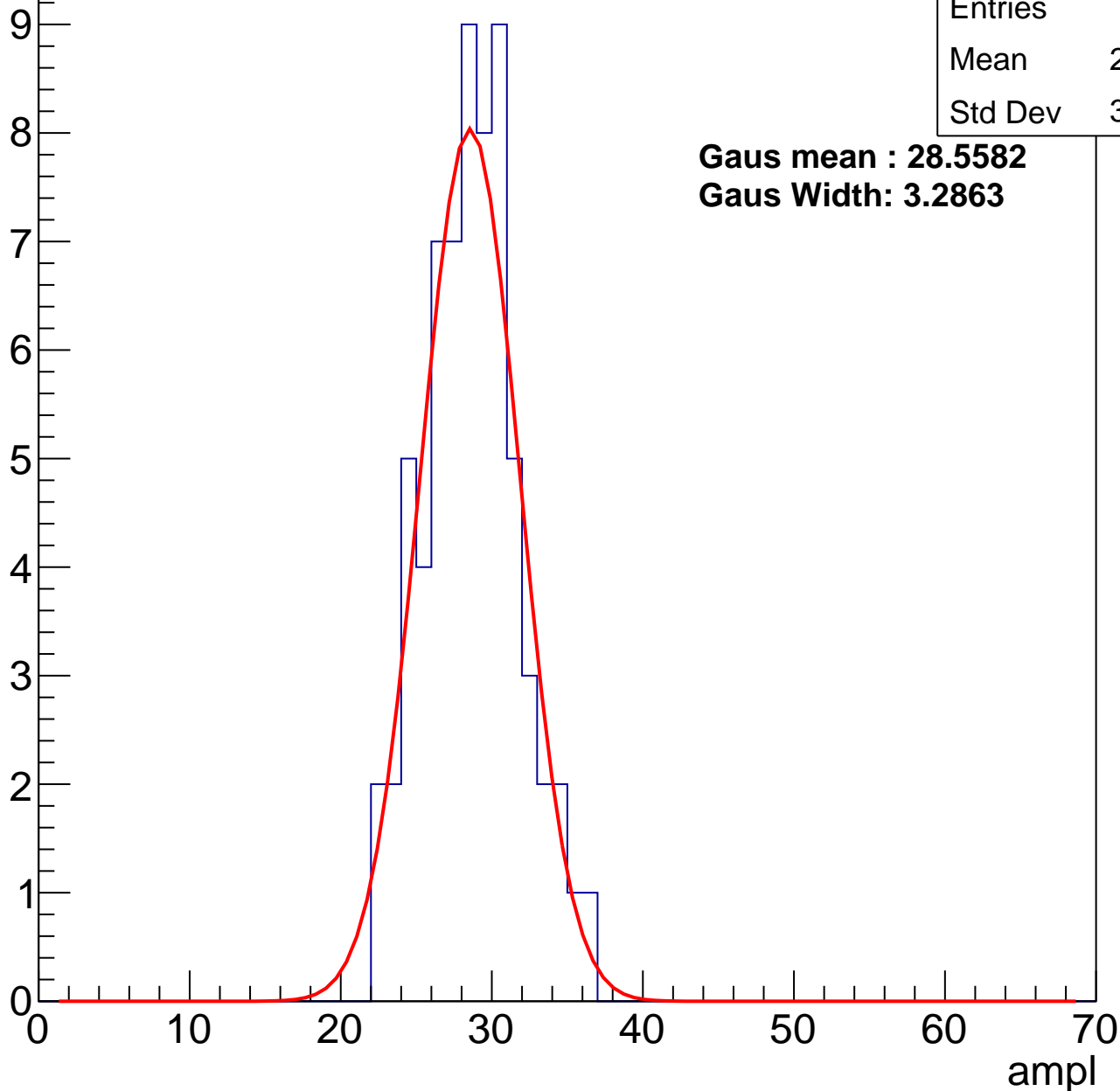
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	28.22
Std Dev	3.095

**Gaus mean : 28.5582**

**Gaus Width: 3.2863**



# B1L102S, U8-ch68, adc1

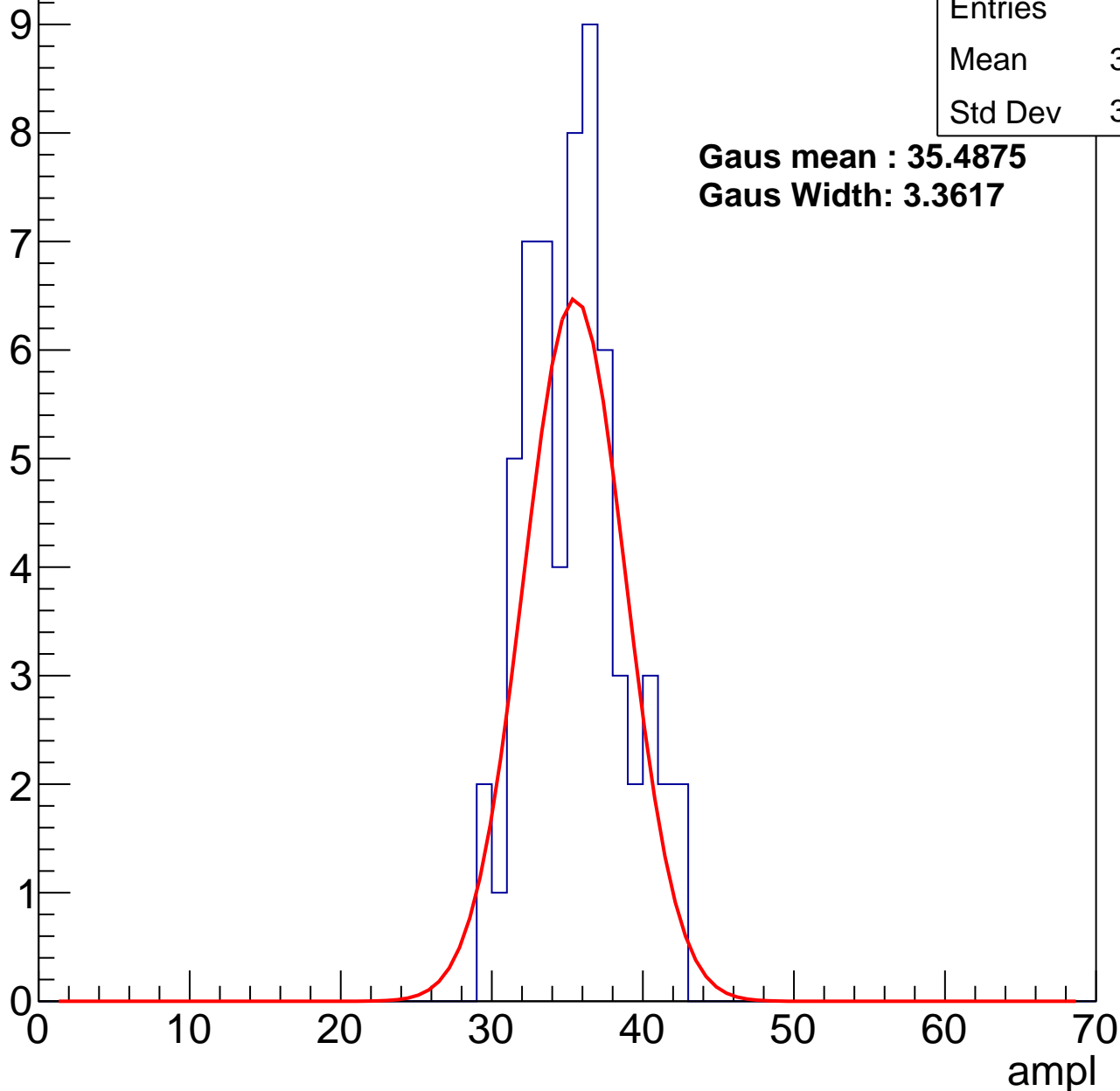
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	35.05
Std Dev	3.159

**Gaus mean : 35.4875**

**Gaus Width: 3.3617**



# B1L102S, U8-ch68, adc2

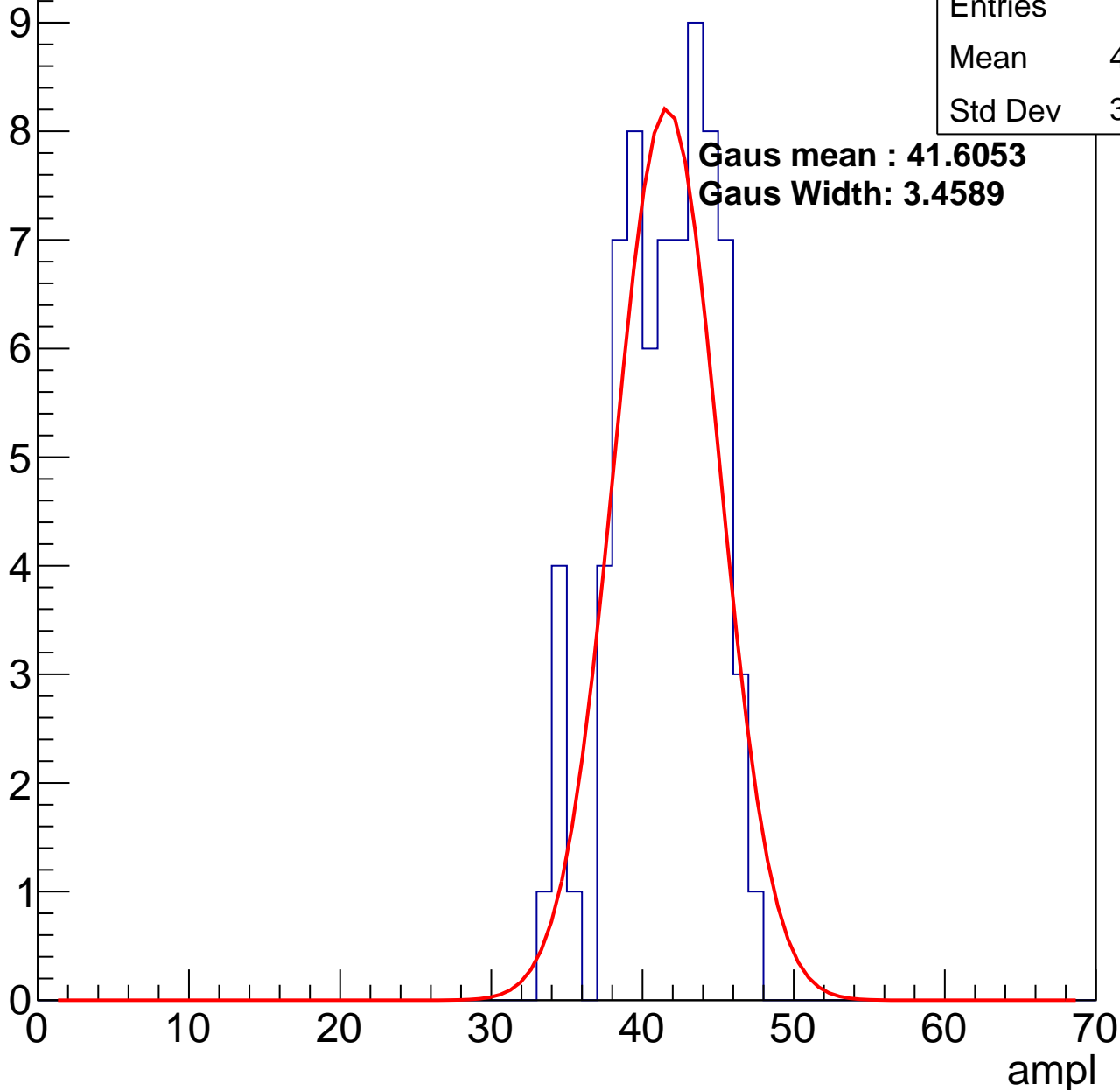
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	40.96
Std Dev	3.308

**Gaus mean : 41.6053**

**Gaus Width: 3.4589**

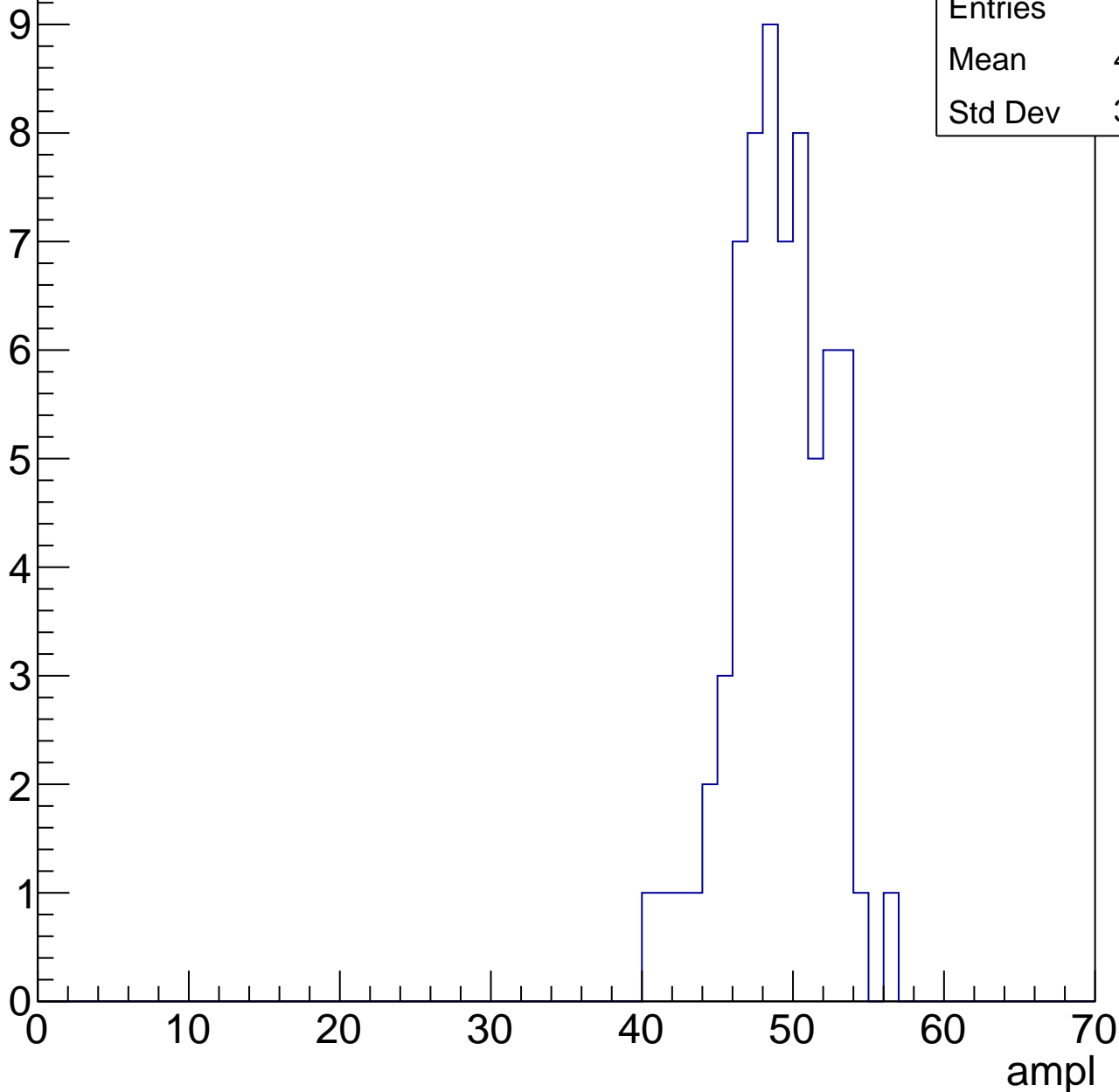


# B1L102S, U8-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

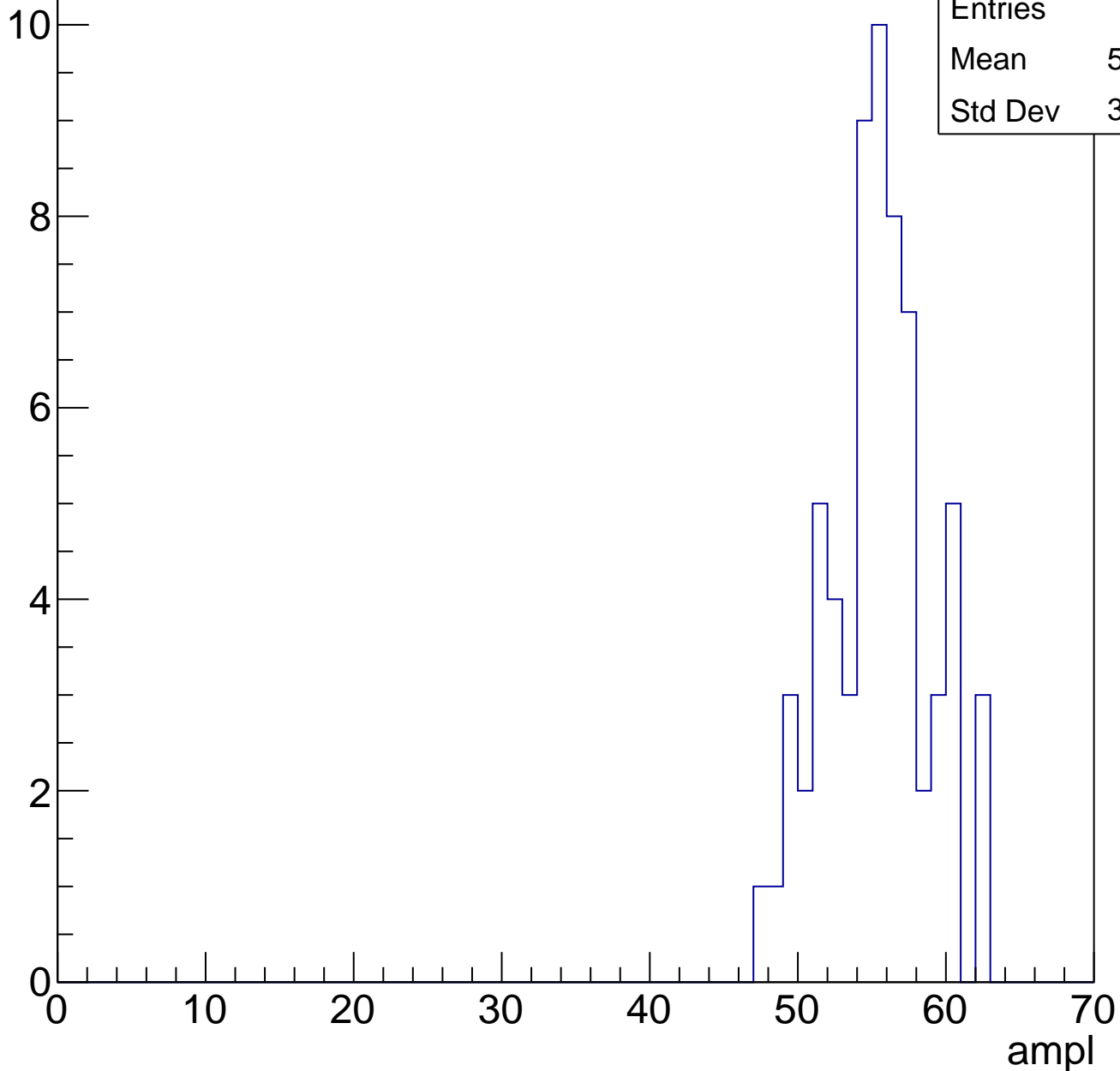
Entries	67
Mean	48.61
Std Dev	3.171



# B1L102S, U8-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

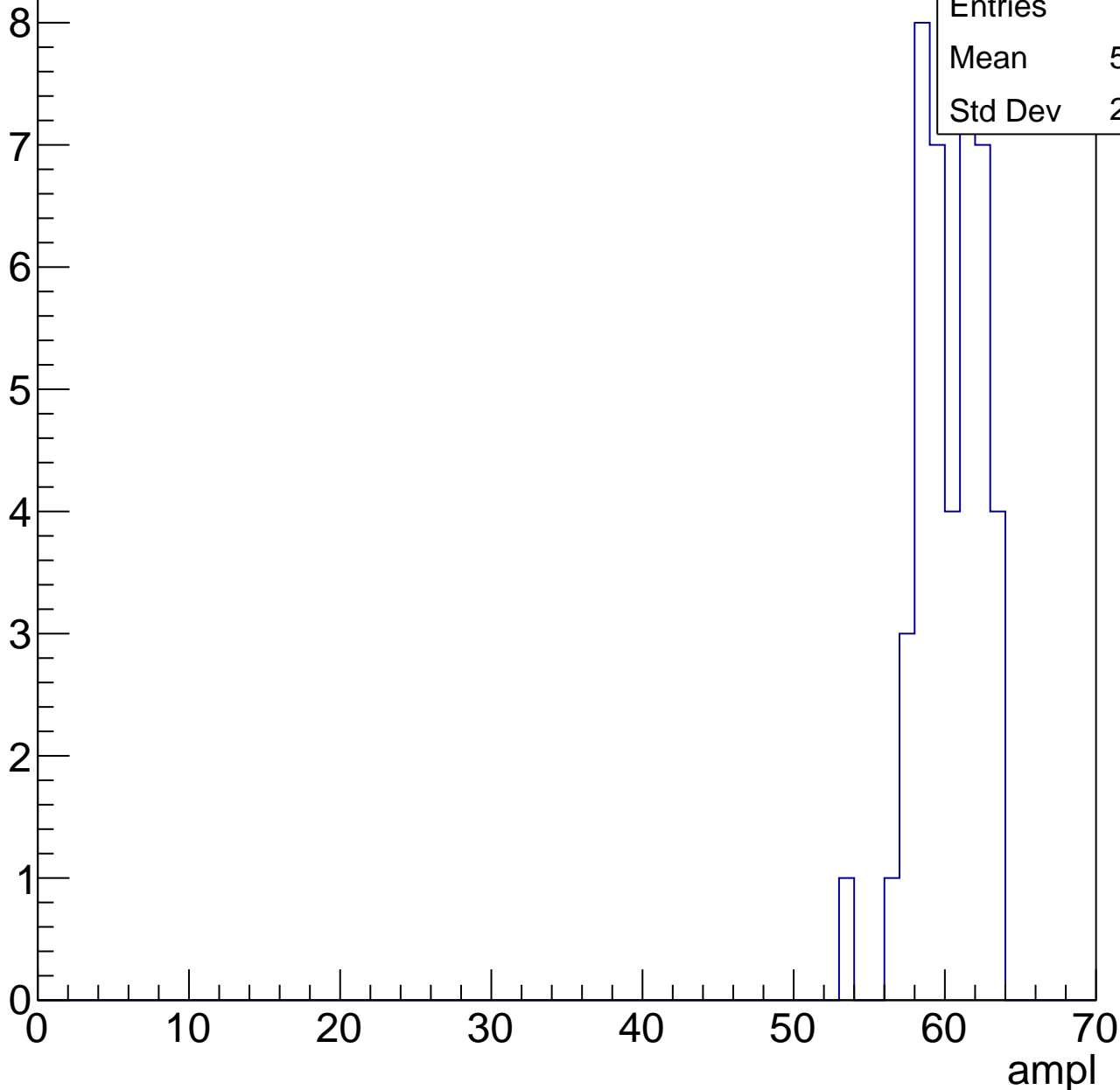


# B1L102S, U8-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	43
Mean	59.79
Std Dev	2.163

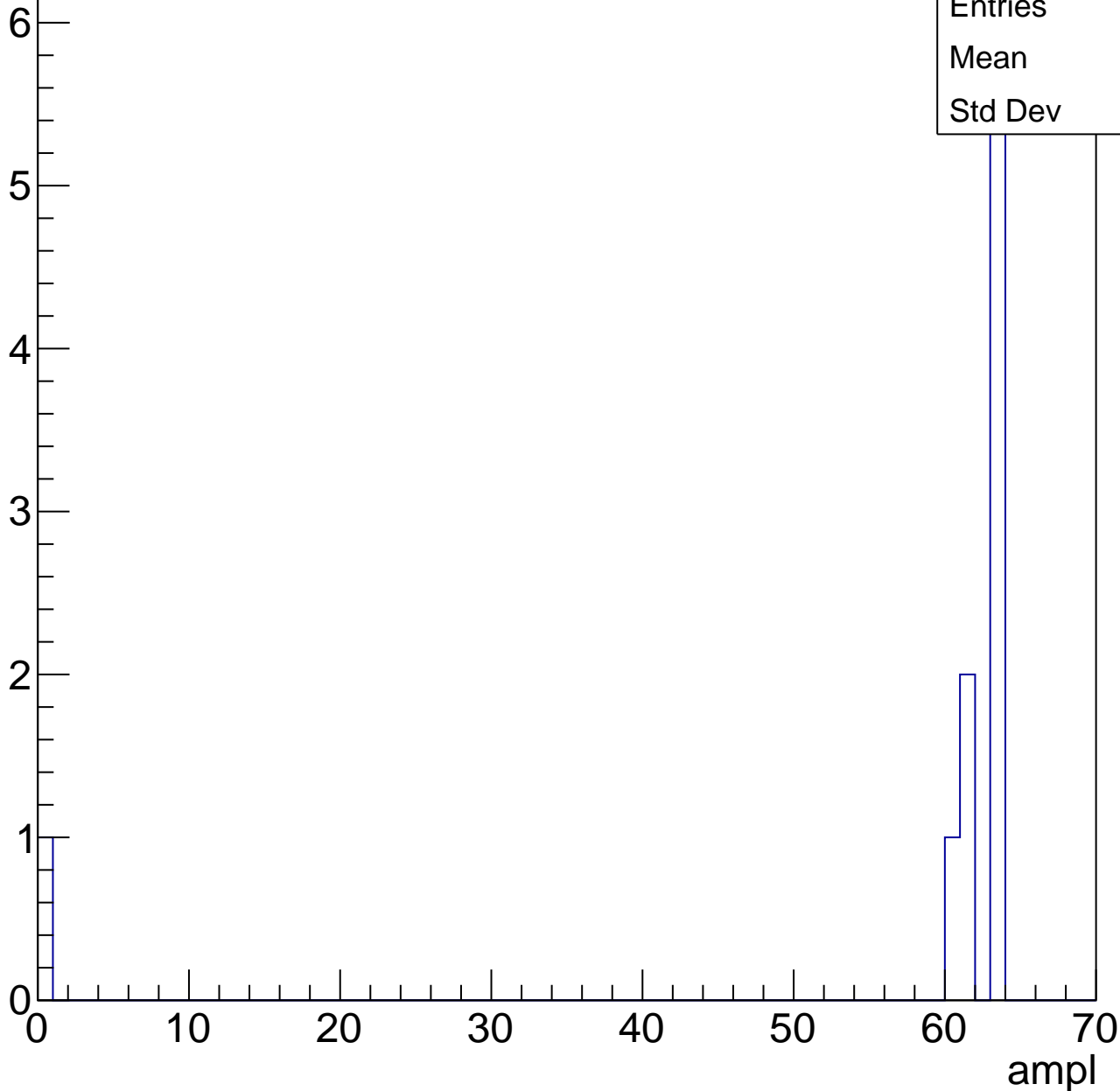


# B1L102S, U8-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	10
Mean	56
Std Dev	18.7





# B1L102S, U8-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch69, adc0

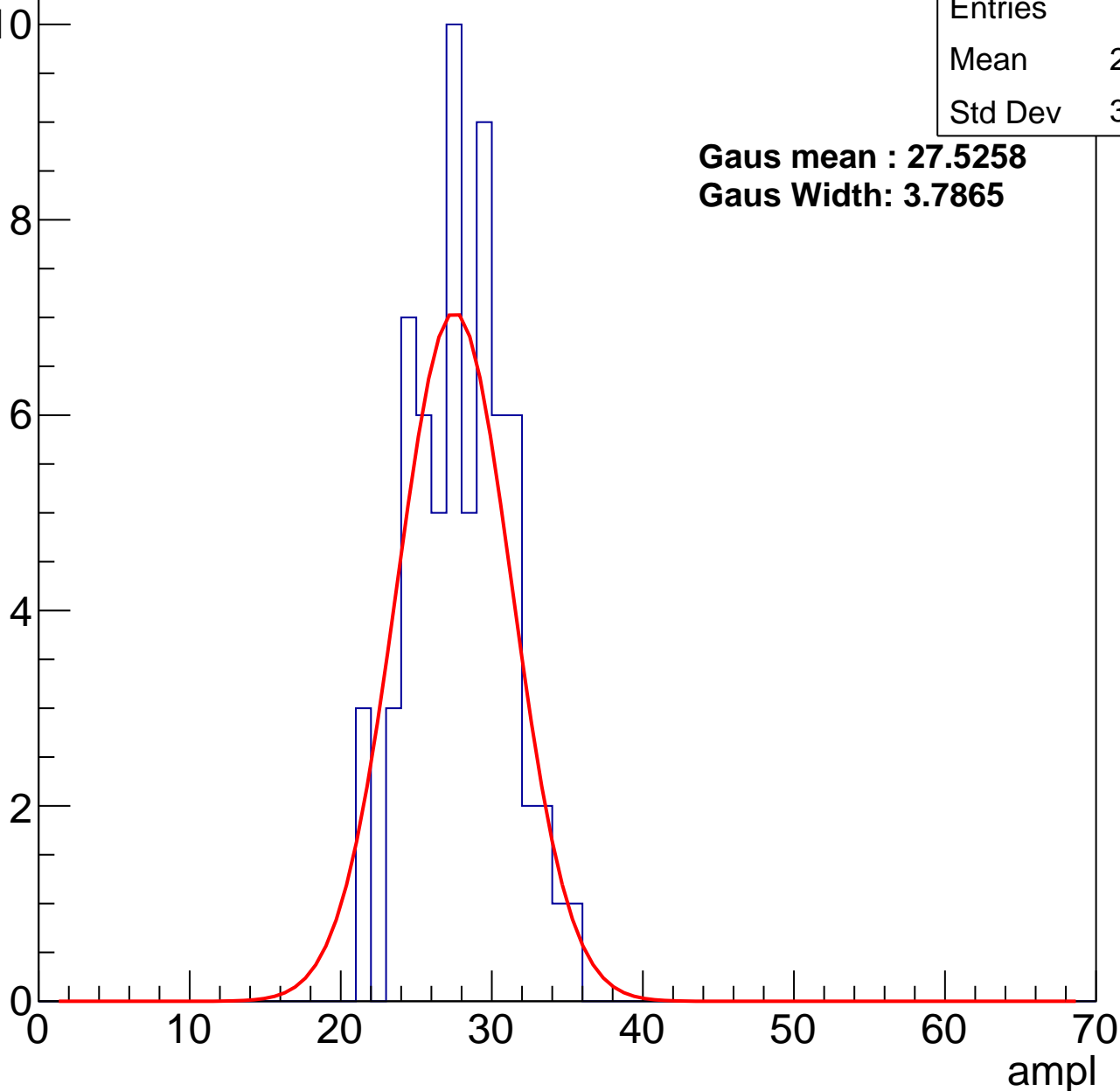
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	27.52
Std Dev	3.154

**Gaus mean : 27.5258**

**Gaus Width: 3.7865**



# B1L102S, U8-ch69, adc1

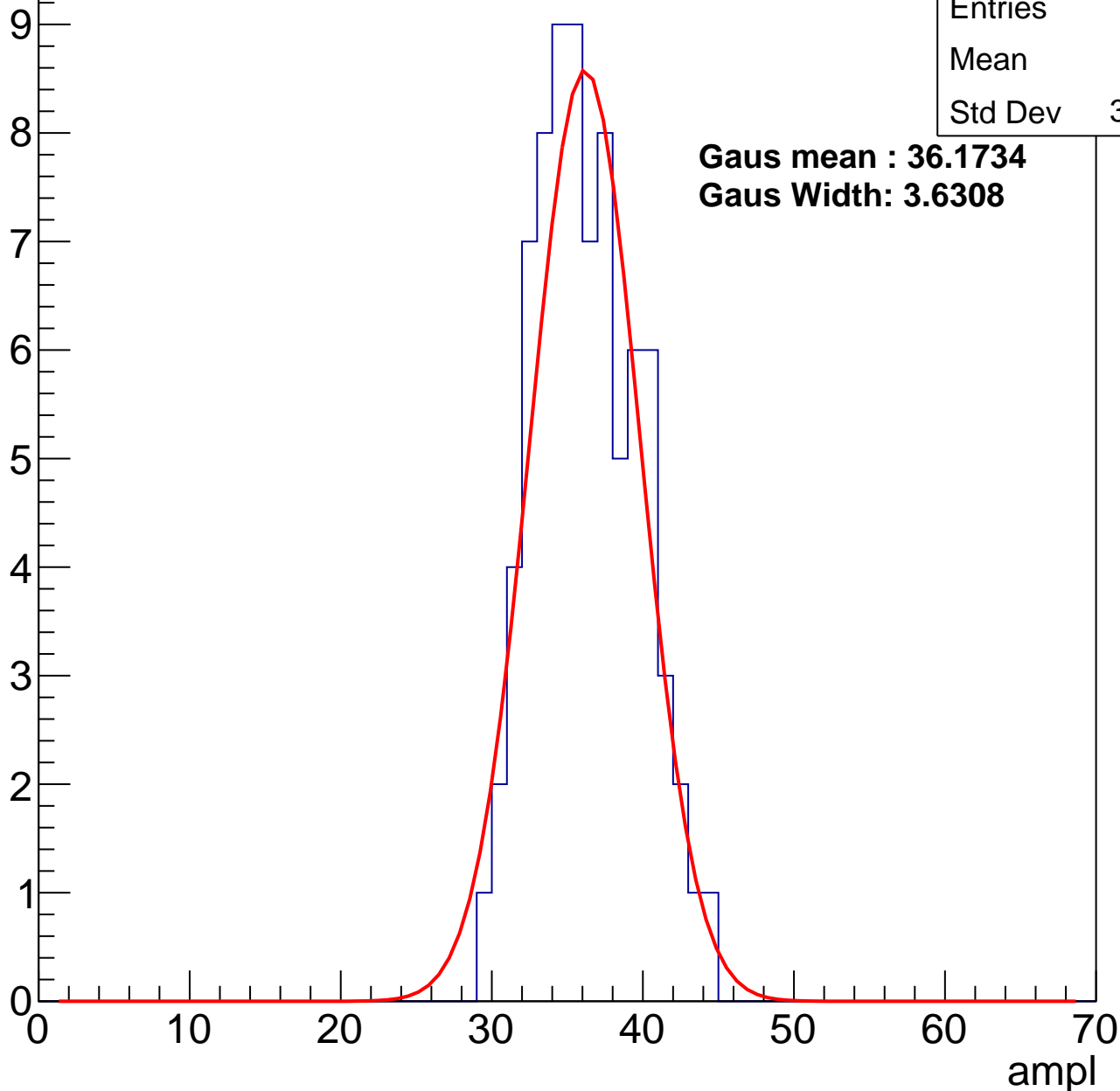
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	35.8
Std Dev	3.347

**Gaus mean : 36.1734**

**Gaus Width: 3.6308**



# B1L102S, U8-ch69, adc2

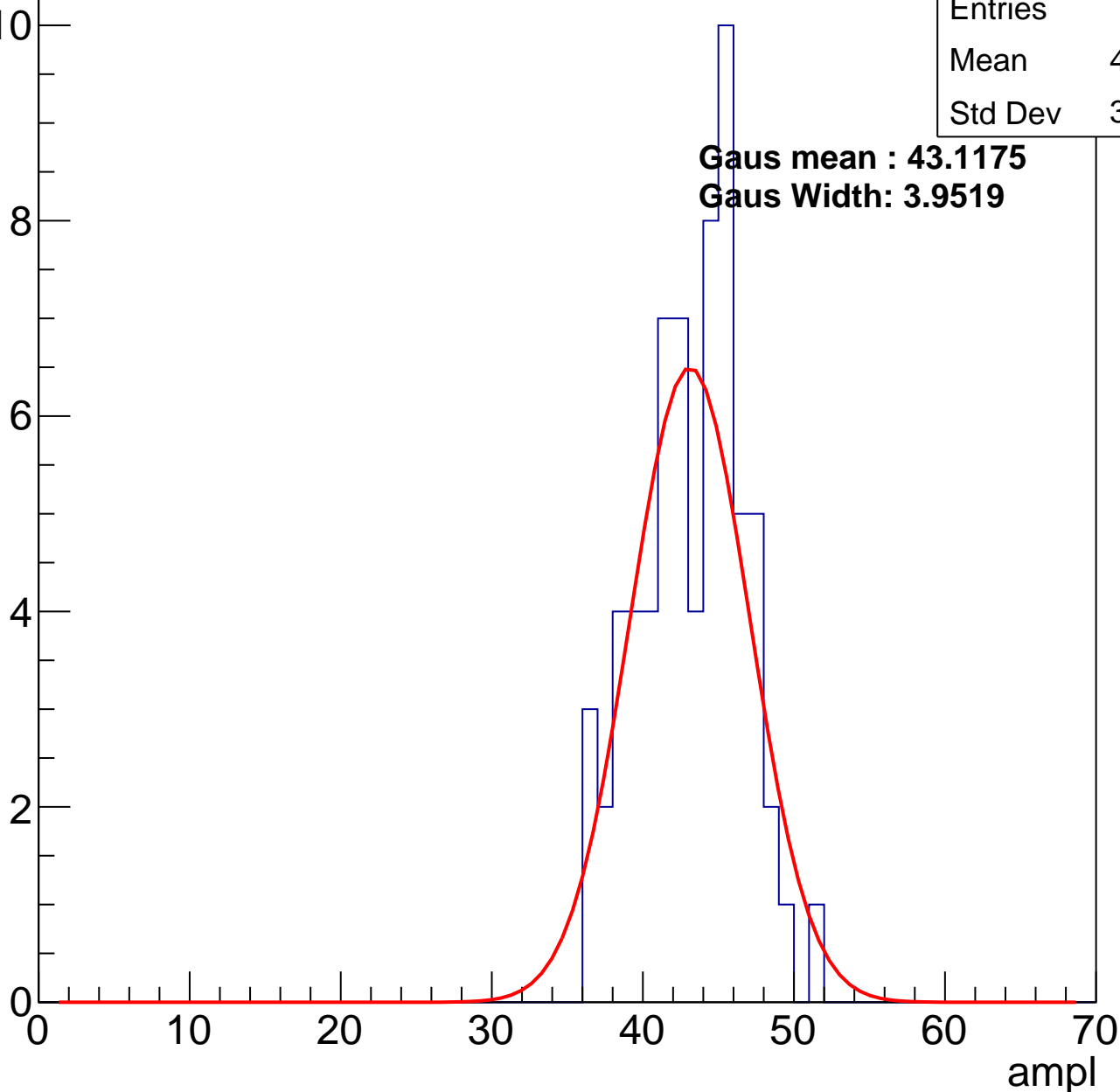
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	42.78
Std Dev	3.398

**Gaus mean : 43.1175**

**Gaus Width: 3.9519**

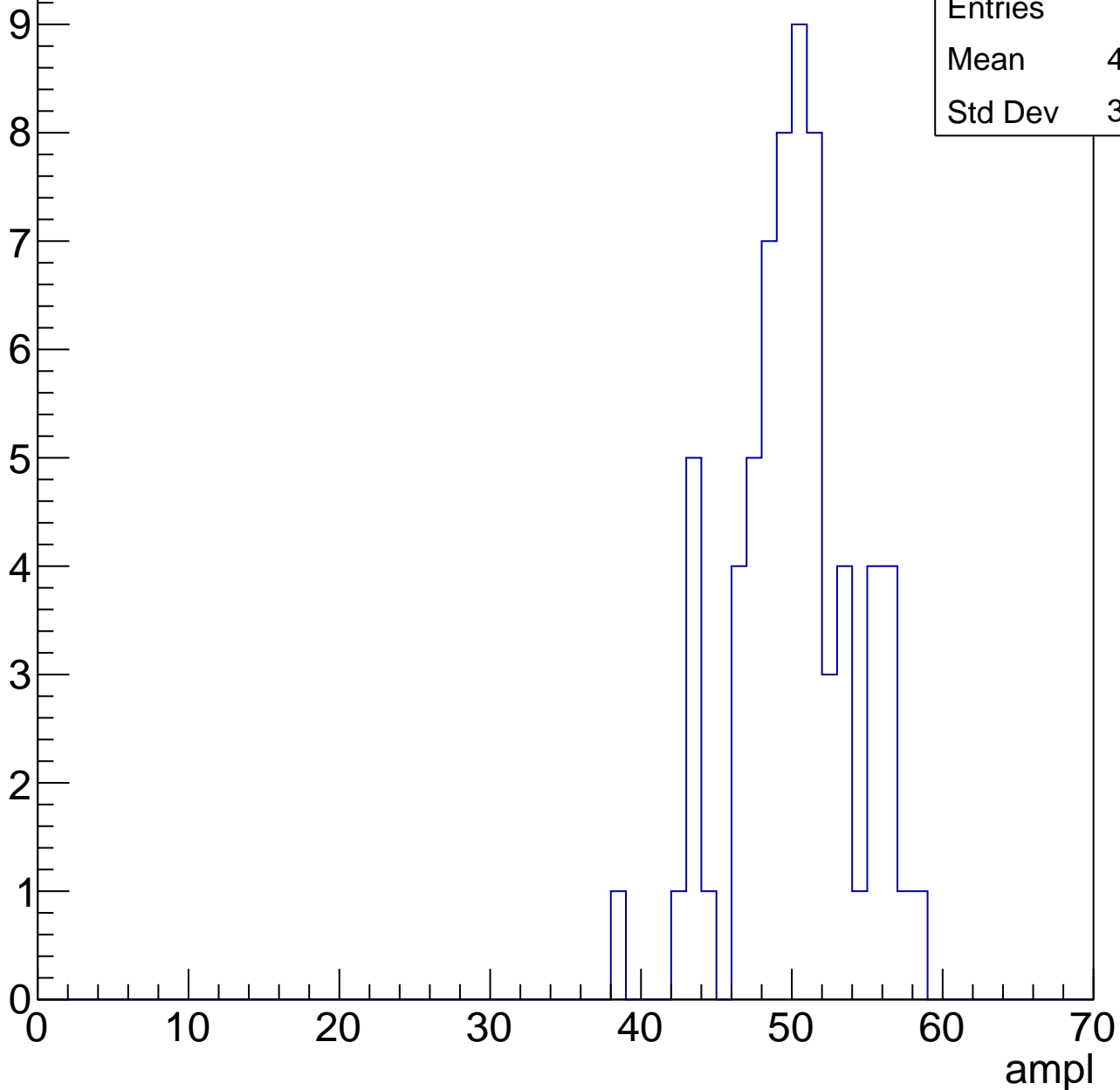


# B1L102S, U8-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

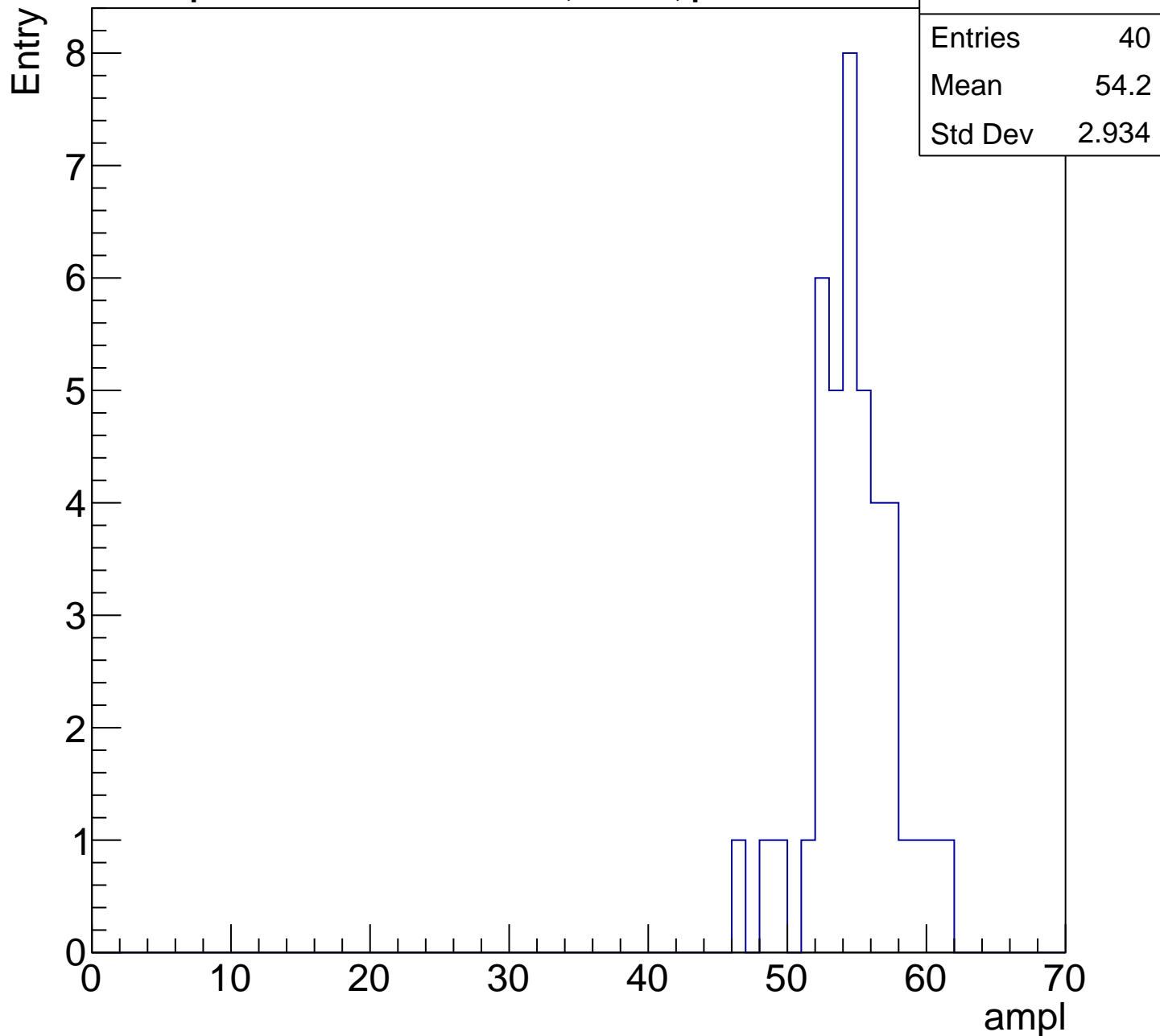
Entry

Entries	67
Mean	49.63
Std Dev	3.966



# B1L102S, U8-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U8-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	60
Mean	58.37
Std Dev	8.095

Entry

10

8

6

4

2

0

0

10

20

30

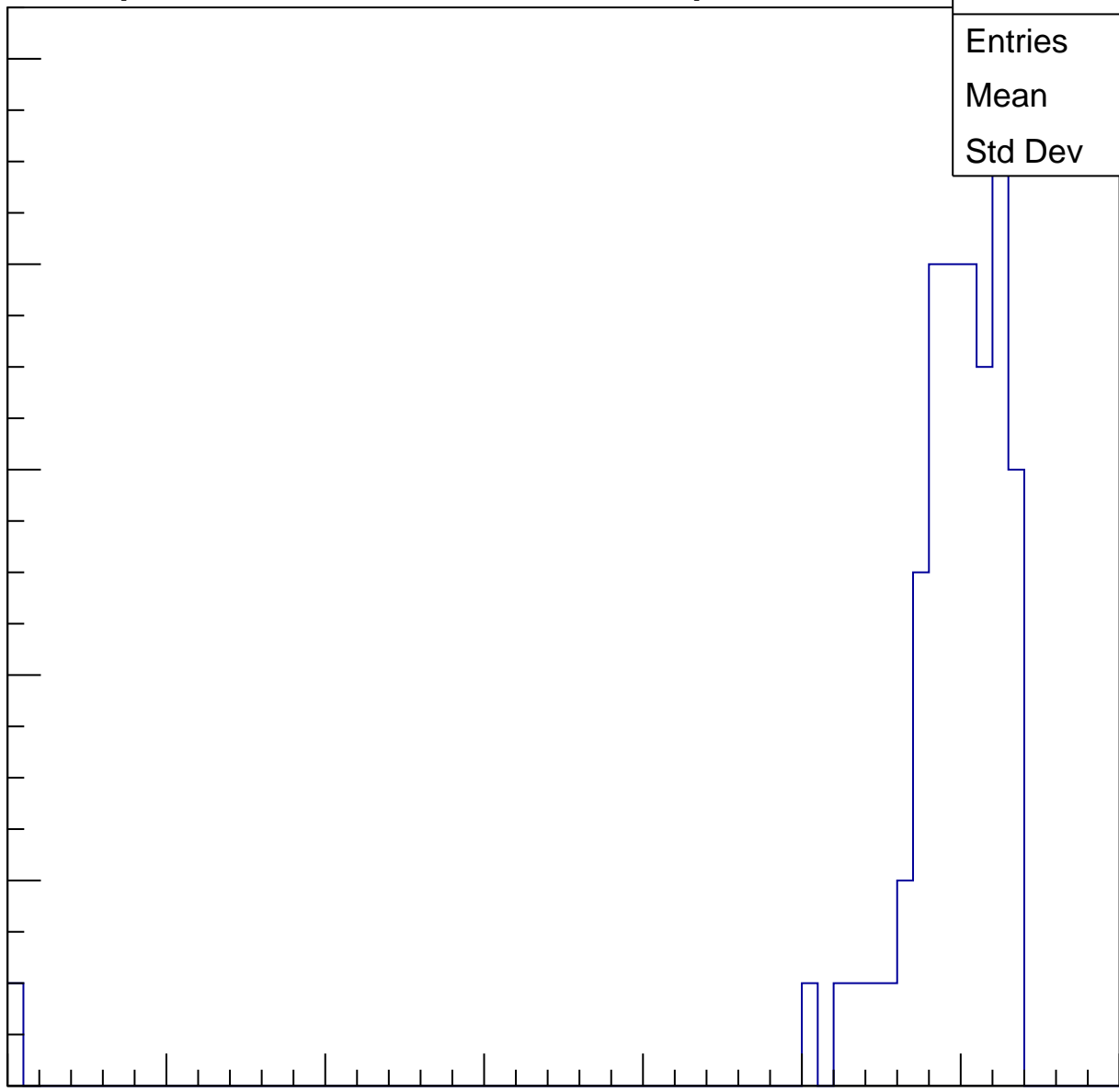
40

50

60

70

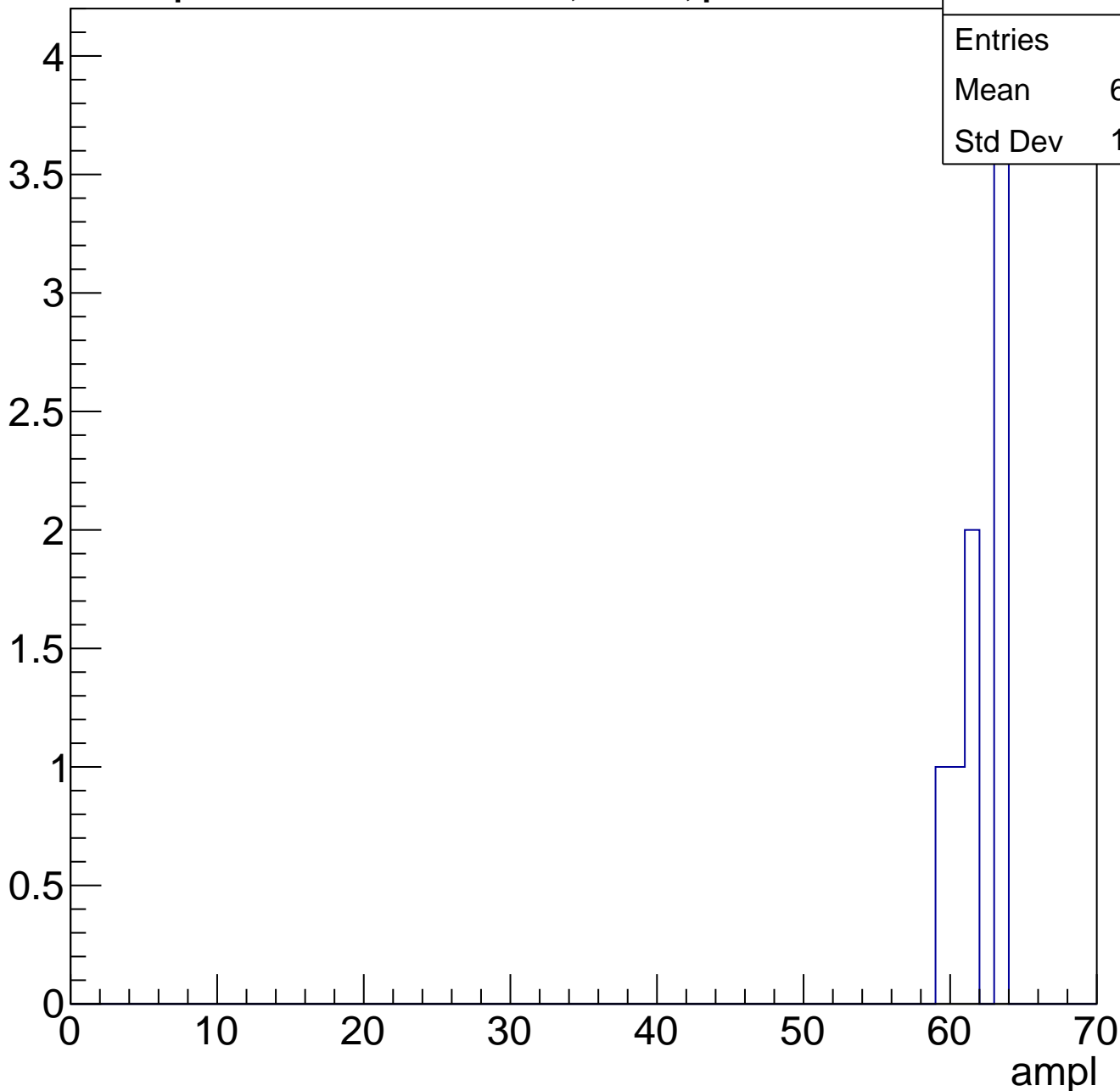
ampl



# B1L102S, U8-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	20
Std Dev	0

ampl

# B1L102S, U8-ch70, adc0

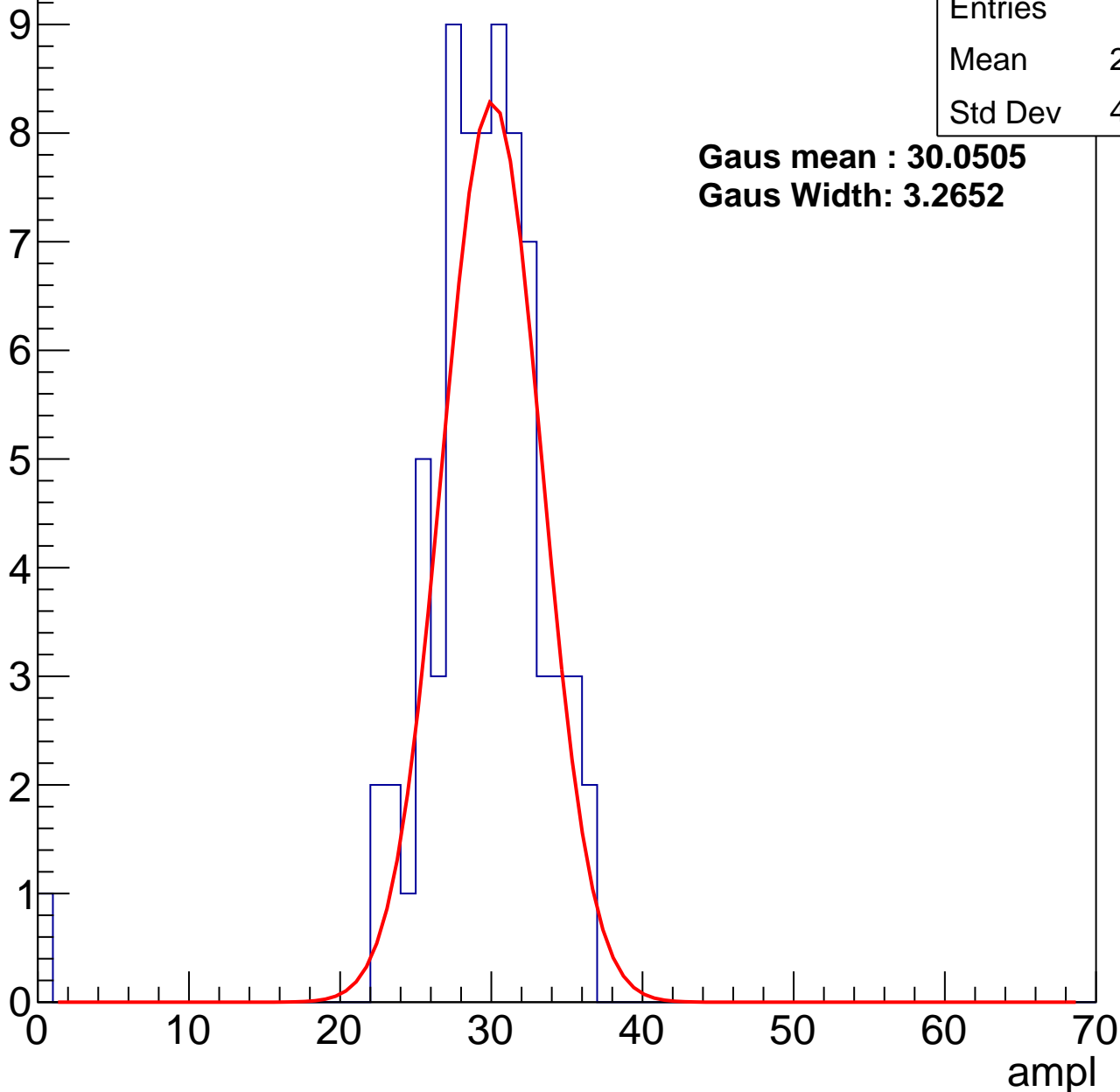
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	28.86
Std Dev	4.677

**Gaus mean : 30.0505**

**Gaus Width: 3.2652**



# B1L102S, U8-ch70, adc1

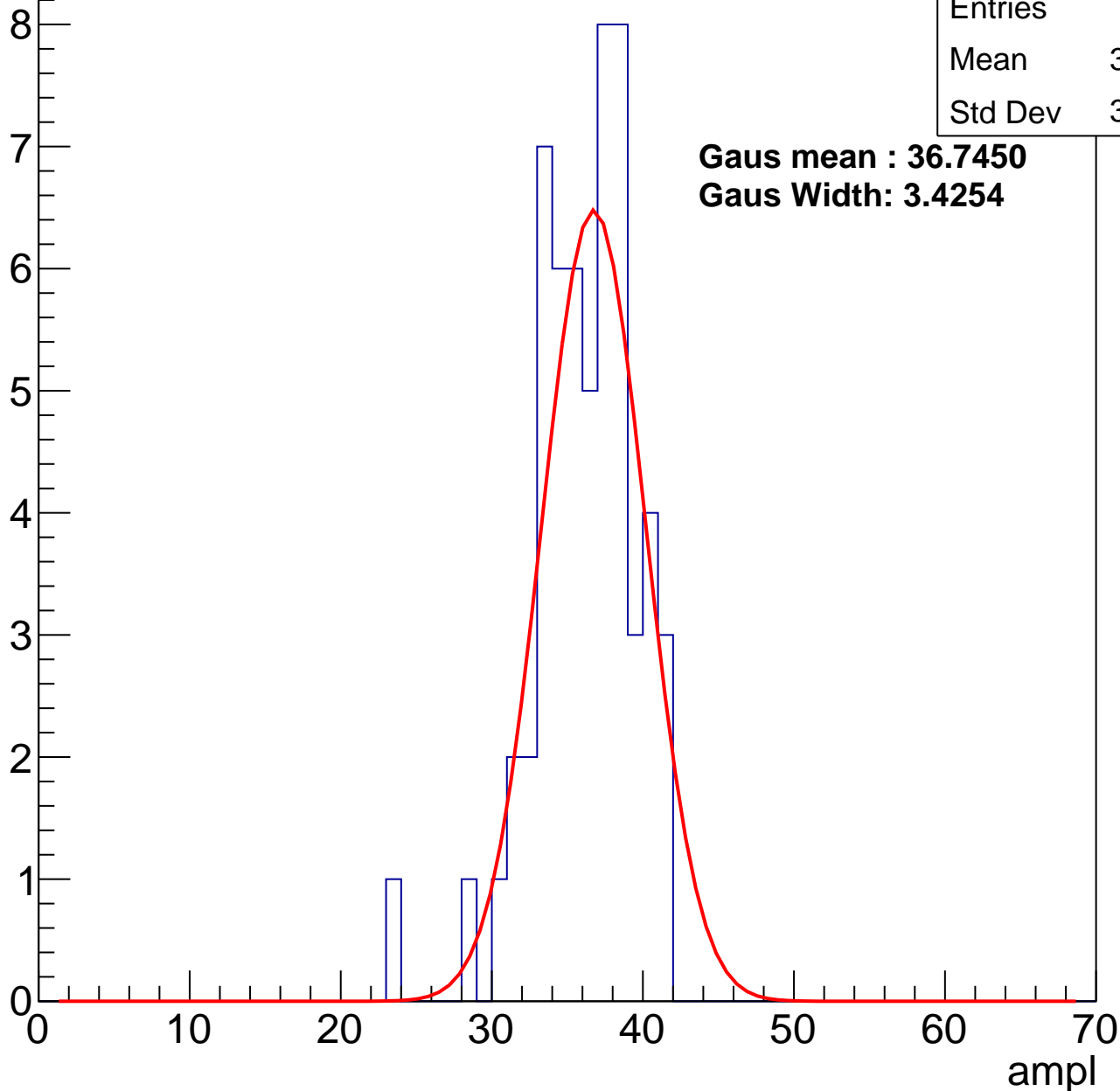
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	35.65
Std Dev	3.359

**Gaus mean : 36.7450**

**Gaus Width: 3.4254**



# B1L102S, U8-ch70, adc2

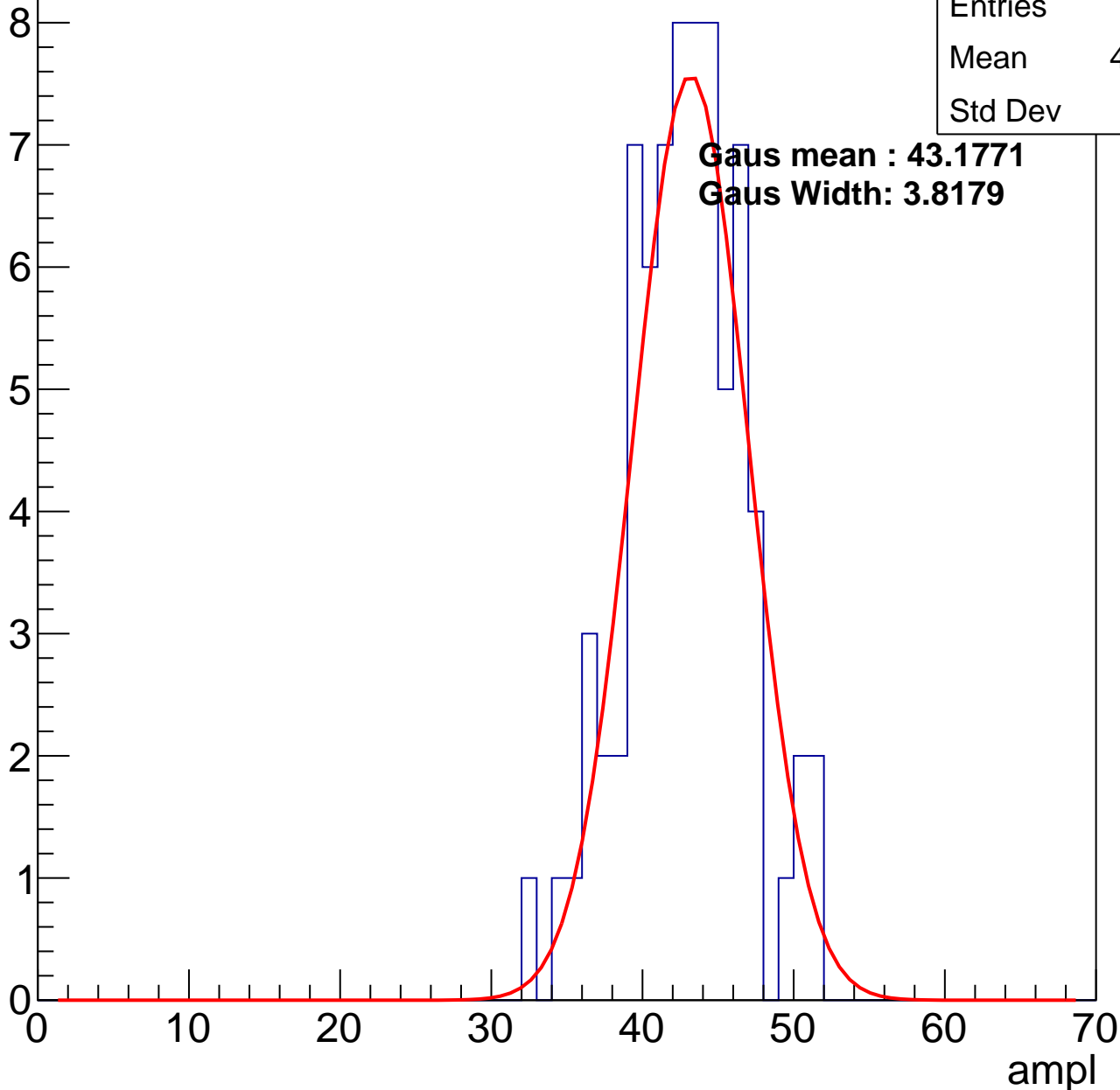
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	42.36
Std Dev	3.87

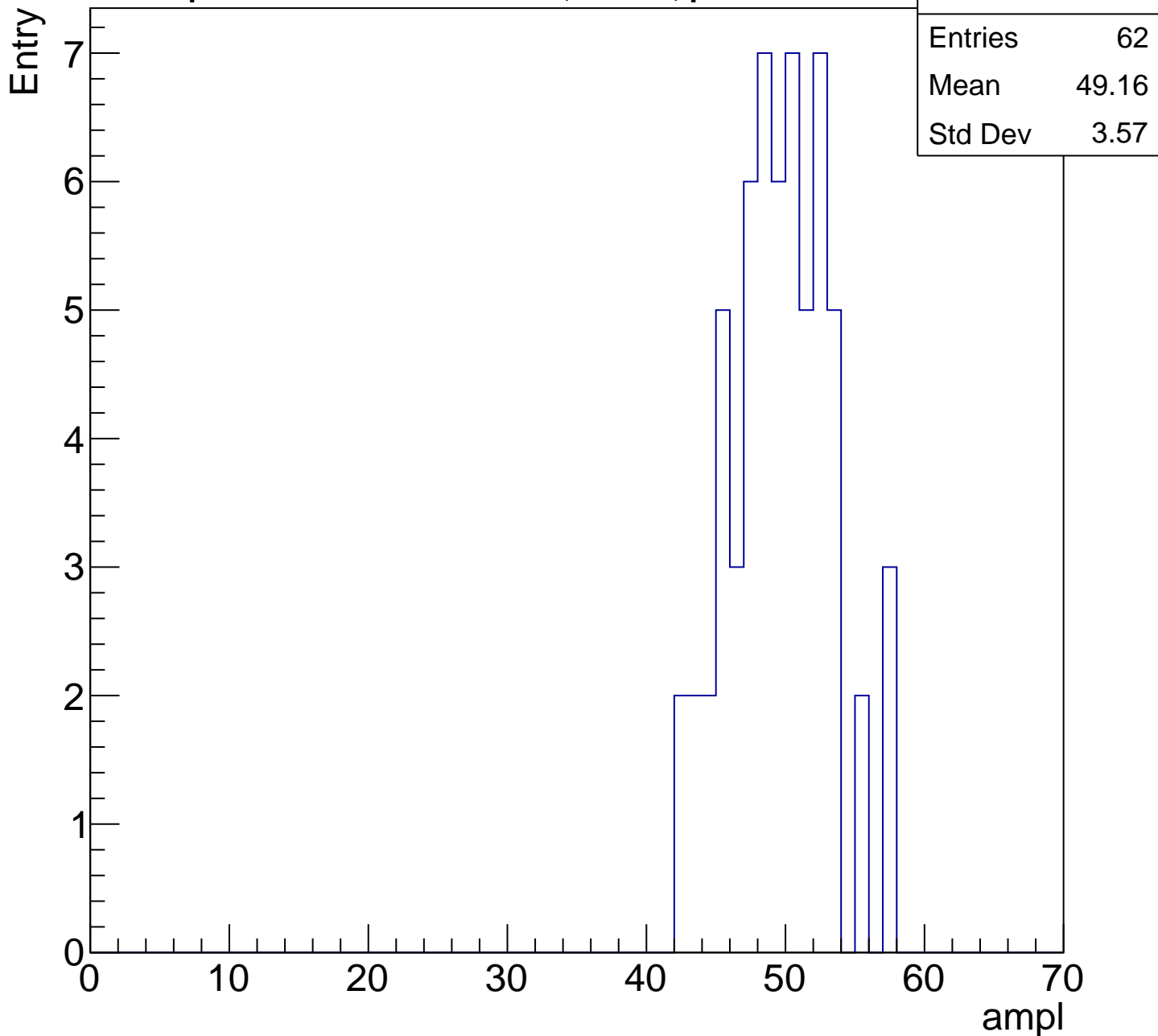
**Gaus mean : 43.1771**

**Gaus Width: 3.8179**



# B1L102S, U8-ch70, adc3

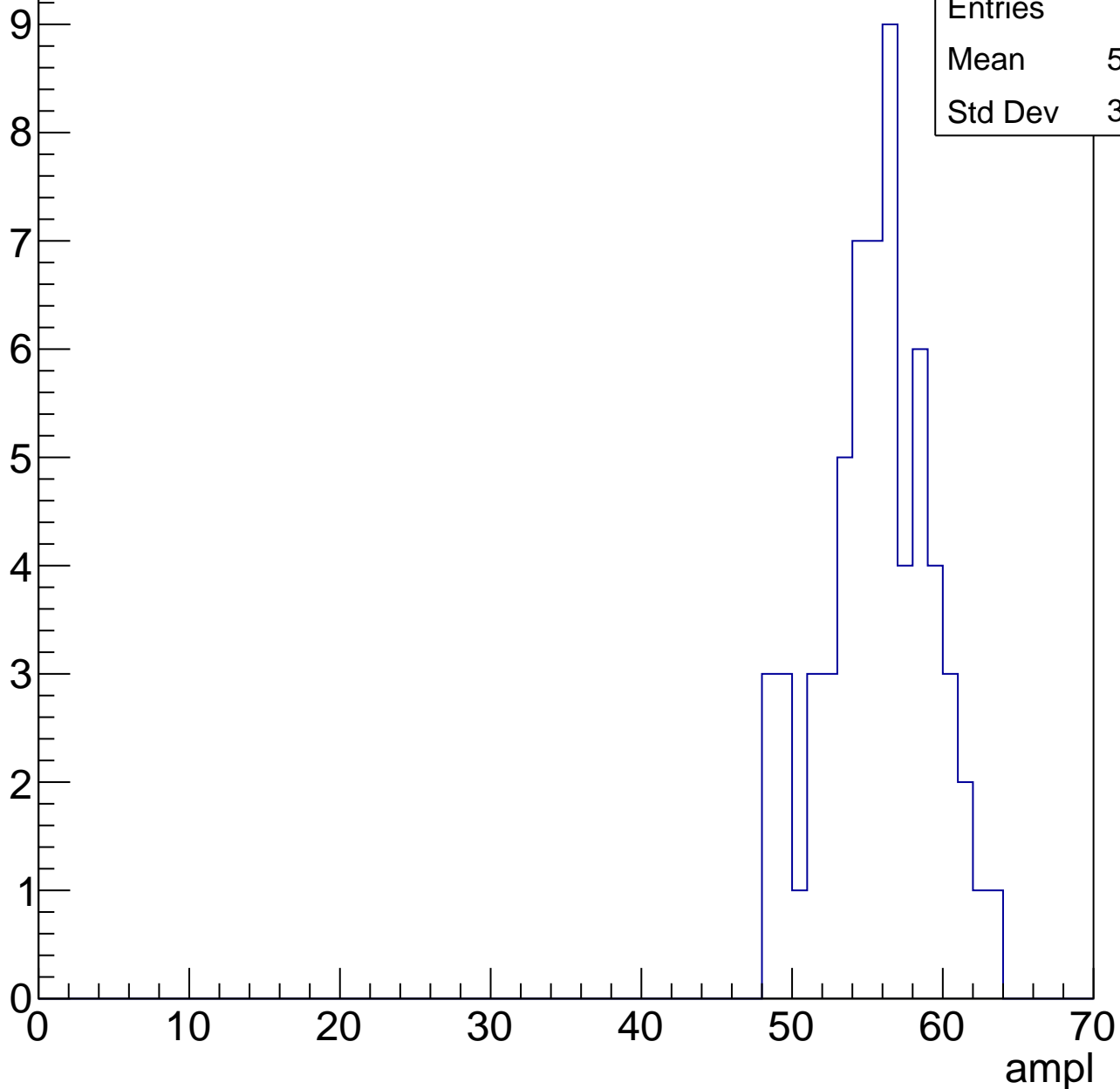
calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U8-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

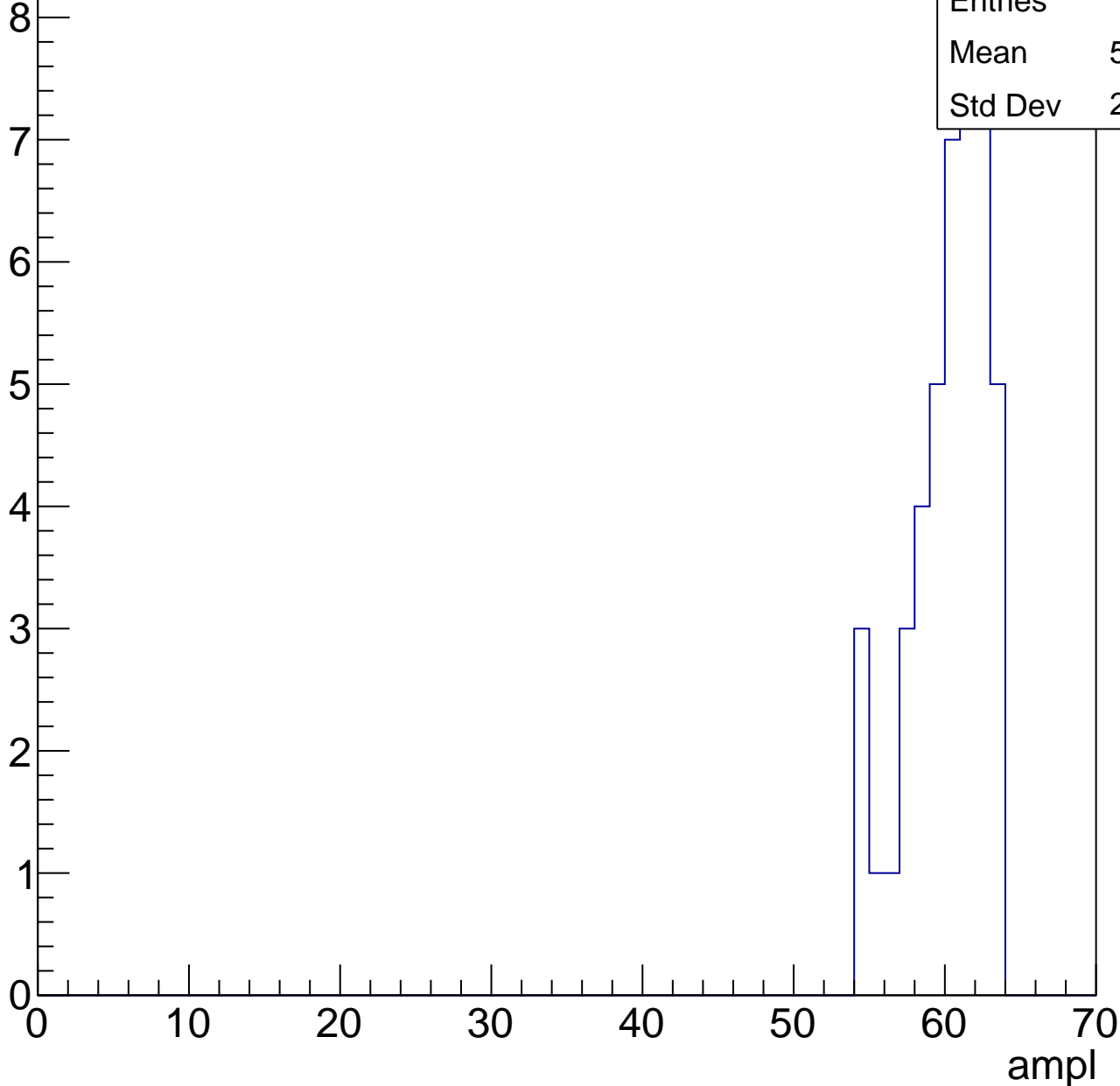


# B1L102S, U8-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

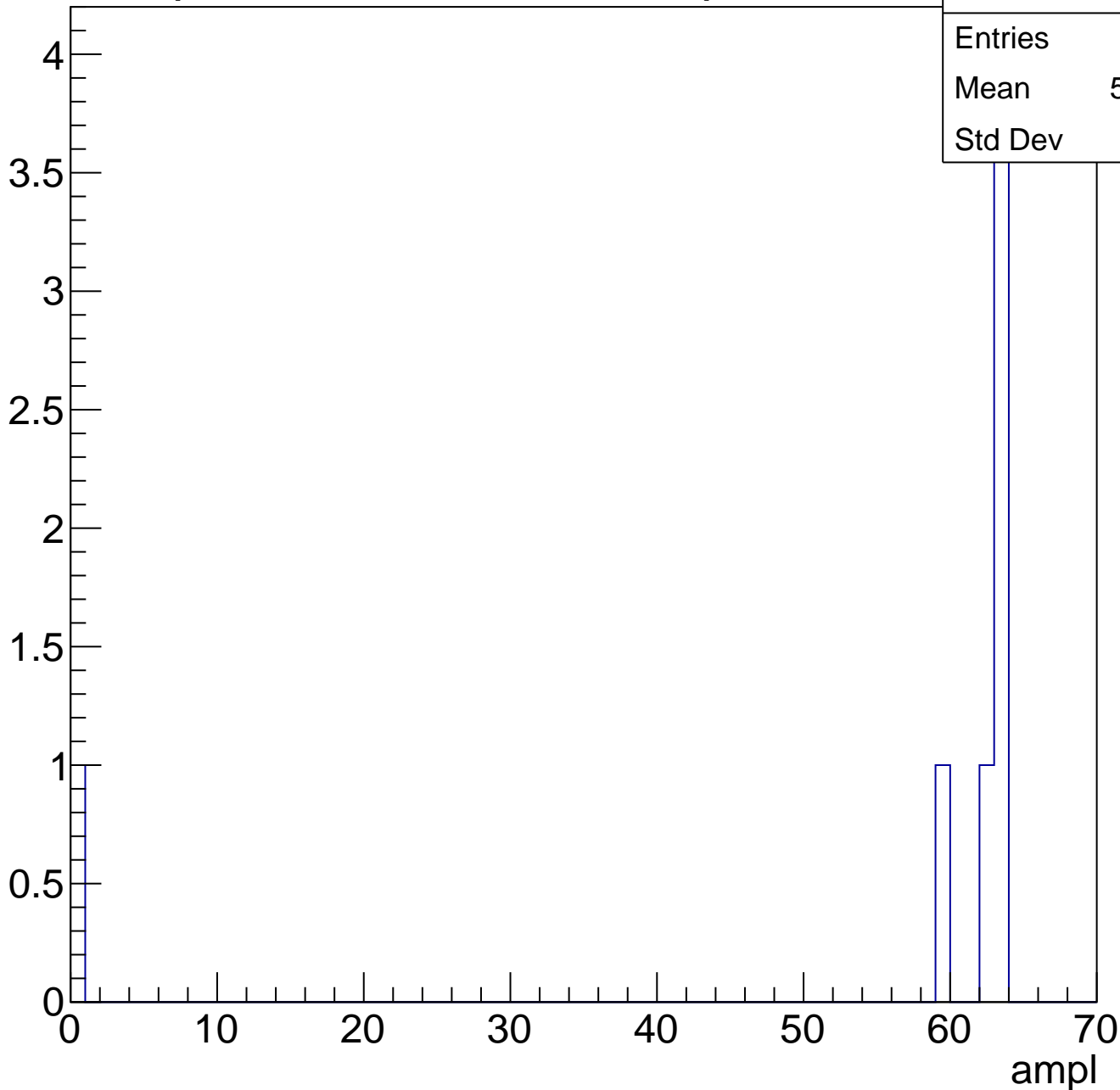
Entries	45
Mean	59.78
Std Dev	2.493



# B1L102S, U8-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U8-ch71, adc0

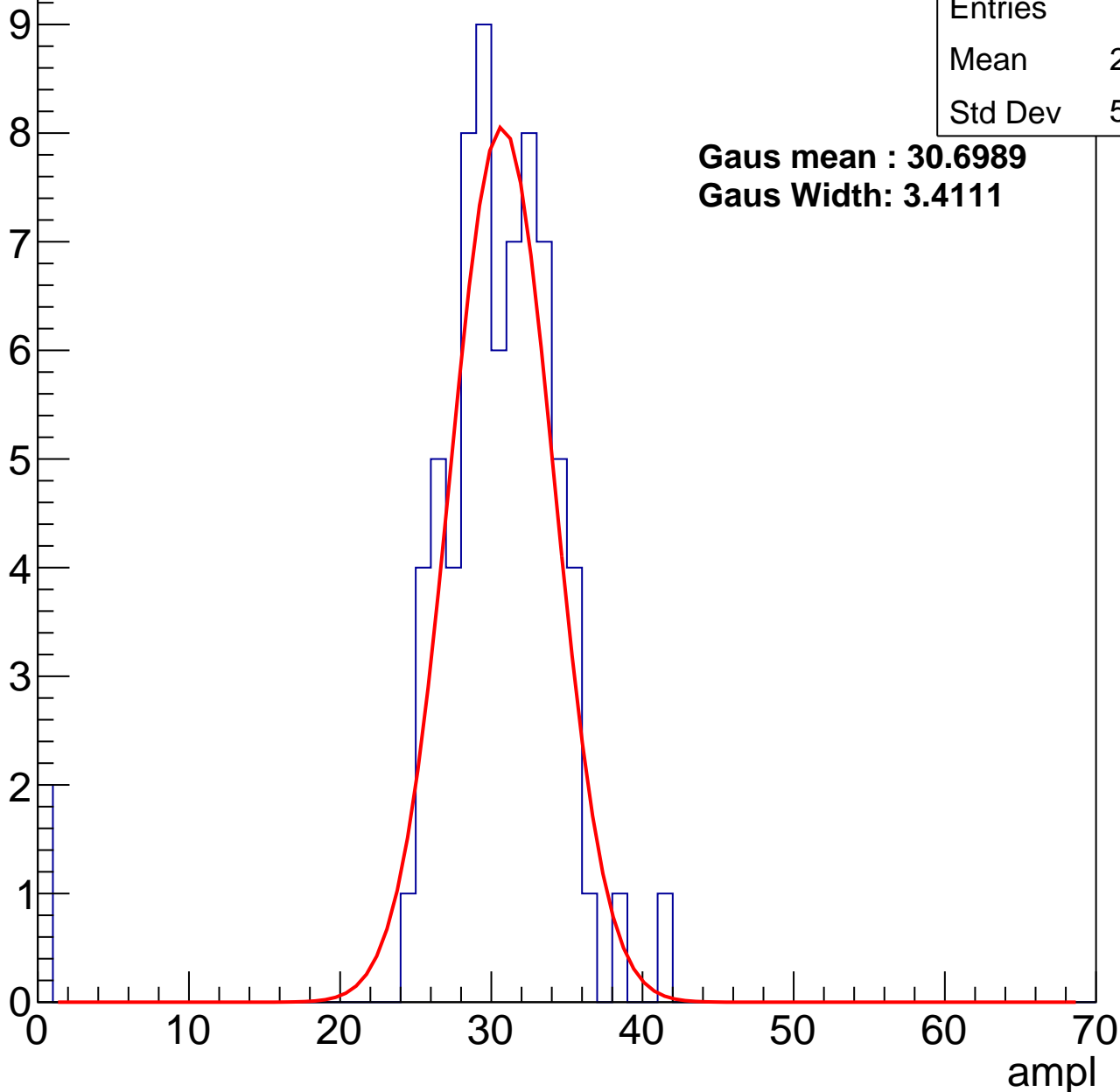
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	29.53
Std Dev	5.945

**Gaus mean : 30.6989**

**Gaus Width: 3.4111**



# B1L102S, U8-ch71, adc1

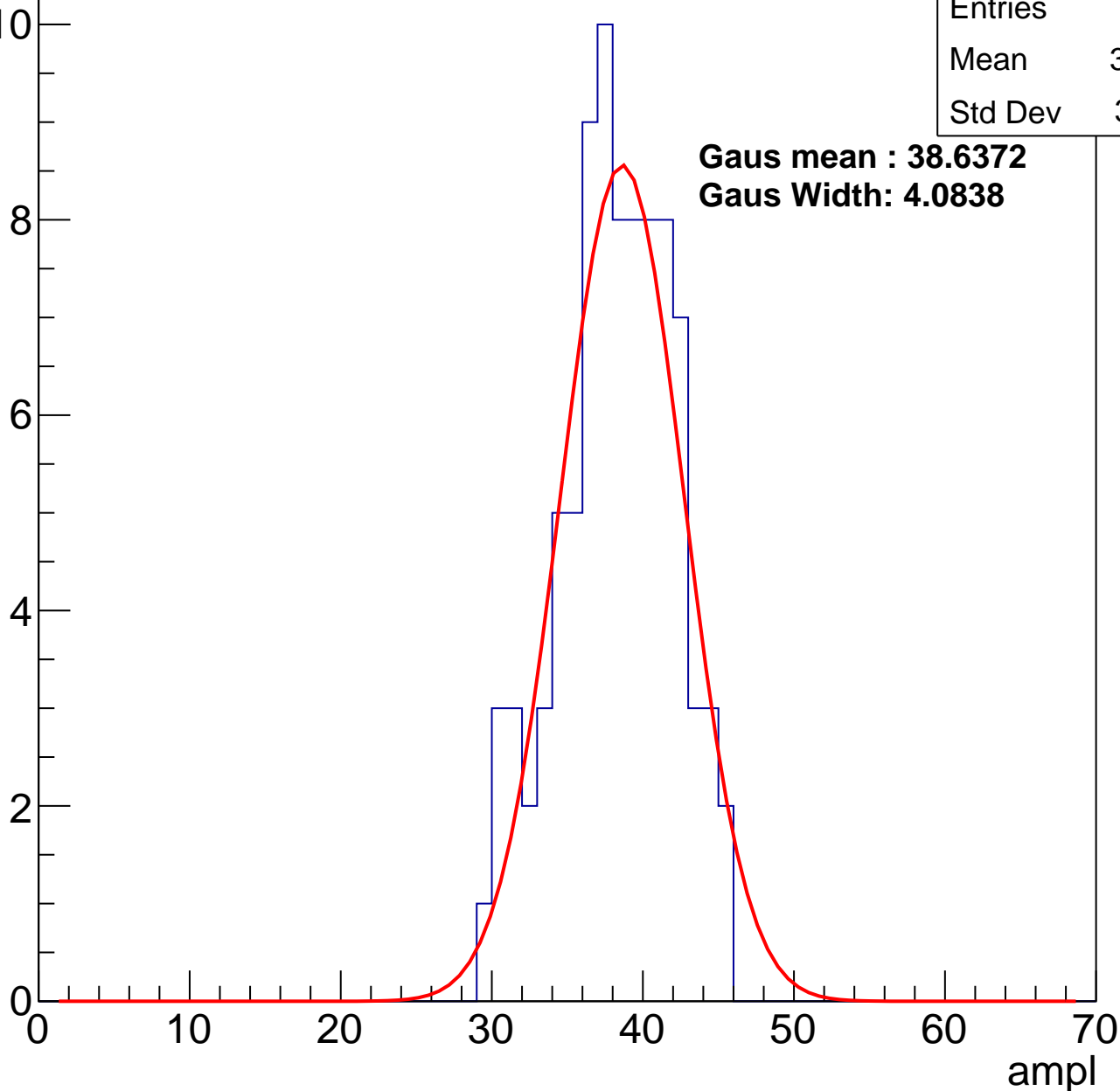
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	88
Mean	37.76
Std Dev	3.751

**Gaus mean : 38.6372**

**Gaus Width: 4.0838**



# B1L102S, U8-ch71, adc2

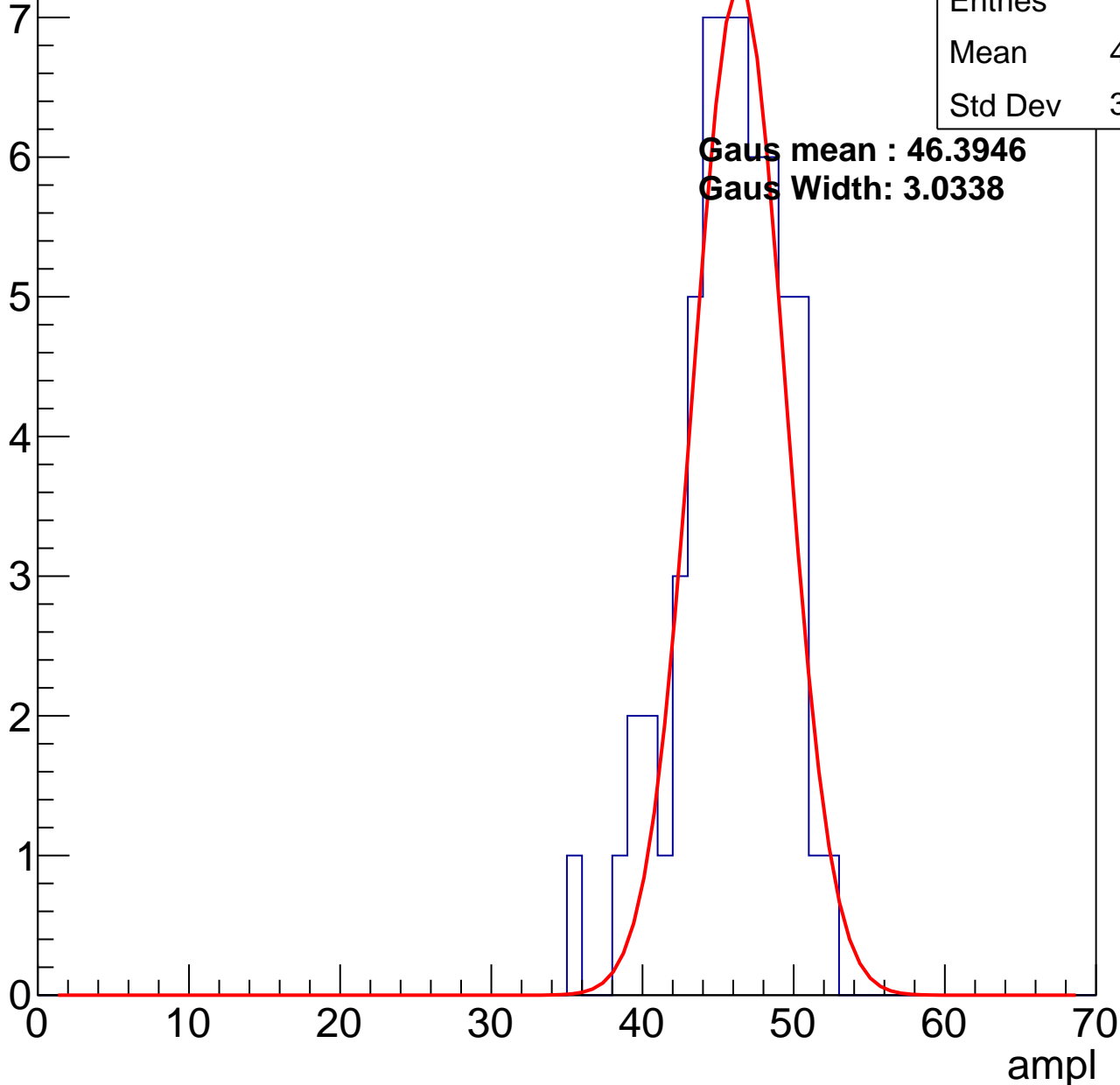
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	45.43
Std Dev	3.427

**Gaus mean : 46.3946**

**Gaus Width: 3.0338**

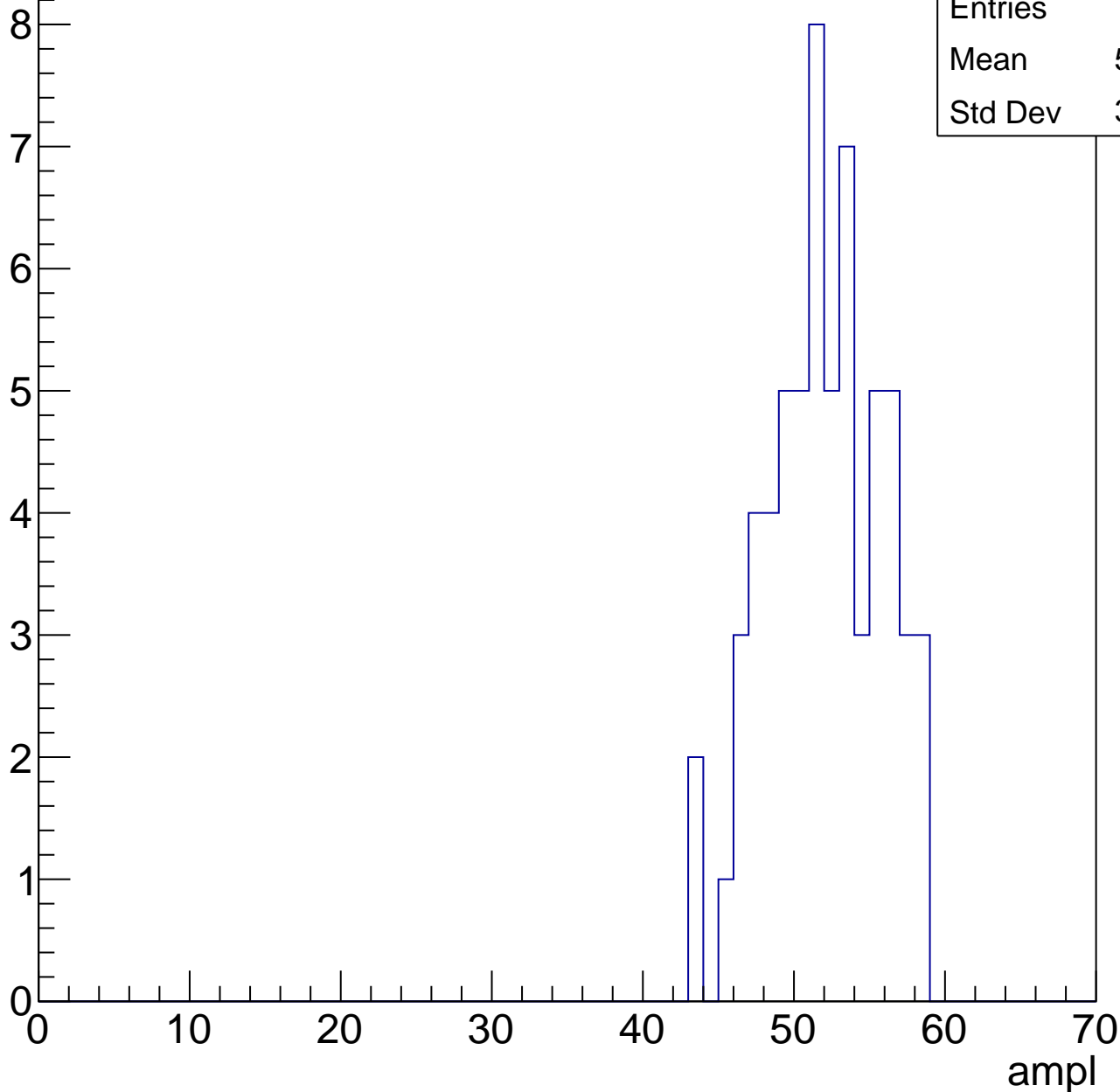


# B1L102S, U8-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	51.51
Std Dev	3.711

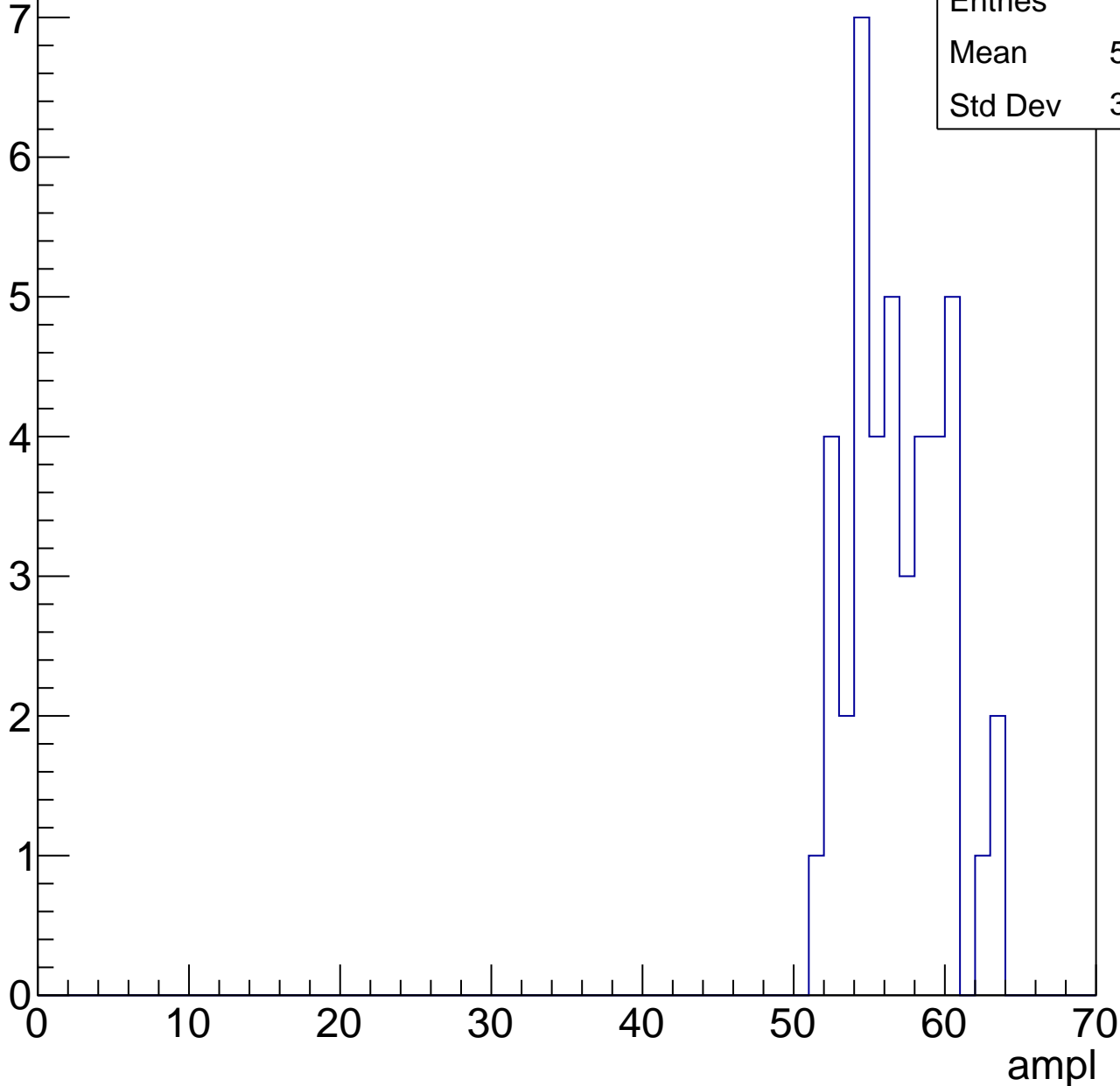


# B1L102S, U8-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	42
Mean	56.43
Std Dev	3.087

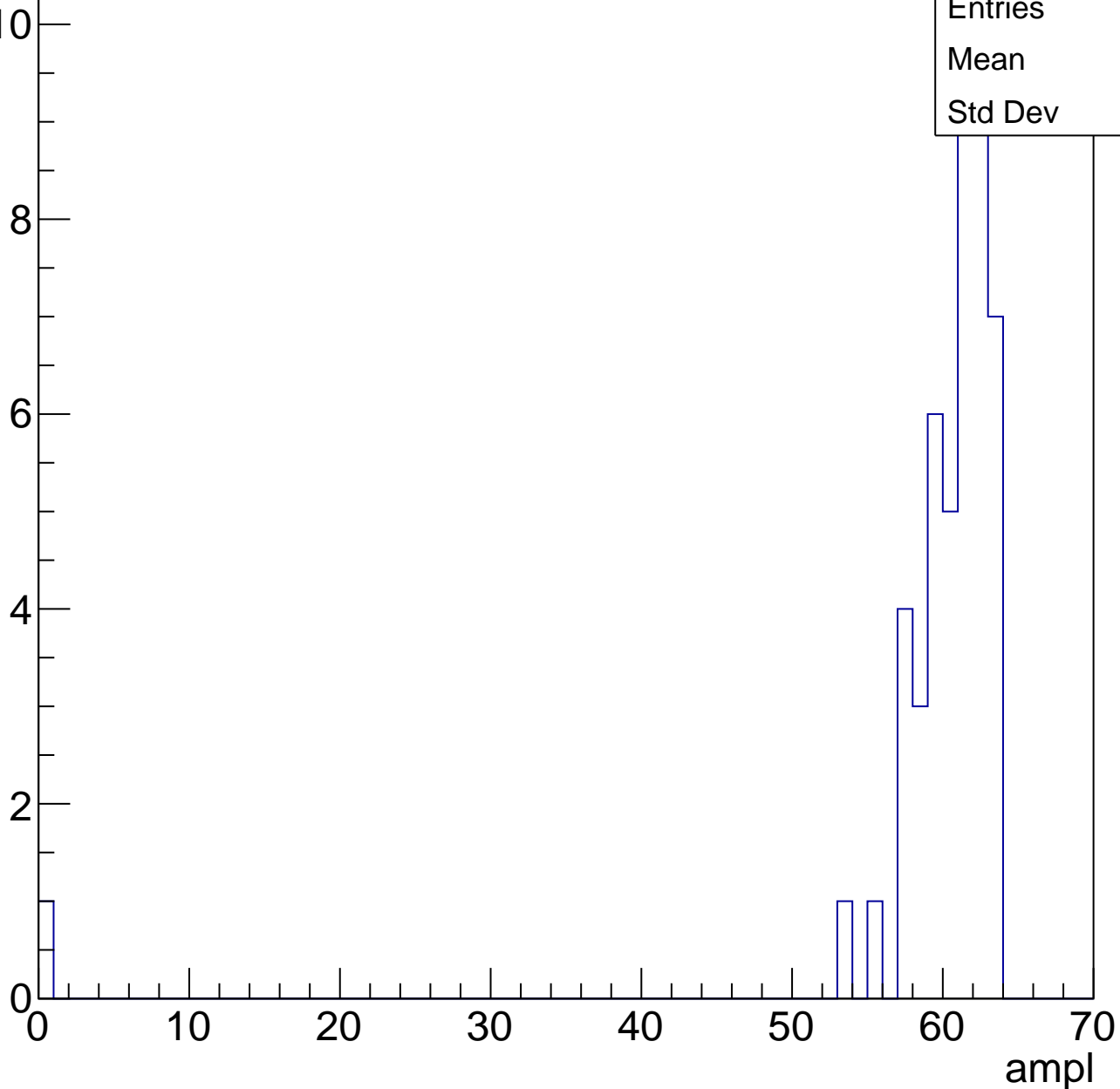


# B1L102S, U8-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

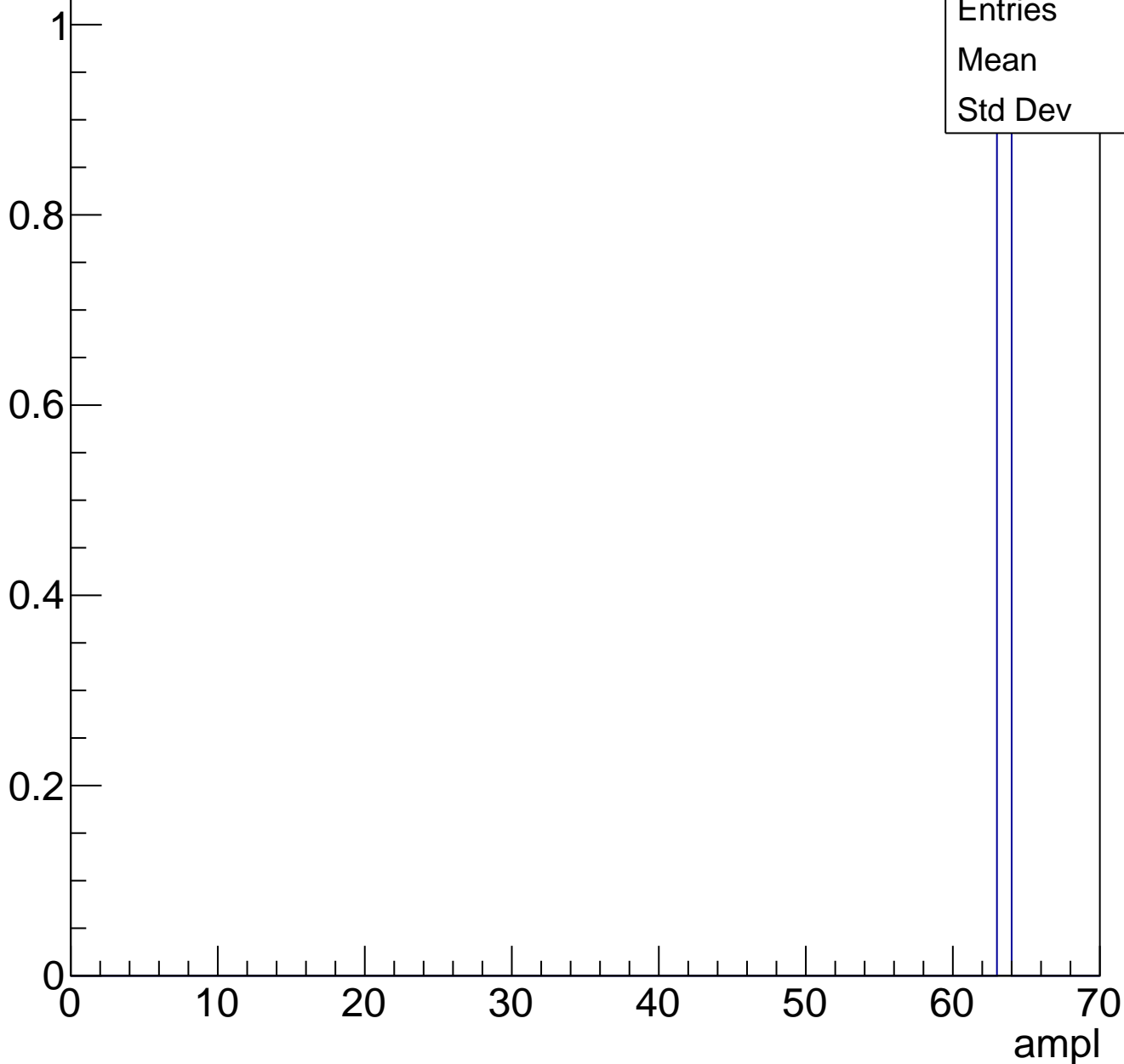
Entries	47
Mean	59
Std Dev	8.98



# B1L102S, U8-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch72, adc0

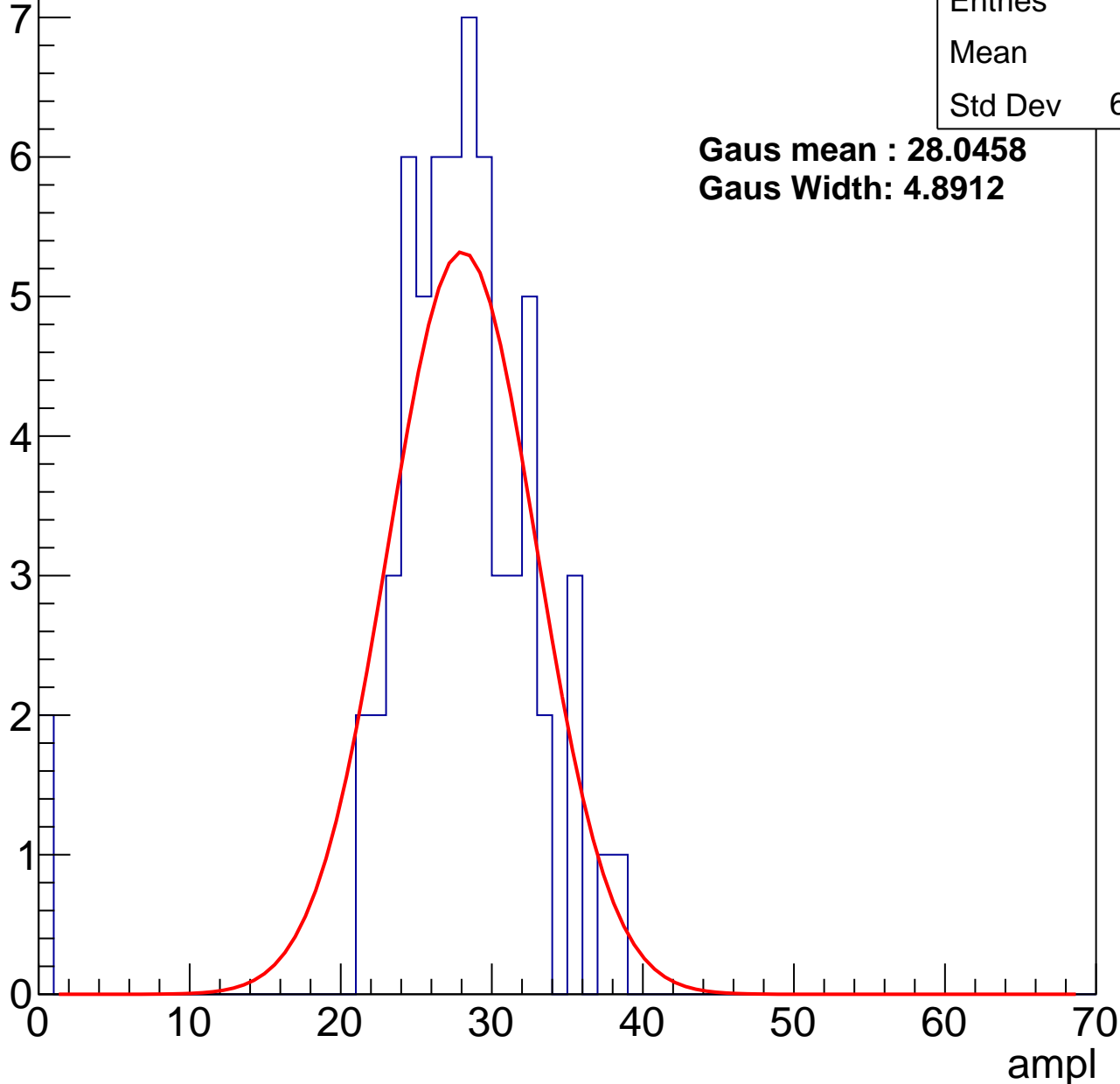
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	27
Std Dev	6.203

**Gaus mean : 28.0458**

**Gaus Width: 4.8912**



# B1L102S, U8-ch72, adc1

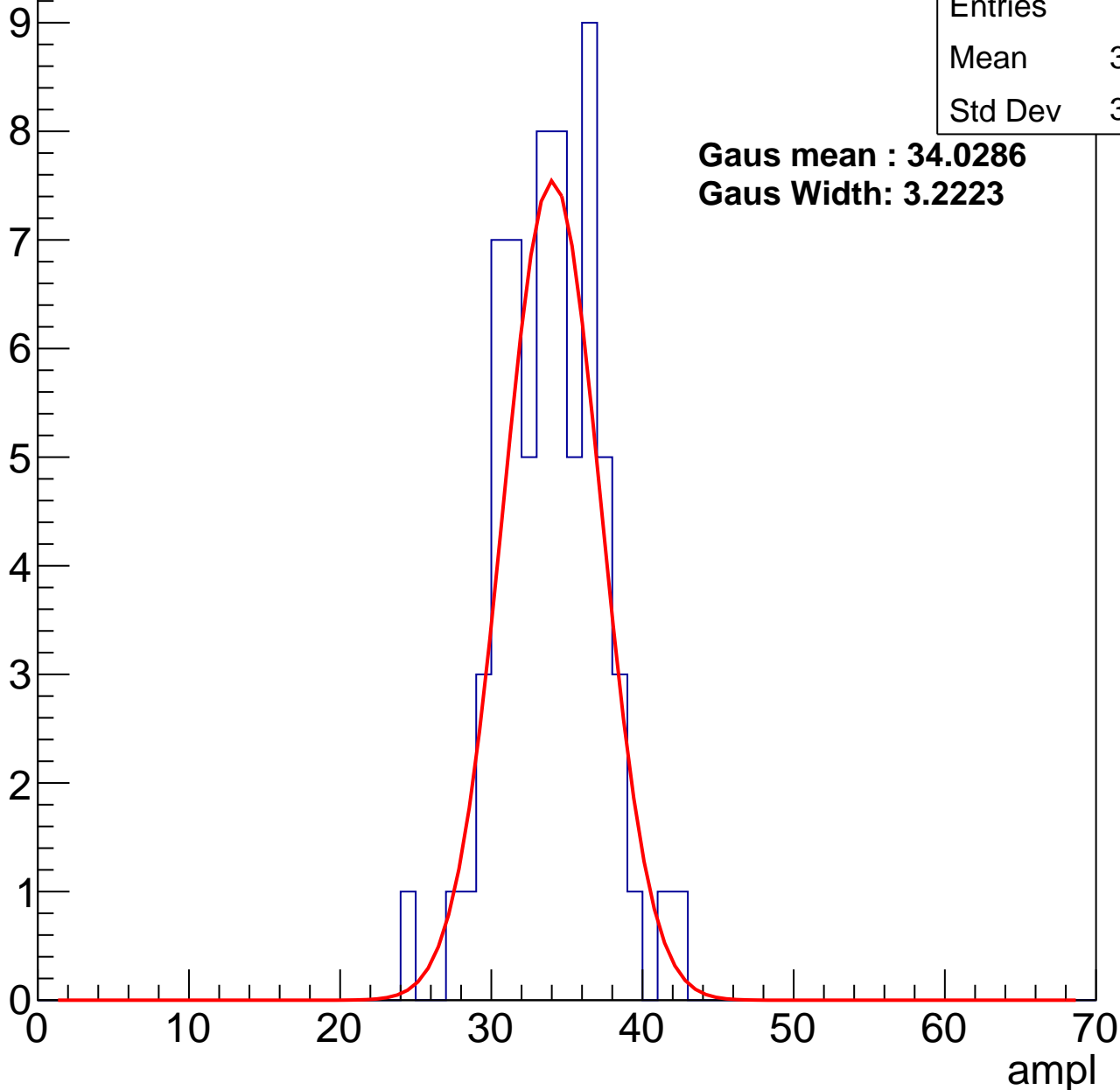
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	33.47
Std Dev	3.295

**Gaus mean : 34.0286**

**Gaus Width: 3.2223**



# B1L102S, U8-ch72, adc2

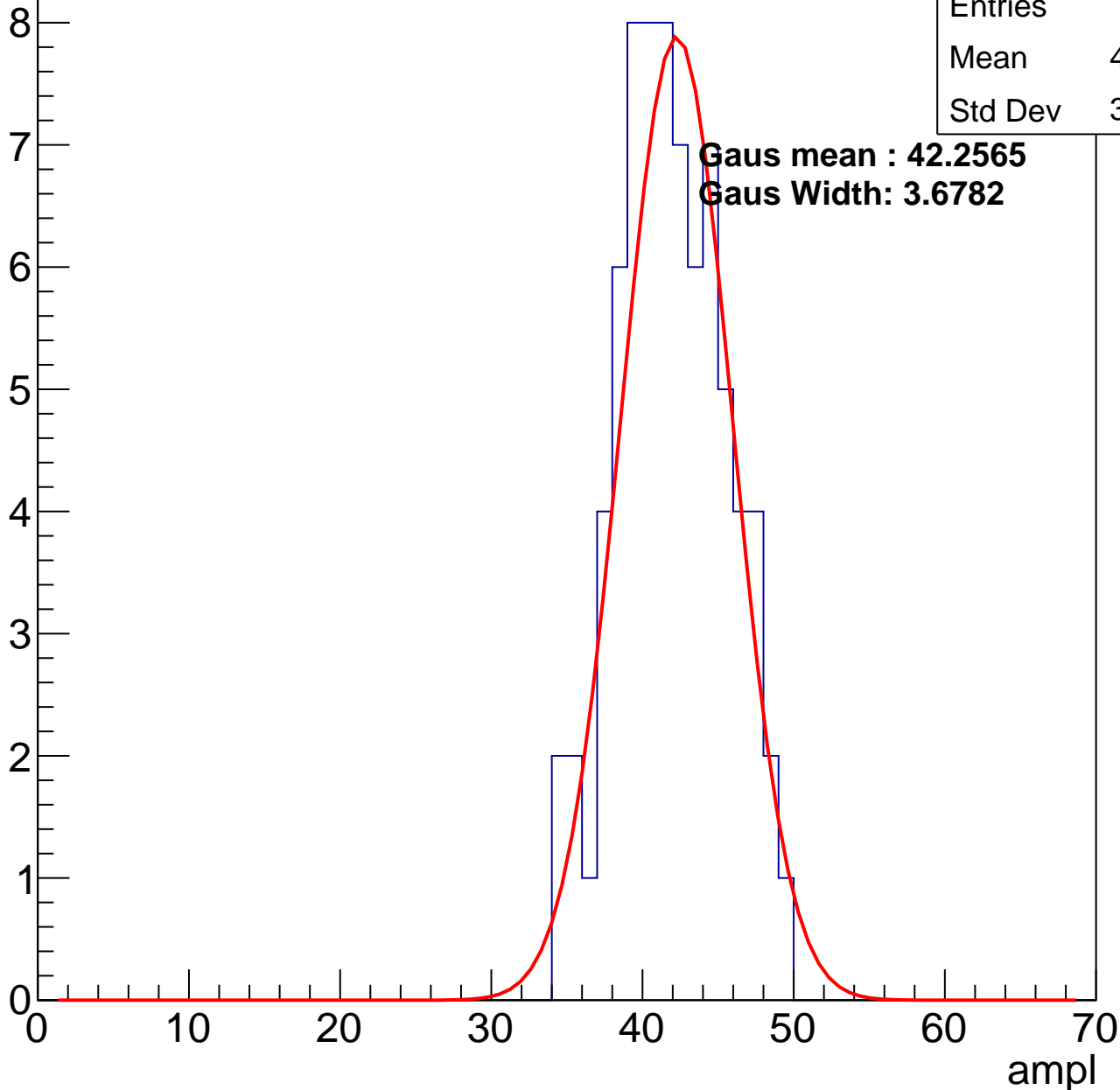
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	41.49
Std Dev	3.492

**Gaus mean : 42.2565**

**Gaus Width: 3.6782**

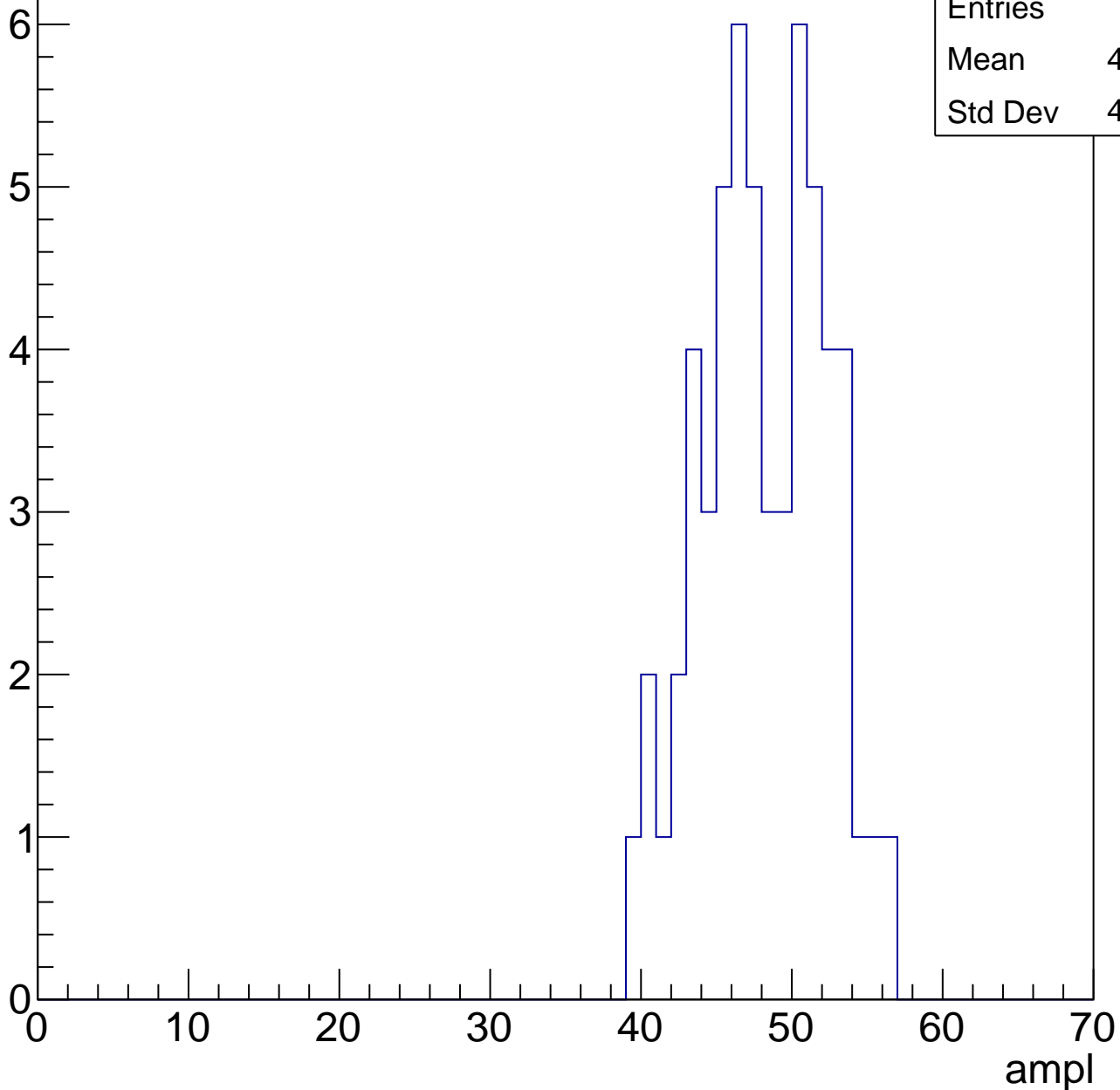


# B1L102S, U8-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	47.63
Std Dev	4.038

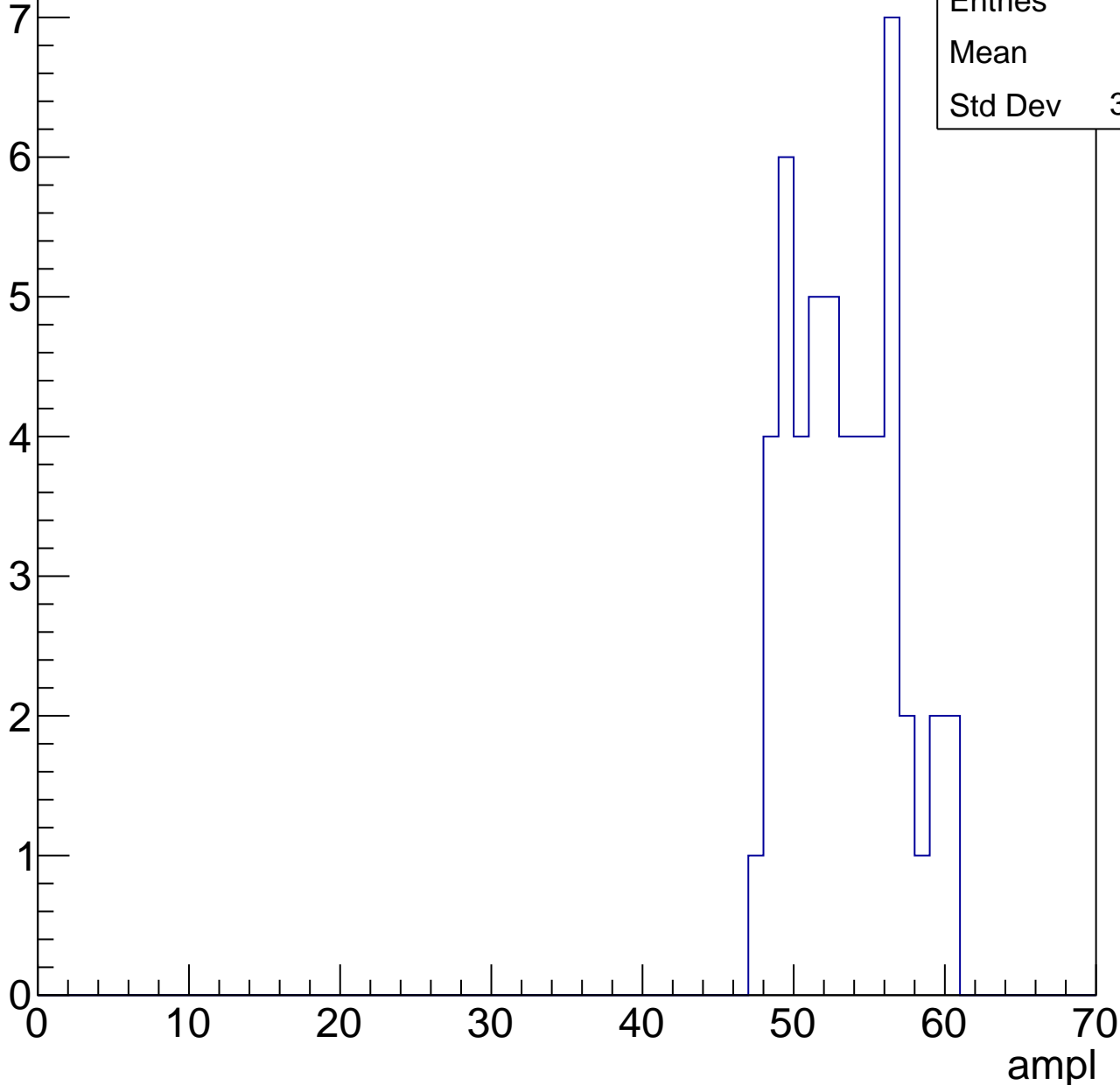


# B1L102S, U8-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	52.9
Std Dev	3.437

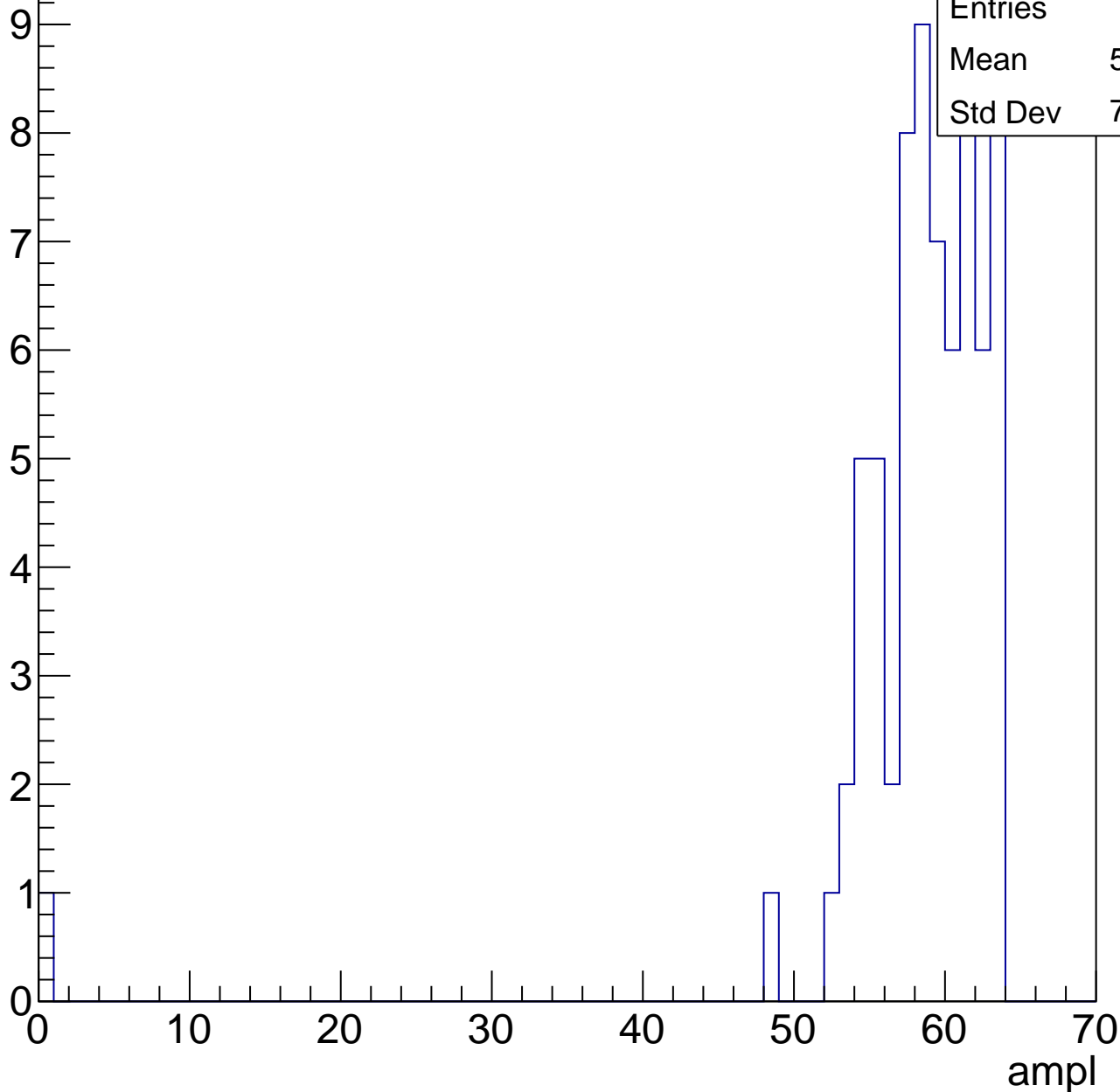


# B1L102S, U8-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	57.77
Std Dev	7.618



# B1L102S, U8-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

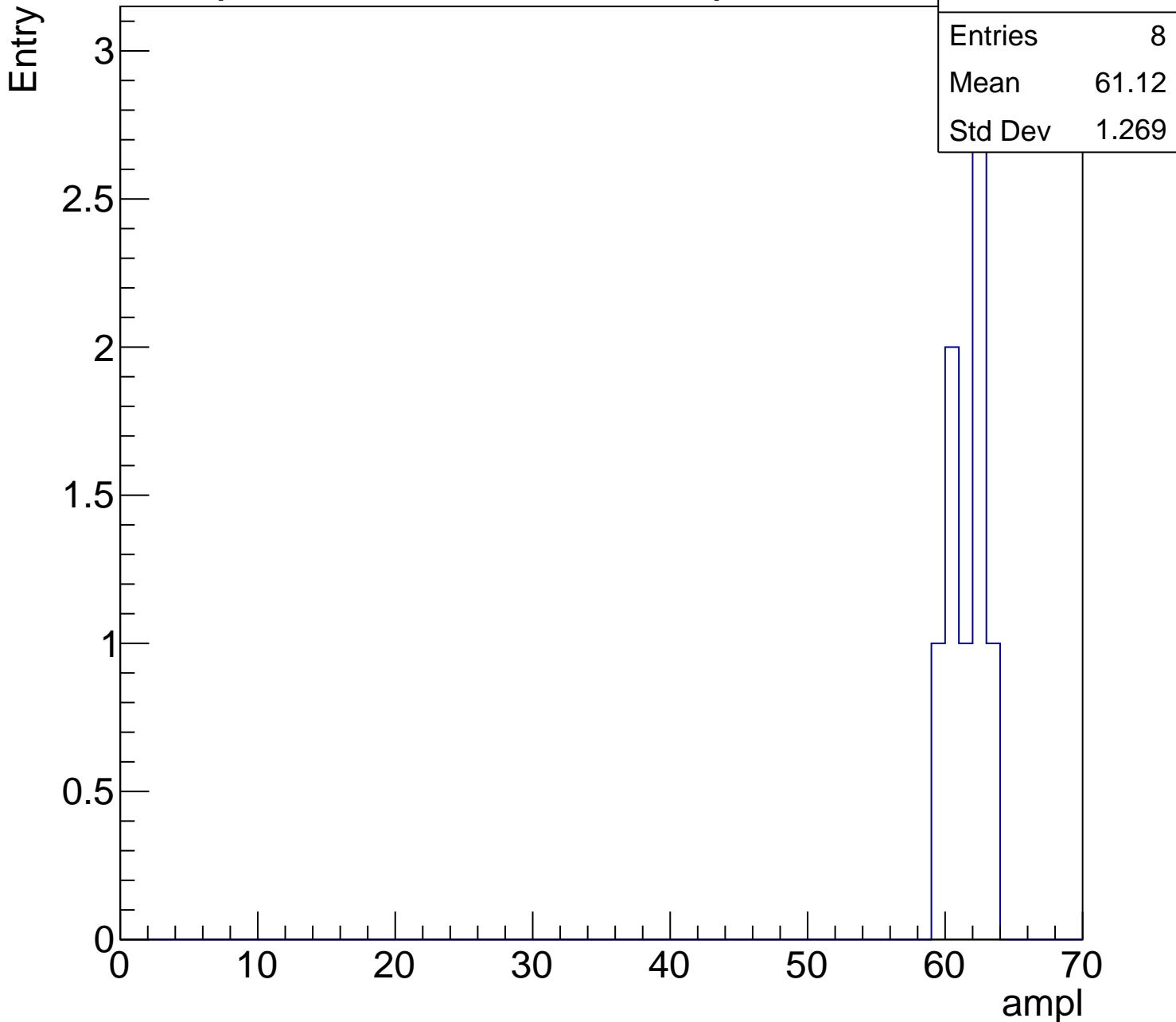
8

Mean

61.12

Std Dev

1.269

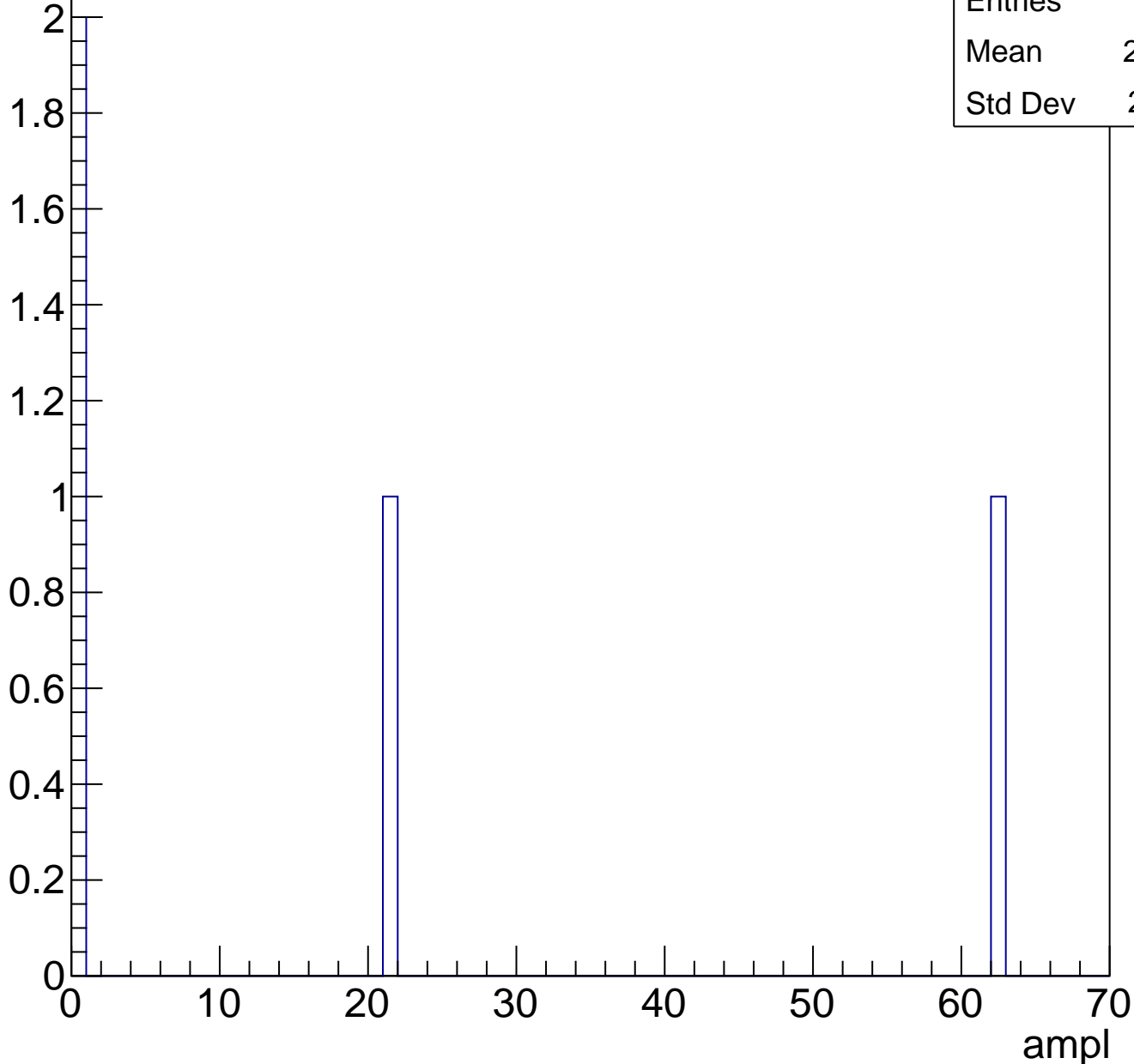




# B1L102S, U8-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	4
Mean	20.75
Std Dev	25.31

# B1L102S, U8-ch73, adc0

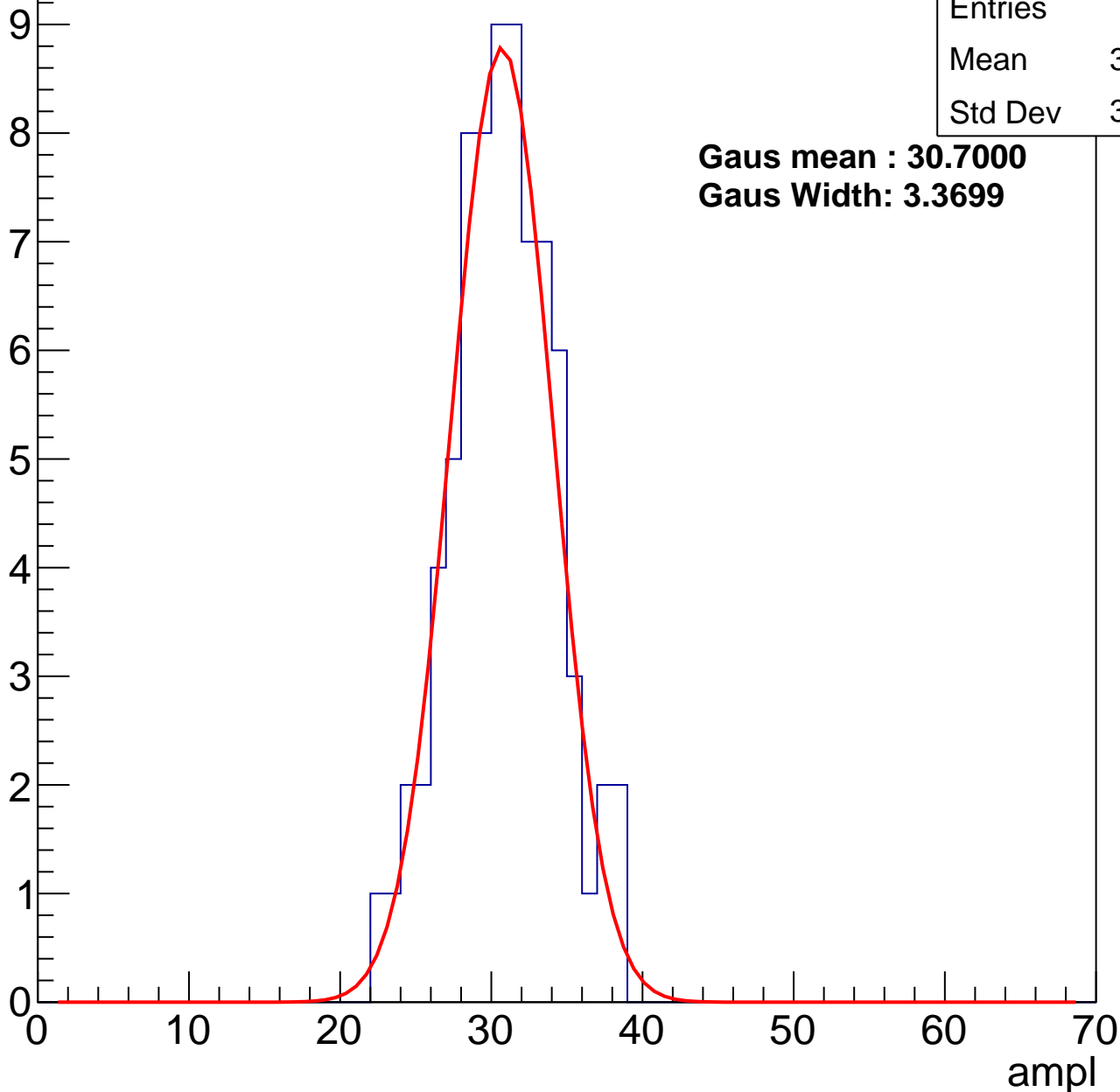
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	30.35
Std Dev	3.433

**Gaus mean : 30.7000**

**Gaus Width: 3.3699**



# B1L102S, U8-ch73, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

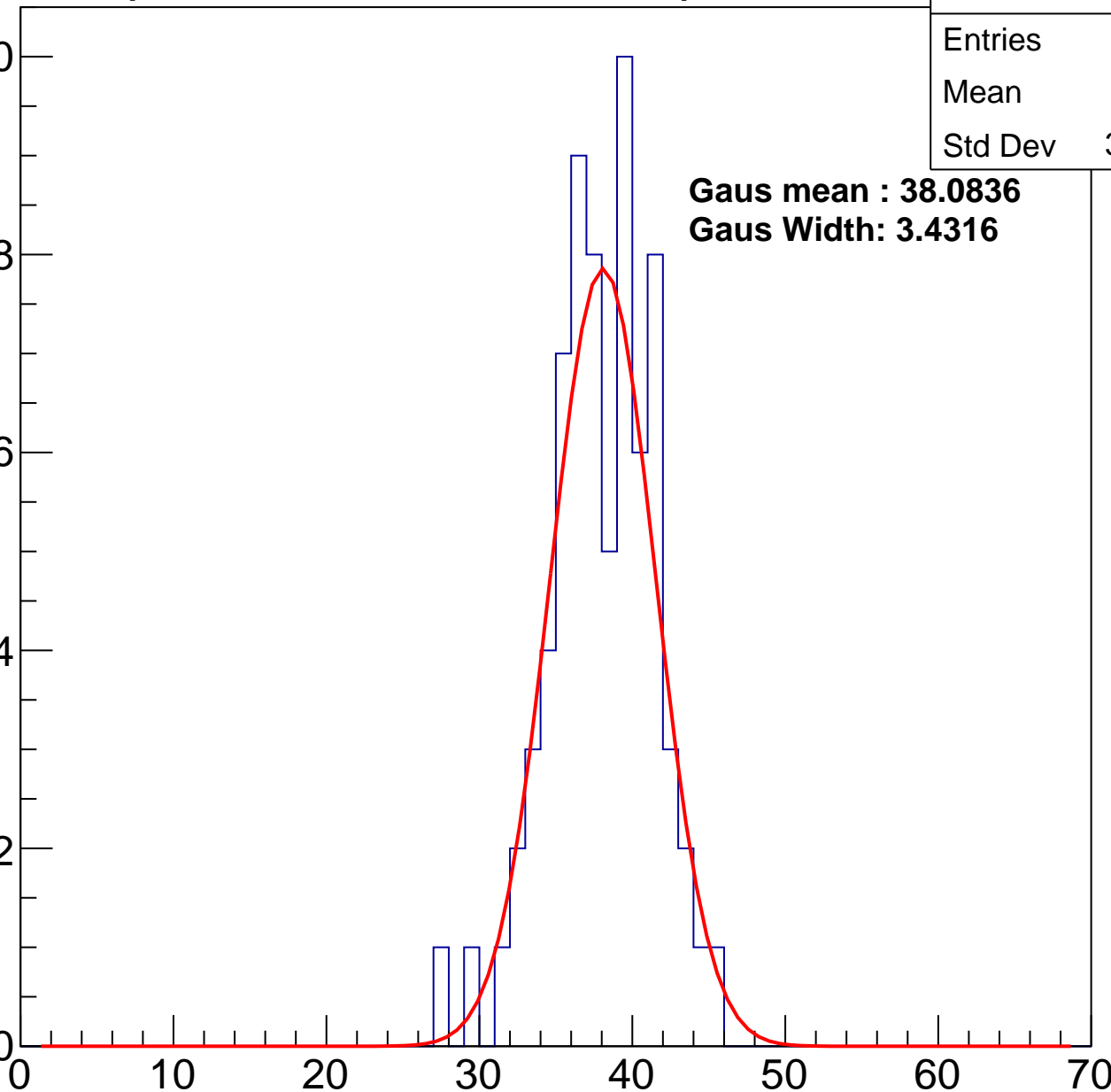
Entries	72
Mean	37.5
Std Dev	3.416

**Gaus mean : 38.0836**

**Gaus Width: 3.4316**

10  
8  
6  
4  
2  
0

ampl



# B1L102S, U8-ch73, adc2

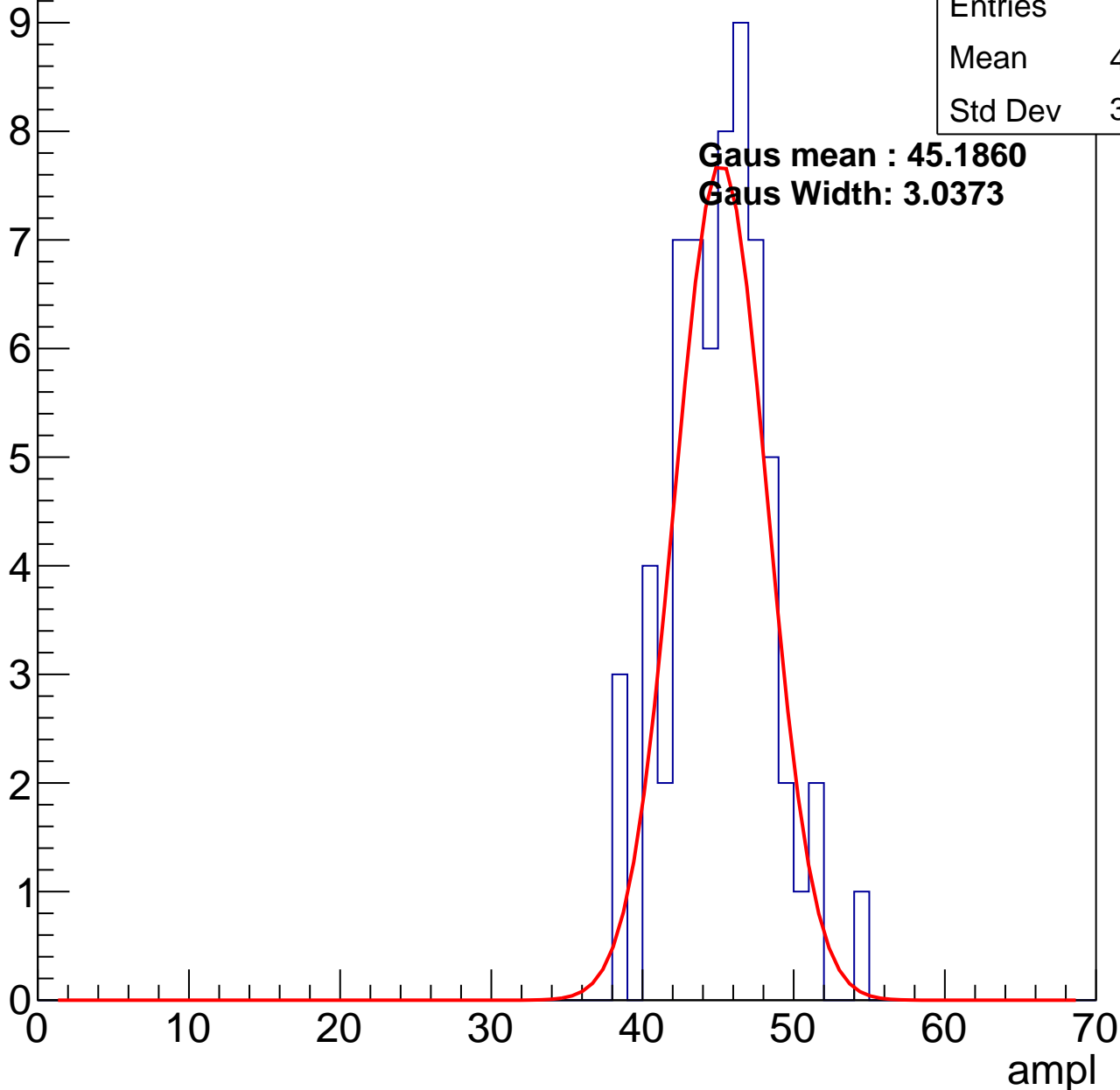
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	44.72
Std Dev	3.218

**Gaus mean : 45.1860**

**Gaus Width: 3.0373**

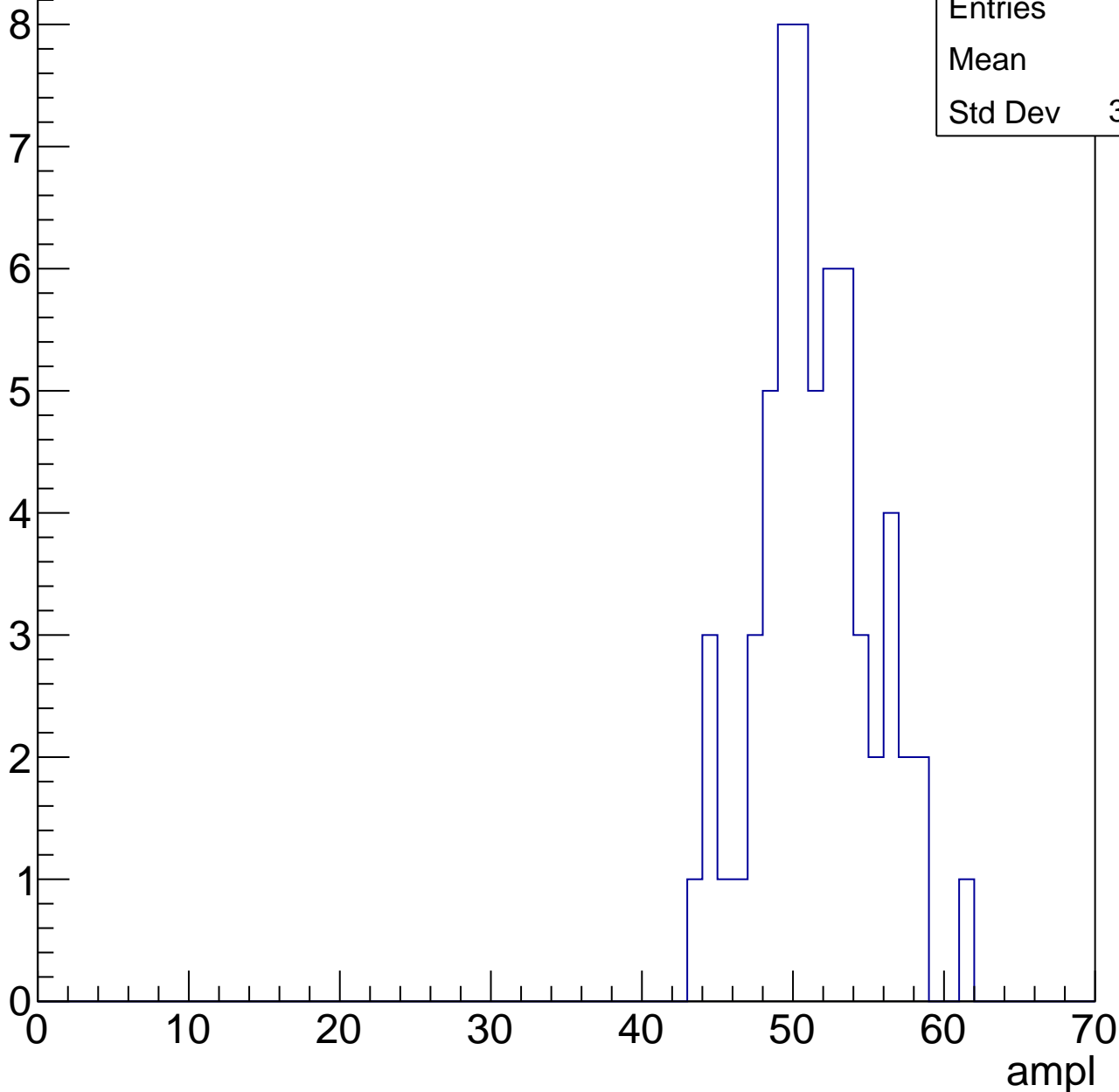


# B1L102S, U8-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	51
Std Dev	3.764

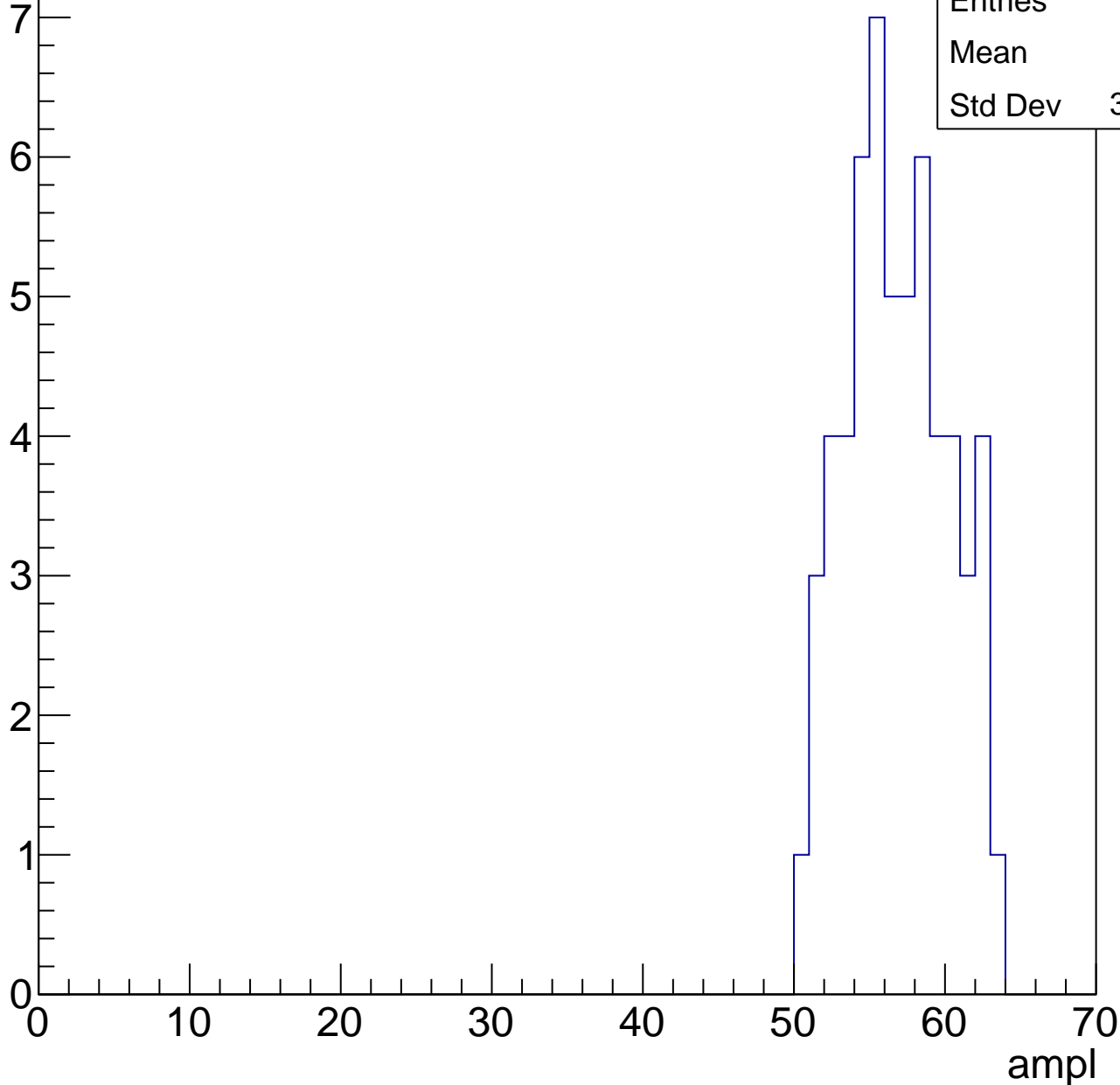


# B1L102S, U8-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	56.4
Std Dev	3.324

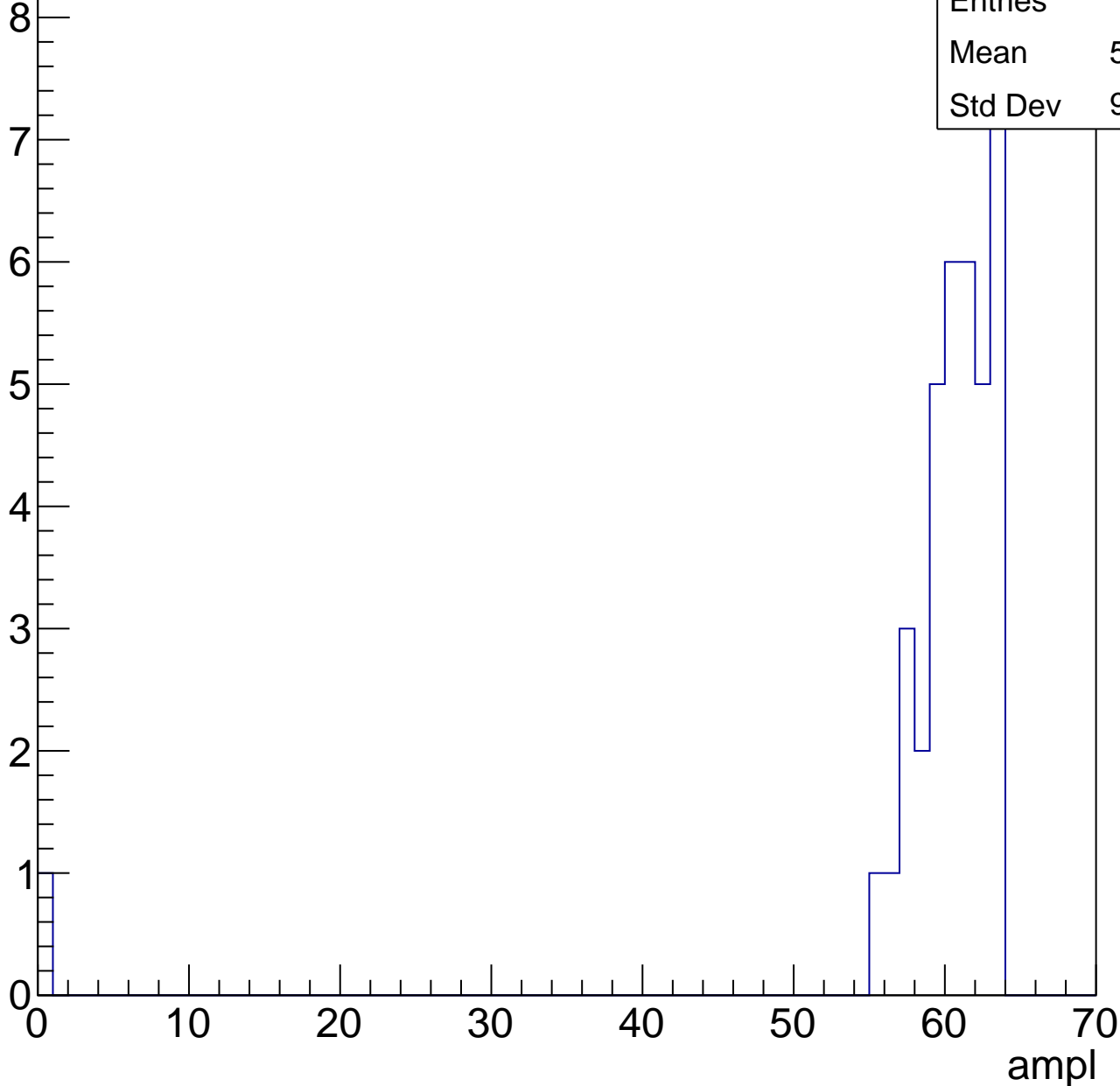


# B1L102S, U8-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

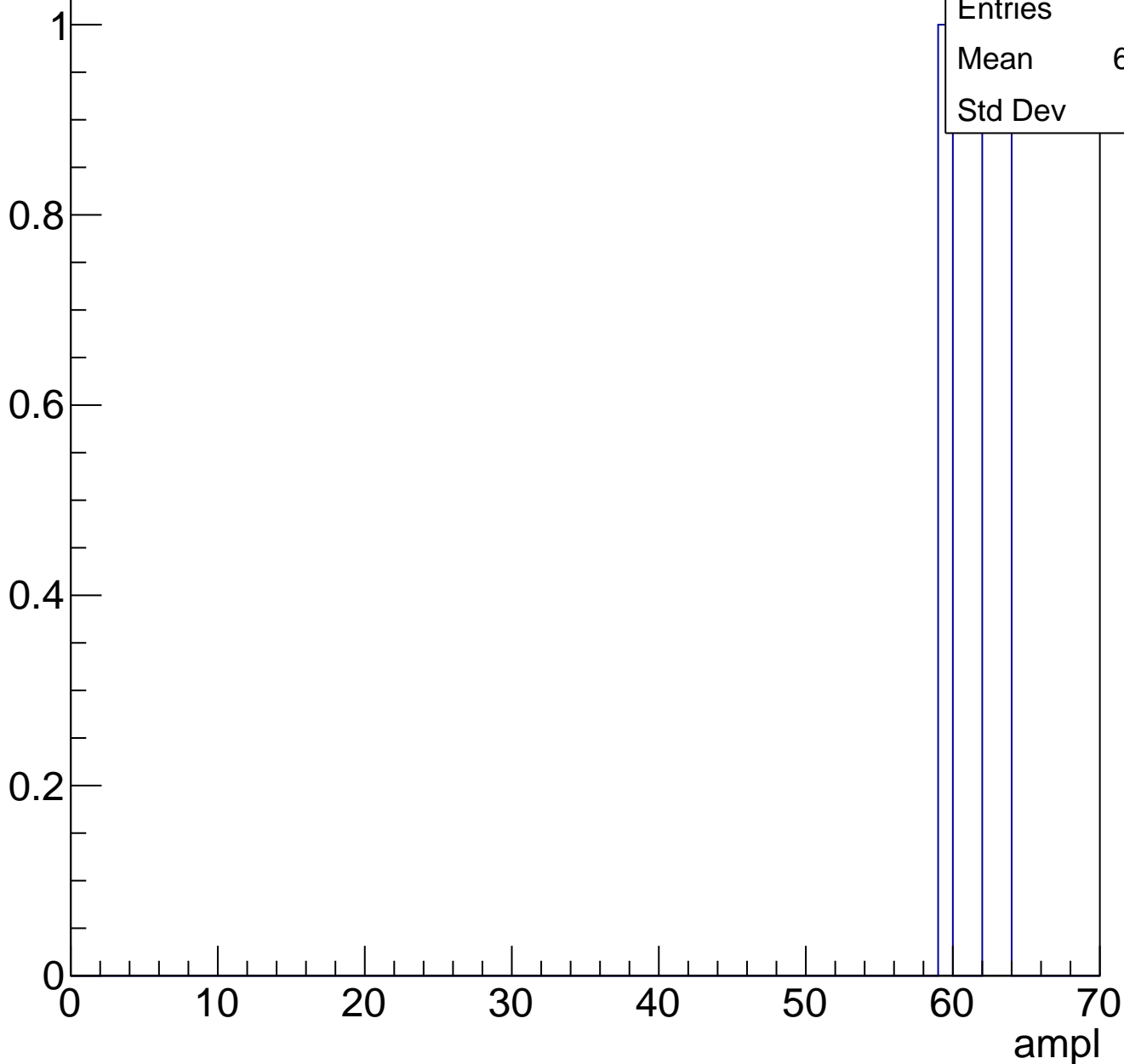
Entries	38
Mean	58.76
Std Dev	9.895



# B1L102S, U8-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch74, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

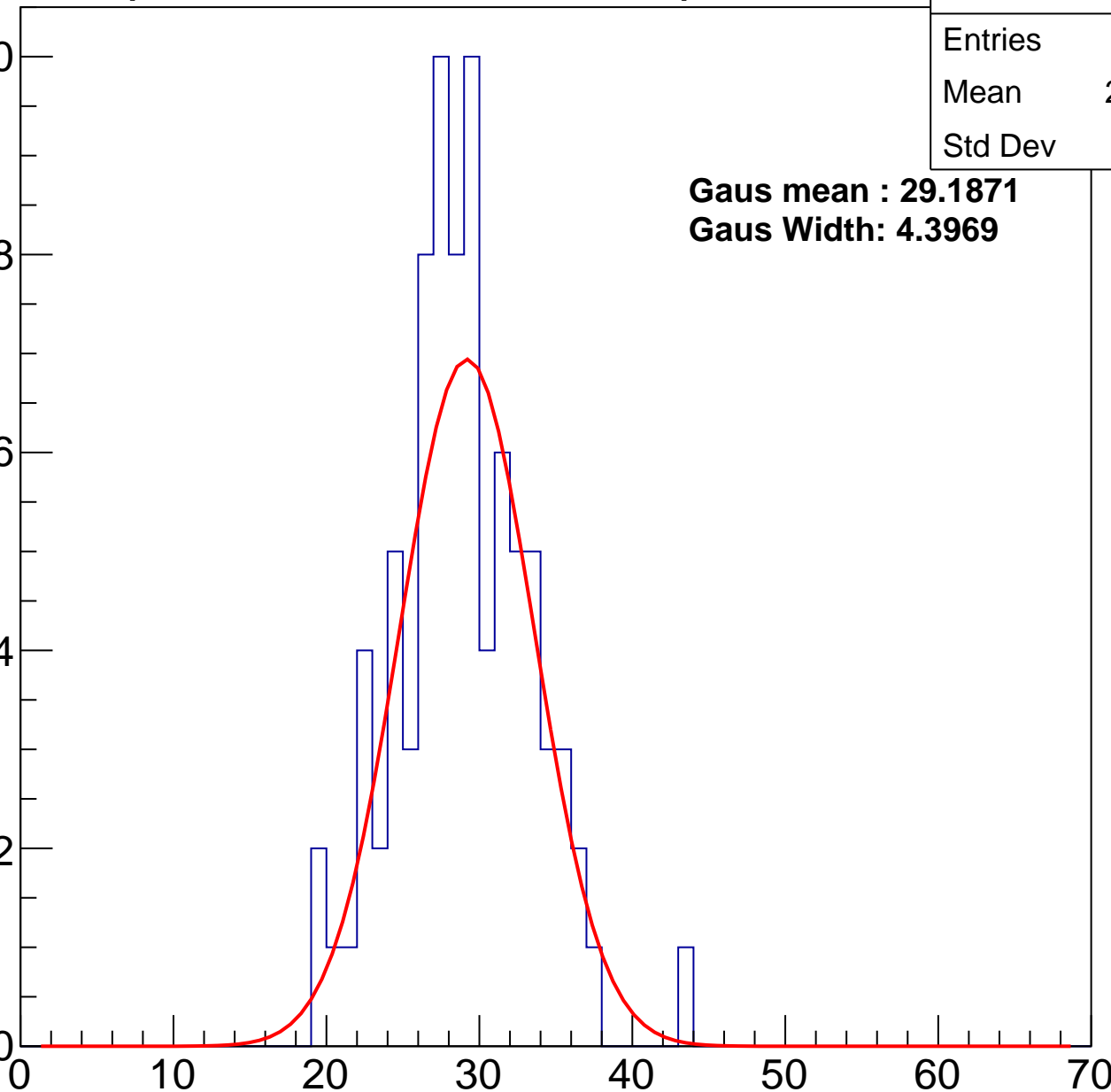
Entries	84
Mean	28.45
Std Dev	4.33

**Gaus mean : 29.1871**

**Gaus Width: 4.3969**

10  
8  
6  
4  
2  
0

ampl



# B1L102S, U8-ch74, adc1

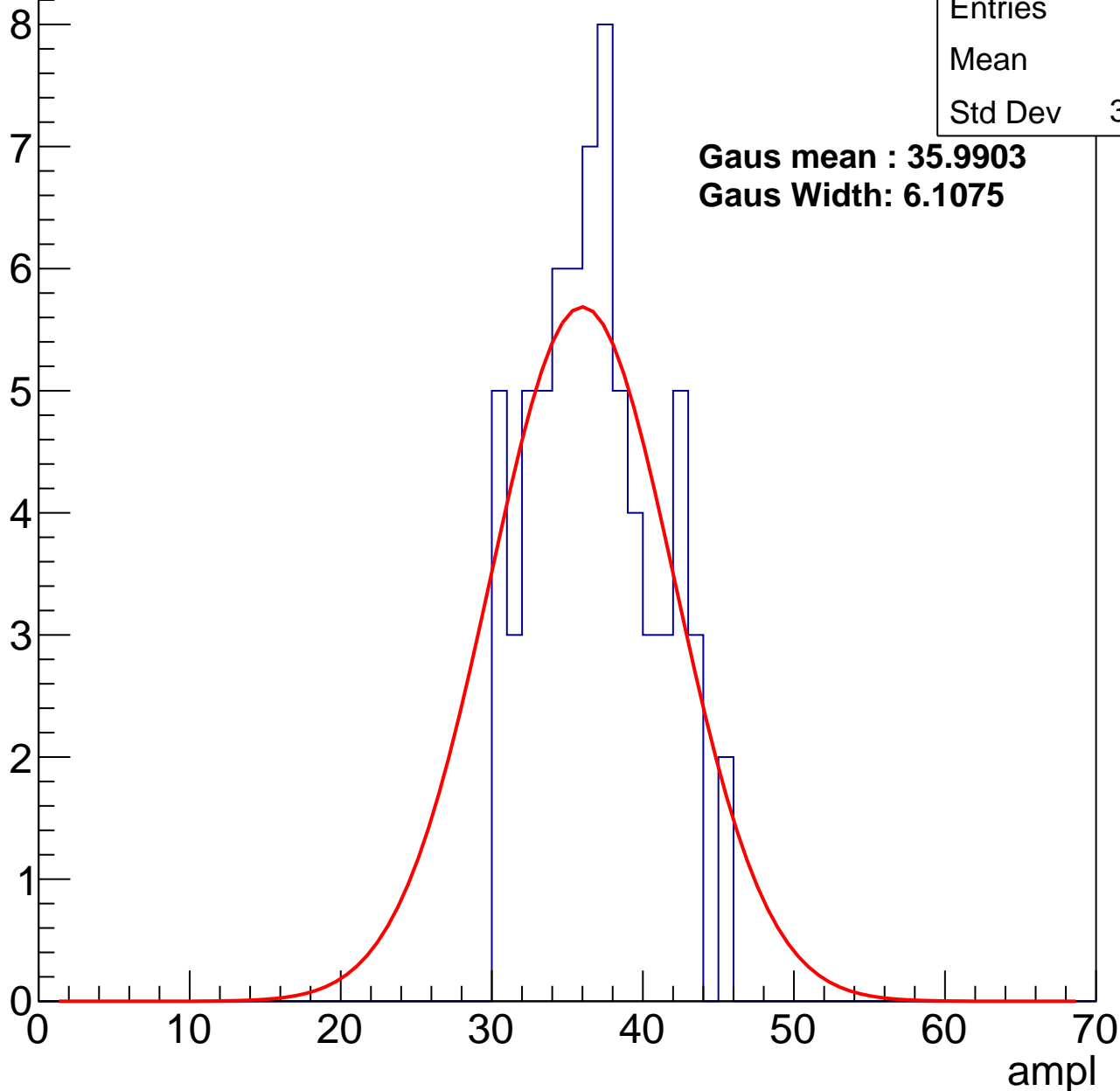
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	36.4
Std Dev	3.918

**Gaus mean : 35.9903**

**Gaus Width: 6.1075**



# B1L102S, U8-ch74, adc2

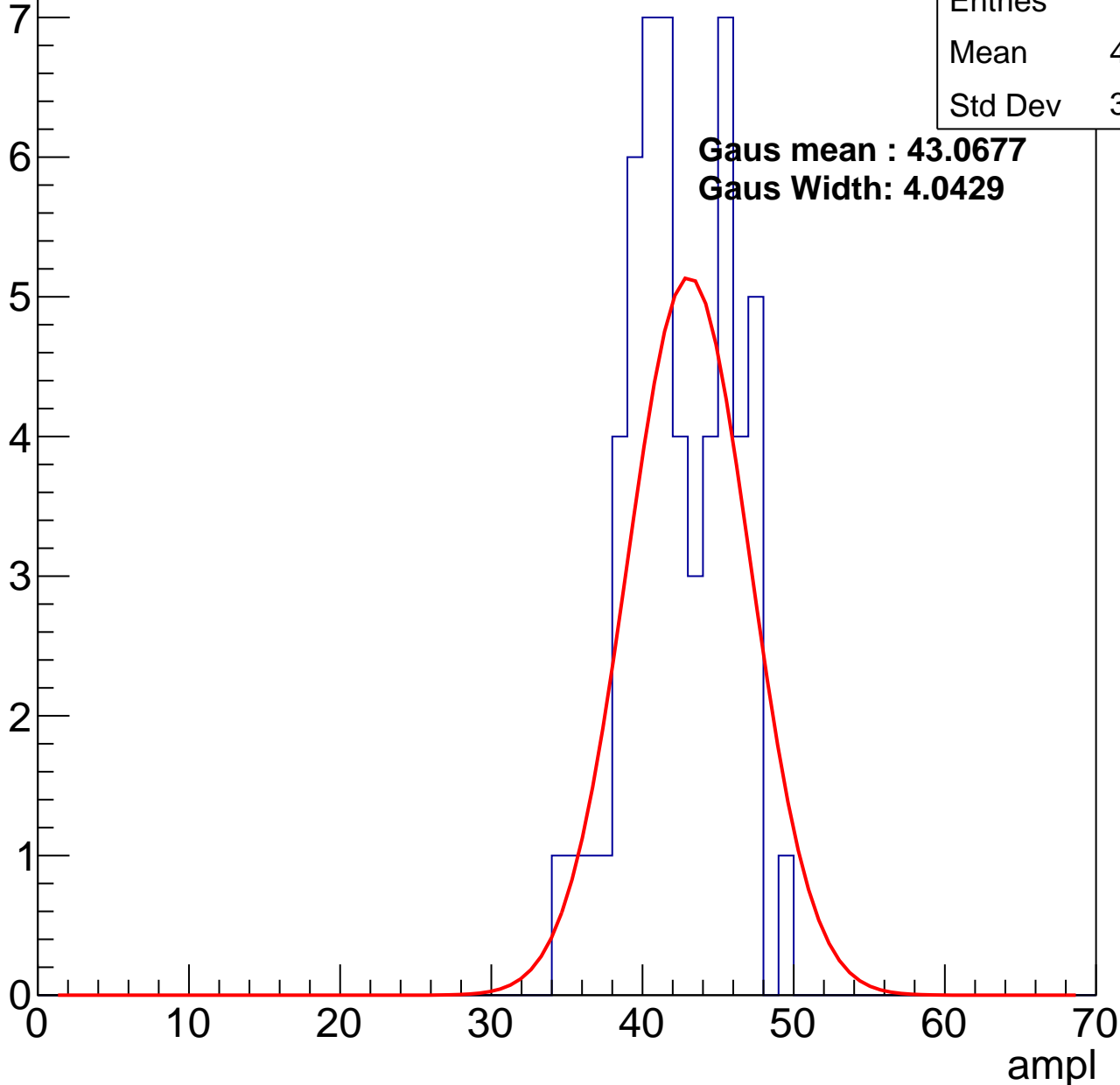
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	41.98
Std Dev	3.399

**Gaus mean : 43.0677**

**Gaus Width: 4.0429**

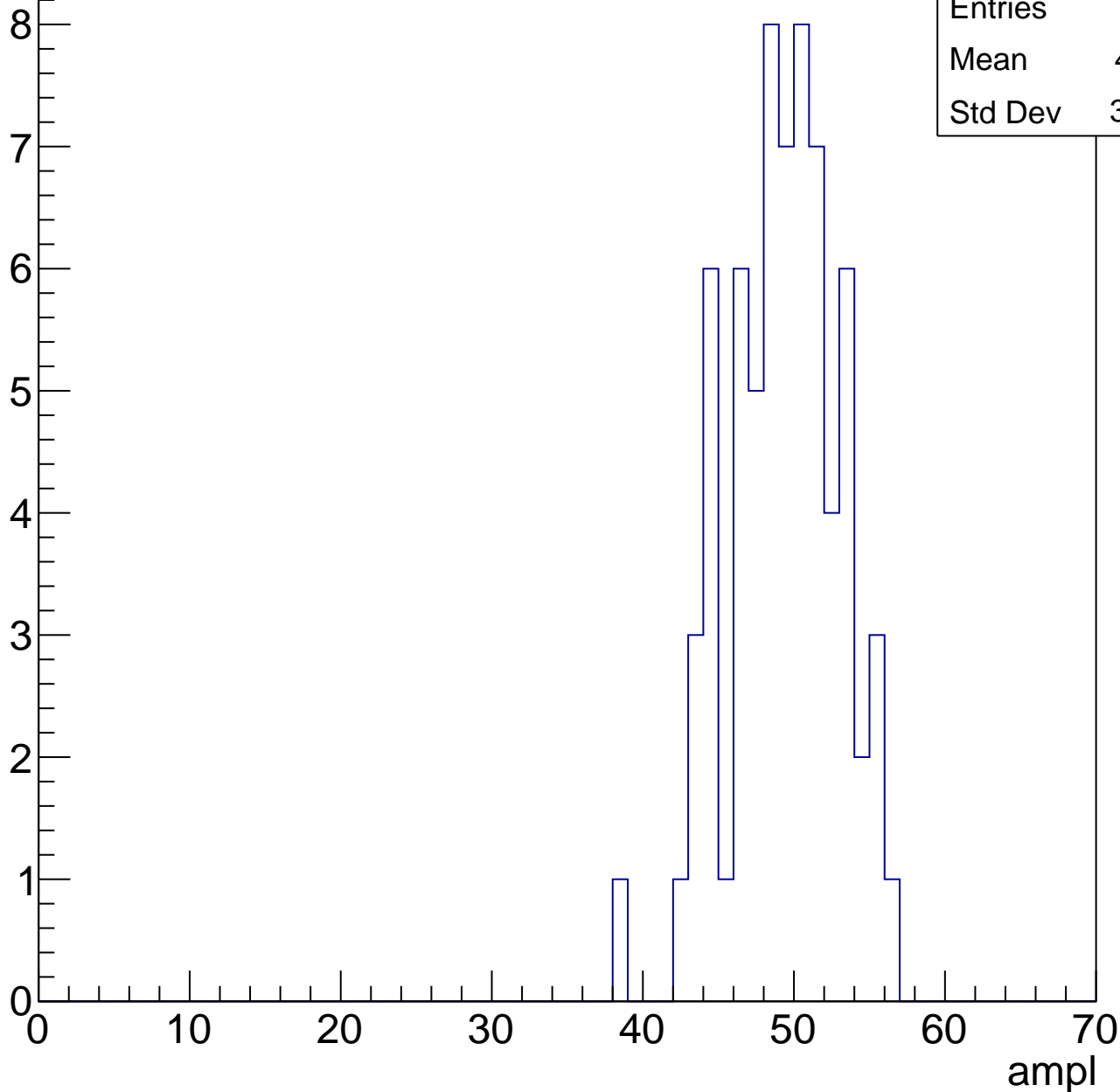


# B1L102S, U8-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	48.81
Std Dev	3.609

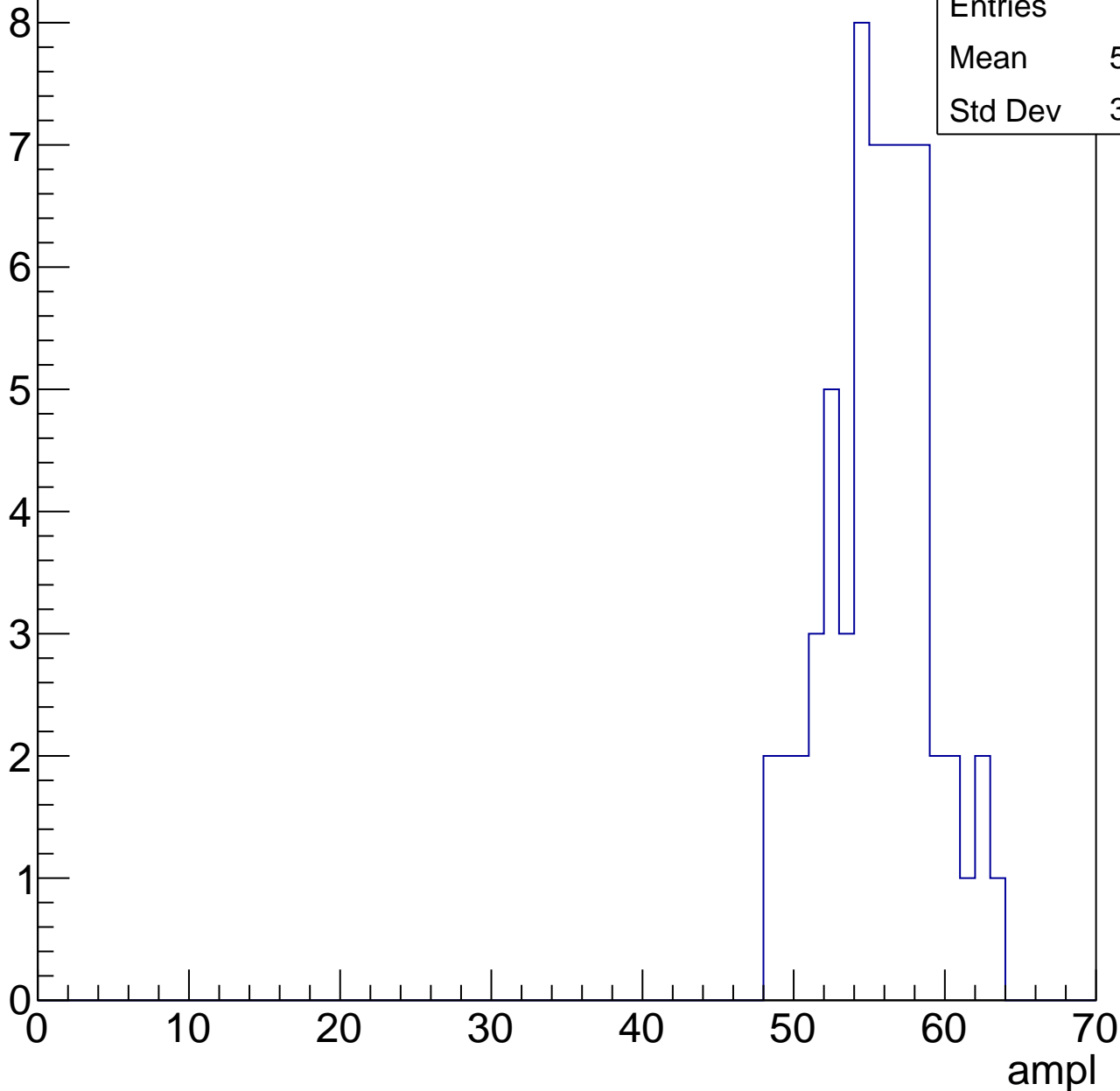


# B1L102S, U8-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	55.18
Std Dev	3.409

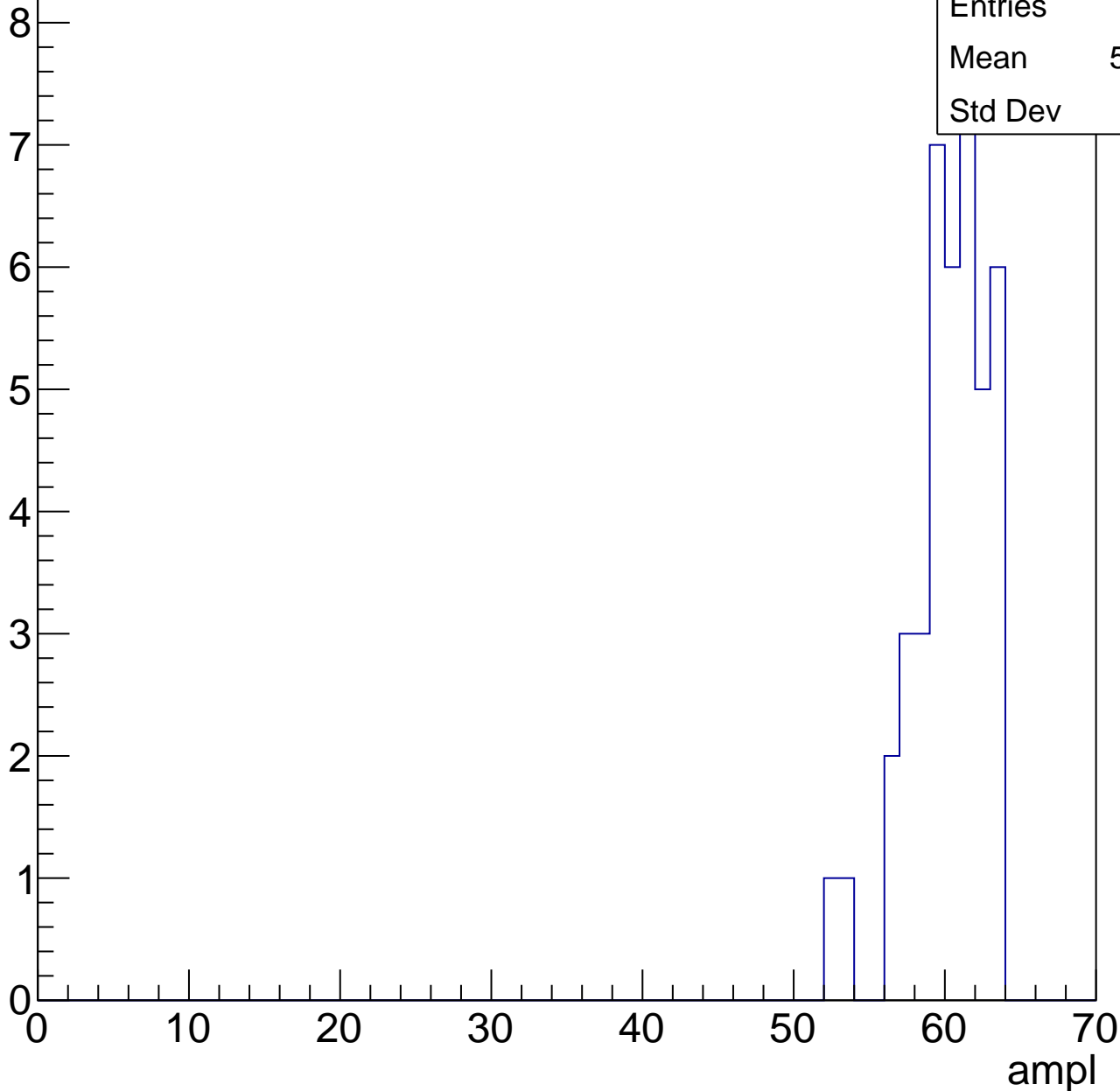


# B1L102S, U8-ch74, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

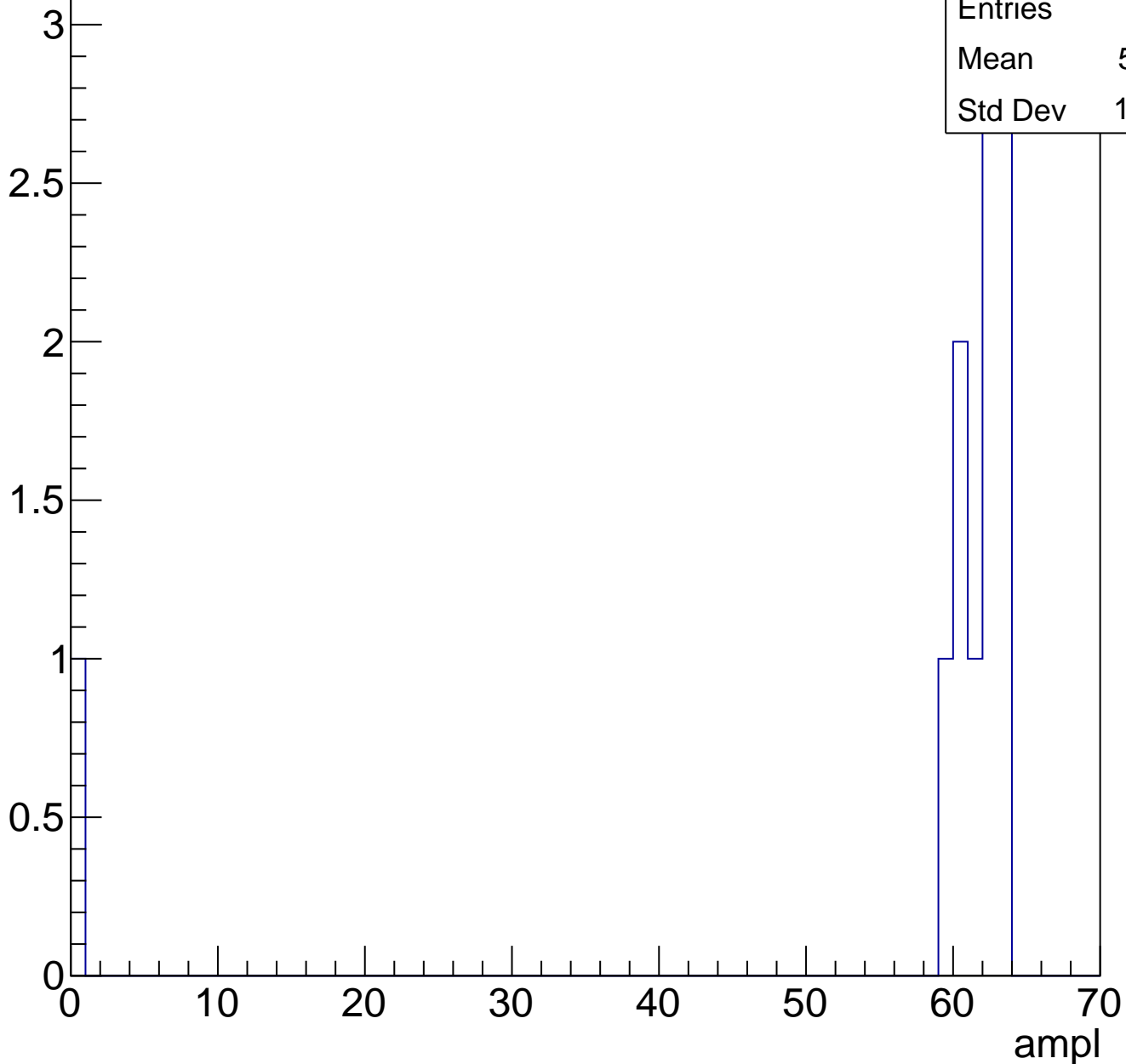
Entries	42
Mean	59.79
Std Dev	2.54



# B1L102S, U8-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	11
Mean	55.91
Std Dev	17.73



# B1L102S, U8-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch75, adc0

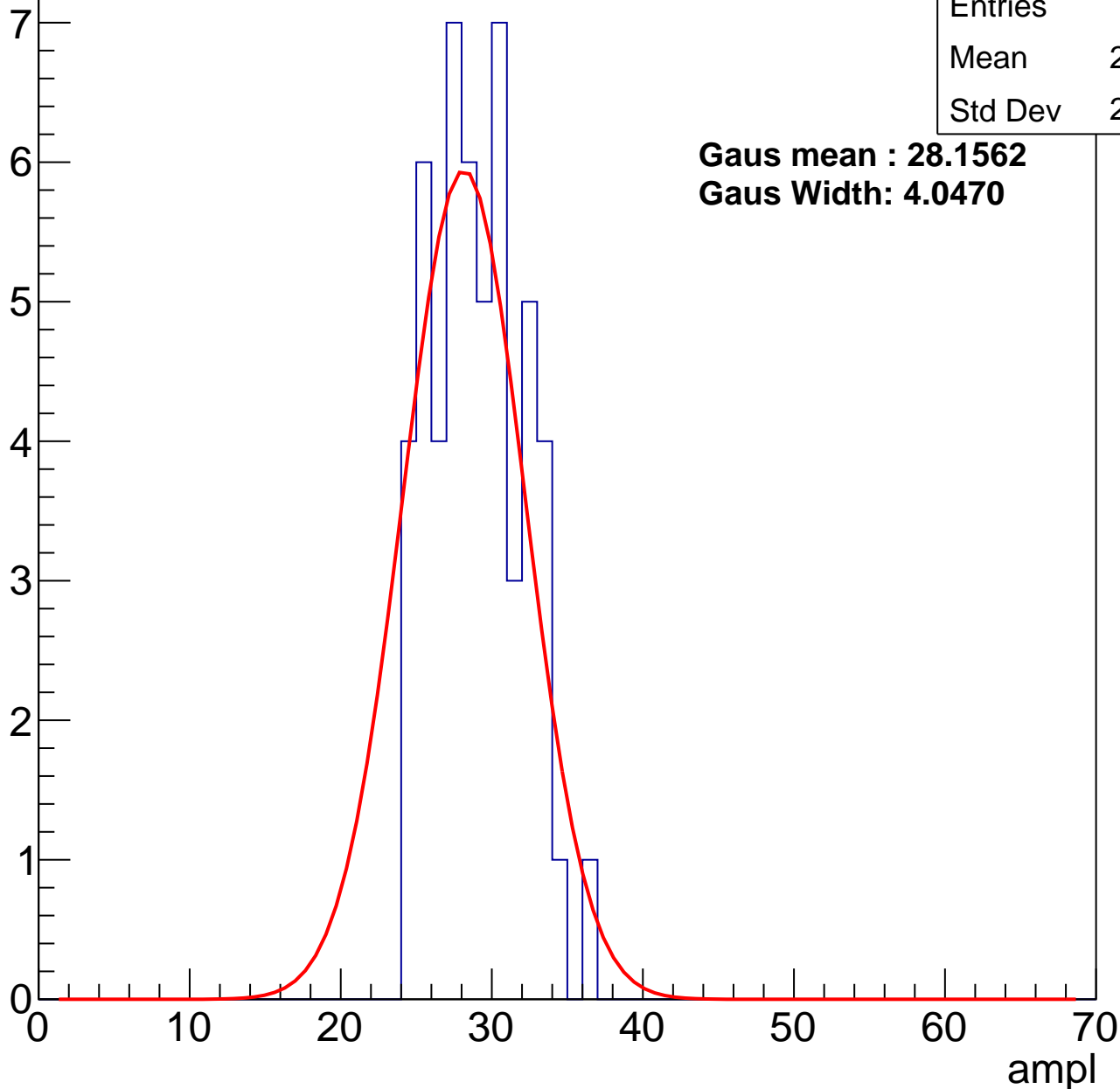
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	28.62
Std Dev	2.948

**Gaus mean : 28.1562**

**Gaus Width: 4.0470**



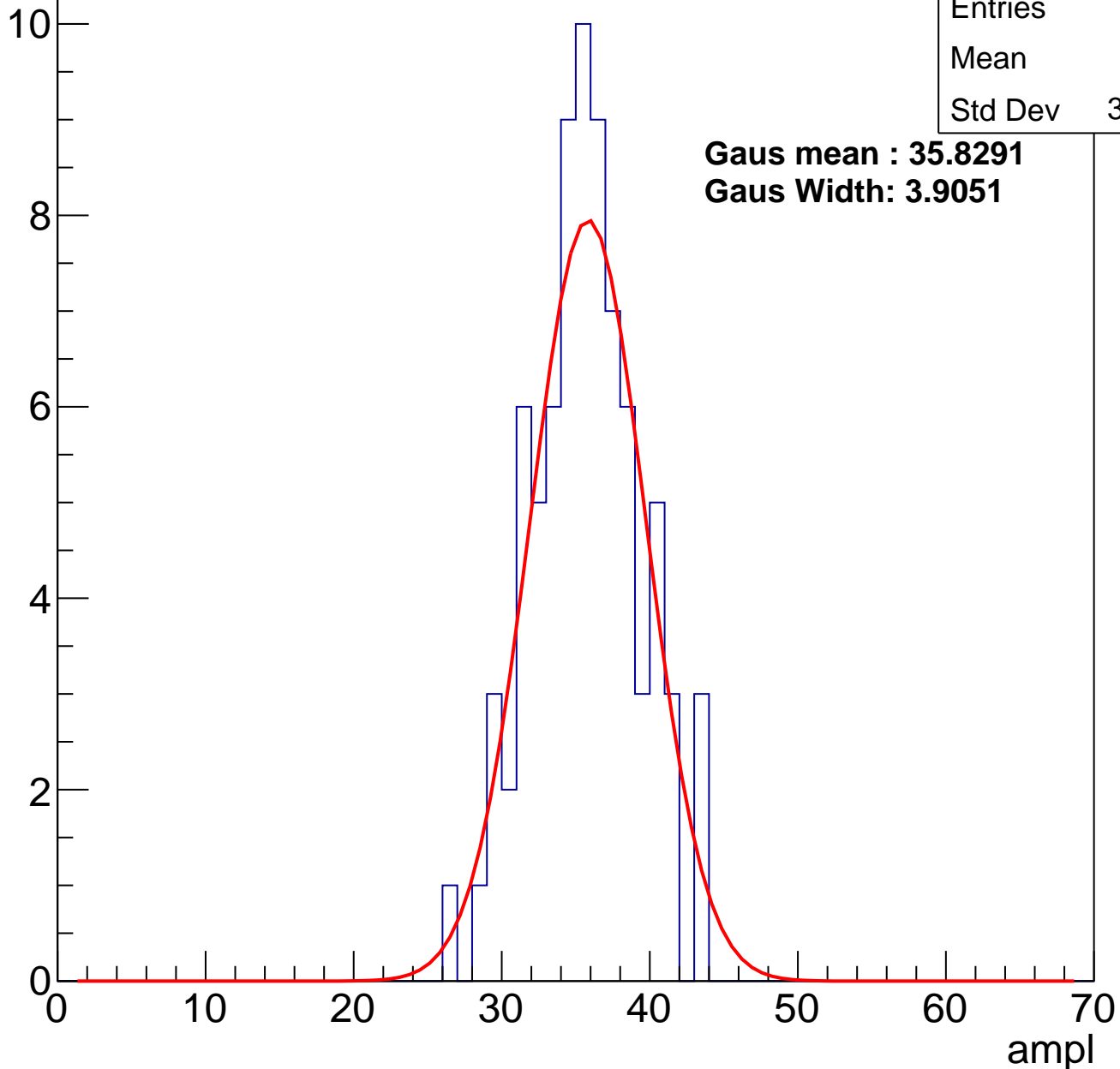
# B1L102S, U8-ch75, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	79
Mean	35.2
Std Dev	3.598

**Gaus mean : 35.8291**  
**Gaus Width: 3.9051**

Entry



# B1L102S, U8-ch75, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	70
Mean	43.07
Std Dev	3.465

**Gaus mean : 42.8783**

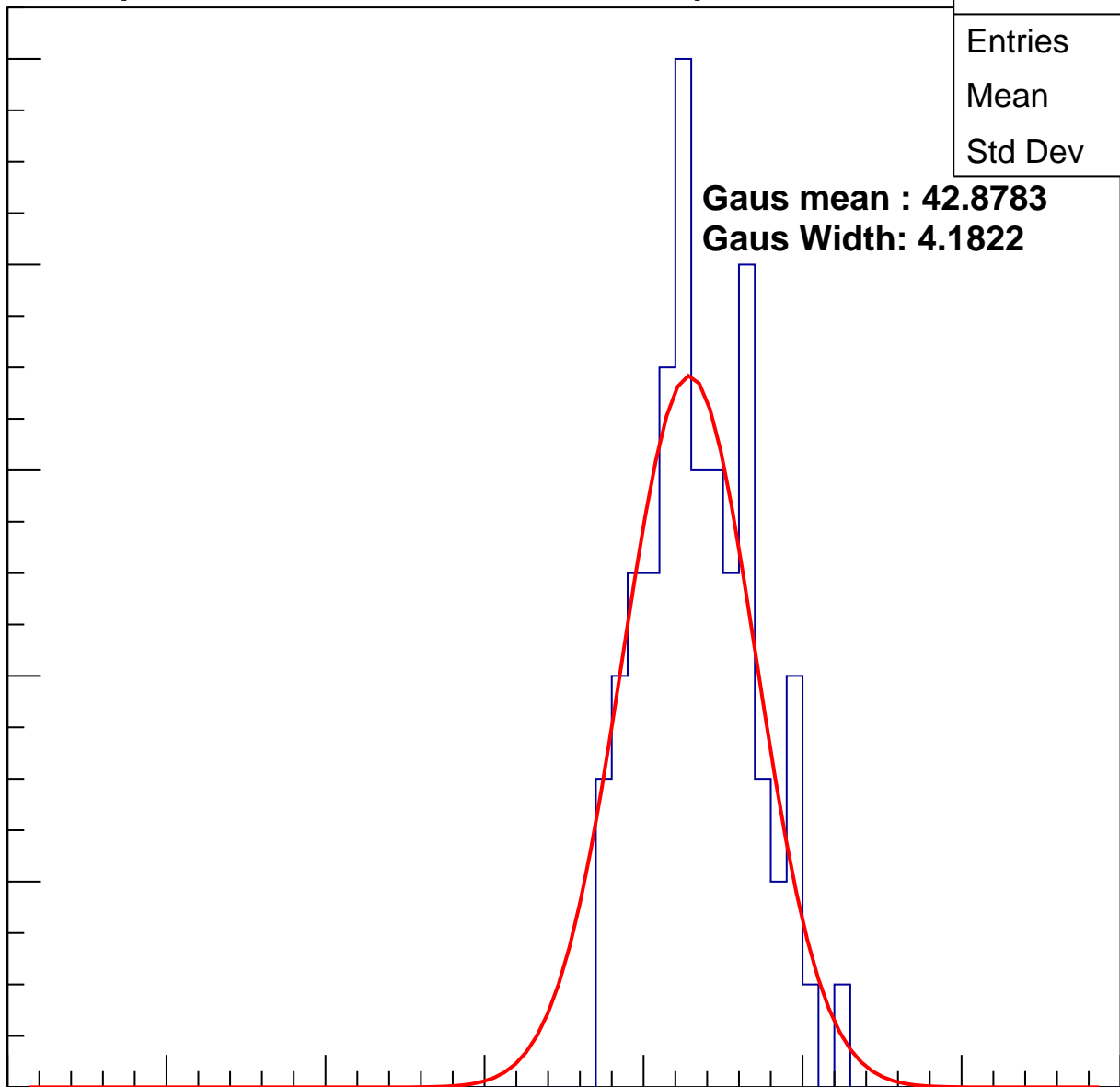
**Gaus Width: 4.1822**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

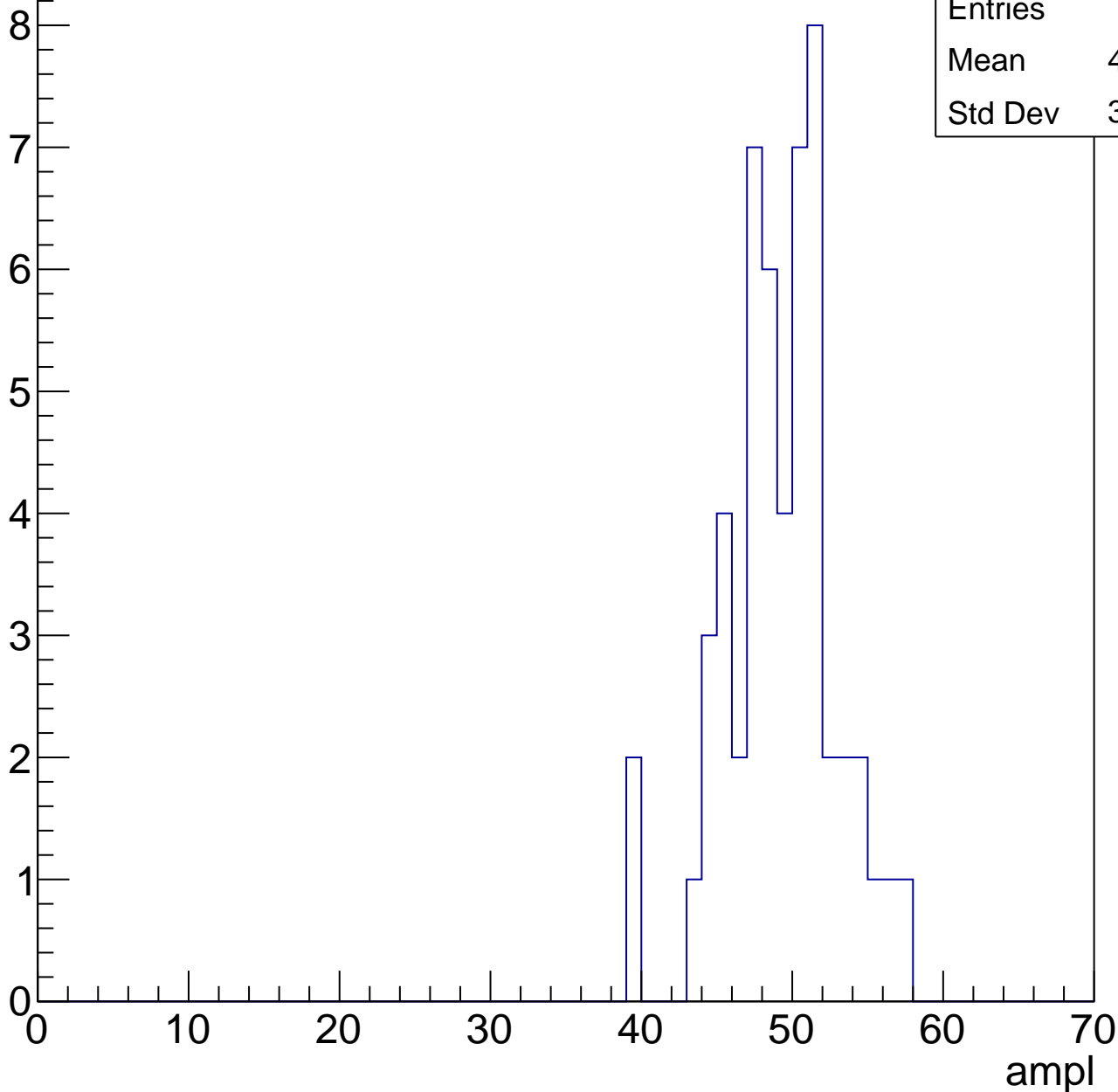


# B1L102S, U8-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	48.72
Std Dev	3.662

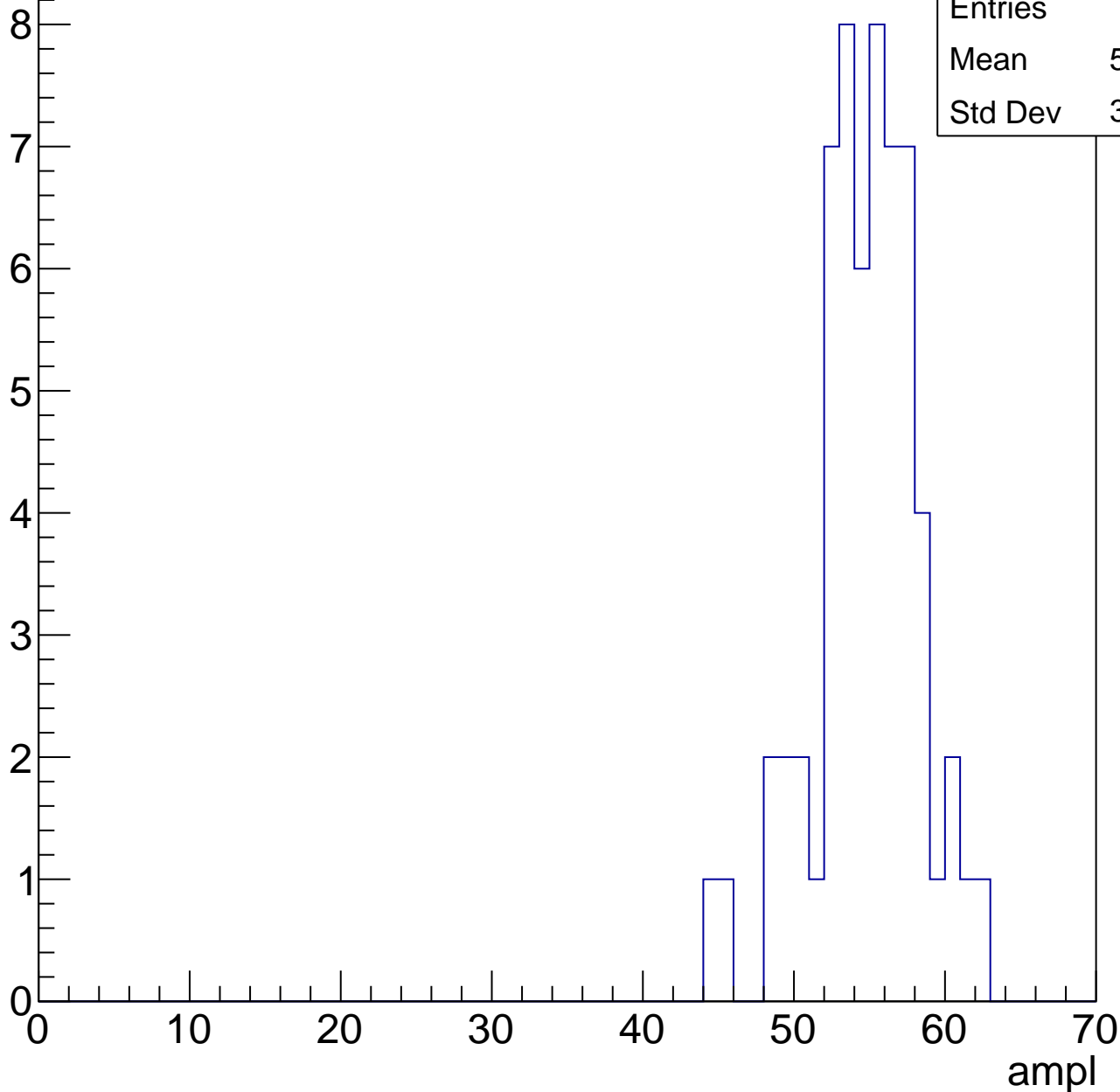


# B1L102S, U8-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

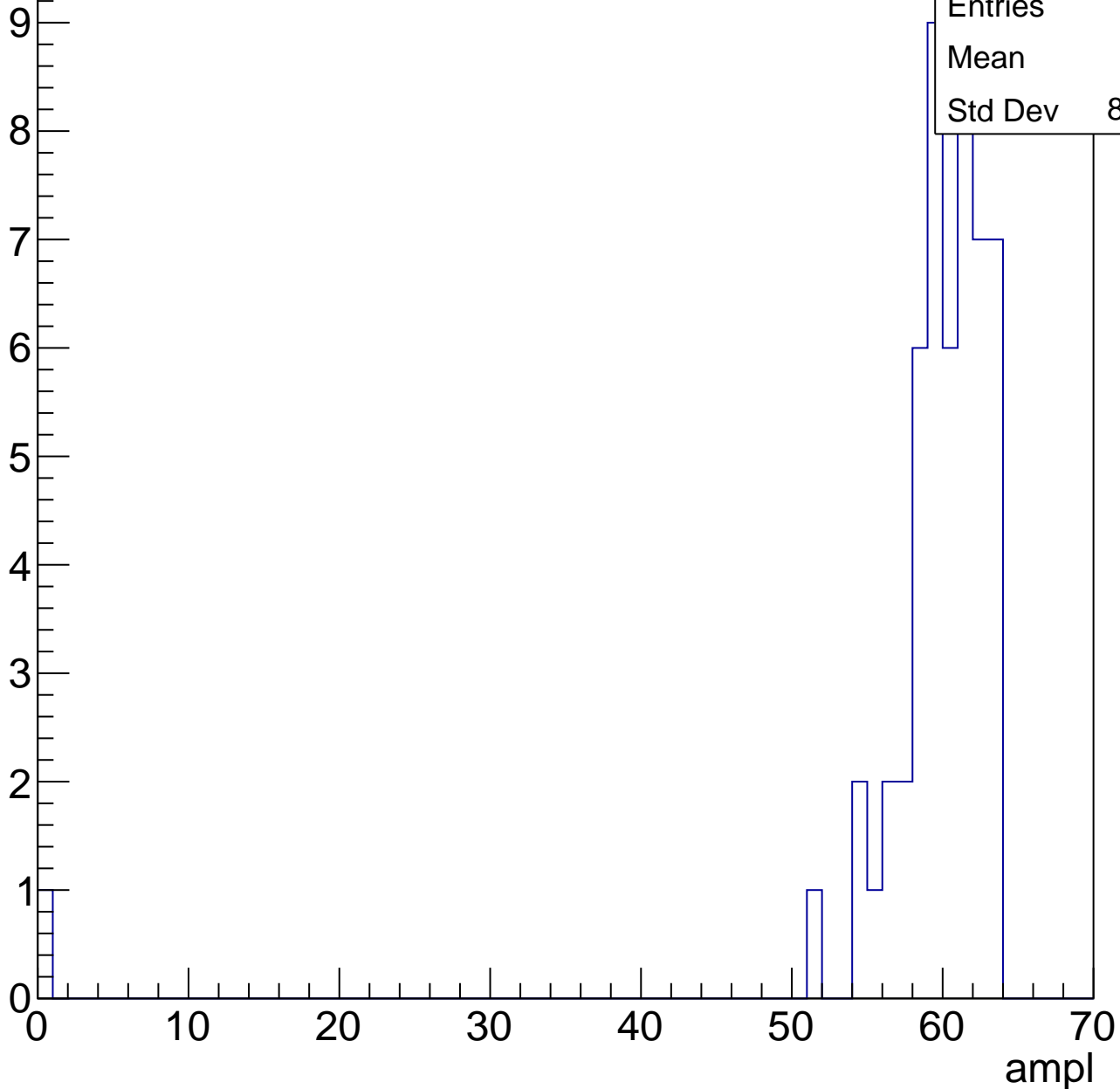
Entries	61
Mean	54.28
Std Dev	3.502



# B1L102S, U8-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

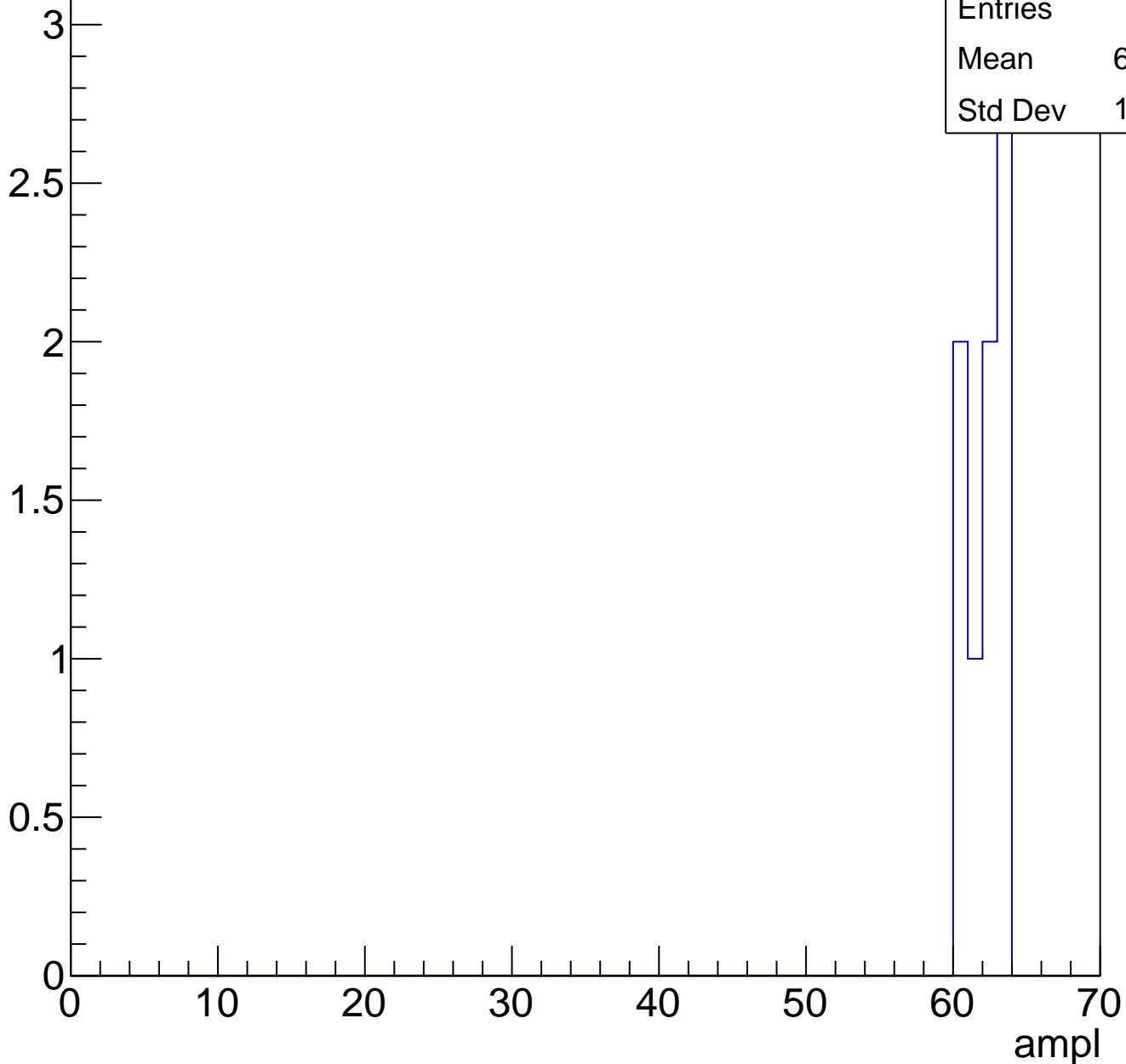
Entry



# B1L102S, U8-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch76, adc0

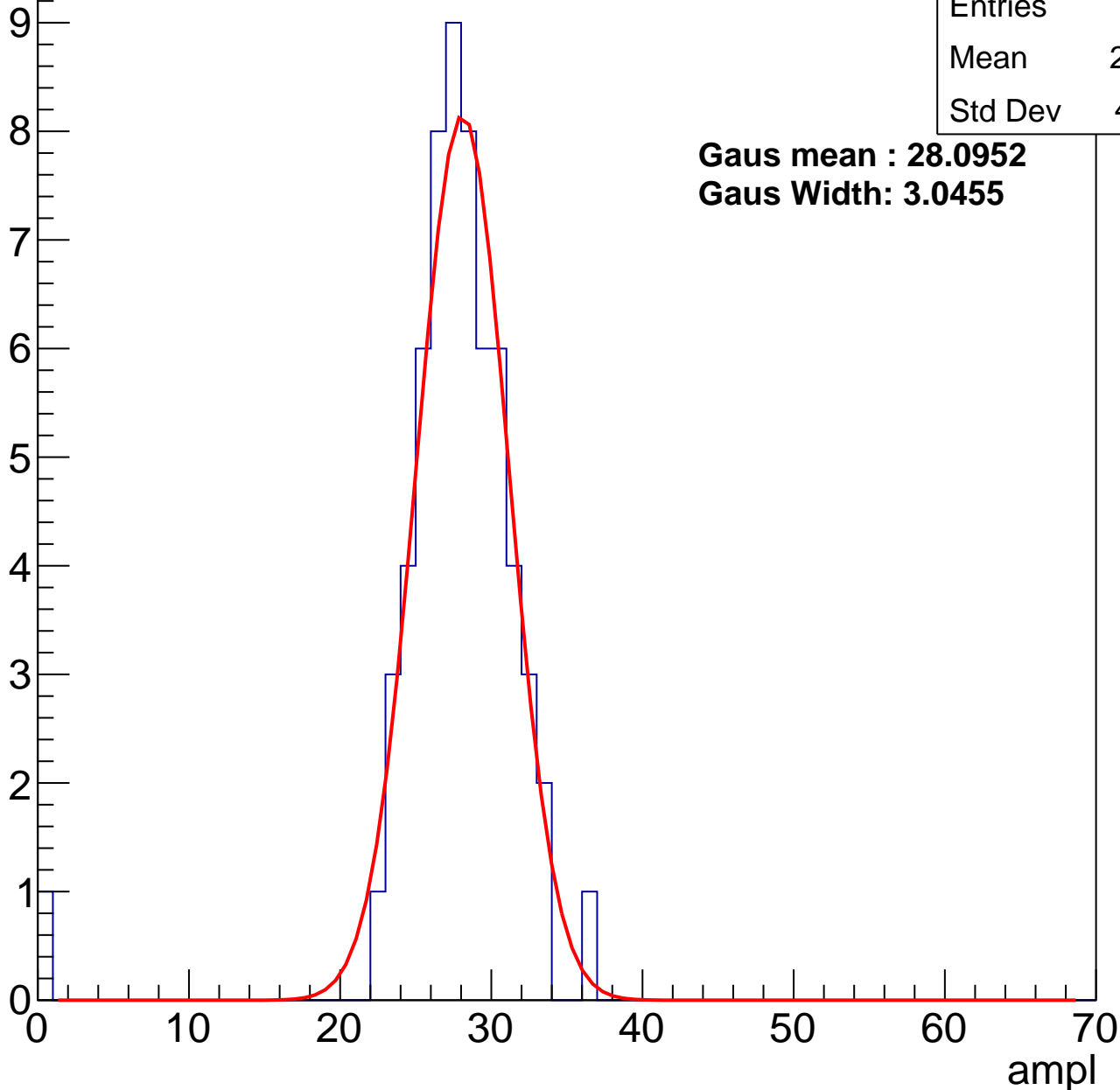
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	27.23
Std Dev	4.481

**Gaus mean : 28.0952**

**Gaus Width: 3.0455**



# B1L102S, U8-ch76, adc1

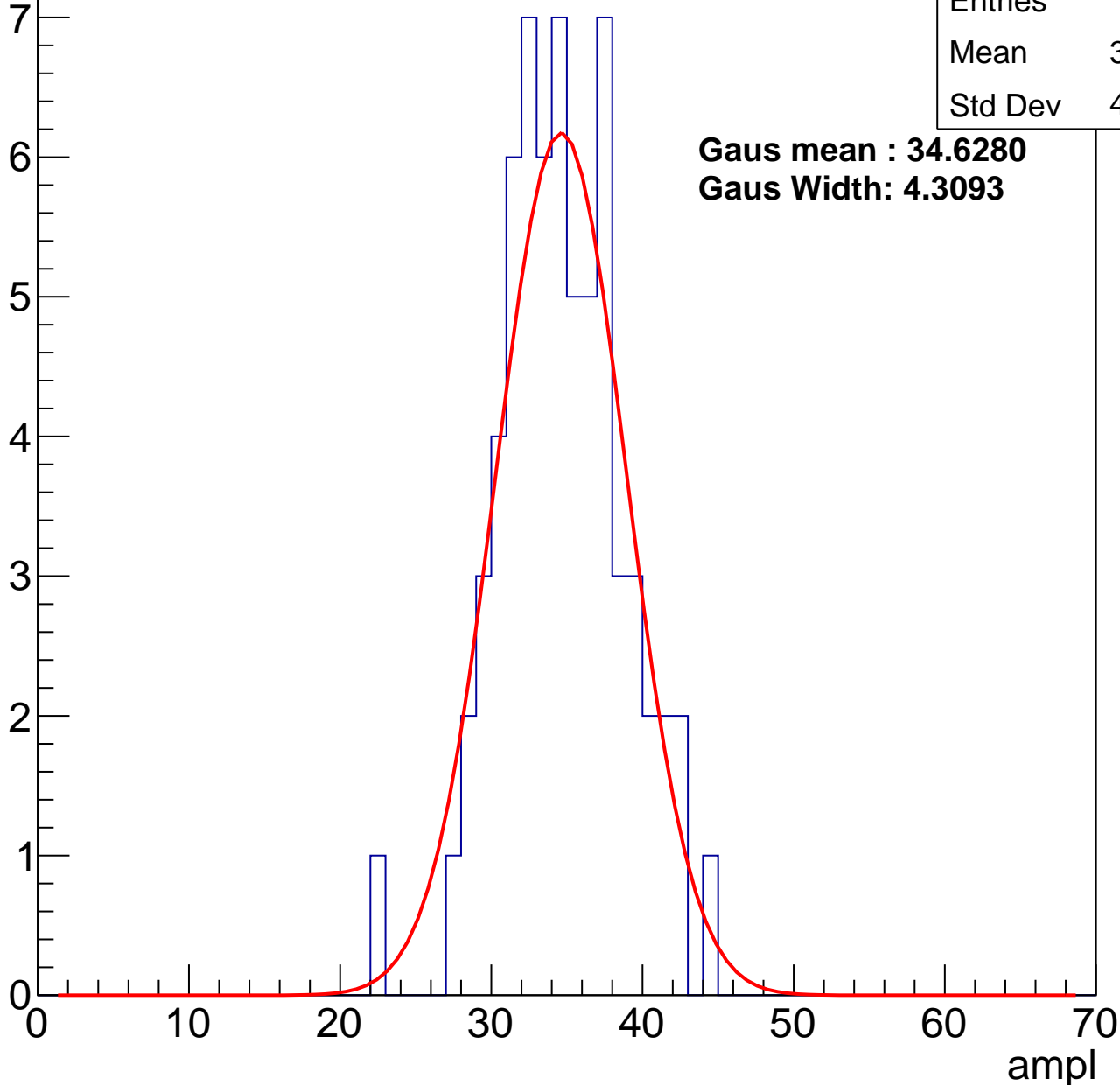
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	34.22
Std Dev	4.048

**Gaus mean : 34.6280**

**Gaus Width: 4.3093**



# B1L102S, U8-ch76, adc2

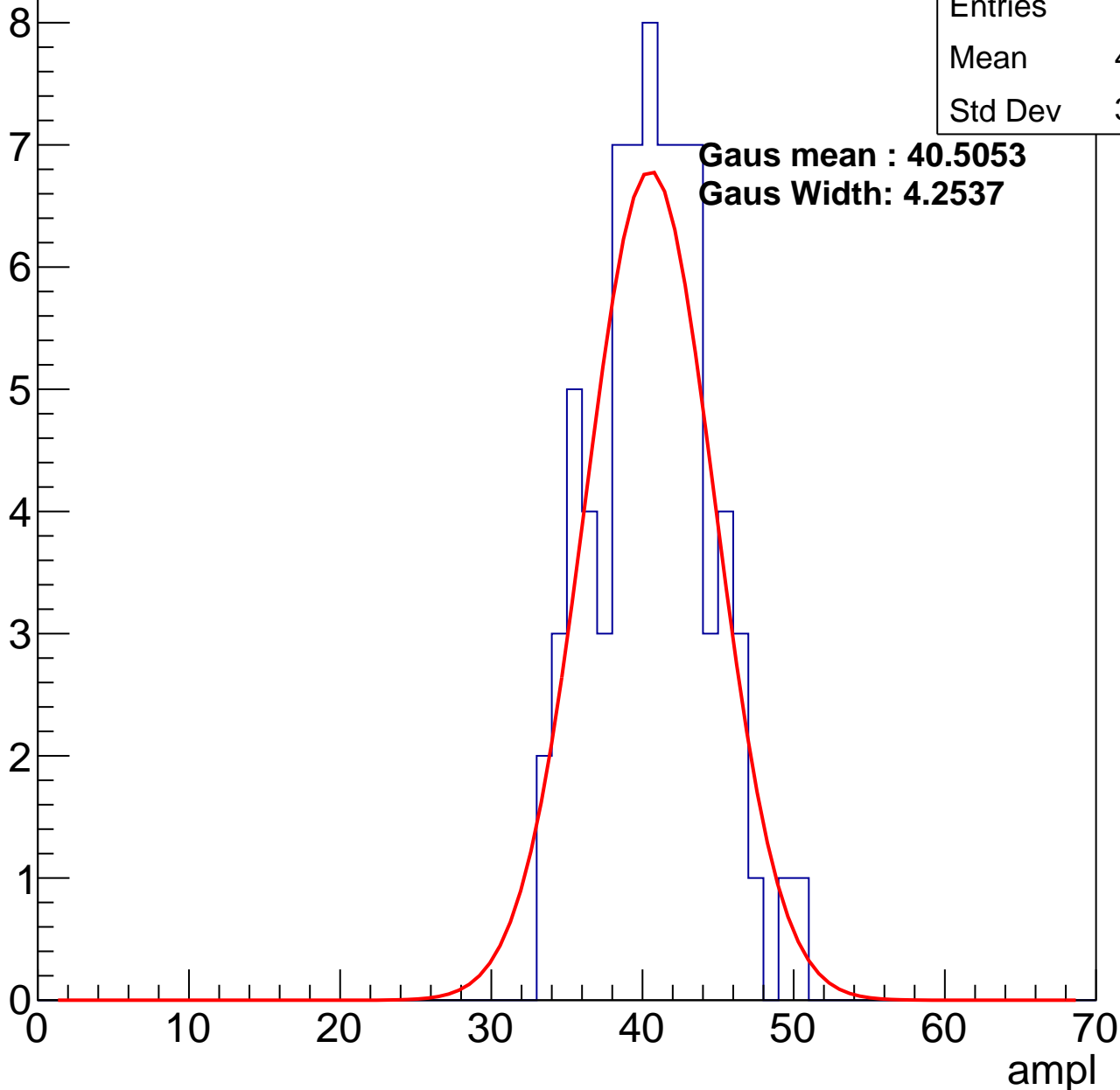
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	40.21
Std Dev	3.771

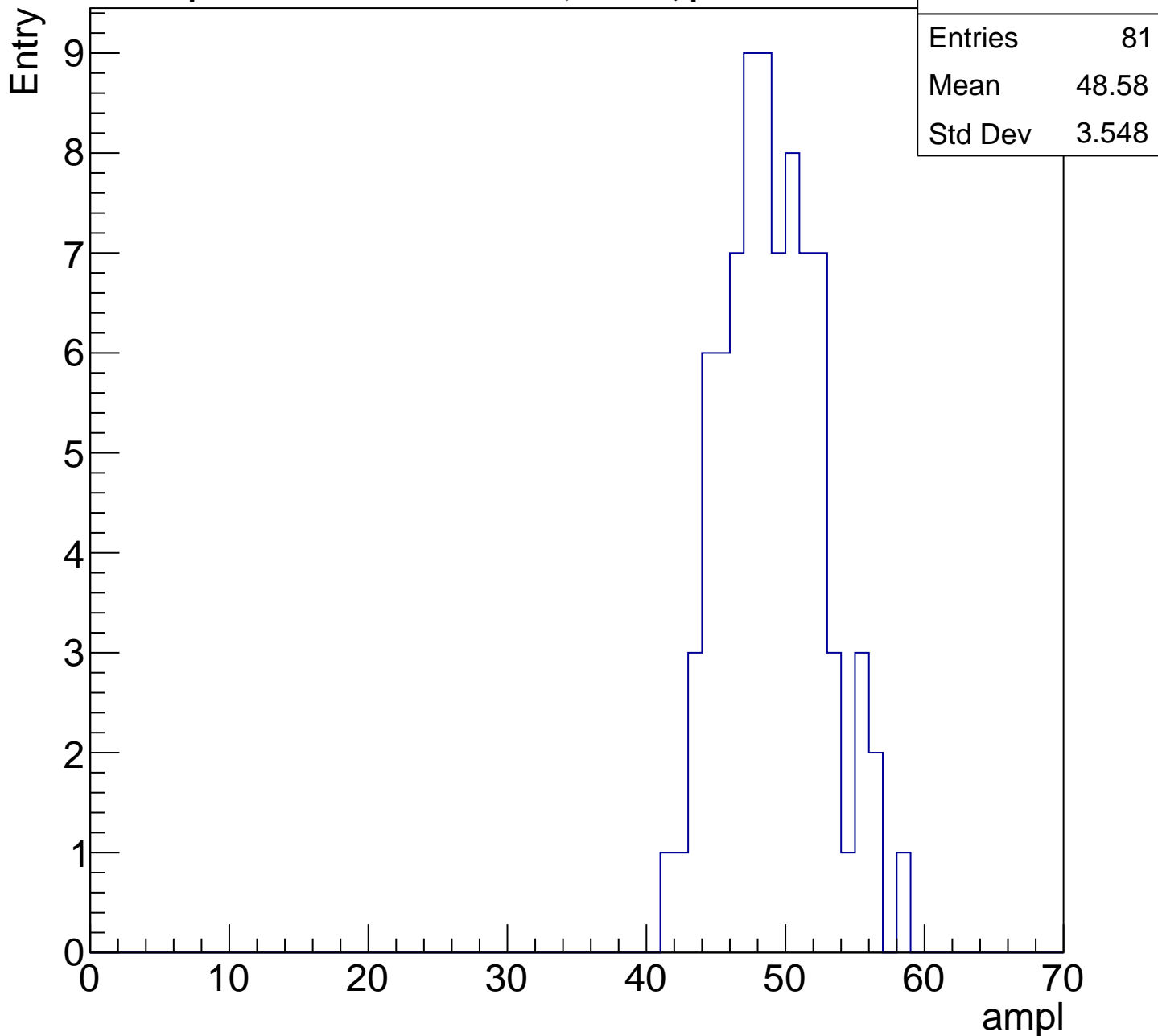
**Gaus mean : 40.5053**

**Gaus Width: 4.2537**



# B1L102S, U8-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

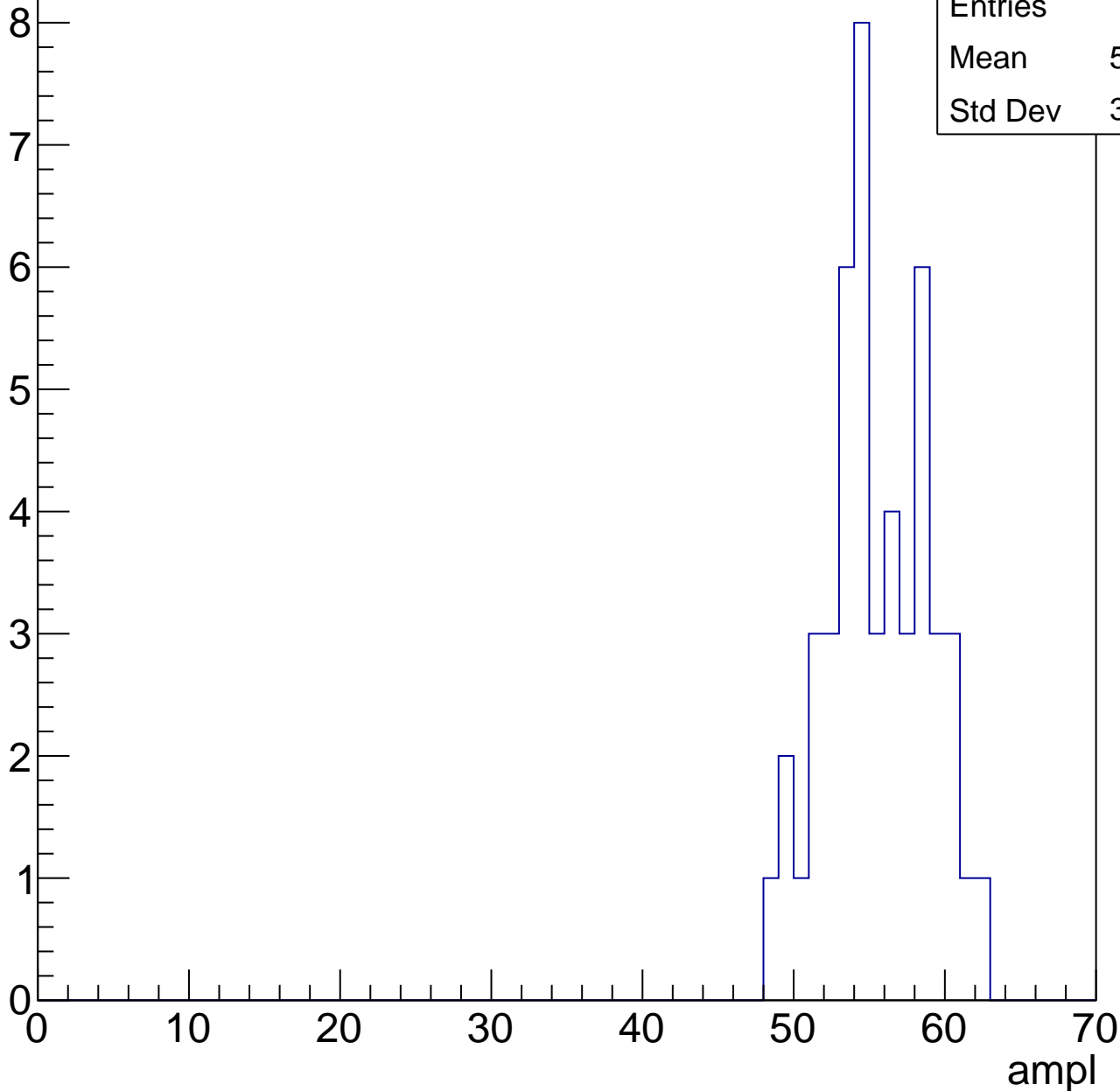


# B1L102S, U8-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	55.06
Std Dev	3.325

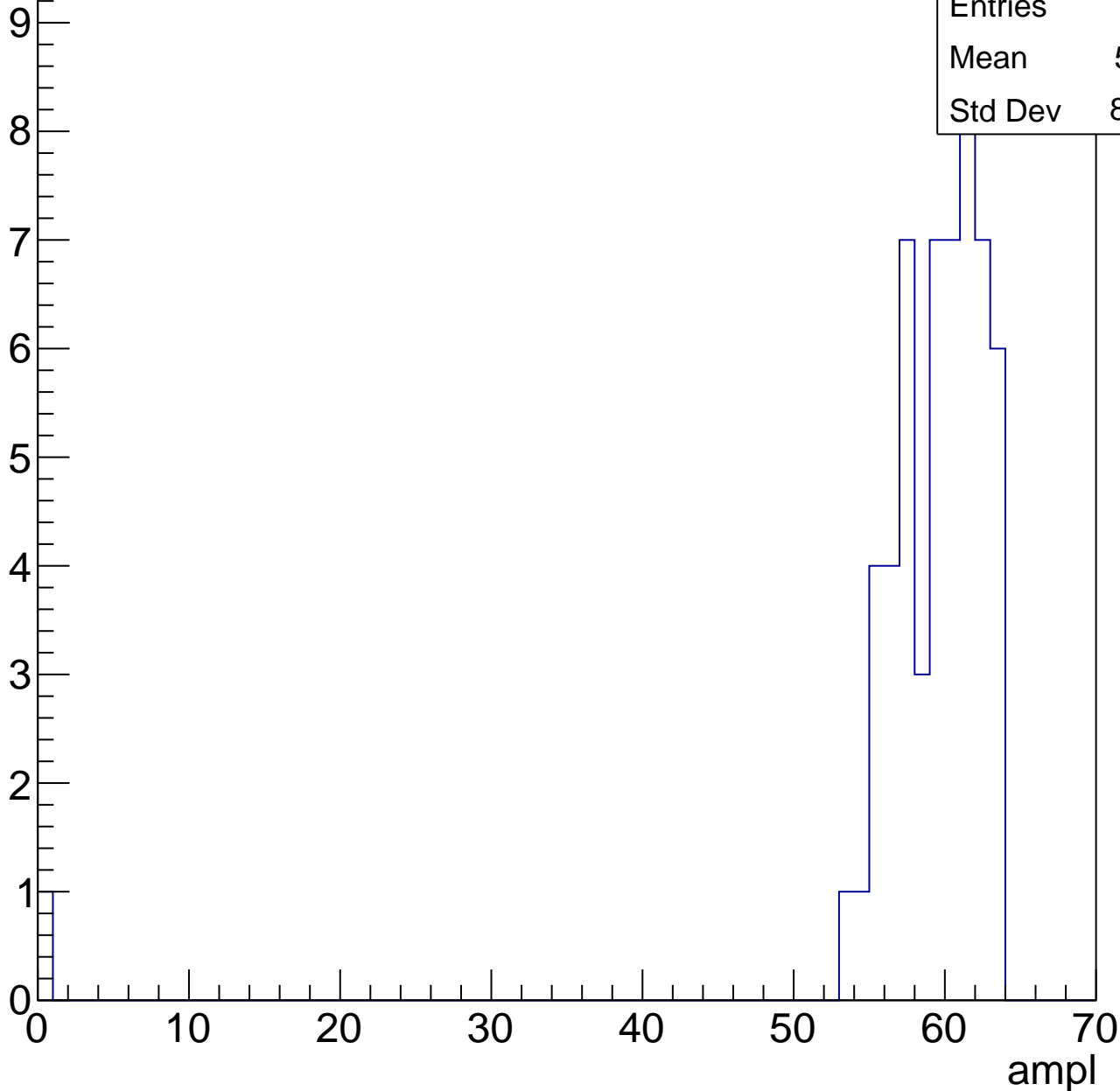


# B1L102S, U8-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

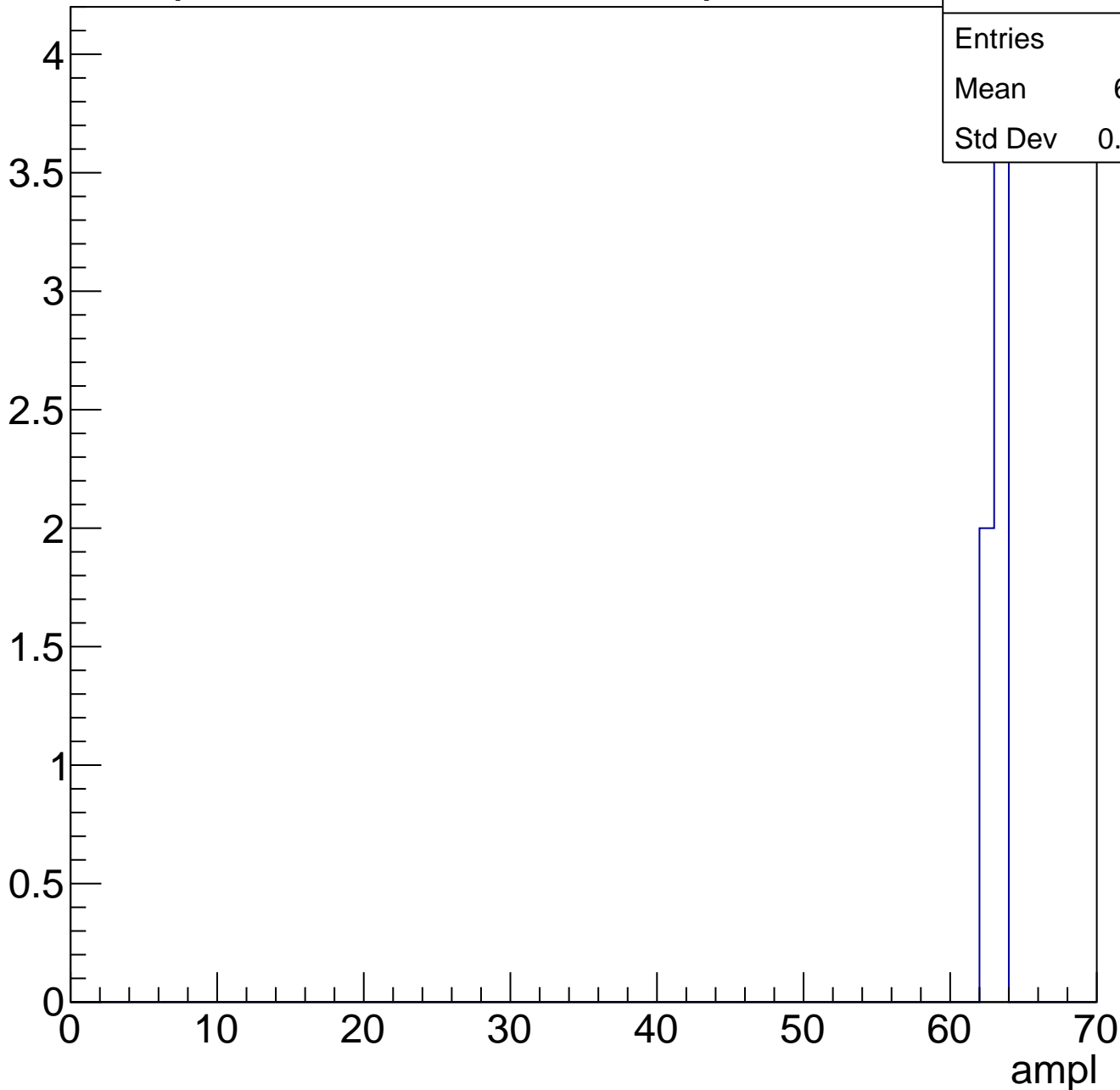
Entries	57
Mean	58.21
Std Dev	8.207



# B1L102S, U8-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch77, adc0

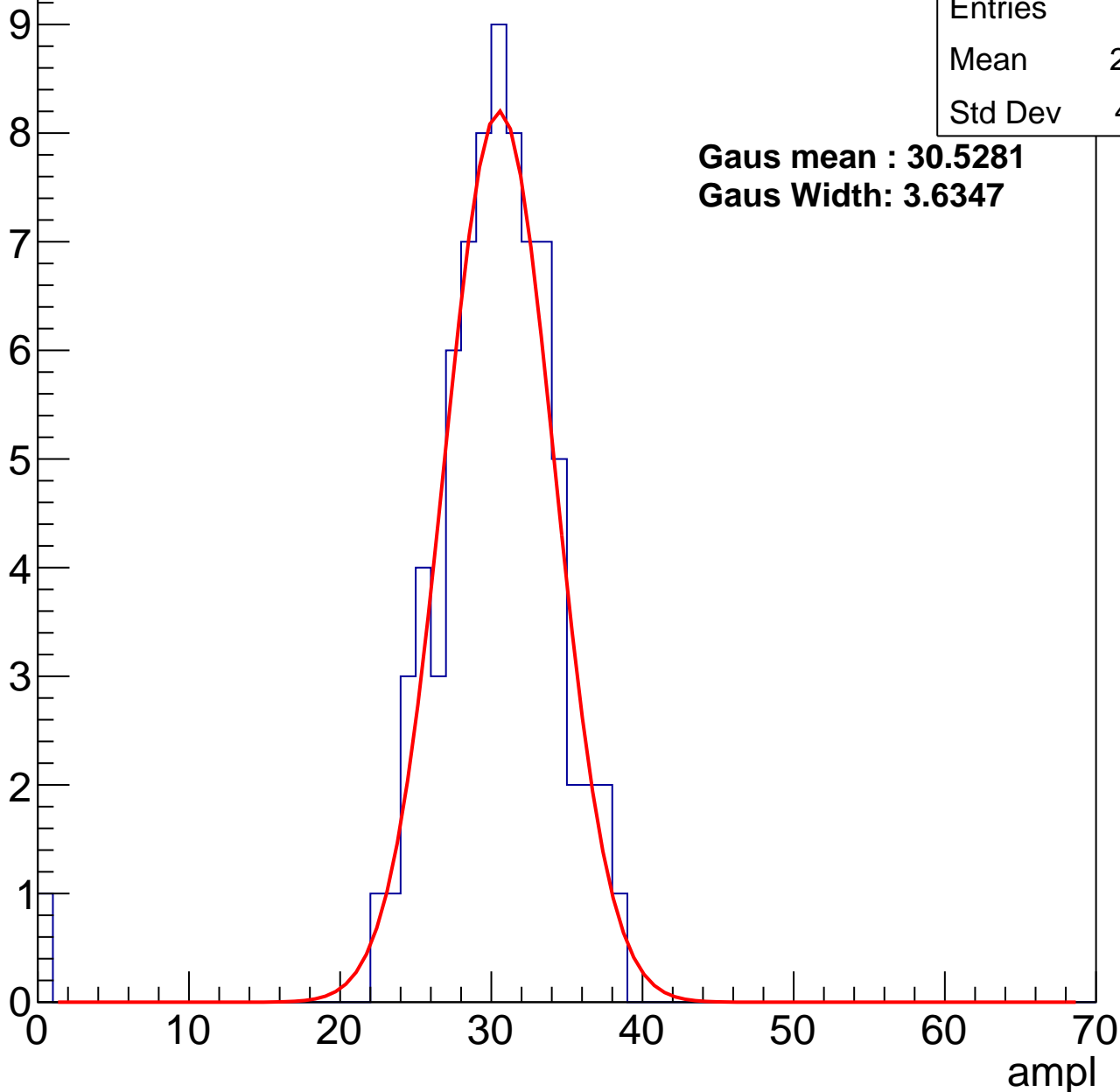
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	29.64
Std Dev	4.851

**Gaus mean : 30.5281**

**Gaus Width: 3.6347**



# B1L102S, U8-ch77, adc1

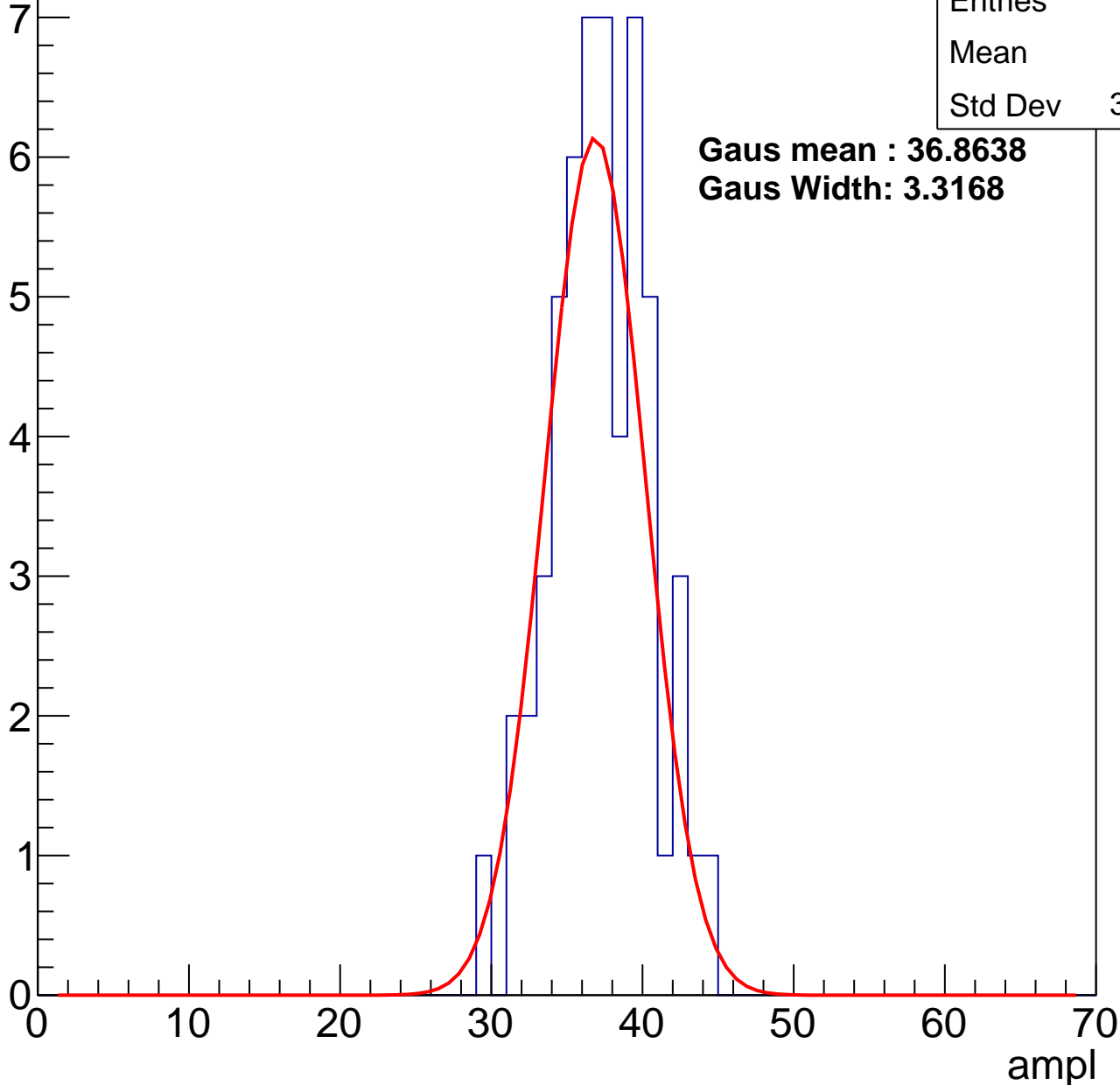
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	36.8
Std Dev	3.193

**Gaus mean : 36.8638**

**Gaus Width: 3.3168**



# B1L102S, U8-ch77, adc2

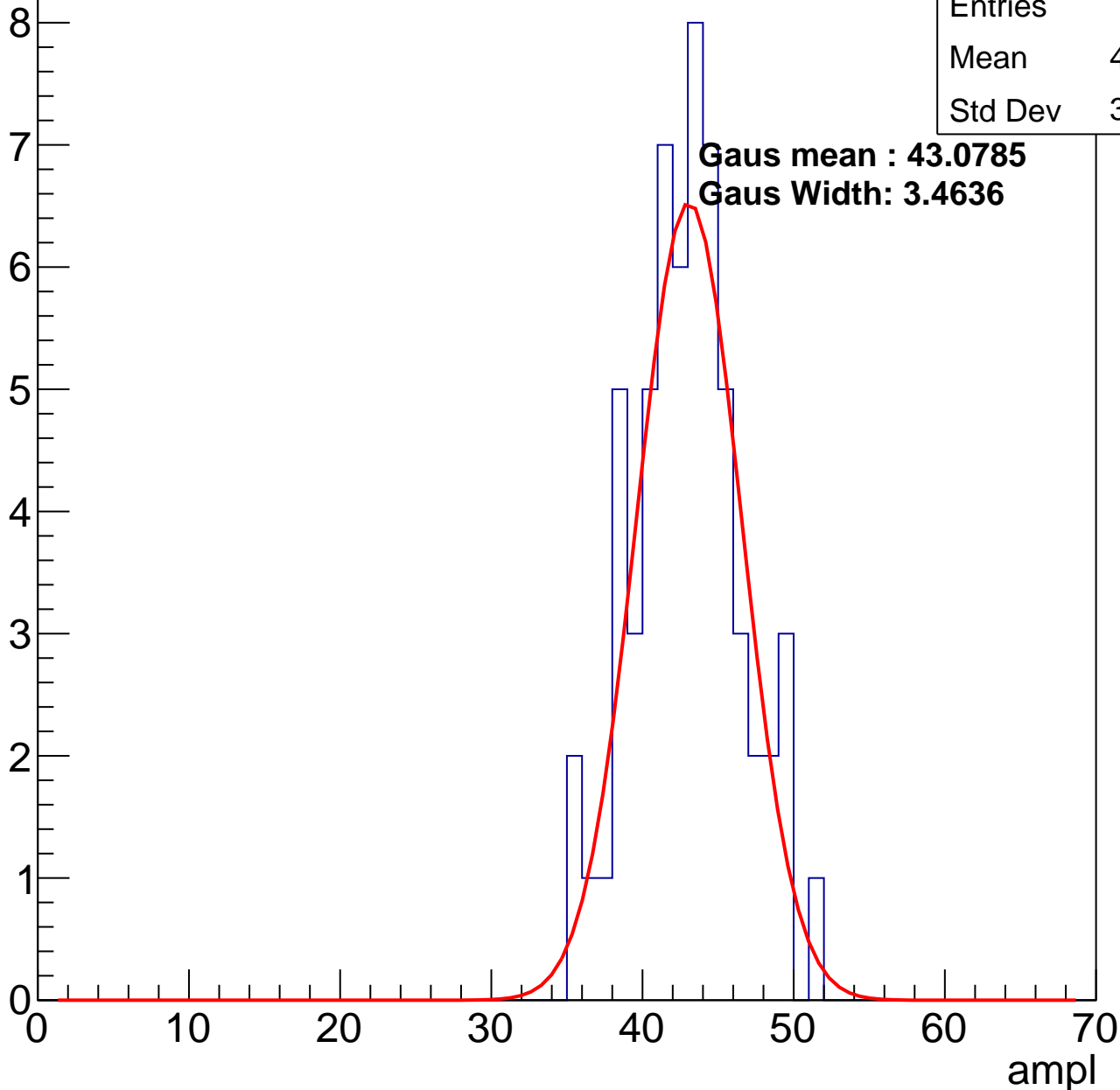
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	42.49
Std Dev	3.523

**Gaus mean : 43.0785**

**Gaus Width: 3.4636**

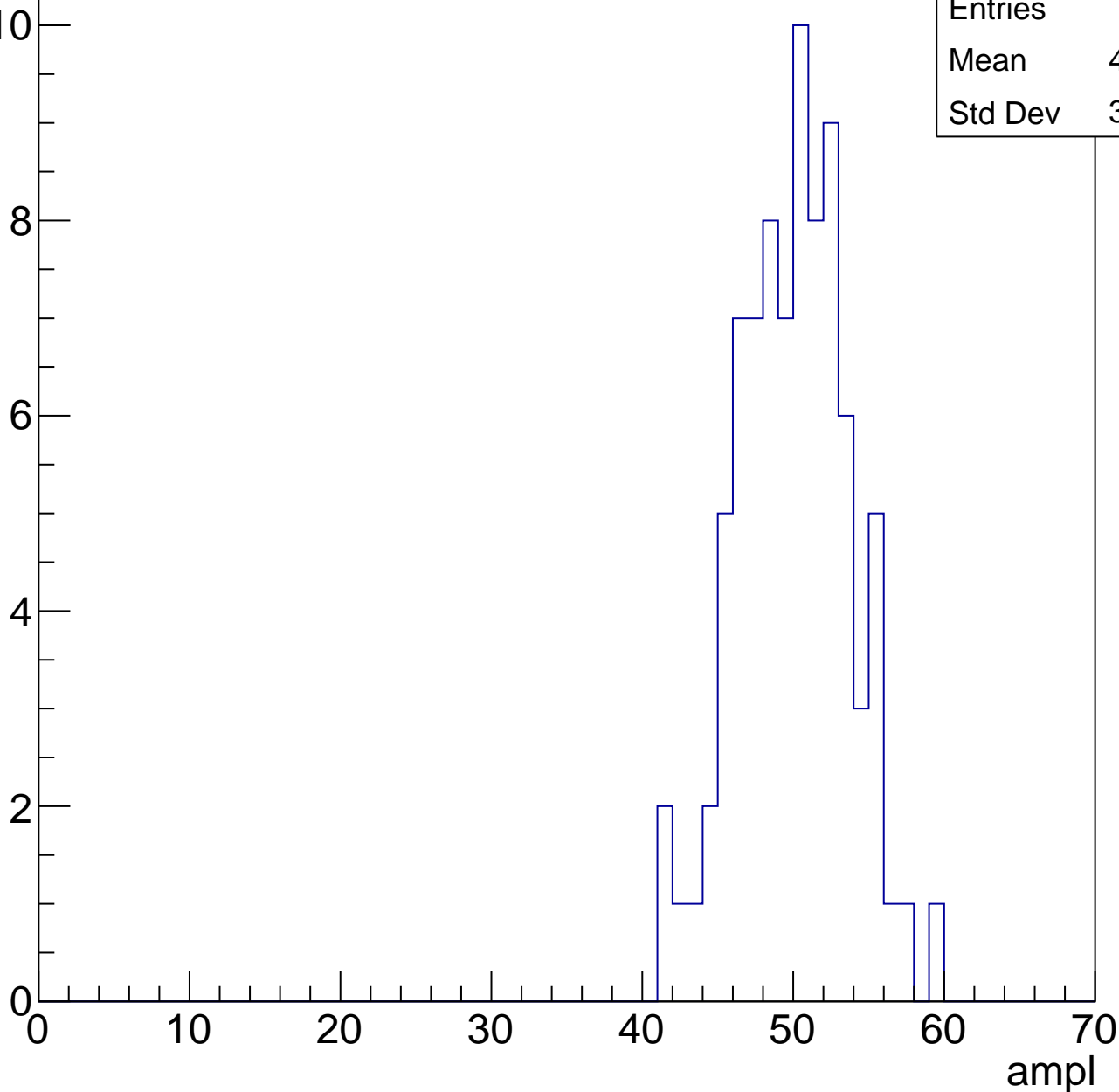


# B1L102S, U8-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	49.54
Std Dev	3.627

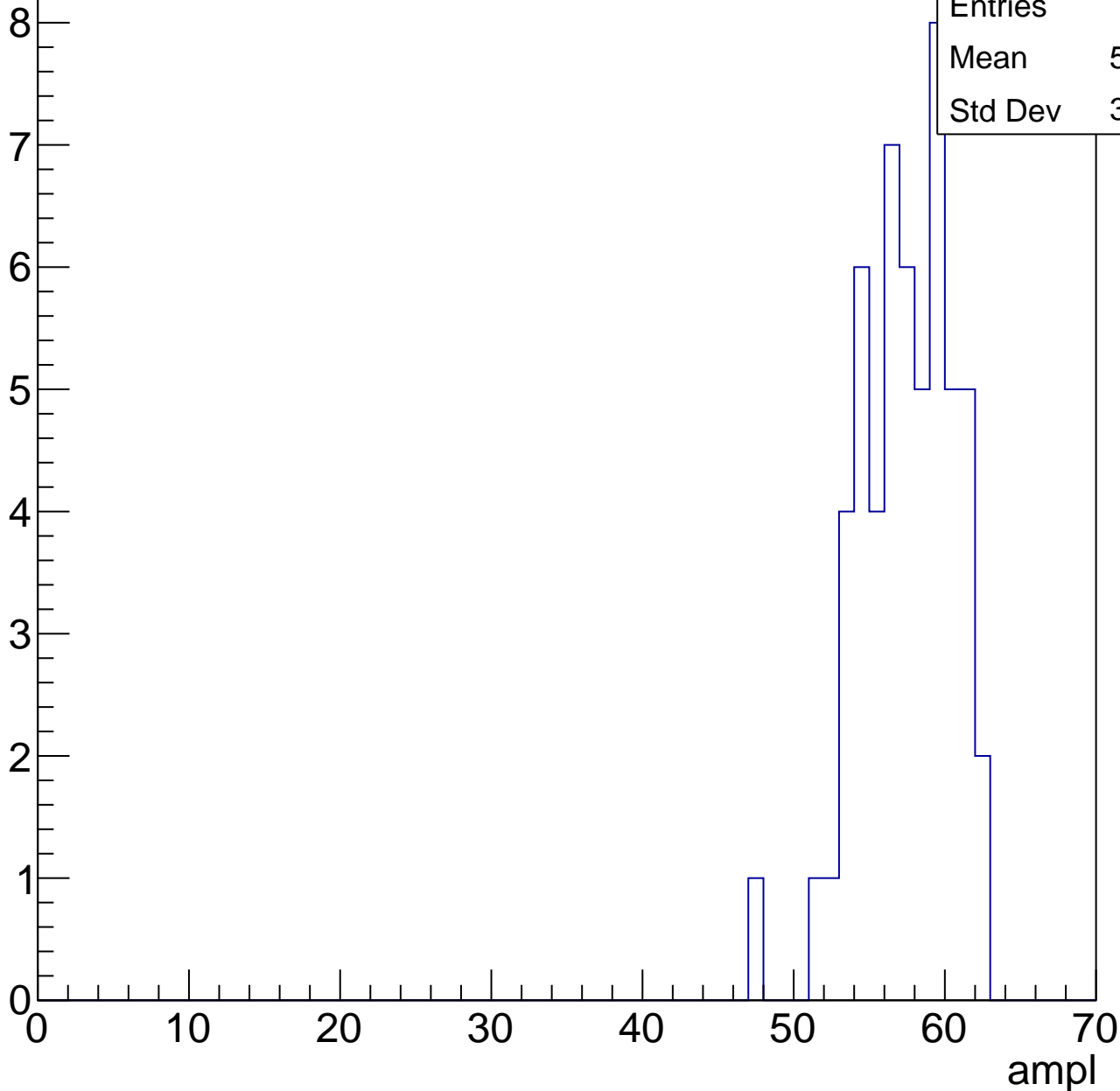


# B1L102S, U8-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	56.93
Std Dev	3.056

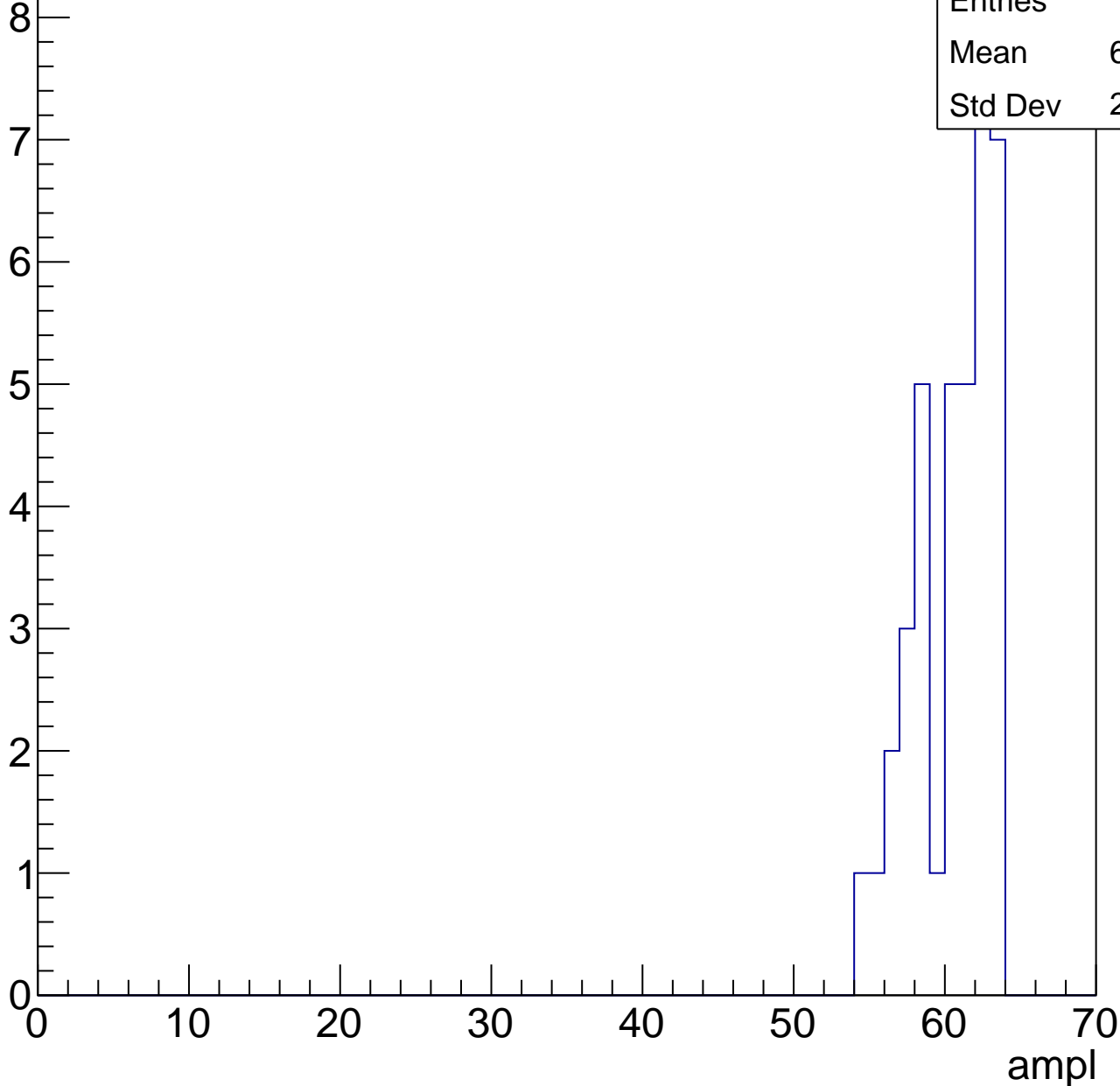


# B1L102S, U8-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

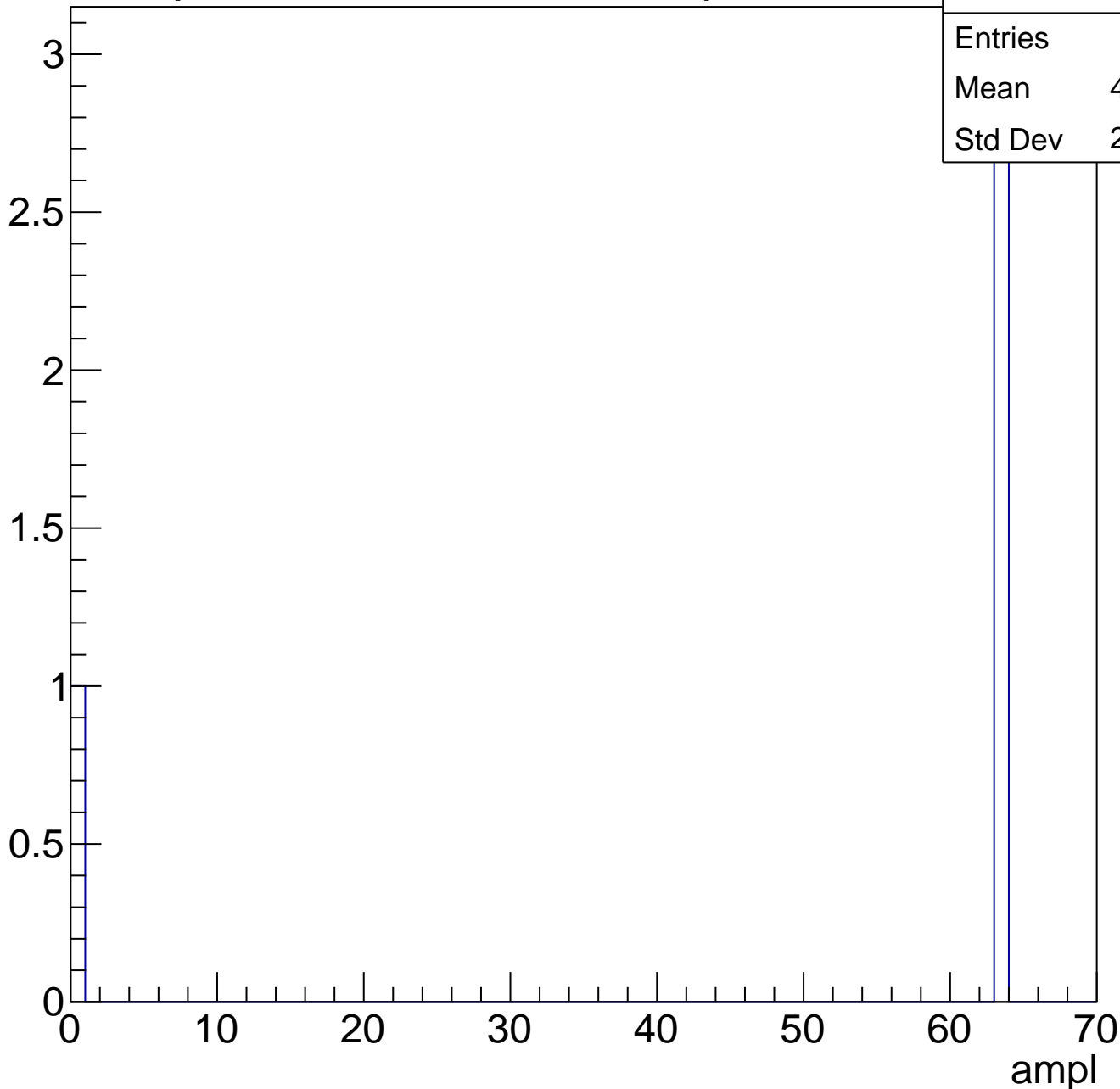
Entries	38
Mean	60.08
Std Dev	2.517



# B1L102S, U8-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch78, adc0

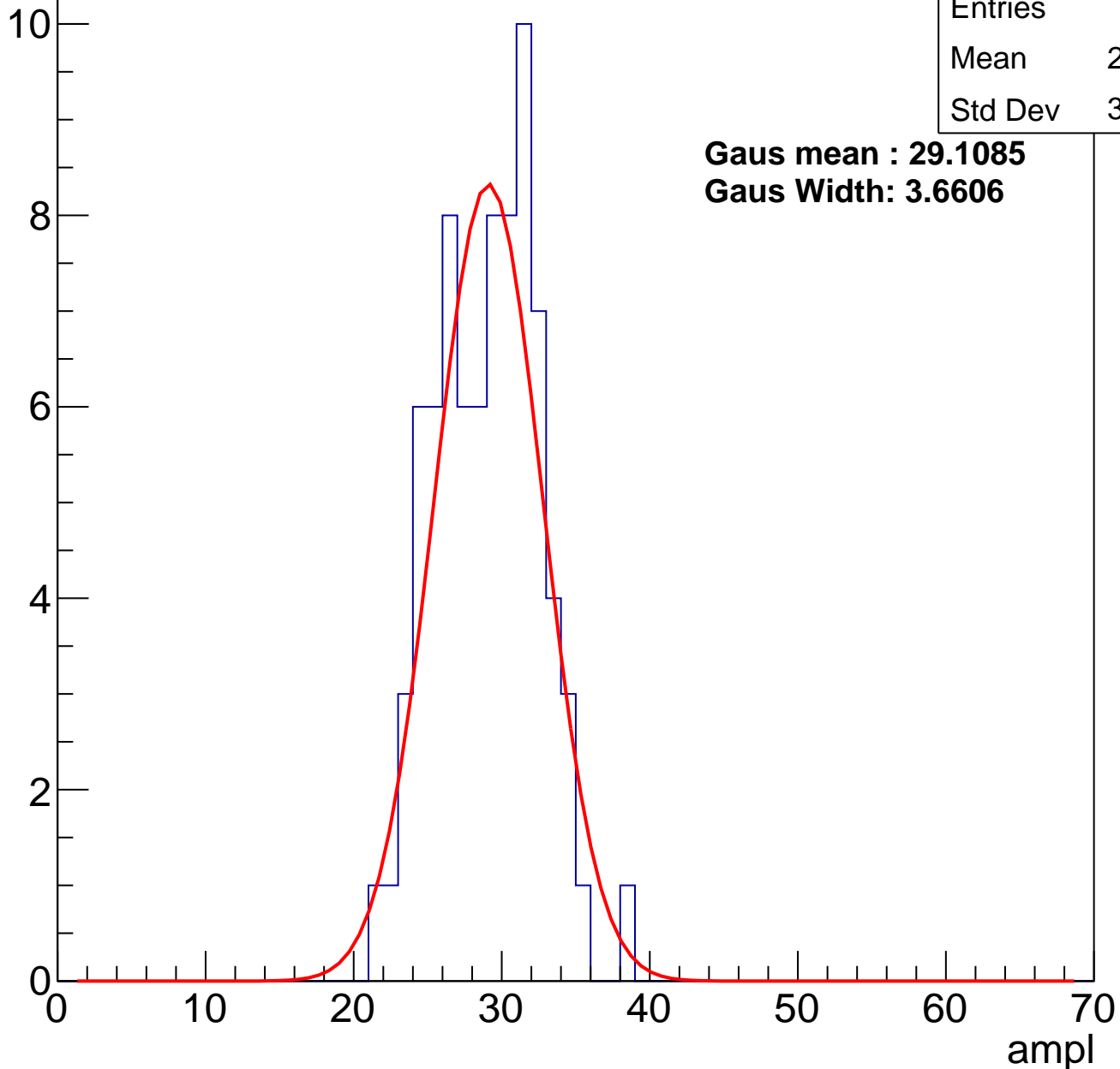
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	79
Mean	28.57
Std Dev	3.415

**Gaus mean : 29.1085**

**Gaus Width: 3.6606**

Entry



# B1L102S, U8-ch78, adc1

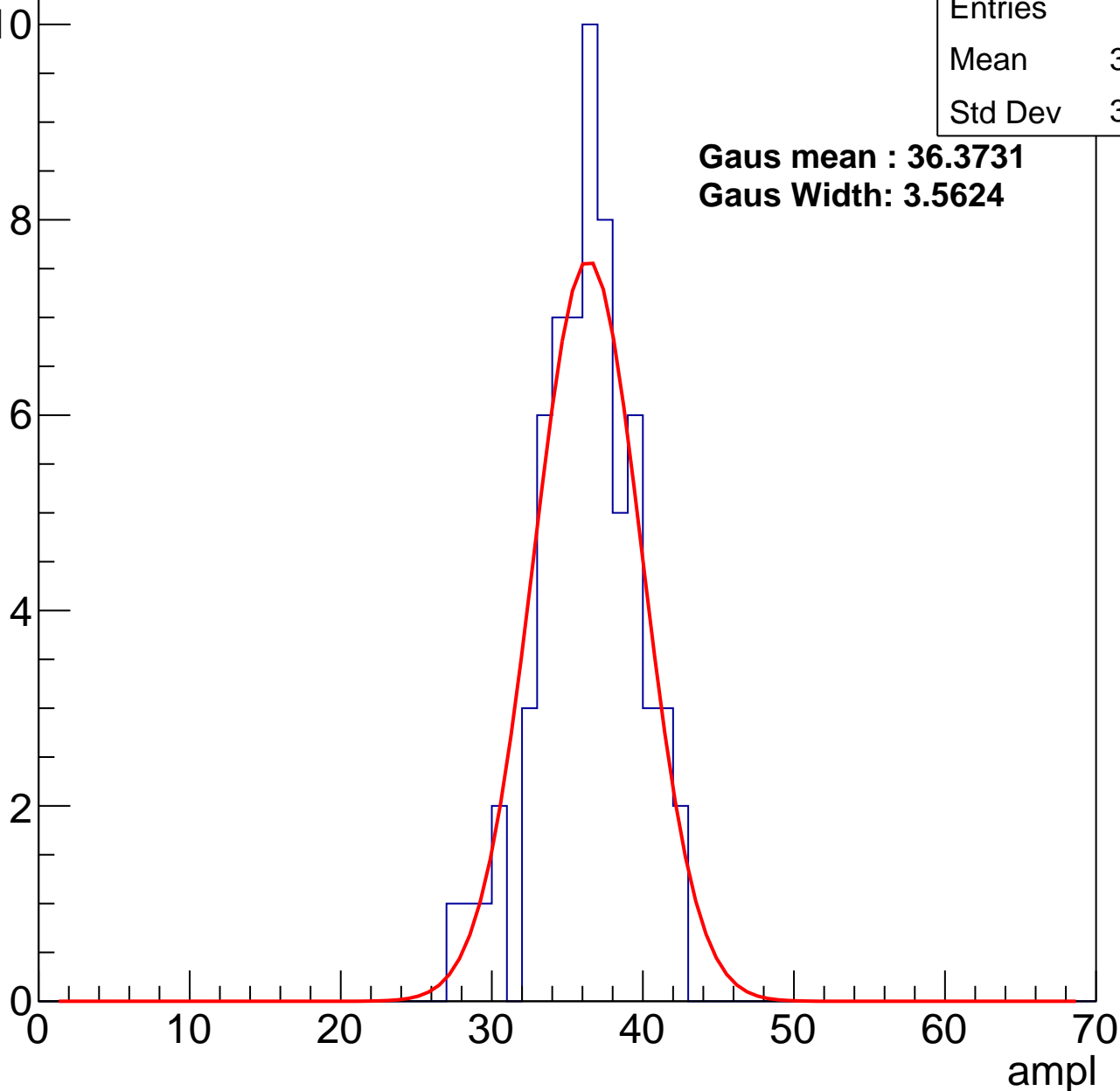
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	35.82
Std Dev	3.229

**Gaus mean : 36.3731**

**Gaus Width: 3.5624**



# B1L102S, U8-ch78, adc2

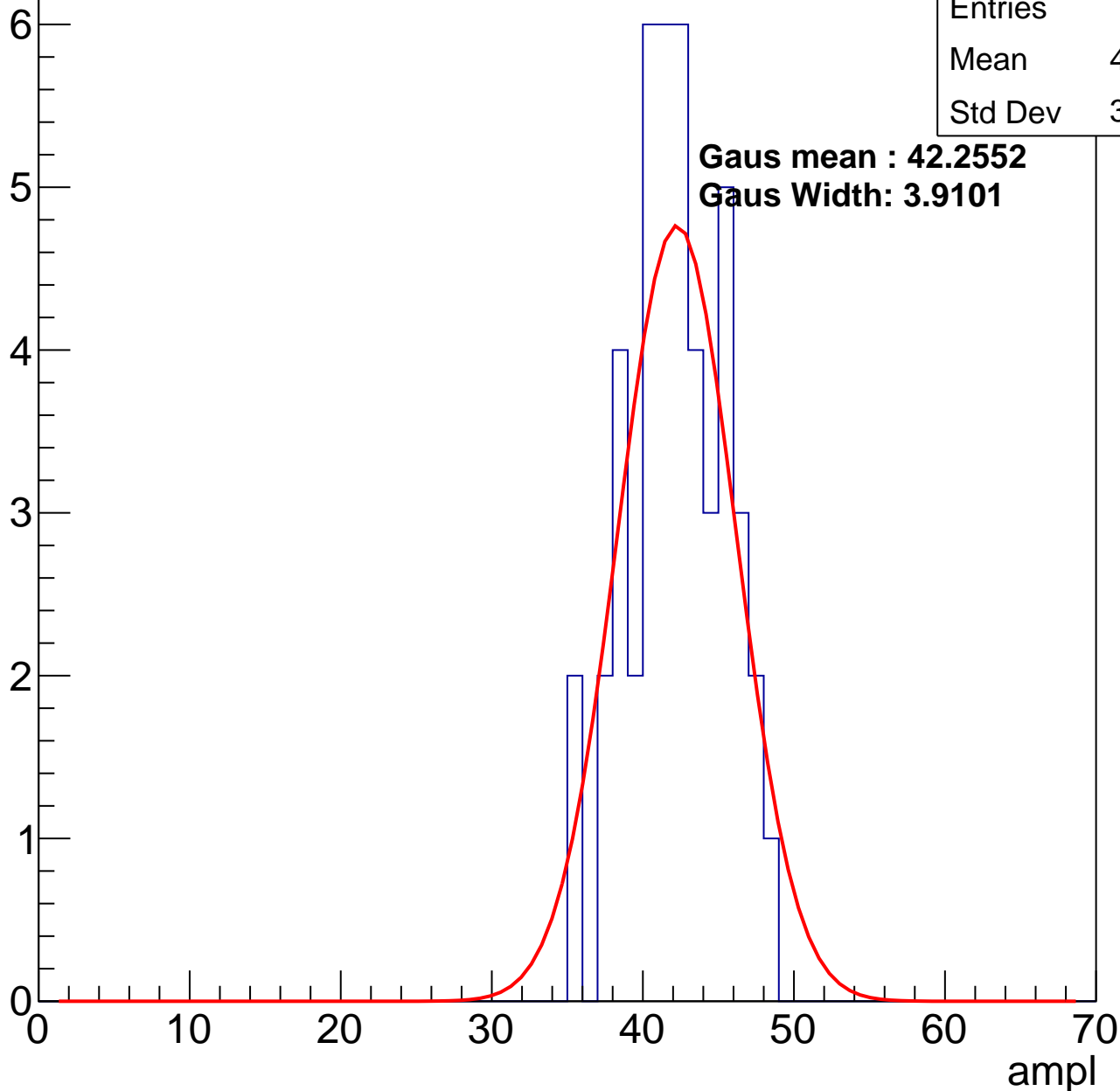
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	41.76
Std Dev	3.136

**Gaus mean : 42.2552**

**Gaus Width: 3.9101**

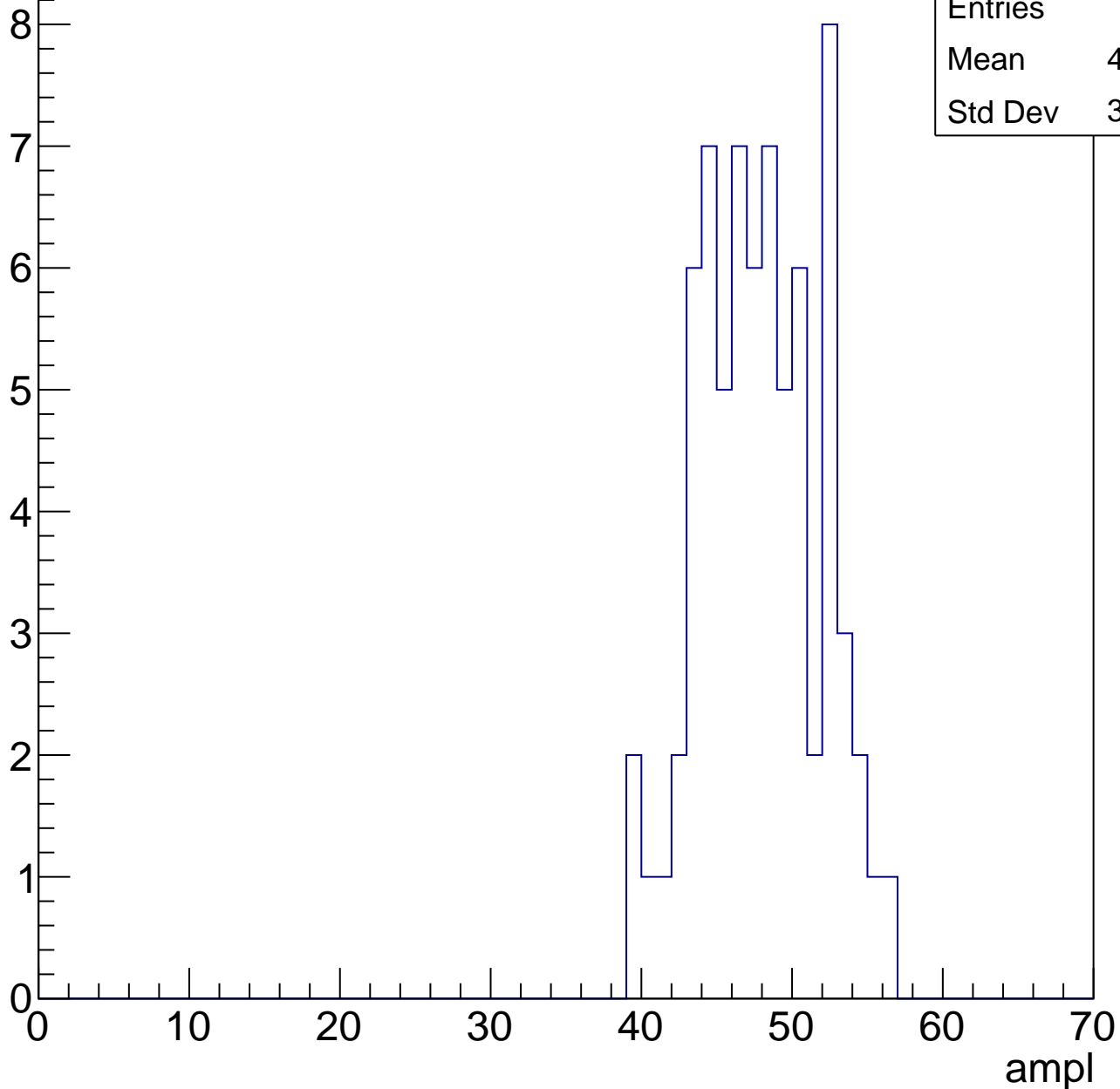


# B1L102S, U8-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	47.43
Std Dev	3.908

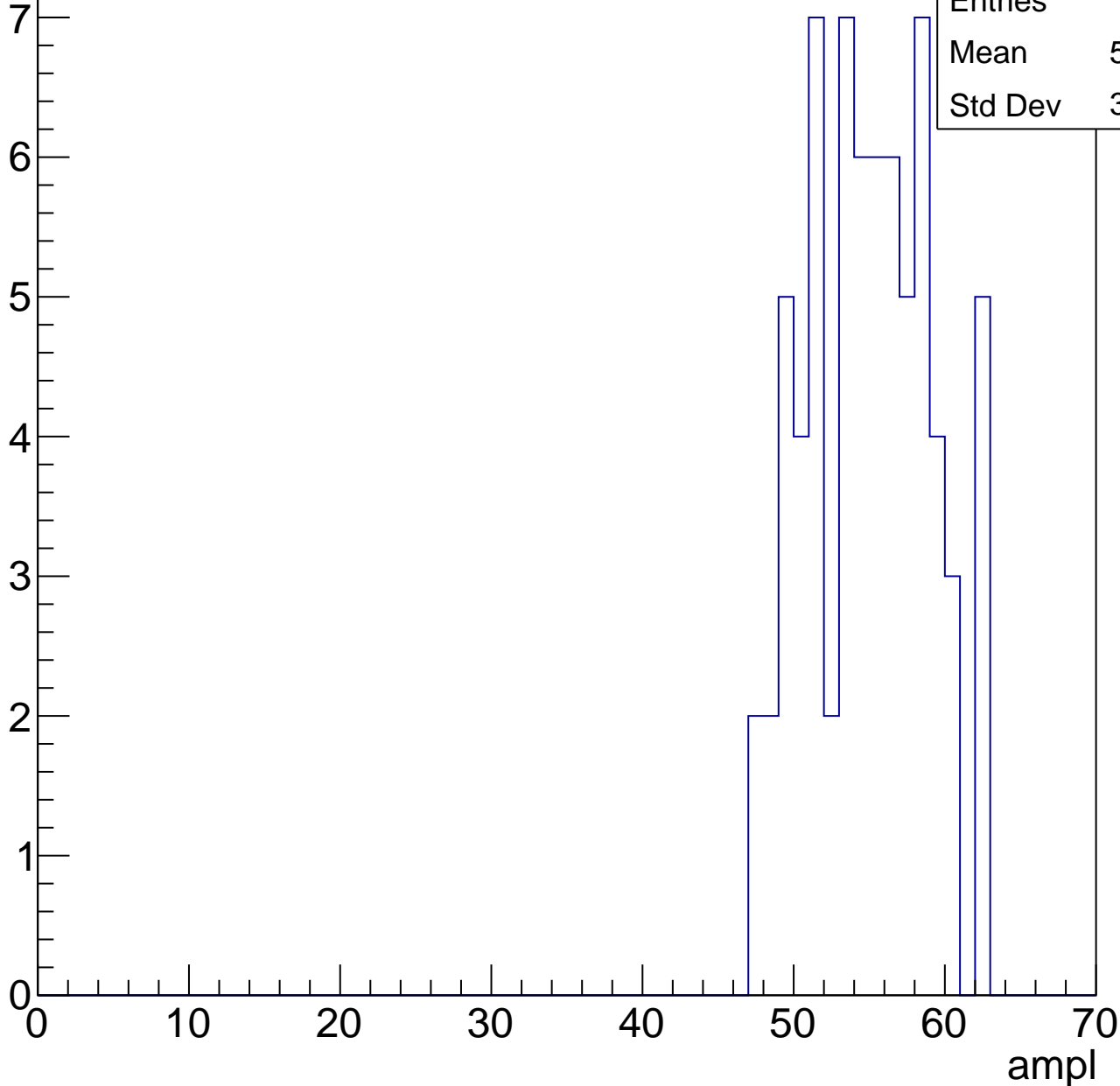


# B1L102S, U8-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	54.56
Std Dev	3.988

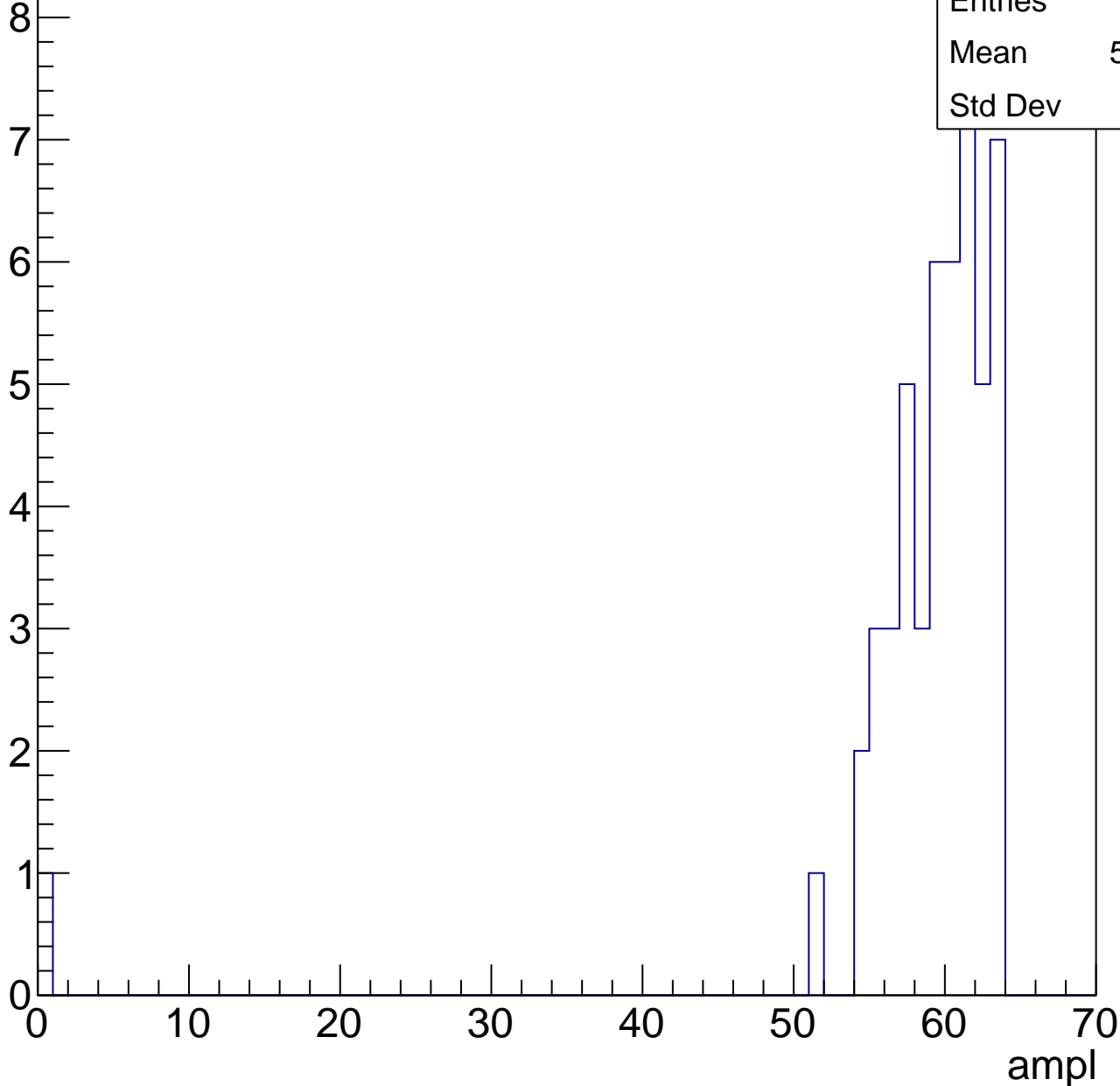


# B1L102S, U8-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

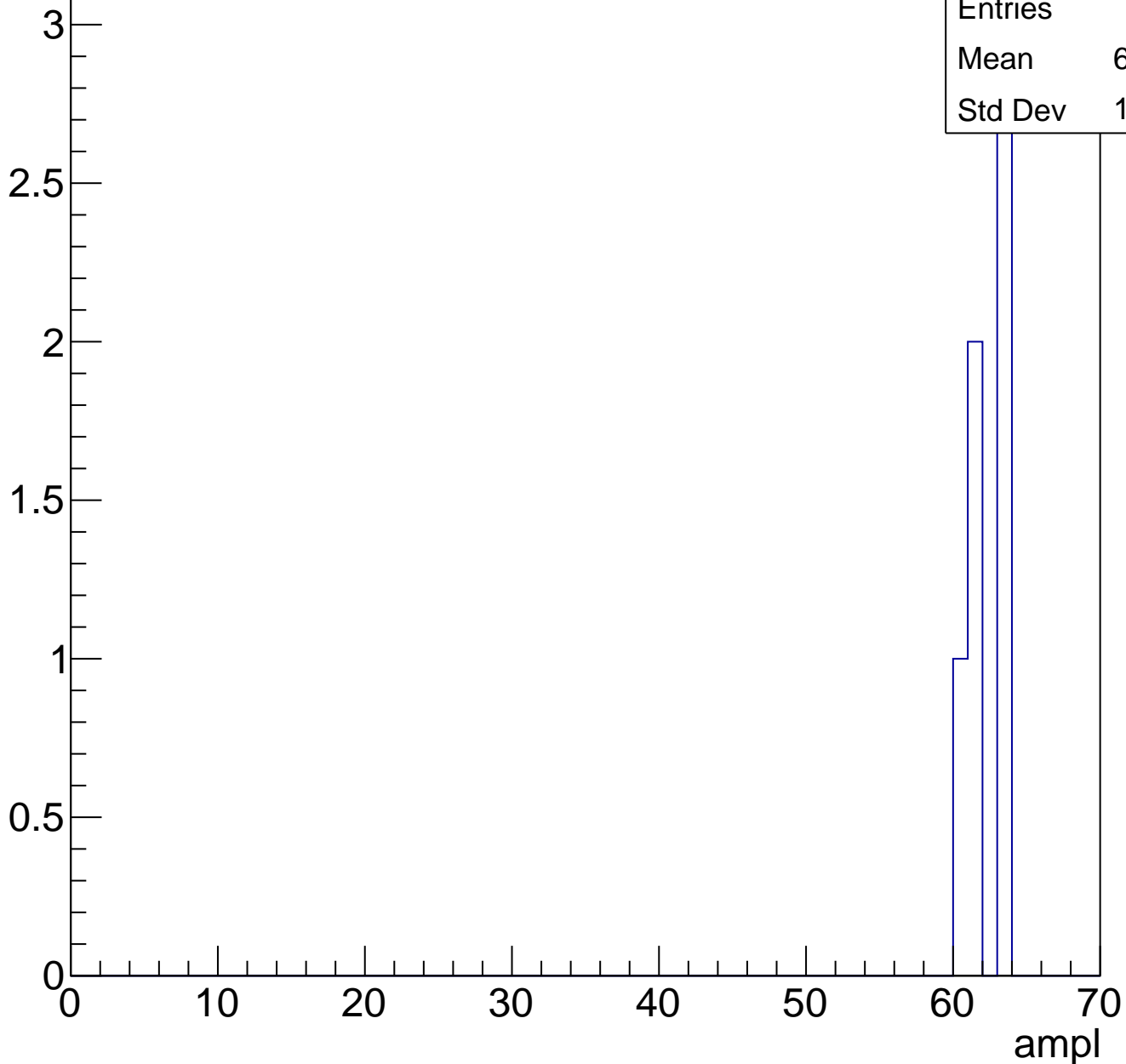
Entries	50
Mean	58.08
Std Dev	8.77



# B1L102S, U8-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch79, adc0

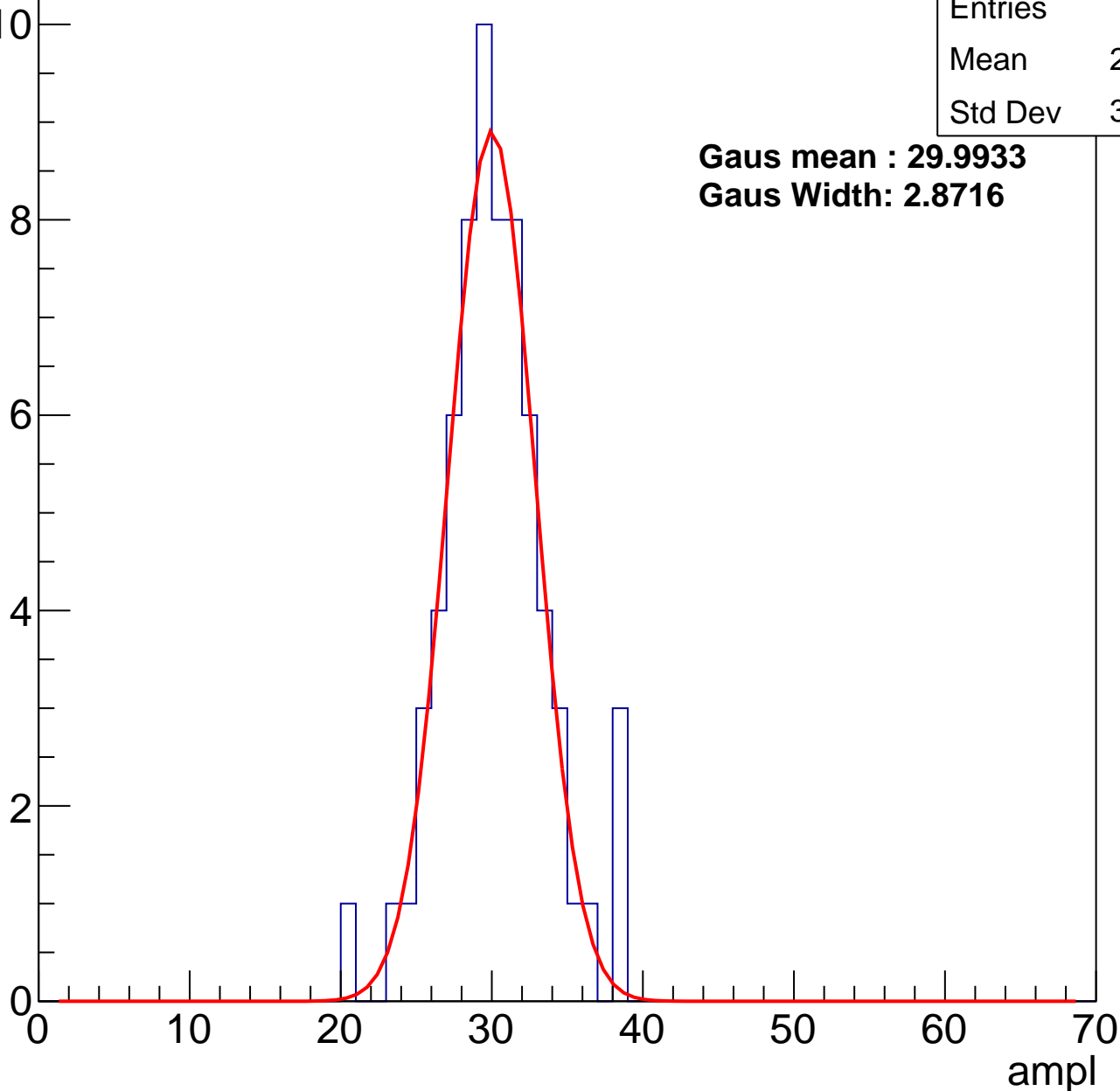
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	29.72
Std Dev	3.395

**Gaus mean : 29.9933**

**Gaus Width: 2.8716**



# B1L102S, U8-ch79, adc1

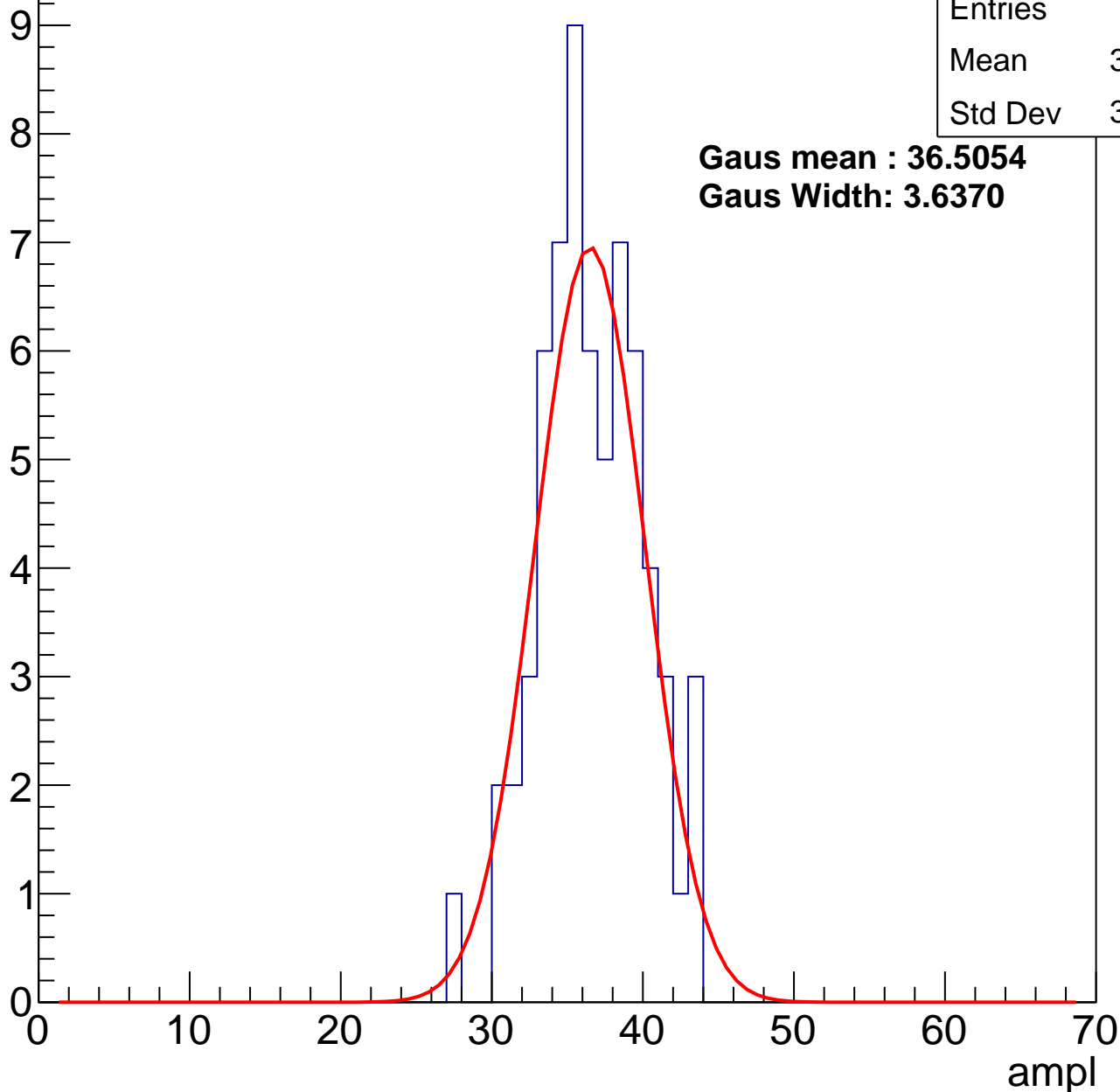
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	36.17
Std Dev	3.395

**Gaus mean : 36.5054**

**Gaus Width: 3.6370**



# B1L102S, U8-ch79, adc2

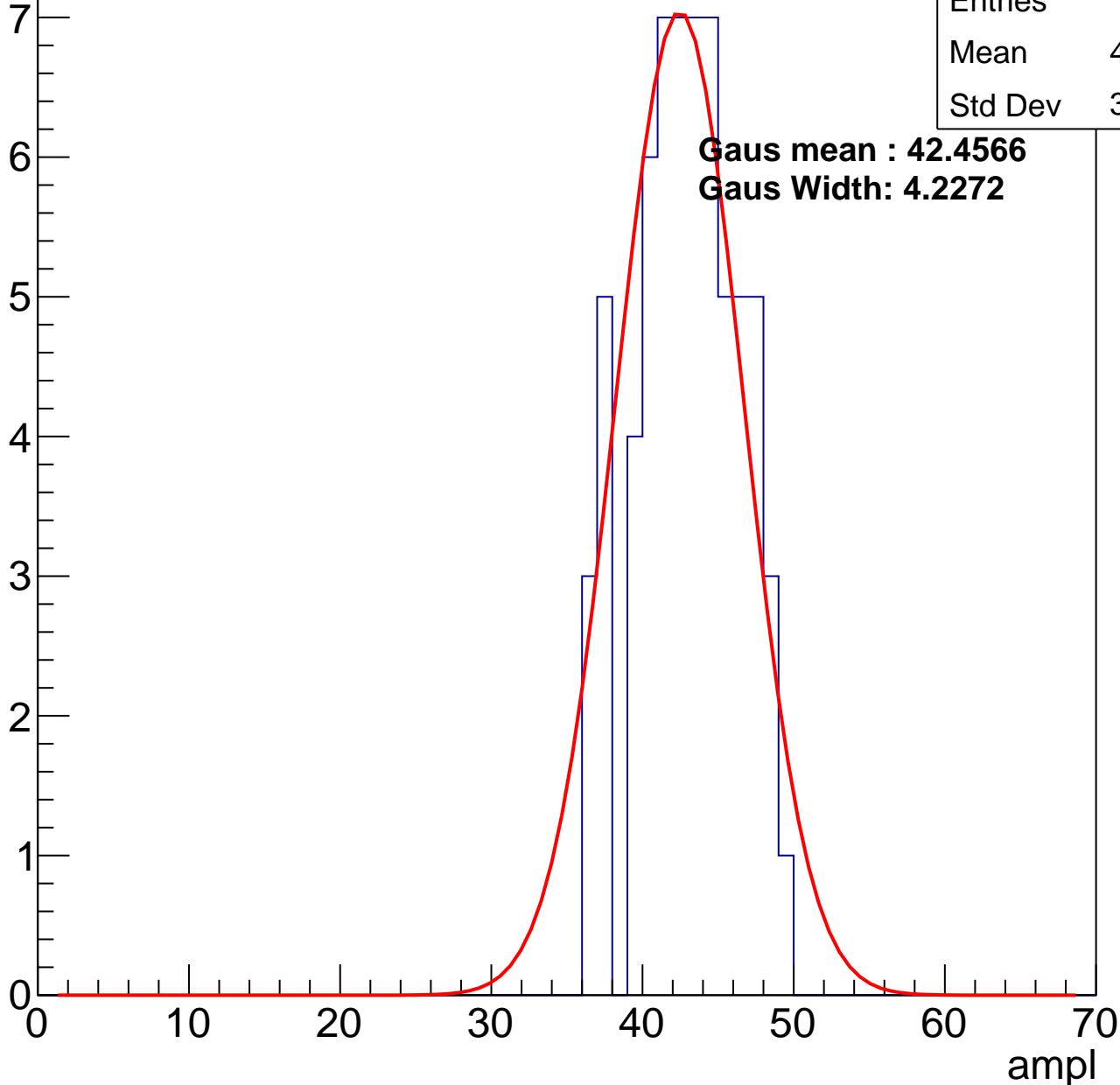
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	42.49
Std Dev	3.343

**Gaus mean : 42.4566**

**Gaus Width: 4.2272**

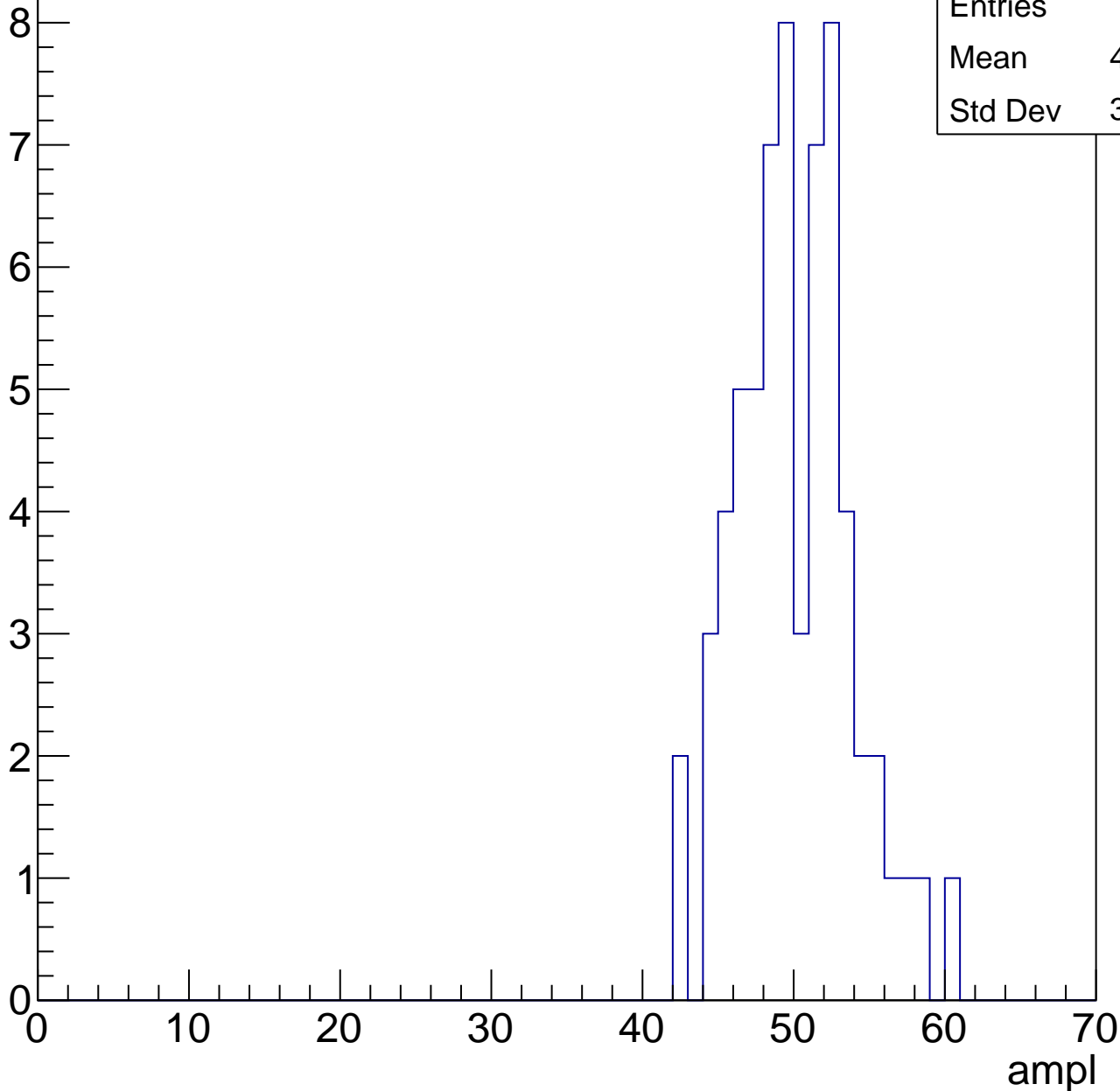


# B1L102S, U8-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	49.58
Std Dev	3.732

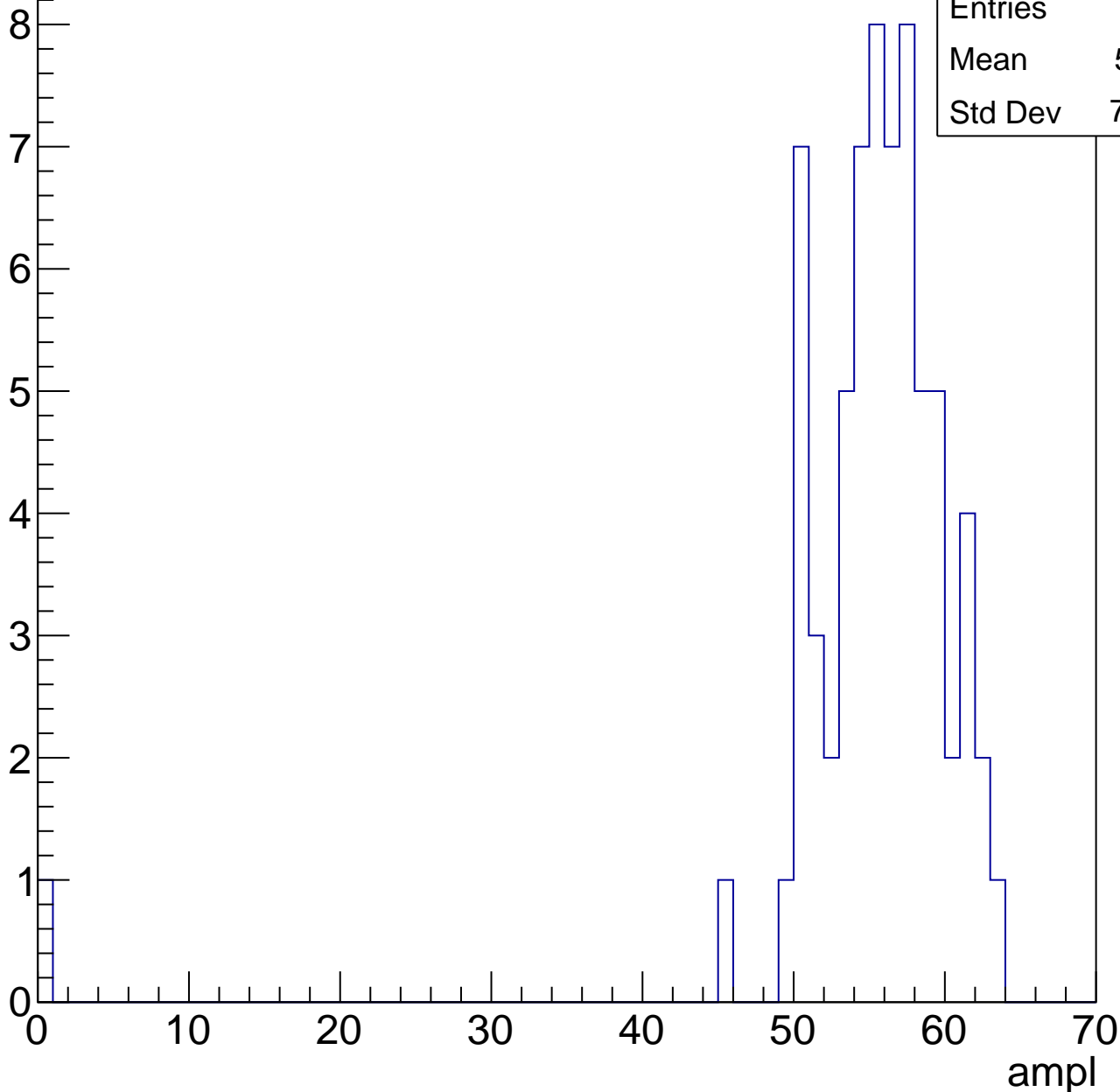


# B1L102S, U8-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	54.61
Std Dev	7.555

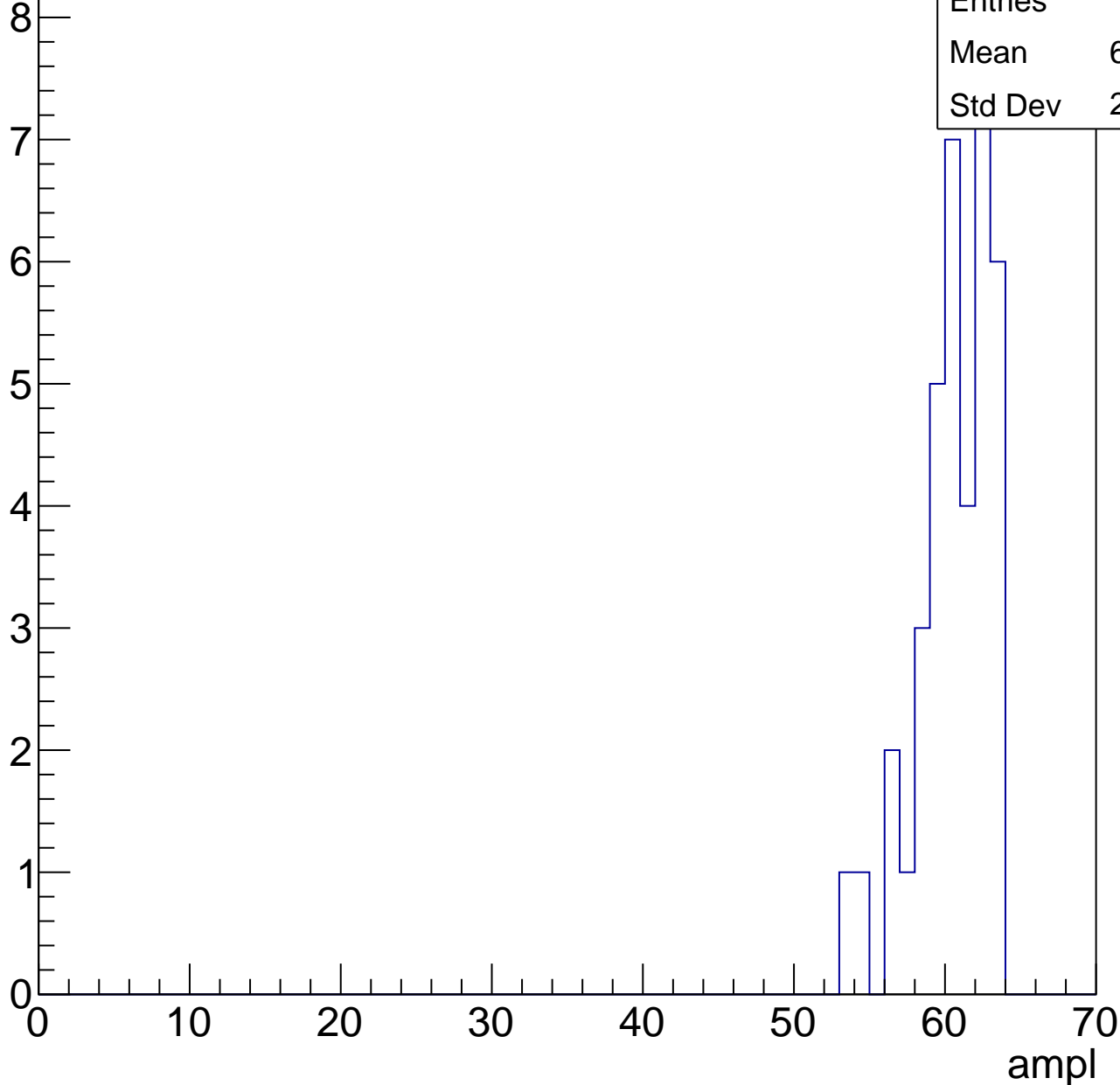


# B1L102S, U8-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

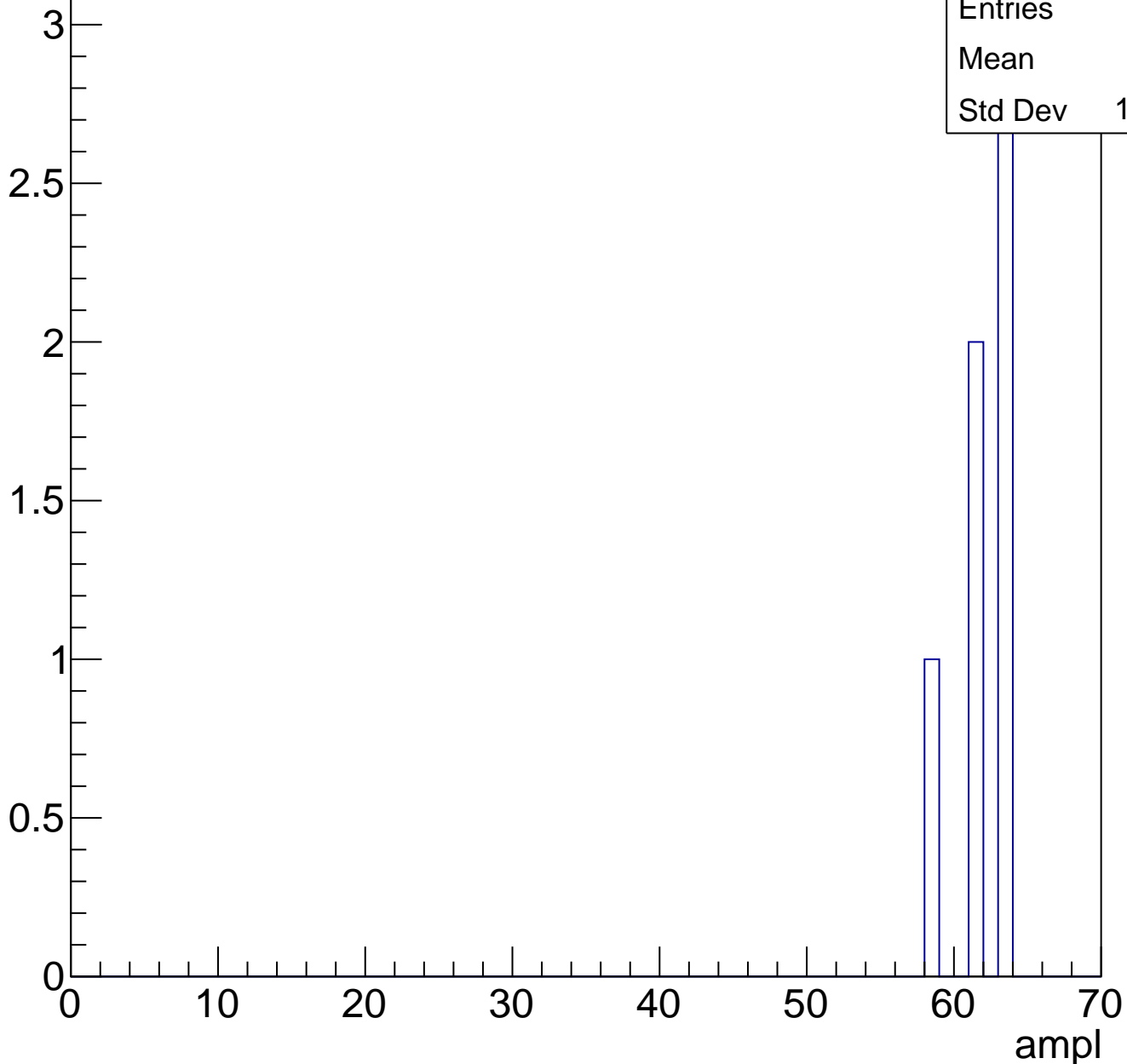
Entries	38
Mean	60.08
Std Dev	2.475



# B1L102S, U8-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L102S, U8-ch80, adc0

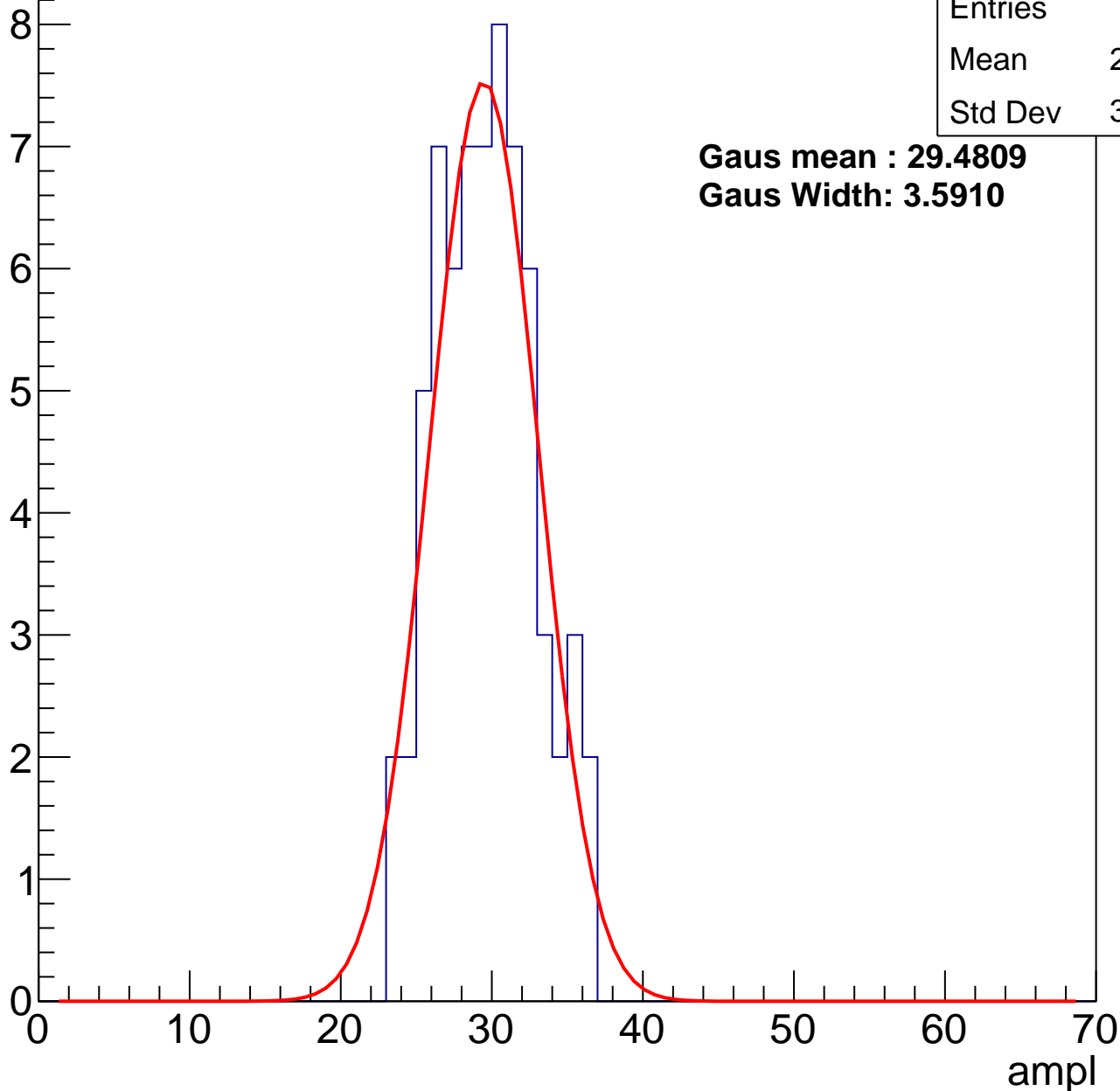
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	29.18
Std Dev	3.204

**Gaus mean : 29.4809**

**Gaus Width: 3.5910**



# B1L102S, U8-ch80, adc1

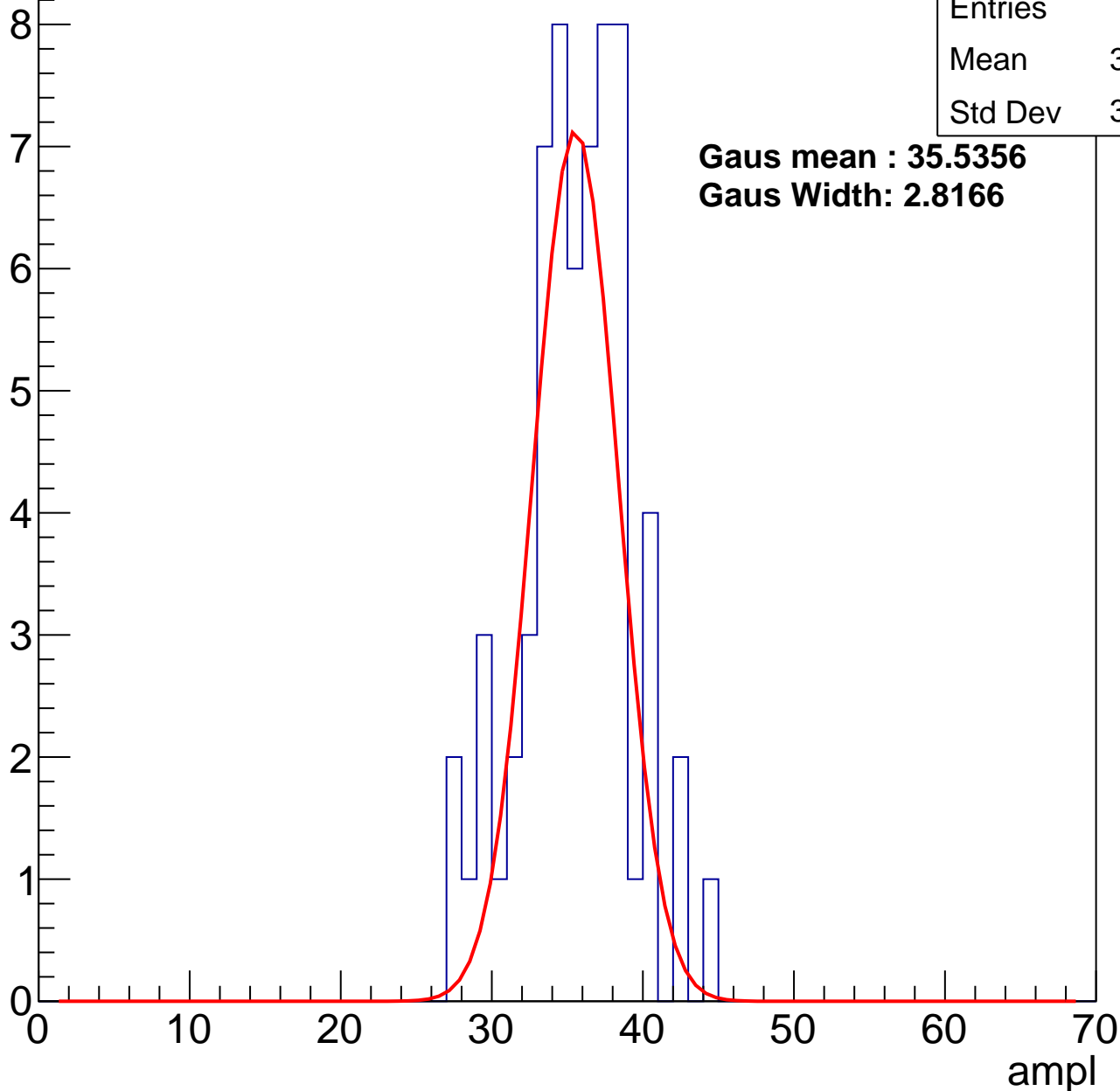
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	35.14
Std Dev	3.557

**Gaus mean : 35.5356**

**Gaus Width: 2.8166**



# B1L102S, U8-ch80, adc2

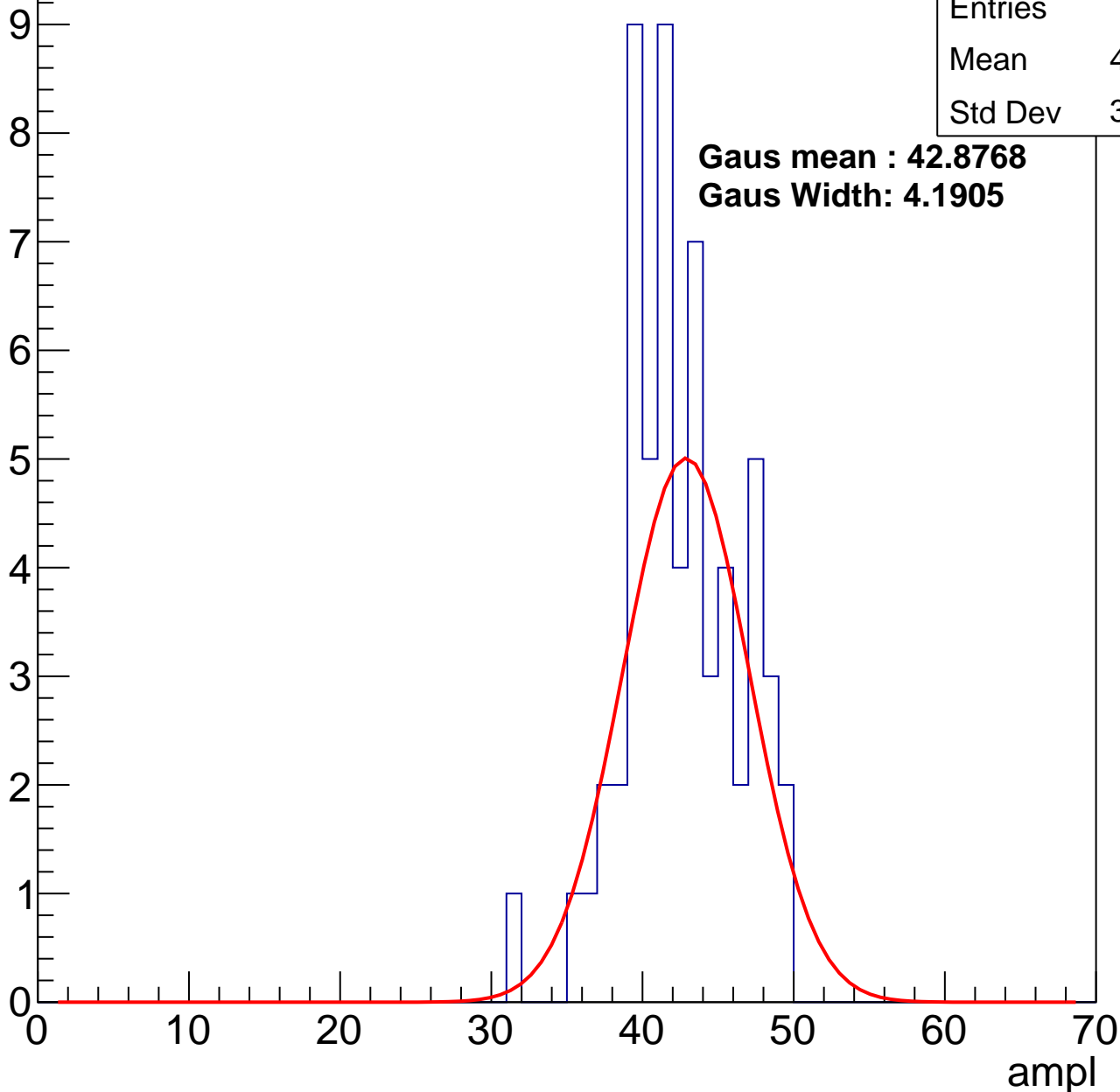
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	42.03
Std Dev	3.688

**Gaus mean : 42.8768**

**Gaus Width: 4.1905**



# B1L102S, U8-ch80, adc3

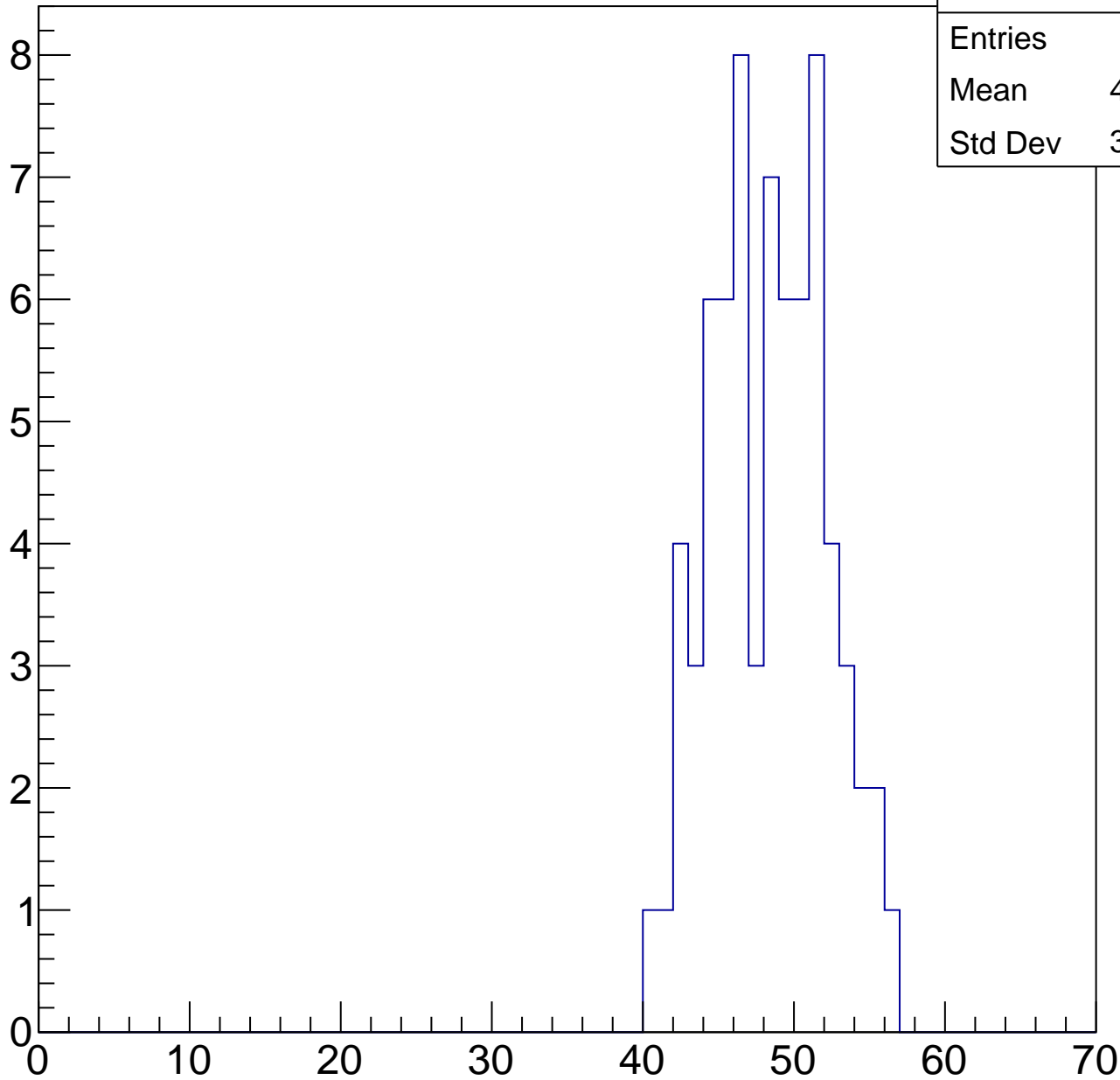
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	71
Mean	47.89
Std Dev	3.736

ampl

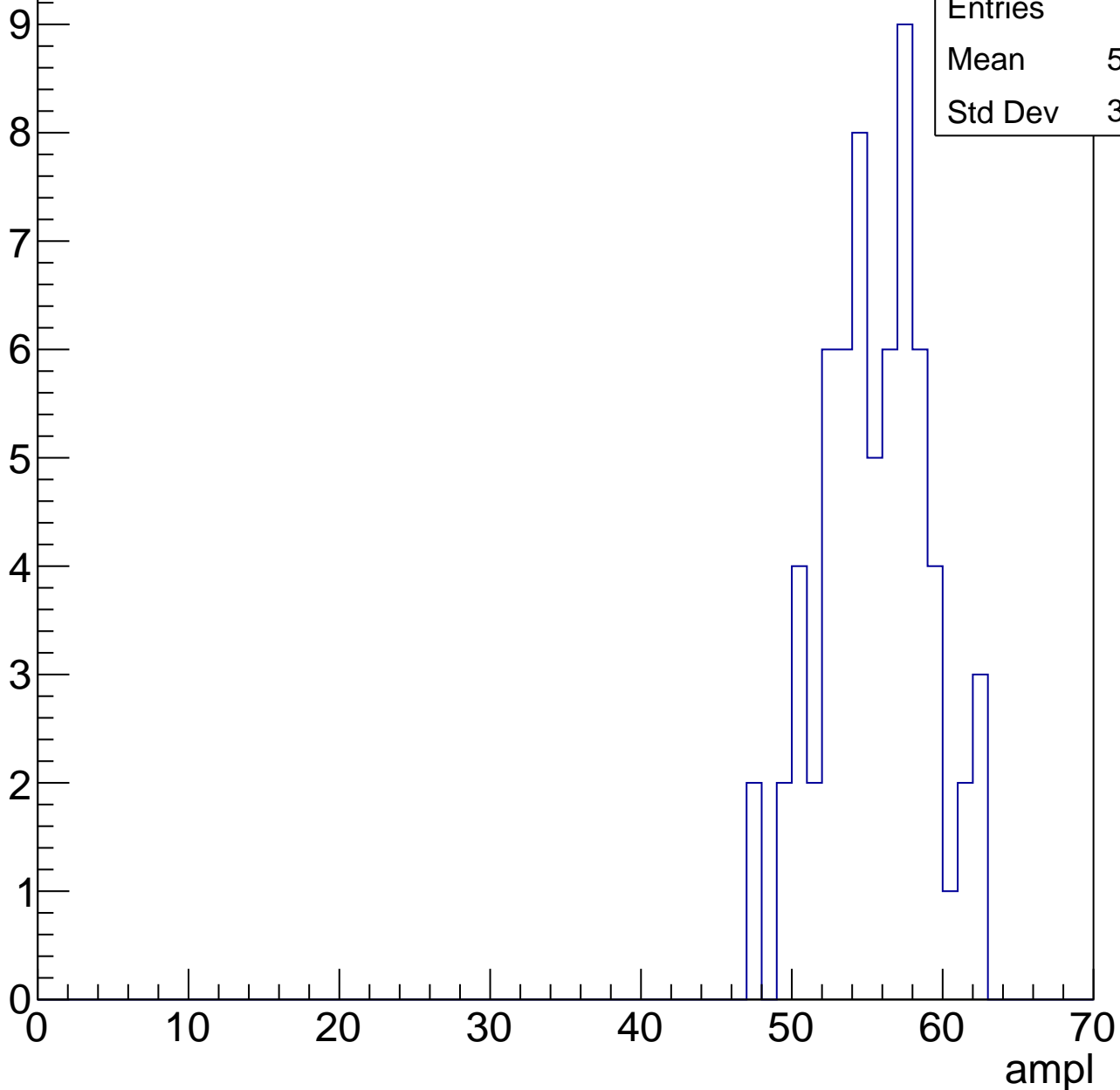


# B1L102S, U8-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	55.03
Std Dev	3.529

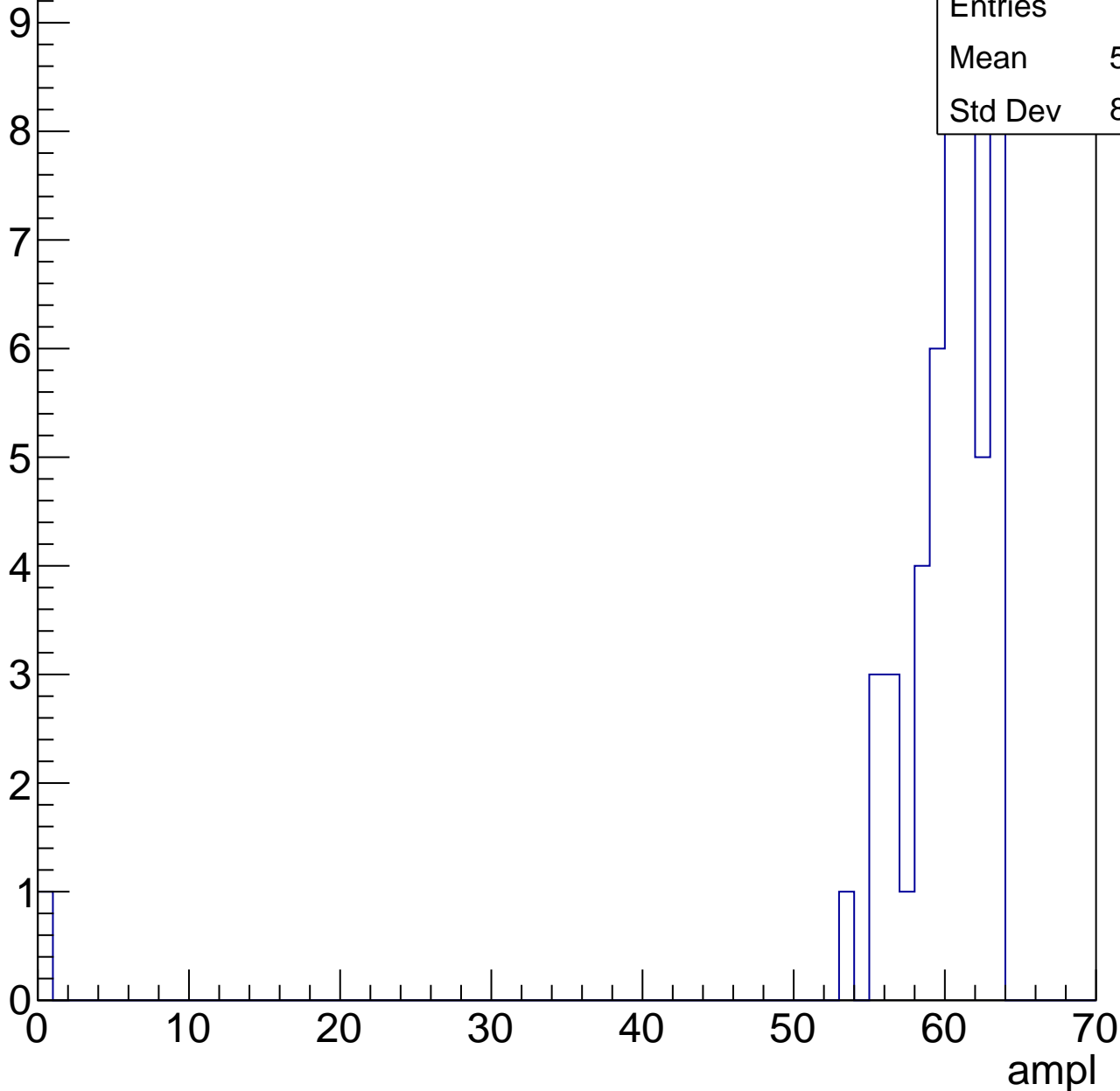


# B1L102S, U8-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	58.68
Std Dev	8.746



# B1L102S, U8-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

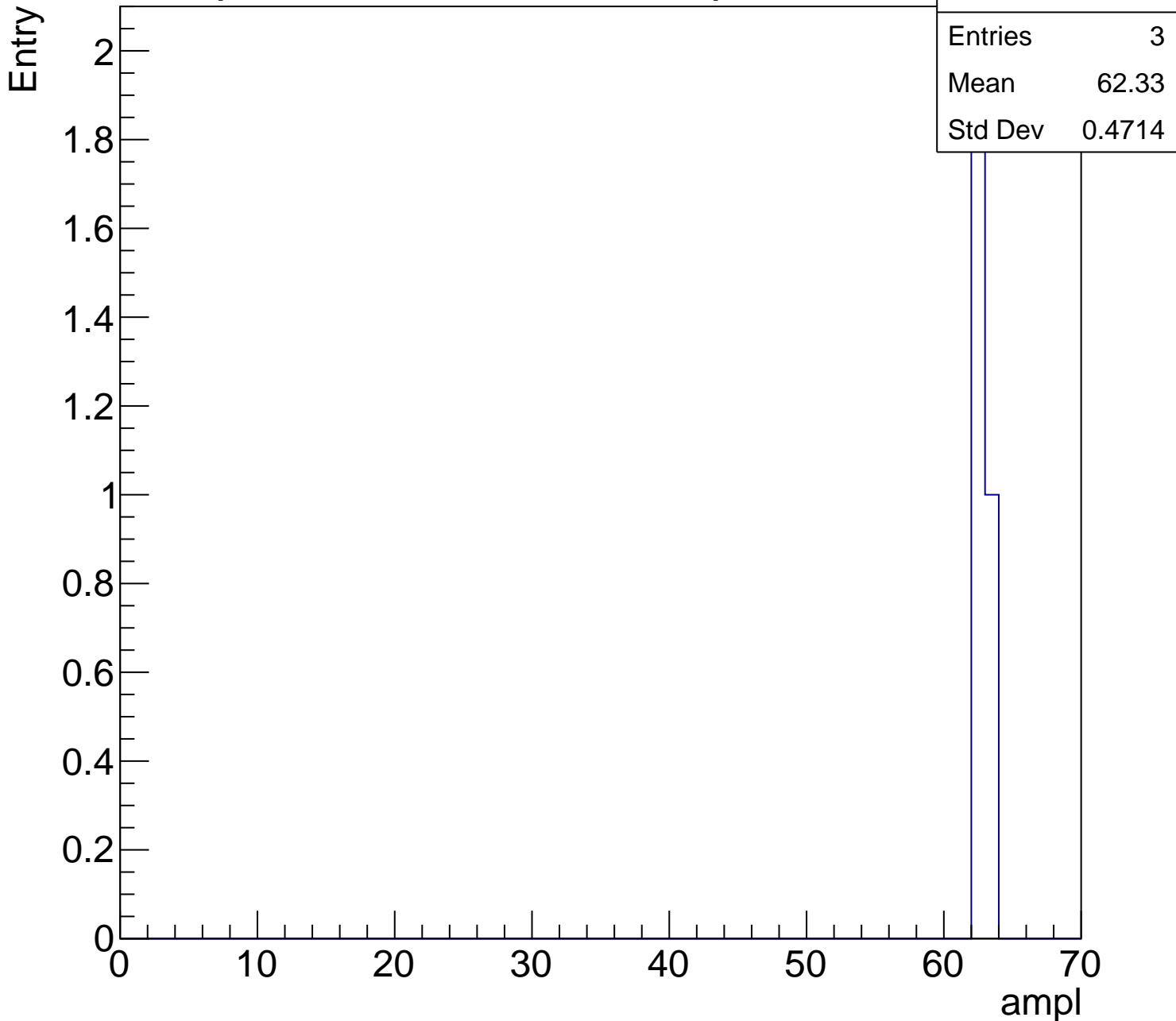
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.4714

0 10 20 30 40 50 60 70

ampl





# B1L102S, U8-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U8-ch81, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	88
Mean	30.19
Std Dev	5.902

**Gaus mean : 31.1839**

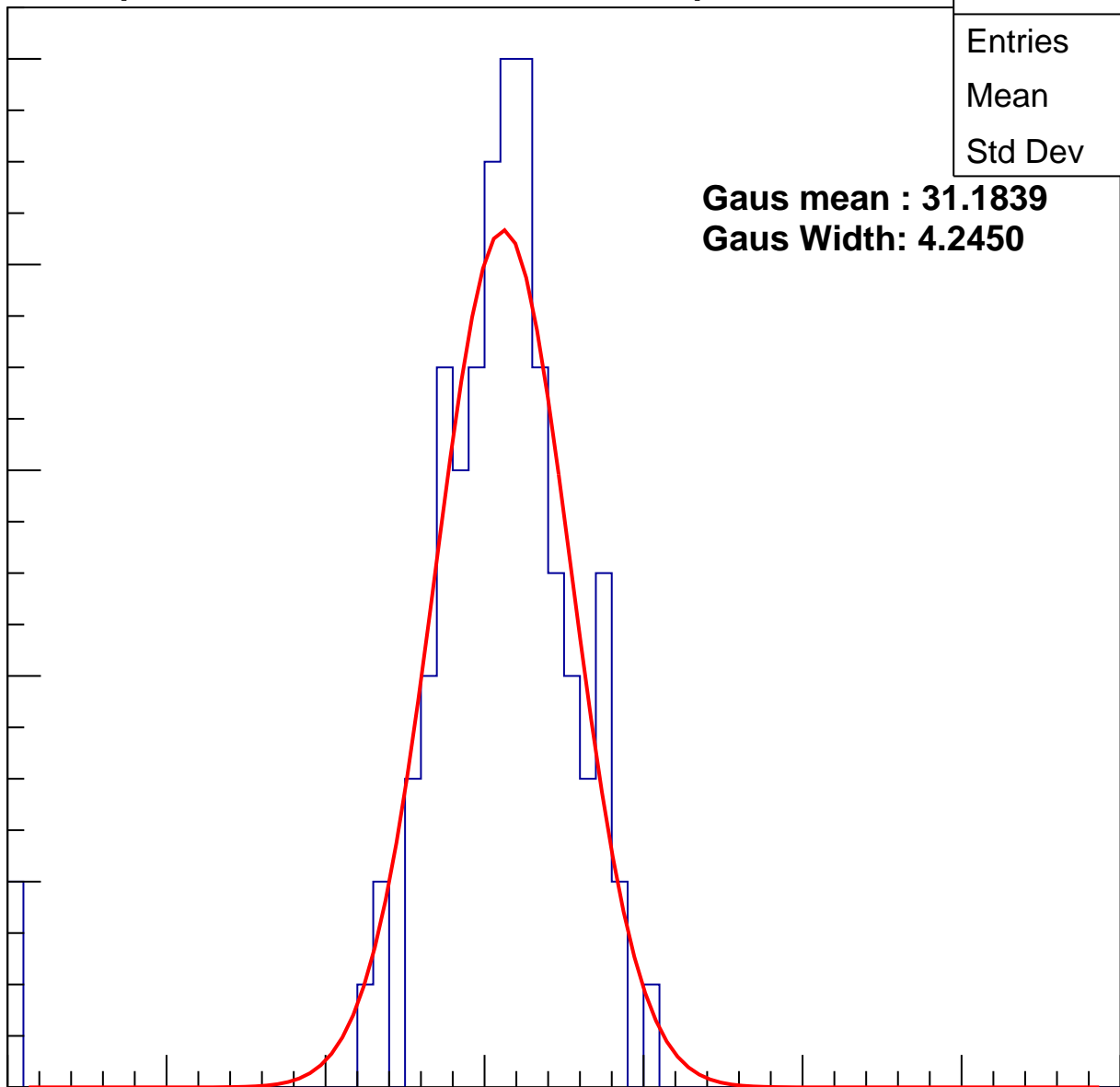
**Gaus Width: 4.2450**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U8-ch81, adc1

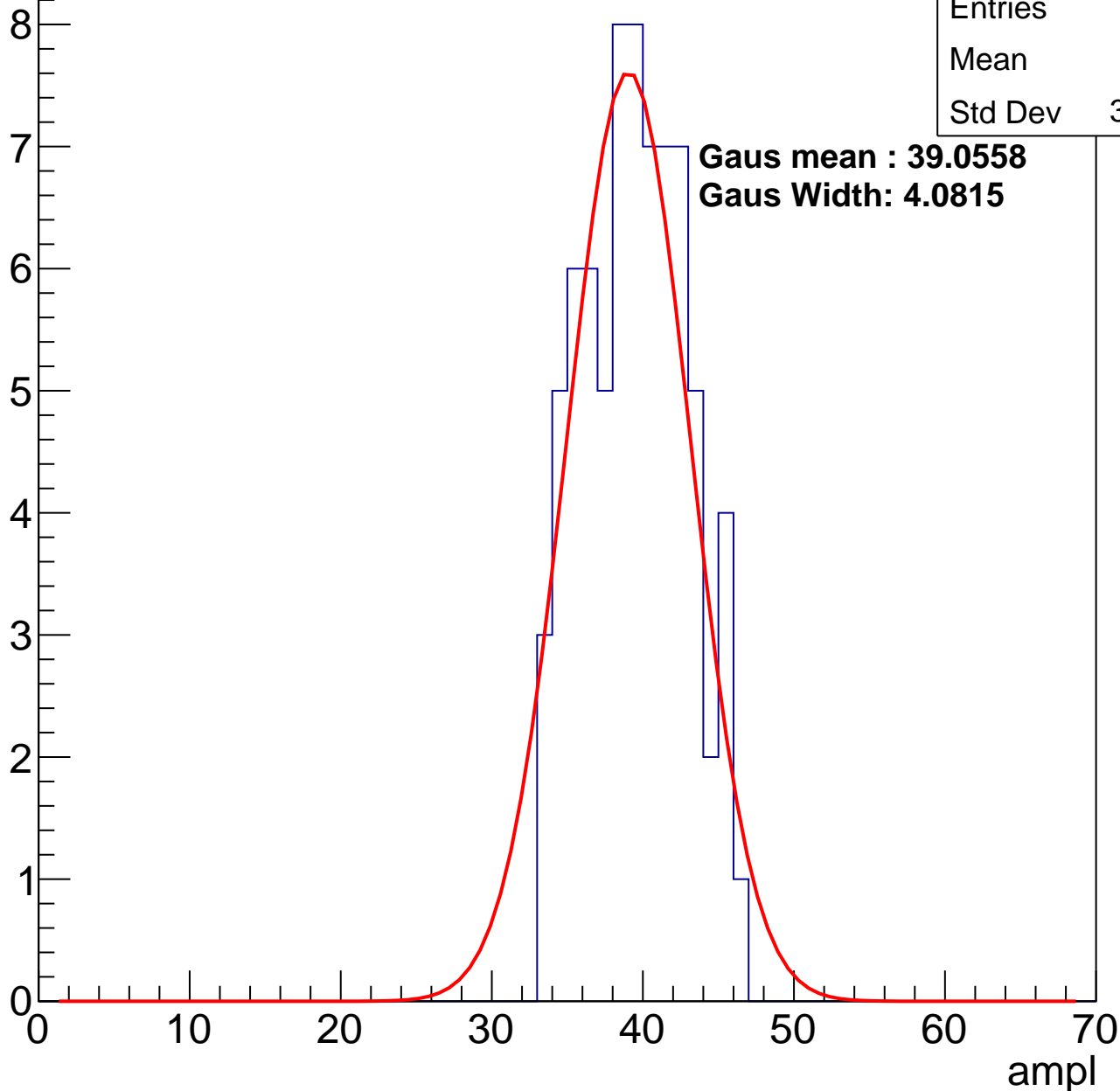
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	39
Std Dev	3.353

**Gaus mean : 39.0558**

**Gaus Width: 4.0815**



# B1L102S, U8-ch81, adc2

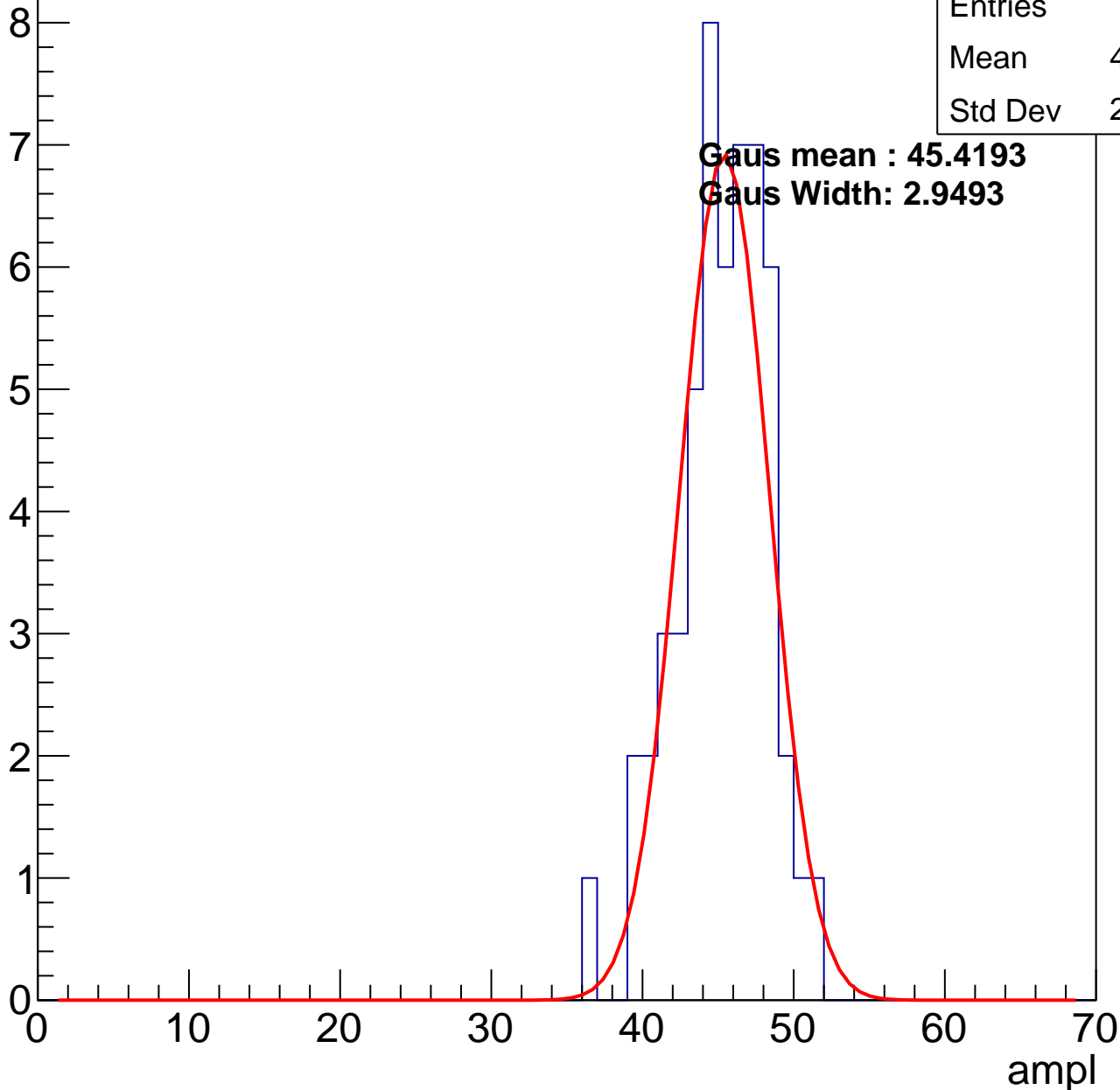
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	44.78
Std Dev	2.998

Gaus mean : 45.4193

Gaus Width: 2.9493

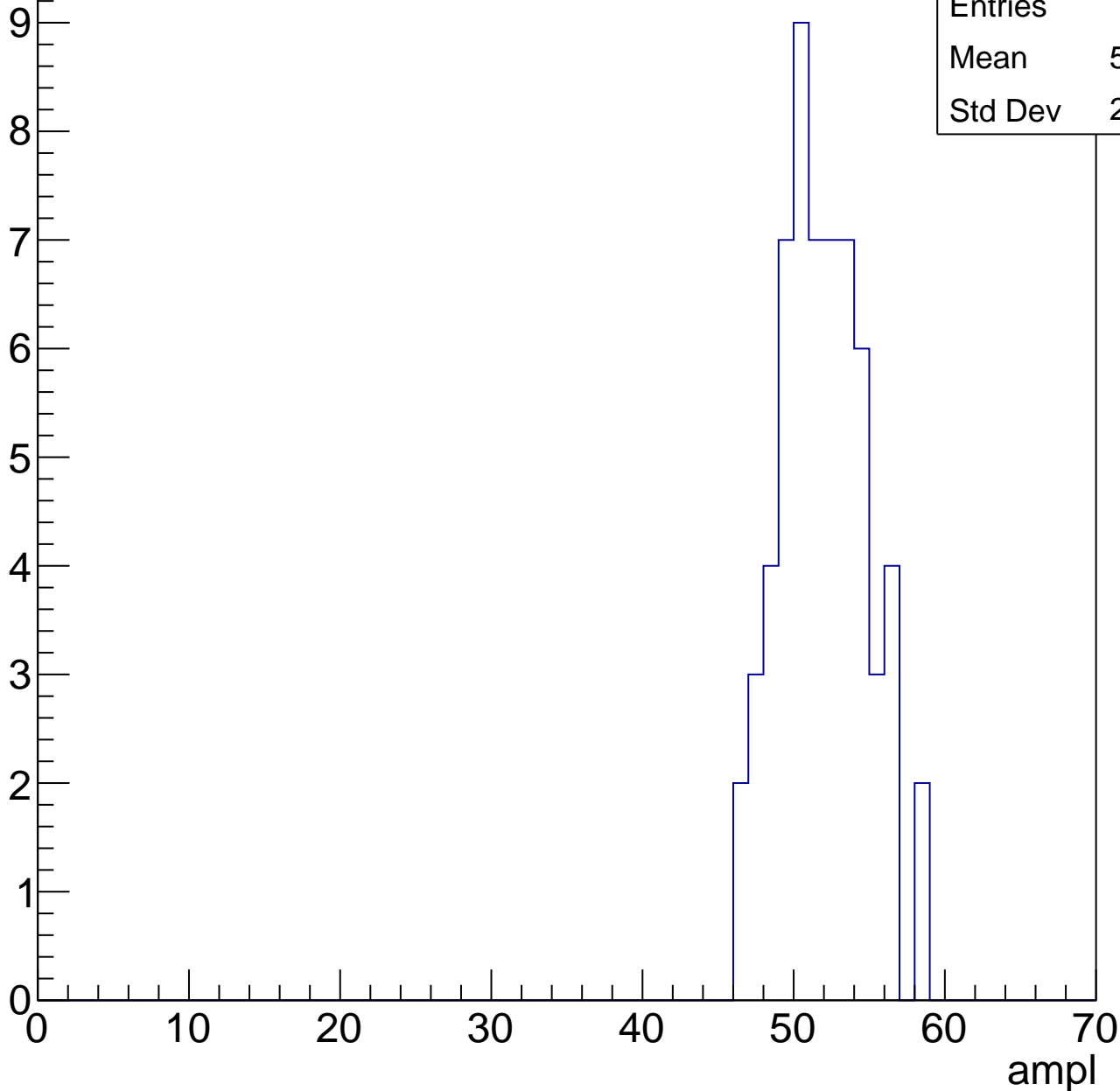


# B1L102S, U8-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	51.46
Std Dev	2.843

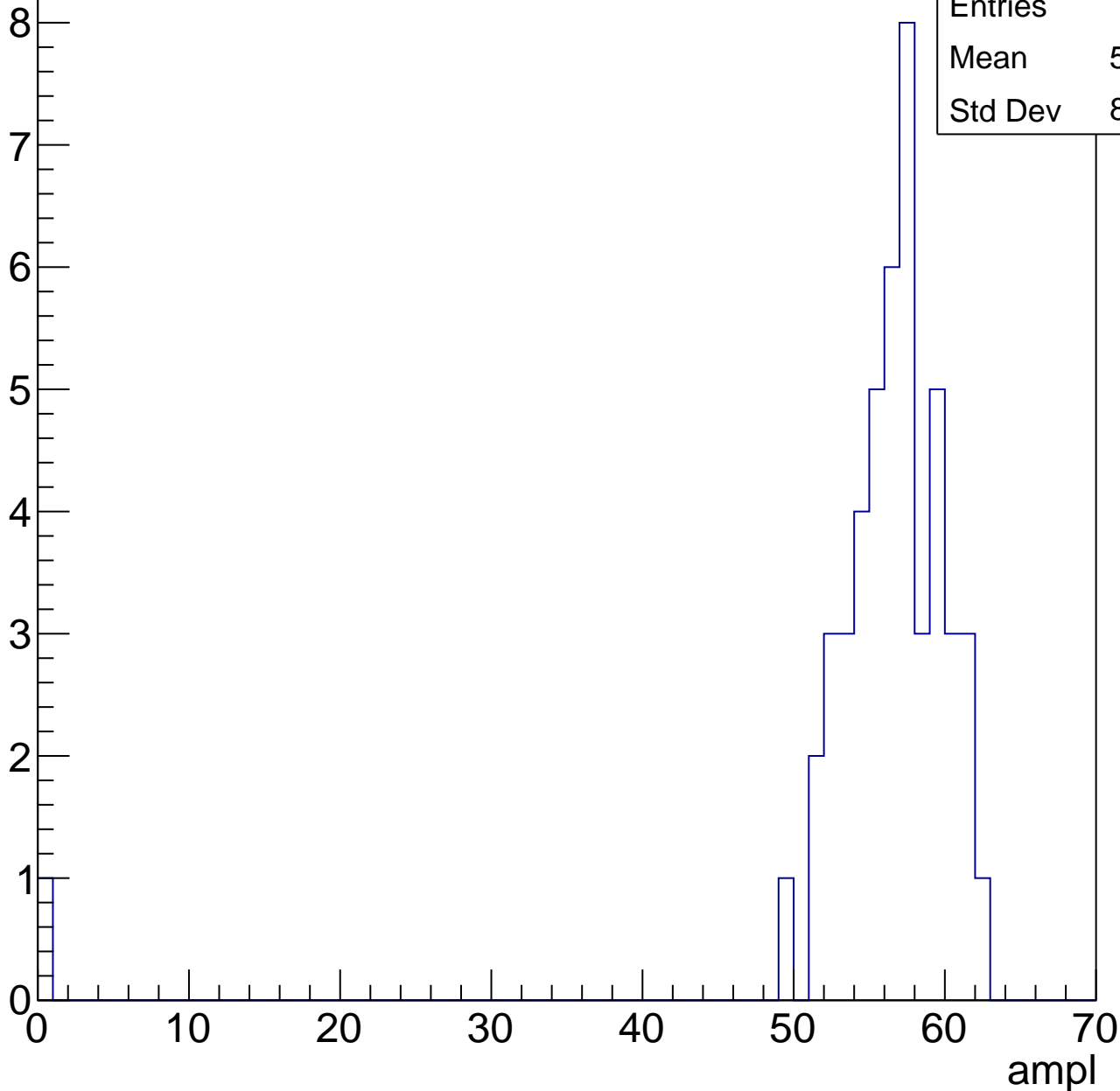


# B1L102S, U8-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	55.06
Std Dev	8.555

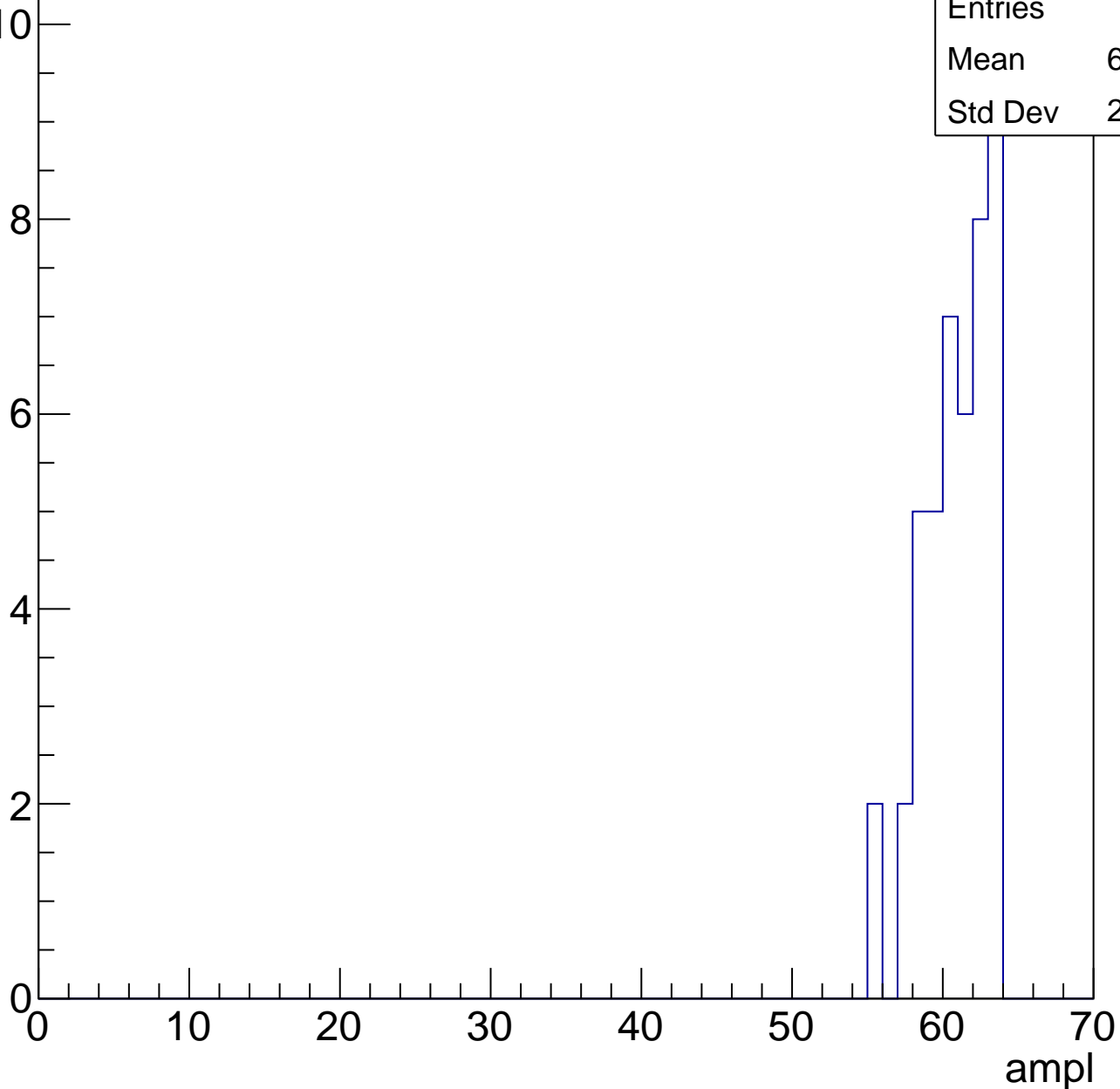


# B1L102S, U8-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

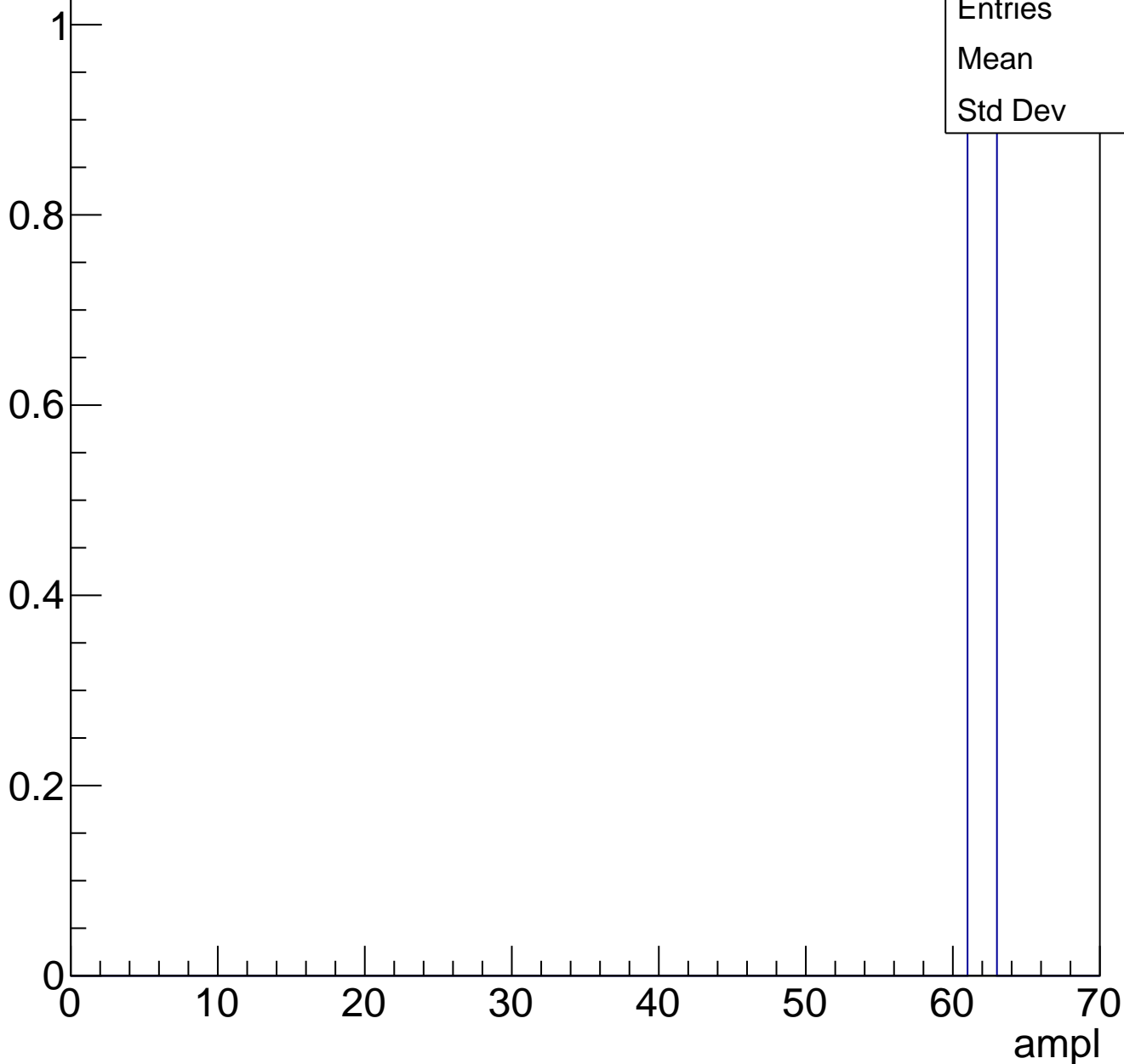
Entries	45
Mean	60.47
Std Dev	2.166



# B1L102S, U8-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U8-ch82, adc0

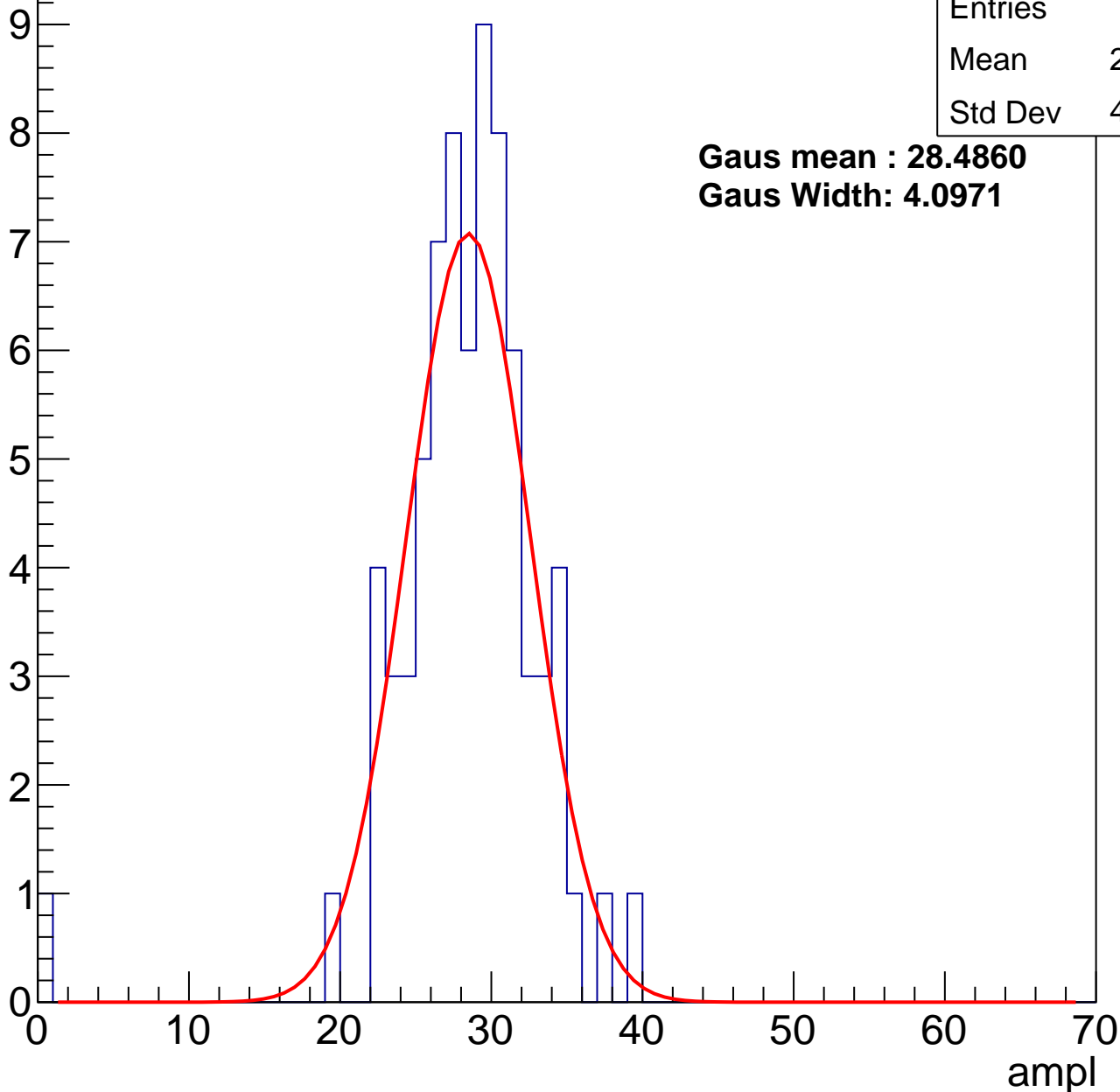
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	27.95
Std Dev	4.967

**Gaus mean : 28.4860**

**Gaus Width: 4.0971**



# B1L102S, U8-ch82, adc1

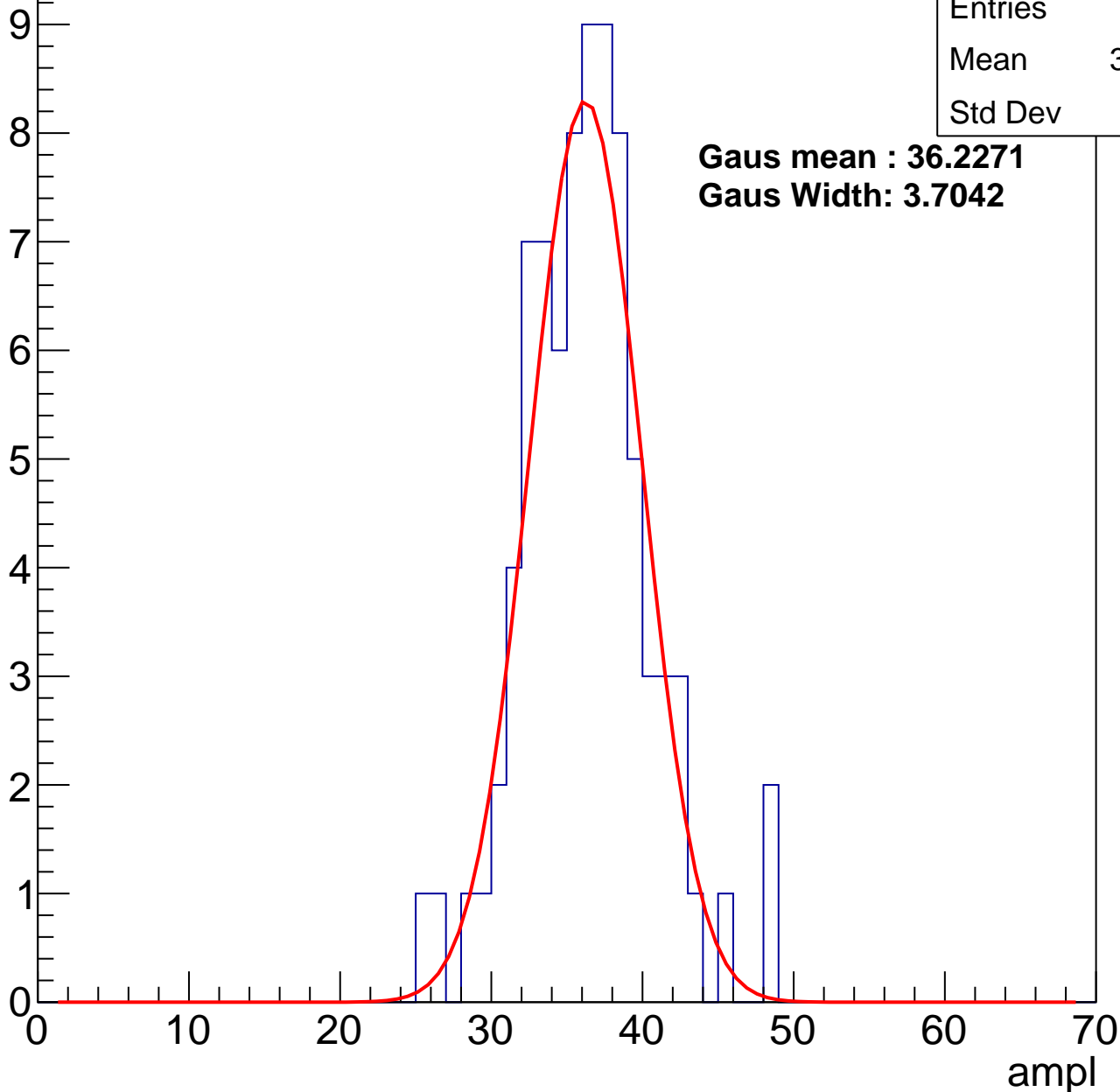
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	35.85
Std Dev	4.2

**Gaus mean : 36.2271**

**Gaus Width: 3.7042**



# B1L102S, U8-ch82, adc2

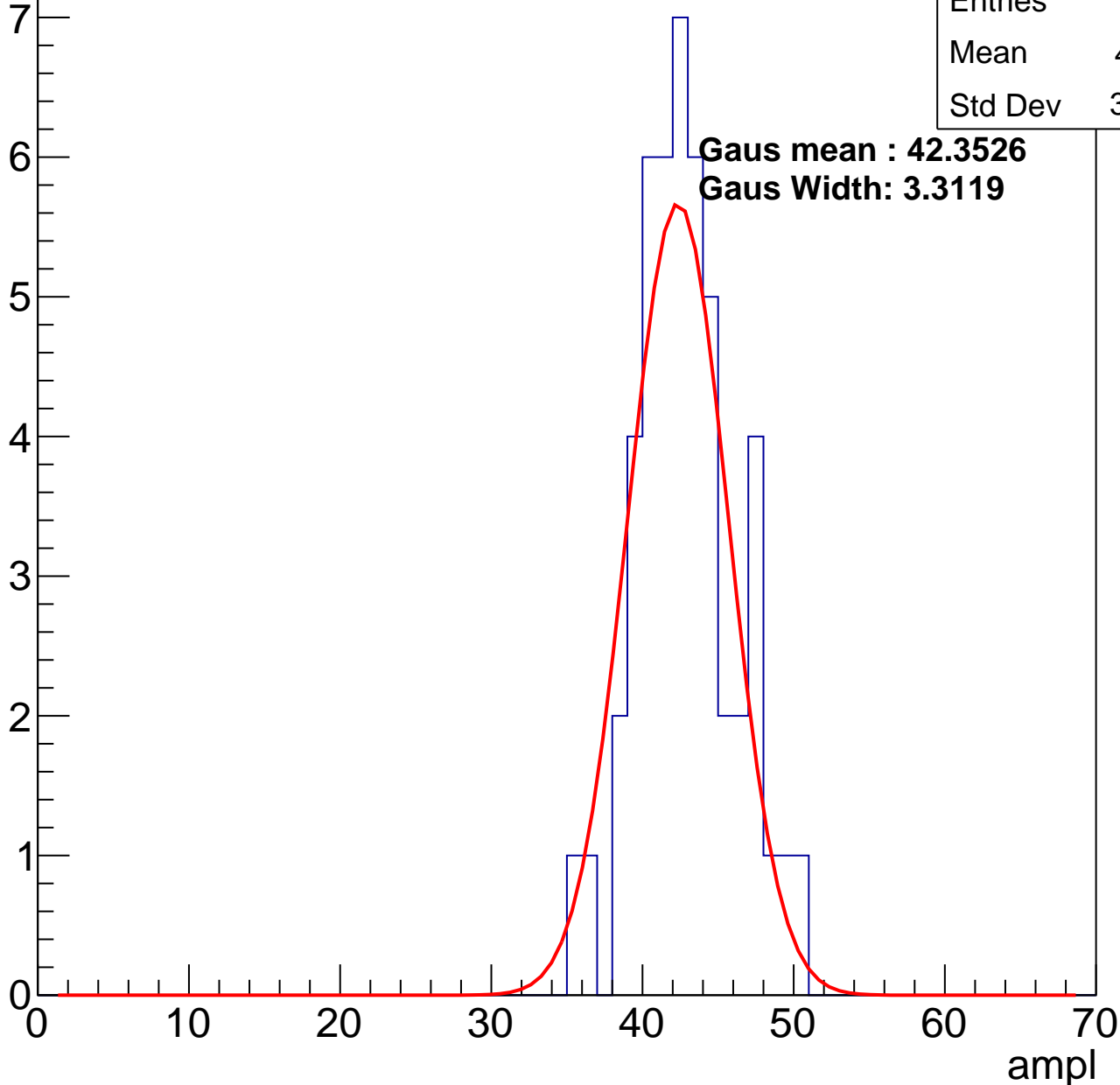
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	42.41
Std Dev	3.194

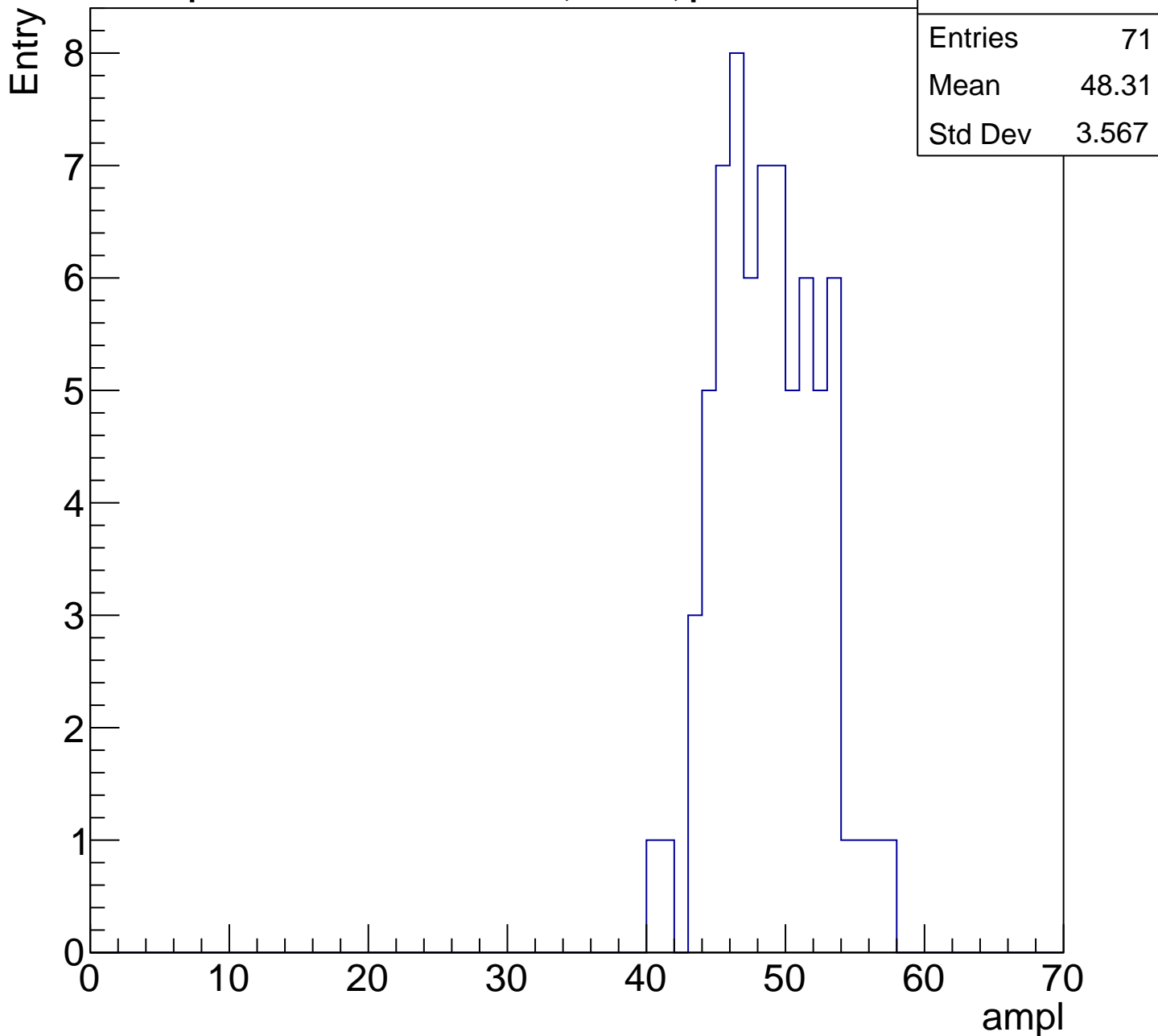
**Gaus mean : 42.3526**

**Gaus Width: 3.3119**



# B1L102S, U8-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

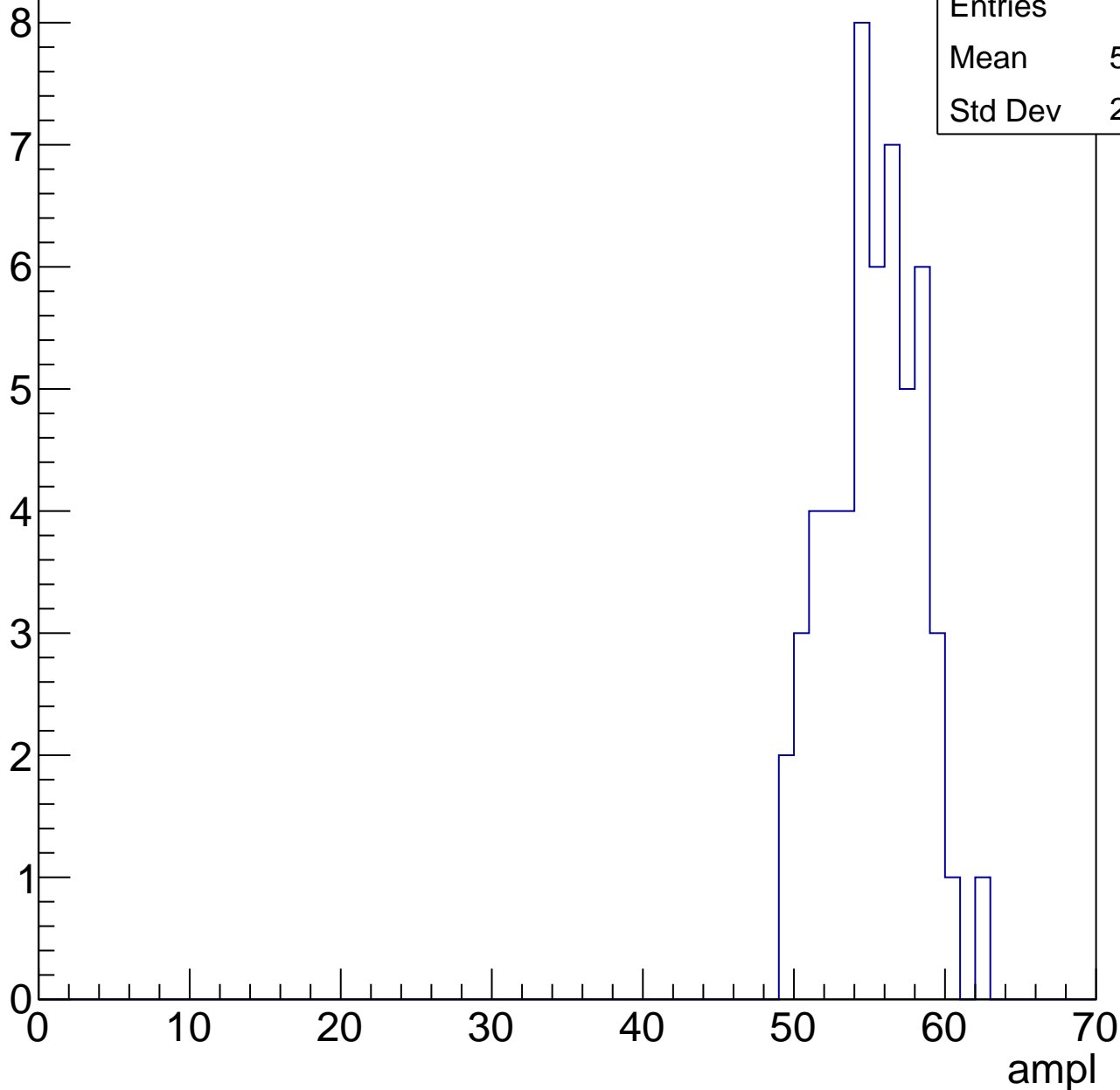


# B1L102S, U8-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	54.78
Std Dev	2.954

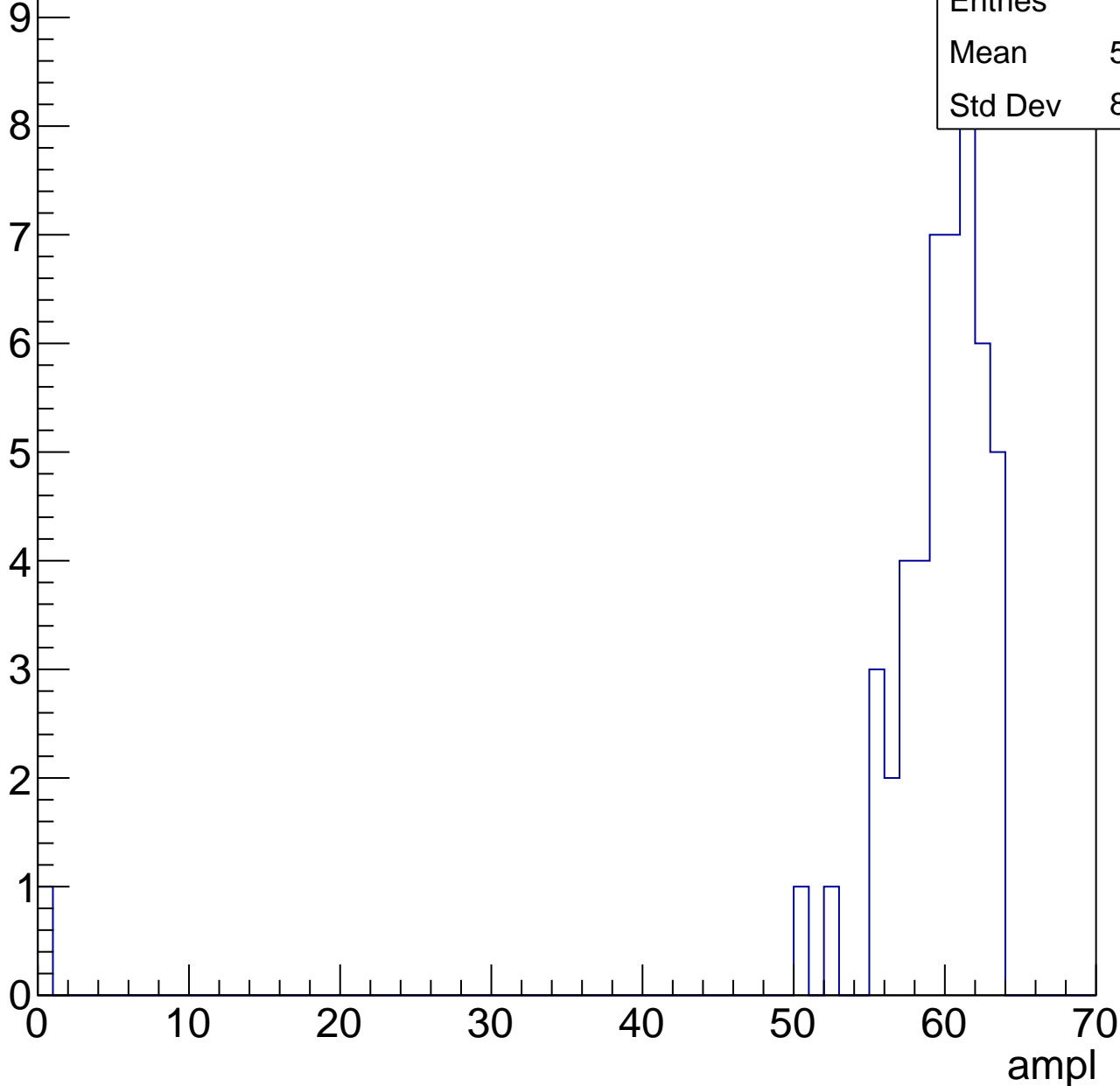


# B1L102S, U8-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	58.16
Std Dev	8.762

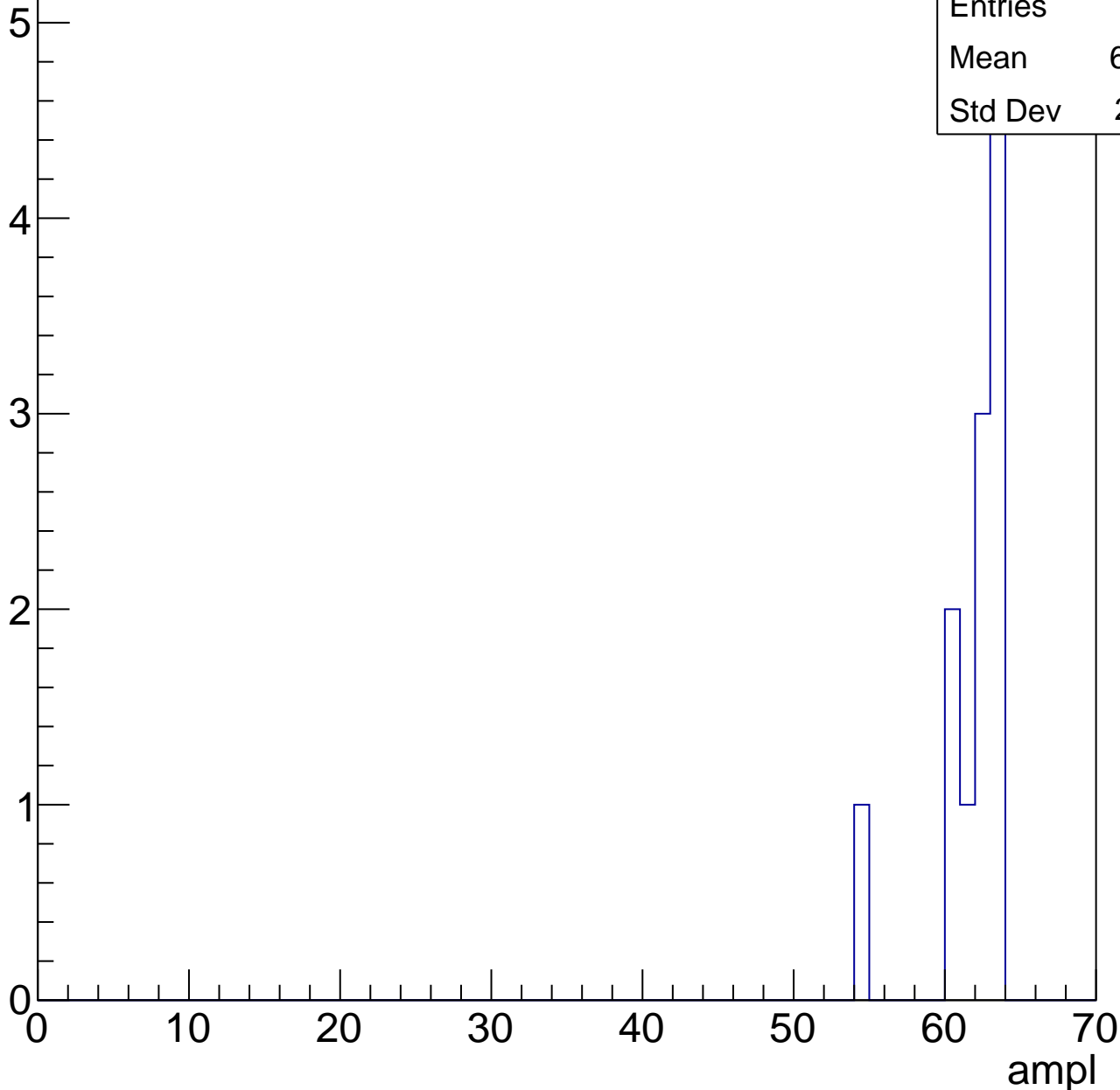


# B1L102S, U8-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	12
Mean	61.33
Std Dev	2.461





# B1L102S, U8-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U8-ch83, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	79
Mean	28.57
Std Dev	4.69

**Gaus mean : 29.4633**

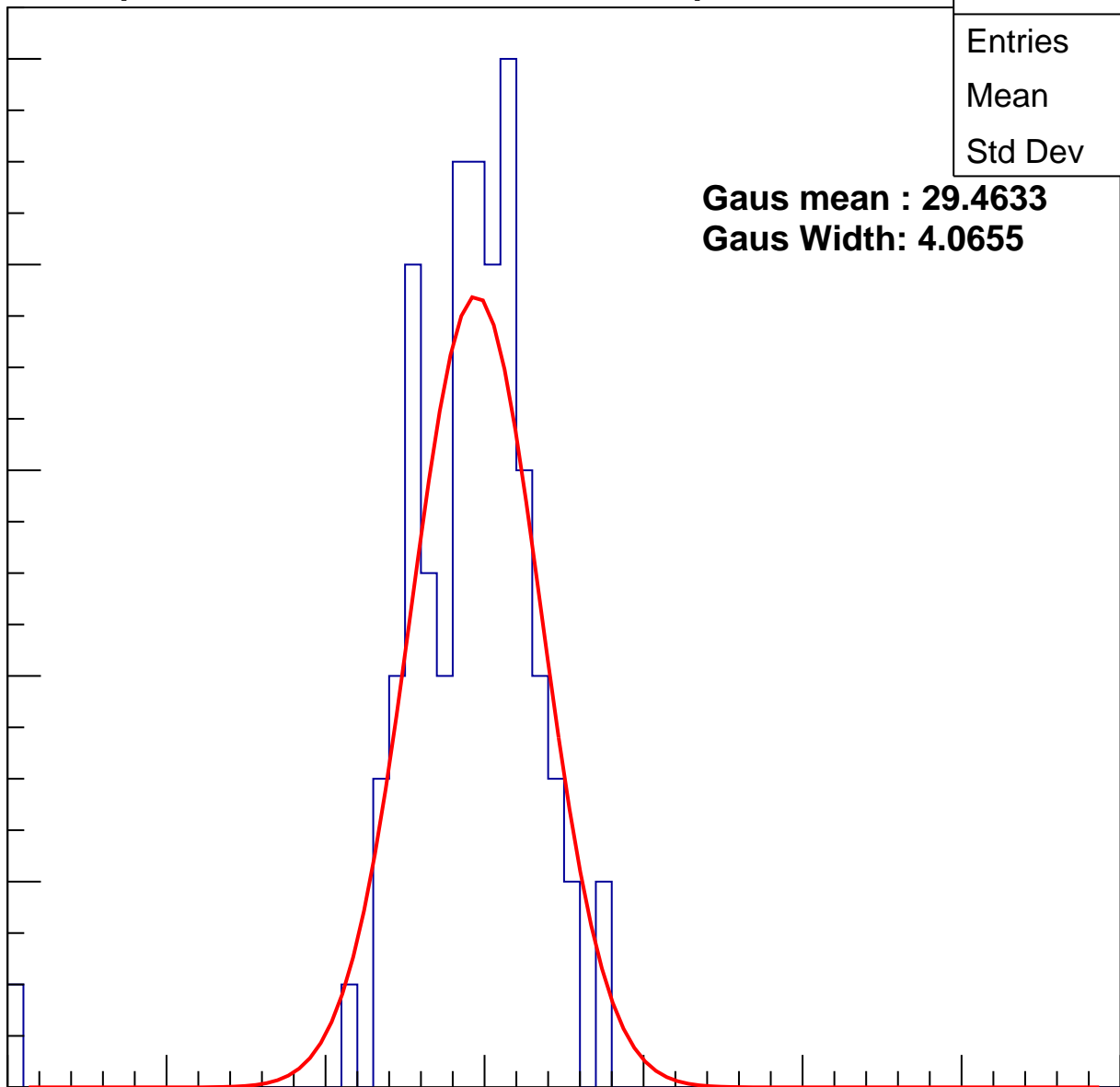
**Gaus Width: 4.0655**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U8-ch83, adc1

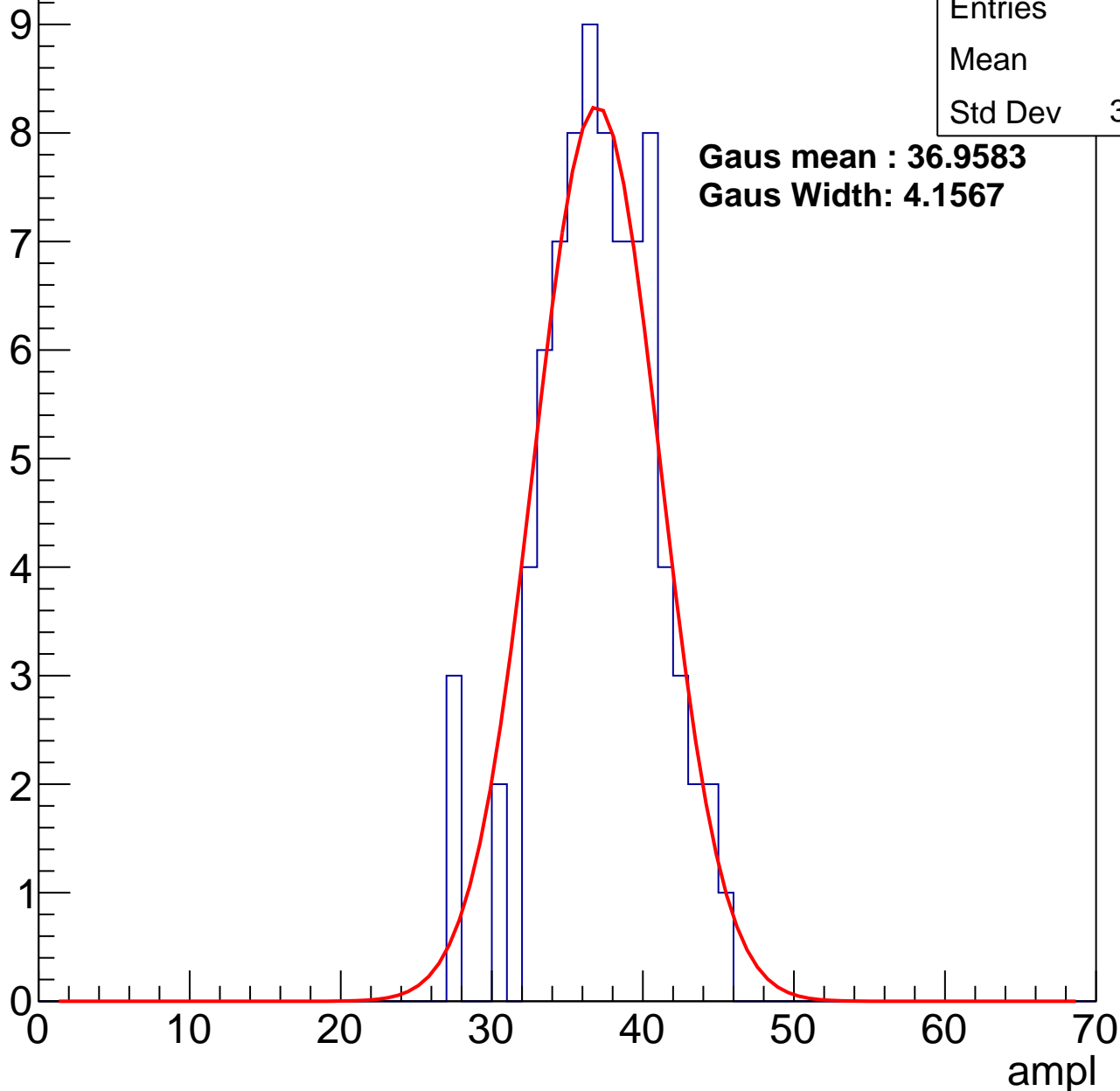
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	81
Mean	36.7
Std Dev	3.802

**Gaus mean : 36.9583**

**Gaus Width: 4.1567**



# B1L102S, U8-ch83, adc2

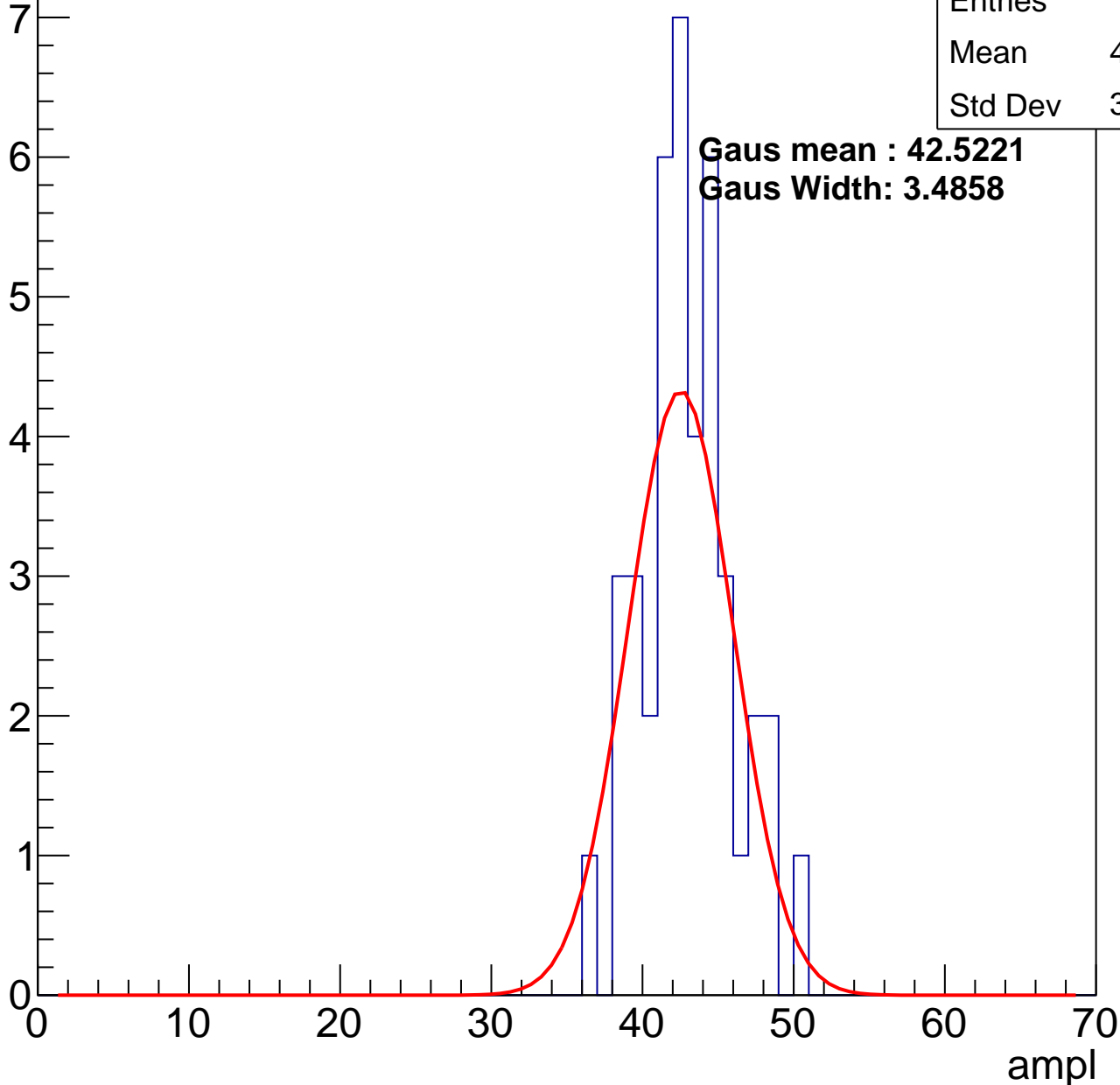
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	41
Mean	42.54
Std Dev	3.005

**Gaus mean : 42.5221**

**Gaus Width: 3.4858**

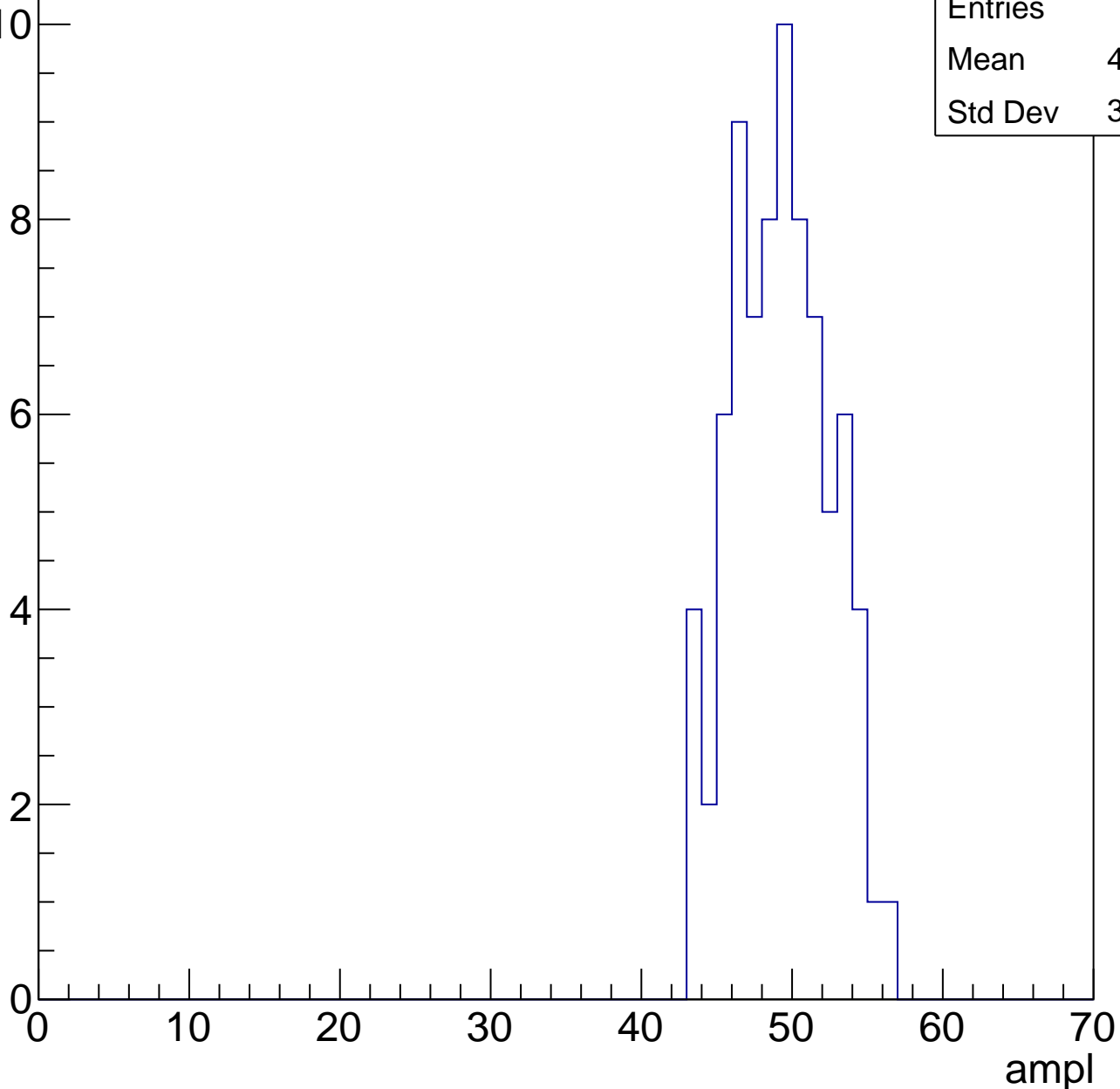


# B1L102S, U8-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	48.83
Std Dev	3.135

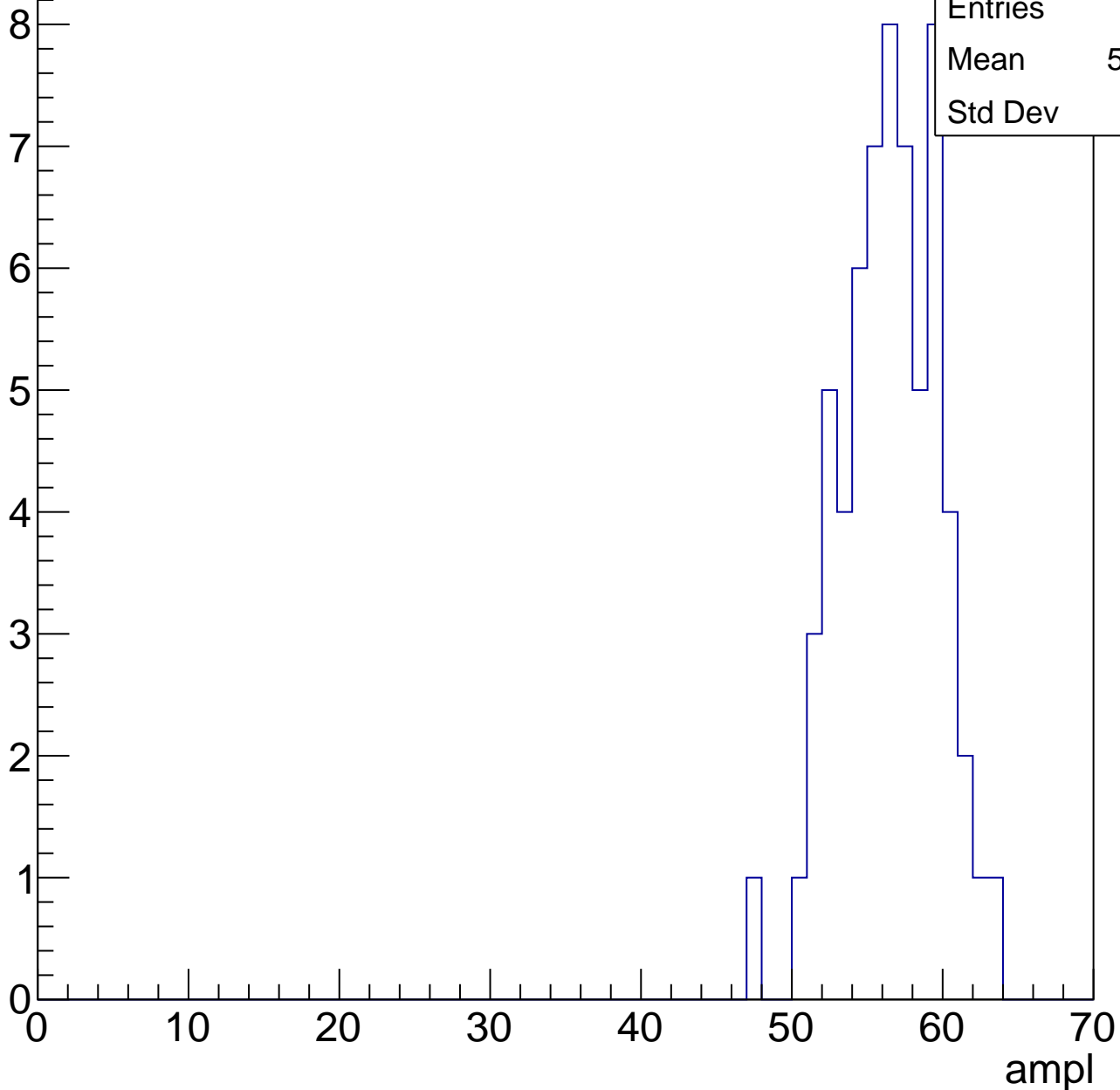


# B1L102S, U8-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	55.98
Std Dev	3.18

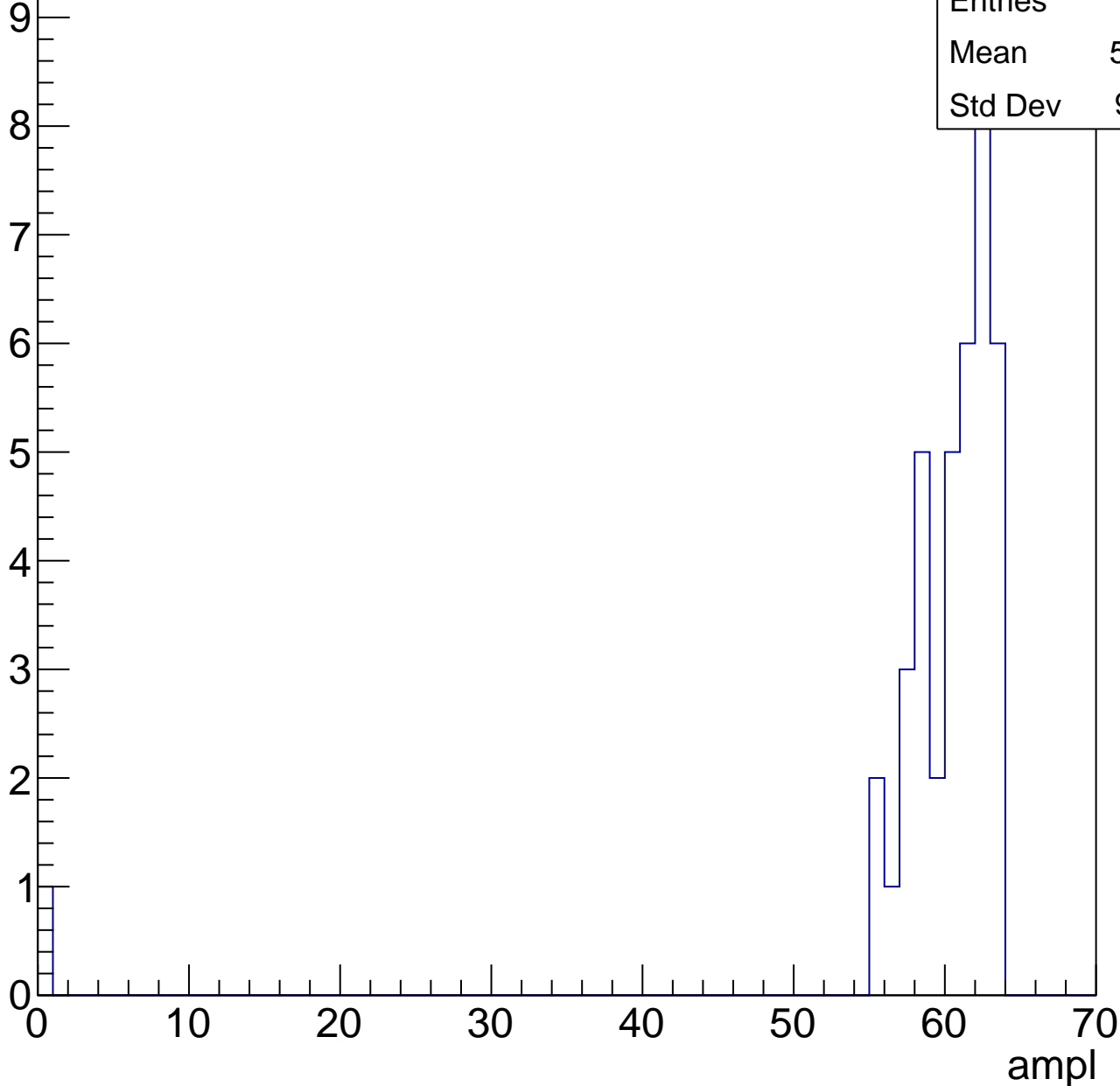


# B1L102S, U8-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

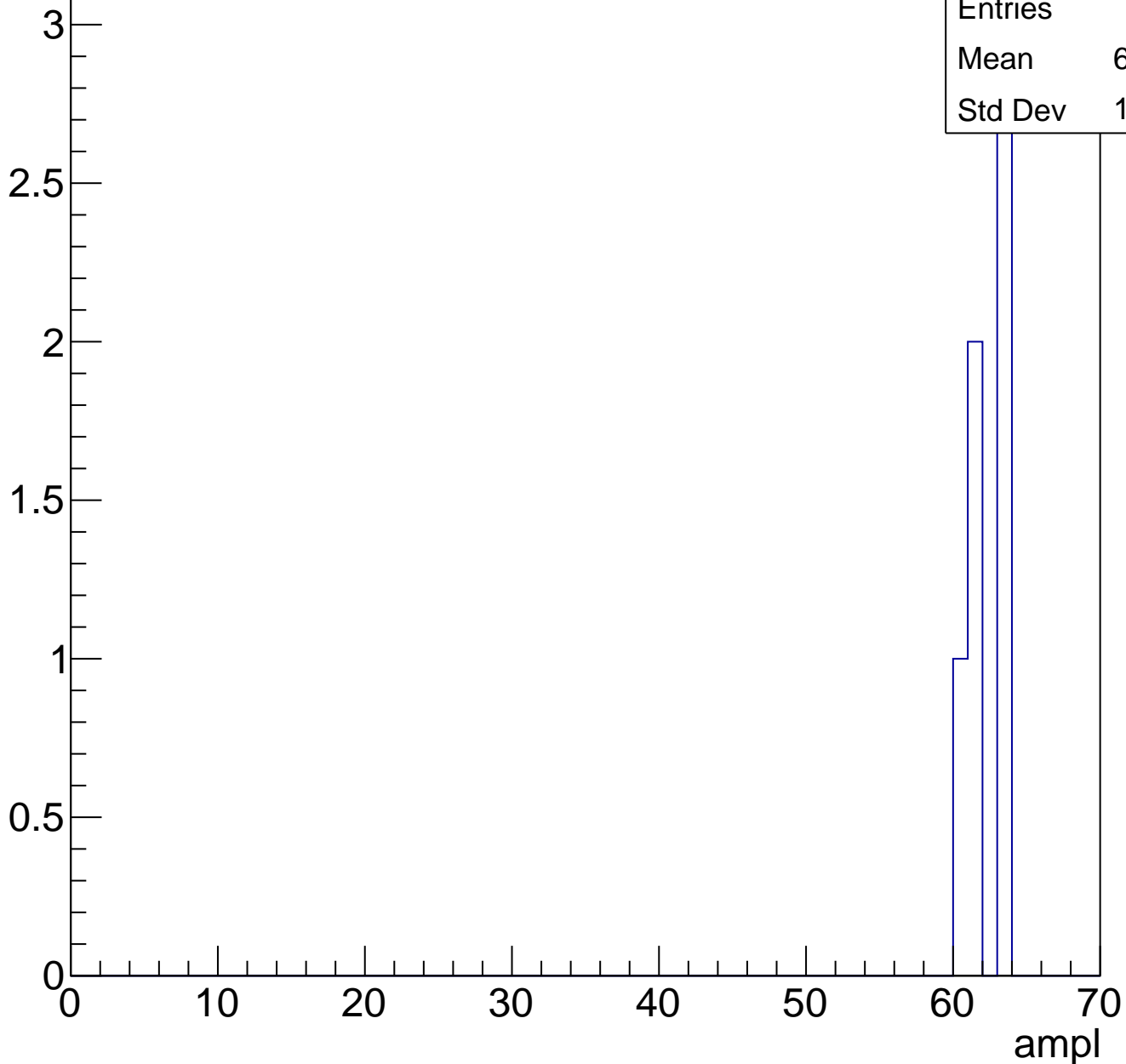
Entries	40
Mean	58.67
Std Dev	9.671



# B1L102S, U8-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch84, adc0

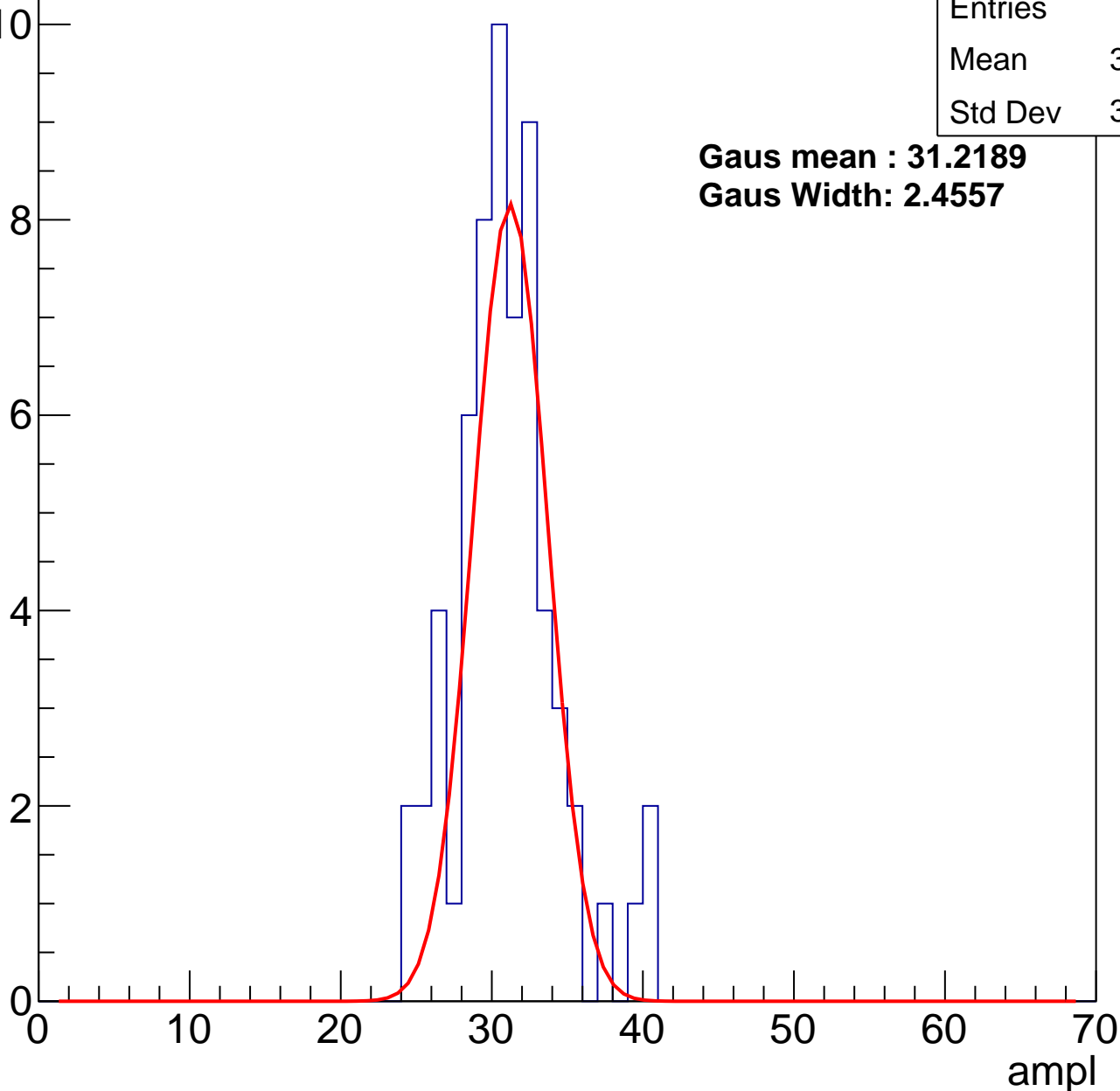
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	30.55
Std Dev	3.397

**Gaus mean : 31.2189**

**Gaus Width: 2.4557**



# B1L102S, U8-ch84, adc1

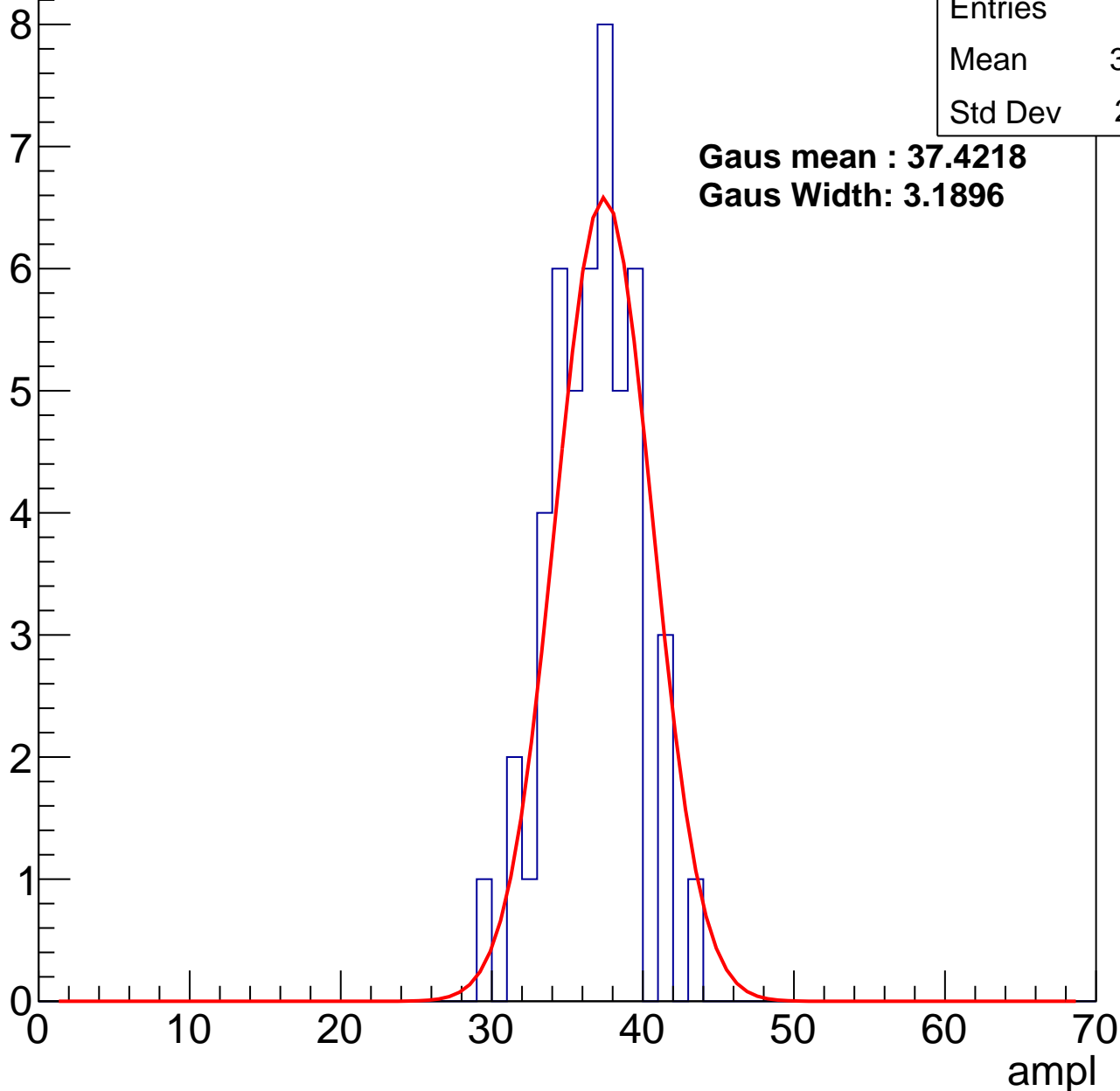
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	36.17
Std Dev	2.831

**Gaus mean : 37.4218**

**Gaus Width: 3.1896**



# B1L102S, U8-ch84, adc2

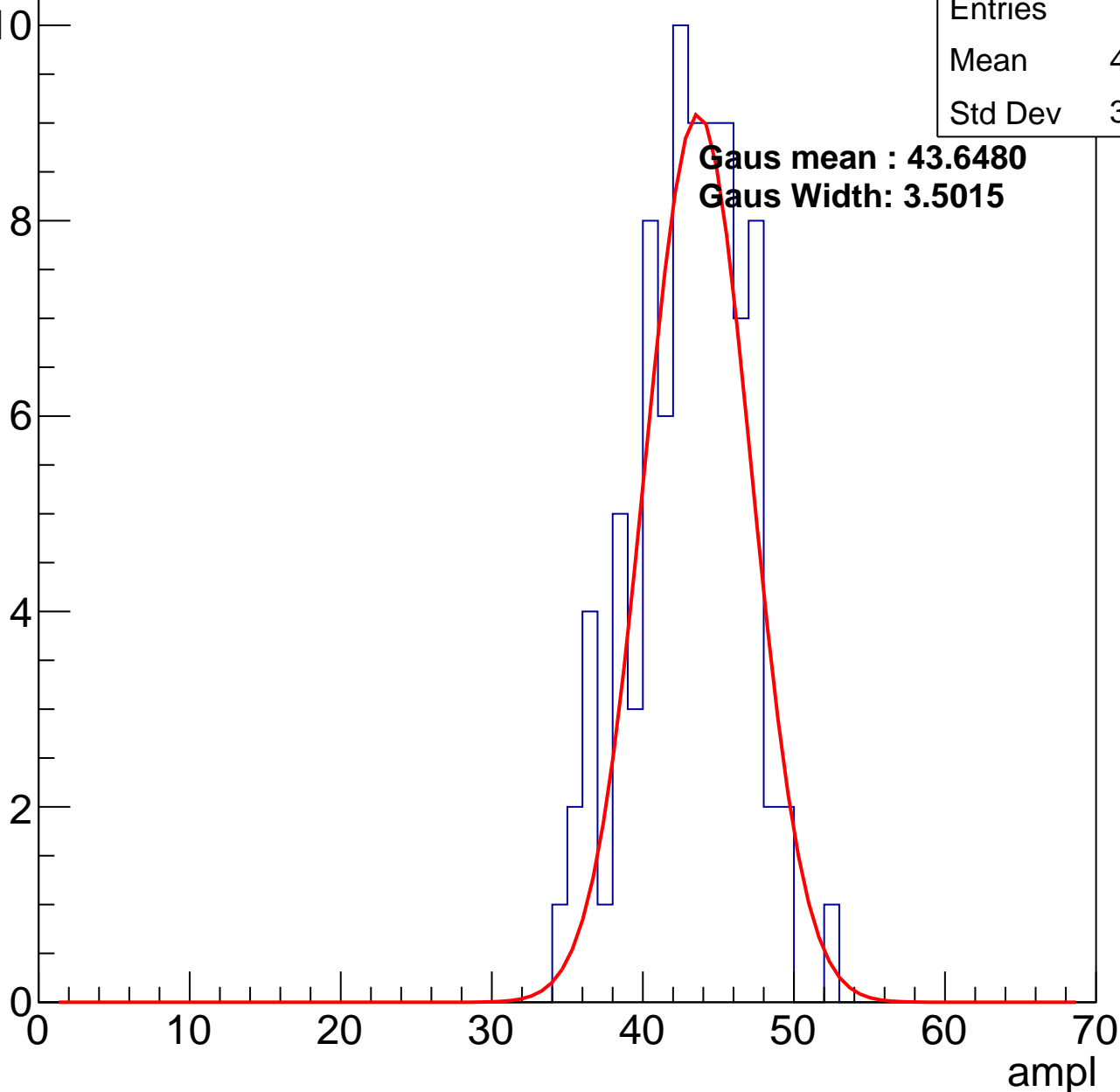
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	87
Mean	42.64
Std Dev	3.632

**Gaus mean : 43.6480**

**Gaus Width: 3.5015**

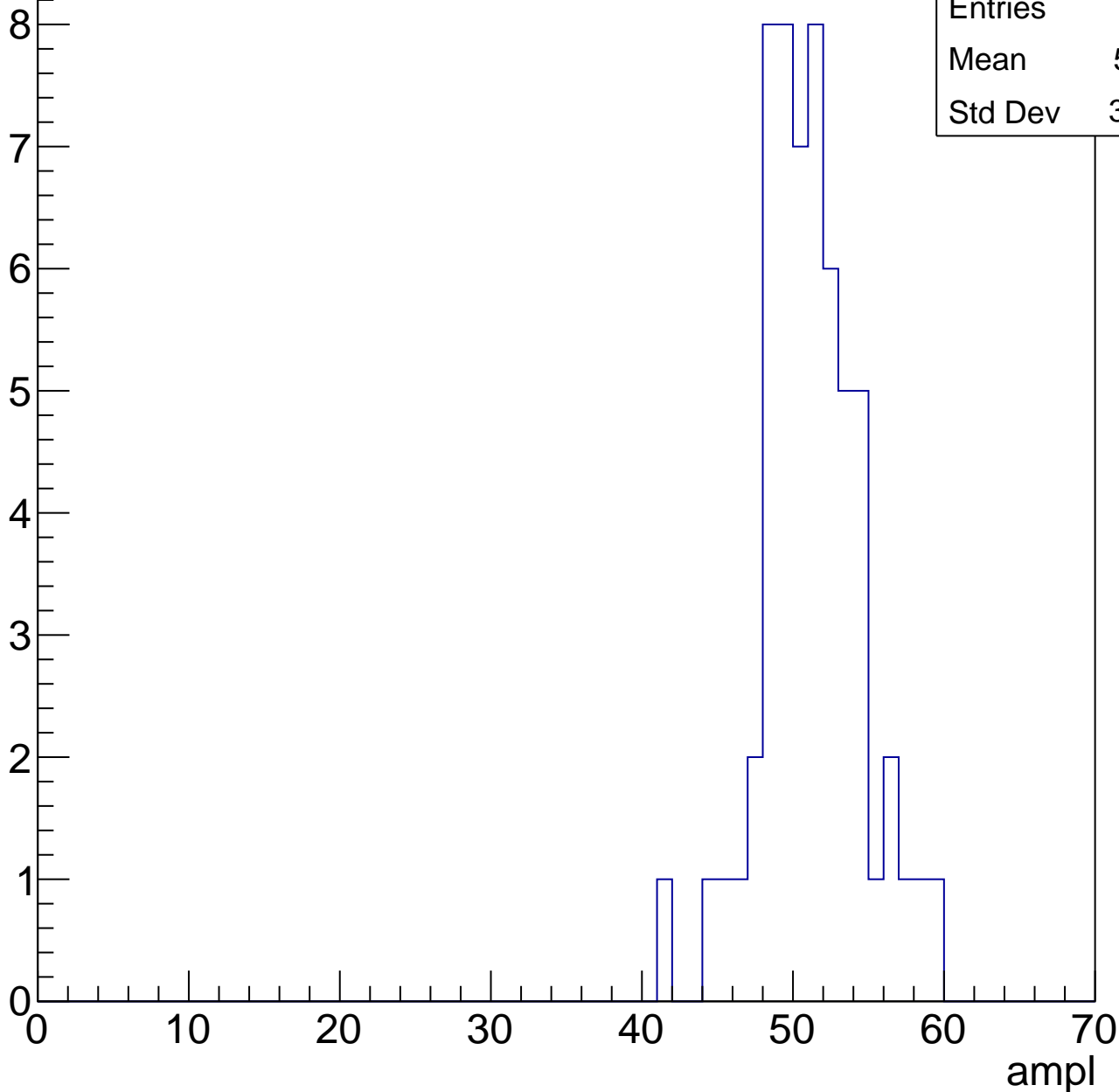


# B1L102S, U8-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

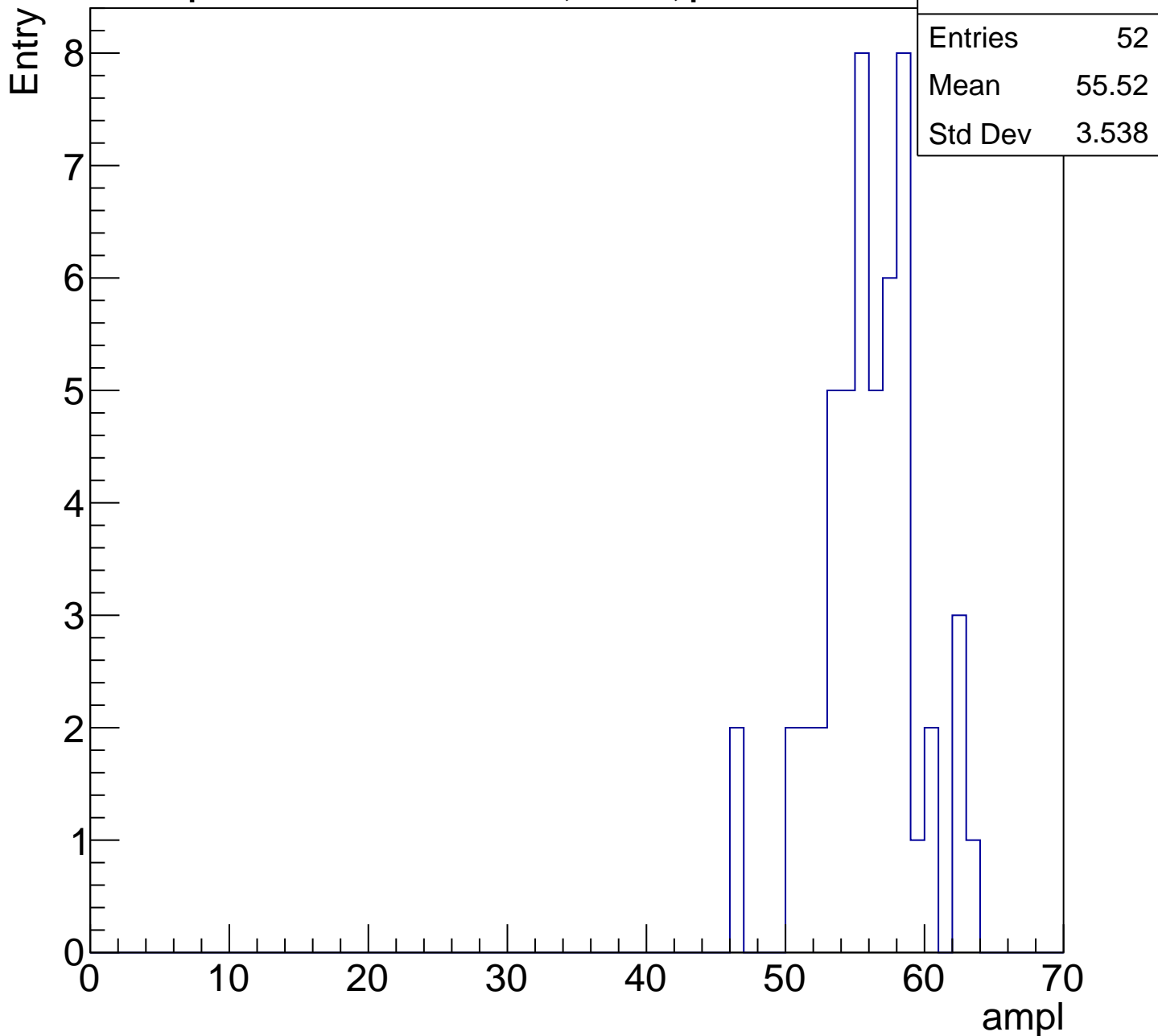
Entry

Entries	59
Mean	50.71
Std Dev	3.278



# B1L102S, U8-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U8-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	47
Mean	59.74
Std Dev	2.779

ampl

0 10 20 30 40 50 60 70

50

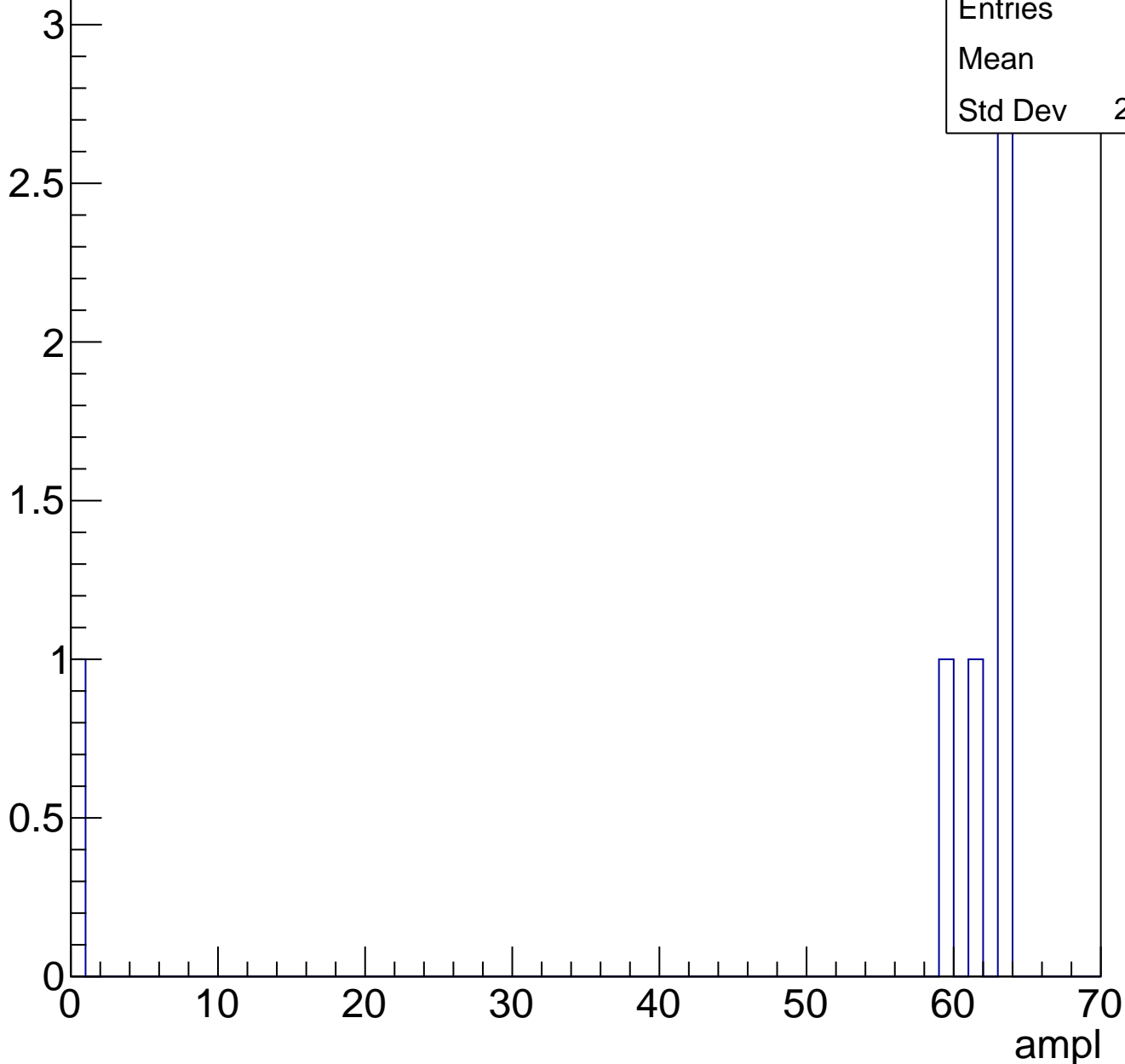
60

70

# B1L102S, U8-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

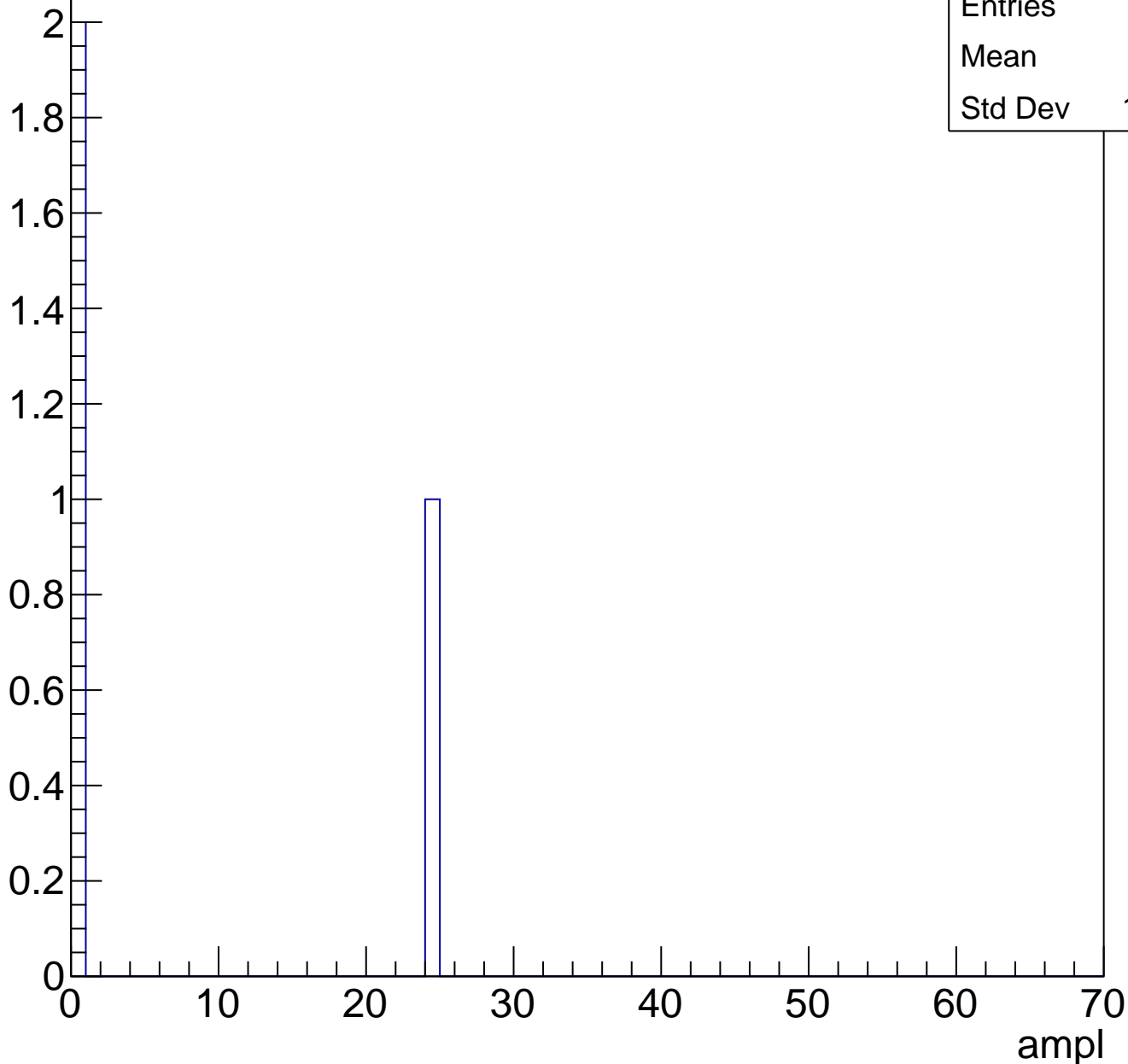




# B1L102S, U8-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch85, adc0

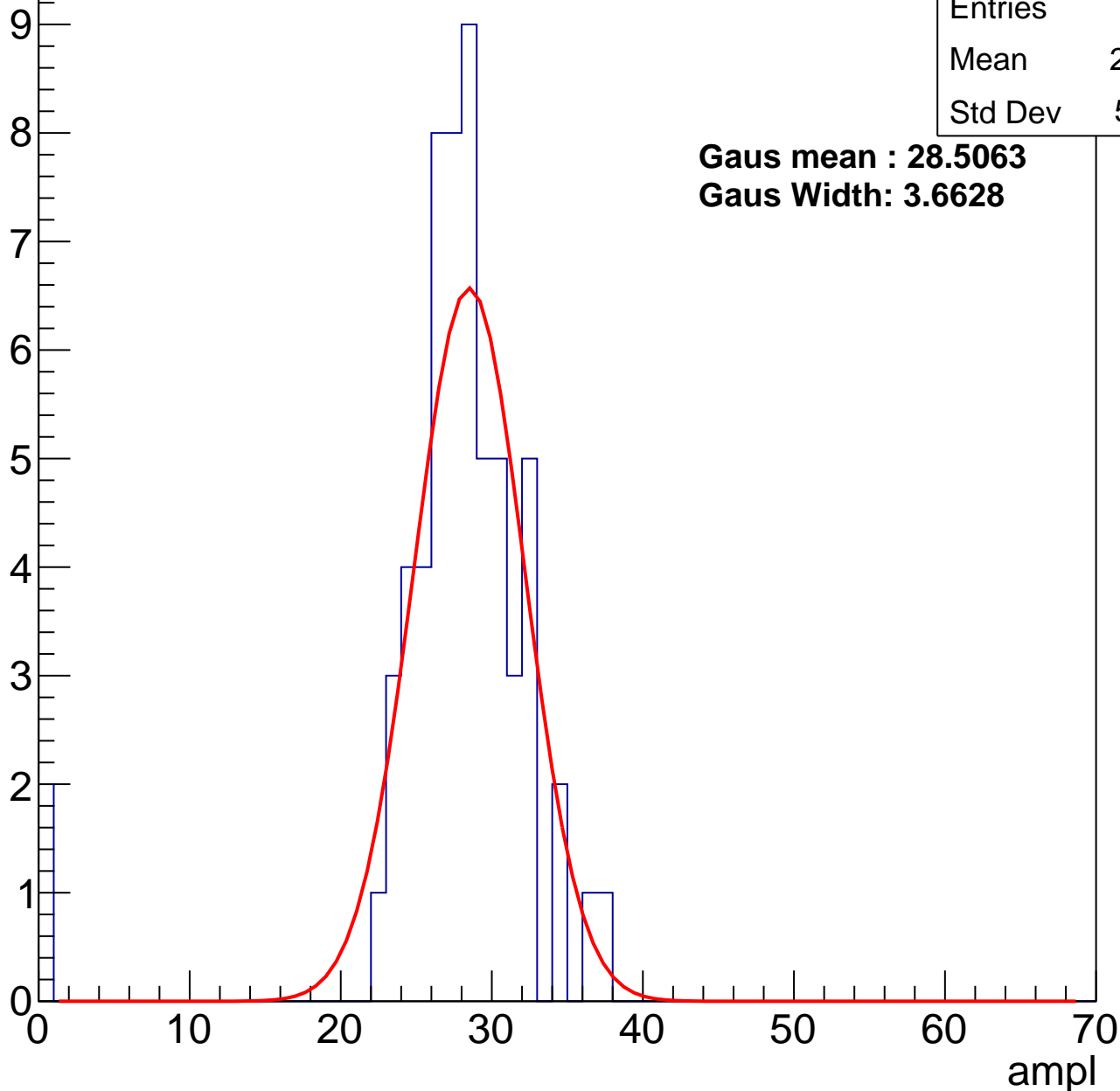
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	27.08
Std Dev	5.891

**Gaus mean : 28.5063**

**Gaus Width: 3.6628**



# B1L102S, U8-ch85, adc1

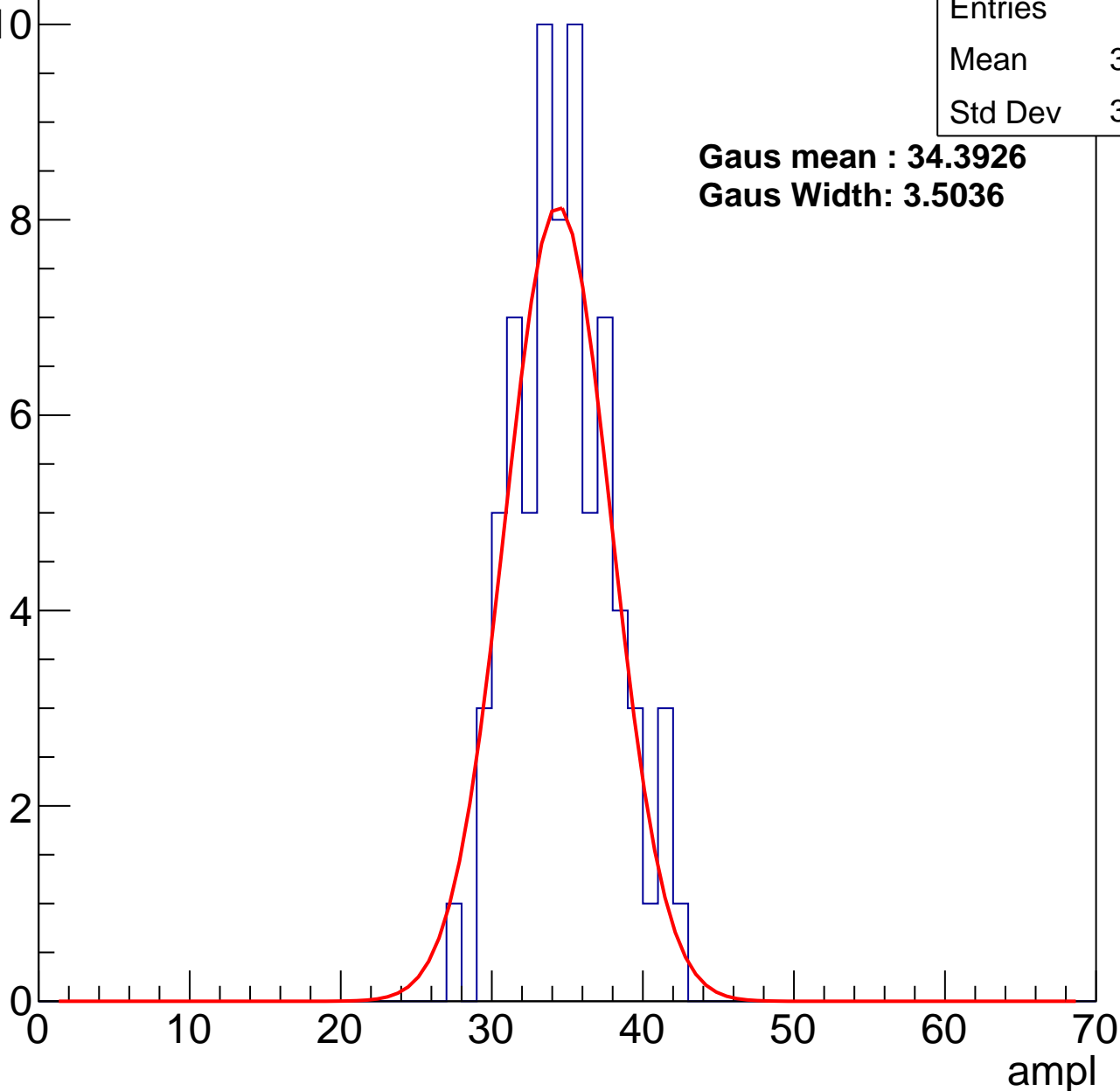
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	34.33
Std Dev	3.244

**Gaus mean : 34.3926**

**Gaus Width: 3.5036**



# B1L102S, U8-ch85, adc2

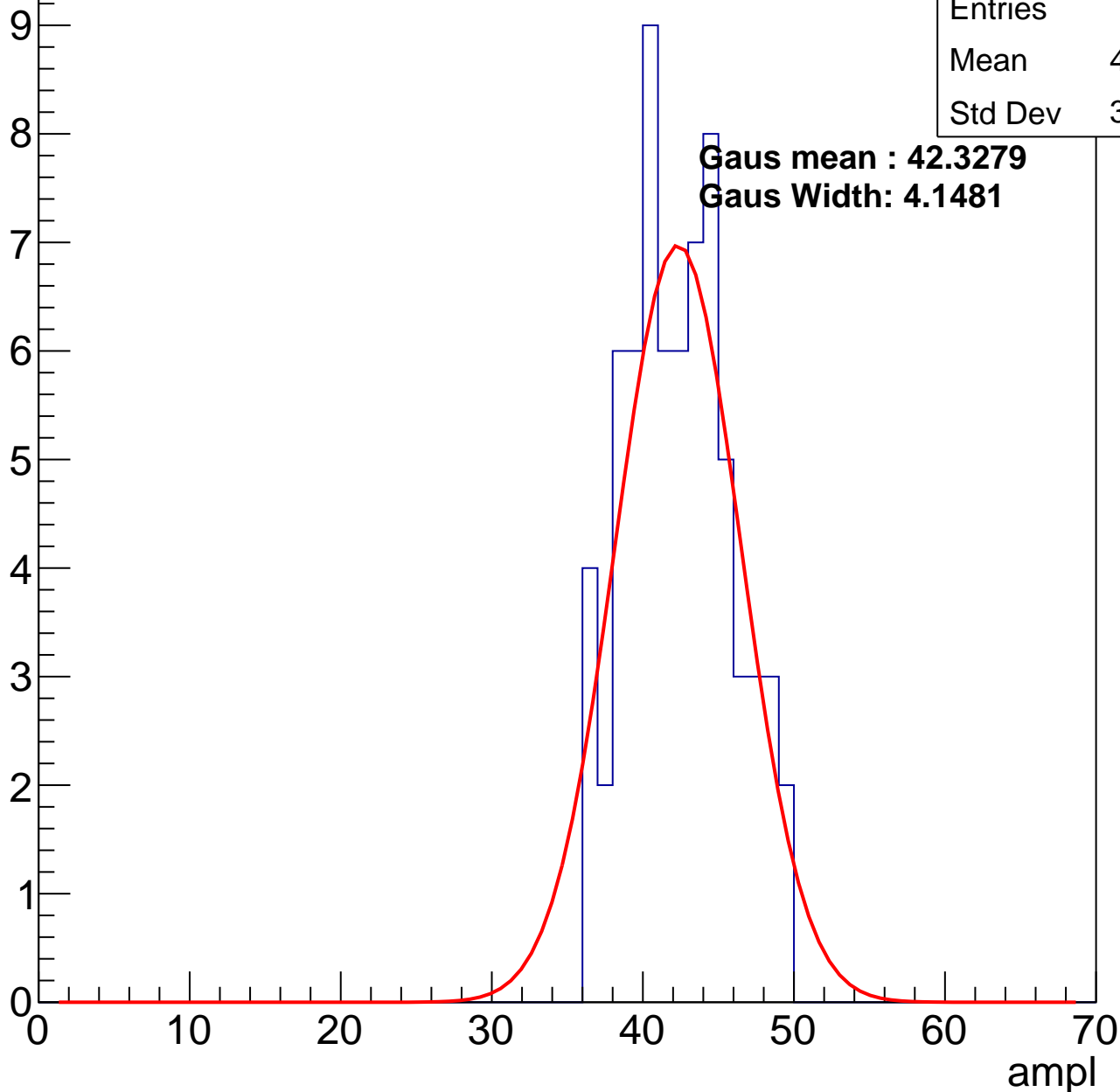
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	41.96
Std Dev	3.378

**Gaus mean : 42.3279**

**Gaus Width: 4.1481**

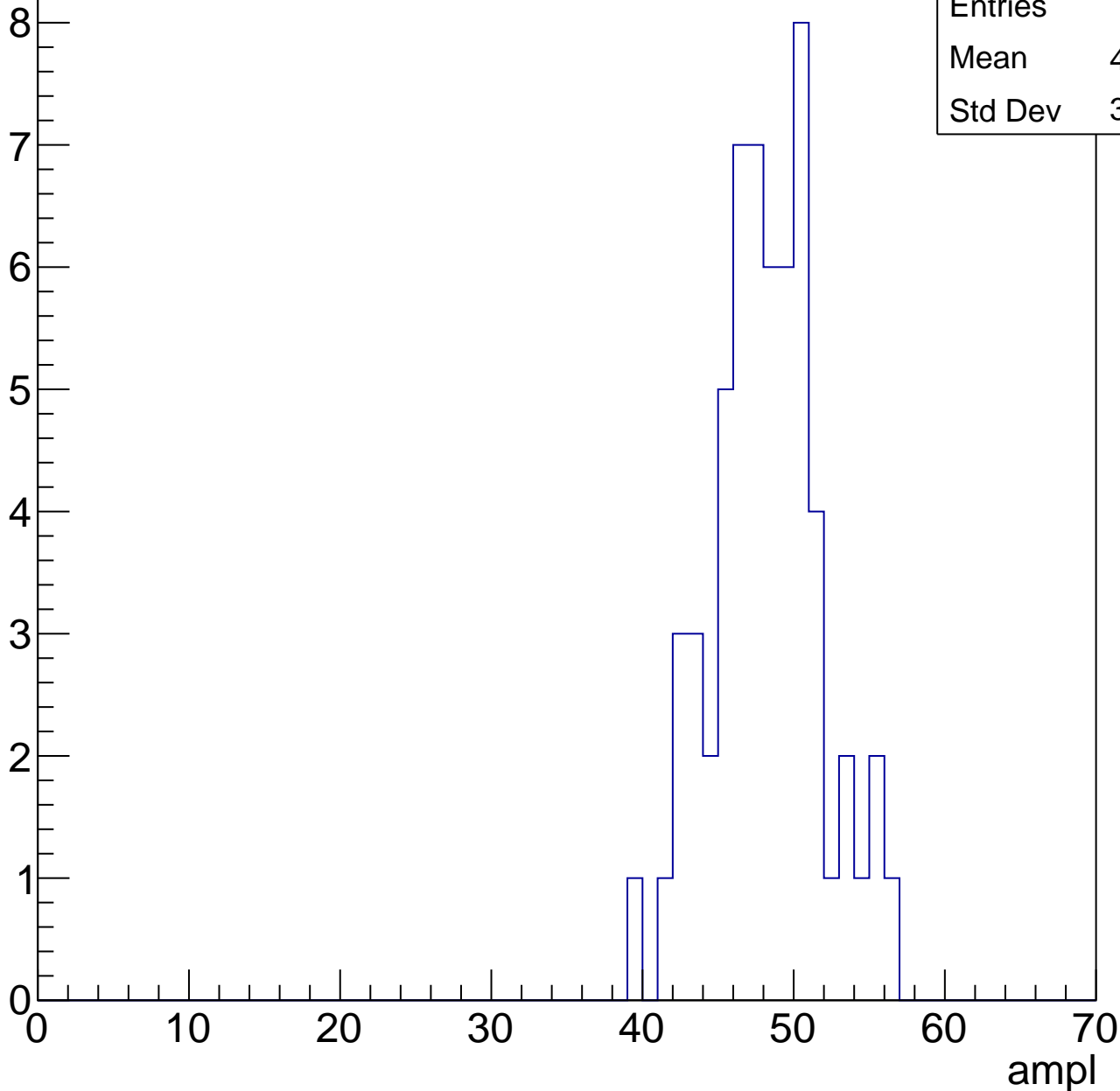


# B1L102S, U8-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

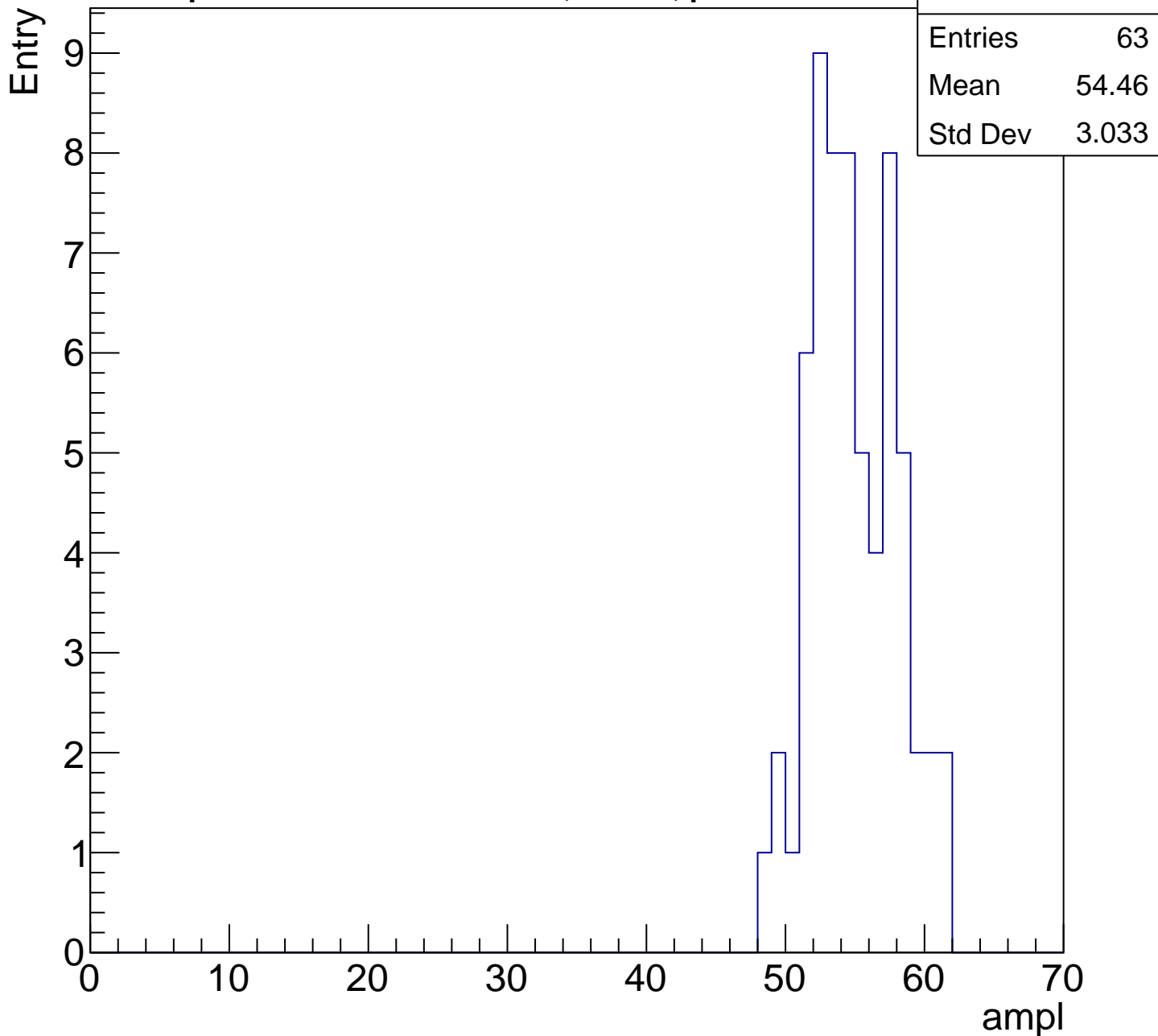
Entry

Entries	60
Mean	47.72
Std Dev	3.555



# B1L102S, U8-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

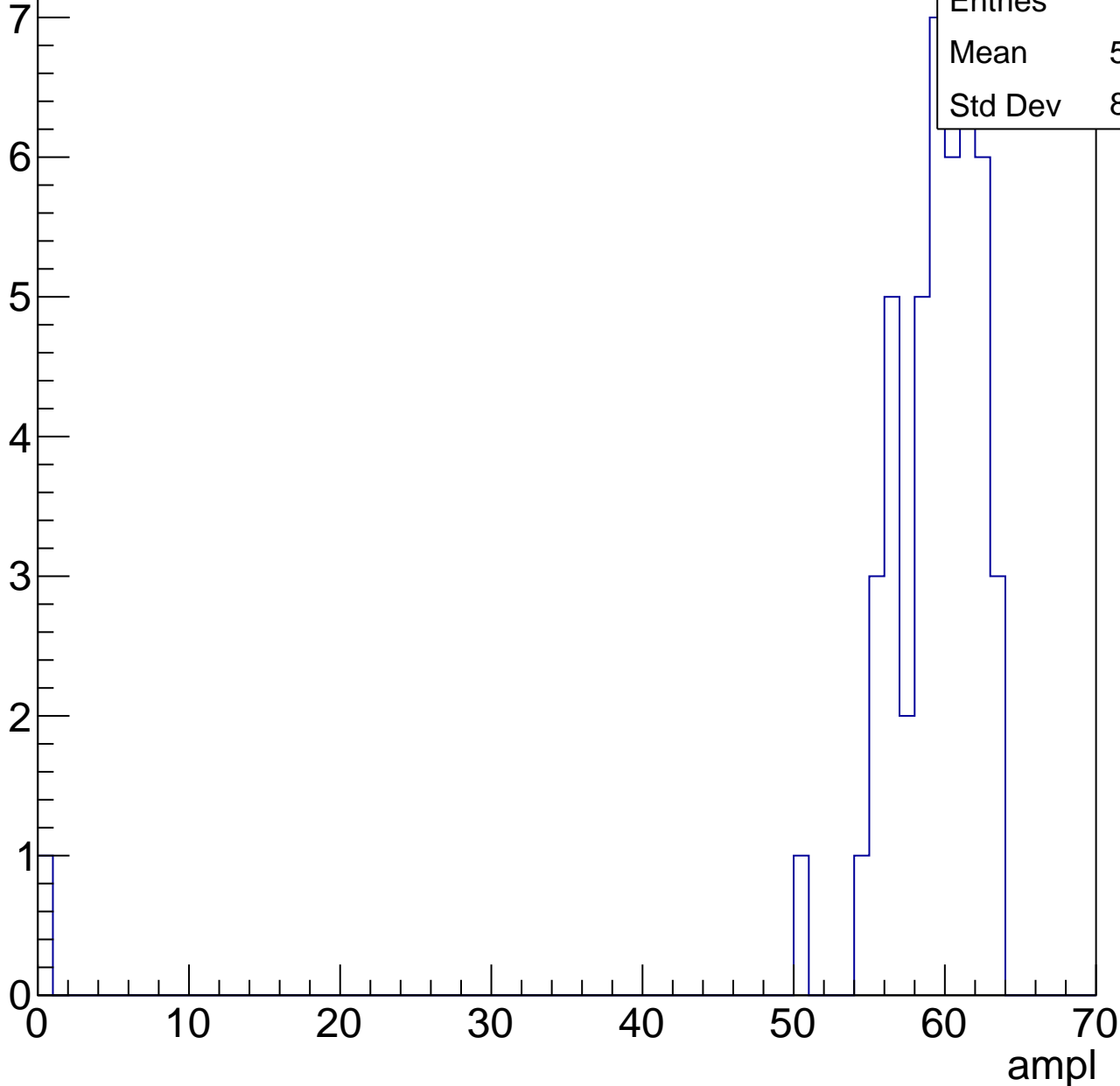


# B1L102S, U8-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	57.74
Std Dev	8.938

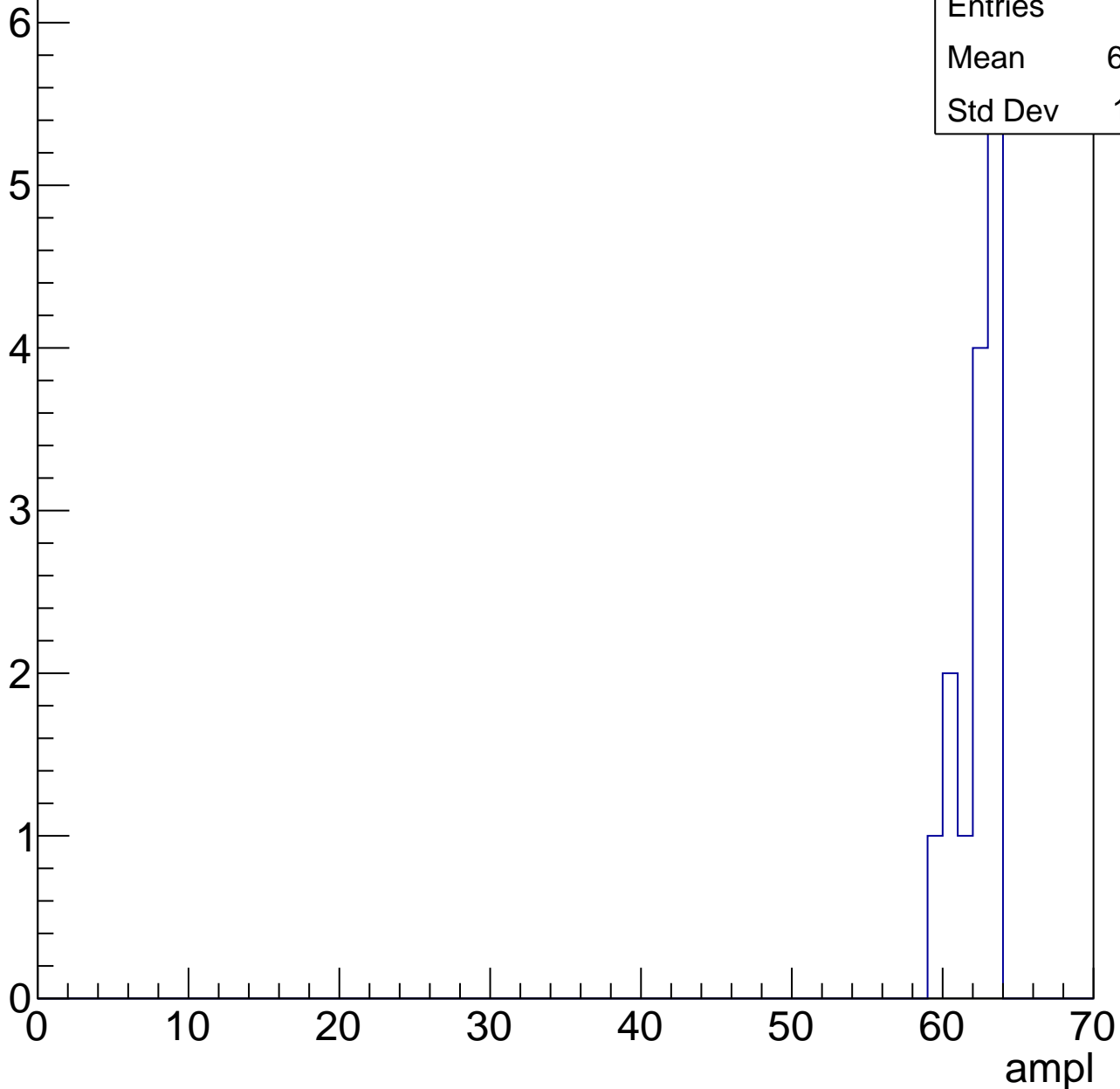


# B1L102S, U8-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	14
Mean	61.86
Std Dev	1.301





# B1L102S, U8-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch86, adc0

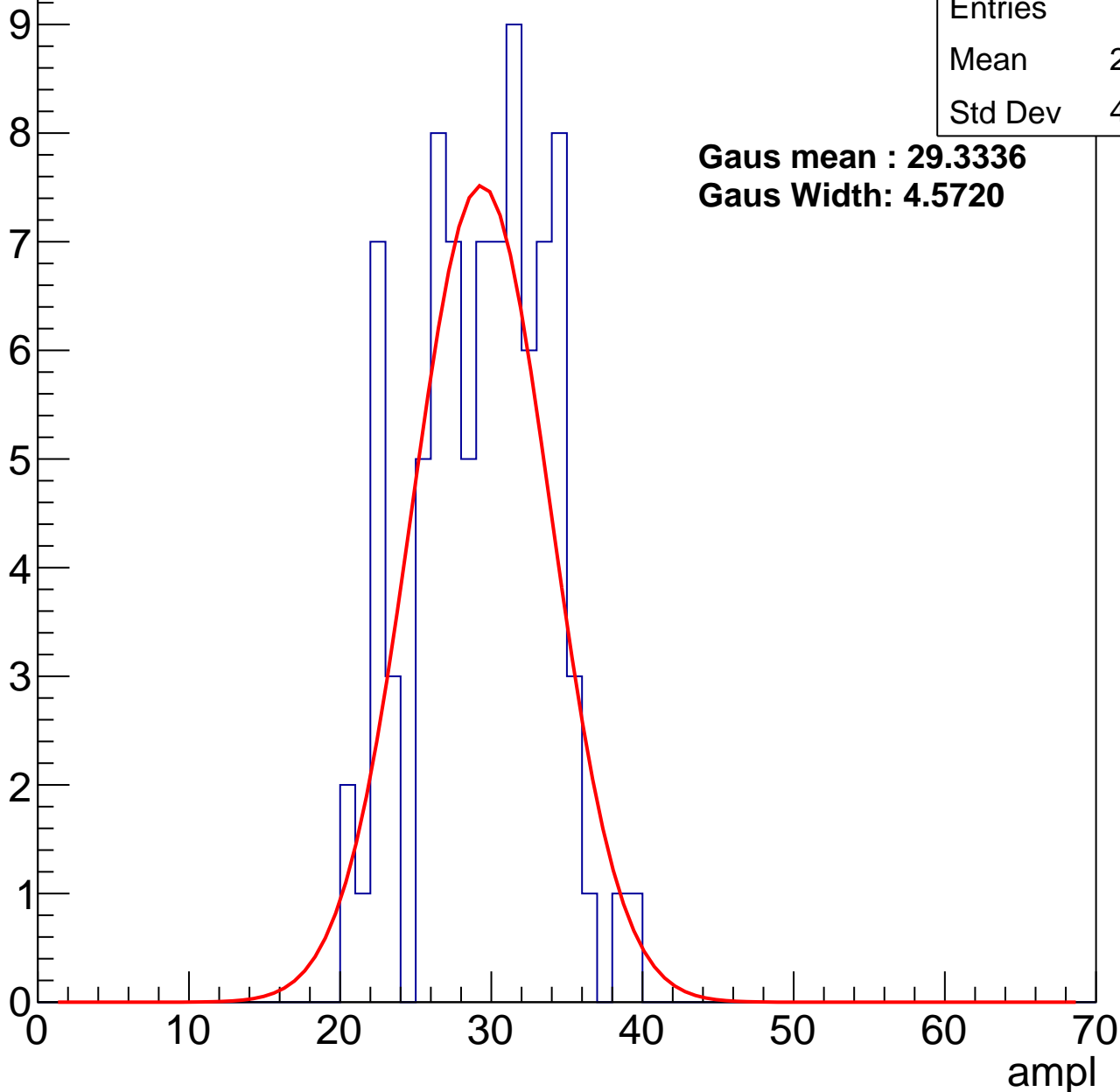
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	88
Mean	28.99
Std Dev	4.276

**Gaus mean : 29.3336**

**Gaus Width: 4.5720**



# B1L102S, U8-ch86, adc1

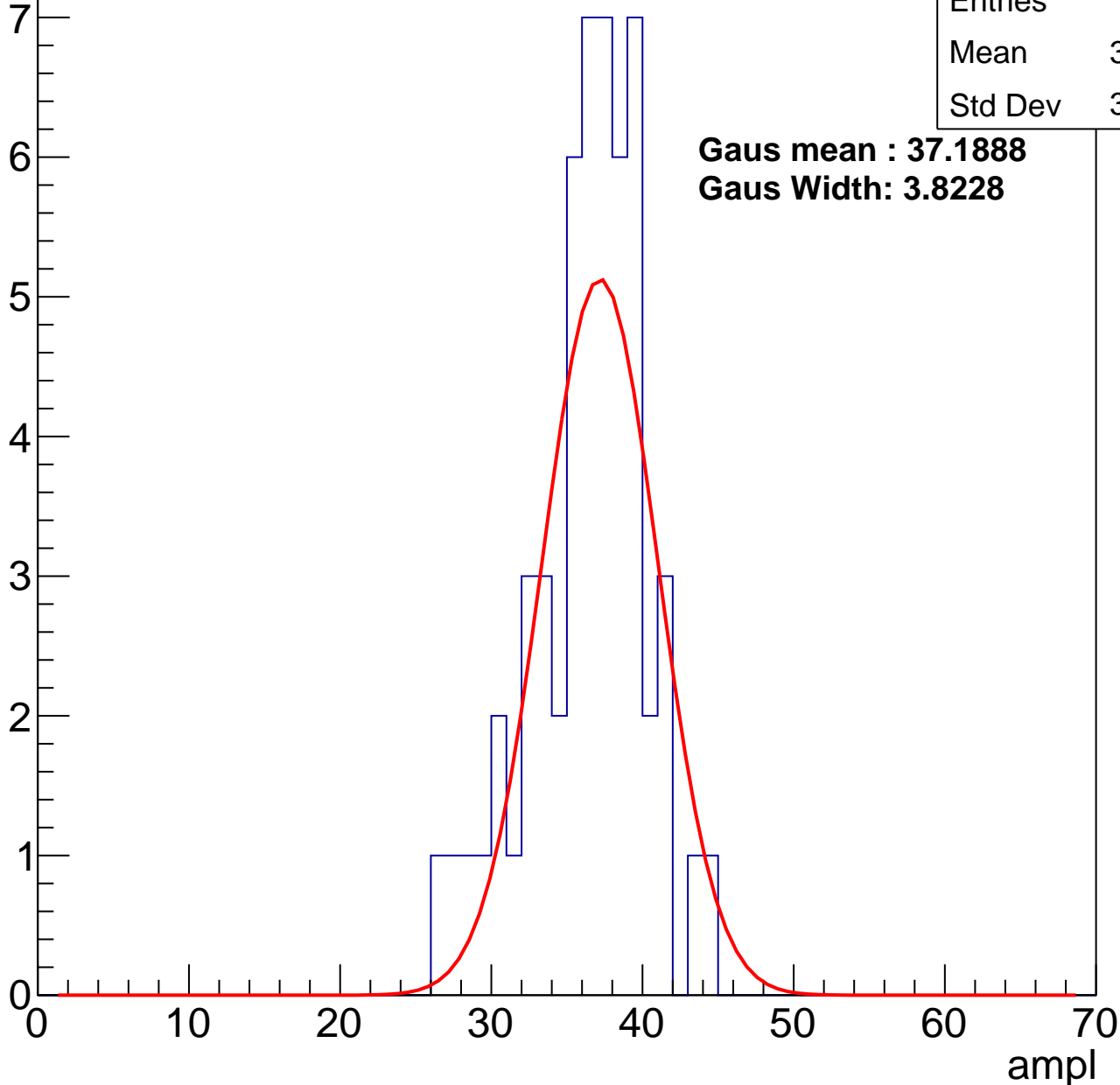
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	35.93
Std Dev	3.799

**Gaus mean : 37.1888**

**Gaus Width: 3.8228**



# B1L102S, U8-ch86, adc2

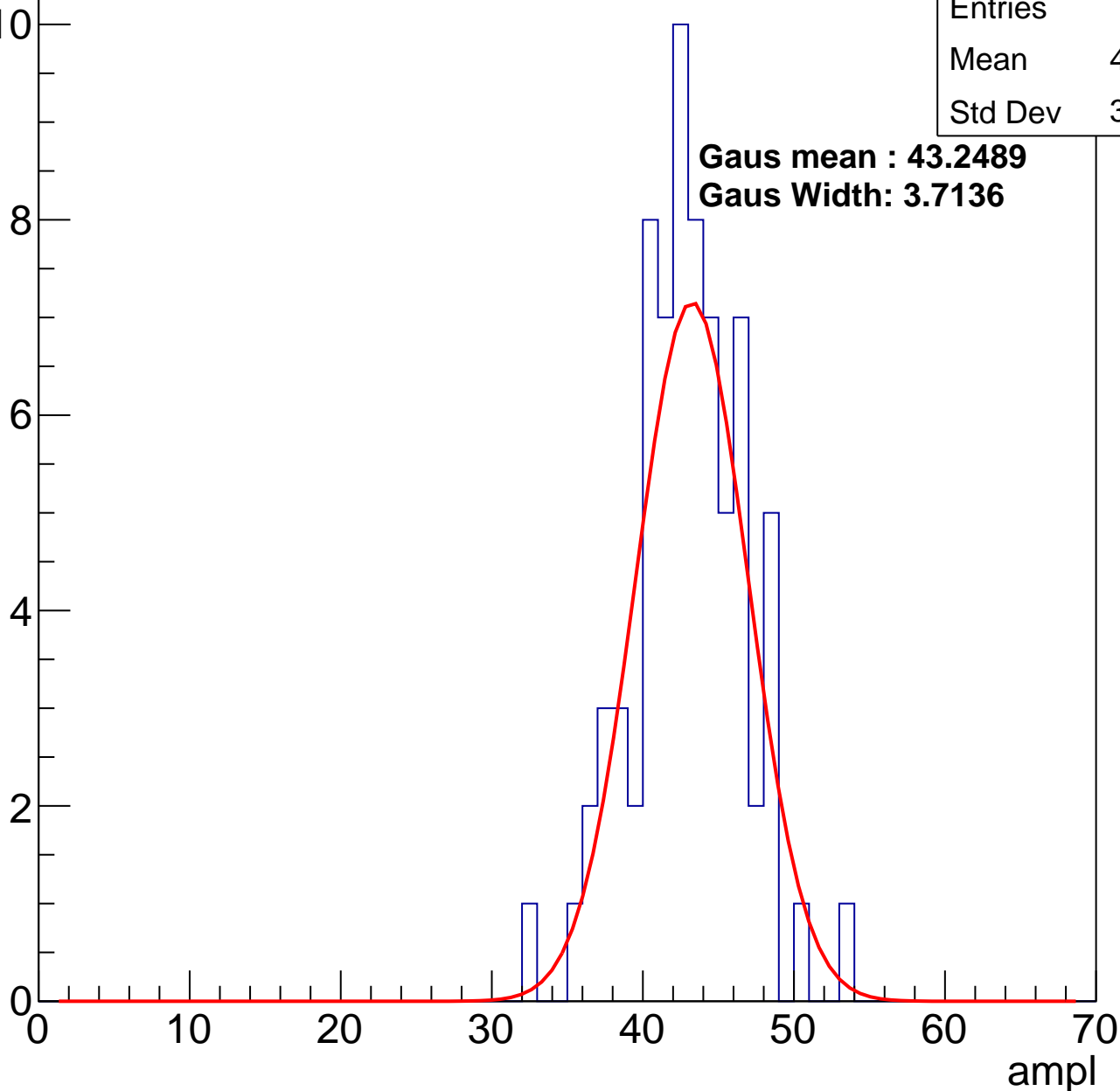
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	42.53
Std Dev	3.679

**Gaus mean : 43.2489**

**Gaus Width: 3.7136**

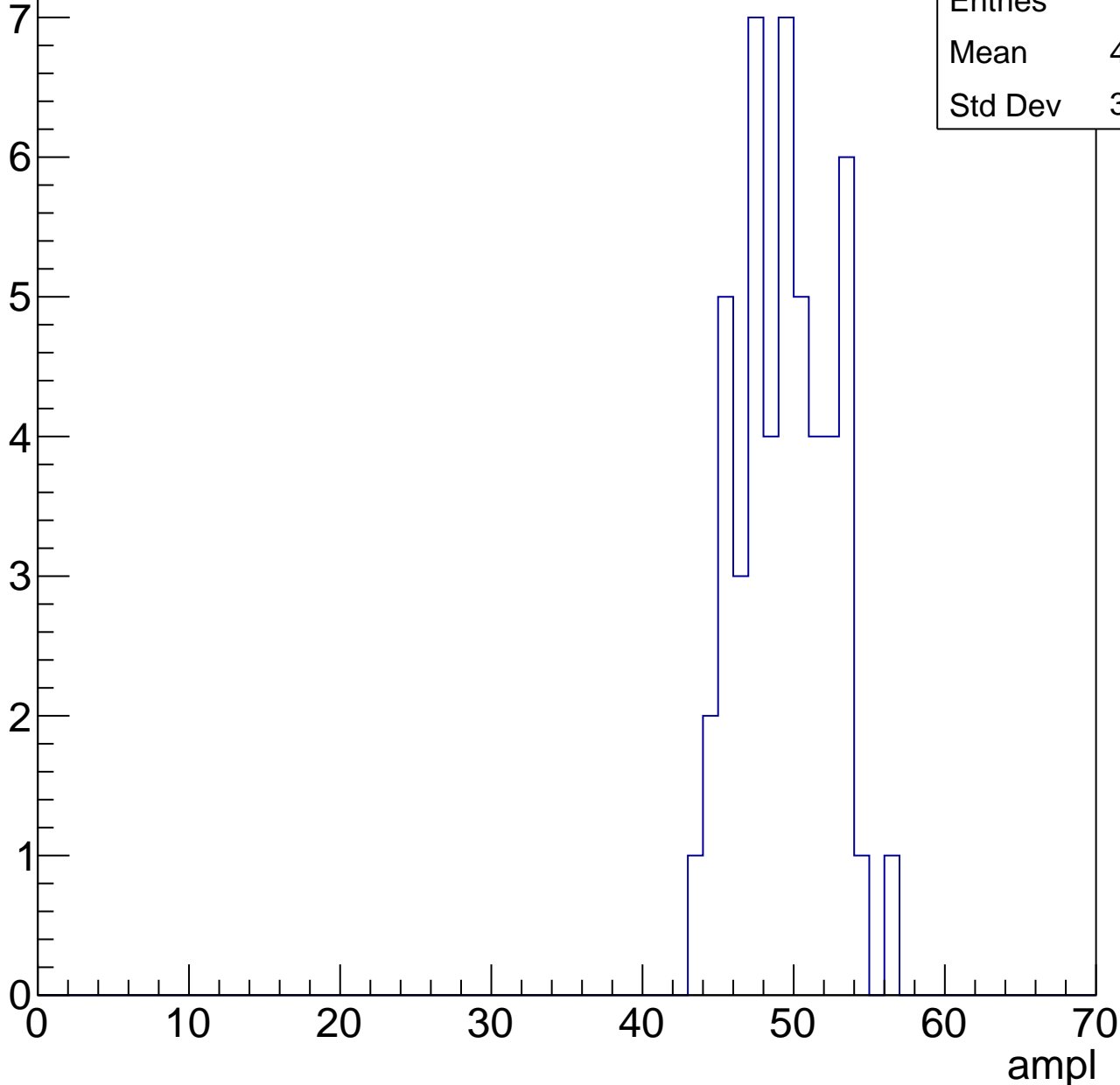


# B1L102S, U8-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

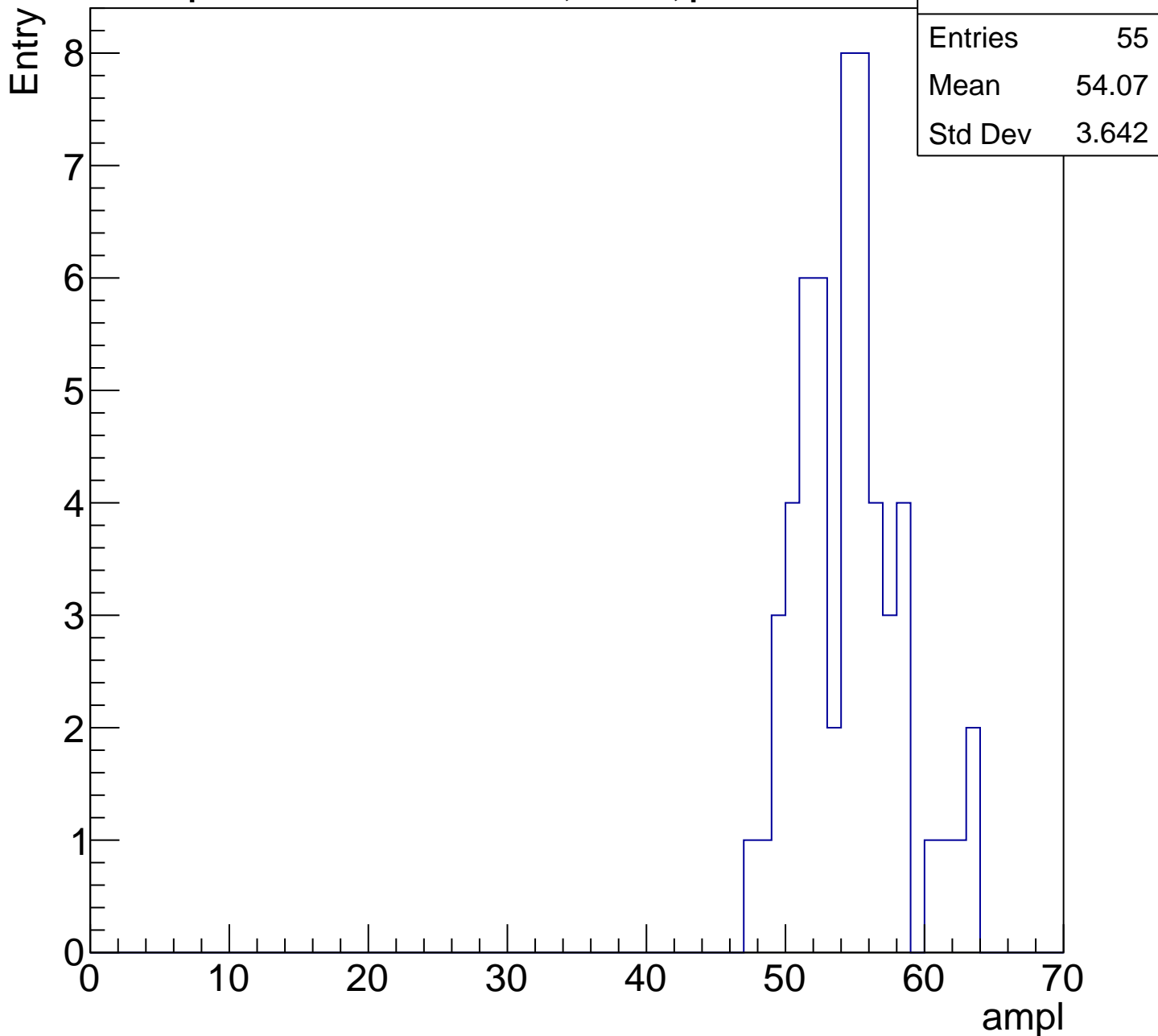
Entry

Entries	50
Mean	48.96
Std Dev	3.006



# B1L102S, U8-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

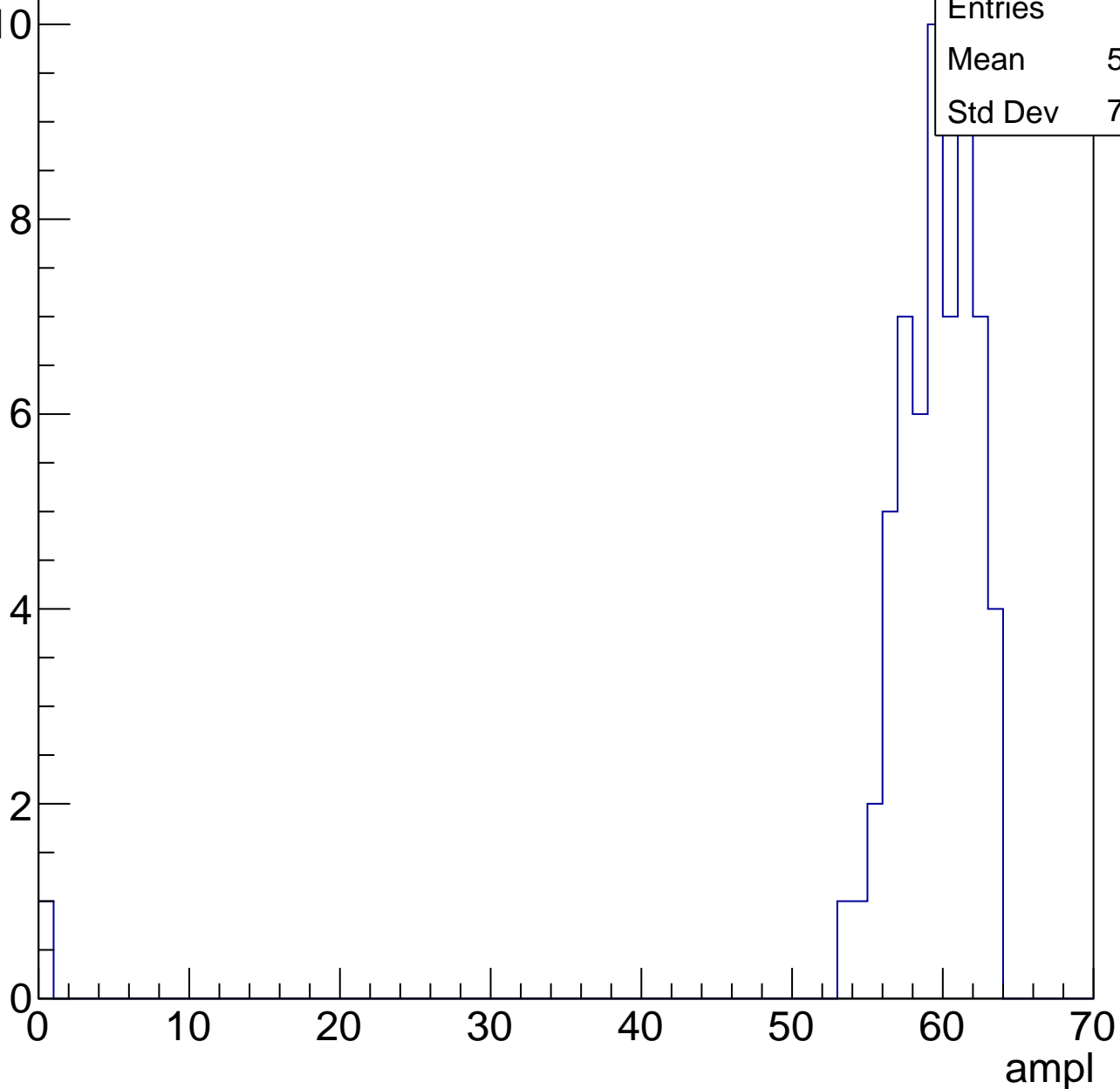


# B1L102S, U8-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

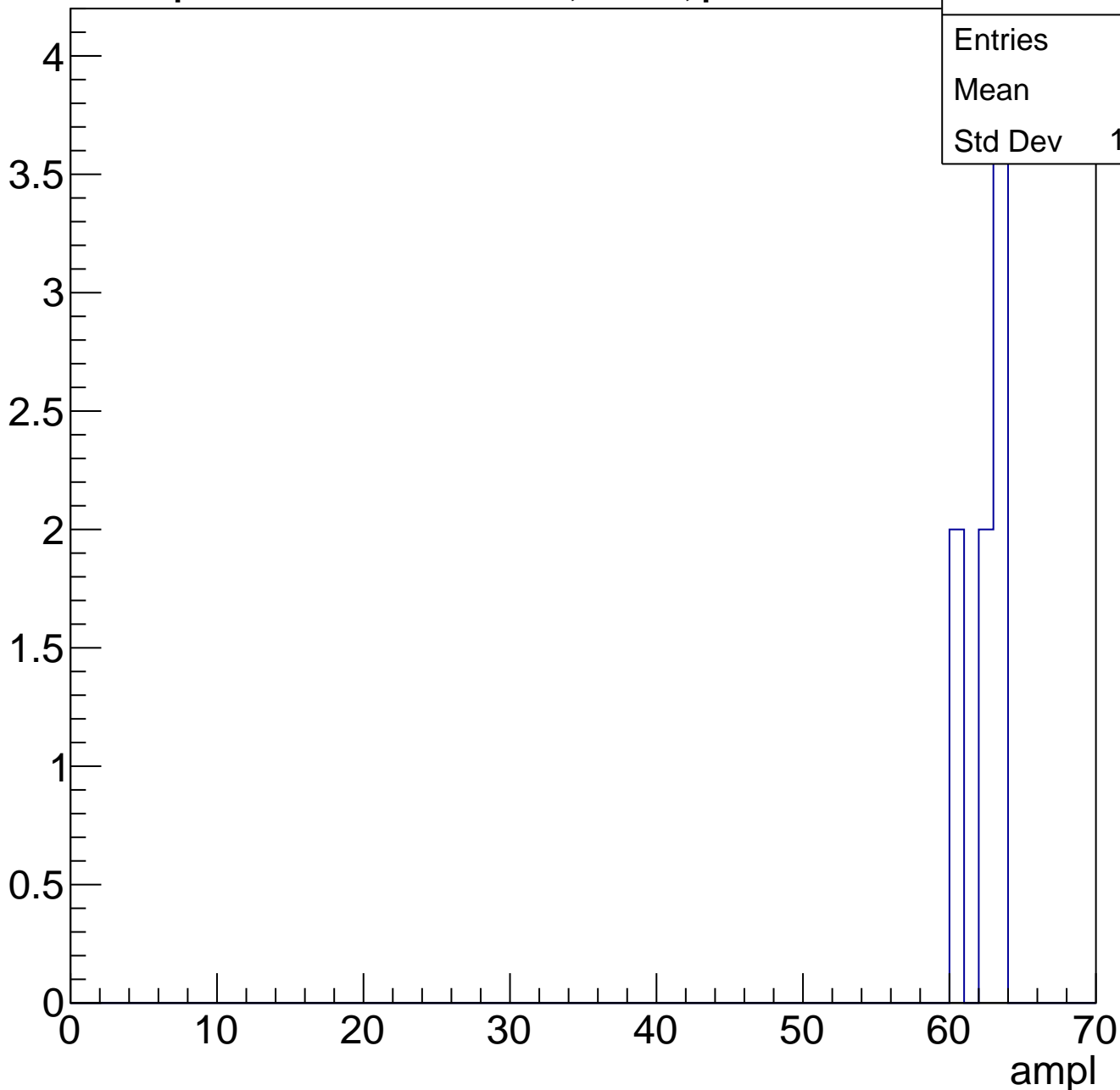
Entries	60
Mean	58.15
Std Dev	7.937



# B1L102S, U8-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch87, adc0

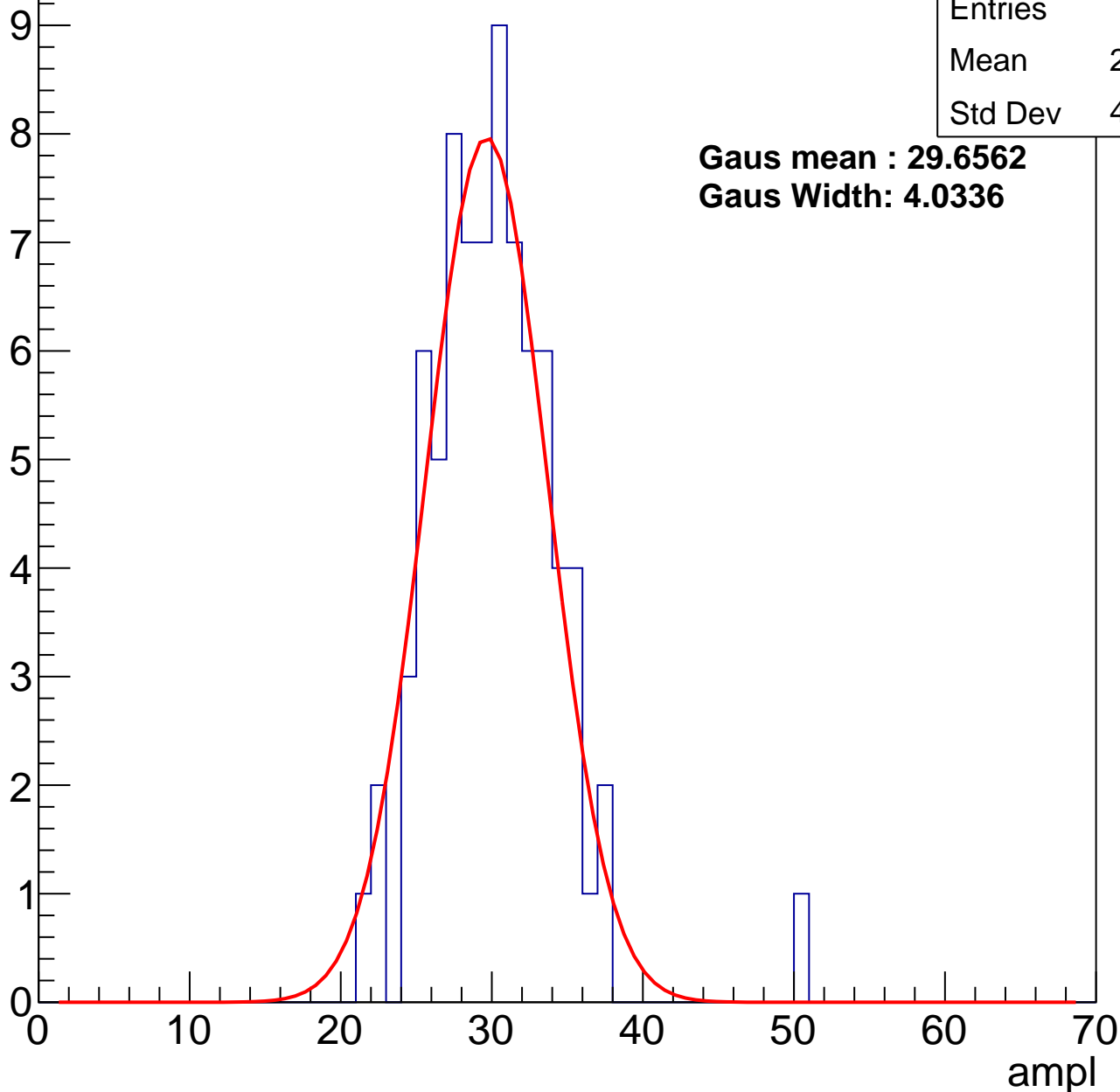
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	29.68
Std Dev	4.253

**Gaus mean : 29.6562**

**Gaus Width: 4.0336**



# B1L102S, U8-ch87, adc1

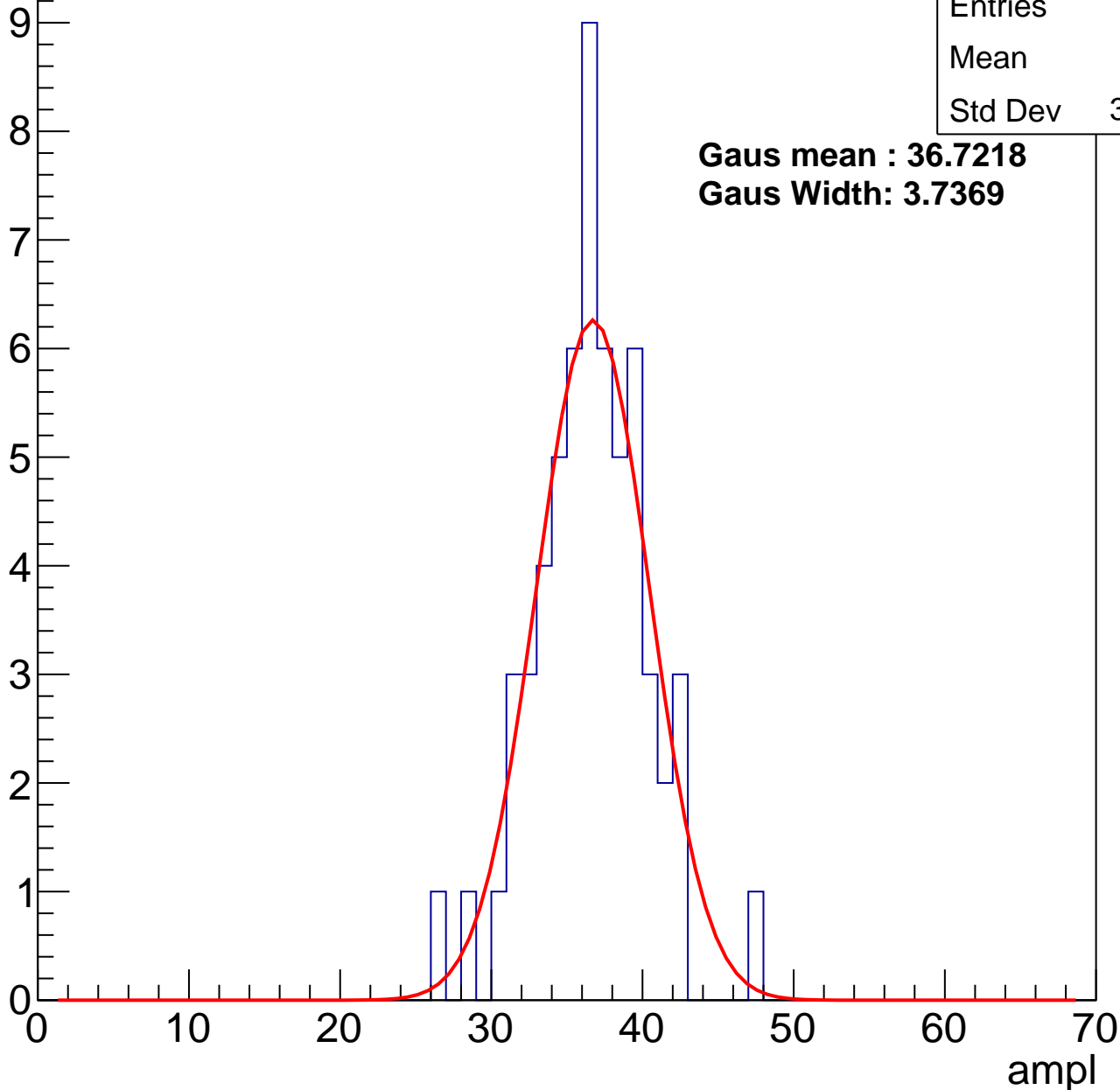
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	36.1
Std Dev	3.662

**Gaus mean : 36.7218**

**Gaus Width: 3.7369**



# B1L102S, U8-ch87, adc2

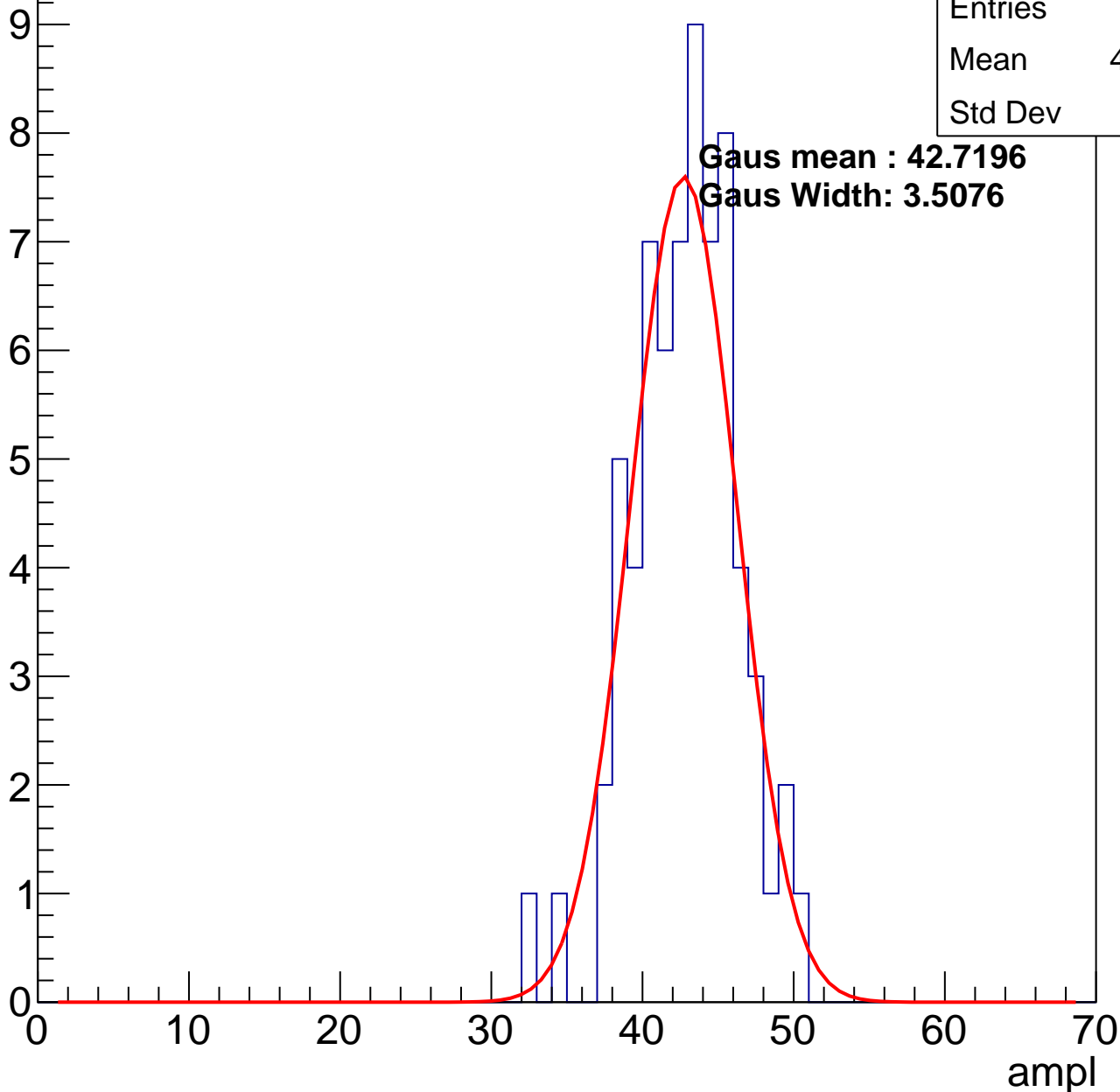
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	42.38
Std Dev	3.43

**Gaus mean : 42.7196**

**Gaus Width: 3.5076**

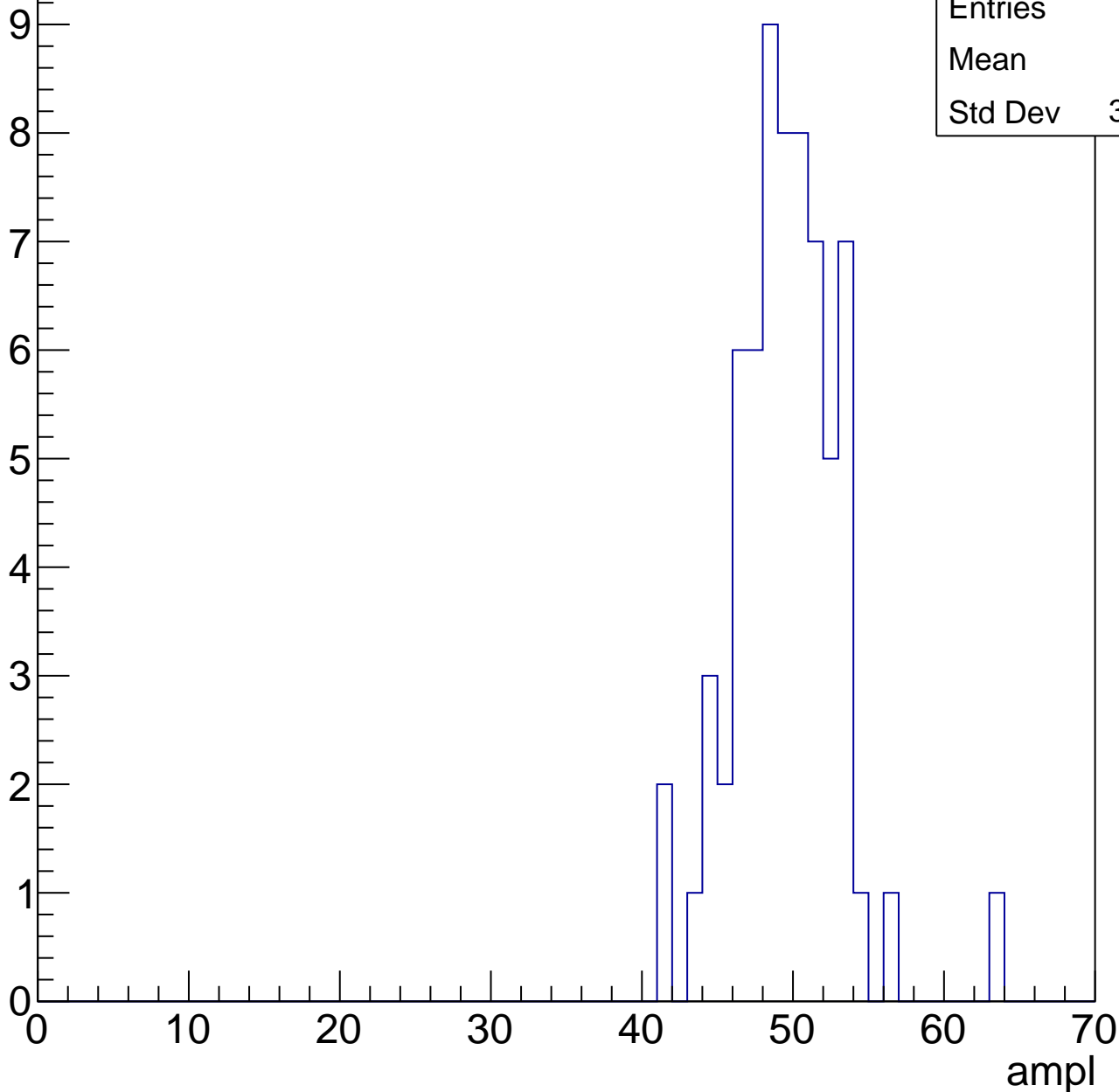


# B1L102S, U8-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	49.1
Std Dev	3.499

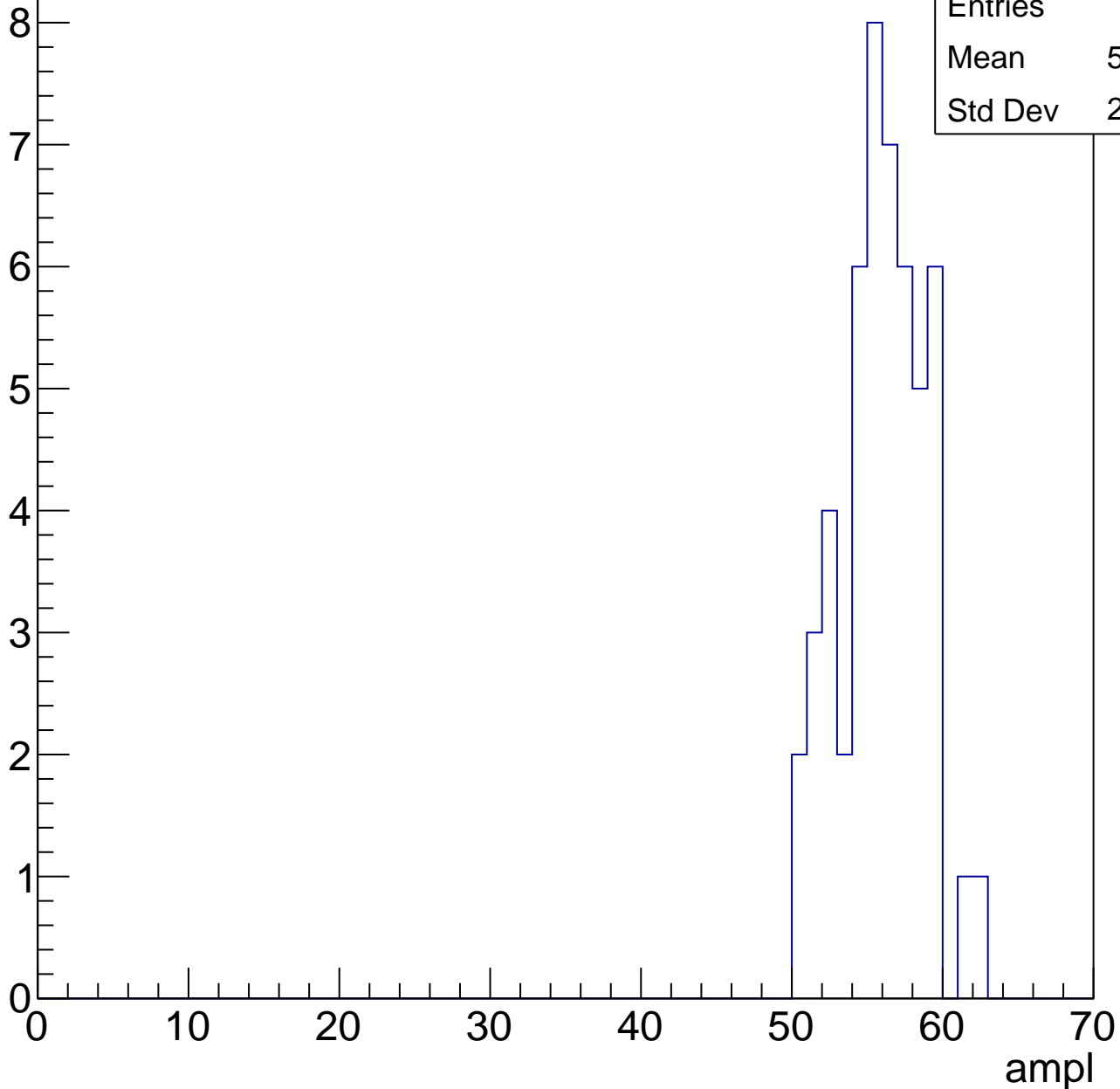


# B1L102S, U8-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	55.53
Std Dev	2.768

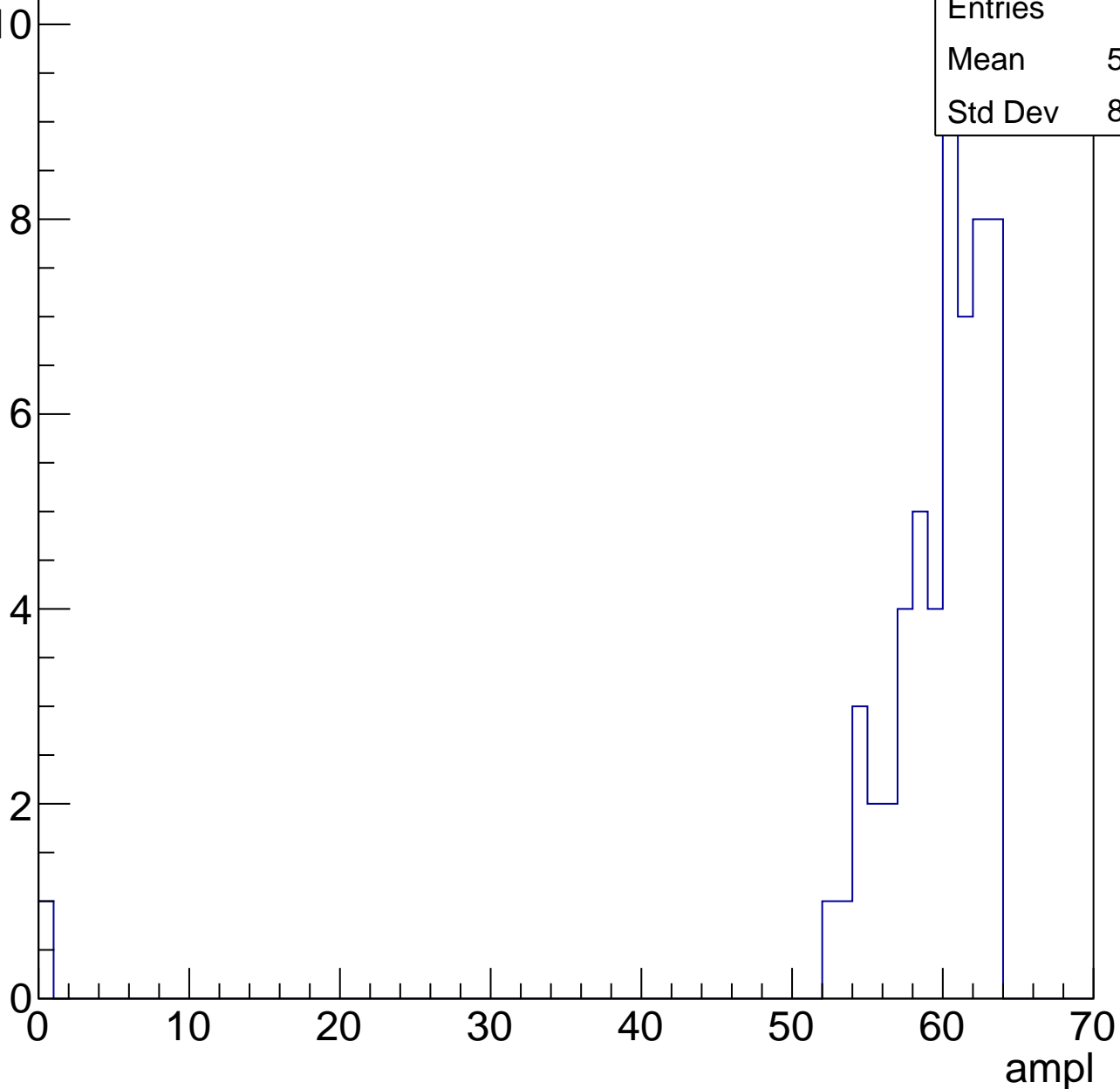


# B1L102S, U8-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	58.39
Std Dev	8.377



# B1L102S, U8-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch88, adc0

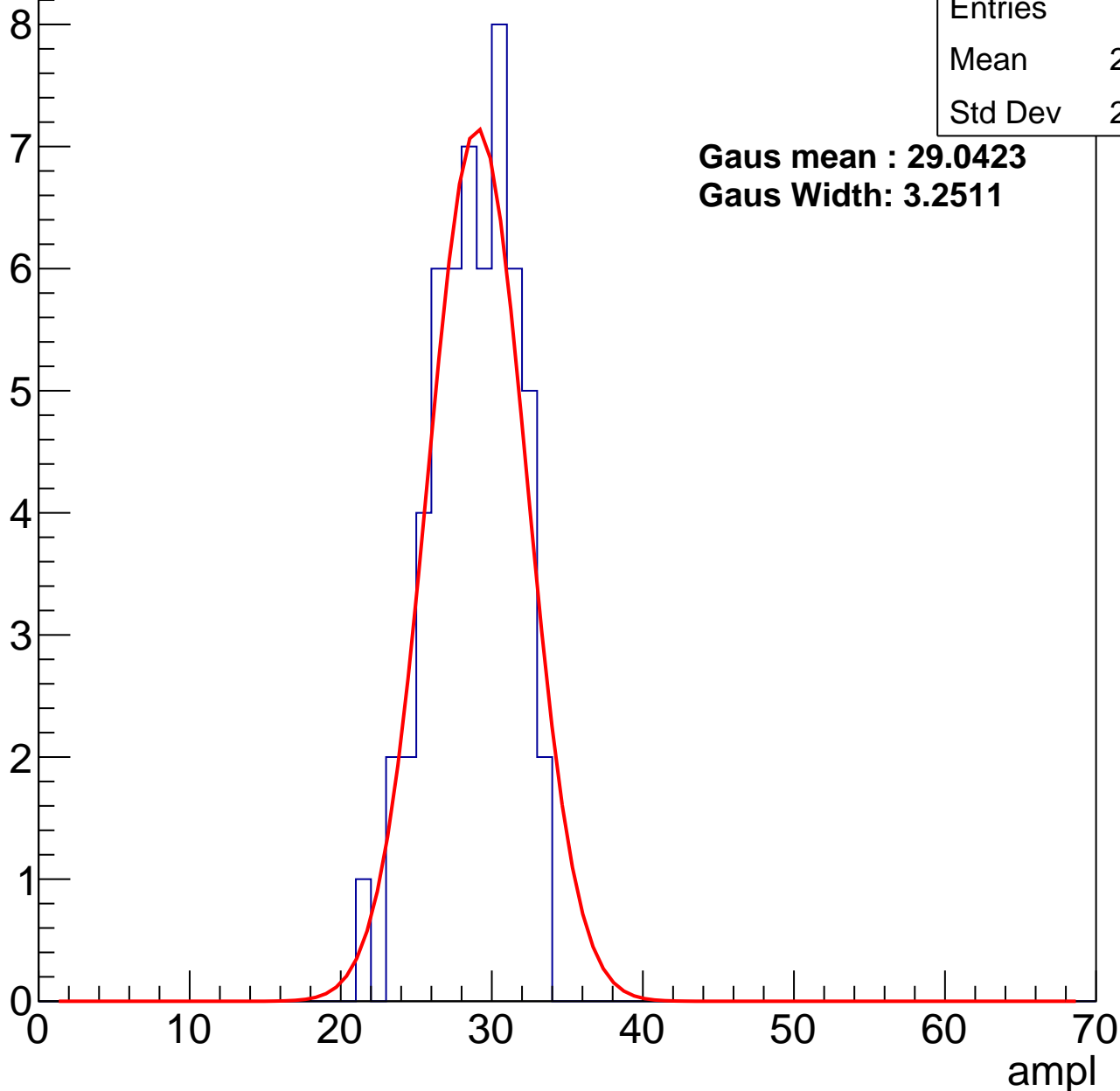
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	28.27
Std Dev	2.747

**Gaus mean : 29.0423**

**Gaus Width: 3.2511**



# B1L102S, U8-ch88, adc1

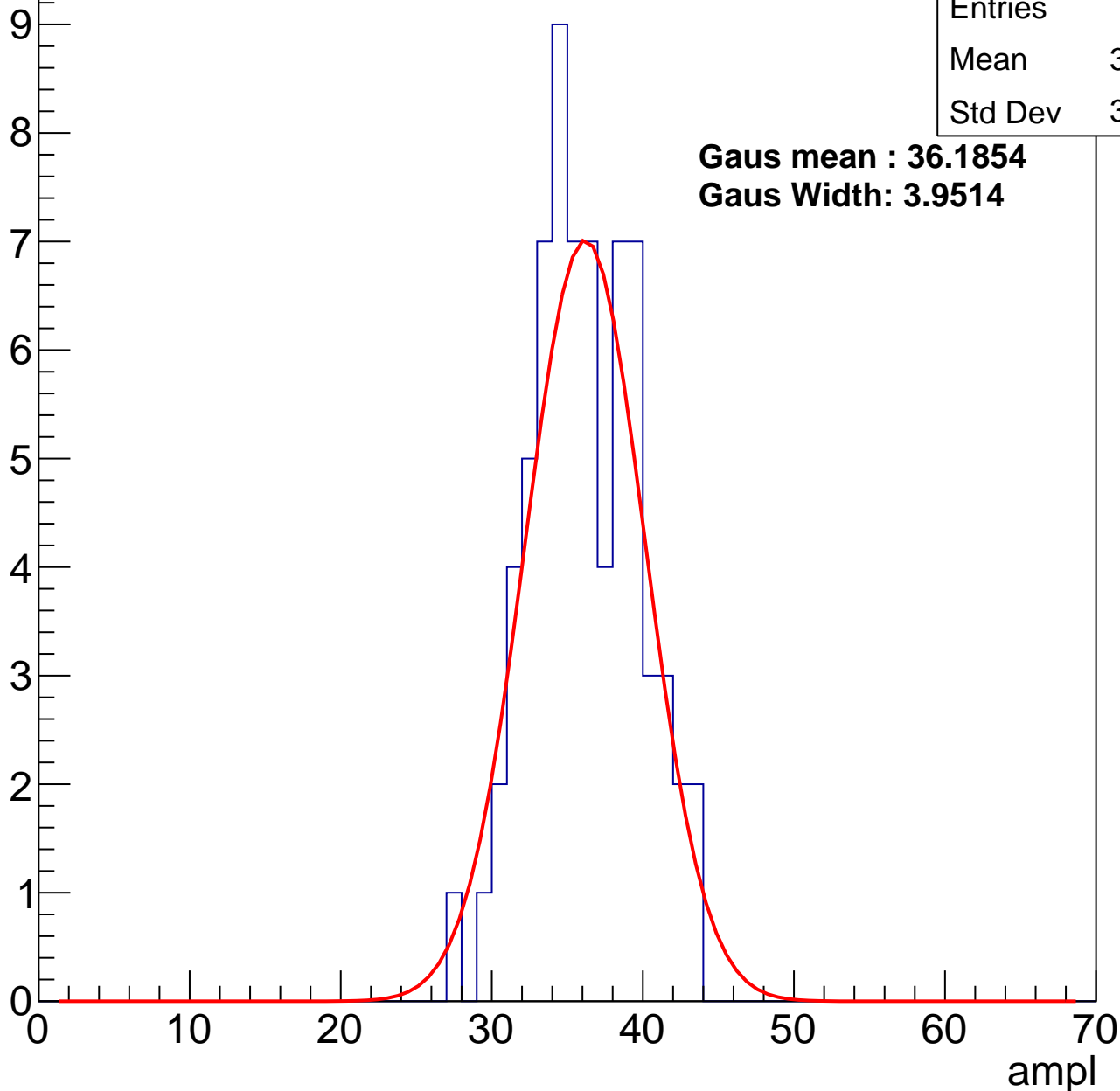
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	35.69
Std Dev	3.499

**Gaus mean : 36.1854**

**Gaus Width: 3.9514**



# B1L102S, U8-ch88, adc2

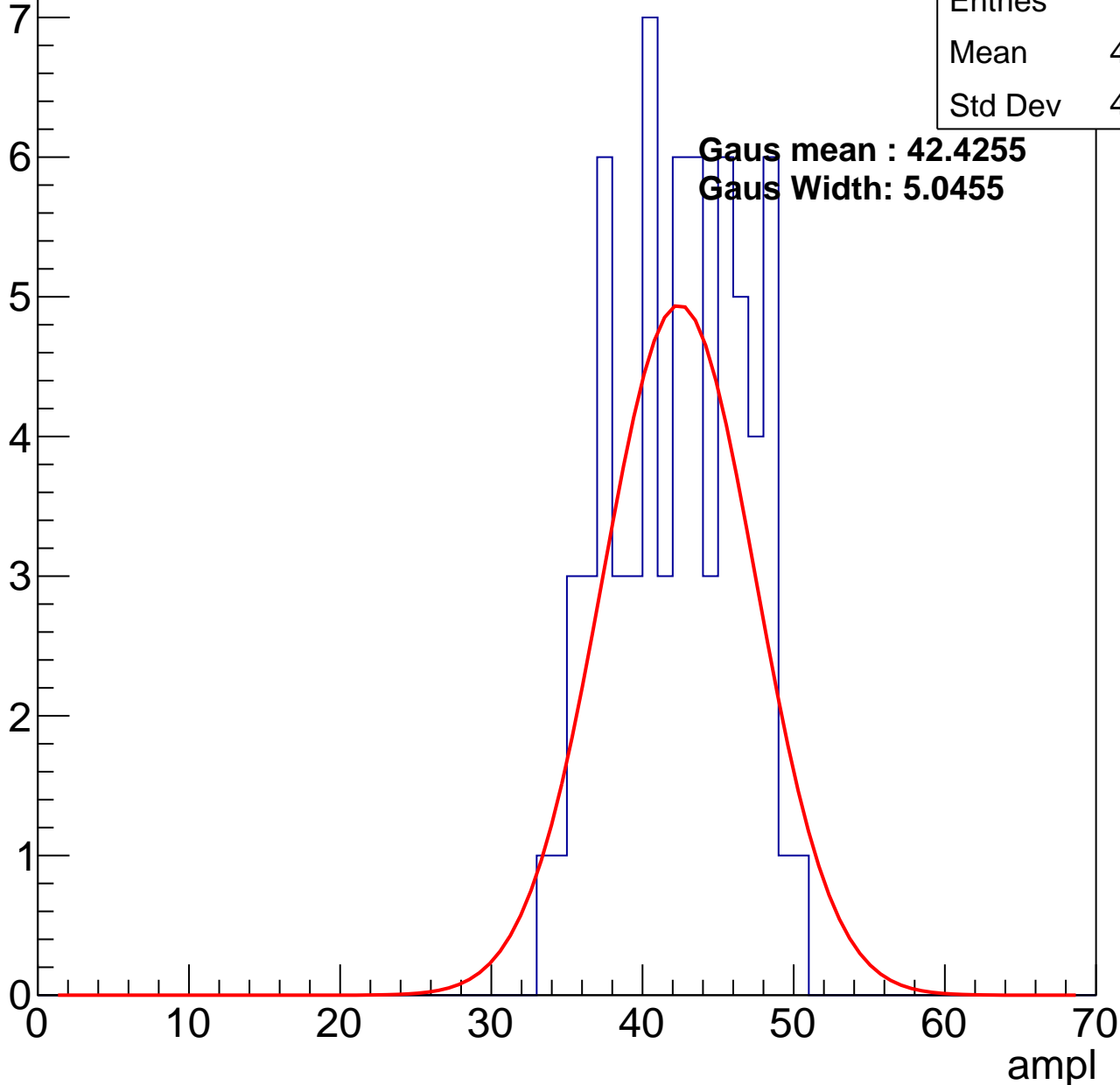
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	41.96
Std Dev	4.265

Gaus mean : 42.4255

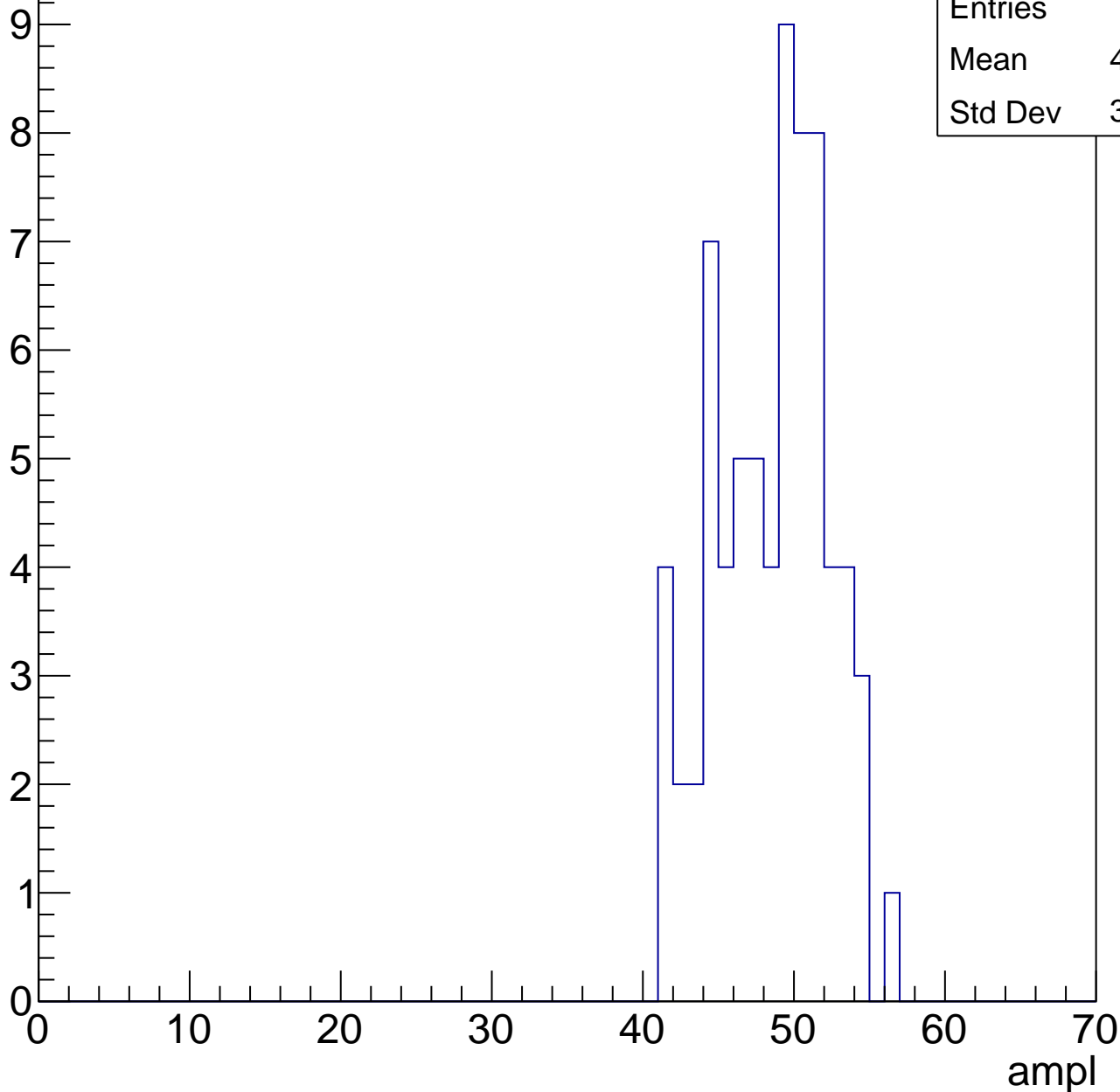
Gaus Width: 5.0455



# B1L102S, U8-ch88, adc3

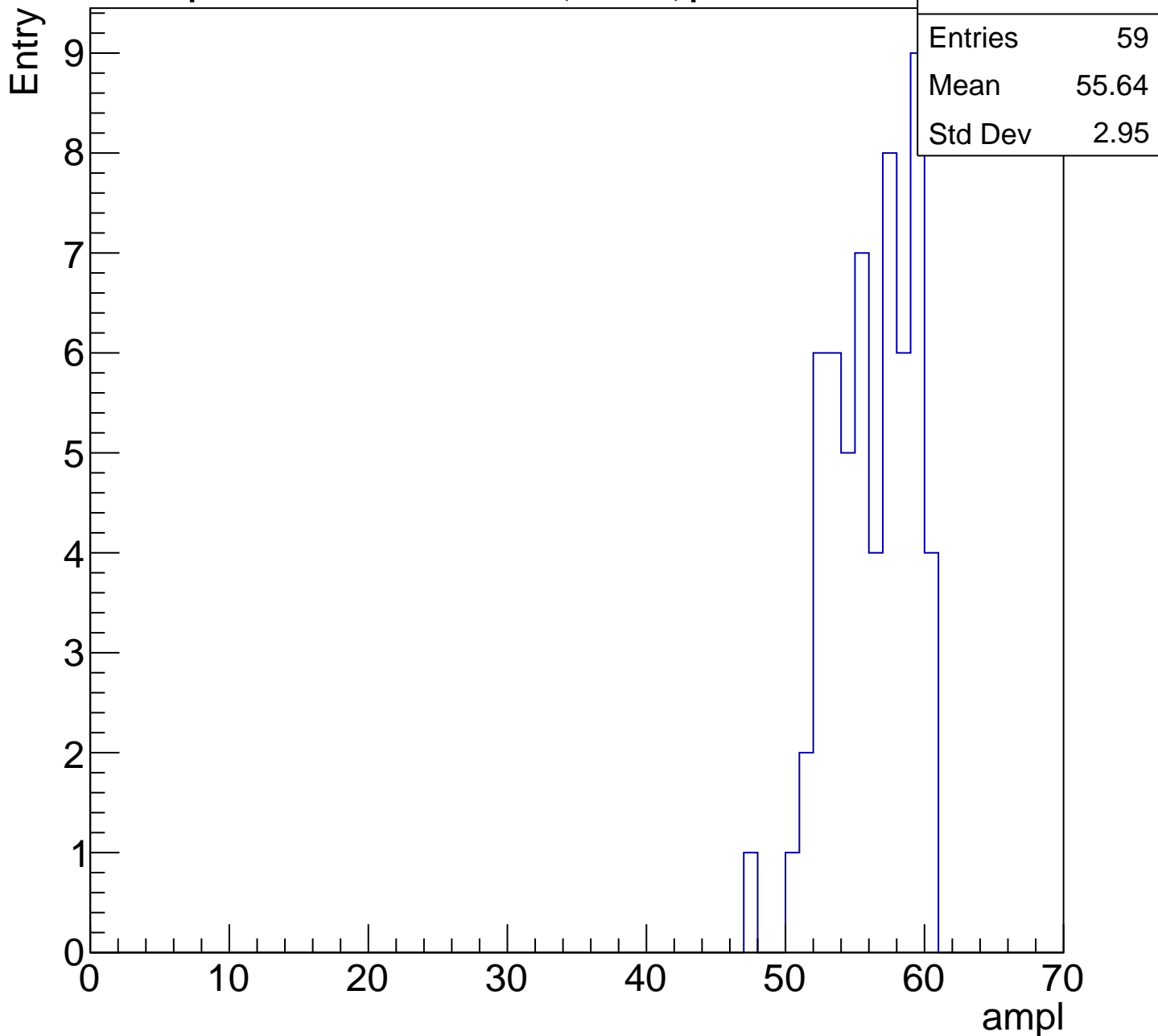
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

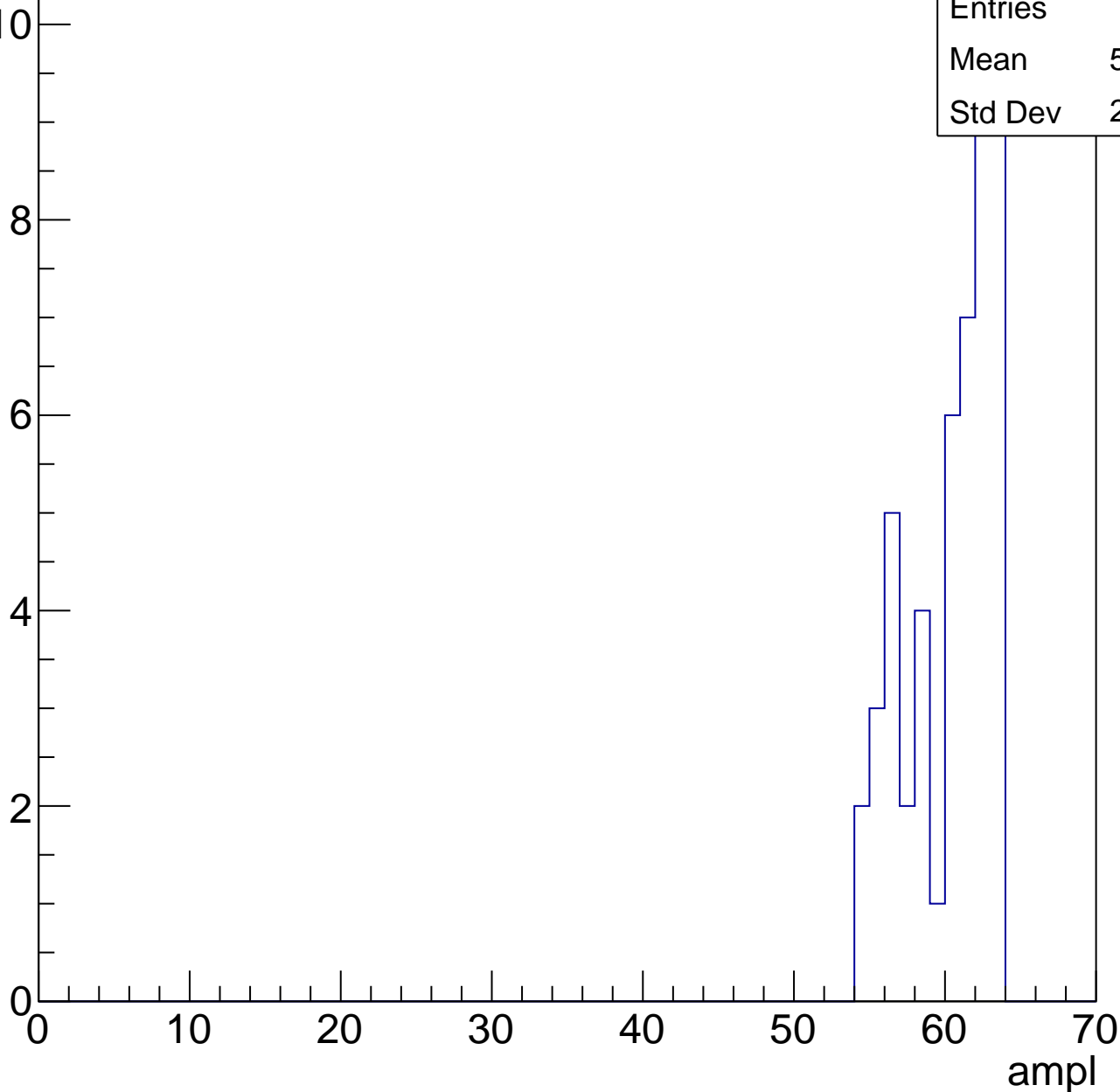


# B1L102S, U8-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

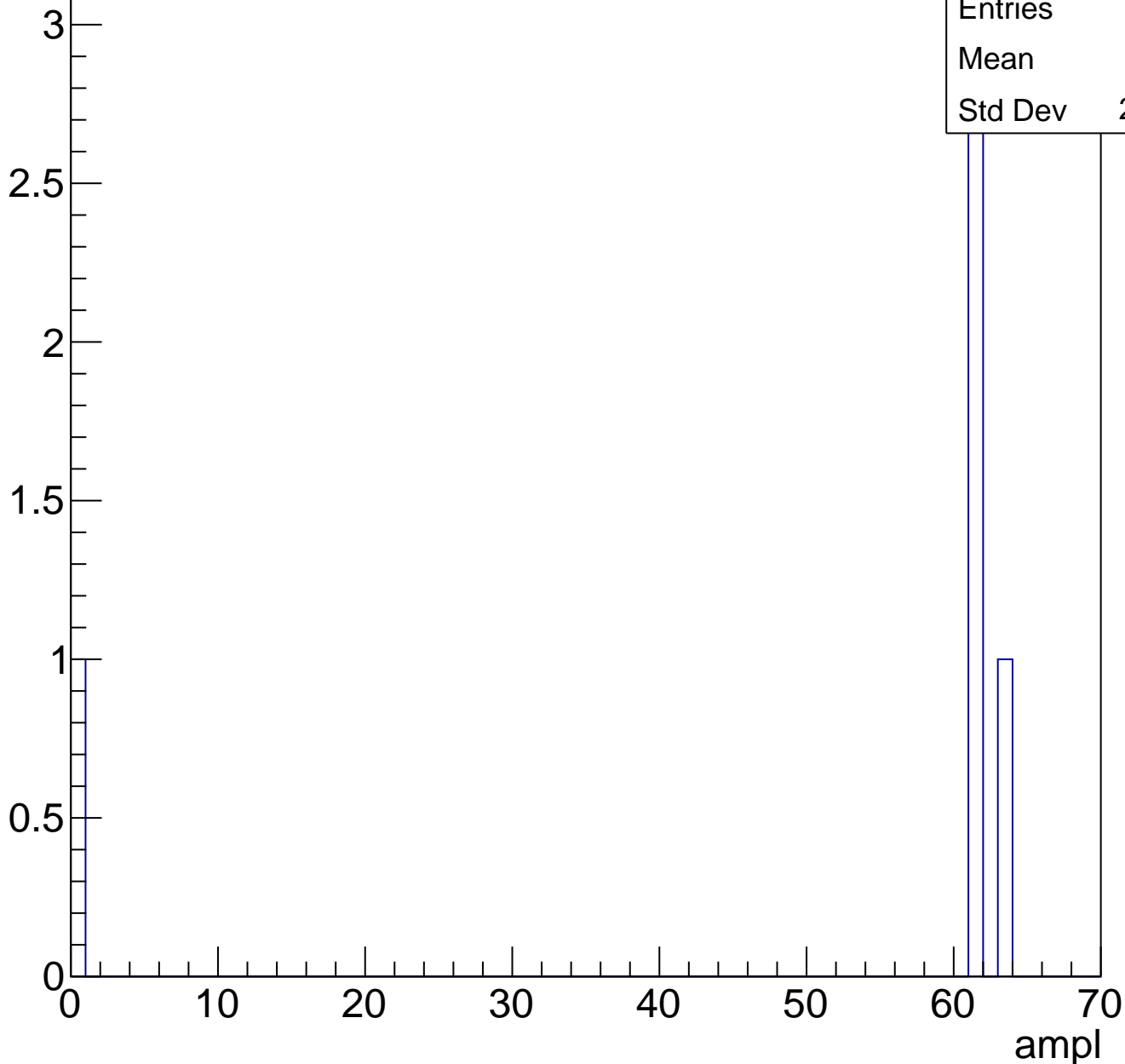
Entries	49
Mean	59.84
Std Dev	2.816



# B1L102S, U8-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

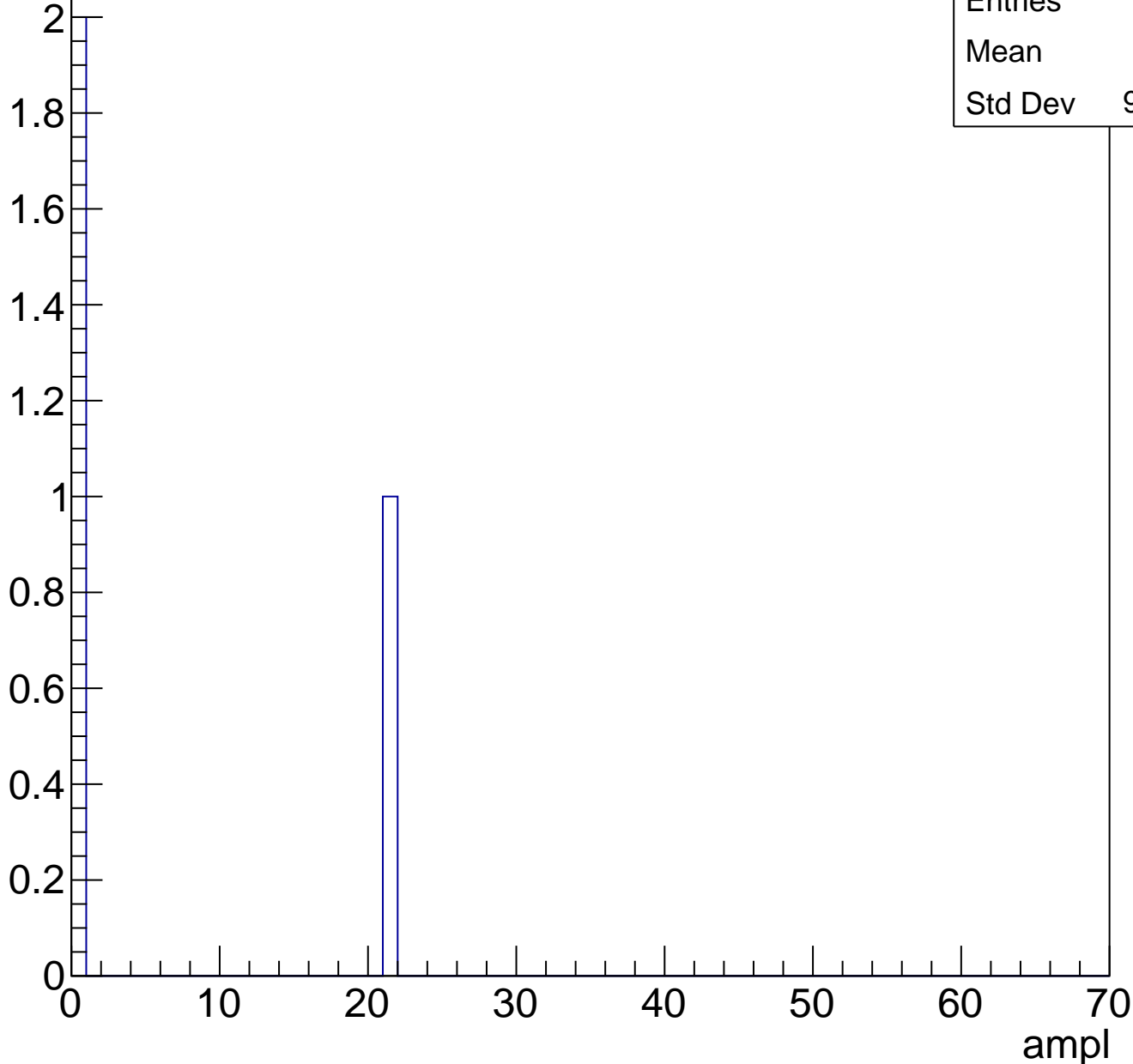




# B1L102S, U8-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	7
Std Dev	9.899

# B1L102S, U8-ch89, adc0

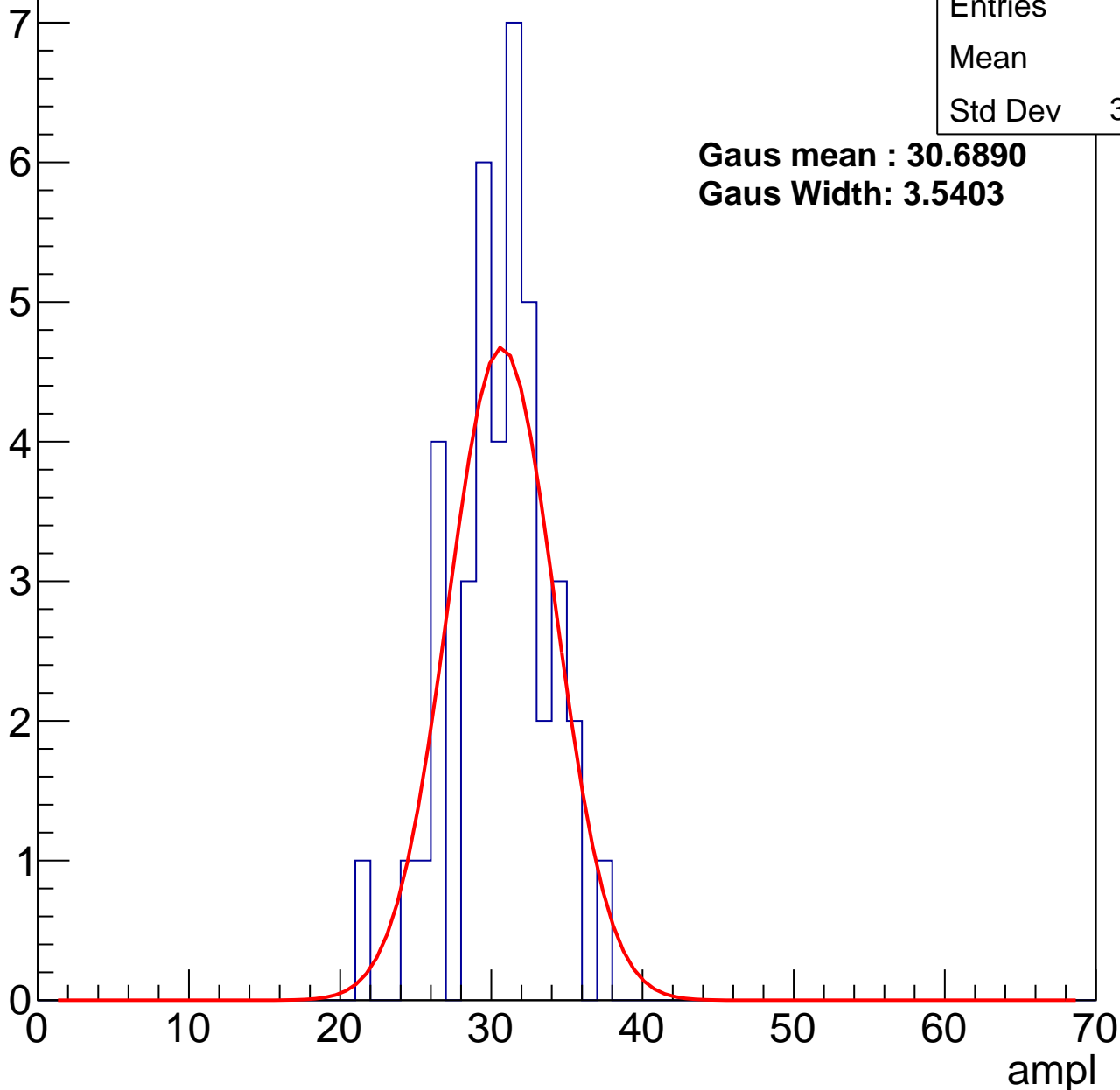
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	30.1
Std Dev	3.223

**Gaus mean : 30.6890**

**Gaus Width: 3.5403**



# B1L102S, U8-ch89, adc1

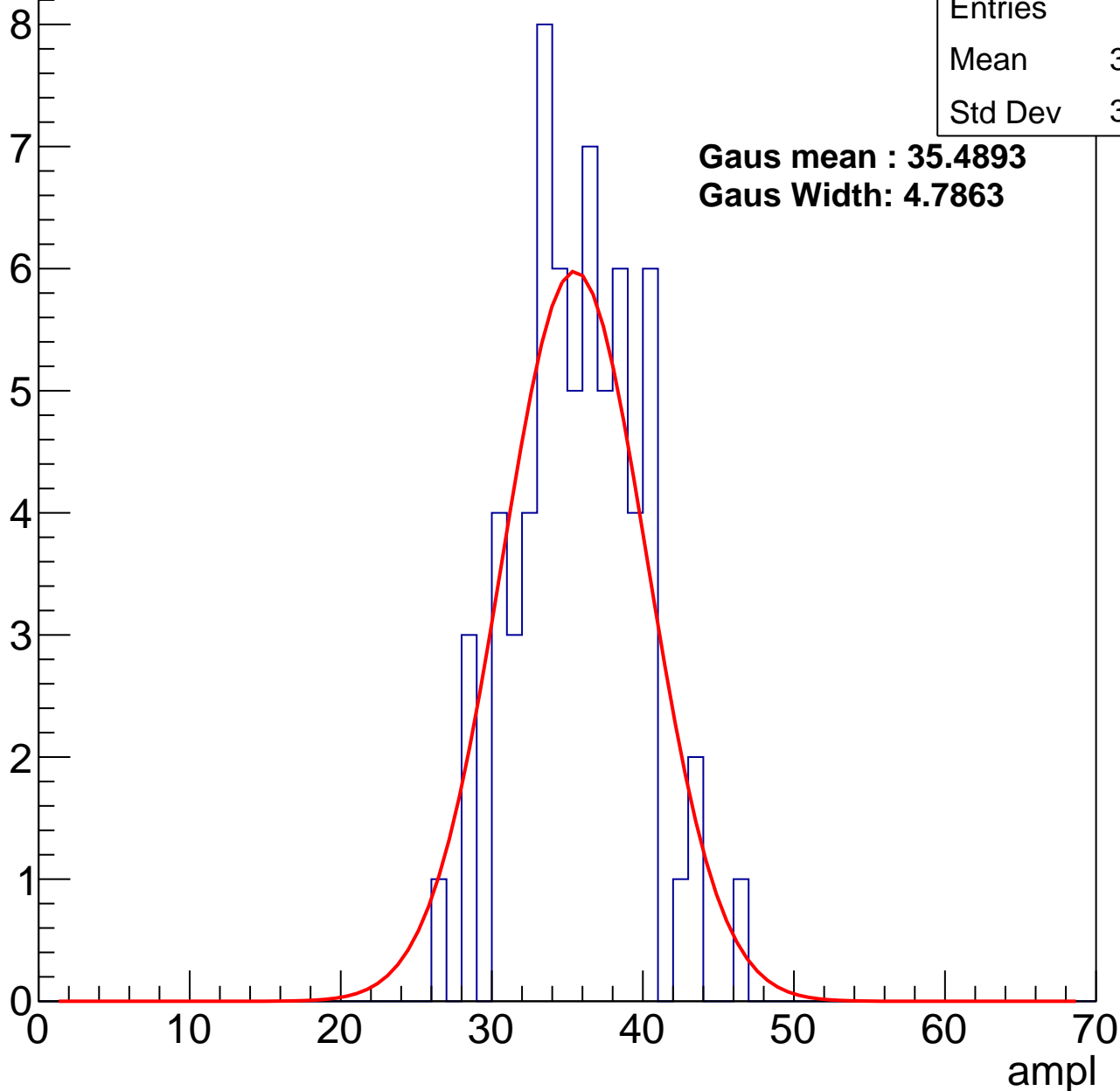
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	35.29
Std Dev	3.965

**Gaus mean : 35.4893**

**Gaus Width: 4.7863**



# B1L102S, U8-ch89, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	85
Mean	42.65
Std Dev	4.163

**Gaus mean : 43.0435**

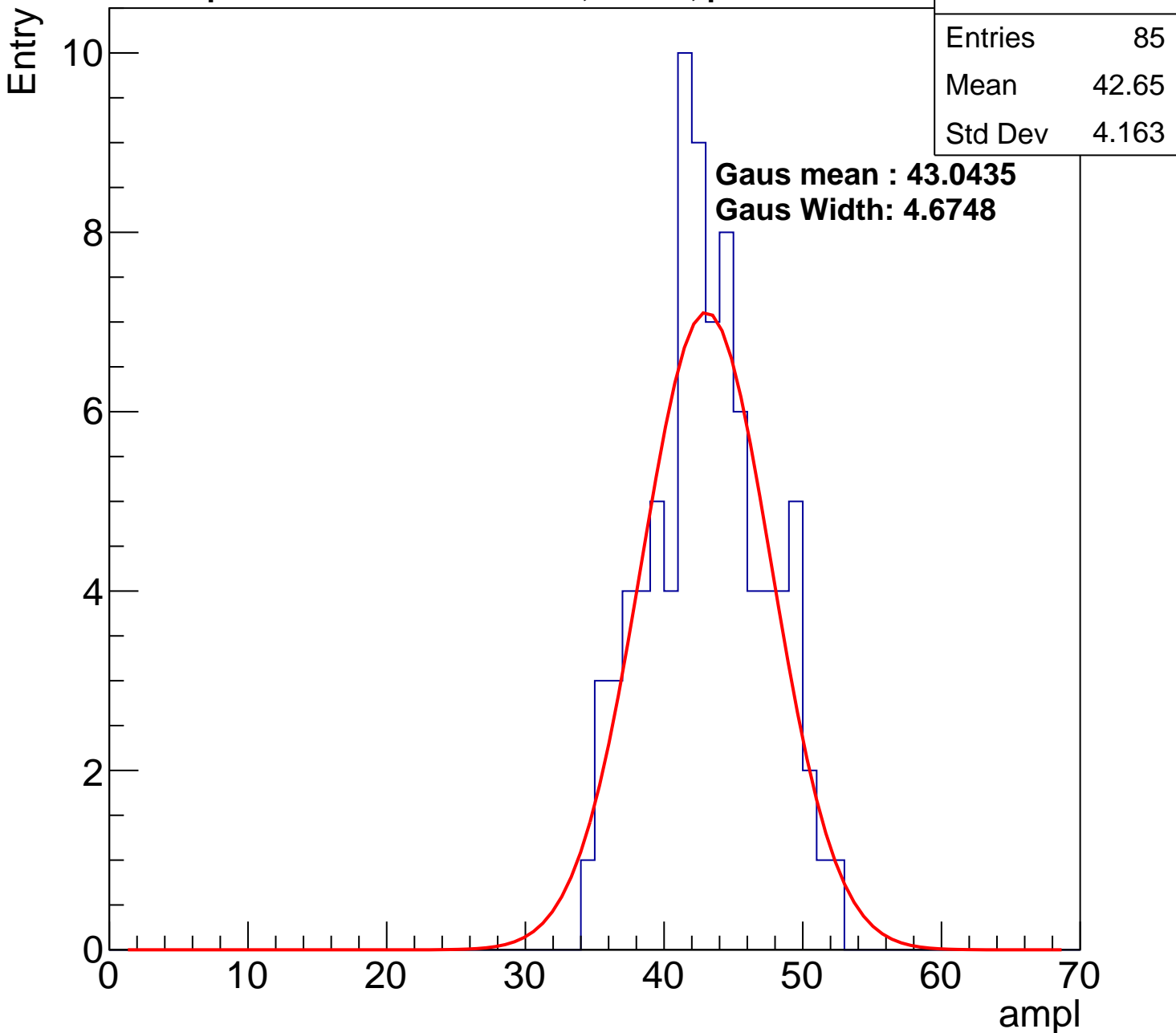
**Gaus Width: 4.6748**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

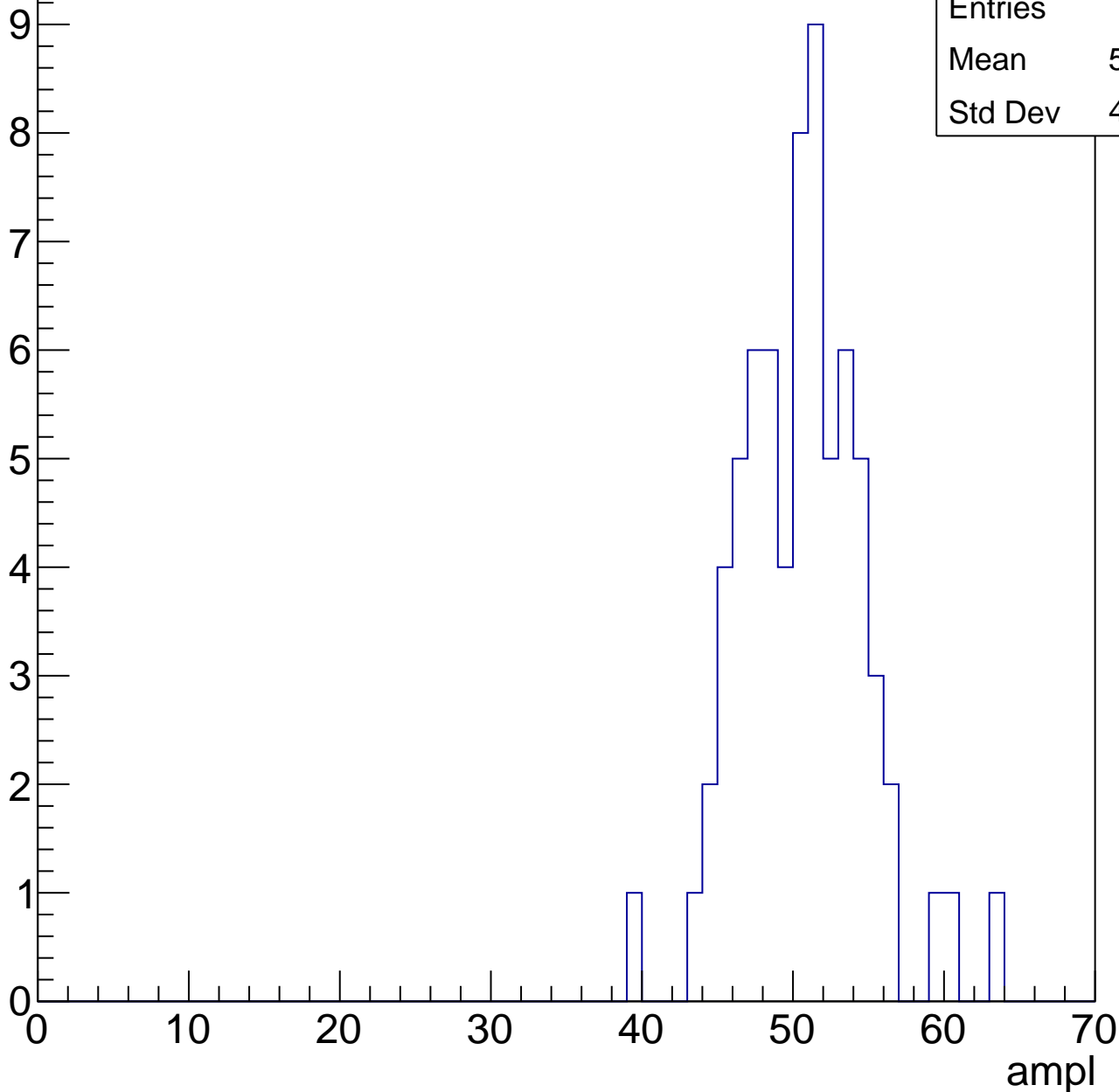


# B1L102S, U8-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	50.17
Std Dev	4.074

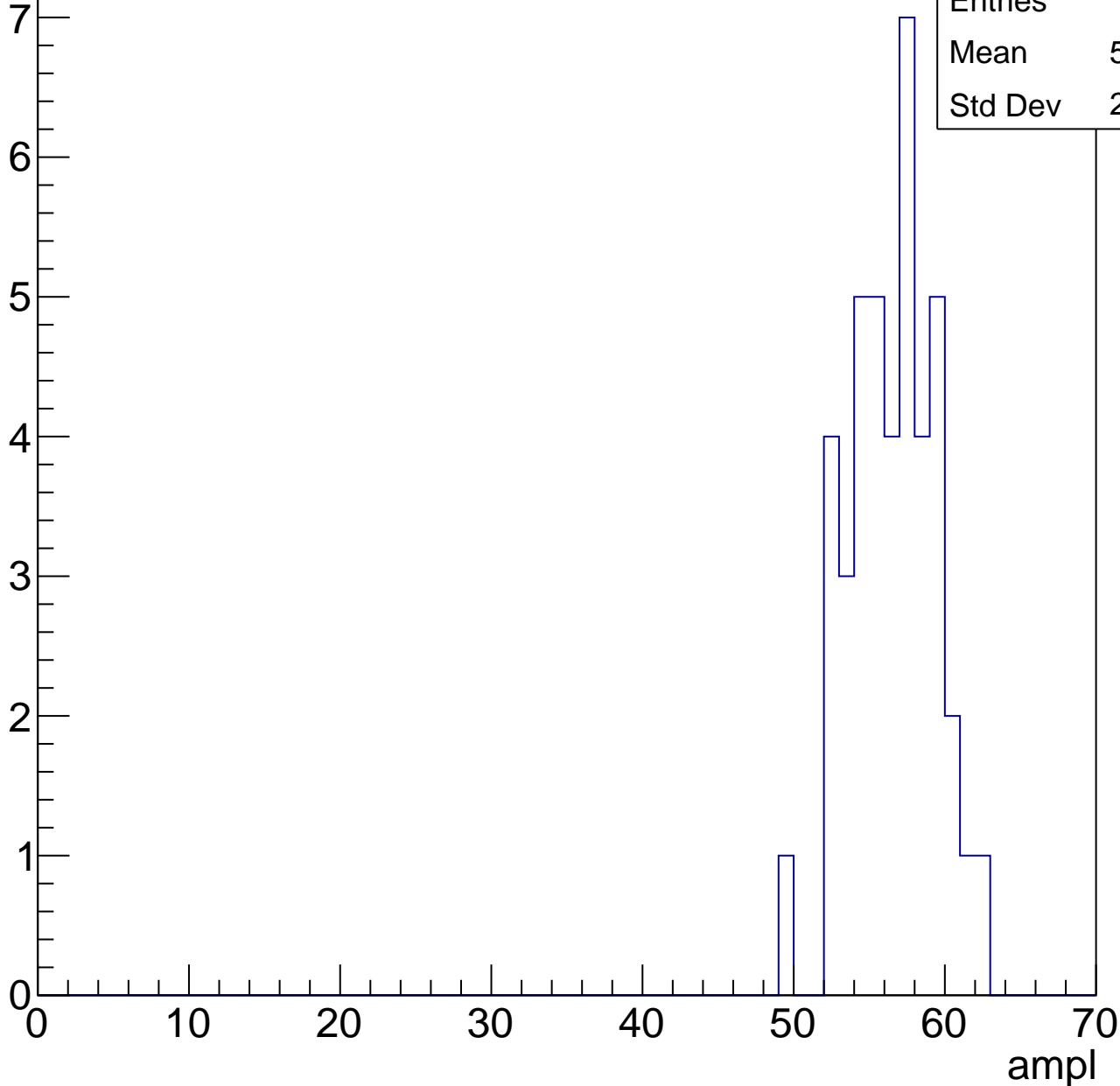


# B1L102S, U8-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

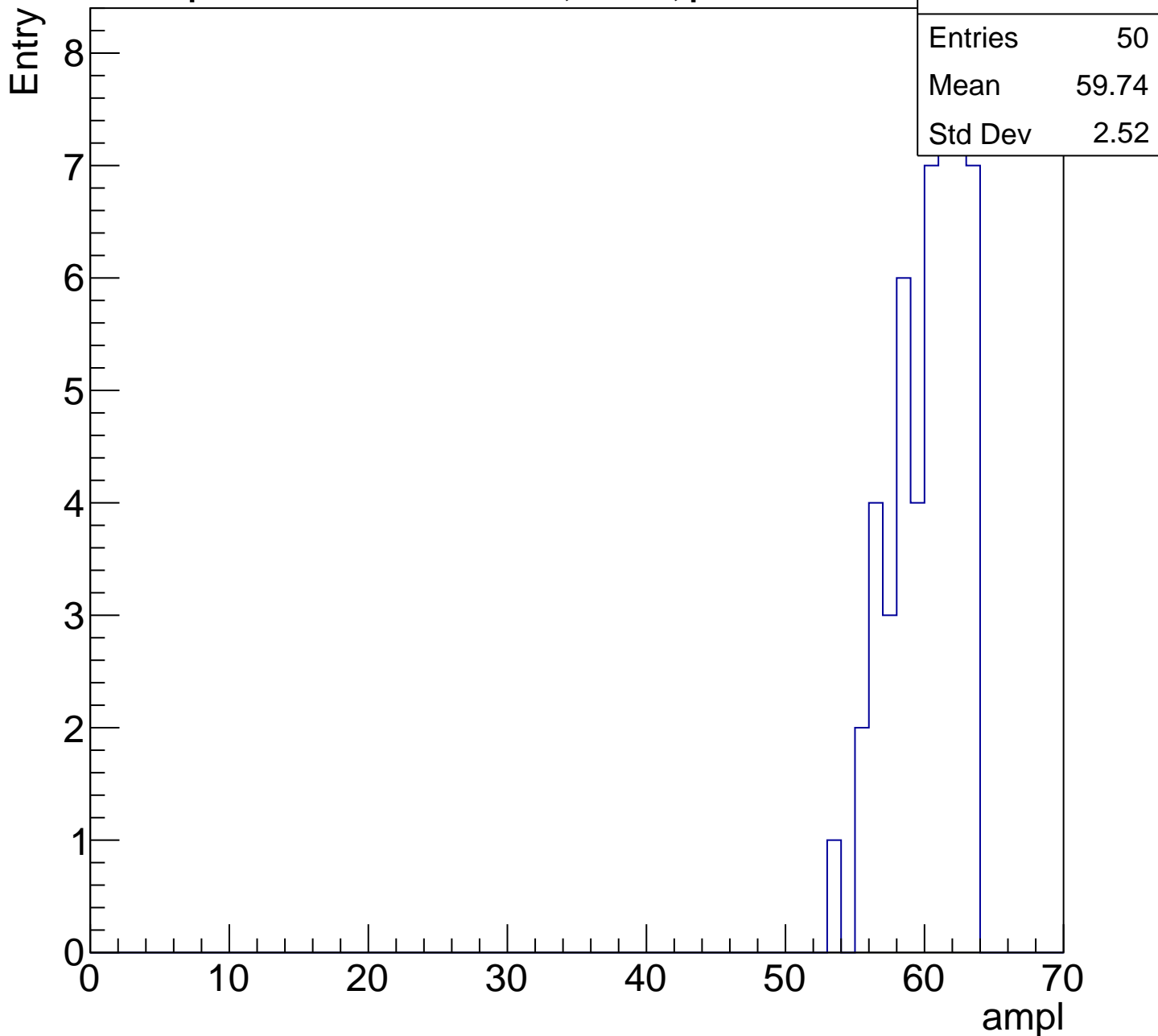
Entry

Entries	42
Mean	56.05
Std Dev	2.786



# B1L102S, U8-ch89, adc5

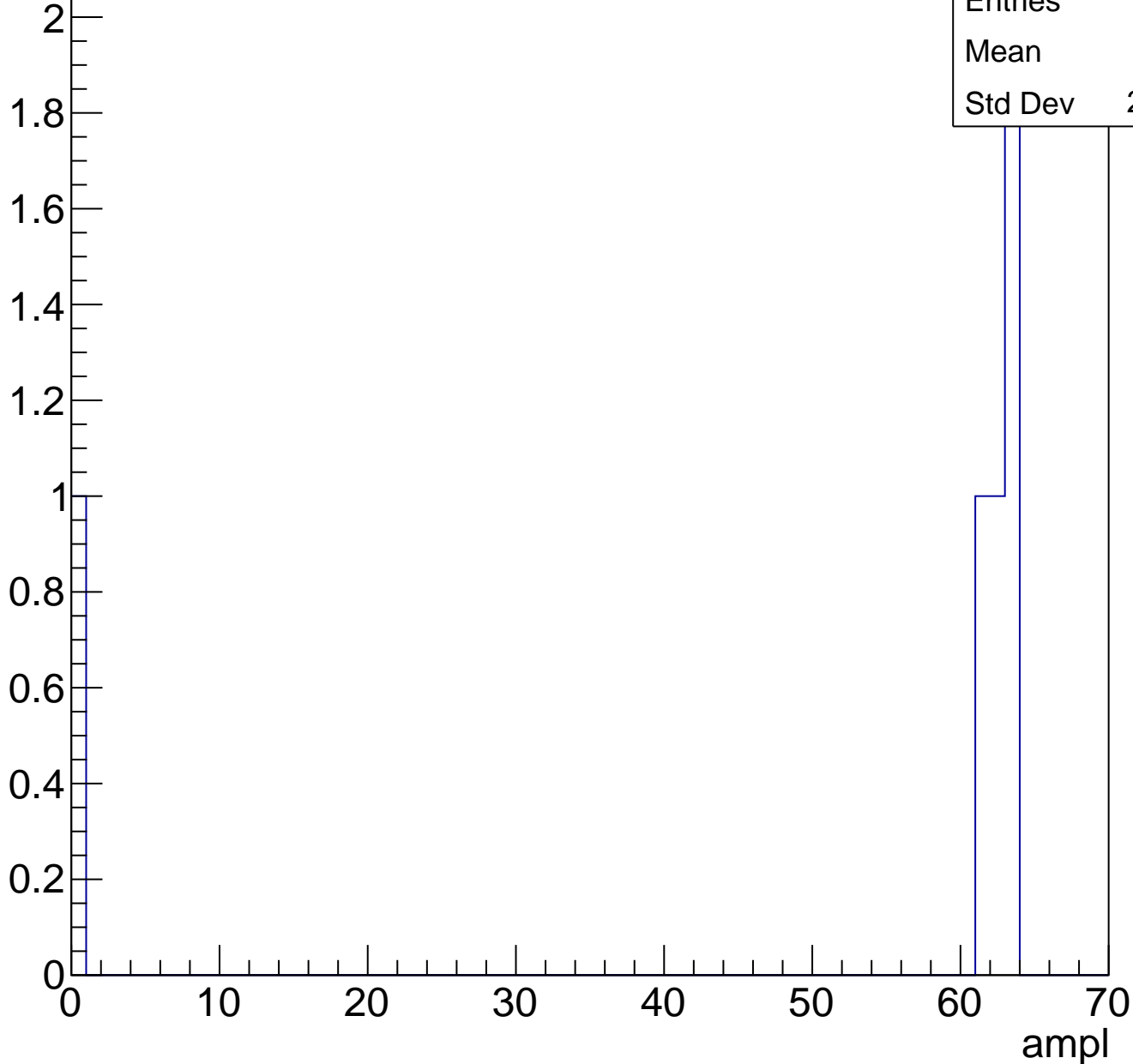
calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U8-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	5
Mean	49.8
Std Dev	24.91



# B1L102S, U8-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch90, adc0

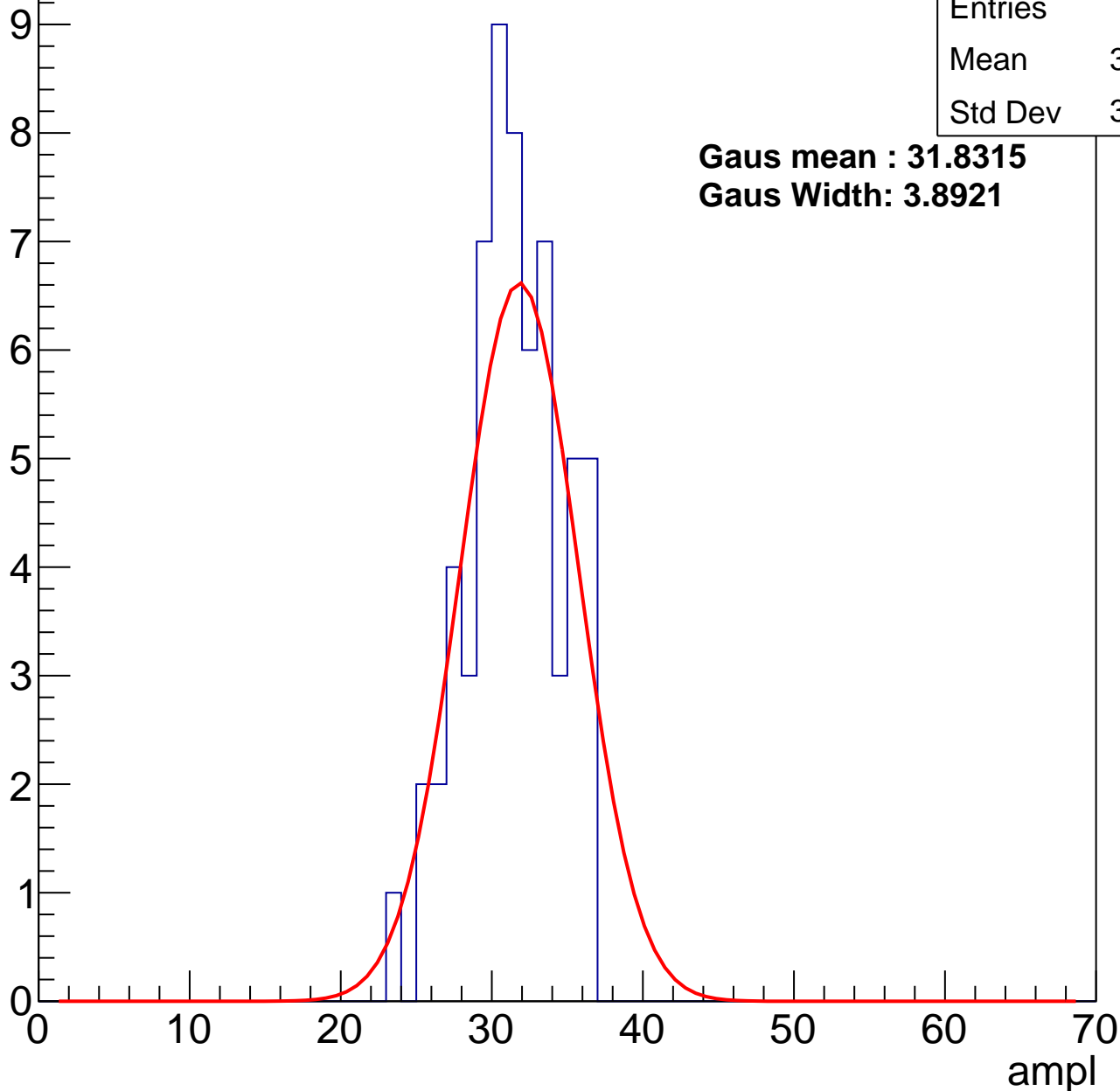
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	30.94
Std Dev	3.058

**Gaus mean : 31.8315**

**Gaus Width: 3.8921**



# B1L102S, U8-ch90, adc1

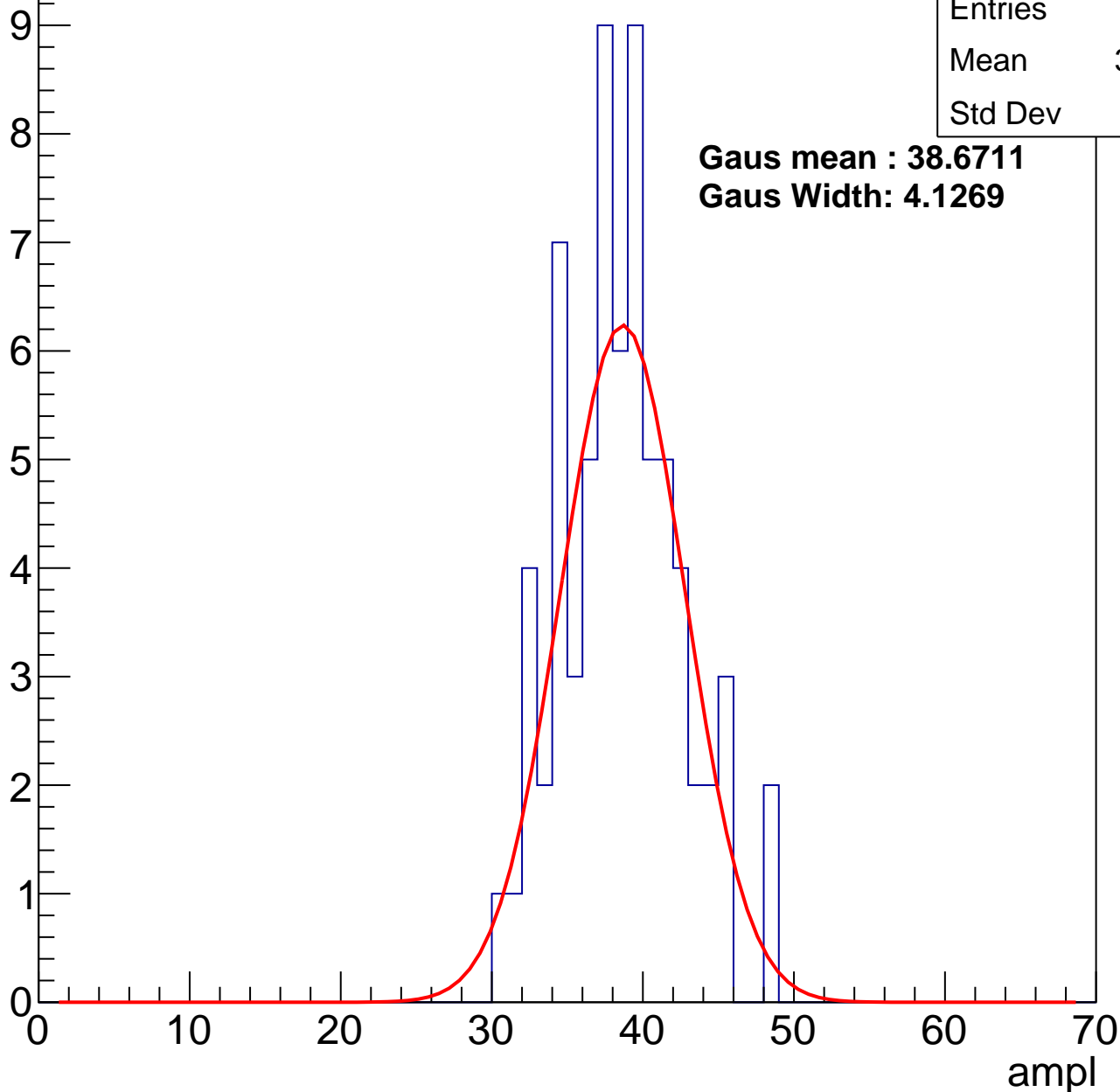
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	38.11
Std Dev	3.93

**Gaus mean : 38.6711**

**Gaus Width: 4.1269**



# B1L102S, U8-ch90, adc2

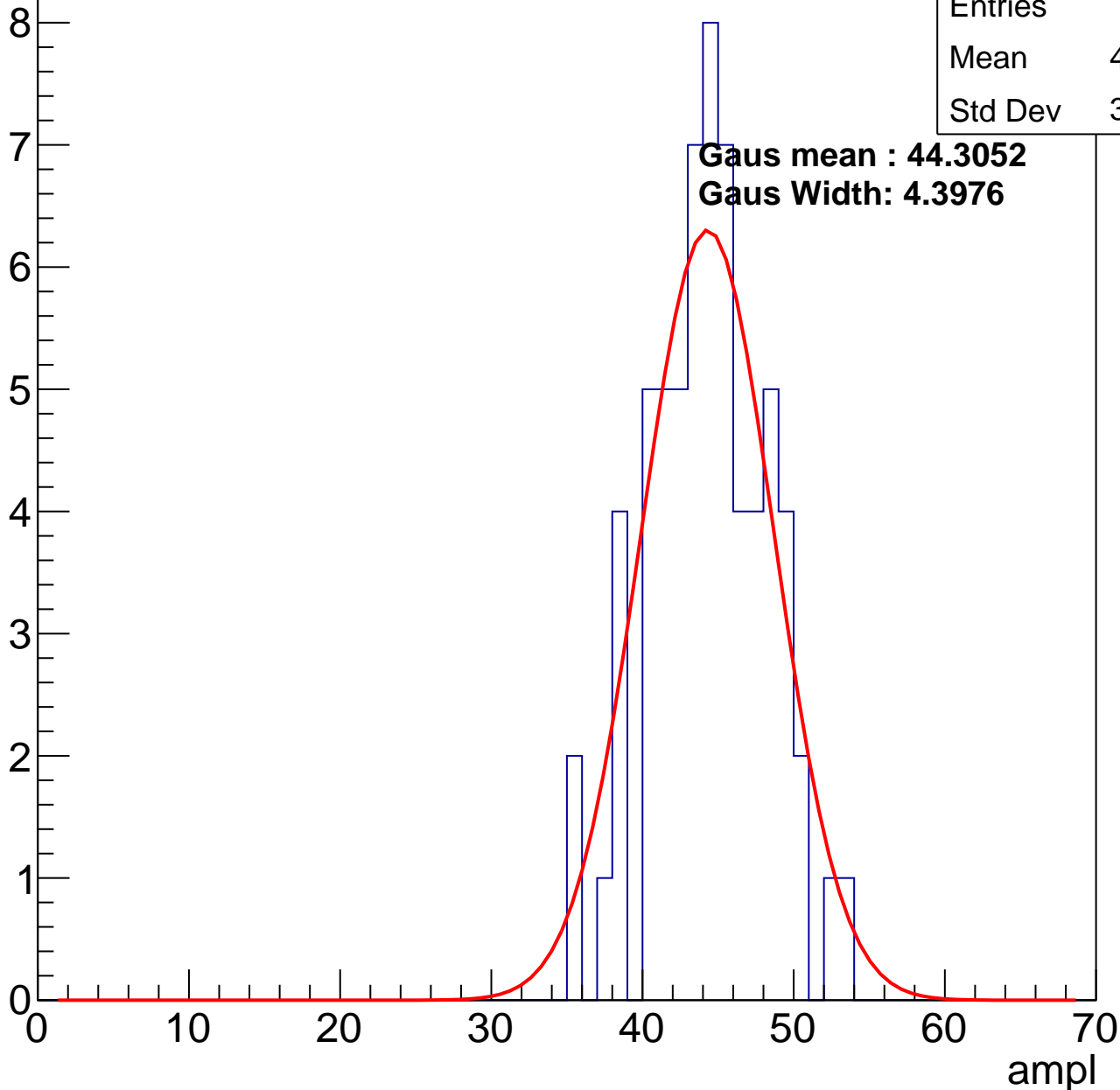
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	43.92
Std Dev	3.848

**Gaus mean : 44.3052**

**Gaus Width: 4.3976**

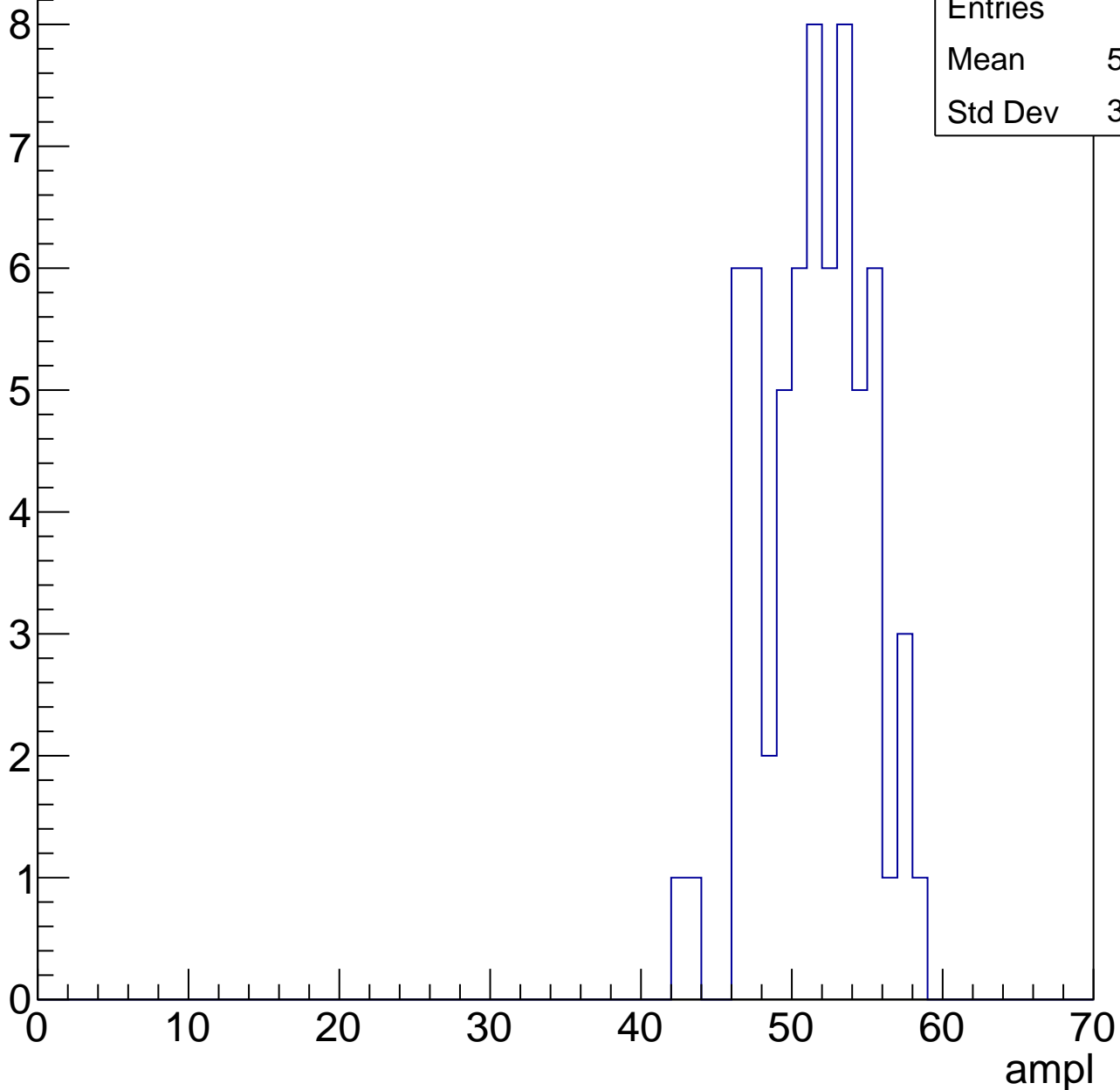


# B1L102S, U8-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	50.97
Std Dev	3.499

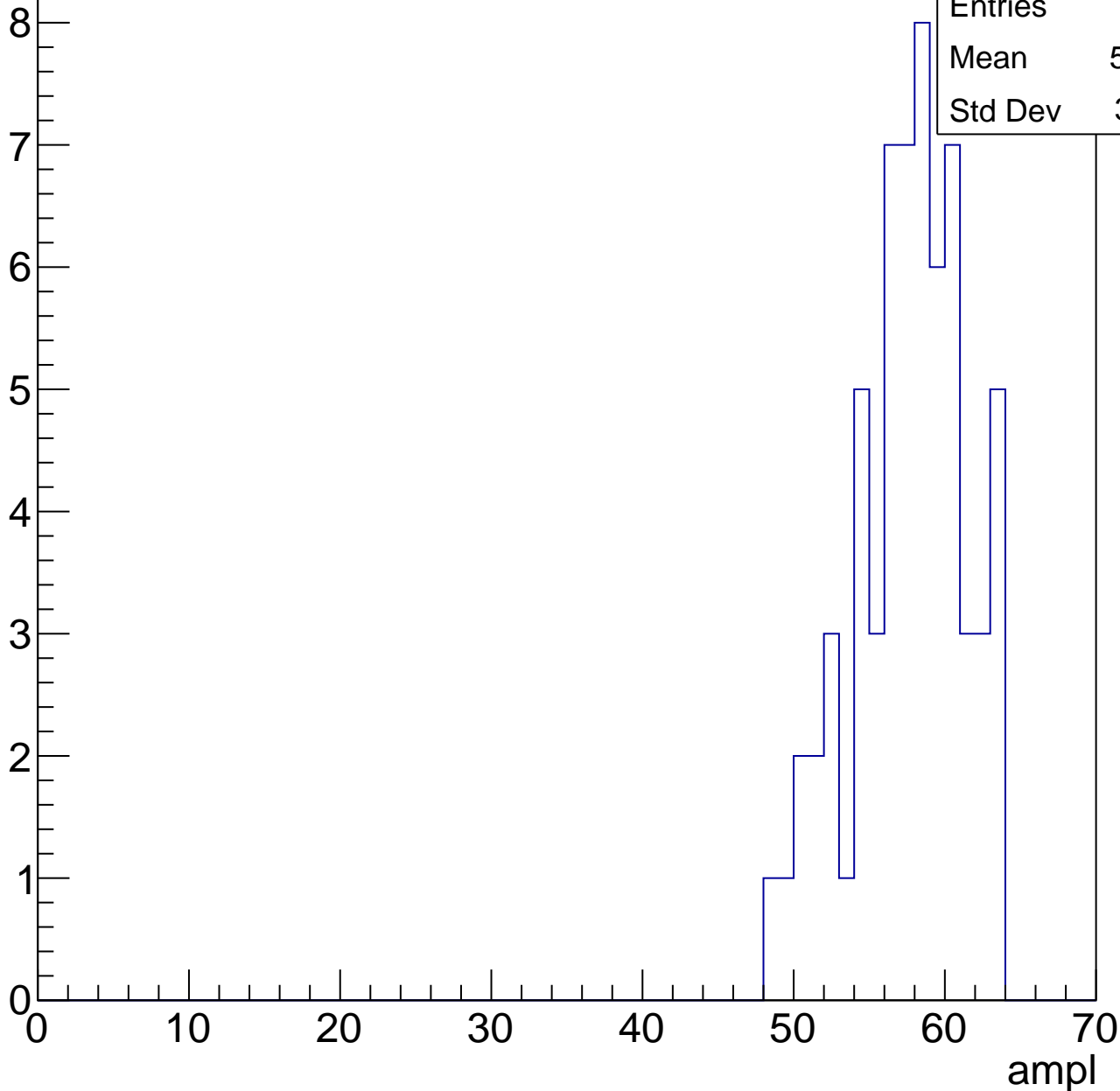


# B1L102S, U8-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	57.12
Std Dev	3.681

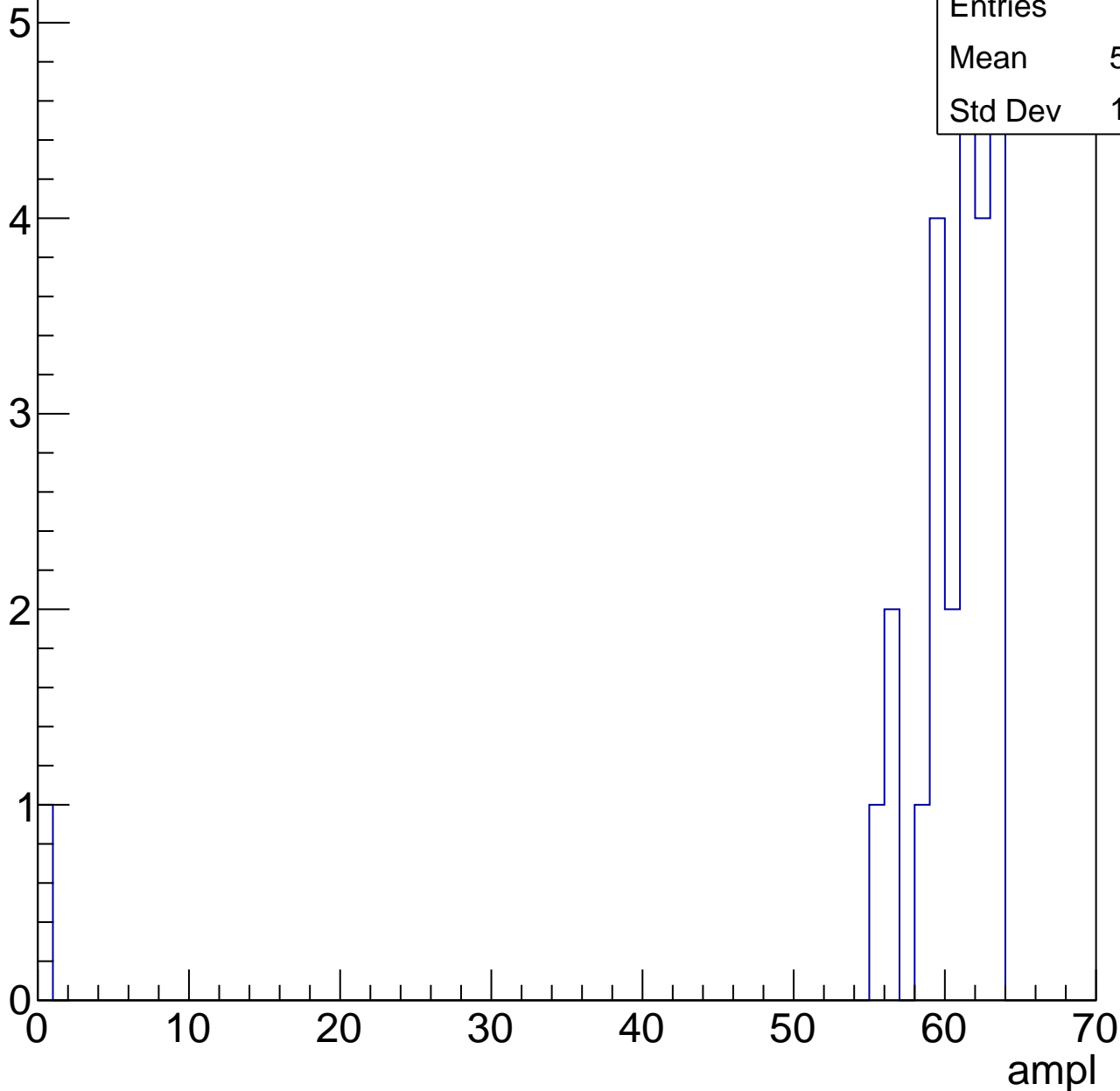


# B1L102S, U8-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

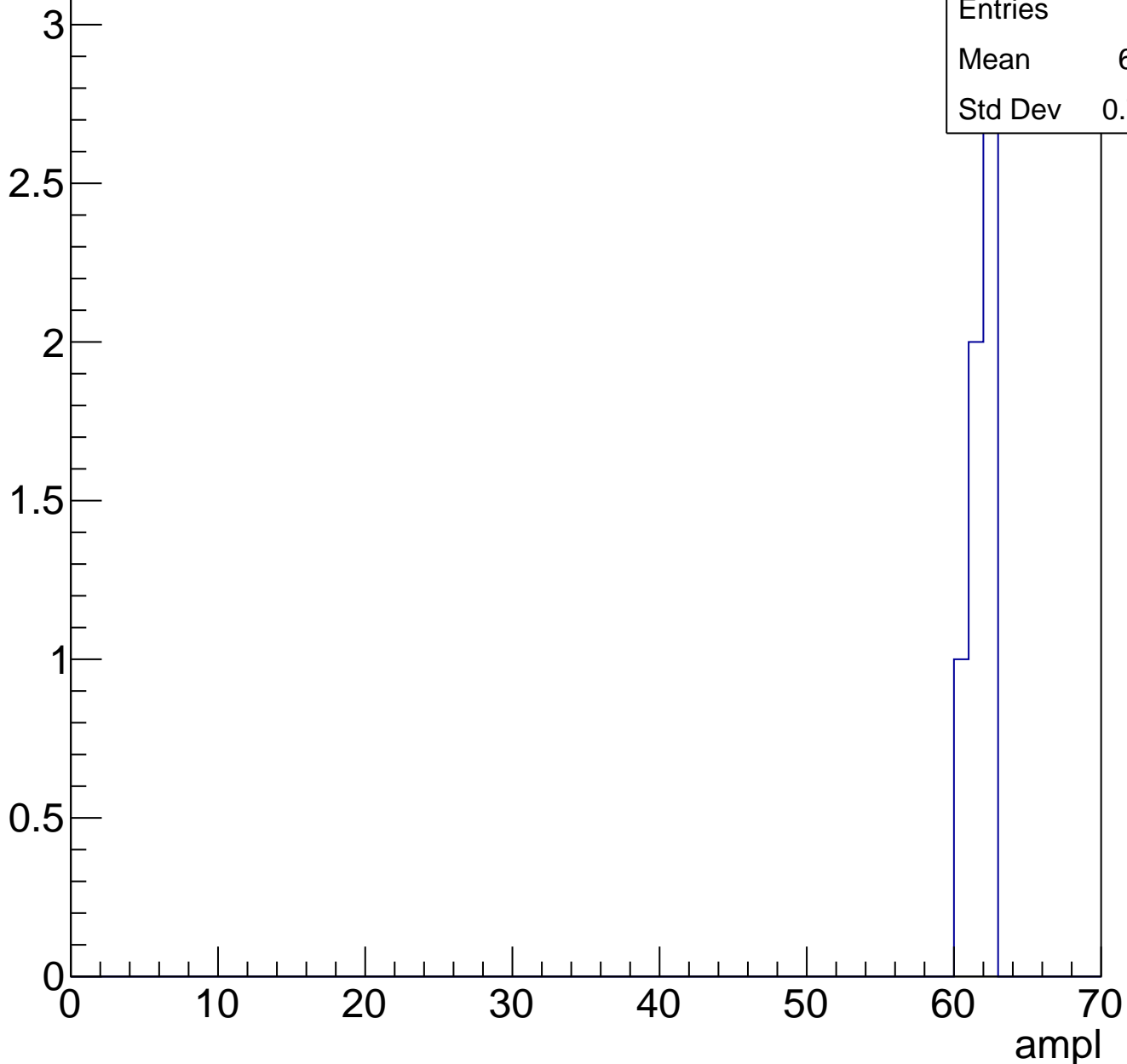
Entries	25
Mean	57.96
Std Dev	12.04



# B1L102S, U8-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch91, adc0

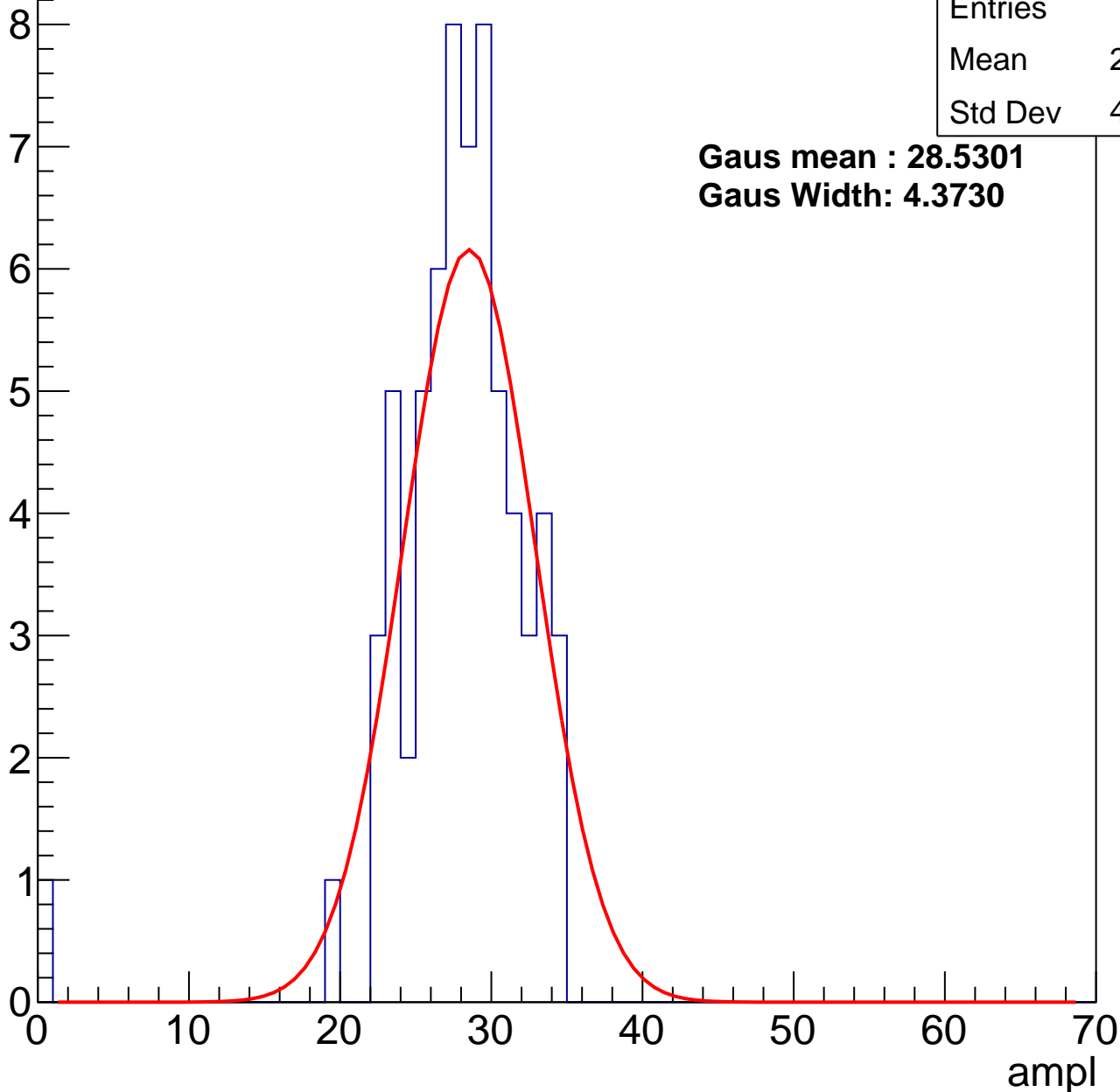
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	27.34
Std Dev	4.802

**Gaus mean : 28.5301**

**Gaus Width: 4.3730**



# B1L102S, U8-ch91, adc1

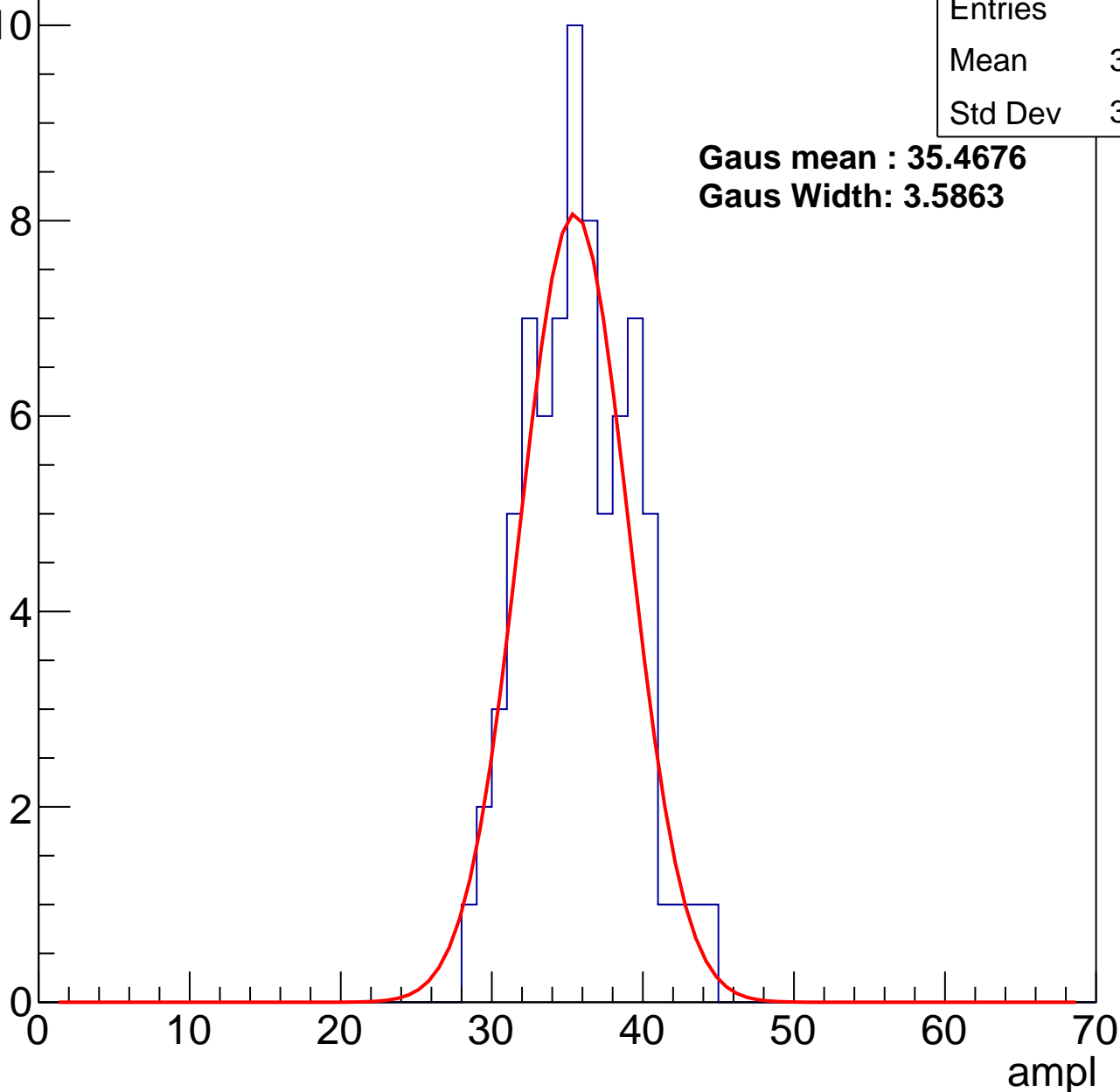
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	35.33
Std Dev	3.462

**Gaus mean : 35.4676**

**Gaus Width: 3.5863**



# B1L102S, U8-ch91, adc2

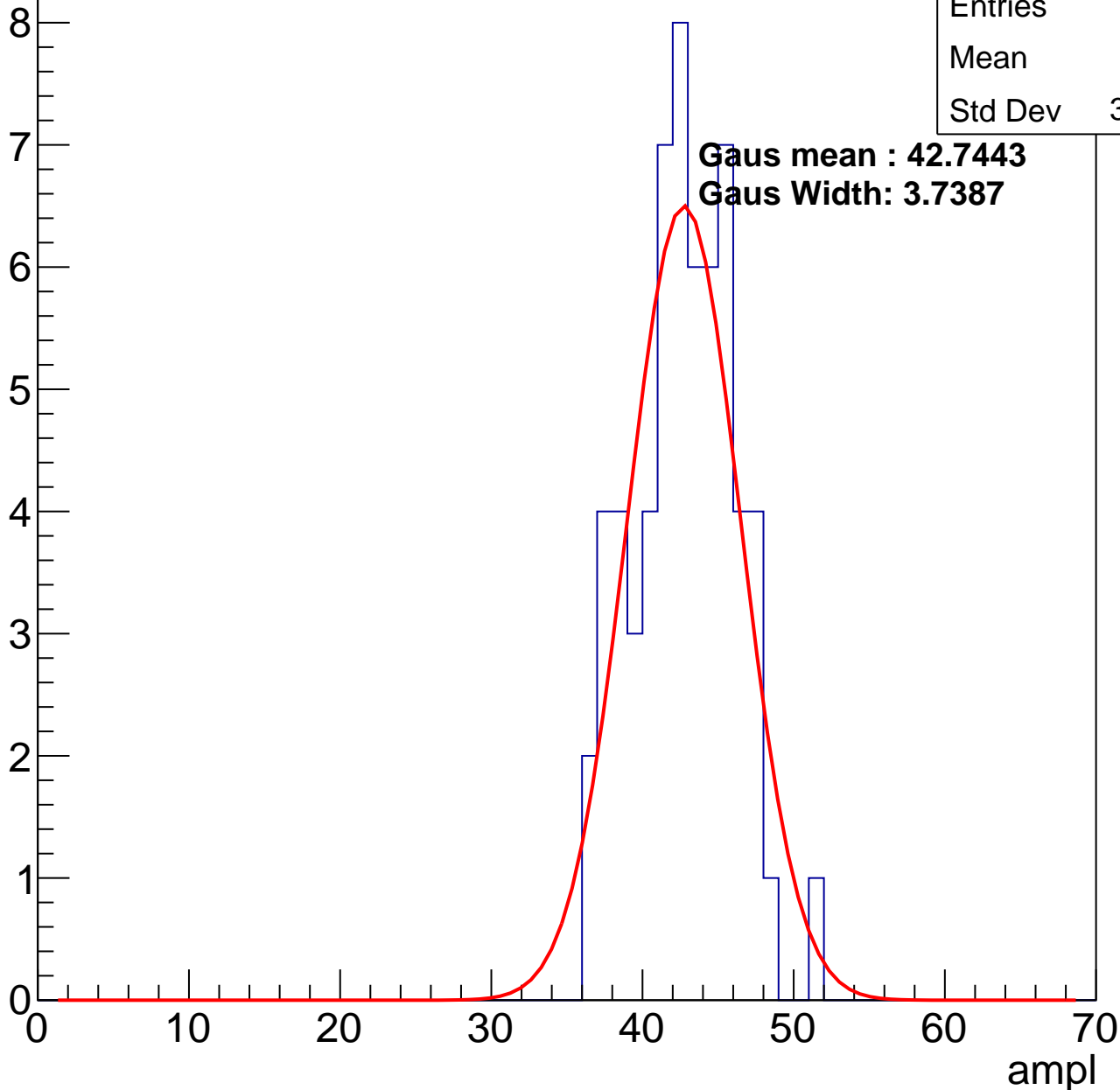
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	42.3
Std Dev	3.276

**Gaus mean : 42.7443**

**Gaus Width: 3.7387**

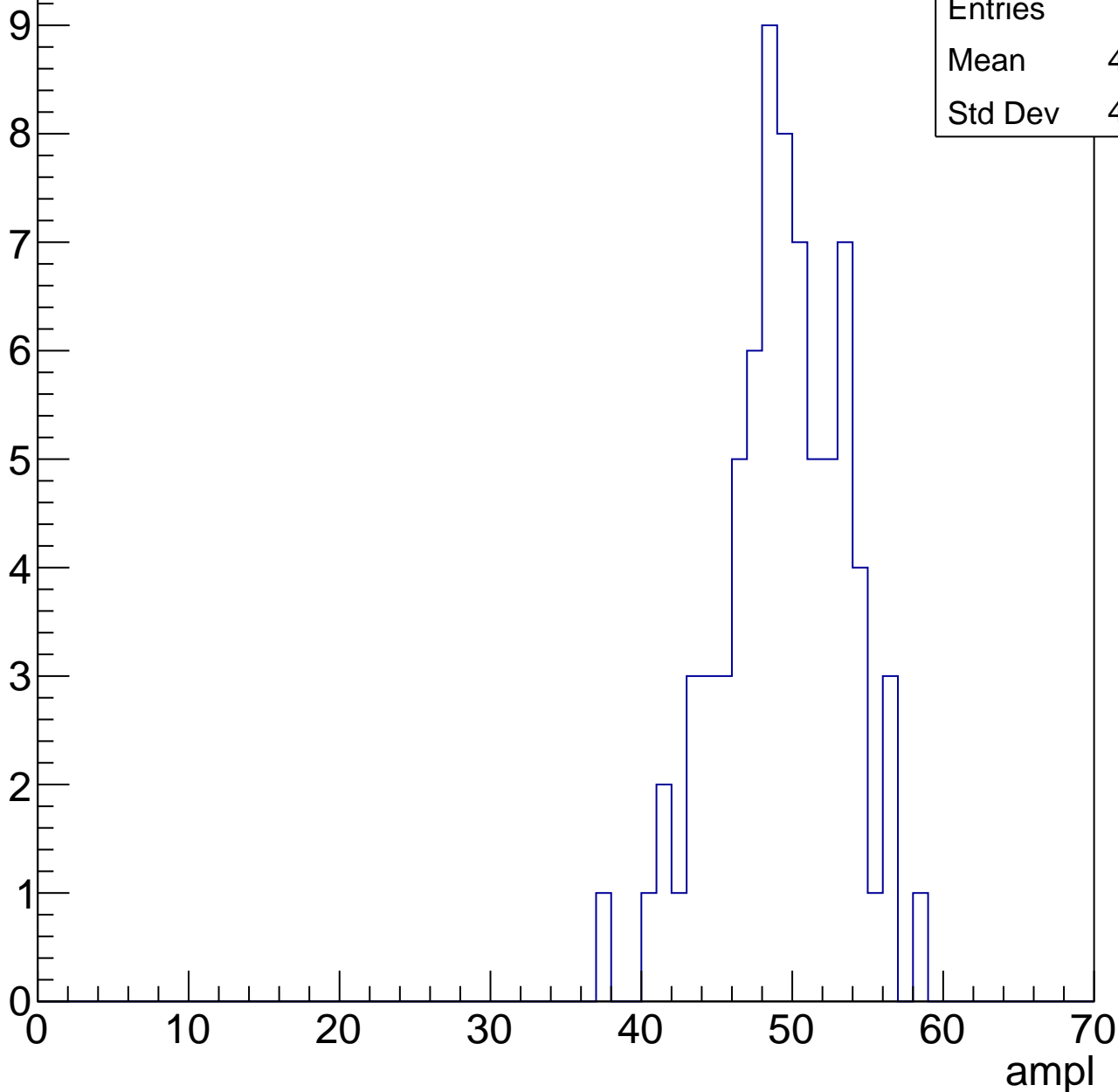


# B1L102S, U8-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	48.88
Std Dev	4.095

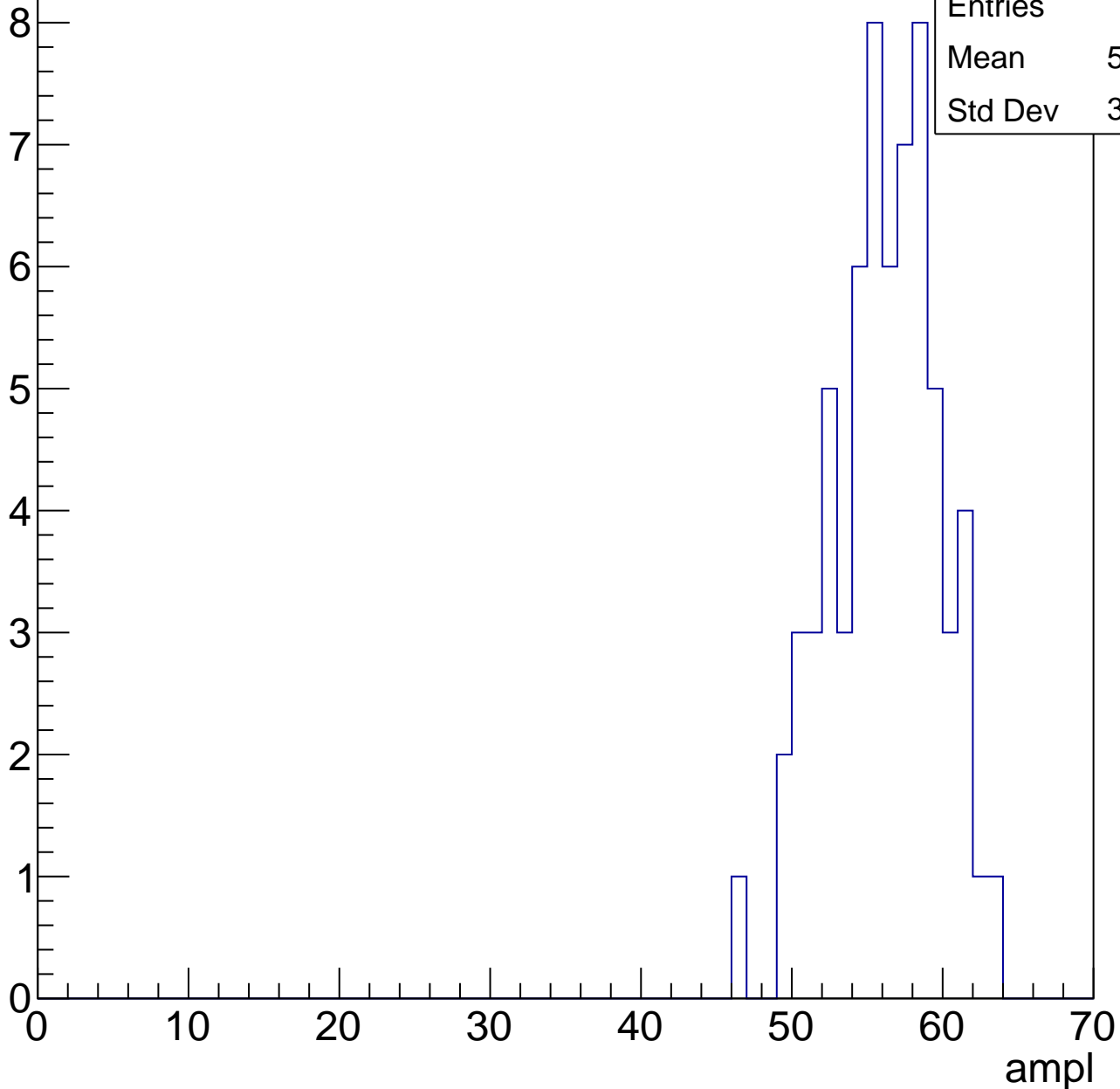


# B1L102S, U8-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	55.65
Std Dev	3.544

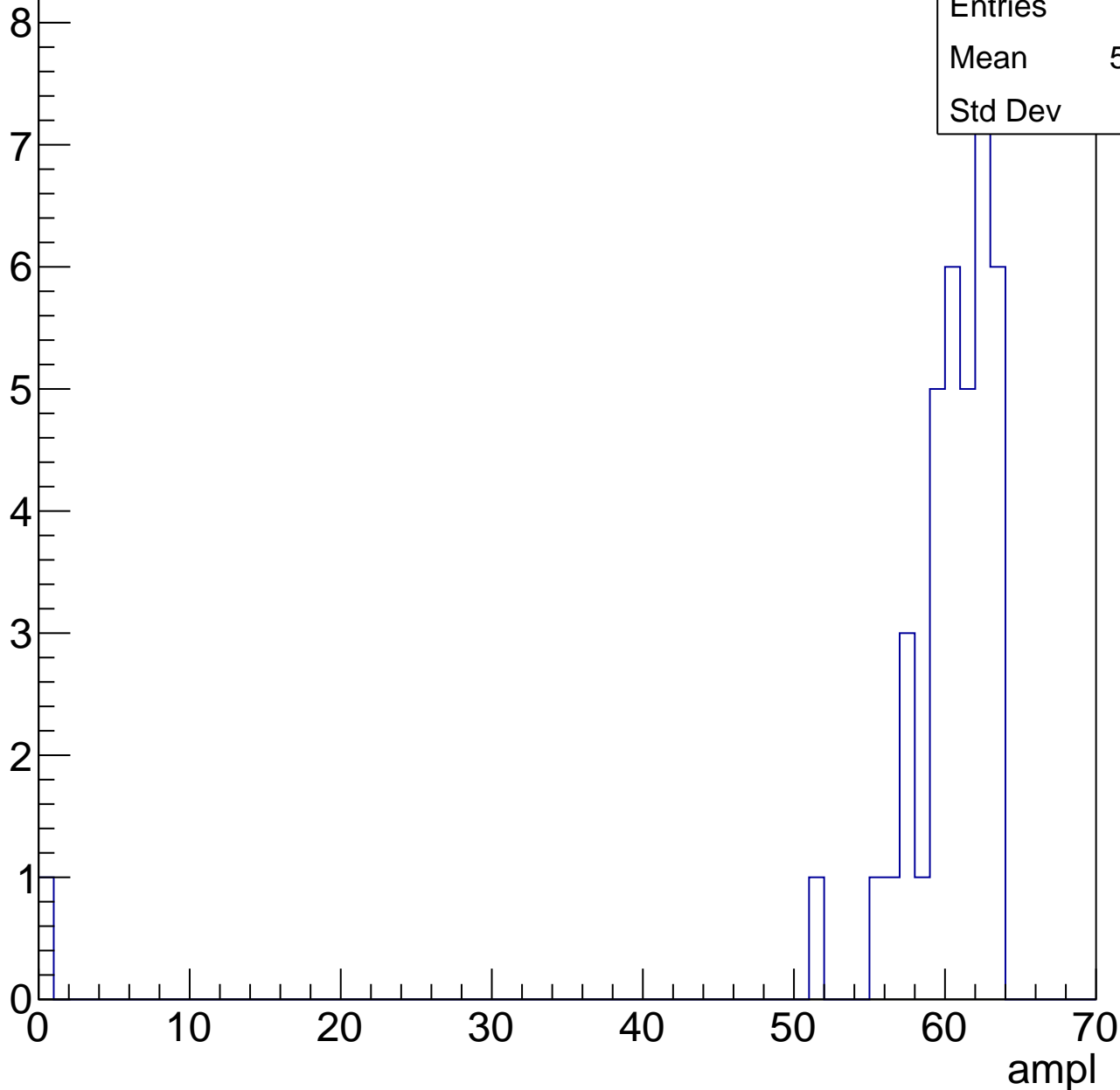


# B1L102S, U8-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

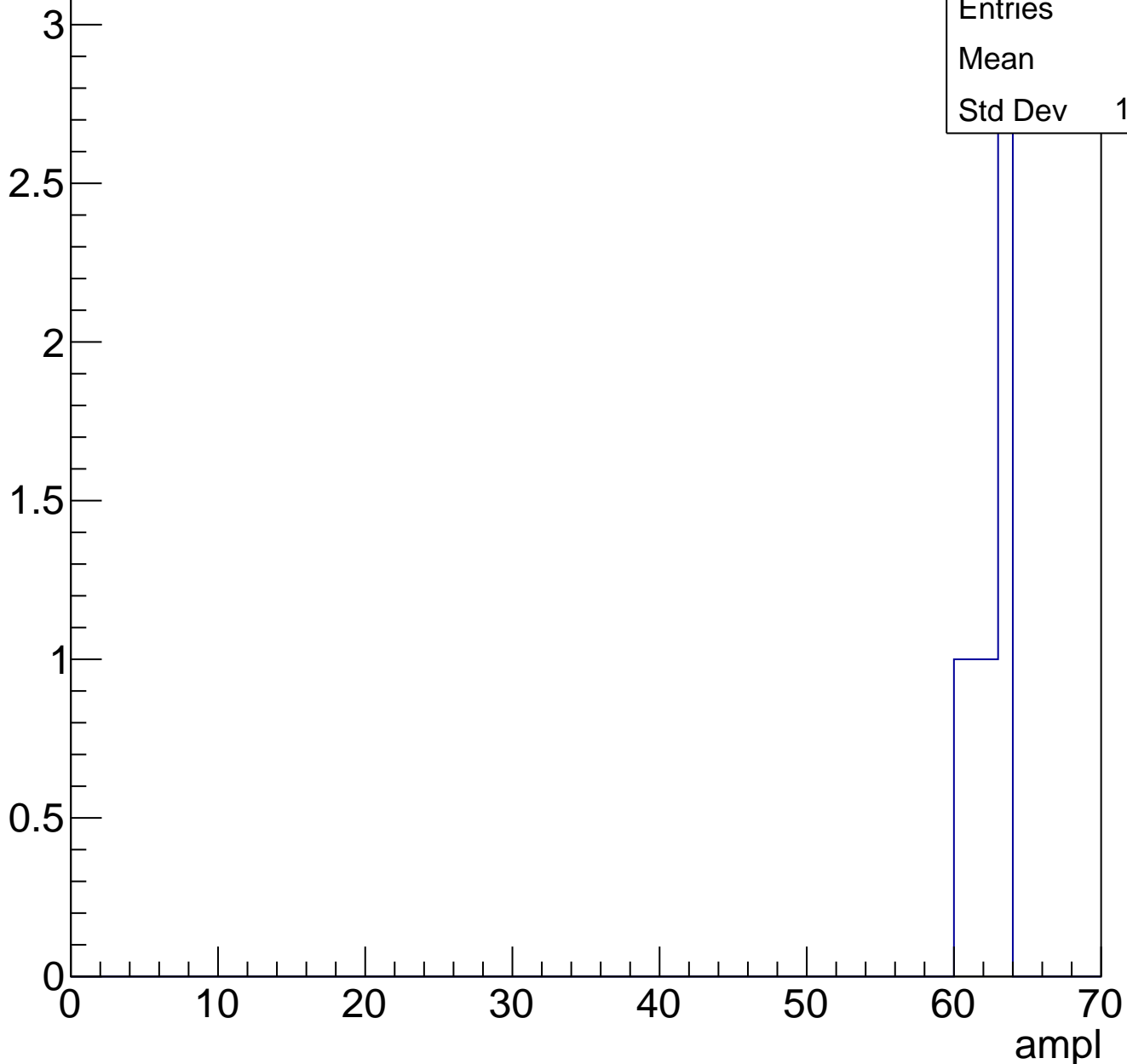
Entries	38
Mean	58.55
Std Dev	9.96



# B1L102S, U8-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch92, adc0

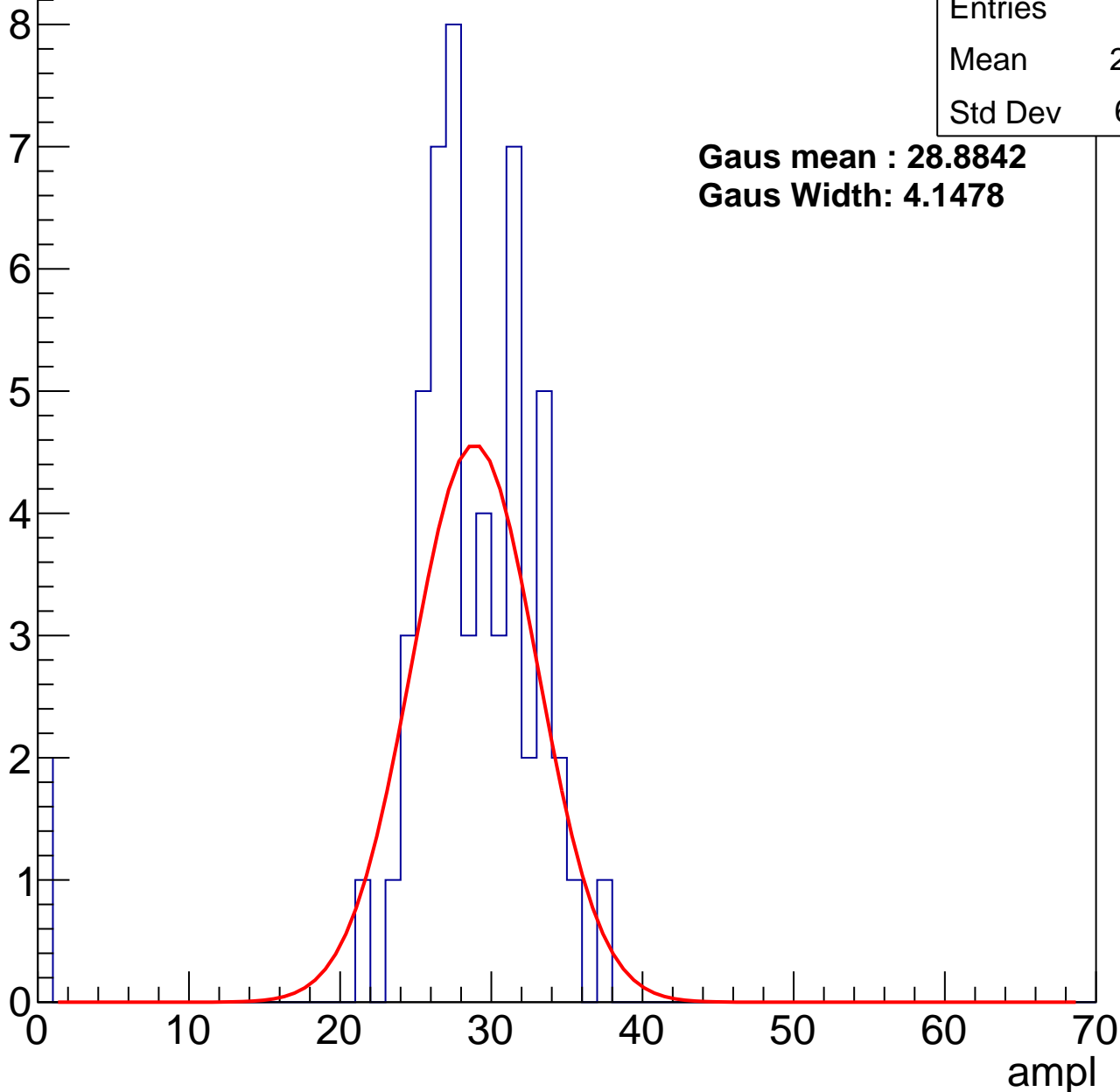
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	27.55
Std Dev	6.321

**Gaus mean : 28.8842**

**Gaus Width: 4.1478**



# B1L102S, U8-ch92, adc1

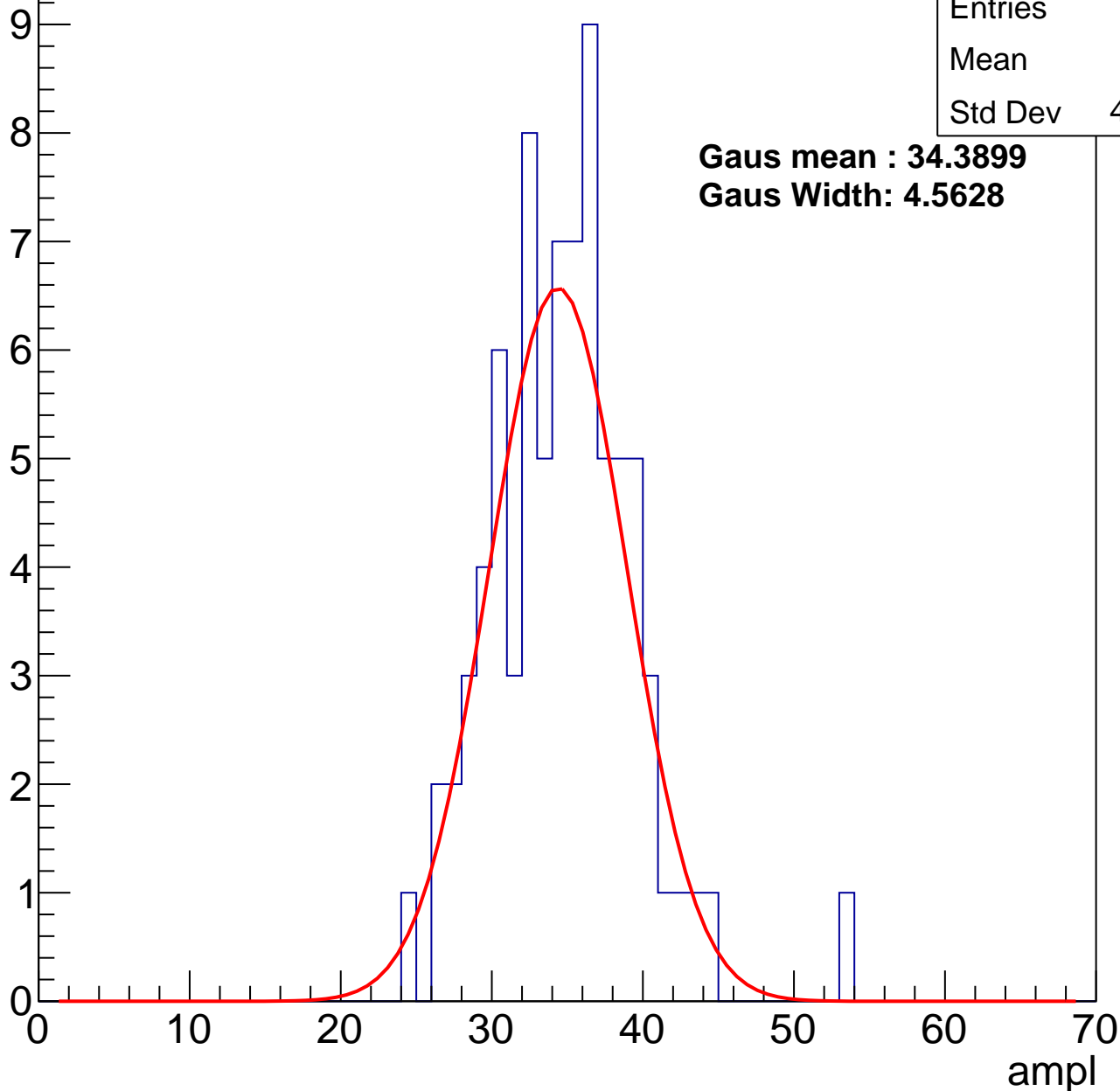
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	34.3
Std Dev	4.667

**Gaus mean : 34.3899**

**Gaus Width: 4.5628**



# B1L102S, U8-ch92, adc2

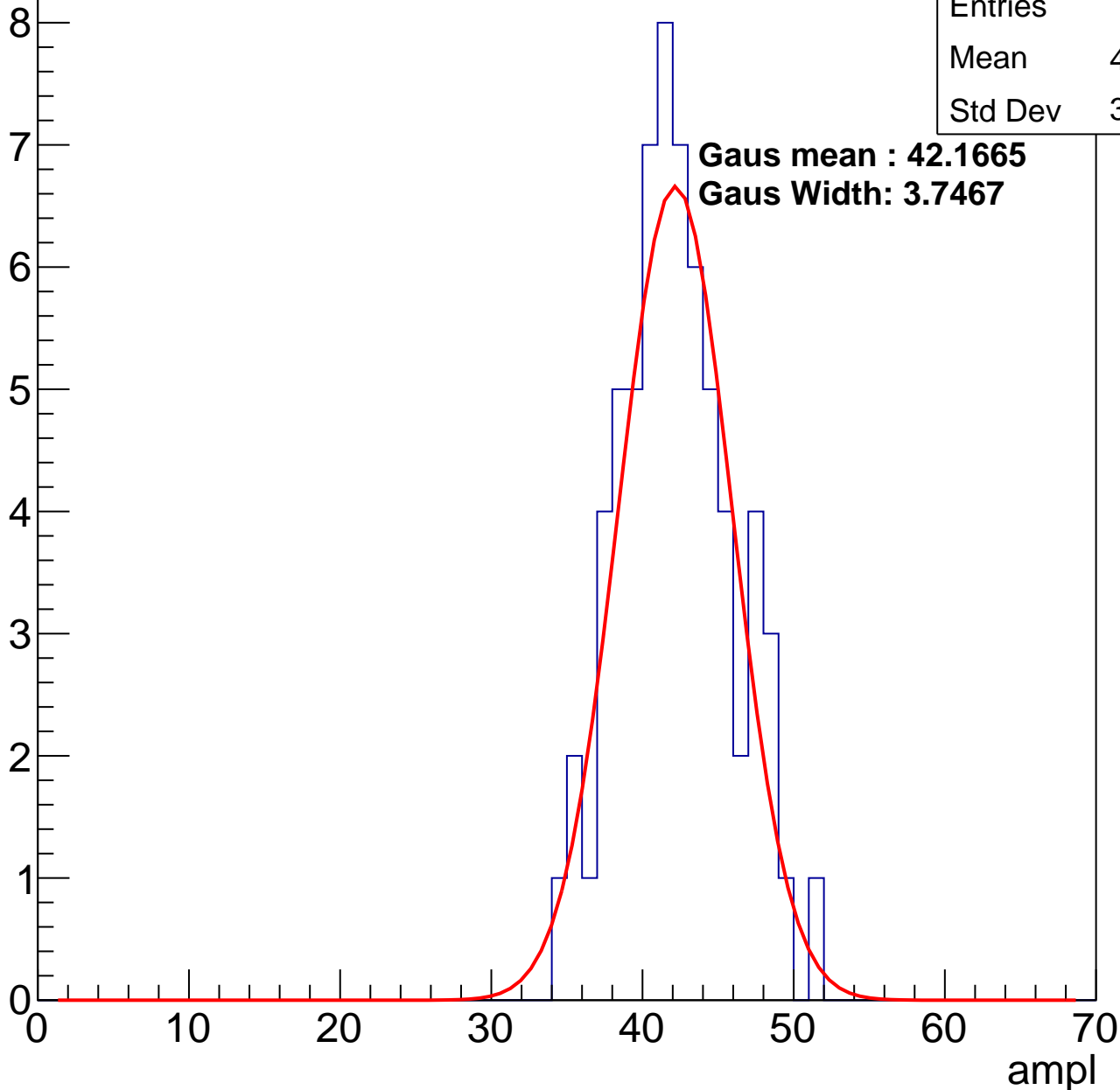
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	41.77
Std Dev	3.667

**Gaus mean : 42.1665**

**Gaus Width: 3.7467**

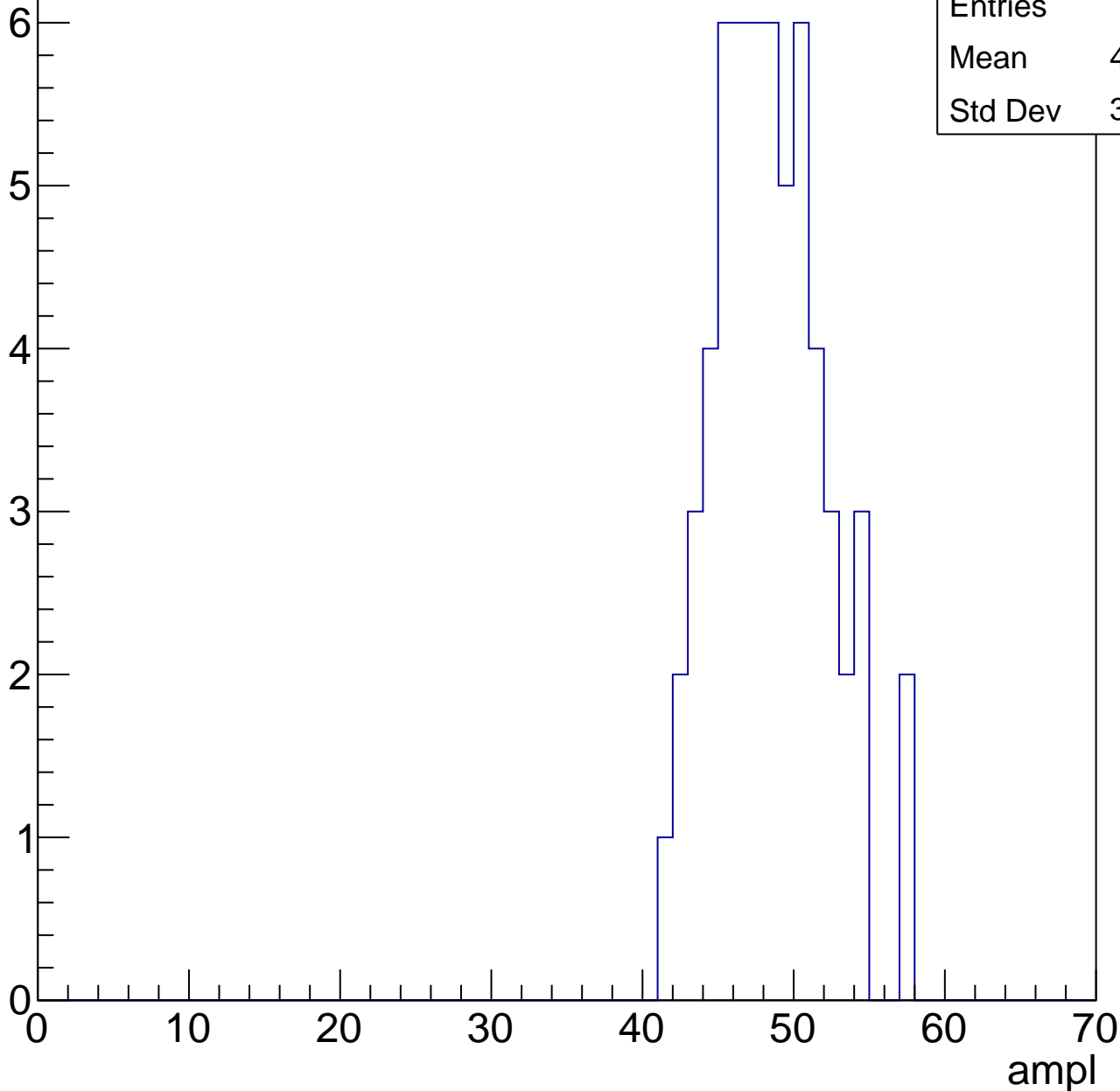


# B1L102S, U8-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	48.02
Std Dev	3.629

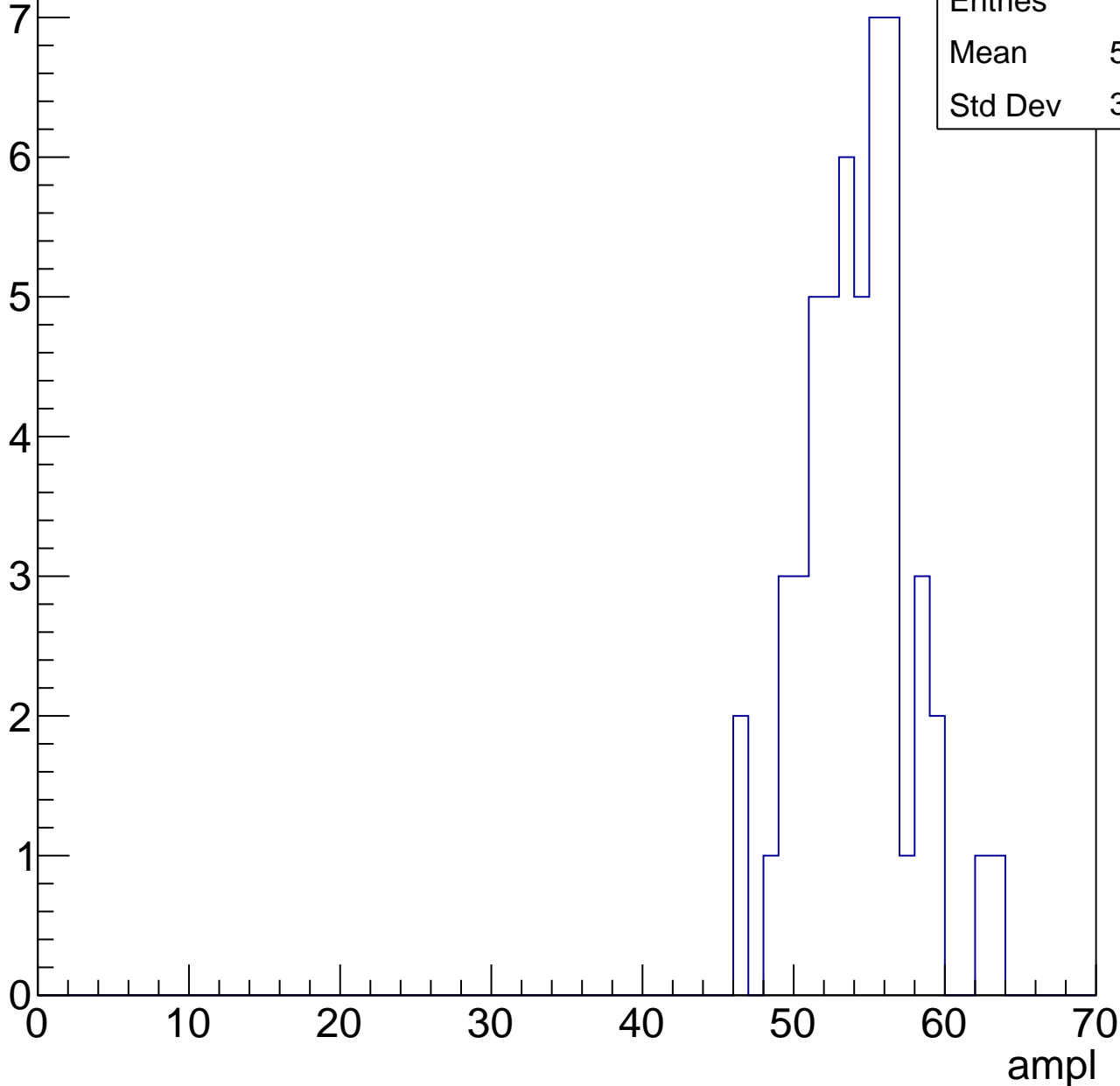


# B1L102S, U8-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

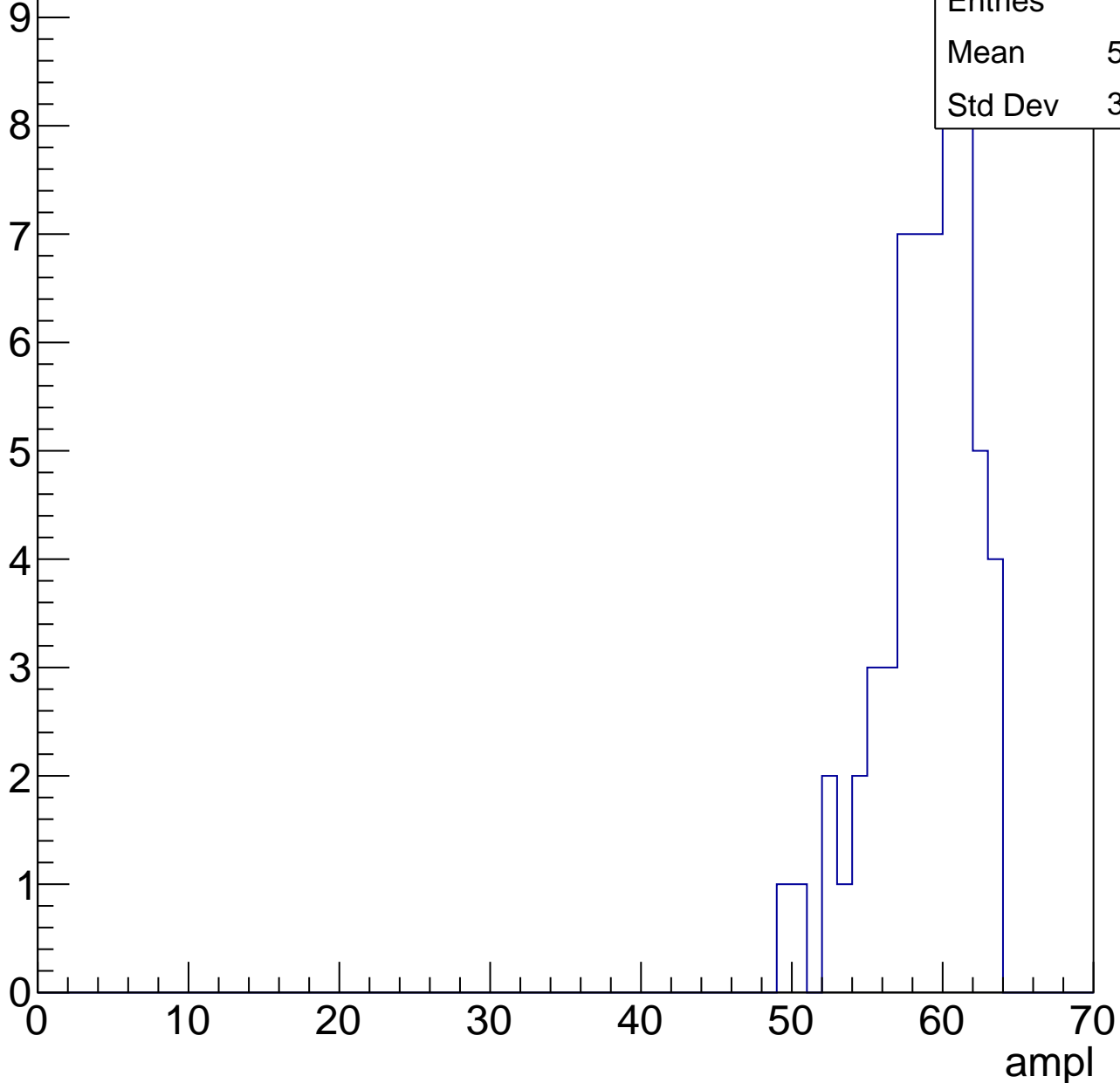
Entries	52
Mean	53.67
Std Dev	3.507



# B1L102S, U8-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

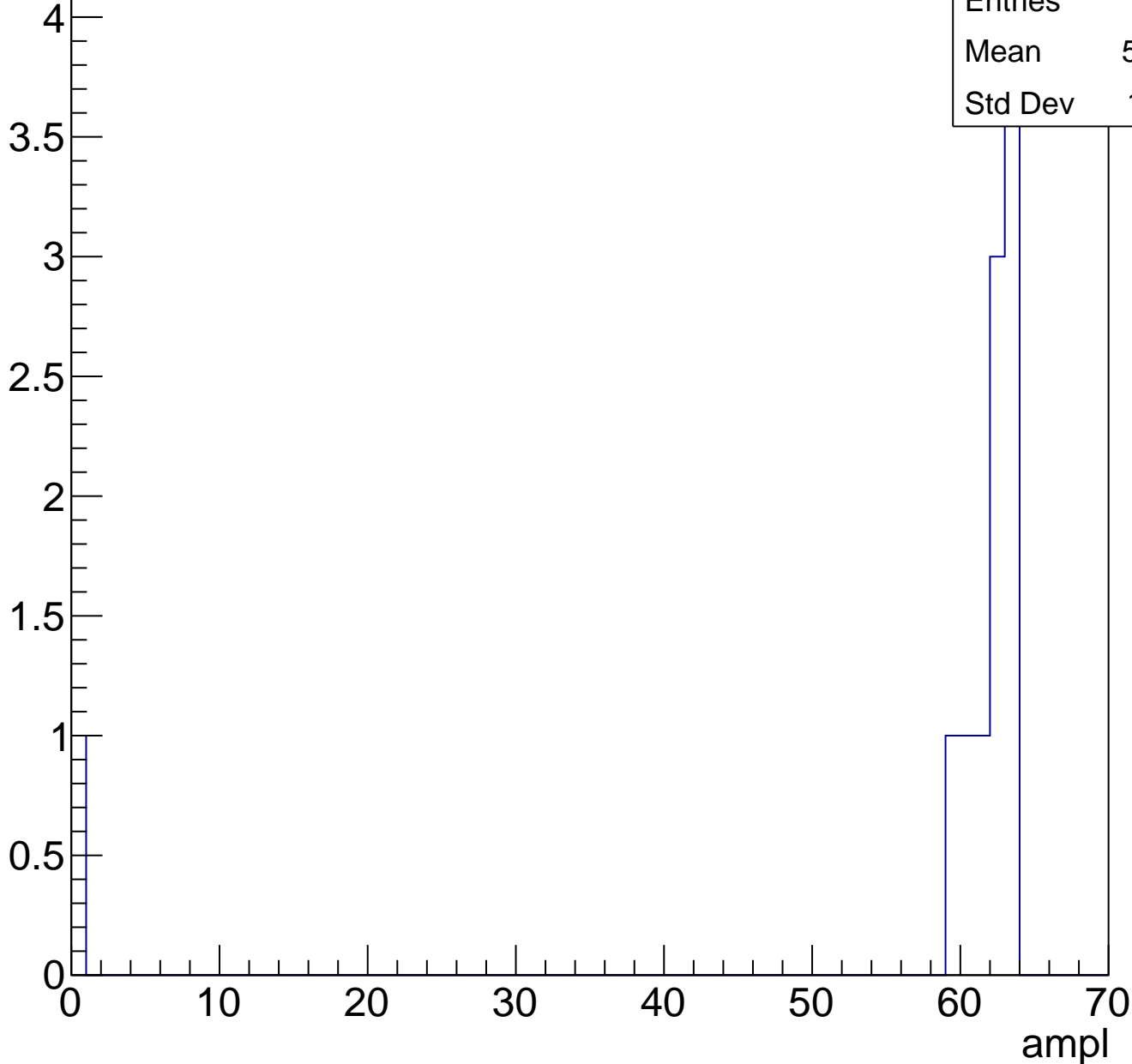
Entry



# B1L102S, U8-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

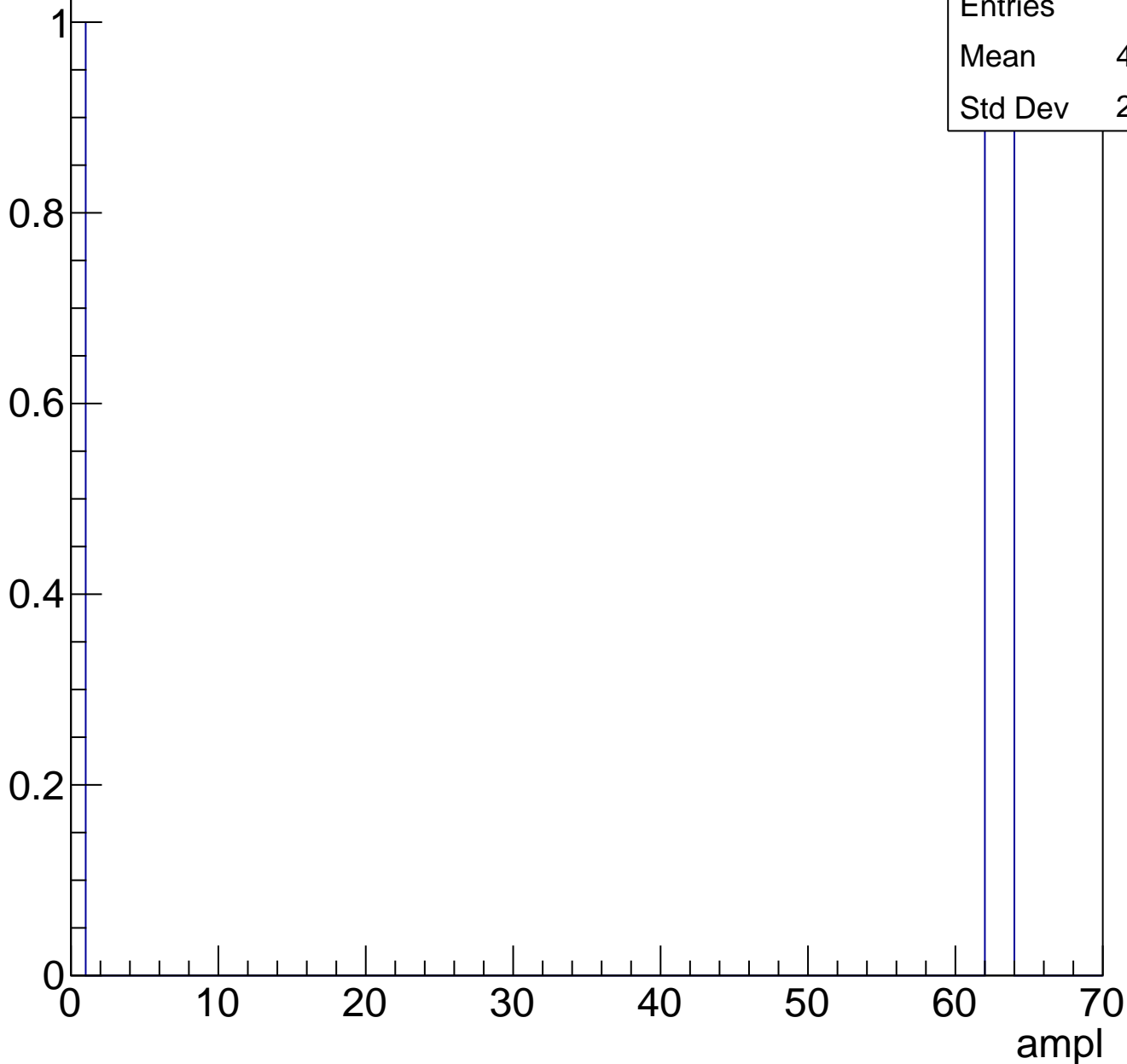




# B1L102S, U8-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch93, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	77
Mean	27.97
Std Dev	3.542

**Gaus mean : 27.9938**

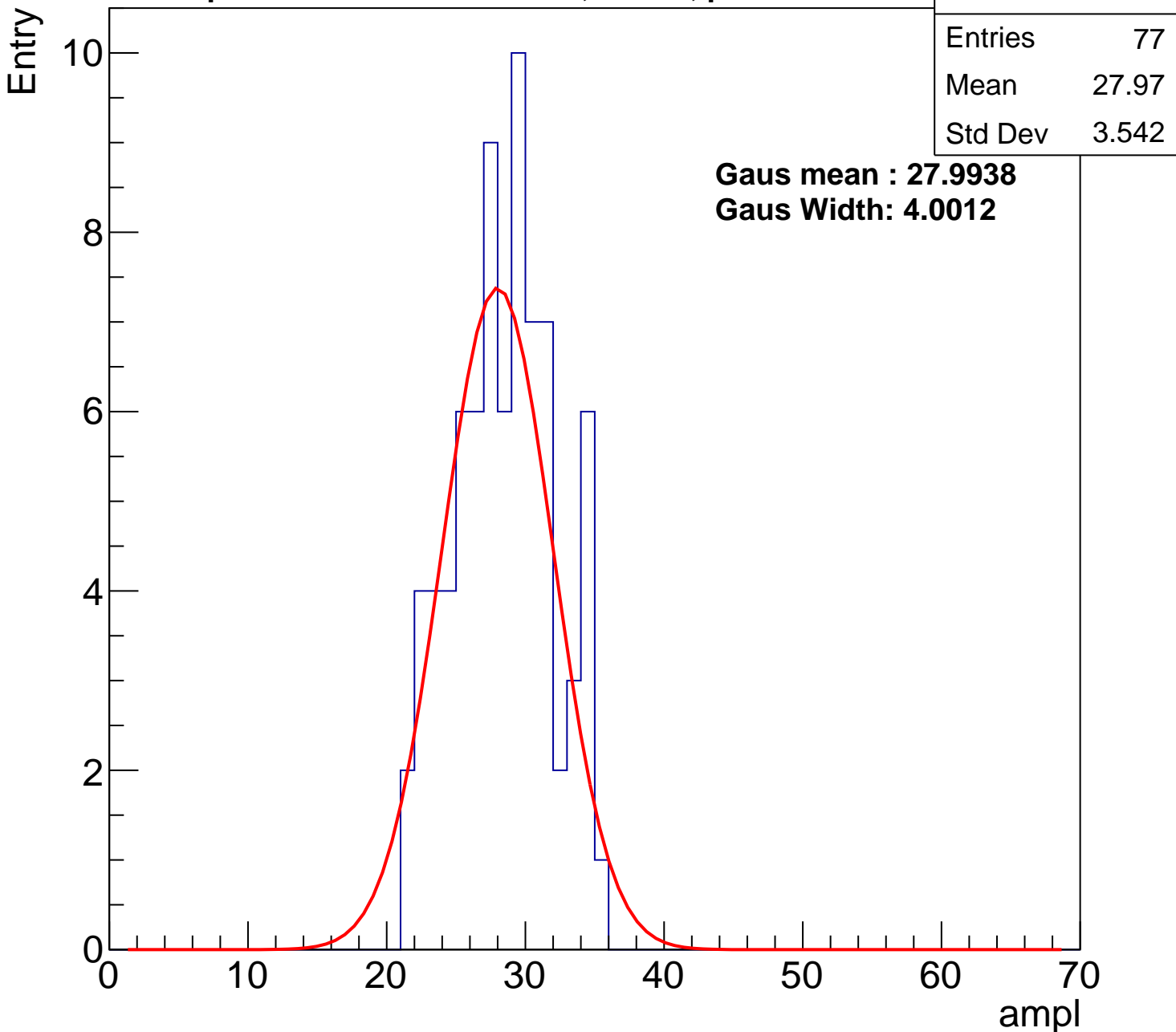
**Gaus Width: 4.0012**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U8-ch93, adc1

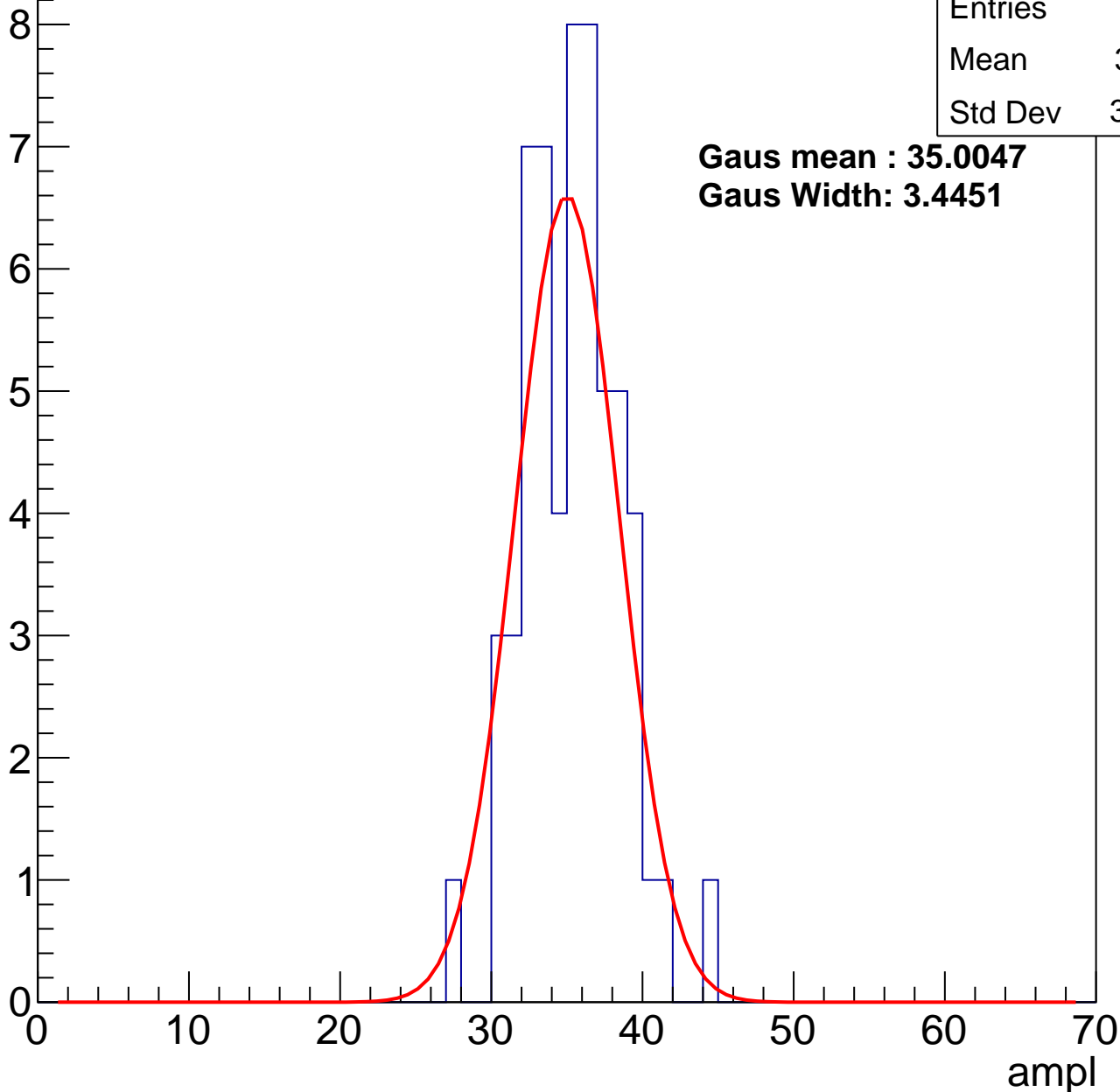
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	34.91
Std Dev	3.109

**Gaus mean : 35.0047**

**Gaus Width: 3.4451**



# B1L102S, U8-ch93, adc2

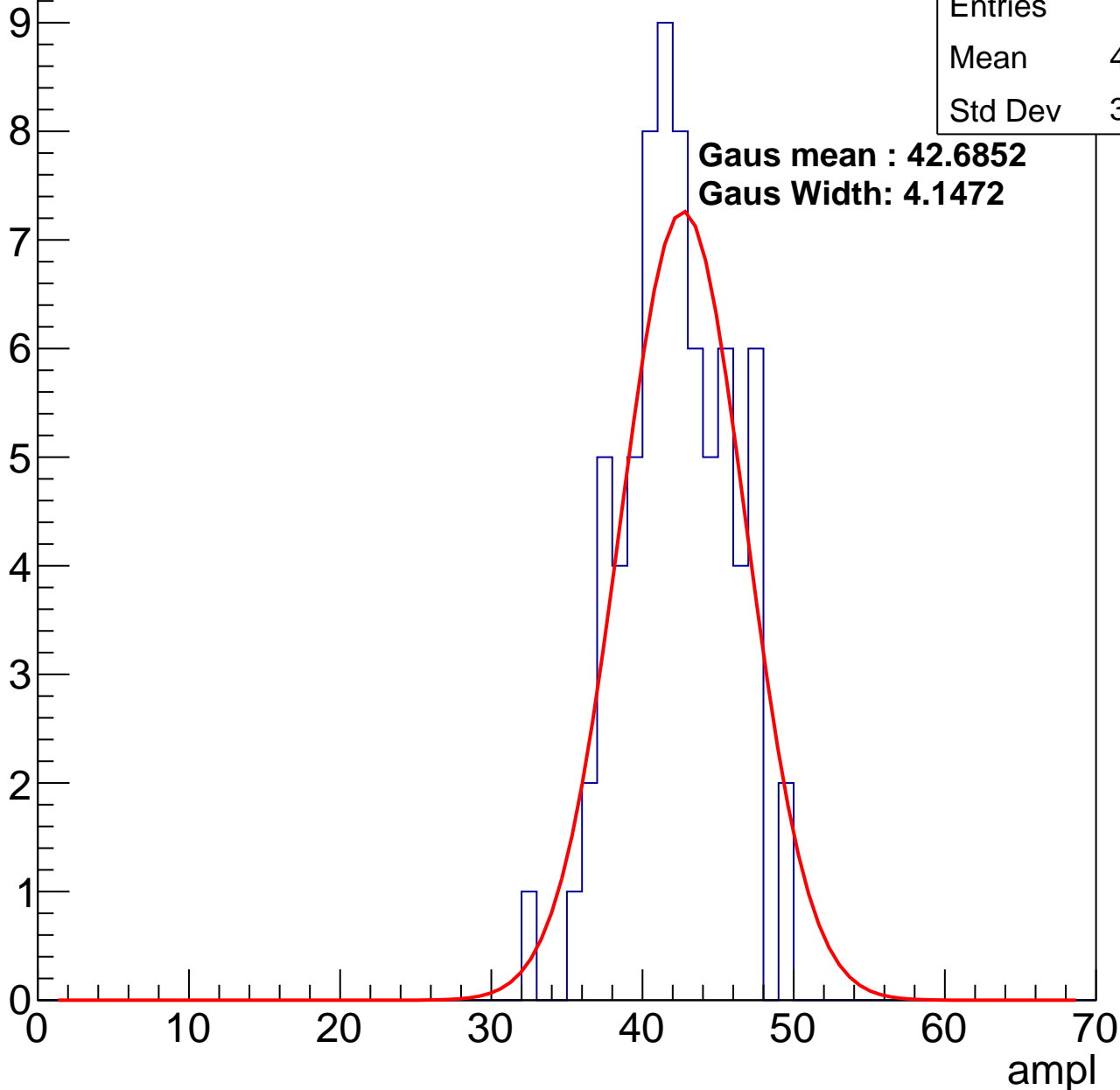
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	41.78
Std Dev	3.505

**Gaus mean : 42.6852**

**Gaus Width: 4.1472**

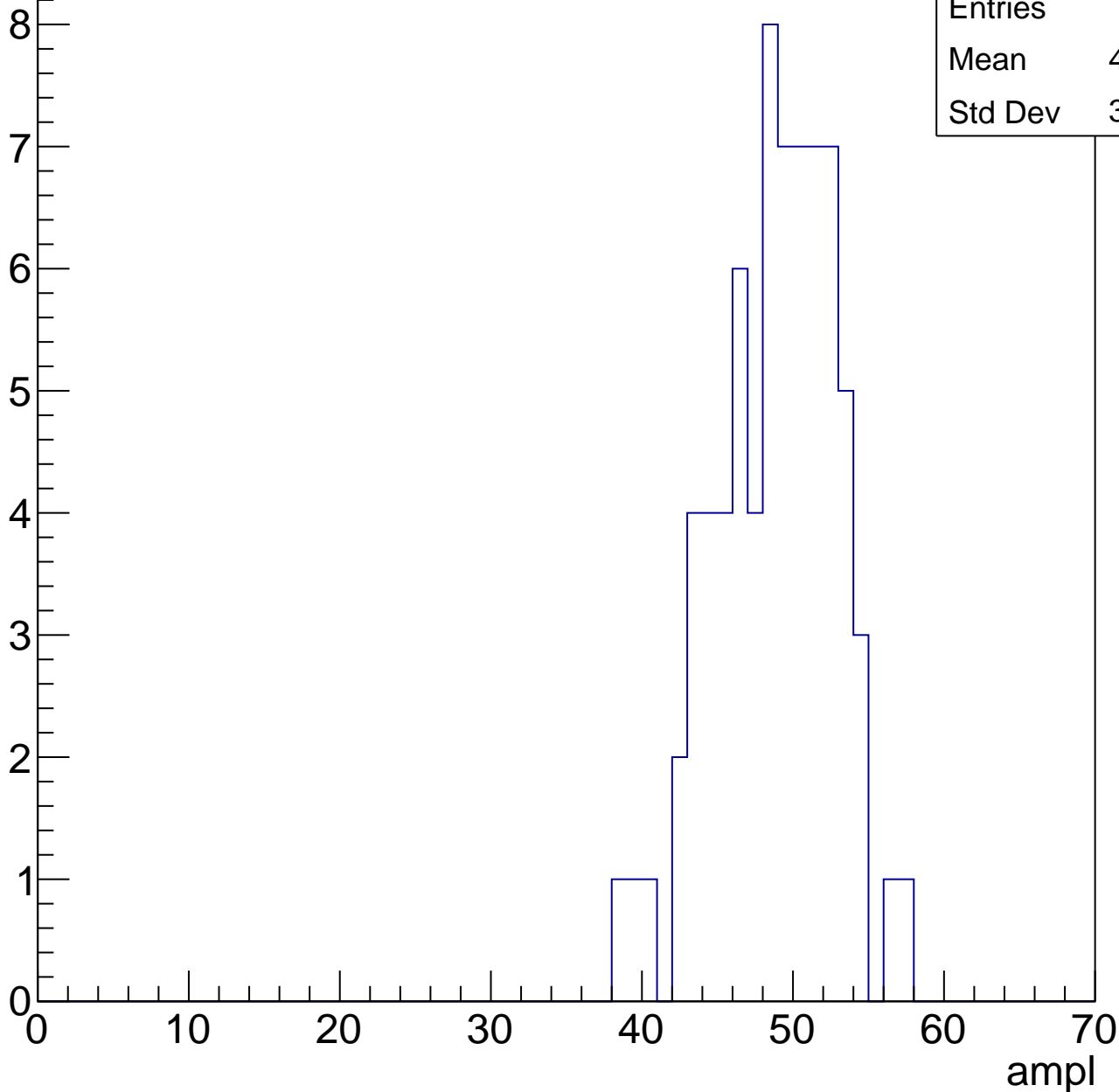


# B1L102S, U8-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	48.37
Std Dev	3.922

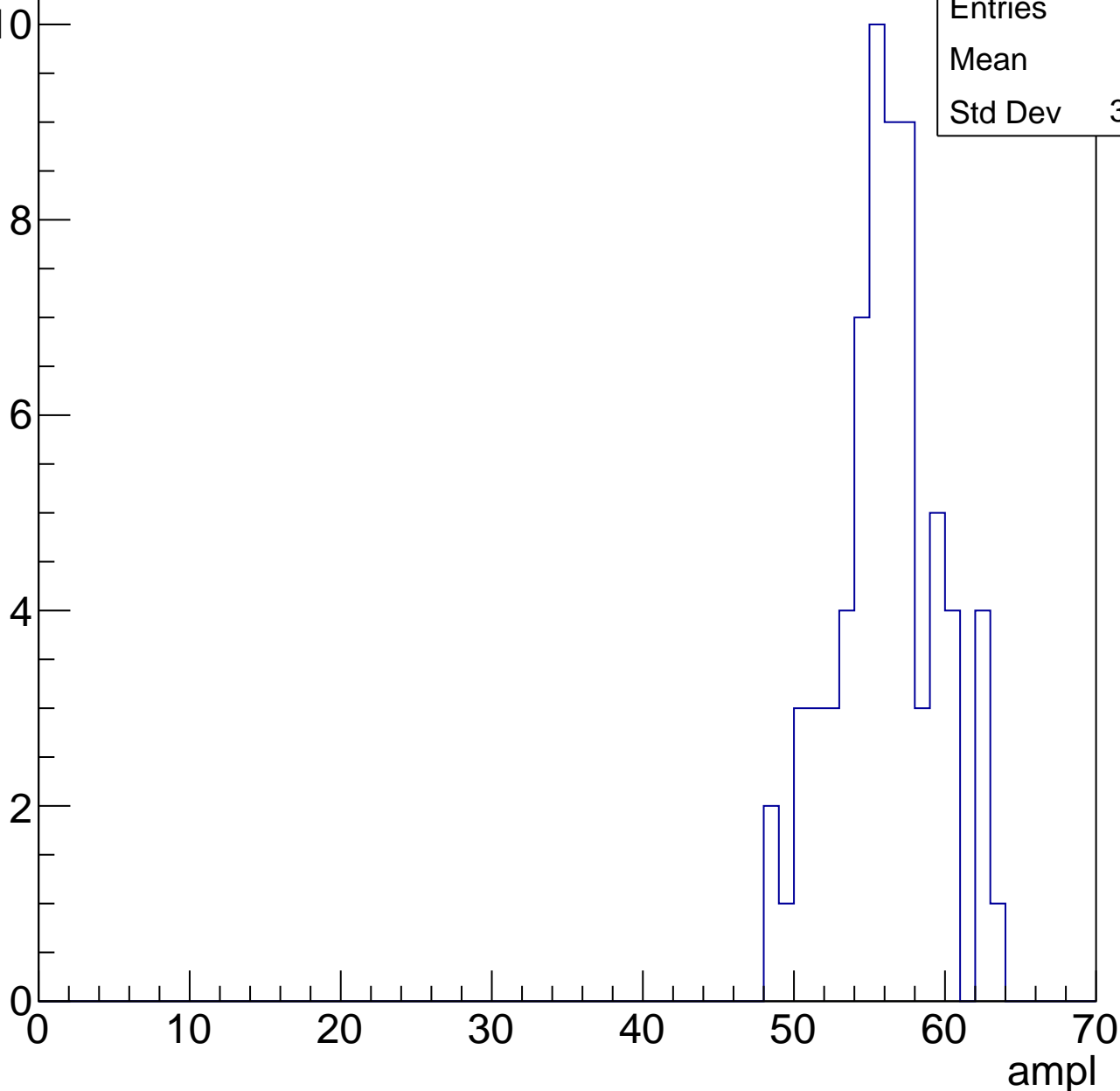


# B1L102S, U8-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	55.6
Std Dev	3.418

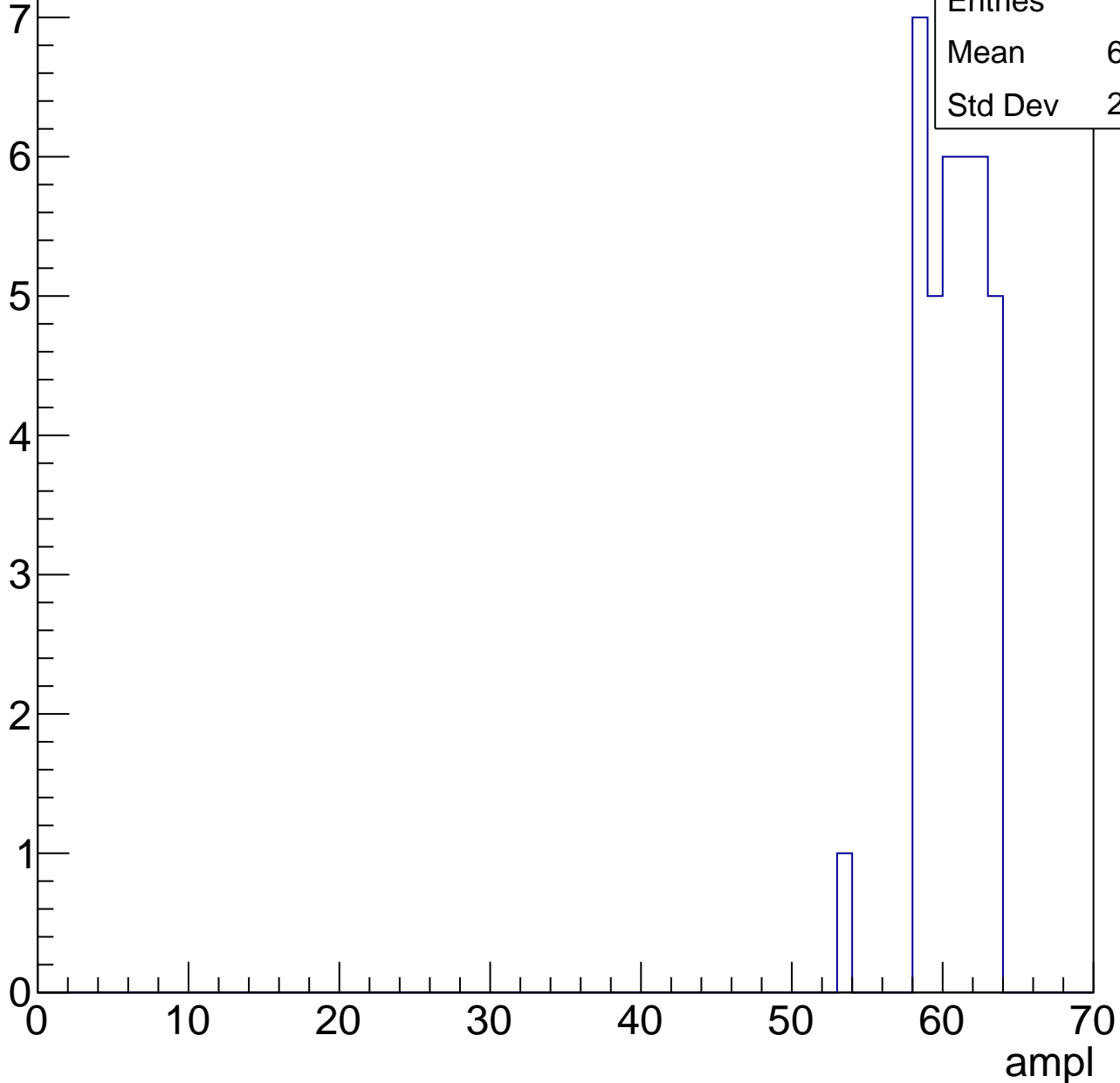


# B1L102S, U8-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

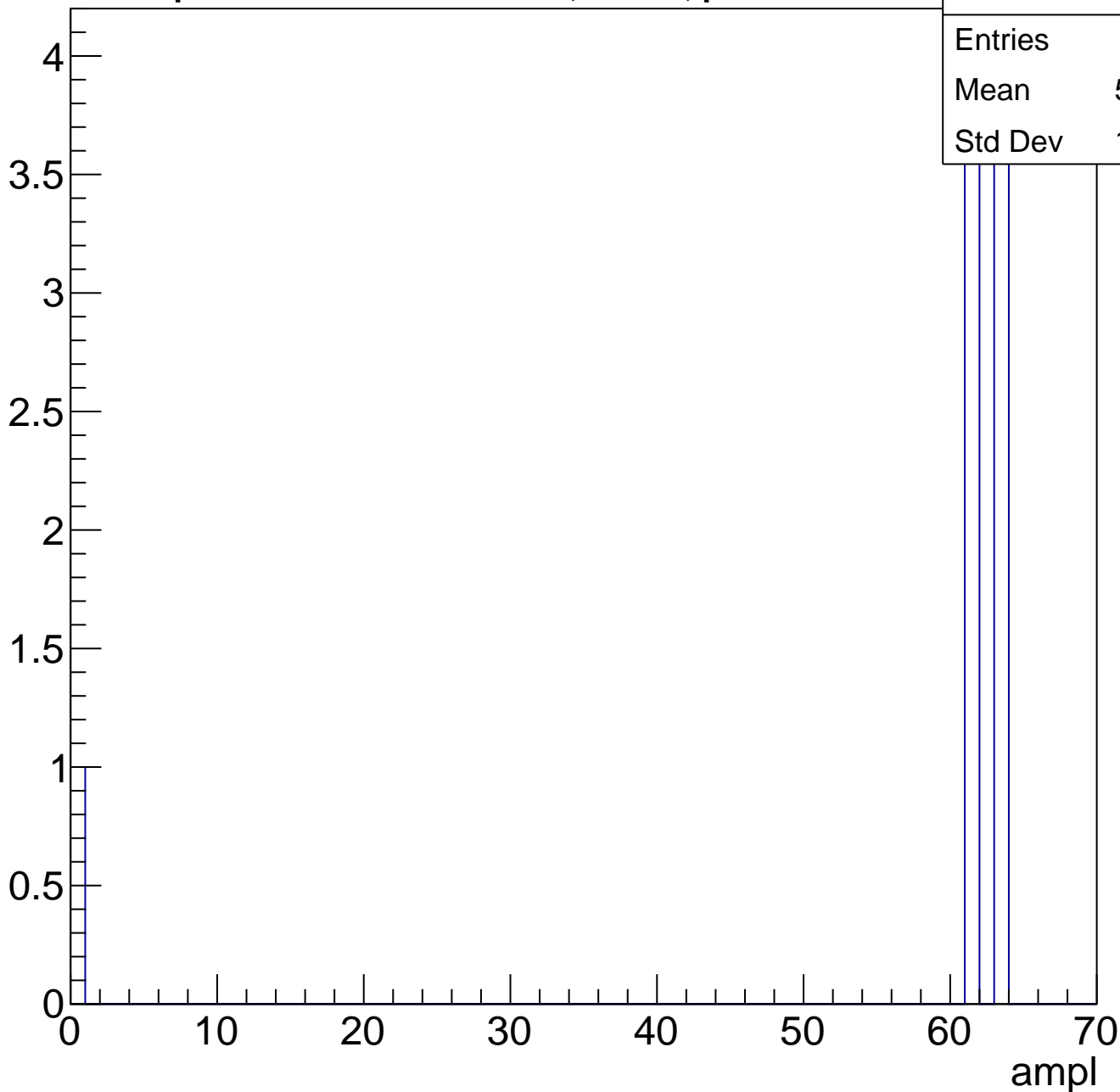
Entries	36
Mean	60.19
Std Dev	2.079



# B1L102S, U8-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch94, adc0

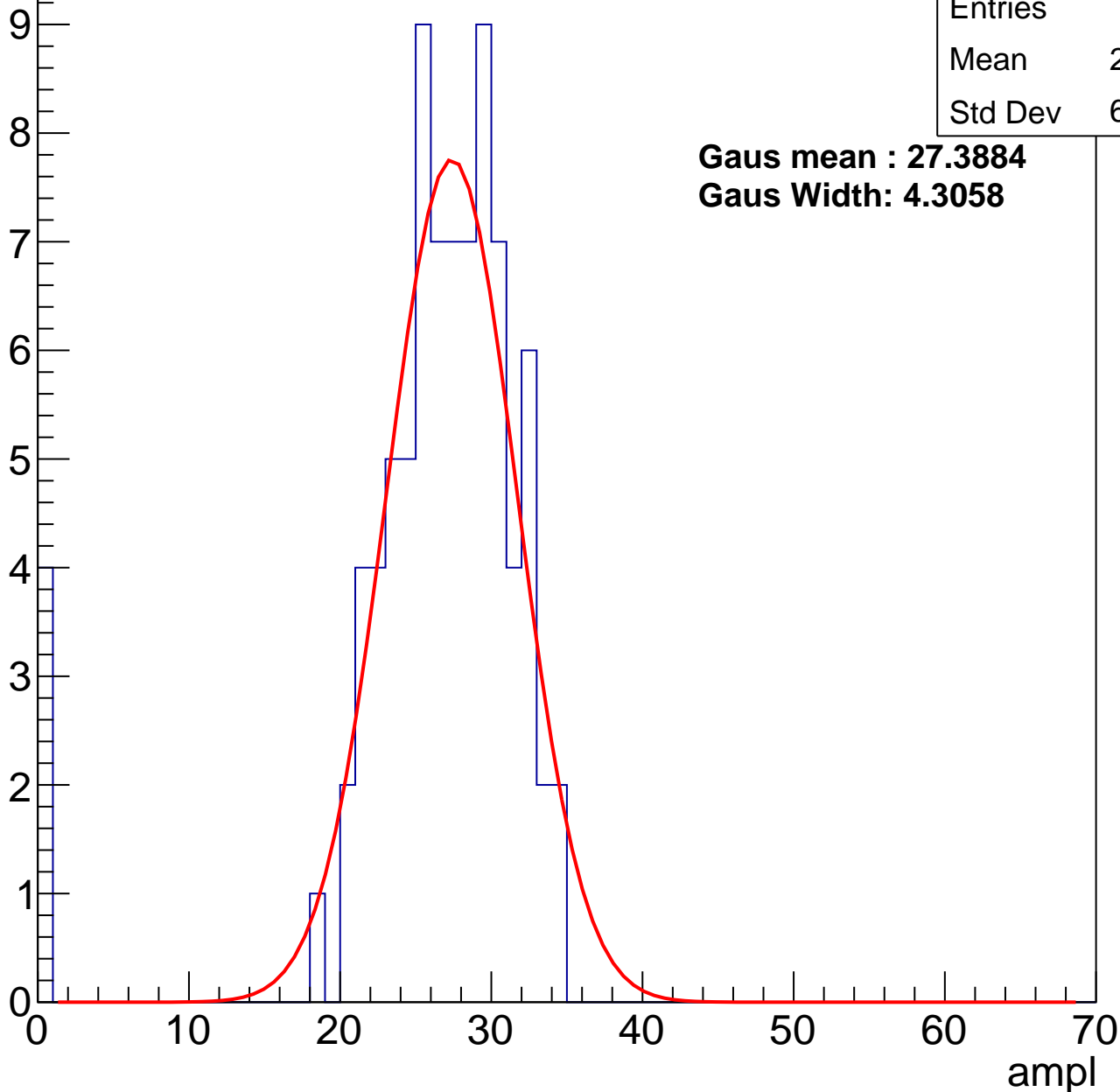
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	85
Mean	25.62
Std Dev	6.718

**Gaus mean : 27.3884**

**Gaus Width: 4.3058**



# B1L102S, U8-ch94, adc1

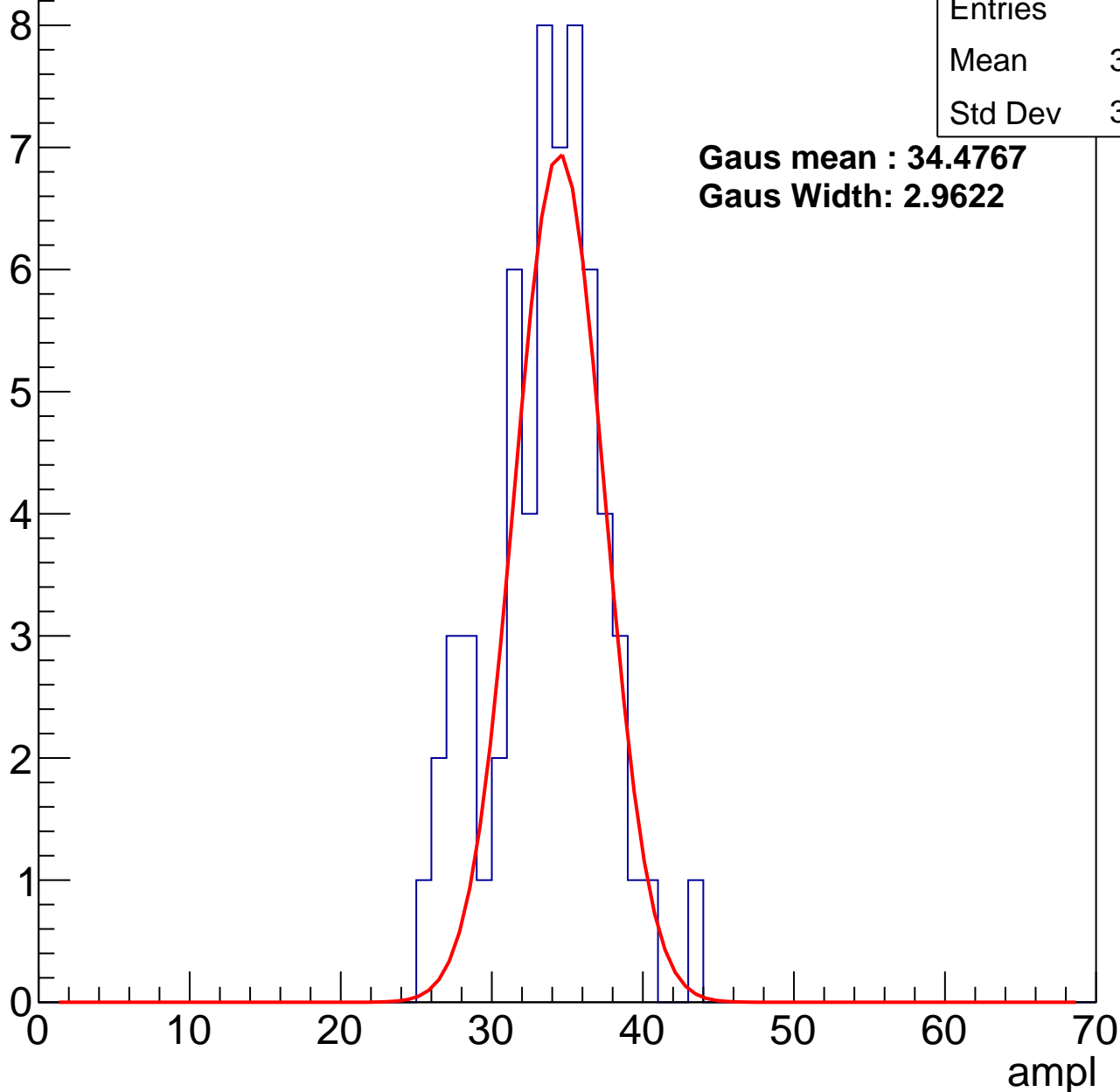
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	33.23
Std Dev	3.668

**Gaus mean : 34.4767**

**Gaus Width: 2.9622**



# B1L102S, U8-ch94, adc2

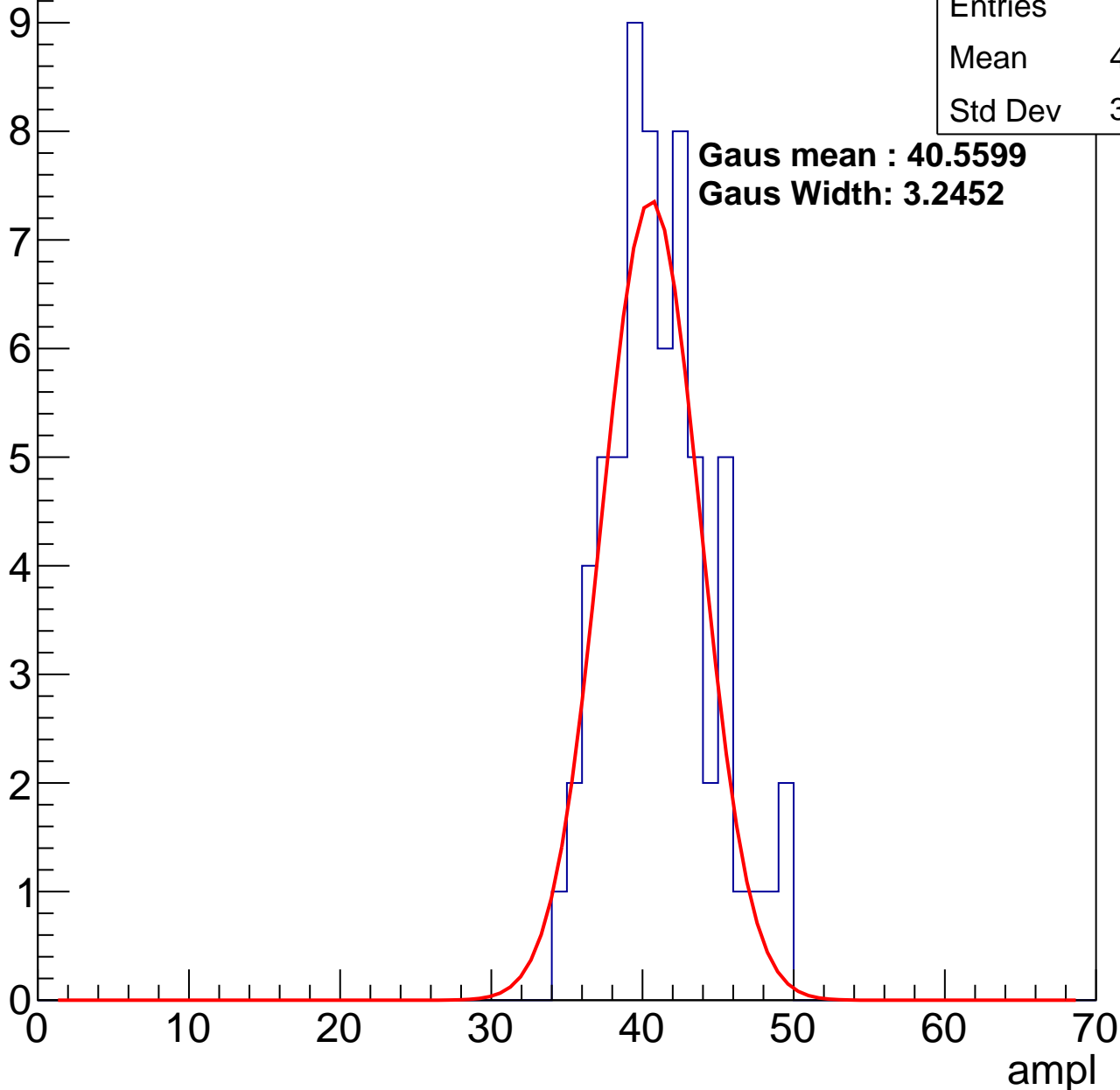
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	40.66
Std Dev	3.389

**Gaus mean : 40.5599**

**Gaus Width: 3.2452**

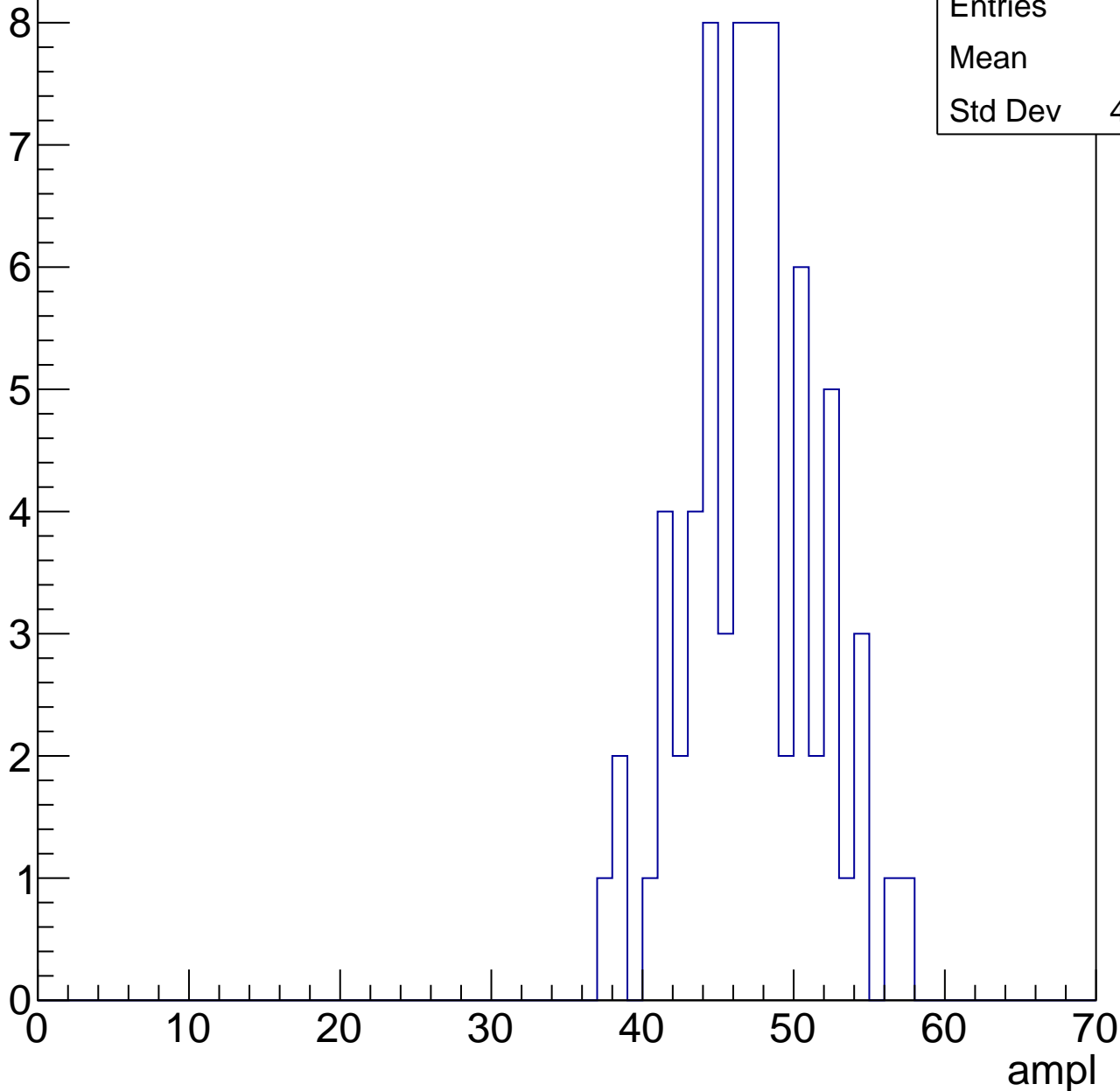


# B1L102S, U8-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	46.8
Std Dev	4.224

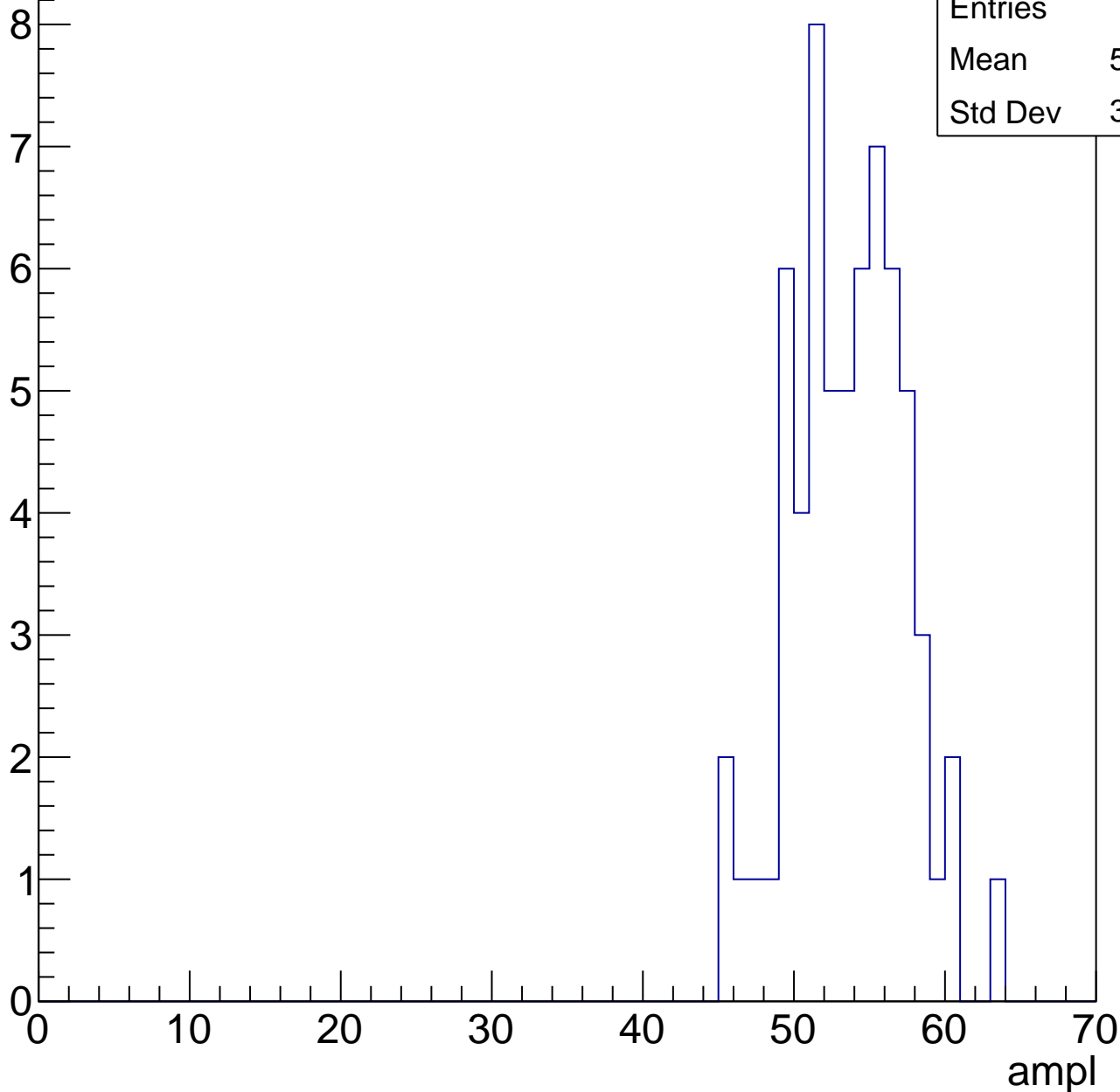


# B1L102S, U8-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

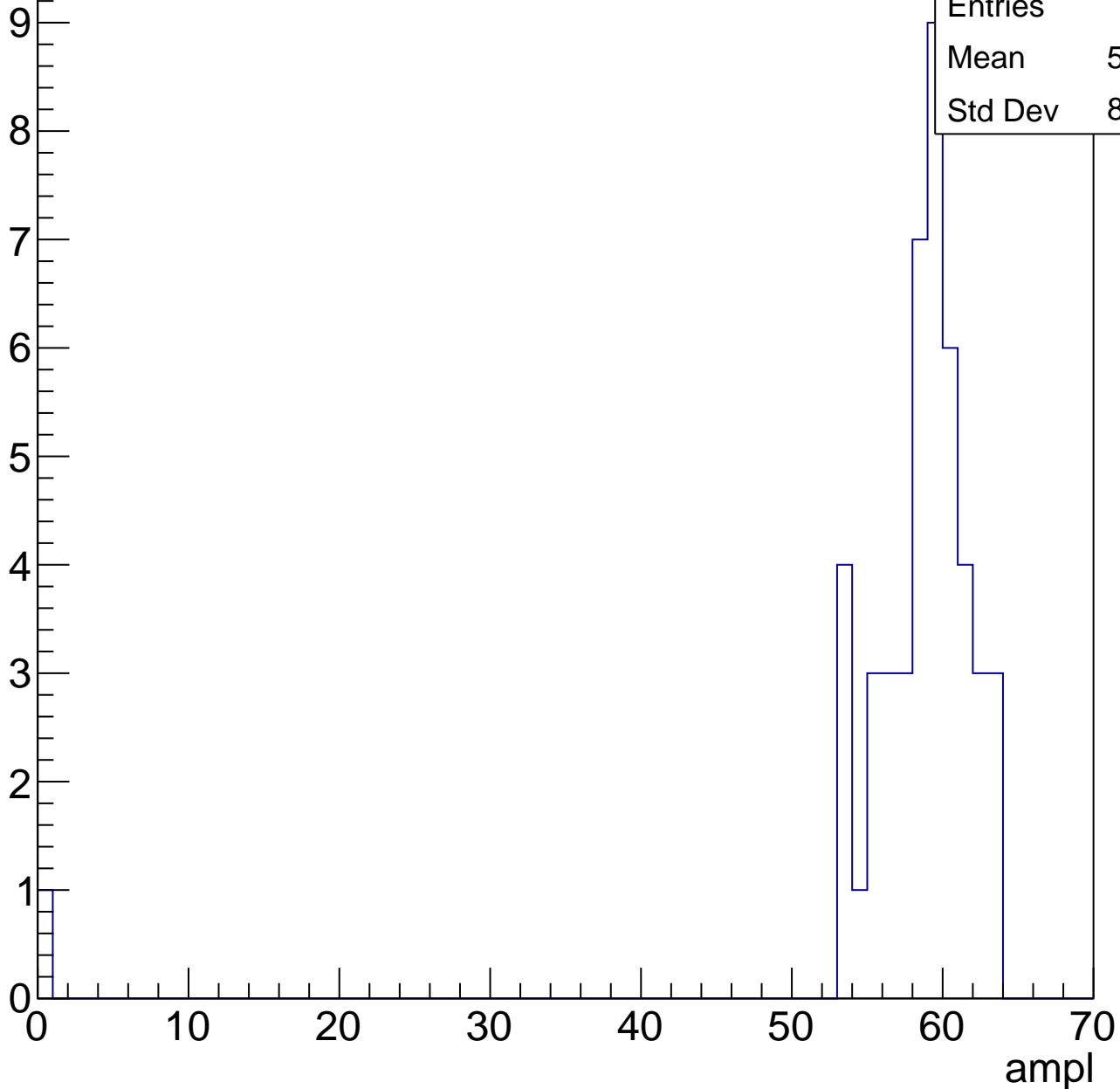
Entries	64
Mean	53.19
Std Dev	3.712



# B1L102S, U8-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

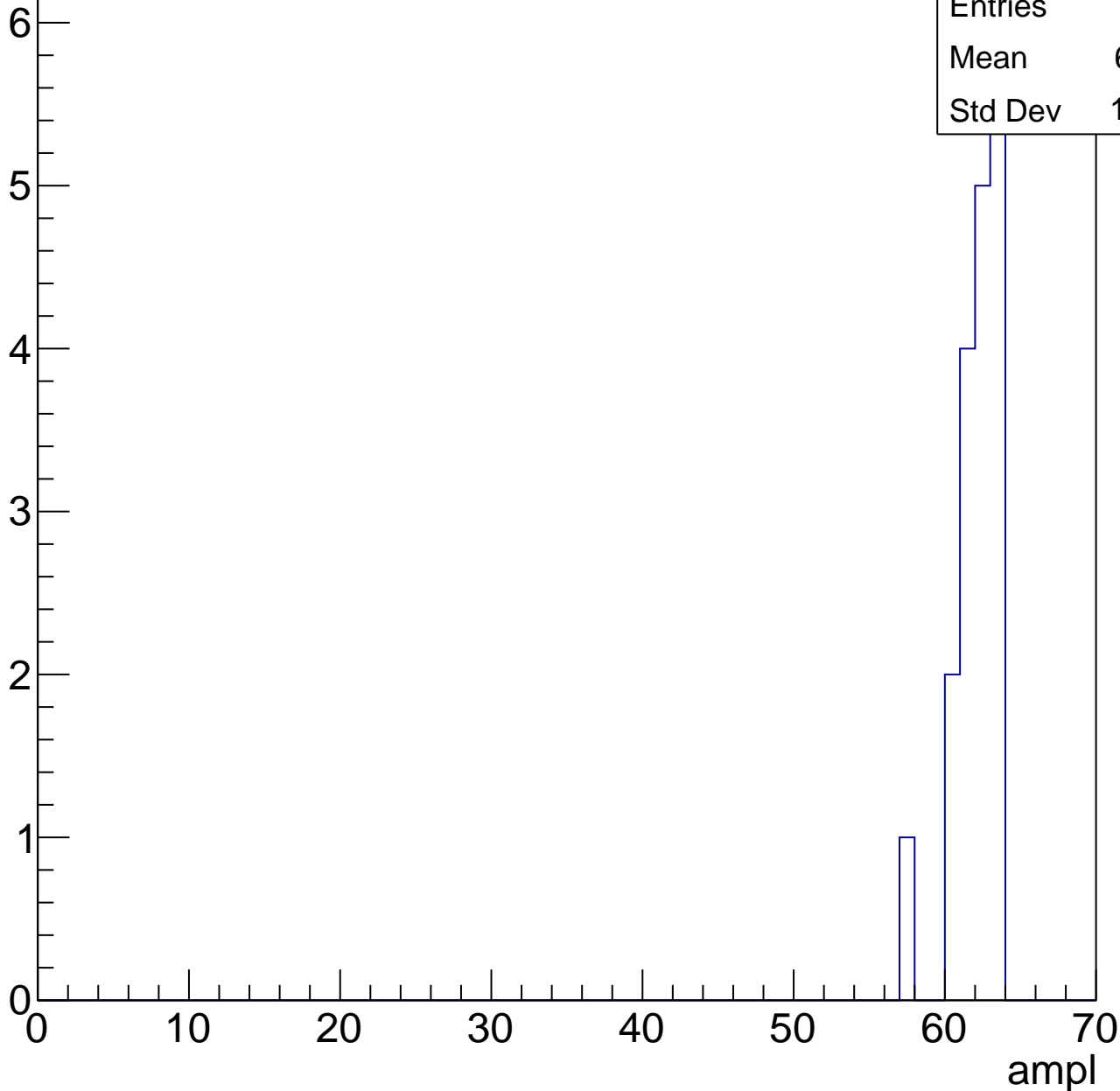


# B1L102S, U8-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	18
Mean	61.61
Std Dev	1.496

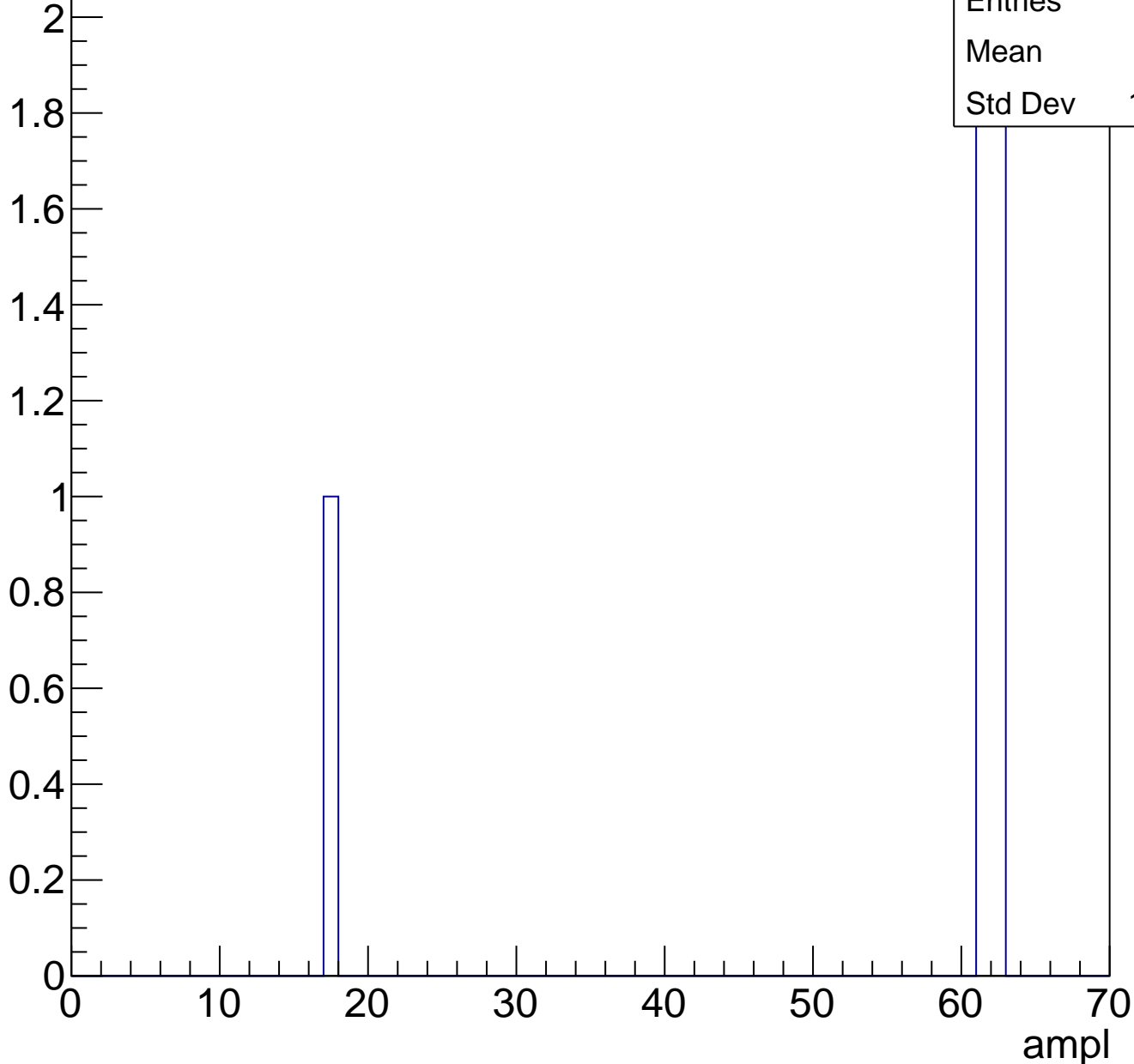




# B1L102S, U8-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch95, adc0

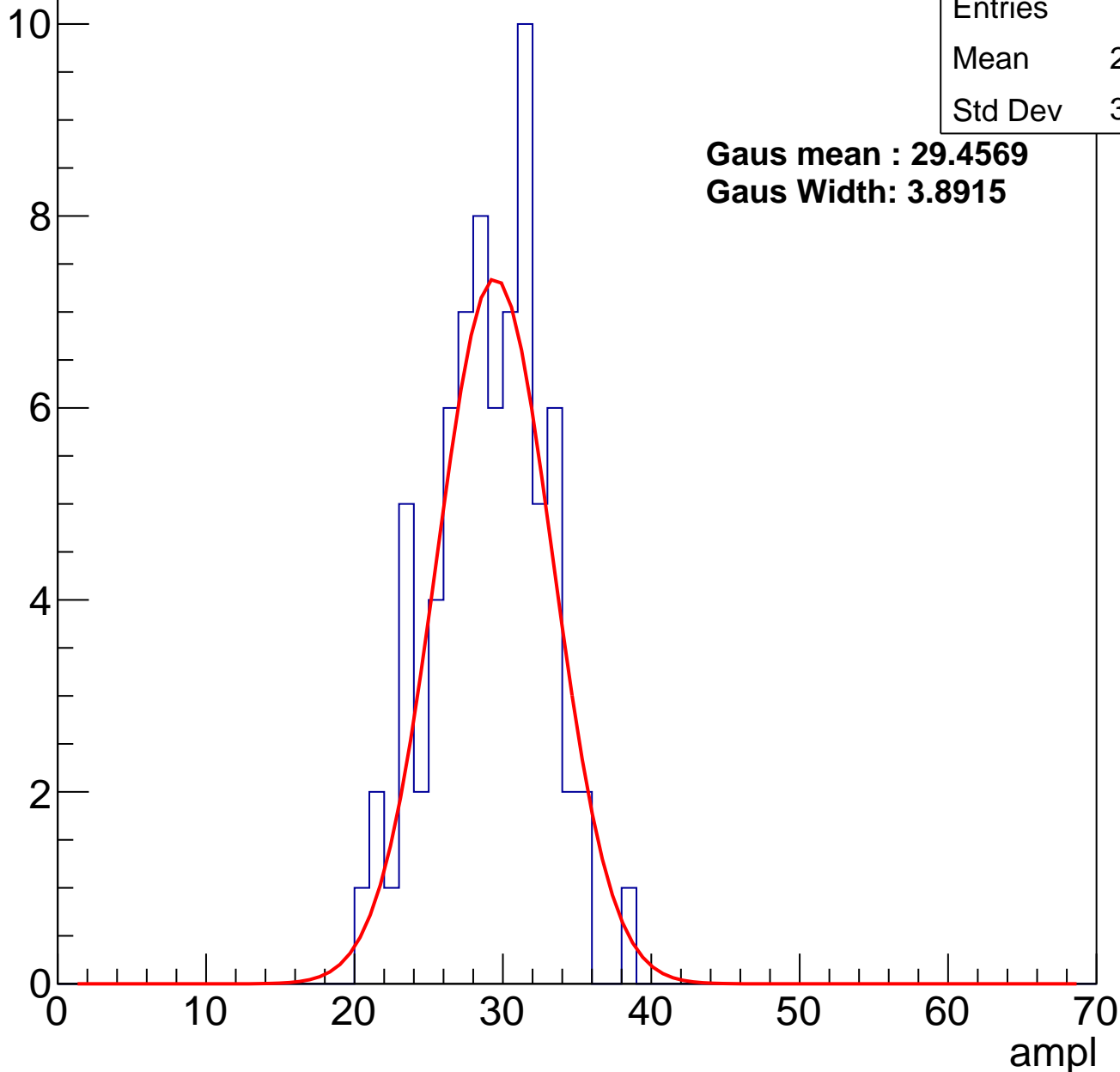
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	75
Mean	28.59
Std Dev	3.688

**Gaus mean : 29.4569**

**Gaus Width: 3.8915**

Entry



# B1L102S, U8-ch95, adc1

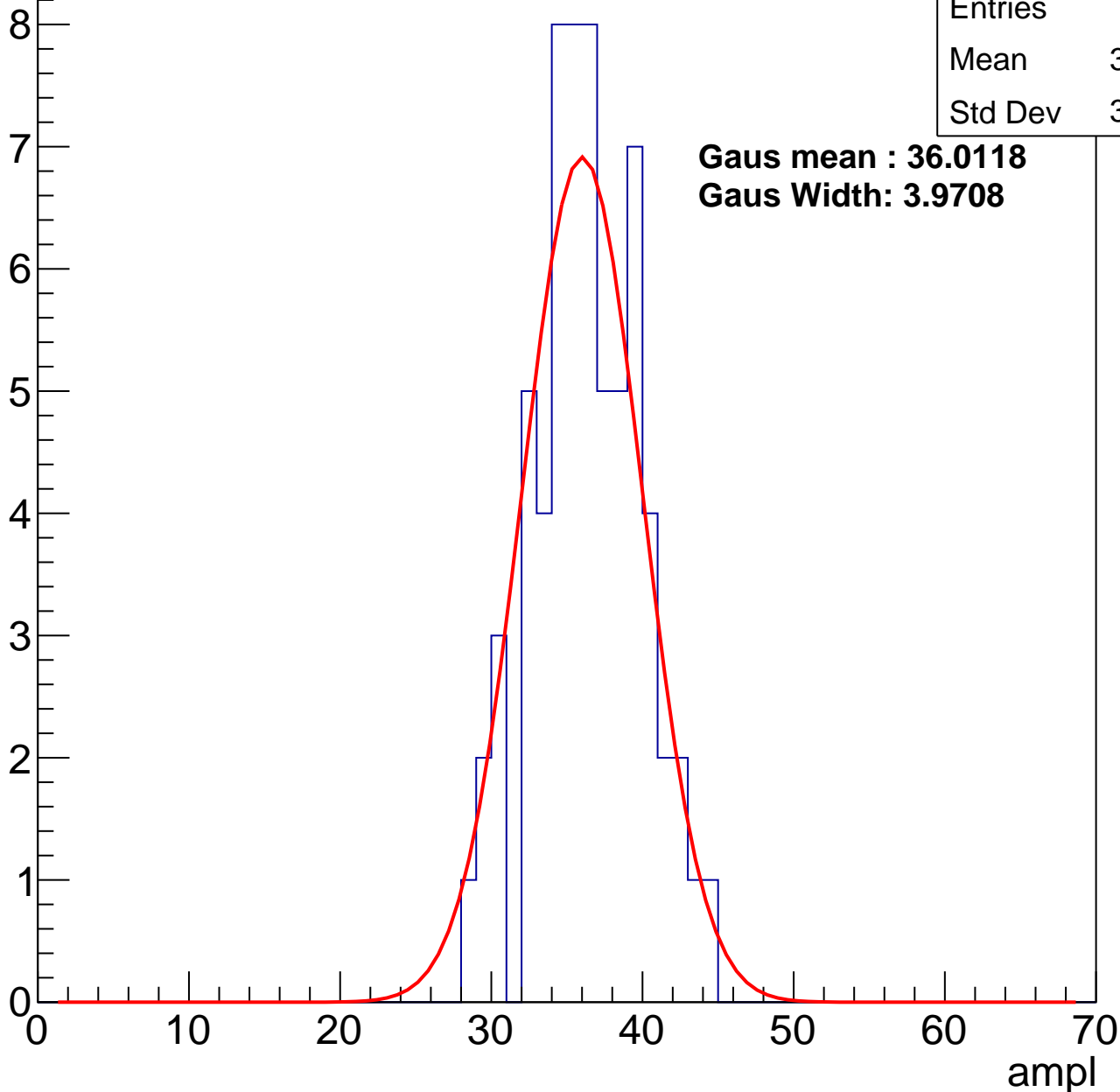
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	35.89
Std Dev	3.508

**Gaus mean : 36.0118**

**Gaus Width: 3.9708**



# B1L102S, U8-ch95, adc2

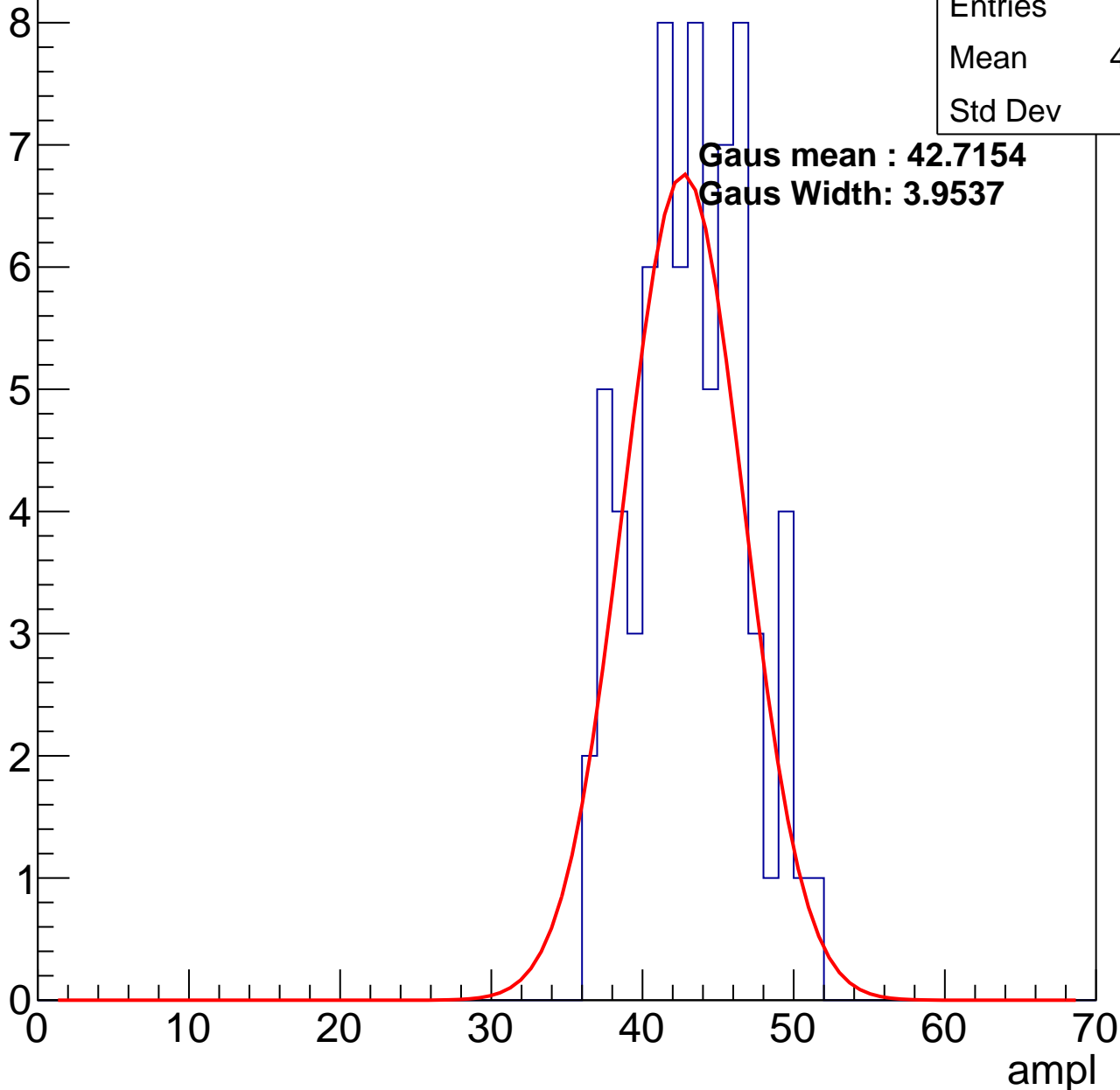
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	42.76
Std Dev	3.63

**Gaus mean : 42.7154**

**Gaus Width: 3.9537**

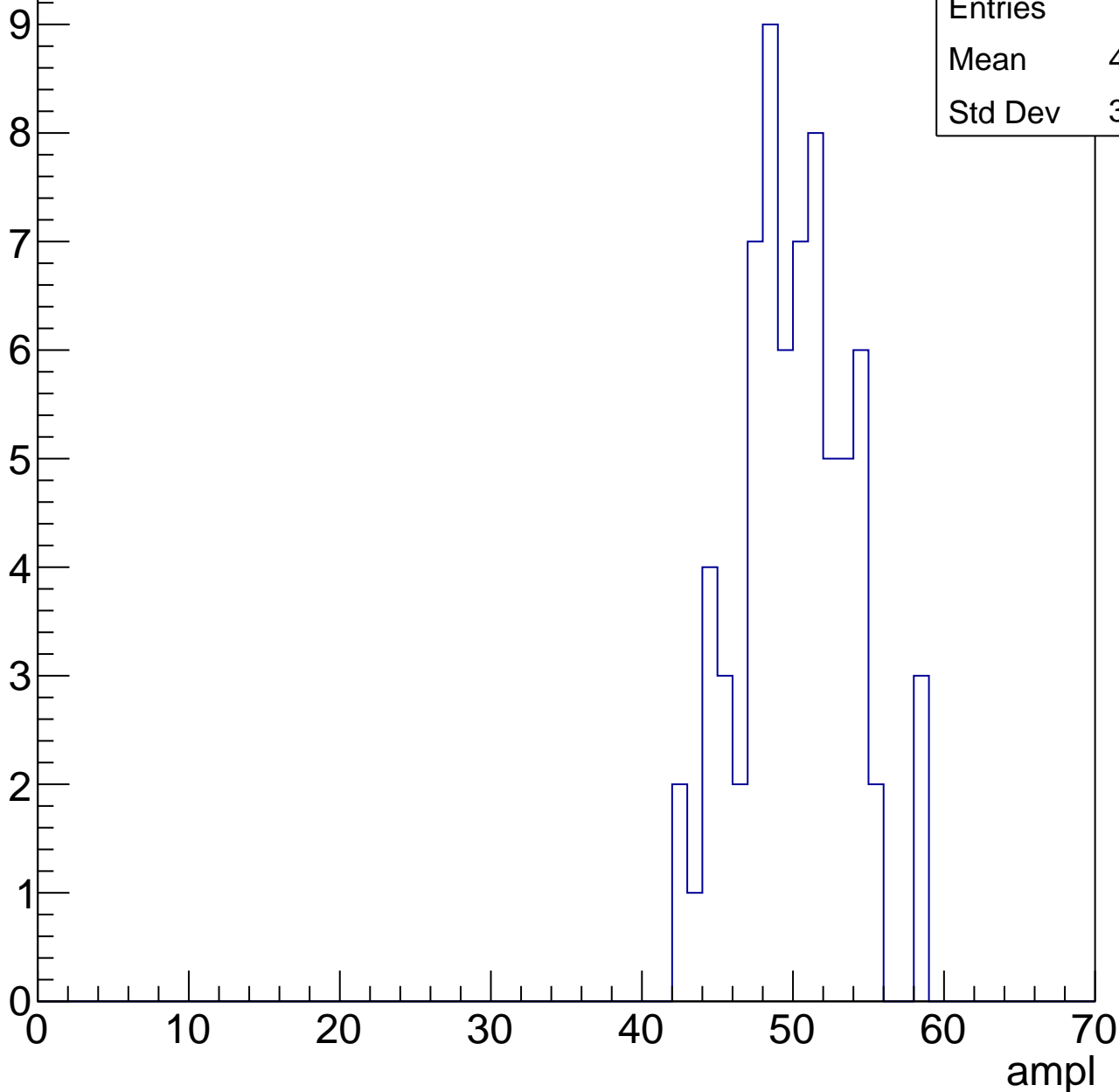


# B1L102S, U8-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	49.66
Std Dev	3.656

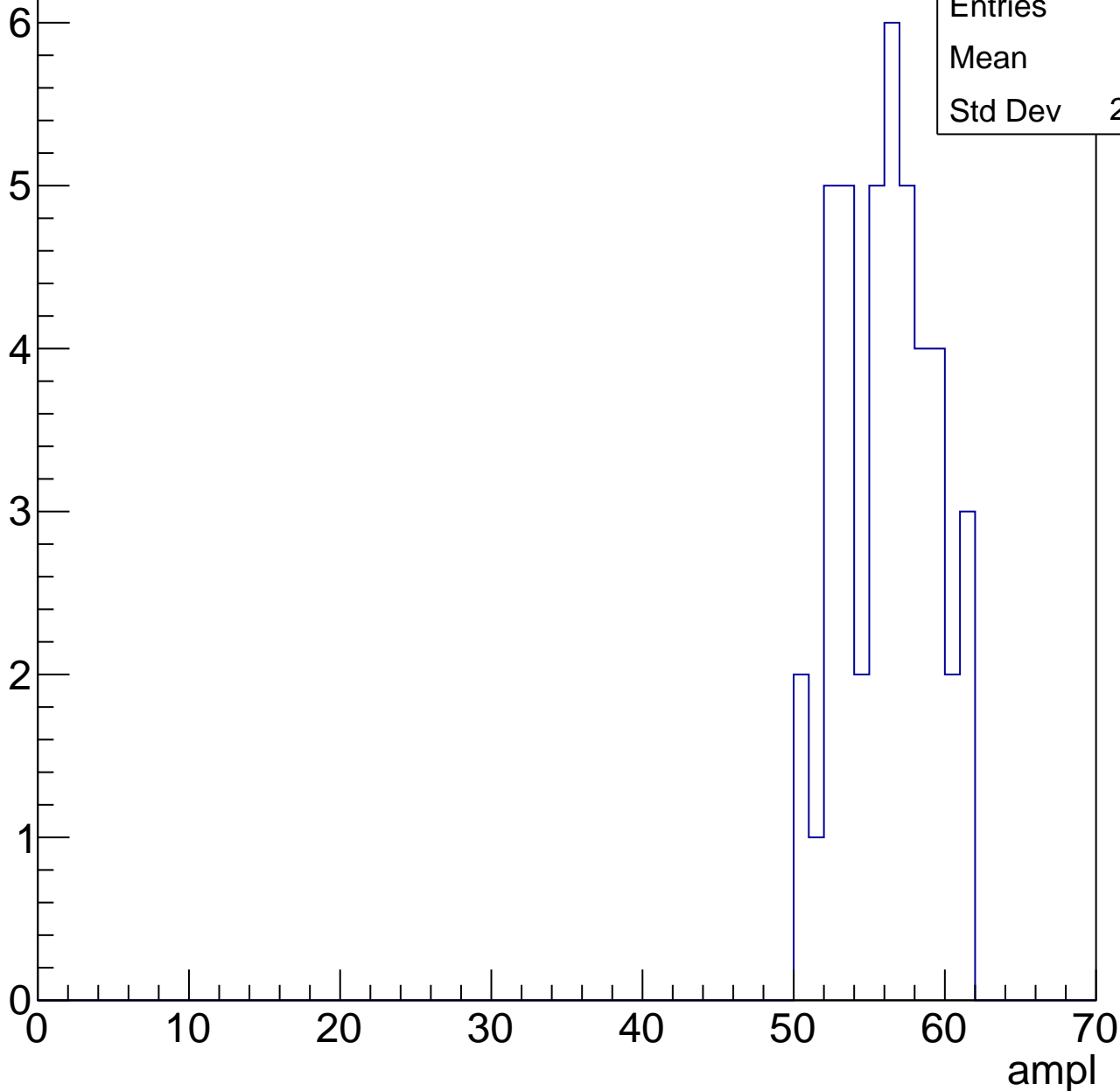


# B1L102S, U8-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

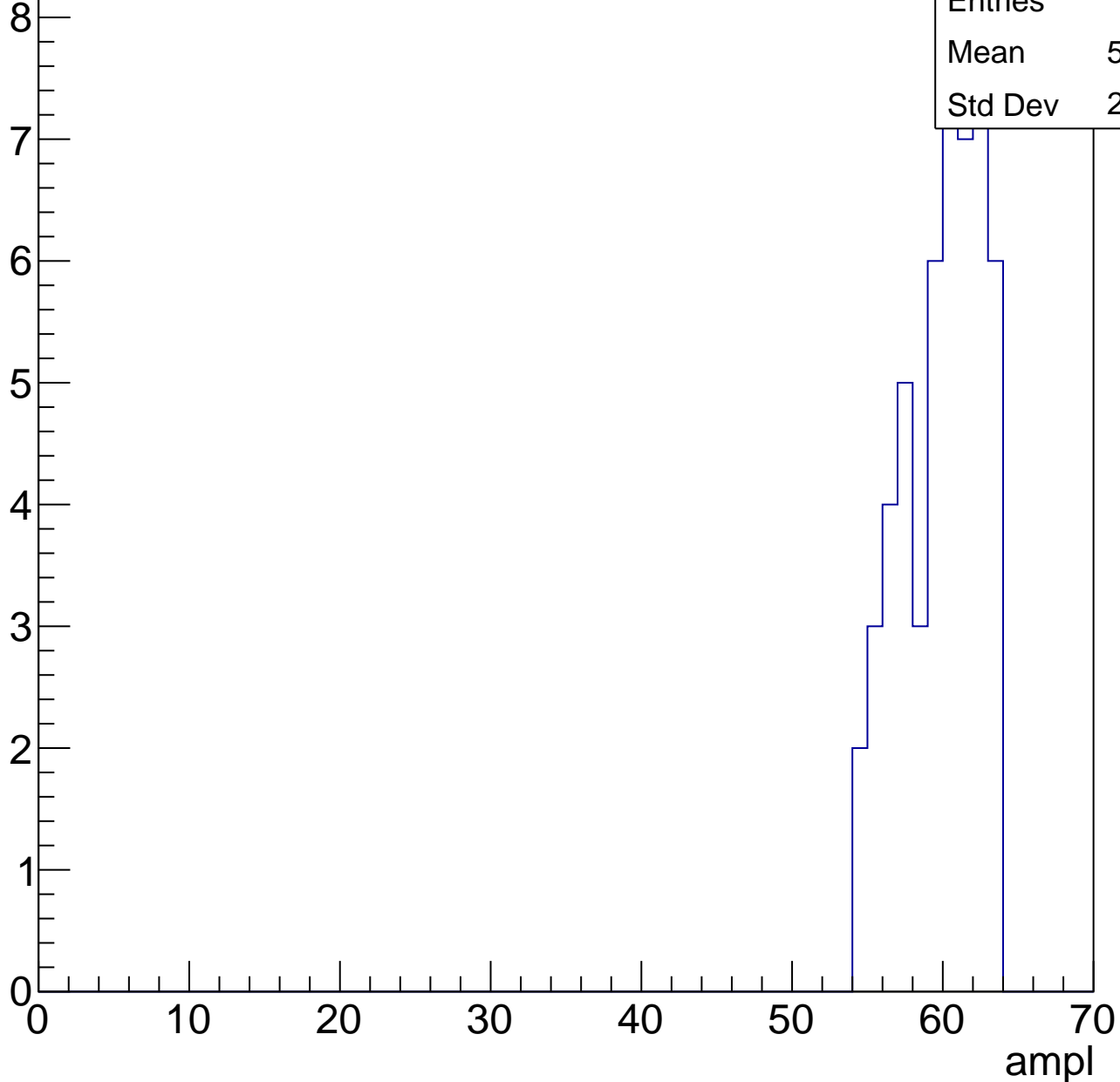
Entries	44
Mean	55.7
Std Dev	2.997



# B1L102S, U8-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

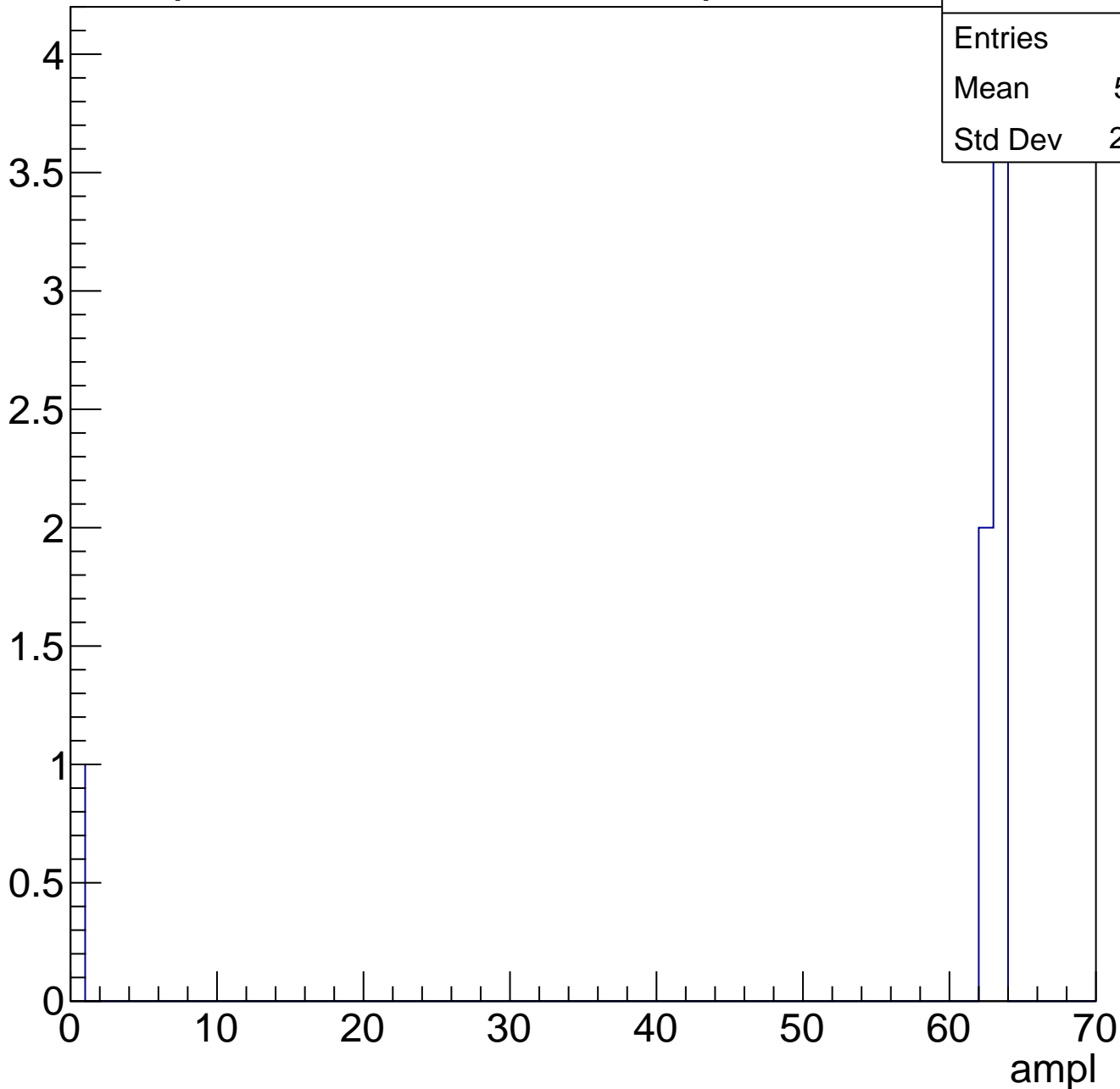
Entry



# B1L102S, U8-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch96, adc0

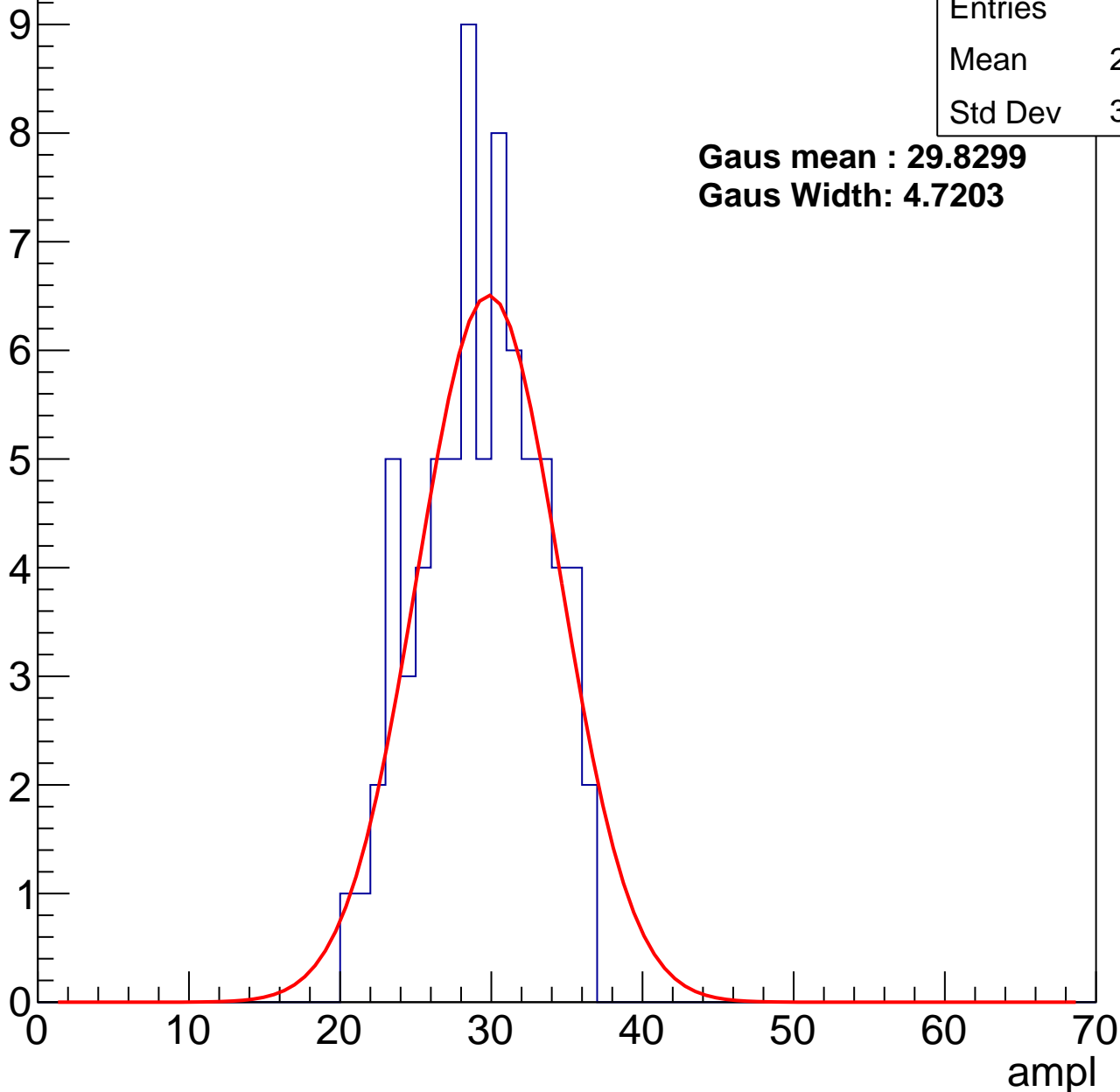
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	28.82
Std Dev	3.912

**Gaus mean : 29.8299**

**Gaus Width: 4.7203**



# B1L102S, U8-ch96, adc1

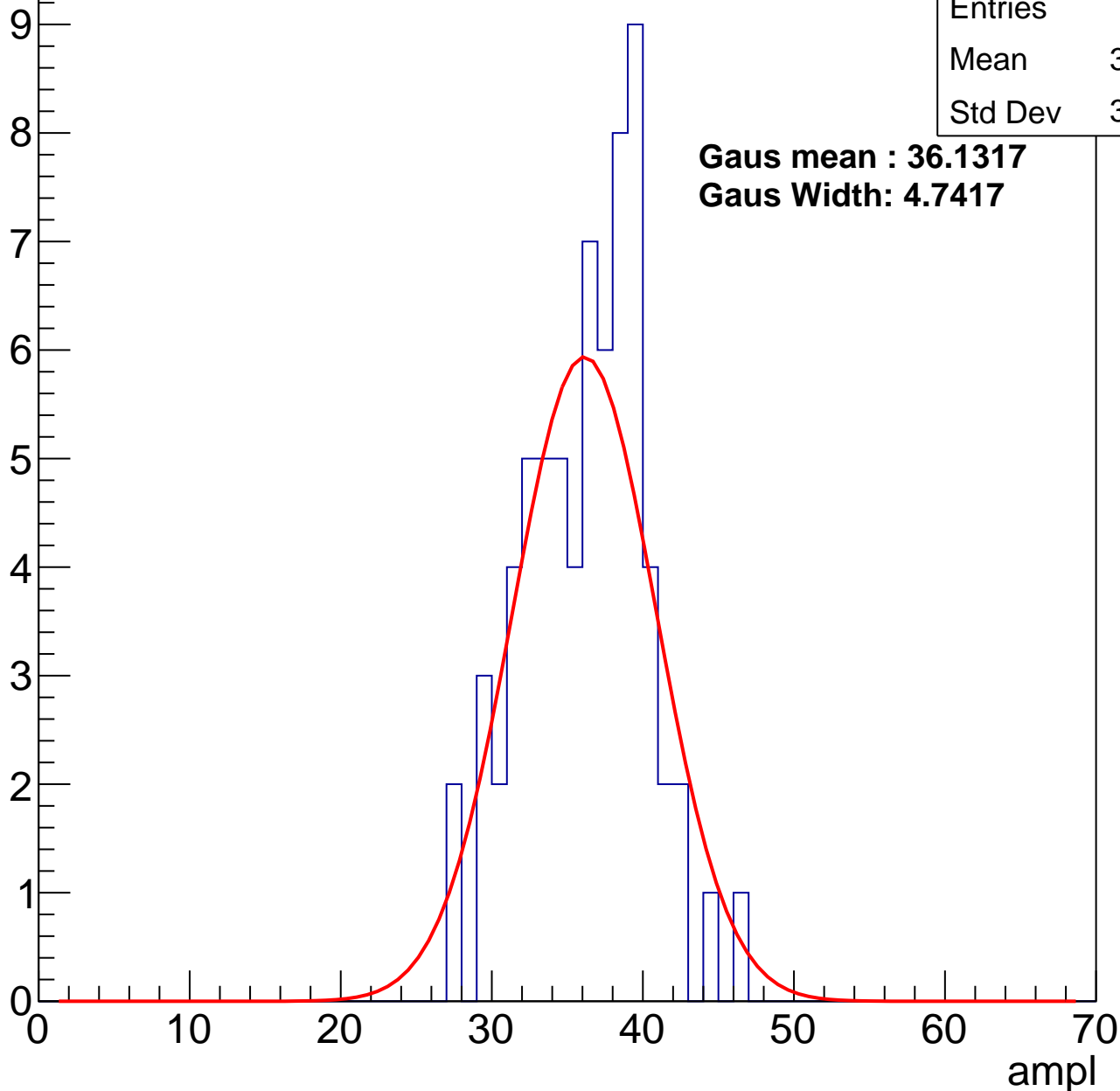
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	35.79
Std Dev	3.957

**Gaus mean : 36.1317**

**Gaus Width: 4.7417**



# B1L102S, U8-ch96, adc2

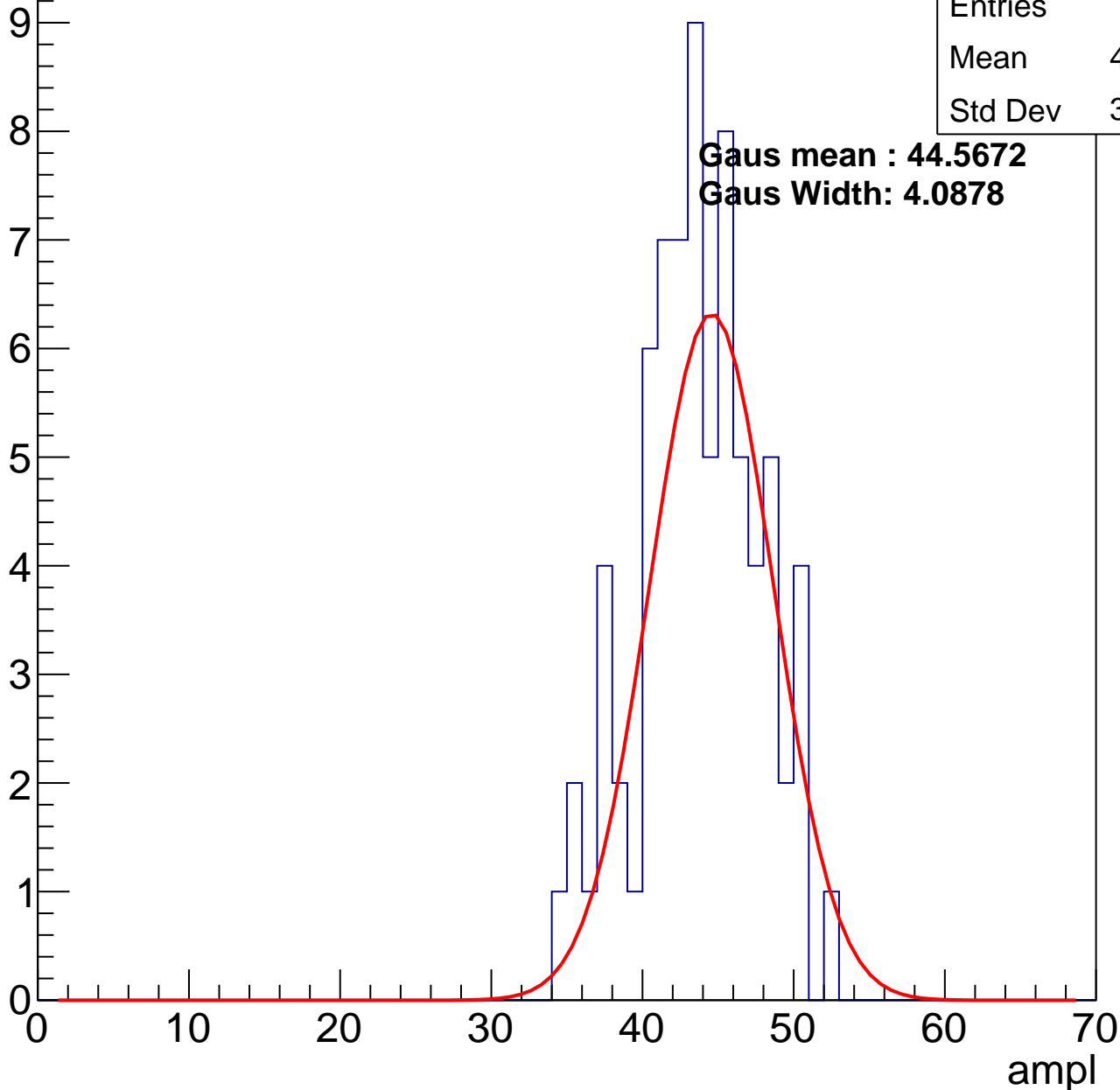
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	43.23
Std Dev	3.982

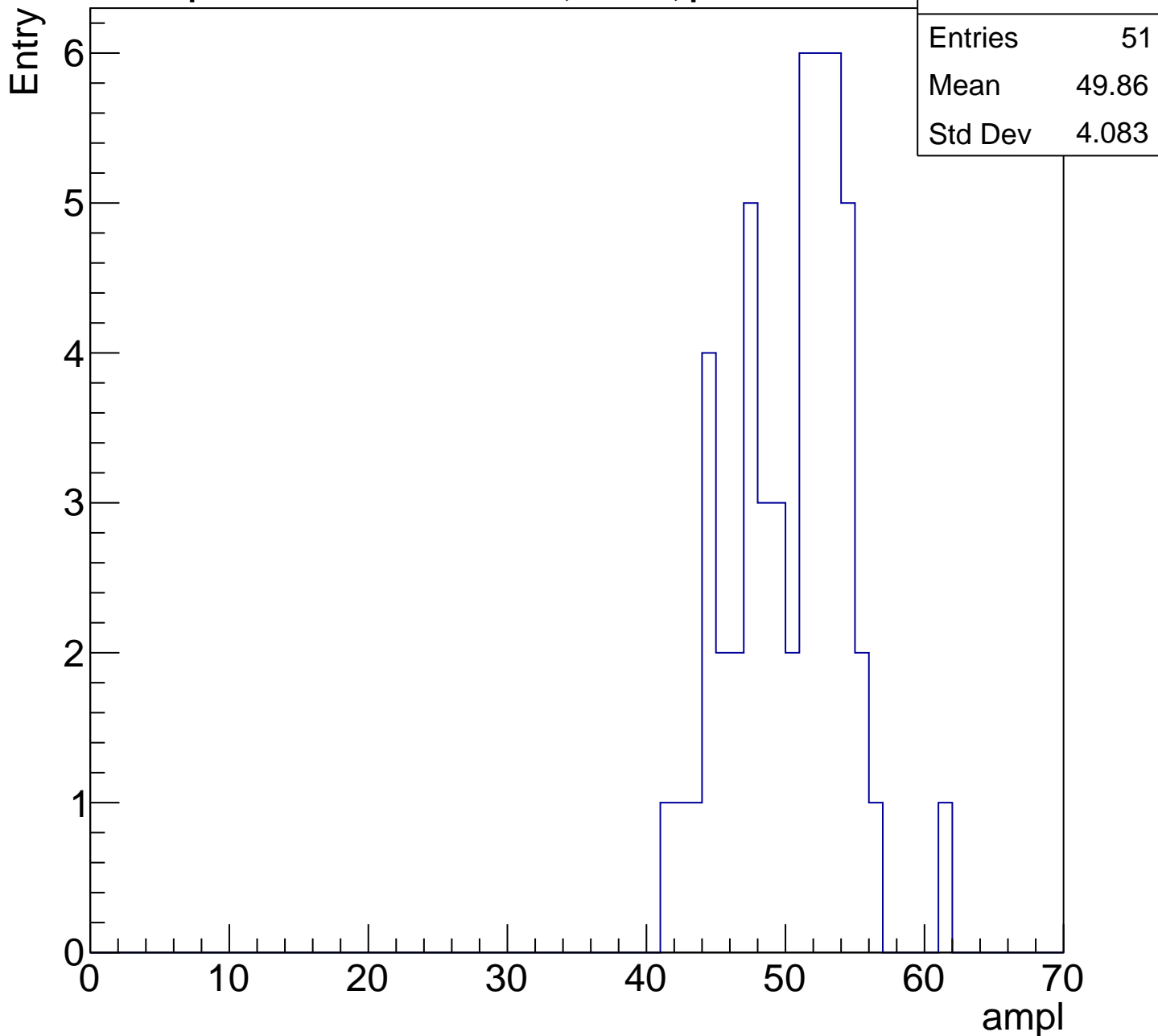
**Gaus mean : 44.5672**

**Gaus Width: 4.0878**



# B1L102S, U8-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

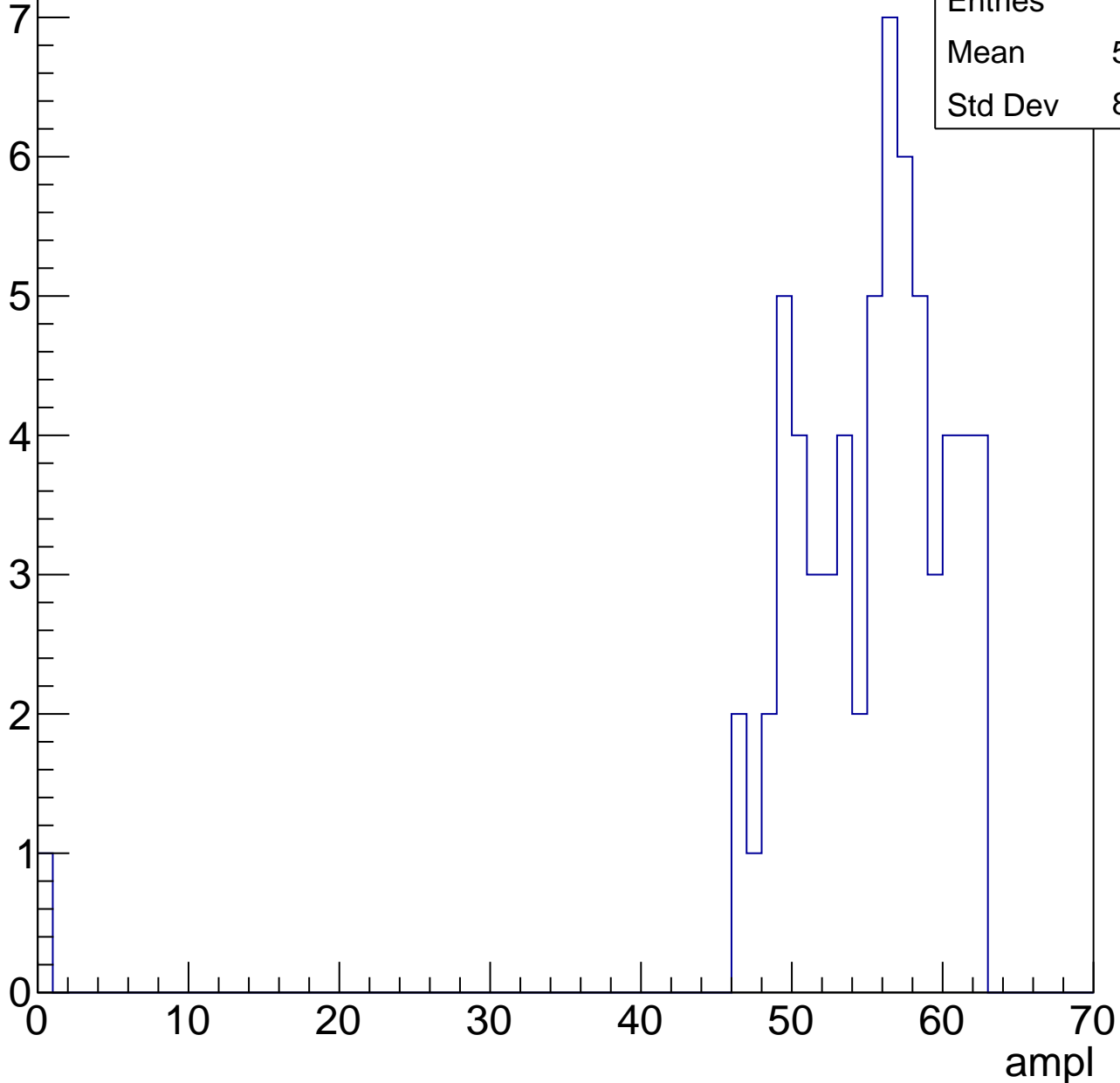


# B1L102S, U8-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

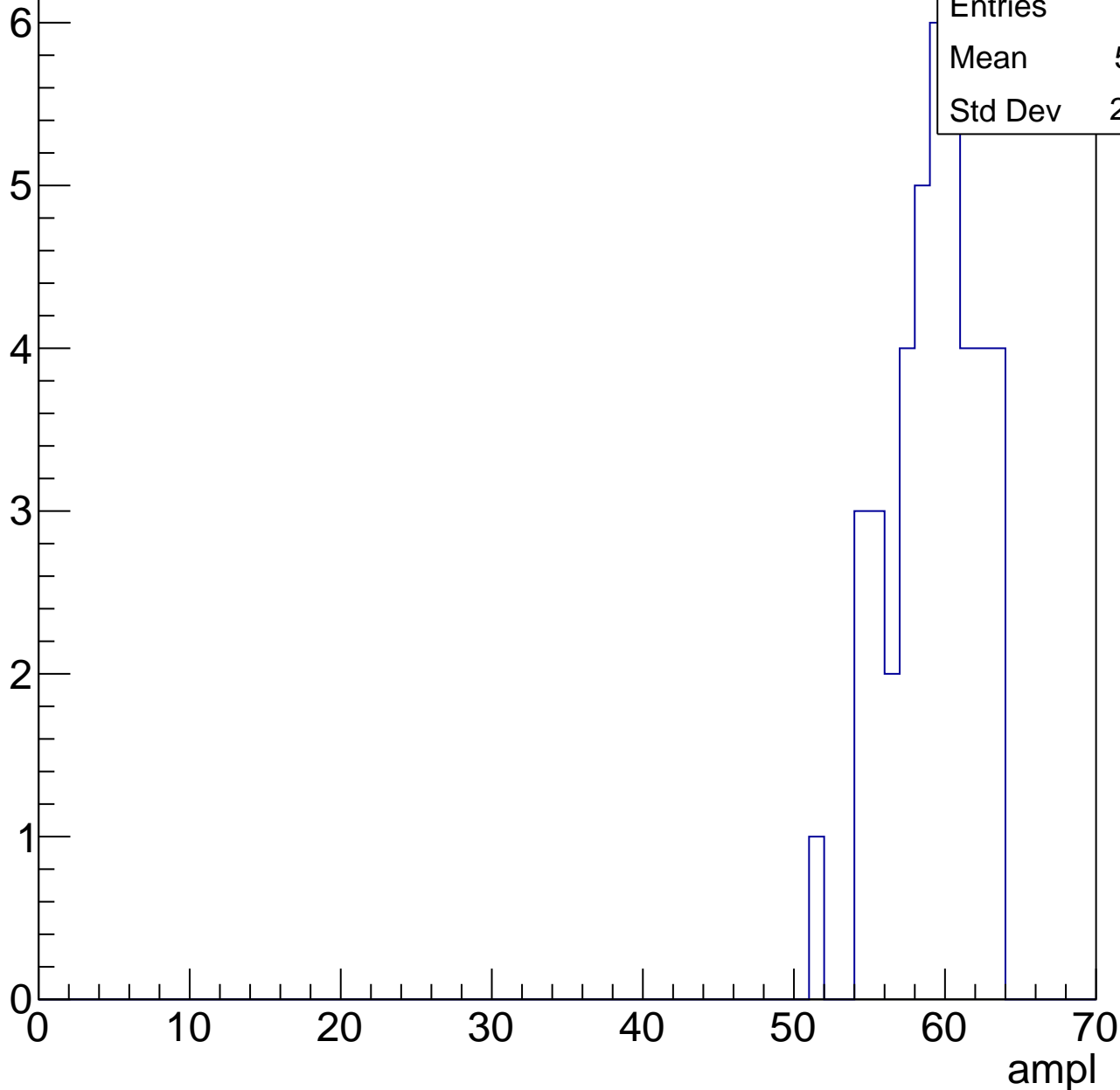
Entries	65
Mean	54.11
Std Dev	8.071



# B1L102S, U8-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

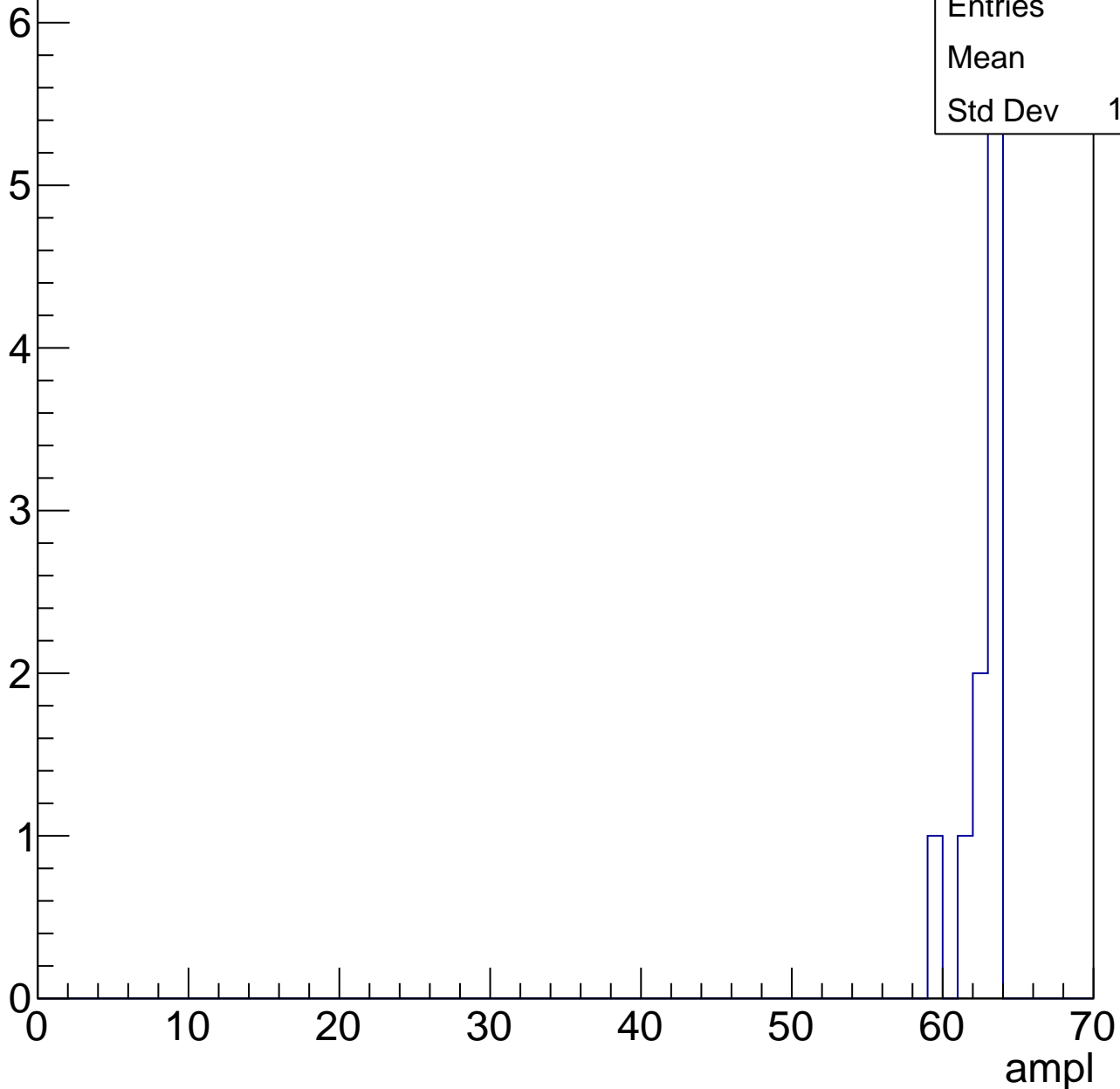


# B1L102S, U8-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	10
Mean	62.2
Std Dev	1.249





# B1L102S, U8-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U8-ch97, adc0

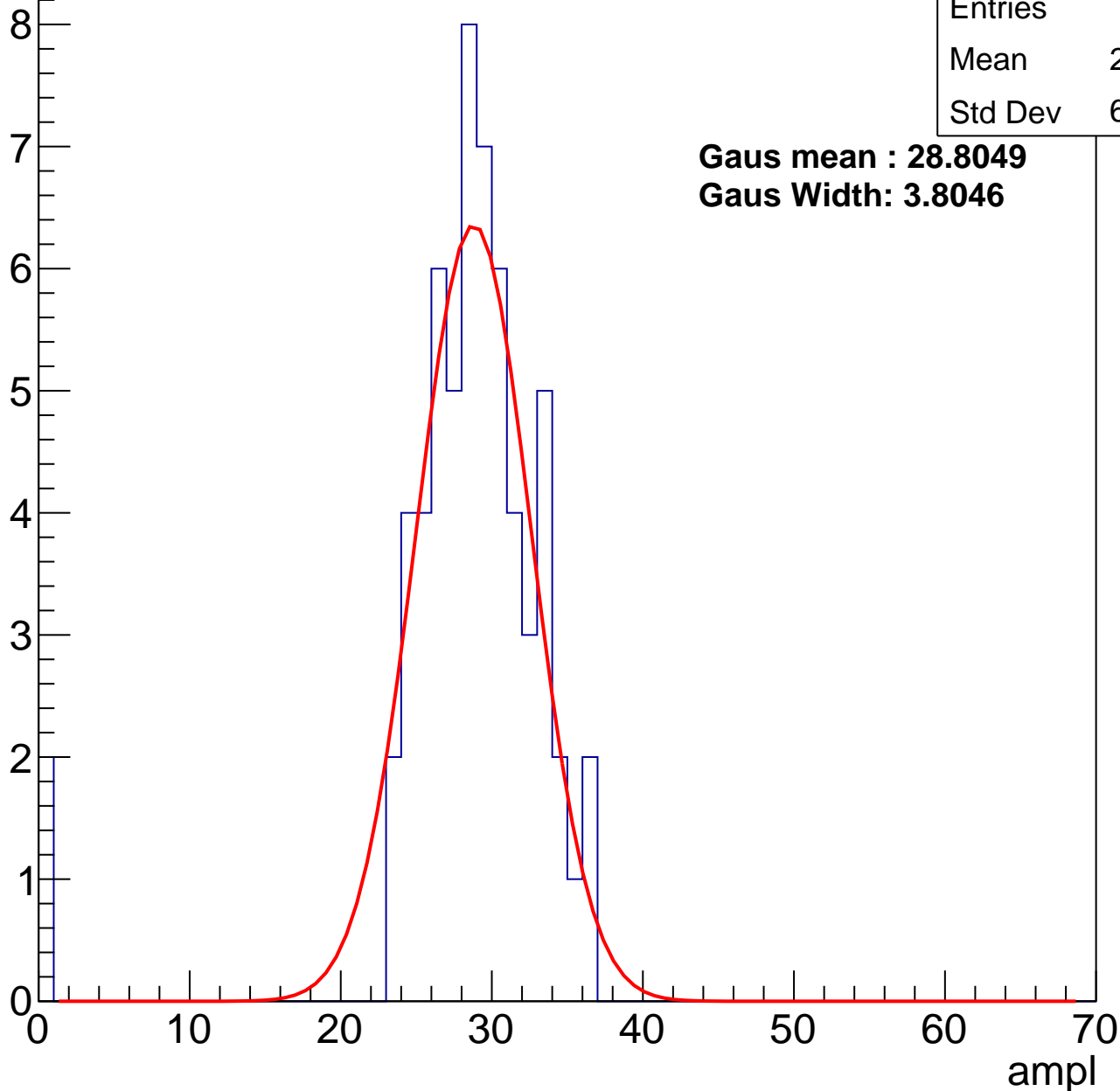
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	27.87
Std Dev	6.053

**Gaus mean : 28.8049**

**Gaus Width: 3.8046**



# B1L102S, U8-ch97, adc1

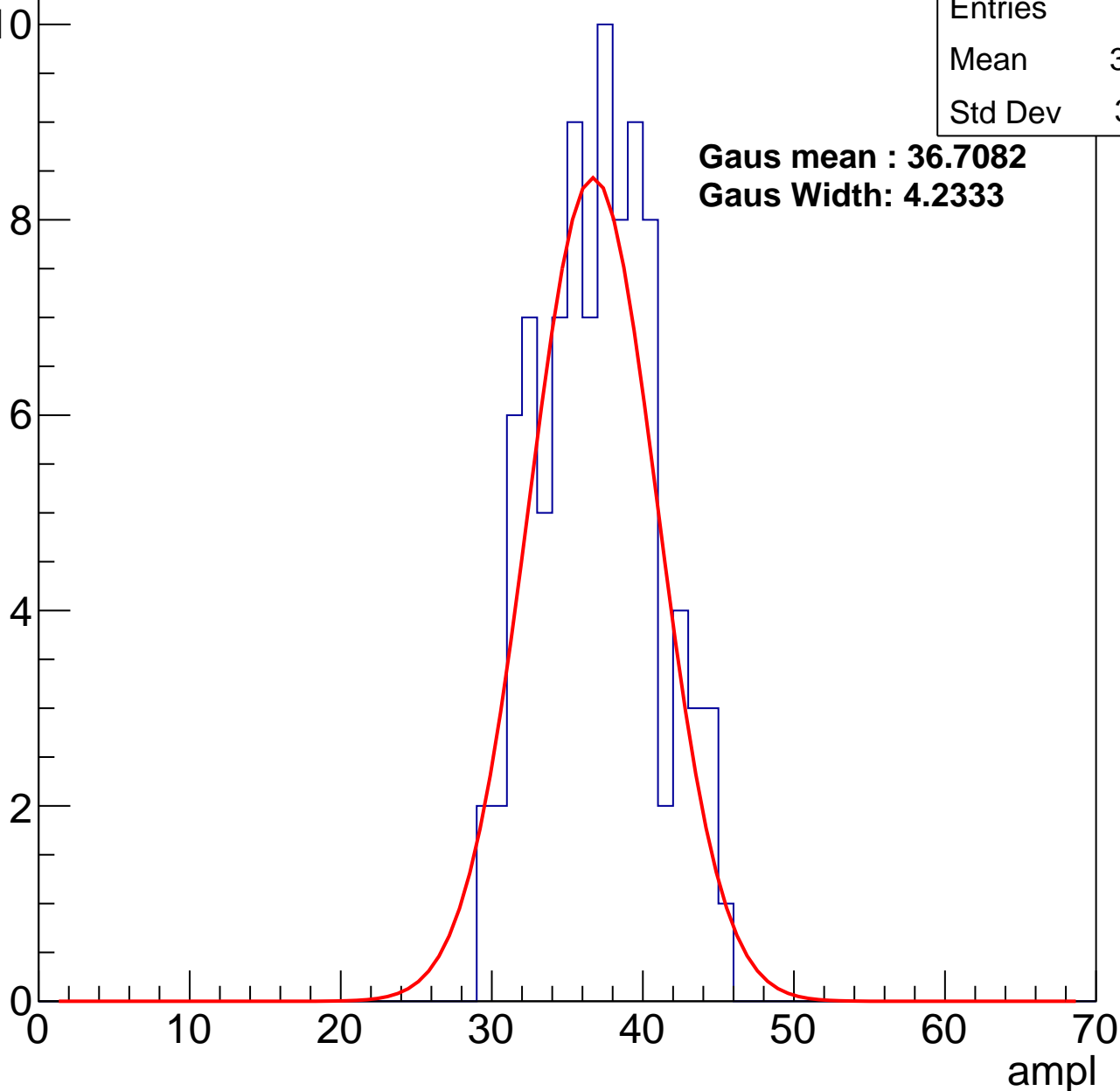
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	93
Mean	36.55
Std Dev	3.811

**Gaus mean : 36.7082**

**Gaus Width: 4.2333**



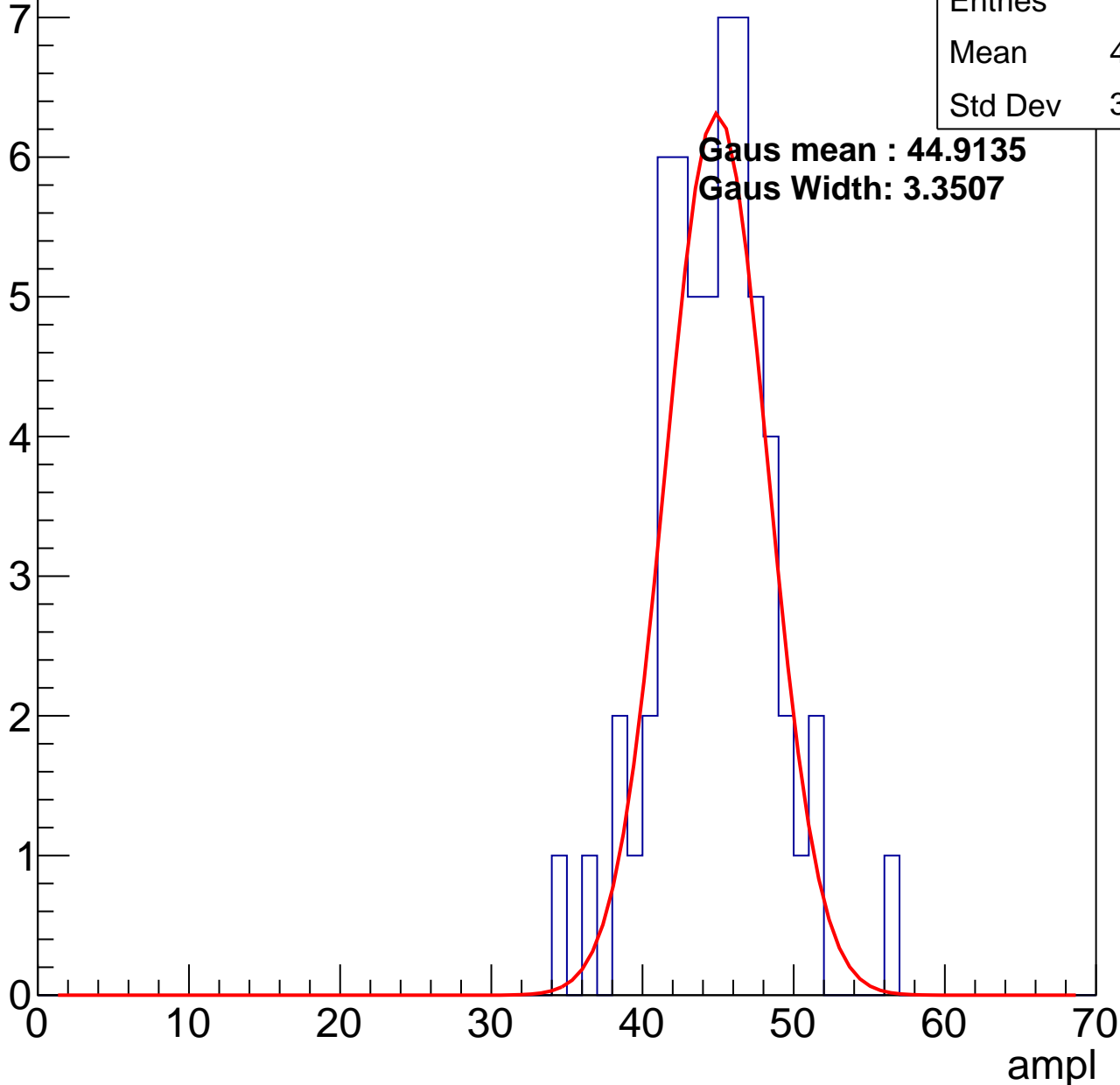
# B1L102S, U8-ch97, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	44.28
Std Dev	3.814

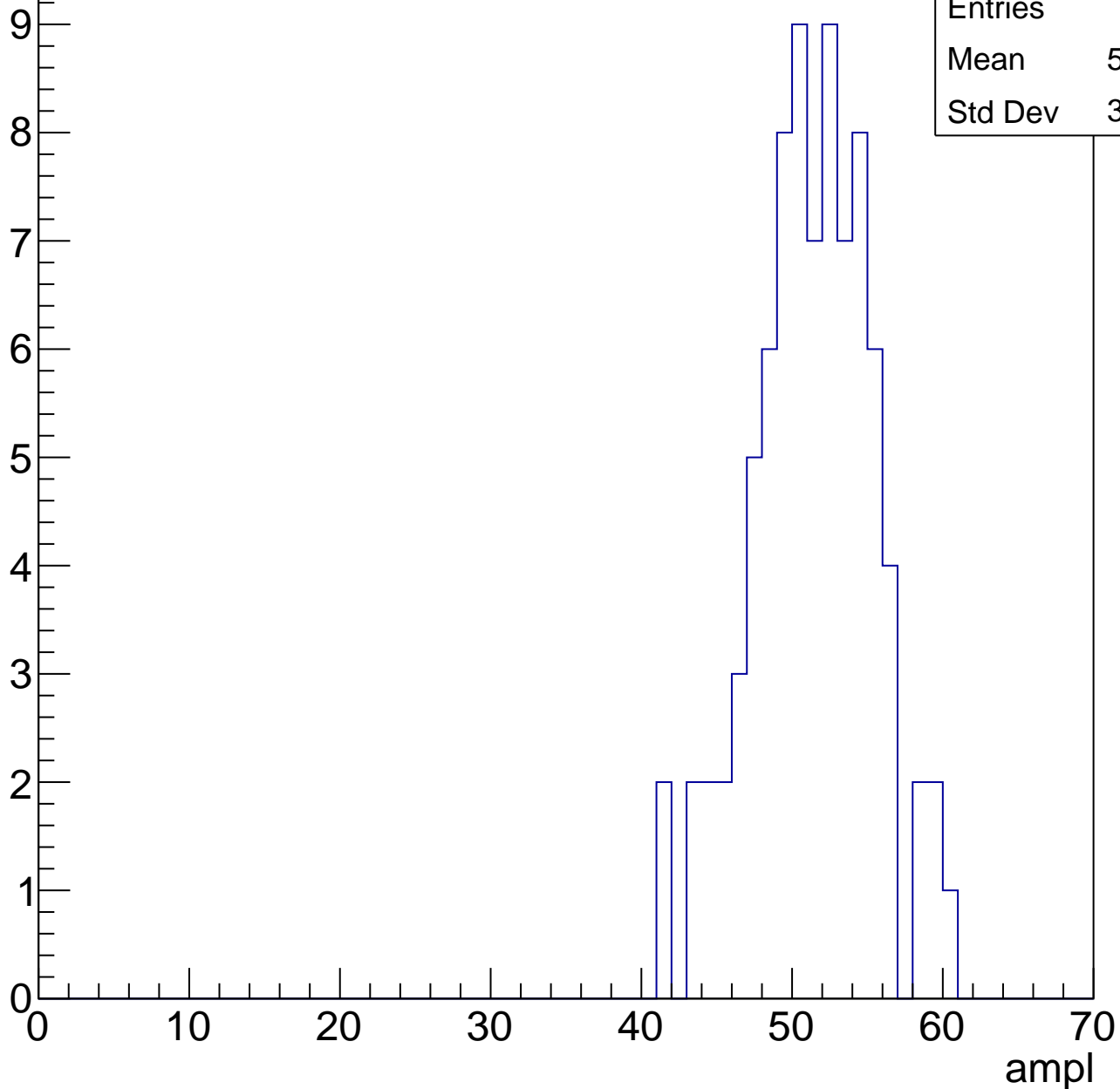
**Gaus mean : 44.9135**  
**Gaus Width: 3.3507**



# B1L102S, U8-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



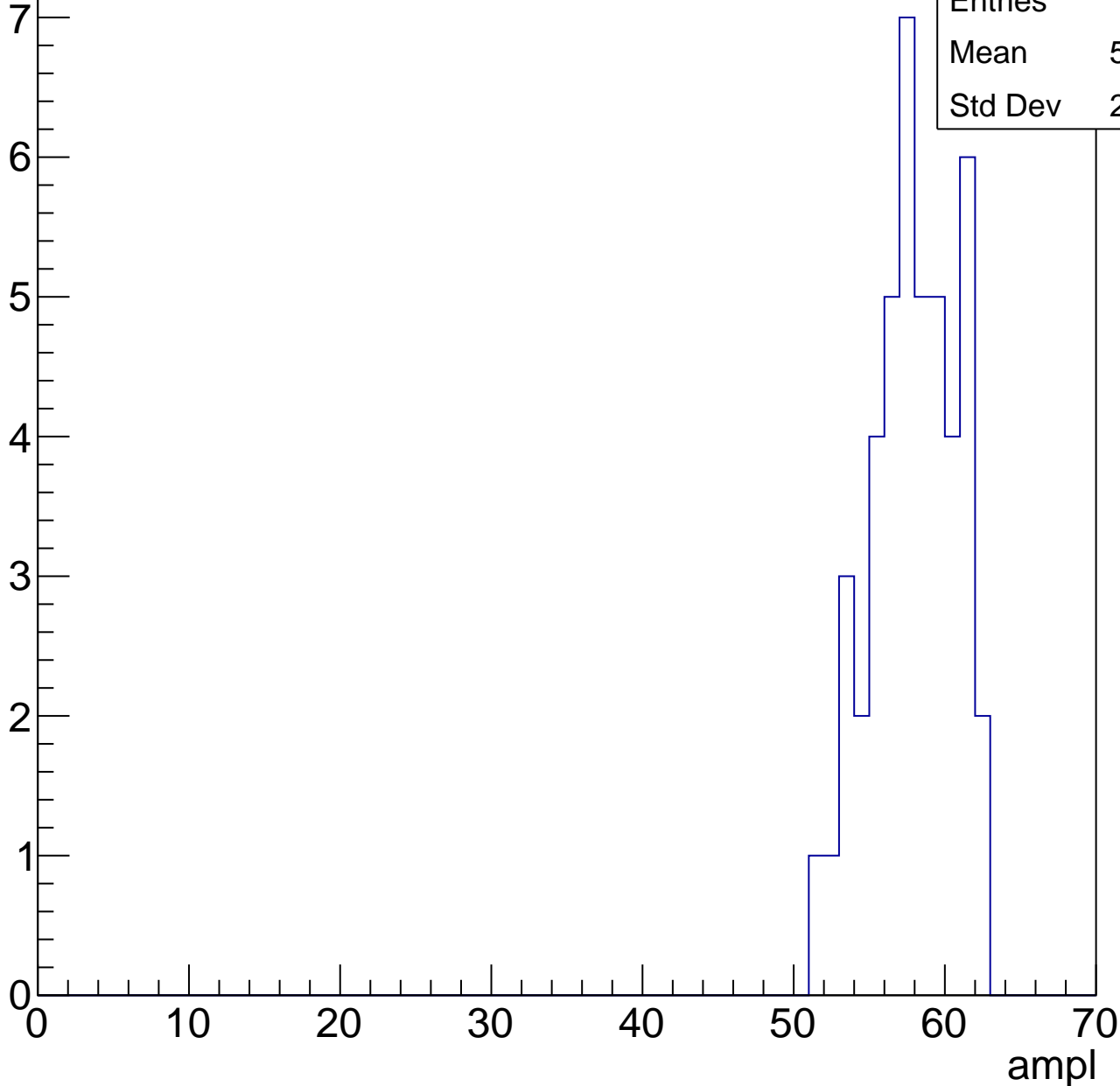
Entries	85
Mean	50.88
Std Dev	3.998

# B1L102S, U8-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	57.42
Std Dev	2.777

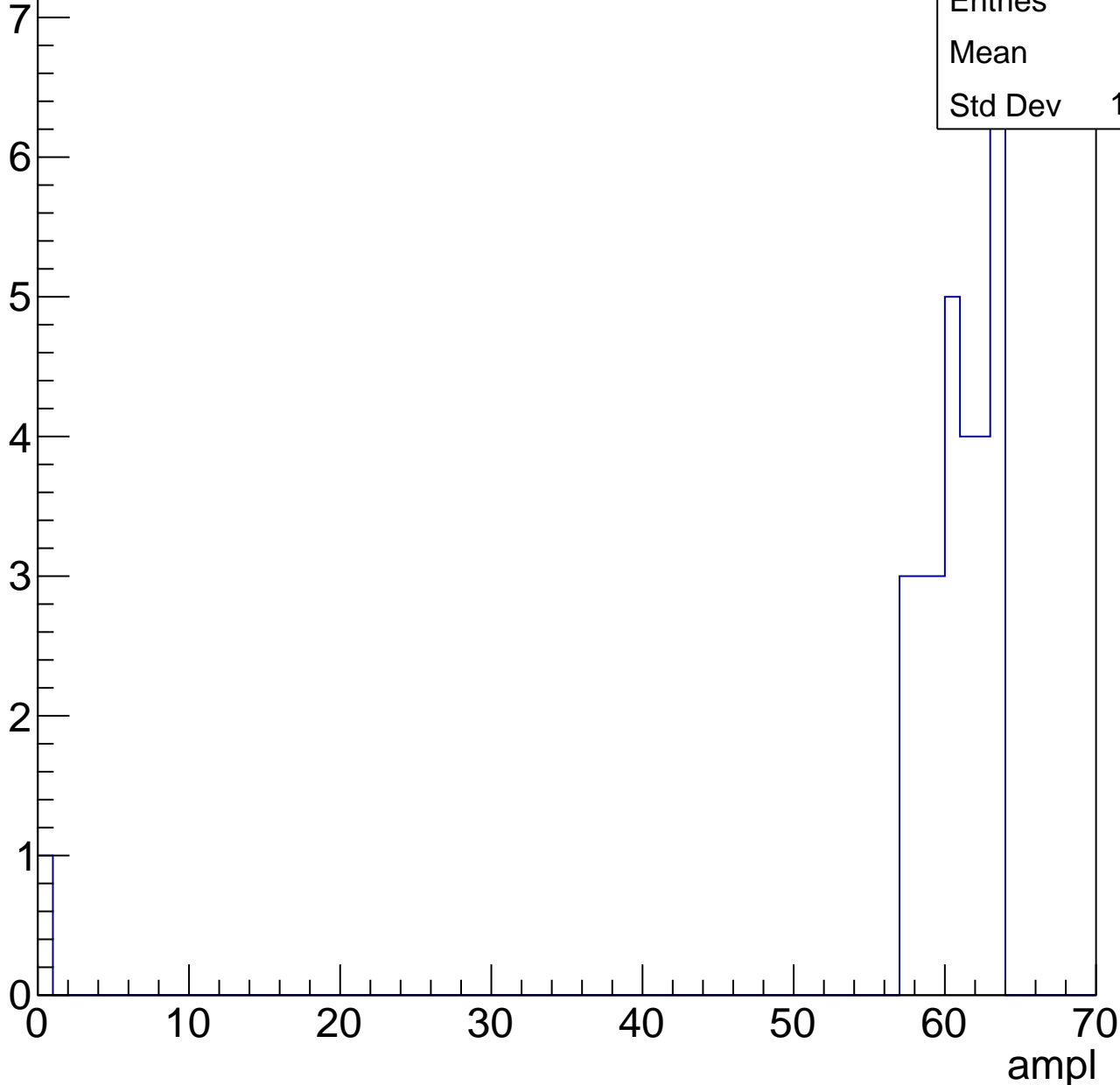


# B1L102S, U8-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

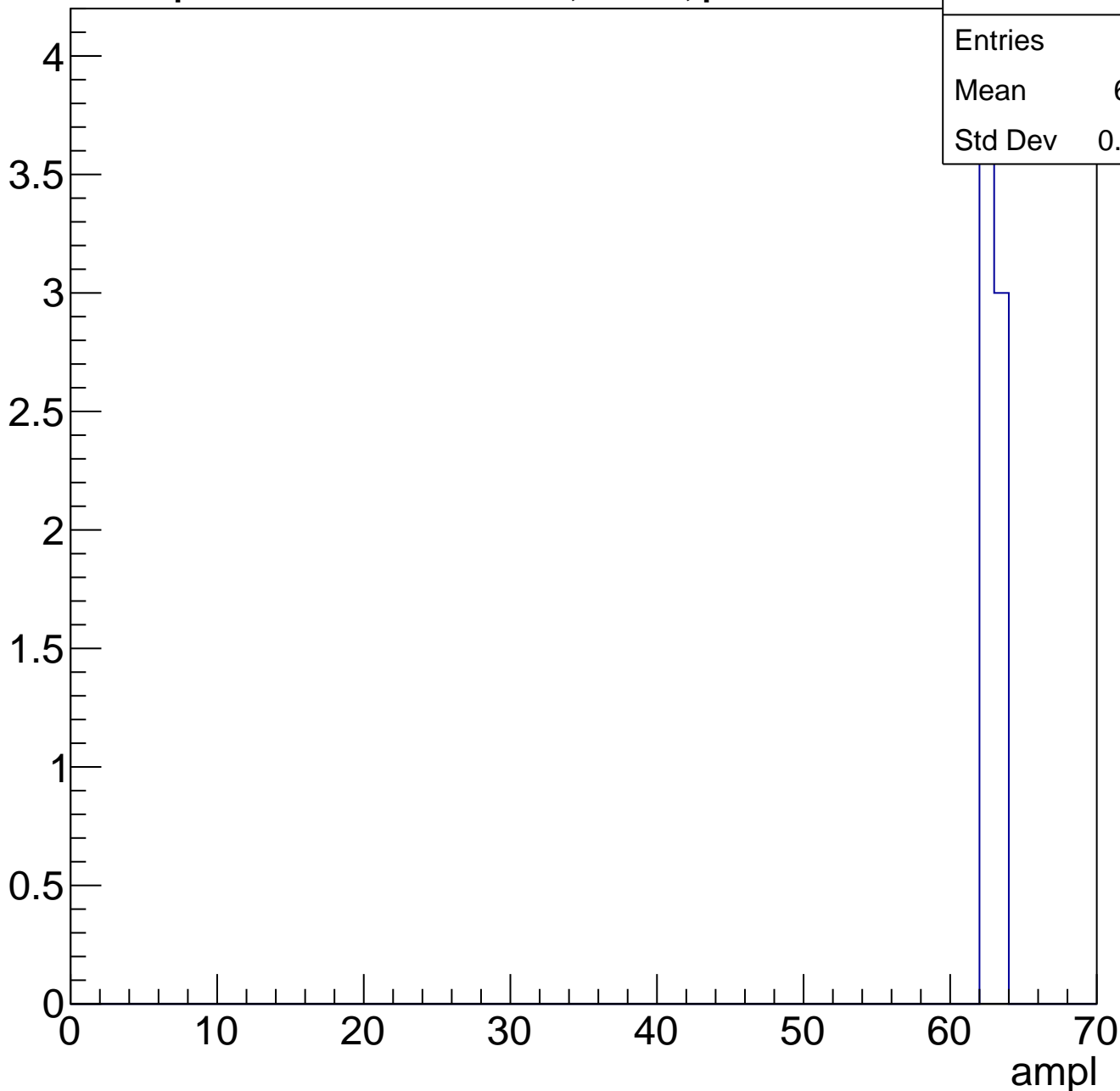
Entries	30
Mean	58.5
Std Dev	11.04



# B1L102S, U8-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U8-ch98, adc0

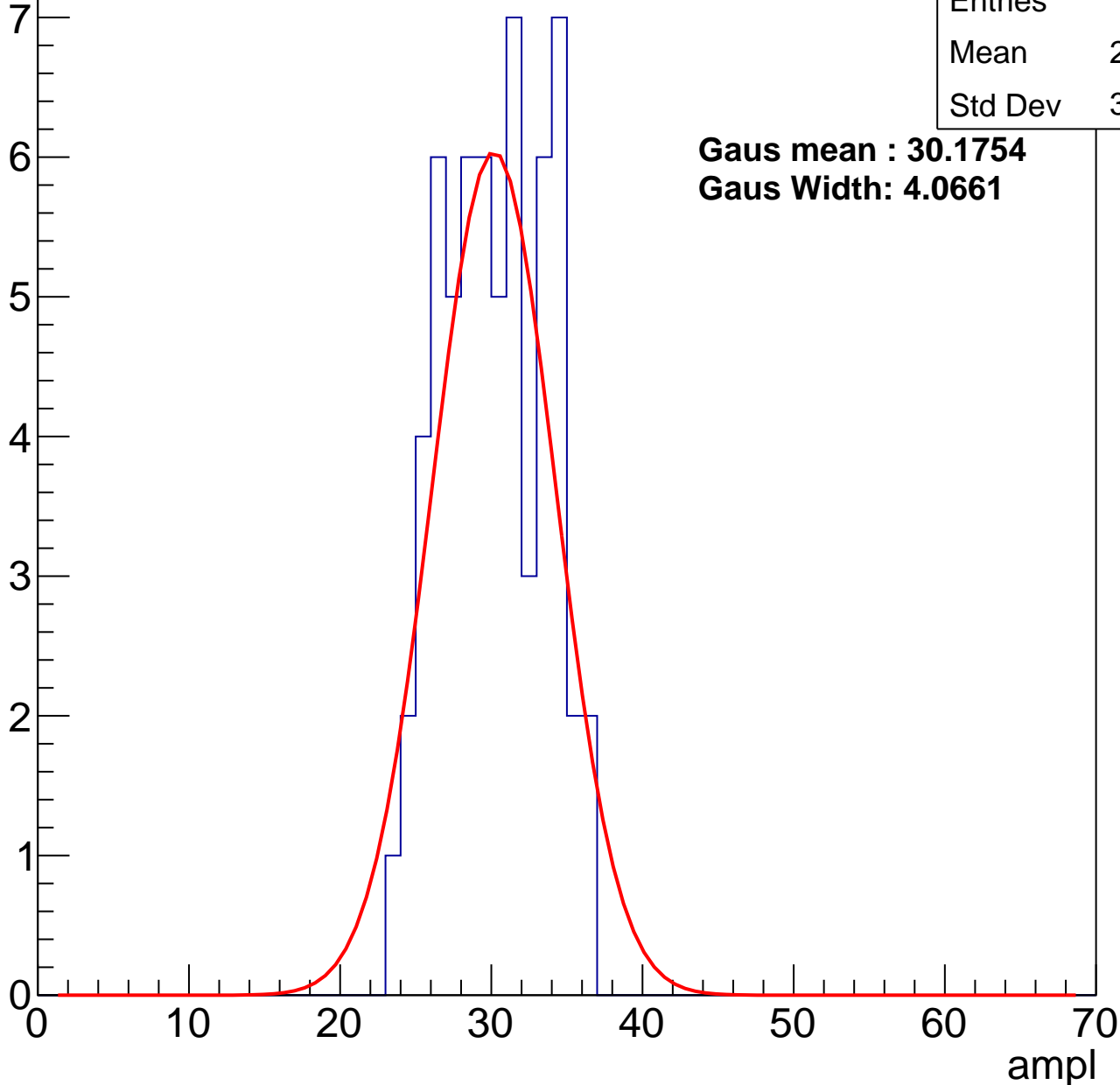
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	29.76
Std Dev	3.349

**Gaus mean : 30.1754**

**Gaus Width: 4.0661**



# B1L102S, U8-ch98, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	85
Mean	36.07
Std Dev	4.259

**Gaus mean : 36.9005**

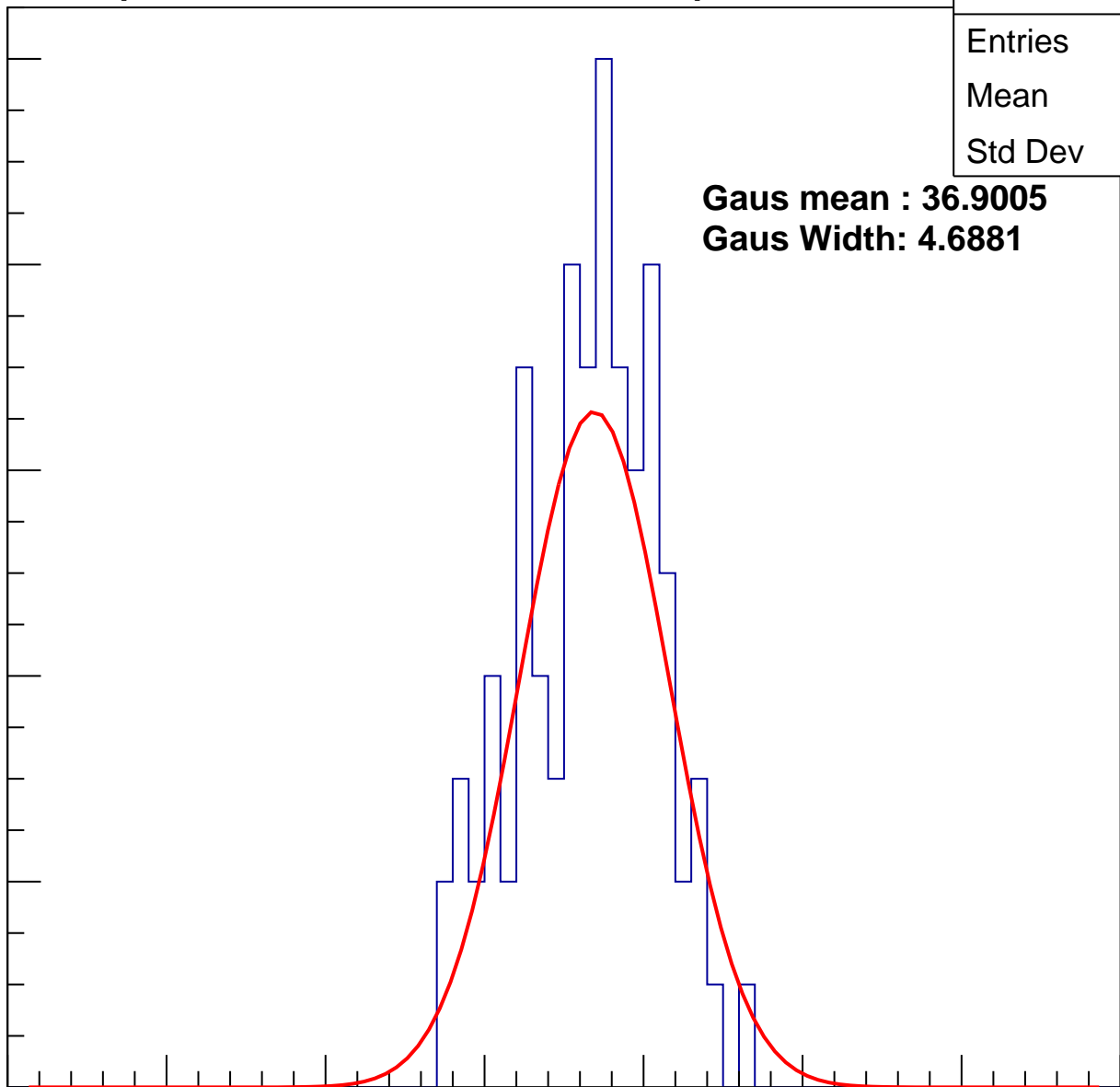
**Gaus Width: 4.6881**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U8-ch98, adc2

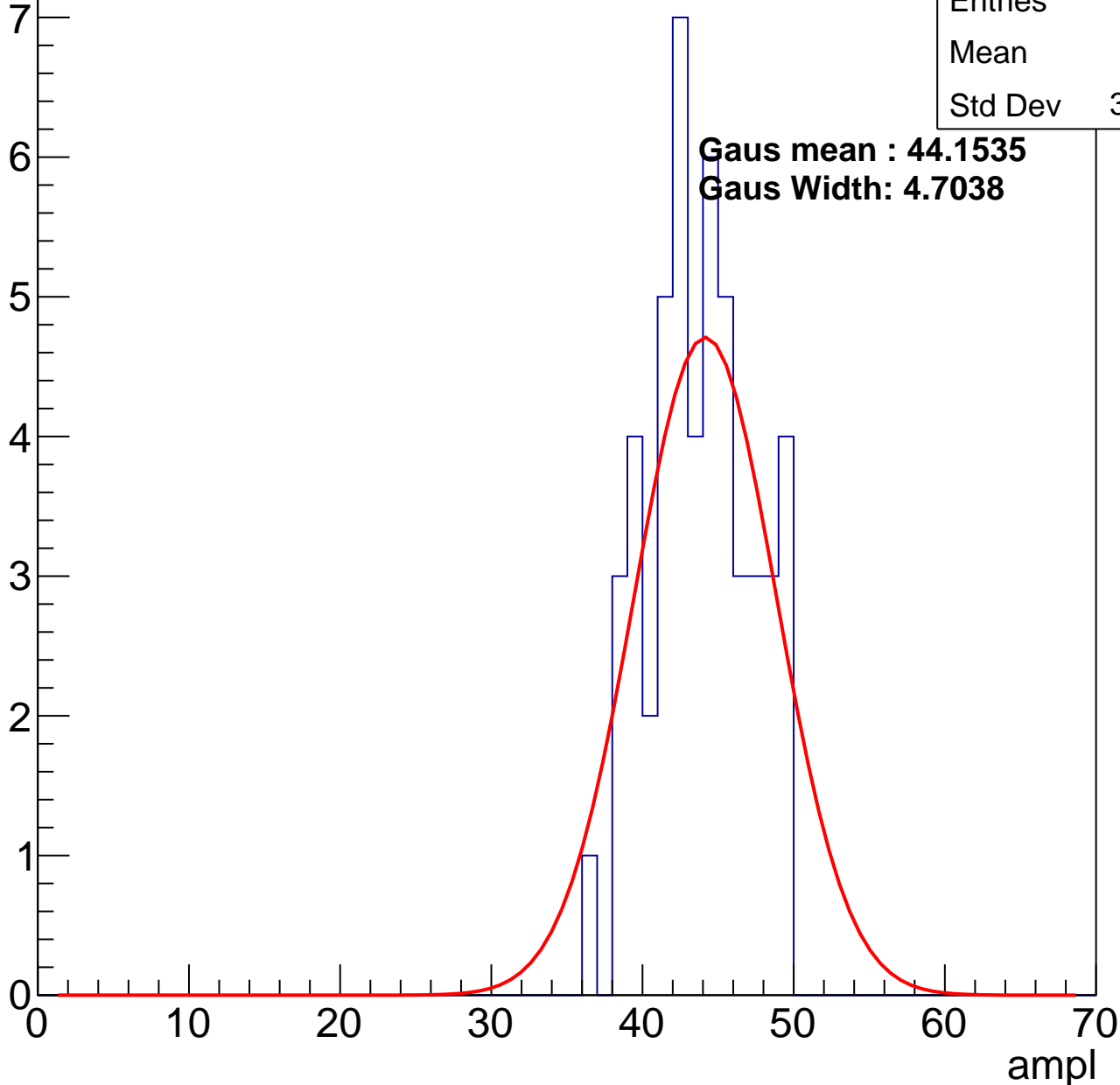
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	43.3
Std Dev	3.312

**Gaus mean : 44.1535**

**Gaus Width: 4.7038**

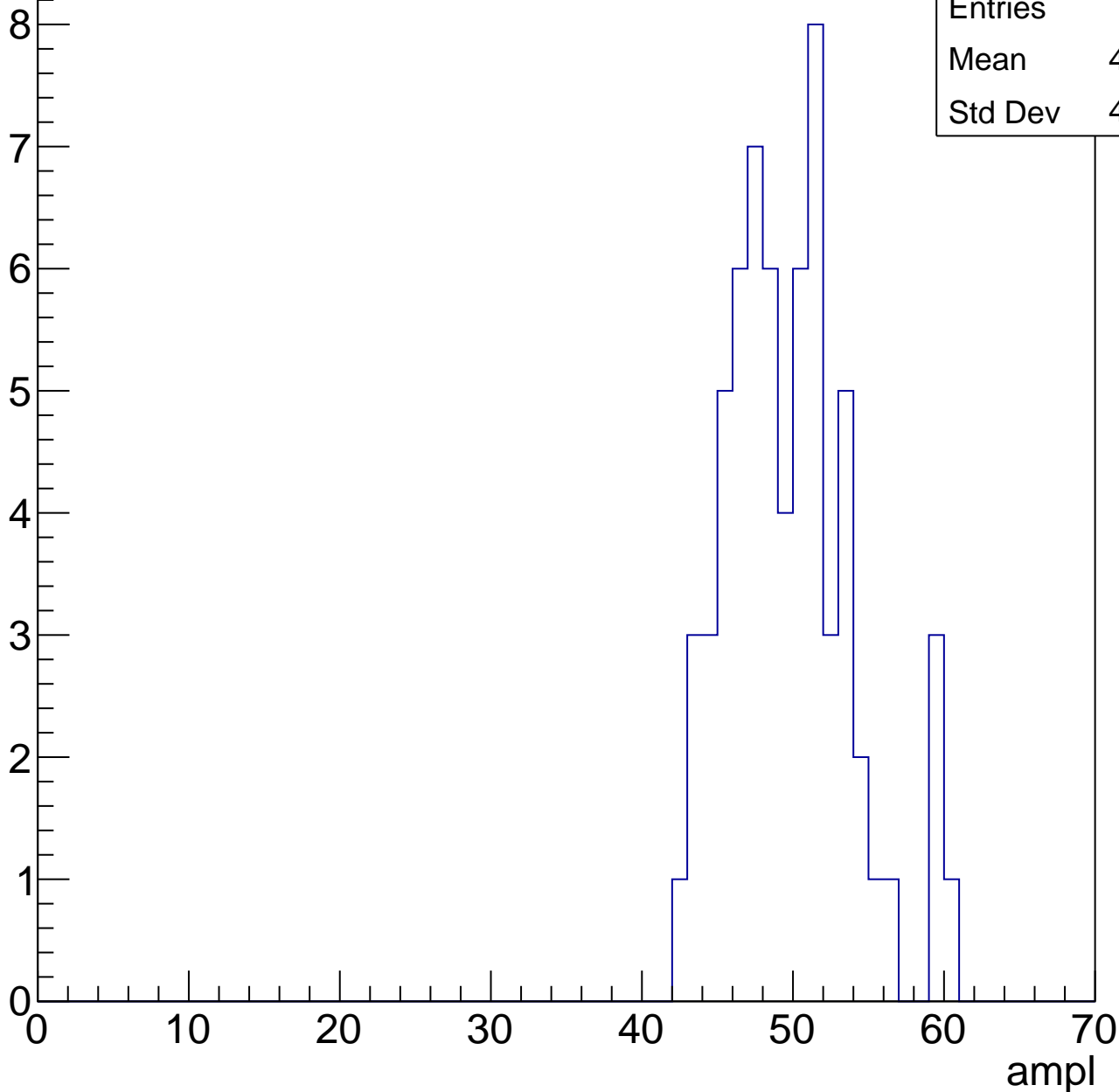


# B1L102S, U8-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	49.26
Std Dev	4.107

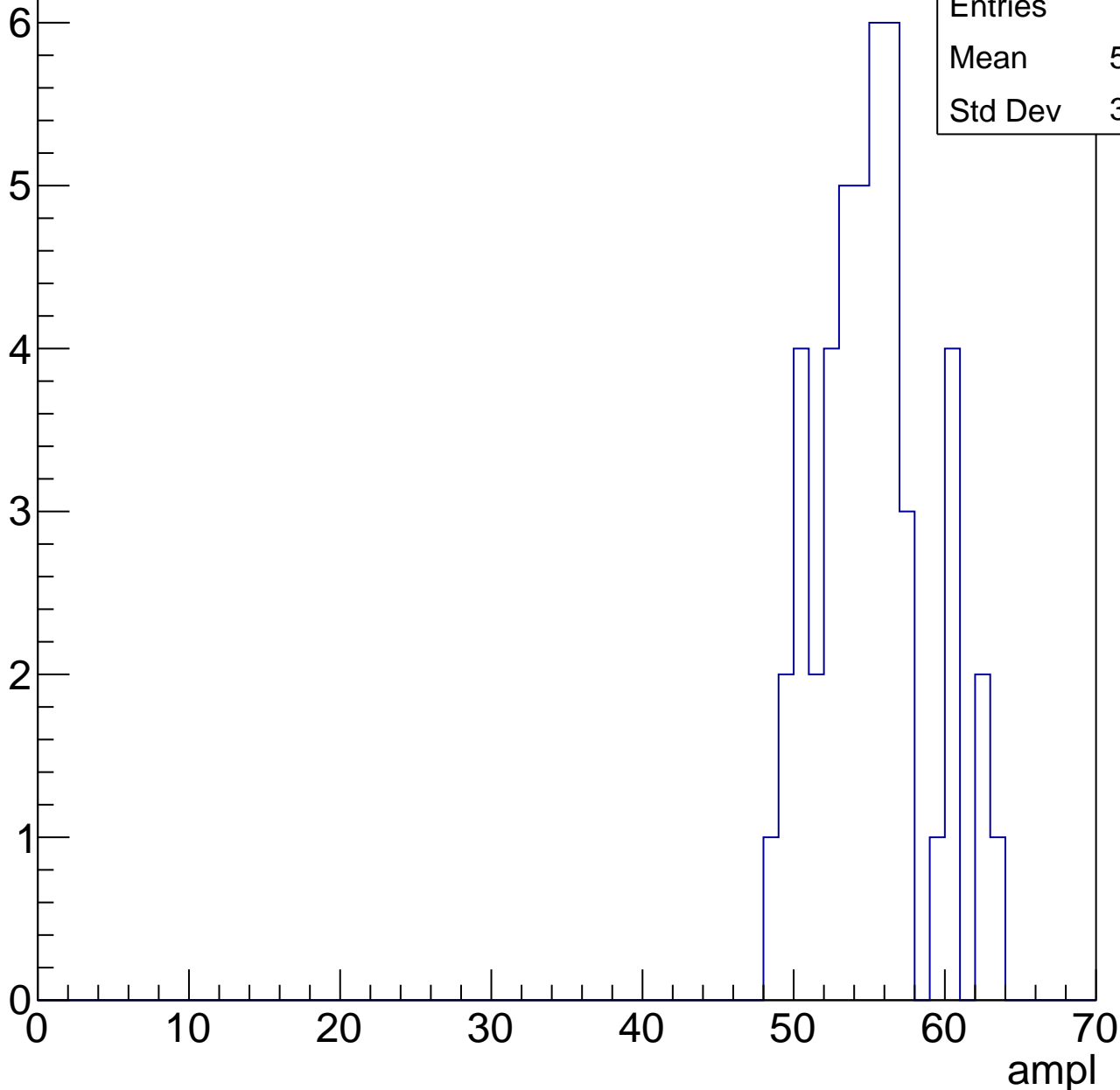


# B1L102S, U8-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

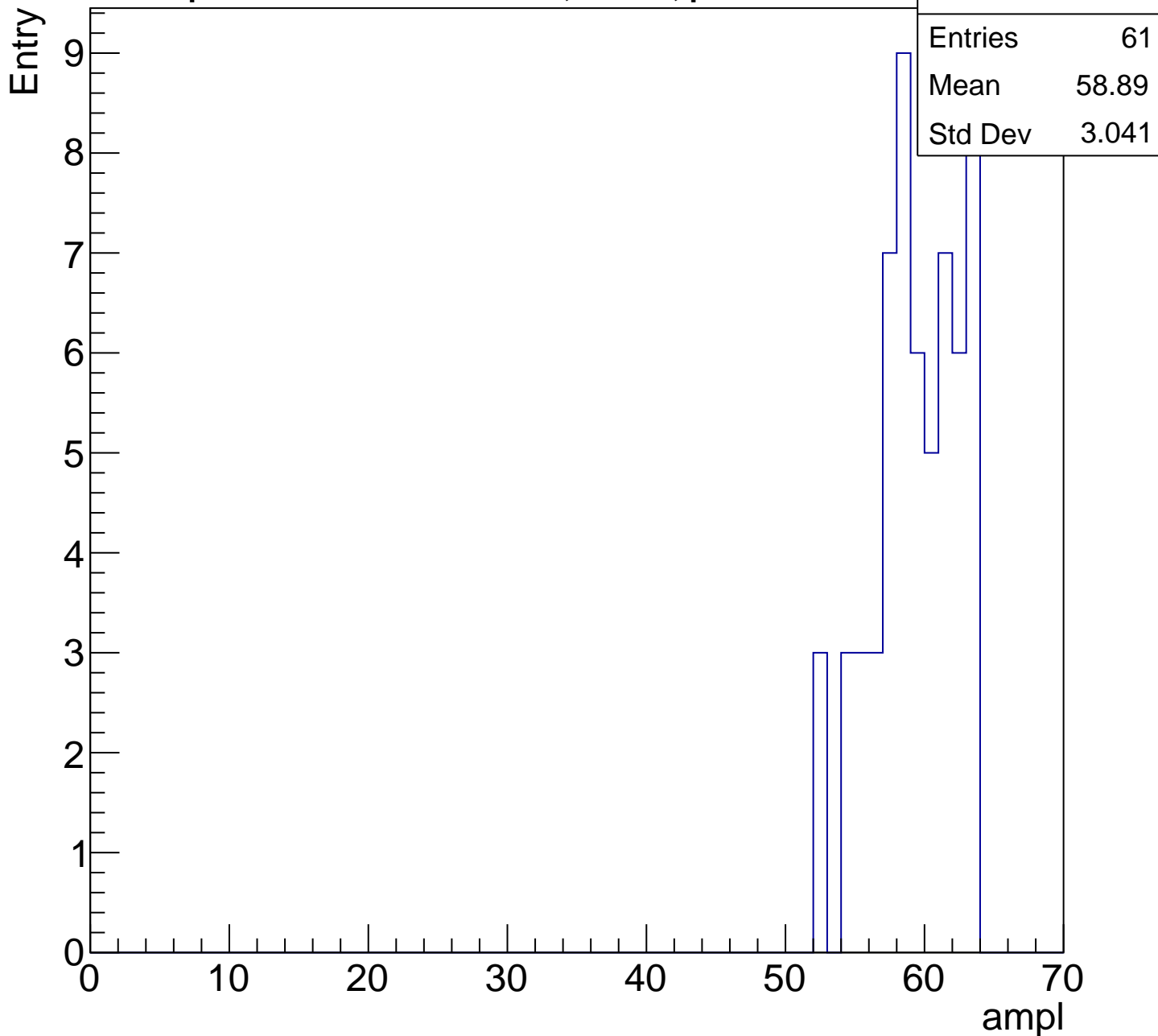
Entry

Entries	46
Mean	54.65
Std Dev	3.625



# B1L102S, U8-ch98, adc5

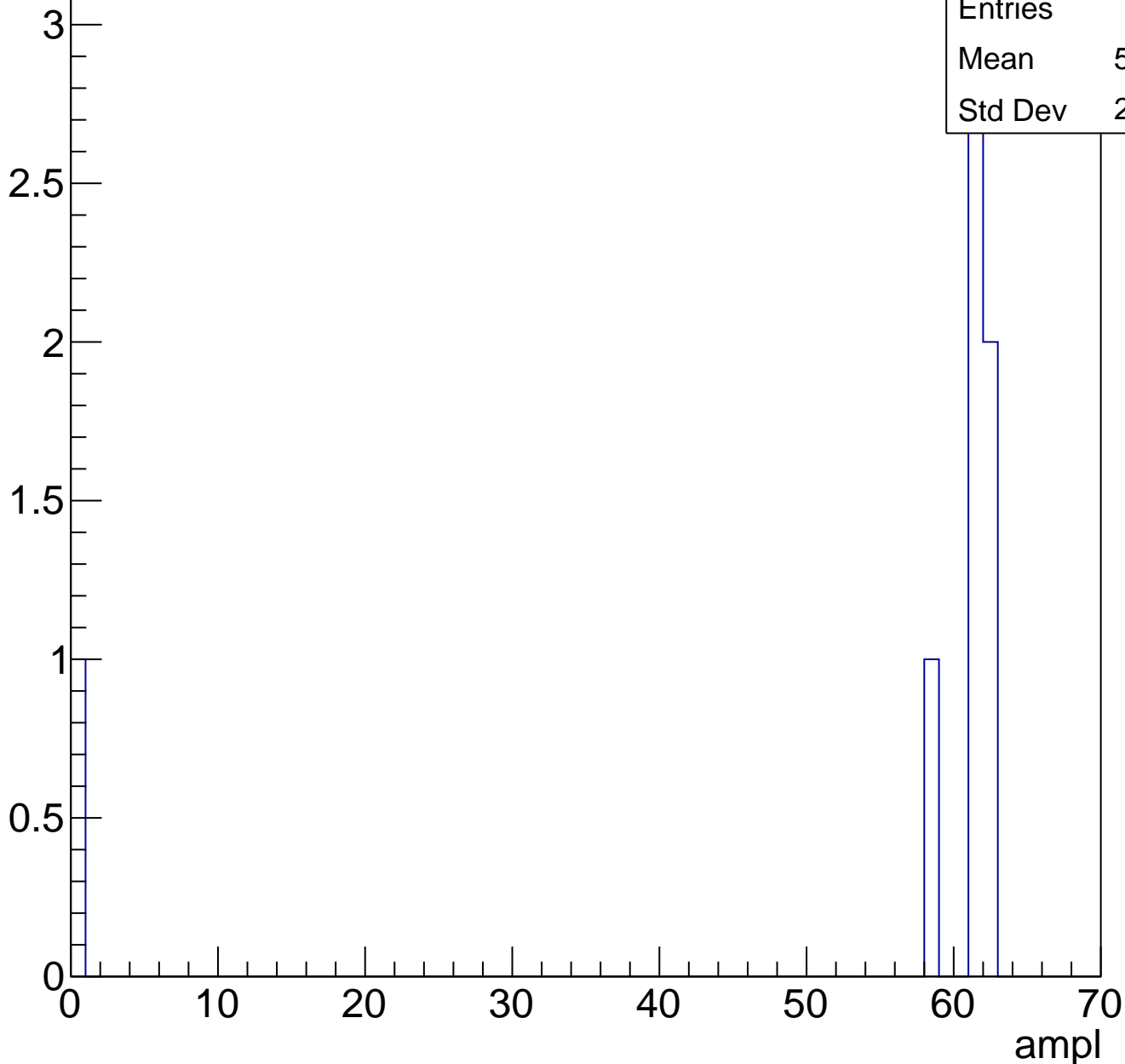
calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U8-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	7.667
Std Dev	10.84

# B1L102S, U8-ch99, adc0

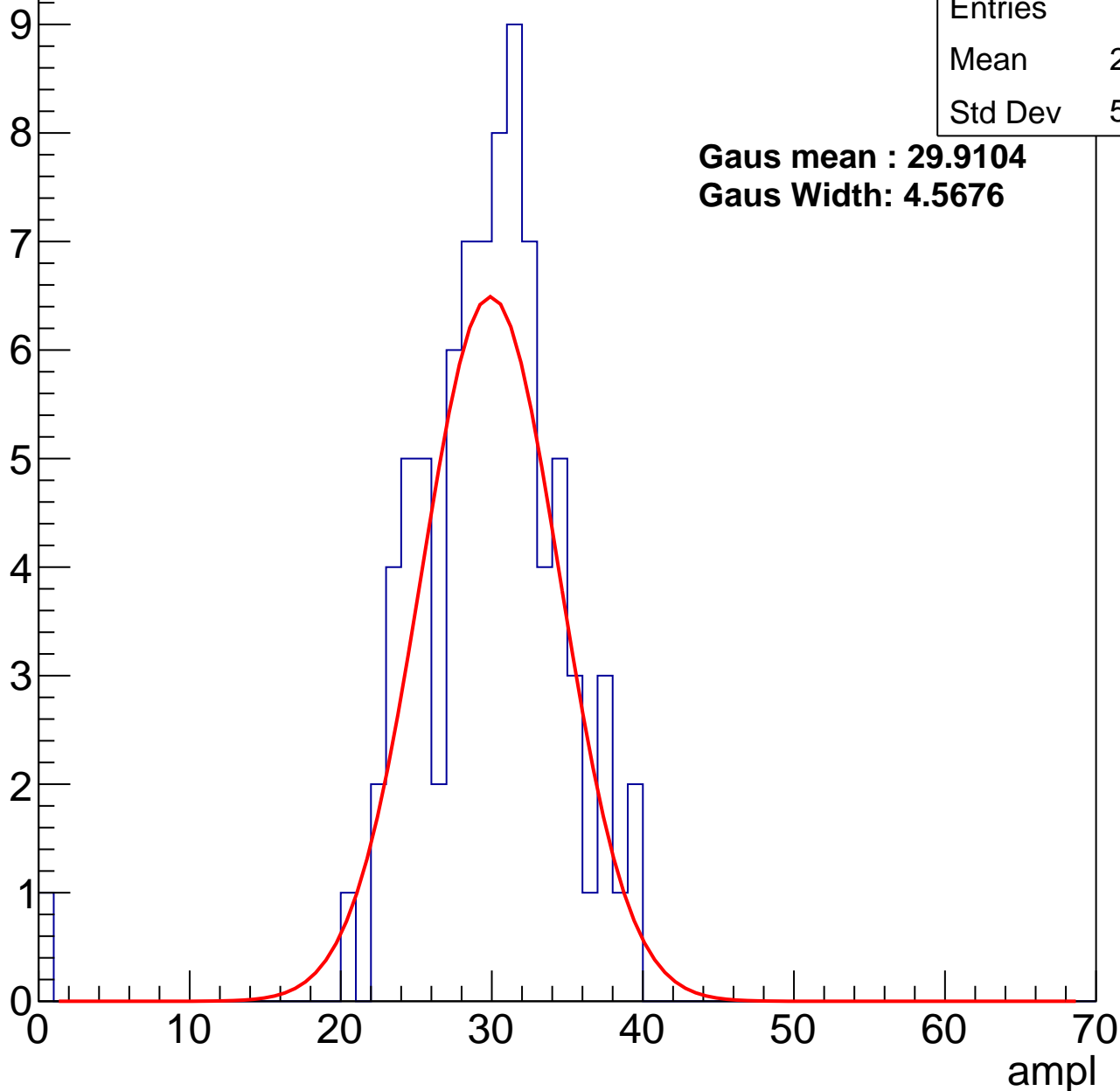
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	83
Mean	29.24
Std Dev	5.309

**Gaus mean : 29.9104**

**Gaus Width: 4.5676**



# B1L102S, U8-ch99, adc1

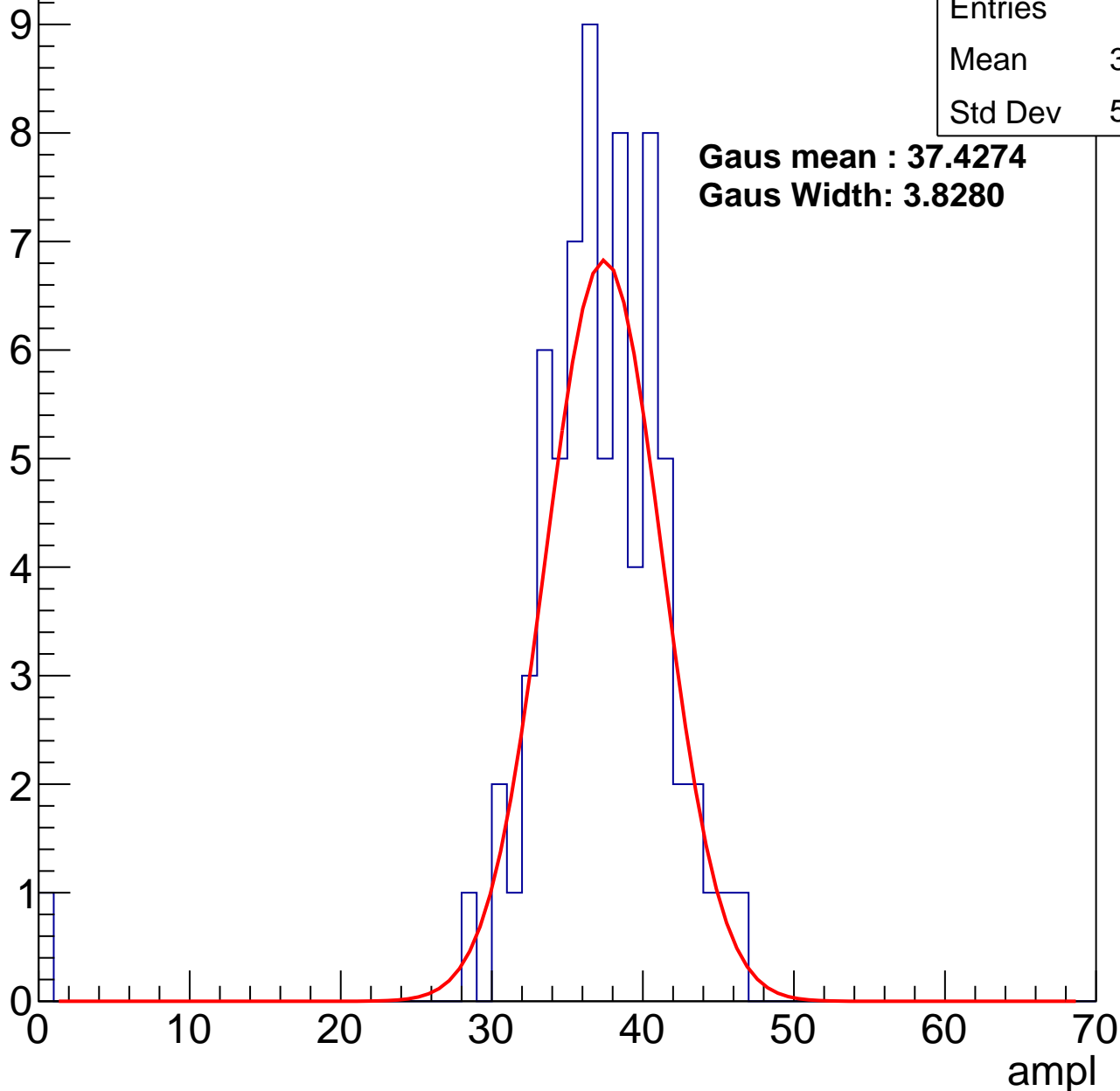
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	36.49
Std Dev	5.664

**Gaus mean : 37.4274**

**Gaus Width: 3.8280**



# B1L102S, U8-ch99, adc2

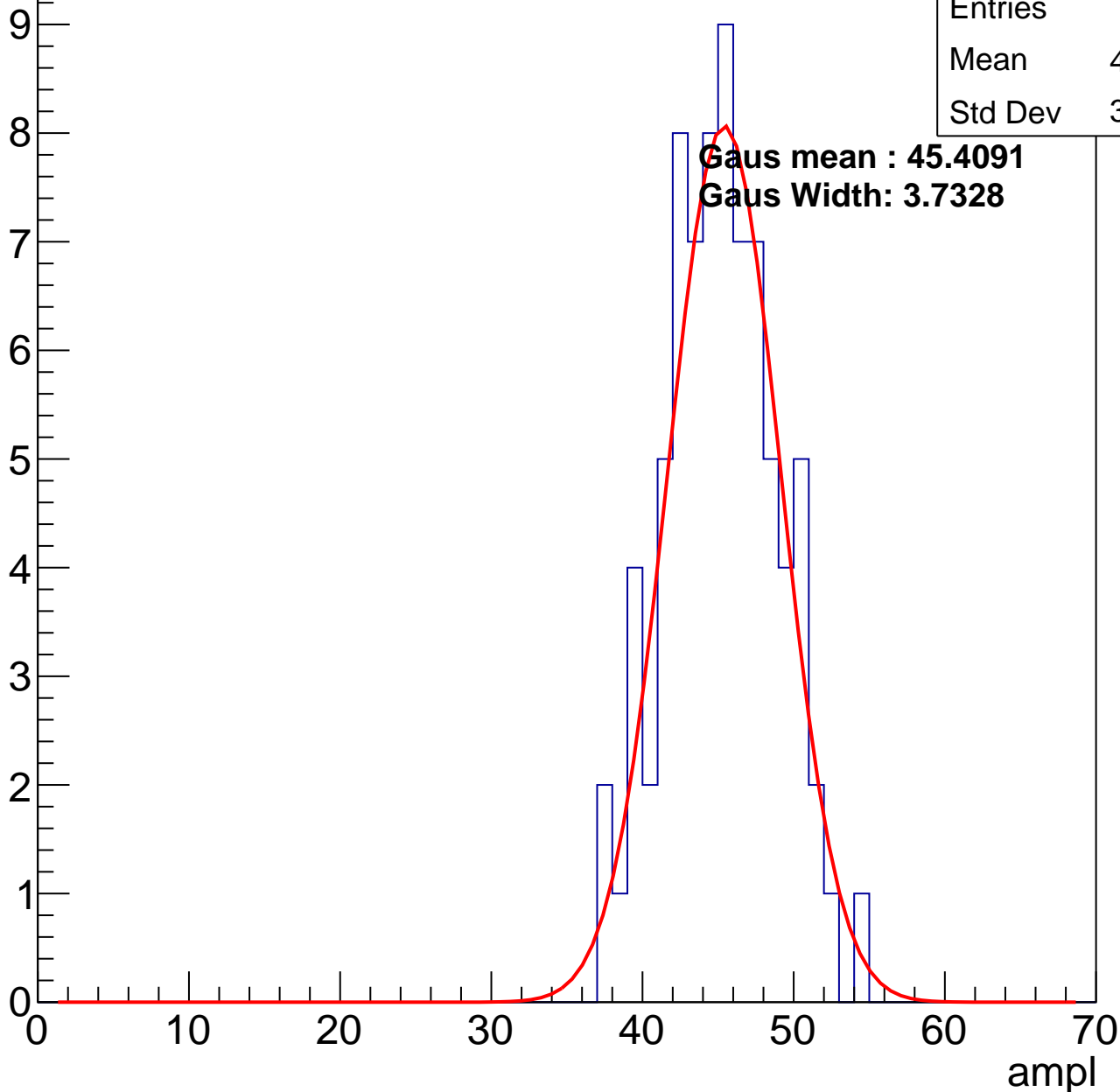
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	44.77
Std Dev	3.627

**Gaus mean : 45.4091**

**Gaus Width: 3.7328**

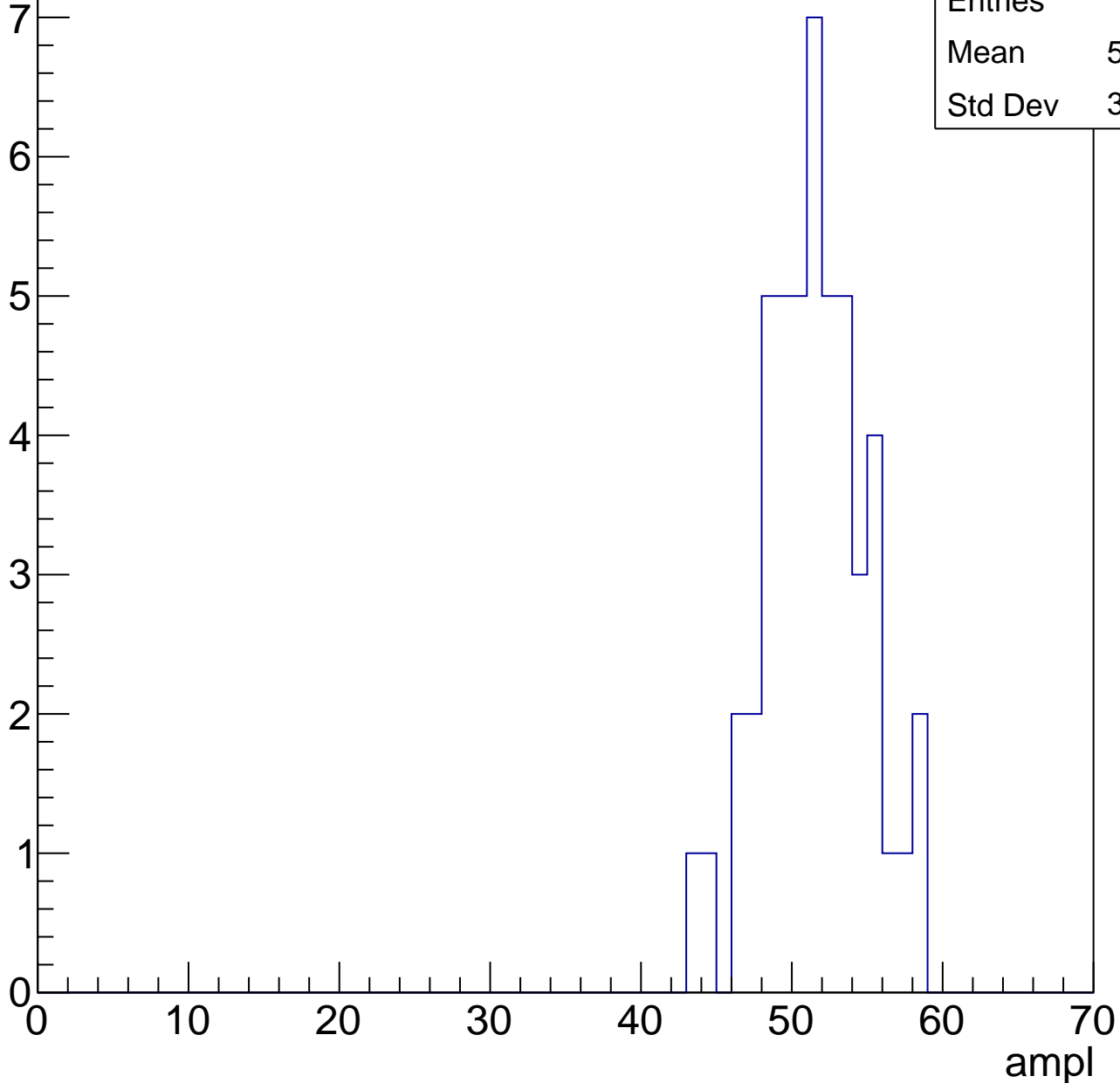


# B1L102S, U8-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	51.04
Std Dev	3.319

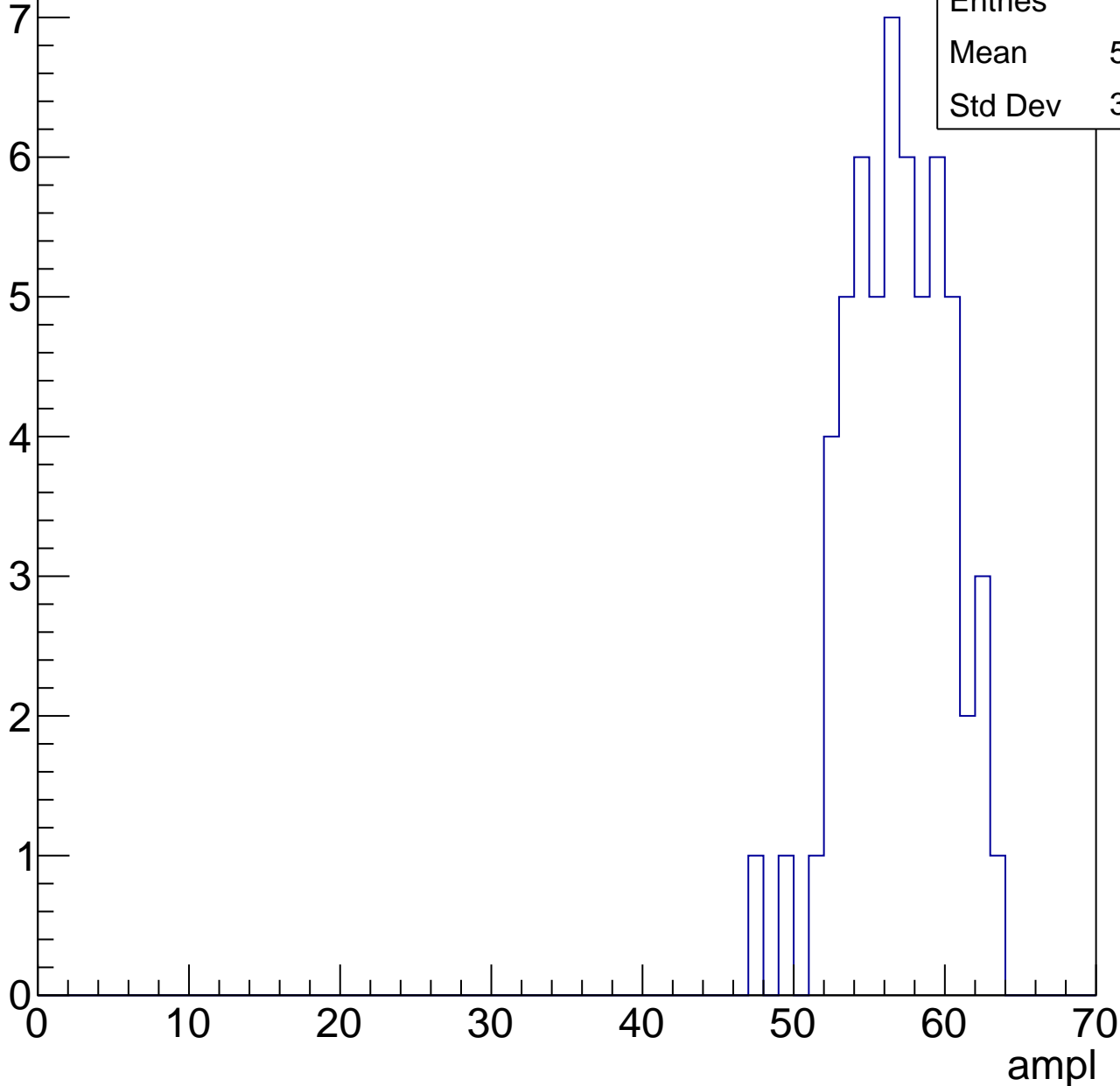


# B1L102S, U8-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	56.34
Std Dev	3.356

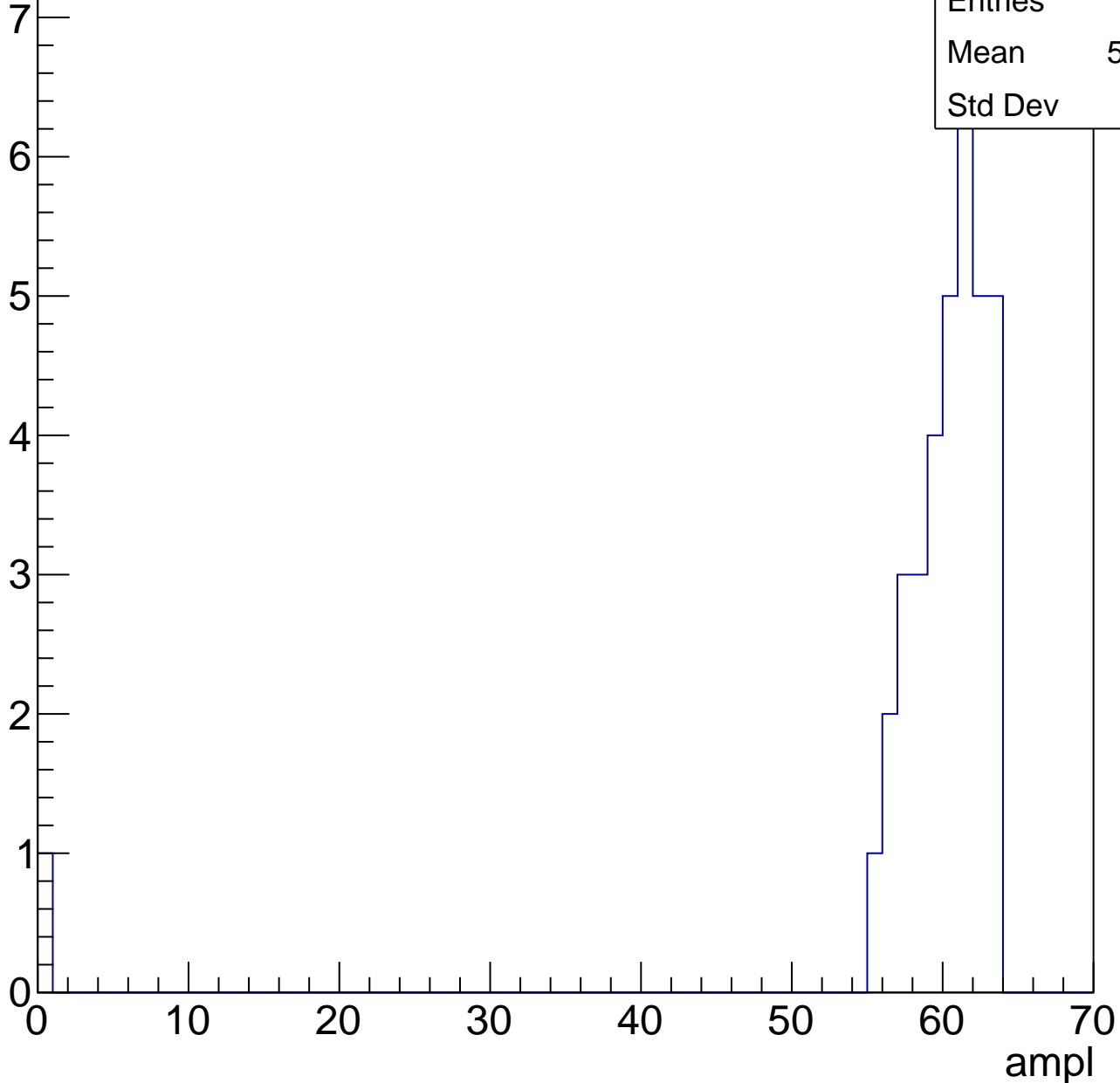


# B1L102S, U8-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

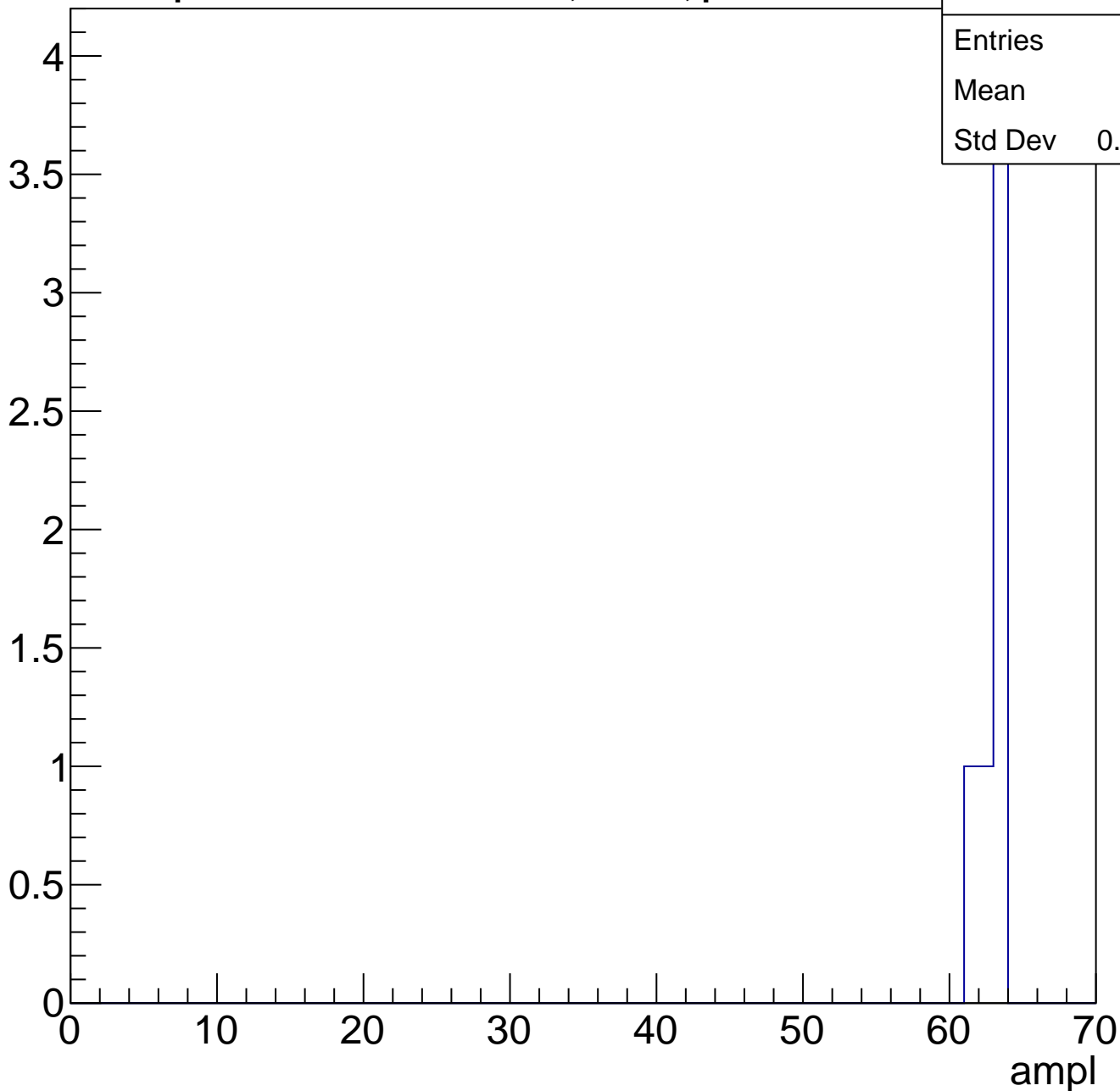
Entries	36
Mean	58.33
Std Dev	10.1



# B1L102S, U8-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch100, adc0

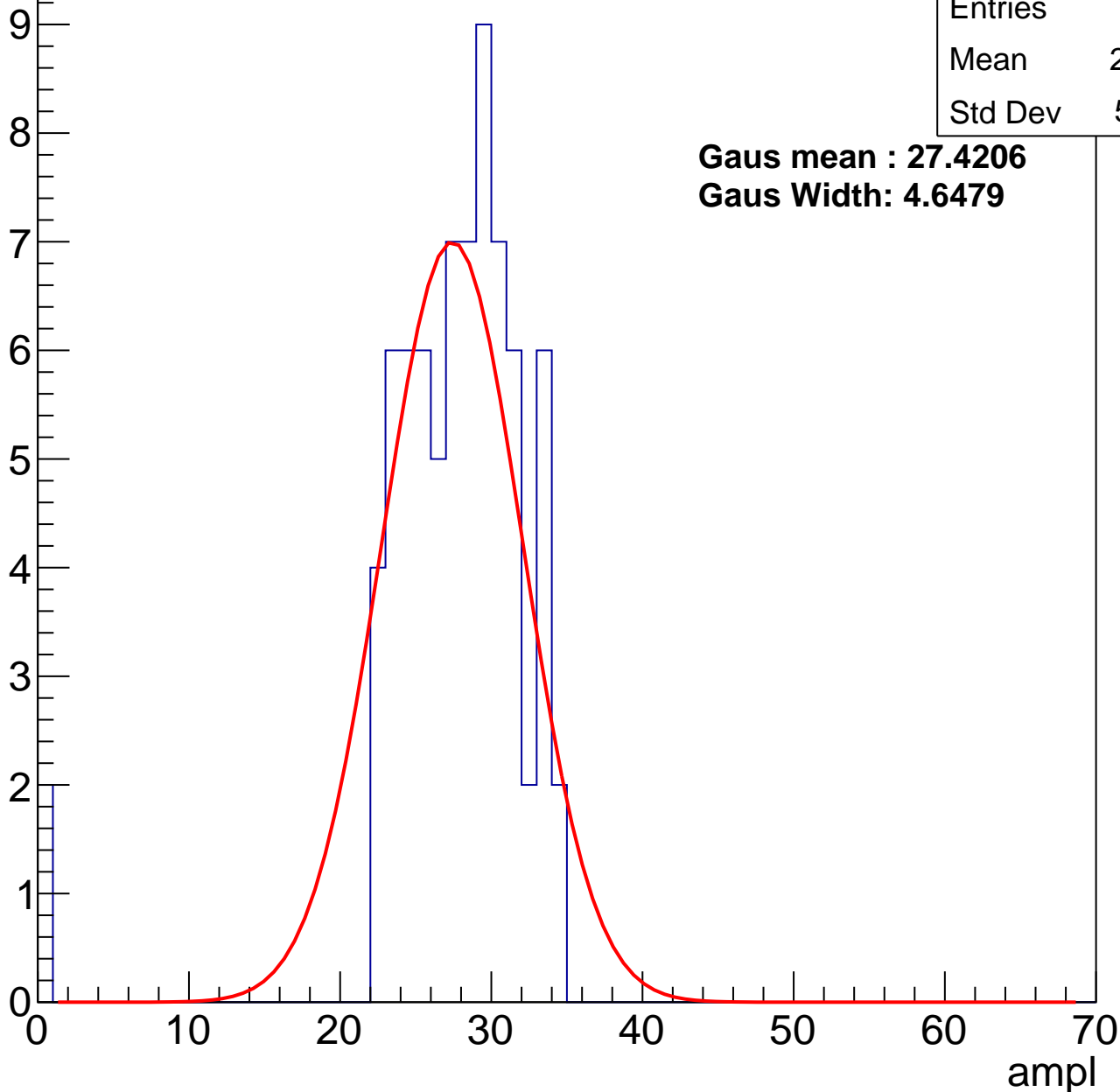
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	26.96
Std Dev	5.541

**Gaus mean : 27.4206**

**Gaus Width: 4.6479**



# B1L102S, U8-ch100, adc1

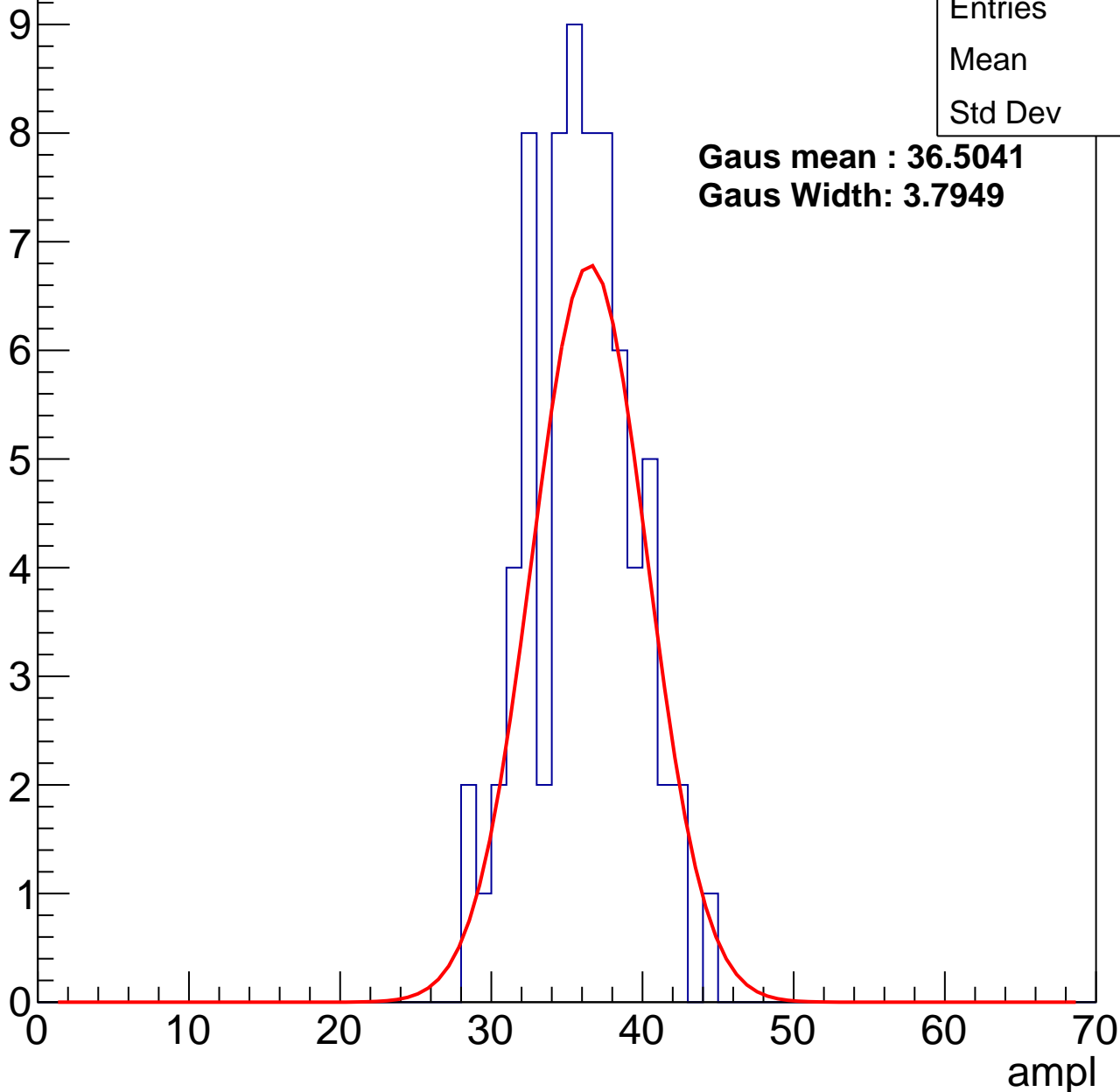
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	35.5
Std Dev	3.44

**Gaus mean : 36.5041**

**Gaus Width: 3.7949**



# B1L102S, U8-ch100, adc2

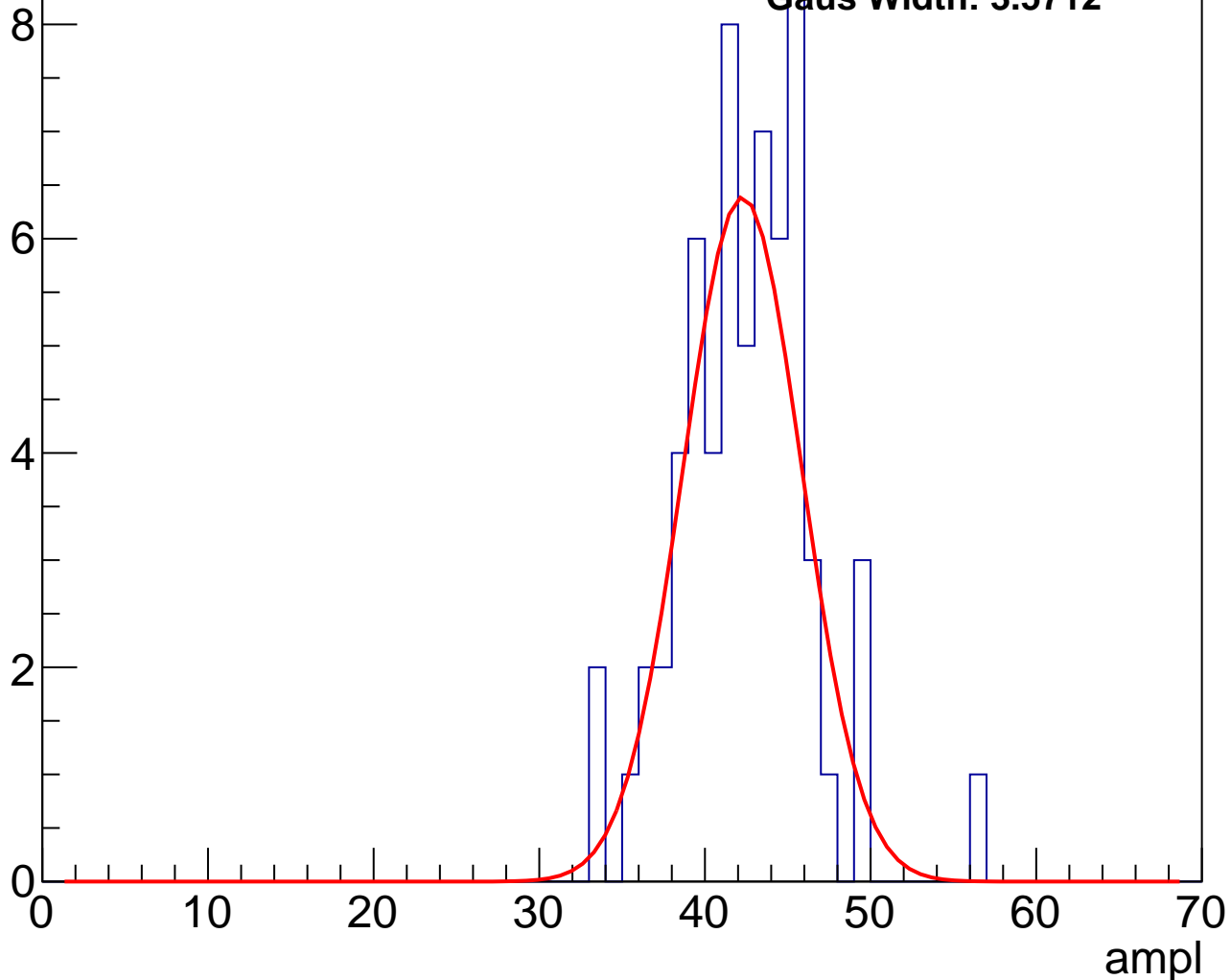
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	42.06
Std Dev	3.945

**Gaus mean : 42.2643**

**Gaus Width: 3.5712**

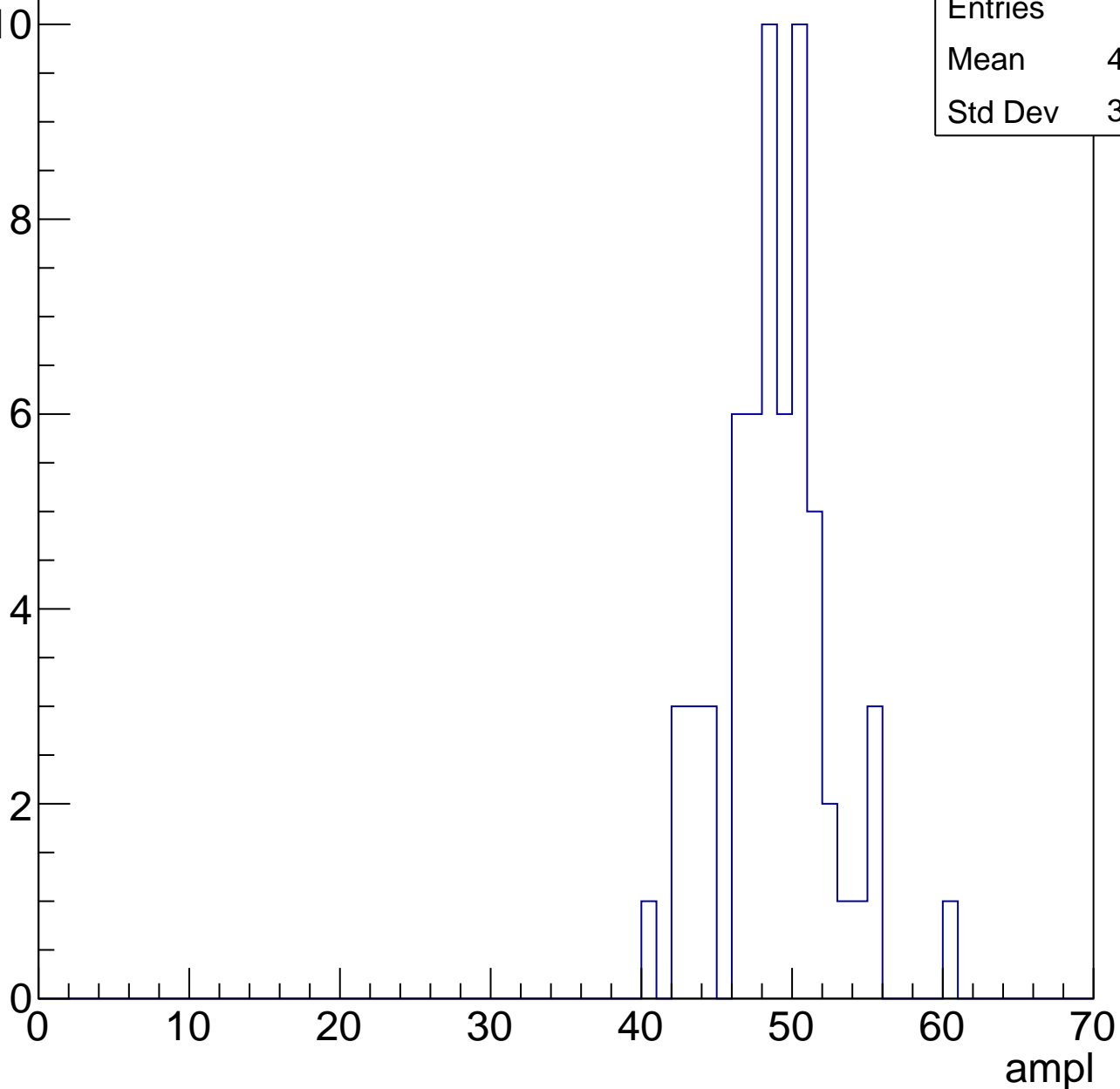


# B1L102S, U8-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	48.36
Std Dev	3.603

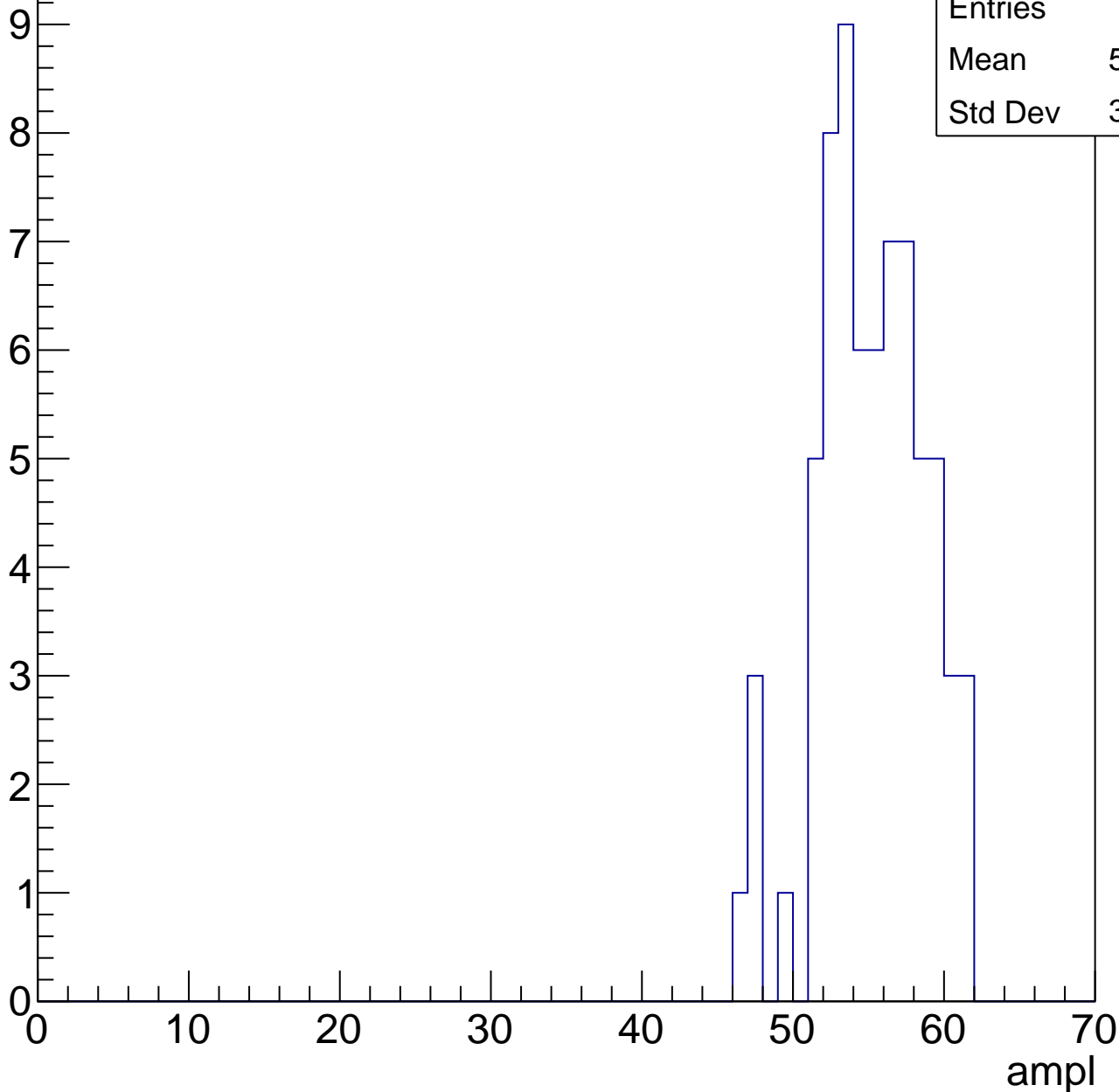


# B1L102S, U8-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

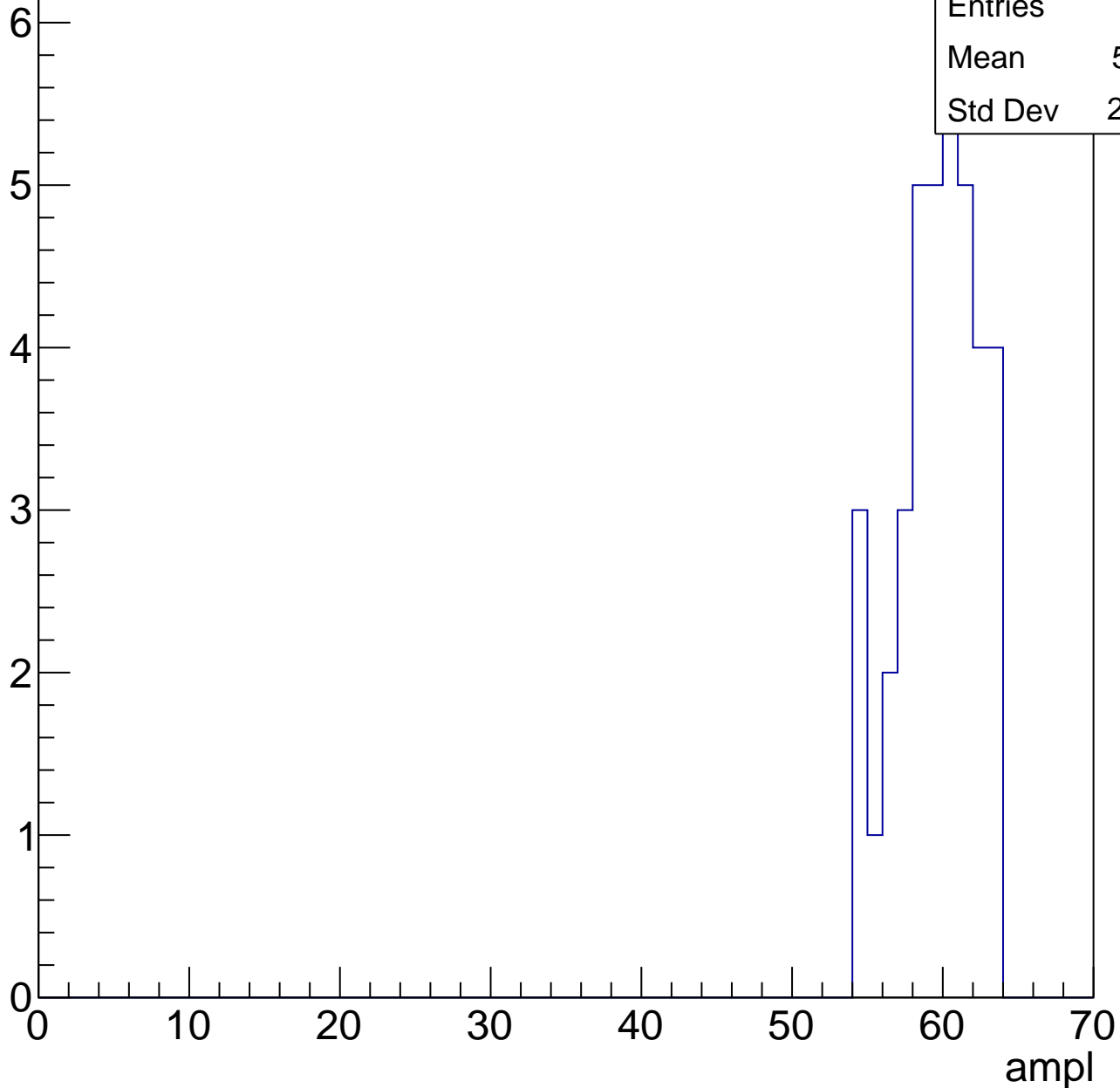
Entries	69
Mean	54.74
Std Dev	3.492



# B1L102S, U8-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



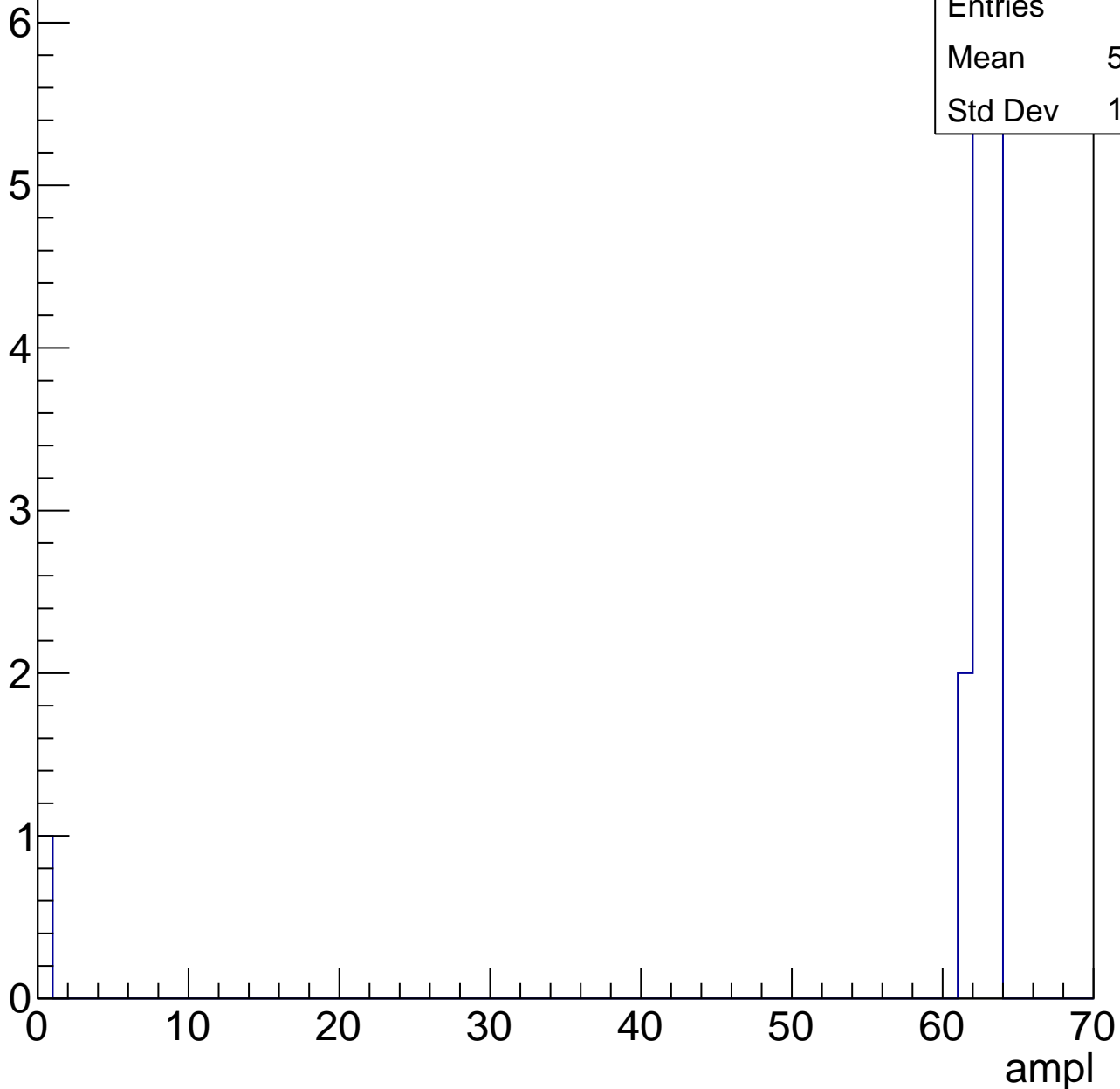
Entries	38
Mean	59.21
Std Dev	2.567

# B1L102S, U8-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	15
Mean	58.13
Std Dev	15.55





# B1L102S, U8-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch101, adc0

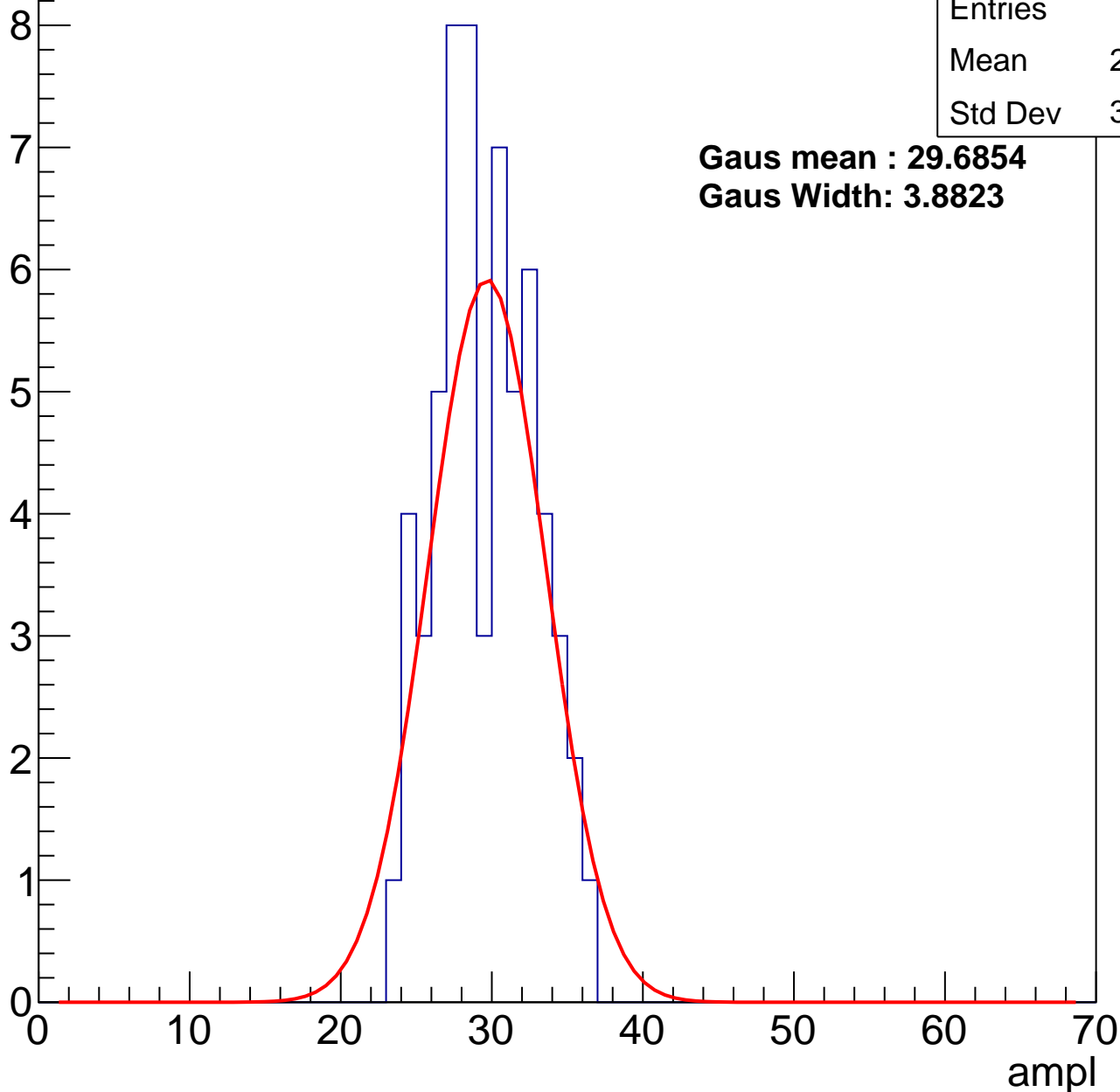
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	29.13
Std Dev	3.186

**Gaus mean : 29.6854**

**Gaus Width: 3.8823**



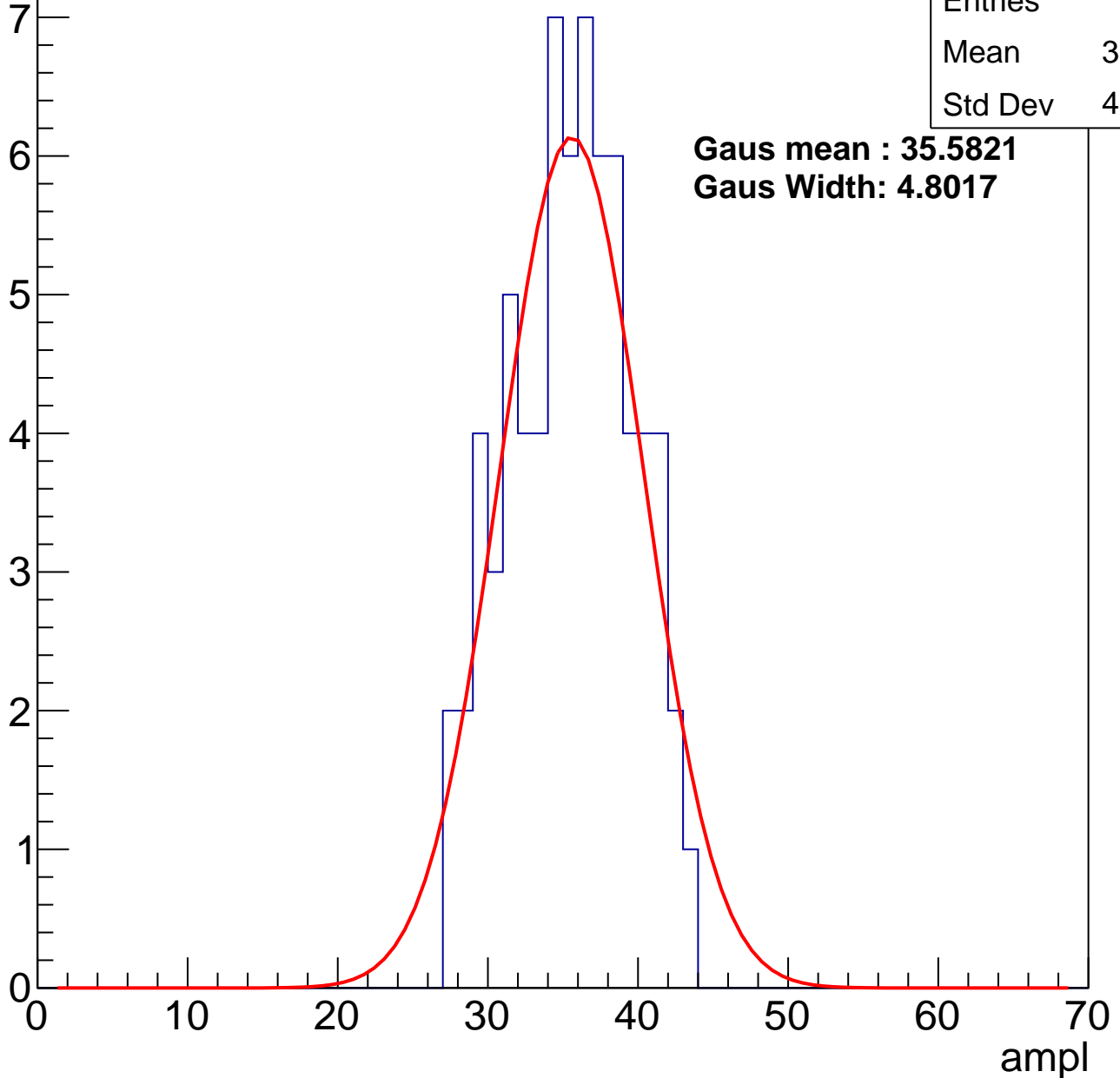
# B1L102S, U8-ch101, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	35.04
Std Dev	4.005

**Gaus mean : 35.5821**  
**Gaus Width: 4.8017**



# B1L102S, U8-ch101, adc2

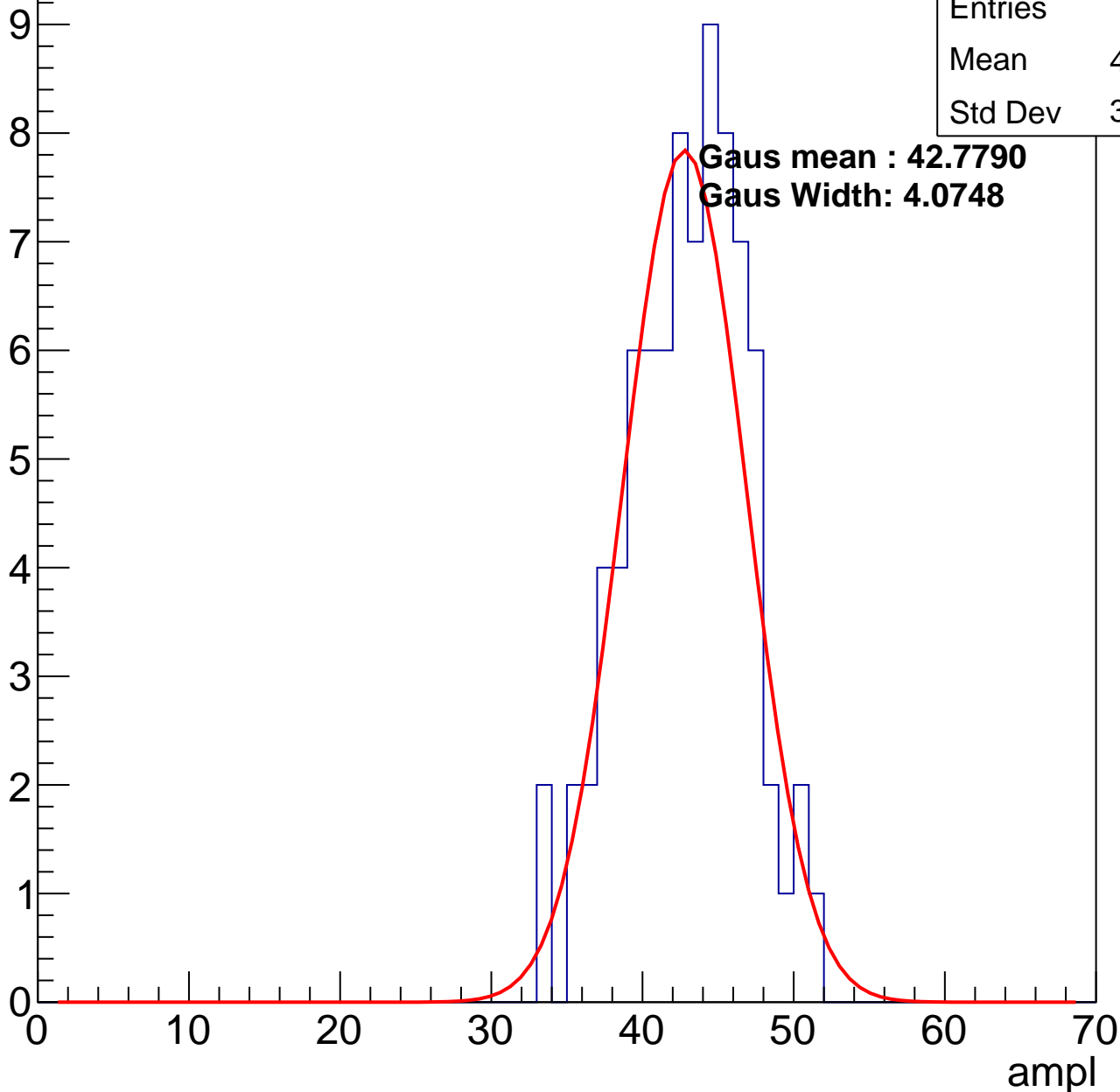
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	83
Mean	42.42
Std Dev	3.915

**Gaus mean : 42.7790**

**Gaus Width: 4.0748**

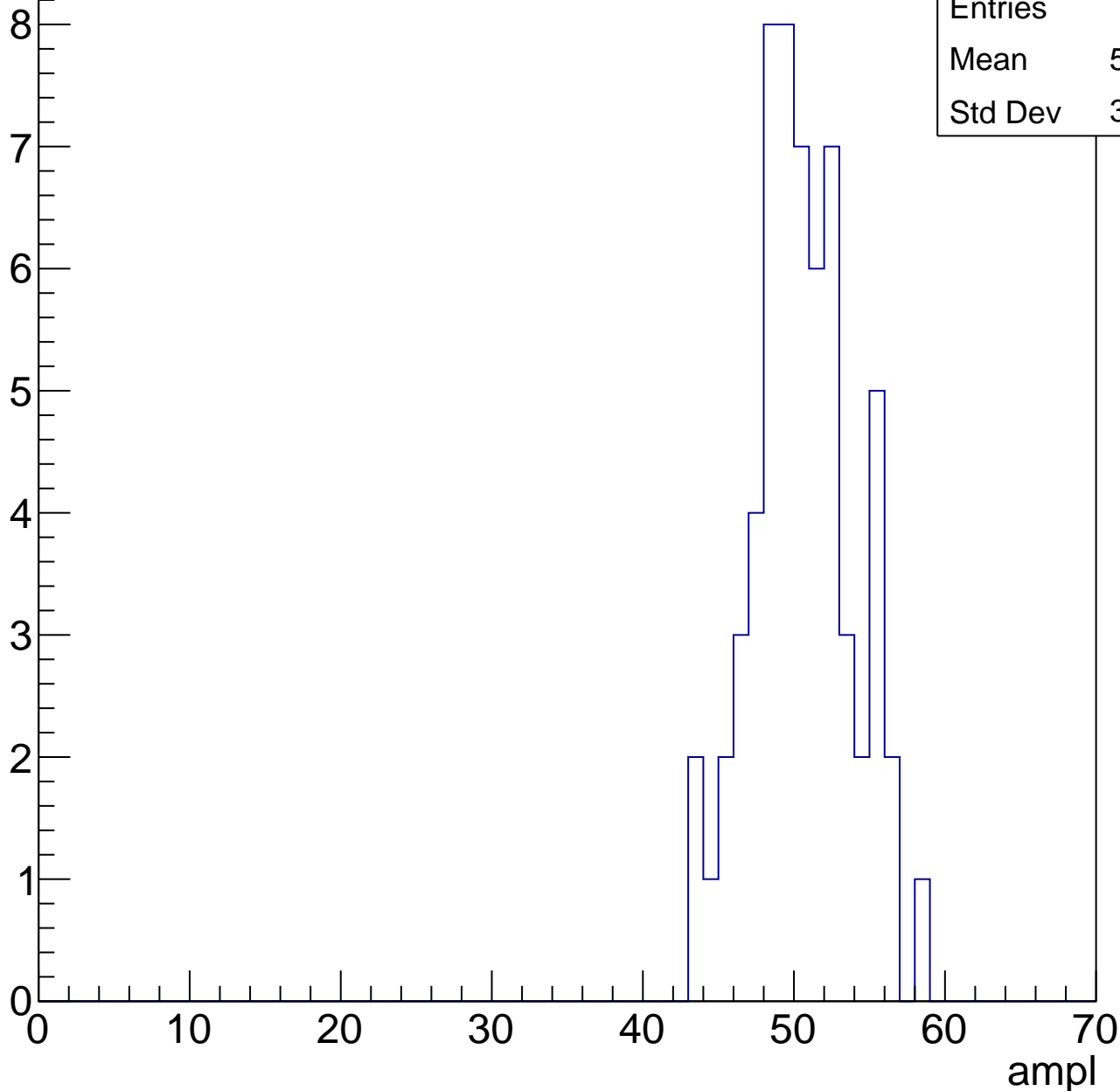


# B1L102S, U8-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	50.07
Std Dev	3.294

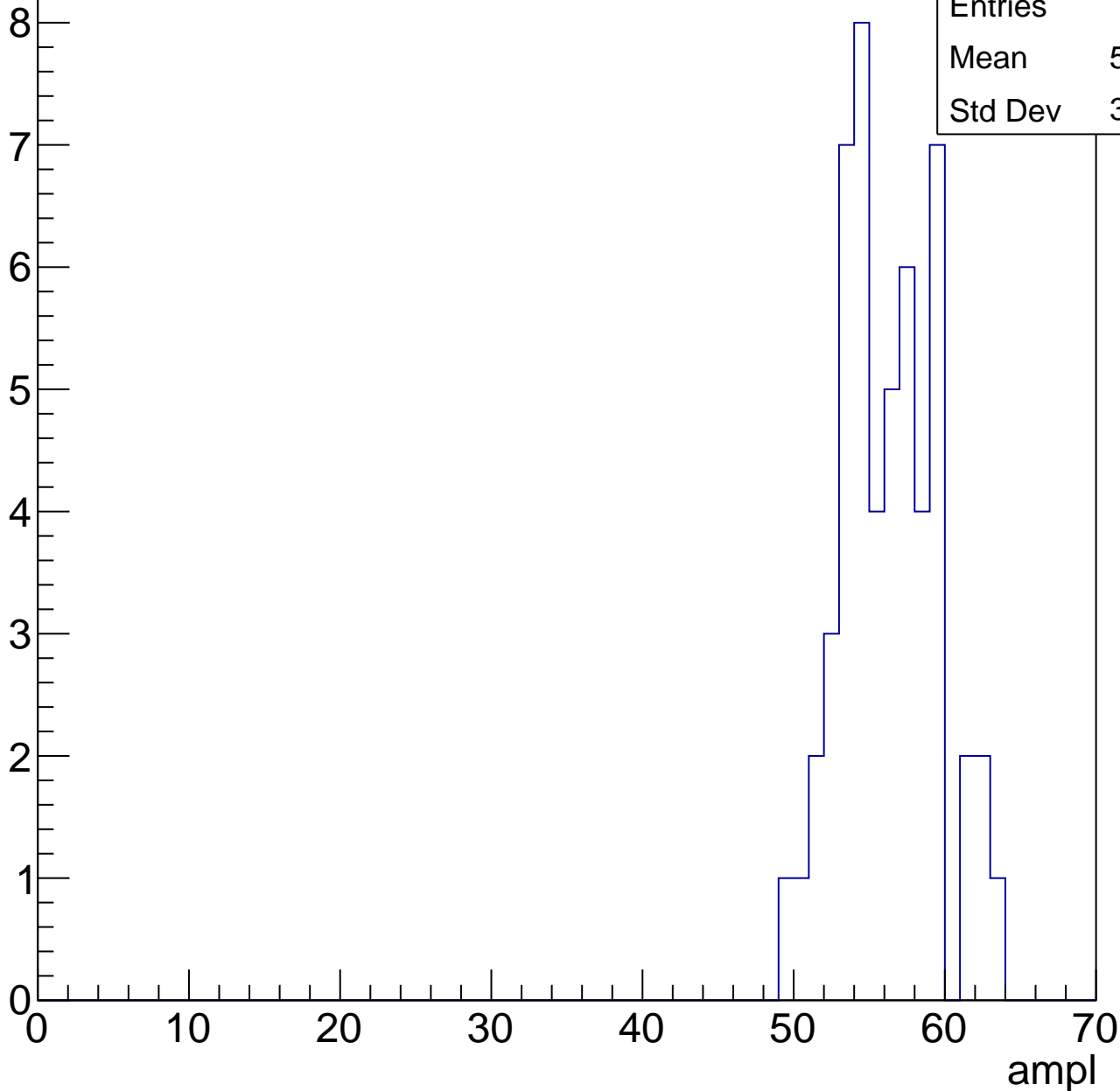


# B1L102S, U8-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	55.77
Std Dev	3.178

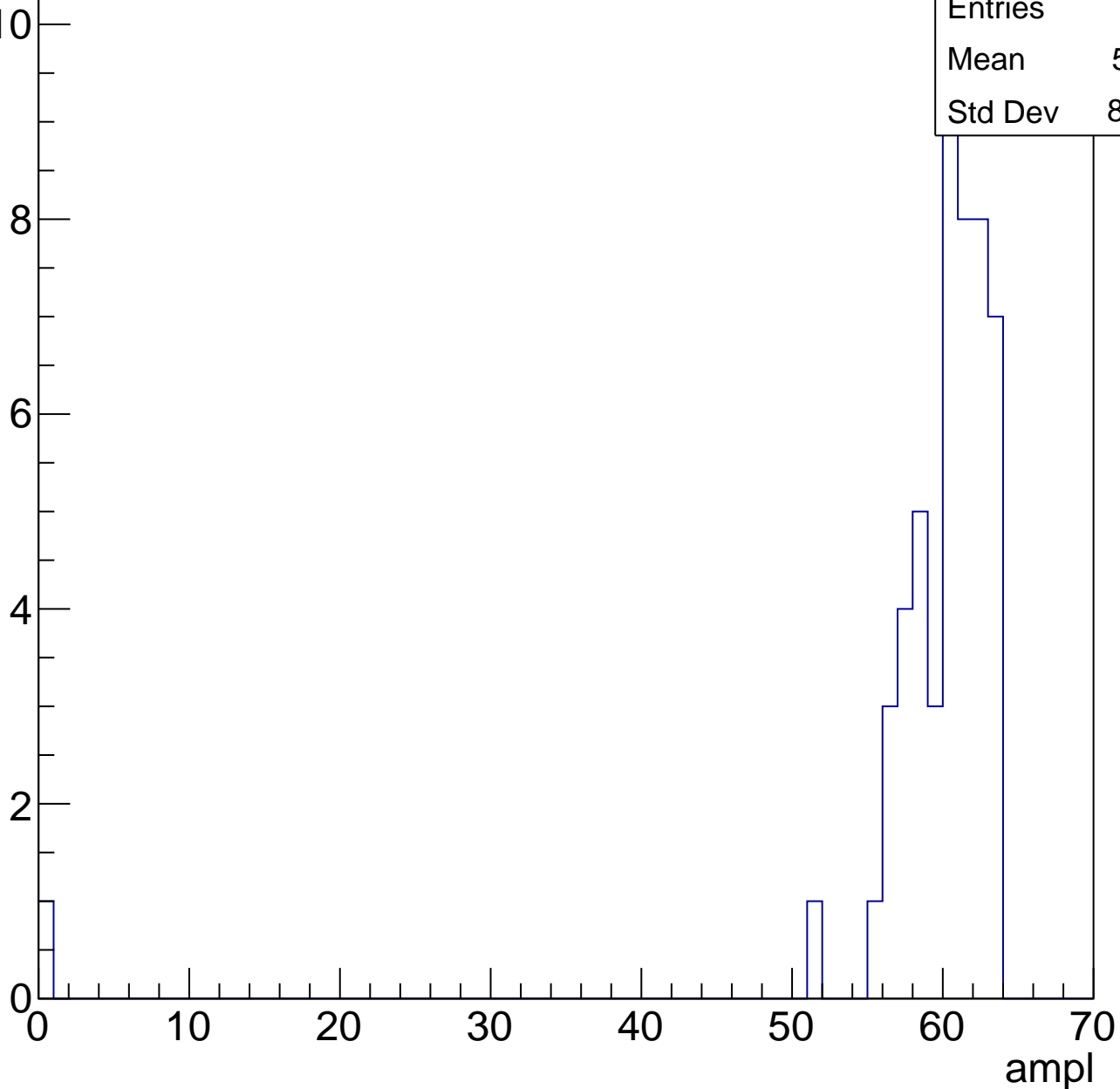


# B1L102S, U8-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	58.71
Std Dev	8.667



# B1L102S, U8-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch102, adc0

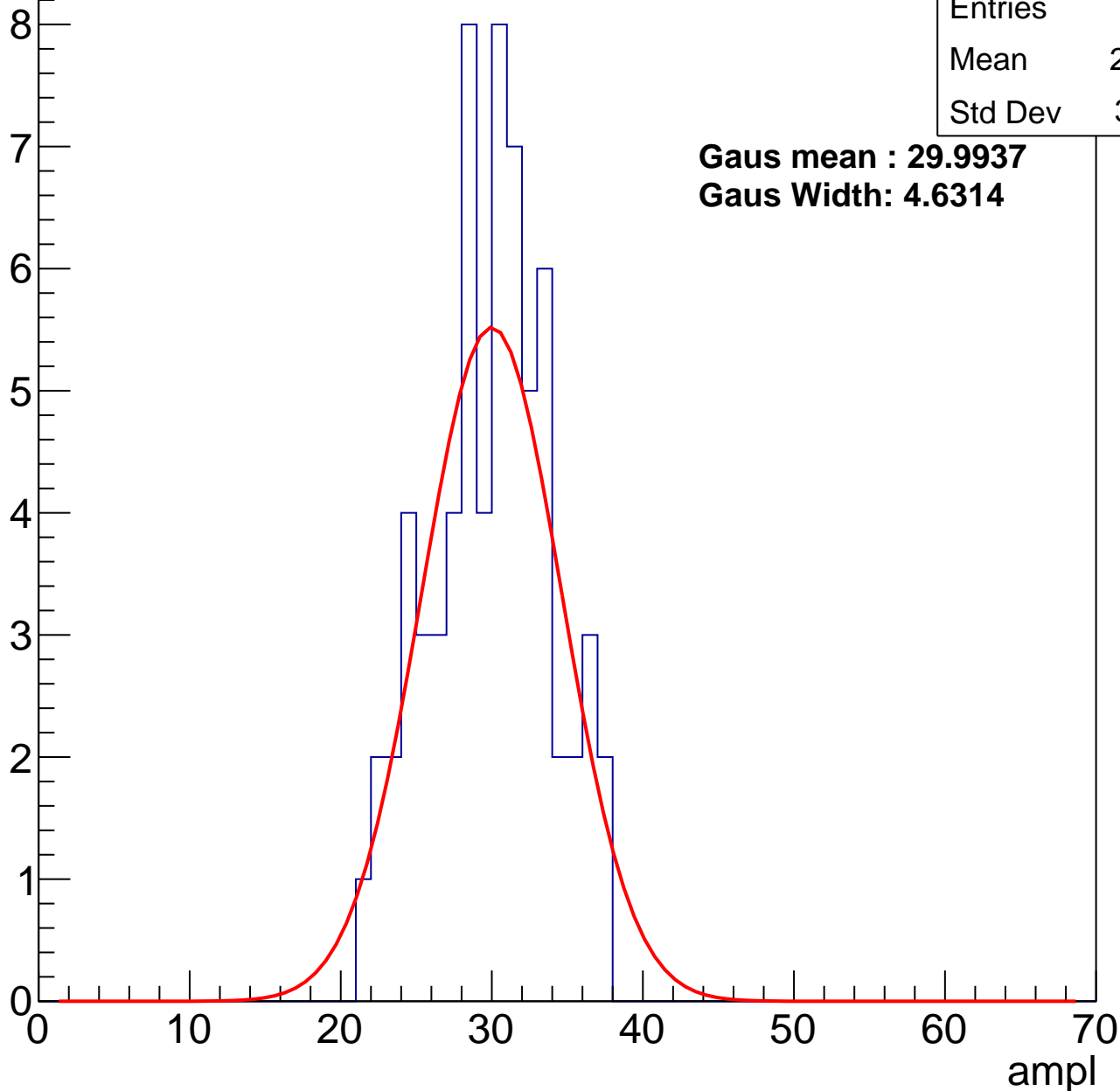
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	29.44
Std Dev	3.881

**Gaus mean : 29.9937**

**Gaus Width: 4.6314**



# B1L102S, U8-ch102, adc1

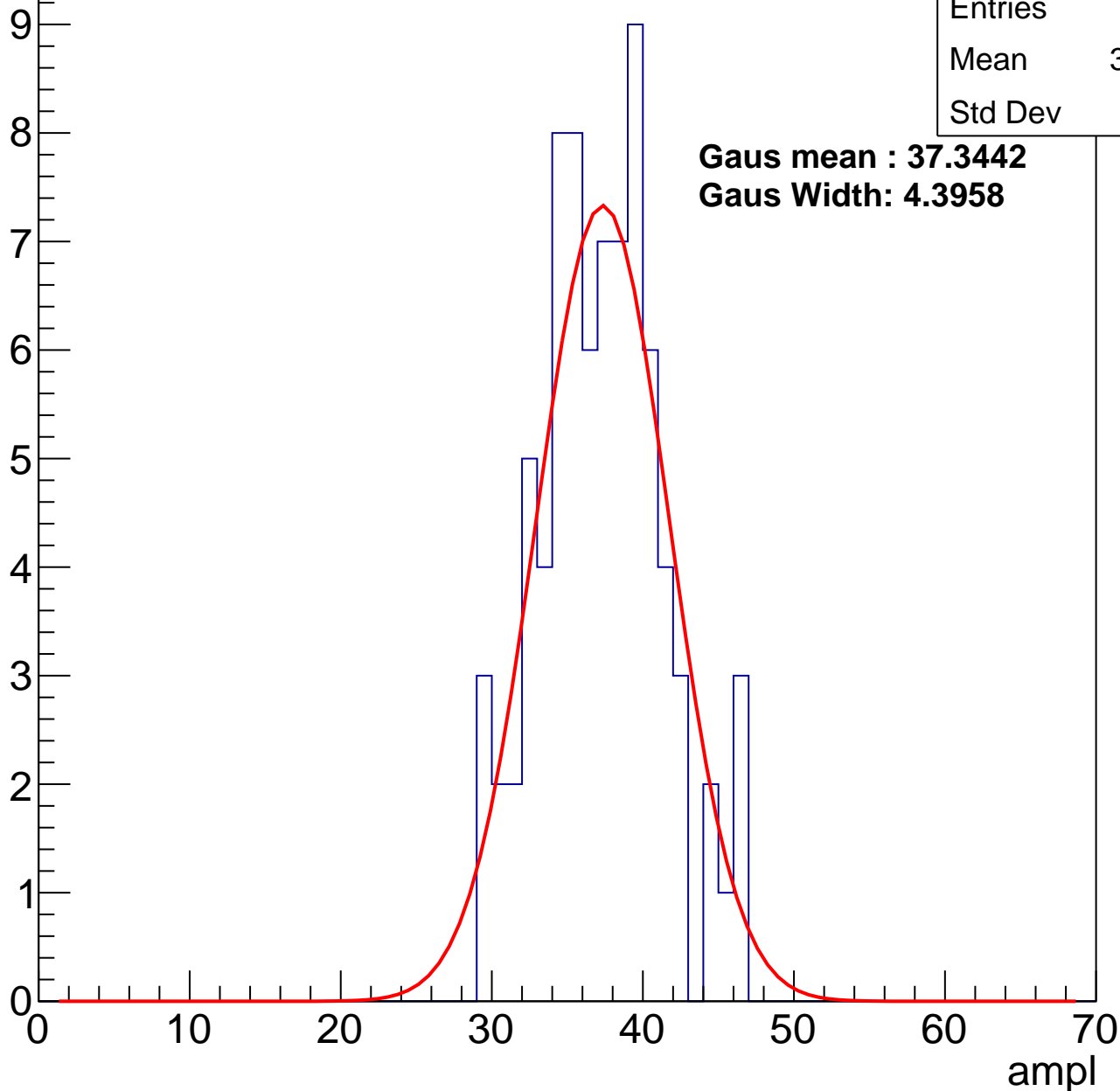
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	36.83
Std Dev	4.03

**Gaus mean : 37.3442**

**Gaus Width: 4.3958**



# B1L102S, U8-ch102, adc2

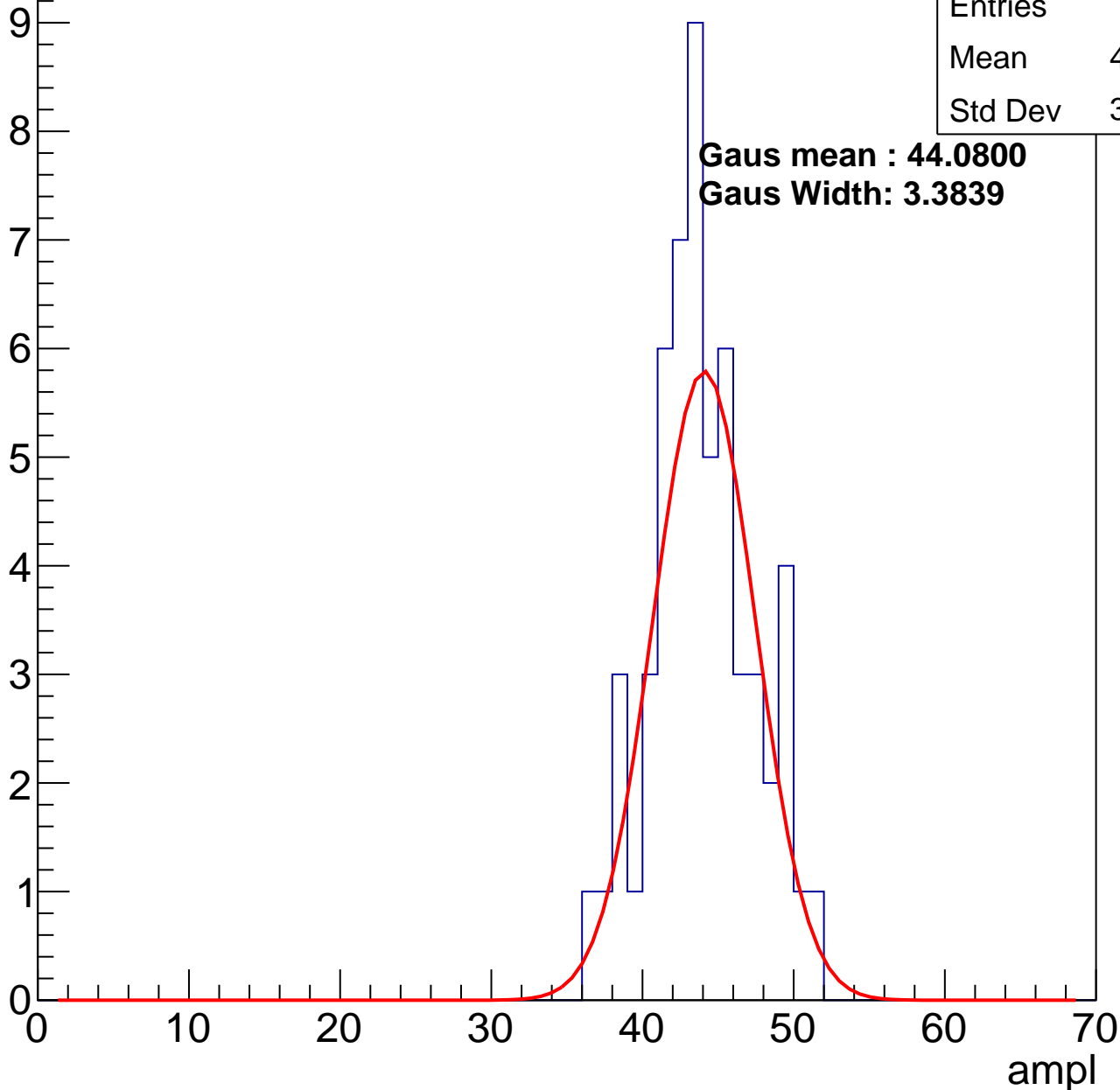
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	43.48
Std Dev	3.359

**Gaus mean : 44.0800**

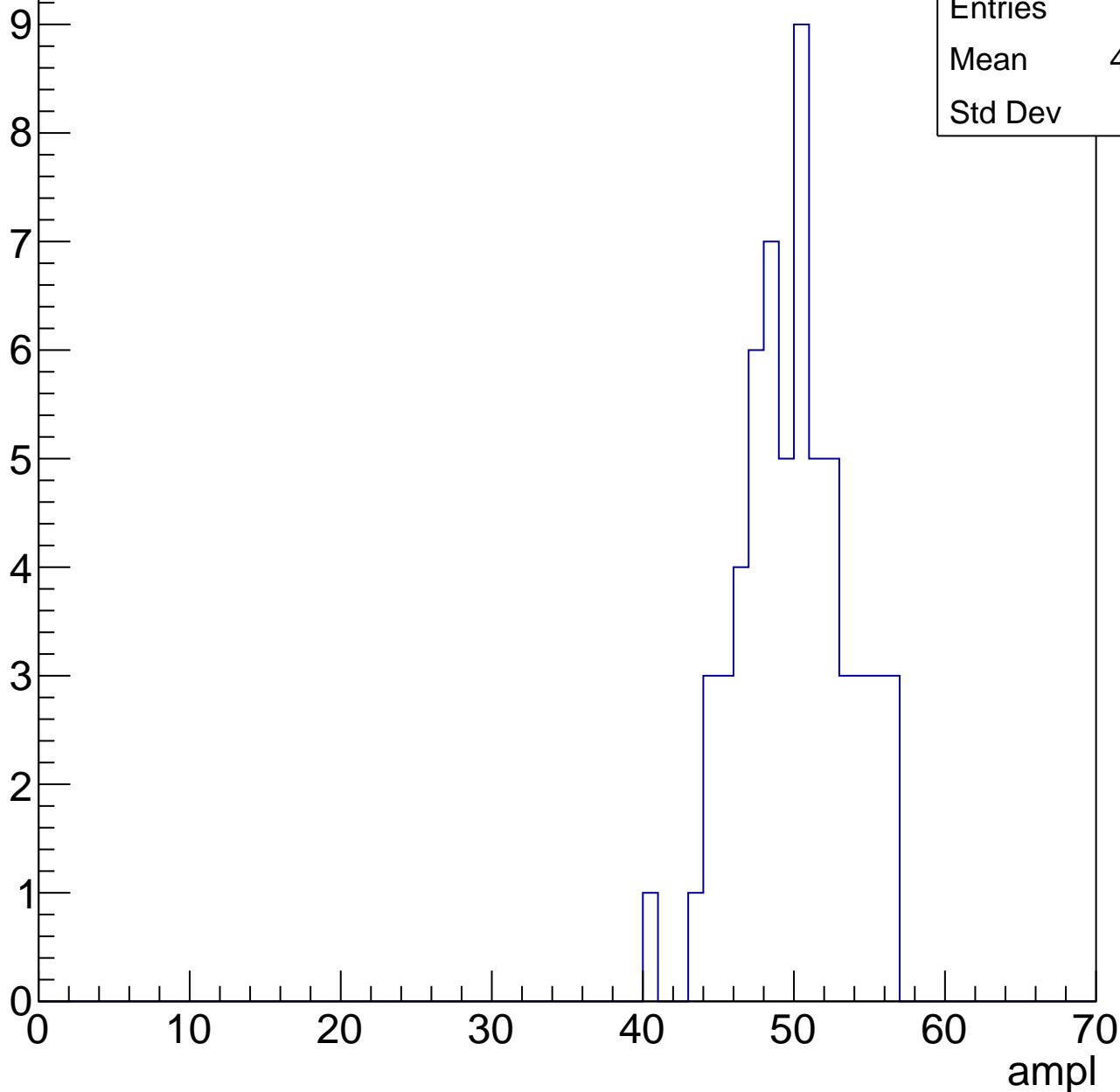
**Gaus Width: 3.3839**



# B1L102S, U8-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



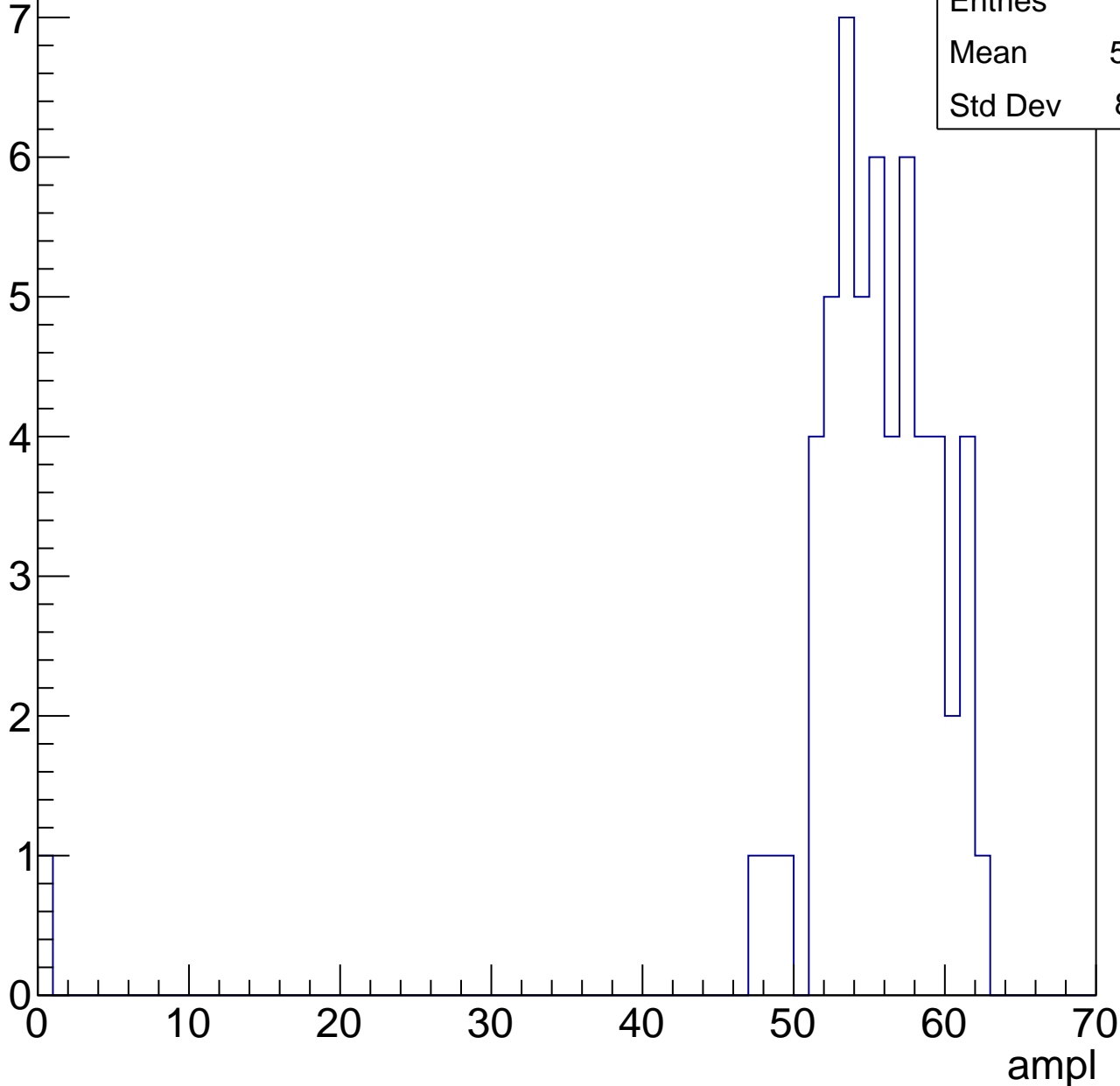
Entries	61
Mean	49.44
Std Dev	3.5

# B1L102S, U8-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	54.27
Std Dev	8.081



# B1L102S, U8-ch102, adc5

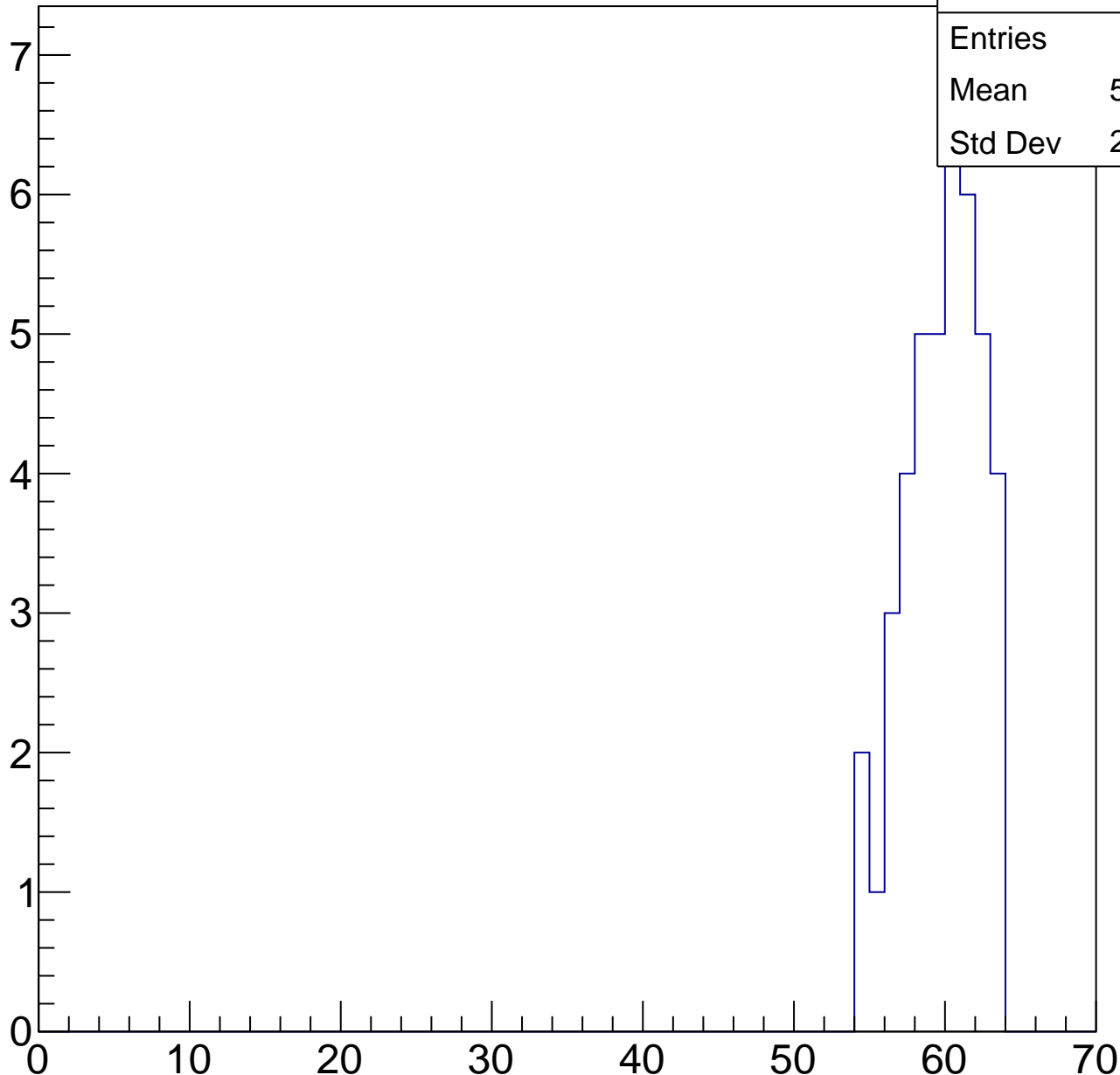
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	42
Mean	59.33
Std Dev	2.436

ampl

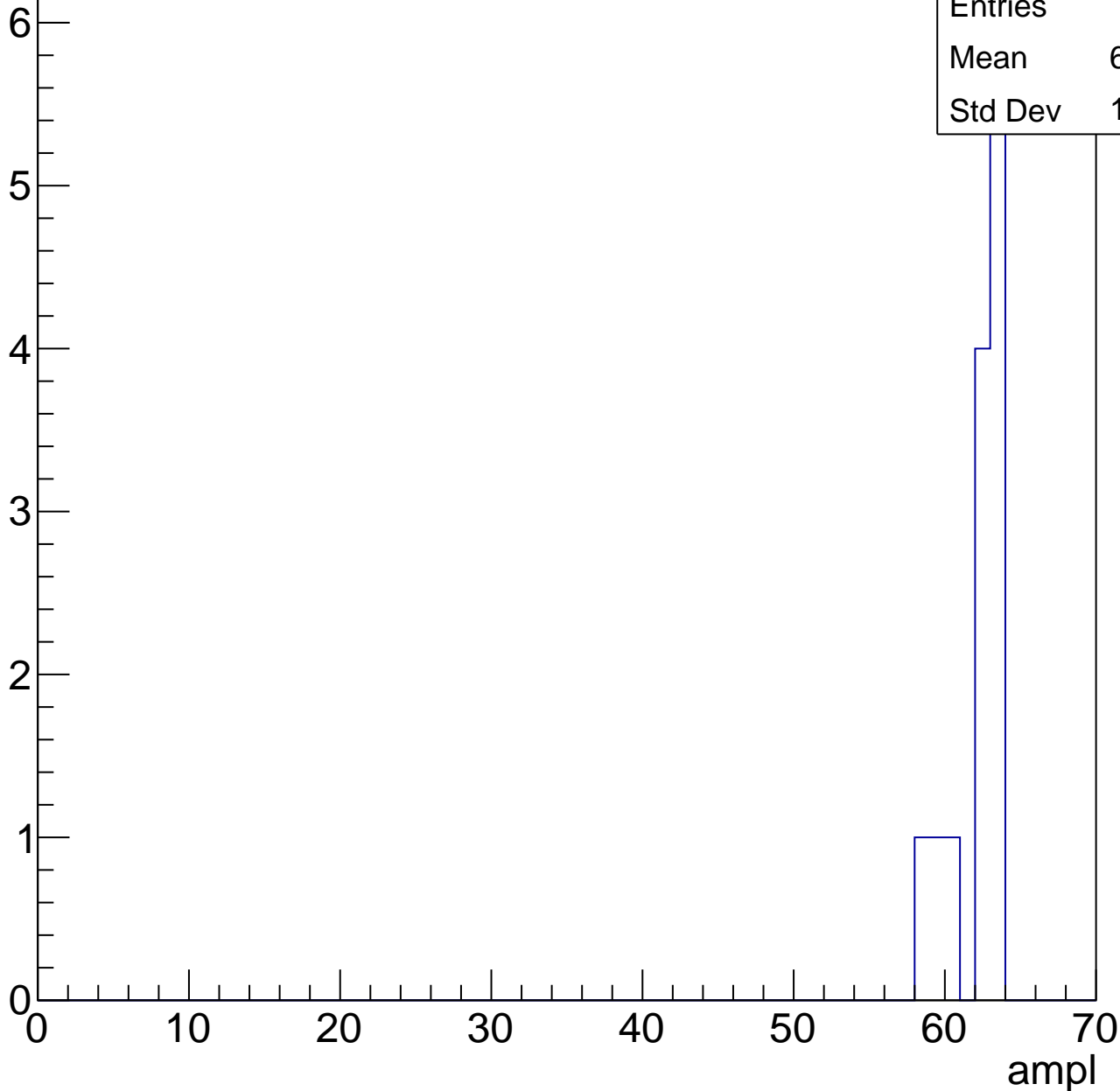


# B1L102S, U8-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	13
Mean	61.77
Std Dev	1.625





# B1L102S, U8-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U8-ch103, adc0

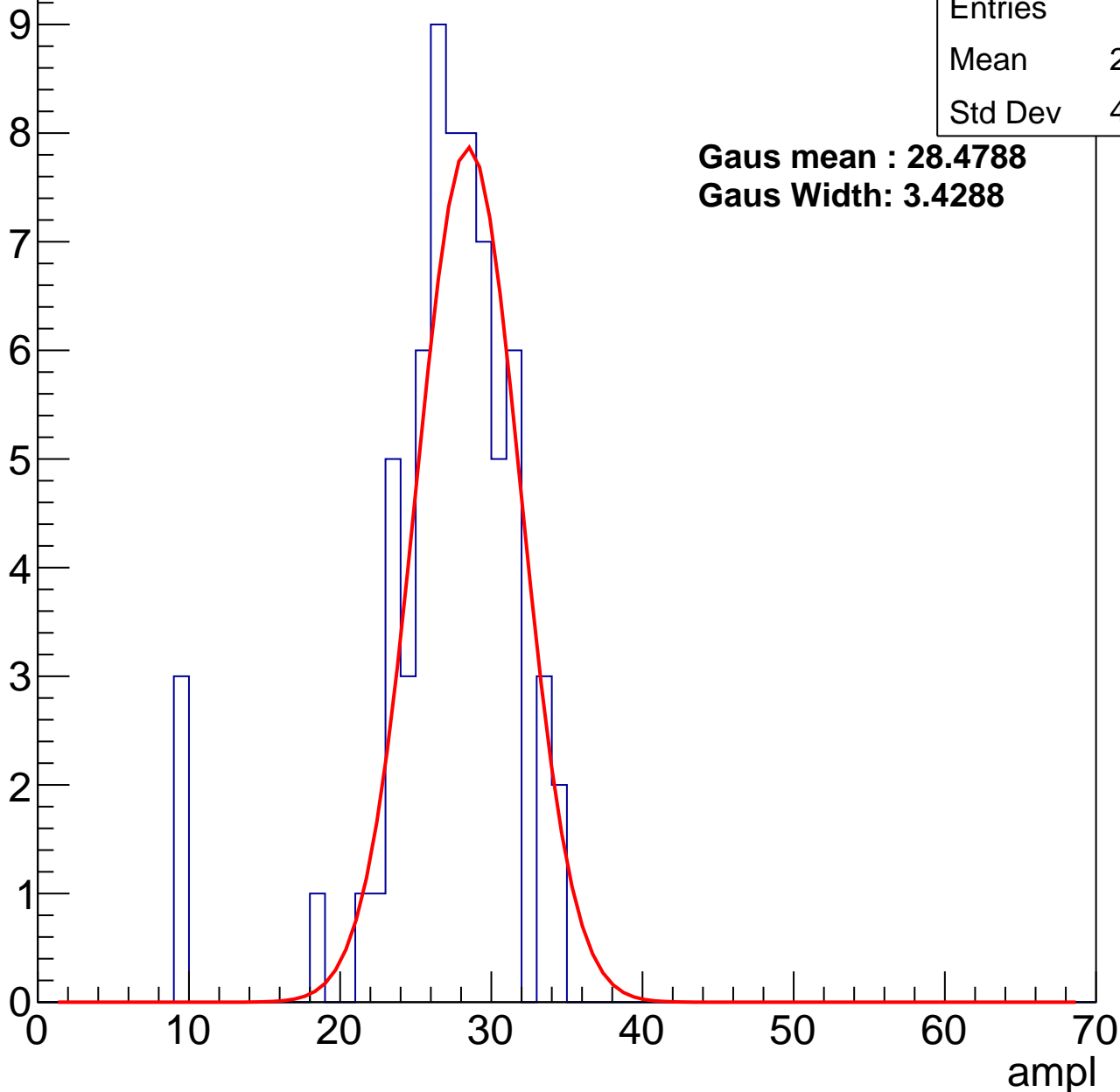
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	26.54
Std Dev	4.885

**Gaus mean : 28.4788**

**Gaus Width: 3.4288**



# B1L102S, U8-ch103, adc1

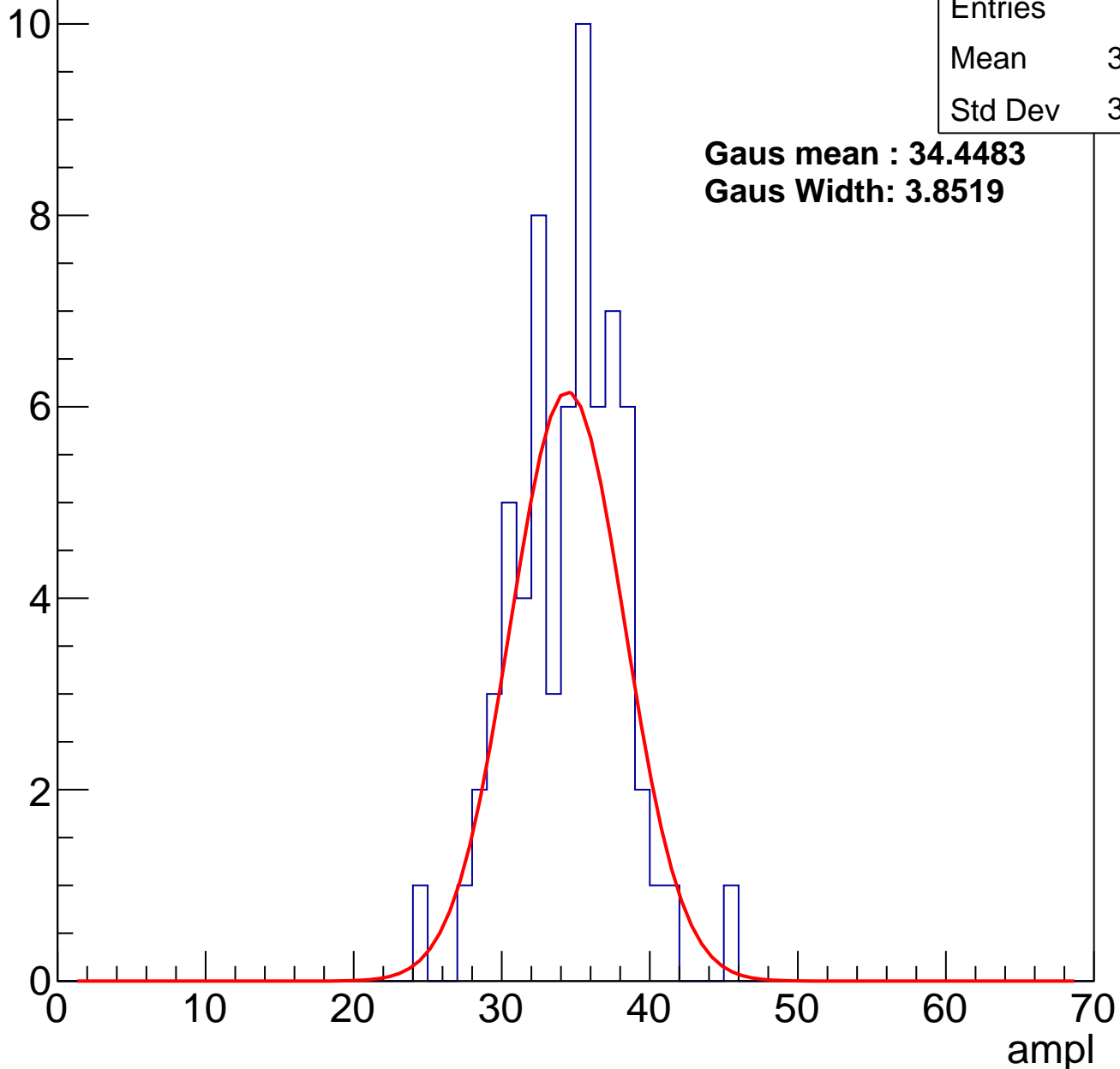
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	67
Mean	34.09
Std Dev	3.656

**Gaus mean : 34.4483**

**Gaus Width: 3.8519**

Entry



# B1L102S, U8-ch103, adc2

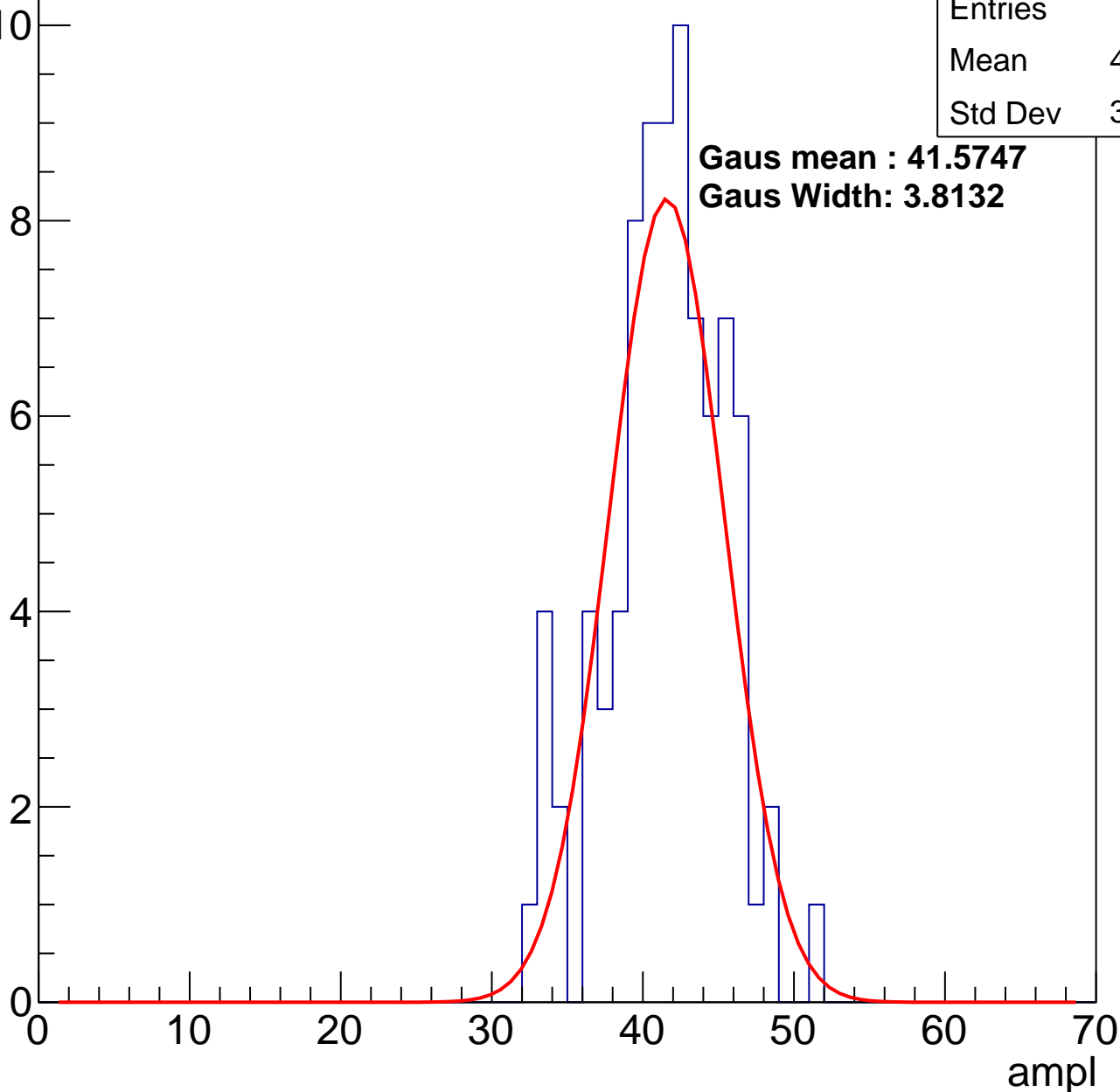
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	41.07
Std Dev	3.854

**Gaus mean : 41.5747**

**Gaus Width: 3.8132**

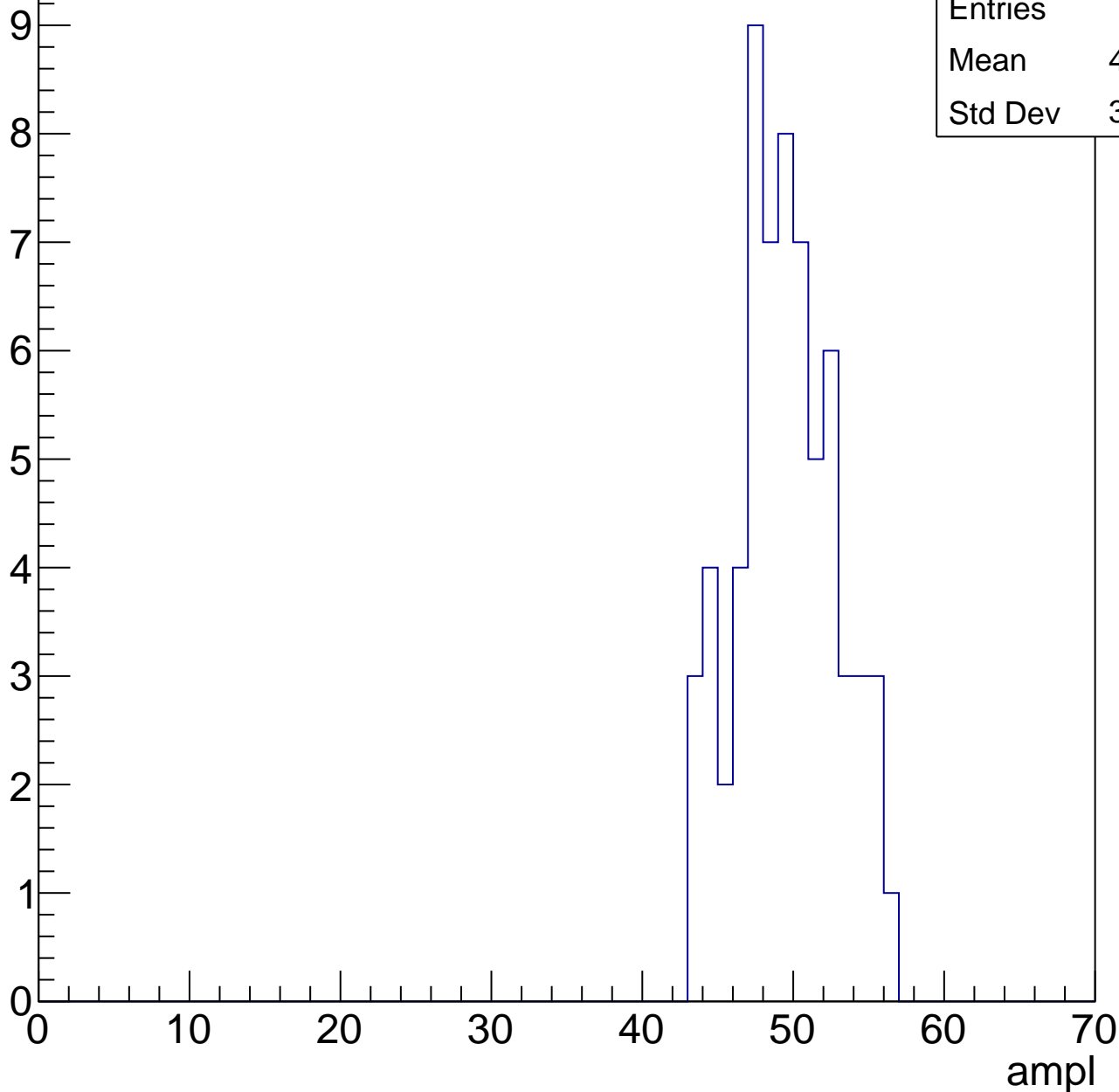


# B1L102S, U8-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	49.06
Std Dev	3.234

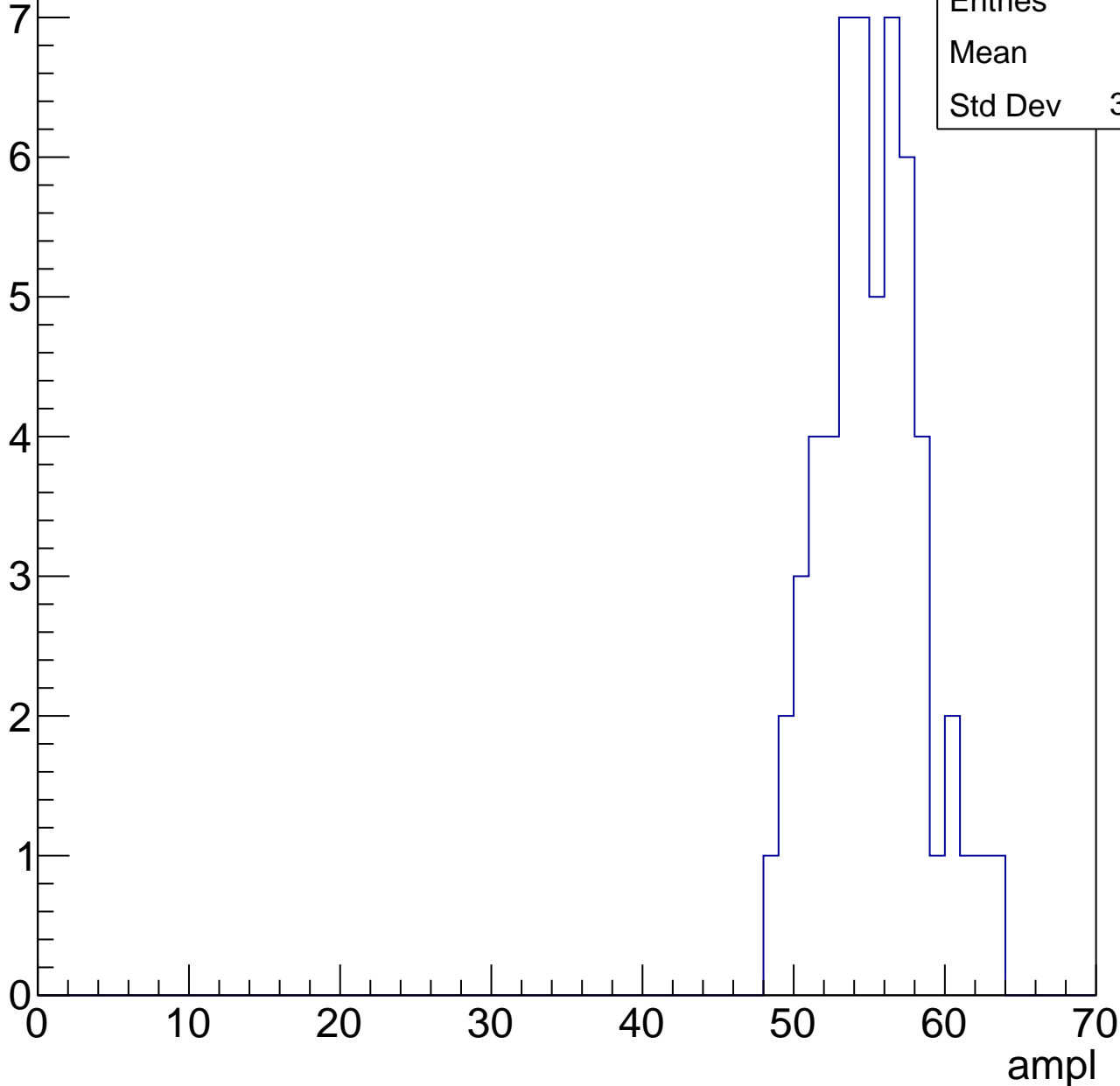


# B1L102S, U8-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	54.7
Std Dev	3.295



# B1L102S, U8-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	50
Mean	58.52
Std Dev	8.628

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

7

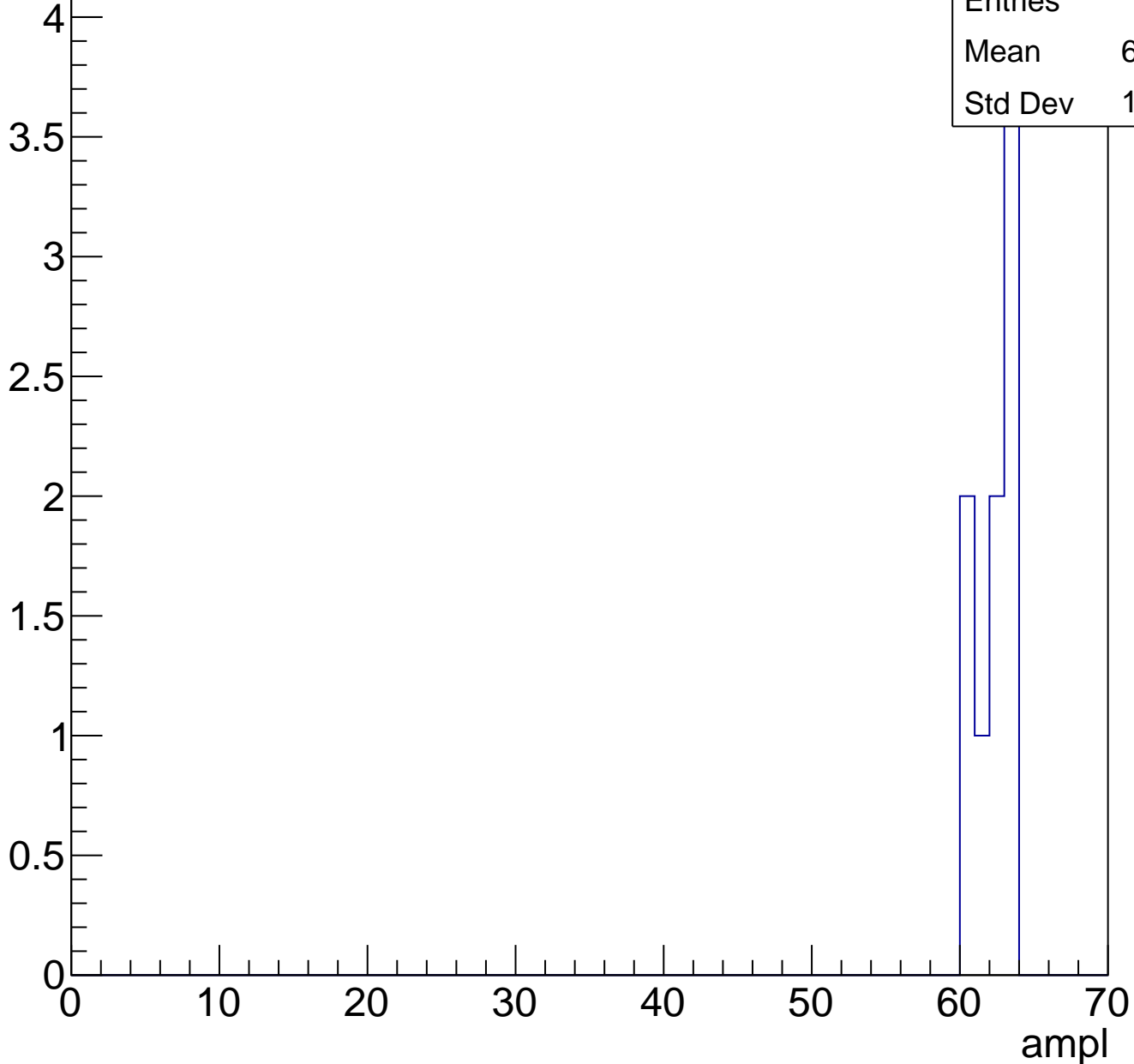
8

9

# B1L102S, U8-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch104, adc0

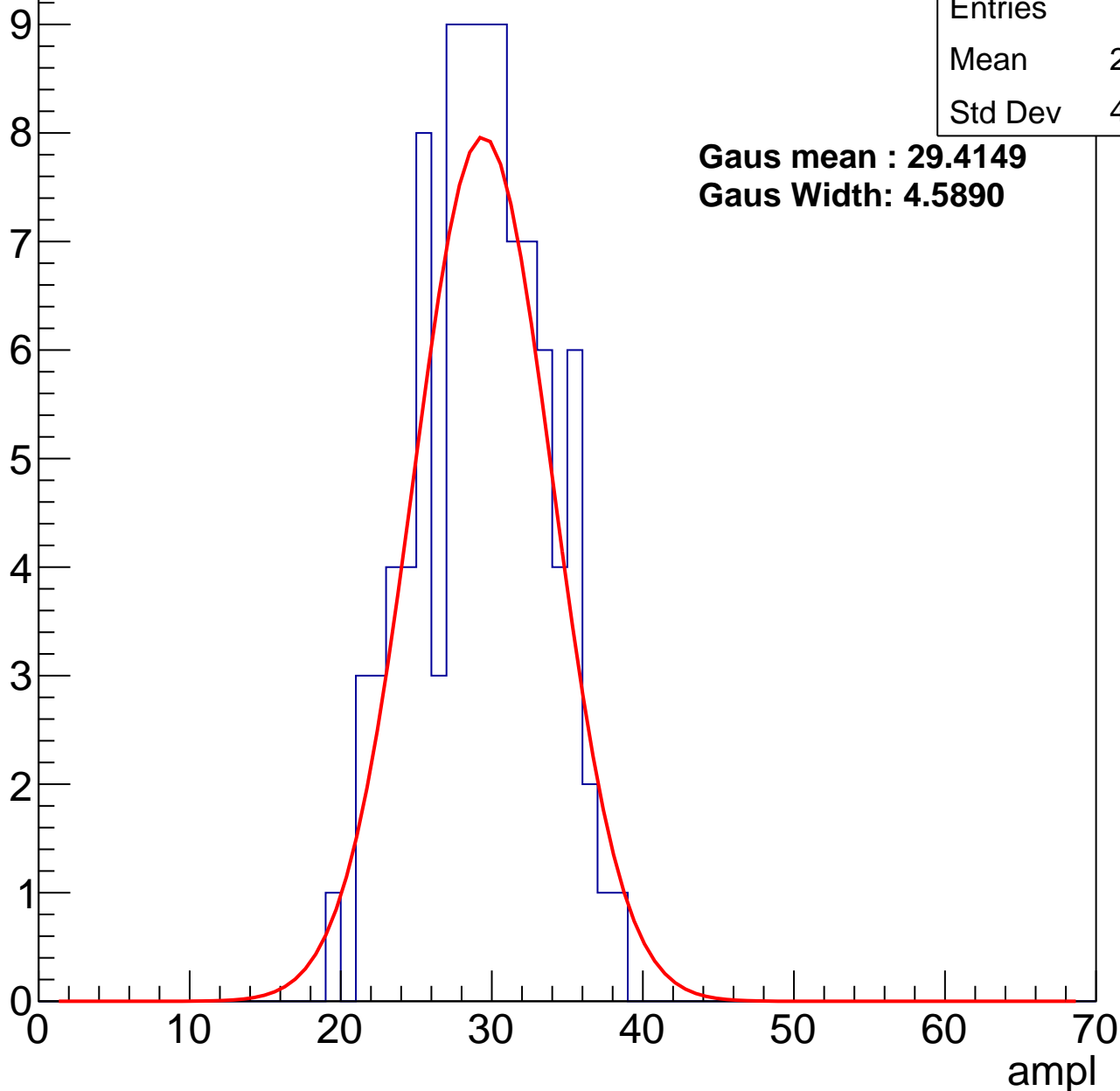
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	96
Mean	28.88
Std Dev	4.129

**Gaus mean : 29.4149**

**Gaus Width: 4.5890**



# B1L102S, U8-ch104, adc1

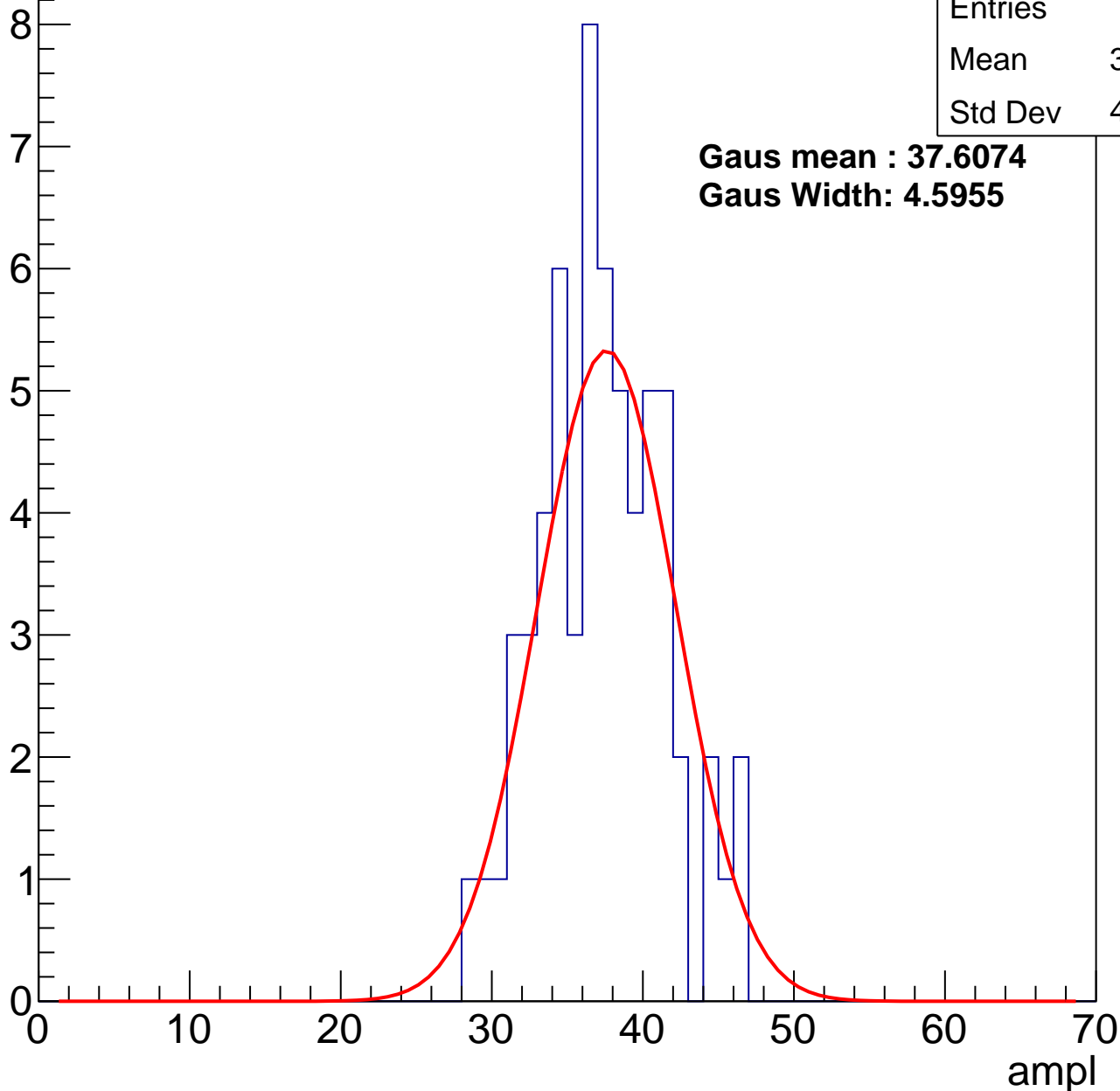
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	36.89
Std Dev	4.084

**Gaus mean : 37.6074**

**Gaus Width: 4.5955**



# B1L102S, U8-ch104, adc2

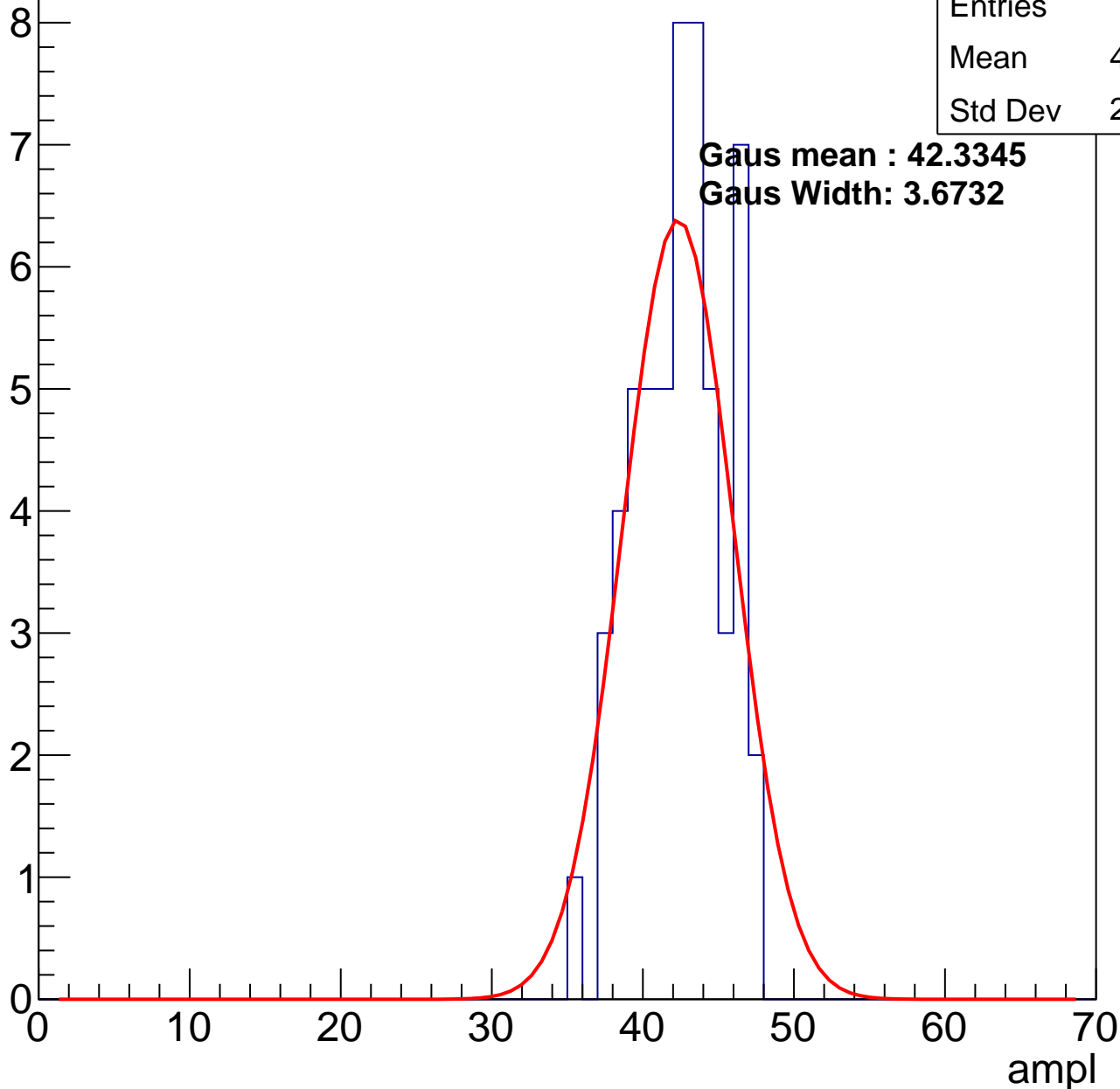
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	41.95
Std Dev	2.912

**Gaus mean : 42.3345**

**Gaus Width: 3.6732**

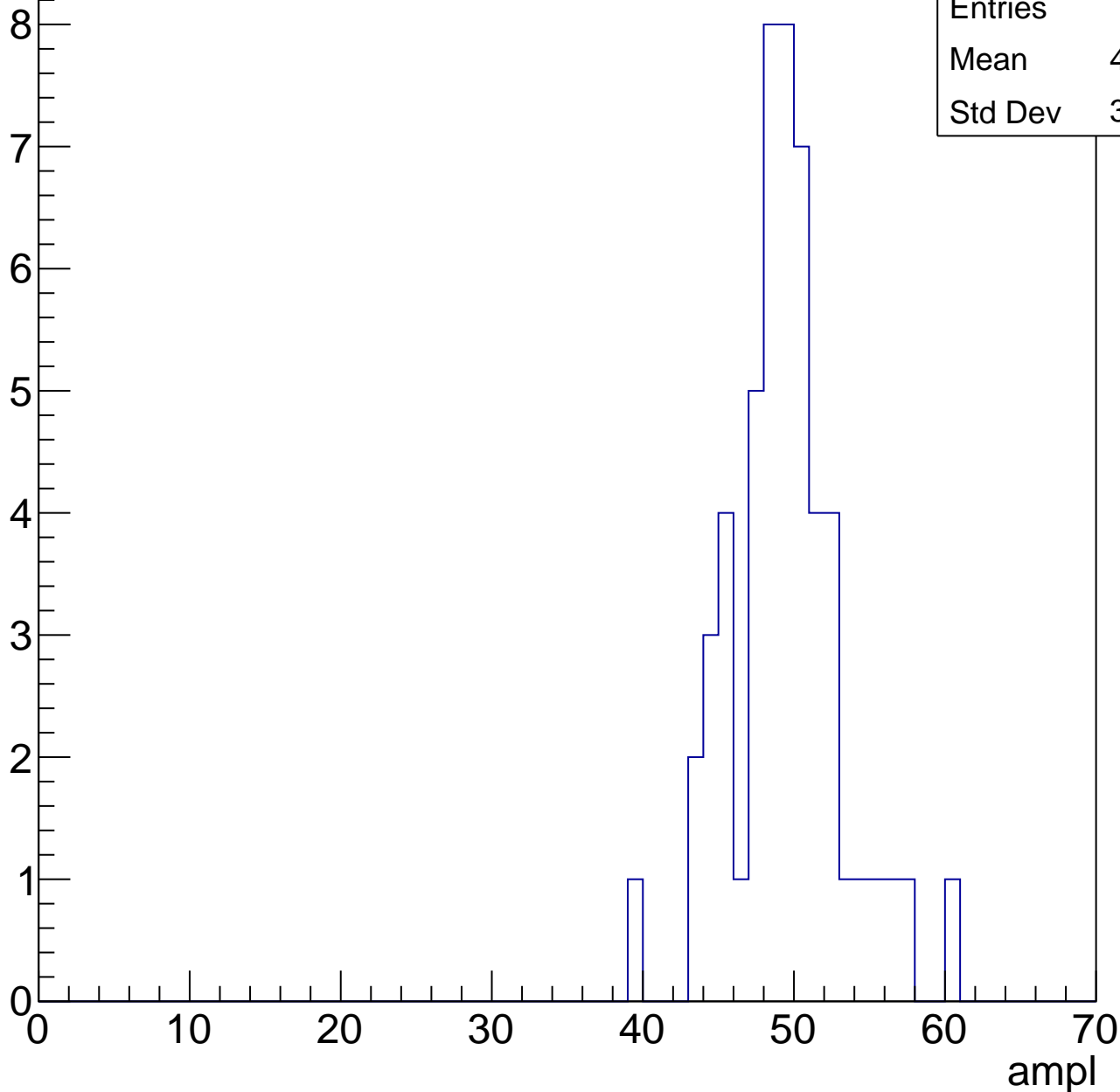


# B1L102S, U8-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	48.89
Std Dev	3.679

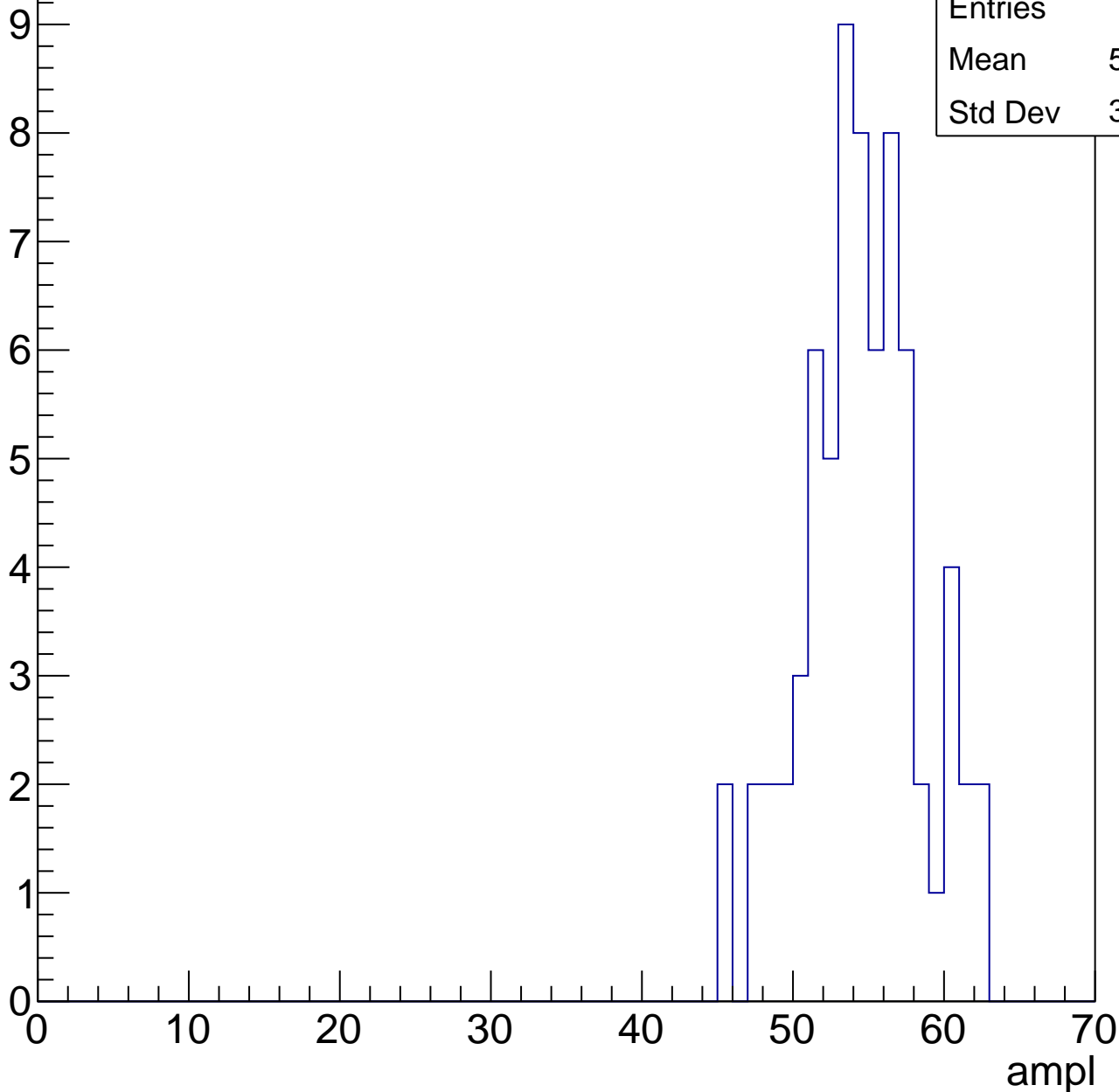


# B1L102S, U8-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	54.06
Std Dev	3.839

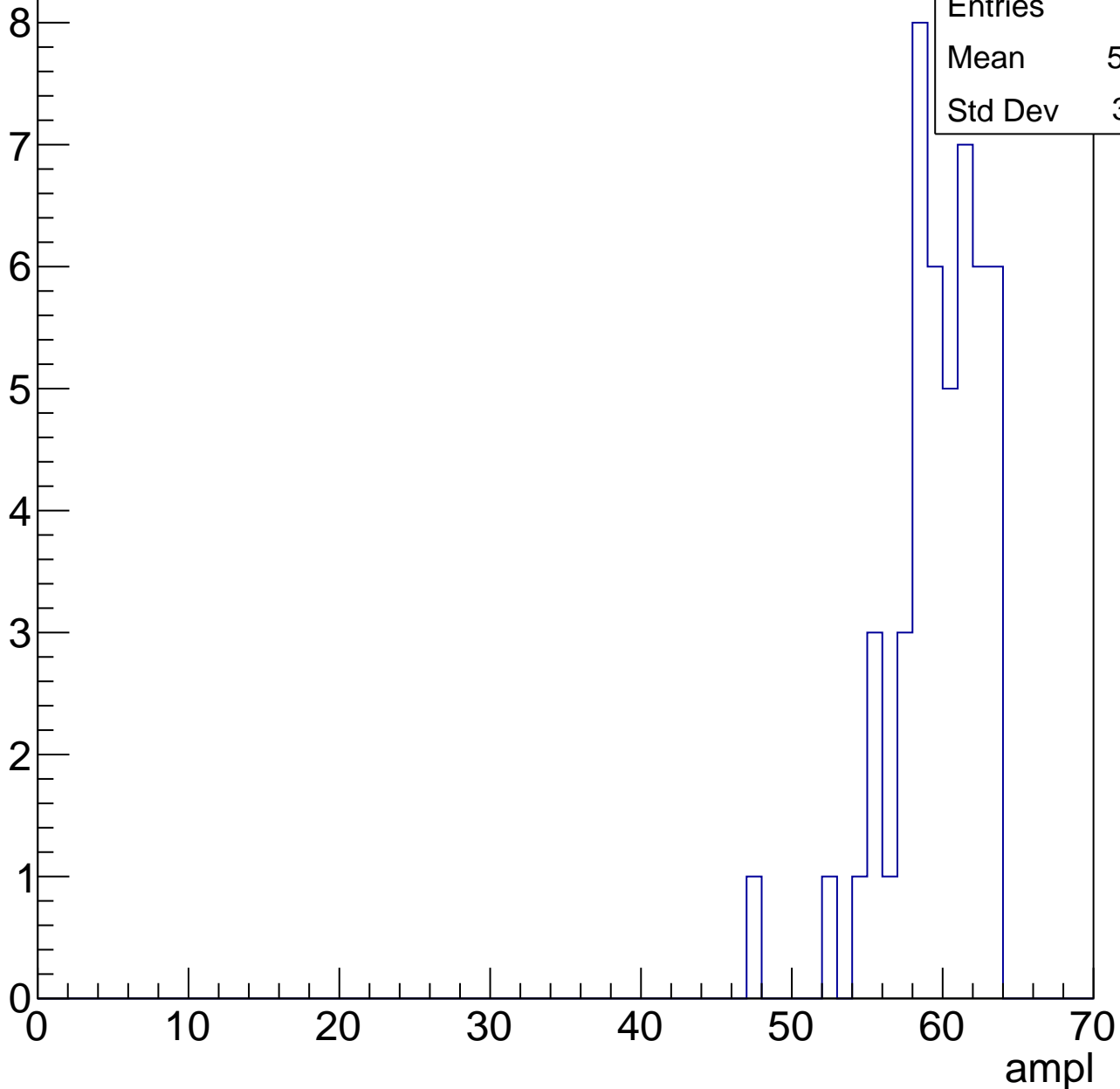


# B1L102S, U8-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

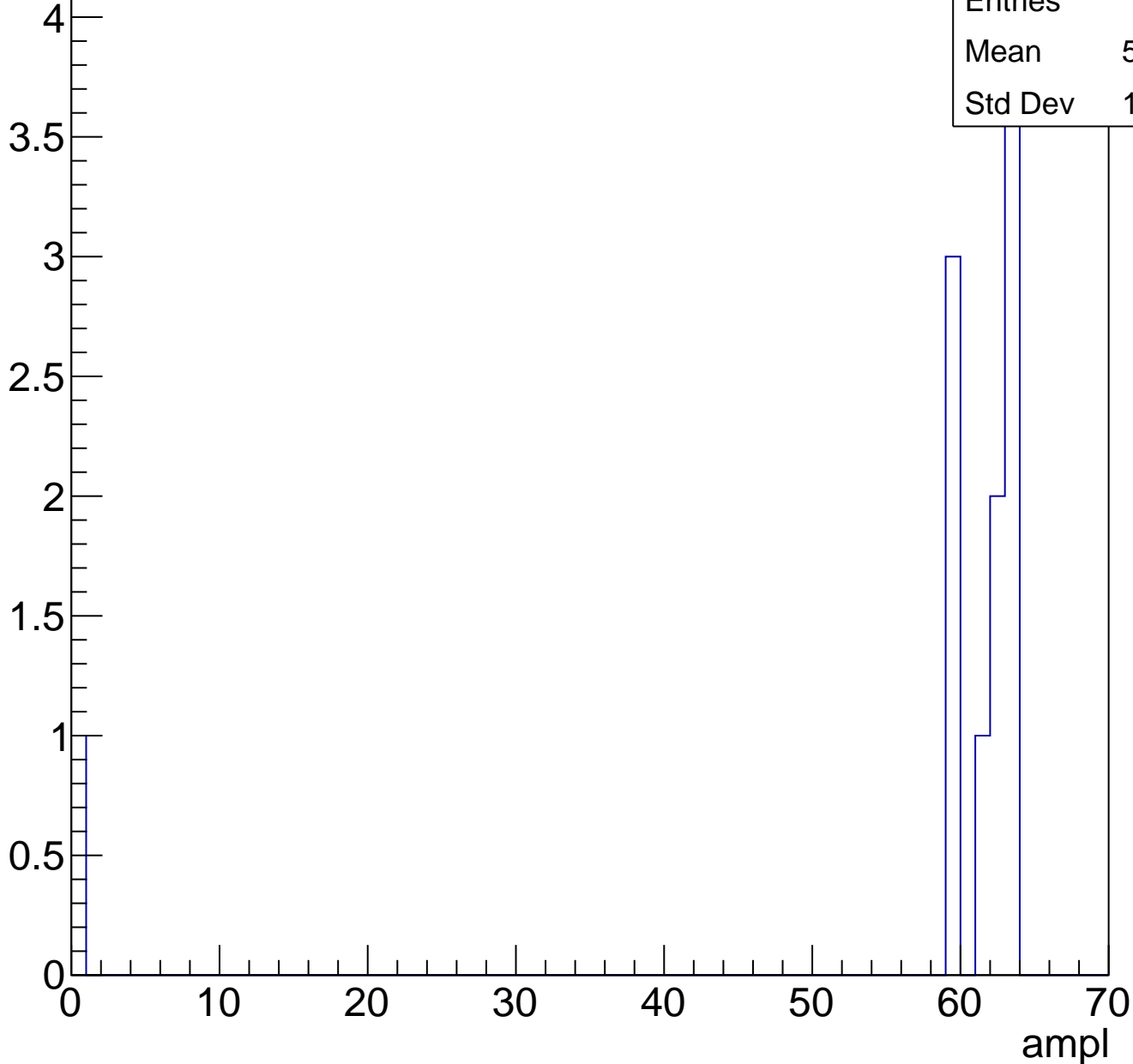
Entries	48
Mean	59.17
Std Dev	3.151



# B1L102S, U8-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch105, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	83
Mean	29.78
Std Dev	5.996

**Gaus mean : 30.6123**

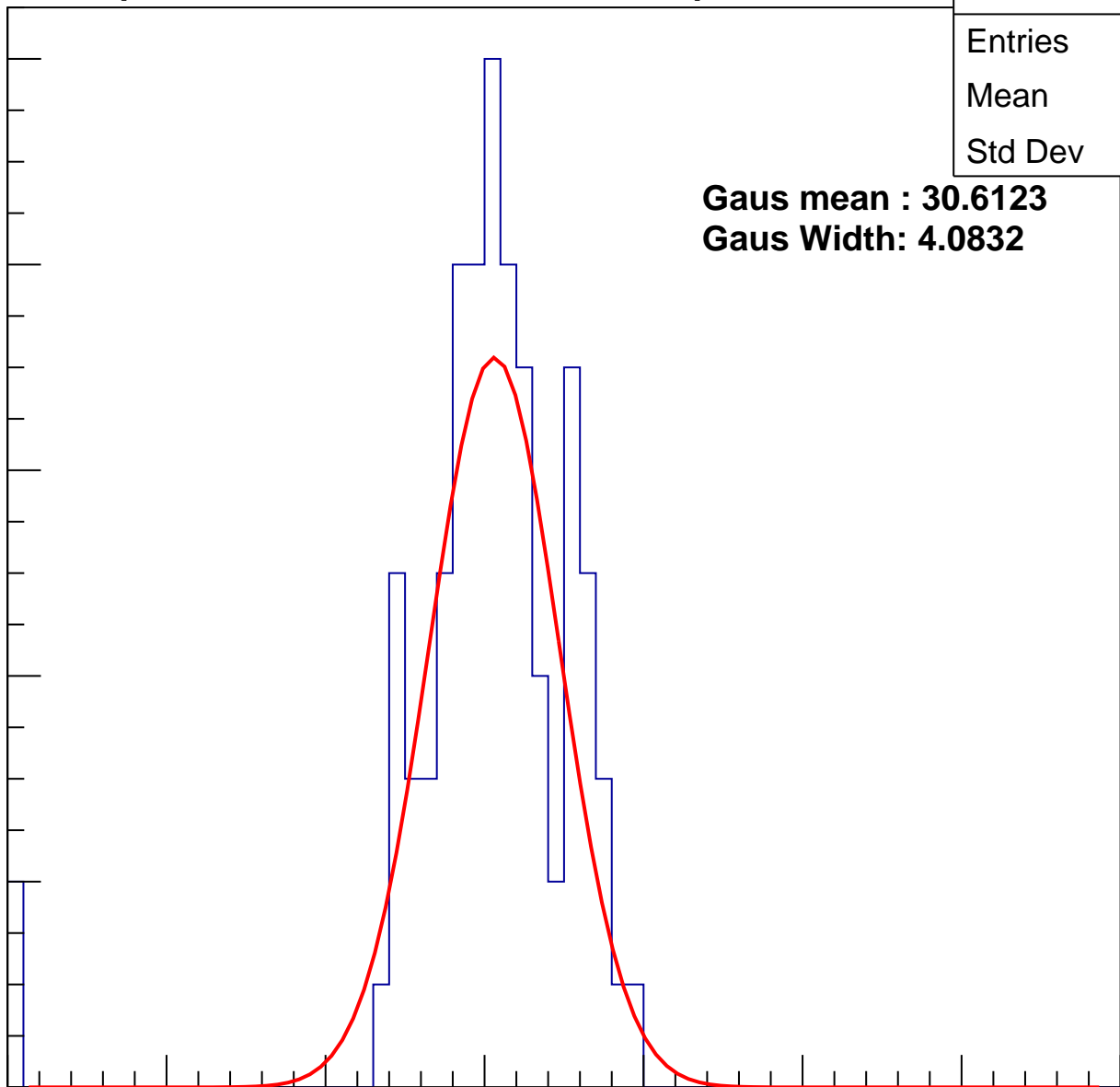
**Gaus Width: 4.0832**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U8-ch105, adc1

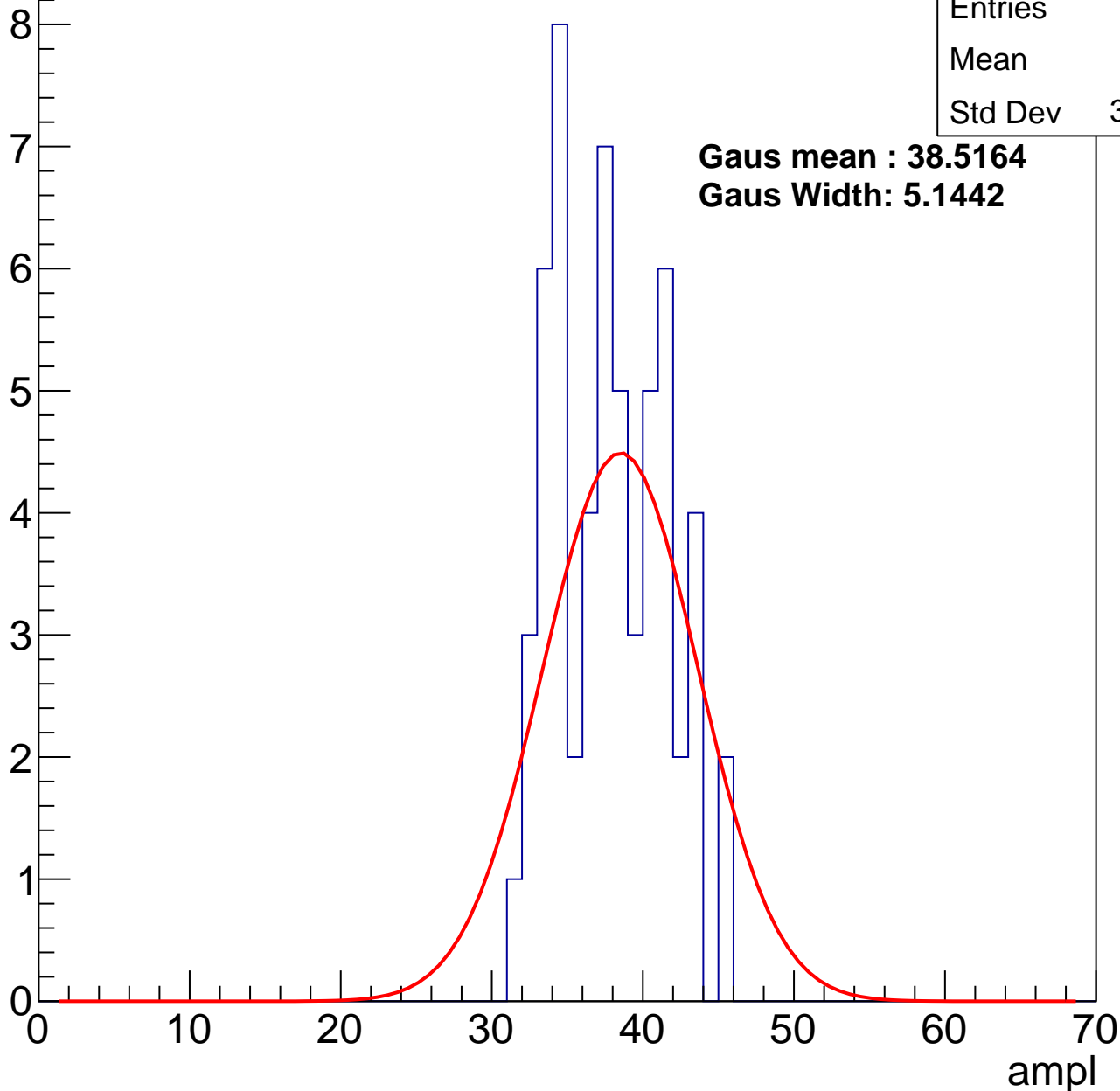
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	37.4
Std Dev	3.624

**Gaus mean : 38.5164**

**Gaus Width: 5.1442**



# B1L102S, U8-ch105, adc2

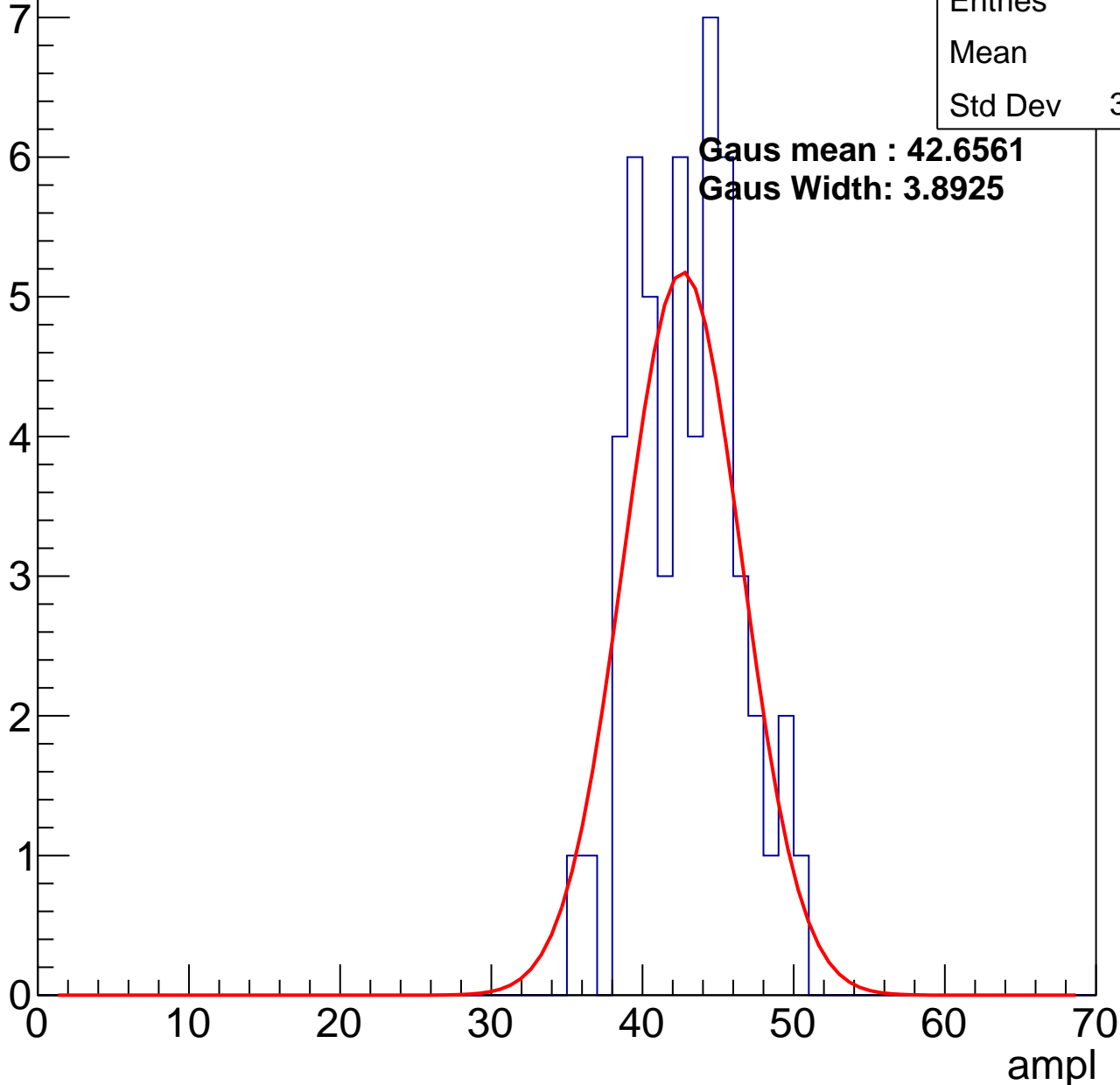
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	42.5
Std Dev	3.383

**Gaus mean : 42.6561**

**Gaus Width: 3.8925**

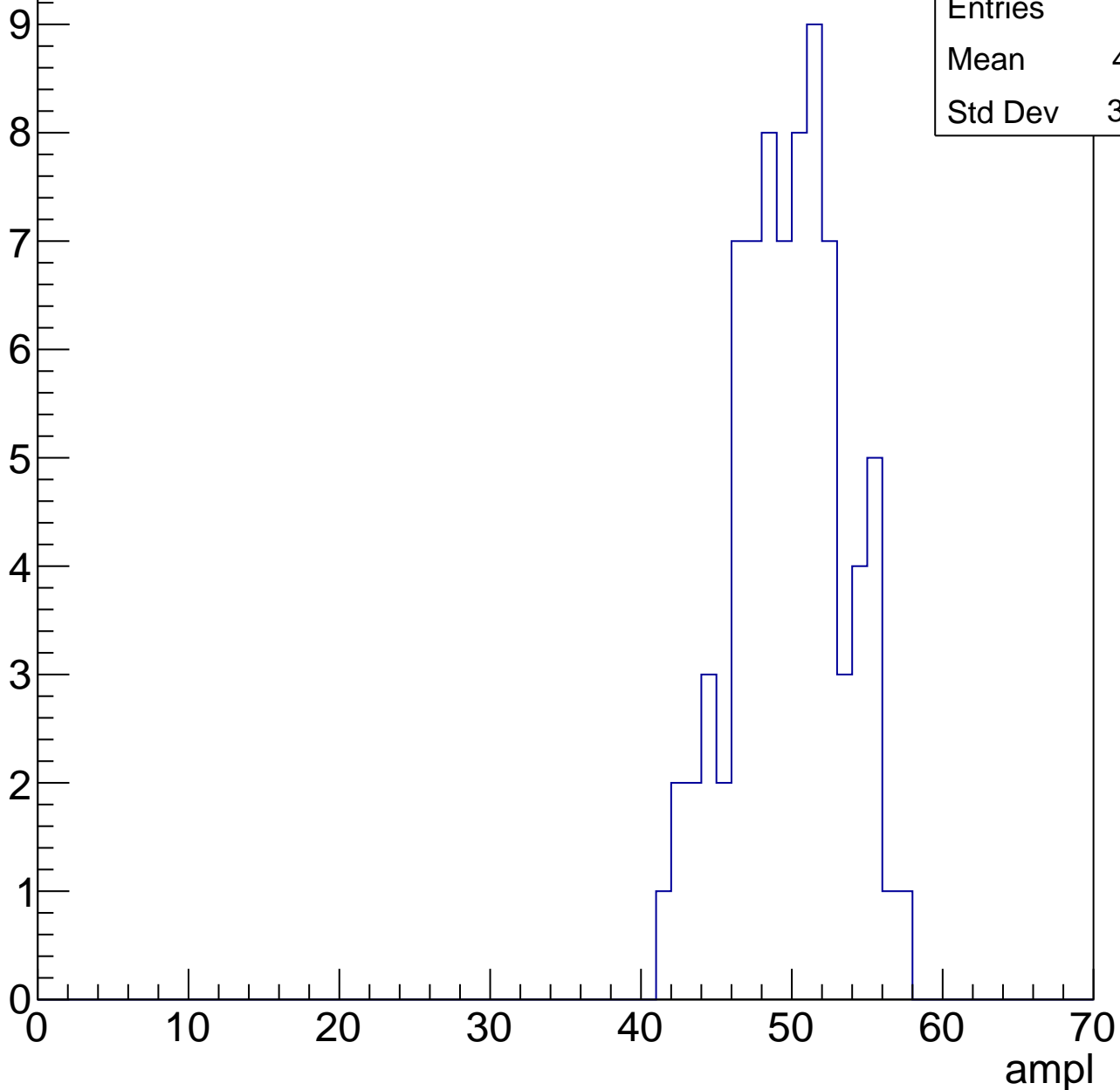


# B1L102S, U8-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

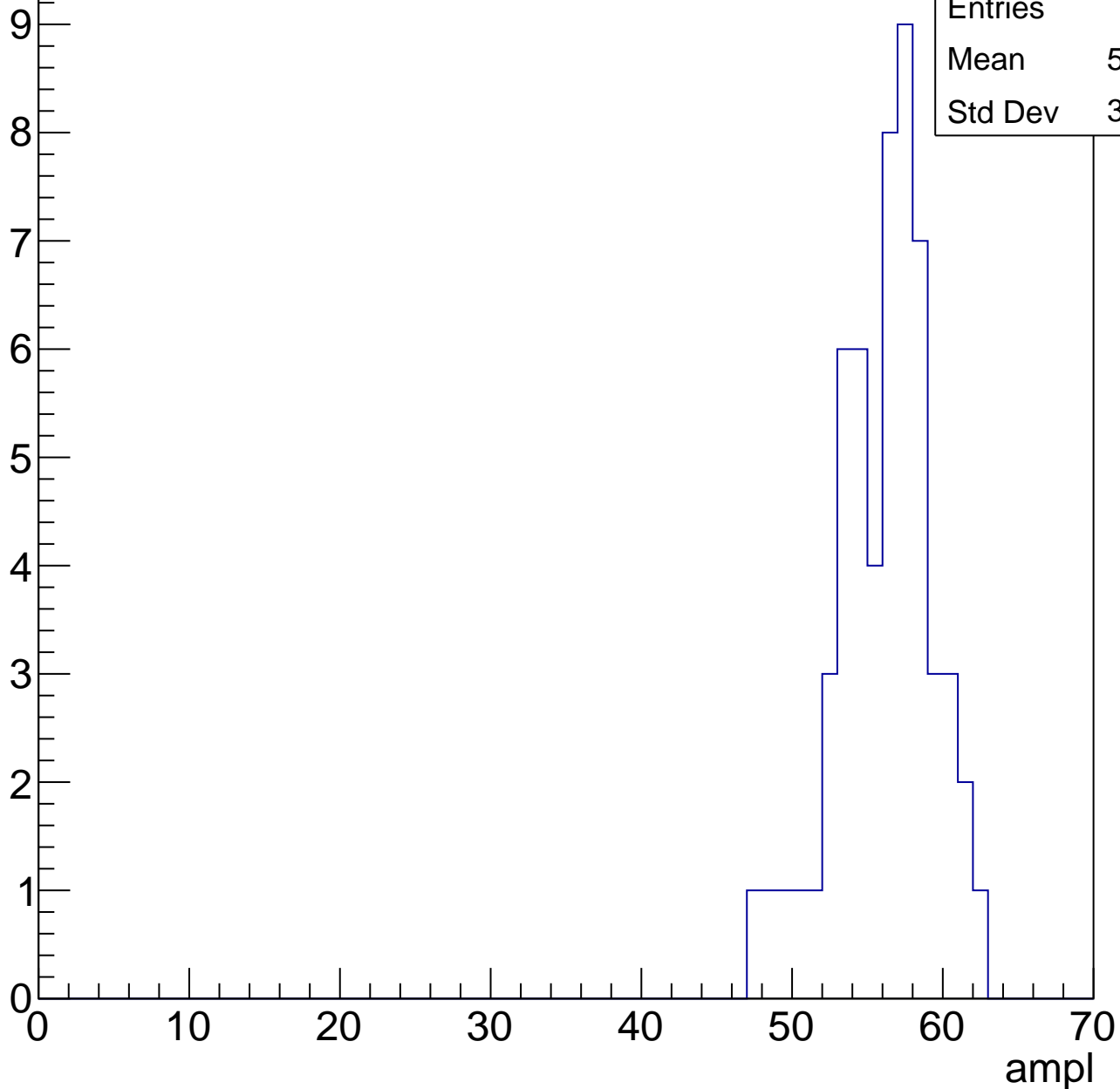
Entries	77
Mean	49.31
Std Dev	3.568



# B1L102S, U8-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



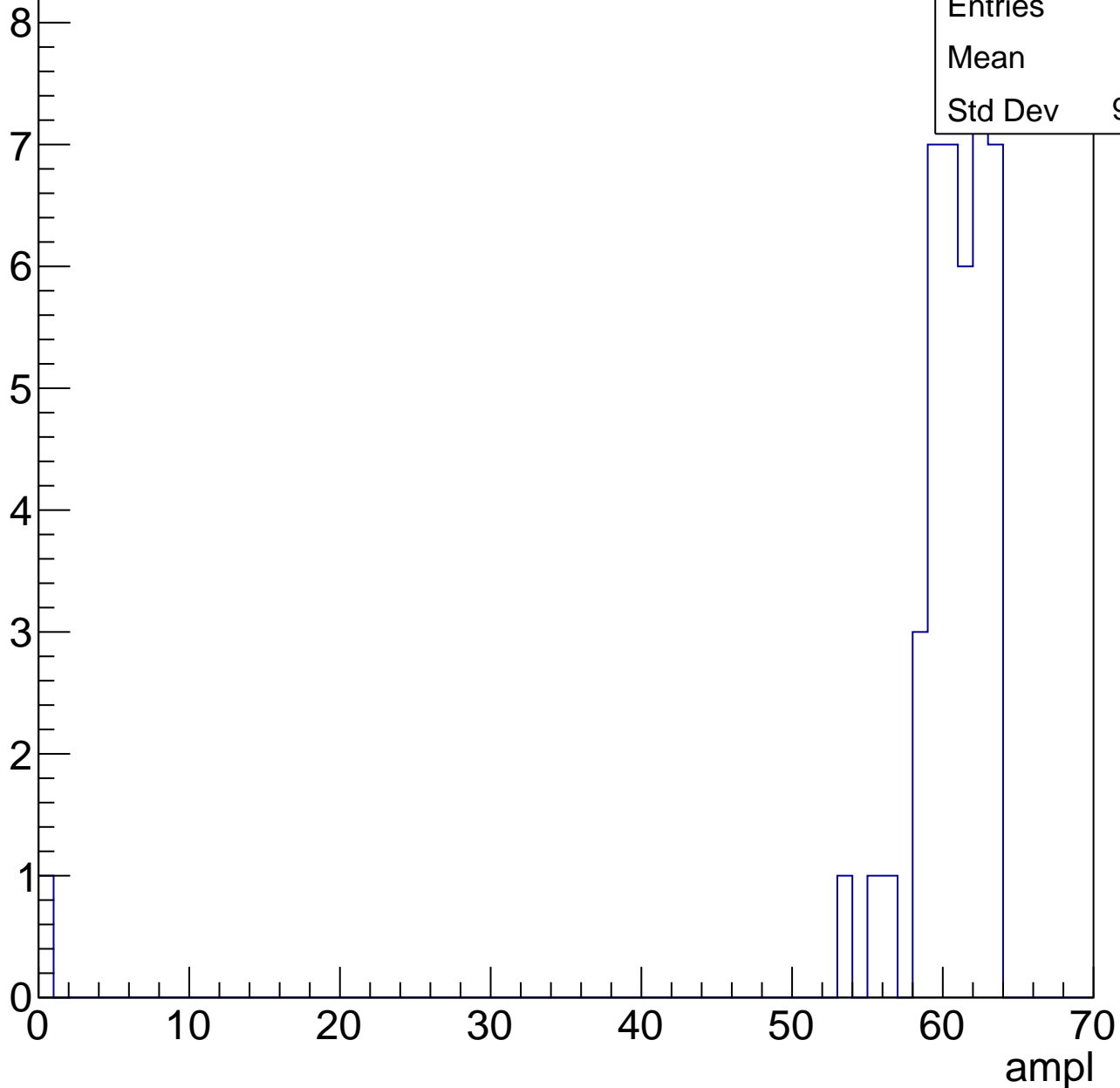
Entries	57
Mean	55.63
Std Dev	3.177

# B1L102S, U8-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	42
Mean	58.9
Std Dev	9.461



# B1L102S, U8-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch106, adc0

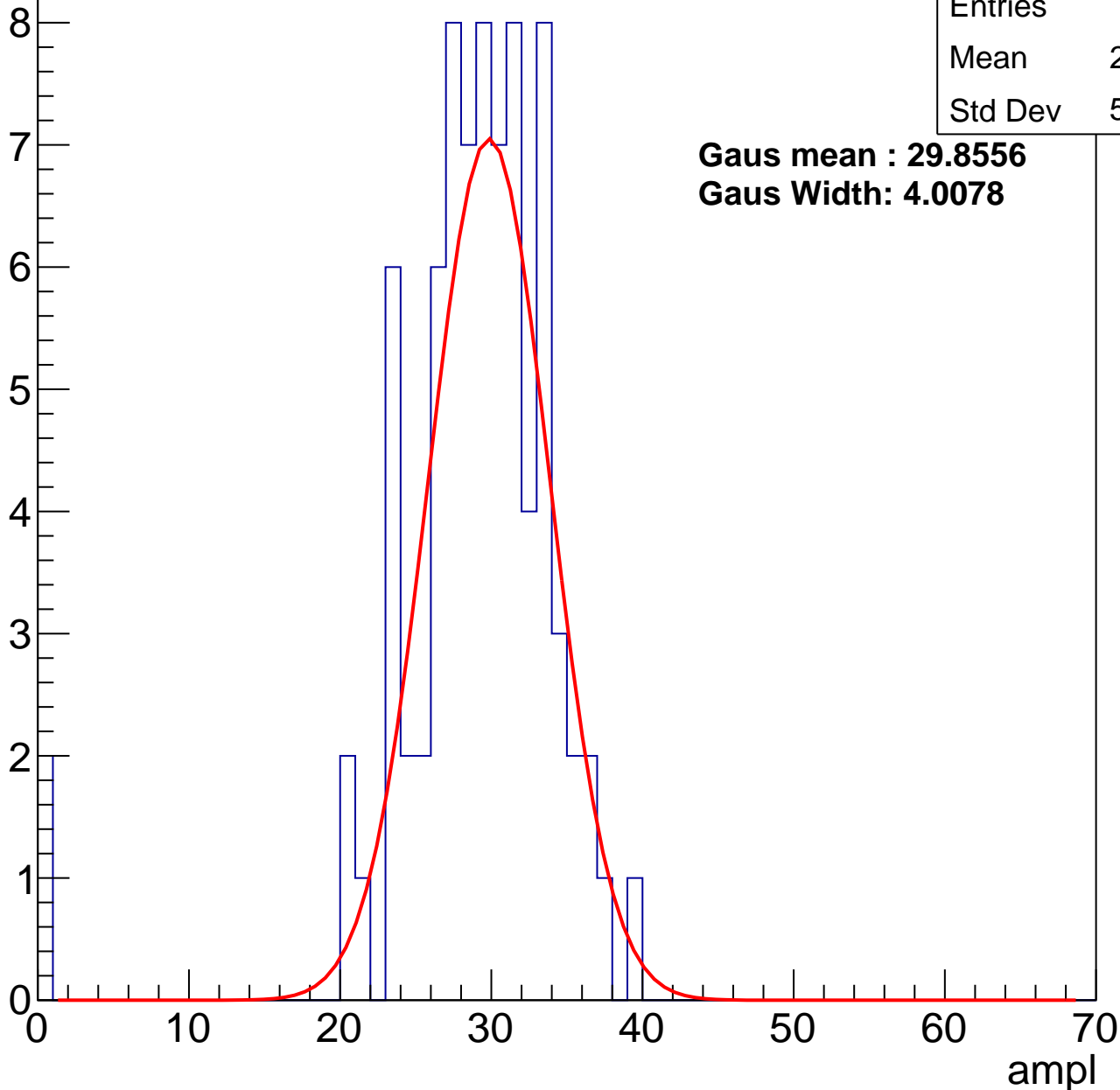
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	28.34
Std Dev	5.996

**Gaus mean : 29.8556**

**Gaus Width: 4.0078**



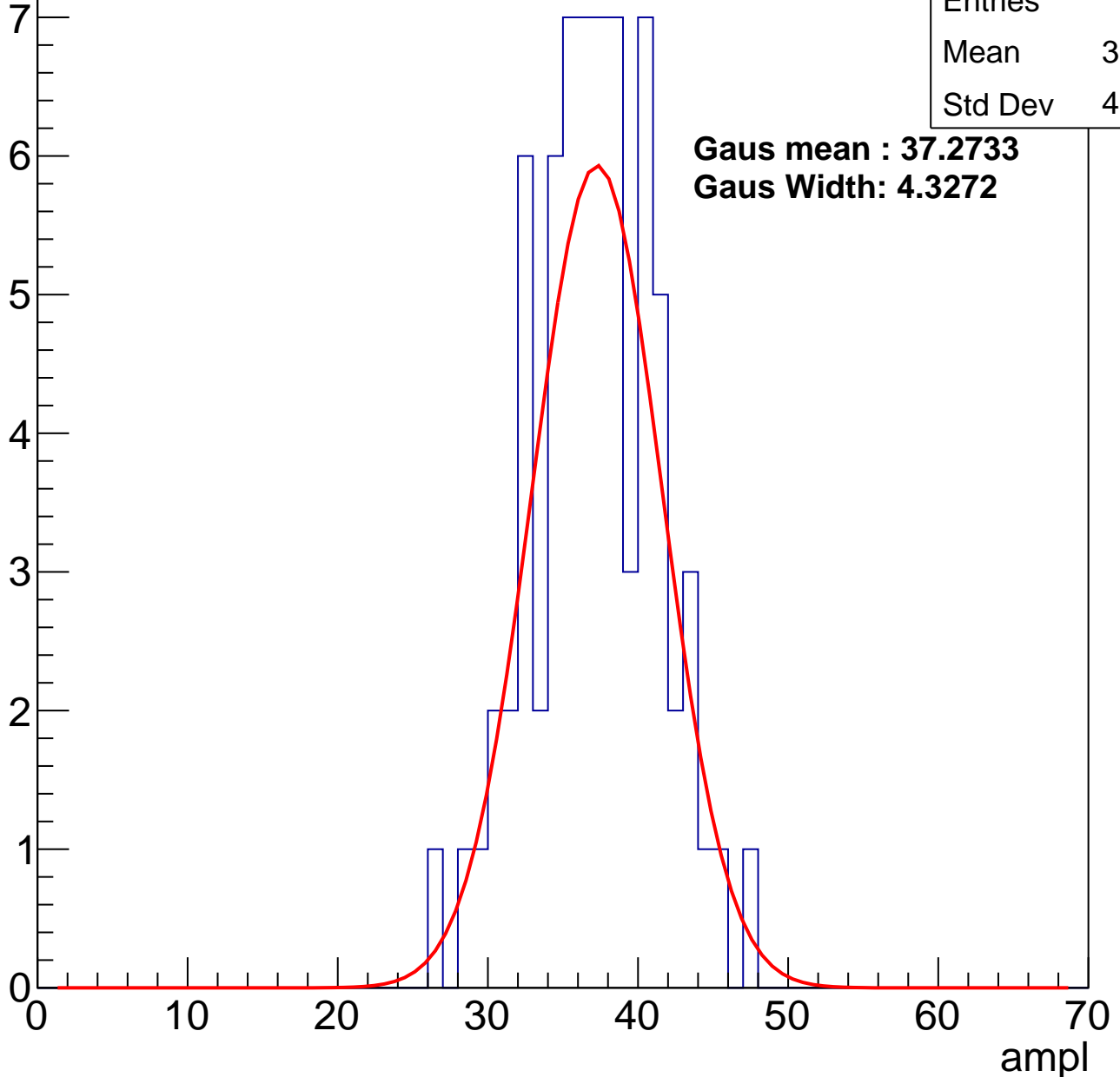
# B1L102S, U8-ch106, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	36.67
Std Dev	4.137

**Gaus mean : 37.2733**  
**Gaus Width: 4.3272**



# B1L102S, U8-ch106, adc2

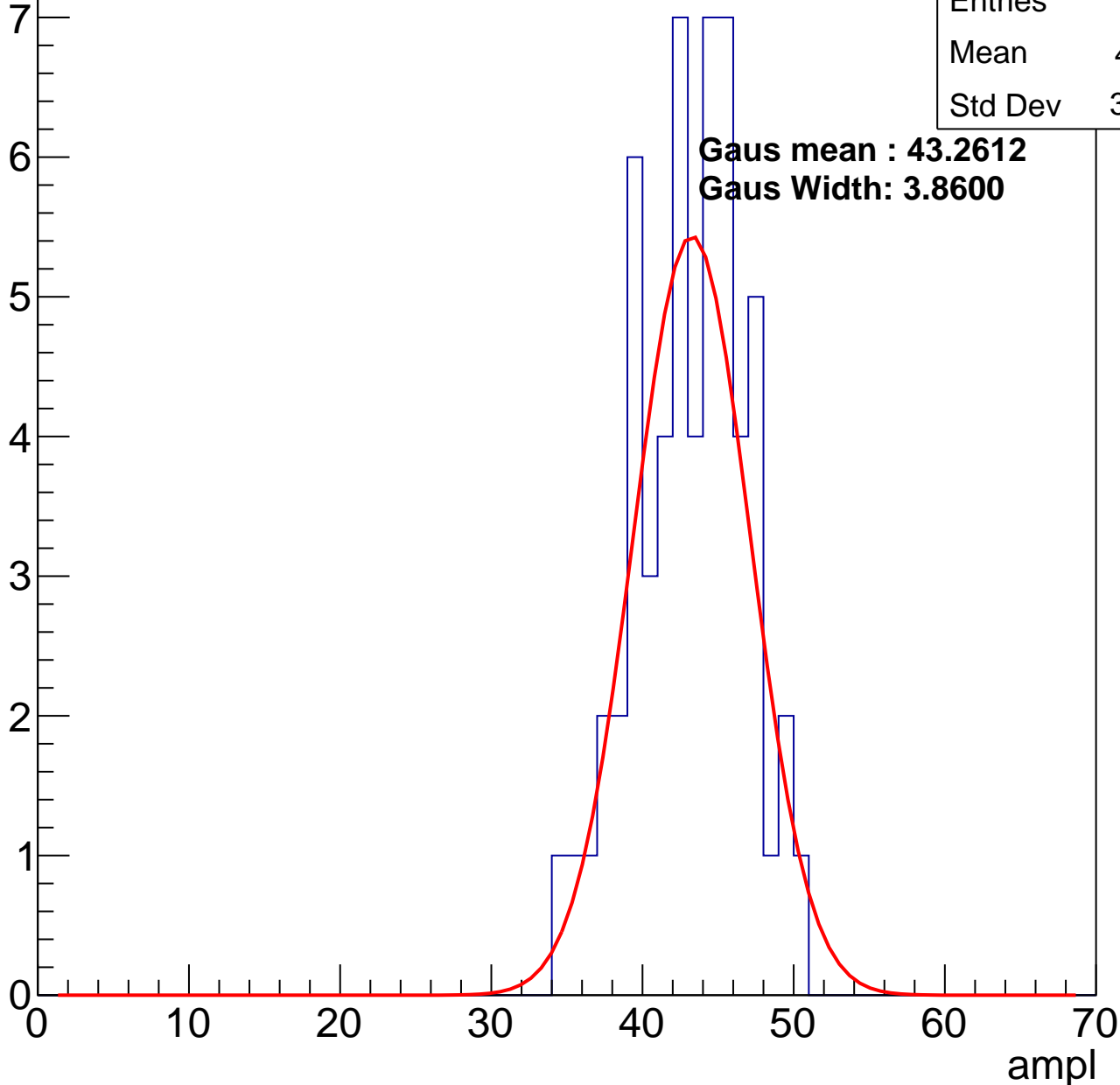
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	42.71
Std Dev	3.606

**Gaus mean : 43.2612**

**Gaus Width: 3.8600**

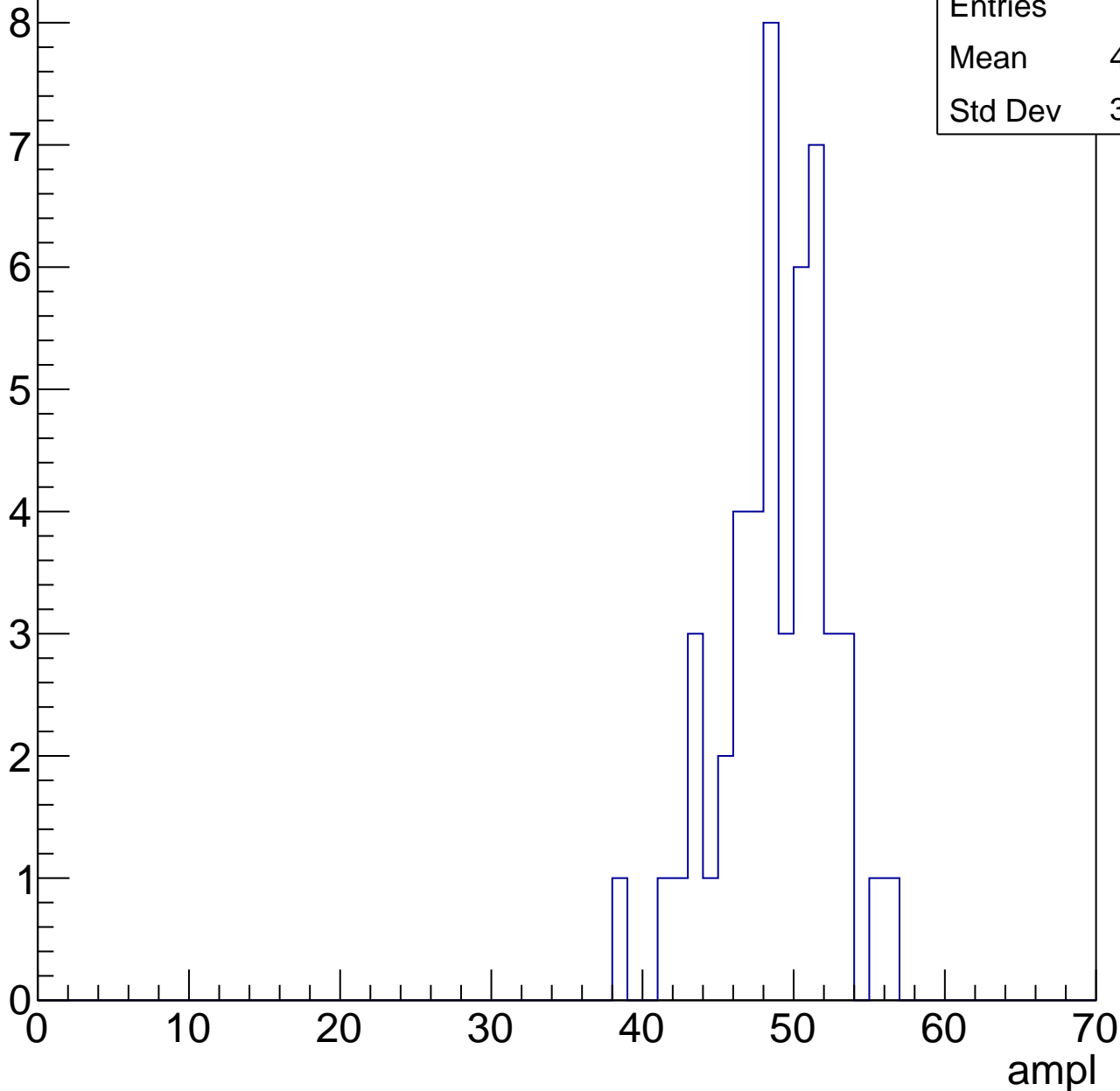


# B1L102S, U8-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	48.37
Std Dev	3.595

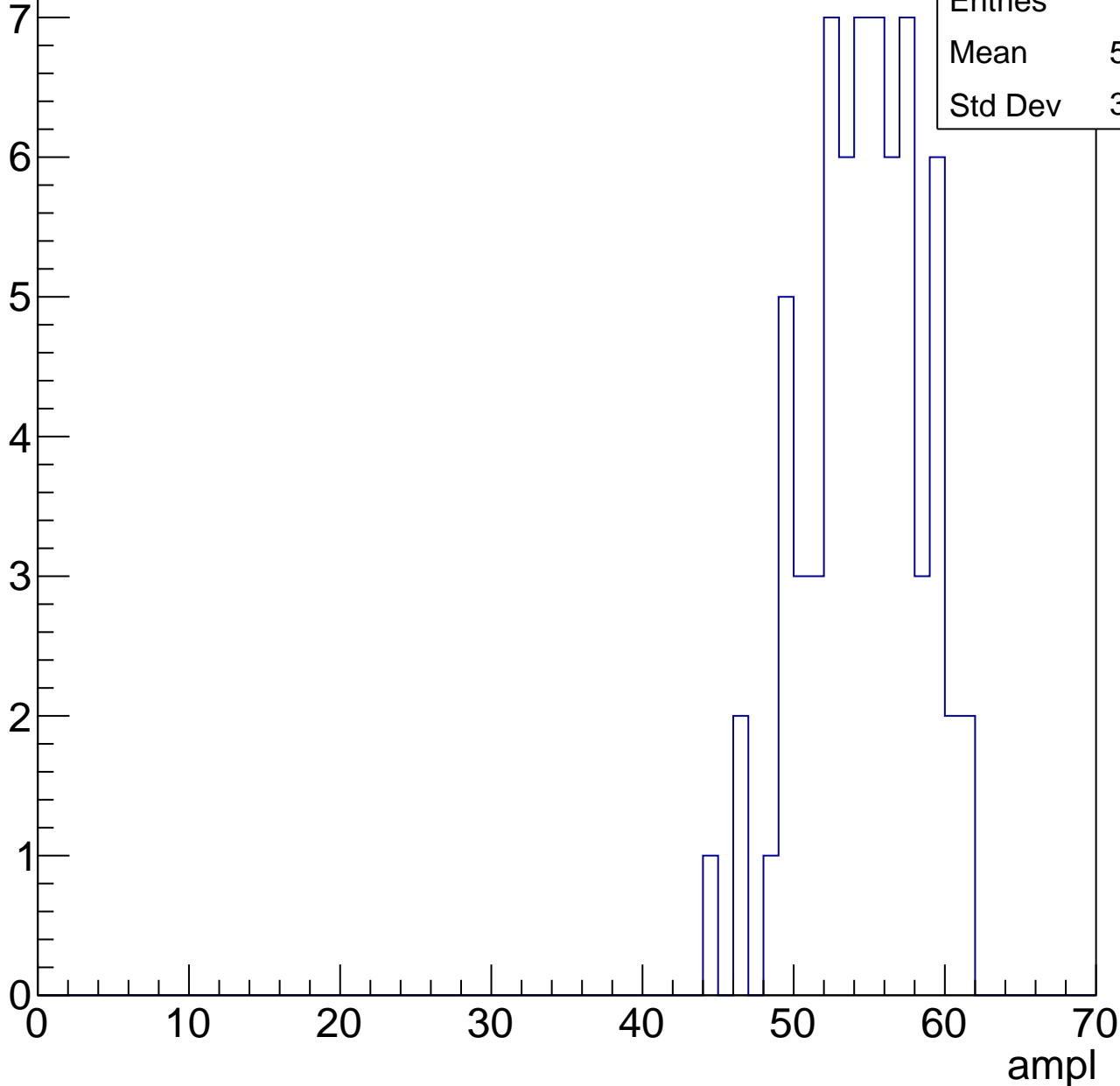


# B1L102S, U8-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	54.15
Std Dev	3.754

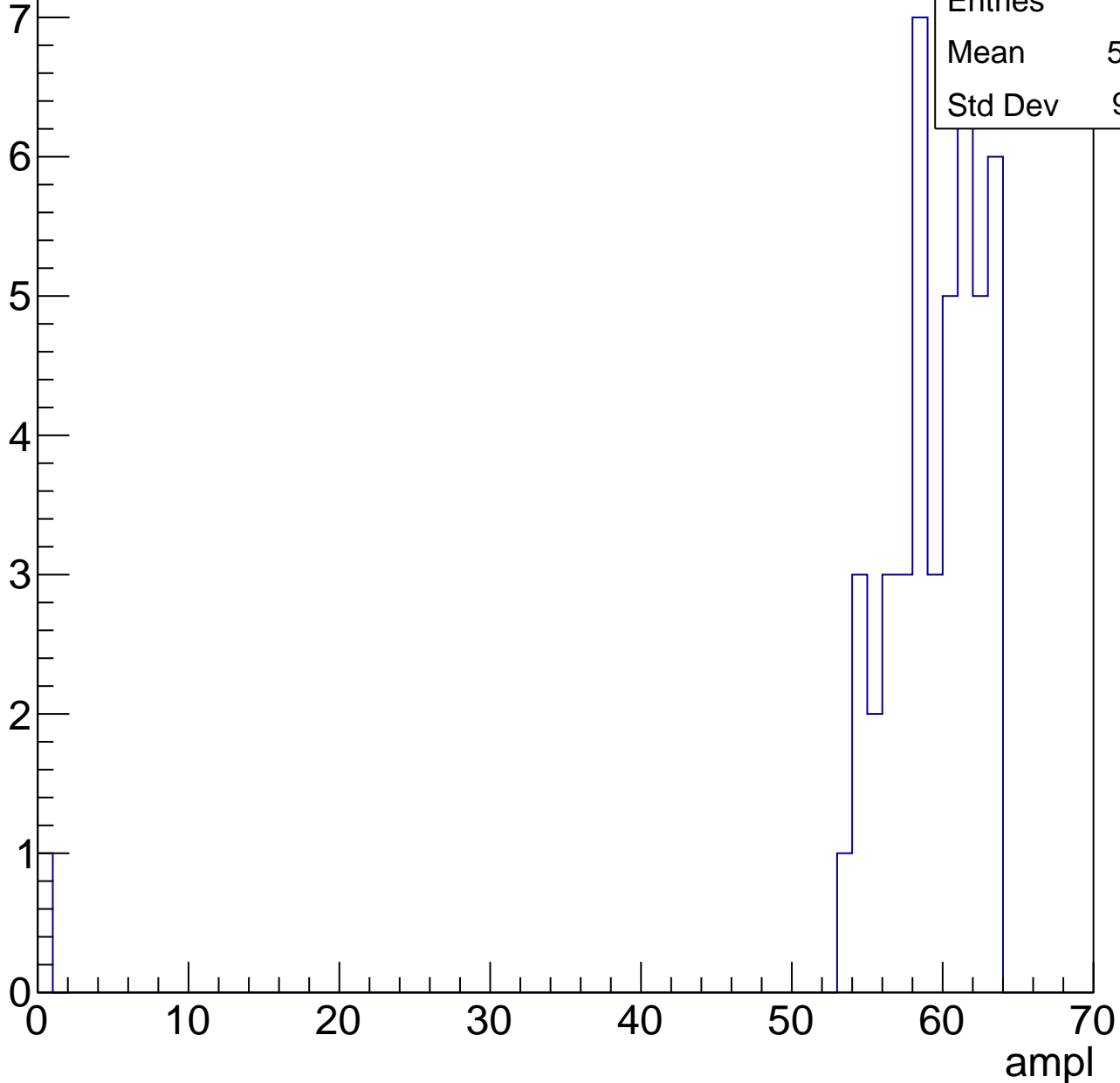


# B1L102S, U8-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

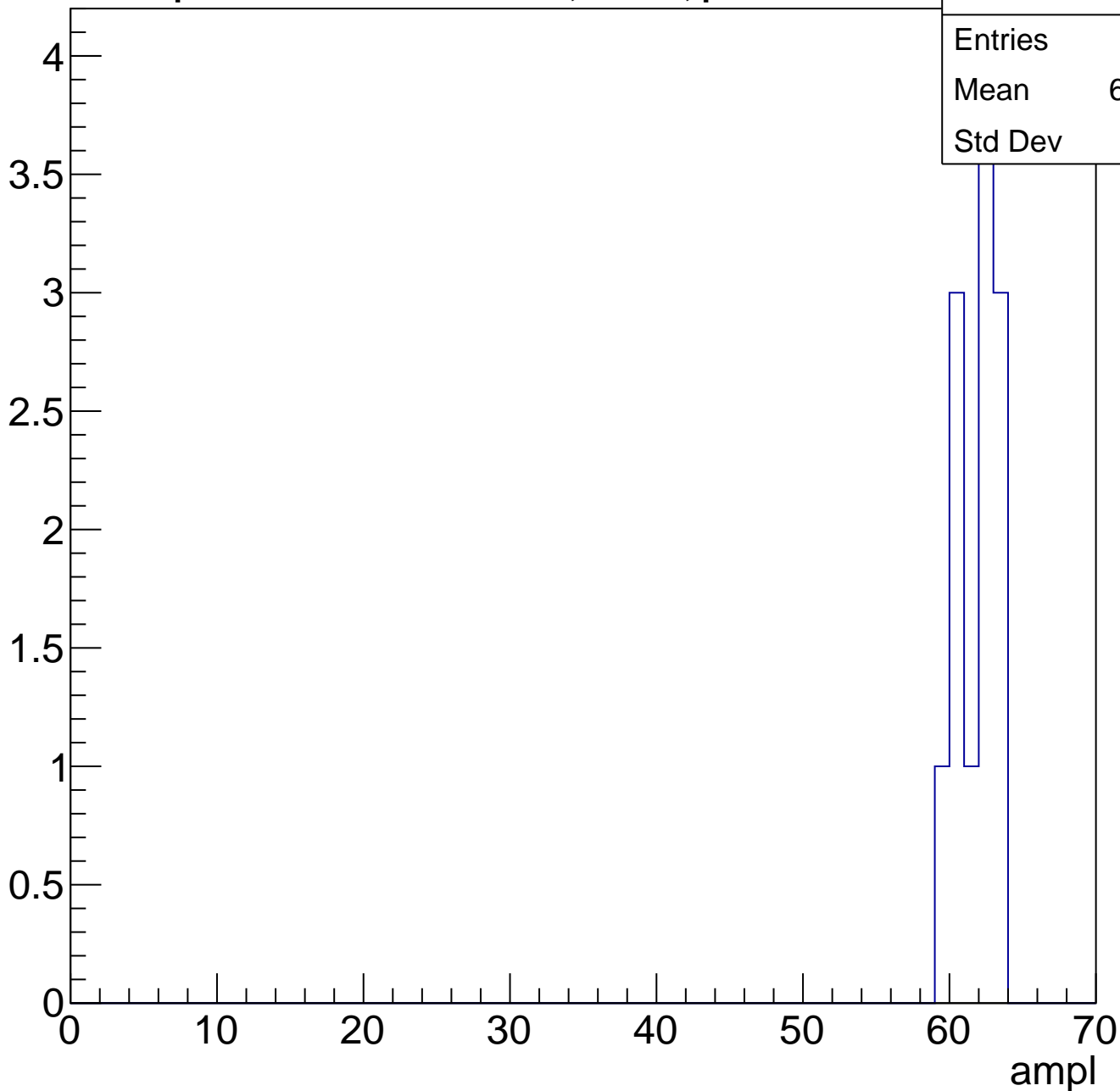
Entries	46
Mean	57.87
Std Dev	9.071



# B1L102S, U8-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

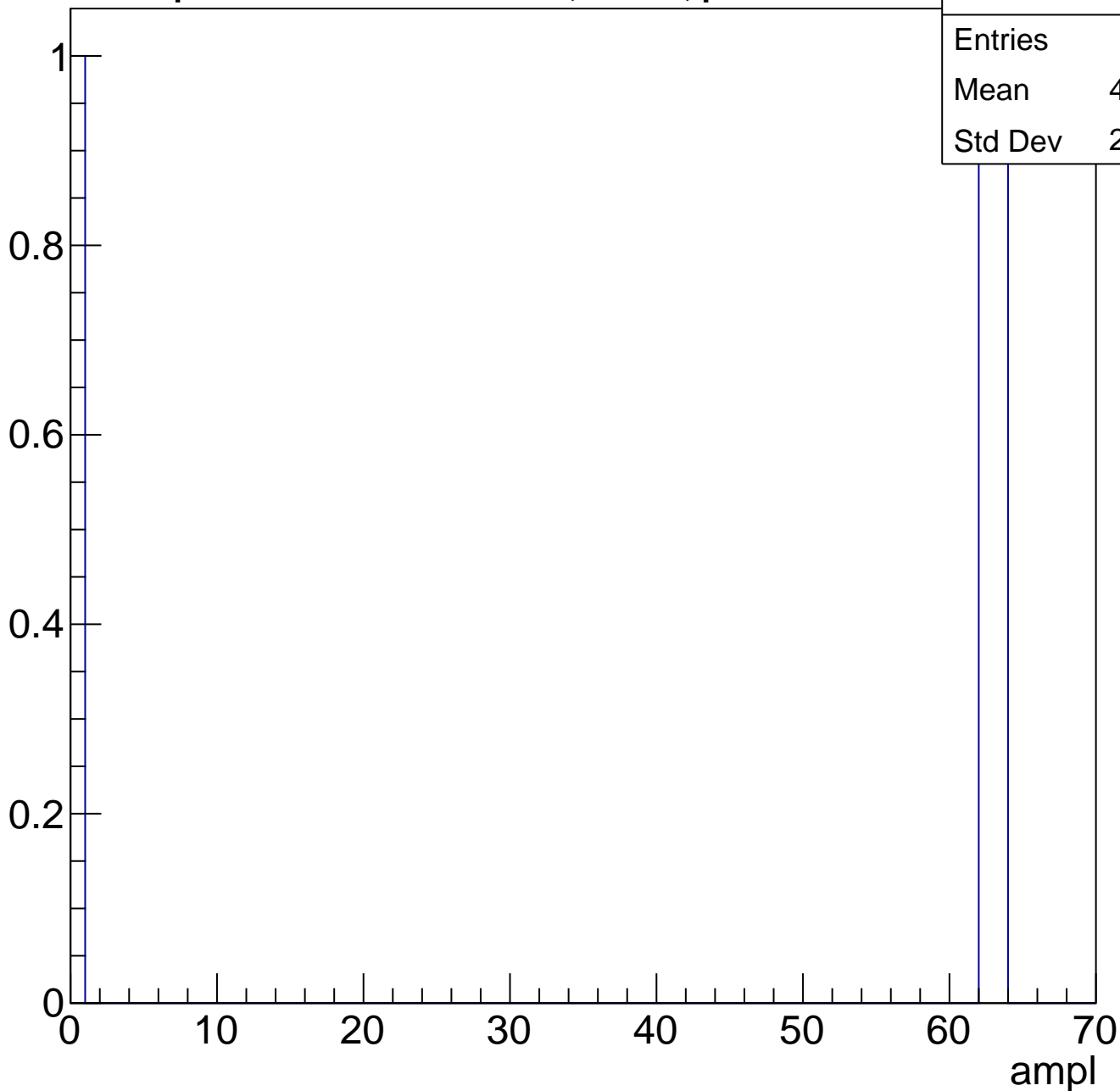




# B1L102S, U8-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



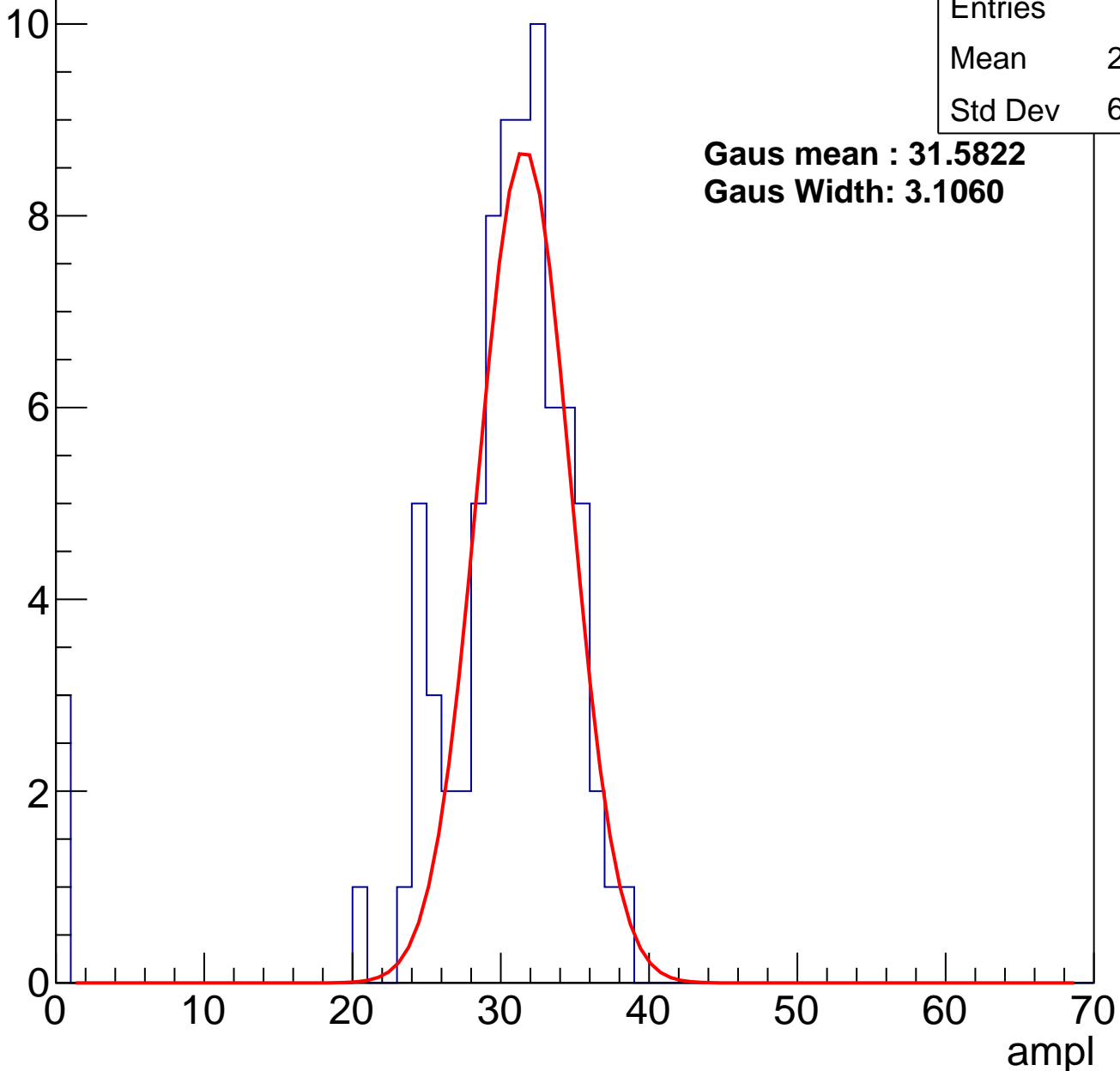
# B1L102S, U8-ch107, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	79
Mean	29.23
Std Dev	6.792

**Gaus mean : 31.5822**  
**Gaus Width: 3.1060**

Entry



# B1L102S, U8-ch107, adc1

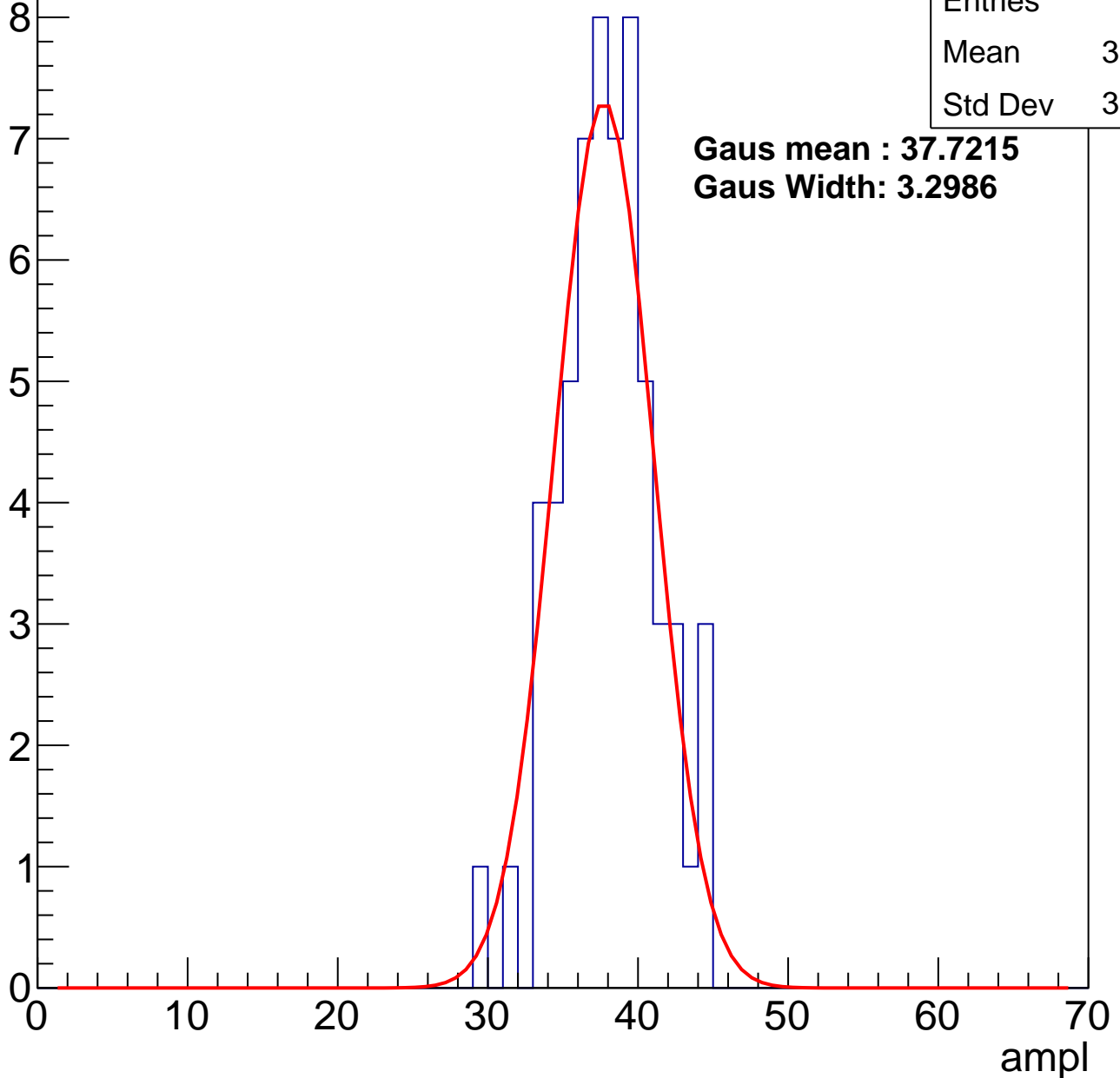
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	37.55
Std Dev	3.159

**Gaus mean : 37.7215**

**Gaus Width: 3.2986**



# B1L102S, U8-ch107, adc2

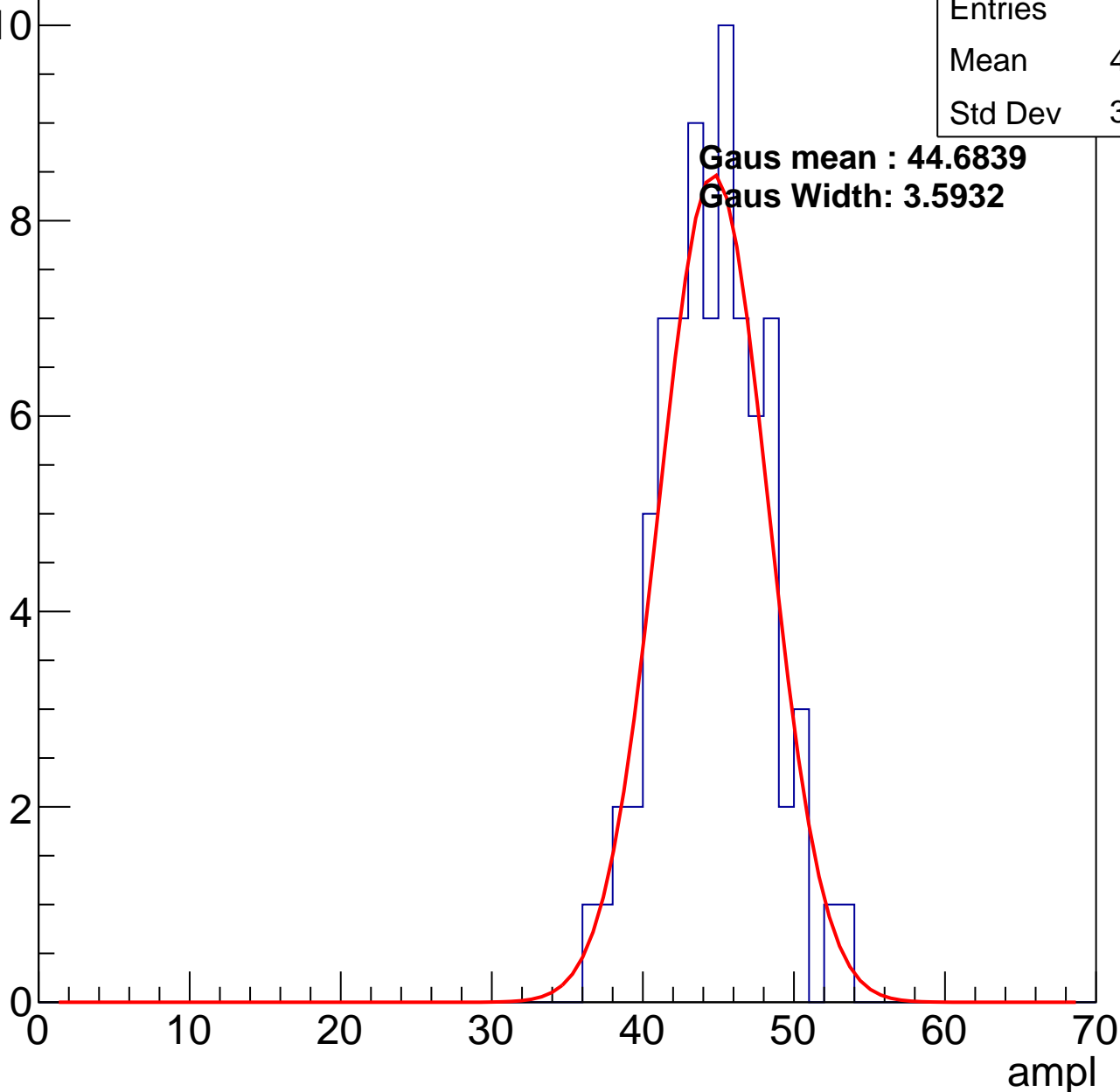
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	44.18
Std Dev	3.433

Gaus mean : 44.6839

Gaus Width: 3.5932

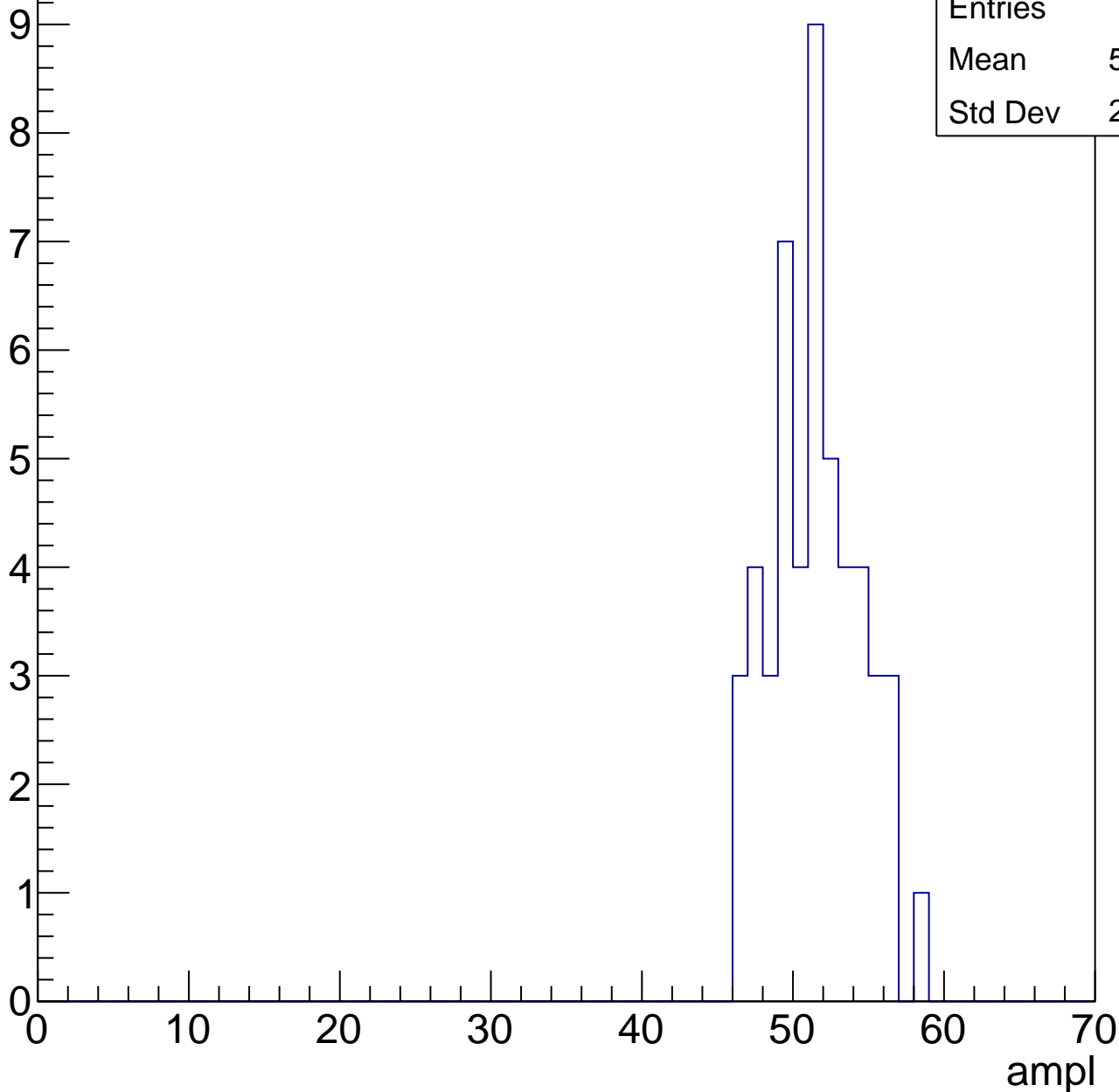


# B1L102S, U8-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	51.02
Std Dev	2.922

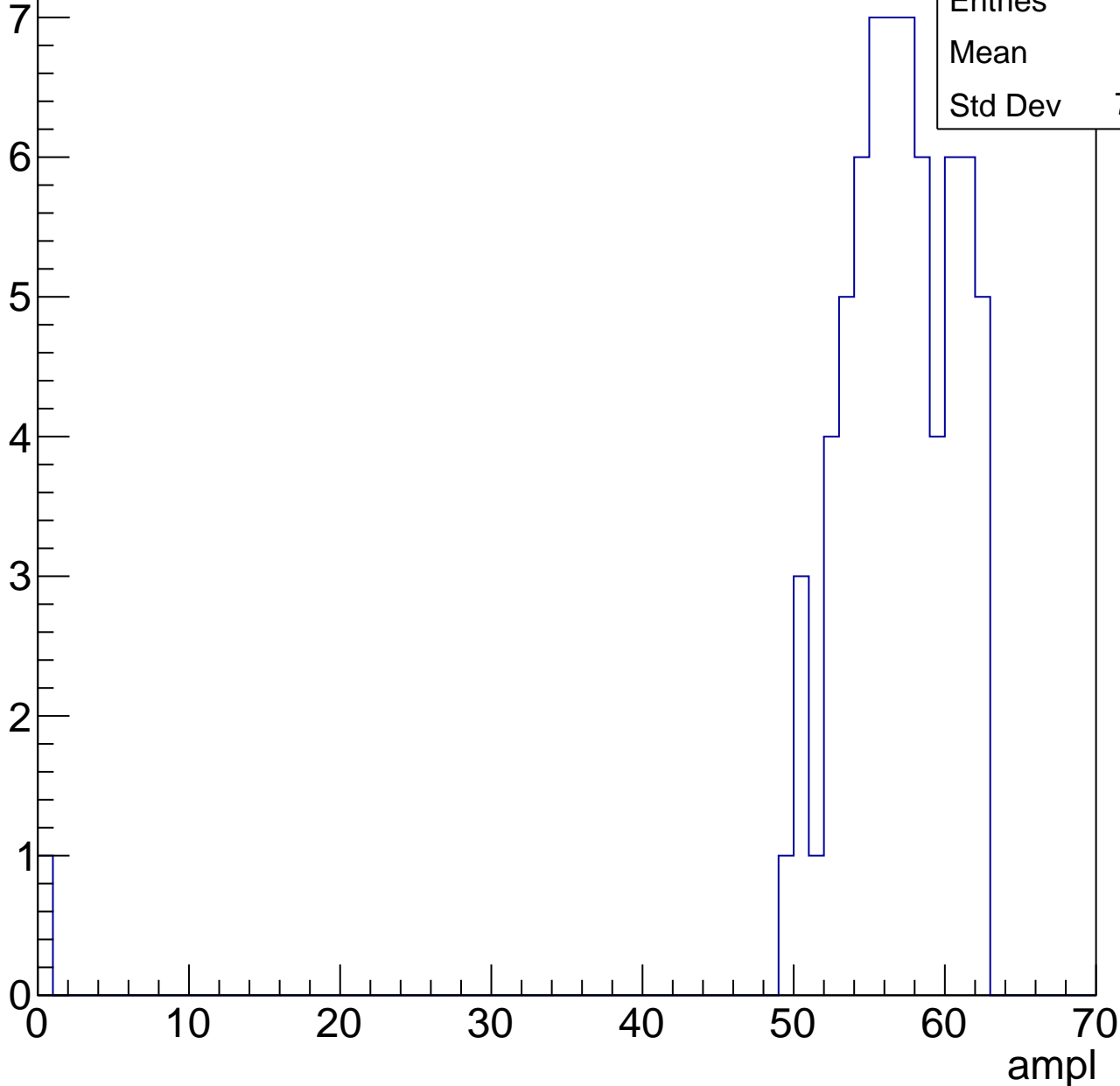


# B1L102S, U8-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	55.7
Std Dev	7.561

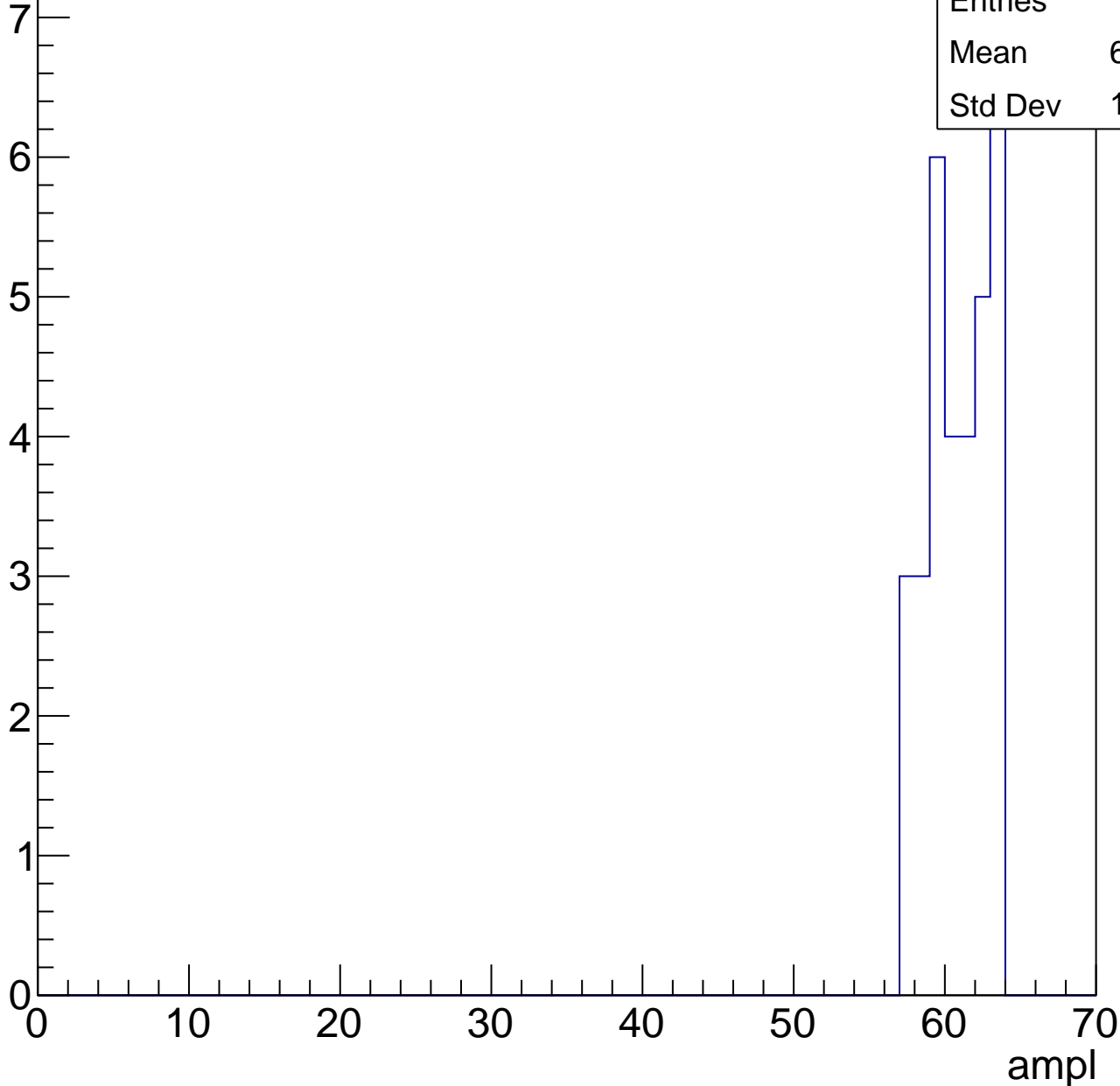


# B1L102S, U8-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	32
Mean	60.44
Std Dev	1.983



# B1L102S, U8-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch108, adc0

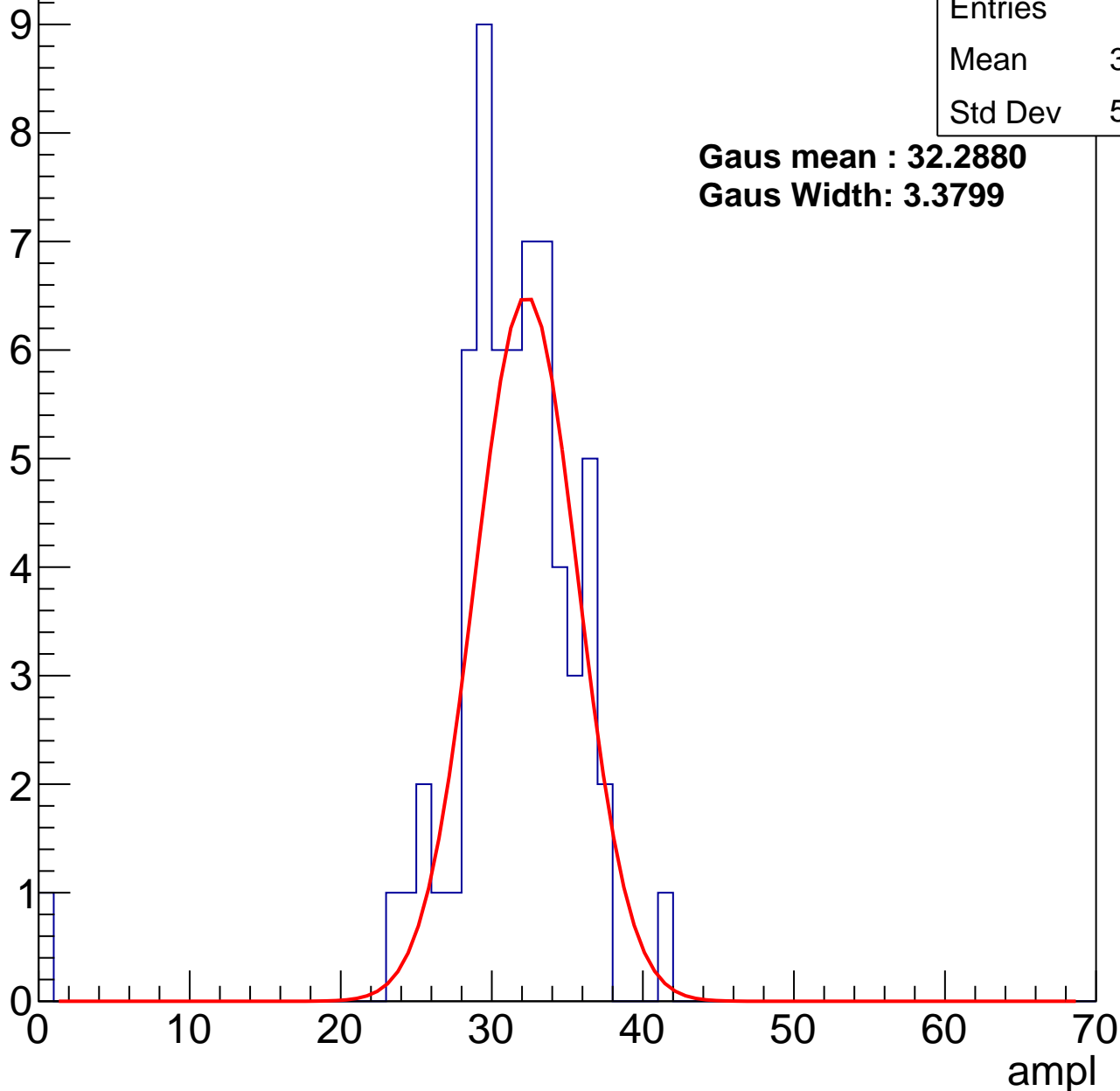
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	30.73
Std Dev	5.186

**Gaus mean : 32.2880**

**Gaus Width: 3.3799**



# B1L102S, U8-ch108, adc1

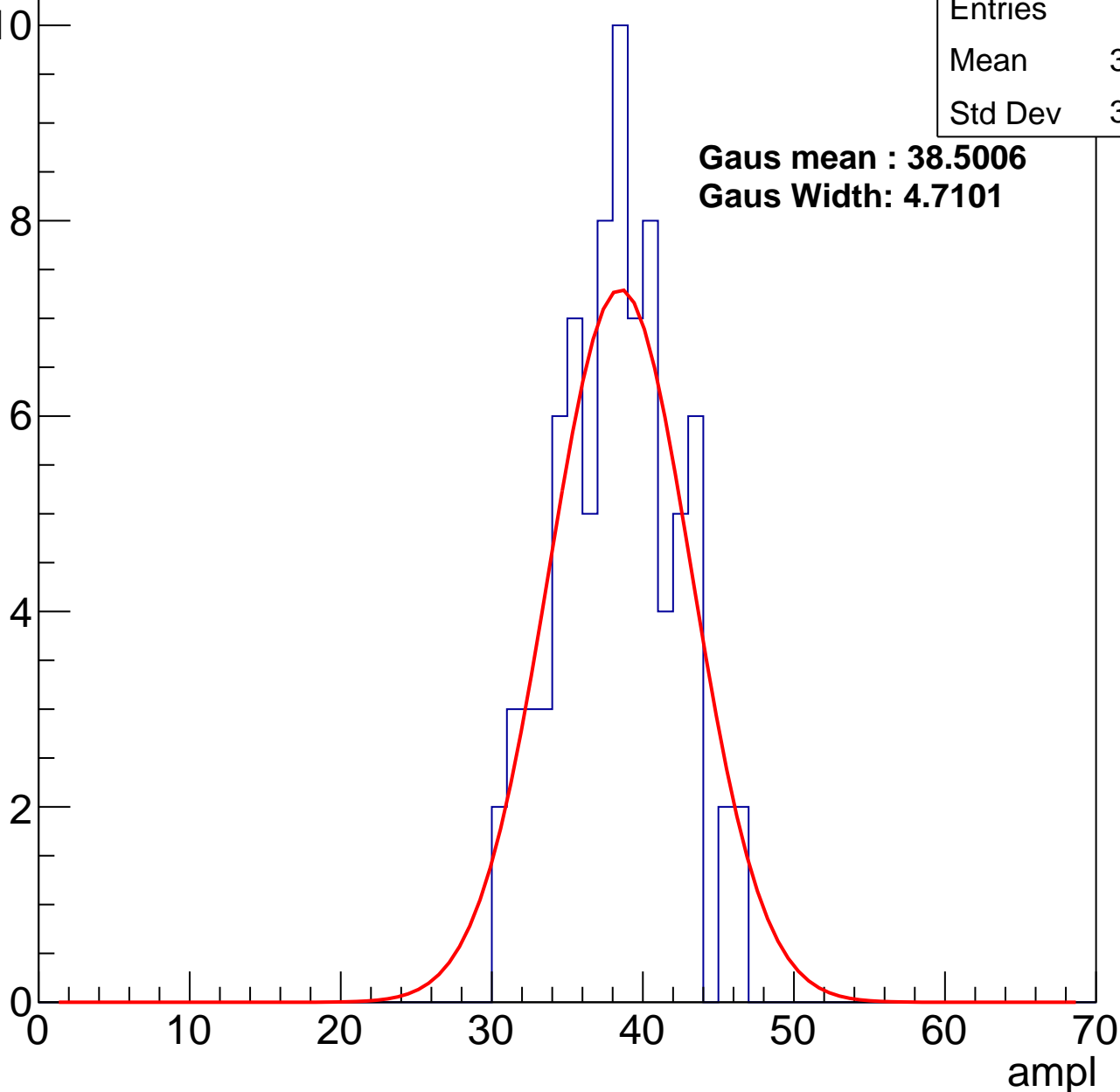
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	81
Mean	37.78
Std Dev	3.804

**Gaus mean : 38.5006**

**Gaus Width: 4.7101**



# B1L102S, U8-ch108, adc2

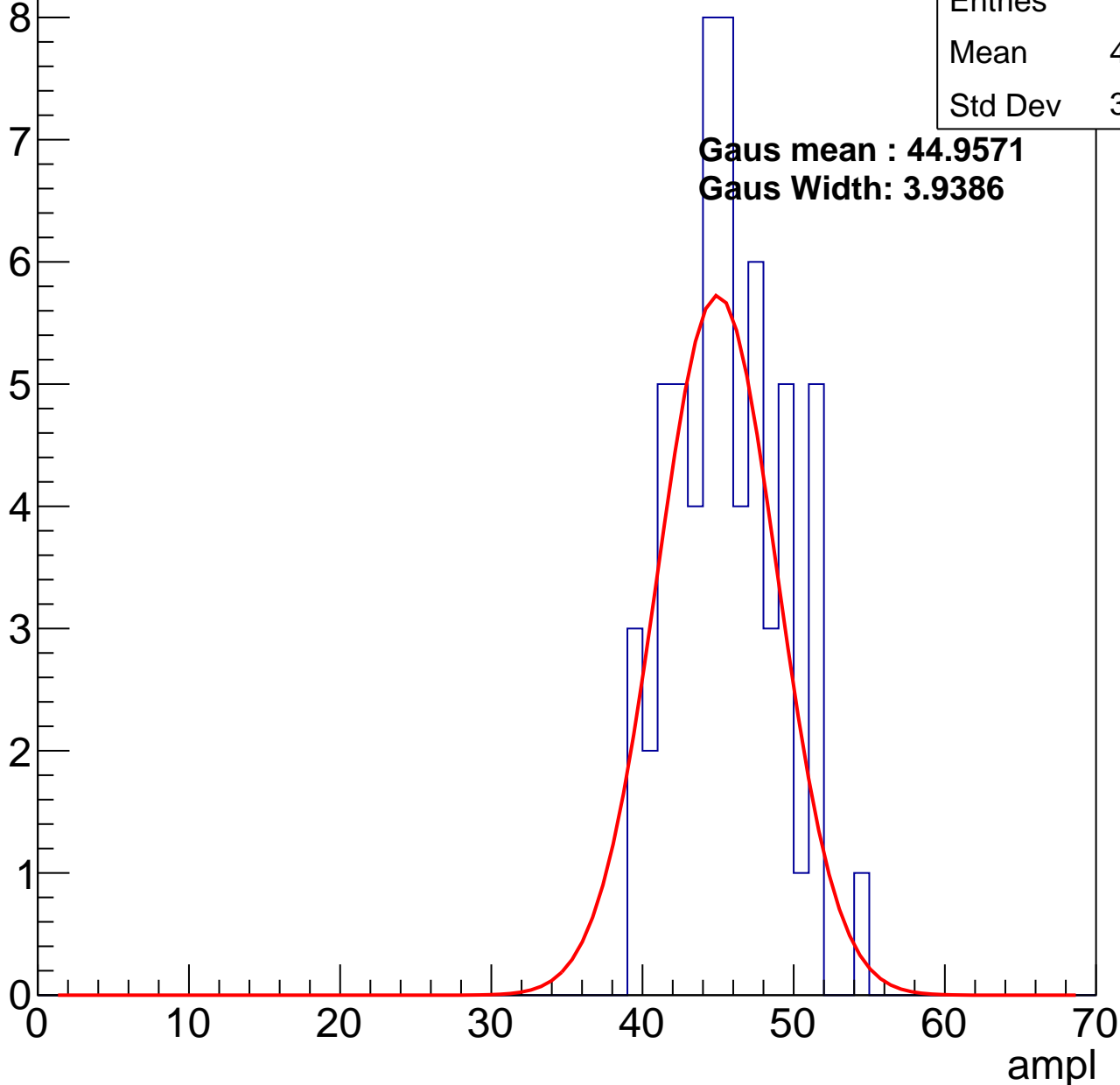
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	45.17
Std Dev	3.479

**Gaus mean : 44.9571**

**Gaus Width: 3.9386**

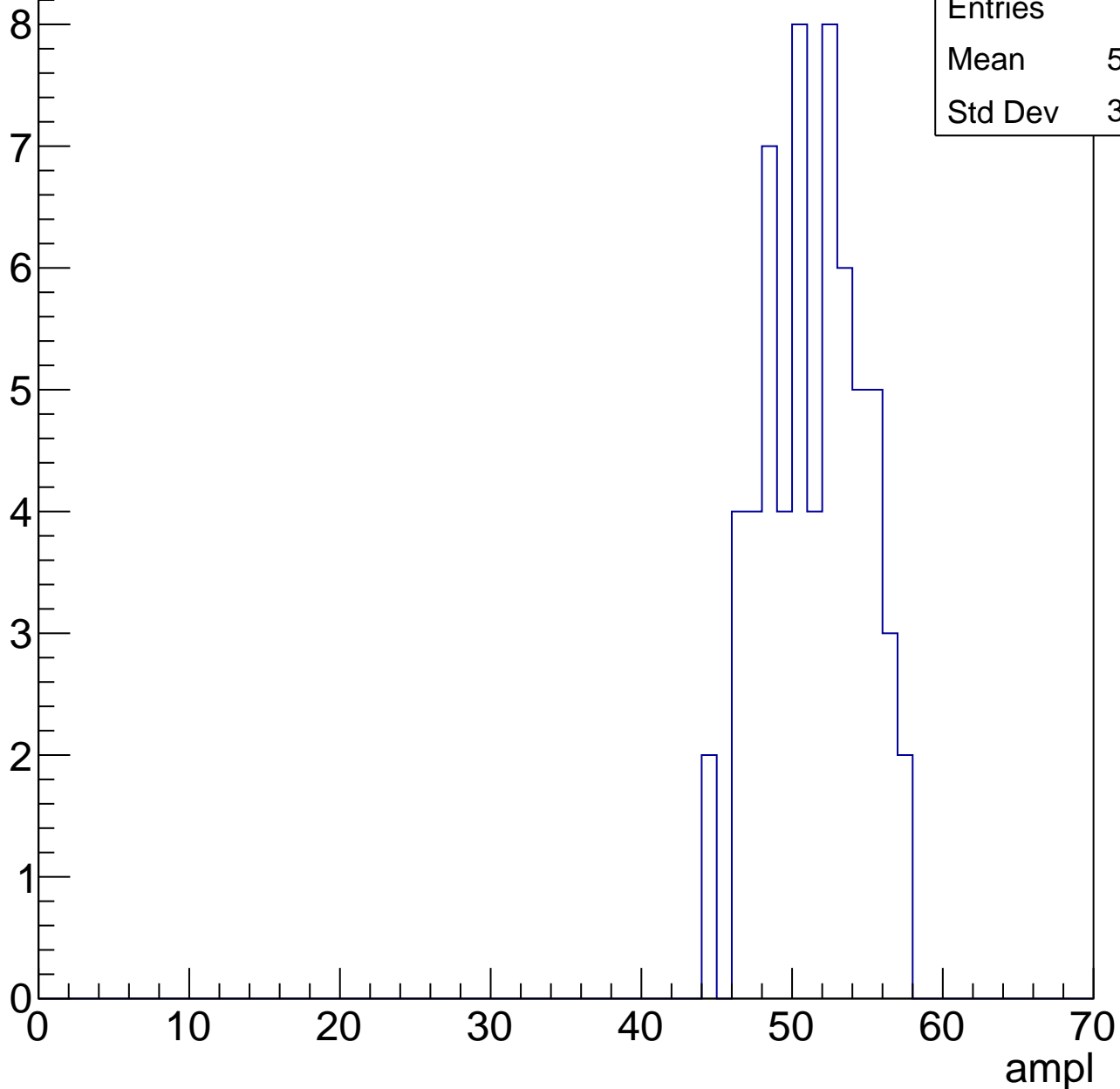


# B1L102S, U8-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

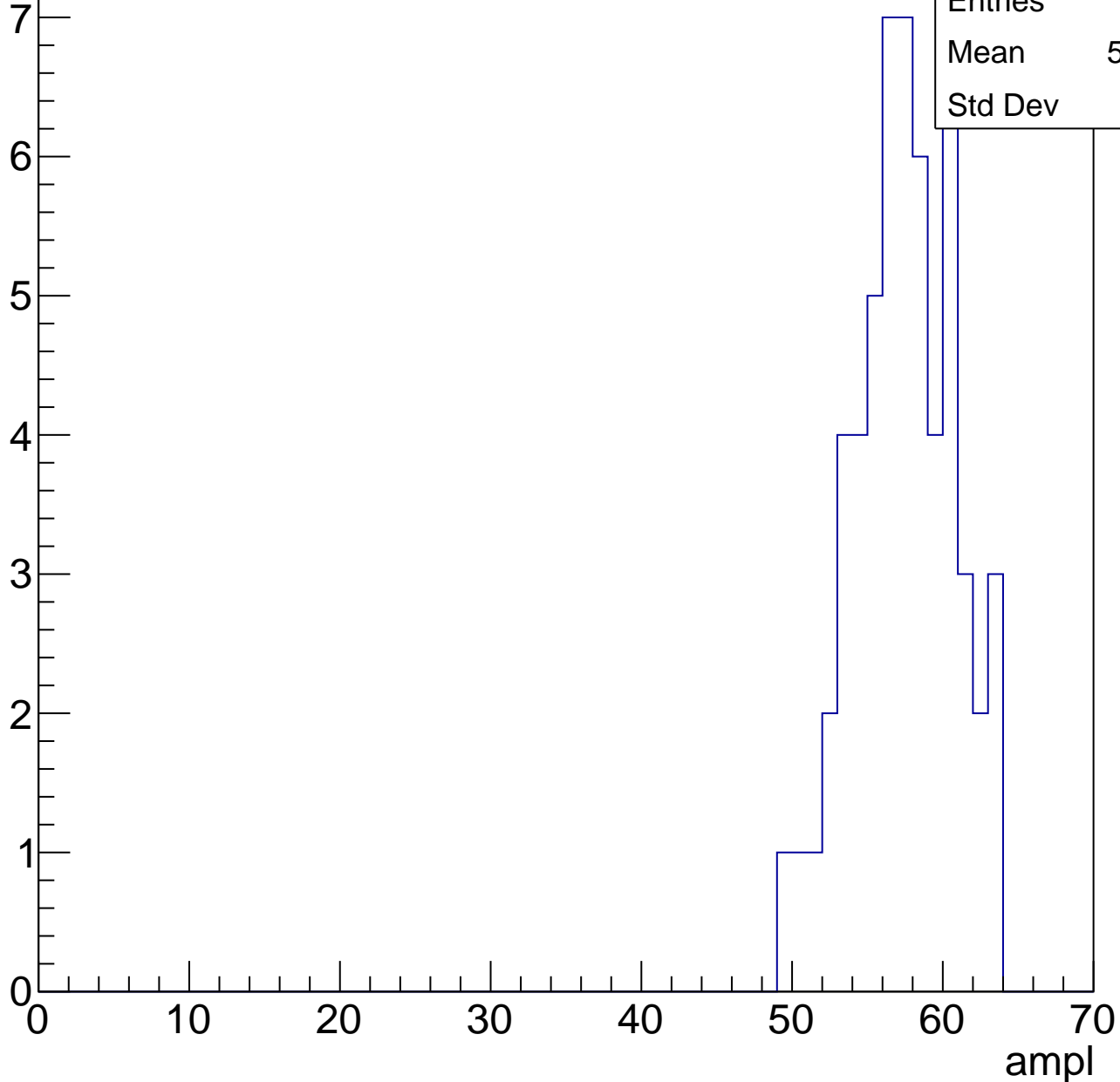
Entries	62
Mean	50.92
Std Dev	3.244



# B1L102S, U8-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



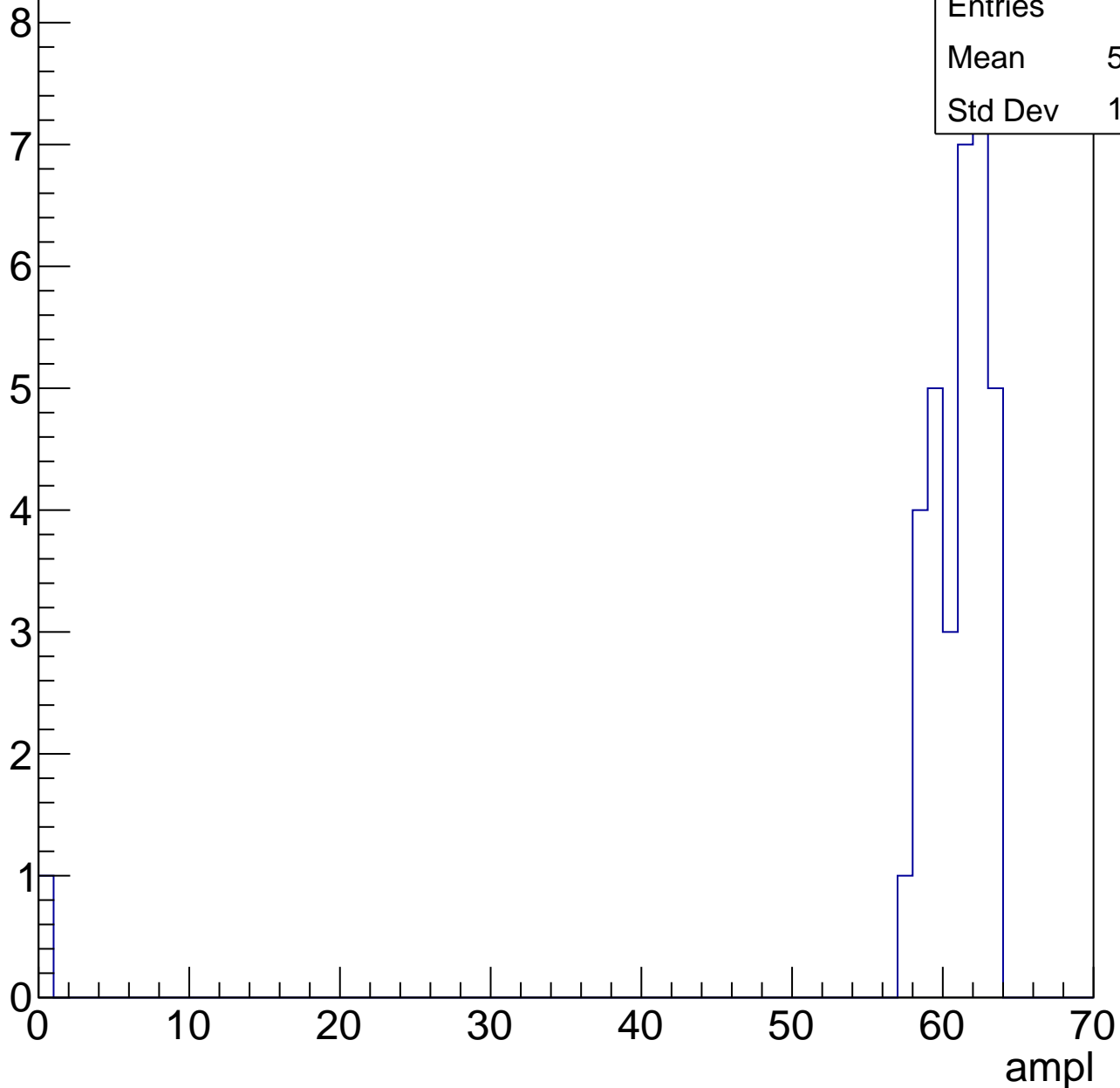
Entries	57
Mean	56.98
Std Dev	3.29

# B1L102S, U8-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	34
Mean	58.88
Std Dev	10.39



# B1L102S, U8-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U8-ch109, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	83
Mean	29.67
Std Dev	4.698

**Gaus mean : 29.9621**

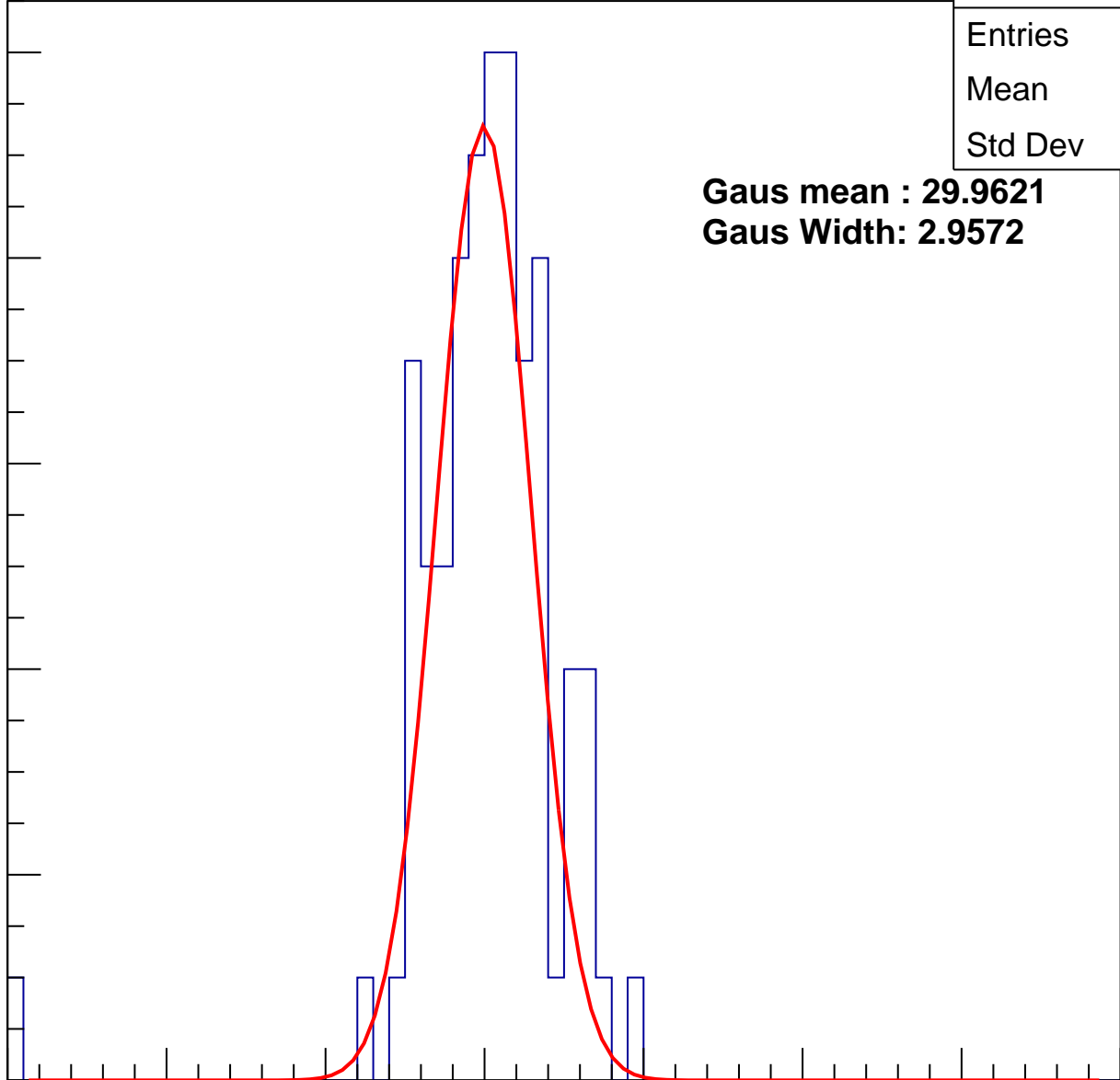
**Gaus Width: 2.9572**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U8-ch109, adc1

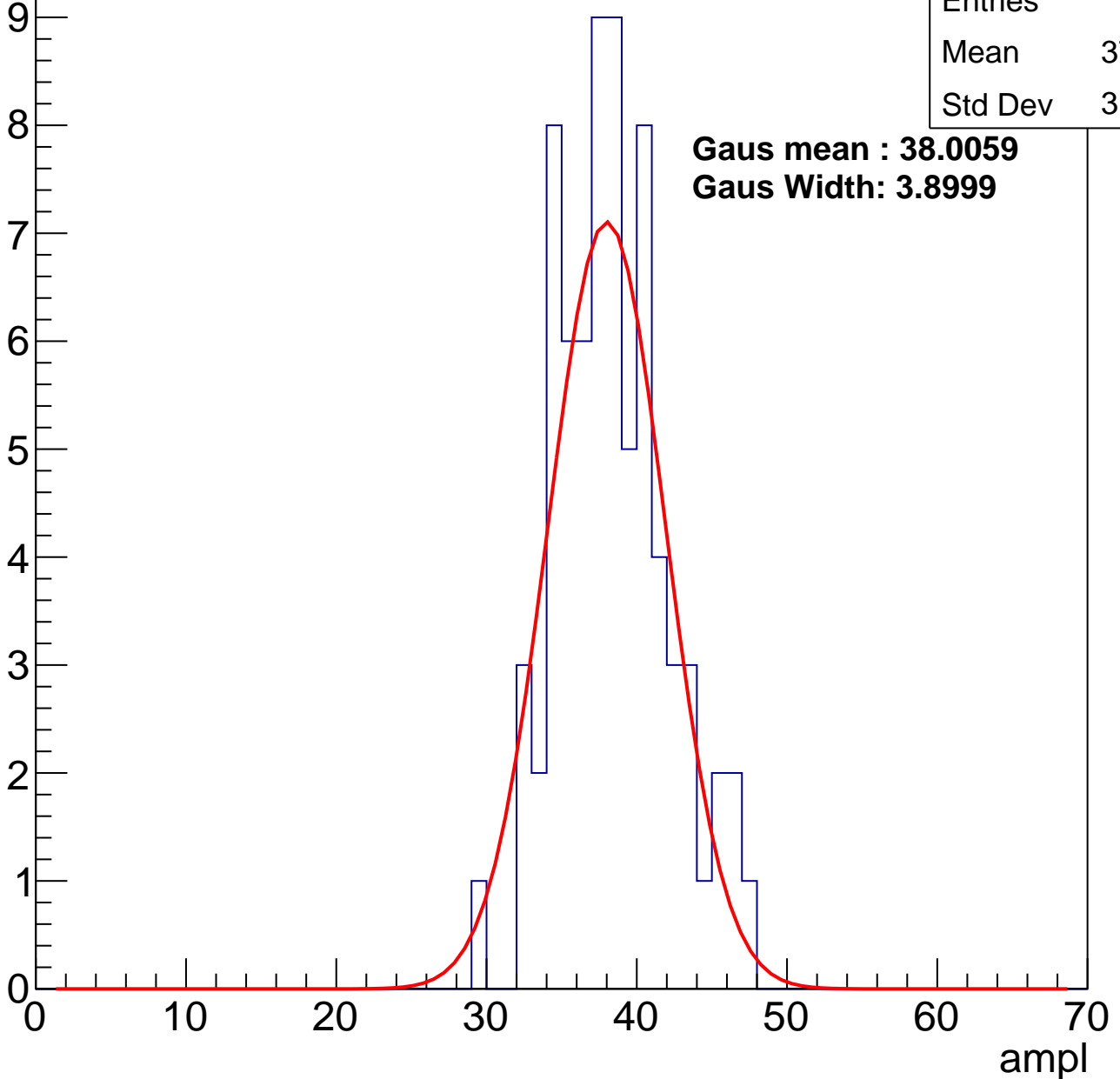
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	37.96
Std Dev	3.688

**Gaus mean : 38.0059**

**Gaus Width: 3.8999**

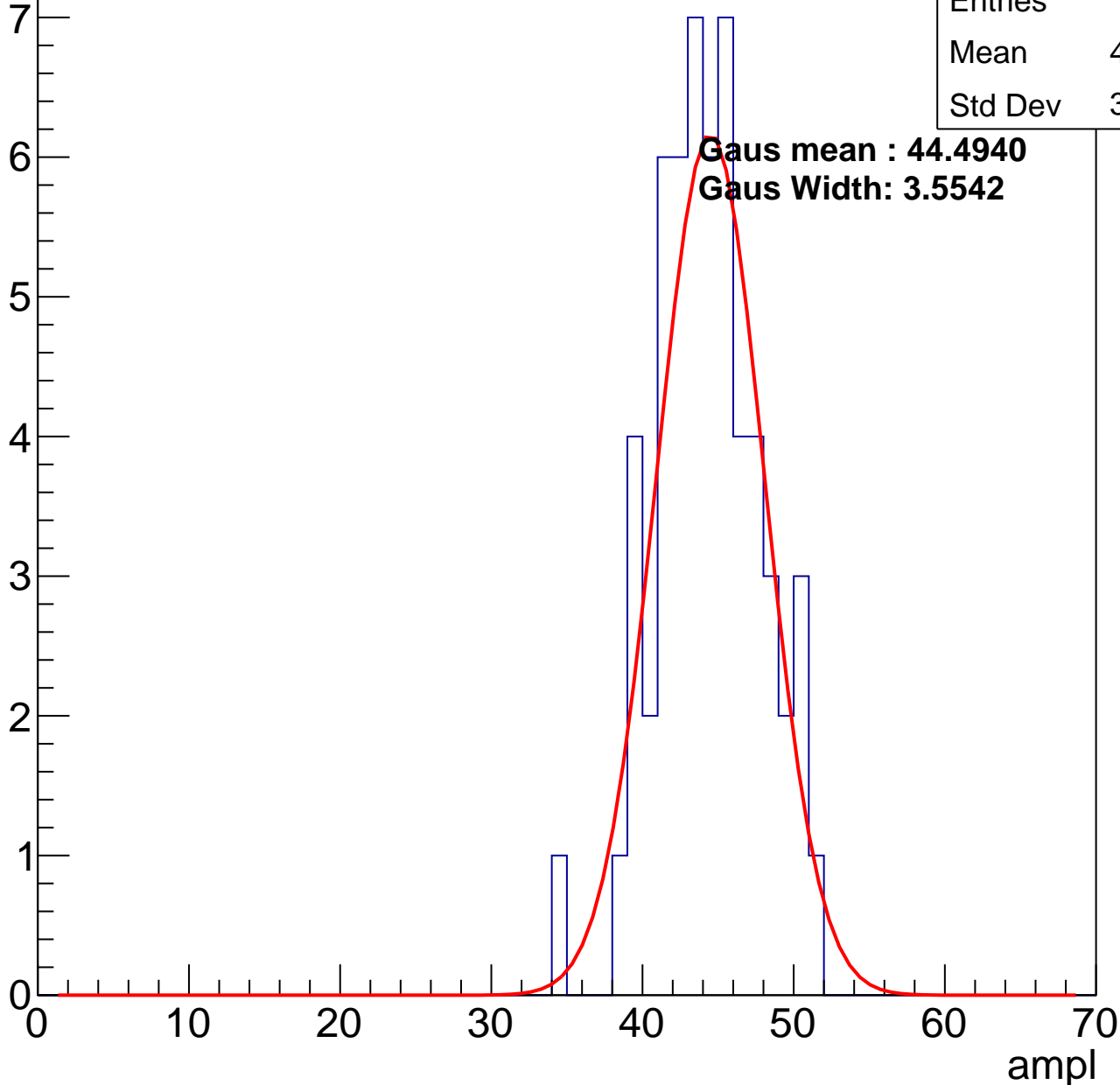


# B1L102S, U8-ch109, adc2

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	43.88
Std Dev	3.419

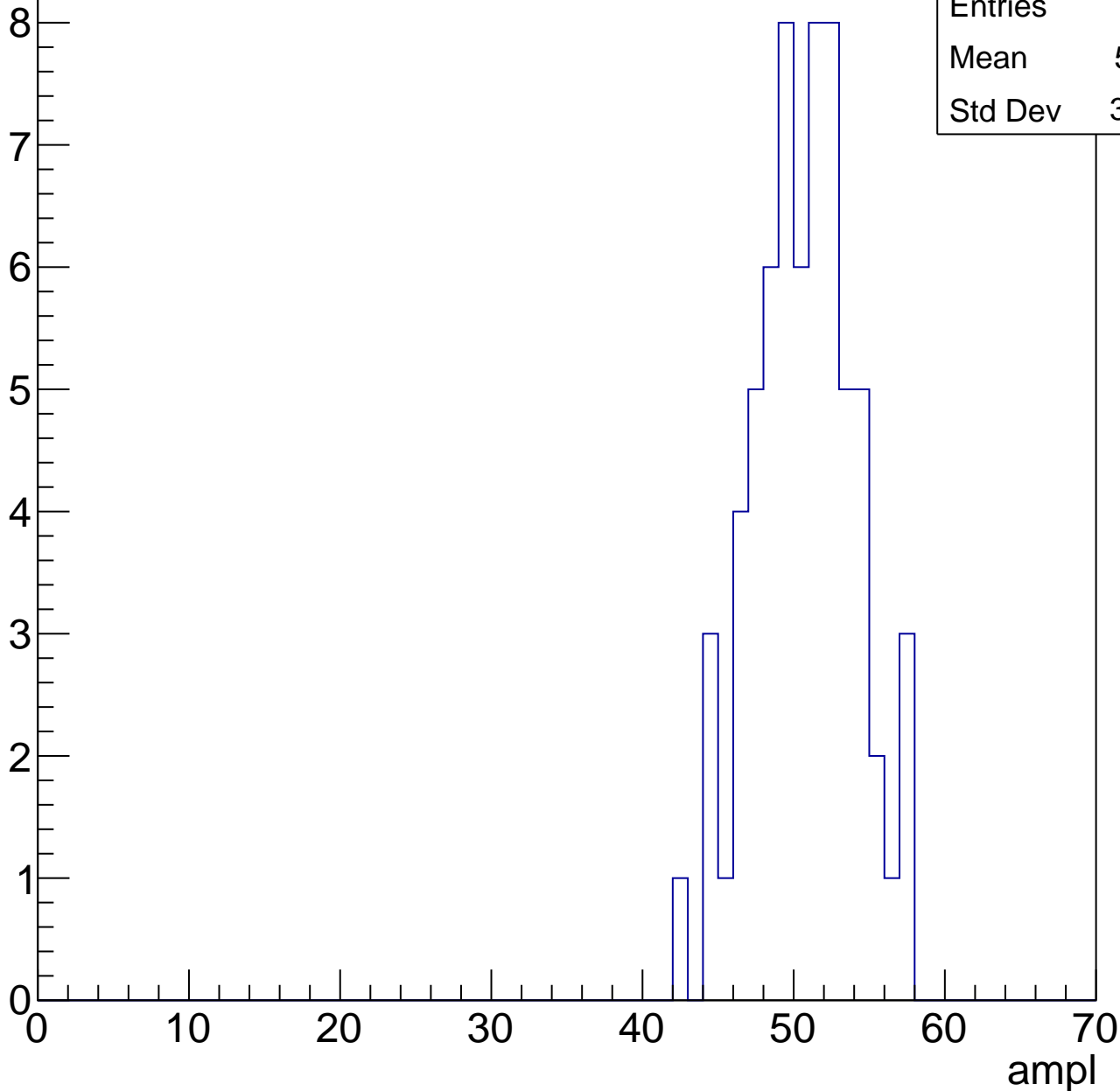


# B1L102S, U8-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	50.21
Std Dev	3.333

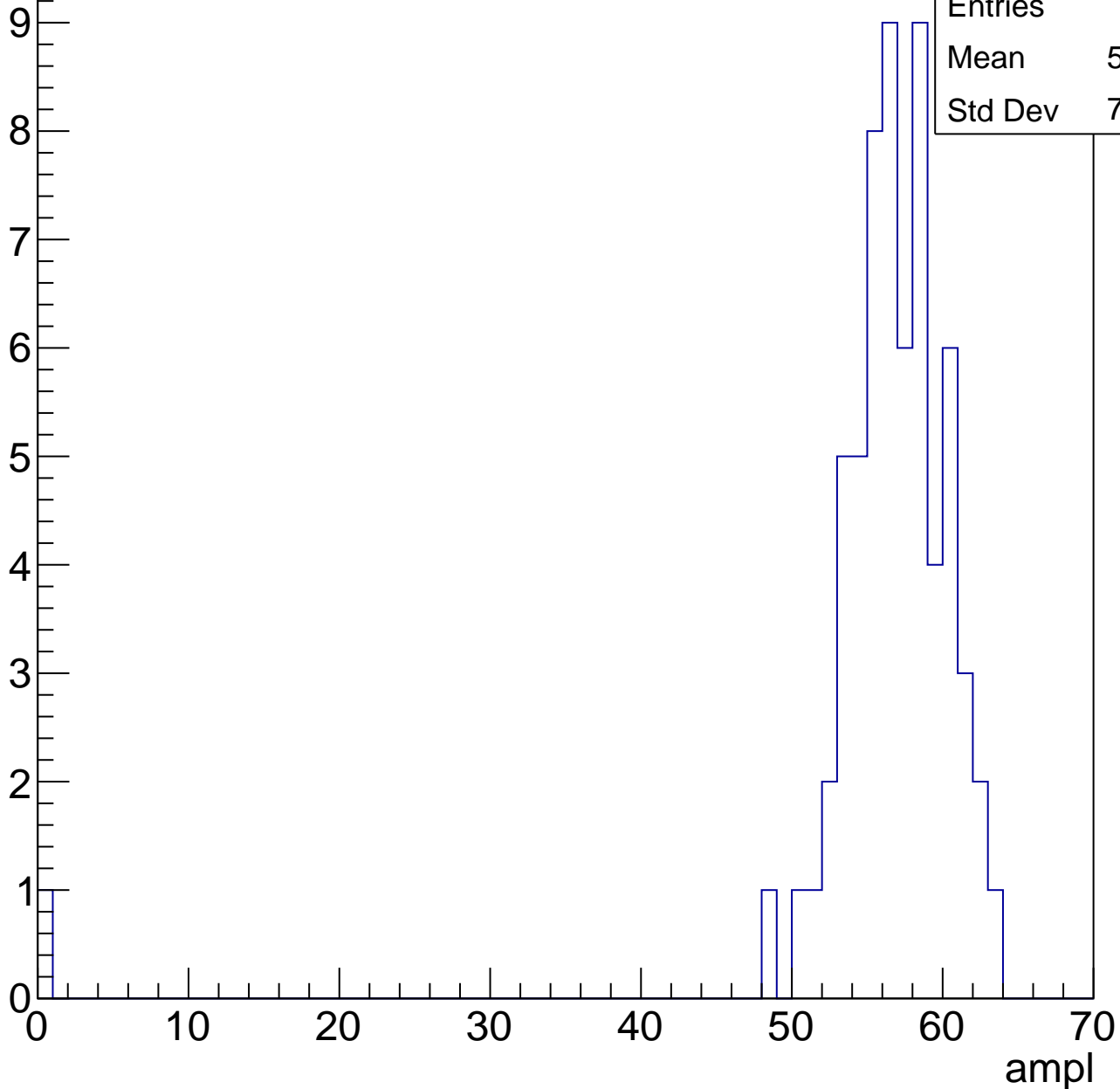


# B1L102S, U8-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	55.66
Std Dev	7.633

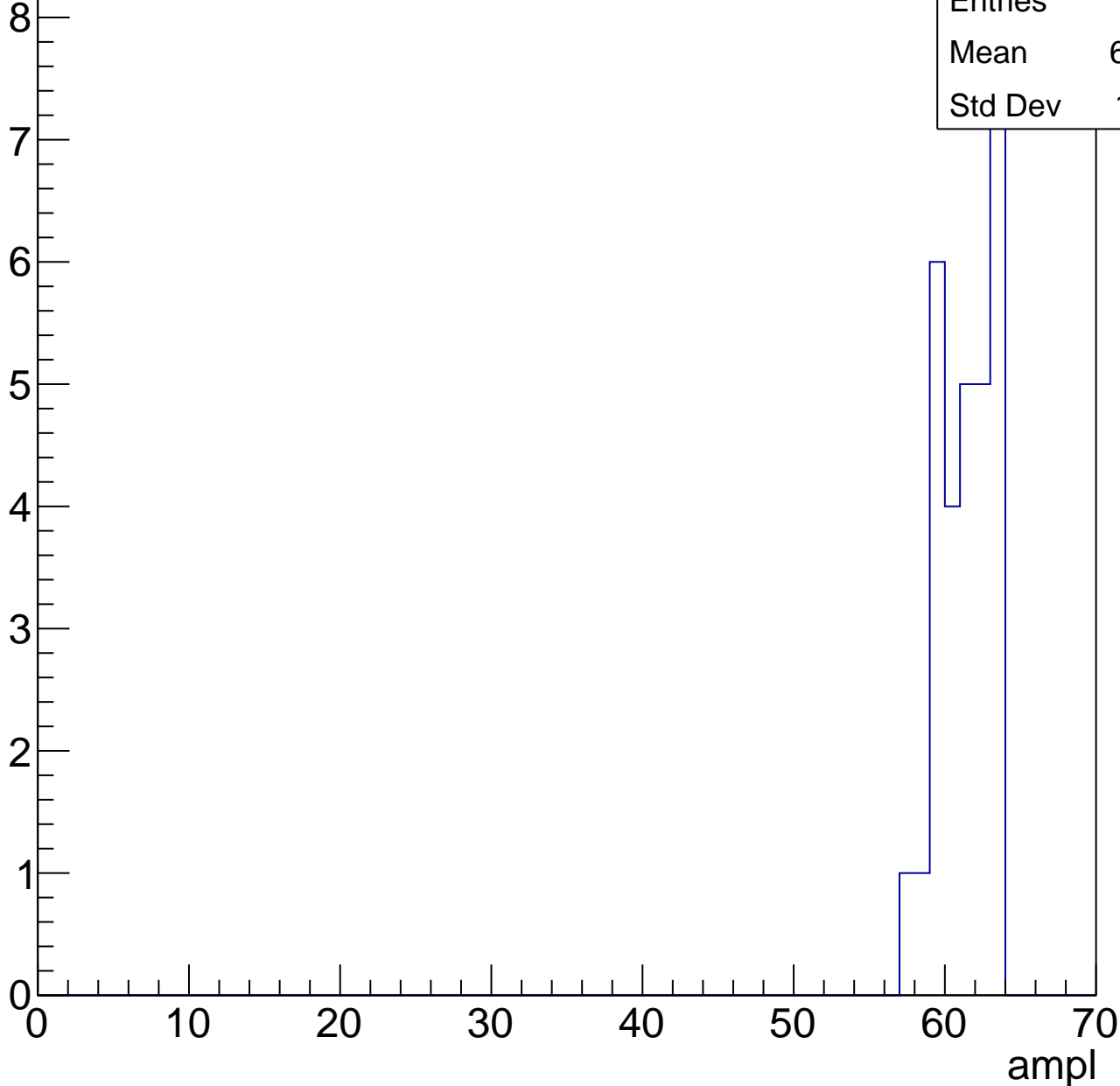


# B1L102S, U8-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

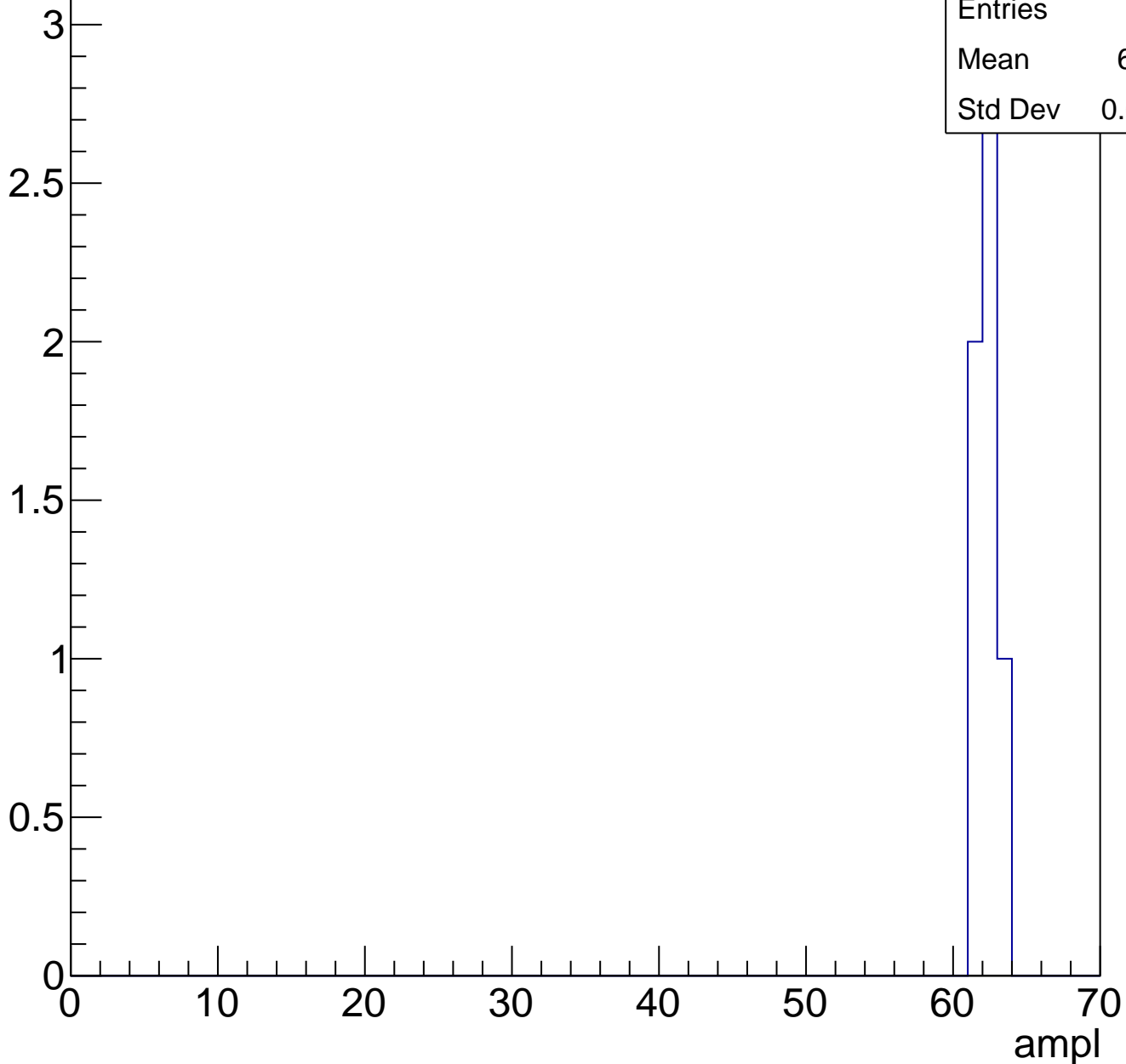
Entries	30
Mean	60.93
Std Dev	1.731



# B1L102S, U8-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch110, adc0

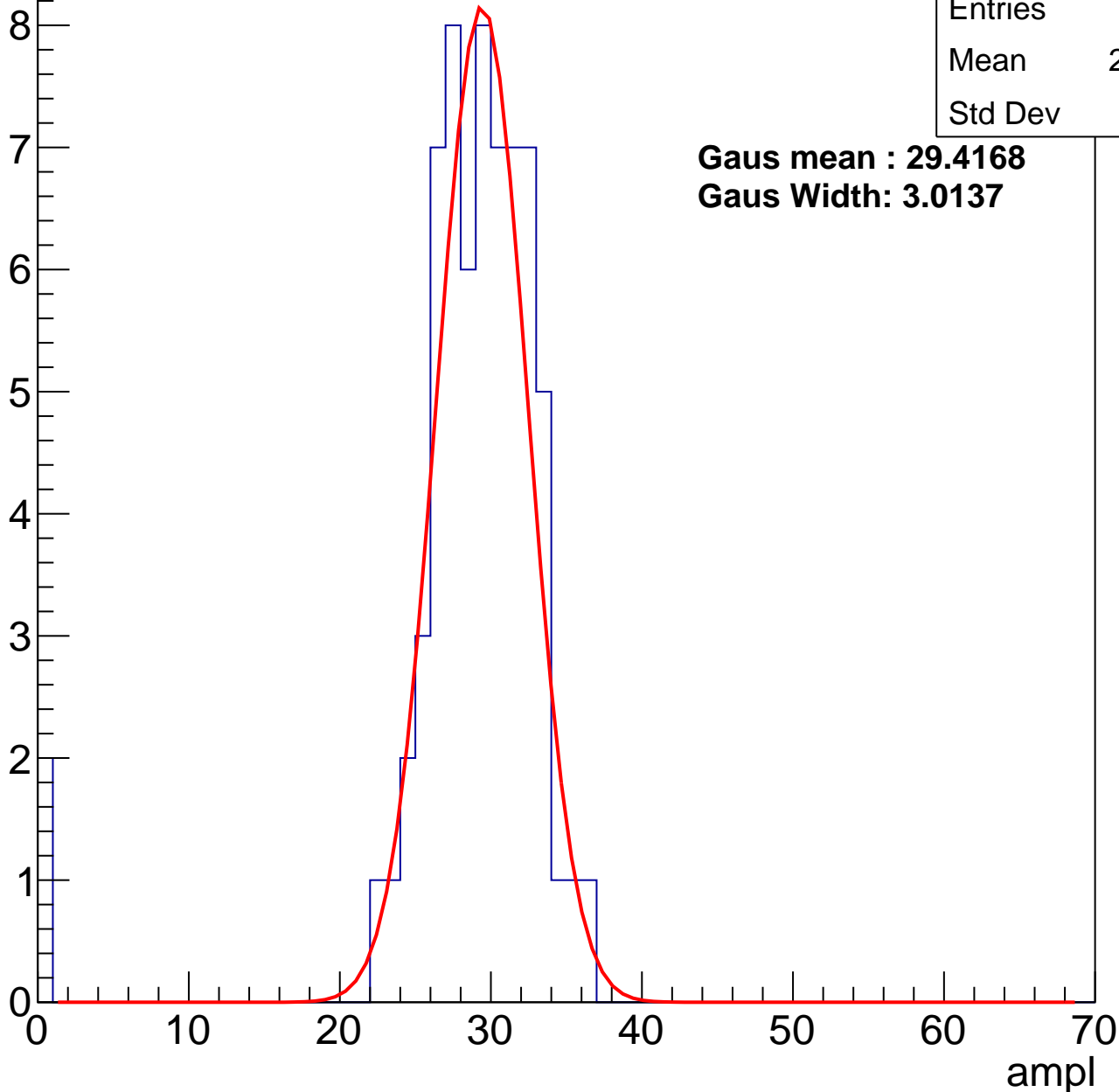
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	28.16
Std Dev	5.74

**Gaus mean : 29.4168**

**Gaus Width: 3.0137**



# B1L102S, U8-ch110, adc1

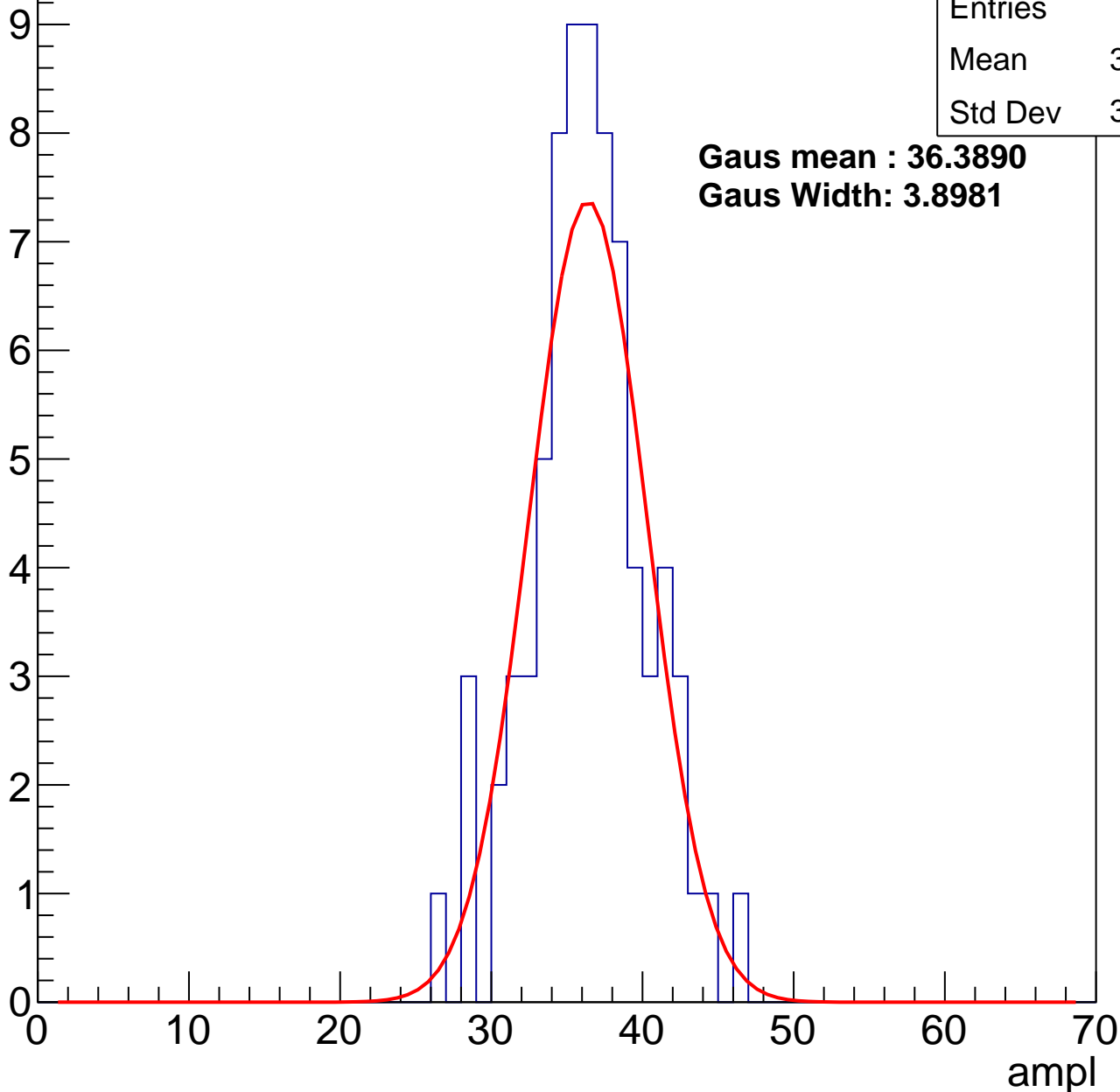
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	35.95
Std Dev	3.854

**Gaus mean : 36.3890**

**Gaus Width: 3.8981**



# B1L102S, U8-ch110, adc2

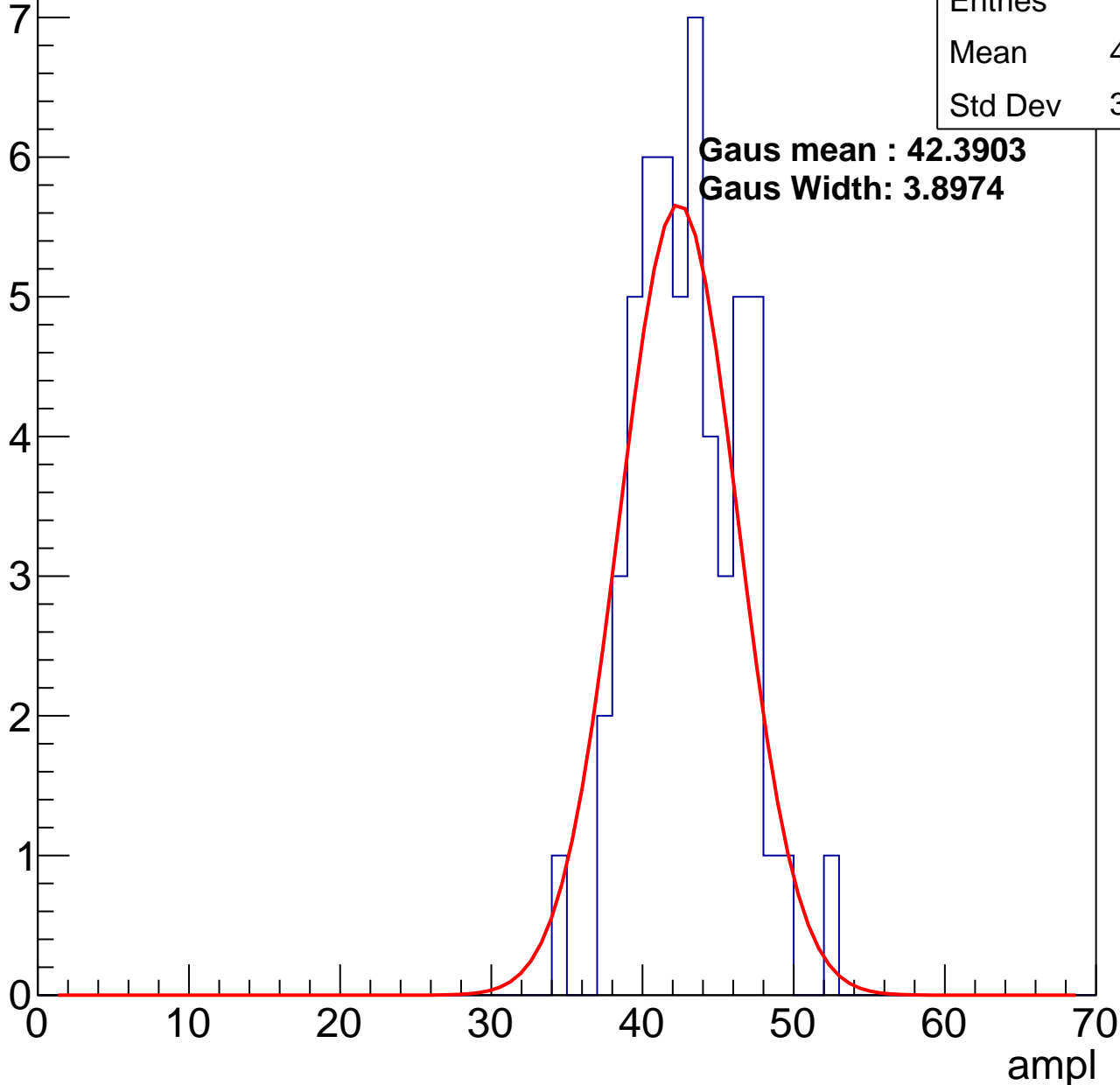
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	42.53
Std Dev	3.469

**Gaus mean : 42.3903**

**Gaus Width: 3.8974**

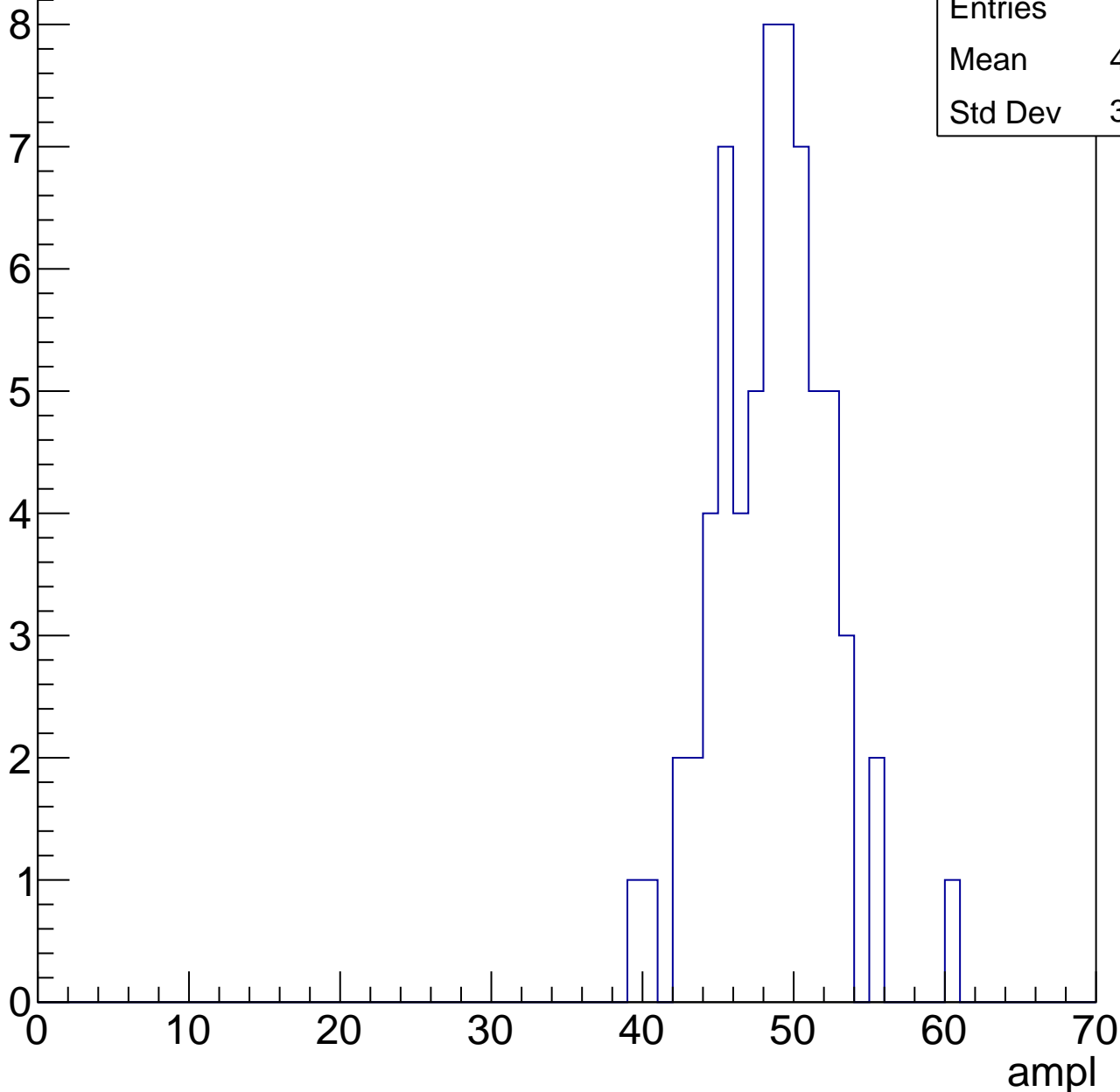


# B1L102S, U8-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	48.14
Std Dev	3.704

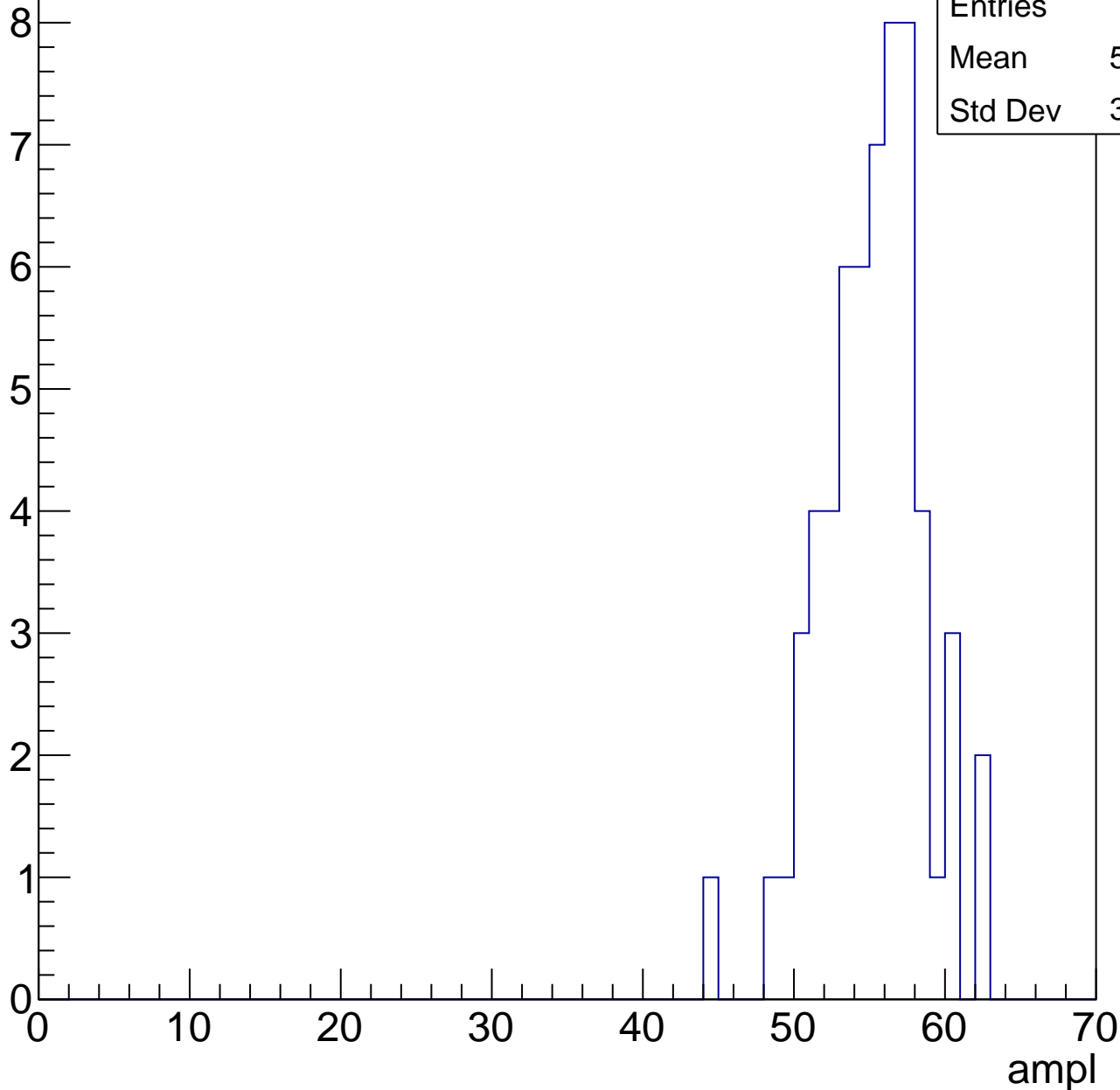


# B1L102S, U8-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	54.73
Std Dev	3.374

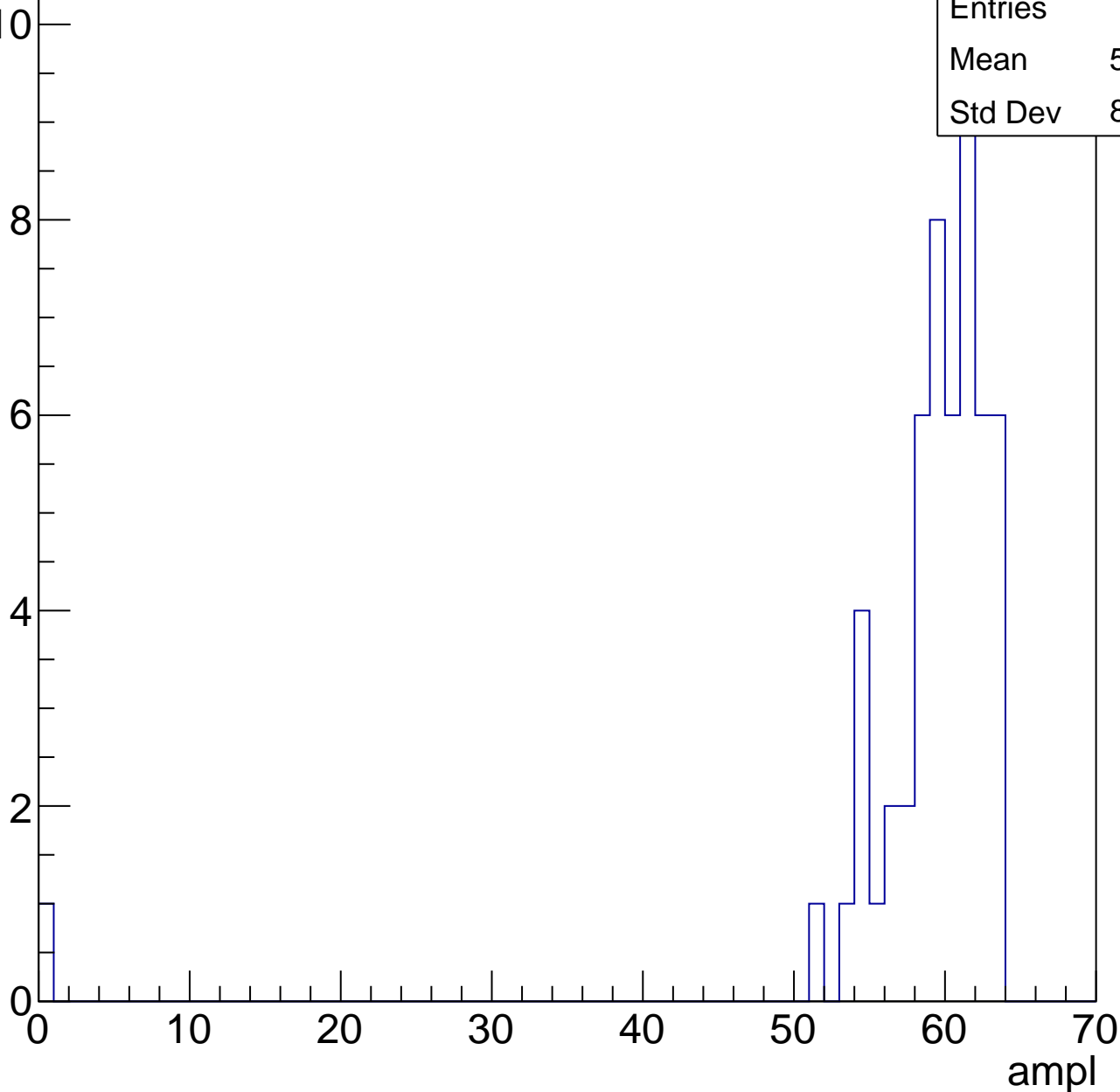


# B1L102S, U8-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

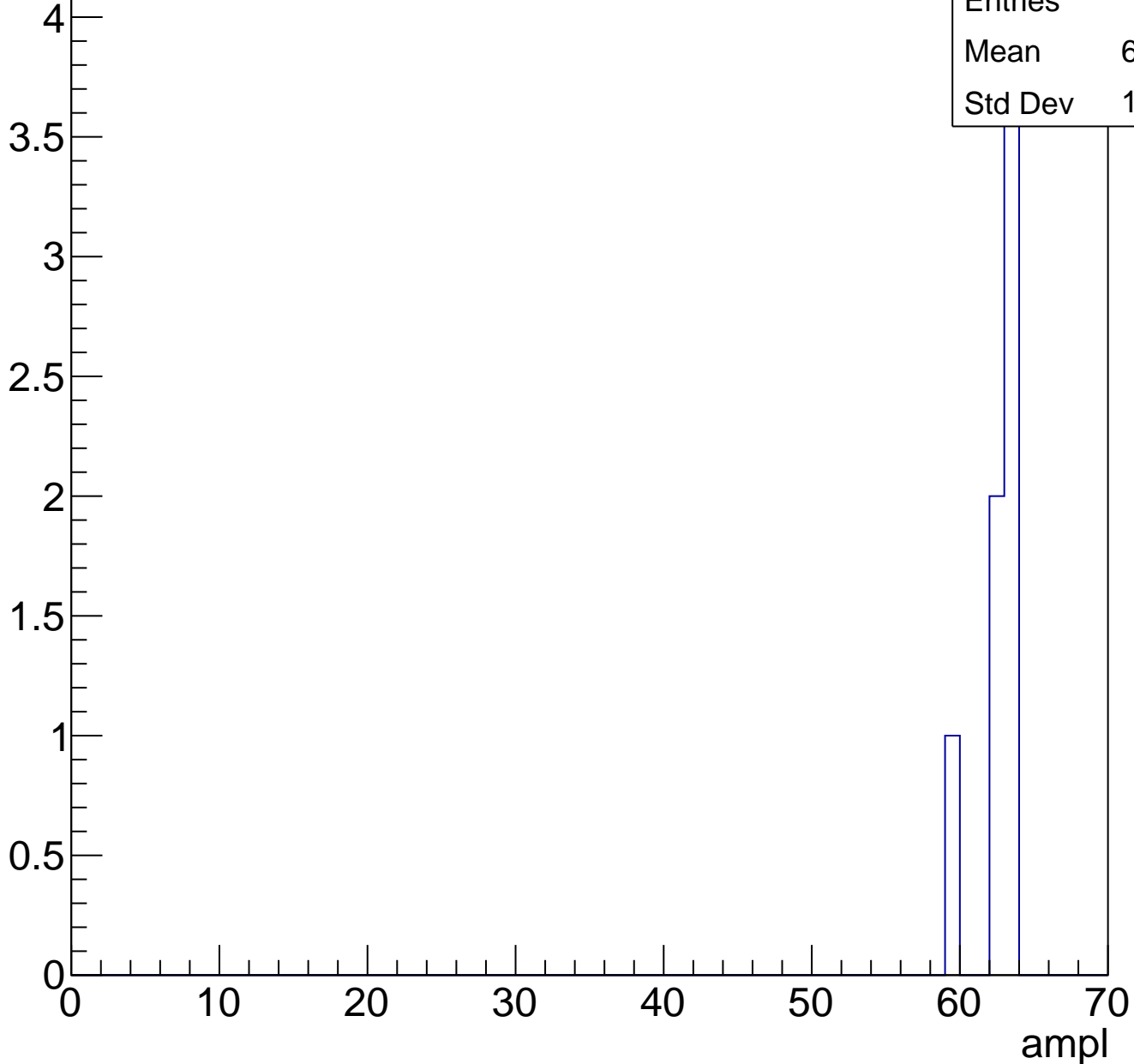
Entries	54
Mean	58.17
Std Dev	8.485



# B1L102S, U8-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch111, adc0

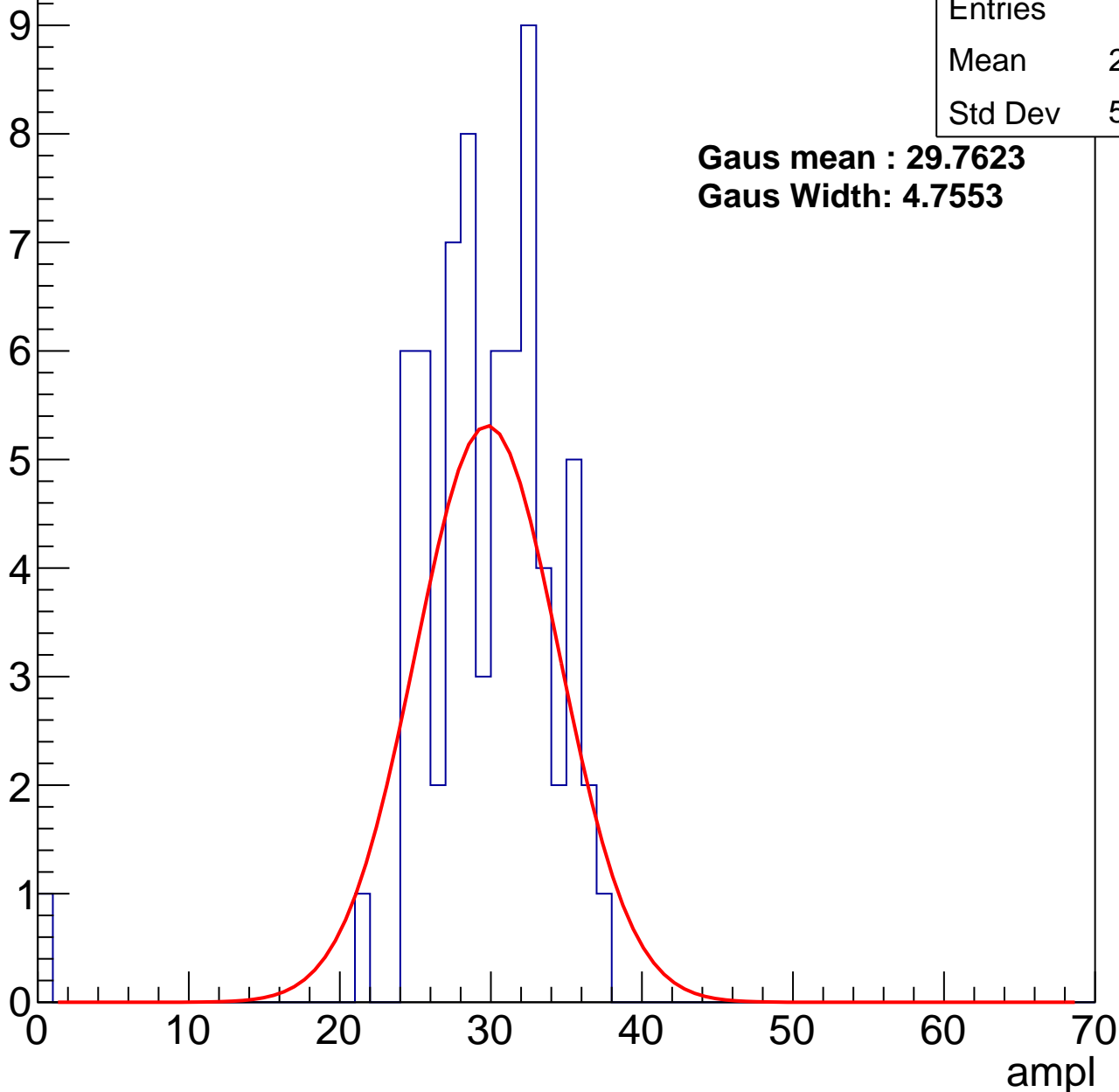
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	29.06
Std Dev	5.067

**Gaus mean : 29.7623**

**Gaus Width: 4.7553**



# B1L102S, U8-ch111, adc1

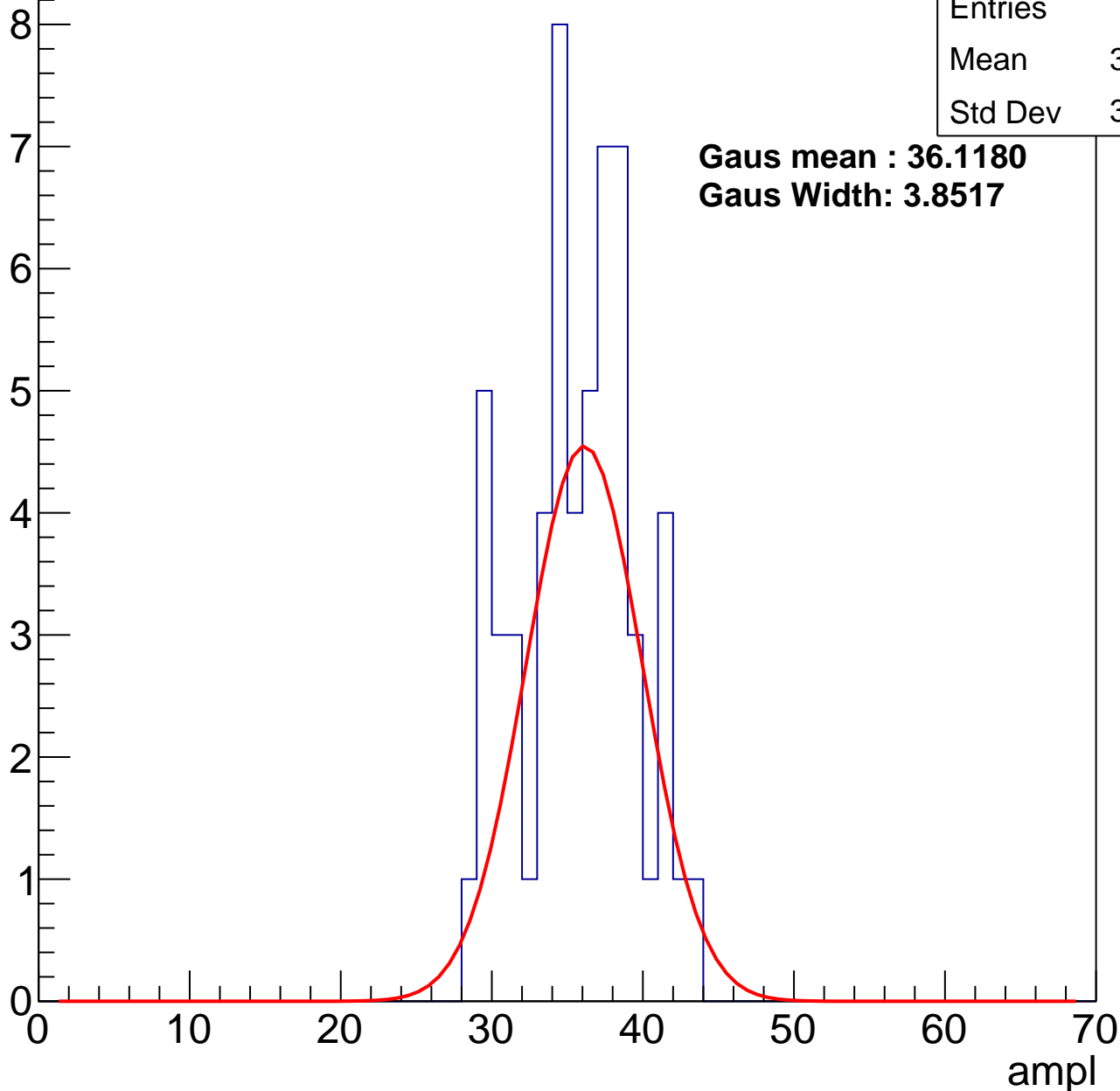
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	35.22
Std Dev	3.733

**Gaus mean : 36.1180**

**Gaus Width: 3.8517**



# B1L102S, U8-ch111, adc2

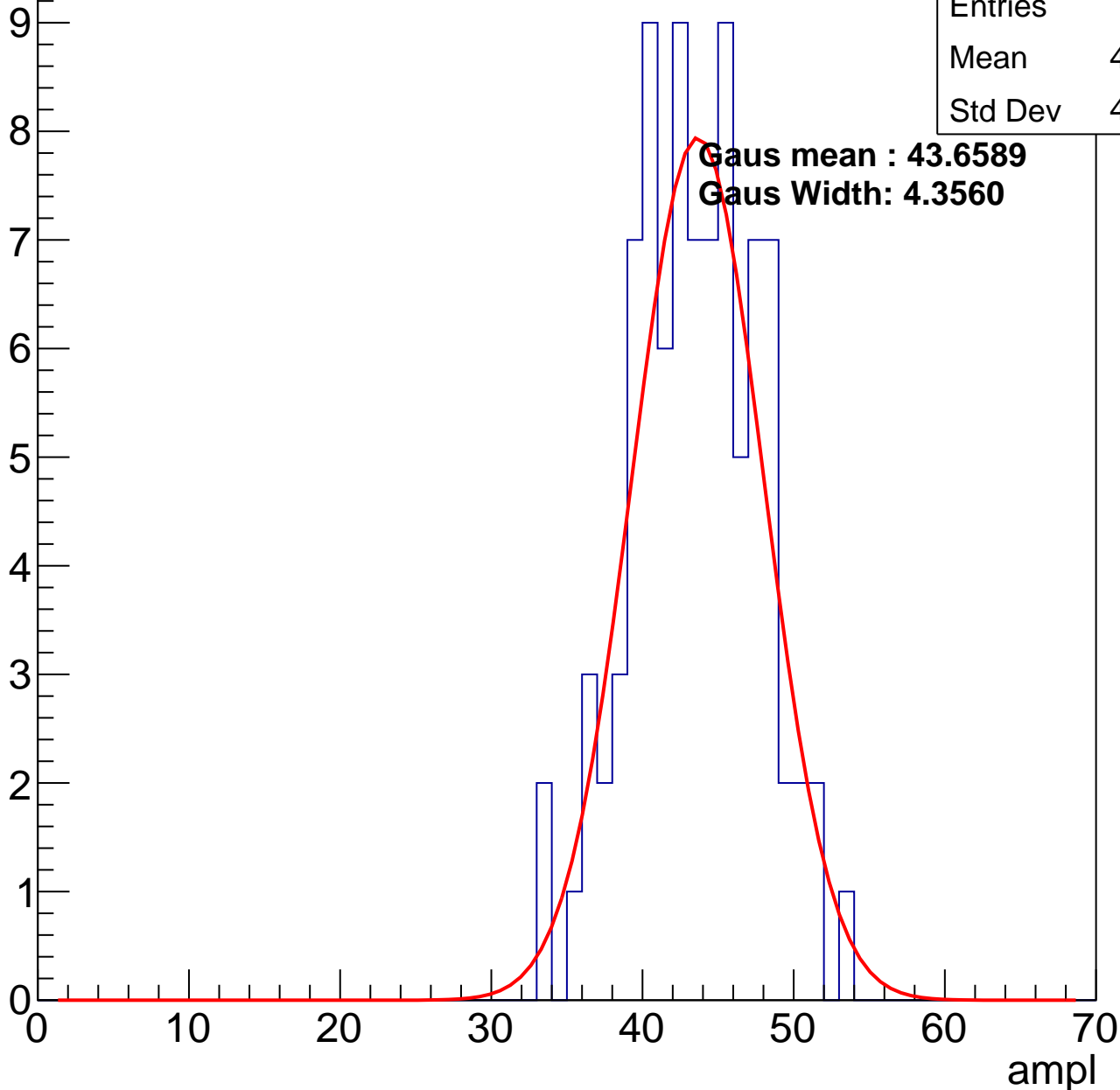
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	91
Mean	43.03
Std Dev	4.136

**Gaus mean : 43.6589**

**Gaus Width: 4.3560**

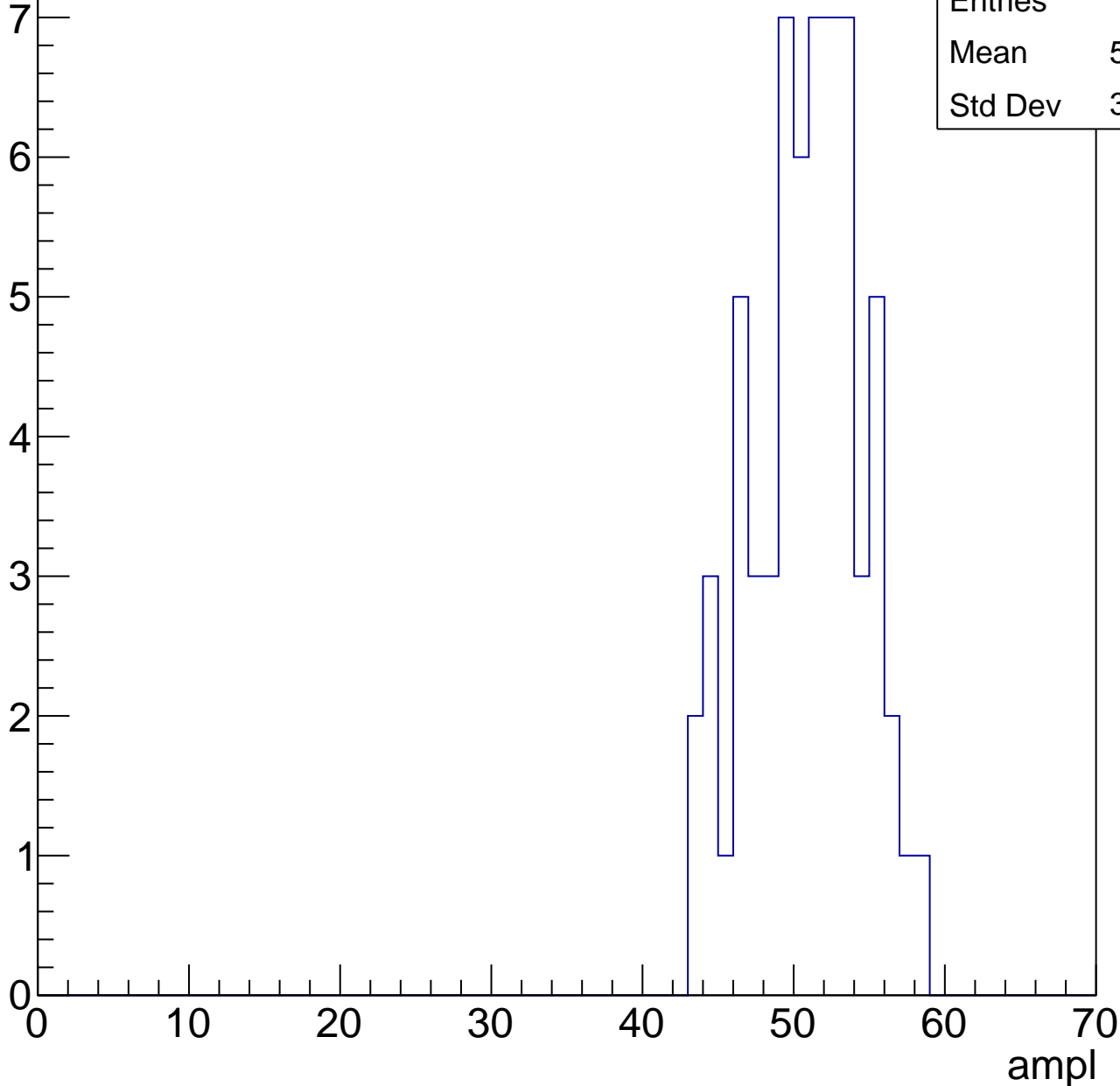


# B1L102S, U8-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	50.43
Std Dev	3.567

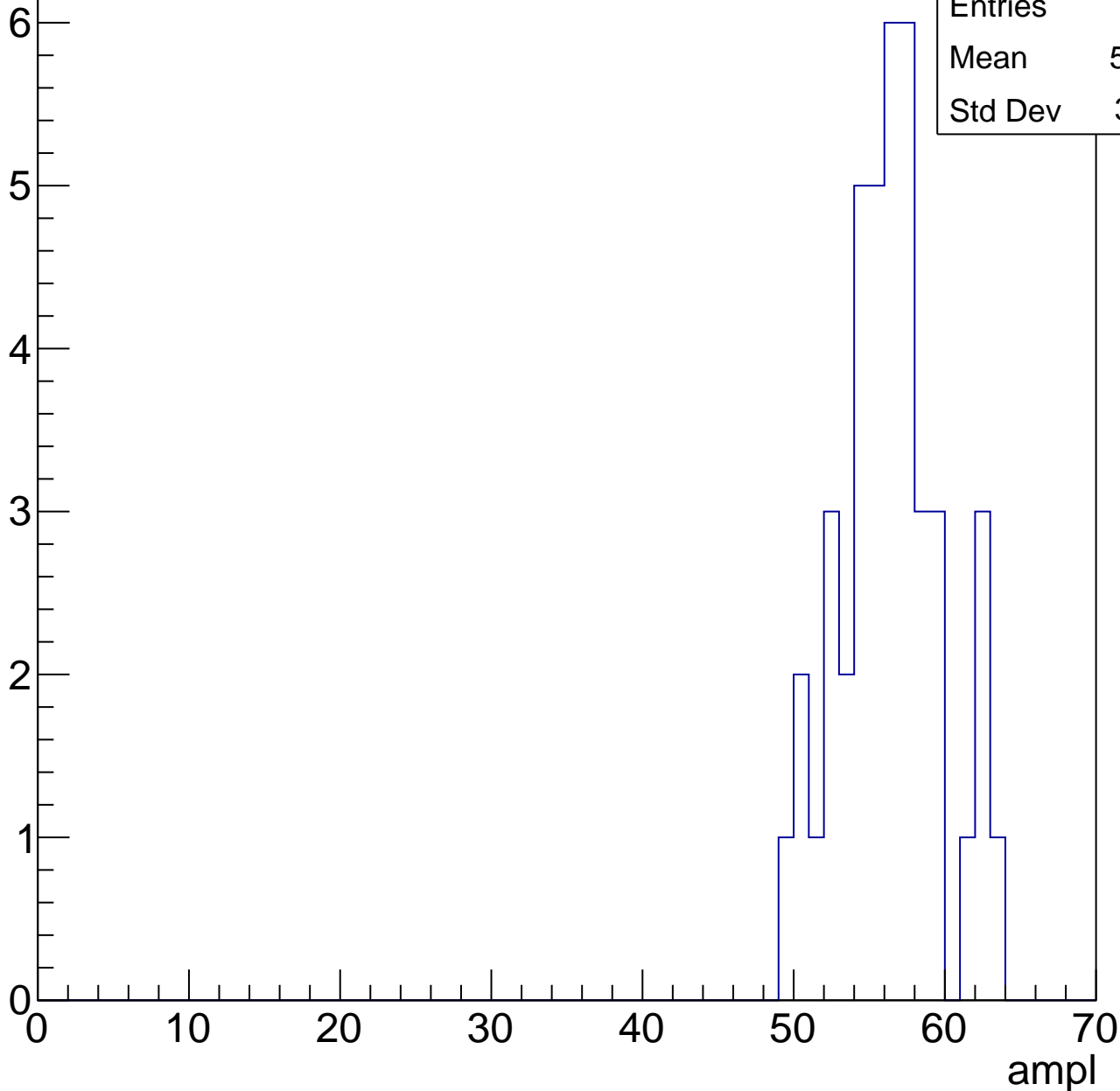


# B1L102S, U8-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	42
Mean	55.86
Std Dev	3.321

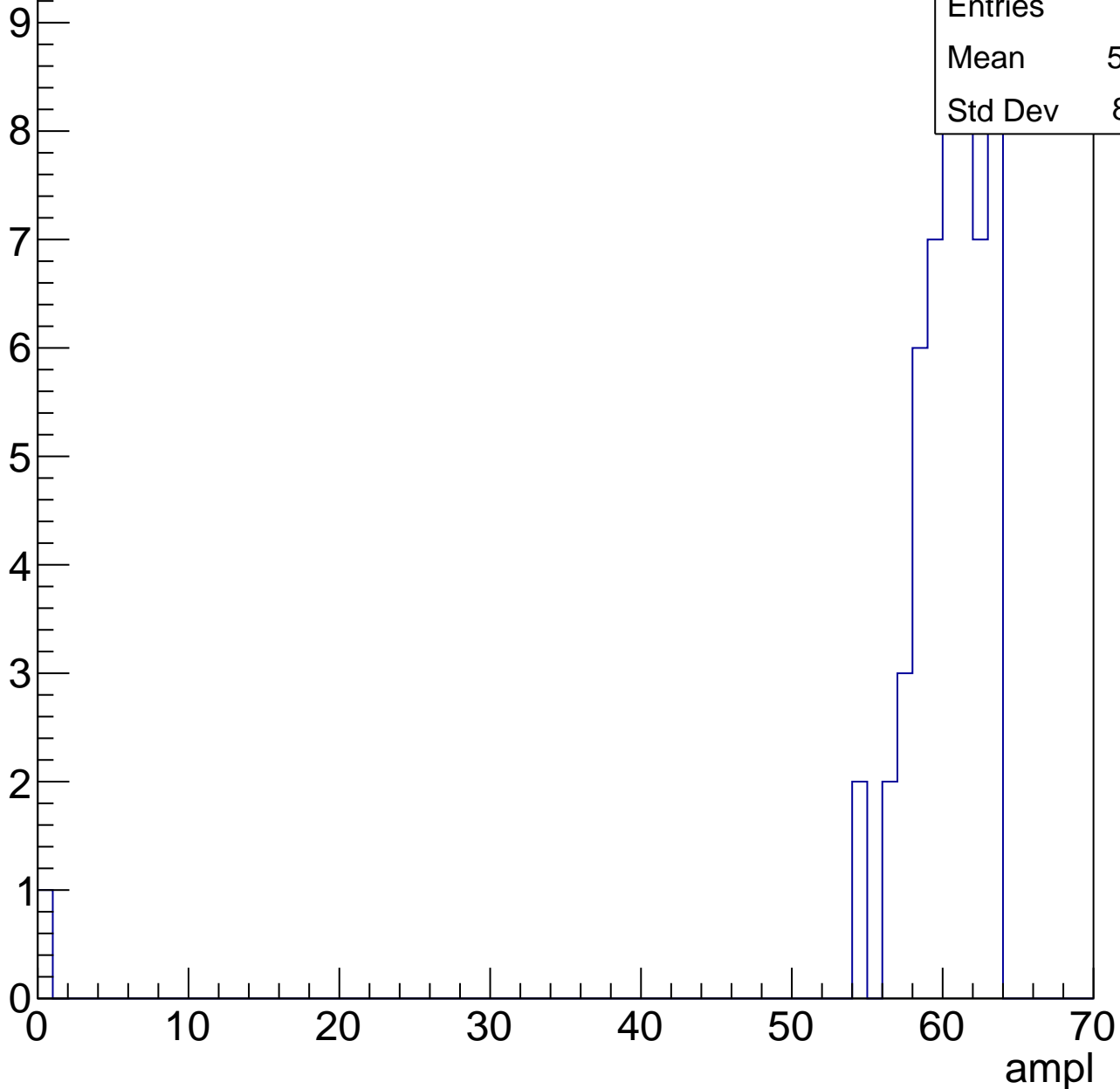


# B1L102S, U8-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	58.87
Std Dev	8.391



# B1L102S, U8-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

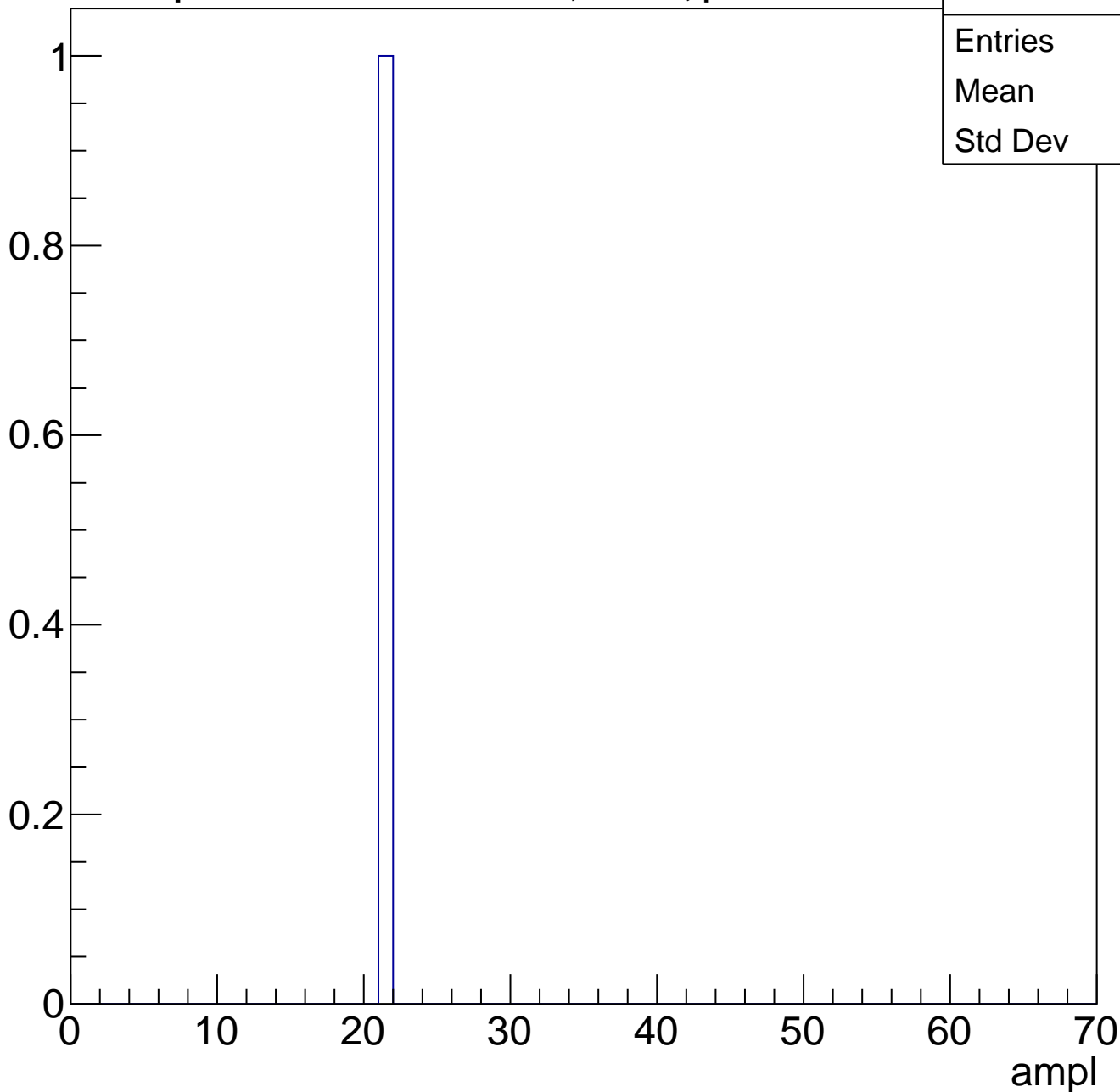




# B1L102S, U8-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch112, adc0

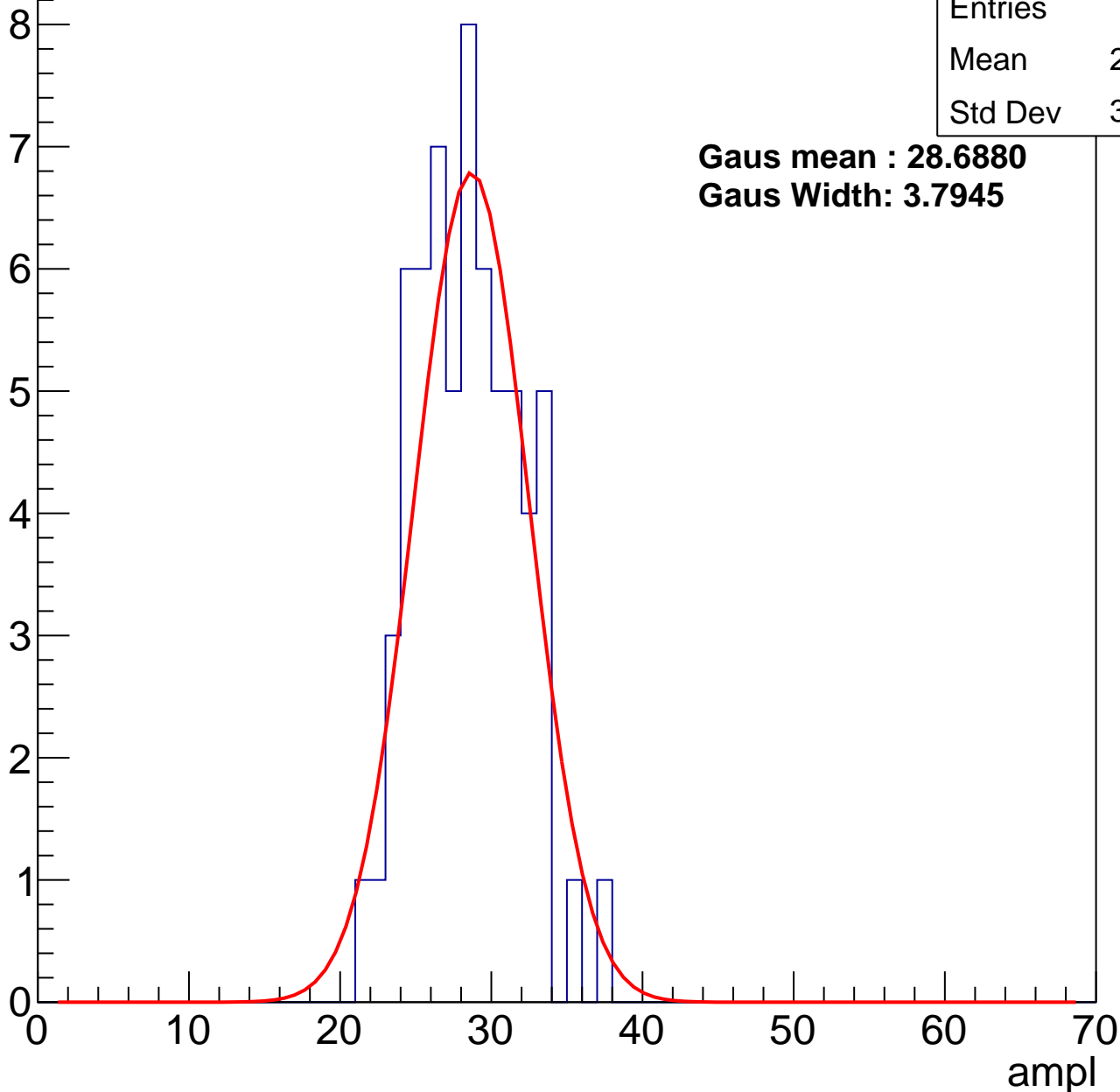
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	27.98
Std Dev	3.384

**Gaus mean : 28.6880**

**Gaus Width: 3.7945**



# B1L102S, U8-ch112, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	86
Mean	35.22
Std Dev	3.963

**Gaus mean : 35.6458**

**Gaus Width: 5.0310**

Entry

10  
8  
6  
4  
2  
0

ampl

0

10

20

30

40

50

60

70

# B1L102S, U8-ch112, adc2

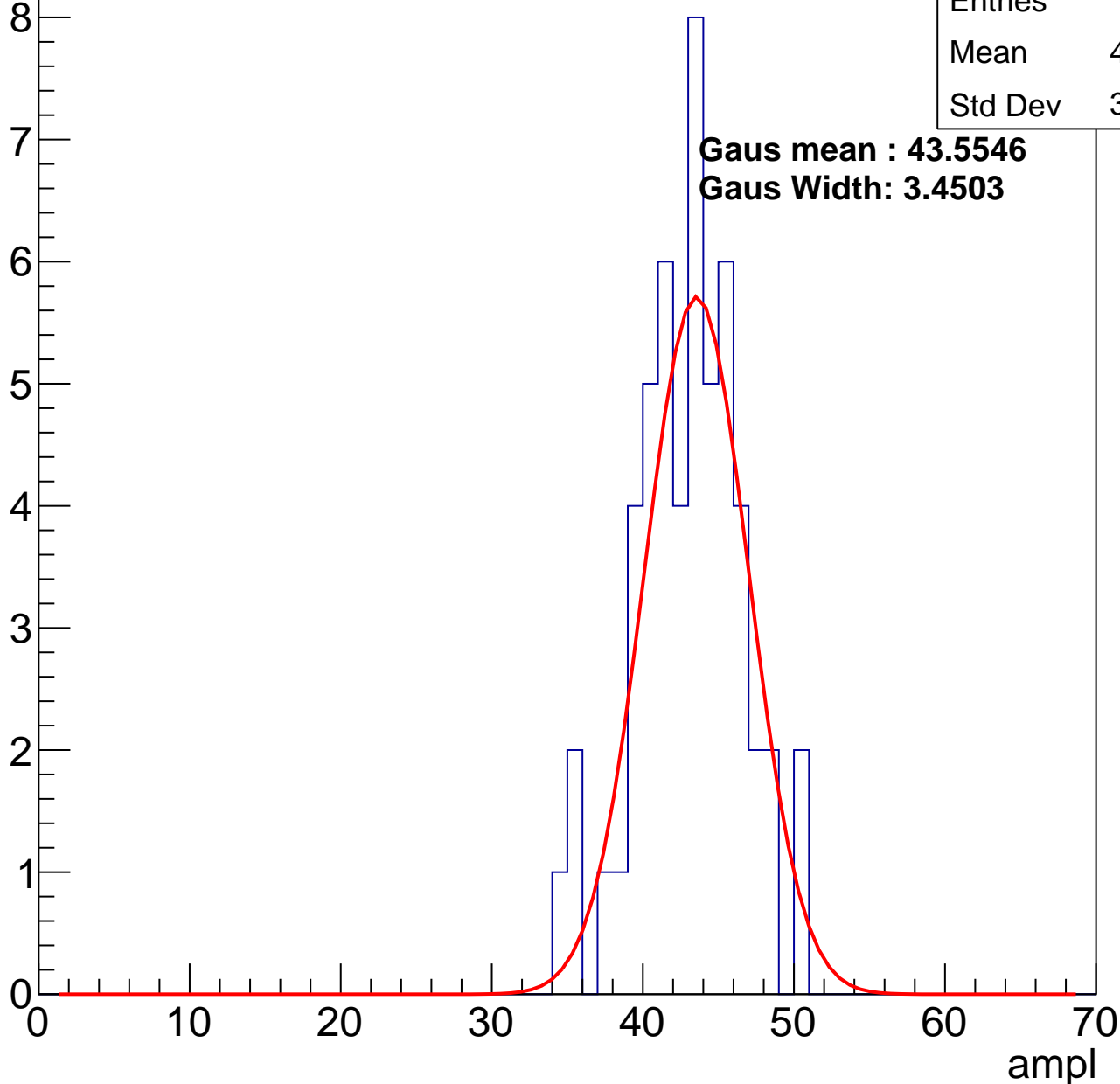
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	42.58
Std Dev	3.483

**Gaus mean : 43.5546**

**Gaus Width: 3.4503**

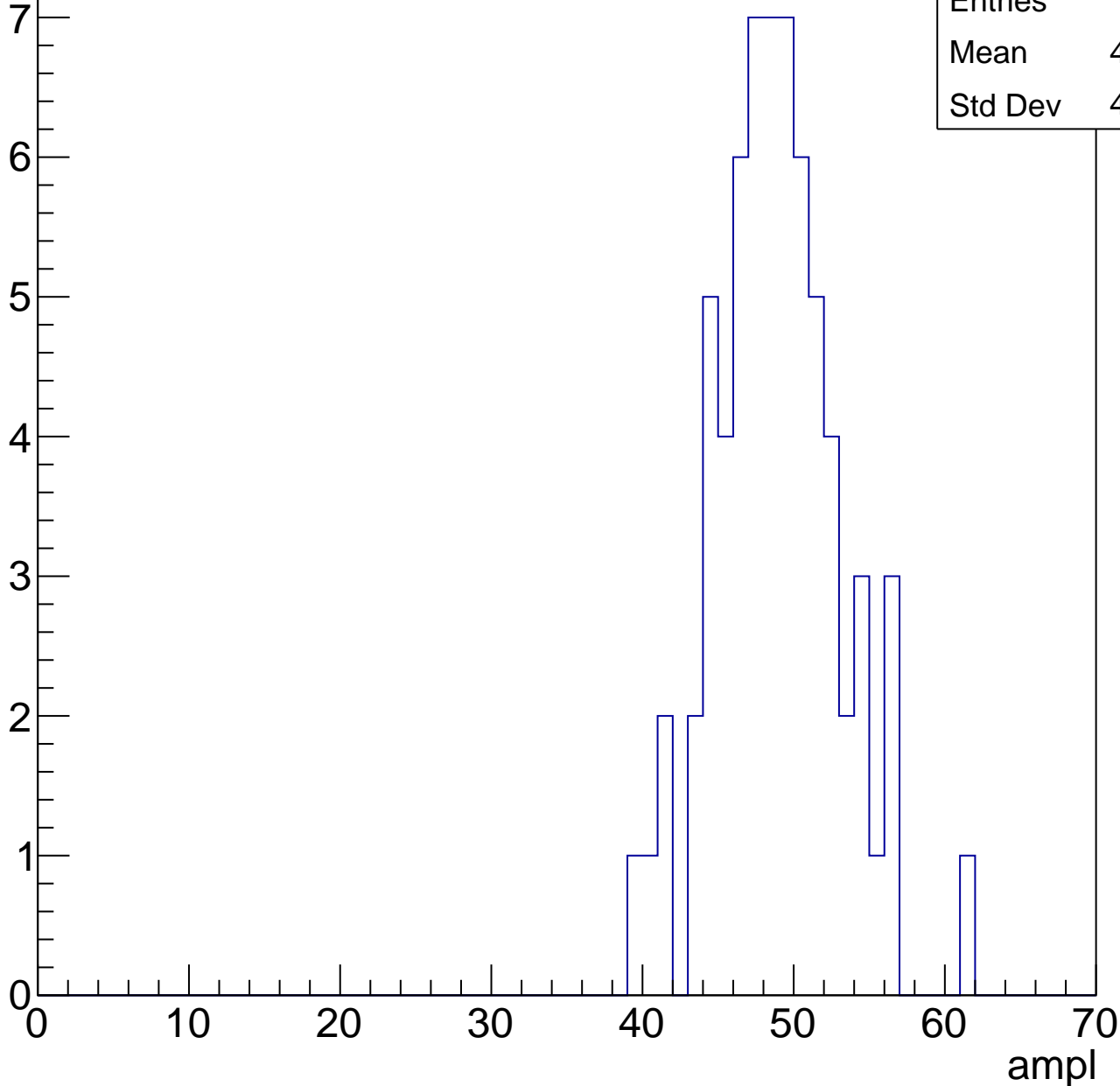


# B1L102S, U8-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

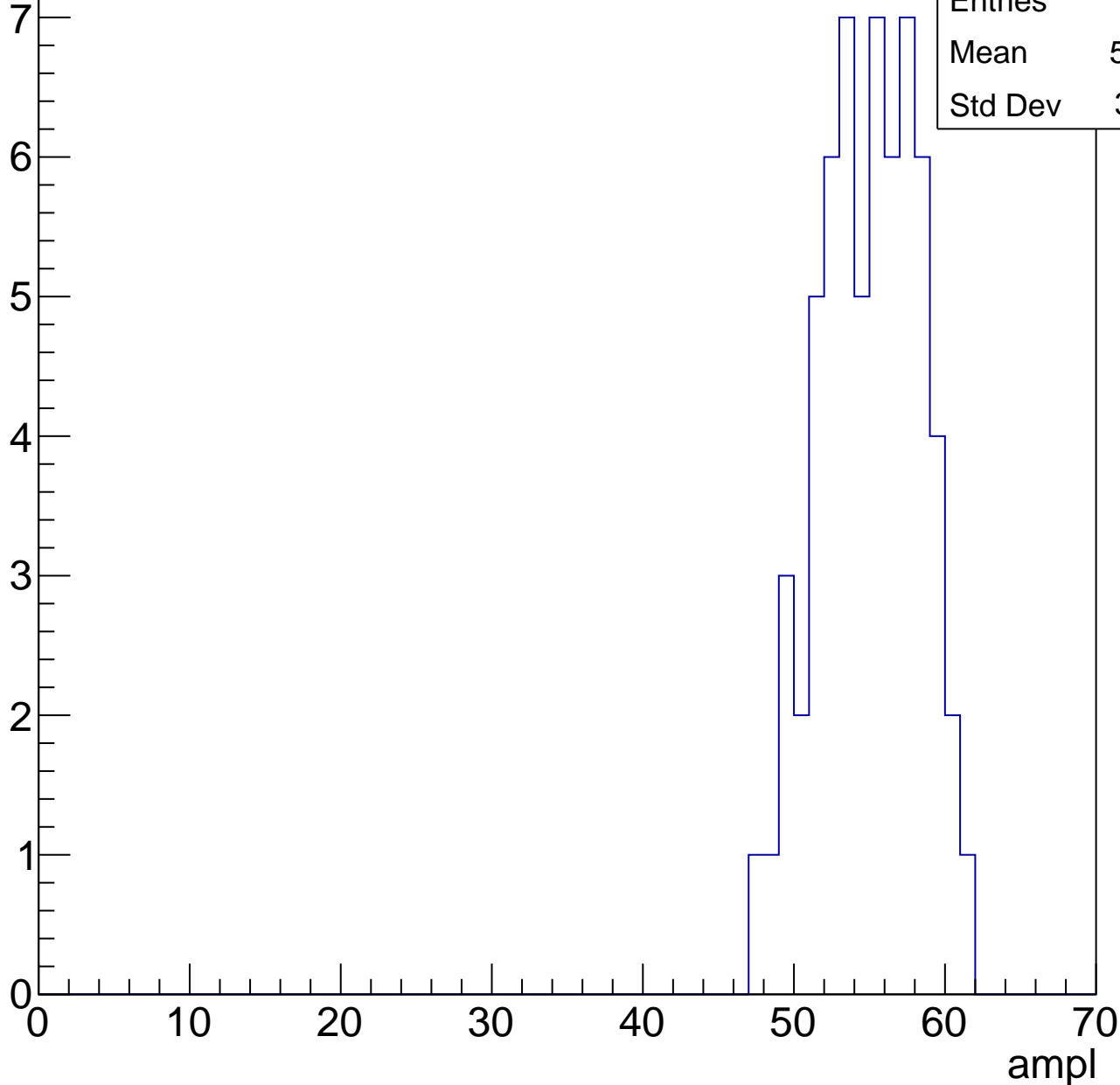
Entries	67
Mean	48.45
Std Dev	4.115



# B1L102S, U8-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

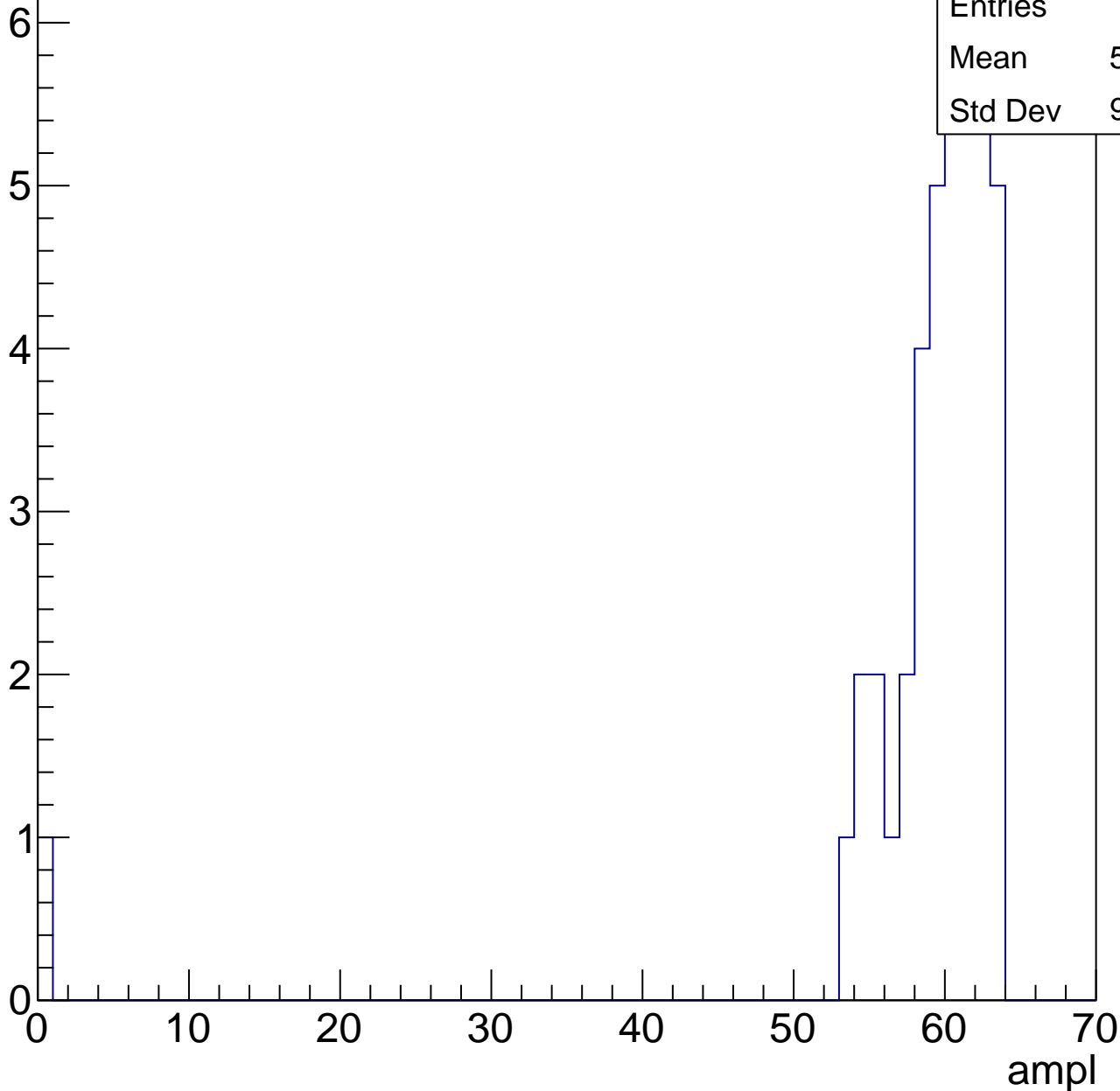


# B1L102S, U8-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

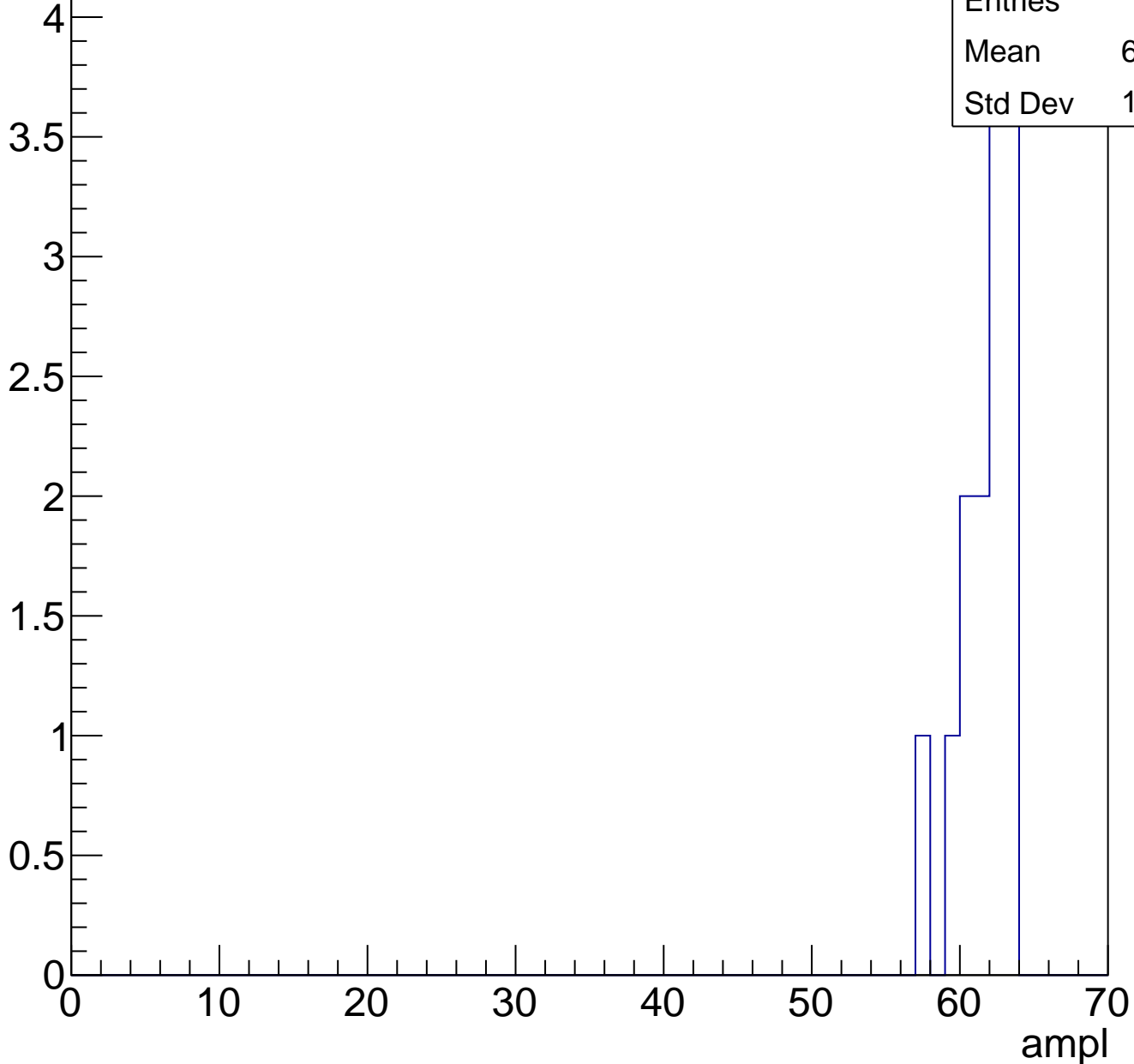
Entries	41
Mean	58.07
Std Dev	9.562



# B1L102S, U8-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch113, adc0

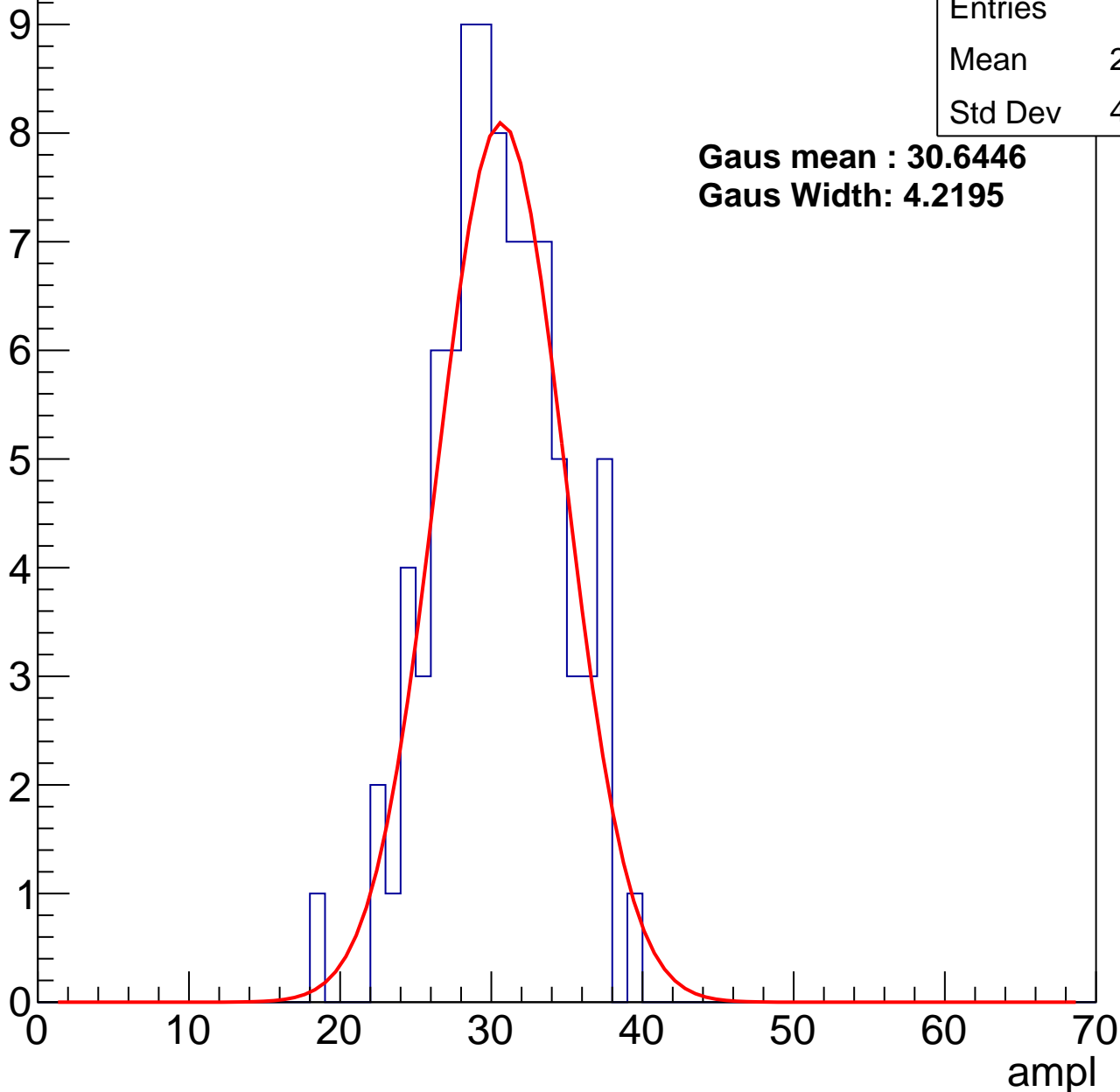
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	87
Mean	29.95
Std Dev	4.043

**Gaus mean : 30.6446**

**Gaus Width: 4.2195**



# B1L102S, U8-ch113, adc1

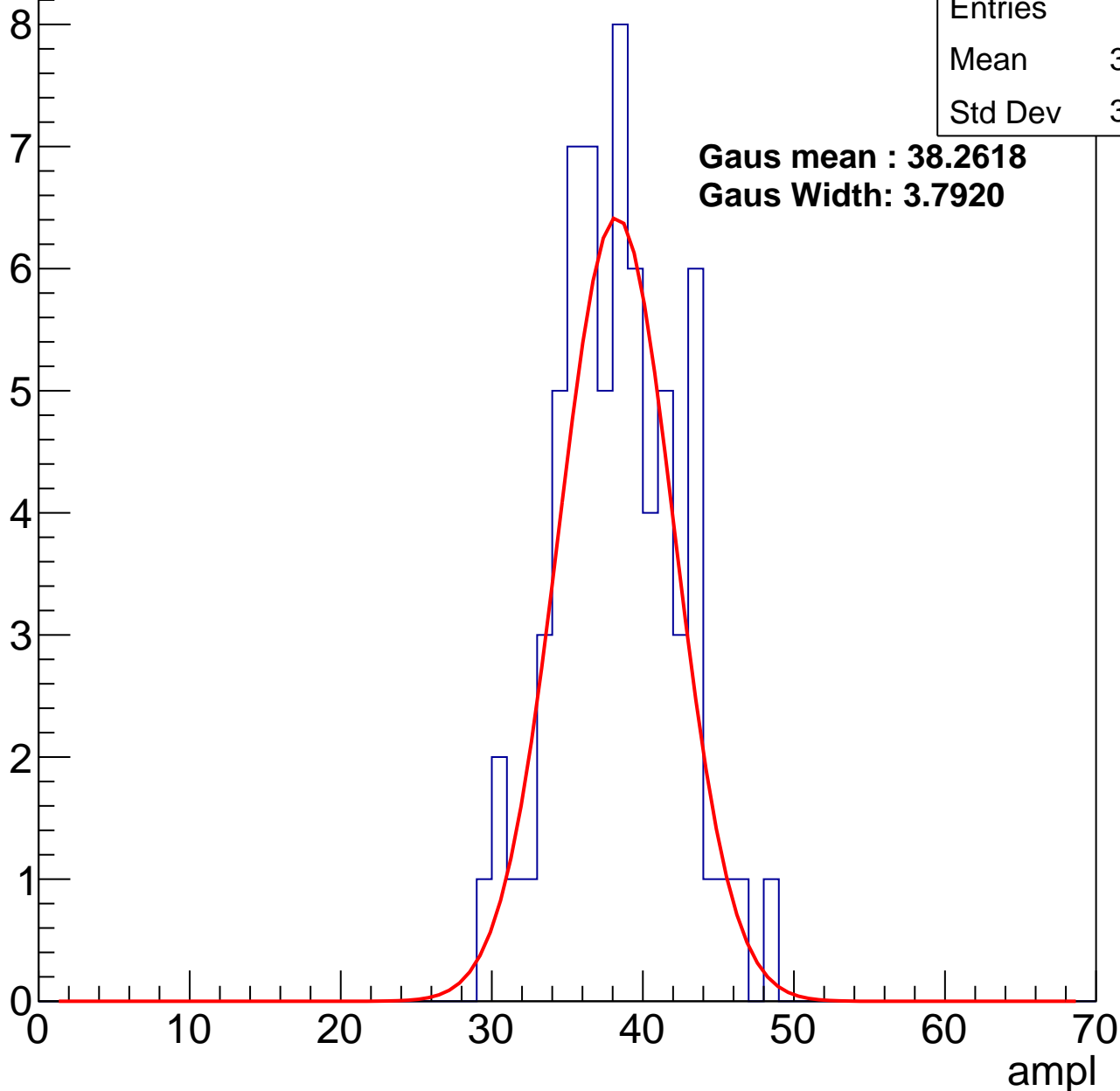
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	37.84
Std Dev	3.943

**Gaus mean : 38.2618**

**Gaus Width: 3.7920**



# B1L102S, U8-ch113, adc2

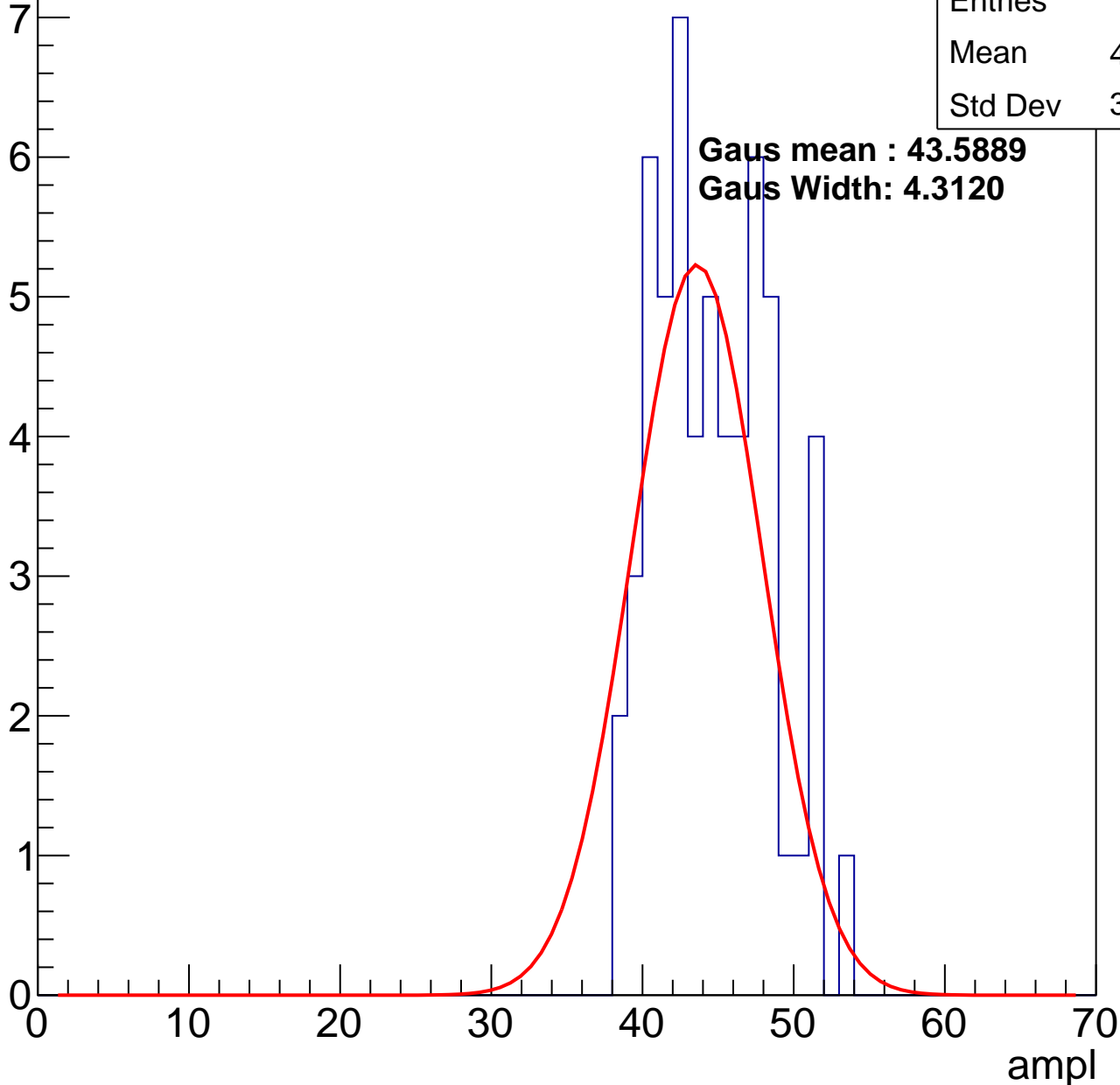
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	44.24
Std Dev	3.734

**Gaus mean : 43.5889**

**Gaus Width: 4.3120**

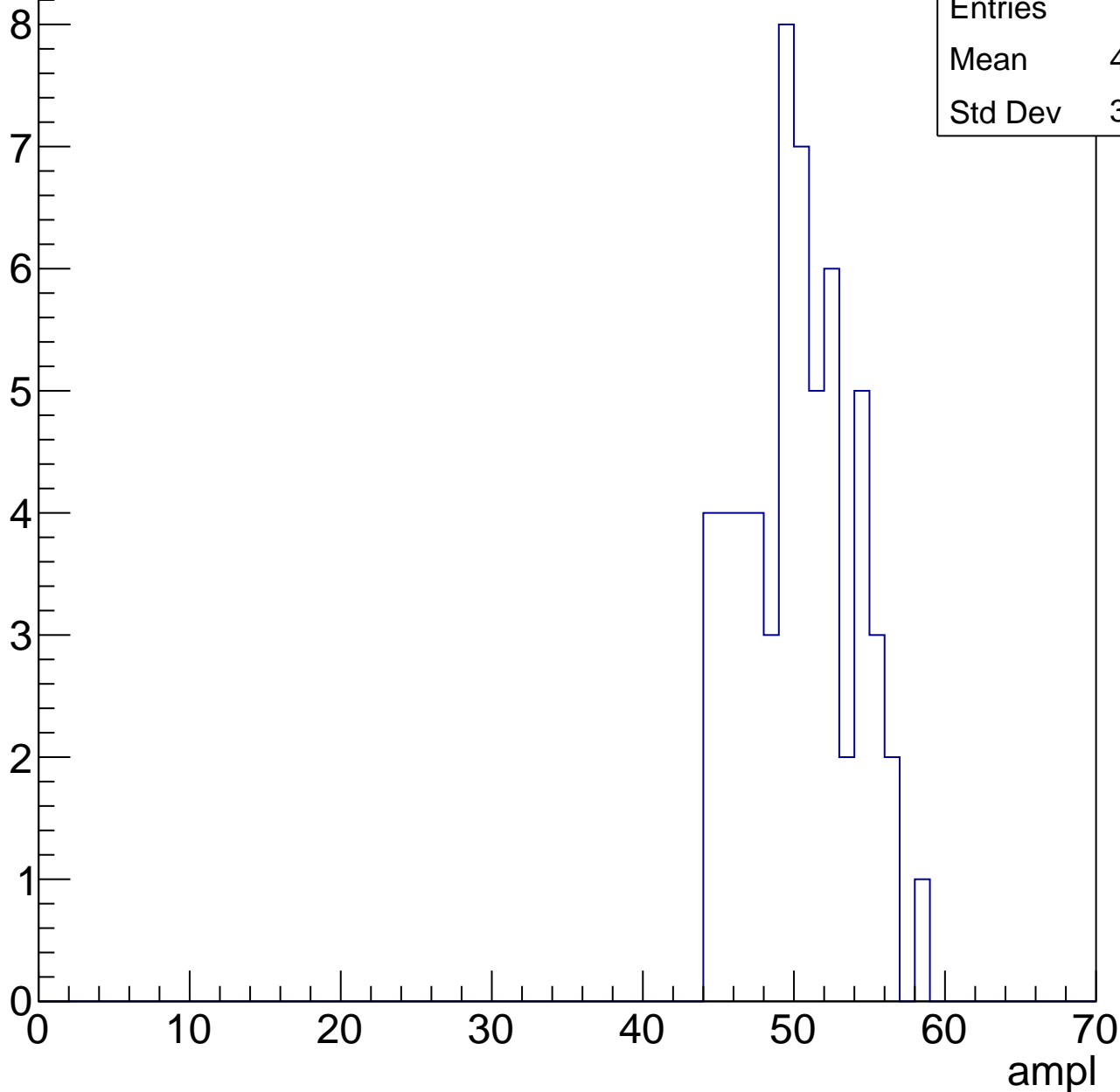


# B1L102S, U8-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	49.86
Std Dev	3.476

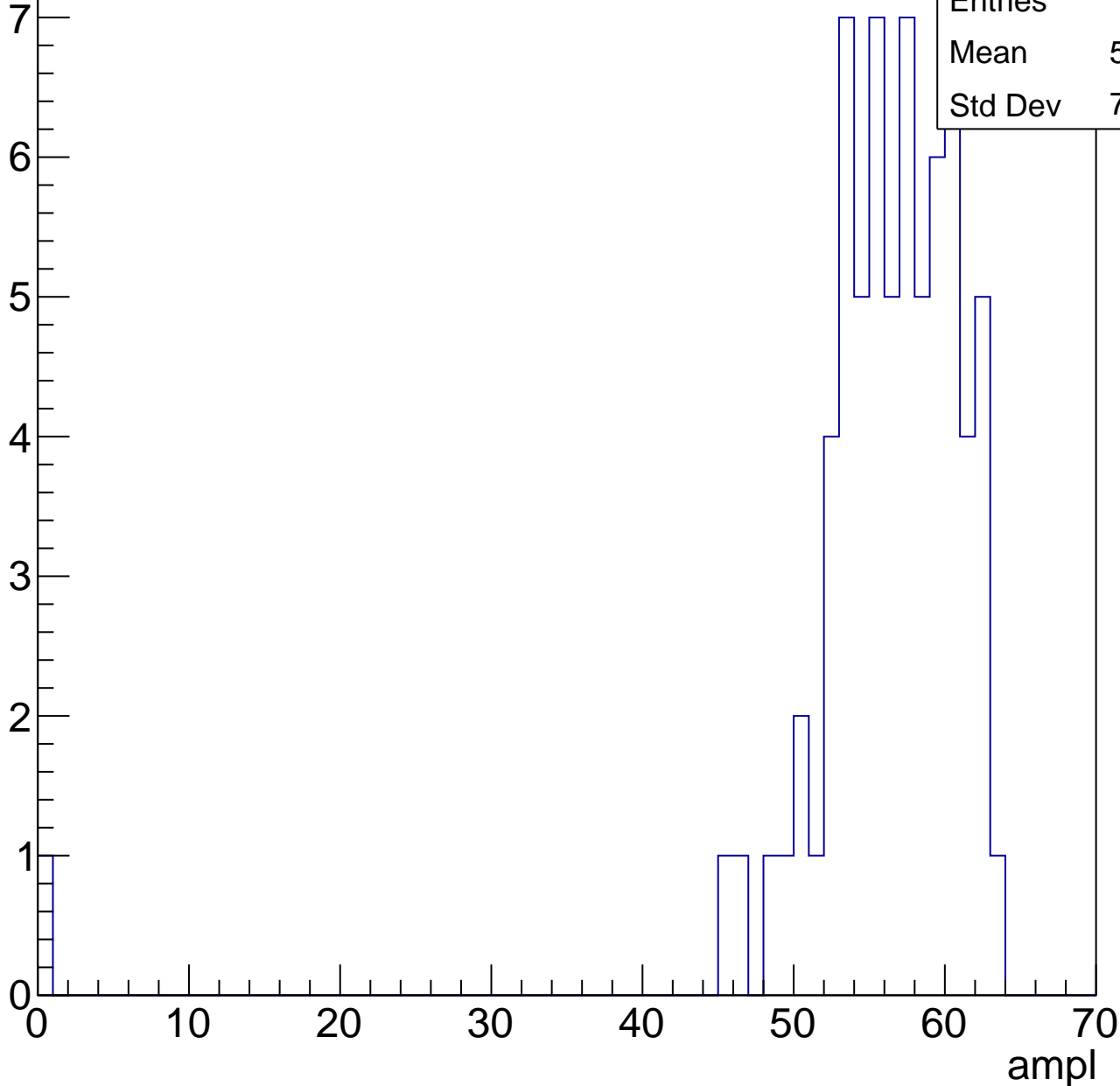


# B1L102S, U8-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	55.39
Std Dev	7.707

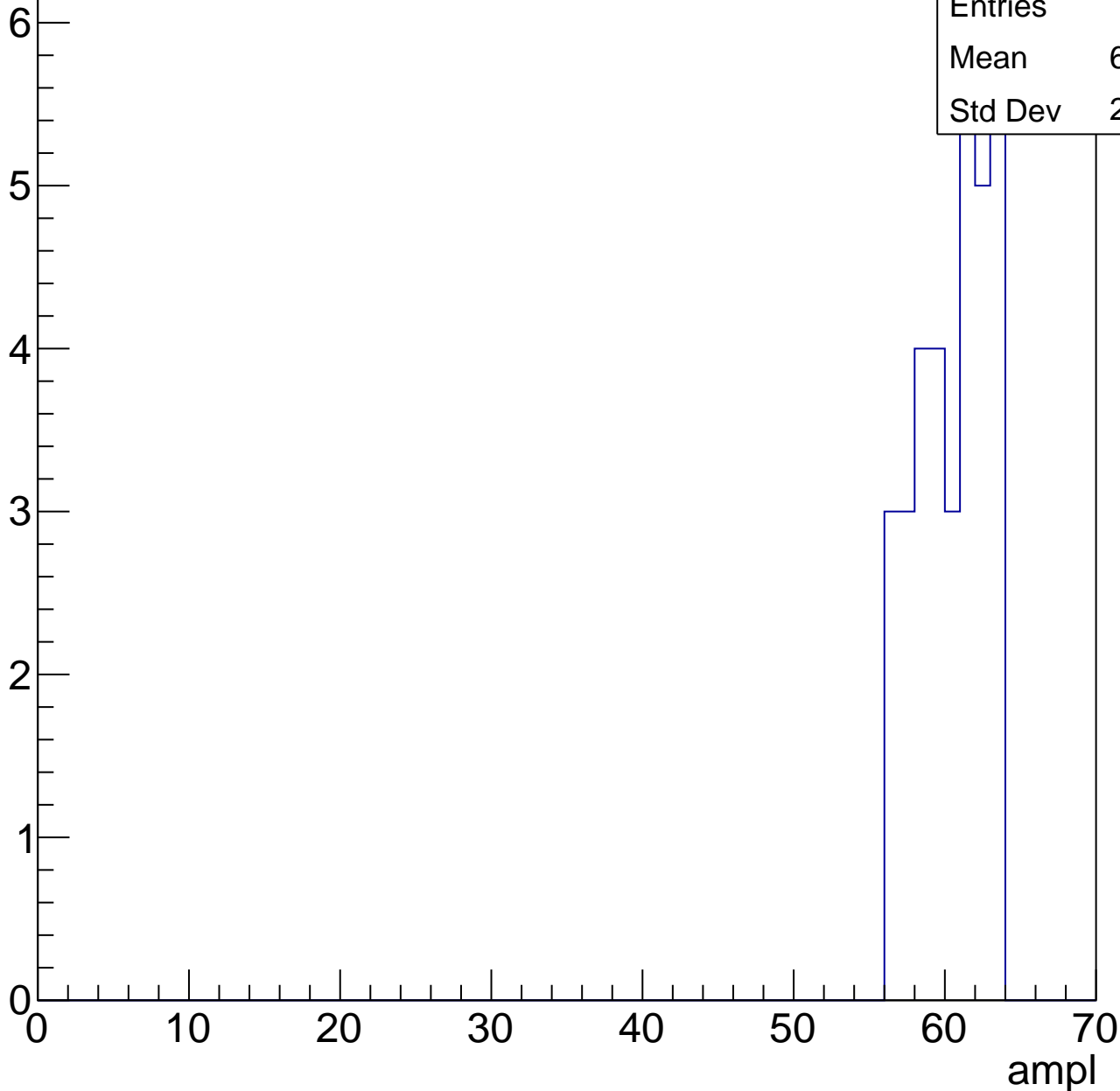


# B1L102S, U8-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	34
Mean	60.03
Std Dev	2.269



# B1L102S, U8-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch114, adc0

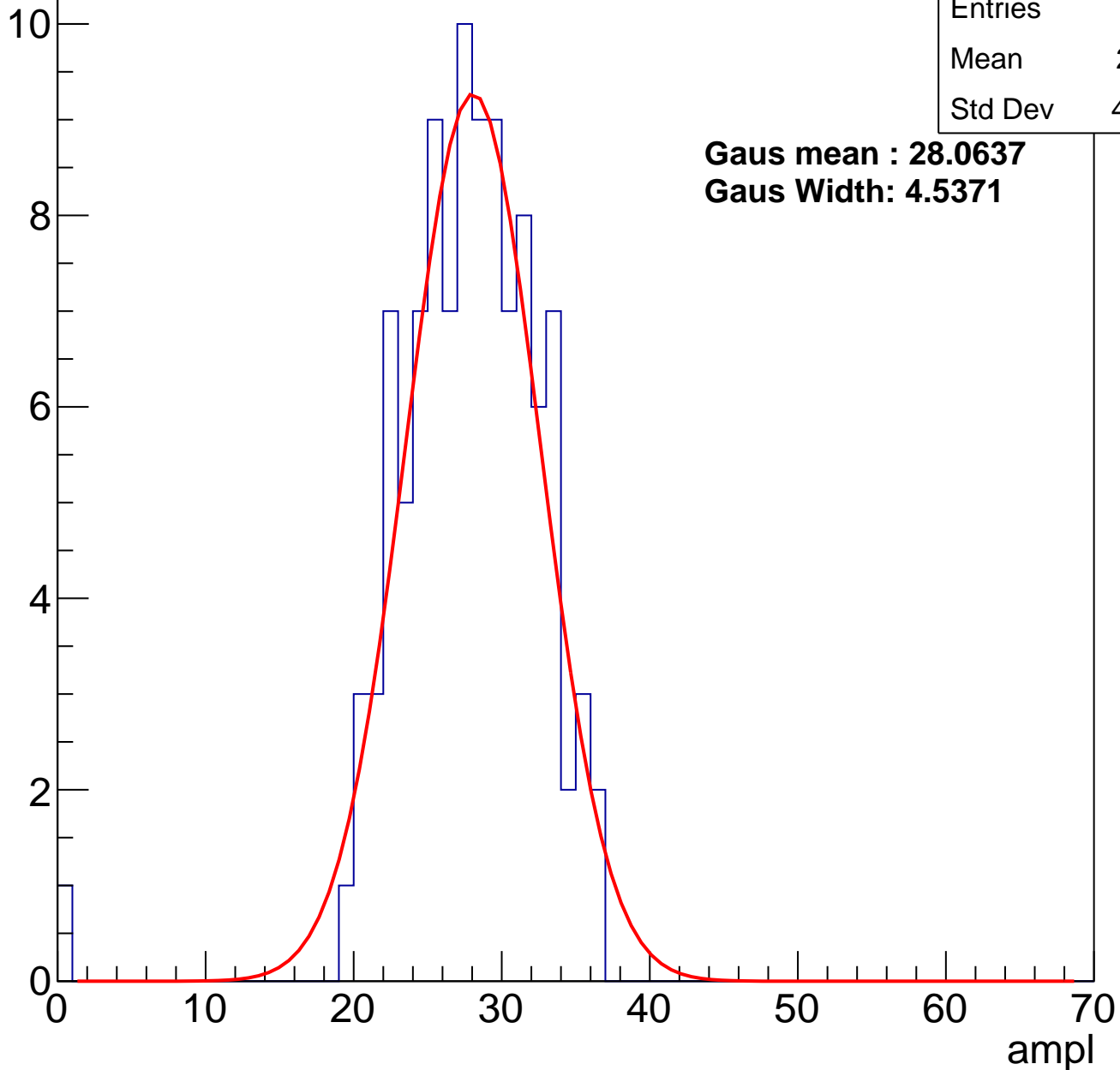
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	106
Mean	27.31
Std Dev	4.845

**Gaus mean : 28.0637**

**Gaus Width: 4.5371**

Entry



# B1L102S, U8-ch114, adc1

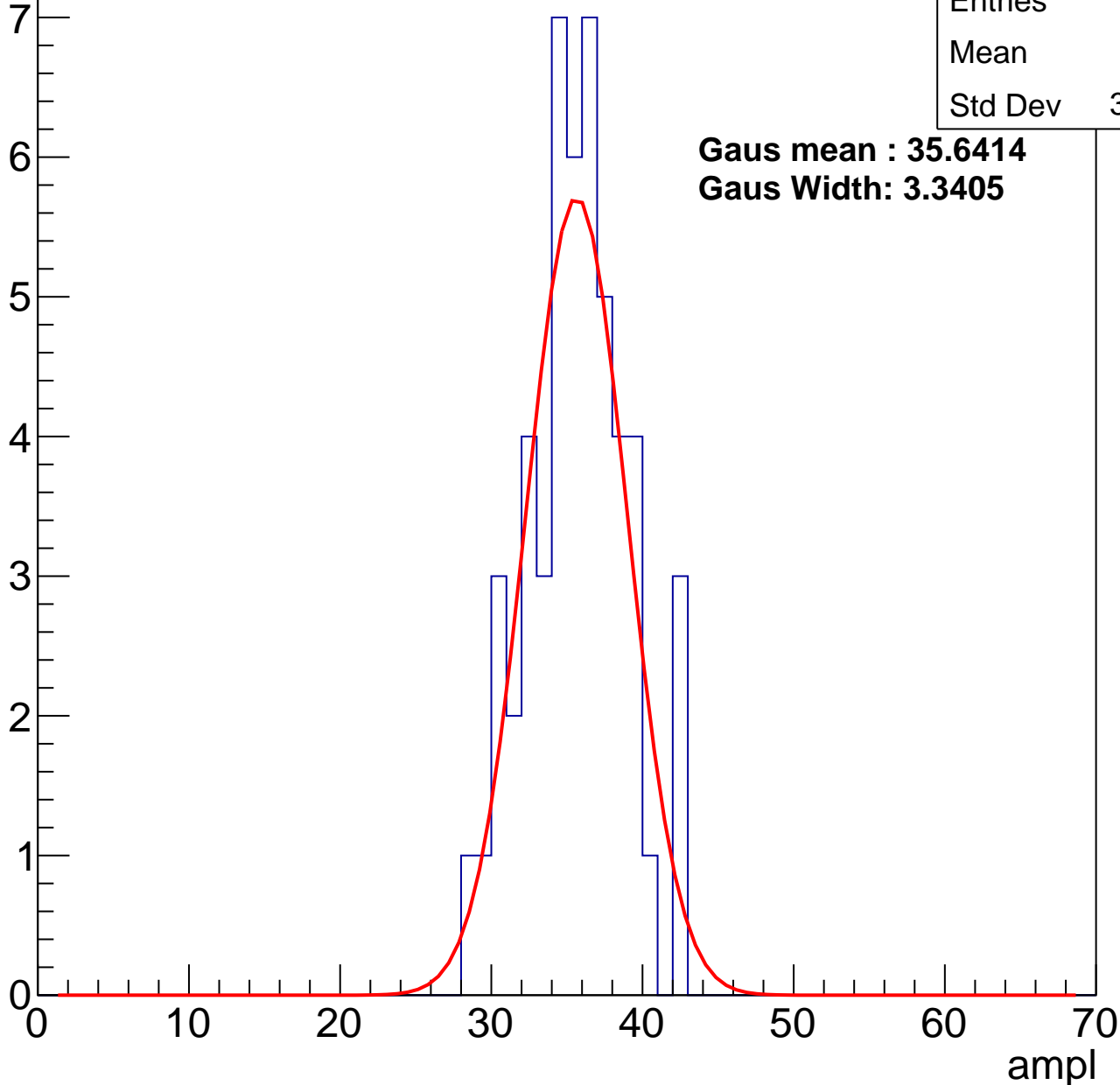
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	35.2
Std Dev	3.266

**Gaus mean : 35.6414**

**Gaus Width: 3.3405**



# B1L102S, U8-ch114, adc2

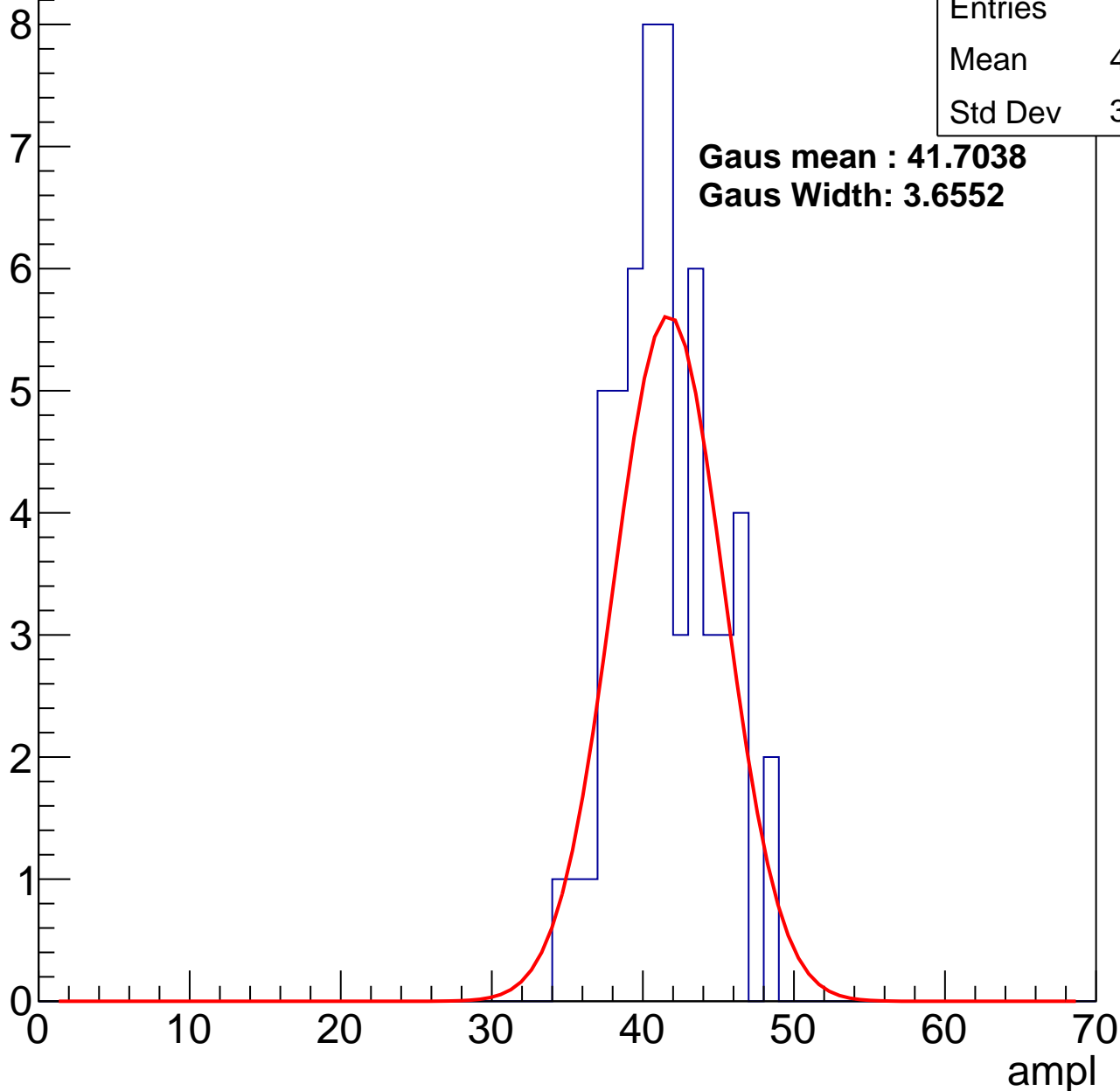
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	40.95
Std Dev	3.182

**Gaus mean : 41.7038**

**Gaus Width: 3.6552**

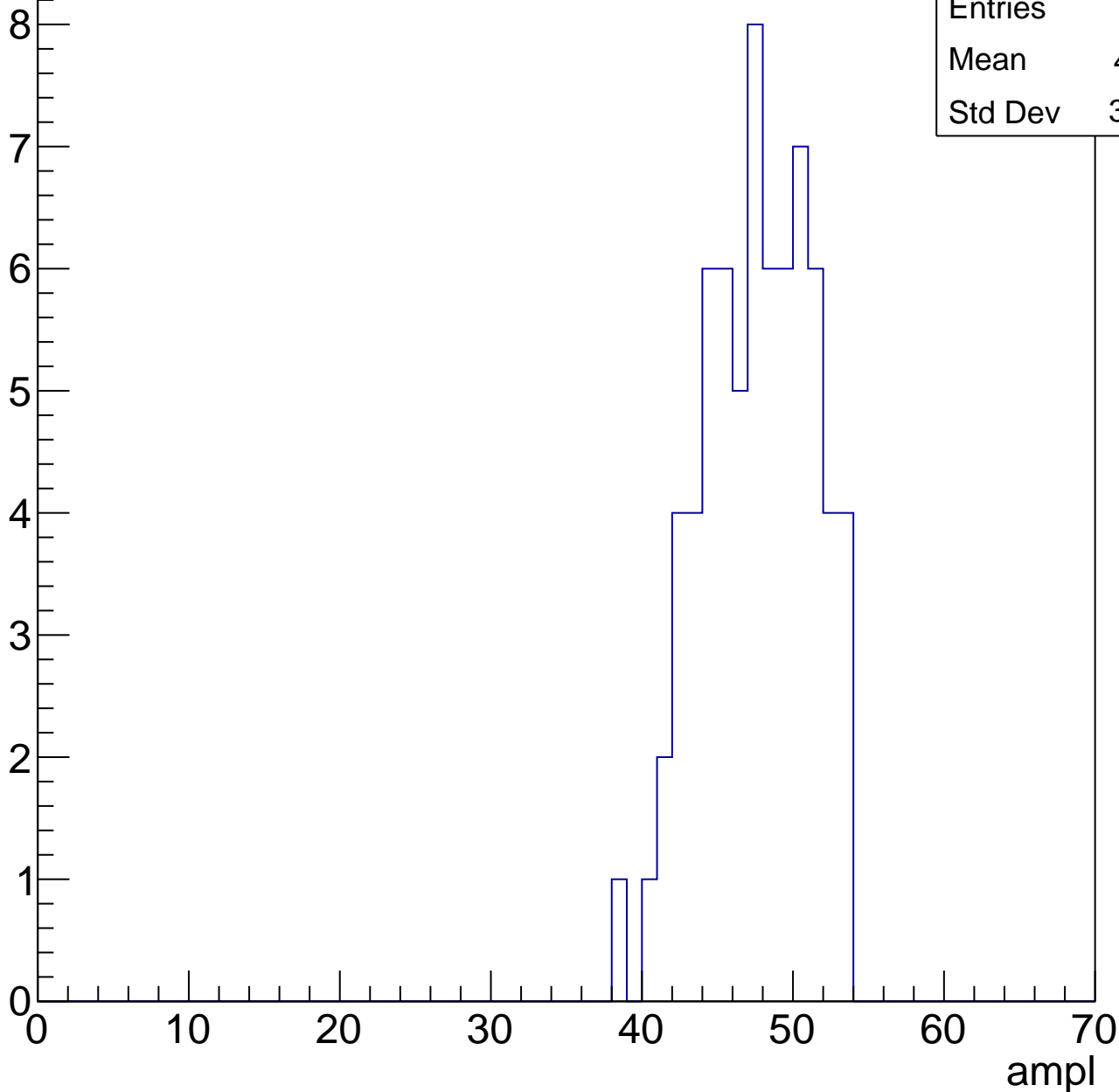


# B1L102S, U8-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	47.11
Std Dev	3.548

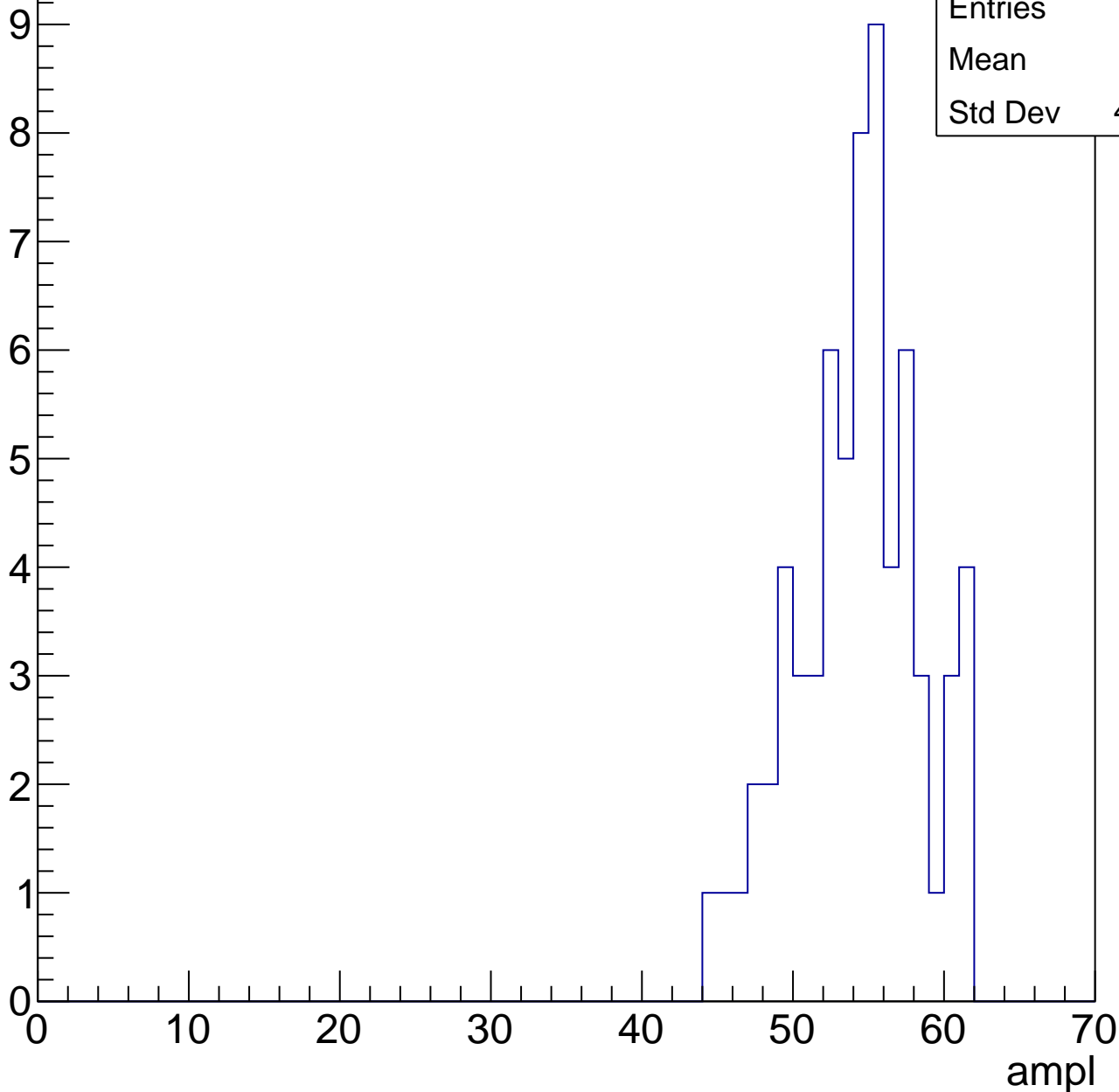


# B1L102S, U8-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	53.8
Std Dev	4.031

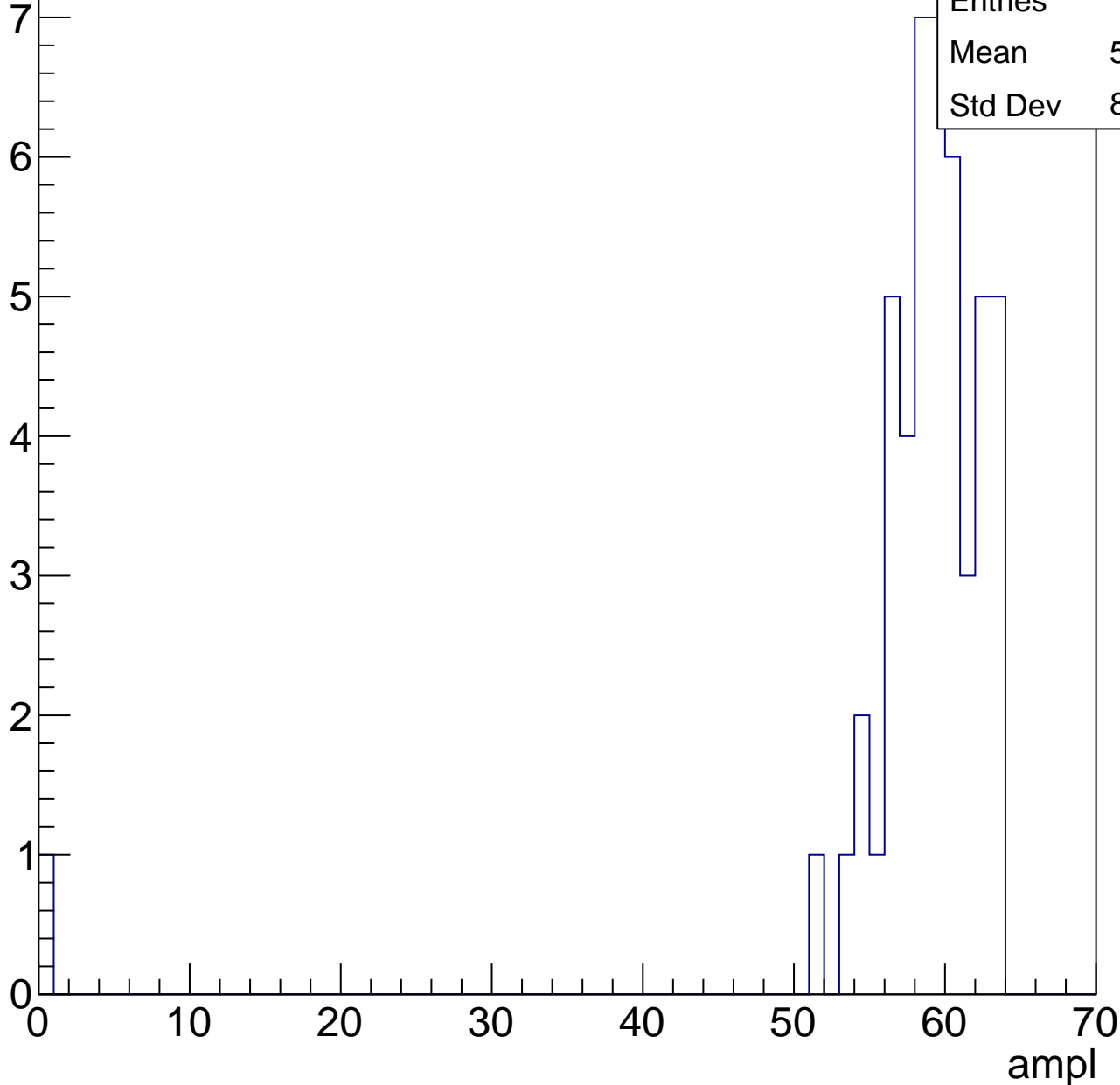


# B1L102S, U8-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	57.54
Std Dev	8.846

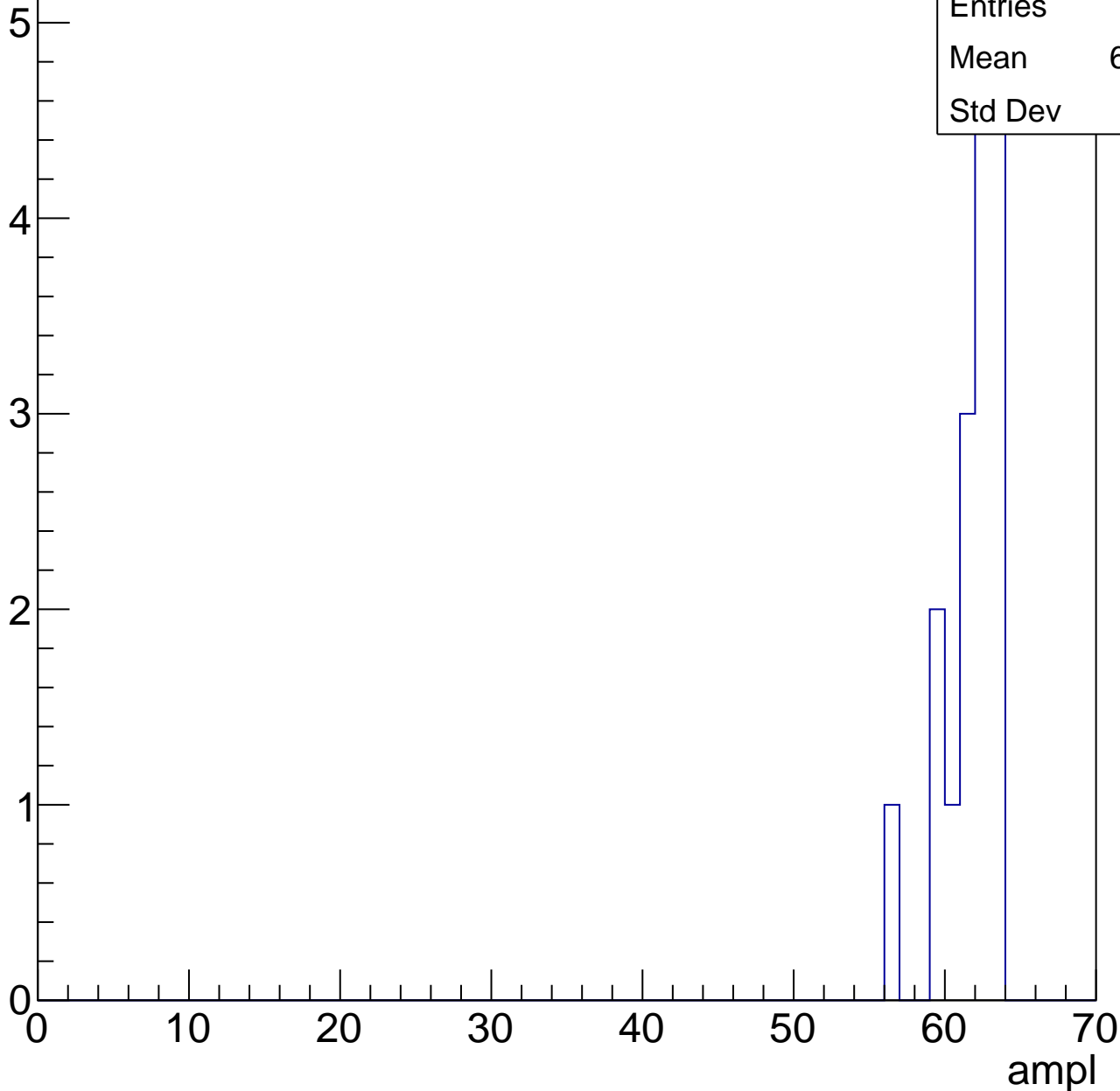


# B1L102S, U8-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	17
Mean	61.29
Std Dev	1.84





# B1L102S, U8-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch115, adc0

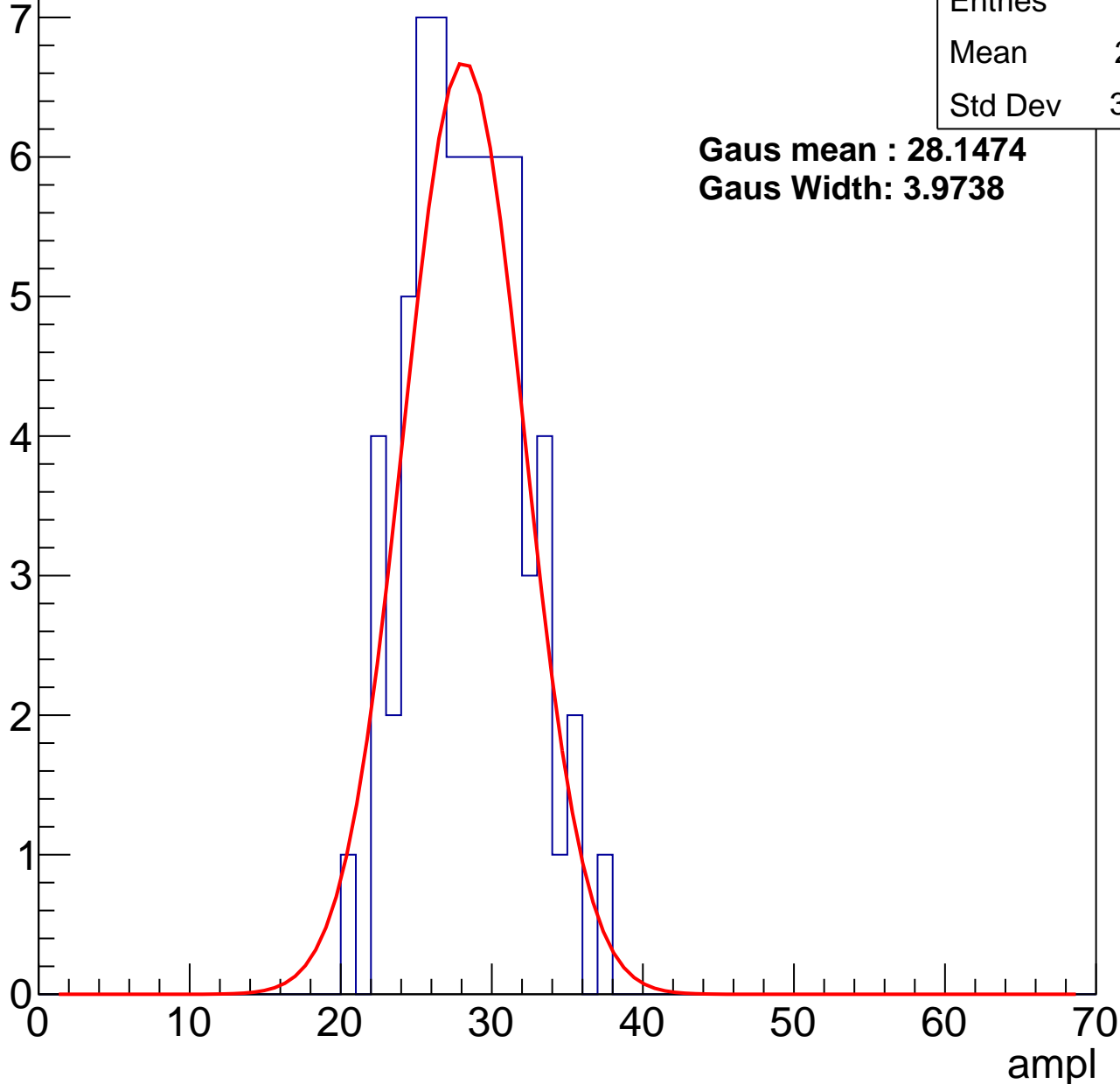
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	27.91
Std Dev	3.627

**Gaus mean : 28.1474**

**Gaus Width: 3.9738**



# B1L102S, U8-ch115, adc1

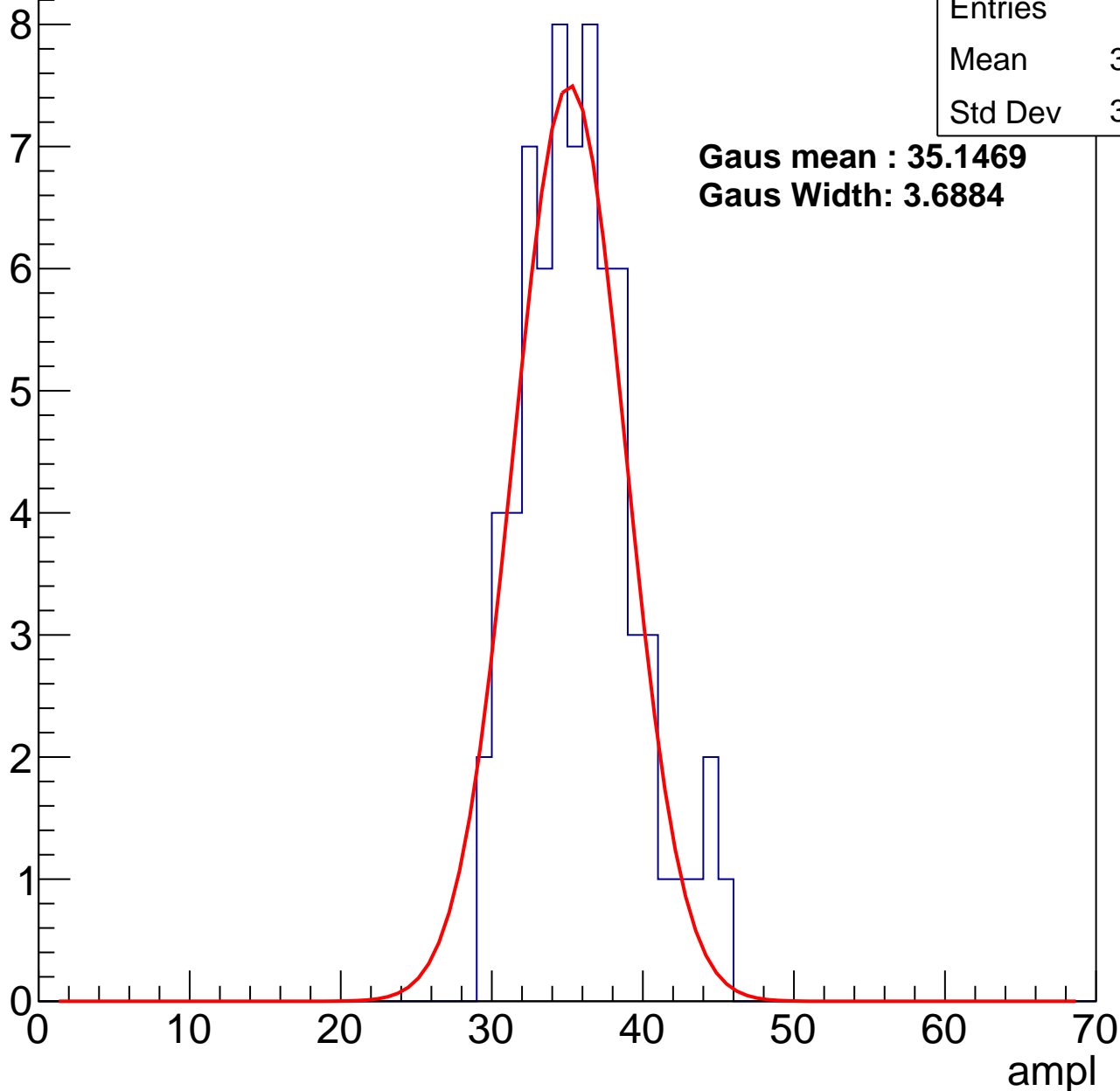
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	35.36
Std Dev	3.669

**Gaus mean : 35.1469**

**Gaus Width: 3.6884**



# B1L102S, U8-ch115, adc2

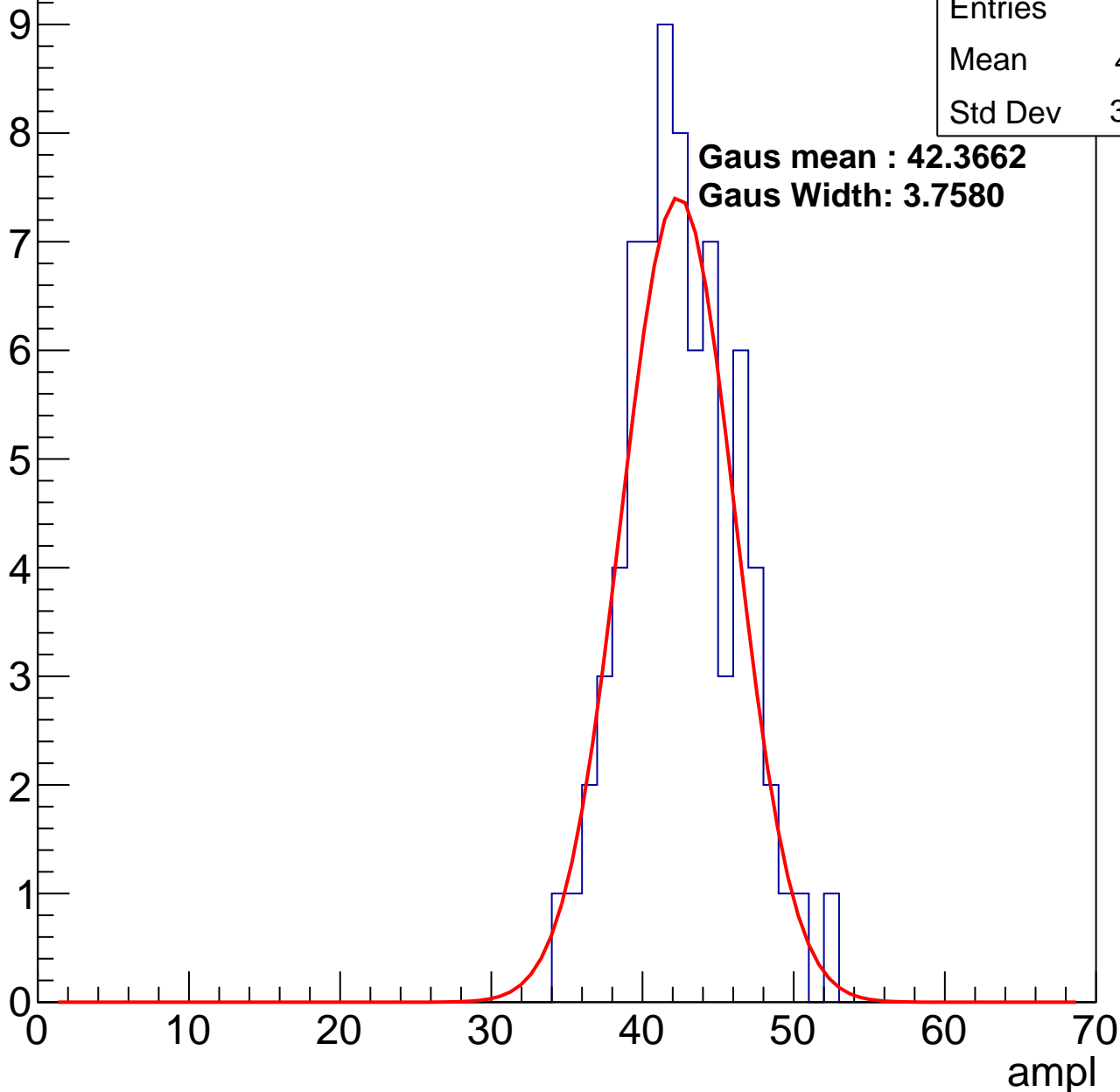
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	42.11
Std Dev	3.636

**Gaus mean : 42.3662**

**Gaus Width: 3.7580**

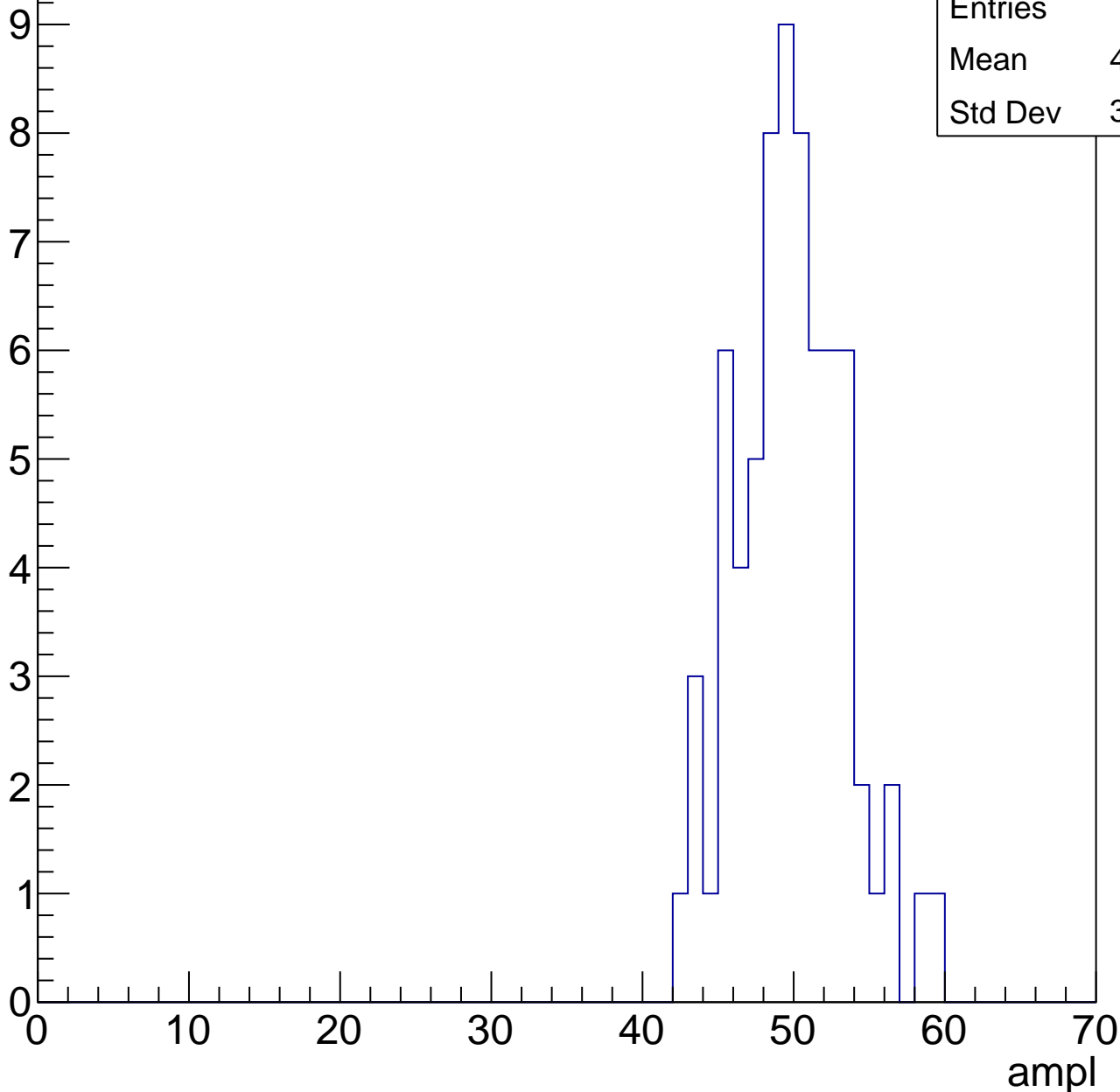


# B1L102S, U8-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	49.39
Std Dev	3.543

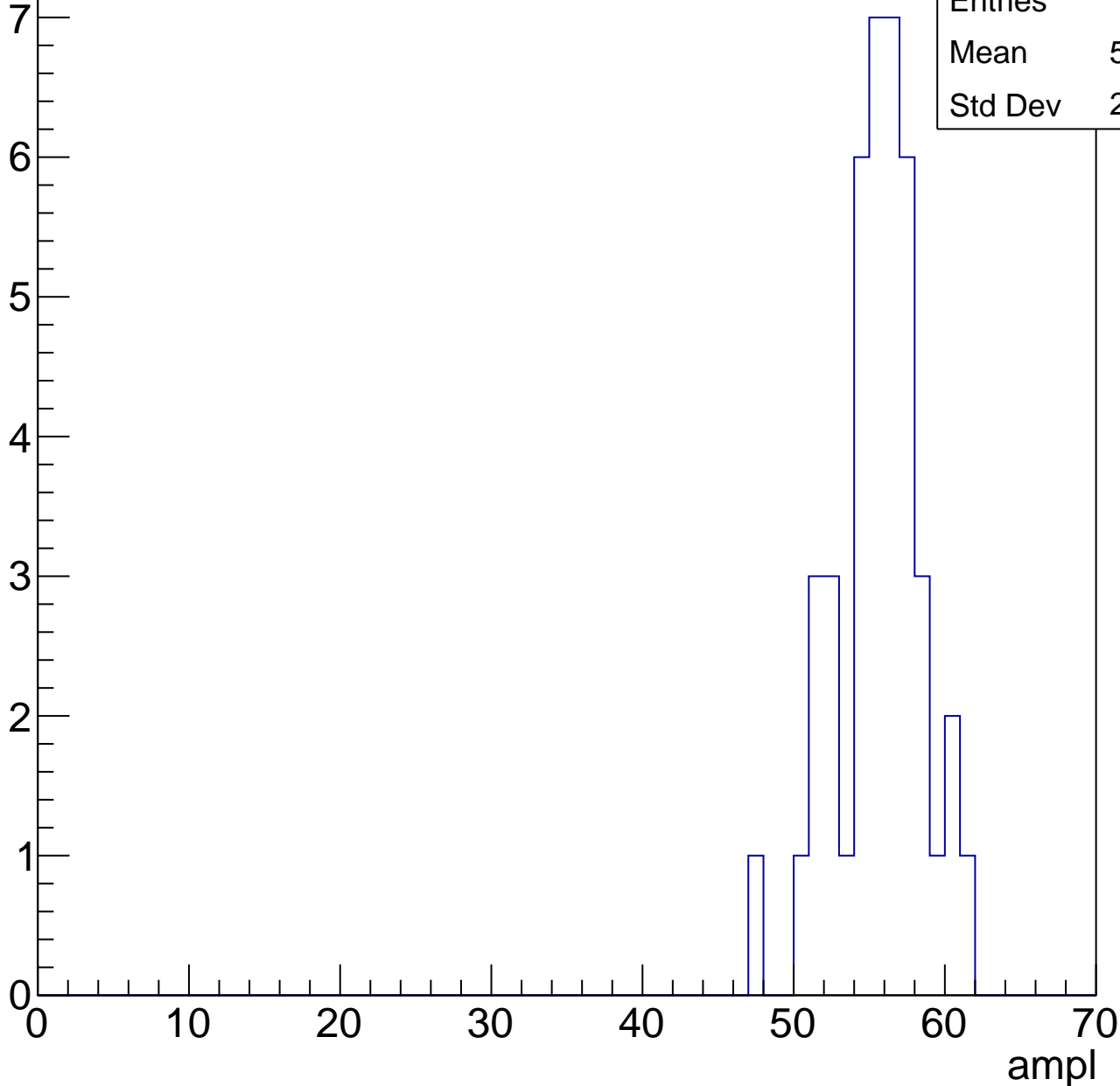


# B1L102S, U8-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	42
Mean	55.14
Std Dev	2.816

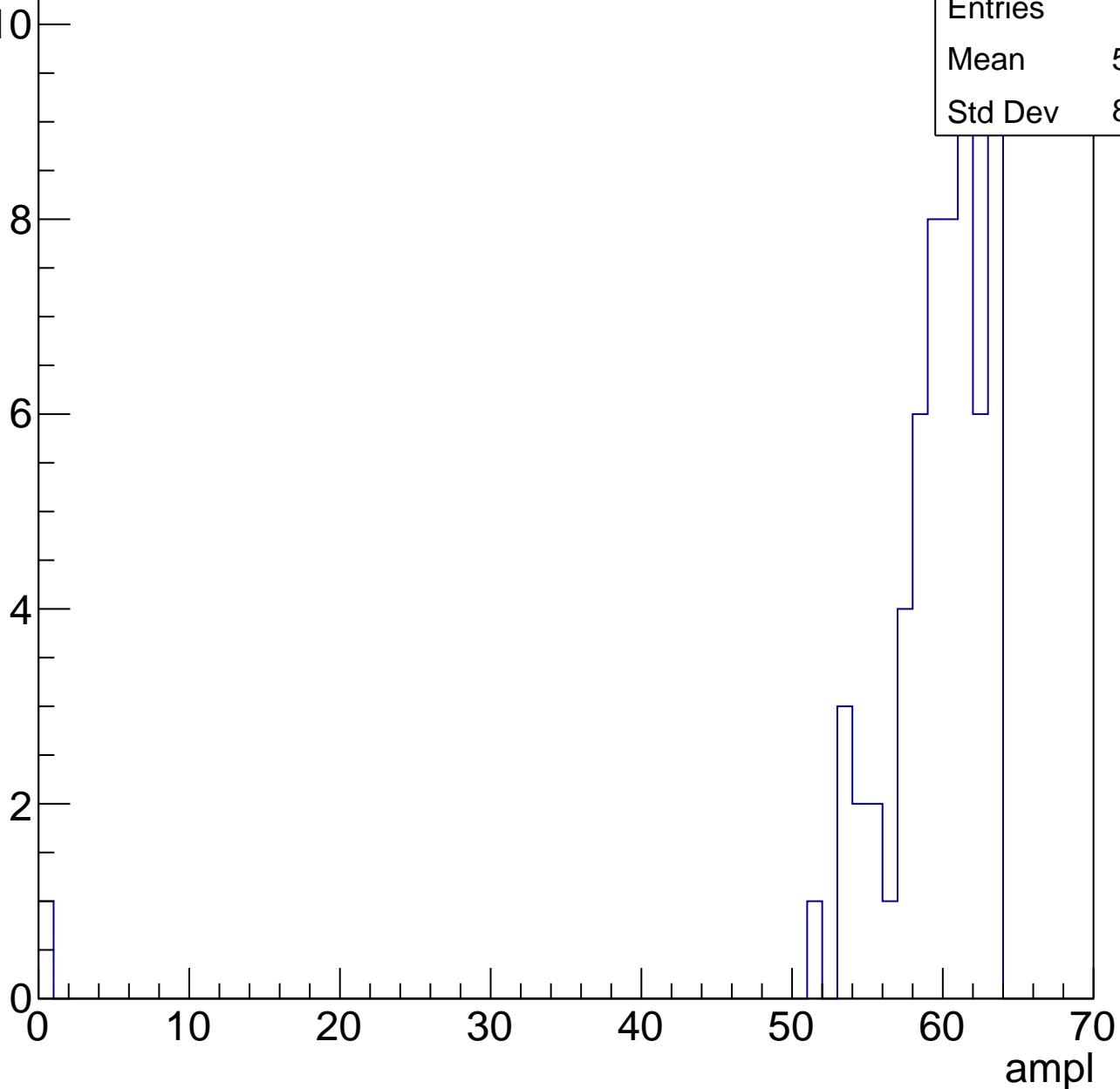


# B1L102S, U8-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

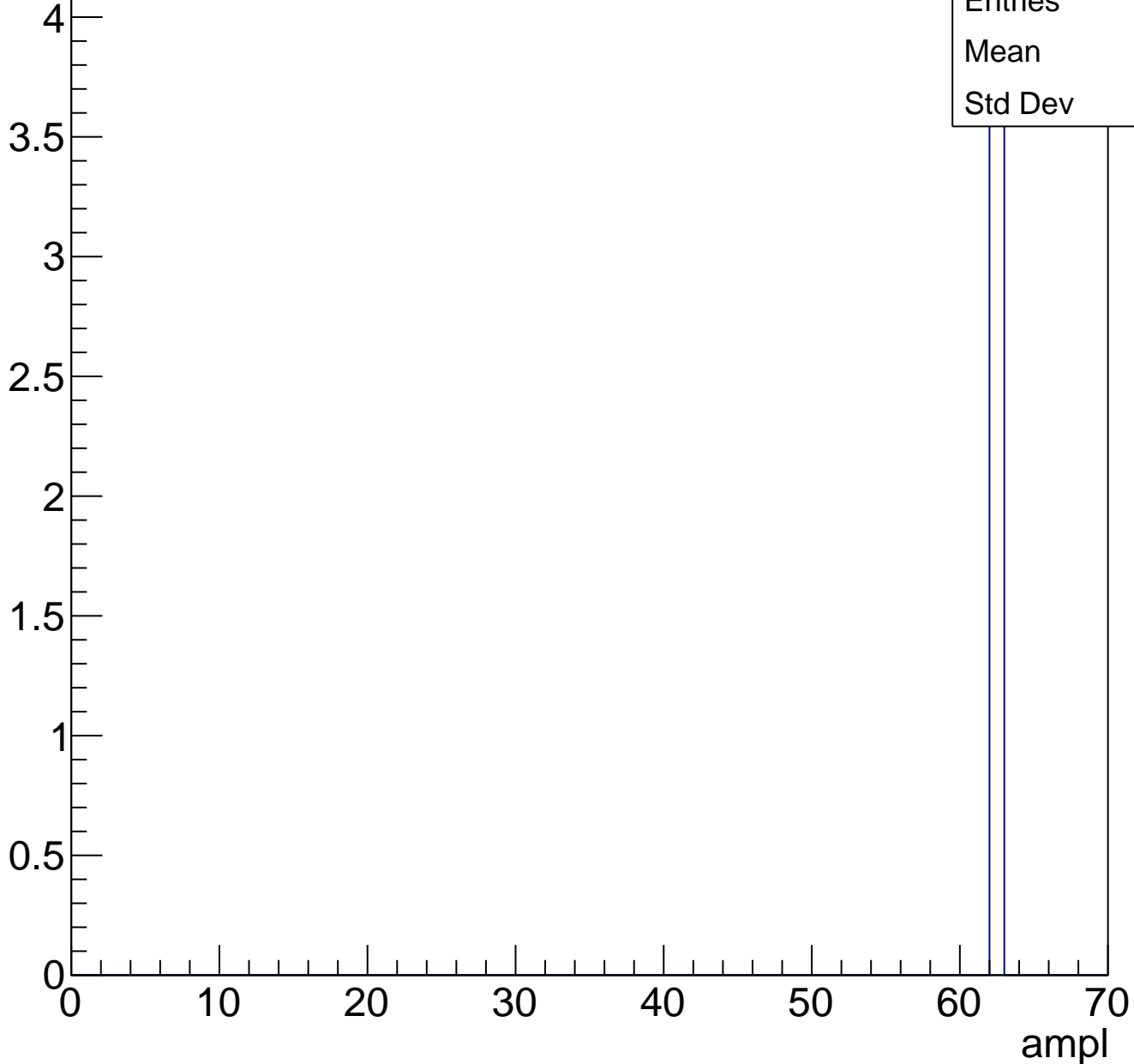
Entries	61
Mean	58.41
Std Dev	8.101



# B1L102S, U8-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch115, adc7

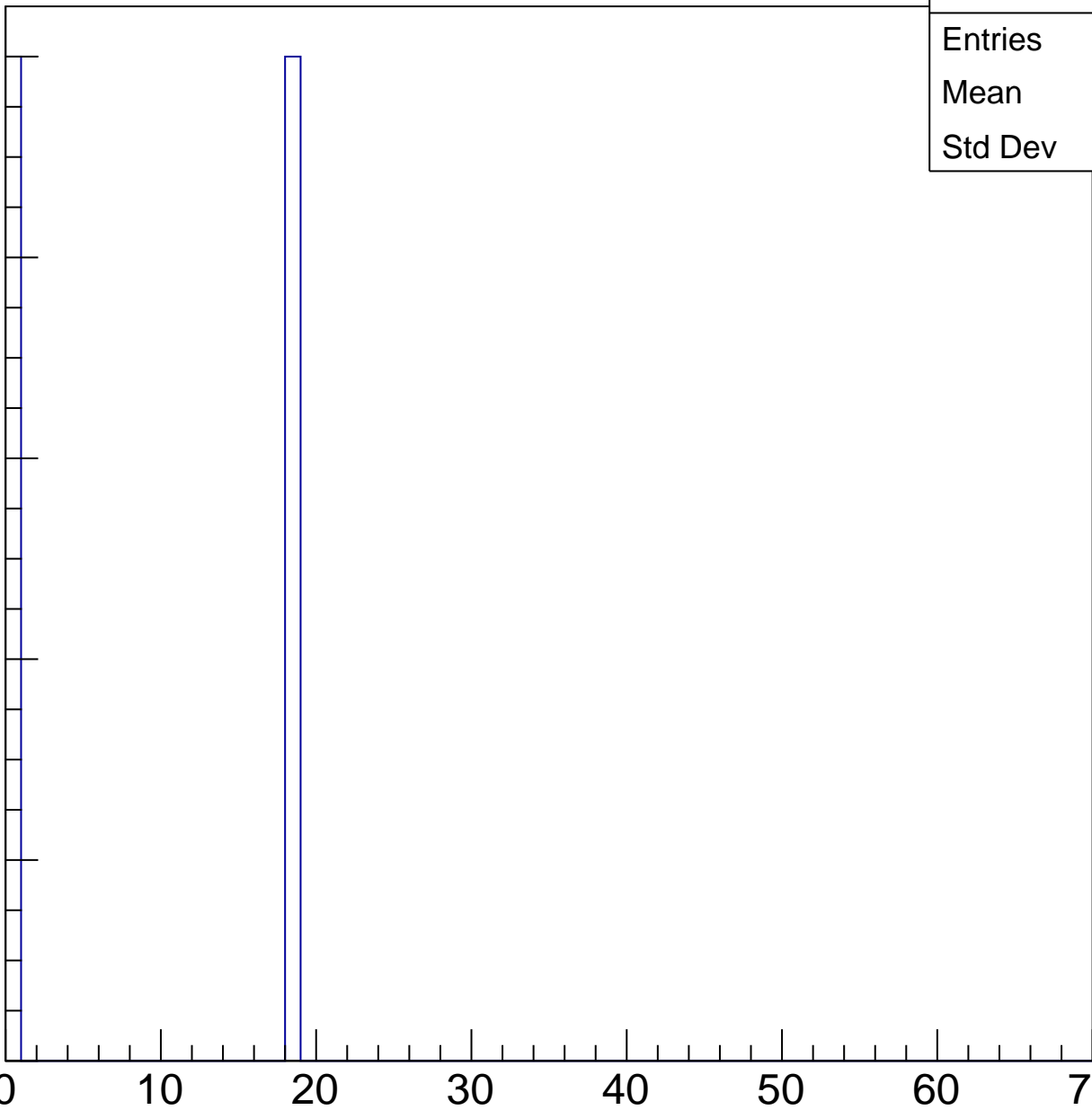
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	9
Std Dev	9

ampl



# B1L102S, U8-ch116, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	84
Mean	27.71
Std Dev	3.524

**Gaus mean : 28.2931**

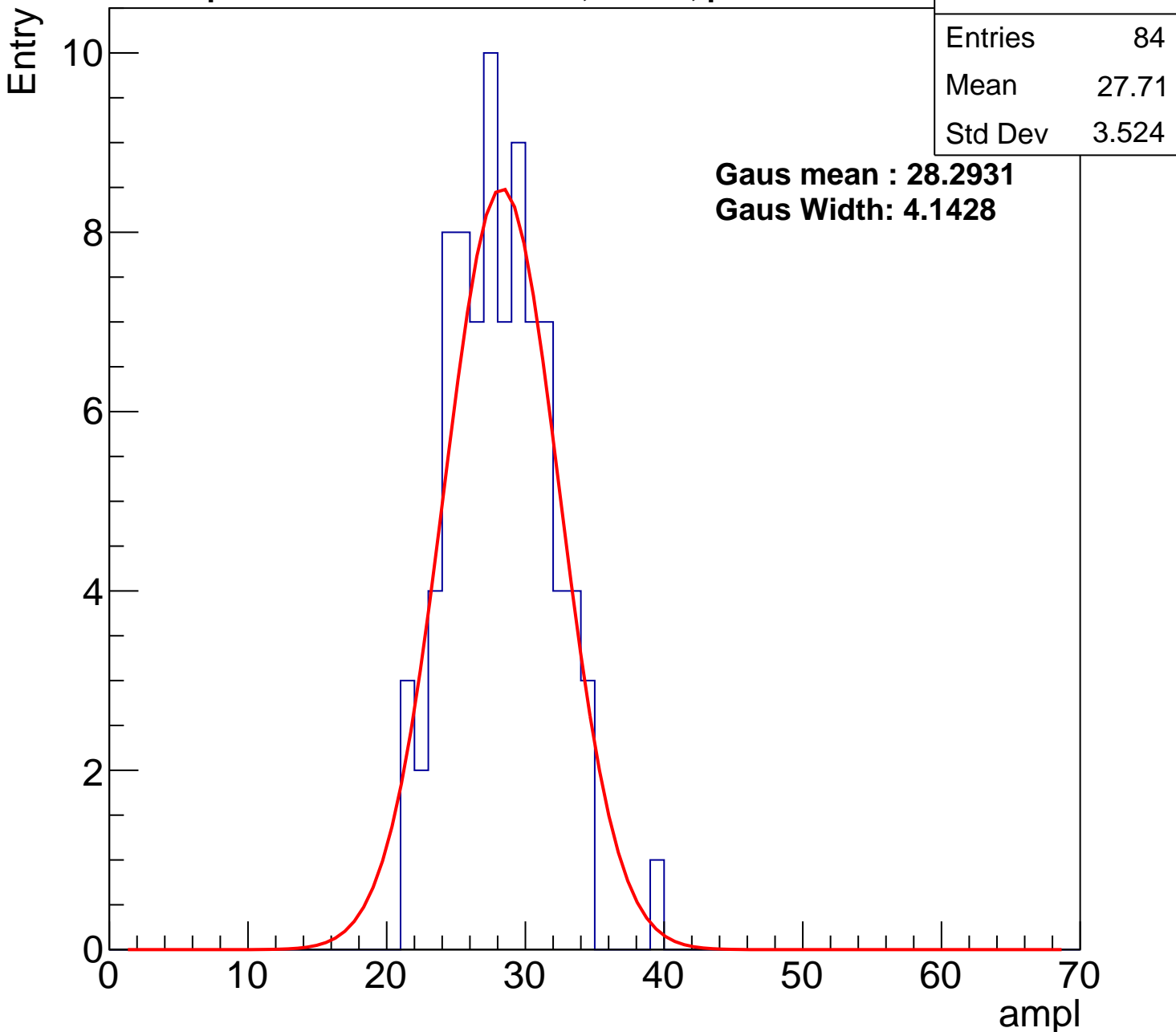
**Gaus Width: 4.1428**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U8-ch116, adc1

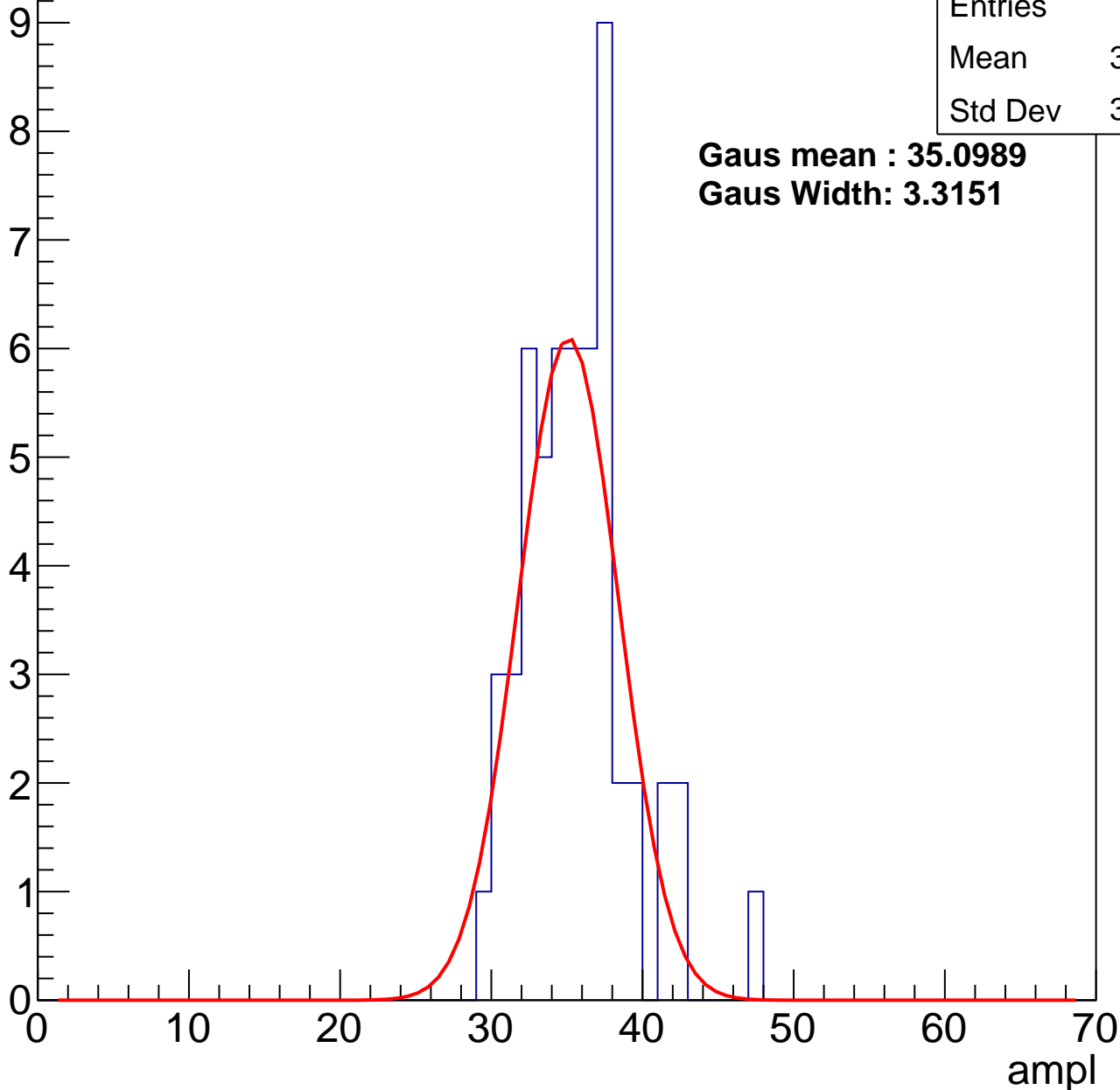
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	35.17
Std Dev	3.452

**Gaus mean : 35.0989**

**Gaus Width: 3.3151**



# B1L102S, U8-ch116, adc2

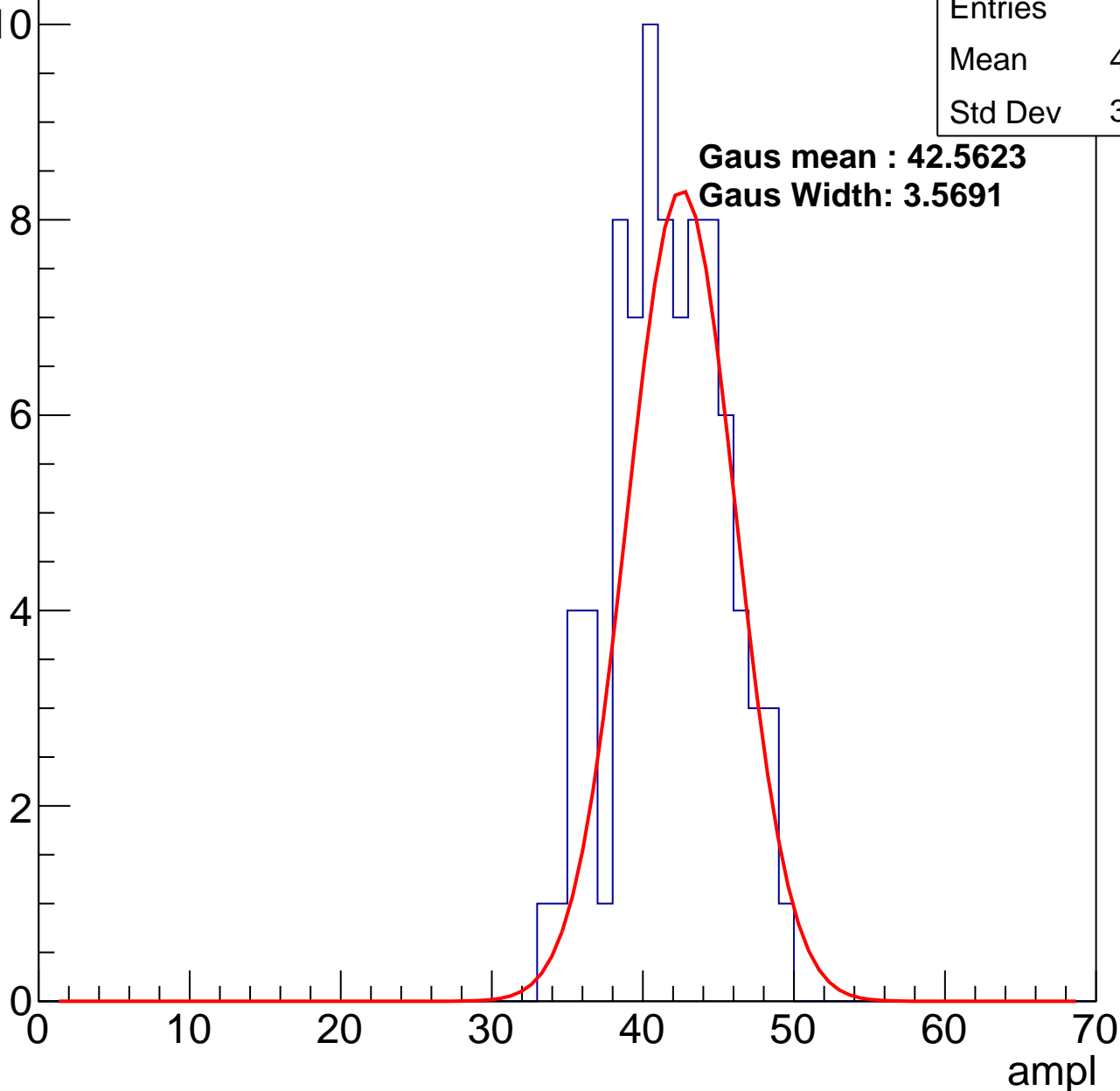
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	41.32
Std Dev	3.619

**Gaus mean : 42.5623**

**Gaus Width: 3.5691**

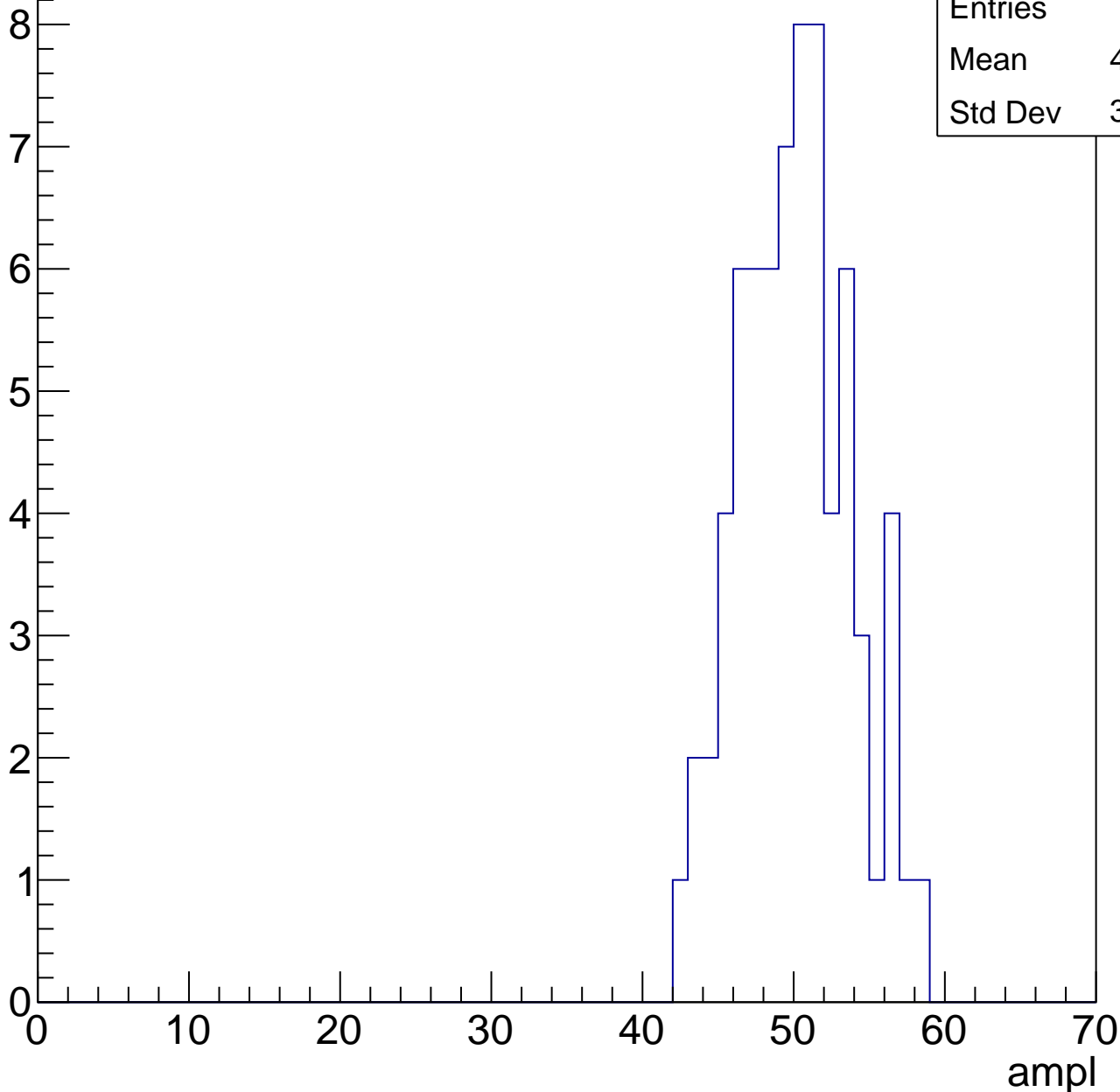


# B1L102S, U8-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	49.64
Std Dev	3.614

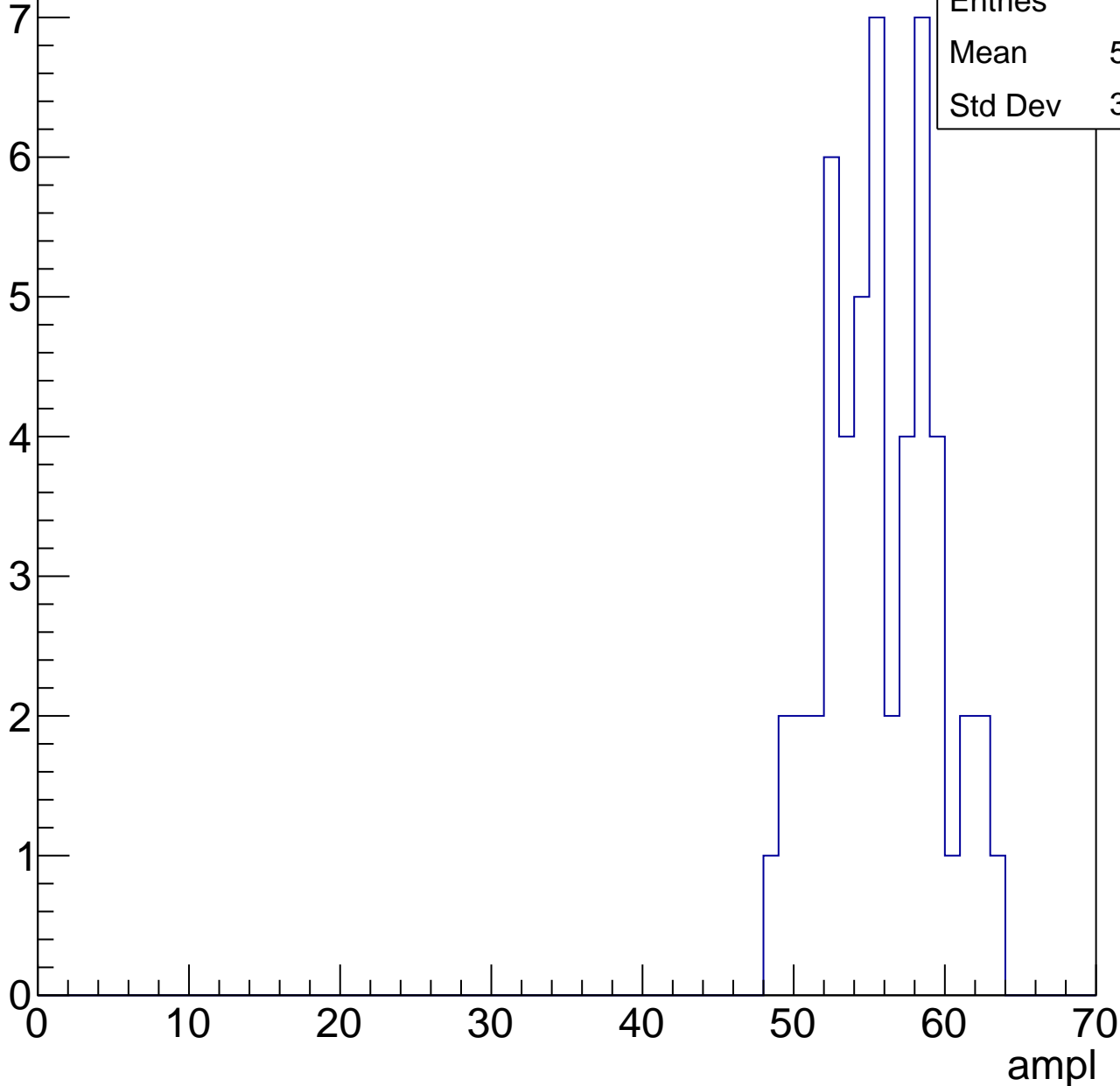


# B1L102S, U8-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	55.35
Std Dev	3.605



# B1L102S, U8-ch116, adc5

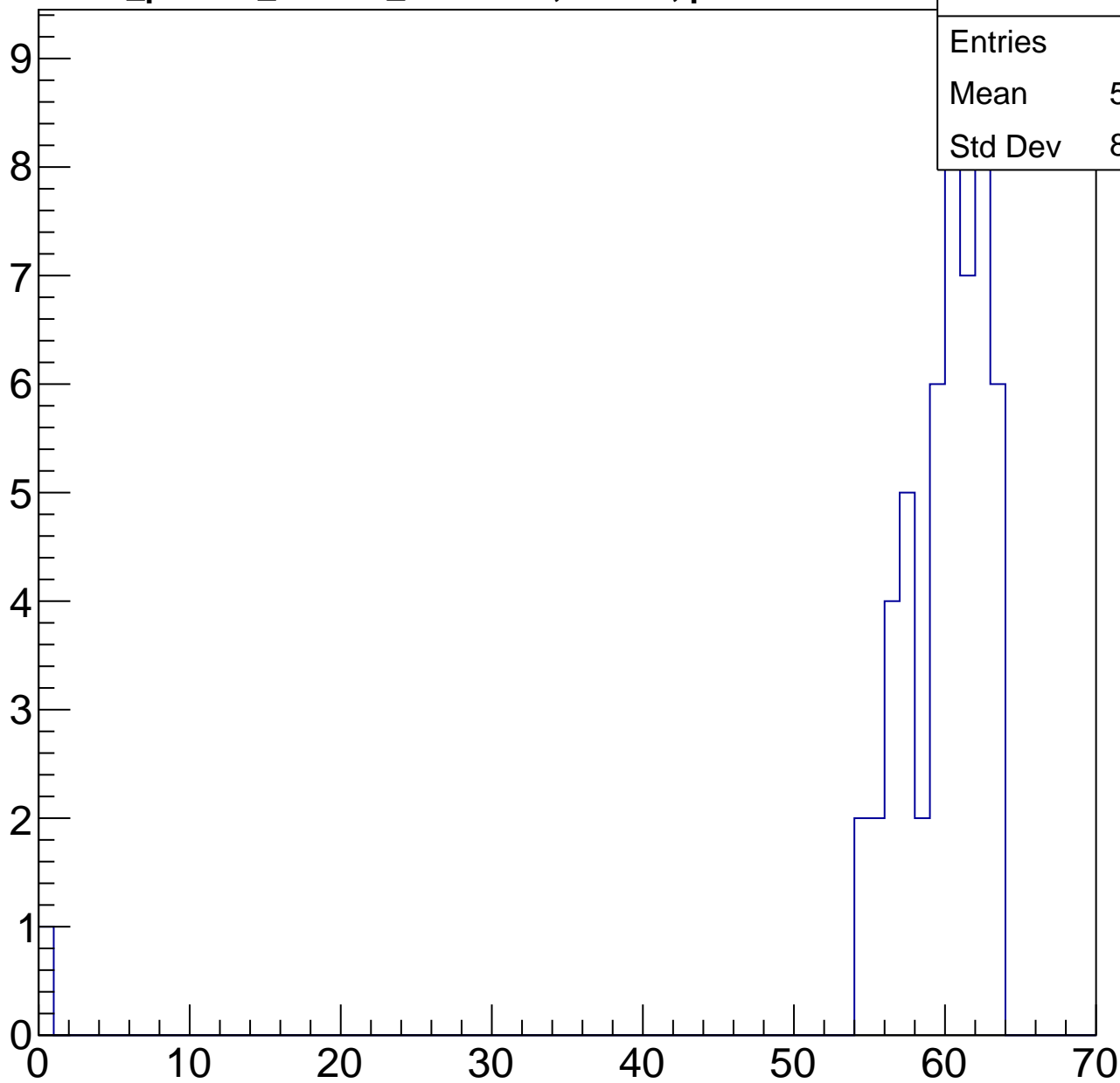
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	52
Mean	58.42
Std Dev	8.558

ampl



# B1L102S, U8-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U8-ch117, adc0

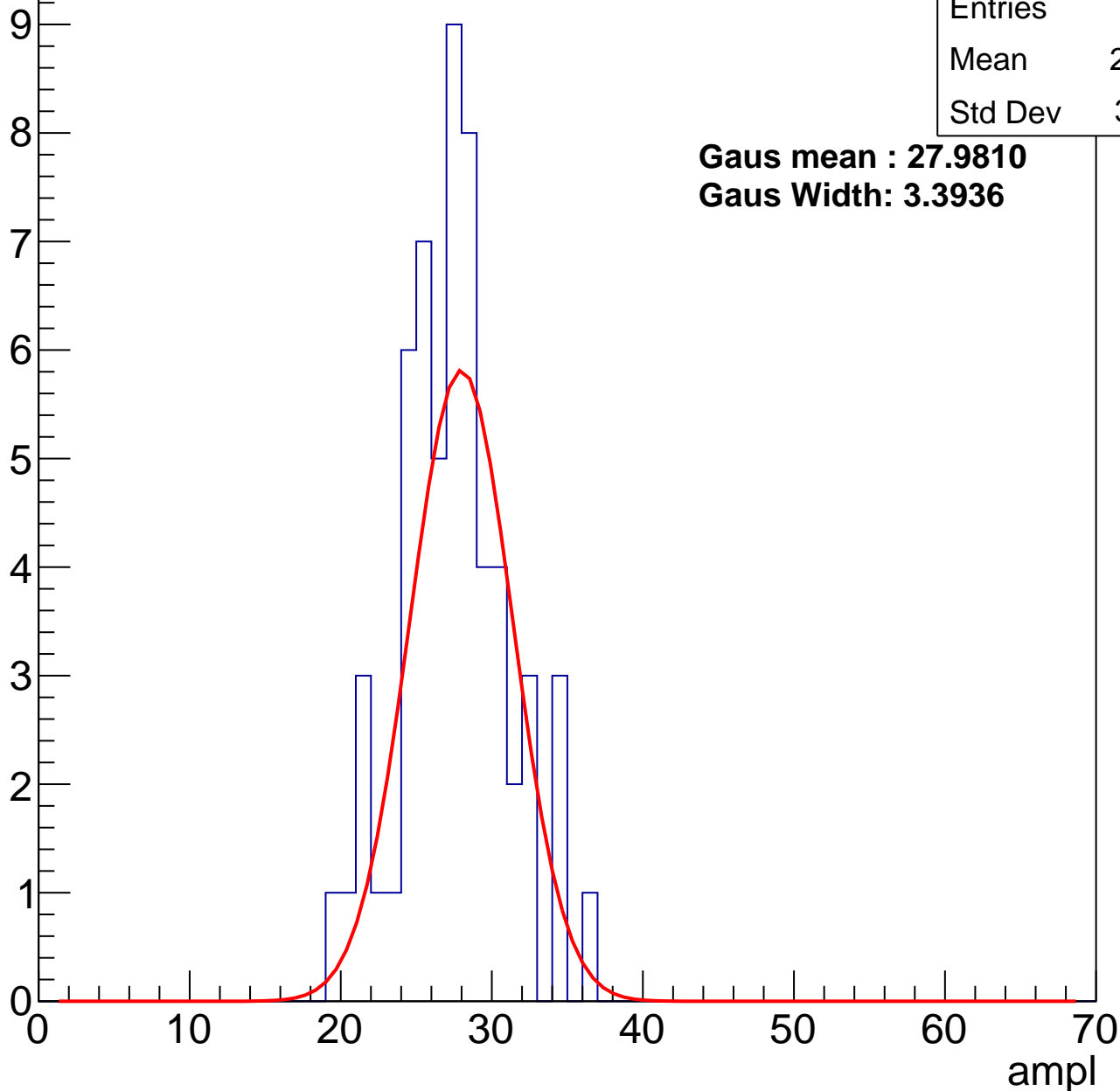
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	27.03
Std Dev	3.551

**Gaus mean : 27.9810**

**Gaus Width: 3.3936**



# B1L102S, U8-ch117, adc1

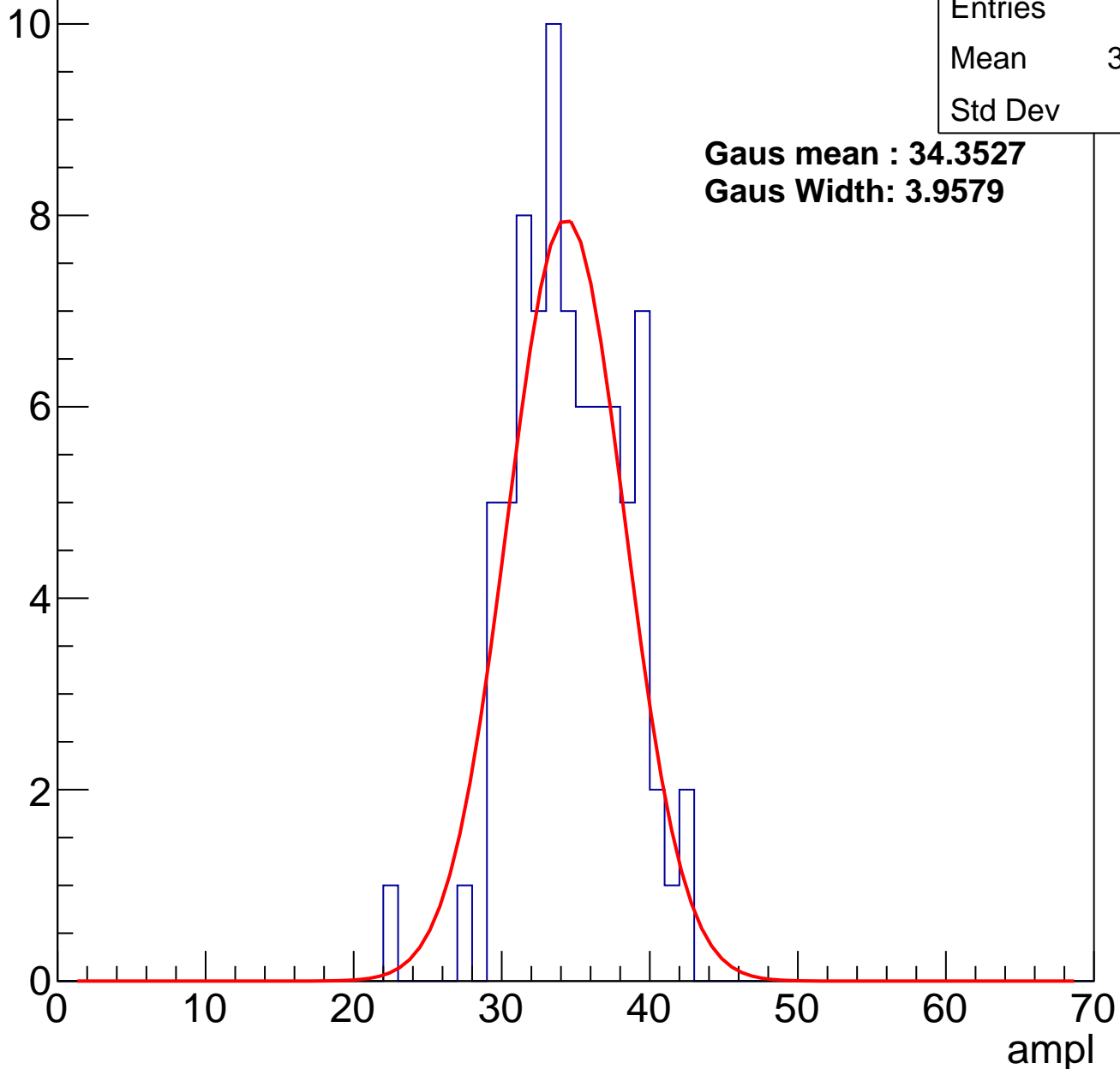
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	79
Mean	34.18
Std Dev	3.72

**Gaus mean : 34.3527**

**Gaus Width: 3.9579**

Entry



# B1L102S, U8-ch117, adc2

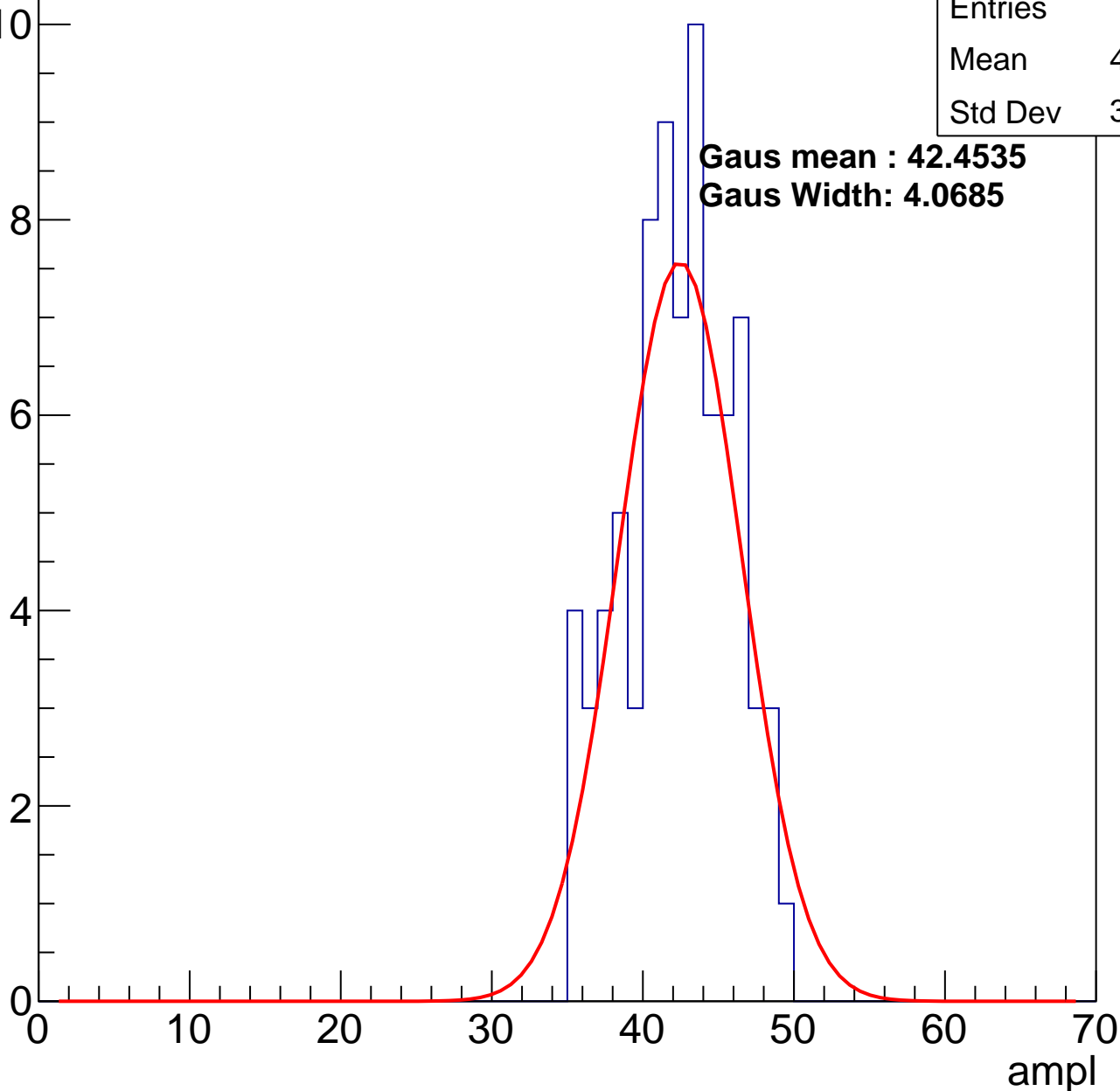
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	41.85
Std Dev	3.526

**Gaus mean : 42.4535**

**Gaus Width: 4.0685**

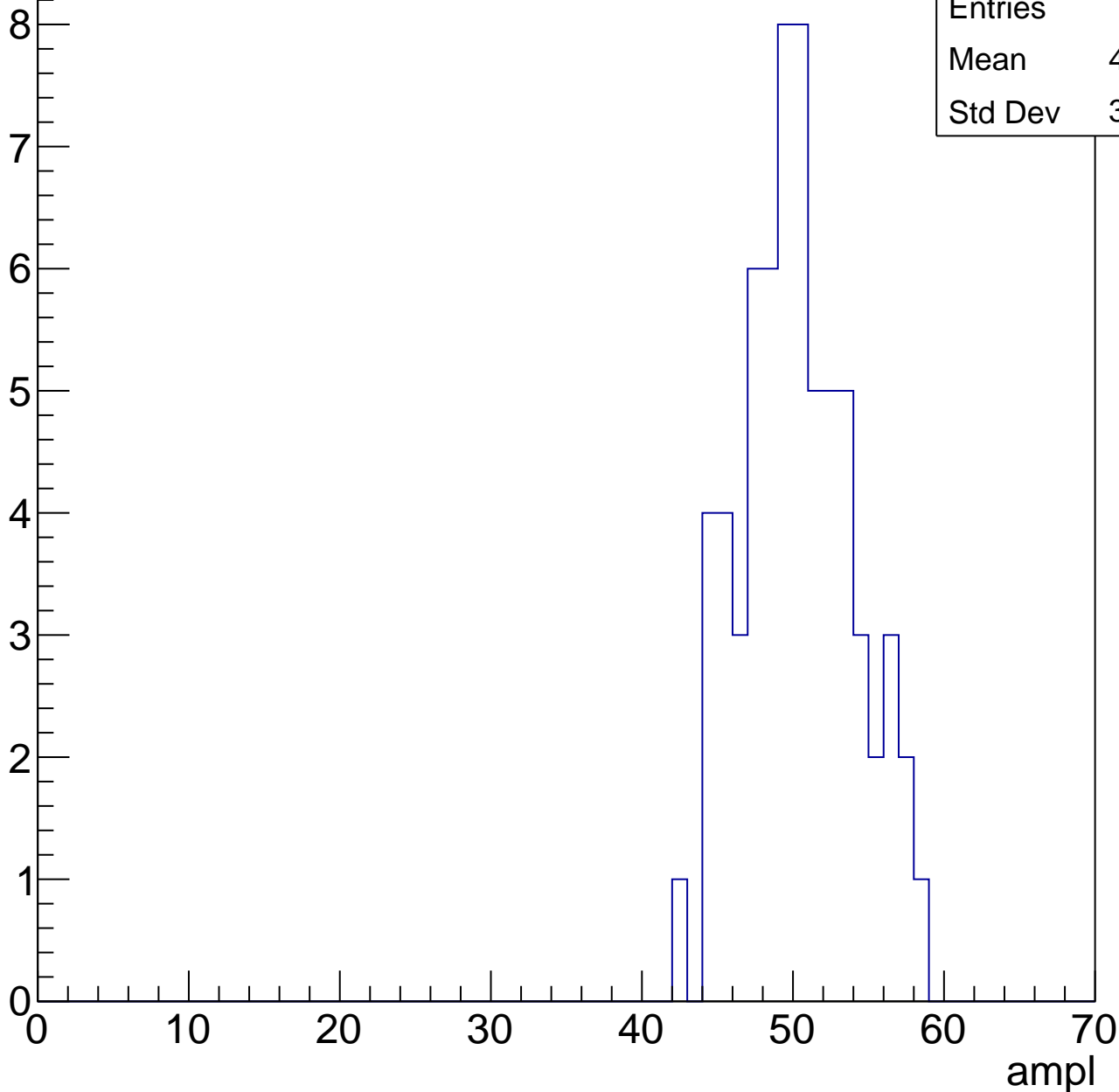


# B1L102S, U8-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	49.85
Std Dev	3.648

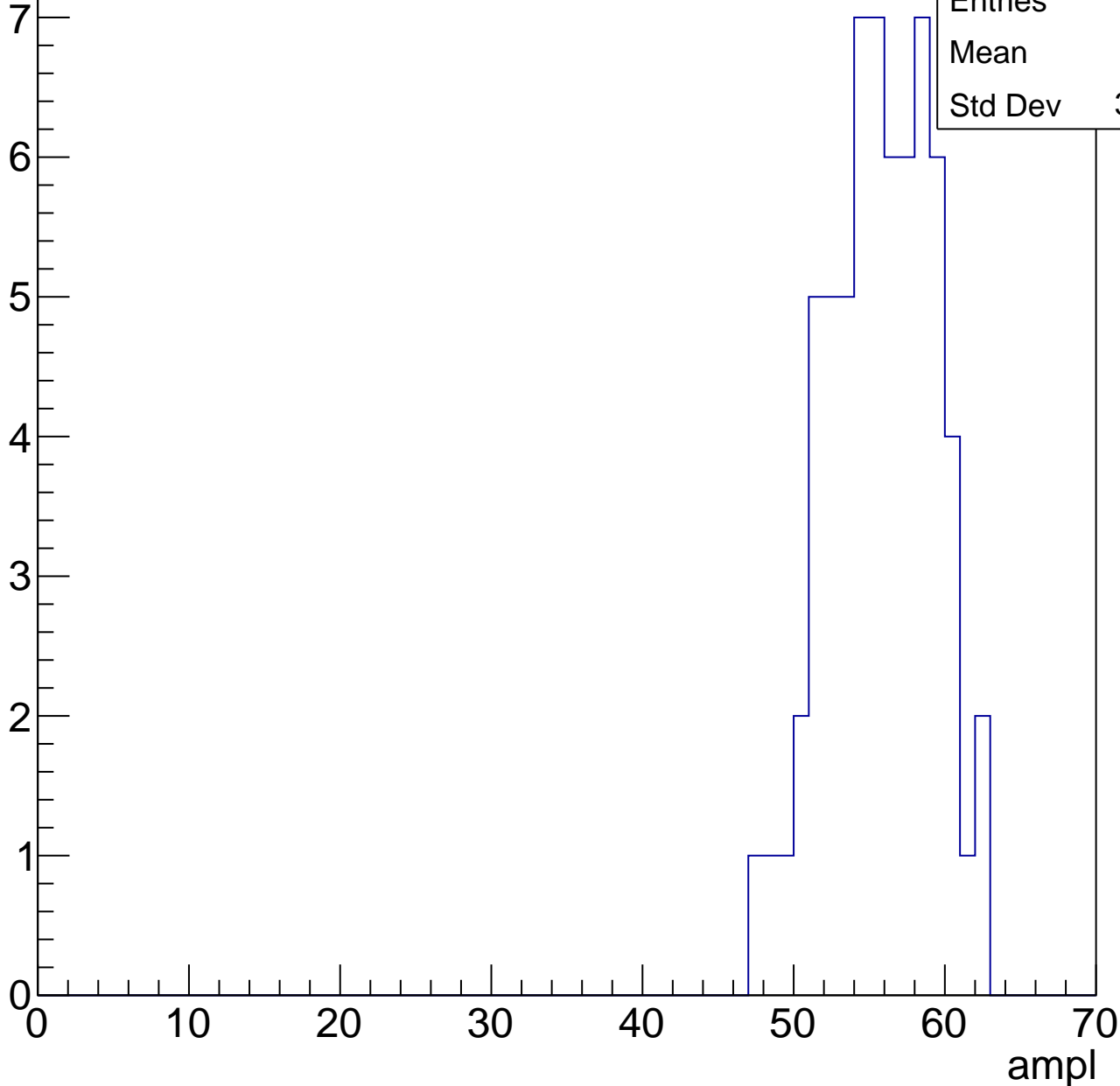


# B1L102S, U8-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	55.3
Std Dev	3.411

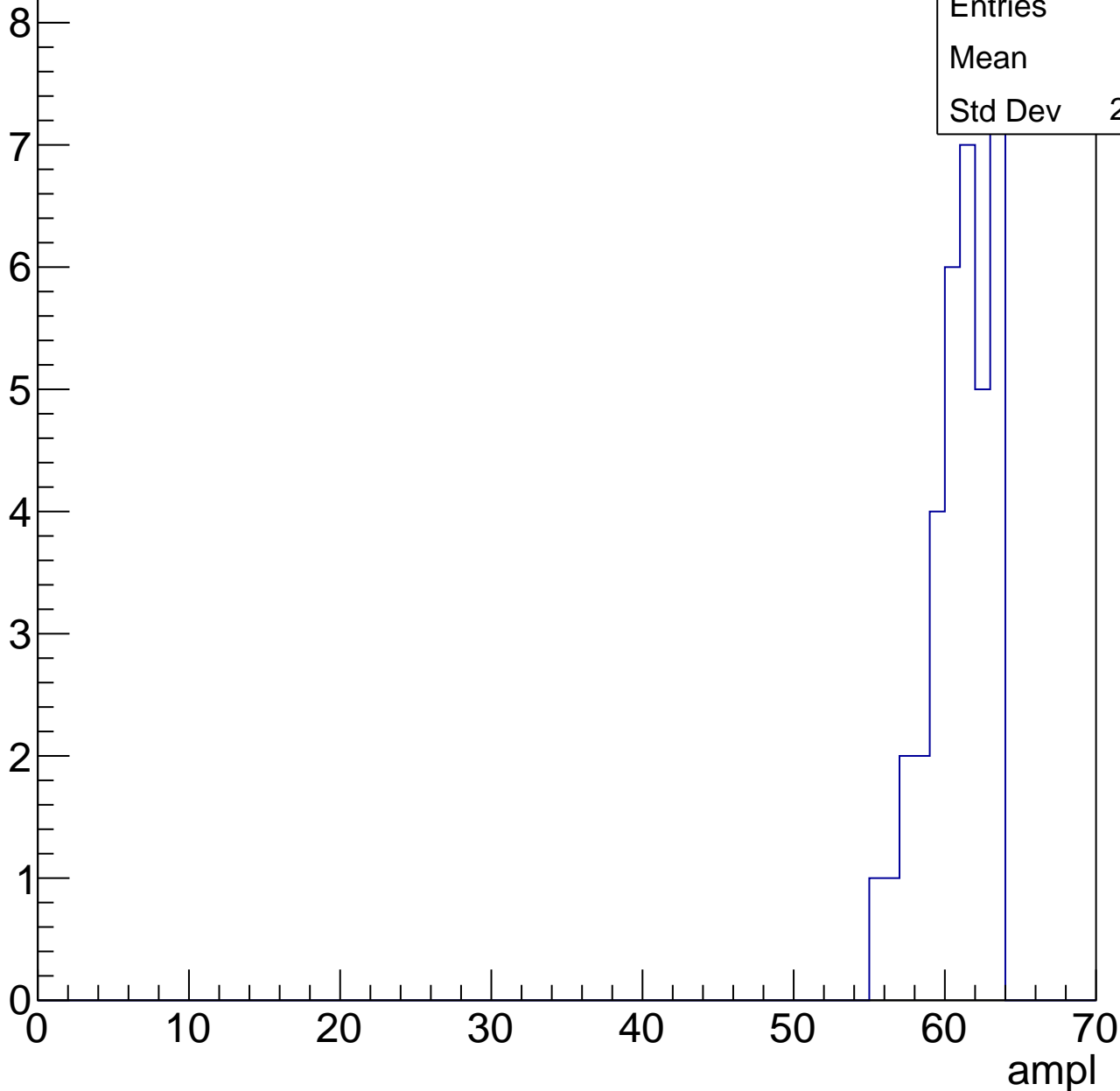


# B1L102S, U8-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

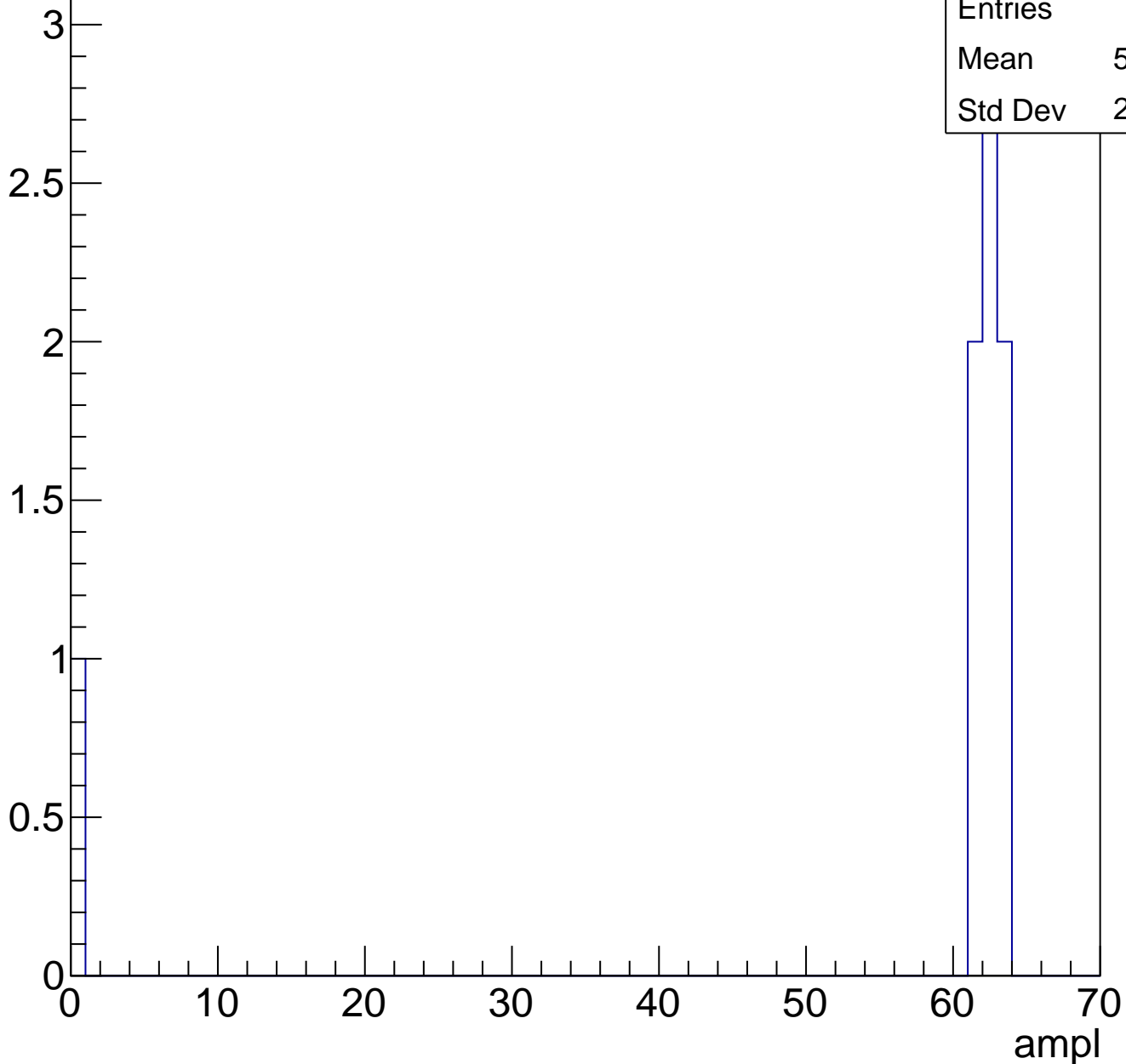
Entries	36
Mean	60.5
Std Dev	2.115



# B1L102S, U8-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch117, adc7

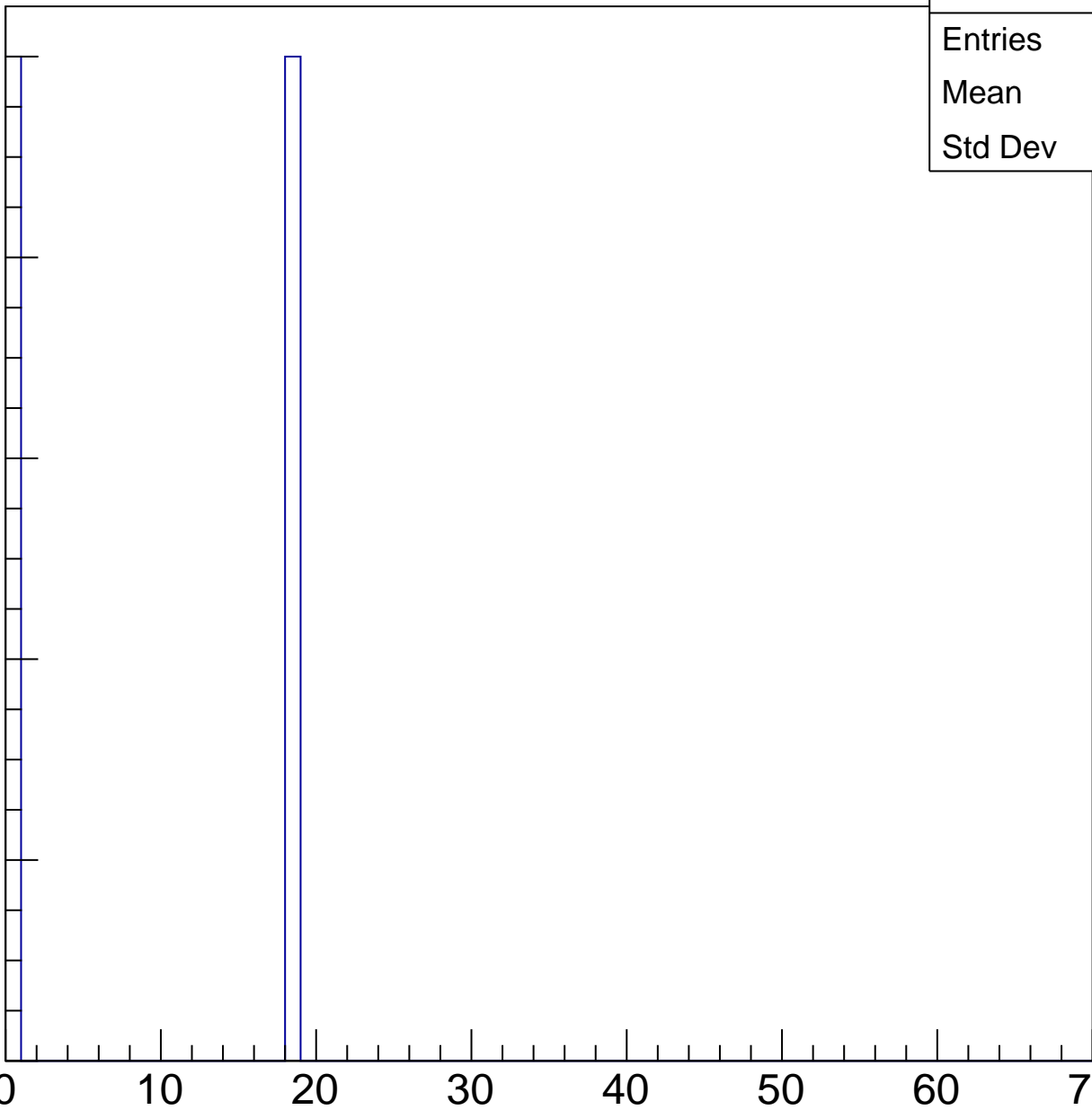
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	9
Std Dev	9

ampl



# B1L102S, U8-ch118, adc0

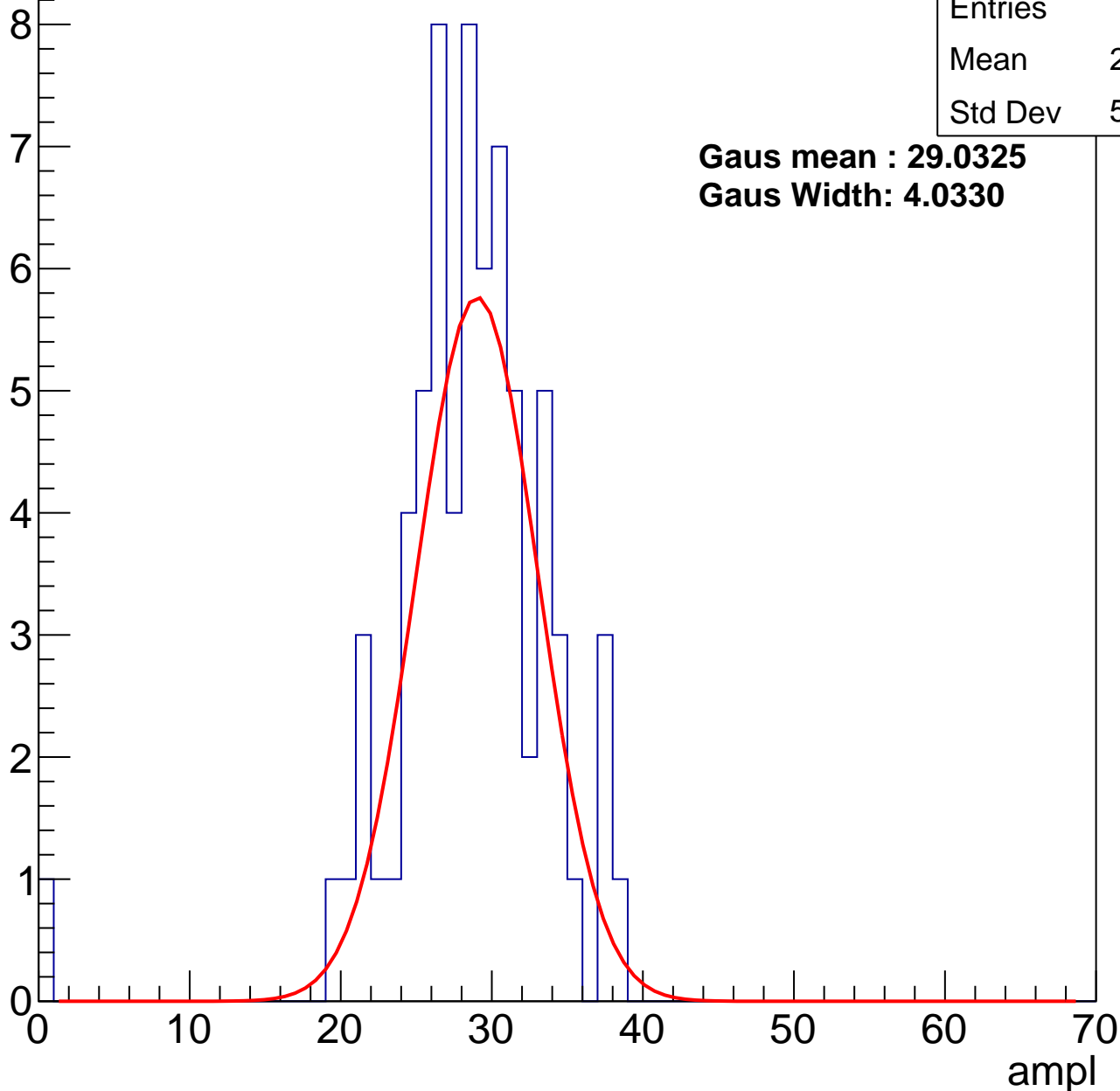
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	28.03
Std Dev	5.369

**Gaus mean : 29.0325**

**Gaus Width: 4.0330**



# B1L102S, U8-ch118, adc1

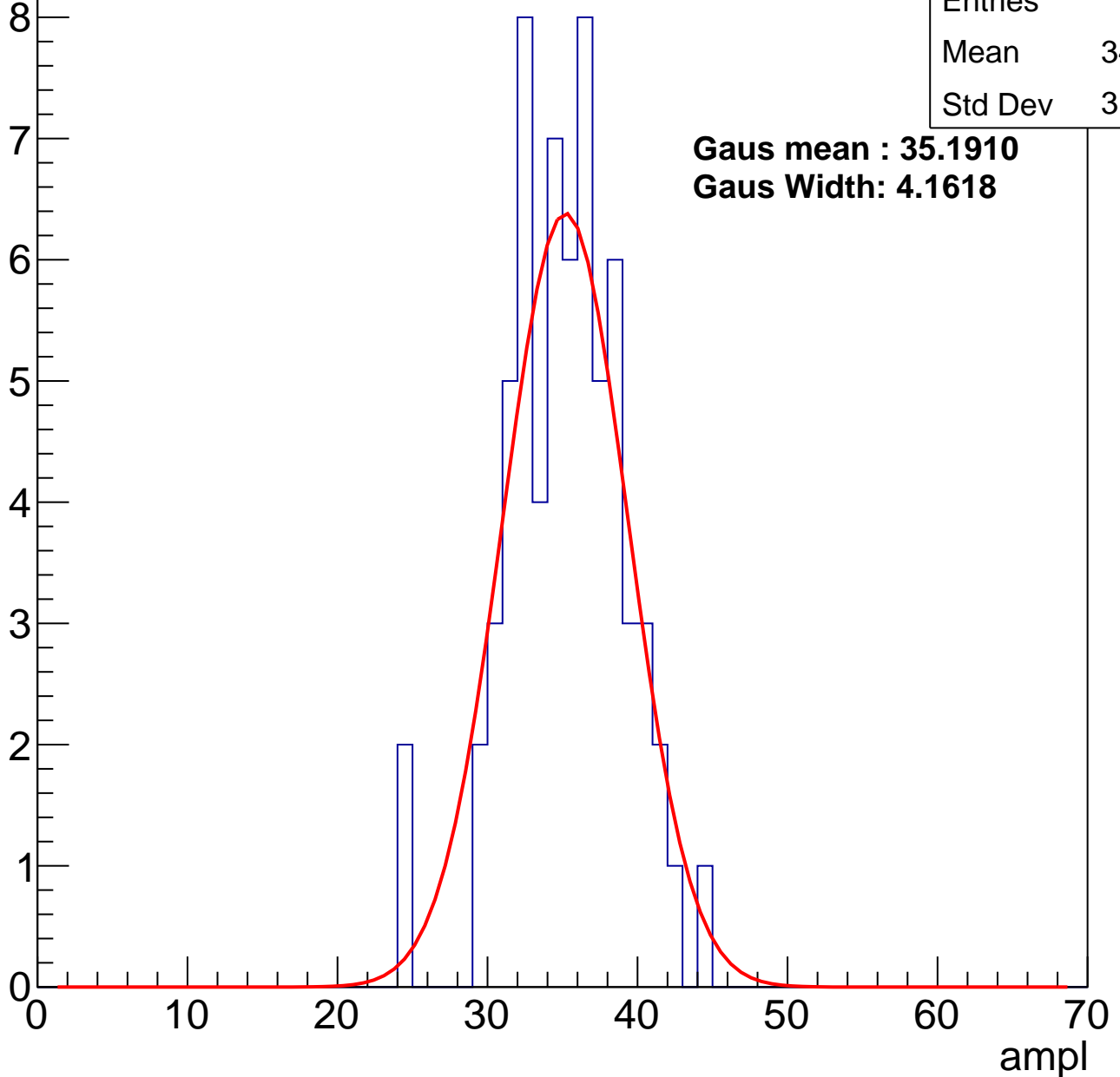
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	34.74
Std Dev	3.827

**Gaus mean : 35.1910**

**Gaus Width: 4.1618**



# B1L102S, U8-ch118, adc2

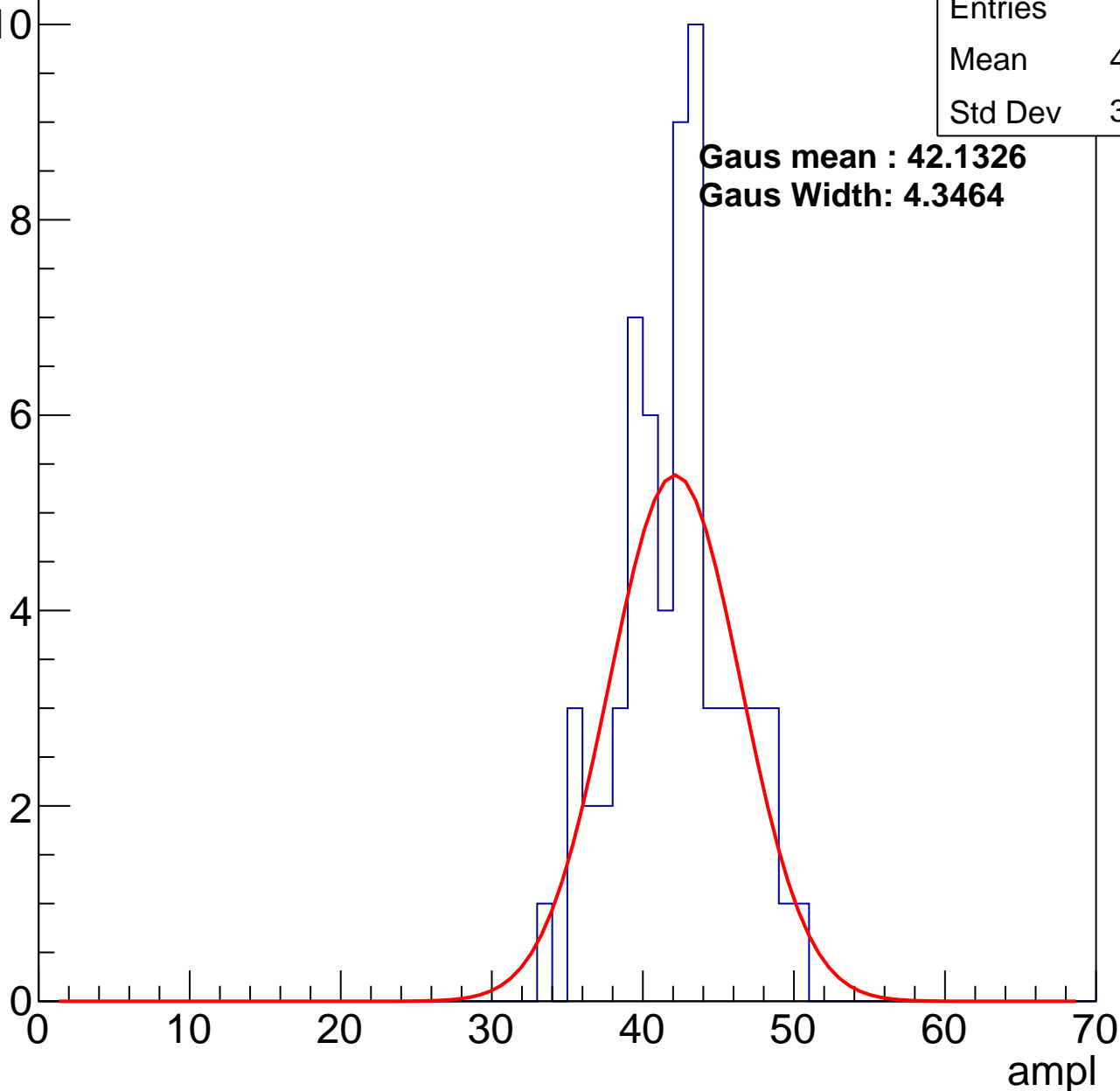
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	41.75
Std Dev	3.704

**Gaus mean : 42.1326**

**Gaus Width: 4.3464**

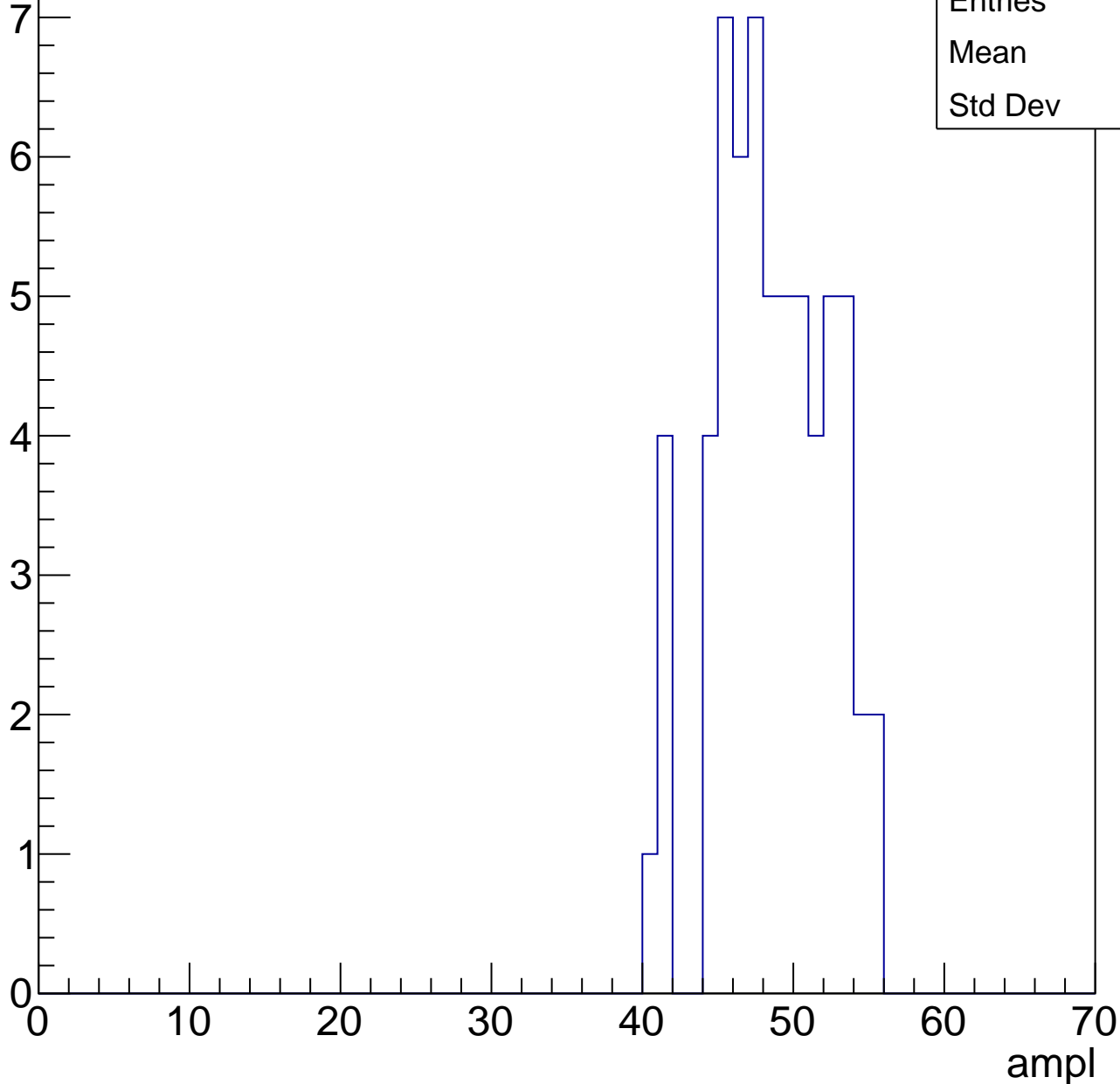


# B1L102S, U8-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

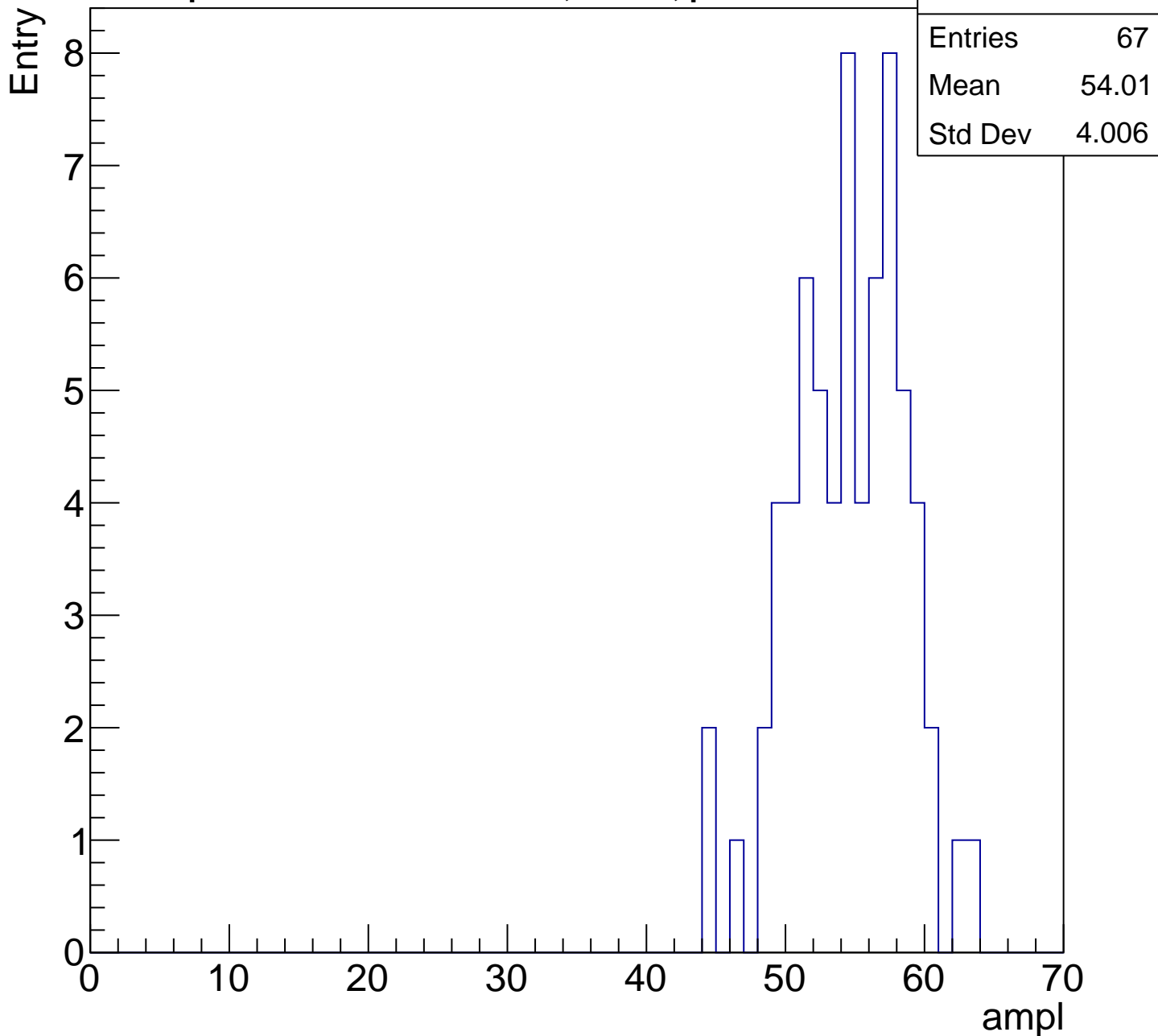
Entry

Entries	62
Mean	48.1
Std Dev	3.71



# B1L102S, U8-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

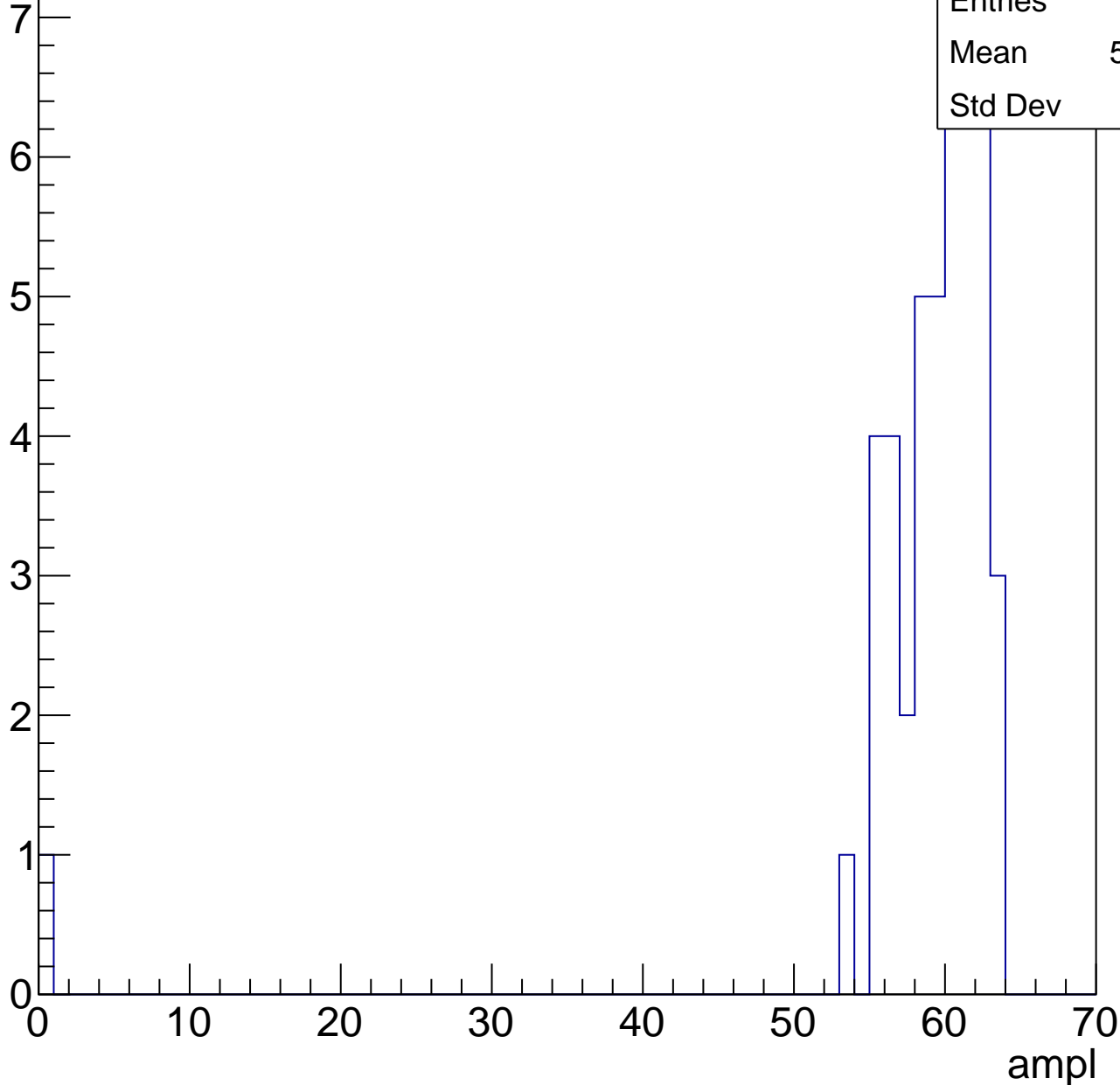


# B1L102S, U8-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	57.96
Std Dev	9

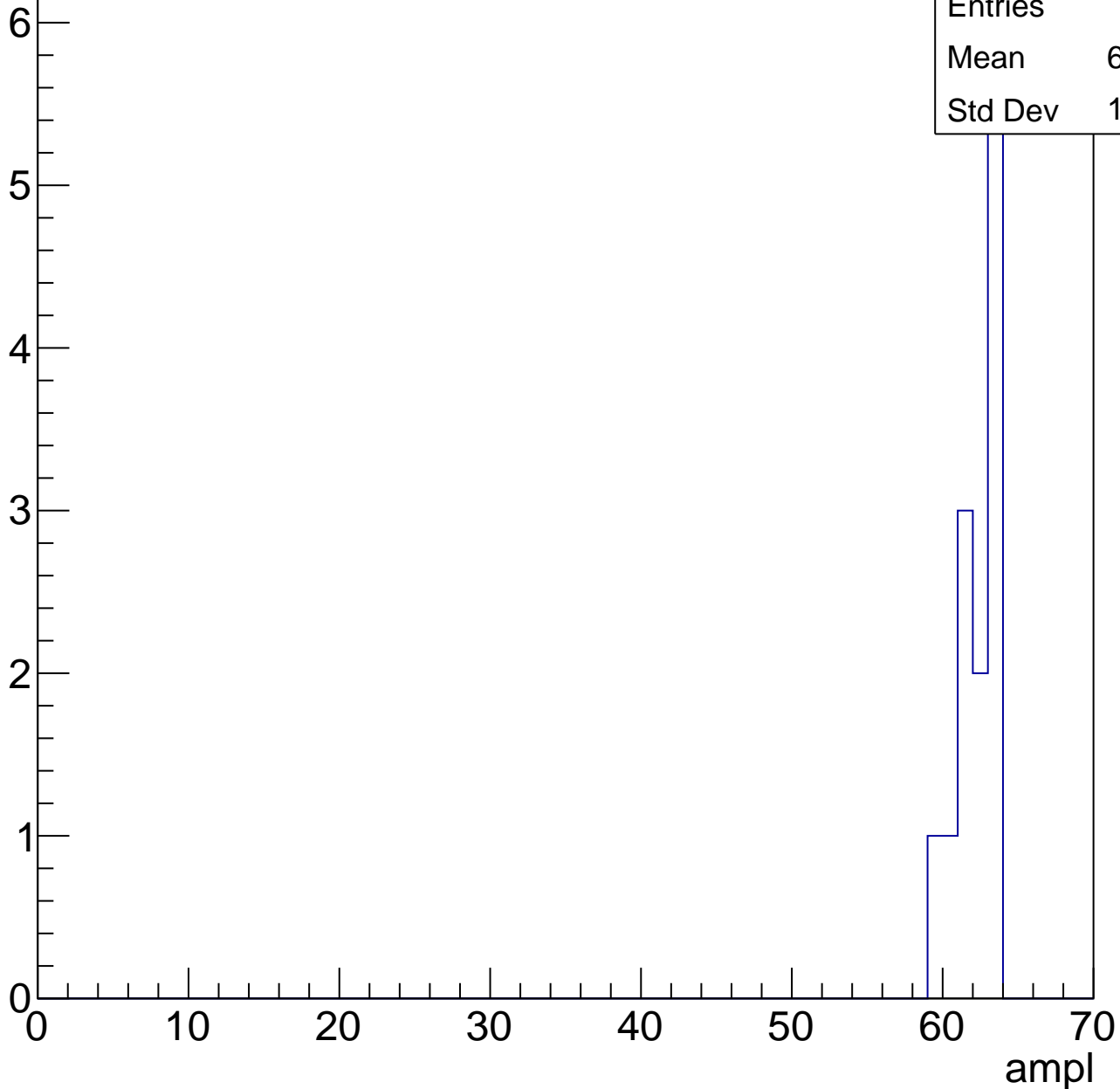


# B1L102S, U8-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	13
Mean	61.85
Std Dev	1.292

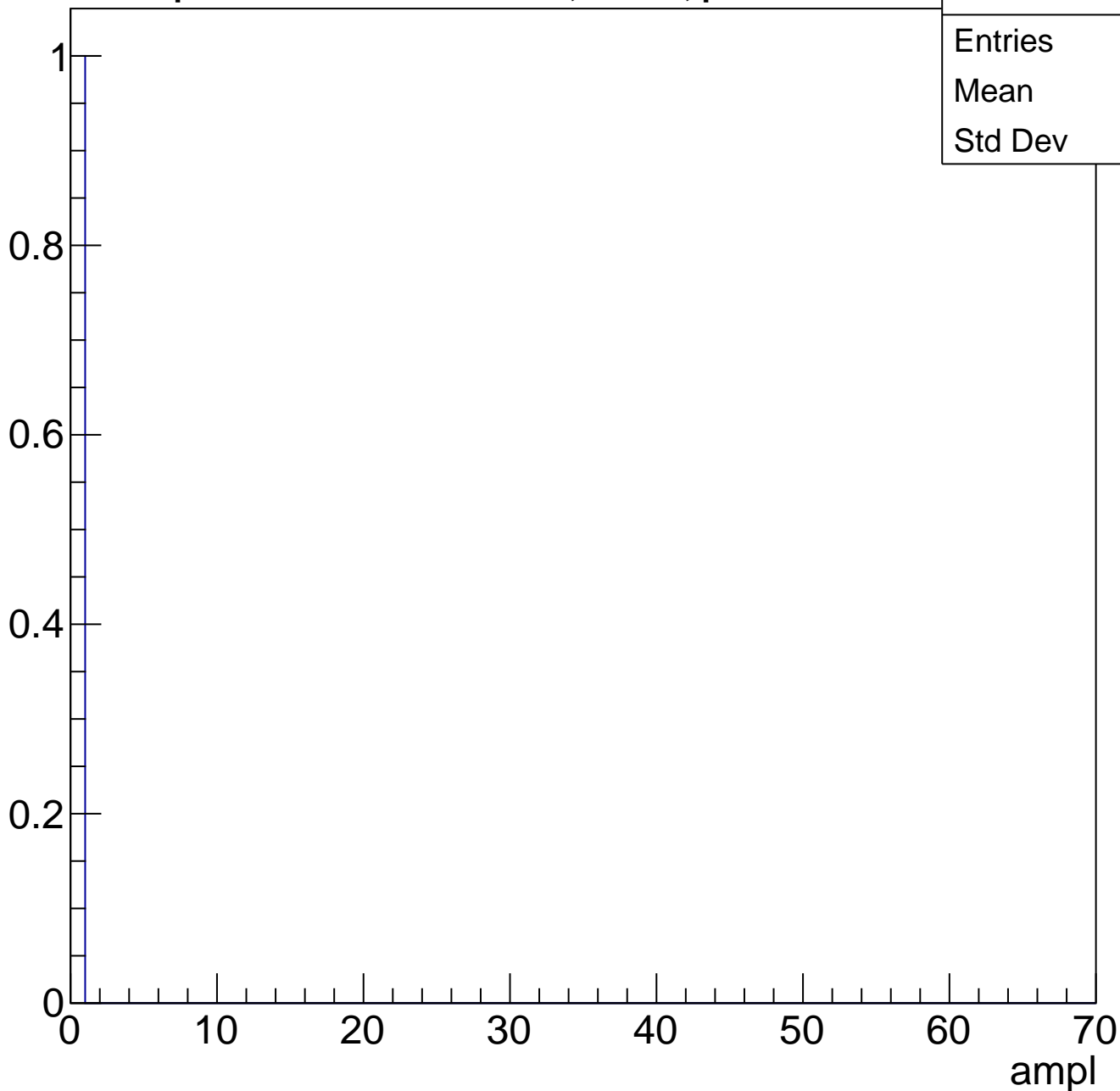




# B1L102S, U8-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U8-ch119, adc0

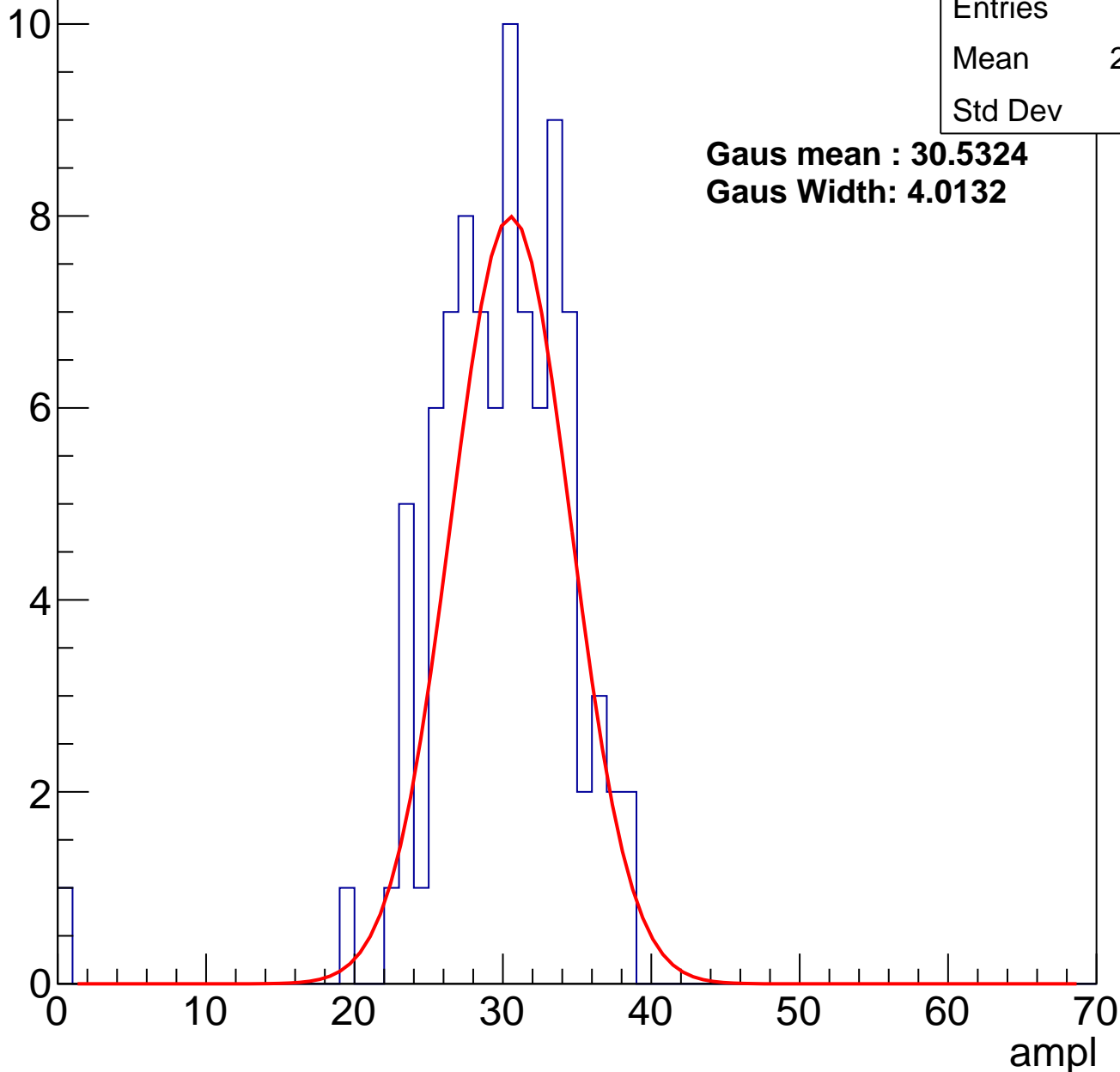
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	91
Mean	29.34
Std Dev	5.03

**Gaus mean : 30.5324**

**Gaus Width: 4.0132**

Entry



# B1L102S, U8-ch119, adc1

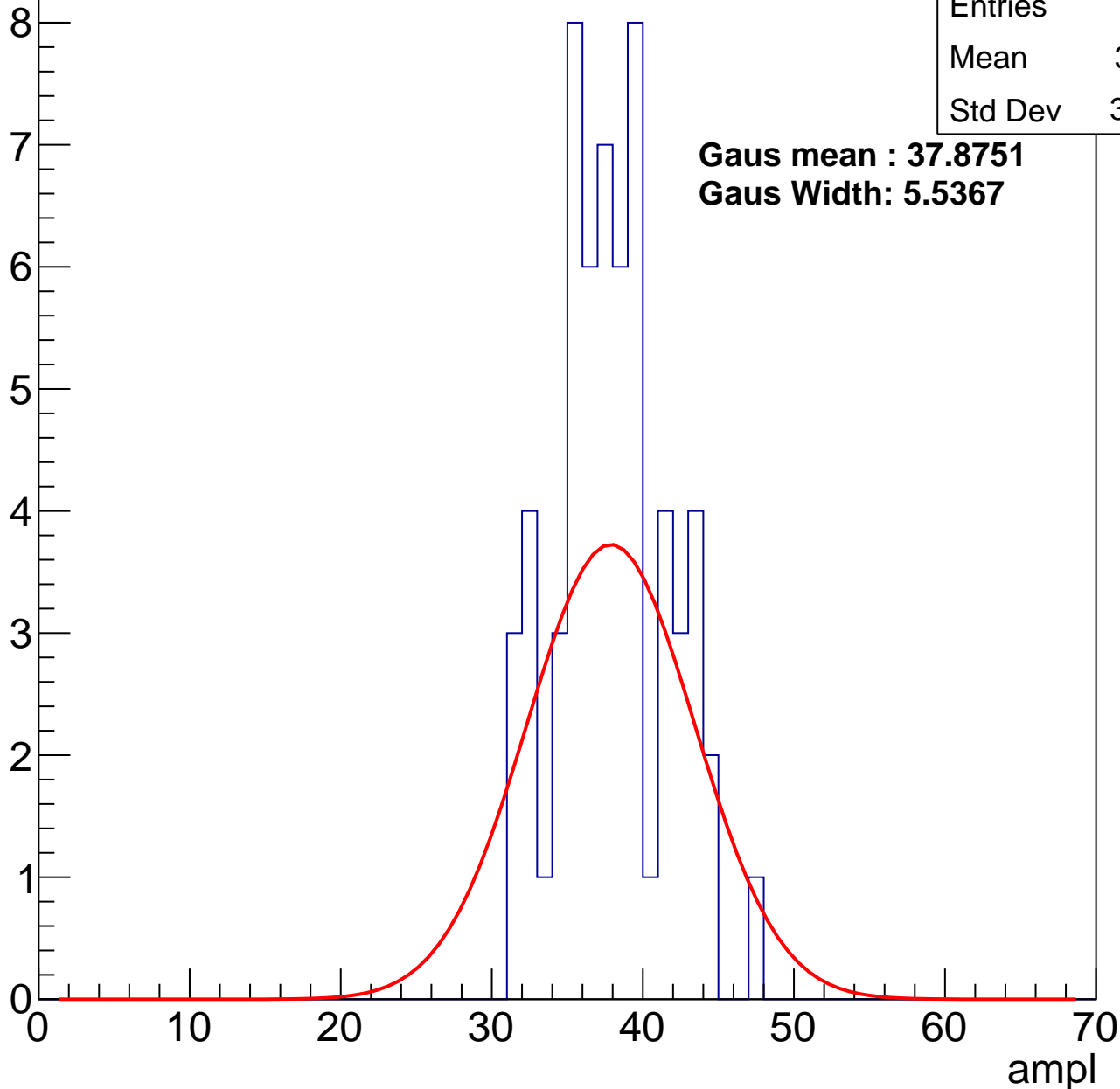
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	37.51
Std Dev	3.624

**Gaus mean : 37.8751**

**Gaus Width: 5.5367**



# B1L102S, U8-ch119, adc2

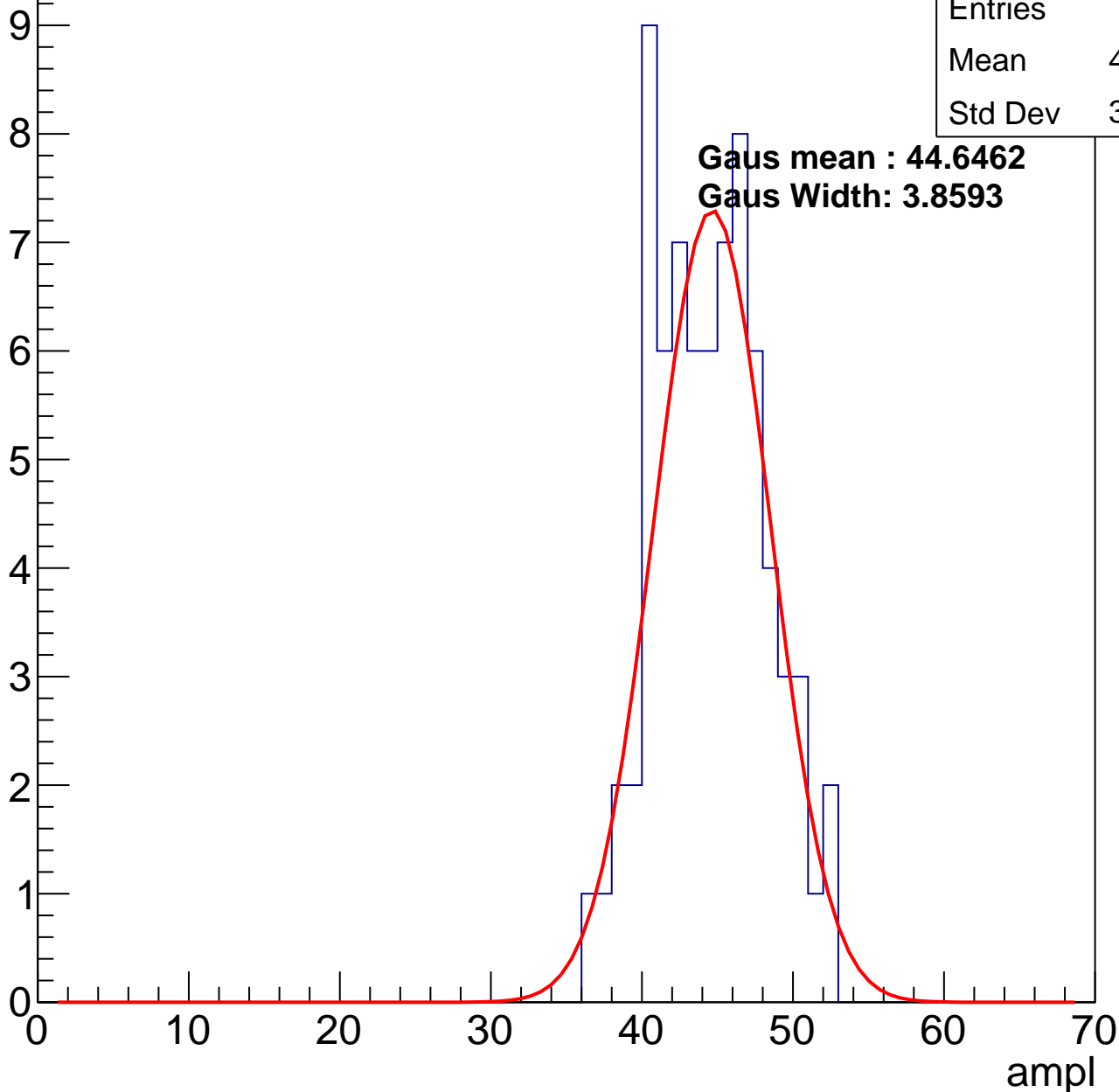
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	44.03
Std Dev	3.646

**Gaus mean : 44.6462**

**Gaus Width: 3.8593**

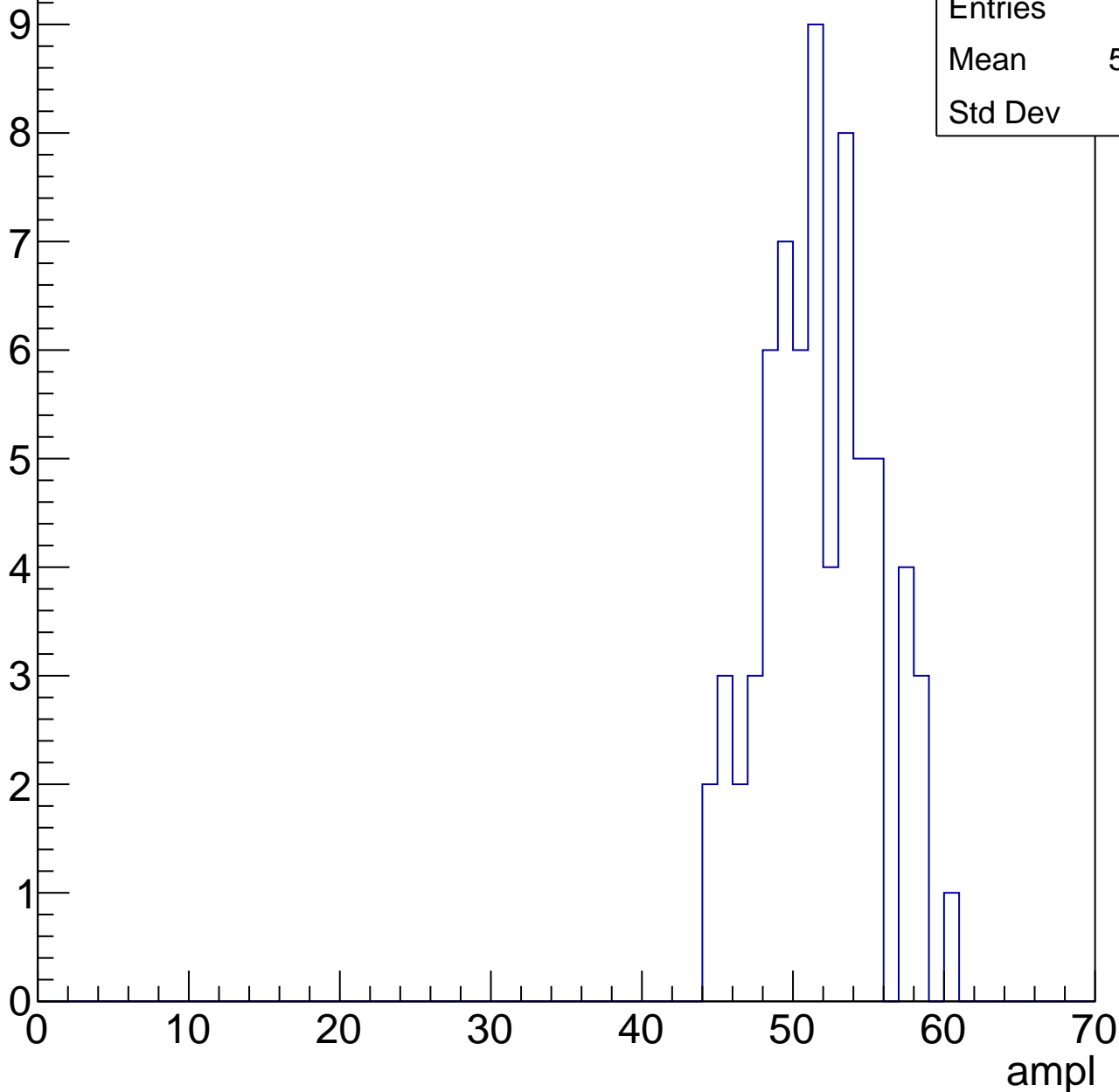


# B1L102S, U8-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	51.25
Std Dev	3.68

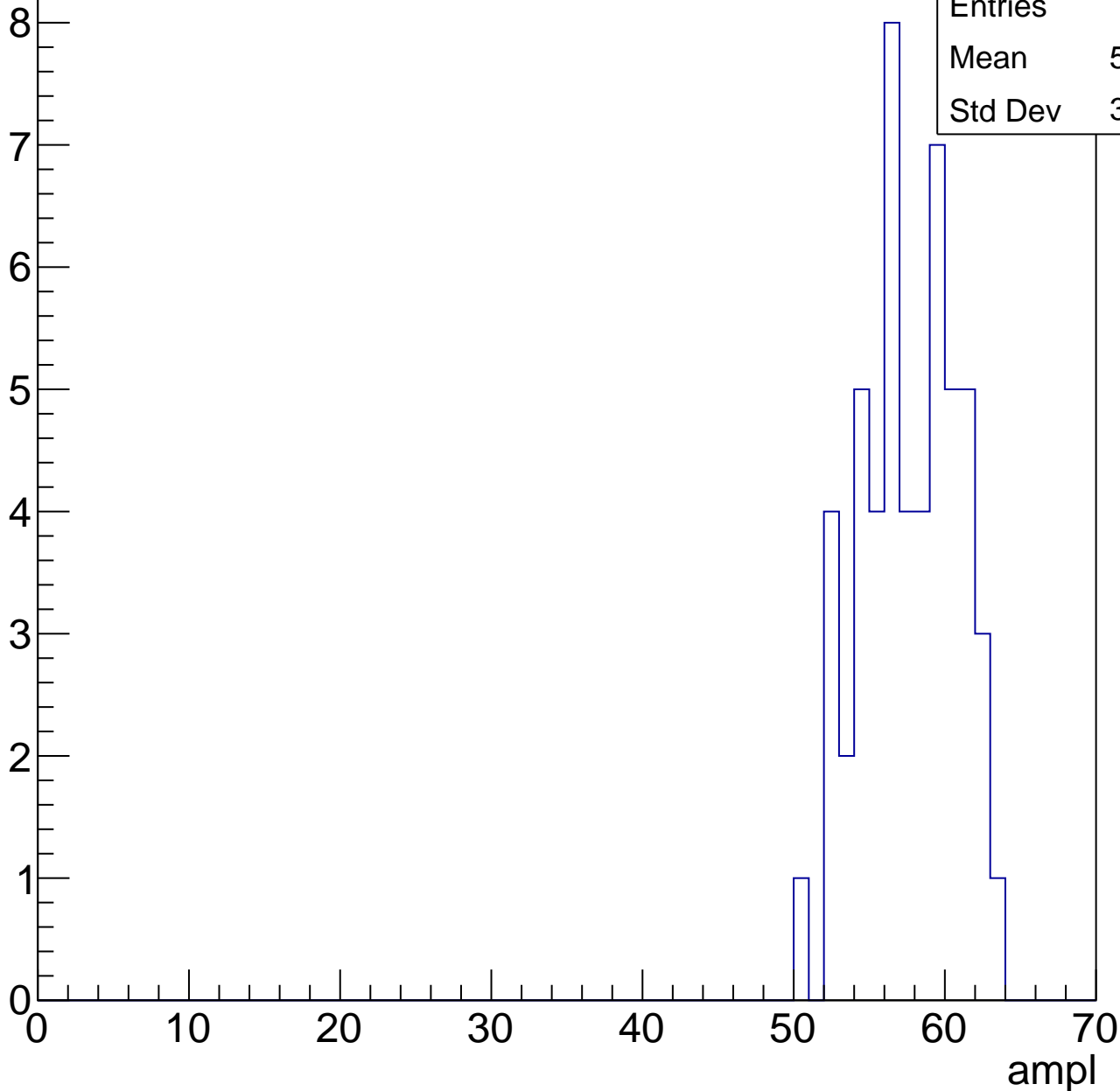


# B1L102S, U8-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	57.15
Std Dev	3.123

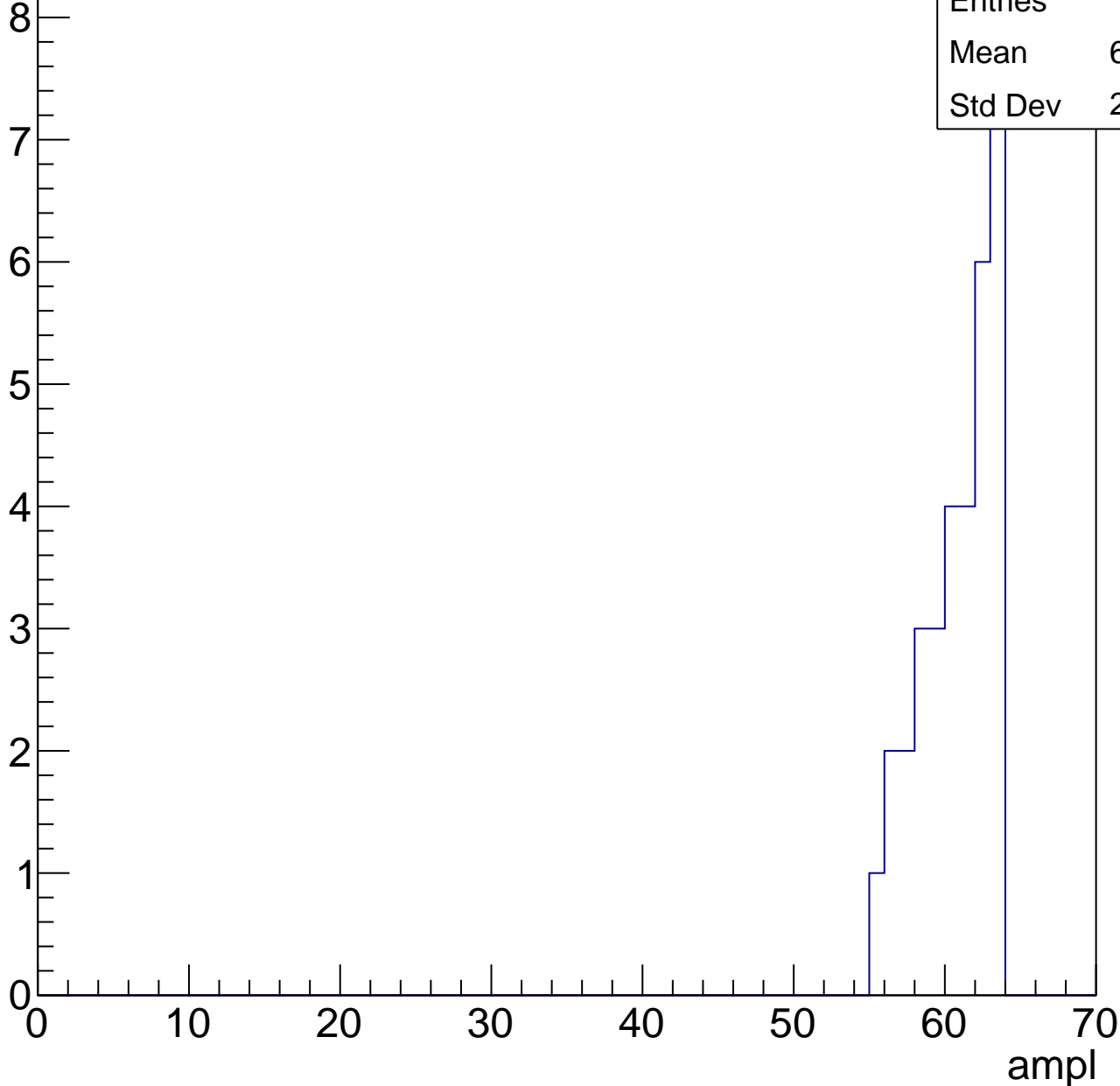


# B1L102S, U8-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	33
Mean	60.36
Std Dev	2.372



# B1L102S, U8-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U8-ch120, adc0

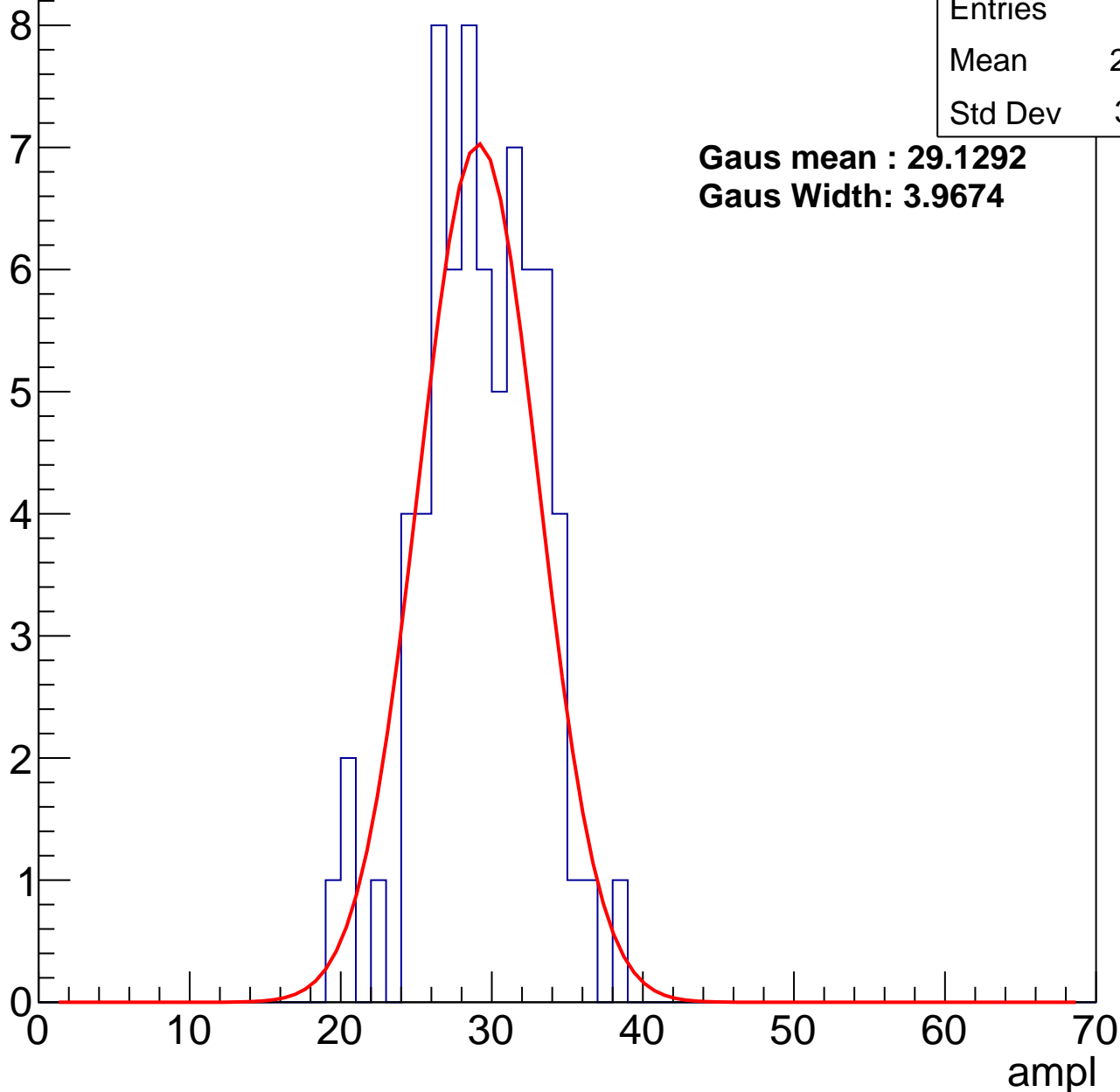
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	28.83
Std Dev	3.801

**Gaus mean : 29.1292**

**Gaus Width: 3.9674**



# B1L102S, U8-ch120, adc1

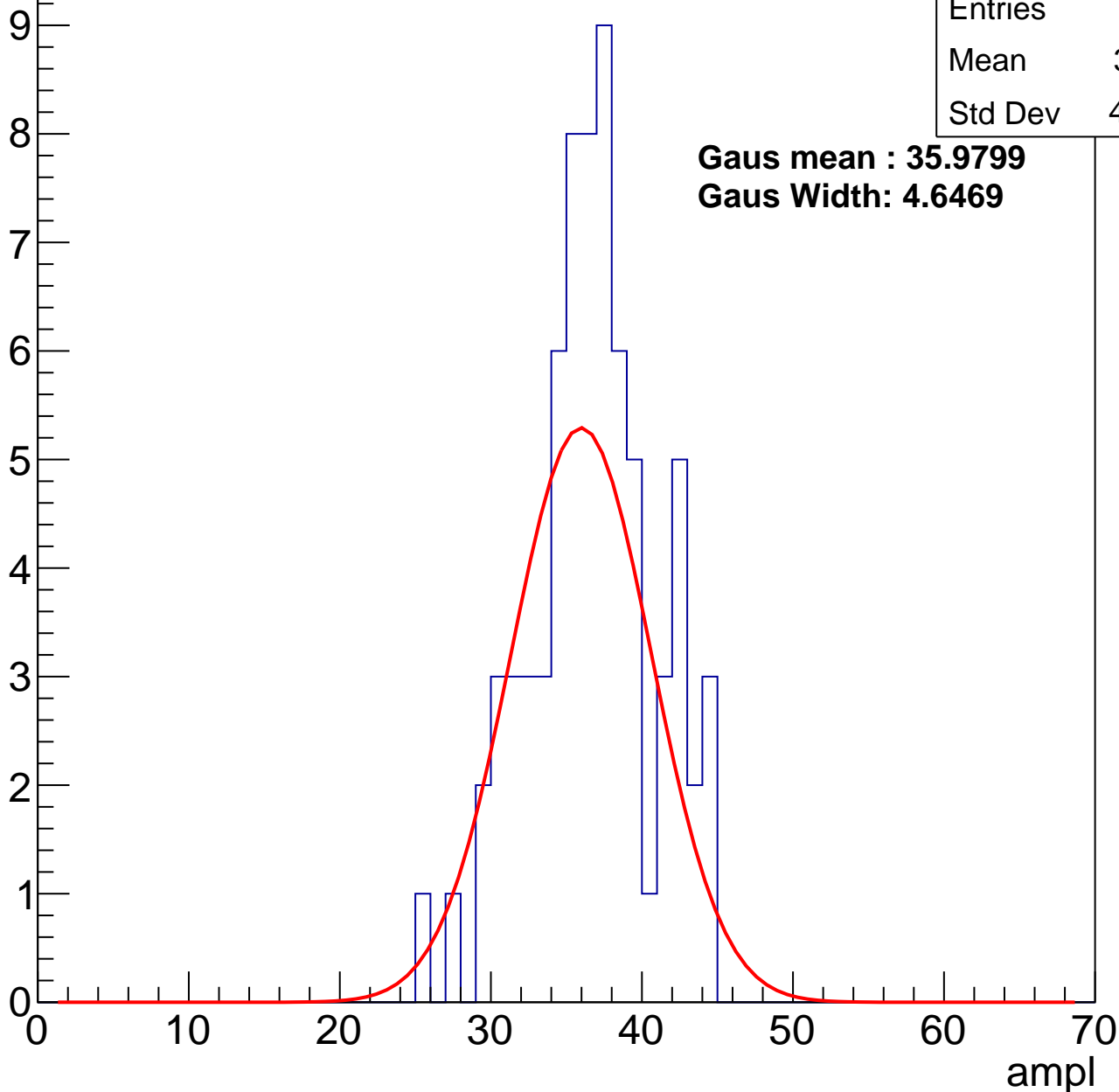
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	36.21
Std Dev	4.126

**Gaus mean : 35.9799**

**Gaus Width: 4.6469**



# B1L102S, U8-ch120, adc2

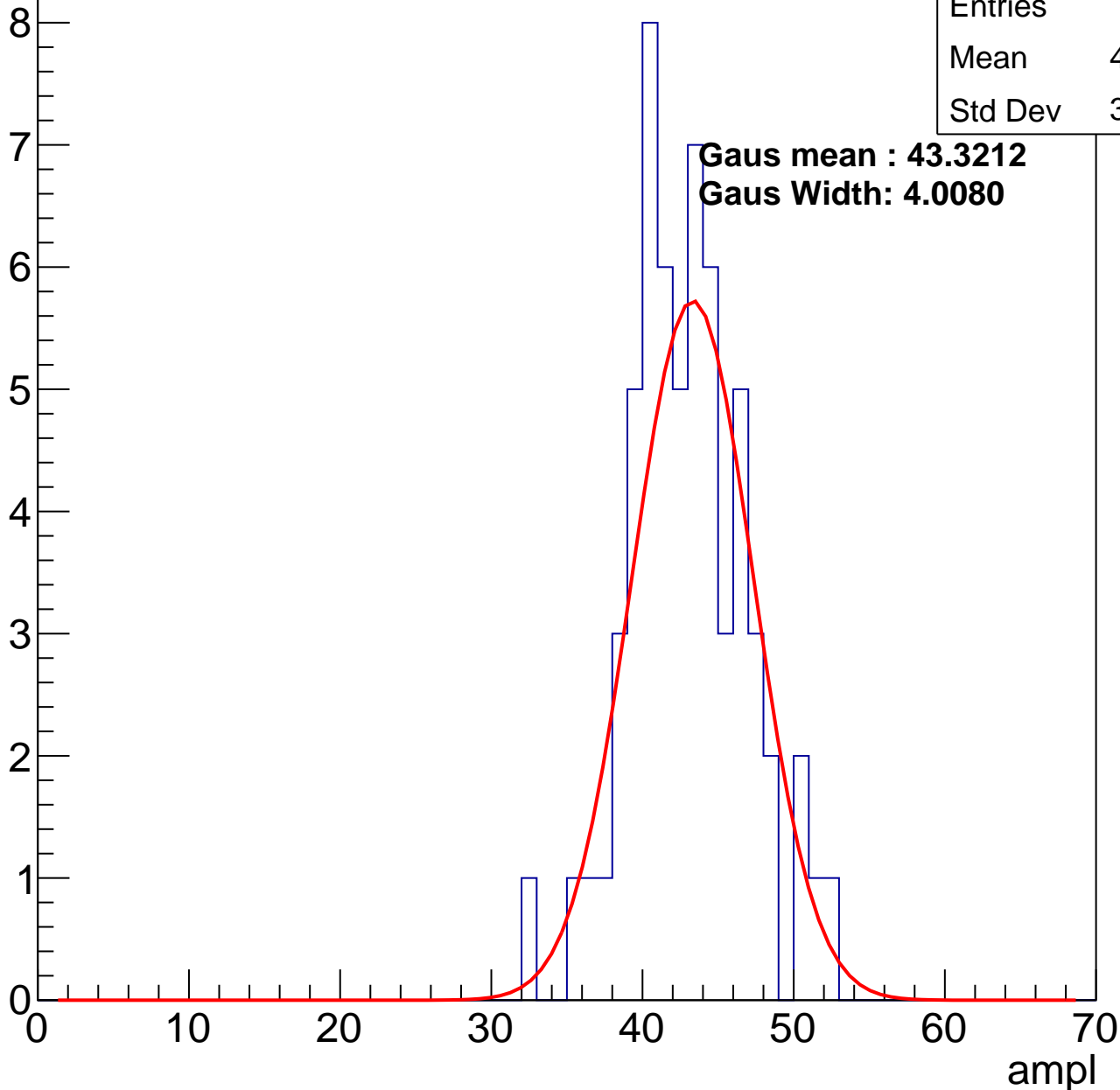
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	42.54
Std Dev	3.878

**Gaus mean : 43.3212**

**Gaus Width: 4.0080**

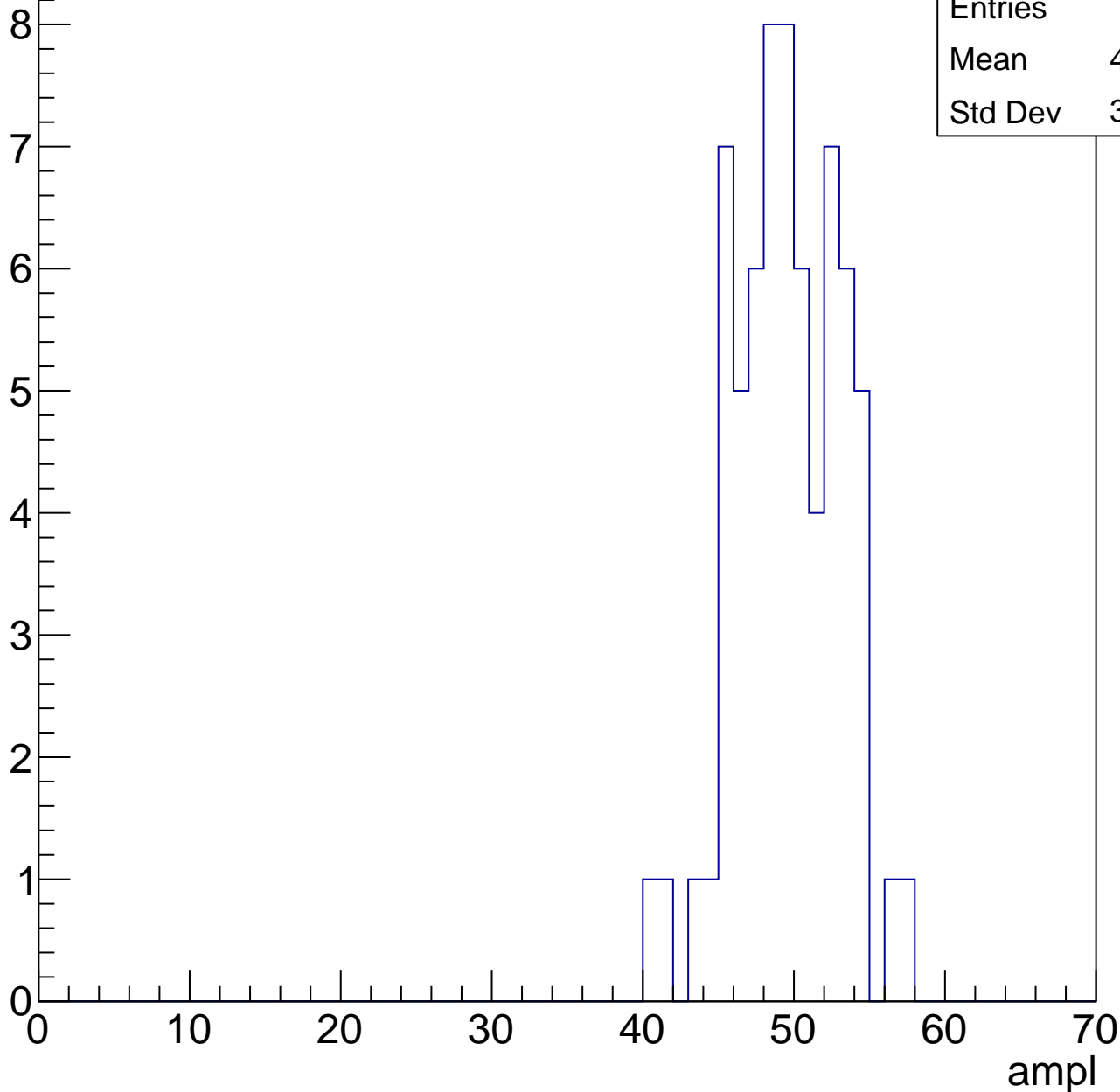


# B1L102S, U8-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	49.12
Std Dev	3.458

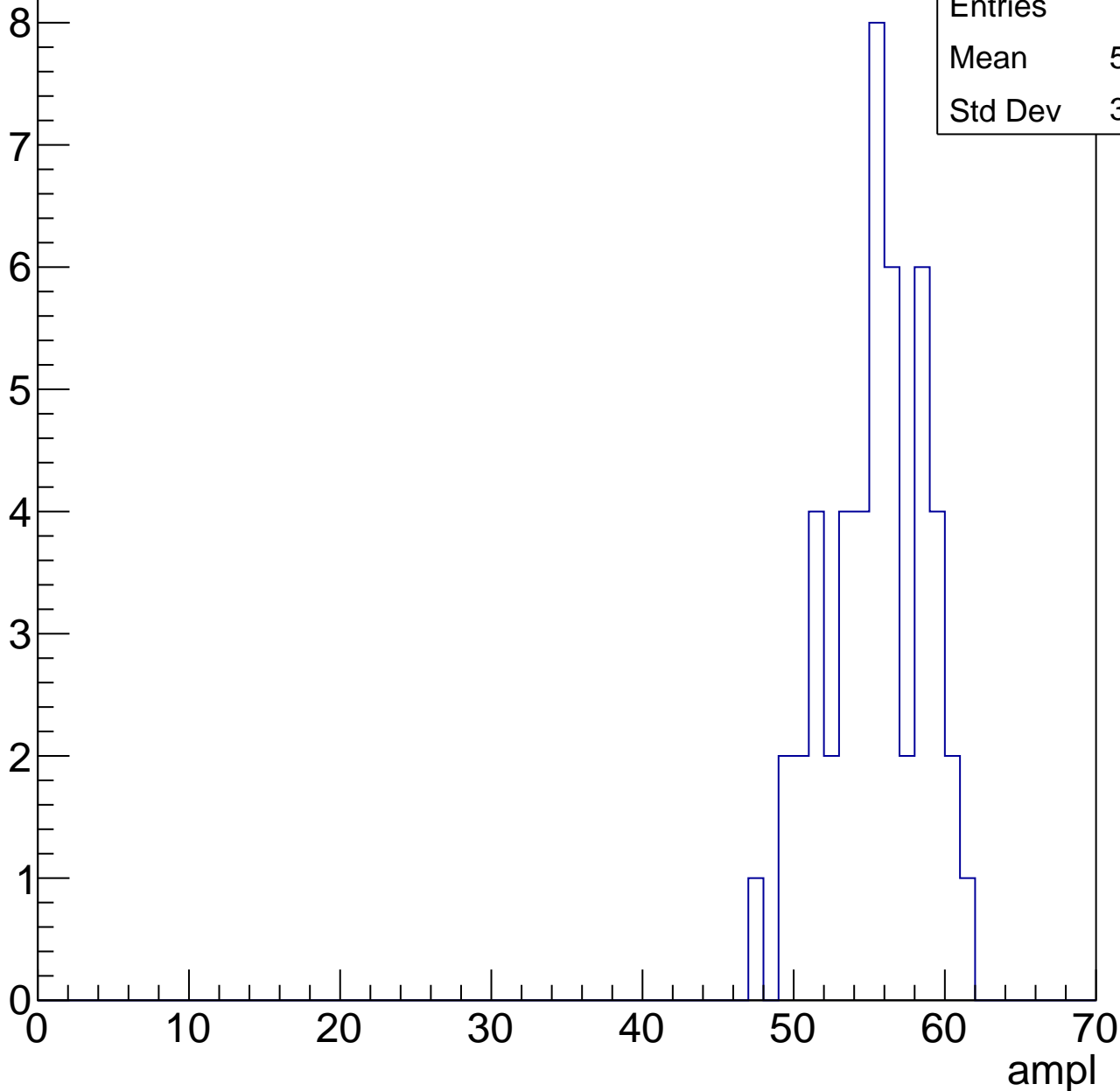


# B1L102S, U8-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	54.92
Std Dev	3.246

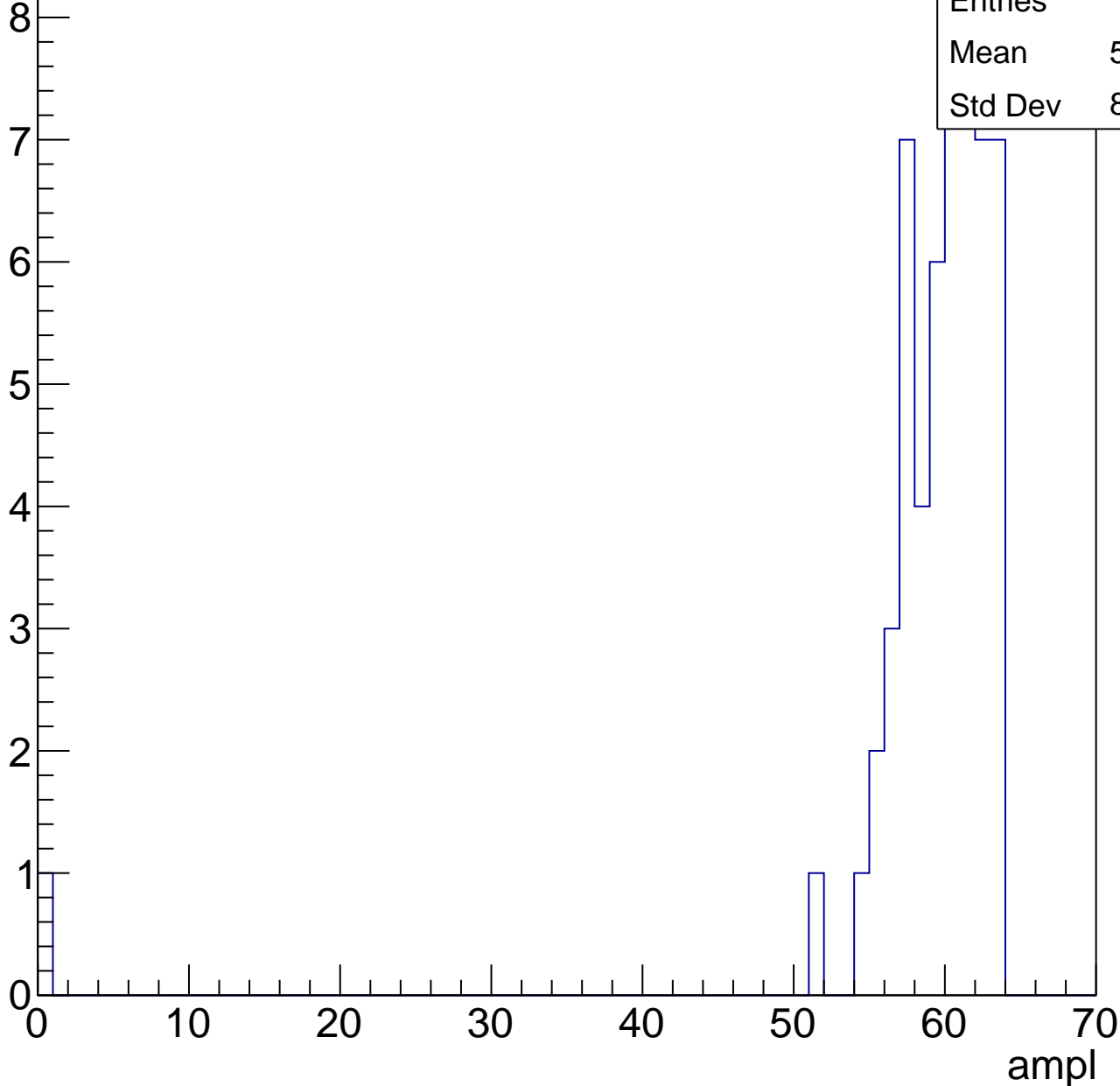


# B1L102S, U8-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	58.38
Std Dev	8.372



# B1L102S, U8-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U8-ch121, adc0

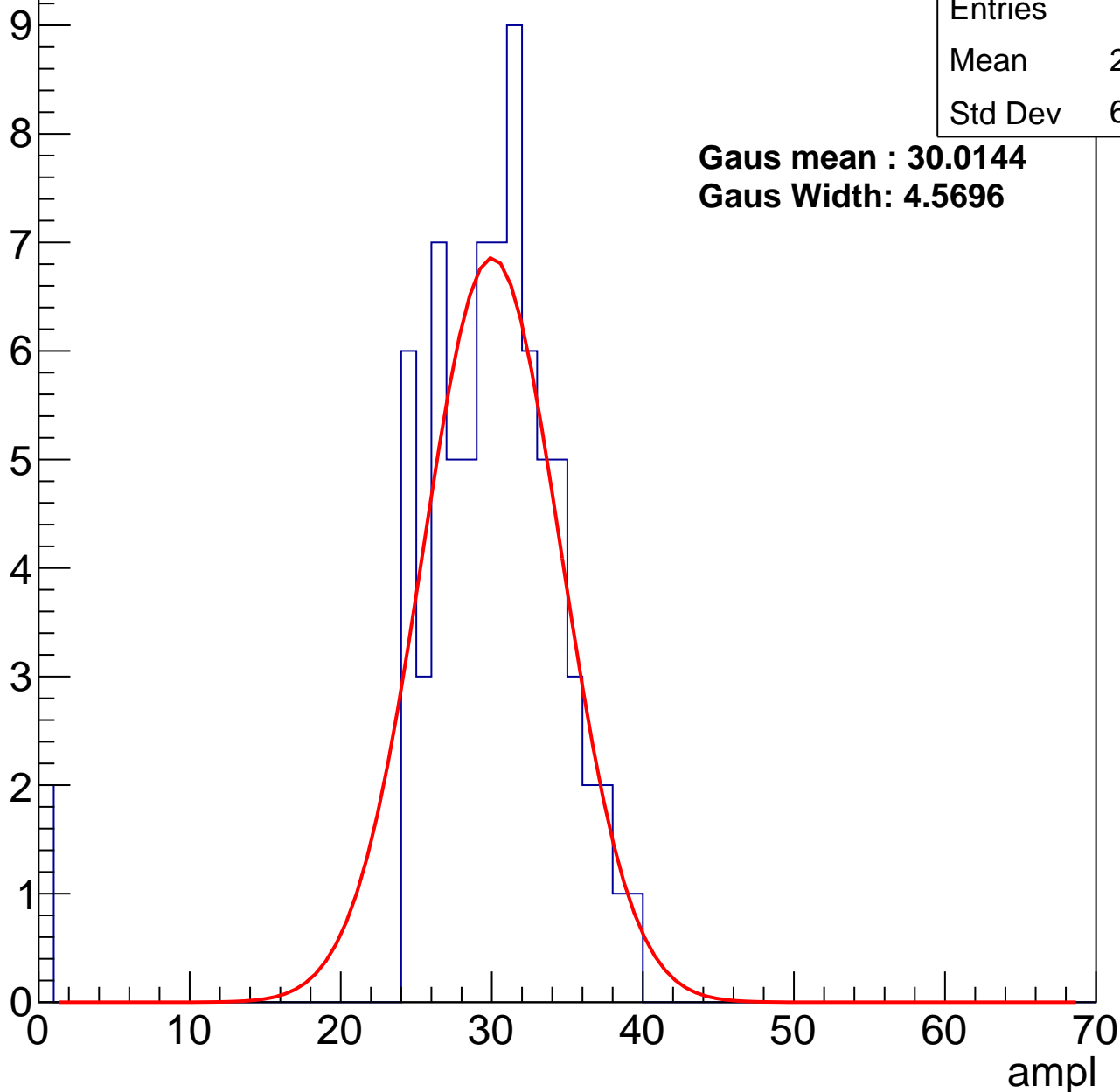
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	29.25
Std Dev	6.048

**Gaus mean : 30.0144**

**Gaus Width: 4.5696**



# B1L102S, U8-ch121, adc1

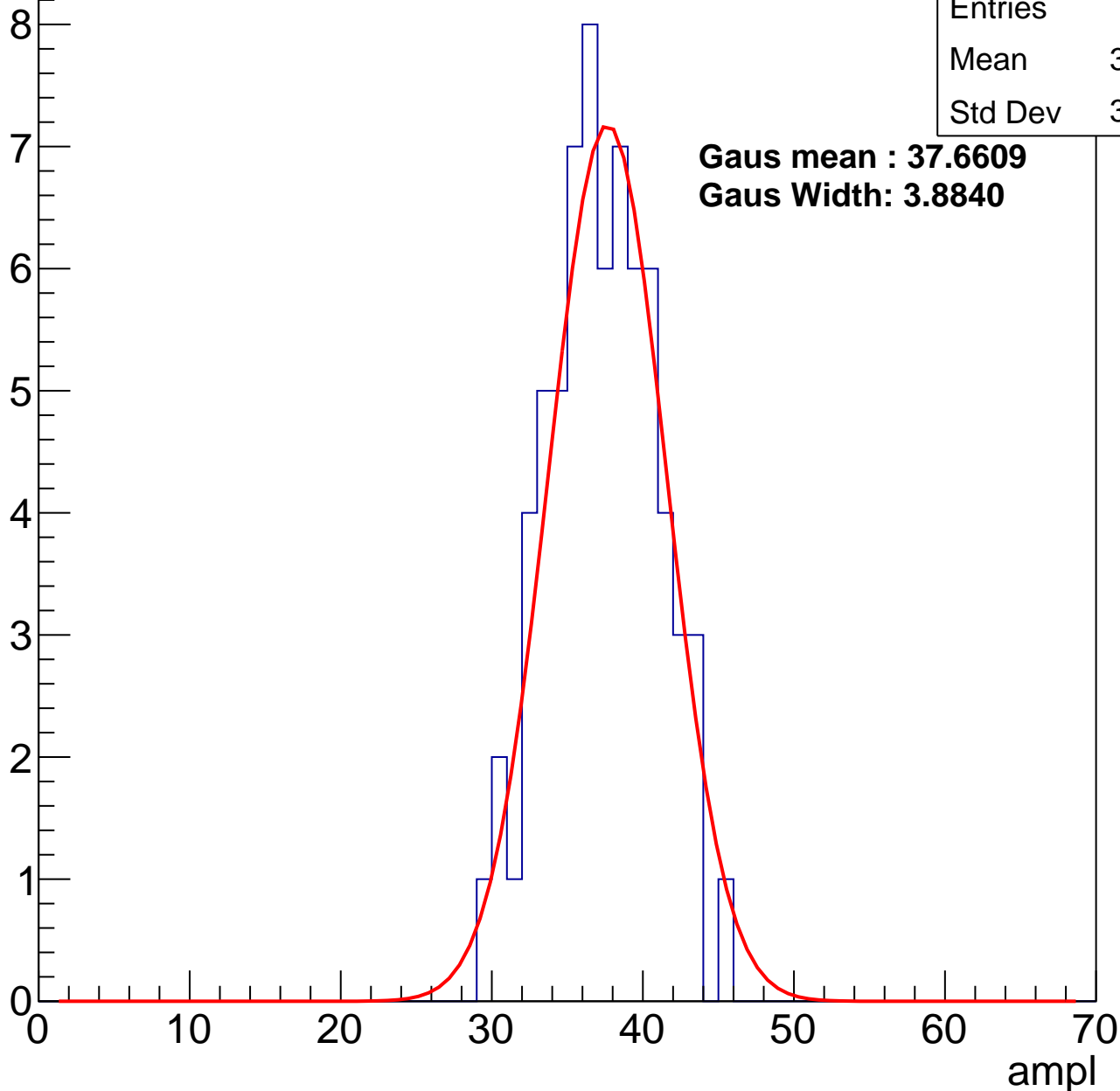
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	36.84
Std Dev	3.517

**Gaus mean : 37.6609**

**Gaus Width: 3.8840**



# B1L102S, U8-ch121, adc2

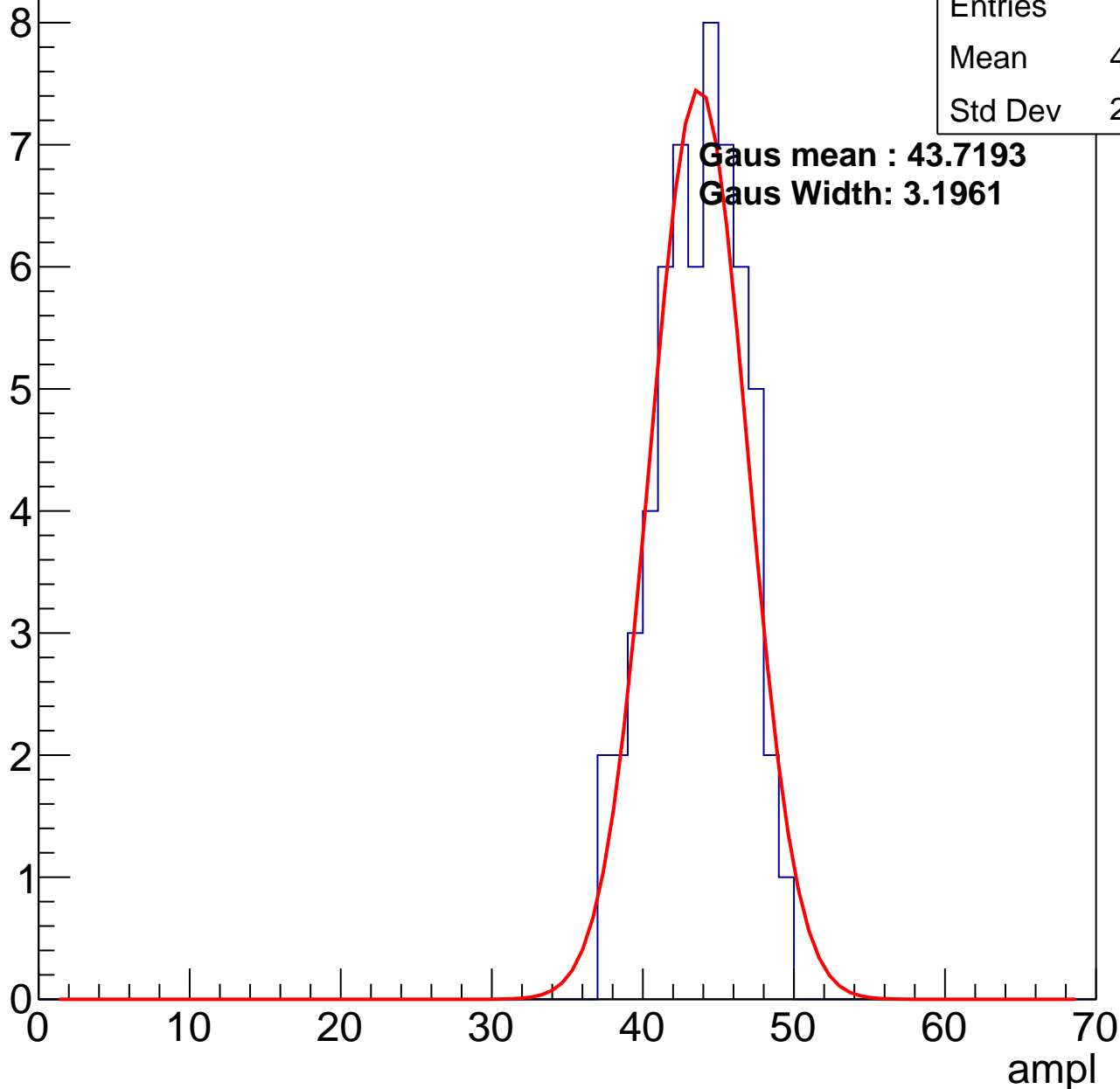
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	43.19
Std Dev	2.885

**Gaus mean : 43.7193**

**Gaus Width: 3.1961**



# B1L102S, U8-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	72
Mean	50.25
Std Dev	3.179

Entry

10

8

6

4

2

0

0

10

20

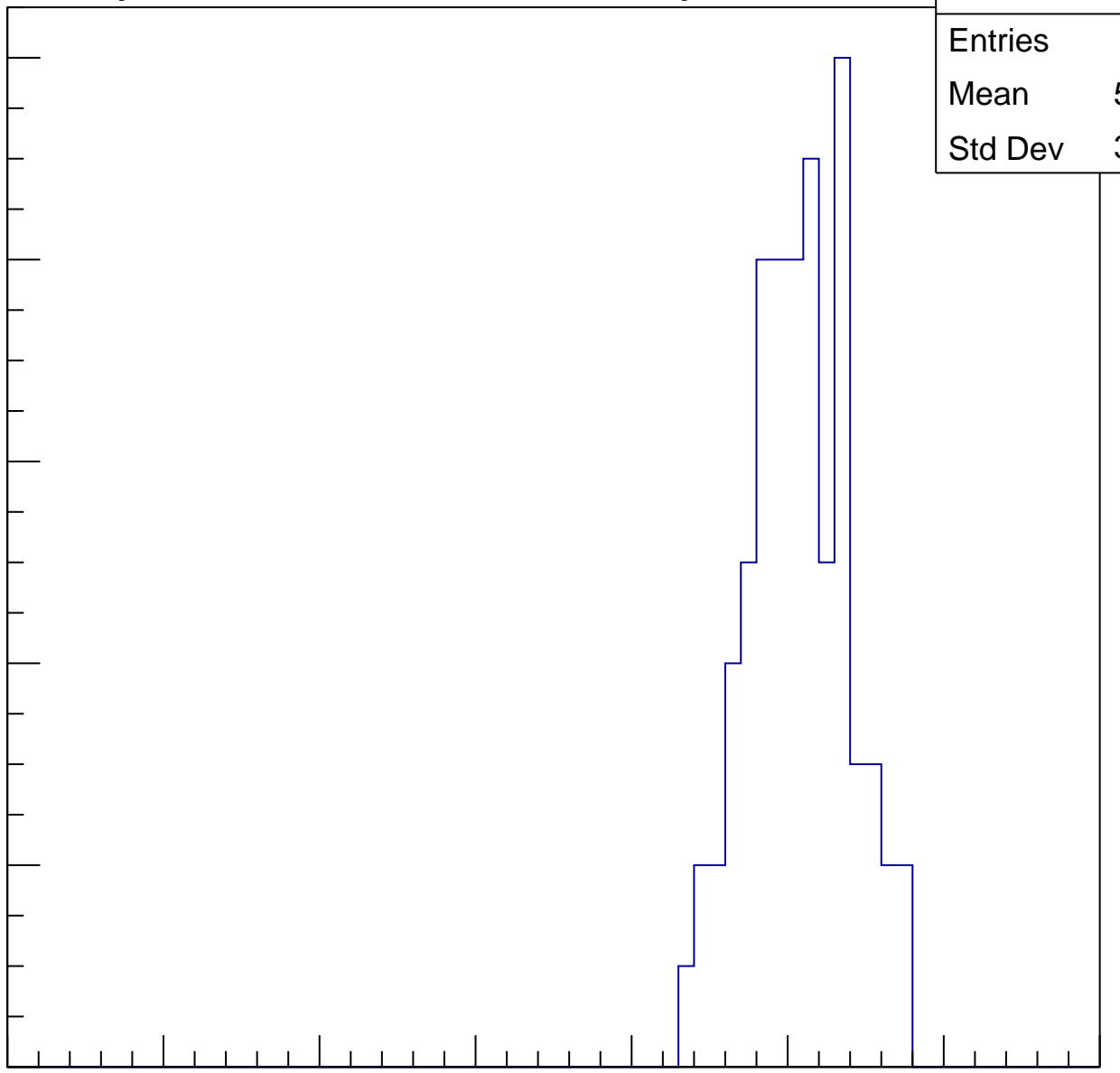
30

40

50

60

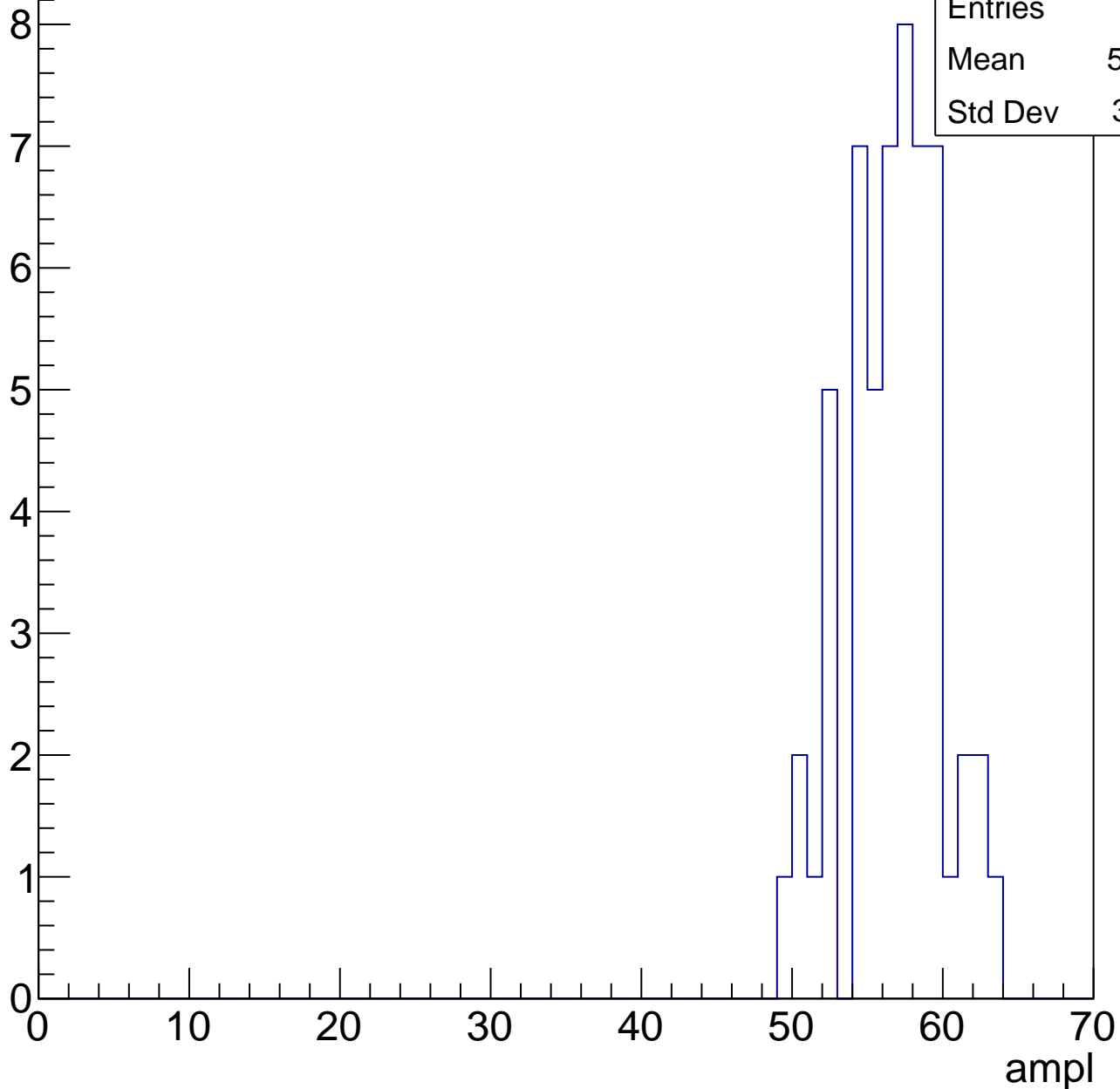
ampl



# B1L102S, U8-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

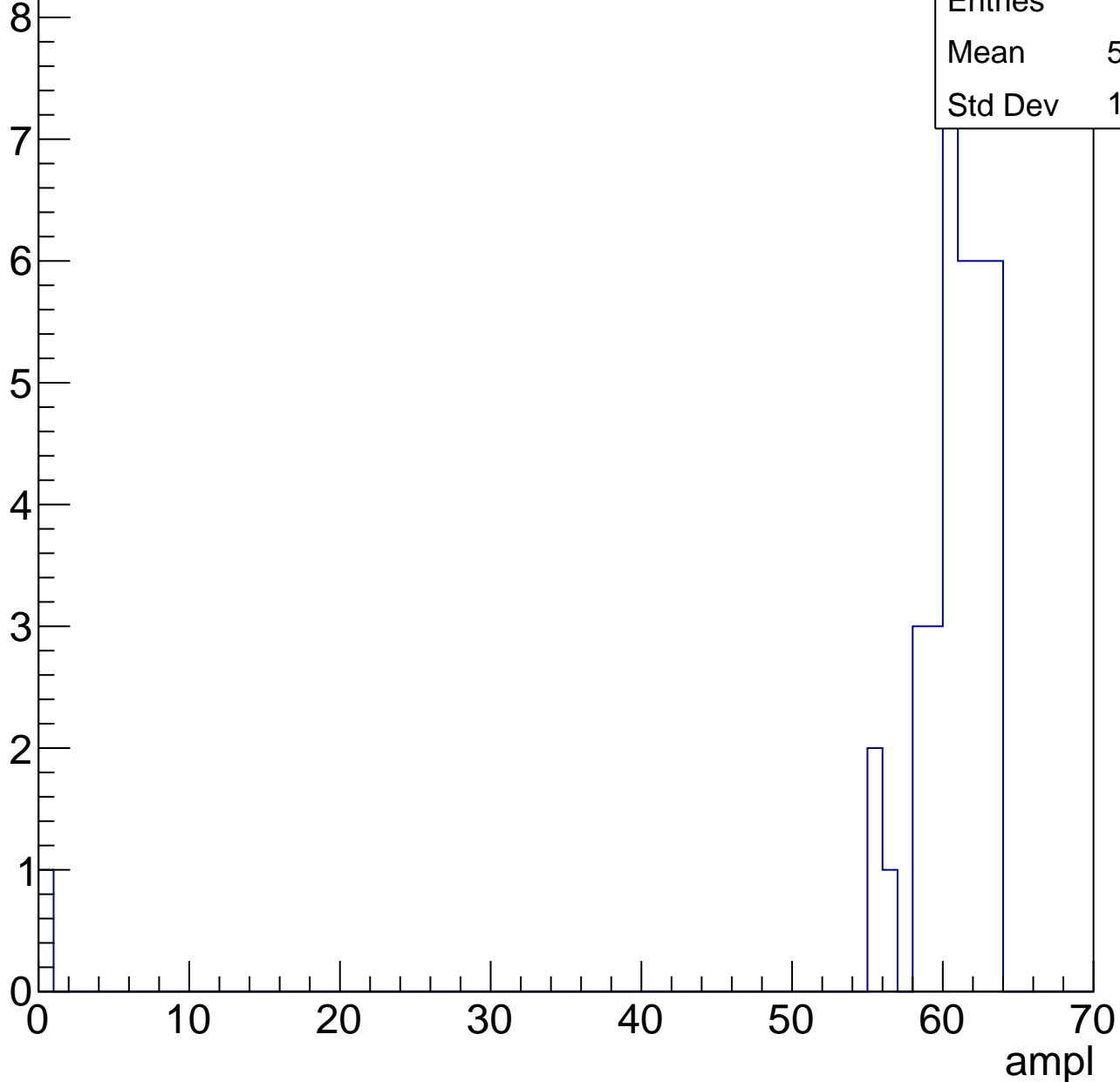
Entry



# B1L102S, U8-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch122, adc0

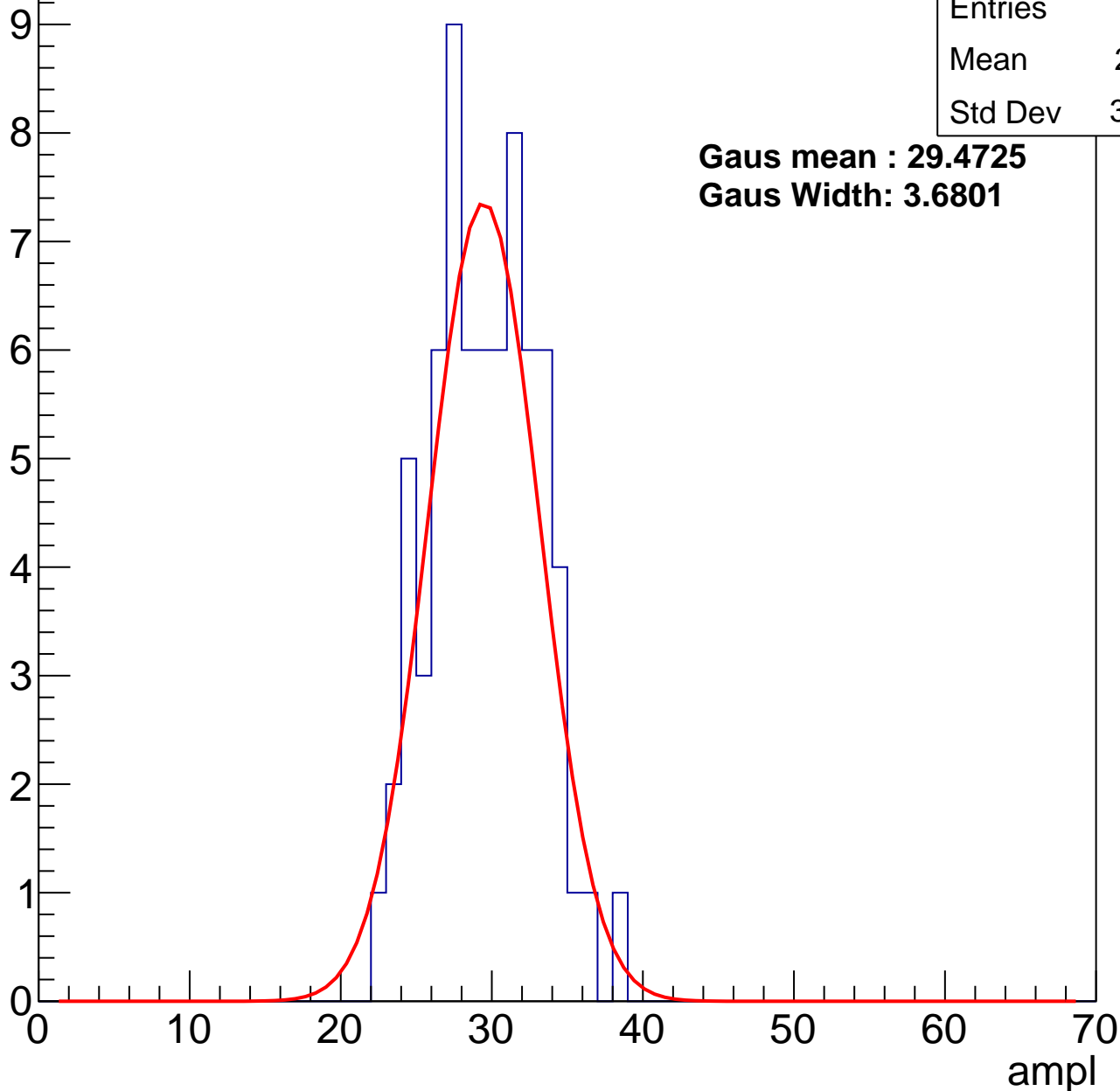
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	29.11
Std Dev	3.446

**Gaus mean : 29.4725**

**Gaus Width: 3.6801**



# B1L102S, U8-ch122, adc1

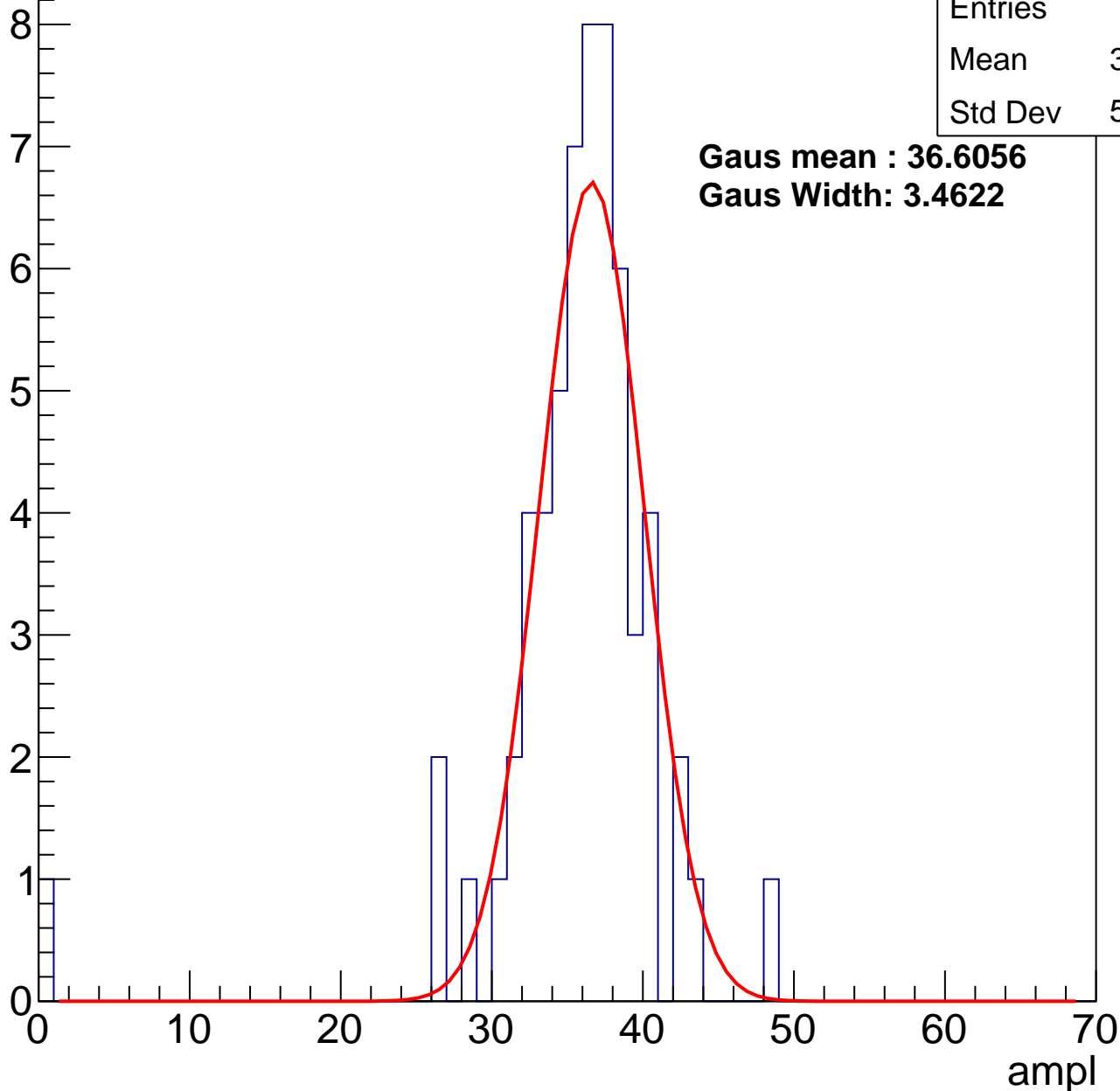
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	35.18
Std Dev	5.946

**Gaus mean : 36.6056**

**Gaus Width: 3.4622**



# B1L102S, U8-ch122, adc2

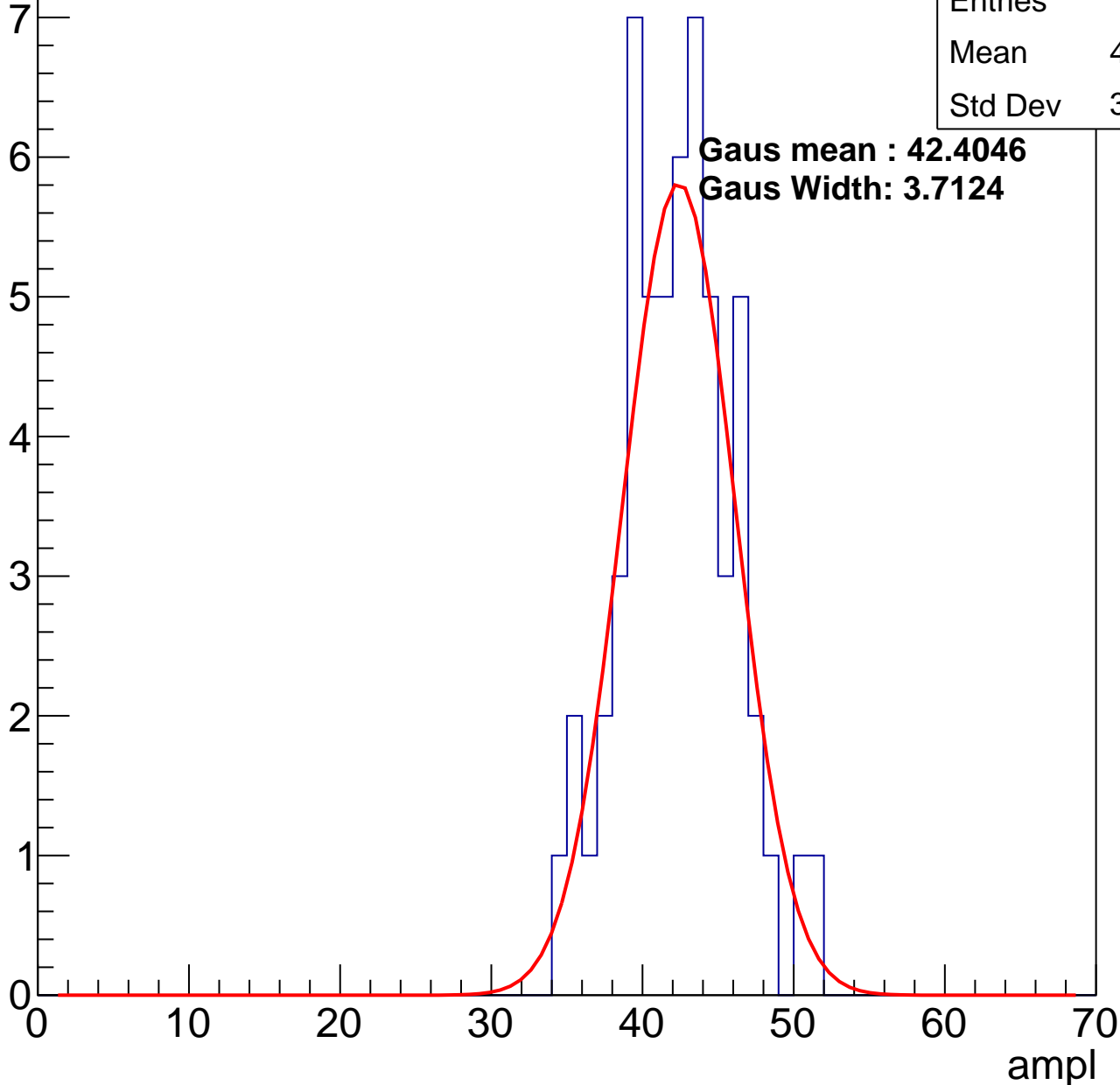
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	41.88
Std Dev	3.623

**Gaus mean : 42.4046**

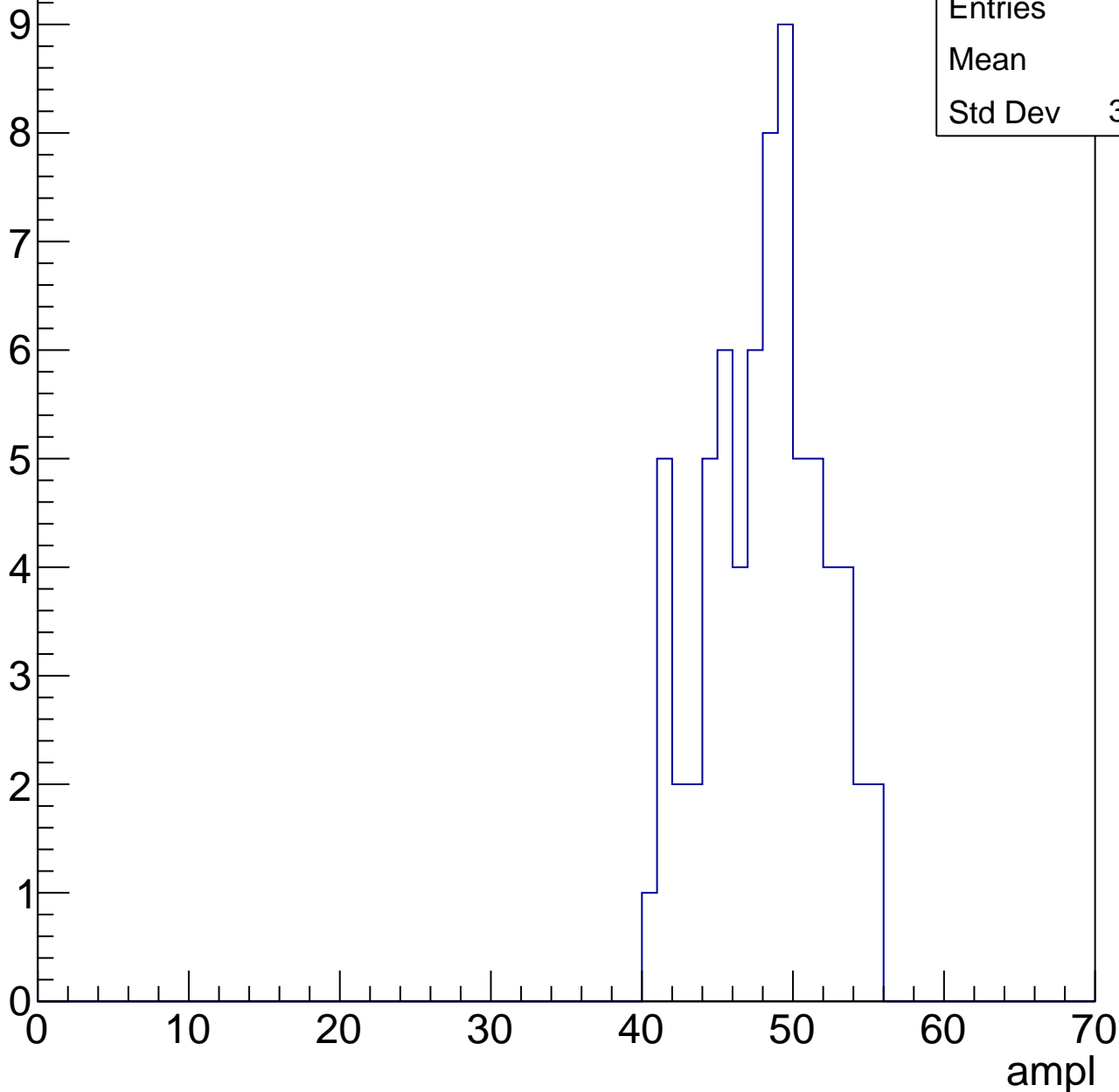
**Gaus Width: 3.7124**



# B1L102S, U8-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



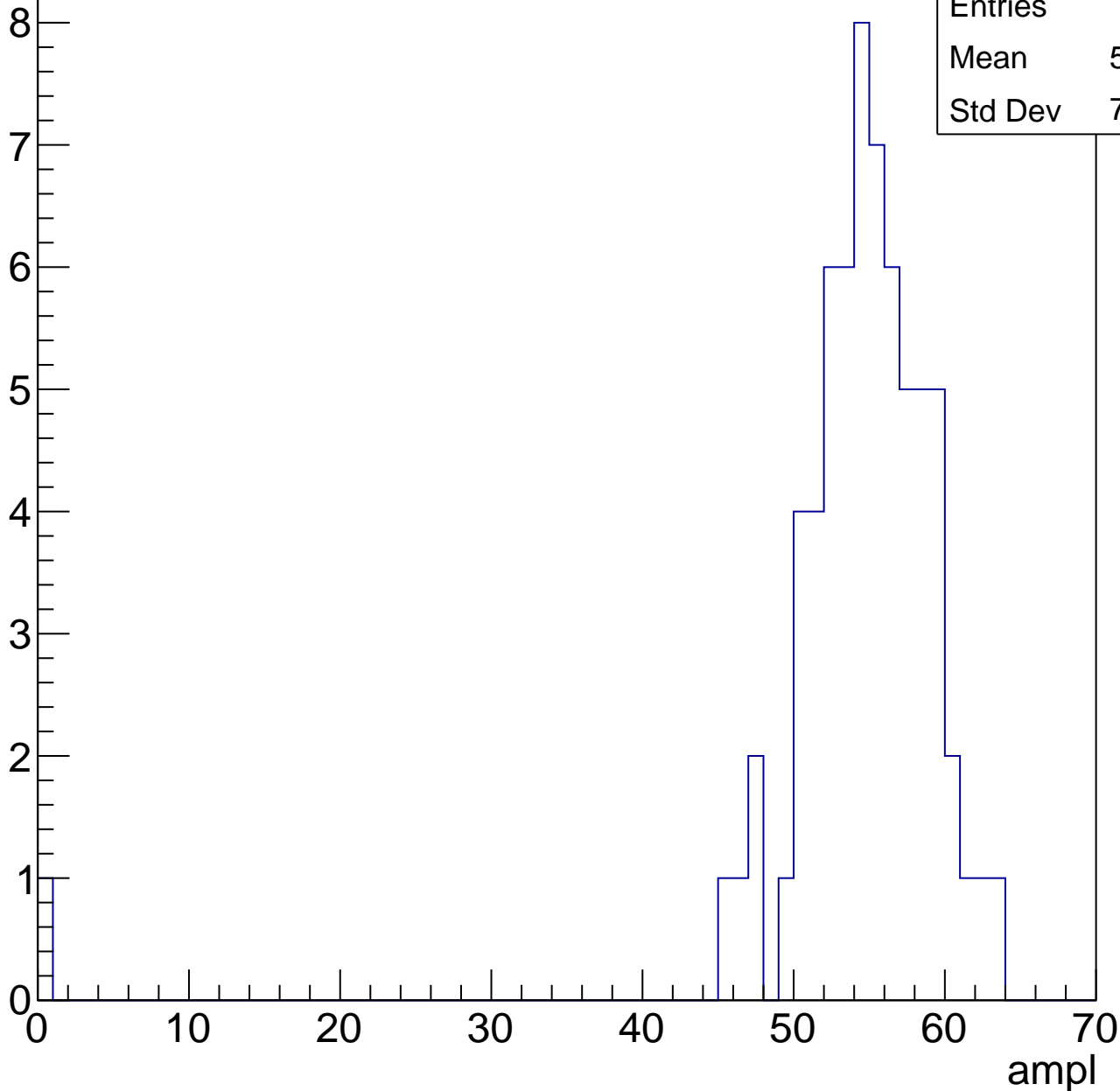
Entries	70
Mean	47.7
Std Dev	3.758

# B1L102S, U8-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	53.69
Std Dev	7.585

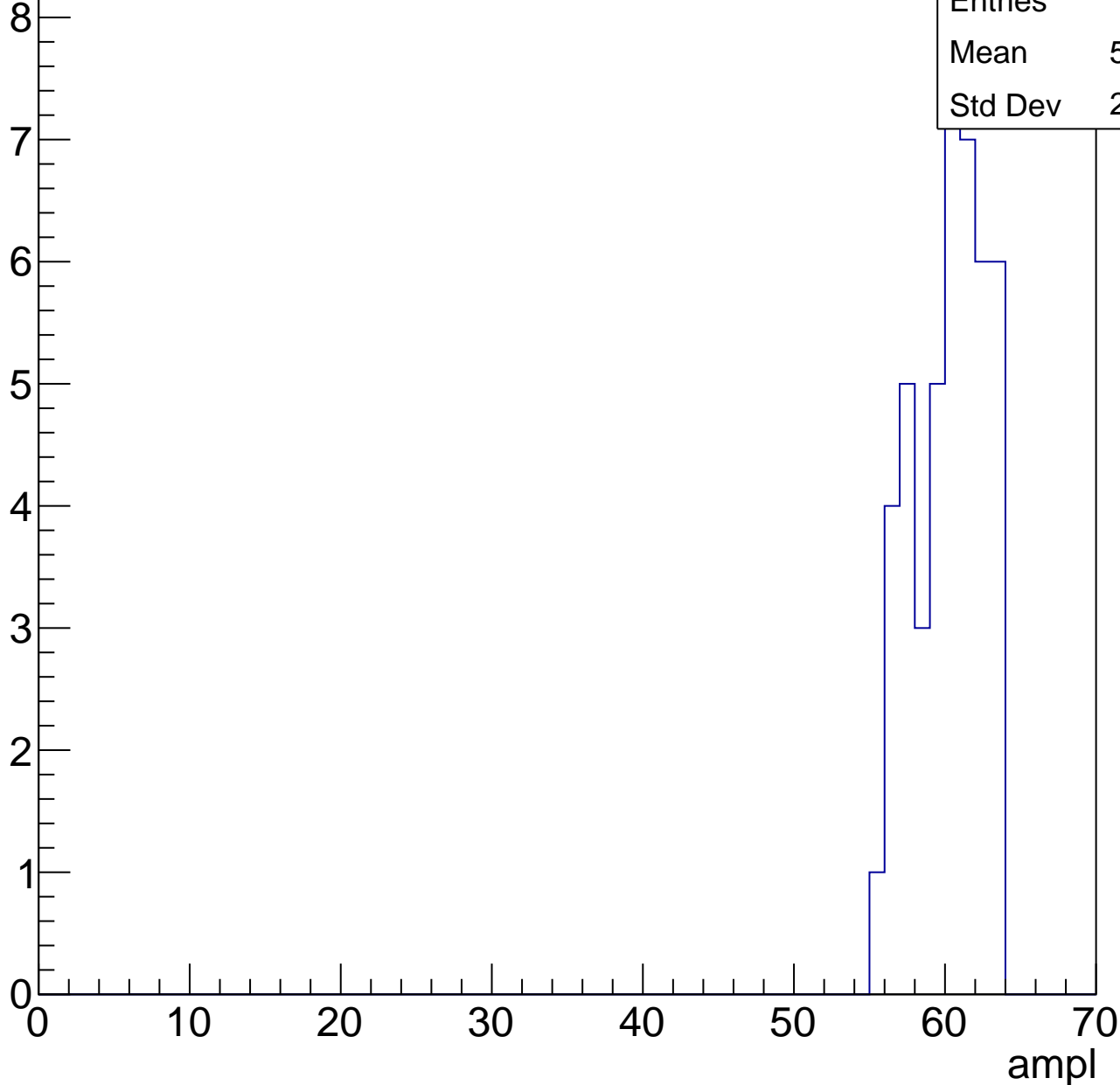


# B1L102S, U8-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

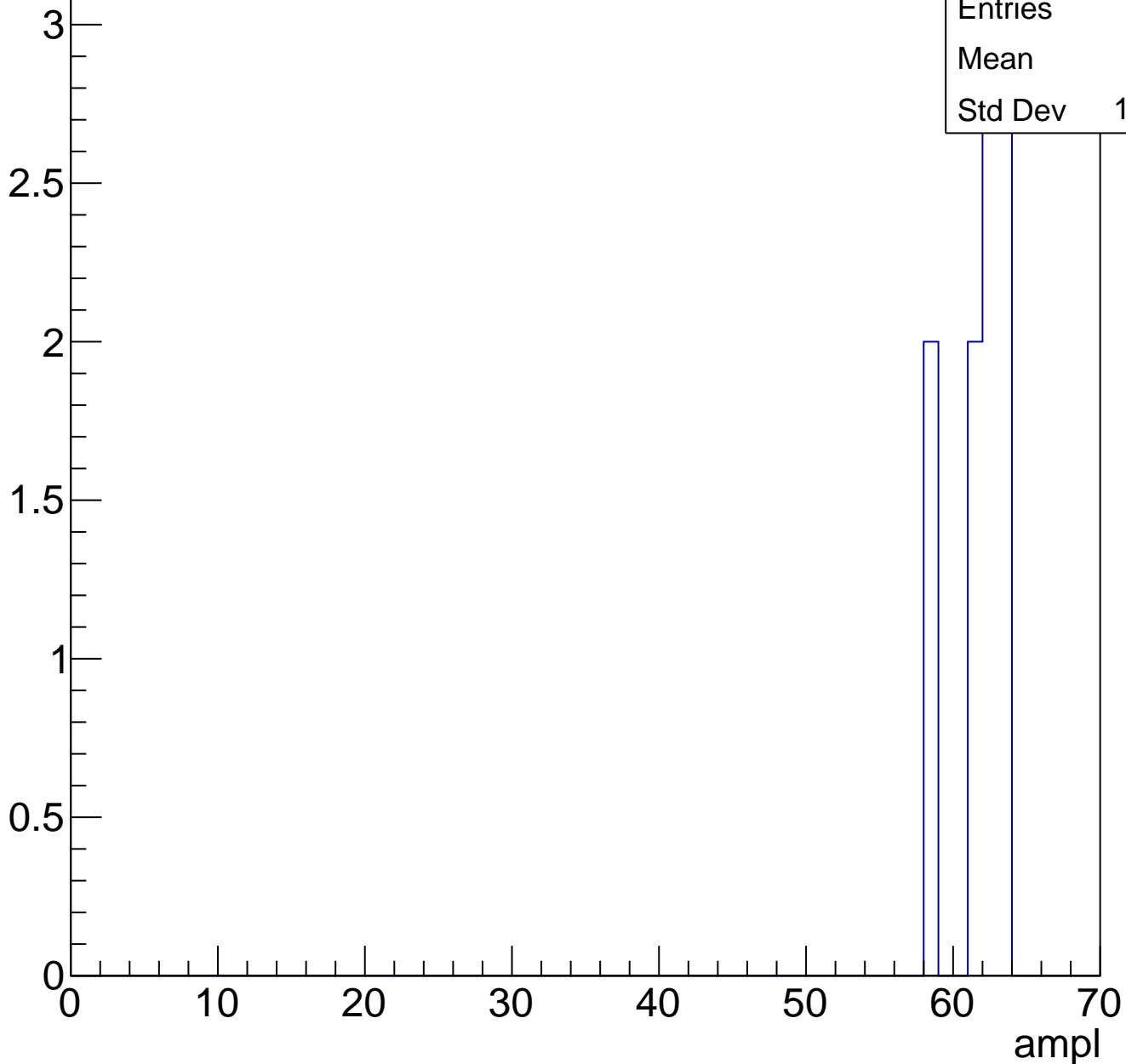
Entries	45
Mean	59.78
Std Dev	2.279



# B1L102S, U8-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U8-ch123, adc0

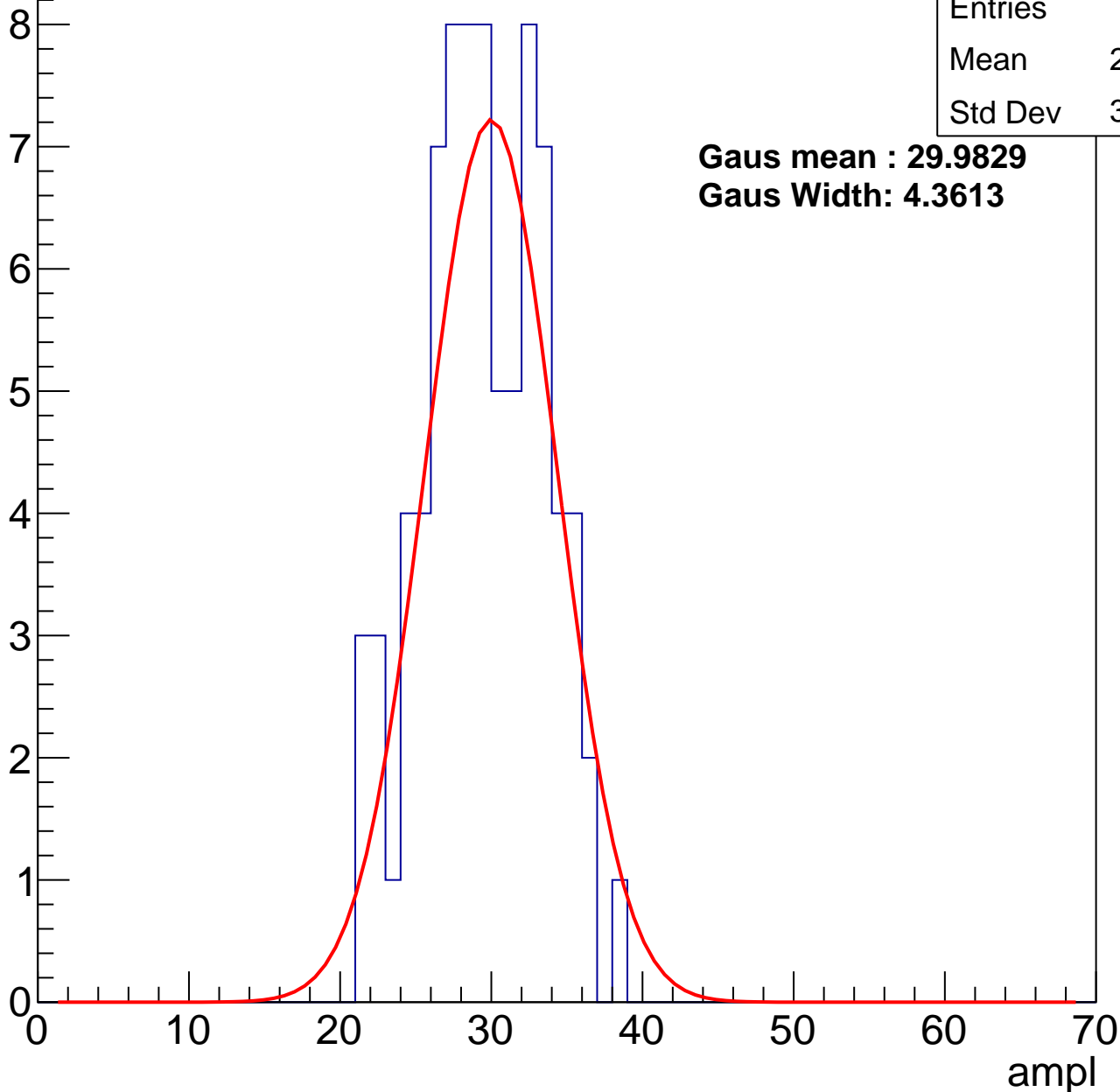
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	29.02
Std Dev	3.942

**Gaus mean : 29.9829**

**Gaus Width: 4.3613**



# B1L102S, U8-ch123, adc1

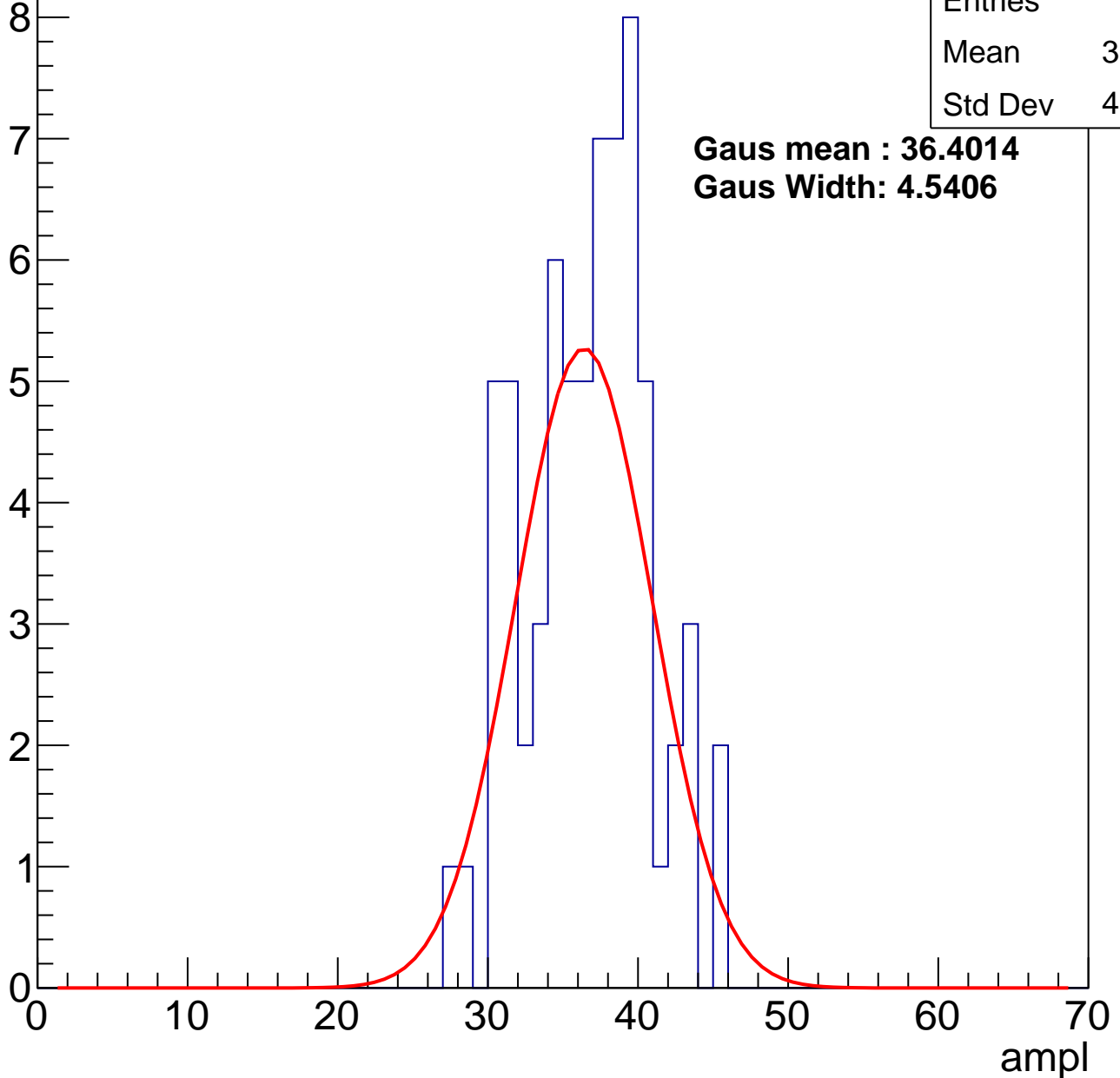
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	36.22
Std Dev	4.072

**Gaus mean : 36.4014**

**Gaus Width: 4.5406**



# B1L102S, U8-ch123, adc2

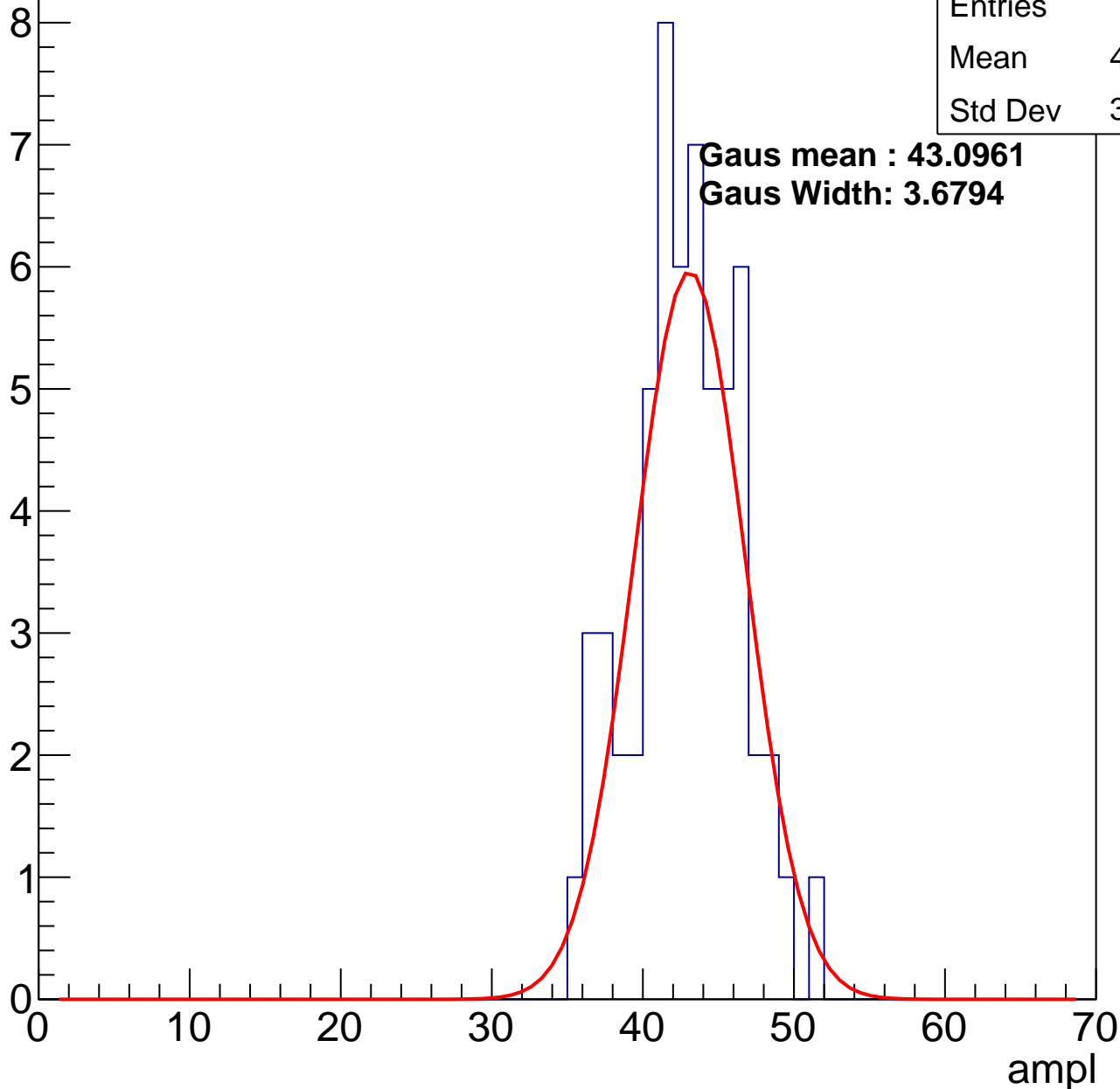
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	42.37
Std Dev	3.498

**Gaus mean : 43.0961**

**Gaus Width: 3.6794**

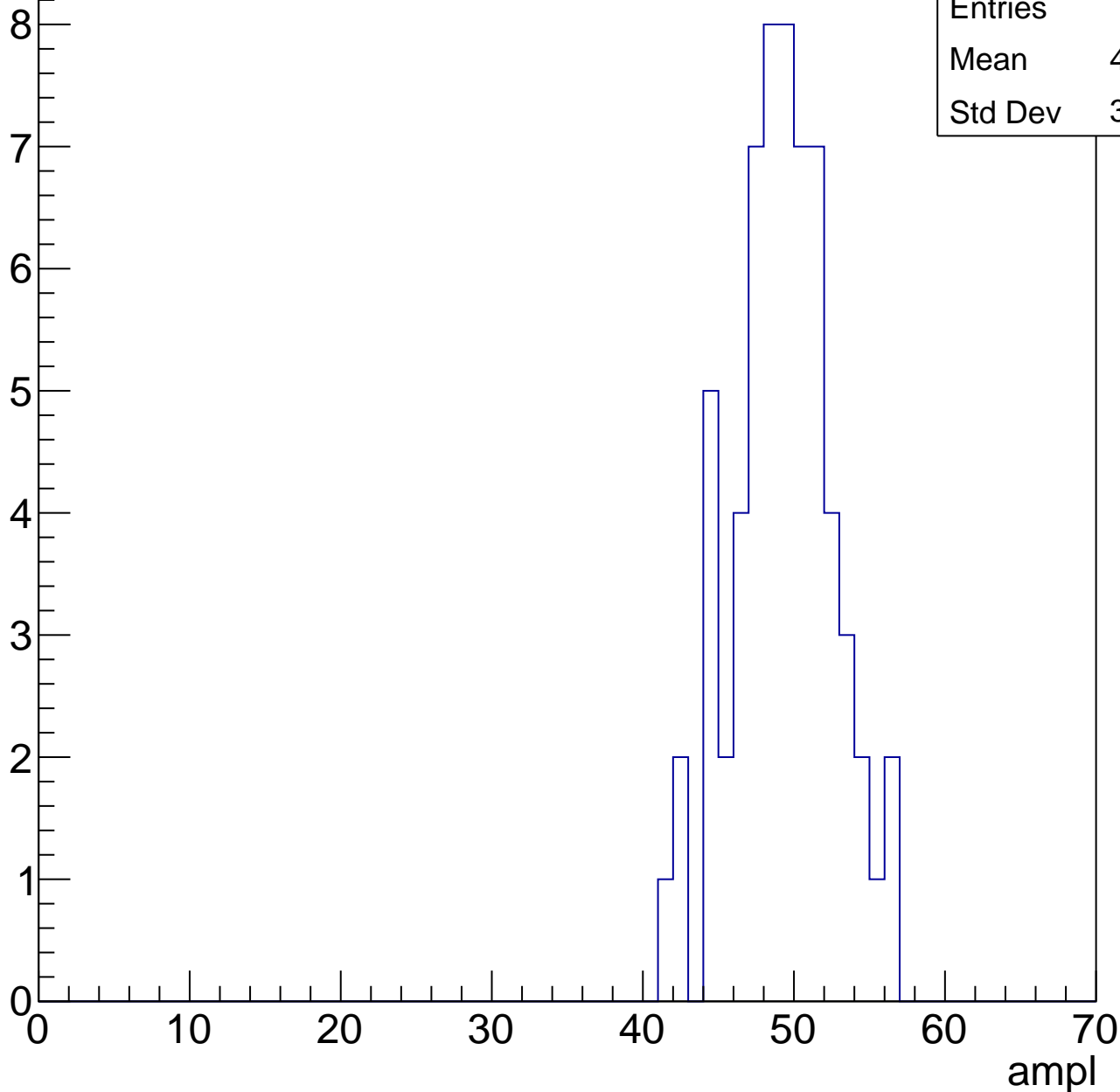


# B1L102S, U8-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

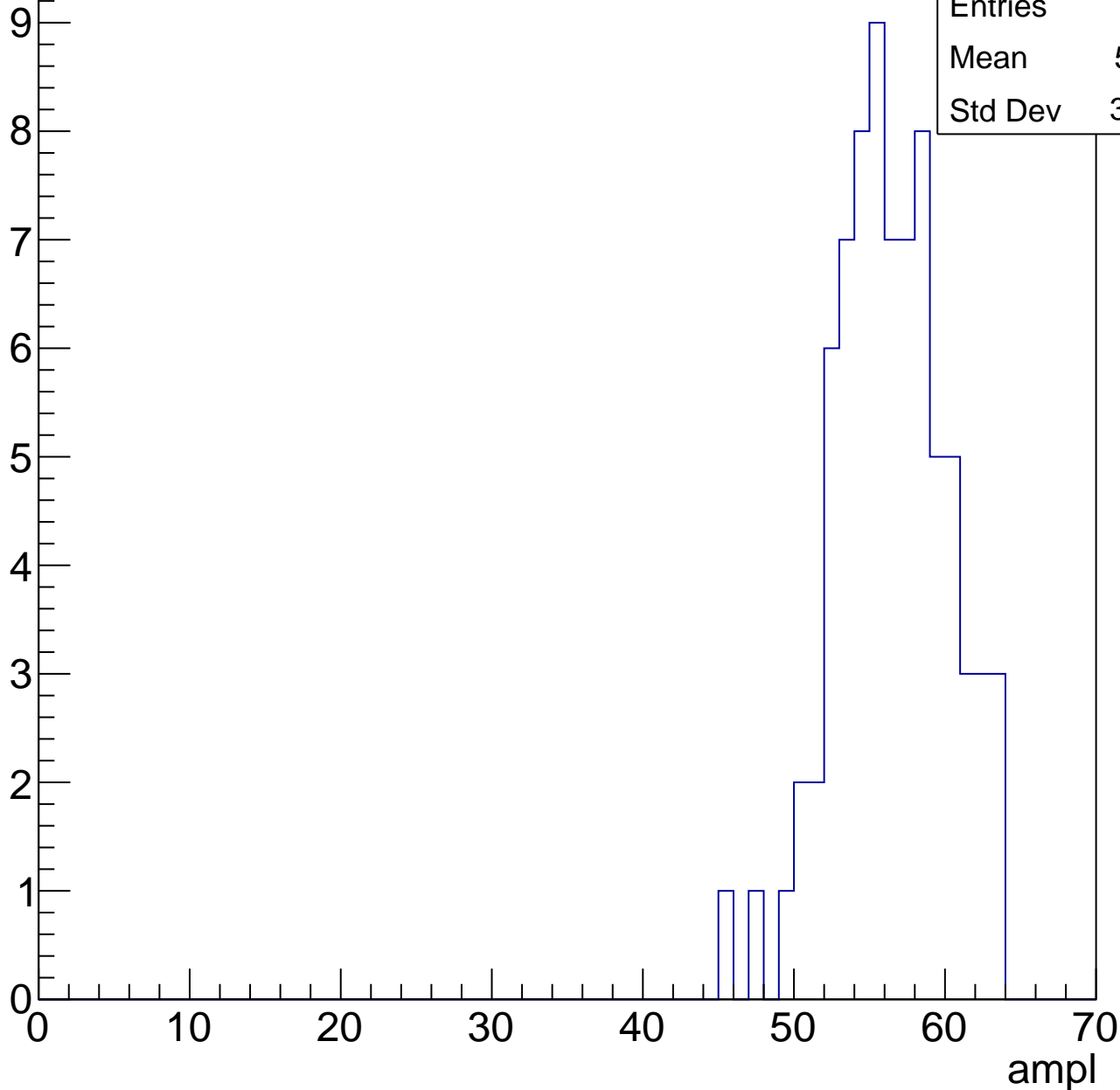
Entries	63
Mean	48.78
Std Dev	3.312



# B1L102S, U8-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



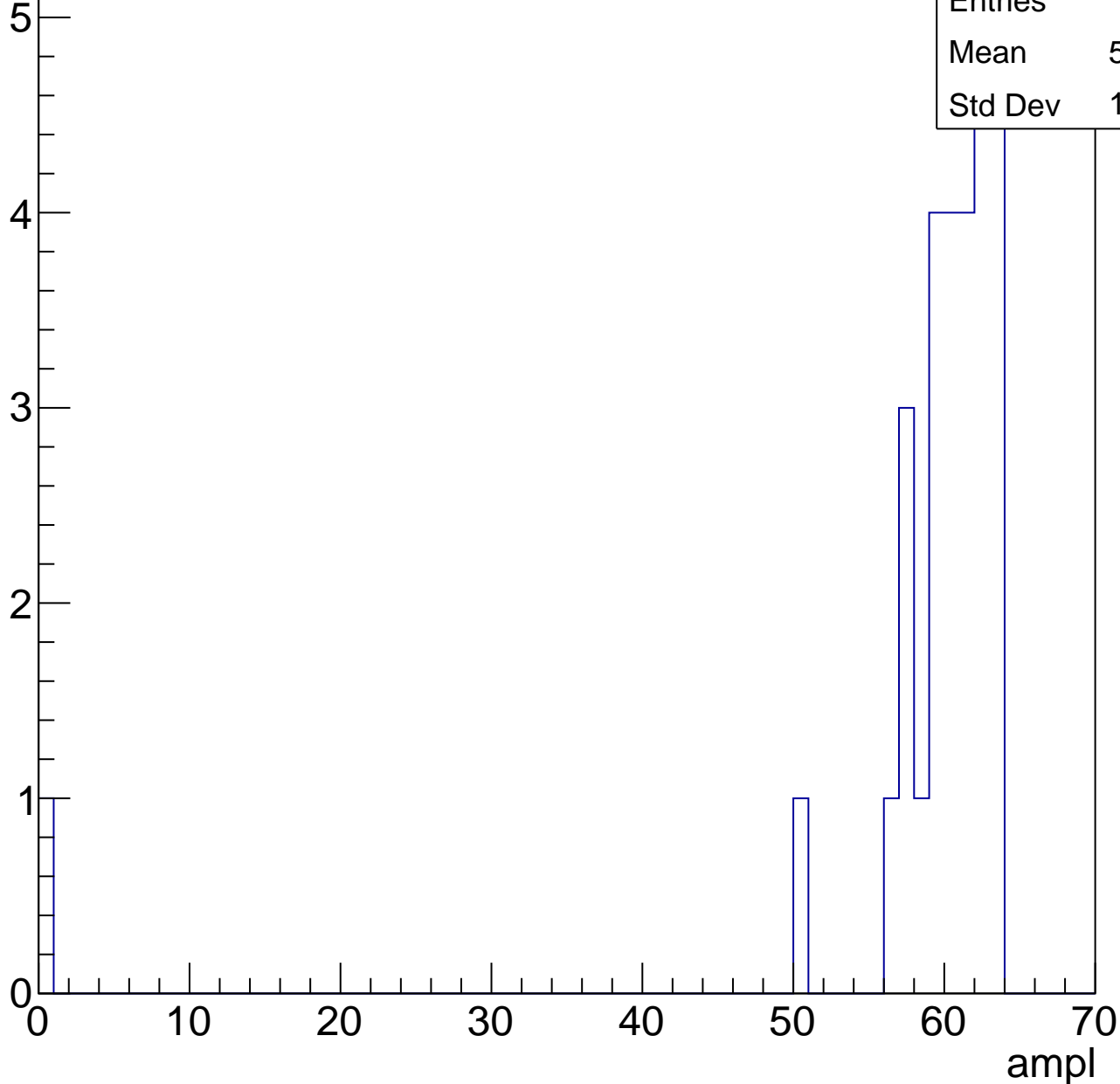
Entries	78
Mean	55.91
Std Dev	3.697

# B1L102S, U8-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	29
Mean	57.93
Std Dev	11.29



# B1L102S, U8-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

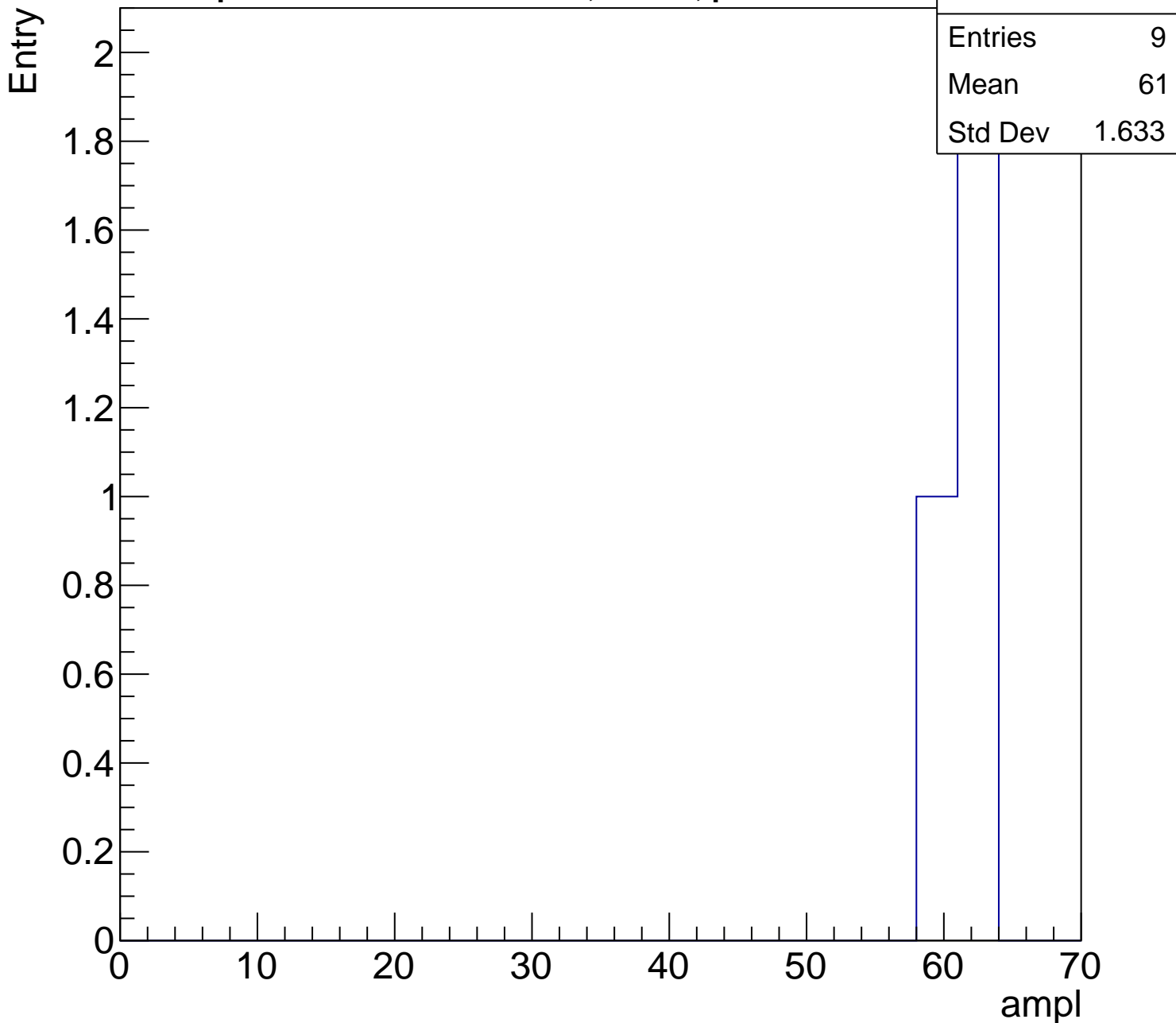
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	9
Mean	61
Std Dev	1.633

ampl

0 10 20 30 40 50 60 70





# B1L102S, U8-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U8-ch124, adc0

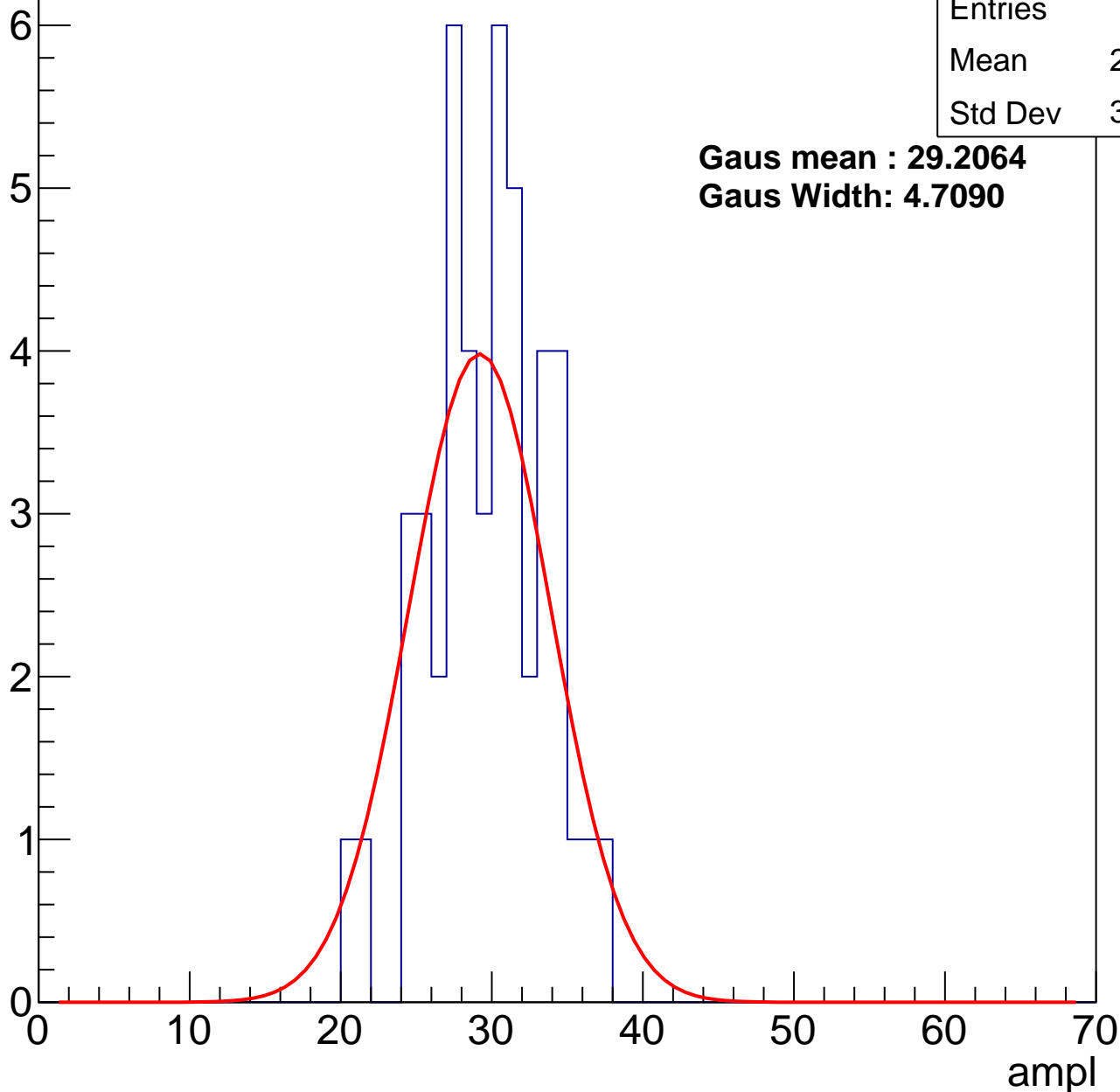
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	29.28
Std Dev	3.768

**Gaus mean : 29.2064**

**Gaus Width: 4.7090**



# B1L102S, U8-ch124, adc1

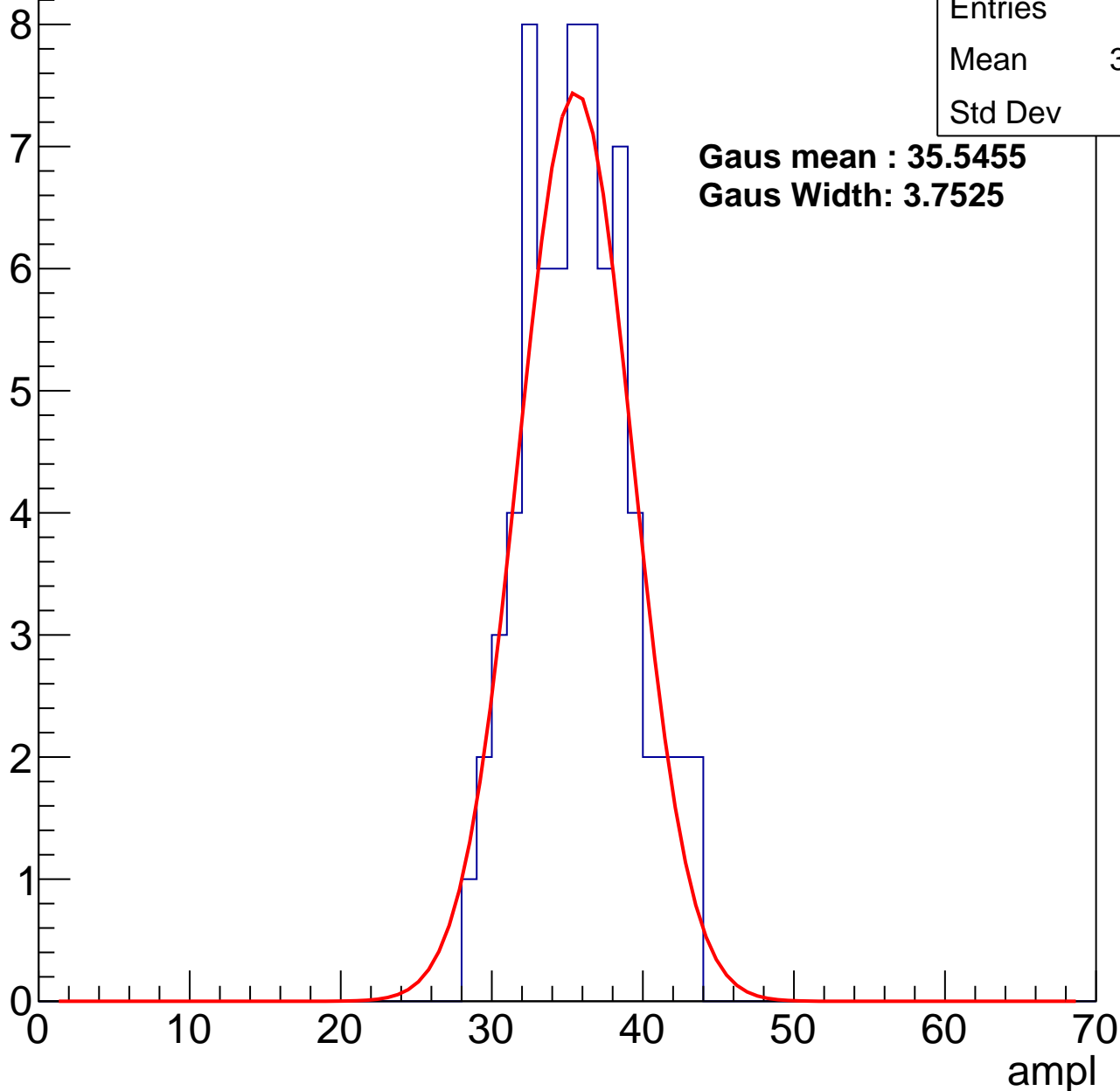
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	35.24
Std Dev	3.49

**Gaus mean : 35.5455**

**Gaus Width: 3.7525**



# B1L102S, U8-ch124, adc2

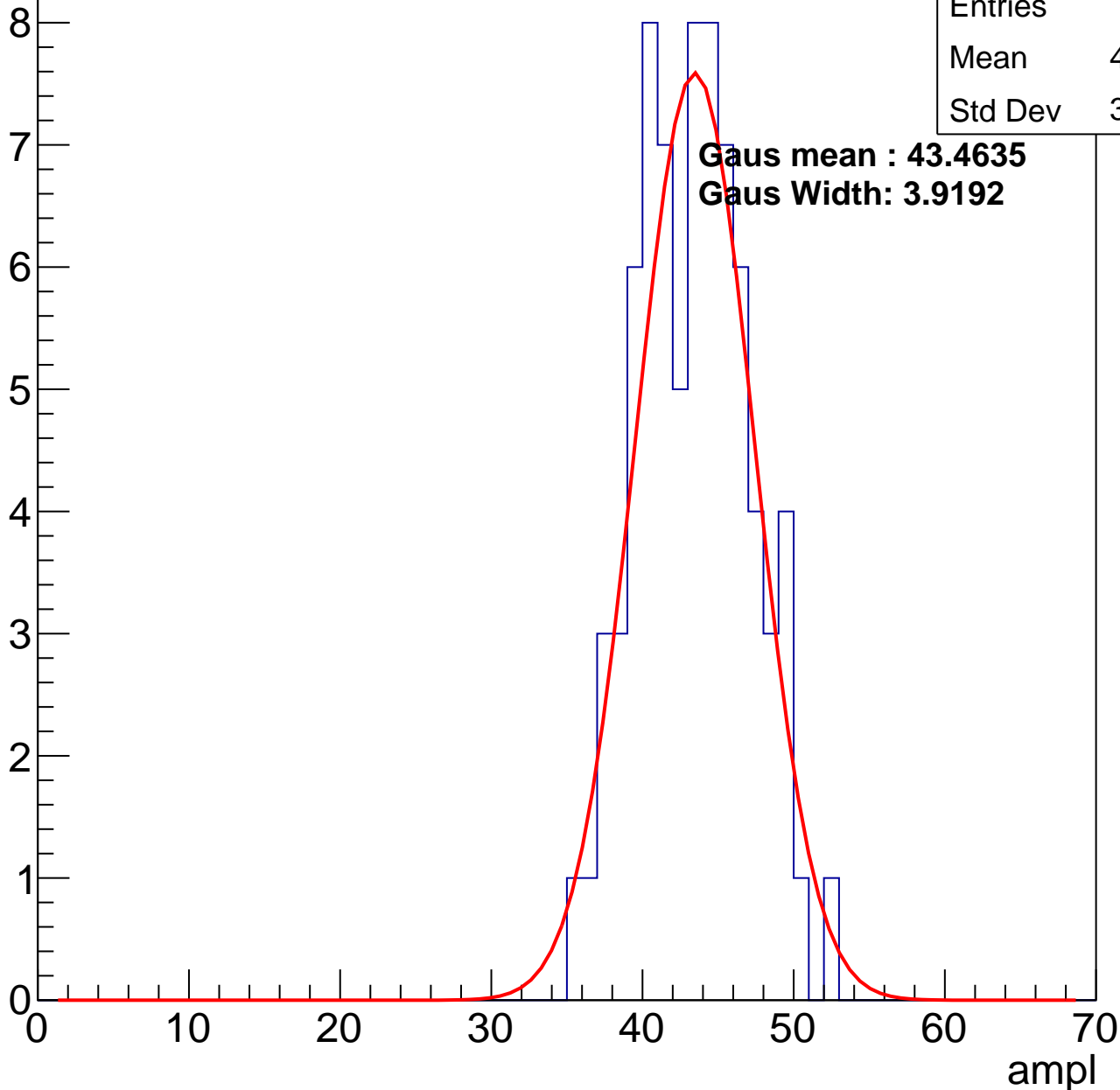
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	42.95
Std Dev	3.627

**Gaus mean : 43.4635**

**Gaus Width: 3.9192**

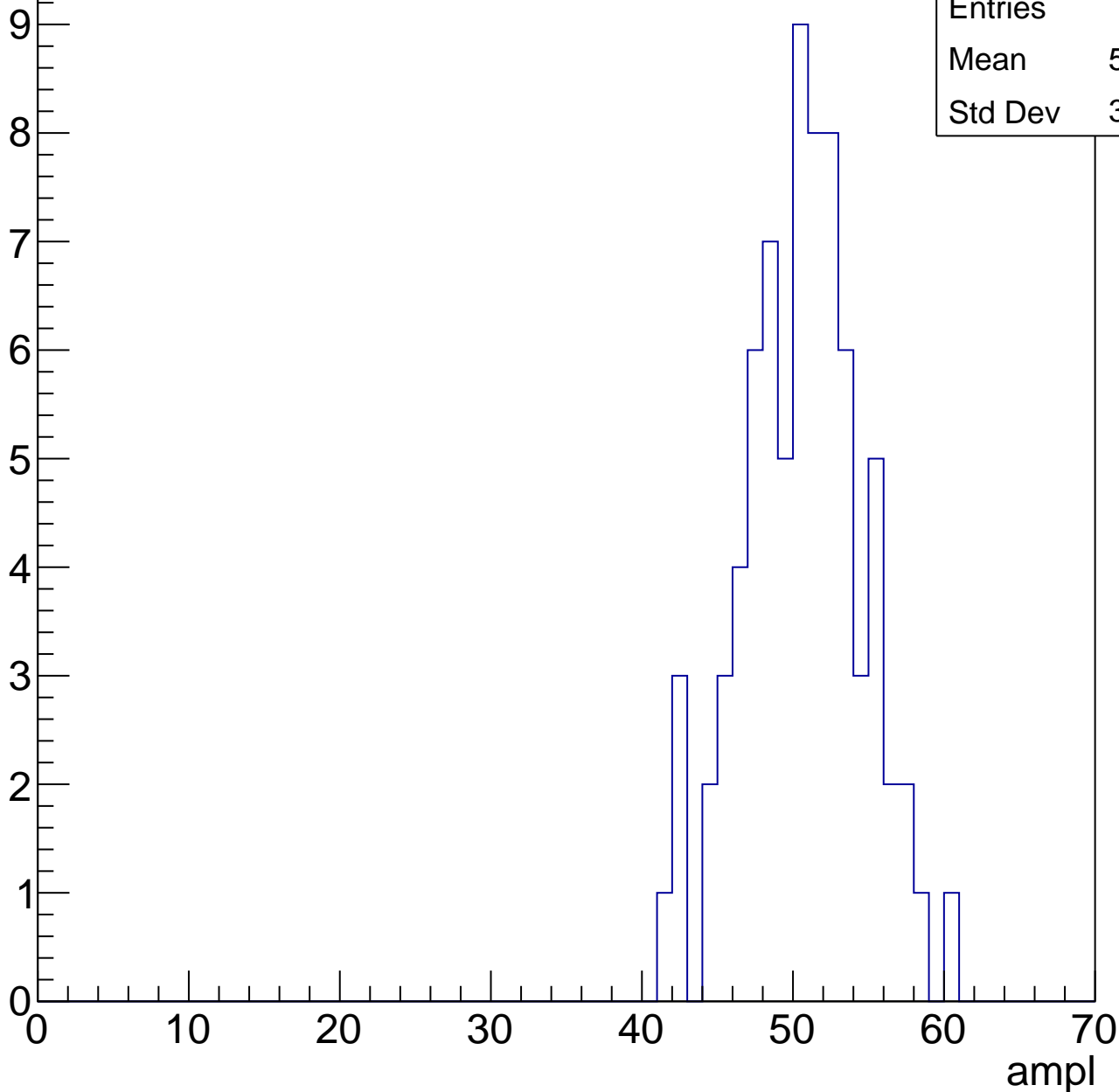


# B1L102S, U8-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	50.13
Std Dev	3.925

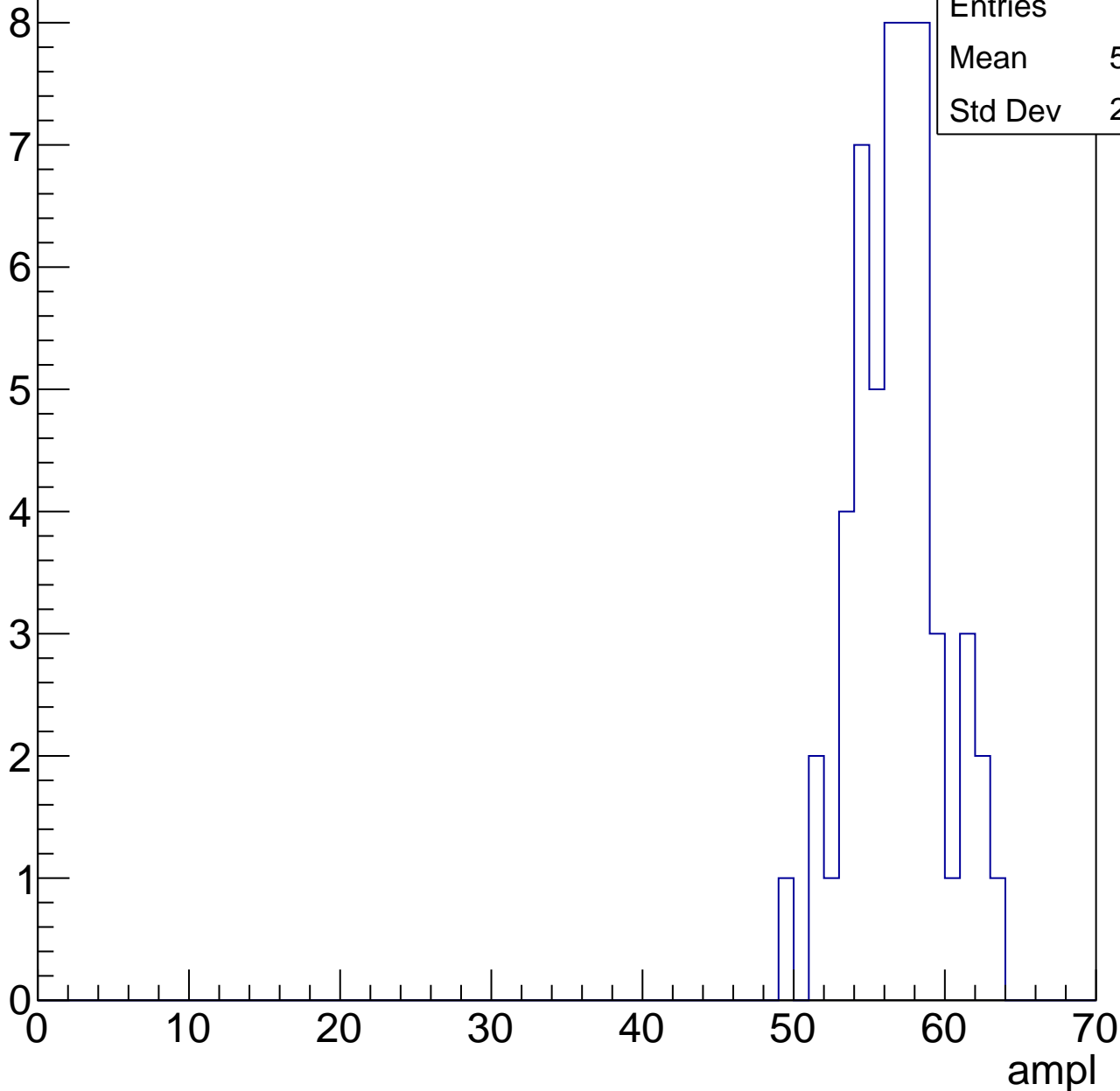


# B1L102S, U8-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

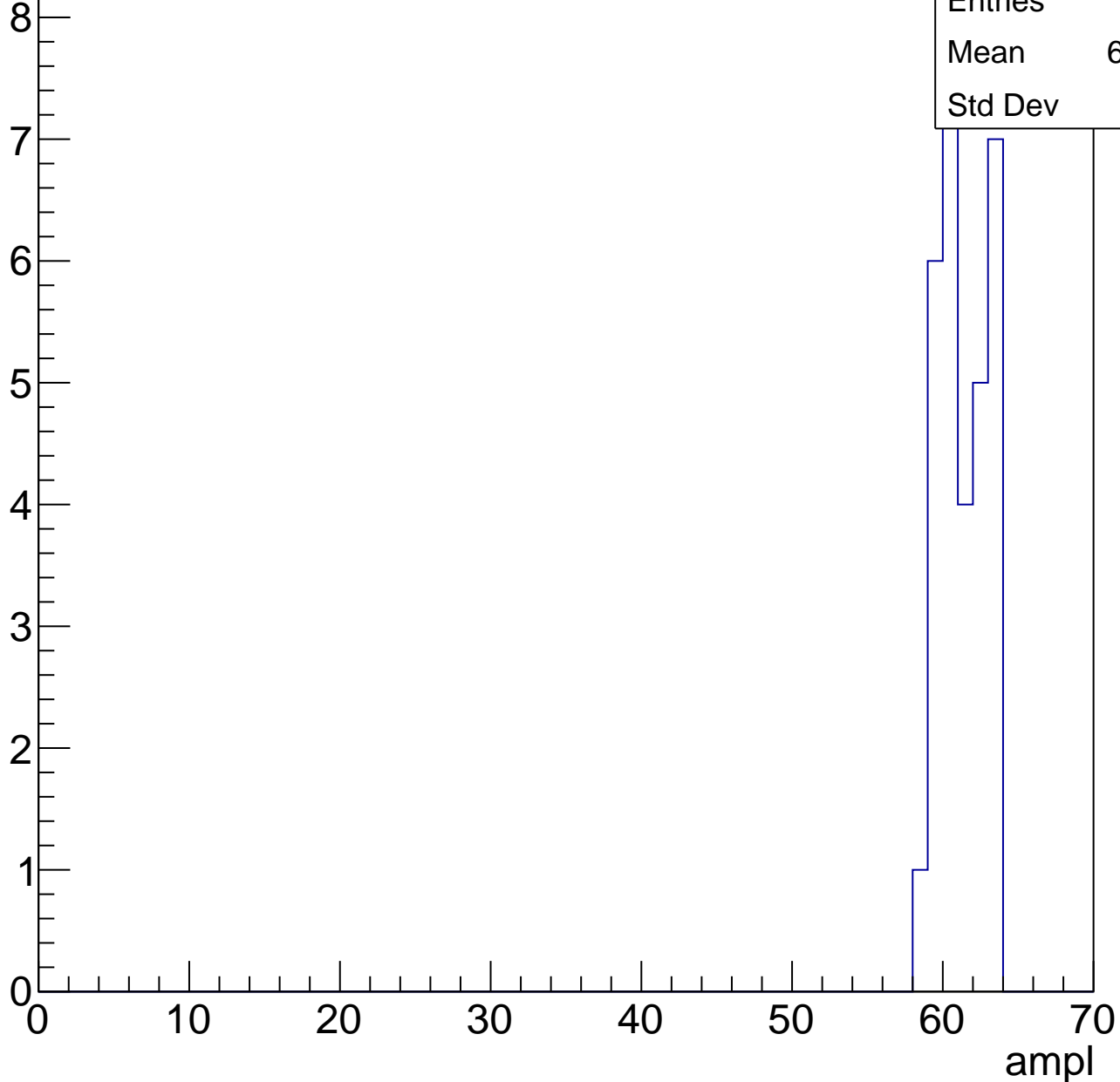
Entries	54
Mean	56.35
Std Dev	2.907



# B1L102S, U8-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

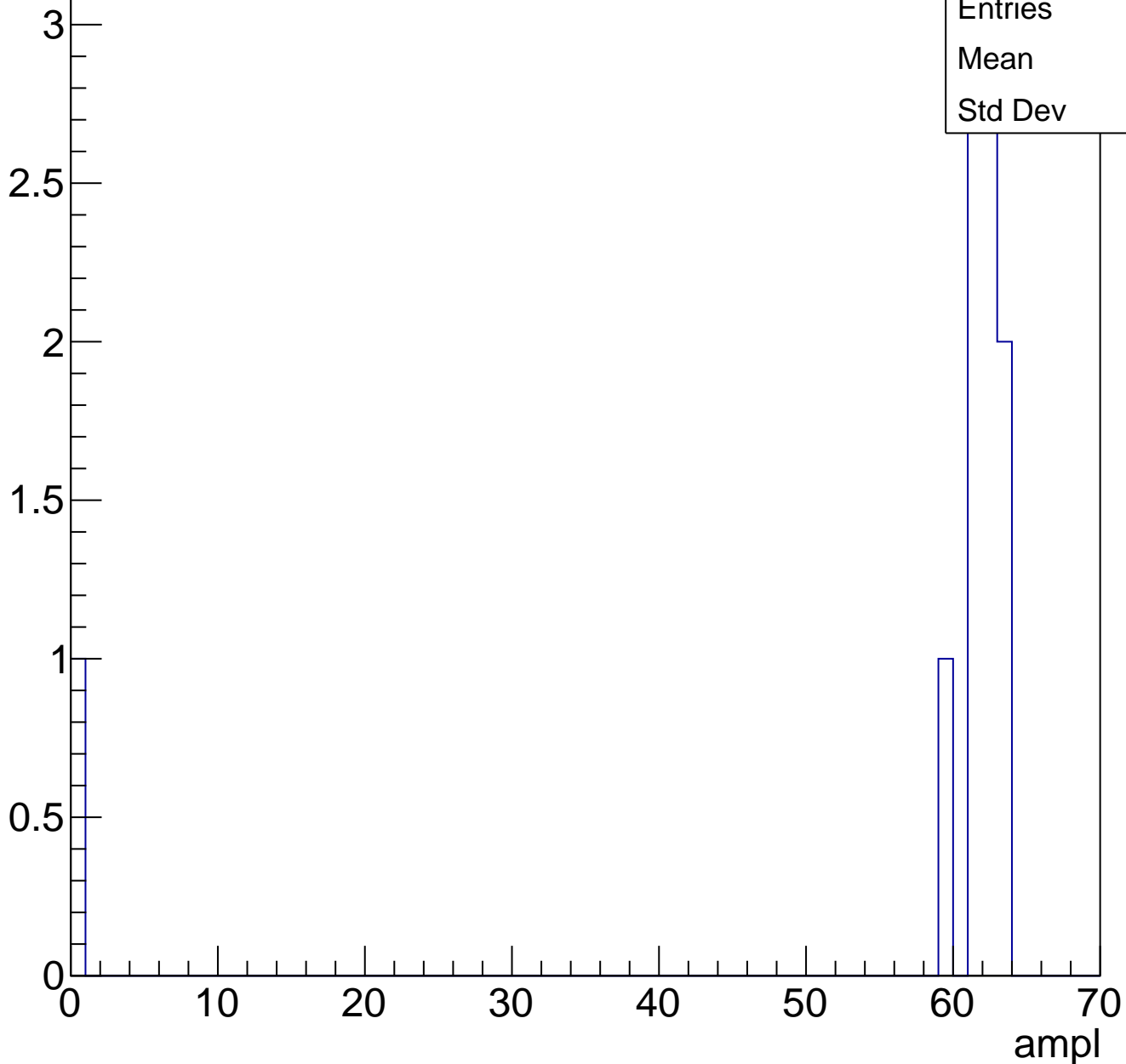
Entry



# B1L102S, U8-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U8-ch125, adc0

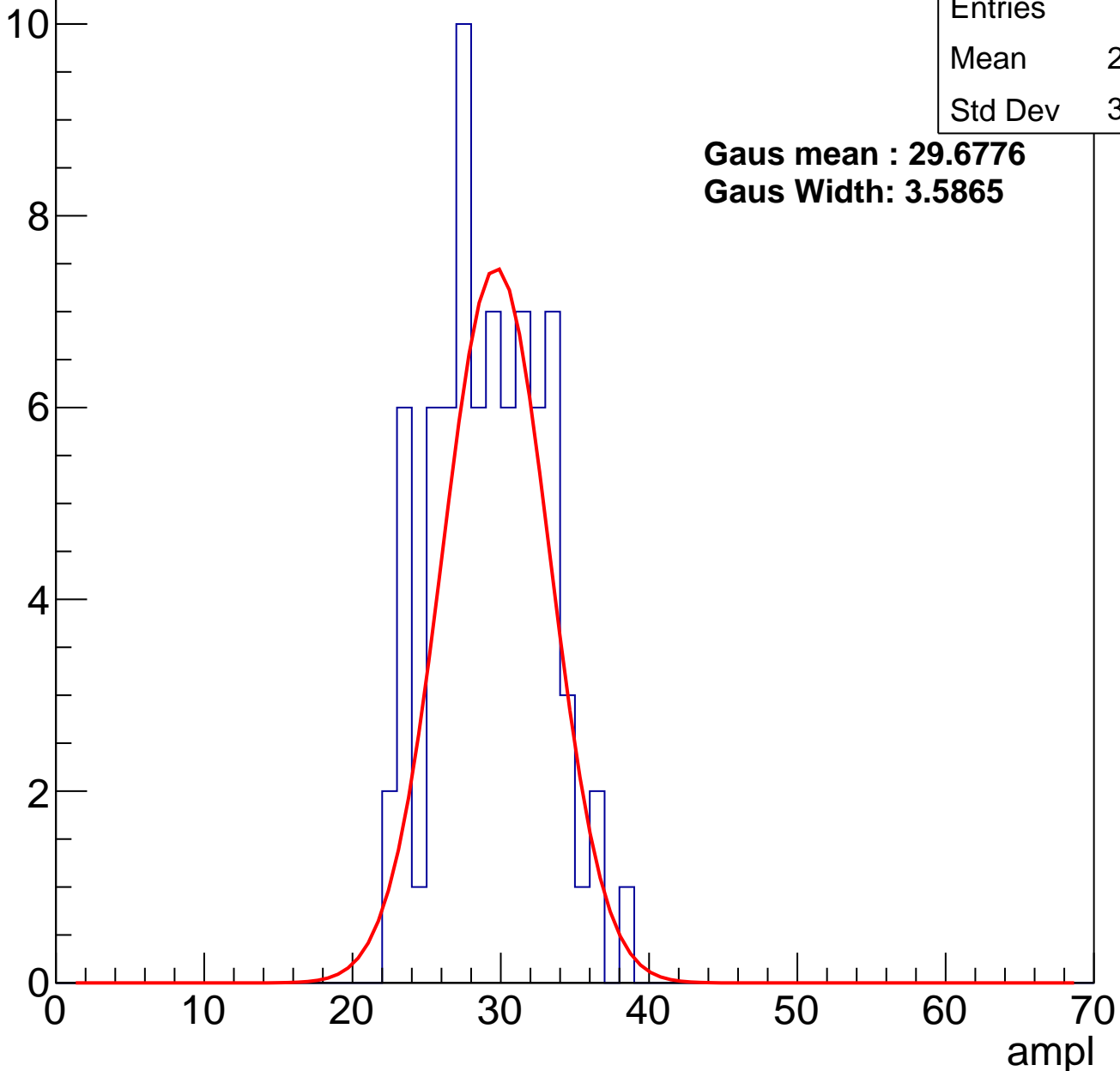
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	77
Mean	28.83
Std Dev	3.645

**Gaus mean : 29.6776**

**Gaus Width: 3.5865**

Entry



# B1L102S, U8-ch125, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	74
Mean	36.47
Std Dev	3.422

**Gaus mean : 37.1470**

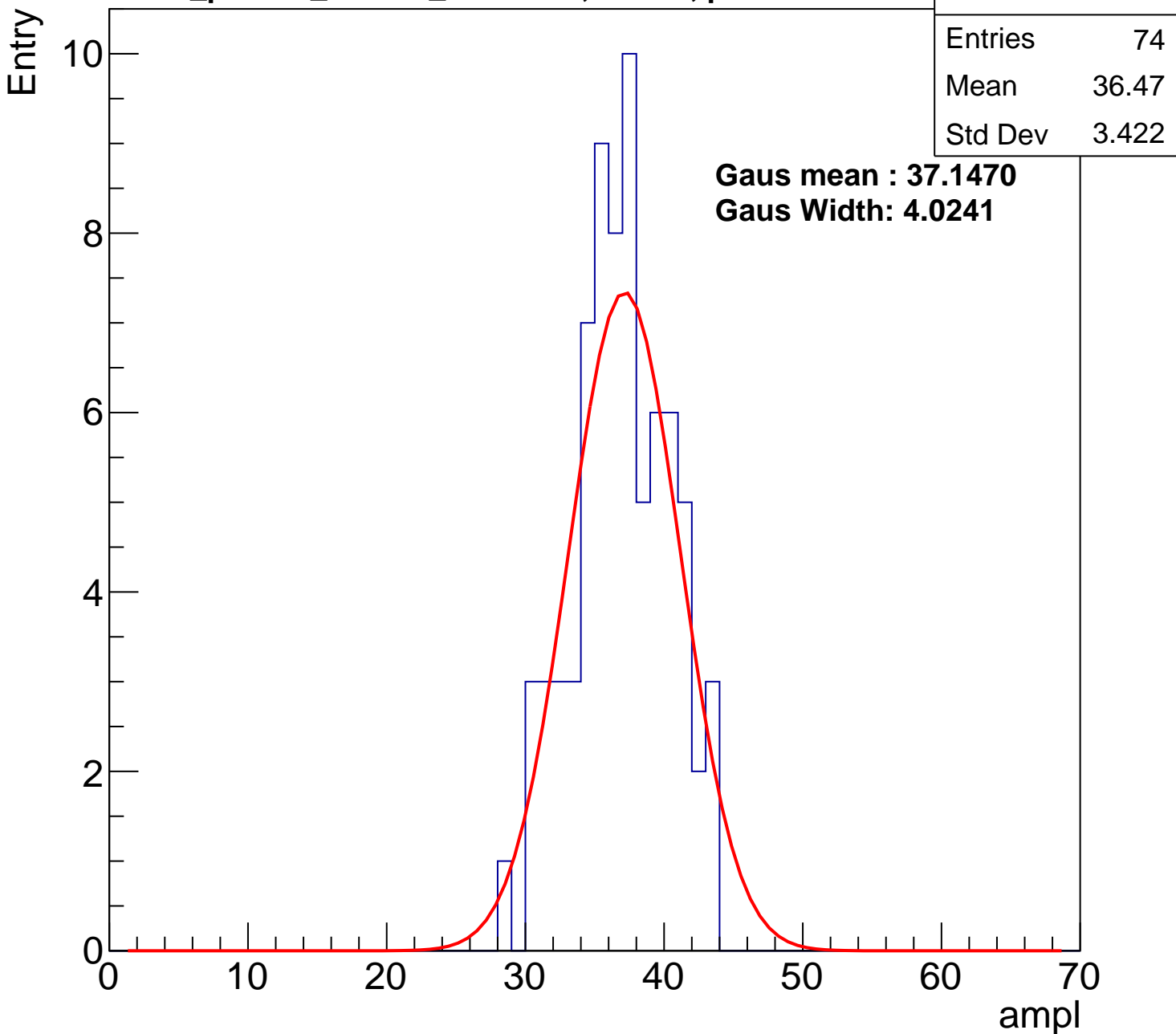
**Gaus Width: 4.0241**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U8-ch125, adc2

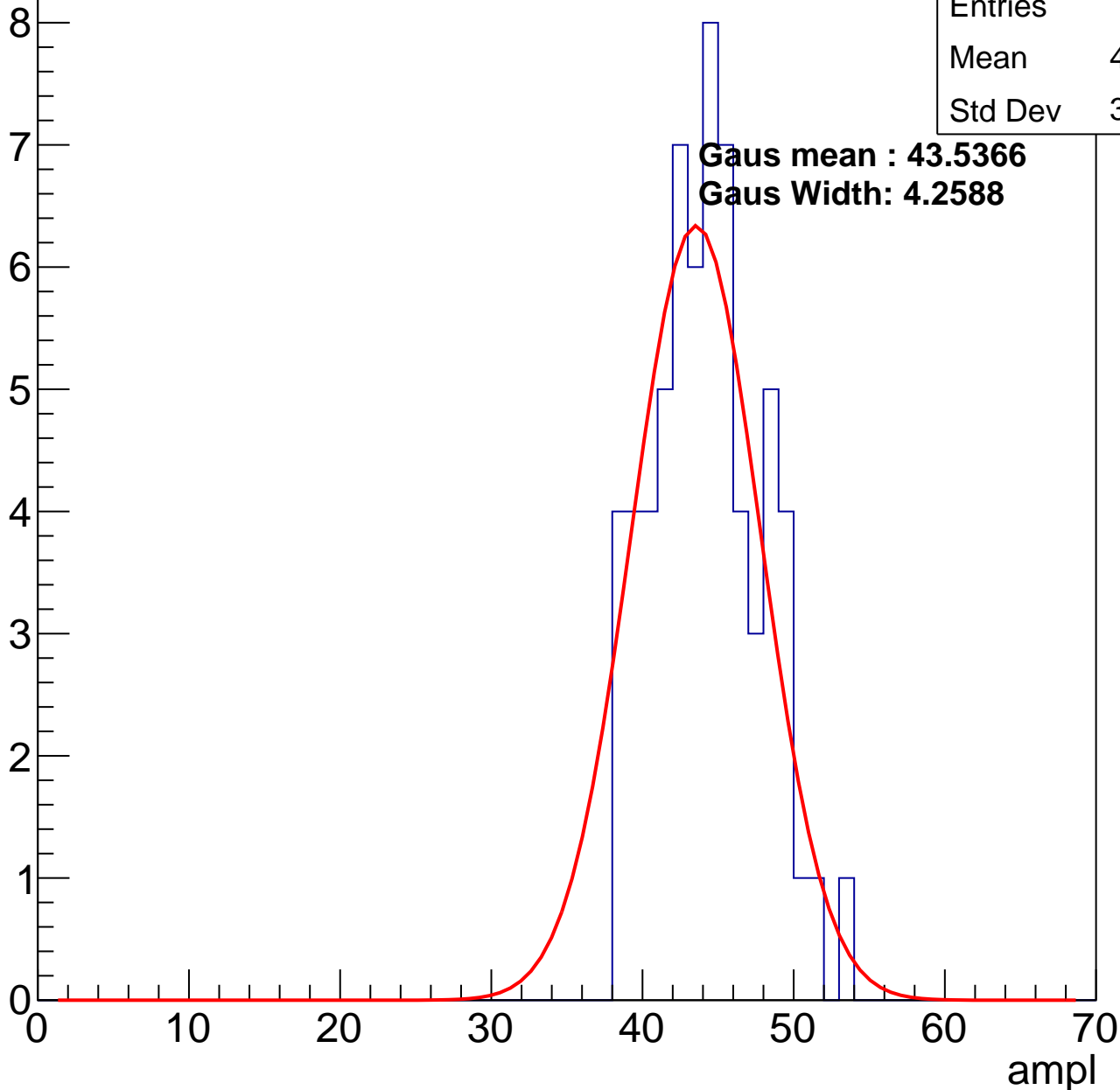
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	43.86
Std Dev	3.495

**Gaus mean : 43.5366**

**Gaus Width: 4.2588**

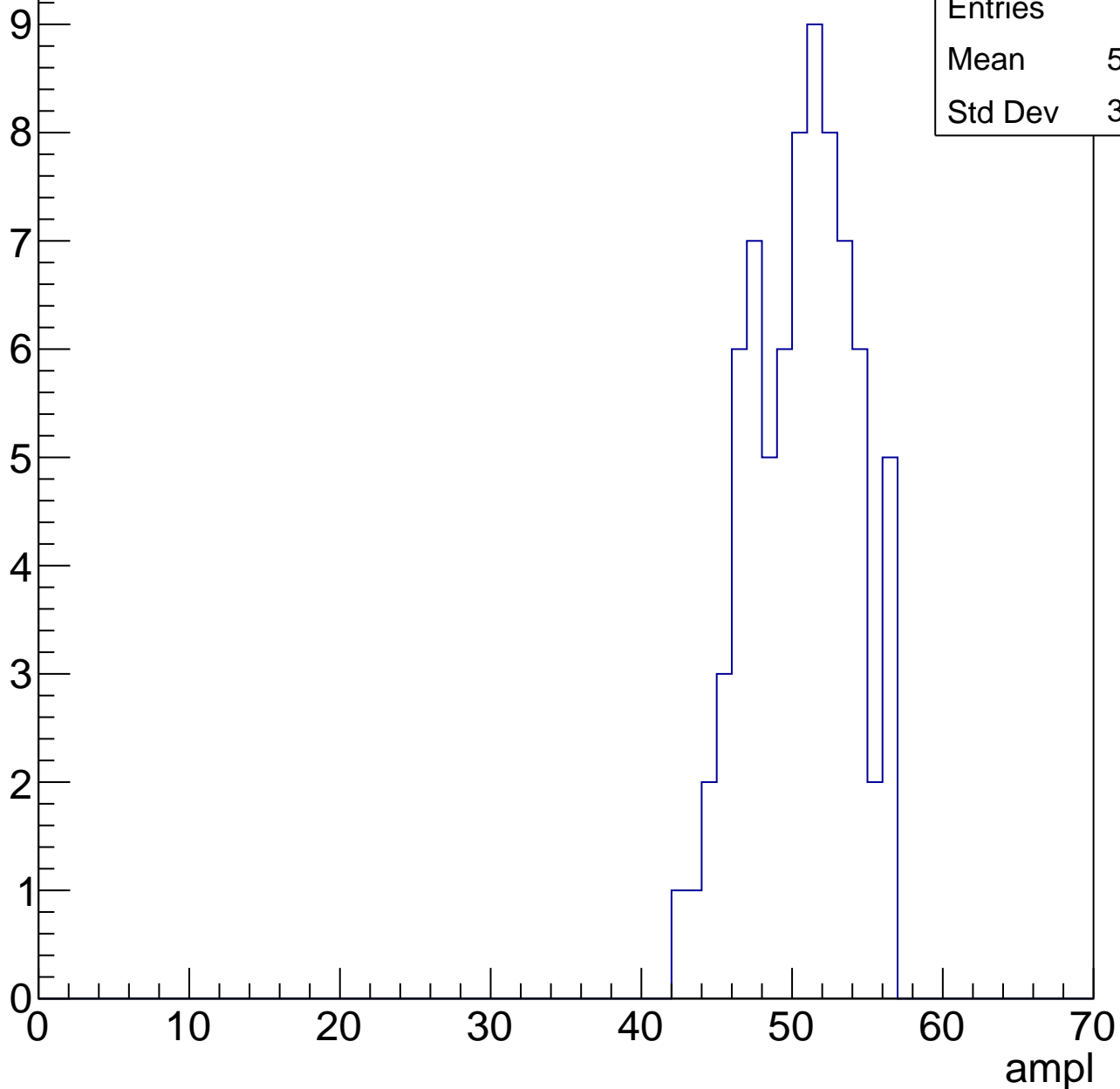


# B1L102S, U8-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	50.09
Std Dev	3.392

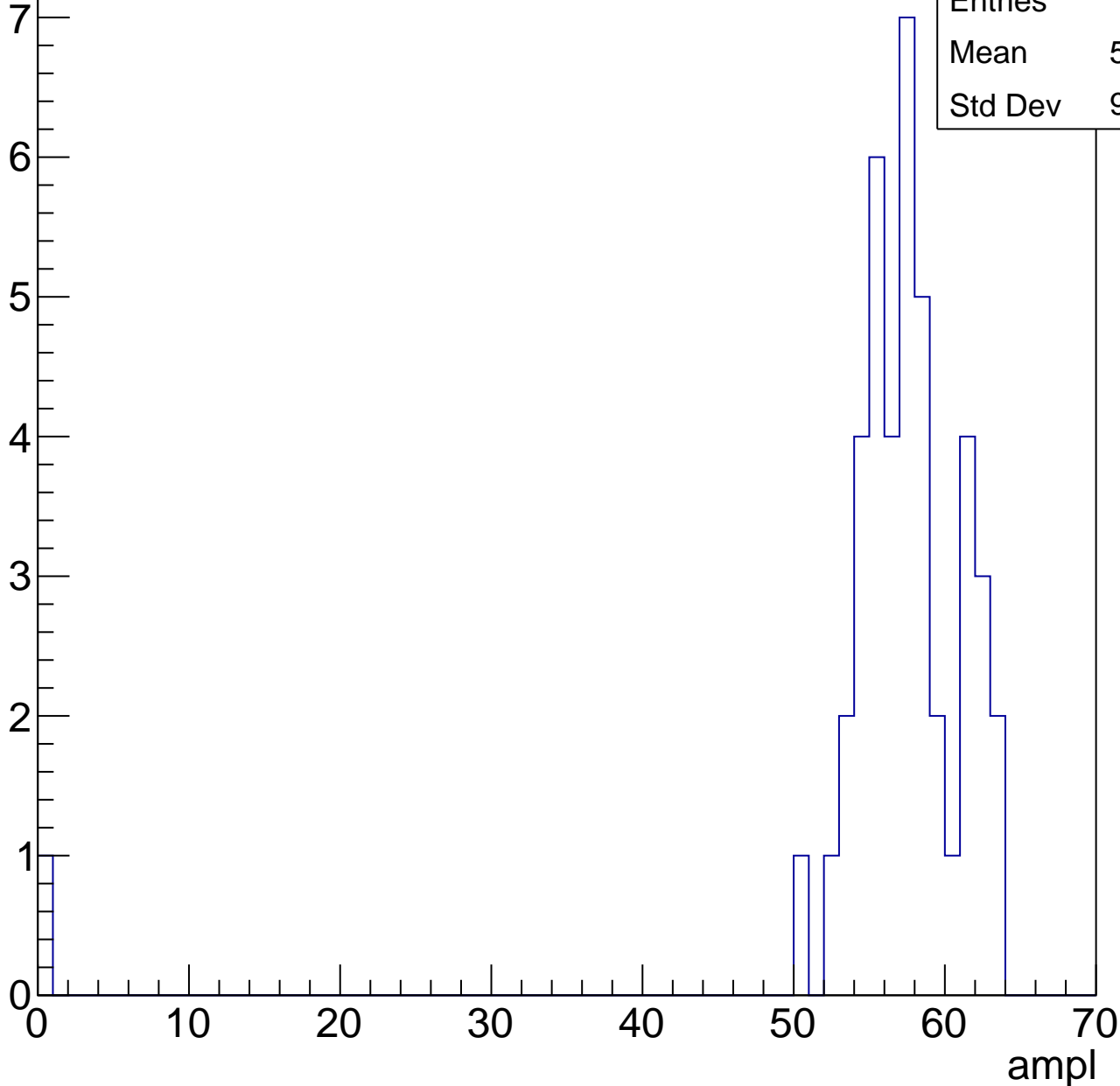


# B1L102S, U8-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	43
Mean	55.84
Std Dev	9.142

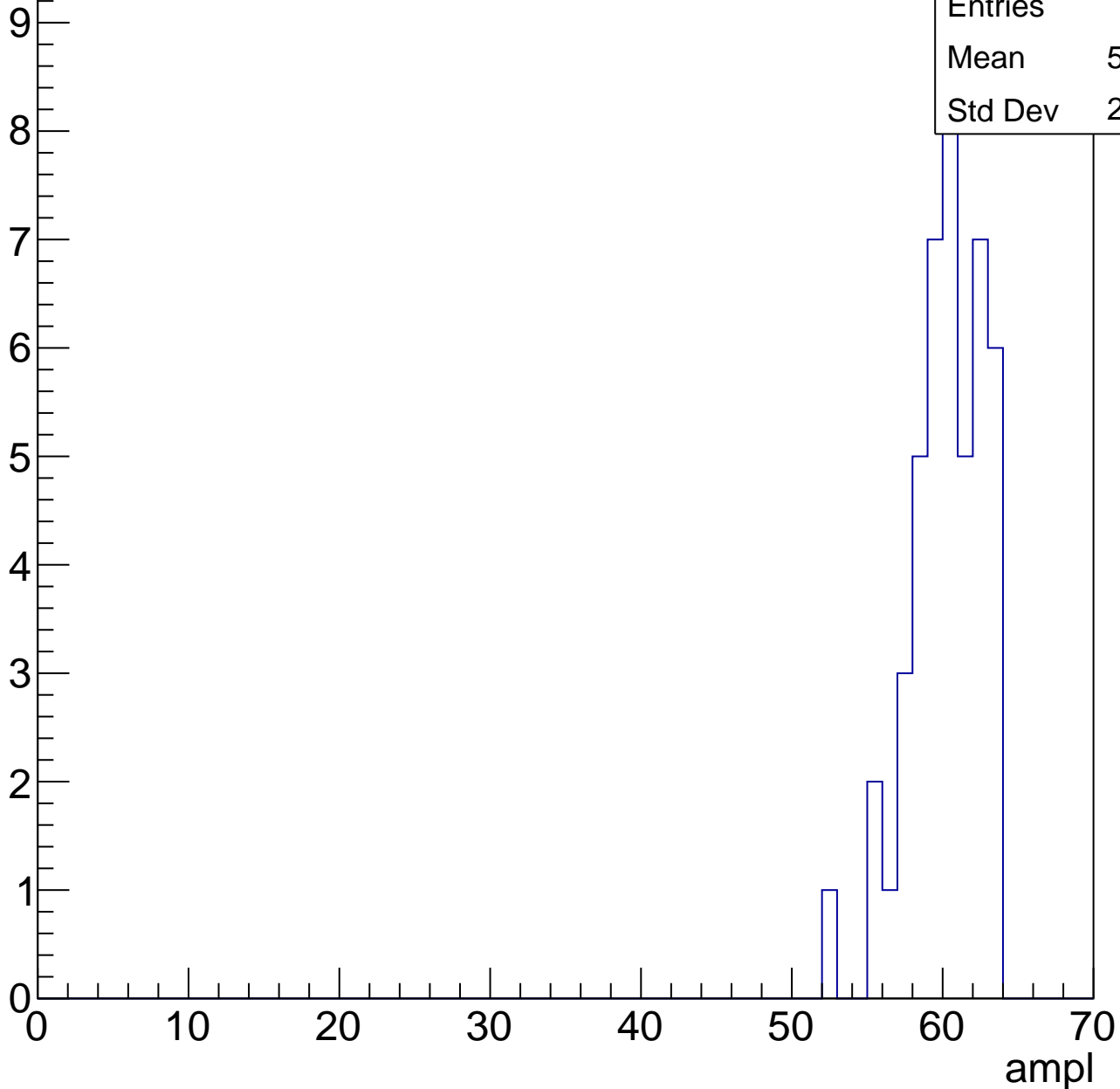


# B1L102S, U8-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

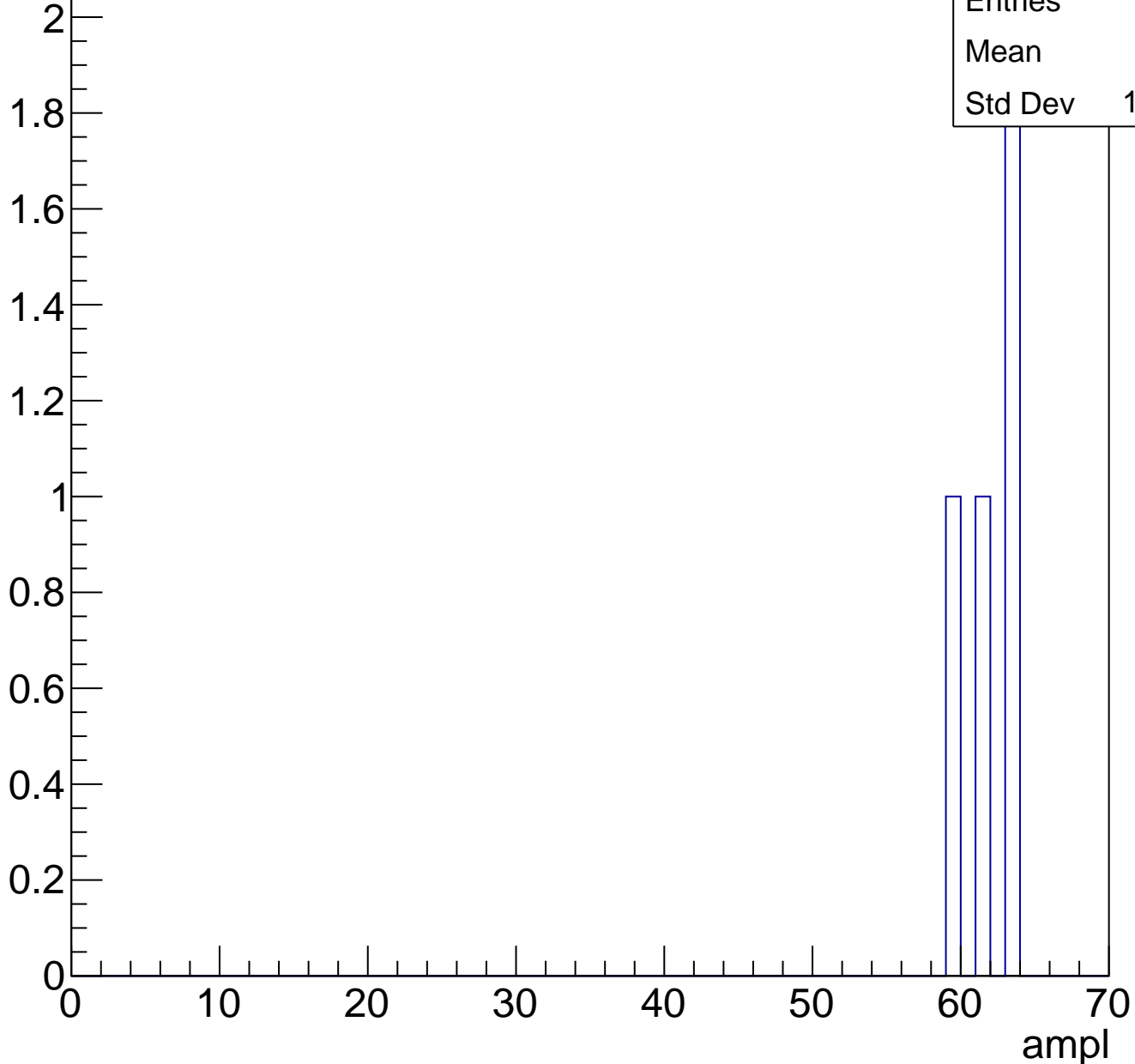
Entries	46
Mean	59.76
Std Dev	2.415



# B1L102S, U8-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	4
Mean	61.5
Std Dev	1.658



# B1L102S, U8-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	6.333
Std Dev	8.957

# B1L102S, U8-ch126, adc0

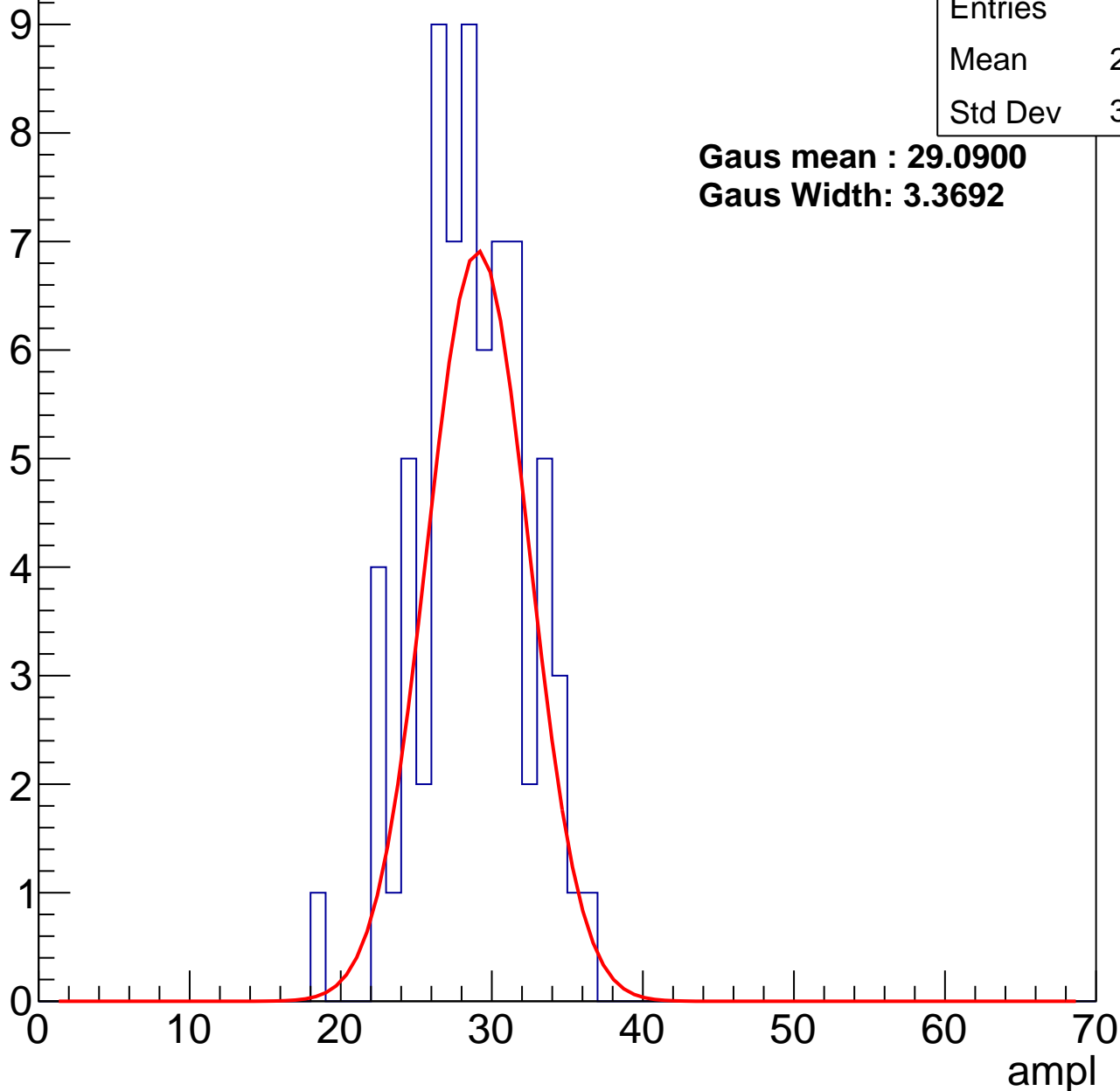
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	28.24
Std Dev	3.547

**Gaus mean : 29.0900**

**Gaus Width: 3.3692**



# B1L102S, U8-ch126, adc1

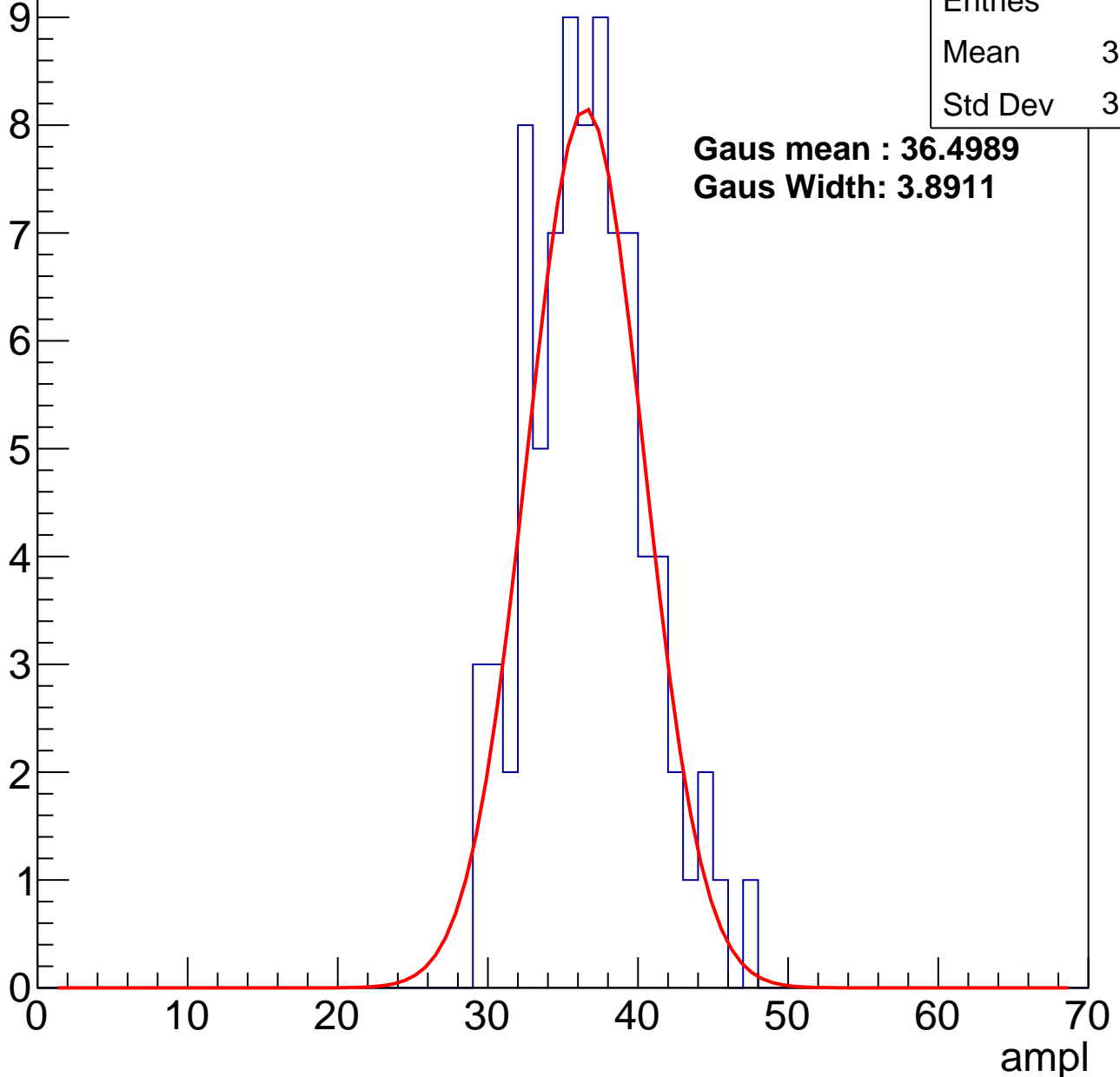
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	83
Mean	36.19
Std Dev	3.845

**Gaus mean : 36.4989**

**Gaus Width: 3.8911**



# B1L102S, U8-ch126, adc2

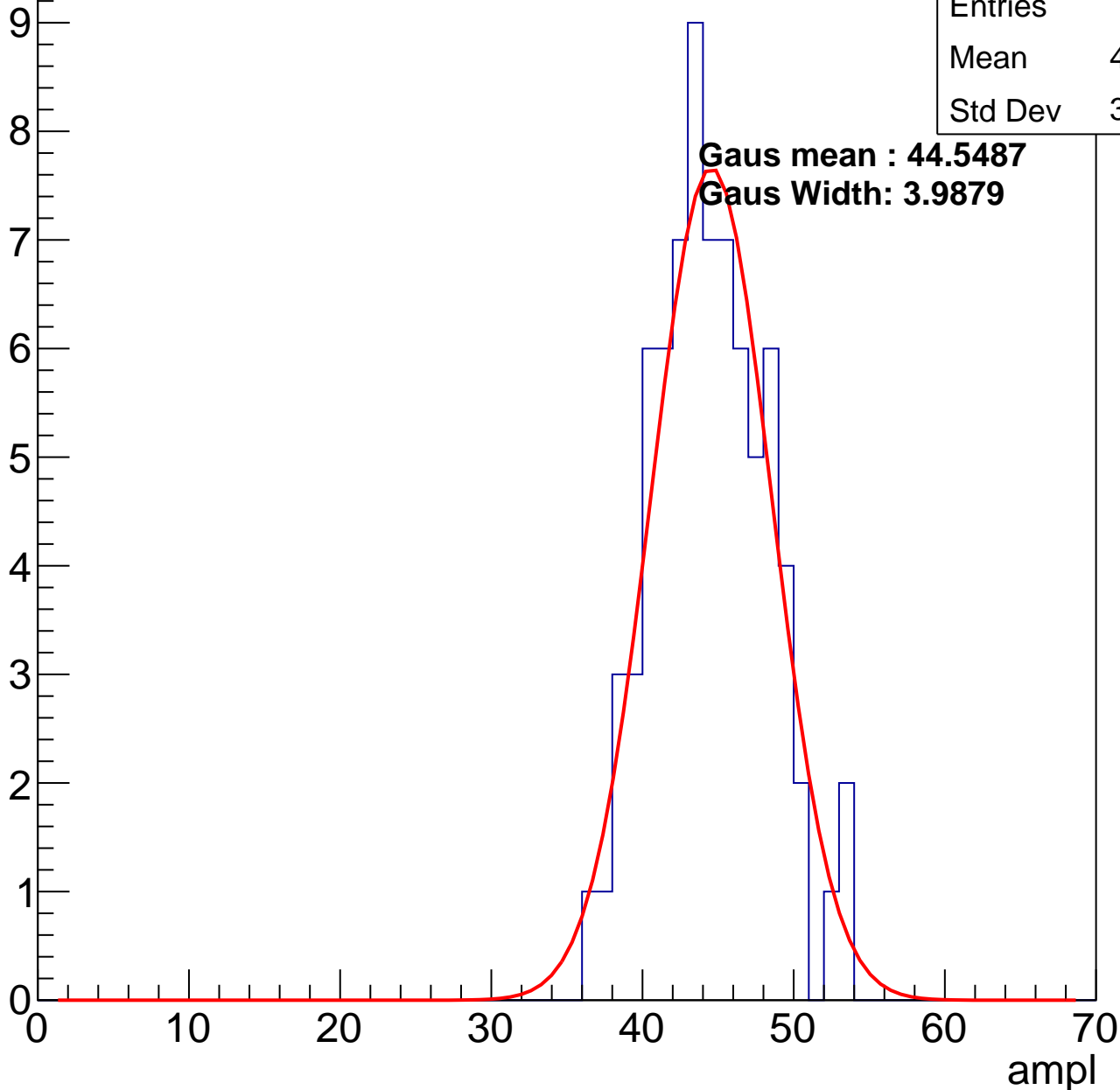
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	44.04
Std Dev	3.722

**Gaus mean : 44.5487**

**Gaus Width: 3.9879**

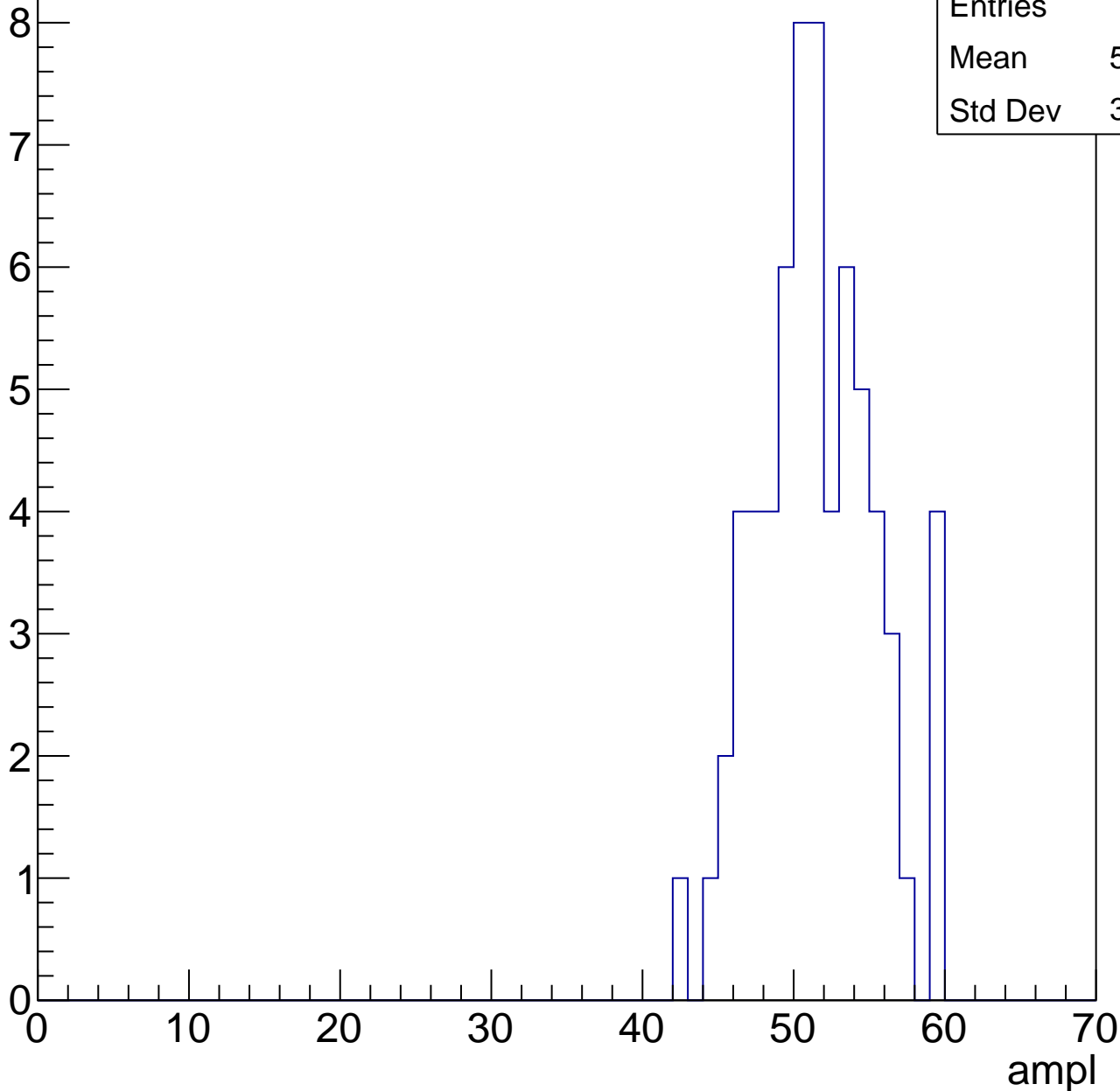


# B1L102S, U8-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	51.06
Std Dev	3.798

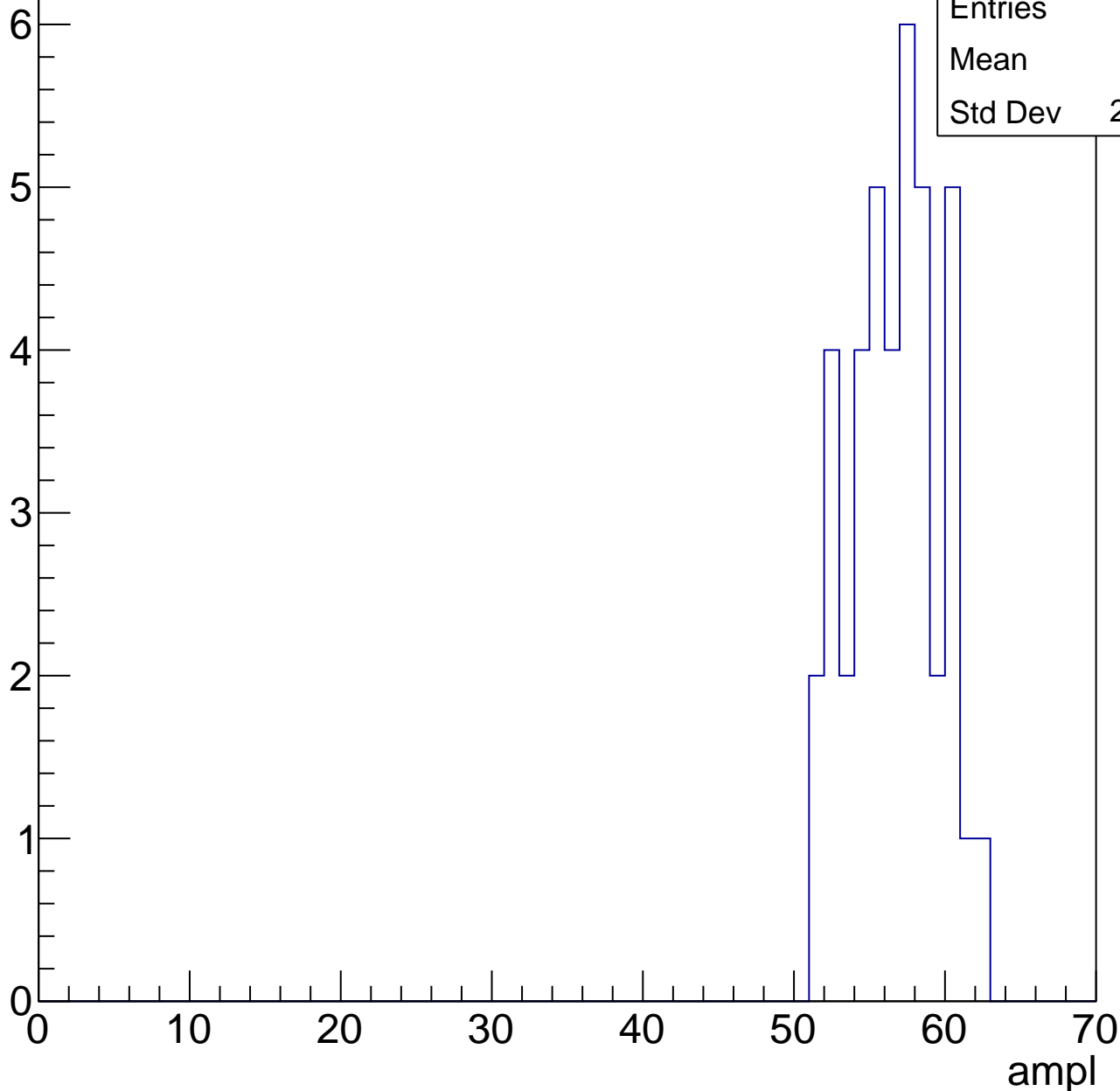


# B1L102S, U8-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	41
Mean	56.2
Std Dev	2.865

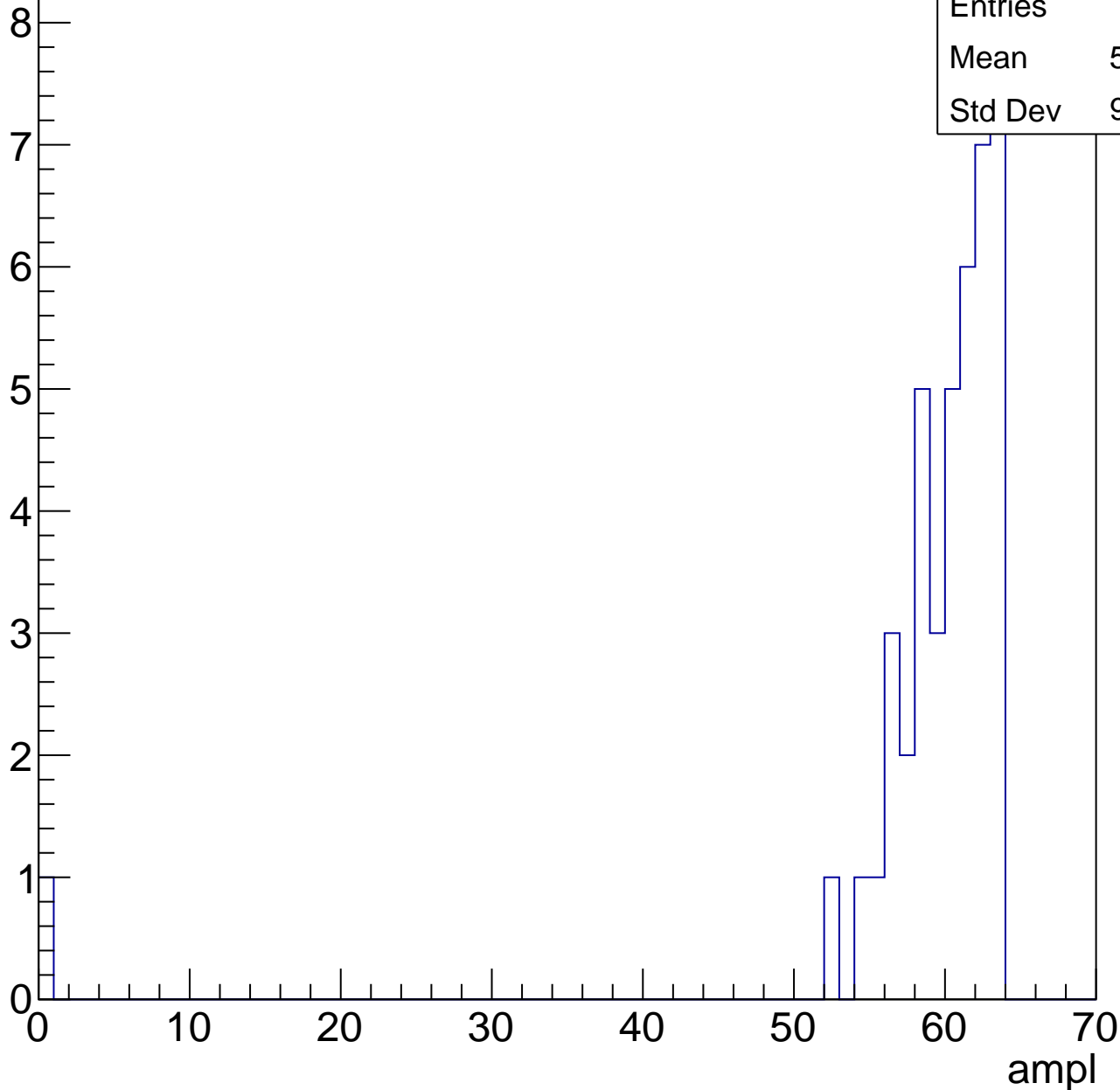


# B1L102S, U8-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

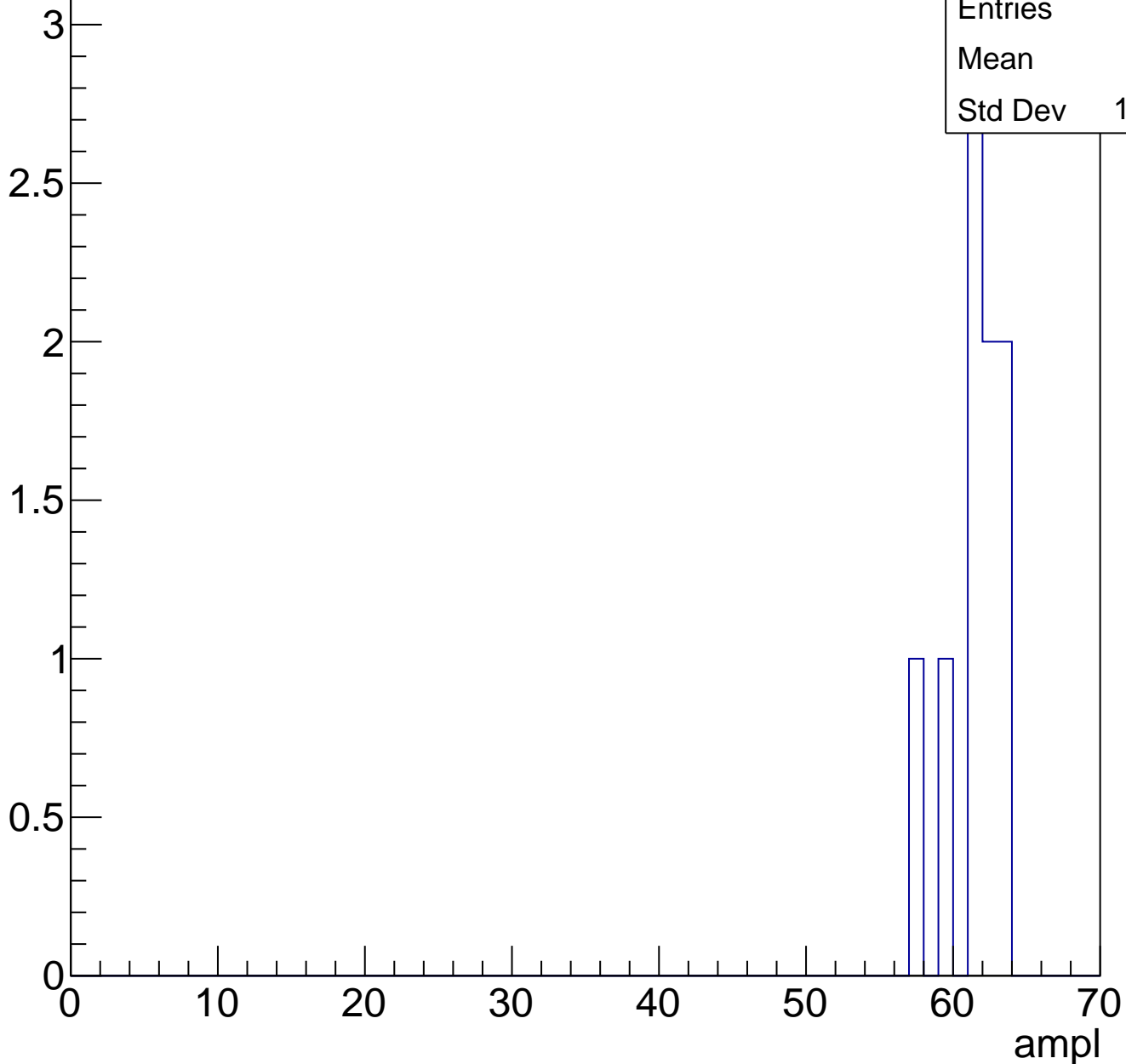
Entries	43
Mean	58.47
Std Dev	9.424



# B1L102S, U8-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U8-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U8-ch127, adc0

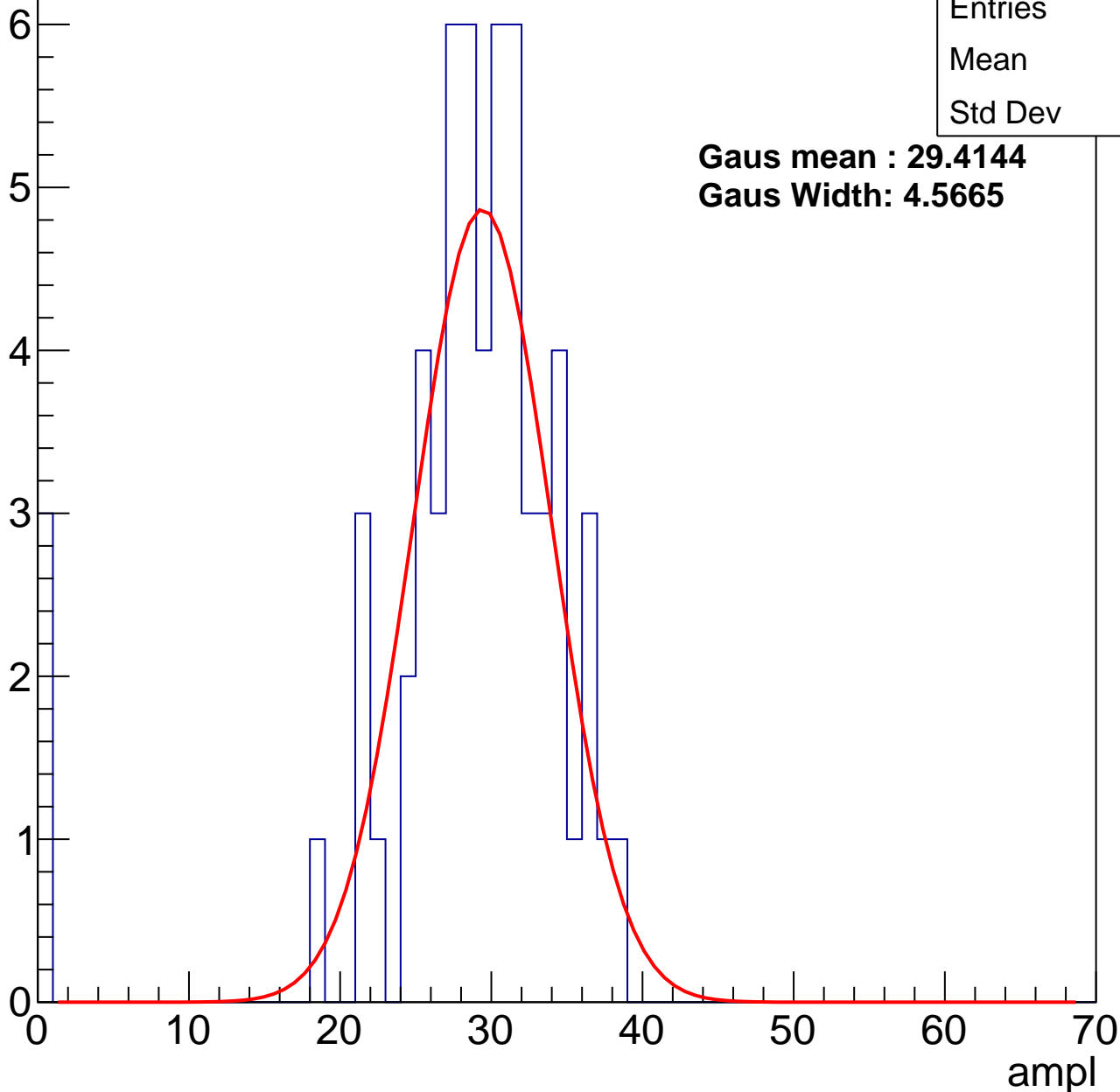
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	27.7
Std Dev	7.56

**Gaus mean : 29.4144**

**Gaus Width: 4.5665**



# B1L102S, U8-ch127, adc1

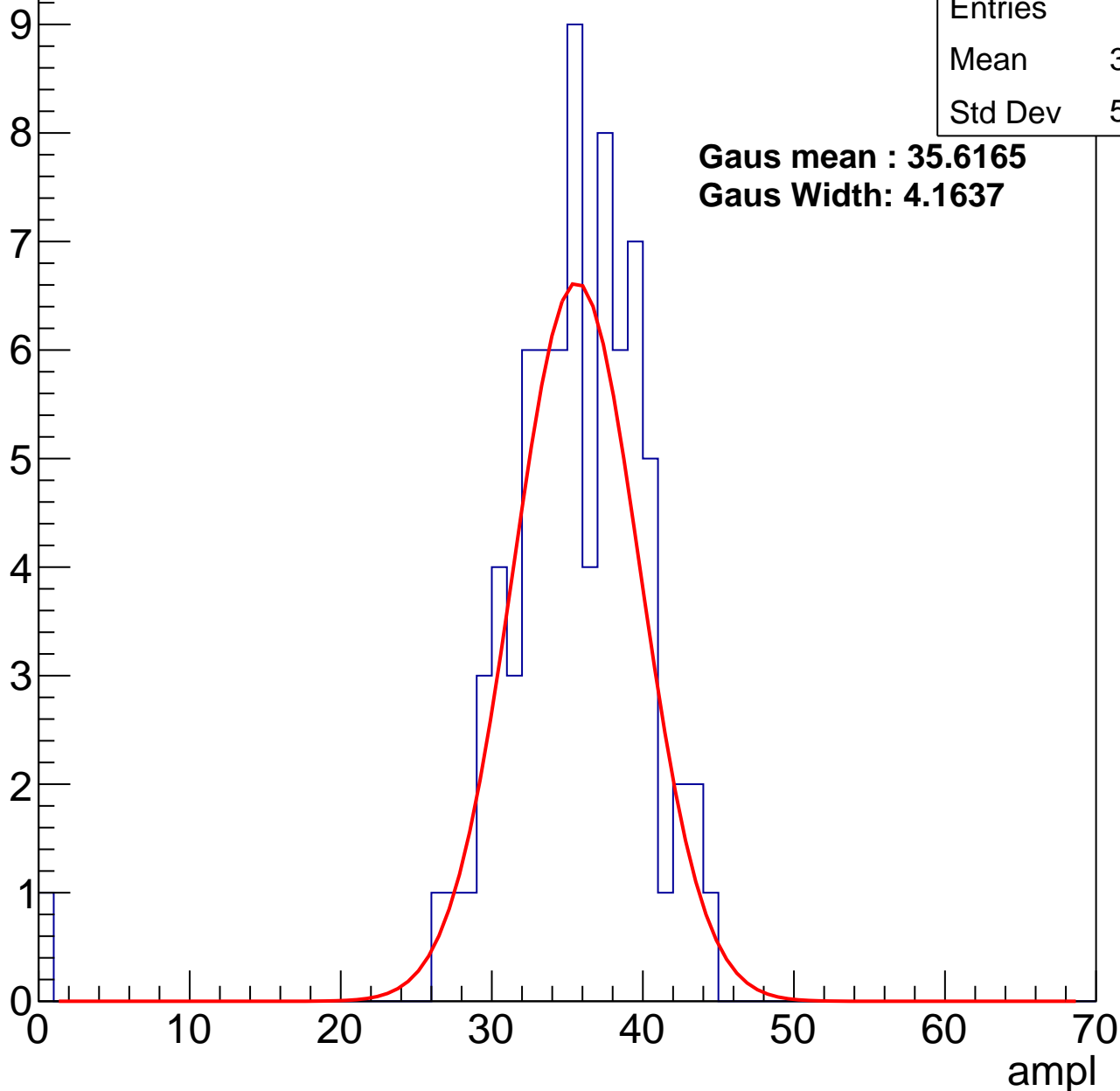
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	34.88
Std Dev	5.615

**Gaus mean : 35.6165**

**Gaus Width: 4.1637**



# B1L102S, U8-ch127, adc2

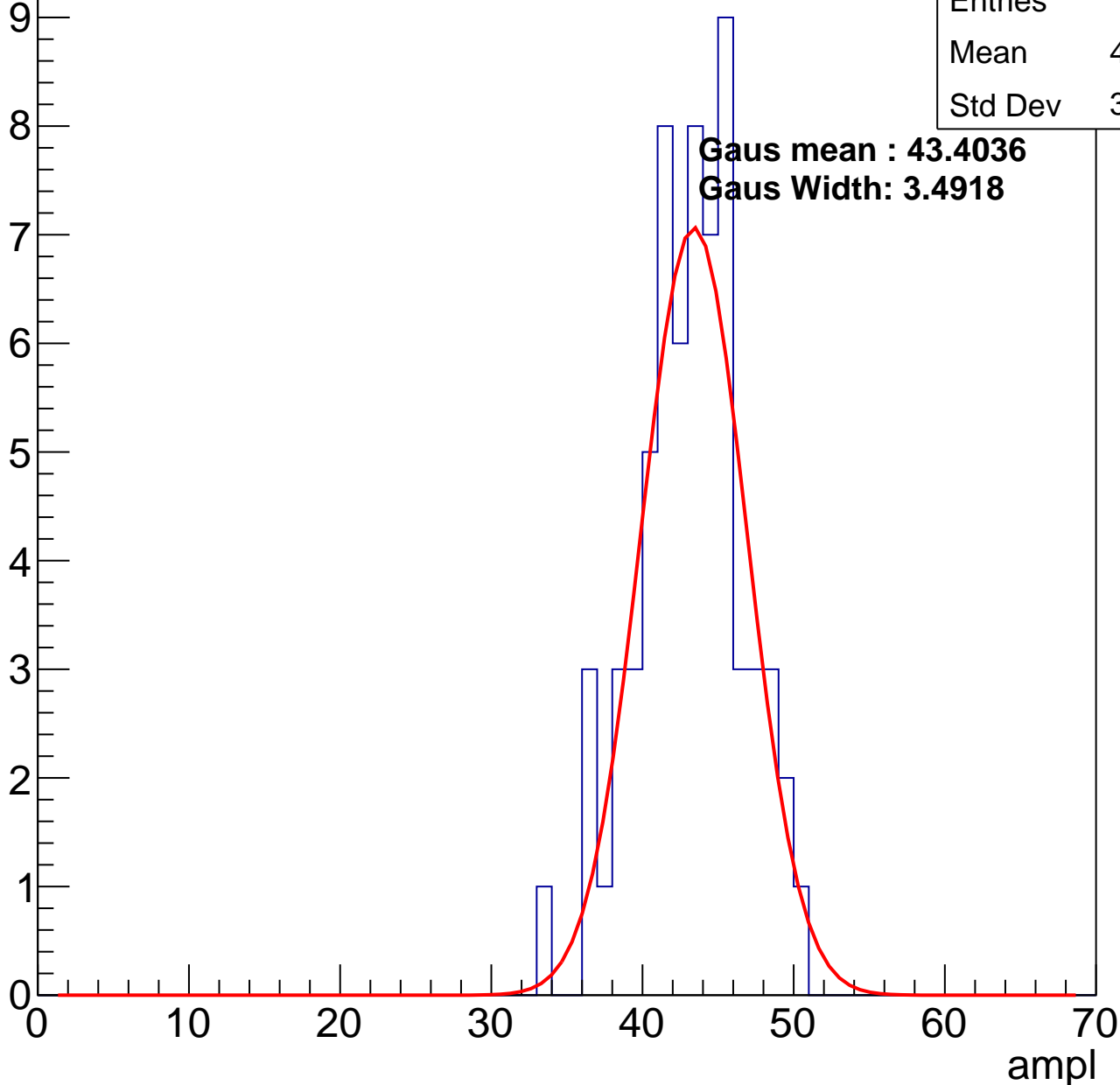
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	42.68
Std Dev	3.474

**Gaus mean : 43.4036**

**Gaus Width: 3.4918**

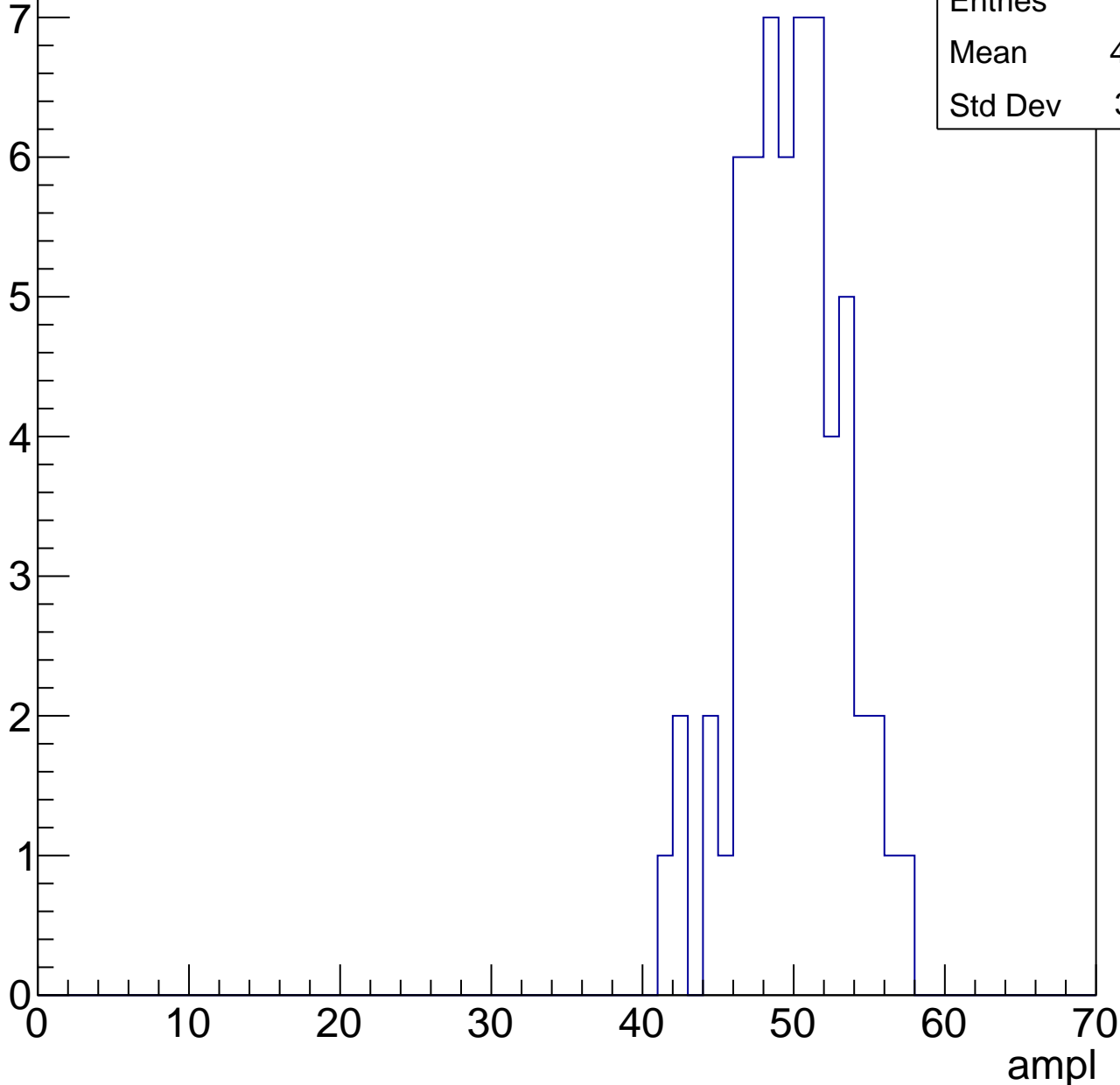


# B1L102S, U8-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	49.28
Std Dev	3.401

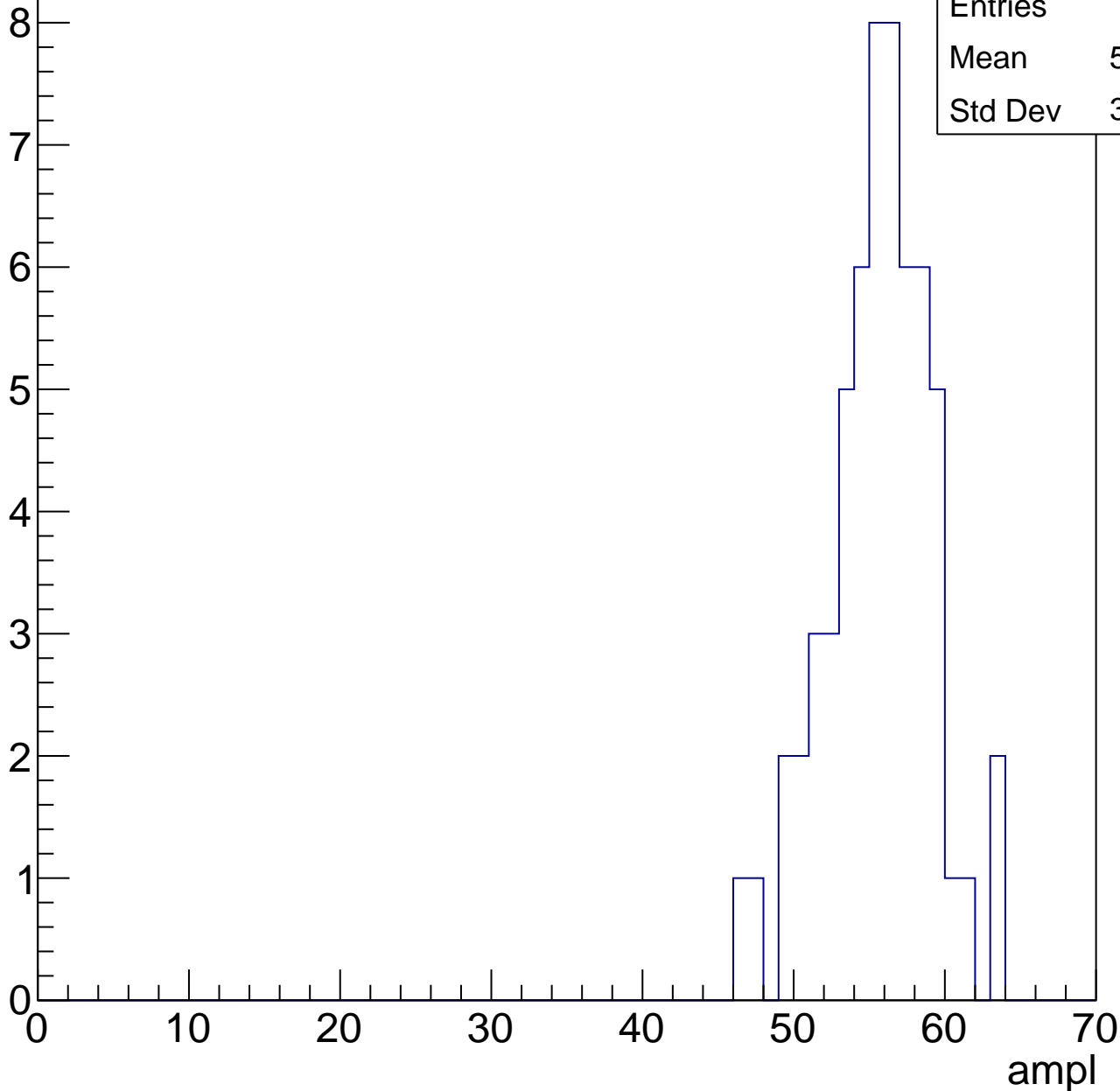


# B1L102S, U8-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	55.15
Std Dev	3.468

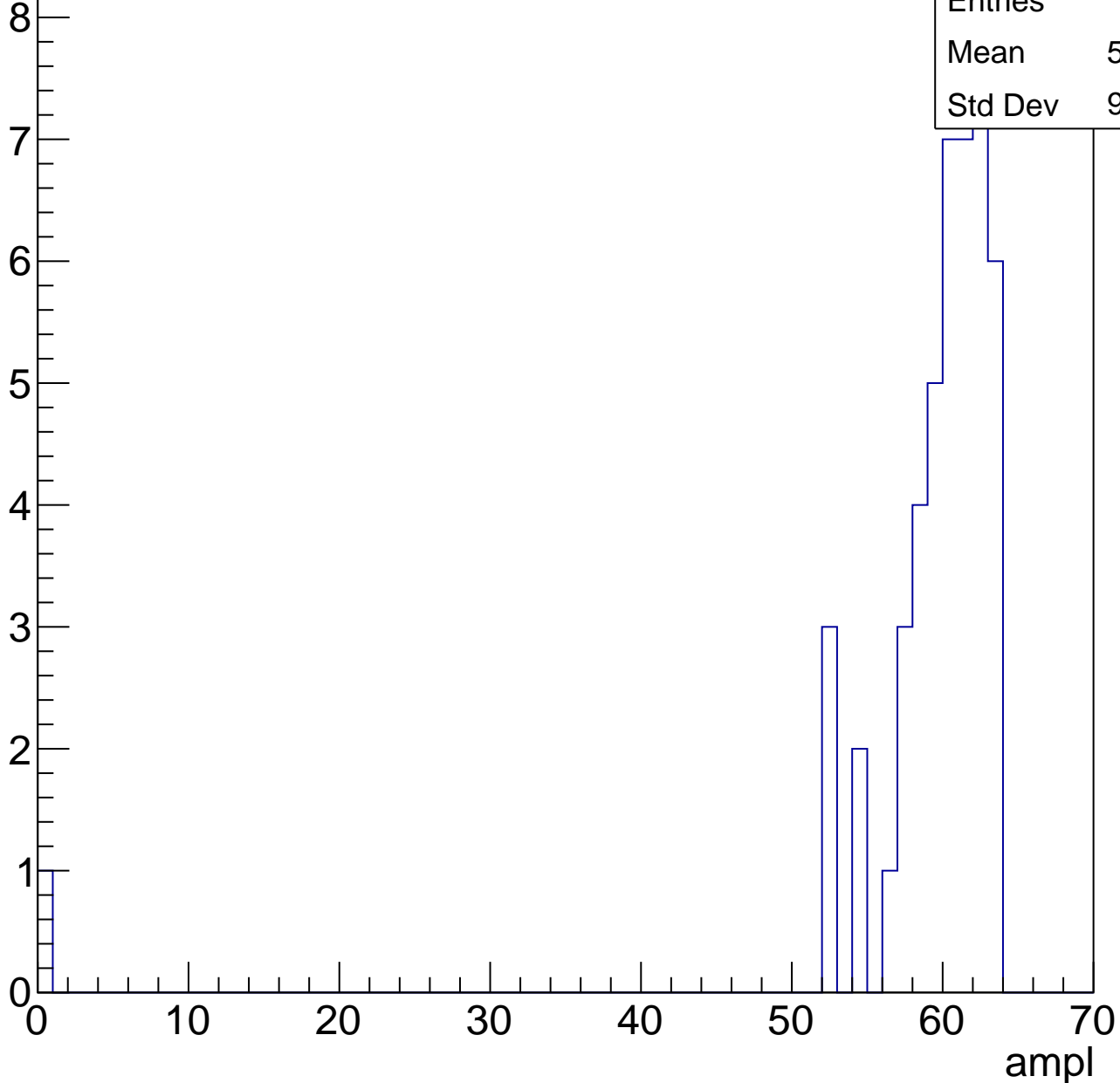


# B1L102S, U8-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	58.28
Std Dev	9.088



# B1L102S, U8-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	8
Mean	61.5
Std Dev	1.118

0 10 20 30 40 50 60 70

ampl



# B1L102S, U8-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U8-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

