



# B1L101S, U16-ch0, adc0

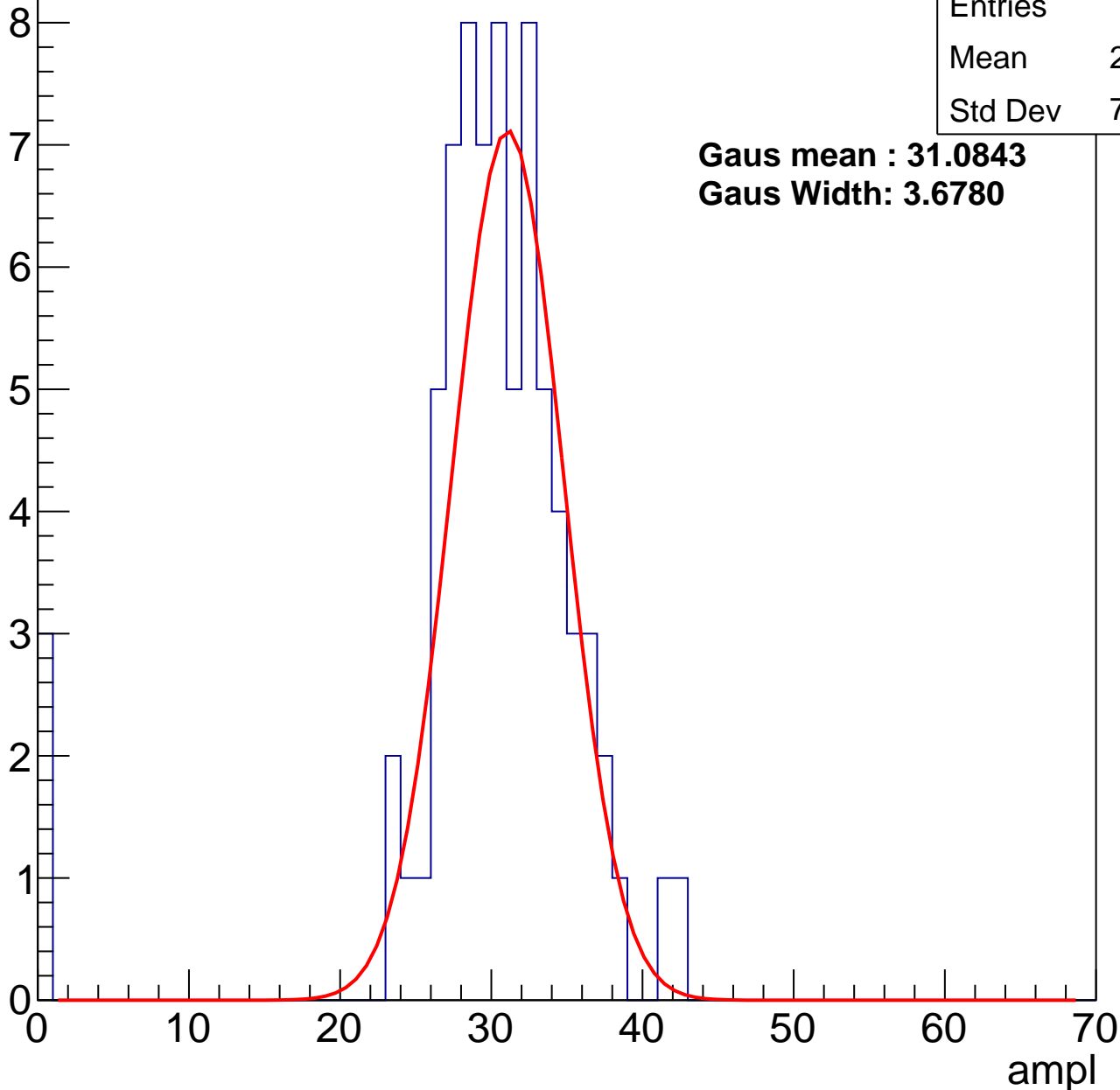
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	29.35
Std Dev	7.085

**Gaus mean : 31.0843**

**Gaus Width: 3.6780**



# B1L101S, U16-ch0, adc1

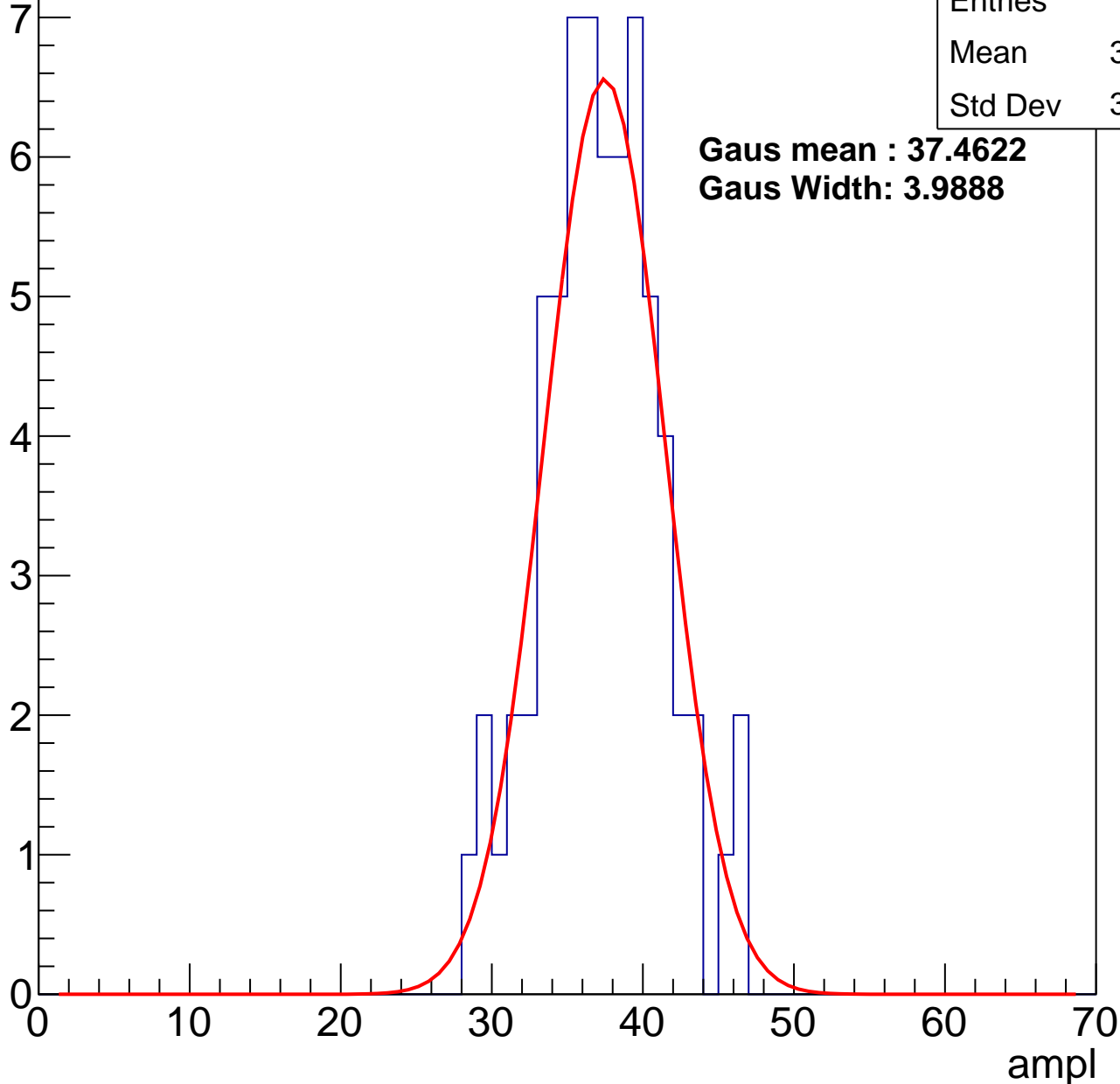
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	36.84
Std Dev	3.919

**Gaus mean : 37.4622**

**Gaus Width: 3.9888**



# B1L101S, U16-ch0, adc2

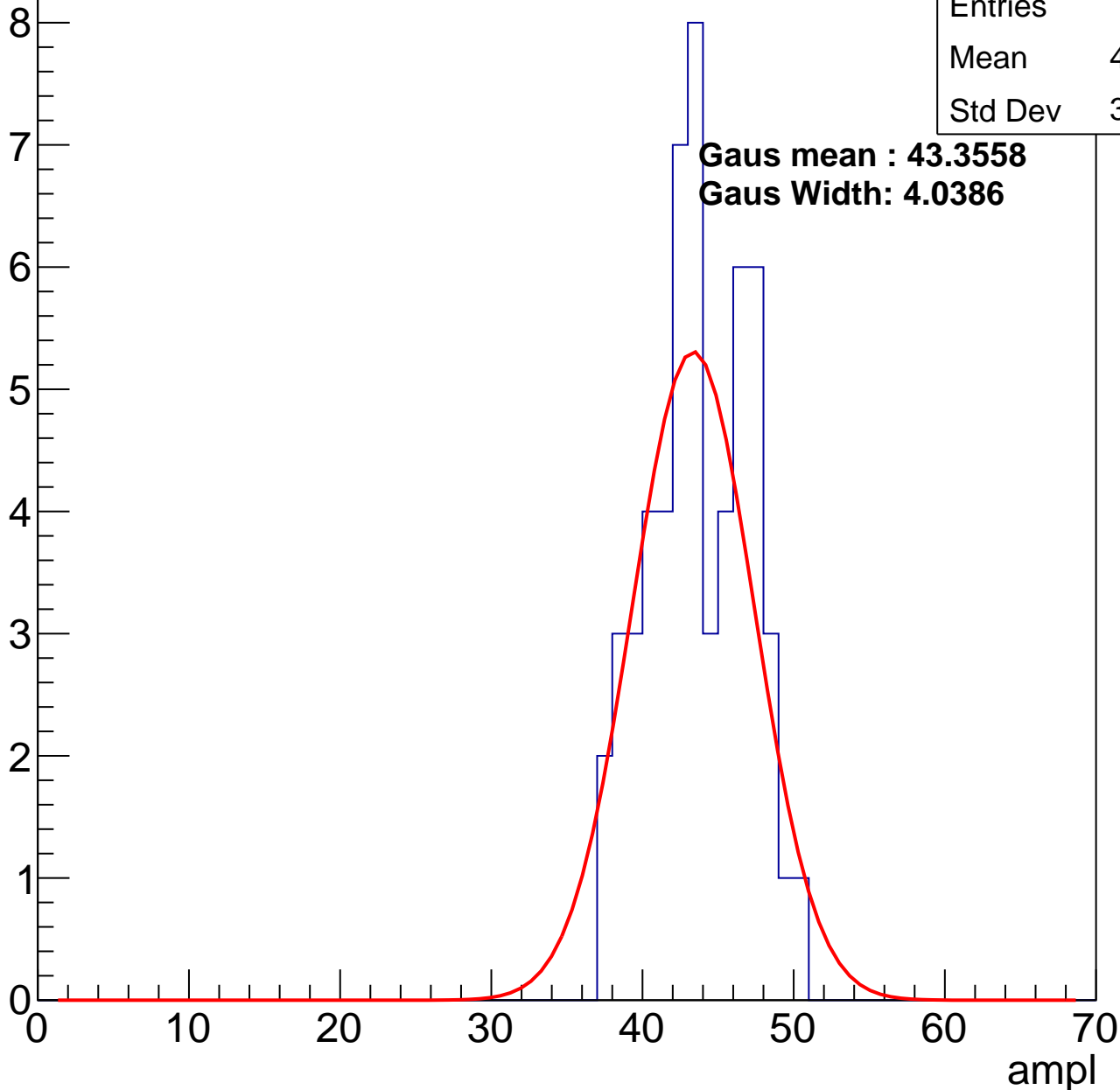
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	43.27
Std Dev	3.244

**Gaus mean : 43.3558**

**Gaus Width: 4.0386**

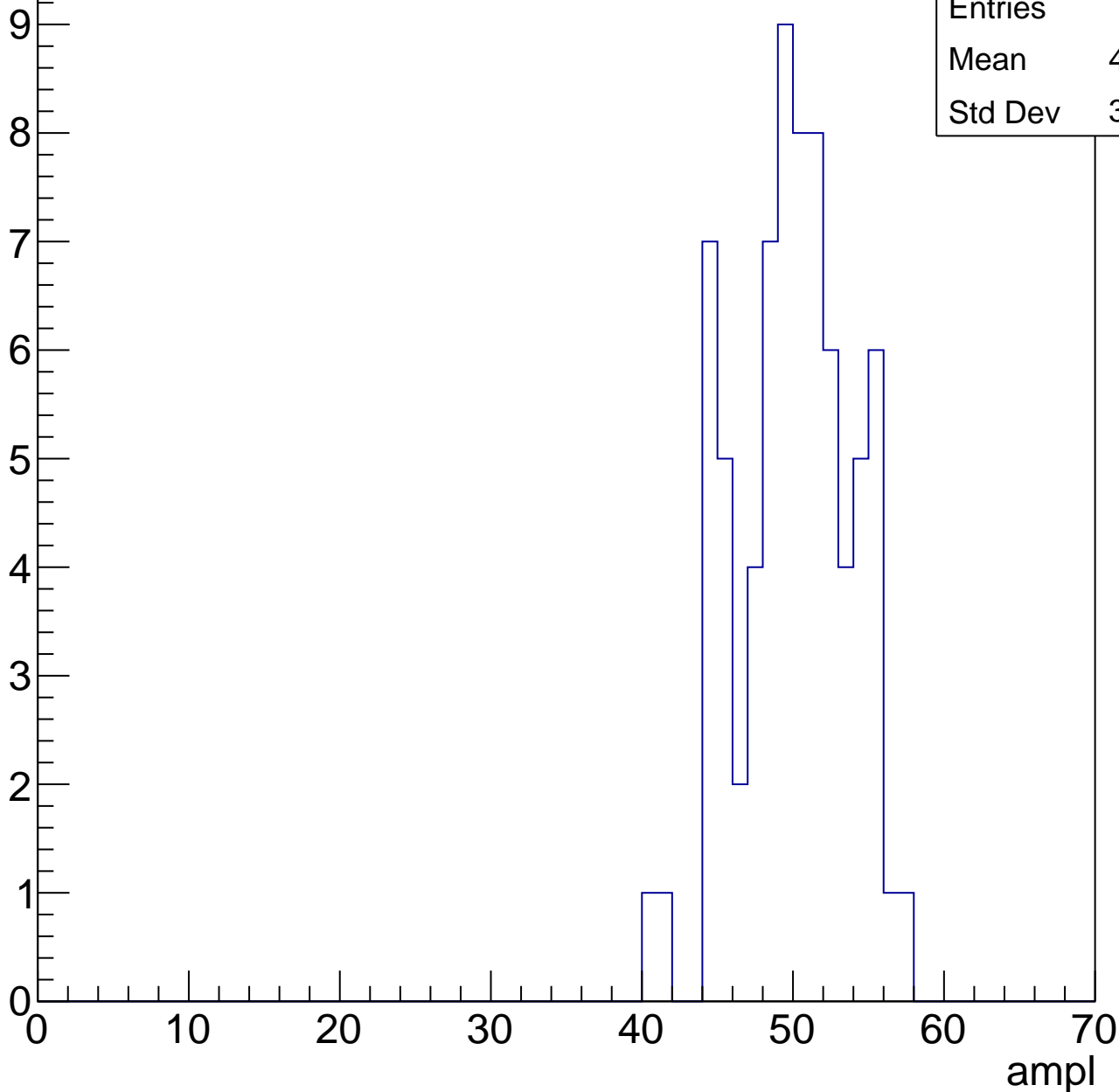


# B1L101S, U16-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

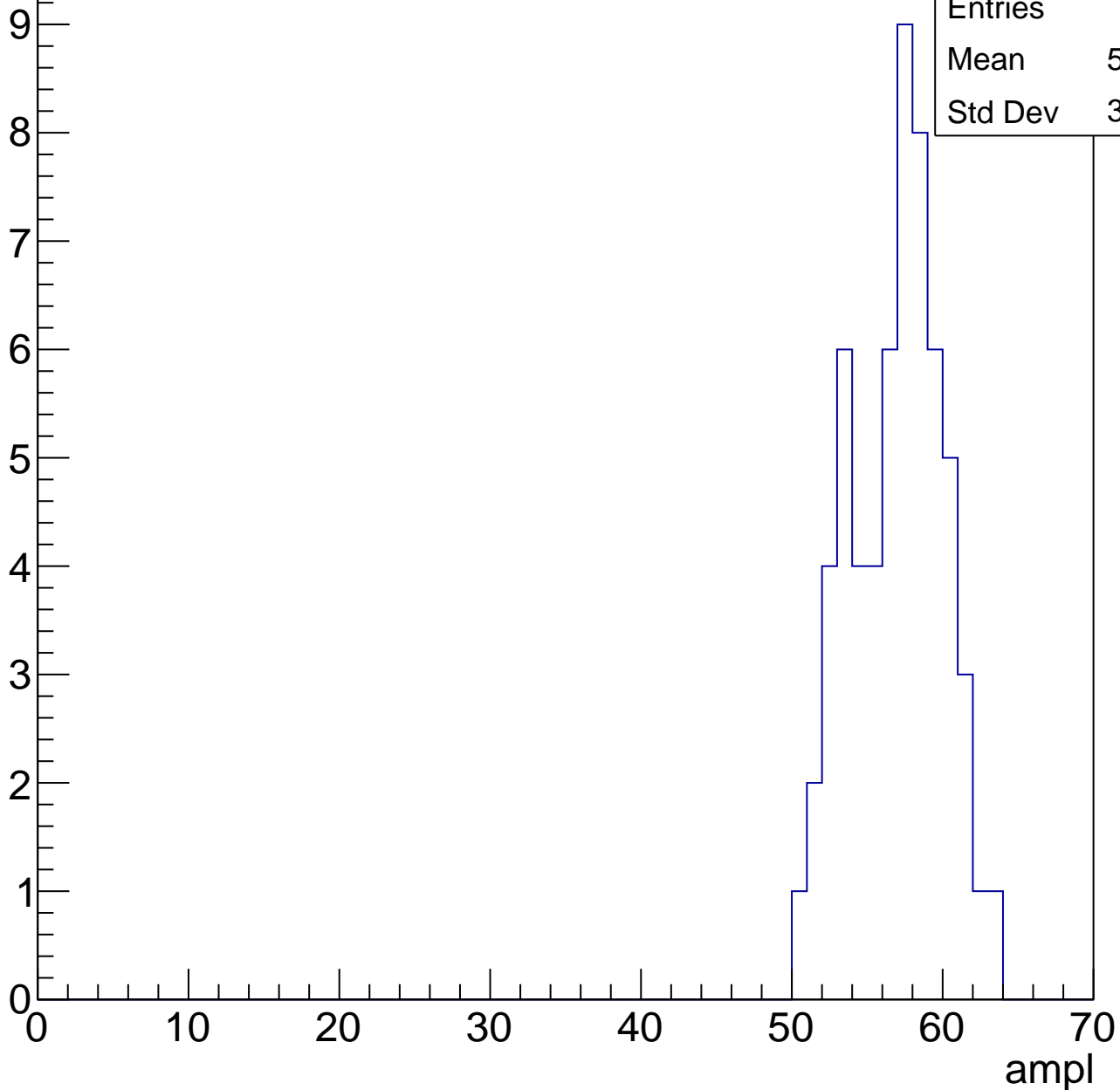
Entries	75
Mean	49.55
Std Dev	3.707



# B1L101S, U16-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

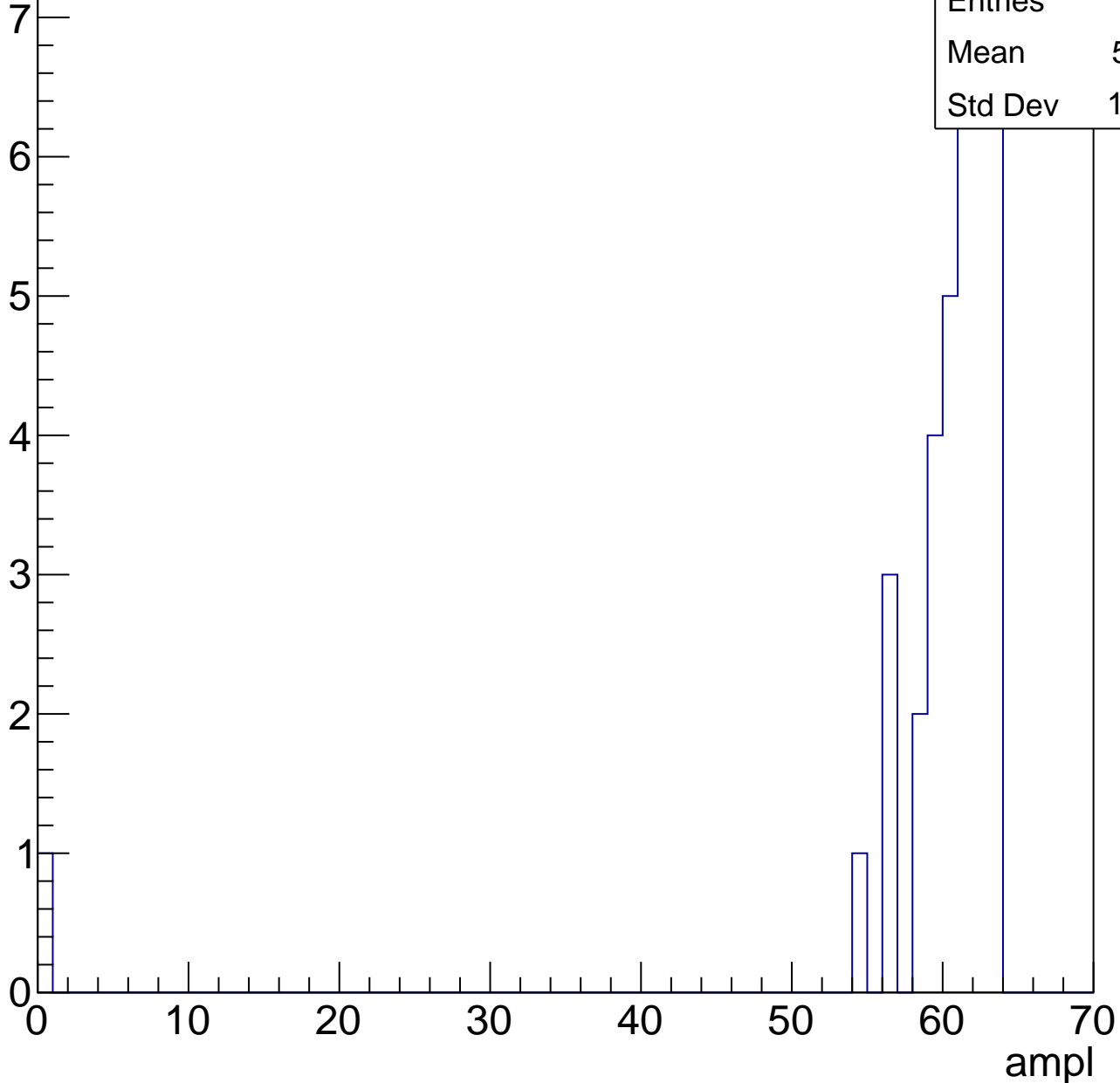


# B1L101S, U16-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	37
Mean	58.81
Std Dev	10.06



# B1L101S, U16-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

0

10

20

30

40

50

60

70

ampl

Entries	4
Mean	62.5
Std Dev	0.5



# B1L101S, U16-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U16-ch1, adc0

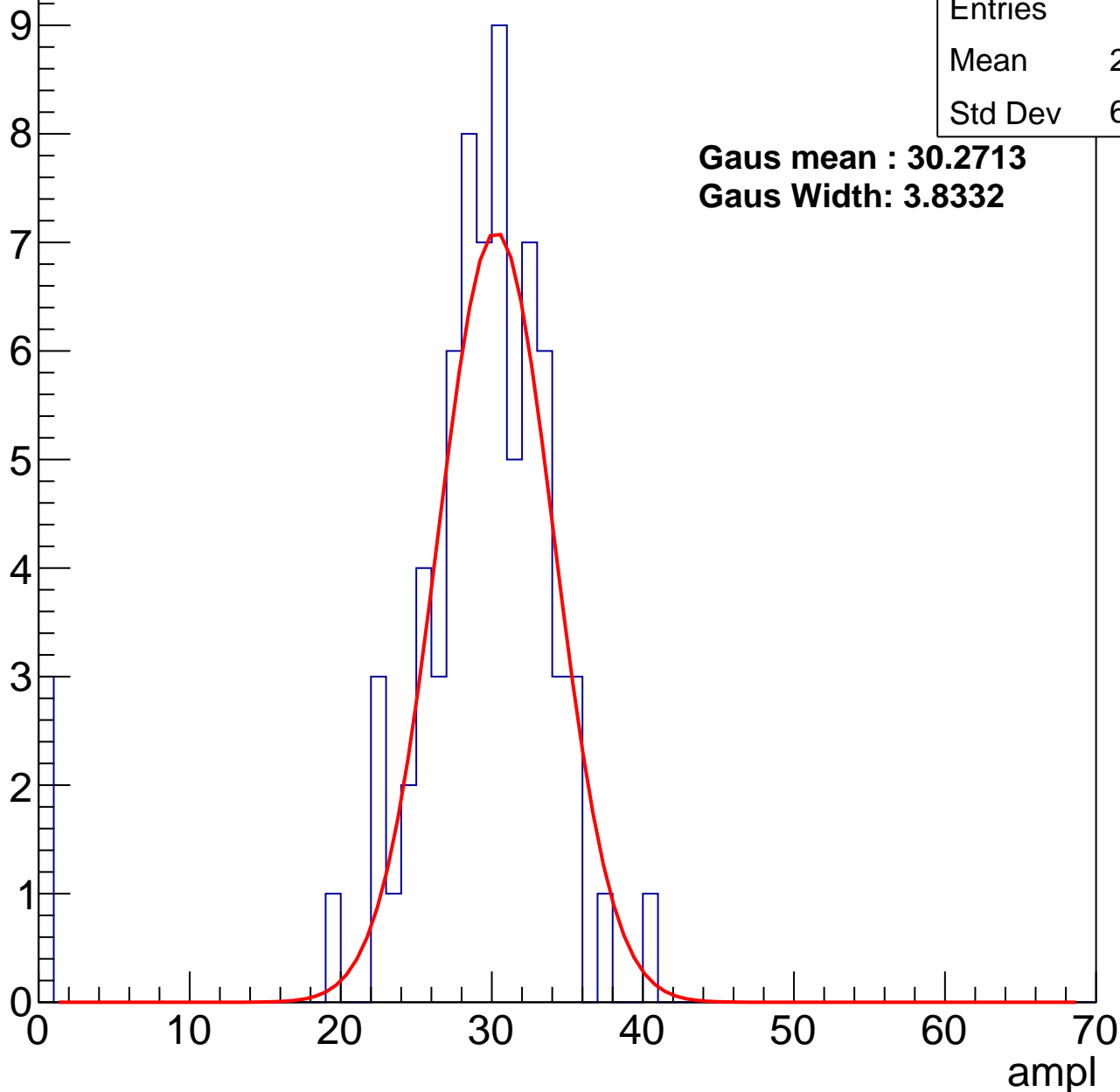
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	28.14
Std Dev	6.905

**Gaus mean : 30.2713**

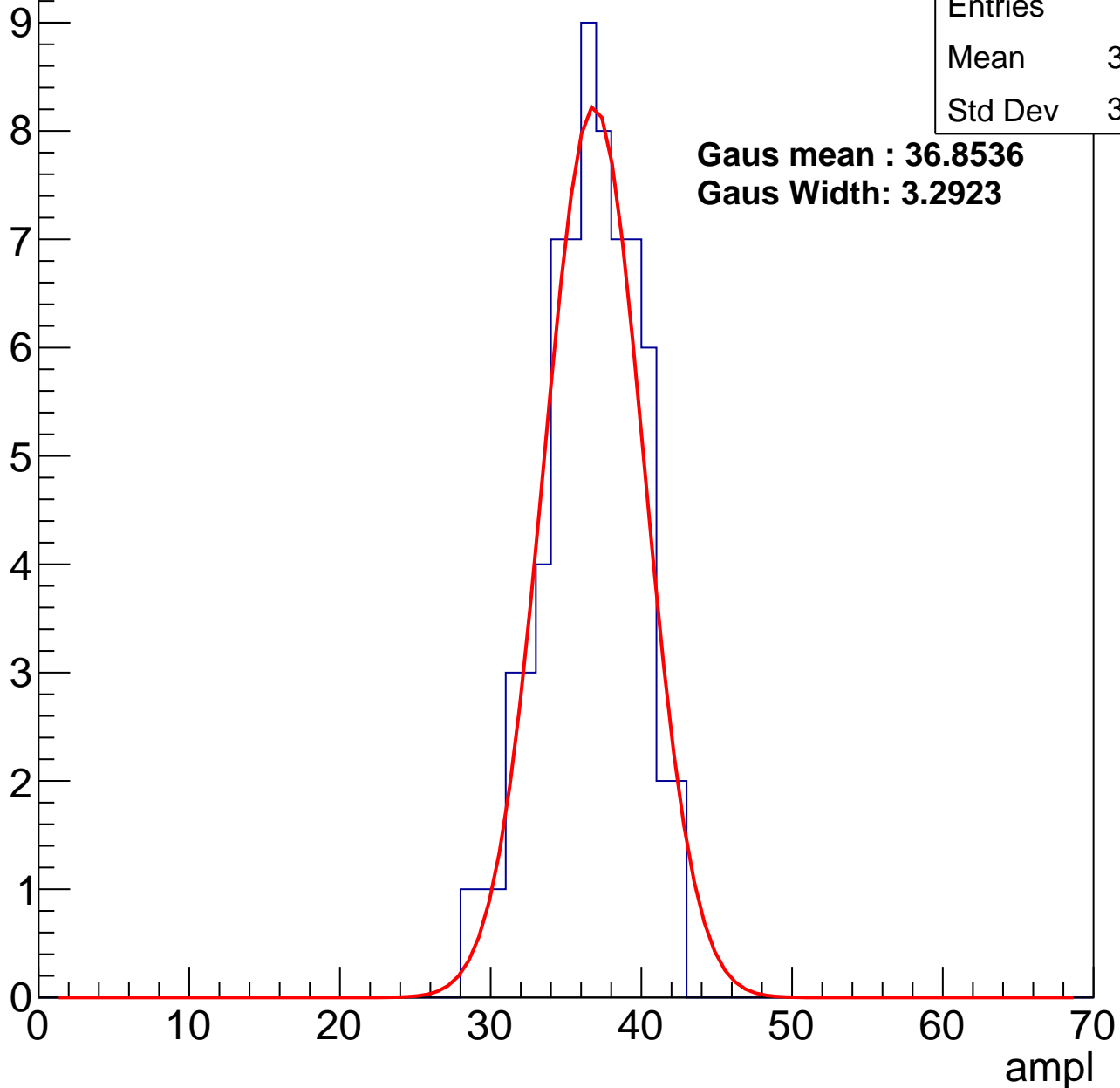
**Gaus Width: 3.8332**



# B1L101S, U16-ch1, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

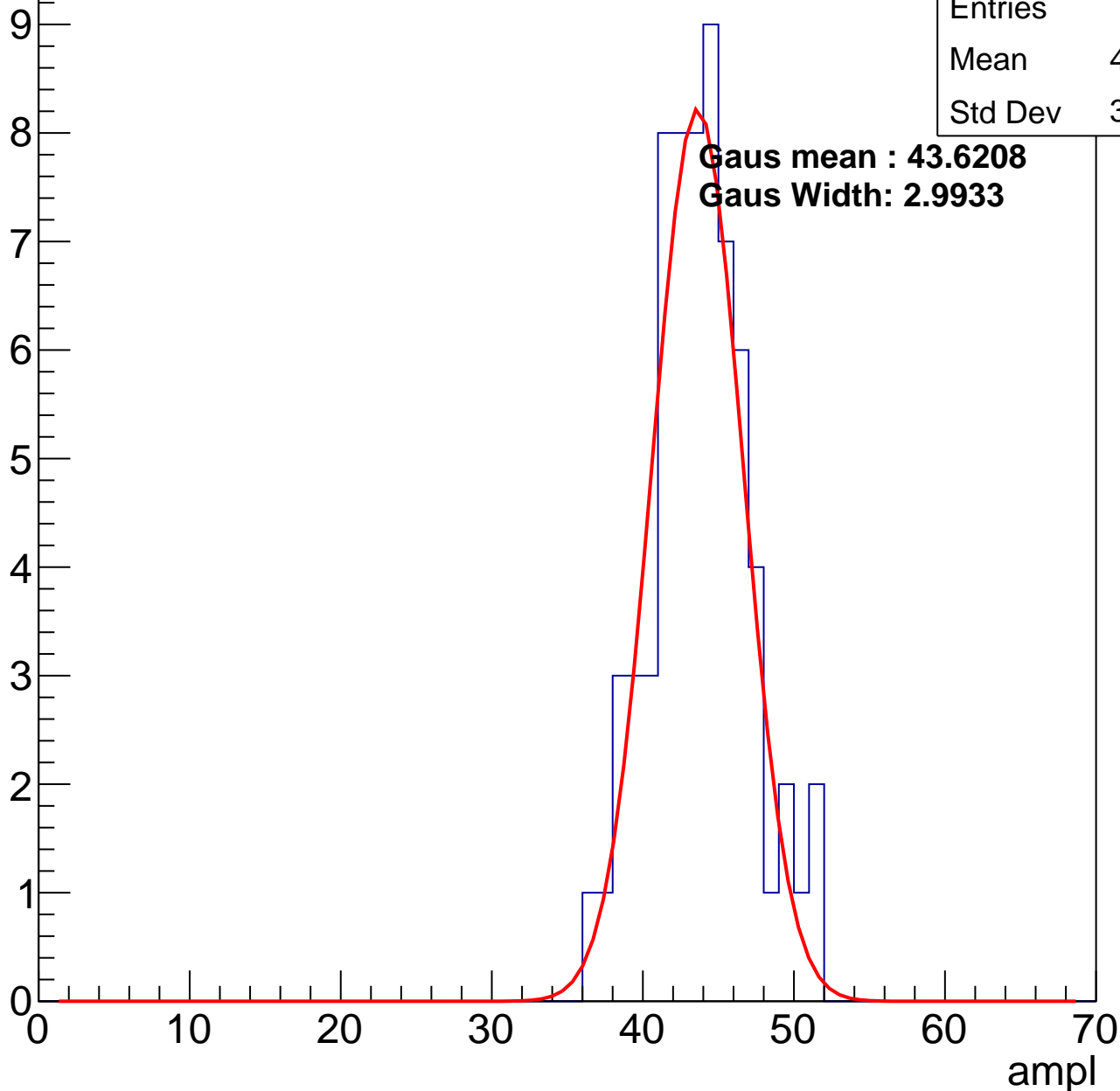
Entry



# B1L101S, U16-ch1, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

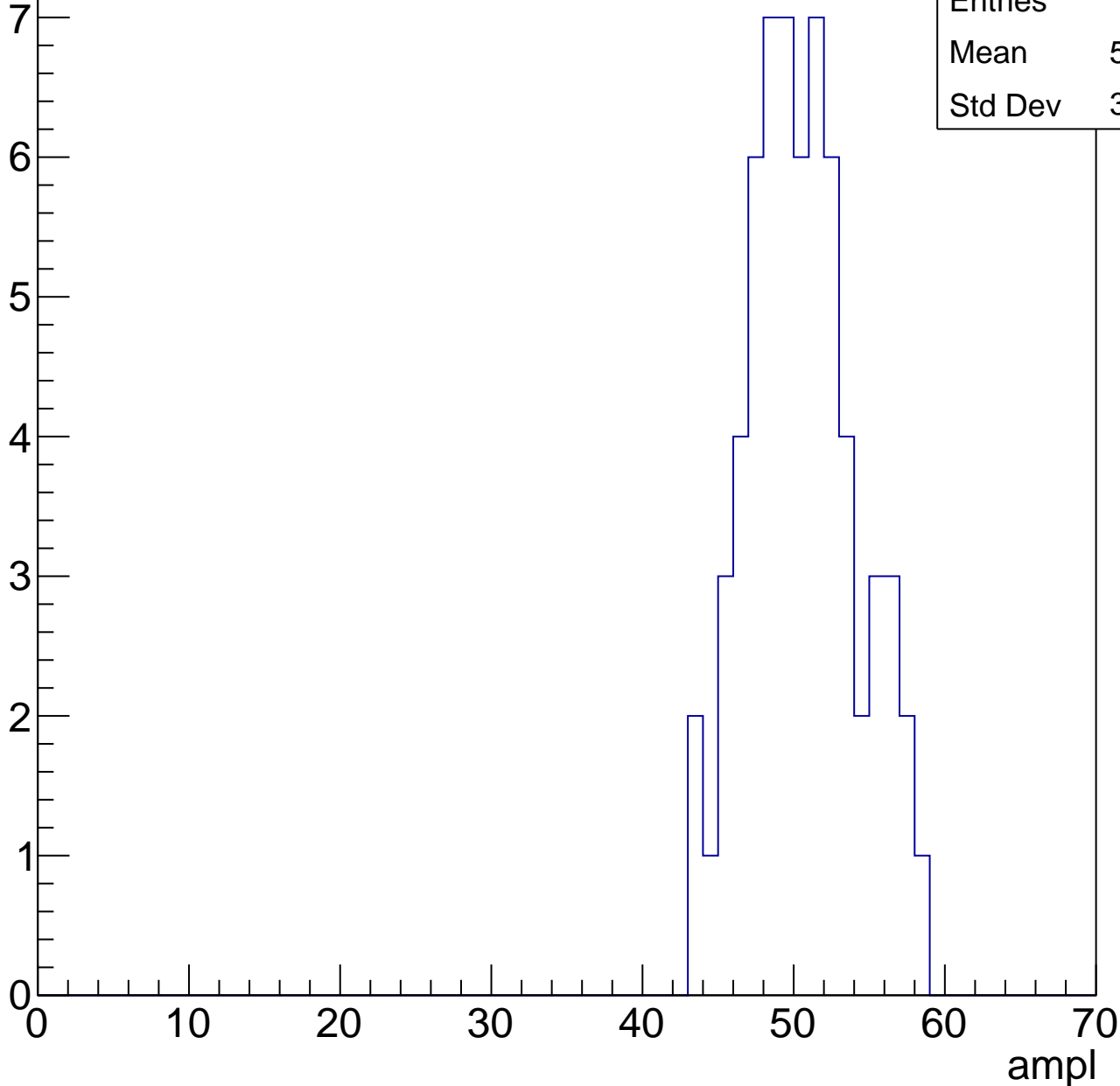


# B1L101S, U16-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	50.06
Std Dev	3.548

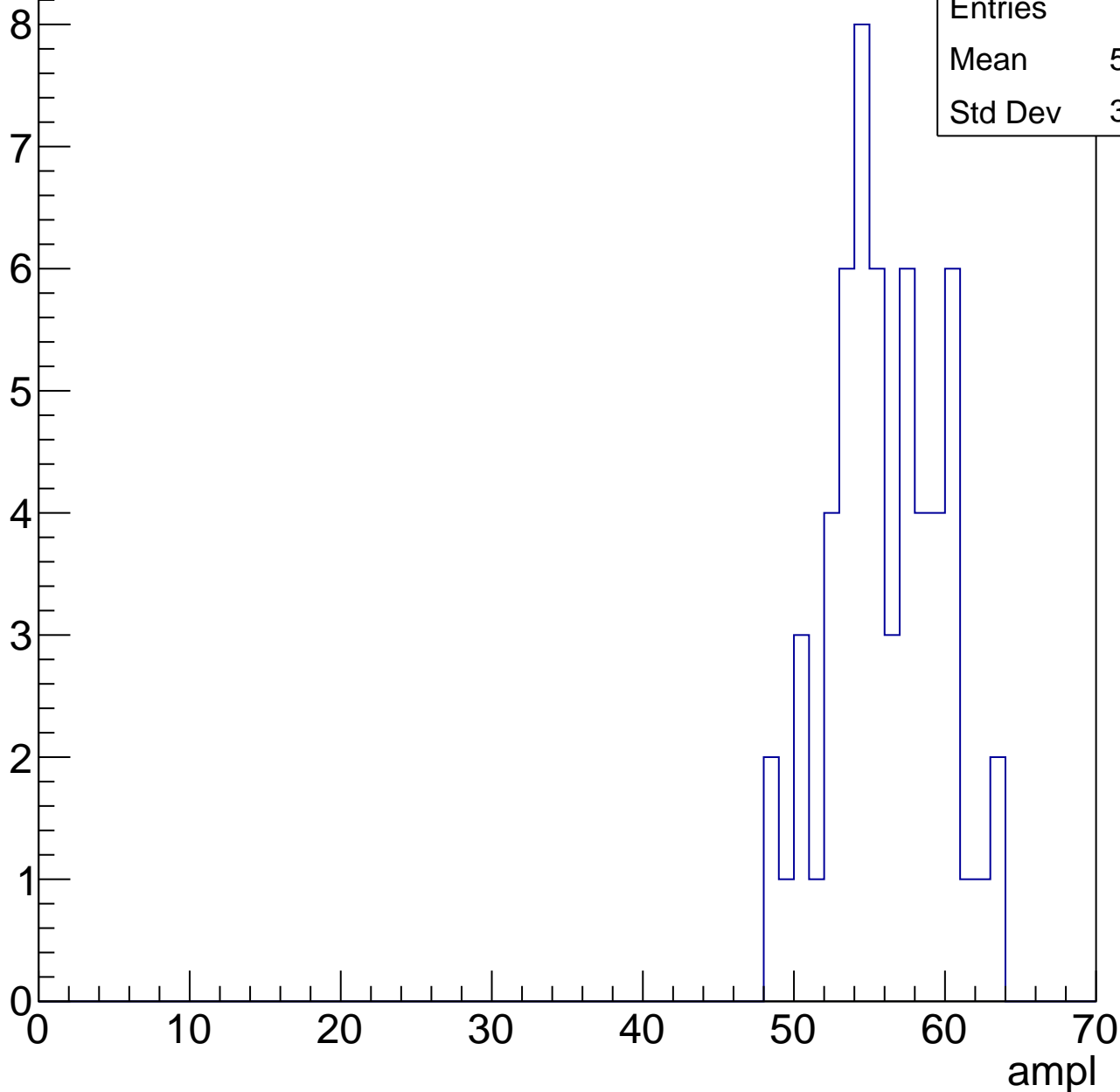


# B1L101S, U16-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	55.53
Std Dev	3.635

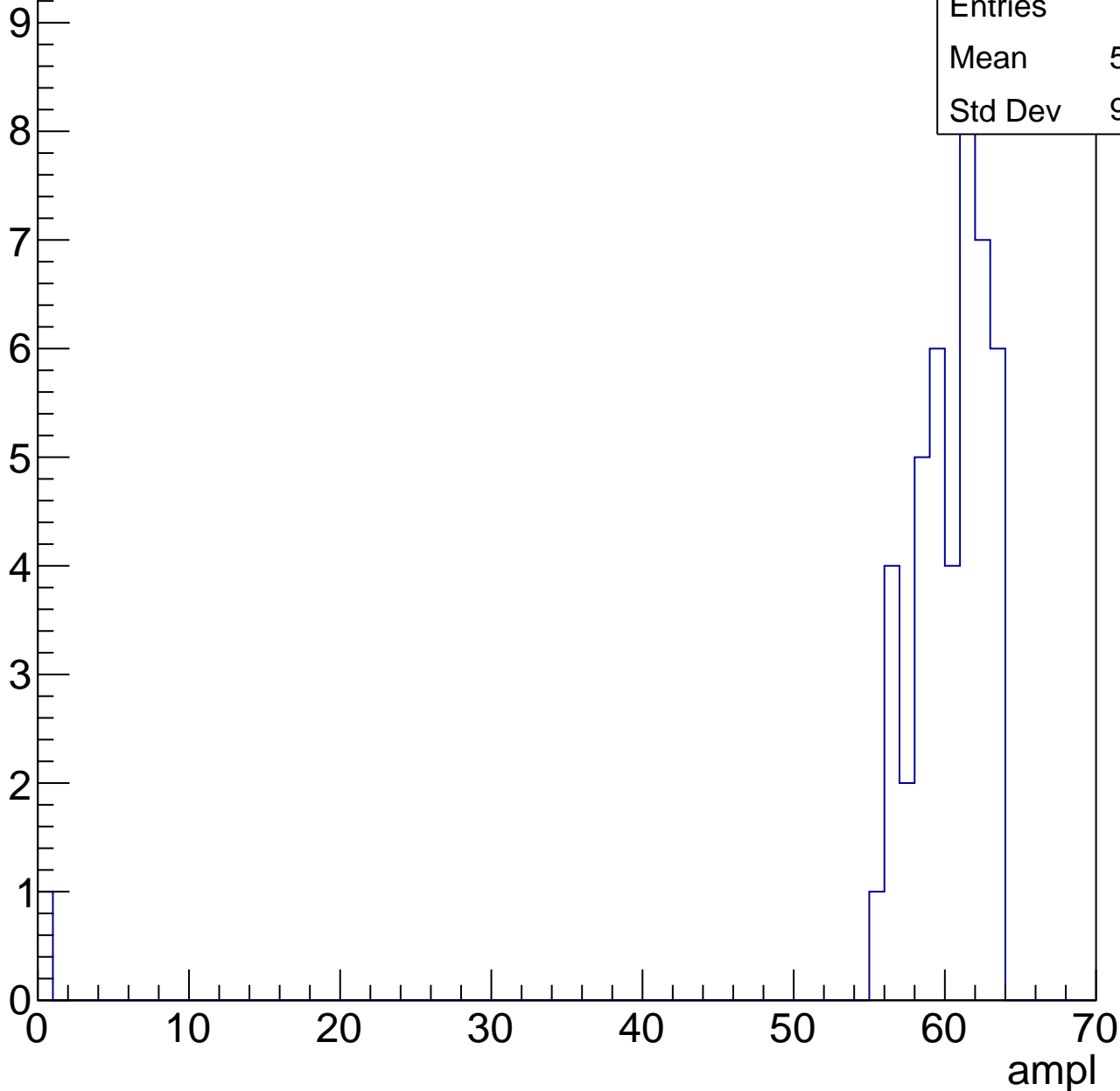


# B1L101S, U16-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

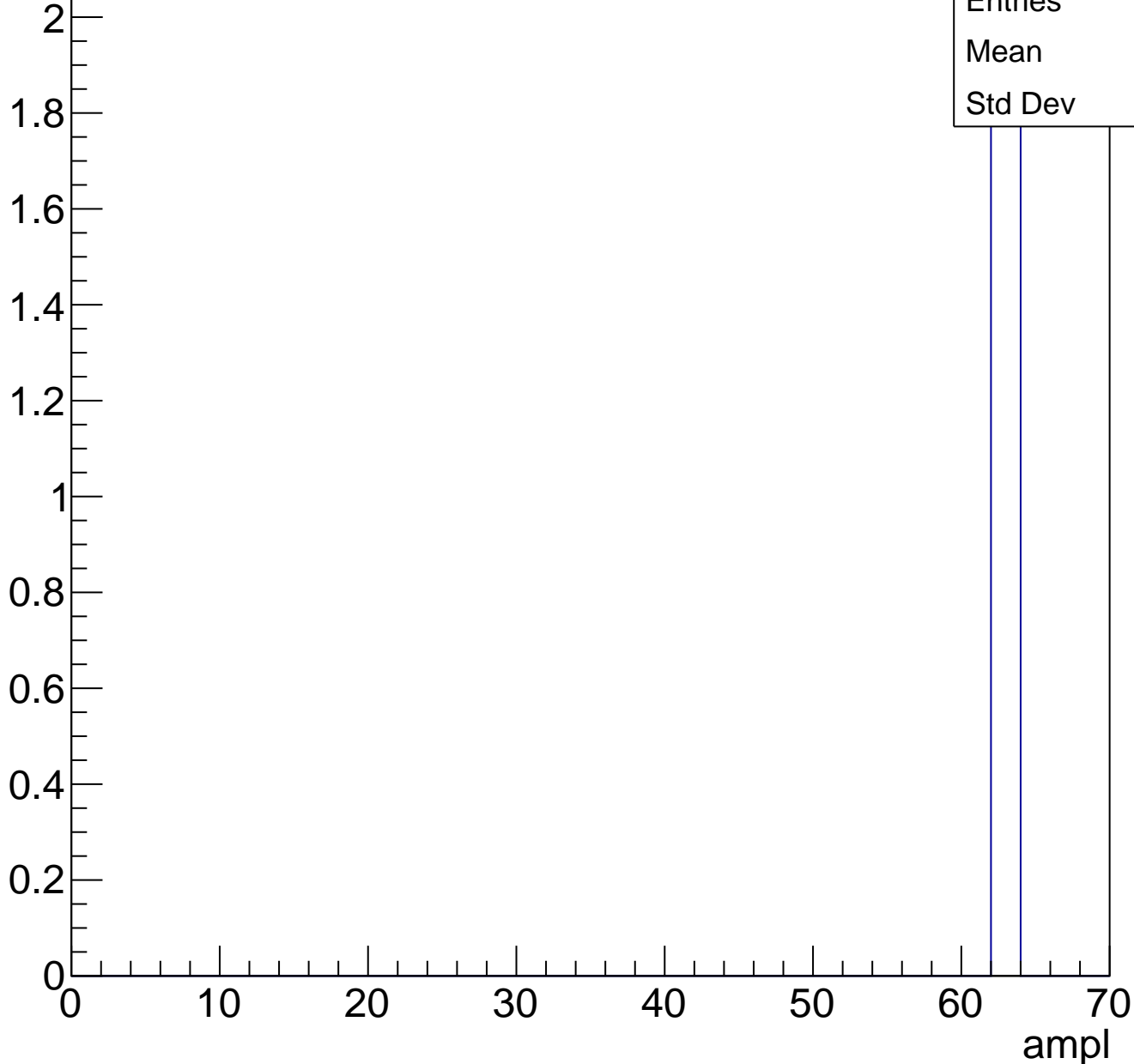
Entries	45
Mean	58.62
Std Dev	9.115



# B1L101S, U16-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U16-ch2, adc0

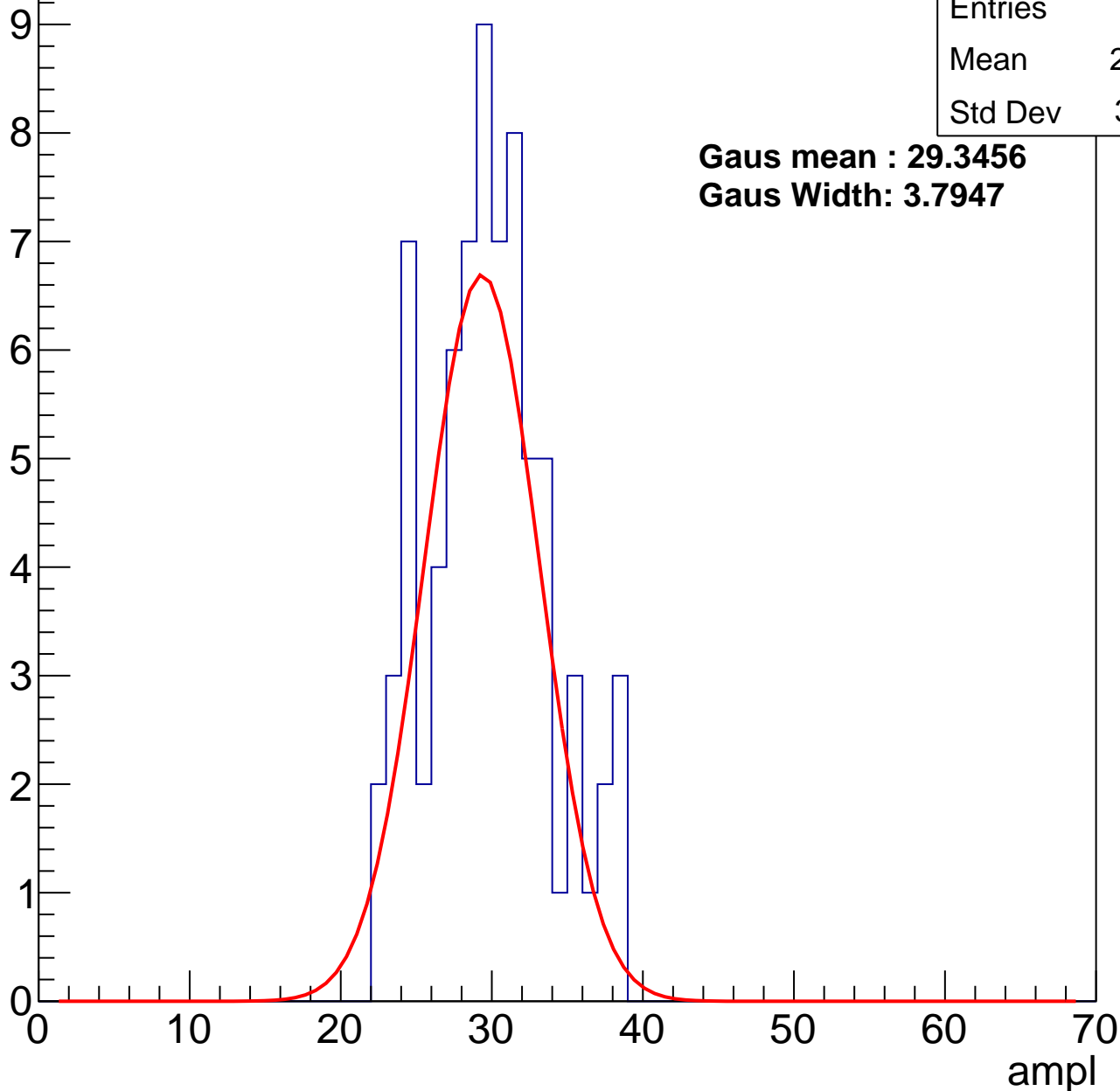
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	29.33
Std Dev	3.981

**Gaus mean : 29.3456**

**Gaus Width: 3.7947**



# B1L101S, U16-ch2, adc1

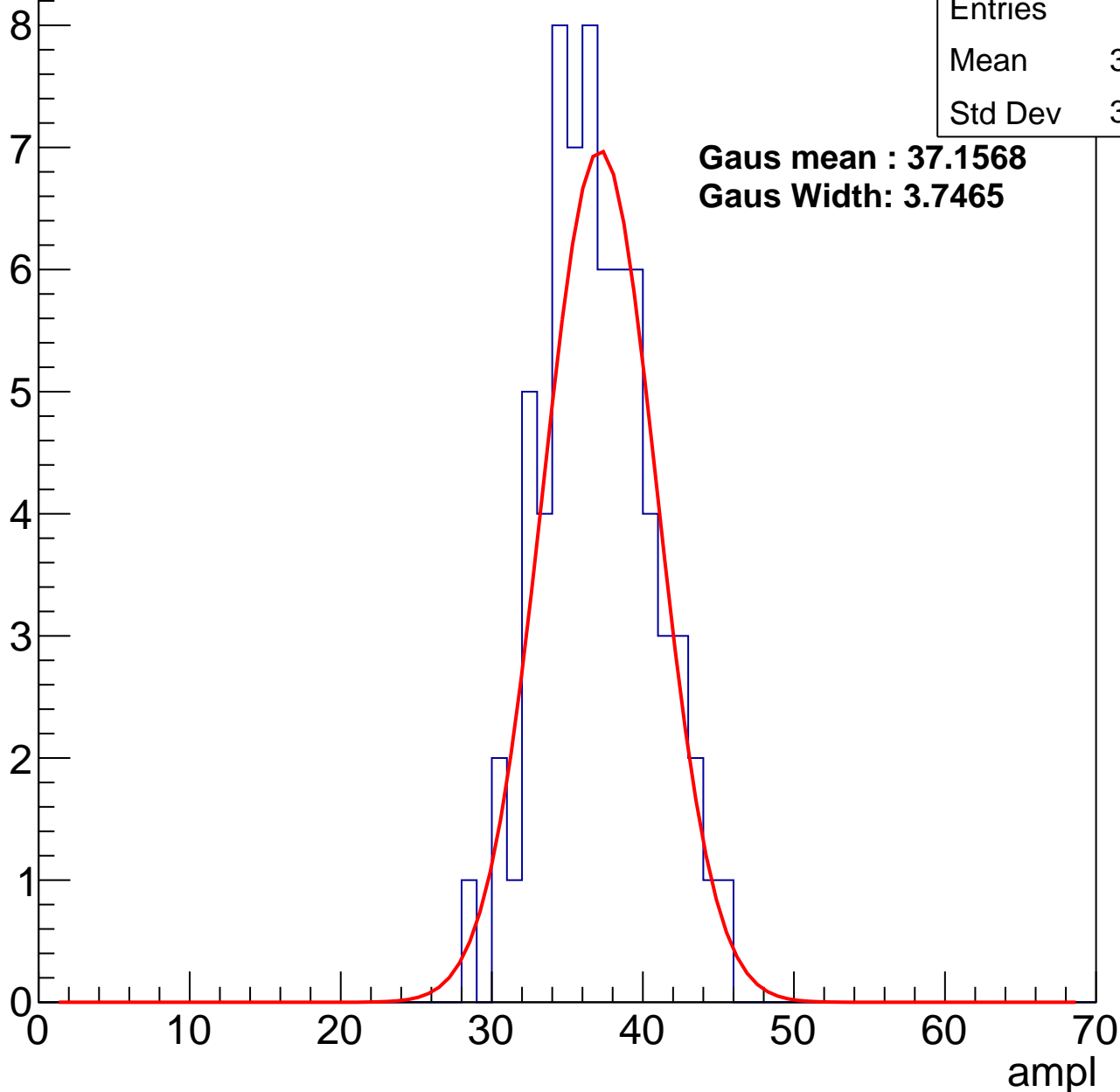
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	36.53
Std Dev	3.579

**Gaus mean : 37.1568**

**Gaus Width: 3.7465**



# B1L101S, U16-ch2, adc2

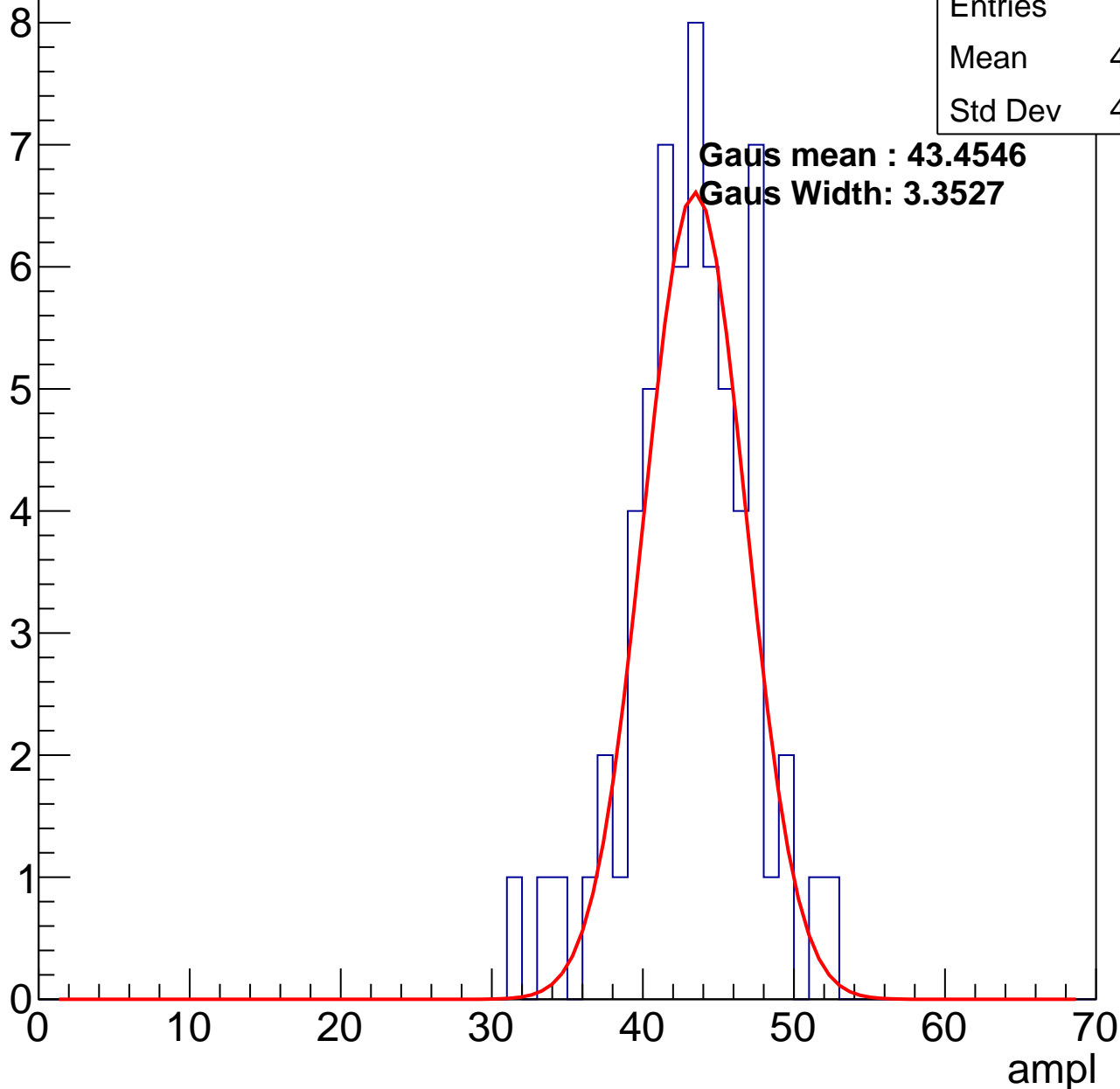
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	42.75
Std Dev	4.004

**Gaus mean : 43.4546**

**Gaus Width: 3.3527**

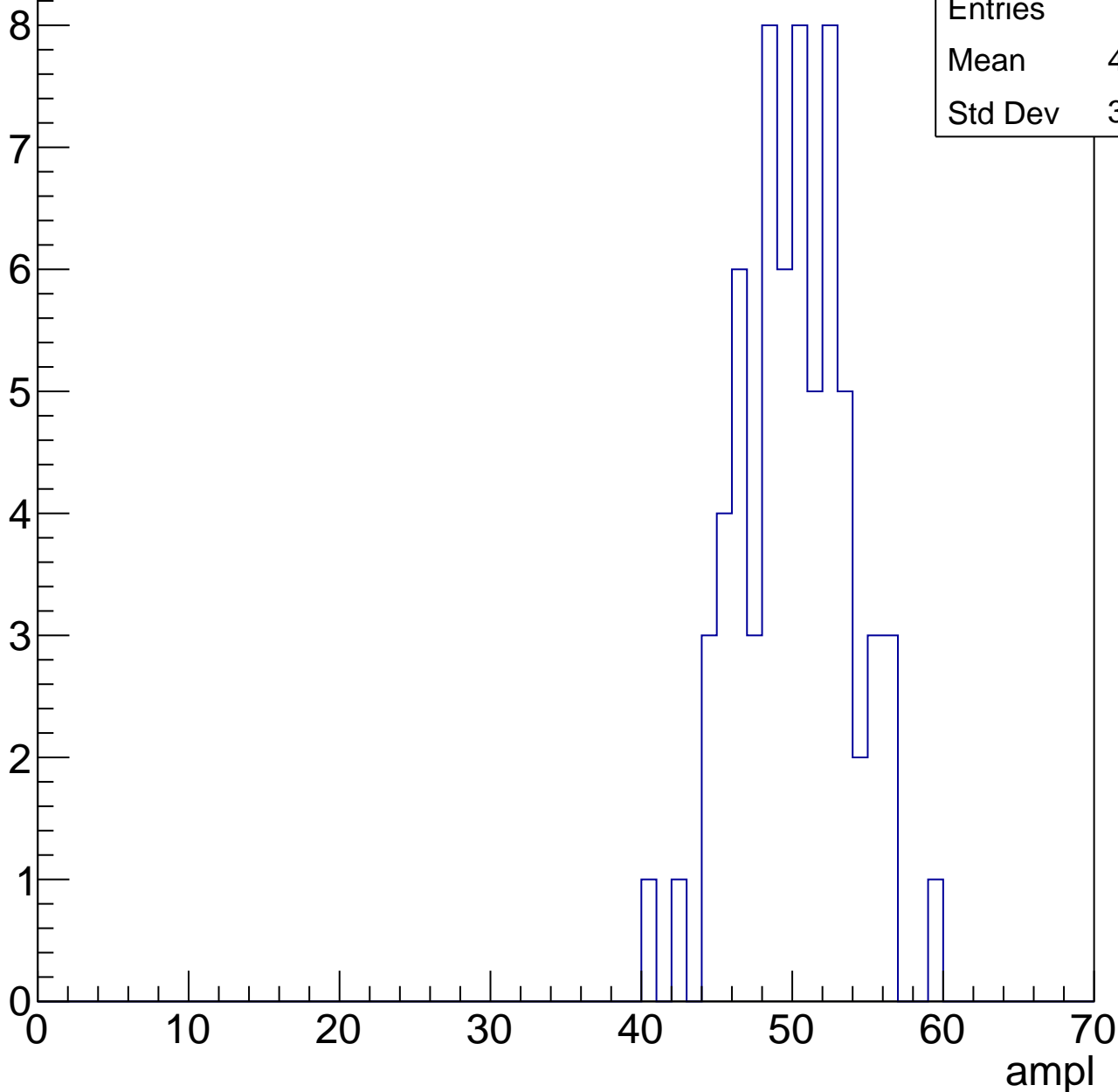


# B1L101S, U16-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	49.63
Std Dev	3.668

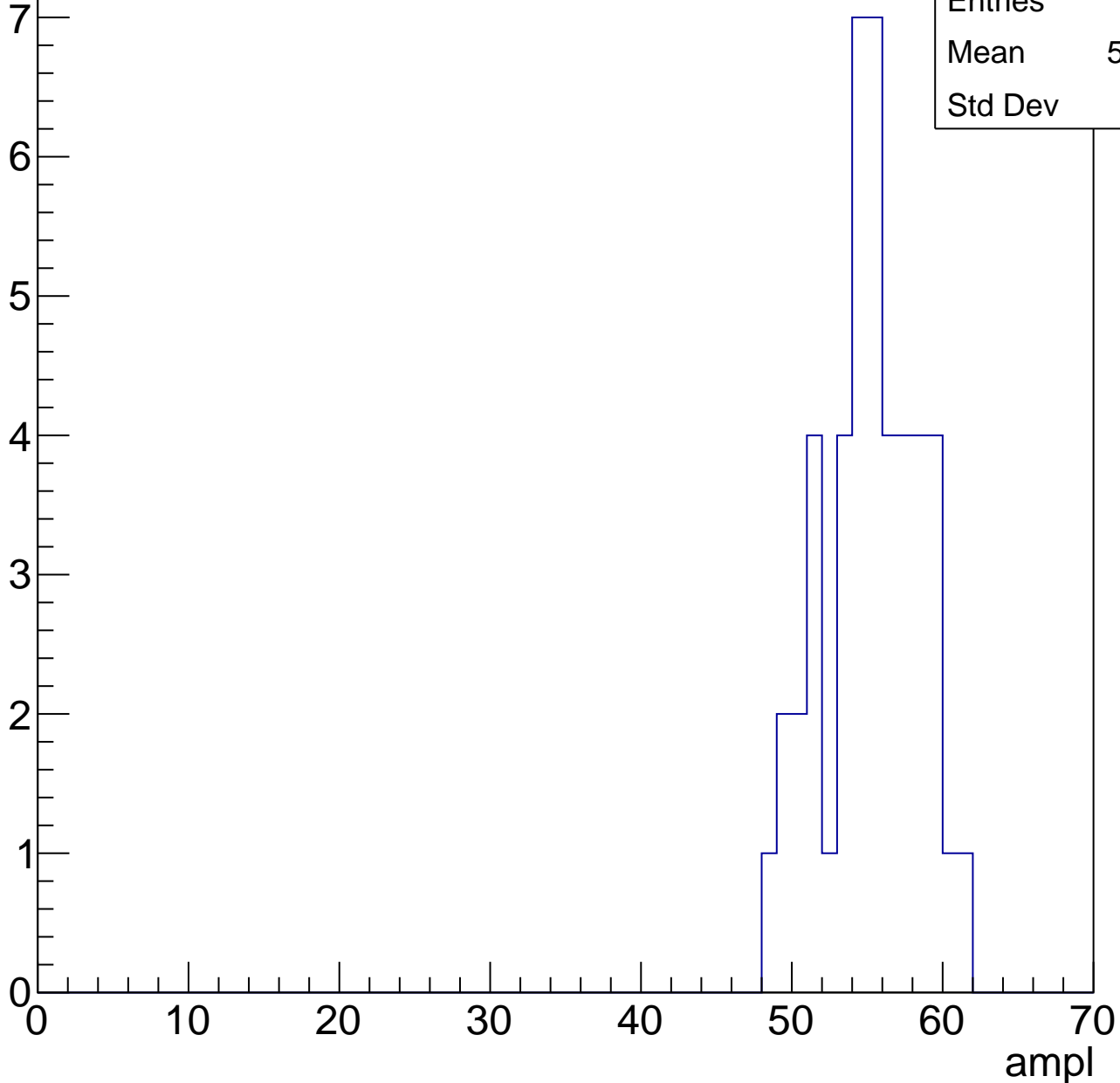


# B1L101S, U16-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	54.74
Std Dev	3.11

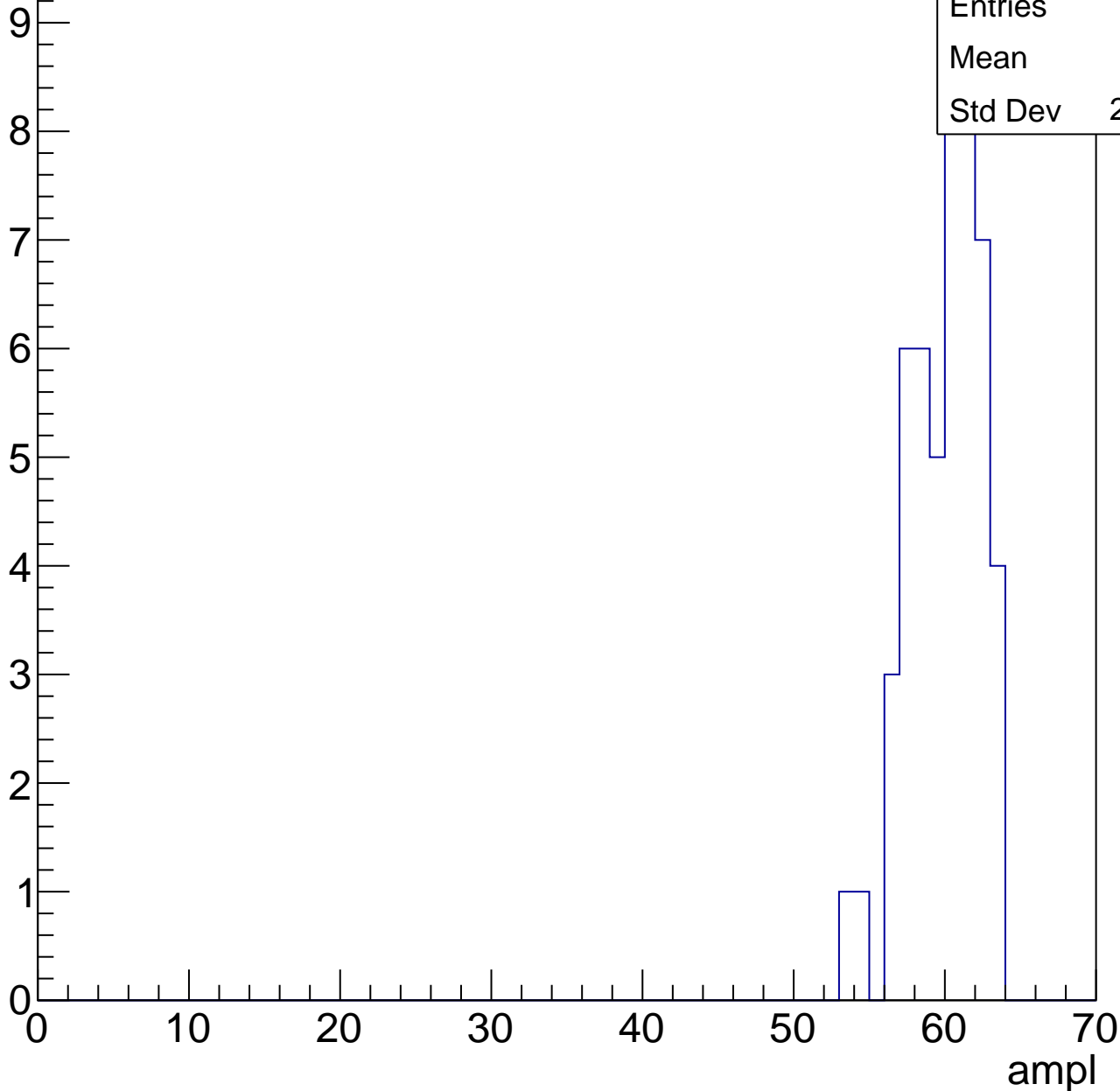


# B1L101S, U16-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	59.5
Std Dev	2.352

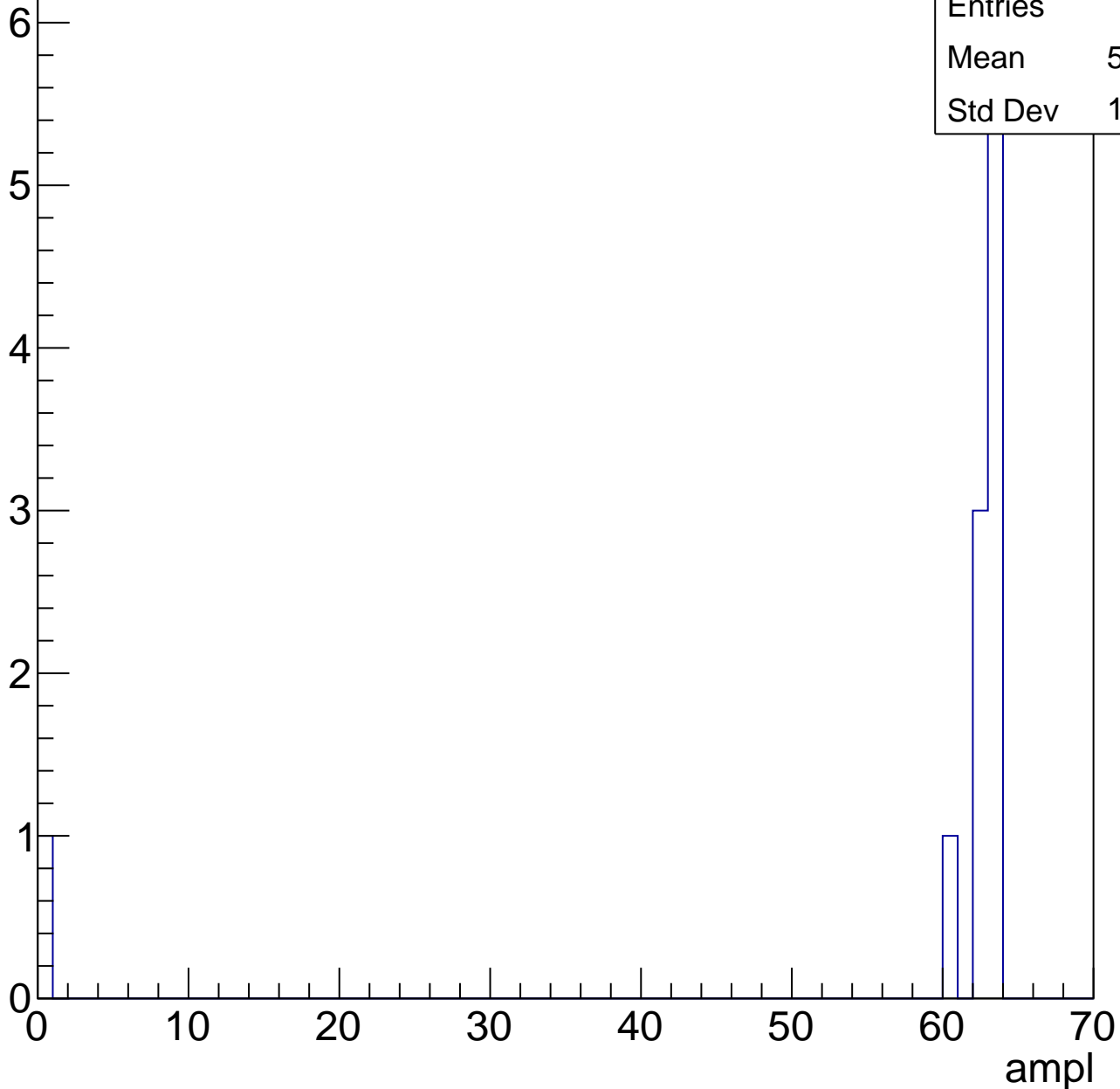


# B1L101S, U16-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	11
Mean	56.73
Std Dev	17.96





# B1L101S, U16-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch3, adc0

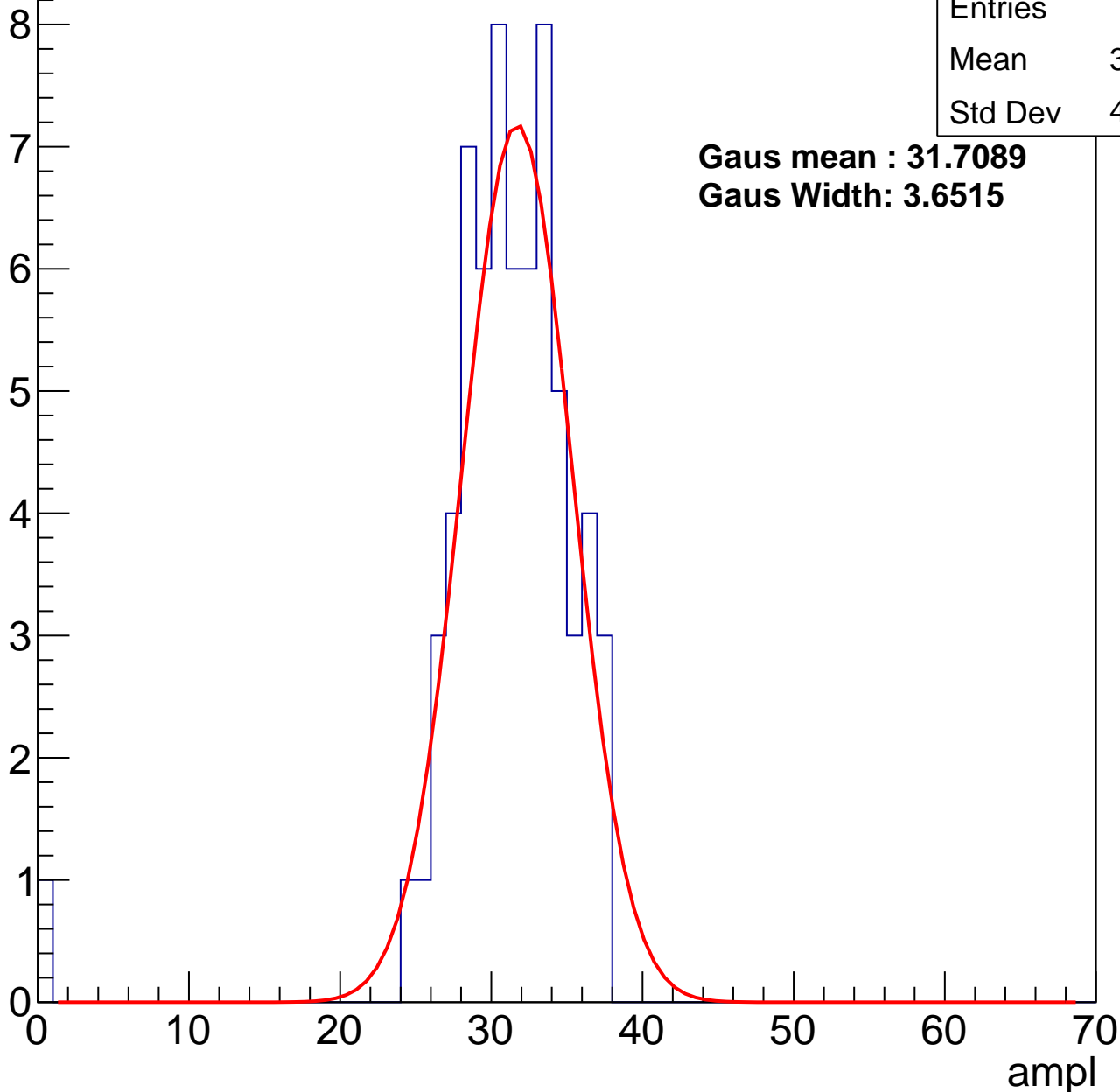
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	30.56
Std Dev	4.933

**Gaus mean : 31.7089**

**Gaus Width: 3.6515**



# B1L101S, U16-ch3, adc1

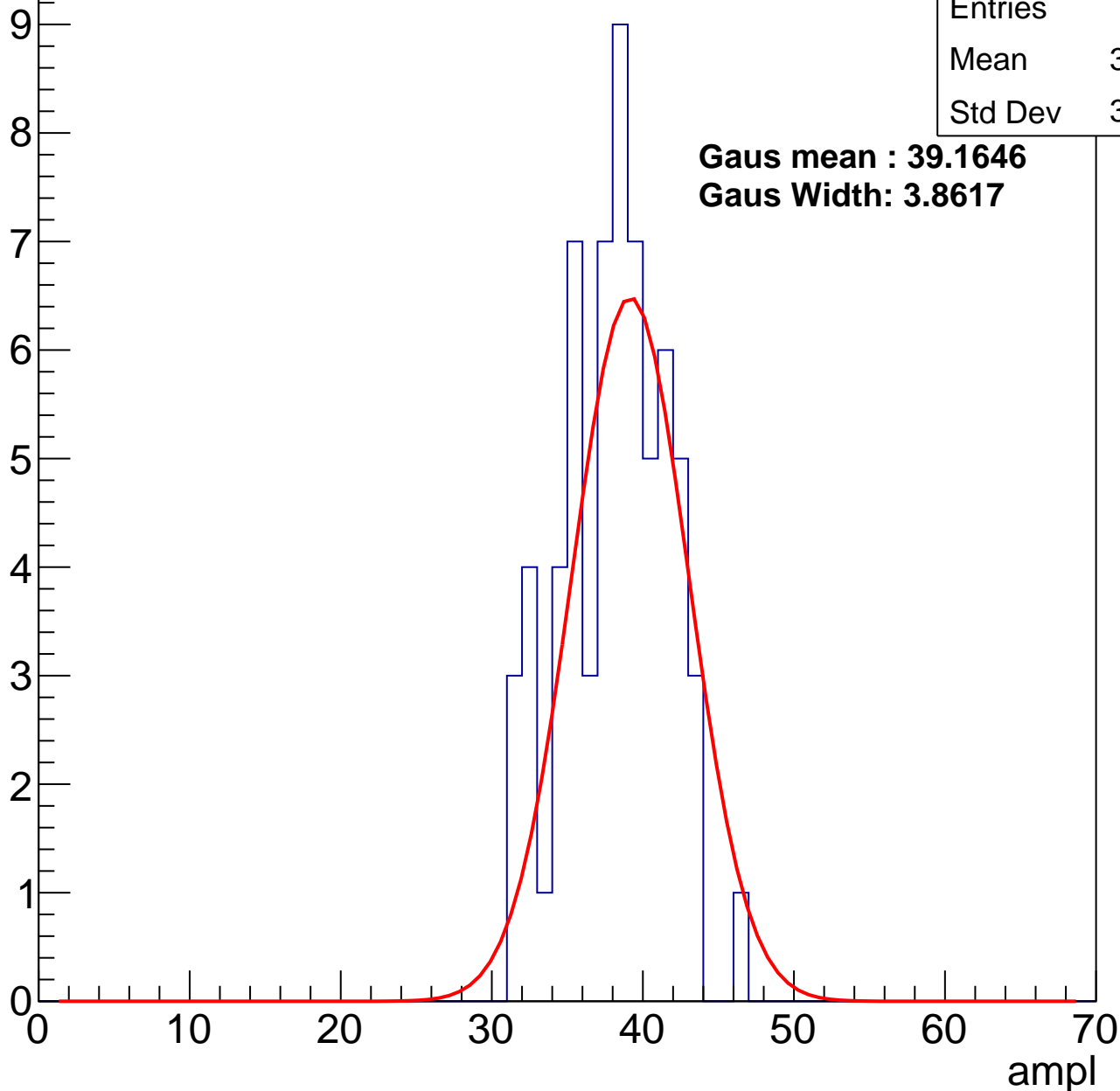
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	37.66
Std Dev	3.407

**Gaus mean : 39.1646**

**Gaus Width: 3.8617**



# B1L101S, U16-ch3, adc2

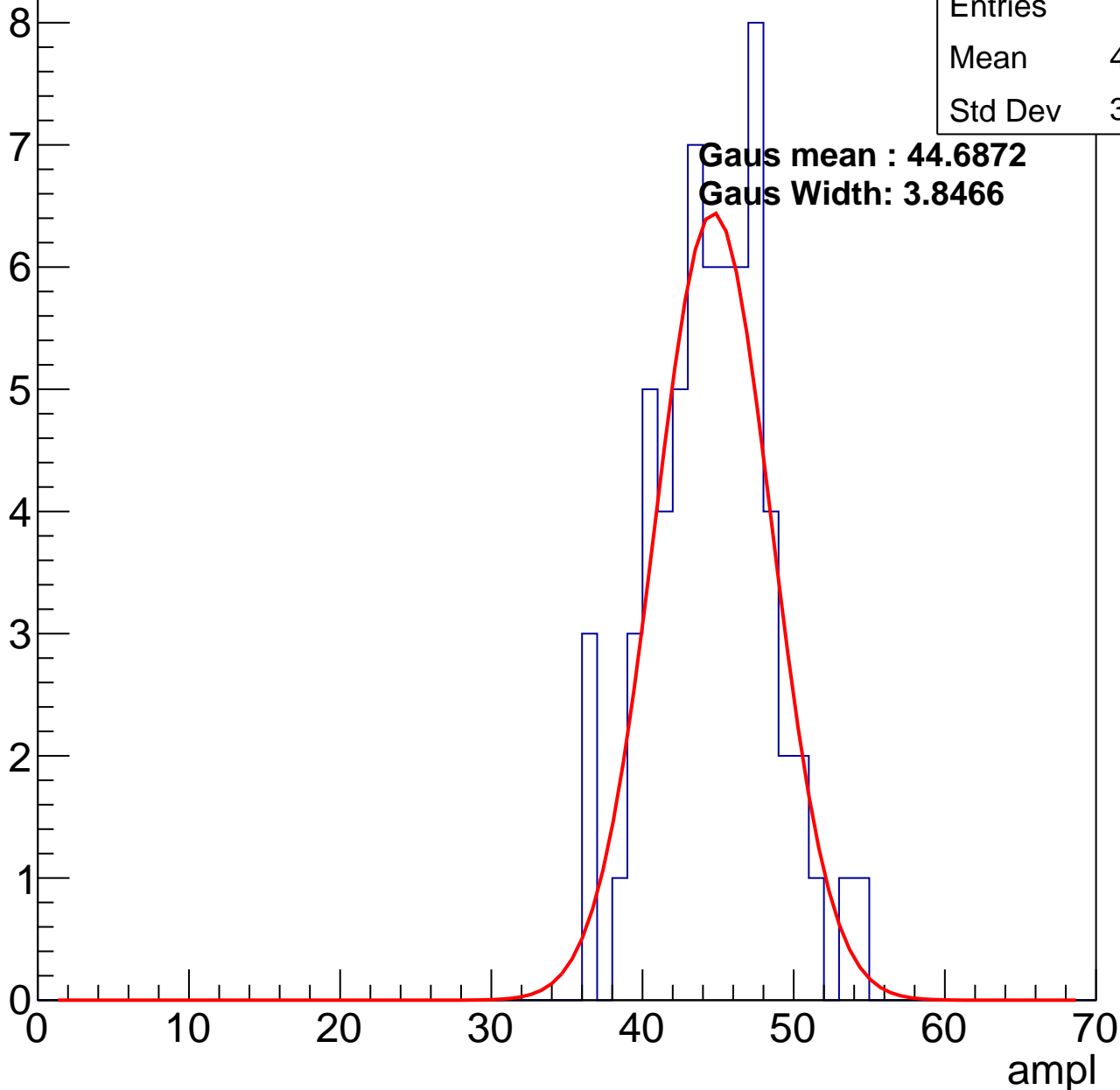
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	44.18
Std Dev	3.847

**Gaus mean : 44.6872**

**Gaus Width: 3.8466**

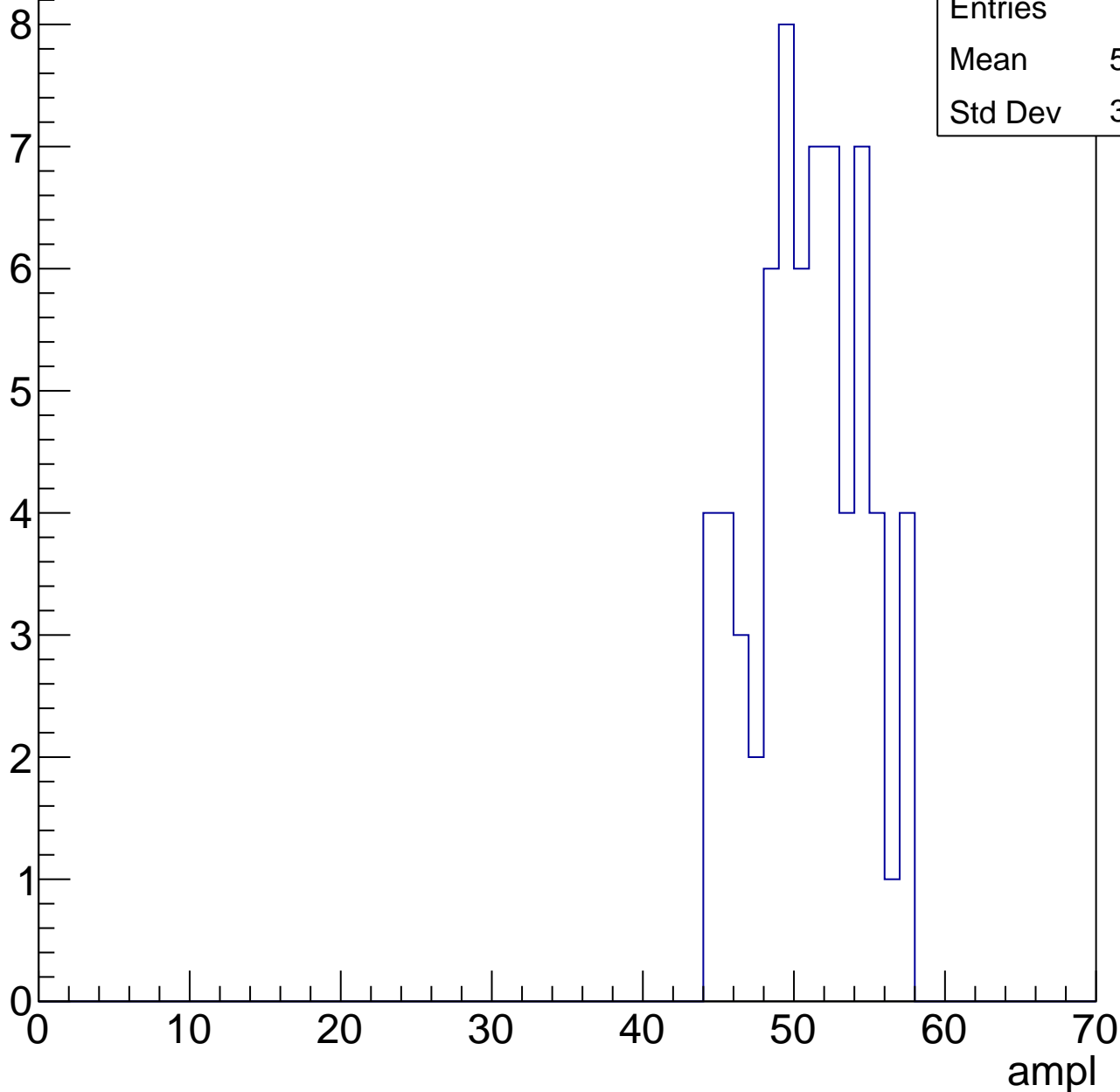


# B1L101S, U16-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	50.49
Std Dev	3.542



# B1L101S, U16-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	61
Mean	56.89
Std Dev	3.214

Entry

10

8

6

4

2

0

0

10

20

30

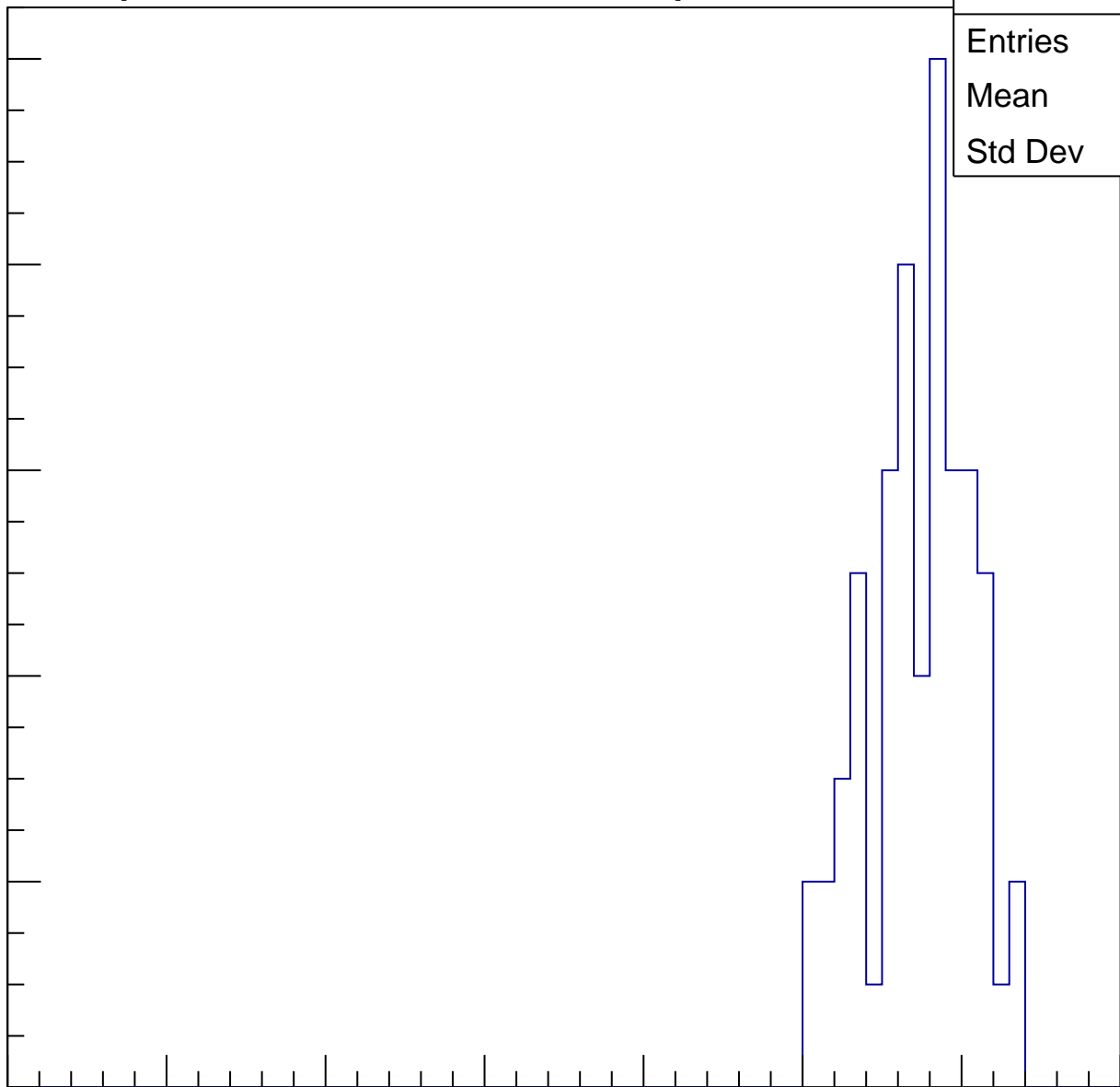
40

50

60

70

ampl

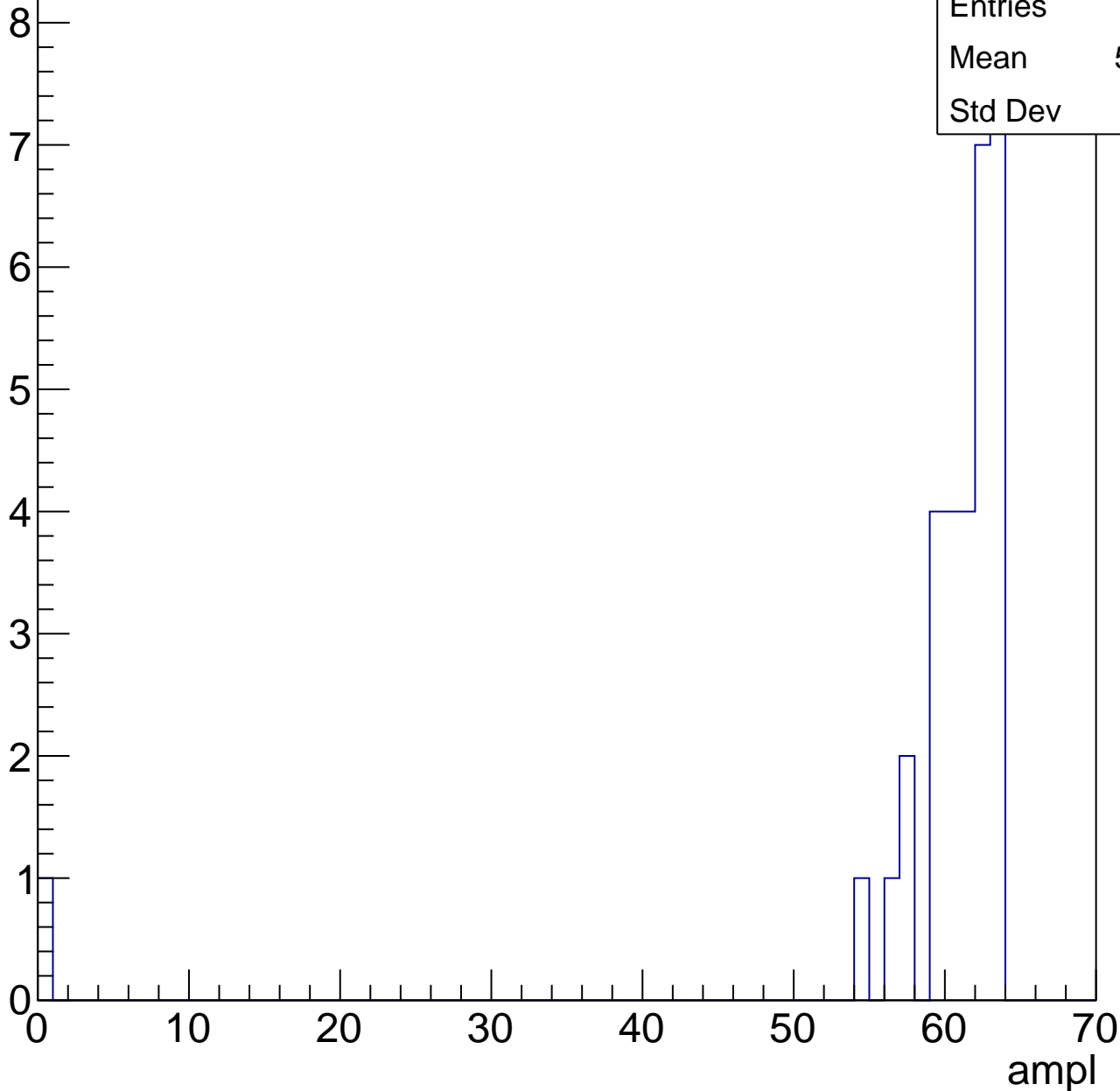


# B1L101S, U16-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	32
Mean	58.81
Std Dev	10.8



# B1L101S, U16-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

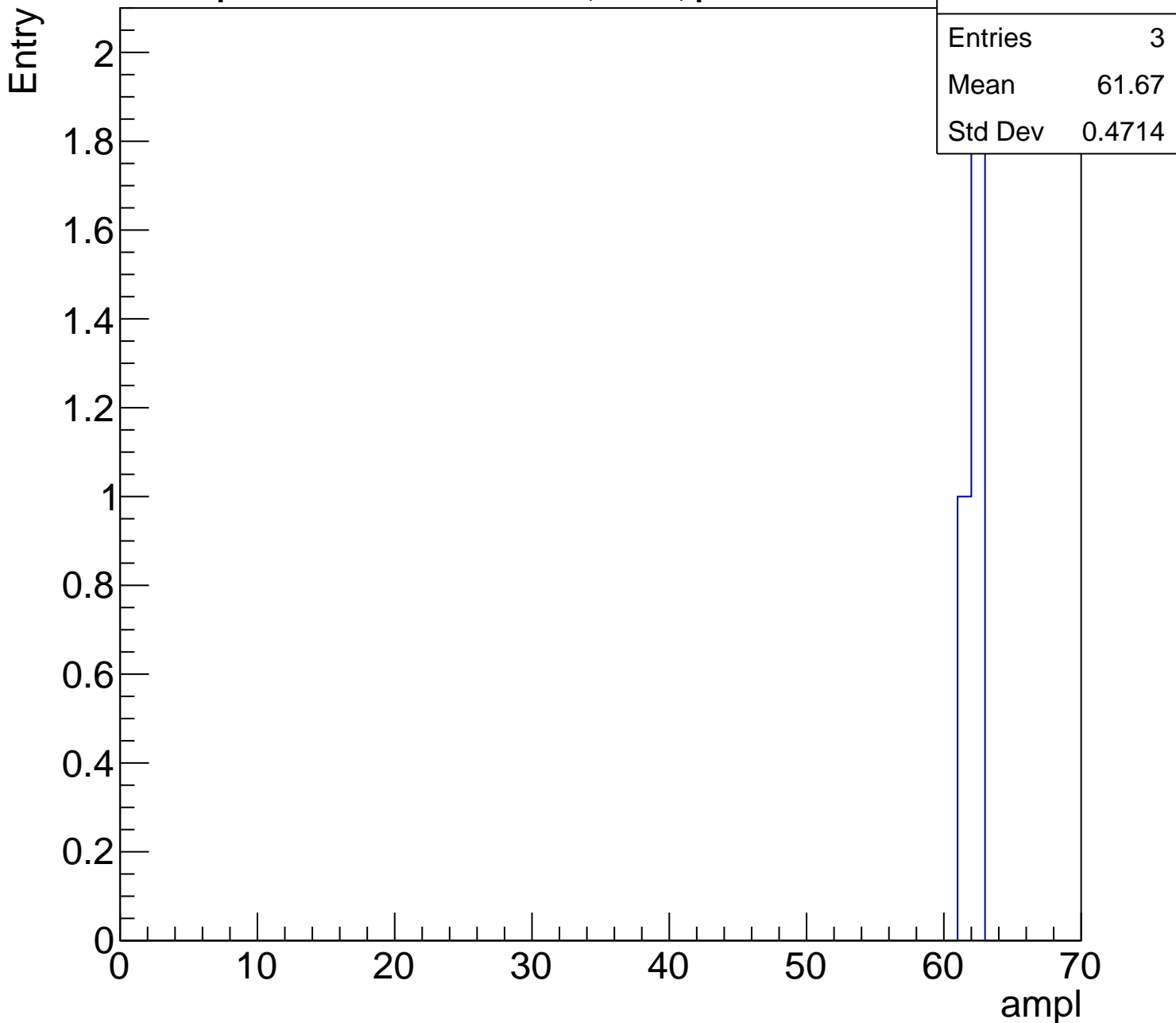
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	61.67
Std Dev	0.4714

0 10 20 30 40 50 60 70

ampl

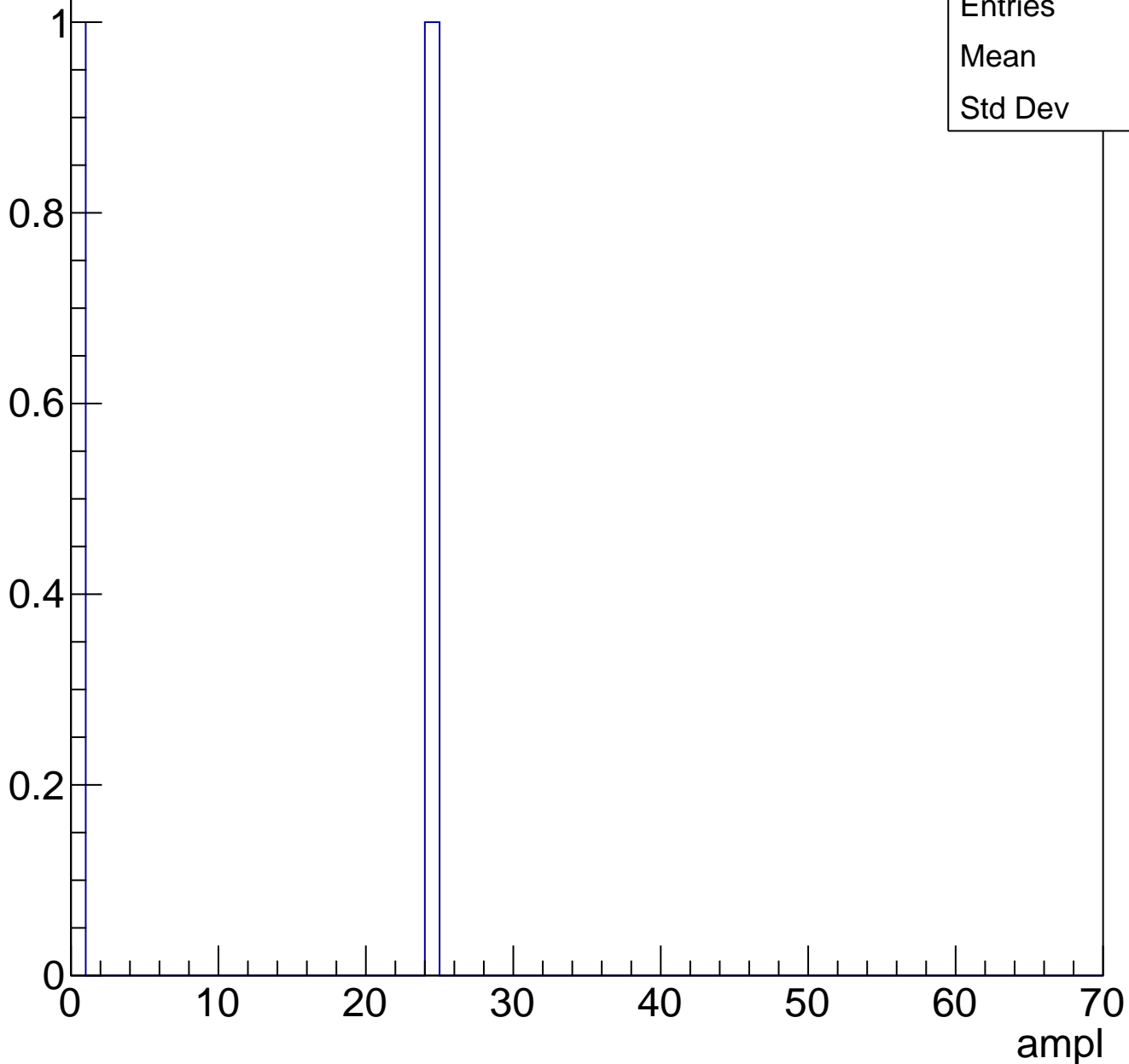




# B1L101S, U16-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch4, adc0

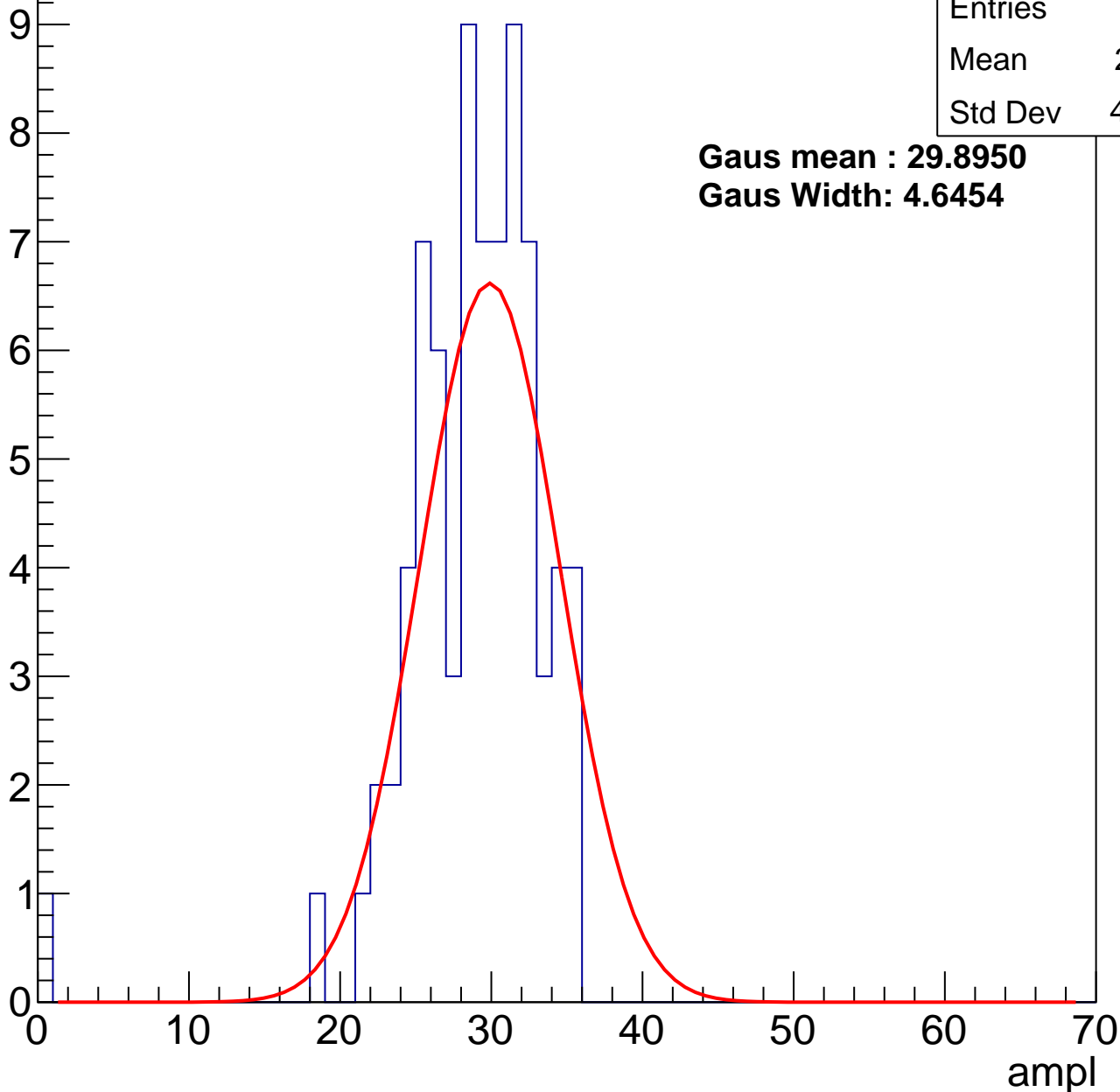
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	28.31
Std Dev	4.894

**Gaus mean : 29.8950**

**Gaus Width: 4.6454**



# B1L101S, U16-ch4, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	55
Mean	35.27
Std Dev	3.066

**Gaus mean : 36.1940**

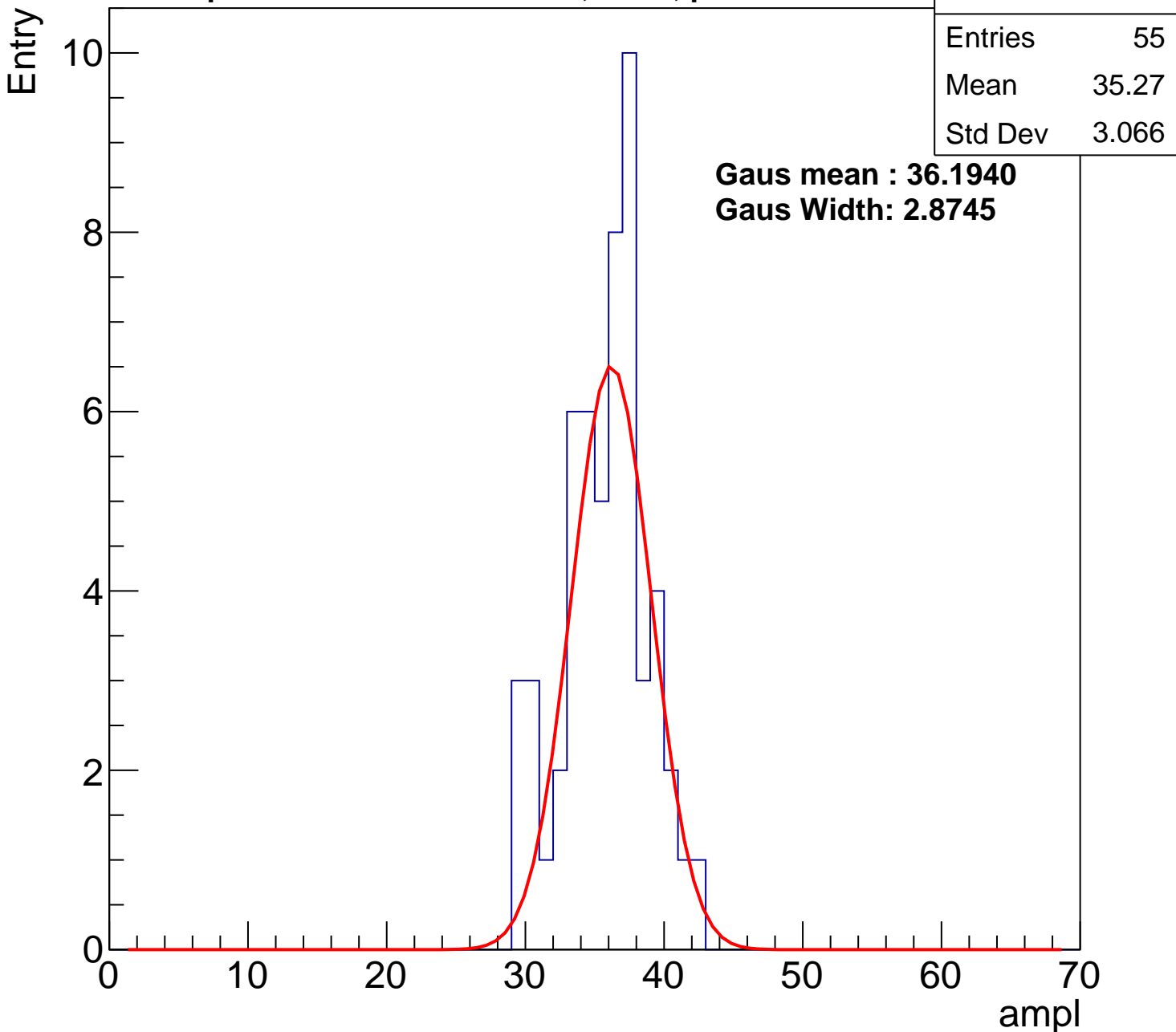
**Gaus Width: 2.8745**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch4, adc2

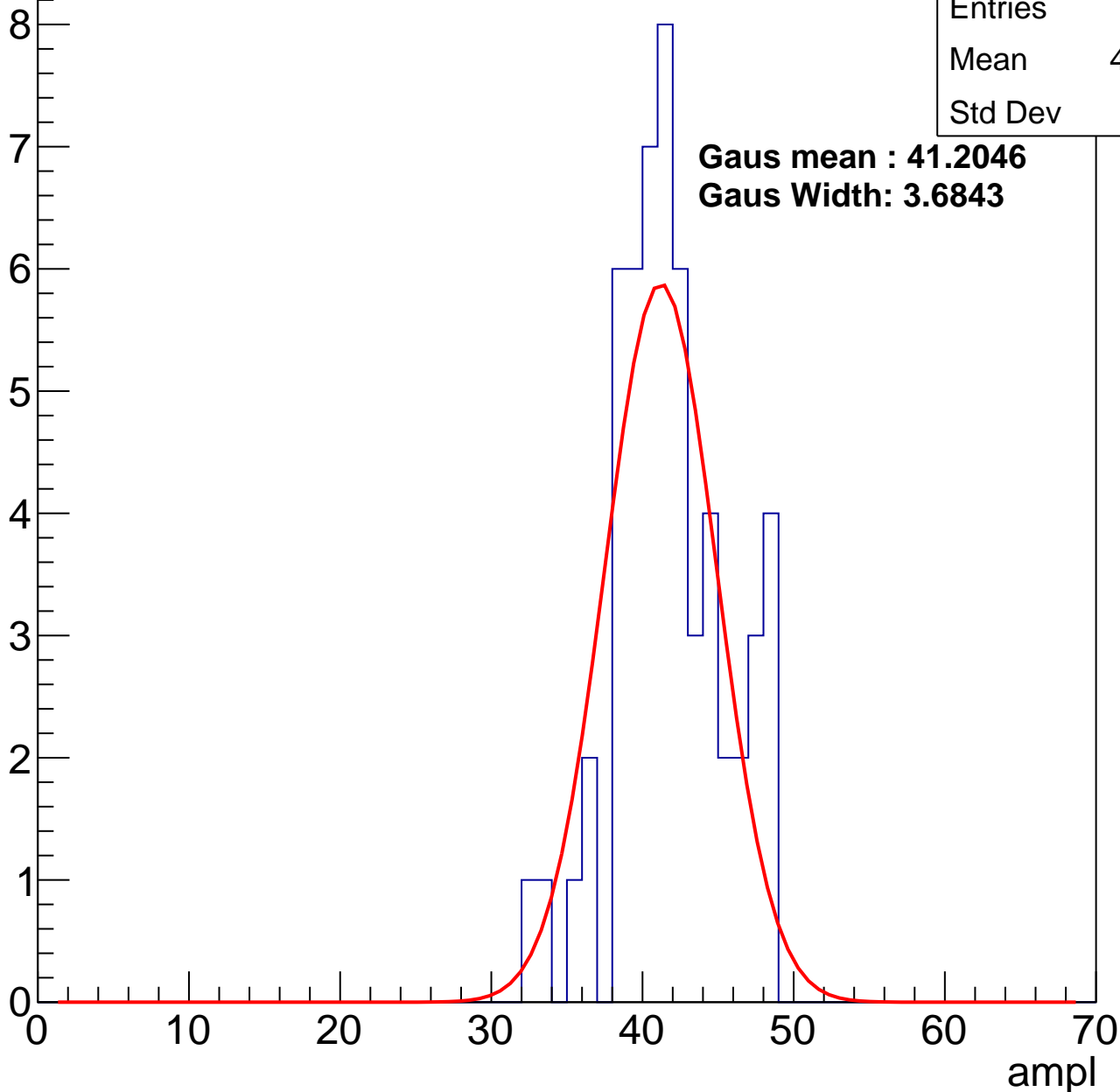
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	41.32
Std Dev	3.66

**Gaus mean : 41.2046**

**Gaus Width: 3.6843**

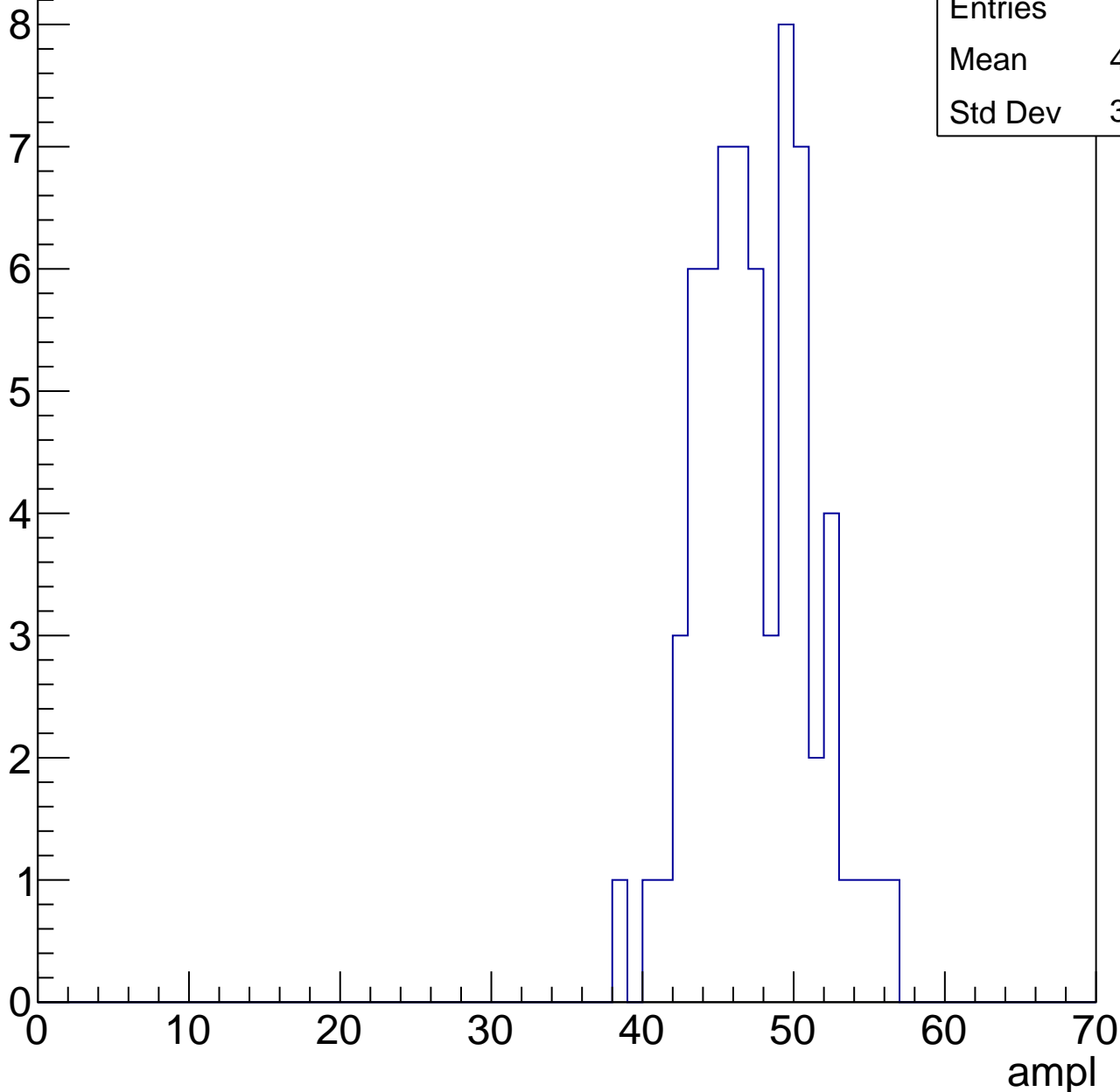


# B1L101S, U16-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

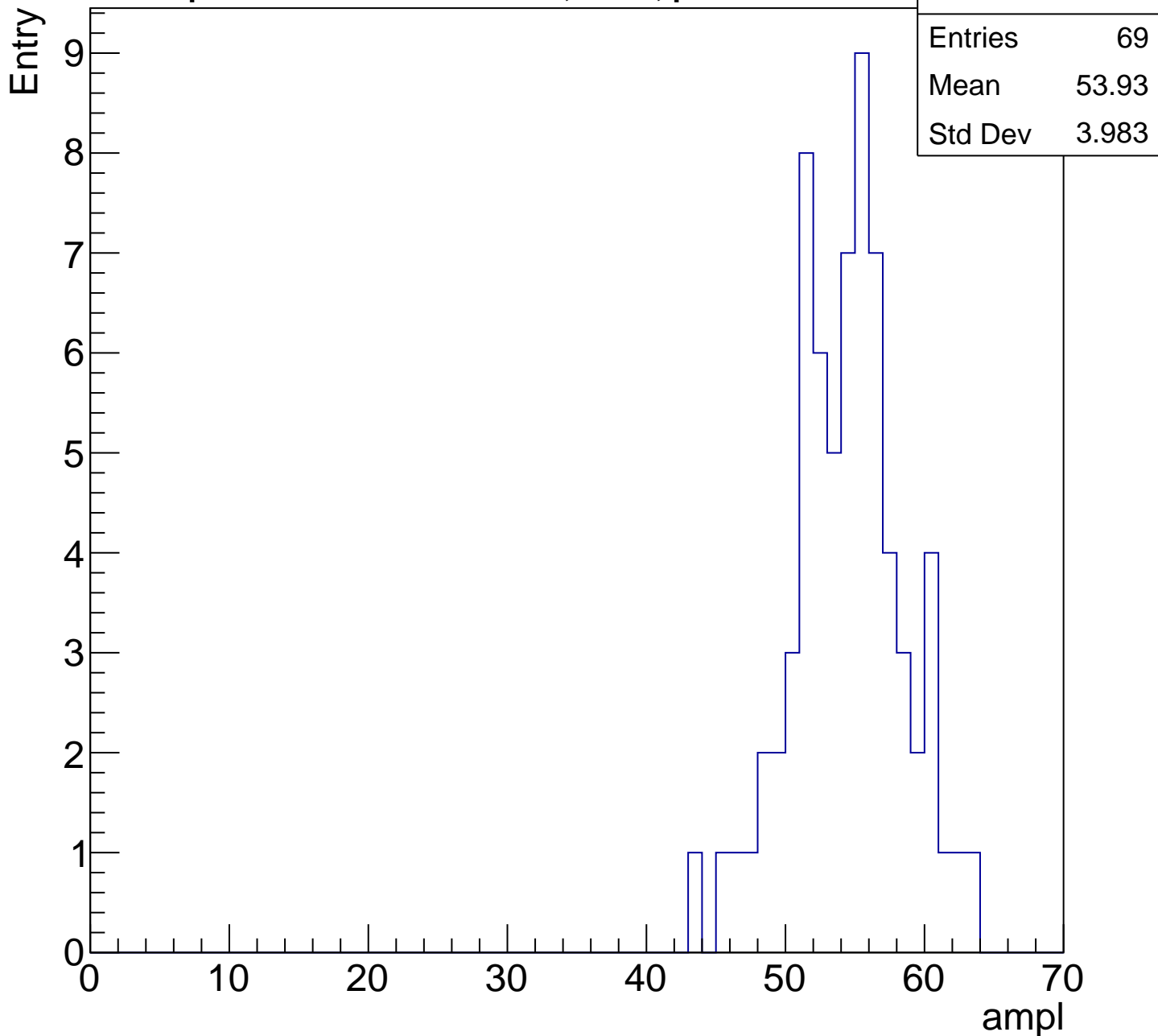
Entry

Entries	66
Mean	46.97
Std Dev	3.664



# B1L101S, U16-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

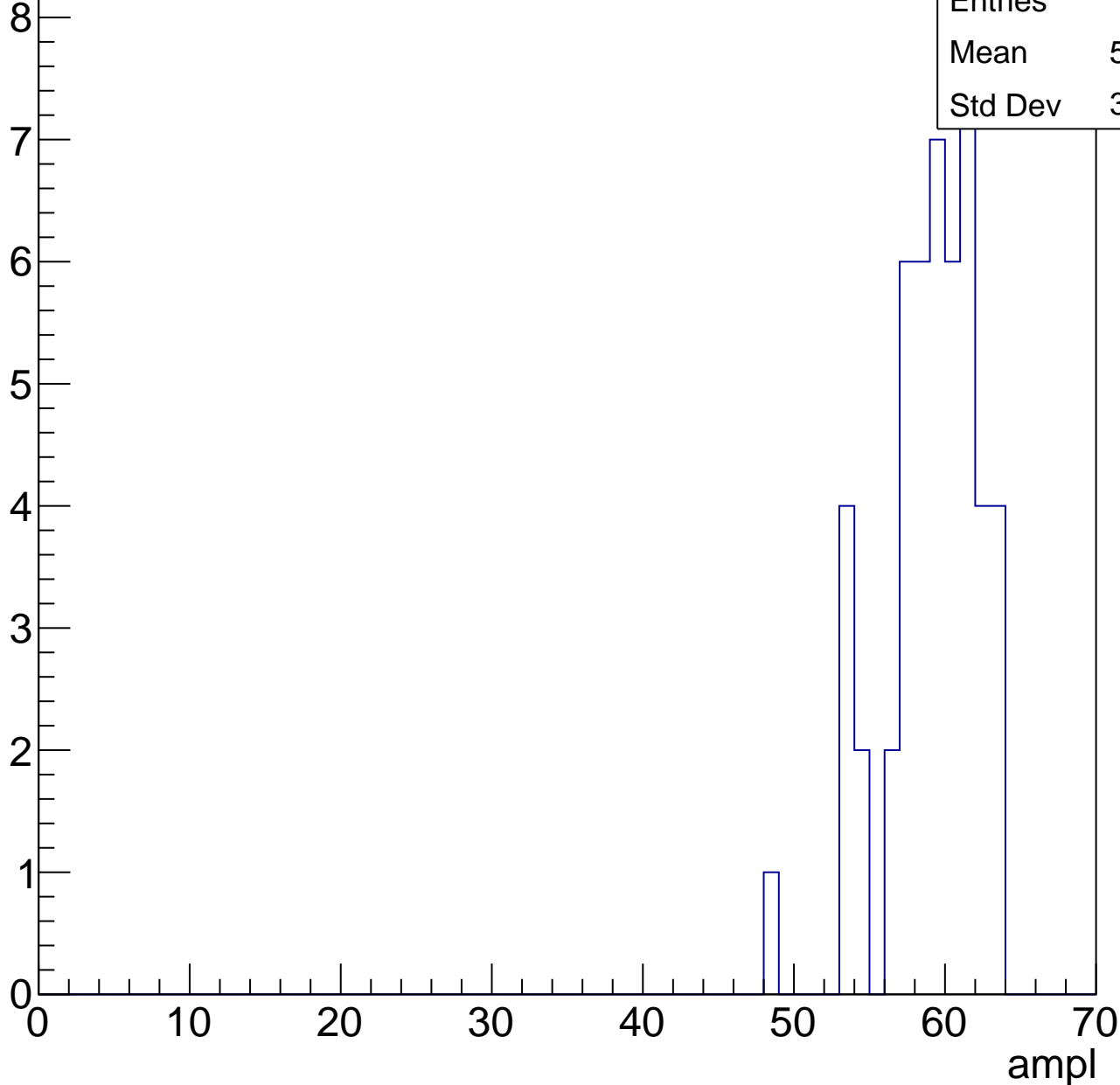


# B1L101S, U16-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	58.62
Std Dev	3.143

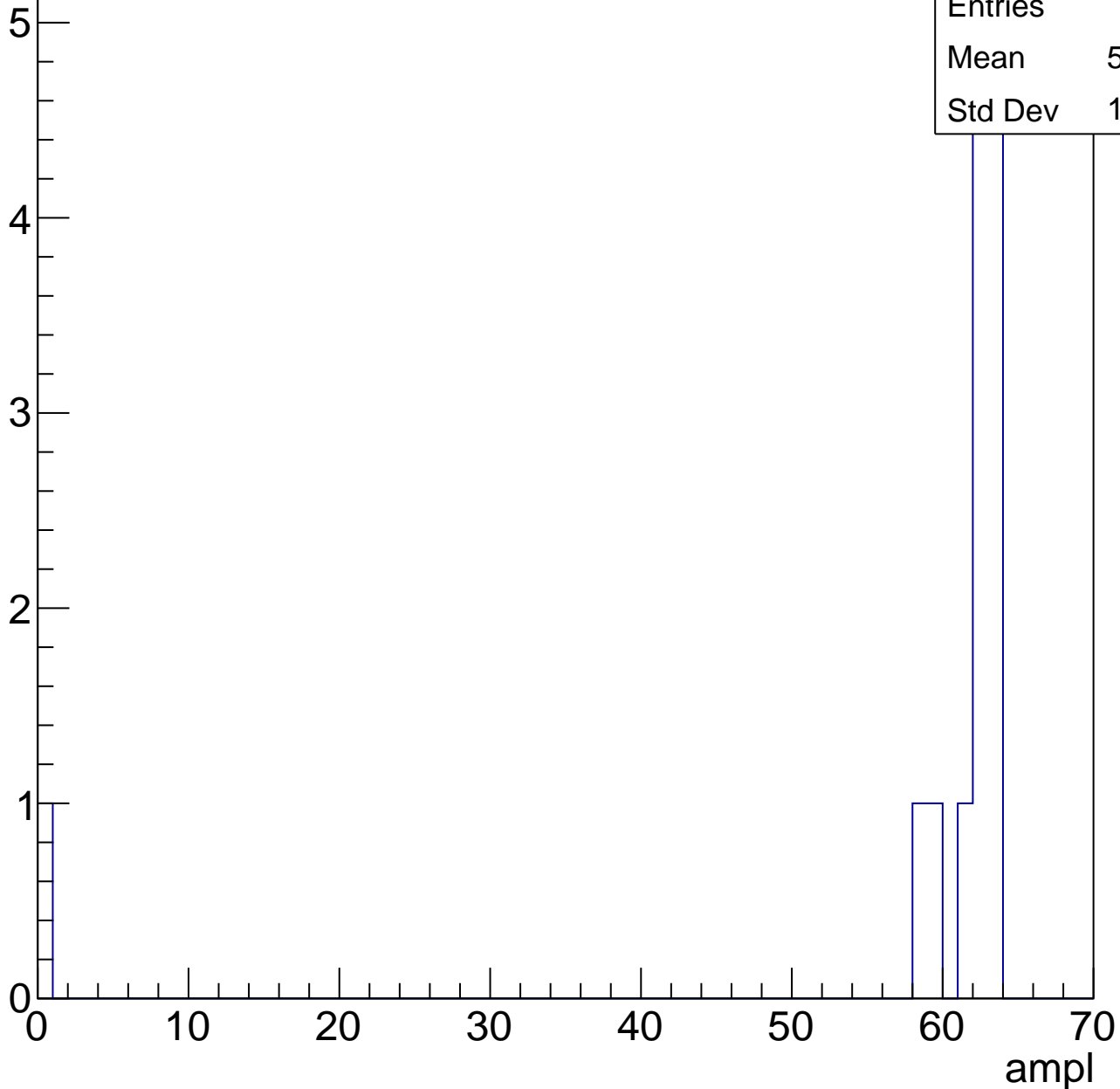


# B1L101S, U16-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	14
Mean	57.36
Std Dev	15.98





# B1L101S, U16-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch5, adc0

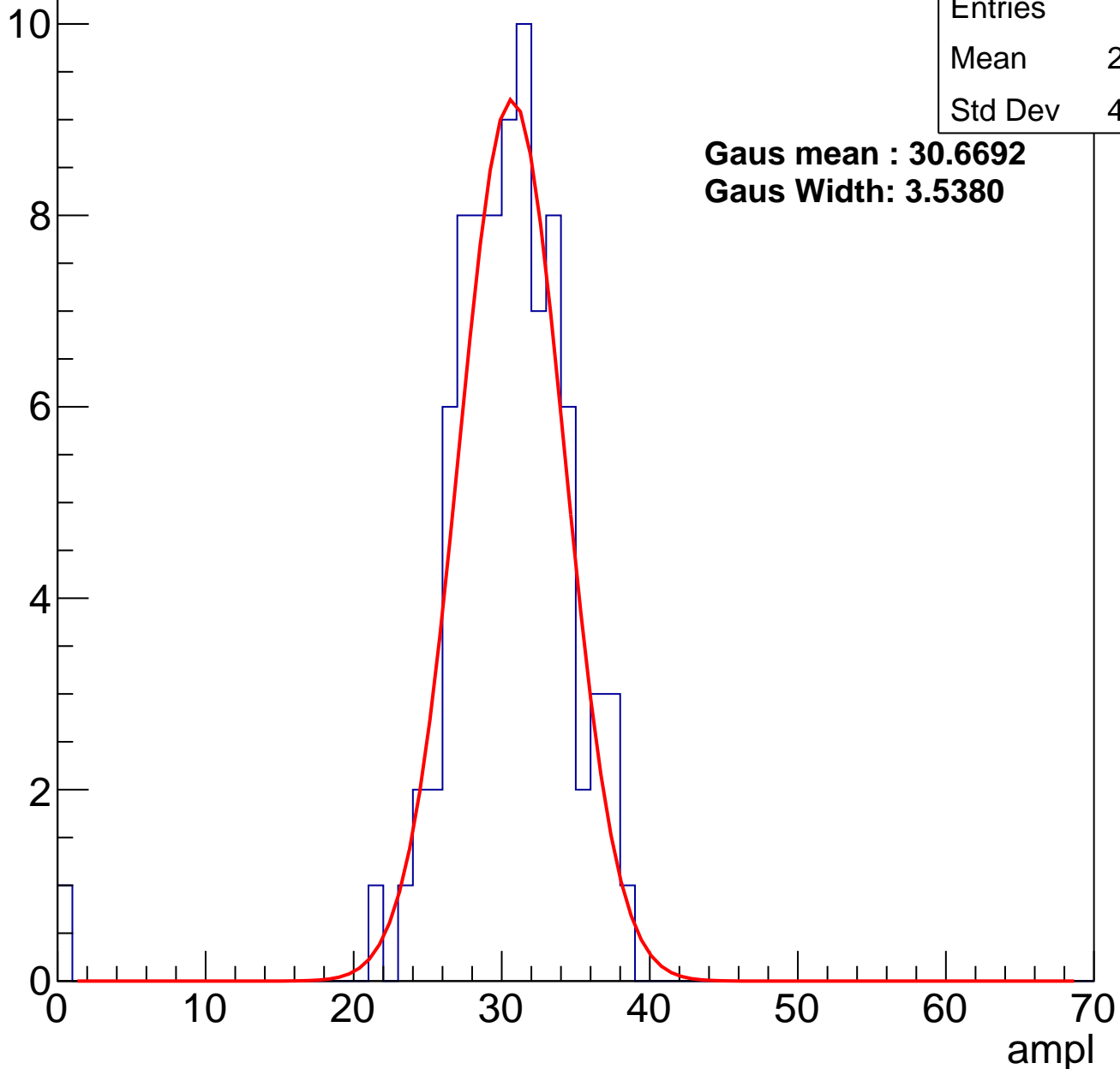
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	86
Mean	29.87
Std Dev	4.742

**Gaus mean : 30.6692**

**Gaus Width: 3.5380**

Entry



# B1L101S, U16-ch5, adc1

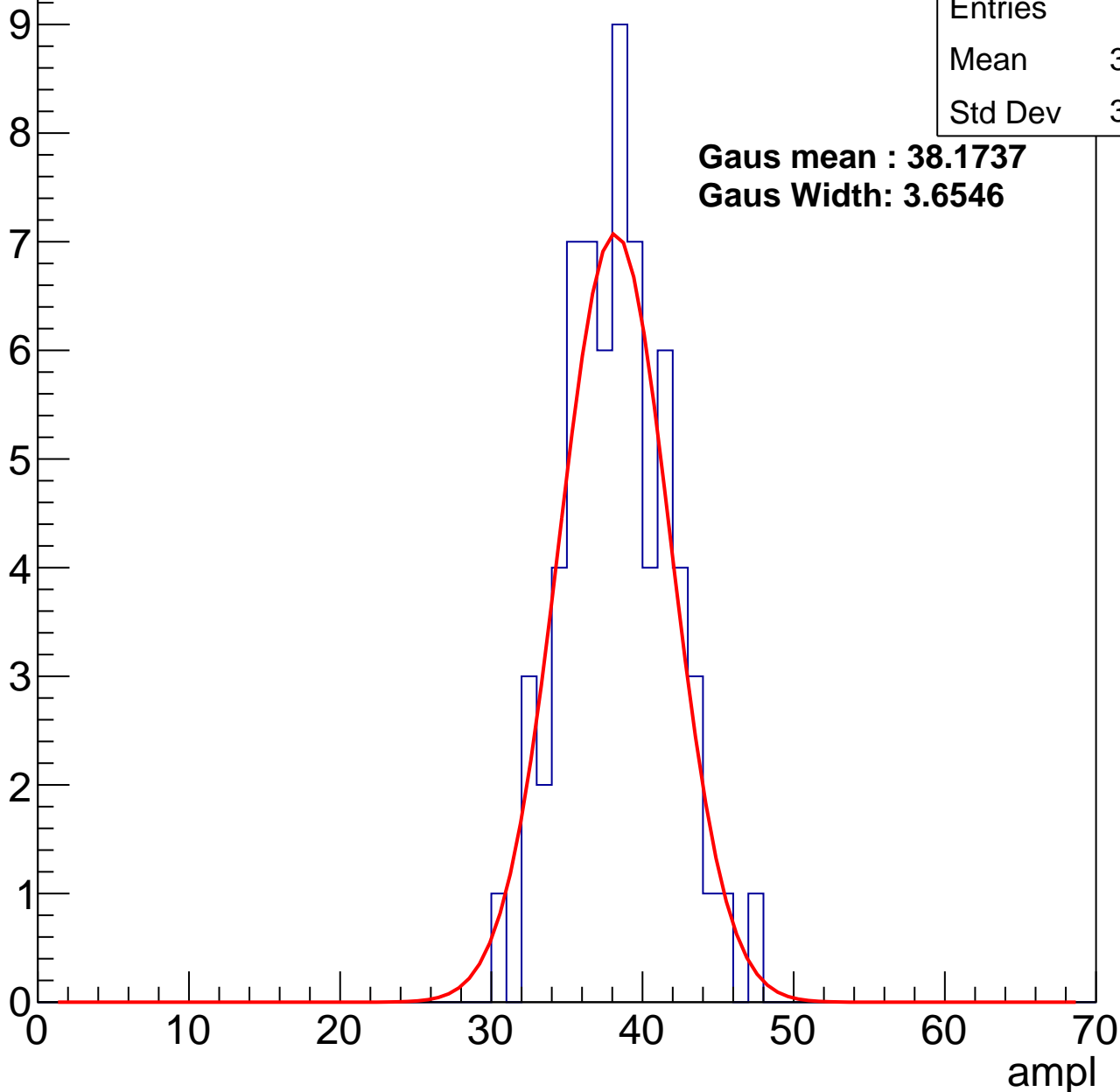
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	37.89
Std Dev	3.403

**Gaus mean : 38.1737**

**Gaus Width: 3.6546**



# B1L101S, U16-ch5, adc2

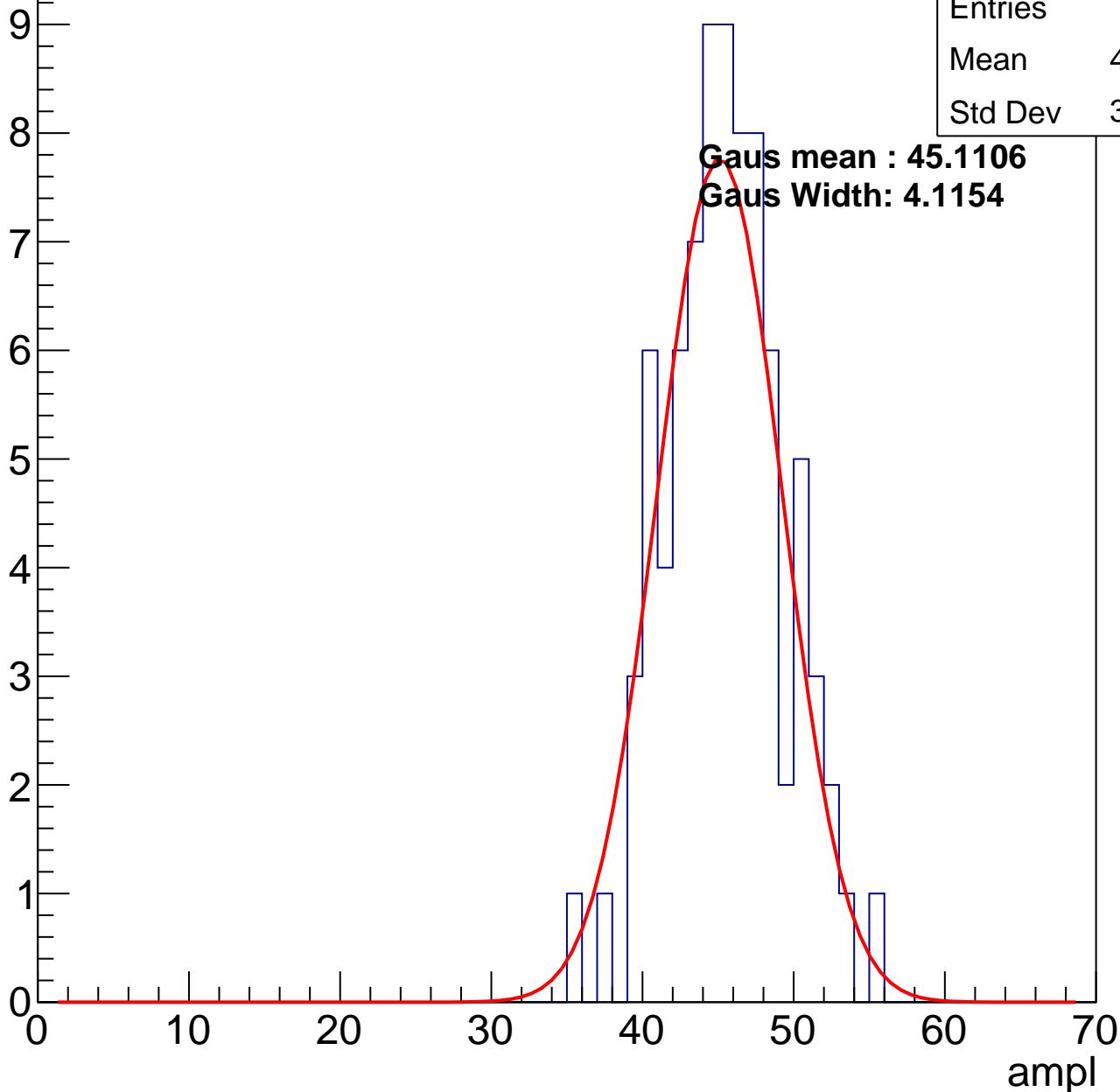
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	45.02
Std Dev	3.822

**Gaus mean : 45.1106**

**Gaus Width: 4.1154**

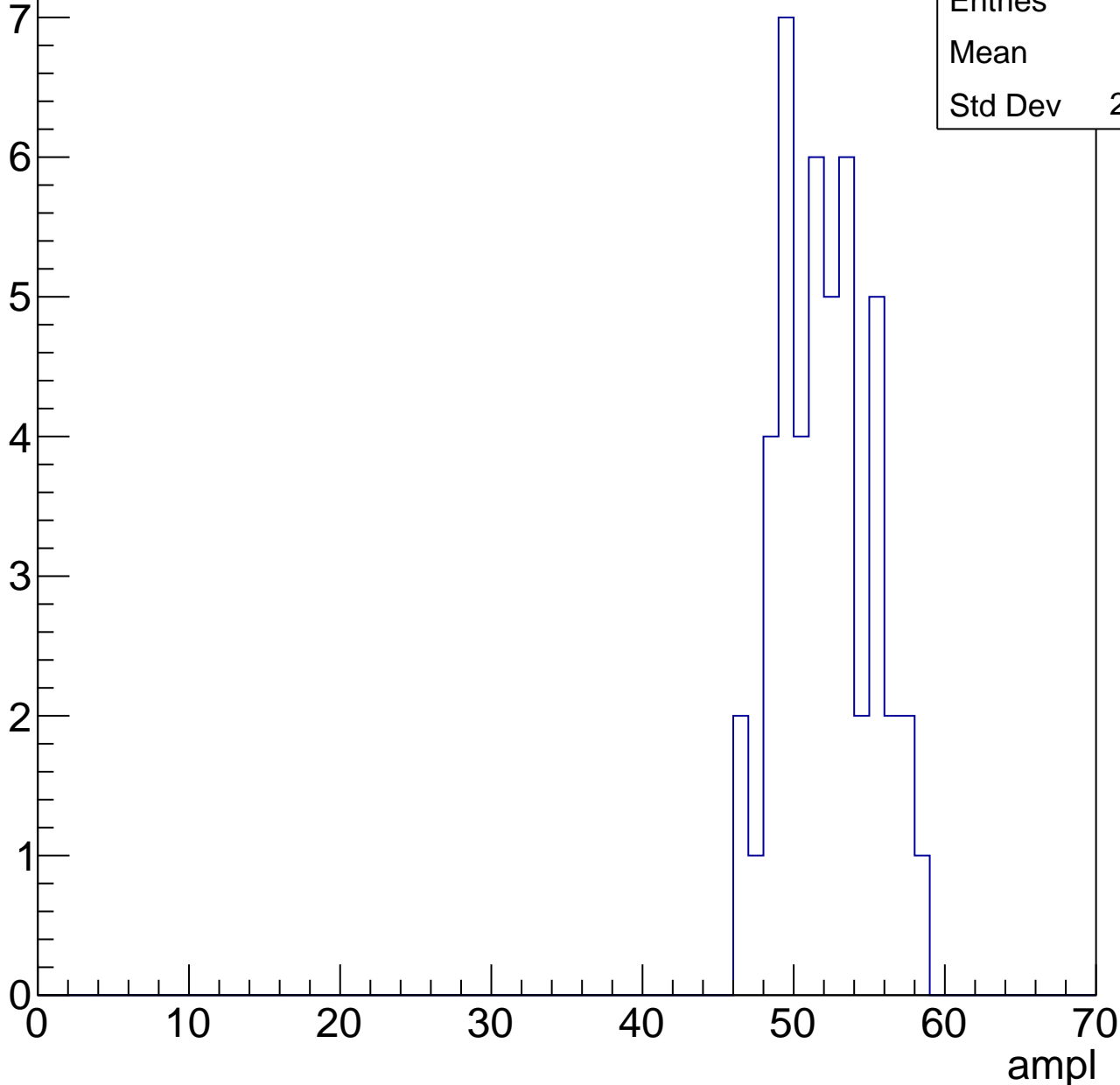


# B1L101S, U16-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

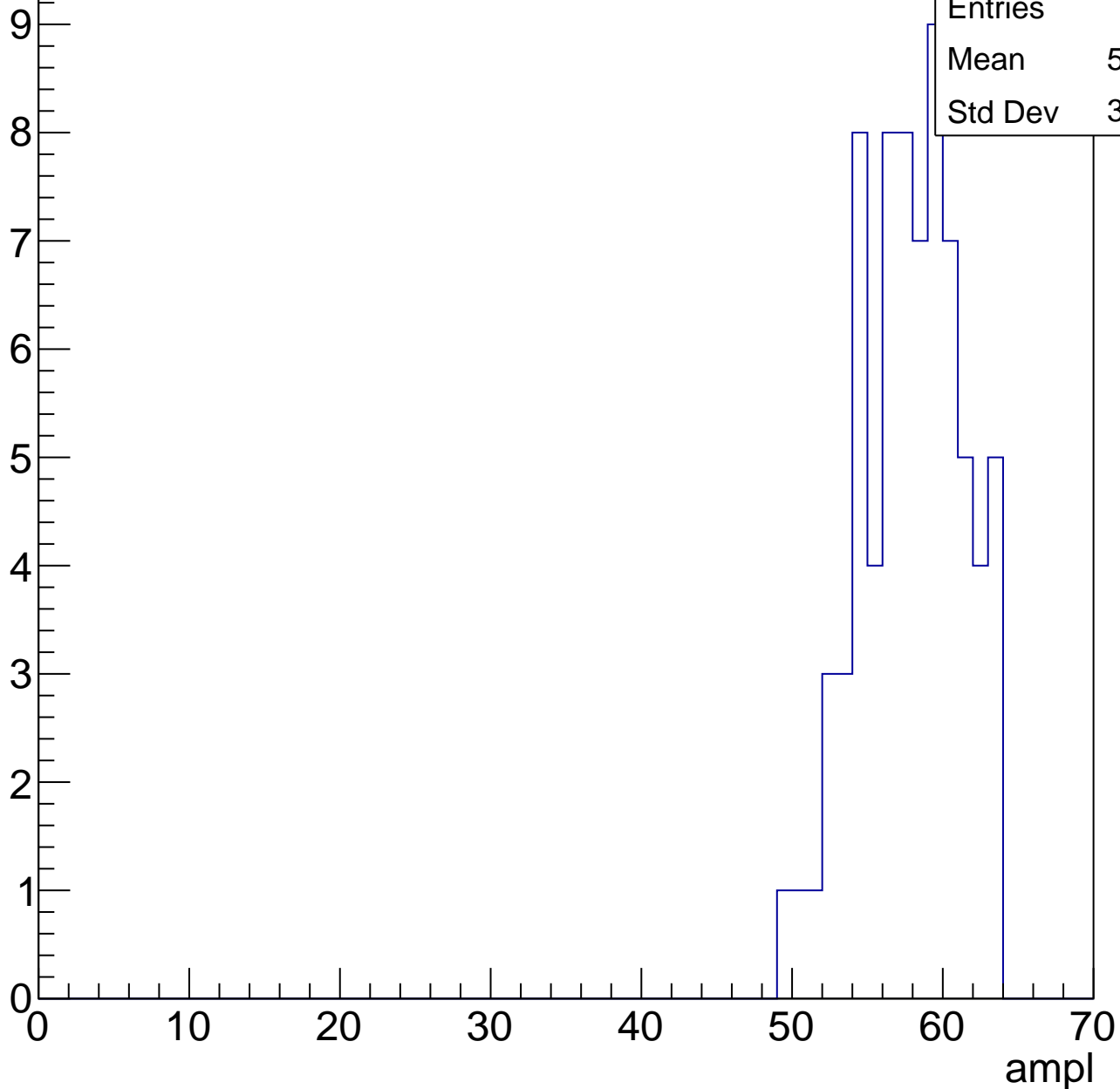
Entries	47
Mean	51.6
Std Dev	2.973



# B1L101S, U16-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



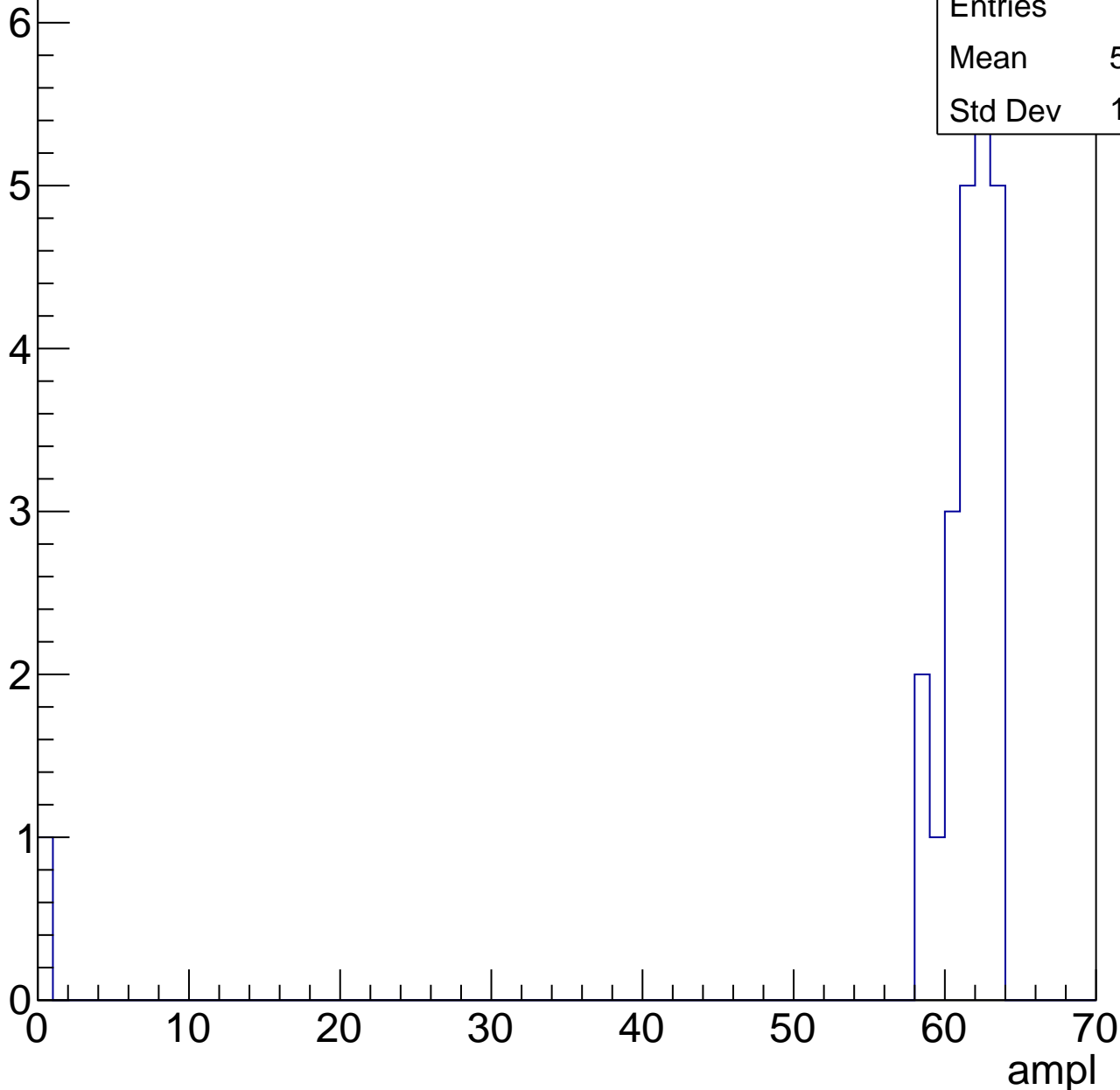
Entries	74
Mean	57.38
Std Dev	3.336

# B1L101S, U16-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	23
Mean	58.57
Std Dev	12.57



# B1L101S, U16-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L101S, U16-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U16-ch6, adc0

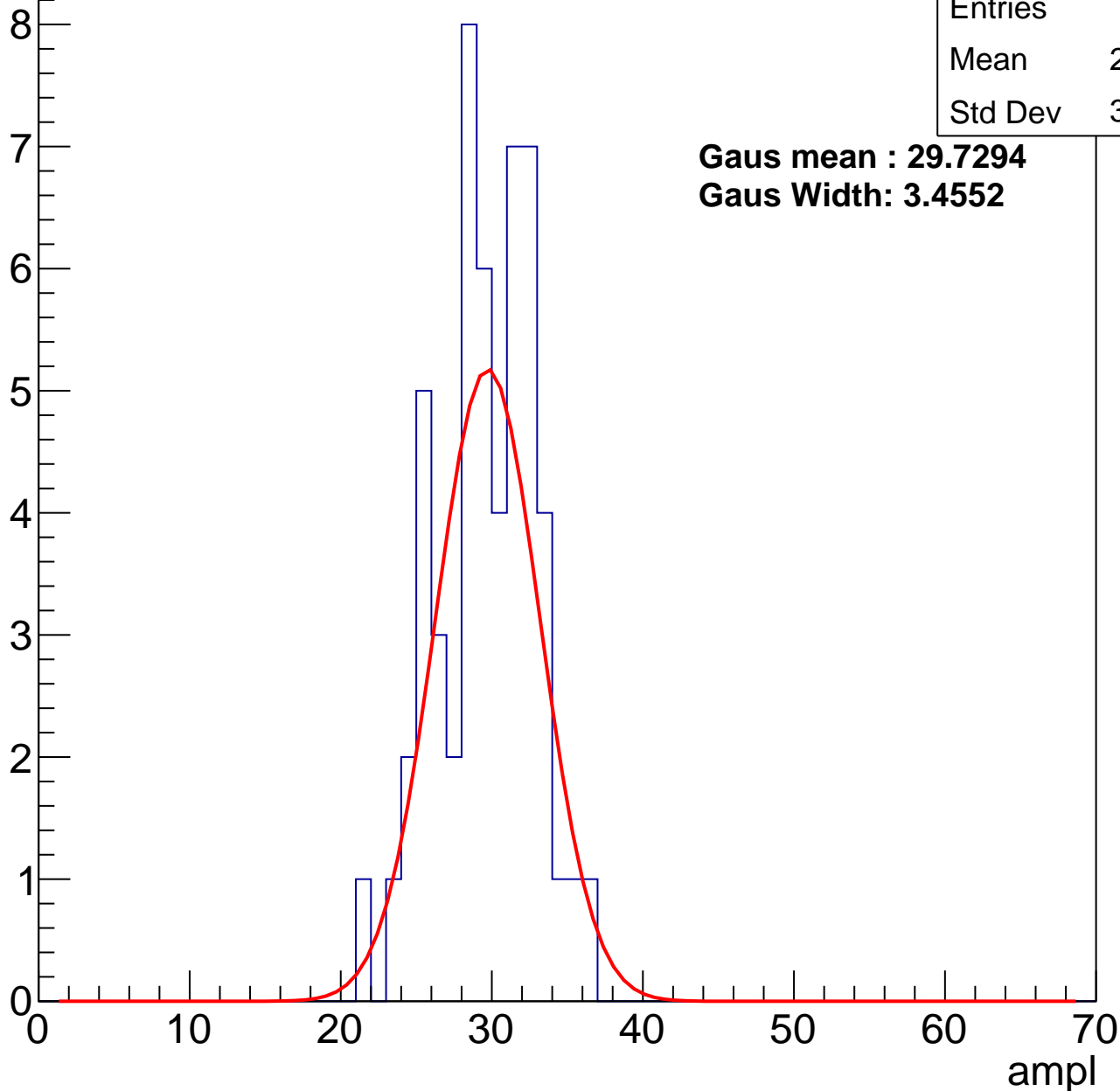
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	29.15
Std Dev	3.194

**Gaus mean : 29.7294**

**Gaus Width: 3.4552**



# B1L101S, U16-ch6, adc1

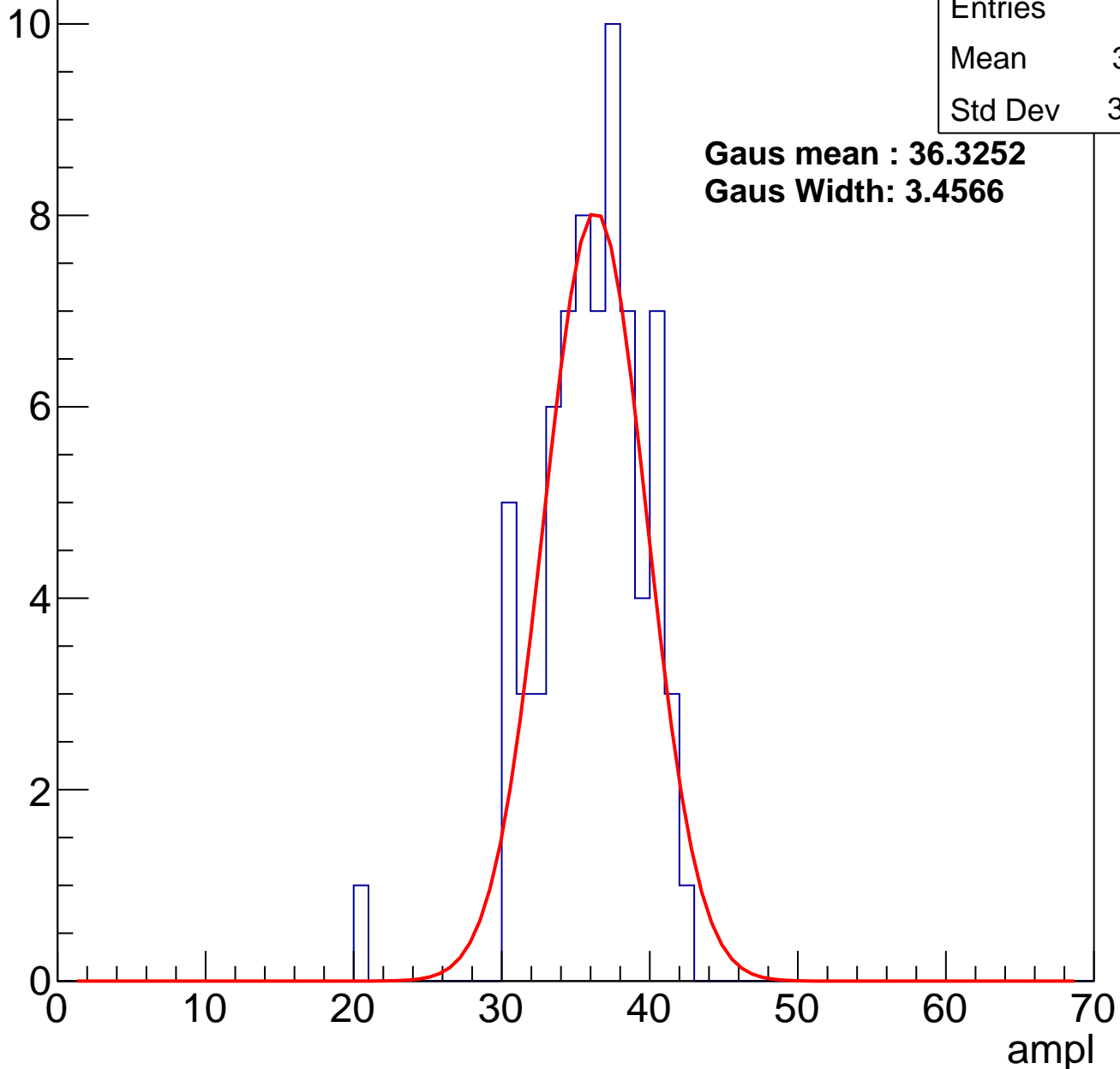
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	72
Mean	35.61
Std Dev	3.604

**Gaus mean : 36.3252**

**Gaus Width: 3.4566**

Entry



# B1L101S, U16-ch6, adc2

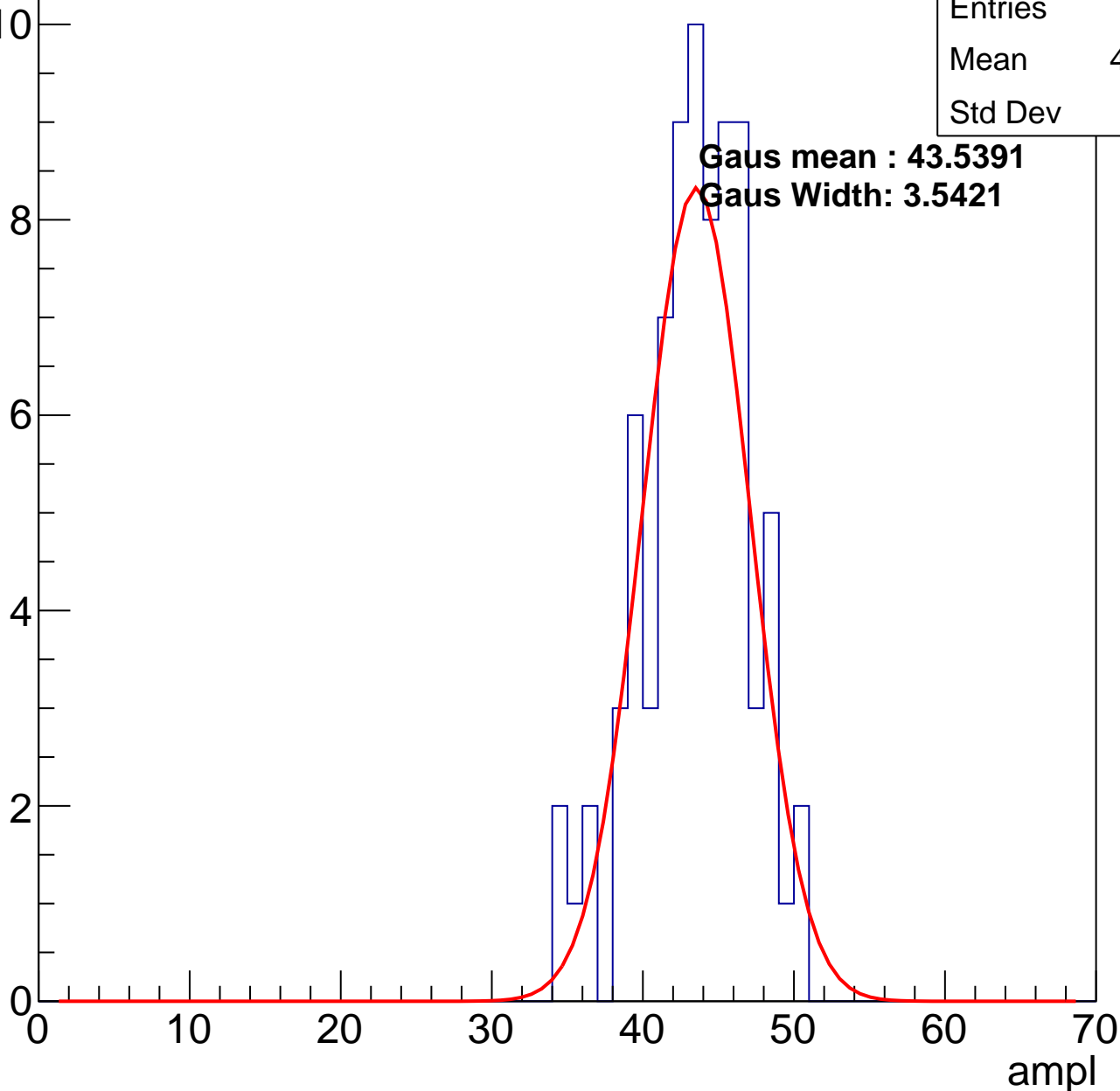
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	42.99
Std Dev	3.52

**Gaus mean : 43.5391**

**Gaus Width: 3.5421**

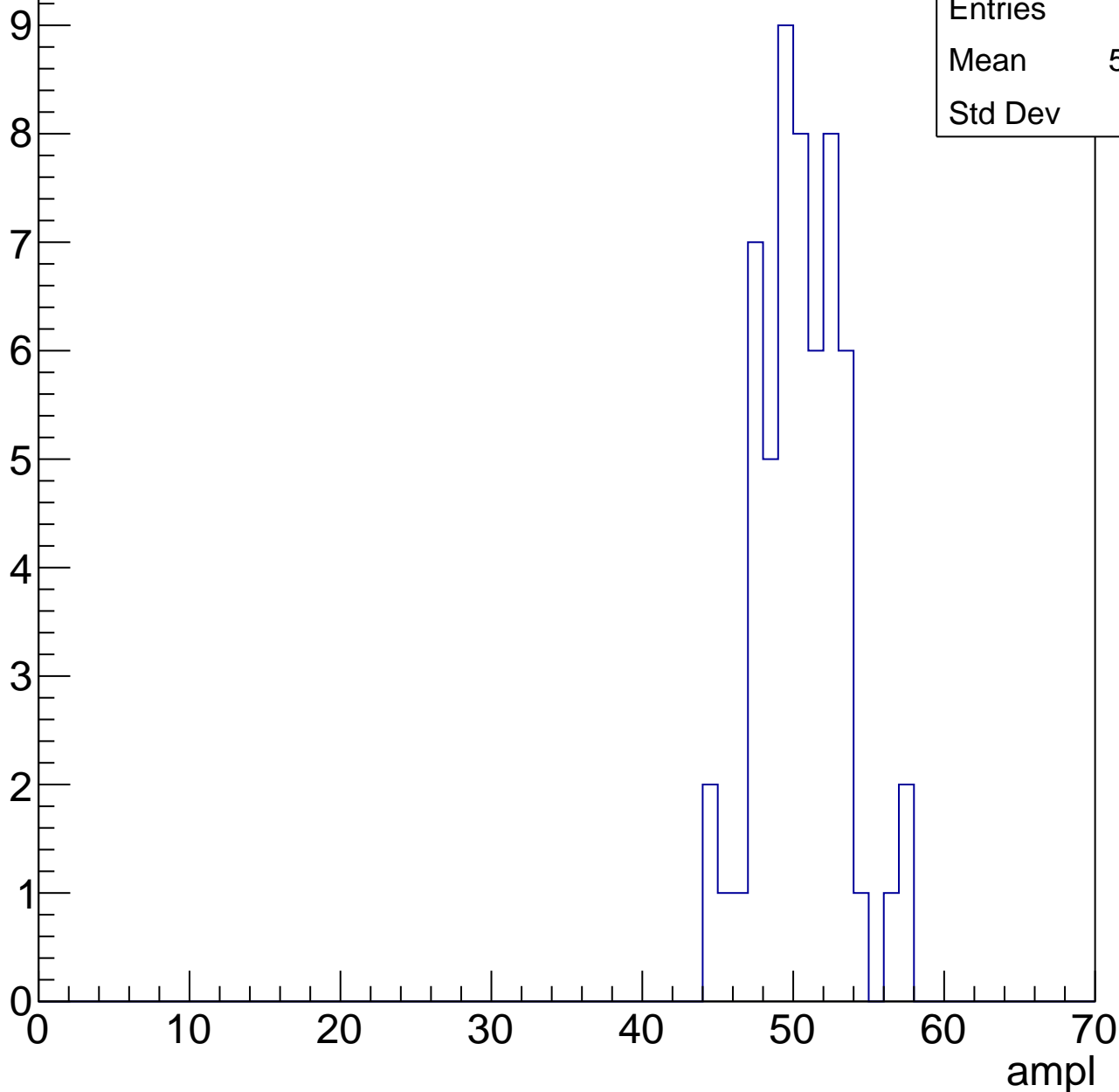


# B1L101S, U16-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

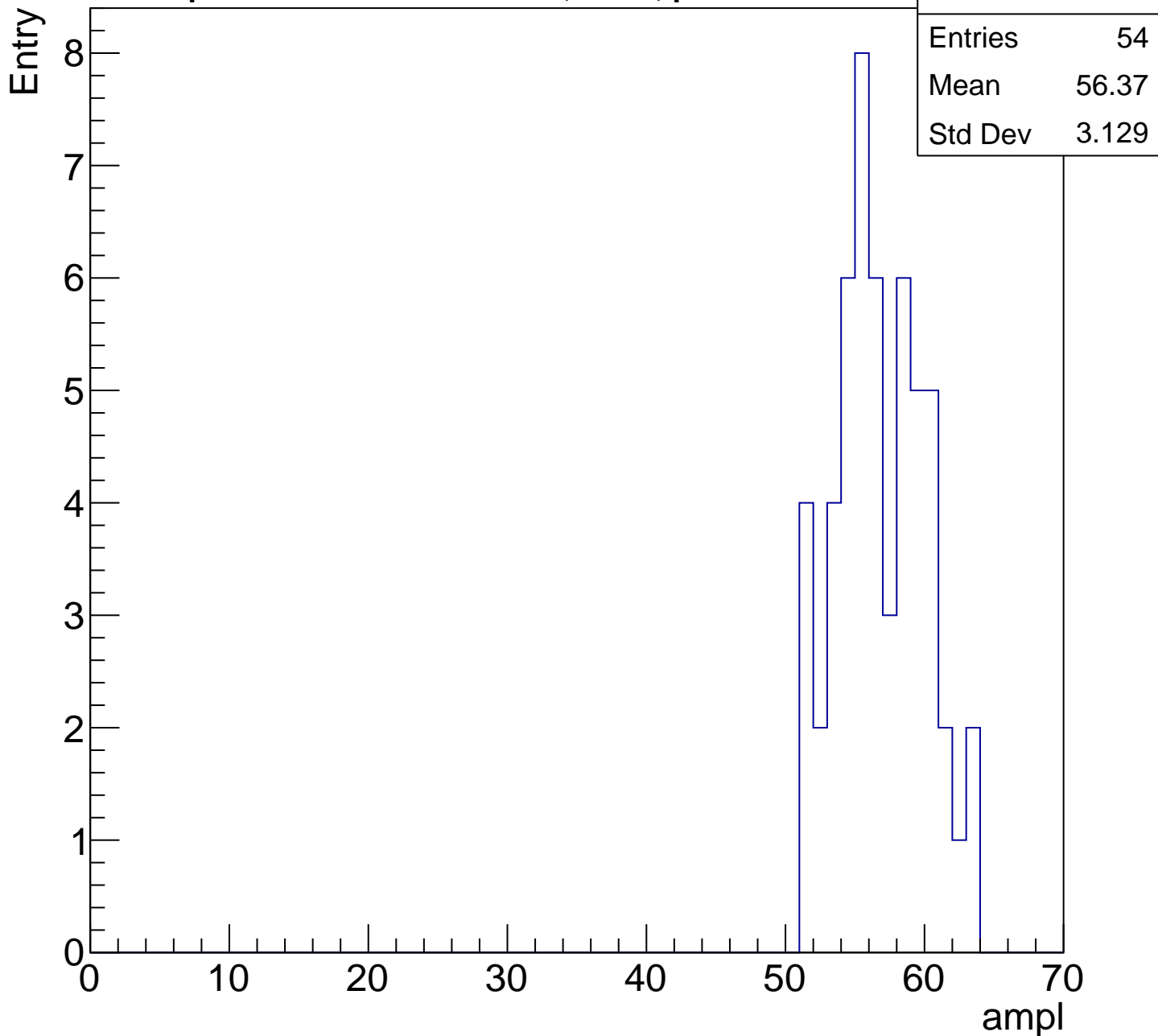
Entry

Entries	57
Mean	50.05
Std Dev	2.8



# B1L101S, U16-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

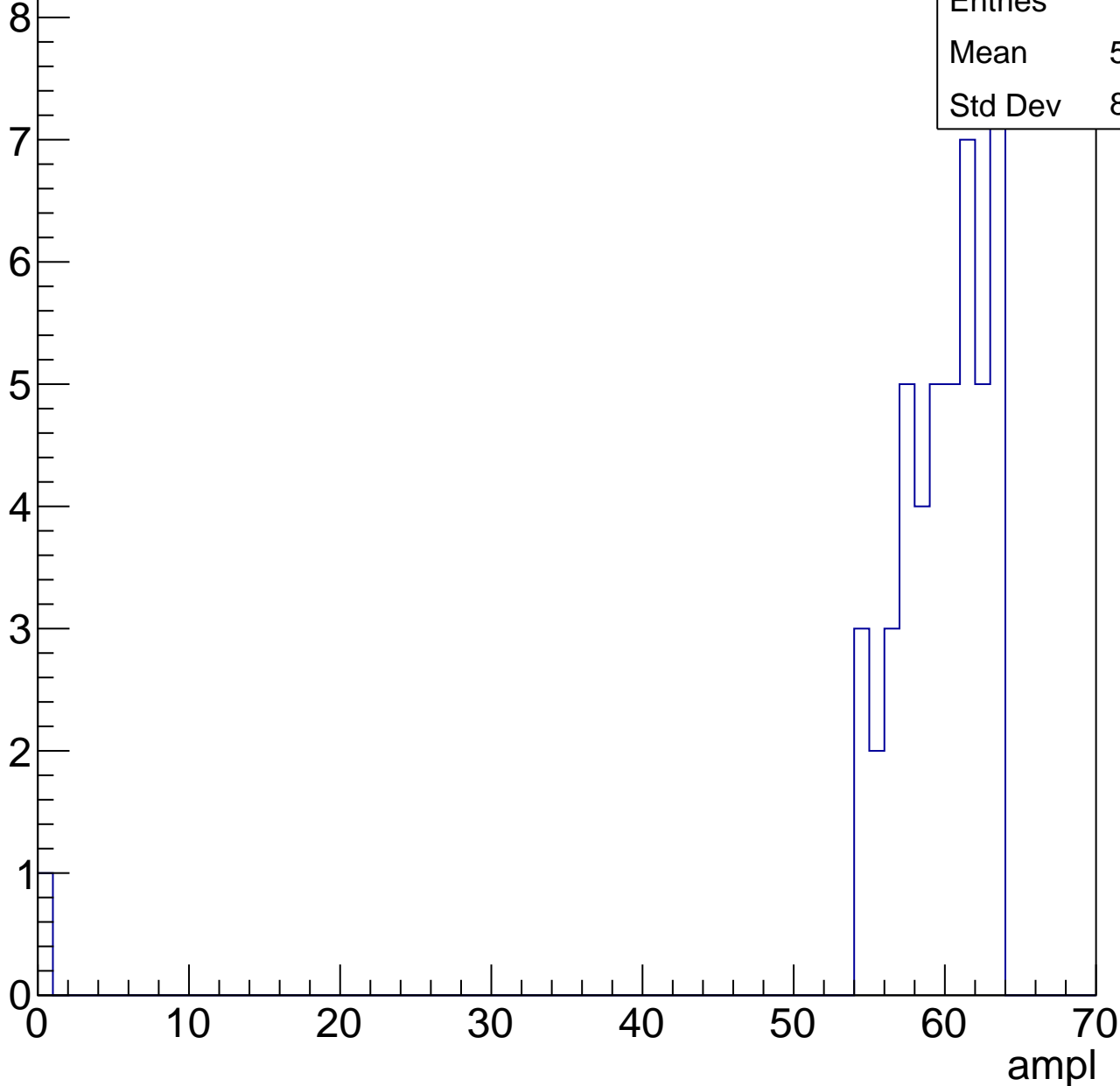


# B1L101S, U16-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	58.19
Std Dev	8.913



# B1L101S, U16-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	62
Std Dev	0

ampl

# B1L101S, U16-ch7, adc0

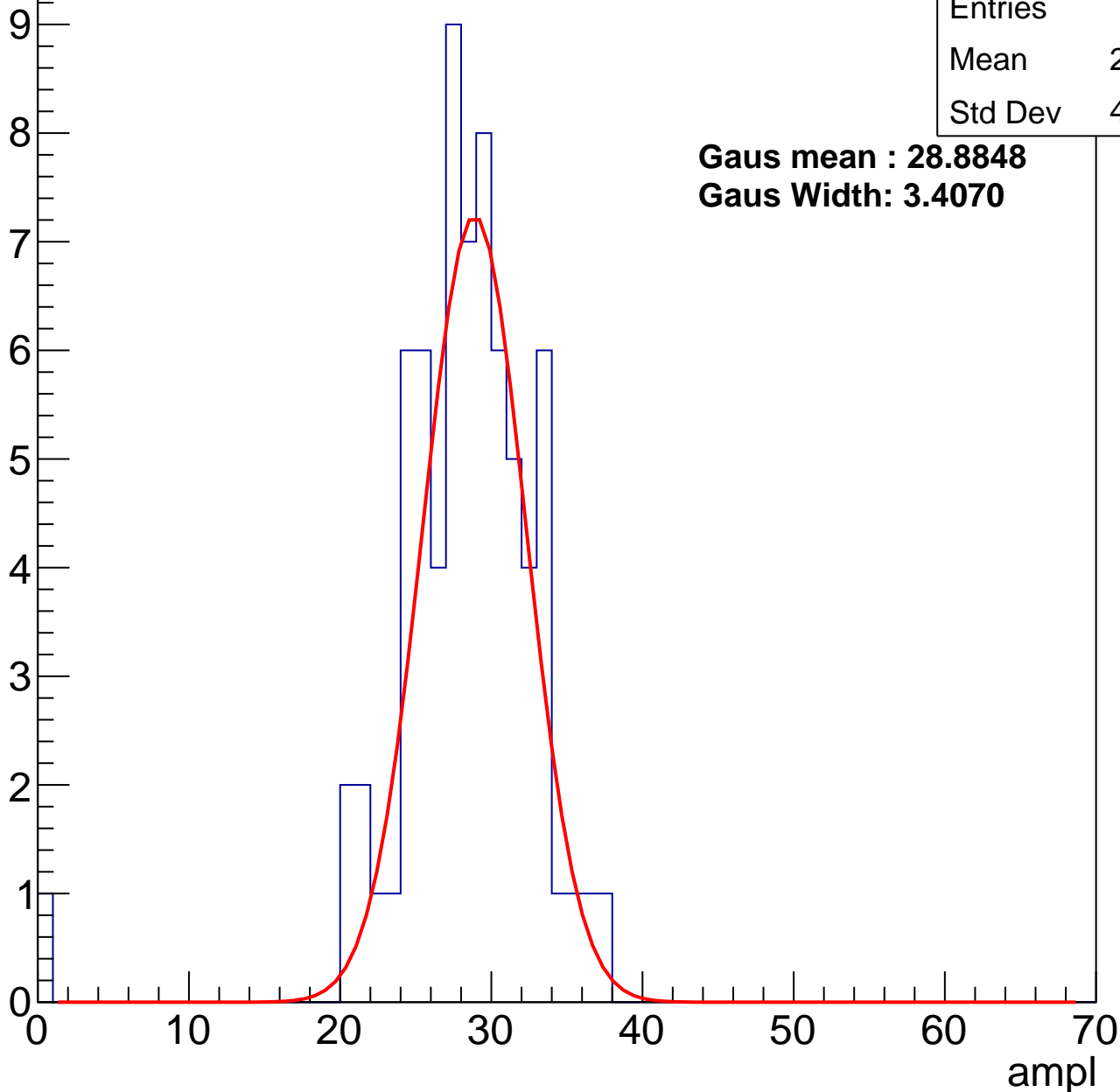
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	27.76
Std Dev	4.948

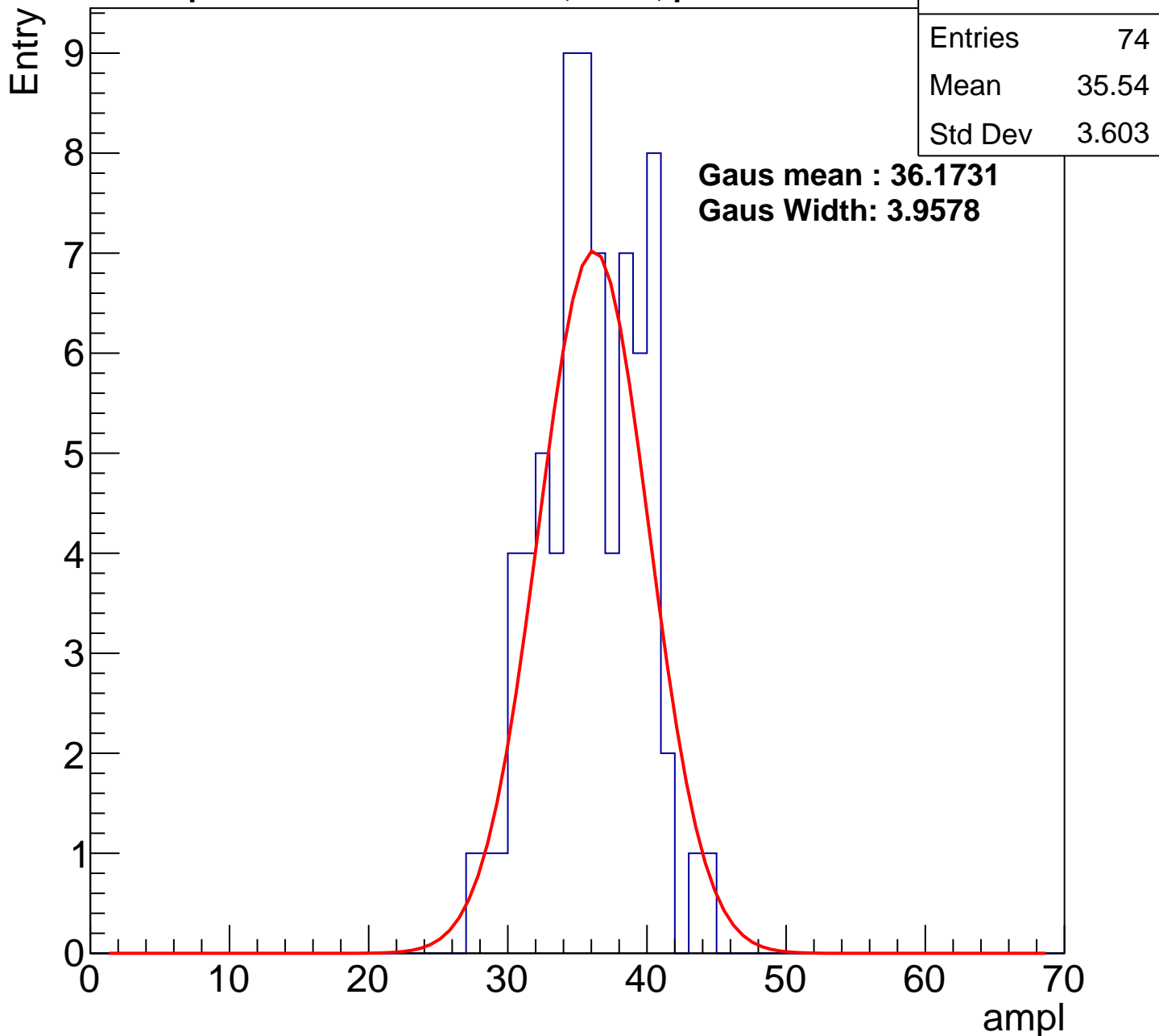
**Gaus mean : 28.8848**

**Gaus Width: 3.4070**



# B1L101S, U16-ch7, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U16-ch7, adc2

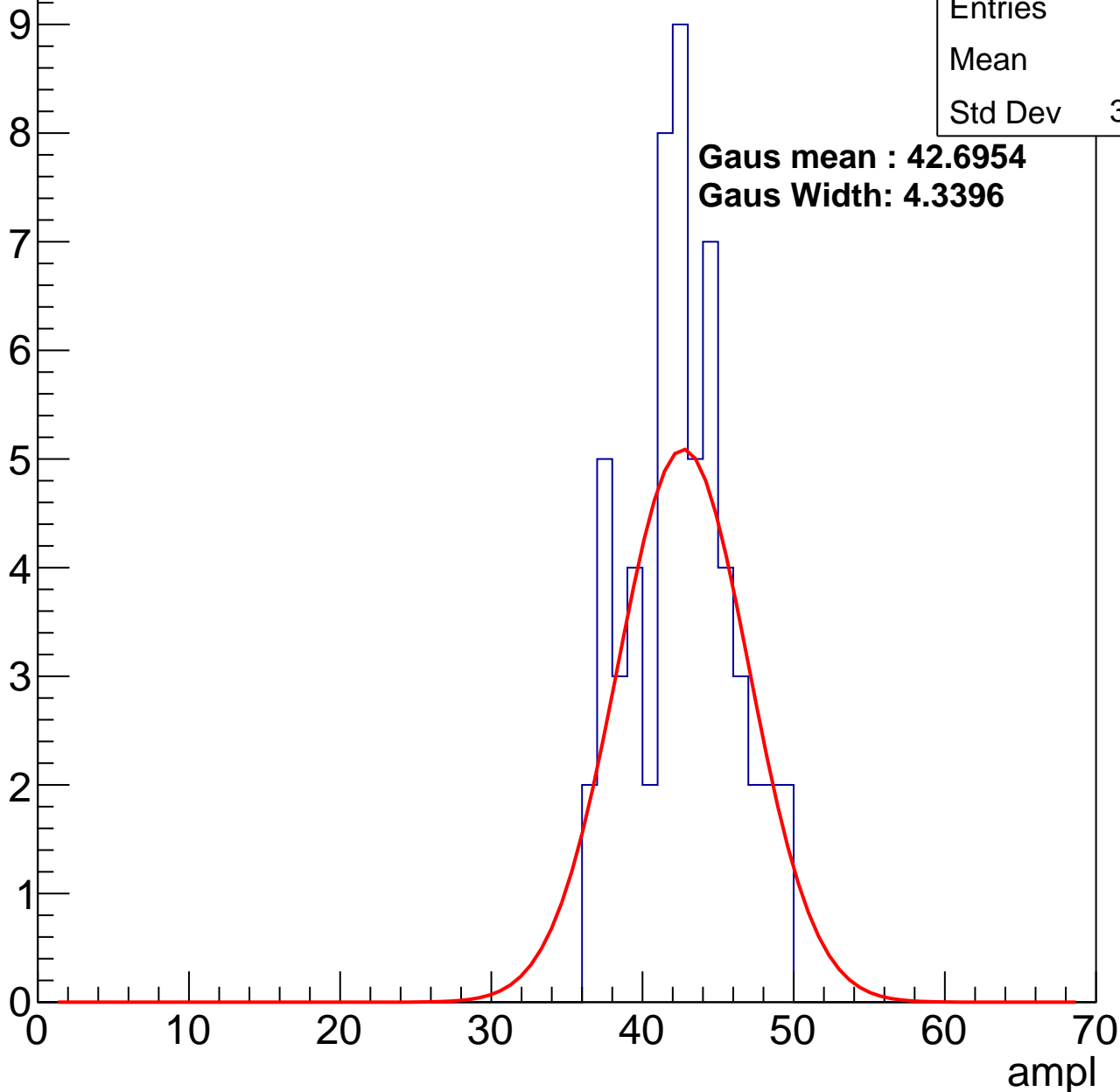
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	42.1
Std Dev	3.305

**Gaus mean : 42.6954**

**Gaus Width: 4.3396**

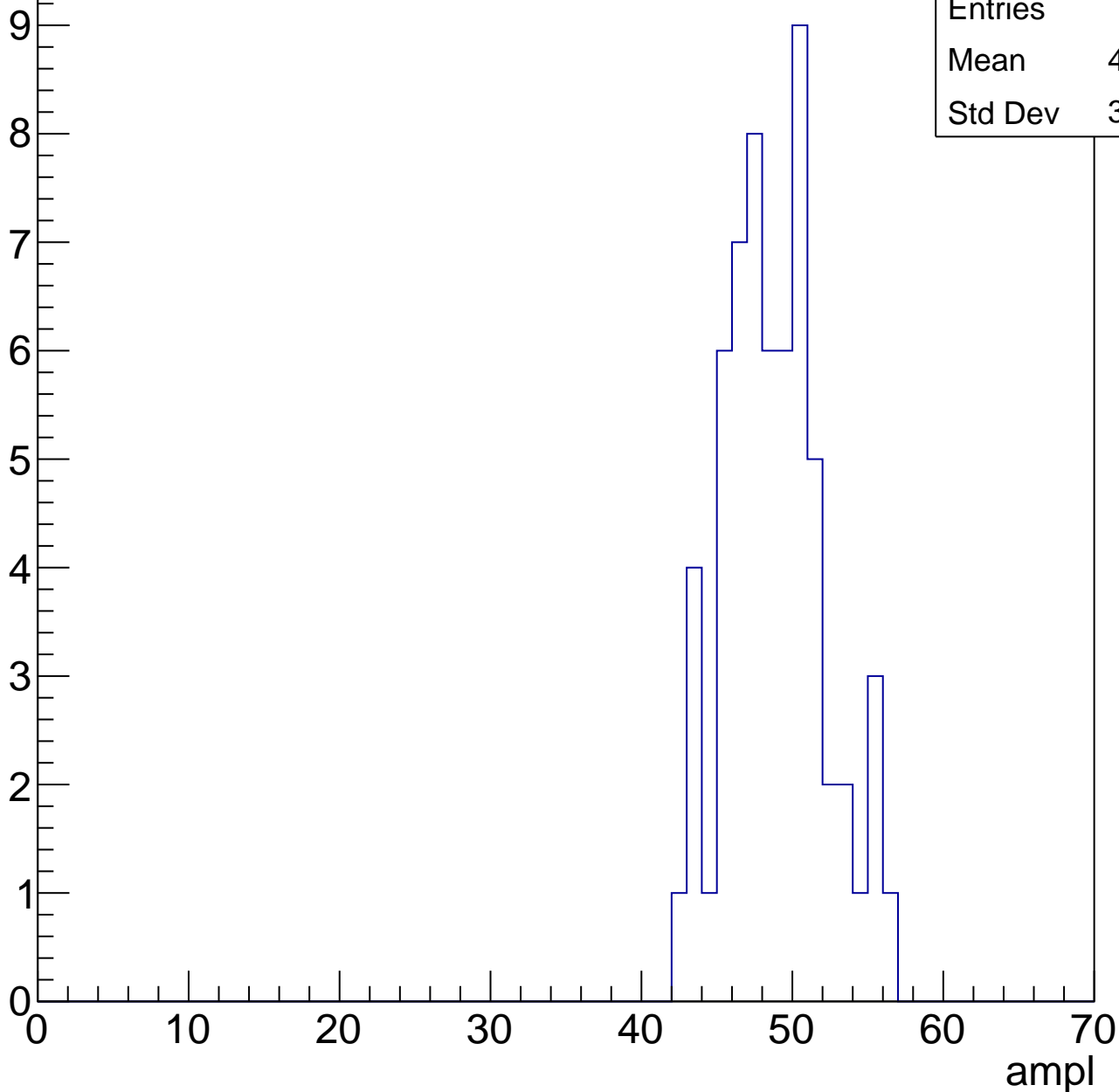


# B1L101S, U16-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

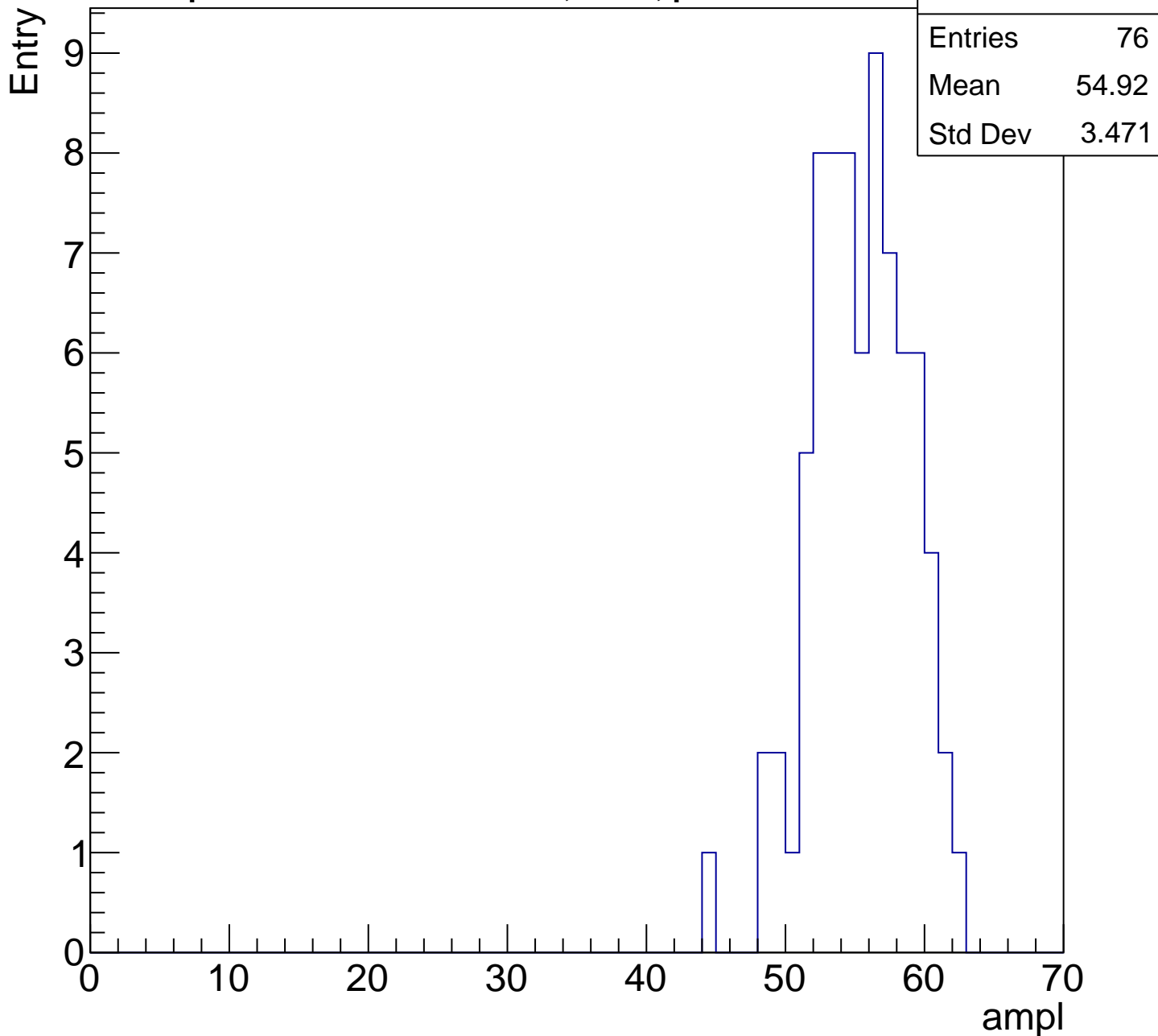
Entry

Entries	62
Mean	48.35
Std Dev	3.238



# B1L101S, U16-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

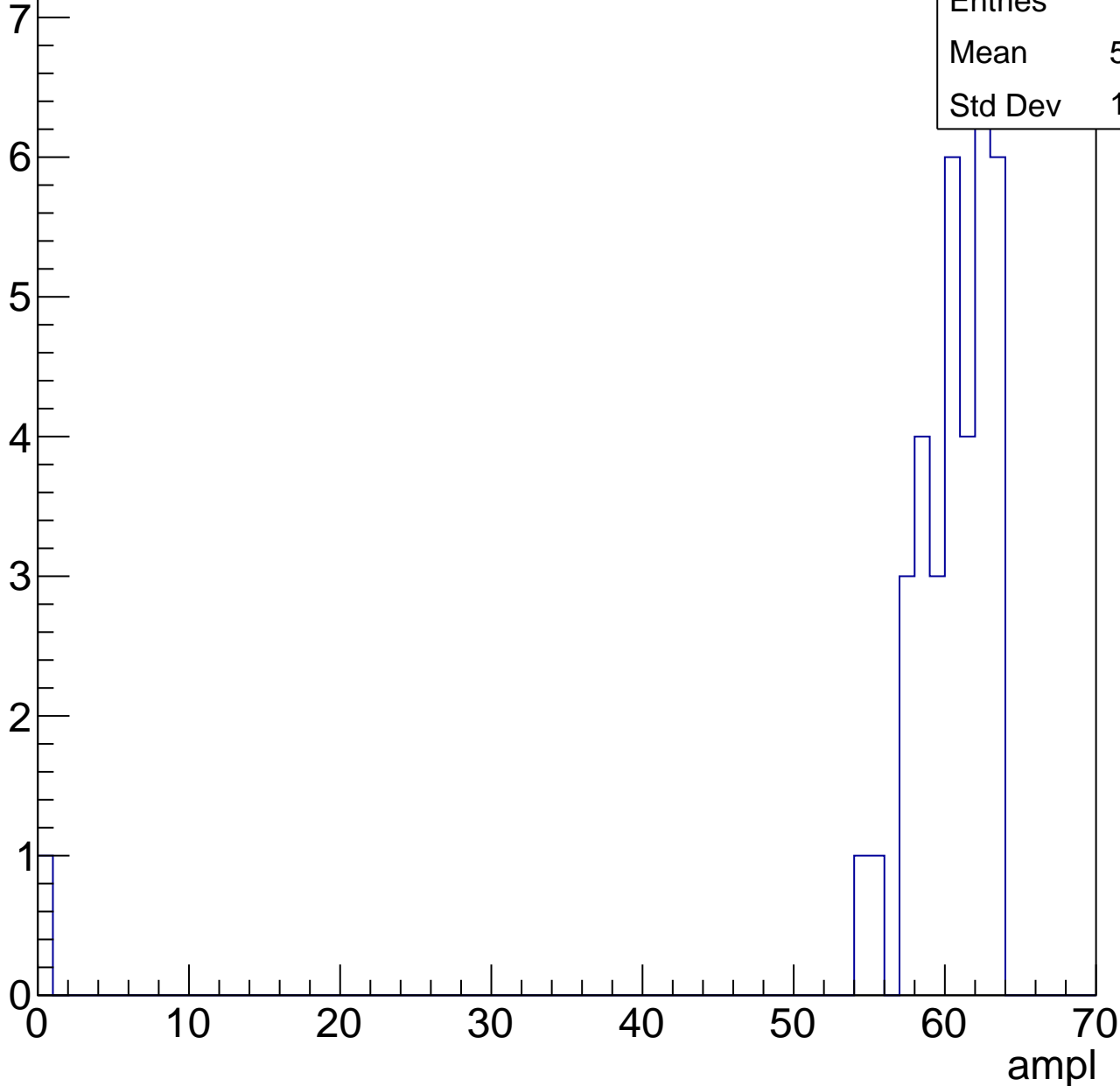


# B1L101S, U16-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

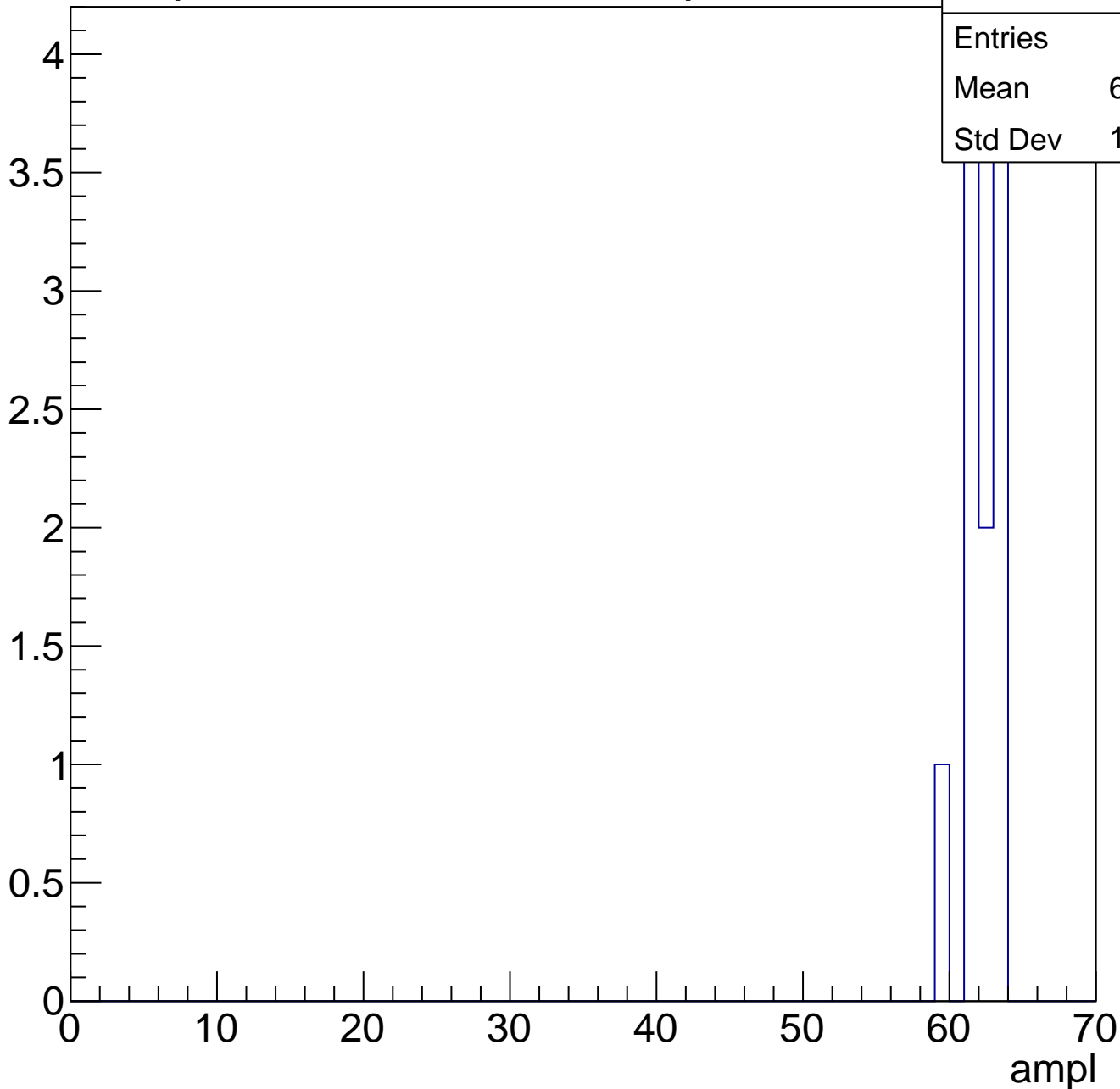
Entries	36
Mean	58.47
Std Dev	10.15



# B1L101S, U16-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U16-ch8, adc0

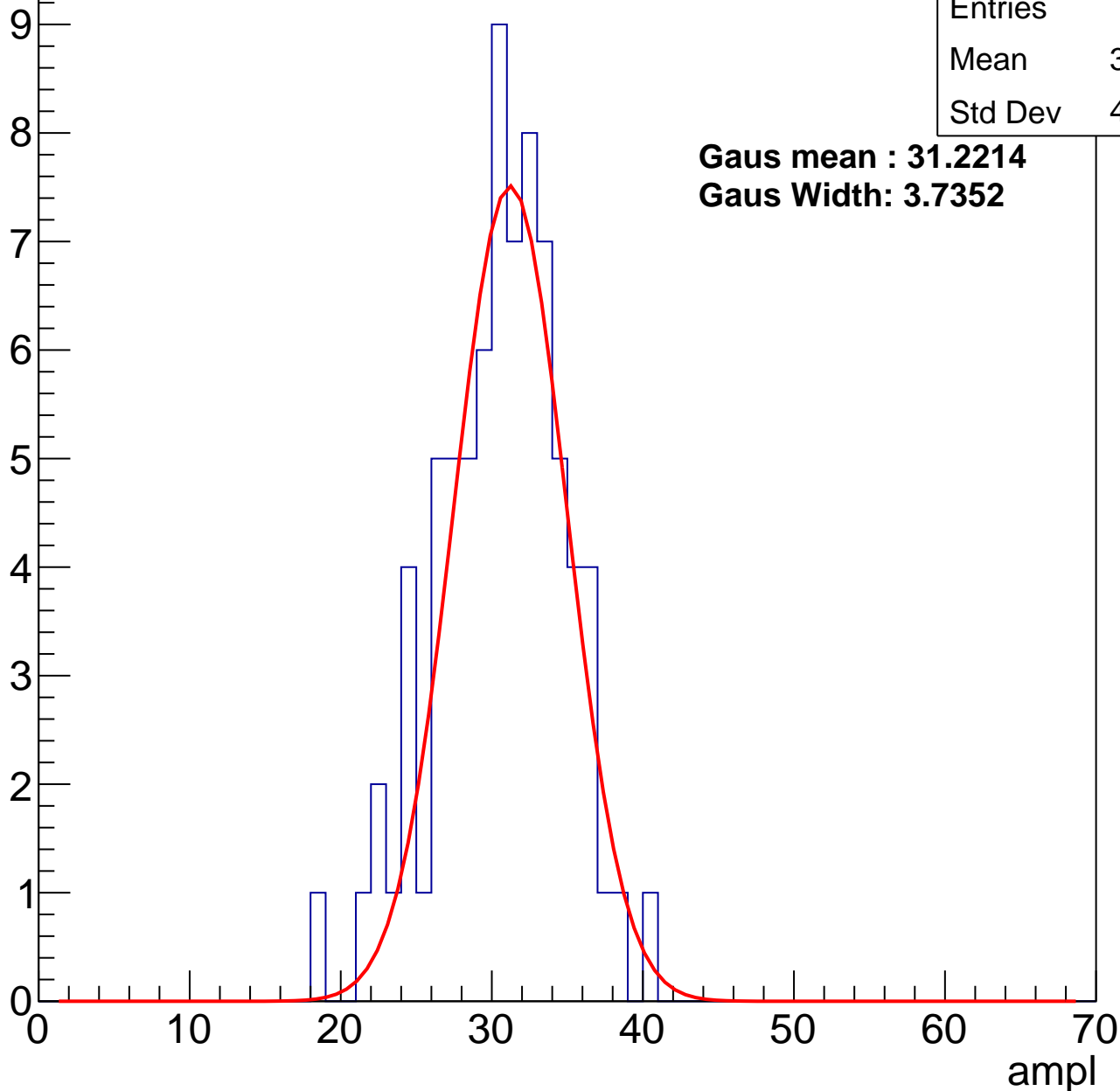
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	30.12
Std Dev	4.176

**Gaus mean : 31.2214**

**Gaus Width: 3.7352**



# B1L101S, U16-ch8, adc1

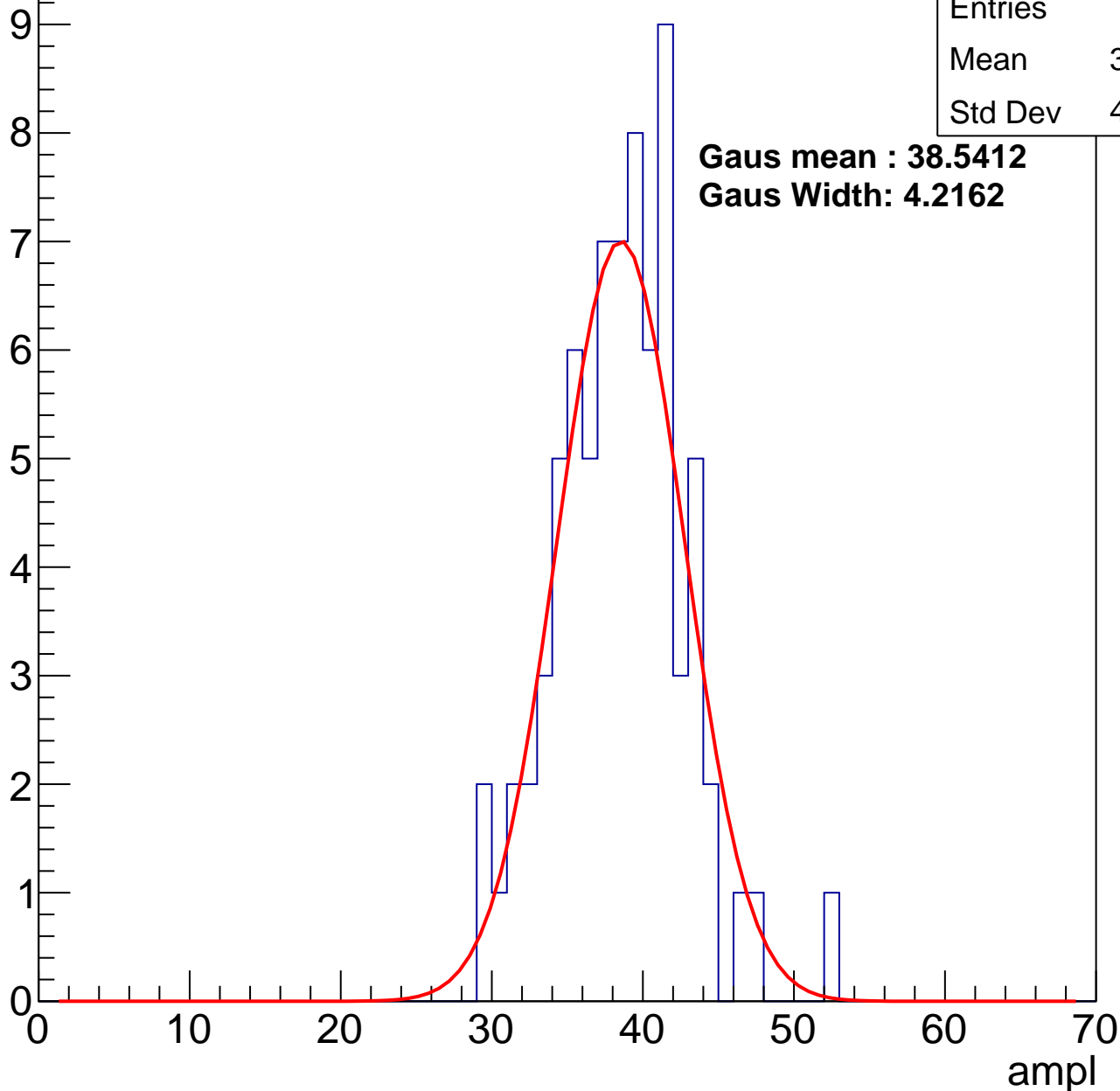
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	38.07
Std Dev	4.184

**Gaus mean : 38.5412**

**Gaus Width: 4.2162**



# B1L101S, U16-ch8, adc2

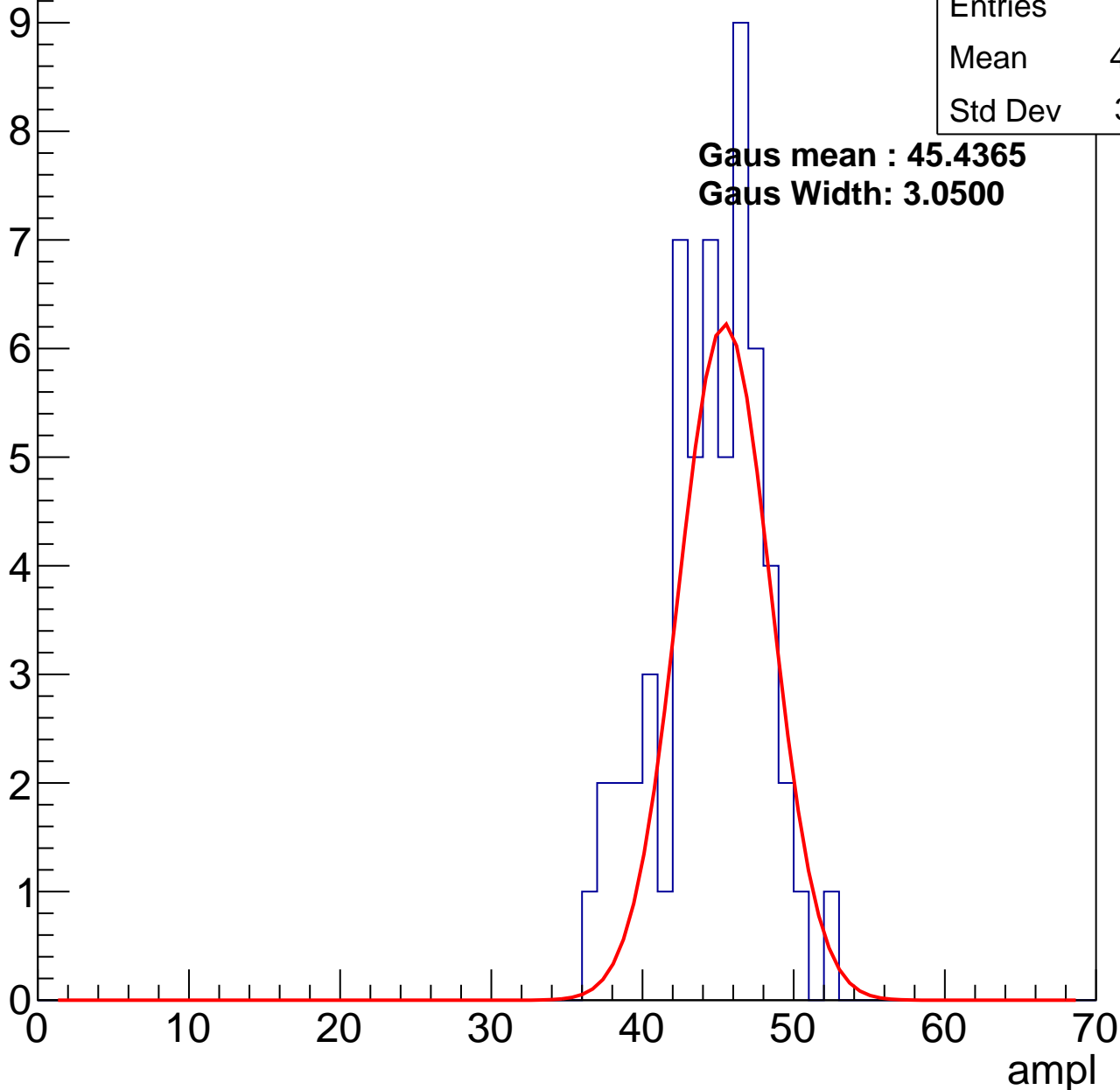
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	44.05
Std Dev	3.431

**Gaus mean : 45.4365**

**Gaus Width: 3.0500**

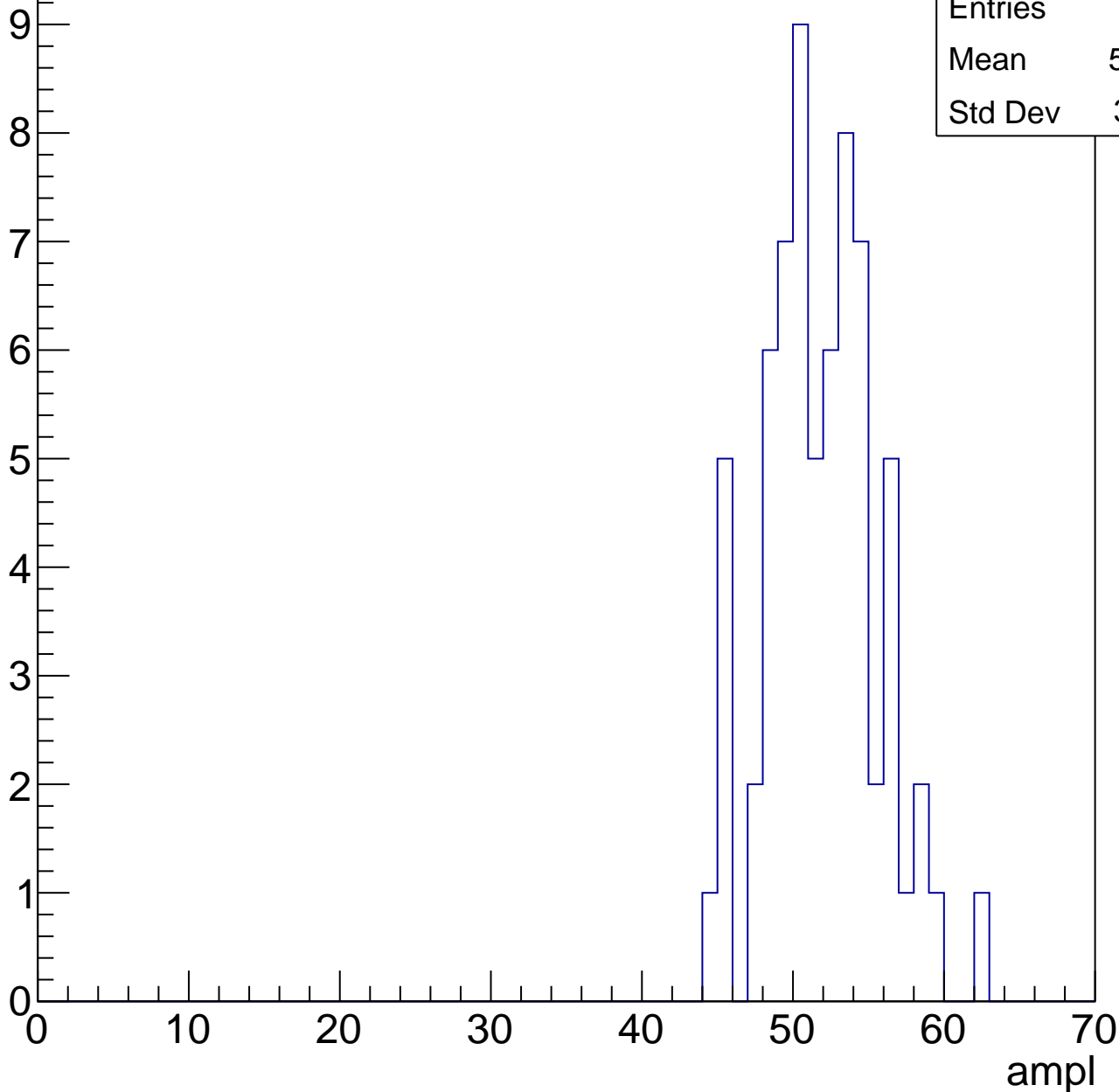


# B1L101S, U16-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

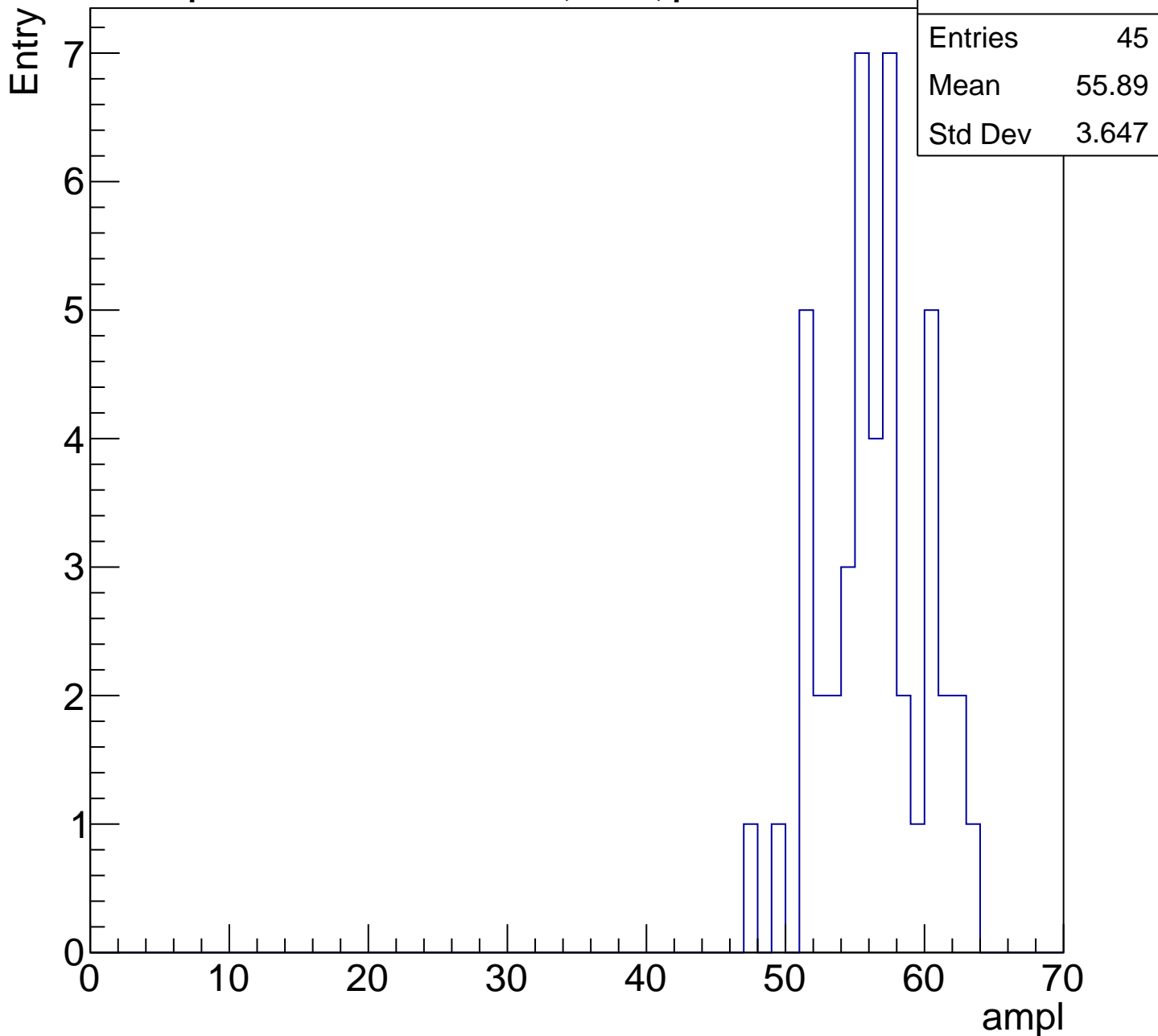
Entry

Entries	68
Mean	51.43
Std Dev	3.671



# B1L101S, U16-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U16-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	45
Mean	58.87
Std Dev	9.118

ampl

0 10 20 30 40 50 60 70

0

1

2

3

4

5

6

7

8

9

# B1L101S, U16-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	61.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U16-ch9, adc0

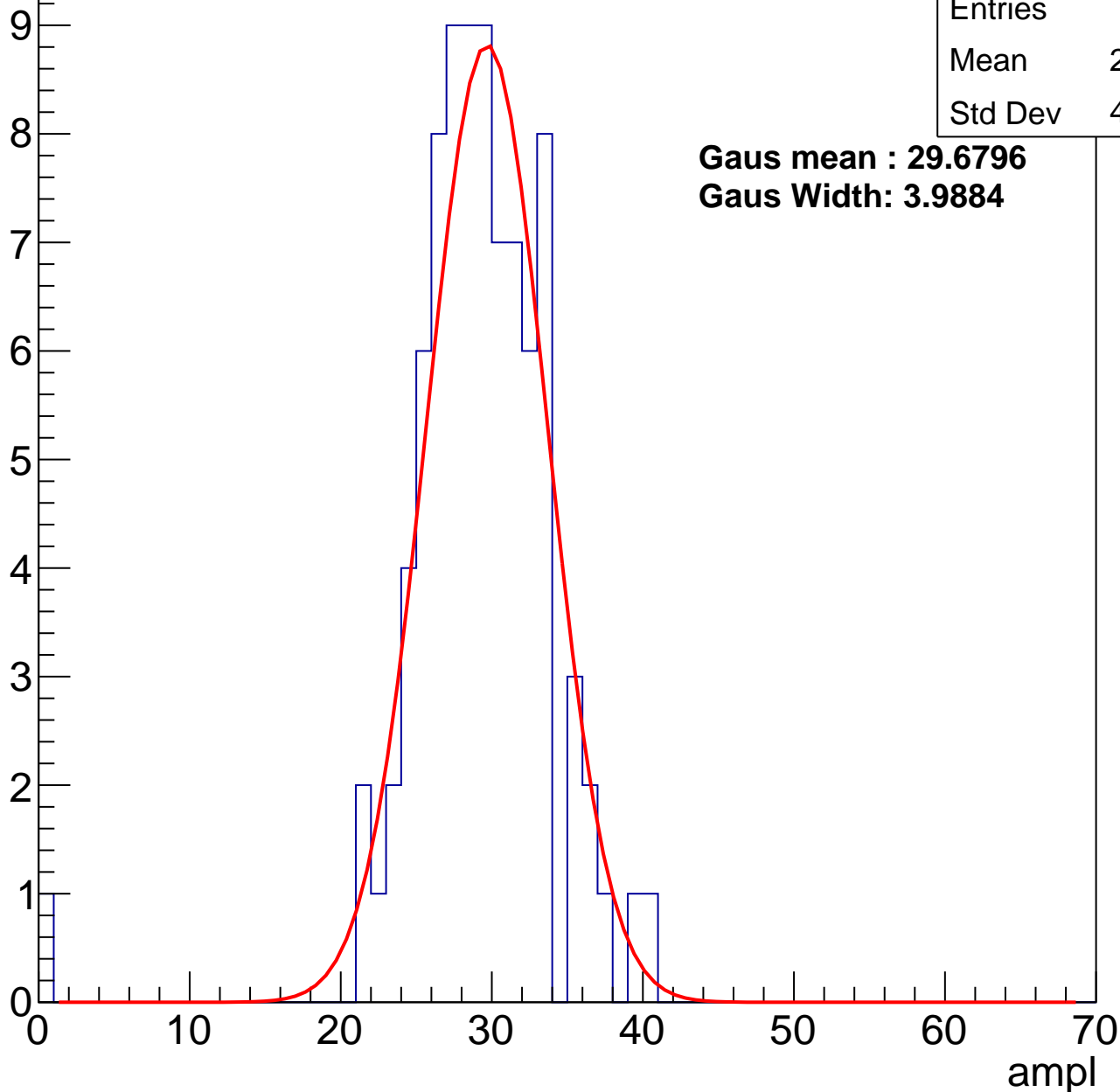
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	87
Mean	28.69
Std Dev	4.916

**Gaus mean : 29.6796**

**Gaus Width: 3.9884**



# B1L101S, U16-ch9, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	73
Mean	36.42
Std Dev	3.483

**Gaus mean : 37.1790**

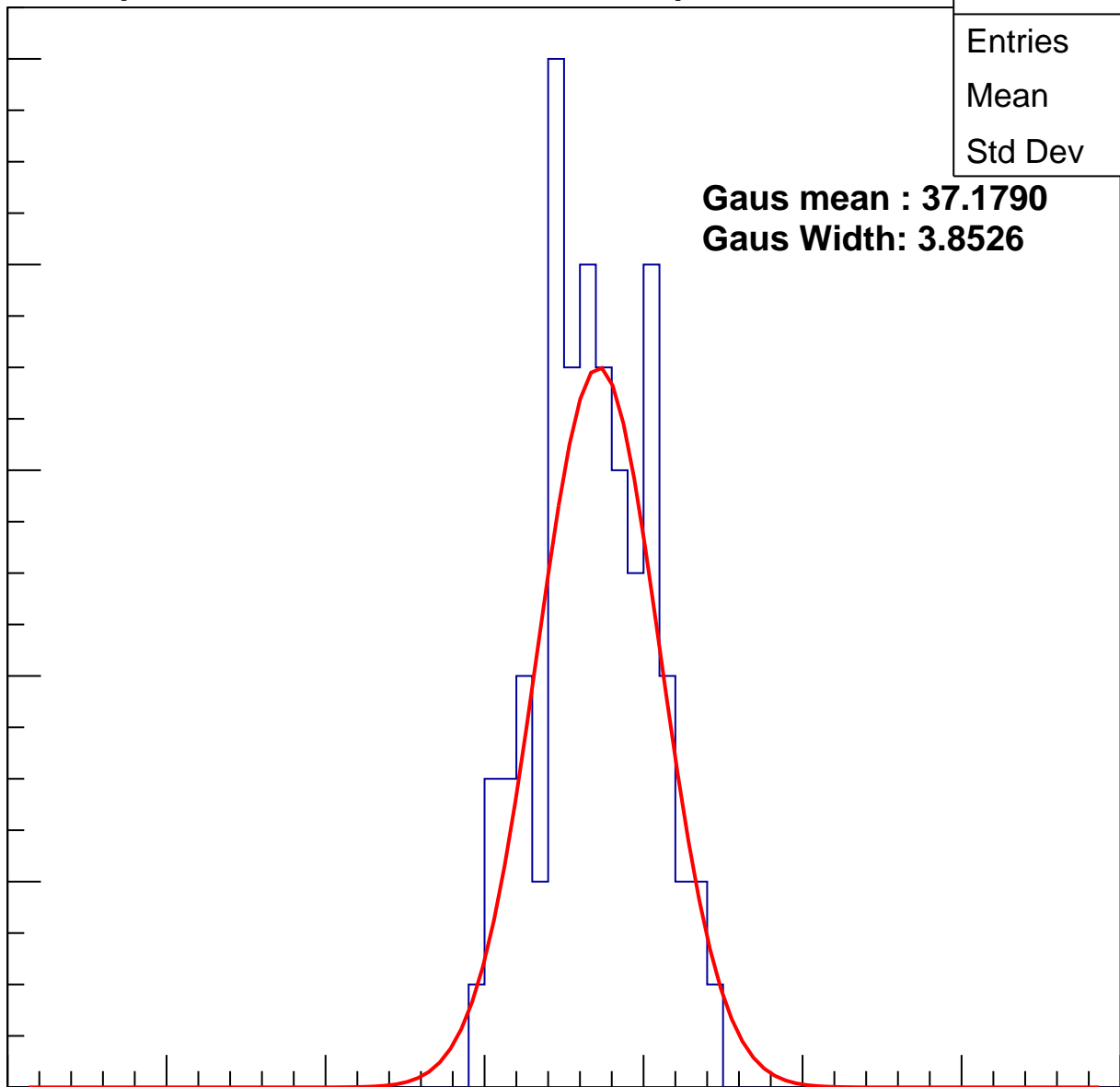
**Gaus Width: 3.8526**

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

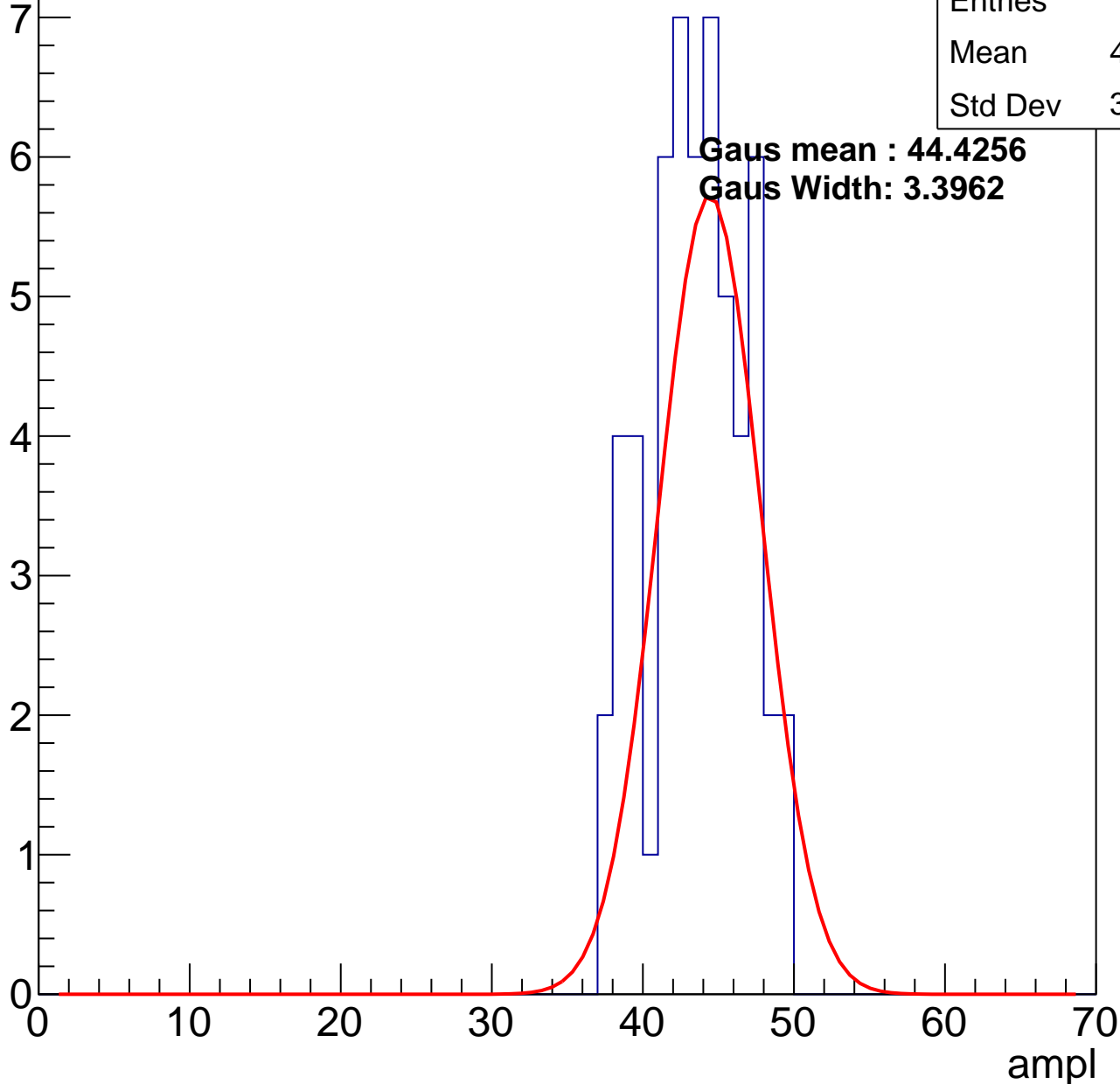


# B1L101S, U16-ch9, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	43.09
Std Dev	3.153

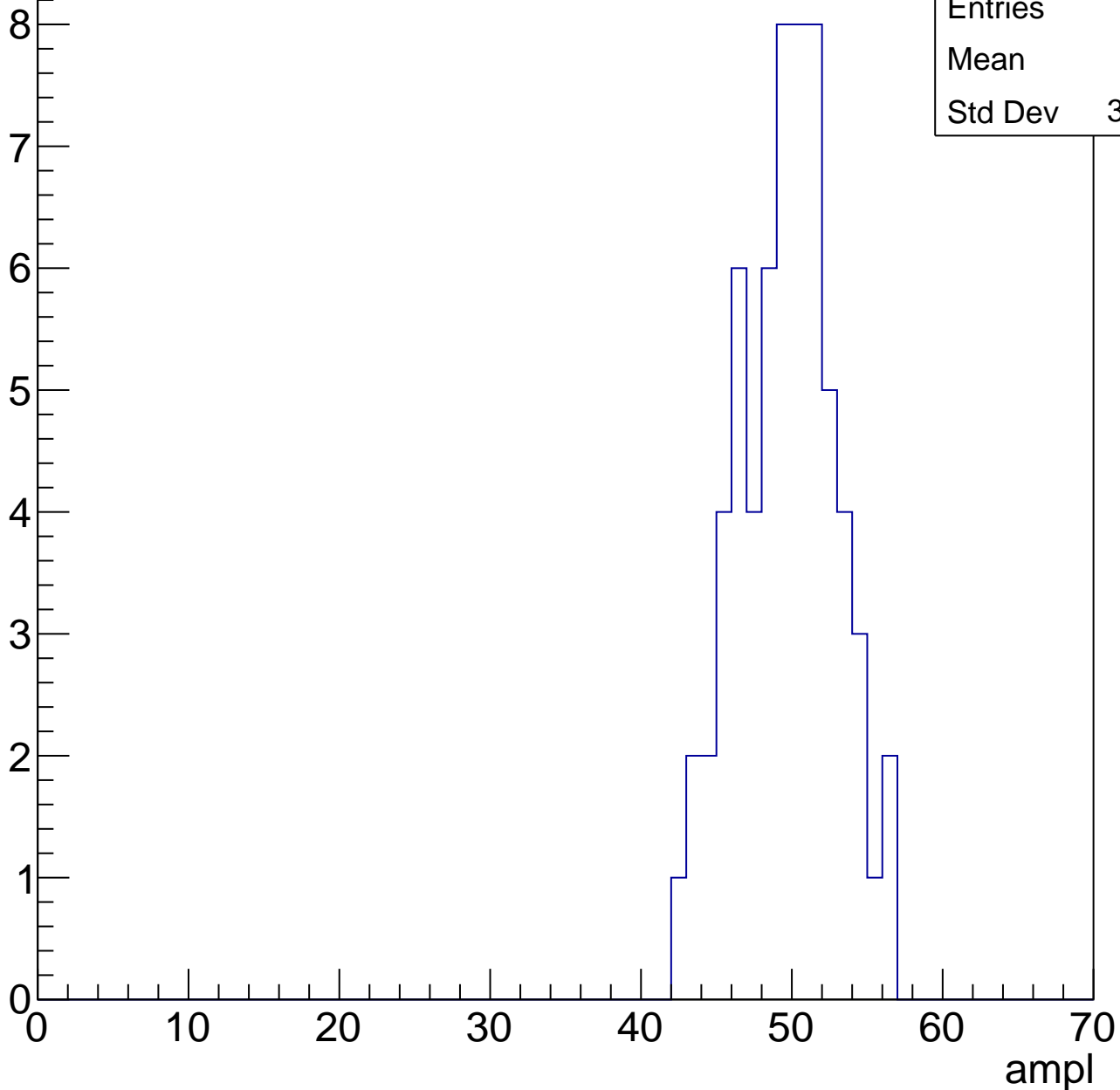


# B1L101S, U16-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

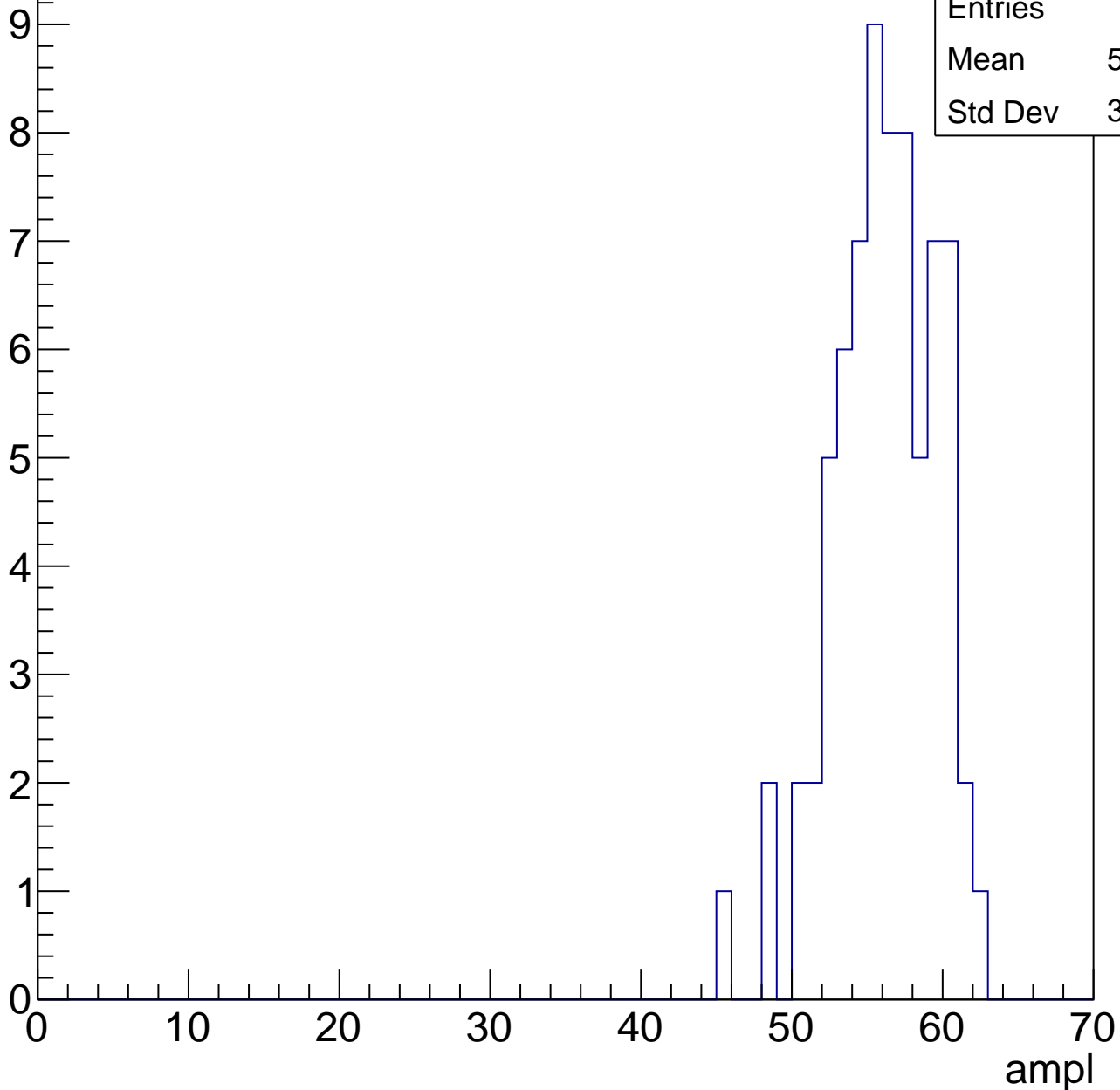
Entries	64
Mean	49.2
Std Dev	3.227



# B1L101S, U16-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

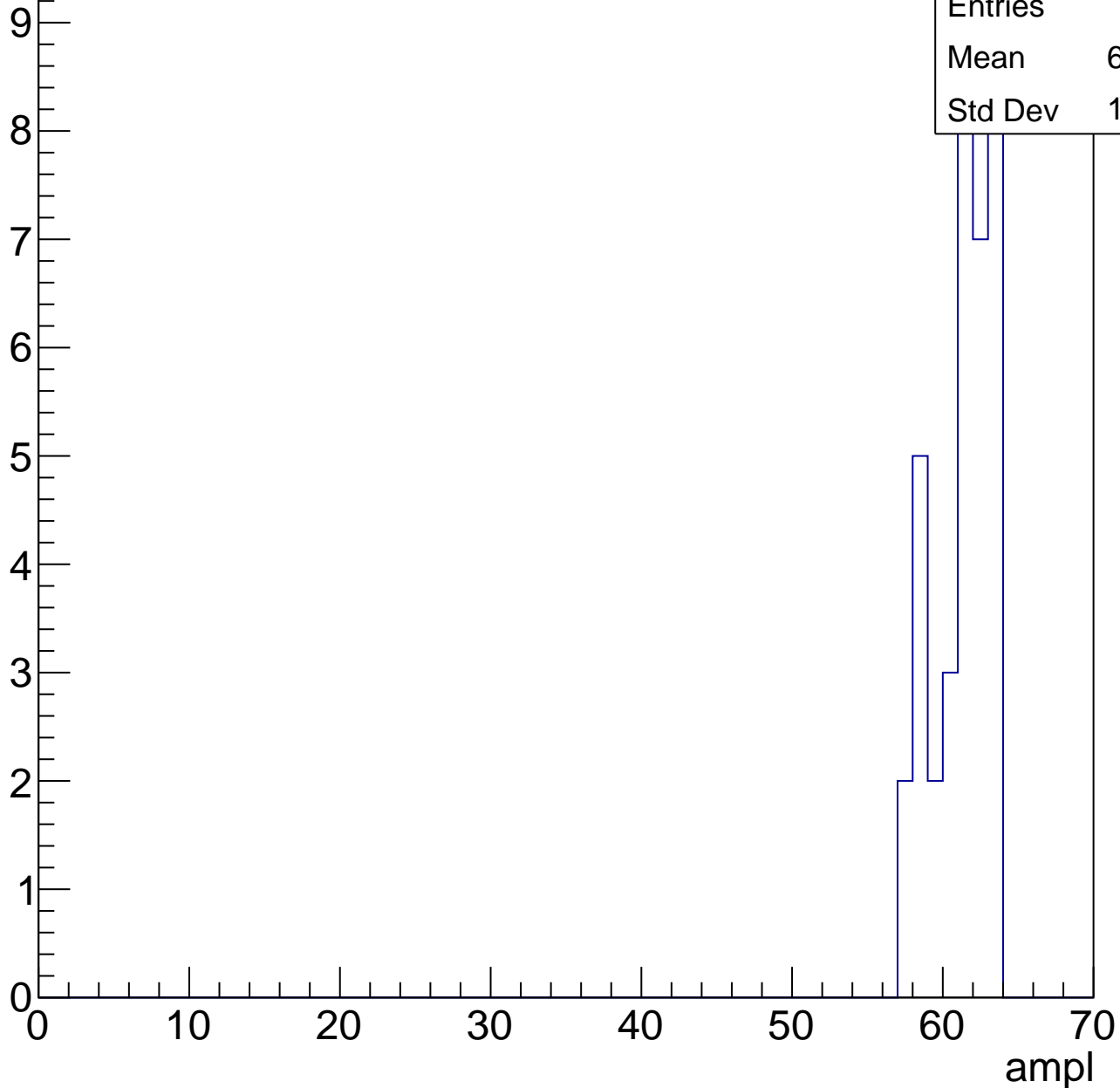


Entries	72
Mean	55.62
Std Dev	3.377

# B1L101S, U16-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

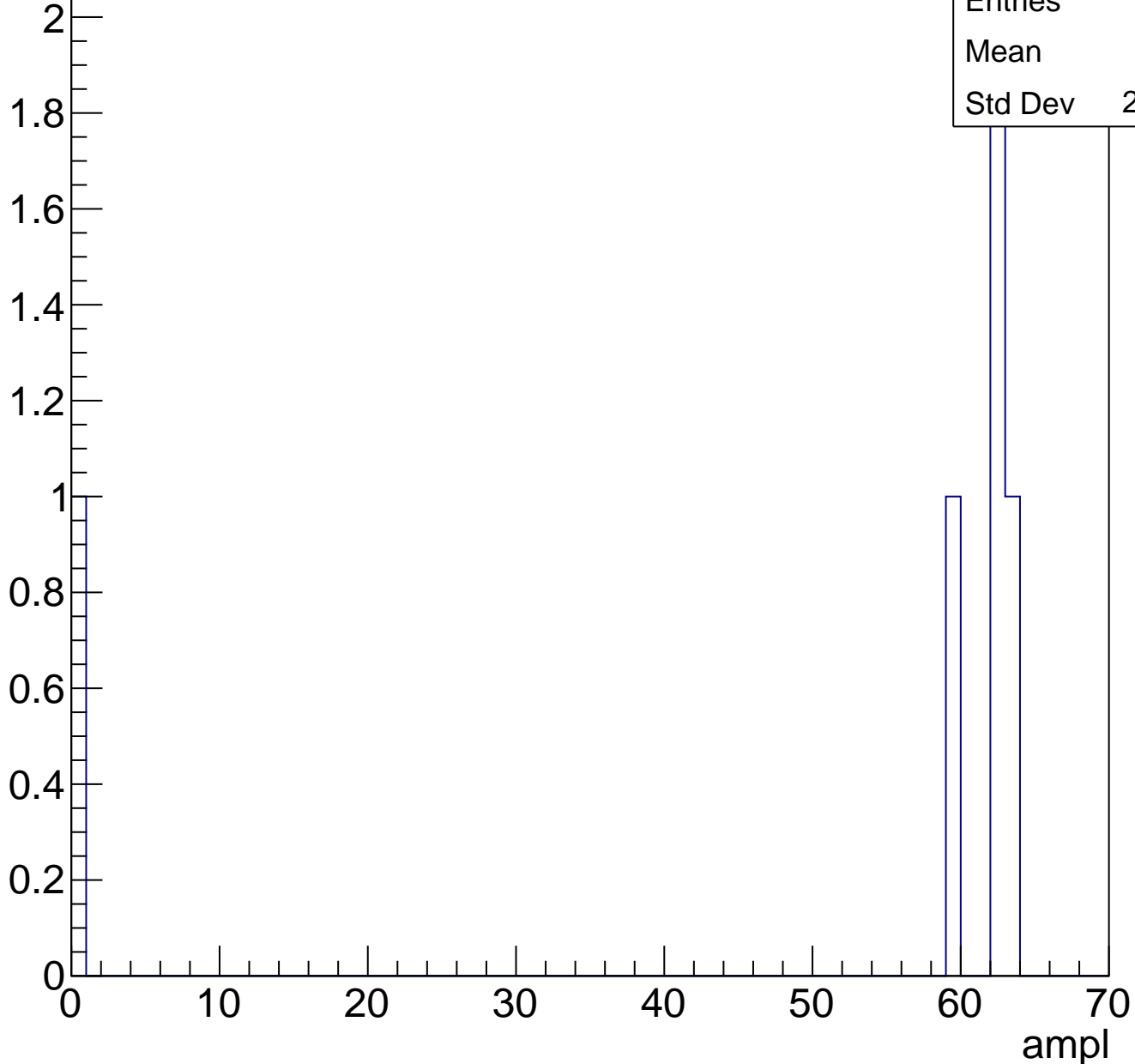
Entry



# B1L101S, U16-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U16-ch10, adc0

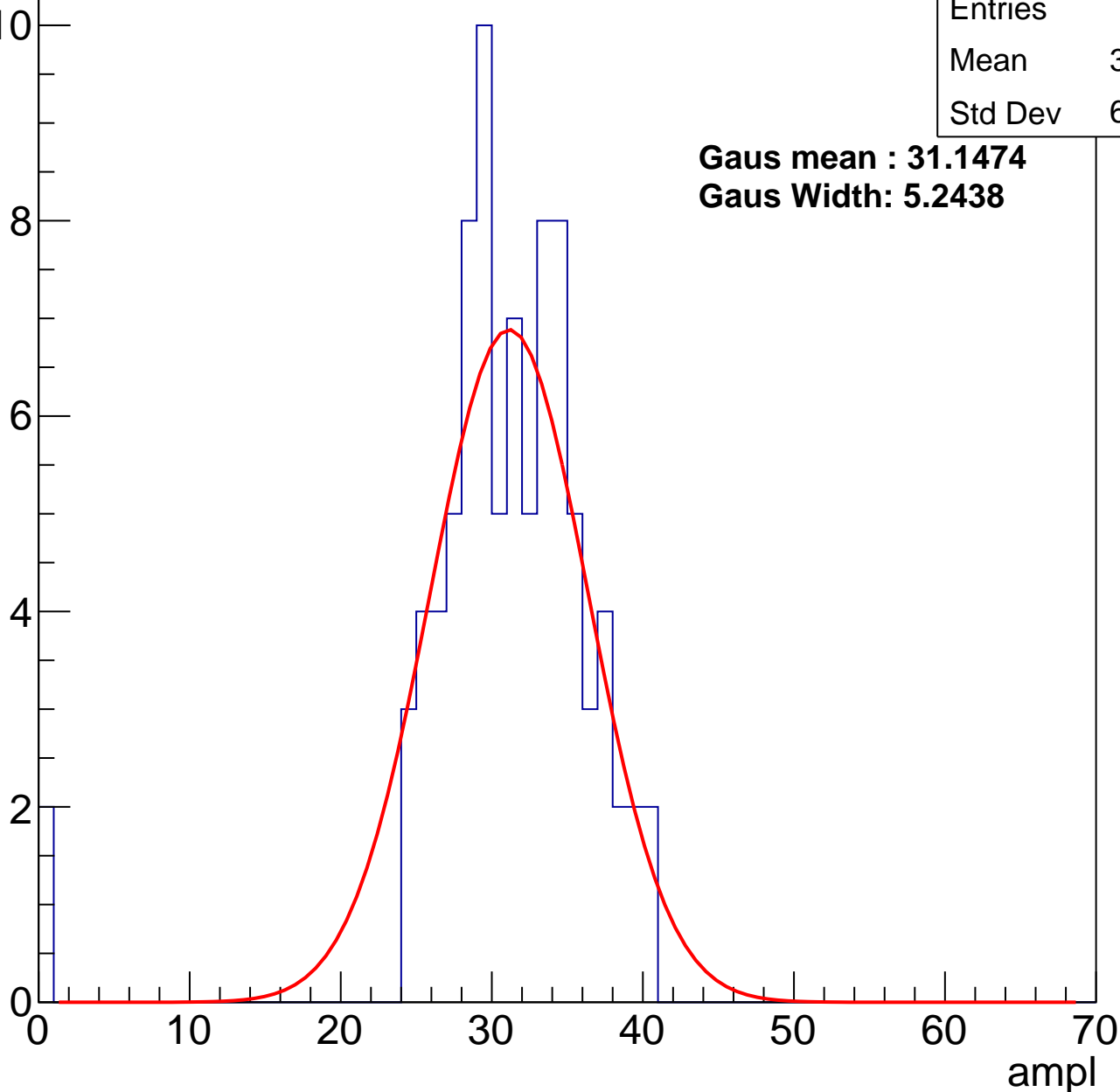
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	87
Mean	30.49
Std Dev	6.144

**Gaus mean : 31.1474**

**Gaus Width: 5.2438**



# B1L101S, U16-ch10, adc1

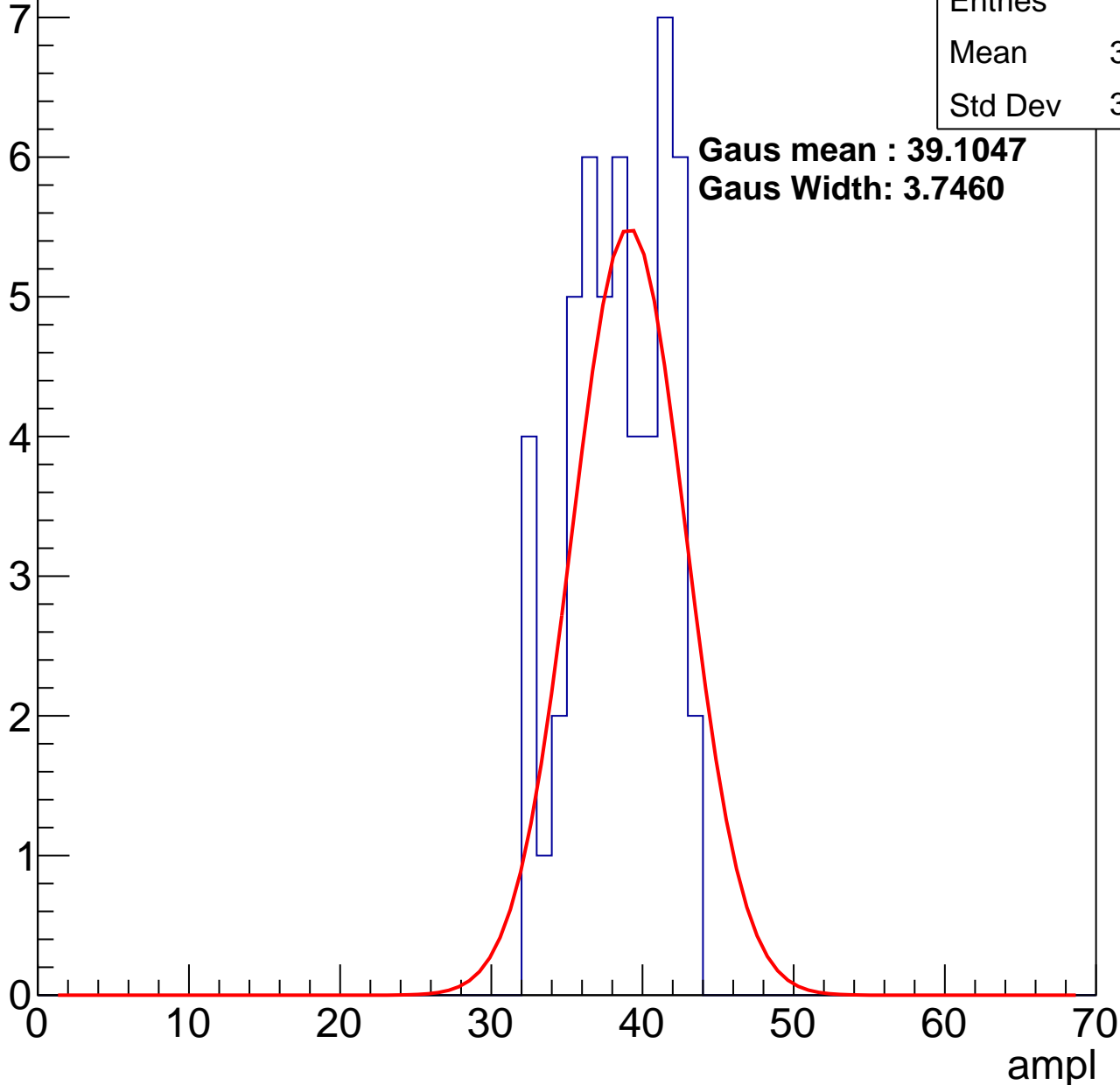
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	37.96
Std Dev	3.113

**Gaus mean : 39.1047**

**Gaus Width: 3.7460**



# B1L101S, U16-ch10, adc2

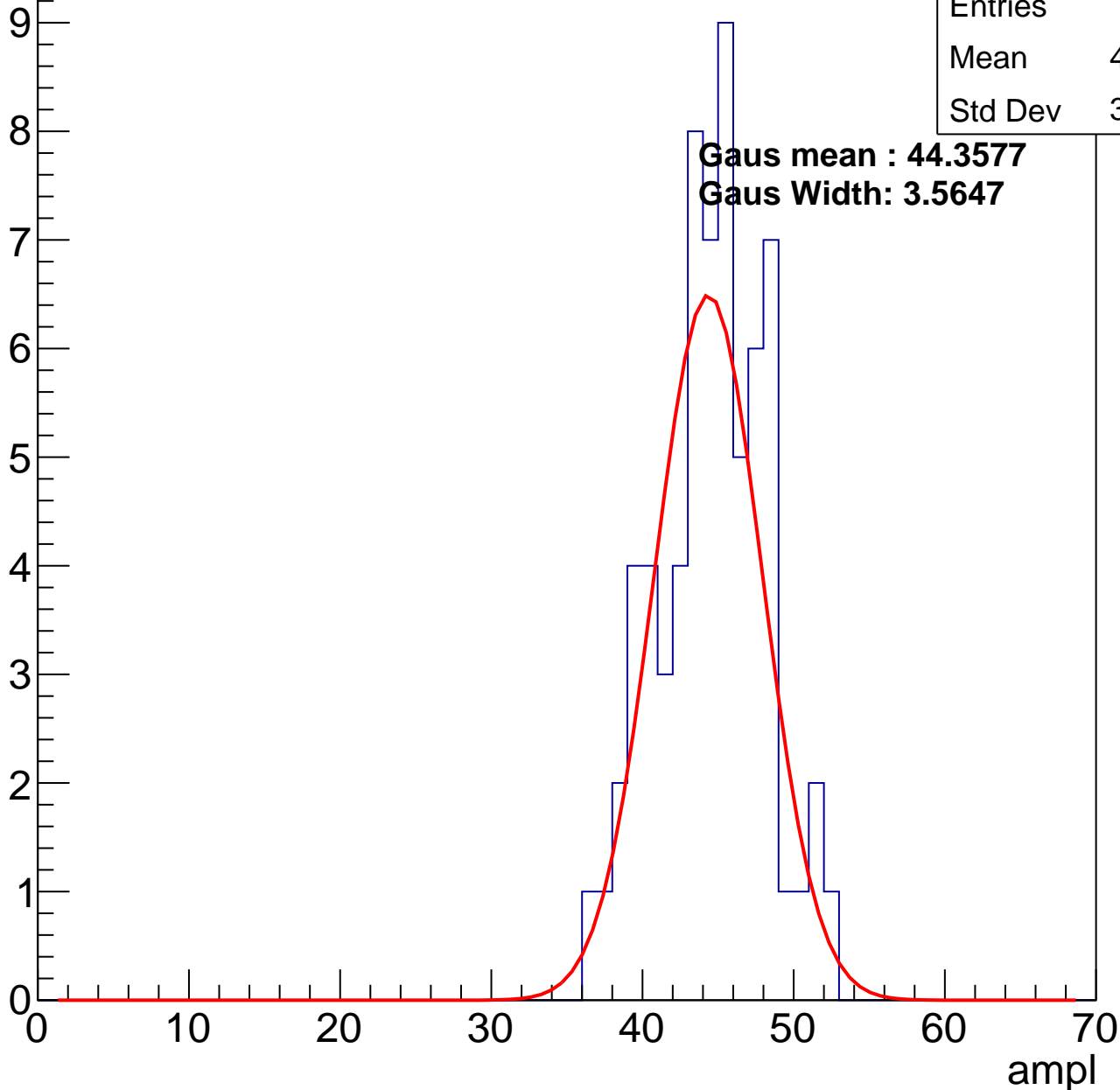
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	44.15
Std Dev	3.517

**Gaus mean : 44.3577**

**Gaus Width: 3.5647**

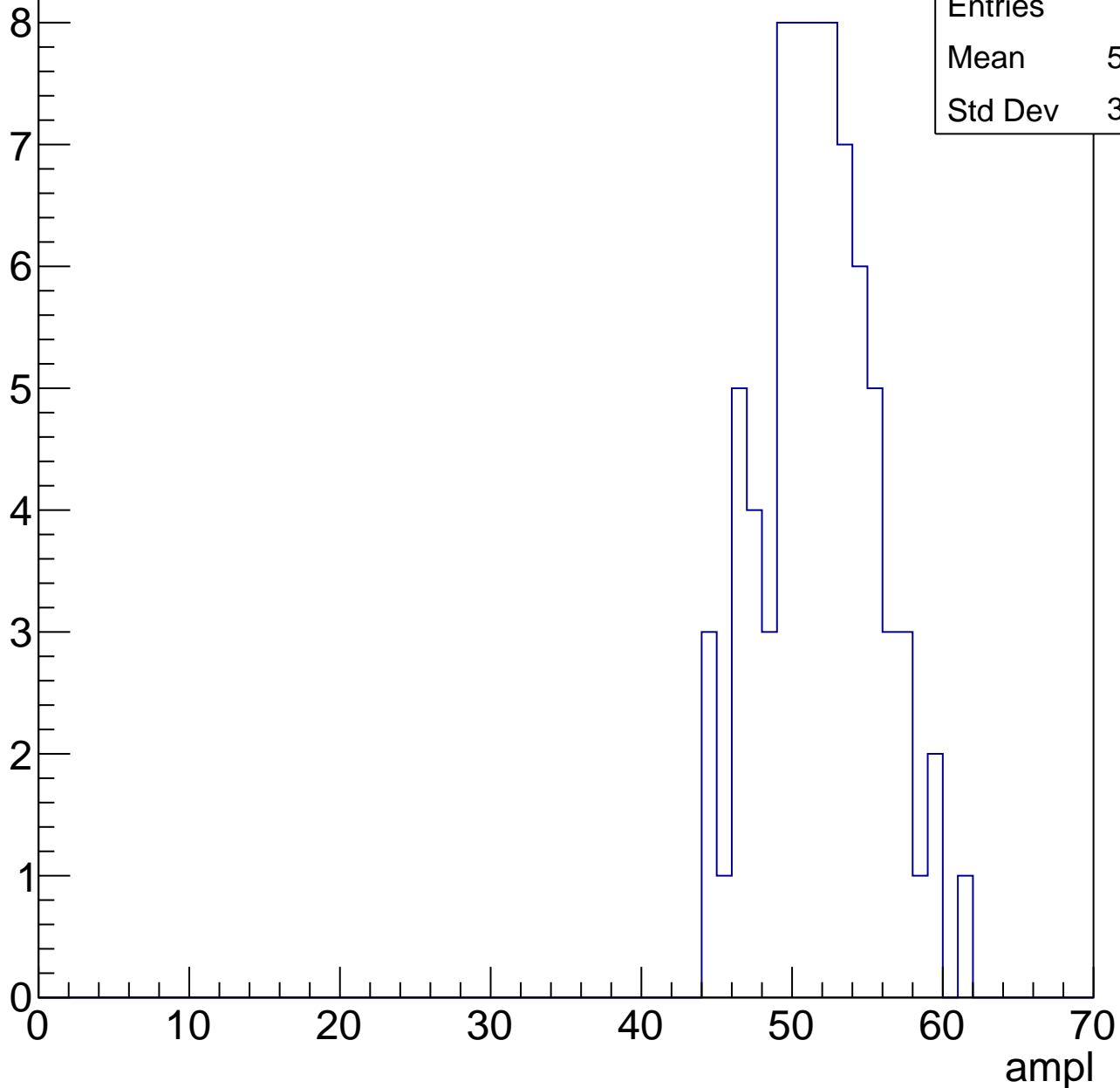


# B1L101S, U16-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	51.33
Std Dev	3.736

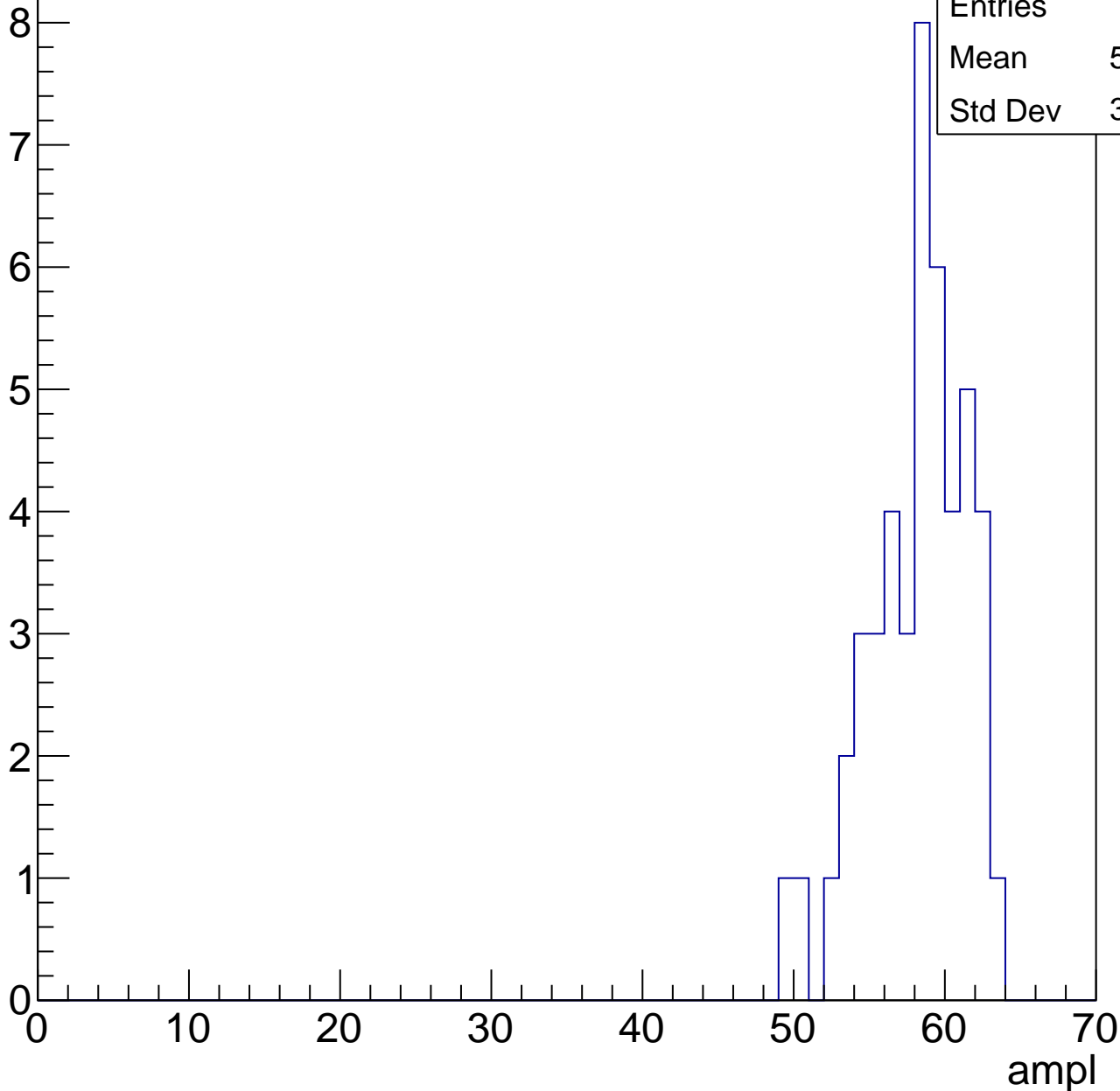


# B1L101S, U16-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	57.67
Std Dev	3.217

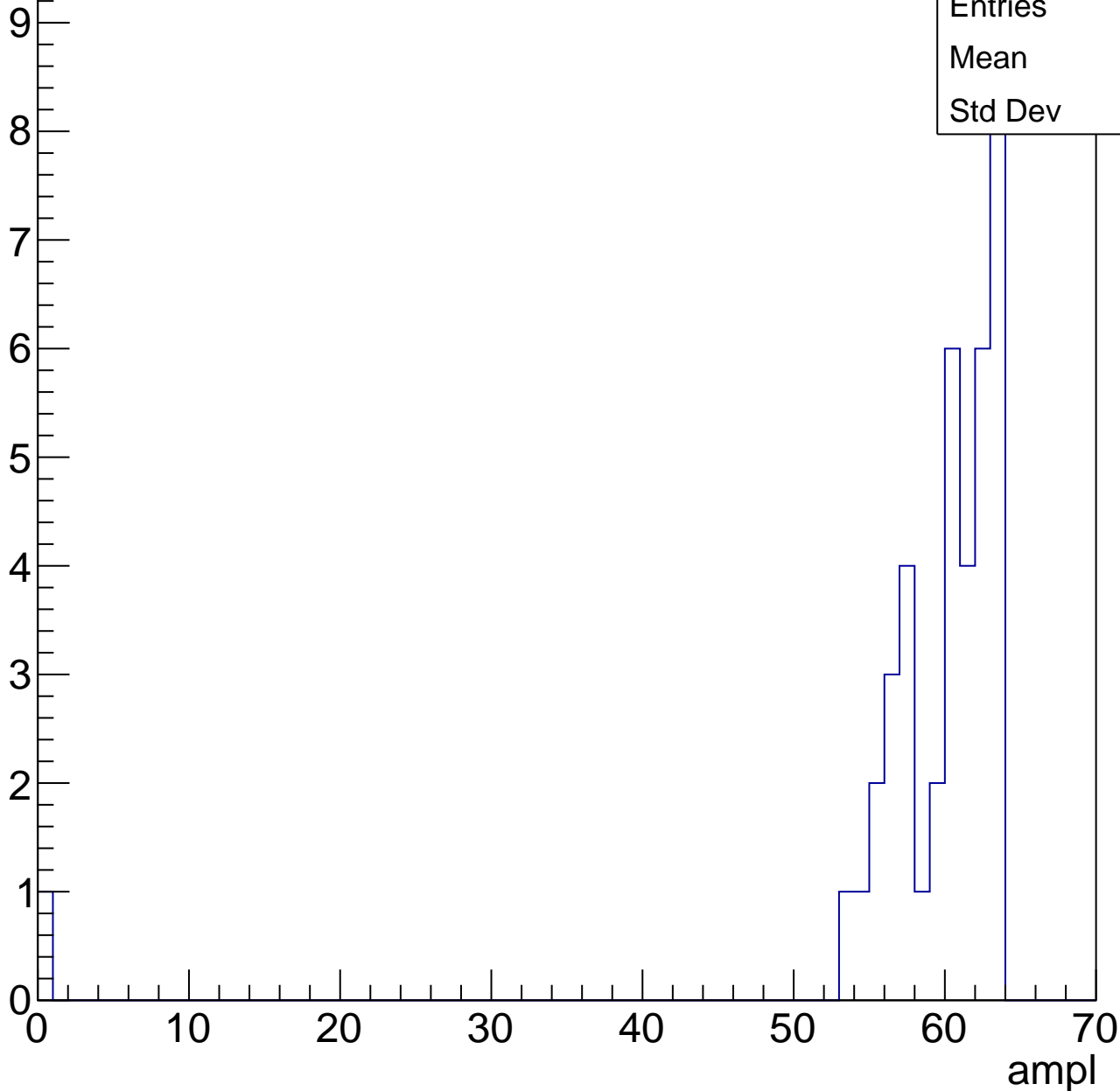


# B1L101S, U16-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	40
Mean	58.3
Std Dev	9.77



# B1L101S, U16-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L101S, U16-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U16-ch11, adc0

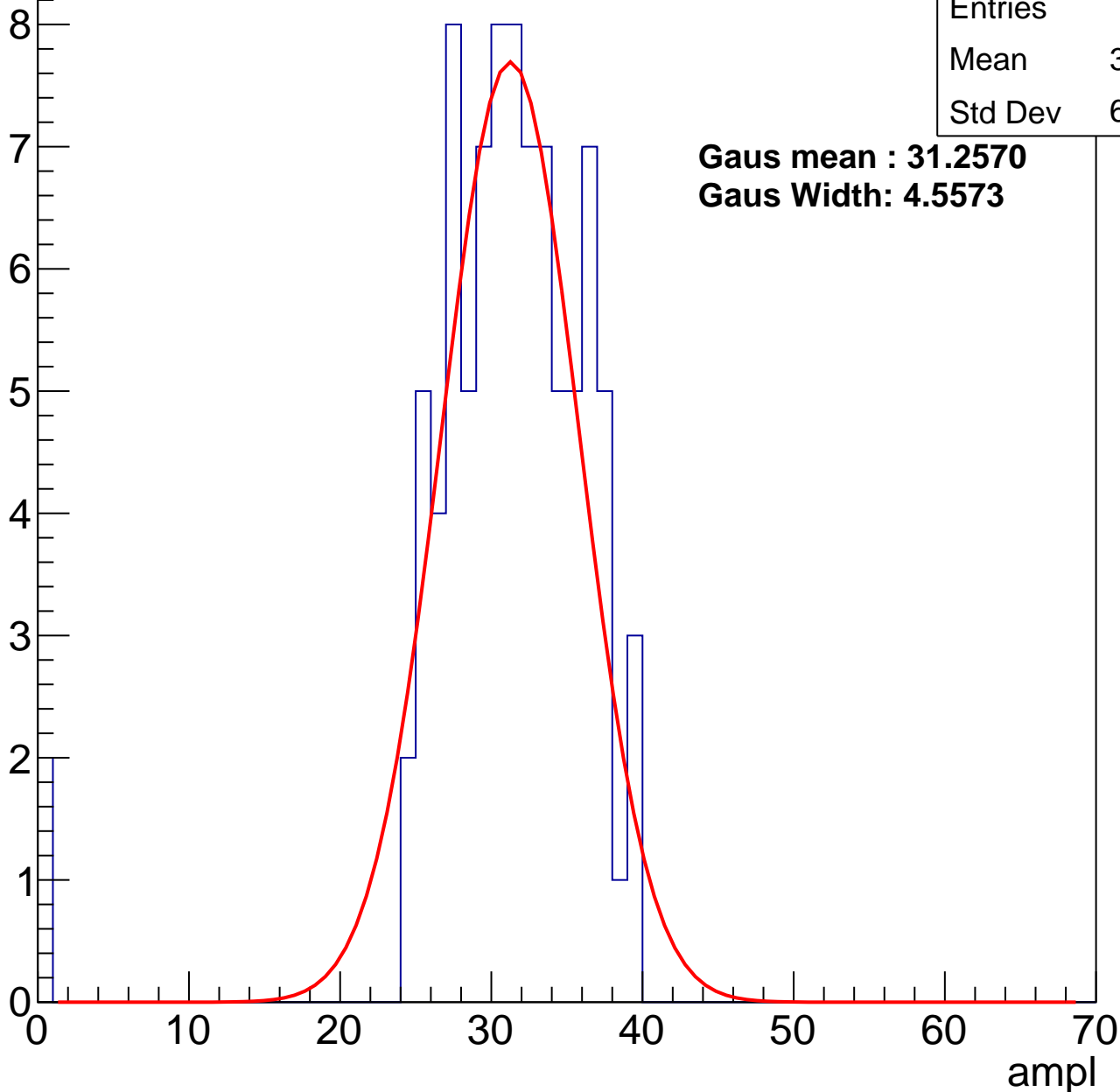
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	89
Mean	30.52
Std Dev	6.038

**Gaus mean : 31.2570**

**Gaus Width: 4.5573**



# B1L101S, U16-ch11, adc1

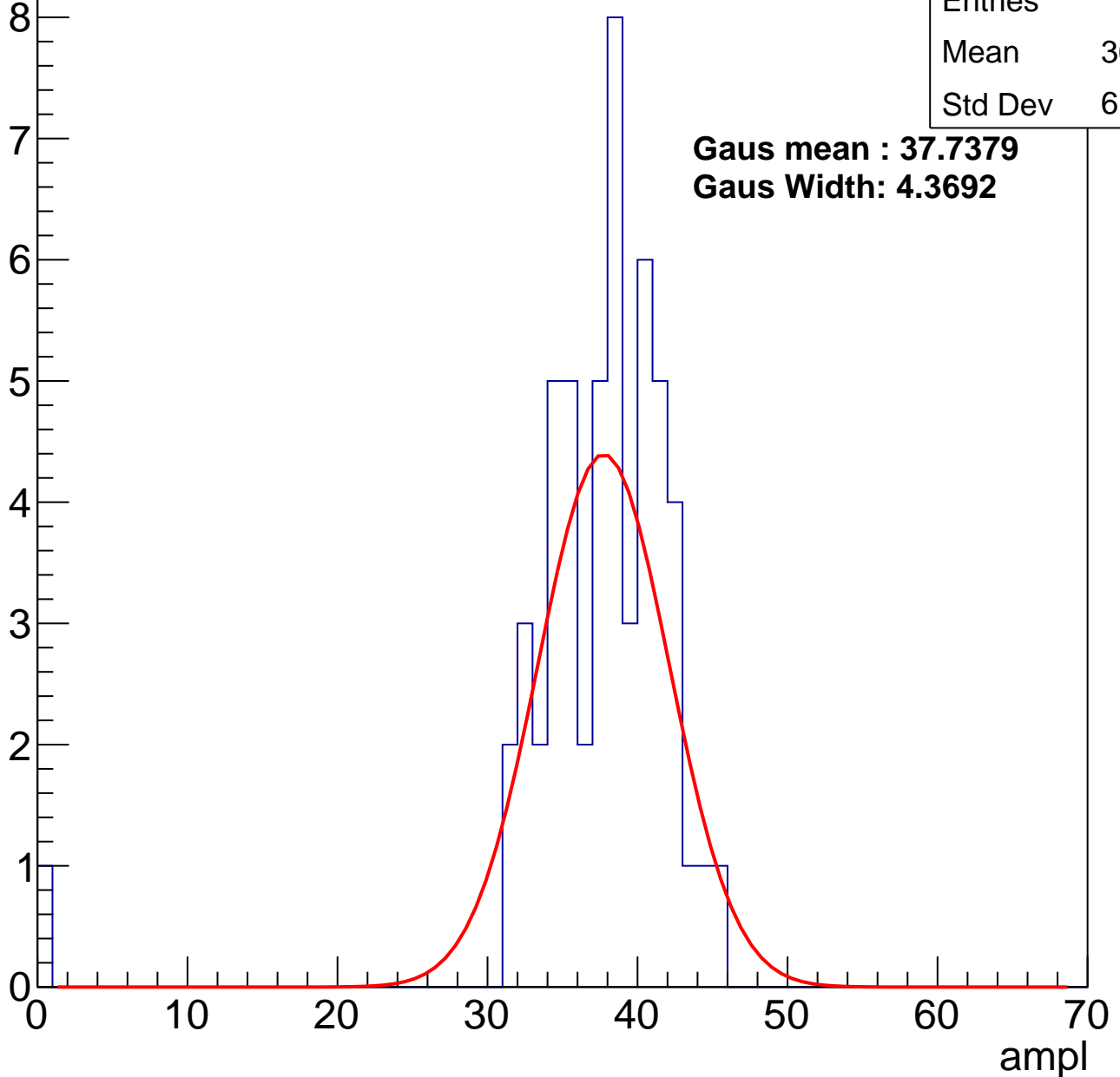
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	36.89
Std Dev	6.112

**Gaus mean : 37.7379**

**Gaus Width: 4.3692**



# B1L101S, U16-ch11, adc2

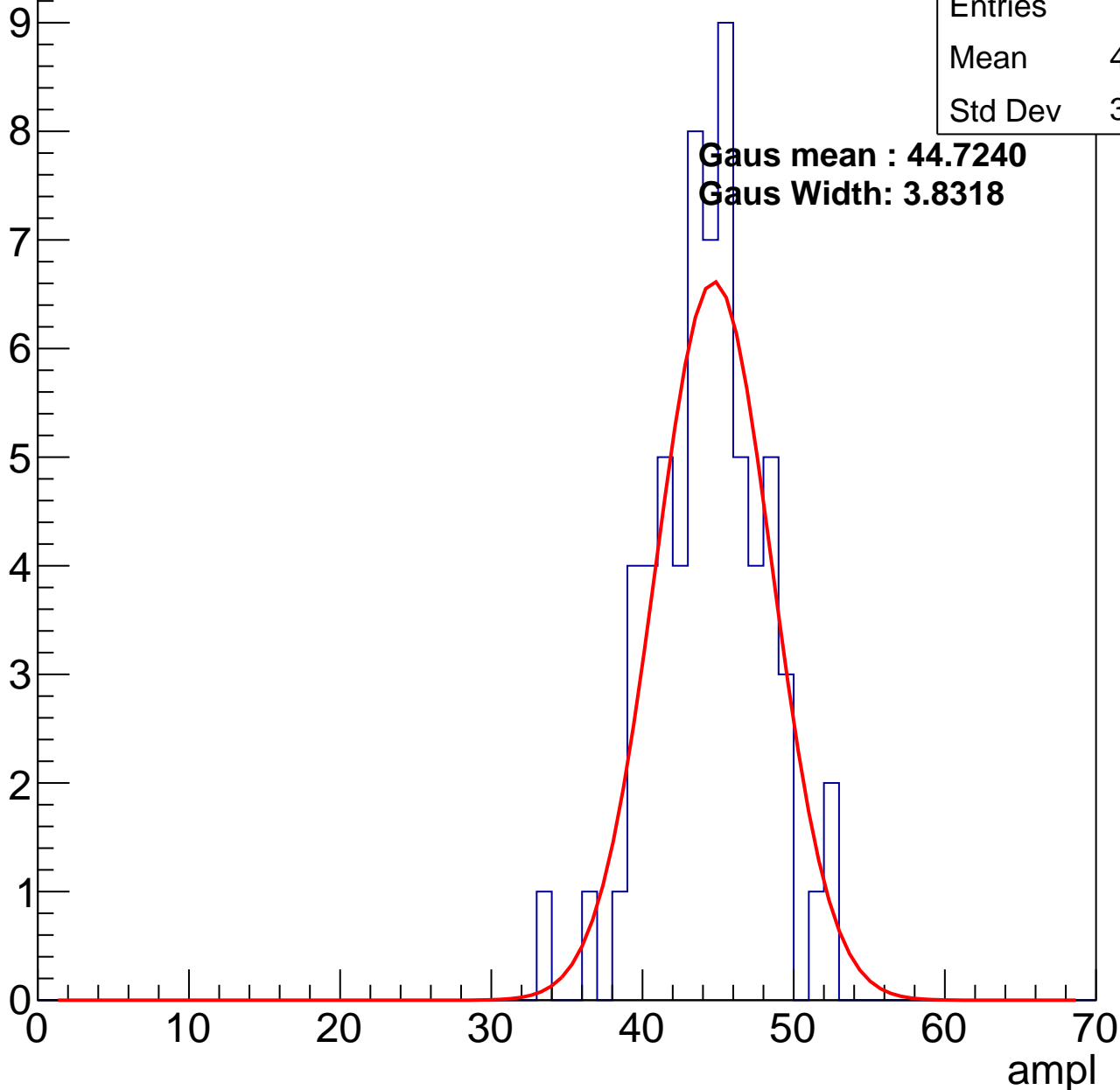
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	43.95
Std Dev	3.646

**Gaus mean : 44.7240**

**Gaus Width: 3.8318**

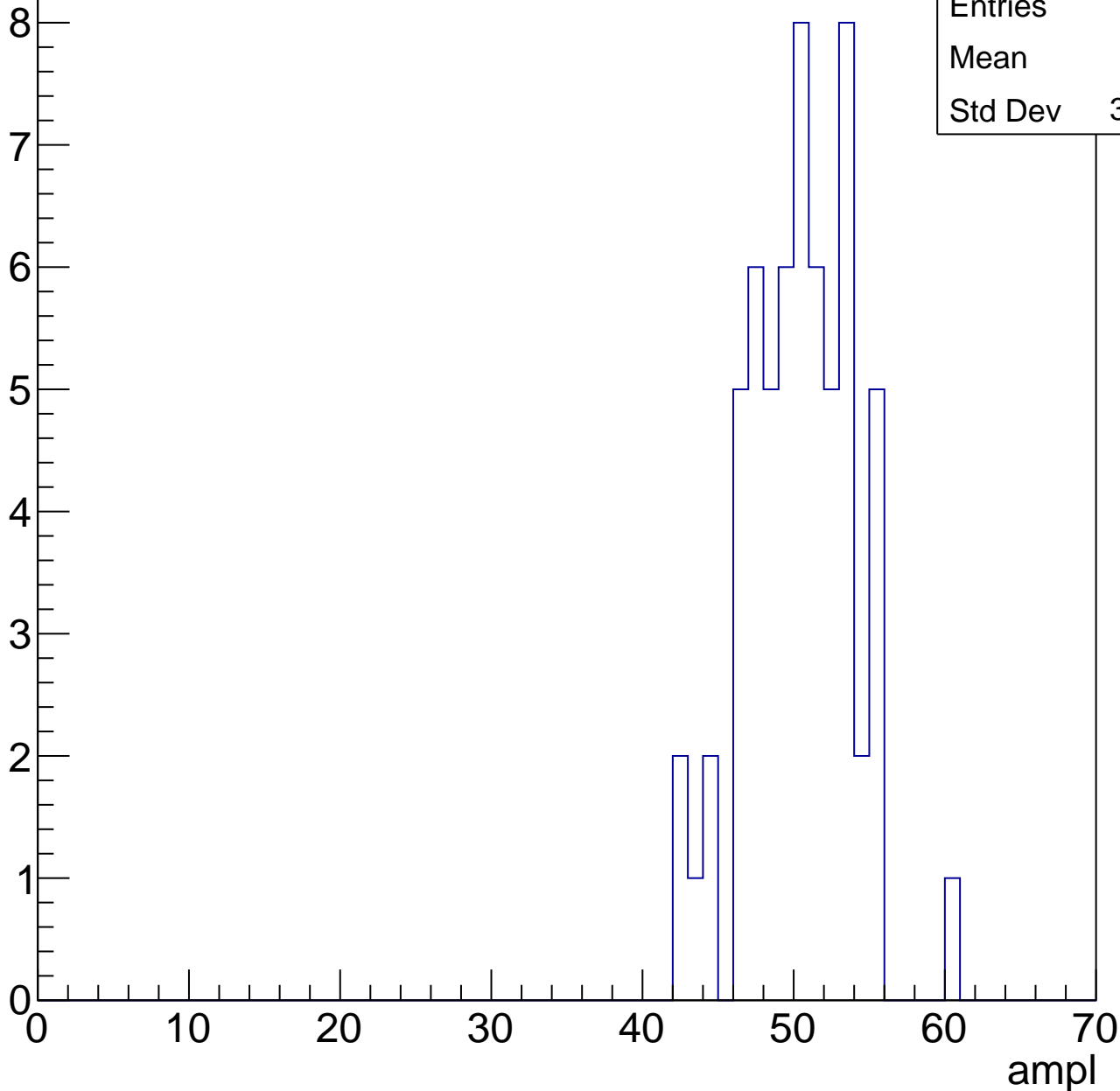


# B1L101S, U16-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

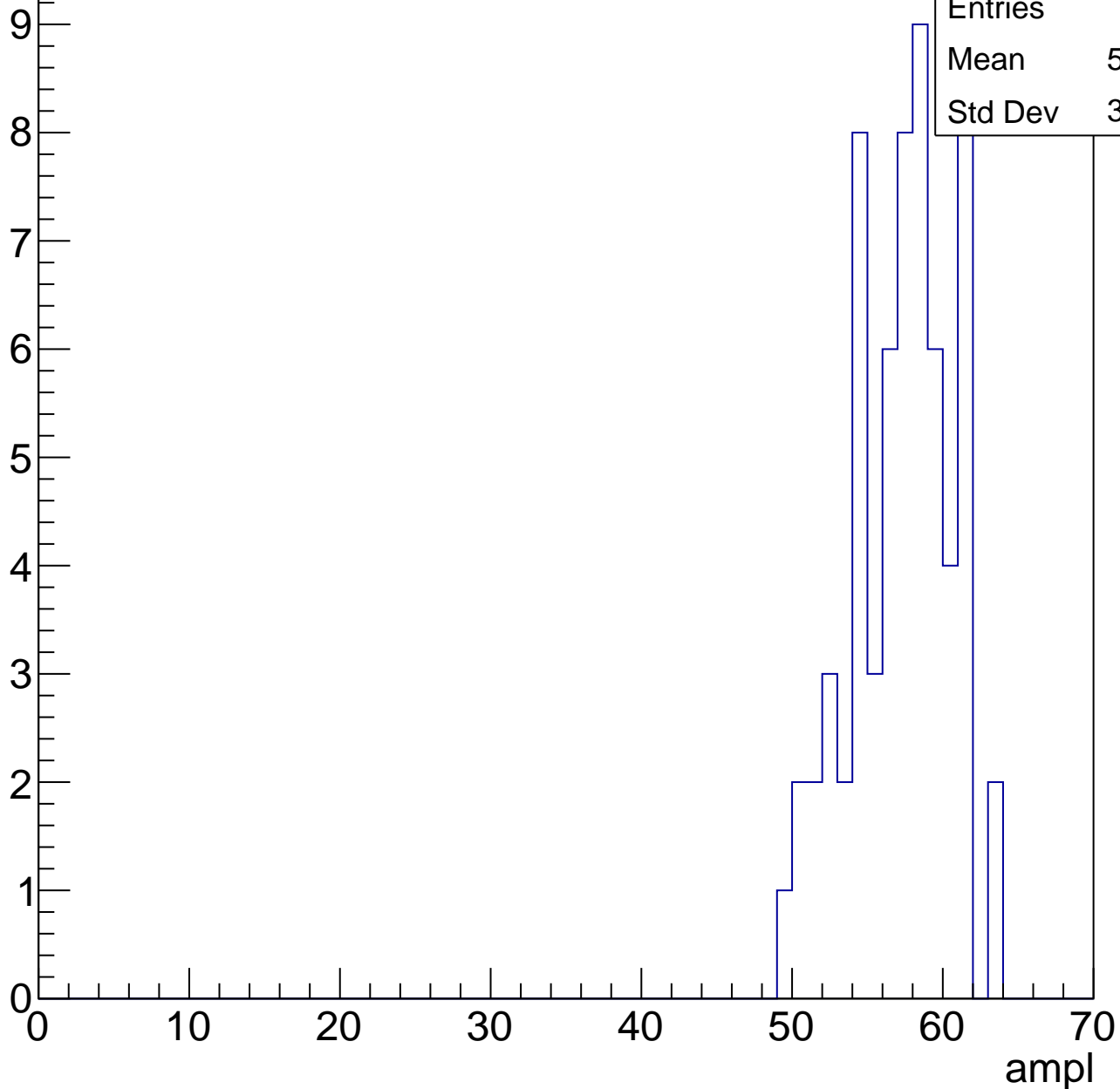
Entries	62
Mean	49.9
Std Dev	3.509



# B1L101S, U16-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

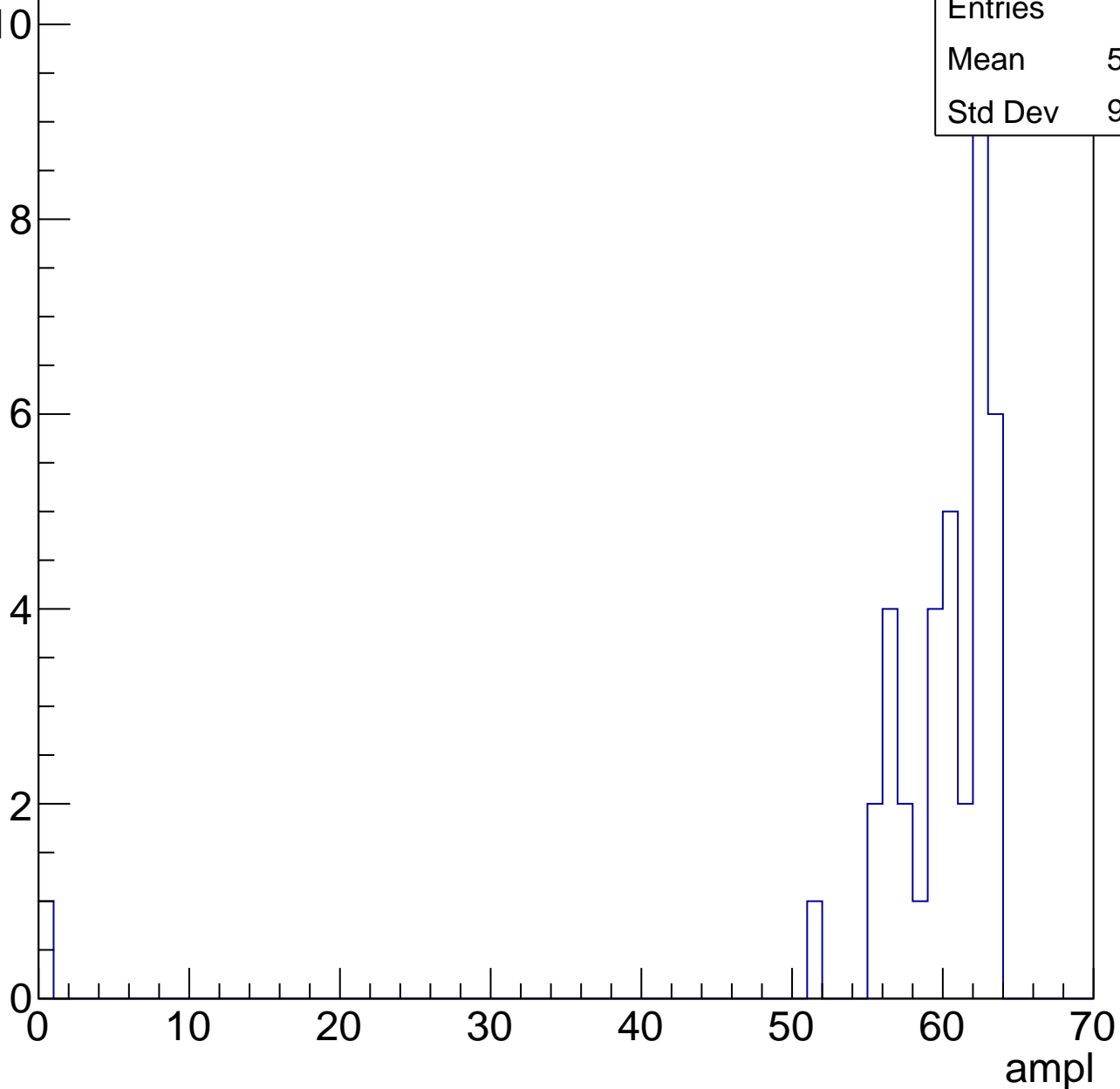


# B1L101S, U16-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	38
Mean	58.24
Std Dev	9.999



# B1L101S, U16-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	63
Std Dev	0



# B1L101S, U16-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U16-ch12, adc0

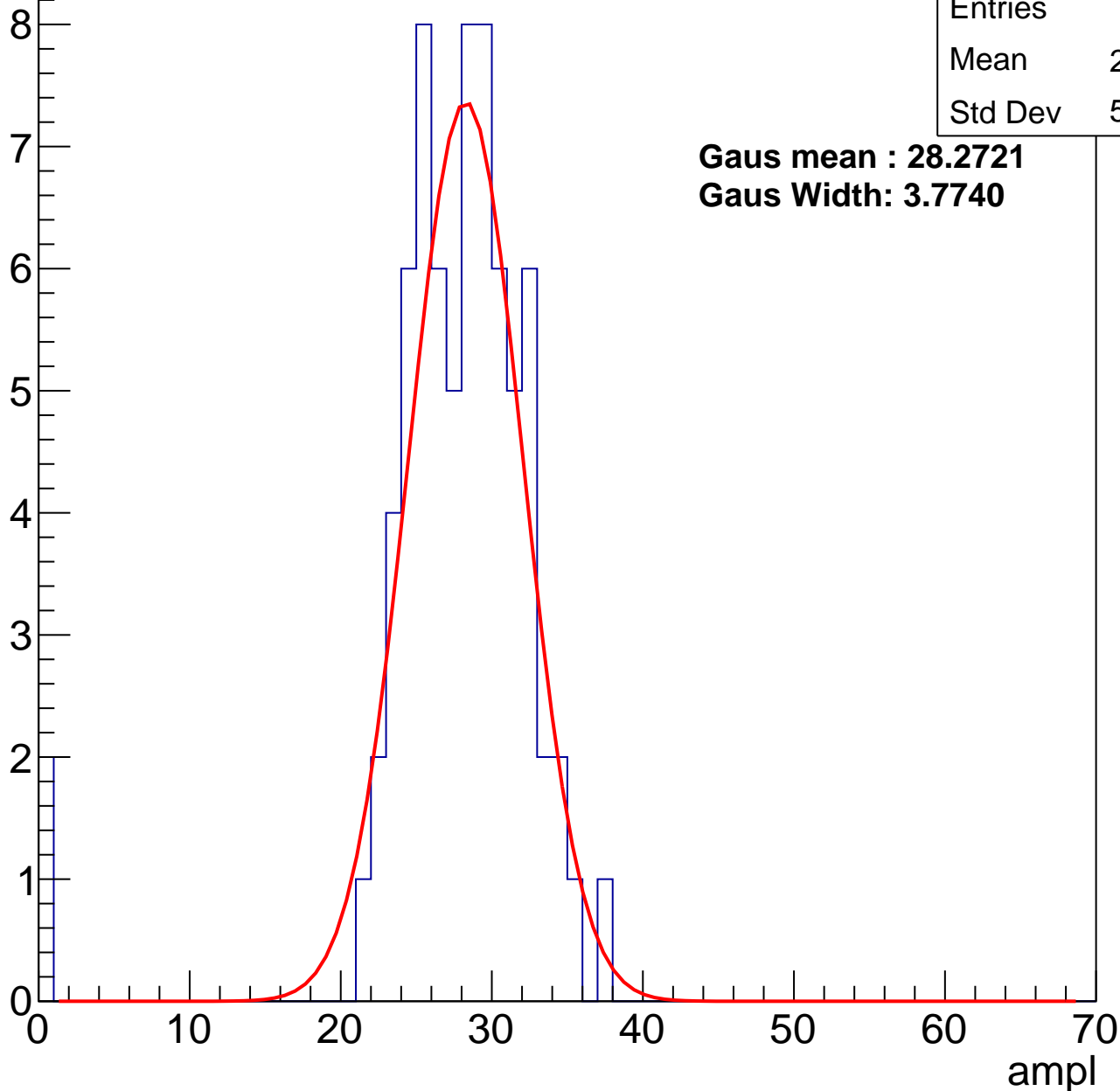
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	27.14
Std Dev	5.682

**Gaus mean : 28.2721**

**Gaus Width: 3.7740**



# B1L101S, U16-ch12, adc1

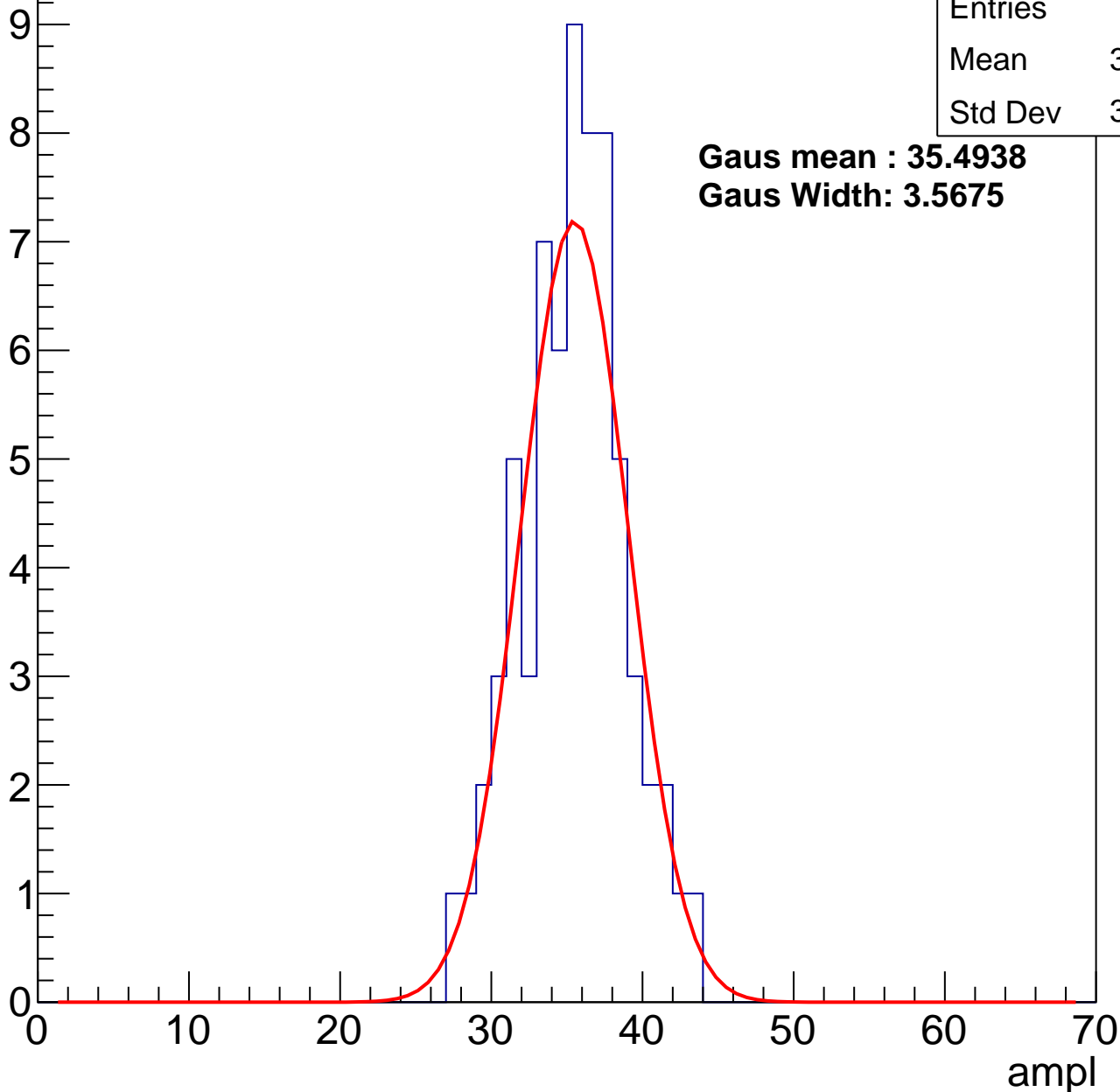
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	34.96
Std Dev	3.388

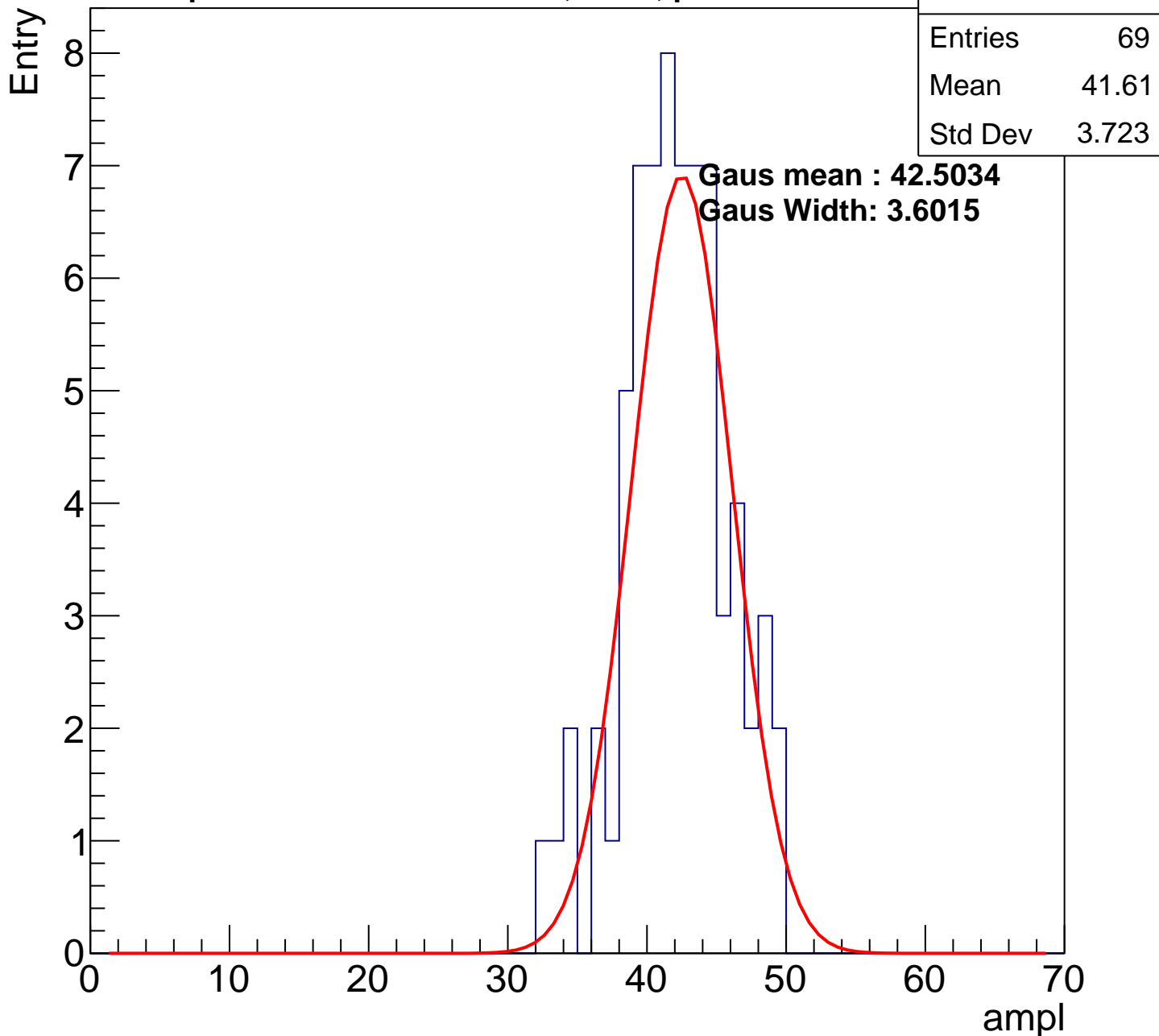
**Gaus mean : 35.4938**

**Gaus Width: 3.5675**



# B1L101S, U16-ch12, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

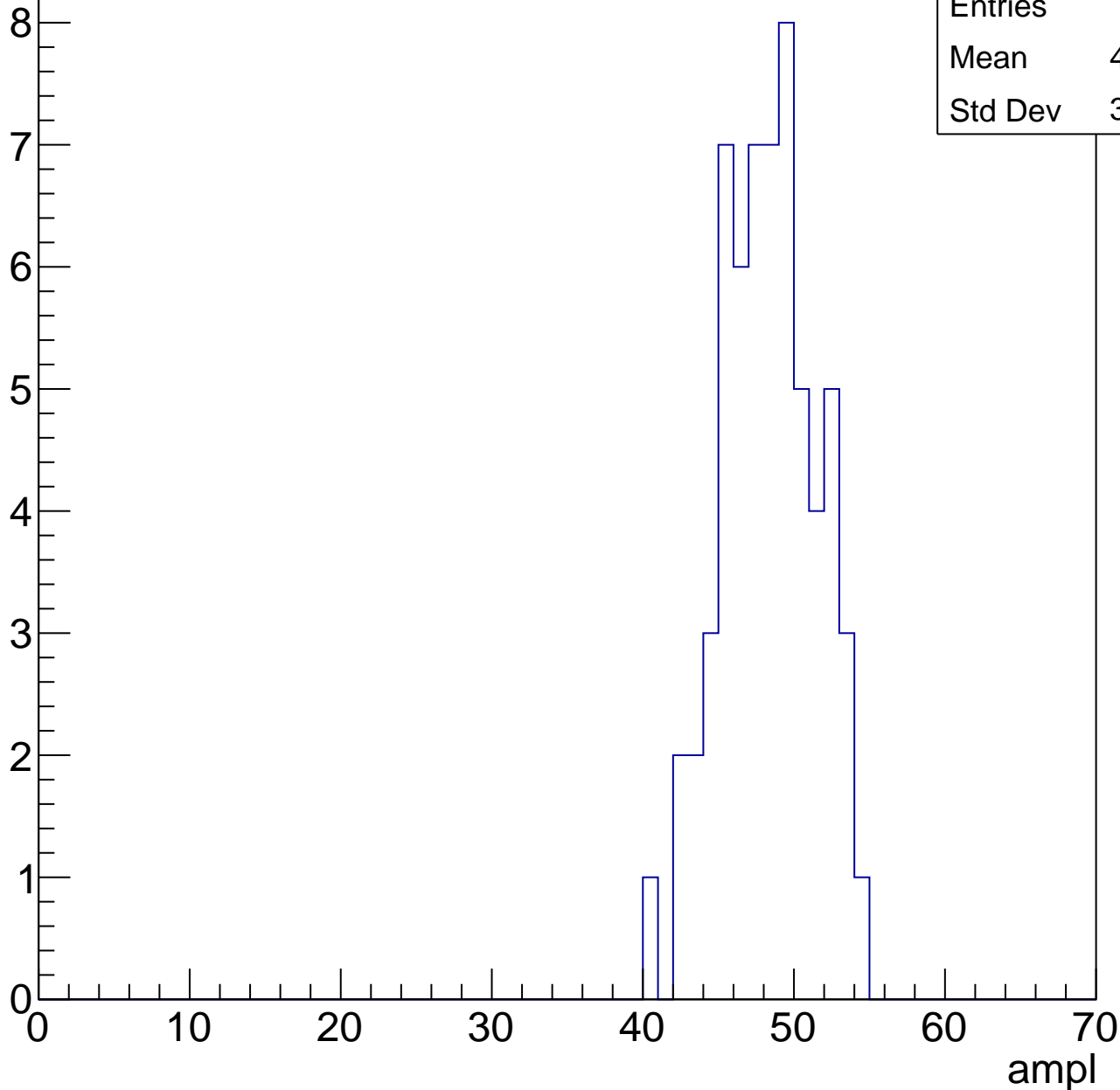


# B1L101S, U16-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

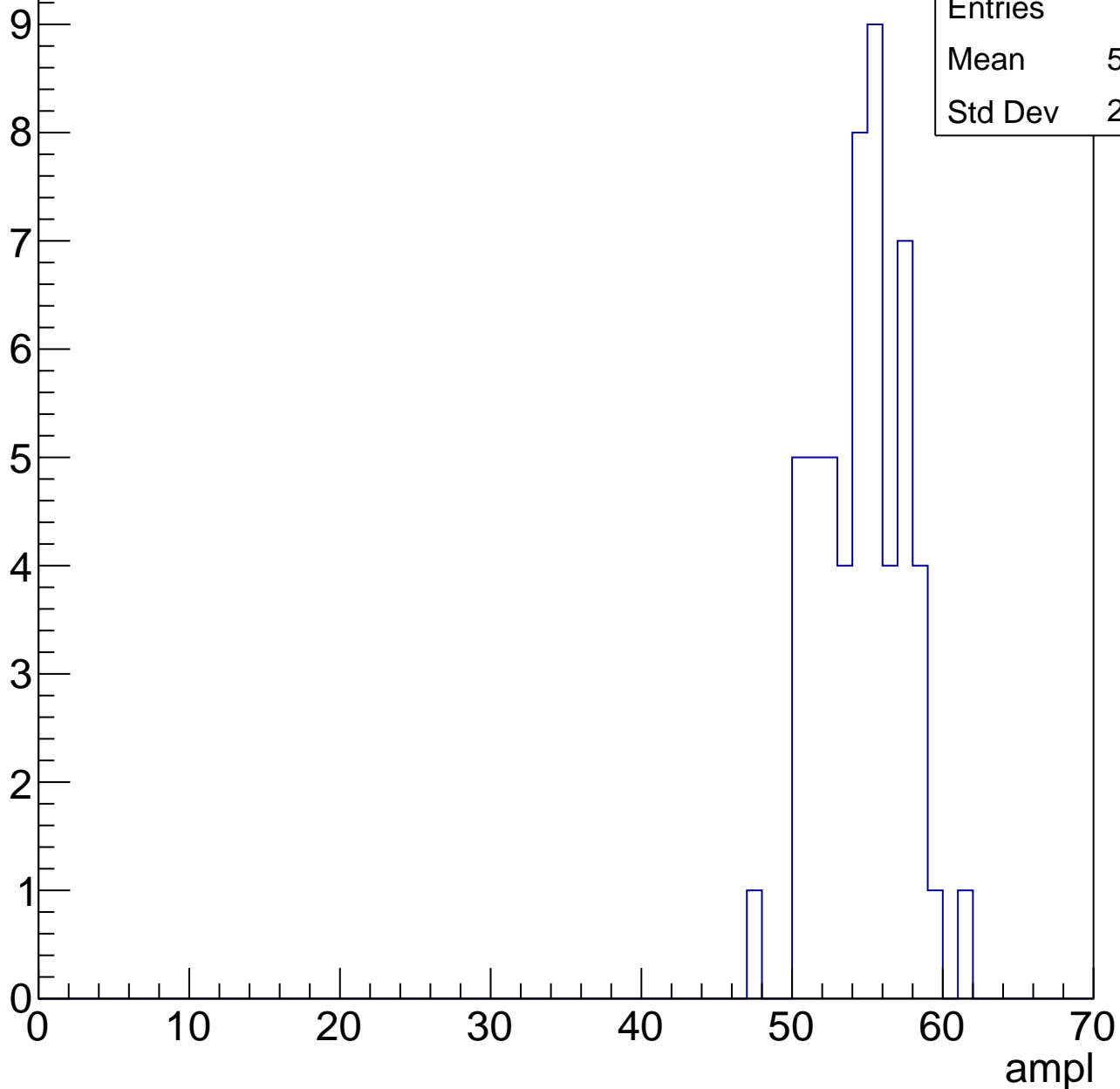
Entries	61
Mean	47.82
Std Dev	3.086



# B1L101S, U16-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



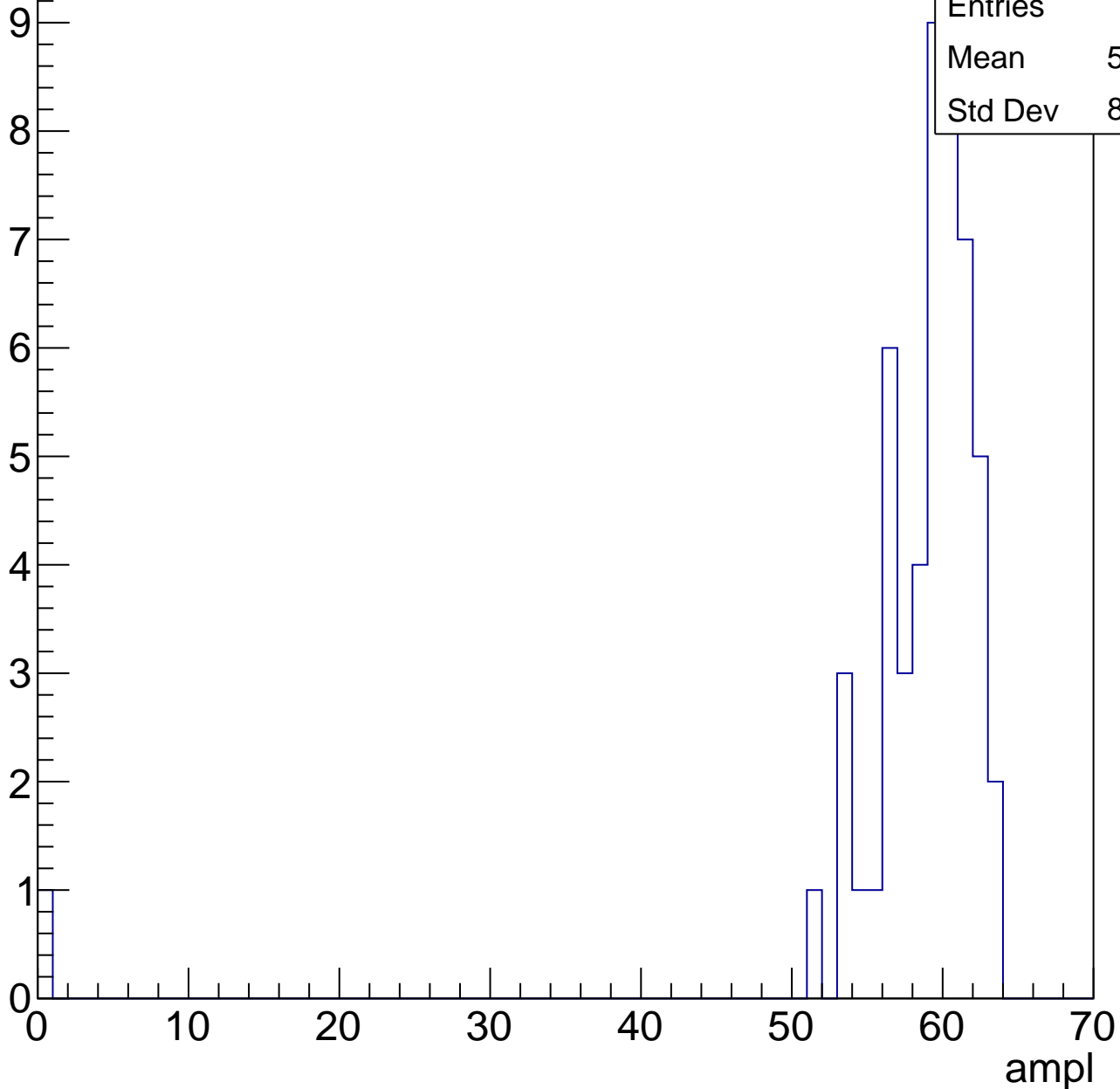
Entries	54
Mean	54.19
Std Dev	2.796

# B1L101S, U16-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	57.49
Std Dev	8.587

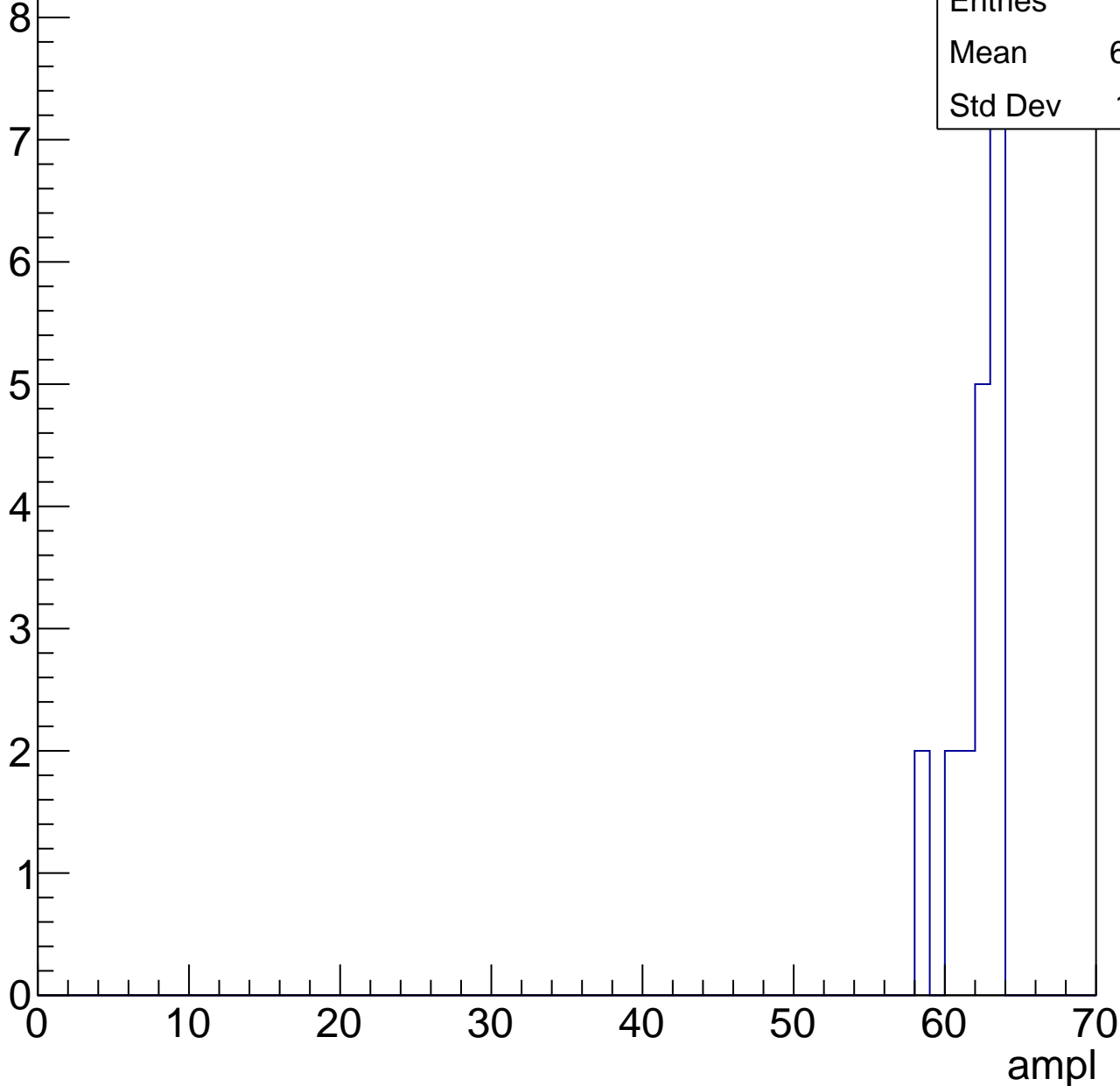


# B1L101S, U16-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	19
Mean	61.68
Std Dev	1.591

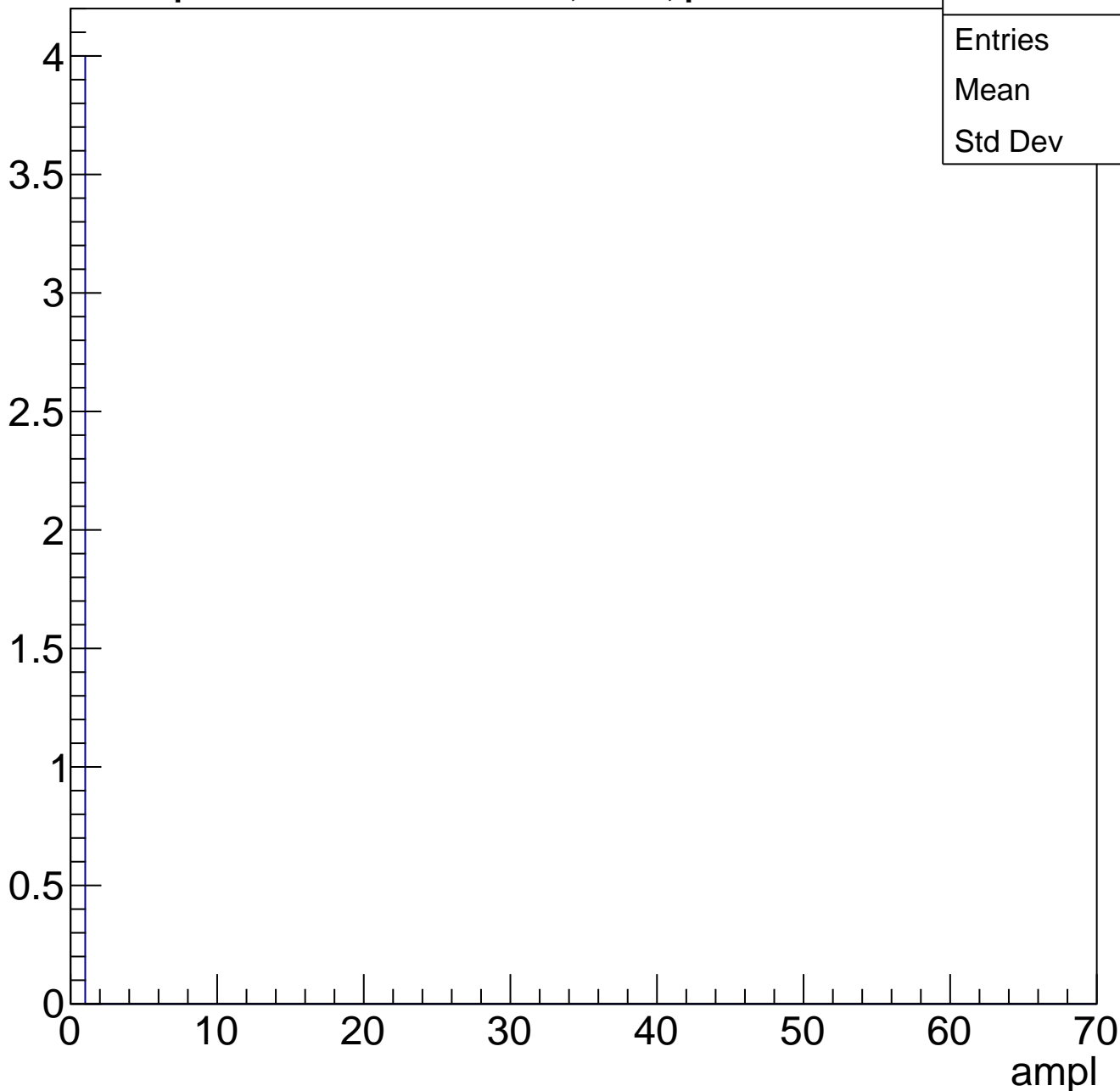




# B1L101S, U16-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	4
Mean	0
Std Dev	0

# B1L101S, U16-ch13, adc0

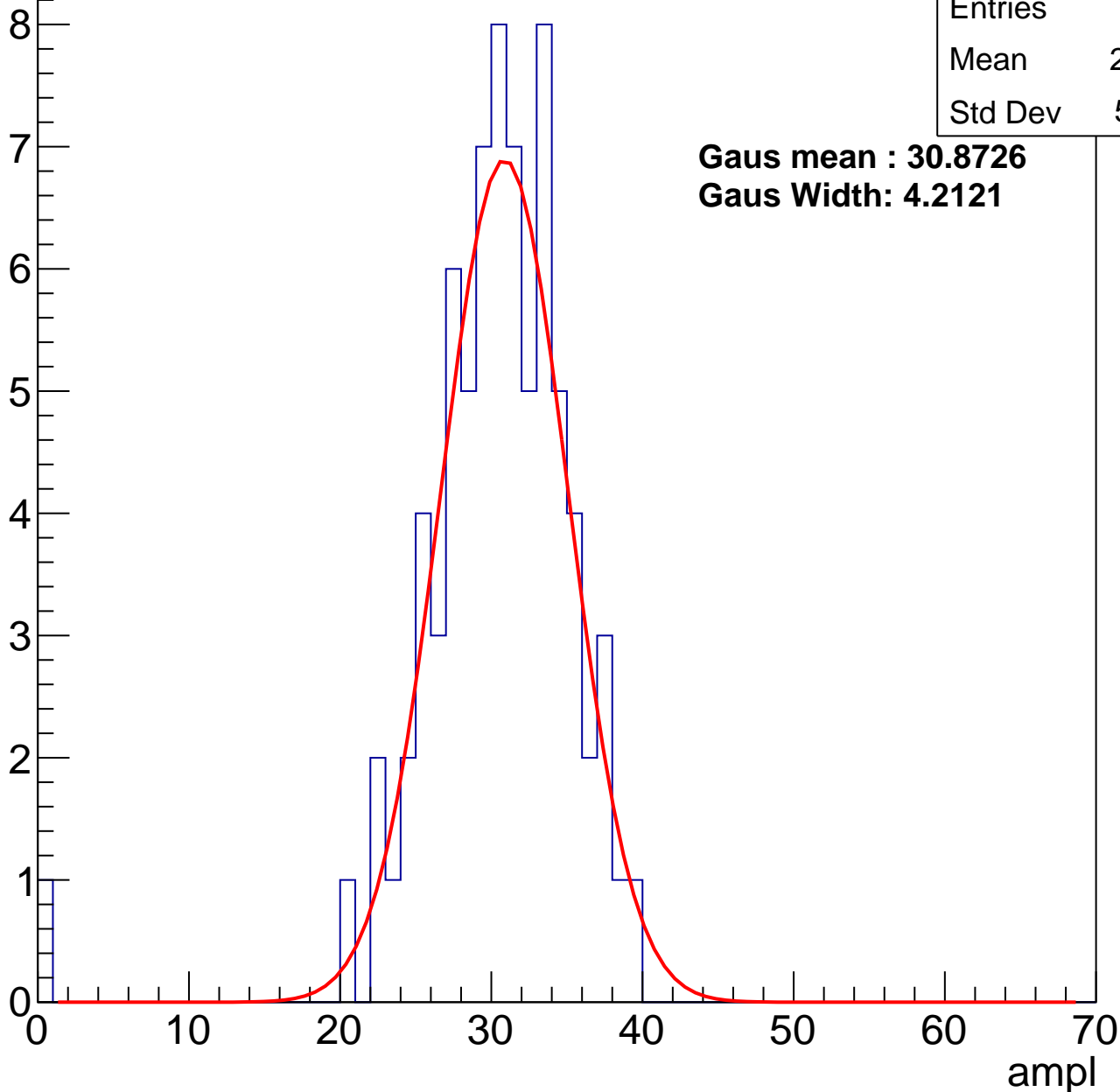
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	29.86
Std Dev	5.281

**Gaus mean : 30.8726**

**Gaus Width: 4.2121**



# B1L101S, U16-ch13, adc1

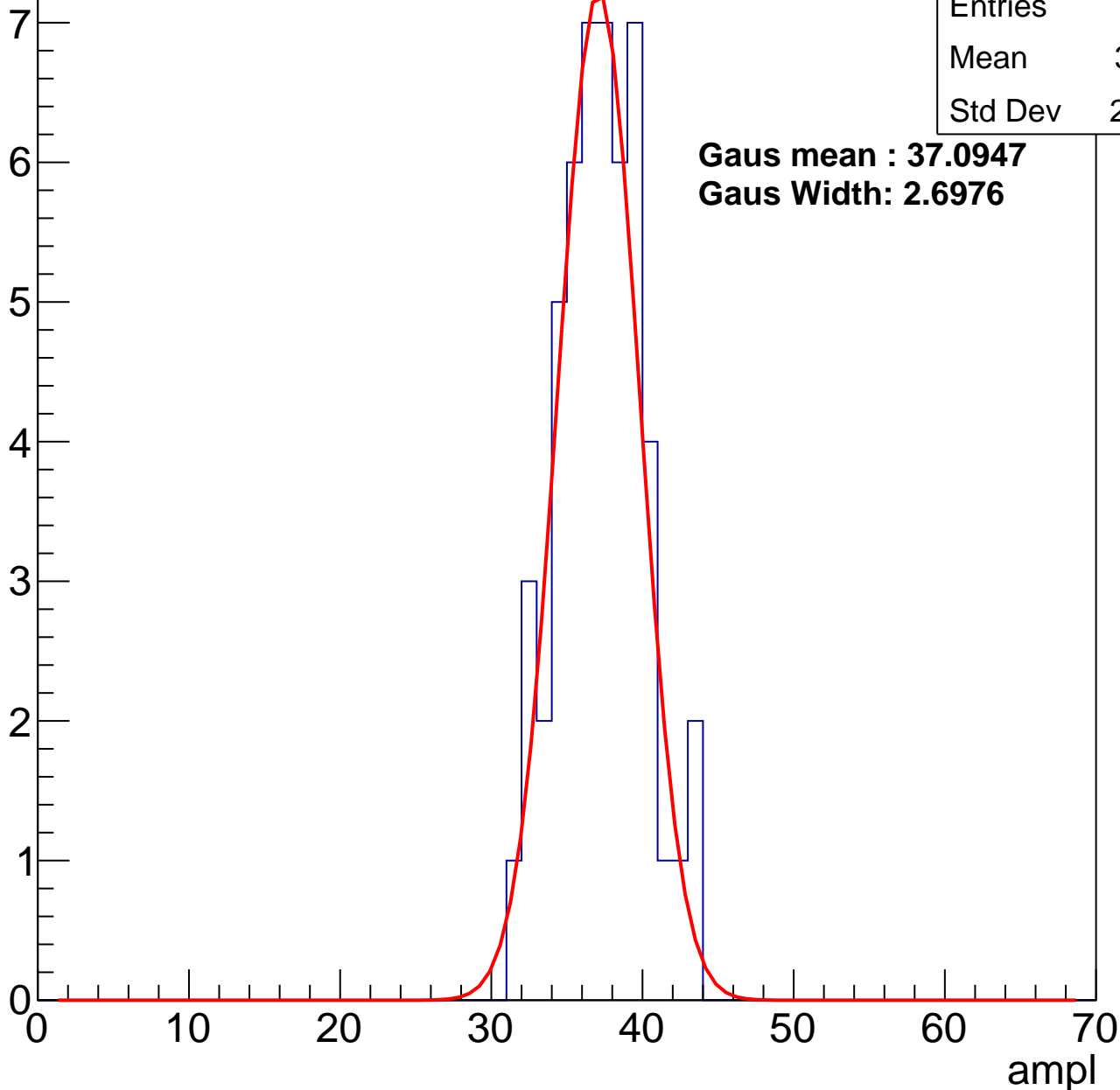
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	36.81
Std Dev	2.774

**Gaus mean : 37.0947**

**Gaus Width: 2.6976**



# B1L101S, U16-ch13, adc2

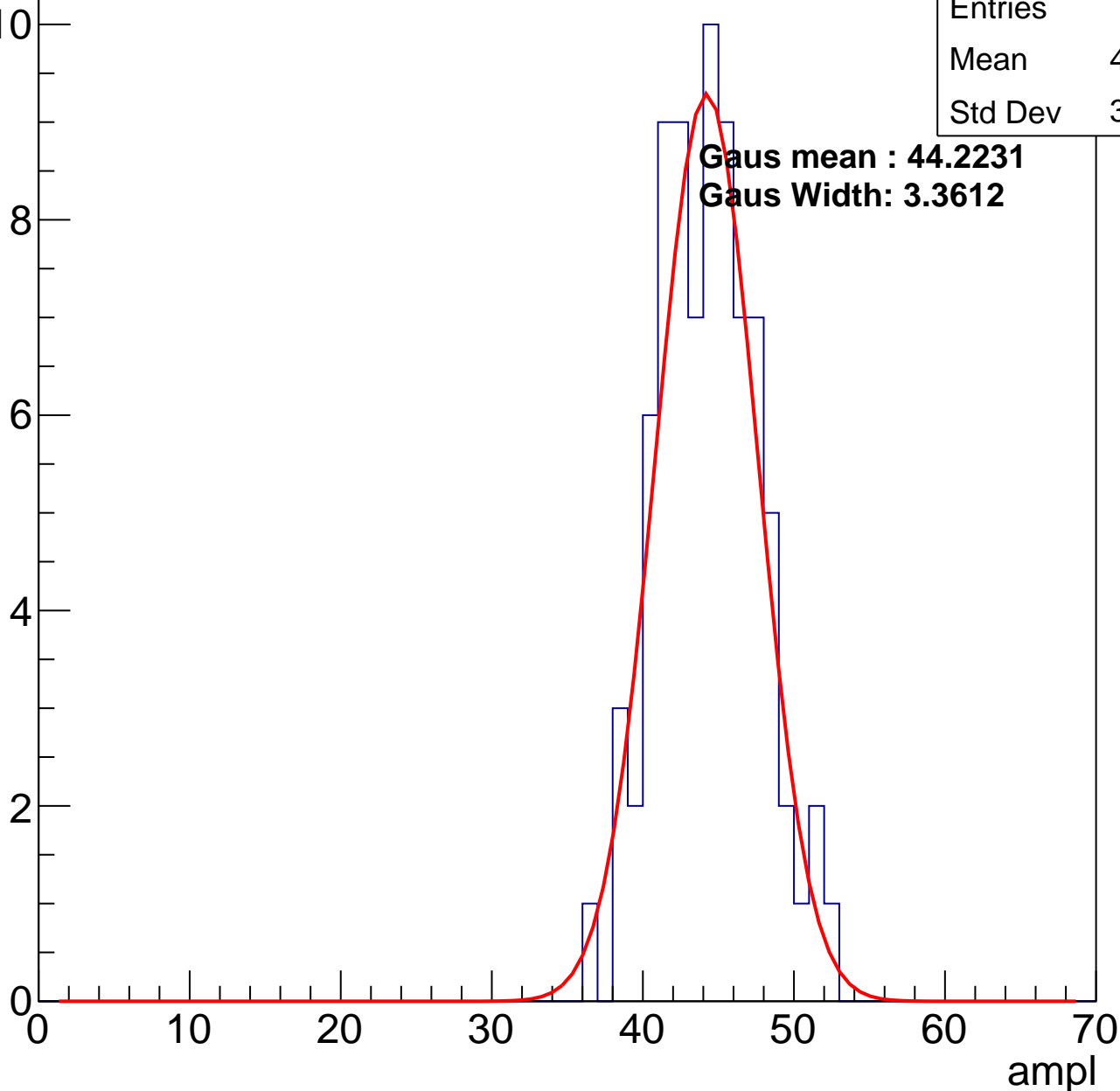
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	43.88
Std Dev	3.275

**Gaus mean : 44.2231**

**Gaus Width: 3.3612**

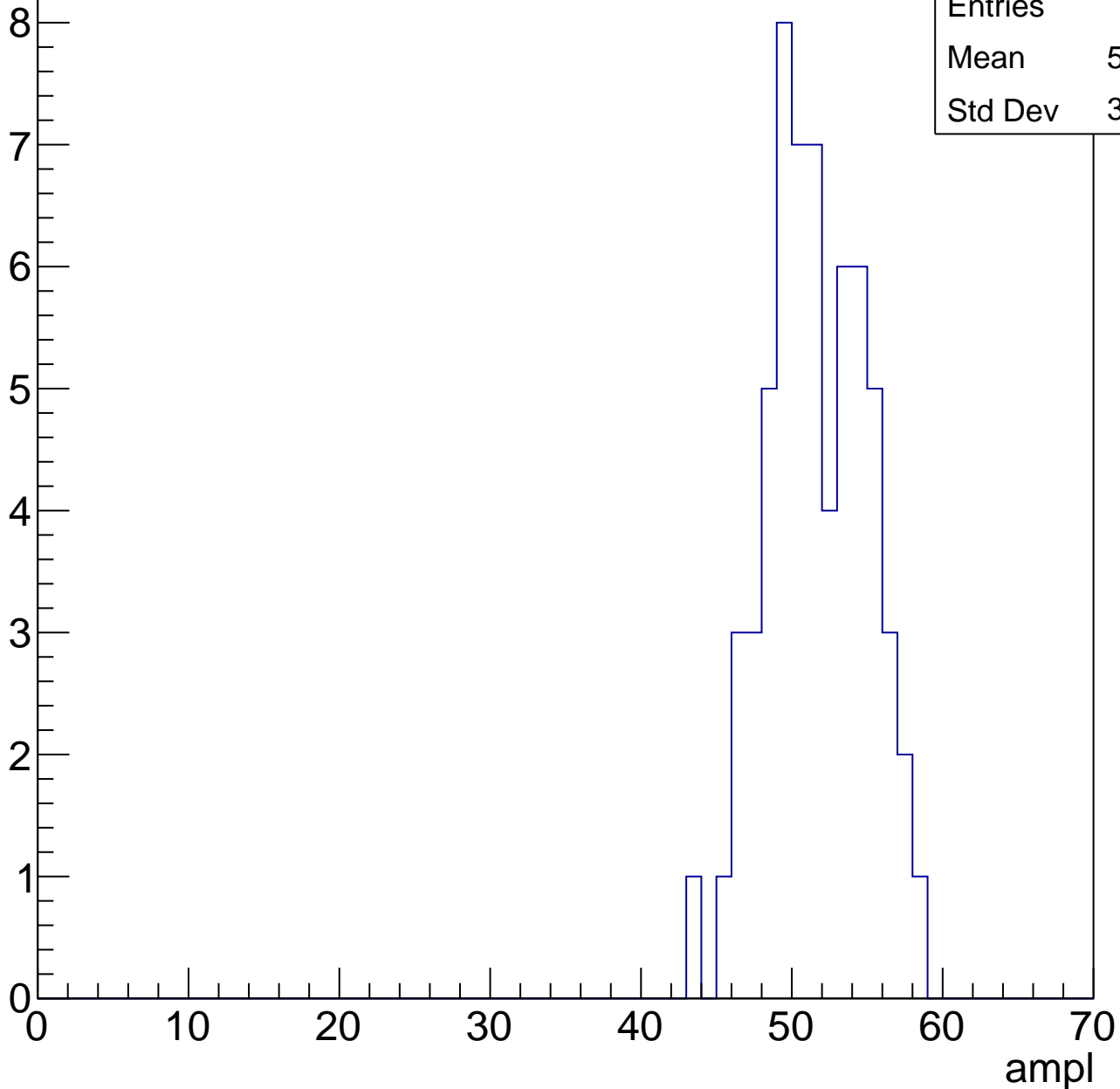


# B1L101S, U16-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	51.15
Std Dev	3.272

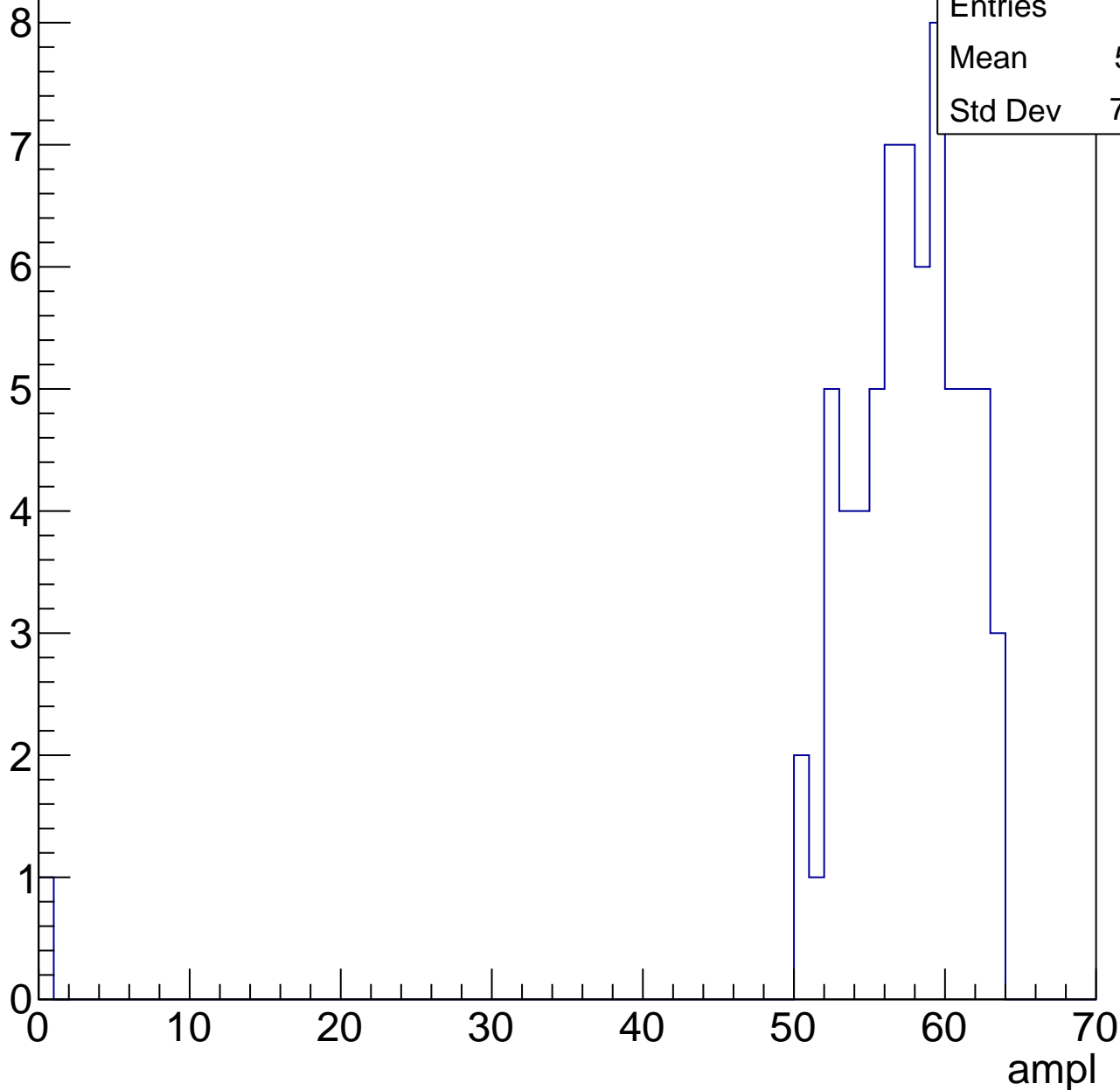


# B1L101S, U16-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	56.31
Std Dev	7.668



# B1L101S, U16-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

5

4

3

2

1

0

Entries	26
Mean	60.73
Std Dev	1.744

10

20

30

40

50

60

70

ampl

# B1L101S, U16-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U16-ch14, adc0

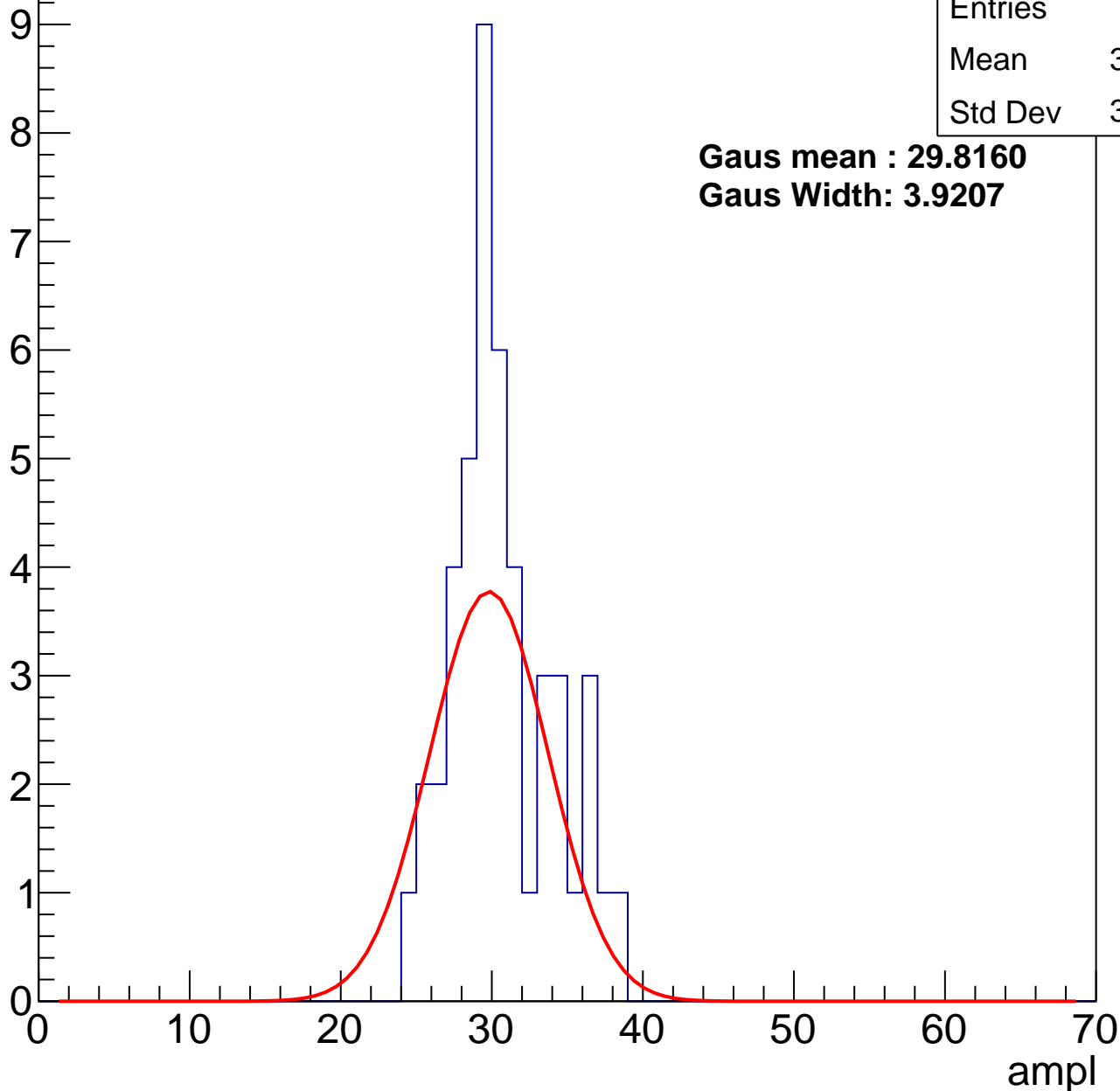
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	30.22
Std Dev	3.329

**Gaus mean : 29.8160**

**Gaus Width: 3.9207**



# B1L101S, U16-ch14, adc1

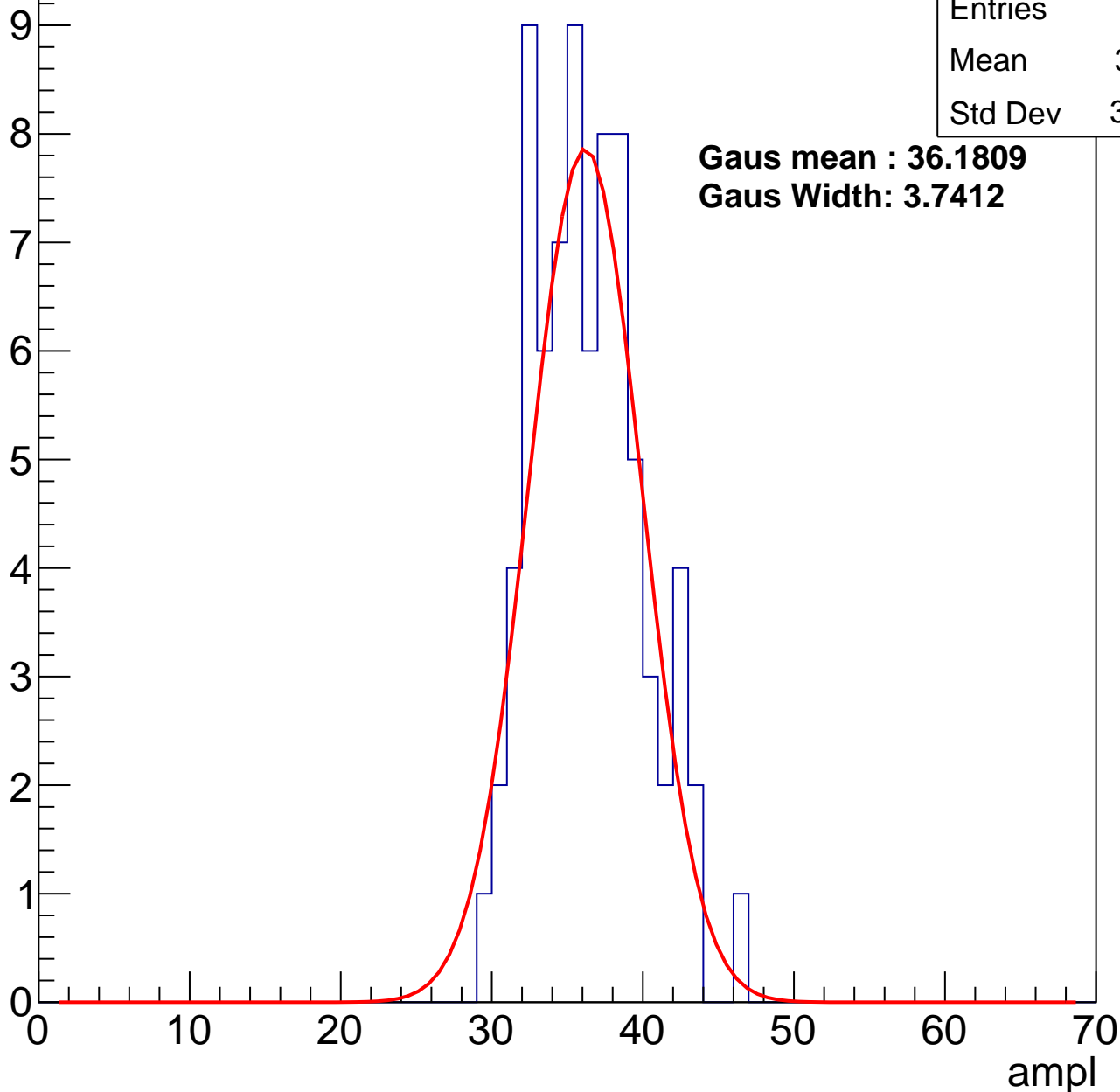
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	35.91
Std Dev	3.568

**Gaus mean : 36.1809**

**Gaus Width: 3.7412**



# B1L101S, U16-ch14, adc2

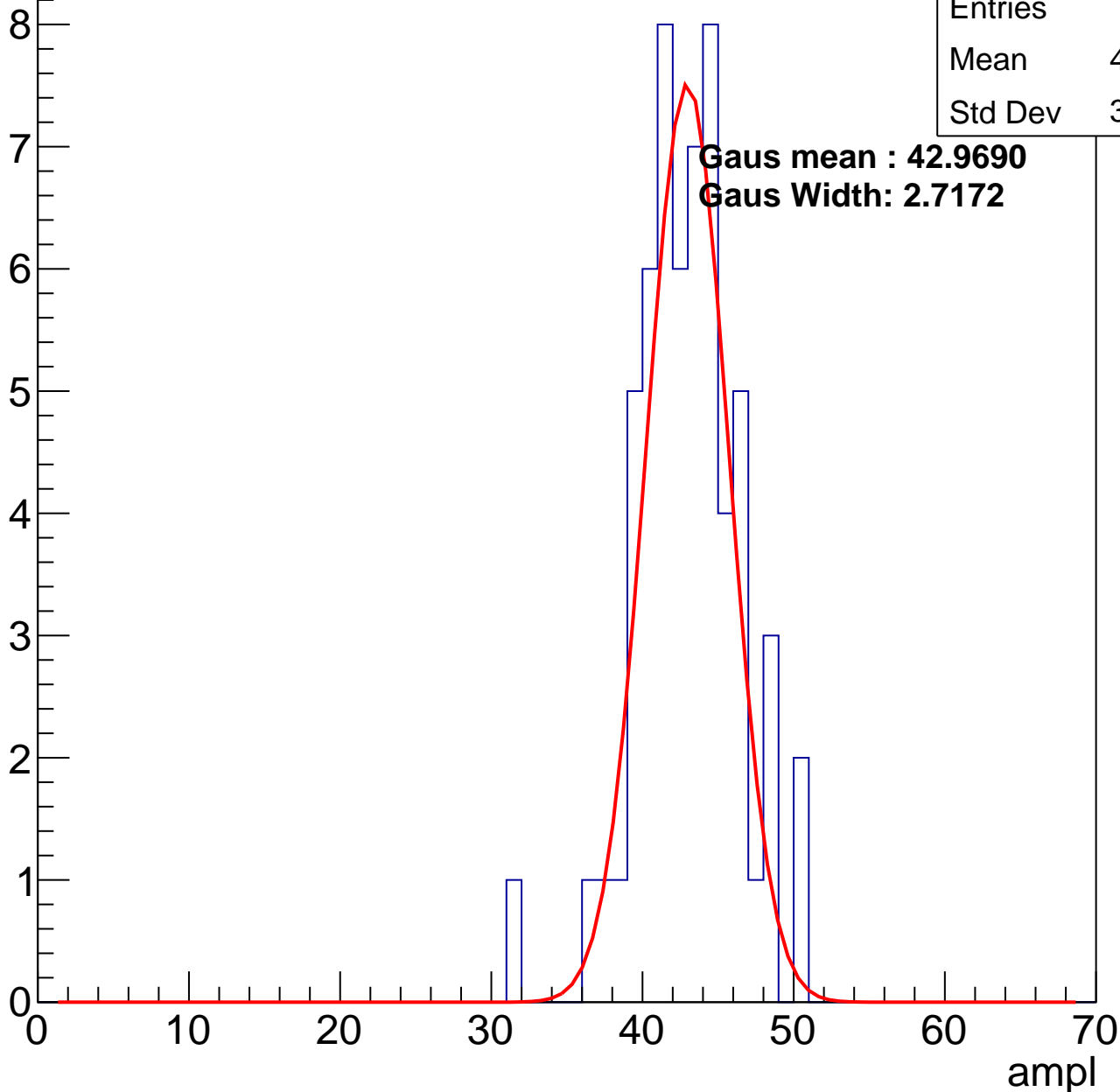
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	42.56
Std Dev	3.376

**Gaus mean : 42.9690**

**Gaus Width: 2.7172**

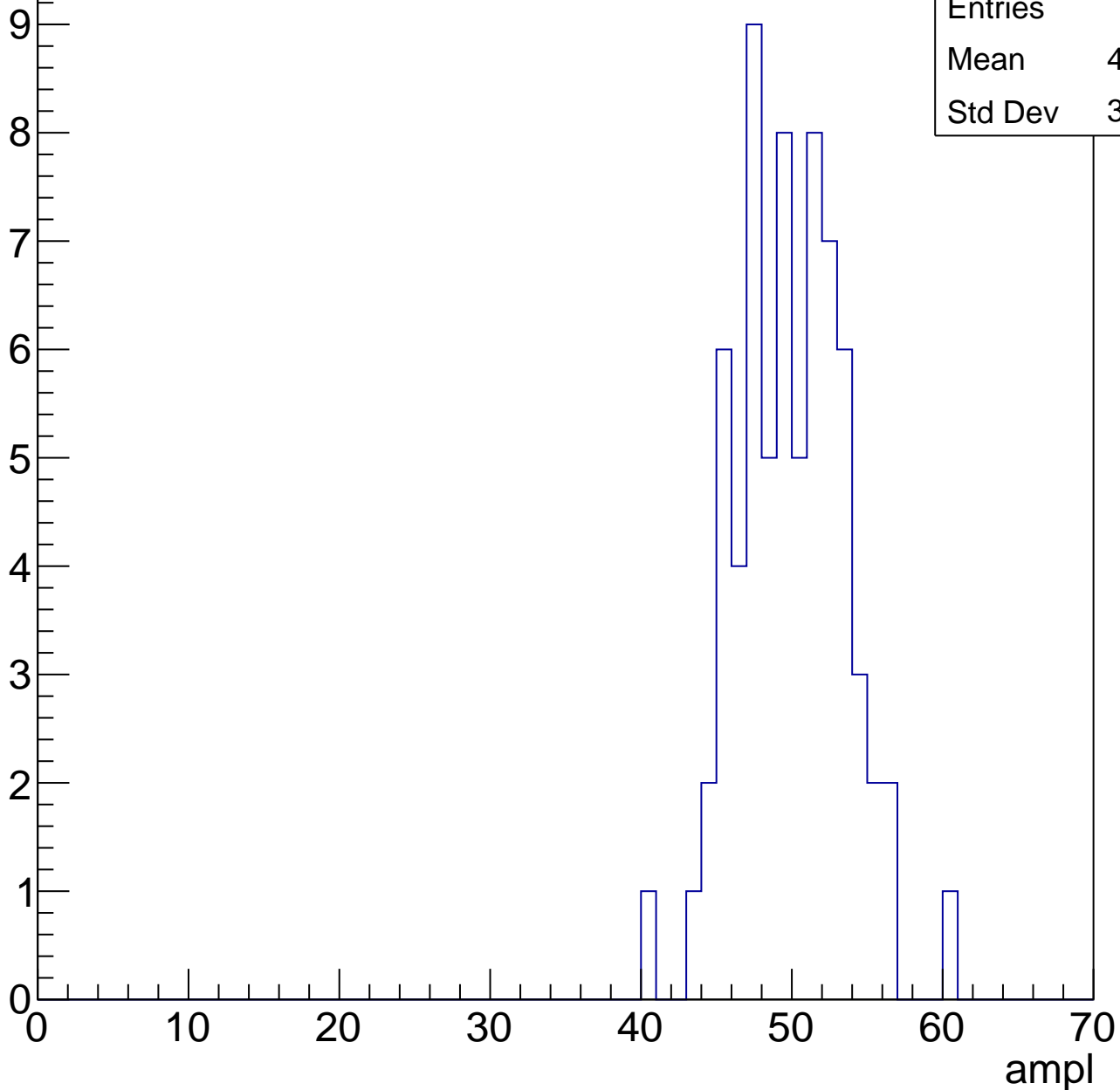


# B1L101S, U16-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	49.49
Std Dev	3.557

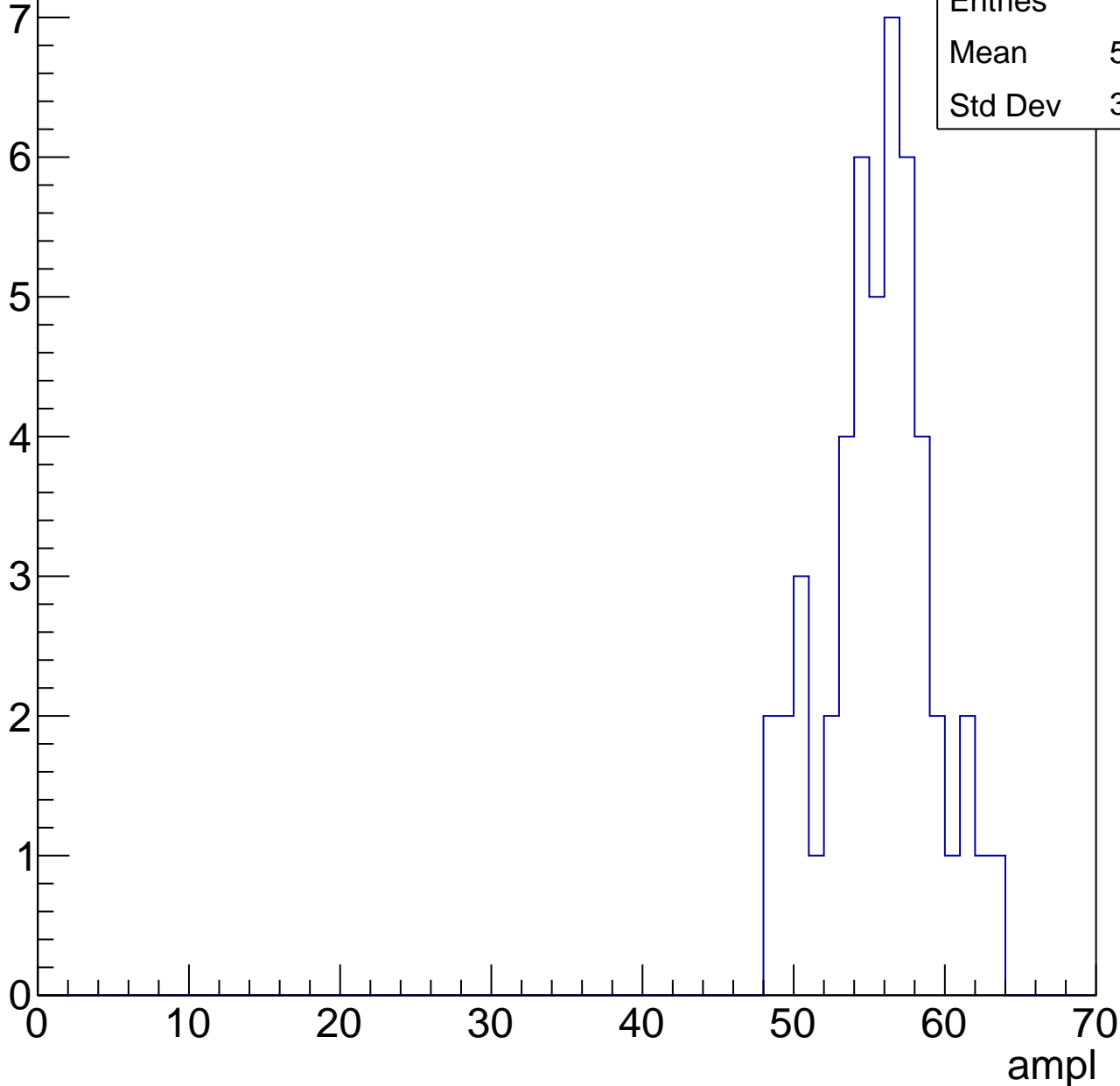


# B1L101S, U16-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	55.12
Std Dev	3.526

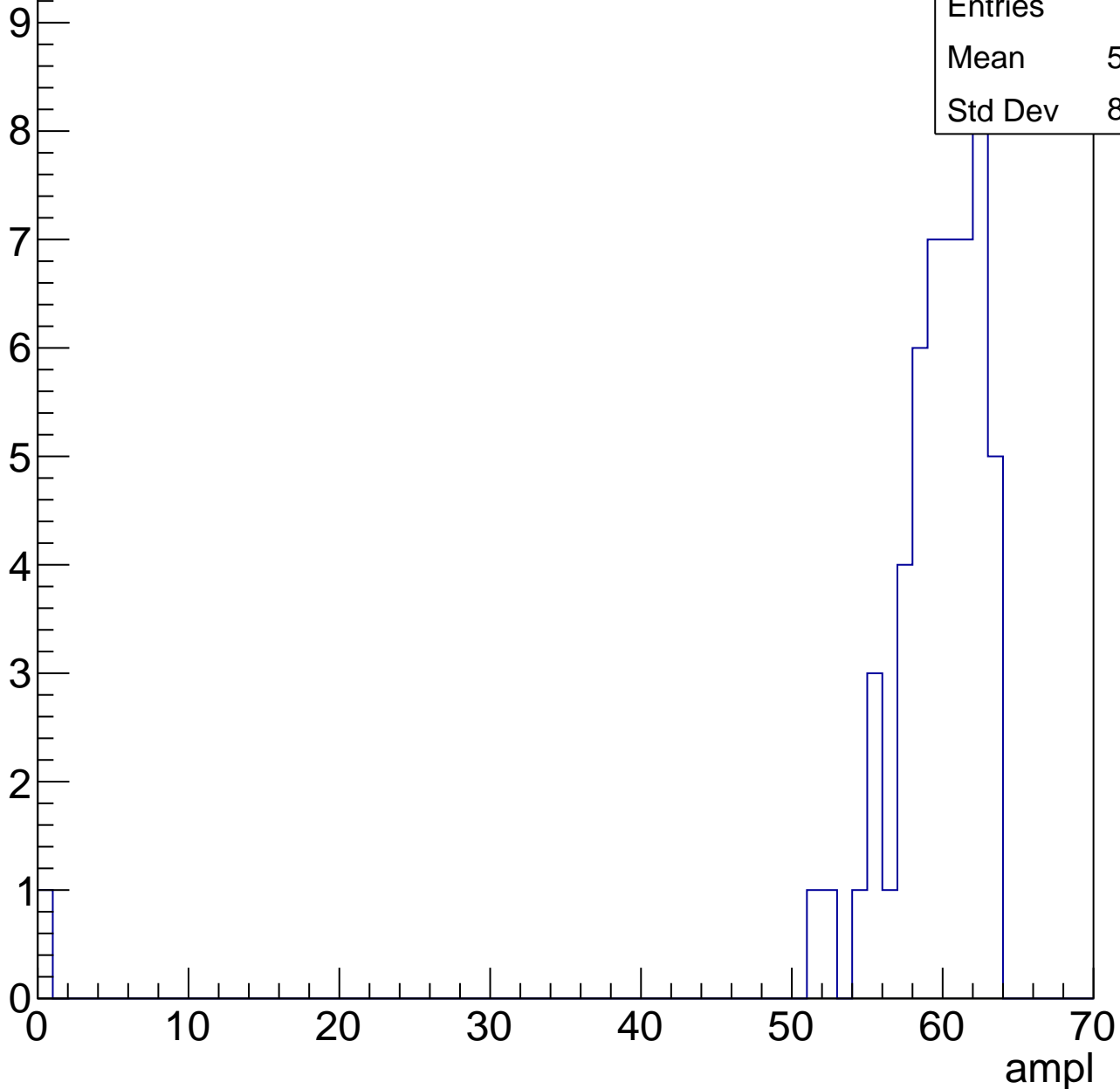


# B1L101S, U16-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

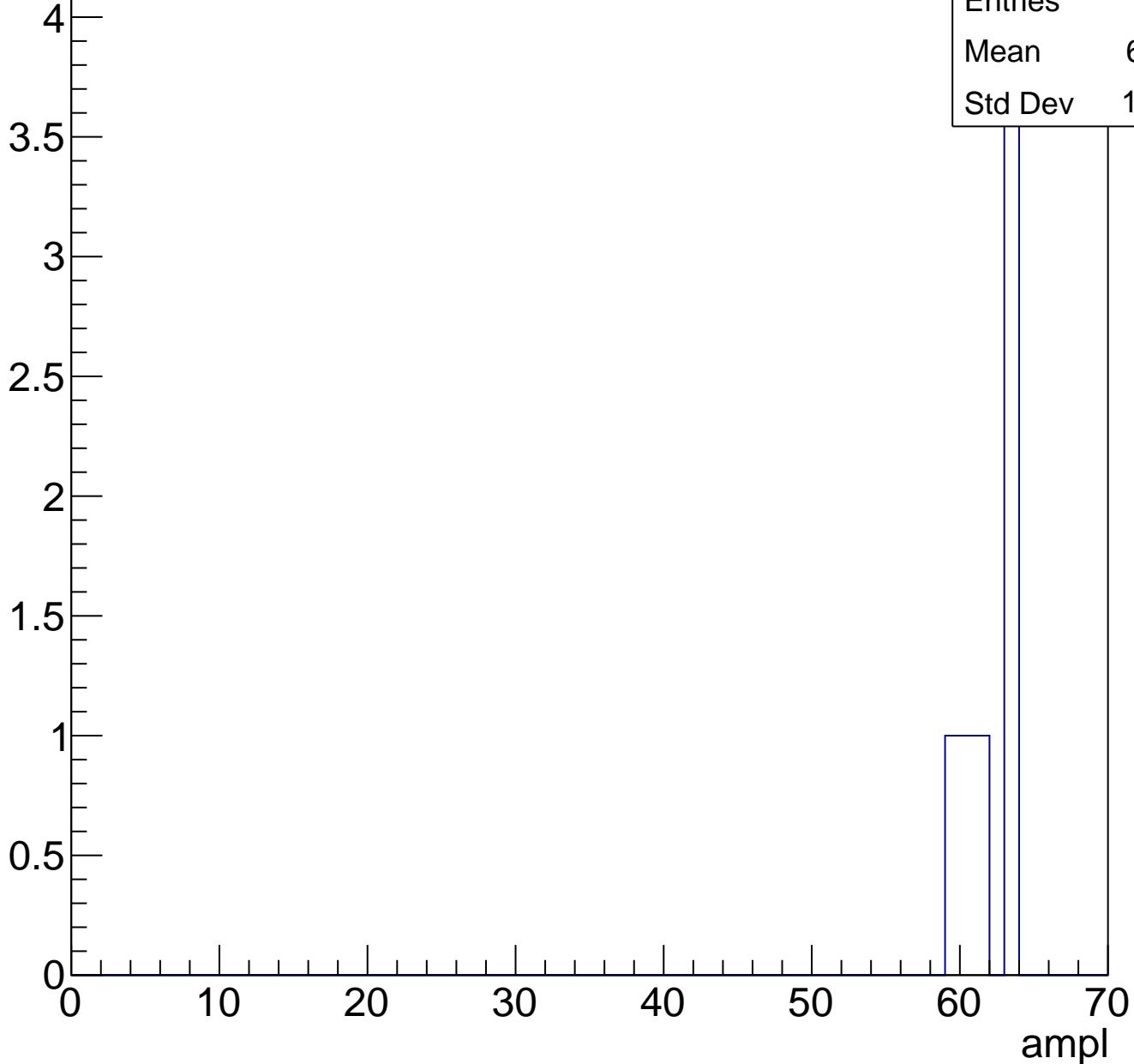
Entries	53
Mean	58.25
Std Dev	8.538



# B1L101S, U16-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch15, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	88
Mean	29.83
Std Dev	6.776

**Gaus mean : 30.2563**

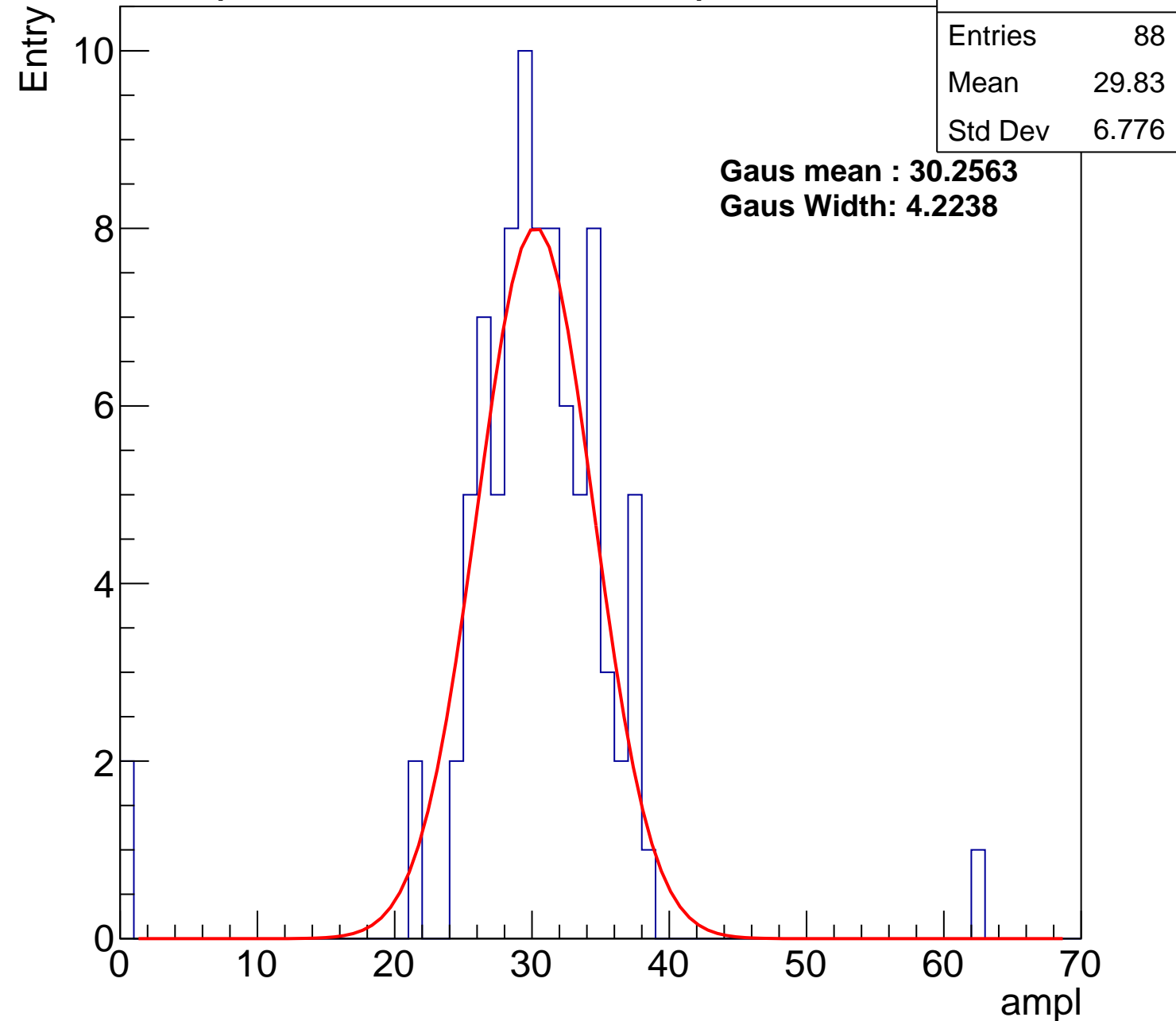
**Gaus Width: 4.2238**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



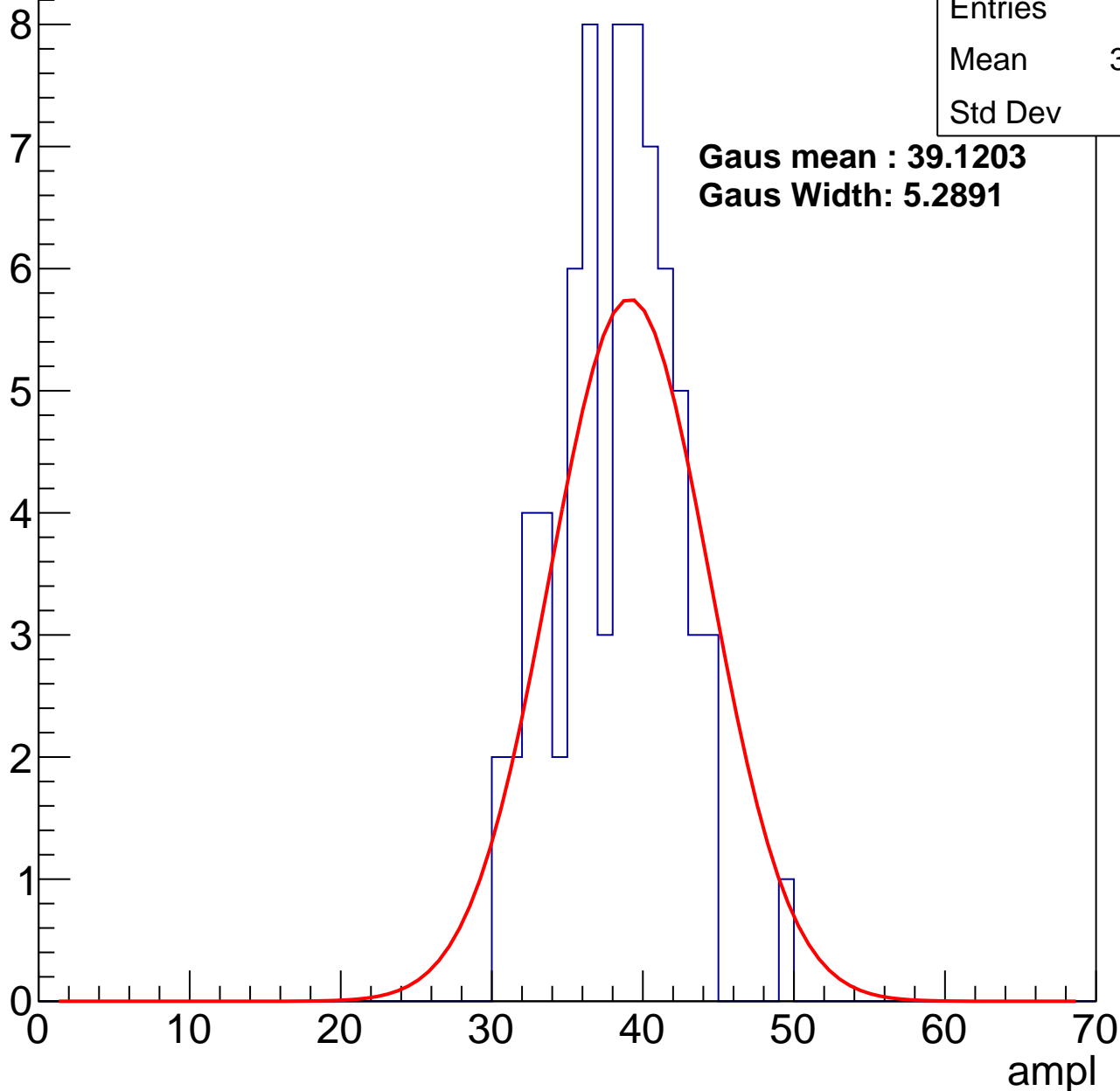
# B1L101S, U16-ch15, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	37.79
Std Dev	3.84

**Gaus mean : 39.1203**  
**Gaus Width: 5.2891**



# B1L101S, U16-ch15, adc2

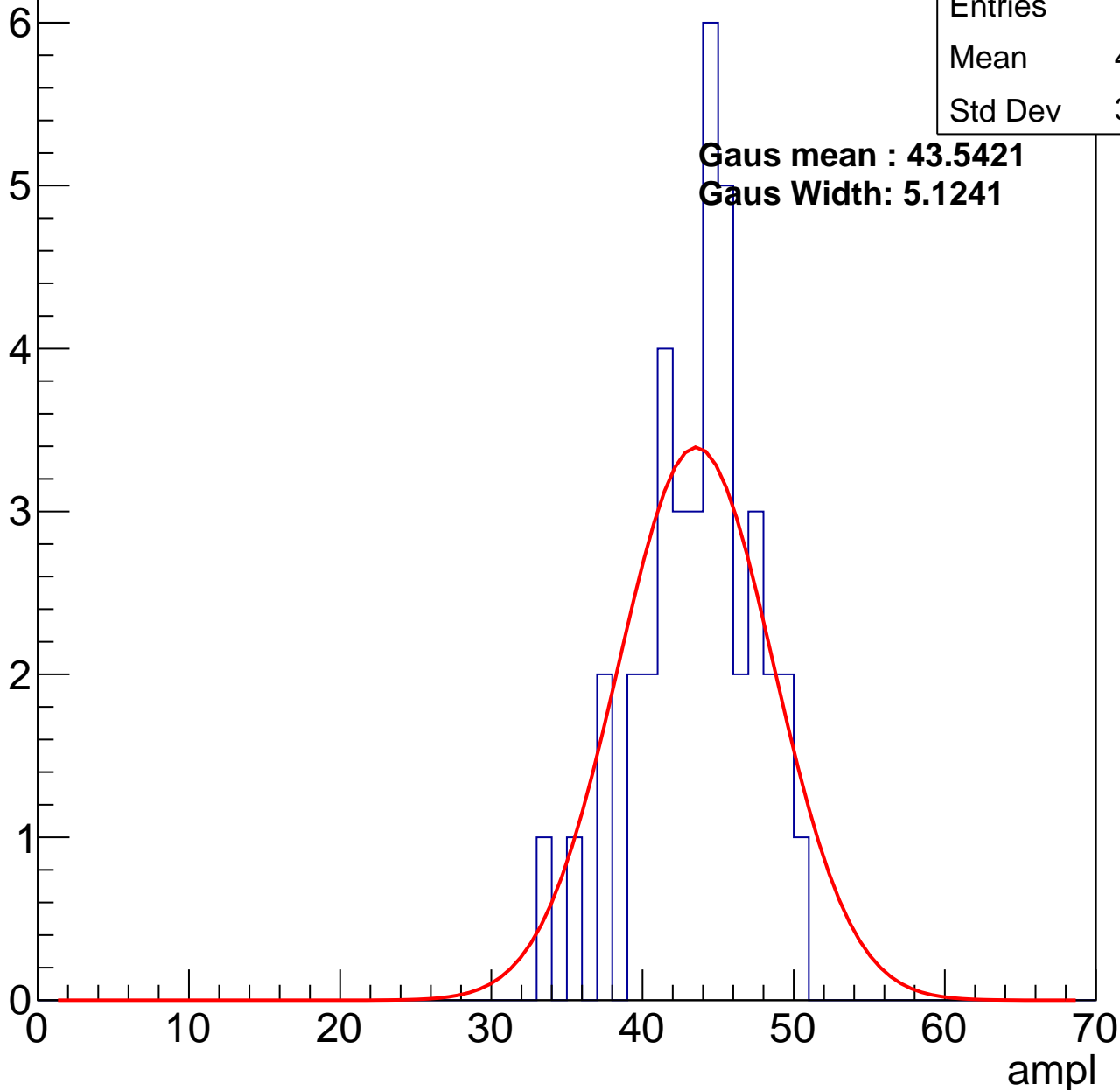
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	39
Mean	43.21
Std Dev	3.811

**Gaus mean : 43.5421**

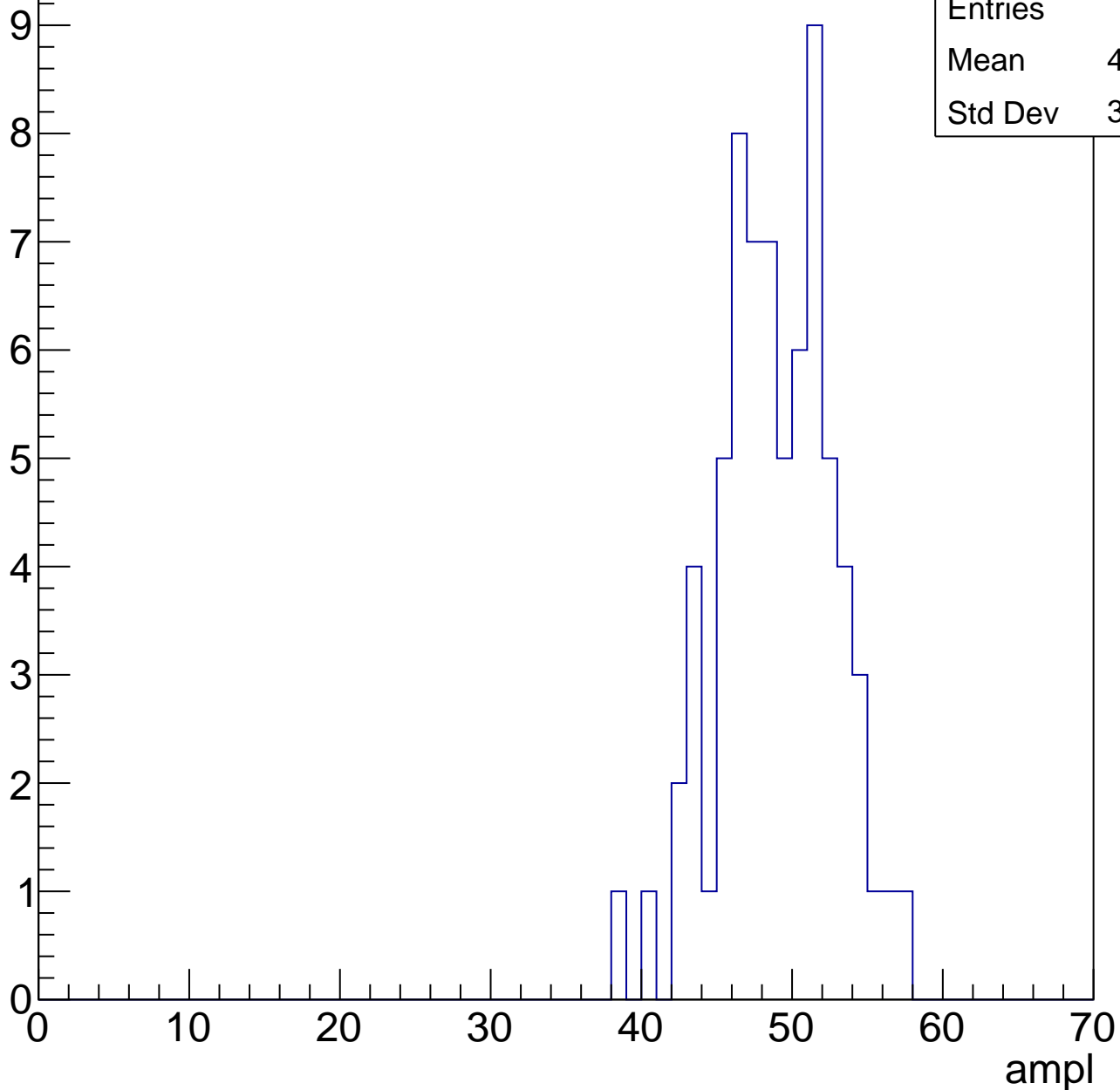
**Gaus Width: 5.1241**



# B1L101S, U16-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

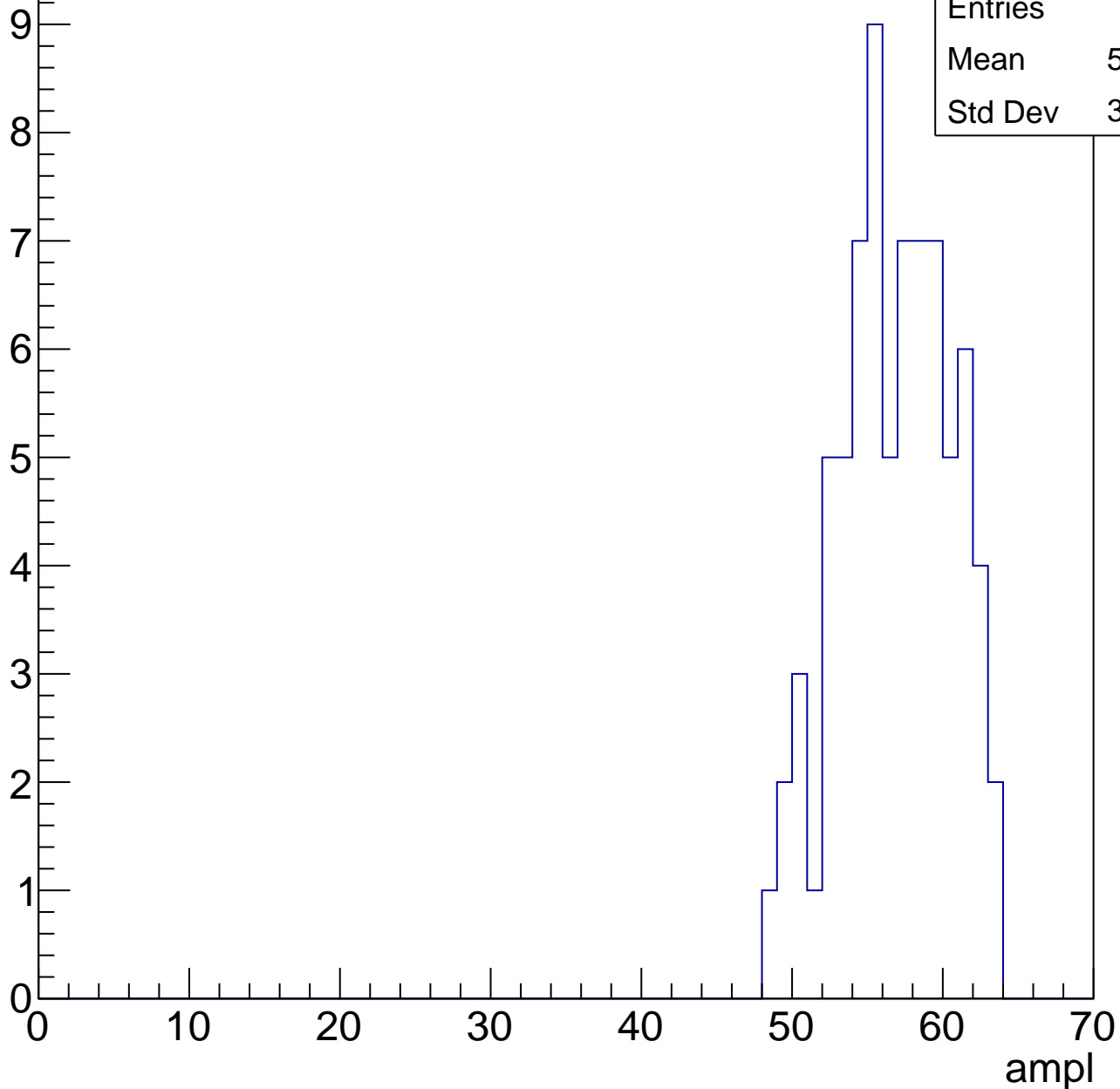
Entry



# B1L101S, U16-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



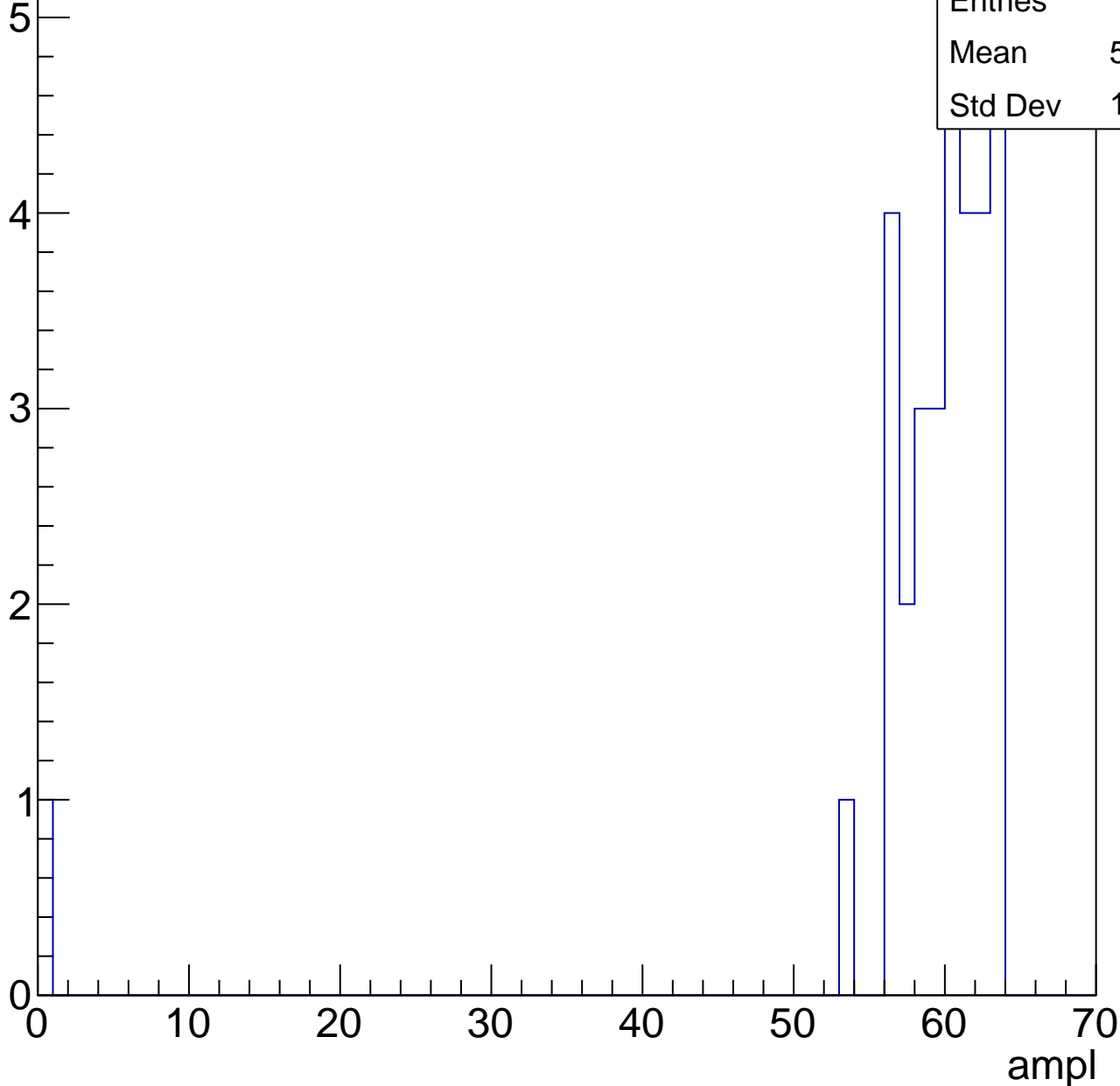
Entries	76
Mean	56.36
Std Dev	3.659

# B1L101S, U16-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	32
Mean	57.78
Std Dev	10.69



# B1L101S, U16-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U16-ch16, adc0

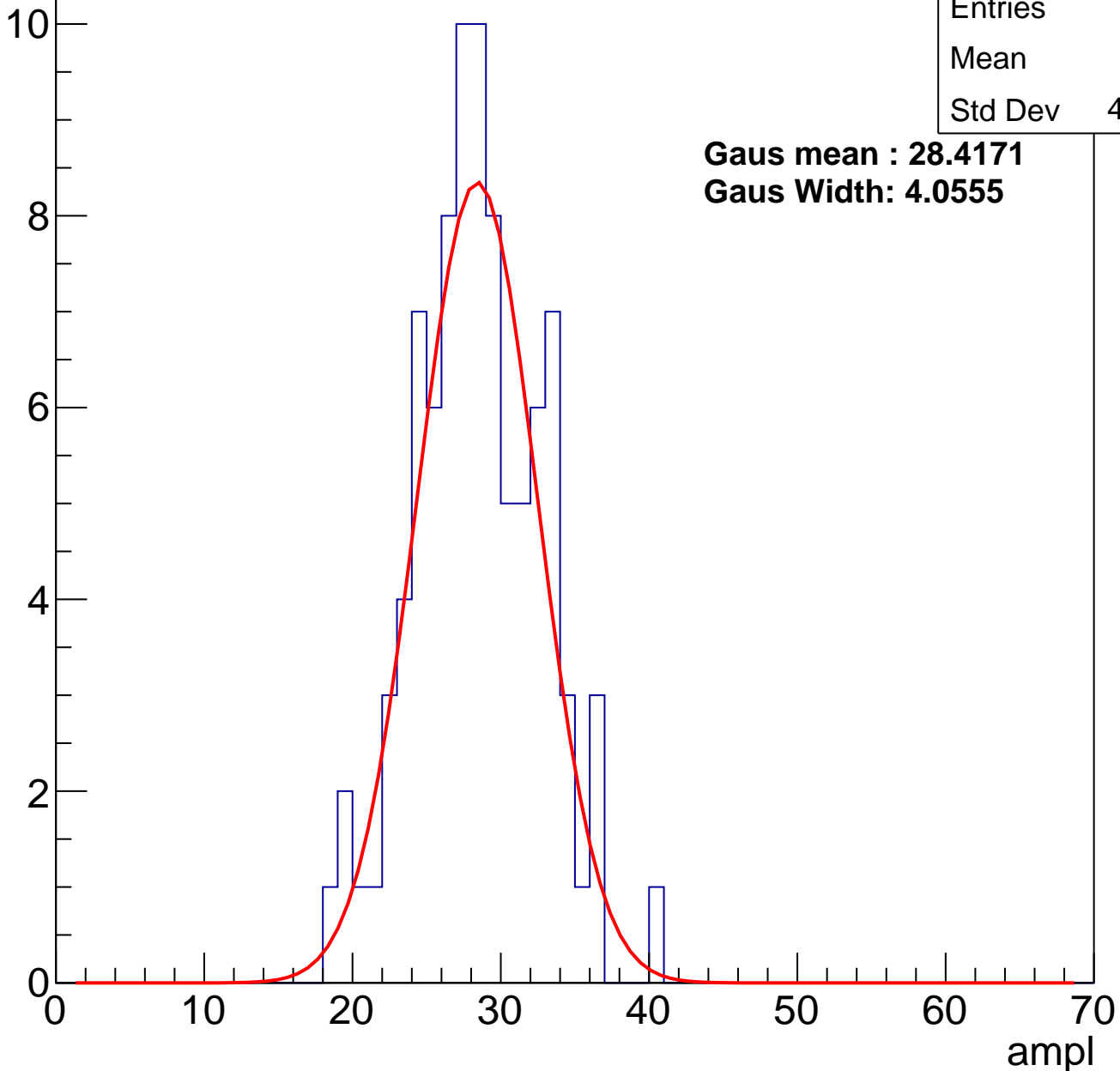
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	92
Mean	28
Std Dev	4.207

**Gaus mean : 28.4171**

**Gaus Width: 4.0555**

Entry



# B1L101S, U16-ch16, adc1

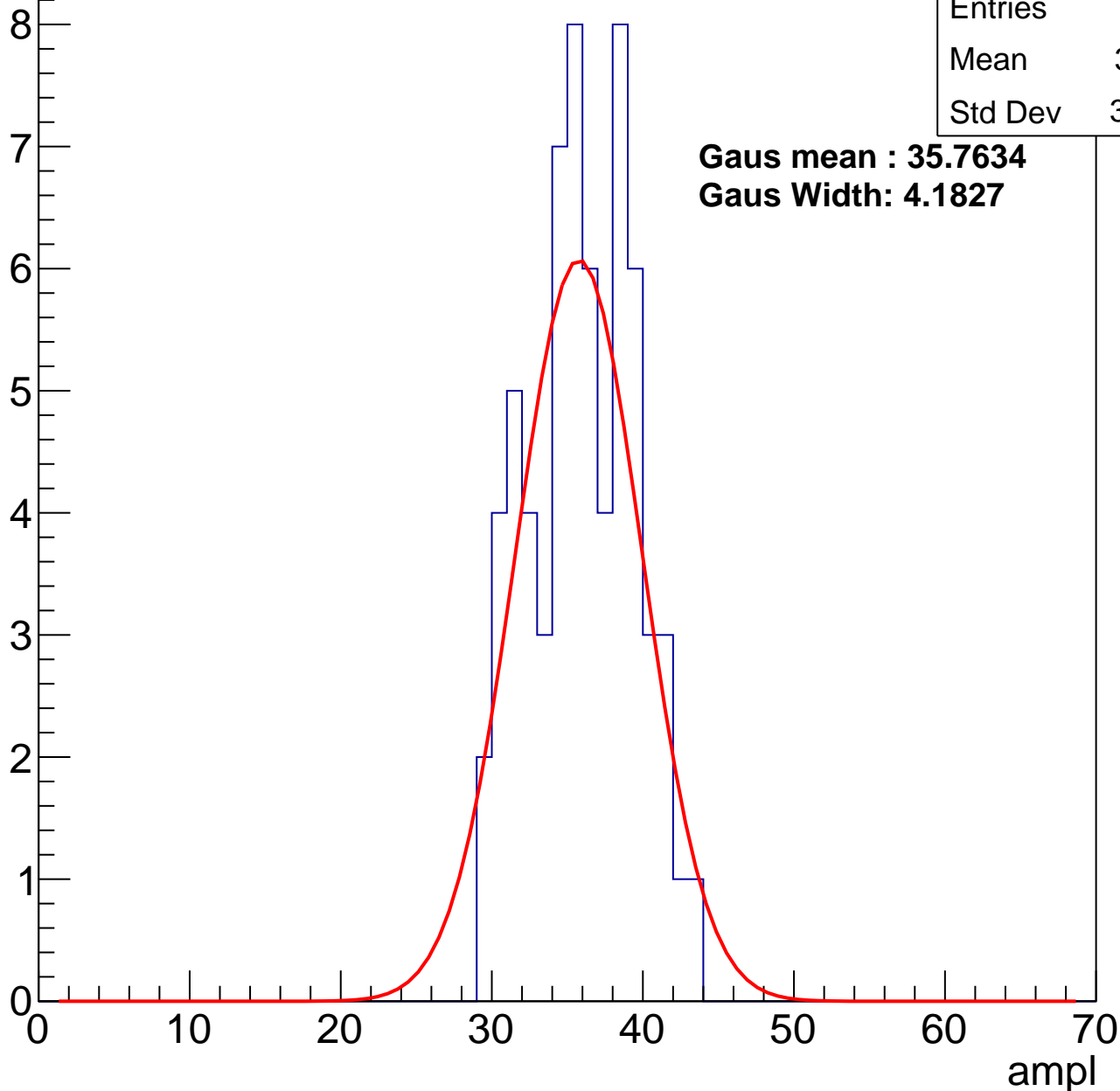
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	35.51
Std Dev	3.456

**Gaus mean : 35.7634**

**Gaus Width: 4.1827**



# B1L101S, U16-ch16, adc2

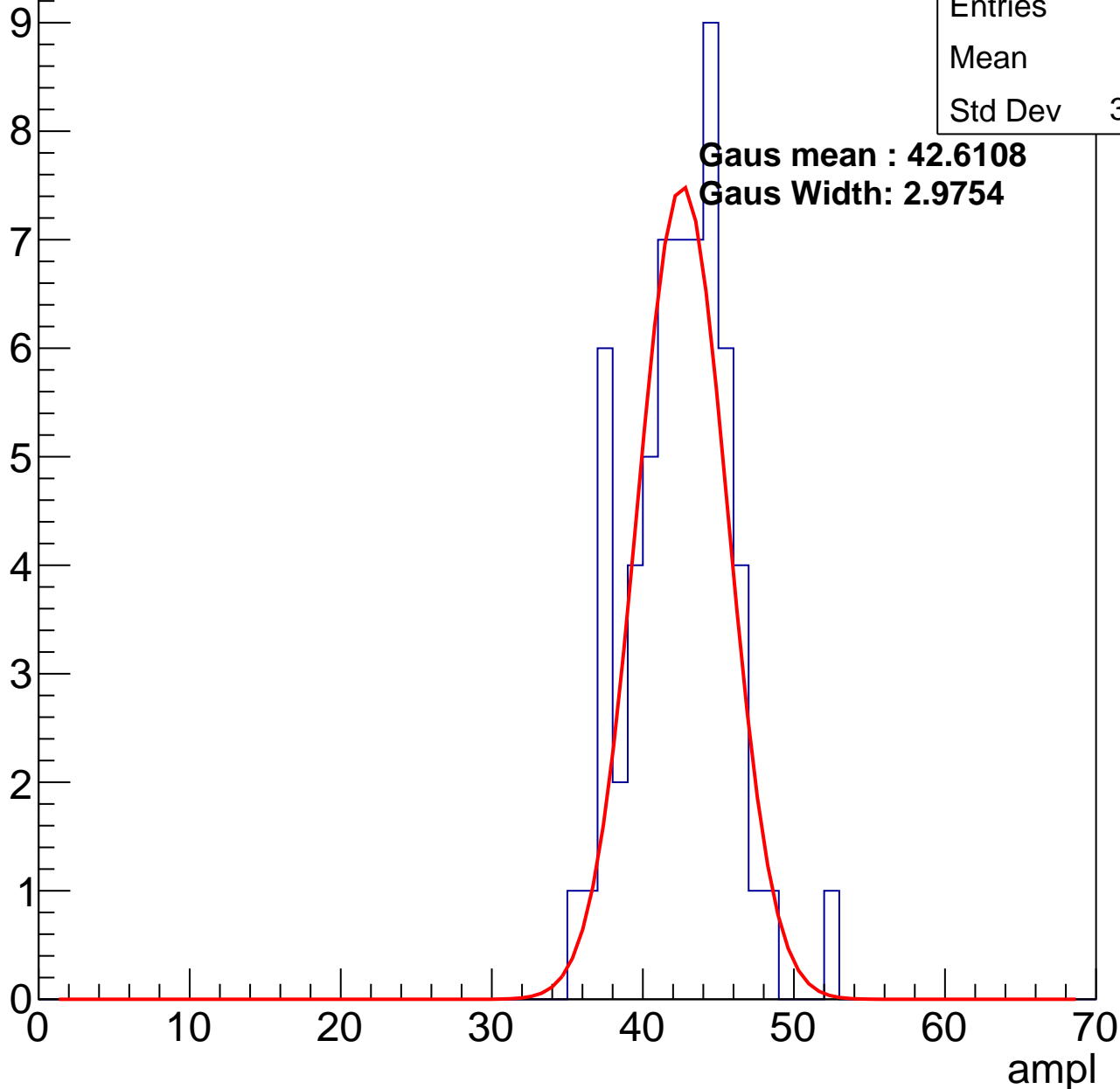
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	42
Std Dev	3.243

**Gaus mean : 42.6108**

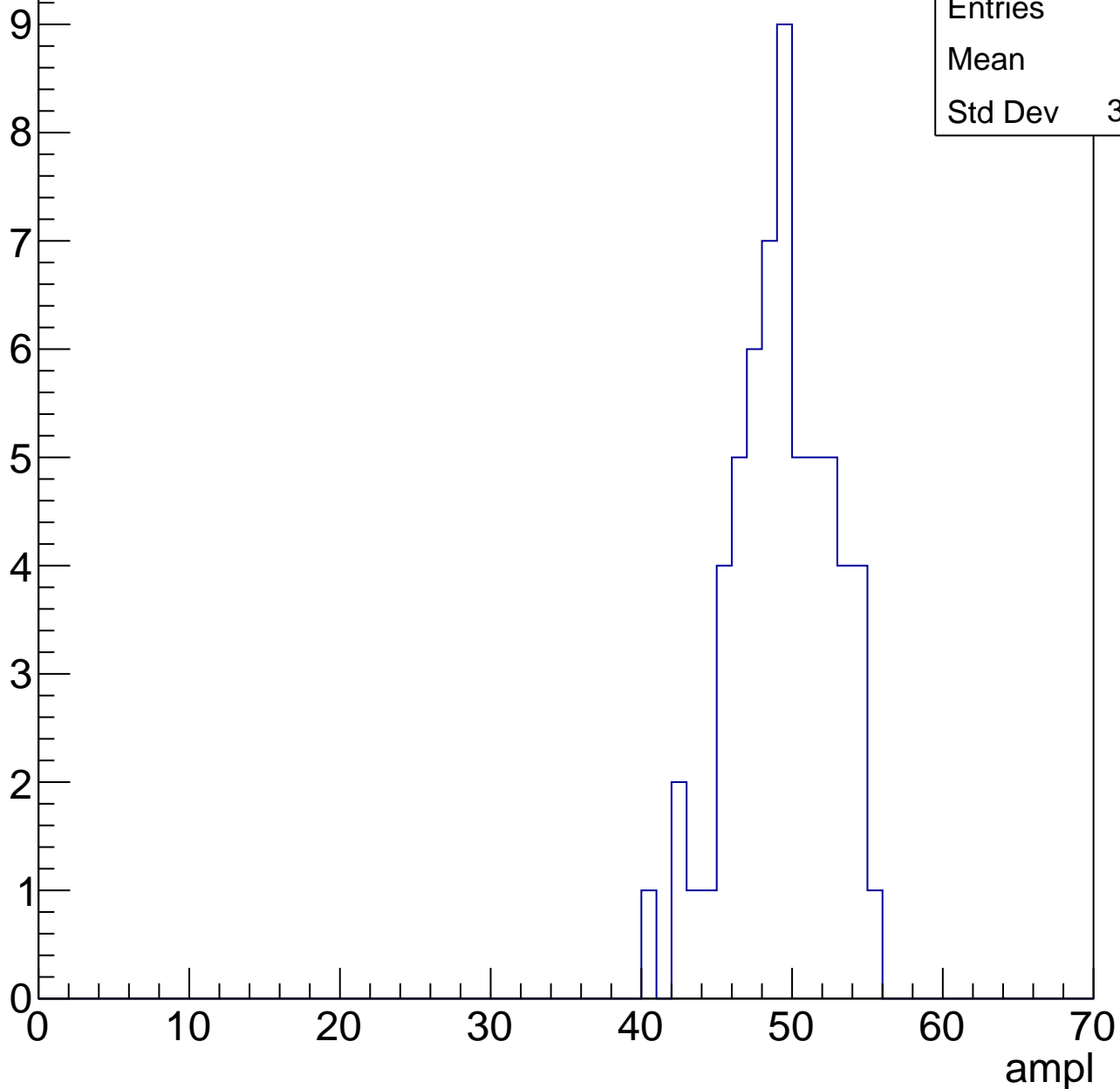
**Gaus Width: 2.9754**



# B1L101S, U16-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



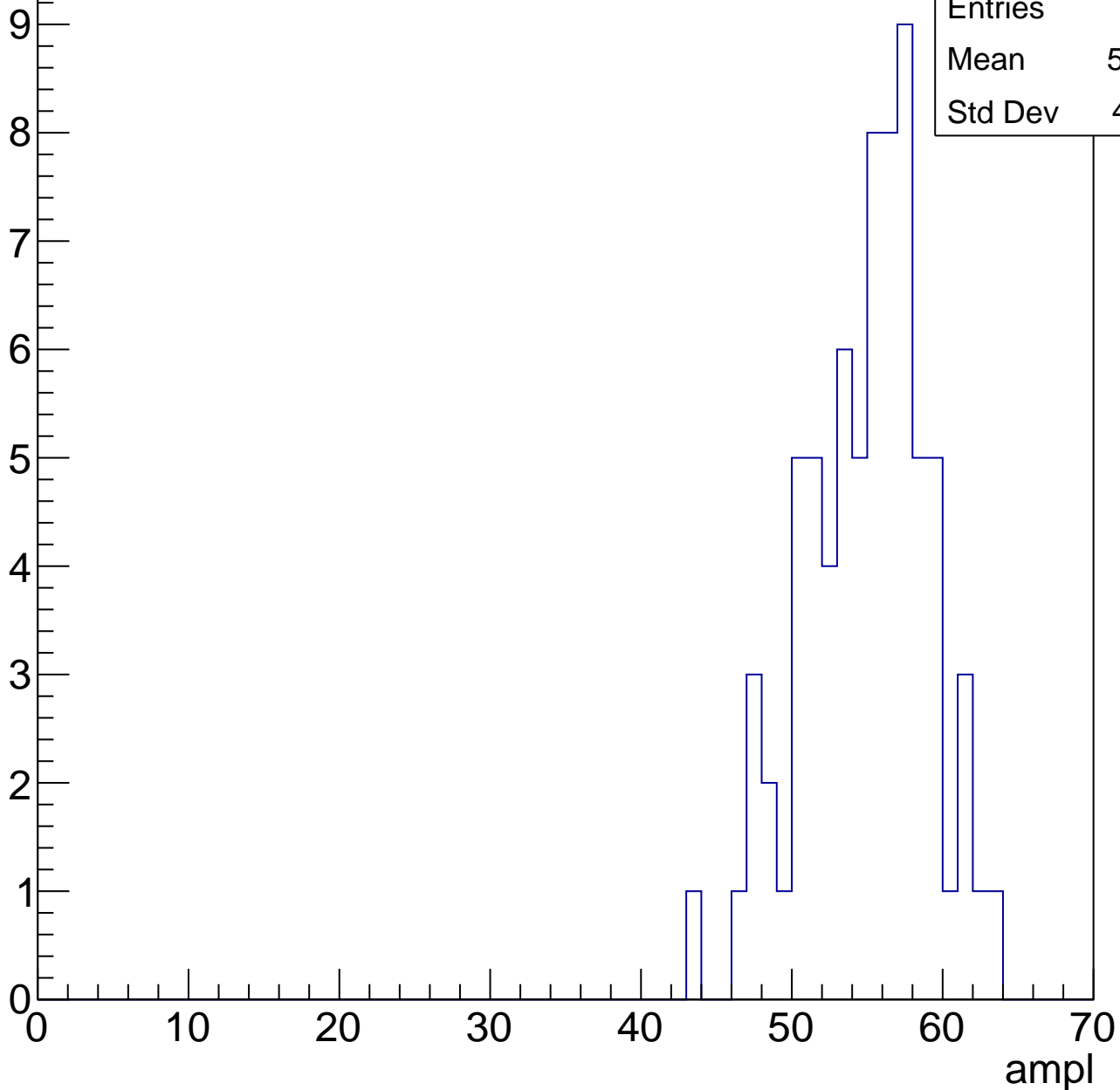
Entries	60
Mean	48.8
Std Dev	3.285

# B1L101S, U16-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	54.46
Std Dev	4.051

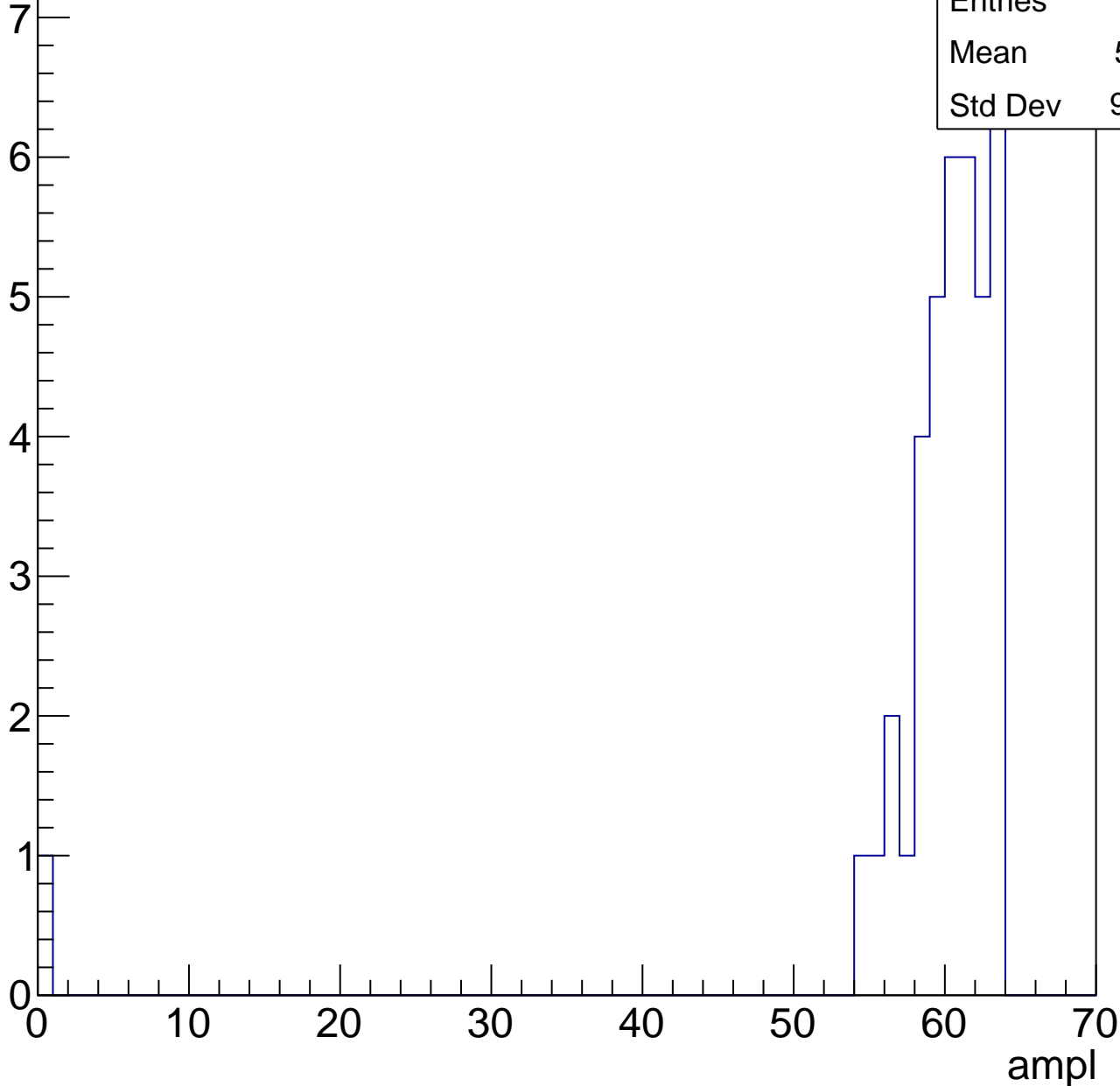


# B1L101S, U16-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

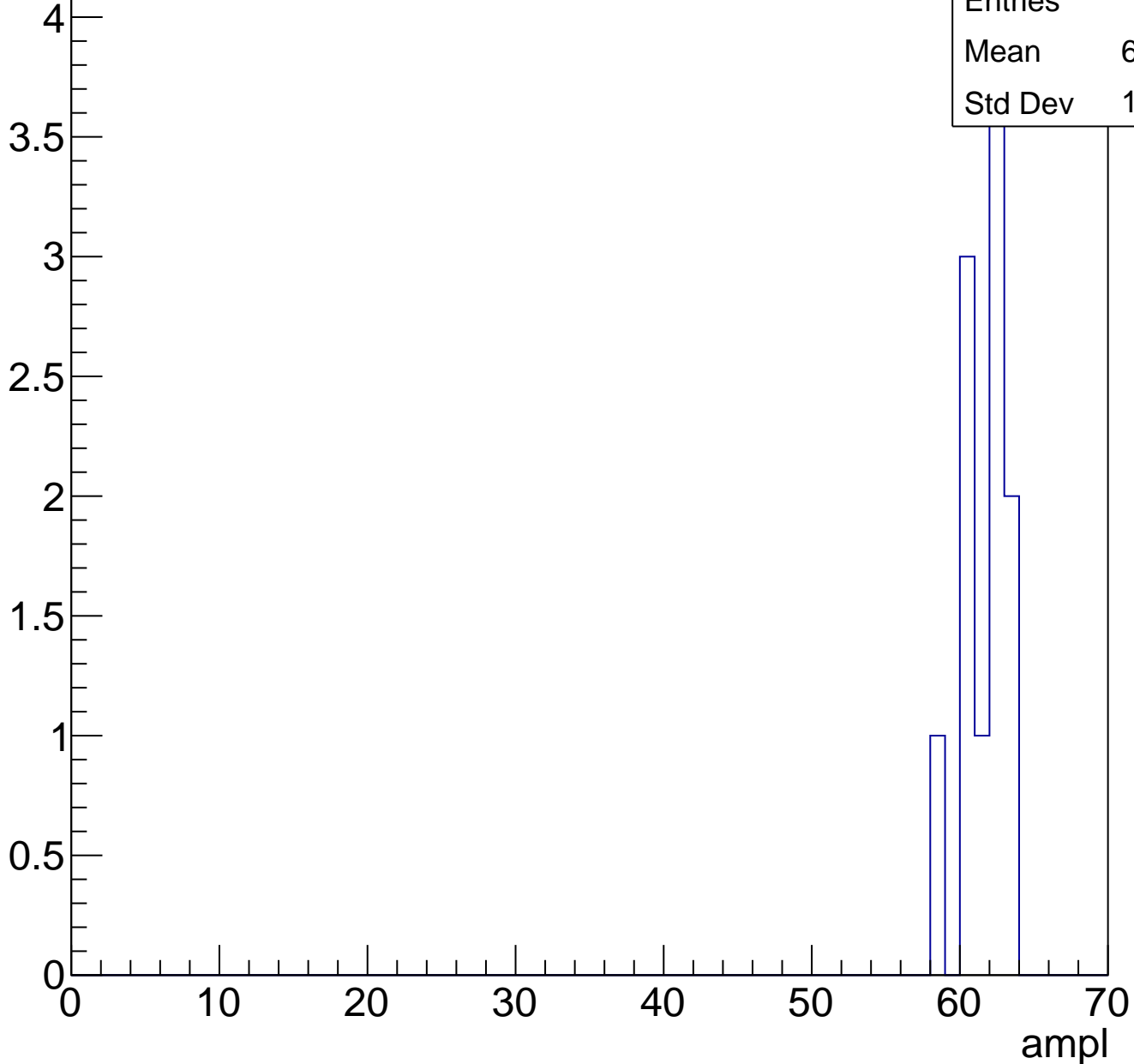
Entries	39
Mean	58.51
Std Dev	9.774



# B1L101S, U16-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch17, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	76
Mean	31.33
Std Dev	3.469

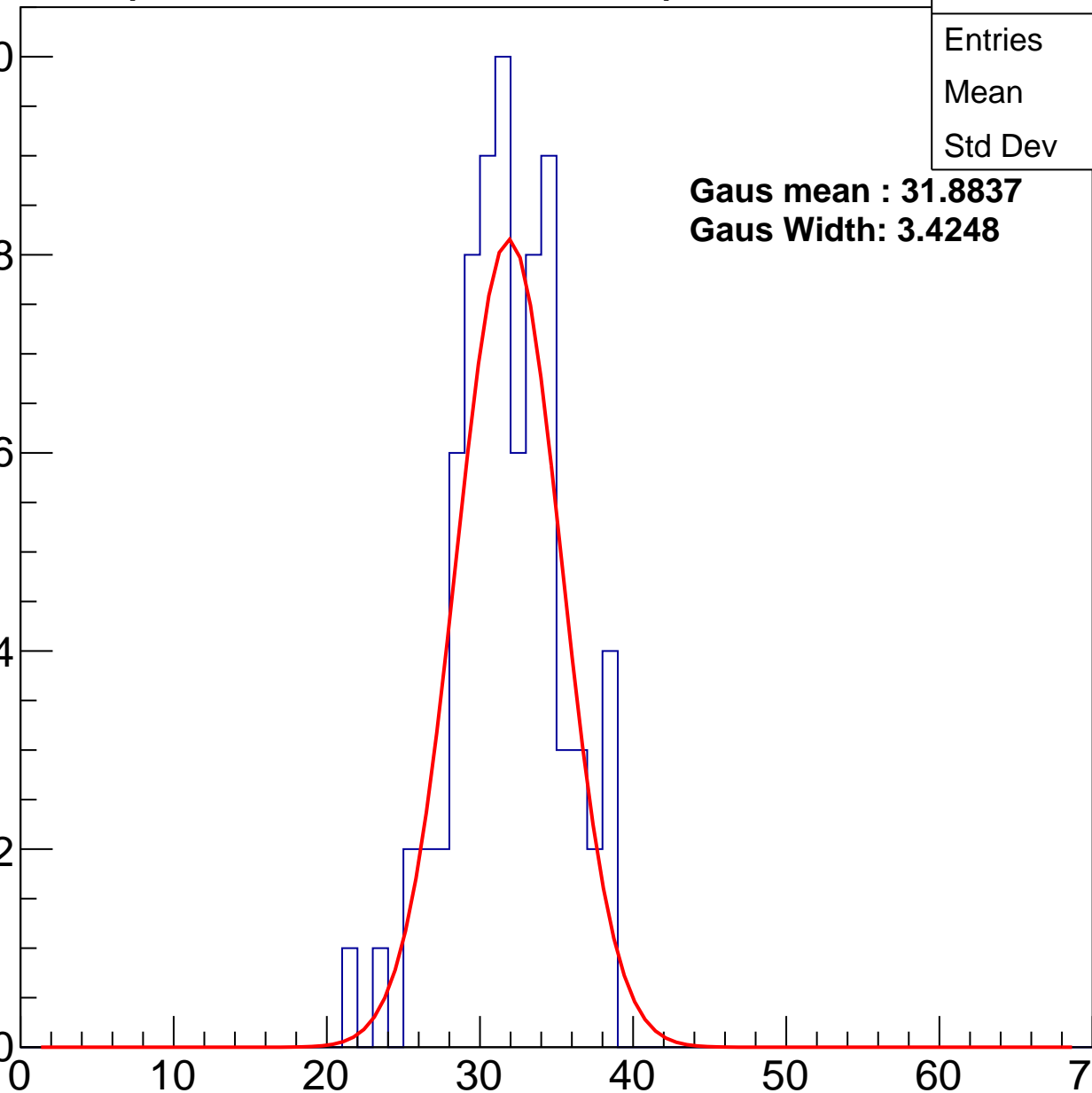
**Gaus mean : 31.8837**

**Gaus Width: 3.4248**

Entry

10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch17, adc1

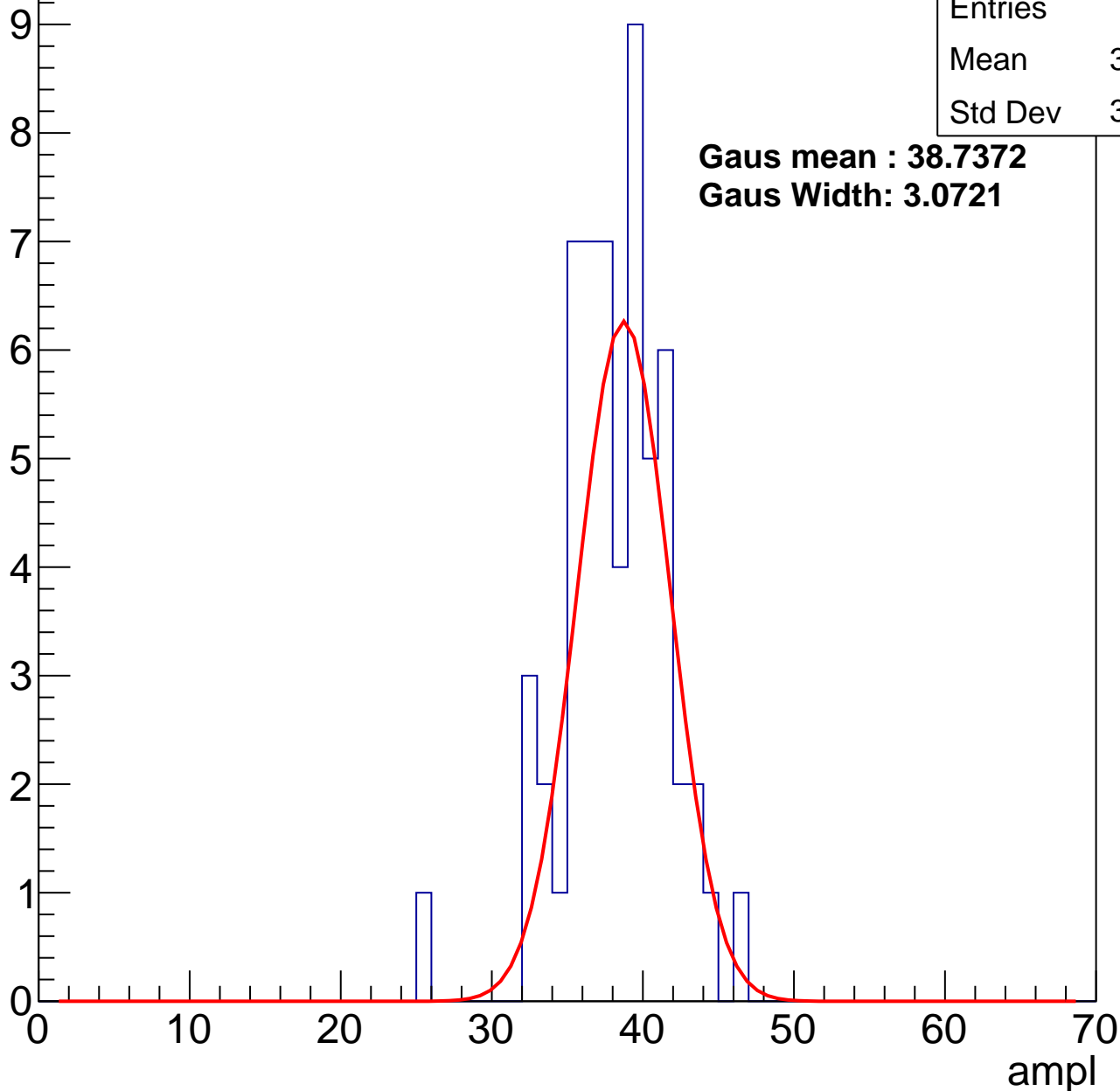
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	37.69
Std Dev	3.475

**Gaus mean : 38.7372**

**Gaus Width: 3.0721**



# B1L101S, U16-ch17, adc2

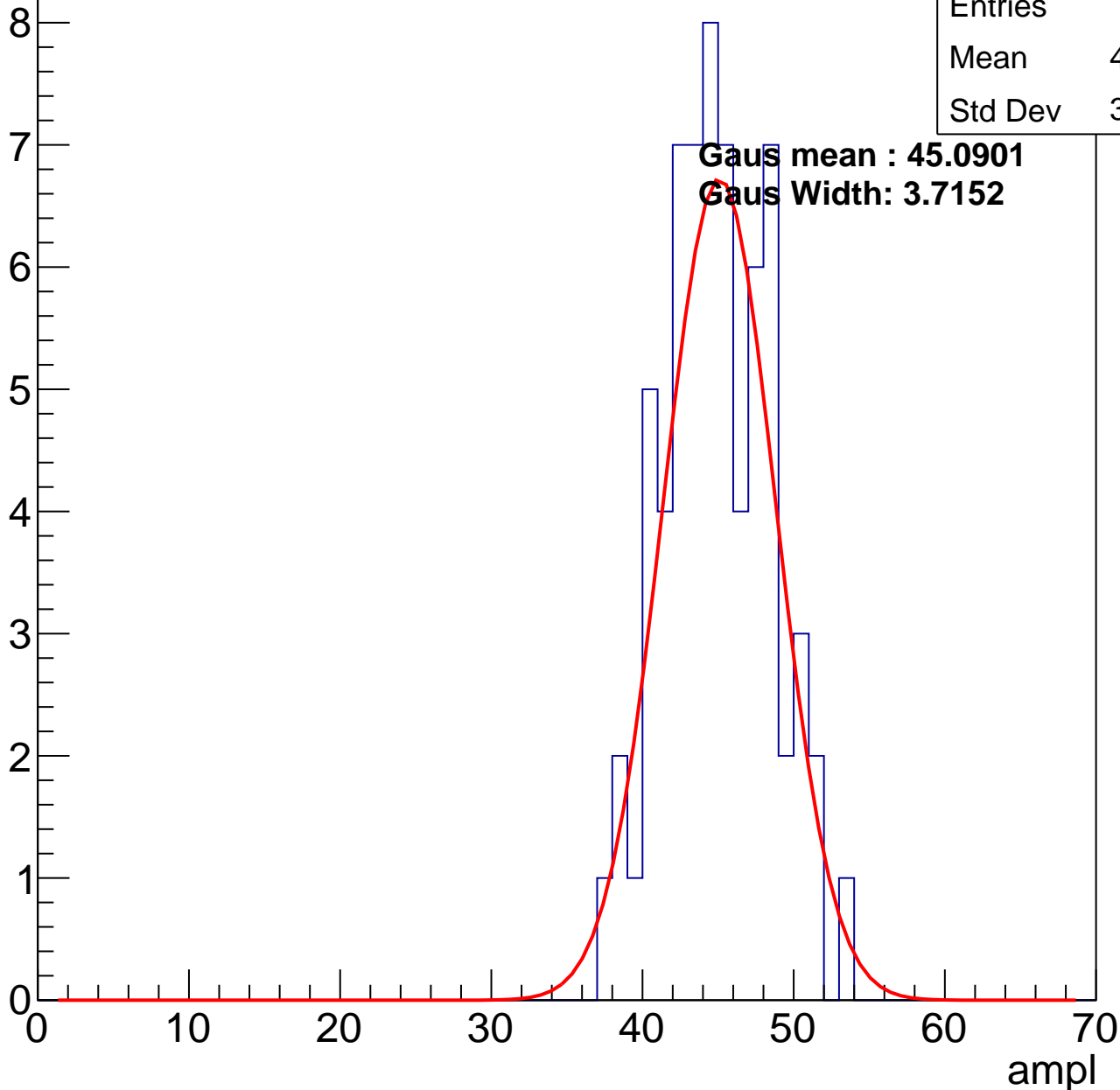
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	44.52
Std Dev	3.466

Gaus mean : 45.0901

Gaus Width: 3.7152

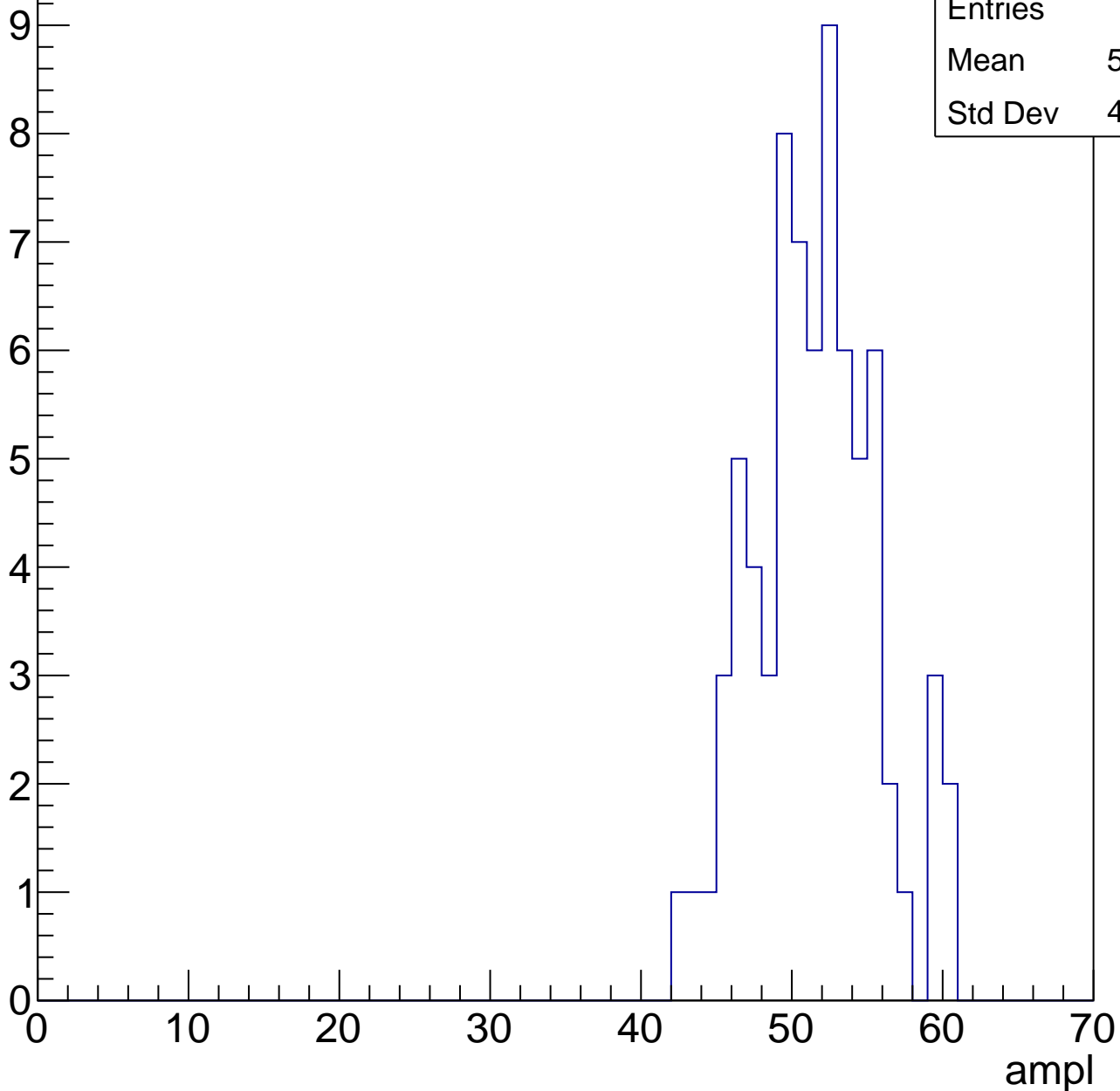


# B1L101S, U16-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	51.04
Std Dev	4.005

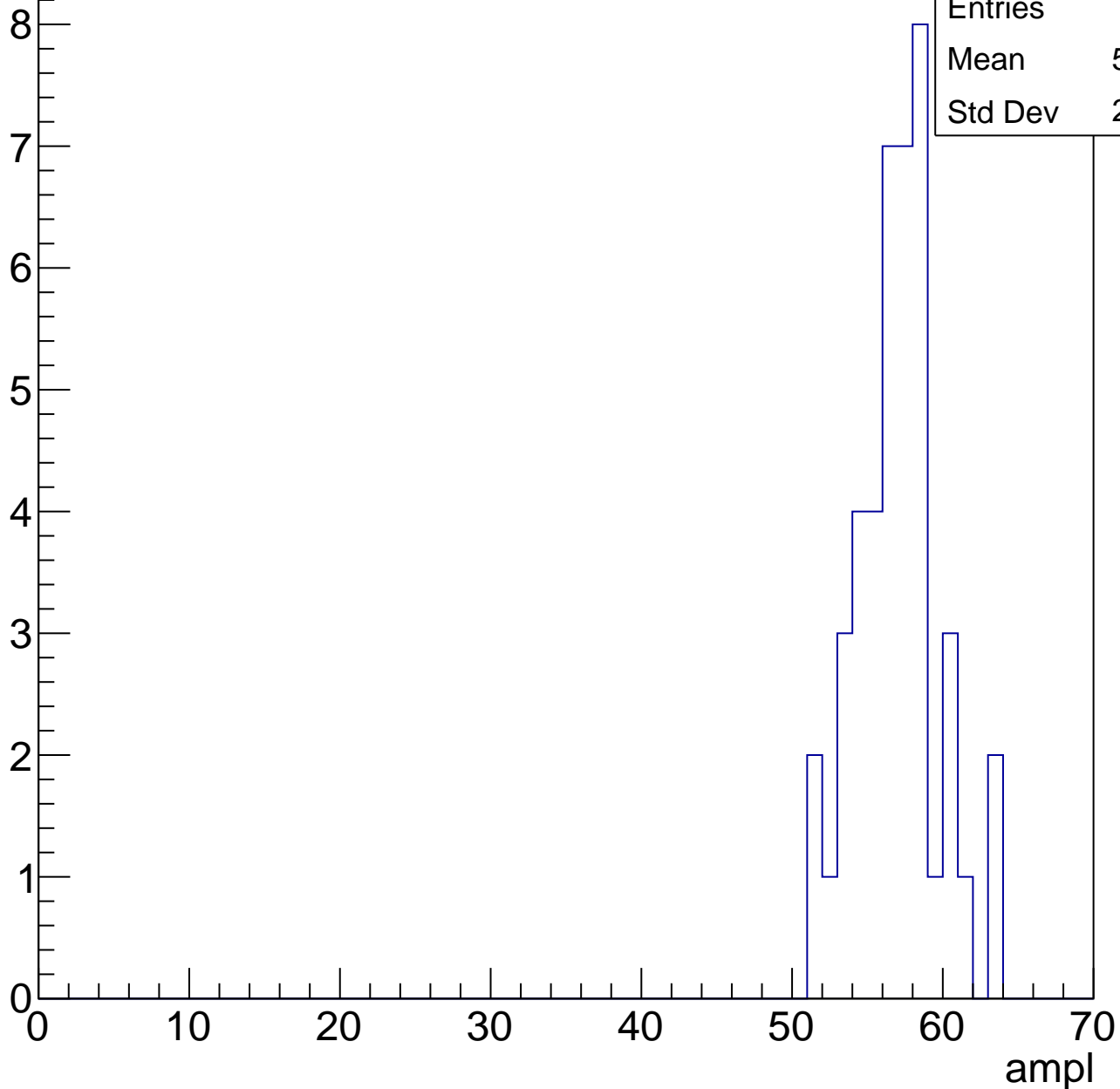


# B1L101S, U16-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	56.51
Std Dev	2.731

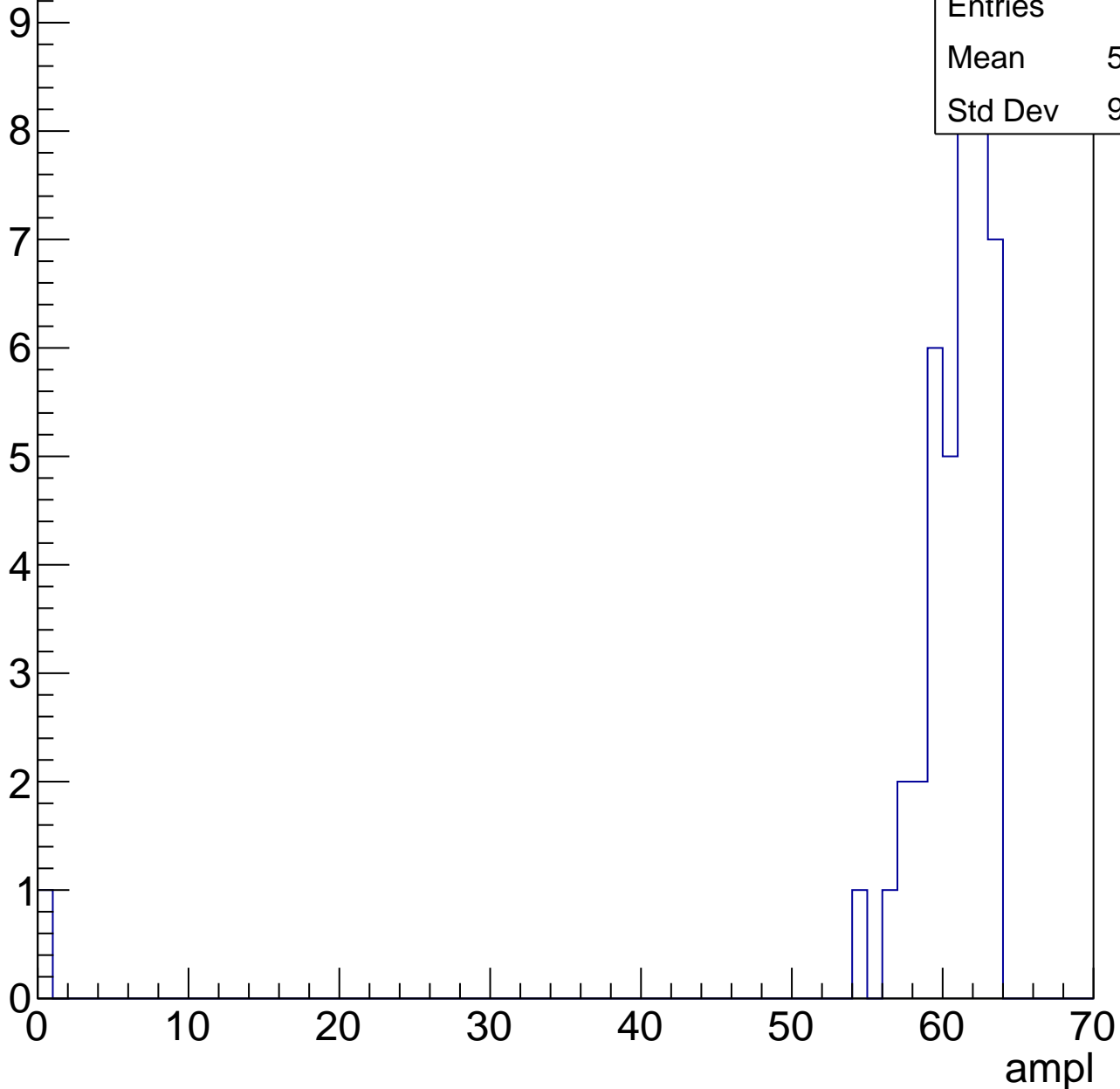


# B1L101S, U16-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	59.12
Std Dev	9.349



# B1L101S, U16-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch18, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	61
Mean	27.59
Std Dev	7.097

**Gaus mean : 29.6181**

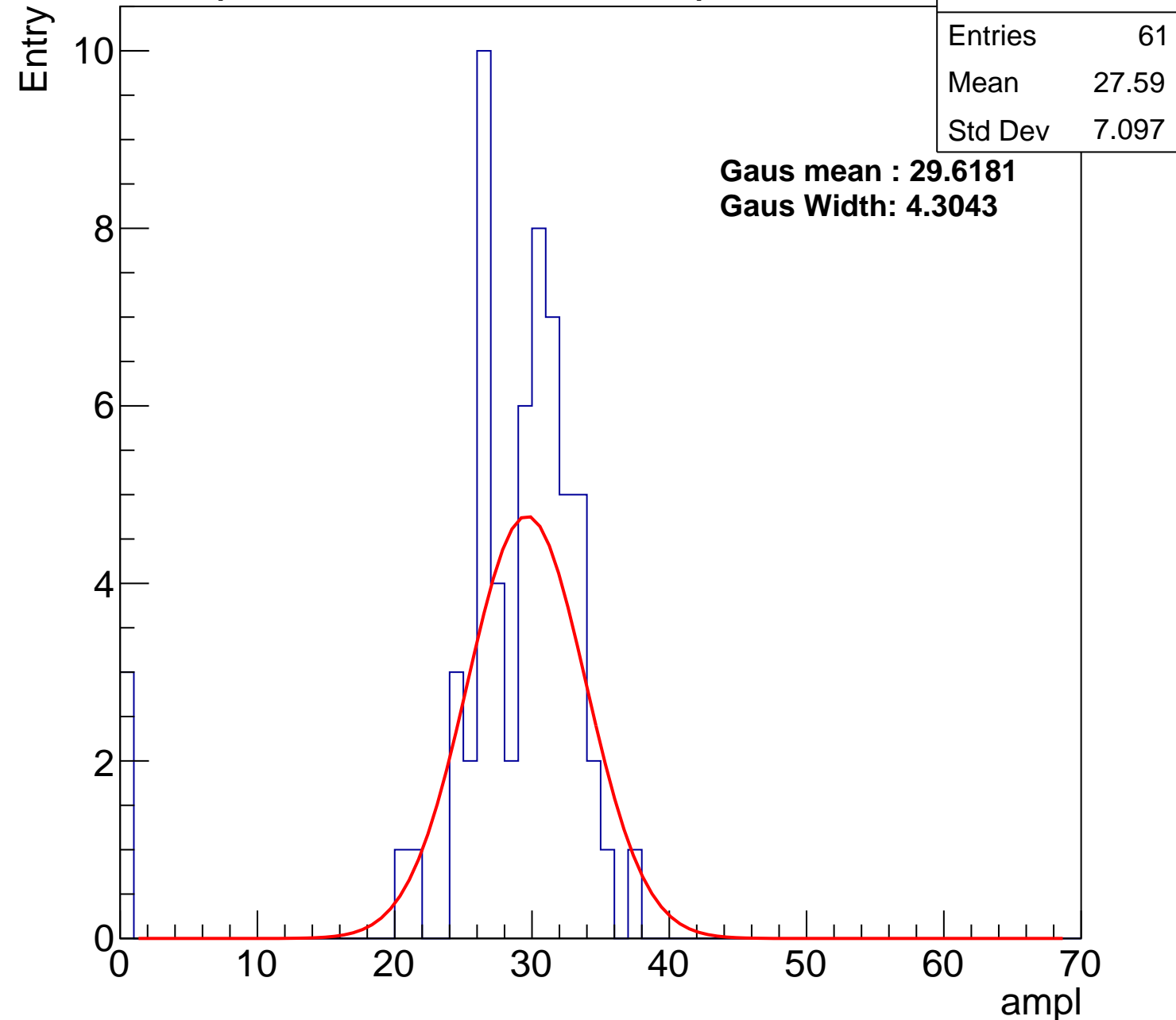
**Gaus Width: 4.3043**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch18, adc1

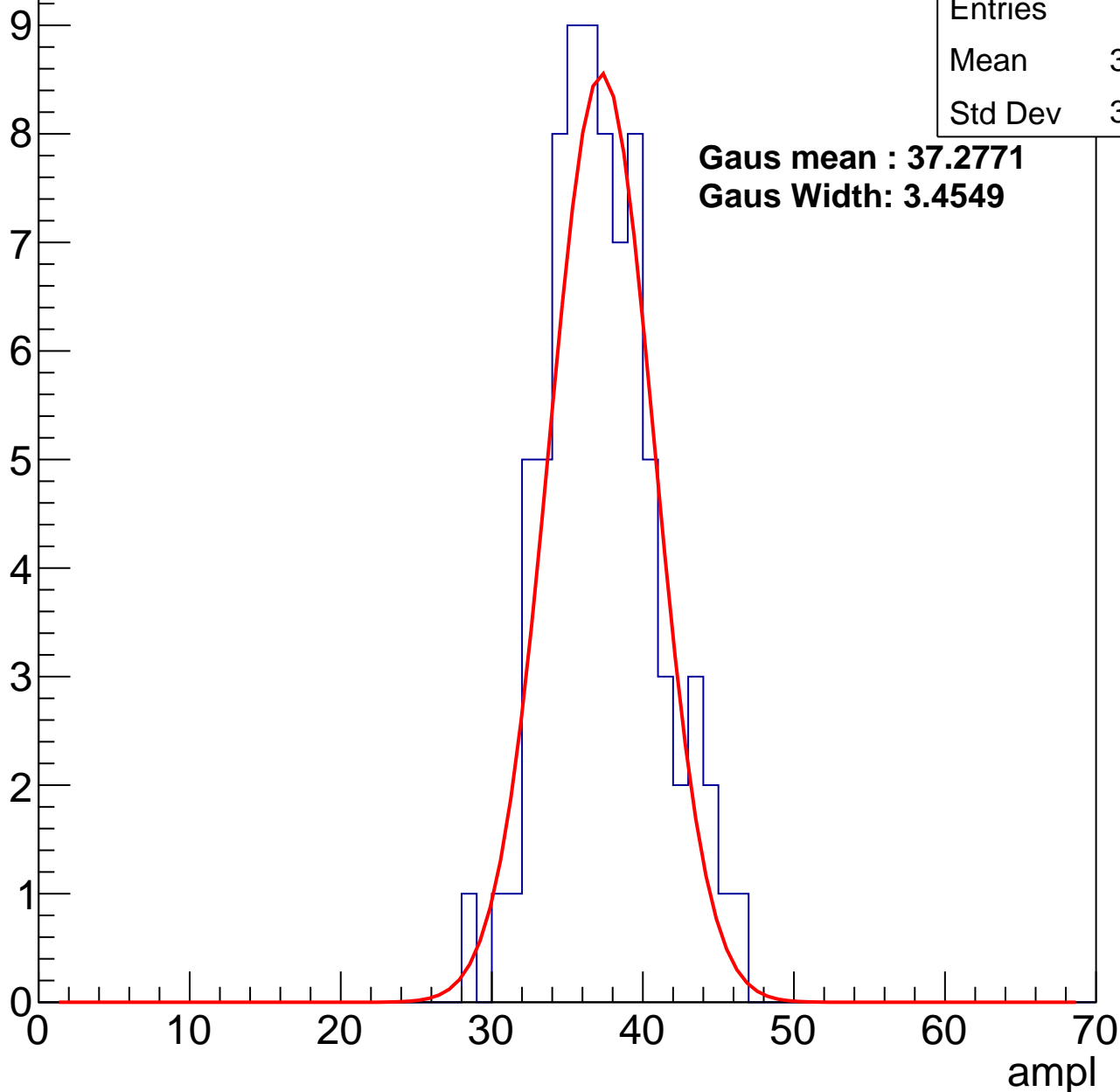
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	36.89
Std Dev	3.593

**Gaus mean : 37.2771**

**Gaus Width: 3.4549**



# B1L101S, U16-ch18, adc2

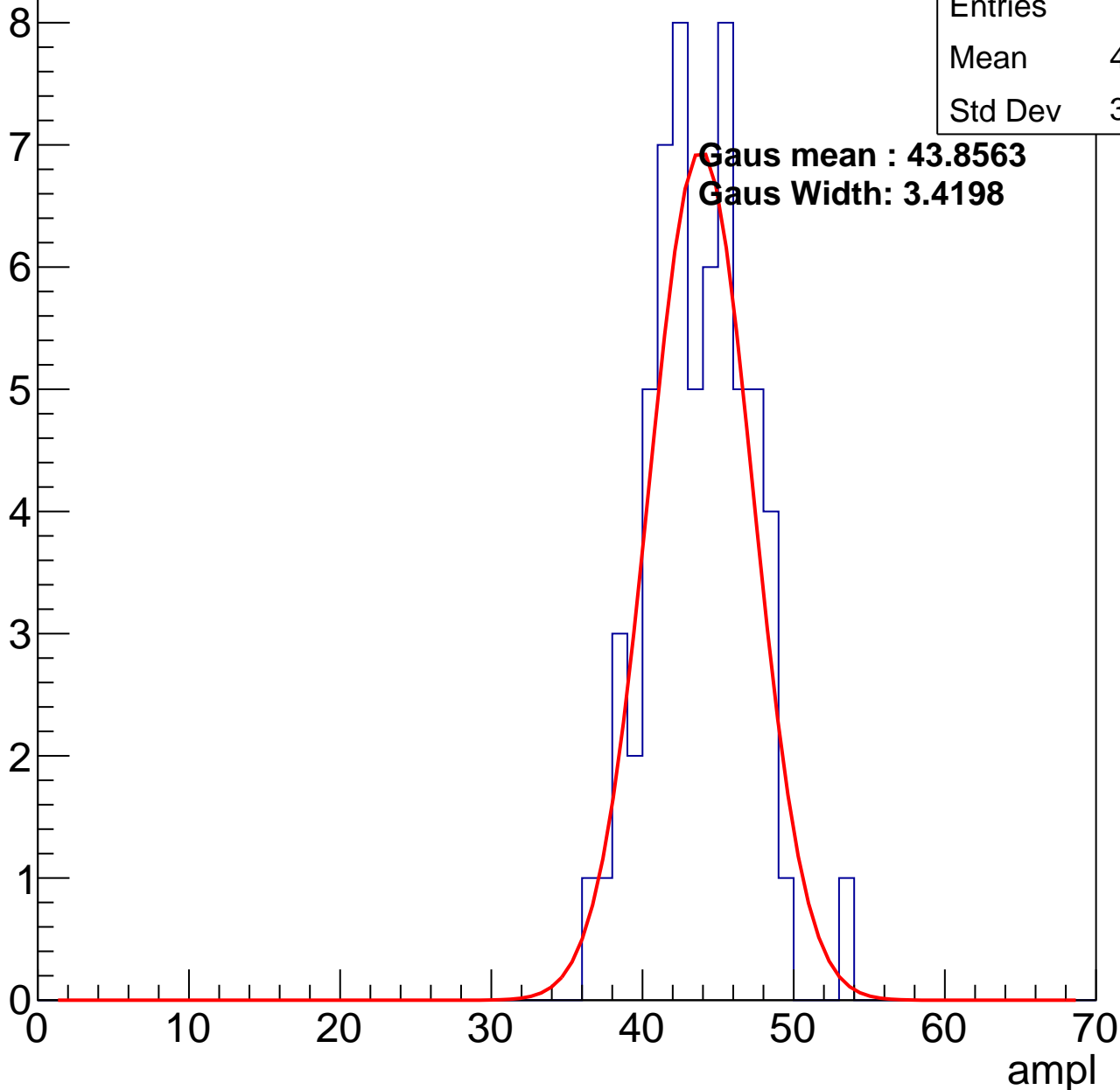
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	43.32
Std Dev	3.276

**Gaus mean : 43.8563**

**Gaus Width: 3.4198**

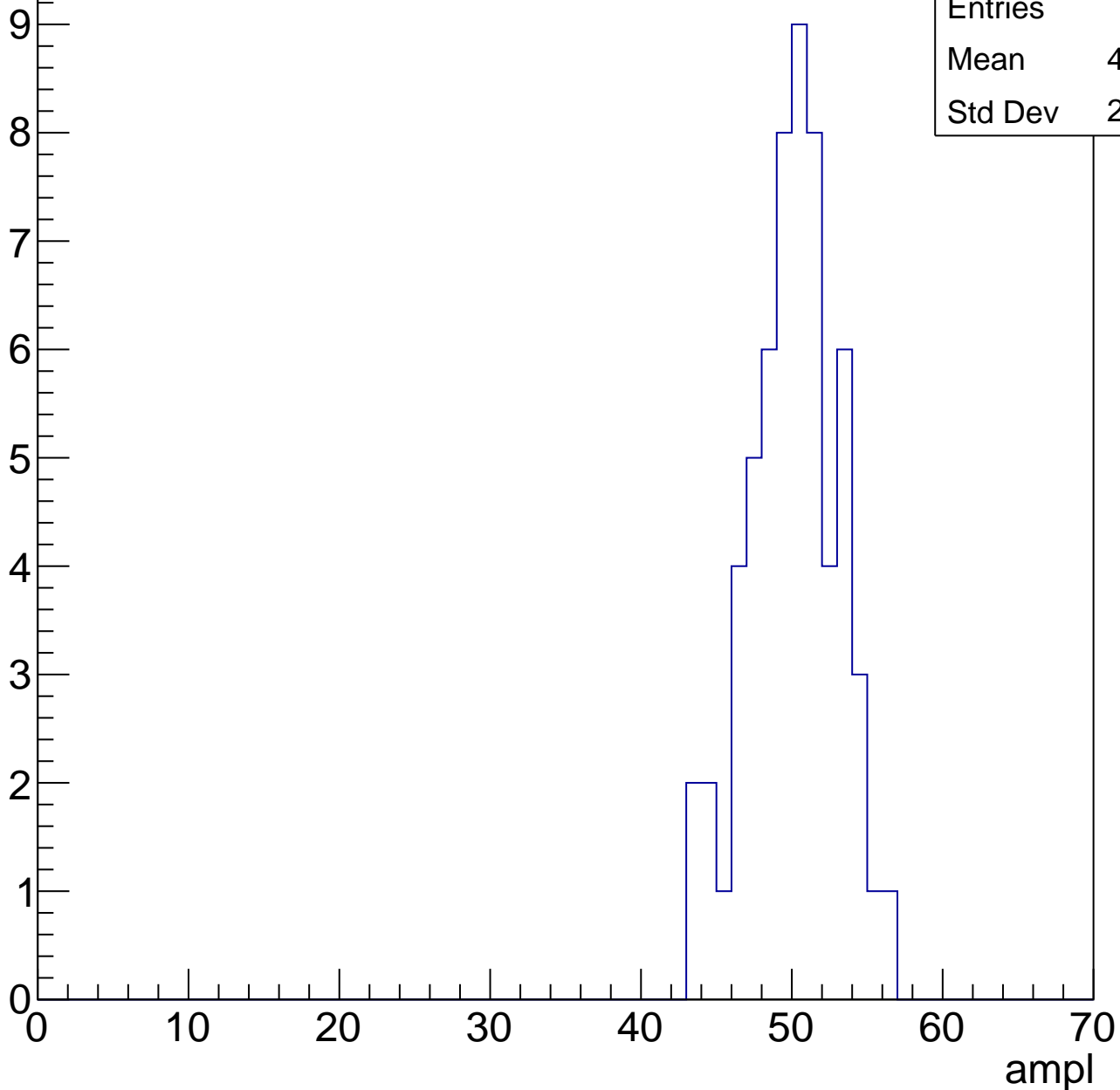


# B1L101S, U16-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	49.58
Std Dev	2.923

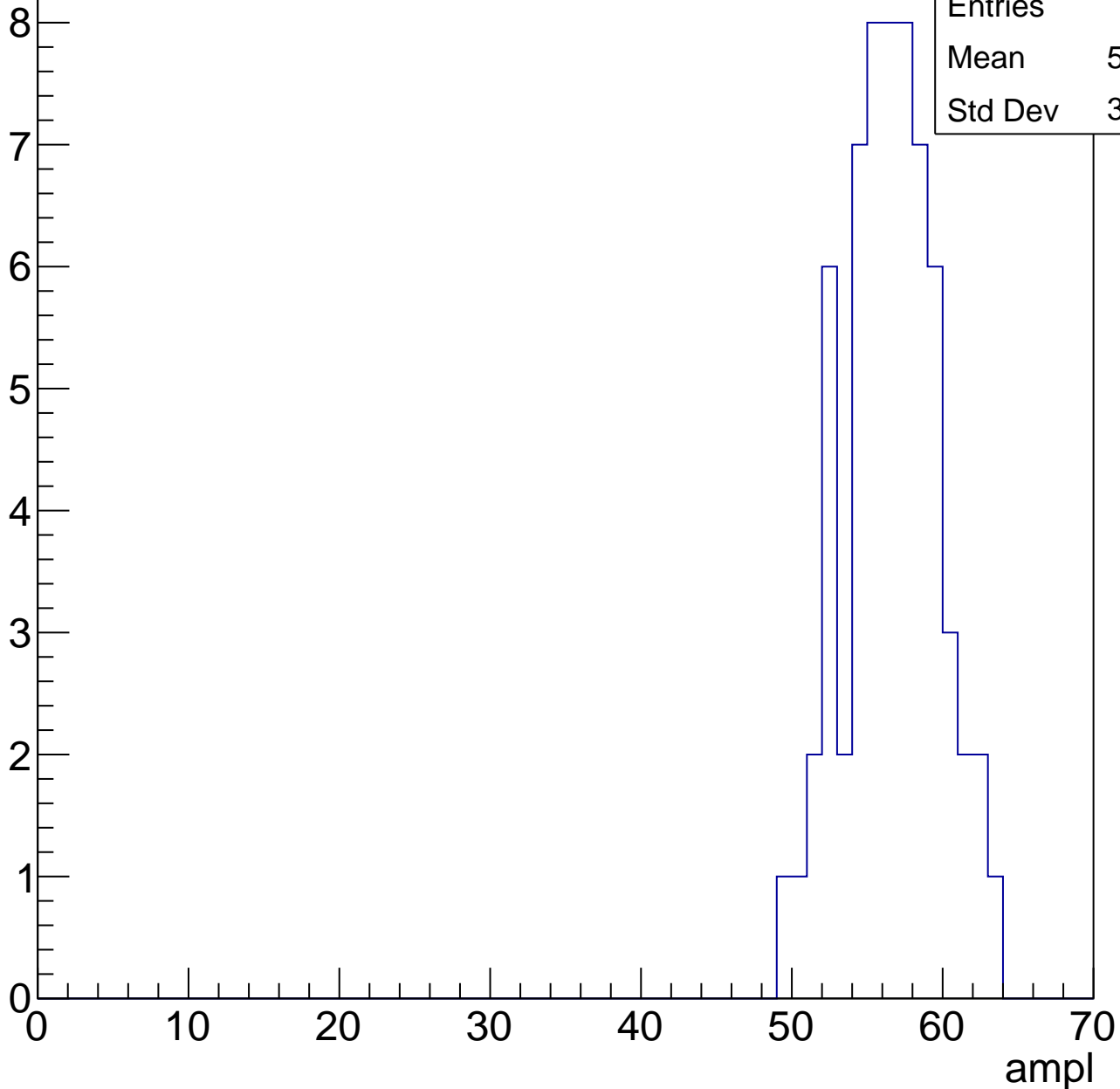


# B1L101S, U16-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	56.09
Std Dev	3.045

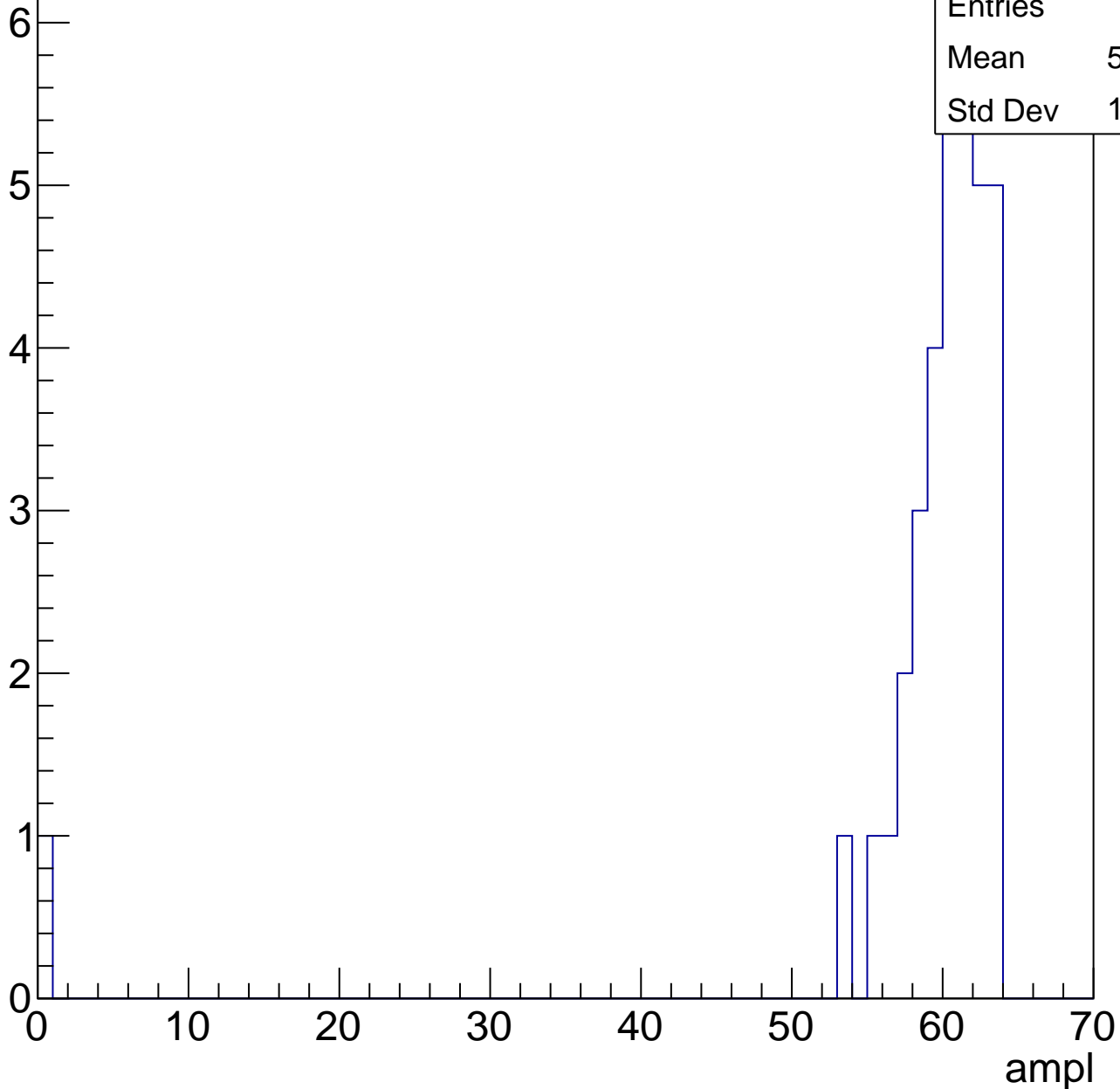


# B1L101S, U16-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

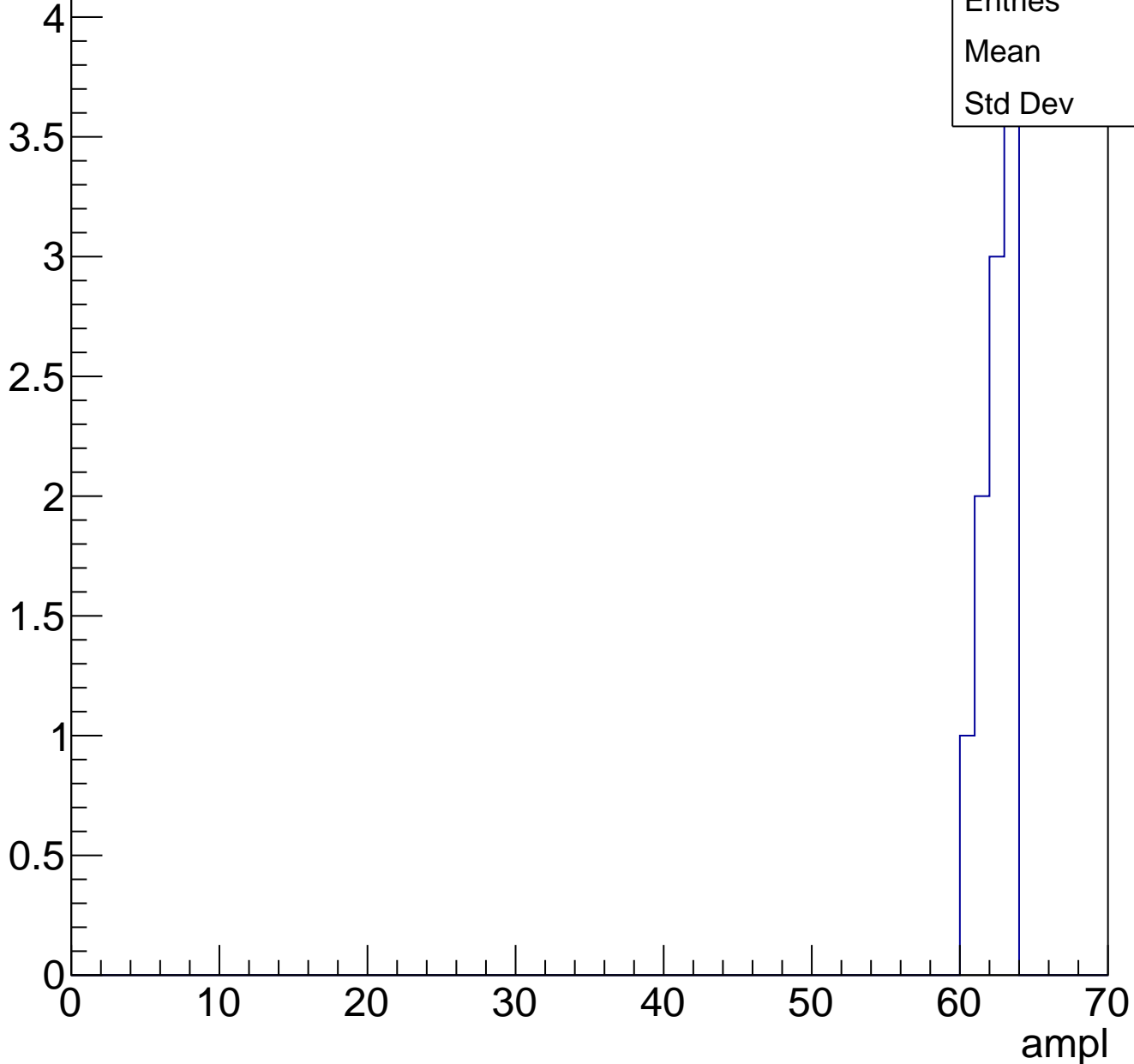
Entries	35
Mean	58.26
Std Dev	10.27



# B1L101S, U16-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U16-ch19, adc0

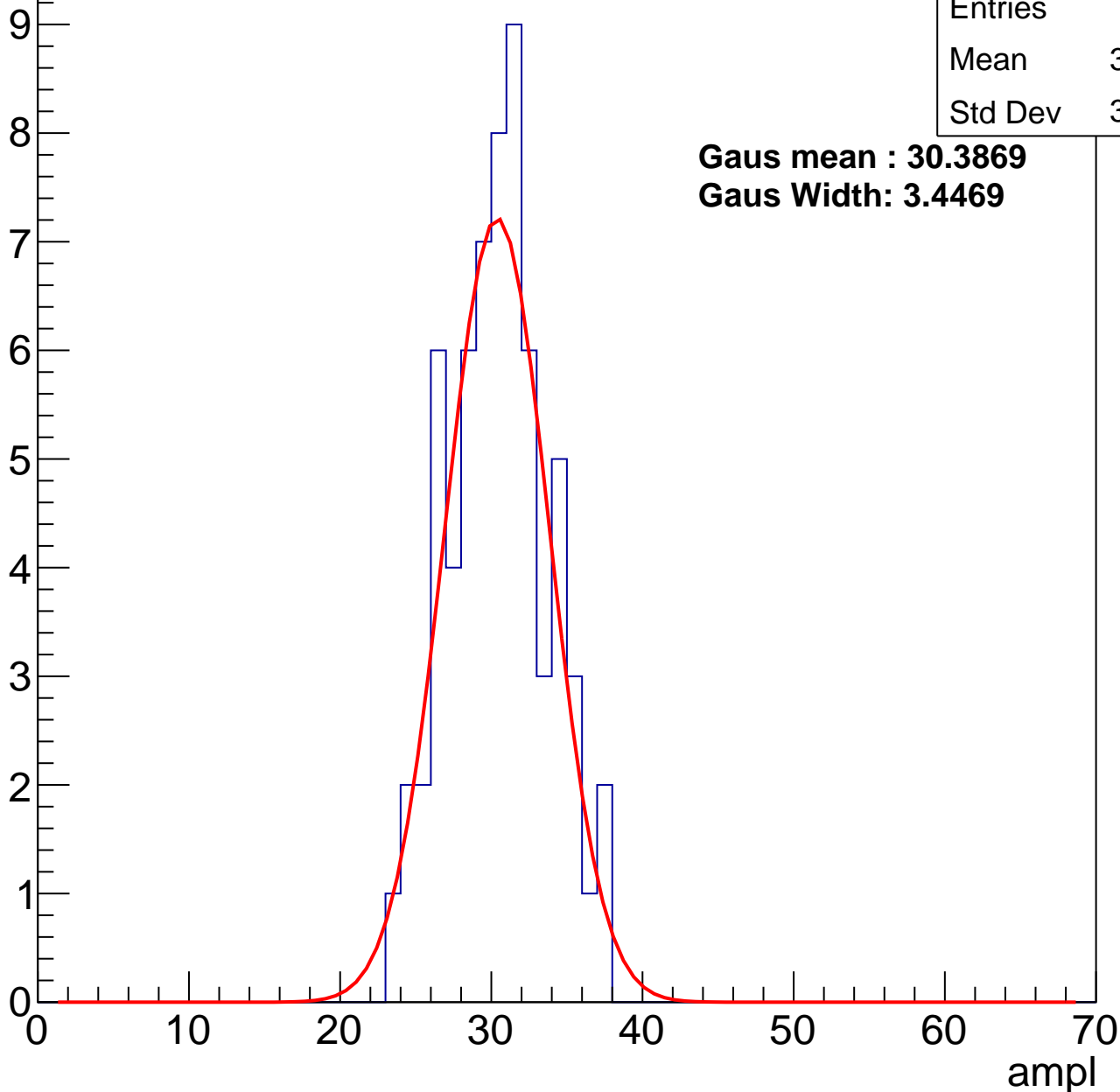
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	30.02
Std Dev	3.242

**Gaus mean : 30.3869**

**Gaus Width: 3.4469**



# B1L101S, U16-ch19, adc1

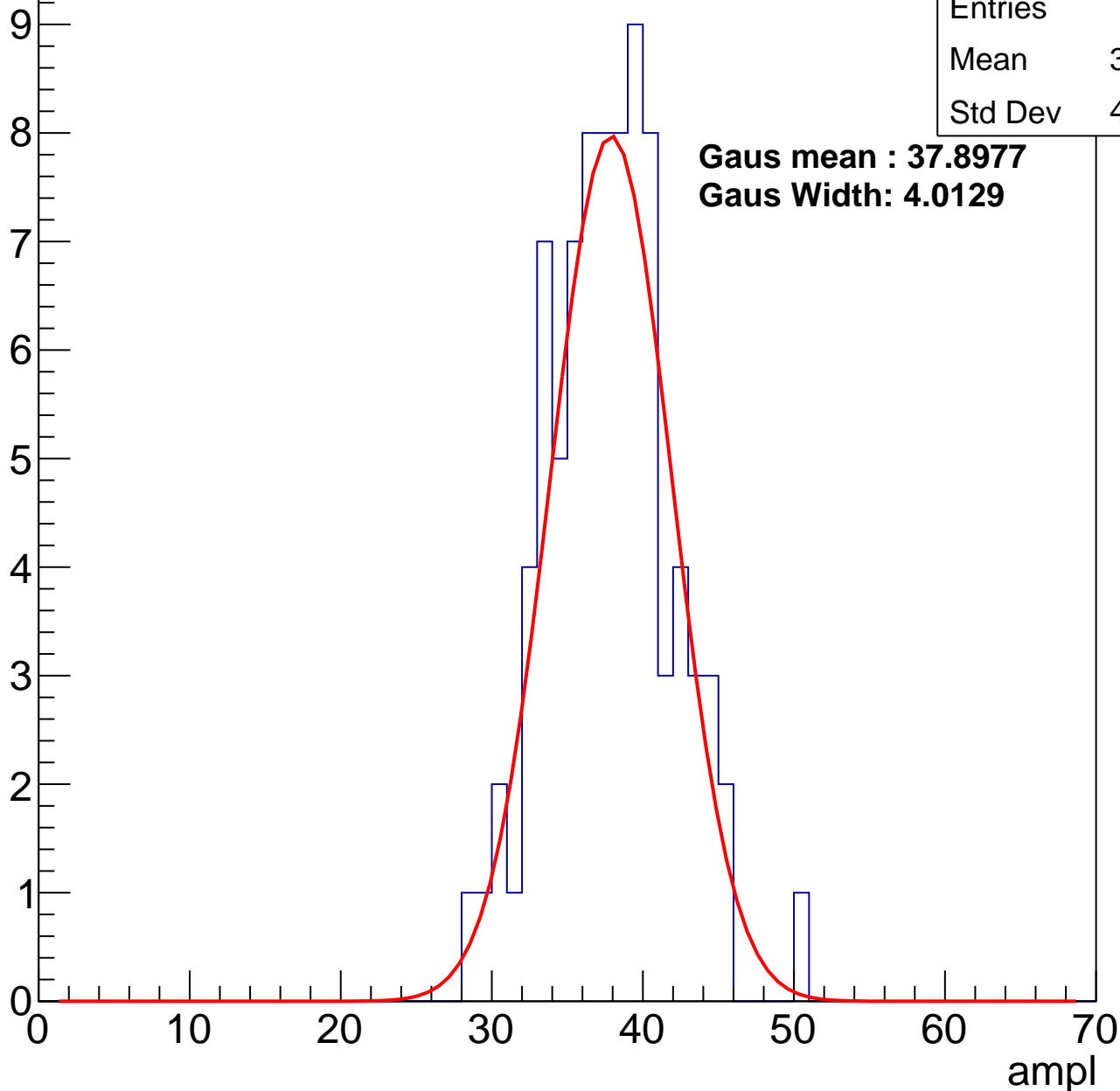
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	85
Mean	37.33
Std Dev	4.028

**Gaus mean : 37.8977**

**Gaus Width: 4.0129**



# B1L101S, U16-ch19, adc2

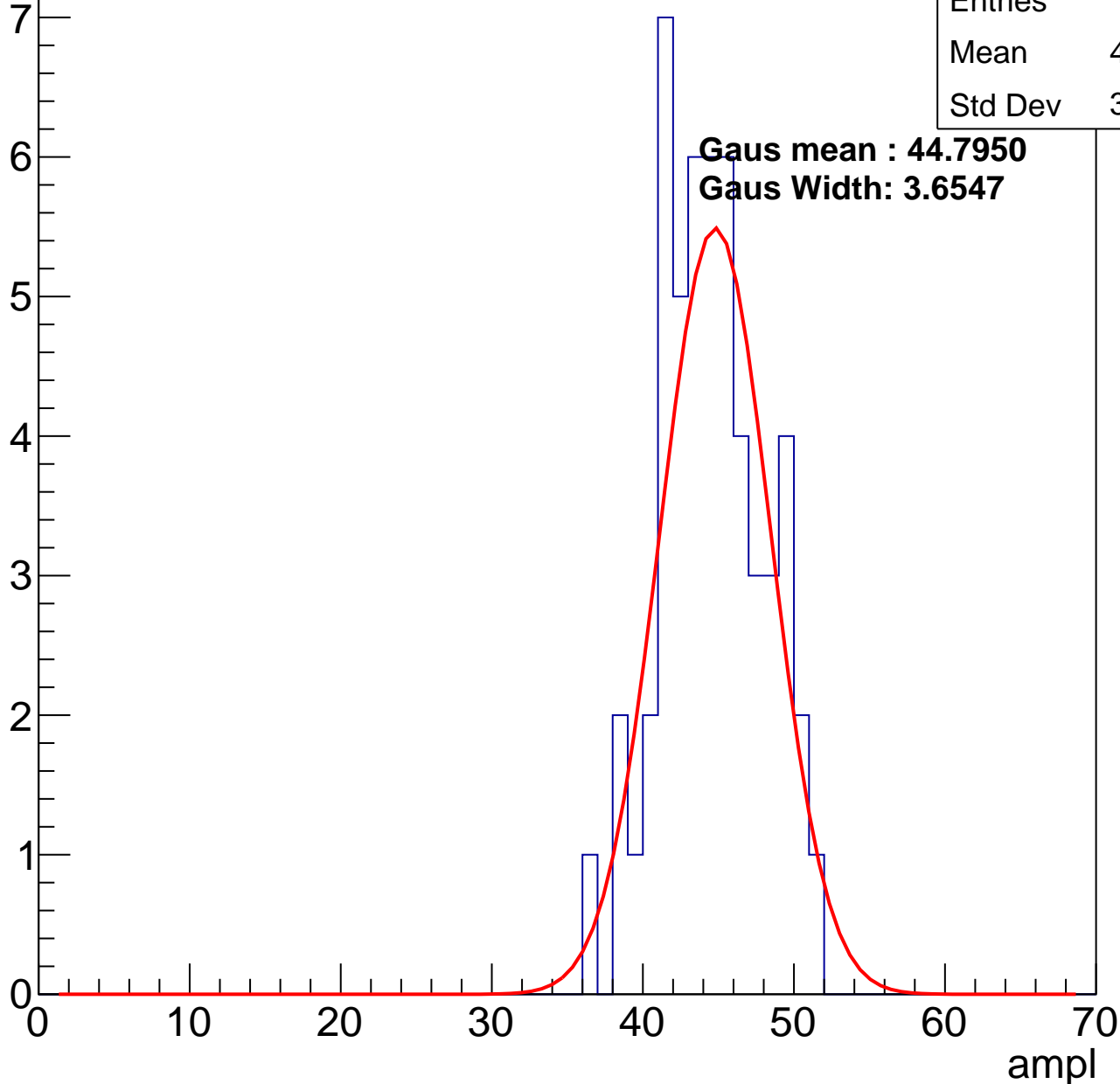
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	44.08
Std Dev	3.364

**Gaus mean : 44.7950**

**Gaus Width: 3.6547**

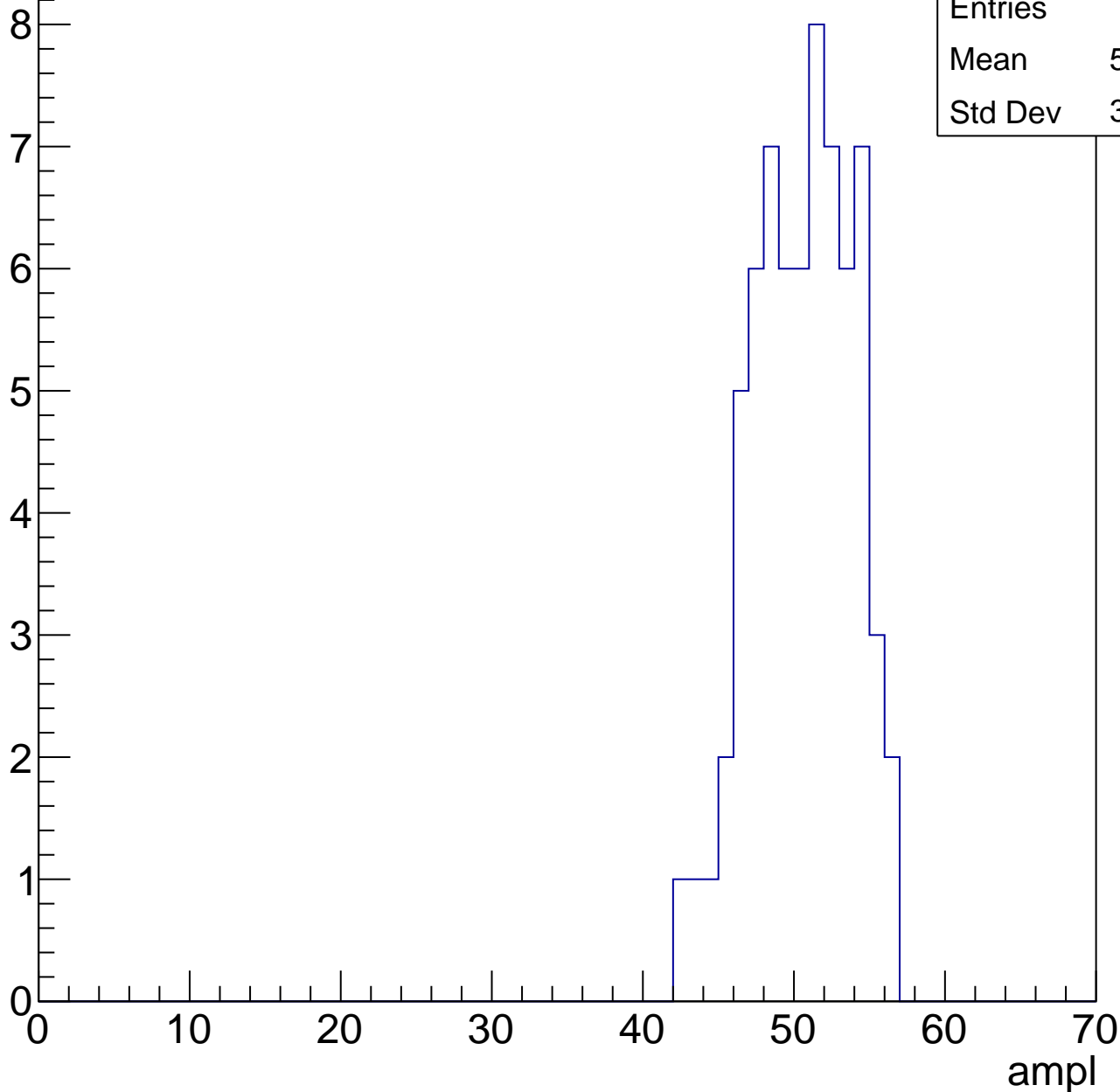


# B1L101S, U16-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	50.09
Std Dev	3.244

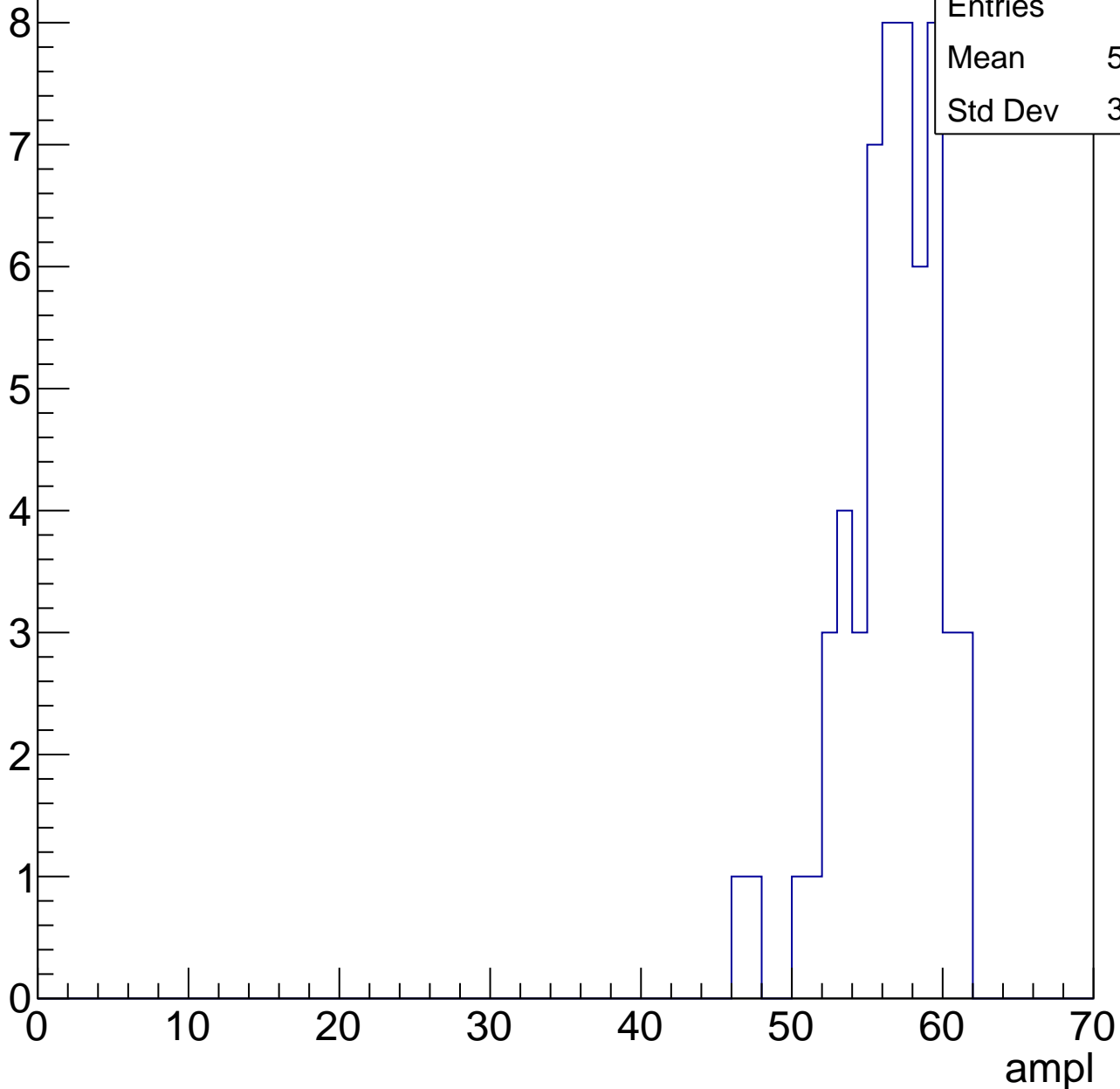


# B1L101S, U16-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	56.07
Std Dev	3.167

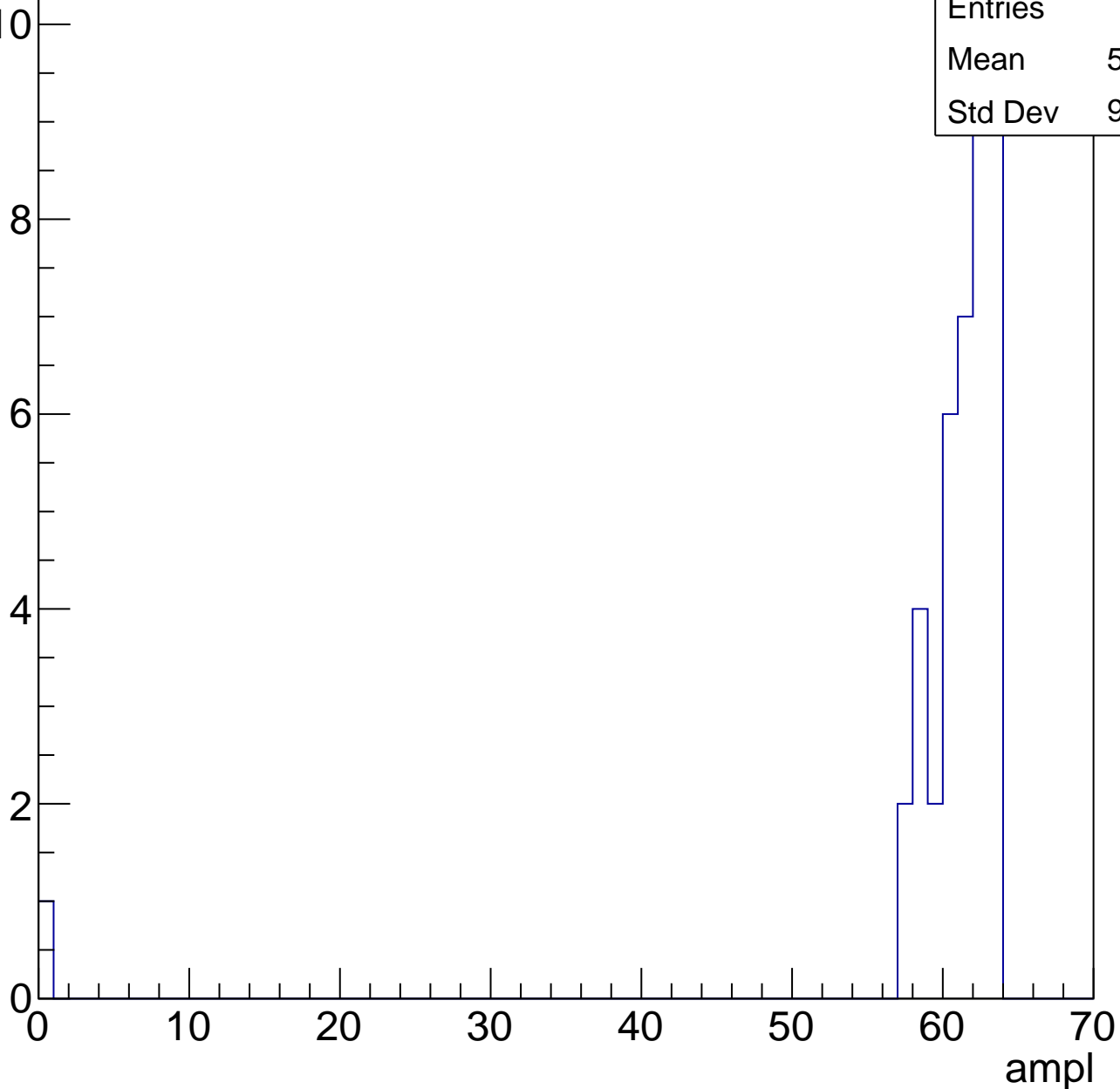


# B1L101S, U16-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	41
Mean	59.46
Std Dev	9.566



# B1L101S, U16-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch20, adc0

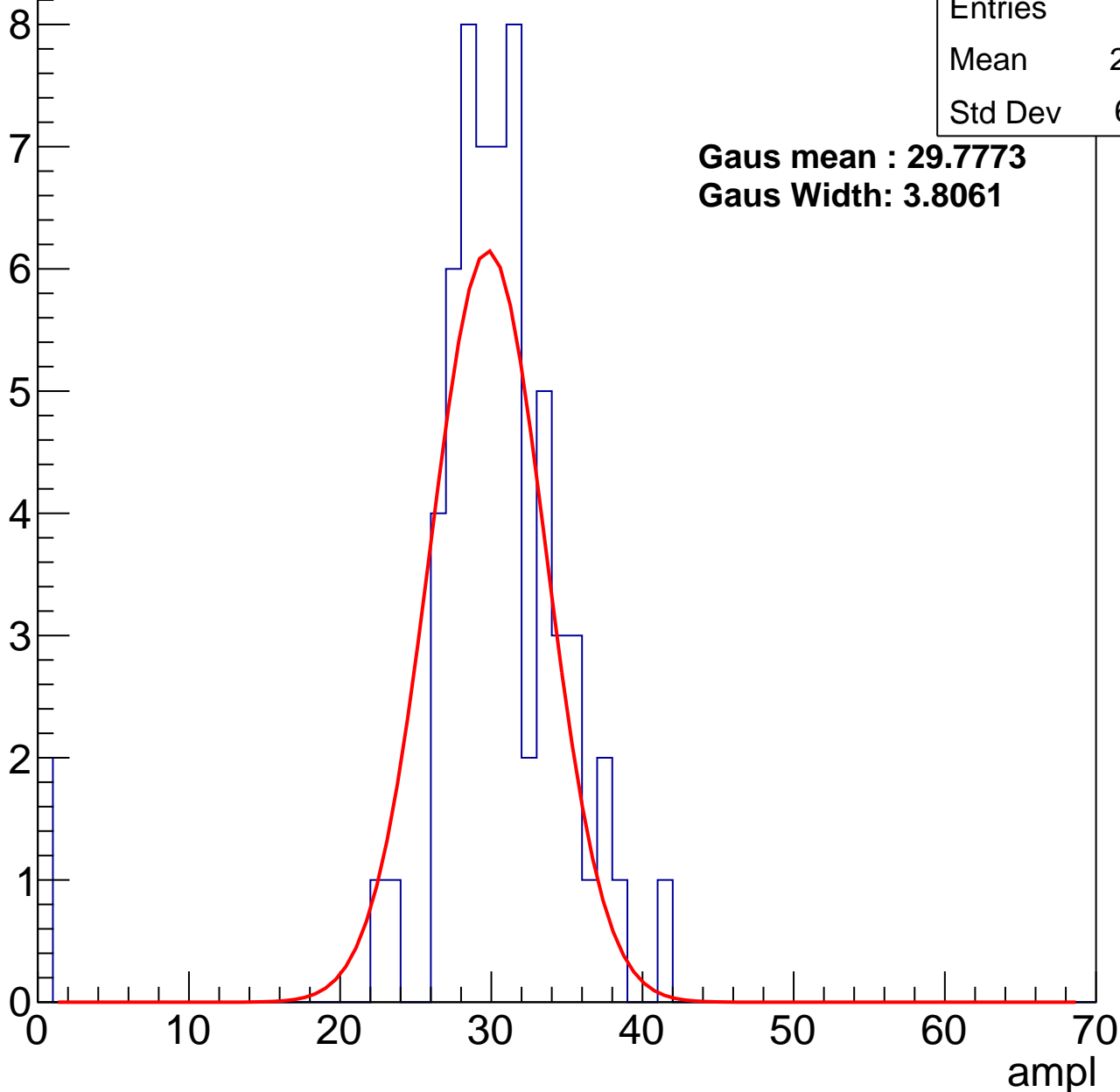
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	29.37
Std Dev	6.411

**Gaus mean : 29.7773**

**Gaus Width: 3.8061**



# B1L101S, U16-ch20, adc1

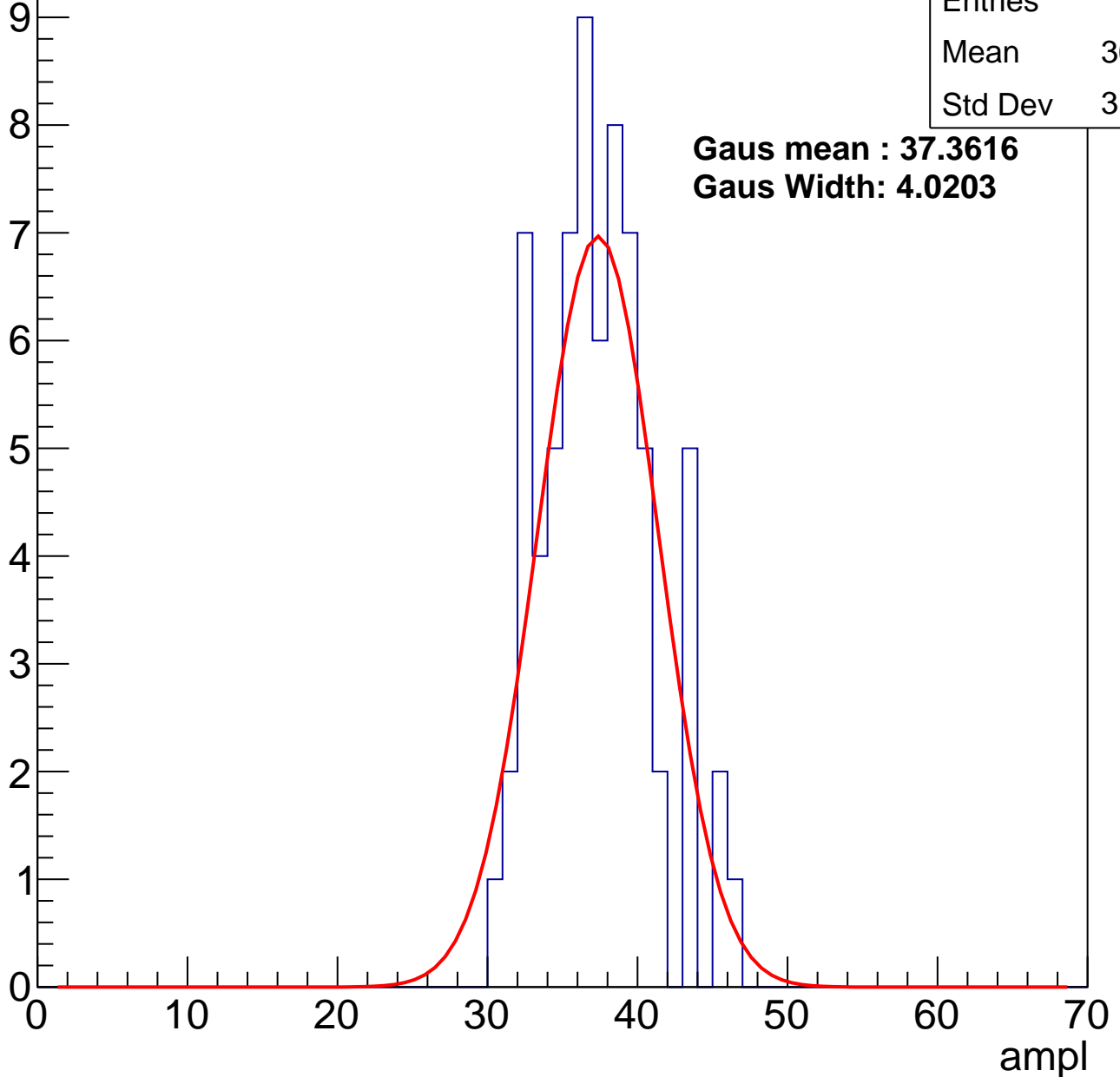
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	36.89
Std Dev	3.645

**Gaus mean : 37.3616**

**Gaus Width: 4.0203**



# B1L101S, U16-ch20, adc2

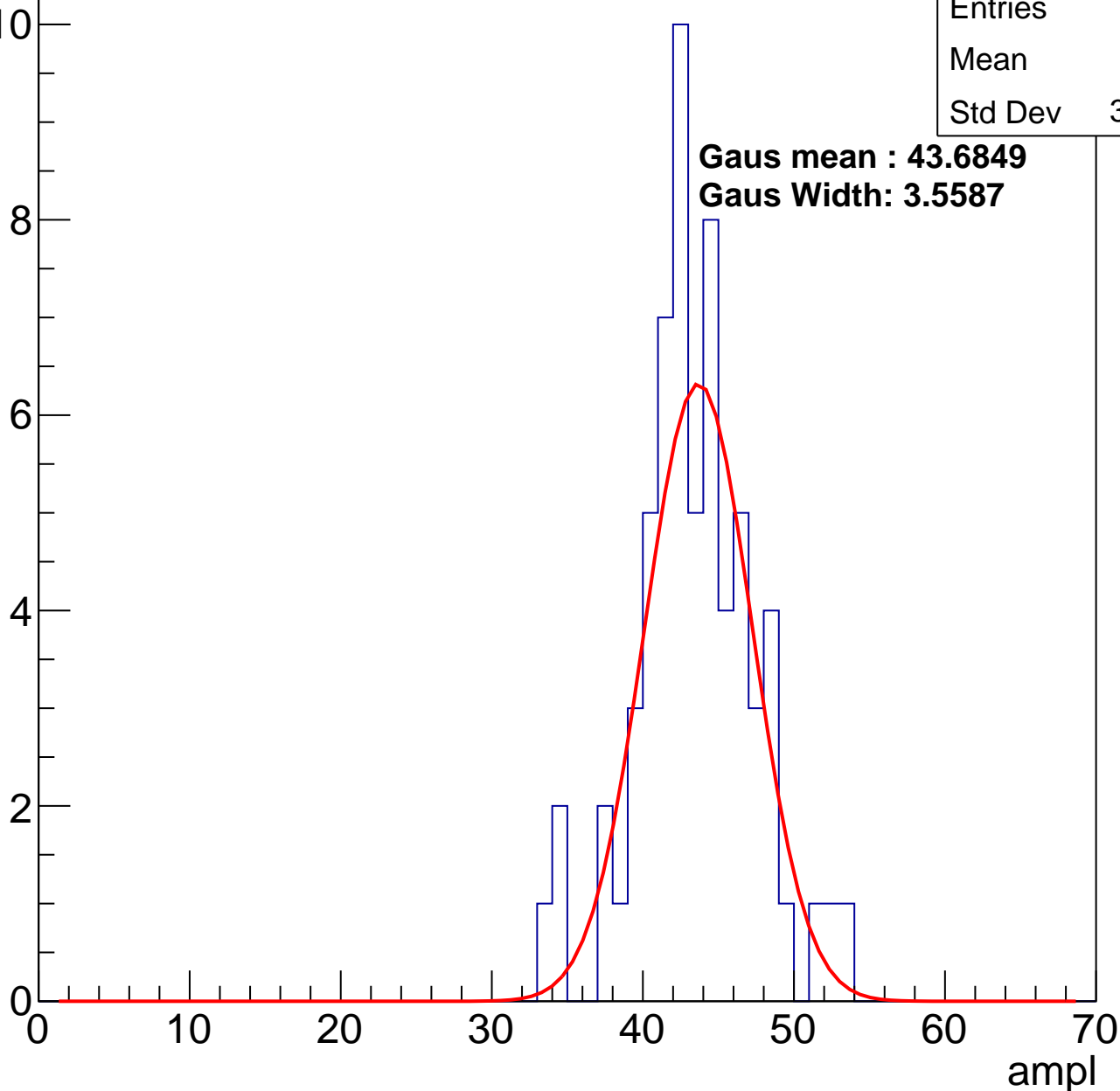
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	43
Std Dev	3.929

**Gaus mean : 43.6849**

**Gaus Width: 3.5587**

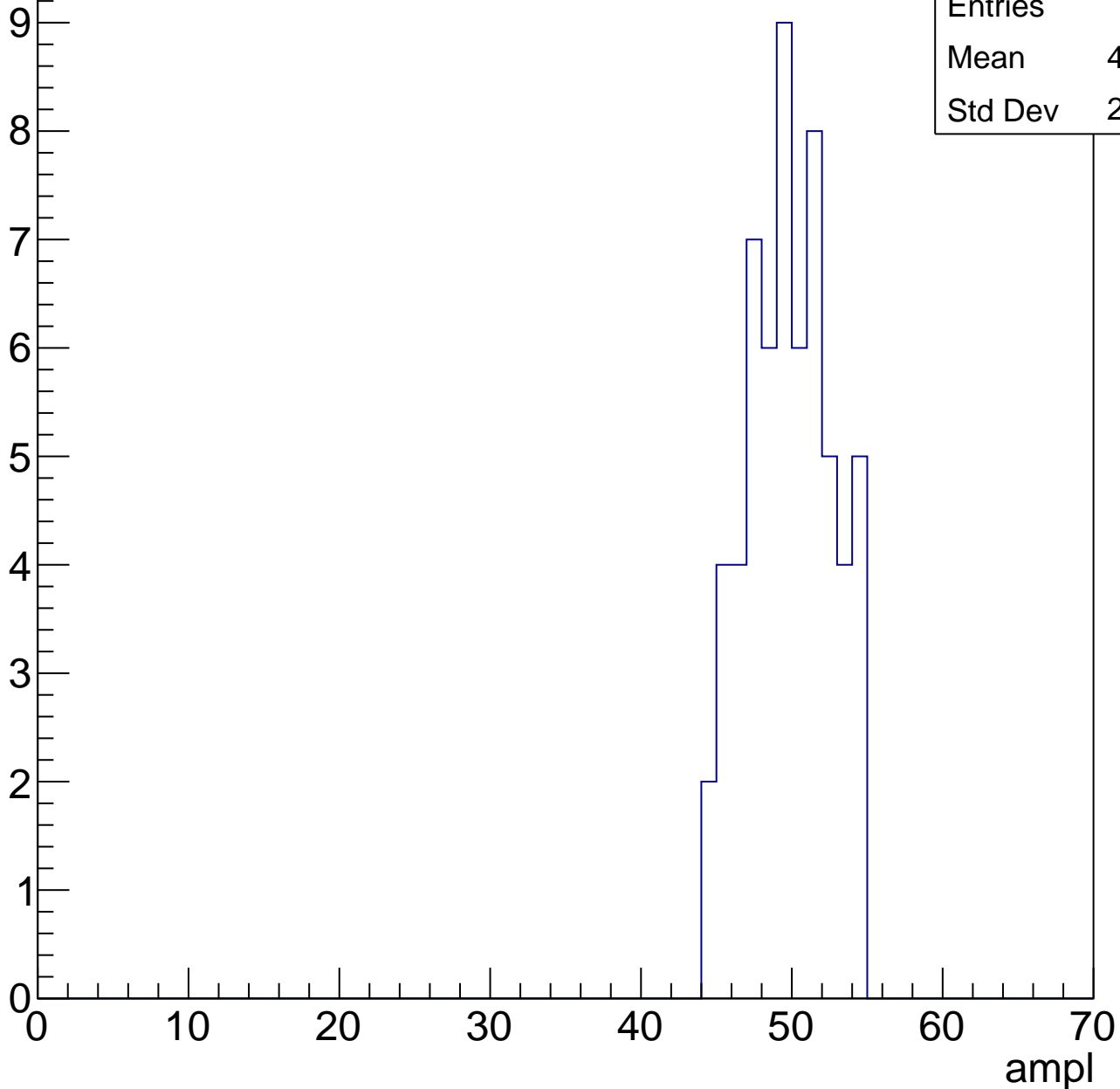


# B1L101S, U16-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

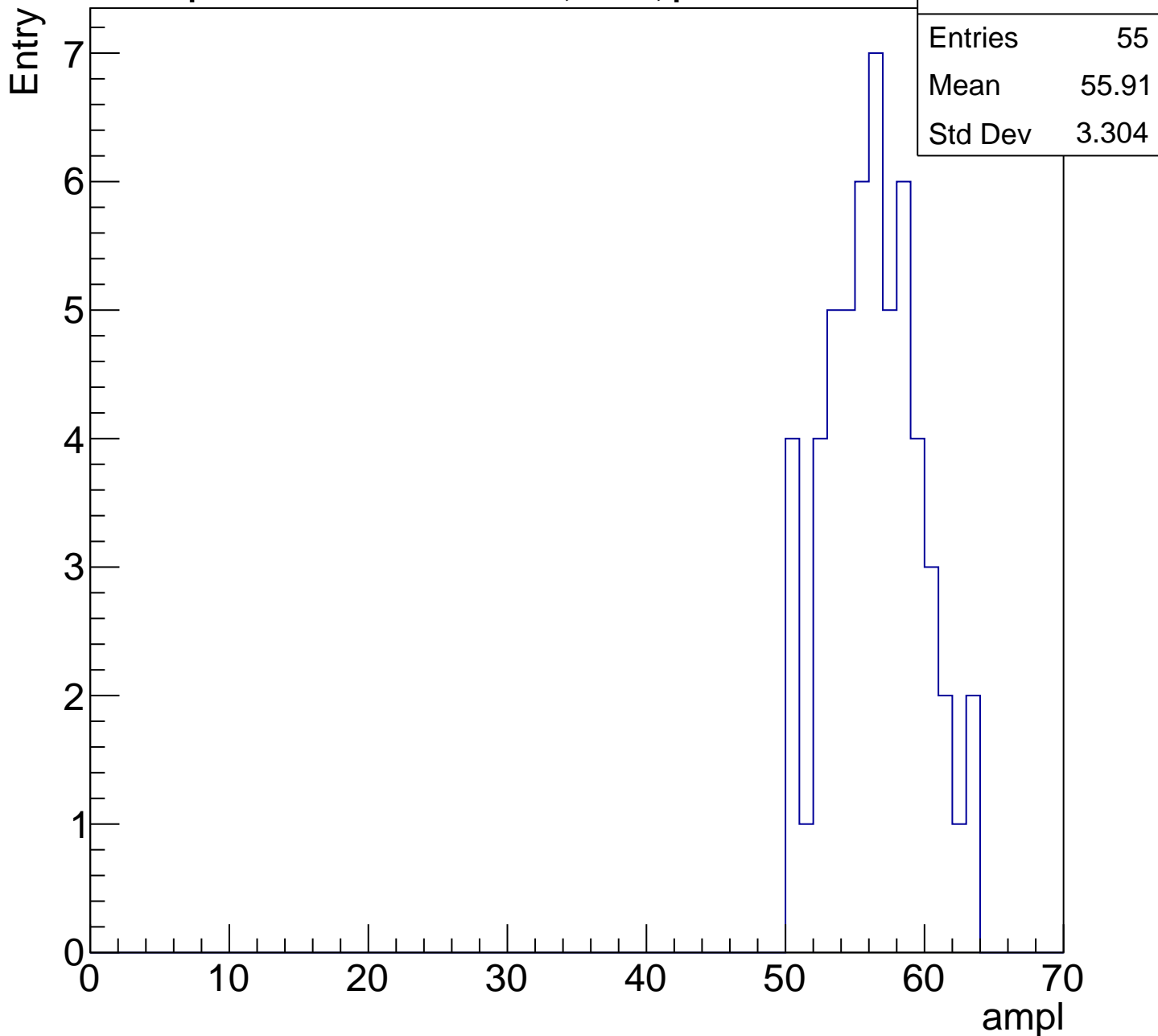
Entry

Entries	60
Mean	49.33
Std Dev	2.737



# B1L101S, U16-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

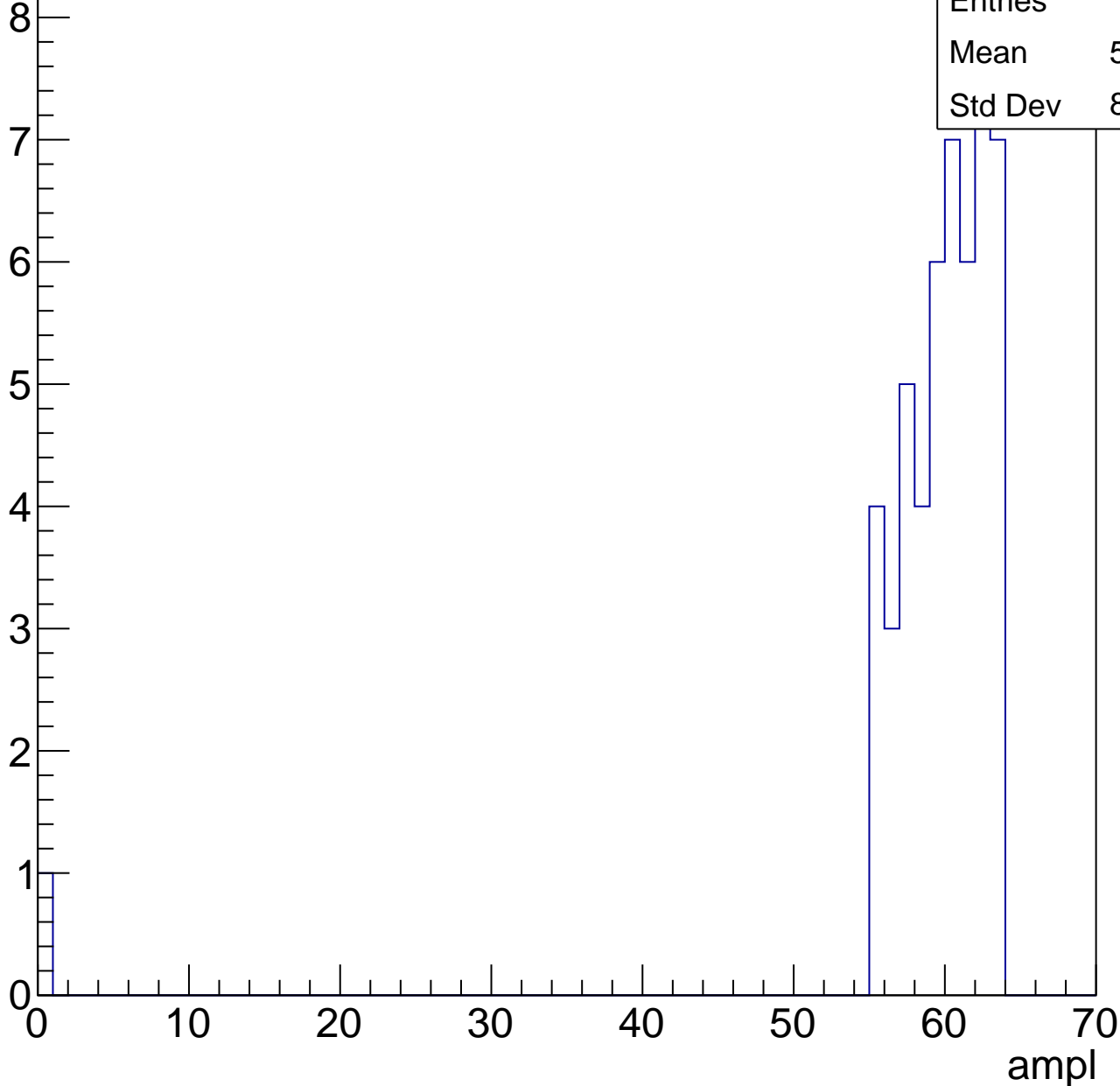


# B1L101S, U16-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

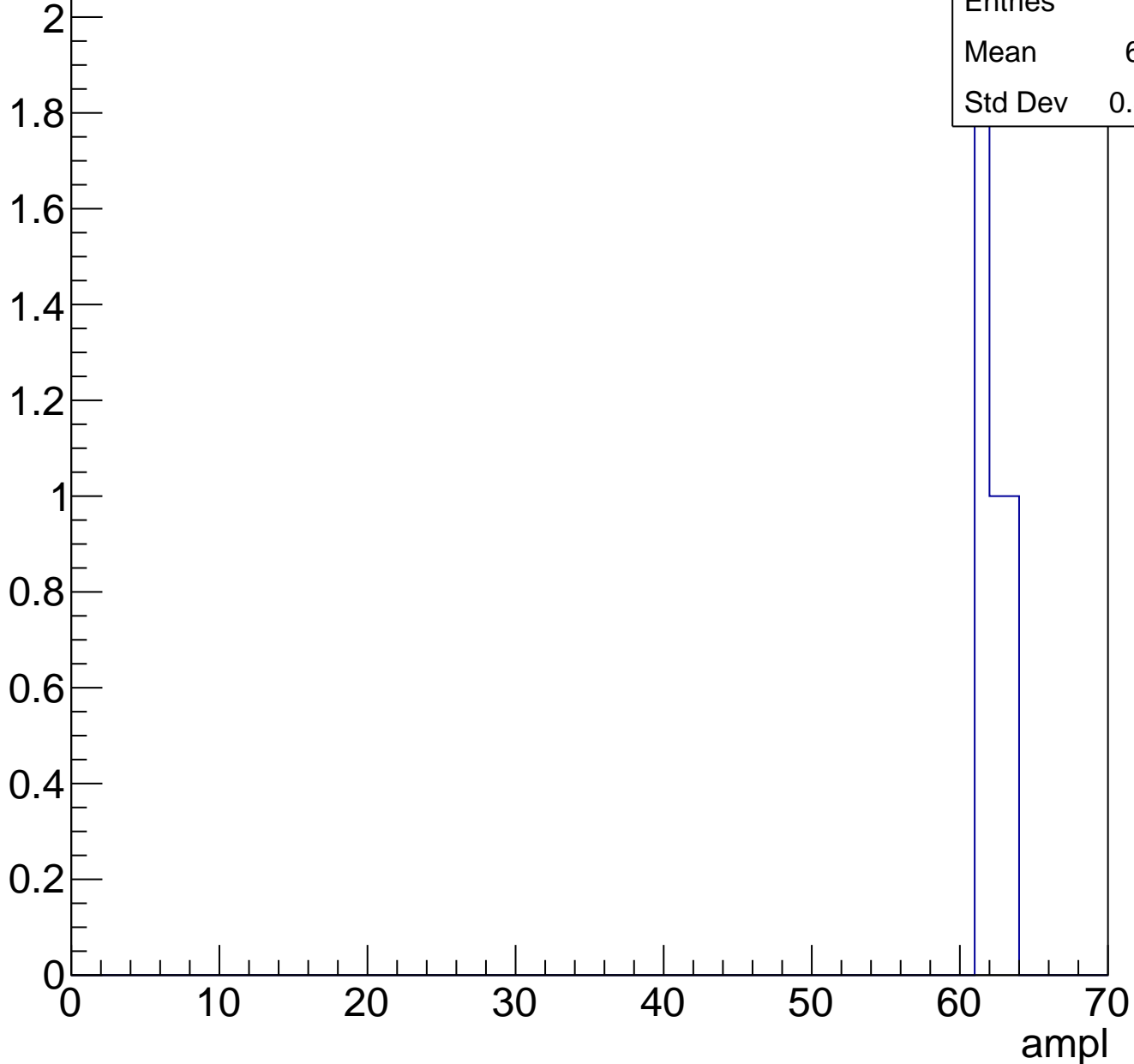
Entries	51
Mean	58.47
Std Dev	8.628



# B1L101S, U16-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U16-ch21, adc0

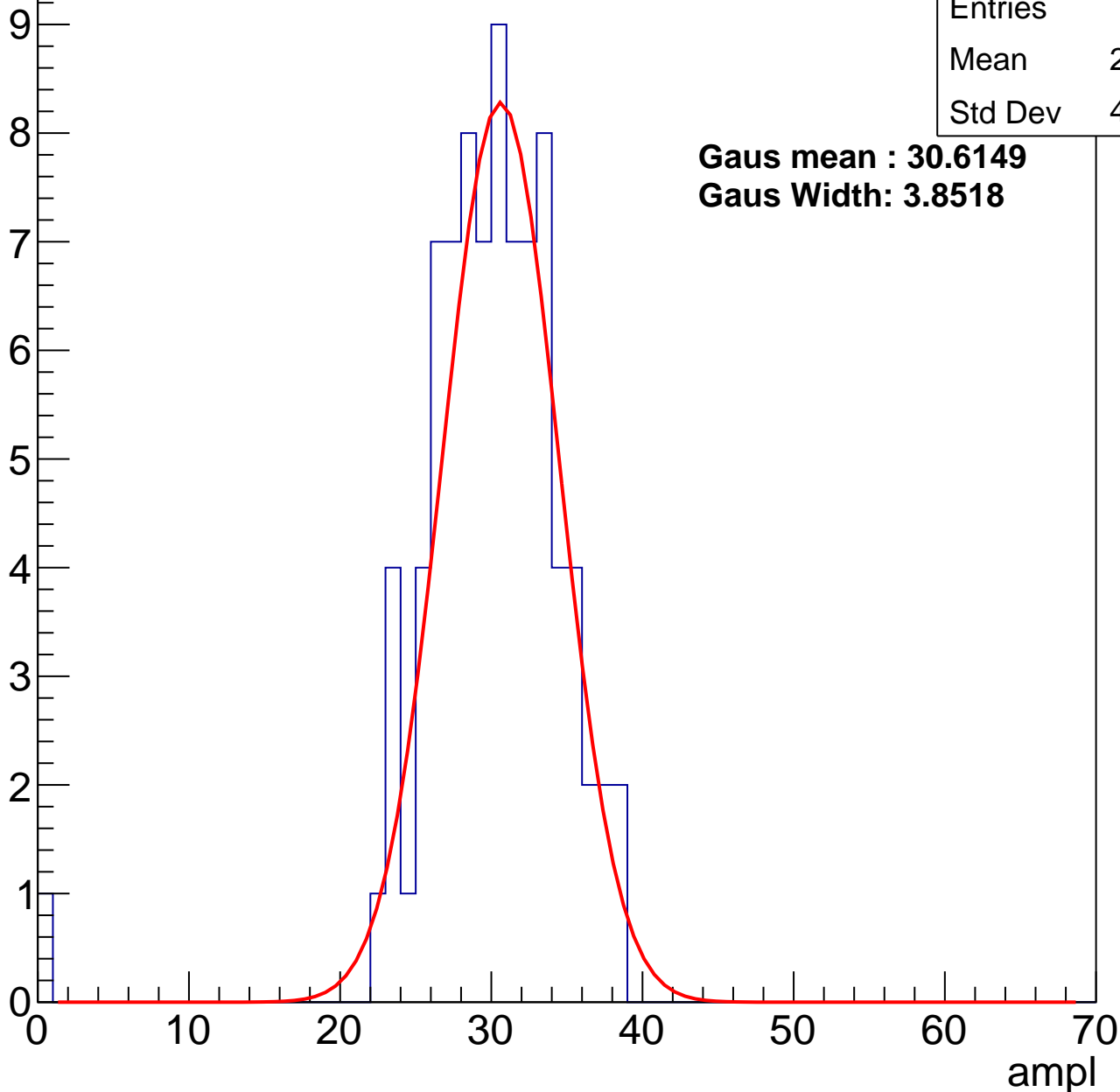
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	85
Mean	29.52
Std Dev	4.922

**Gaus mean : 30.6149**

**Gaus Width: 3.8518**



# B1L101S, U16-ch21, adc1

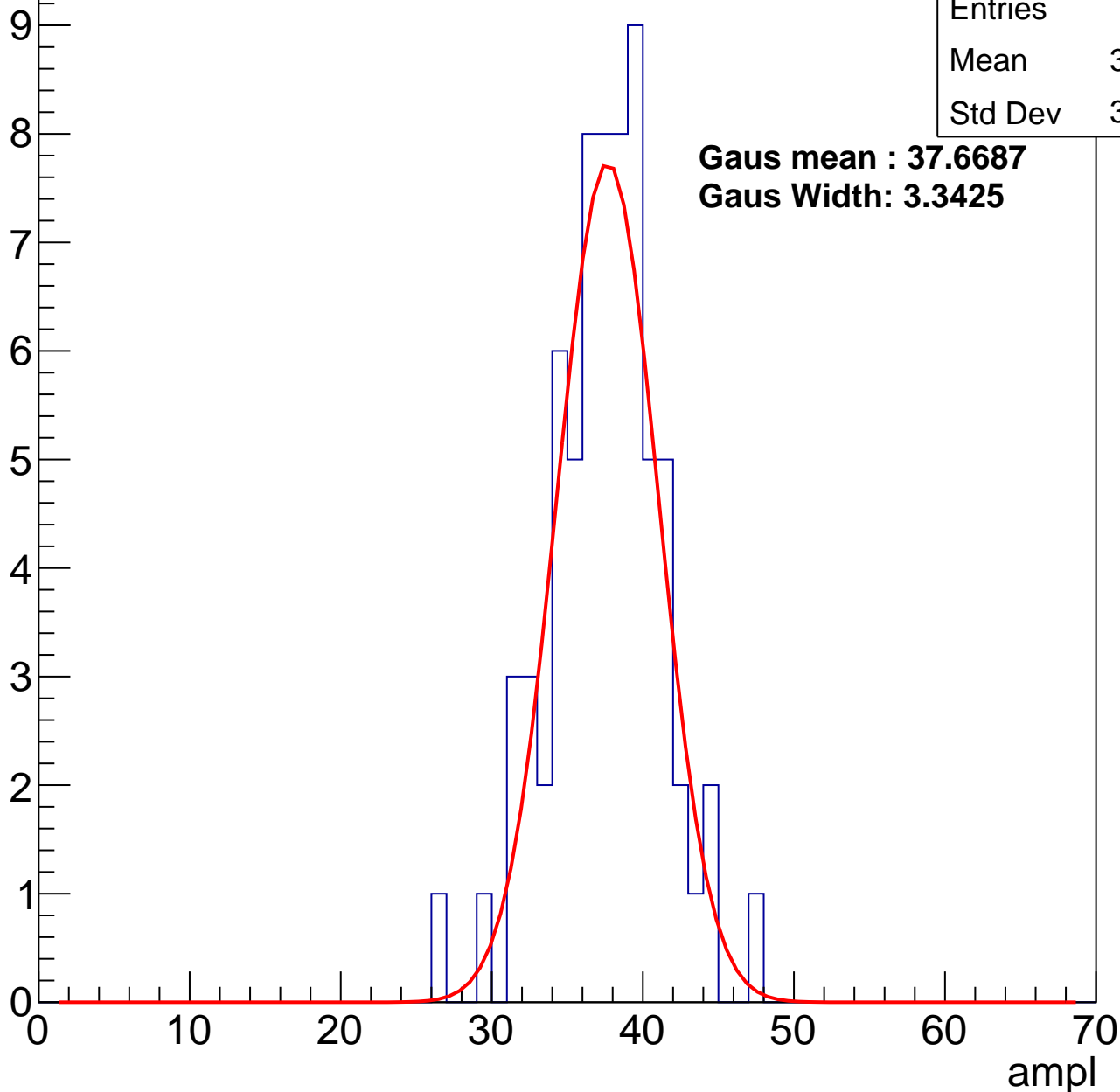
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	37.07
Std Dev	3.654

**Gaus mean : 37.6687**

**Gaus Width: 3.3425**



# B1L101S, U16-ch21, adc2

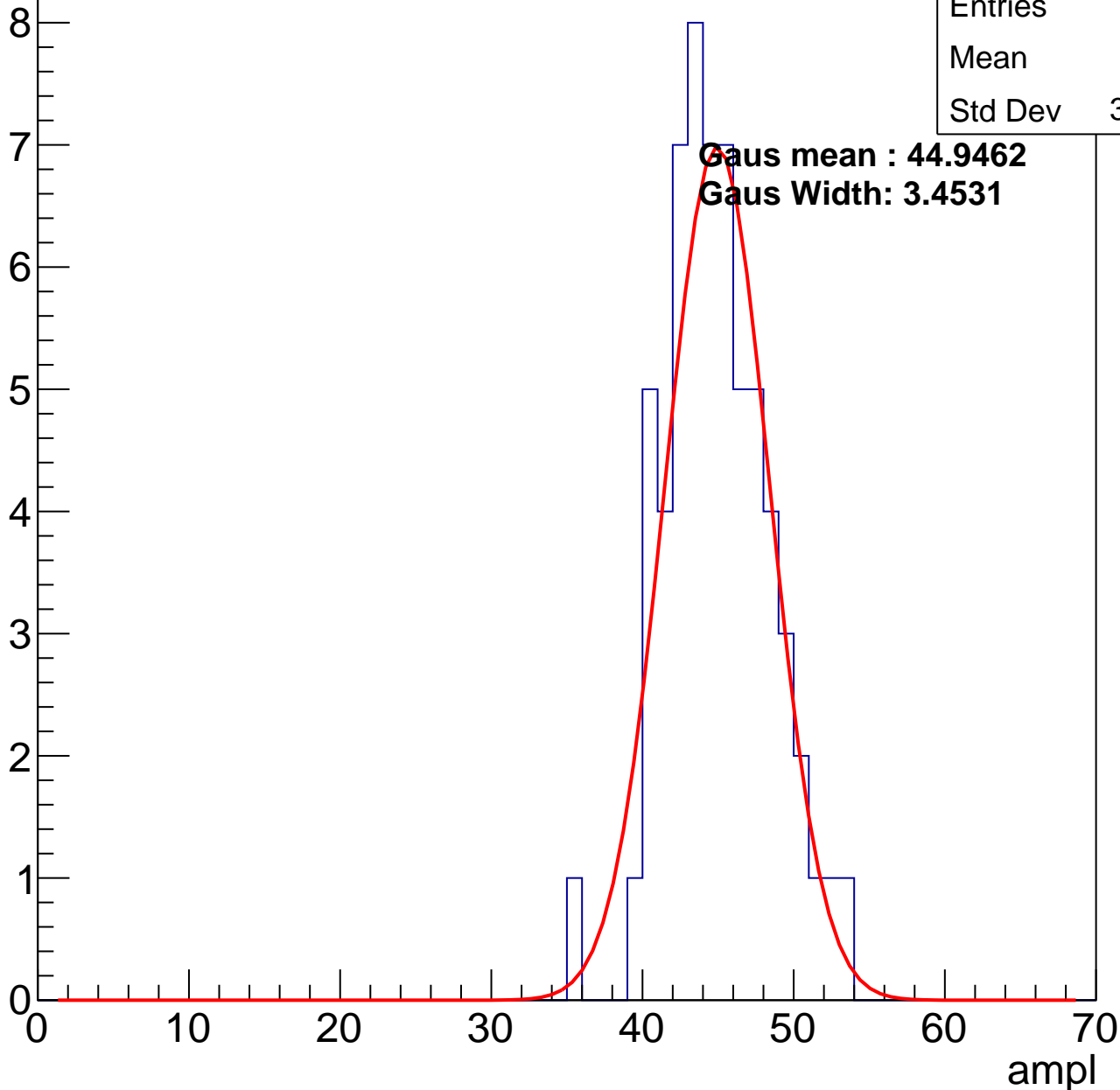
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	44.5
Std Dev	3.407

Gaus mean : 44.9462

Gaus Width: 3.4531

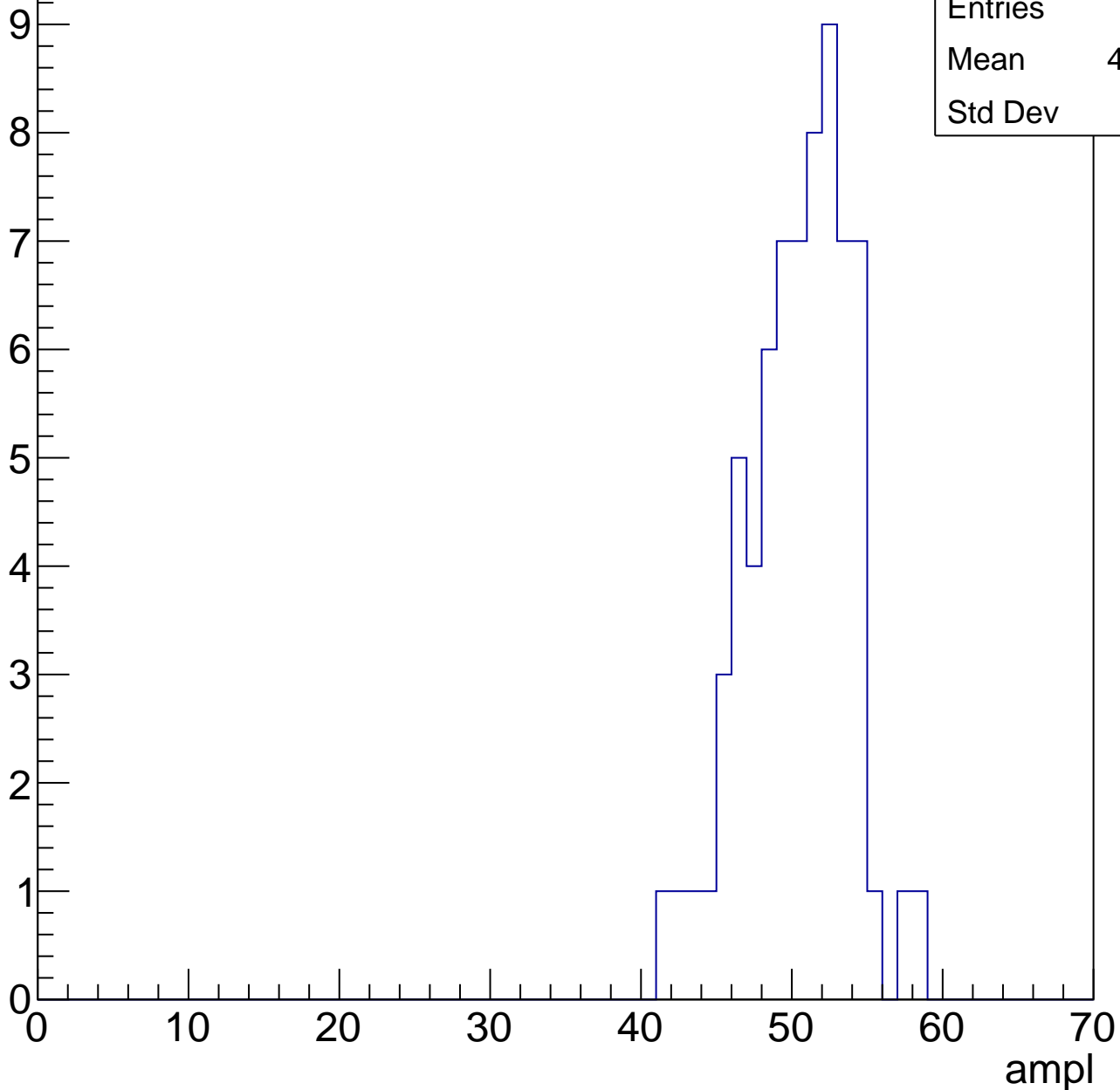


# B1L101S, U16-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	49.99
Std Dev	3.4

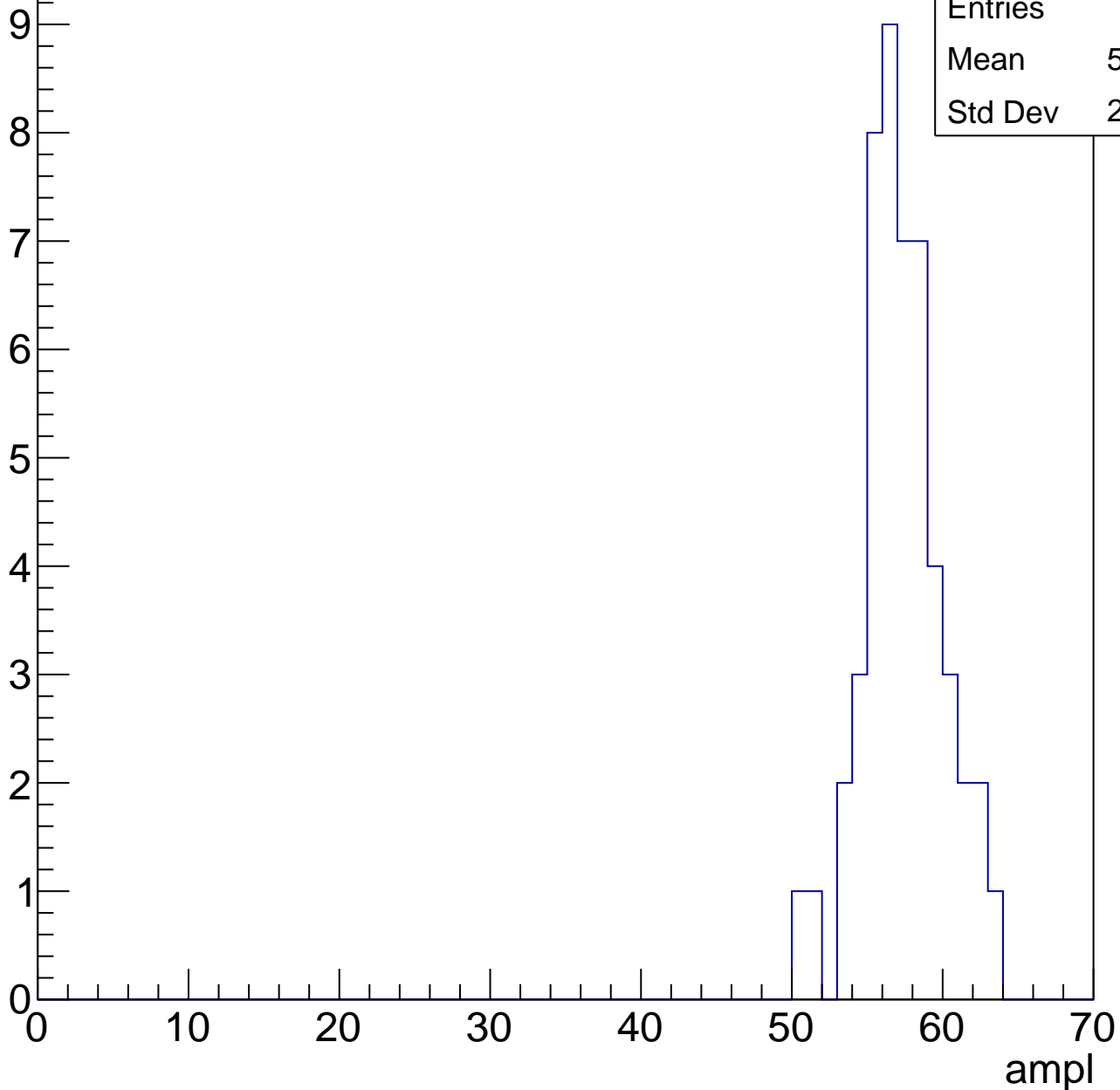


# B1L101S, U16-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	56.86
Std Dev	2.653

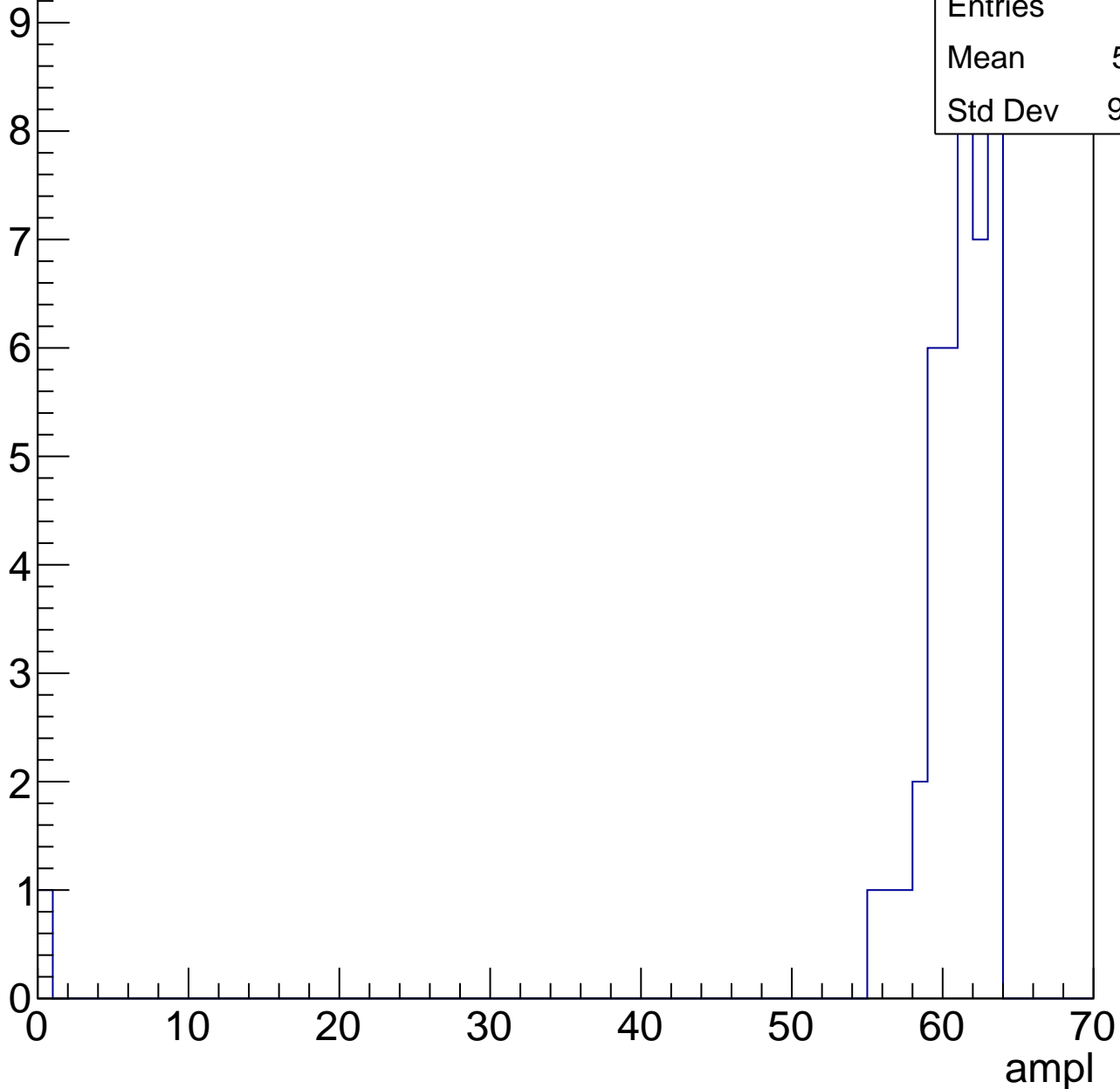


# B1L101S, U16-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	59.21
Std Dev	9.455



# B1L101S, U16-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

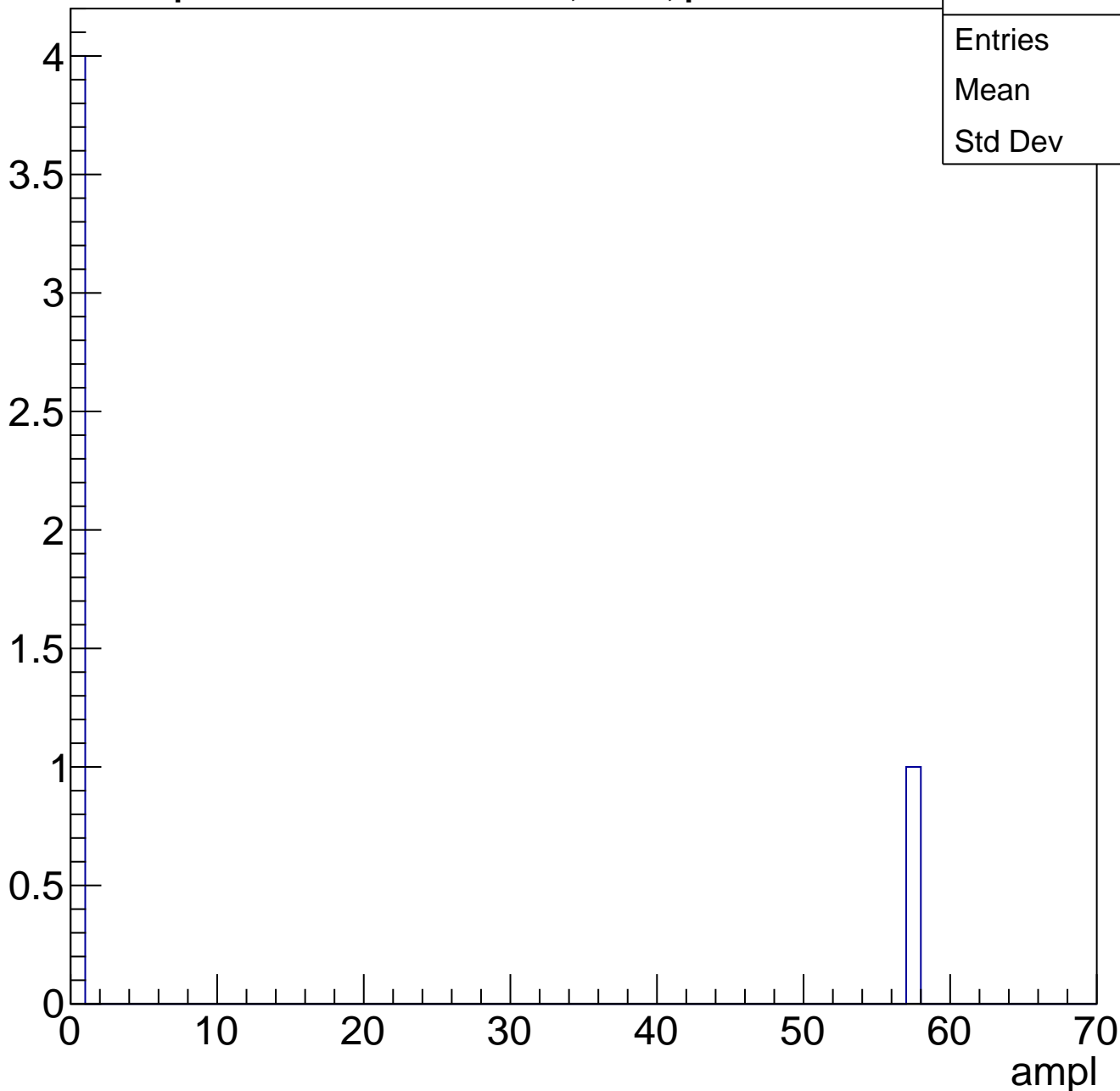




# B1L101S, U16-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	5
Mean	11.4
Std Dev	22.8

# B1L101S, U16-ch22, adc0

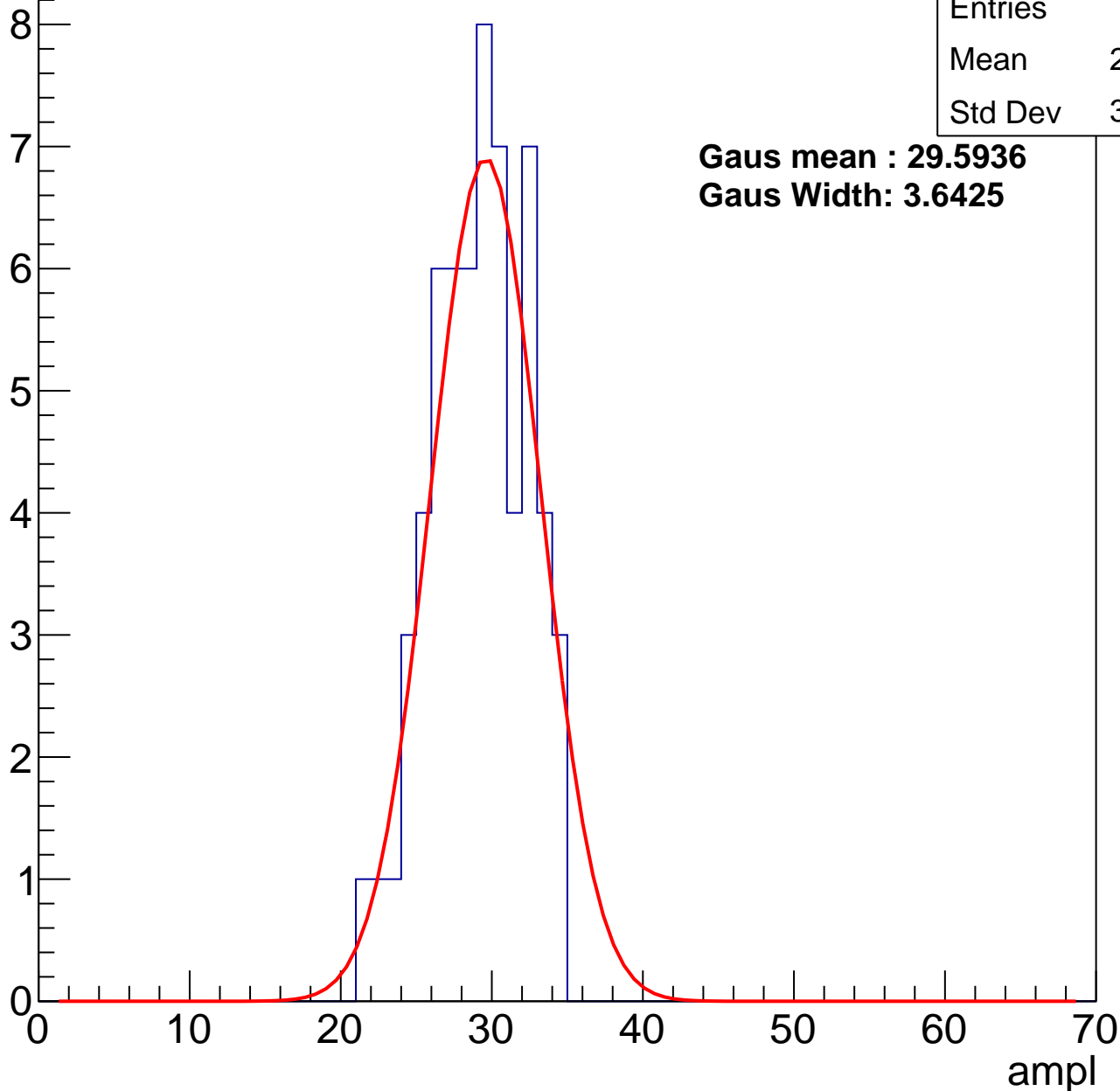
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	28.66
Std Dev	3.109

**Gaus mean : 29.5936**

**Gaus Width: 3.6425**



# B1L101S, U16-ch22, adc1

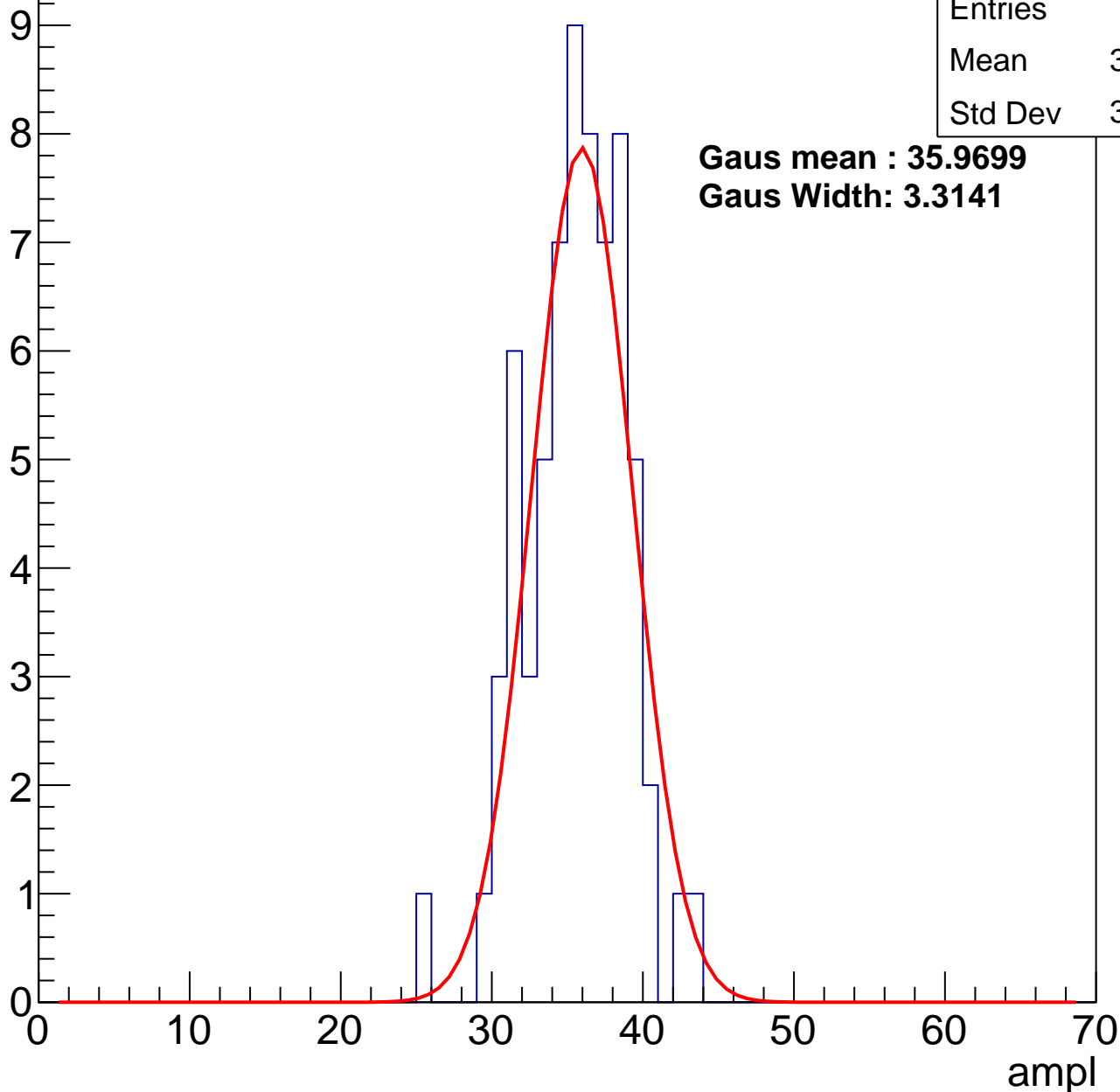
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	35.15
Std Dev	3.256

**Gaus mean : 35.9699**

**Gaus Width: 3.3141**



# B1L101S, U16-ch22, adc2

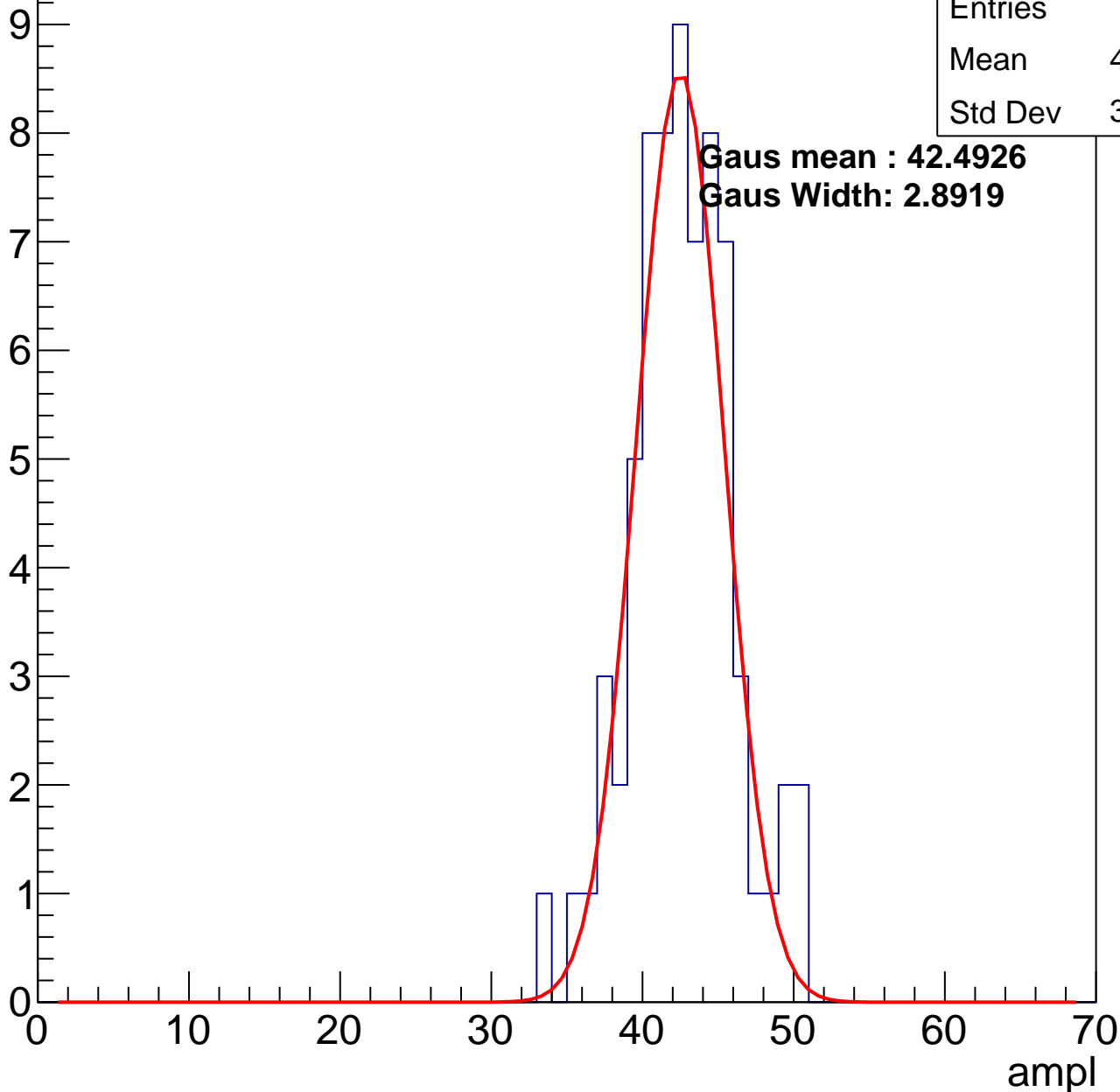
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	42.19
Std Dev	3.389

**Gaus mean : 42.4926**

**Gaus Width: 2.8919**

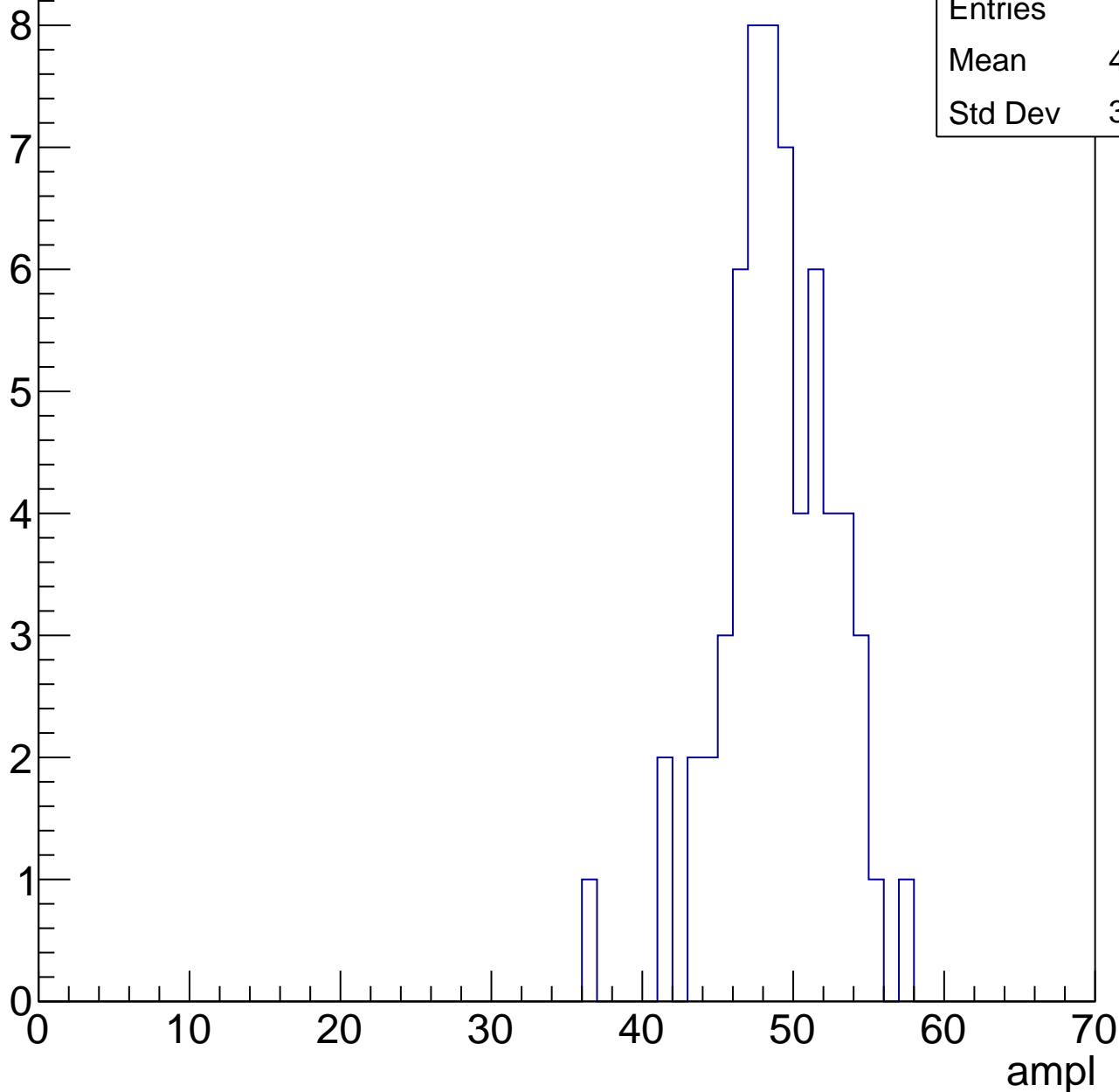


# B1L101S, U16-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	48.48
Std Dev	3.697

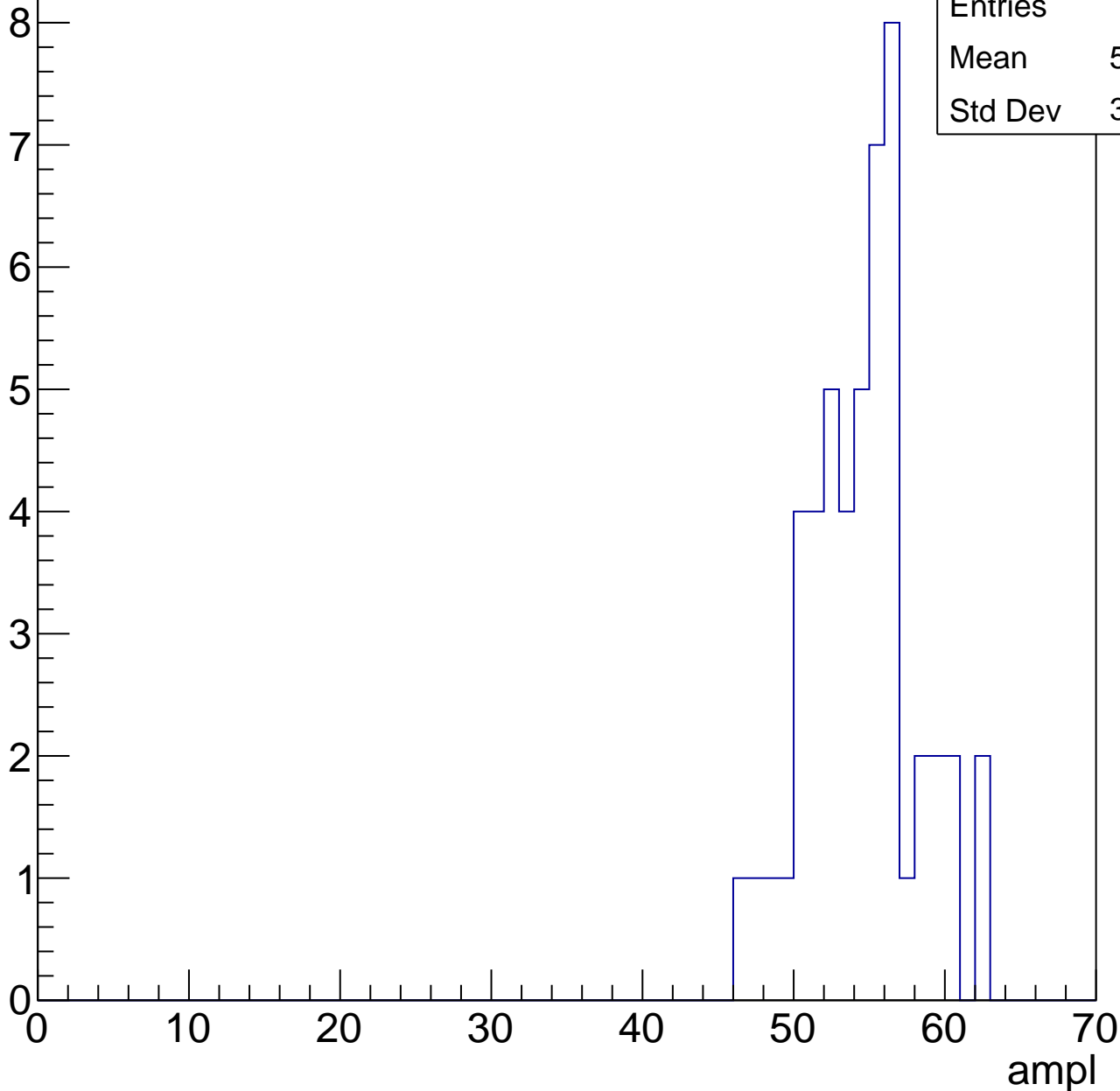


# B1L101S, U16-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

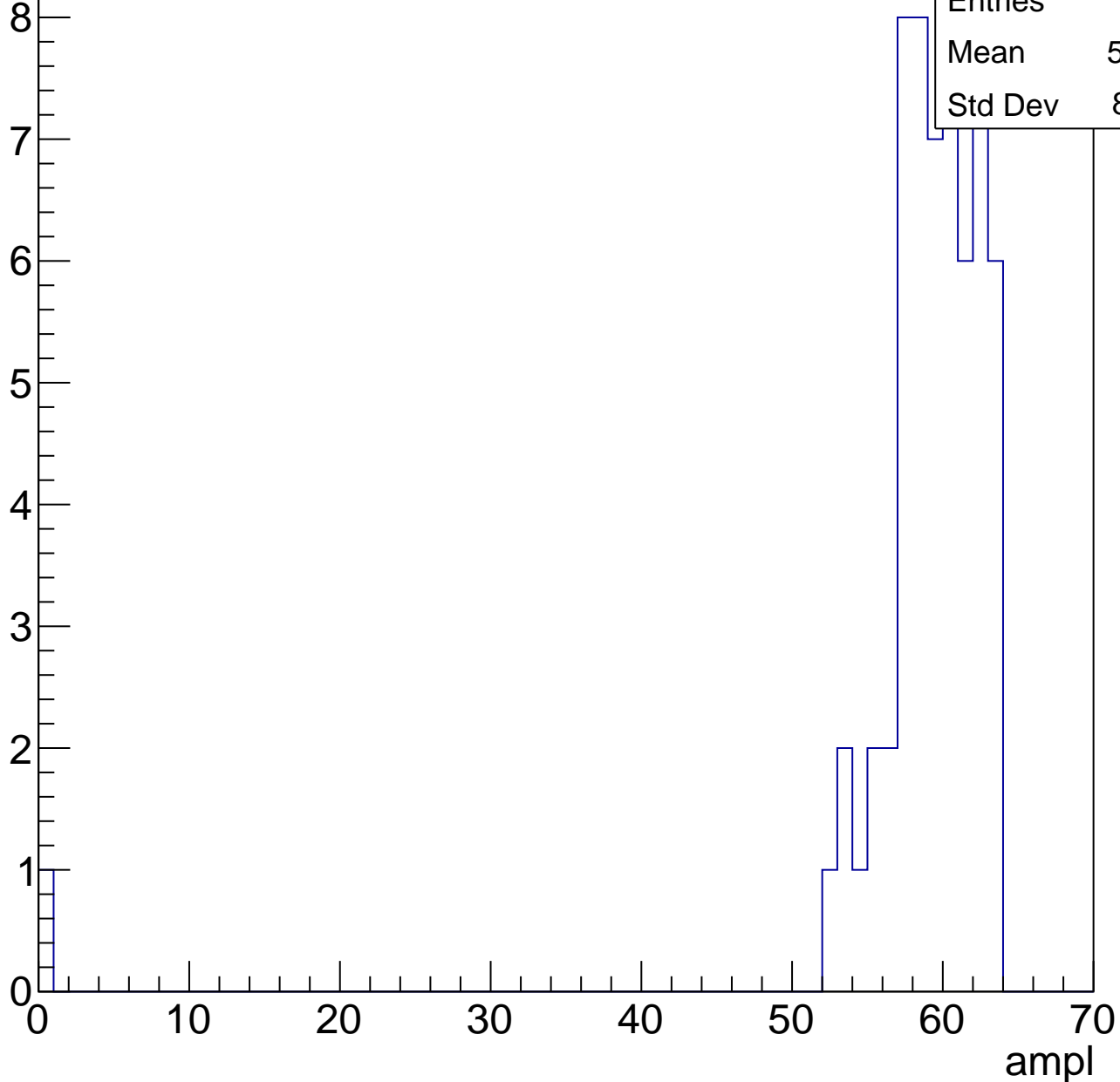
Entries	50
Mean	54.08
Std Dev	3.543



# B1L101S, U16-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

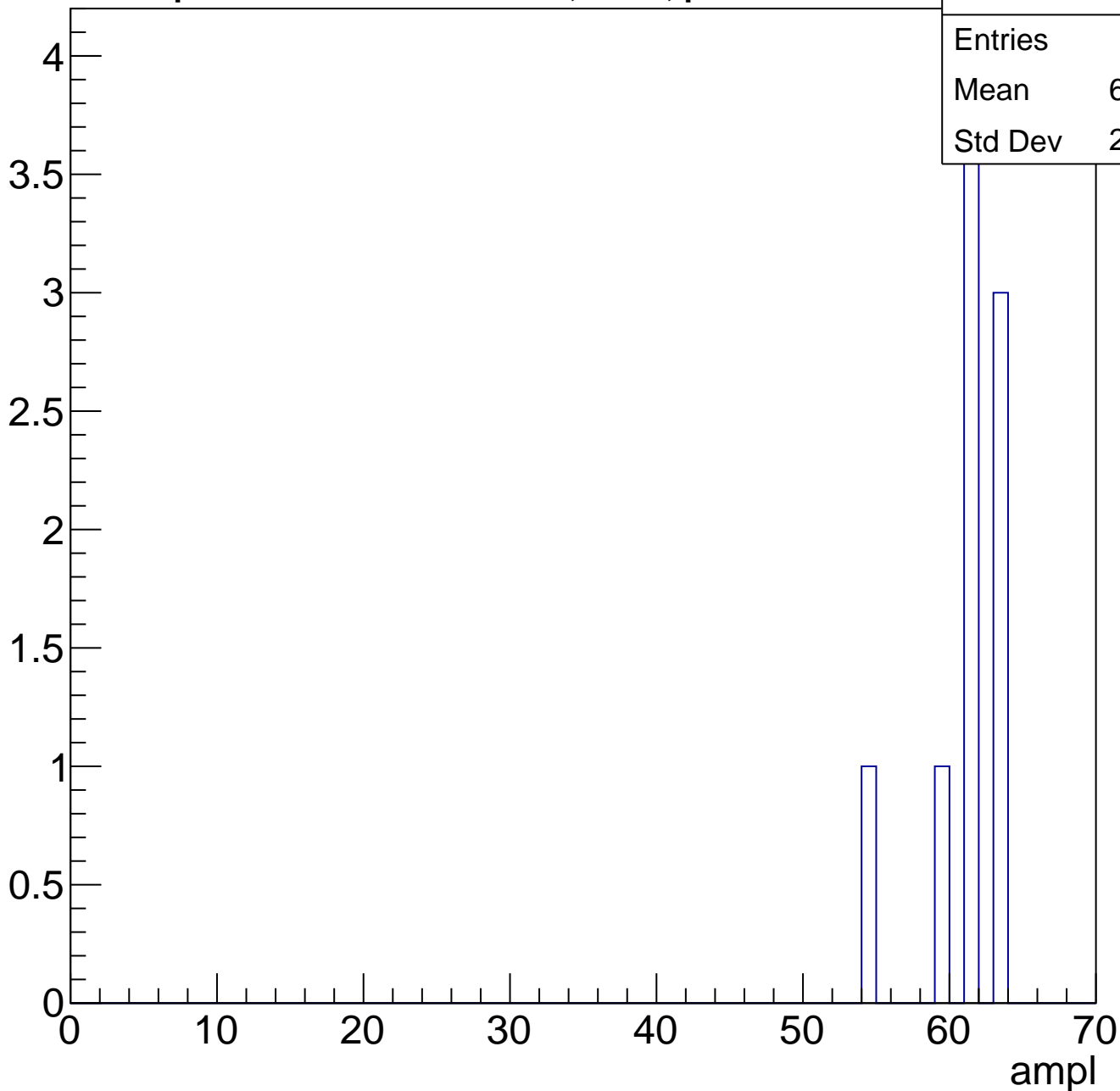
Entry



# B1L101S, U16-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

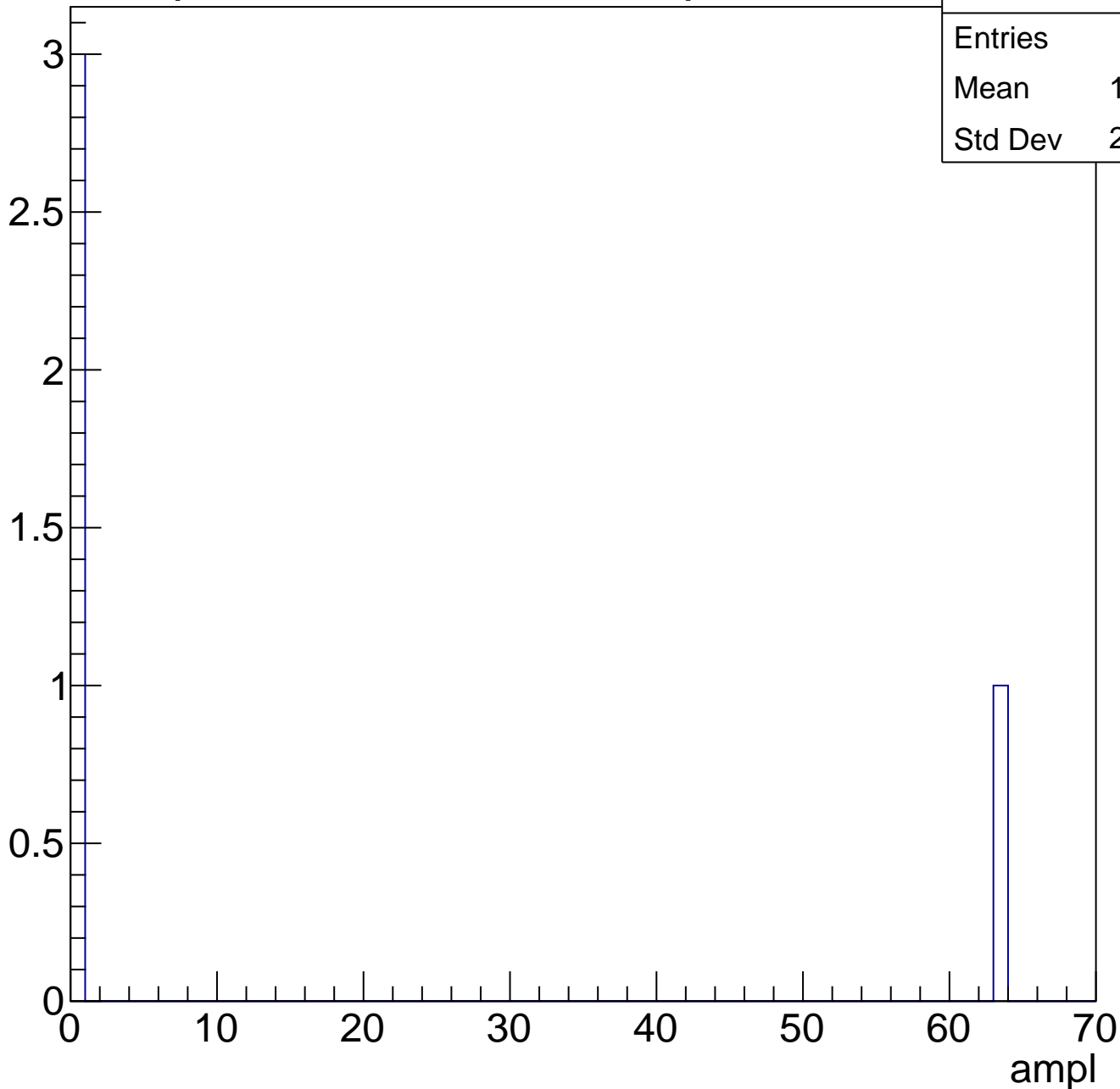




# B1L101S, U16-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch23, adc0

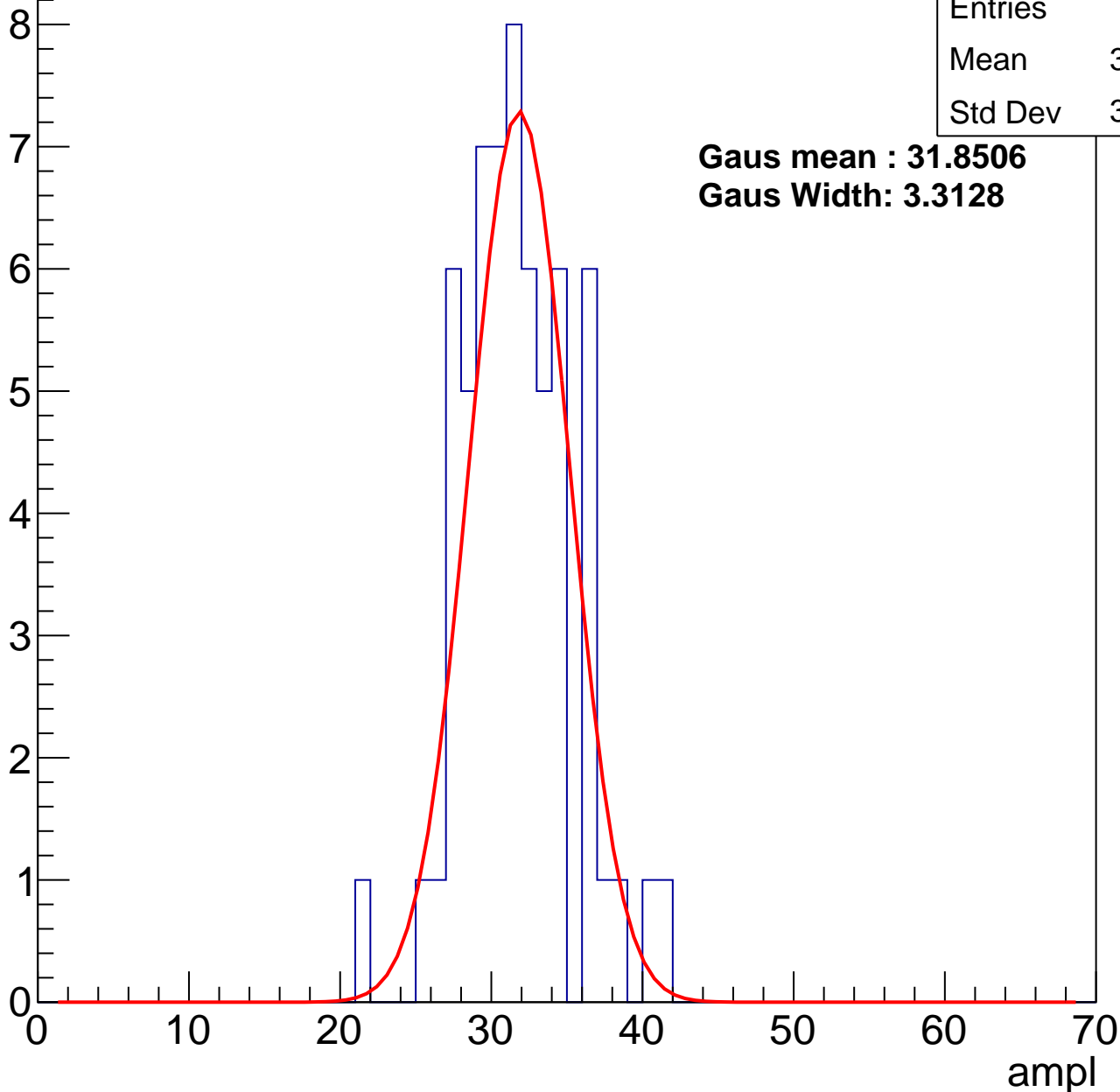
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	31.24
Std Dev	3.628

**Gaus mean : 31.8506**

**Gaus Width: 3.3128**



# B1L101S, U16-ch23, adc1

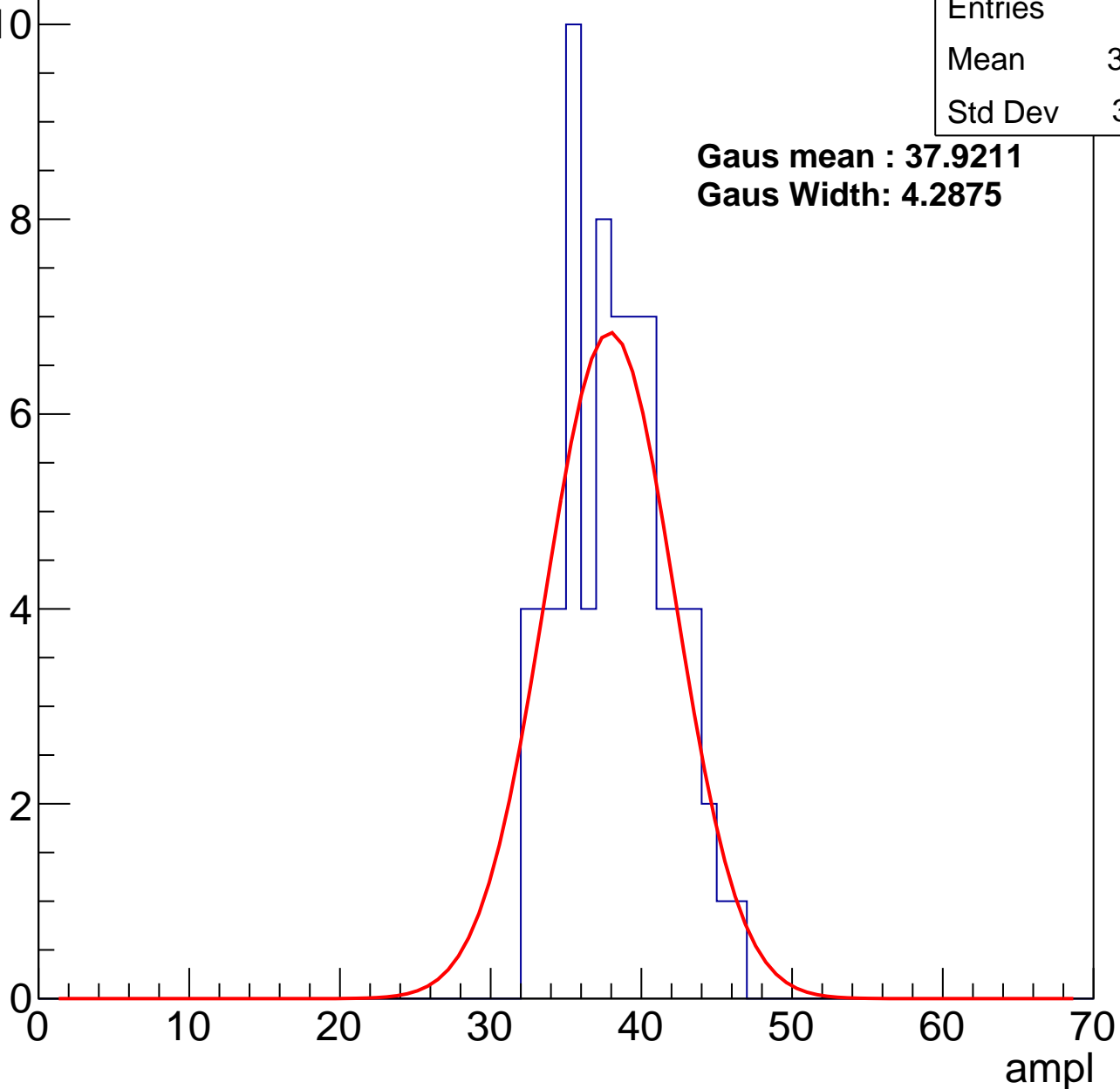
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	37.86
Std Dev	3.441

**Gaus mean : 37.9211**

**Gaus Width: 4.2875**



# B1L101S, U16-ch23, adc2

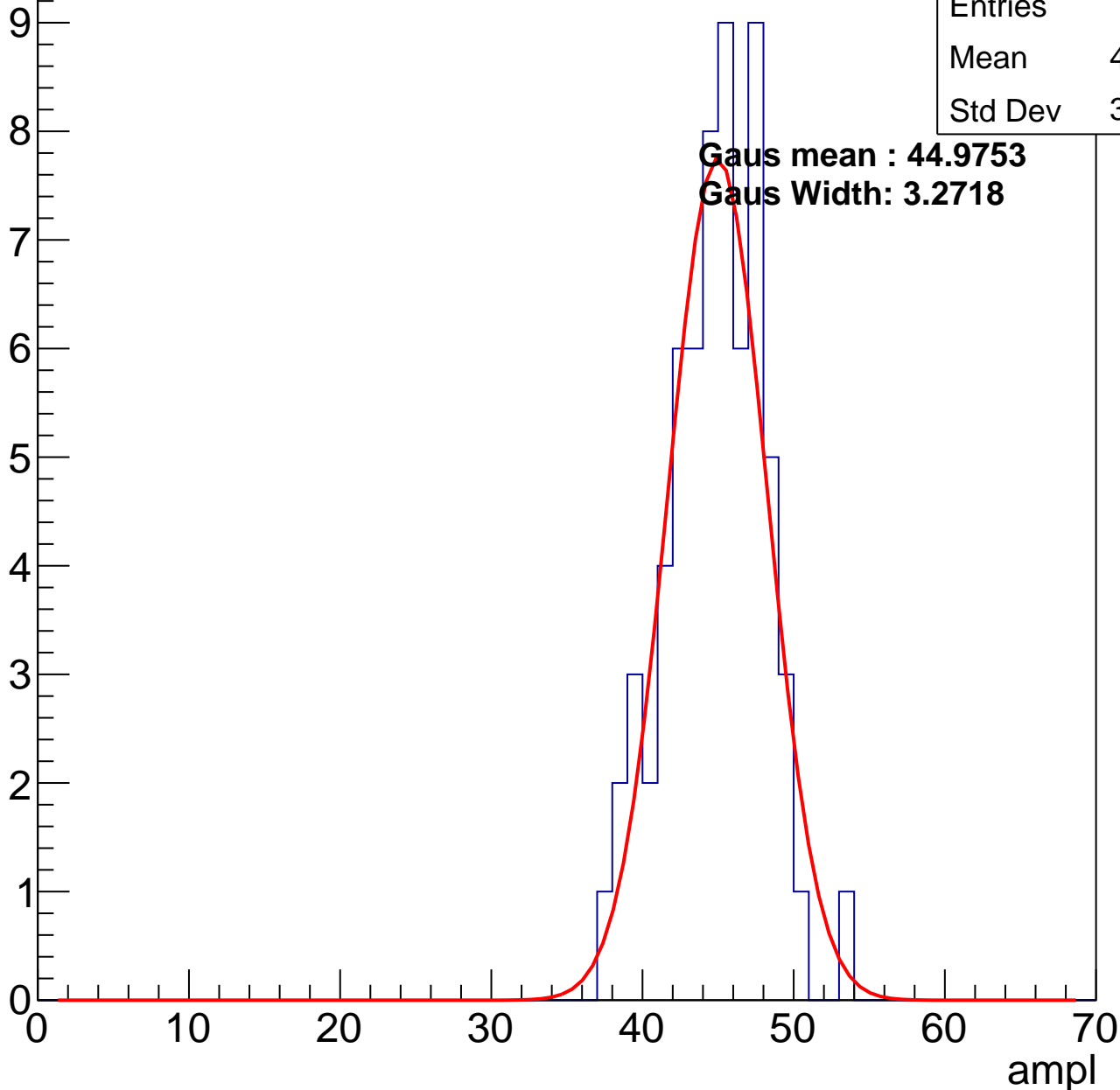
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	44.39
Std Dev	3.186

**Gaus mean : 44.9753**

**Gaus Width: 3.2718**

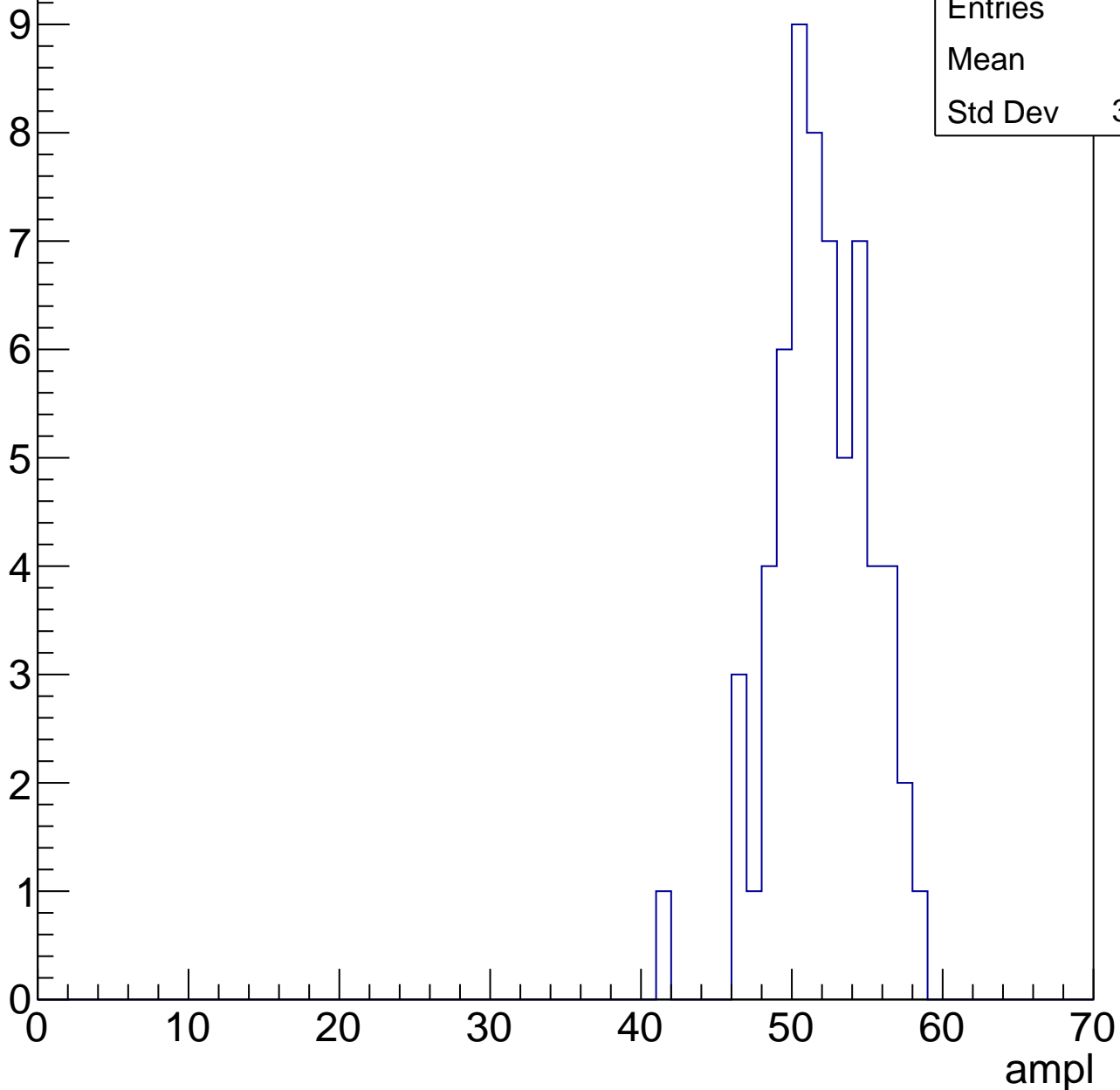


# B1L101S, U16-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	51.5
Std Dev	3.161



# B1L101S, U16-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

Entries

65

Mean

57.23

Std Dev

3.52

0

0

10

20

30

40

50

60

70

ampl

0

1

2

3

4

5

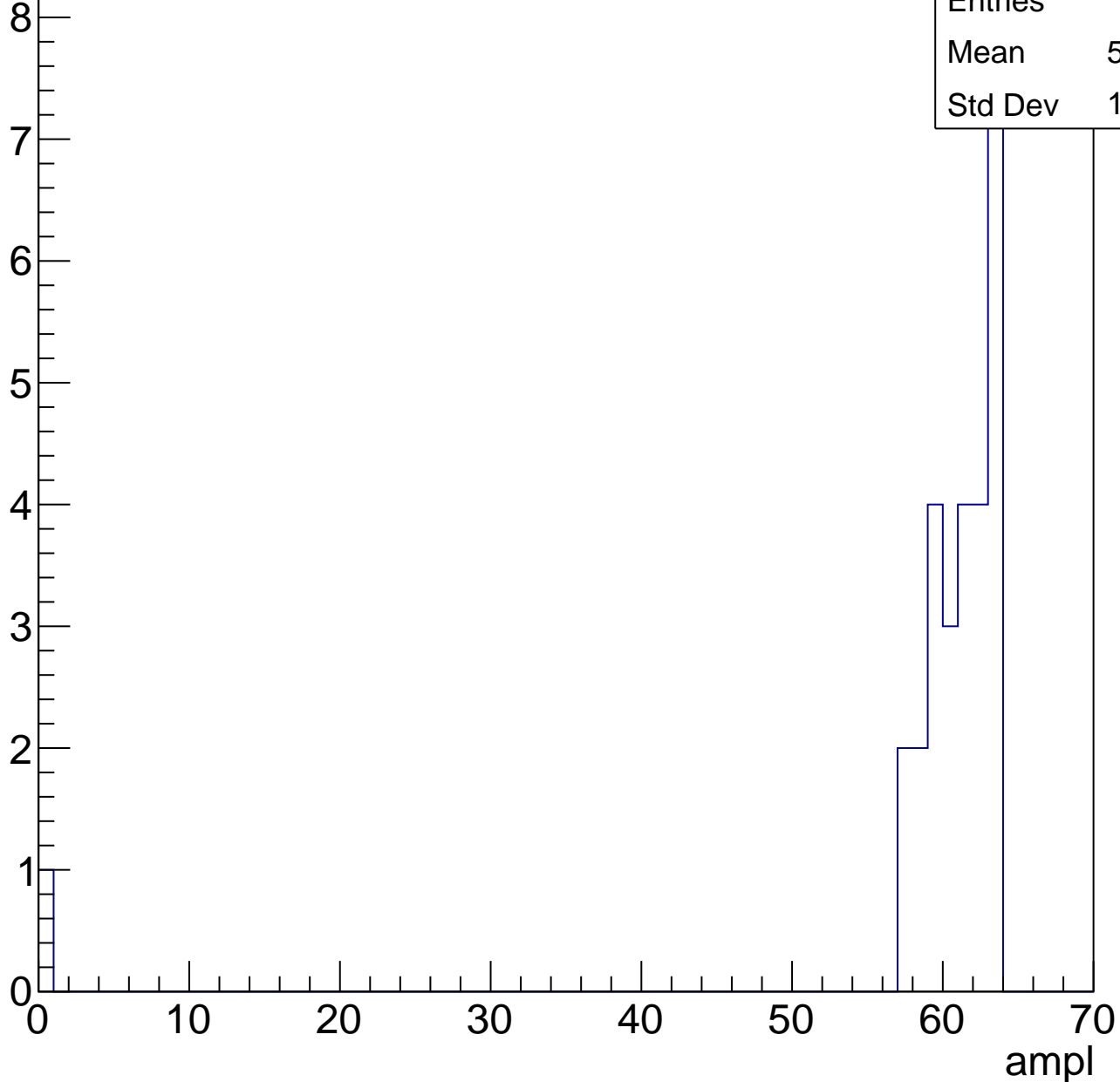
6

7

# B1L101S, U16-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

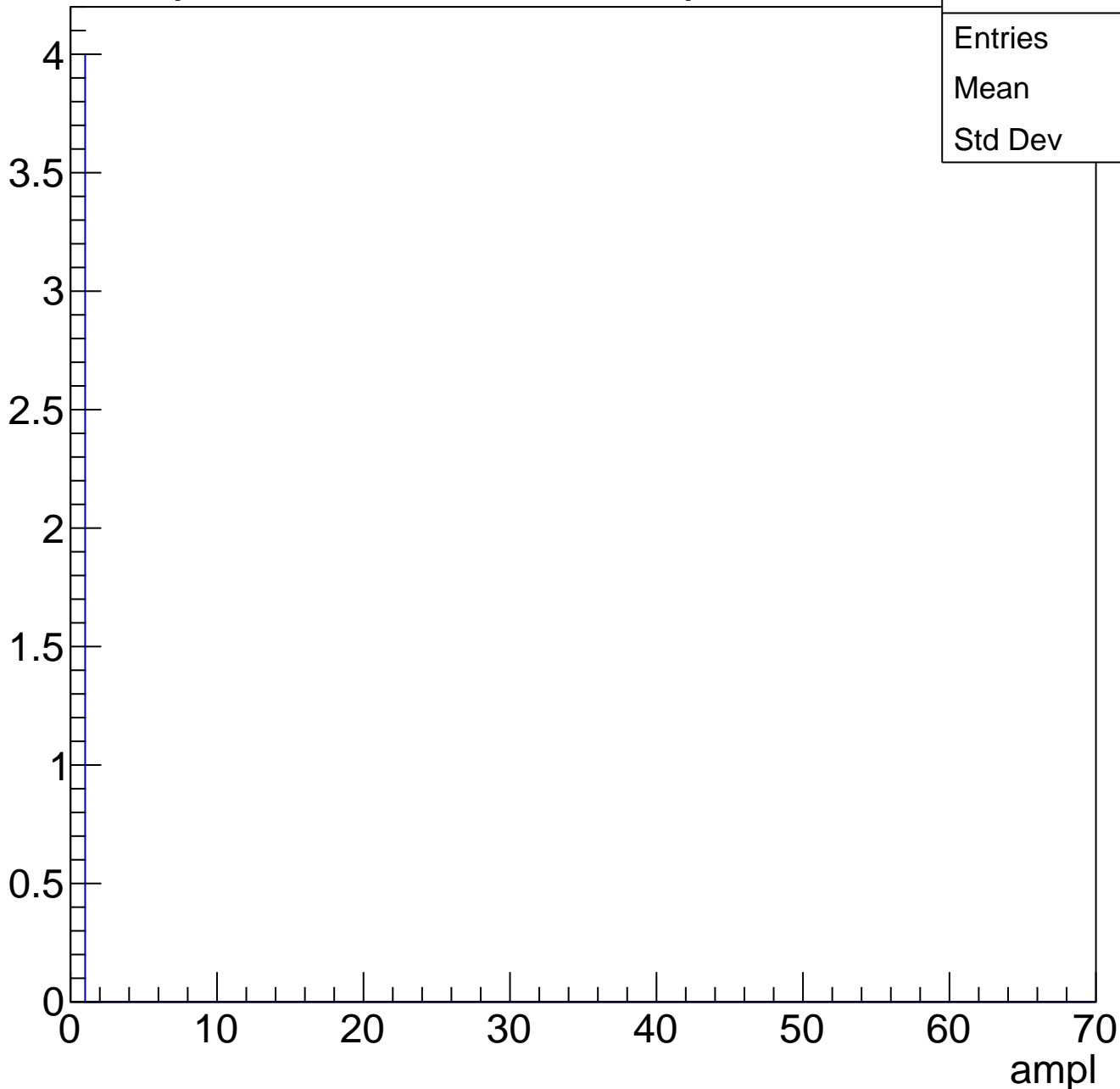




# B1L101S, U16-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	4
Mean	0
Std Dev	0

# B1L101S, U16-ch24, adc0

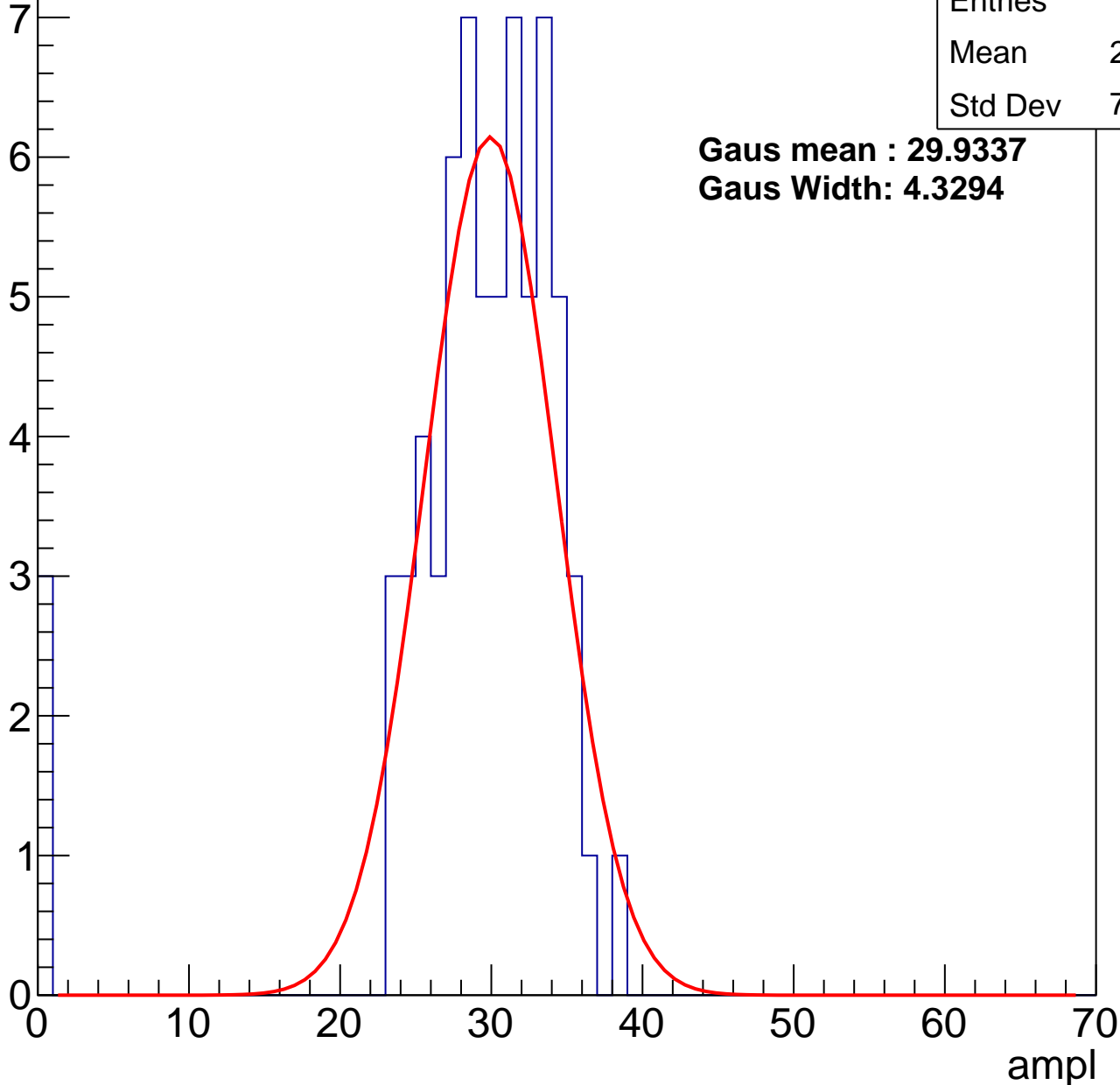
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	28.37
Std Dev	7.023

**Gaus mean : 29.9337**

**Gaus Width: 4.3294**



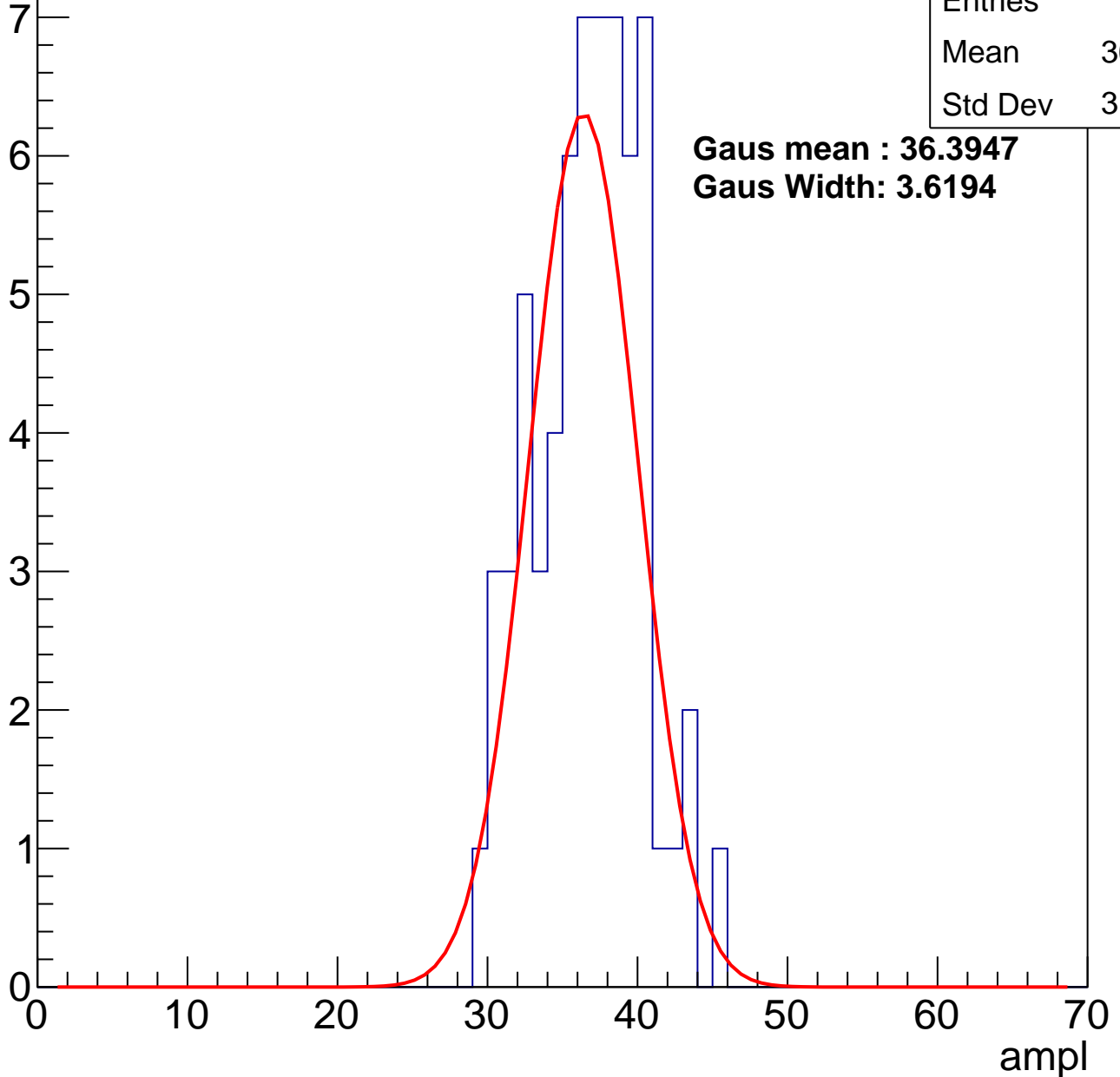
# B1L101S, U16-ch24, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	36.28
Std Dev	3.529

**Gaus mean : 36.3947**  
**Gaus Width: 3.6194**



# B1L101S, U16-ch24, adc2

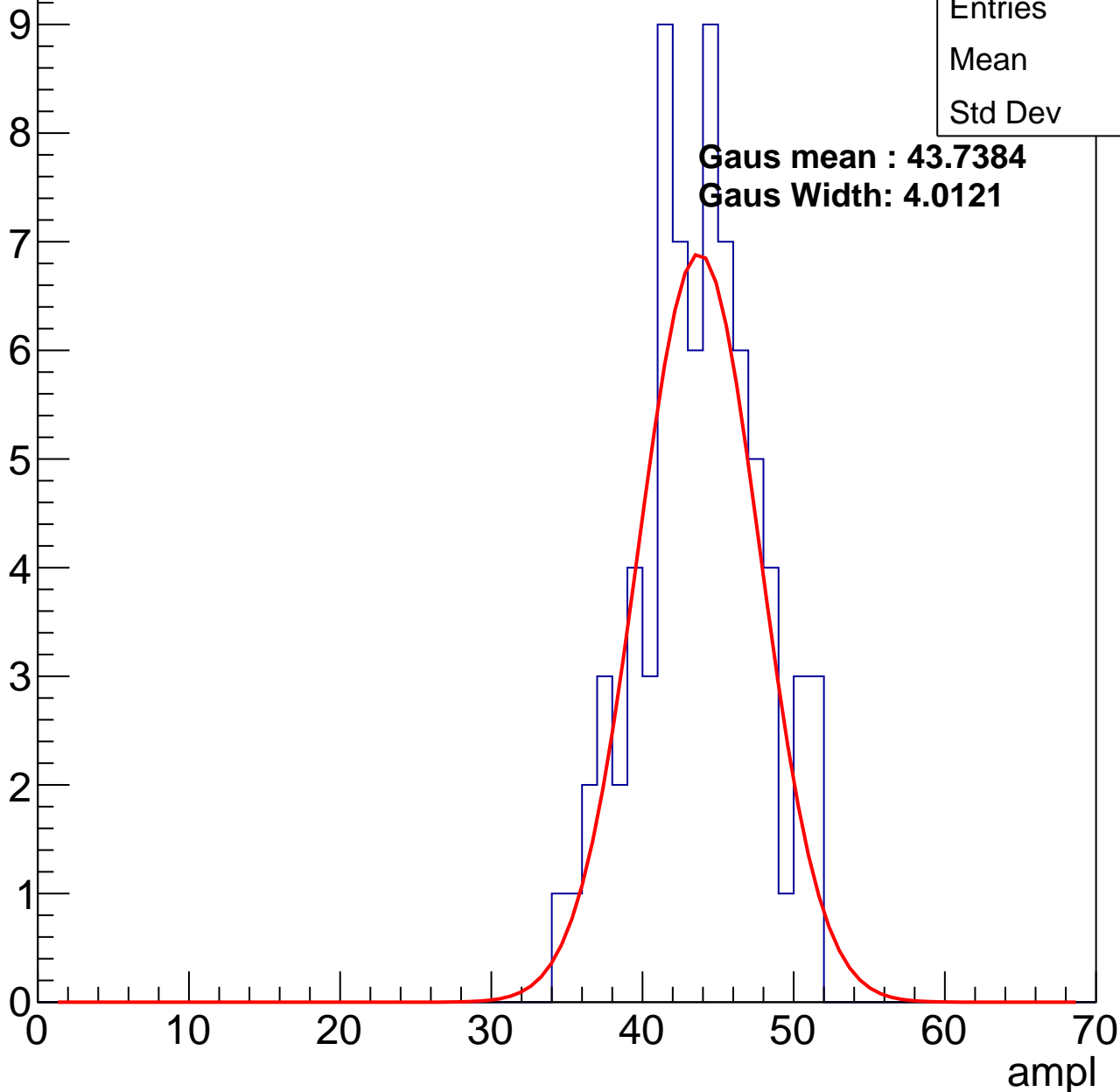
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	43.3
Std Dev	3.93

**Gaus mean : 43.7384**

**Gaus Width: 4.0121**

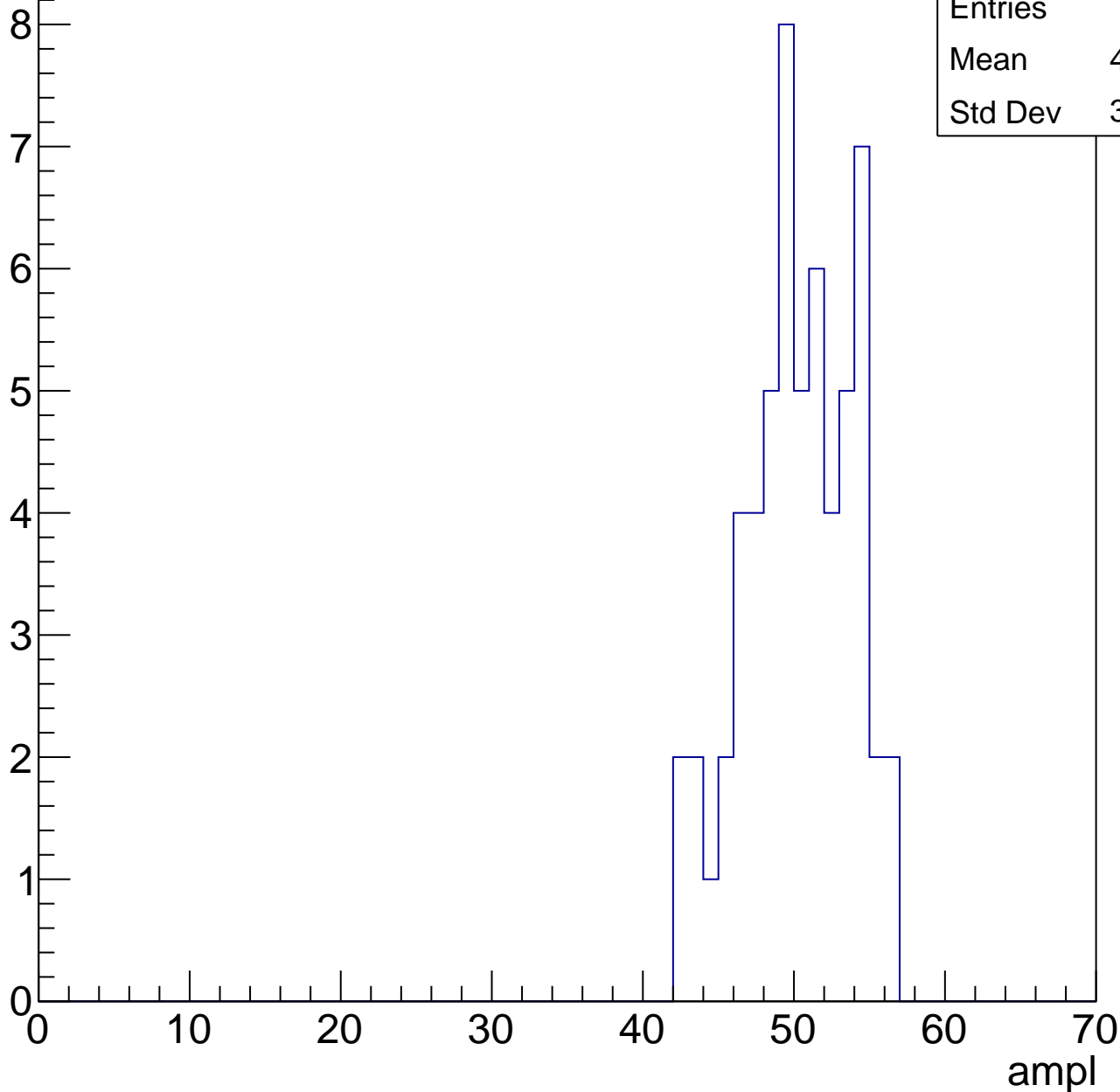


# B1L101S, U16-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	49.78
Std Dev	3.537

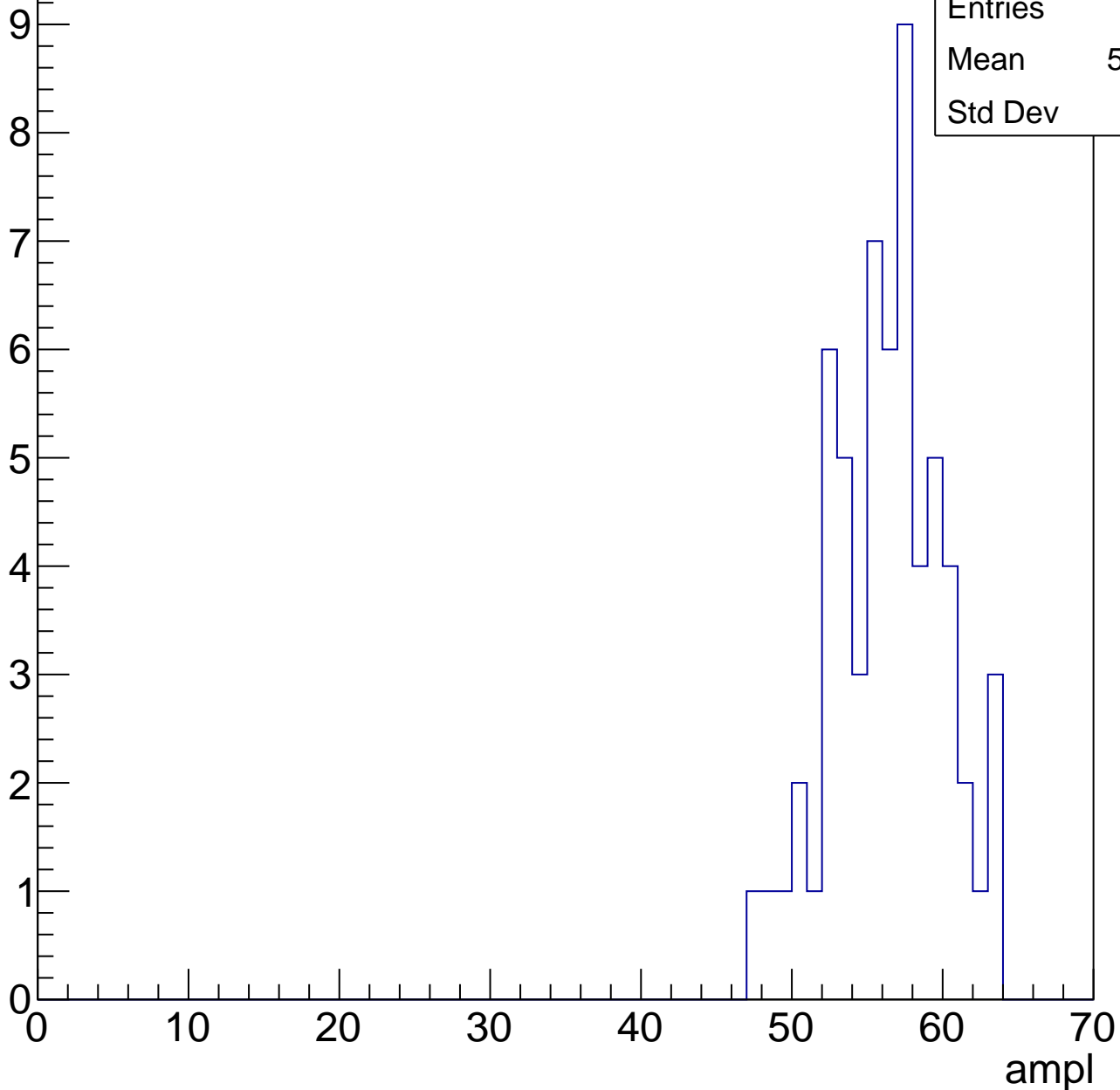


# B1L101S, U16-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	55.87
Std Dev	3.66

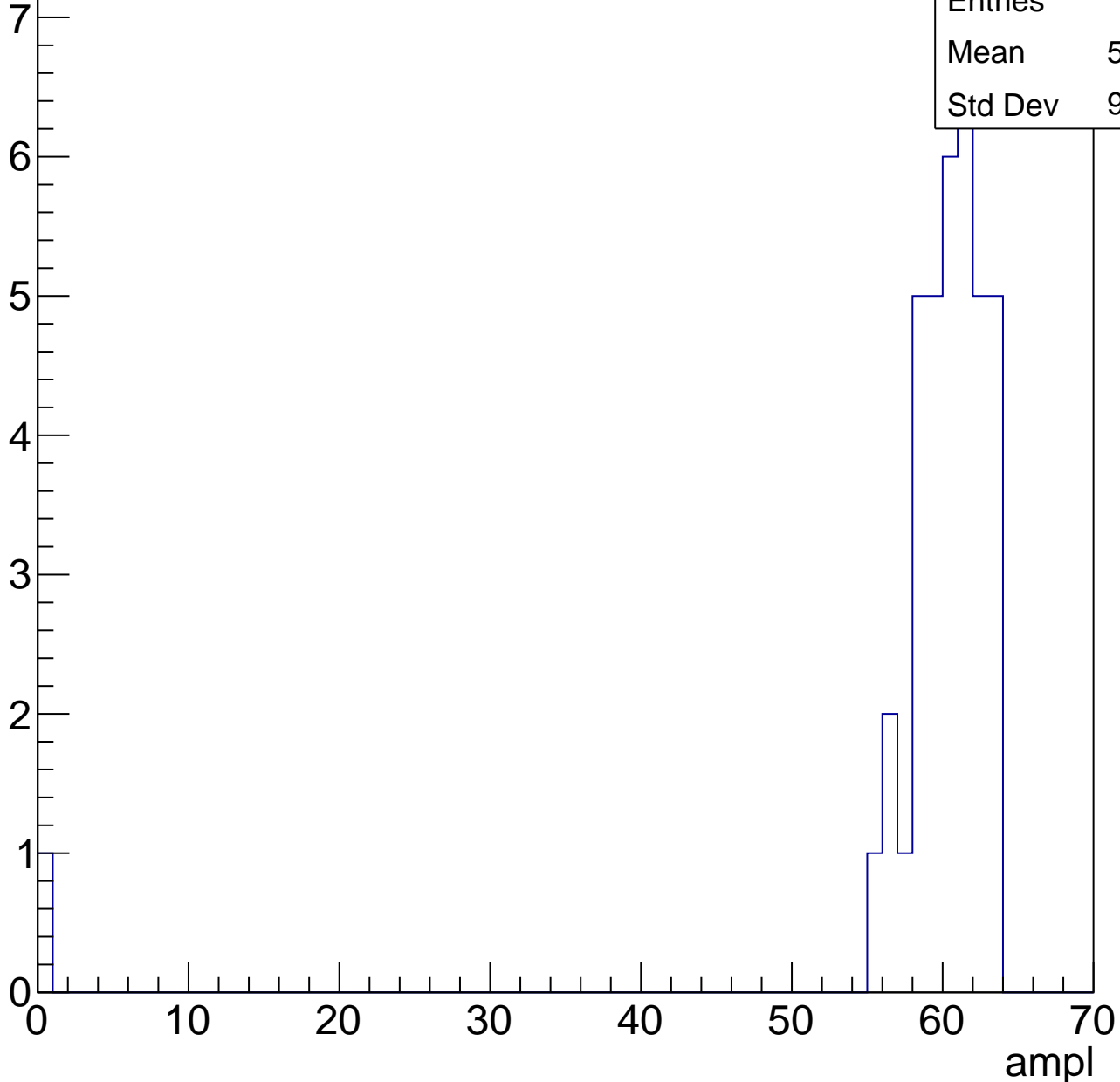


# B1L101S, U16-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

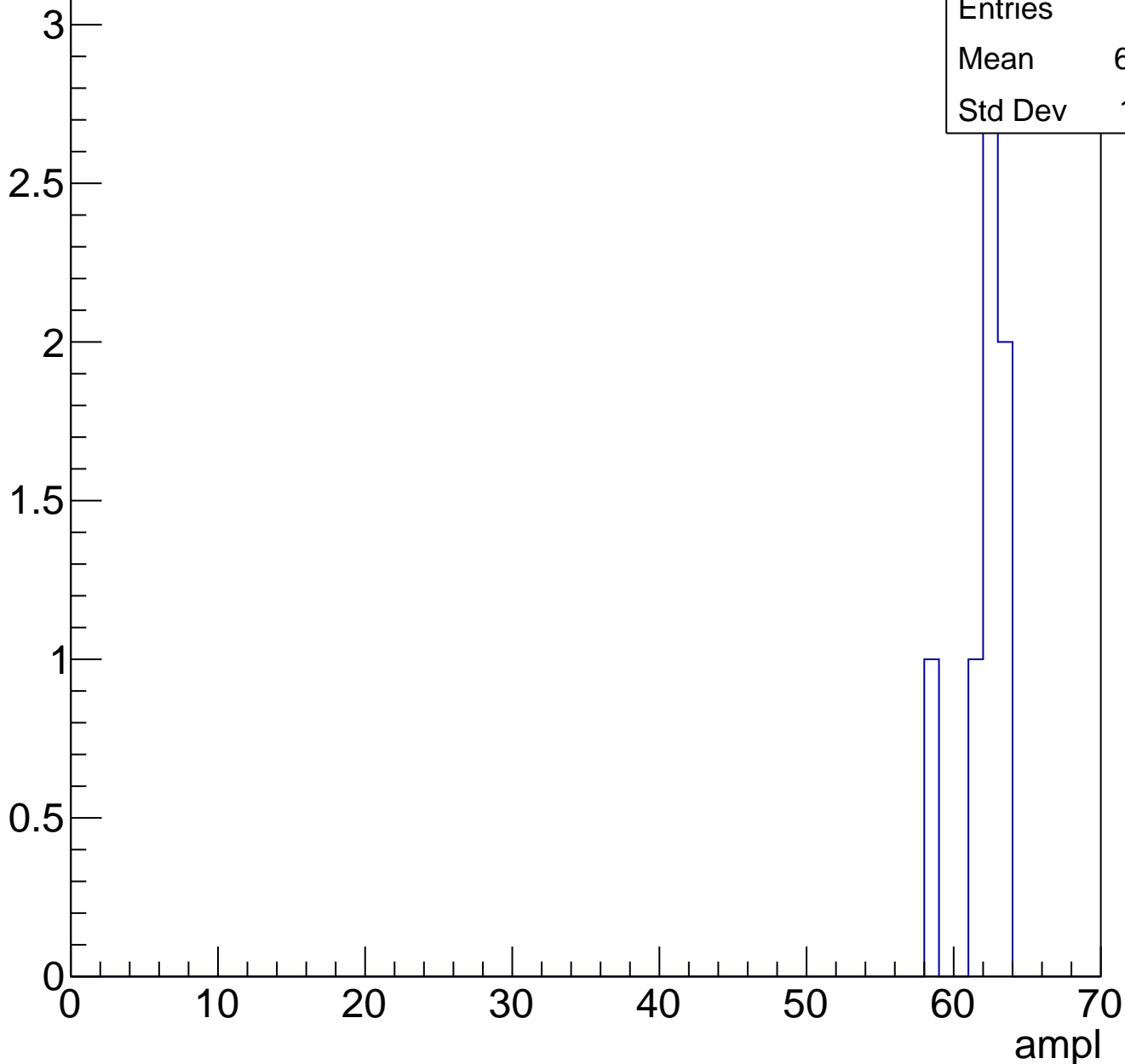
Entries	38
Mean	58.45
Std Dev	9.829



# B1L101S, U16-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch25, adc0

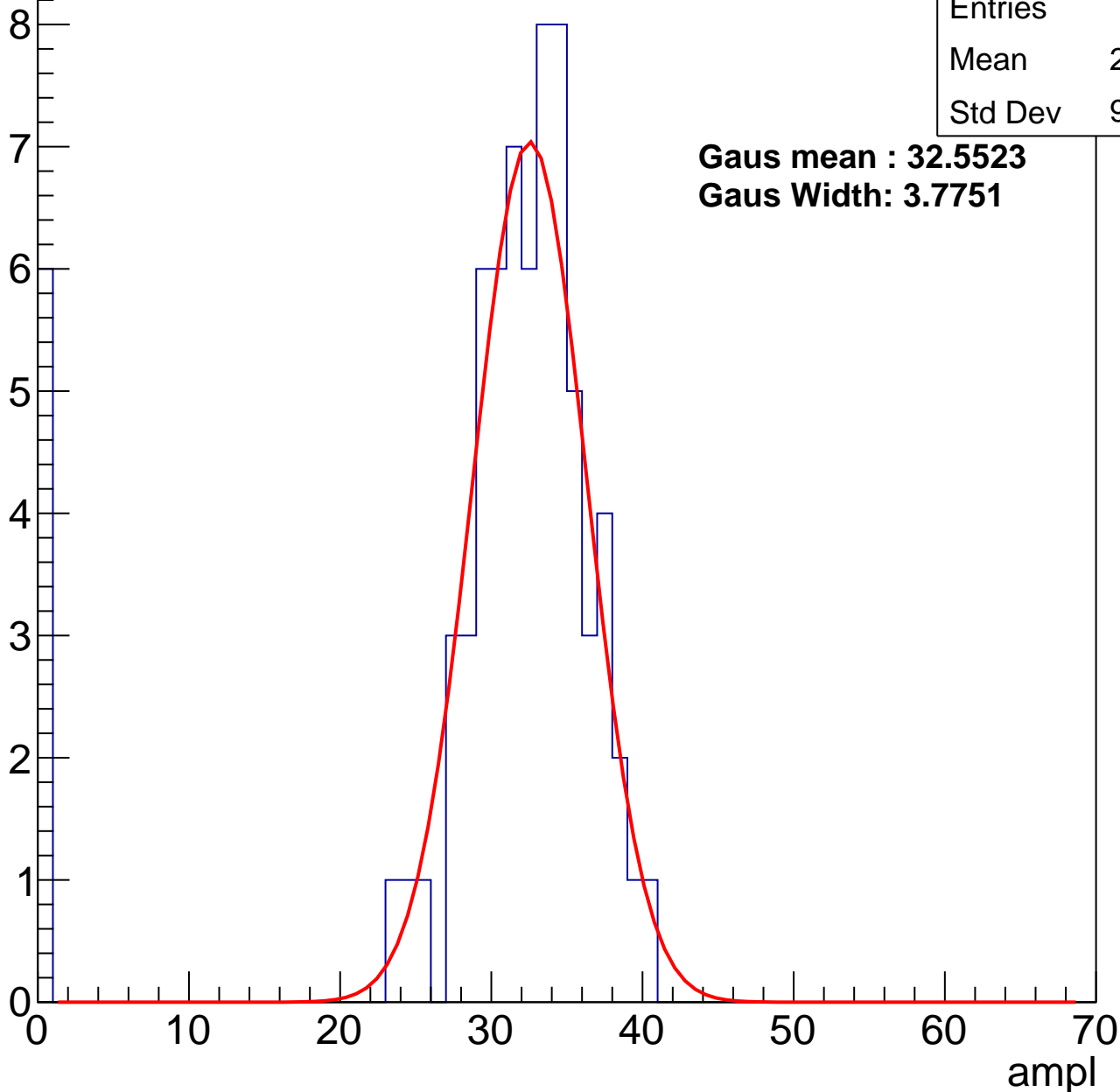
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	29.47
Std Dev	9.504

**Gaus mean : 32.5523**

**Gaus Width: 3.7751**



# B1L101S, U16-ch25, adc1

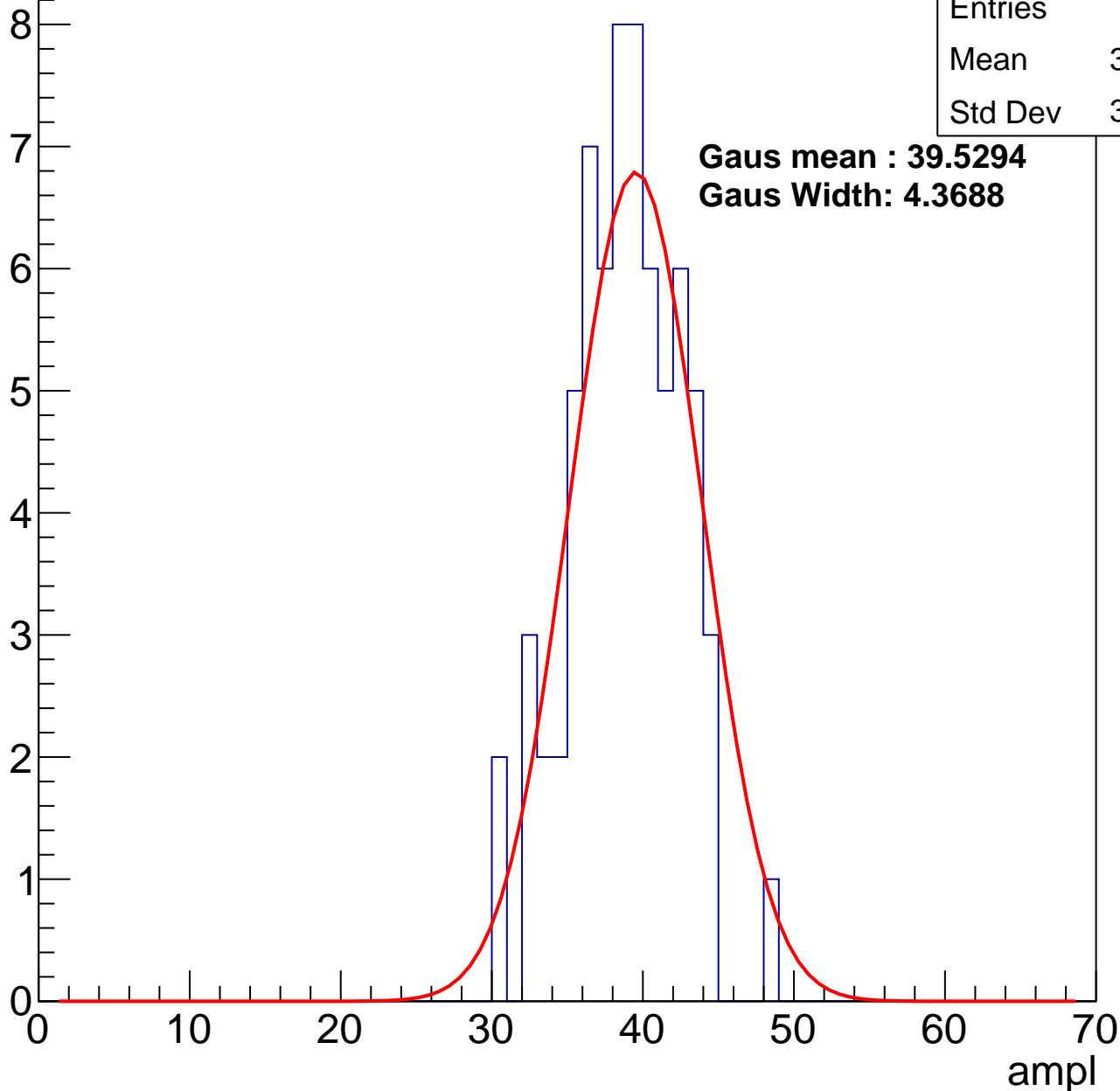
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	38.36
Std Dev	3.599

**Gaus mean : 39.5294**

**Gaus Width: 4.3688**



# B1L101S, U16-ch25, adc2

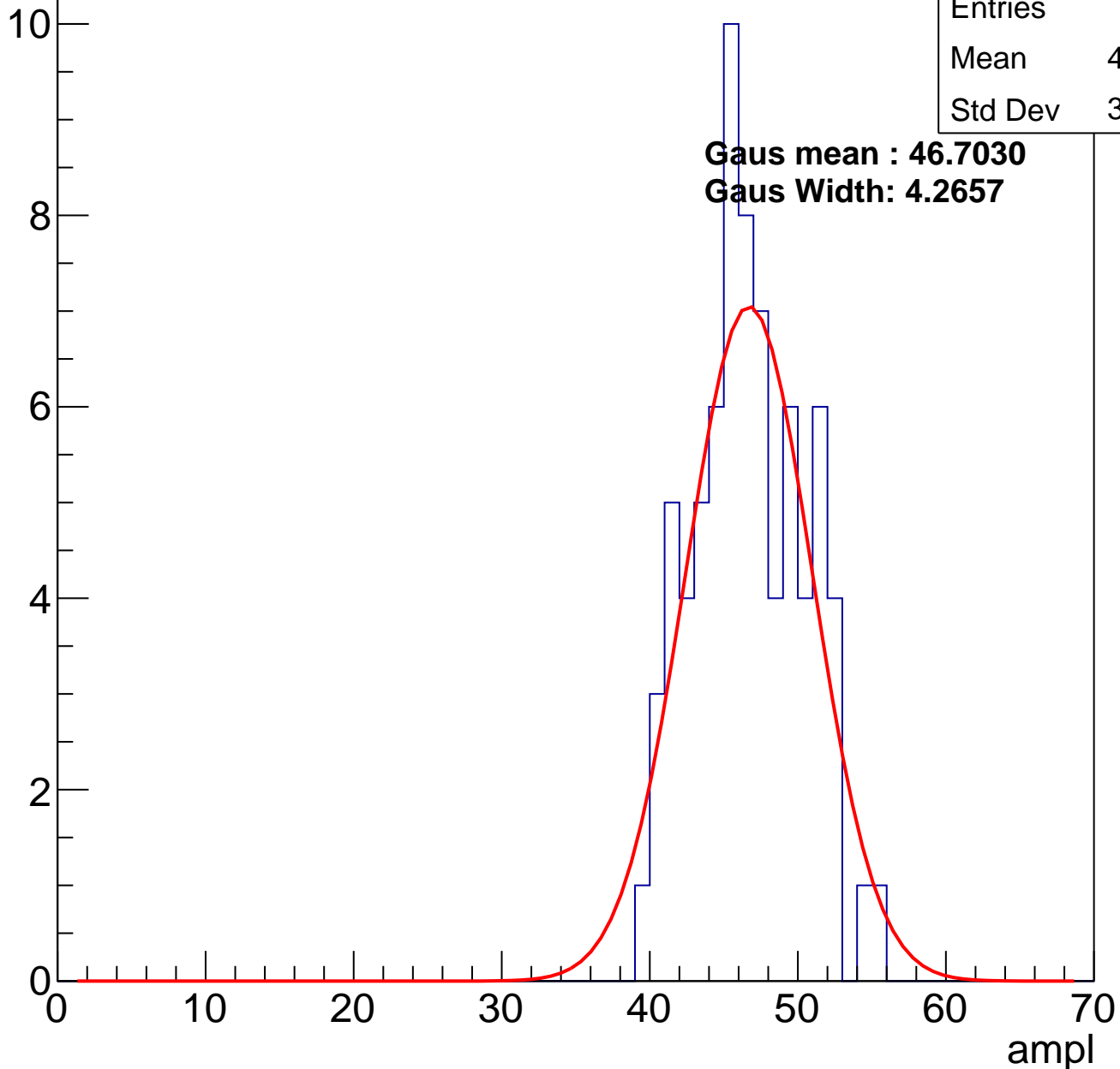
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	75
Mean	46.23
Std Dev	3.654

**Gaus mean : 46.7030**

**Gaus Width: 4.2657**

Entry

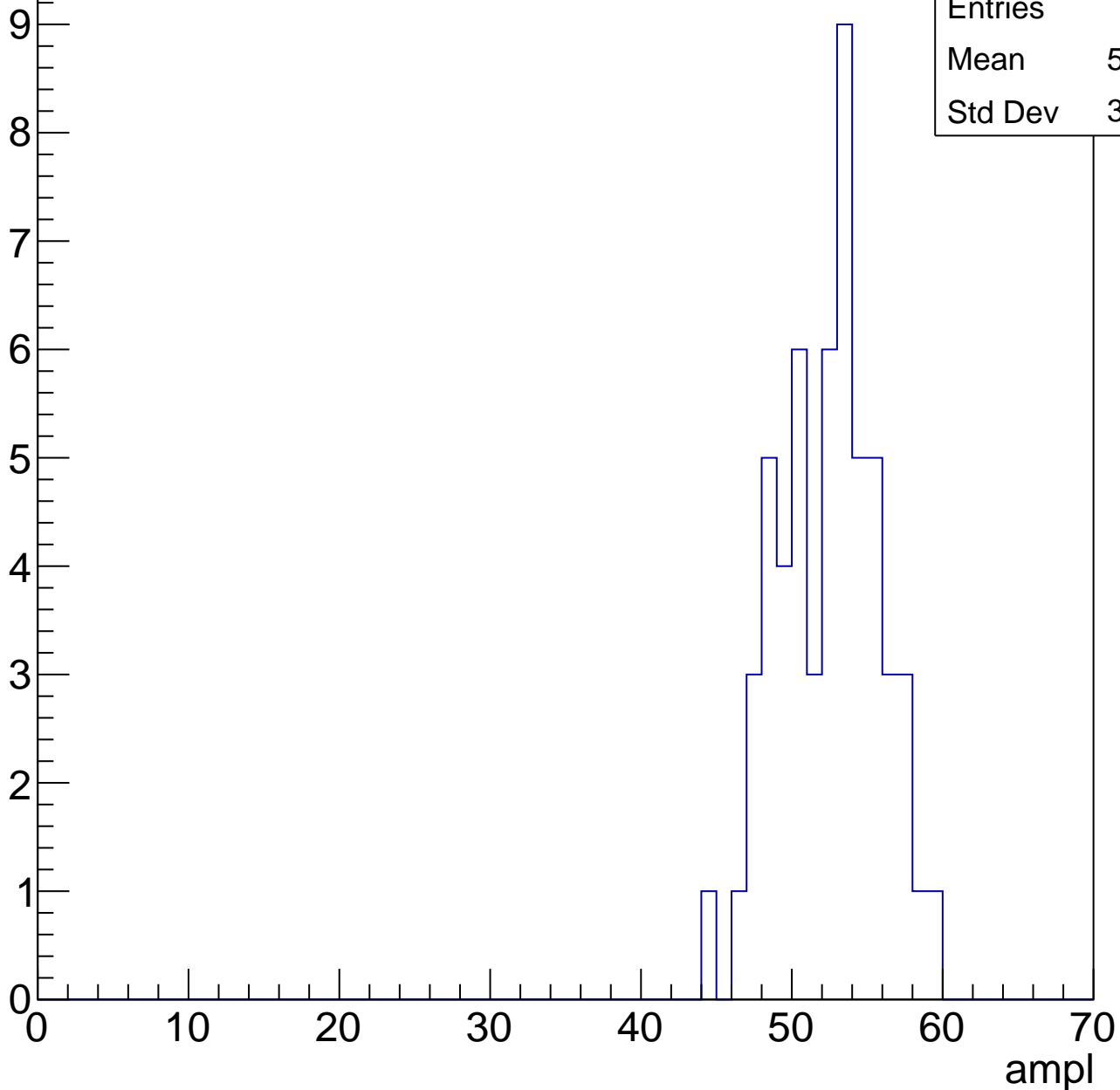


# B1L101S, U16-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	51.96
Std Dev	3.273

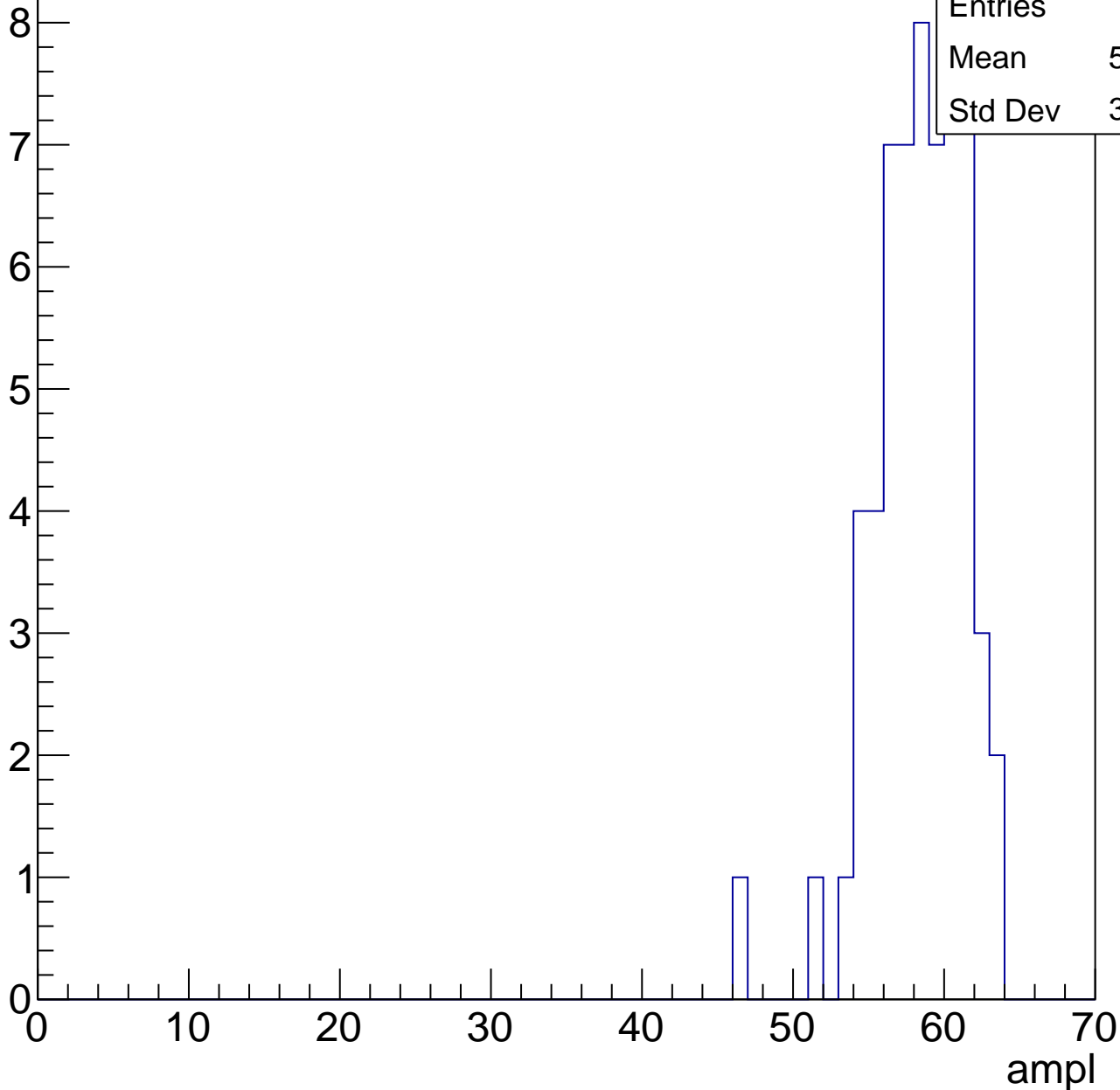


# B1L101S, U16-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	57.93
Std Dev	3.035

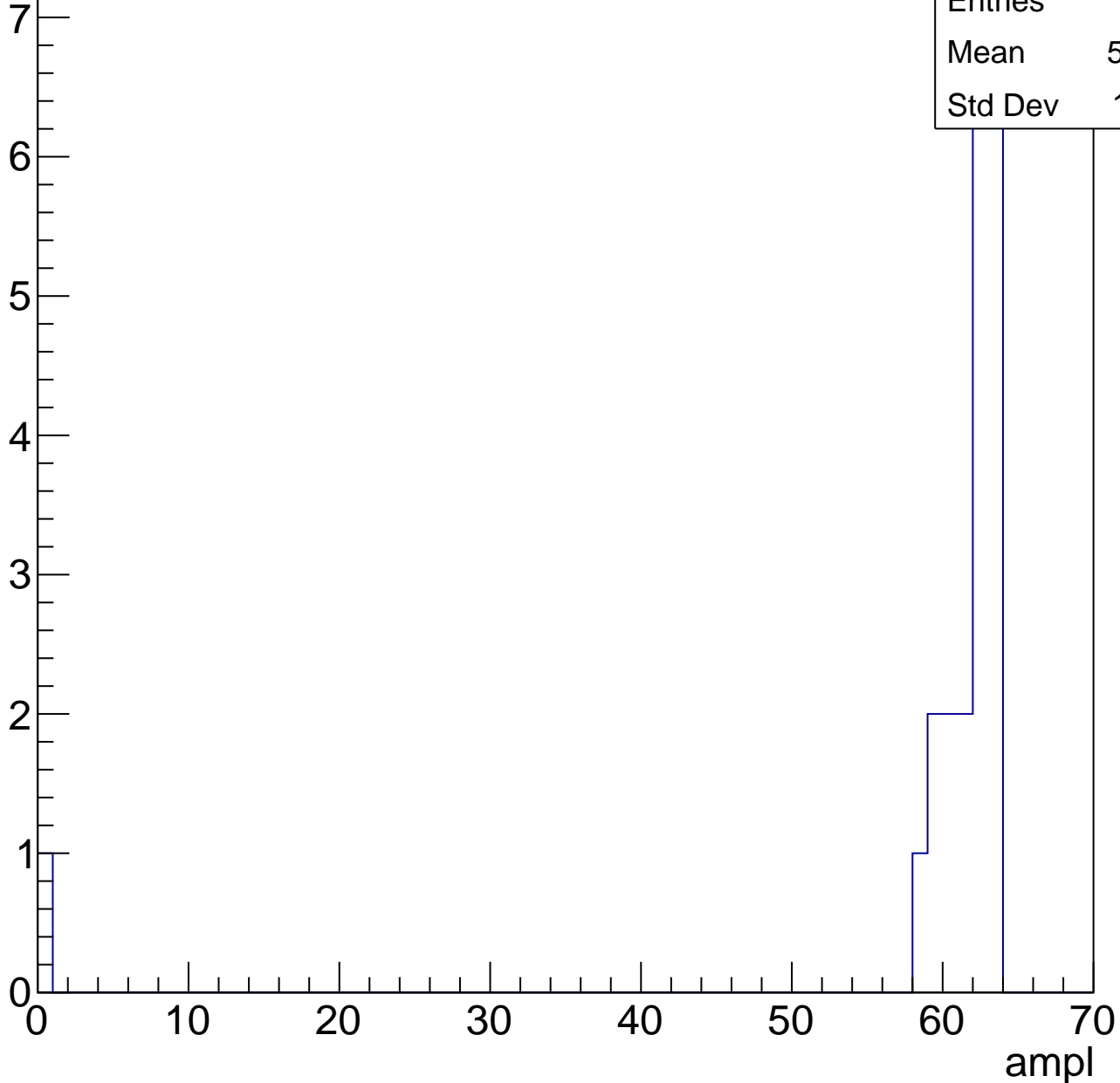


# B1L101S, U16-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	22
Mean	58.77
Std Dev	12.91



# B1L101S, U16-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U16-ch26, adc0

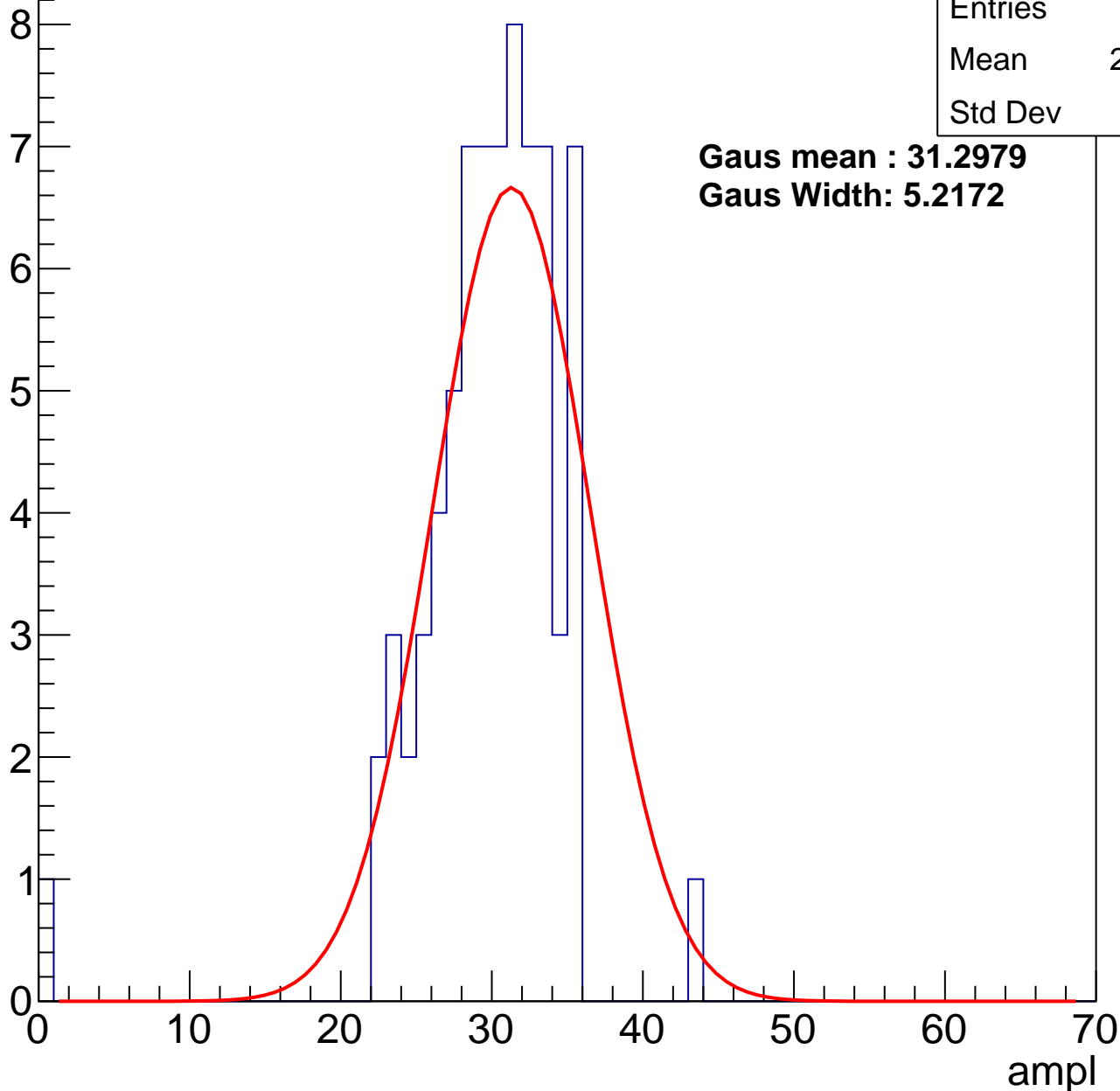
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	29.42
Std Dev	5.11

**Gaus mean : 31.2979**

**Gaus Width: 5.2172**



# B1L101S, U16-ch26, adc1

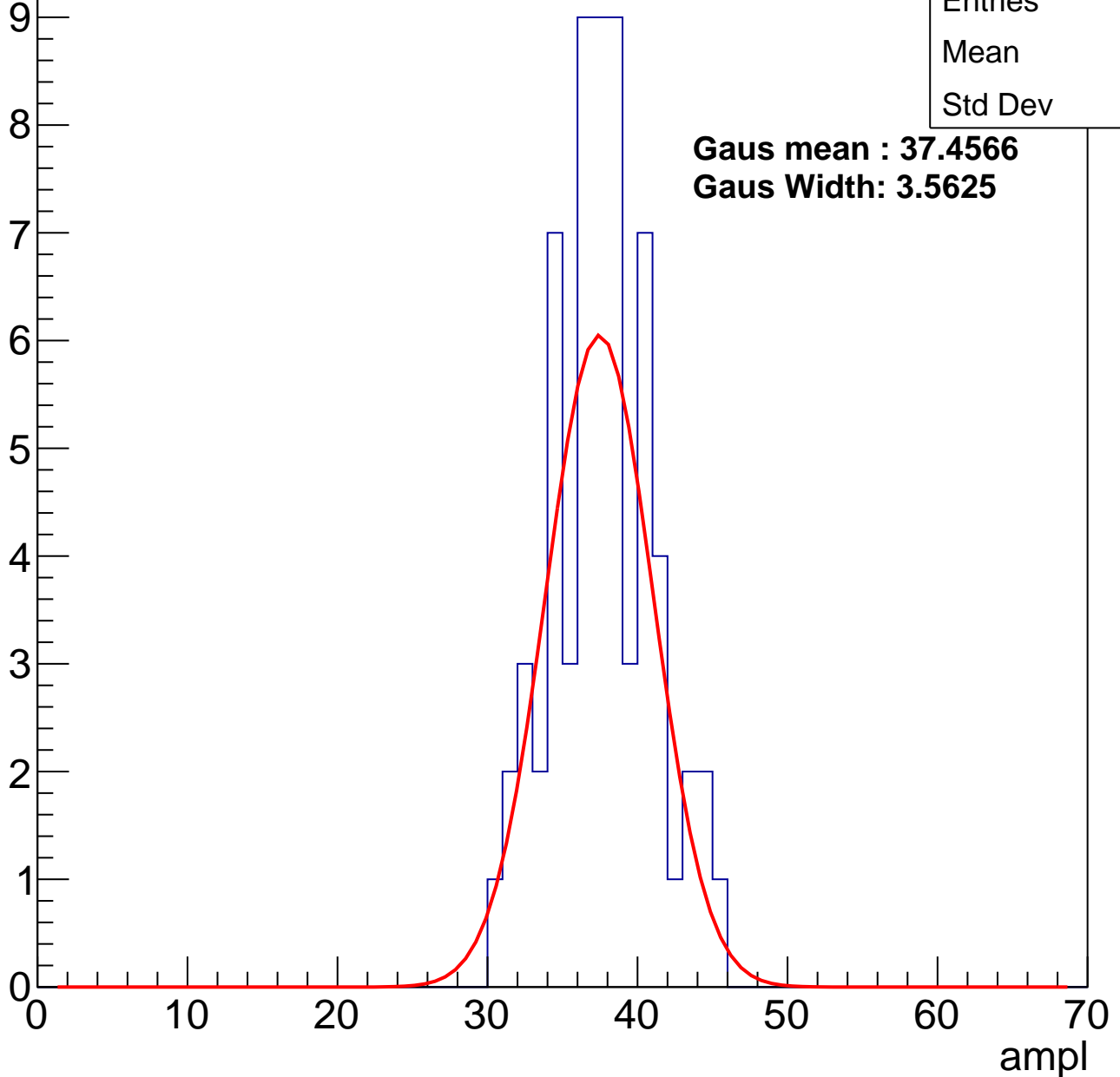
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	37.2
Std Dev	3.32

**Gaus mean : 37.4566**

**Gaus Width: 3.5625**



# B1L101S, U16-ch26, adc2

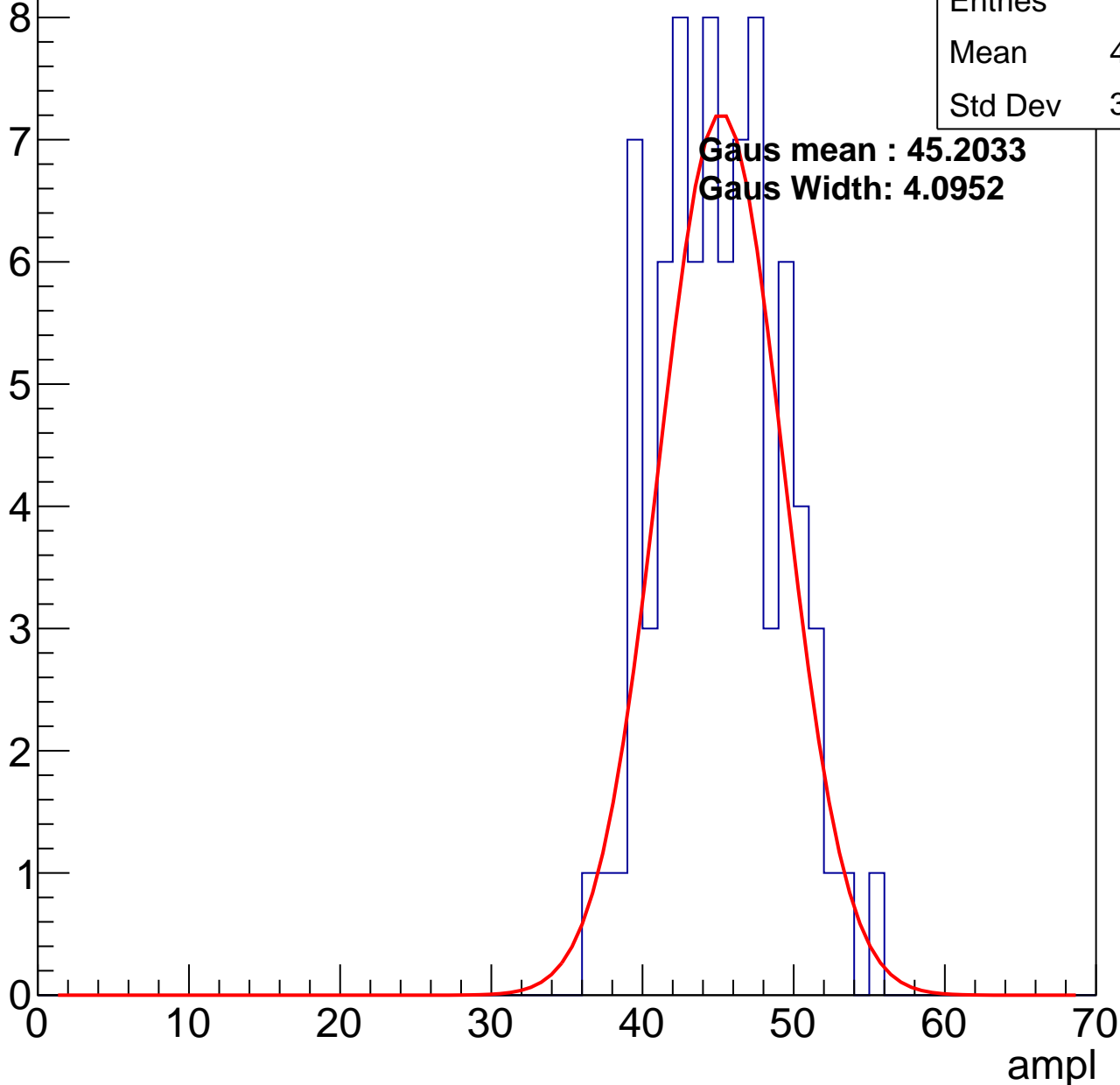
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	44.63
Std Dev	3.995

**Gaus mean : 45.2033**

**Gaus Width: 4.0952**

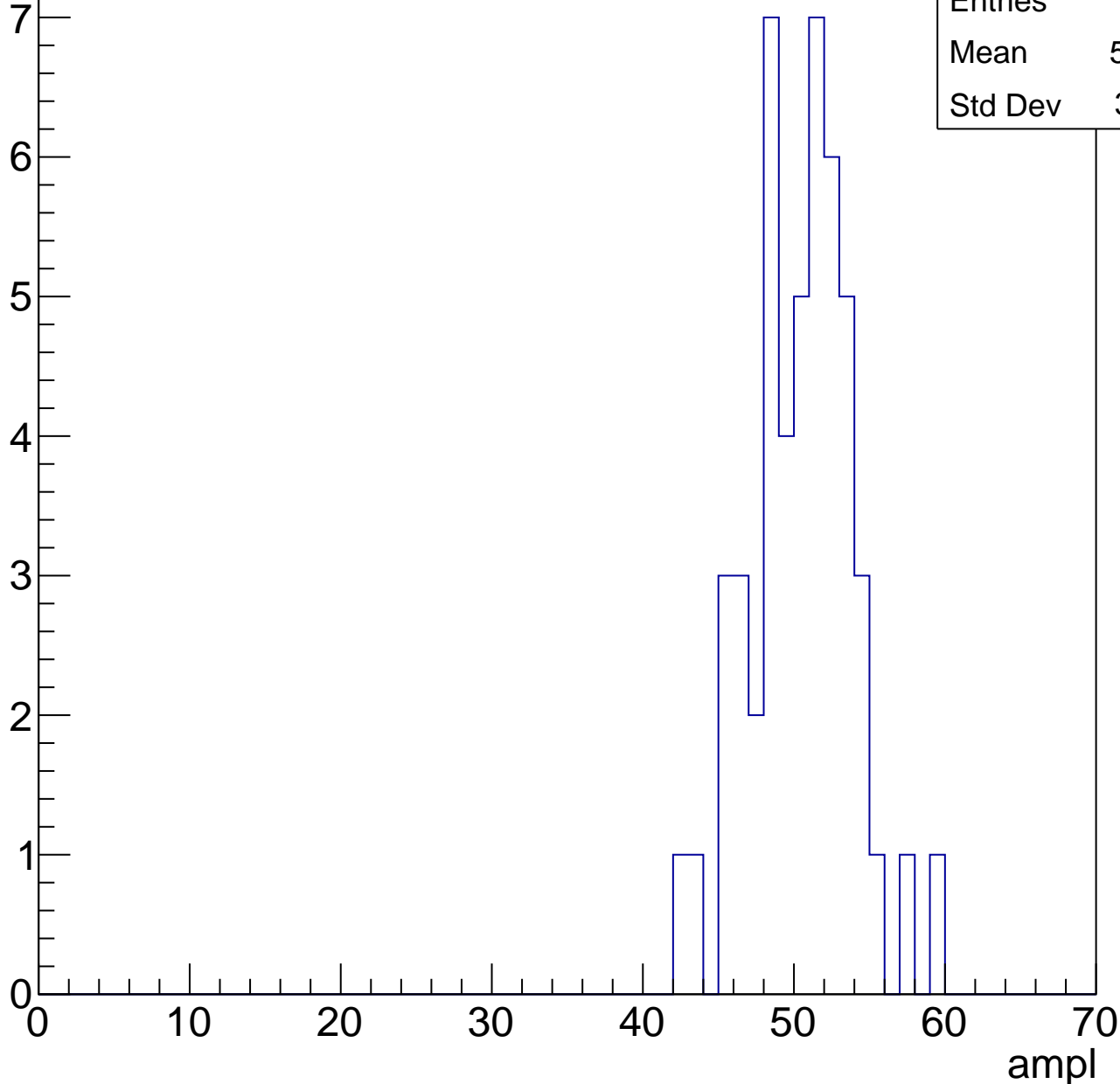


# B1L101S, U16-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	50.02
Std Dev	3.361

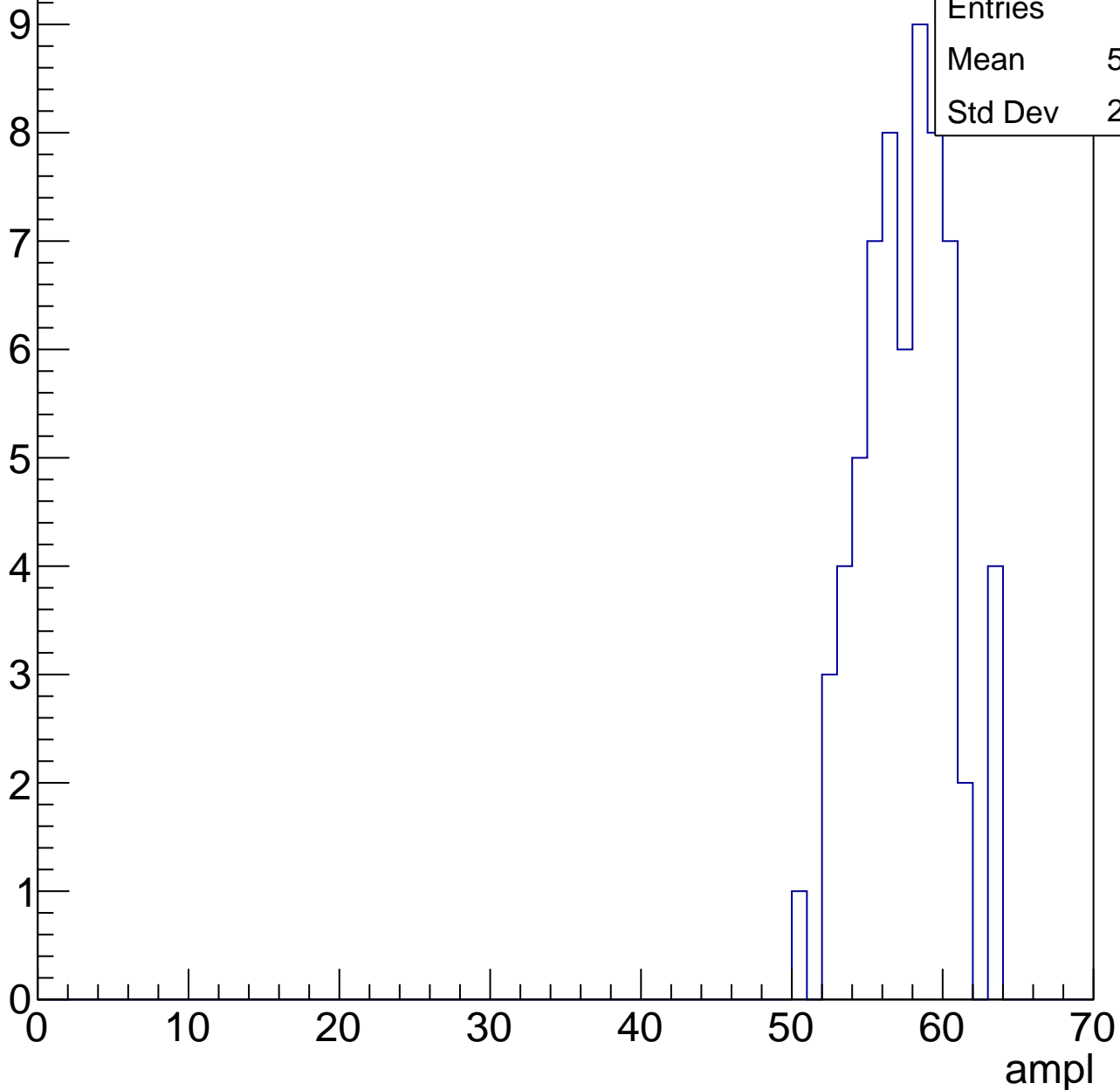


# B1L101S, U16-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	57.05
Std Dev	2.928



# B1L101S, U16-ch26, adc5

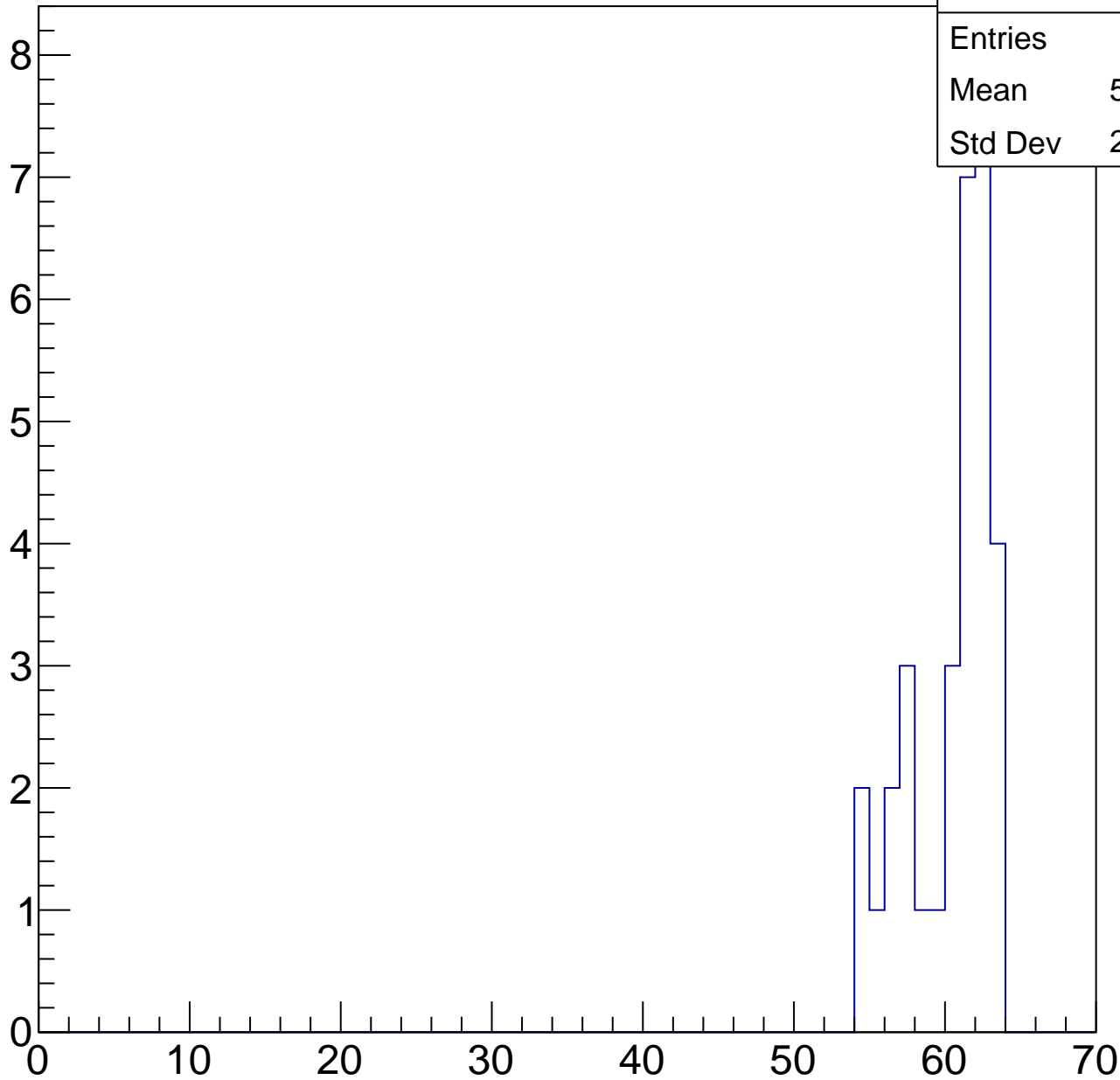
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	32
Mean	59.94
Std Dev	2.715

ampl



# B1L101S, U16-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	6
Mean	51.83
Std Dev	23.19



# B1L101S, U16-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U16-ch27, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	64
Mean	30.45
Std Dev	3.34

**Gaus mean : 30.7373**

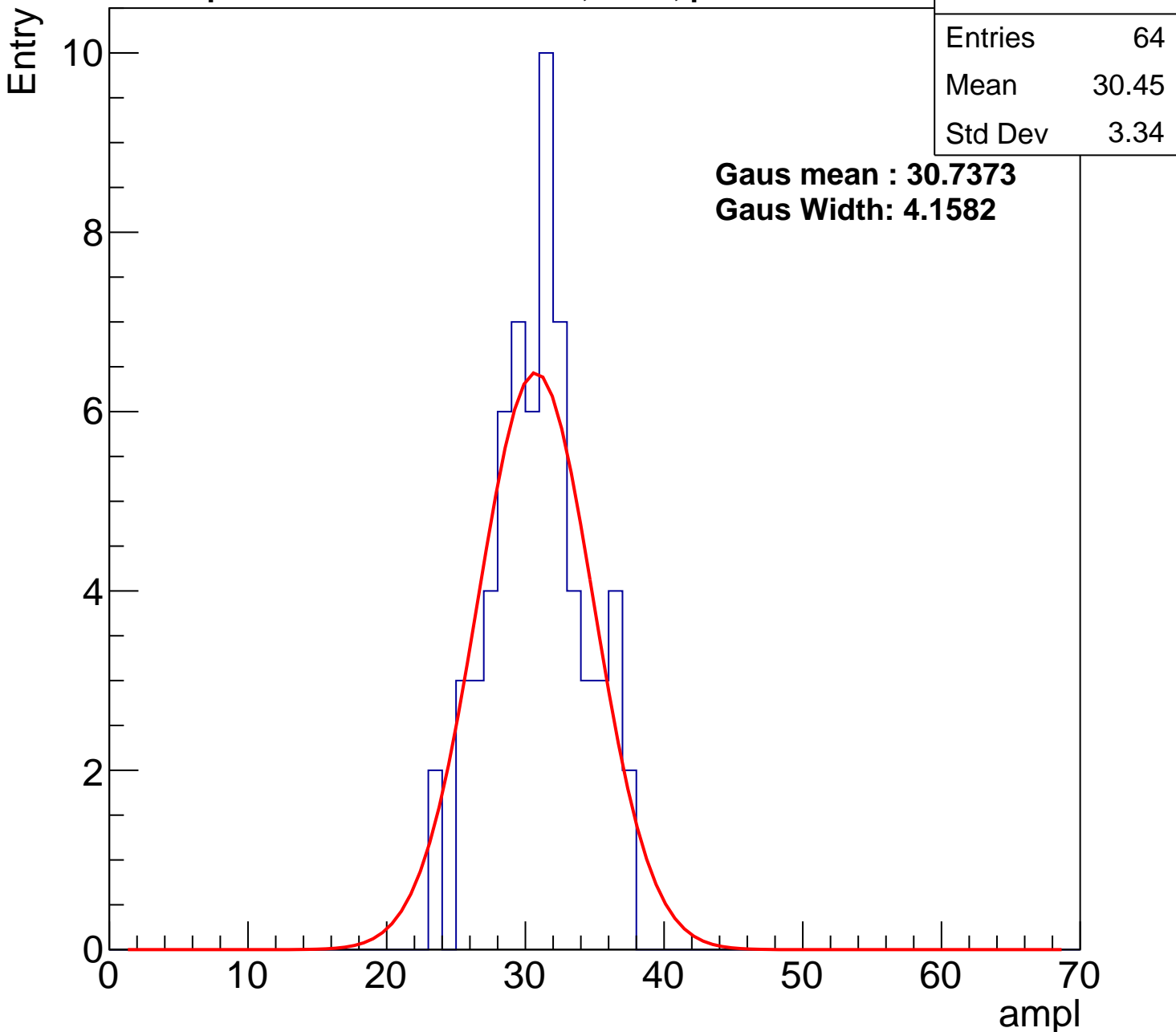
**Gaus Width: 4.1582**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch27, adc1

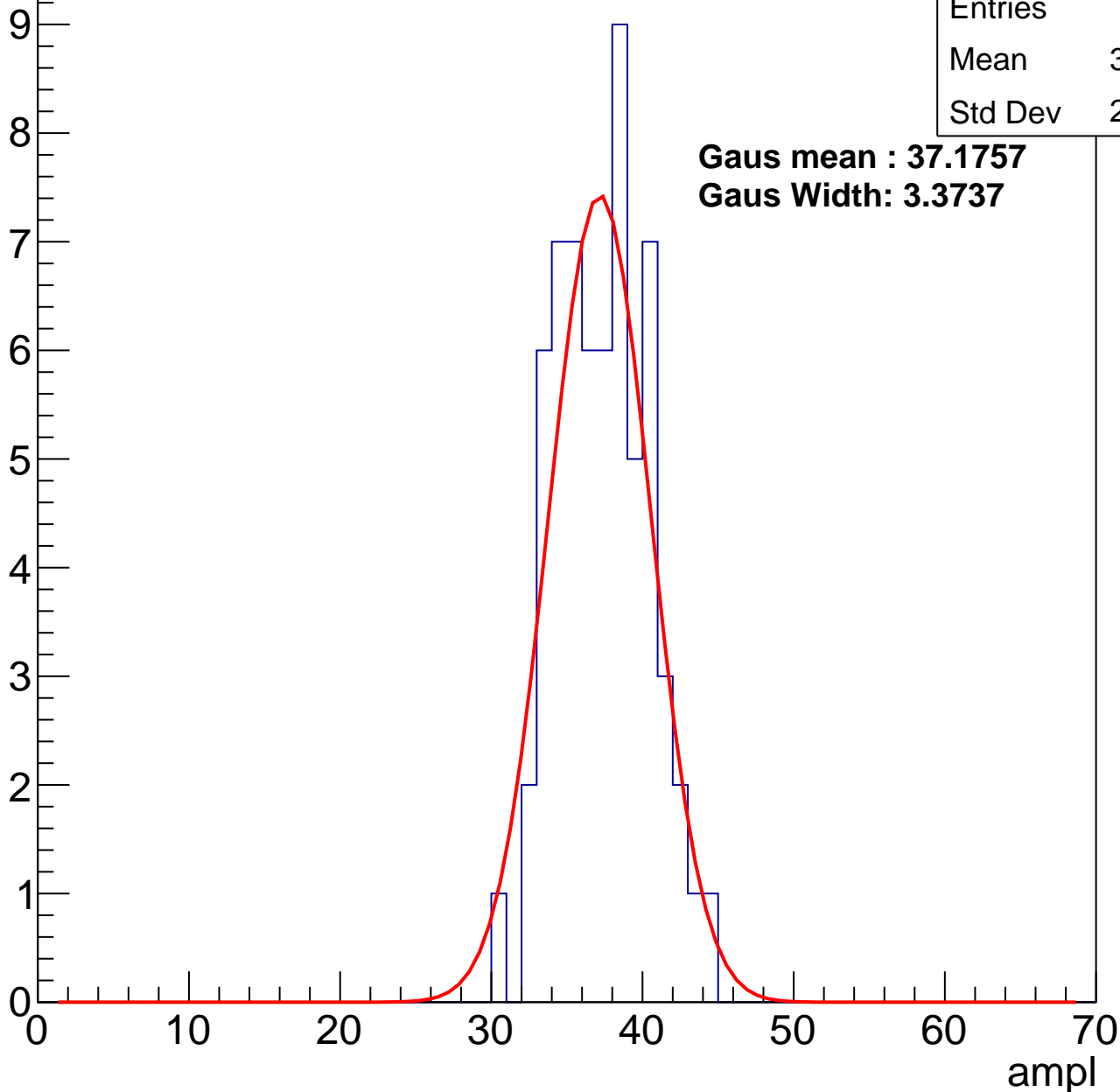
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	36.89
Std Dev	2.998

**Gaus mean : 37.1757**

**Gaus Width: 3.3737**



# B1L101S, U16-ch27, adc2

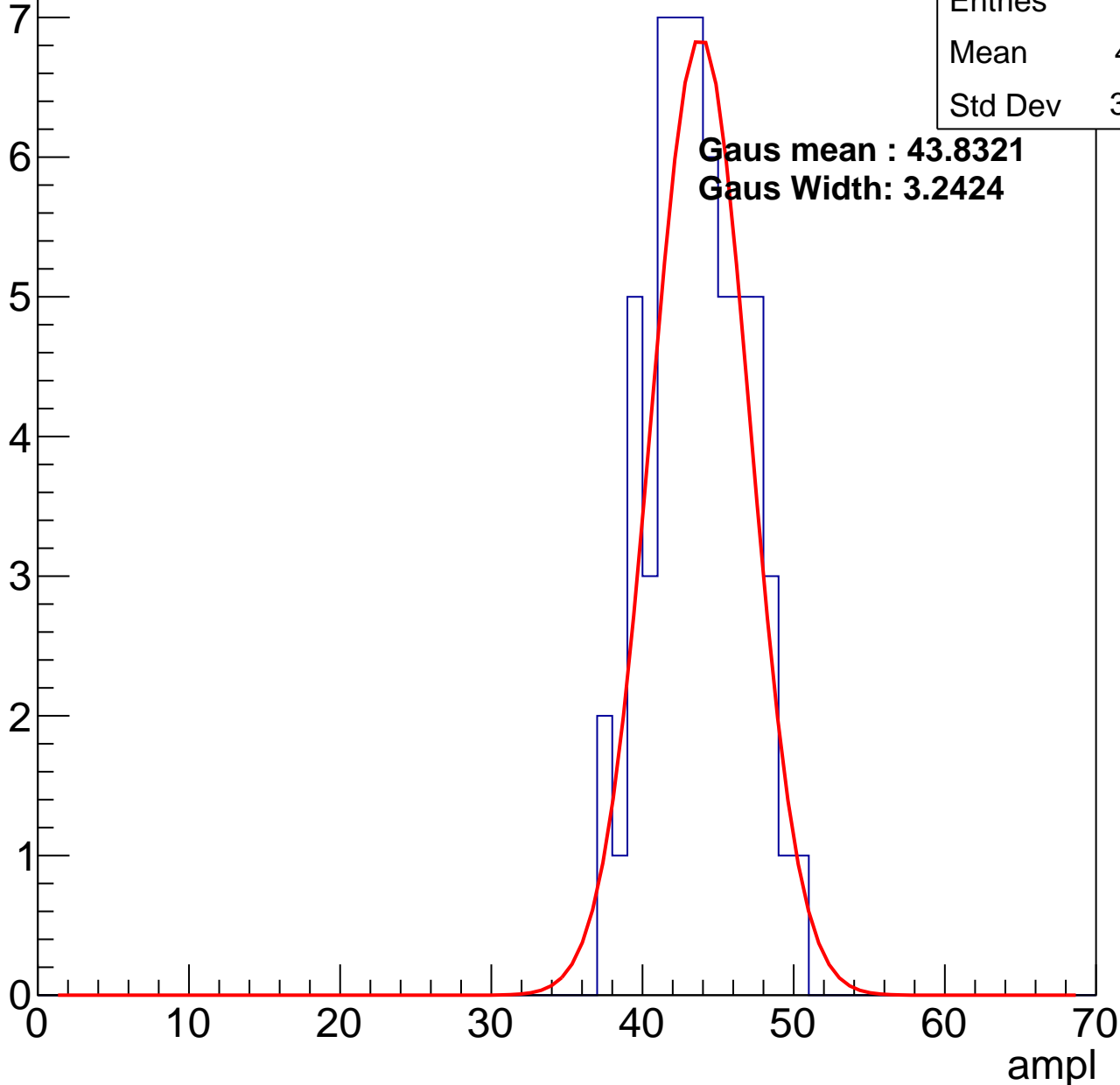
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	43.21
Std Dev	3.072

**Gaus mean : 43.8321**

**Gaus Width: 3.2424**

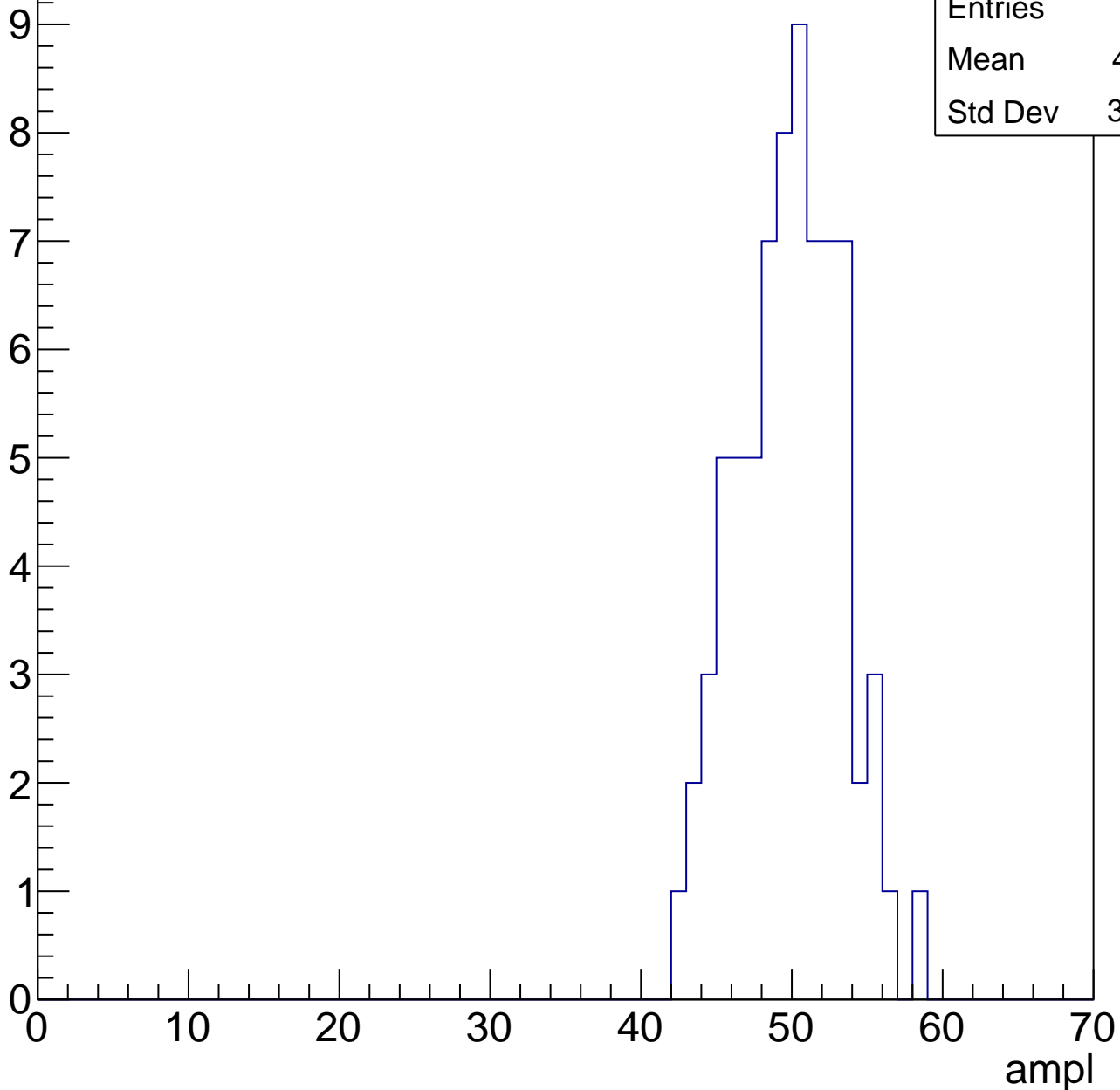


# B1L101S, U16-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	49.41
Std Dev	3.383

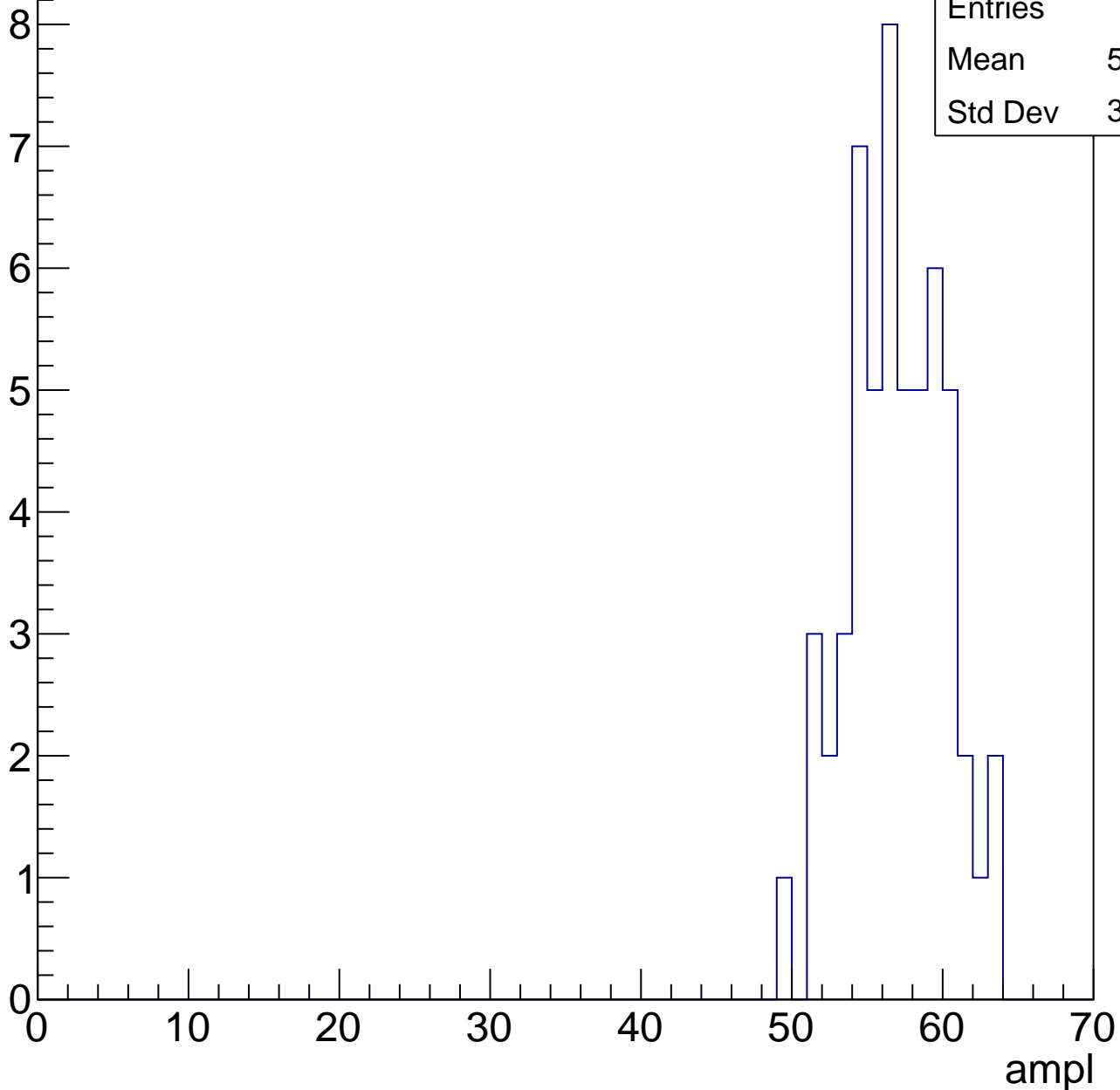


# B1L101S, U16-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

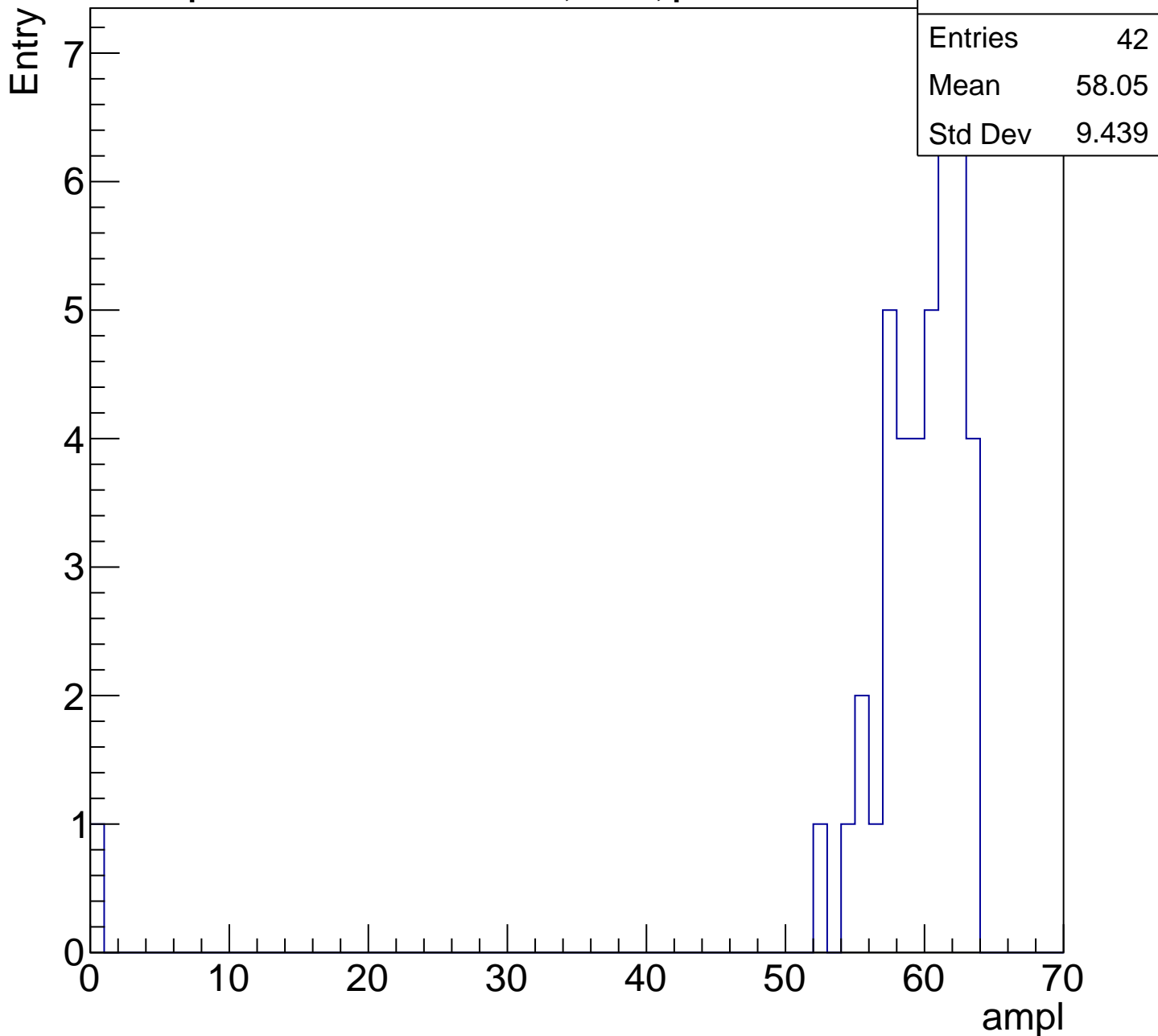
Entry

Entries	55
Mean	56.45
Std Dev	3.155



# B1L101S, U16-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U16-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch28, adc0

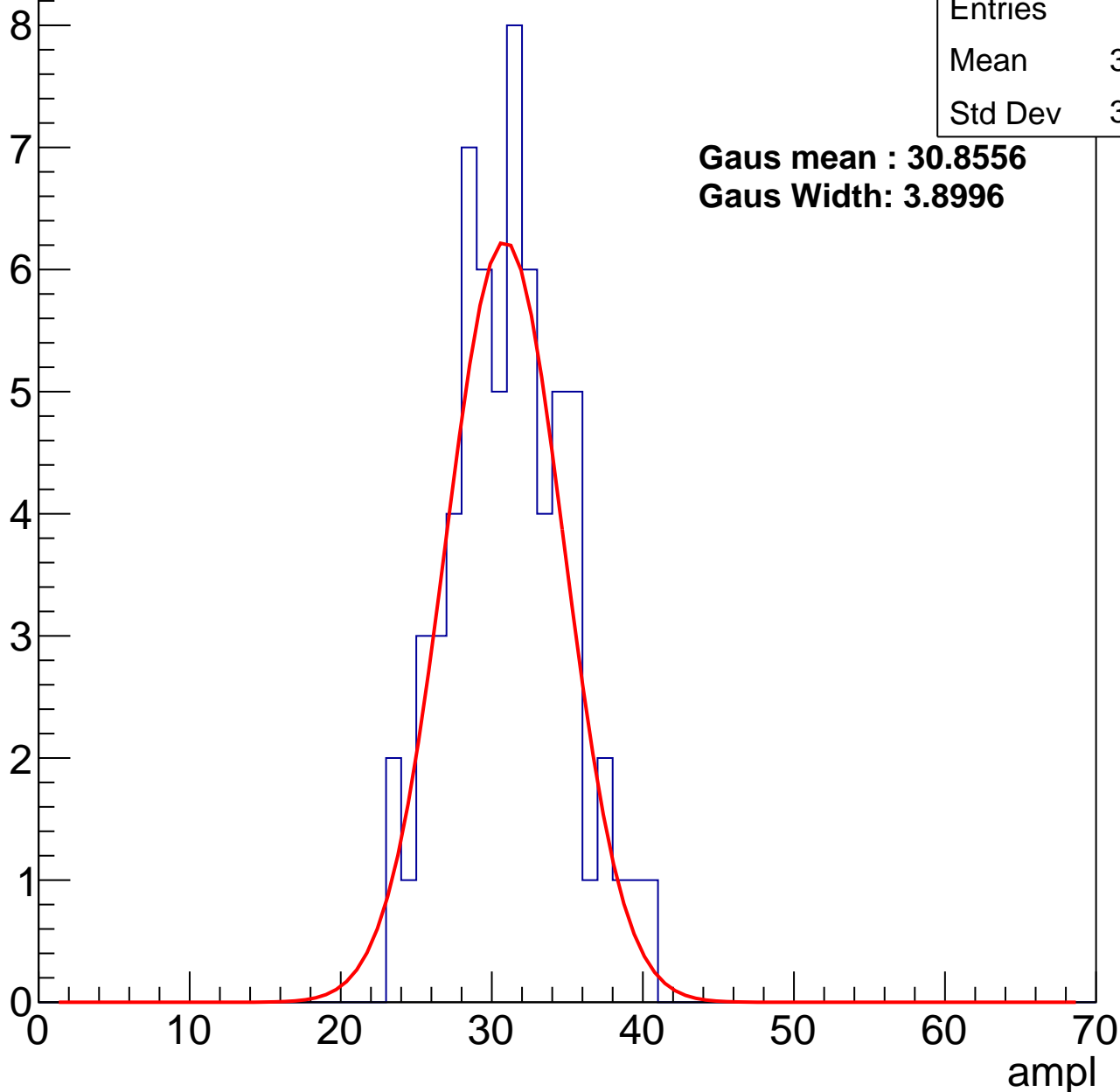
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	30.69
Std Dev	3.819

**Gaus mean : 30.8556**

**Gaus Width: 3.8996**



# B1L101S, U16-ch28, adc1

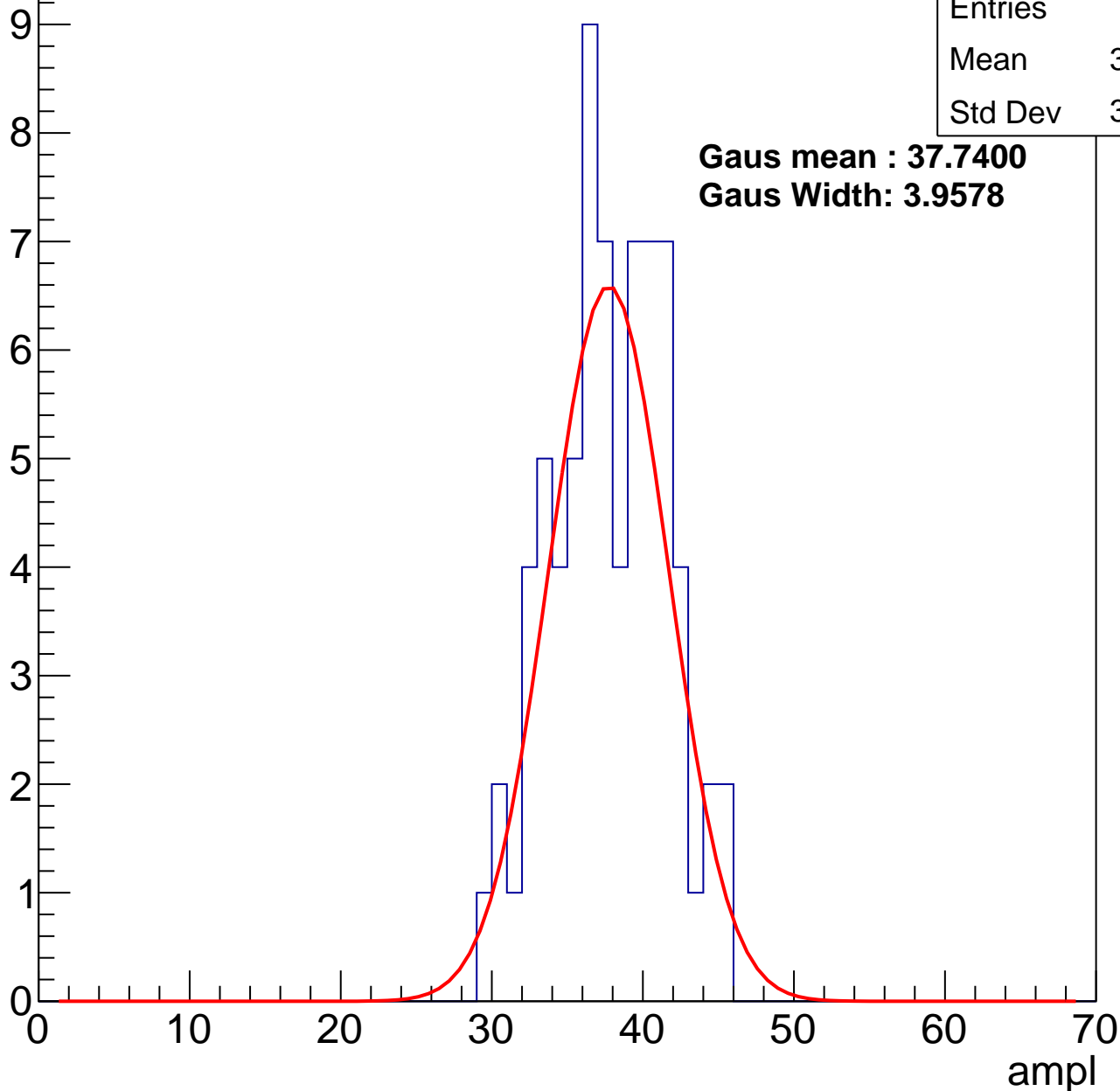
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	37.33
Std Dev	3.734

**Gaus mean : 37.7400**

**Gaus Width: 3.9578**



# B1L101S, U16-ch28, adc2

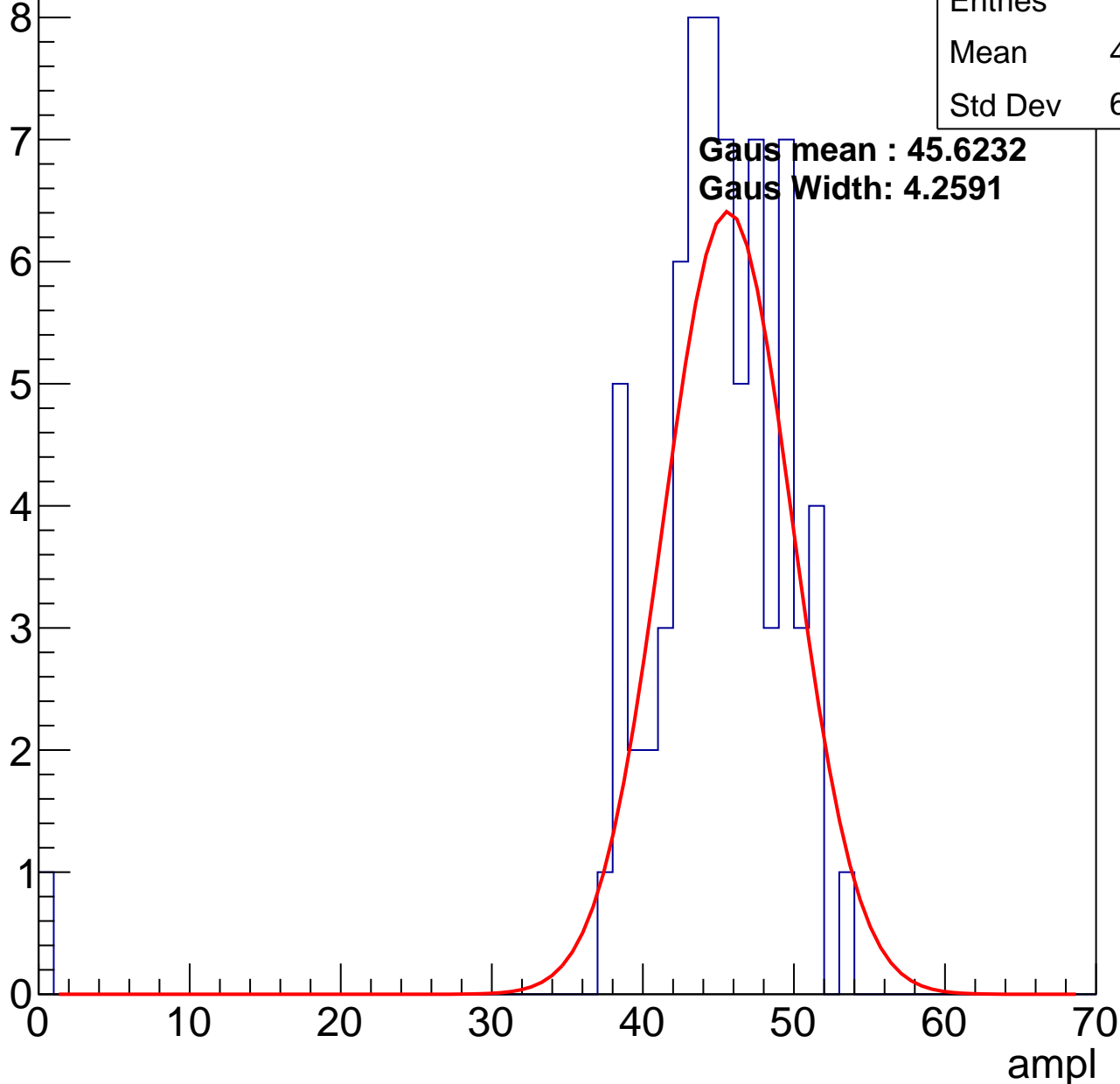
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	44.16
Std Dev	6.413

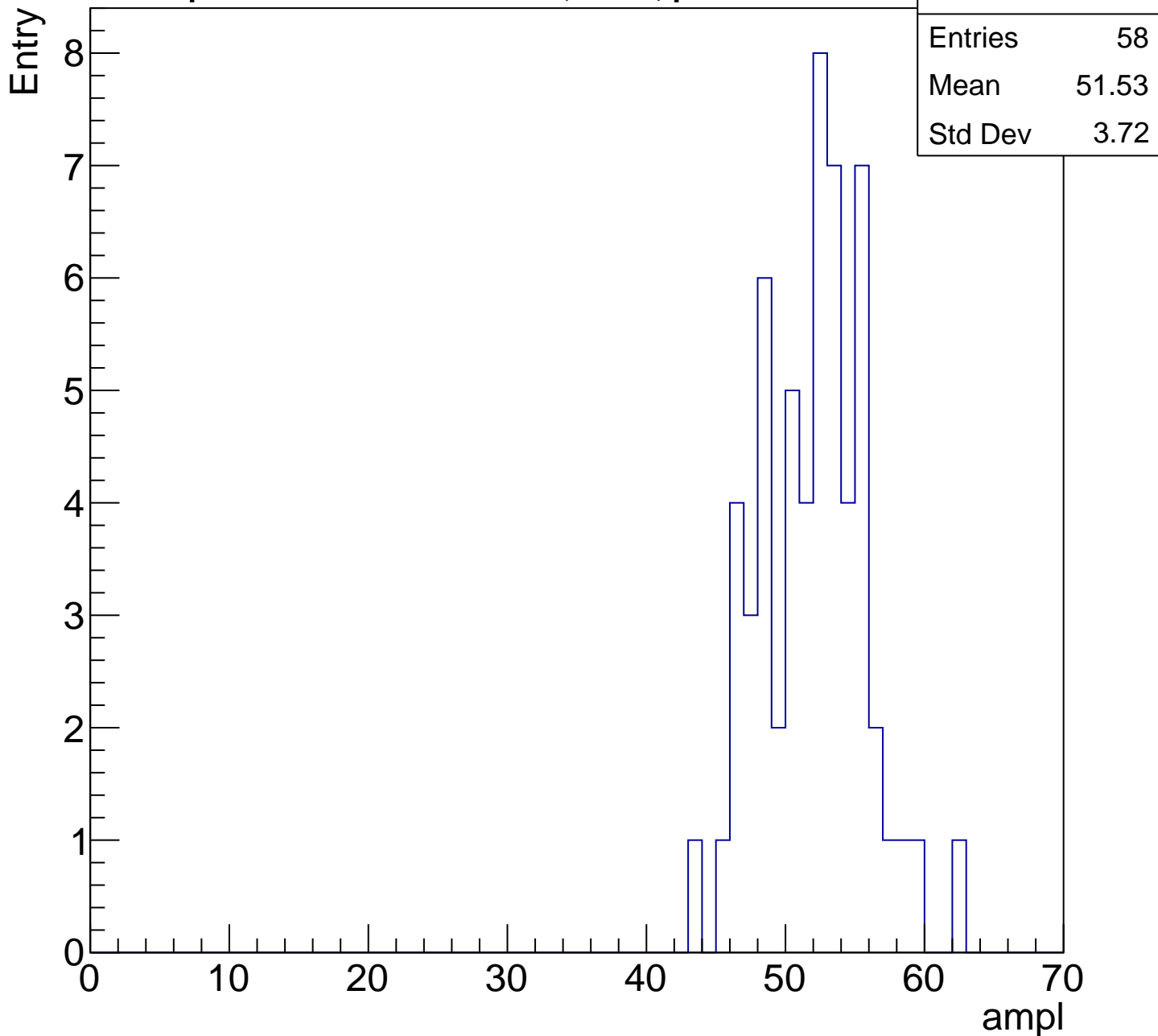
Gaus mean : 45.6232

Gaus Width: 4.2591



# B1L101S, U16-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

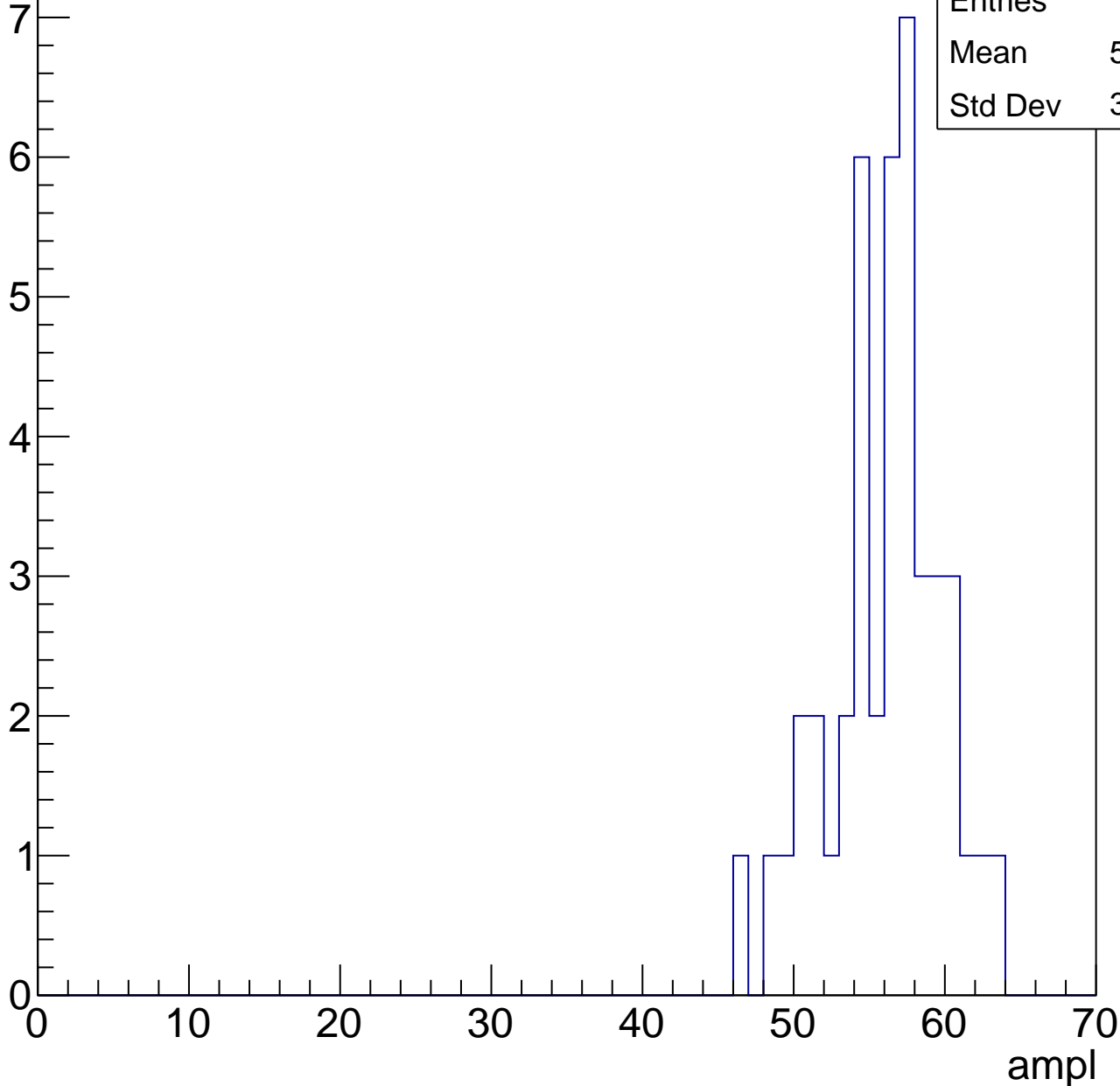


# B1L101S, U16-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	55.56
Std Dev	3.706

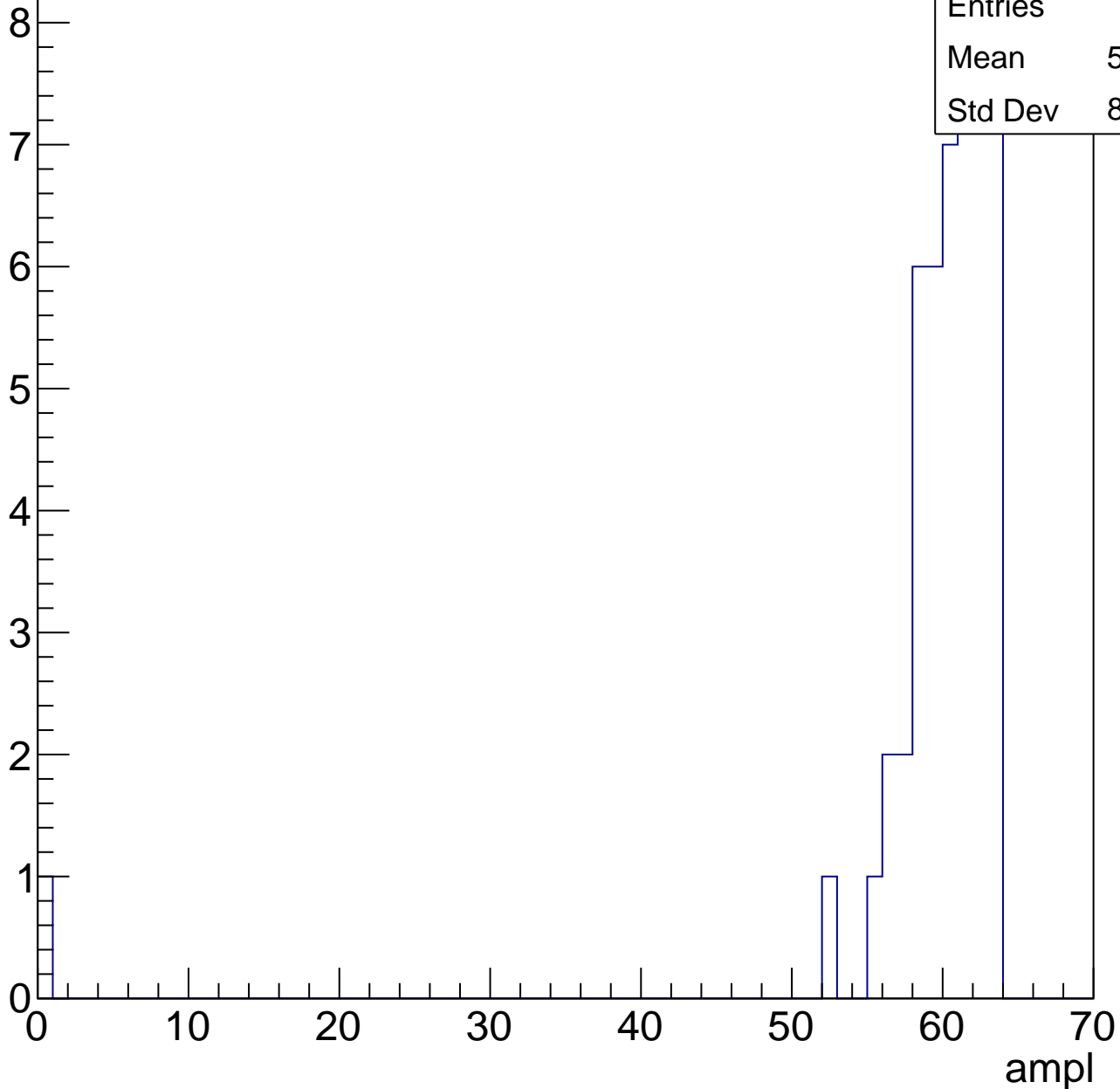


# B1L101S, U16-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	58.86
Std Dev	8.736



# B1L101S, U16-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch29, adc0

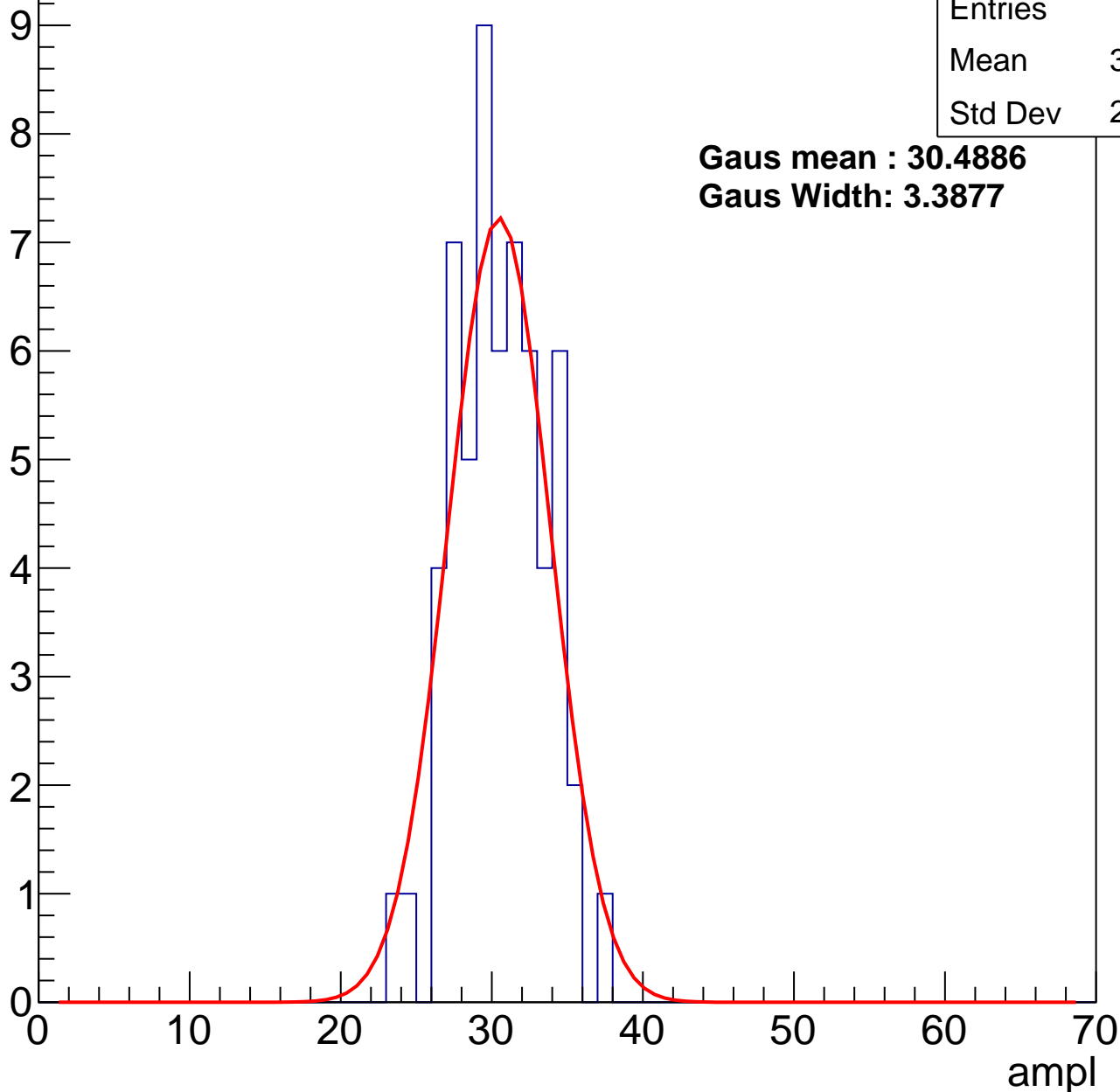
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	30.05
Std Dev	2.919

**Gaus mean : 30.4886**

**Gaus Width: 3.3877**

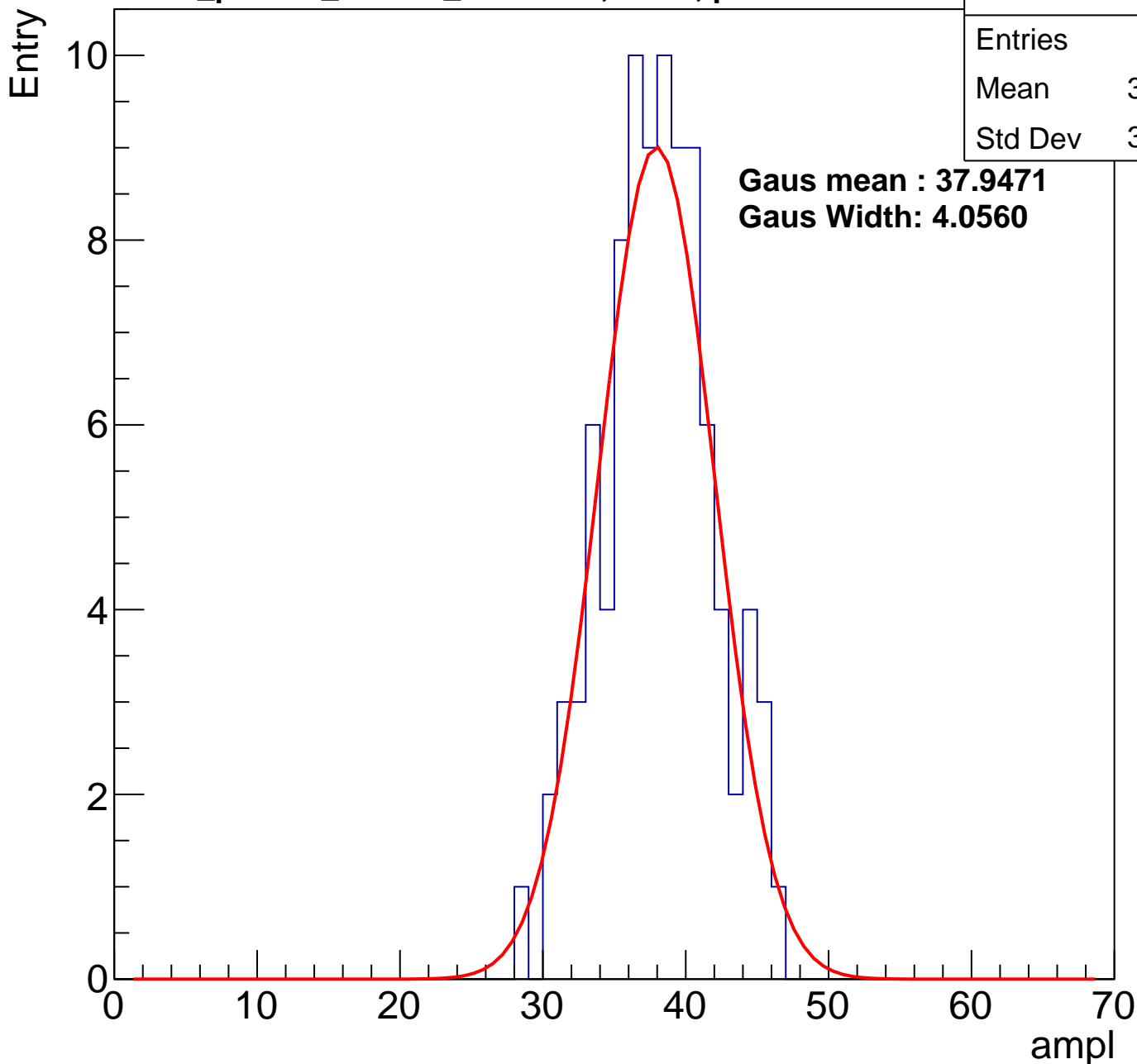


# B1L101S, U16-ch29, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	94
Mean	37.57
Std Dev	3.816

**Gaus mean : 37.9471**  
**Gaus Width: 4.0560**



# B1L101S, U16-ch29, adc2

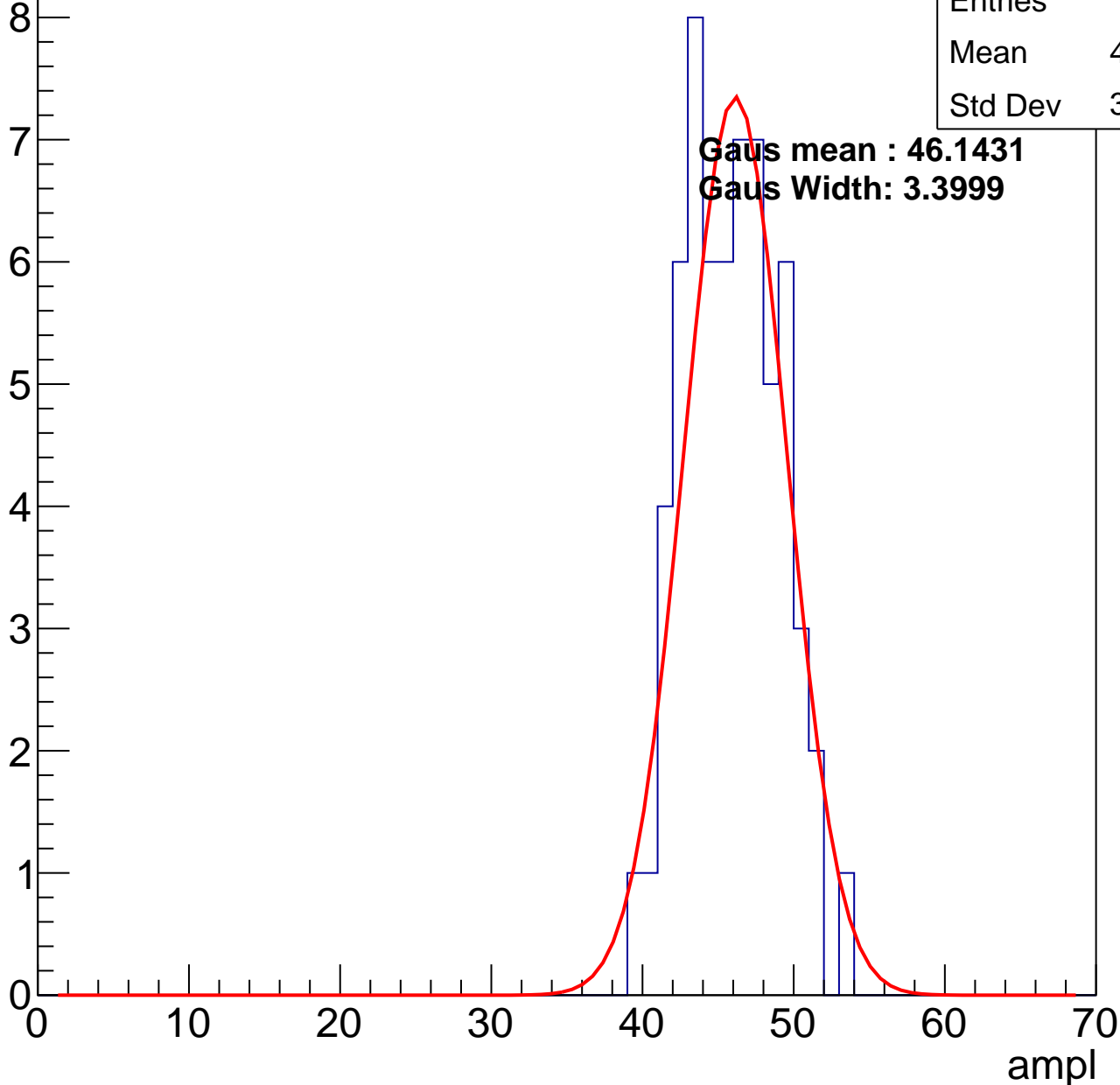
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	45.44
Std Dev	3.064

**Gaus mean : 46.1431**

**Gaus Width: 3.3999**

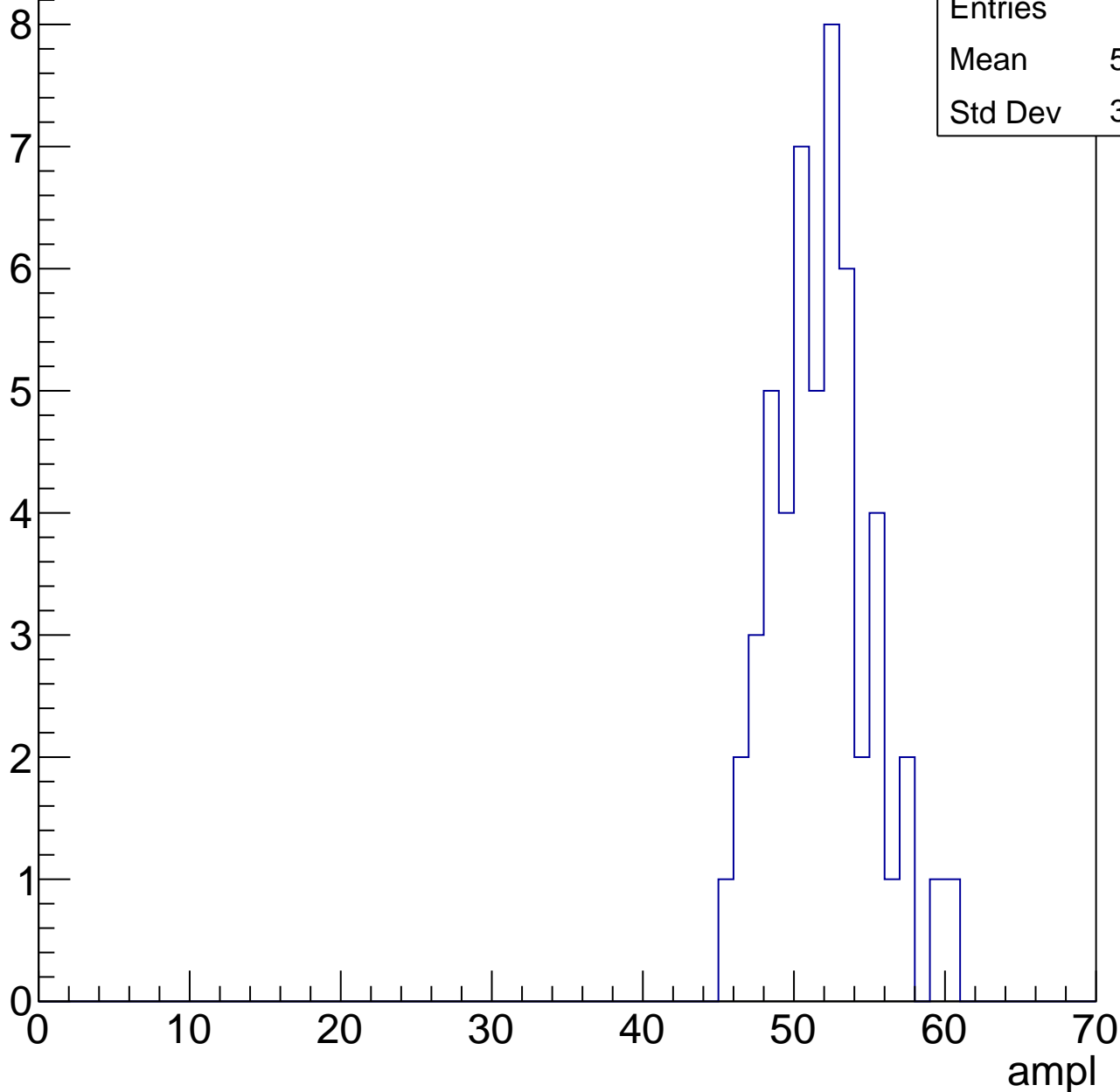


# B1L101S, U16-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	51.35
Std Dev	3.257

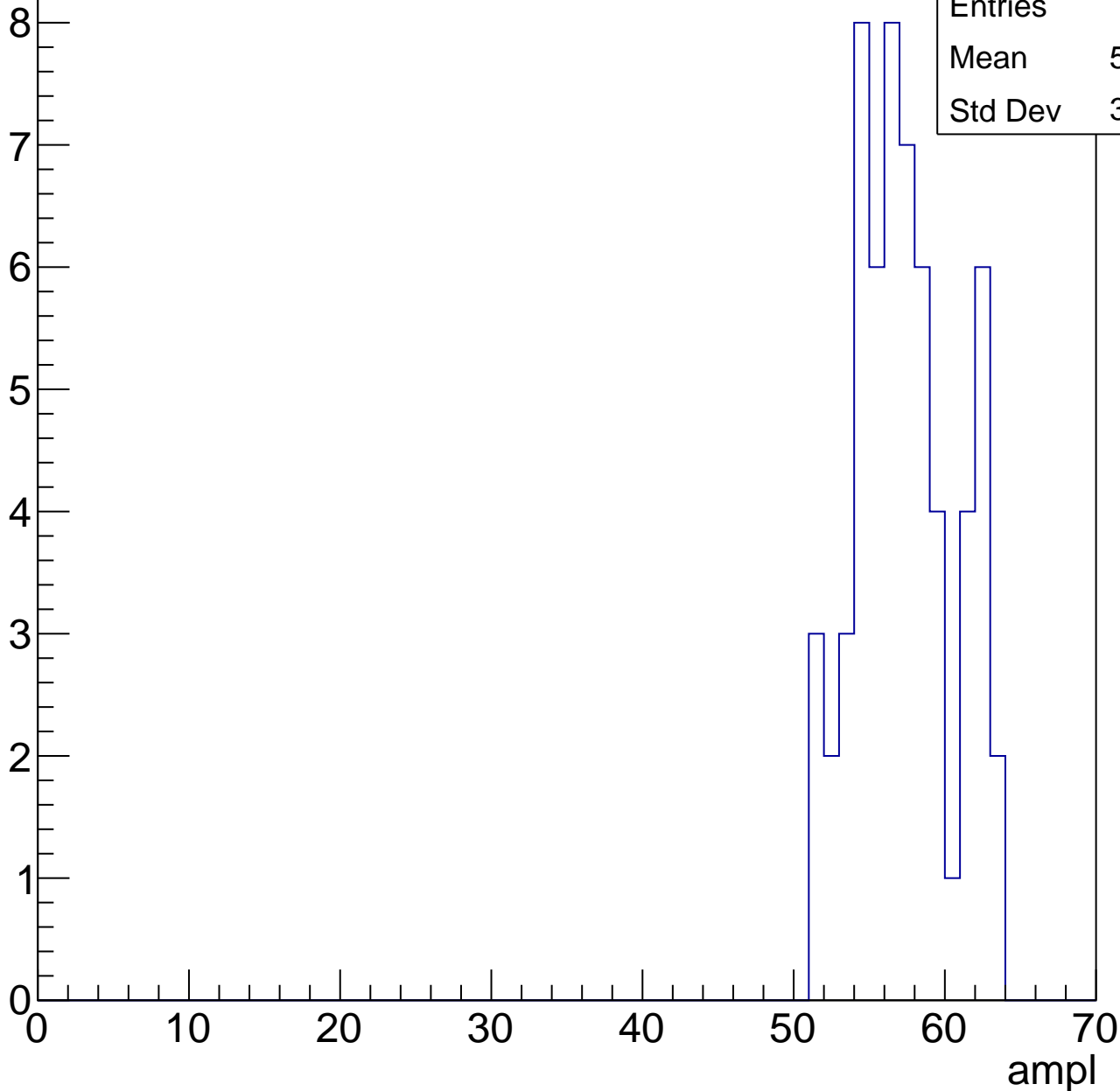


# B1L101S, U16-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	56.85
Std Dev	3.229



# B1L101S, U16-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

Entries

32

Mean

60.28

Std Dev

1.891

0

ampl

0

10

20

30

40

50

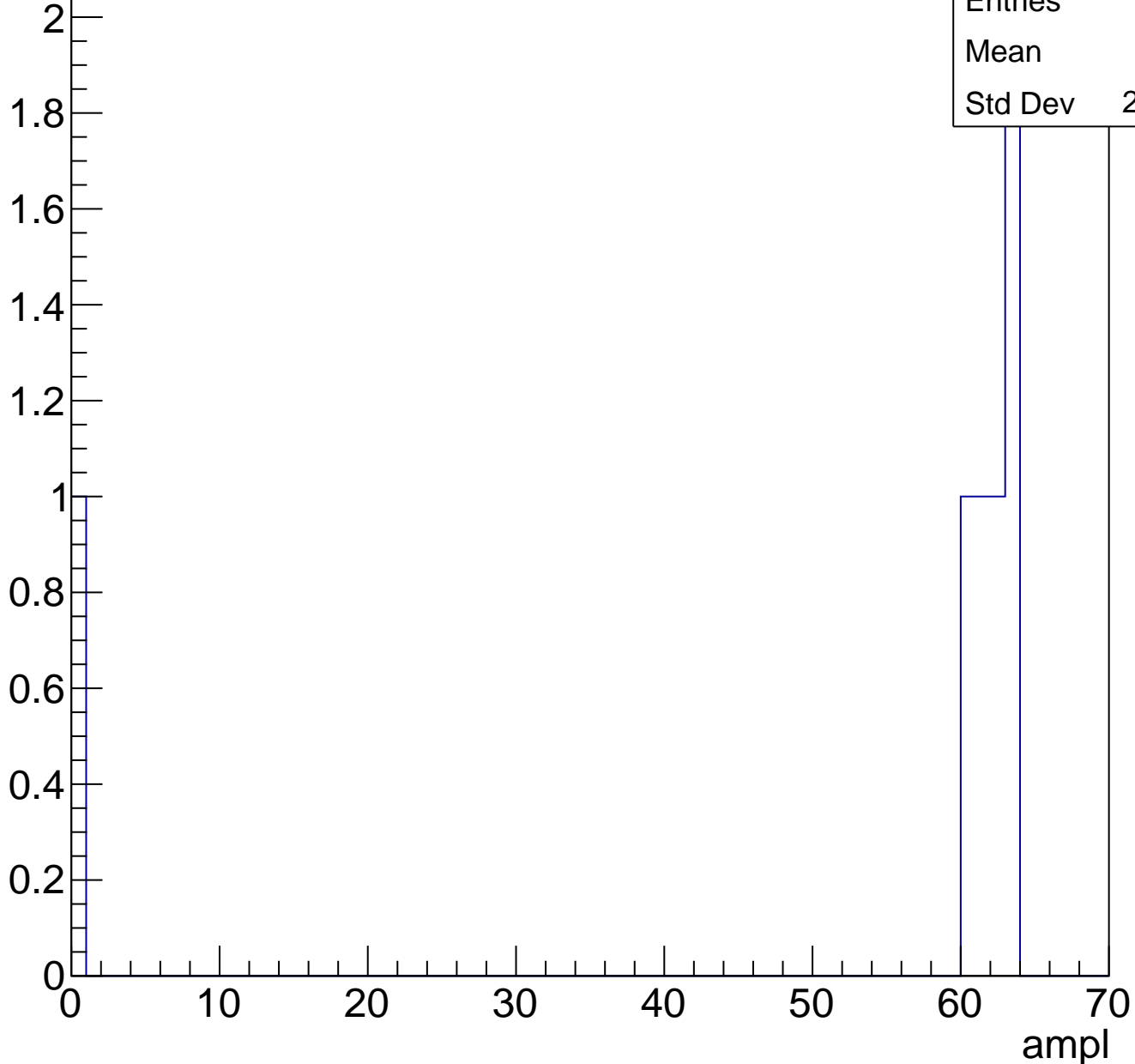
60

70

# B1L101S, U16-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	6
Mean	51.5
Std Dev	23.06



# B1L101S, U16-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U16-ch30, adc0

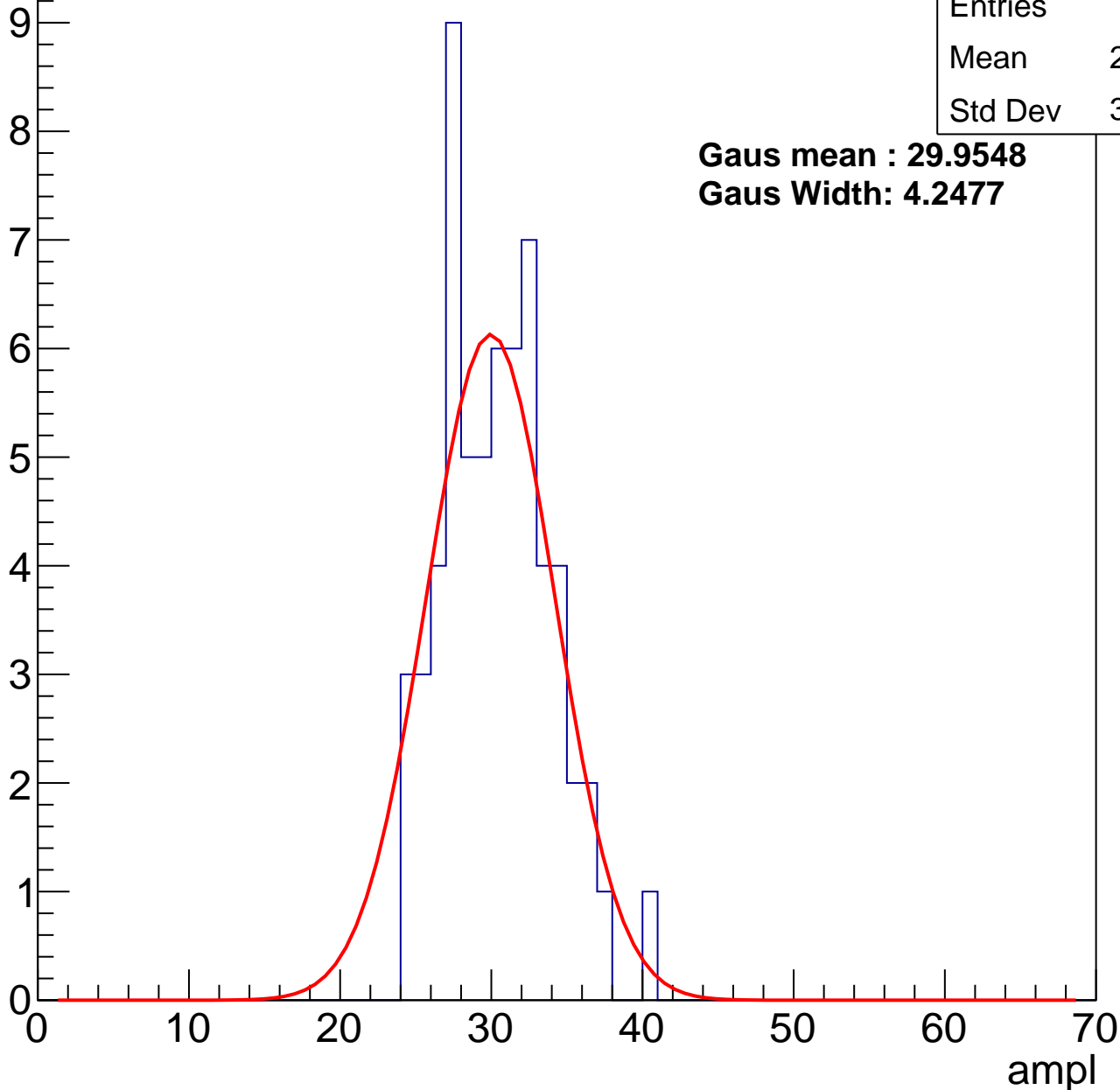
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	29.94
Std Dev	3.496

**Gaus mean : 29.9548**

**Gaus Width: 4.2477**



# B1L101S, U16-ch30, adc1

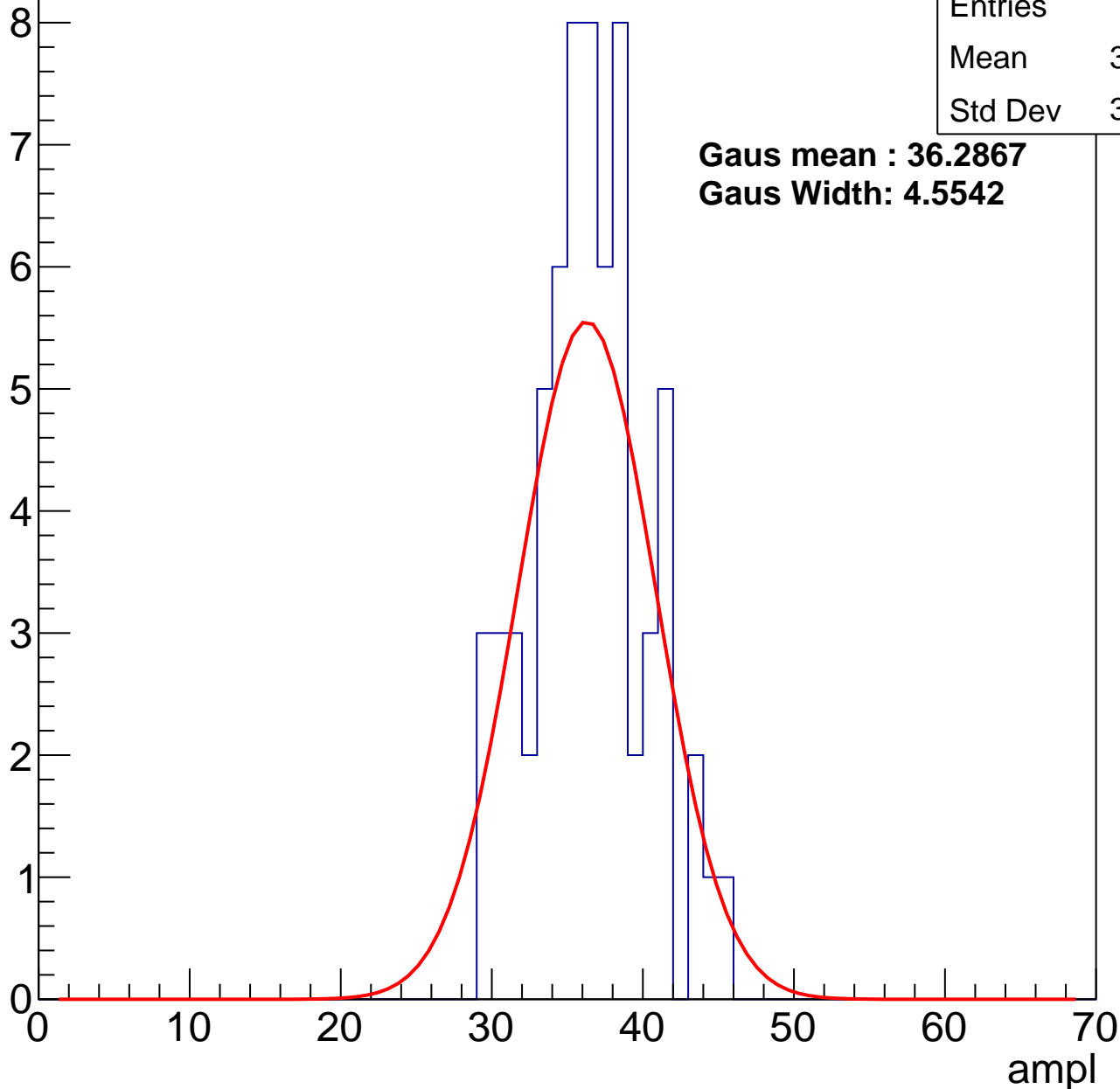
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	35.98
Std Dev	3.715

**Gaus mean : 36.2867**

**Gaus Width: 4.5542**



# B1L101S, U16-ch30, adc2

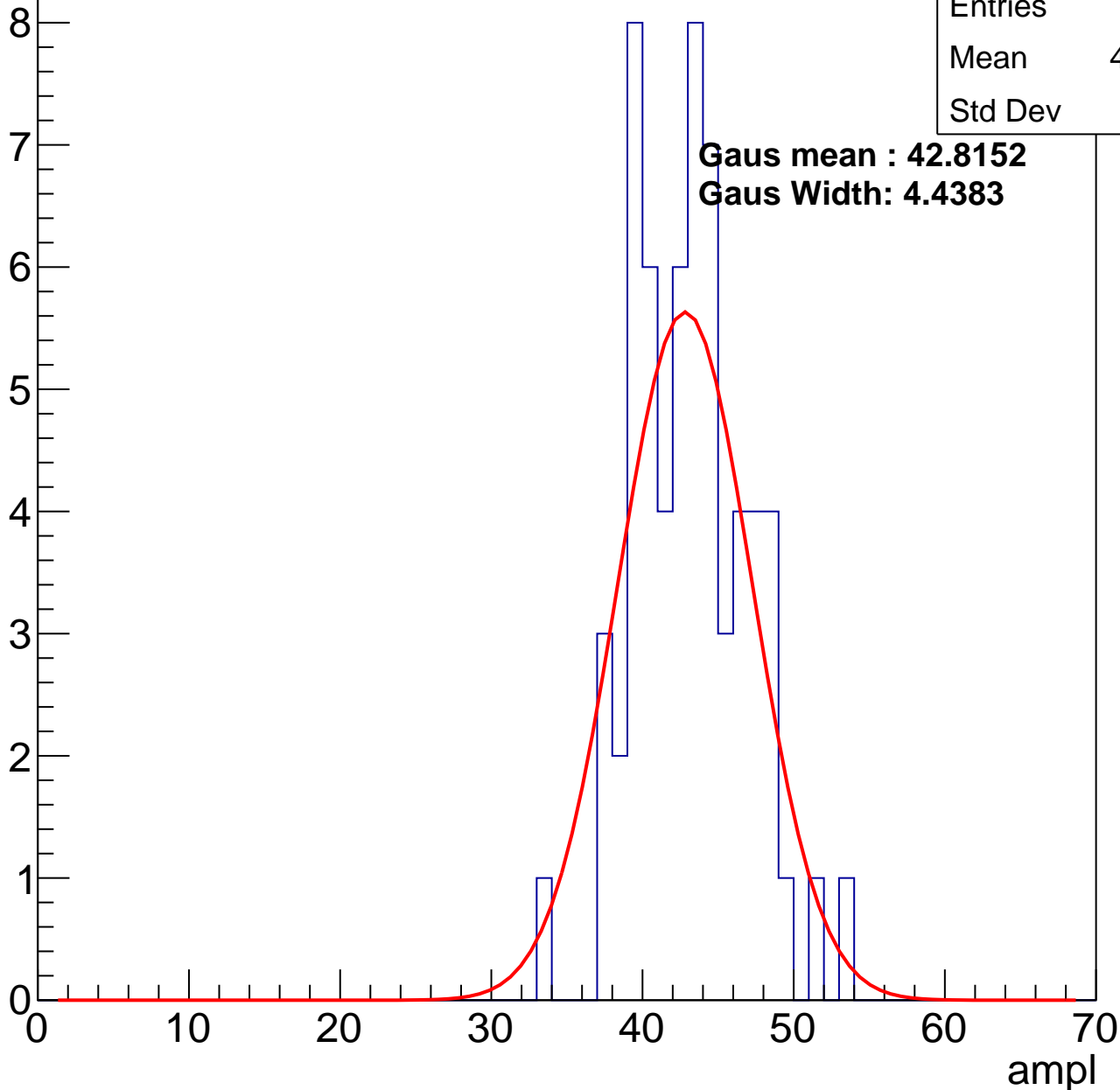
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	42.73
Std Dev	3.73

**Gaus mean : 42.8152**

**Gaus Width: 4.4383**

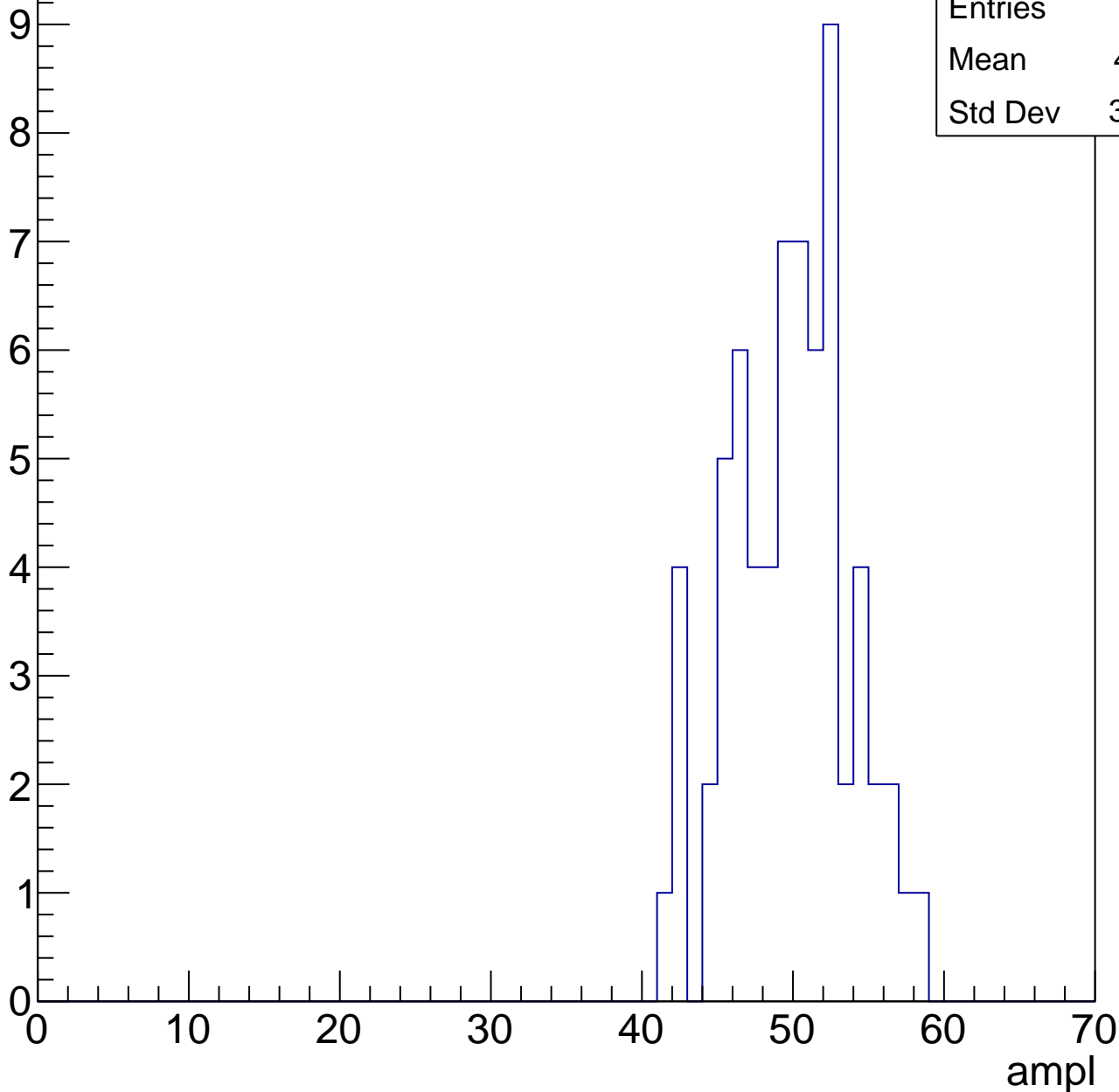


# B1L101S, U16-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	49.31
Std Dev	3.895

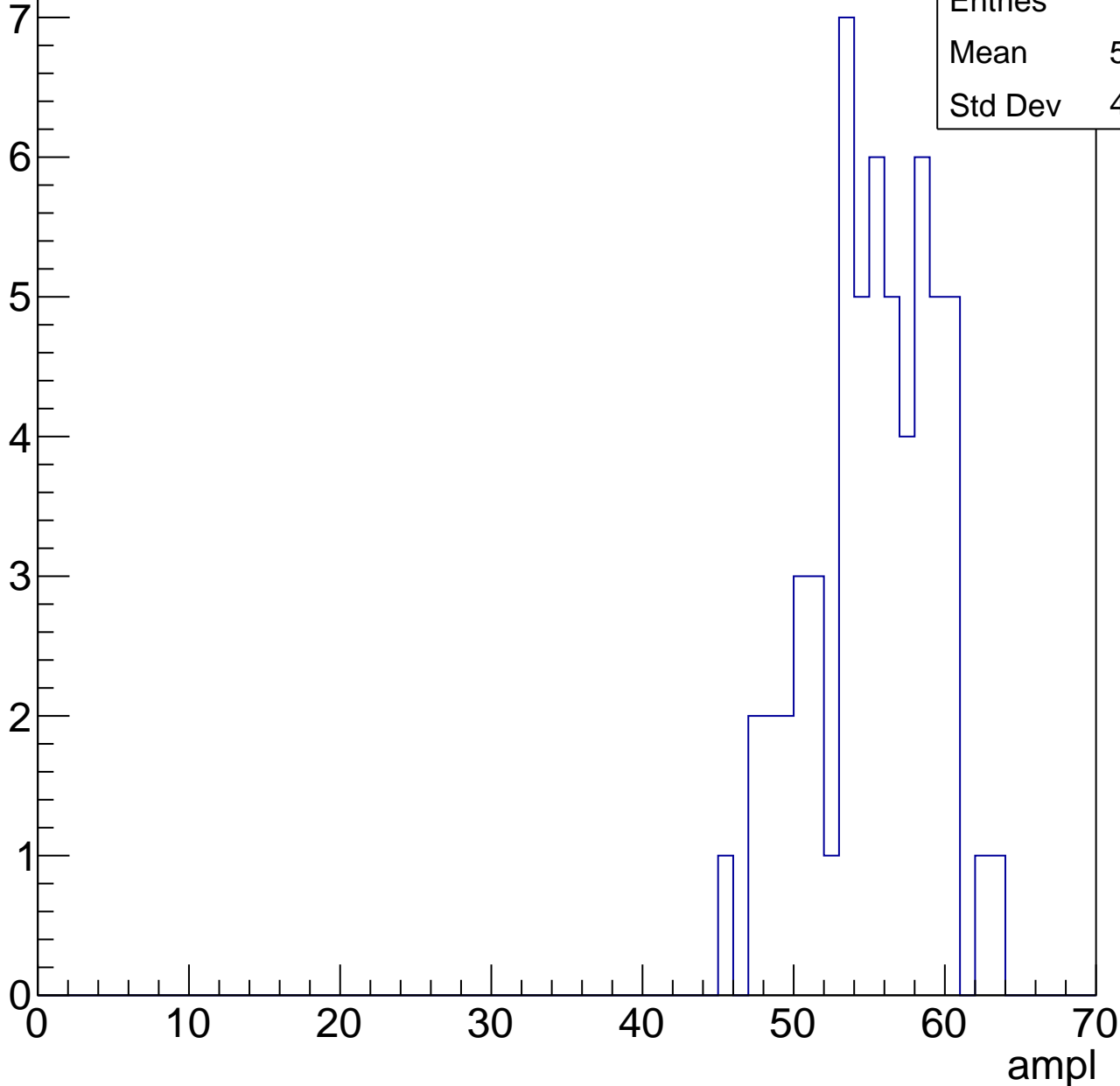


# B1L101S, U16-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	54.83
Std Dev	4.022

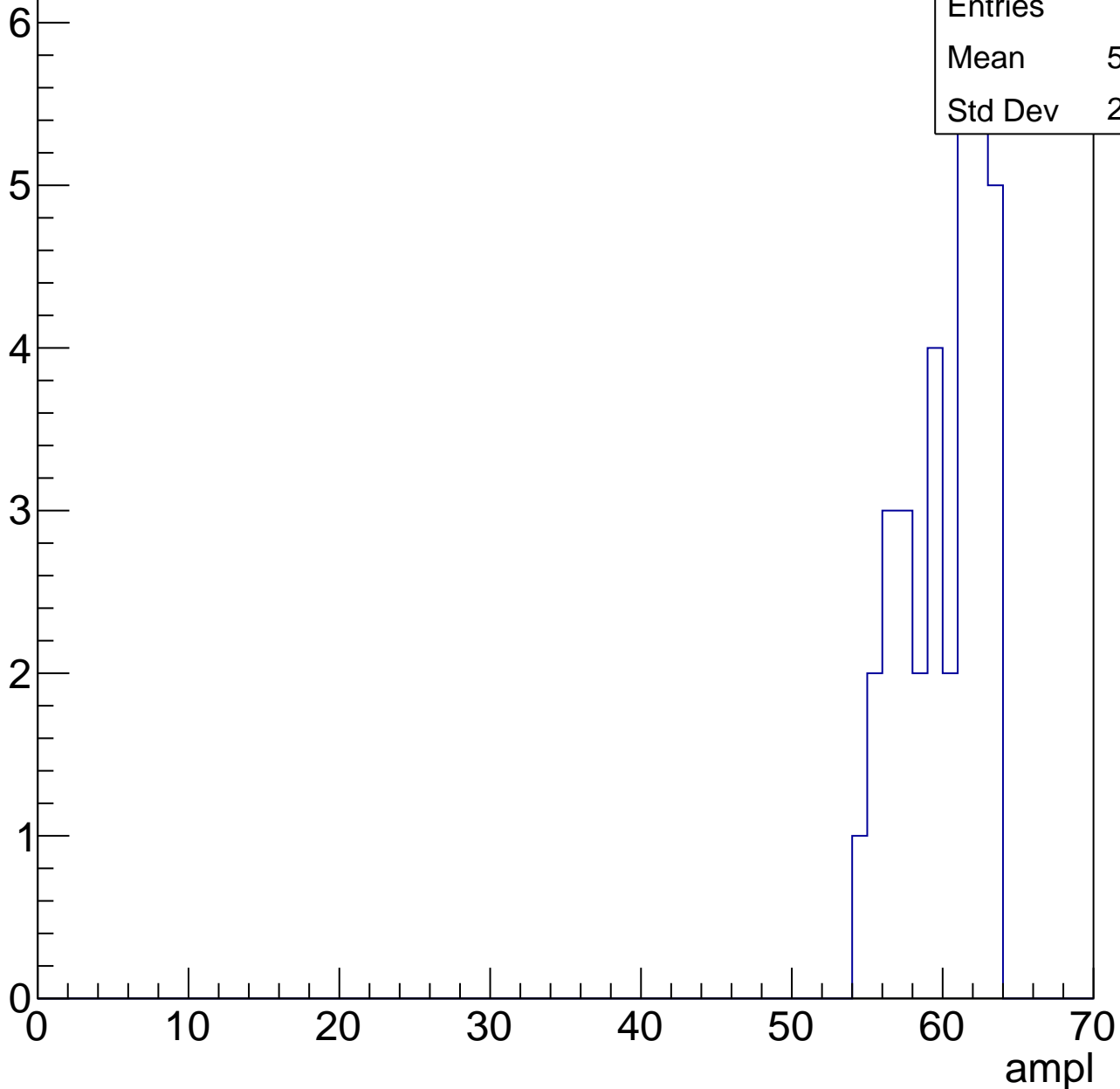


# B1L101S, U16-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

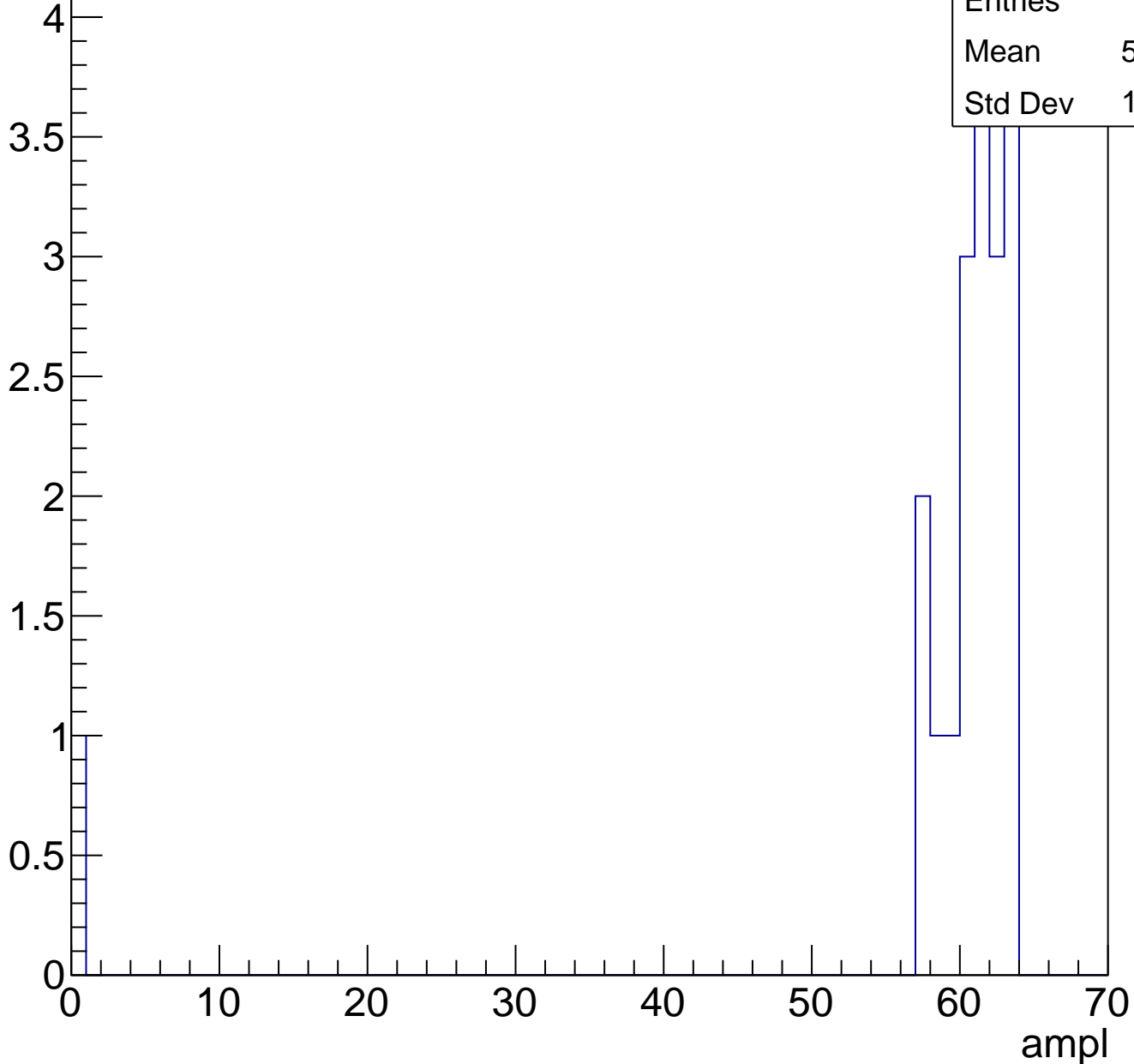
Entries	34
Mean	59.65
Std Dev	2.678



# B1L101S, U16-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	22
Std Dev	0

ampl

# B1L101S, U16-ch31, adc0

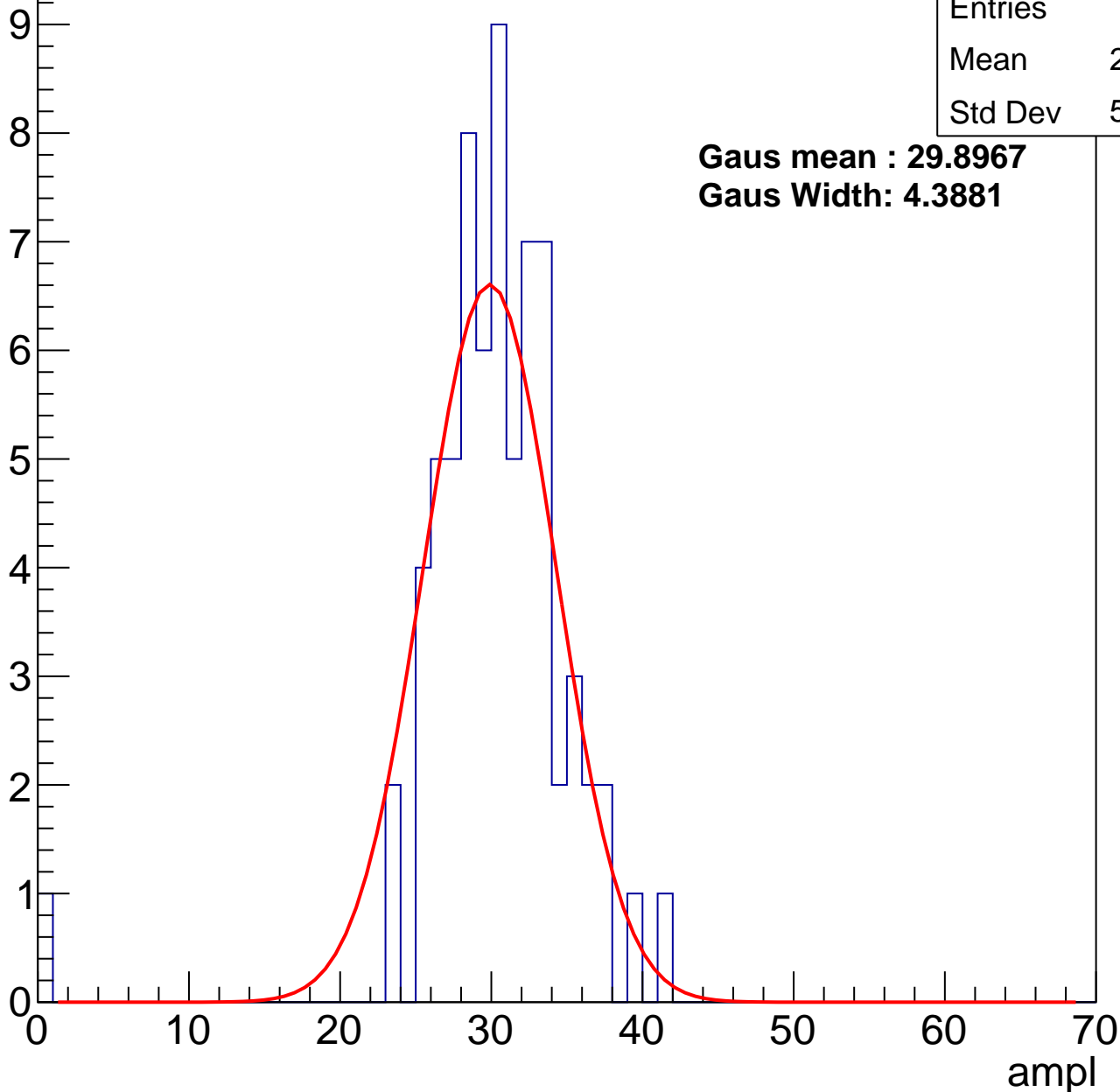
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	29.83
Std Dev	5.119

**Gaus mean : 29.8967**

**Gaus Width: 4.3881**



# B1L101S, U16-ch31, adc1

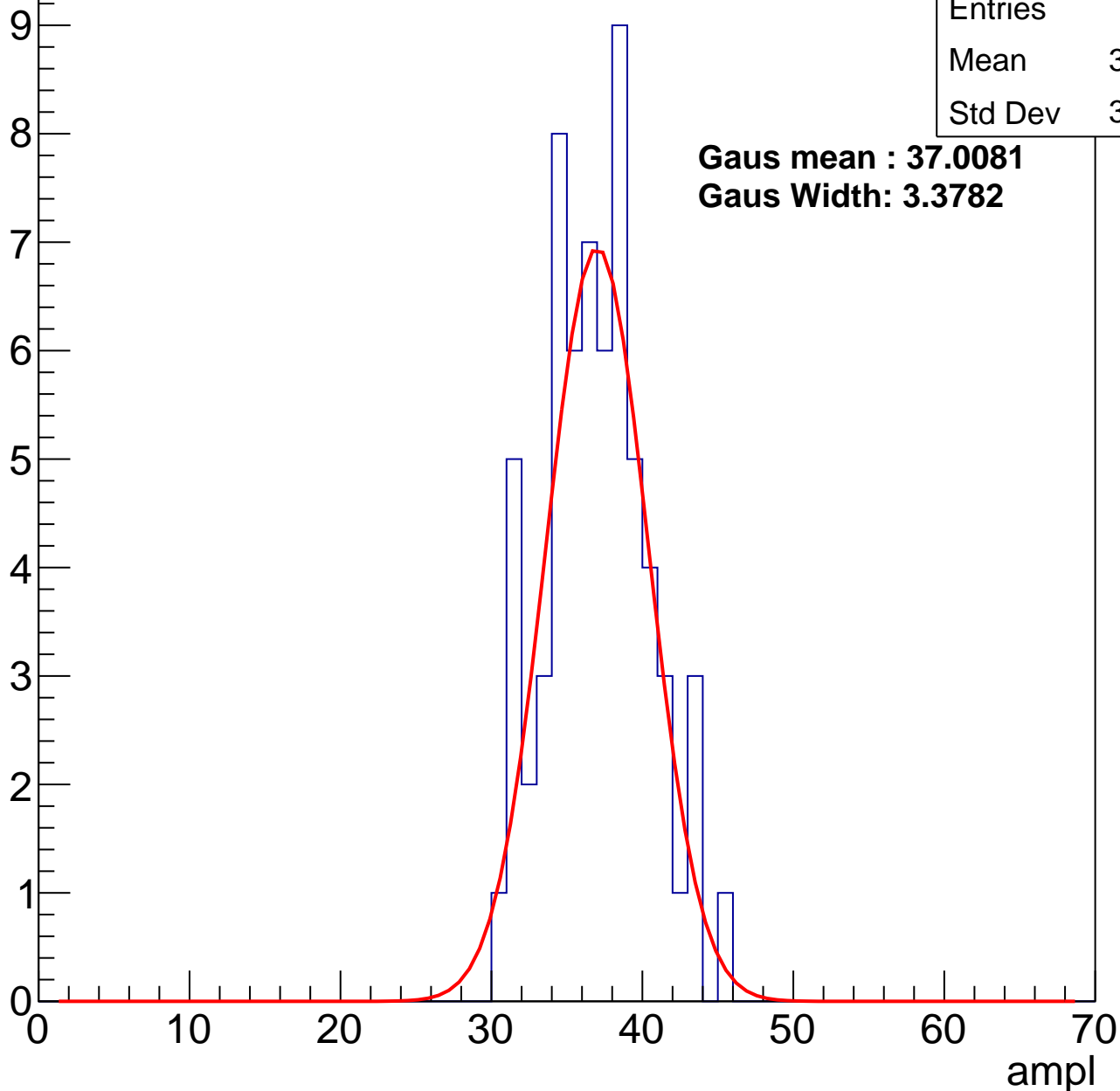
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	36.56
Std Dev	3.372

**Gaus mean : 37.0081**

**Gaus Width: 3.3782**



# B1L101S, U16-ch31, adc2

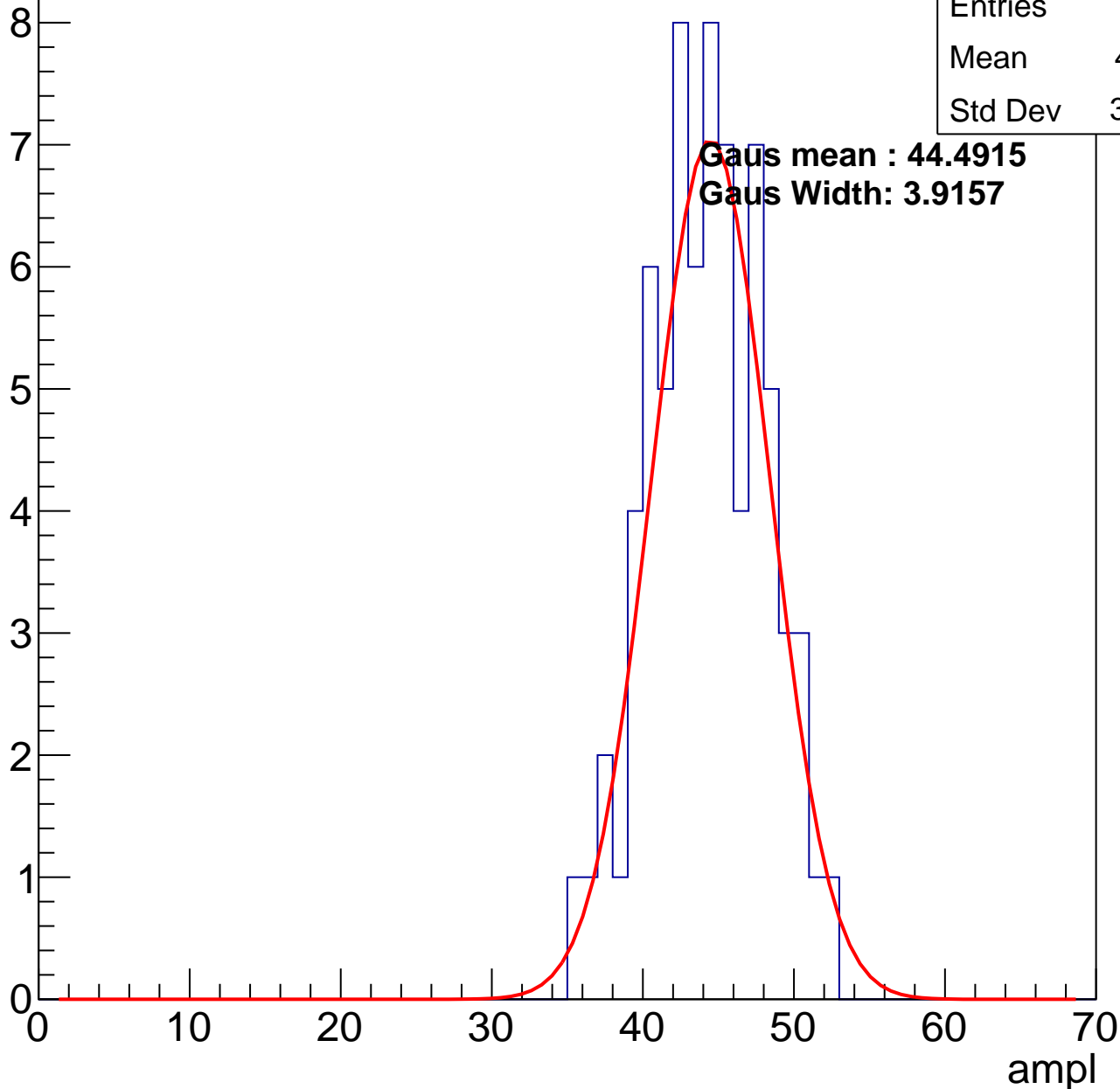
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	43.81
Std Dev	3.733

**Gaus mean : 44.4915**

**Gaus Width: 3.9157**

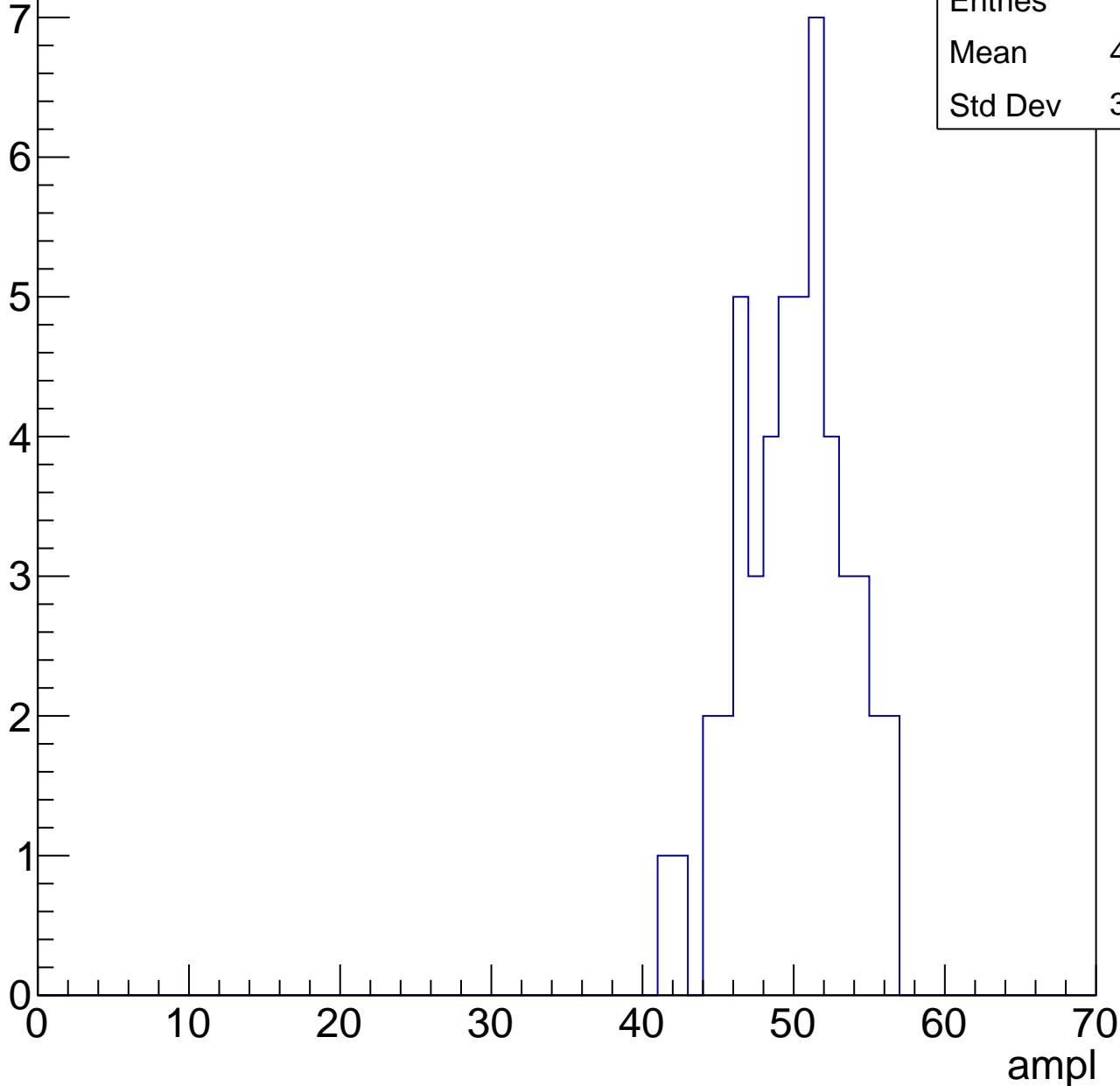


# B1L101S, U16-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	49.53
Std Dev	3.512

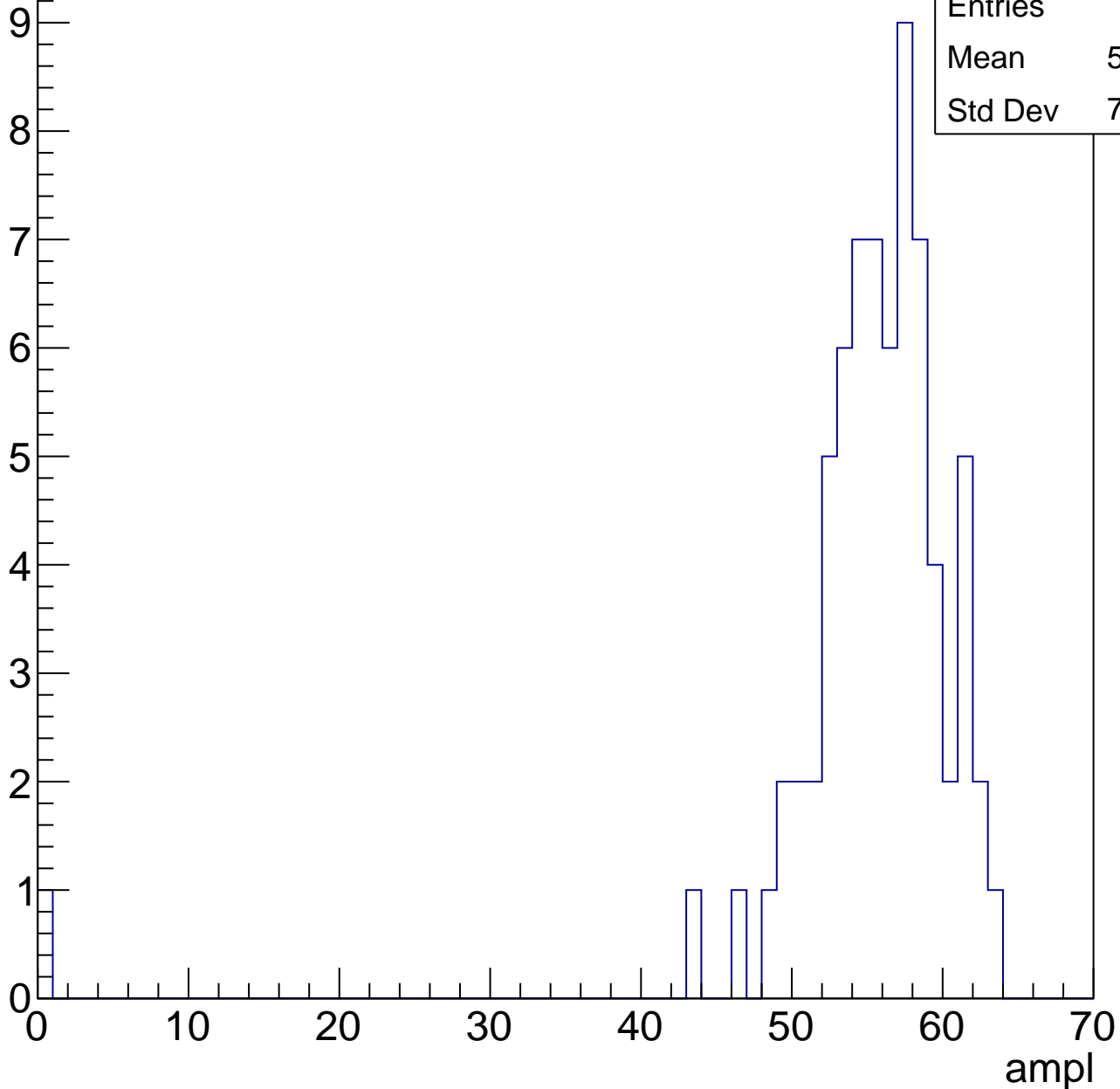


# B1L101S, U16-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

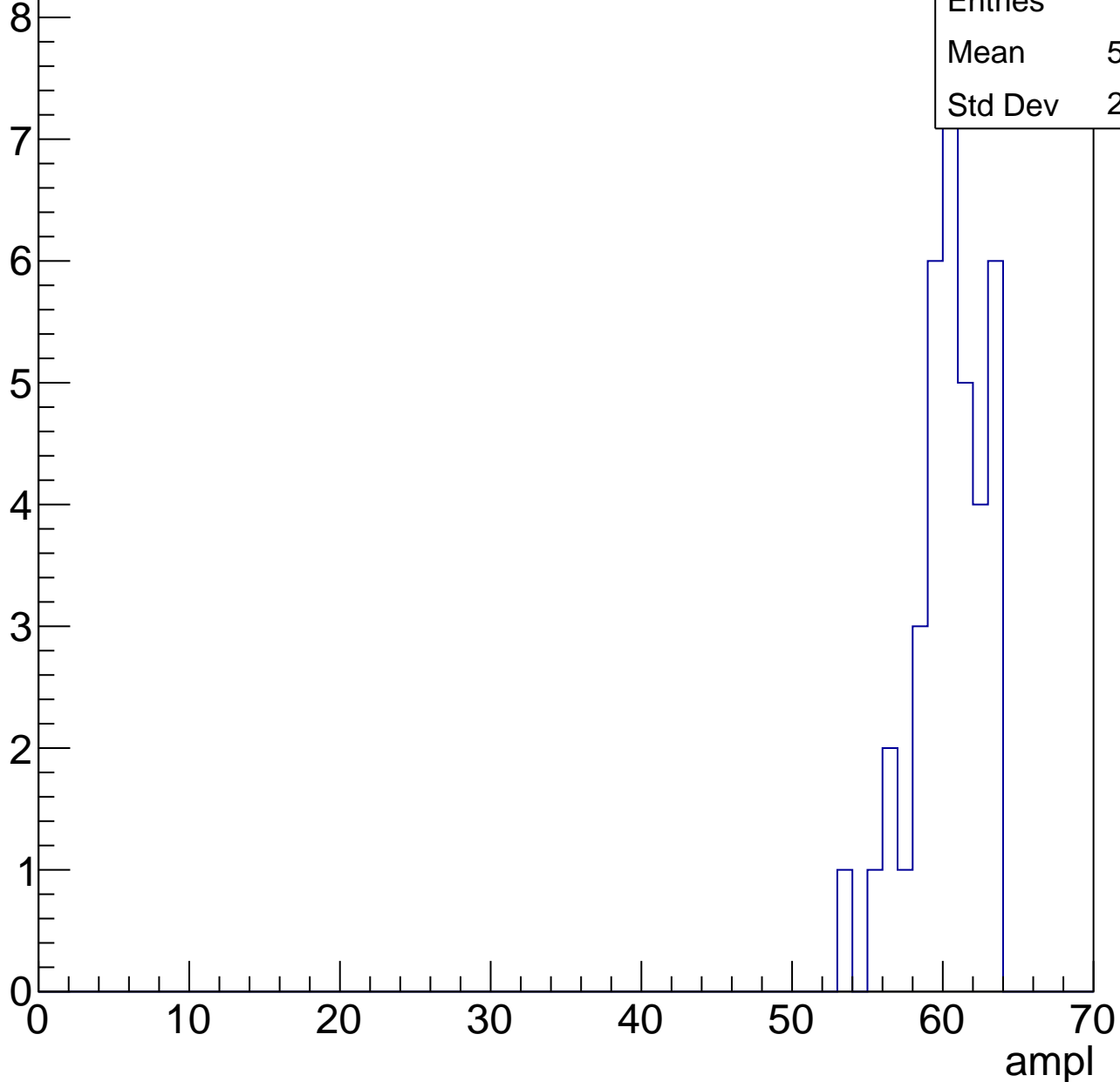
Entries	71
Mean	54.66
Std Dev	7.582



# B1L101S, U16-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

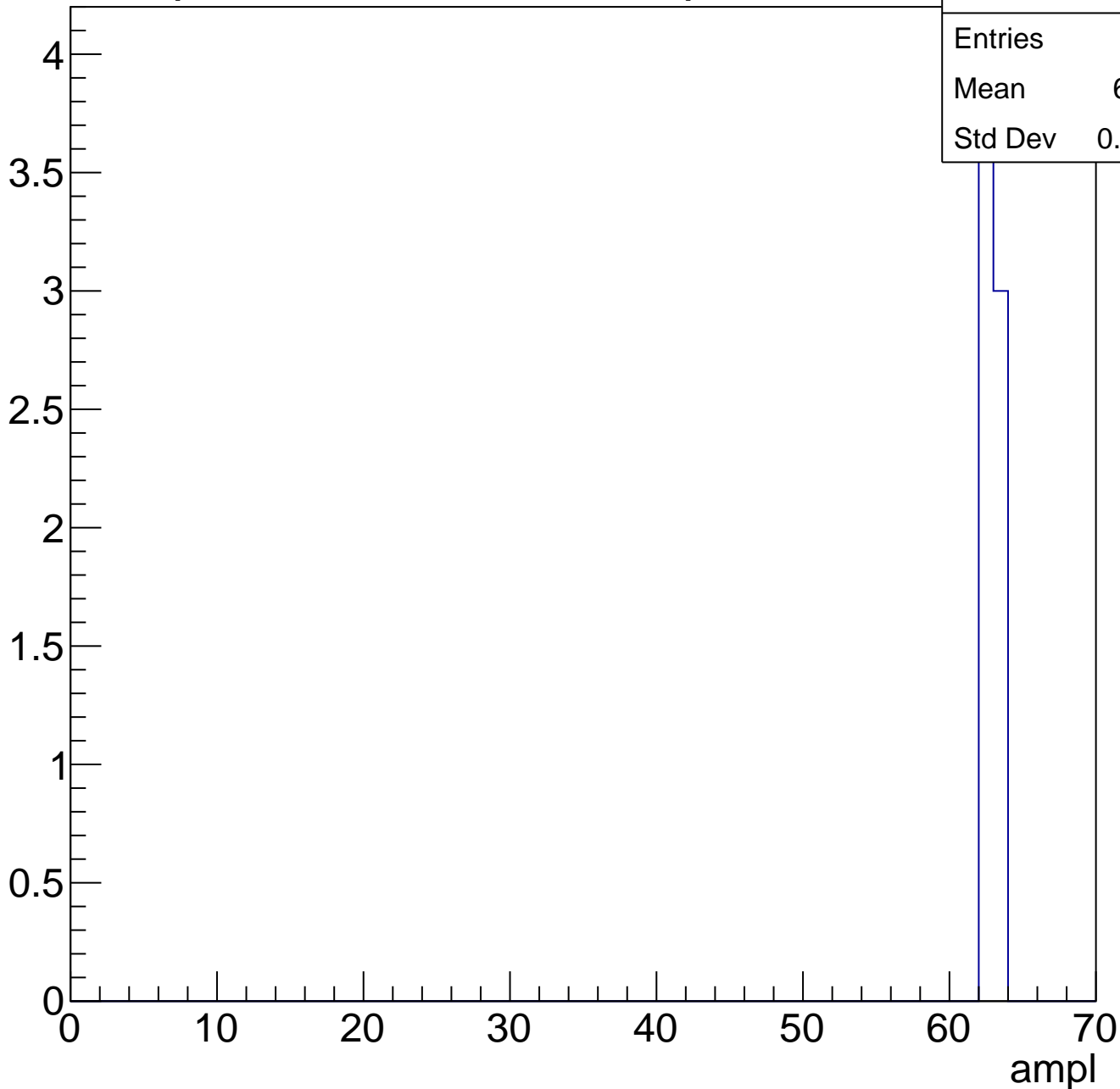
Entry



# B1L101S, U16-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	7
Mean	62.43
Std Dev	0.4949



# B1L101S, U16-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U16-ch32, adc0

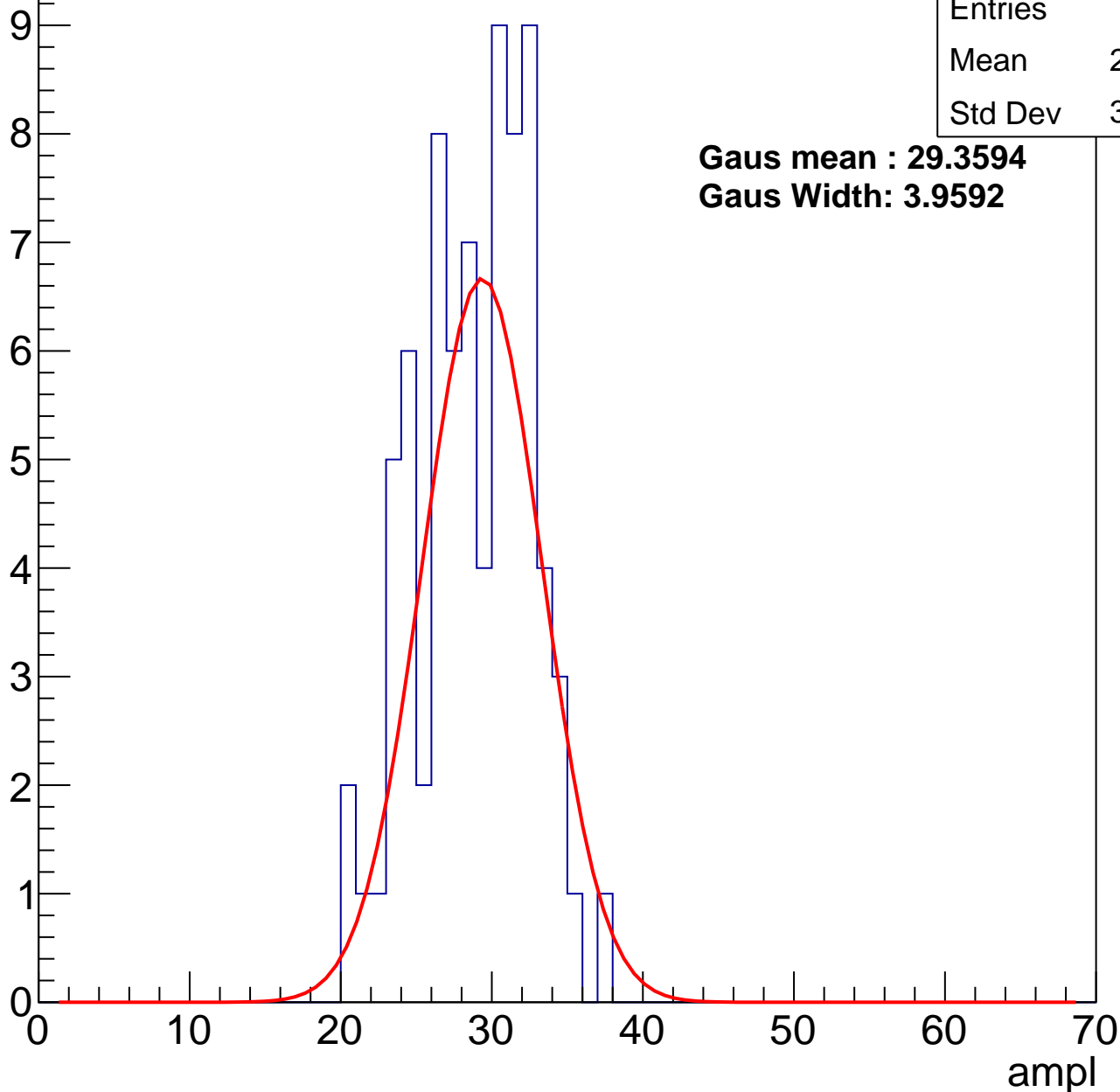
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	28.39
Std Dev	3.732

**Gaus mean : 29.3594**

**Gaus Width: 3.9592**



# B1L101S, U16-ch32, adc1

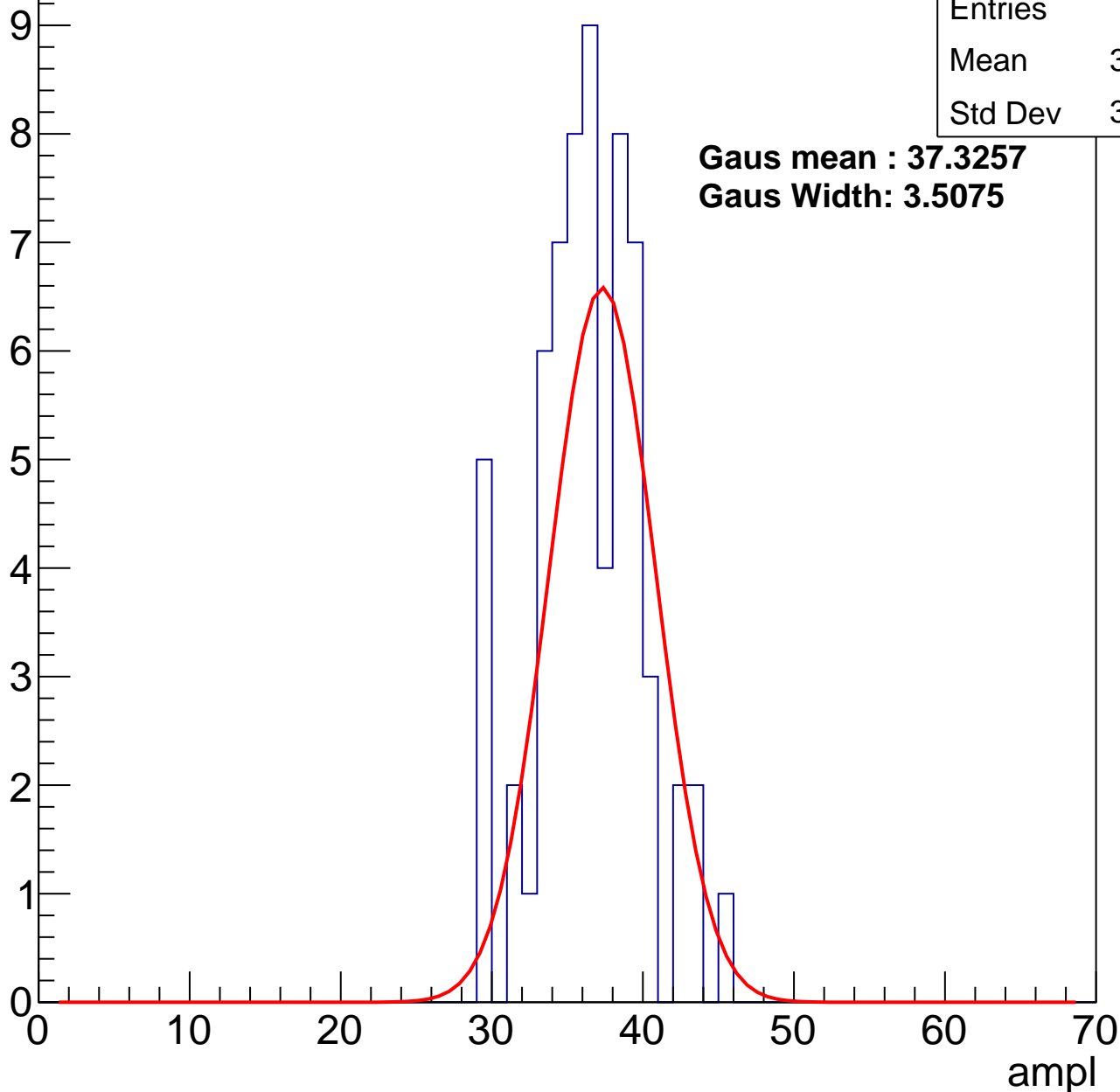
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	35.98
Std Dev	3.506

**Gaus mean : 37.3257**

**Gaus Width: 3.5075**



# B1L101S, U16-ch32, adc2

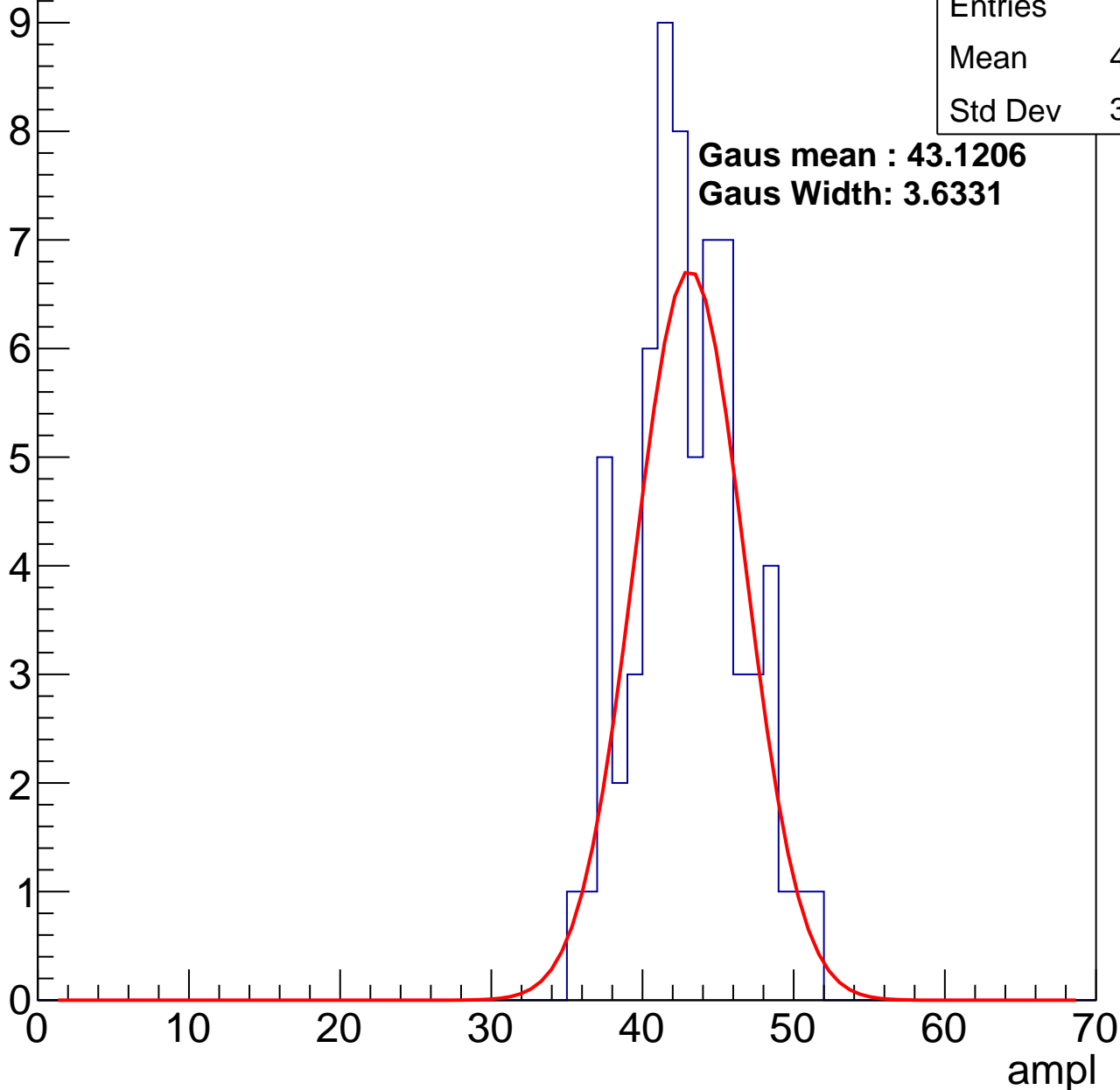
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	42.58
Std Dev	3.533

**Gaus mean : 43.1206**

**Gaus Width: 3.6331**

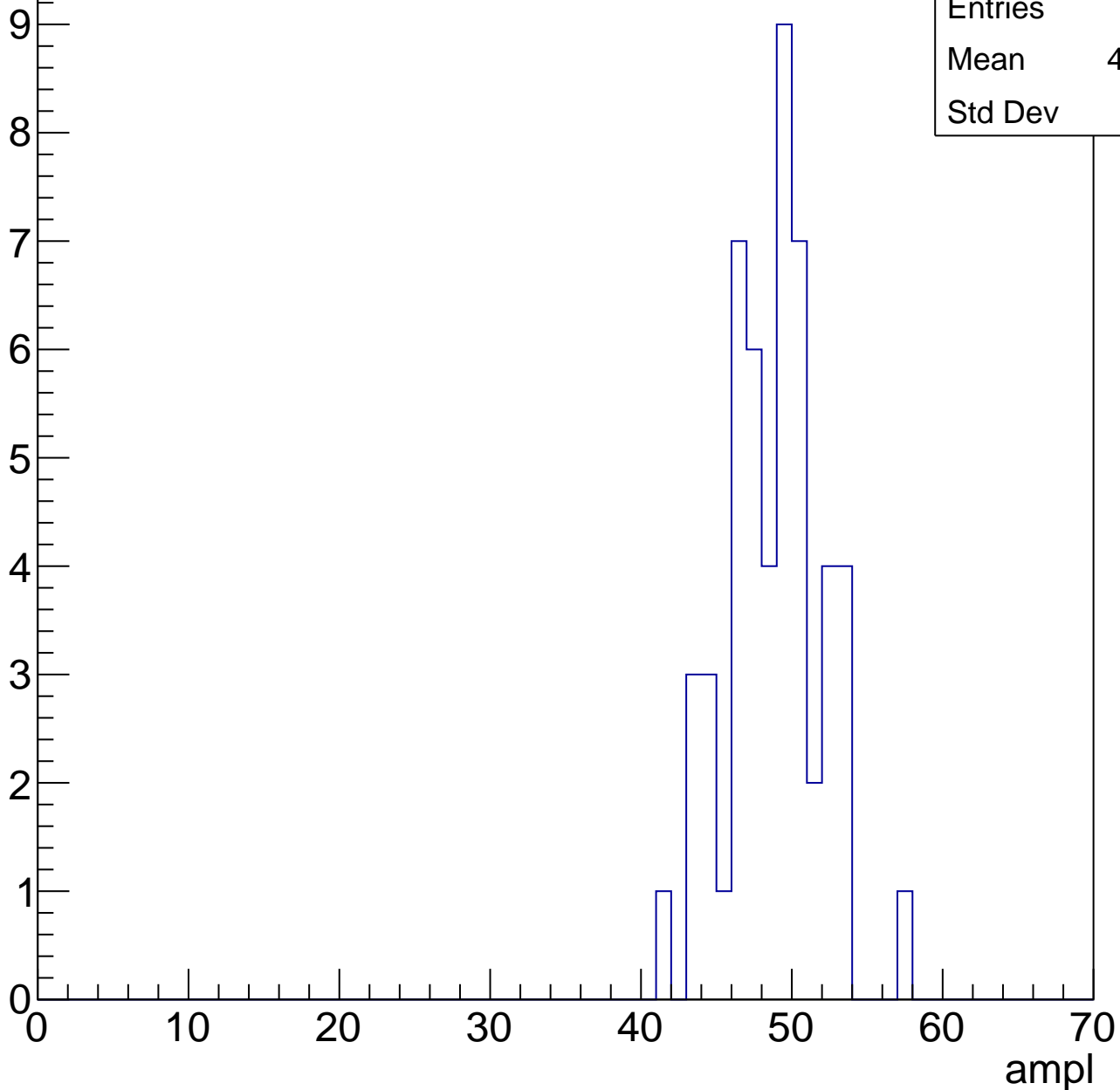


# B1L101S, U16-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	48.33
Std Dev	3.13



# B1L101S, U16-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	63
Mean	54.1
Std Dev	3.824

Entry

10

8

6

4

2

0

0

10

20

30

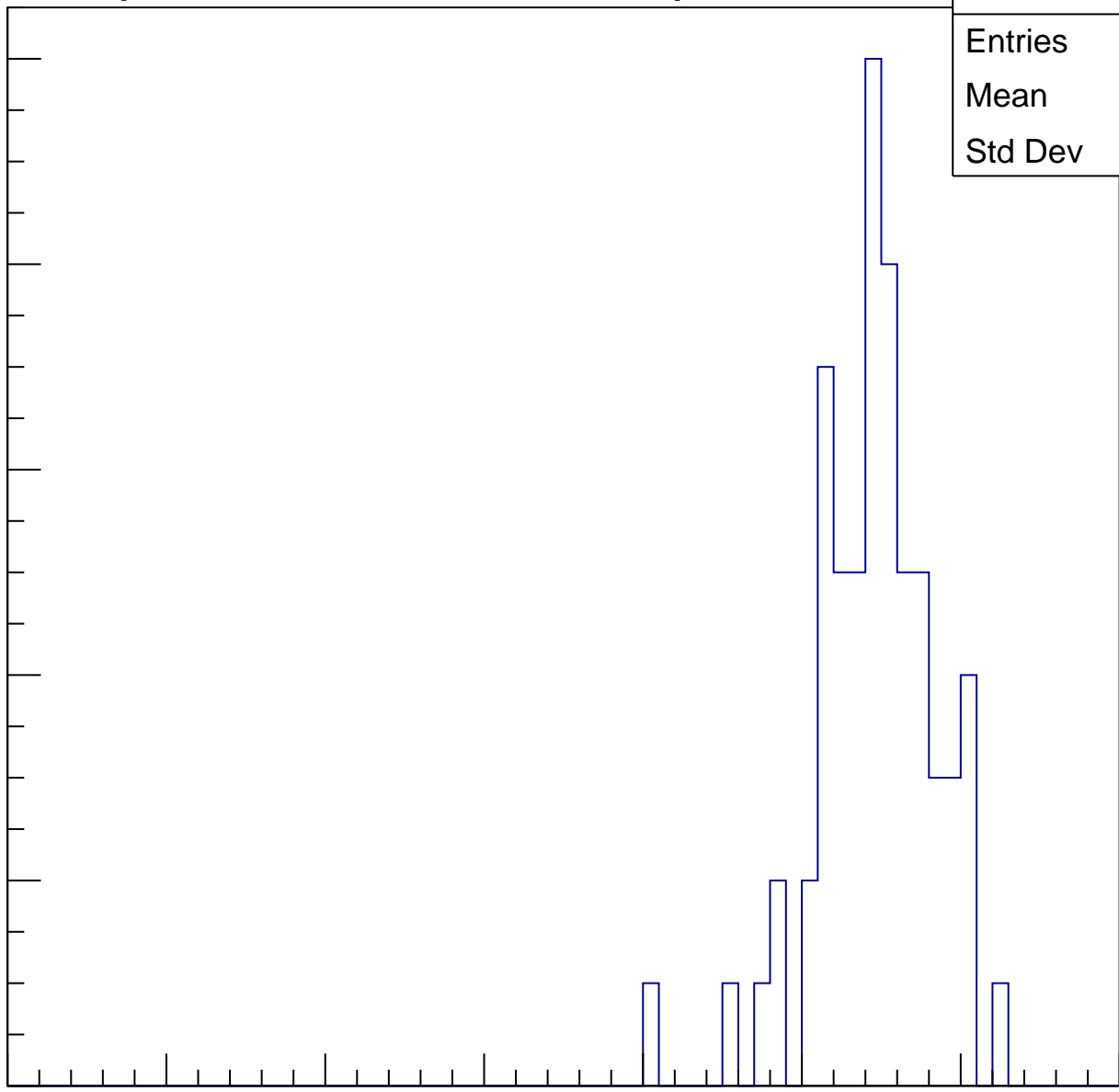
40

50

60

70

ampl

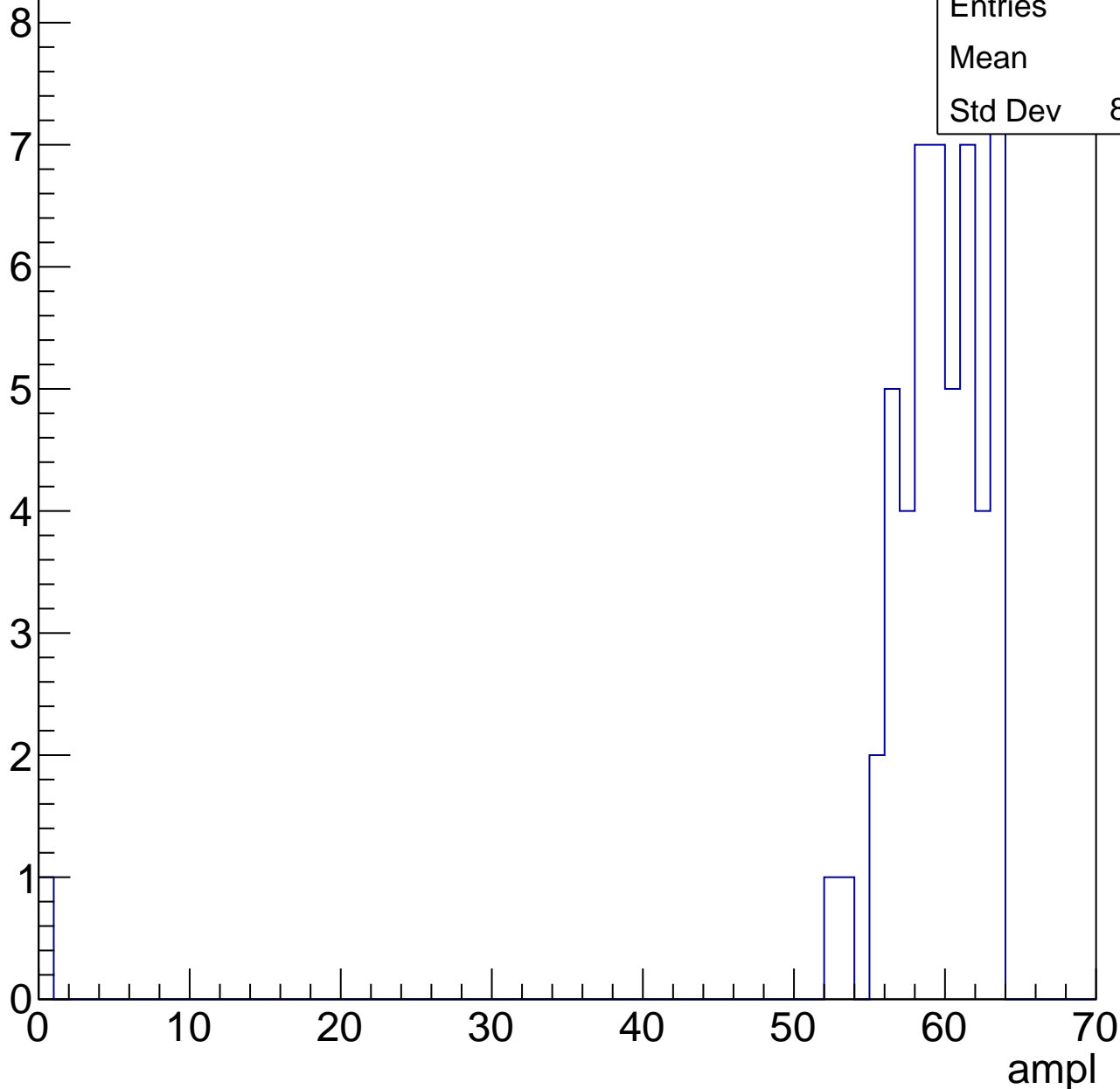


# B1L101S, U16-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	58.1
Std Dev	8.572

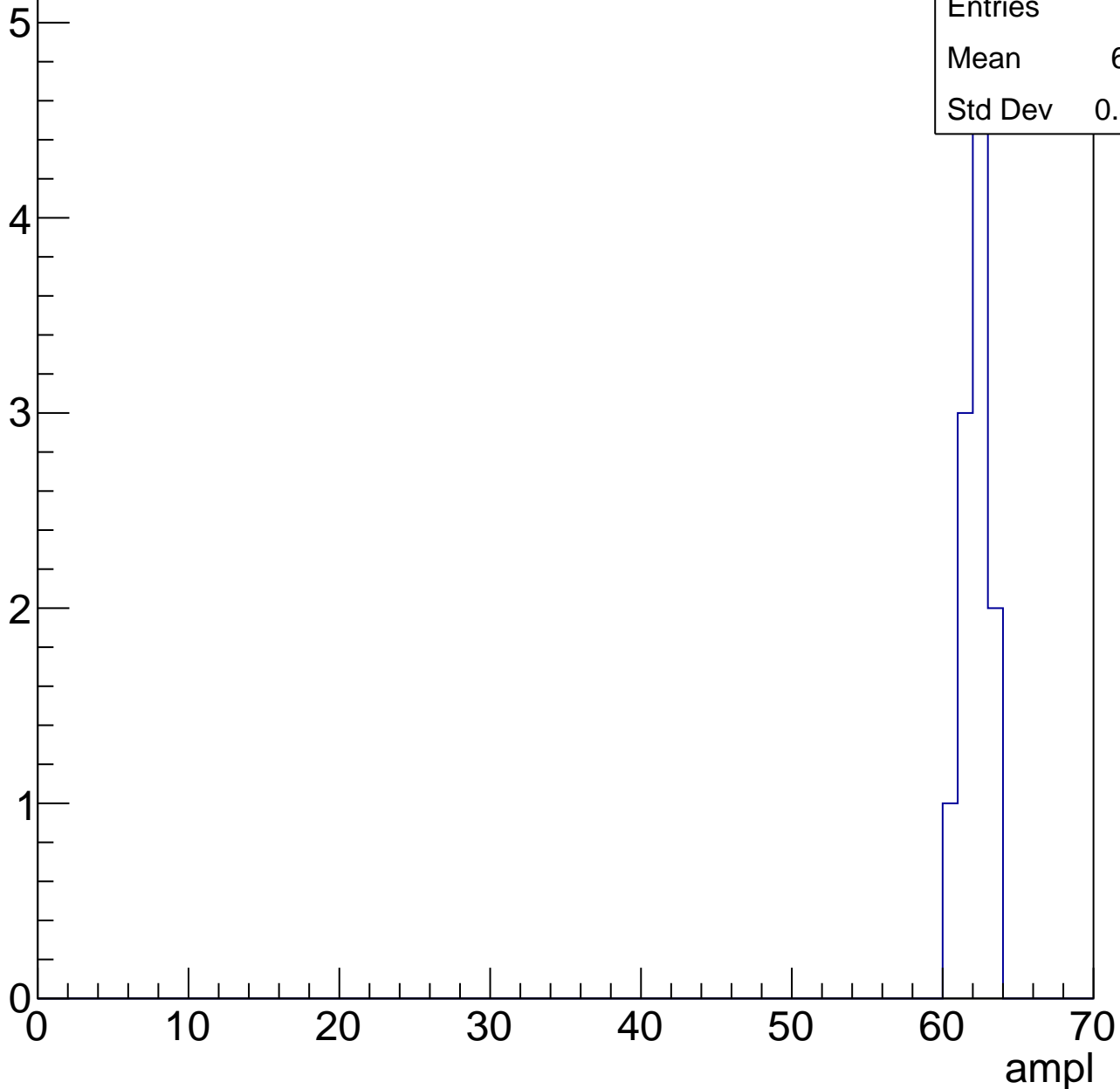


# B1L101S, U16-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	11
Mean	61.73
Std Dev	0.8624



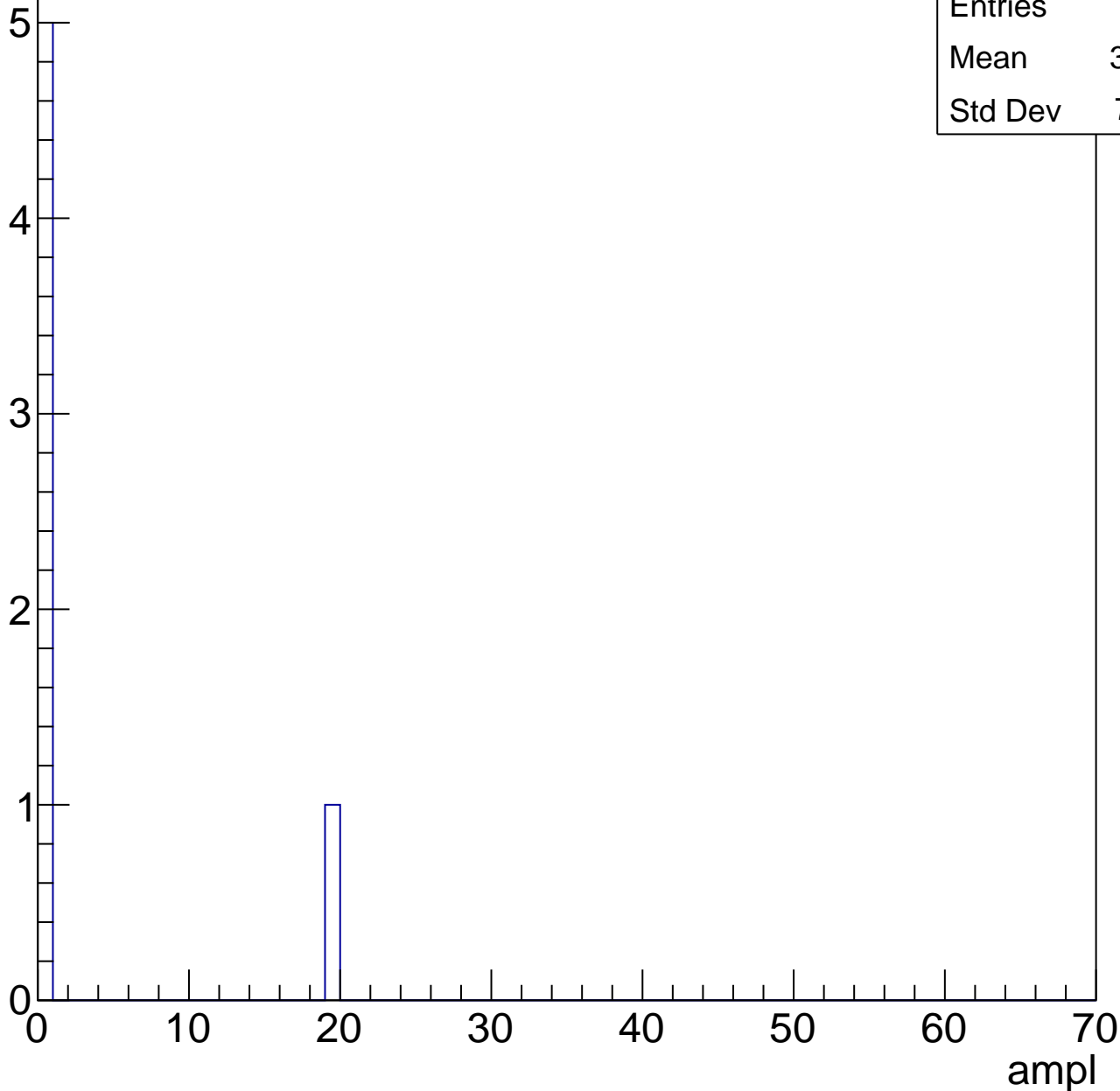


# B1L101S, U16-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	6
Mean	3.167
Std Dev	7.081



# B1L101S, U16-ch33, adc0

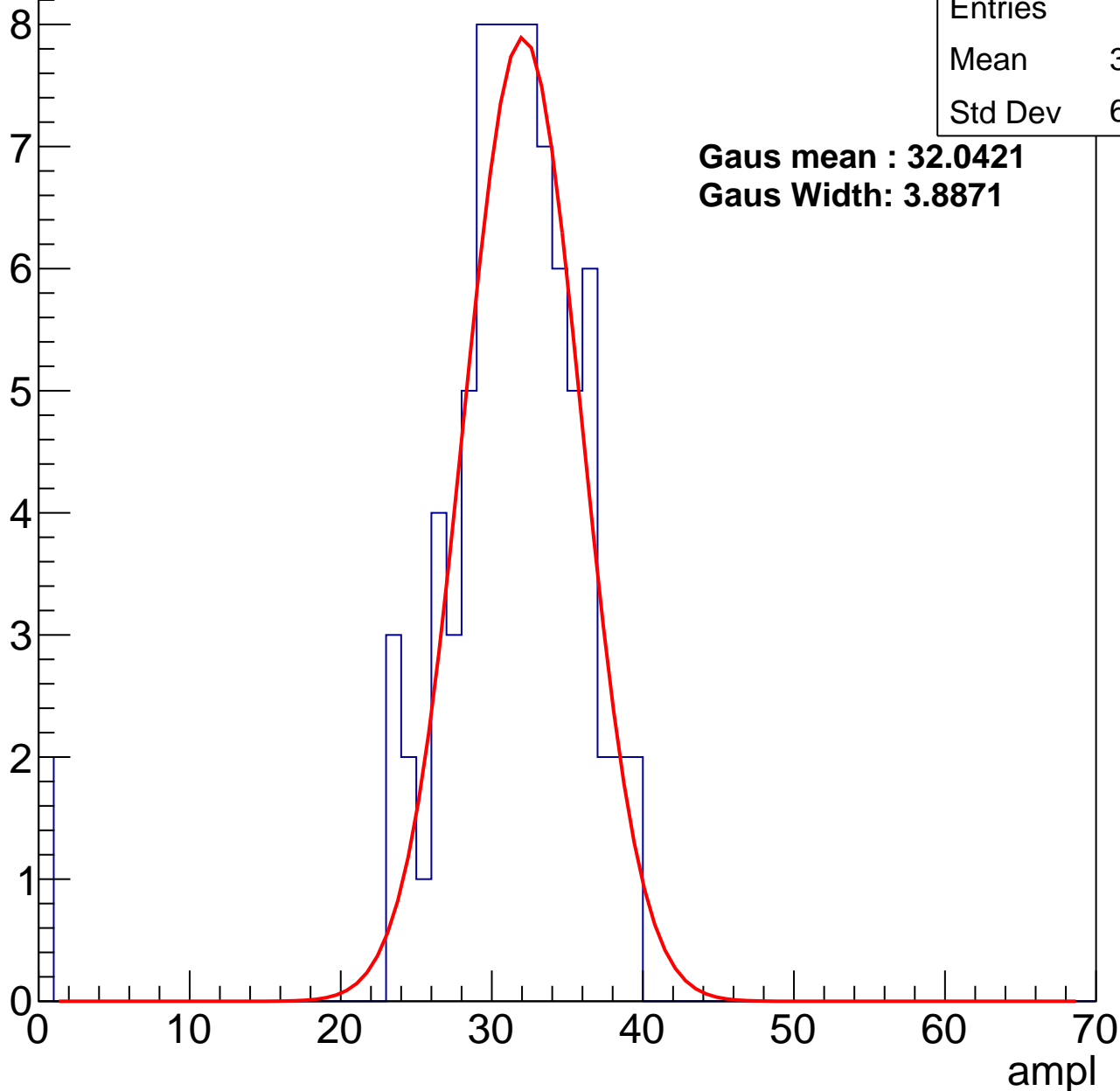
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	30.45
Std Dev	6.123

**Gaus mean : 32.0421**

**Gaus Width: 3.8871**



# B1L101S, U16-ch33, adc1

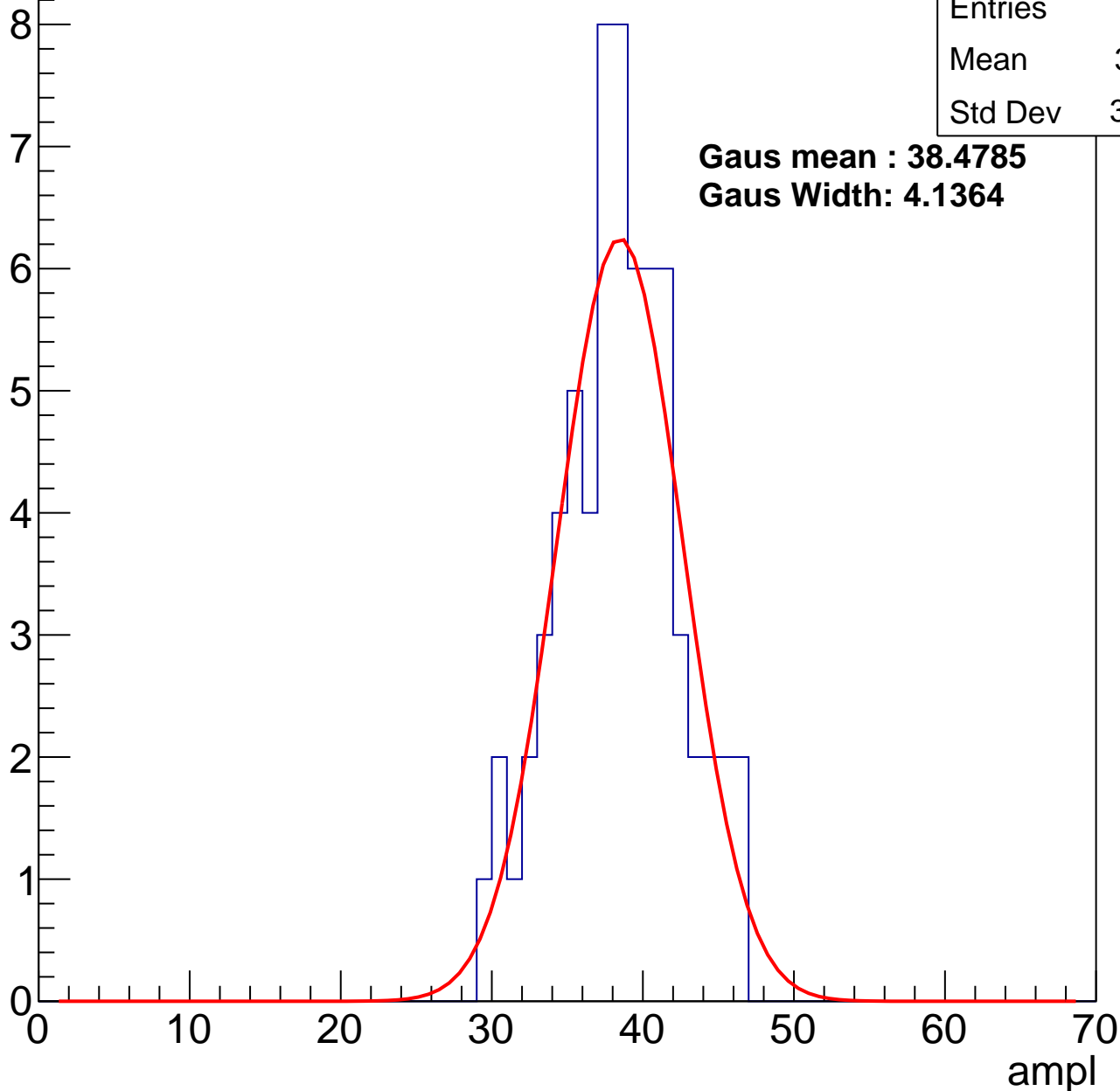
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	37.91
Std Dev	3.897

**Gaus mean : 38.4785**

**Gaus Width: 4.1364**



# B1L101S, U16-ch33, adc2

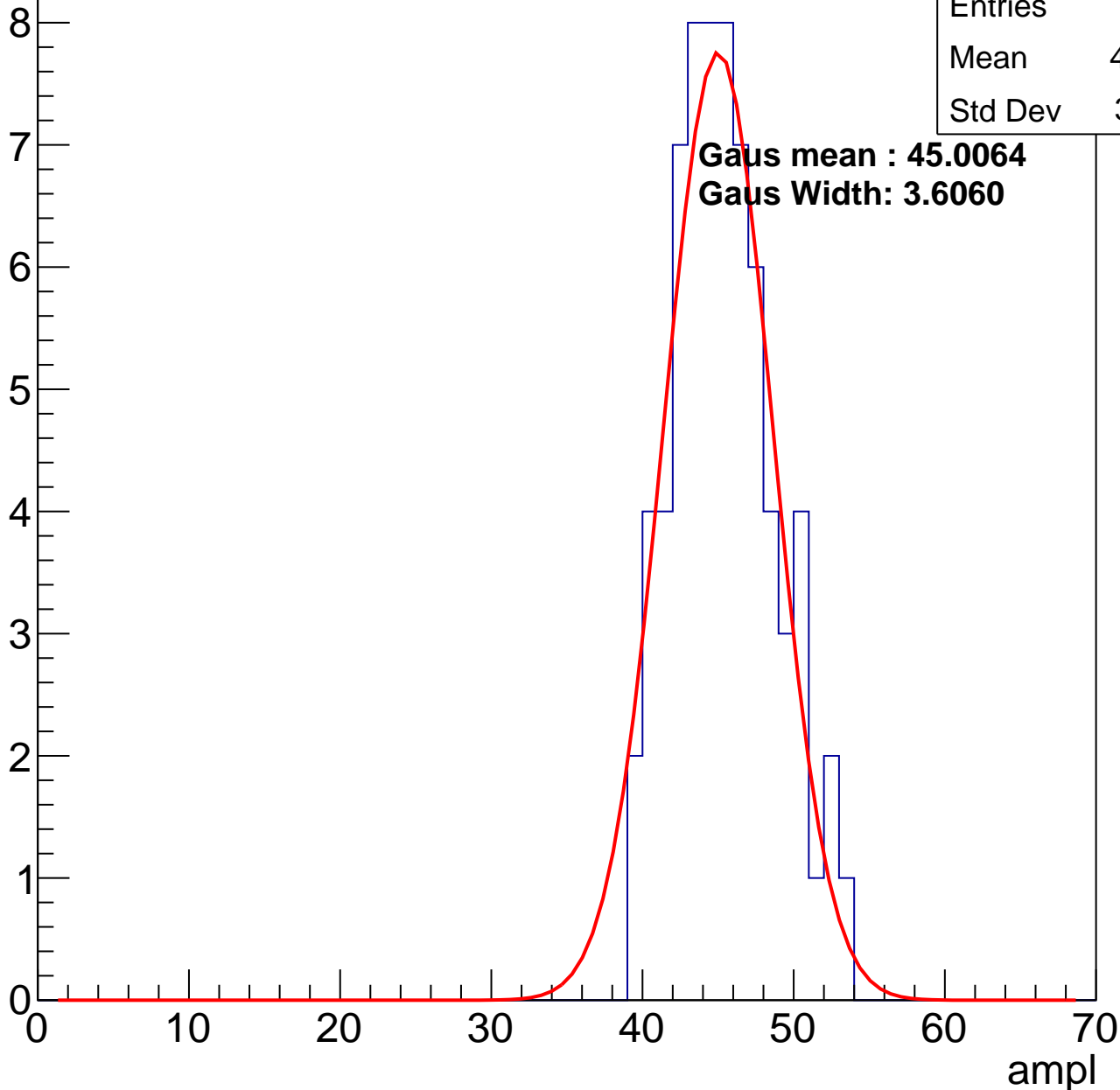
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	44.97
Std Dev	3.301

**Gaus mean : 45.0064**

**Gaus Width: 3.6060**

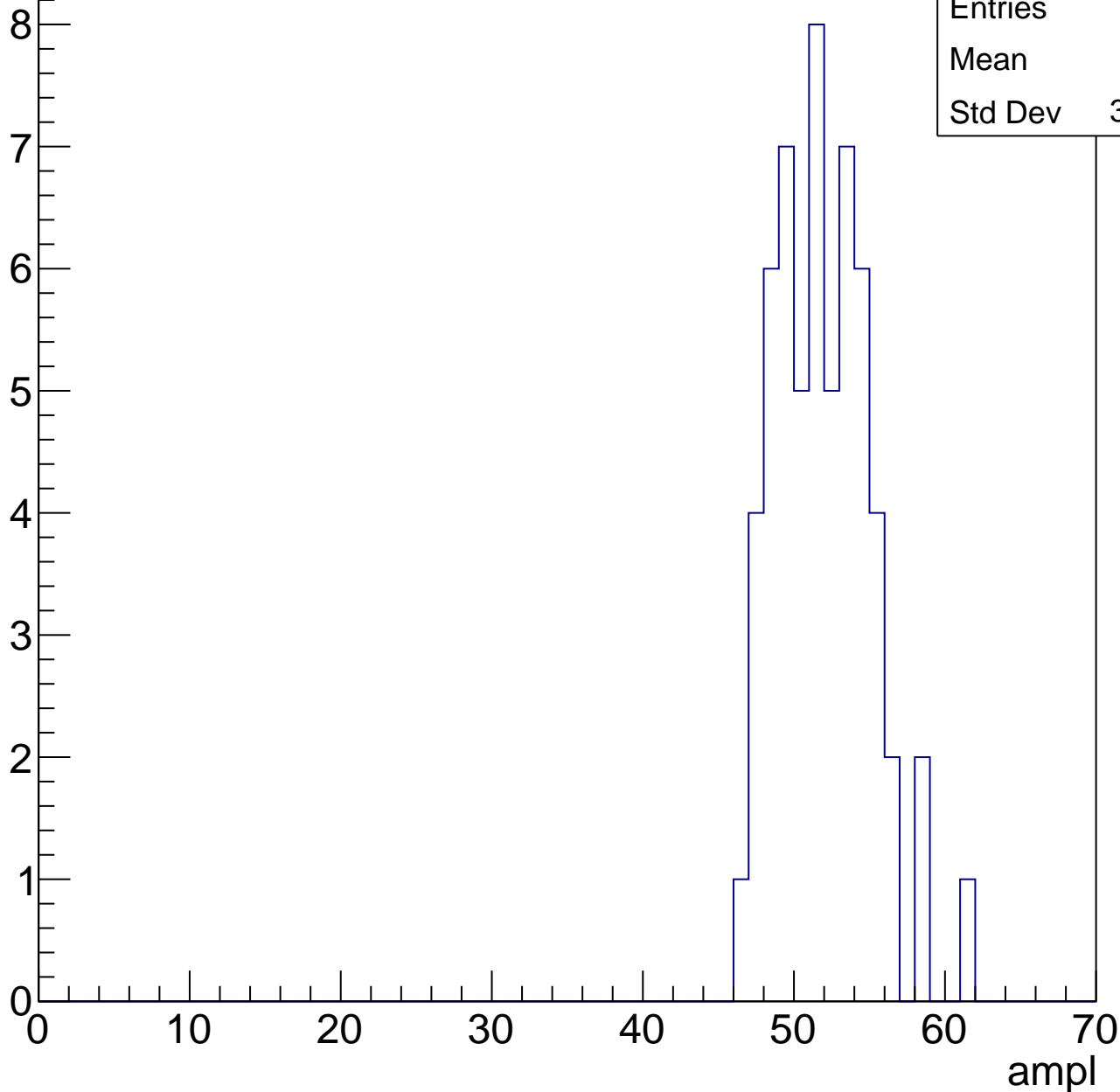


# B1L101S, U16-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	51.5
Std Dev	3.109

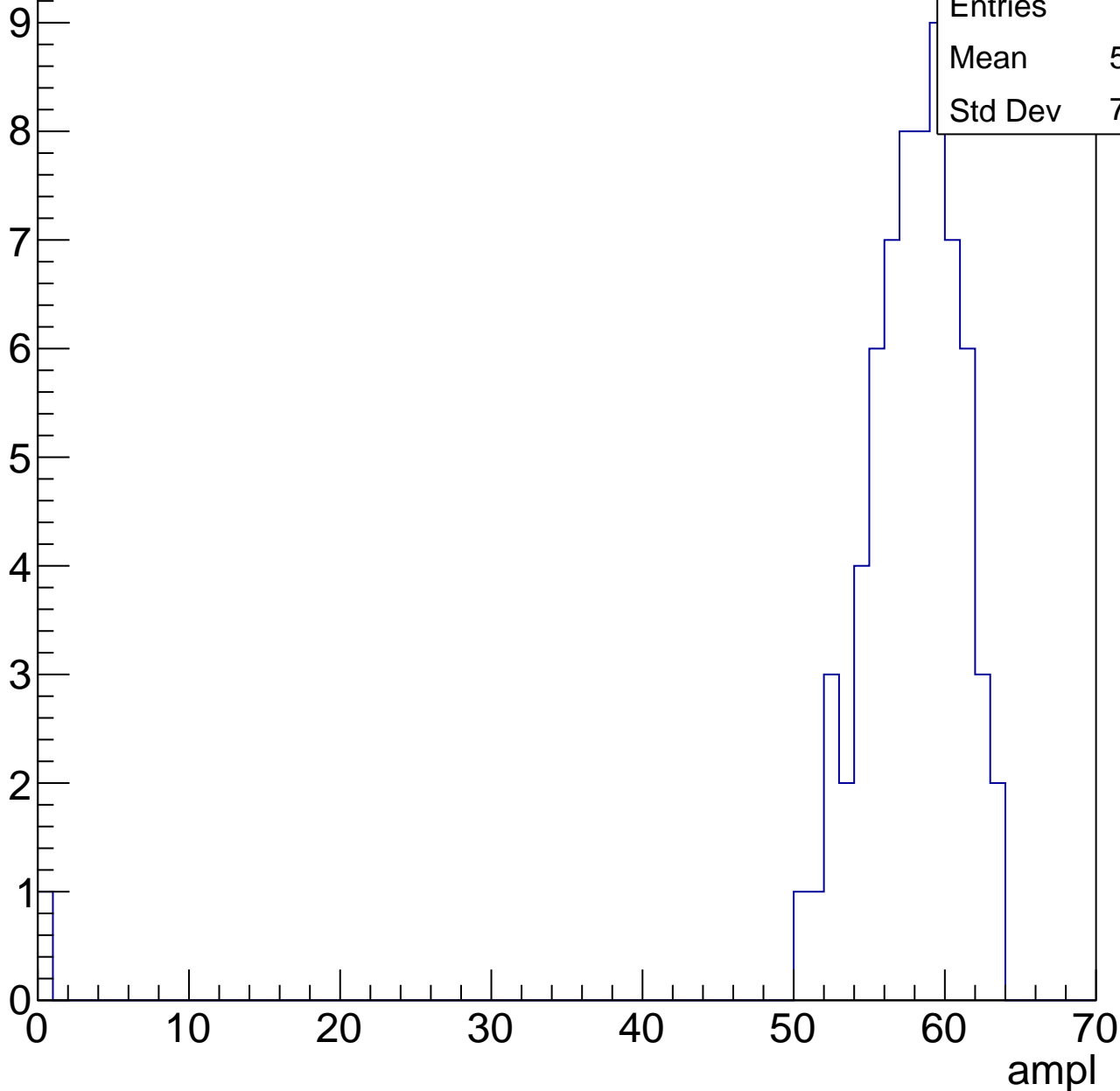


# B1L101S, U16-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

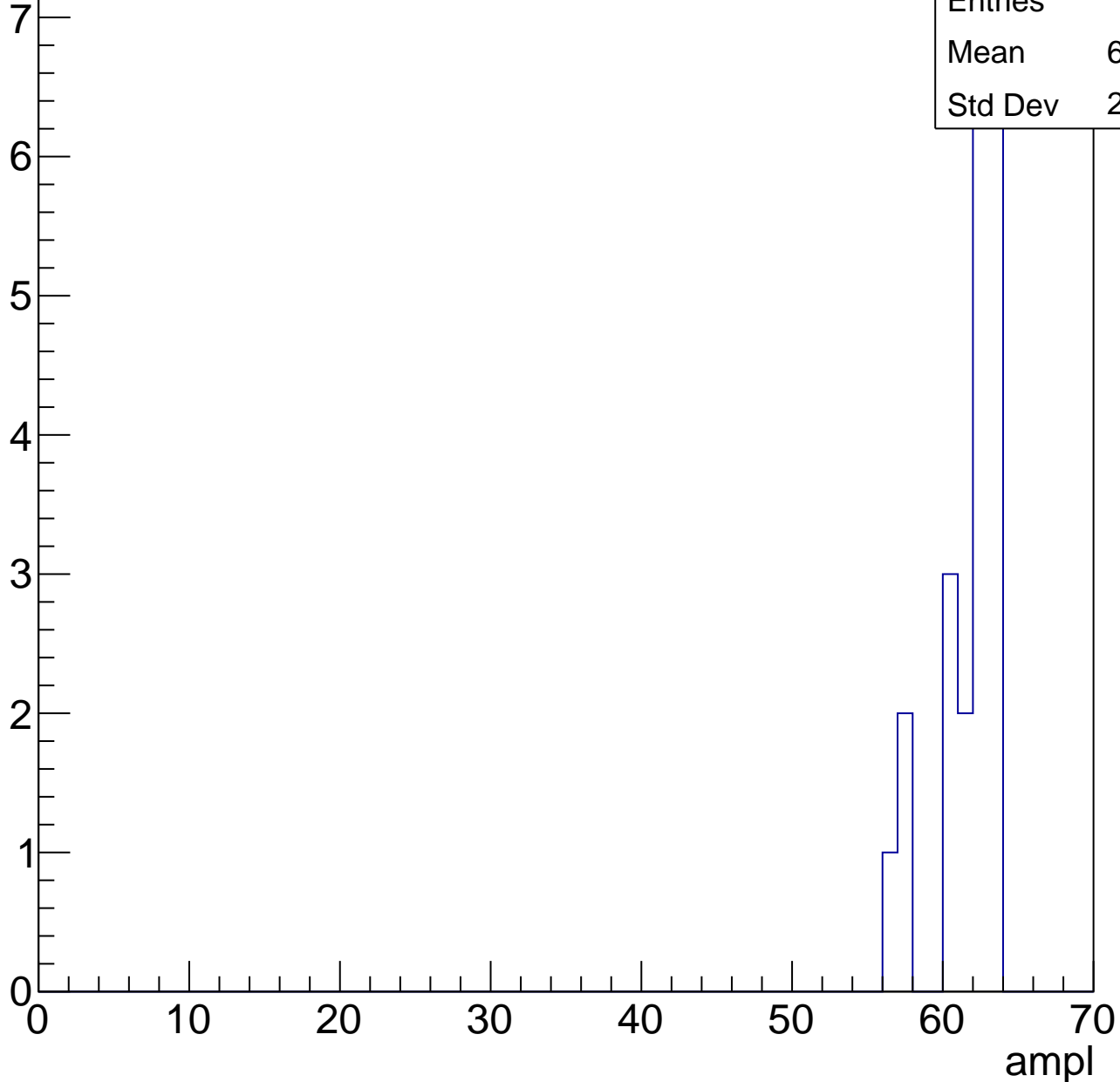
Entries	68
Mean	56.62
Std Dev	7.523



# B1L101S, U16-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

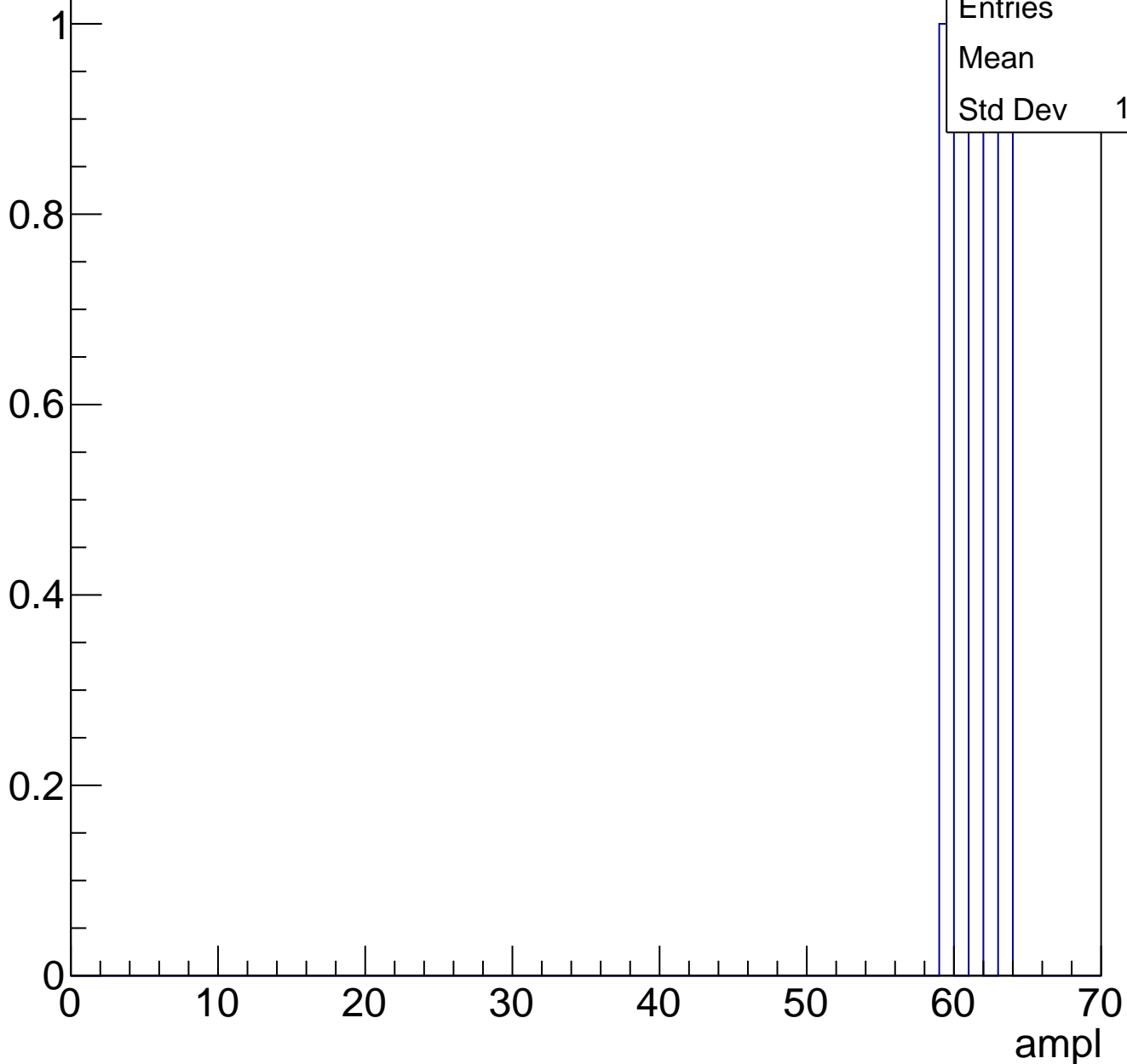


Entries	22
Mean	61.23
Std Dev	2.066

# B1L101S, U16-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch34, adc0

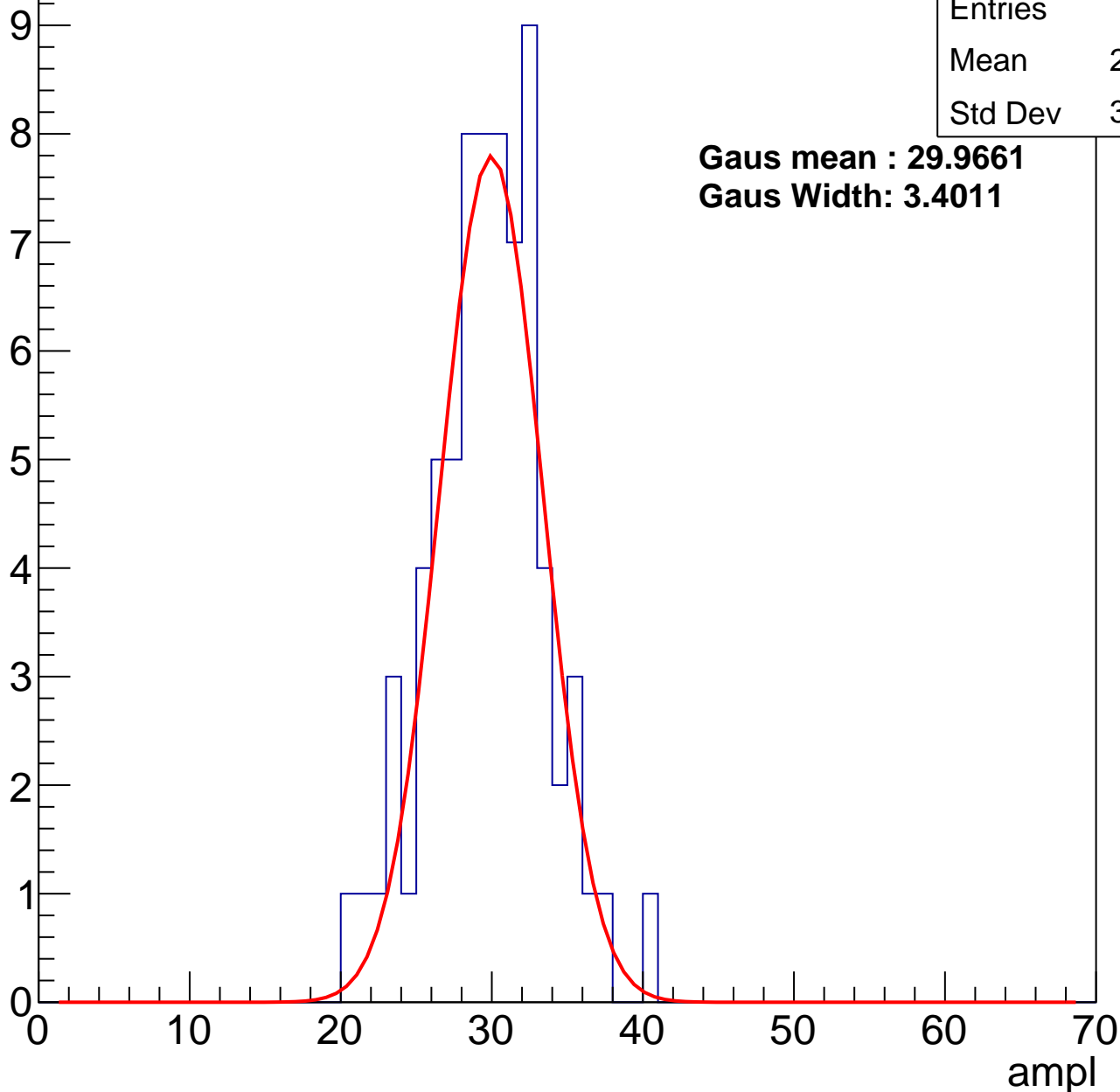
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	29.32
Std Dev	3.756

**Gaus mean : 29.9661**

**Gaus Width: 3.4011**



# B1L101S, U16-ch34, adc1

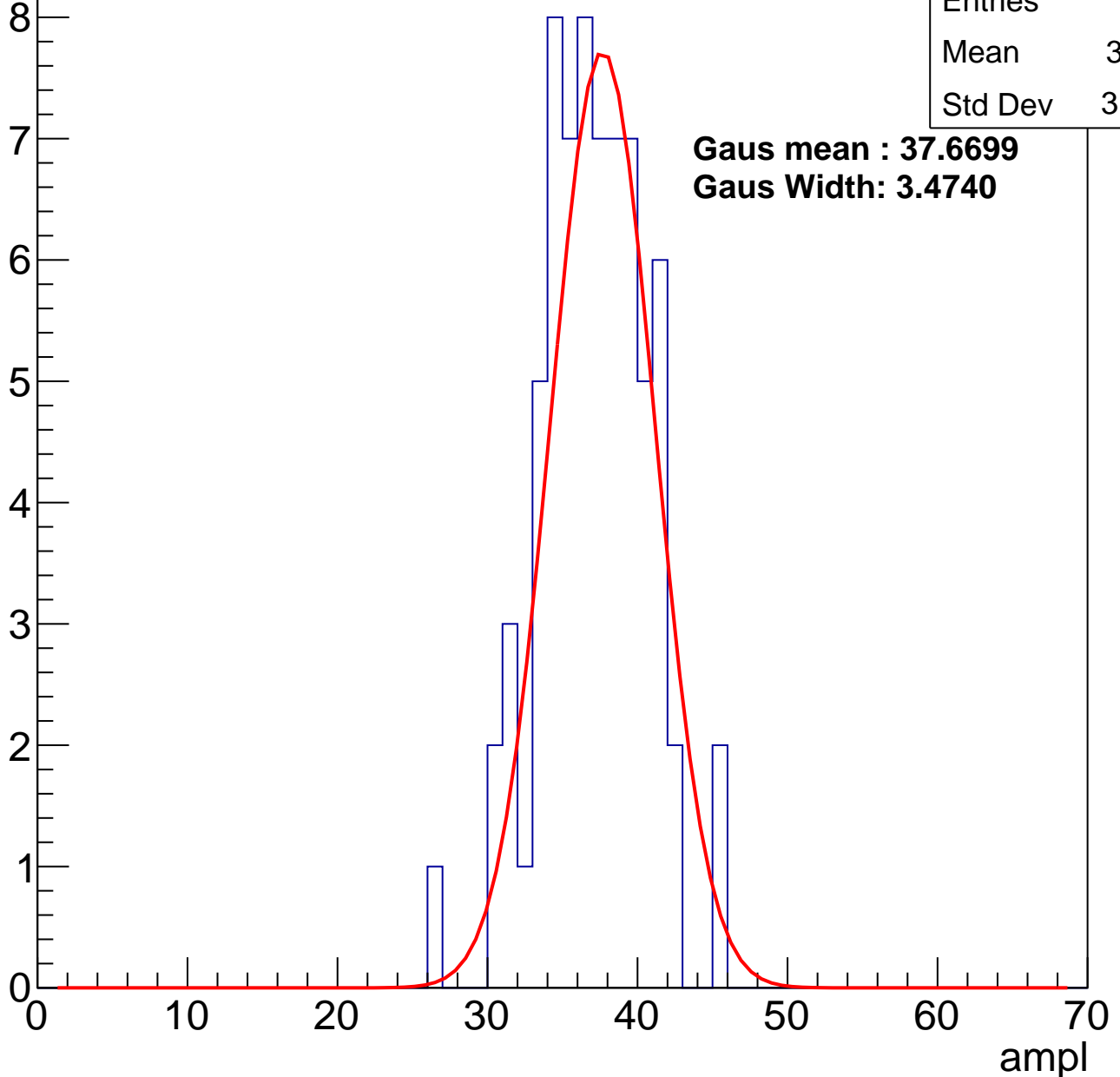
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	36.61
Std Dev	3.526

**Gaus mean : 37.6699**

**Gaus Width: 3.4740**



# B1L101S, U16-ch34, adc2

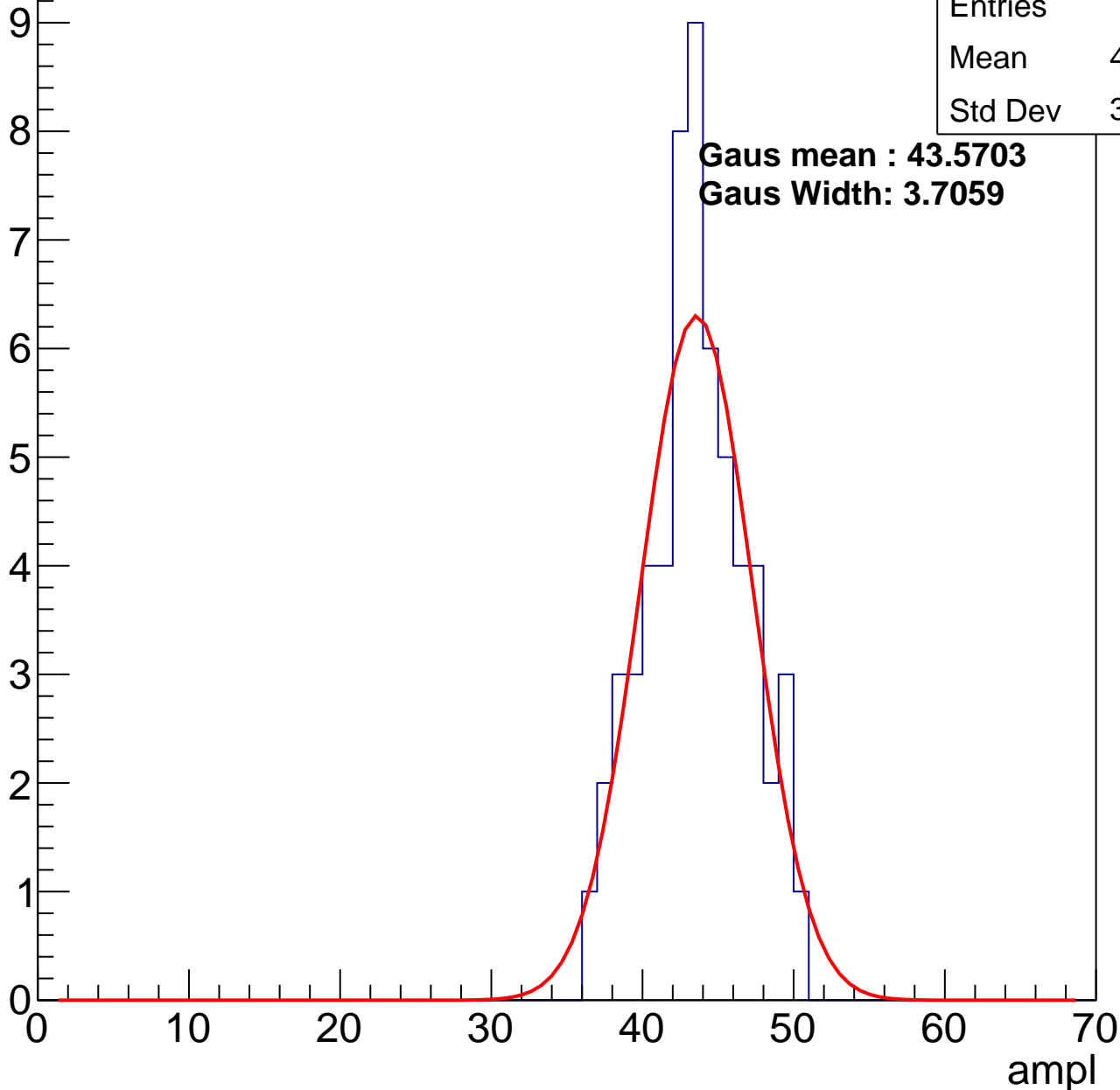
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	43.08
Std Dev	3.285

**Gaus mean : 43.5703**

**Gaus Width: 3.7059**

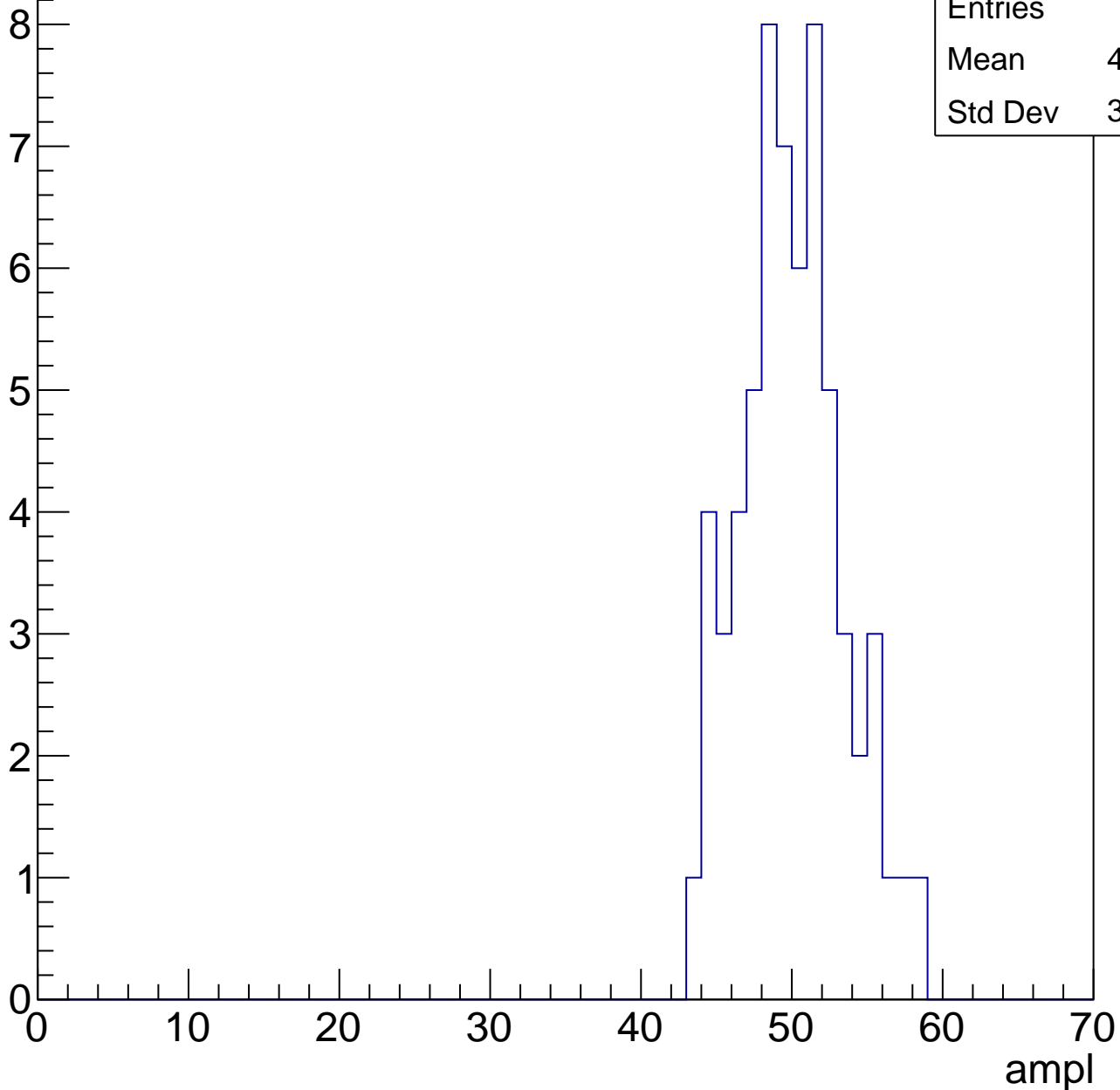


# B1L101S, U16-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	49.53
Std Dev	3.392

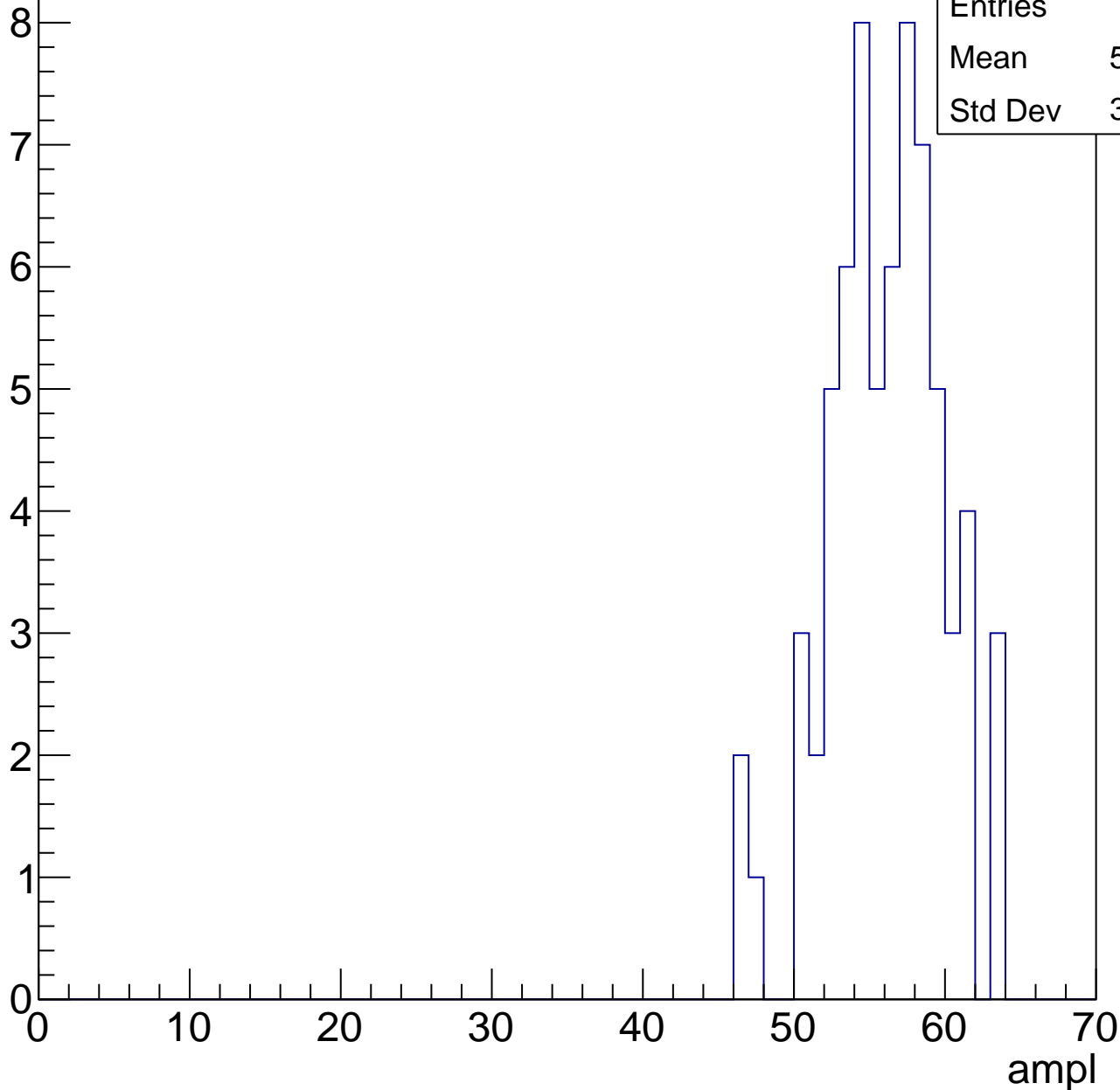


# B1L101S, U16-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	55.62
Std Dev	3.789

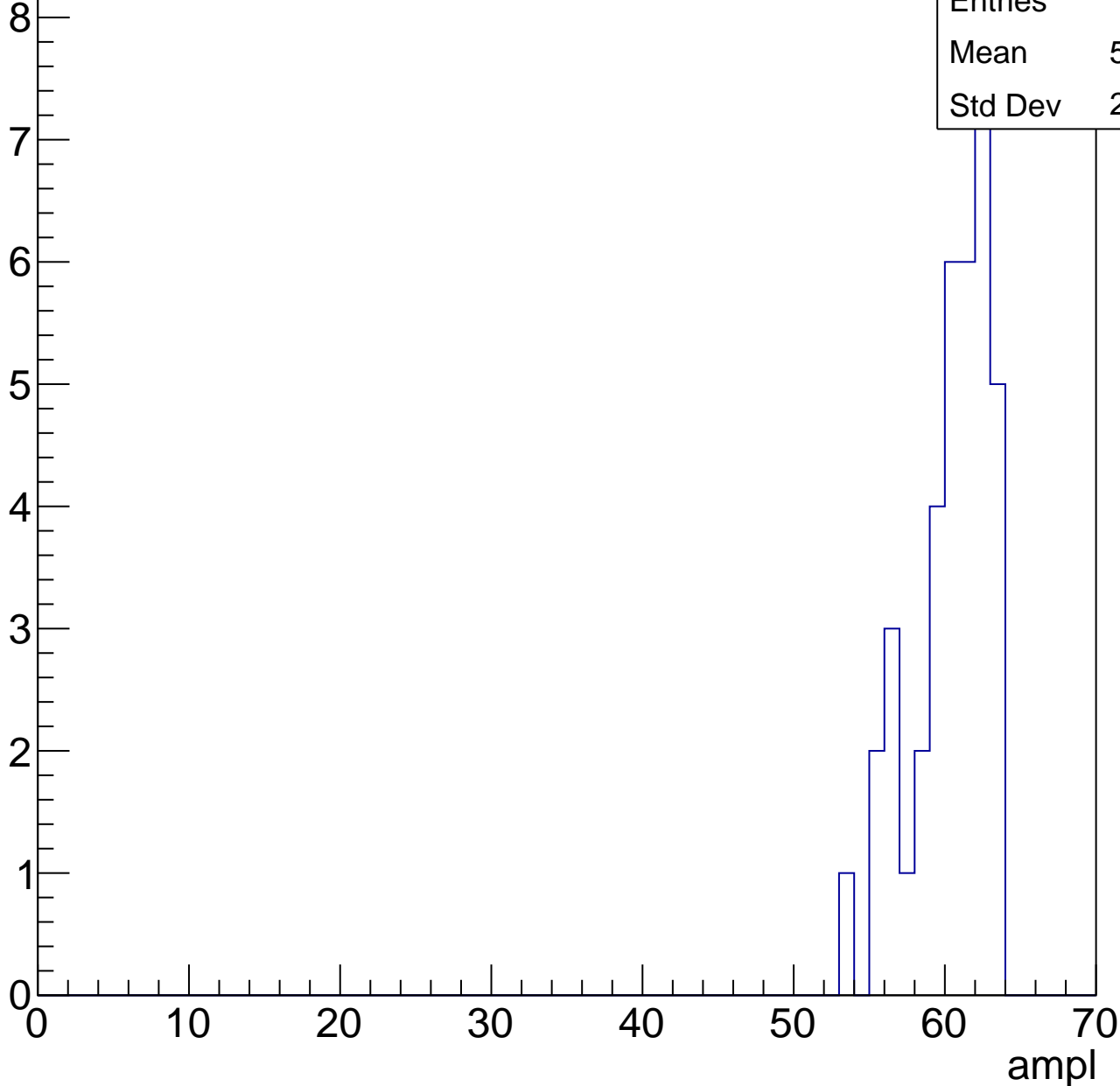


# B1L101S, U16-ch34, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	38
Mean	59.92
Std Dev	2.569



# B1L101S, U16-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

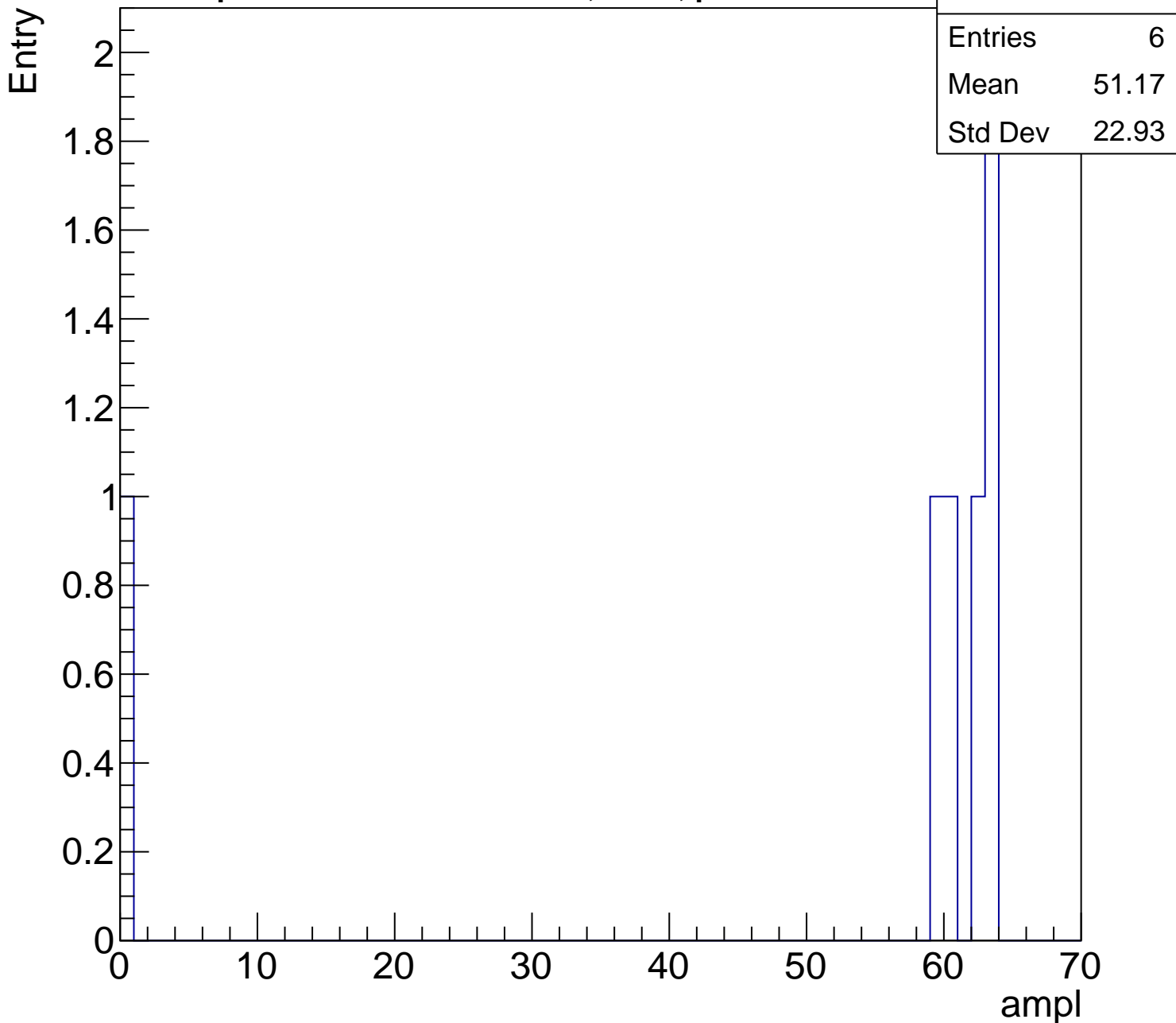
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	51.17
Std Dev	22.93

0 10 20 30 40 50 60 70

ampl





# B1L101S, U16-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch35, adc0

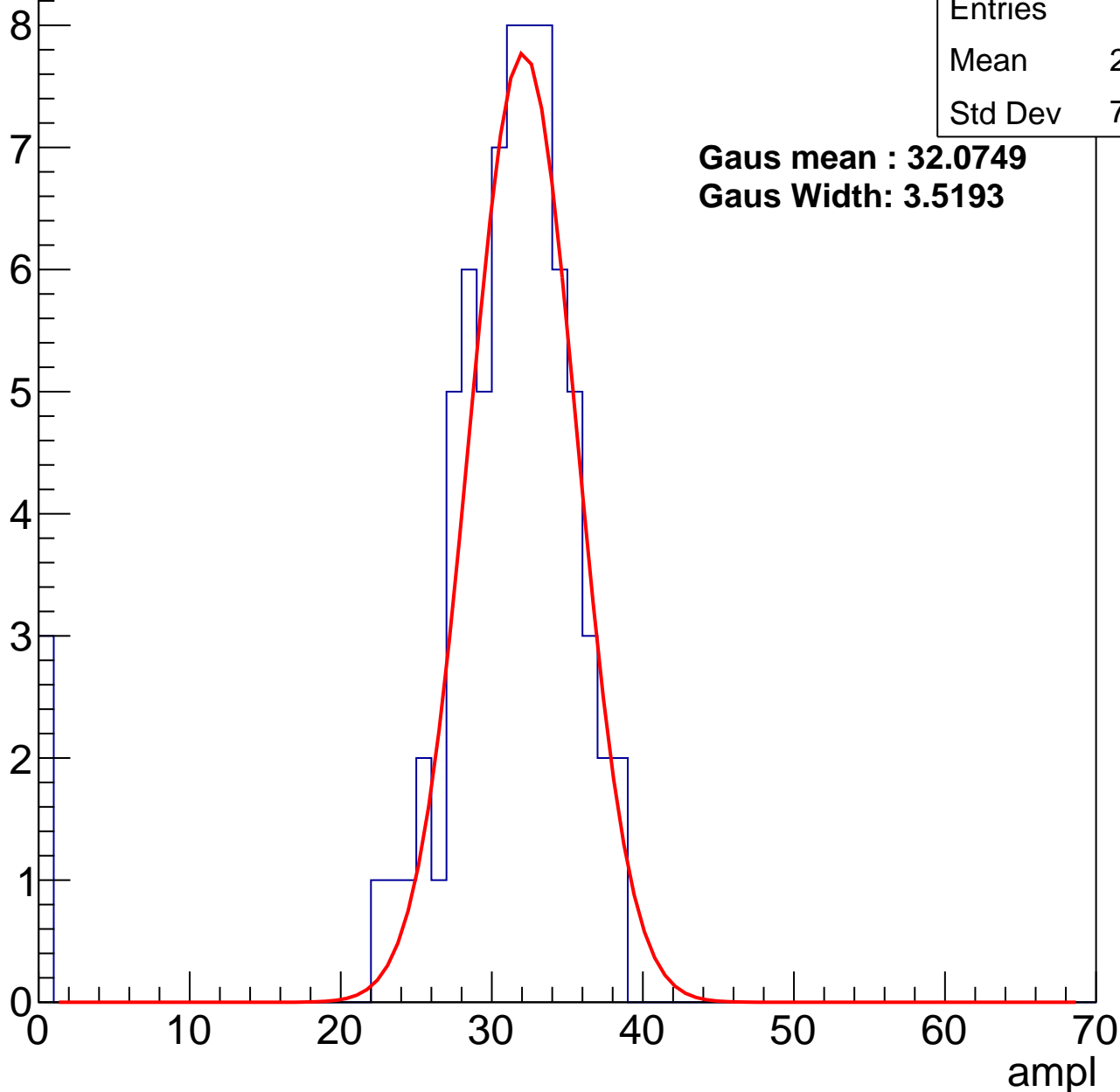
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	29.84
Std Dev	7.027

**Gaus mean : 32.0749**

**Gaus Width: 3.5193**



# B1L101S, U16-ch35, adc1

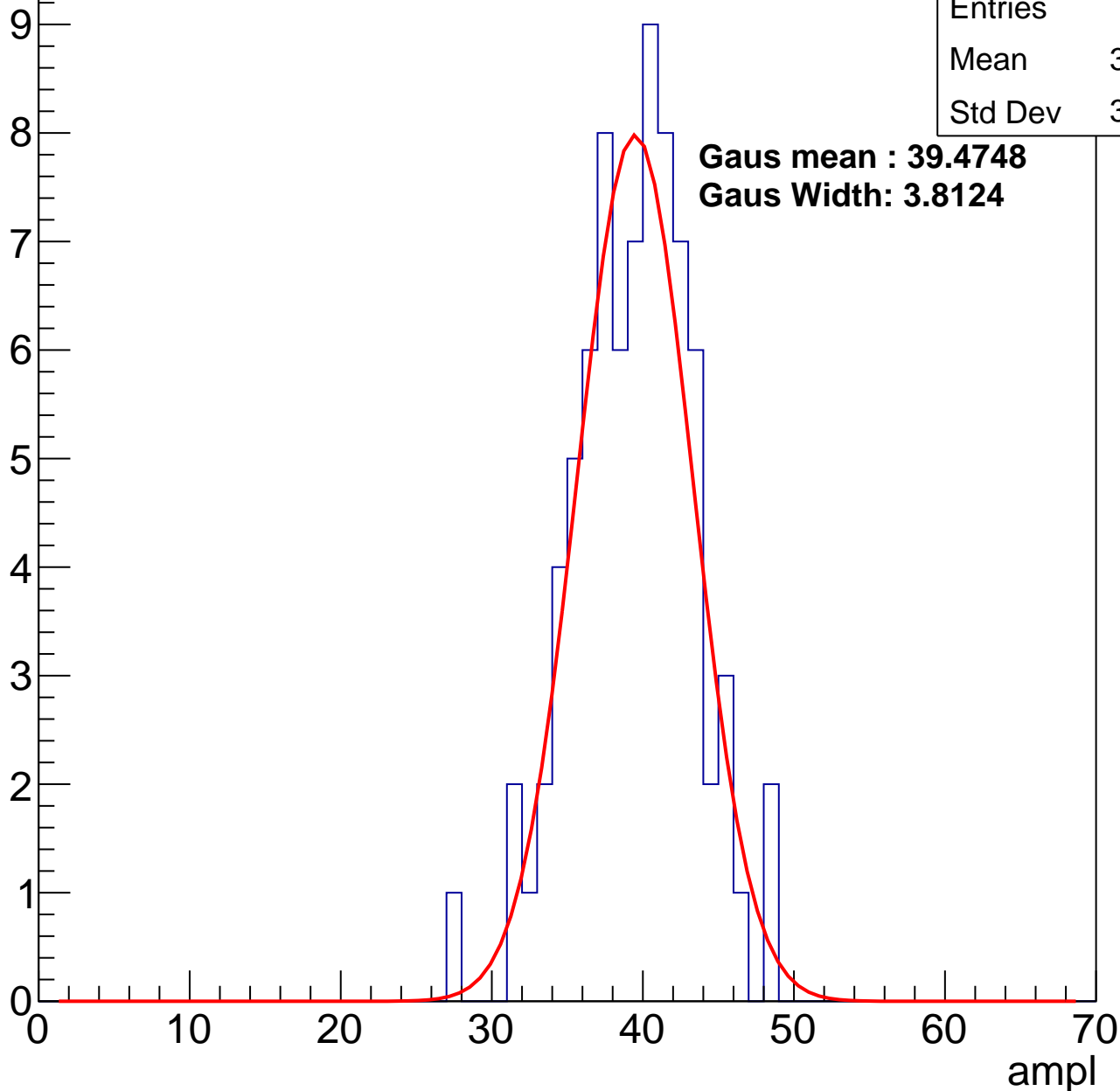
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	38.95
Std Dev	3.927

**Gaus mean : 39.4748**

**Gaus Width: 3.8124**



# B1L101S, U16-ch35, adc2

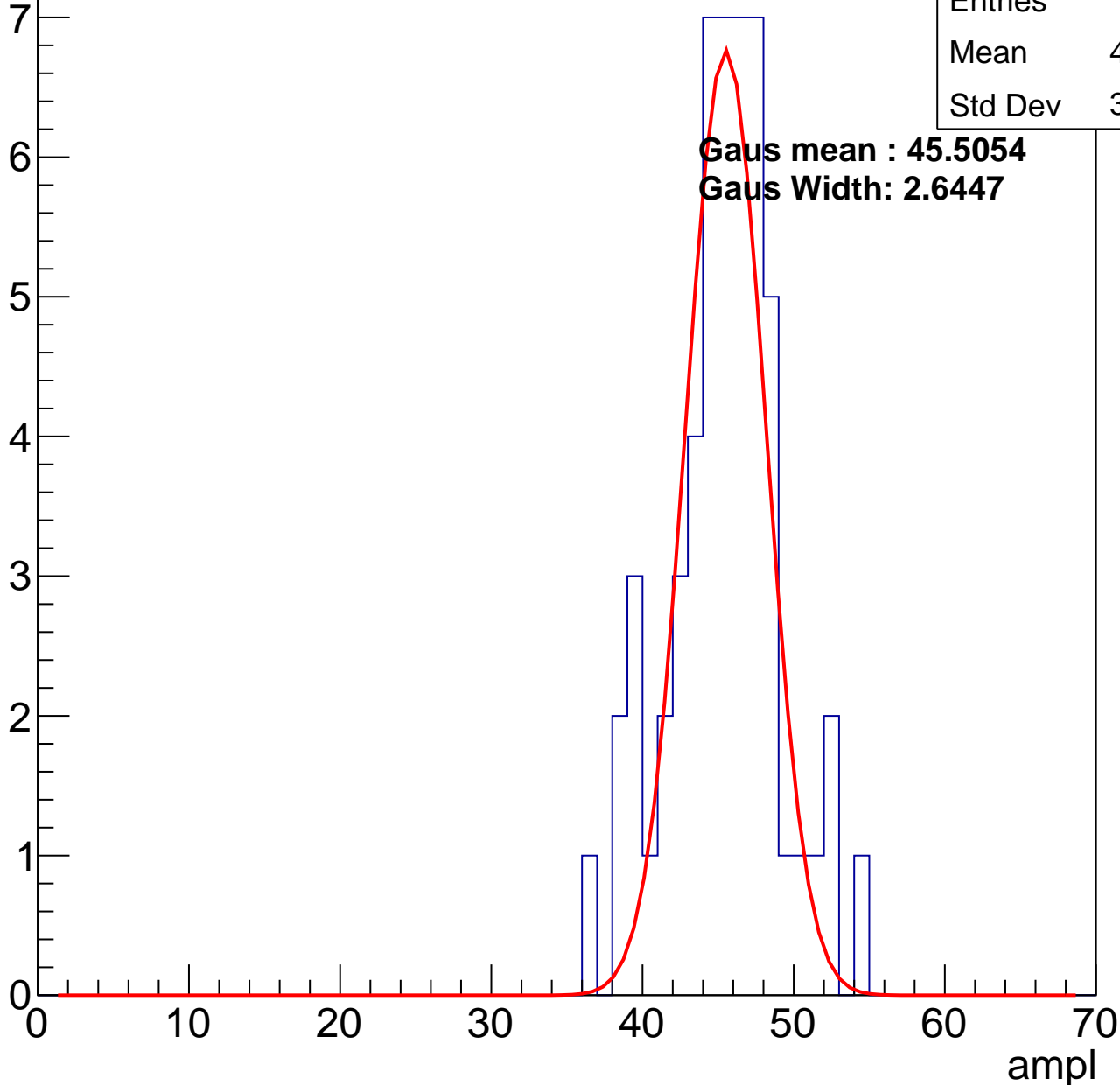
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	44.93
Std Dev	3.642

**Gaus mean : 45.5054**

**Gaus Width: 2.6447**

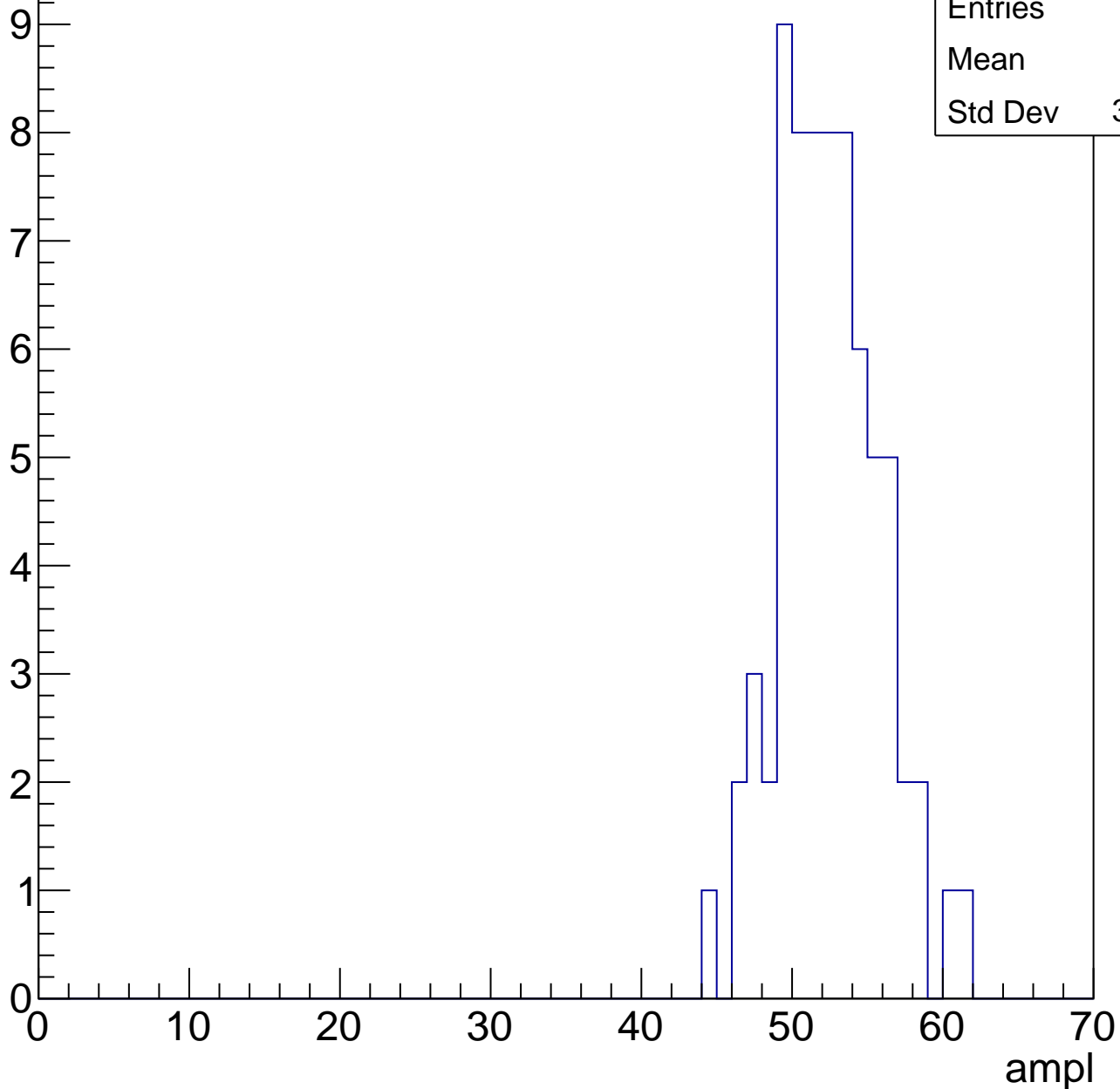


# B1L101S, U16-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

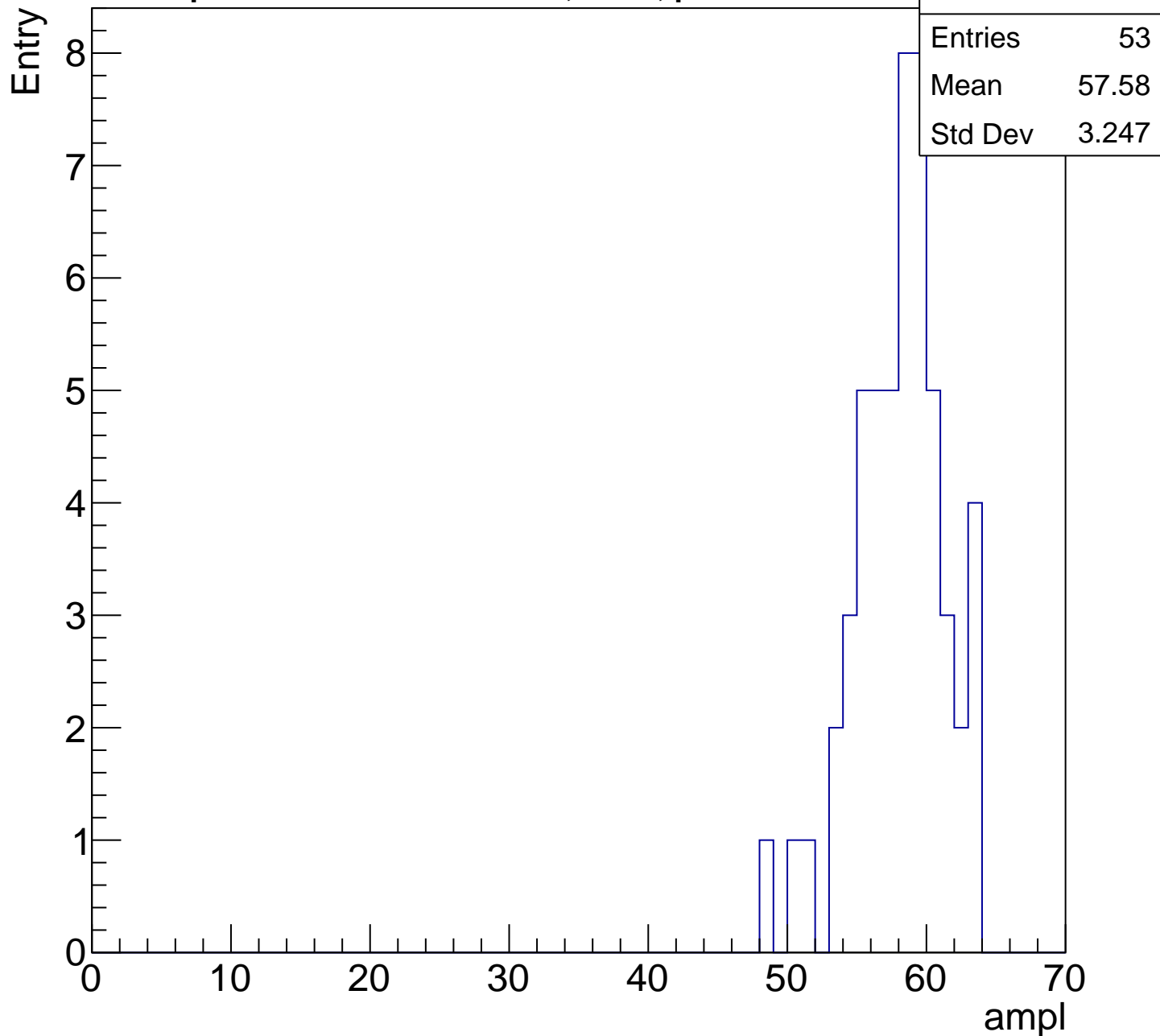
Entry

Entries	71
Mean	52
Std Dev	3.331



# B1L101S, U16-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

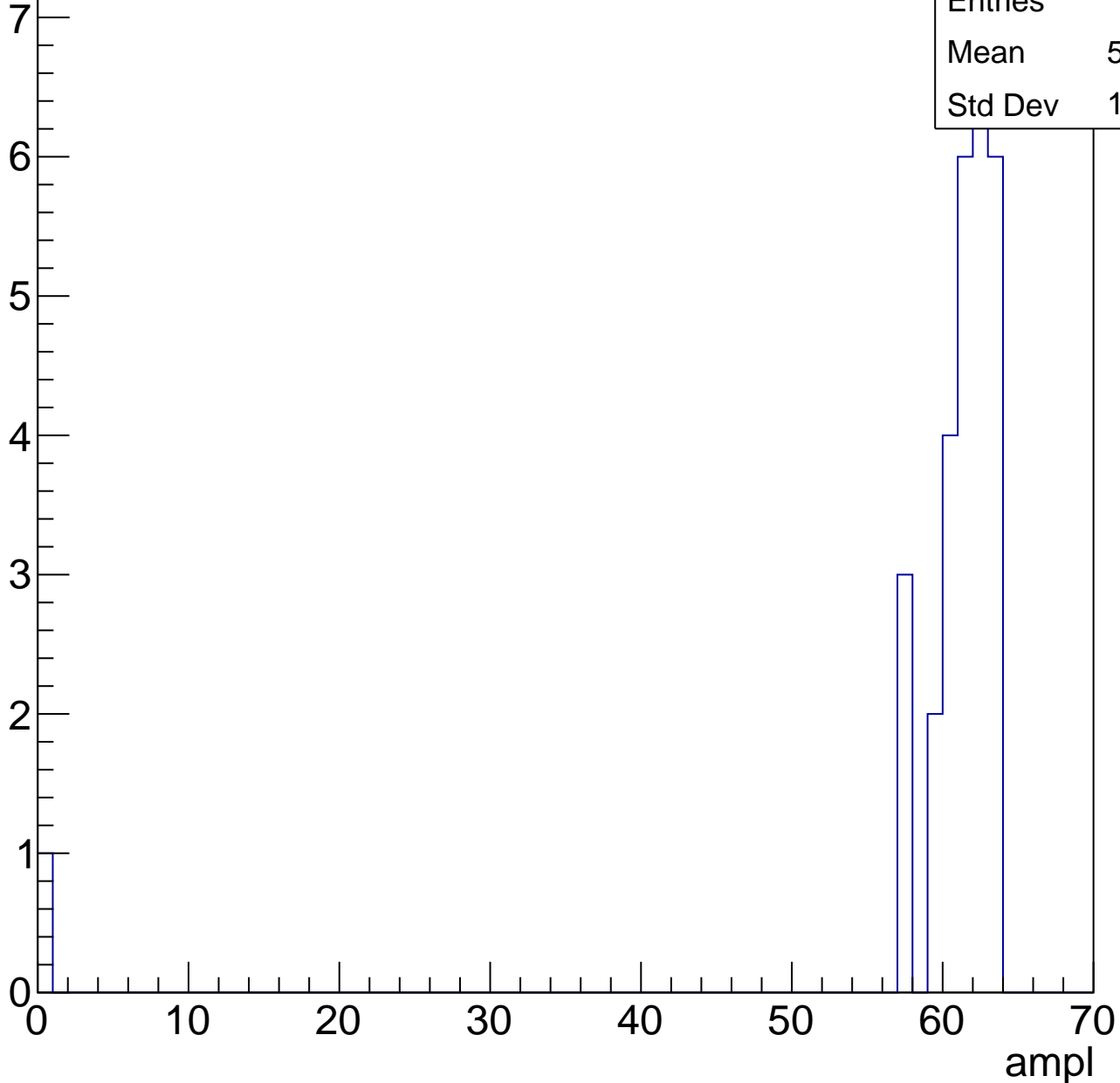


# B1L101S, U16-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	29
Mean	58.86
Std Dev	11.26



# B1L101S, U16-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch36, adc0

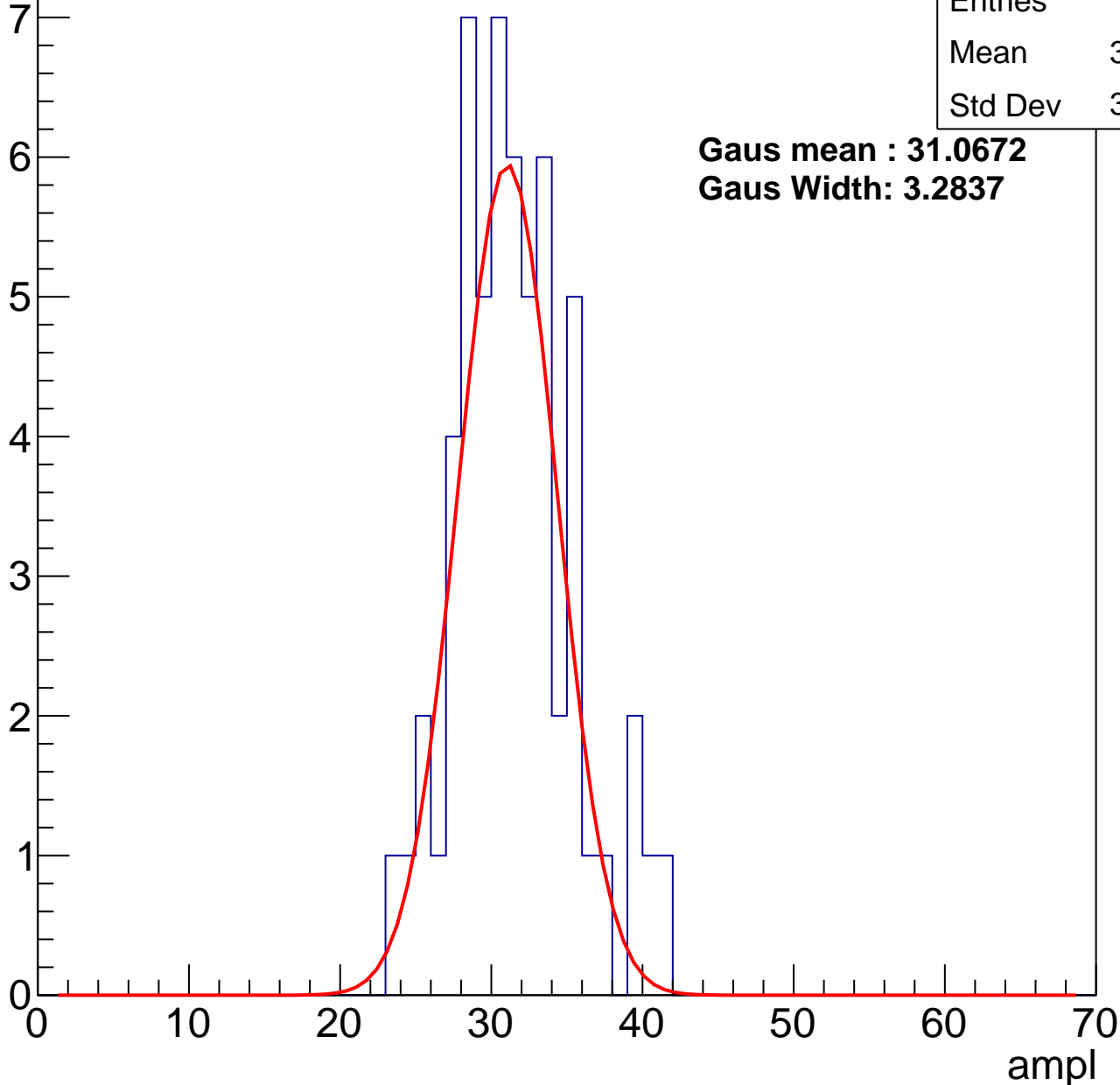
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	31.05
Std Dev	3.853

**Gaus mean : 31.0672**

**Gaus Width: 3.2837**



# B1L101S, U16-ch36, adc1

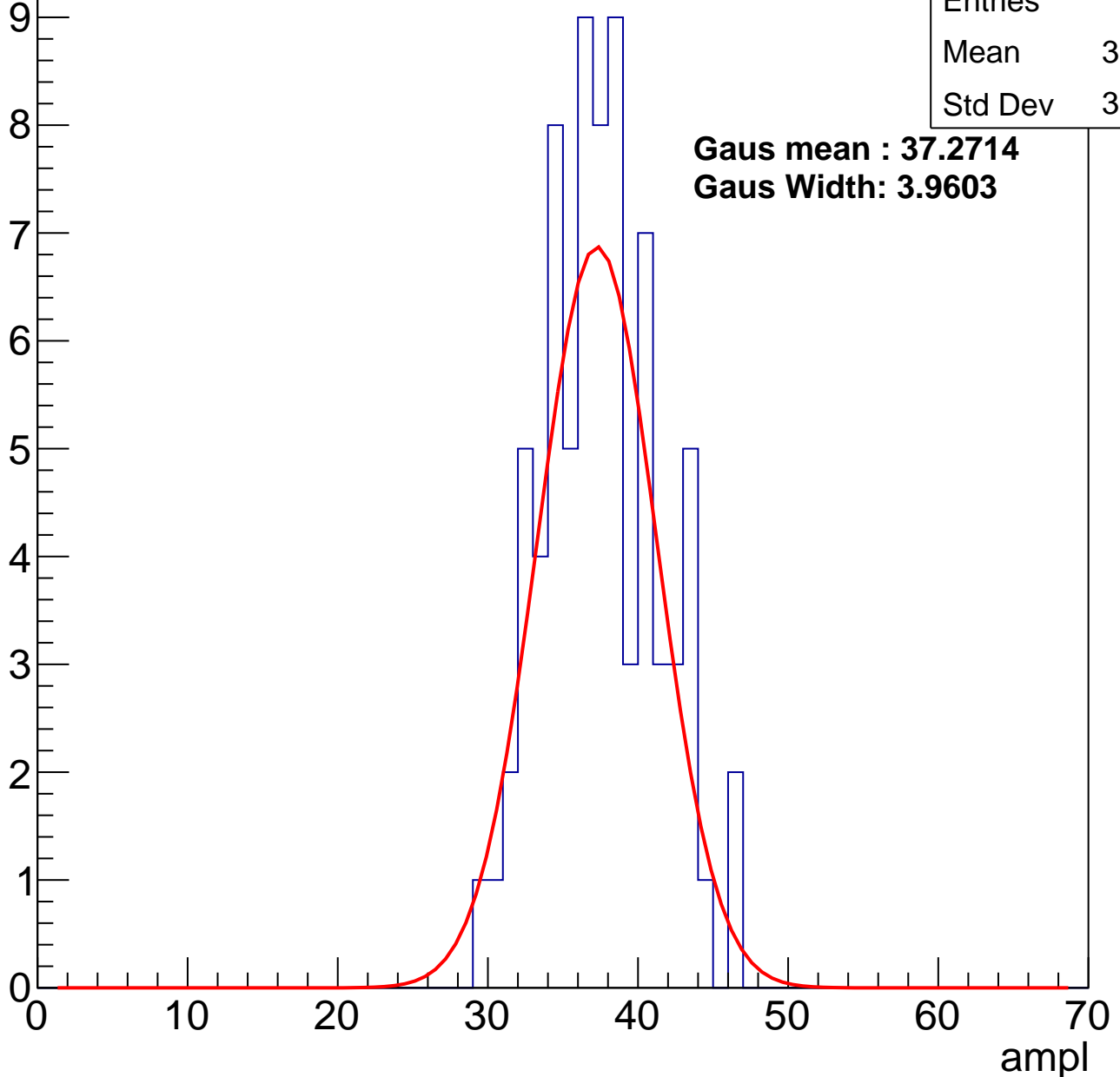
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	37.09
Std Dev	3.756

**Gaus mean : 37.2714**

**Gaus Width: 3.9603**



# B1L101S, U16-ch36, adc2

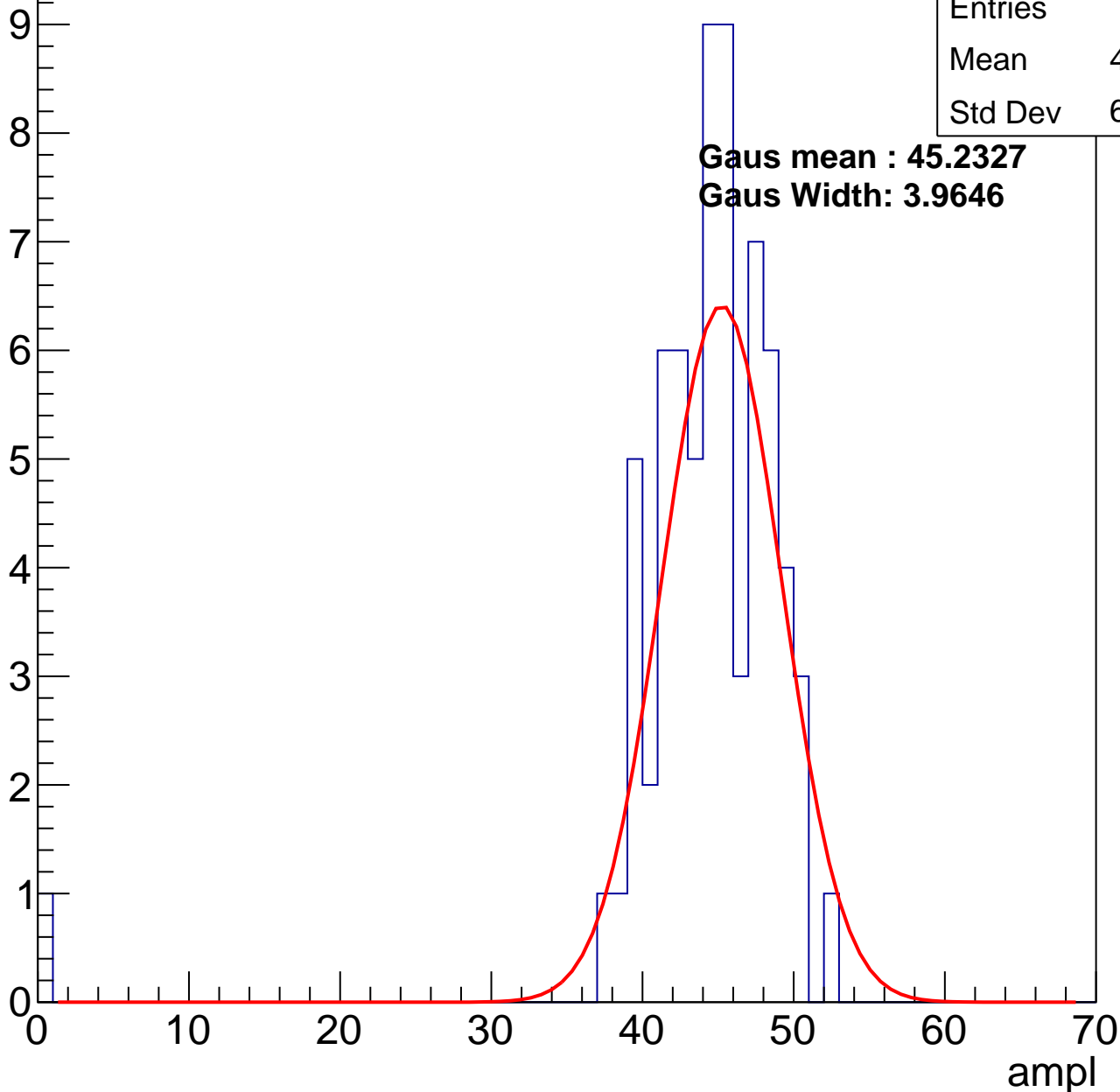
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	43.72
Std Dev	6.264

**Gaus mean : 45.2327**

**Gaus Width: 3.9646**

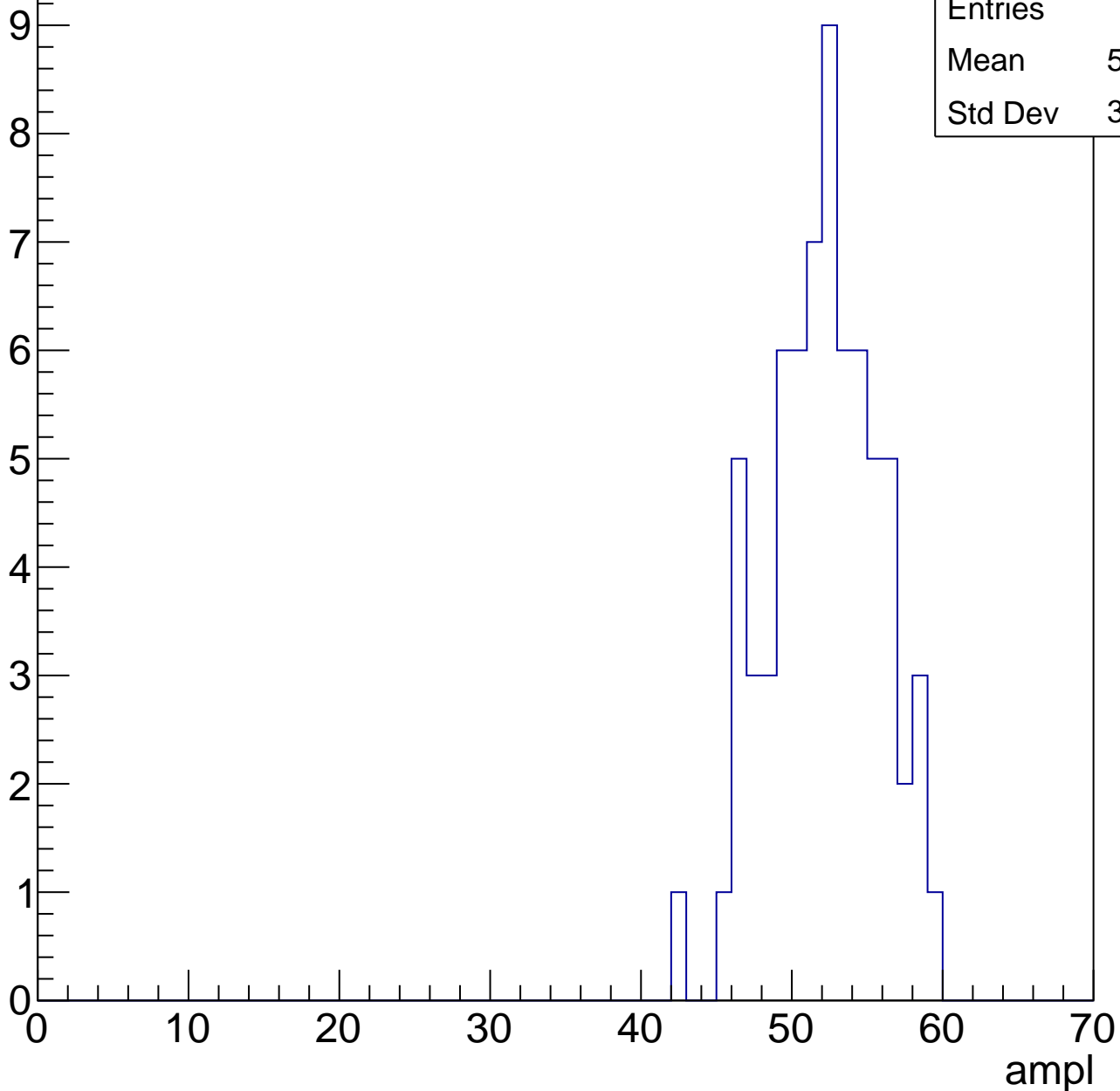


# B1L101S, U16-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	51.67
Std Dev	3.594

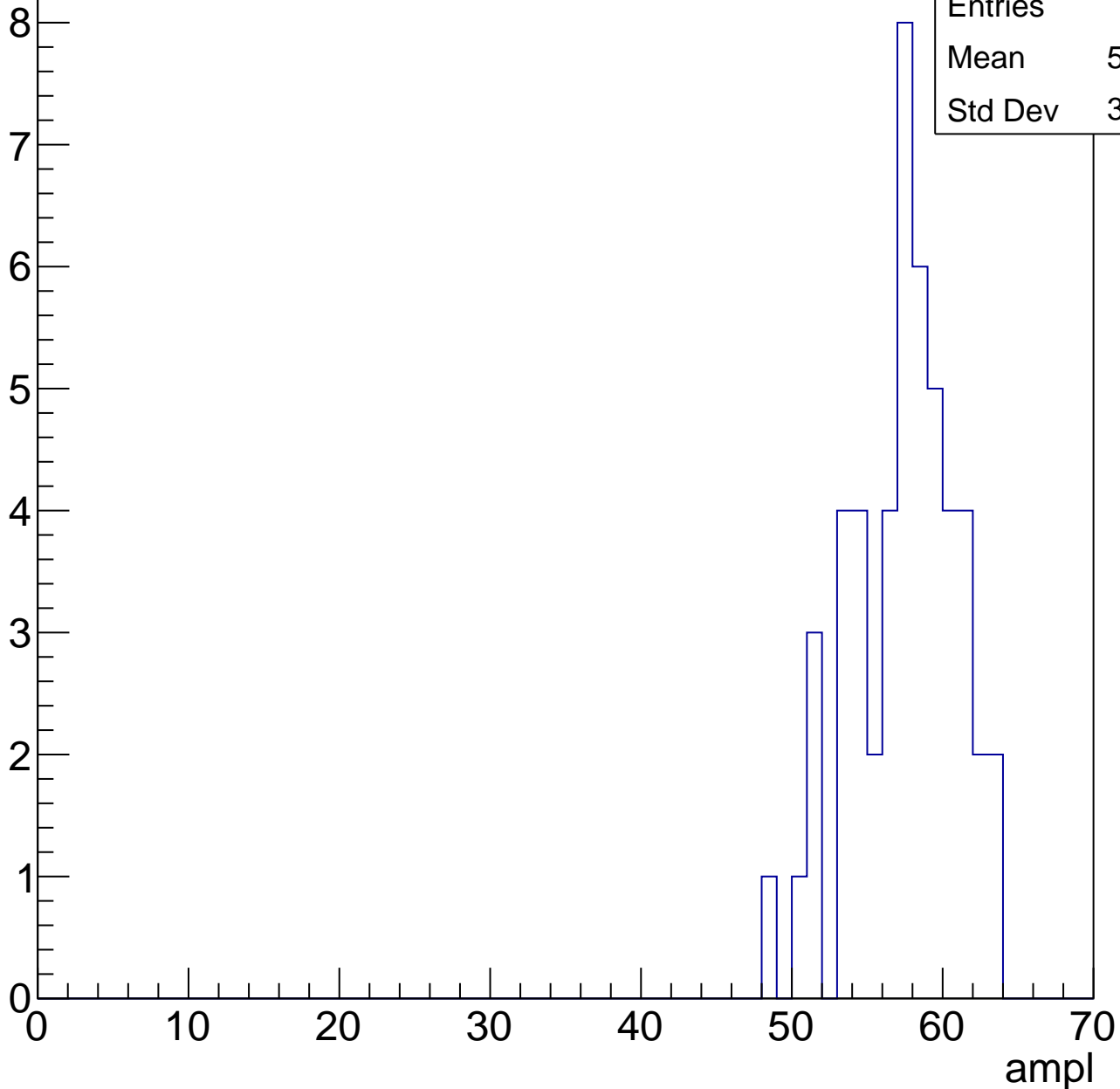


# B1L101S, U16-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	56.92
Std Dev	3.457

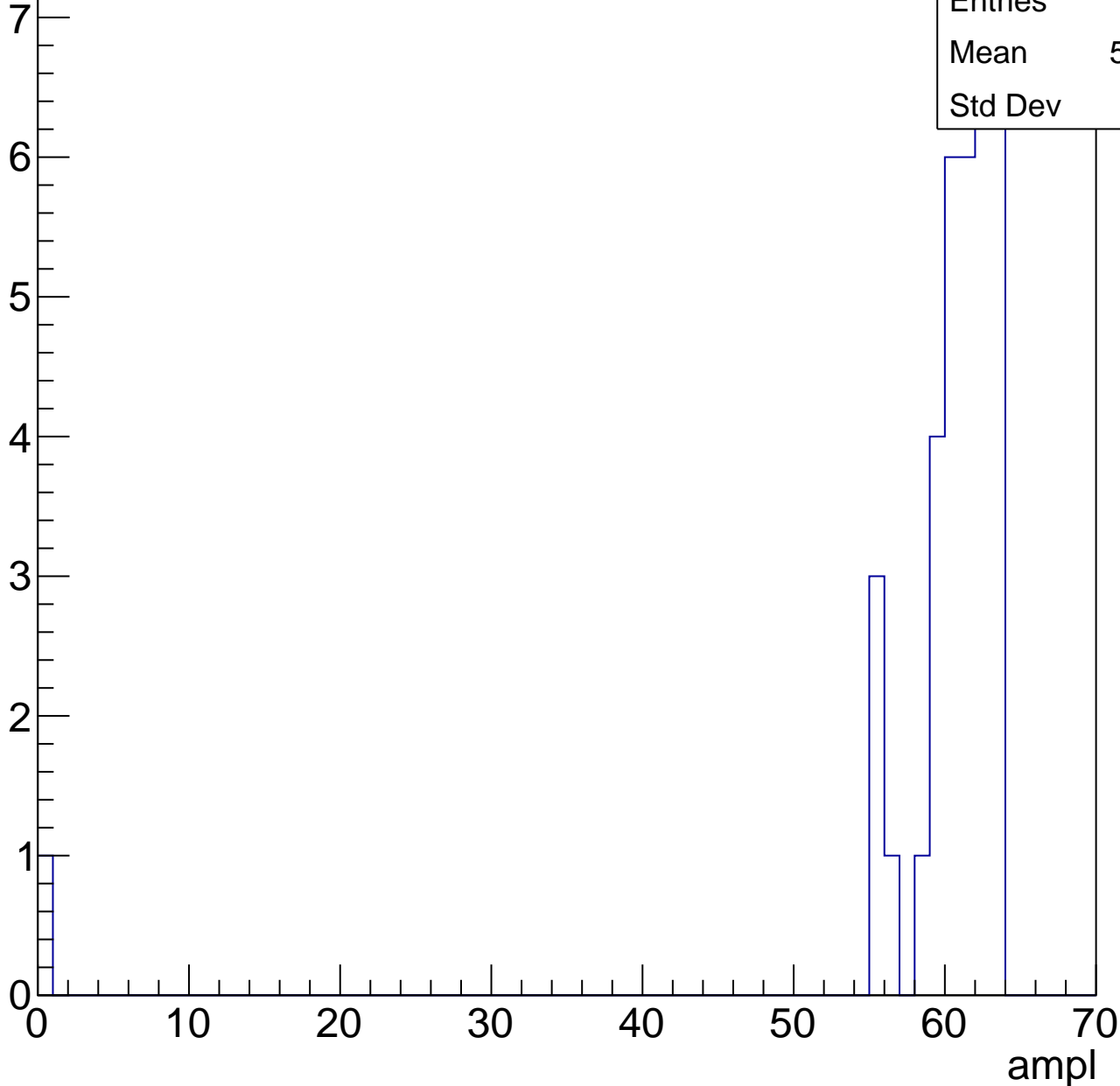


# B1L101S, U16-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	36
Mean	58.78
Std Dev	10.2



# B1L101S, U16-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U16-ch37, adc0

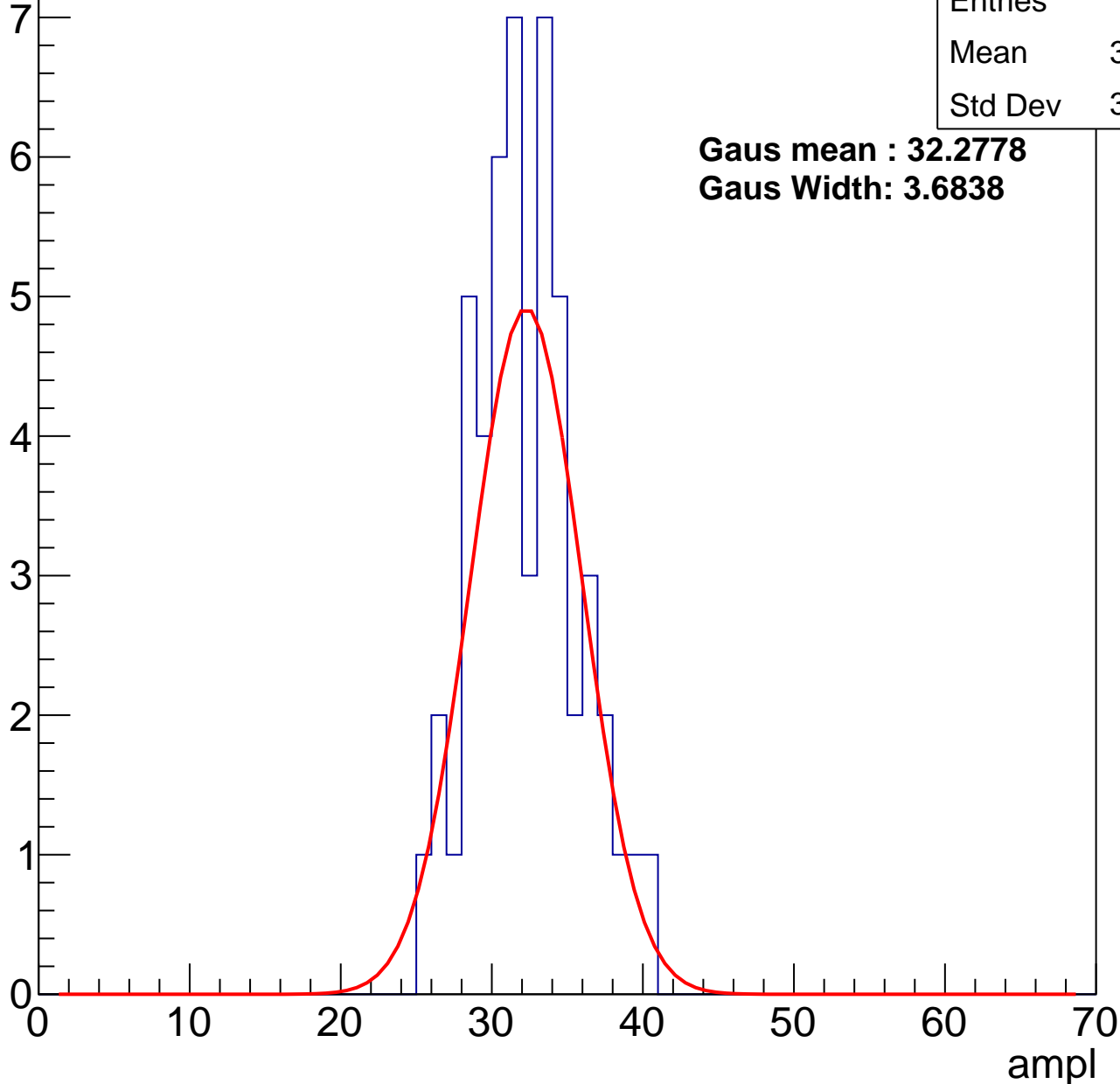
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	31.82
Std Dev	3.382

**Gaus mean : 32.2778**

**Gaus Width: 3.6838**



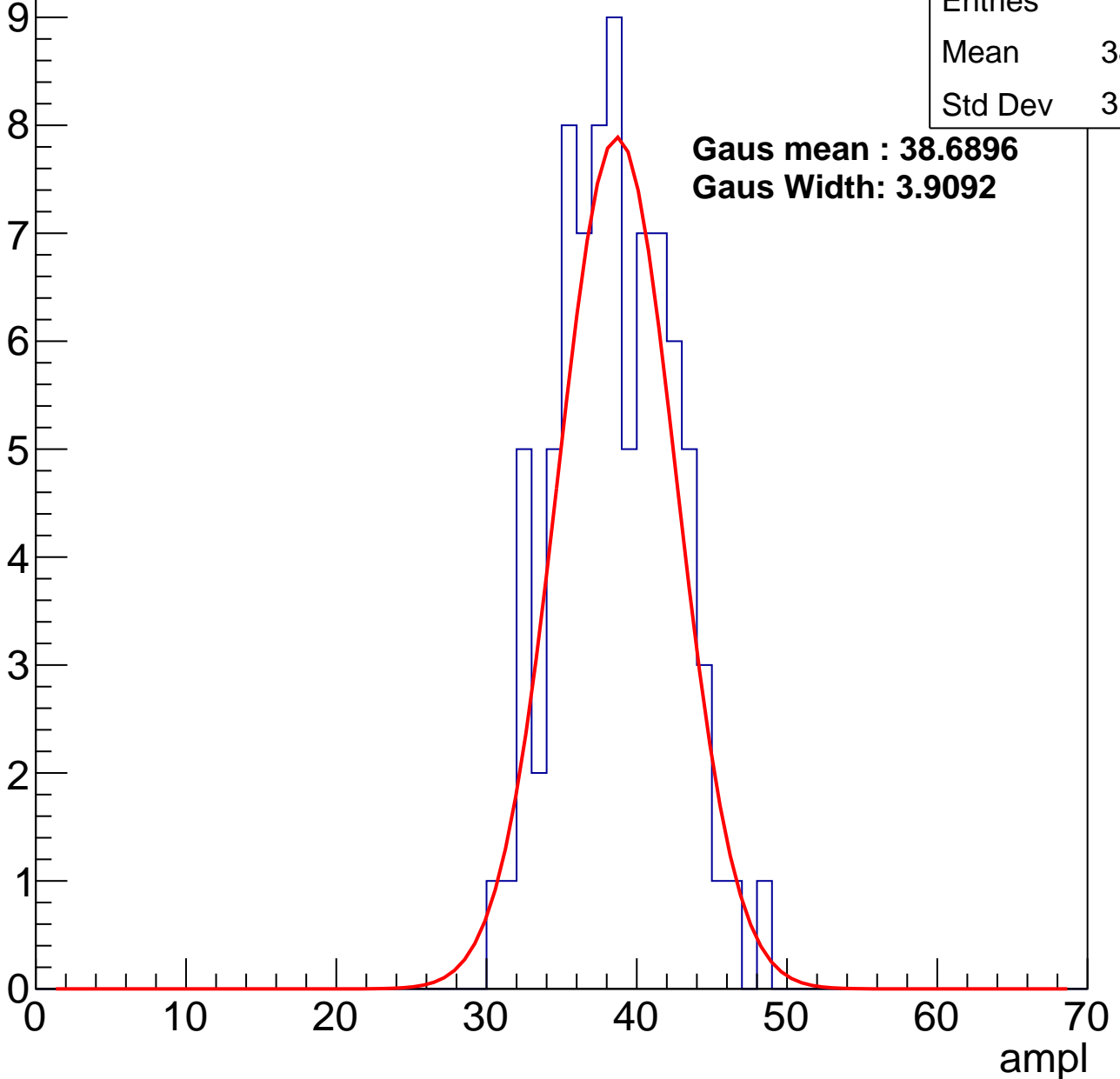
# B1L101S, U16-ch37, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

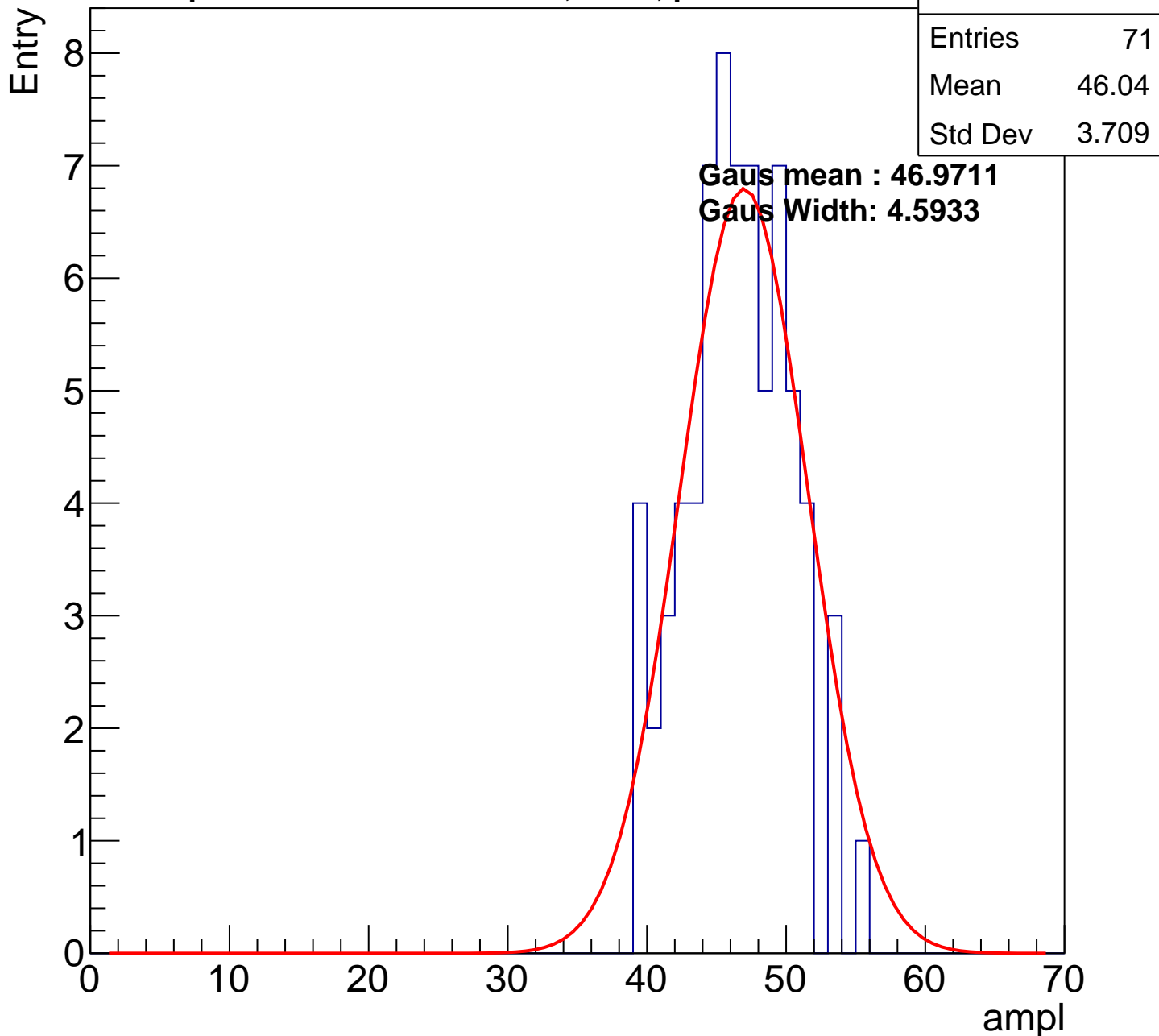
Entries	82
Mean	38.13
Std Dev	3.773

**Gaus mean : 38.6896**  
**Gaus Width: 3.9092**



# B1L101S, U16-ch37, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

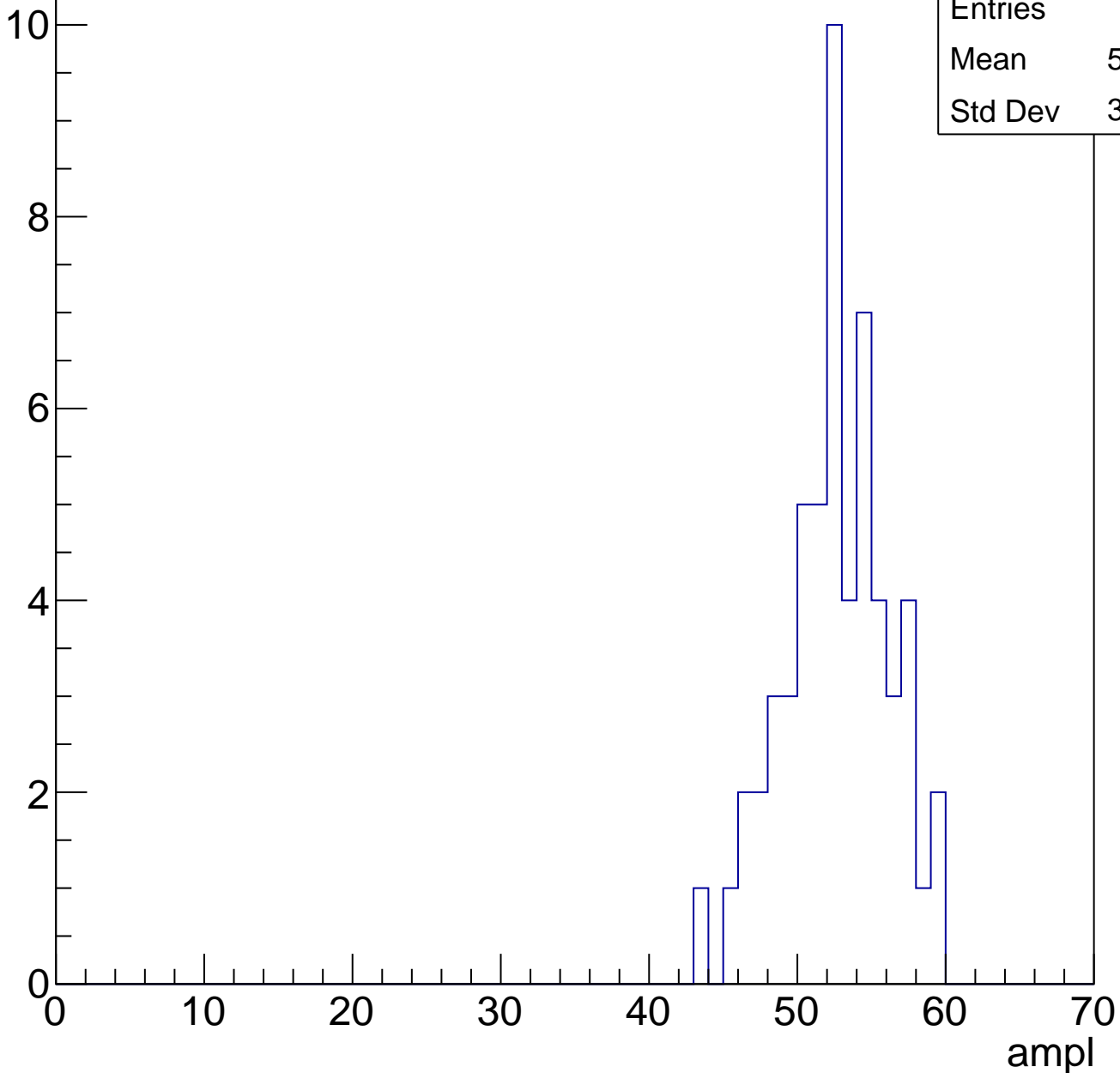


# B1L101S, U16-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

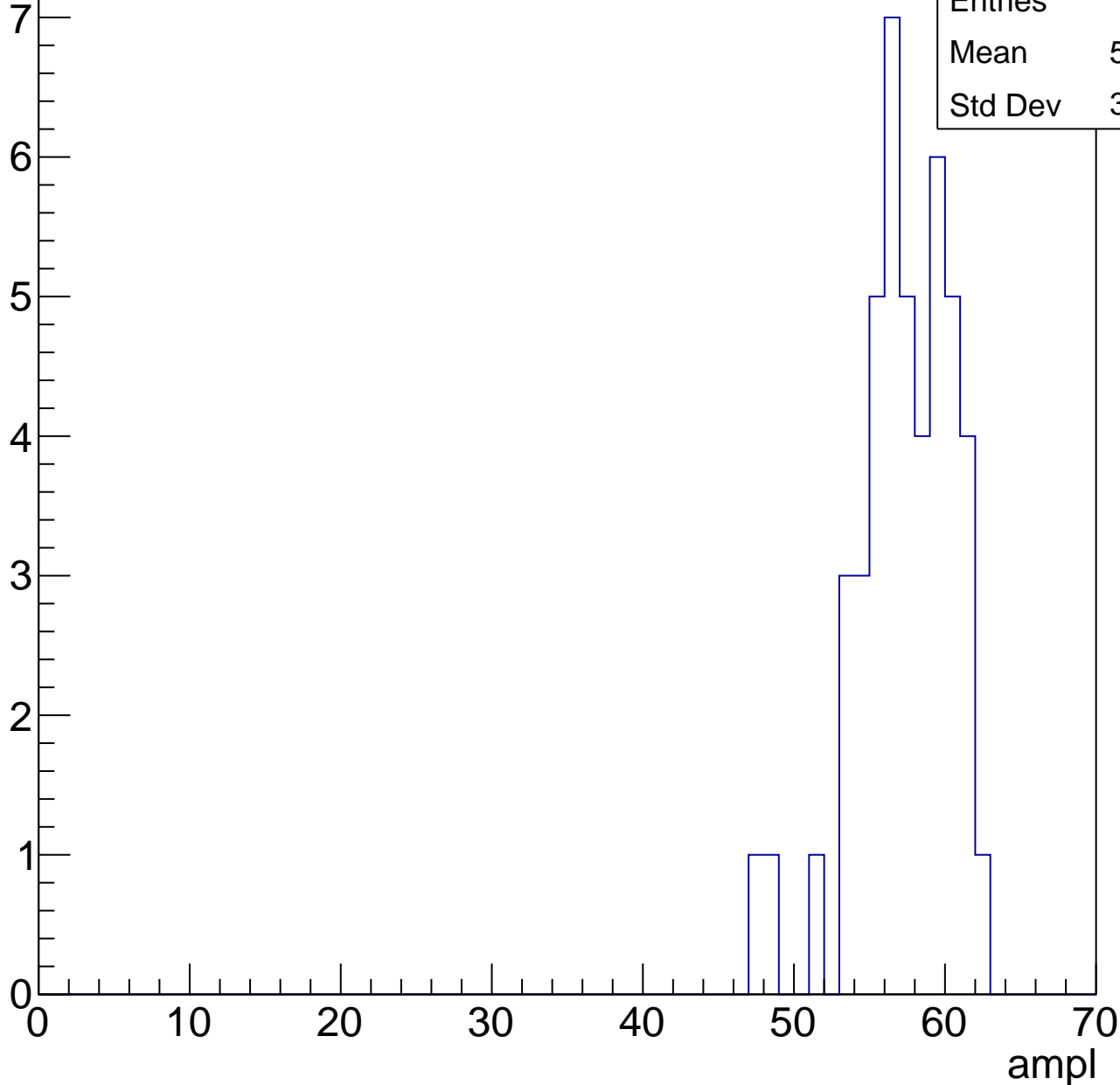
Entries	57
Mean	52.14
Std Dev	3.507



# B1L101S, U16-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

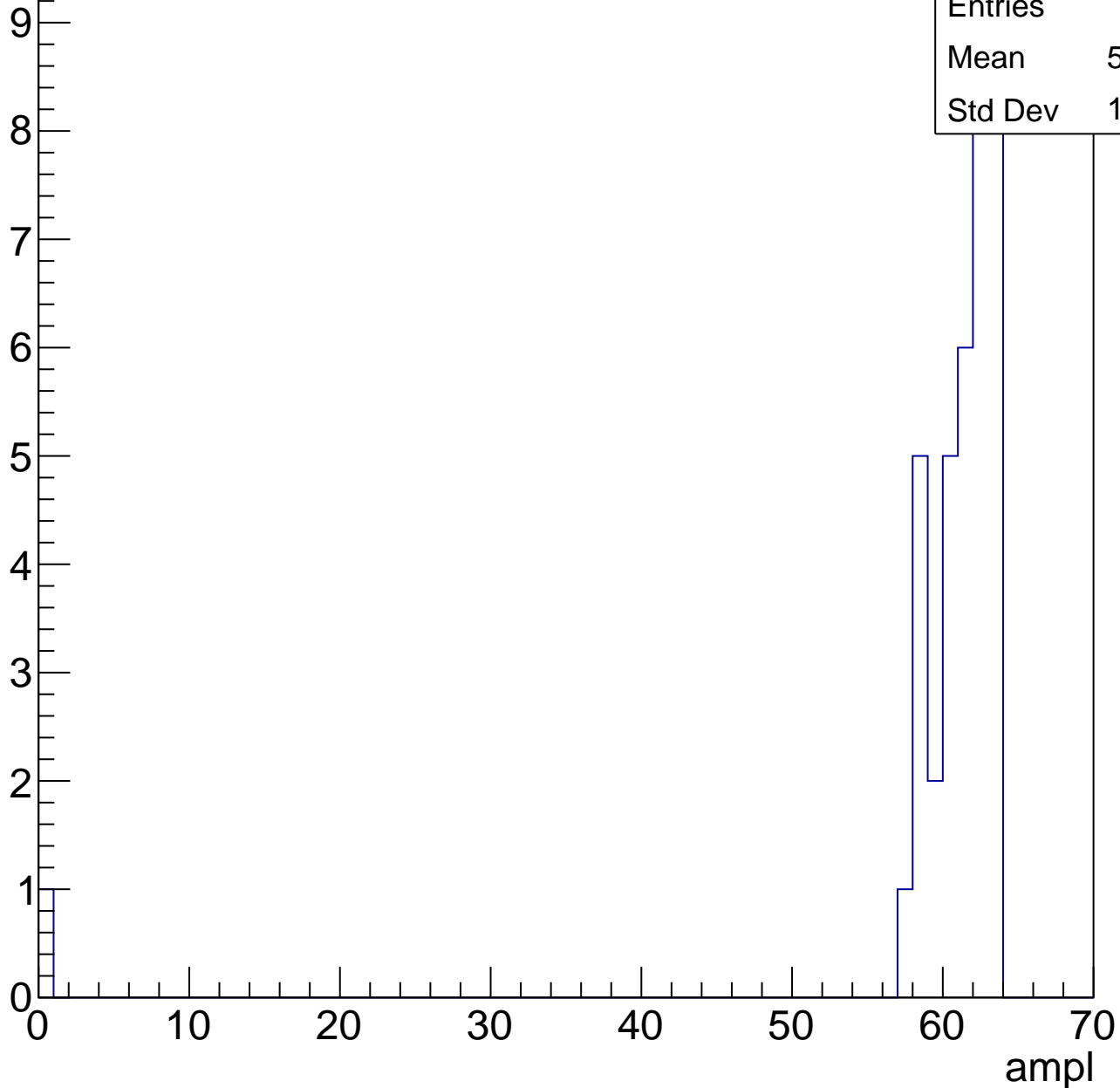
Entry



# B1L101S, U16-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U16-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U16-ch38, adc0

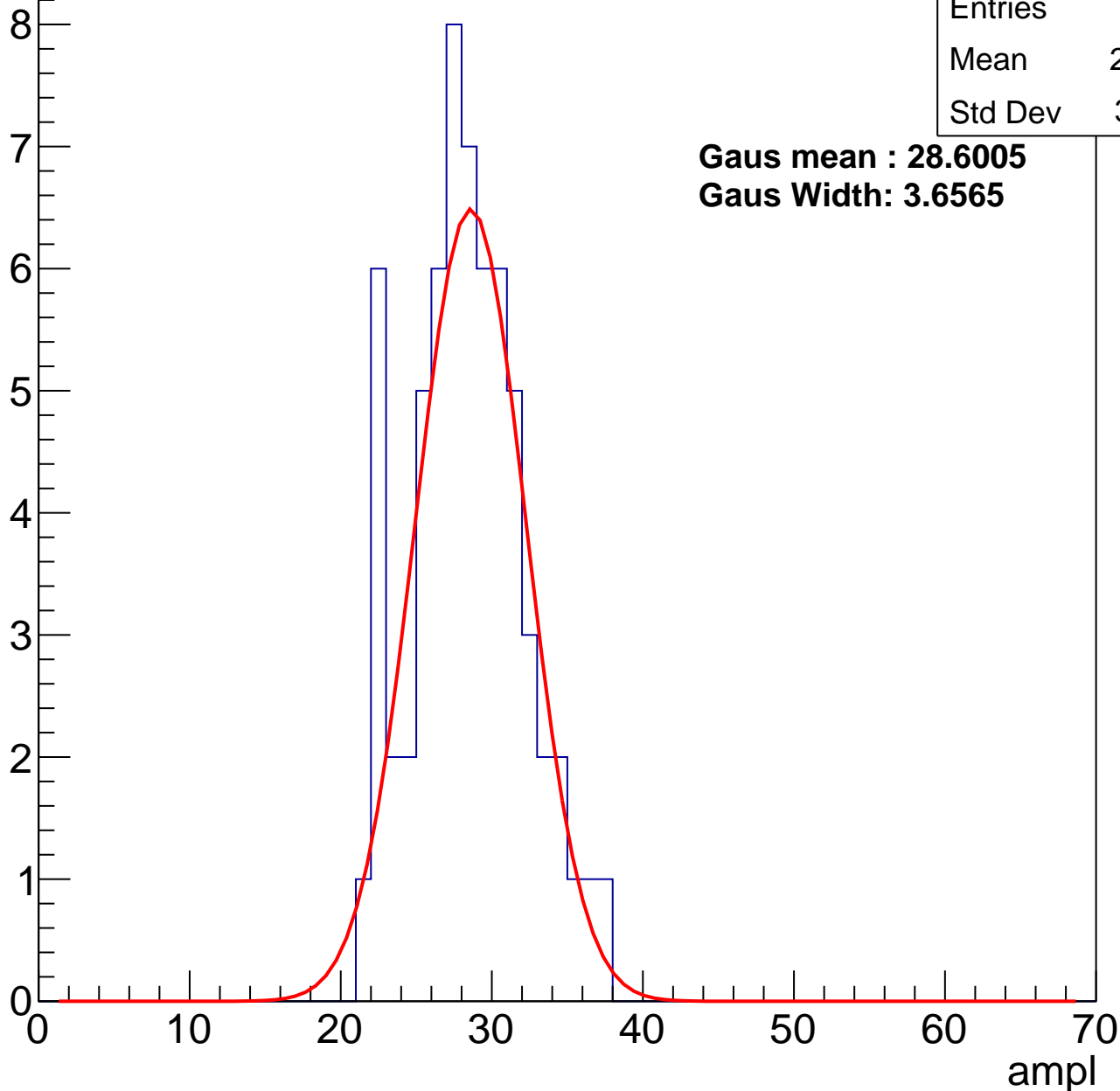
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	27.92
Std Dev	3.671

**Gaus mean : 28.6005**

**Gaus Width: 3.6565**



# B1L101S, U16-ch38, adc1

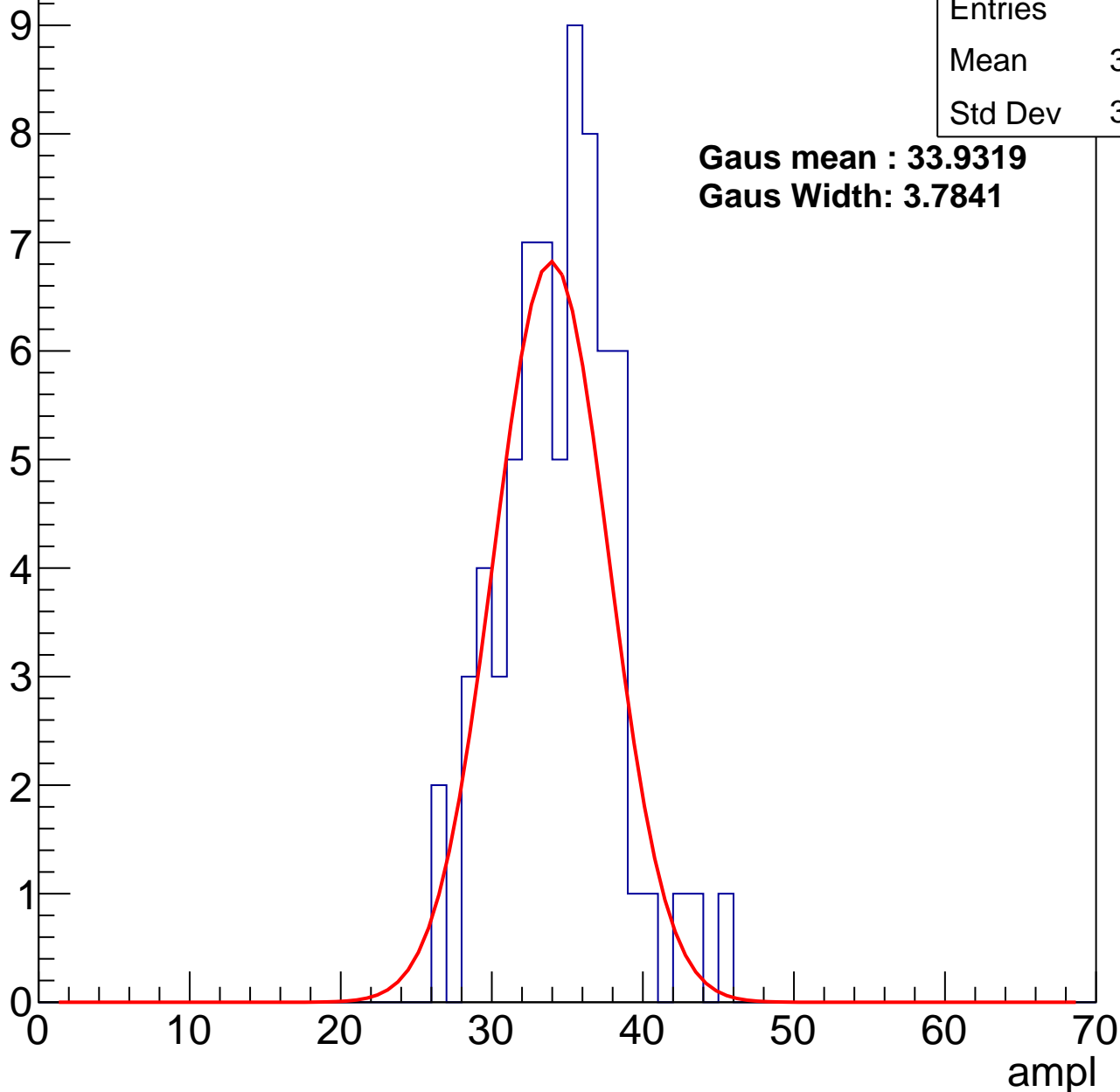
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	34.06
Std Dev	3.745

**Gaus mean : 33.9319**

**Gaus Width: 3.7841**



# B1L101S, U16-ch38, adc2

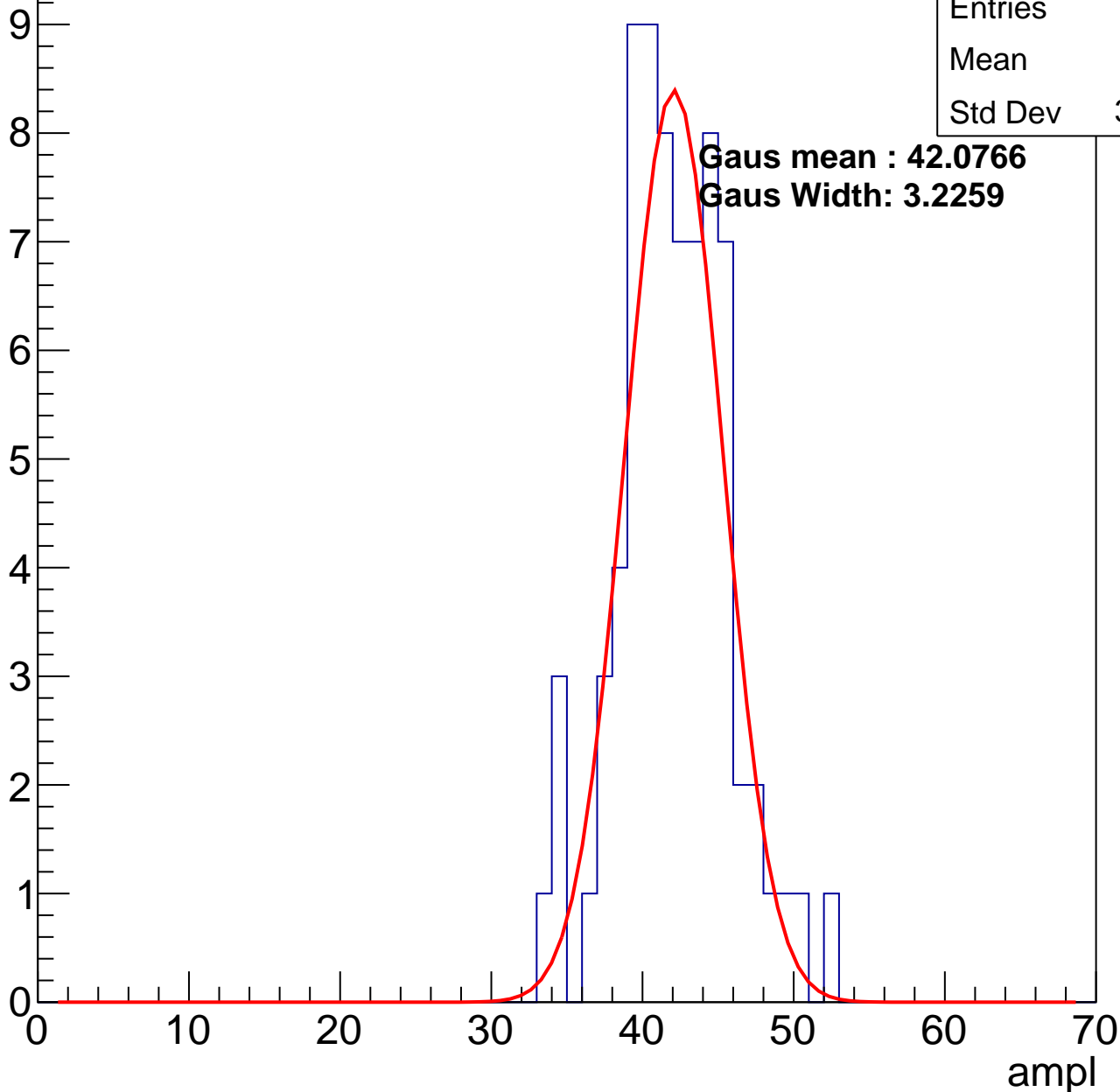
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	41.6
Std Dev	3.641

**Gaus mean : 42.0766**

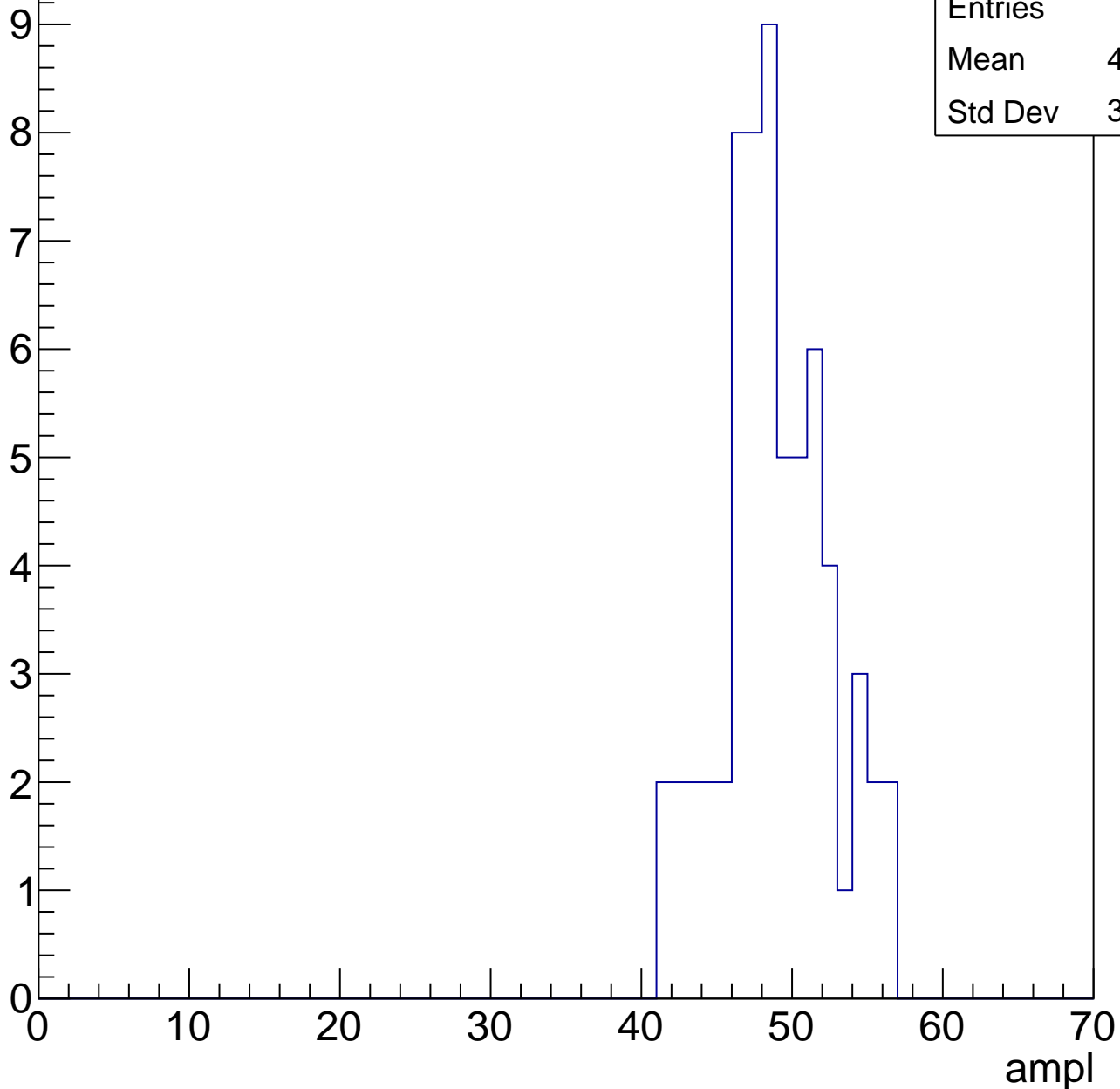
**Gaus Width: 3.2259**



# B1L101S, U16-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

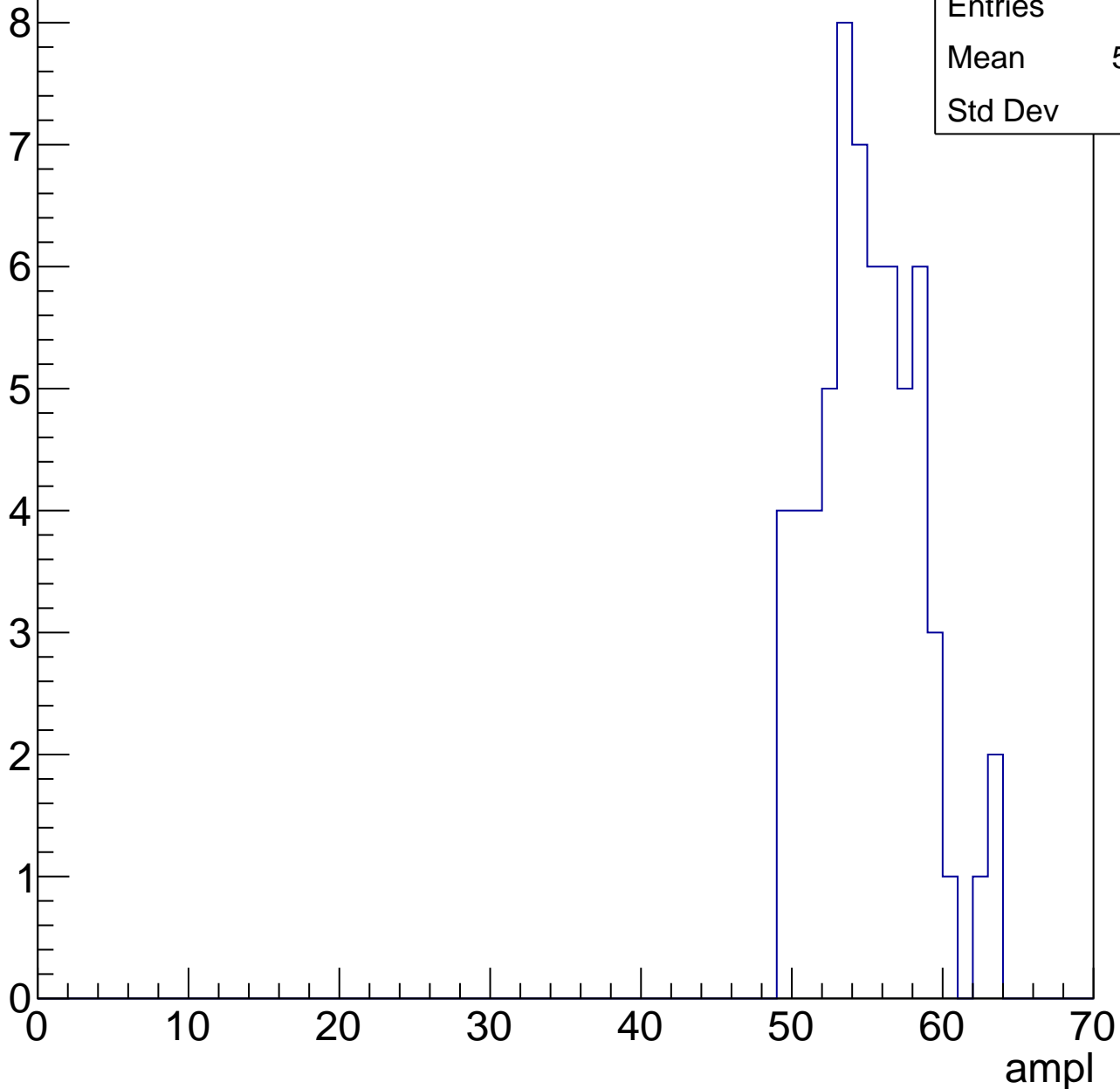


# B1L101S, U16-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	54.61
Std Dev	3.39

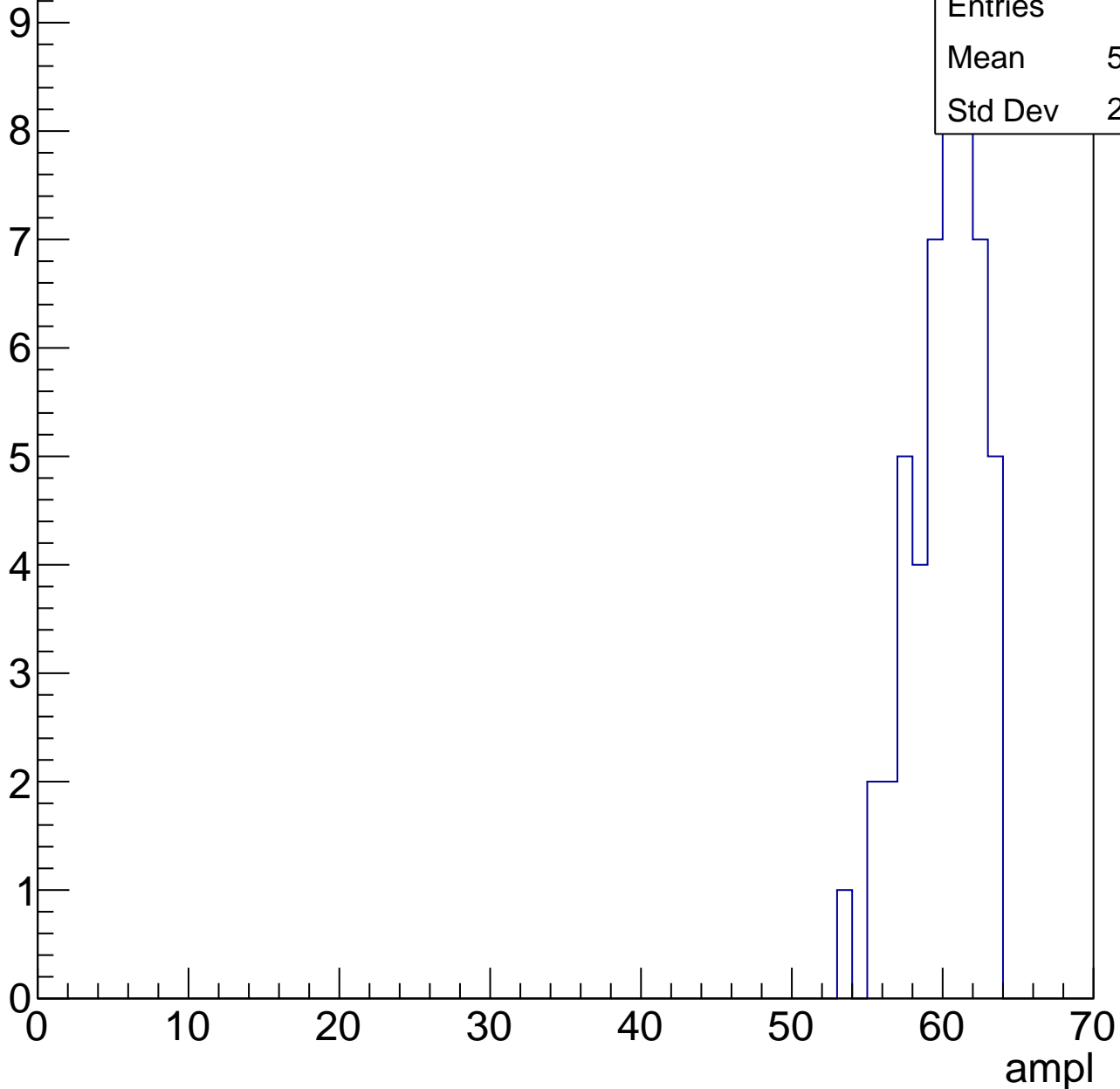


# B1L101S, U16-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

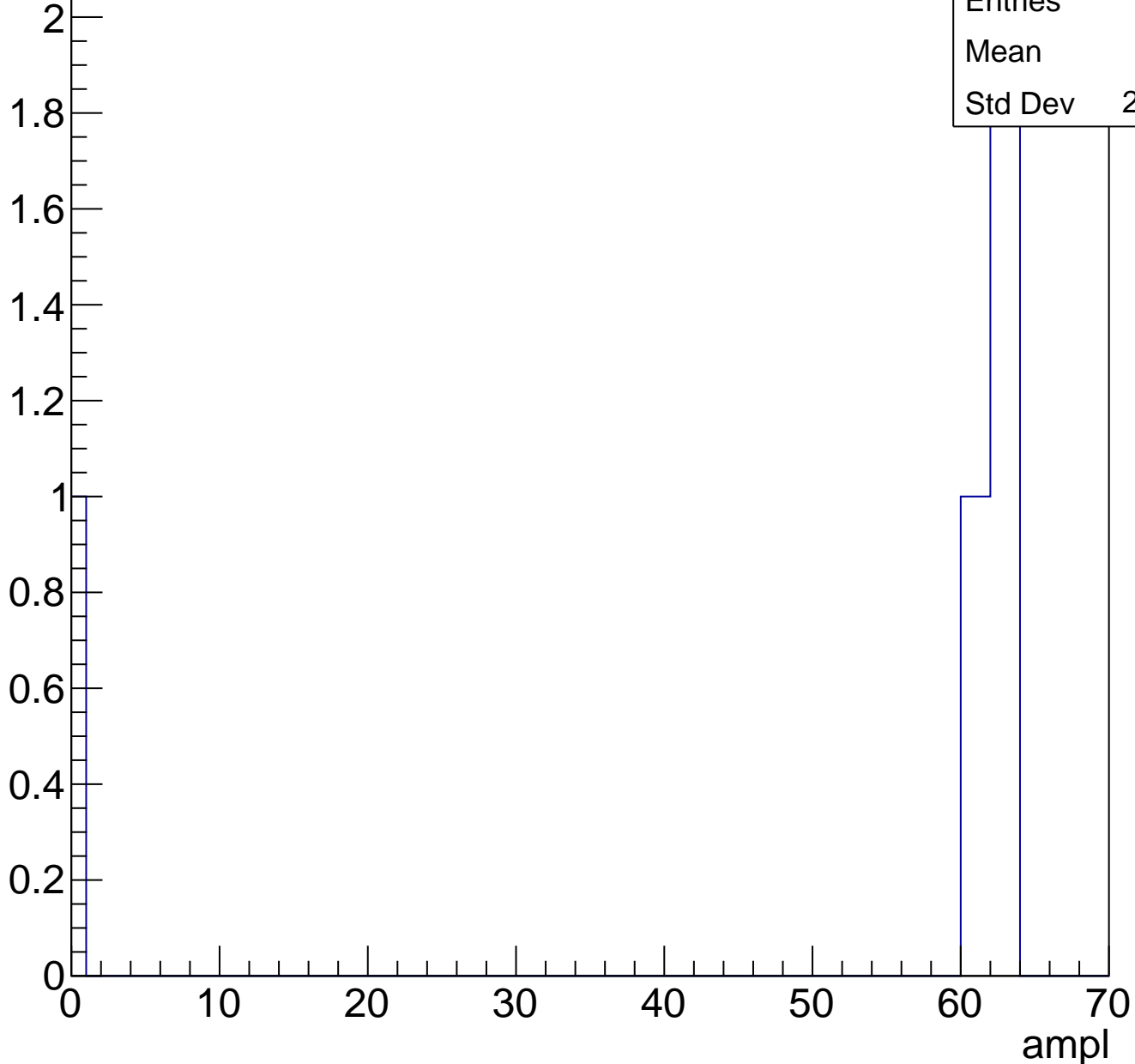
Entries	50
Mean	59.66
Std Dev	2.346



# B1L101S, U16-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch39, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	67
Mean	29.96
Std Dev	3.16

**Gaus mean : 30.3001**

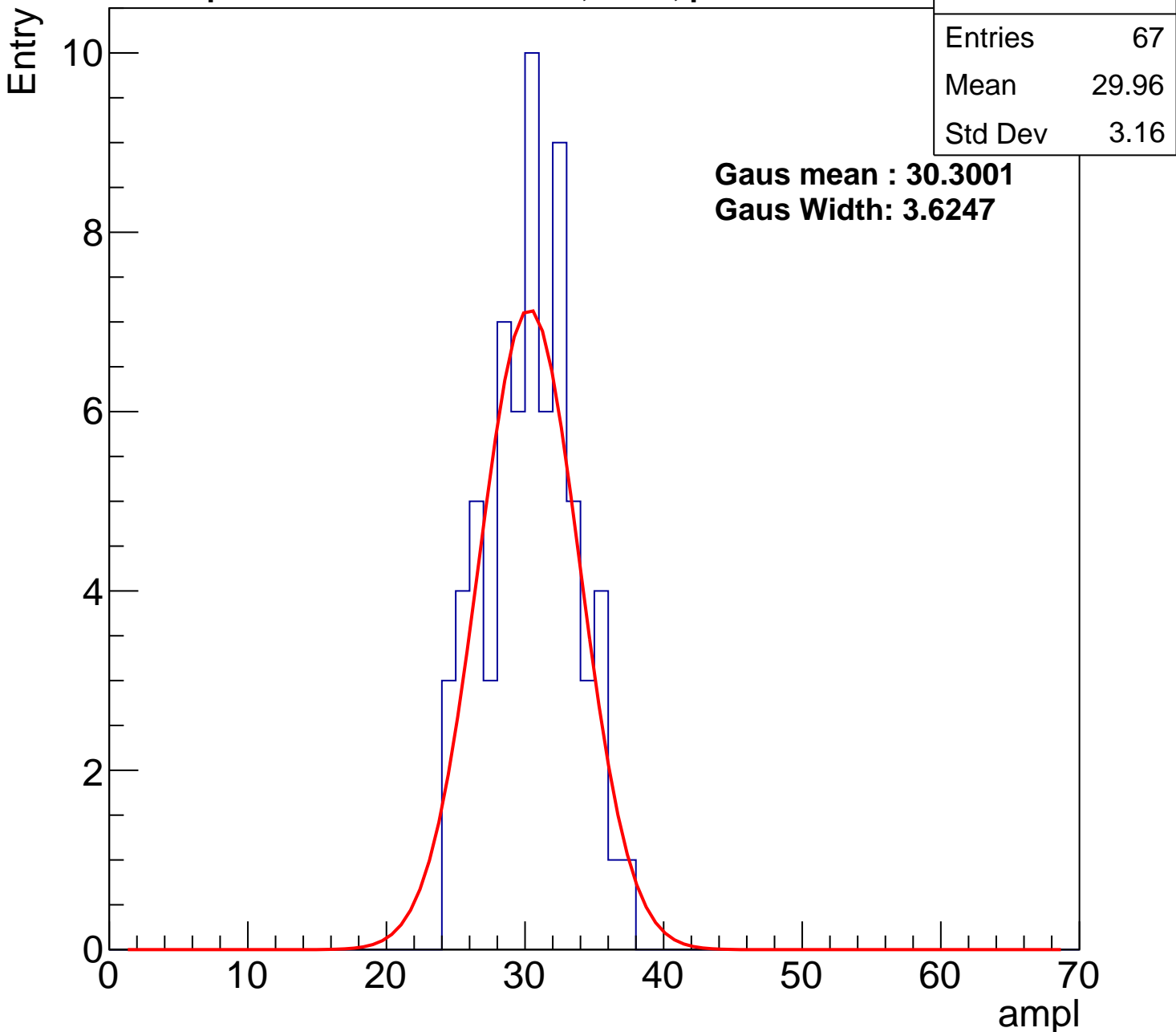
**Gaus Width: 3.6247**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch39, adc1

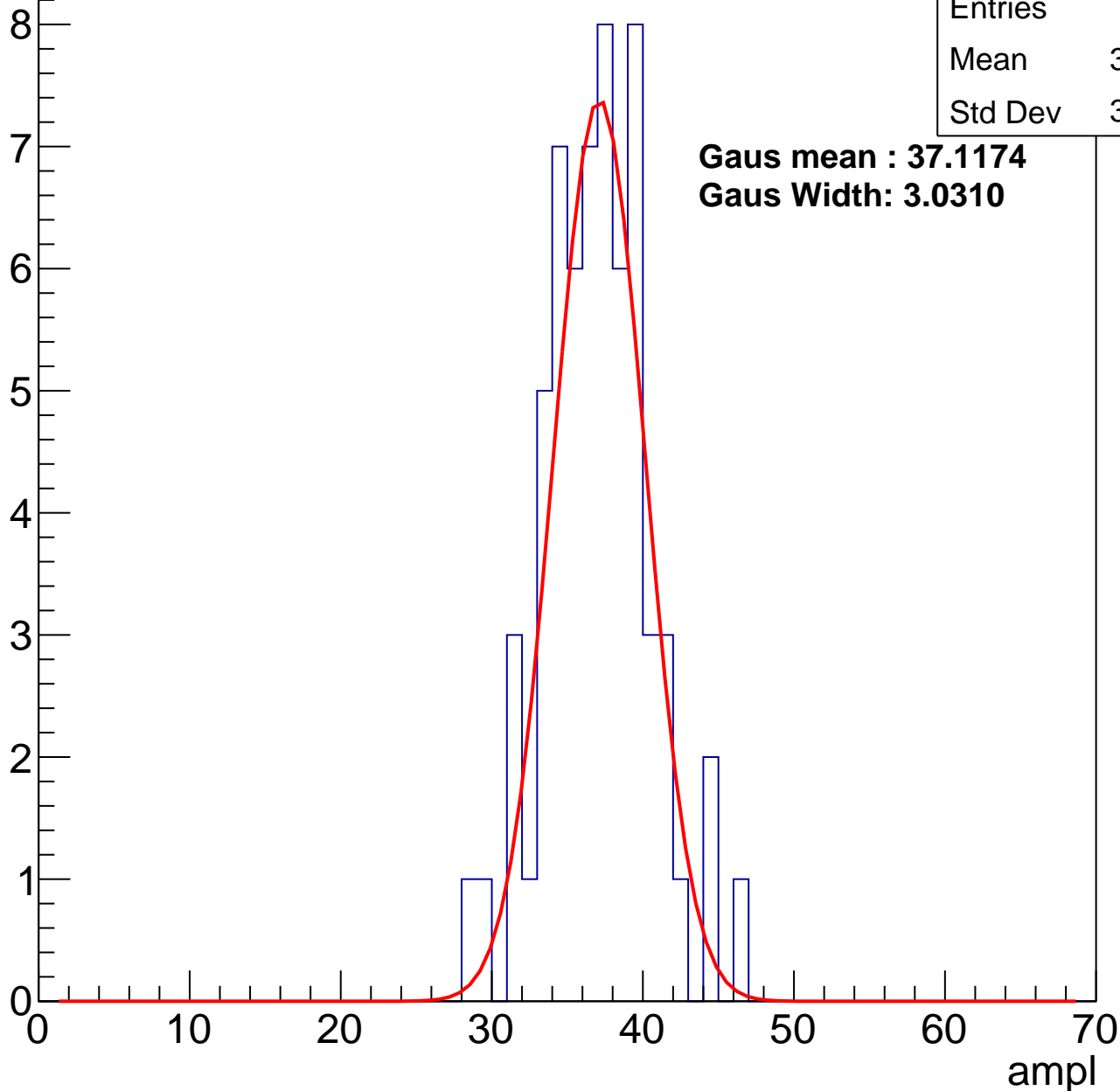
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	36.54
Std Dev	3.463

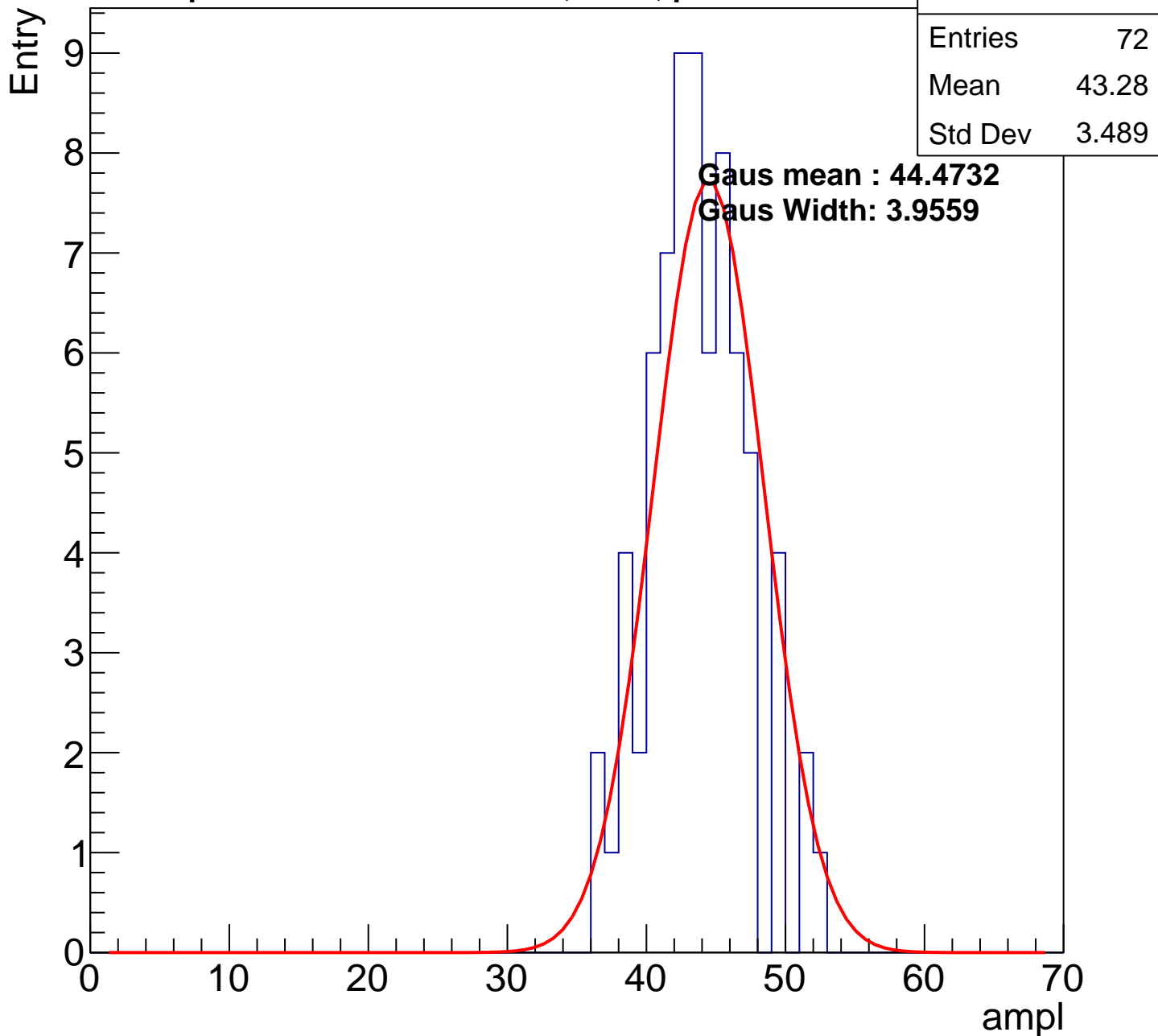
**Gaus mean : 37.1174**

**Gaus Width: 3.0310**



# B1L101S, U16-ch39, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

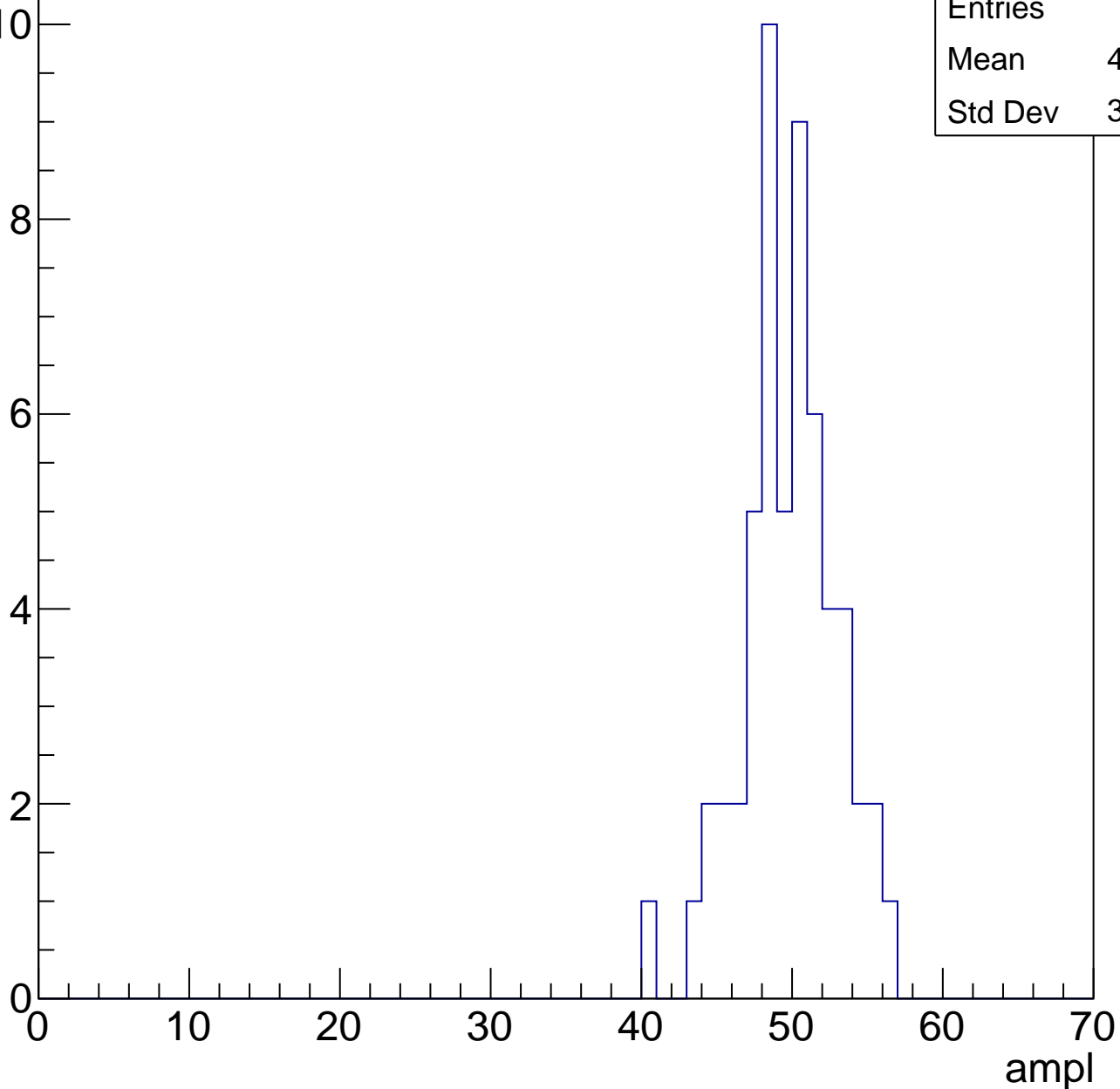


# B1L101S, U16-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

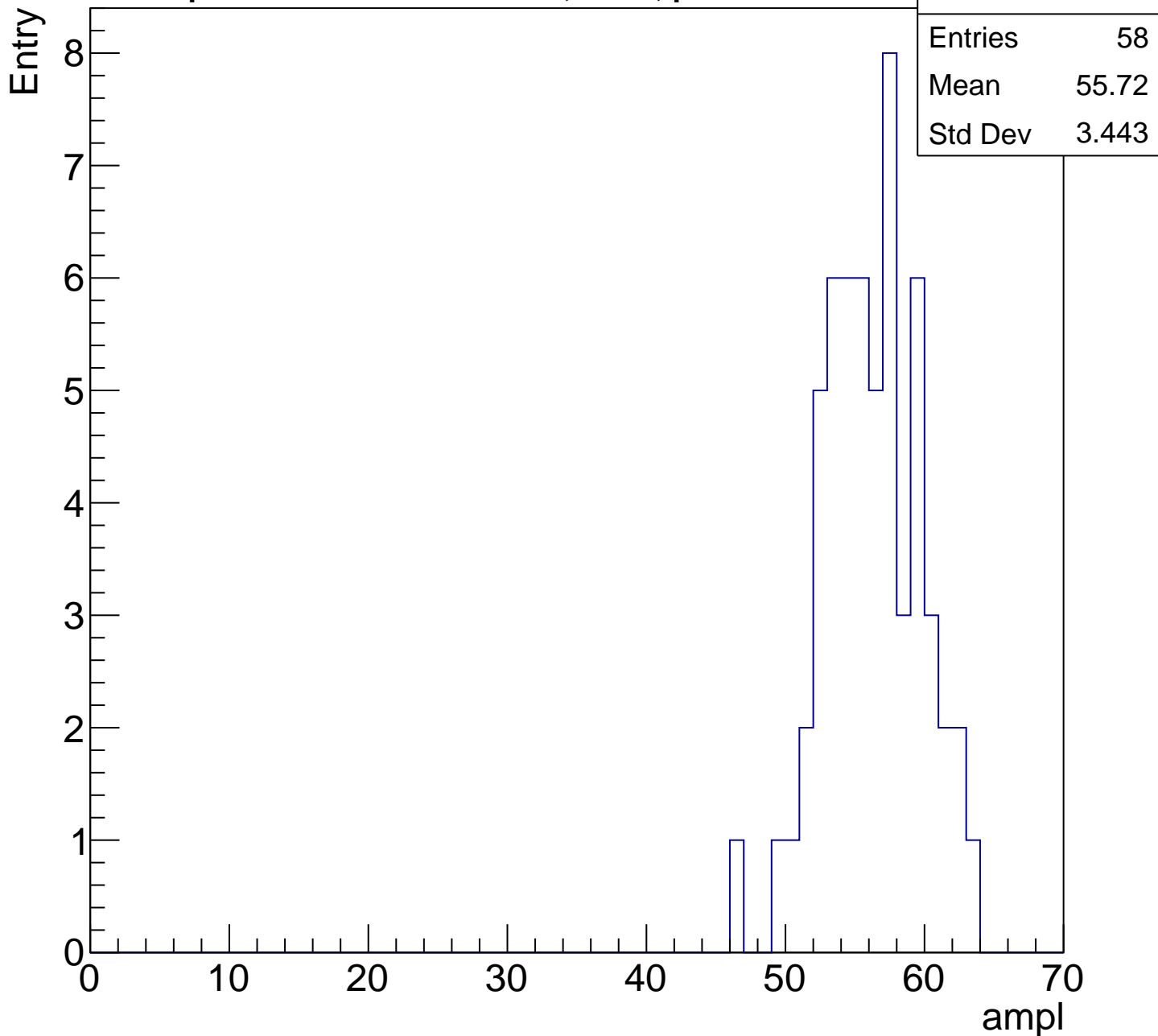
Entry

Entries	56
Mean	49.34
Std Dev	3.118



# B1L101S, U16-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U16-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

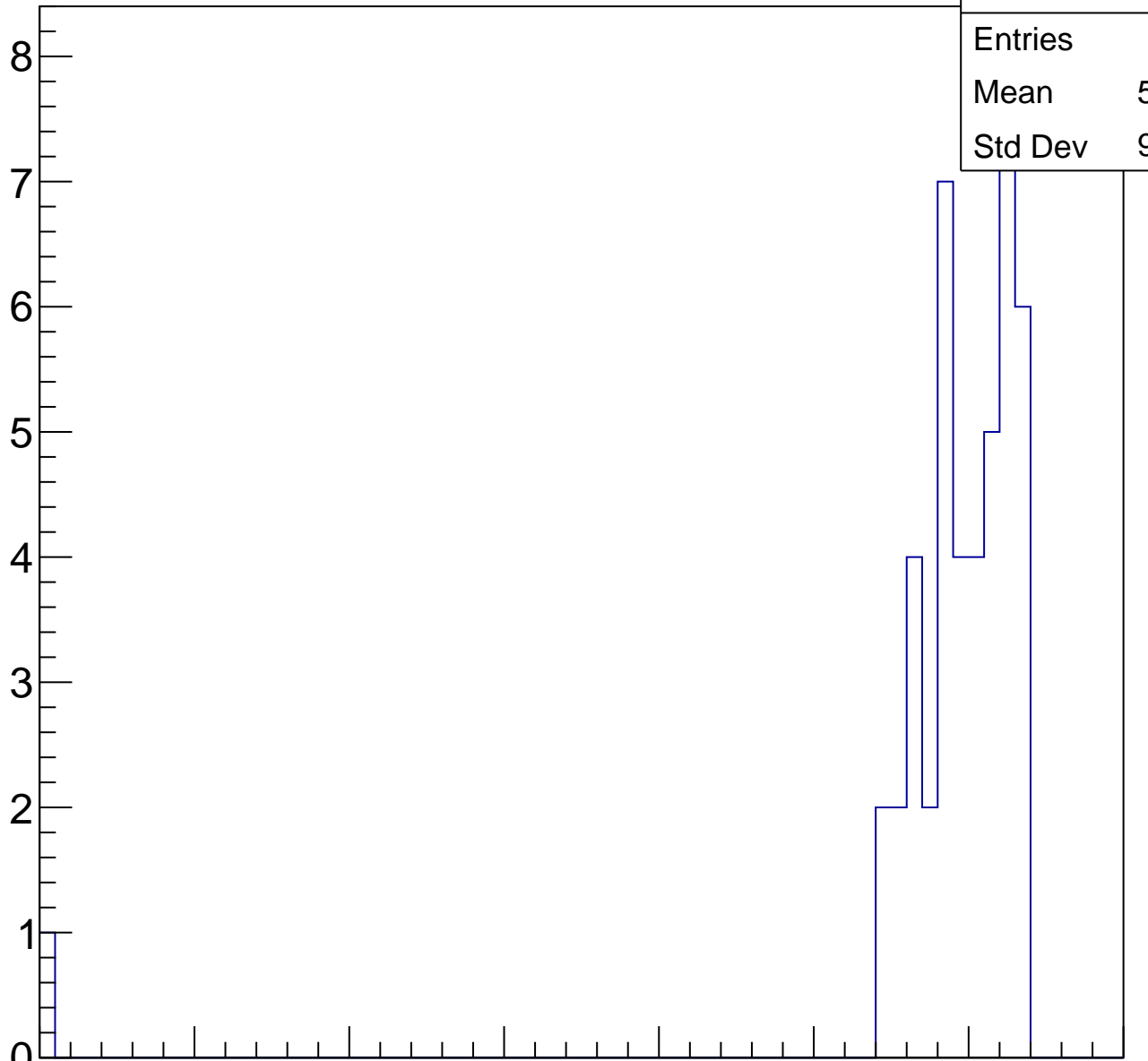
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	45
Mean	58.16
Std Dev	9.158

ampl

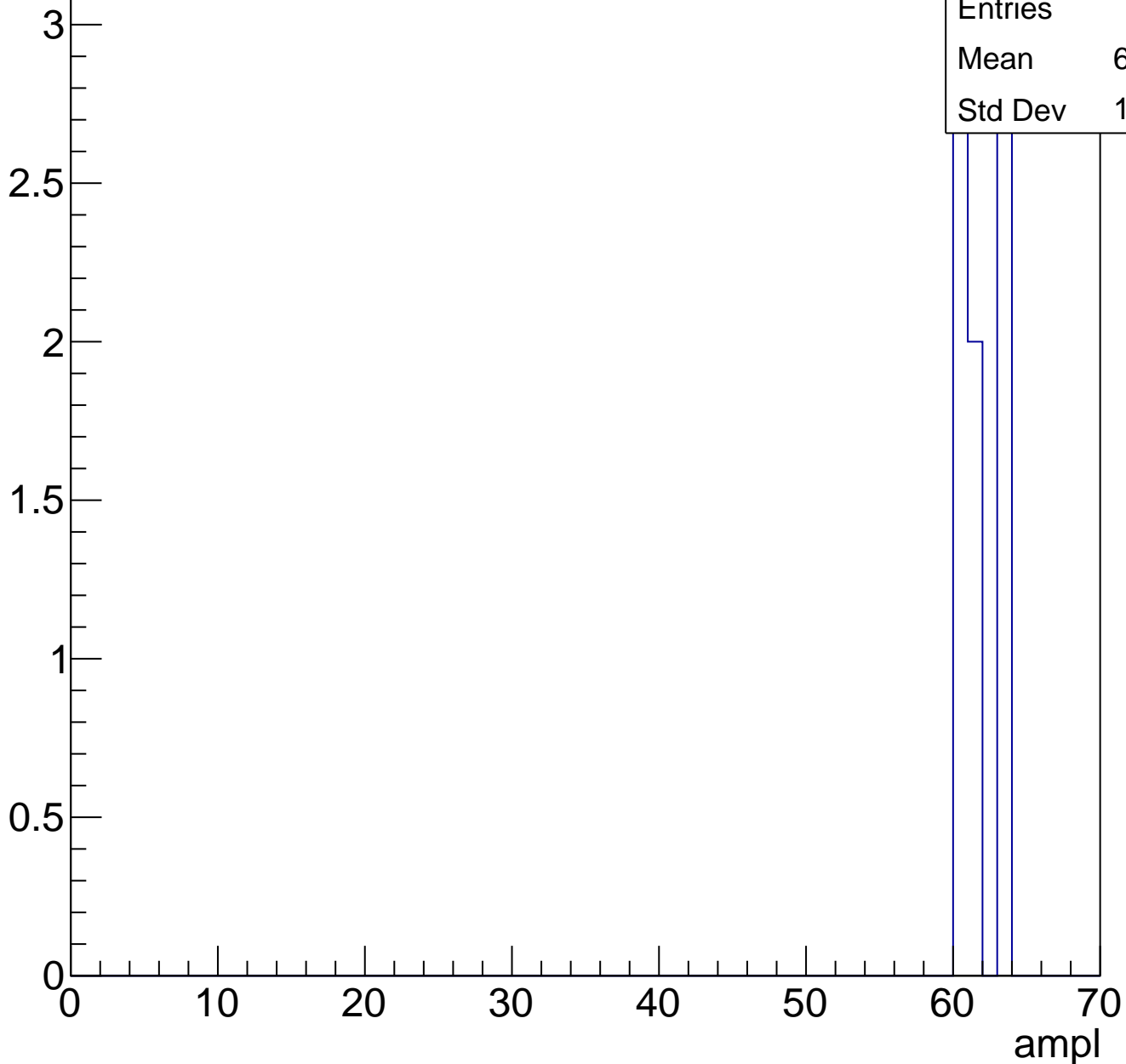
0 10 20 30 40 50 60 70



# B1L101S, U16-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch40, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	76
Mean	28.76
Std Dev	3.677

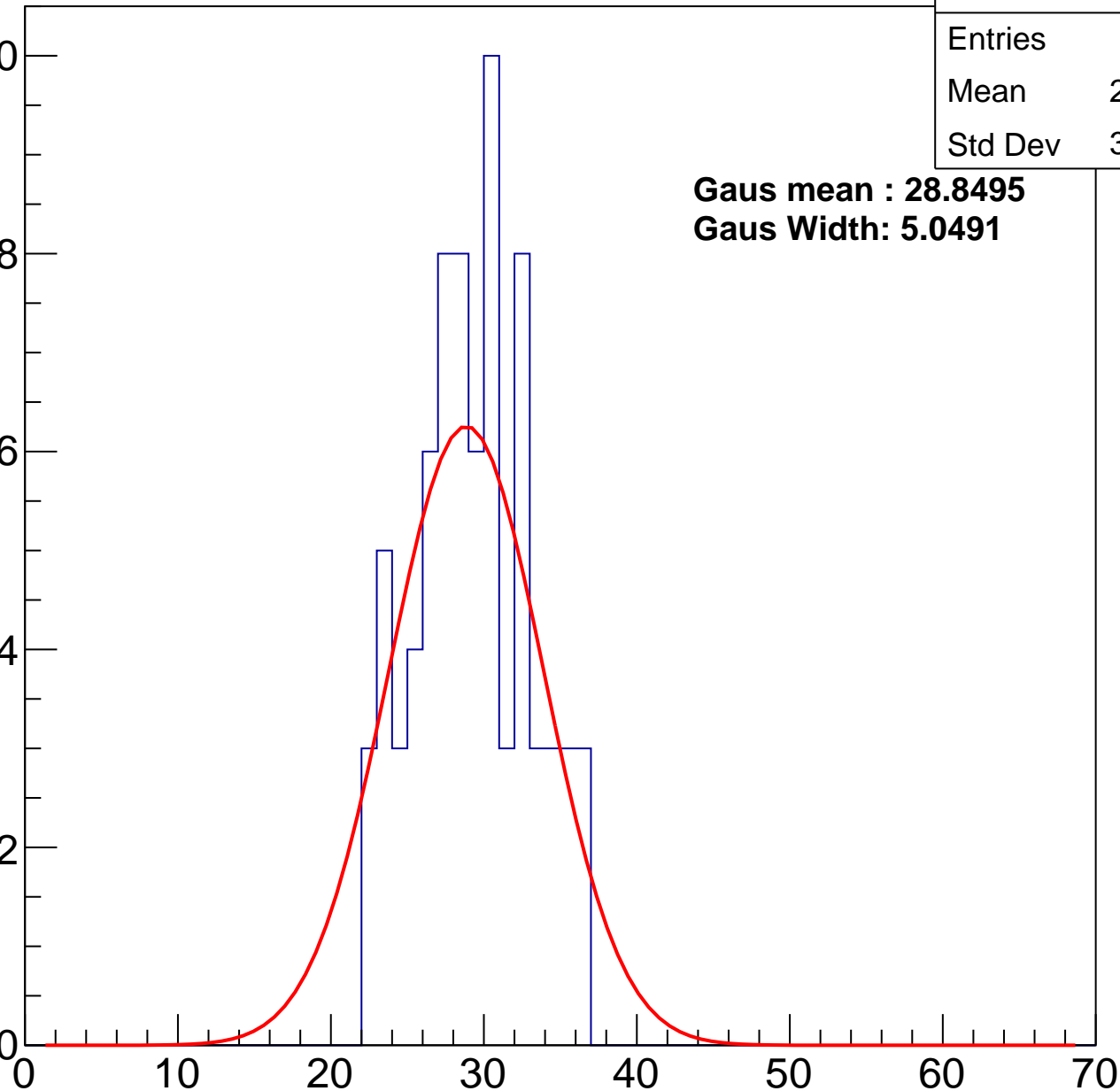
**Gaus mean : 28.8495**

**Gaus Width: 5.0491**

Entry

10  
8  
6  
4  
2  
0

ampl



# B1L101S, U16-ch40, adc1

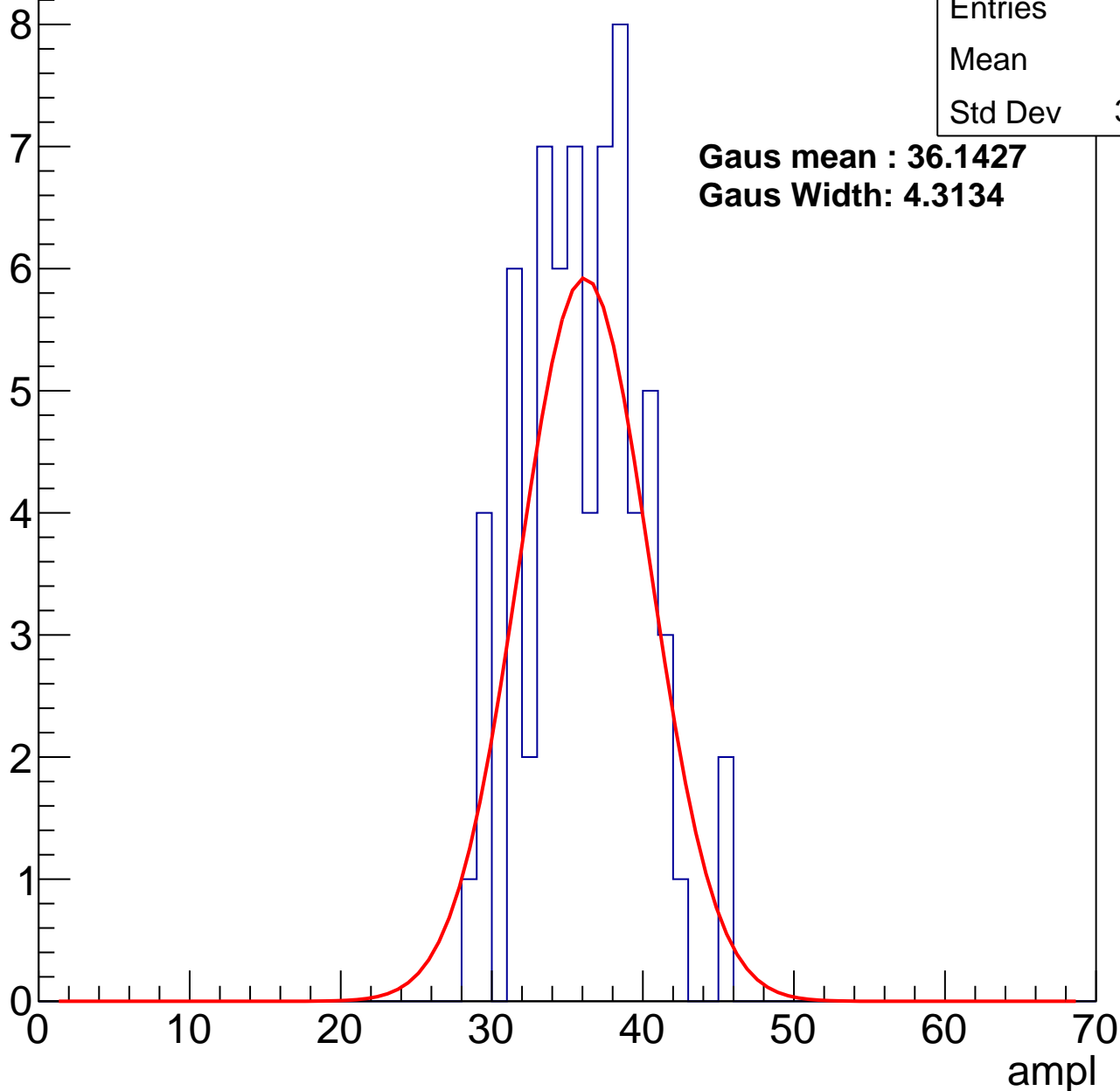
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	35.7
Std Dev	3.781

**Gaus mean : 36.1427**

**Gaus Width: 4.3134**



# B1L101S, U16-ch40, adc2

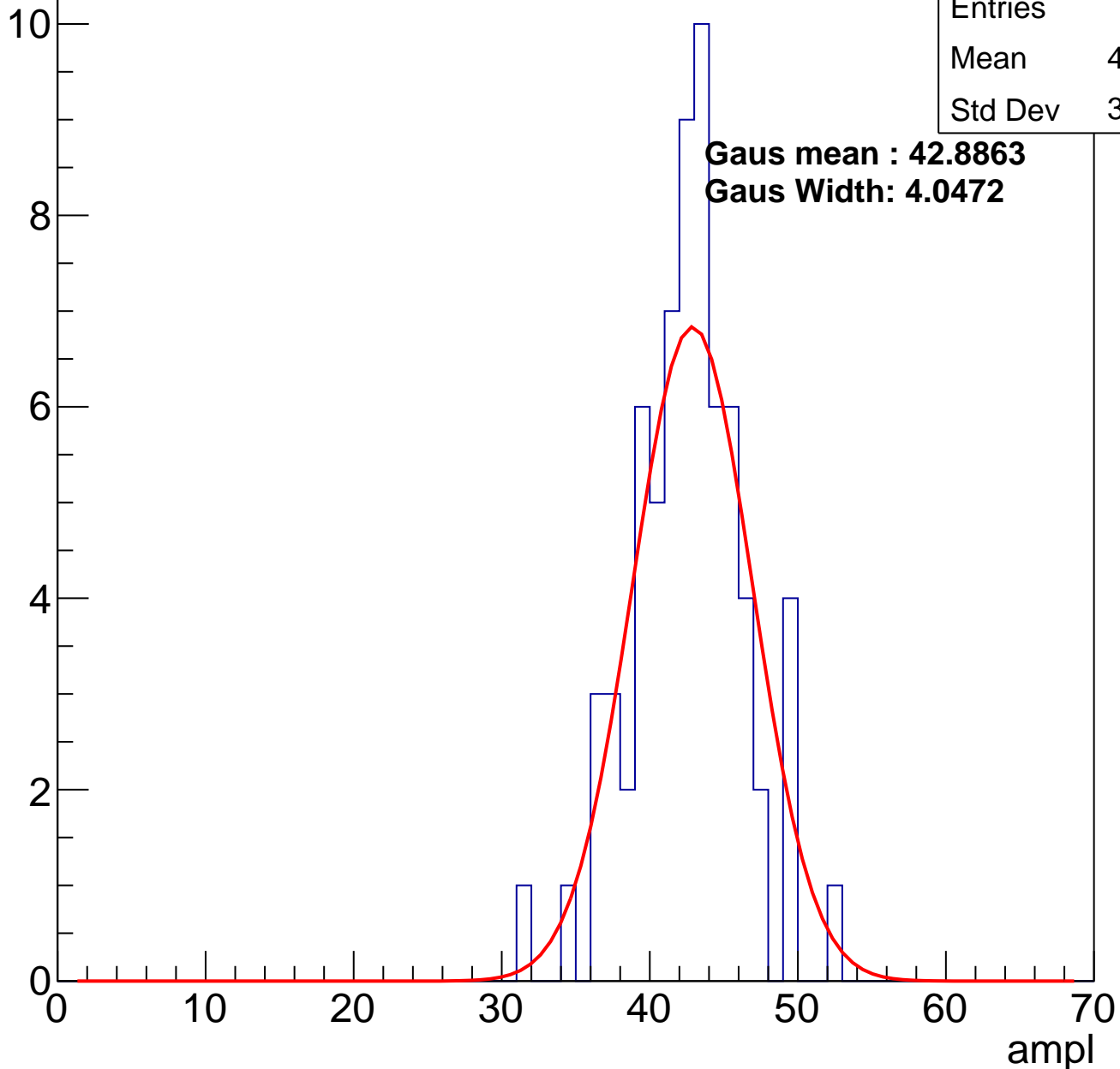
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	70
Mean	42.13
Std Dev	3.738

**Gaus mean : 42.8863**

**Gaus Width: 4.0472**

Entry

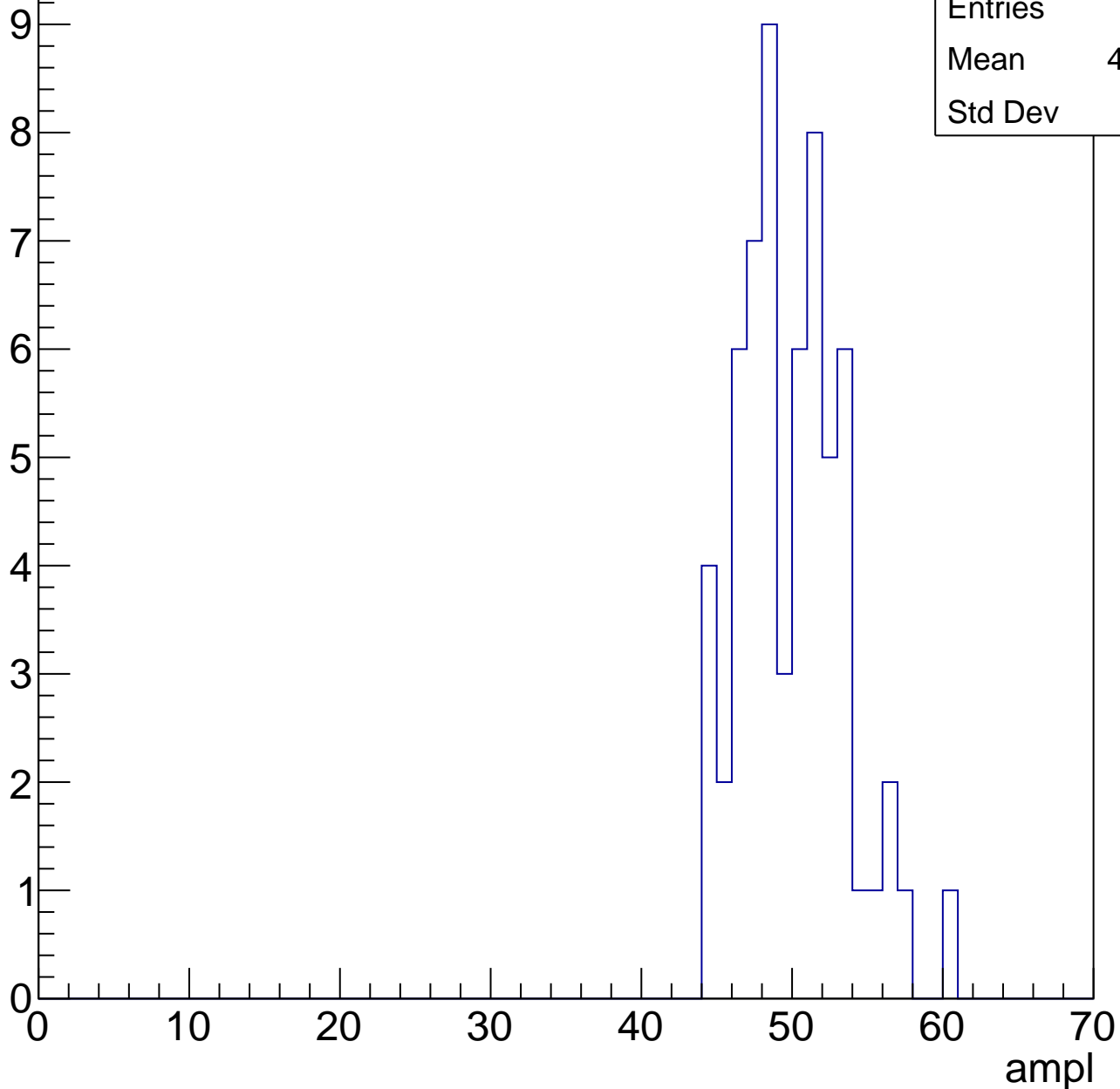


# B1L101S, U16-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	49.58
Std Dev	3.42

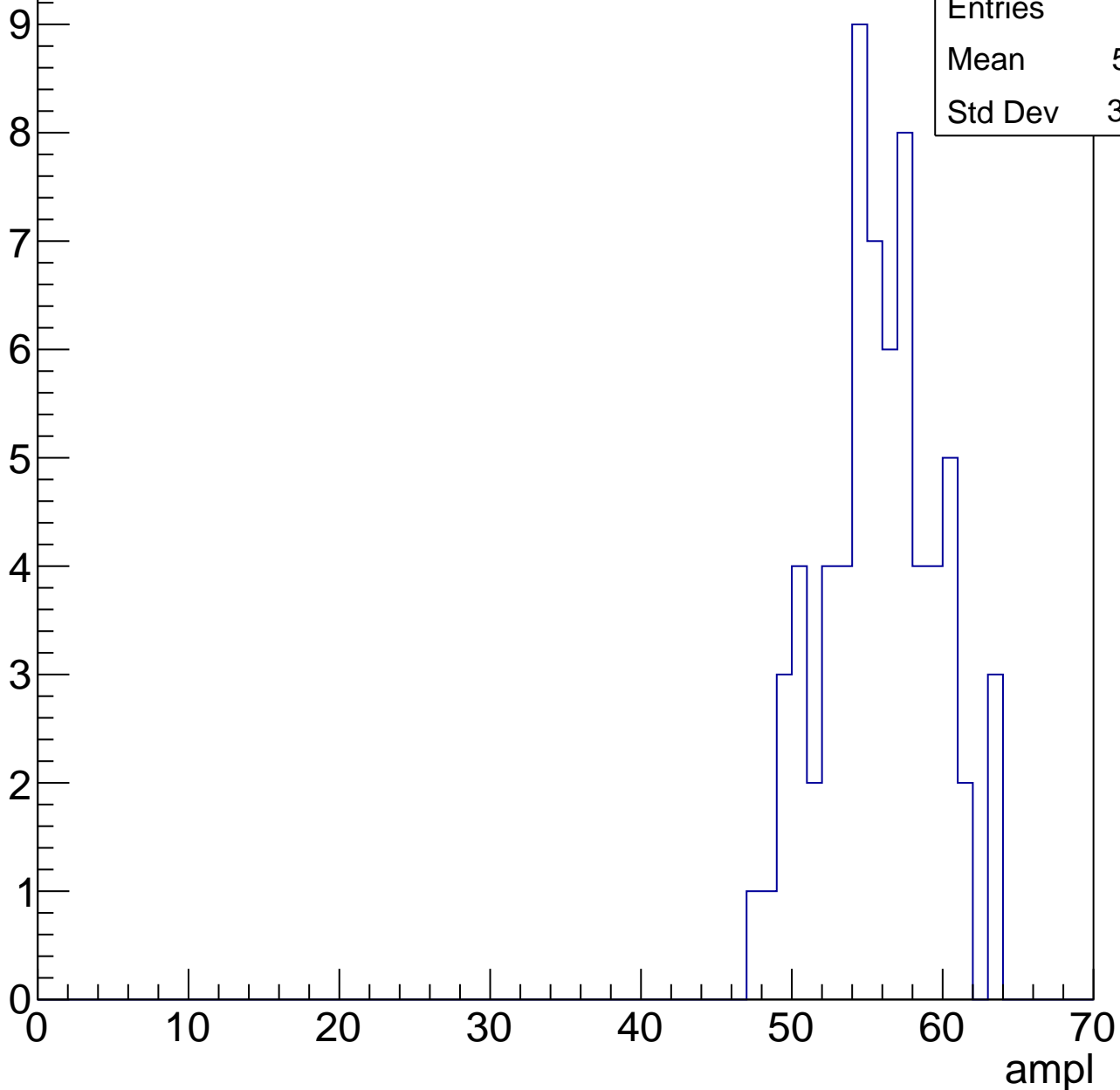


# B1L101S, U16-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	55.31
Std Dev	3.735

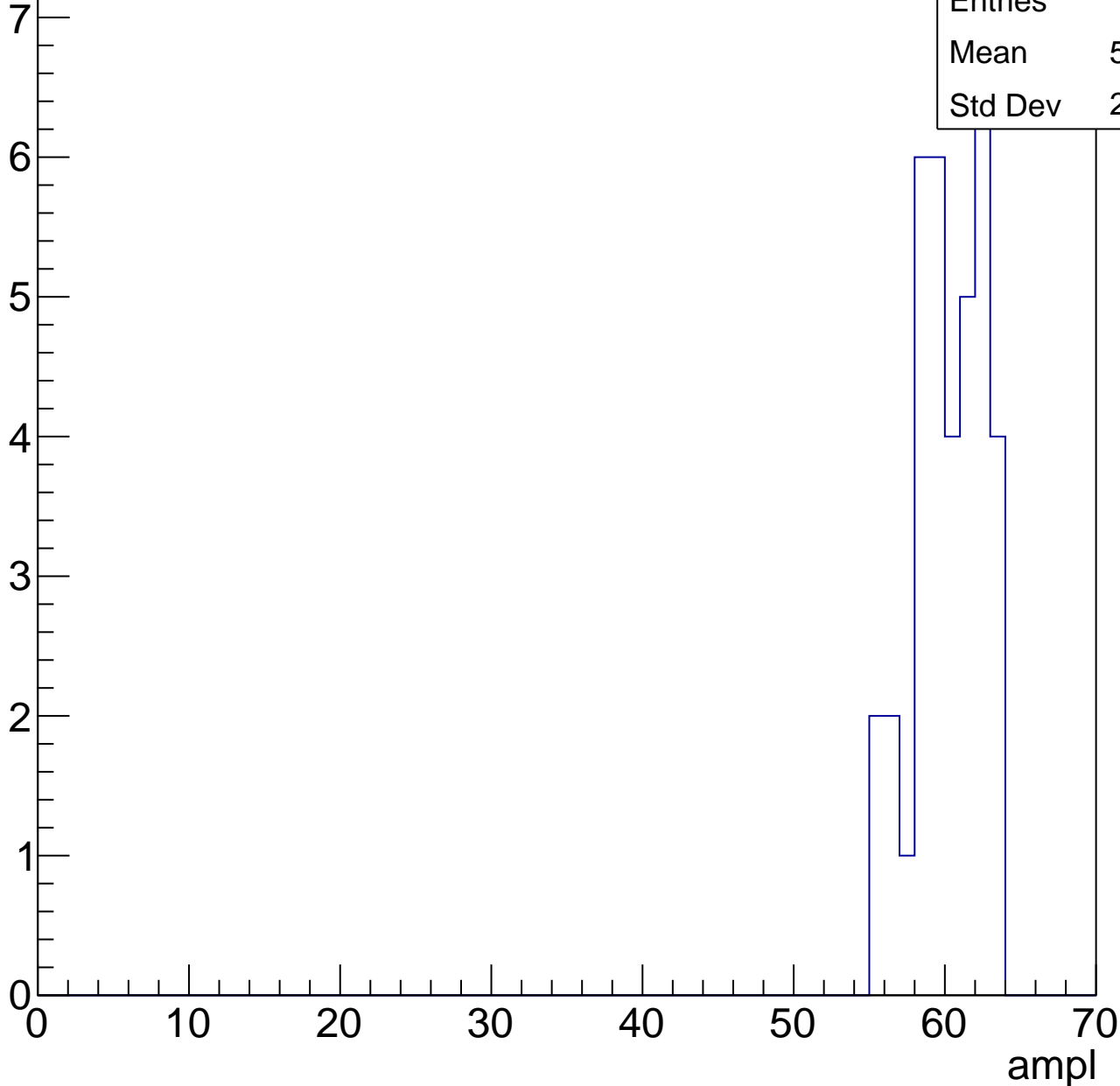


# B1L101S, U16-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	37
Mean	59.78
Std Dev	2.256



# B1L101S, U16-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

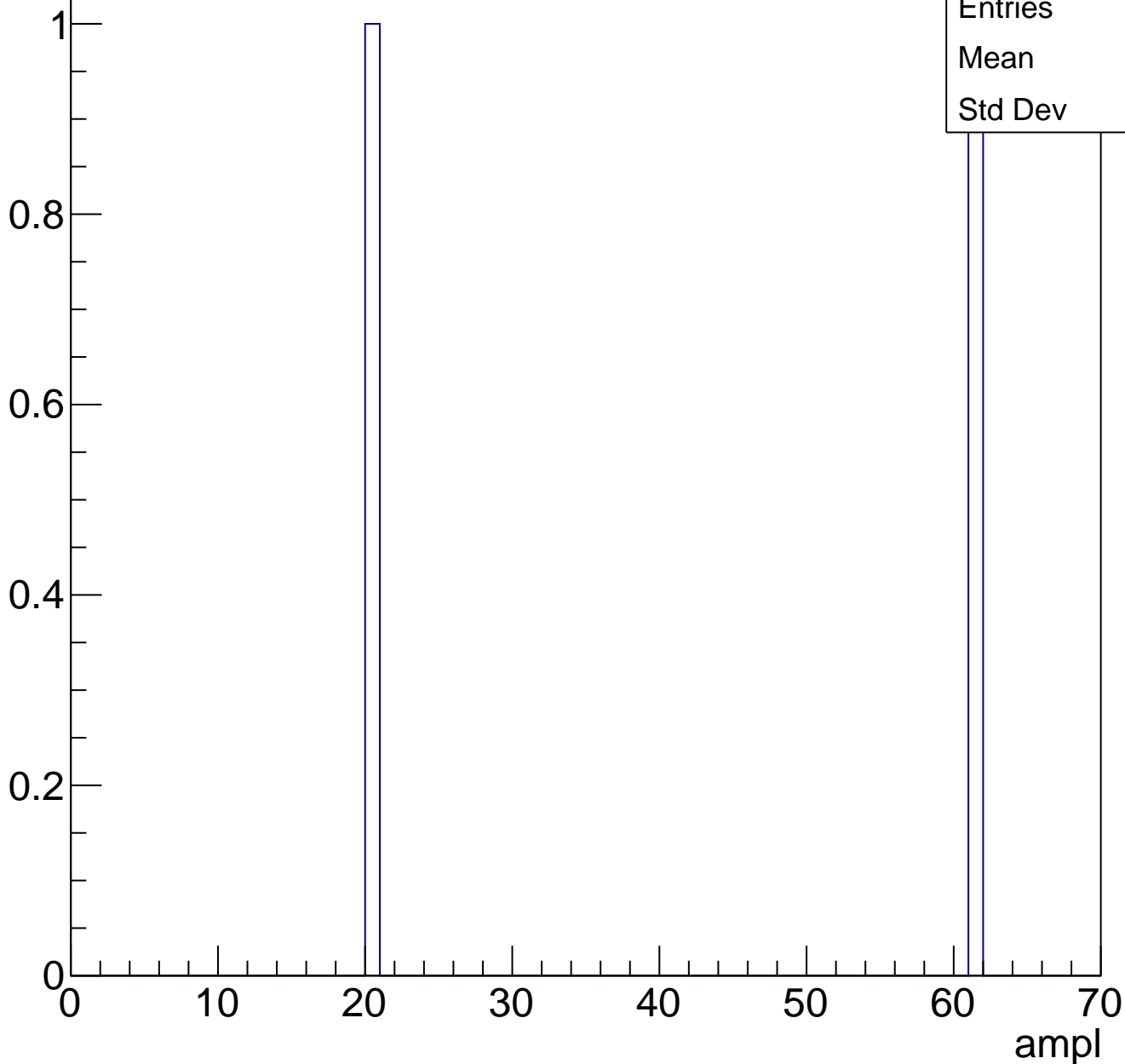
Entries	9
Mean	55.22
Std Dev	19.54



# B1L101S, U16-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch41, adc0

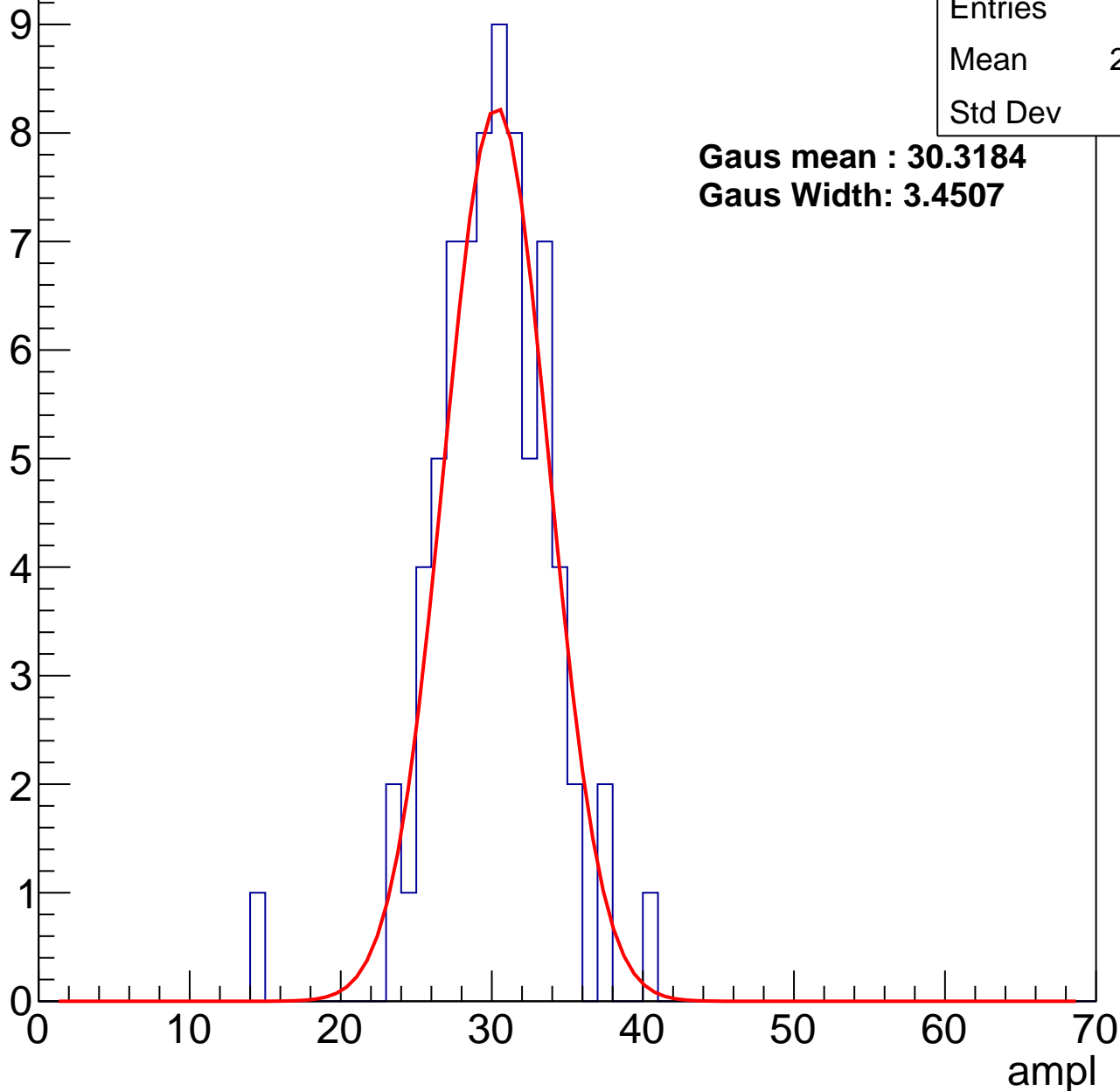
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	29.59
Std Dev	3.81

**Gaus mean : 30.3184**

**Gaus Width: 3.4507**



# B1L101S, U16-ch41, adc1

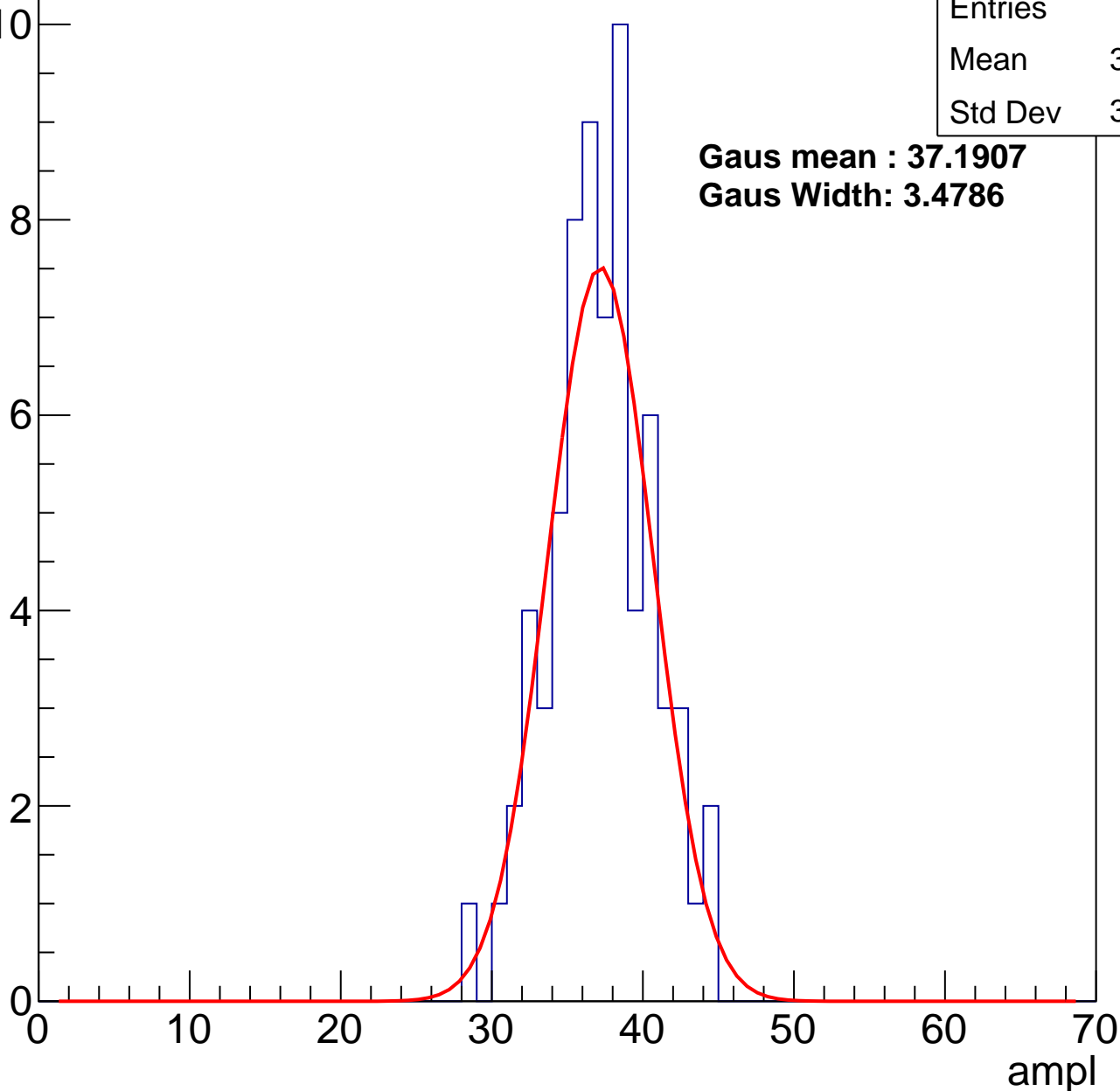
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	36.75
Std Dev	3.338

**Gaus mean : 37.1907**

**Gaus Width: 3.4786**

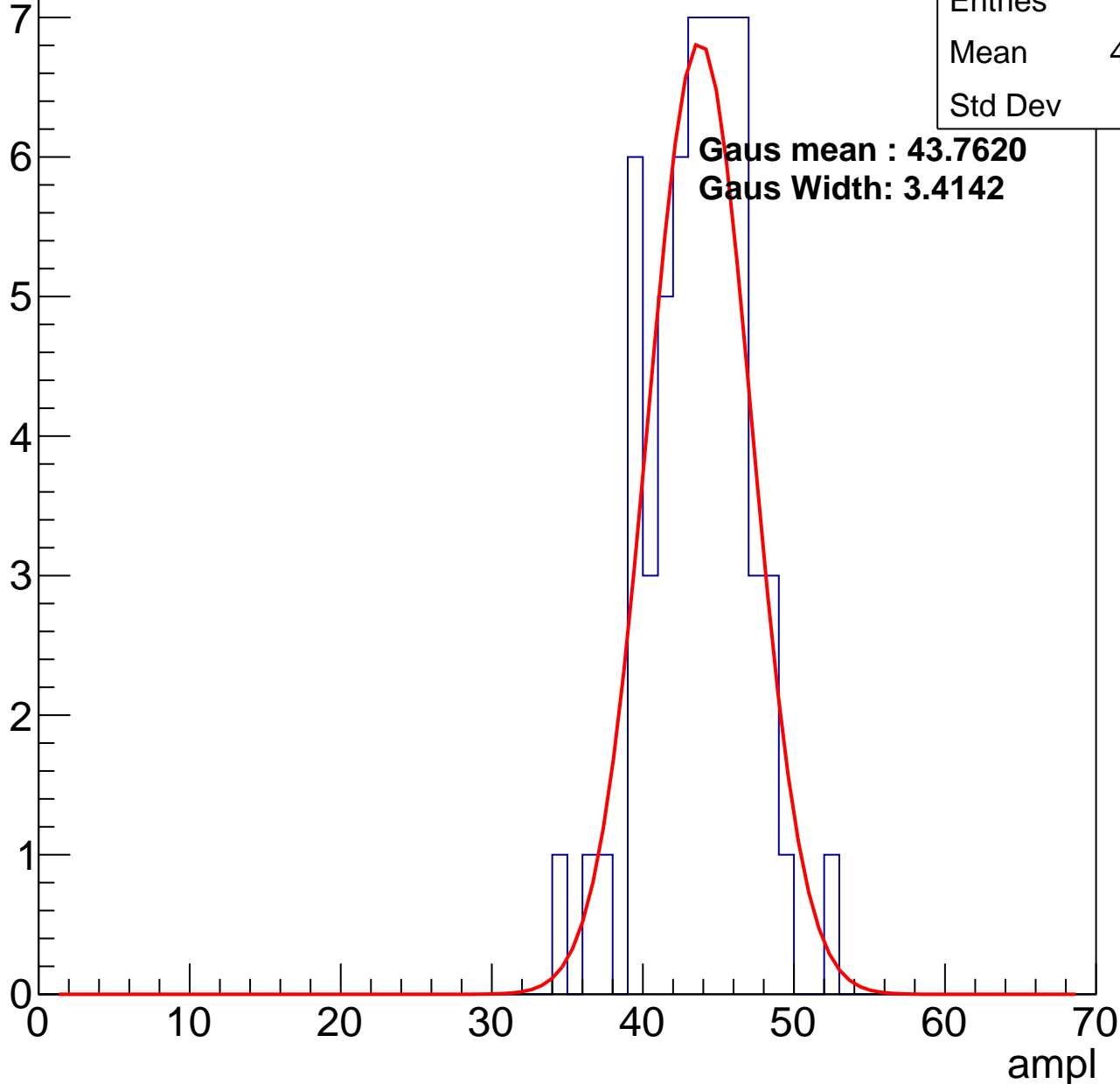


# B1L101S, U16-ch41, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	43.22
Std Dev	3.32

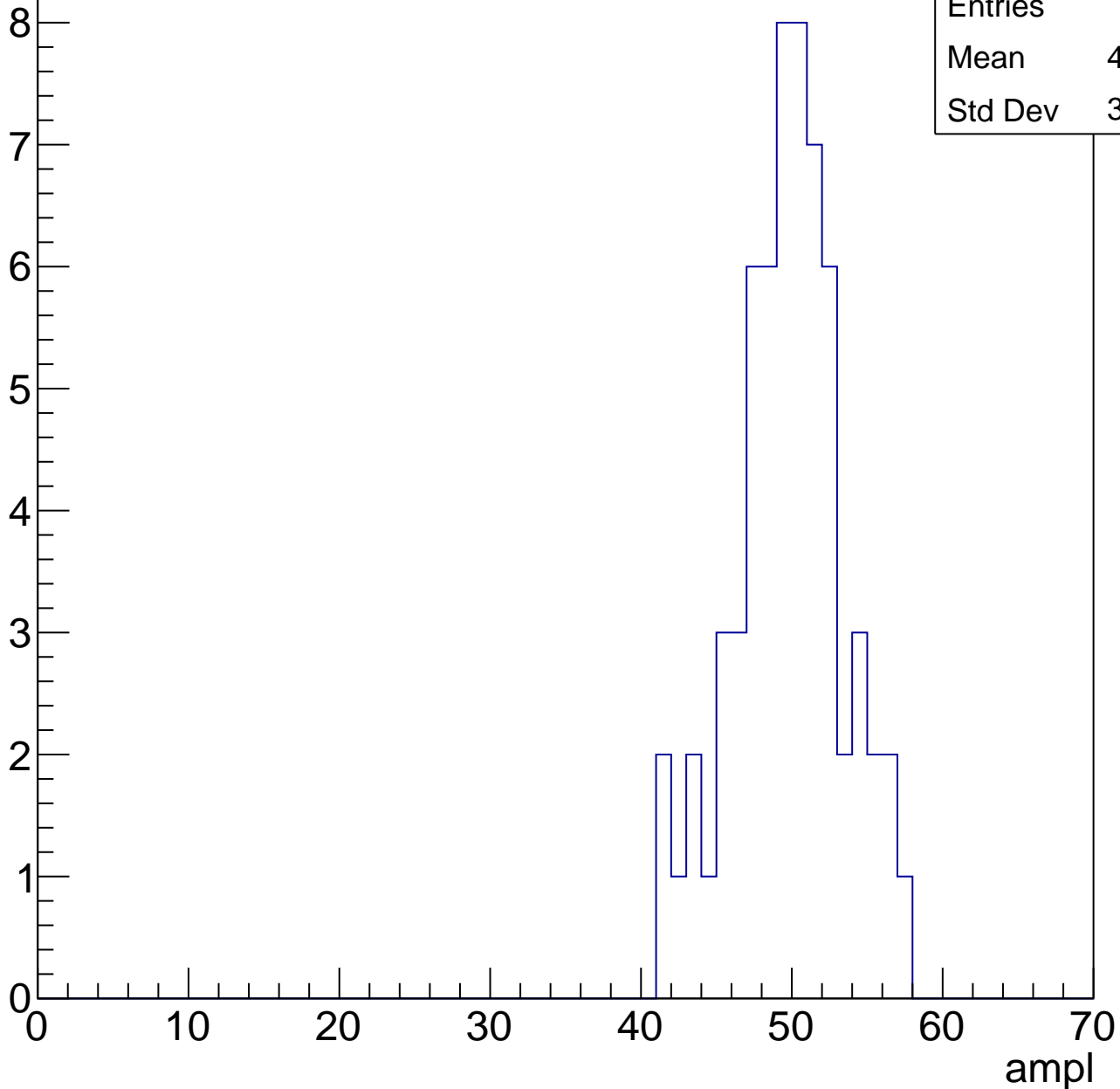


# B1L101S, U16-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	49.29
Std Dev	3.574

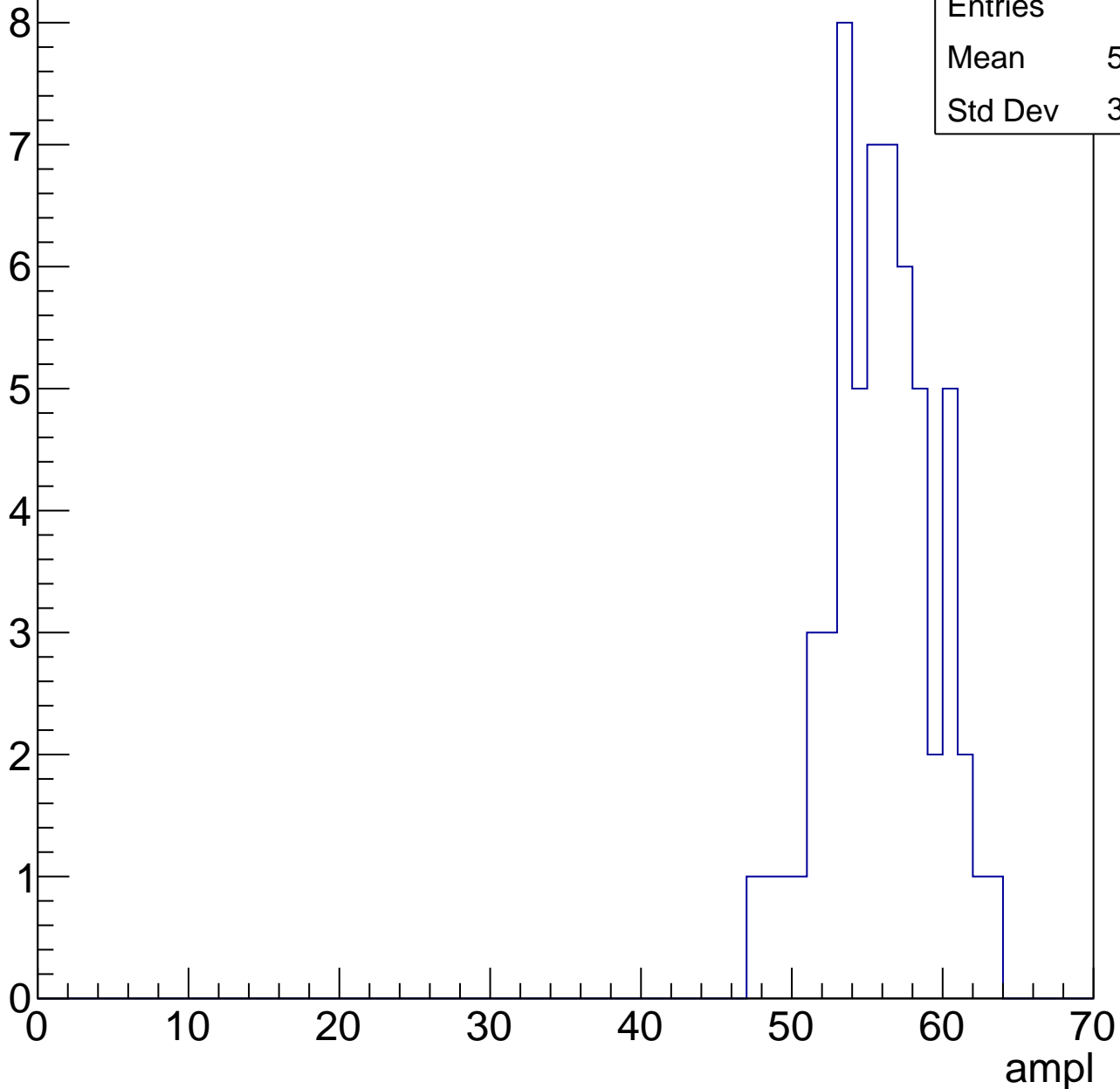


# B1L101S, U16-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	55.44
Std Dev	3.426

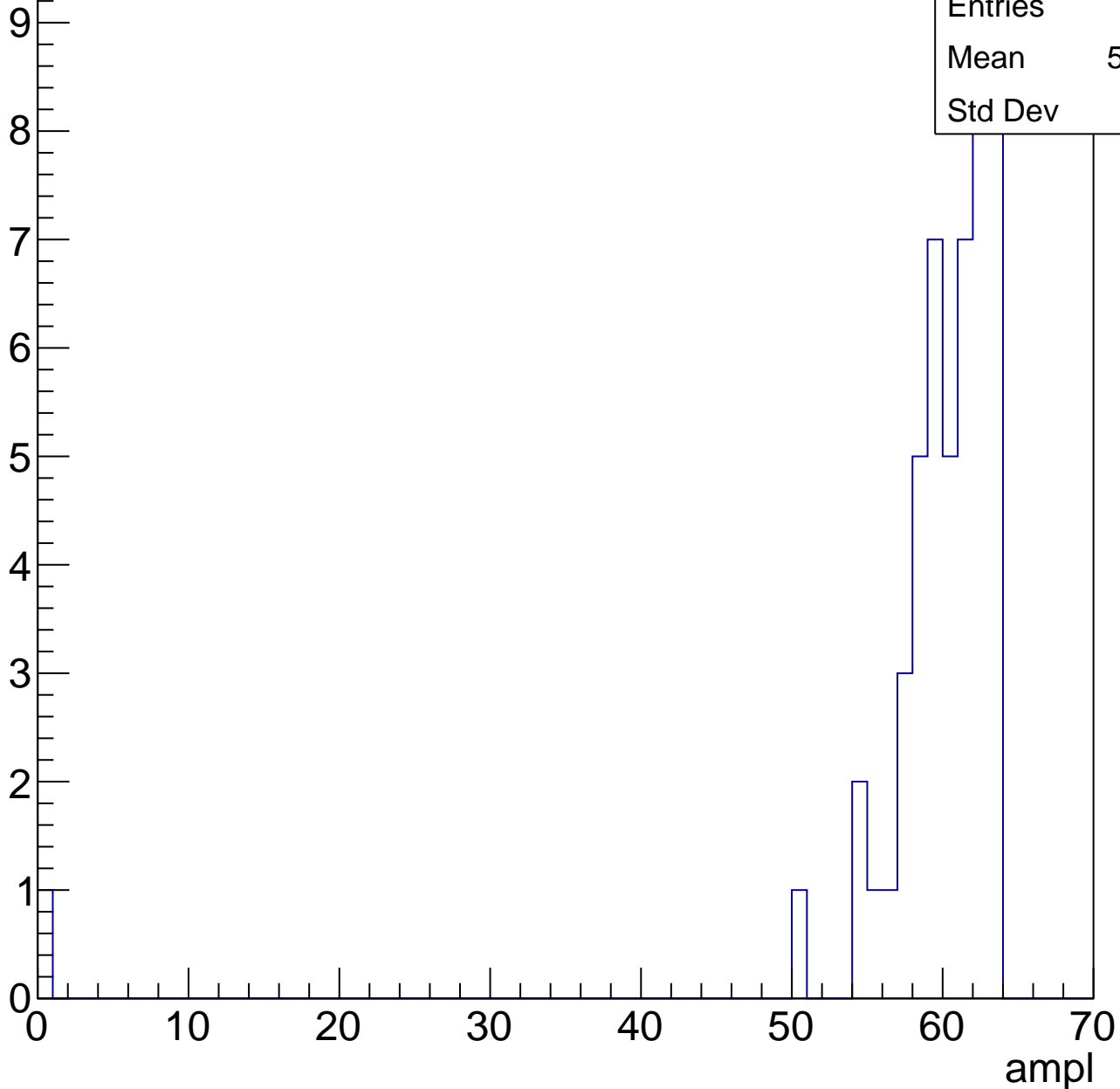


# B1L101S, U16-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

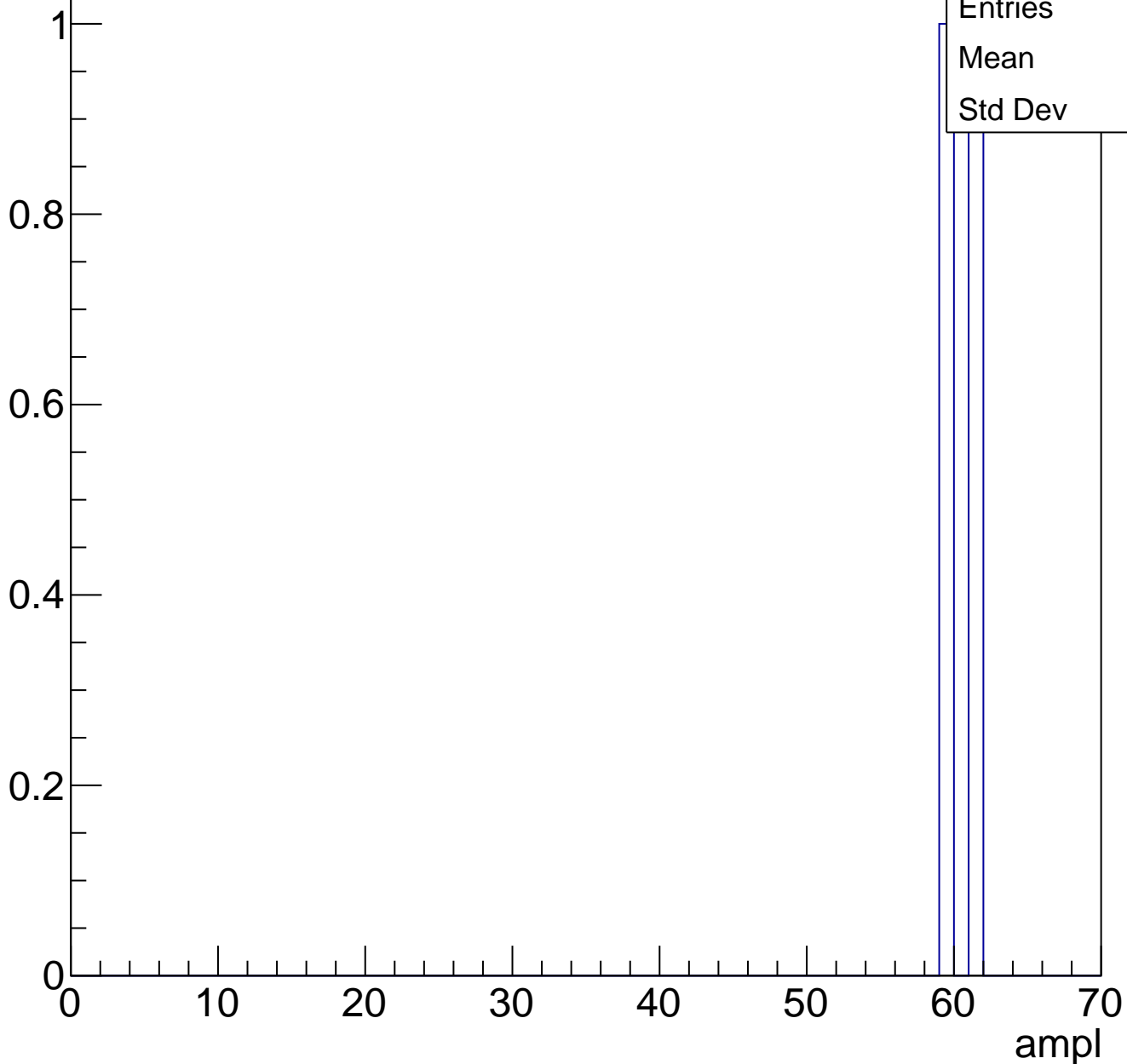
Entries	50
Mean	58.64
Std Dev	8.82



# B1L101S, U16-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L101S, U16-ch42, adc0

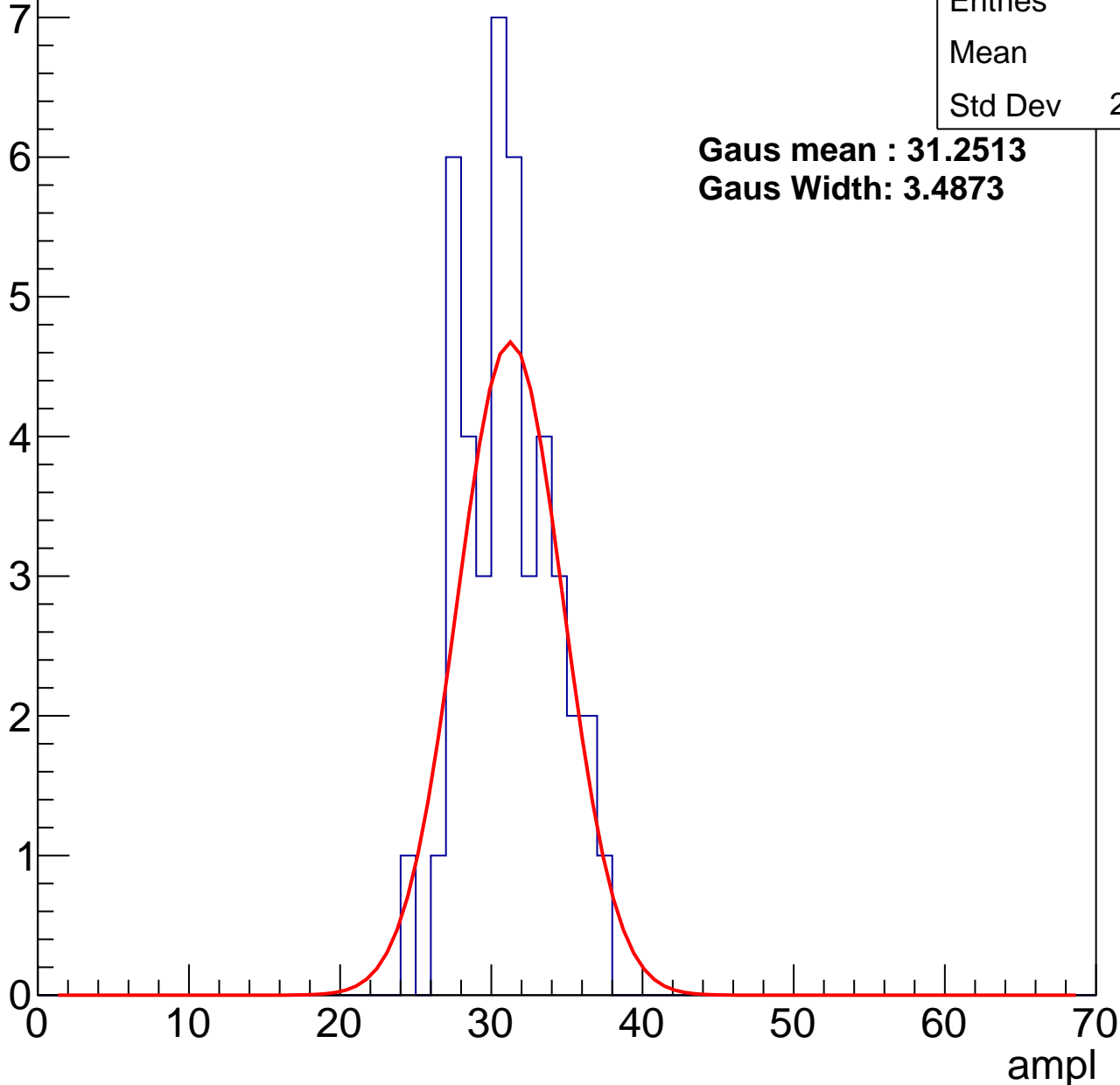
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	30.6
Std Dev	2.982

**Gaus mean : 31.2513**

**Gaus Width: 3.4873**



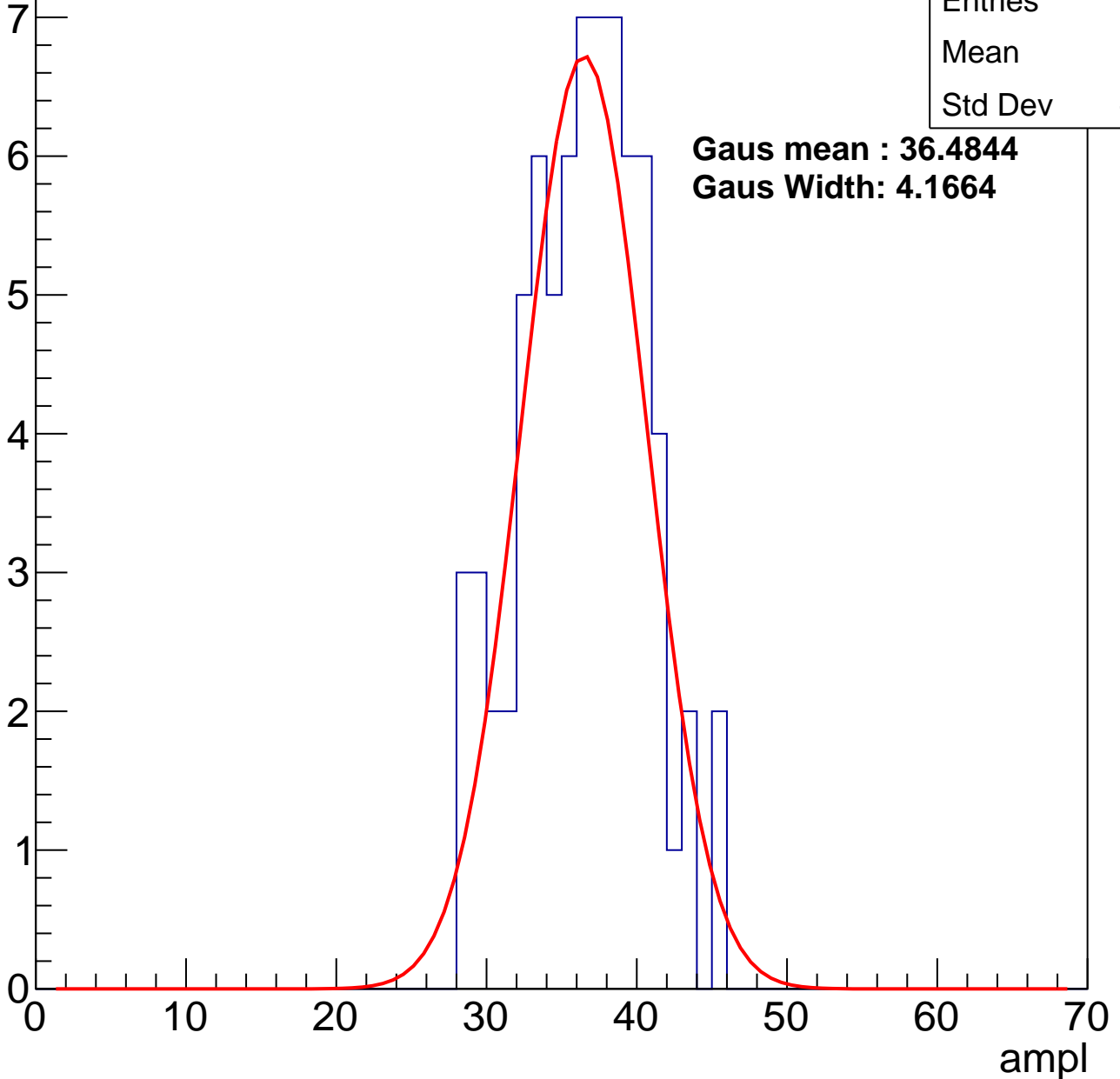
# B1L101S, U16-ch42, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	36
Std Dev	4.03

**Gaus mean : 36.4844**  
**Gaus Width: 4.1664**



# B1L101S, U16-ch42, adc2

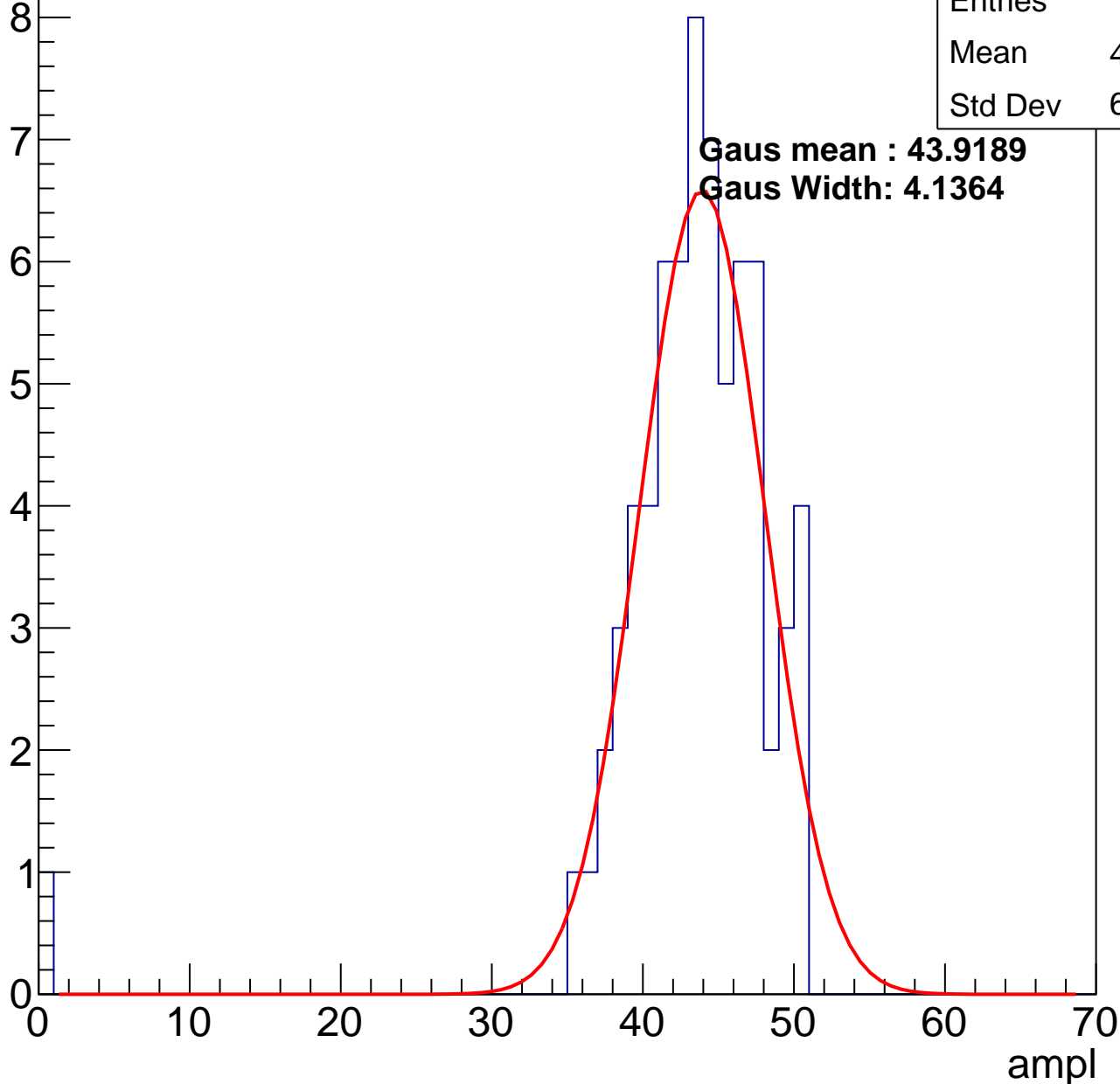
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	42.77
Std Dev	6.332

**Gaus mean : 43.9189**

**Gaus Width: 4.1364**

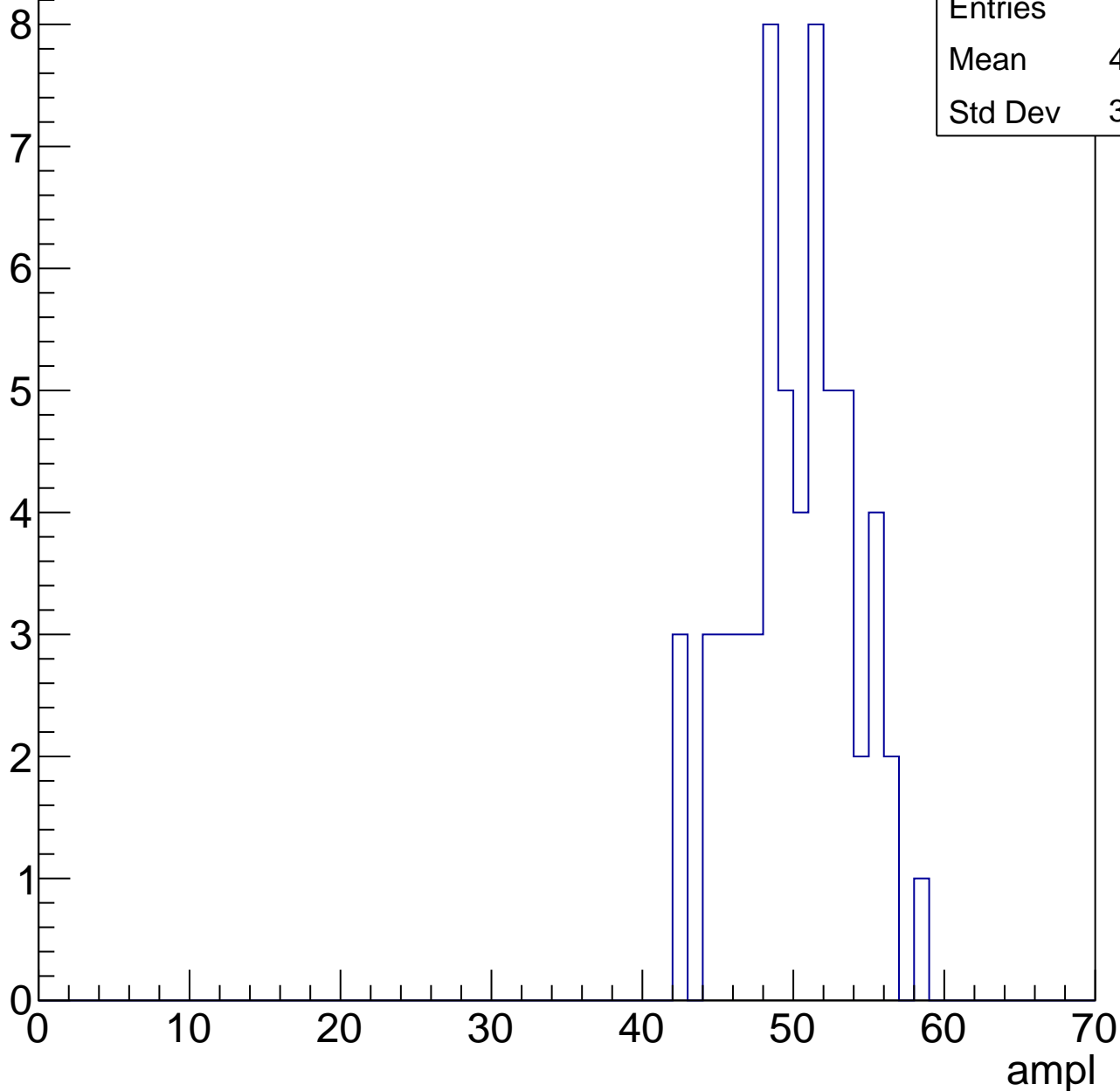


# B1L101S, U16-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	49.69
Std Dev	3.734

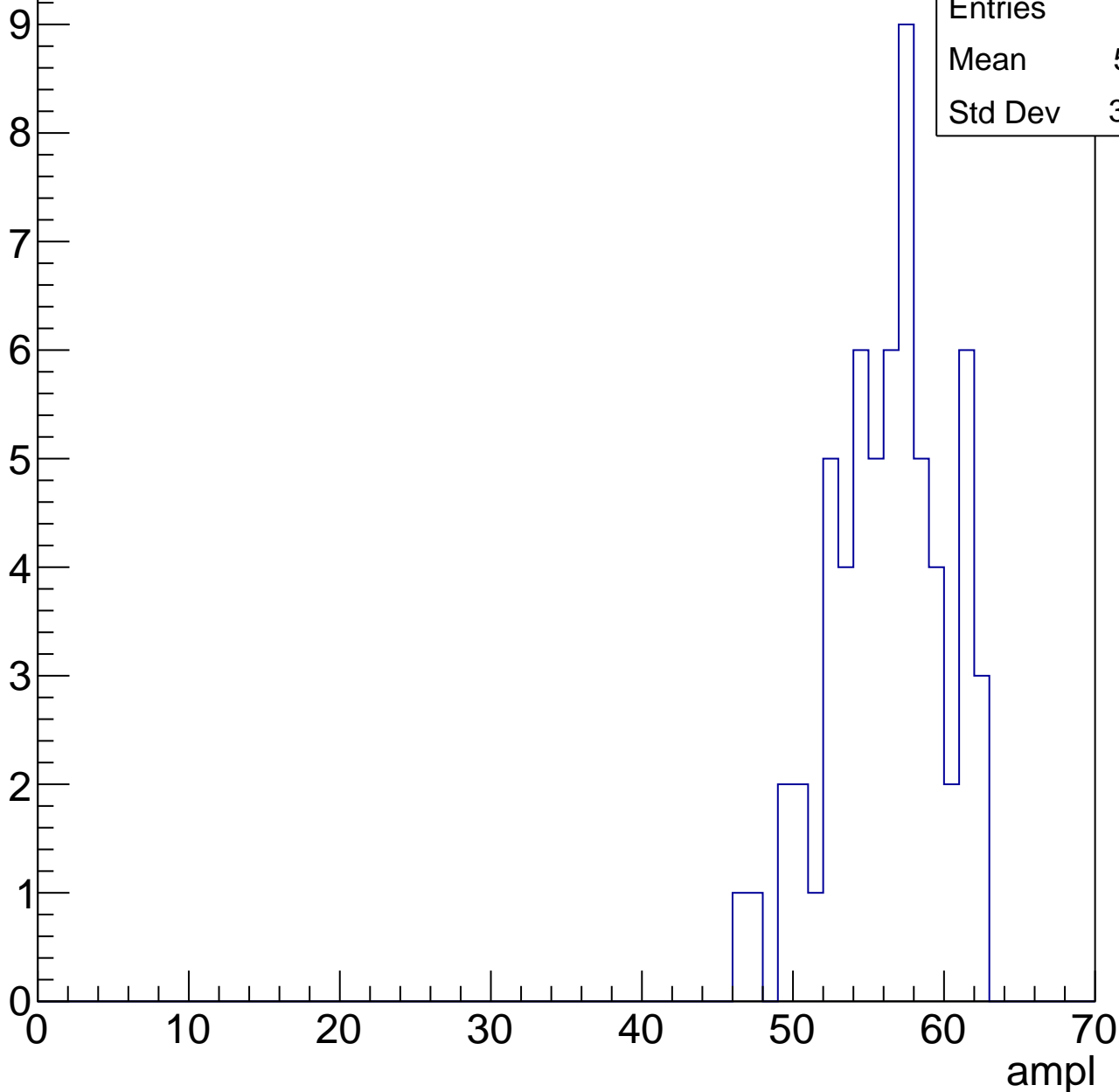


# B1L101S, U16-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	55.81
Std Dev	3.754

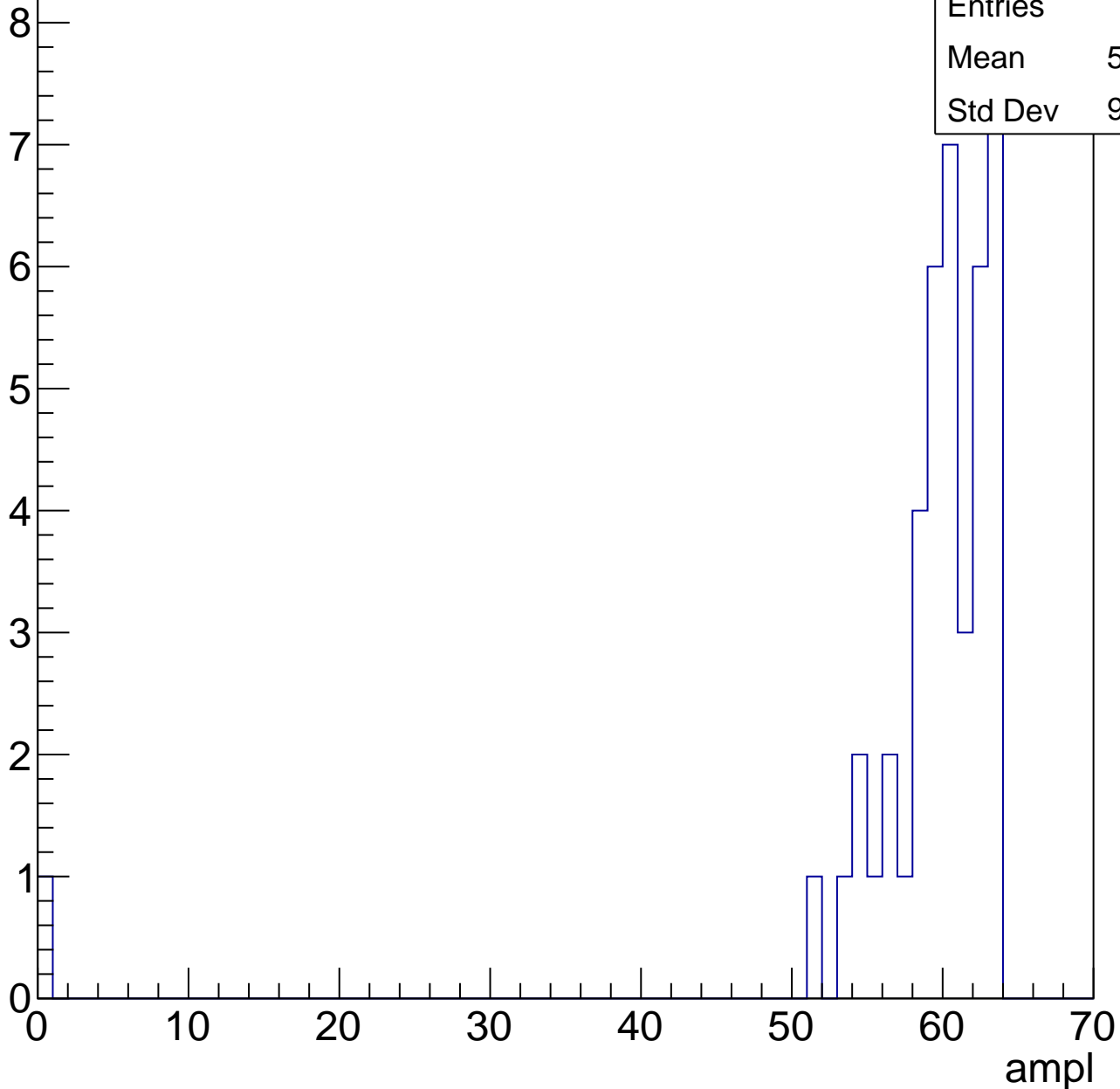


# B1L101S, U16-ch42, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	58.16
Std Dev	9.455



# B1L101S, U16-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.8
Std Dev	1.166

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch43, adc0

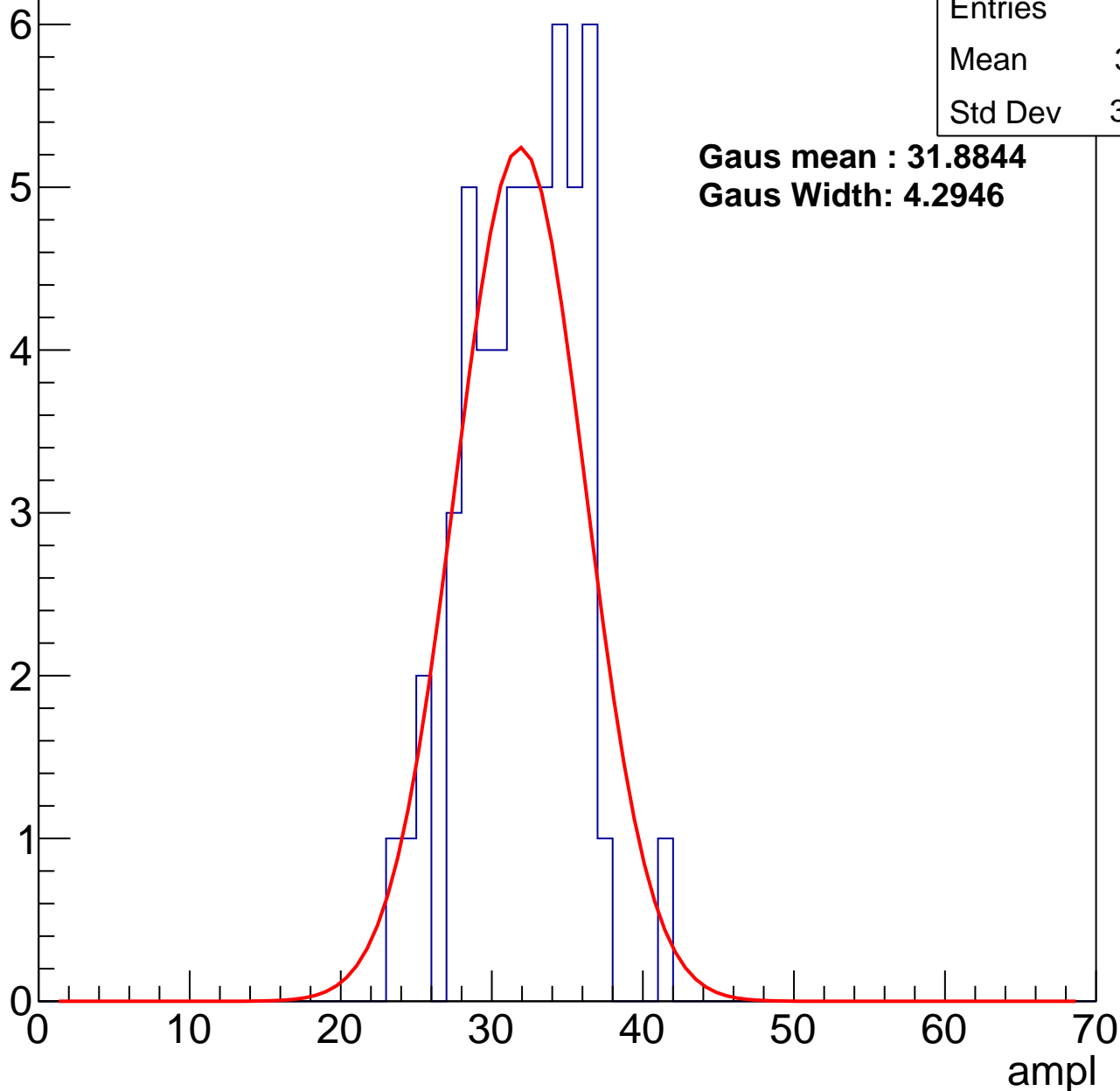
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	31.61
Std Dev	3.659

**Gaus mean : 31.8844**

**Gaus Width: 4.2946**



# B1L101S, U16-ch43, adc1

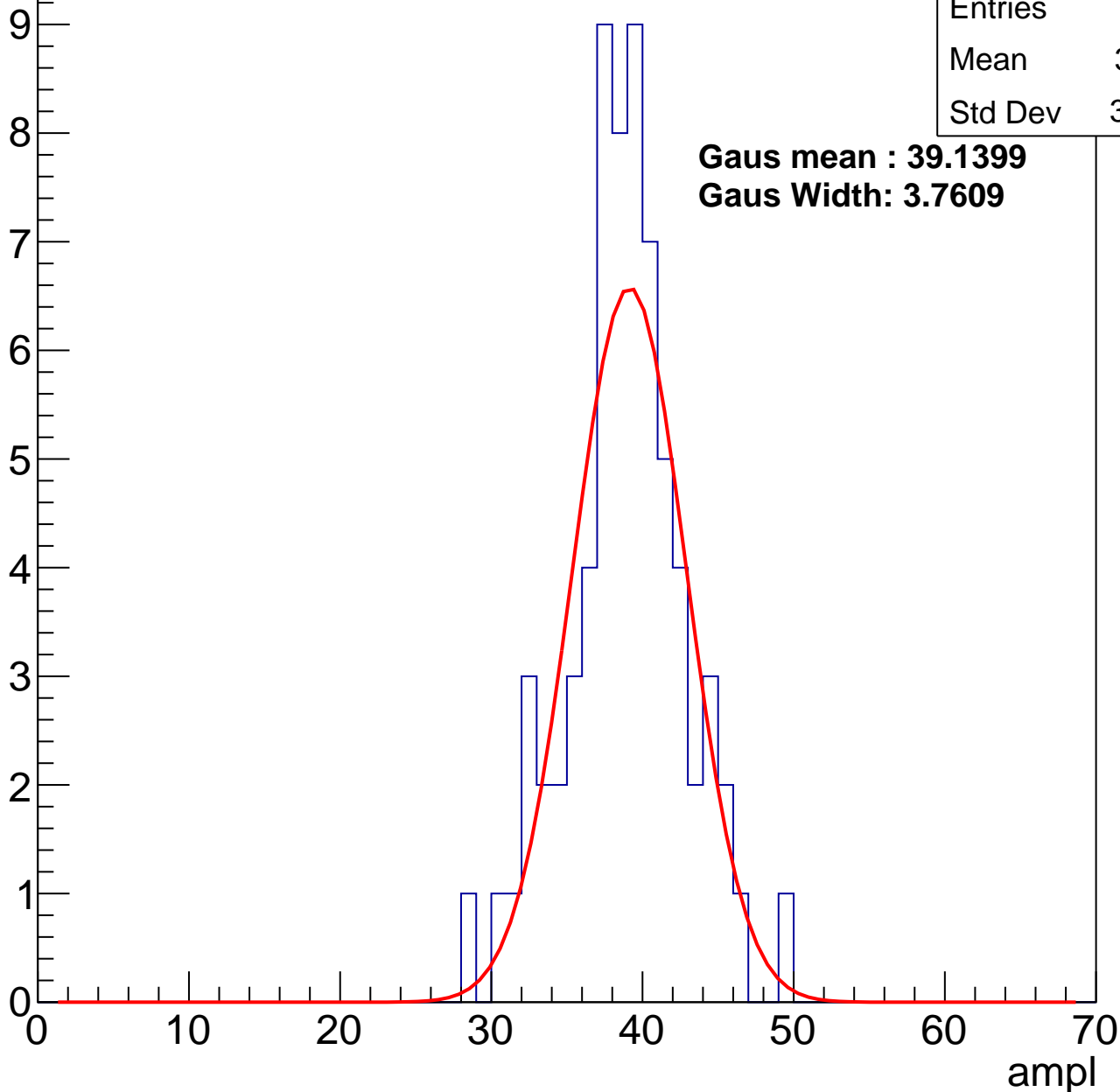
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	38.41
Std Dev	3.893

**Gaus mean : 39.1399**

**Gaus Width: 3.7609**



# B1L101S, U16-ch43, adc2

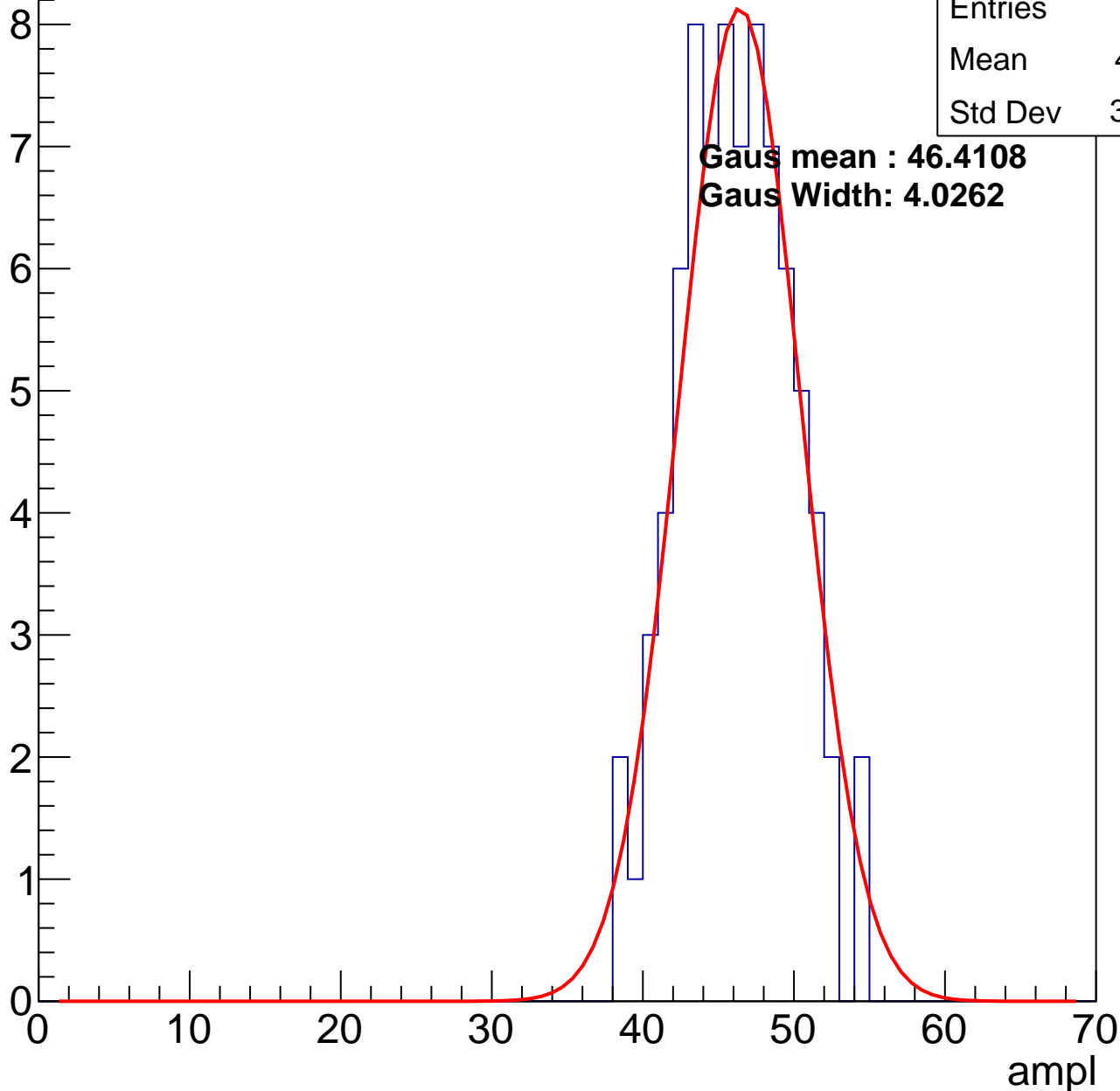
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	45.71
Std Dev	3.627

**Gaus mean : 46.4108**

**Gaus Width: 4.0262**

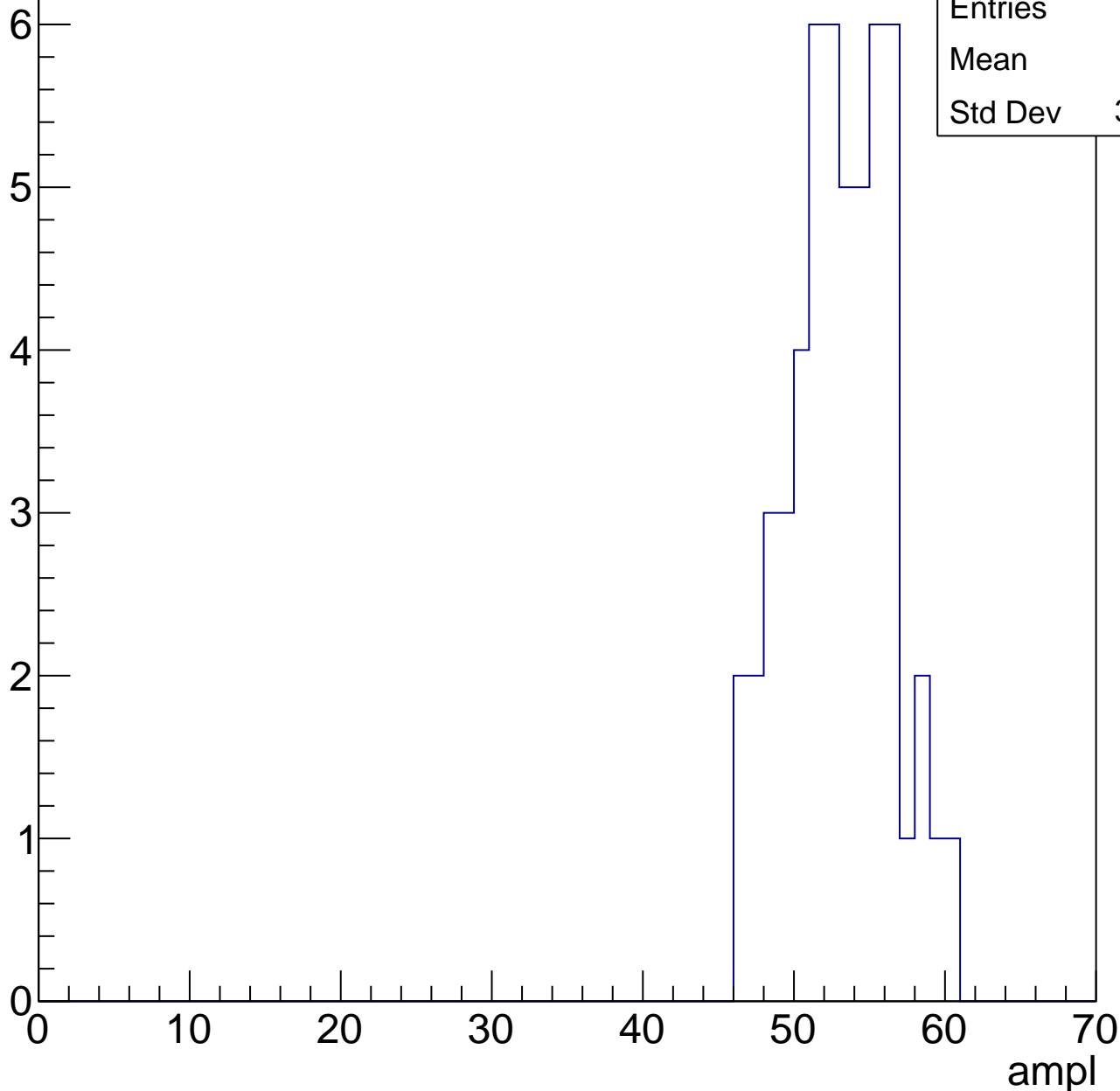


# B1L101S, U16-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

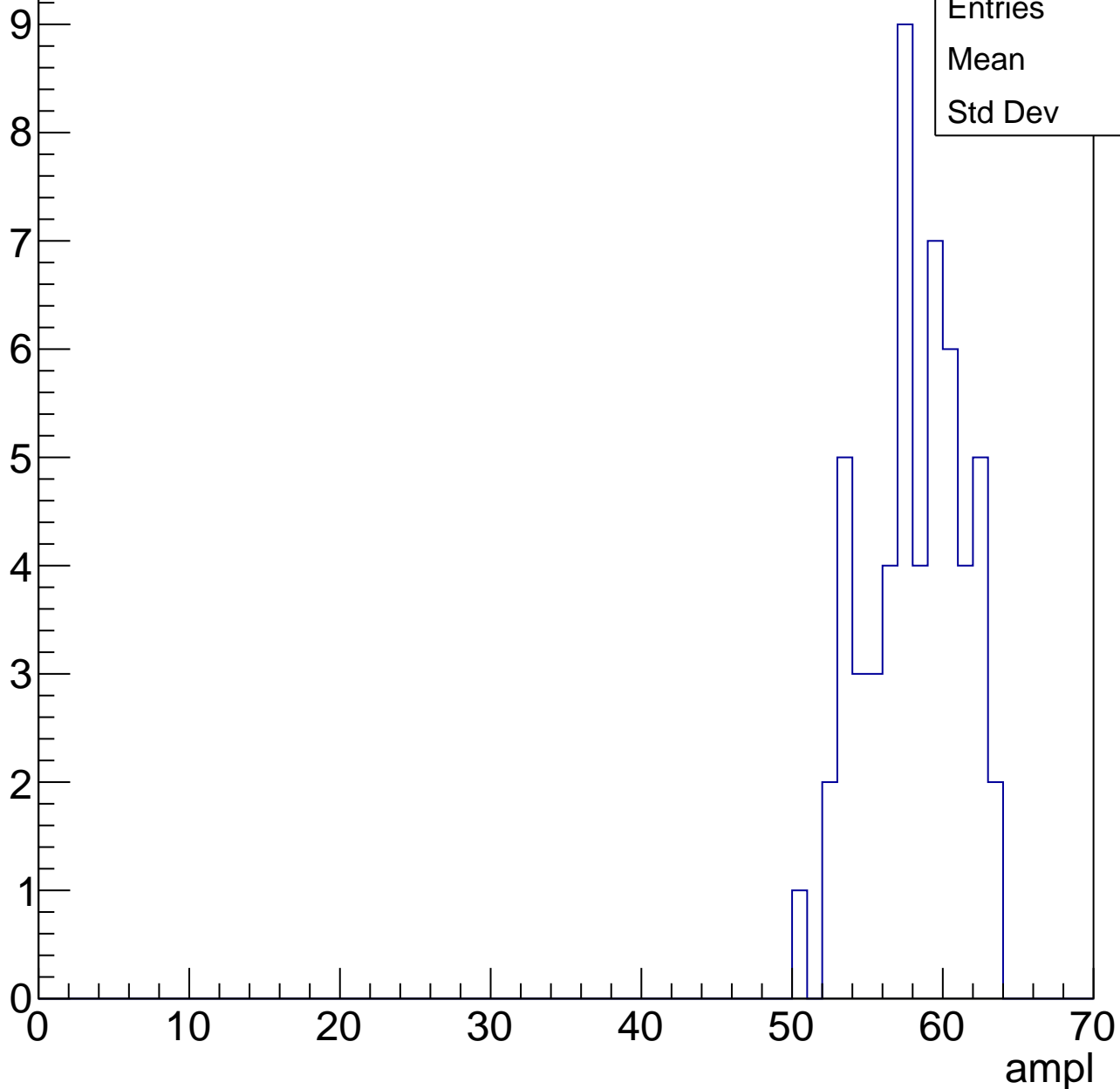
Entries	53
Mean	52.6
Std Dev	3.321



# B1L101S, U16-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

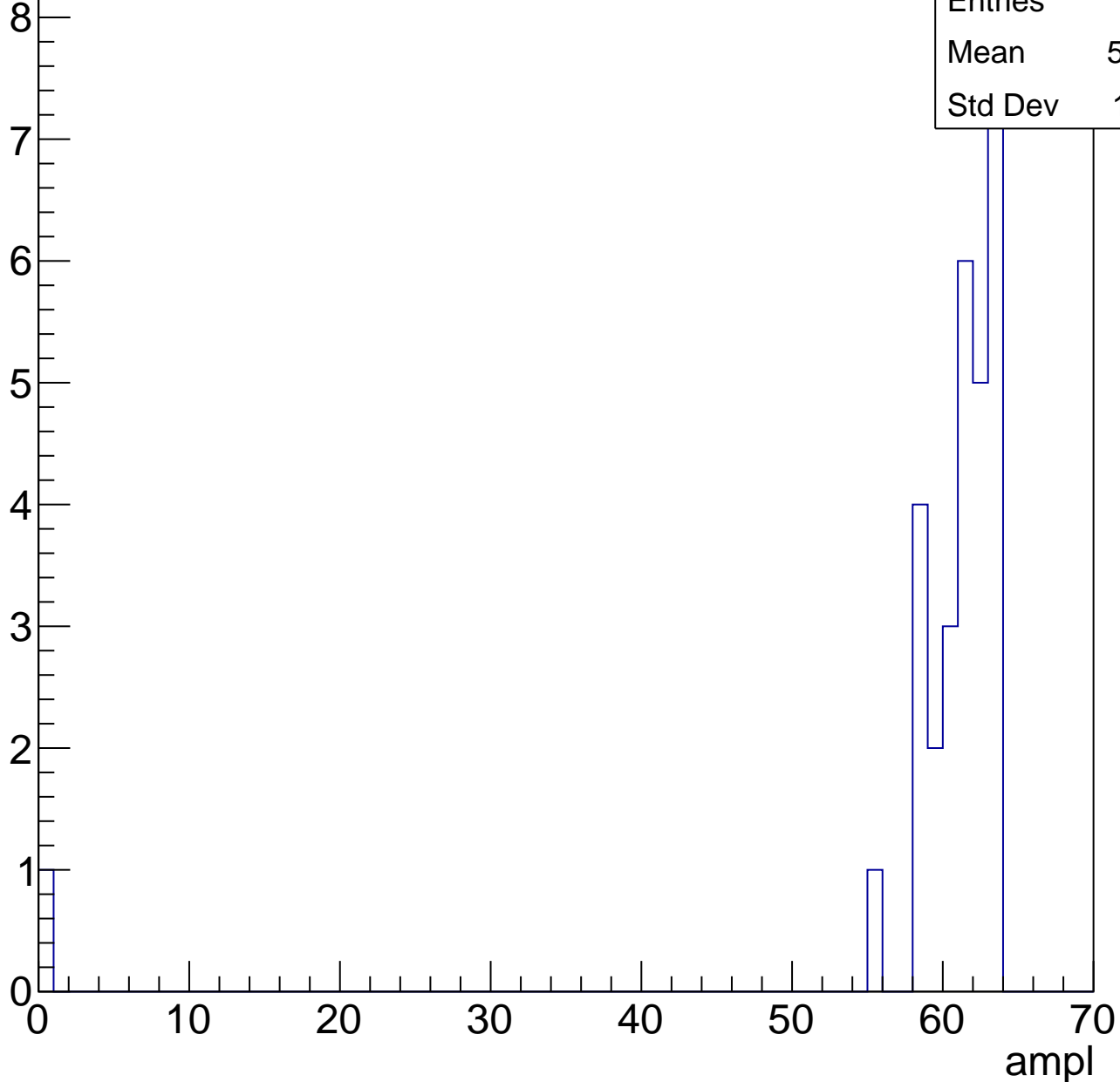


# B1L101S, U16-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	30
Mean	58.83
Std Dev	11.11



# B1L101S, U16-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U16-ch44, adc0

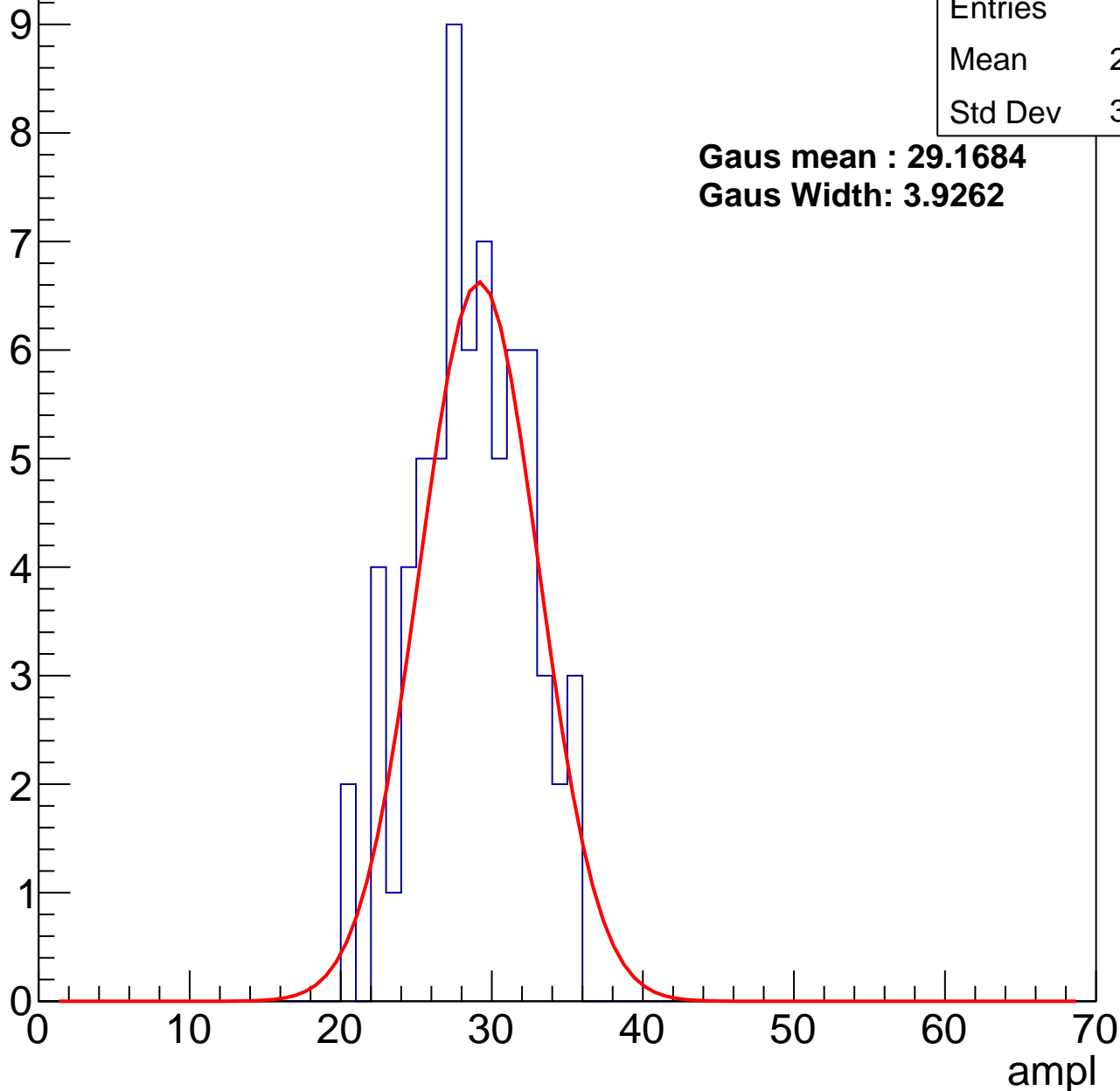
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	28.18
Std Dev	3.646

**Gaus mean : 29.1684**

**Gaus Width: 3.9262**



# B1L101S, U16-ch44, adc1

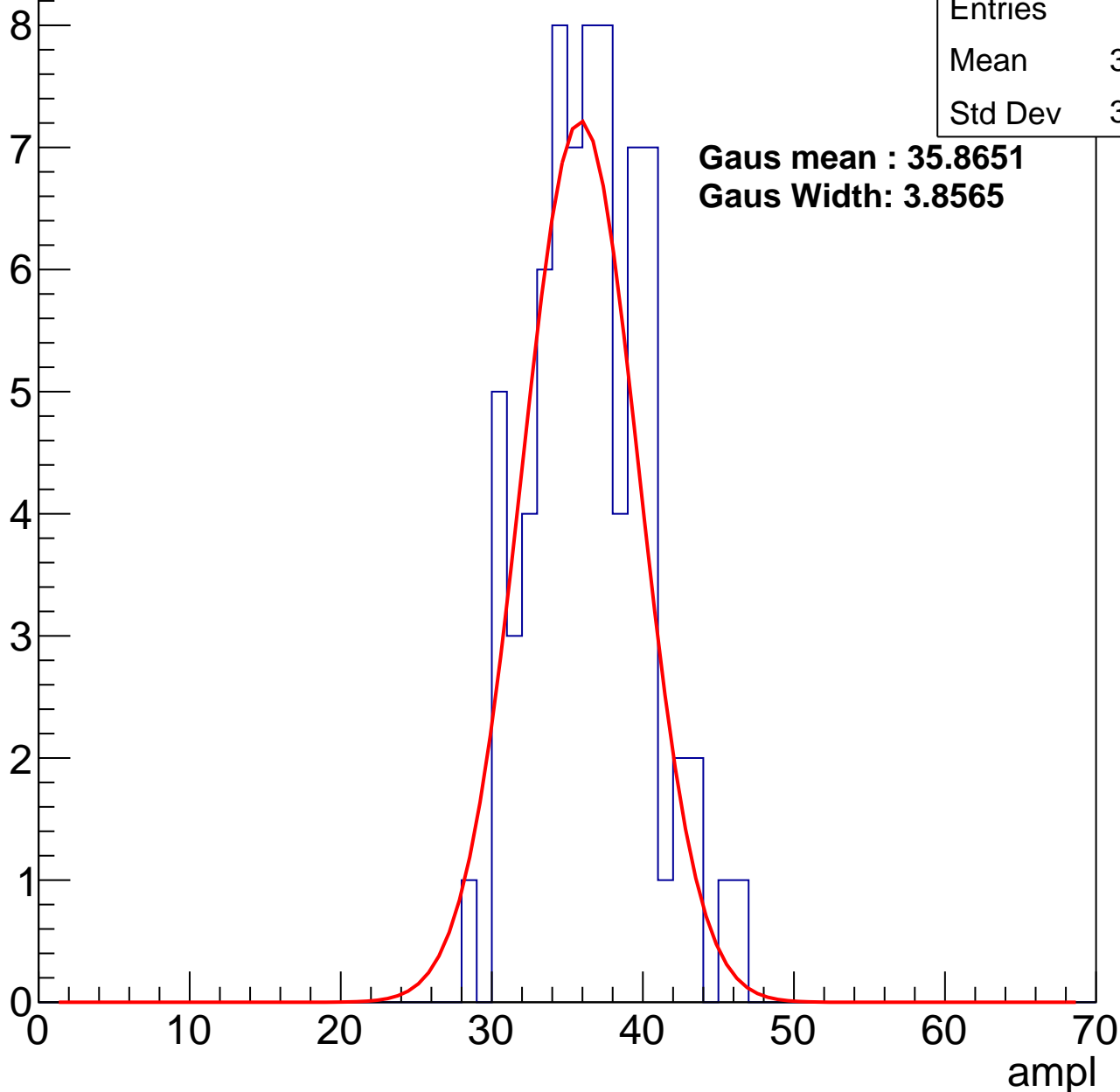
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	36.07
Std Dev	3.743

**Gaus mean : 35.8651**

**Gaus Width: 3.8565**



# B1L101S, U16-ch44, adc2

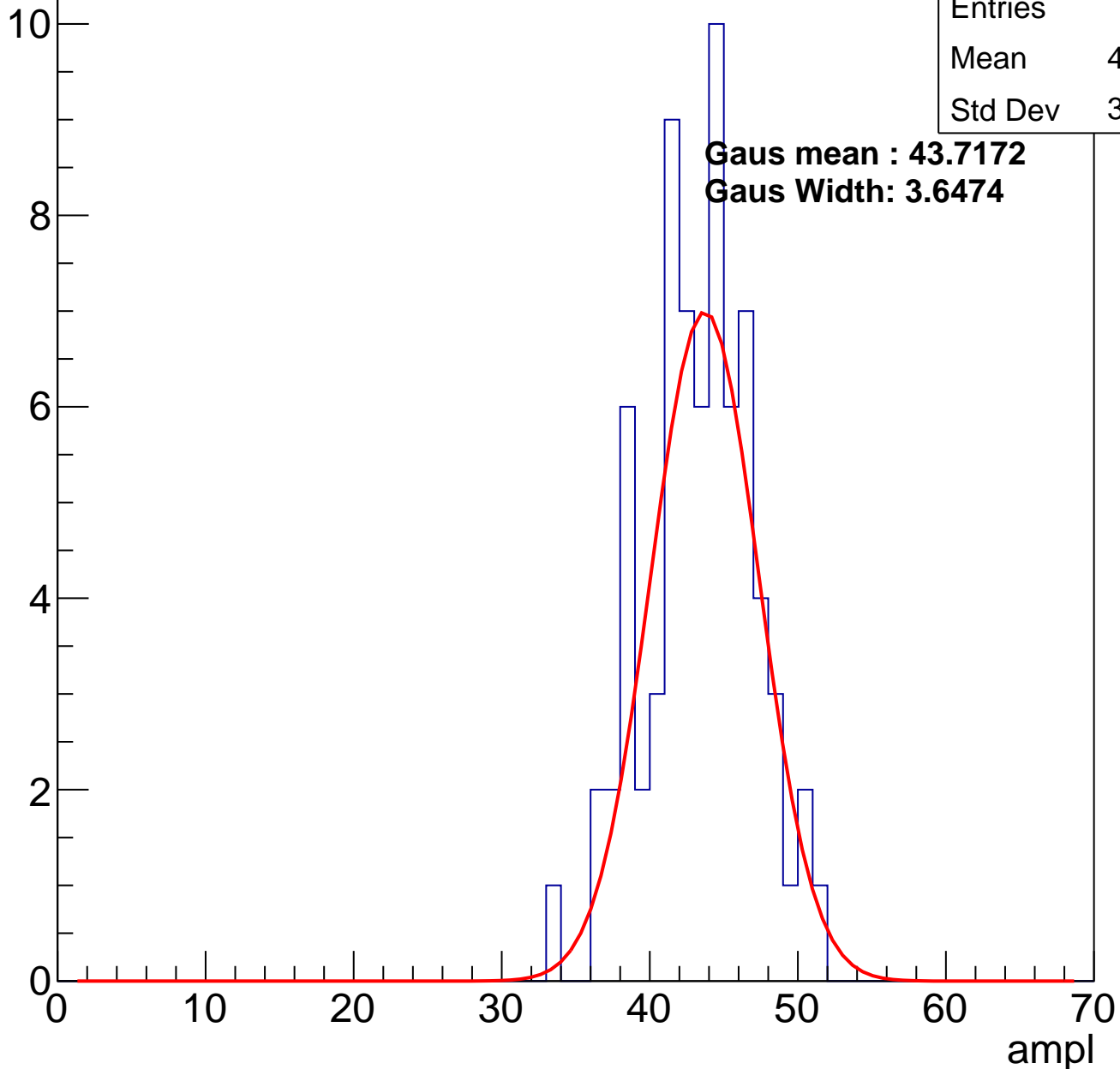
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	72
Mean	42.92
Std Dev	3.643

**Gaus mean : 43.7172**

**Gaus Width: 3.6474**

Entry

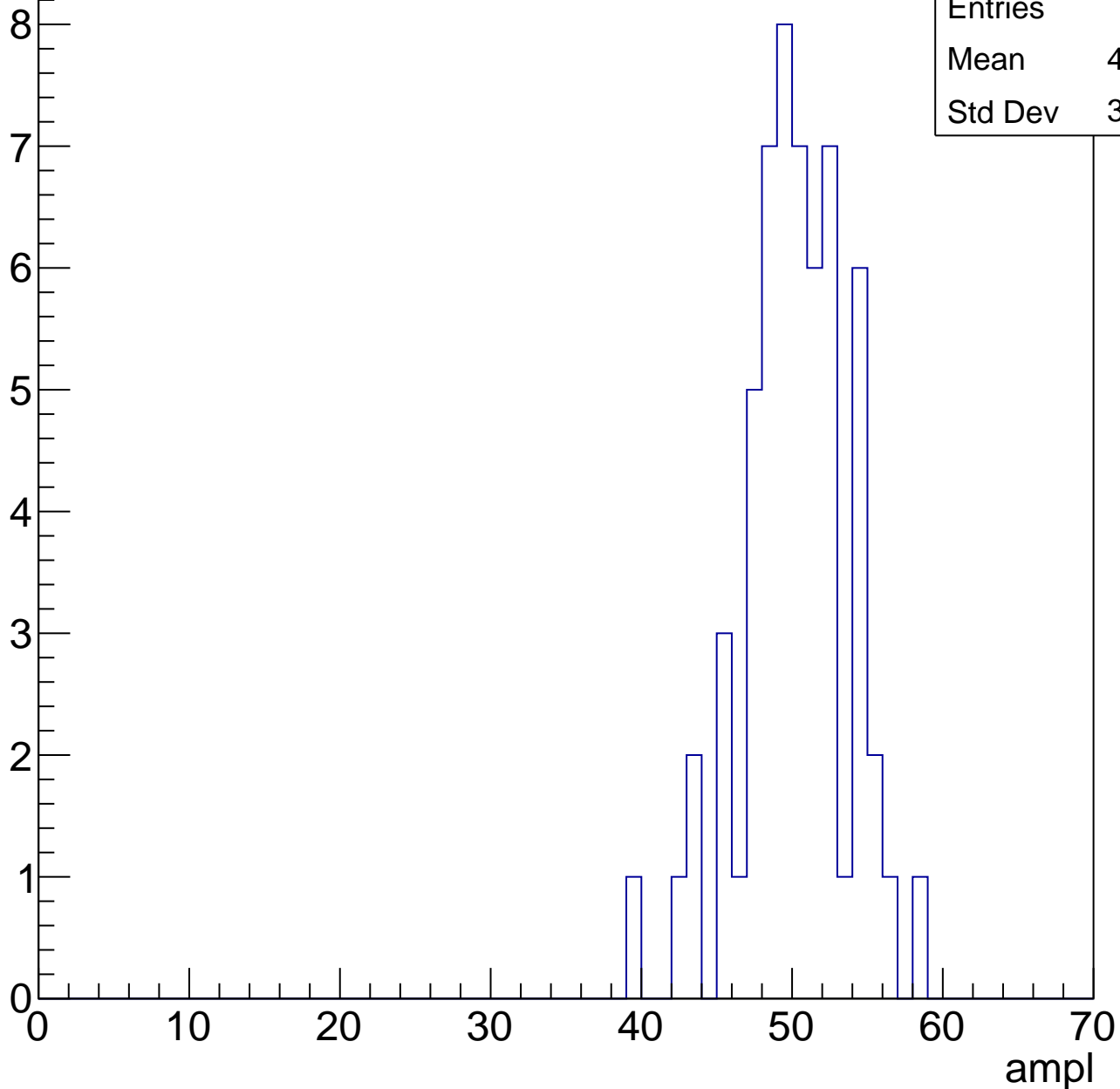


# B1L101S, U16-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

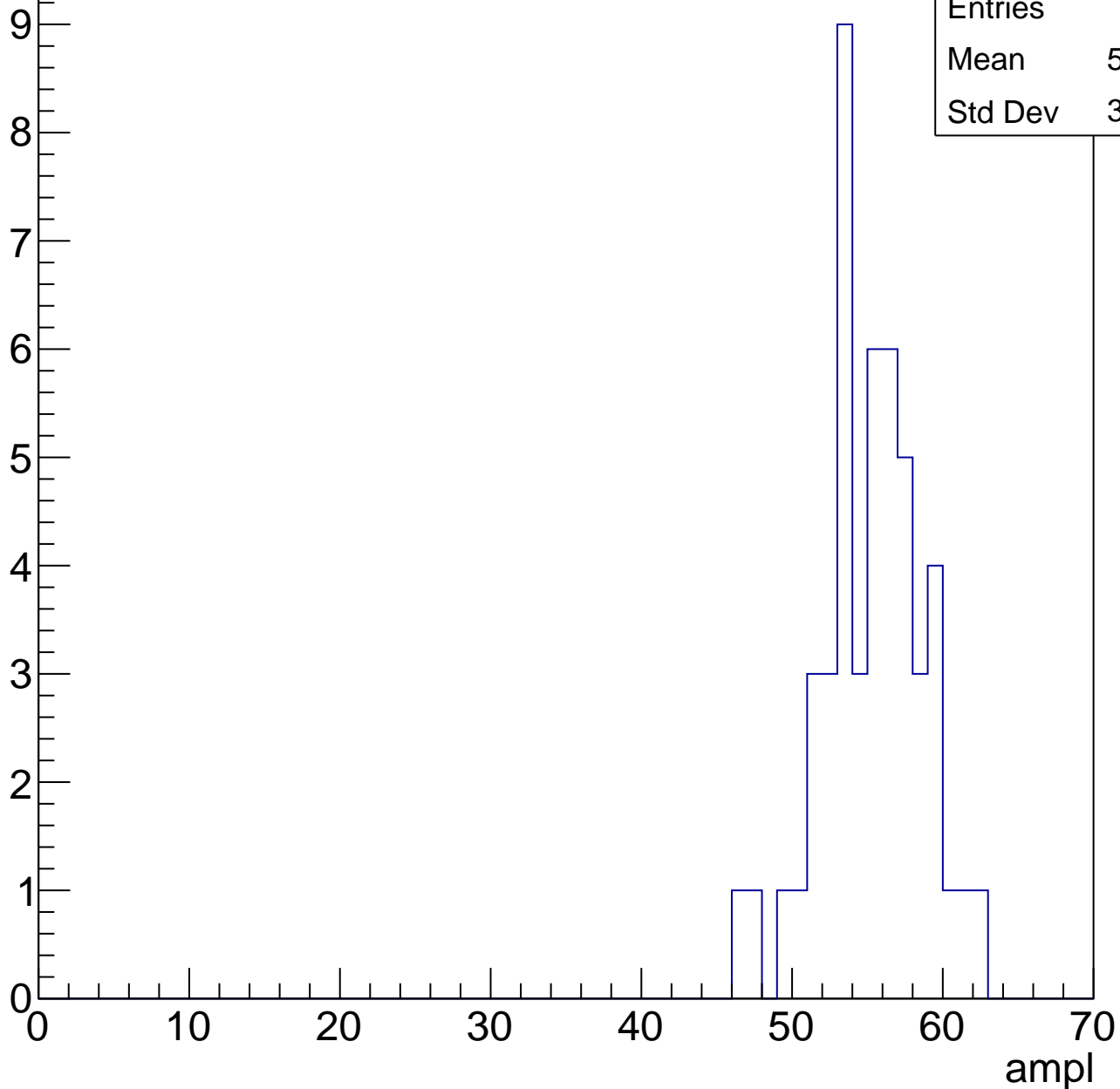
Entries	59
Mean	49.69
Std Dev	3.538



# B1L101S, U16-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch44, adc5

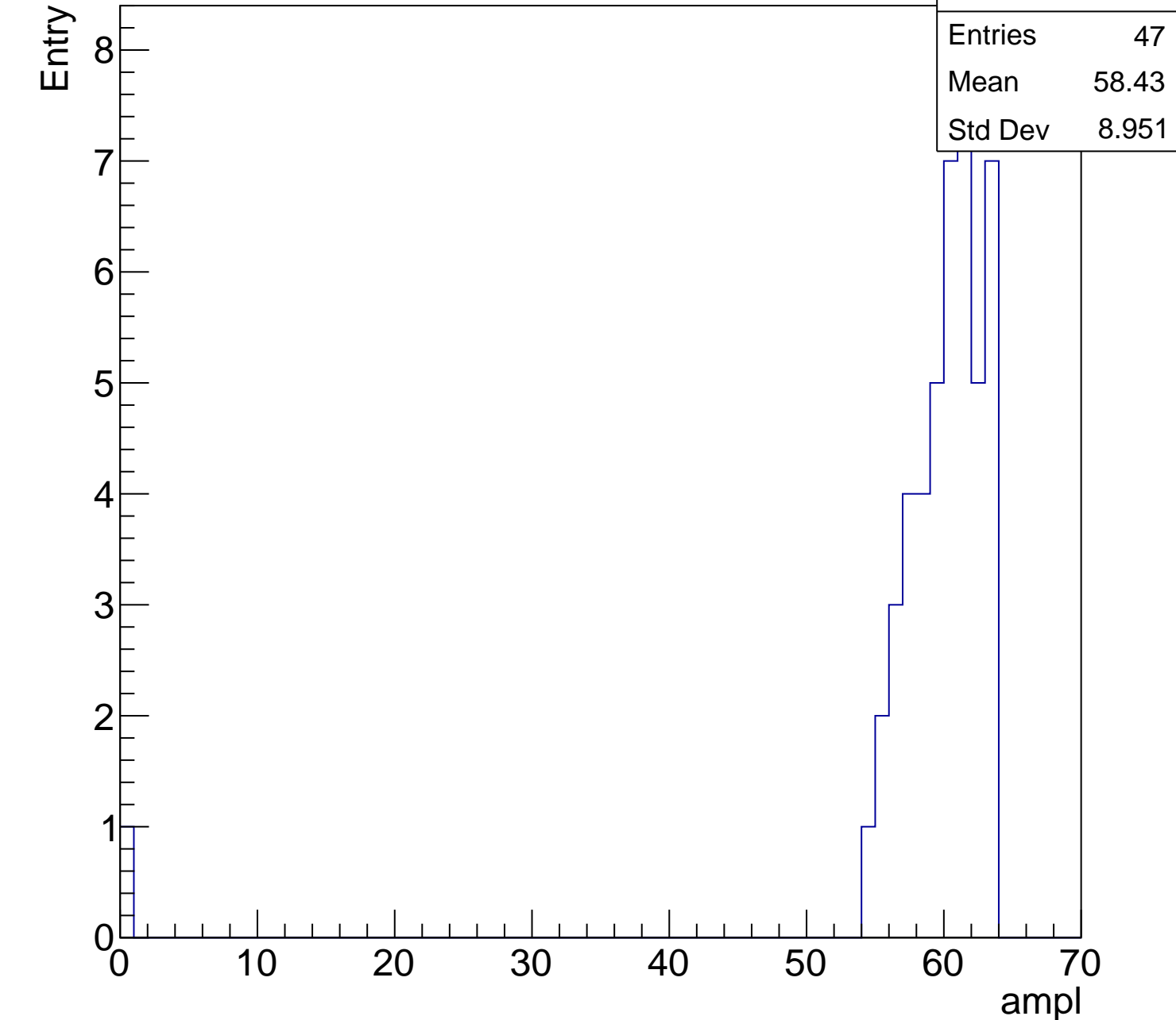
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	47
Mean	58.43
Std Dev	8.951

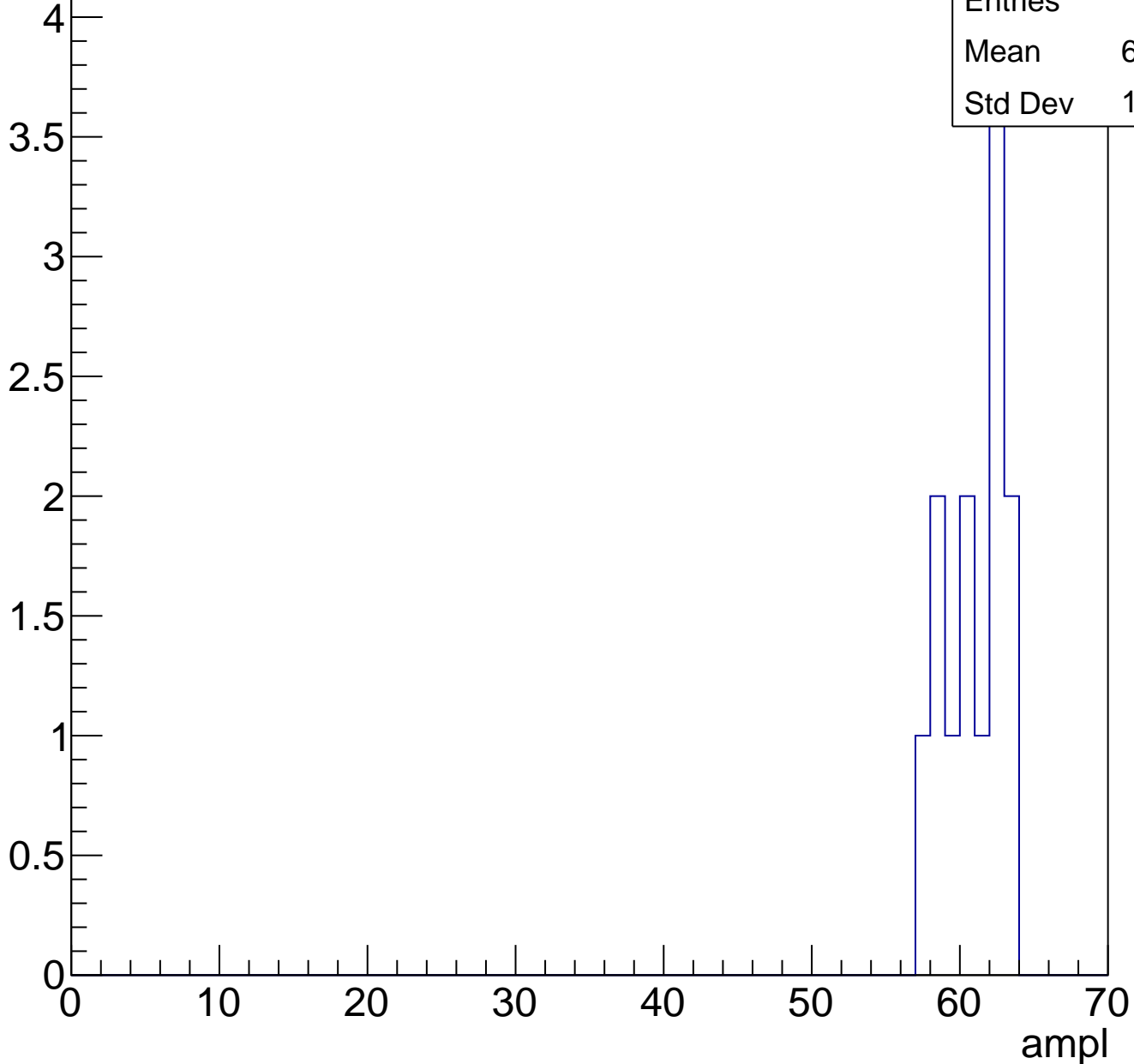
ampl



# B1L101S, U16-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	13
Mean	60.54
Std Dev	1.946



# B1L101S, U16-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch45, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	89
Mean	29.51
Std Dev	5.691

**Gaus mean : 30.3740**

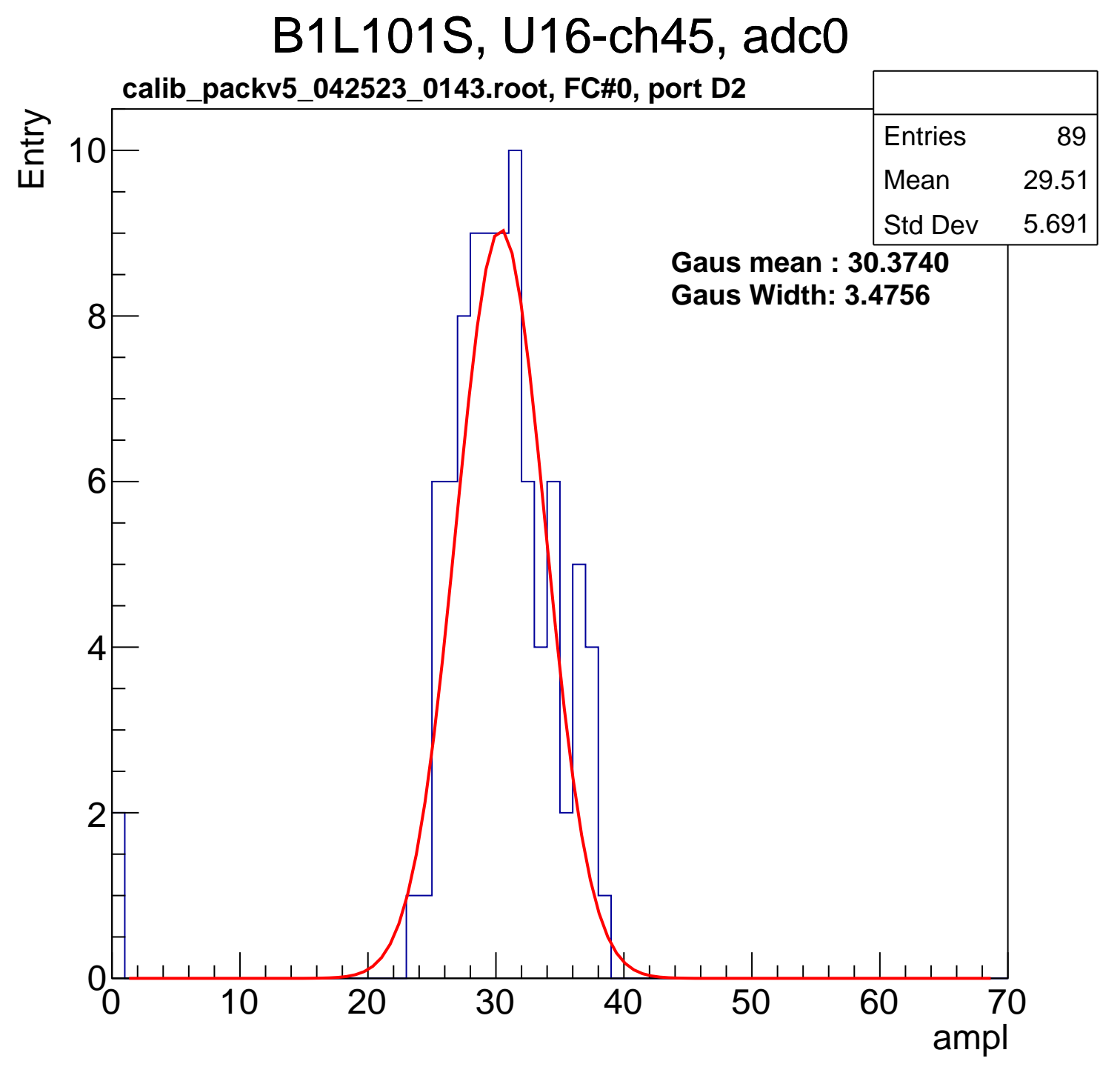
**Gaus Width: 3.4756**

Entry

10  
8  
6  
4  
2  
0

ampl

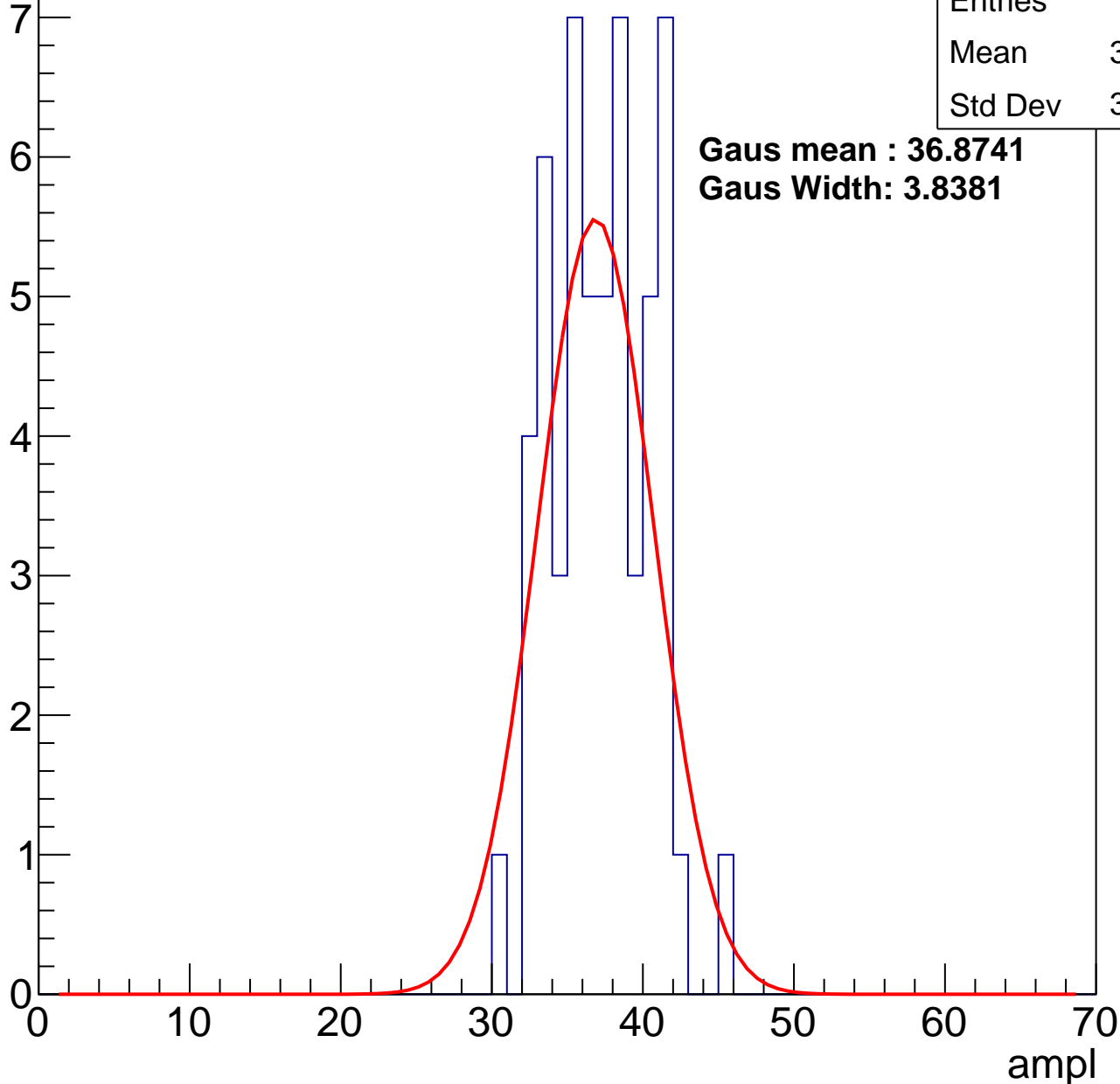
0 10 20 30 40 50 60 70



# B1L101S, U16-ch45, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch45, adc2

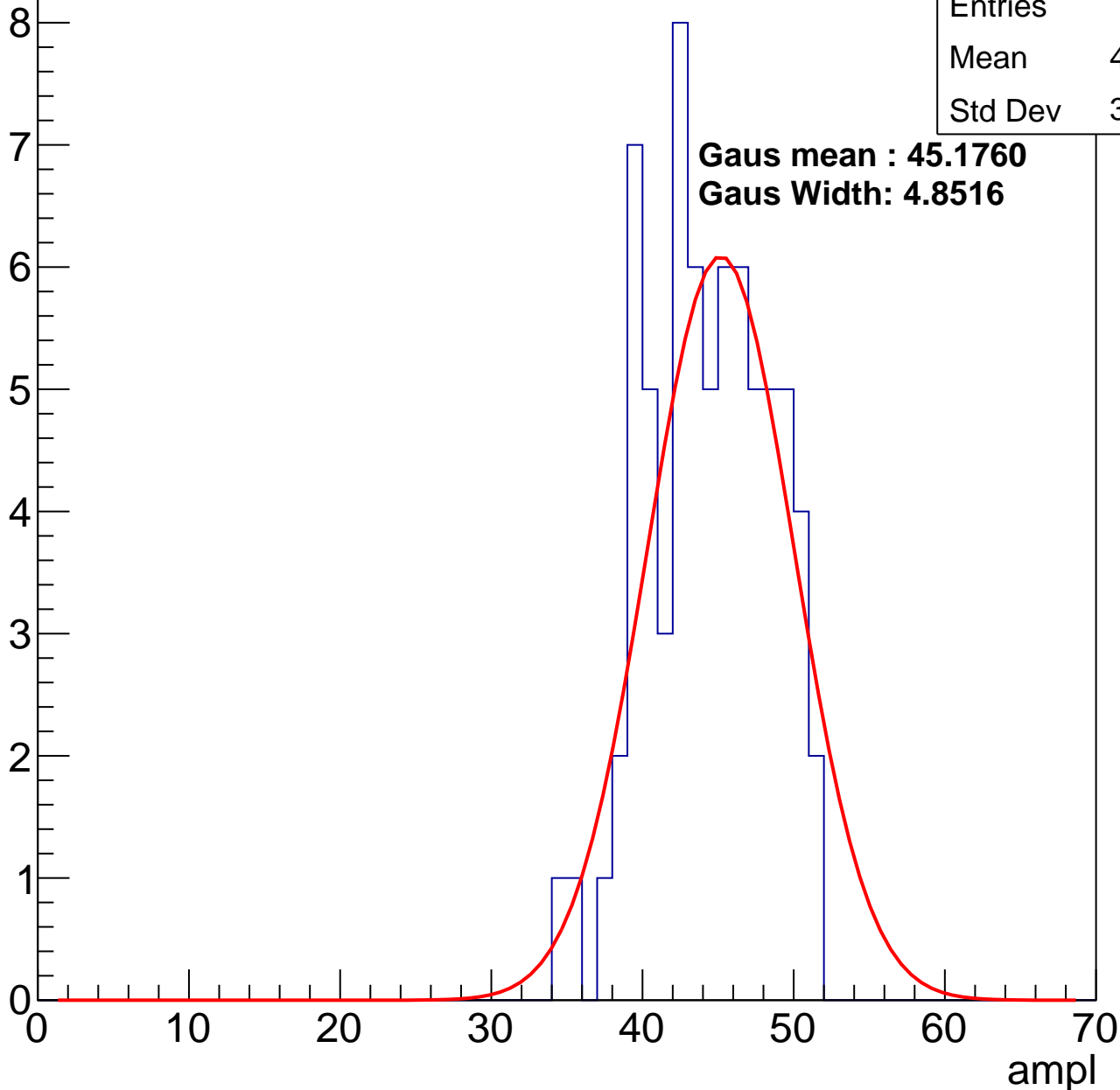
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	43.89
Std Dev	3.985

**Gaus mean : 45.1760**

**Gaus Width: 4.8516**

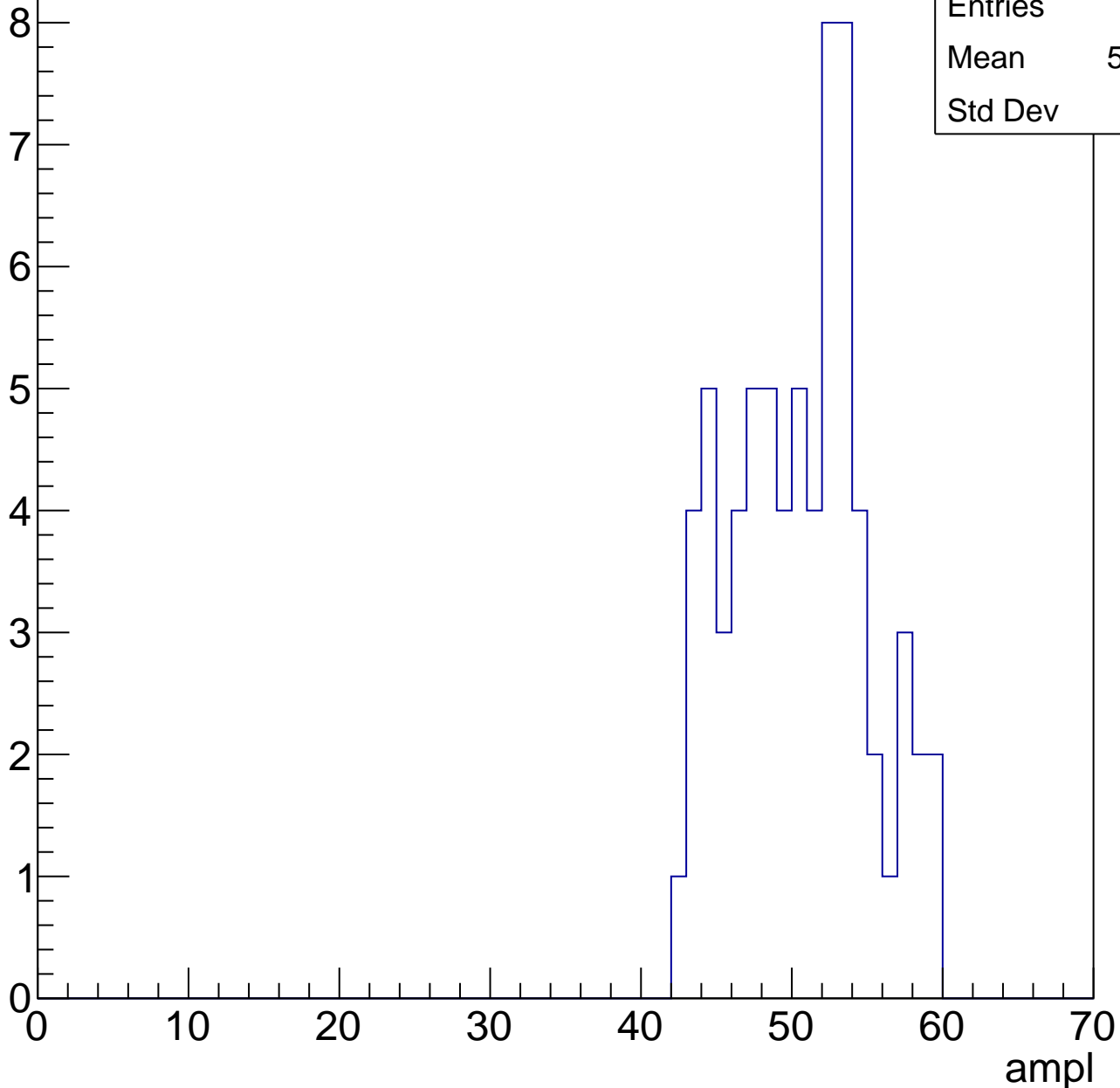


# B1L101S, U16-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

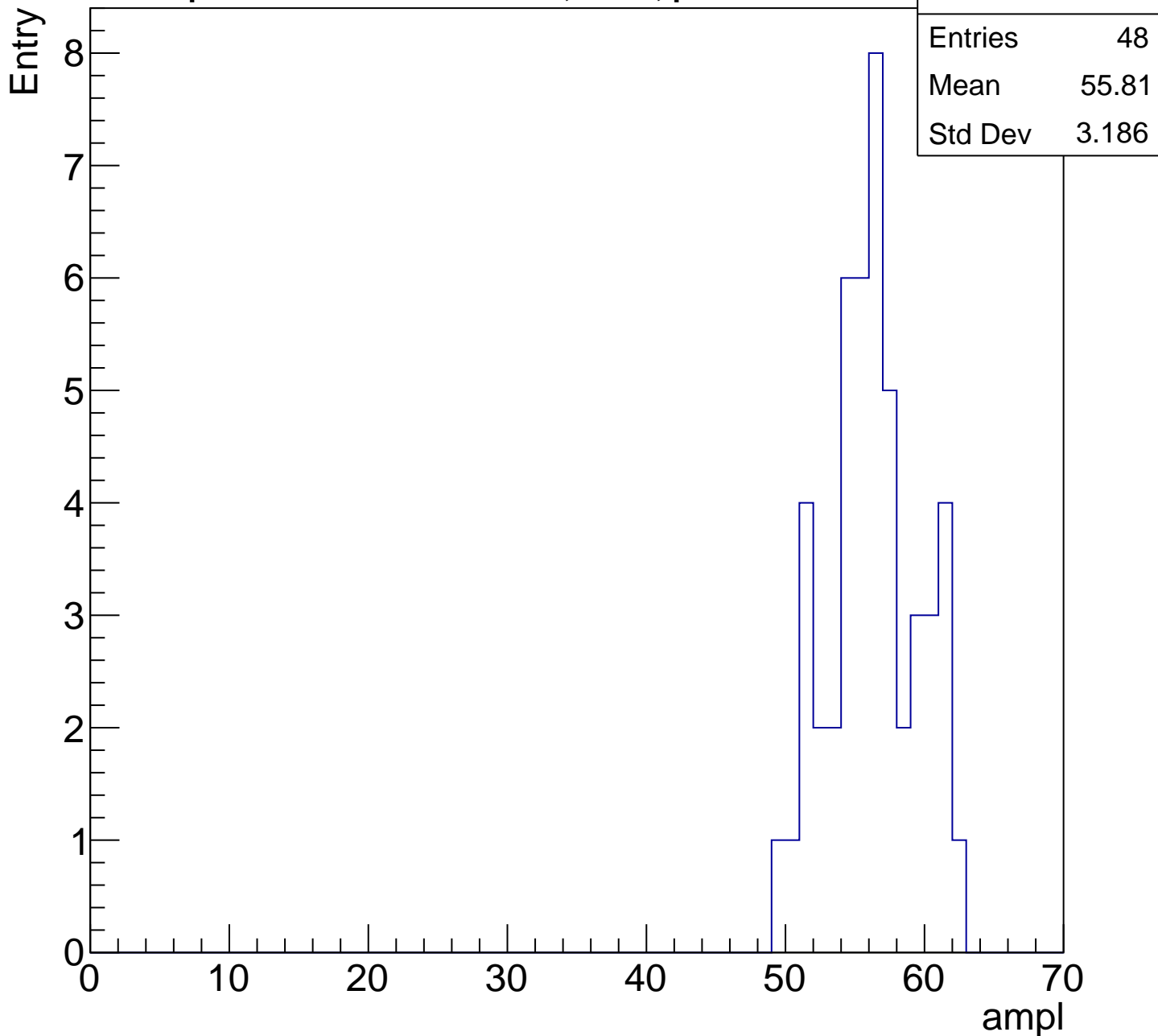
Entry

Entries	70
Mean	50.07
Std Dev	4.38



# B1L101S, U16-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

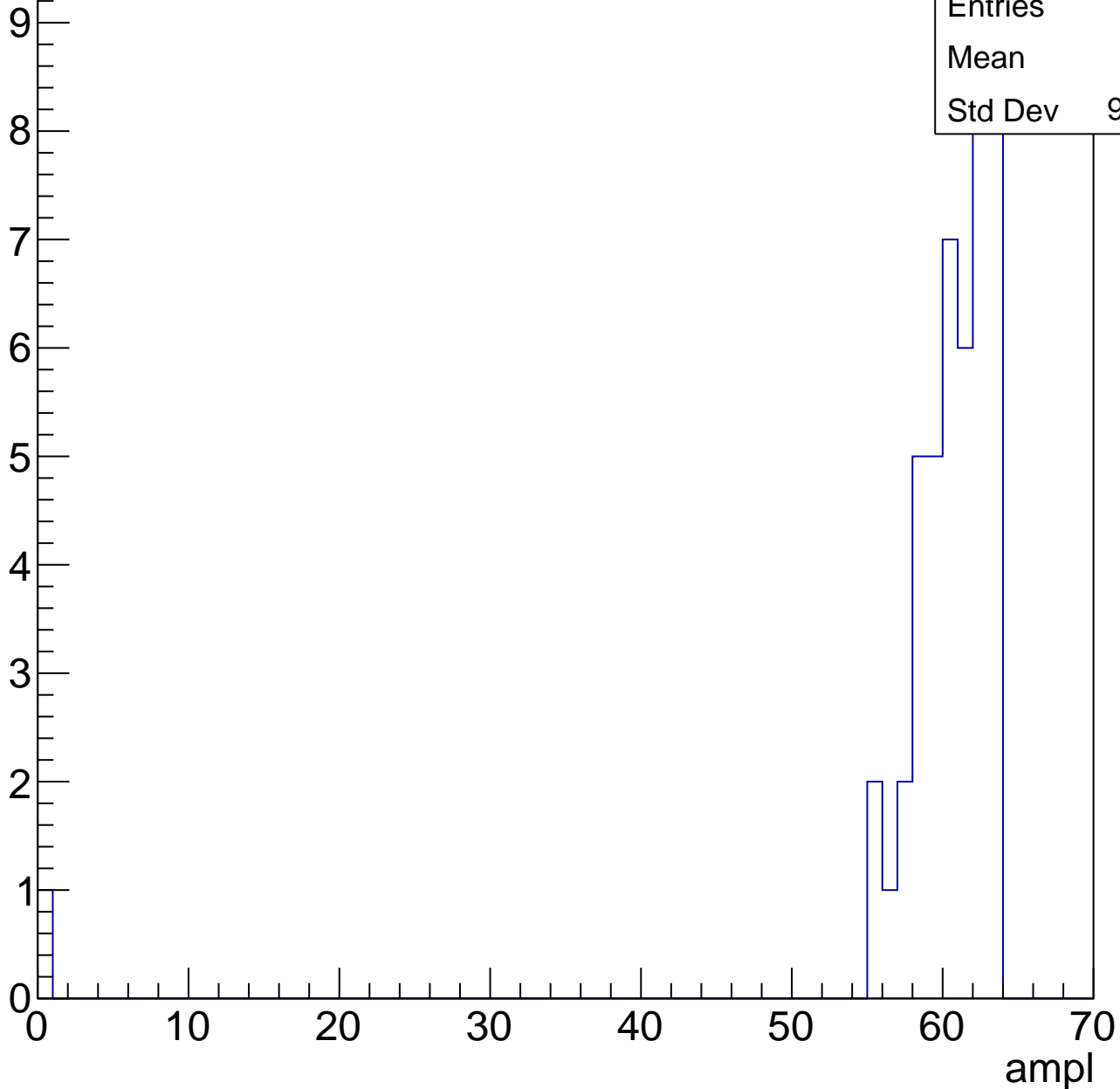


# B1L101S, U16-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

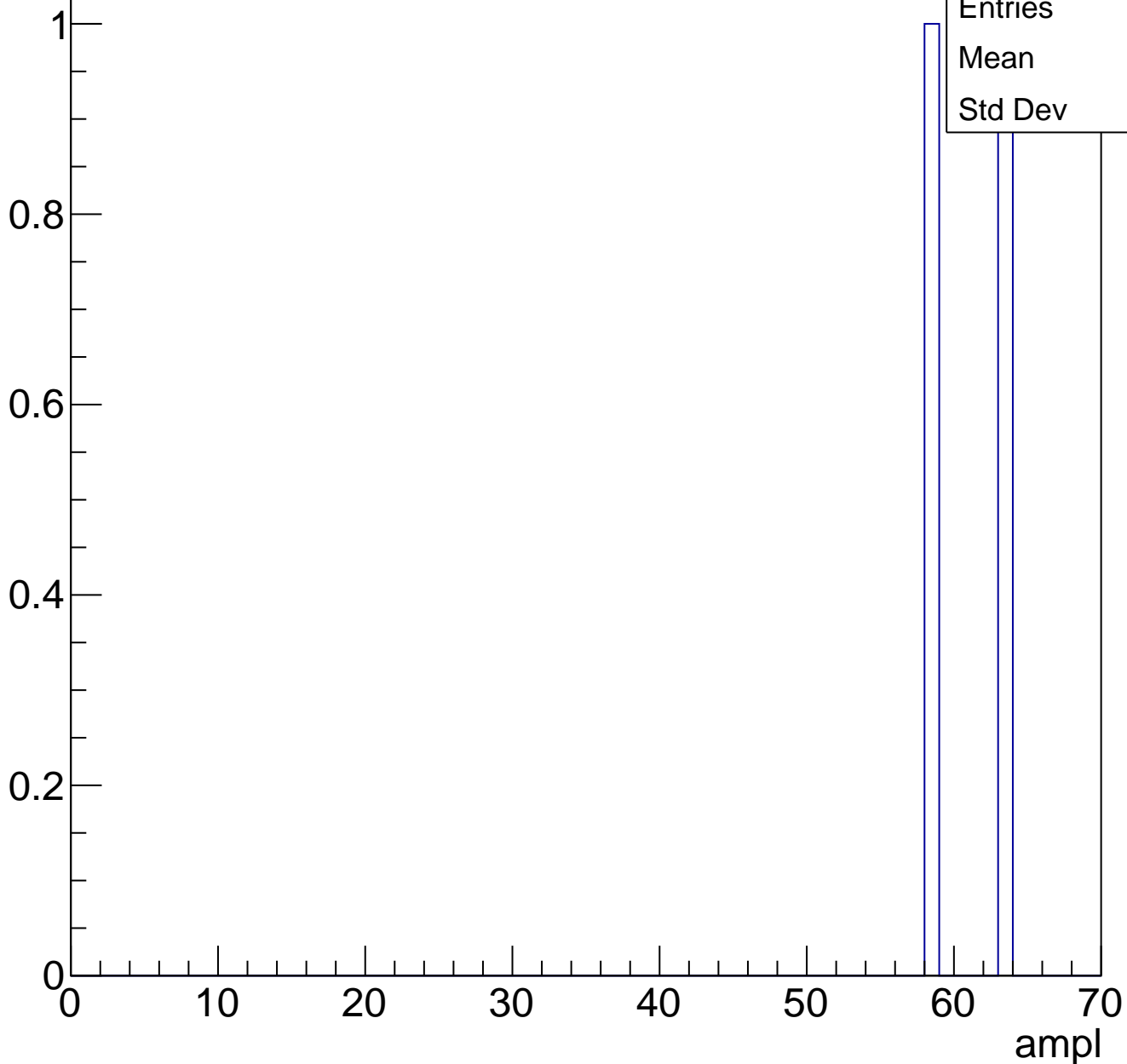
Entries	46
Mean	59
Std Dev	9.067



# B1L101S, U16-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch46, adc0

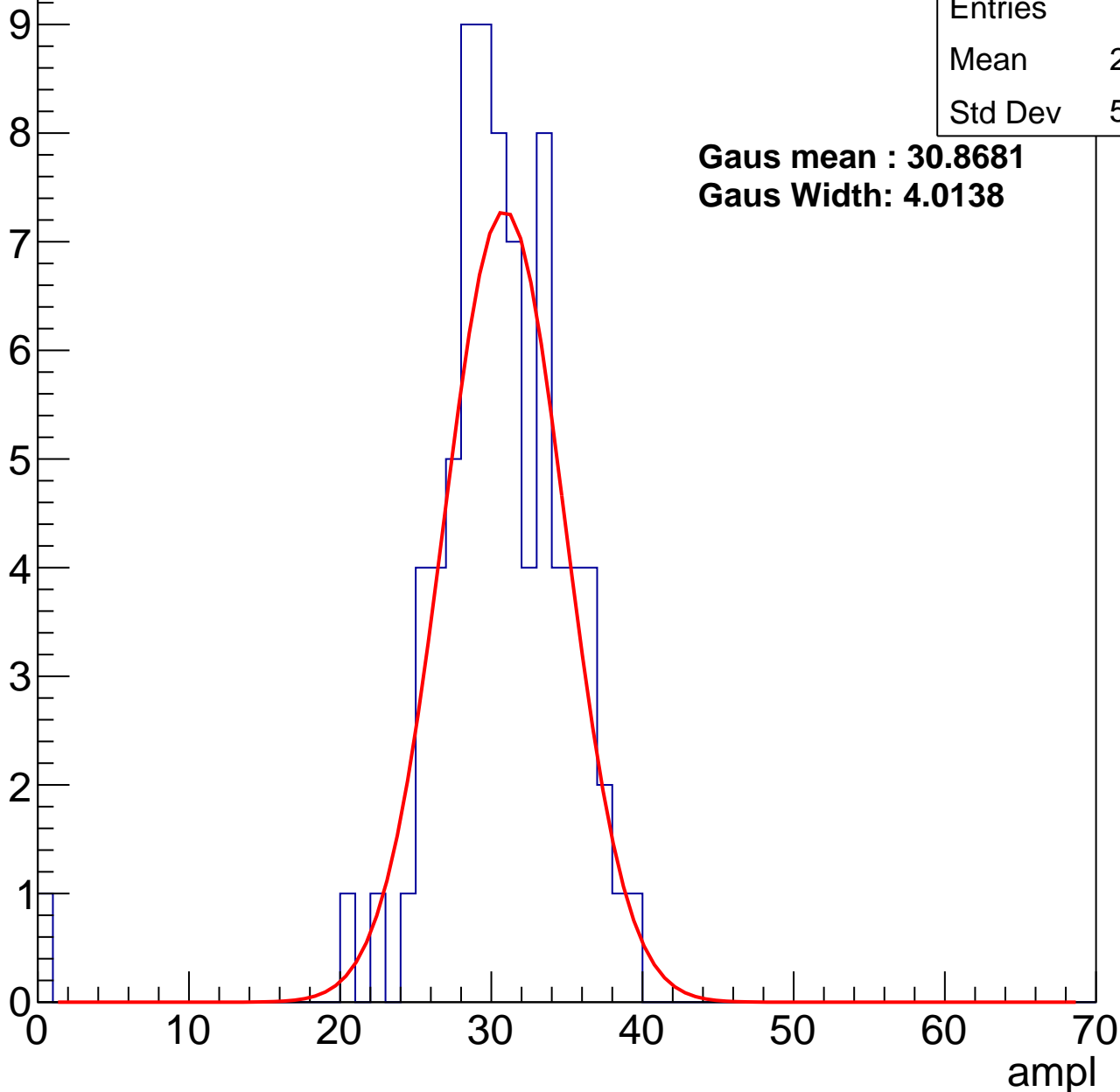
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	29.97
Std Dev	5.064

**Gaus mean : 30.8681**

**Gaus Width: 4.0138**



# B1L101S, U16-ch46, adc1

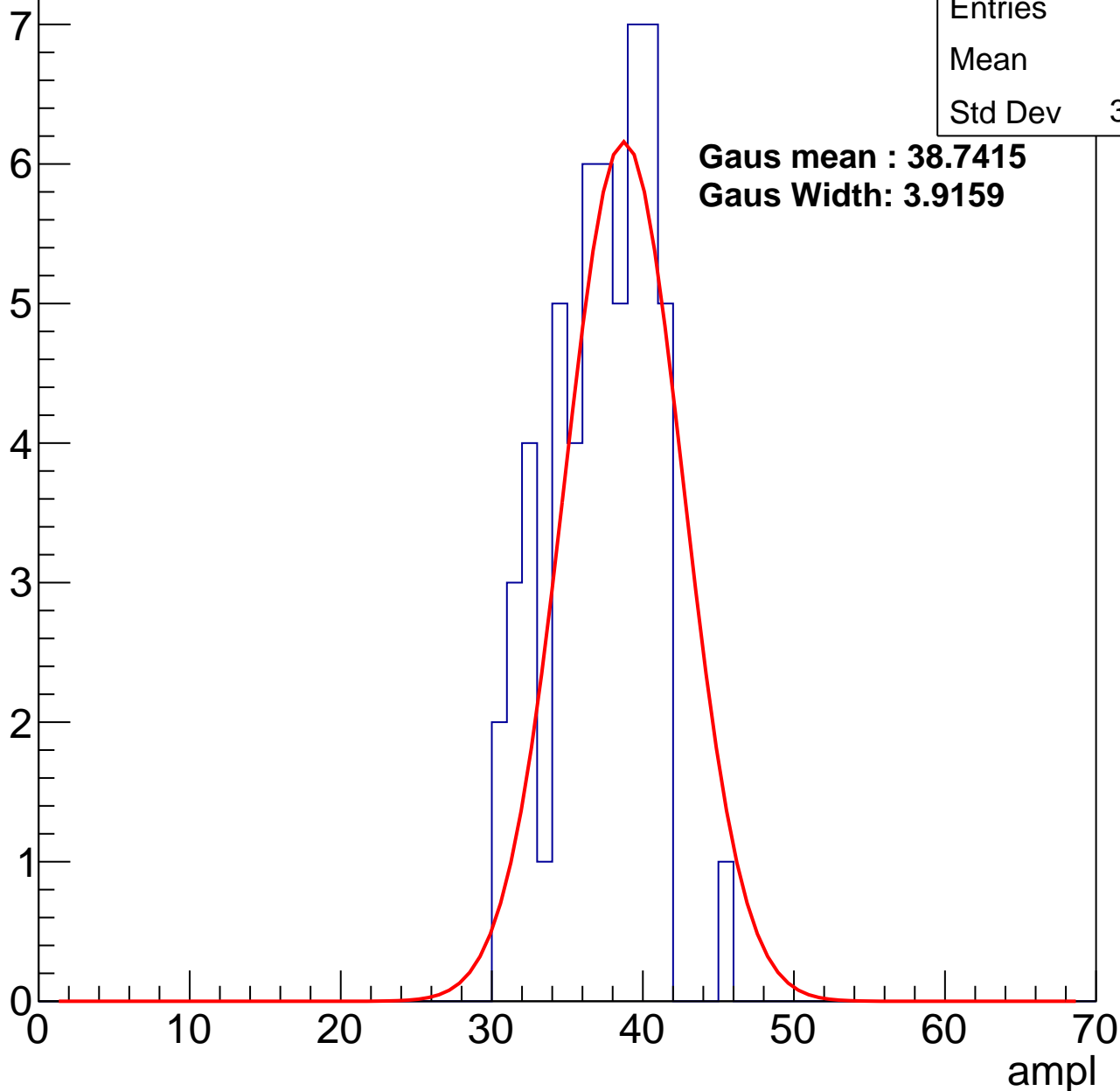
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	36.7
Std Dev	3.338

**Gaus mean : 38.7415**

**Gaus Width: 3.9159**



# B1L101S, U16-ch46, adc2

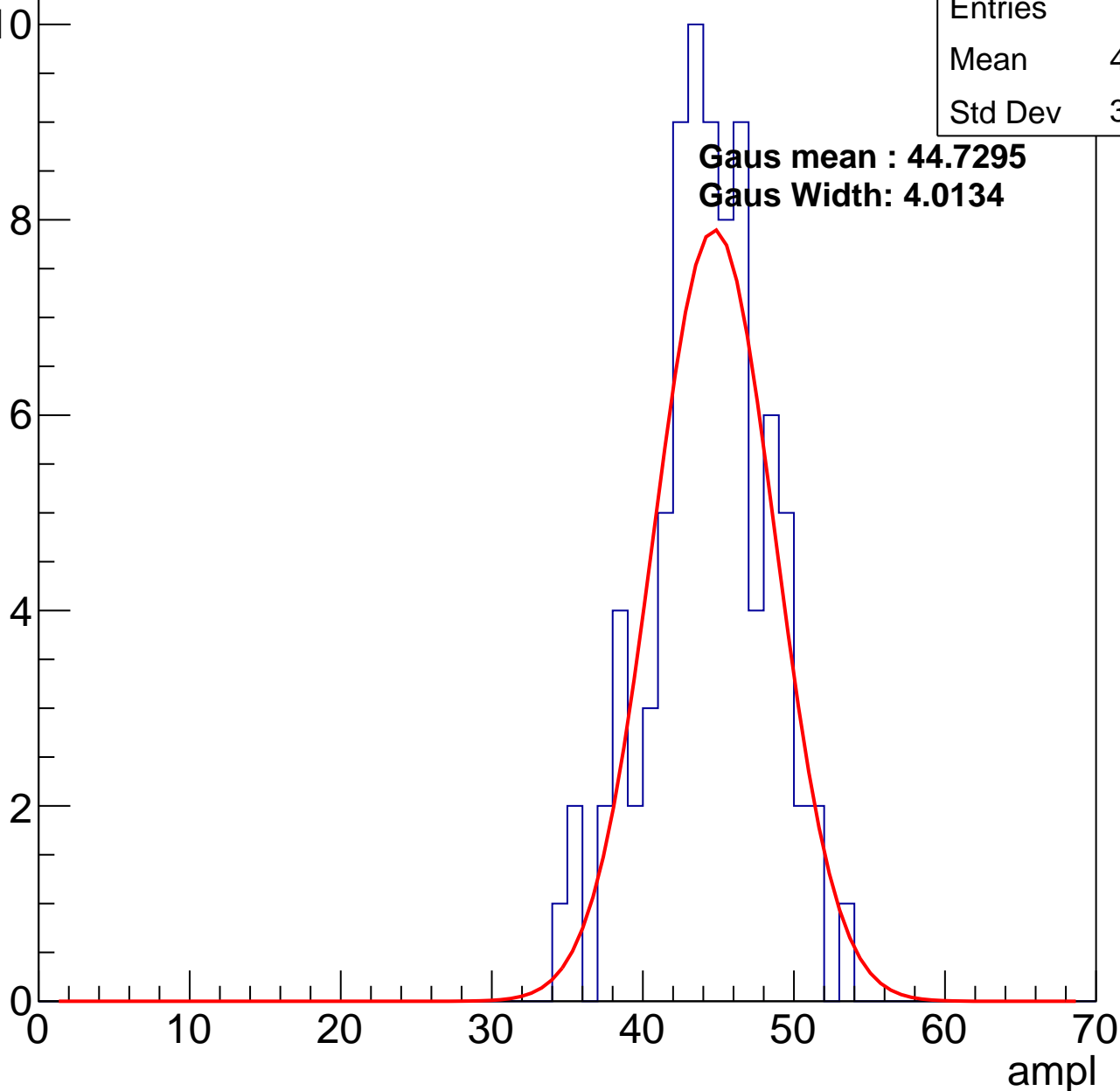
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	84
Mean	43.89
Std Dev	3.848

**Gaus mean : 44.7295**

**Gaus Width: 4.0134**

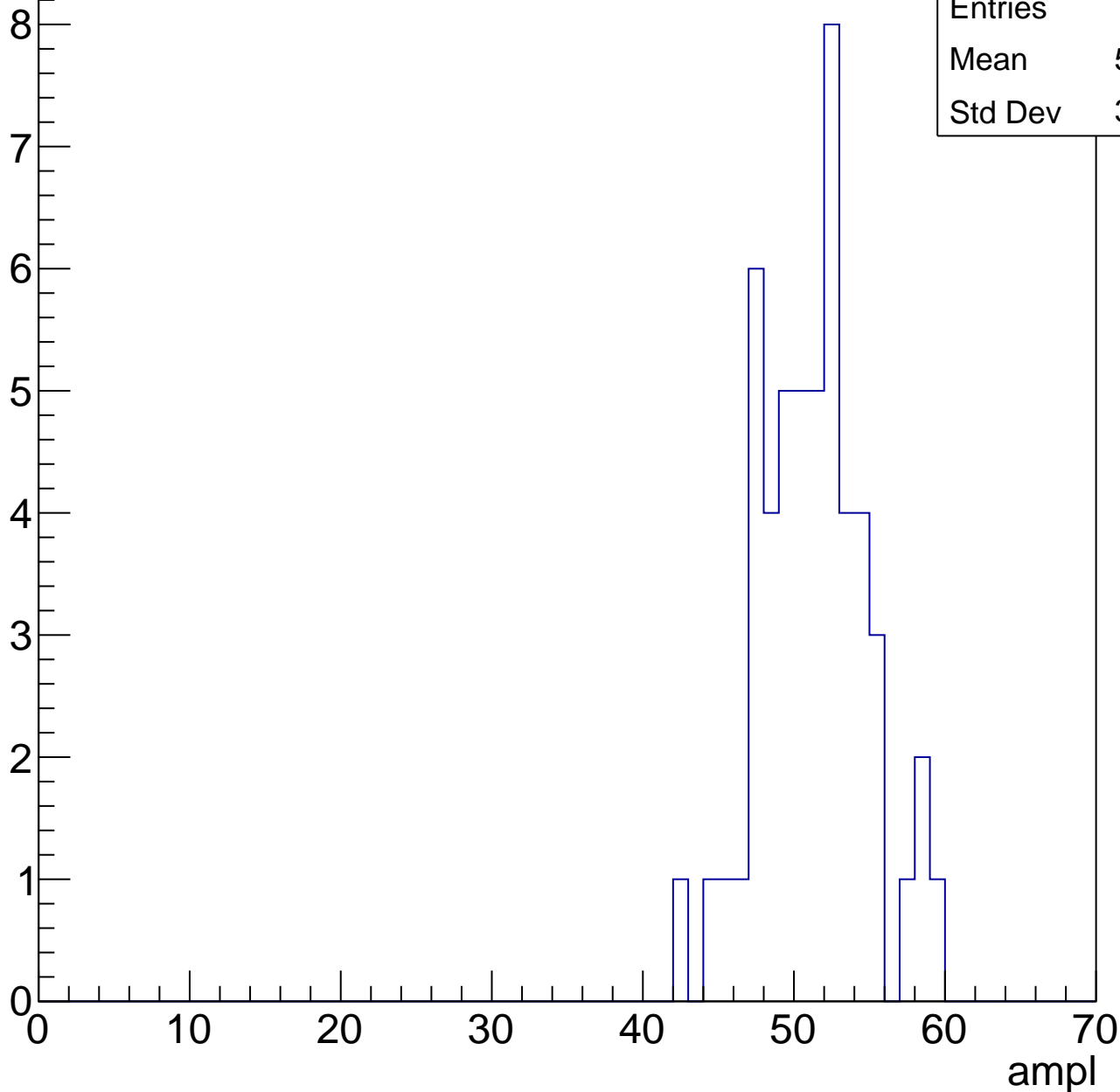


# B1L101S, U16-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

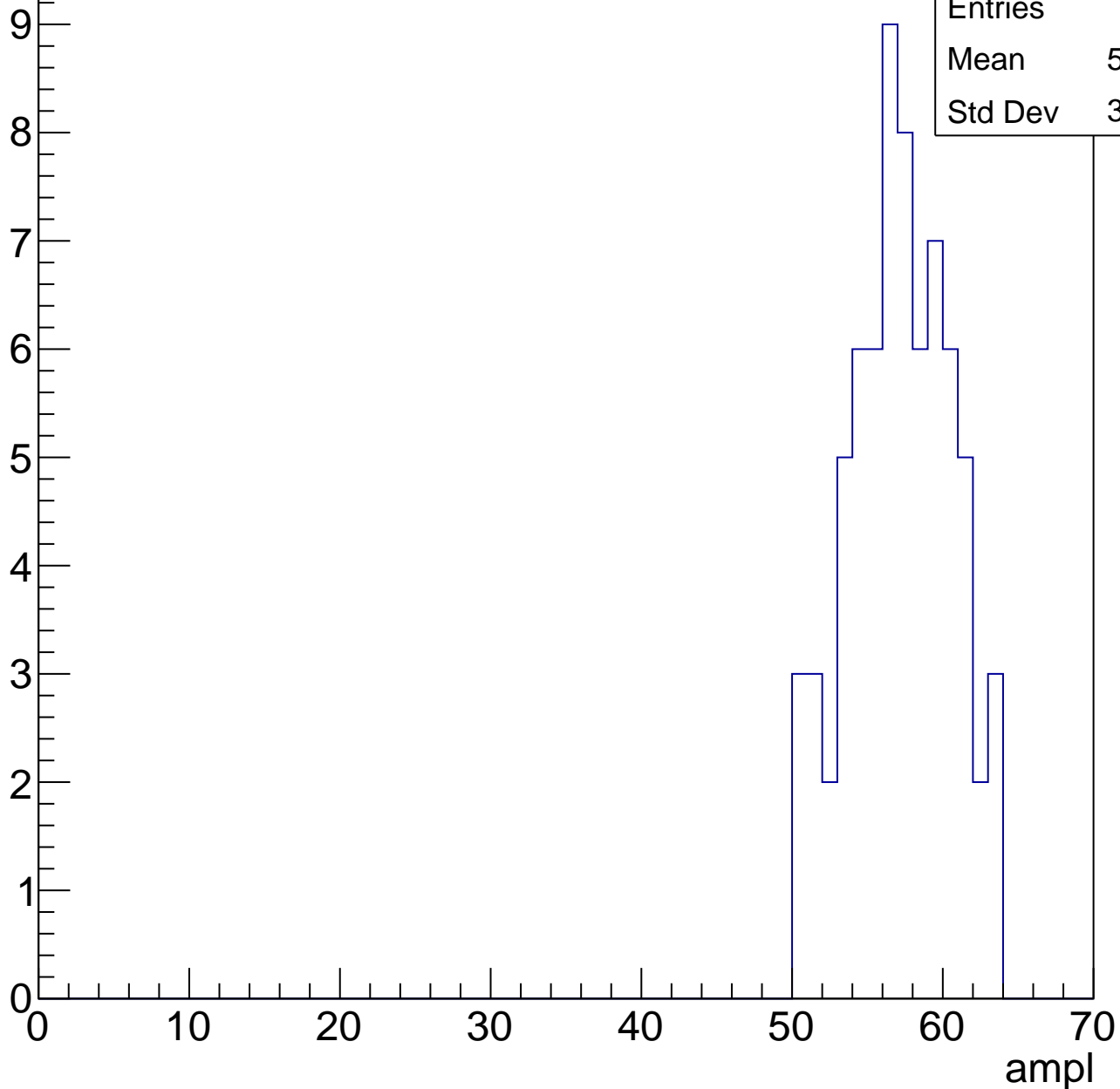
Entries	52
Mean	50.81
Std Dev	3.541



# B1L101S, U16-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

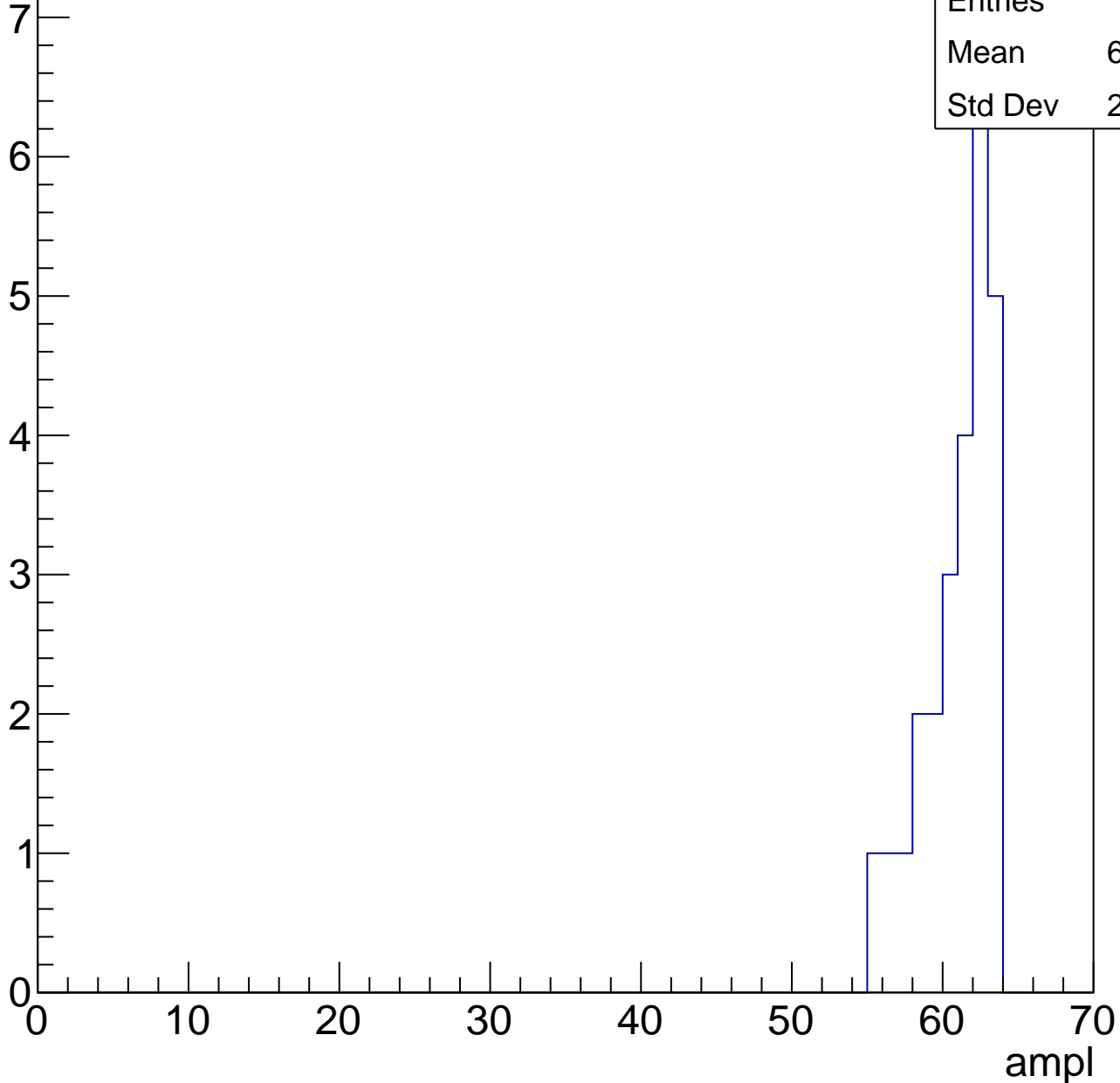


# B1L101S, U16-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

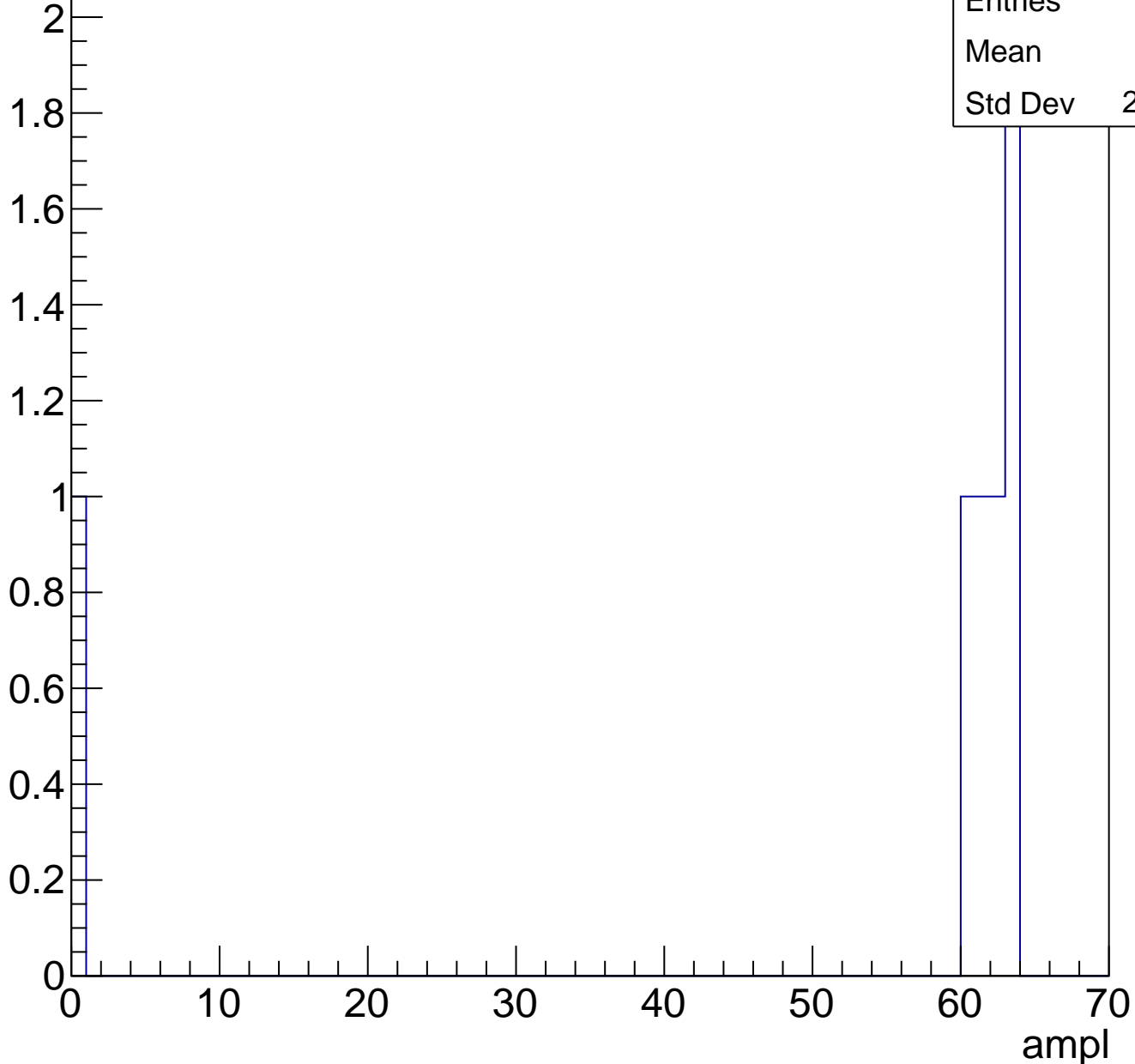
Entries	26
Mean	60.58
Std Dev	2.222



# B1L101S, U16-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U16-ch47, adc0

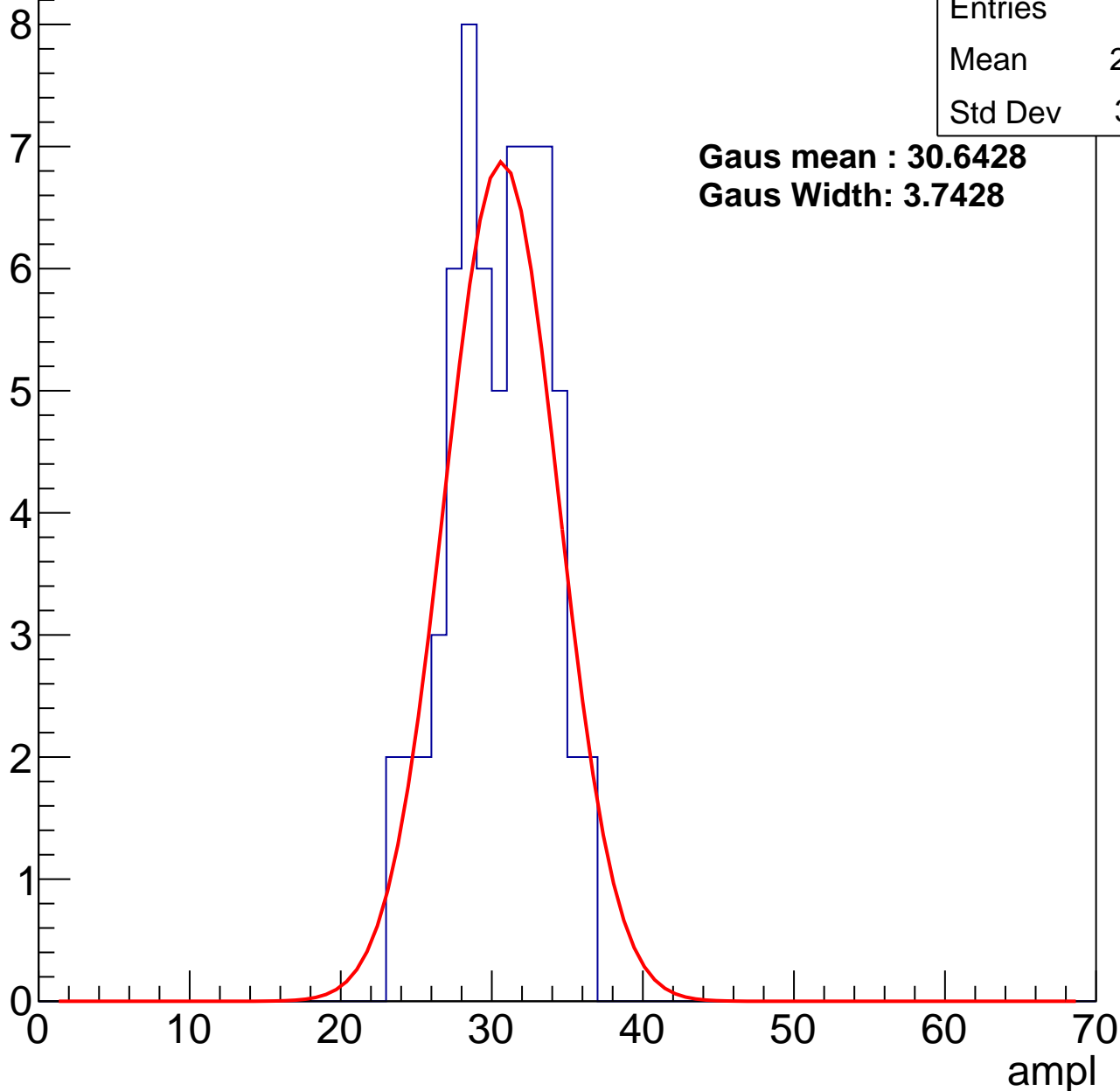
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	29.94
Std Dev	3.211

**Gaus mean : 30.6428**

**Gaus Width: 3.7428**



# B1L101S, U16-ch47, adc1

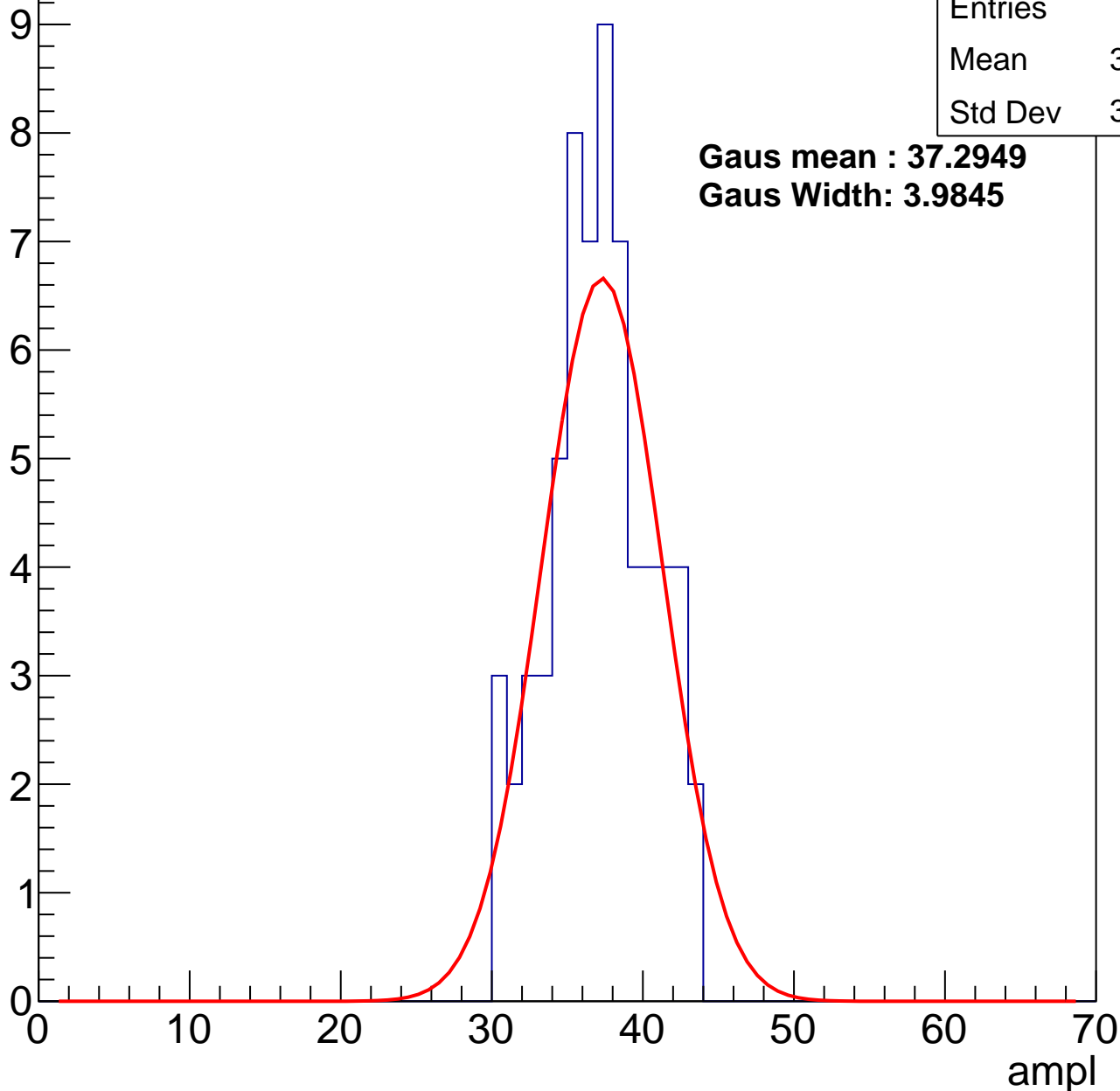
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	36.65
Std Dev	3.312

**Gaus mean : 37.2949**

**Gaus Width: 3.9845**



# B1L101S, U16-ch47, adc2

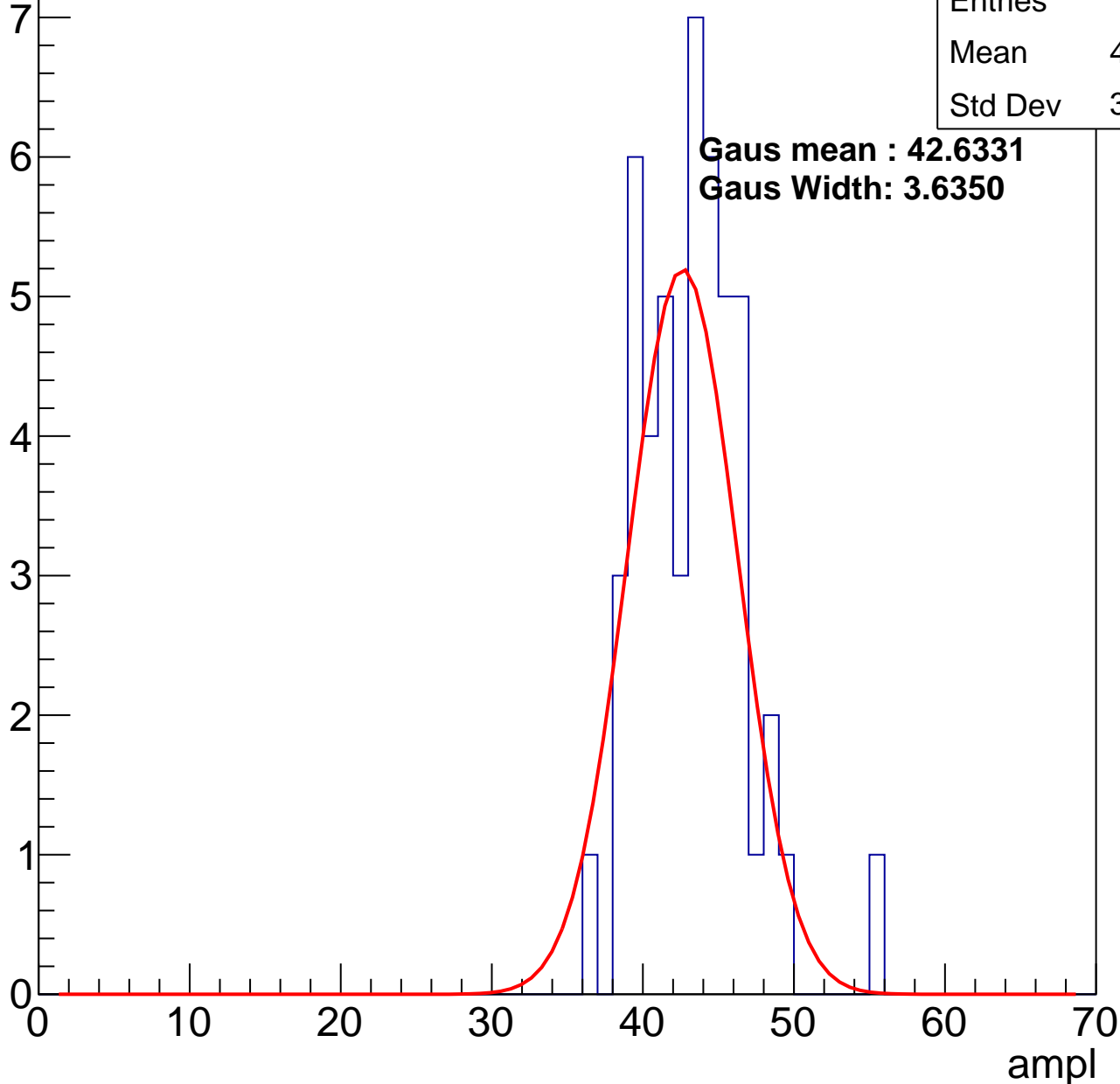
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	42.84
Std Dev	3.449

**Gaus mean : 42.6331**

**Gaus Width: 3.6350**



# B1L101S, U16-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	77
Mean	48.38
Std Dev	3.861

Entry

10

8

6

4

2

0

0

10

20

30

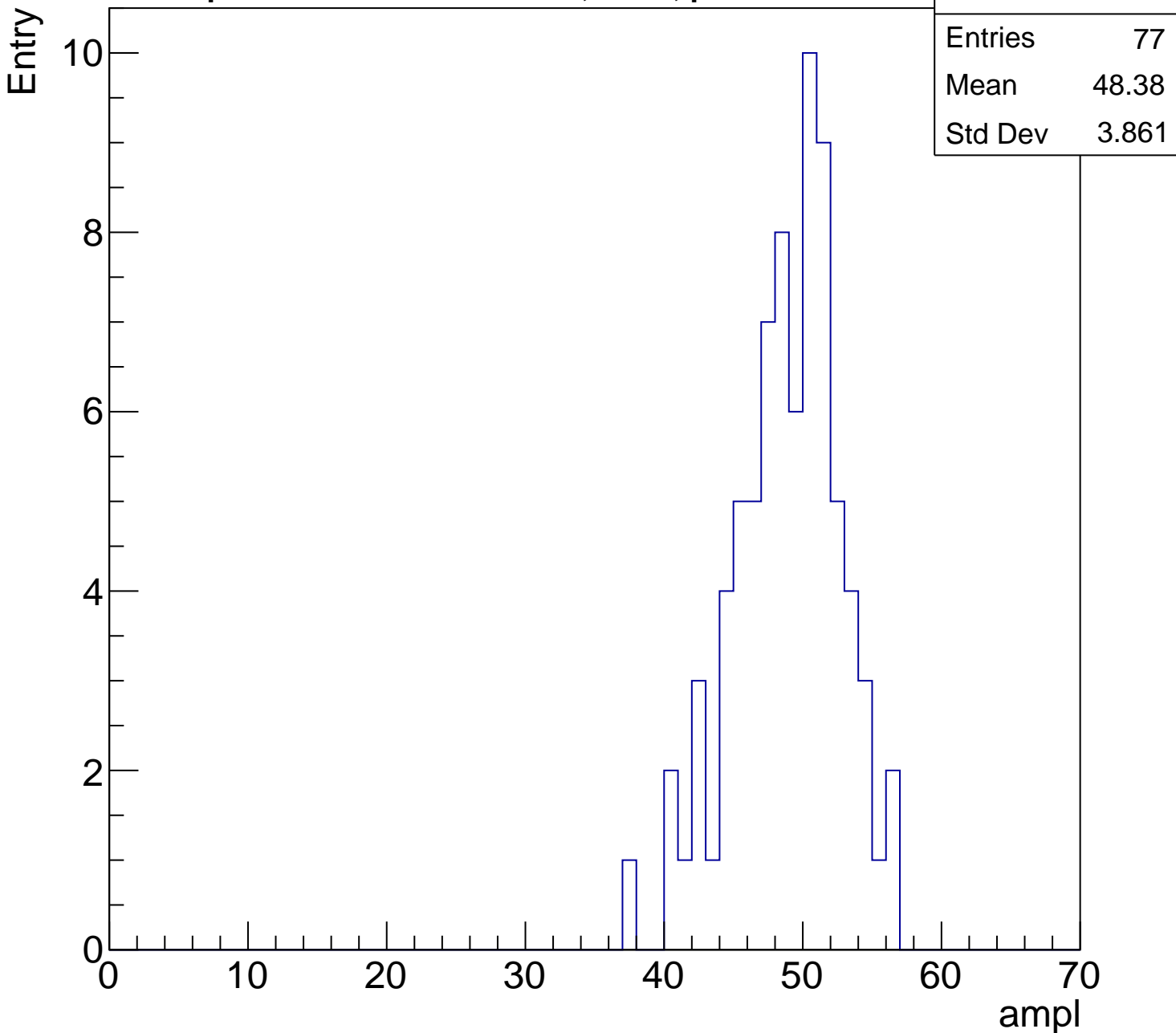
40

50

60

70

ampl

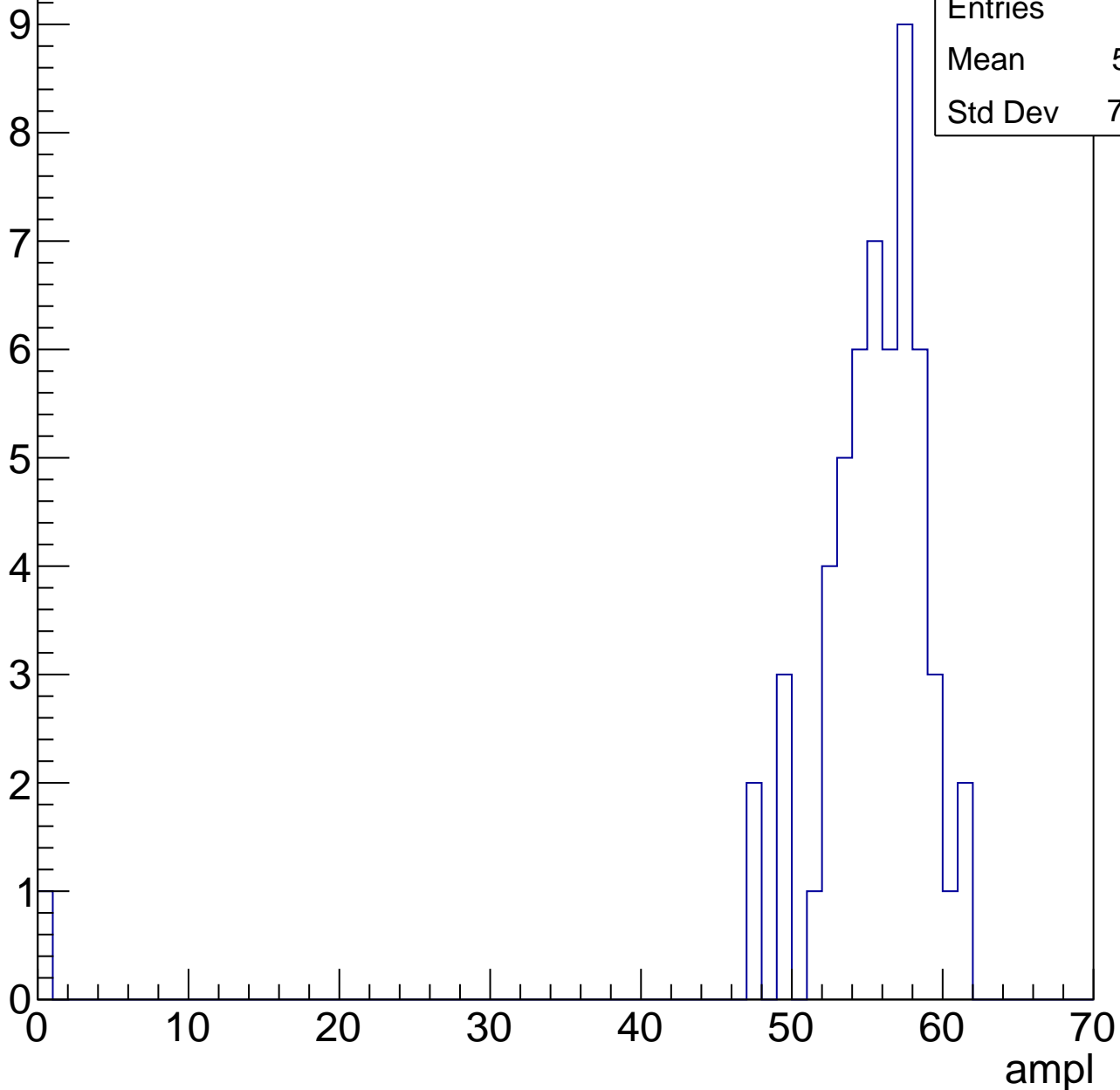


# B1L101S, U16-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

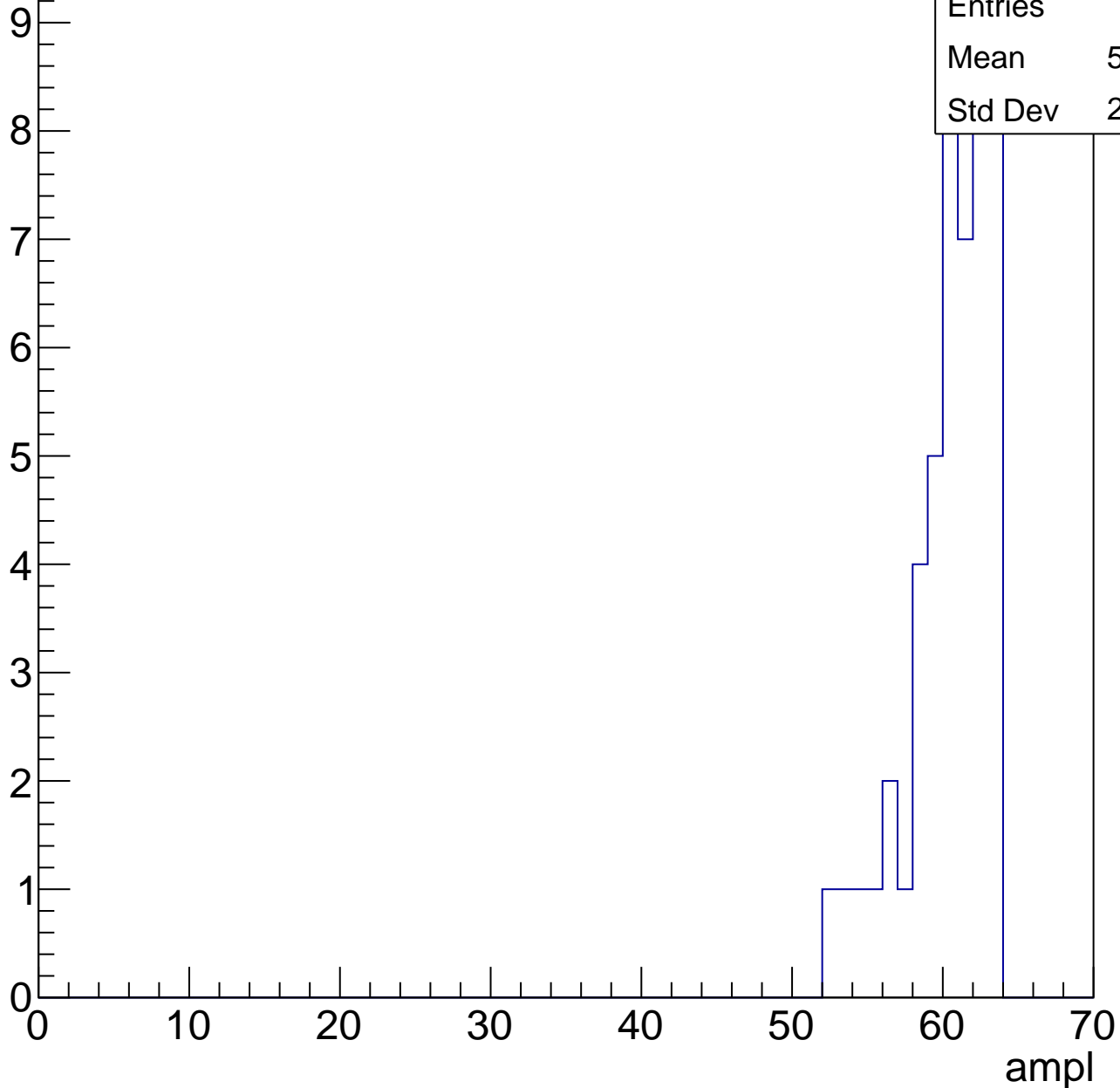
Entries	56
Mean	54.11
Std Dev	7.946



# B1L101S, U16-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	48
Mean	59.98
Std Dev	2.704

# B1L101S, U16-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

0

10

20

30

40

50

60

70

ampl

Entries	7
Mean	61
Std Dev	1.604



# B1L101S, U16-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U16-ch48, adc0

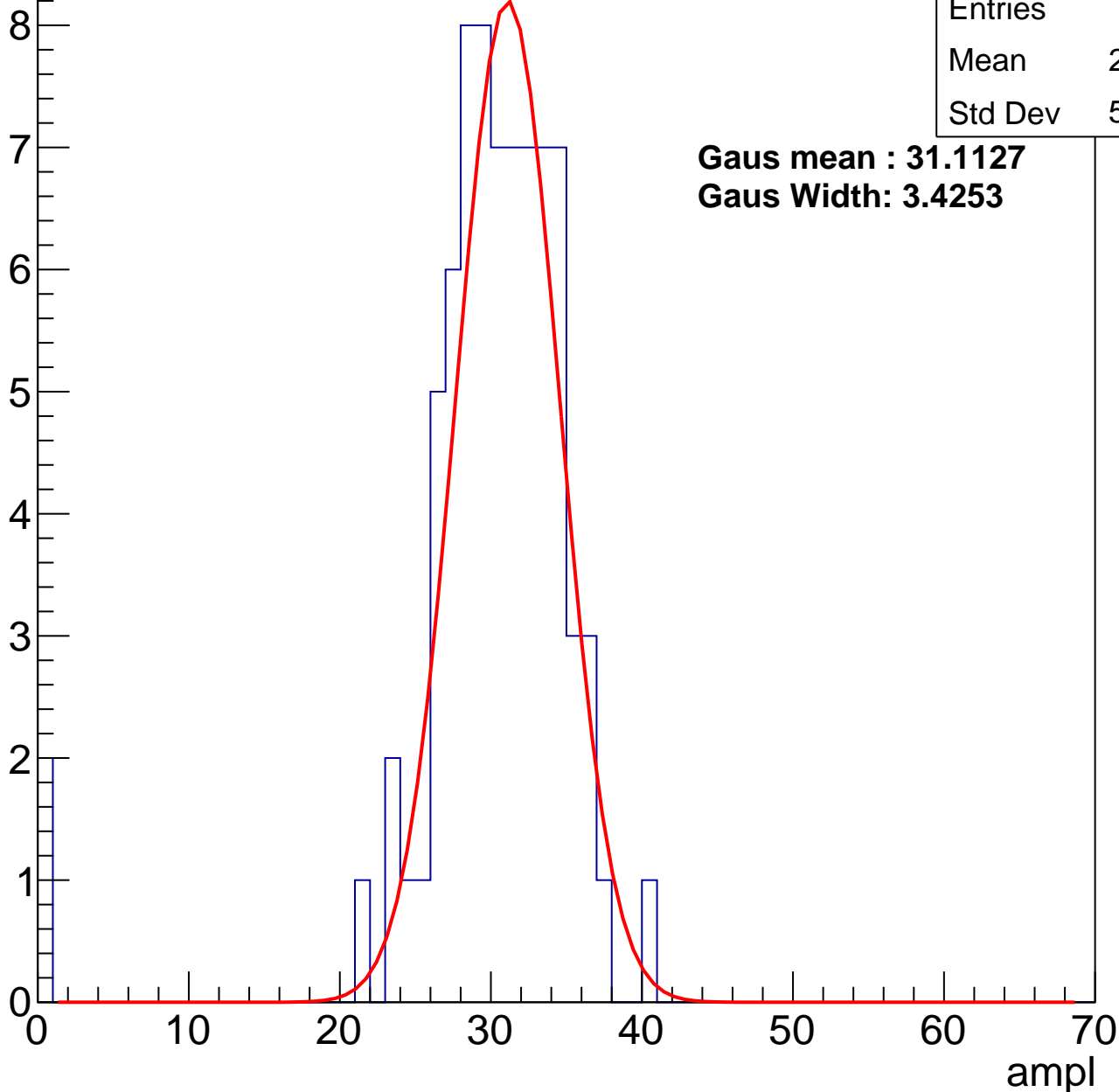
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	29.53
Std Dev	5.964

**Gaus mean : 31.1127**

**Gaus Width: 3.4253**



# B1L101S, U16-ch48, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	81
Mean	37.94
Std Dev	3.68

**Gaus mean : 38.8002**

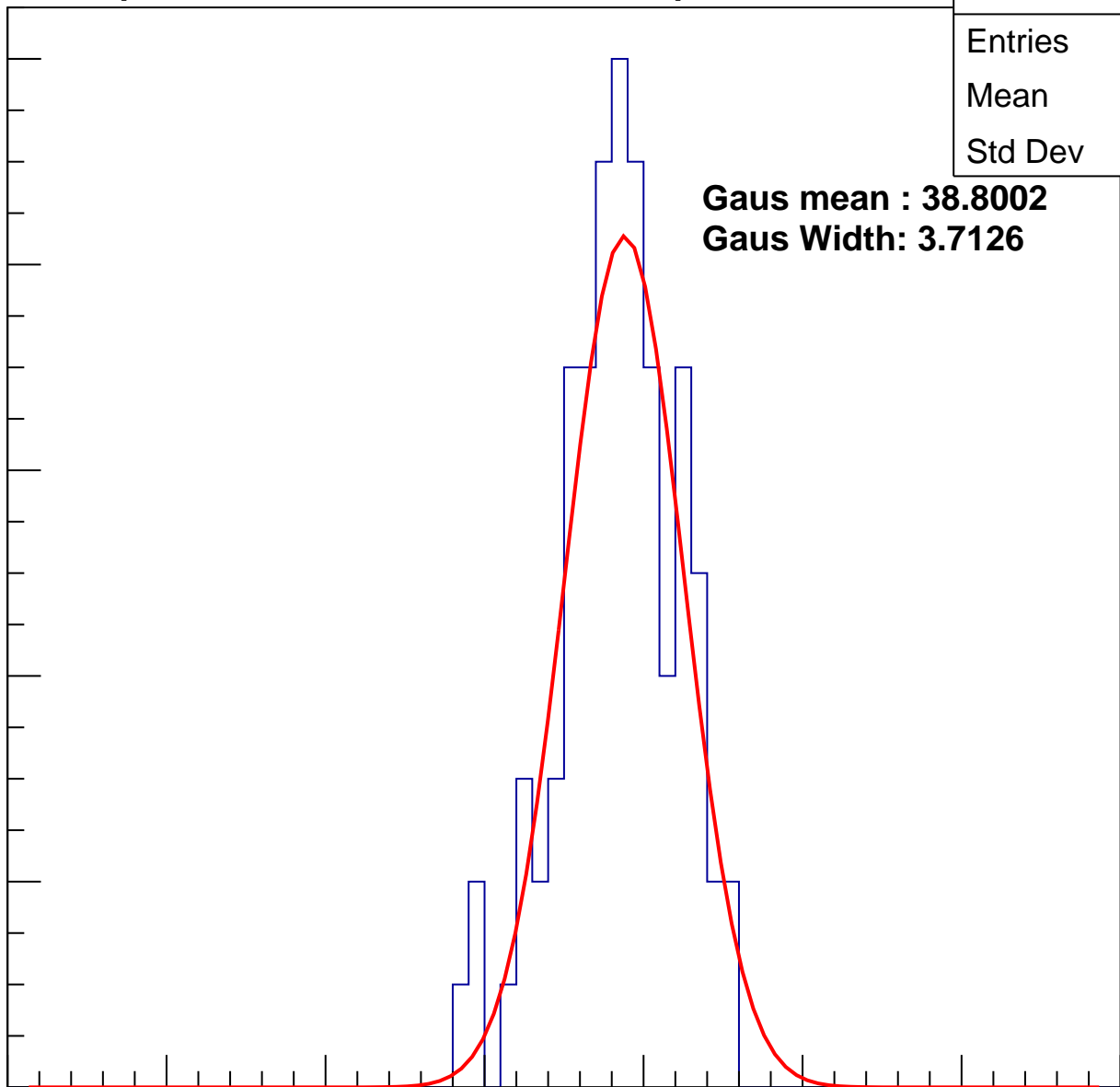
**Gaus Width: 3.7126**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch48, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

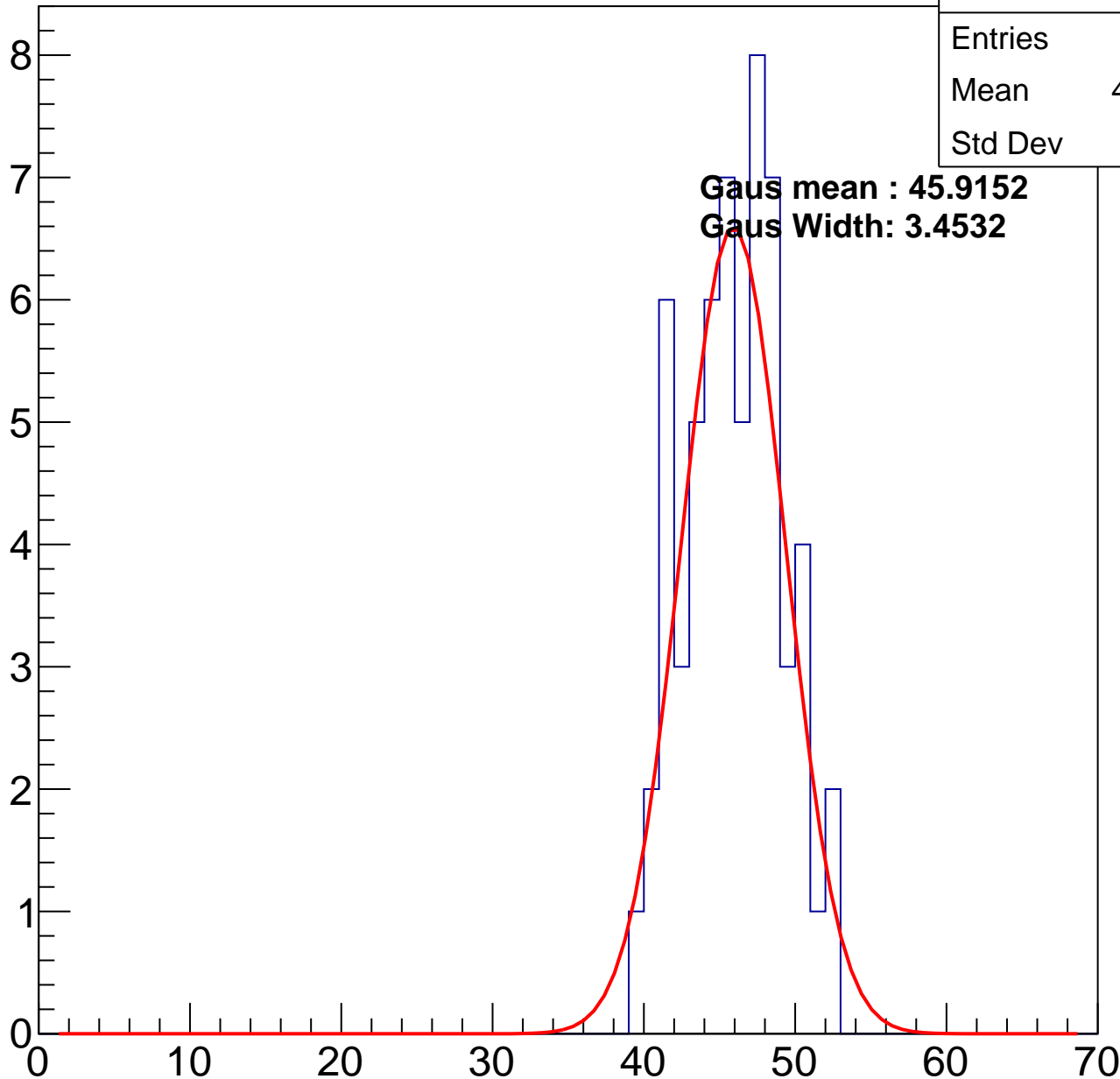
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	60
Mean	45.48
Std Dev	3.17

Gaus mean : 45.9152

Gaus Width: 3.4532

ampl

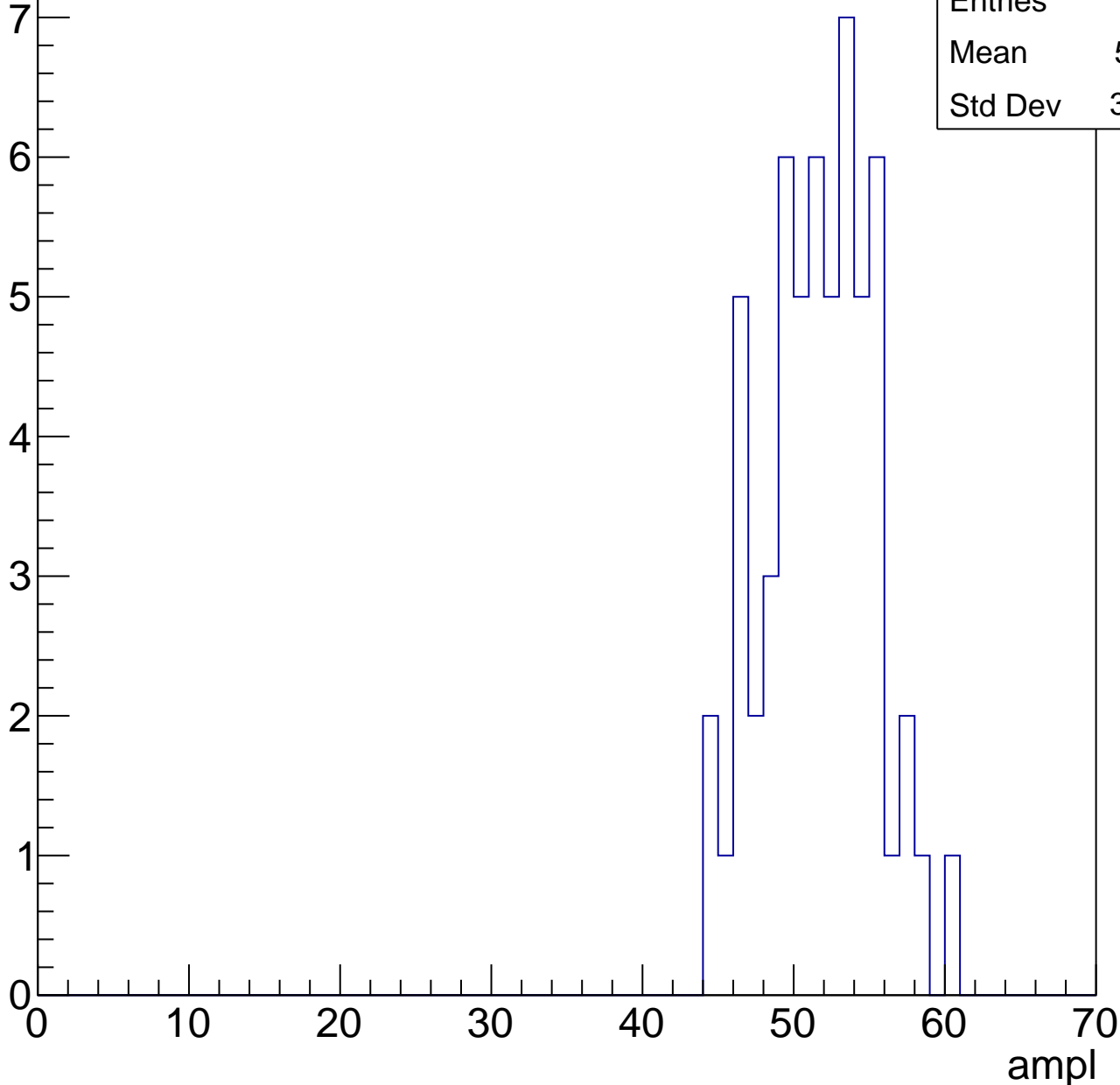


# B1L101S, U16-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	51.21
Std Dev	3.585

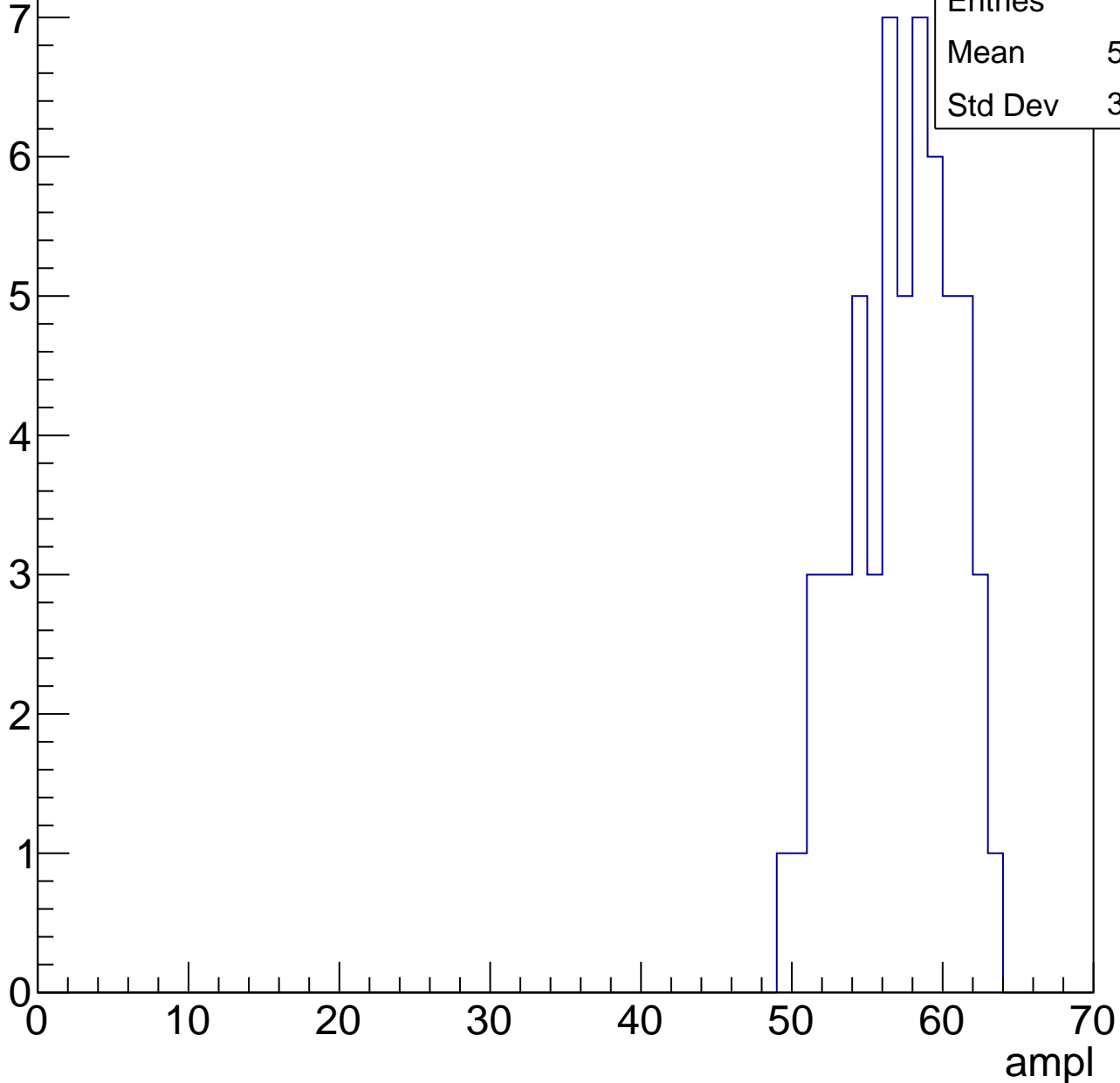


# B1L101S, U16-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	56.78
Std Dev	3.404

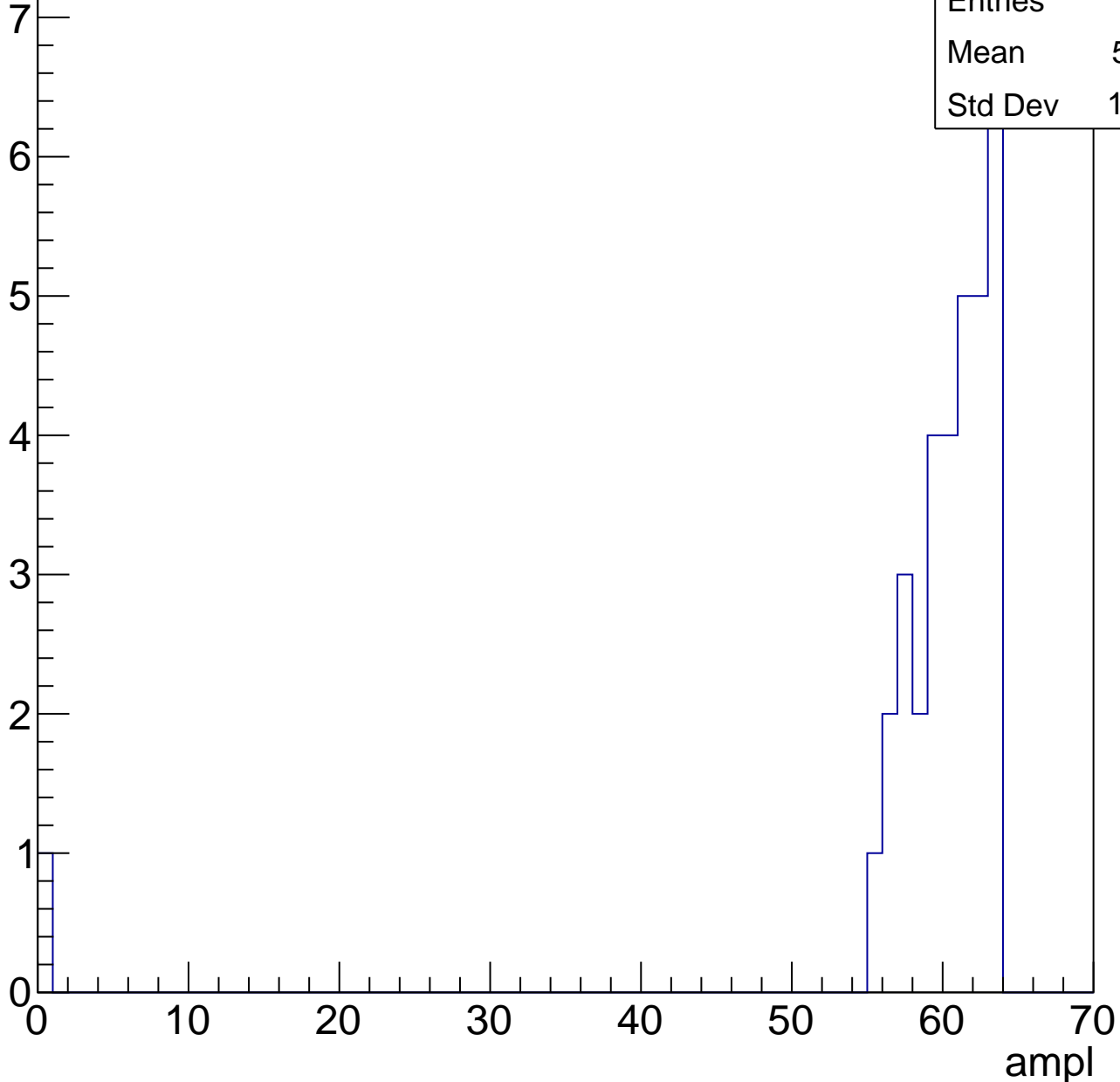


# B1L101S, U16-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	34
Mean	58.41
Std Dev	10.43



# B1L101S, U16-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch49, adc0

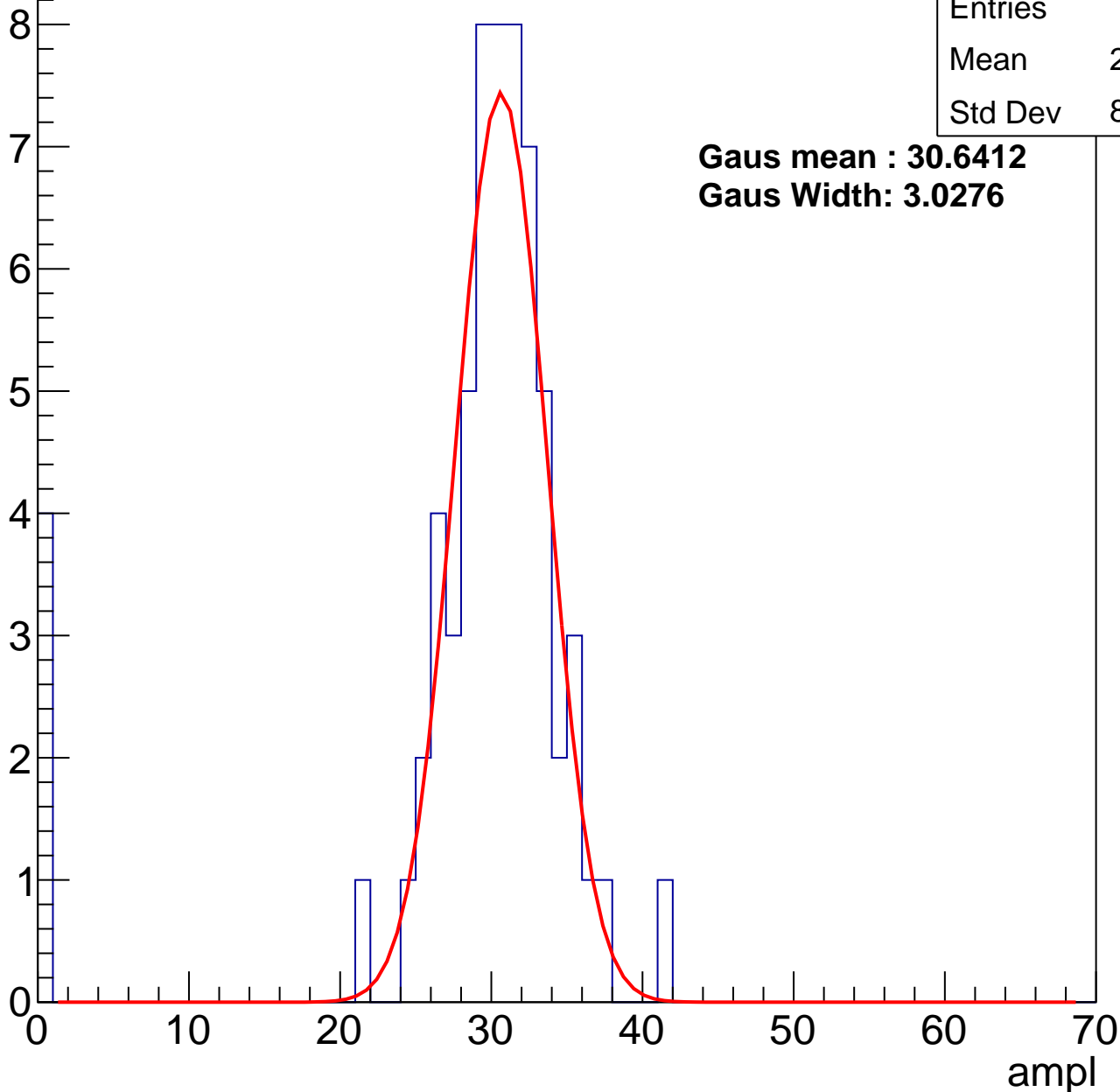
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	28.38
Std Dev	8.015

**Gaus mean : 30.6412**

**Gaus Width: 3.0276**



# B1L101S, U16-ch49, adc1

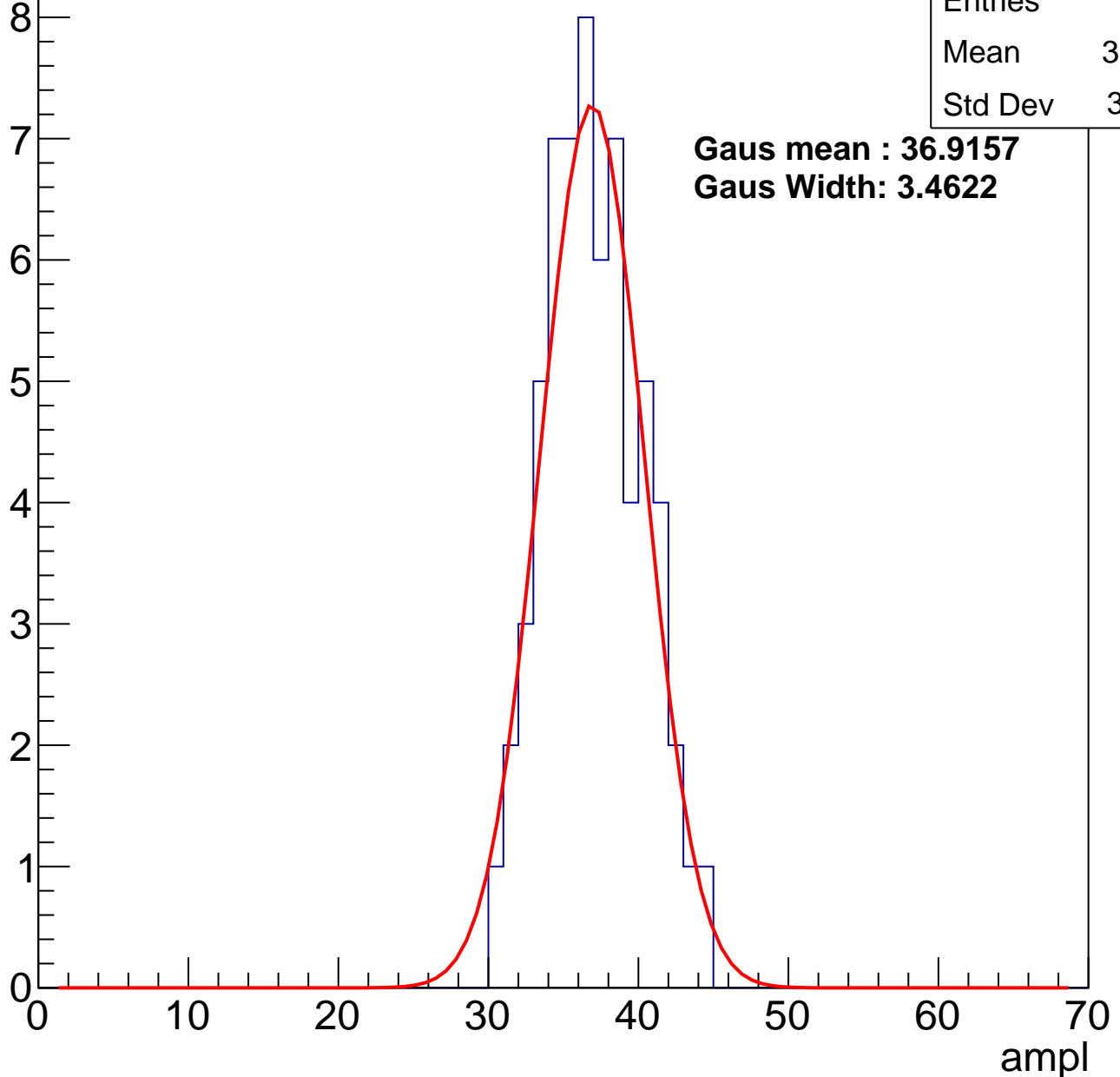
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	36.56
Std Dev	3.161

**Gaus mean : 36.9157**

**Gaus Width: 3.4622**



# B1L101S, U16-ch49, adc2

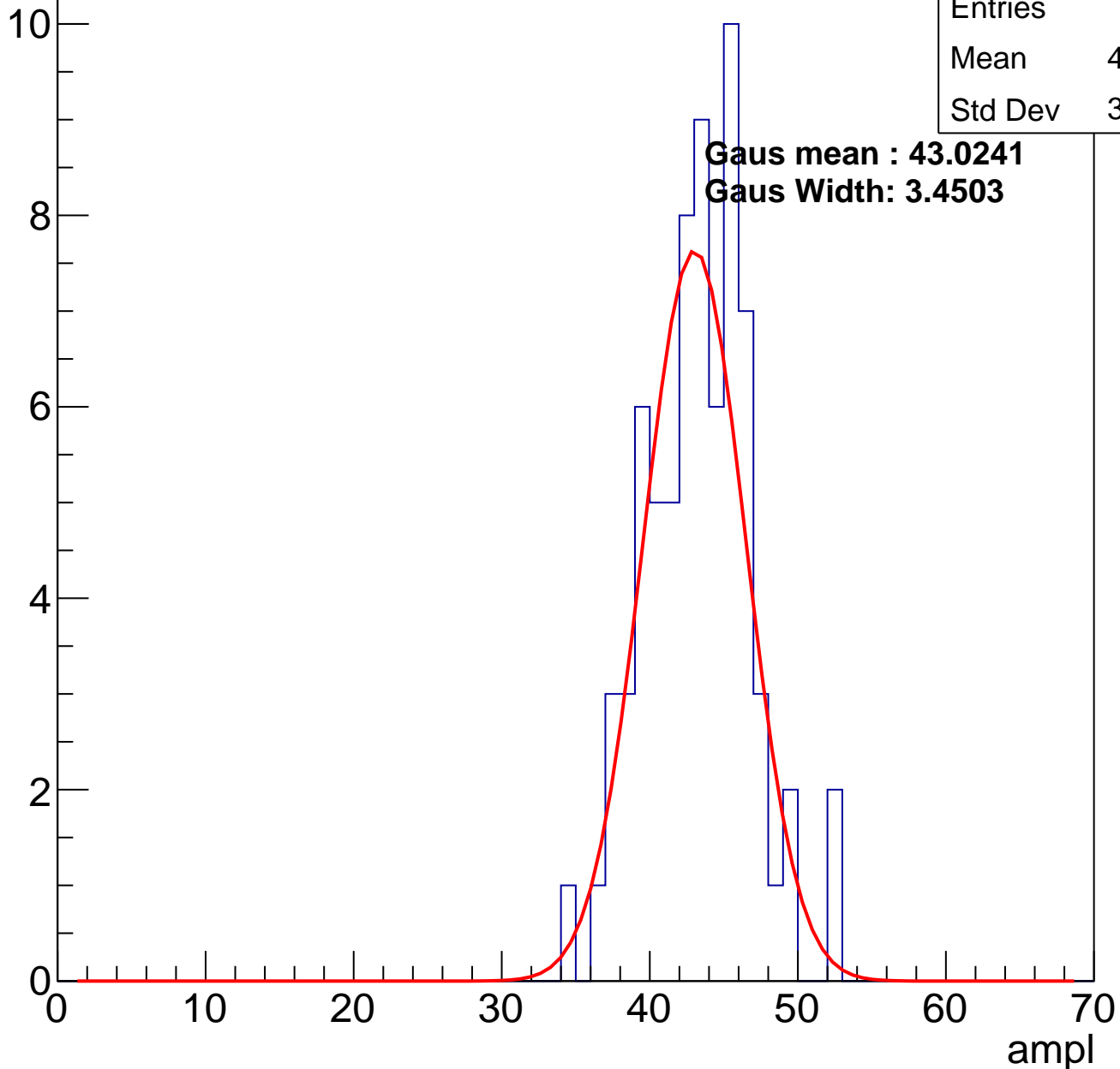
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	72
Mean	42.83
Std Dev	3.528

**Gaus mean : 43.0241**

**Gaus Width: 3.4503**

Entry

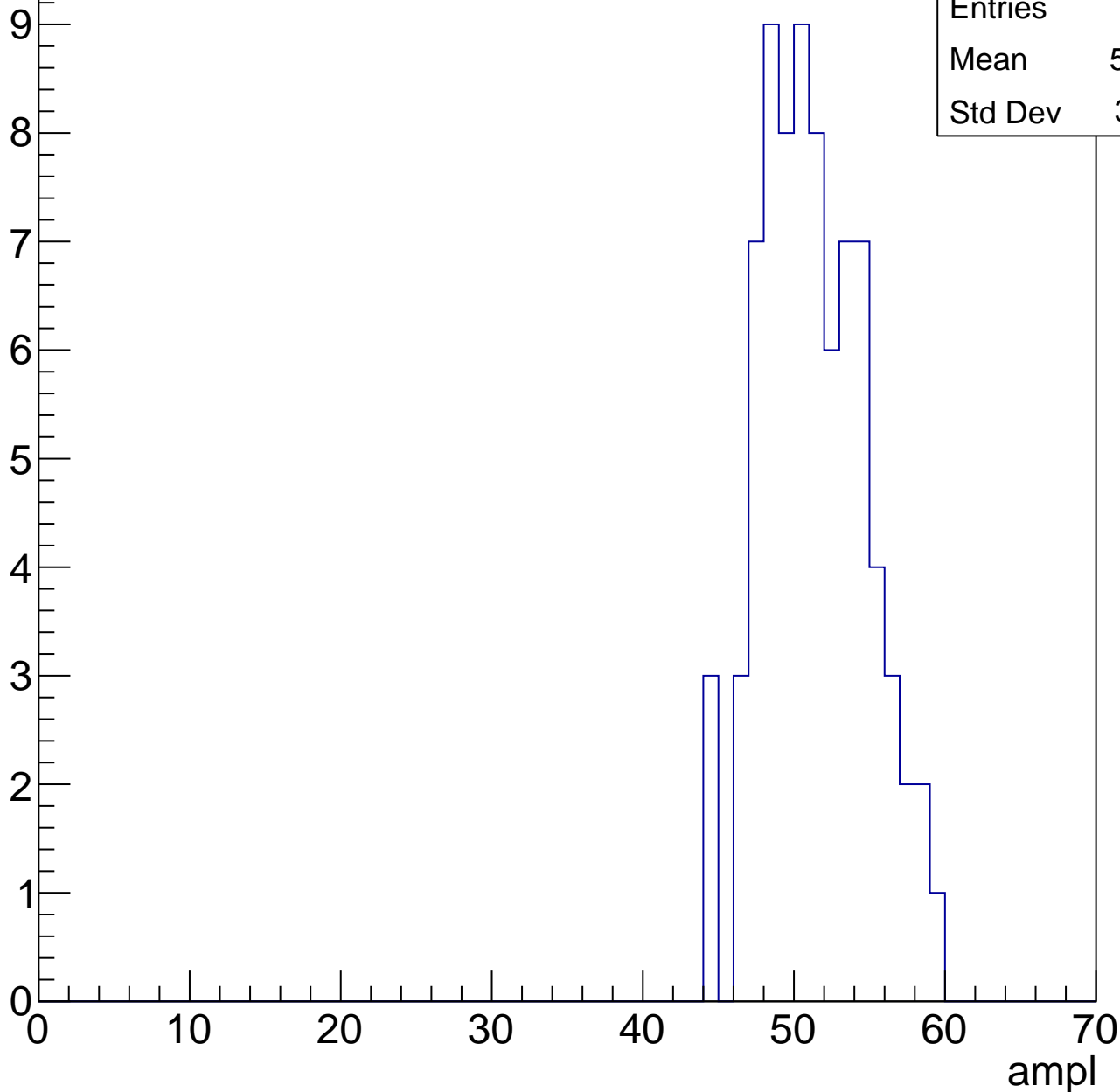


# B1L101S, U16-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

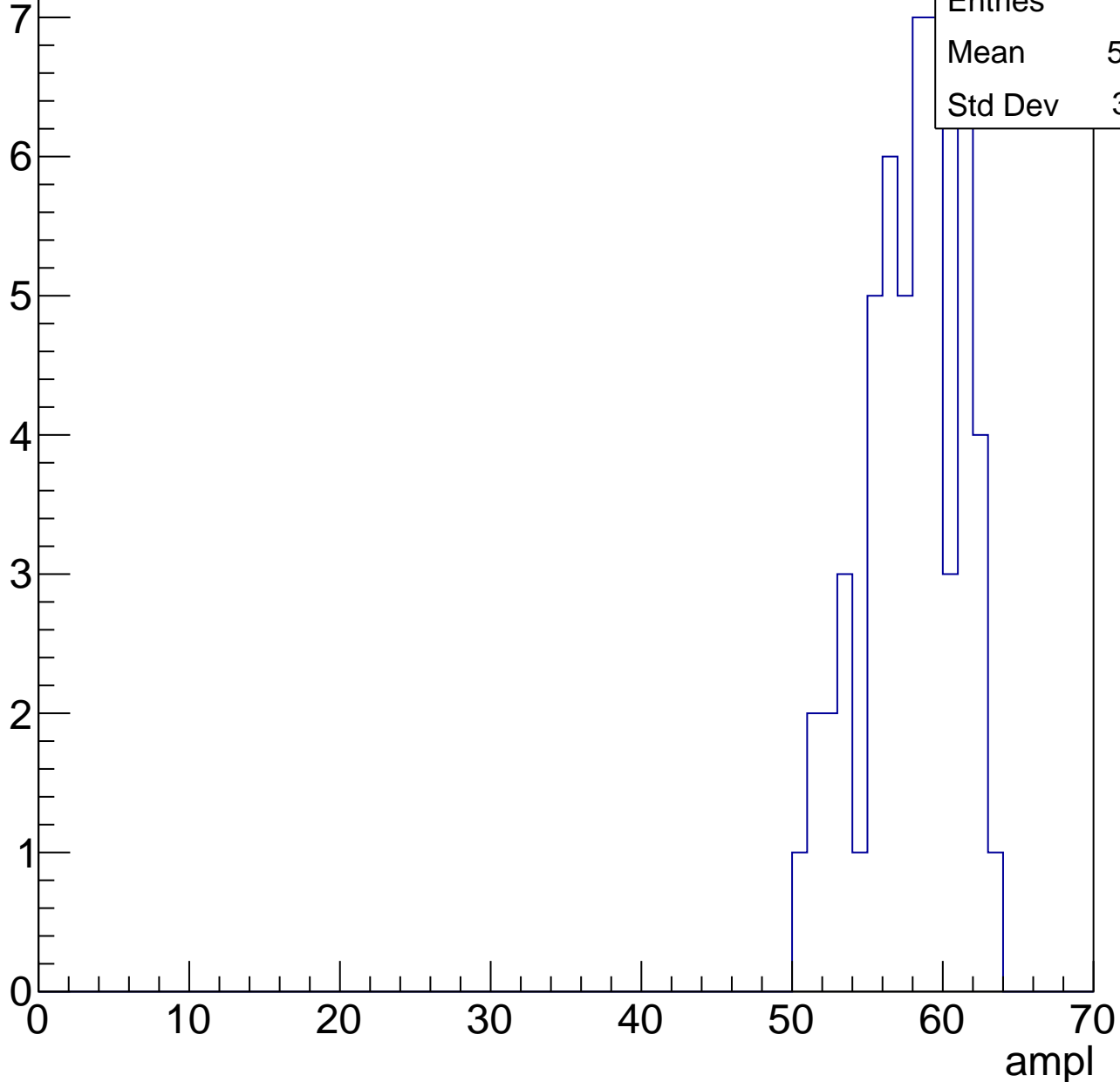
Entries	79
Mean	50.87
Std Dev	3.421



# B1L101S, U16-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch49, adc5

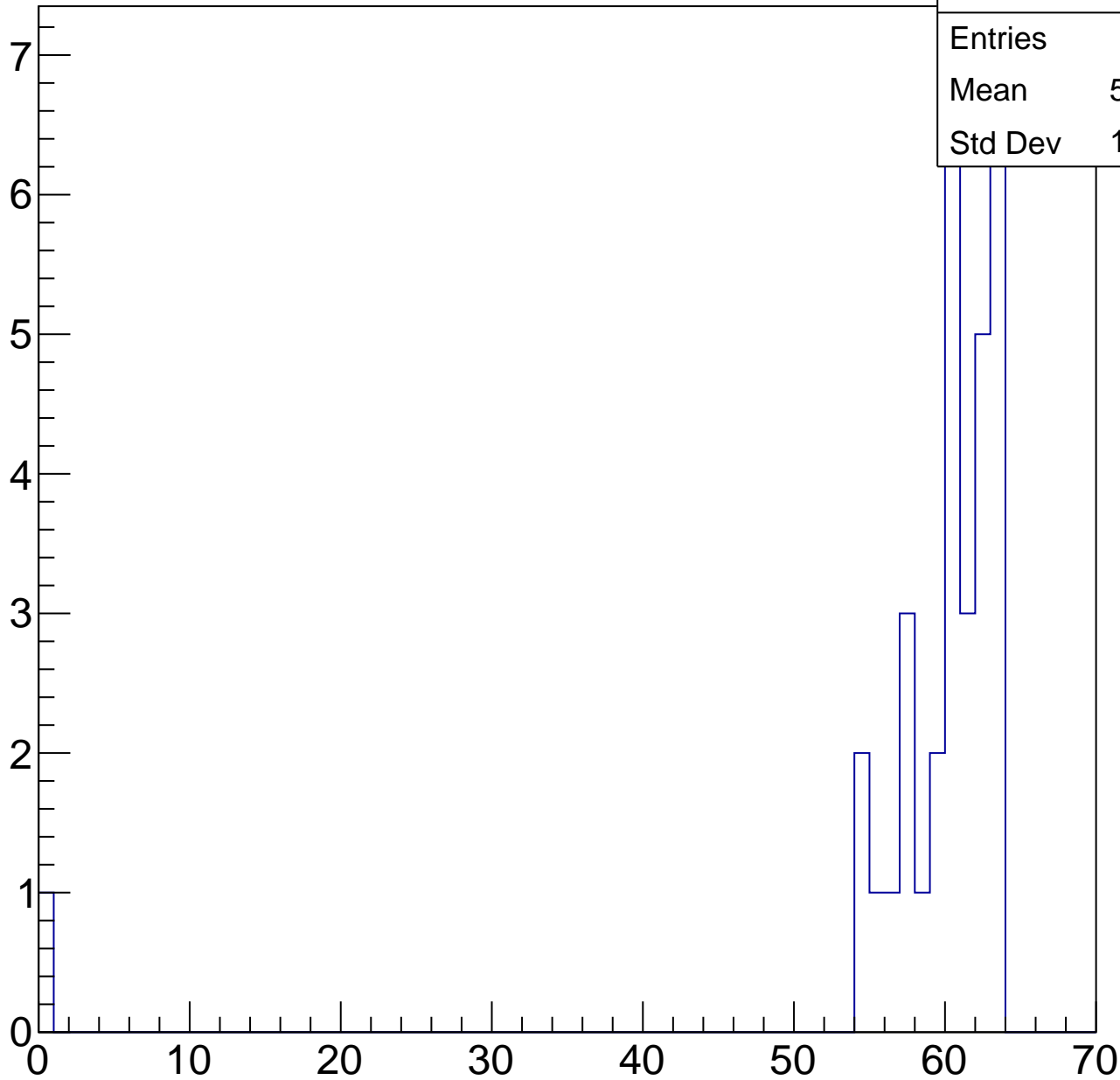
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	33
Mean	58.18
Std Dev	10.62

ampl



# B1L101S, U16-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U16-ch50, adc0

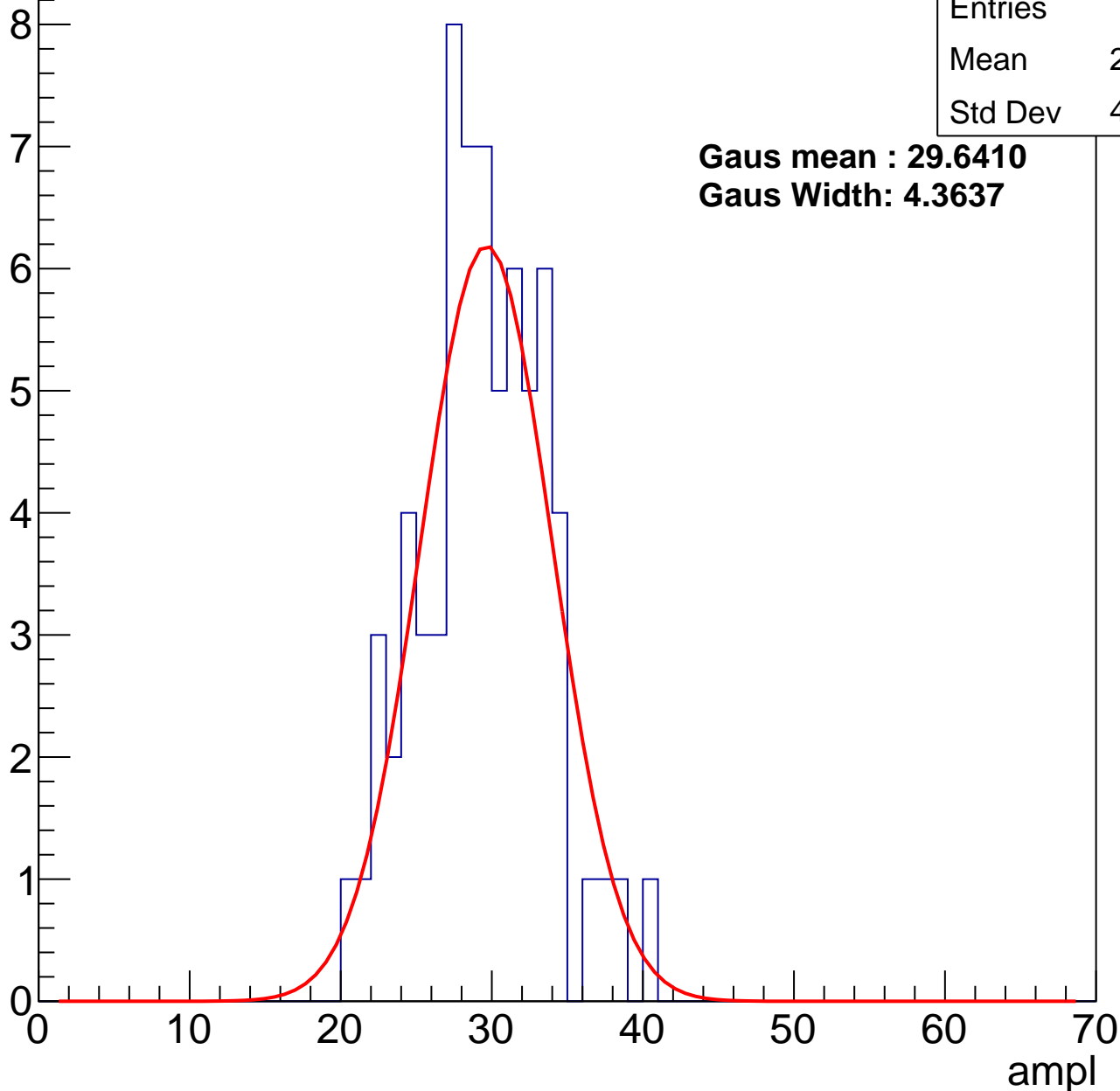
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	28.96
Std Dev	4.105

**Gaus mean : 29.6410**

**Gaus Width: 4.3637**



# B1L101S, U16-ch50, adc1

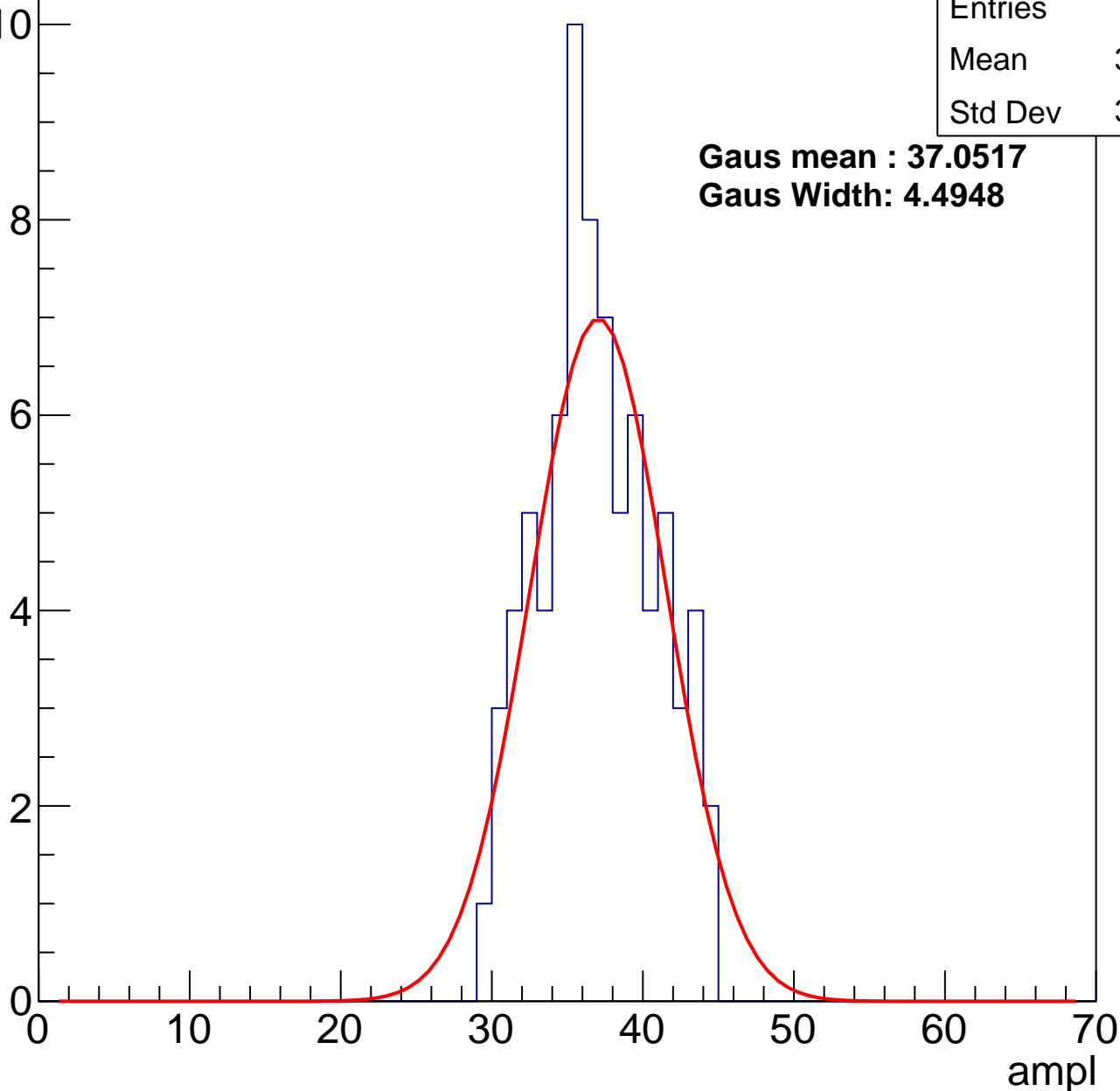
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	36.51
Std Dev	3.761

**Gaus mean : 37.0517**

**Gaus Width: 4.4948**



# B1L101S, U16-ch50, adc2

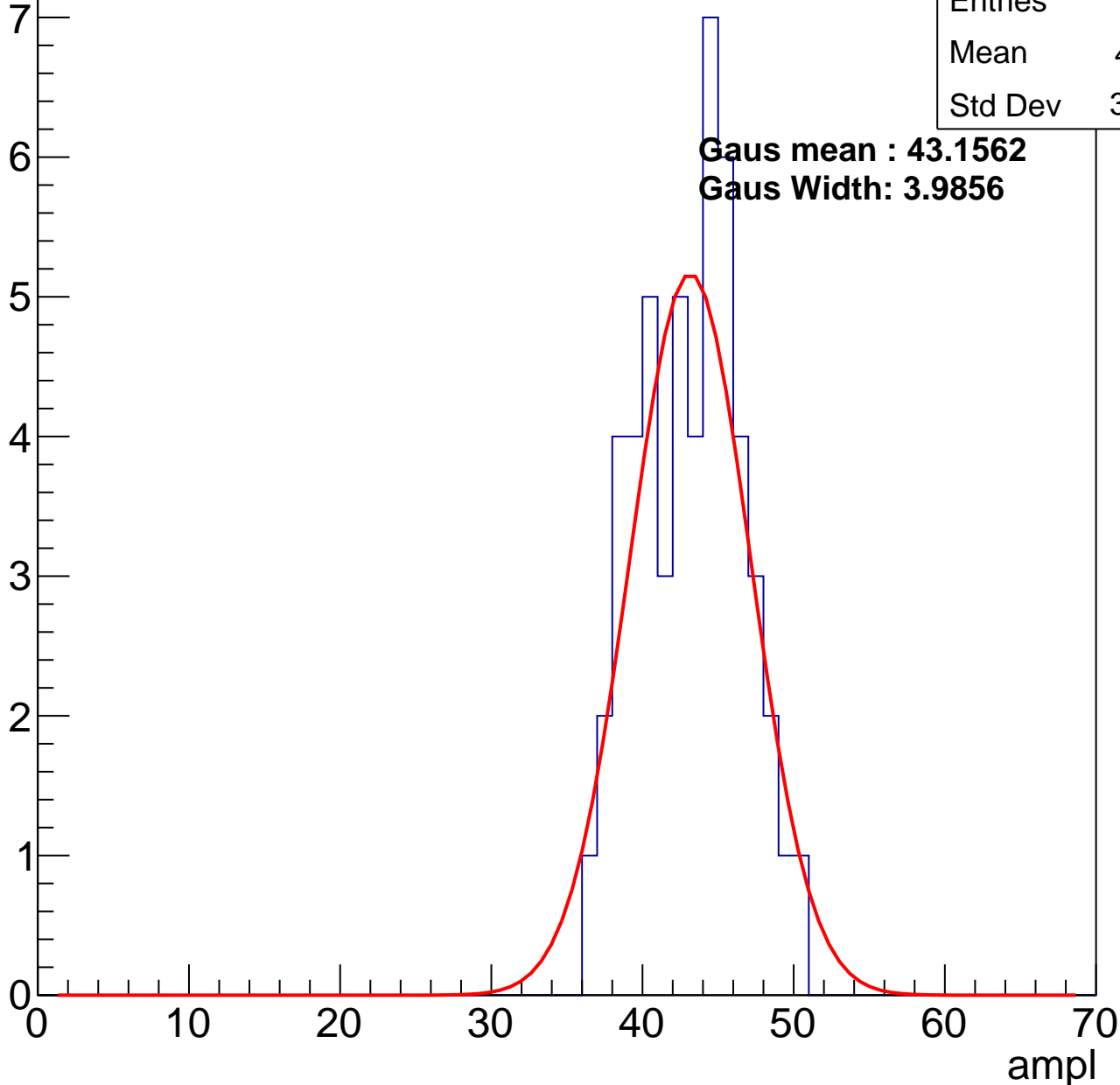
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	42.71
Std Dev	3.376

**Gaus mean : 43.1562**

**Gaus Width: 3.9856**

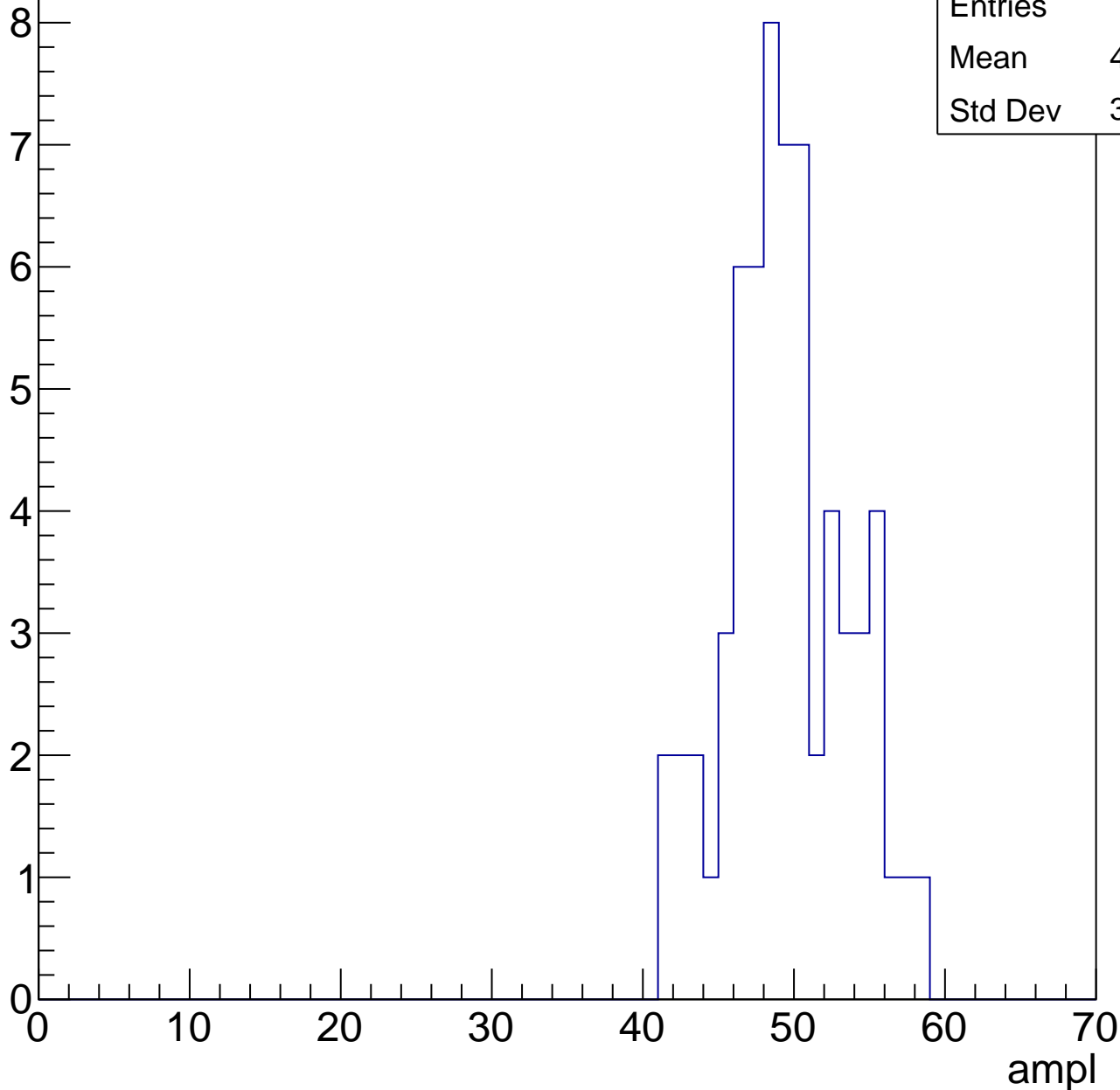


# B1L101S, U16-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	49.02
Std Dev	3.922

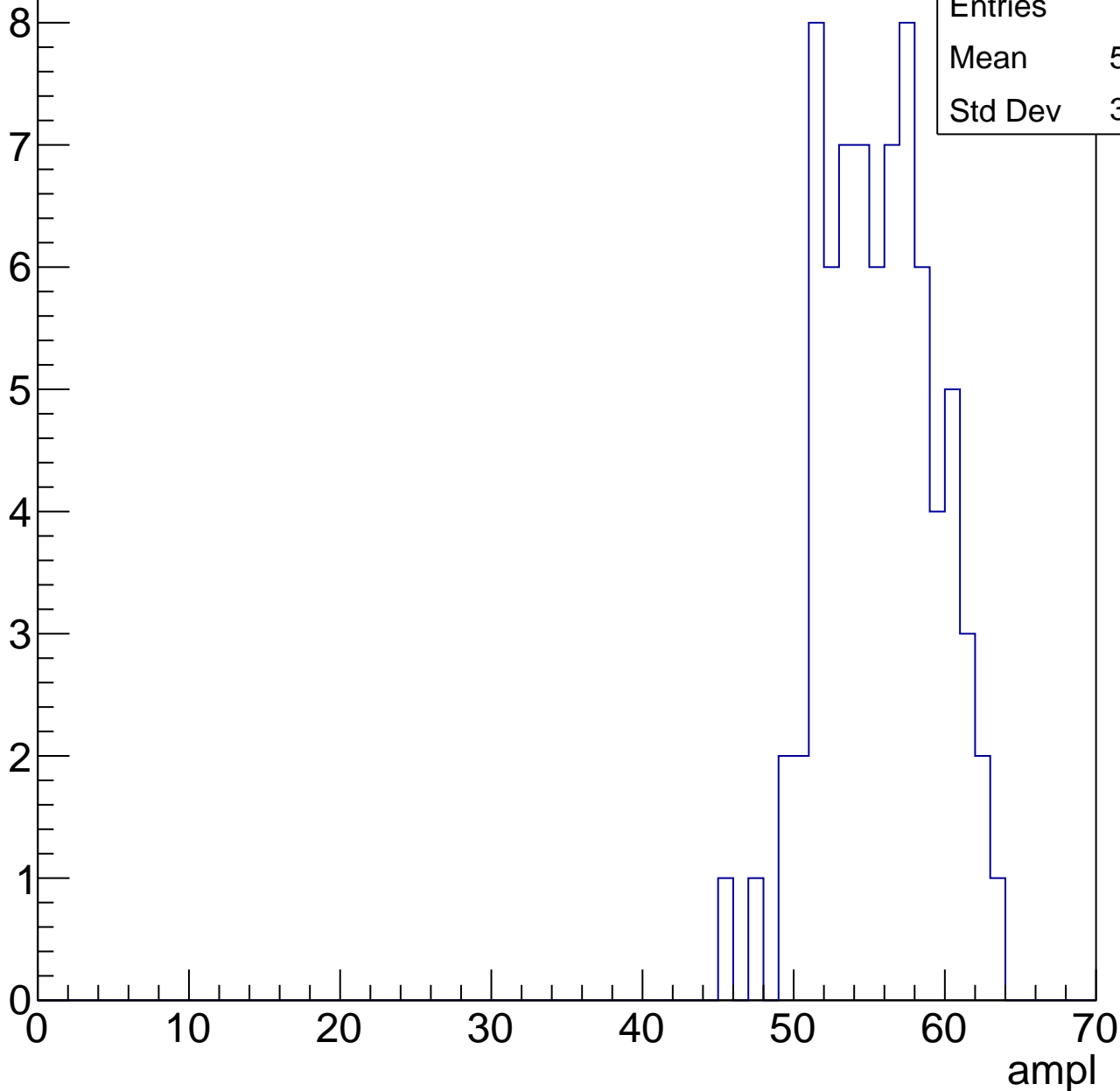


# B1L101S, U16-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

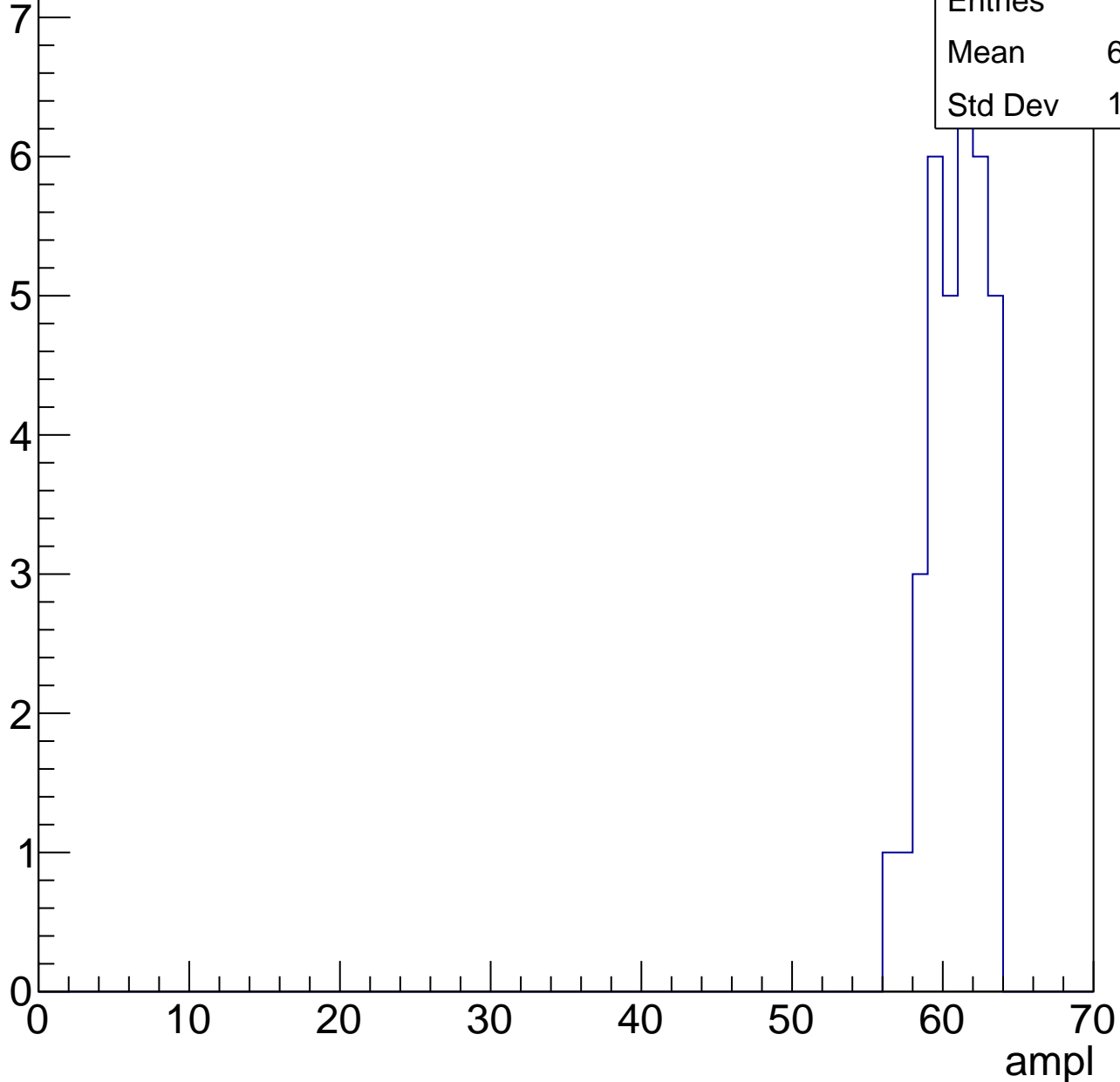
Entries	76
Mean	55.14
Std Dev	3.723



# B1L101S, U16-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

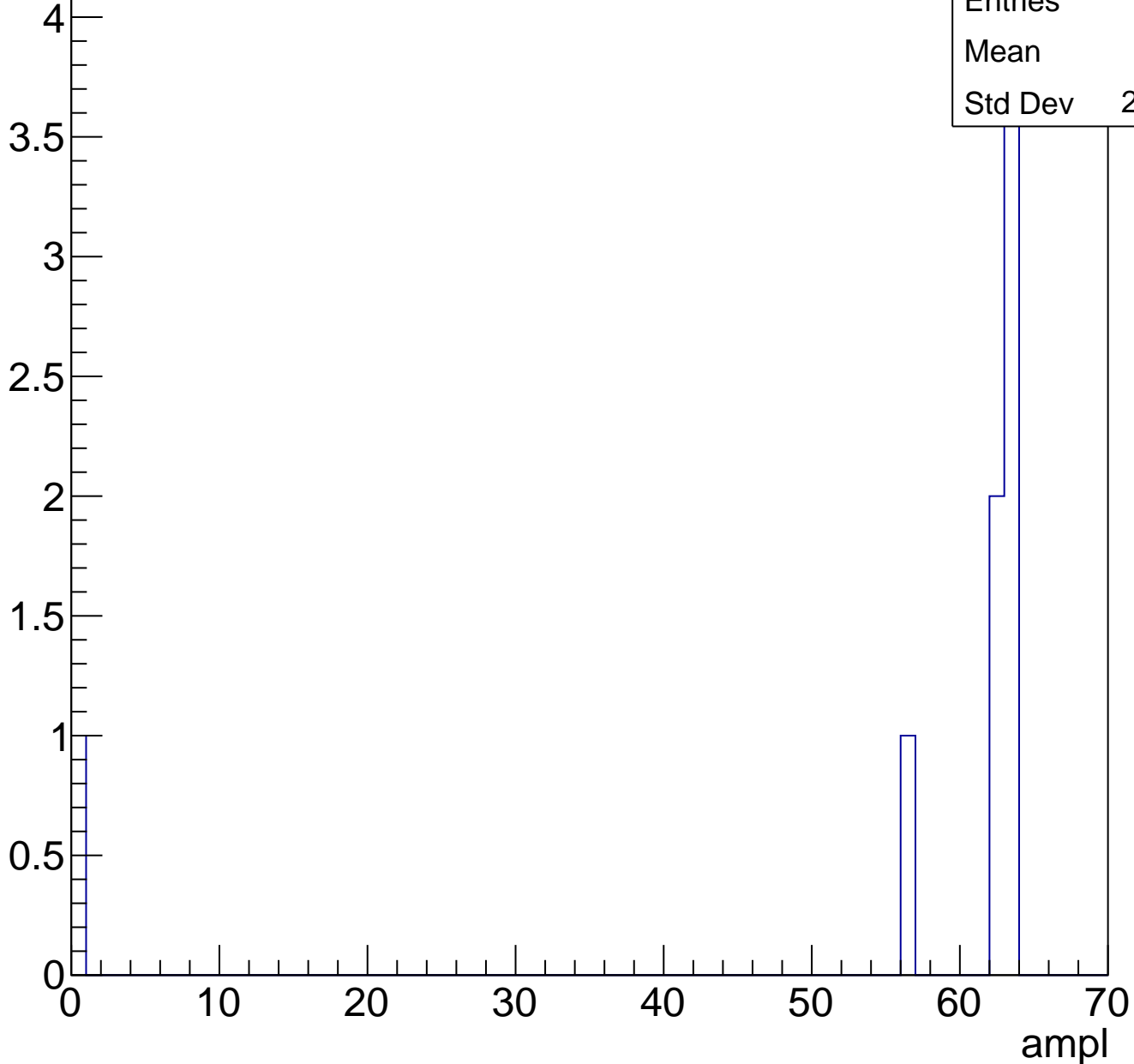
Entry



# B1L101S, U16-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U16-ch51, adc0

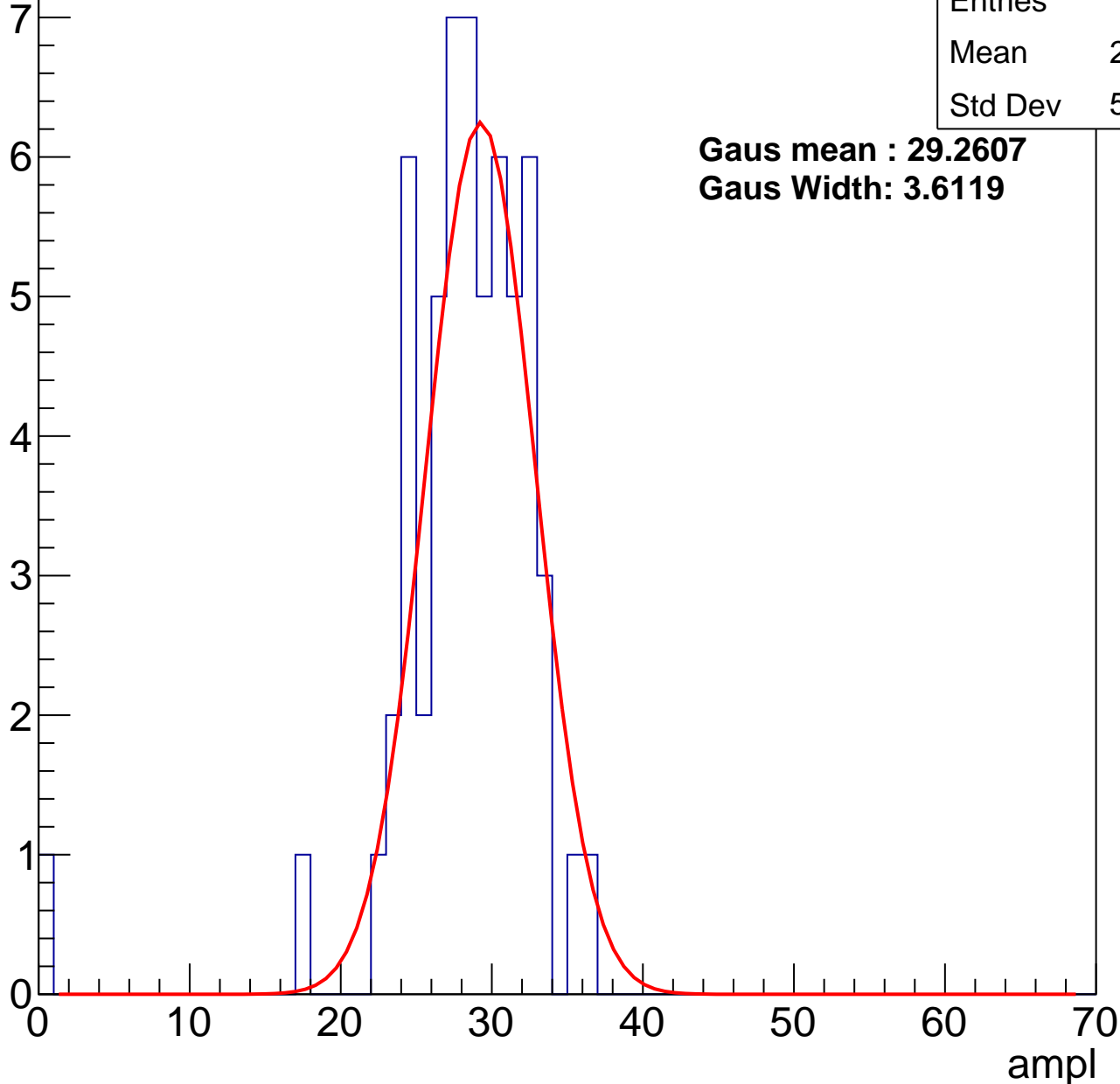
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	27.73
Std Dev	5.018

**Gaus mean : 29.2607**

**Gaus Width: 3.6119**



# B1L101S, U16-ch51, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	80
Mean	34.84
Std Dev	3.897

**Gaus mean : 35.3628**

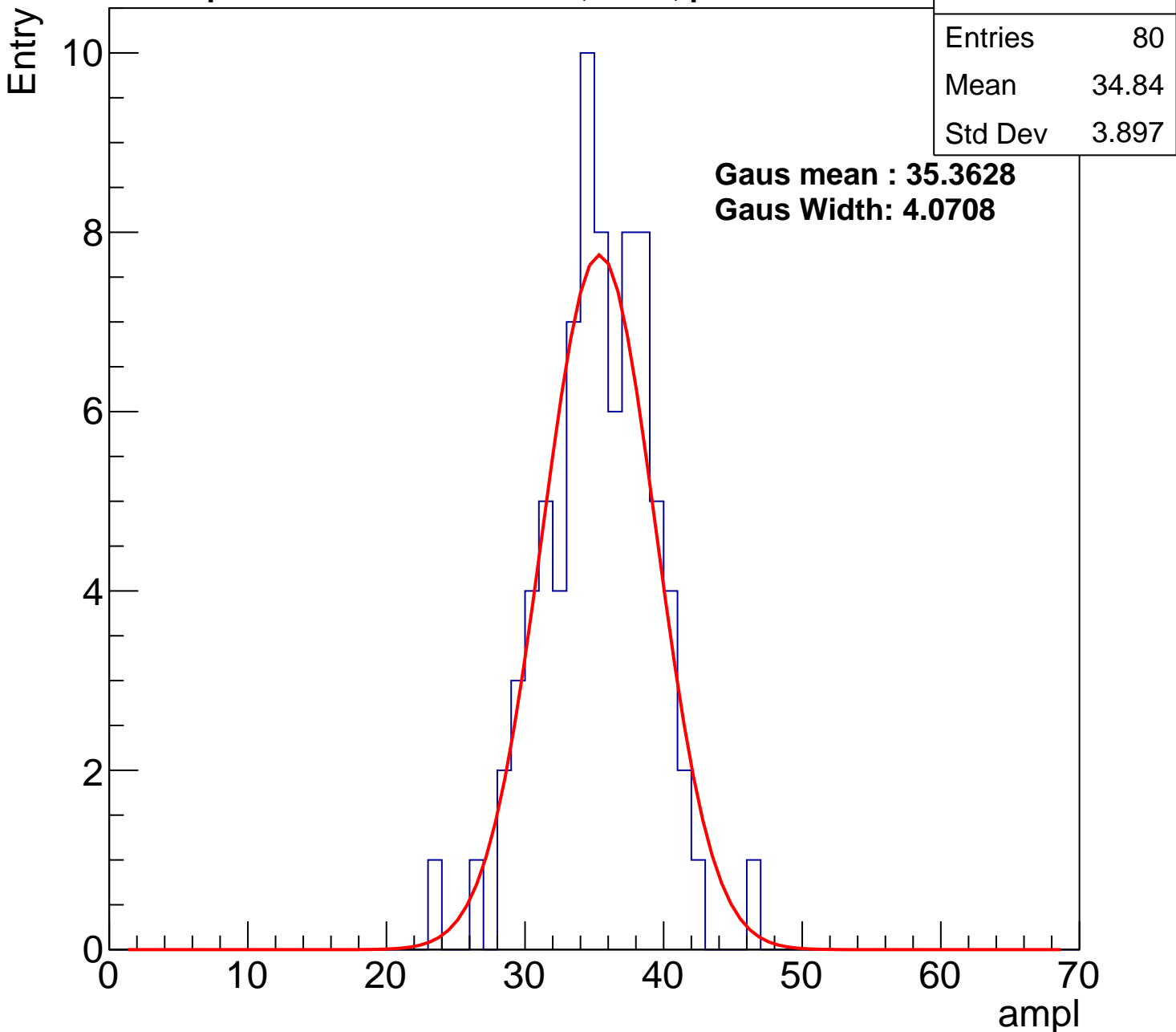
**Gaus Width: 4.0708**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch51, adc2

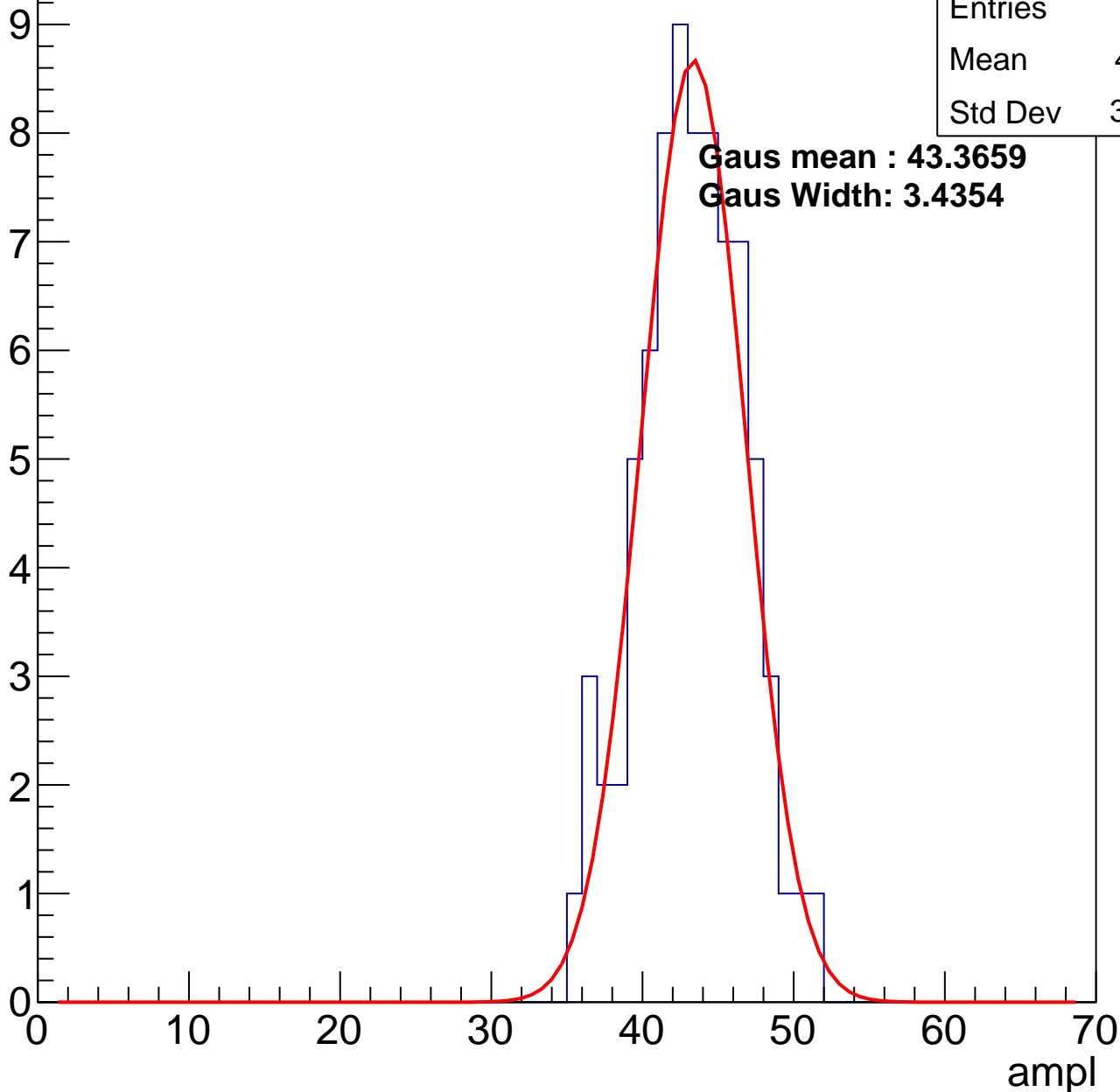
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	42.81
Std Dev	3.434

**Gaus mean : 43.3659**

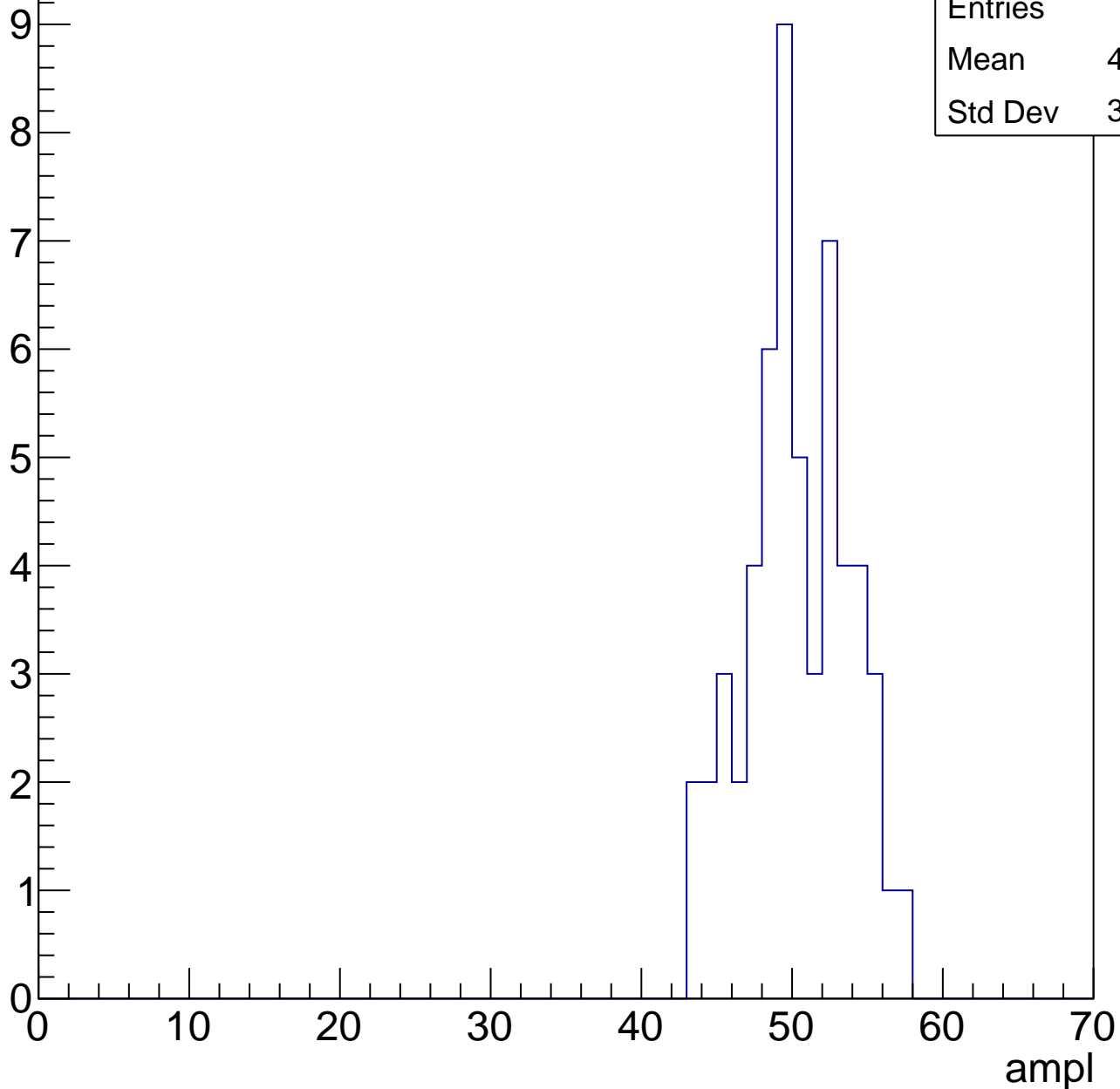
**Gaus Width: 3.4354**



# B1L101S, U16-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



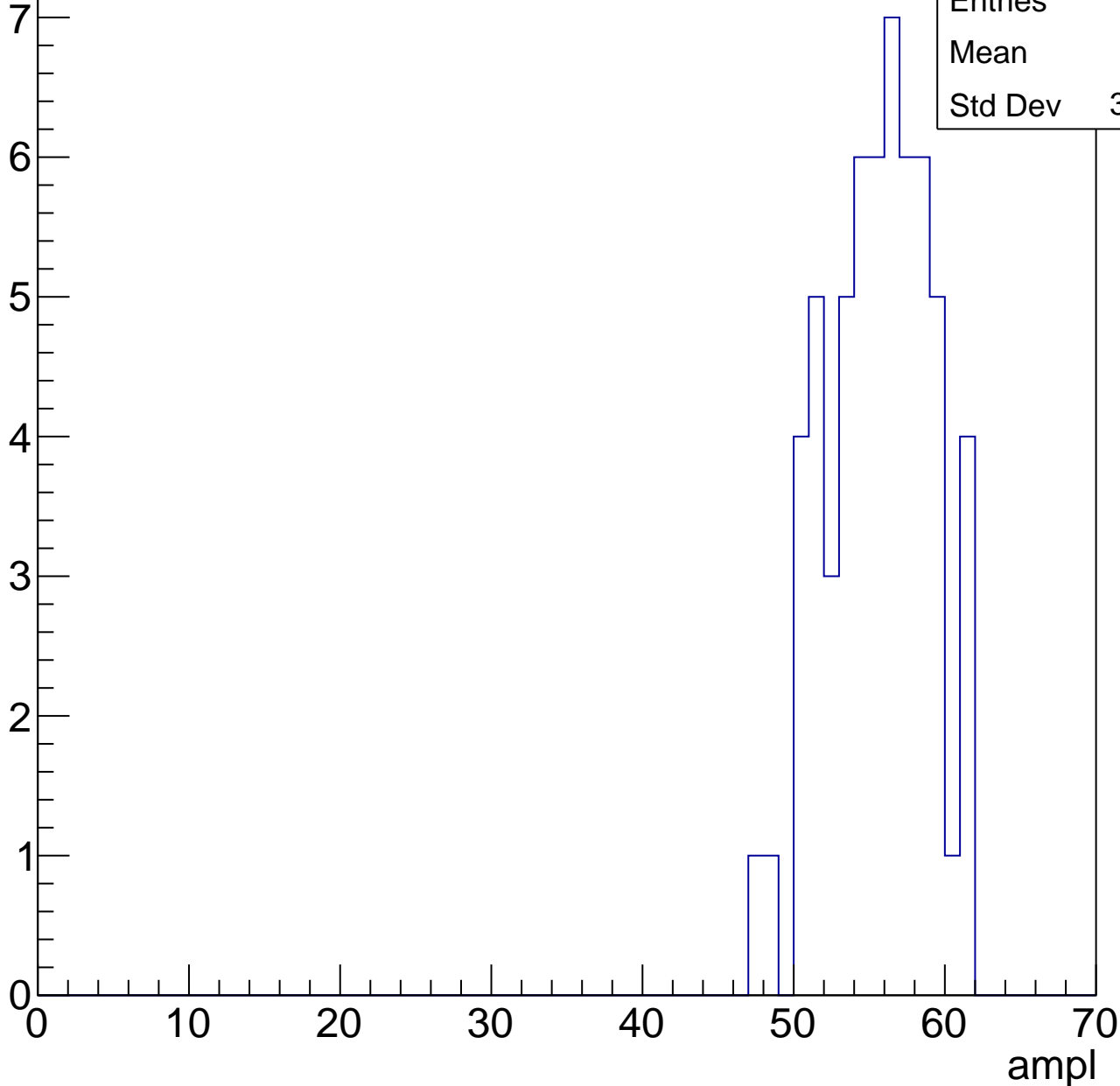
Entries	56
Mean	49.84
Std Dev	3.369

# B1L101S, U16-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	55.1
Std Dev	3.365

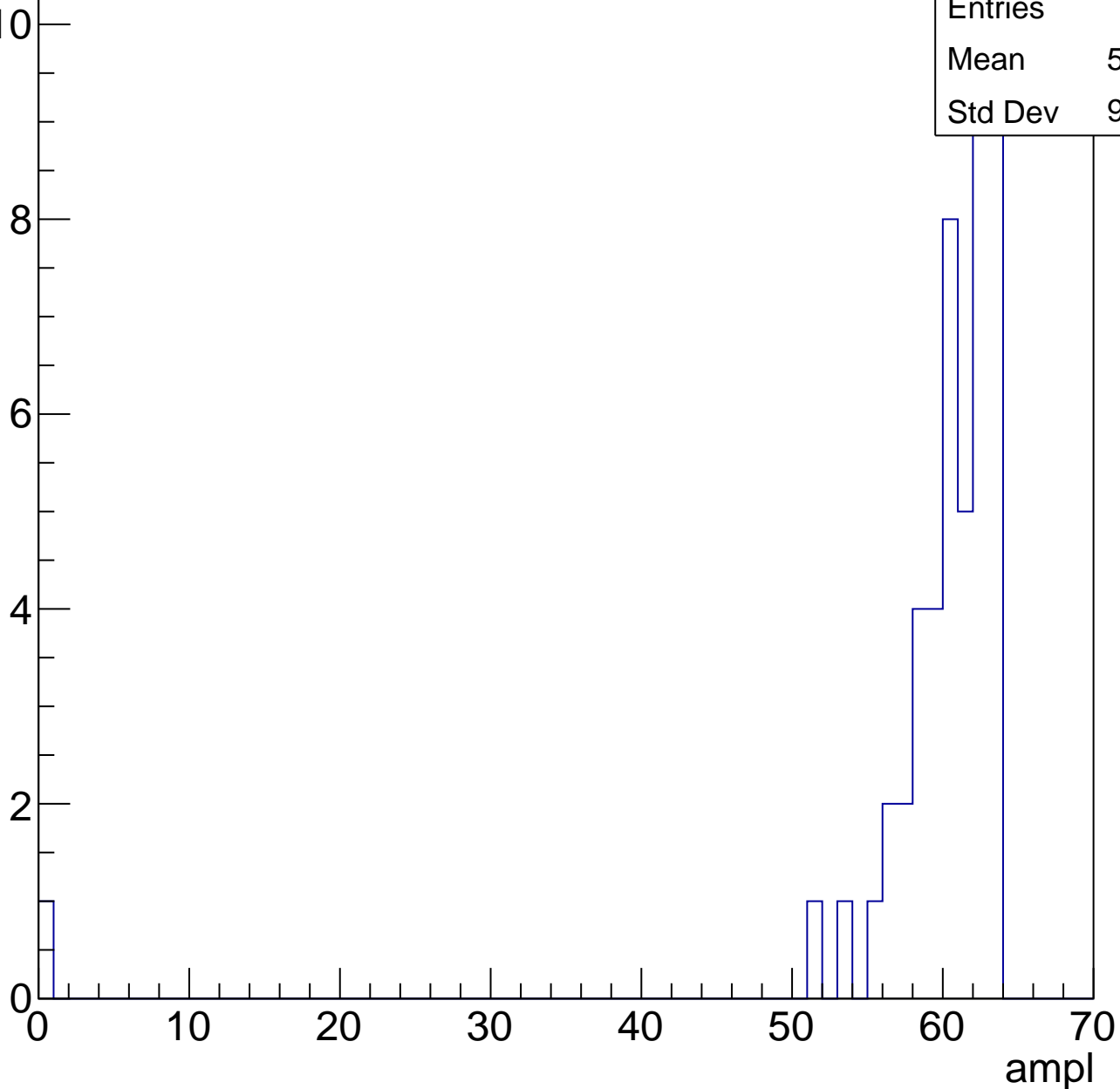


# B1L101S, U16-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	58.88
Std Dev	9.008



# B1L101S, U16-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

5

Mean

59.8

Std Dev

1.72



# B1L101S, U16-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch52, adc0

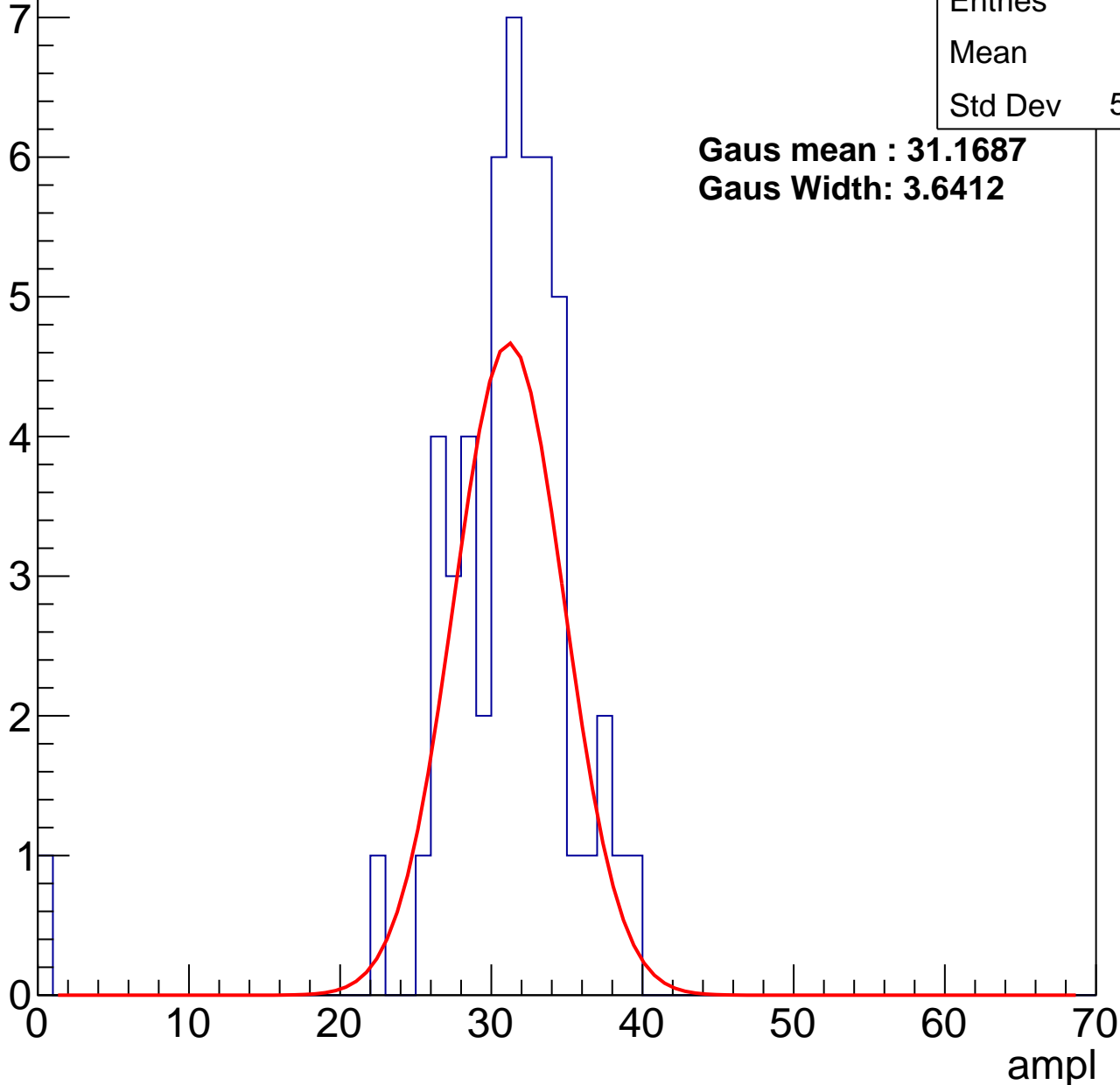
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	30.4
Std Dev	5.475

**Gaus mean : 31.1687**

**Gaus Width: 3.6412**



# B1L101S, U16-ch52, adc1

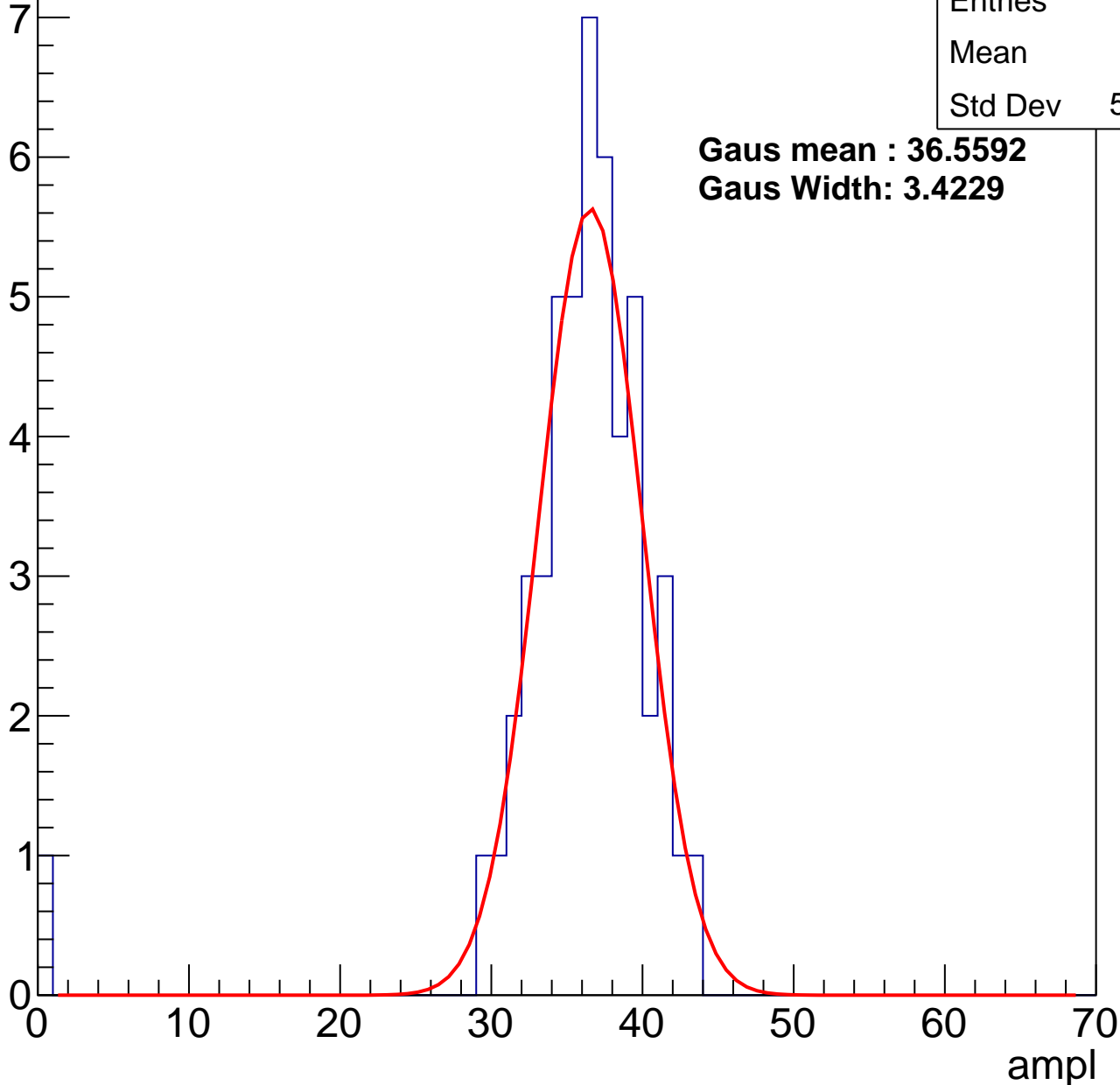
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	35.4
Std Dev	5.953

**Gaus mean : 36.5592**

**Gaus Width: 3.4229**



# B1L101S, U16-ch52, adc2

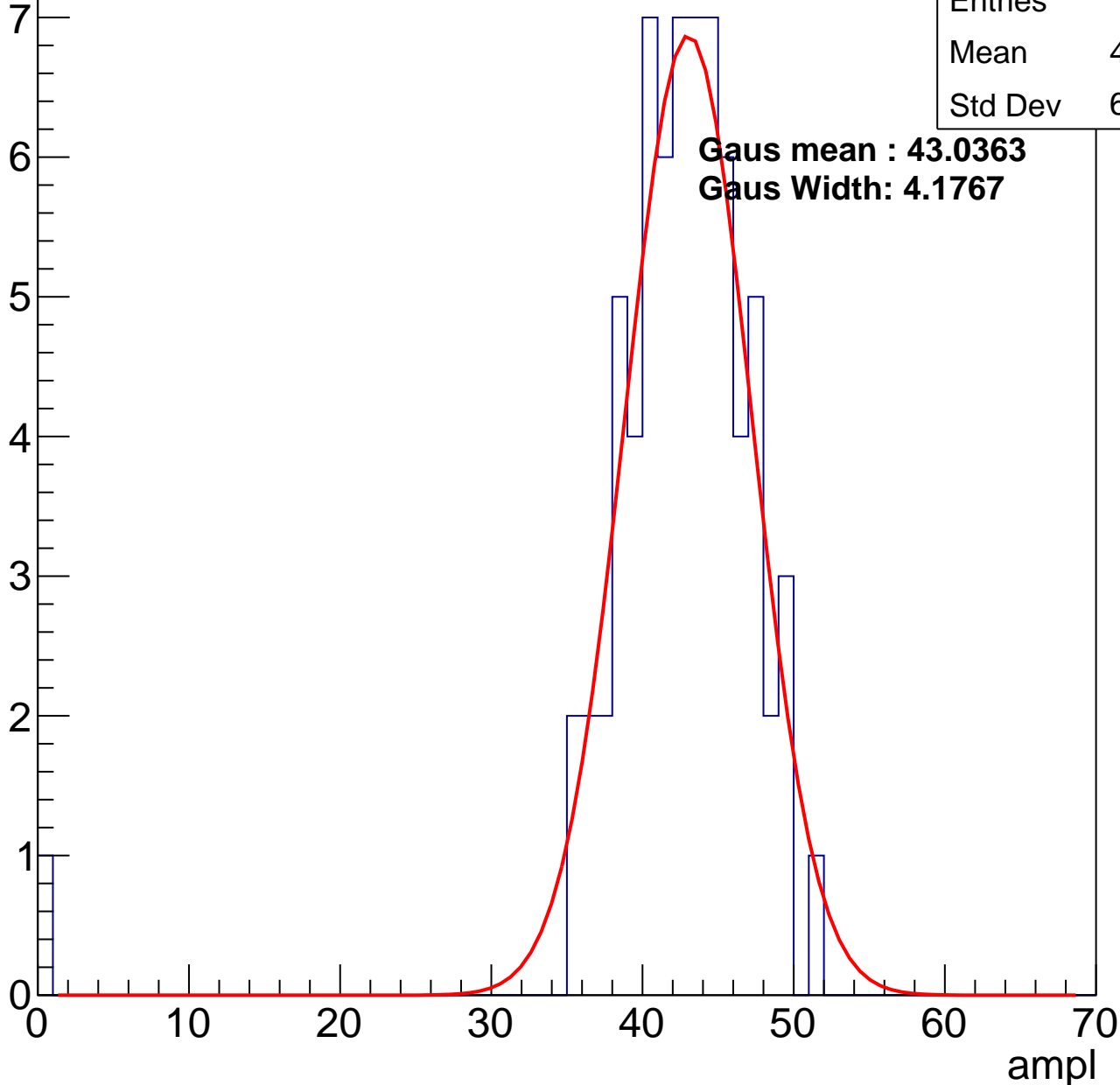
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	41.89
Std Dev	6.179

**Gaus mean : 43.0363**

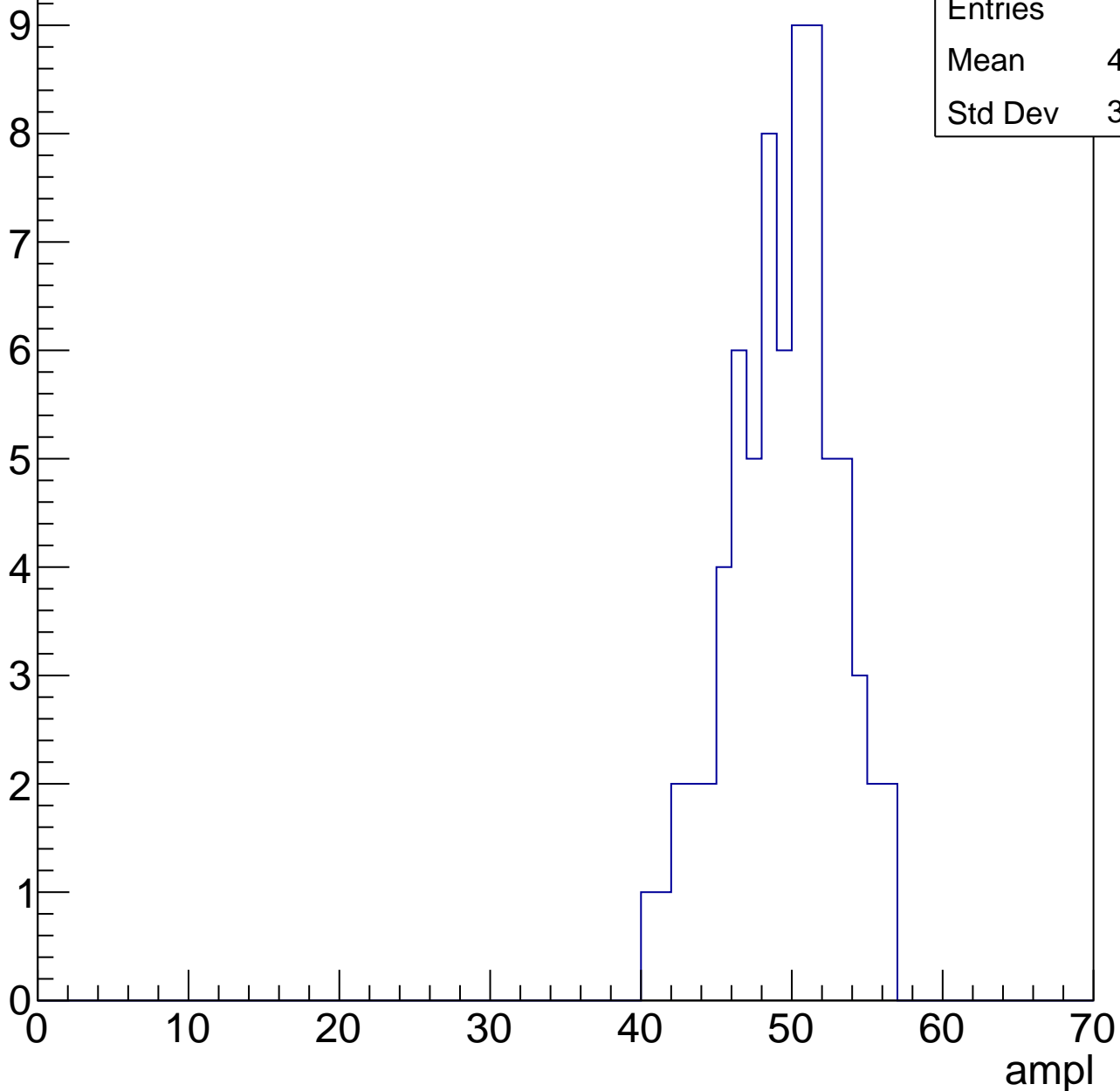
**Gaus Width: 4.1767**



# B1L101S, U16-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

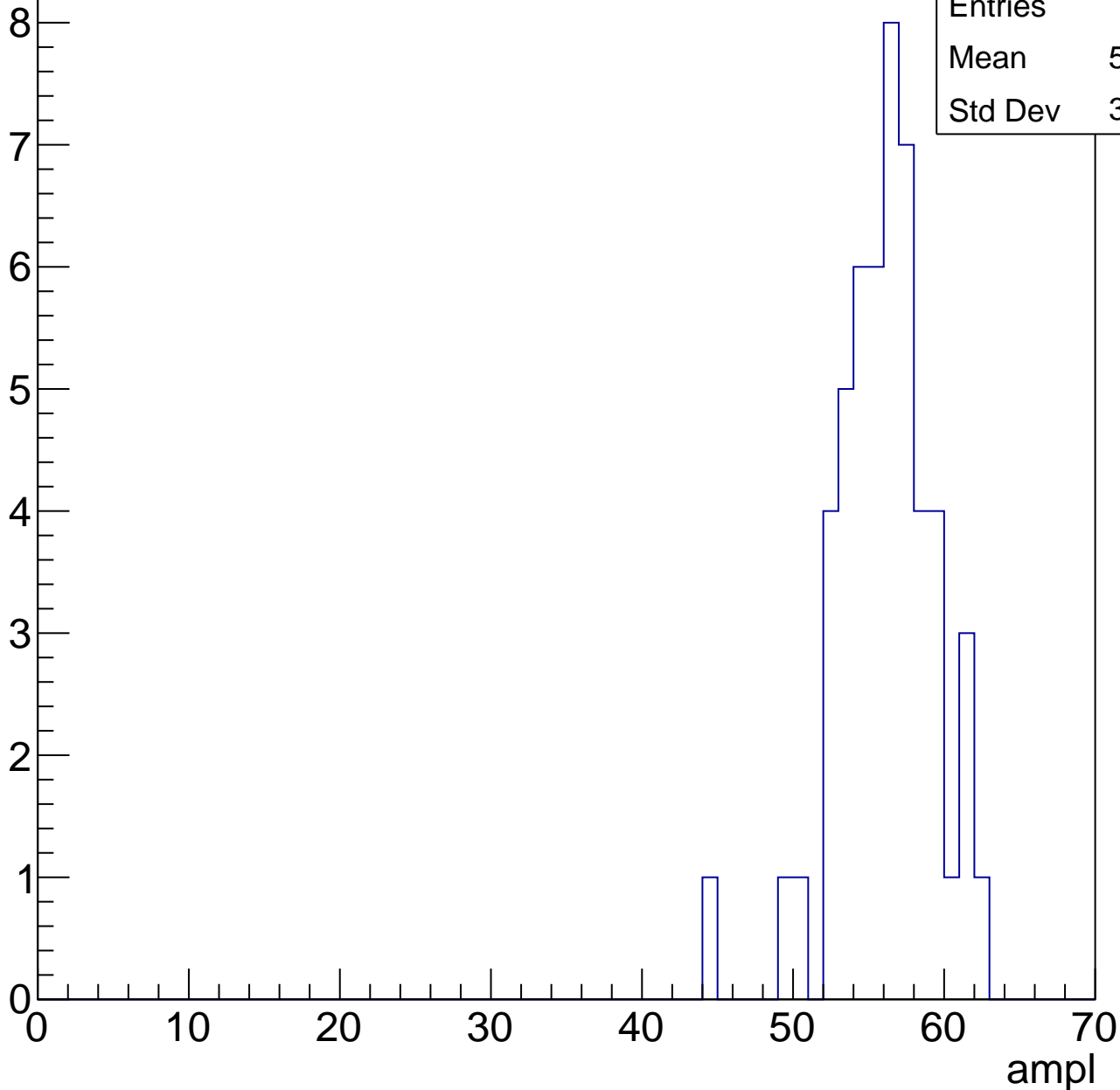


# B1L101S, U16-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	55.58
Std Dev	3.236

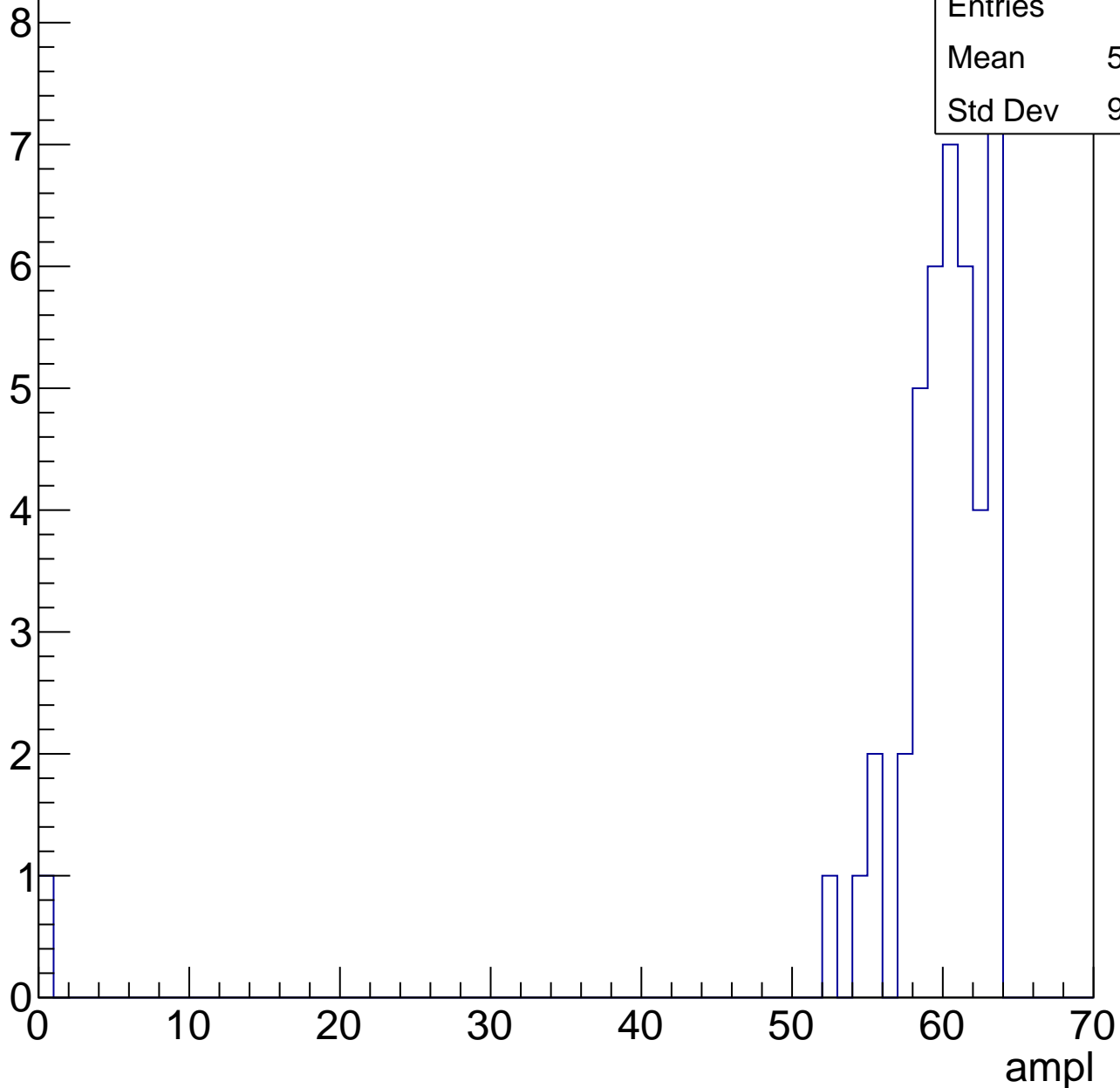


# B1L101S, U16-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	58.42
Std Dev	9.376

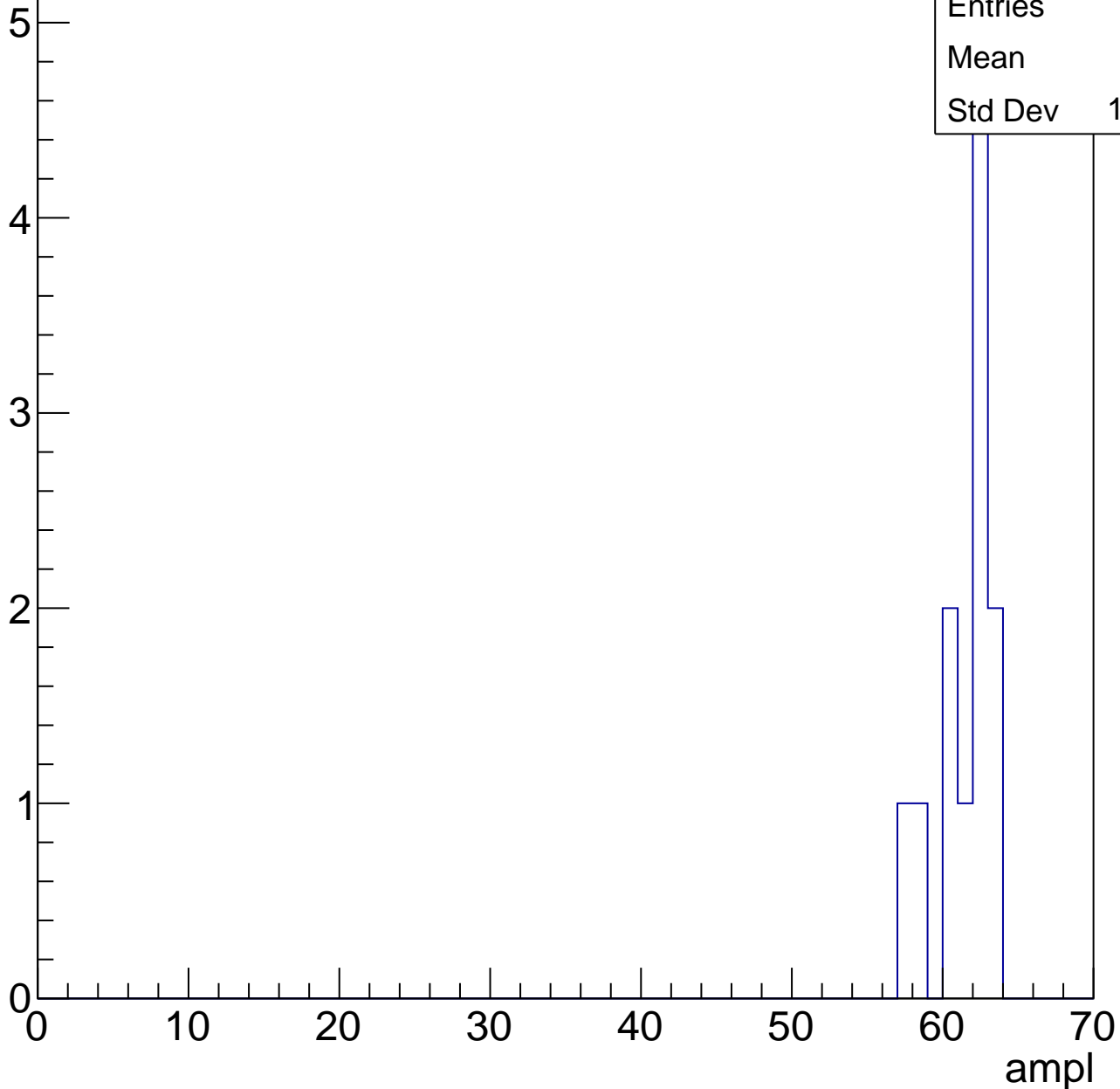


# B1L101S, U16-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	12
Mean	61
Std Dev	1.826





# B1L101S, U16-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U16-ch53, adc0

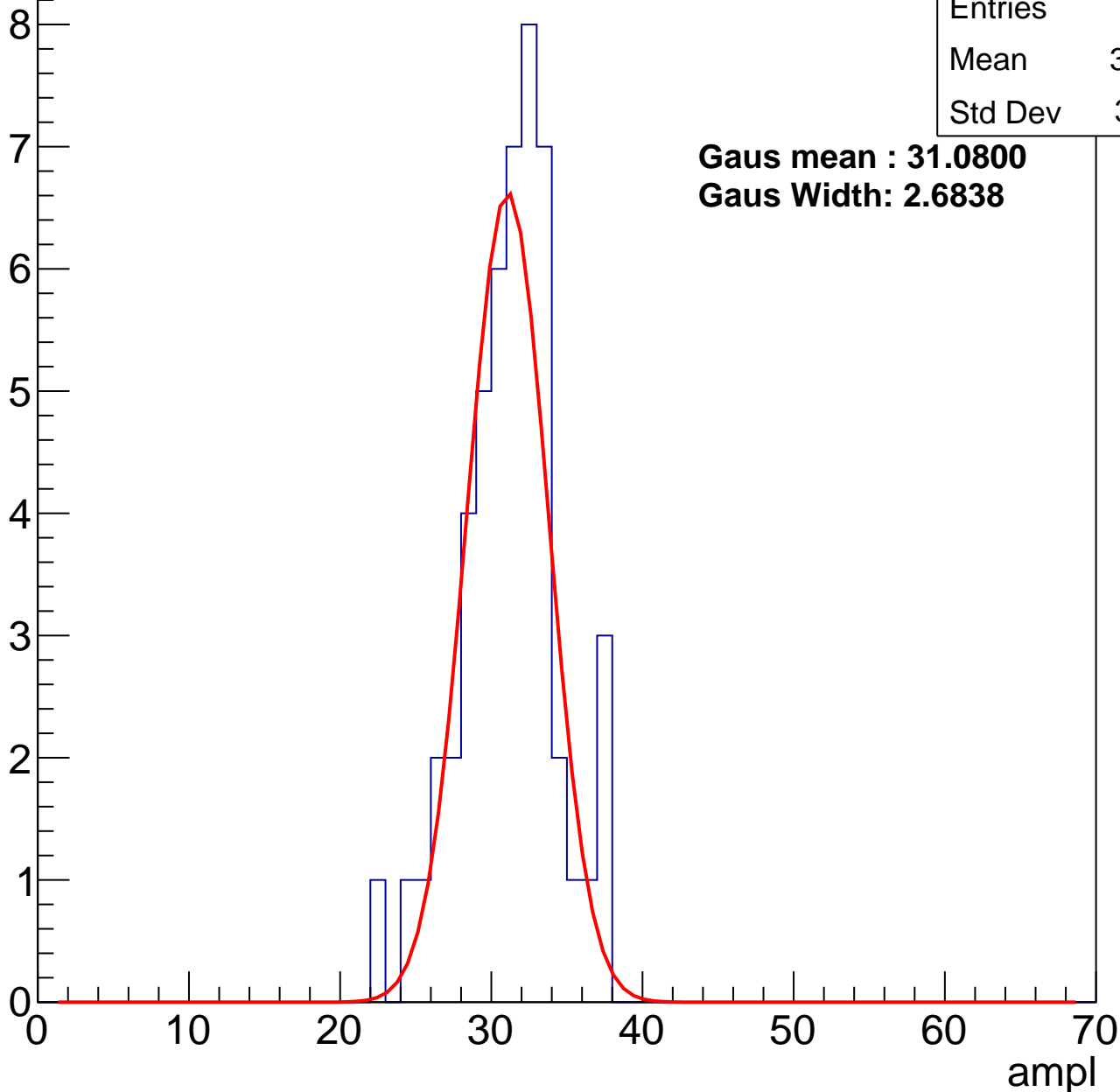
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	30.75
Std Dev	3.161

**Gaus mean : 31.0800**

**Gaus Width: 2.6838**



# B1L101S, U16-ch53, adc1

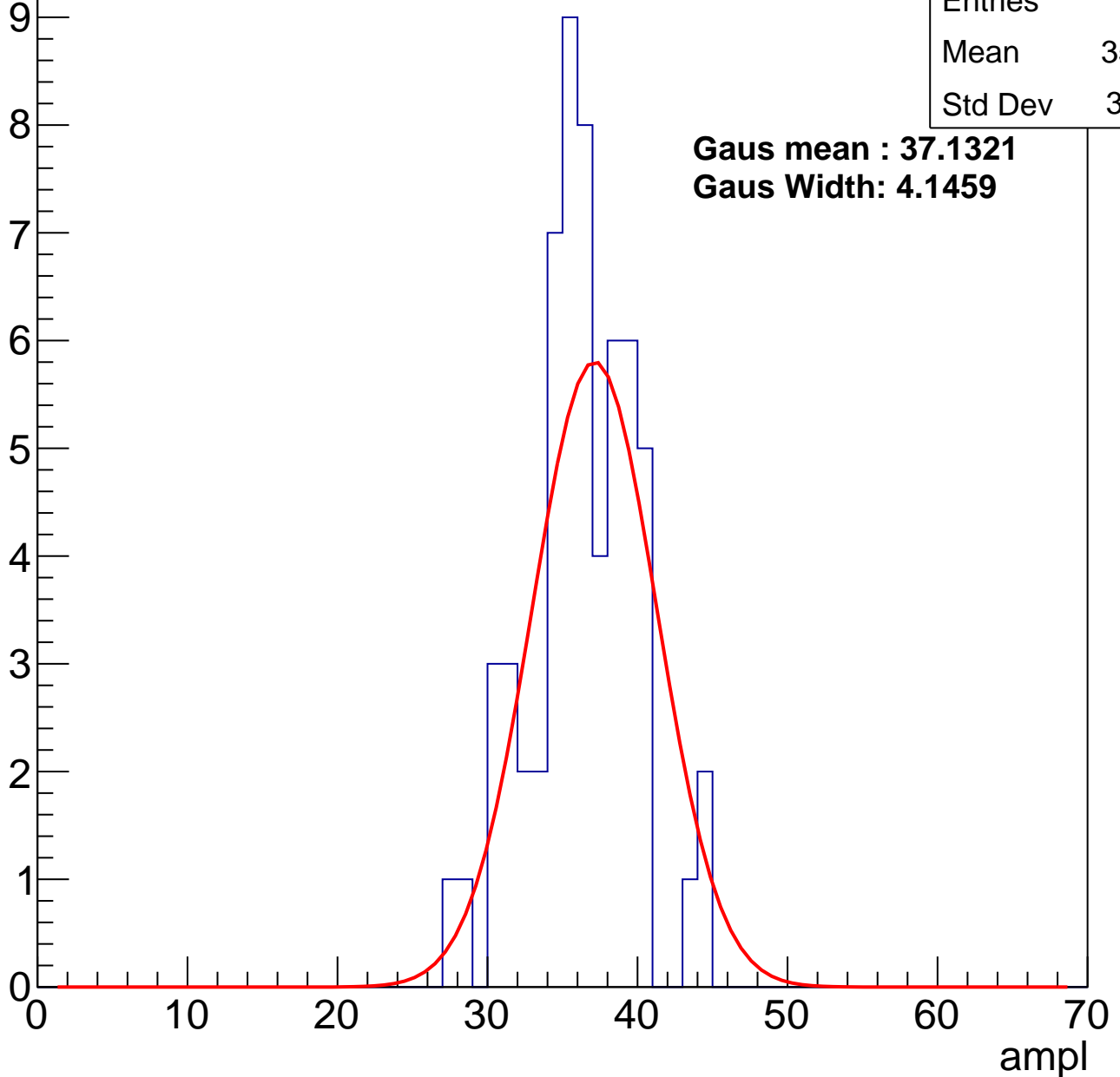
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	35.83
Std Dev	3.541

**Gaus mean : 37.1321**

**Gaus Width: 4.1459**



# B1L101S, U16-ch53, adc2

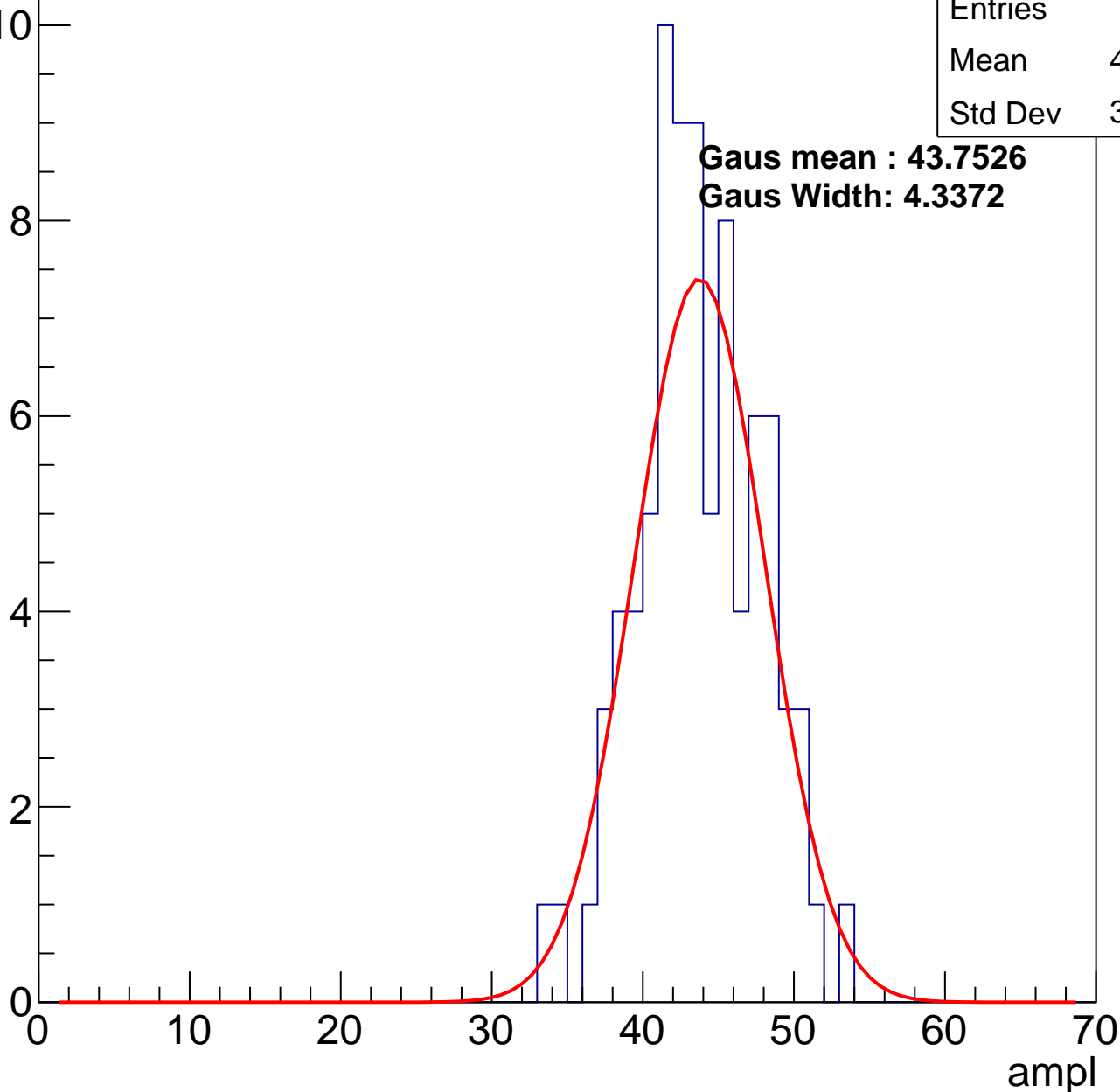
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	84
Mean	43.24
Std Dev	3.978

**Gaus mean : 43.7526**

**Gaus Width: 4.3372**

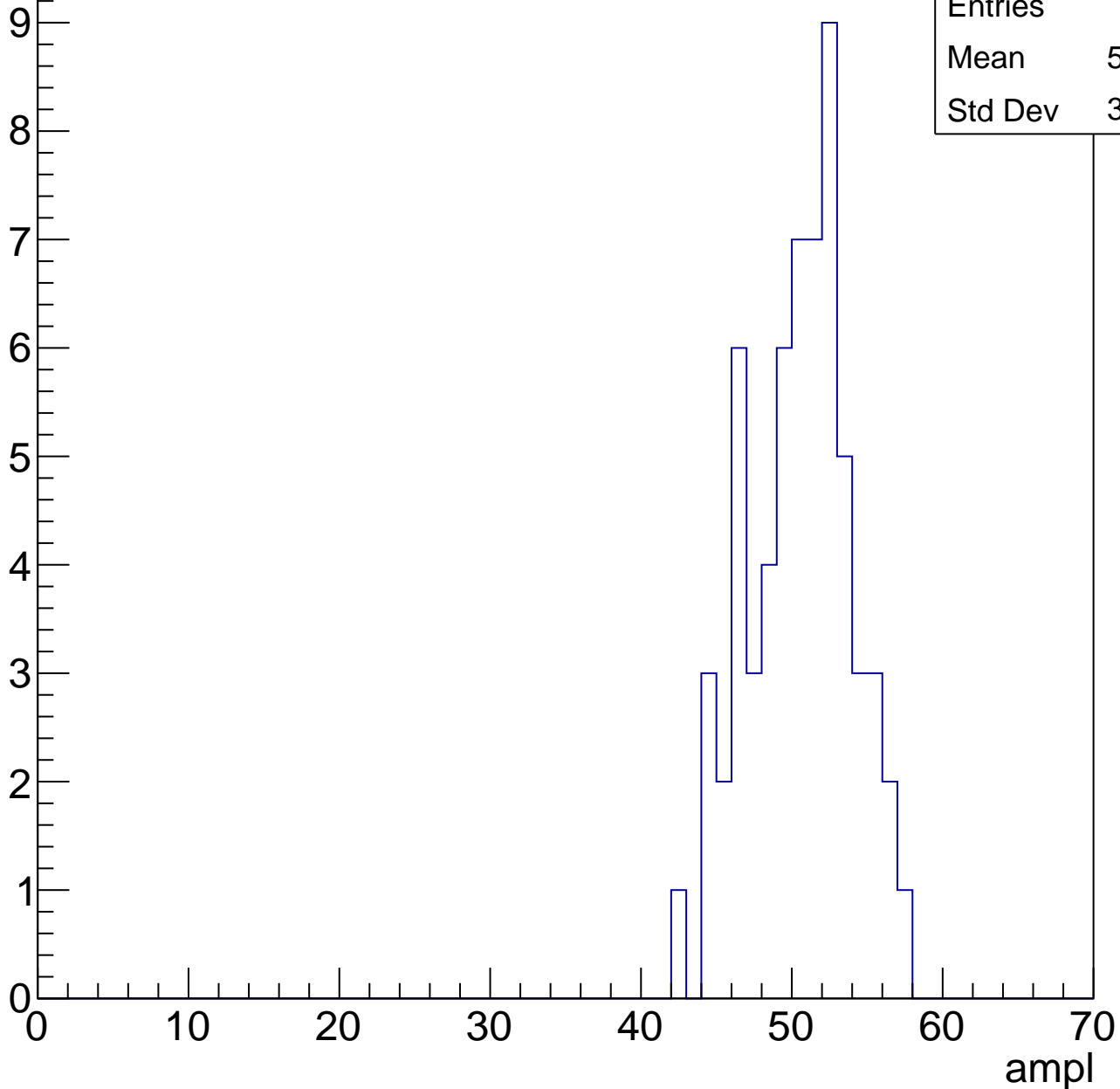


# B1L101S, U16-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	50.05
Std Dev	3.357

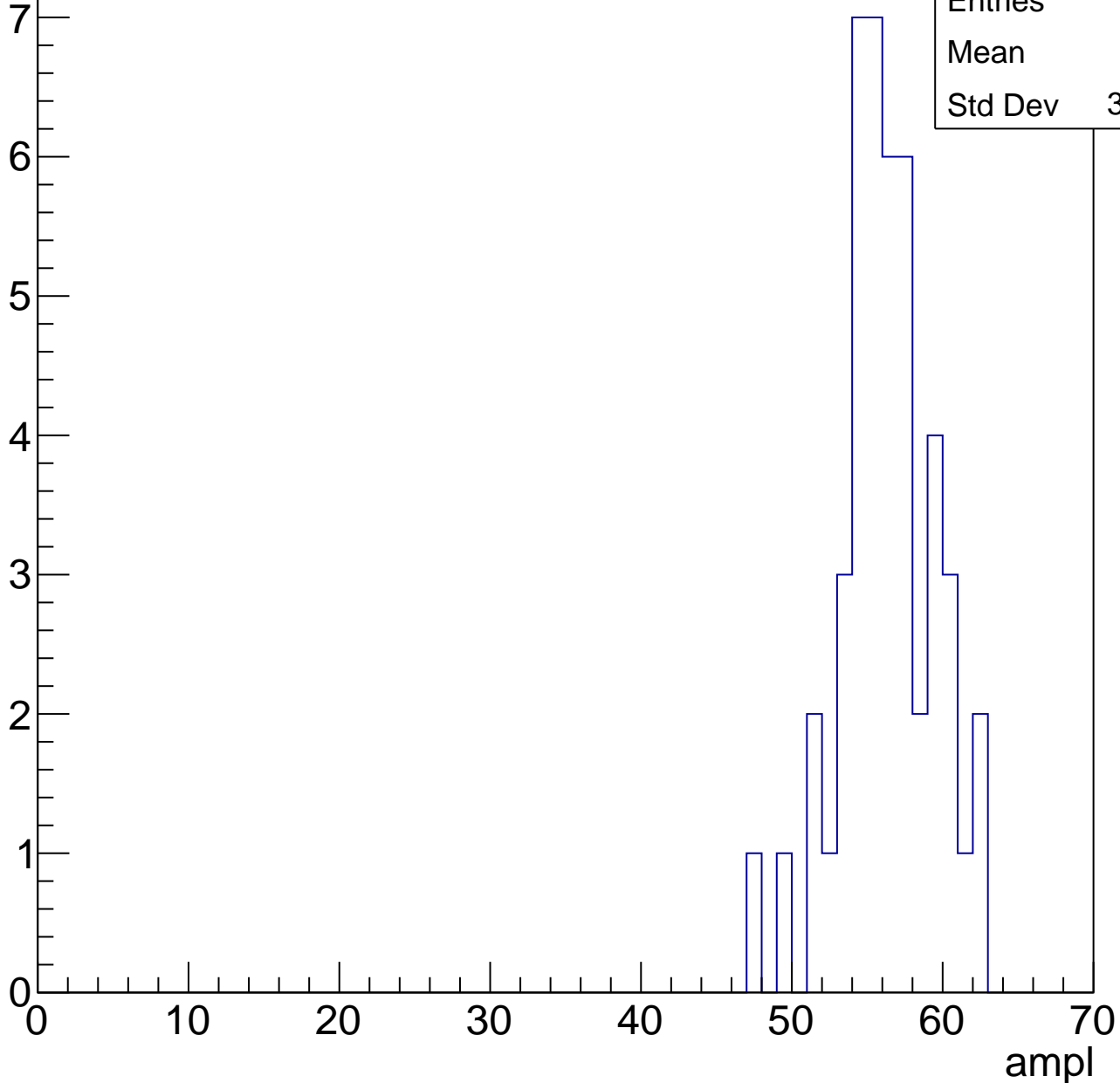


# B1L101S, U16-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

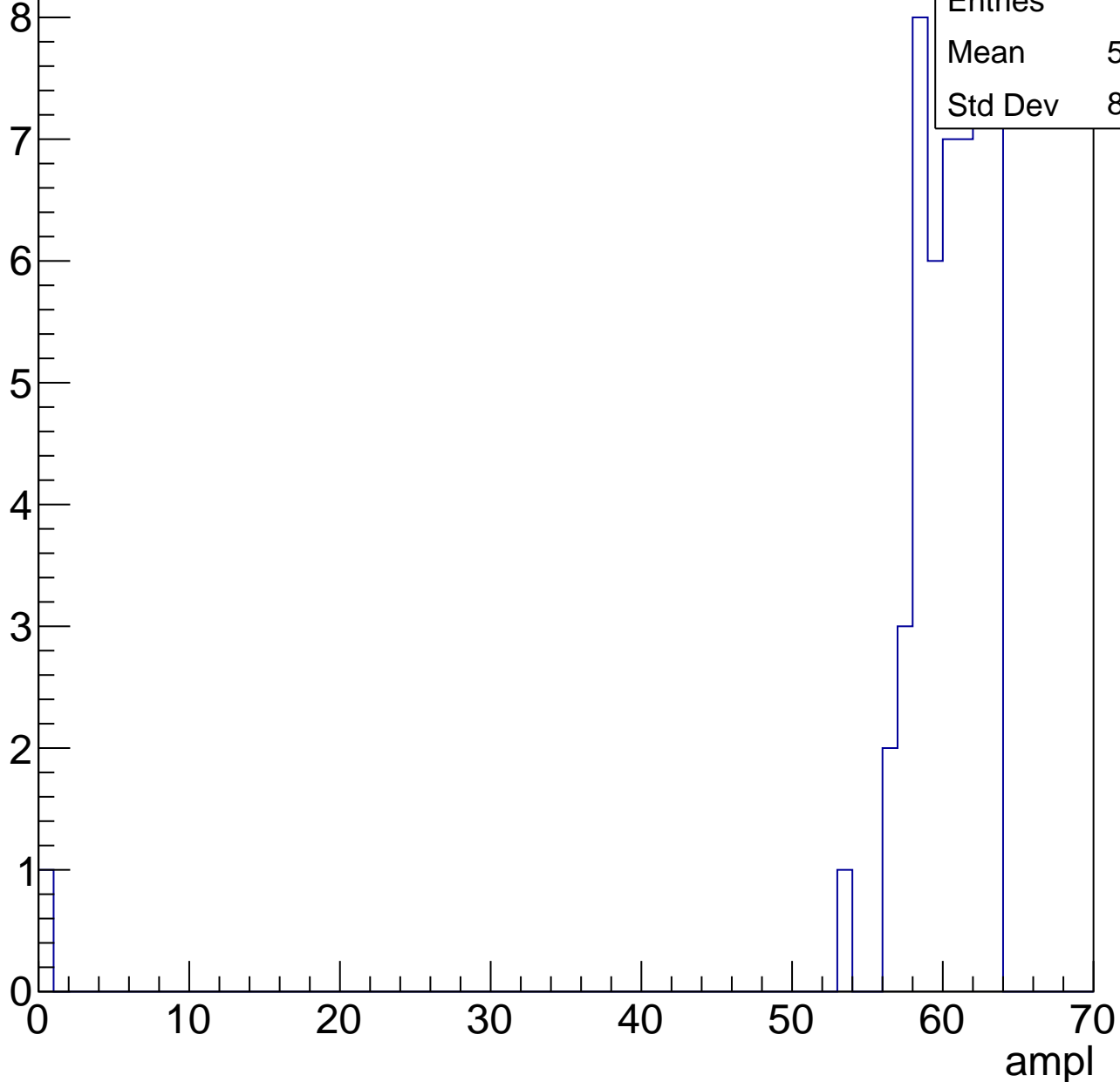
Entries	46
Mean	55.8
Std Dev	3.132



# B1L101S, U16-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

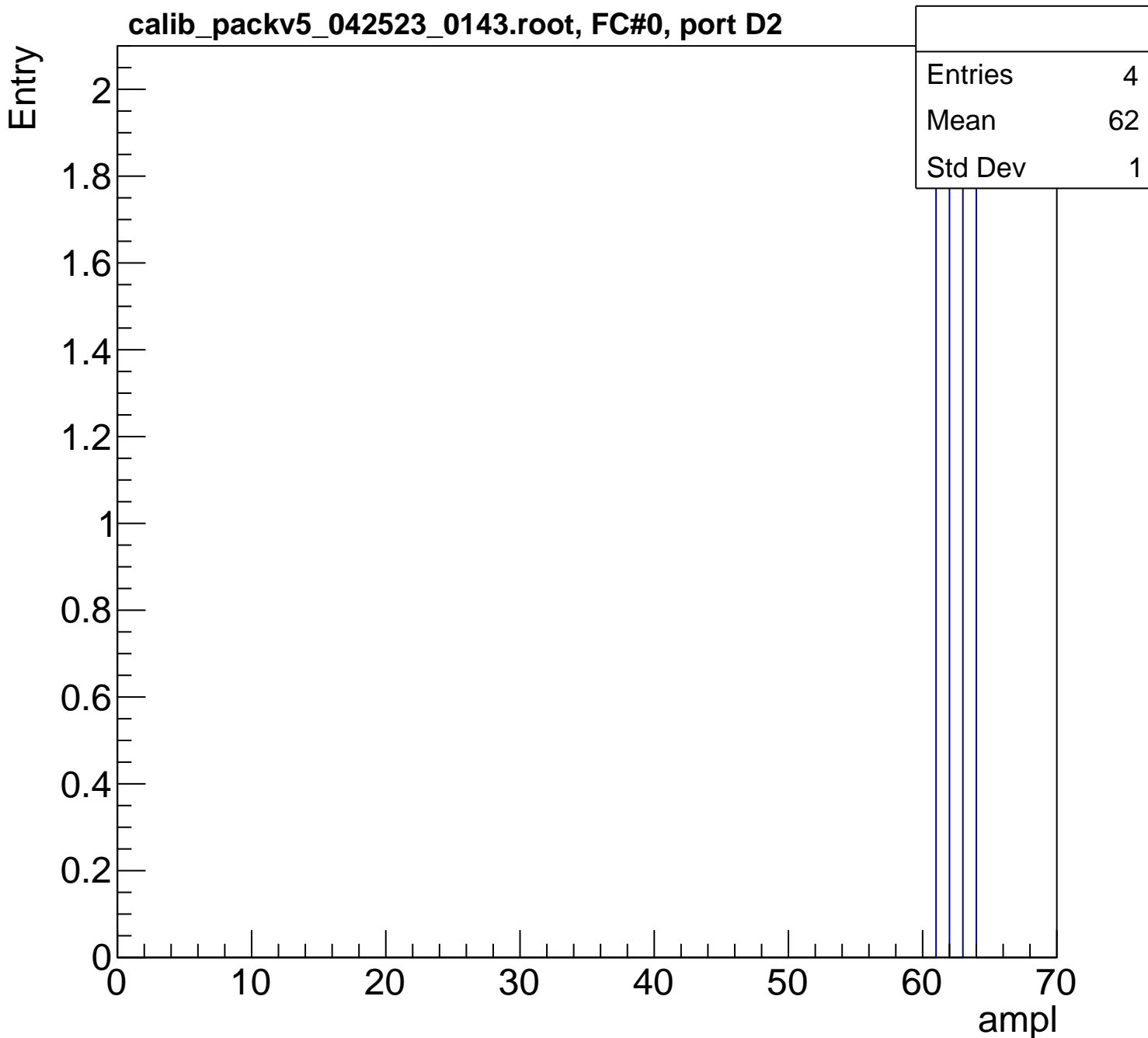
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	62
Std Dev	1

0 10 20 30 40 50 60 70

ampl





# B1L101S, U16-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U16-ch54, adc0

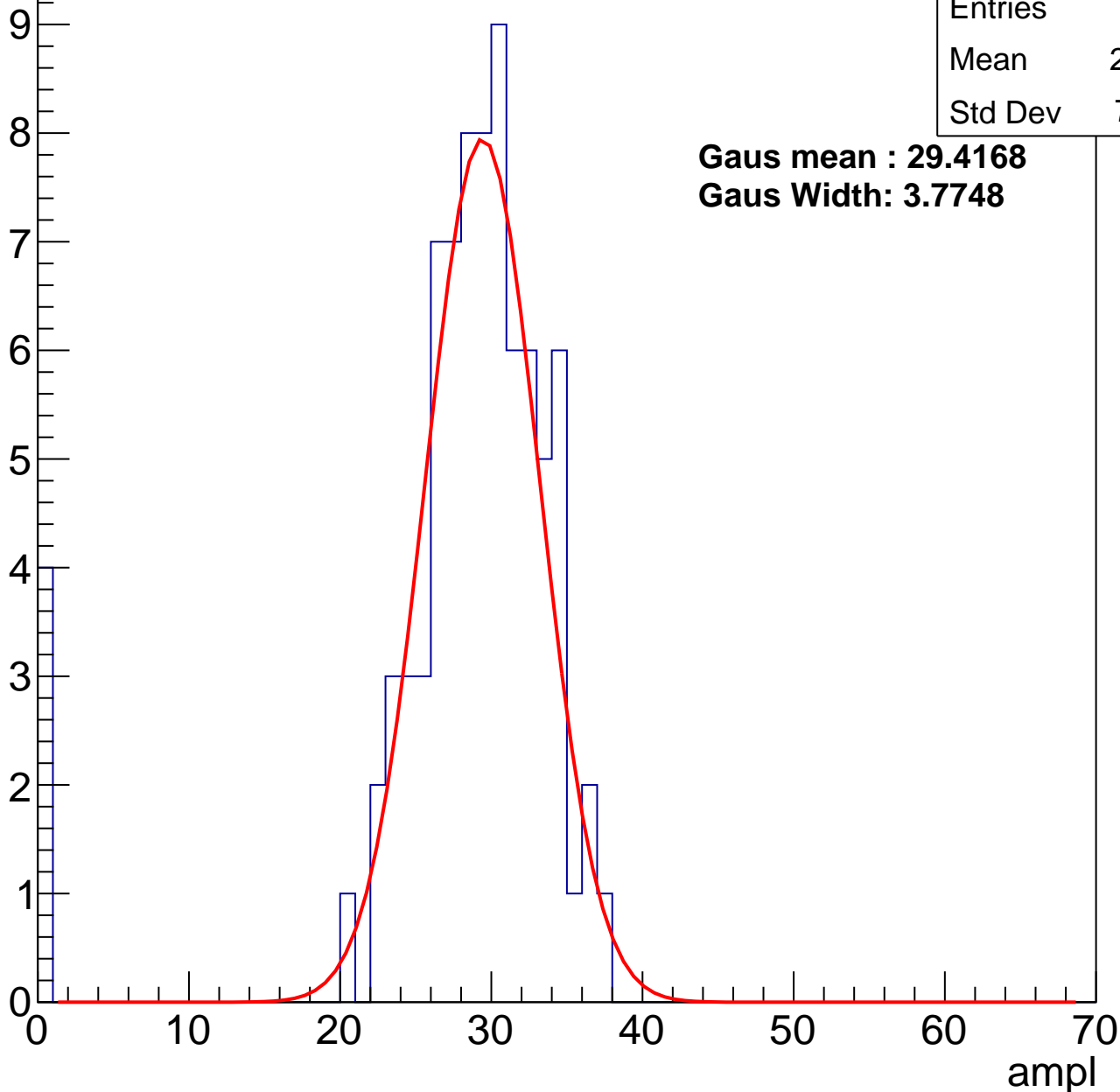
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	27.66
Std Dev	7.191

**Gaus mean : 29.4168**

**Gaus Width: 3.7748**



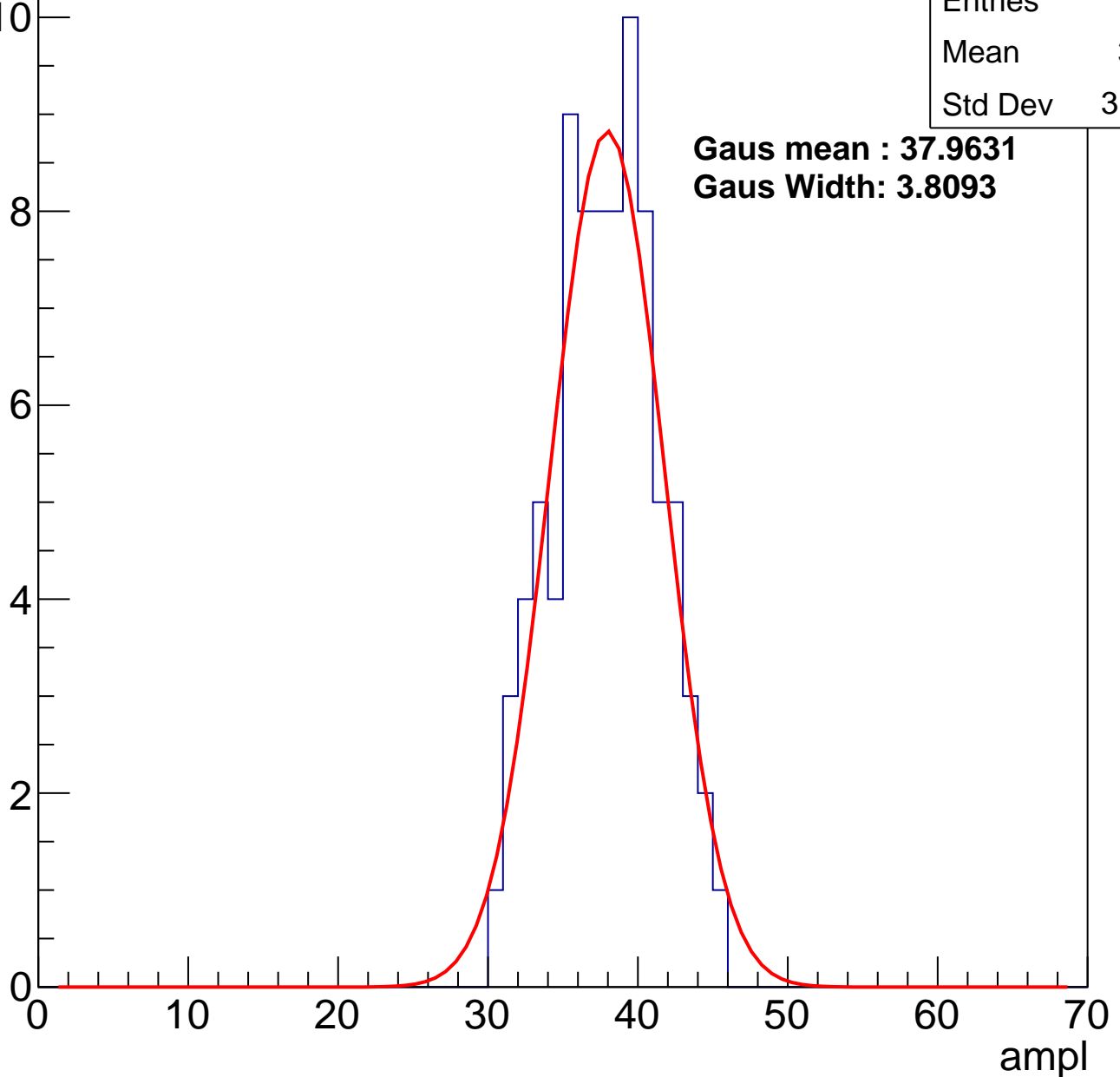
# B1L101S, U16-ch54, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	84
Mean	37.4
Std Dev	3.447

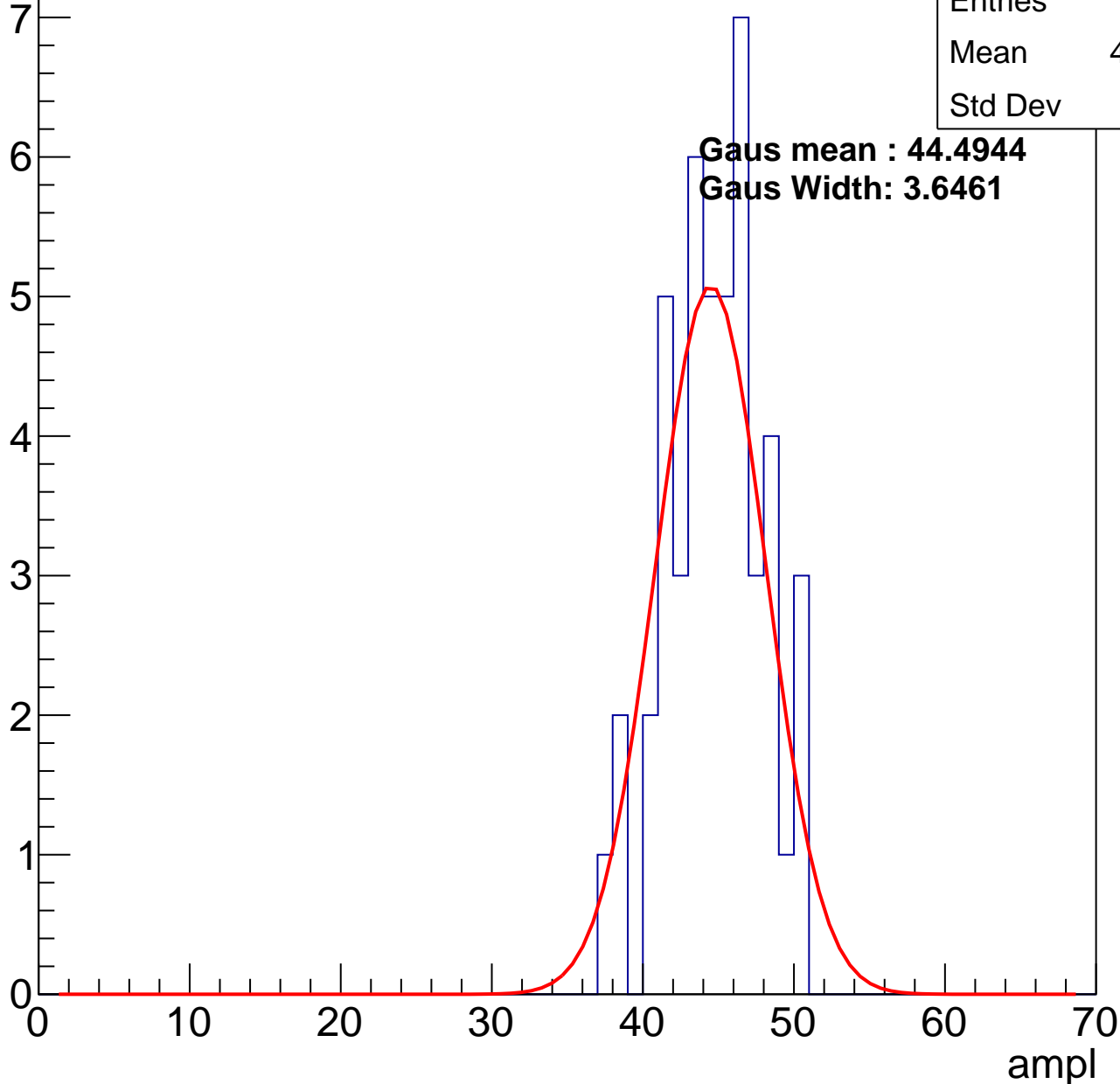
**Gaus mean : 37.9631**  
**Gaus Width: 3.8093**



# B1L101S, U16-ch54, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

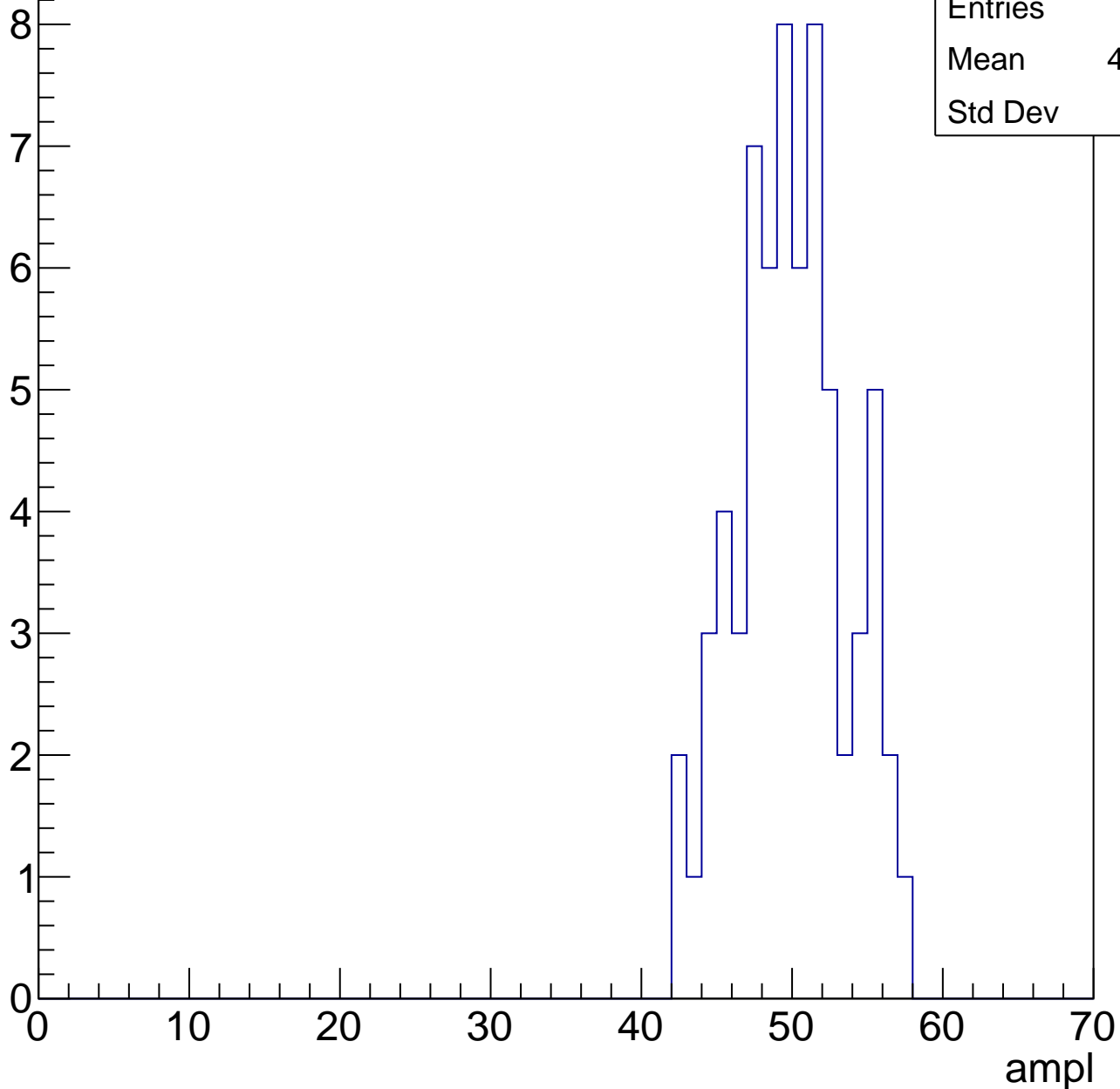
Entry



# B1L101S, U16-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



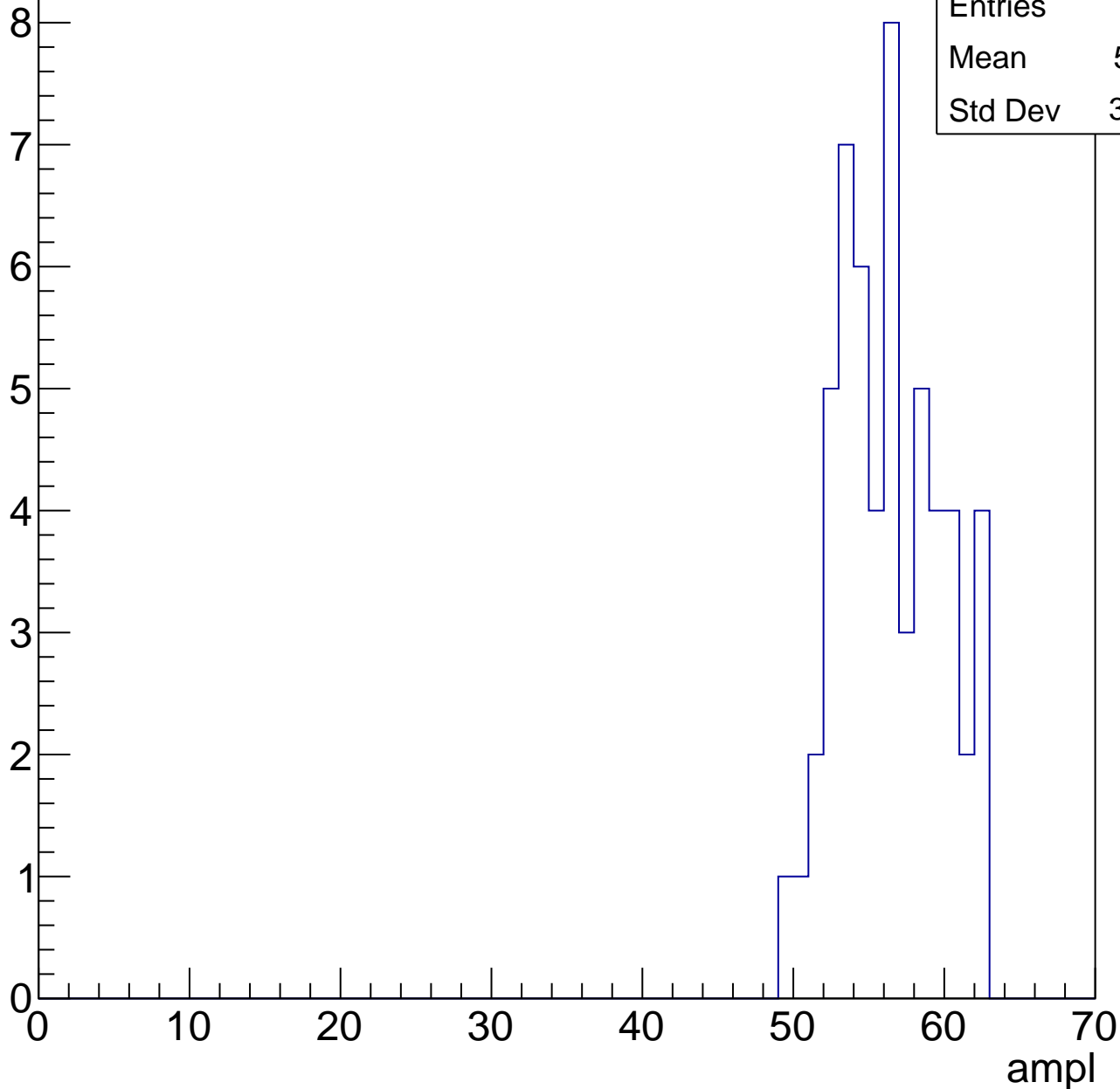
Entries	66
Mean	49.48
Std Dev	3.59

# B1L101S, U16-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	55.91
Std Dev	3.334

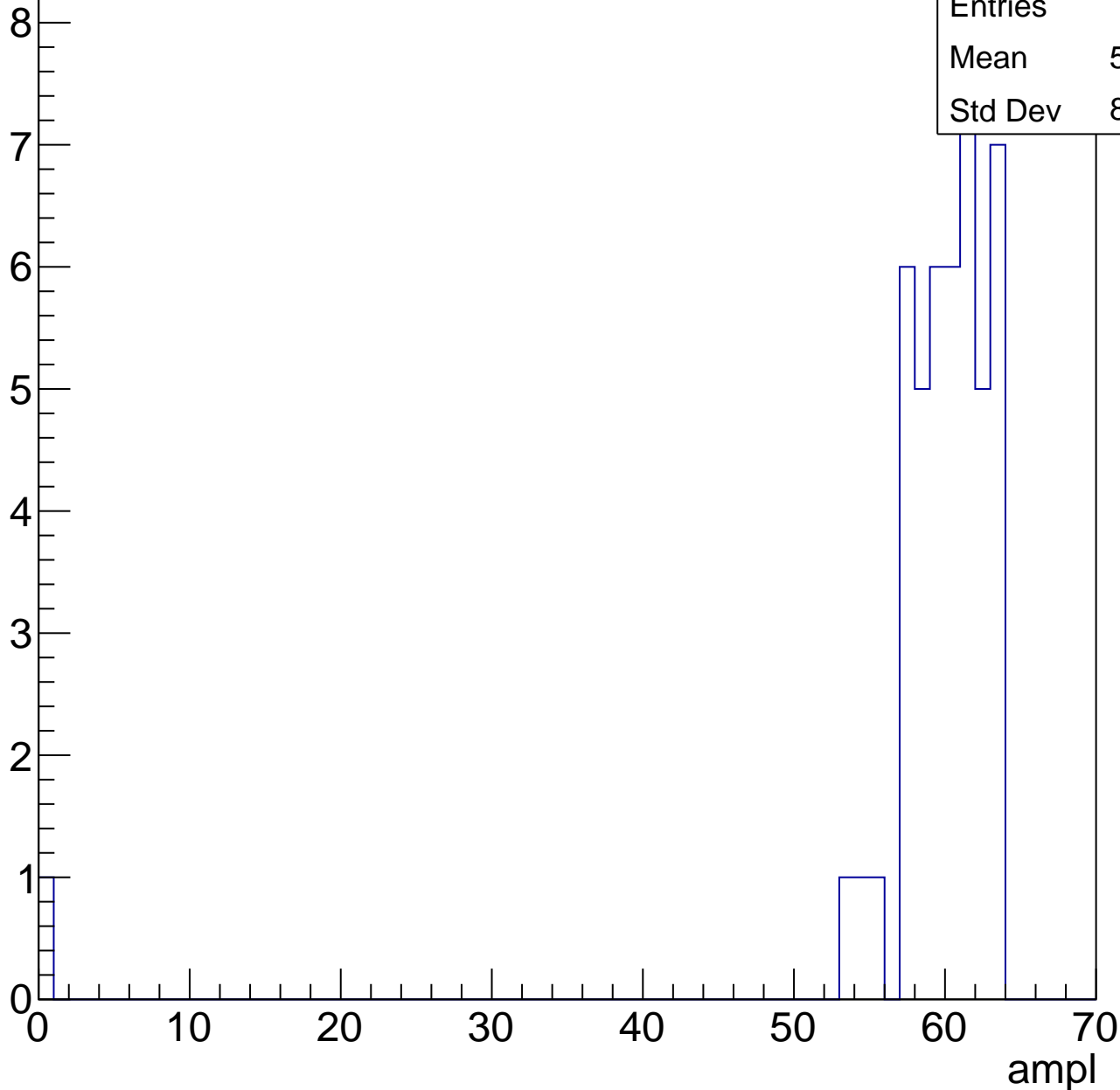


# B1L101S, U16-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	58.45
Std Dev	8.953



# B1L101S, U16-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U16-ch55, adc0

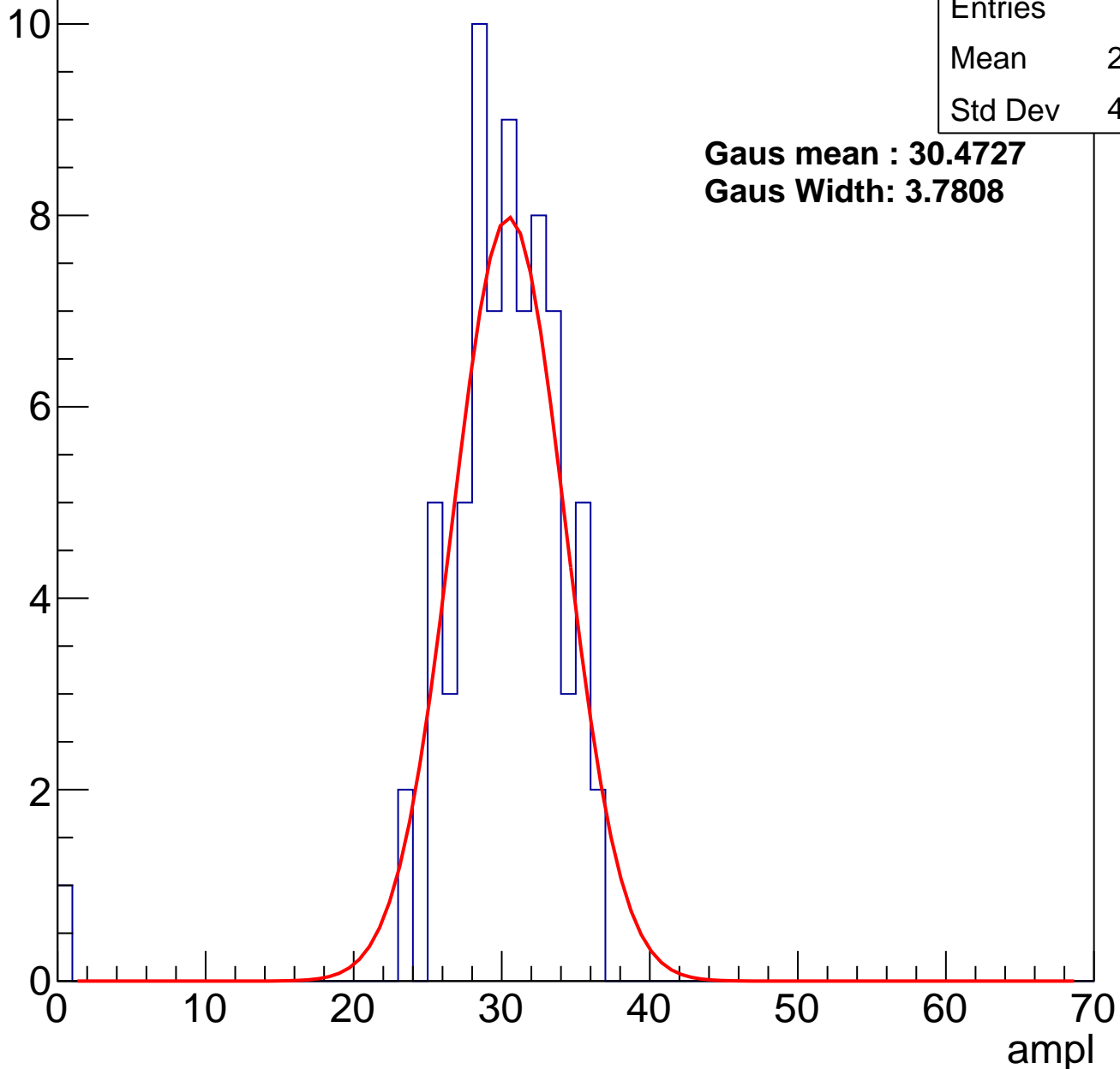
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	74
Mean	29.59
Std Dev	4.647

**Gaus mean : 30.4727**

**Gaus Width: 3.7808**

Entry



# B1L101S, U16-ch55, adc1

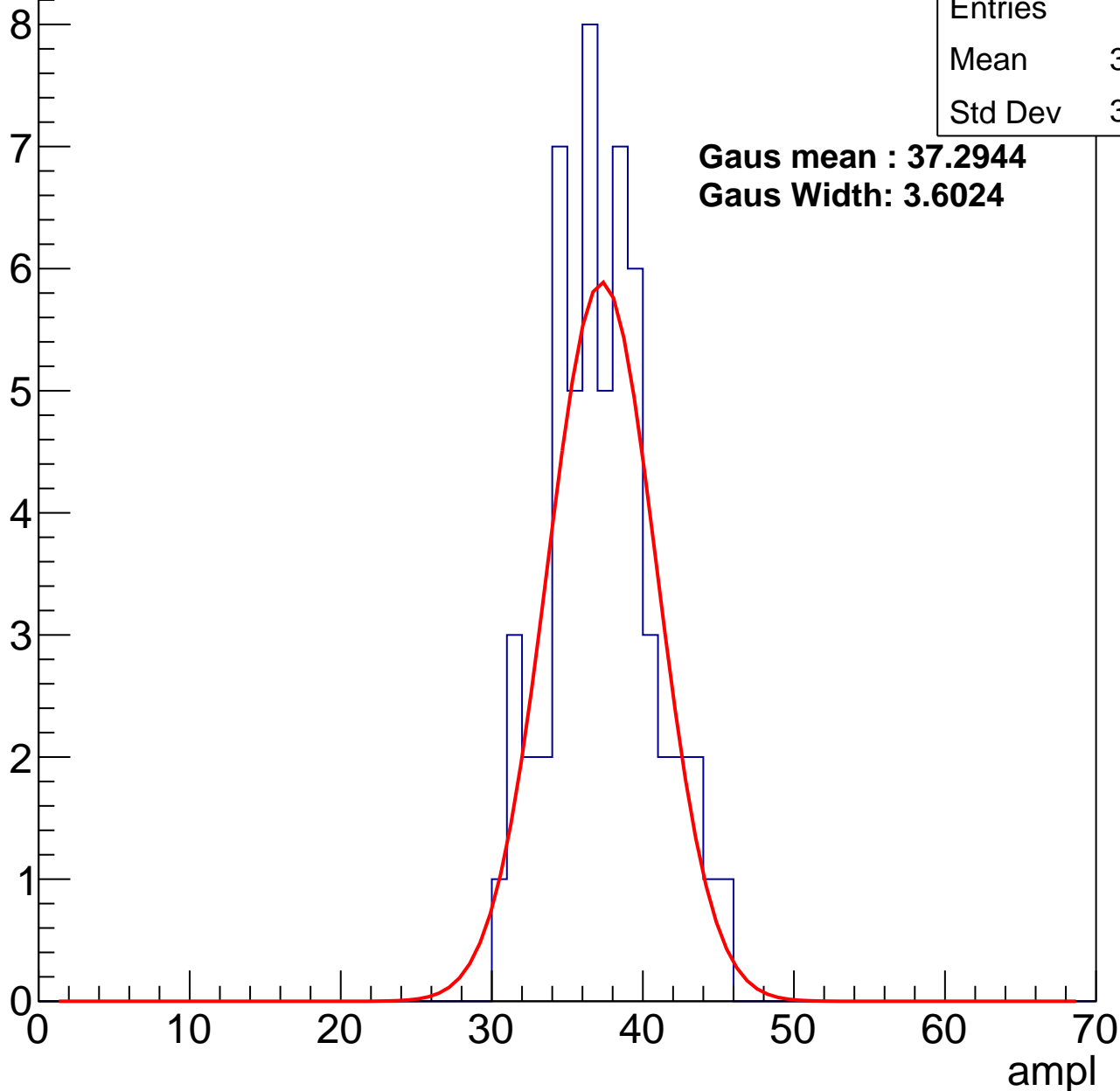
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	36.84
Std Dev	3.386

**Gaus mean : 37.2944**

**Gaus Width: 3.6024**



# B1L101S, U16-ch55, adc2

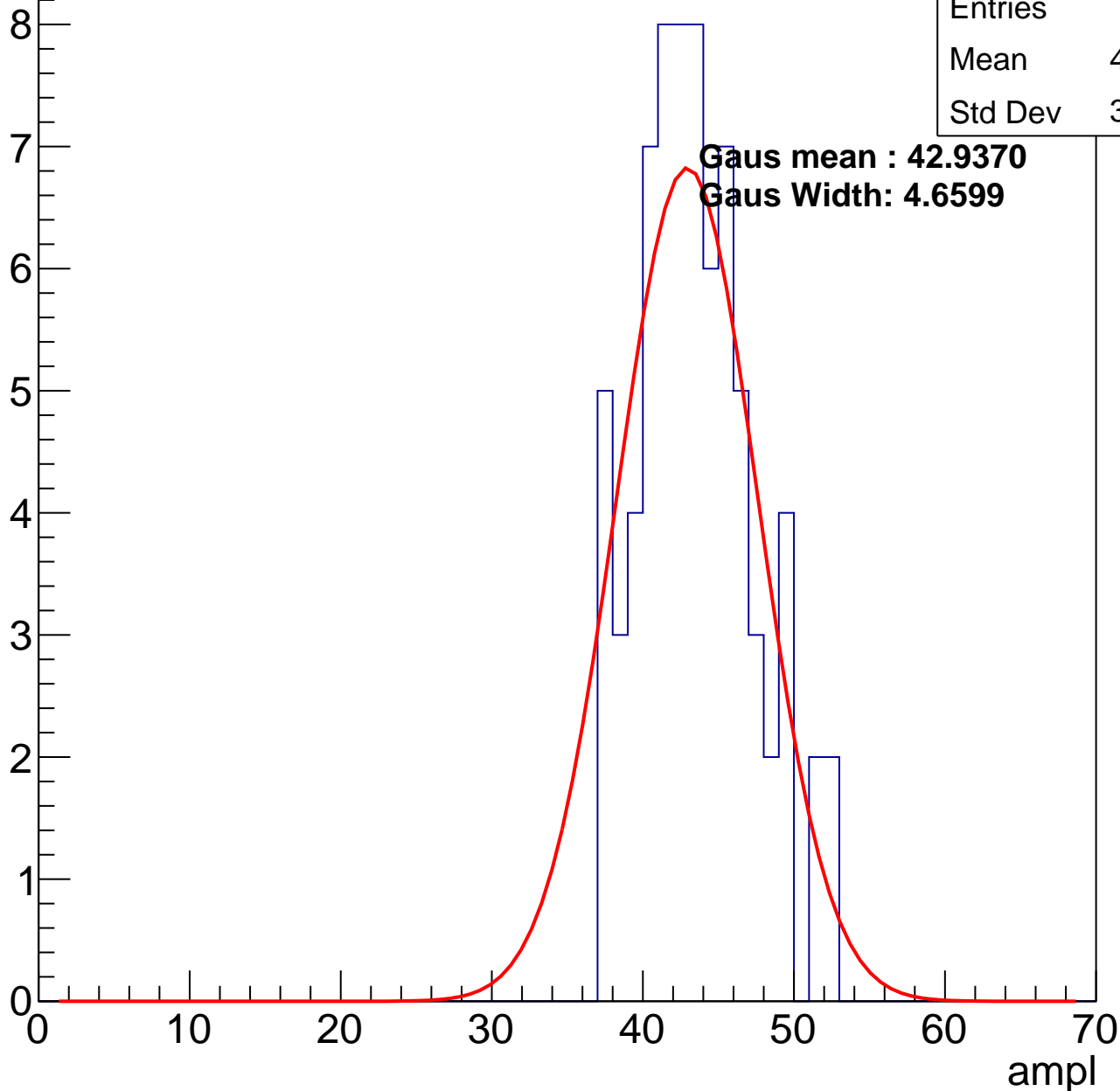
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	43.12
Std Dev	3.734

**Gaus mean : 42.9370**

**Gaus Width: 4.6599**

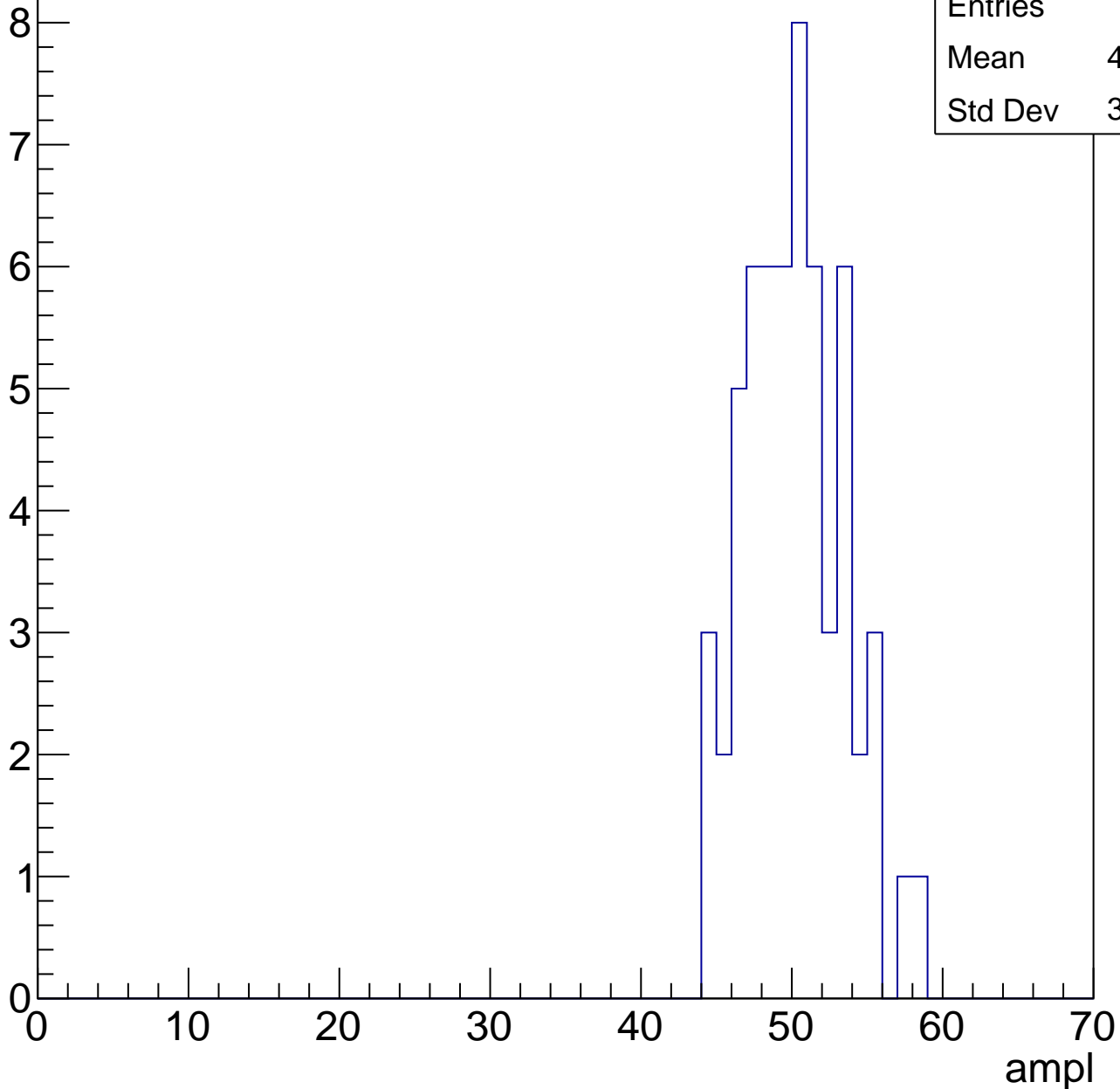


# B1L101S, U16-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	49.72
Std Dev	3.242

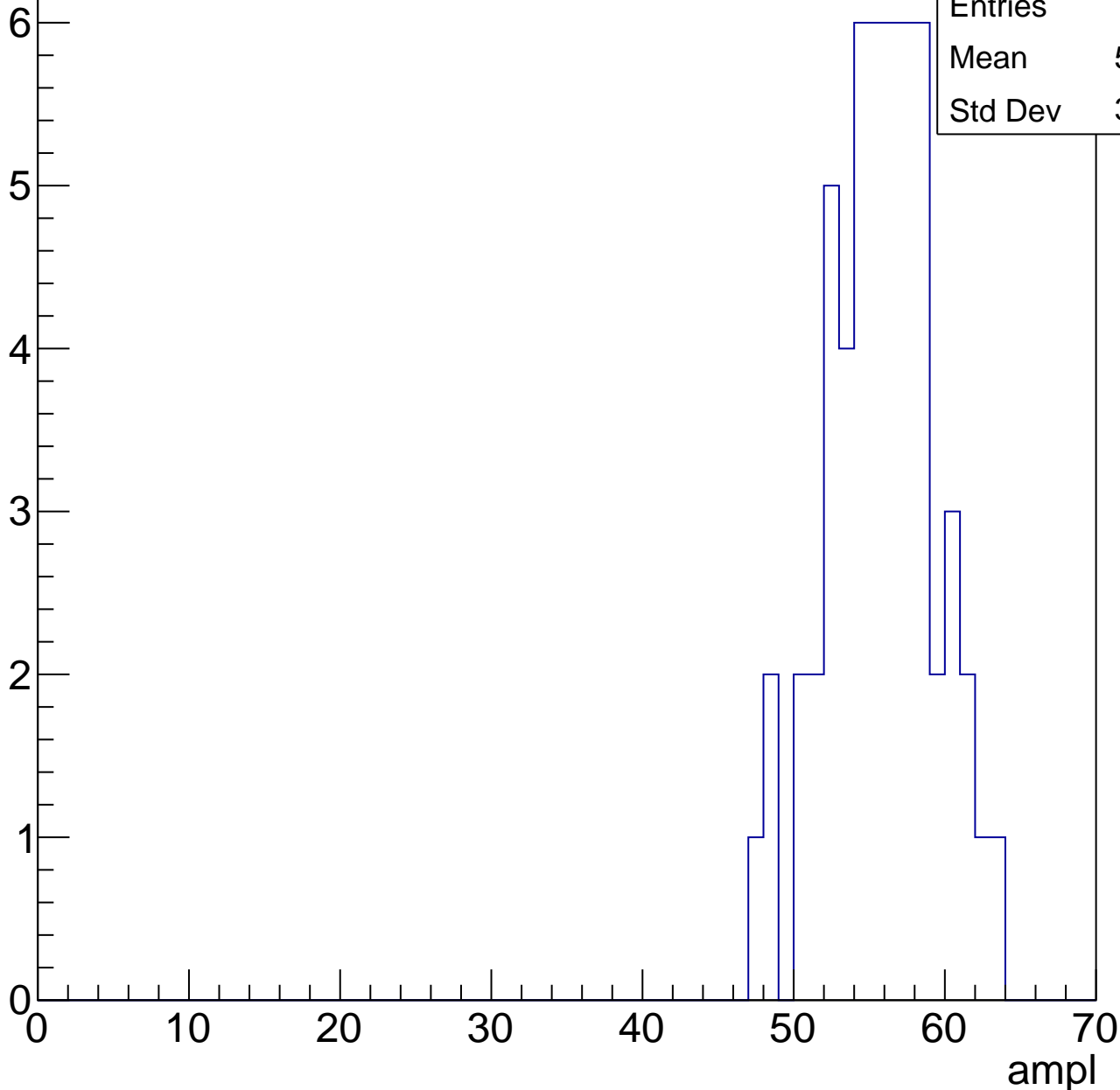


# B1L101S, U16-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	55.31
Std Dev	3.521

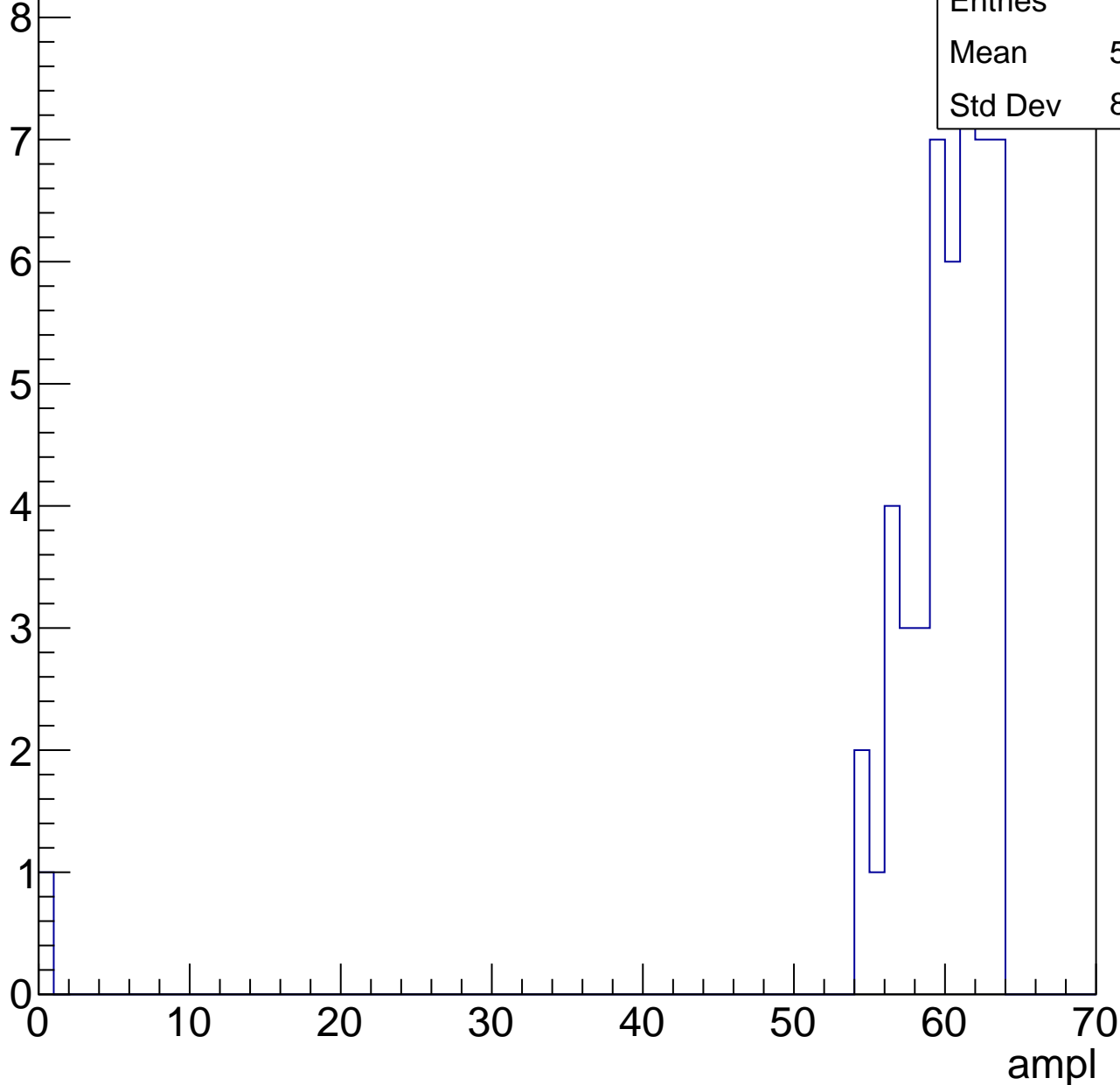


# B1L101S, U16-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

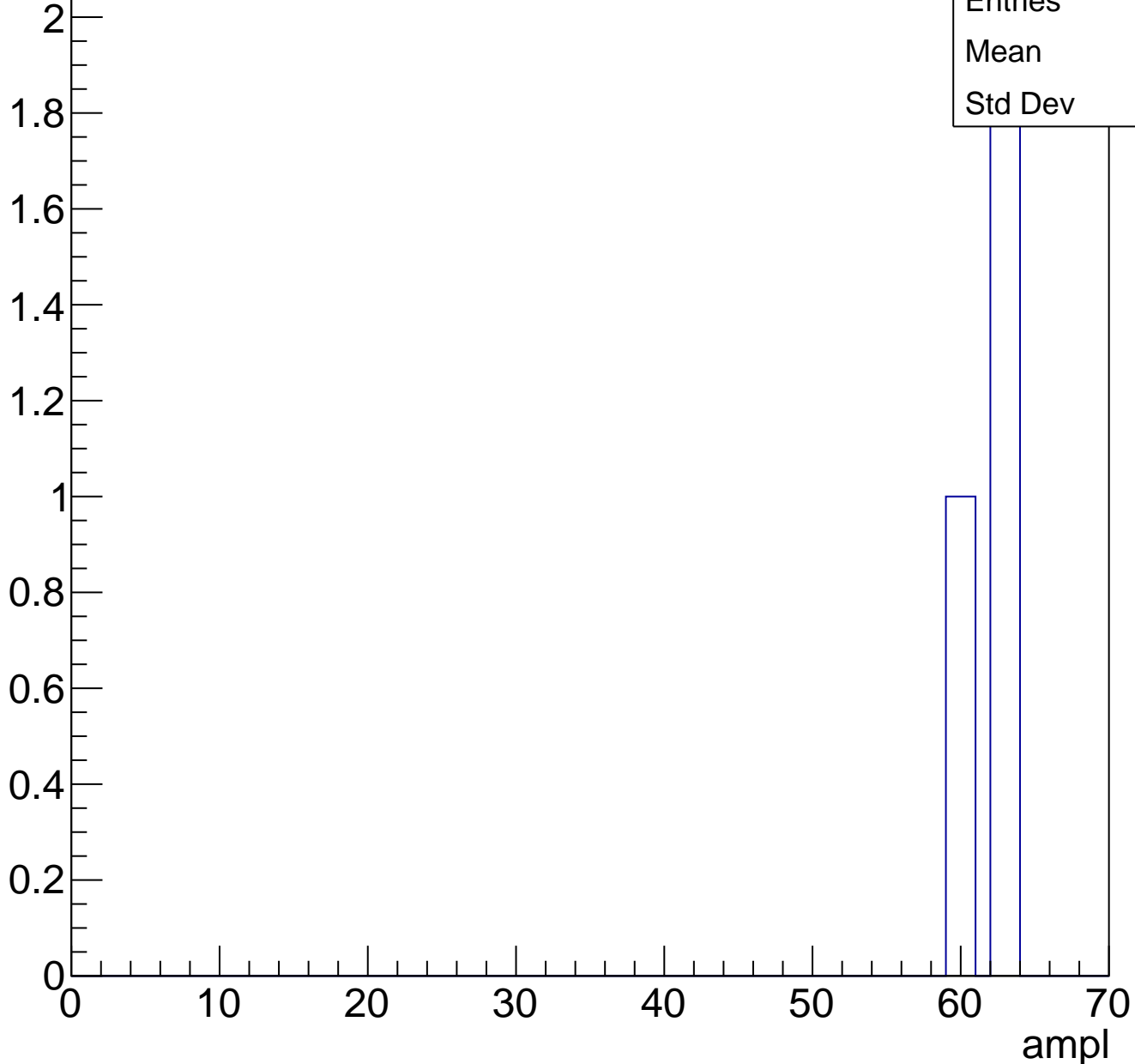
Entries	49
Mean	58.53
Std Dev	8.807



# B1L101S, U16-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

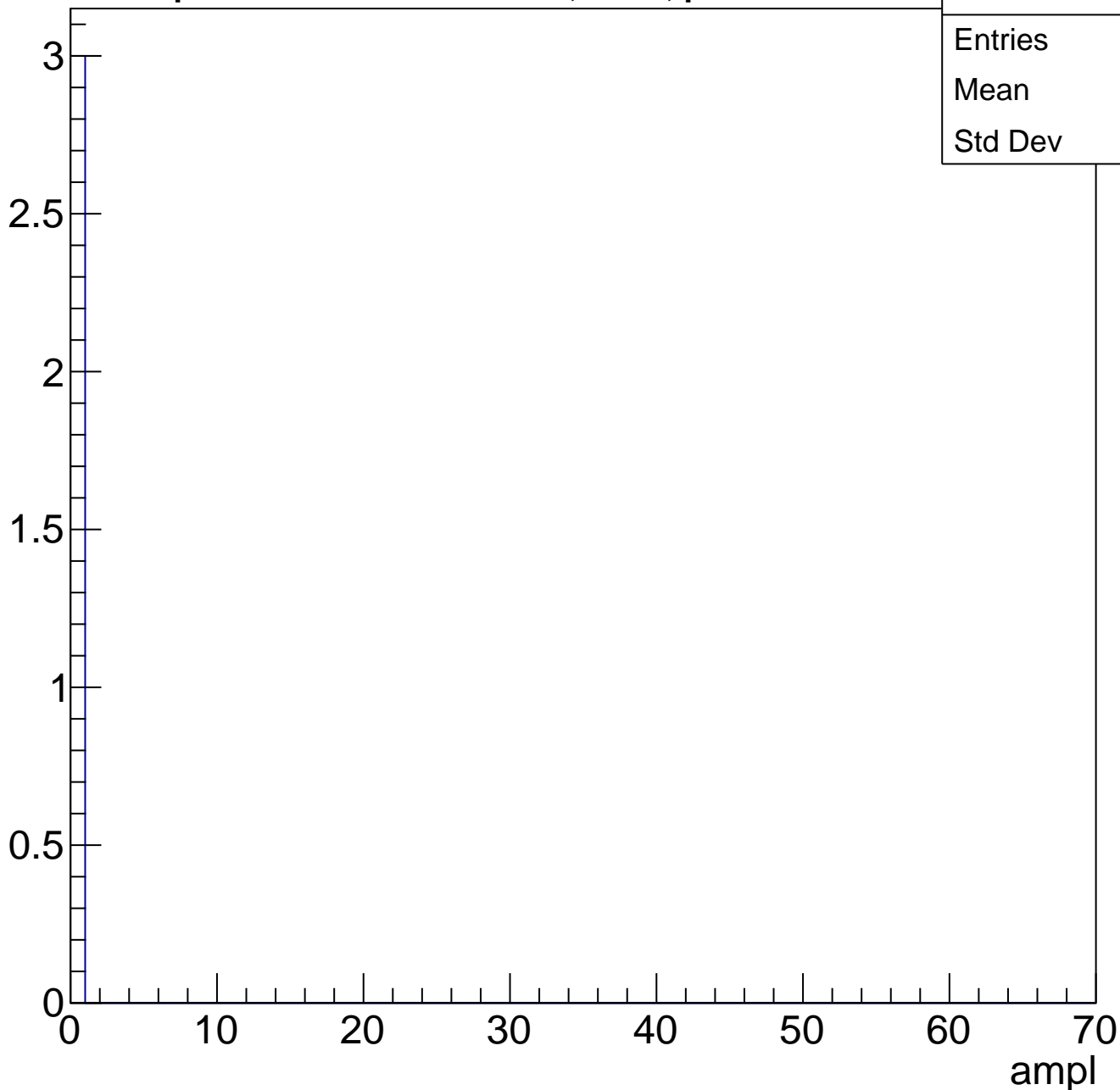




# B1L101S, U16-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U16-ch56, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	75
Mean	28.32
Std Dev	3.601

**Gaus mean : 29.0781**

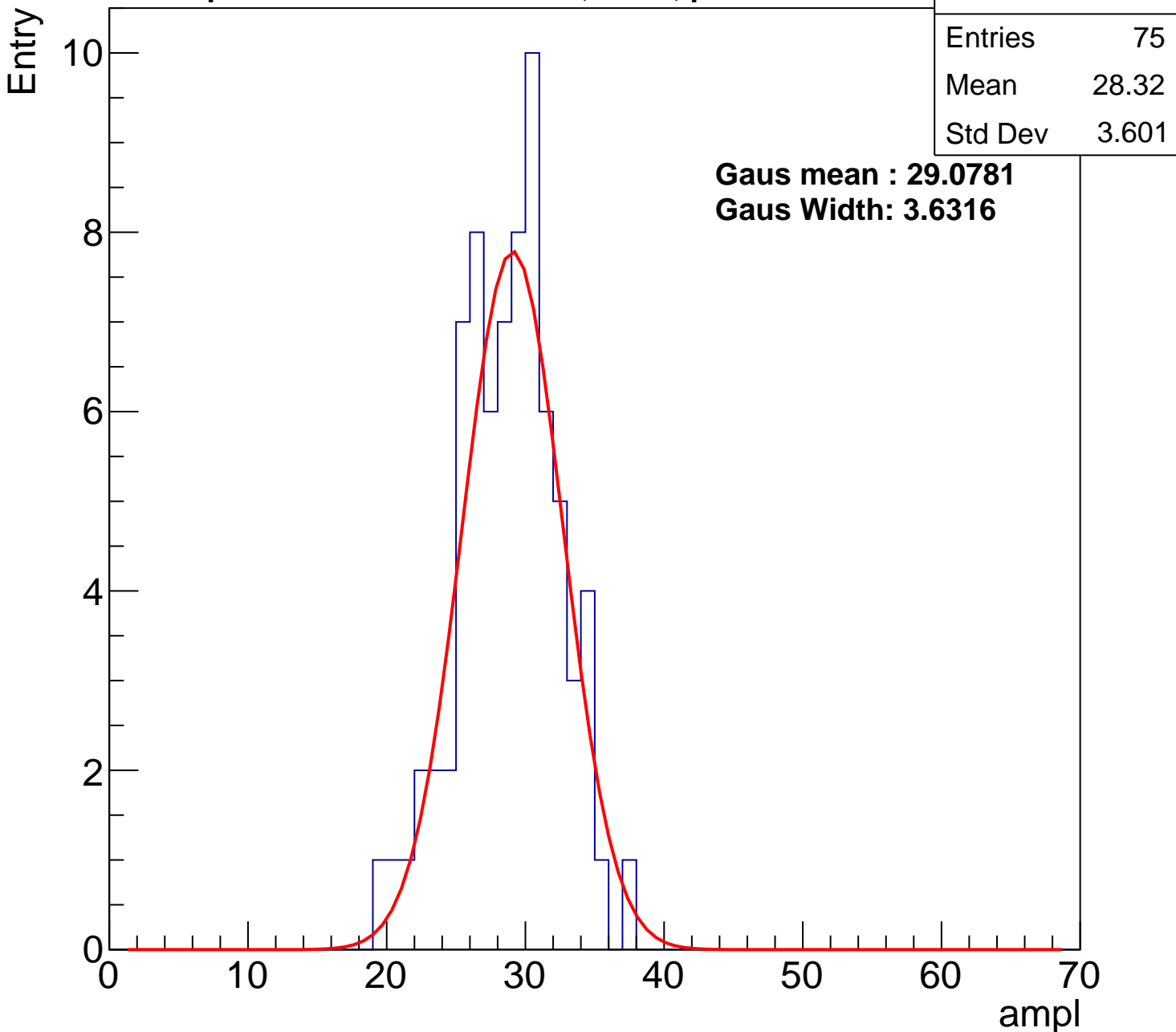
**Gaus Width: 3.6316**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch56, adc1

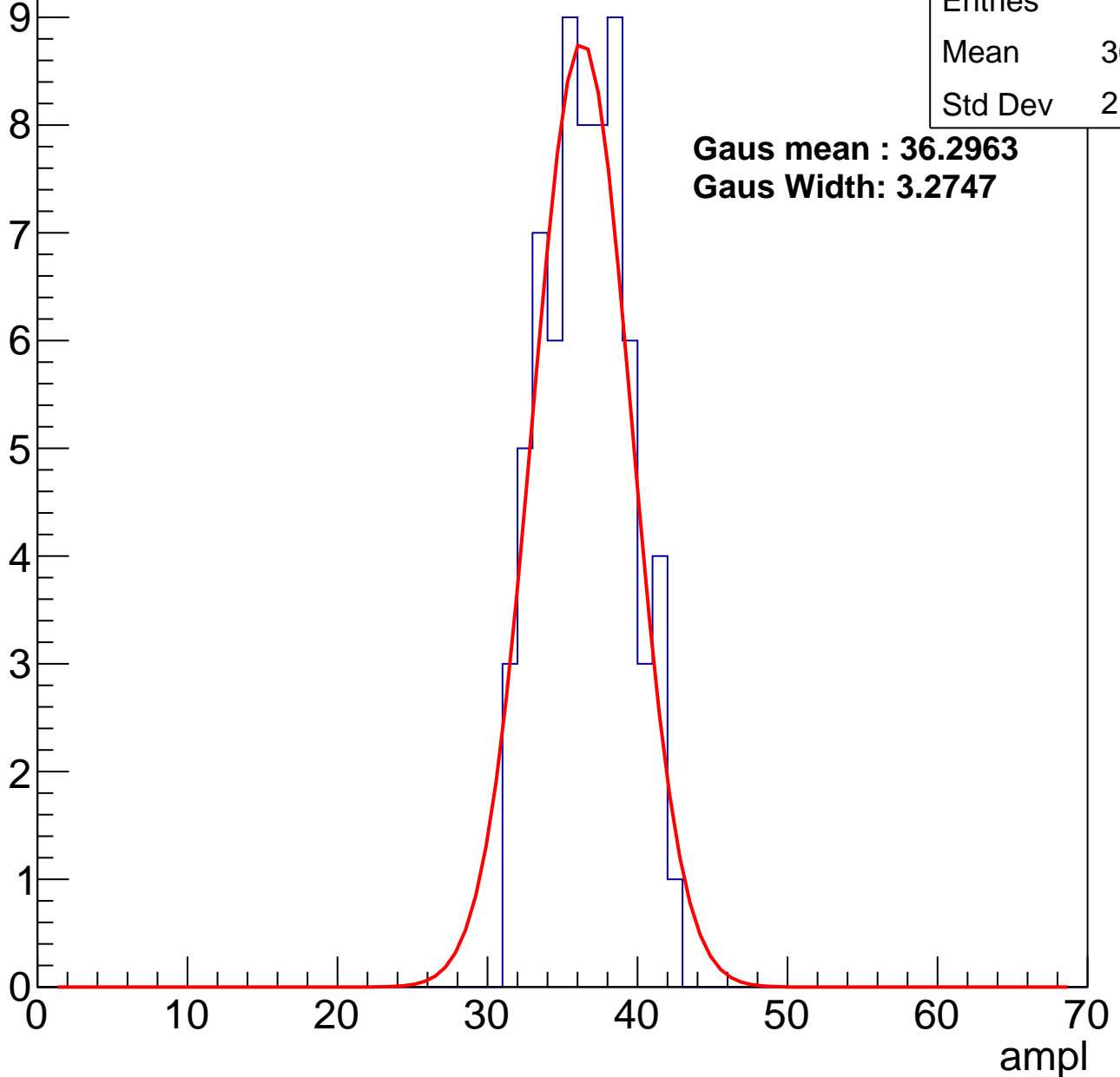
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	36.07
Std Dev	2.778

**Gaus mean : 36.2963**

**Gaus Width: 3.2747**



# B1L101S, U16-ch56, adc2

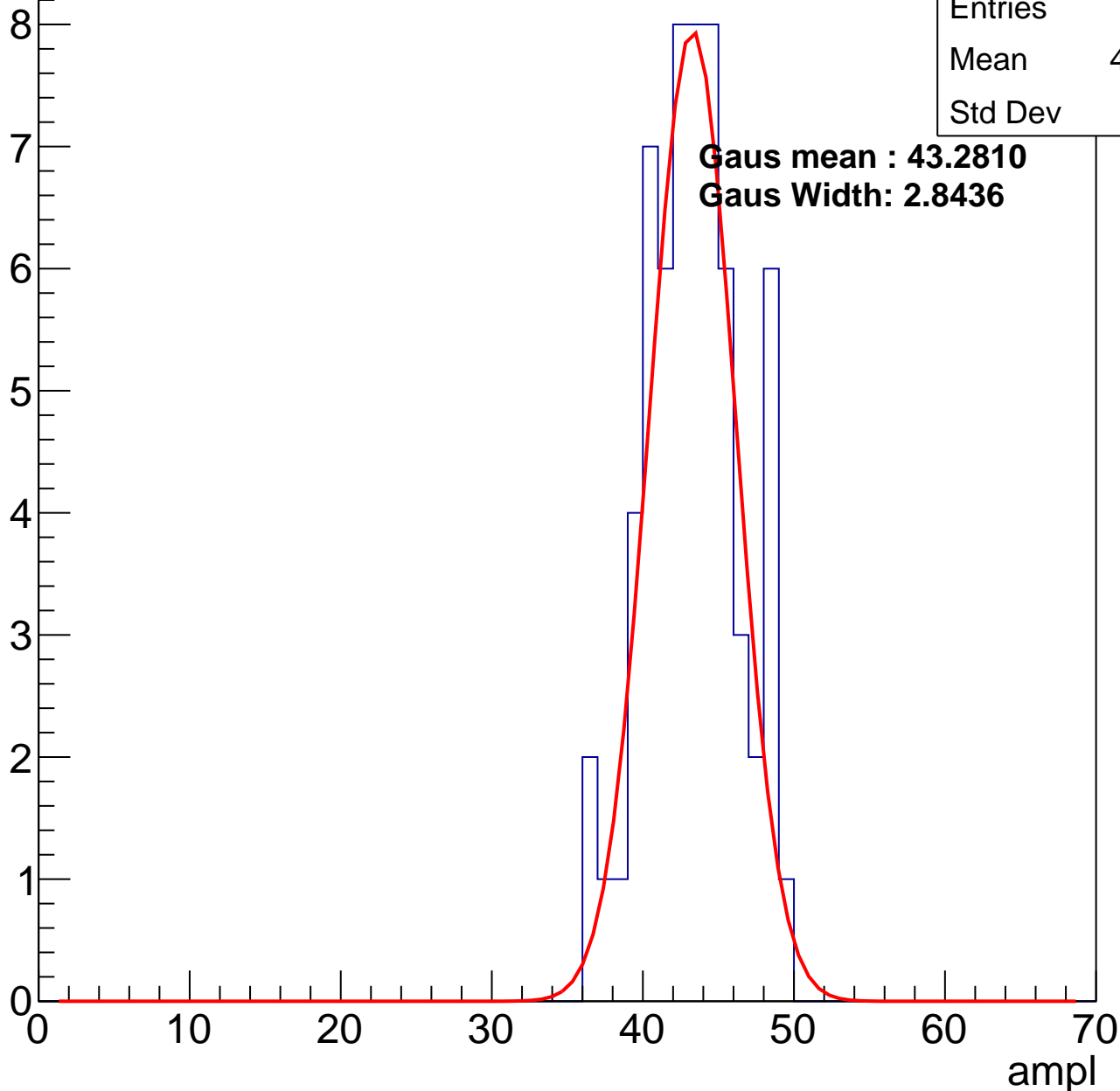
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	42.86
Std Dev	3.07

**Gaus mean : 43.2810**

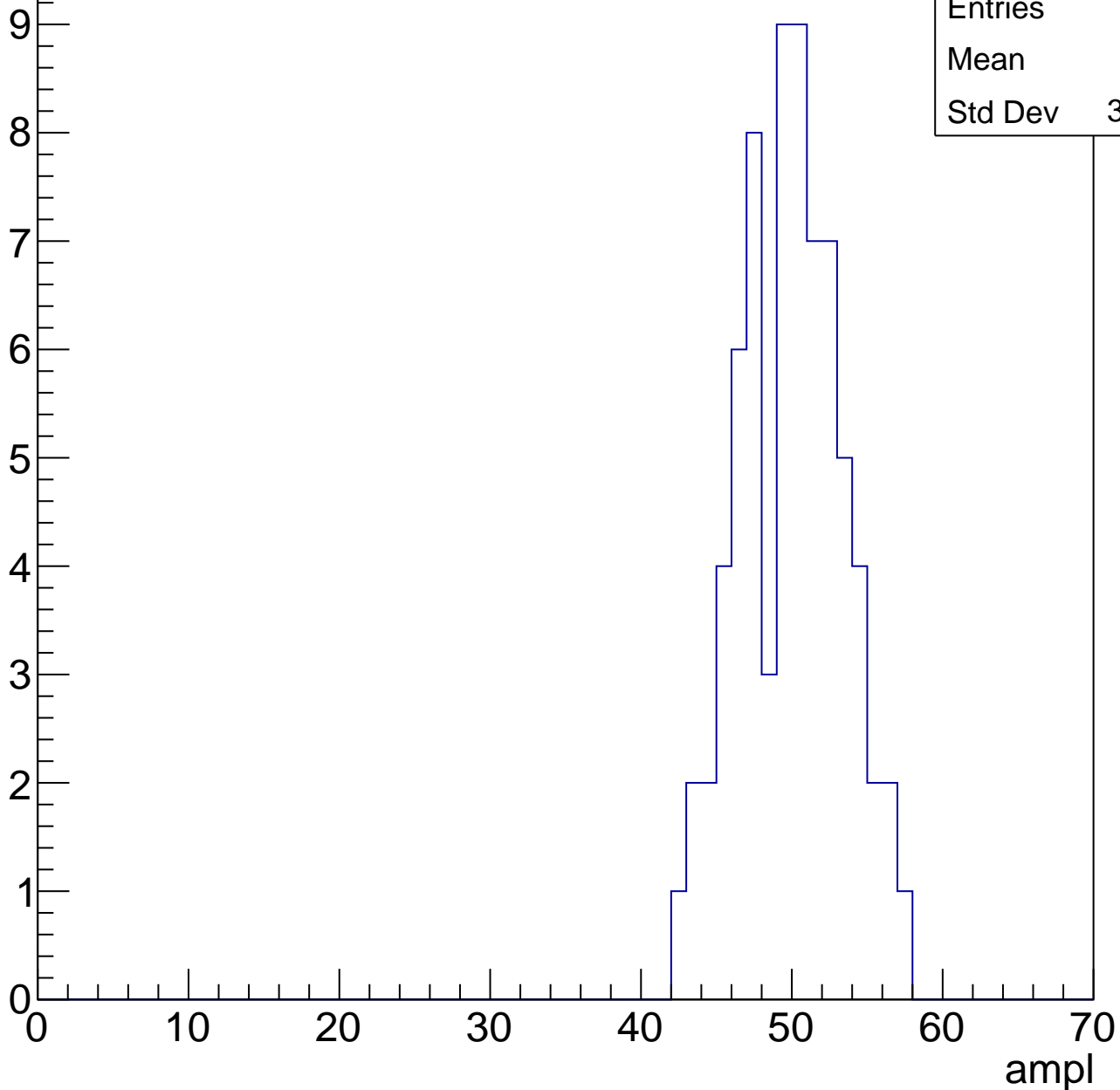
**Gaus Width: 2.8436**



# B1L101S, U16-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

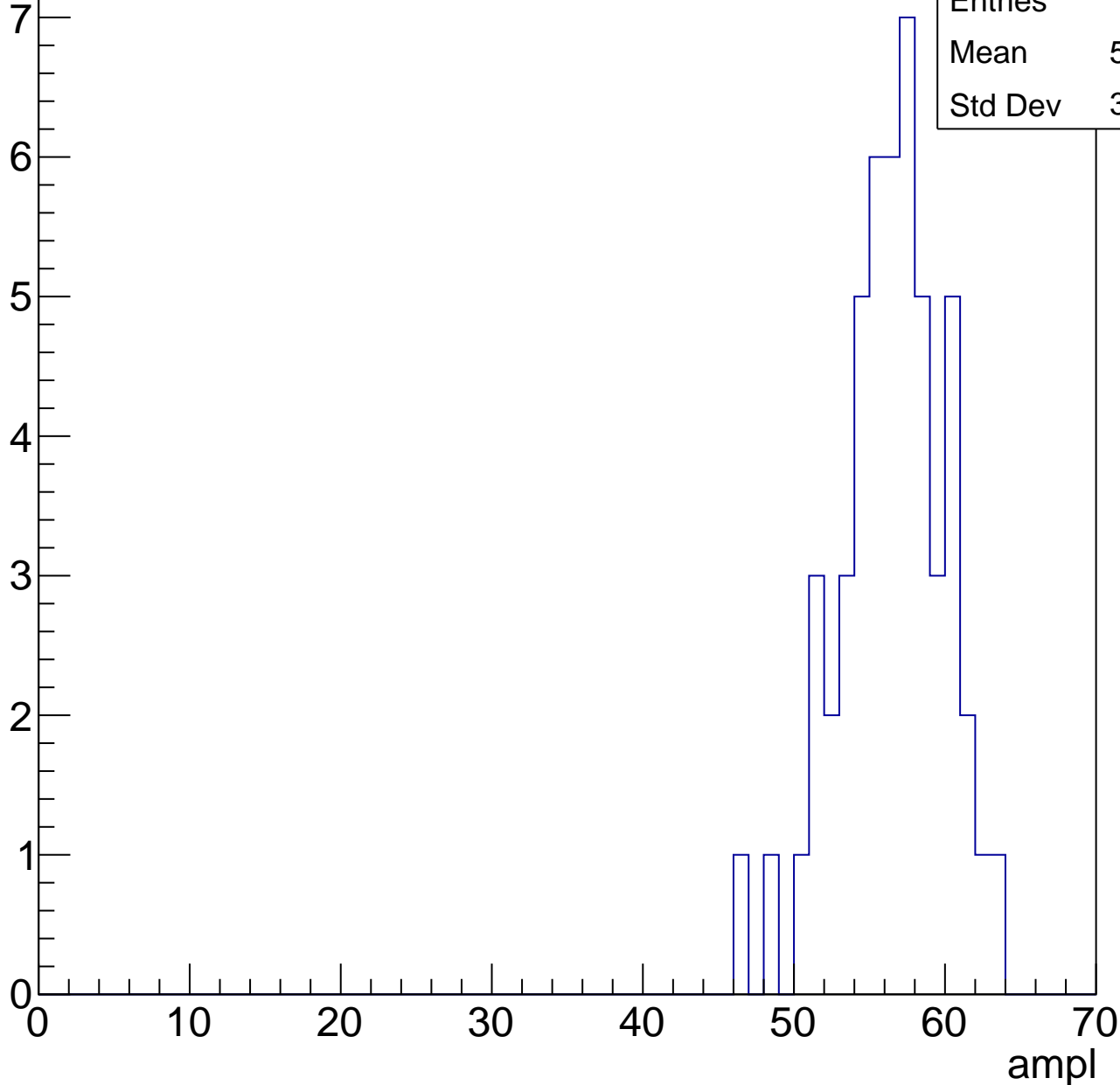
Entry



# B1L101S, U16-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

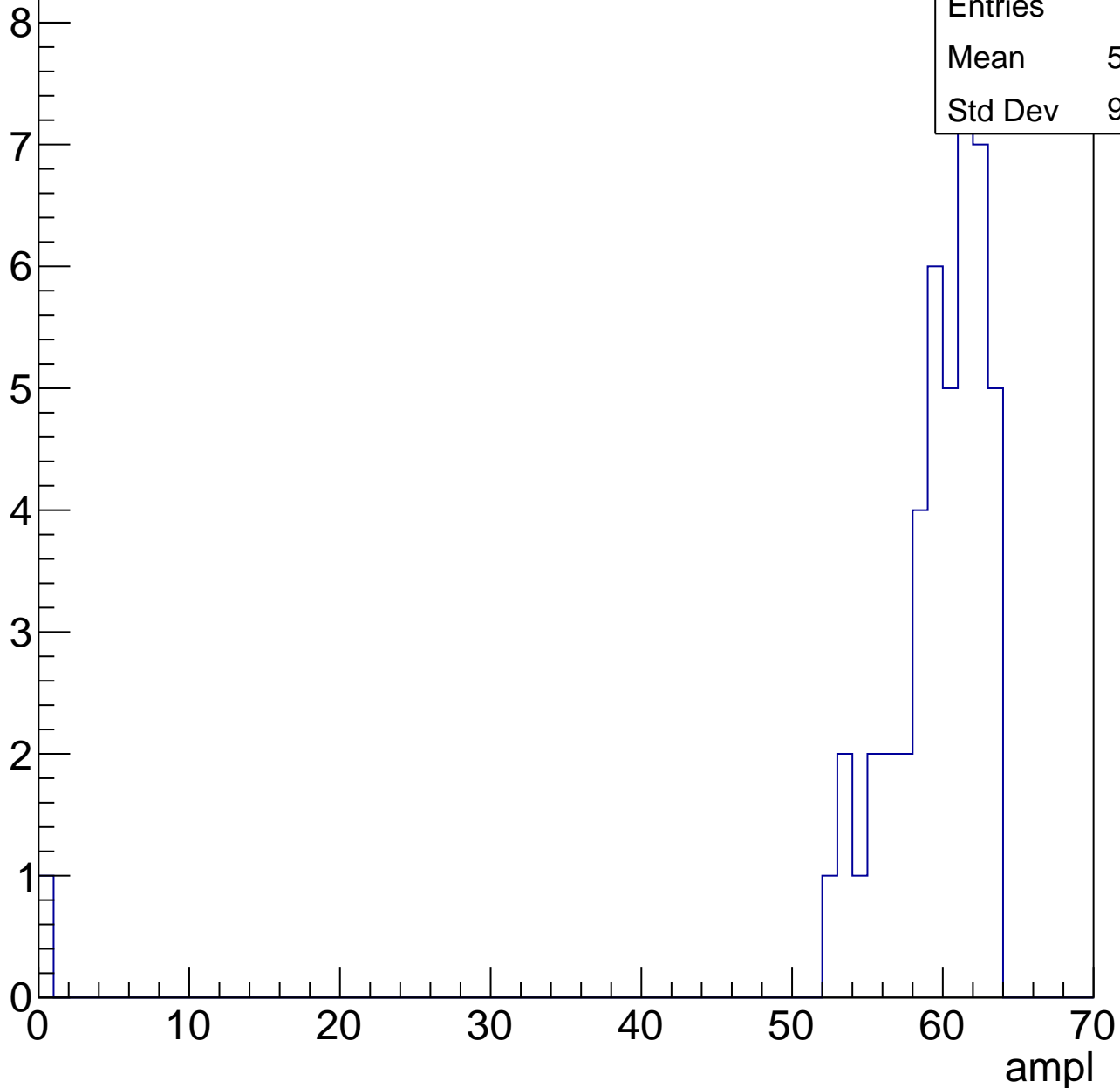
Entry



# B1L101S, U16-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

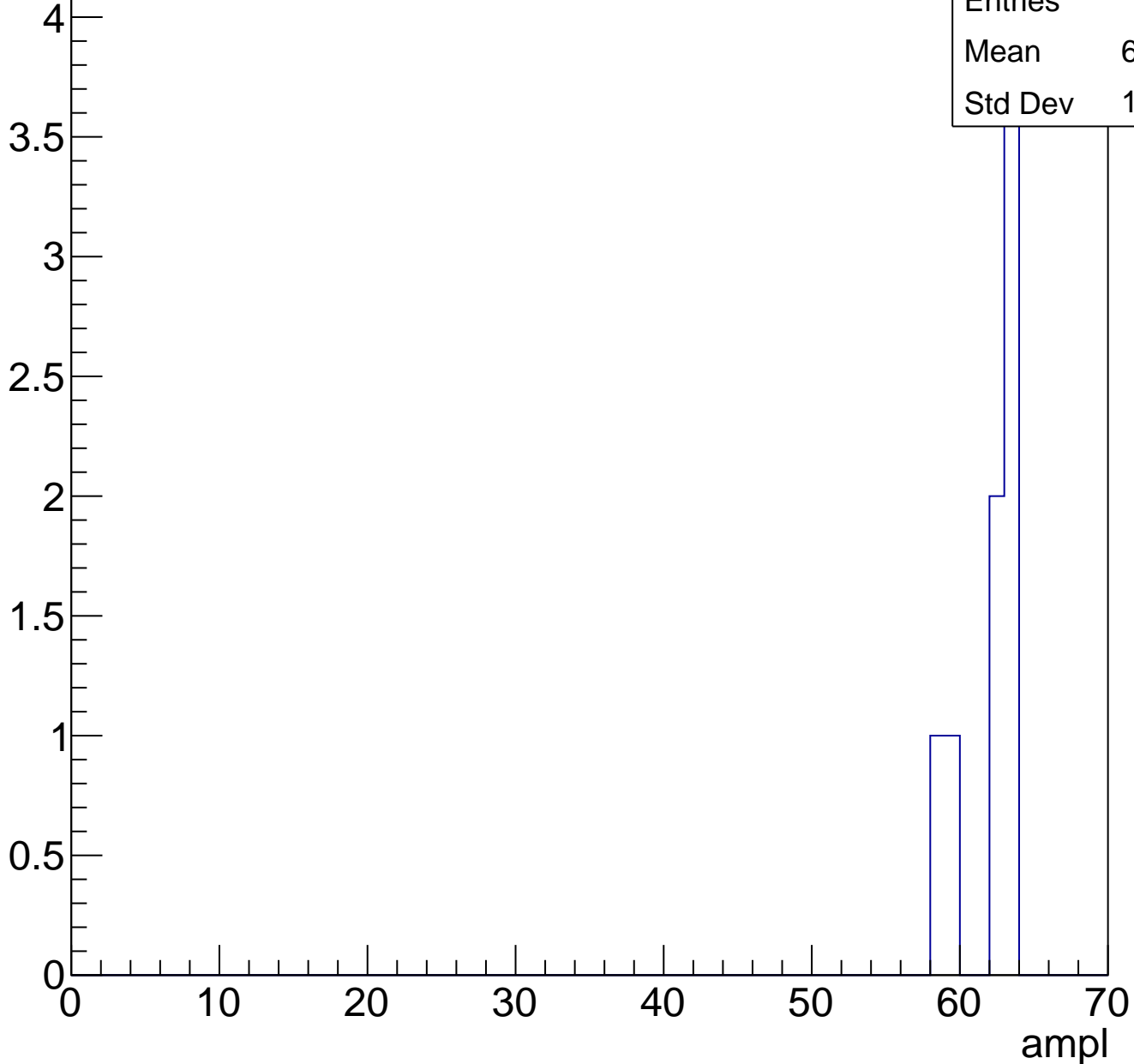
Entry



# B1L101S, U16-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch57, adc0

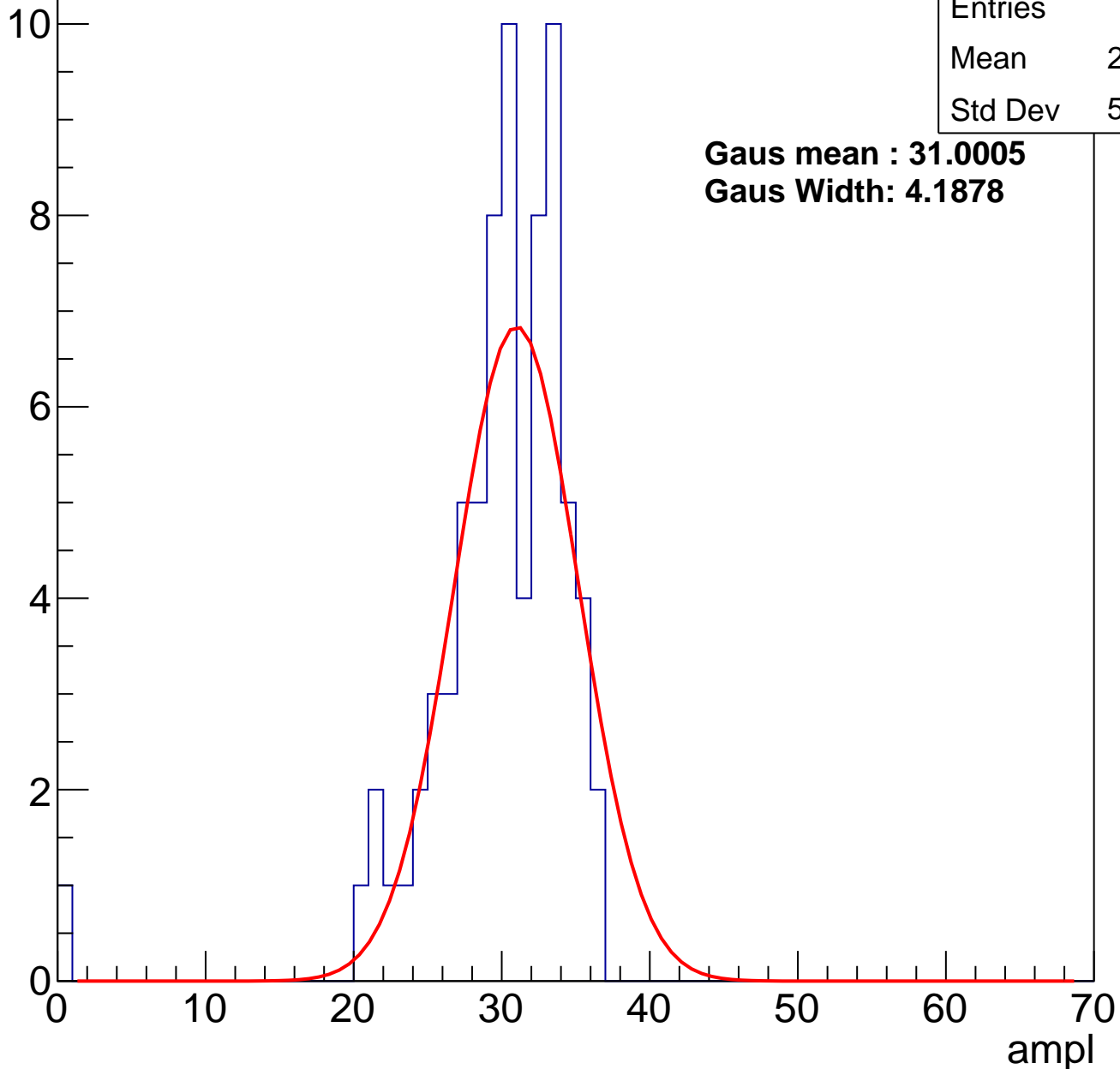
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	75
Mean	29.43
Std Dev	5.028

**Gaus mean : 31.0005**

**Gaus Width: 4.1878**

Entry



# B1L101S, U16-ch57, adc1

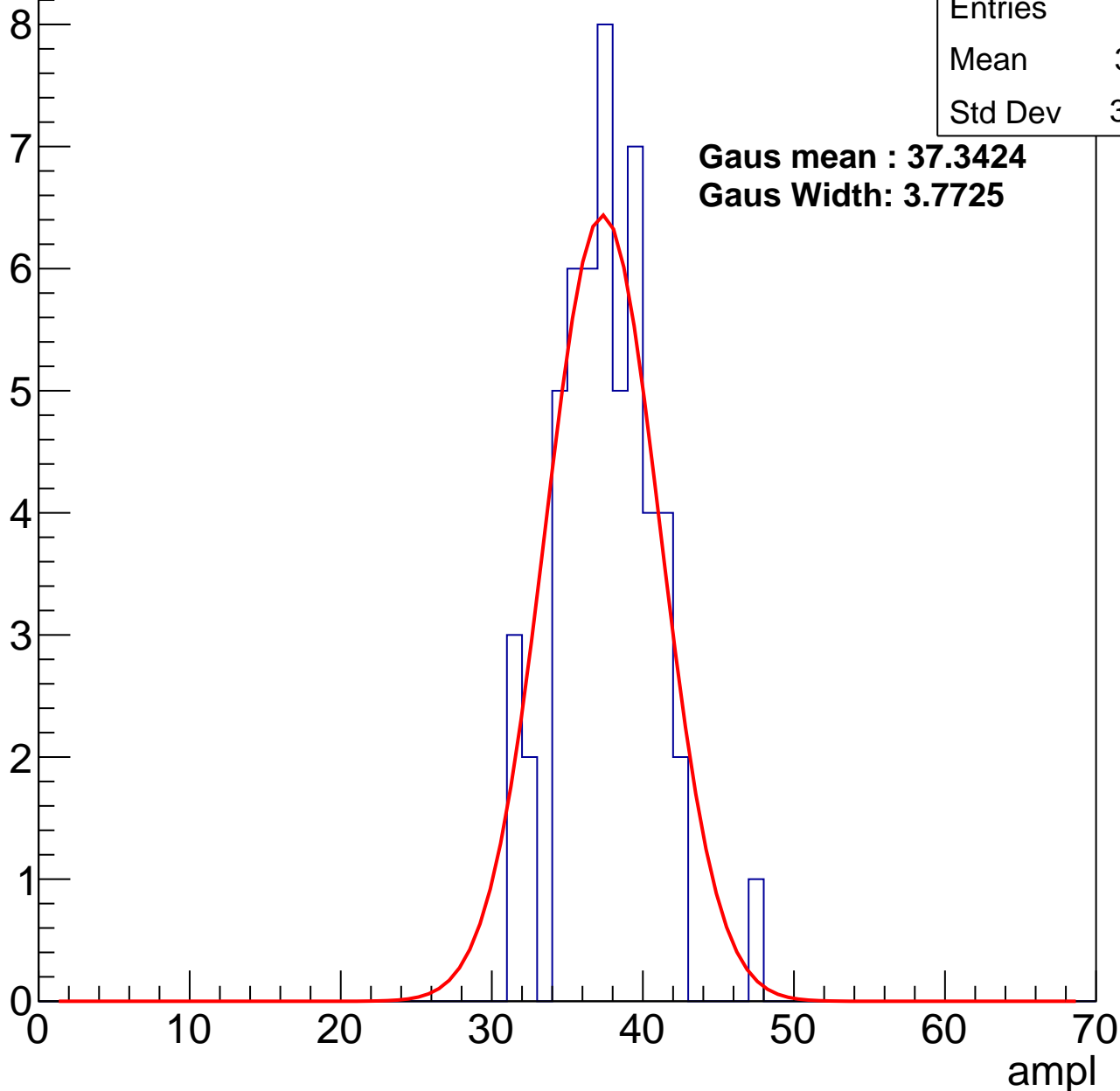
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	37.11
Std Dev	3.118

**Gaus mean : 37.3424**

**Gaus Width: 3.7725**



# B1L101S, U16-ch57, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	81
Mean	43.25
Std Dev	3.936

**Gaus mean : 43.7466**

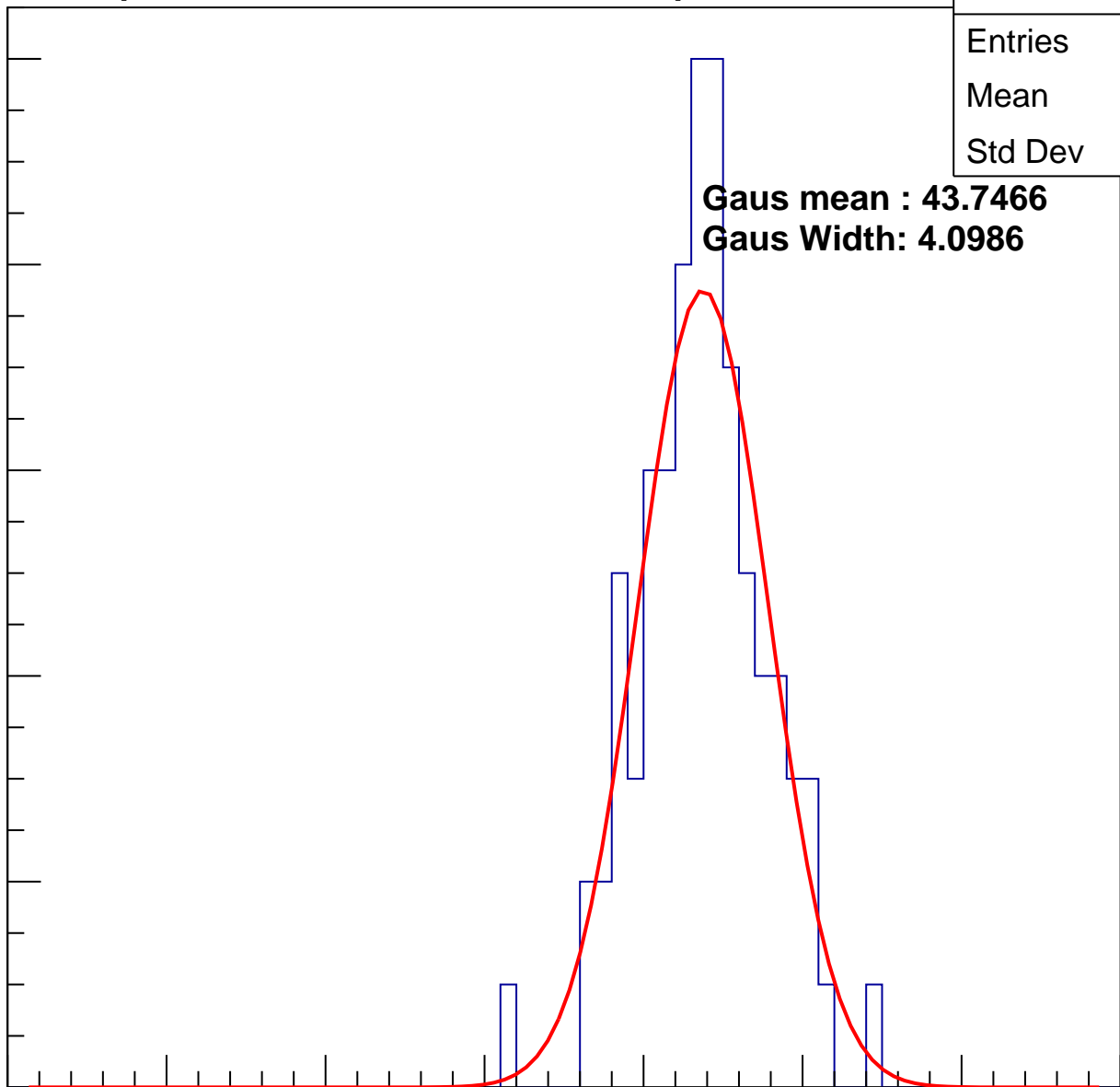
**Gaus Width: 4.0986**

Entry

10  
8  
6  
4  
2  
0

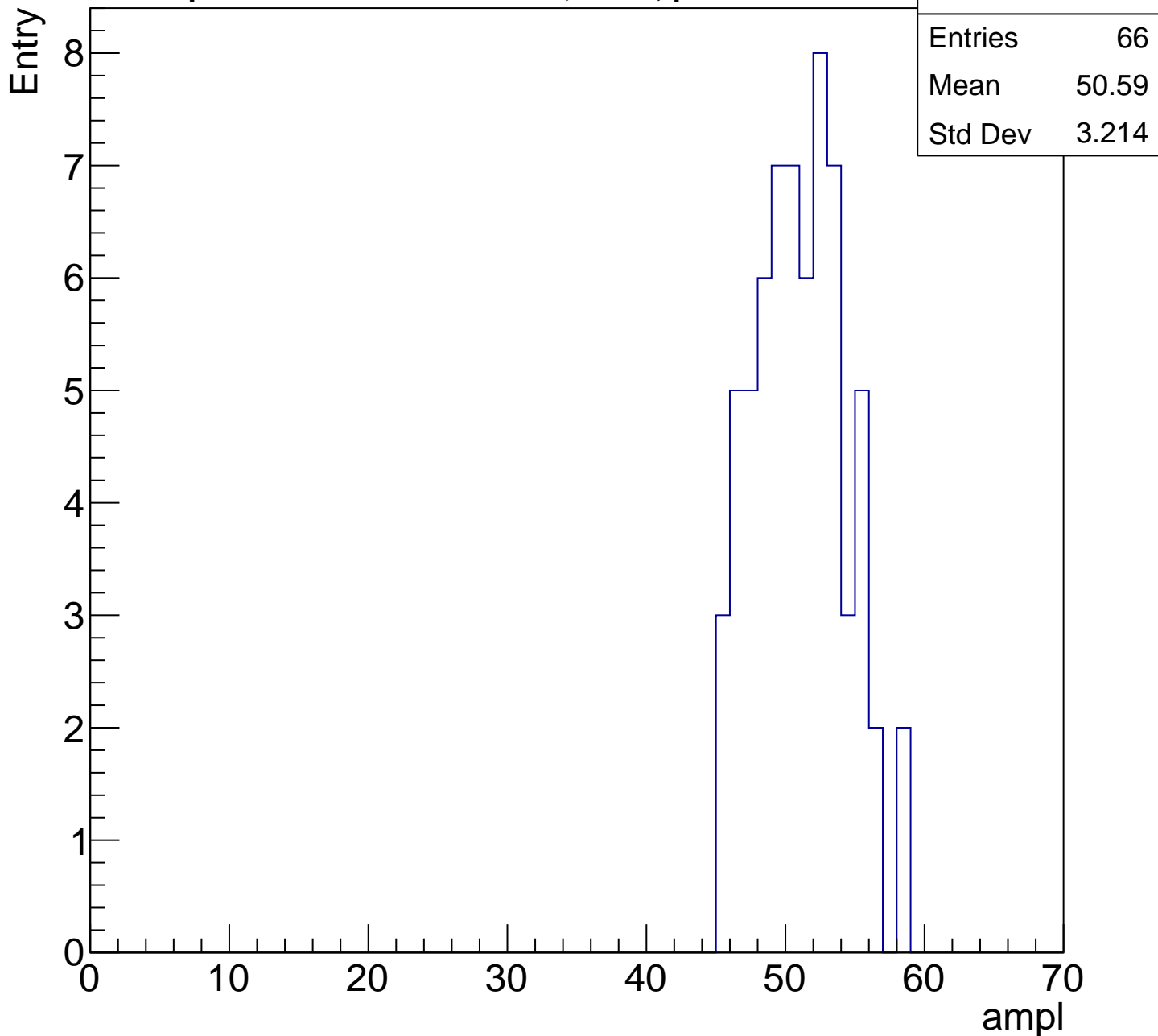
ampl

0 10 20 30 40 50 60 70



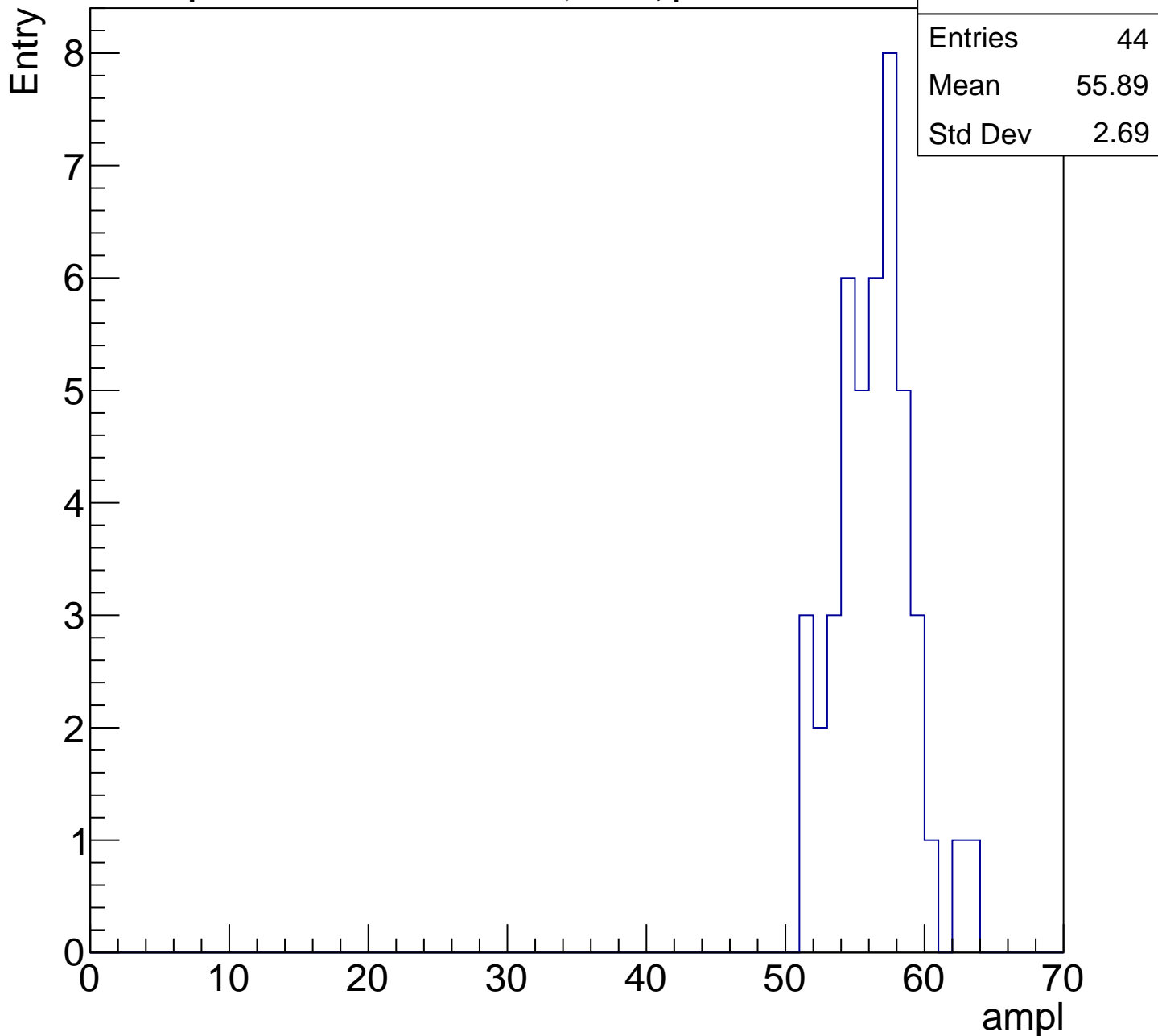
# B1L101S, U16-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U16-ch57, adc4

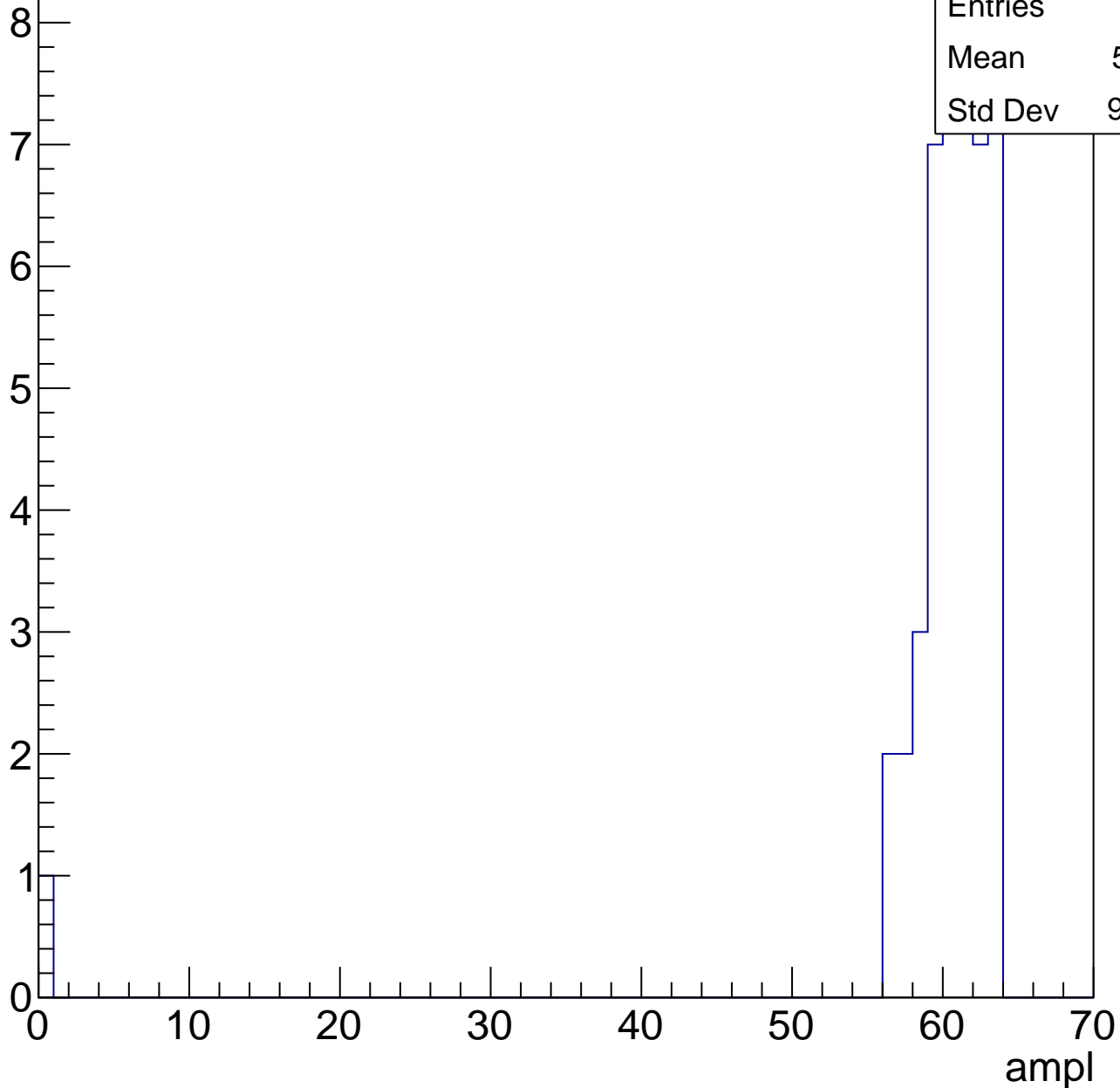
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U16-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

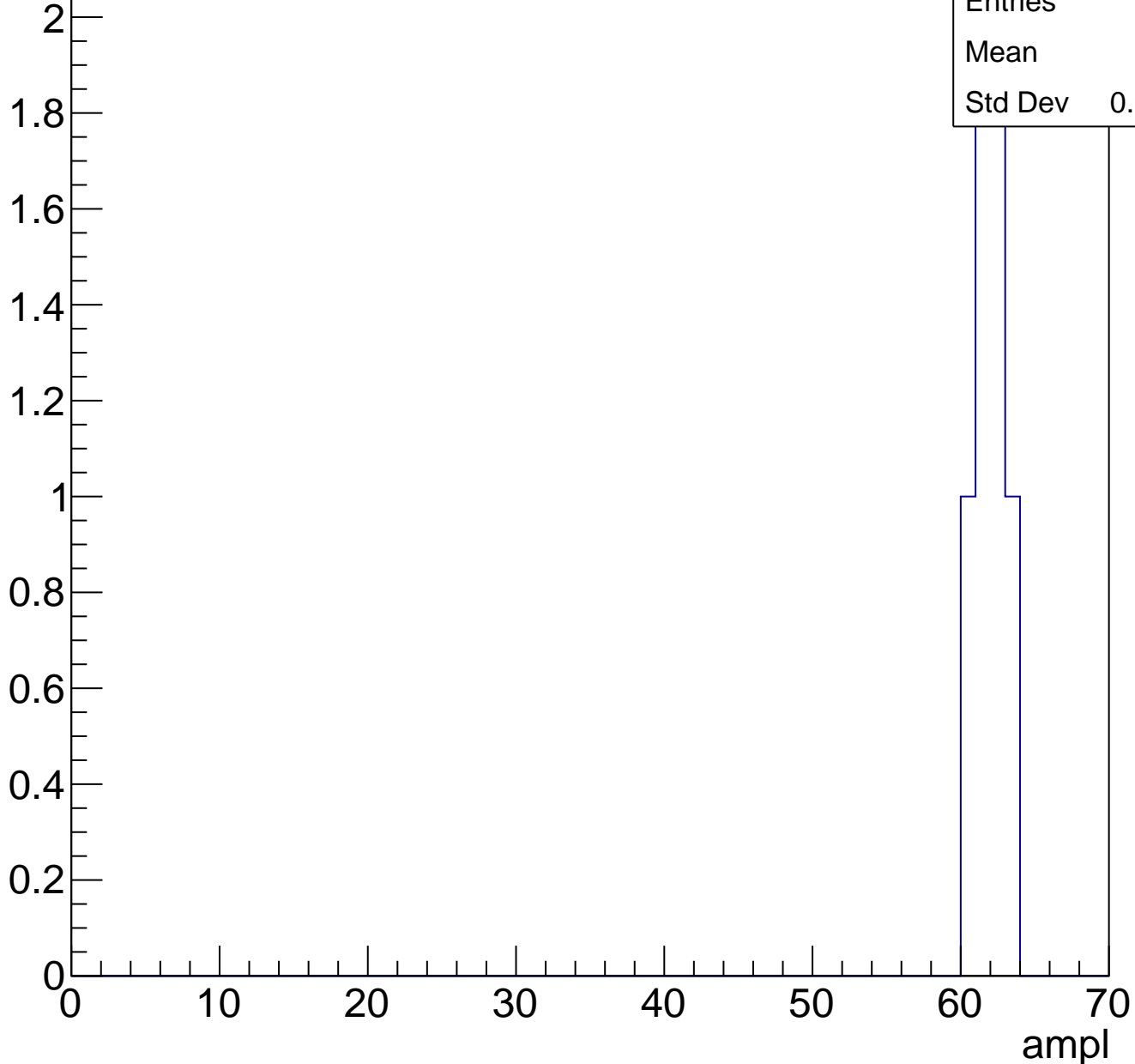


Entries	46
Mean	59.11
Std Dev	9.017

# B1L101S, U16-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U16-ch58, adc0

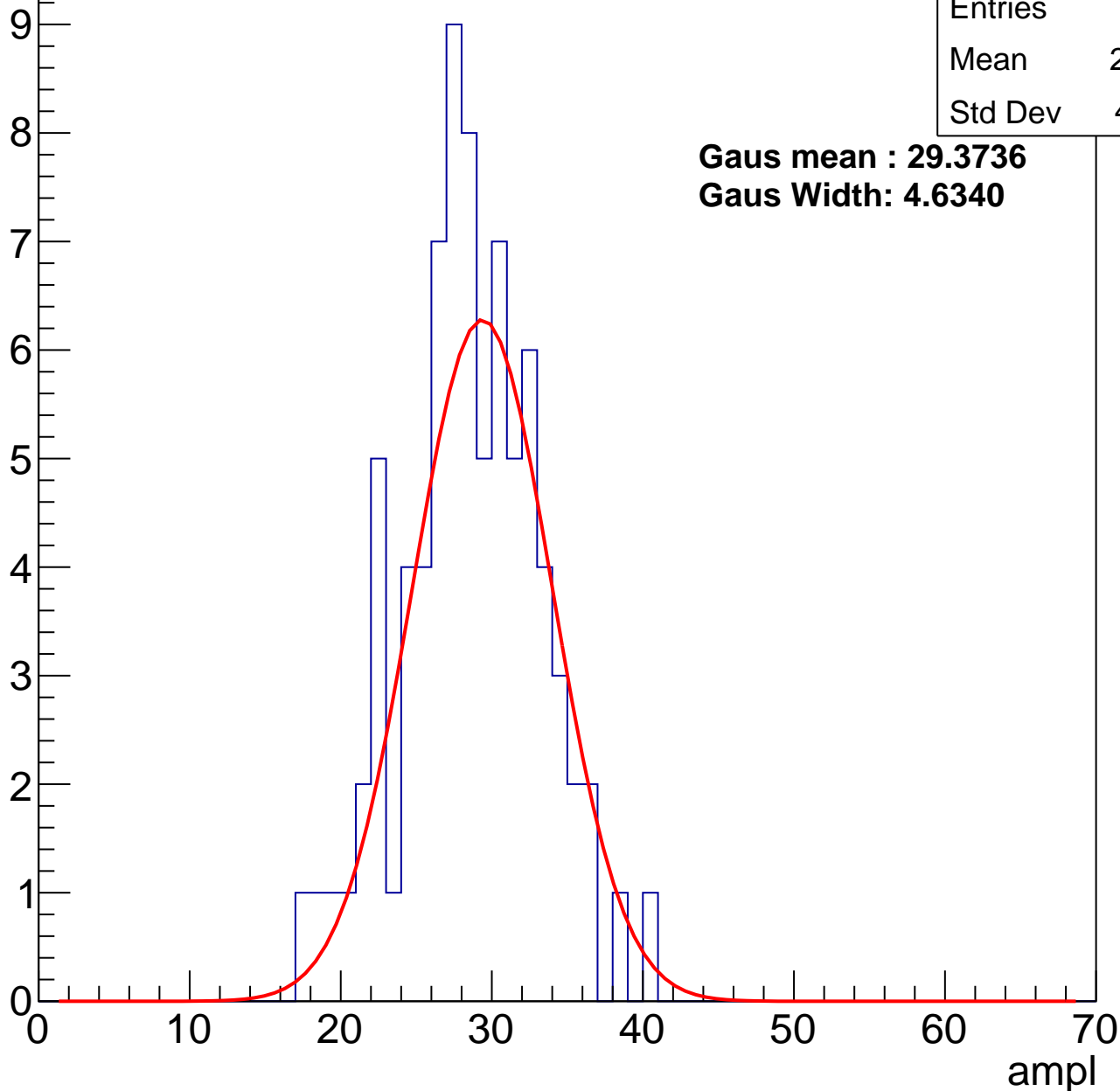
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	28.12
Std Dev	4.551

**Gaus mean : 29.3736**

**Gaus Width: 4.6340**



# B1L101S, U16-ch58, adc1

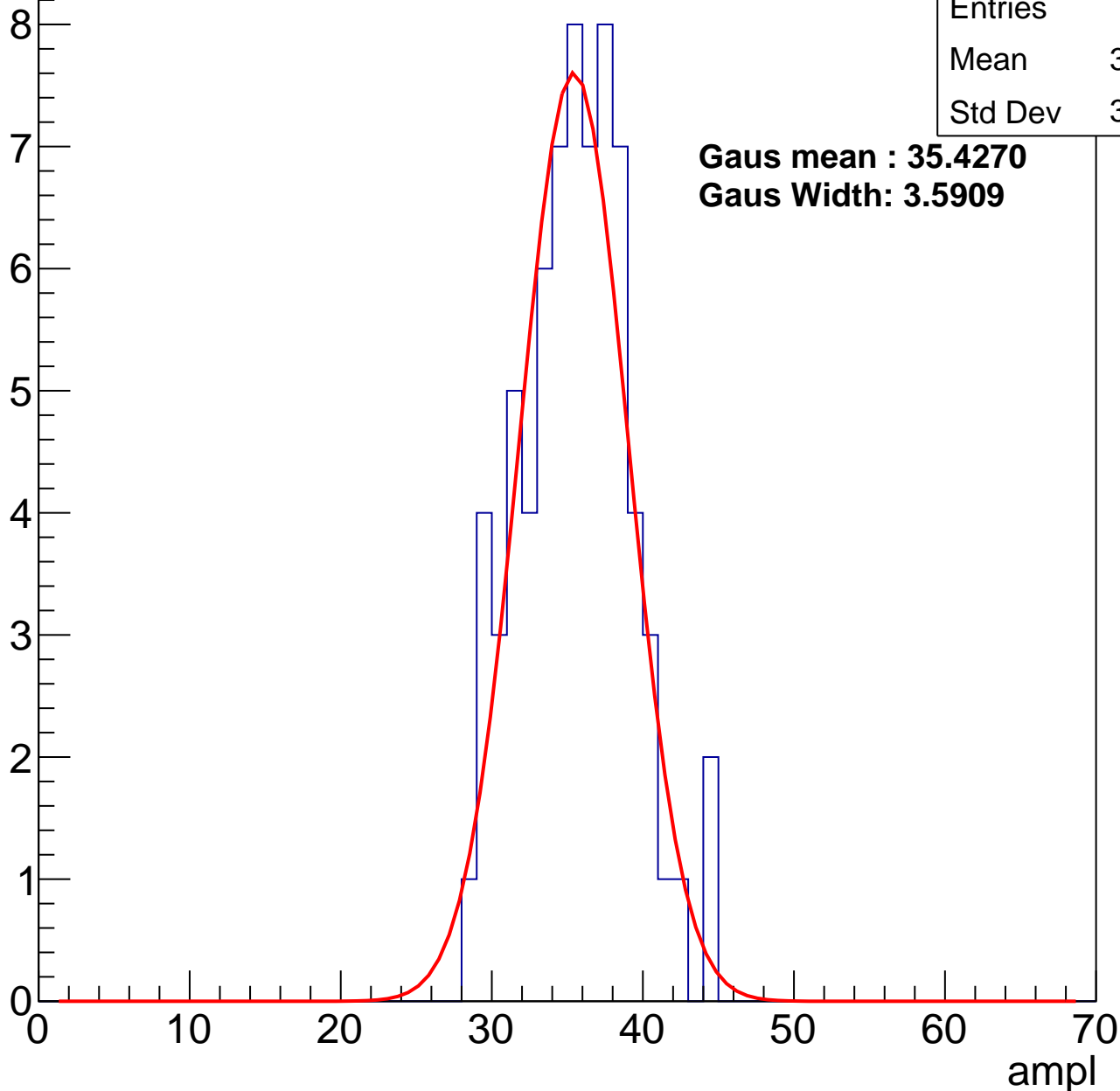
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	35.13
Std Dev	3.564

**Gaus mean : 35.4270**

**Gaus Width: 3.5909**

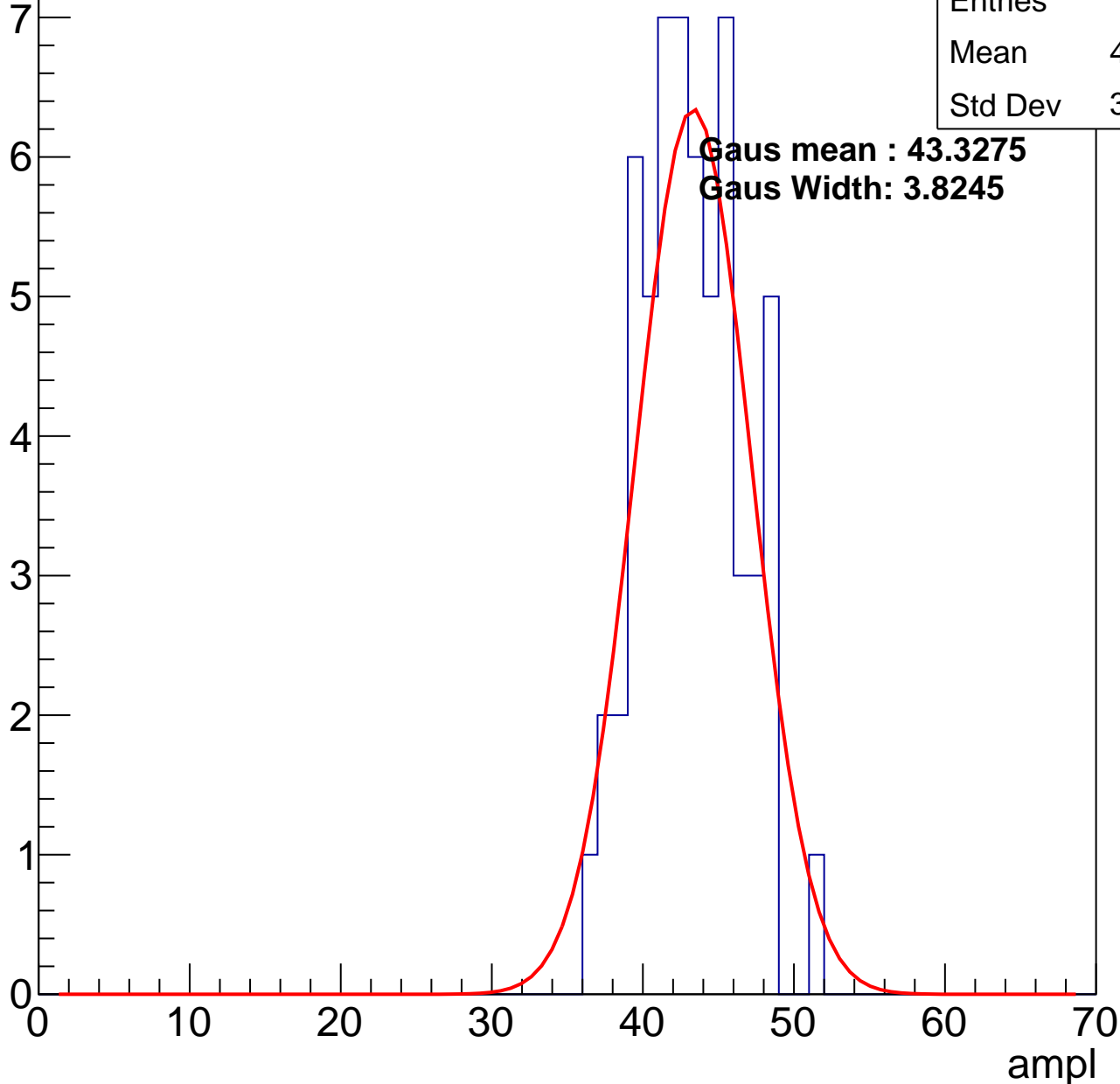


# B1L101S, U16-ch58, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	42.73
Std Dev	3.265

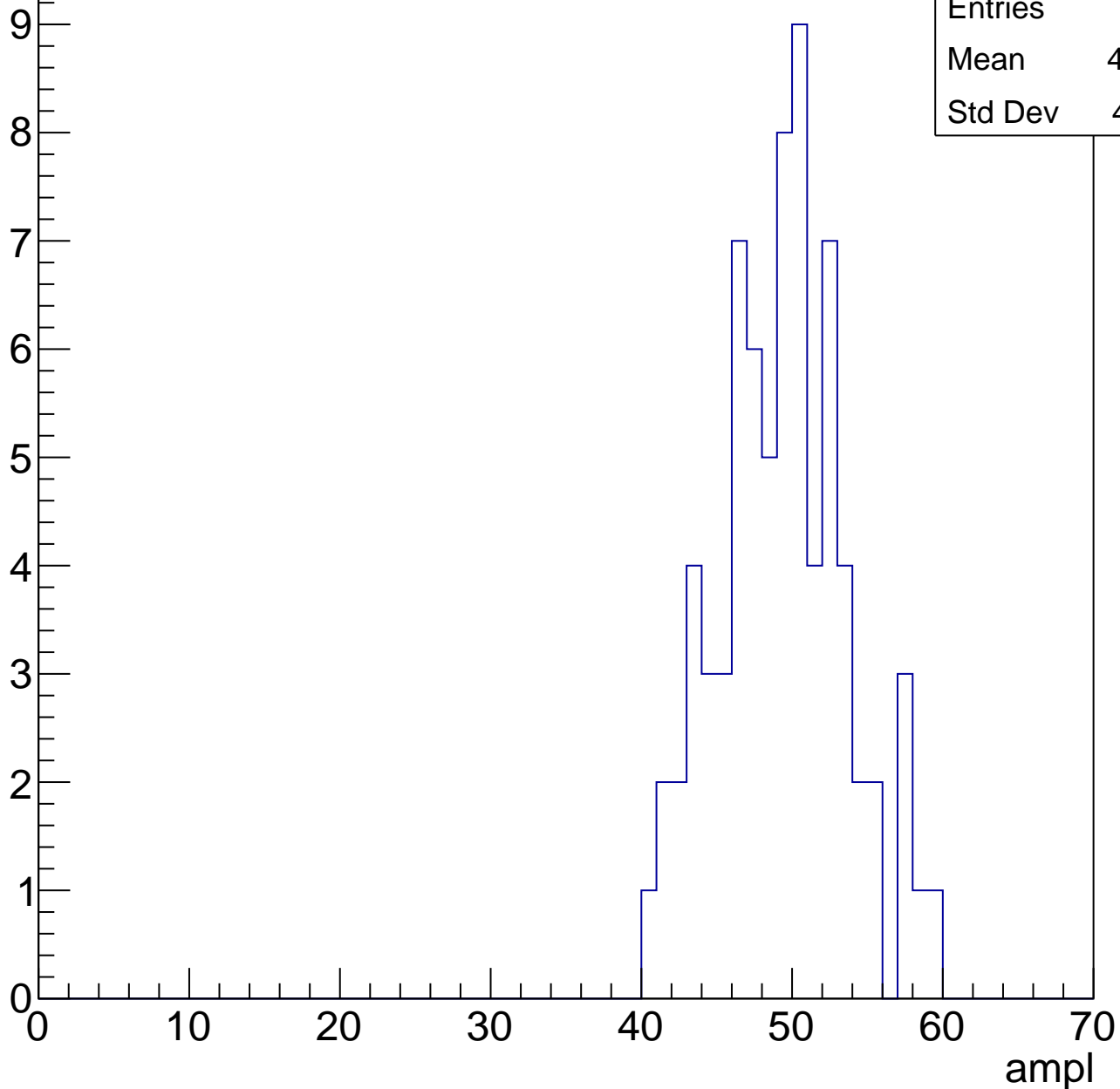


# B1L101S, U16-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

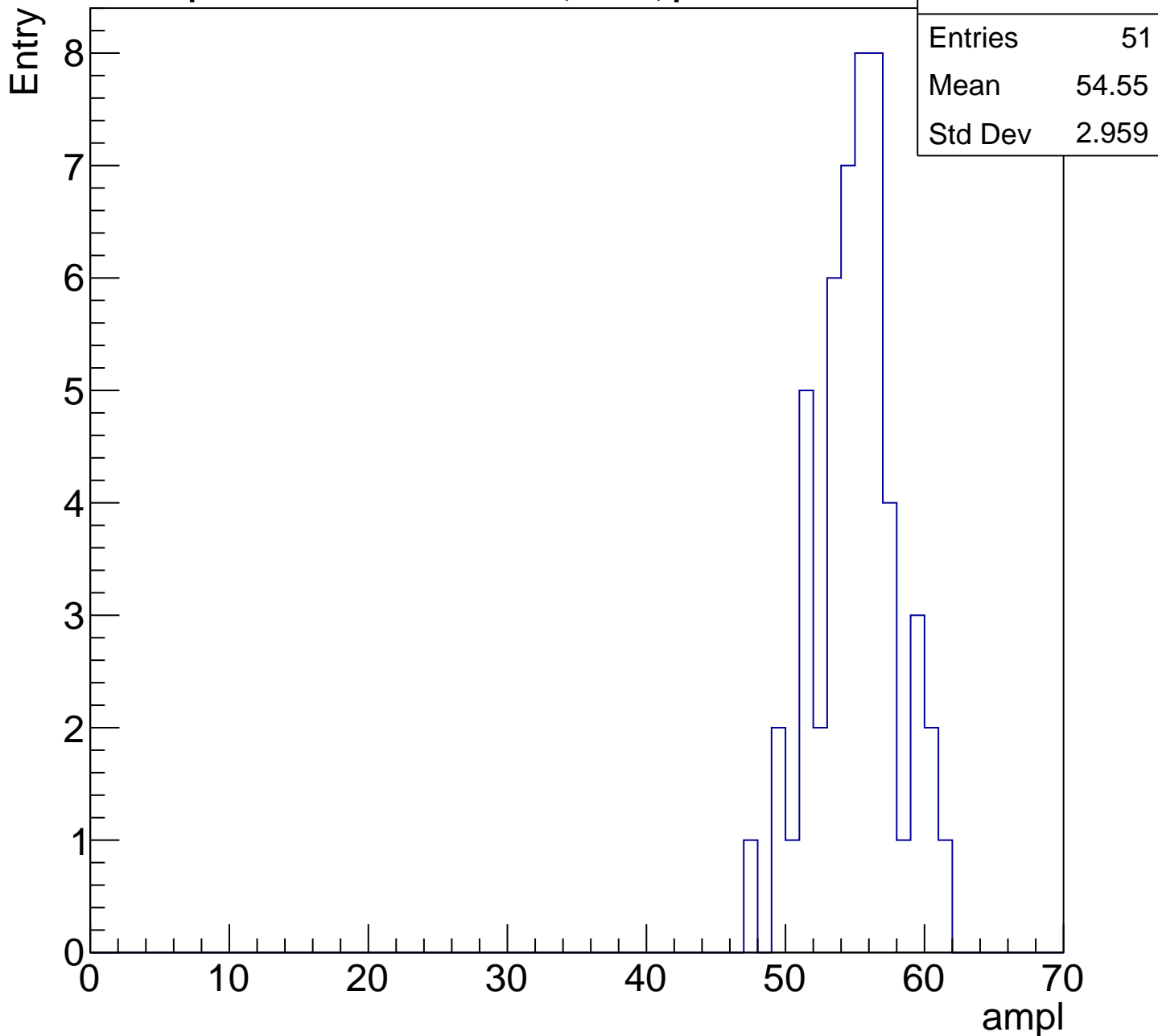
Entry

Entries	74
Mean	48.88
Std Dev	4.211



# B1L101S, U16-ch58, adc4

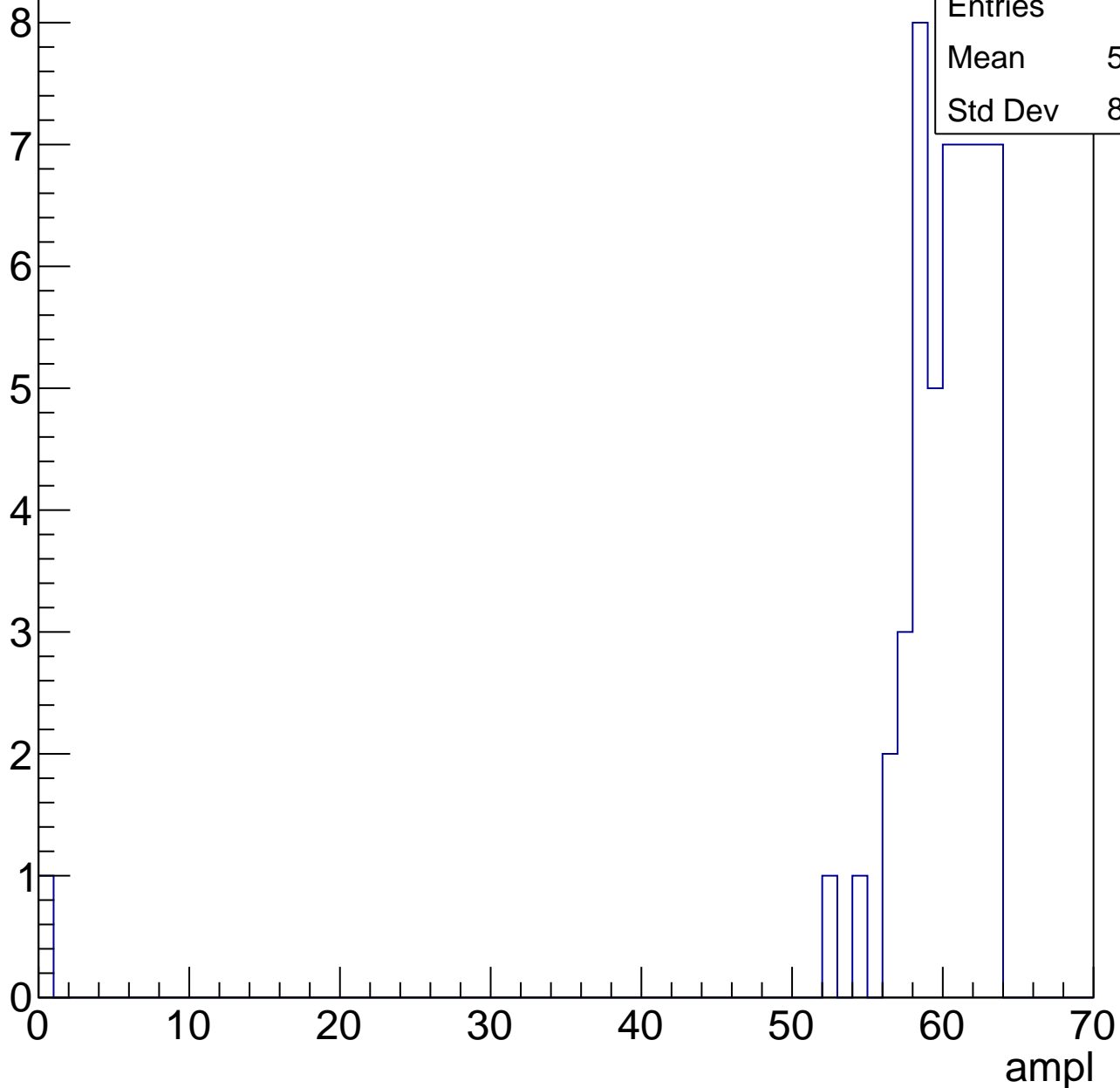
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U16-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

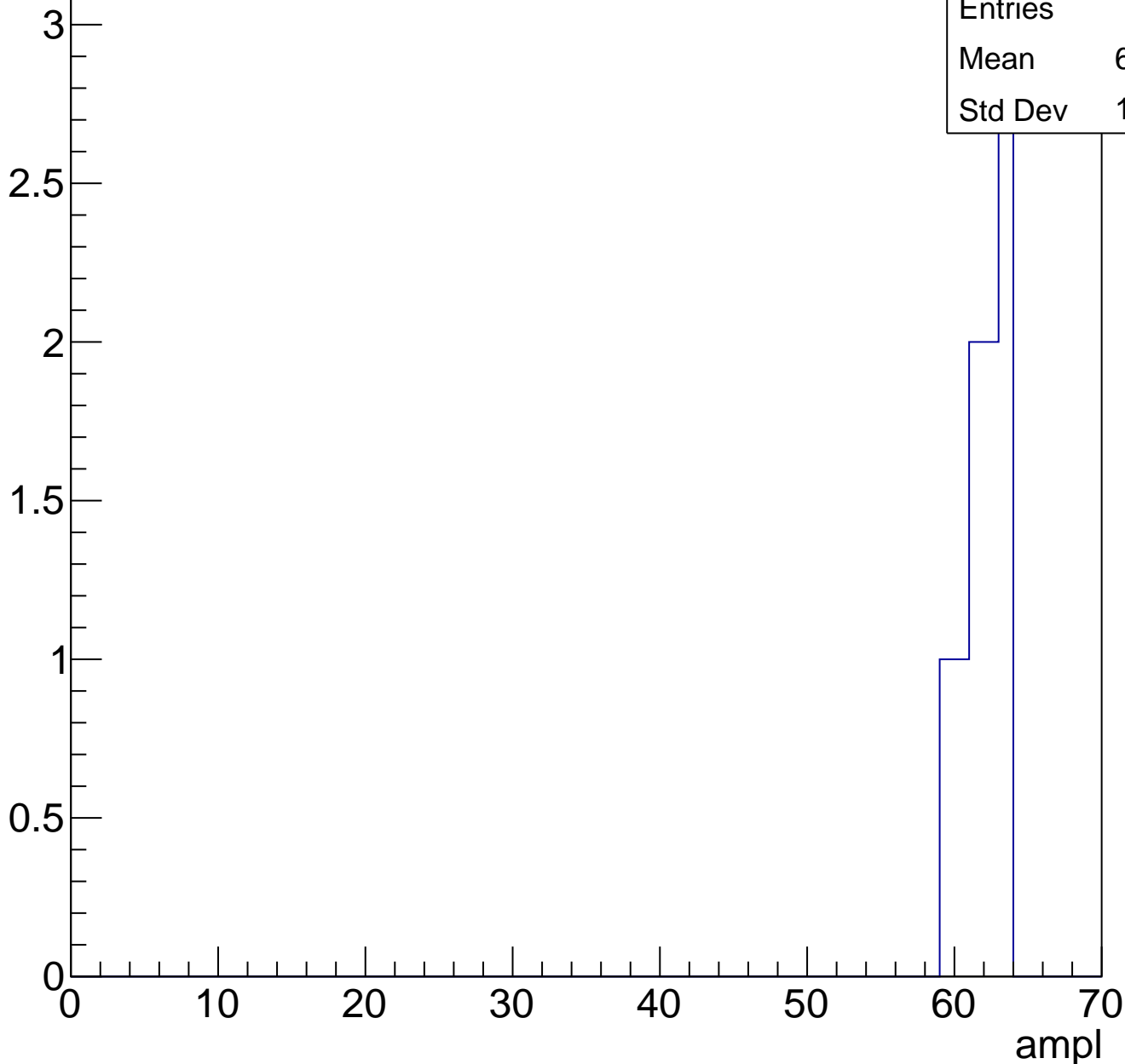
Entry



# B1L101S, U16-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



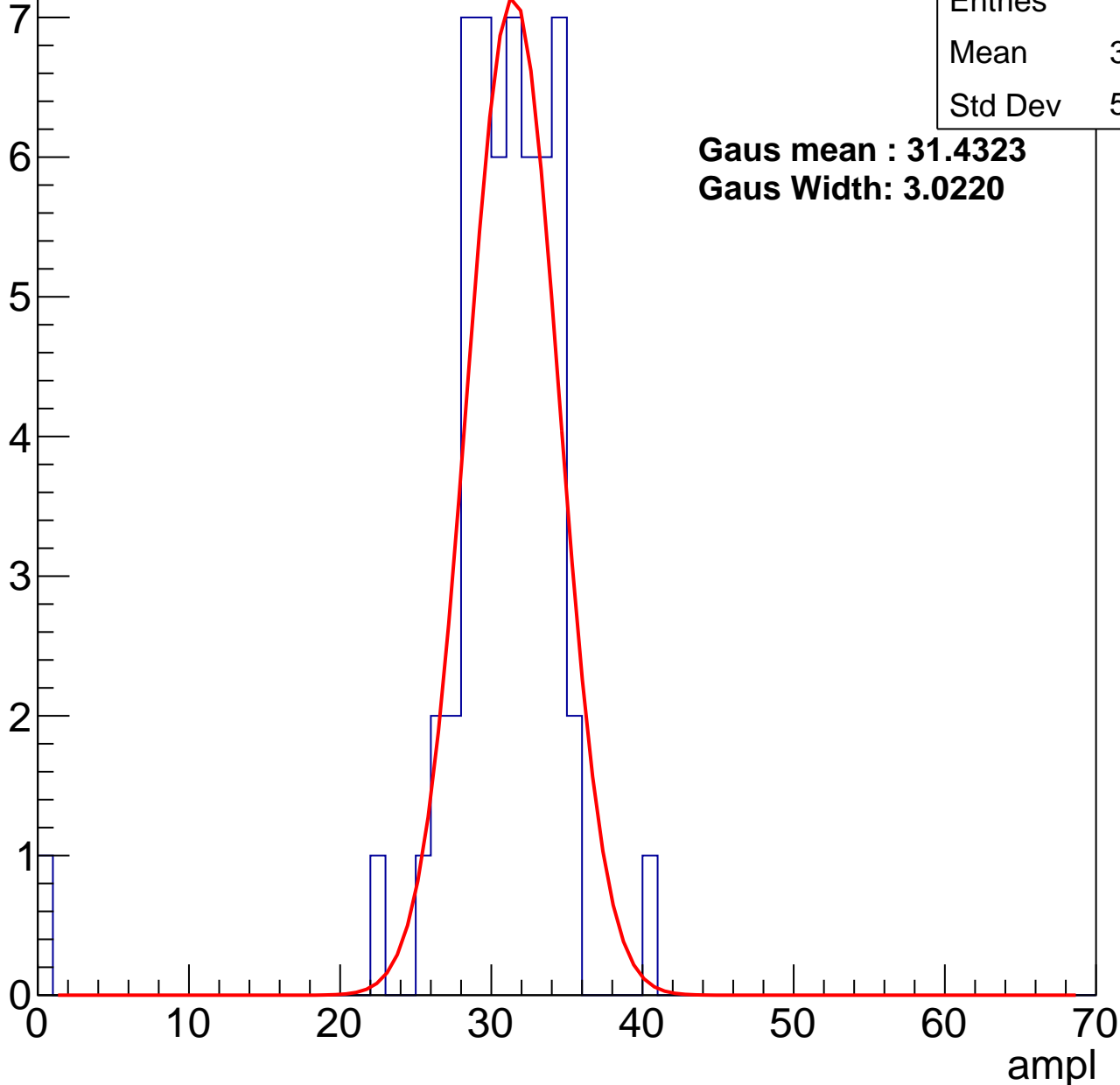
# B1L101S, U16-ch59, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	30.12
Std Dev	5.036

**Gaus mean : 31.4323**  
**Gaus Width: 3.0220**



# B1L101S, U16-ch59, adc1

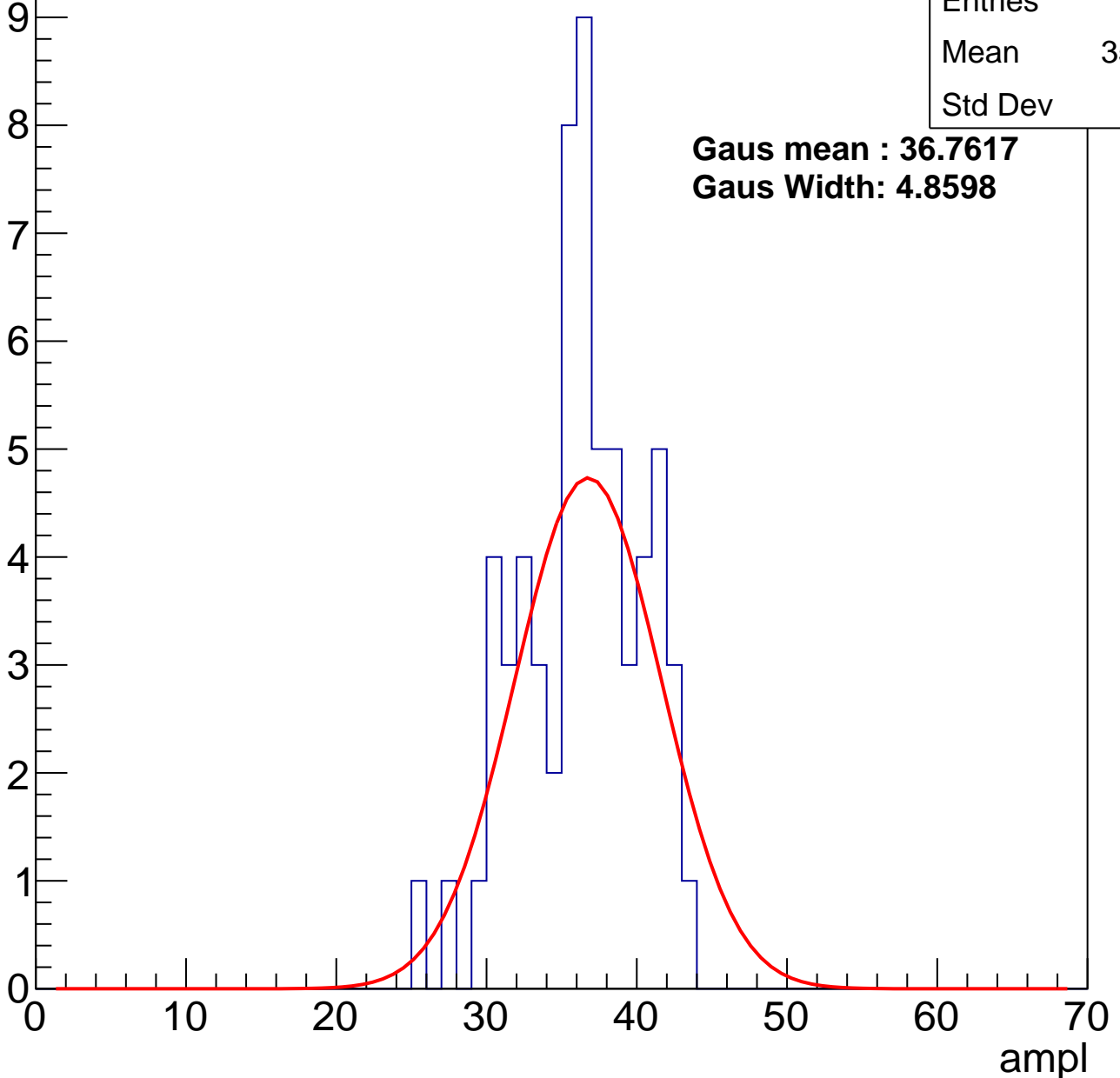
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	35.79
Std Dev	3.96

**Gaus mean : 36.7617**

**Gaus Width: 4.8598**



# B1L101S, U16-ch59, adc2

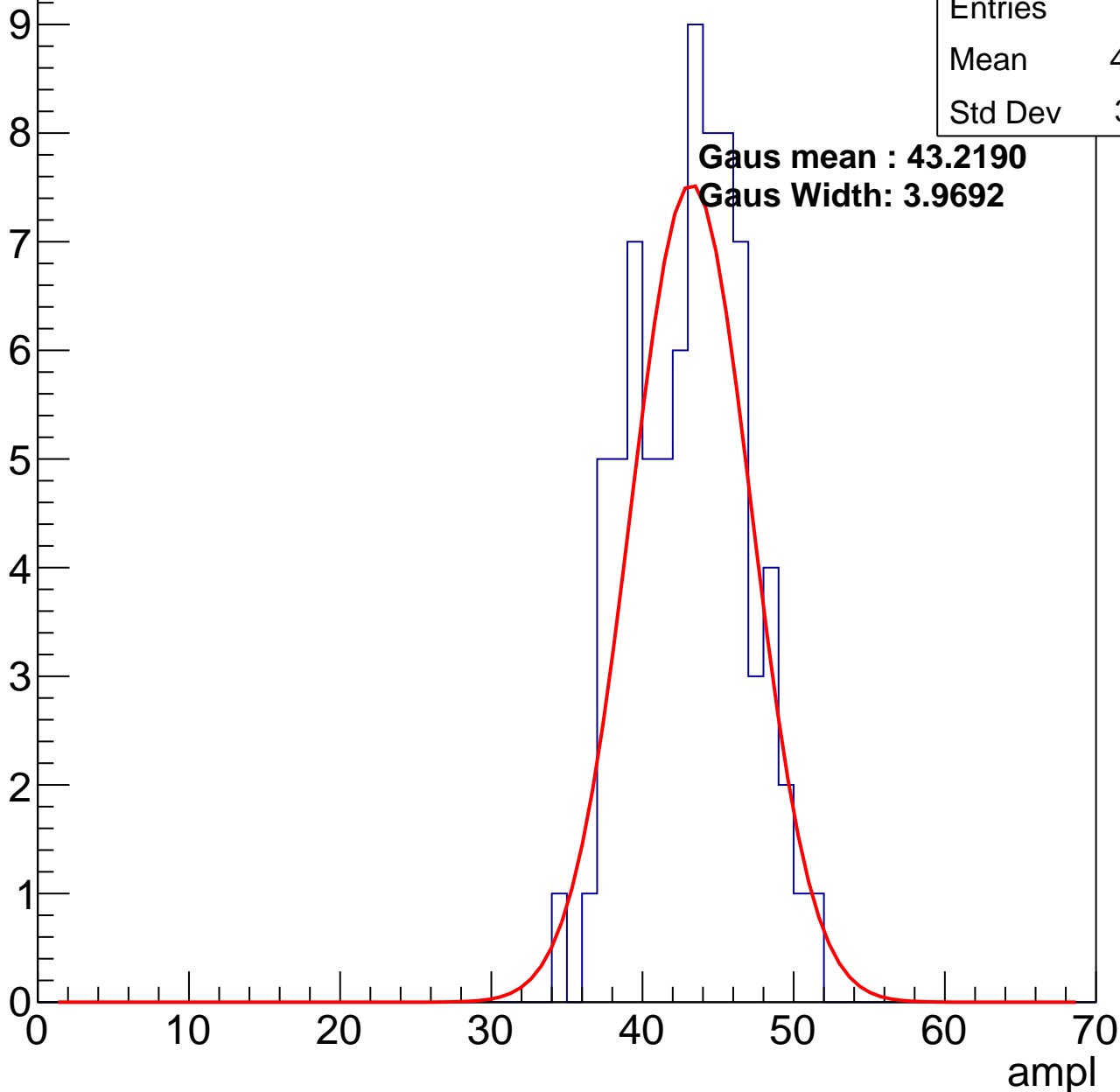
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	42.67
Std Dev	3.661

**Gaus mean : 43.2190**

**Gaus Width: 3.9692**

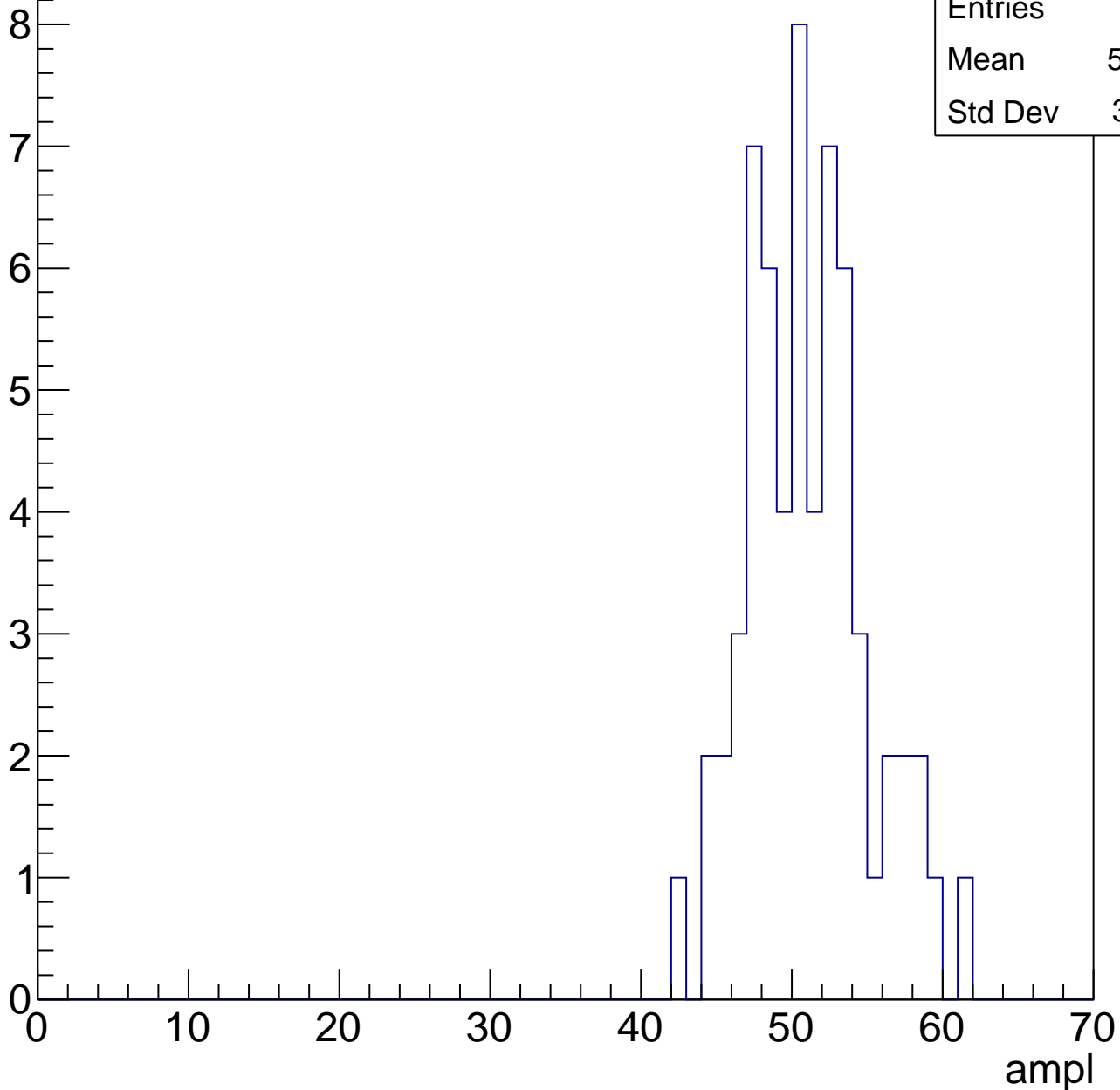


# B1L101S, U16-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

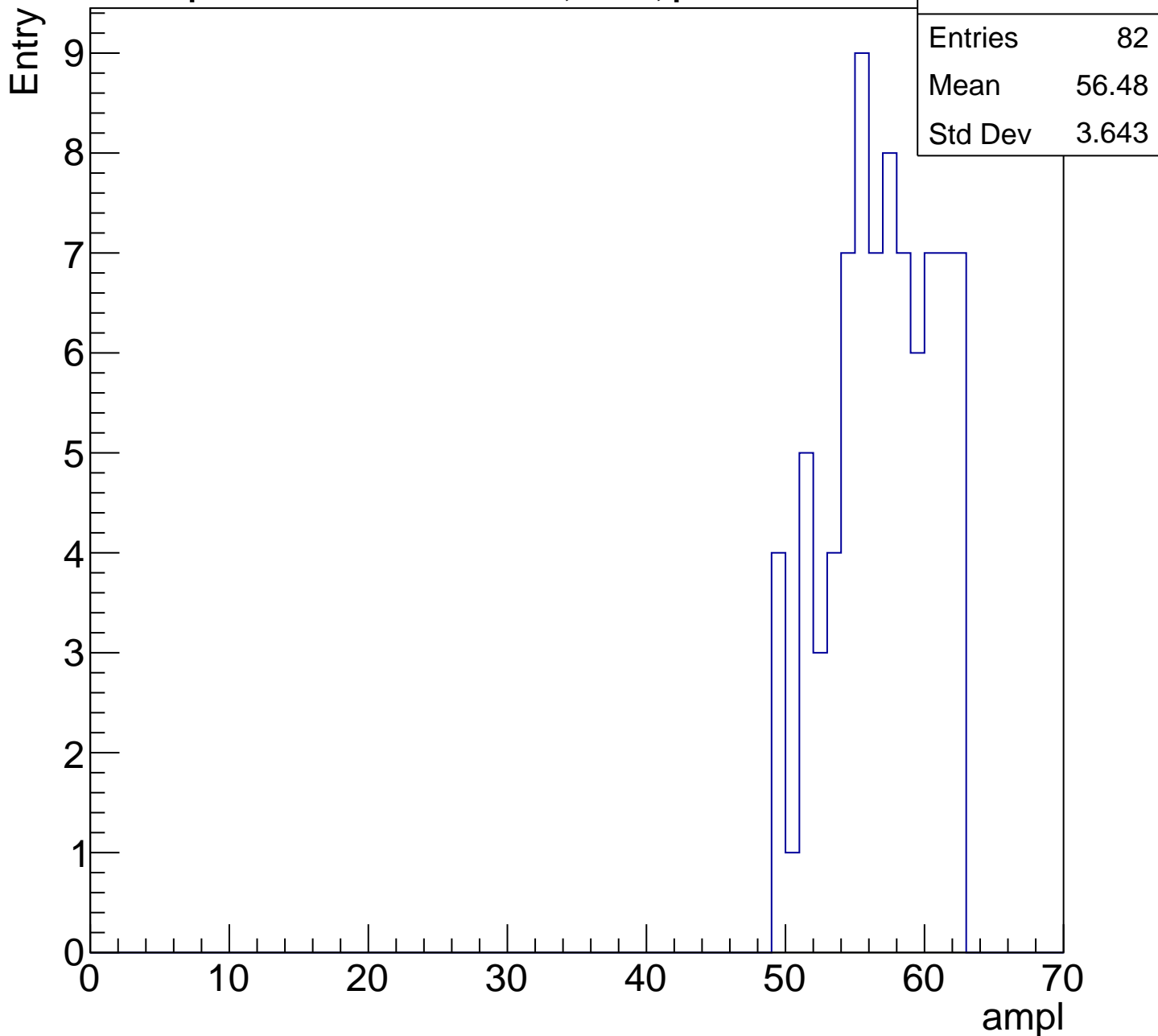
Entry

Entries	62
Mean	50.58
Std Dev	3.941



# B1L101S, U16-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

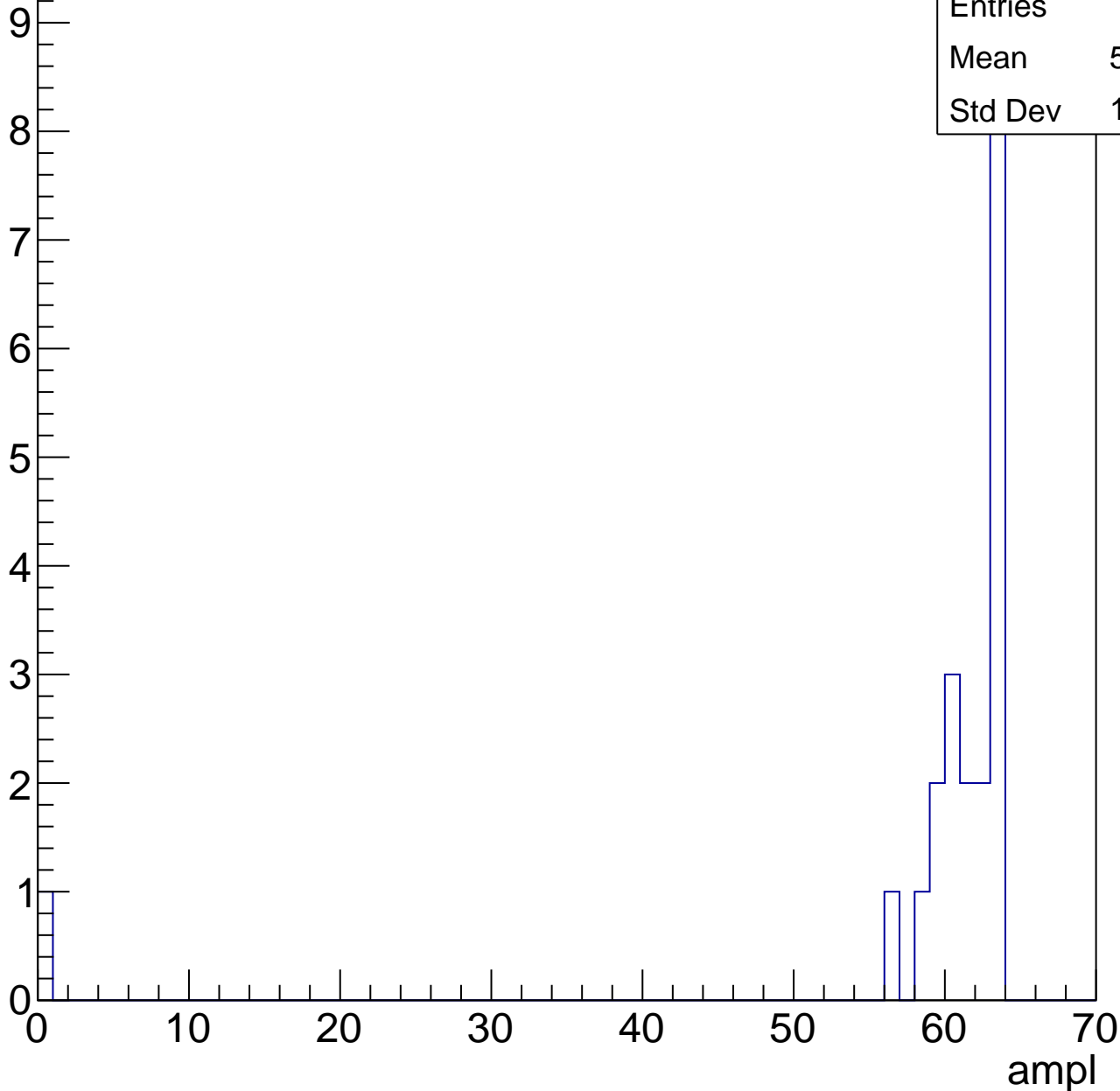


# B1L101S, U16-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

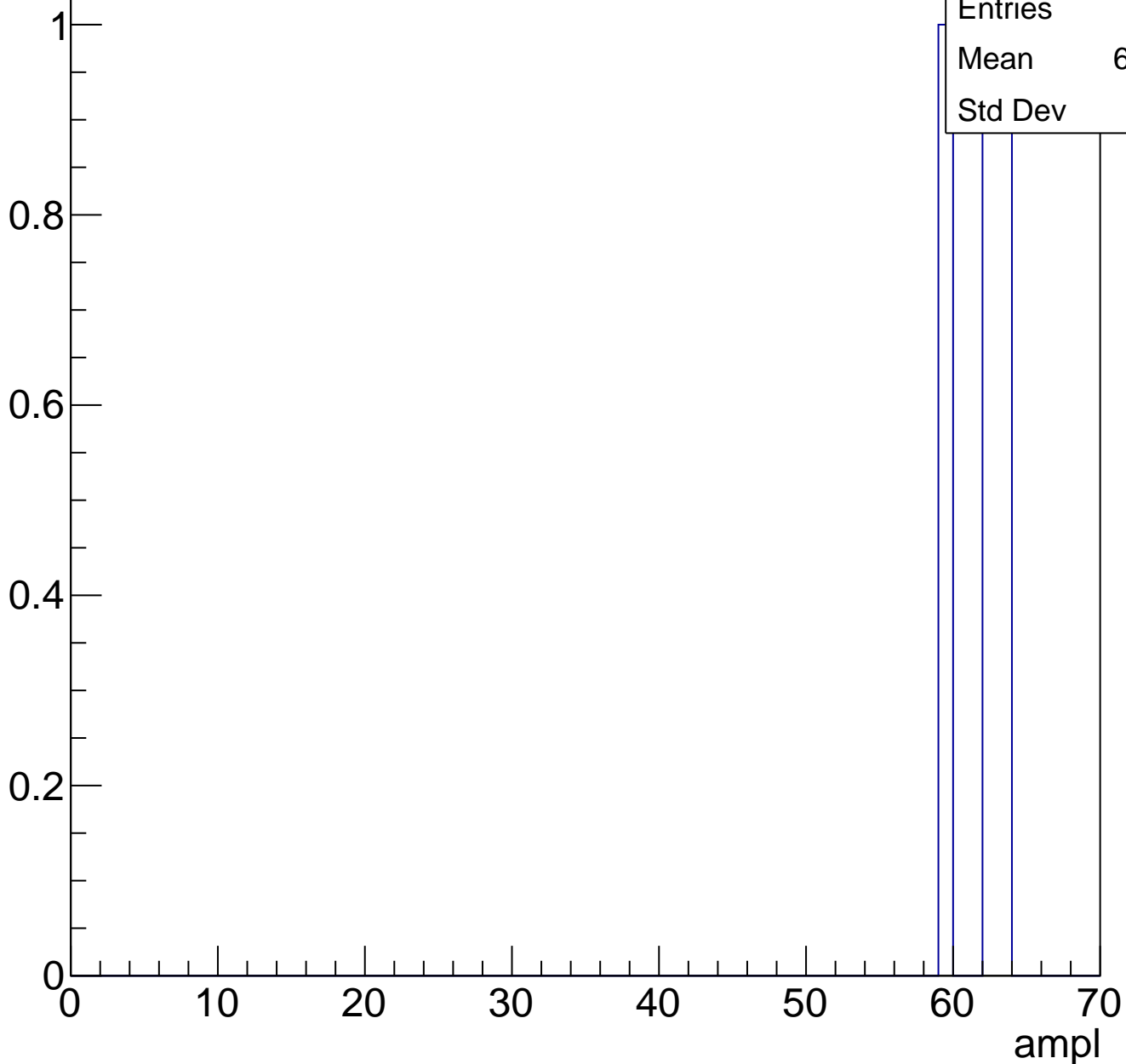
Entries	21
Mean	58.33
Std Dev	13.19



# B1L101S, U16-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch60, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	93
Mean	27.27
Std Dev	5.611

**Gaus mean : 28.3980**

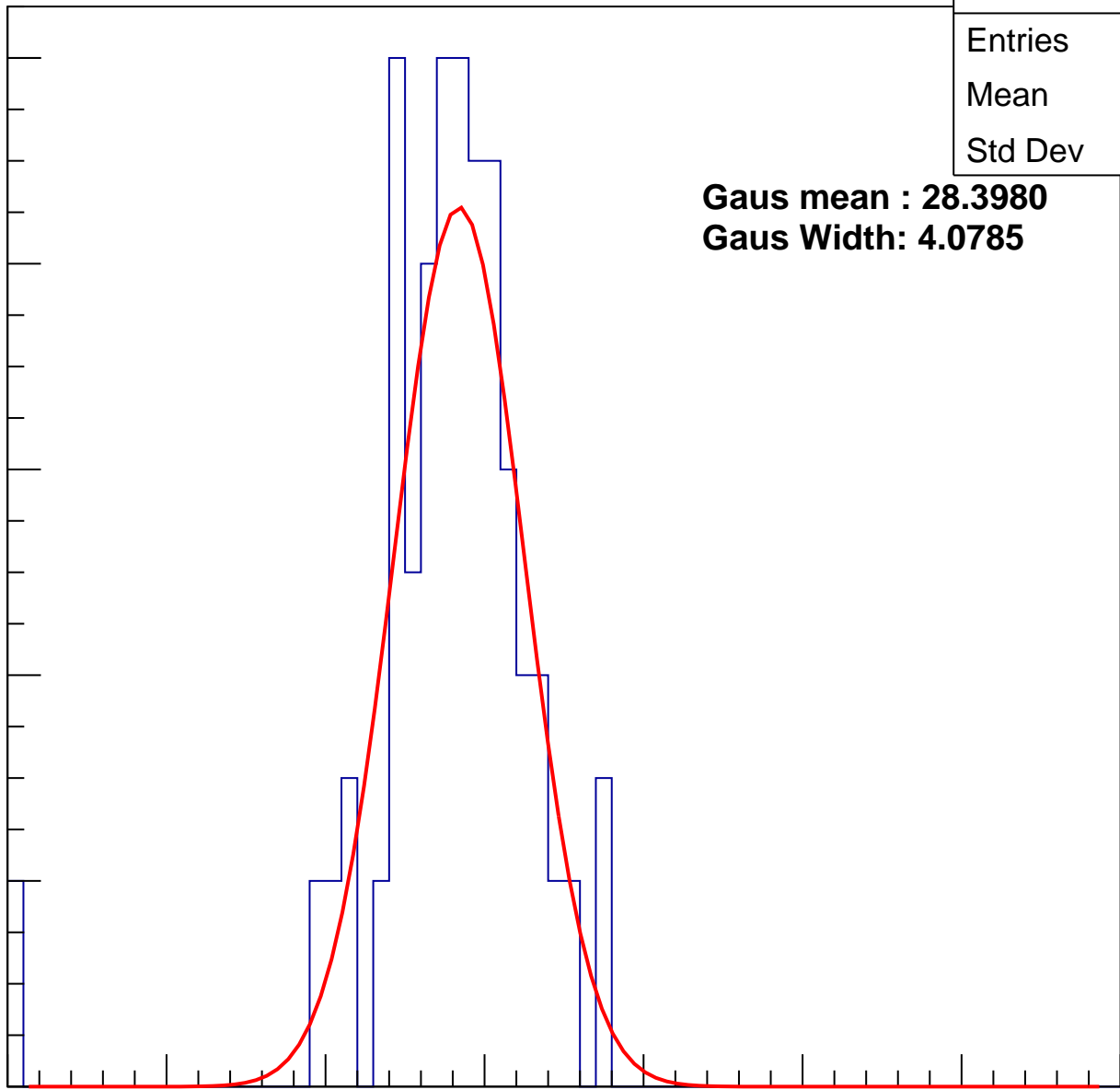
**Gaus Width: 4.0785**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch60, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	65
Mean	35.85
Std Dev	3.119

**Gaus mean : 36.3007**

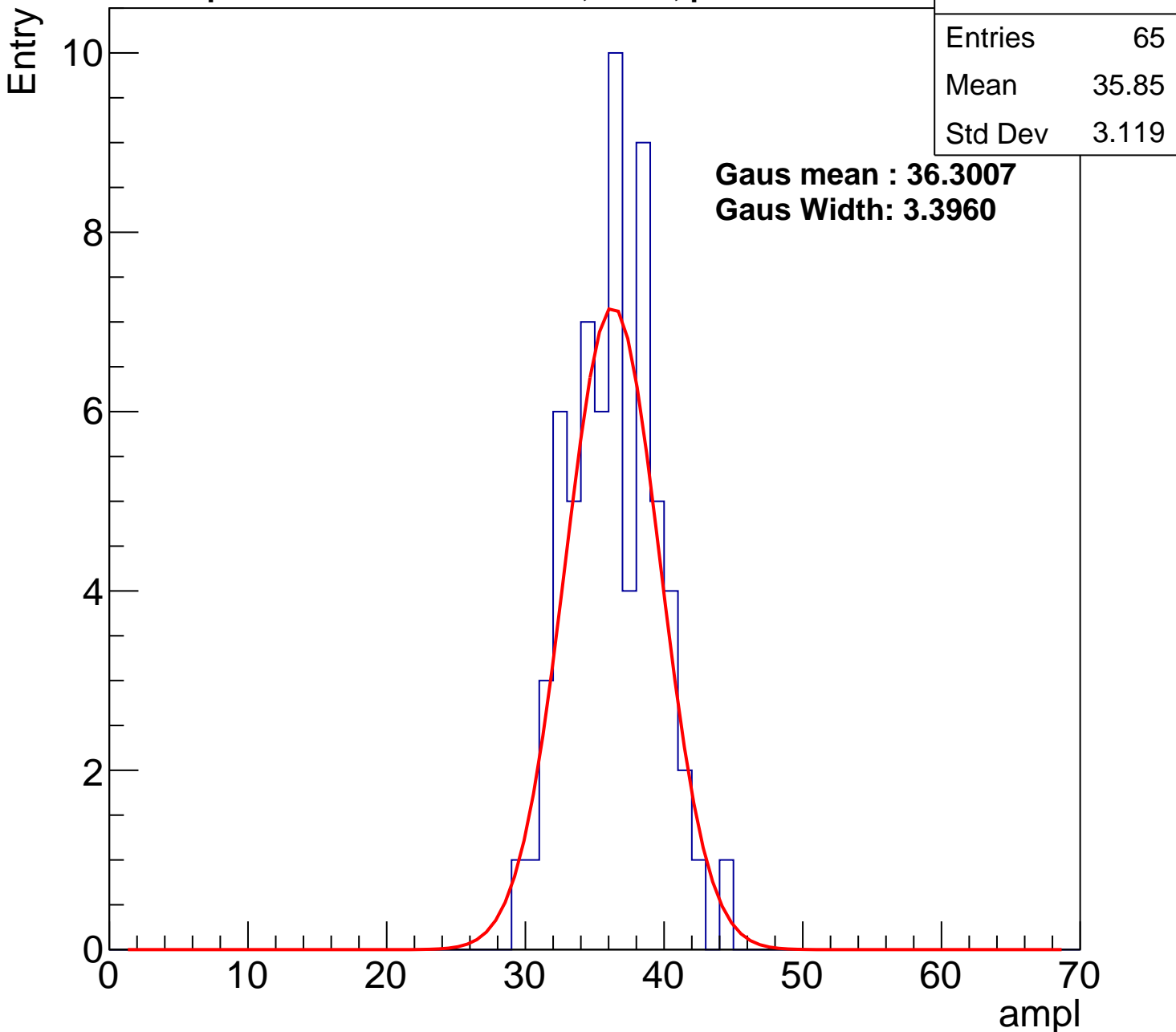
**Gaus Width: 3.3960**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch60, adc2

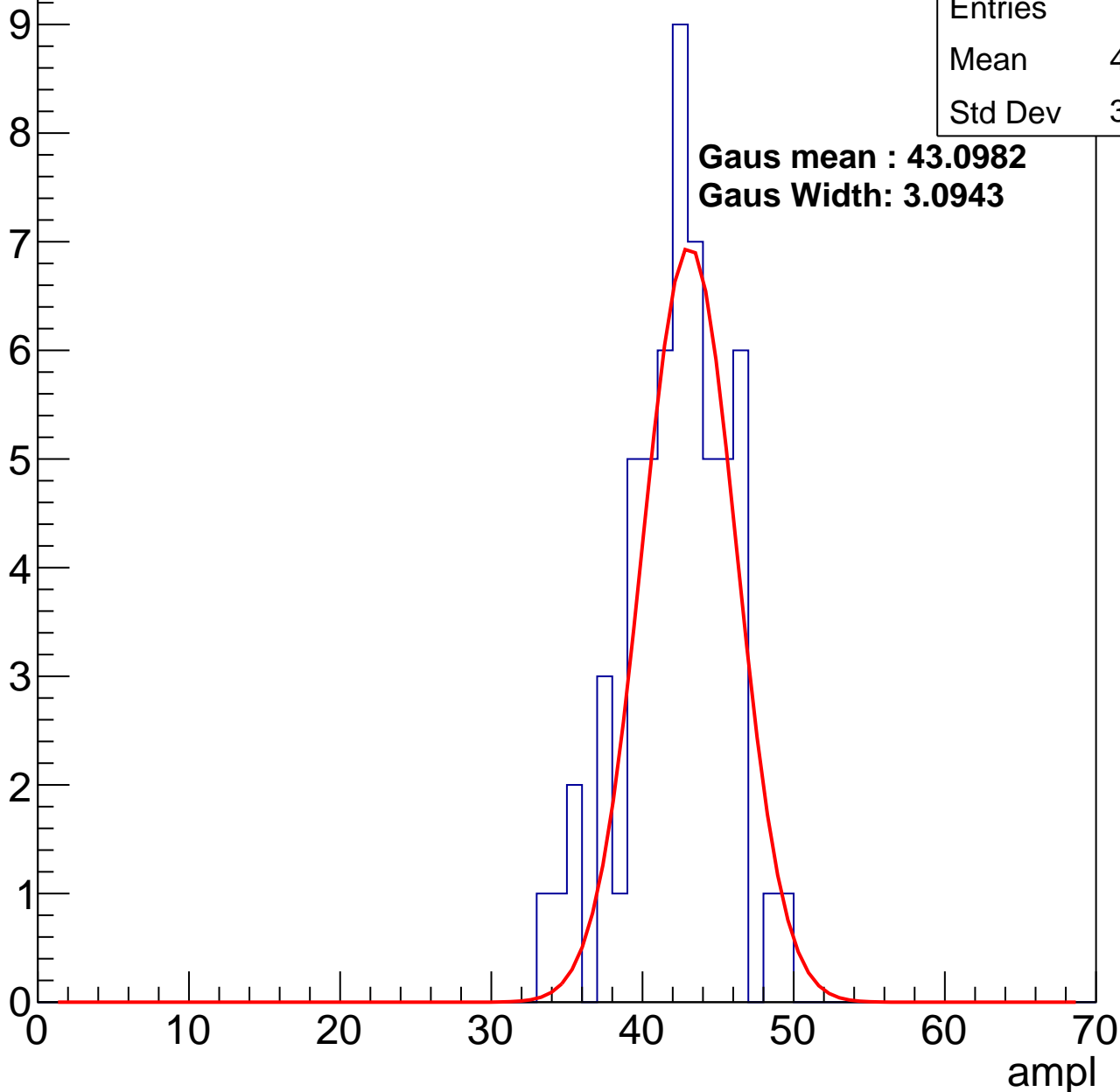
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	41.79
Std Dev	3.362

**Gaus mean : 43.0982**

**Gaus Width: 3.0943**

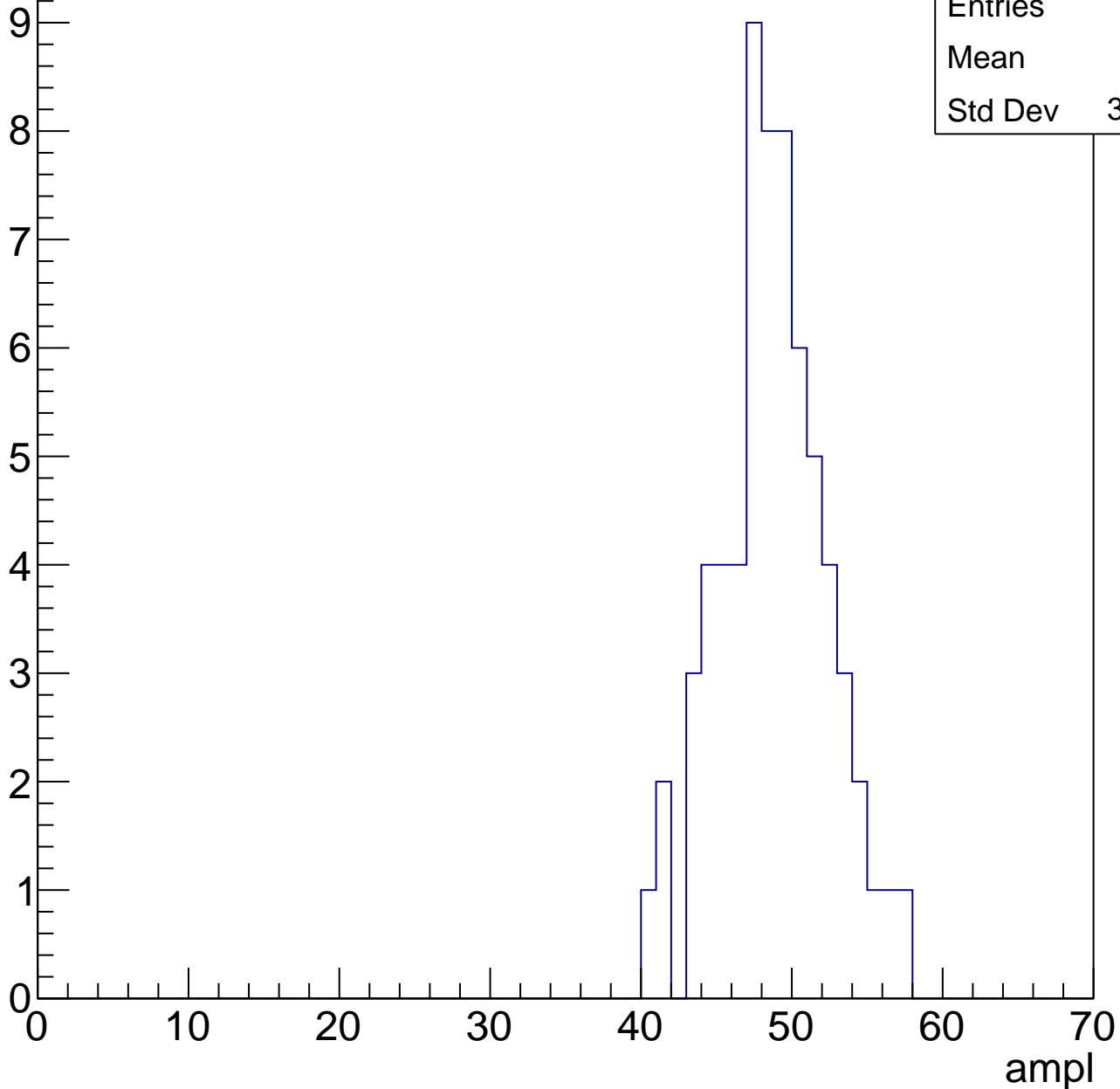


# B1L101S, U16-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

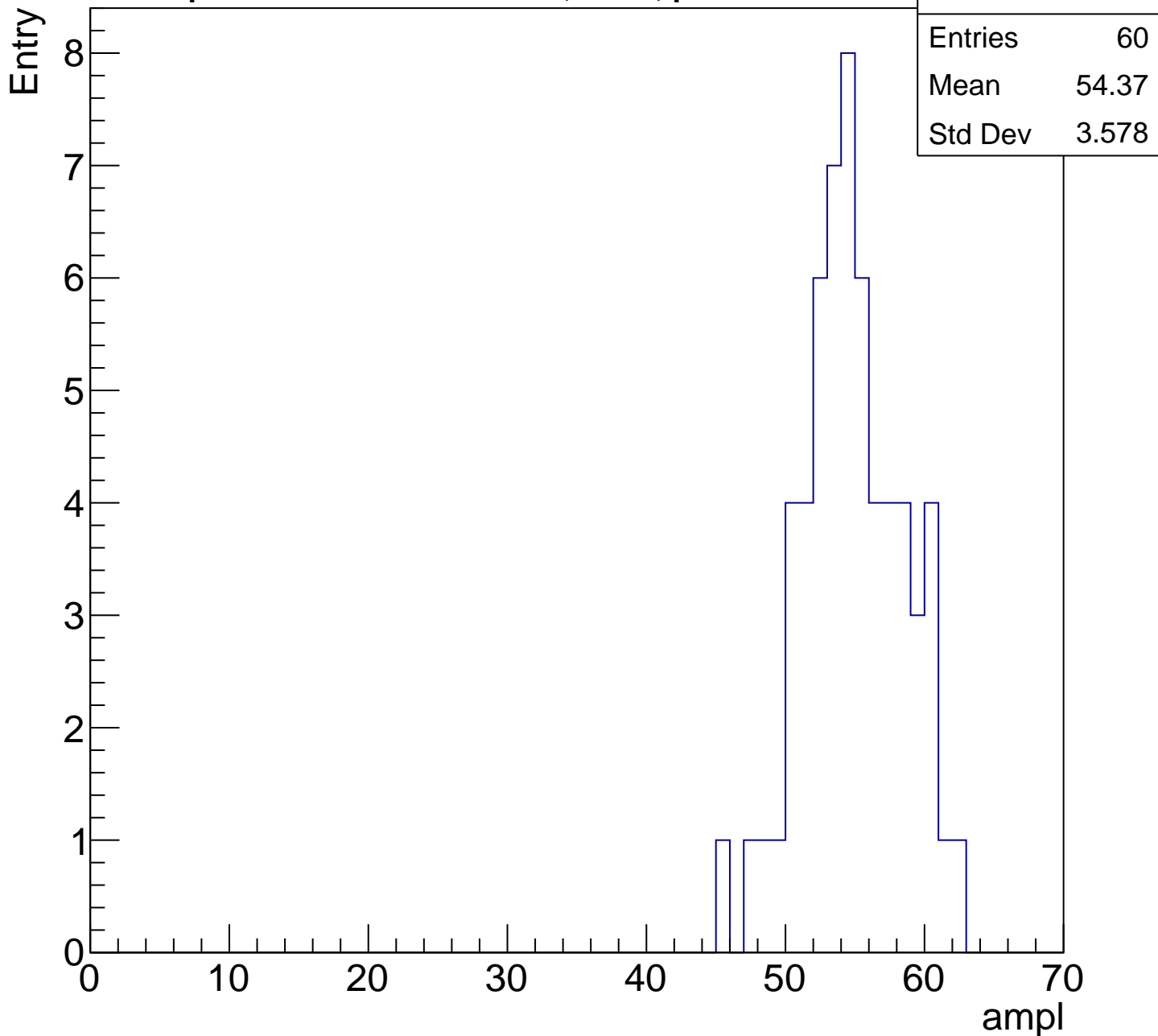
Entry

Entries	66
Mean	48.3
Std Dev	3.563



# B1L101S, U16-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

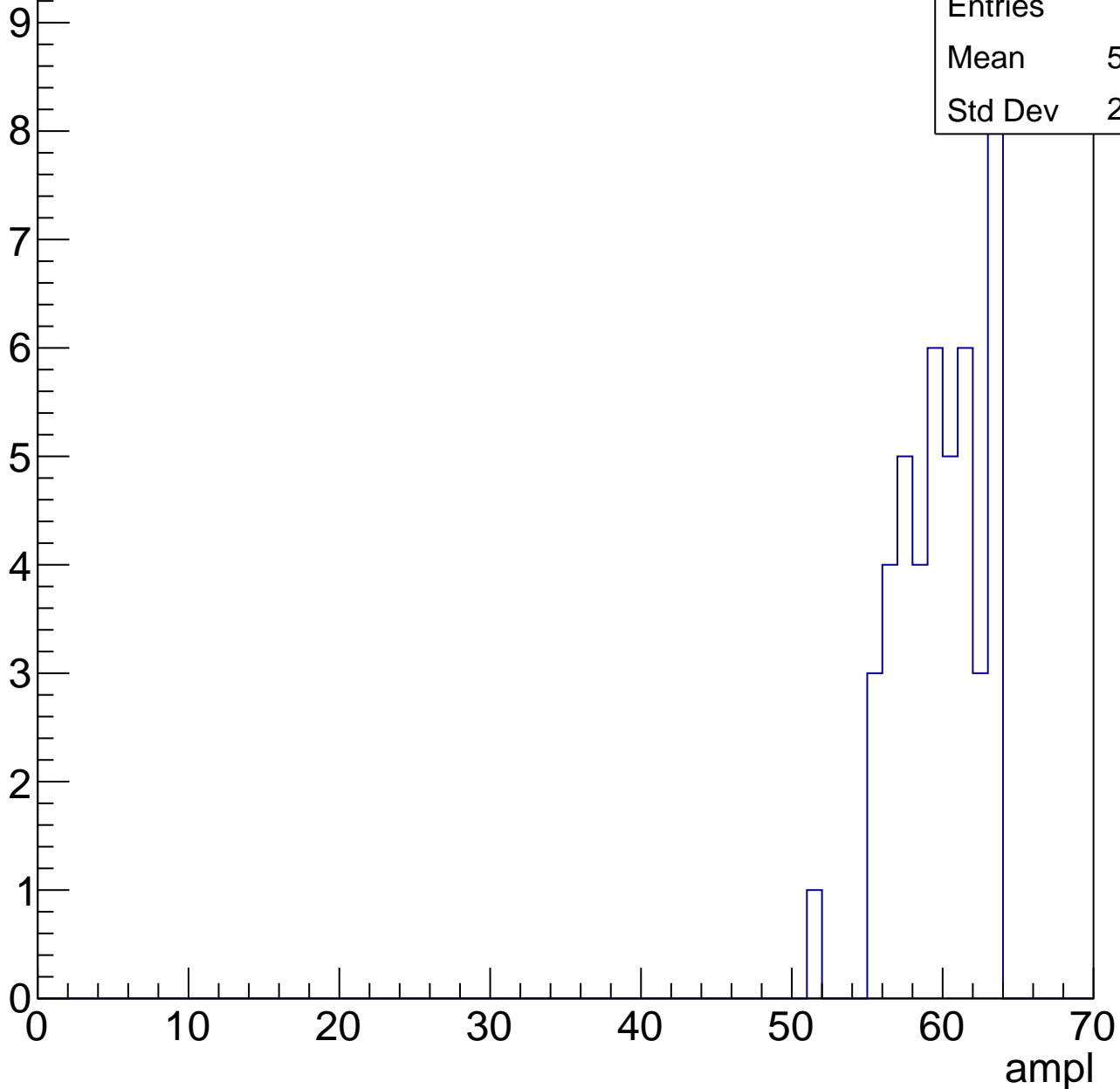


# B1L101S, U16-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	59.35
Std Dev	2.822

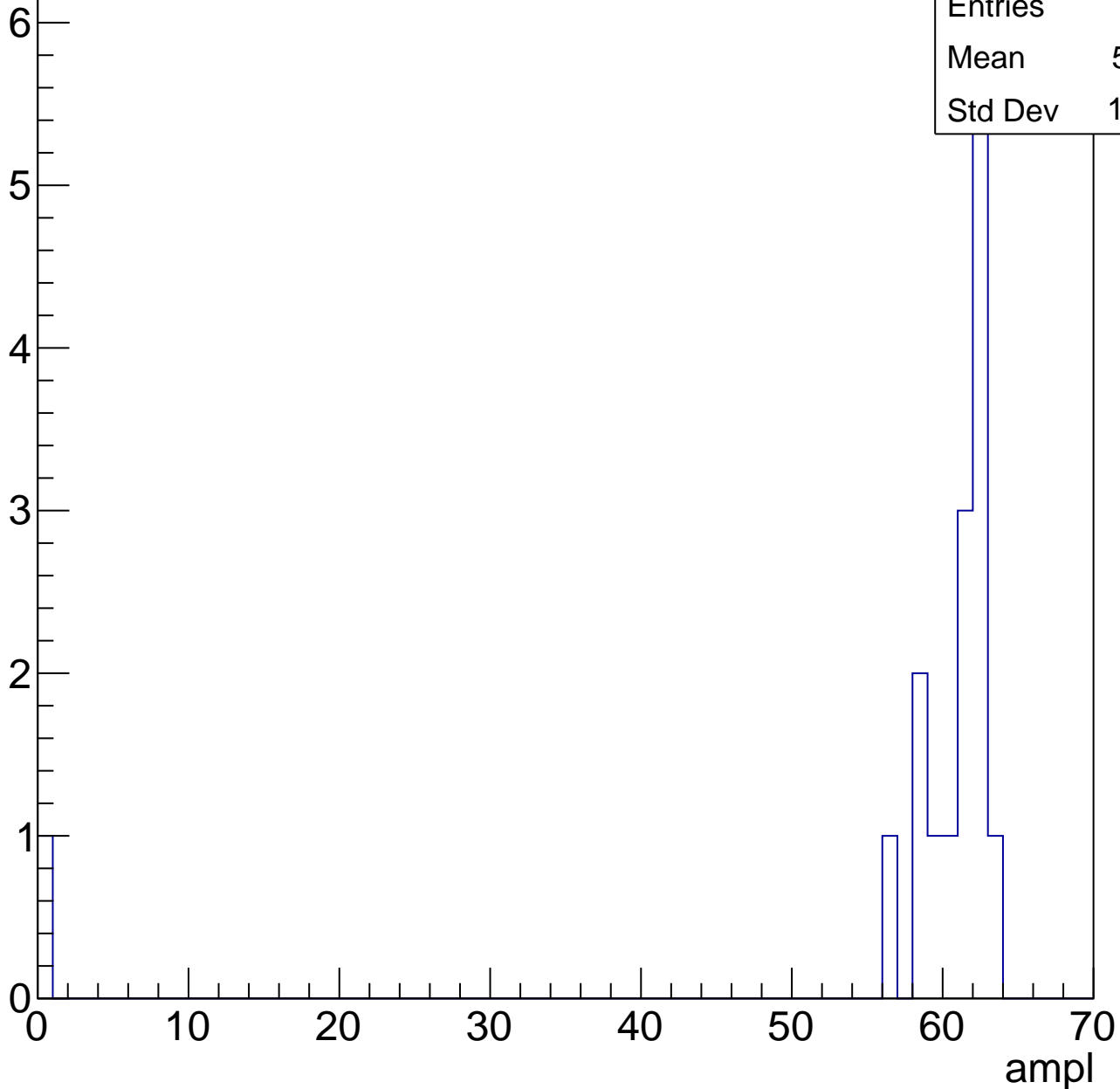


# B1L101S, U16-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	16
Mean	56.81
Std Dev	14.79





# B1L101S, U16-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U16-ch61, adc0

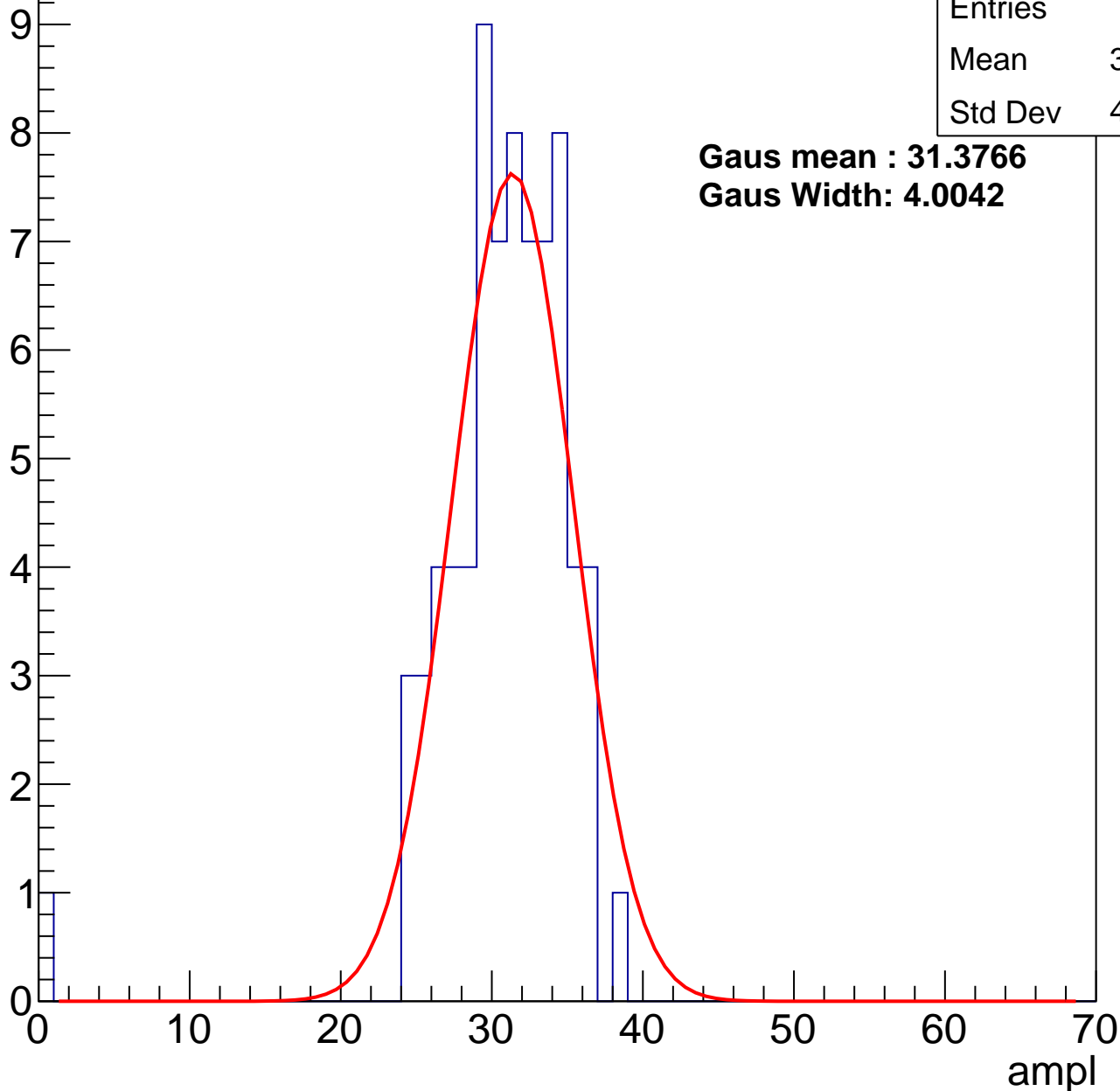
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	30.26
Std Dev	4.846

**Gaus mean : 31.3766**

**Gaus Width: 4.0042**



# B1L101S, U16-ch61, adc1

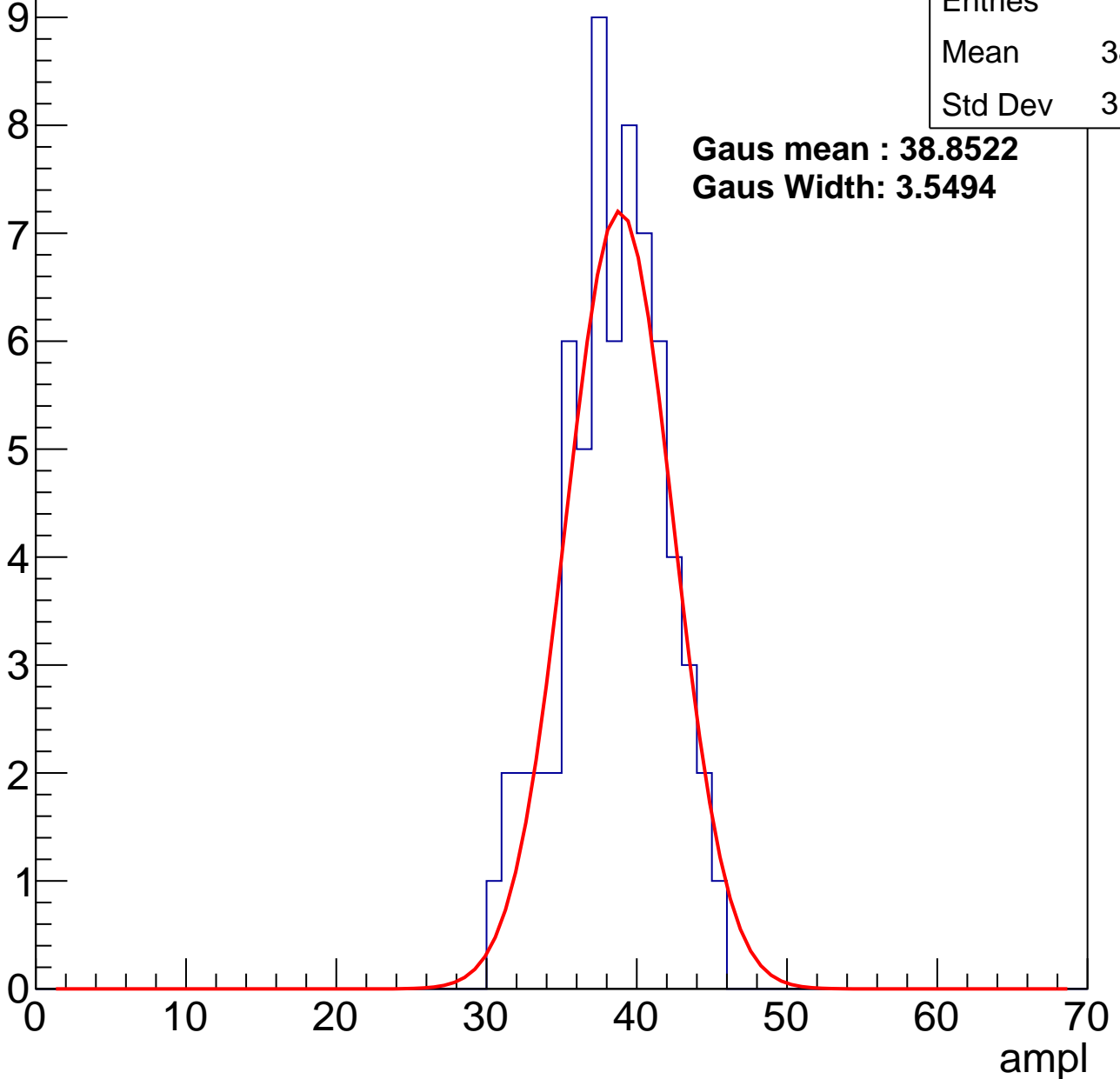
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	38.02
Std Dev	3.369

**Gaus mean : 38.8522**

**Gaus Width: 3.5494**

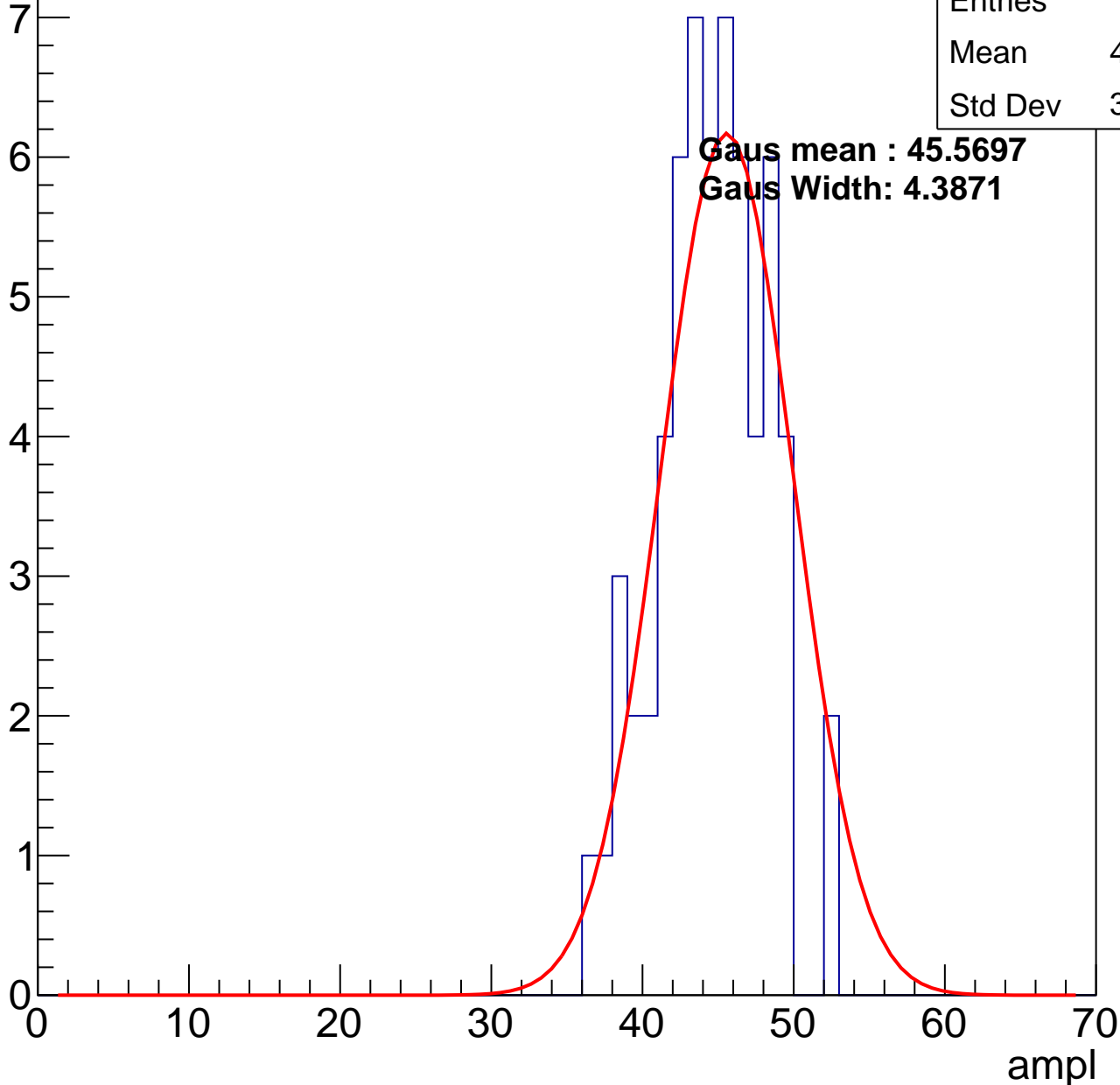


# B1L101S, U16-ch61, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	44.15
Std Dev	3.529



# B1L101S, U16-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

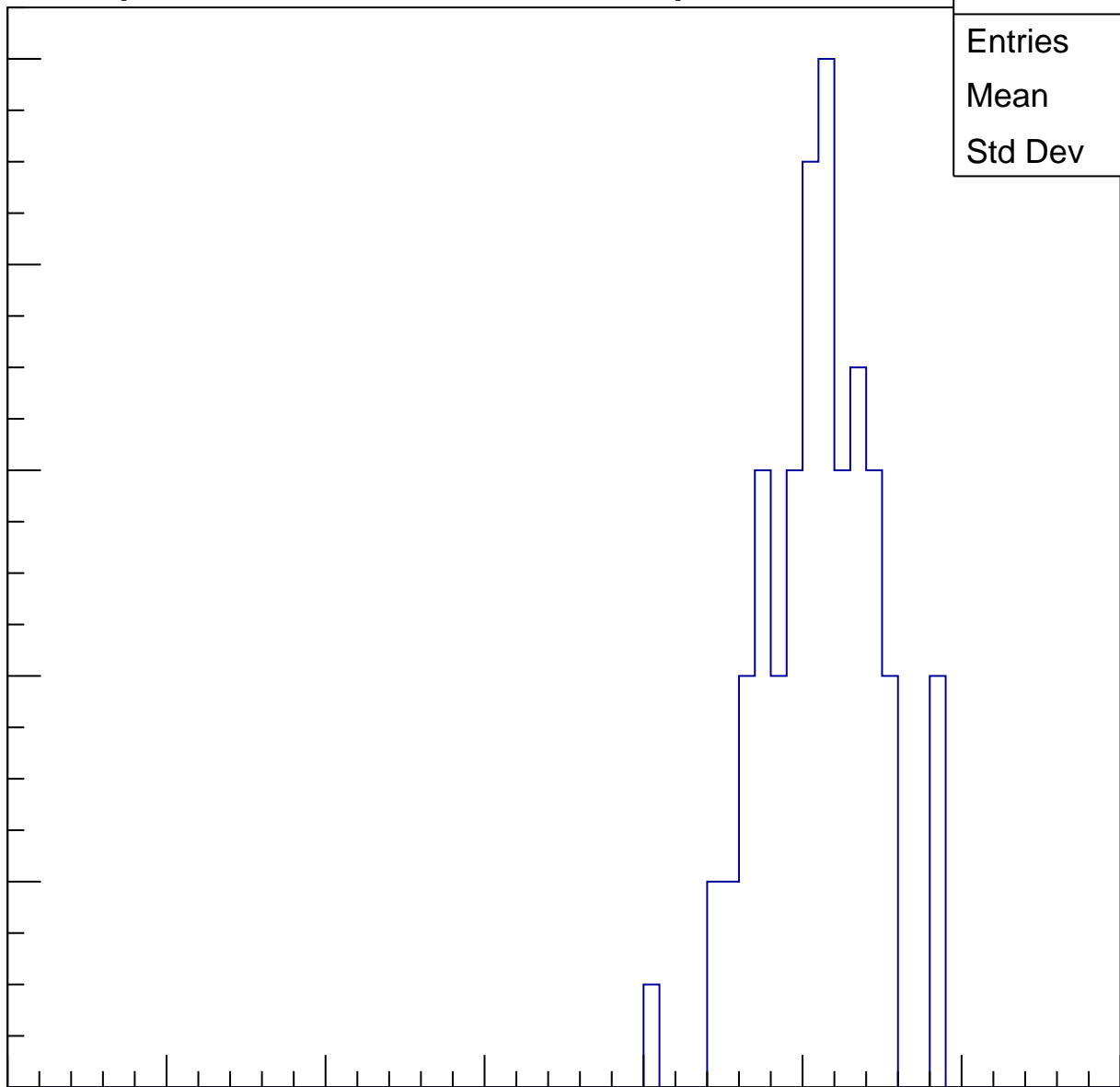
Entries	71
Mean	50.55
Std Dev	3.54

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

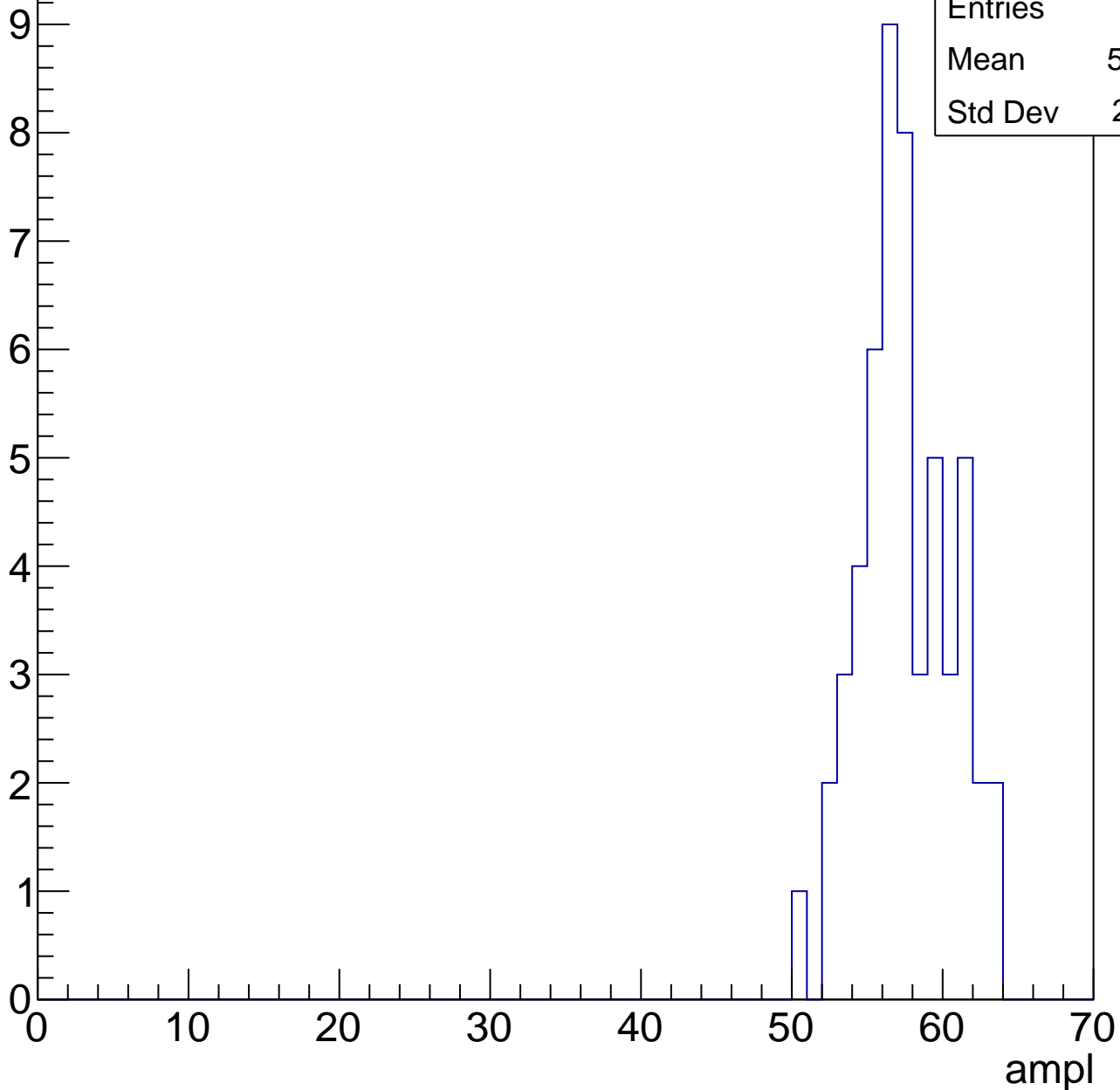


# B1L101S, U16-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	57.04
Std Dev	2.971

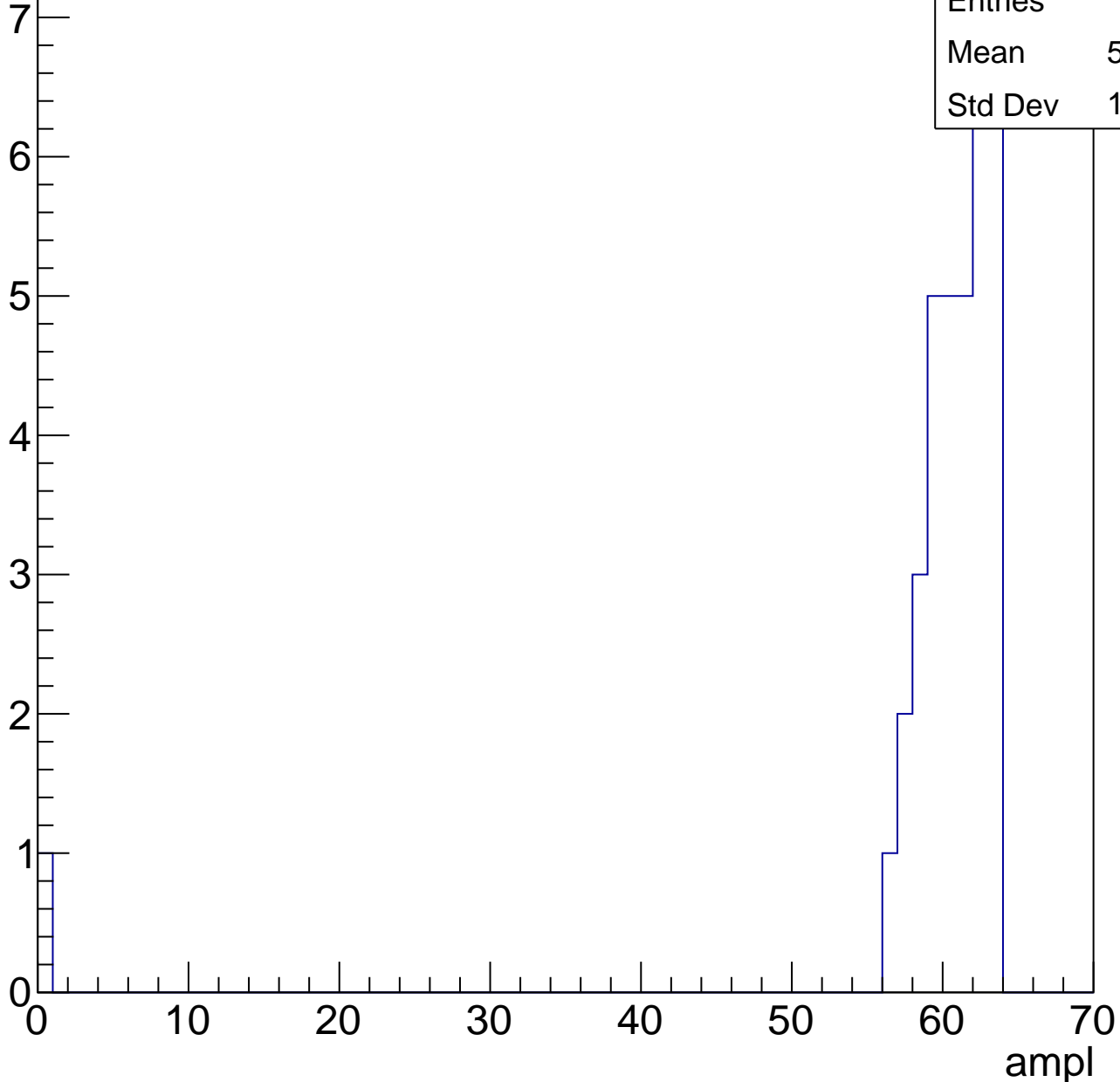


# B1L101S, U16-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

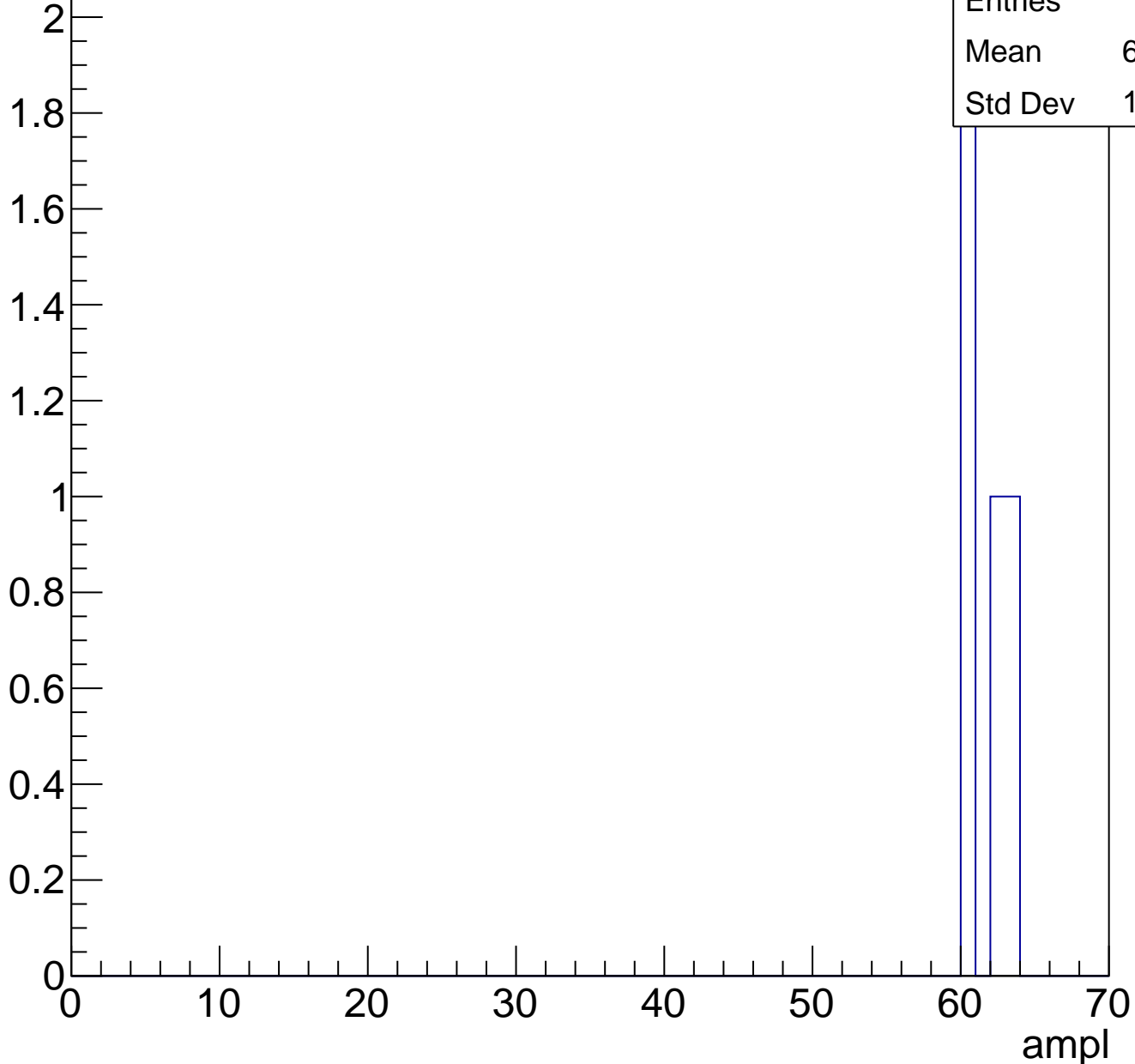
Entries	36
Mean	58.86
Std Dev	10.14



# B1L101S, U16-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch62, adc0

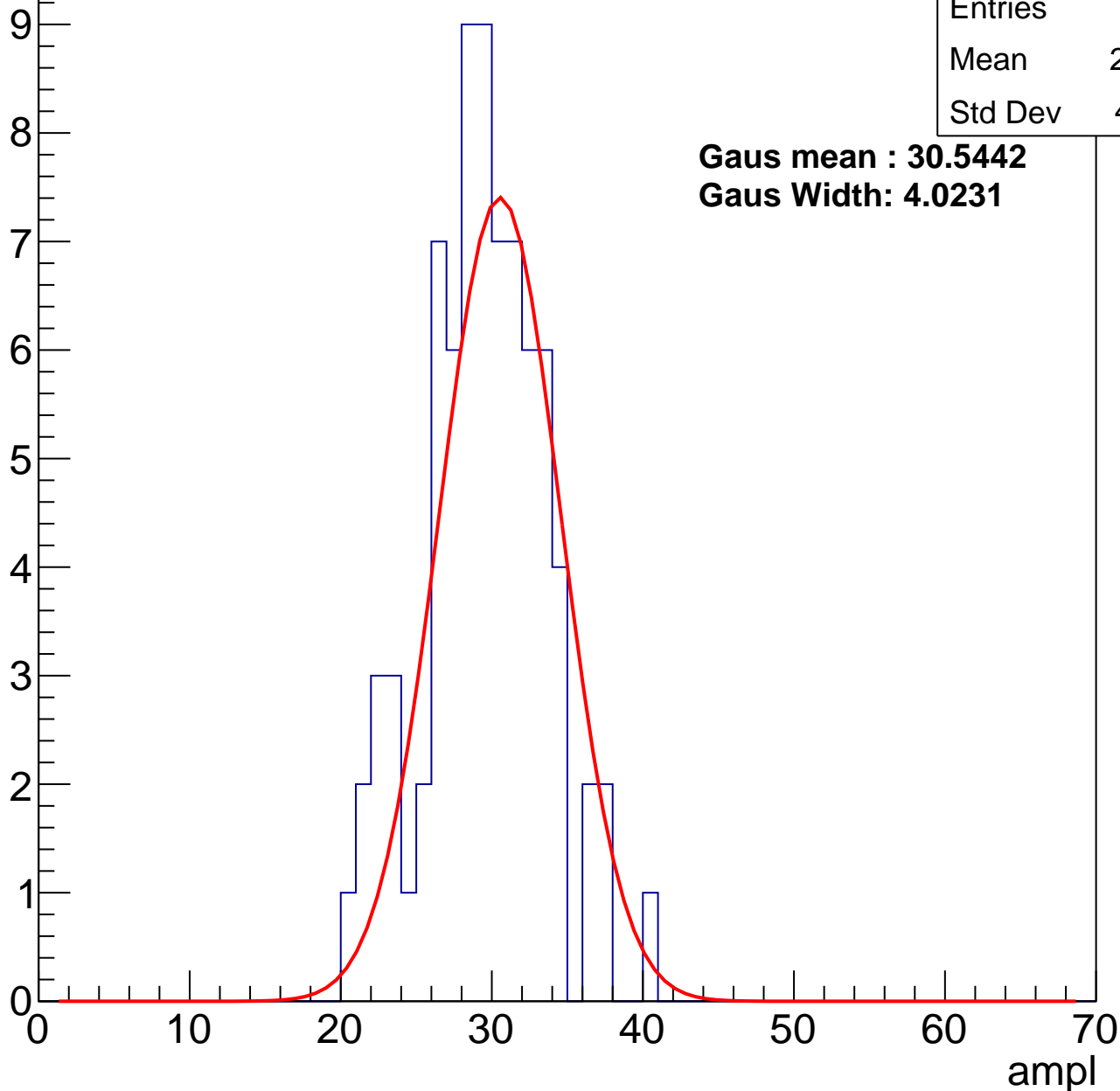
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	29.06
Std Dev	4.001

**Gaus mean : 30.5442**

**Gaus Width: 4.0231**



# B1L101S, U16-ch62, adc1

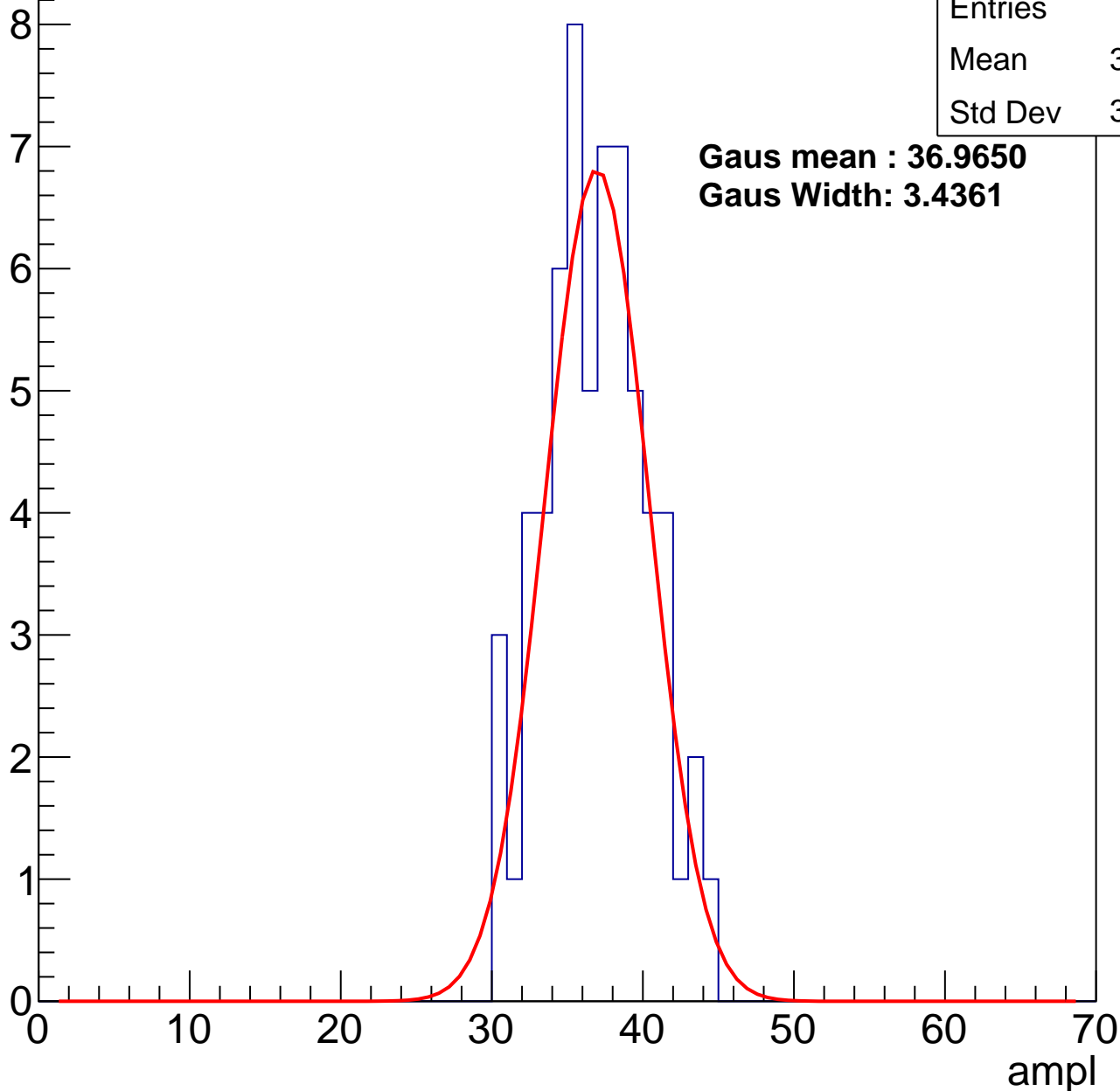
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	36.47
Std Dev	3.344

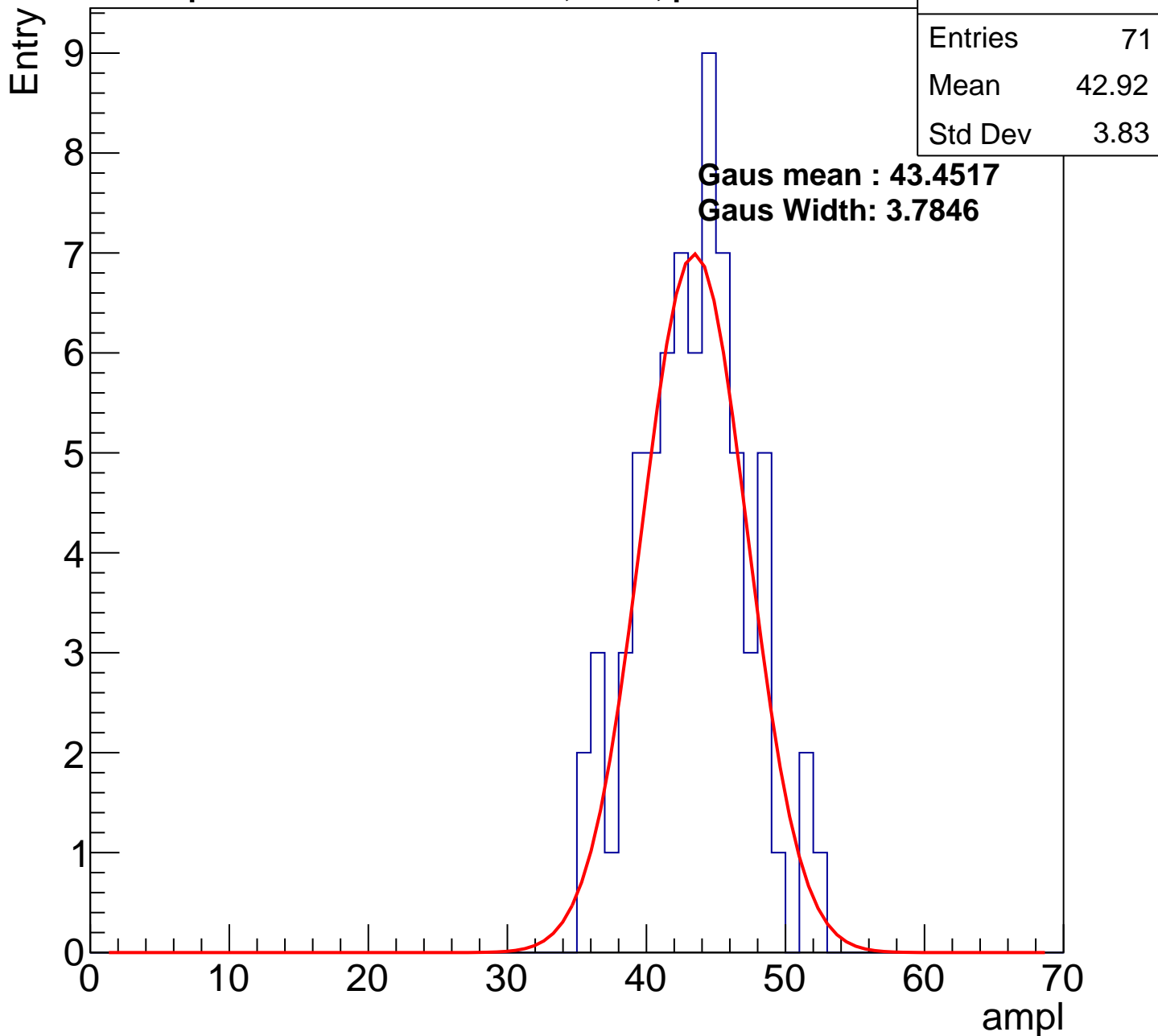
**Gaus mean : 36.9650**

**Gaus Width: 3.4361**



# B1L101S, U16-ch62, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

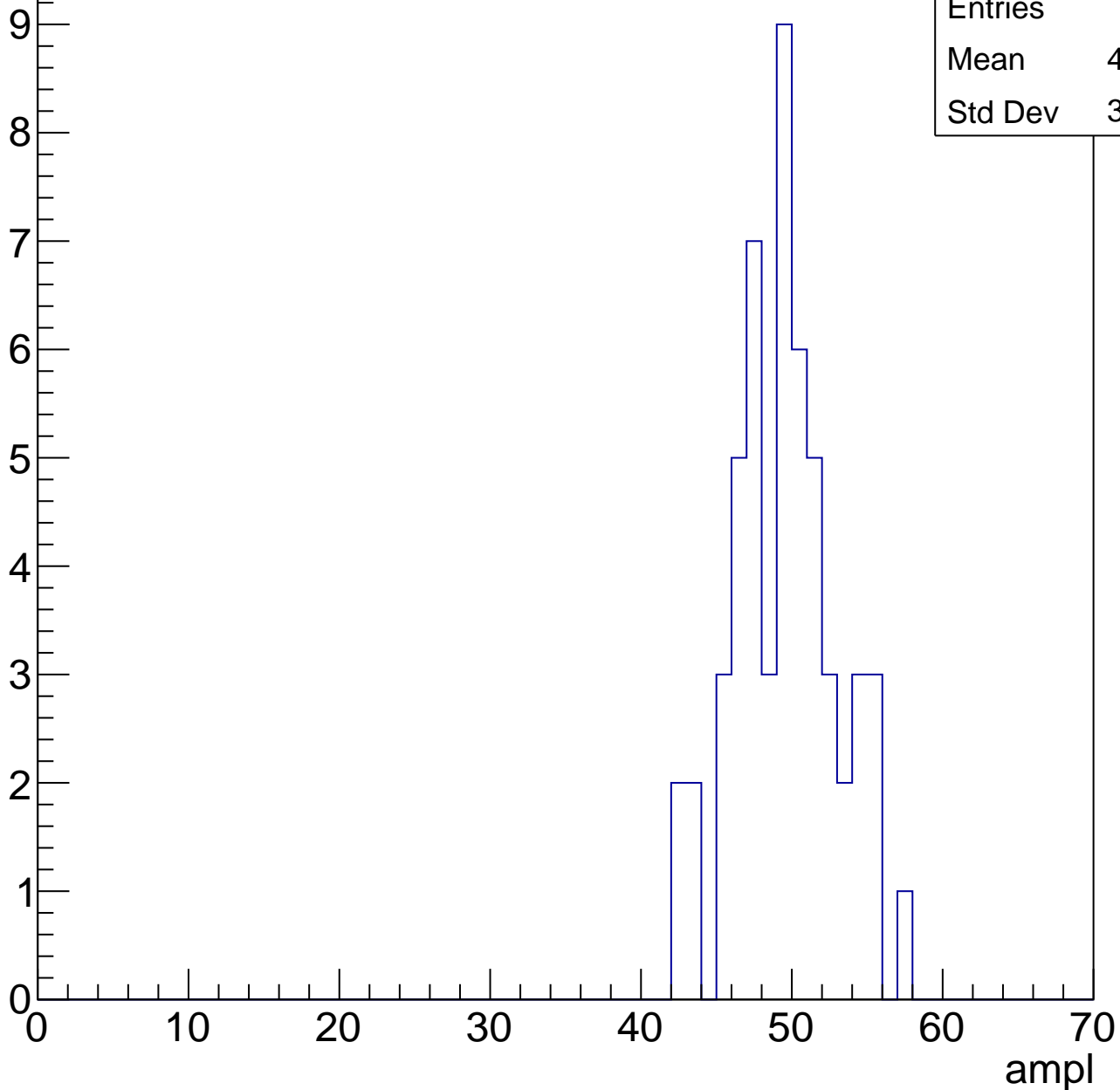


# B1L101S, U16-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	49.07
Std Dev	3.404

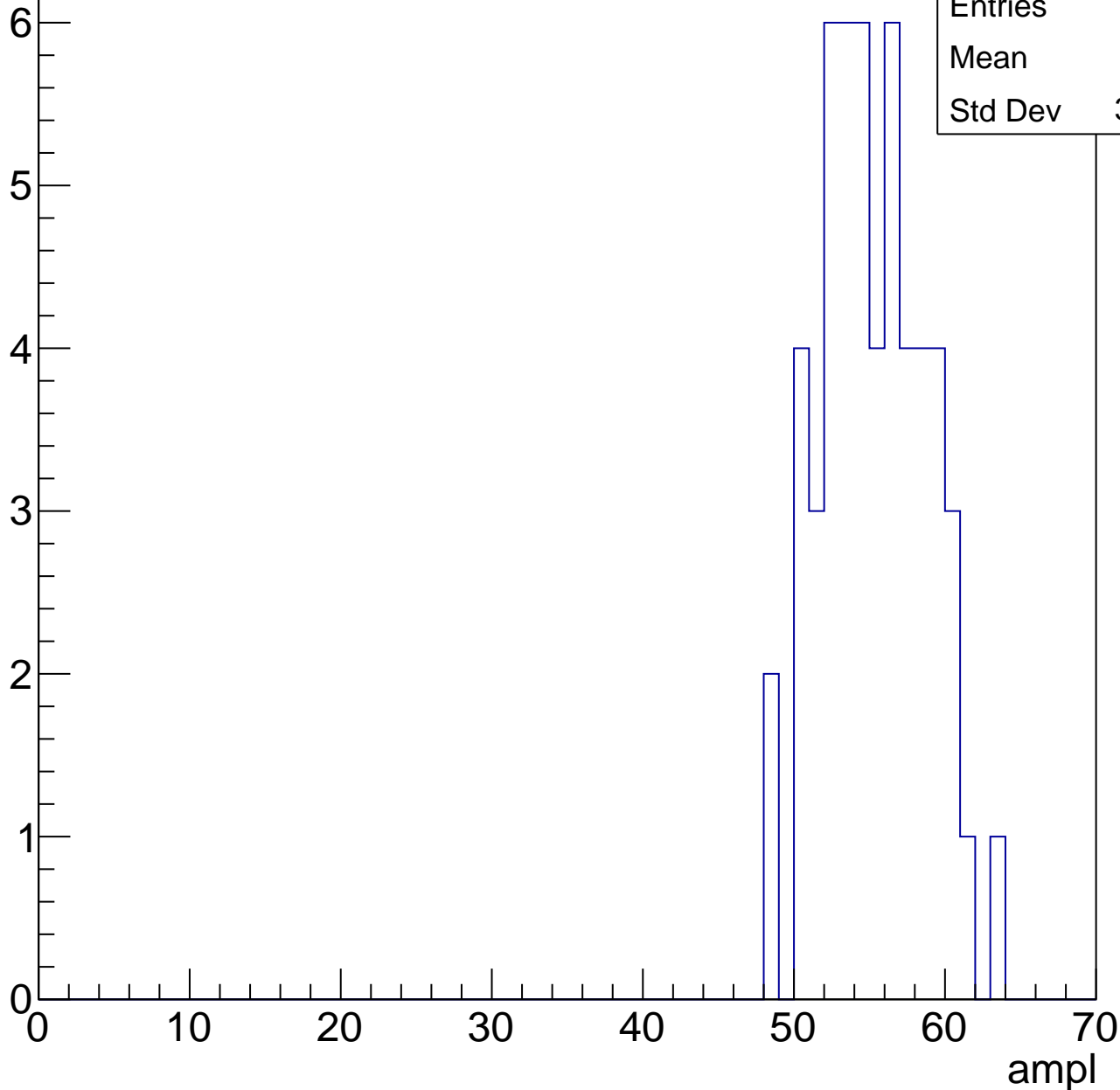


# B1L101S, U16-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

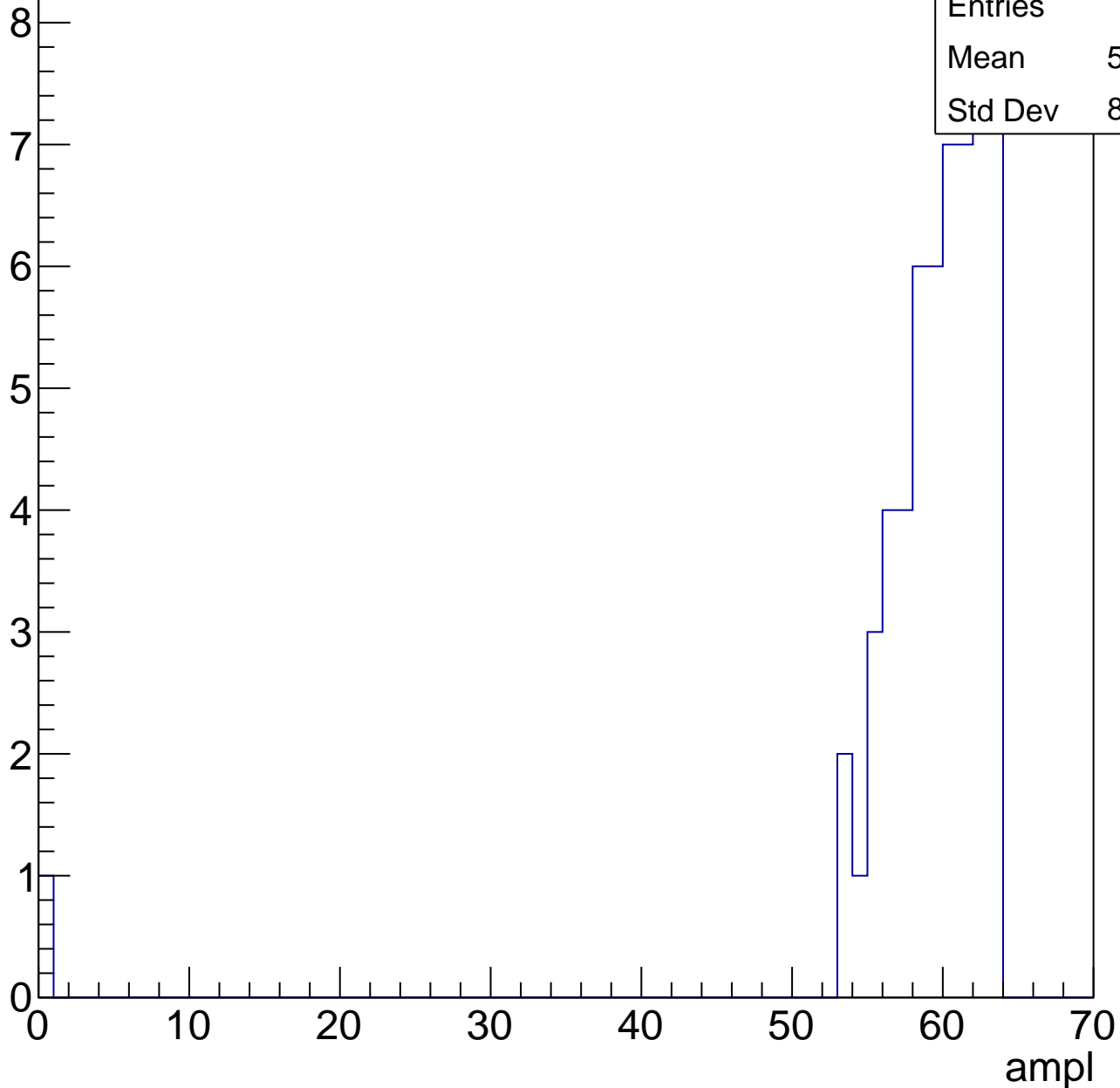
Entries	54
Mean	54.8
Std Dev	3.401



# B1L101S, U16-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

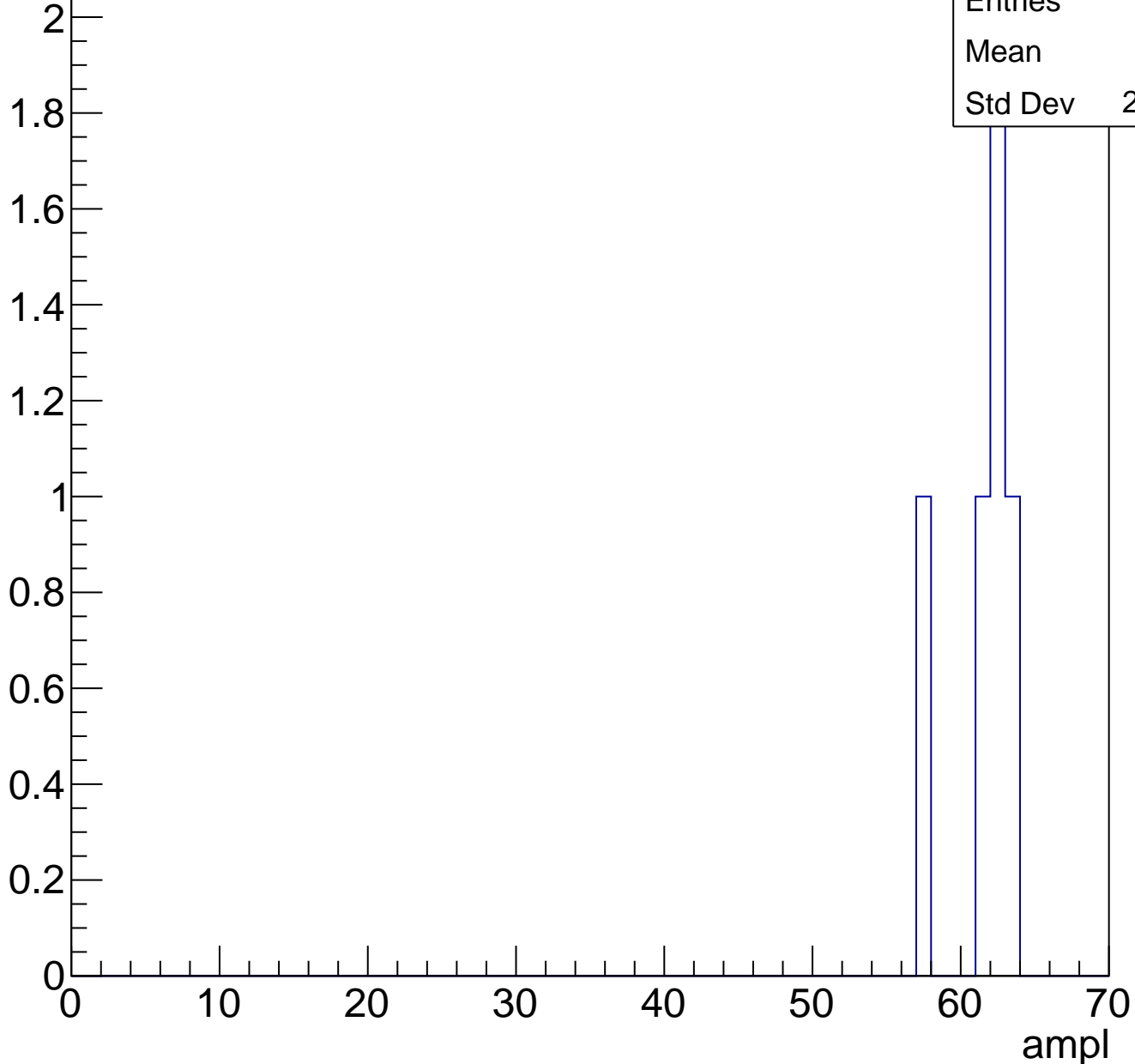
Entry



# B1L101S, U16-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

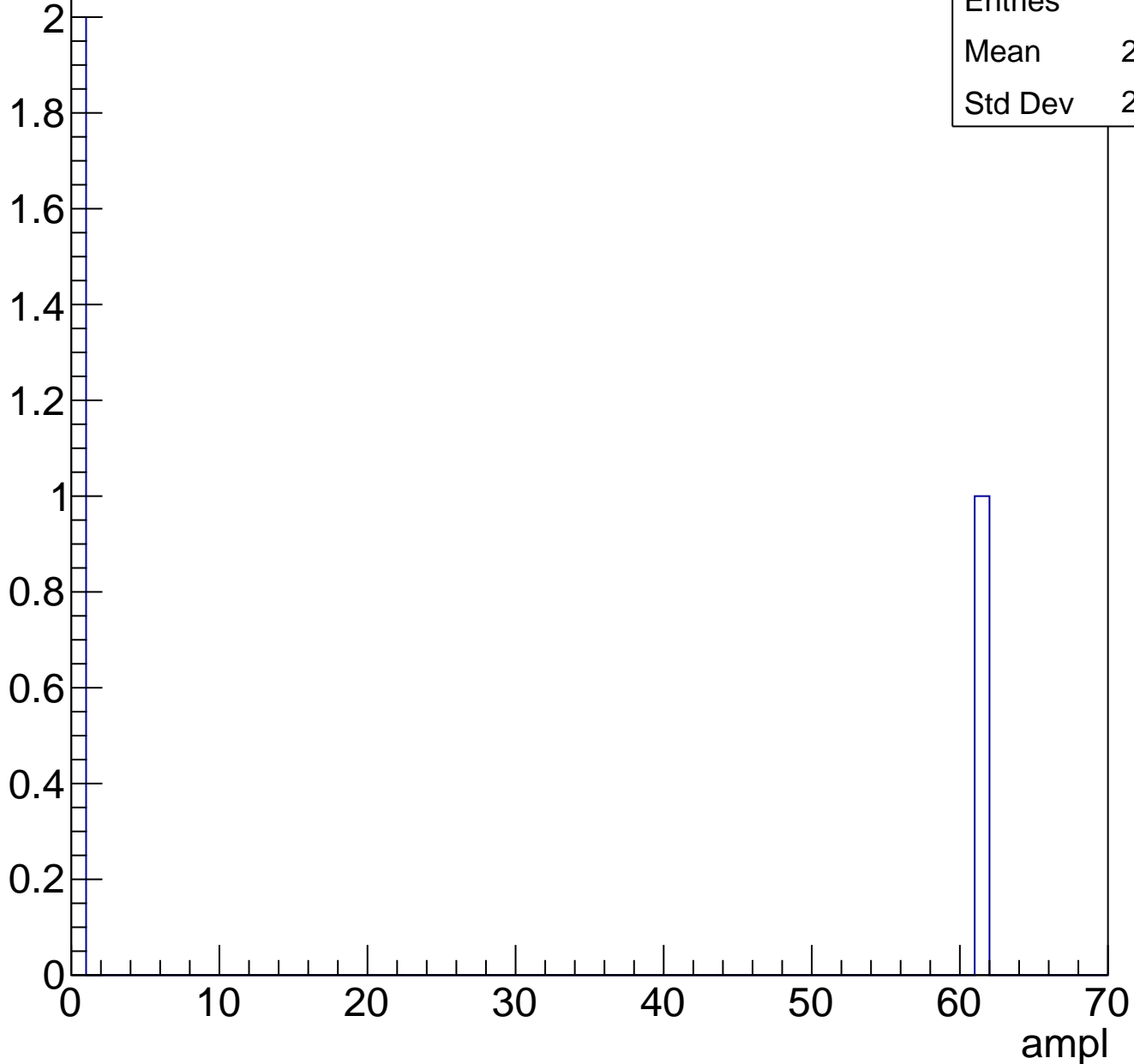




# B1L101S, U16-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch63, adc0

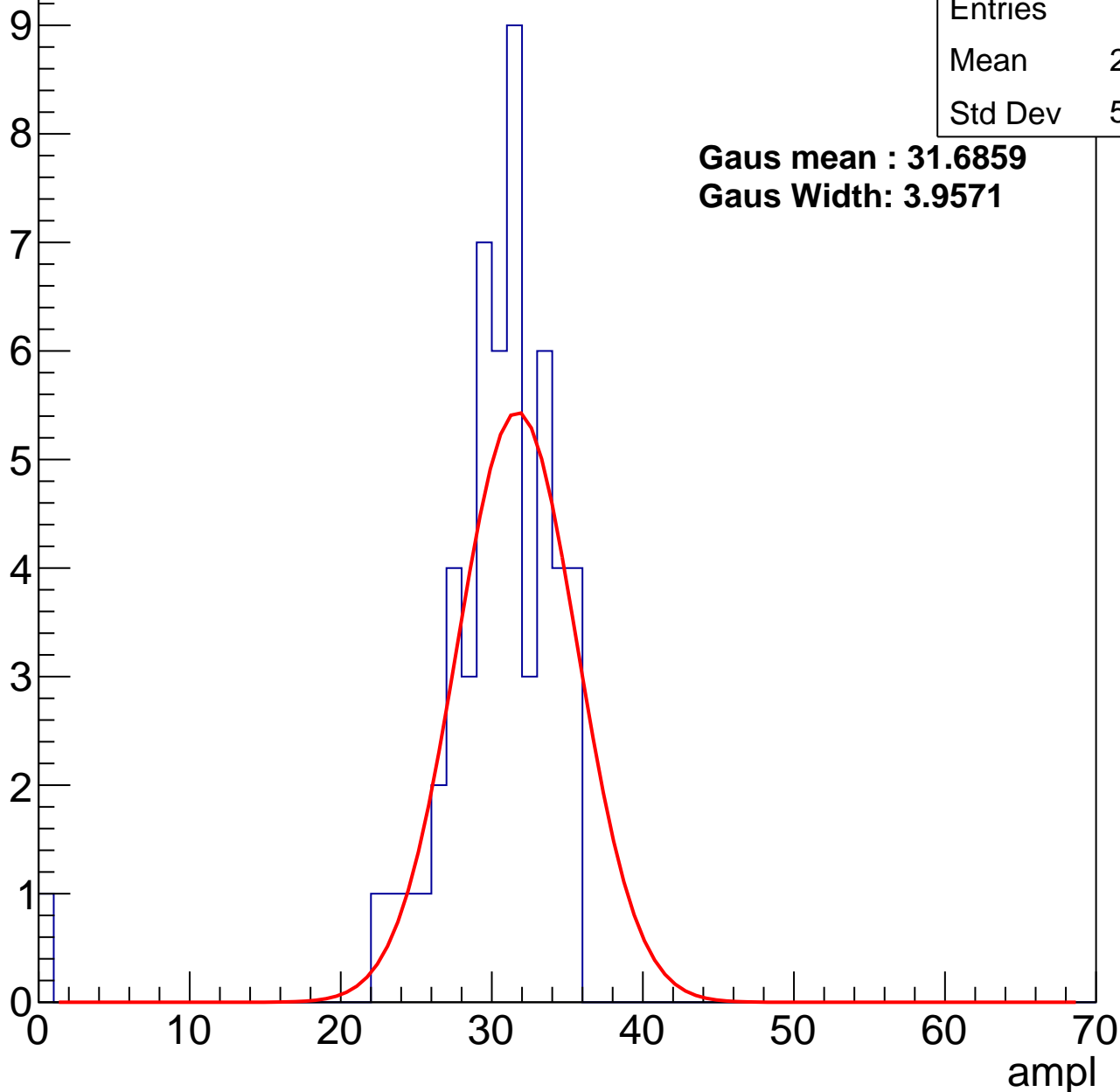
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	29.62
Std Dev	5.126

**Gaus mean : 31.6859**

**Gaus Width: 3.9571**



# B1L101S, U16-ch63, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	72
Mean	36.74
Std Dev	4.14

**Gaus mean : 37.4289**

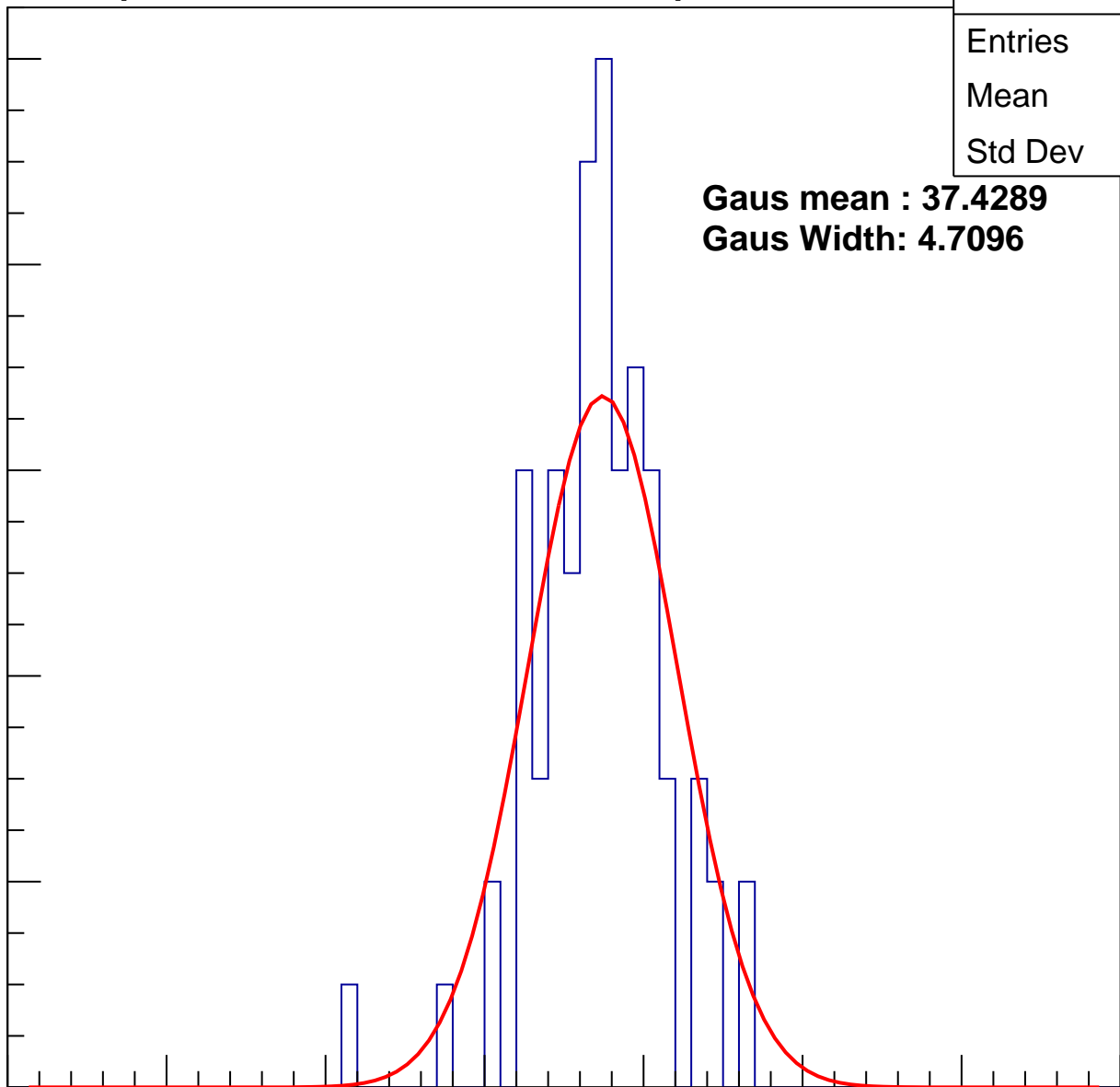
**Gaus Width: 4.7096**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

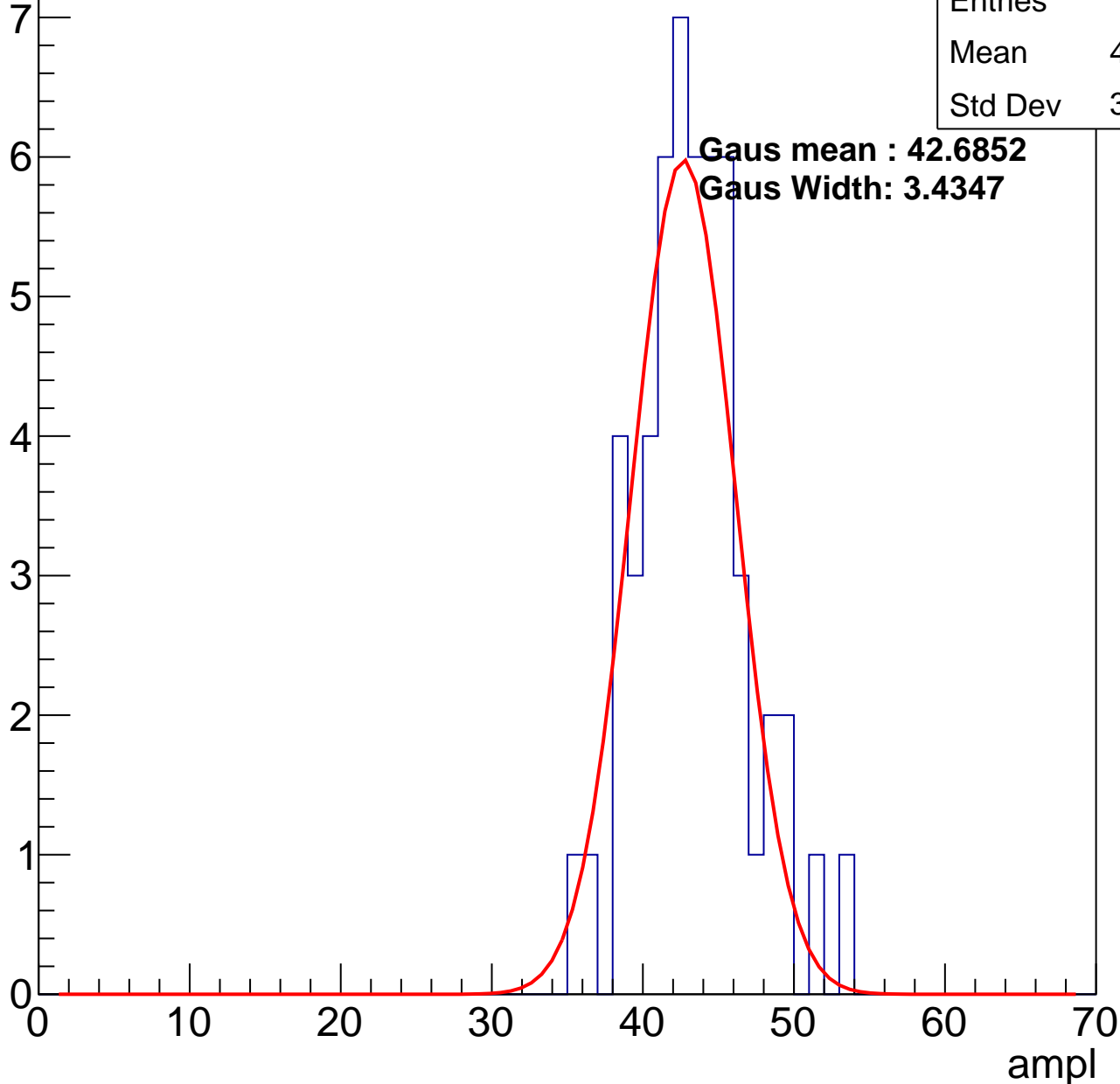


# B1L101S, U16-ch63, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	42.87
Std Dev	3.564



# B1L101S, U16-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	79
Mean	49.25
Std Dev	3.399

Entry

10

8

6

4

2

0

0

10

20

30

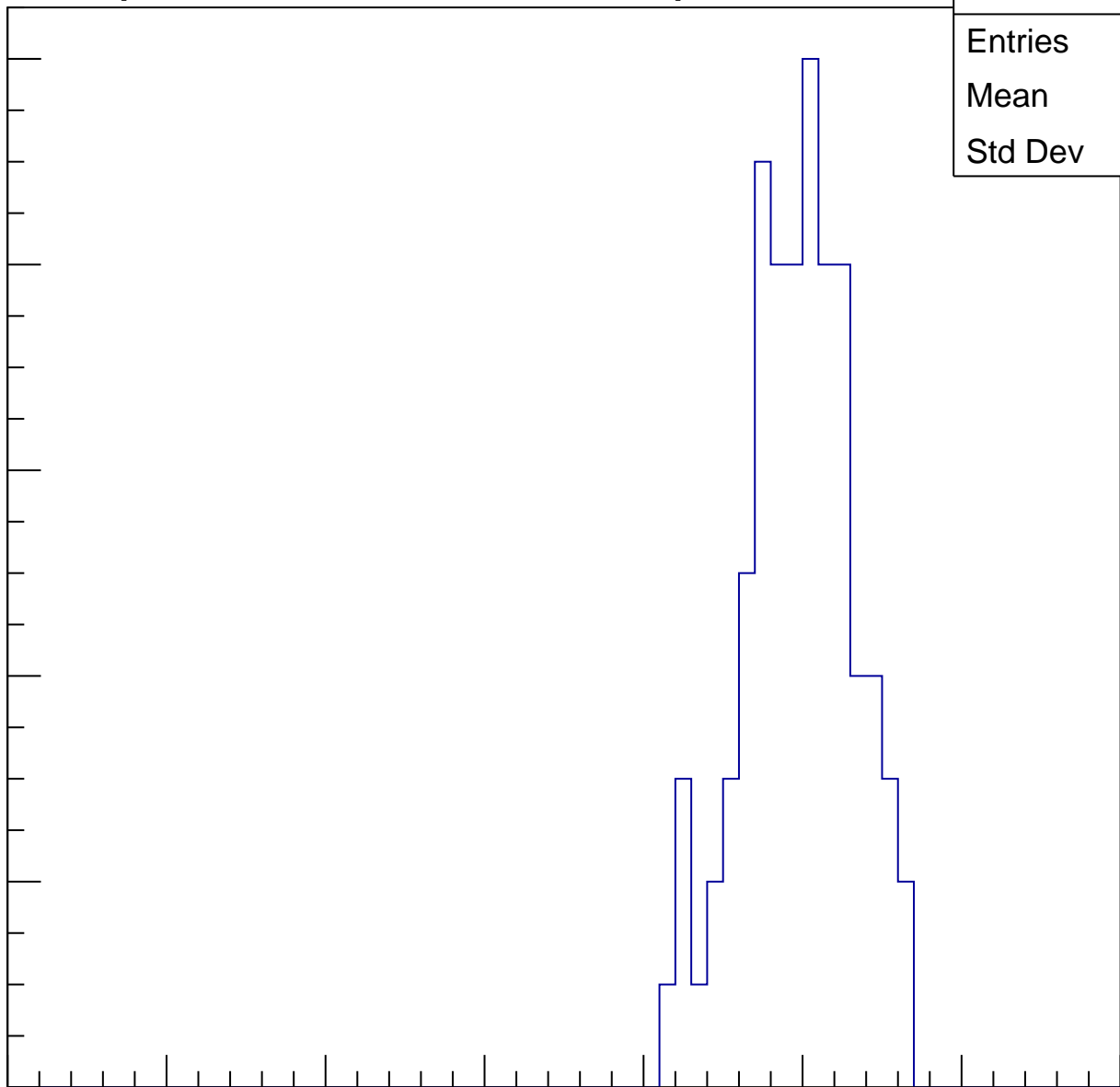
40

50

60

70

ampl

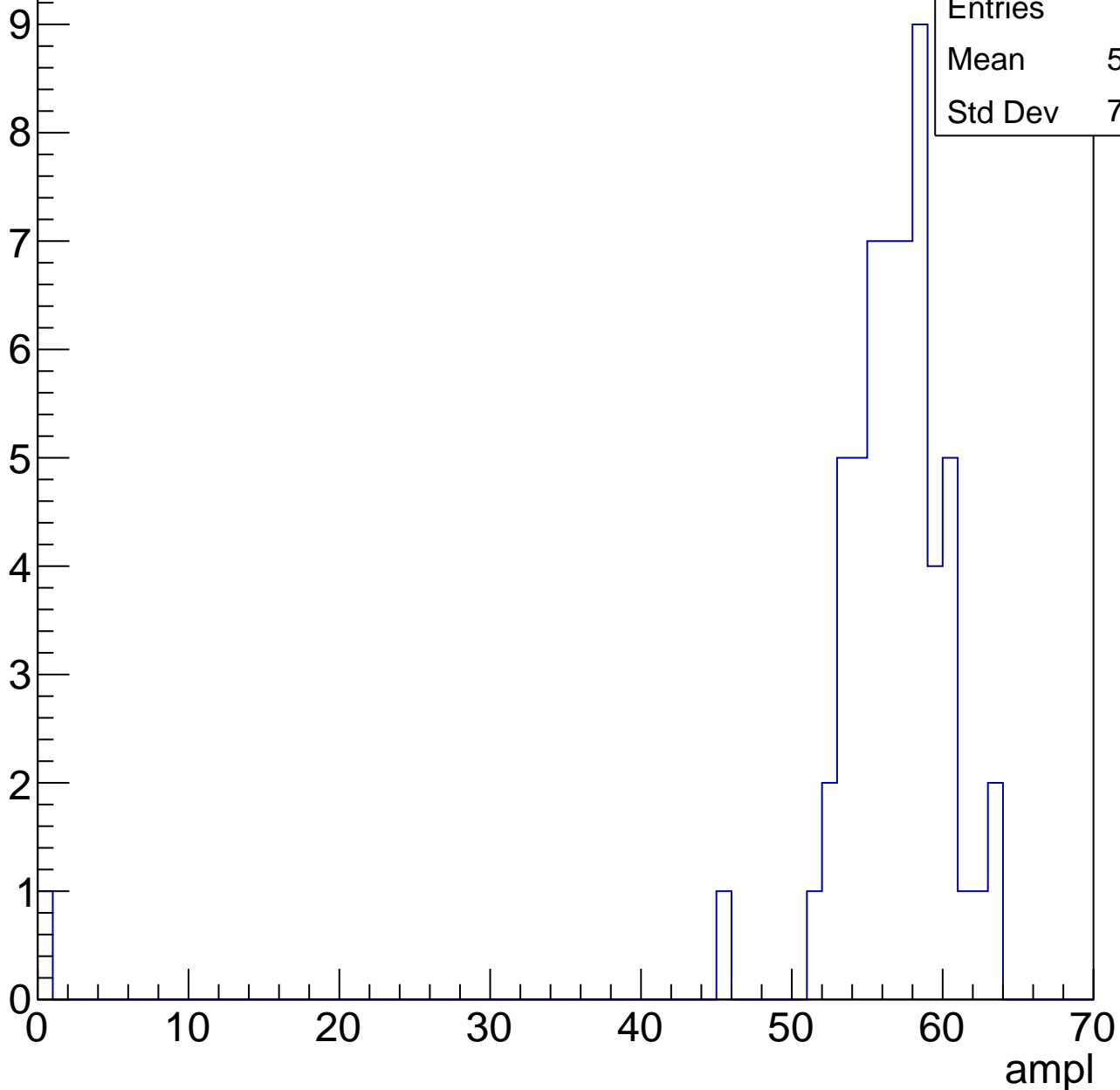


# B1L101S, U16-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	55.48
Std Dev	7.975

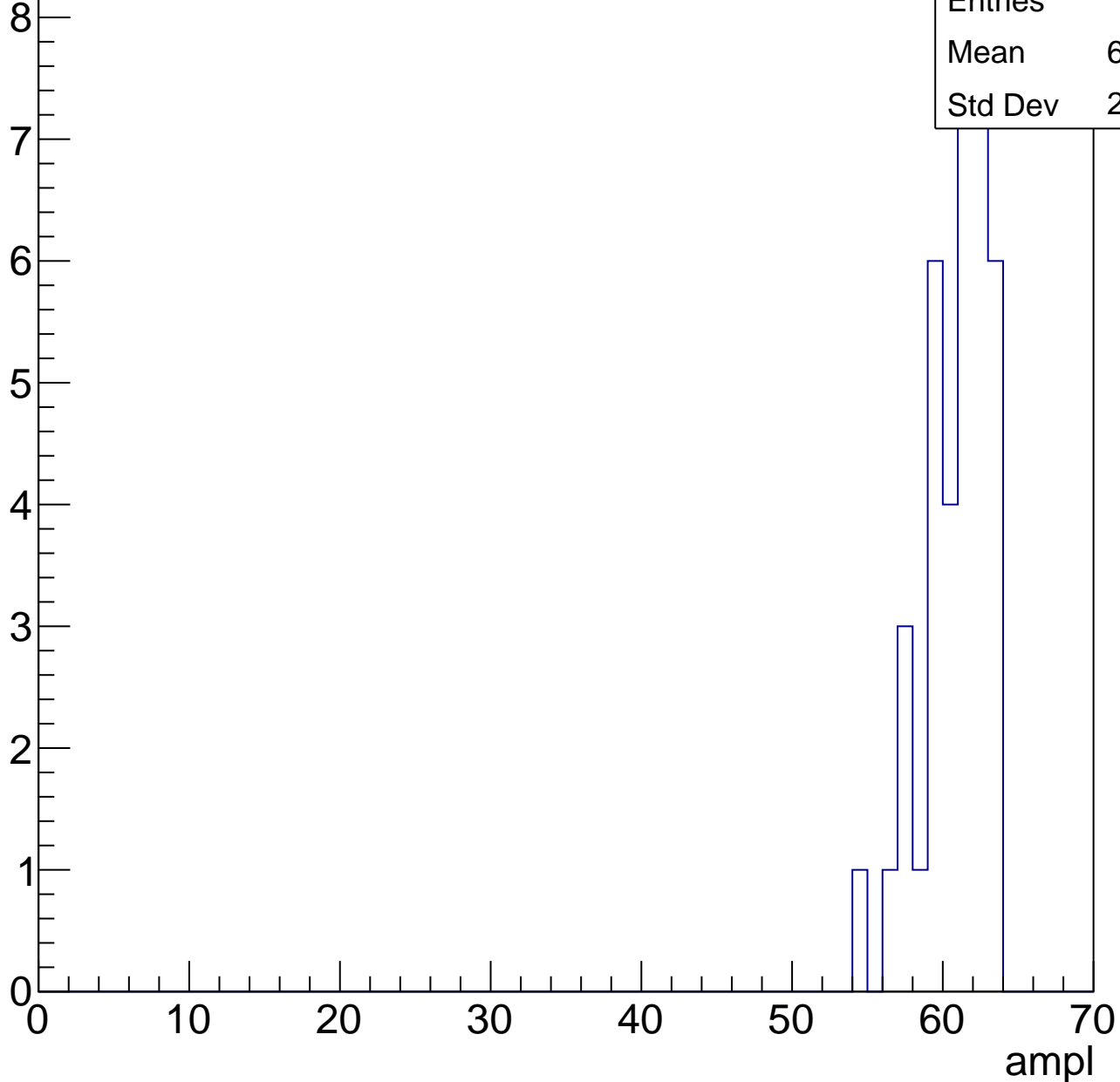


# B1L101S, U16-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	38
Mean	60.39
Std Dev	2.159



# B1L101S, U16-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

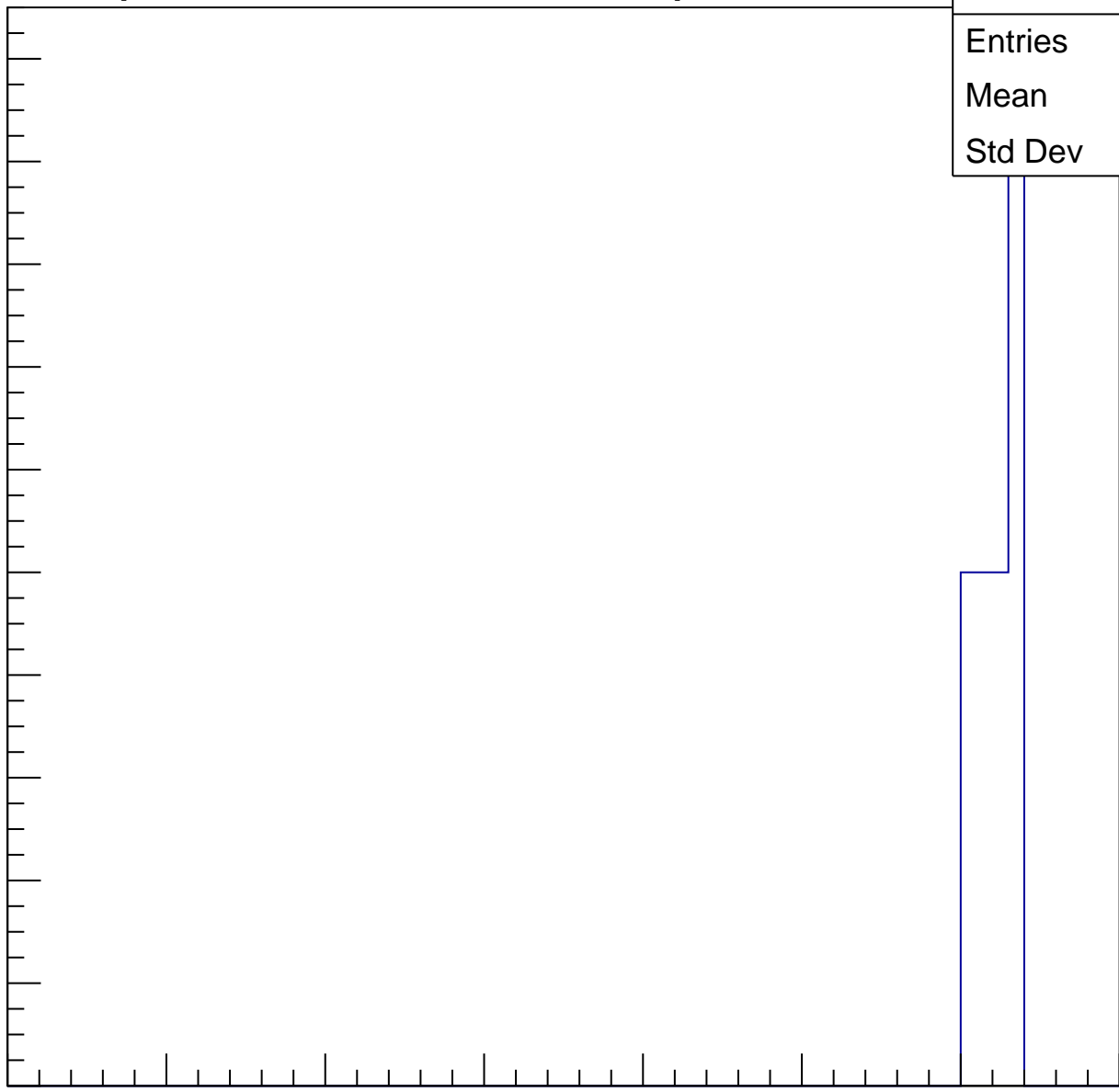
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	61.8
Std Dev	1.166

ampl

0 10 20 30 40 50 60 70





# B1L101S, U16-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U16-ch64, adc0

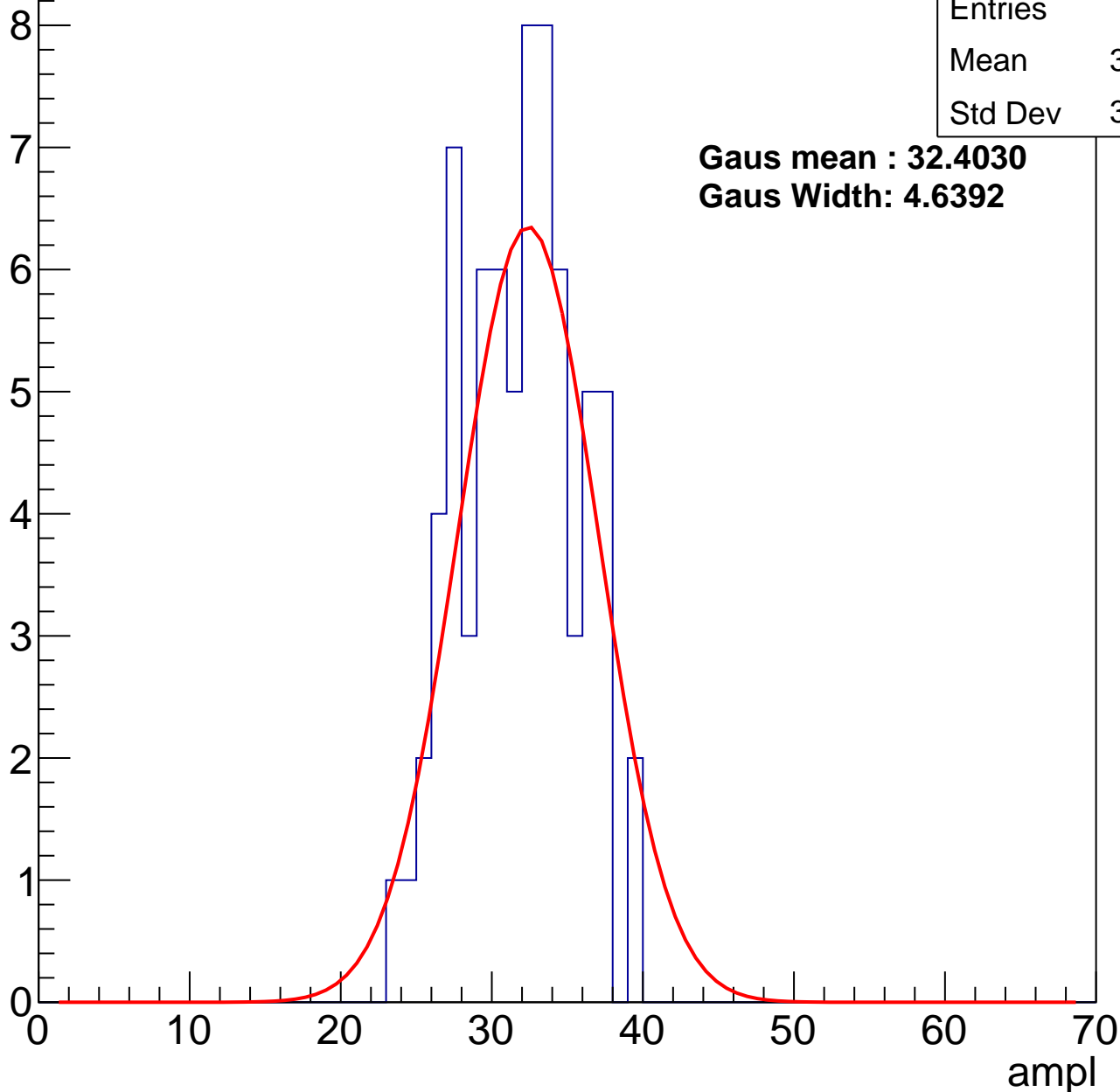
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	31.32
Std Dev	3.767

**Gaus mean : 32.4030**

**Gaus Width: 4.6392**



# B1L101S, U16-ch64, adc1

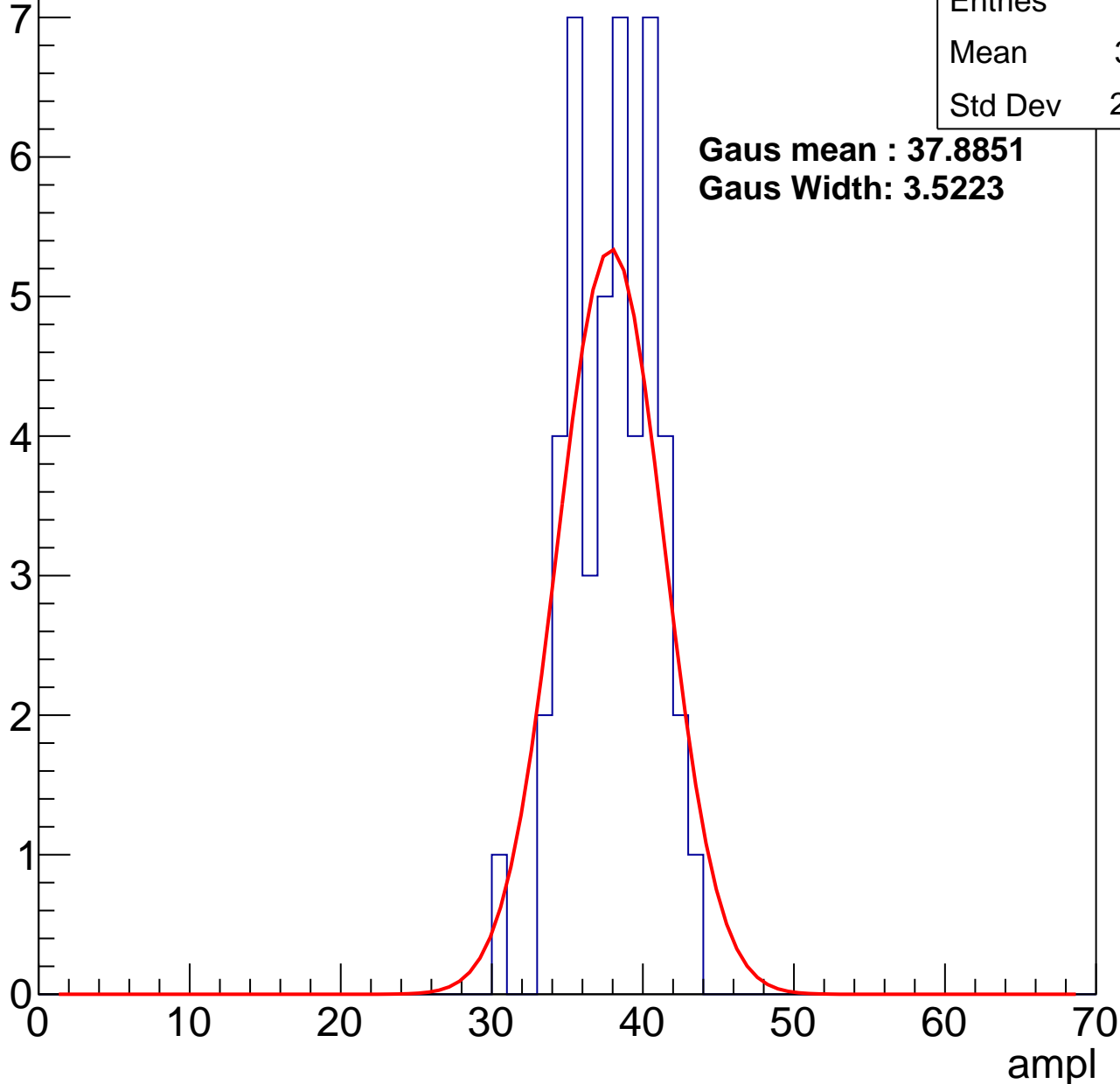
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	37.51
Std Dev	2.812

**Gaus mean : 37.8851**

**Gaus Width: 3.5223**



# B1L101S, U16-ch64, adc2

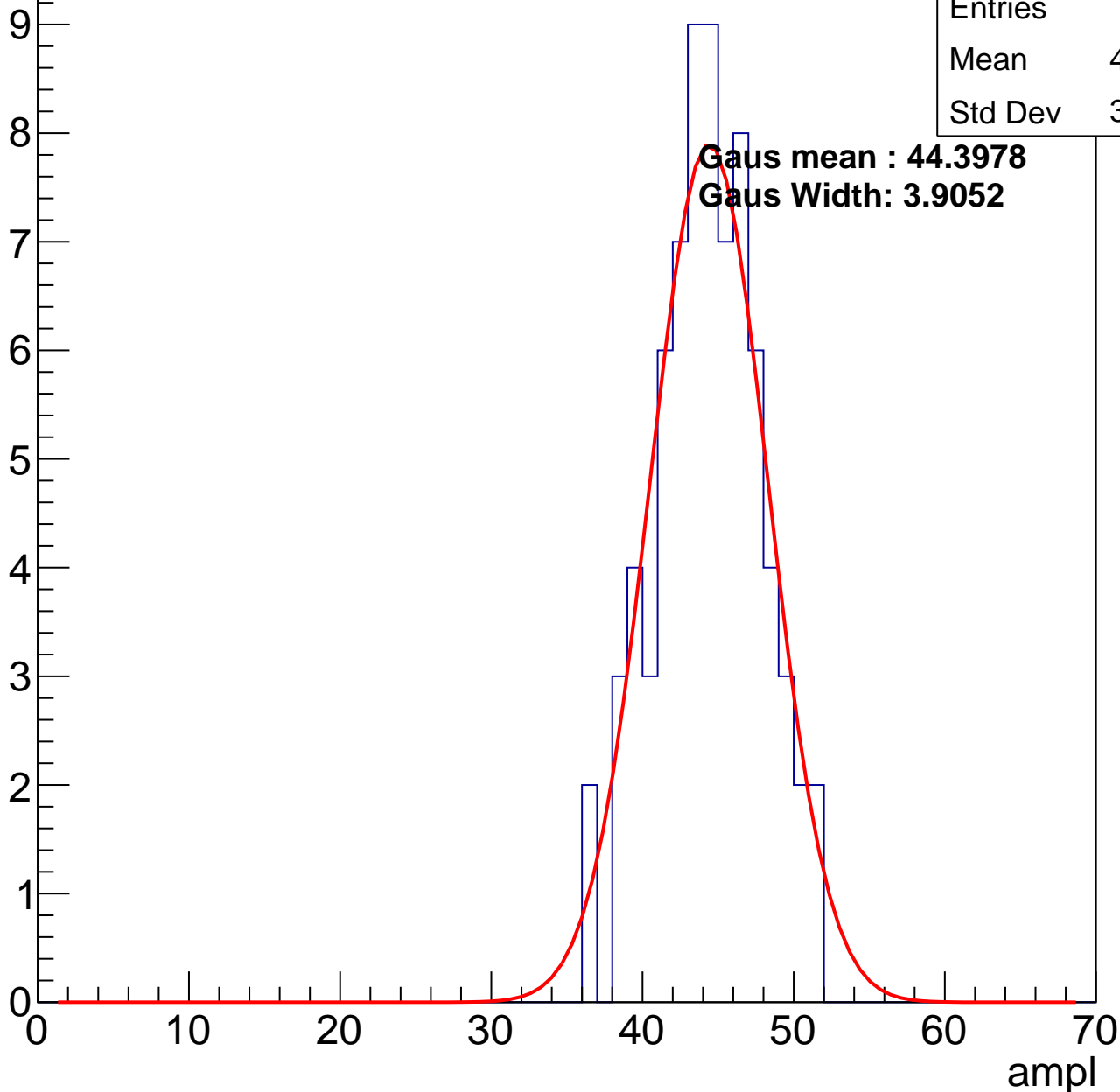
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	43.88
Std Dev	3.417

**Gaus mean : 44.3978**

**Gaus Width: 3.9052**

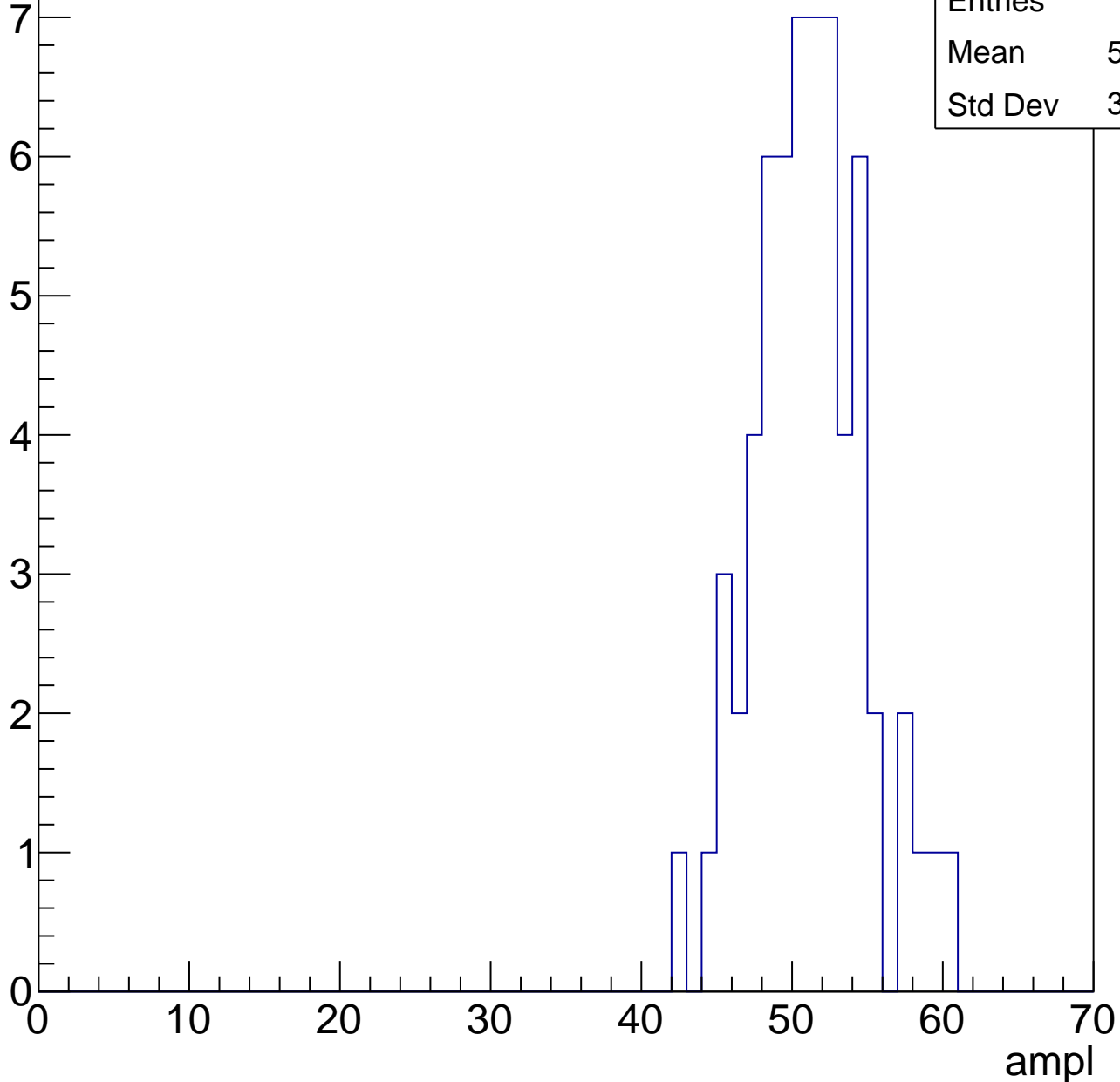


# B1L101S, U16-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	50.67
Std Dev	3.634

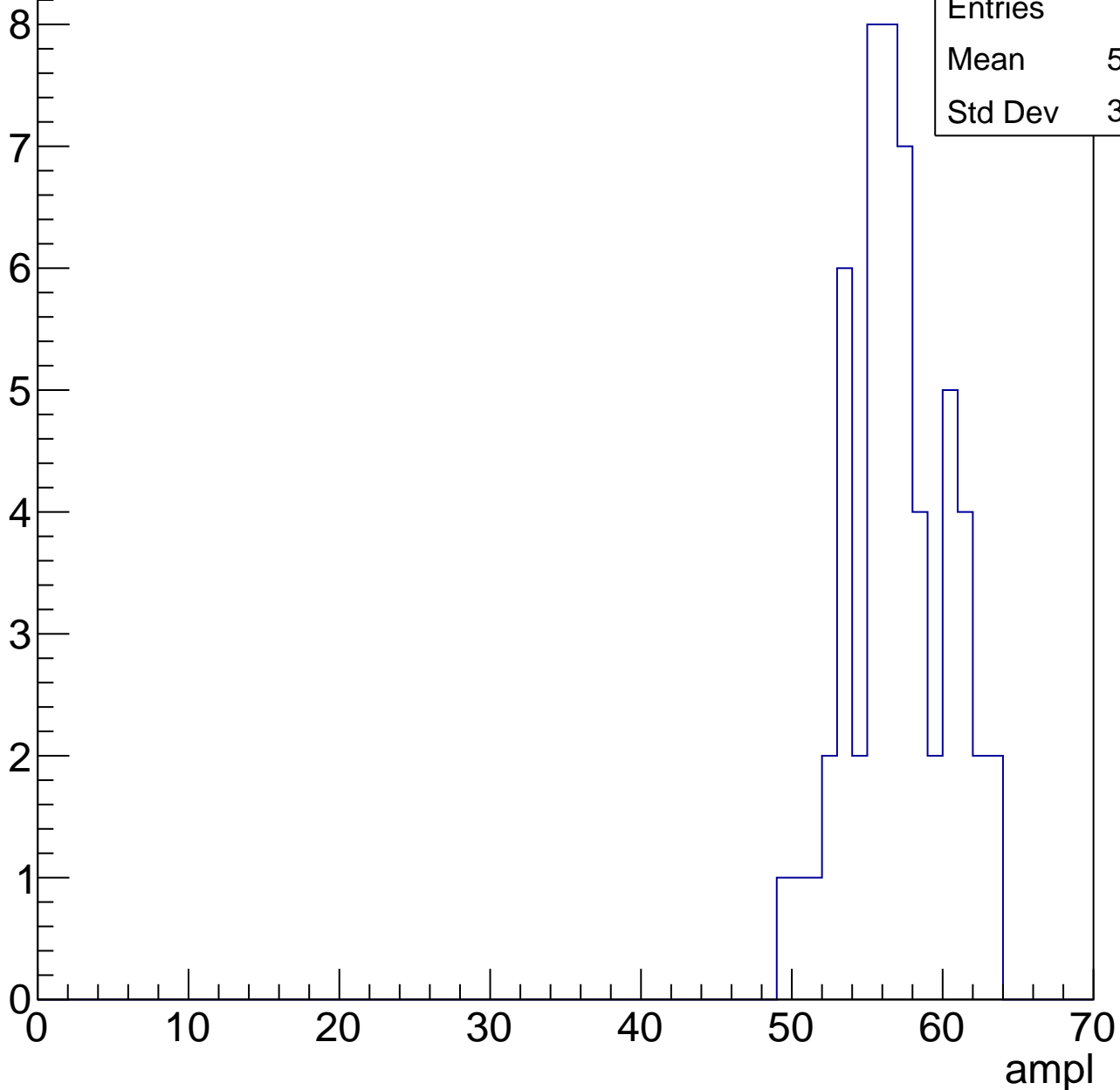


# B1L101S, U16-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

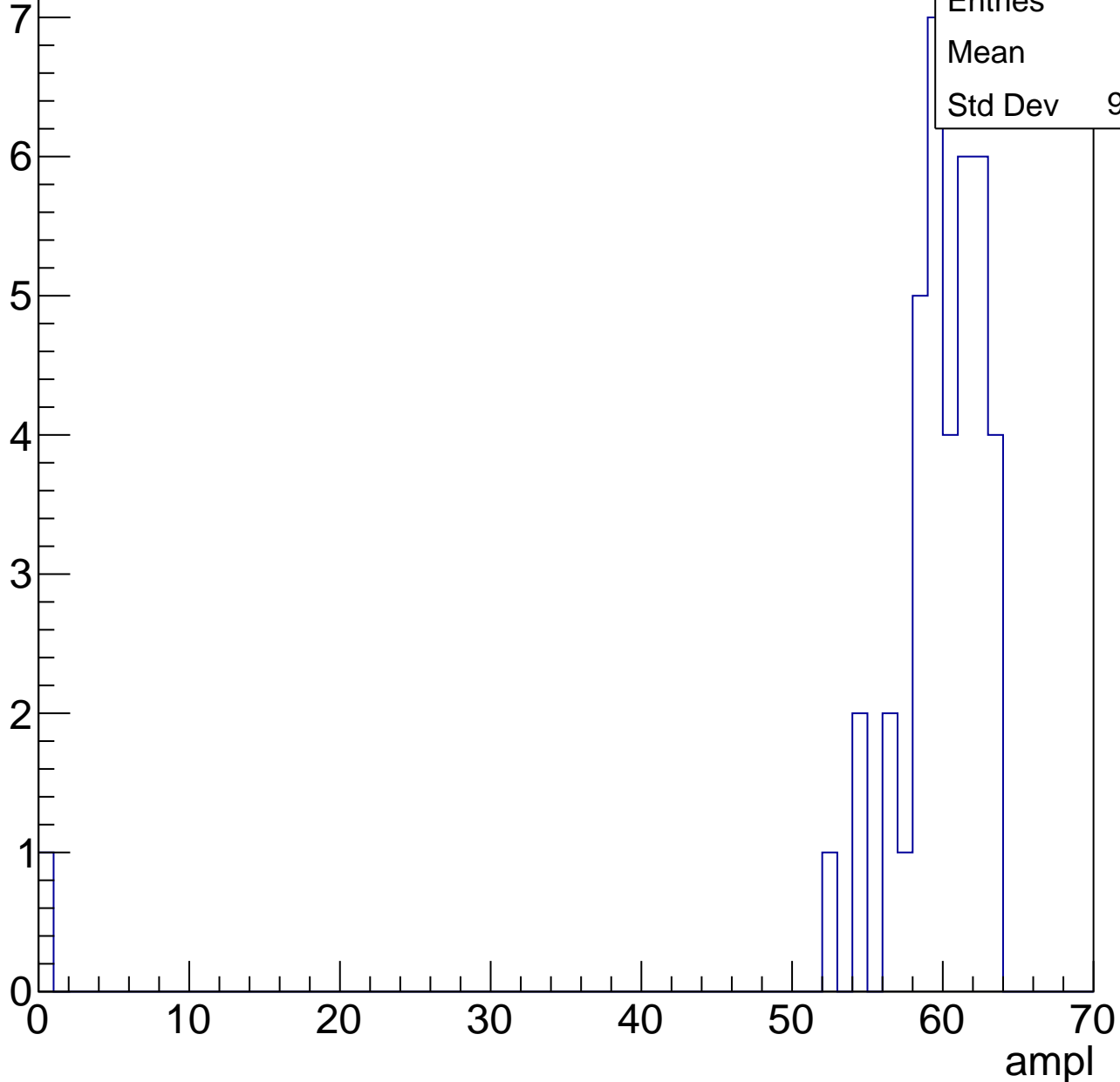
Entries	55
Mean	56.56
Std Dev	3.263



# B1L101S, U16-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

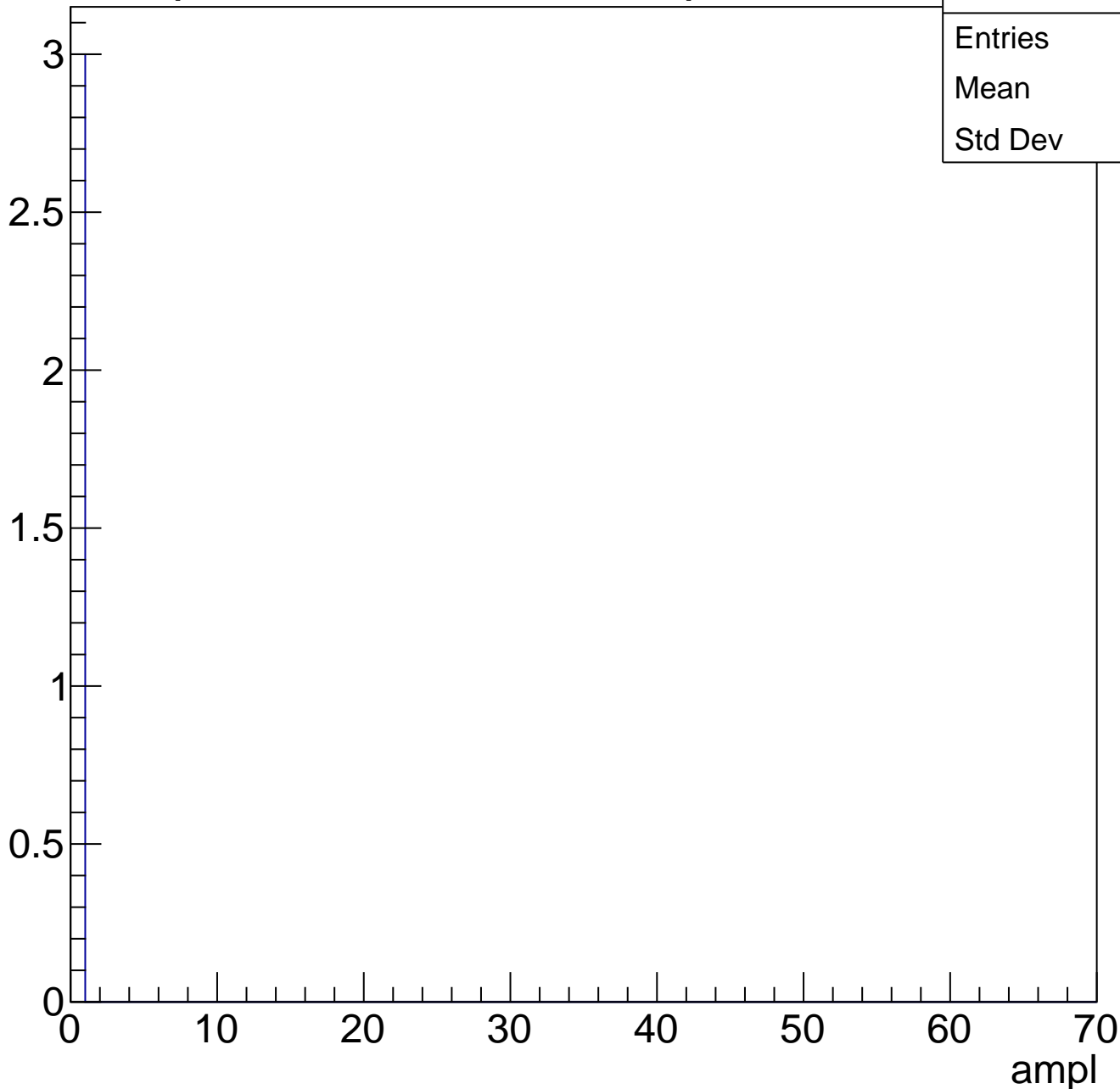




# B1L101S, U16-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U16-ch65, adc0

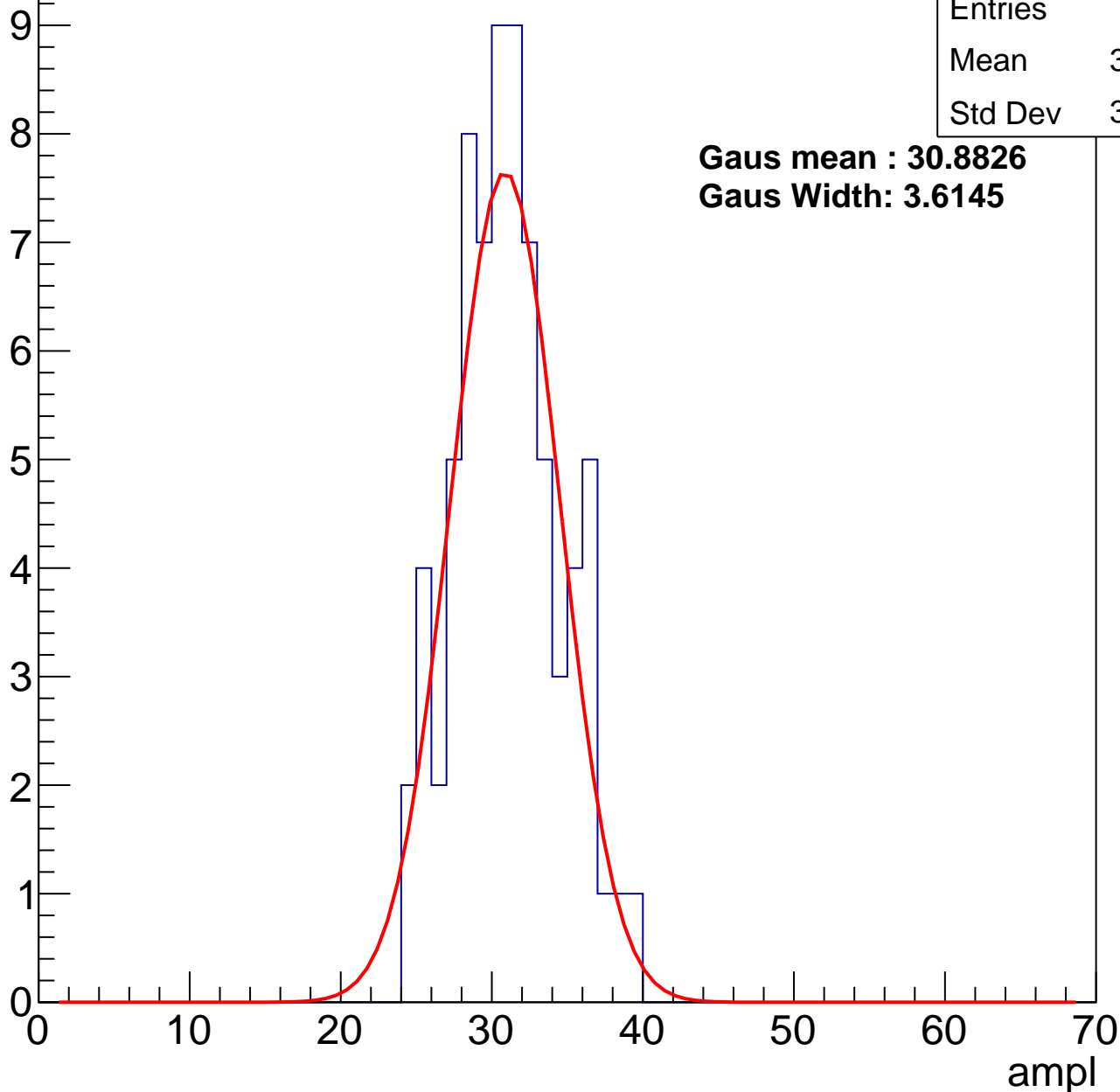
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	30.63
Std Dev	3.438

**Gaus mean : 30.8826**

**Gaus Width: 3.6145**



# B1L101S, U16-ch65, adc1

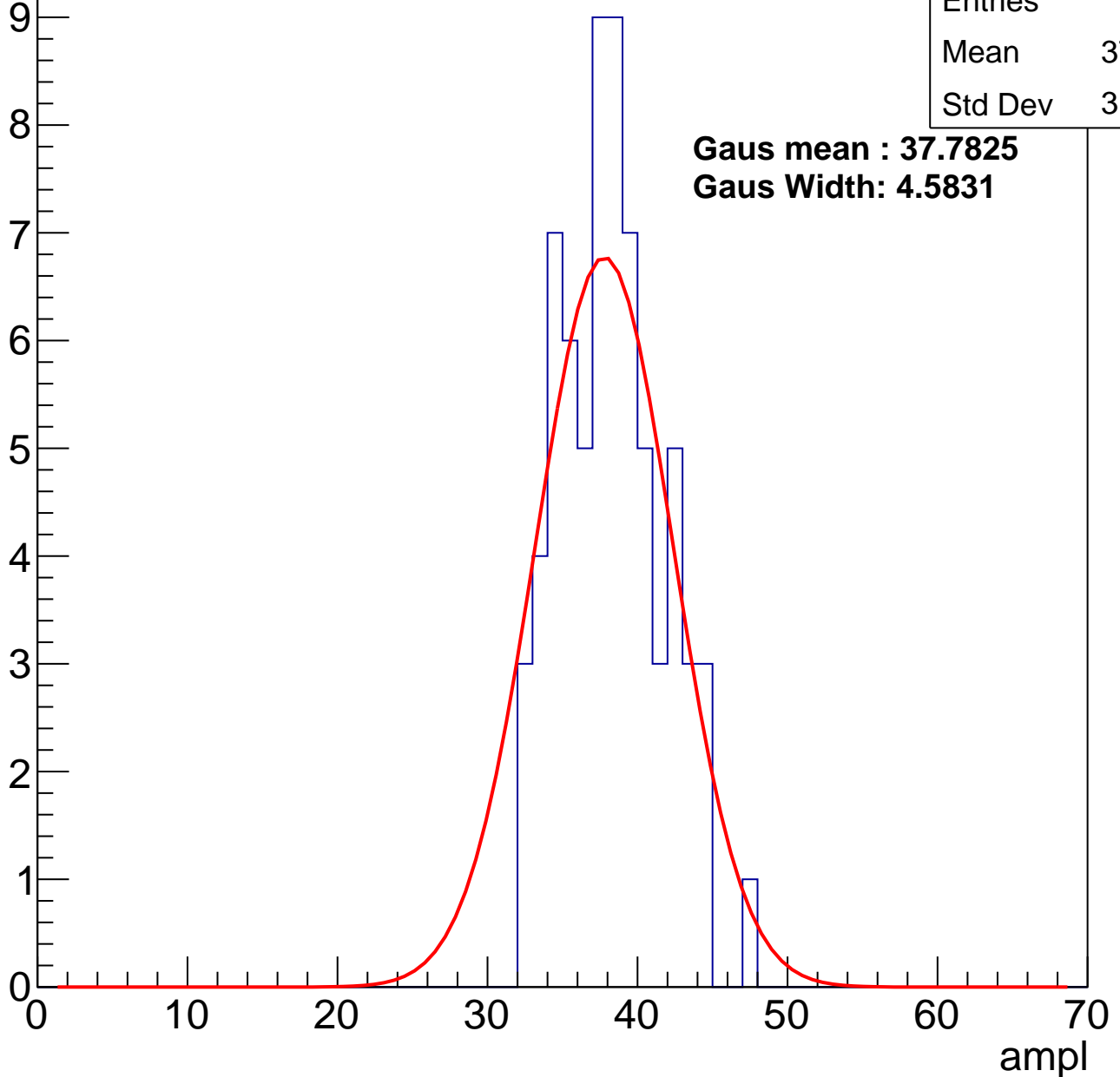
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	37.79
Std Dev	3.376

**Gaus mean : 37.7825**

**Gaus Width: 4.5831**



# B1L101S, U16-ch65, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	44.59
Std Dev	3.172

**Gaus mean : 44.5688**

**Gaus Width: 3.7097**

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

0

1

2

3

4

5

6

7

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11

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14

15

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21

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307

308

309

310

311

312

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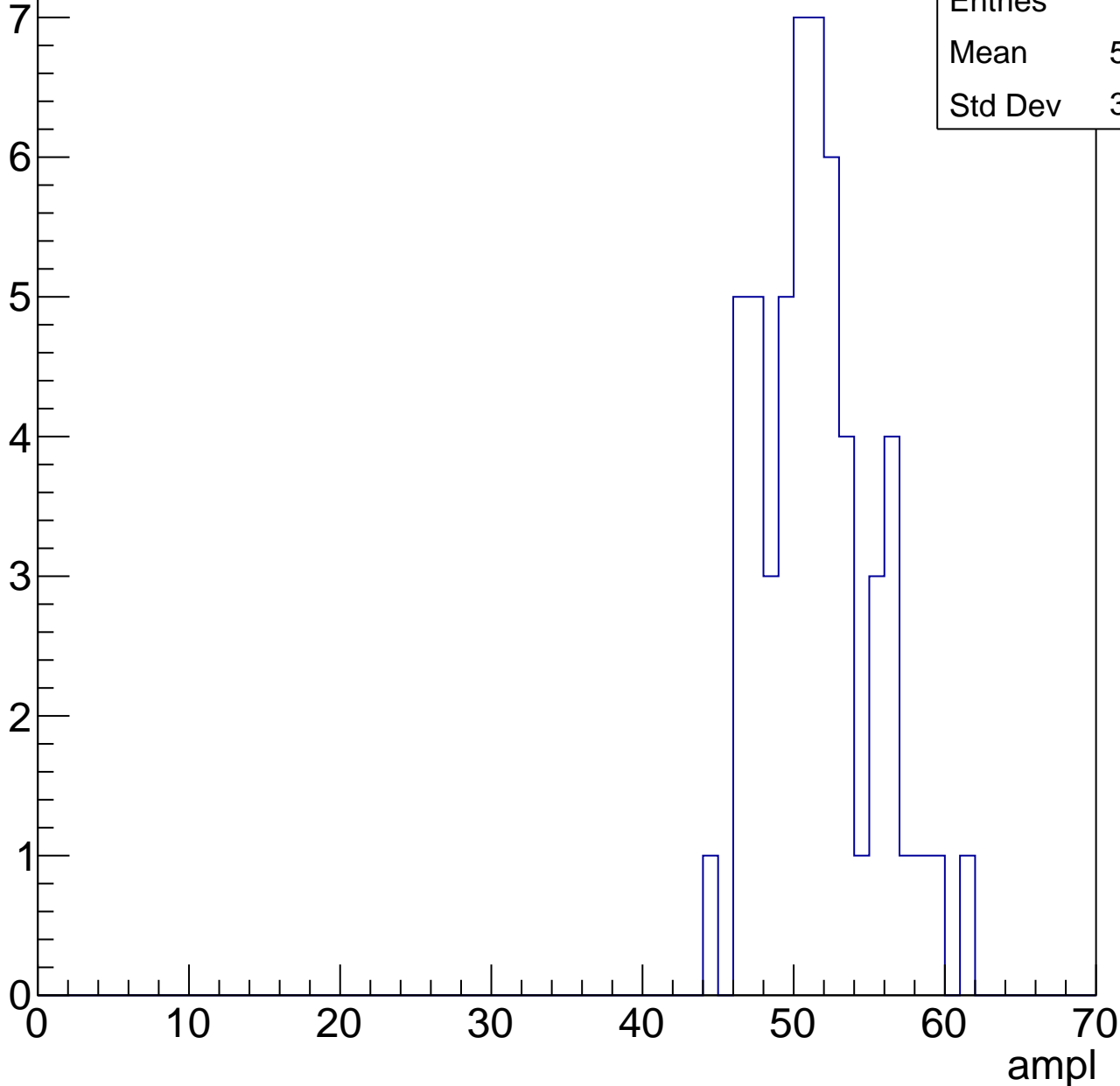
325

# B1L101S, U16-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

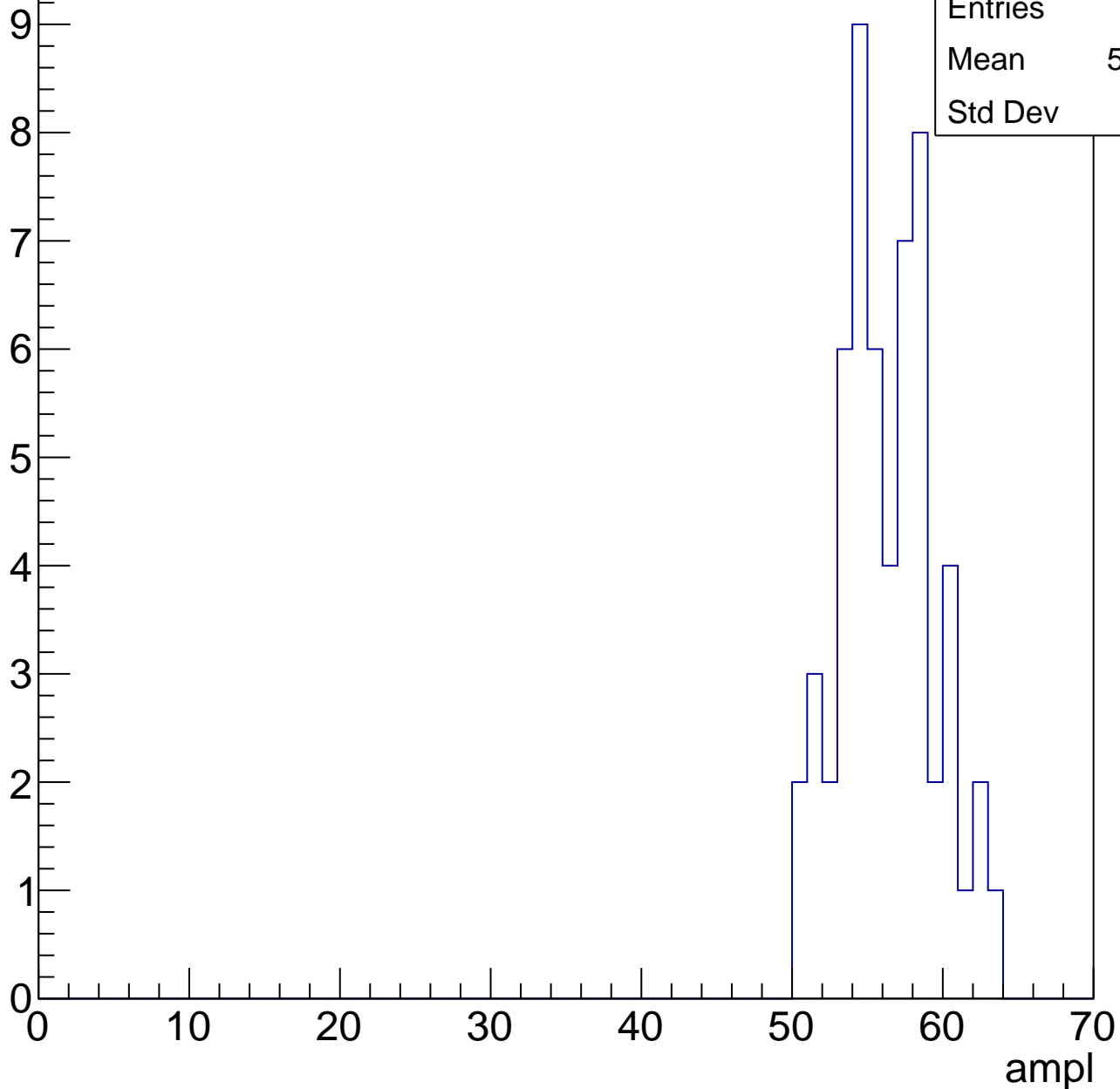
Entries	55
Mean	51.04
Std Dev	3.658



# B1L101S, U16-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch65, adc5

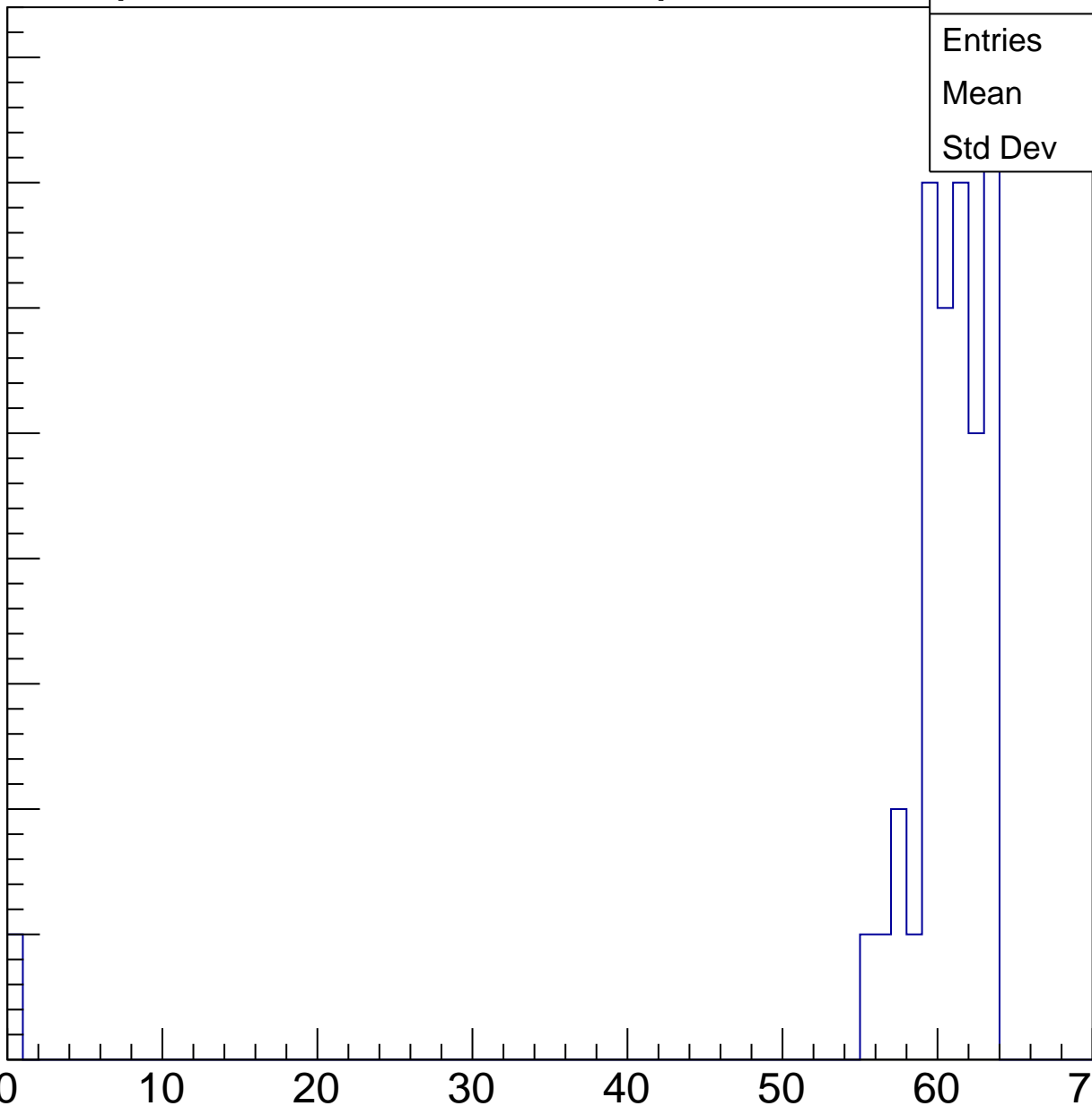
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	39
Mean	58.9
Std Dev	9.769

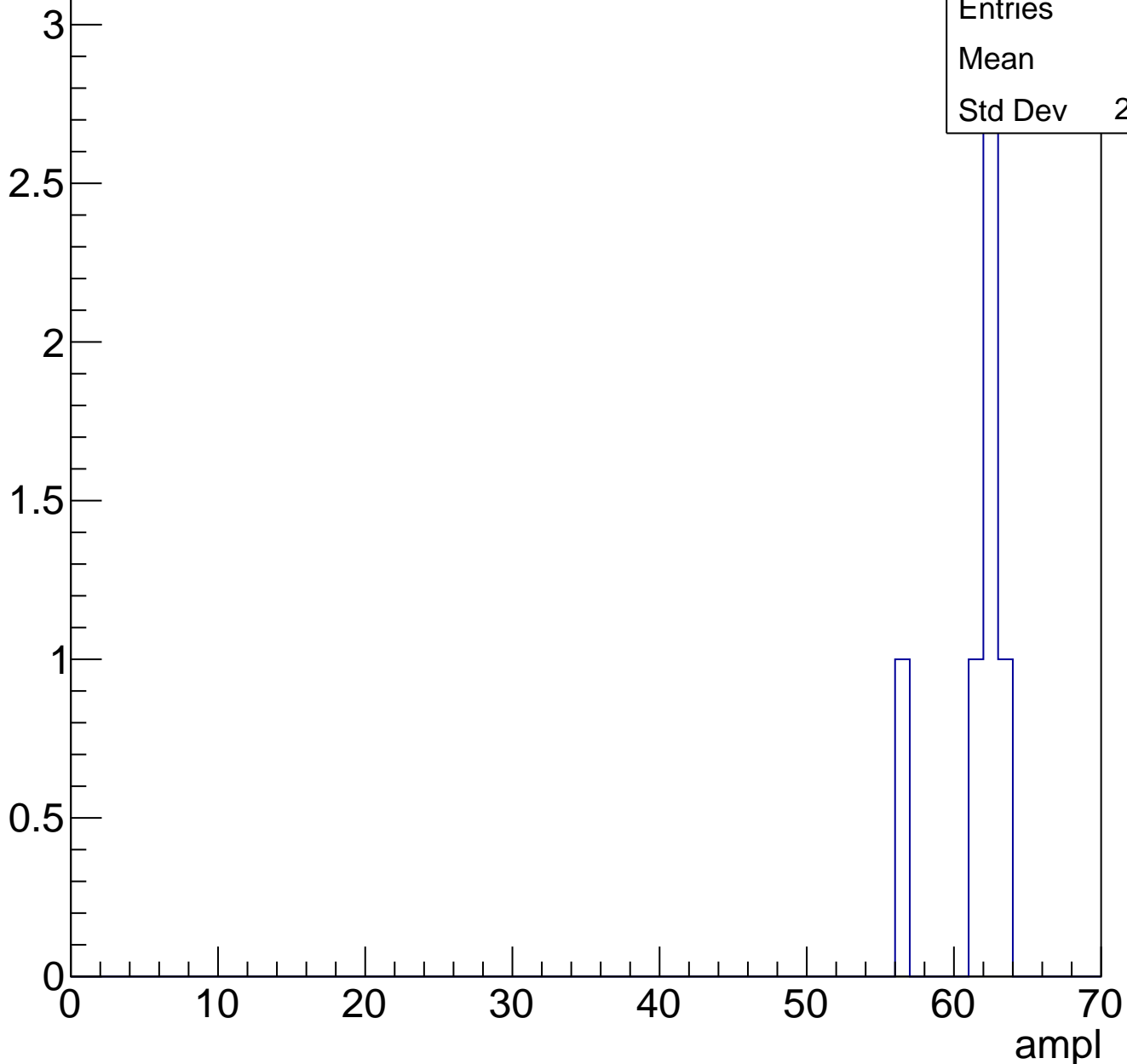
ampl



# B1L101S, U16-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U16-ch66, adc0

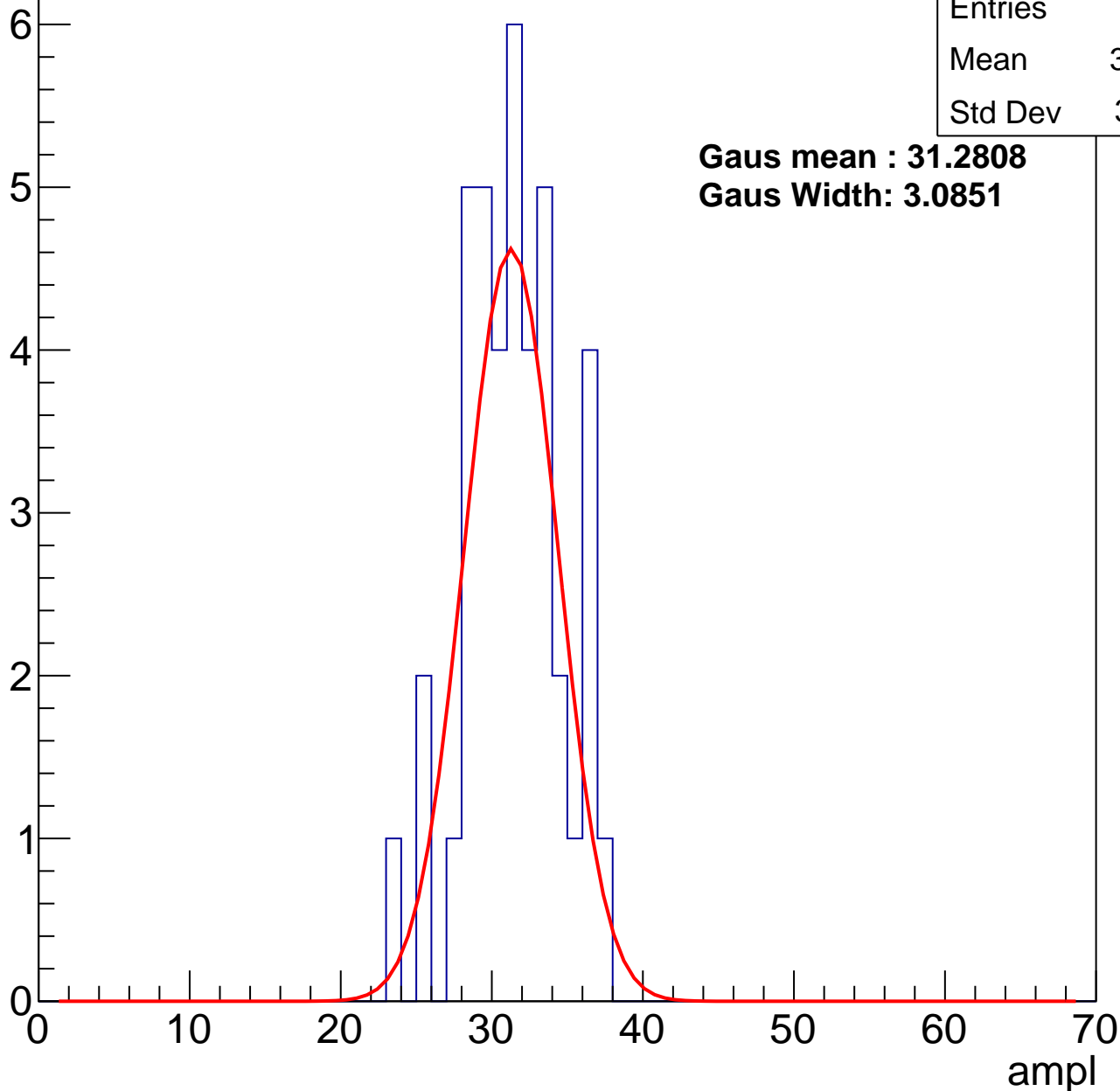
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	41
Mean	30.93
Std Dev	3.181

**Gaus mean : 31.2808**

**Gaus Width: 3.0851**



# B1L101S, U16-ch66, adc1

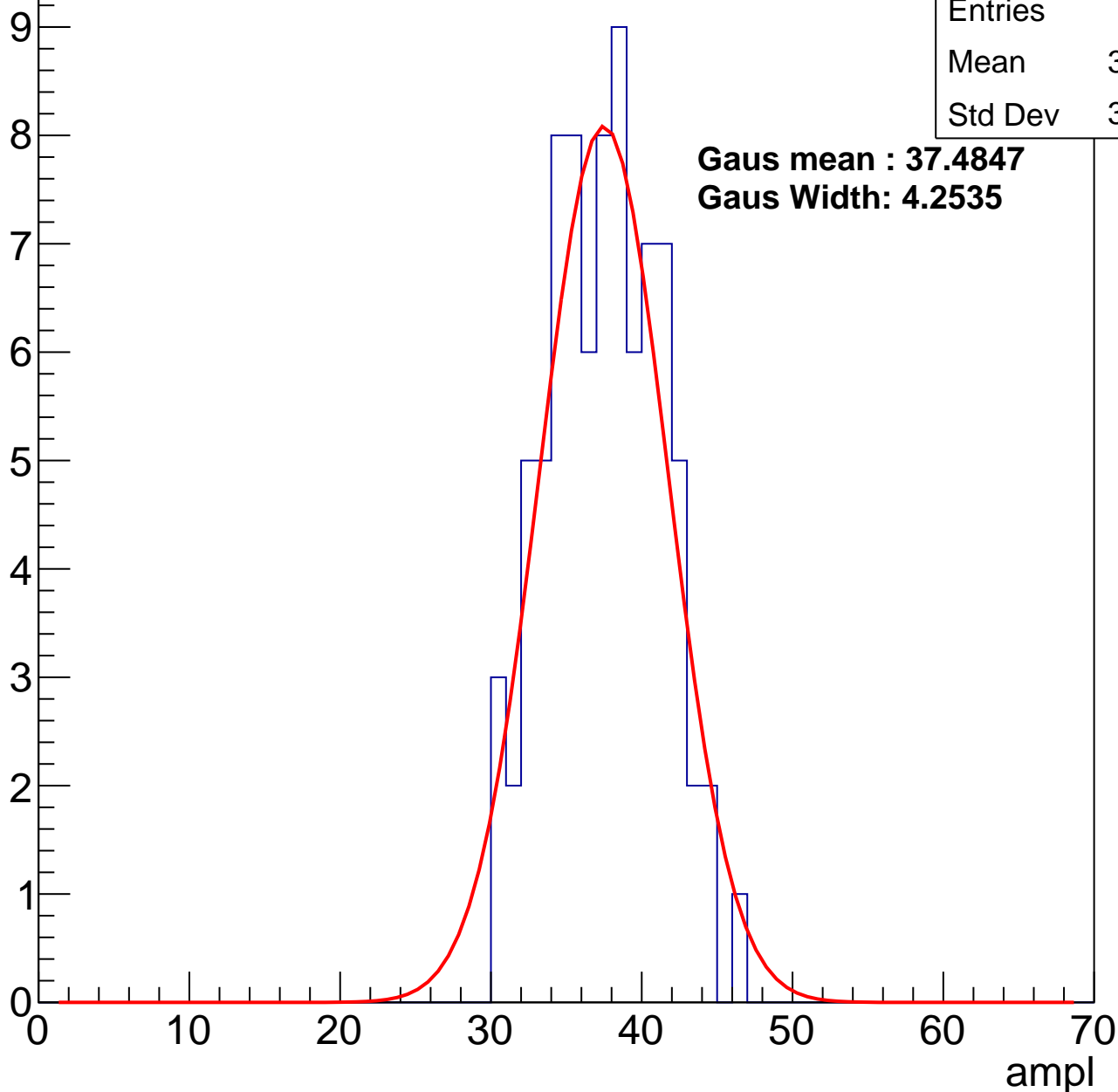
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	84
Mean	37.07
Std Dev	3.648

**Gaus mean : 37.4847**

**Gaus Width: 4.2535**



# B1L101S, U16-ch66, adc2

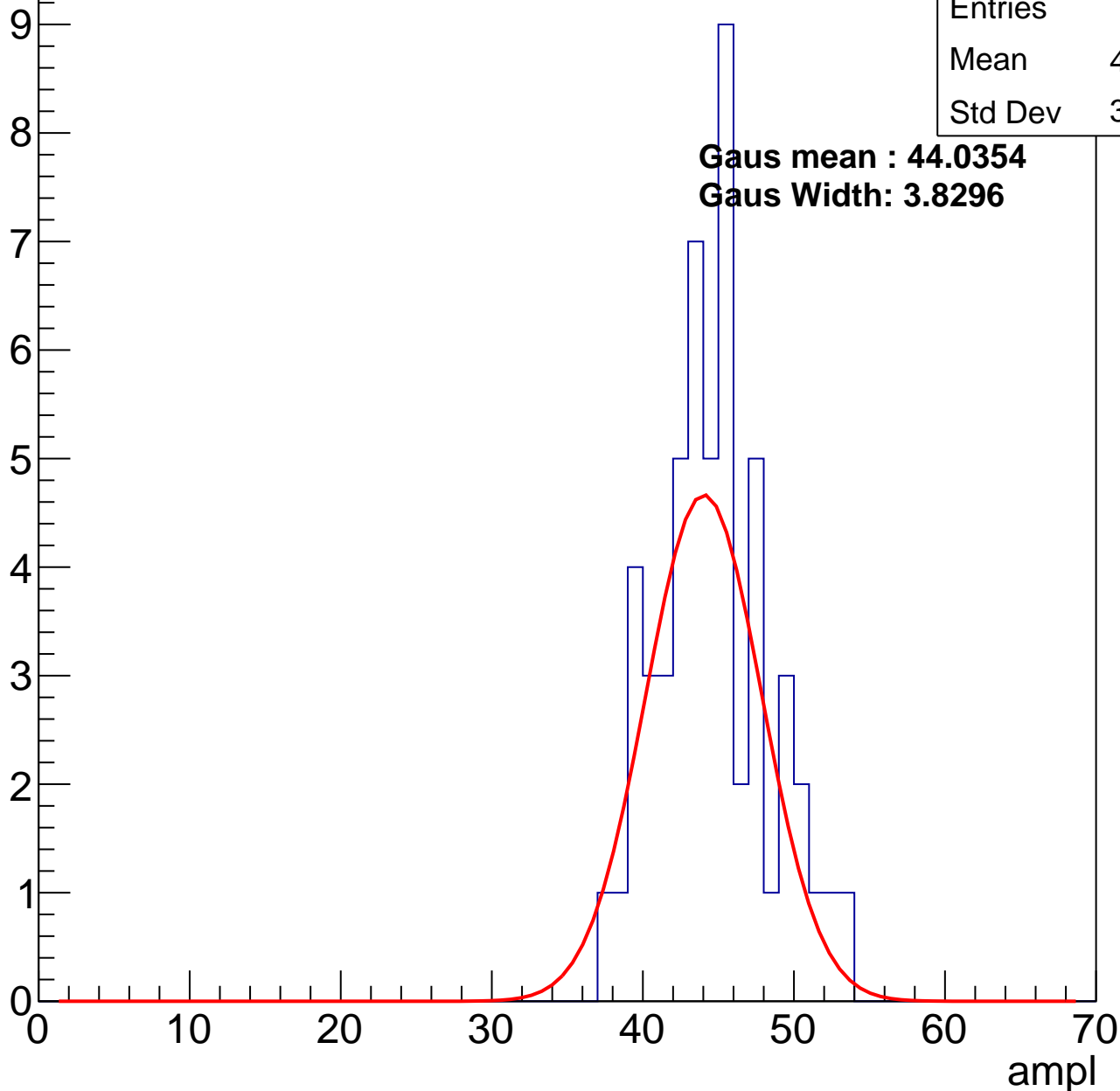
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	44.22
Std Dev	3.609

**Gaus mean : 44.0354**

**Gaus Width: 3.8296**

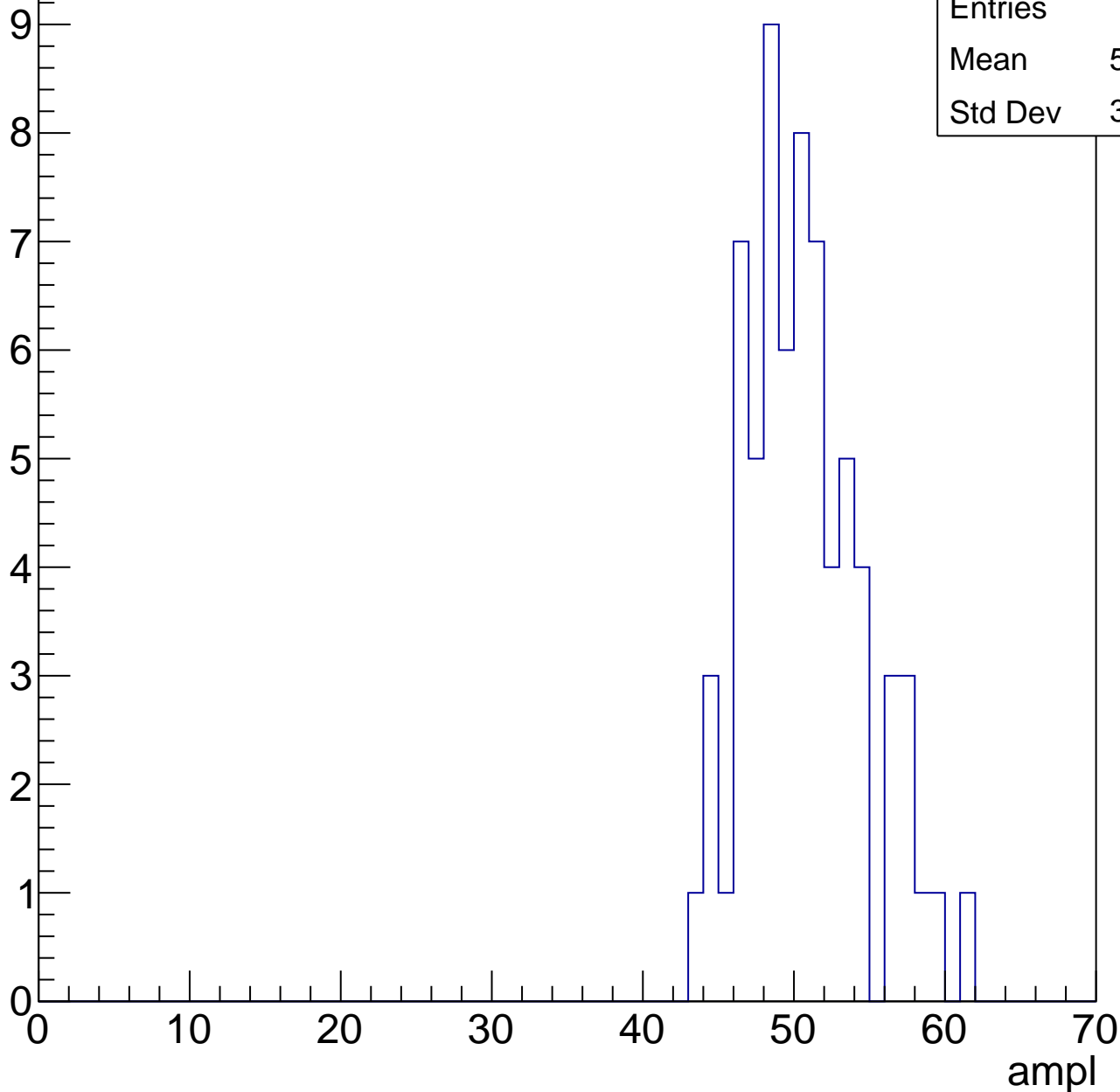


# B1L101S, U16-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	50.23
Std Dev	3.864



# B1L101S, U16-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	67
Mean	56.6
Std Dev	3.163

Entry

10

8

6

4

2

0

0

10

20

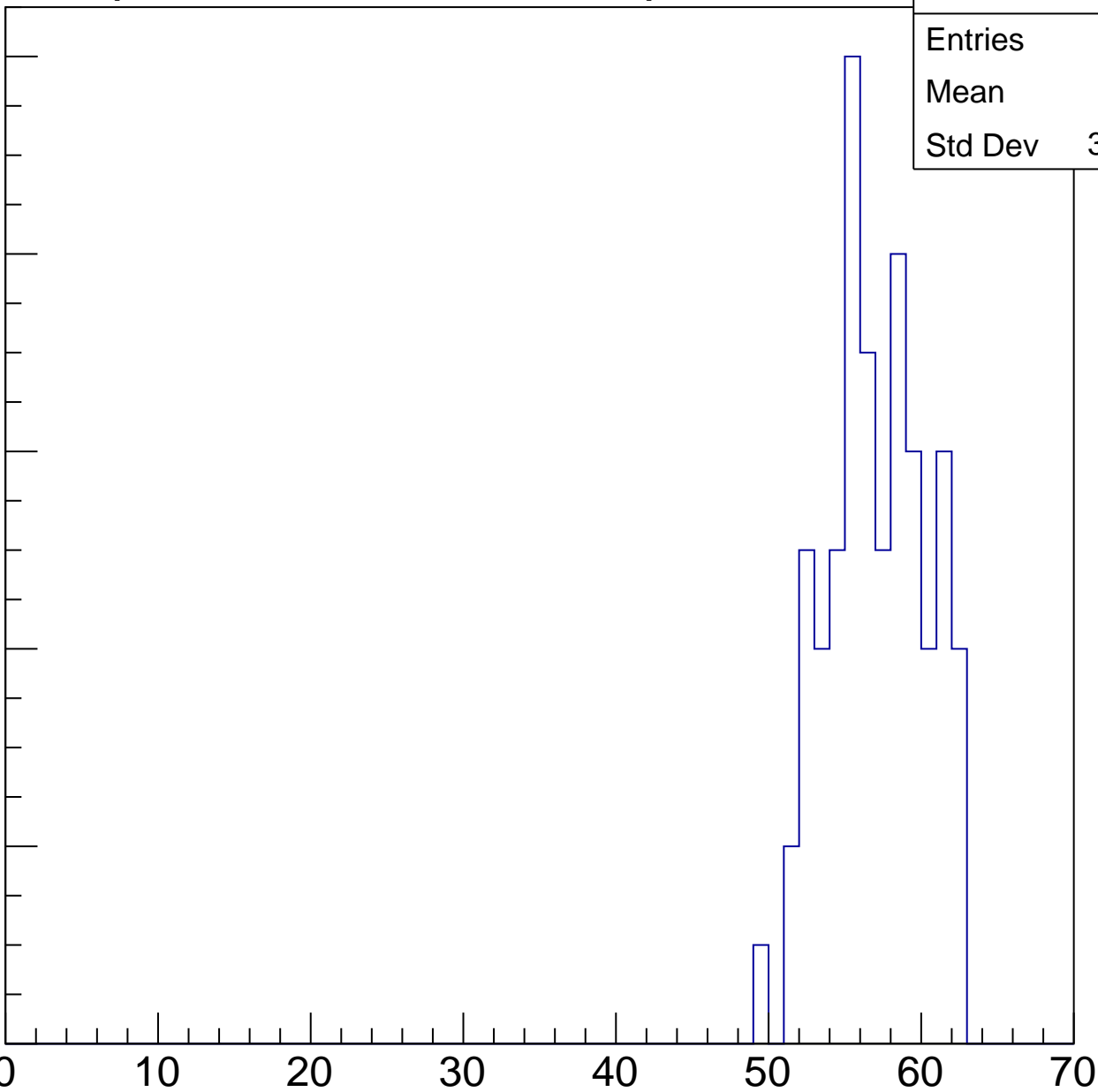
30

40

50

60

ampl

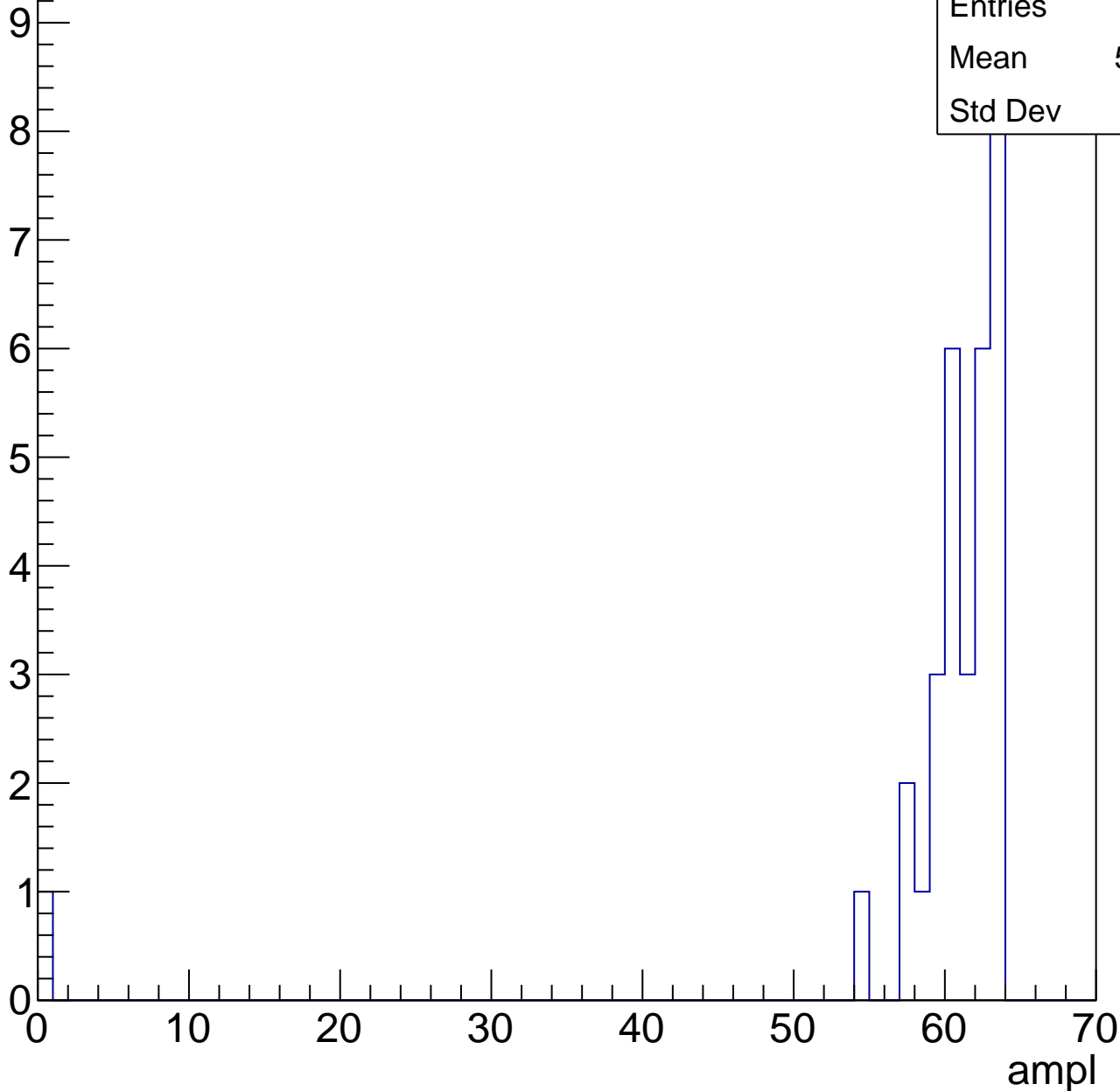


# B1L101S, U16-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	32
Mean	58.91
Std Dev	10.8



# B1L101S, U16-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch67, adc0

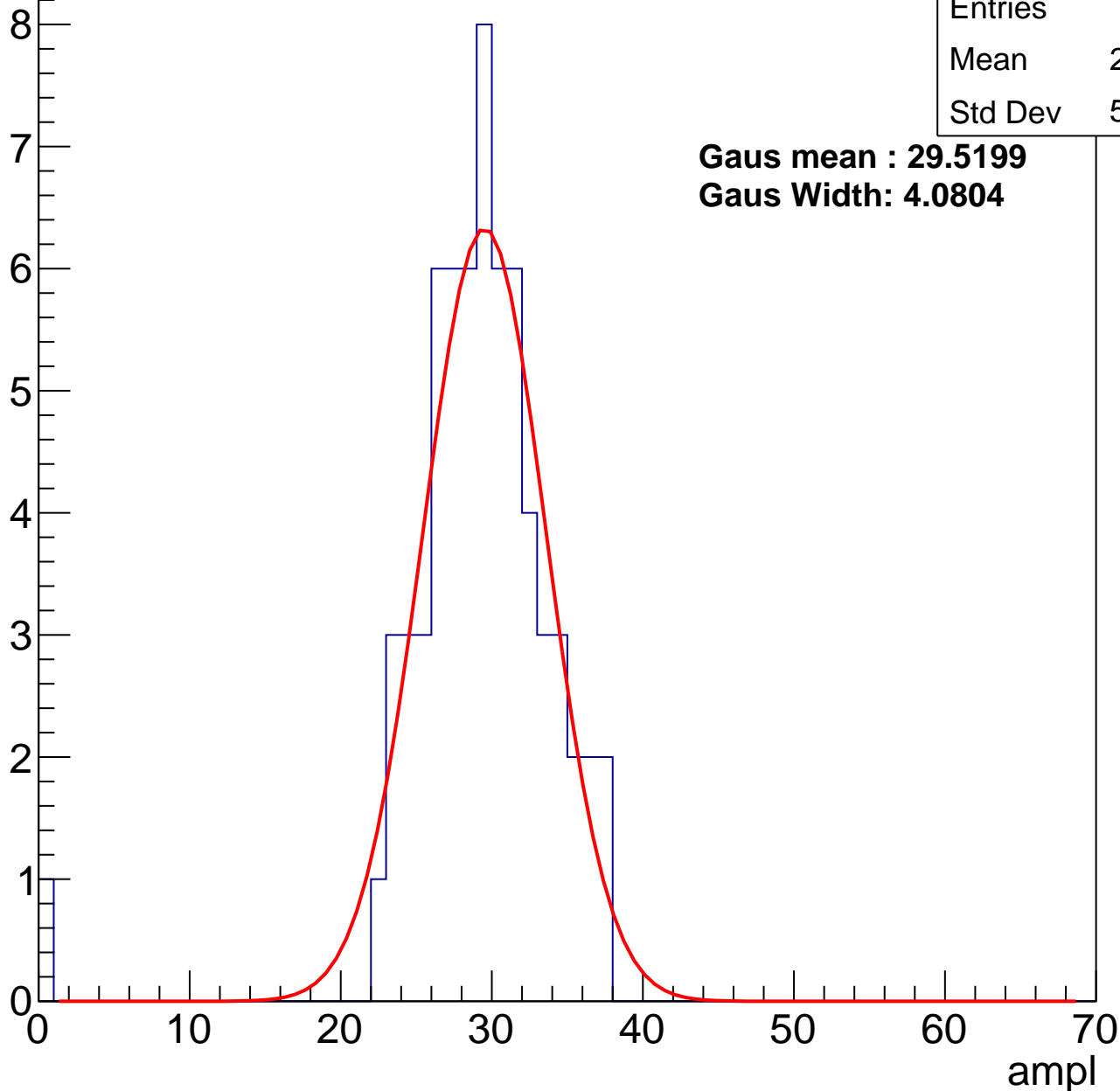
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	28.72
Std Dev	5.095

**Gaus mean : 29.5199**

**Gaus Width: 4.0804**



# B1L101S, U16-ch67, adc1

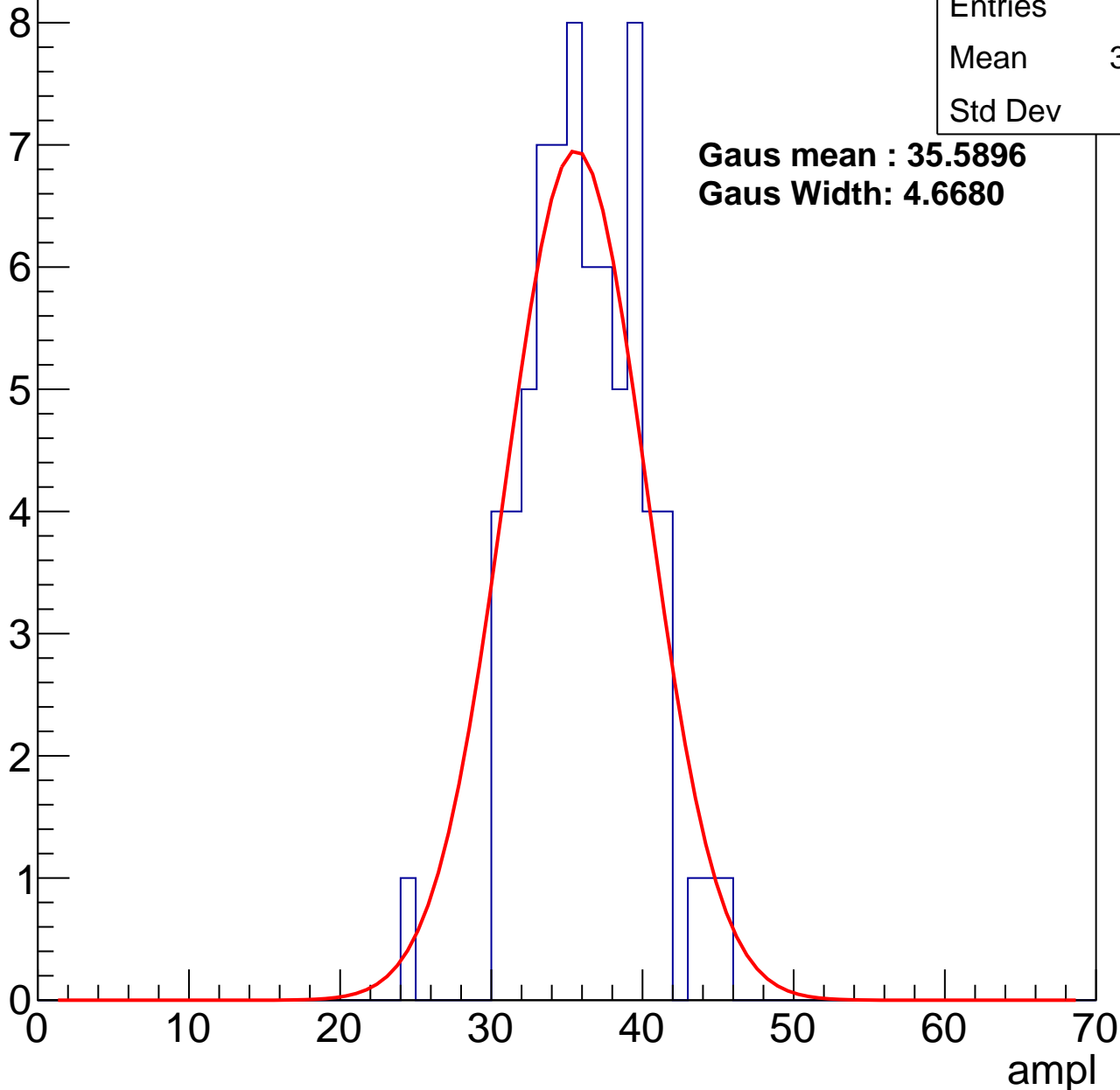
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	35.74
Std Dev	3.76

**Gaus mean : 35.5896**

**Gaus Width: 4.6680**



# B1L101S, U16-ch67, adc2

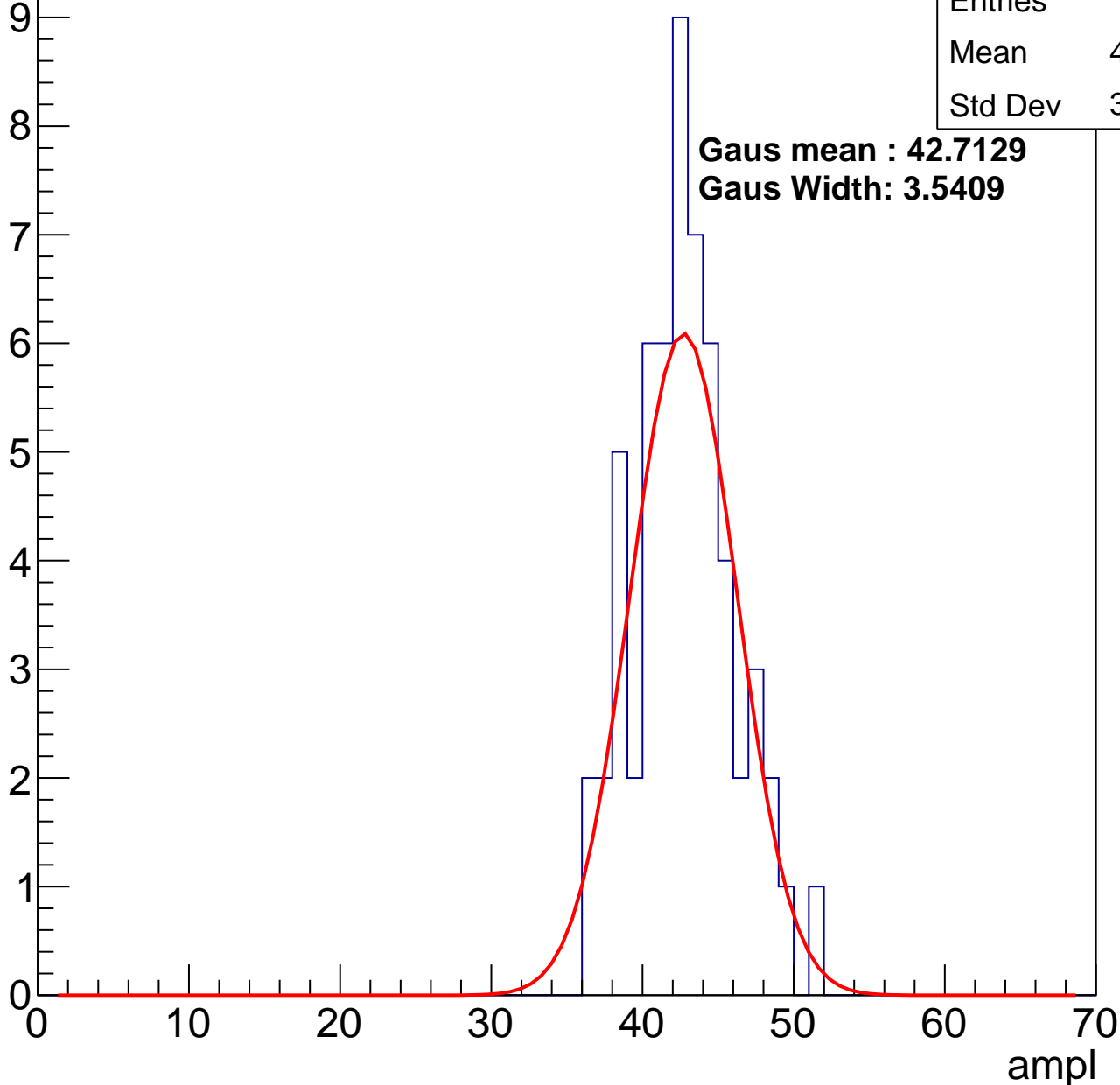
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	42.28
Std Dev	3.274

**Gaus mean : 42.7129**

**Gaus Width: 3.5409**

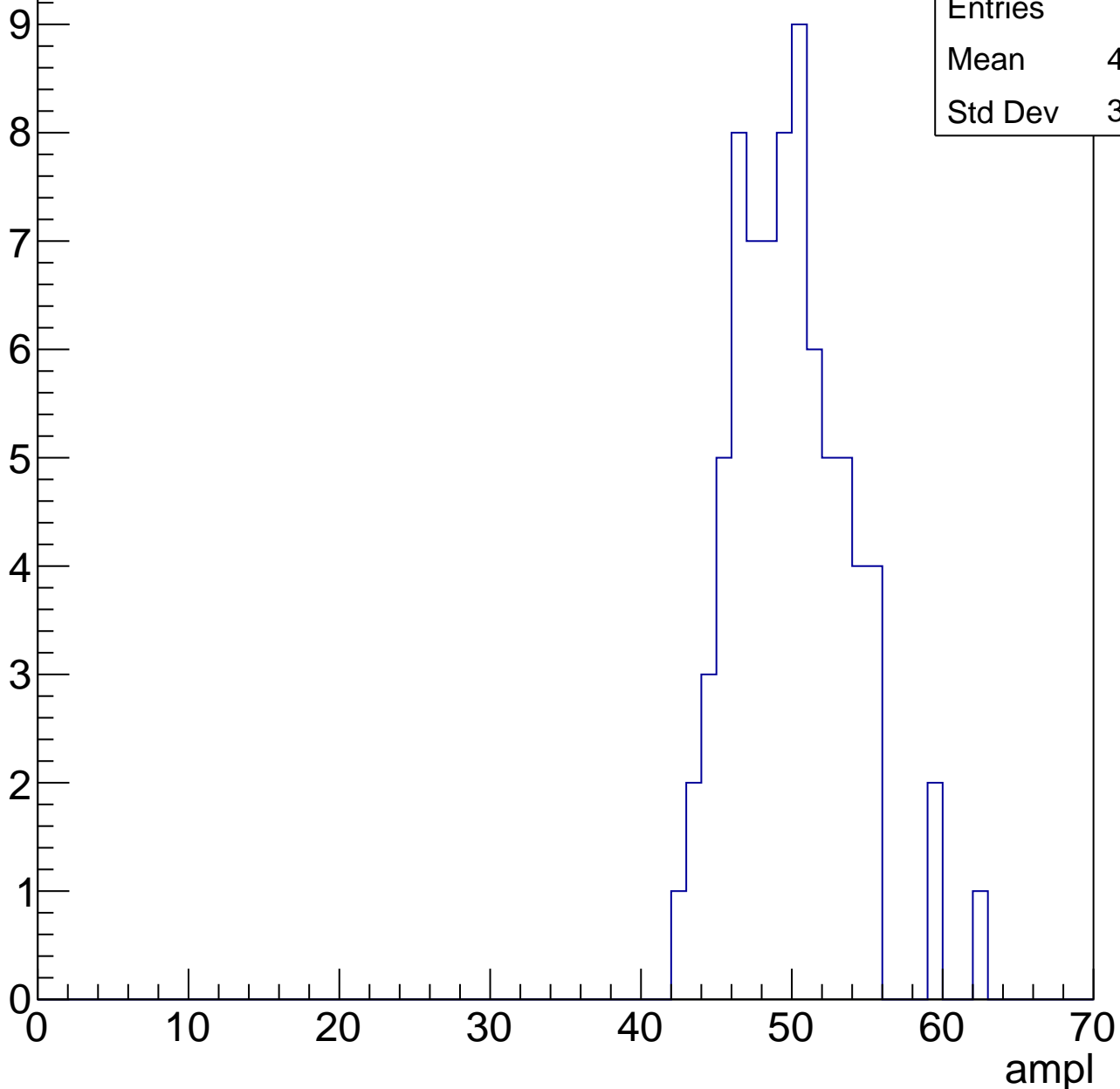


# B1L101S, U16-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	49.44
Std Dev	3.846

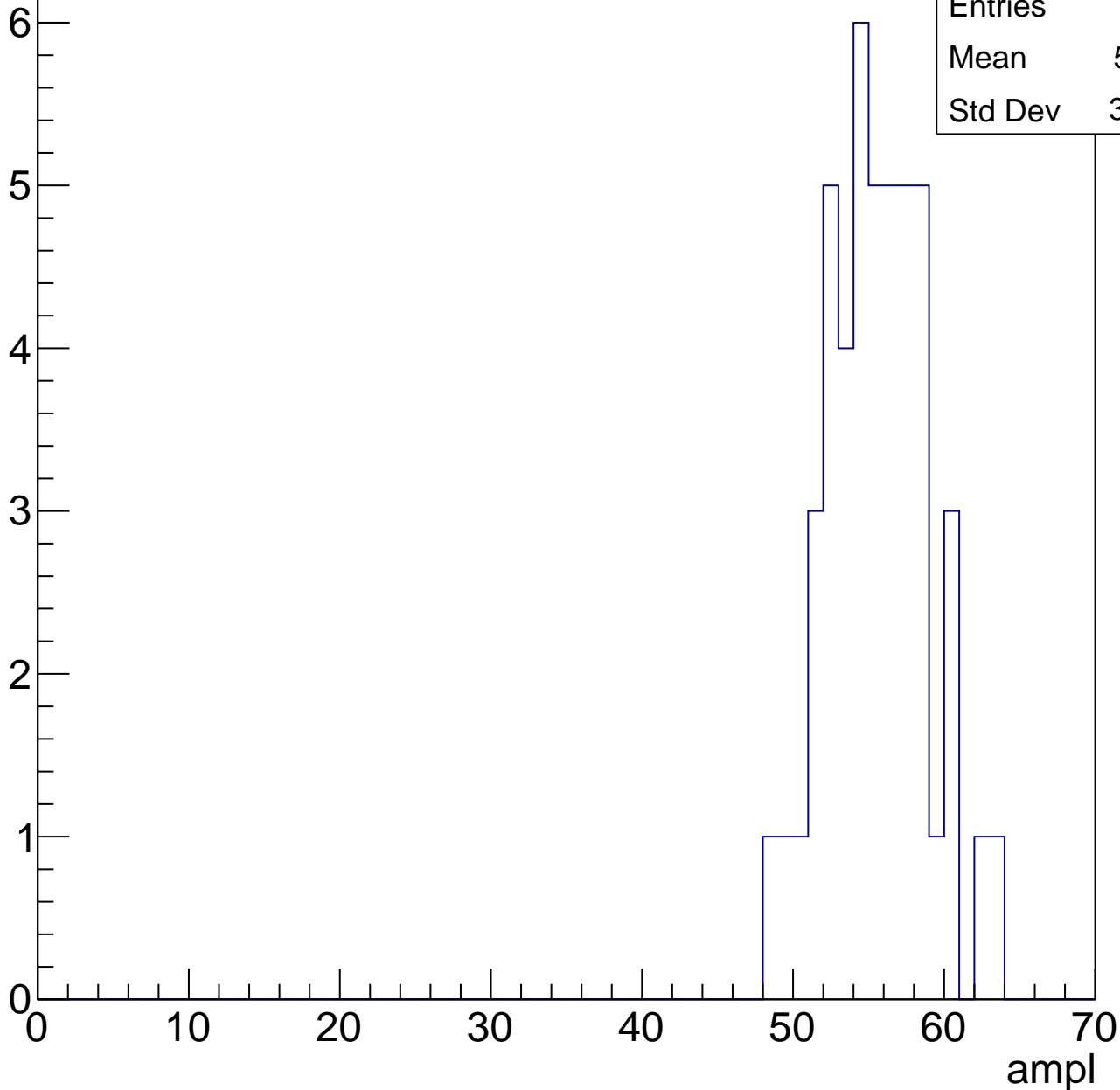


# B1L101S, U16-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

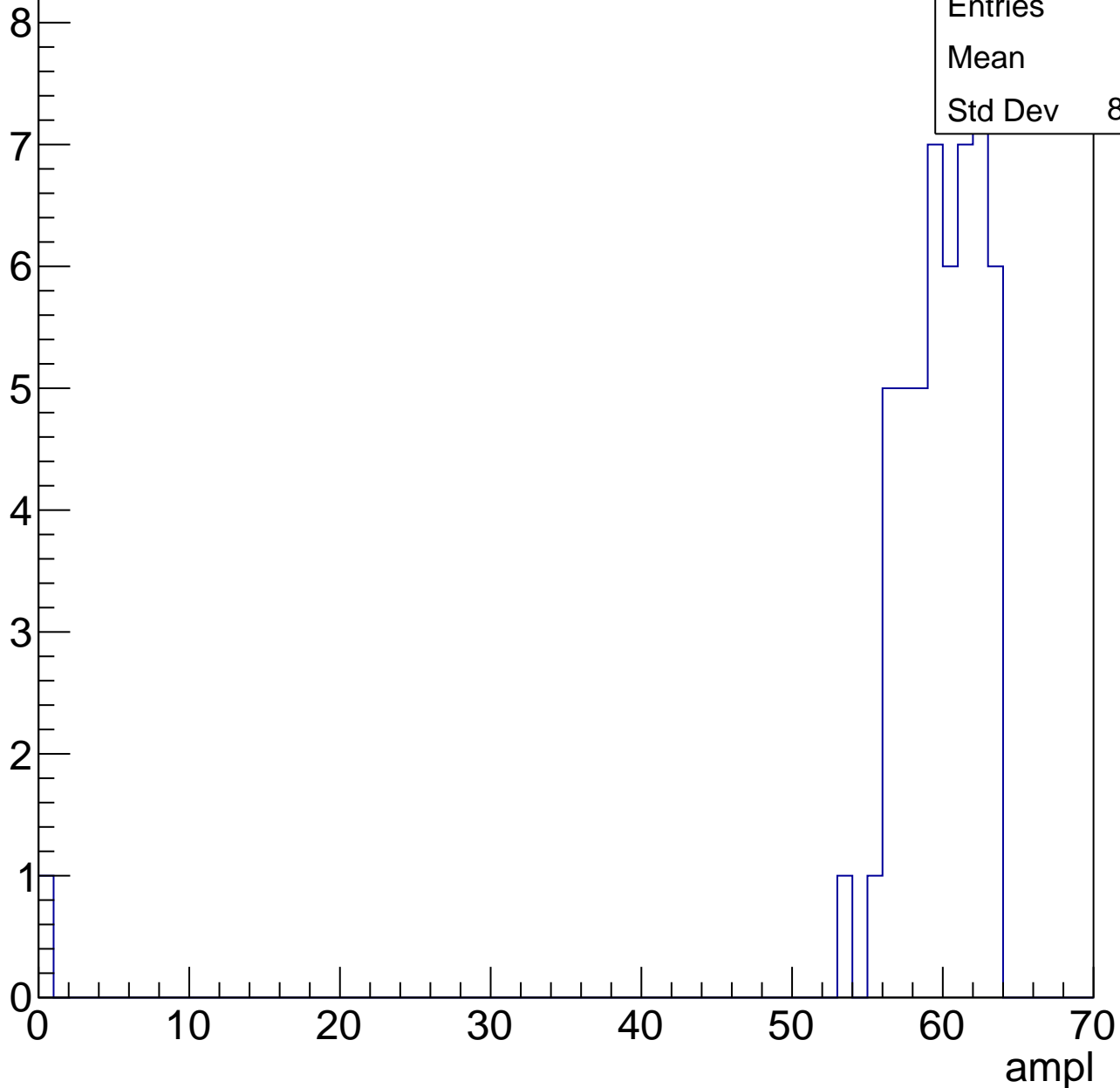
Entries	47
Mean	55.11
Std Dev	3.257



# B1L101S, U16-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

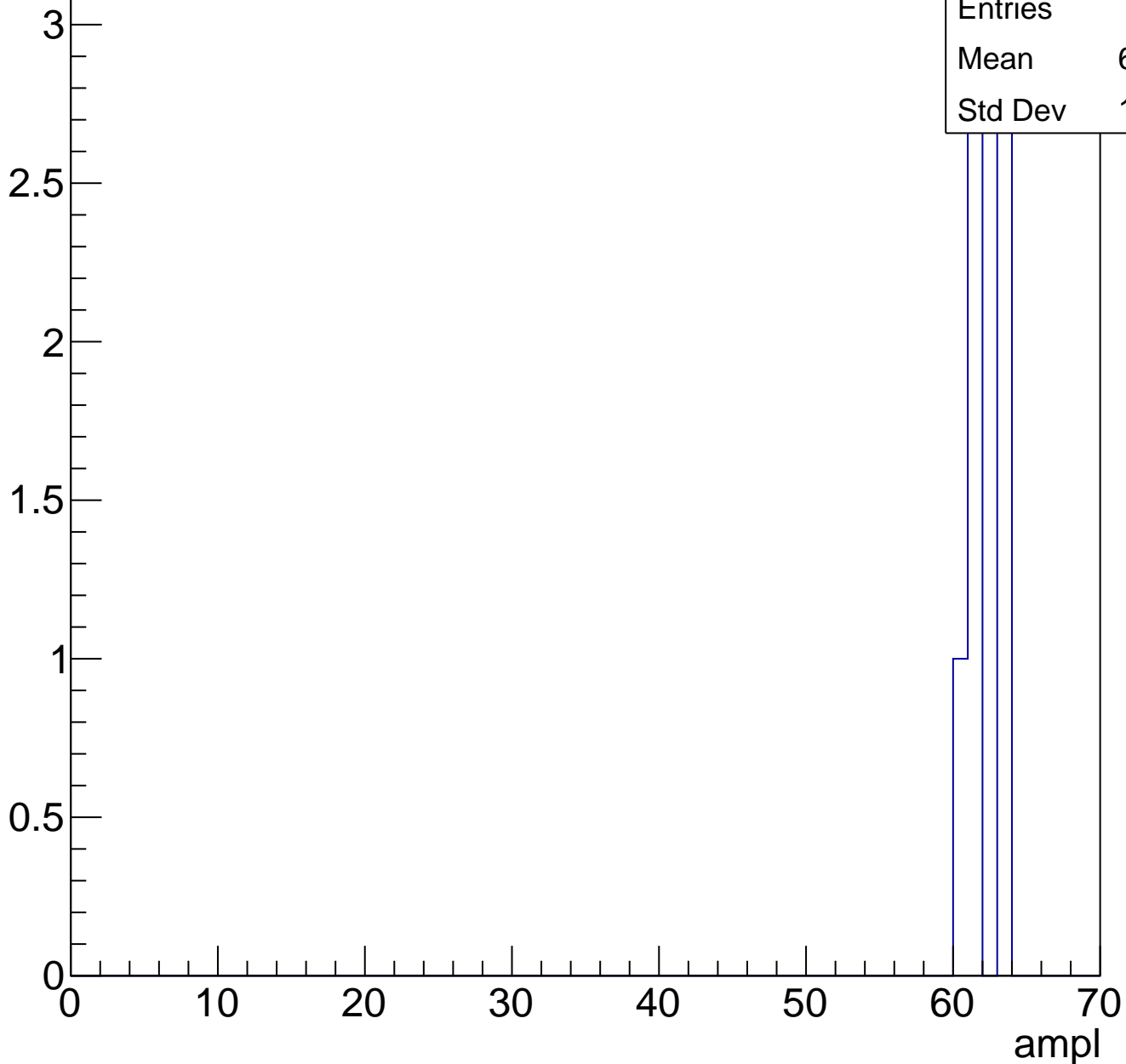
Entry



# B1L101S, U16-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U16-ch68, adc0

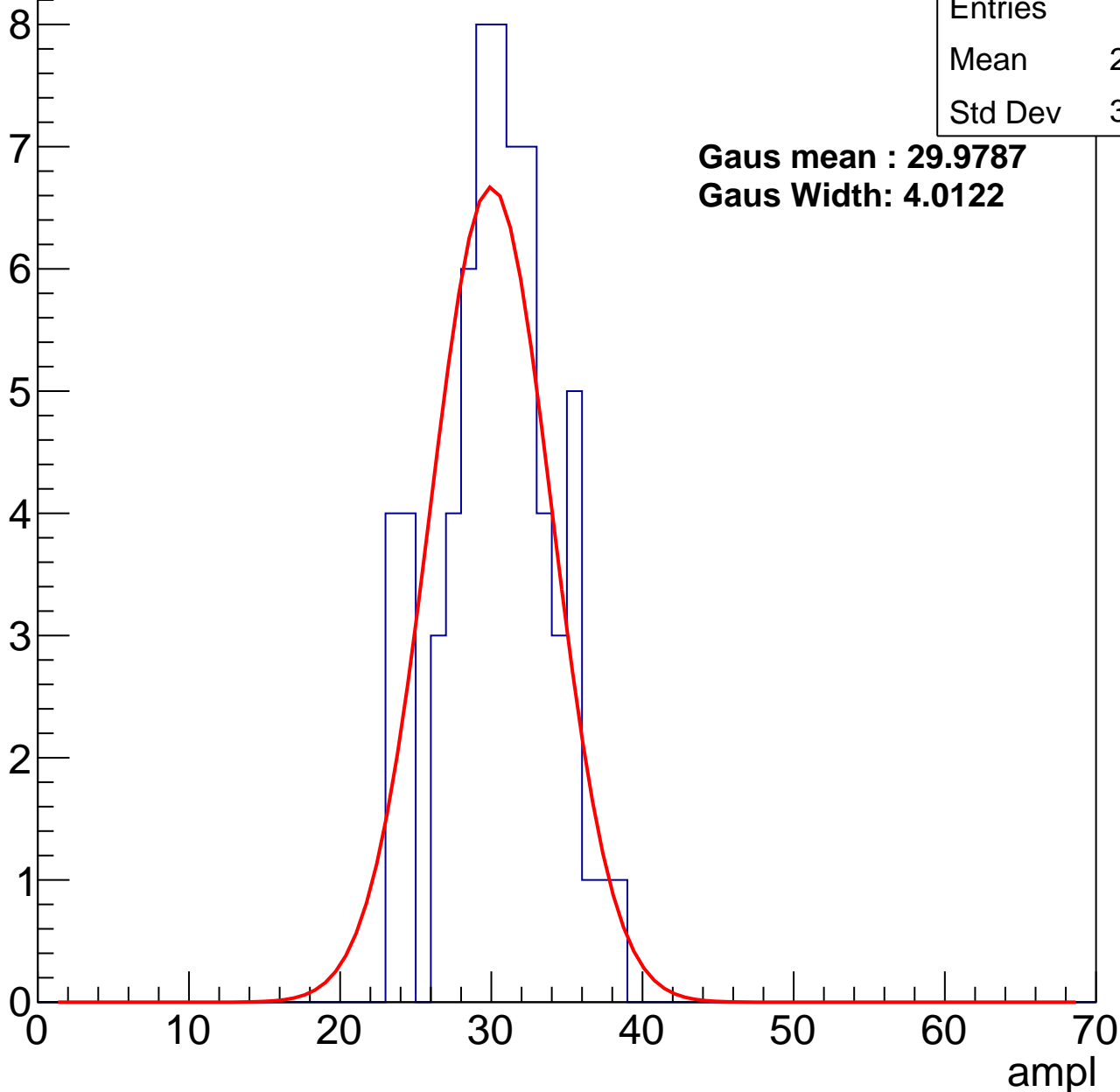
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	29.92
Std Dev	3.586

**Gaus mean : 29.9787**

**Gaus Width: 4.0122**



# B1L101S, U16-ch68, adc1

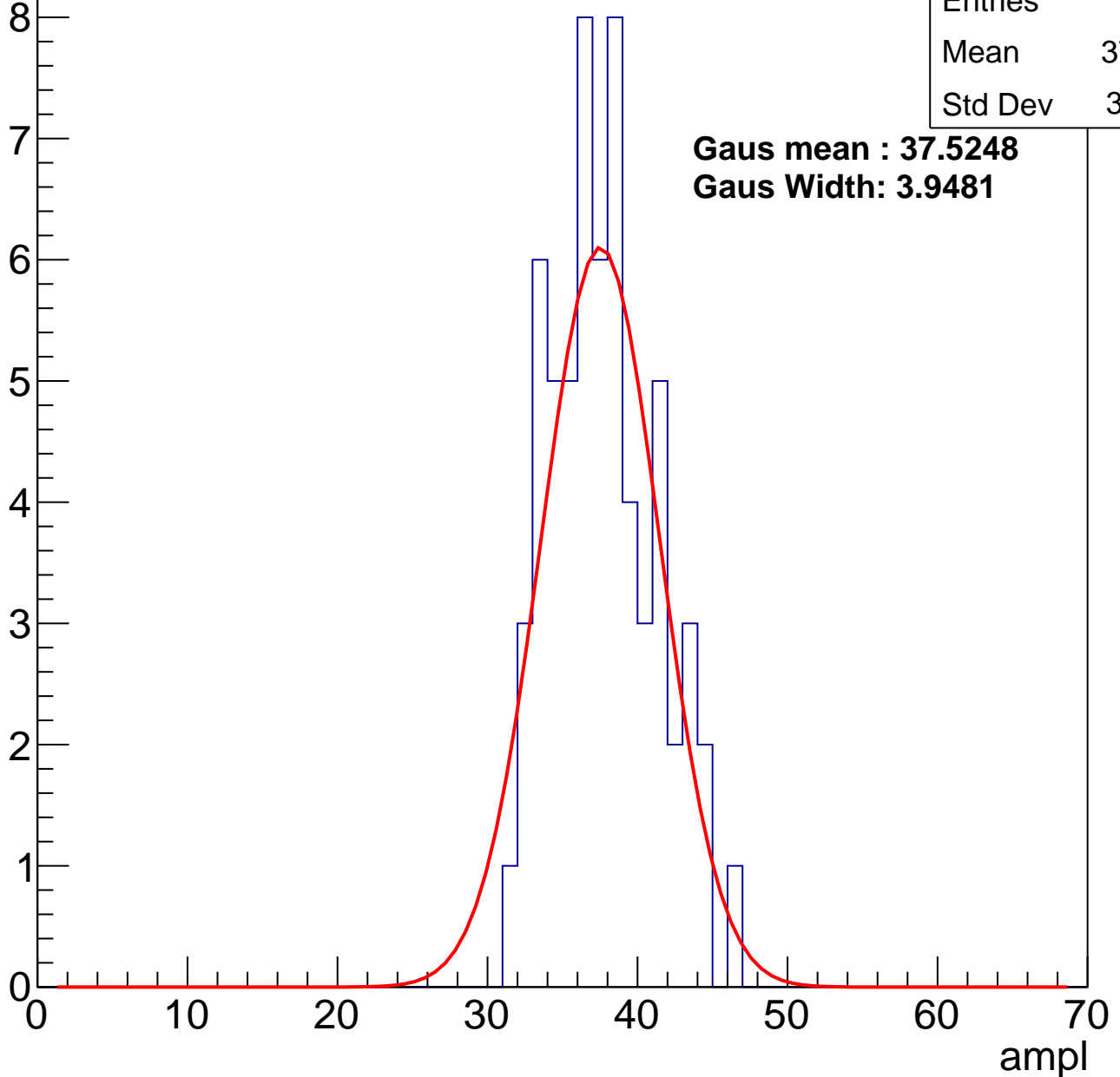
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	37.29
Std Dev	3.461

**Gaus mean : 37.5248**

**Gaus Width: 3.9481**



# B1L101S, U16-ch68, adc2

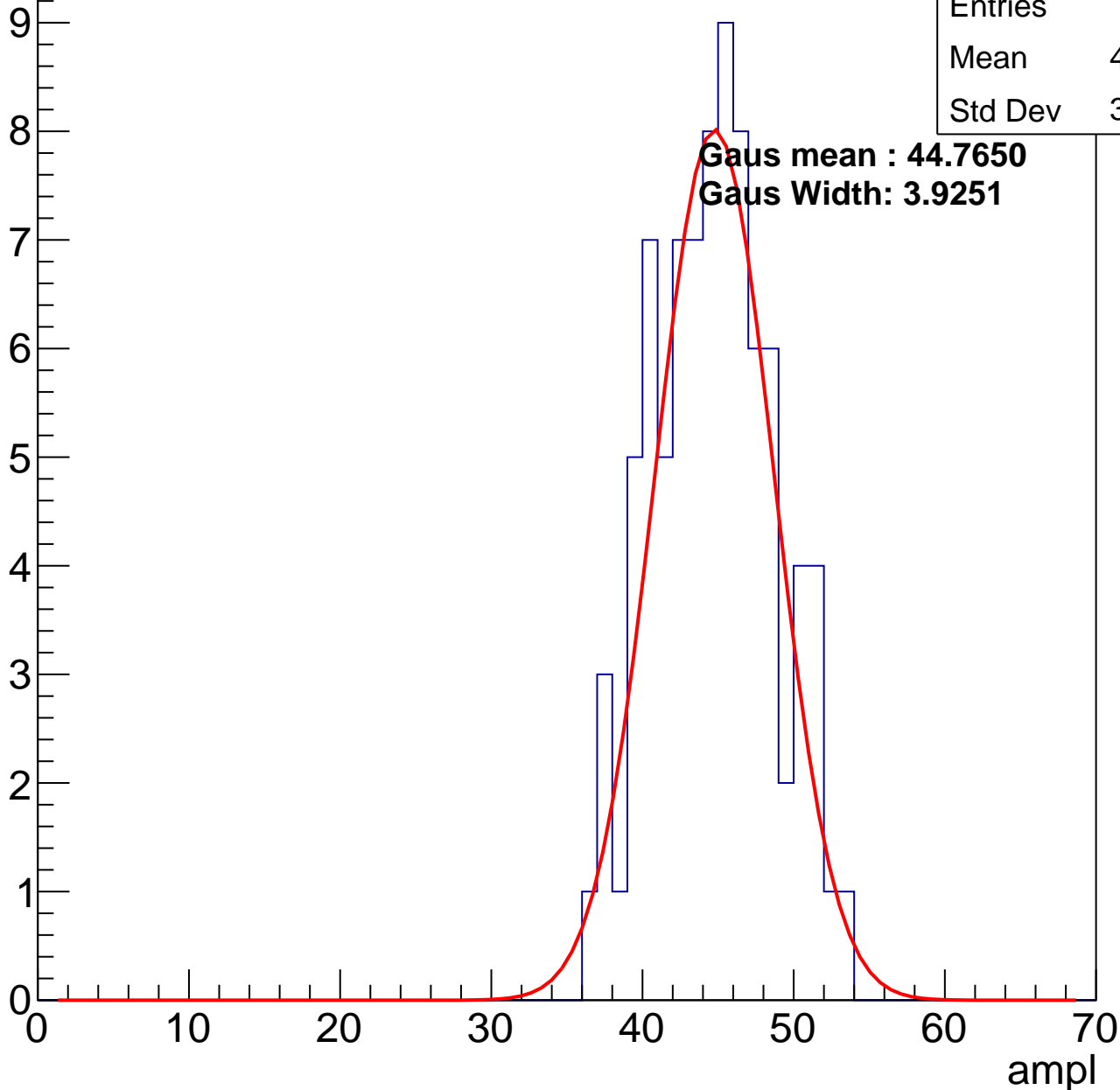
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	85
Mean	44.26
Std Dev	3.887

**Gaus mean : 44.7650**

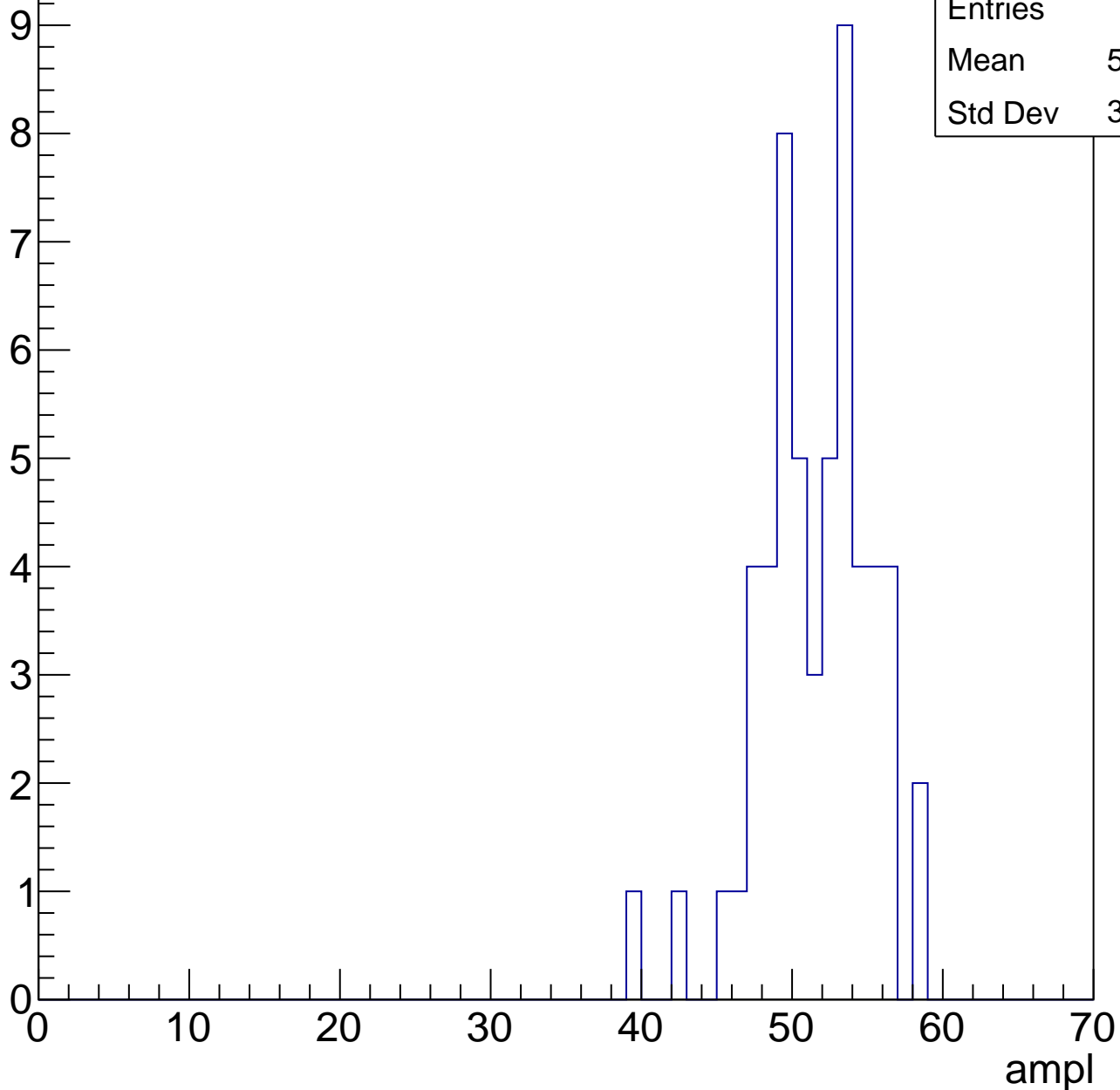
**Gaus Width: 3.9251**



# B1L101S, U16-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

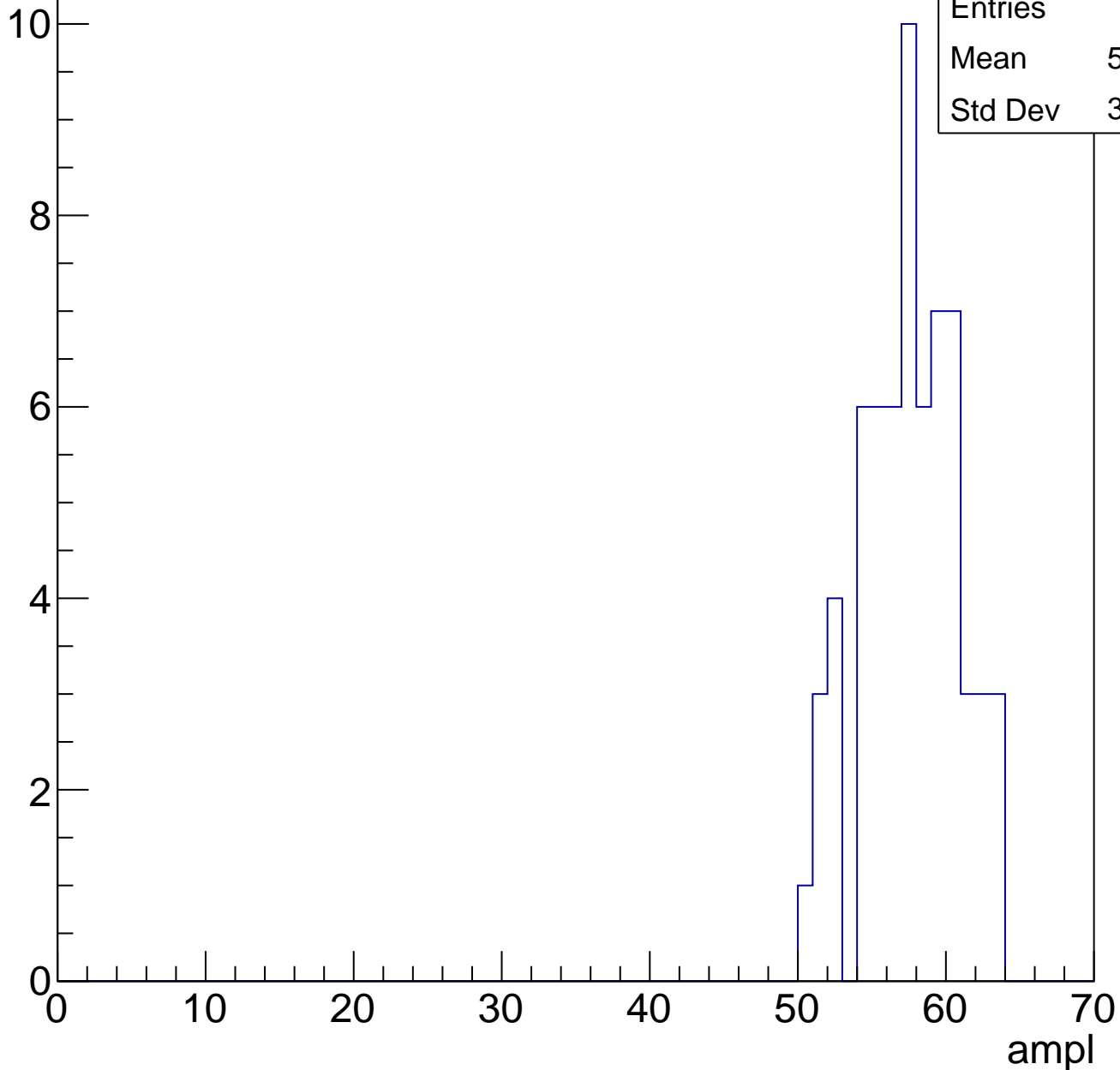


# B1L101S, U16-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	65
Mean	57.08
Std Dev	3.207

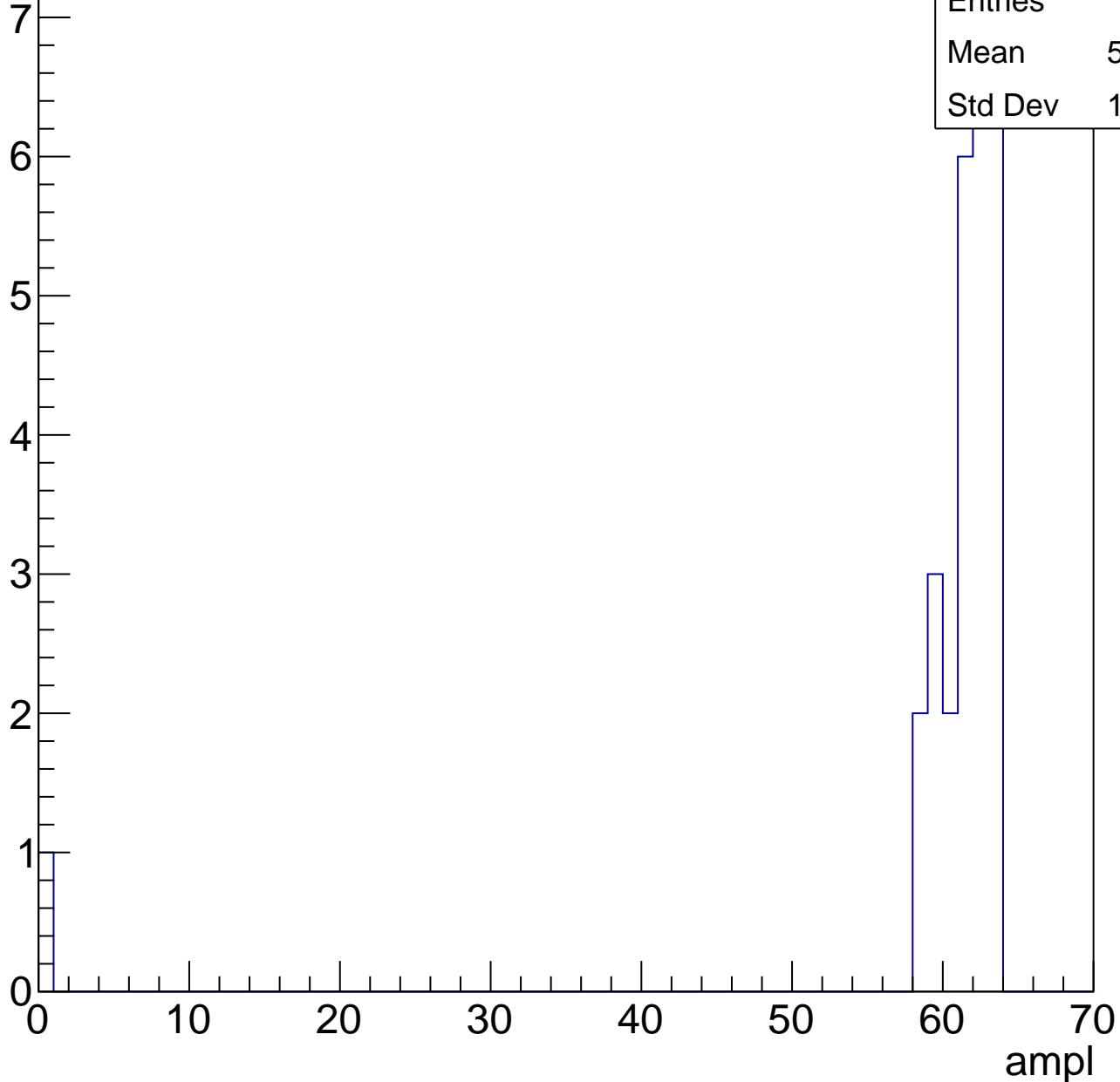
Entry



# B1L101S, U16-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U16-ch69, adc0

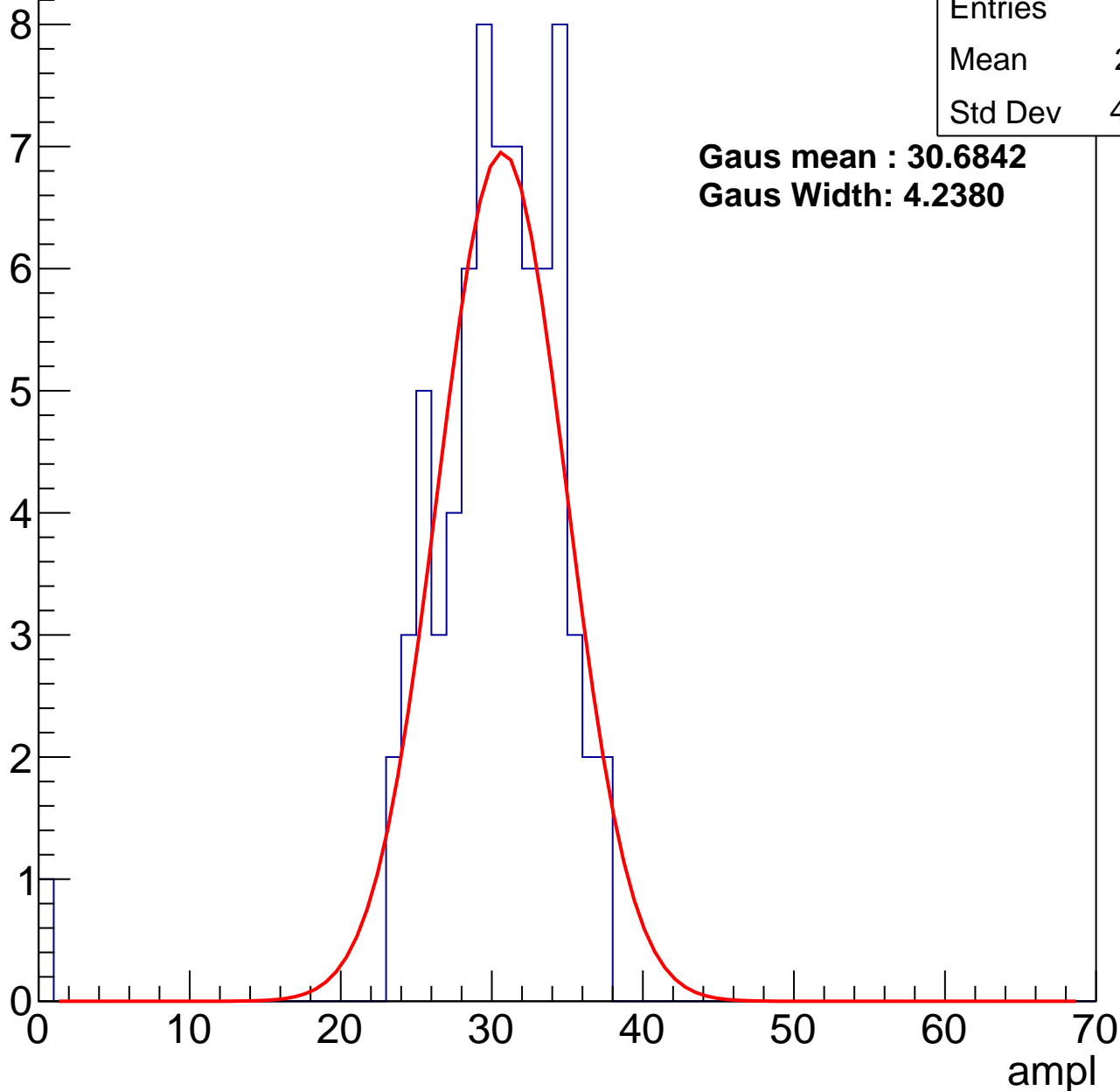
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	29.71
Std Dev	4.964

**Gaus mean : 30.6842**

**Gaus Width: 4.2380**



# B1L101S, U16-ch69, adc1

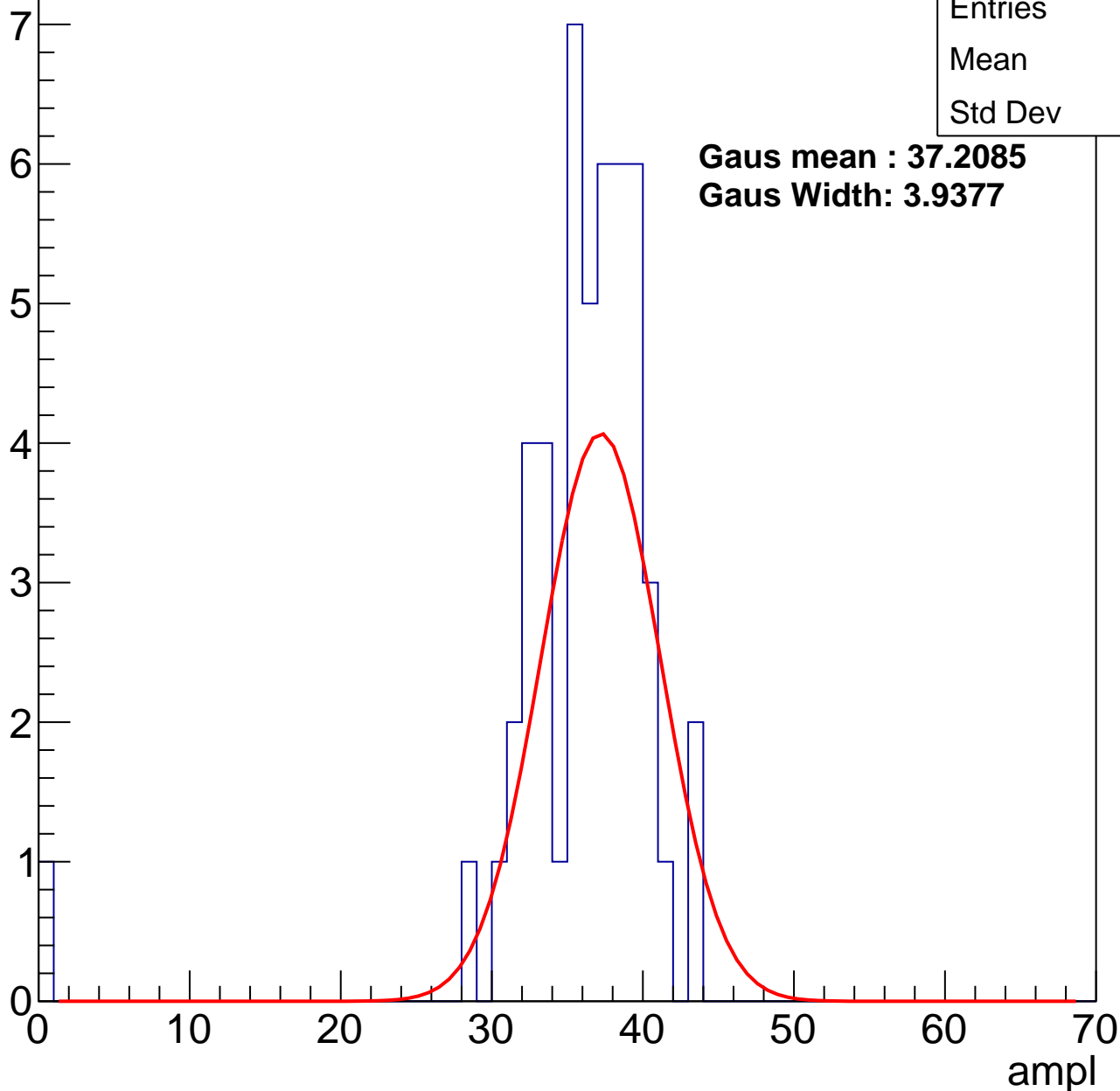
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	35.4
Std Dev	5.99

**Gaus mean : 37.2085**

**Gaus Width: 3.9377**



# B1L101S, U16-ch69, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	42.71
Std Dev	3.494

**Gaus mean : 42.4719**

**Gaus Width: 3.5279**

10

8

6

4

2

0

0

10

20

30

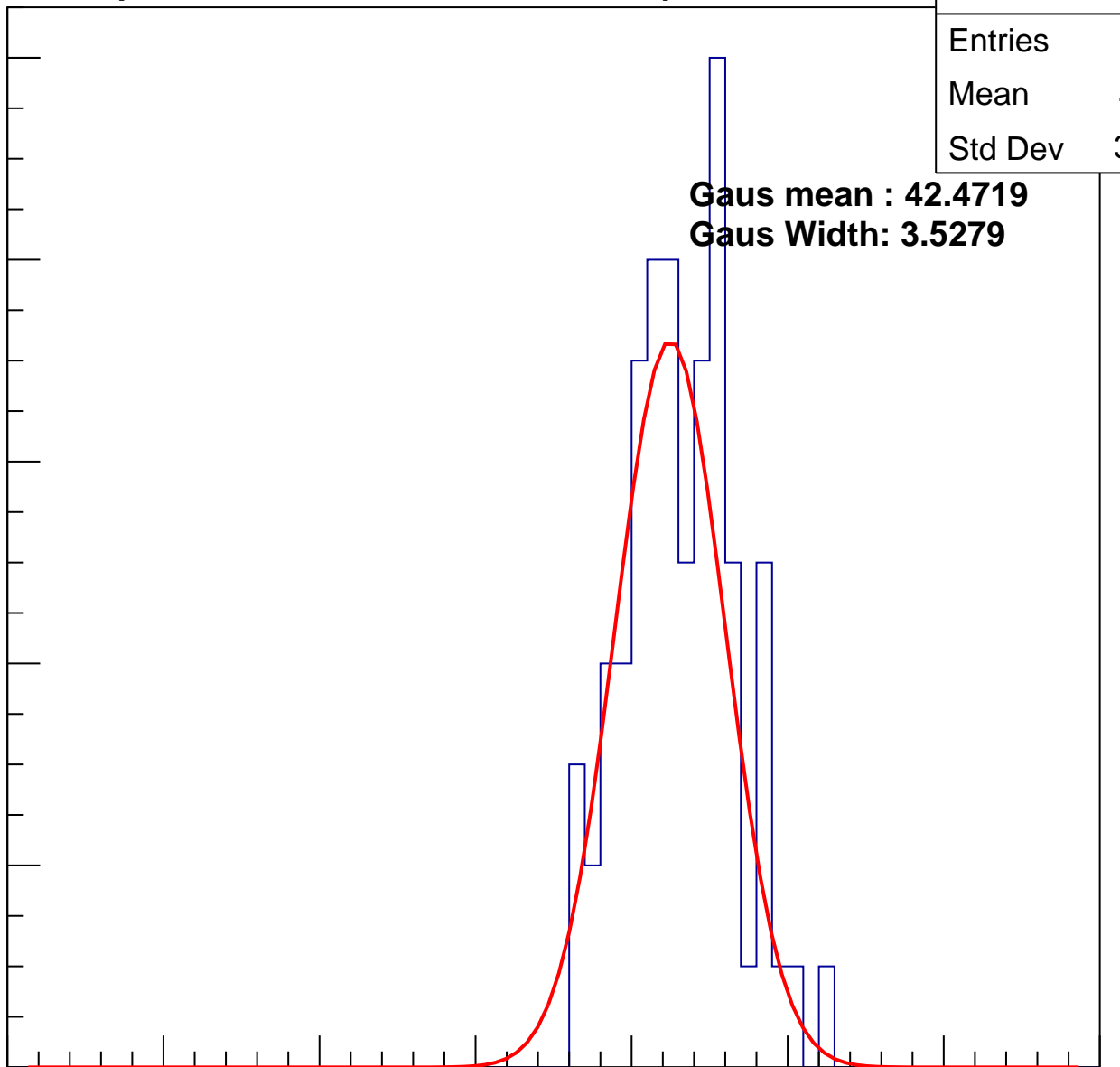
40

50

60

70

ampl

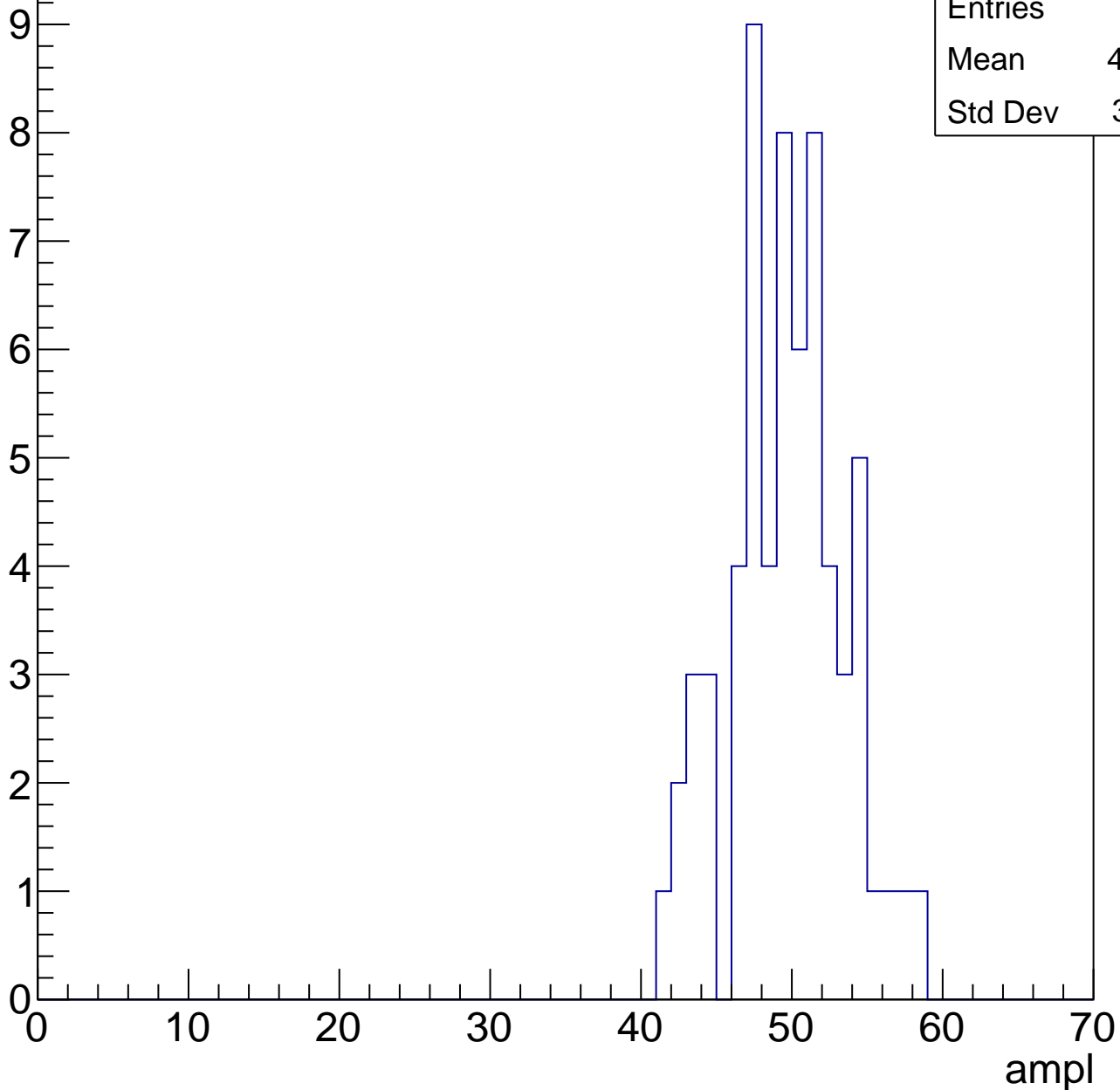


# B1L101S, U16-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	49.19
Std Dev	3.741

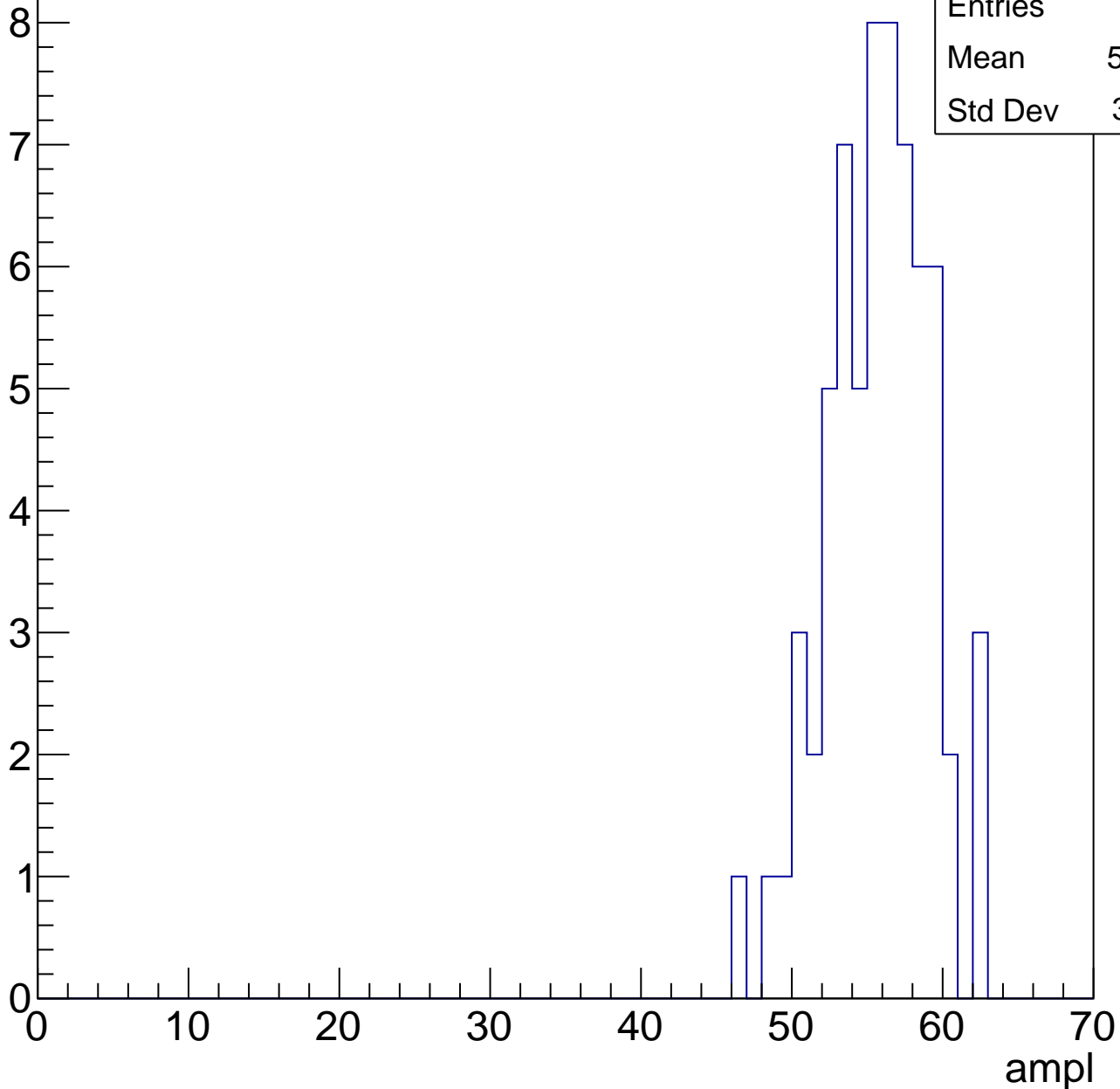


# B1L101S, U16-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

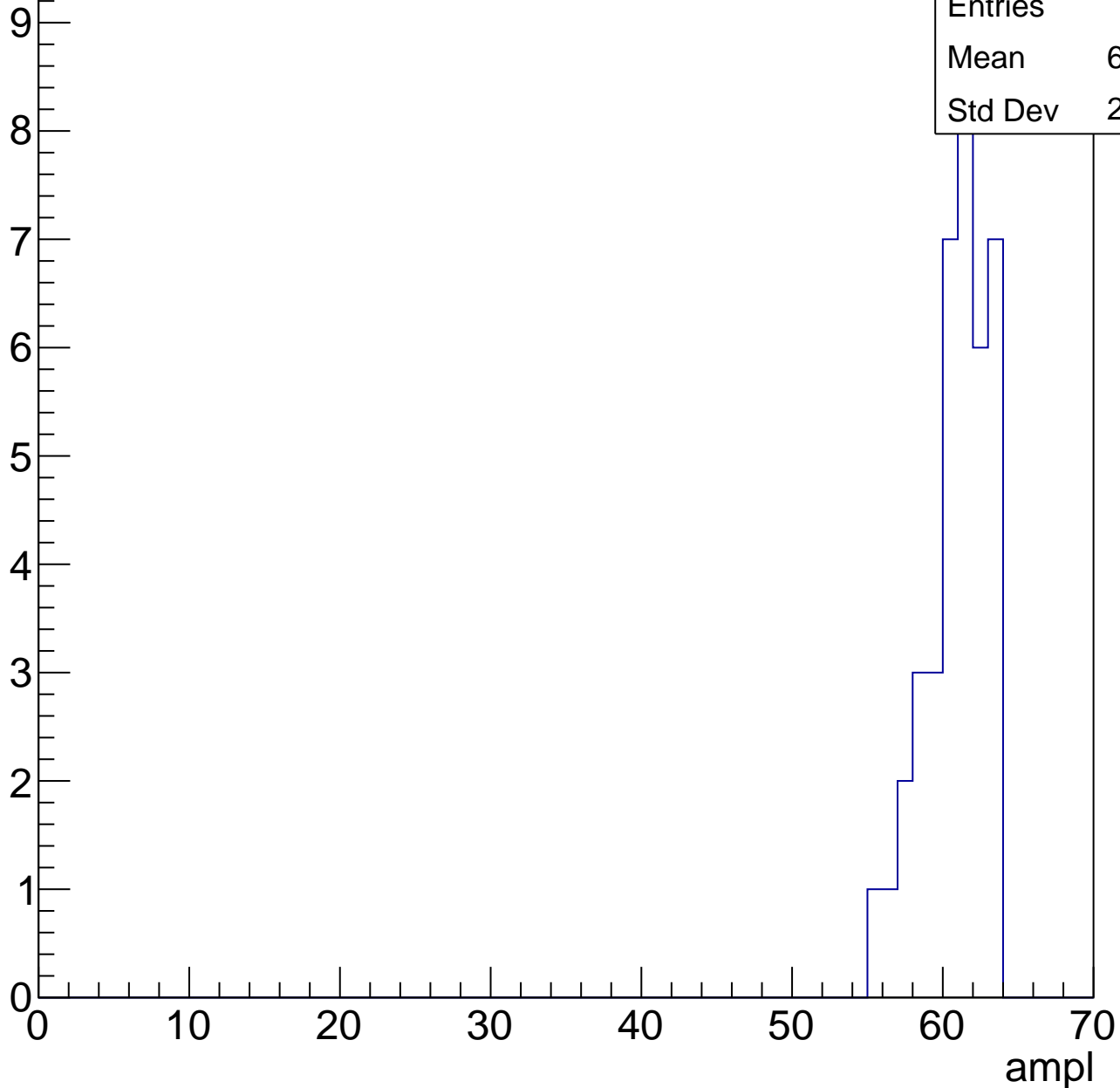
Entries	65
Mean	55.25
Std Dev	3.351



# B1L101S, U16-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

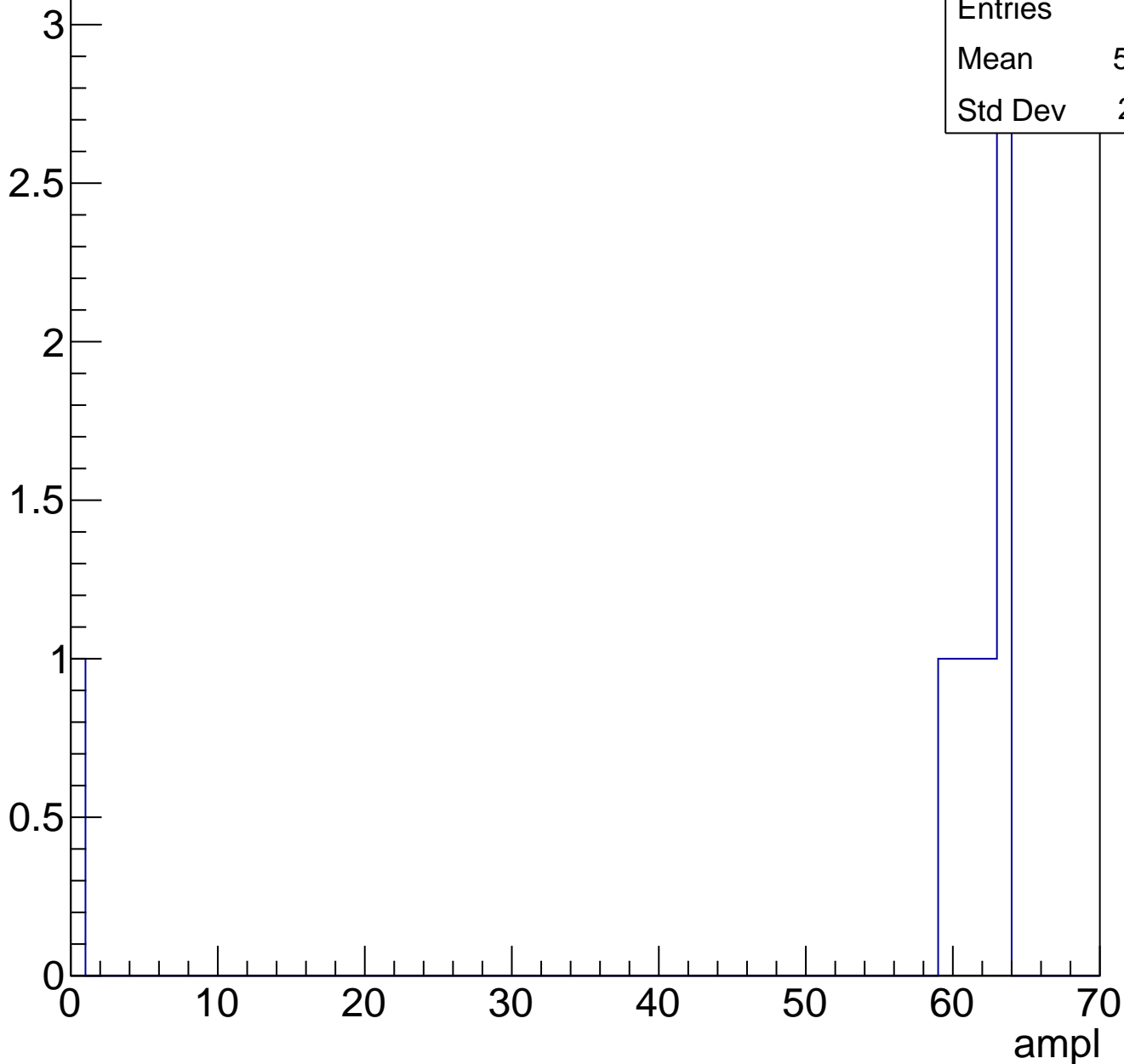


Entries	39
Mean	60.46
Std Dev	2.036

# B1L101S, U16-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U16-ch70, adc0

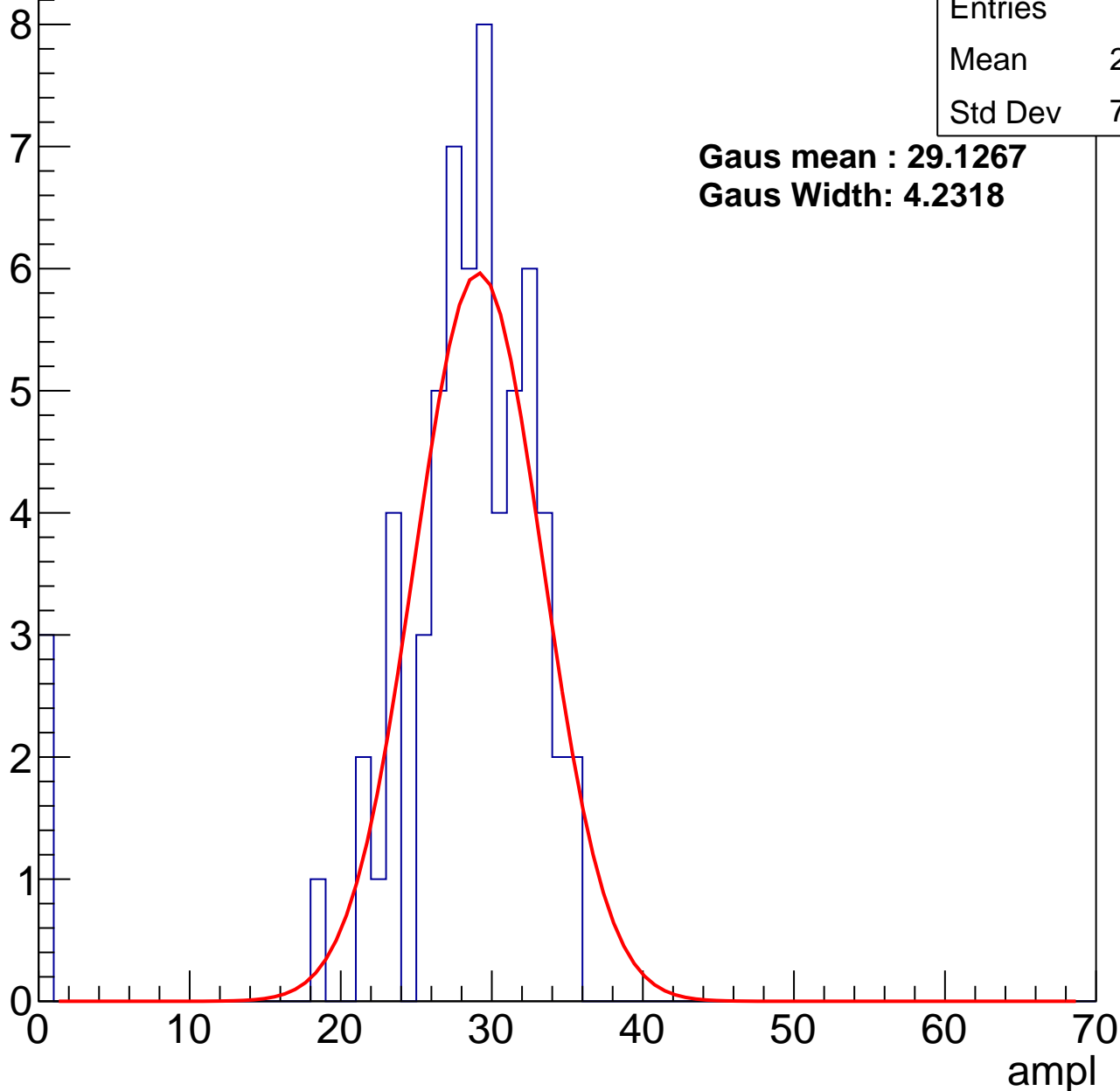
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	27.06
Std Dev	7.037

**Gaus mean : 29.1267**

**Gaus Width: 4.2318**



# B1L101S, U16-ch70, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	79
Mean	35.63
Std Dev	3.997

**Gaus mean : 36.3495**

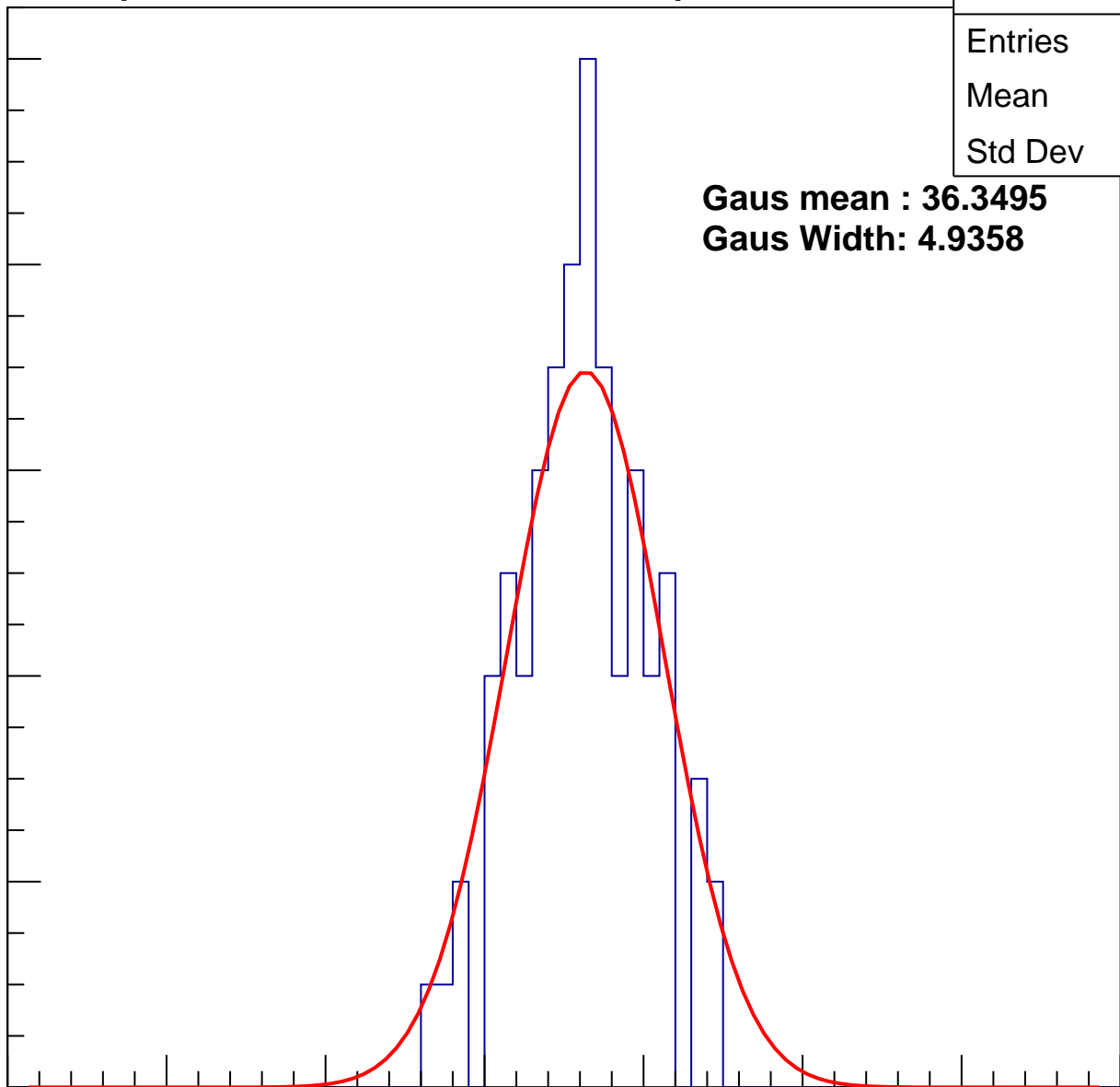
**Gaus Width: 4.9358**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch70, adc2

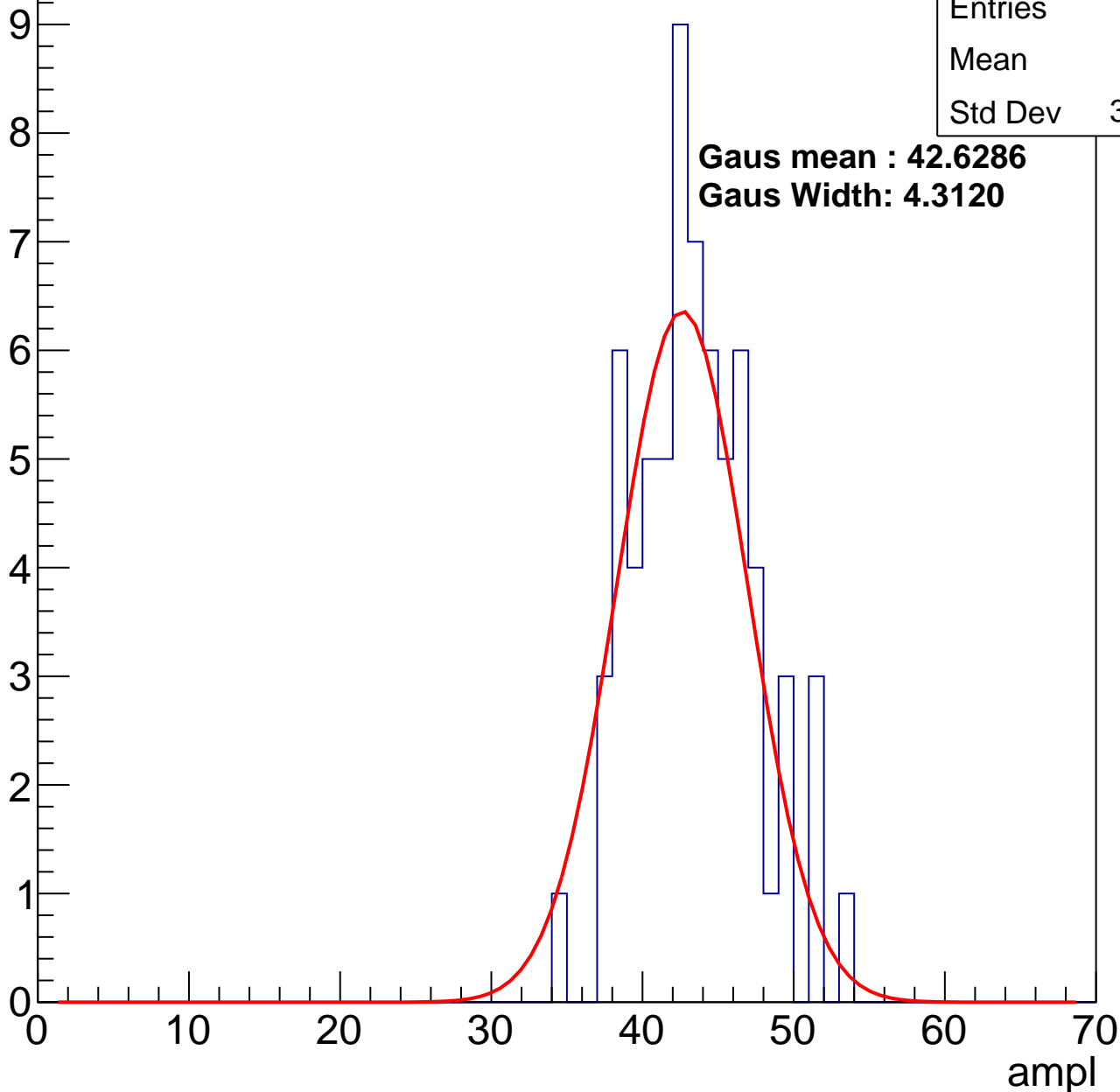
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	43
Std Dev	3.894

**Gaus mean : 42.6286**

**Gaus Width: 4.3120**

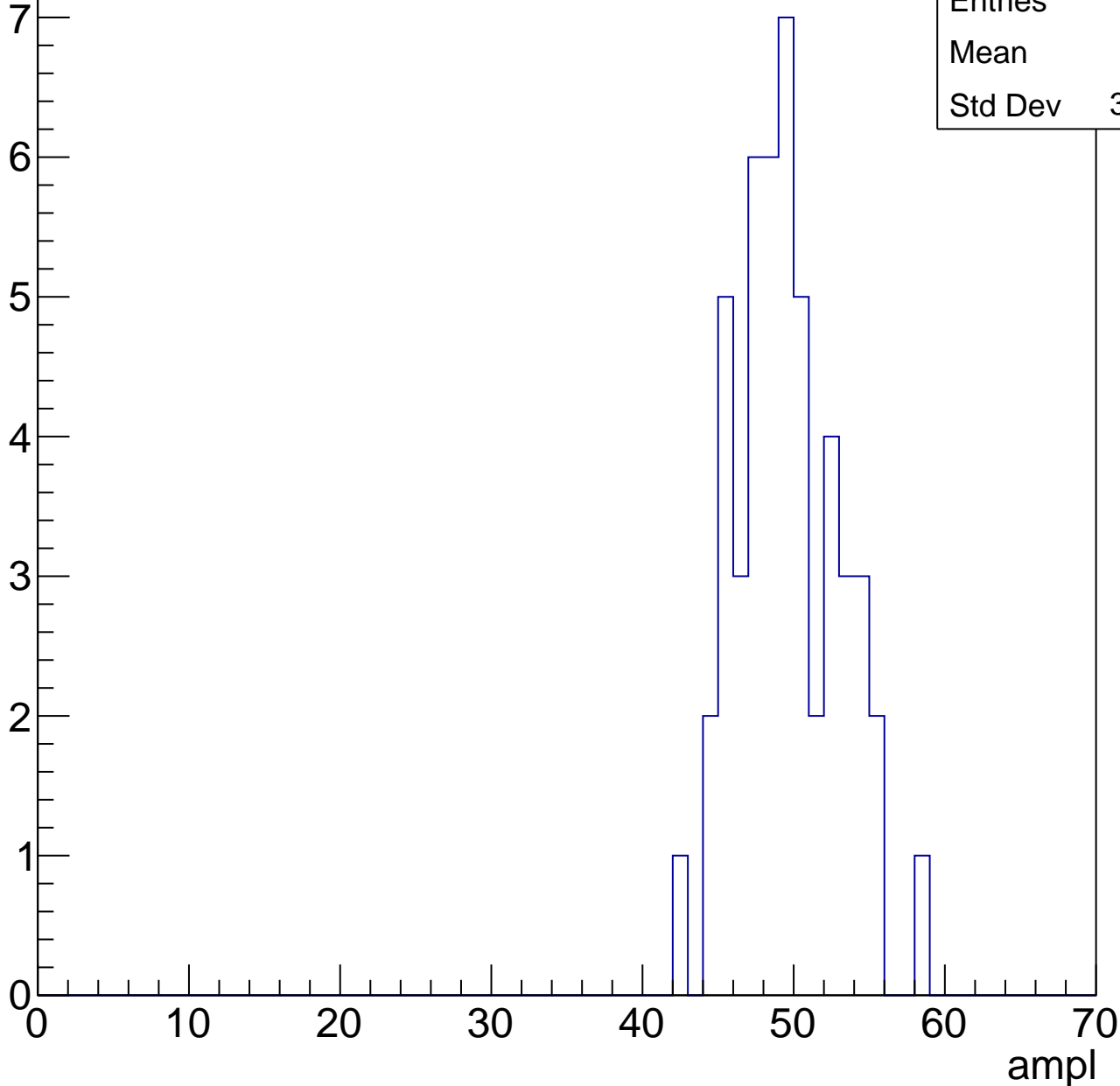


# B1L101S, U16-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

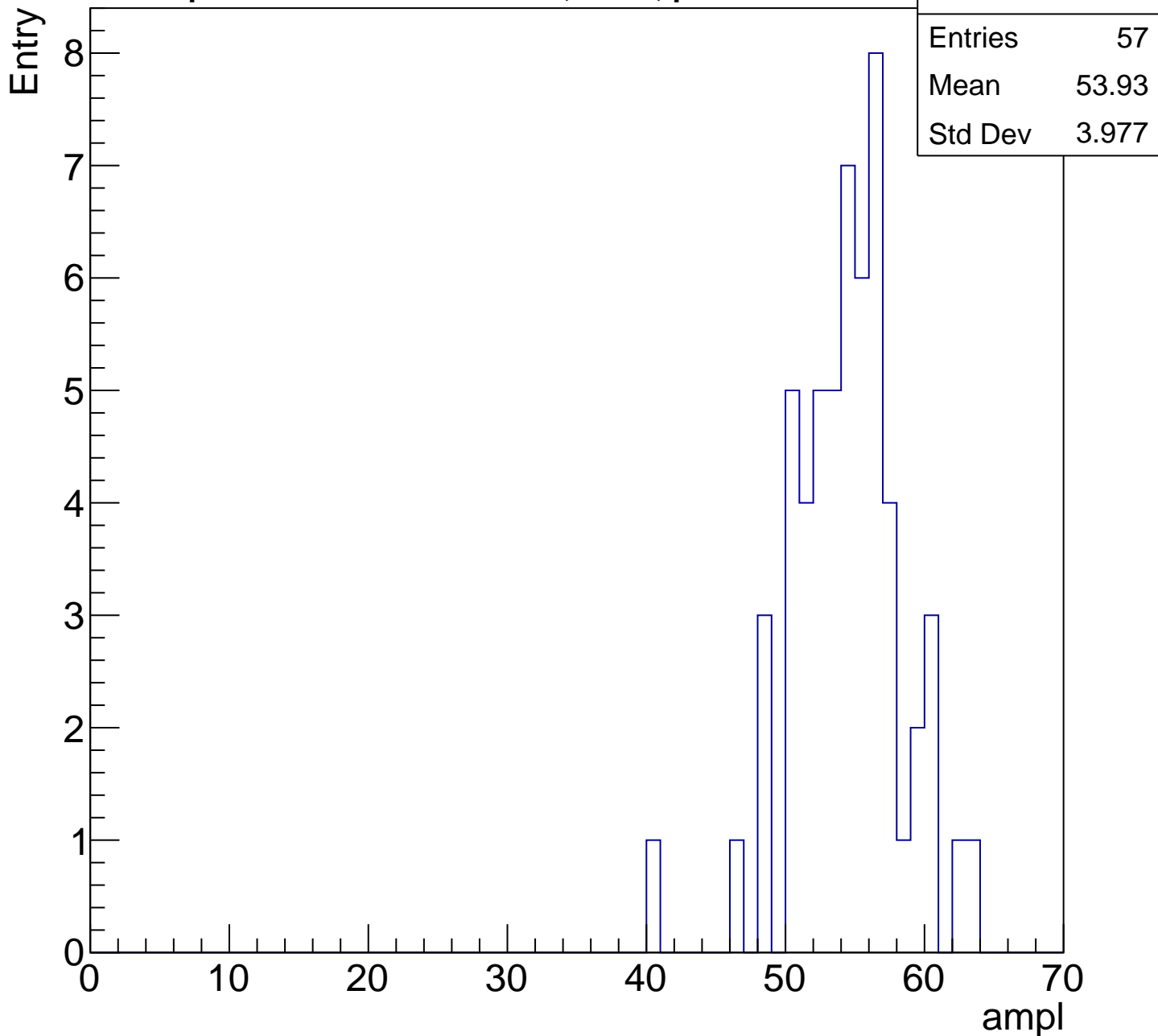
Entry

Entries	50
Mean	49.1
Std Dev	3.348



# B1L101S, U16-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

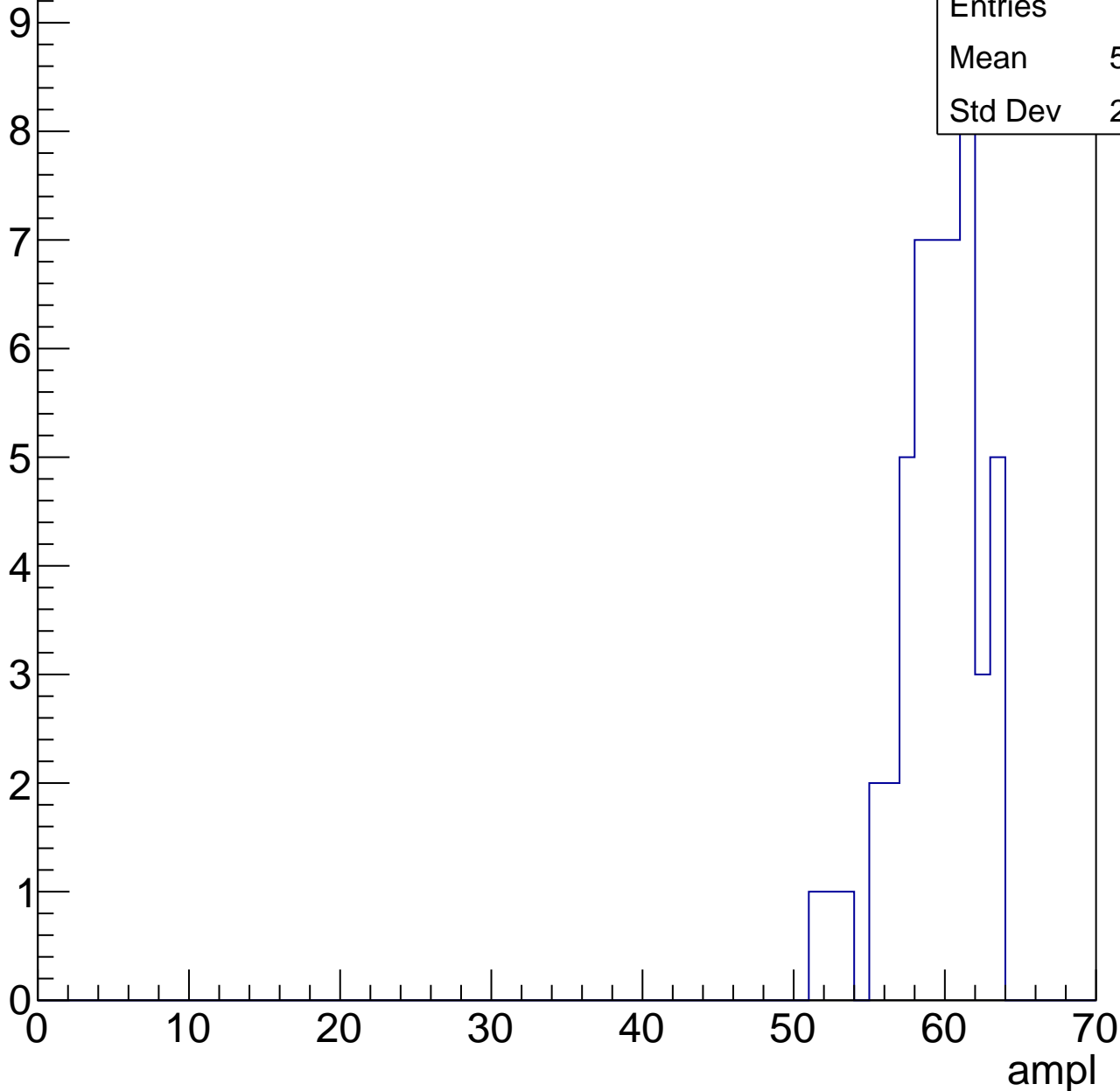


# B1L101S, U16-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	59.04
Std Dev	2.742

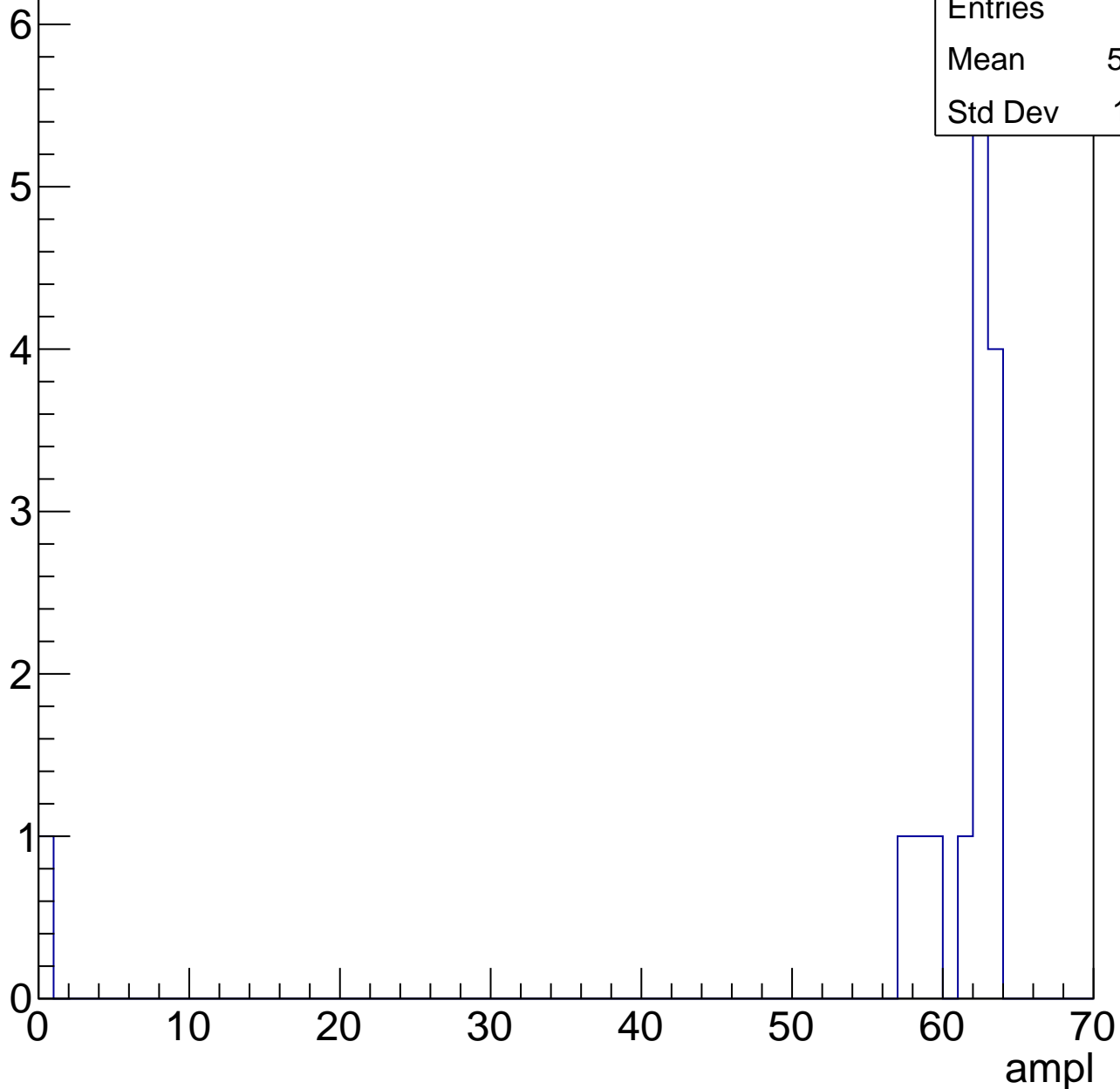


# B1L101S, U16-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	15
Mean	57.27
Std Dev	15.41





# B1L101S, U16-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U16-ch71, adc0

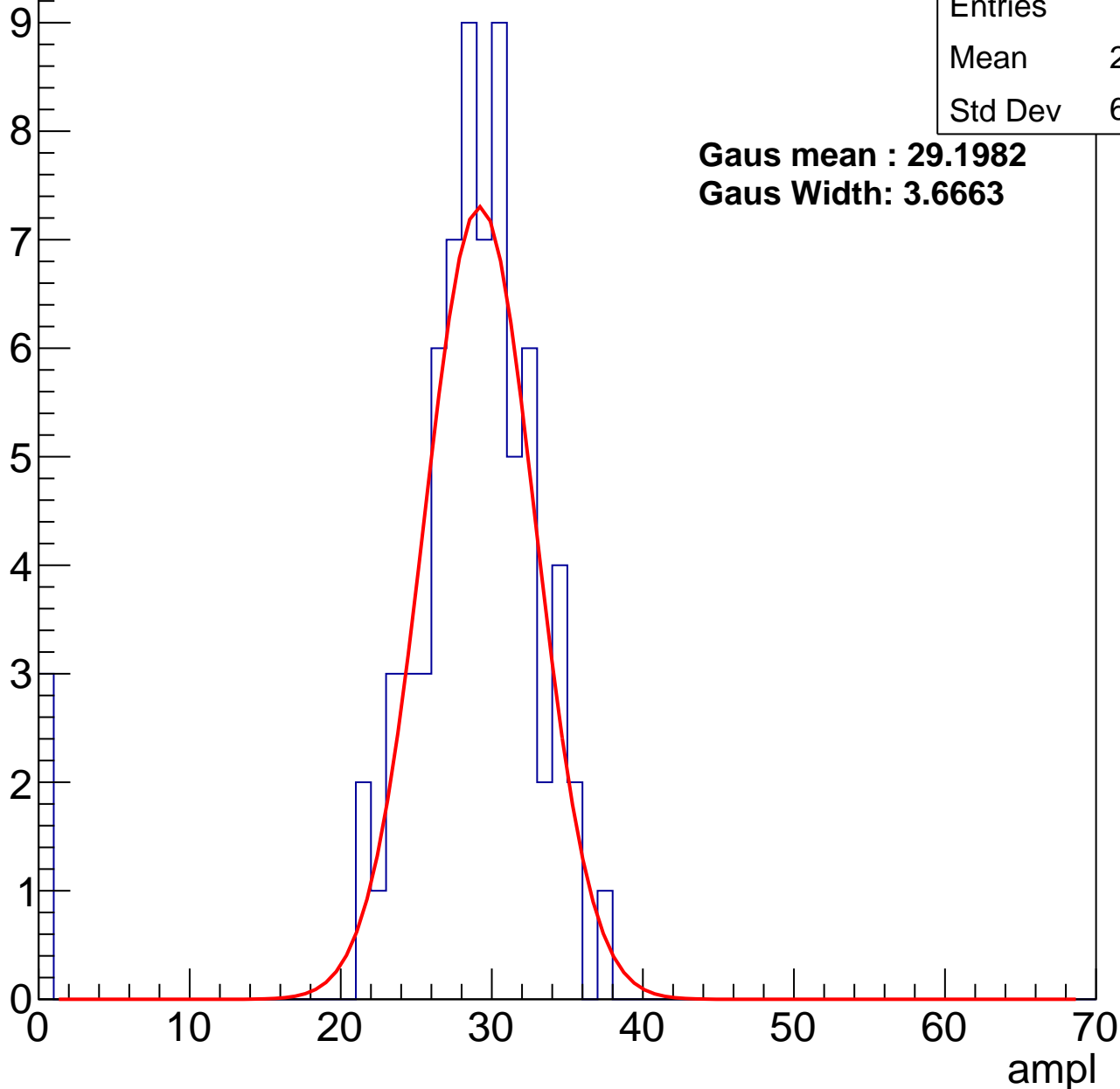
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	27.48
Std Dev	6.625

**Gaus mean : 29.1982**

**Gaus Width: 3.6663**



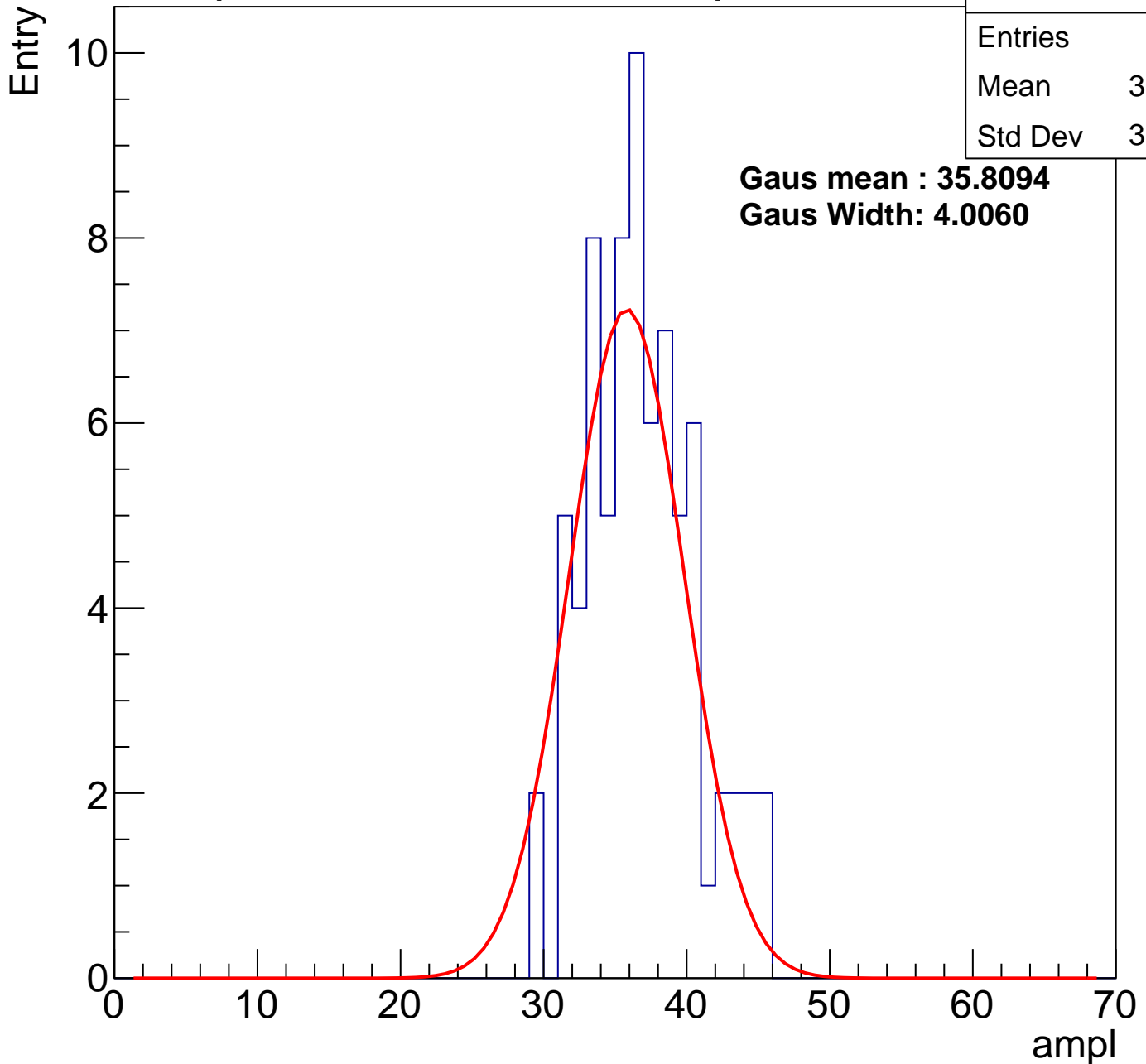
# B1L101S, U16-ch71, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	75
Mean	36.36
Std Dev	3.719

**Gaus mean : 35.8094**

**Gaus Width: 4.0060**



# B1L101S, U16-ch71, adc2

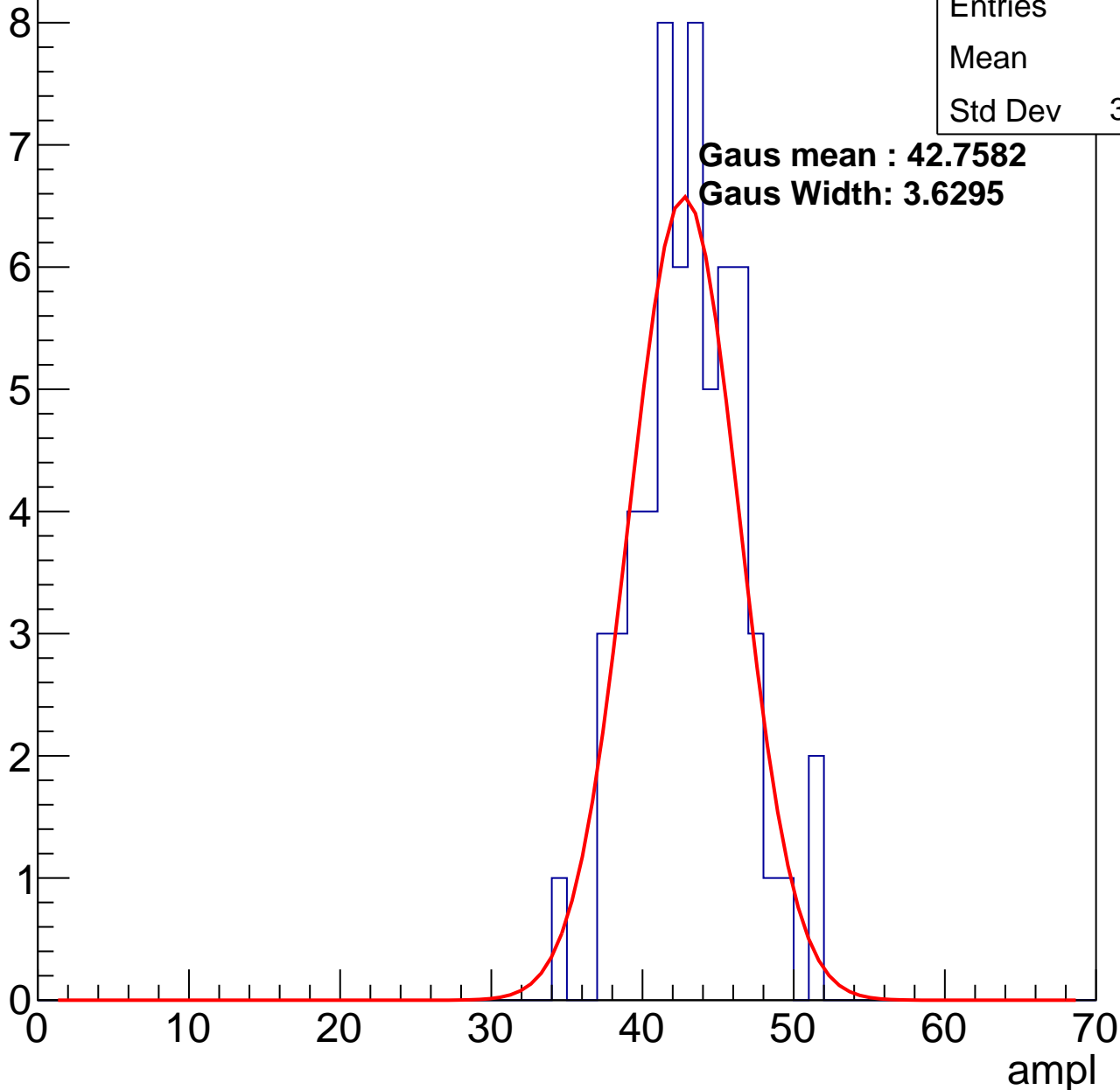
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	42.7
Std Dev	3.428

**Gaus mean : 42.7582**

**Gaus Width: 3.6295**

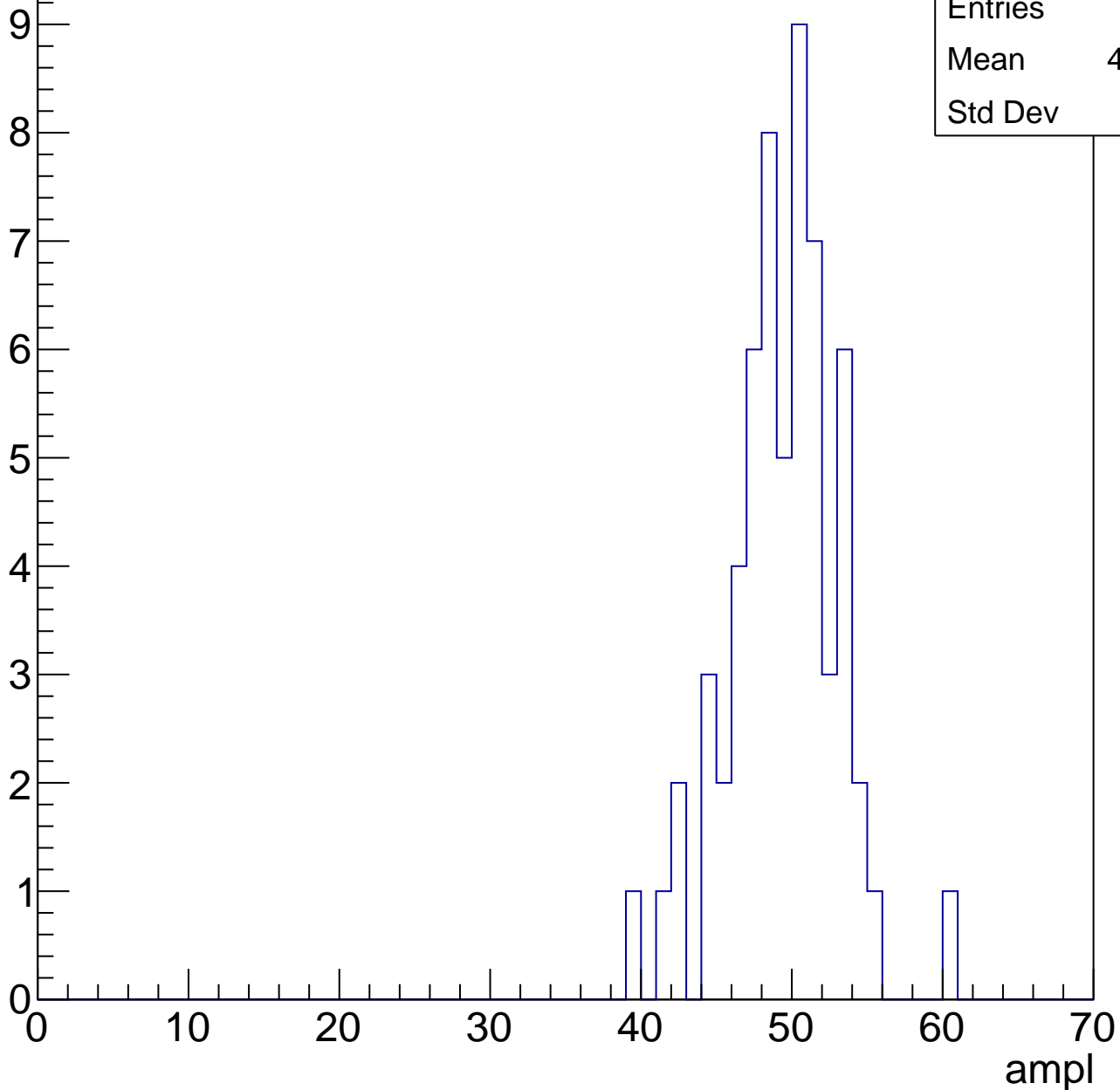


# B1L101S, U16-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	48.93
Std Dev	3.63

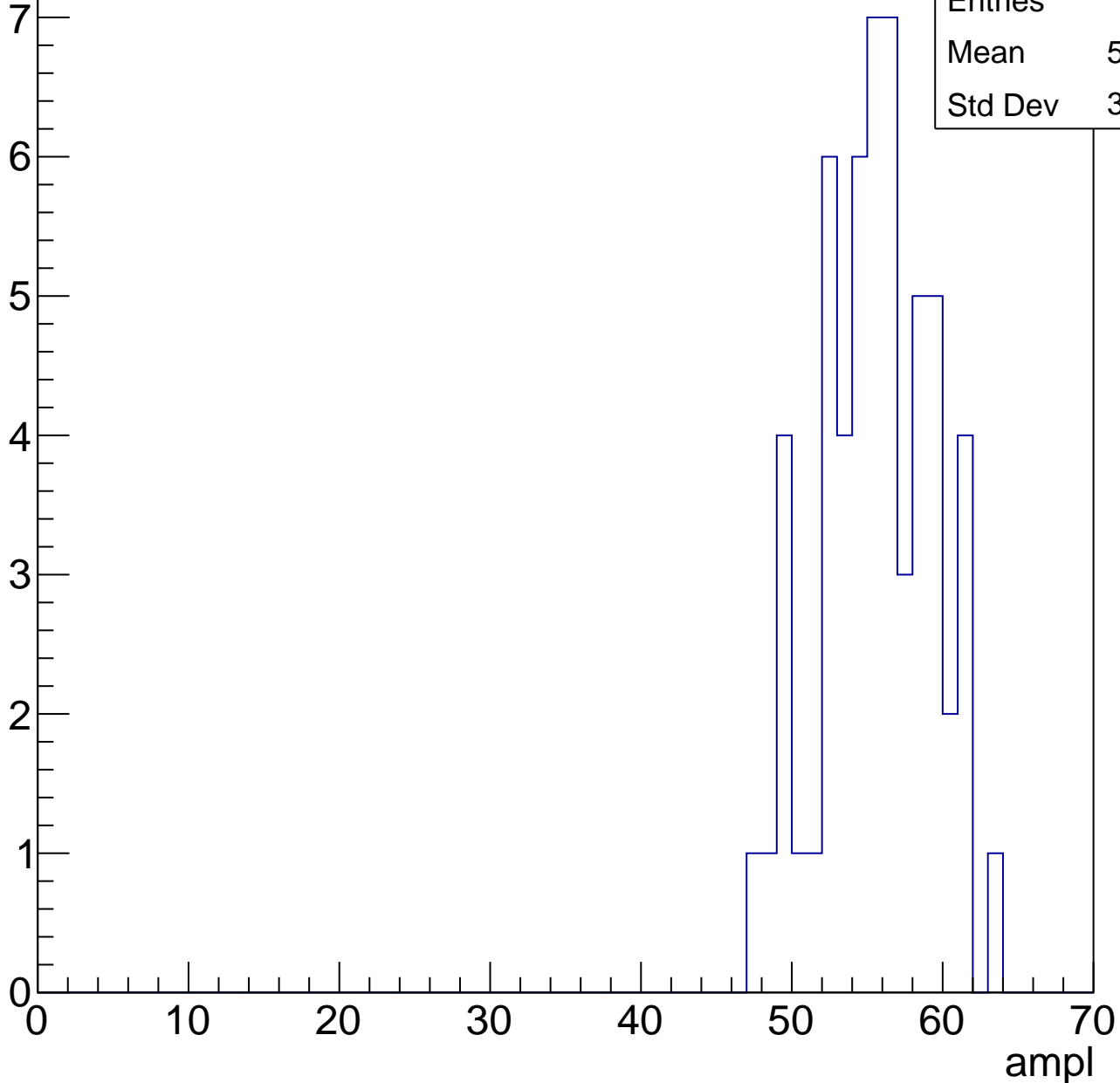


# B1L101S, U16-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	55.17
Std Dev	3.654

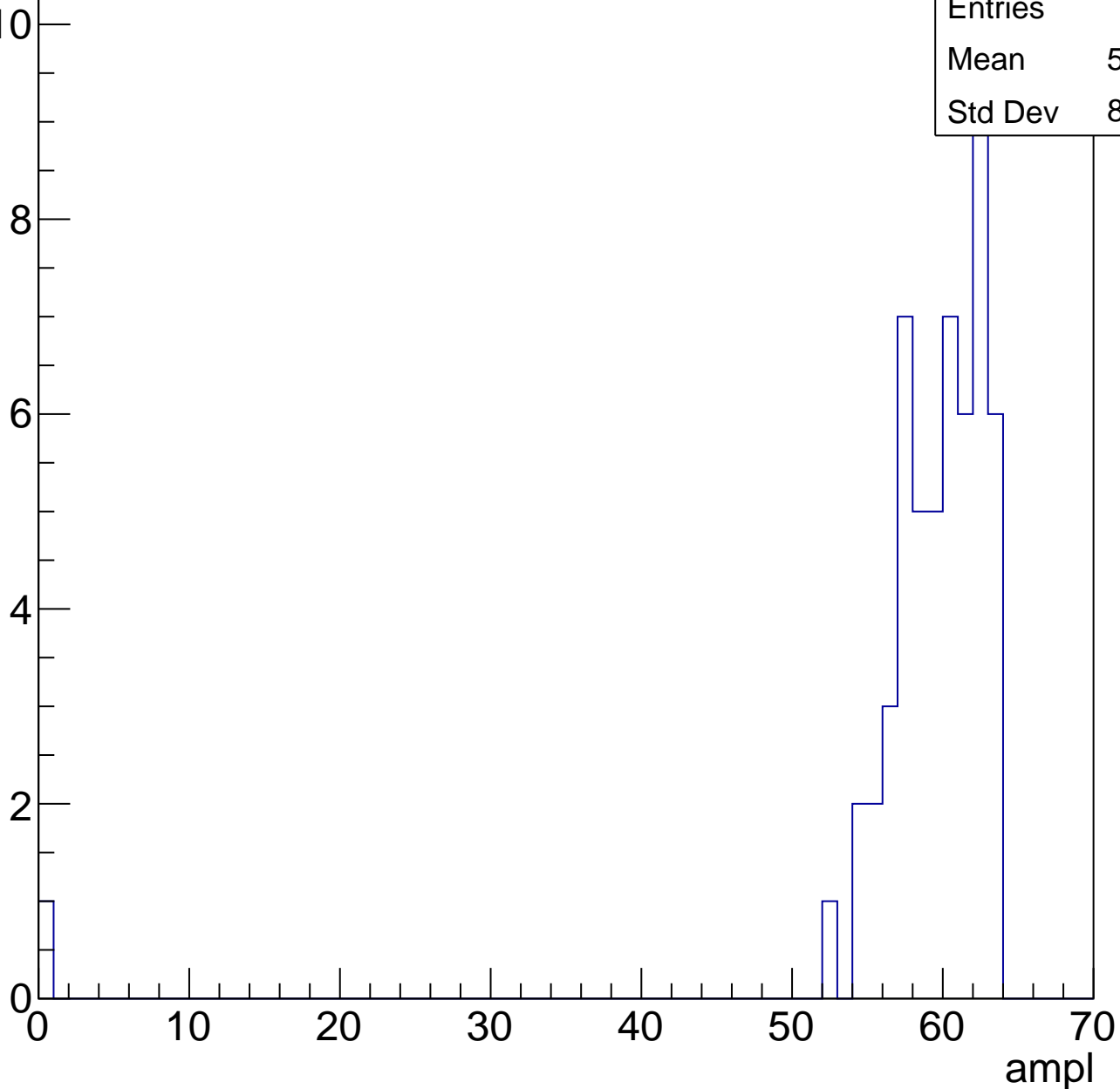


# B1L101S, U16-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	58.29
Std Dev	8.379



# B1L101S, U16-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U16-ch72, adc0

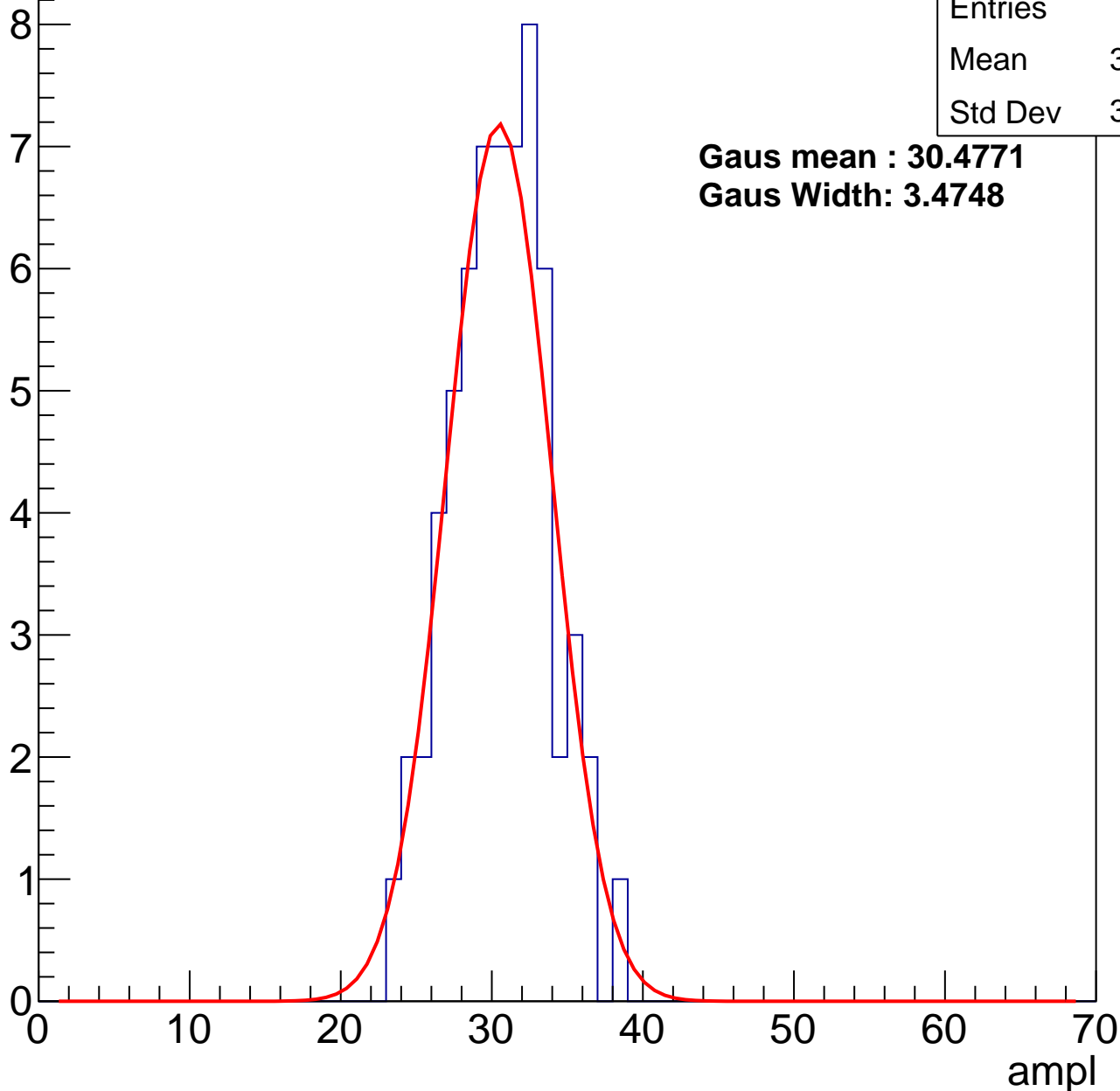
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	30.08
Std Dev	3.204

**Gaus mean : 30.4771**

**Gaus Width: 3.4748**



# B1L101S, U16-ch72, adc1

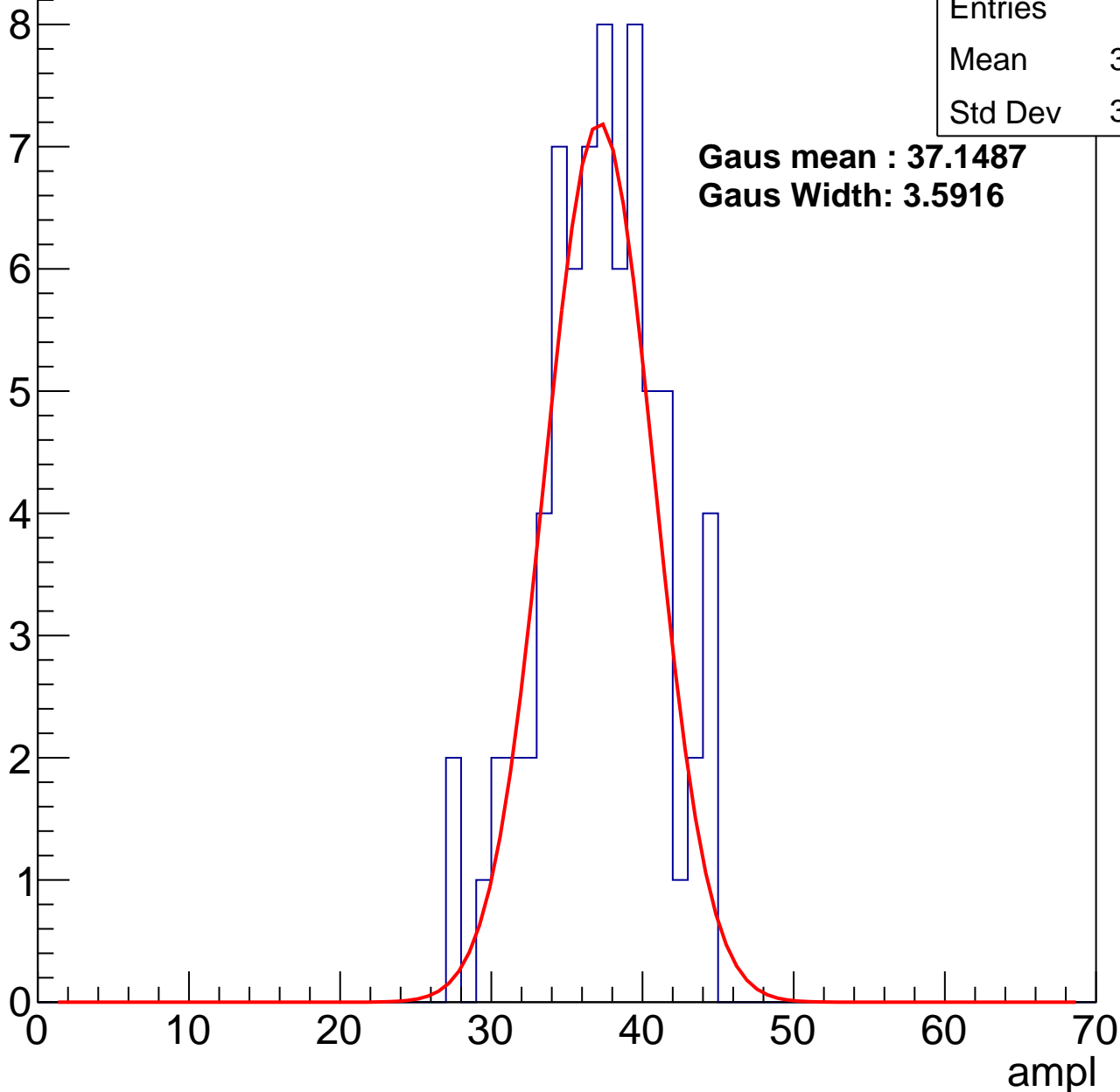
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	36.75
Std Dev	3.897

**Gaus mean : 37.1487**

**Gaus Width: 3.5916**



# B1L101S, U16-ch72, adc2

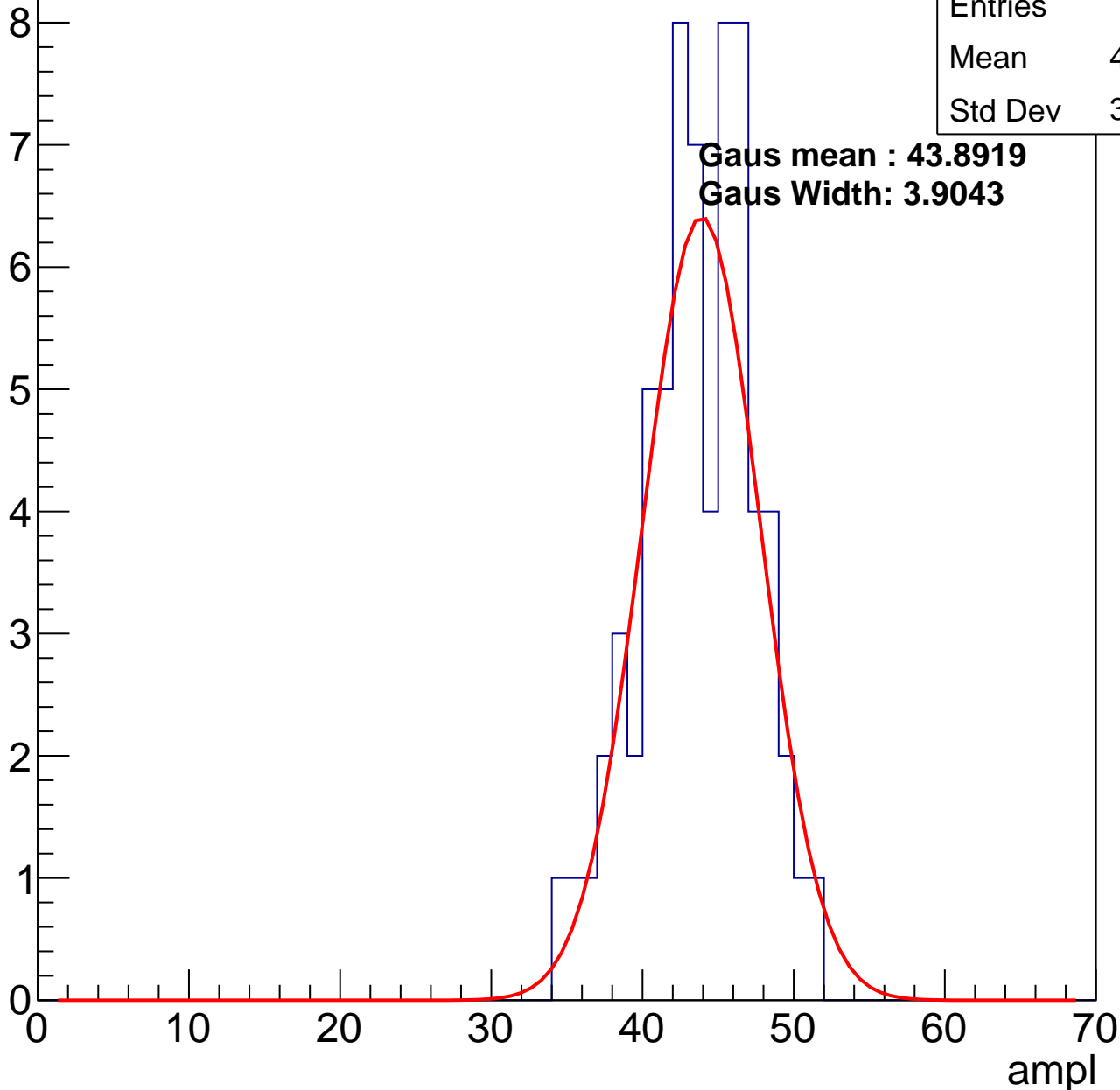
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	43.22
Std Dev	3.664

**Gaus mean : 43.8919**

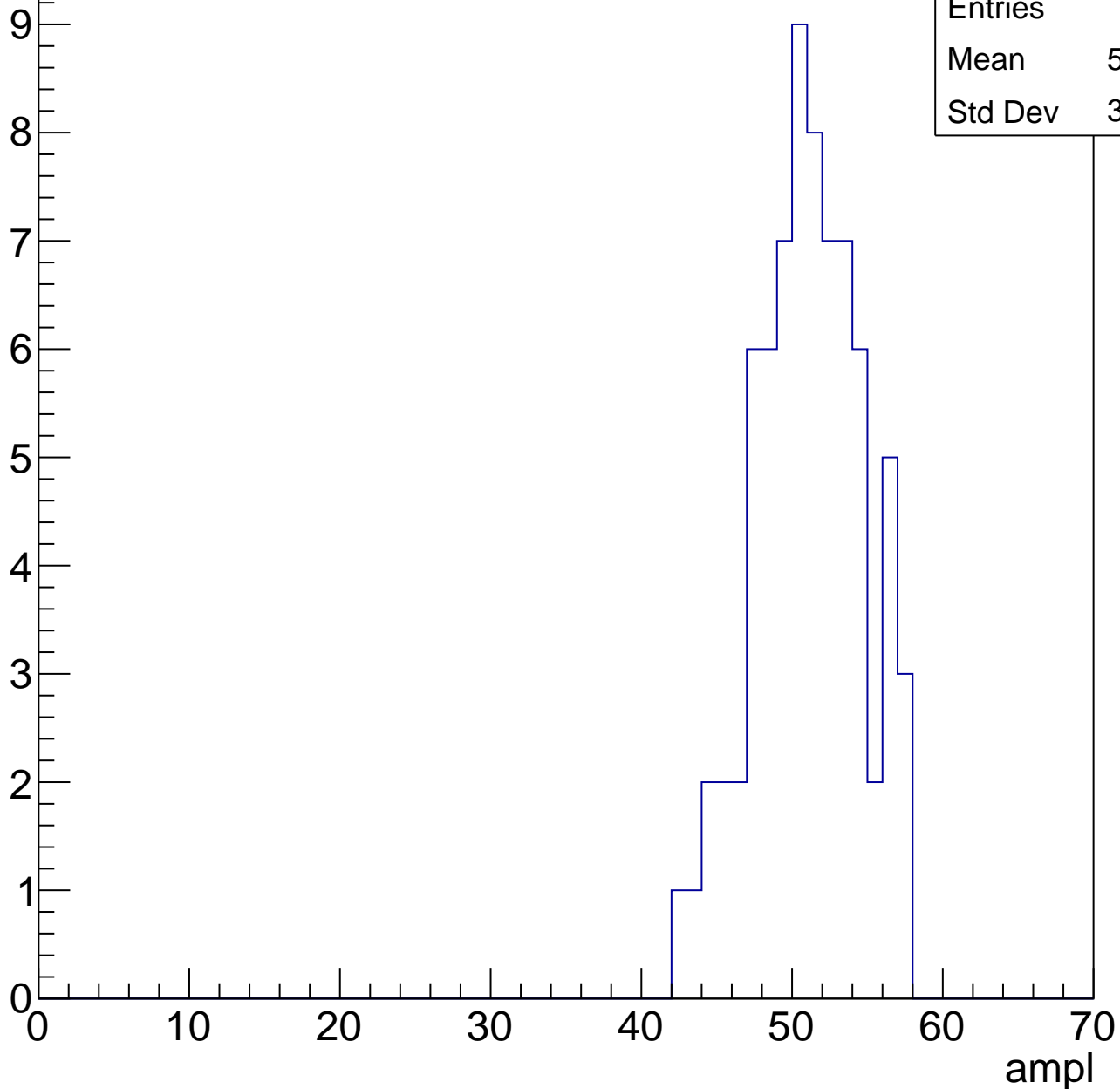
**Gaus Width: 3.9043**



# B1L101S, U16-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



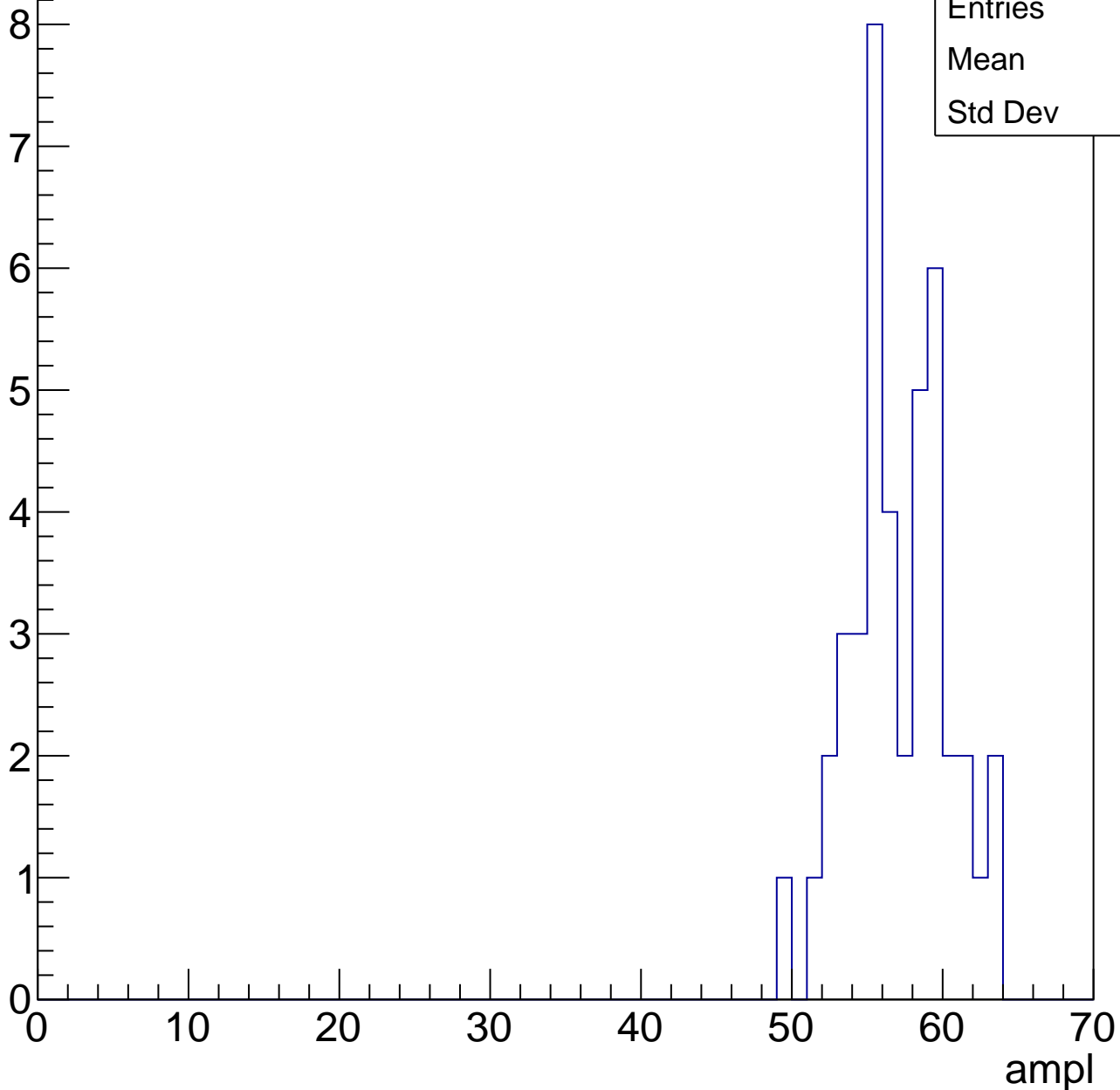
Entries	74
Mean	50.62
Std Dev	3.479

# B1L101S, U16-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	56.6
Std Dev	3.2



# B1L101S, U16-ch72, adc5

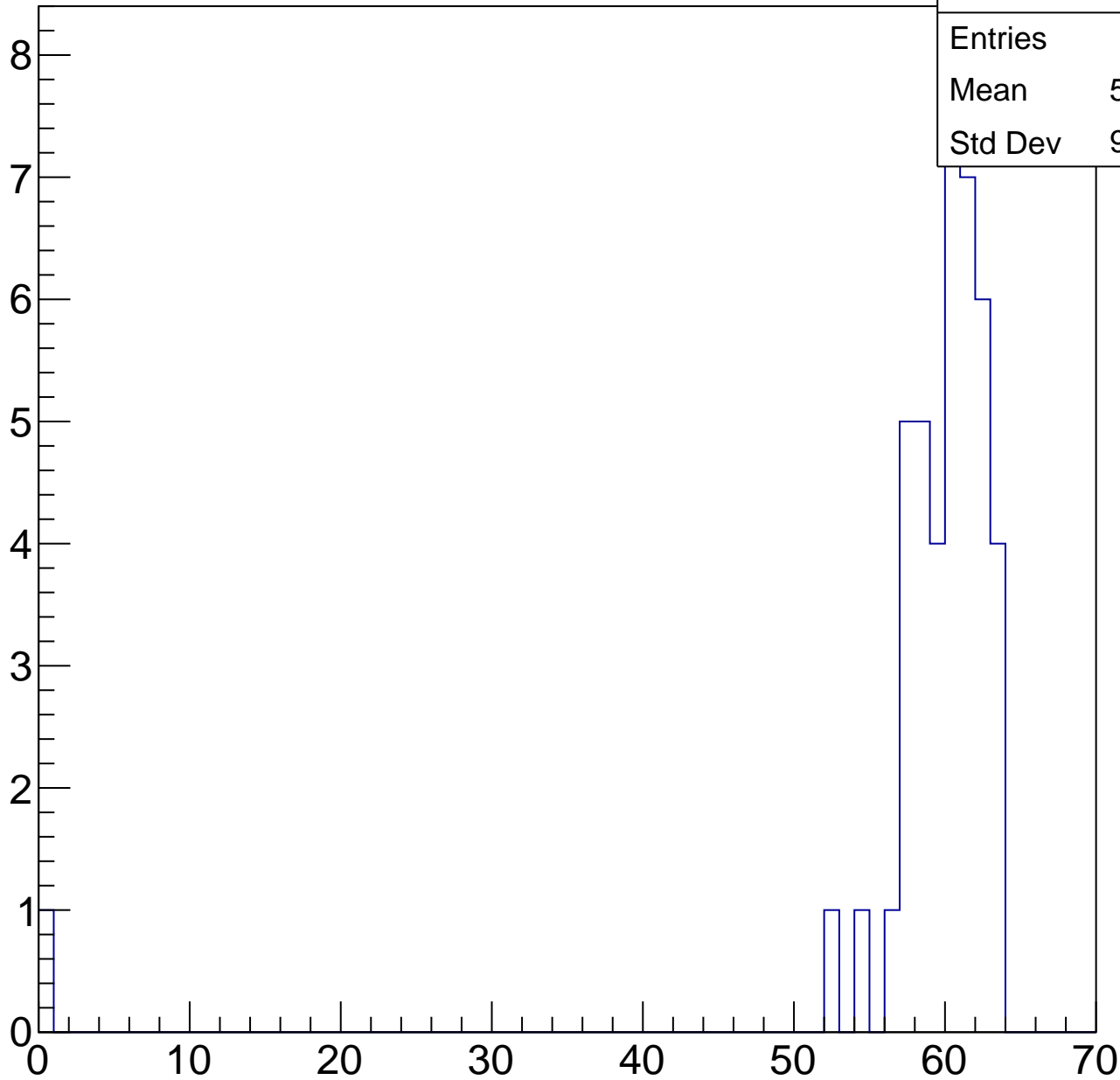
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	43
Mean	58.23
Std Dev	9.298

ampl



# B1L101S, U16-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

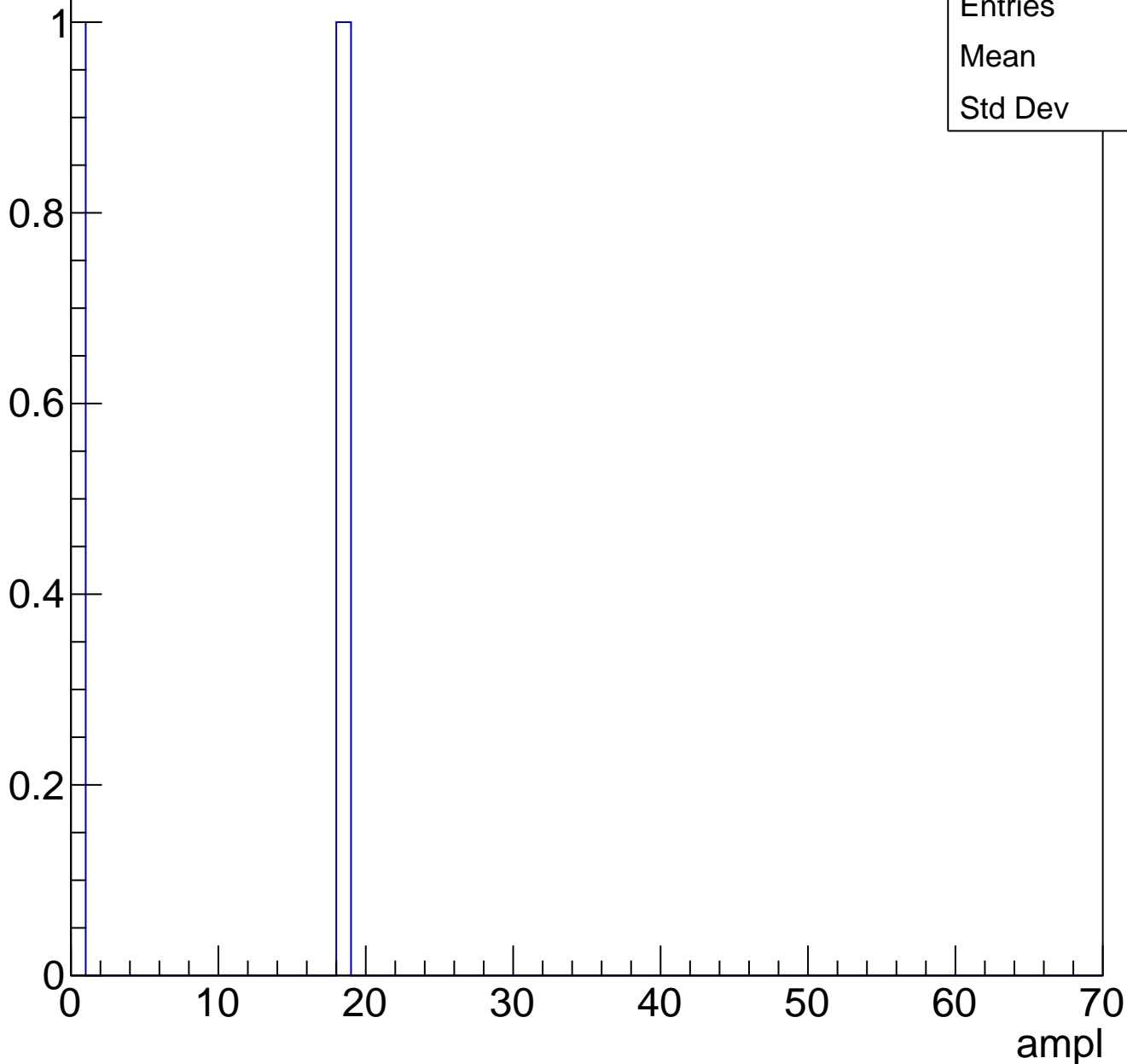




# B1L101S, U16-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch73, adc0

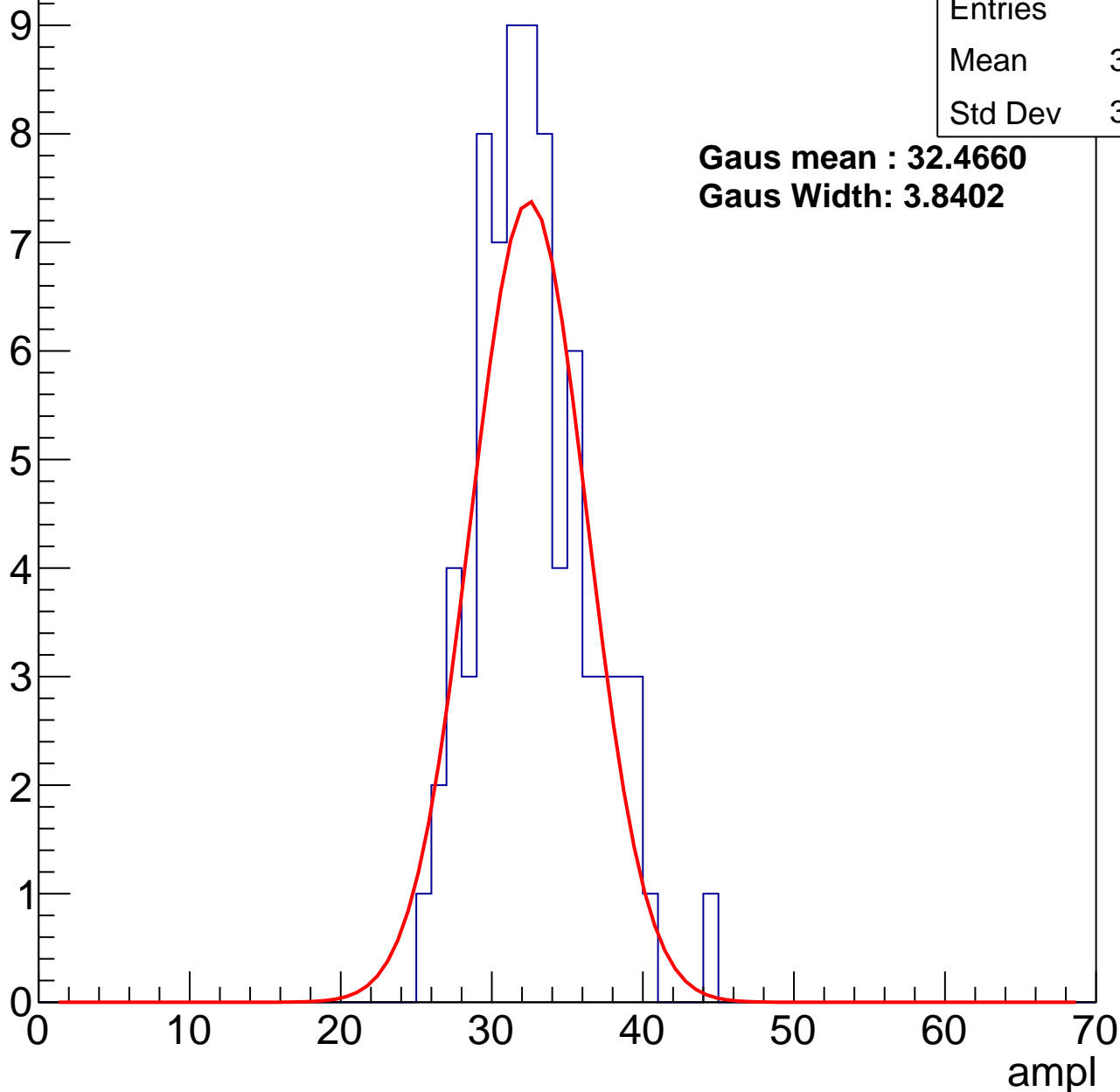
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	32.29
Std Dev	3.716

**Gaus mean : 32.4660**

**Gaus Width: 3.8402**



# B1L101S, U16-ch73, adc1

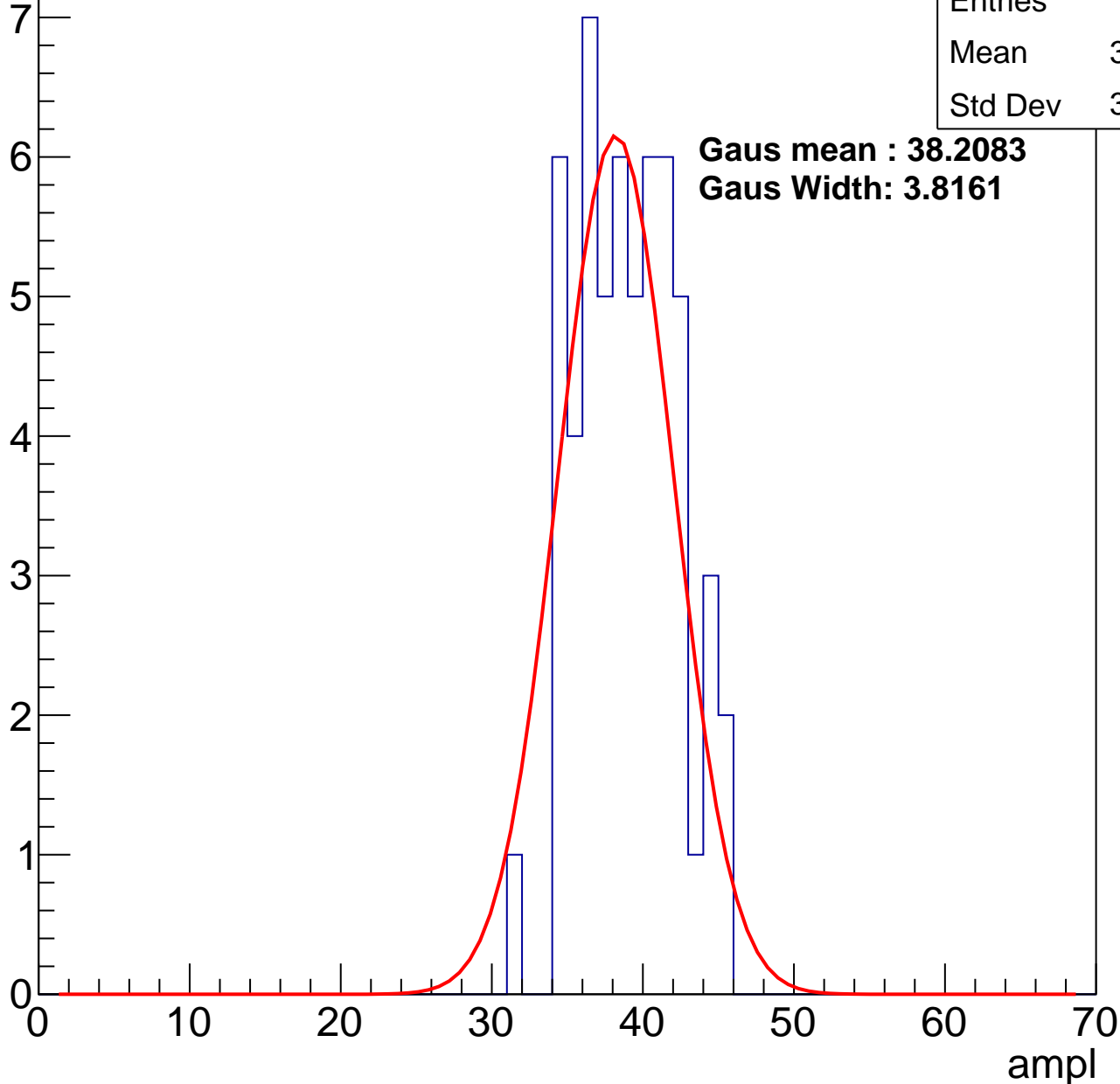
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	38.53
Std Dev	3.223

**Gaus mean : 38.2083**

**Gaus Width: 3.8161**



# B1L101S, U16-ch73, adc2

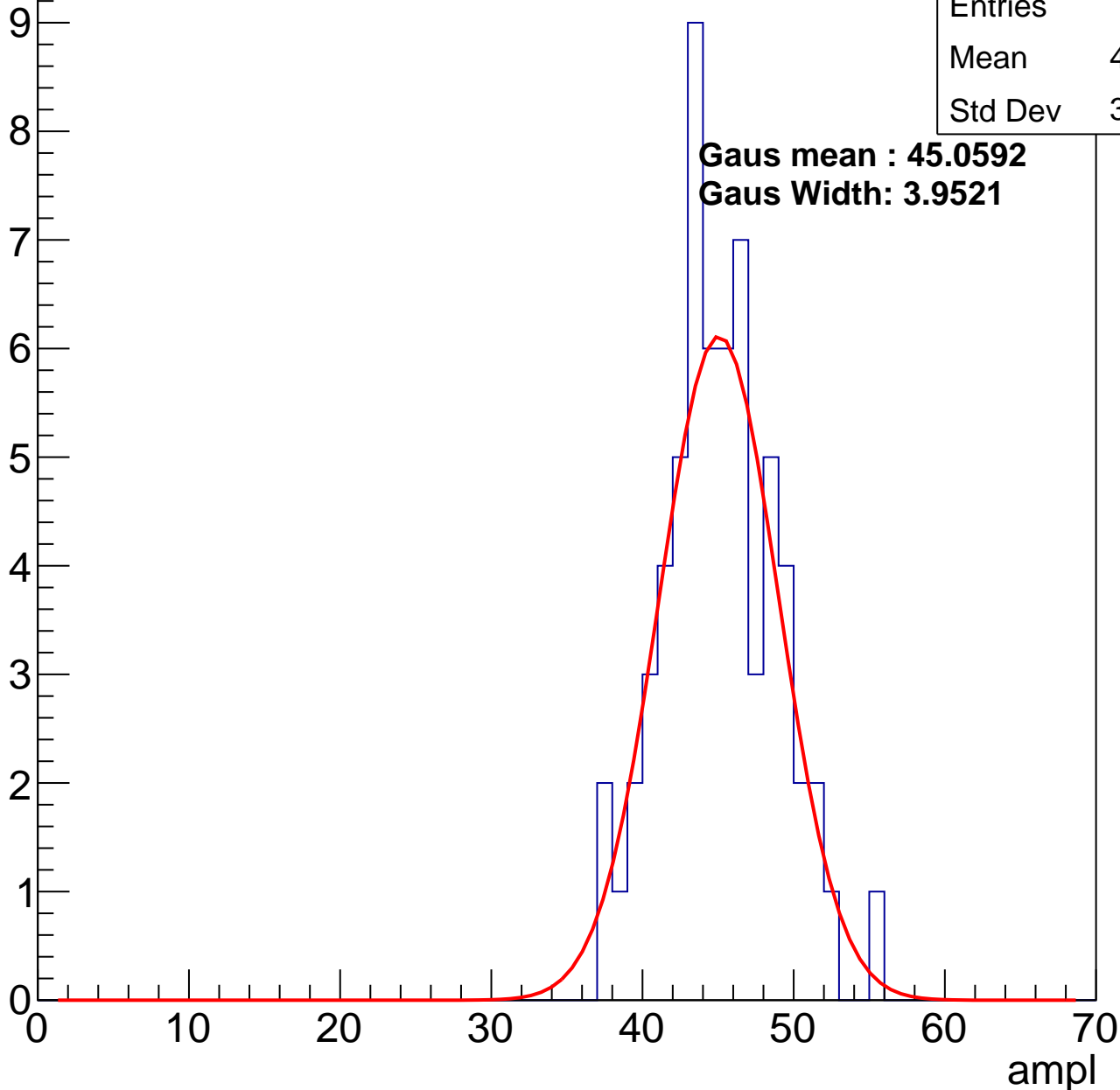
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	44.65
Std Dev	3.708

**Gaus mean : 45.0592**

**Gaus Width: 3.9521**

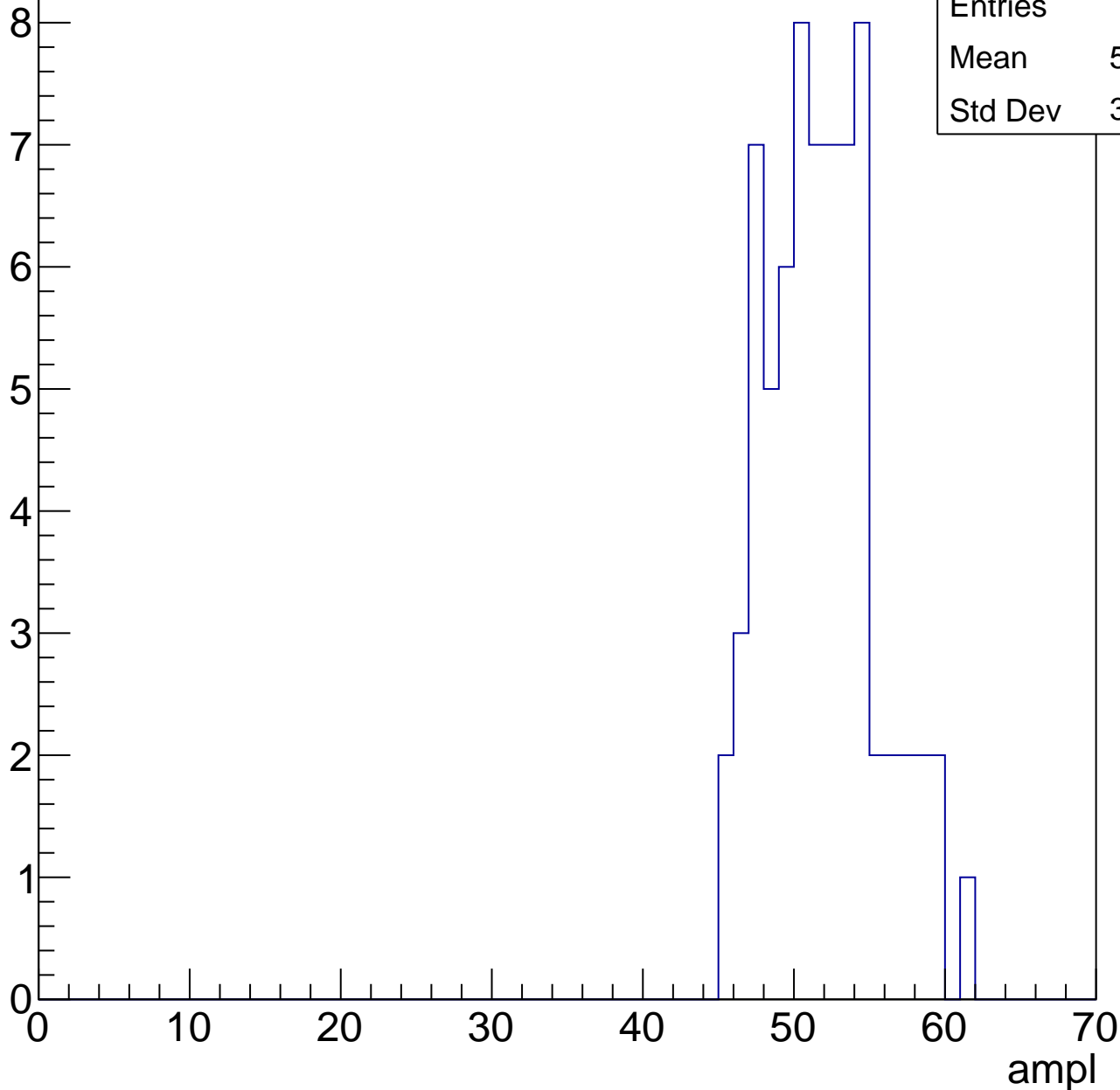


# B1L101S, U16-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	51.35
Std Dev	3.588

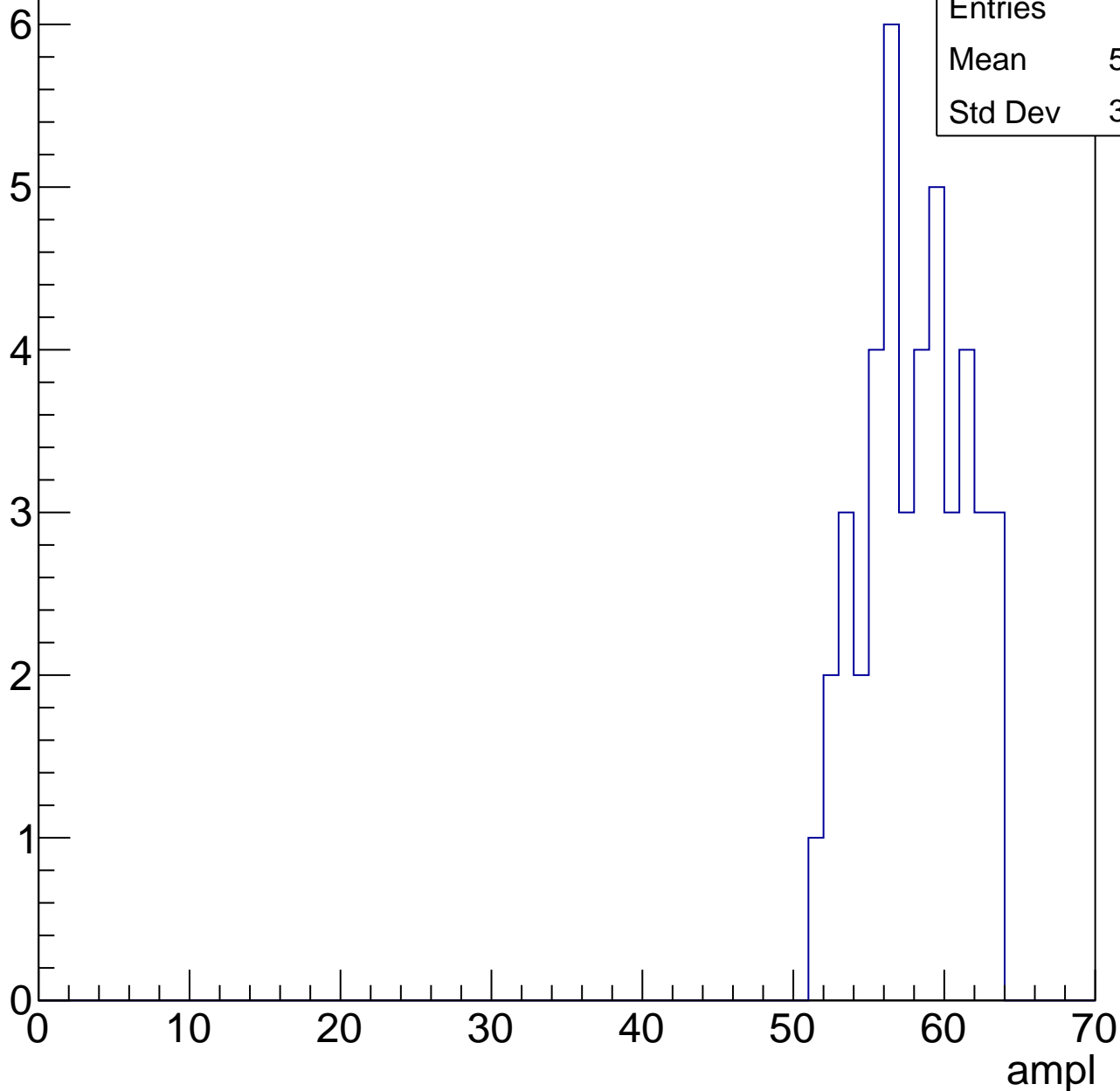


# B1L101S, U16-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

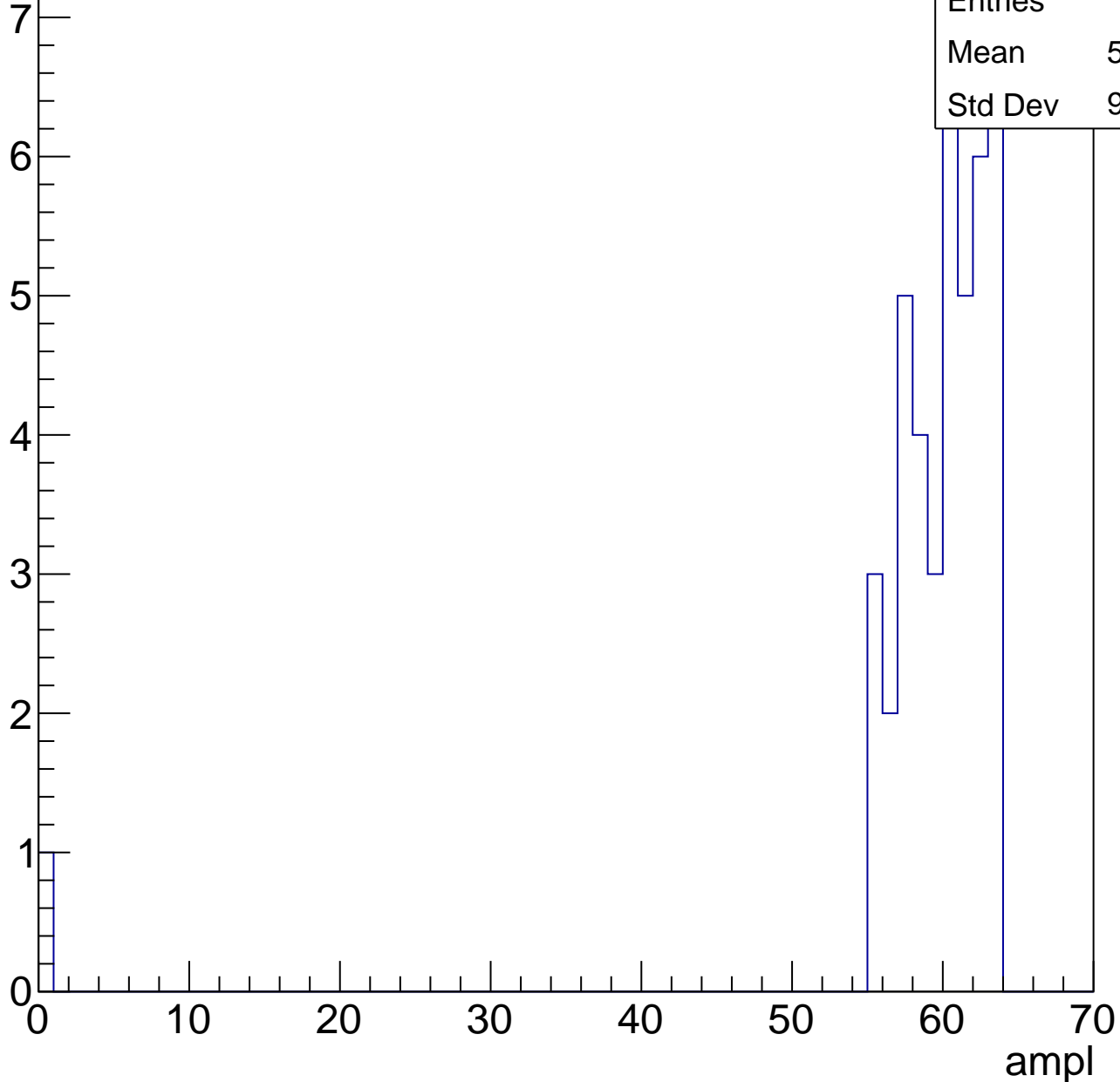
Entries	43
Mean	57.56
Std Dev	3.266



# B1L101S, U16-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch74, adc0

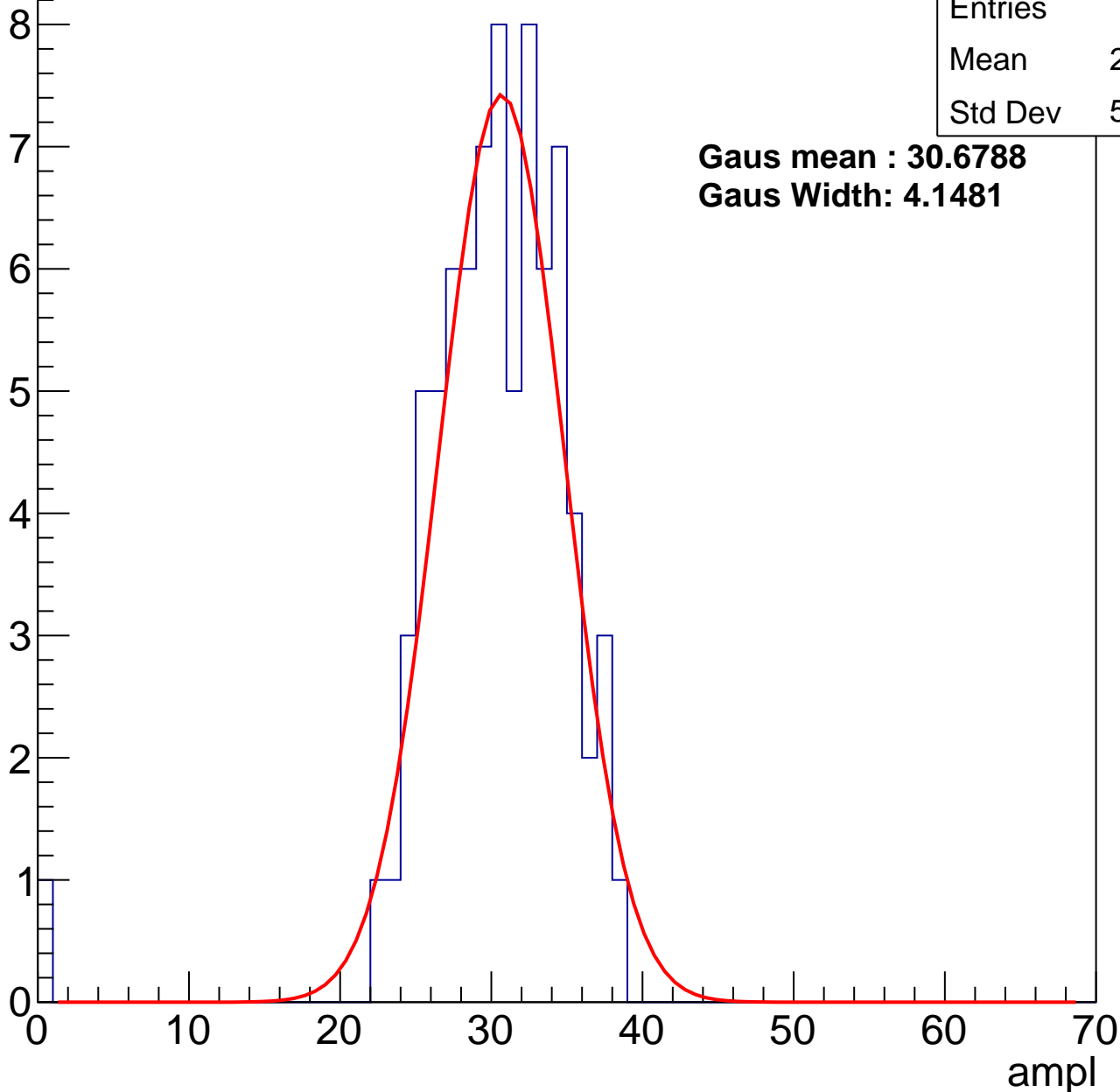
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	29.78
Std Dev	5.023

**Gaus mean : 30.6788**

**Gaus Width: 4.1481**



# B1L101S, U16-ch74, adc1

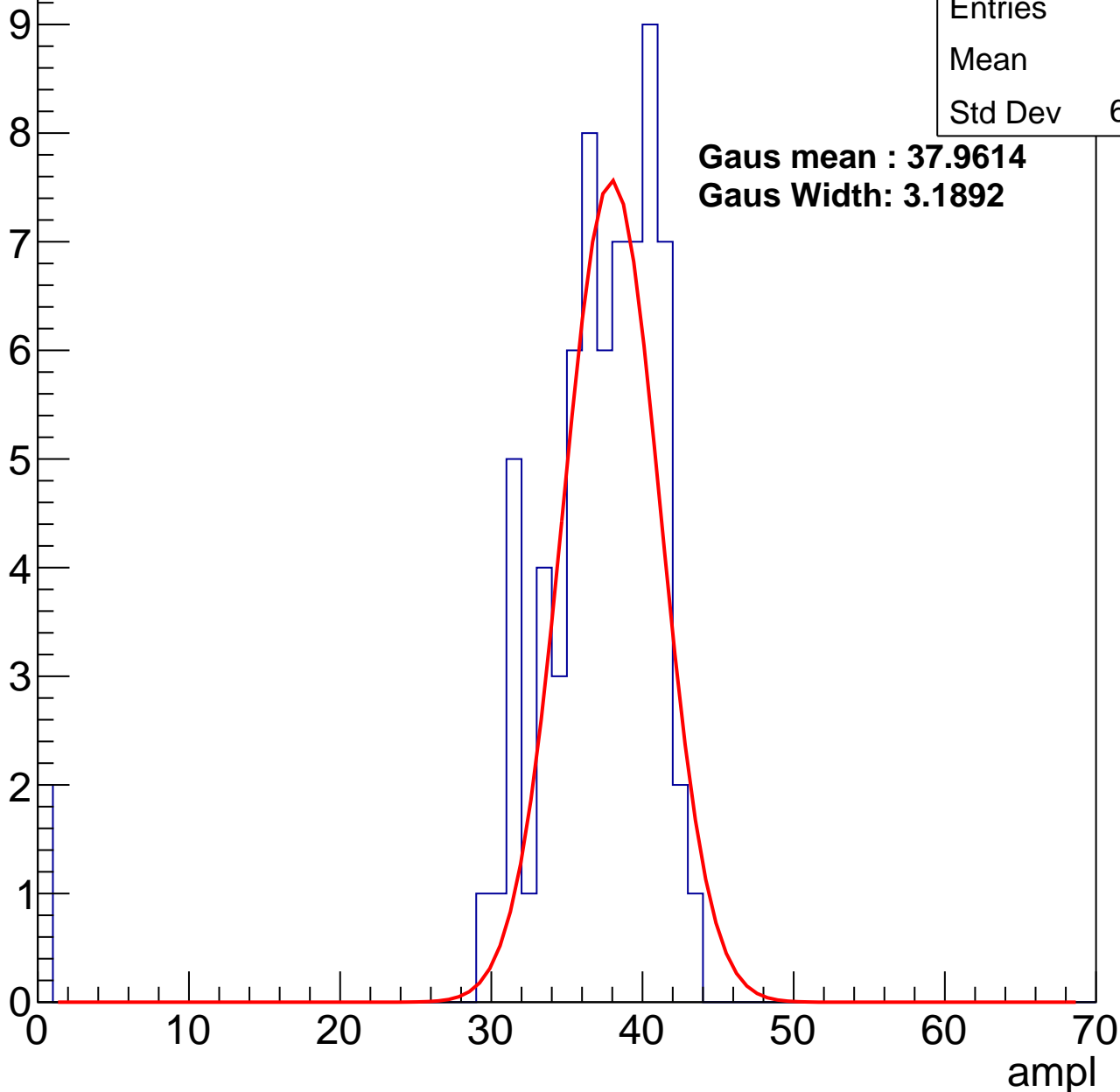
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	35.9
Std Dev	6.978

**Gaus mean : 37.9614**

**Gaus Width: 3.1892**



# B1L101S, U16-ch74, adc2

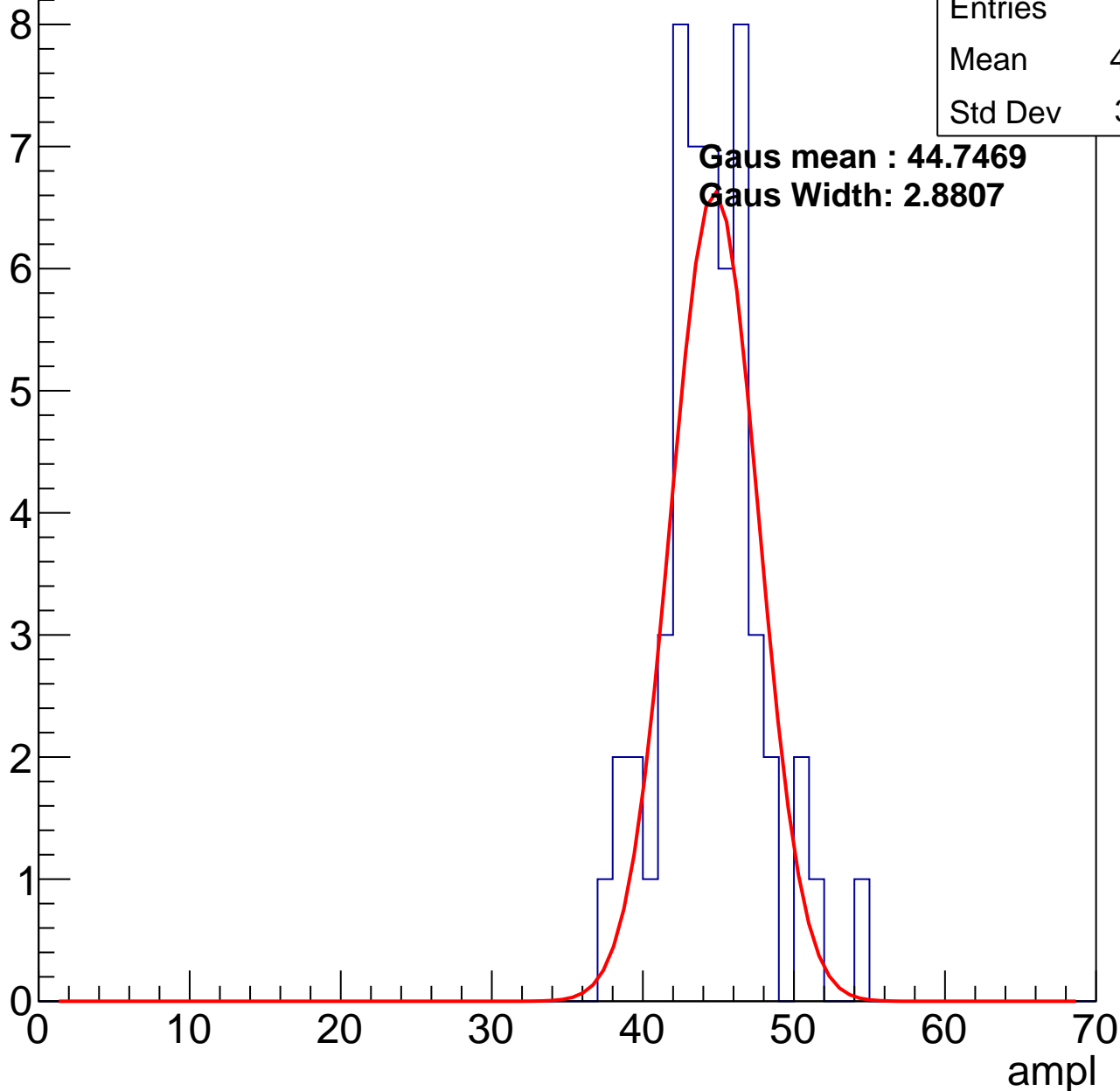
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	44.06
Std Dev	3.251

**Gaus mean : 44.7469**

**Gaus Width: 2.8807**

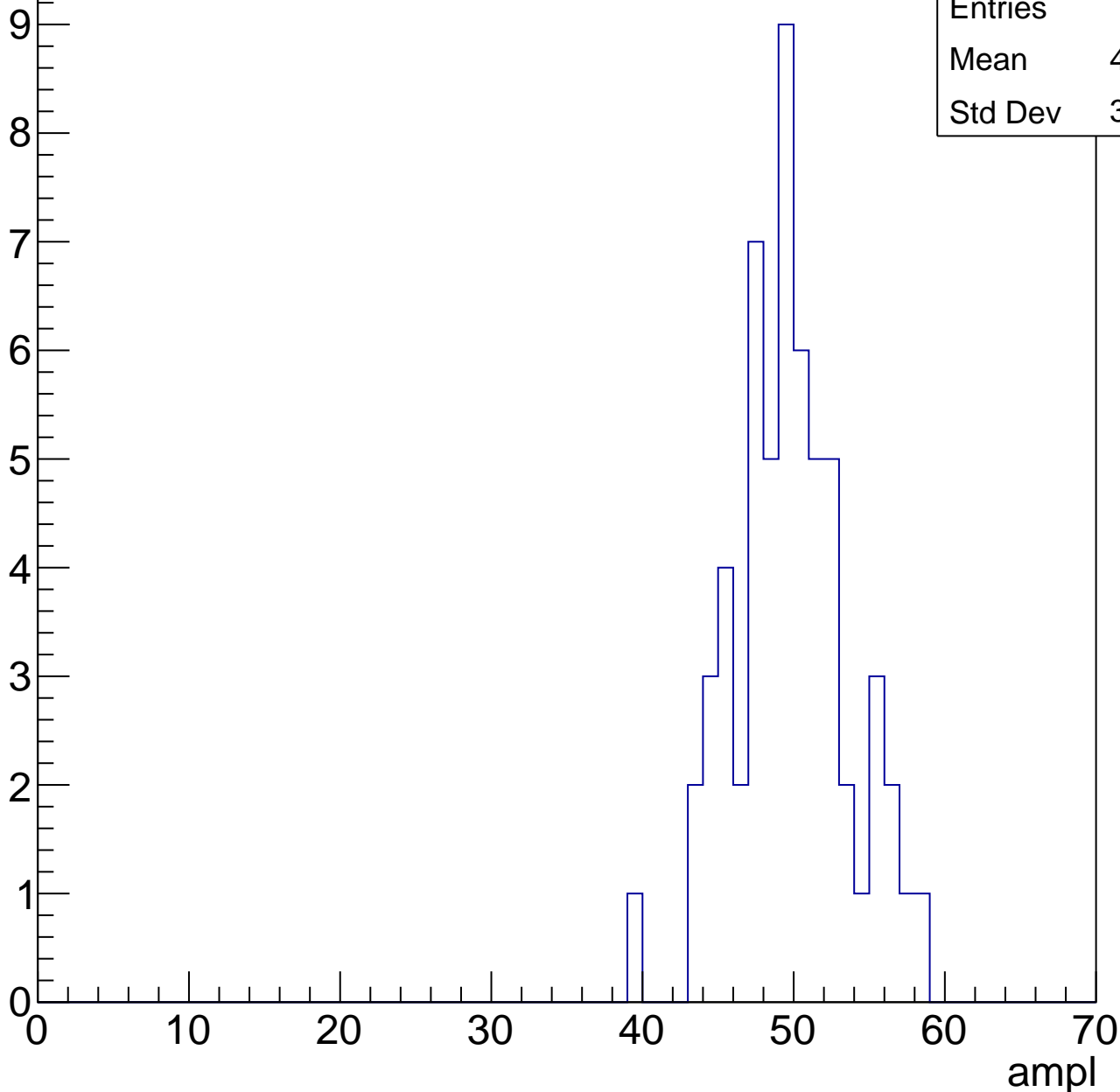


# B1L101S, U16-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	49.25
Std Dev	3.767

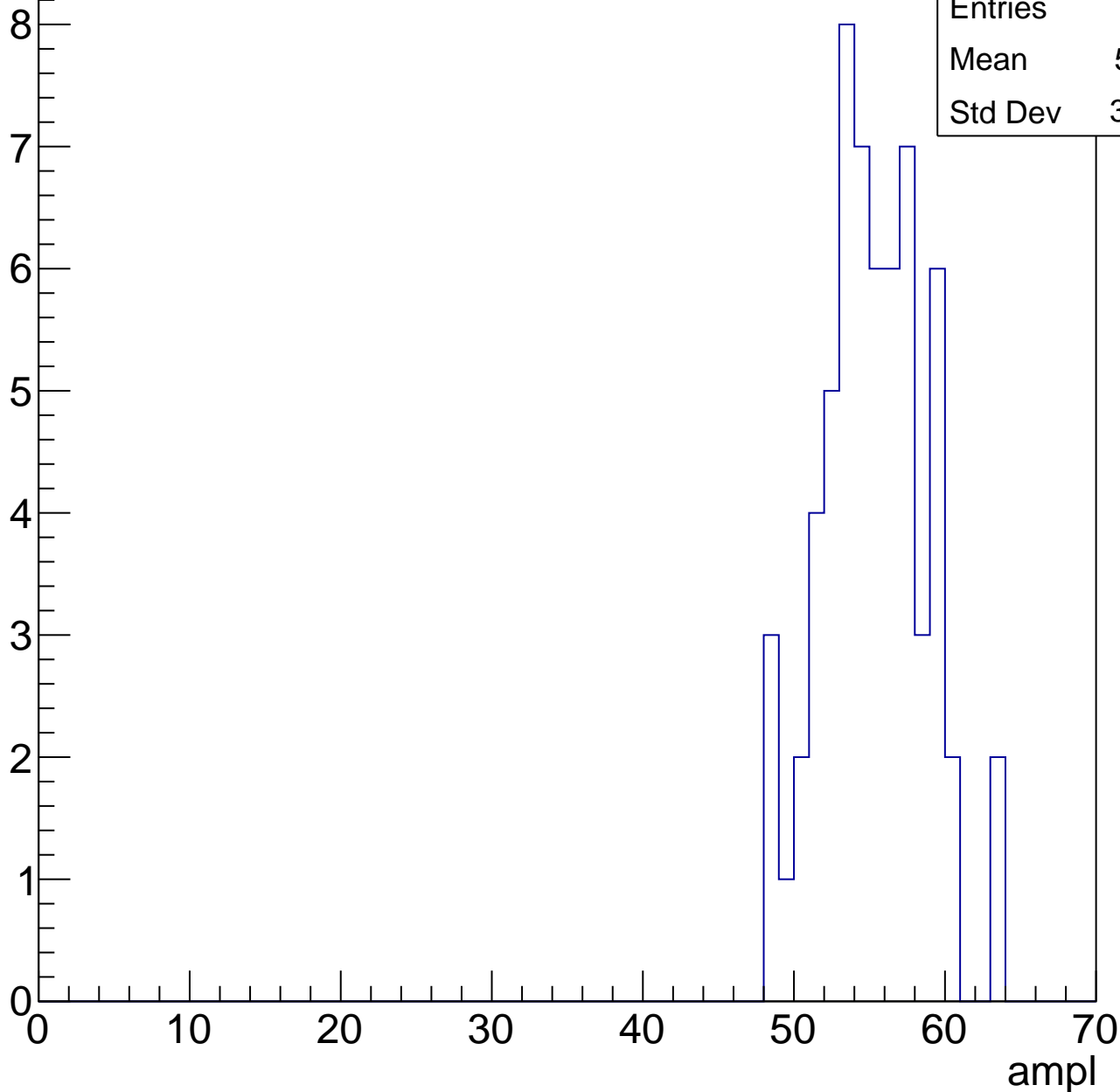


# B1L101S, U16-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	54.81
Std Dev	3.393



# B1L101S, U16-ch74, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

Entries

45

Mean

58.8

Std Dev

9.147

Entries	45
Mean	58.8
Std Dev	9.147

# B1L101S, U16-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	8
Mean	60.88
Std Dev	1.763

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U16-ch75, adc0

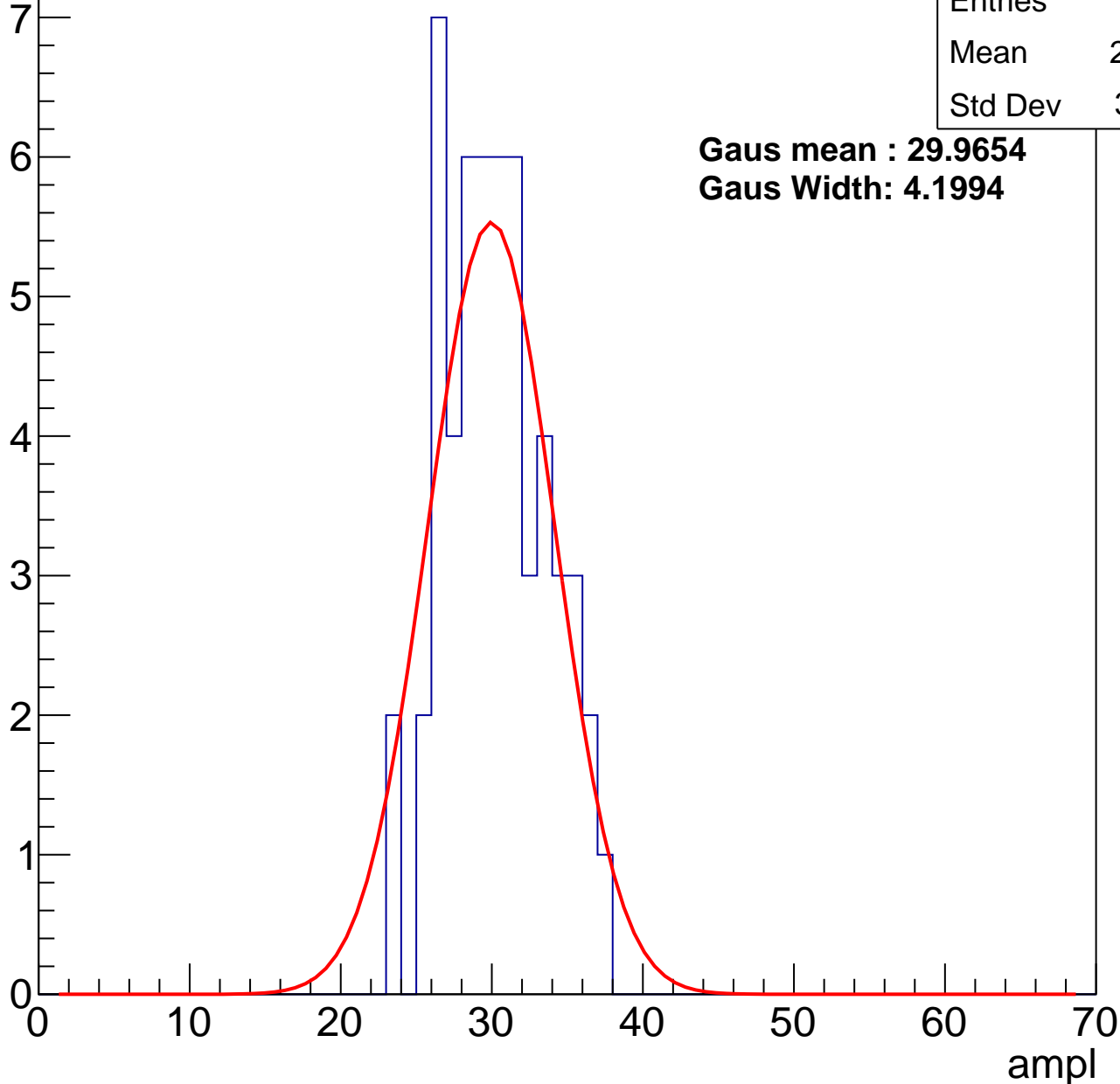
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	29.78
Std Dev	3.361

**Gaus mean : 29.9654**

**Gaus Width: 4.1994**



# B1L101S, U16-ch75, adc1

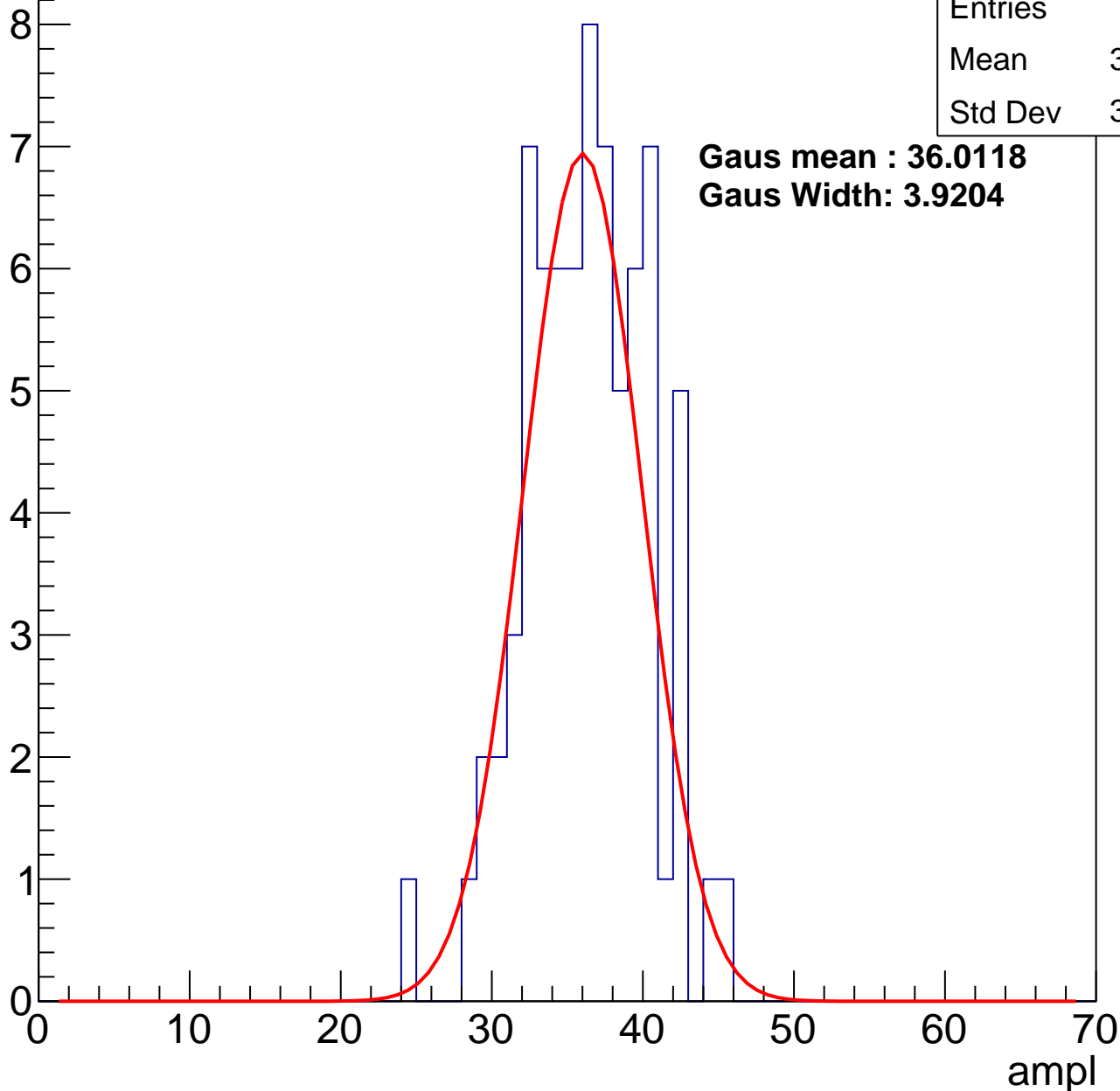
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	35.87
Std Dev	3.984

**Gaus mean : 36.0118**

**Gaus Width: 3.9204**



# B1L101S, U16-ch75, adc2

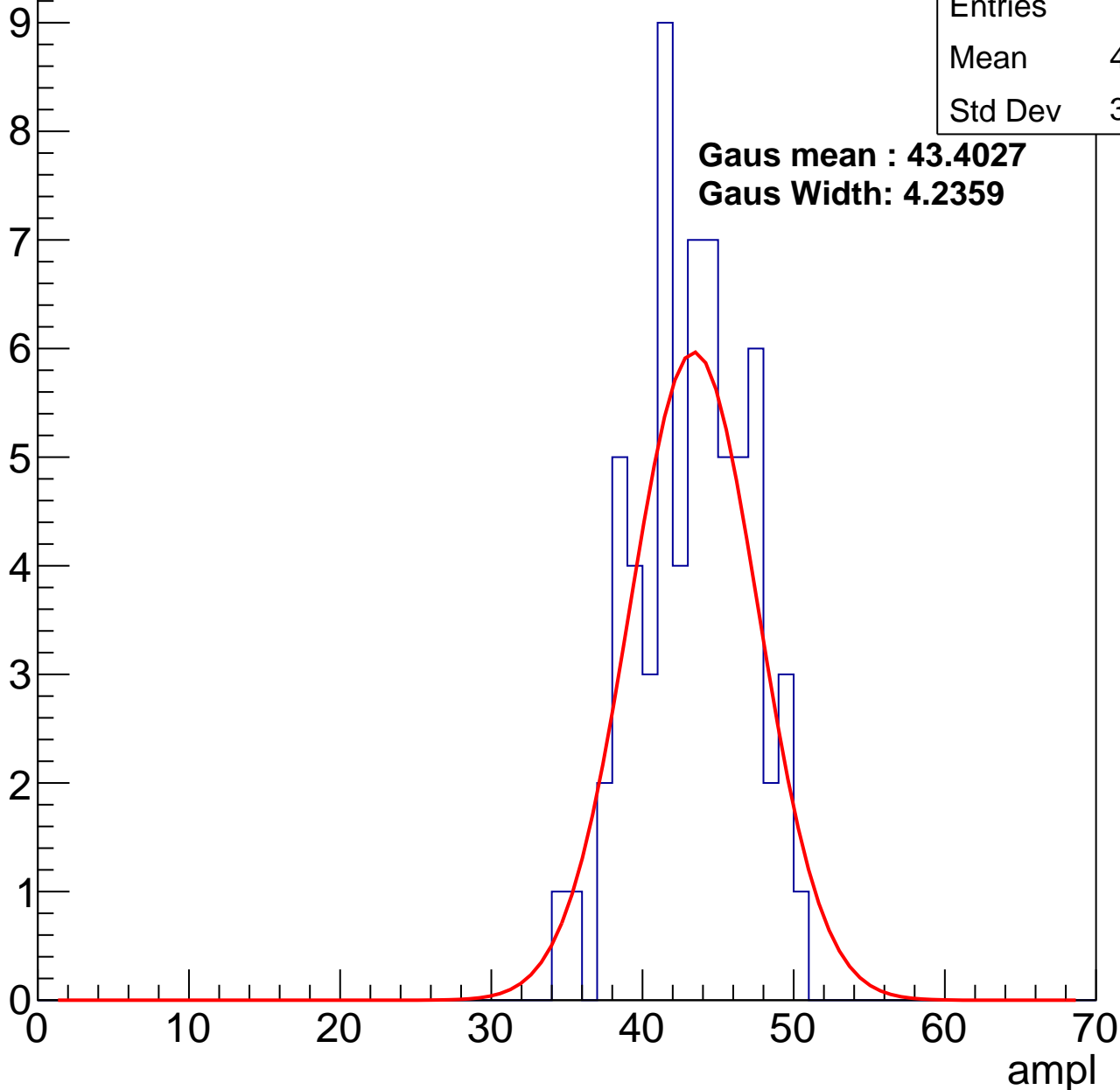
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	42.85
Std Dev	3.609

**Gaus mean : 43.4027**

**Gaus Width: 4.2359**

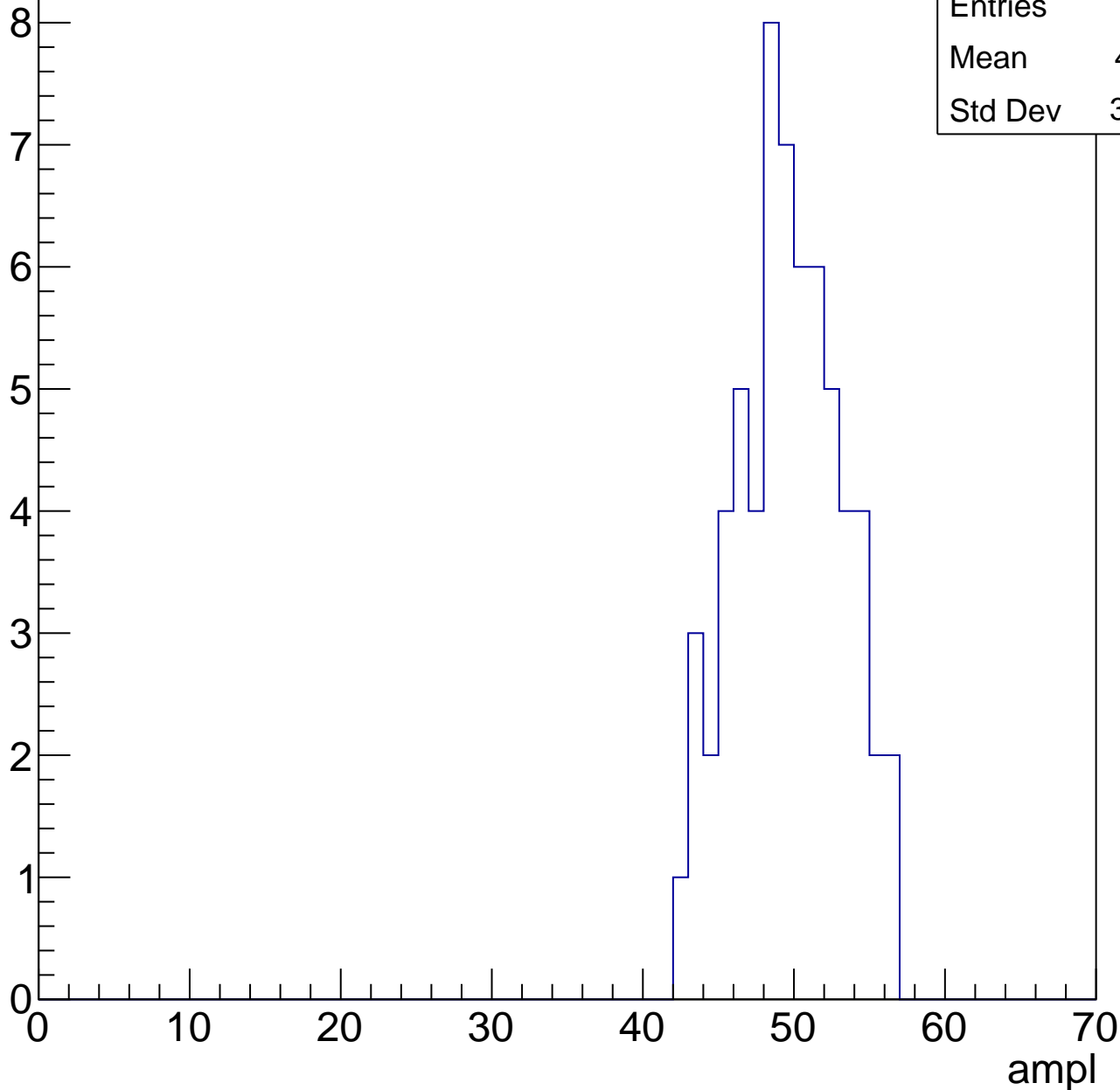


# B1L101S, U16-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	49.21
Std Dev	3.442

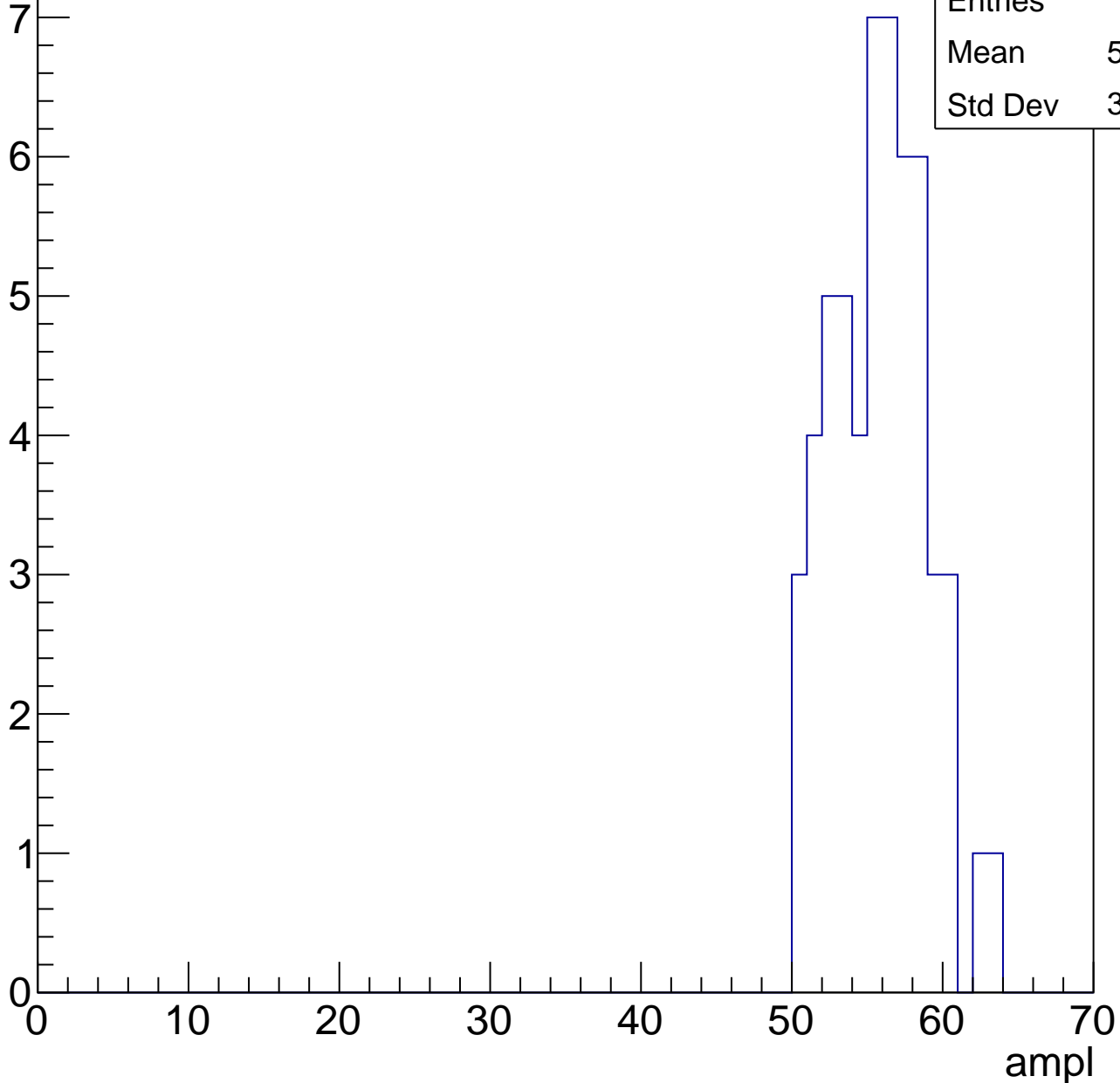


# B1L101S, U16-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	55.35
Std Dev	3.082



# B1L101S, U16-ch75, adc5

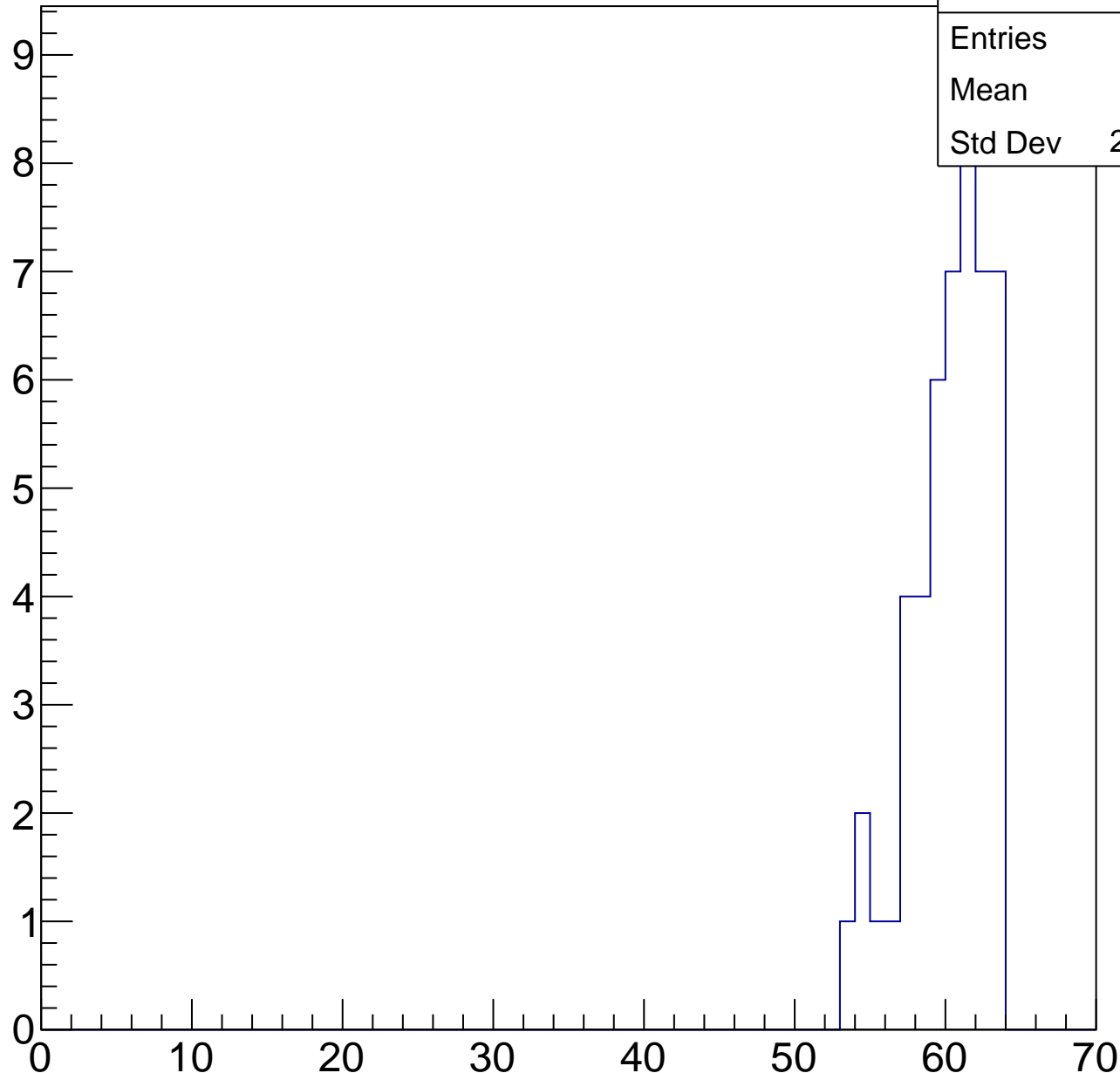
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	59.8
Std Dev	2.547

ampl



# B1L101S, U16-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	52.86
Std Dev	21.62

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U16-ch76, adc0

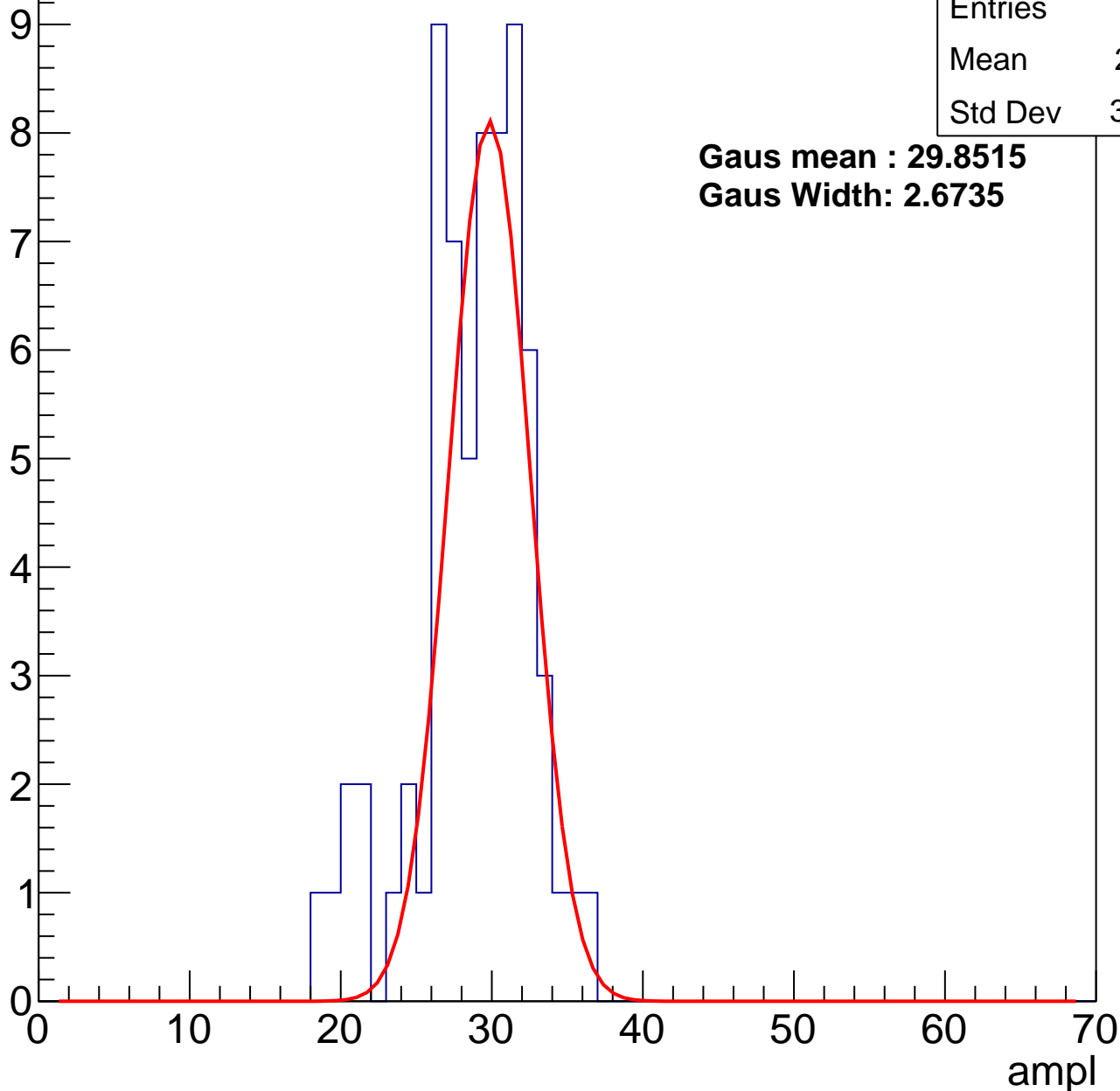
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	28.31
Std Dev	3.739

**Gaus mean : 29.8515**

**Gaus Width: 2.6735**



# B1L101S, U16-ch76, adc1

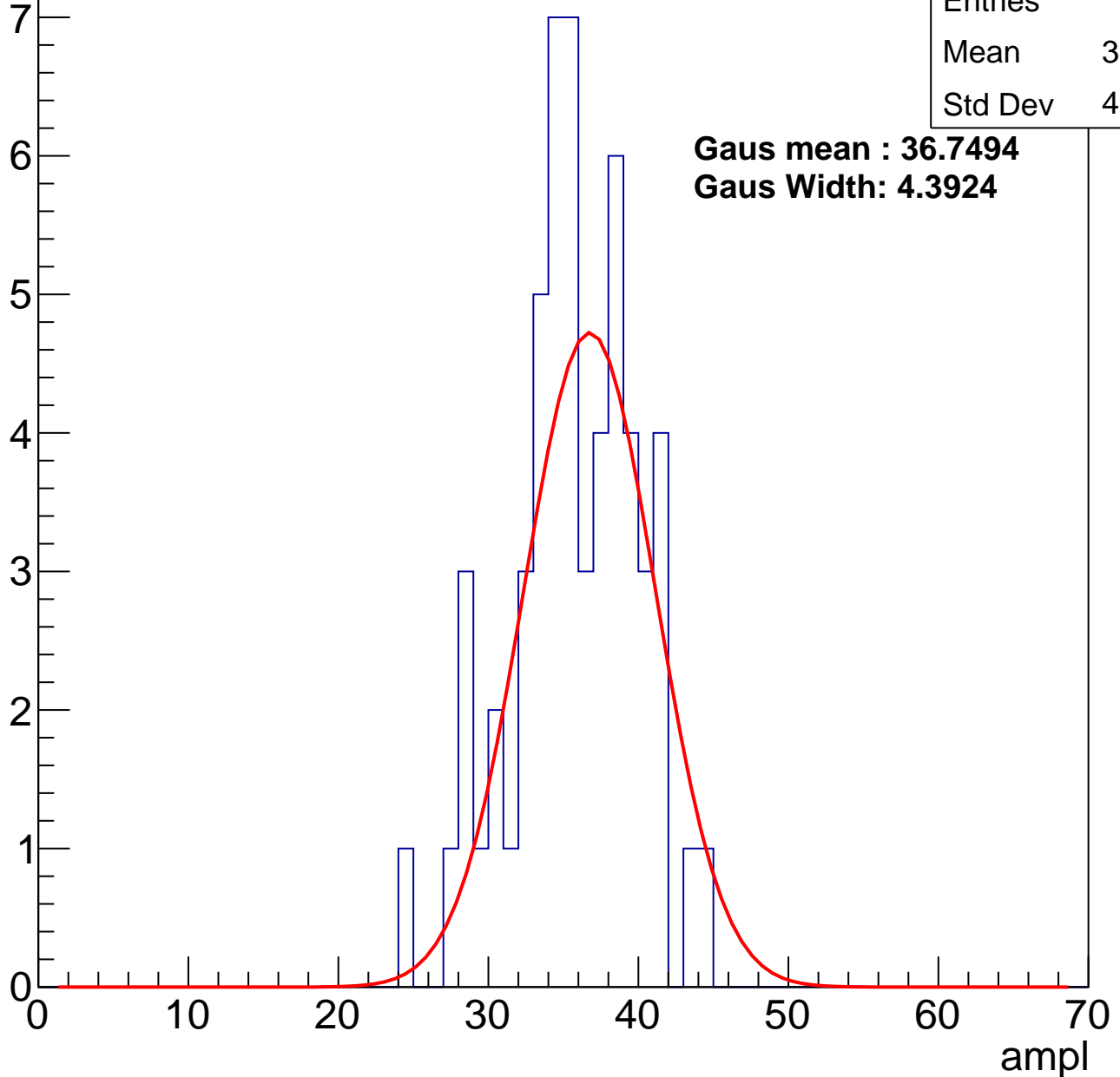
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	35.26
Std Dev	4.157

**Gaus mean : 36.7494**

**Gaus Width: 4.3924**



# B1L101S, U16-ch76, adc2

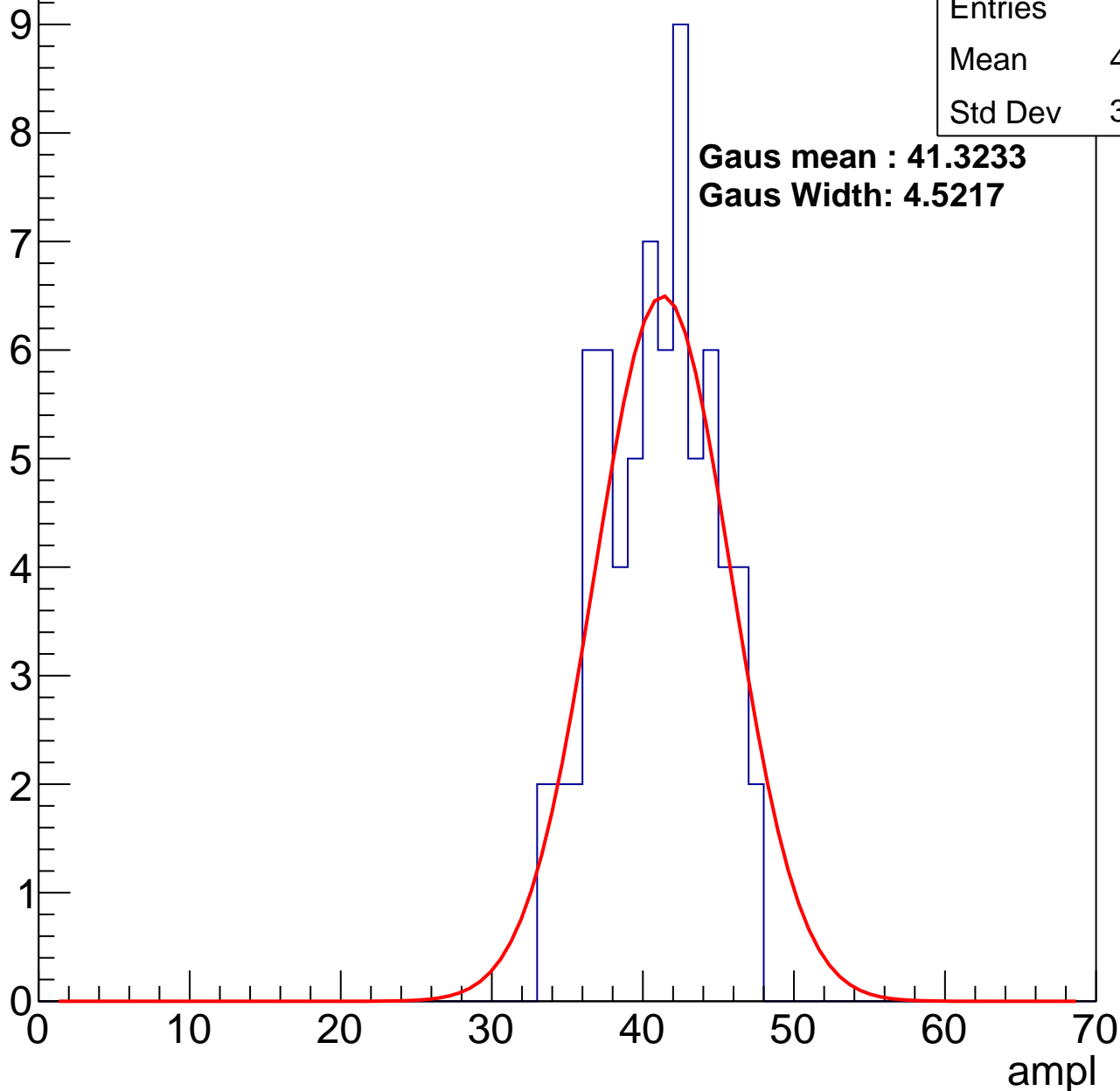
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	40.43
Std Dev	3.592

**Gaus mean : 41.3233**

**Gaus Width: 4.5217**

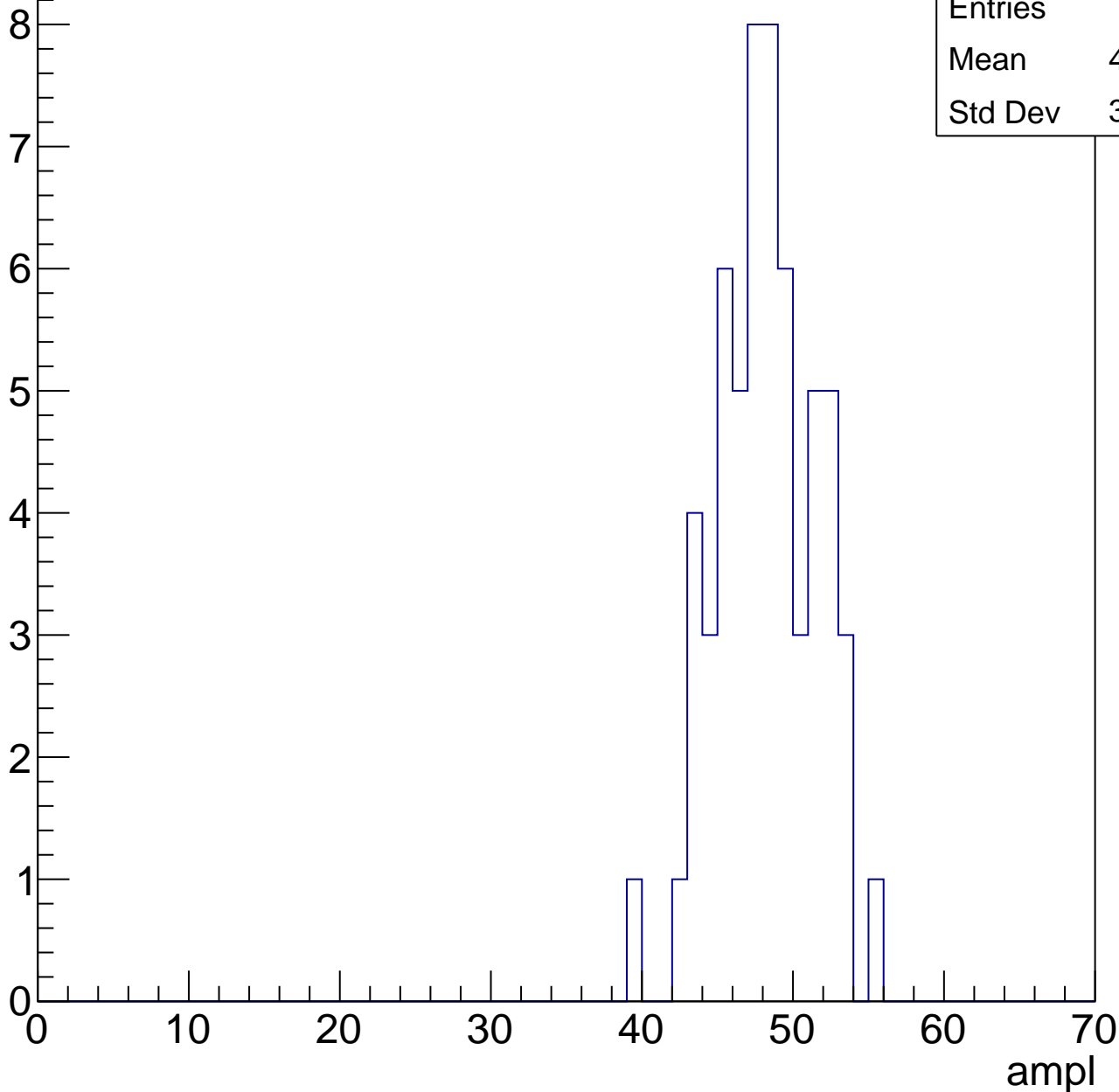


# B1L101S, U16-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	47.76
Std Dev	3.217

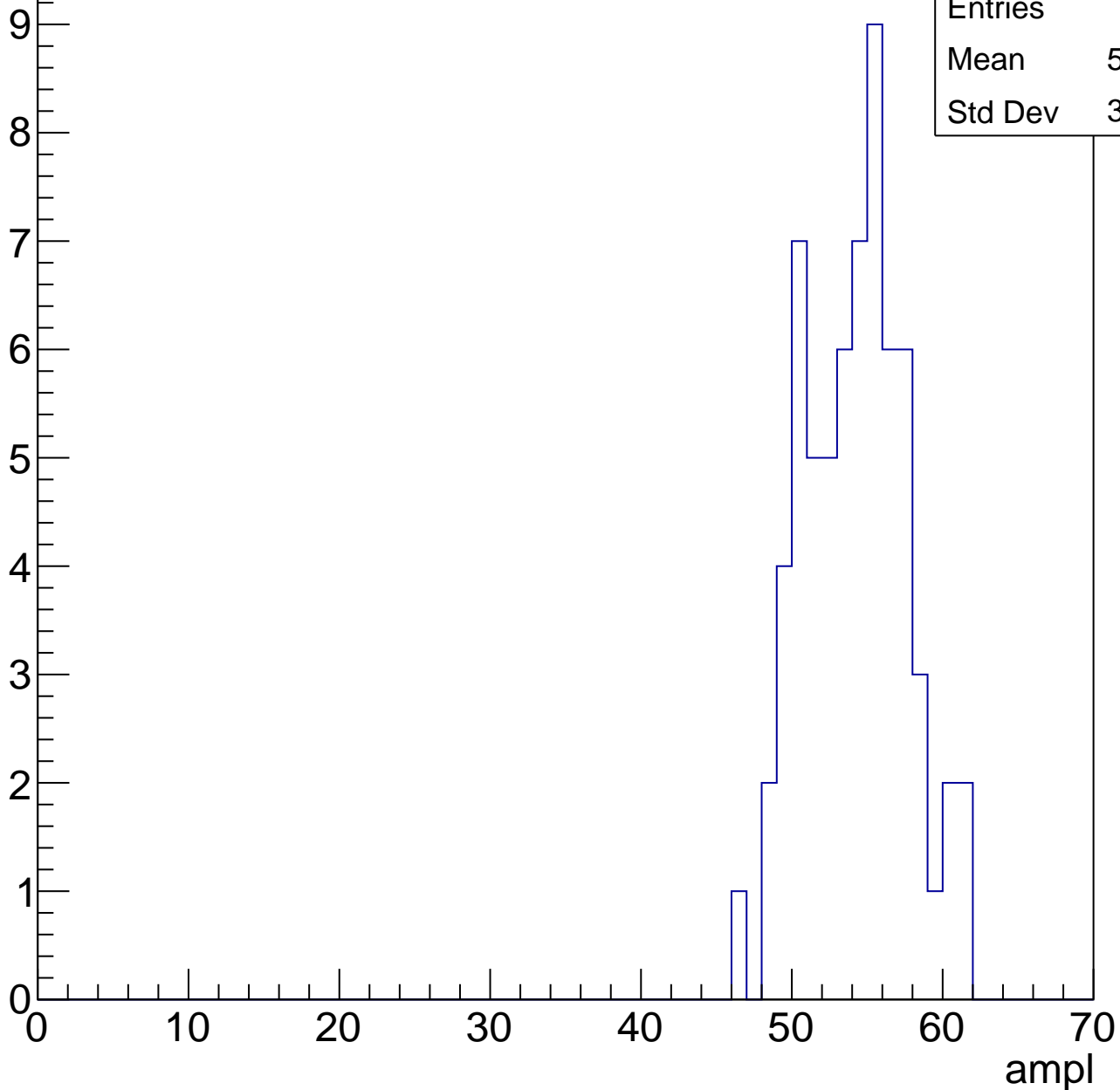


# B1L101S, U16-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	53.74
Std Dev	3.359

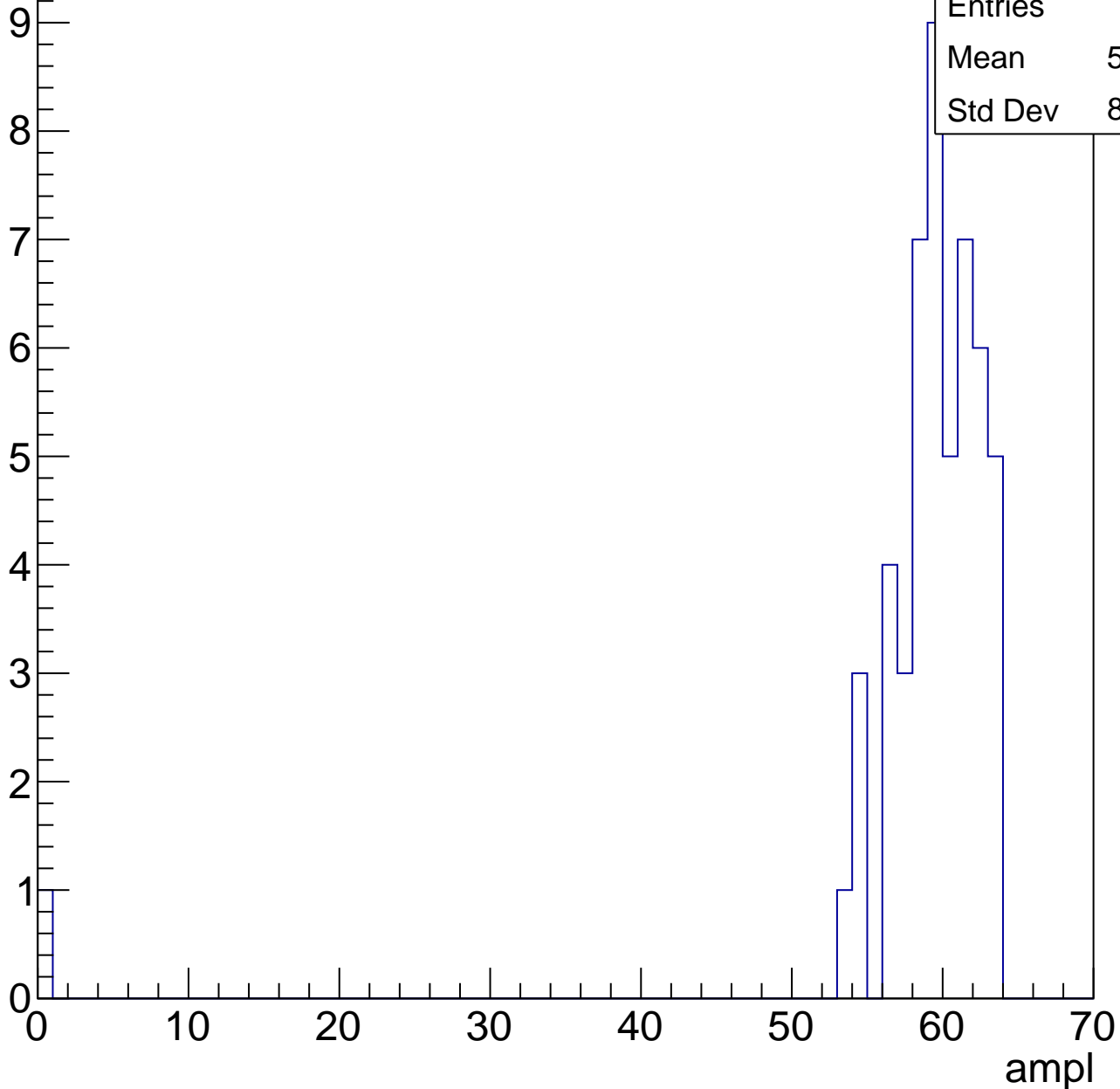


# B1L101S, U16-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	58.06
Std Dev	8.596

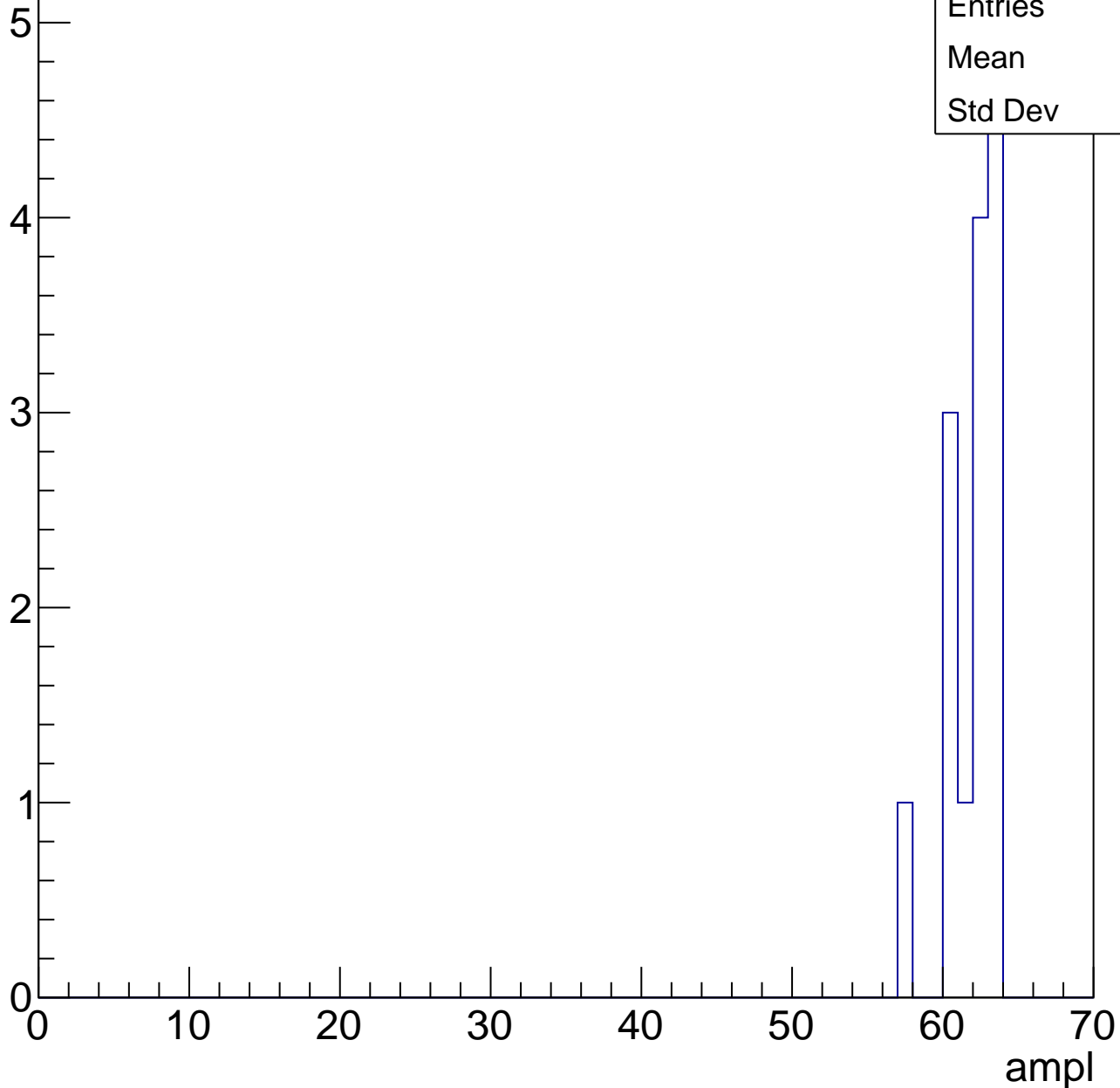


# B1L101S, U16-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	14
Mean	61.5
Std Dev	1.68





# B1L101S, U16-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch77, adc0

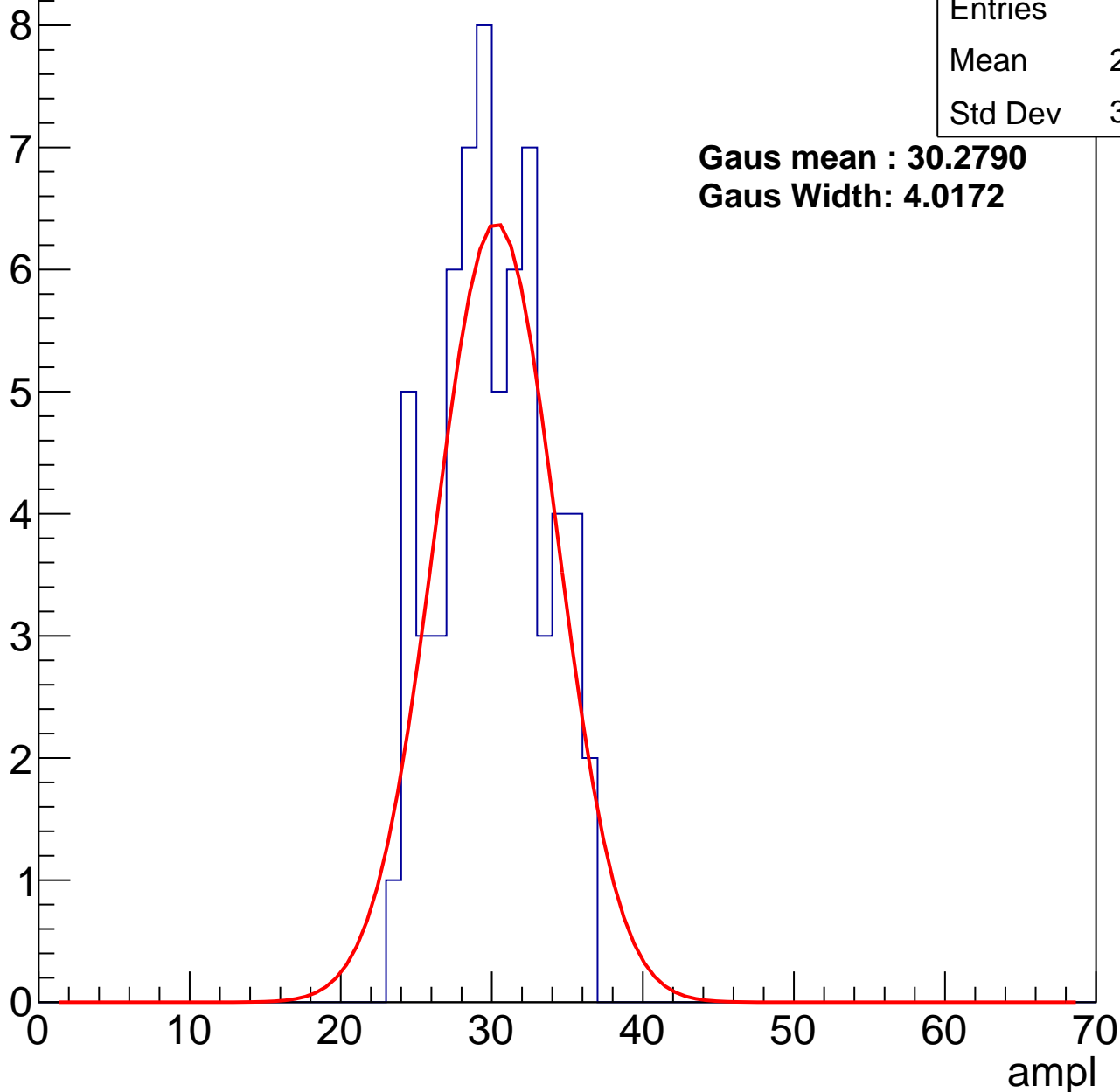
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	29.58
Std Dev	3.372

**Gaus mean : 30.2790**

**Gaus Width: 4.0172**



# B1L101S, U16-ch77, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	78
Mean	36.87
Std Dev	3.804

**Gaus mean : 37.2283**

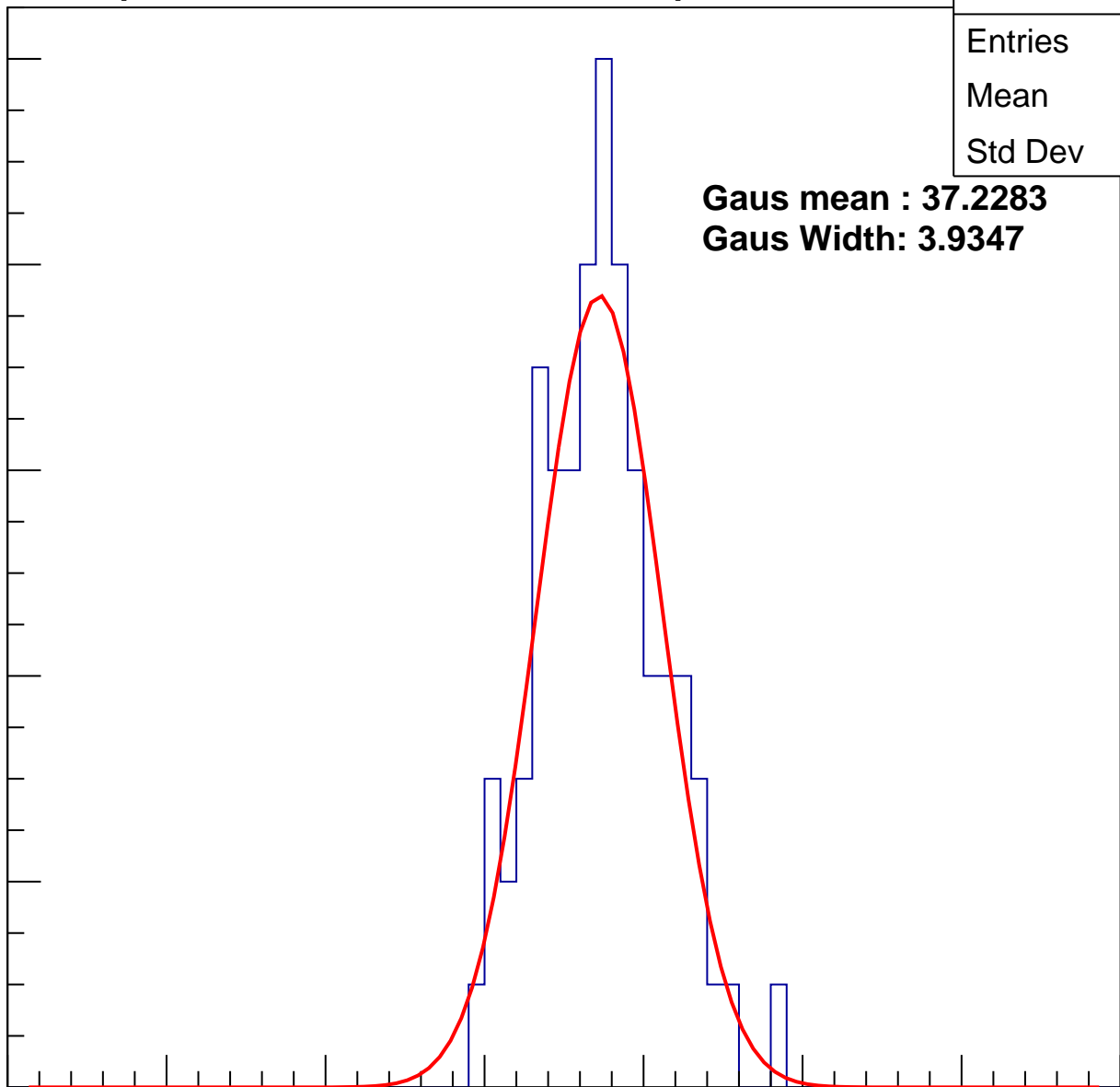
**Gaus Width: 3.9347**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch77, adc2

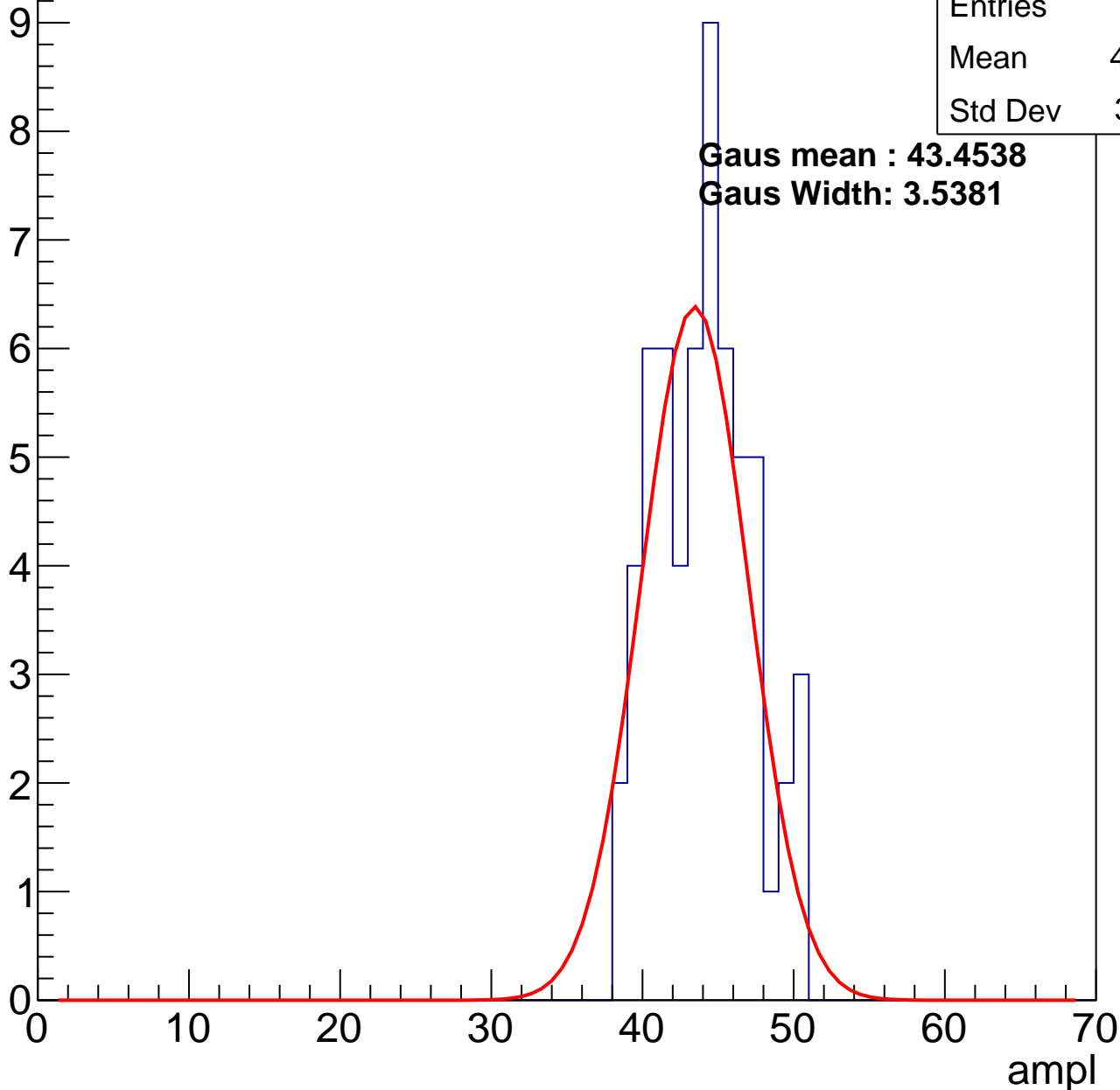
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	43.58
Std Dev	3.131

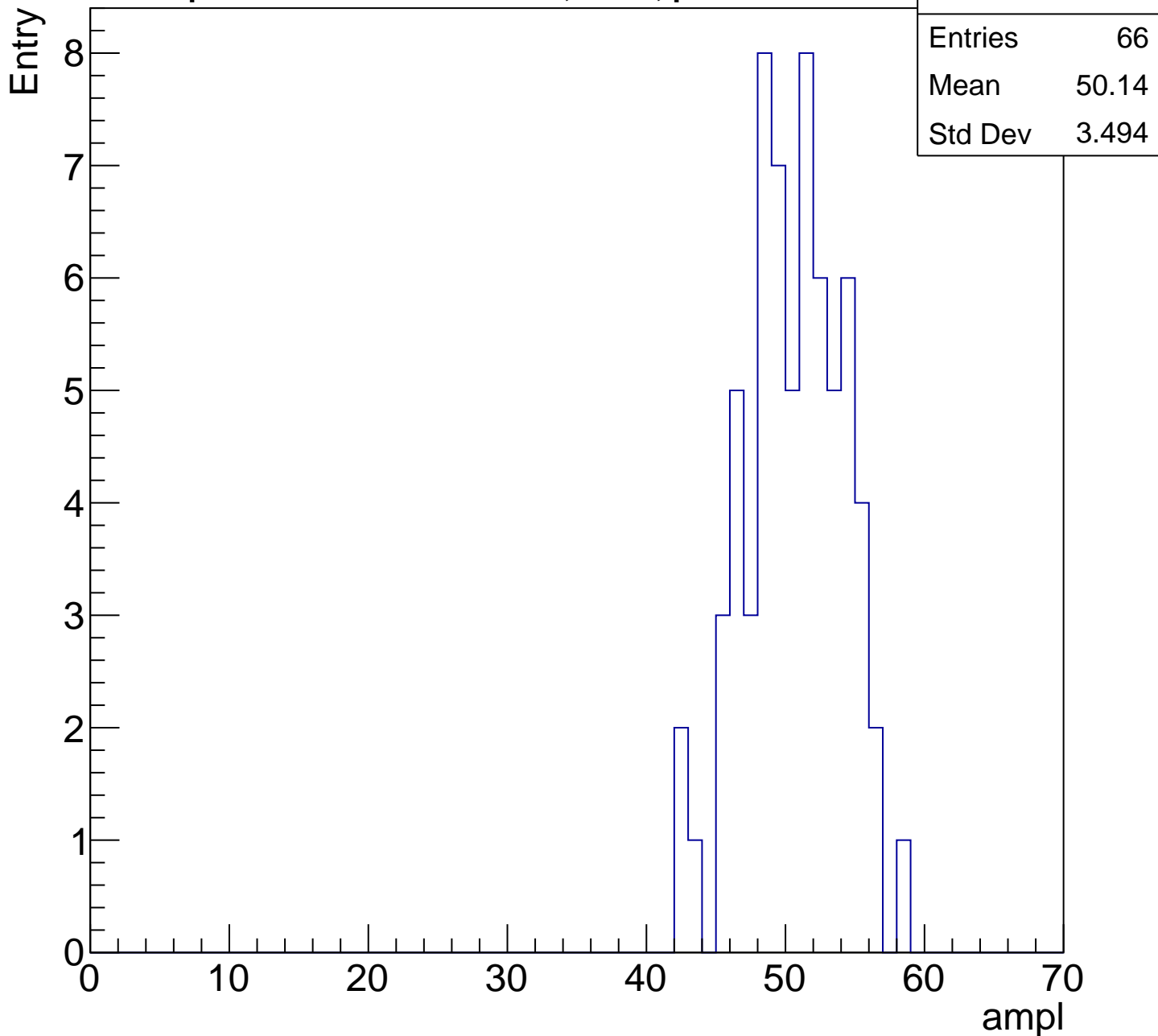
**Gaus mean : 43.4538**

**Gaus Width: 3.5381**



# B1L101S, U16-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

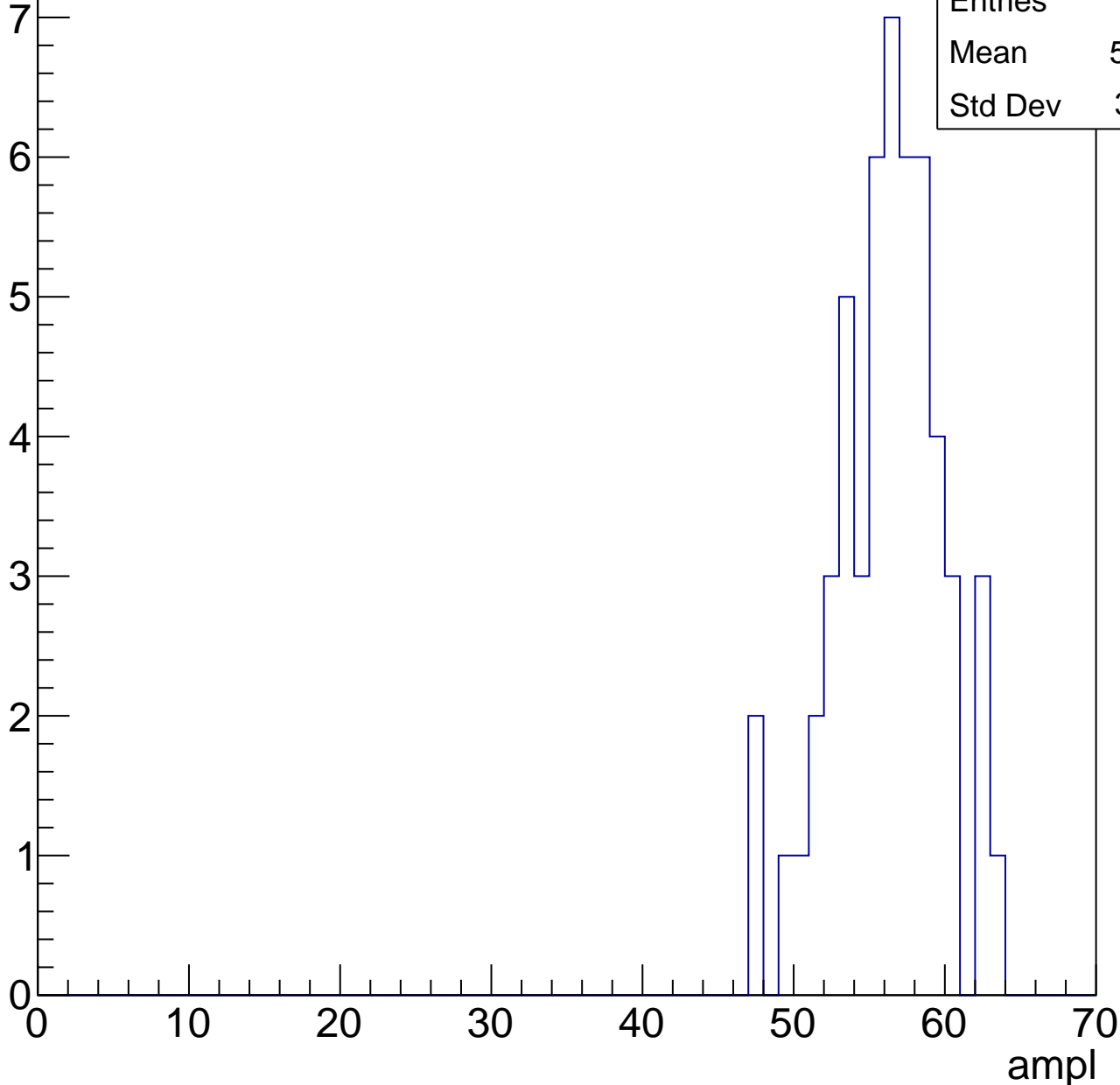


# B1L101S, U16-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	55.75
Std Dev	3.571

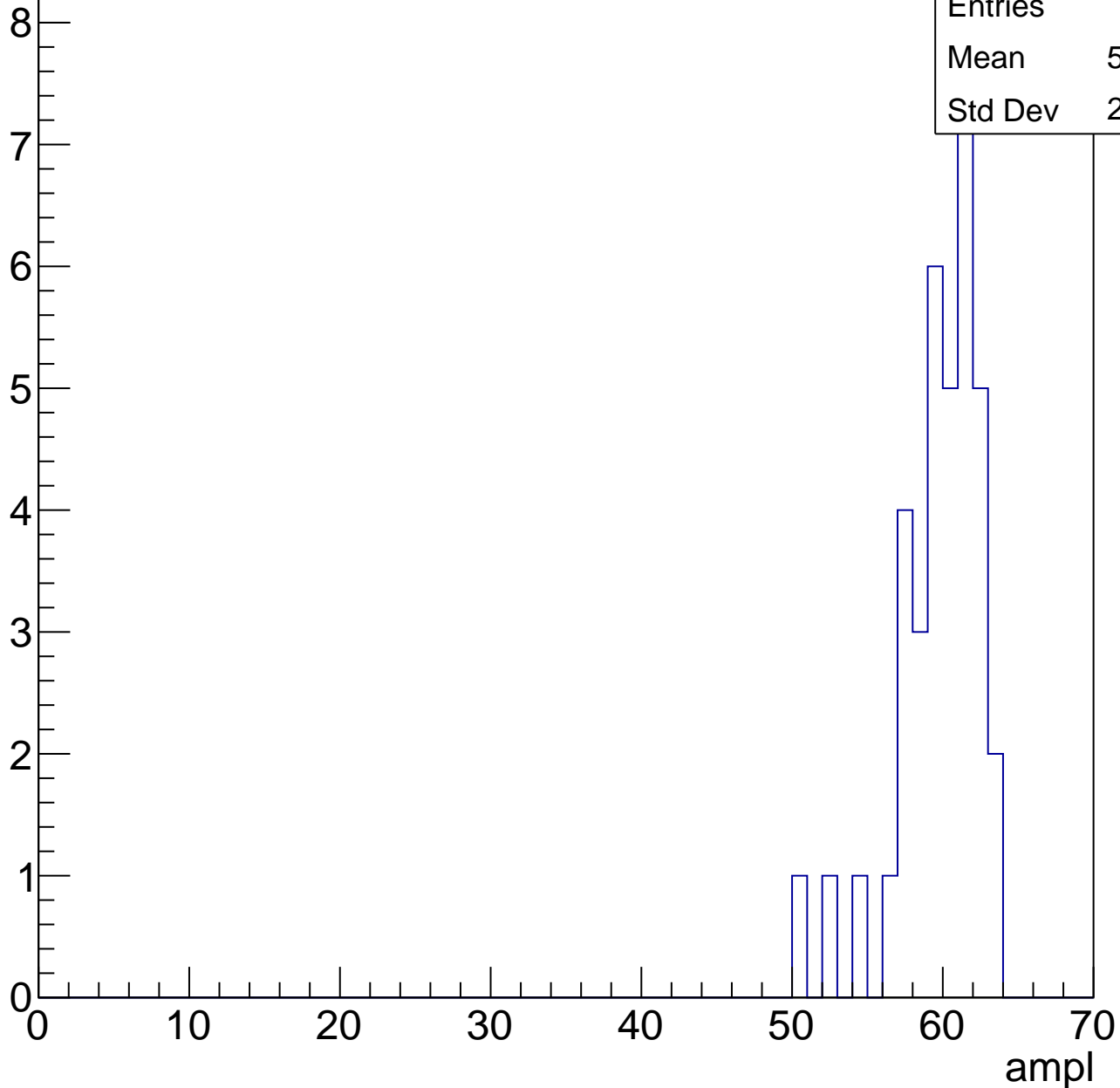


# B1L101S, U16-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	37
Mean	59.24
Std Dev	2.823

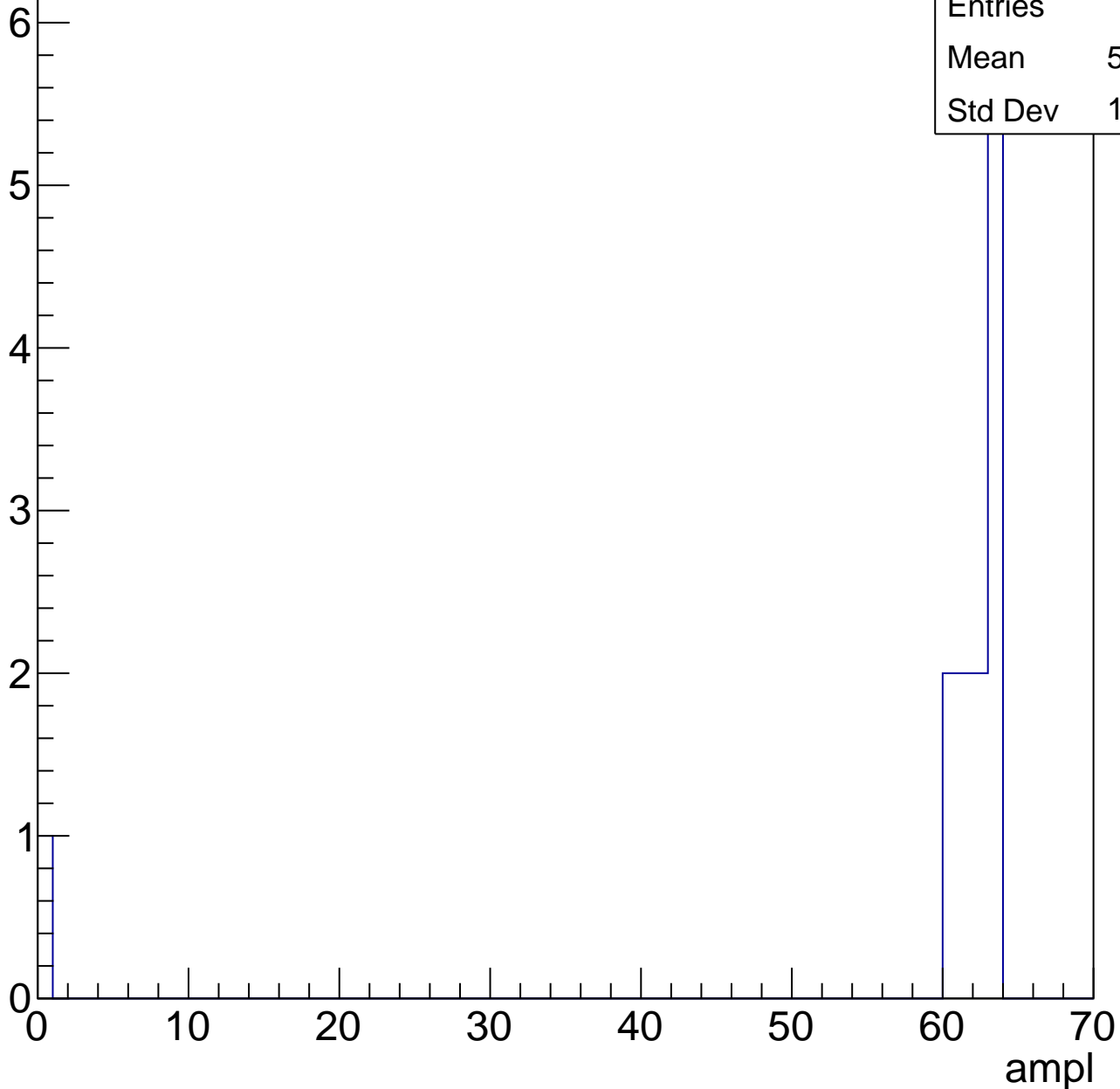


# B1L101S, U16-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	13
Mean	57.23
Std Dev	16.56





# B1L101S, U16-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch78, adc0

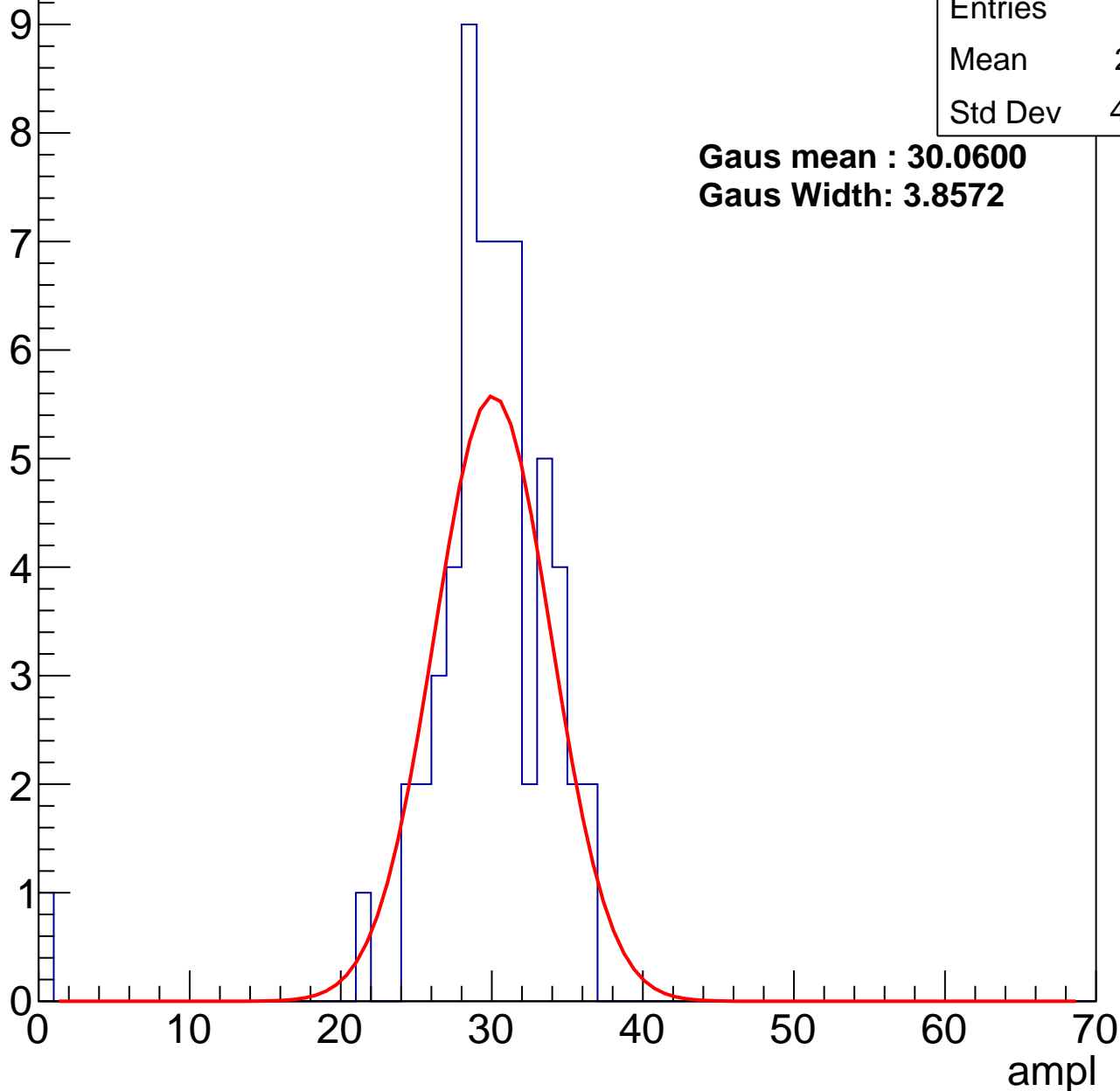
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	29.21
Std Dev	4.982

**Gaus mean : 30.0600**

**Gaus Width: 3.8572**



# B1L101S, U16-ch78, adc1

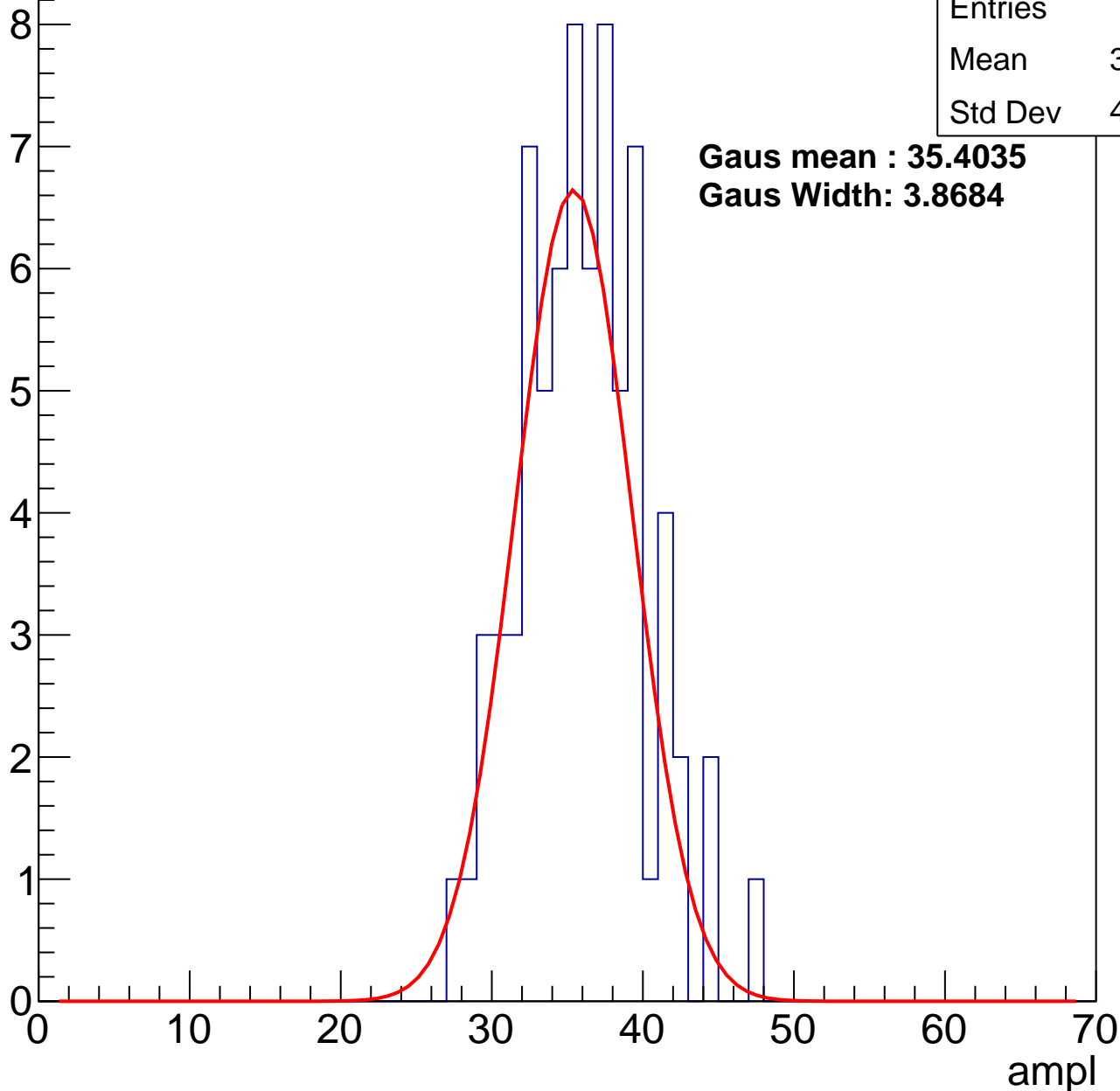
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	35.56
Std Dev	4.017

**Gaus mean : 35.4035**

**Gaus Width: 3.8684**



# B1L101S, U16-ch78, adc2

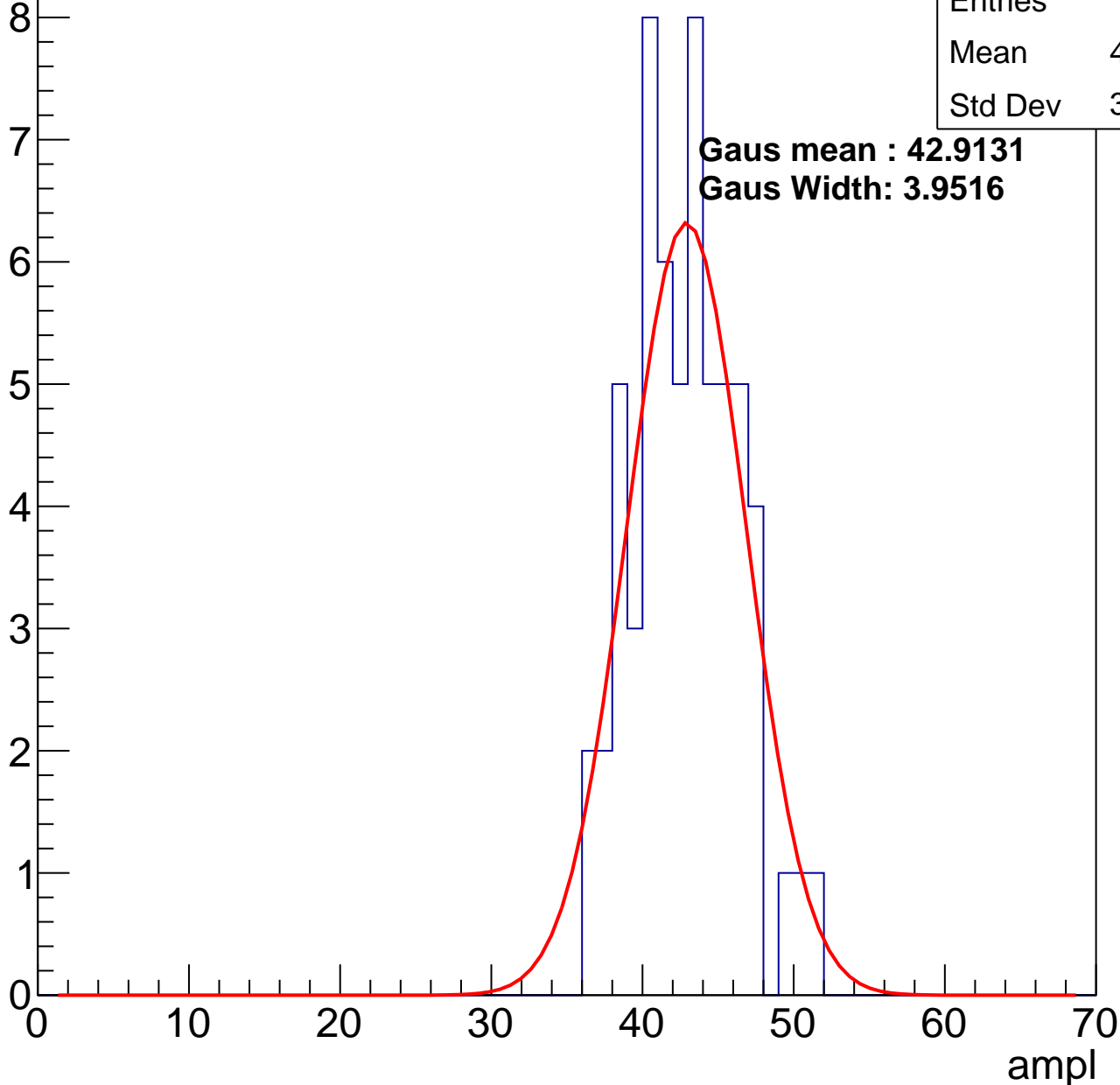
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	42.39
Std Dev	3.399

**Gaus mean : 42.9131**

**Gaus Width: 3.9516**

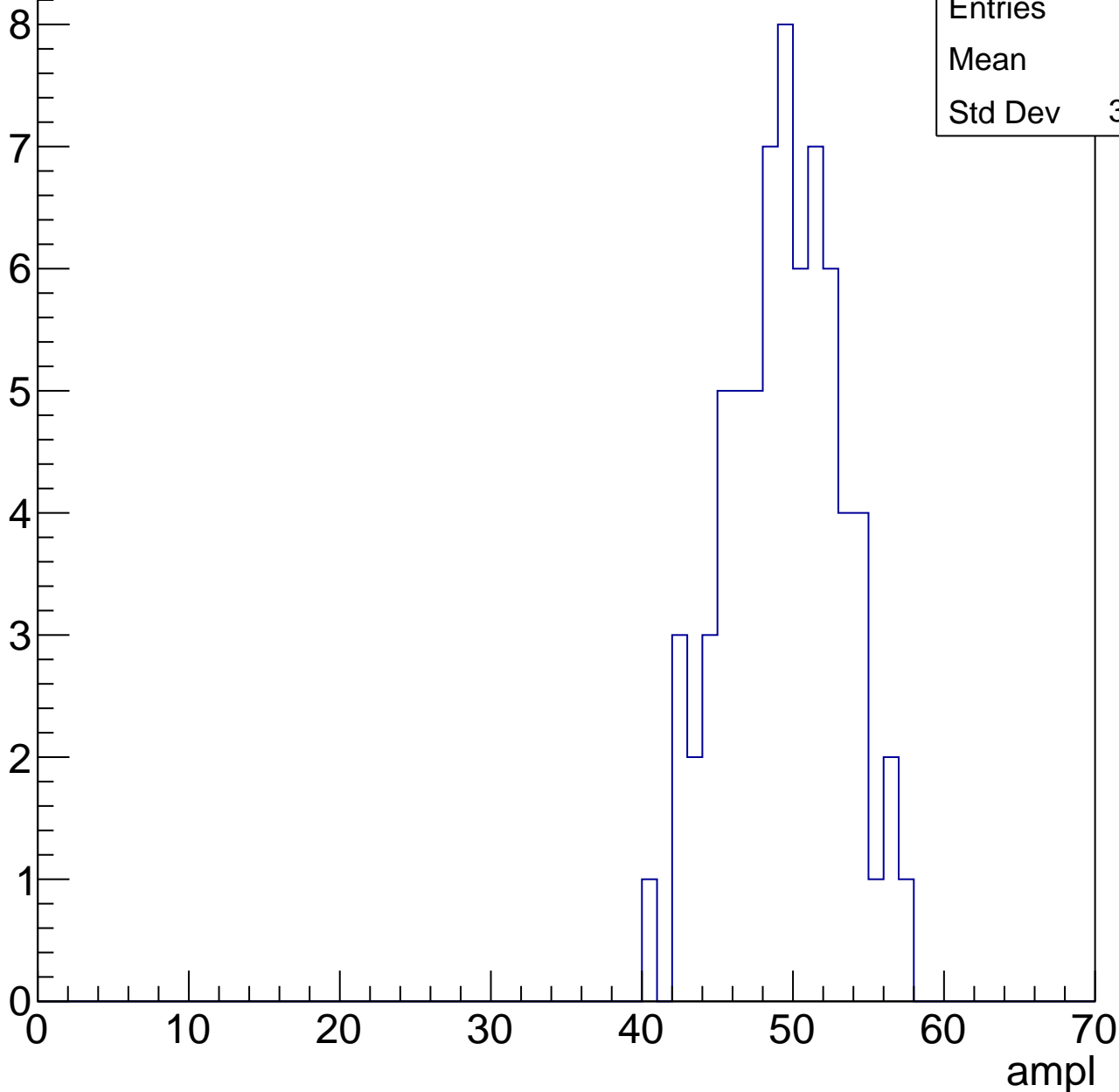


# B1L101S, U16-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	48.9
Std Dev	3.735

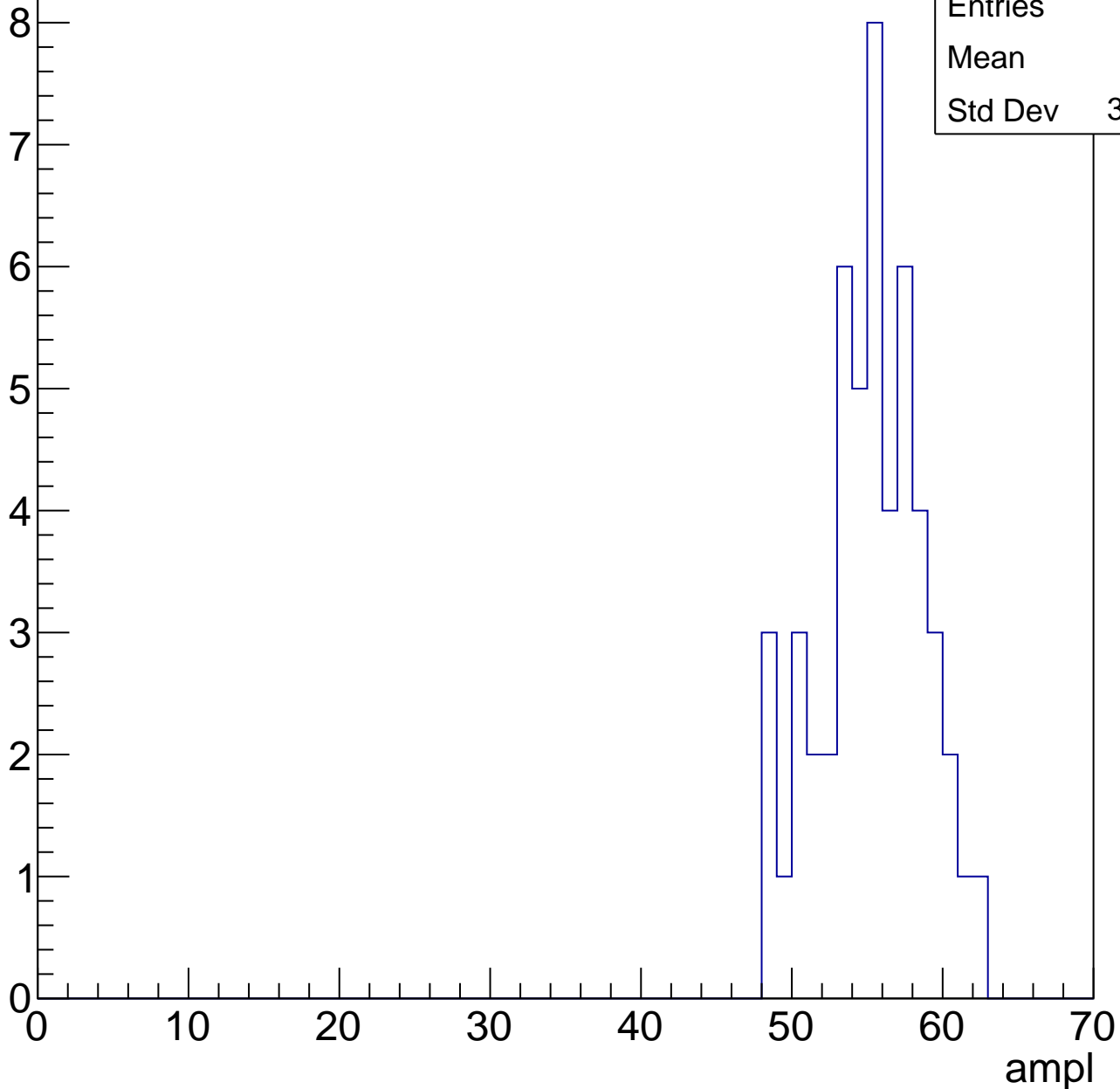


# B1L101S, U16-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	54.8
Std Dev	3.378

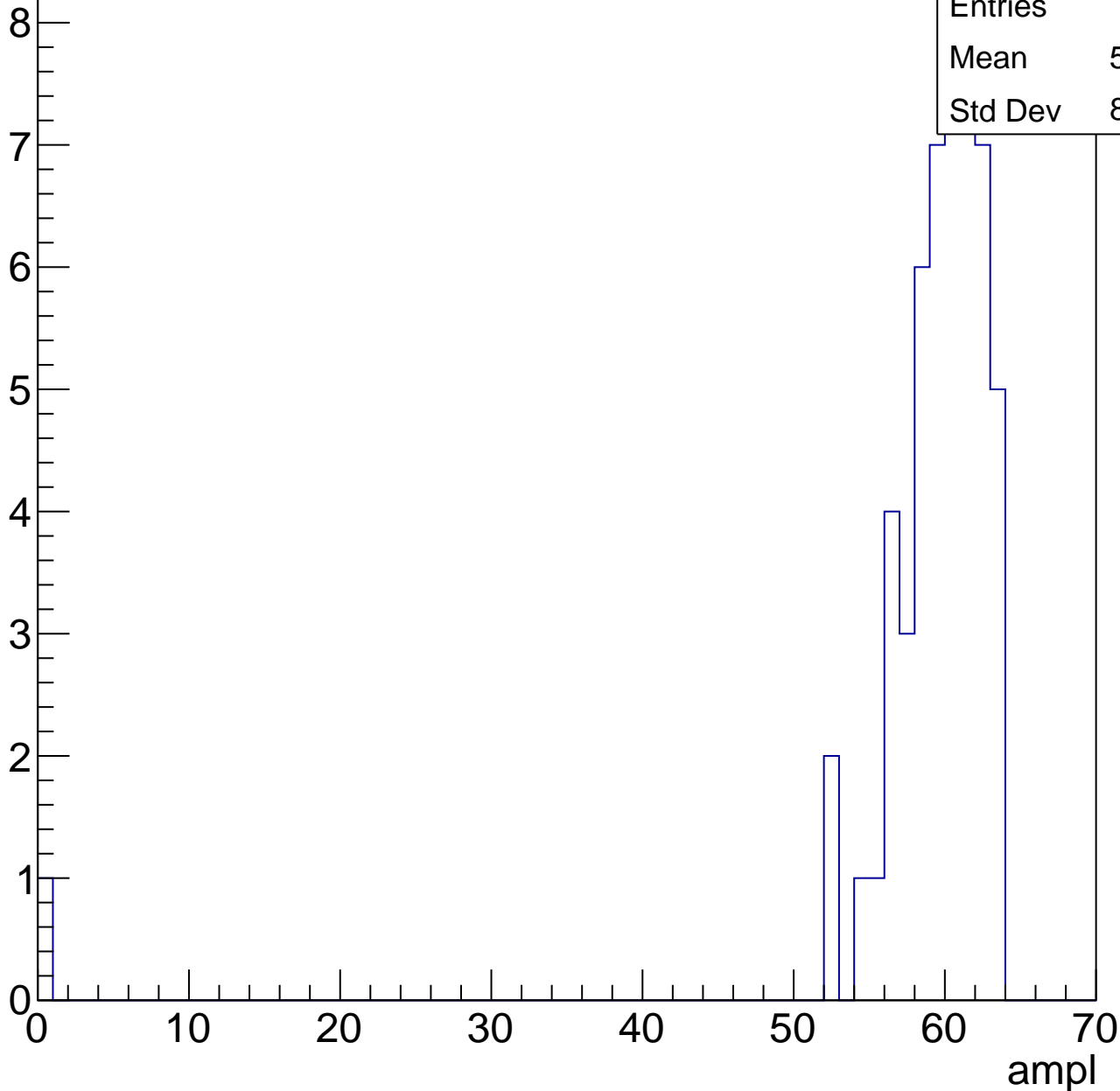


# B1L101S, U16-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	58.23
Std Dev	8.496

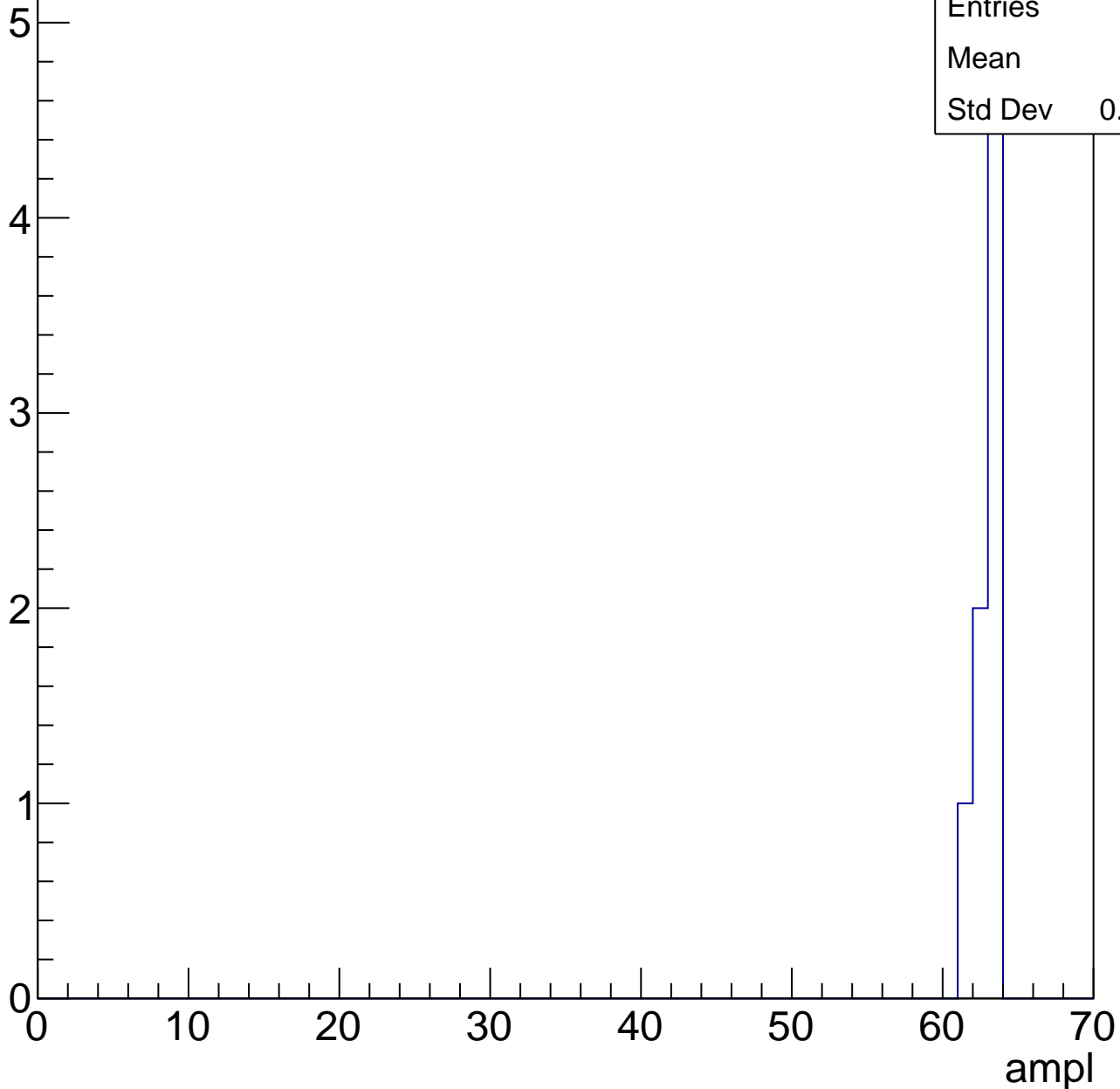


# B1L101S, U16-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	8
Mean	62.5
Std Dev	0.7071





# B1L101S, U16-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U16-ch79, adc0

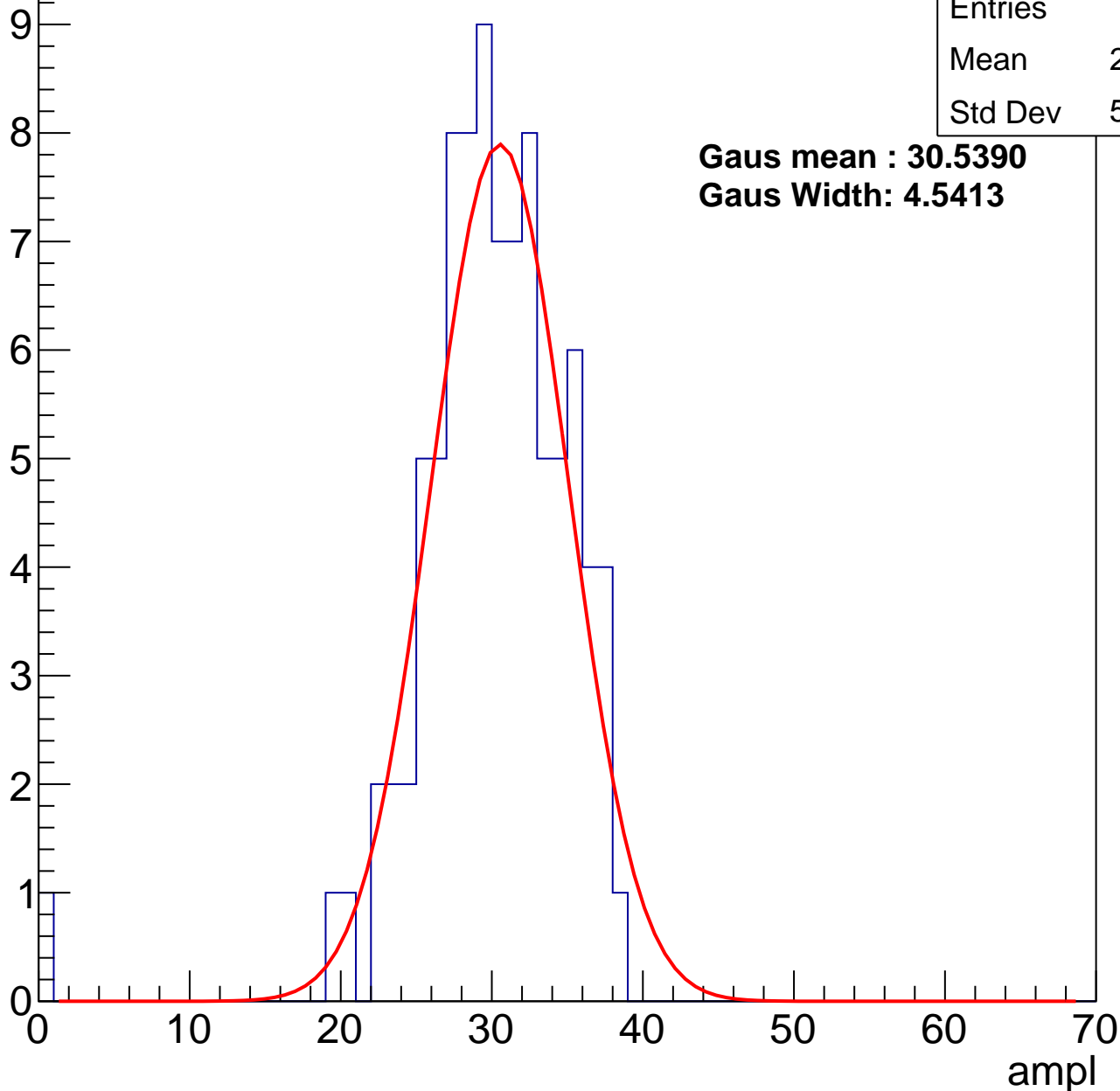
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	91
Mean	29.57
Std Dev	5.176

**Gaus mean : 30.5390**

**Gaus Width: 4.5413**



# B1L101S, U16-ch79, adc1

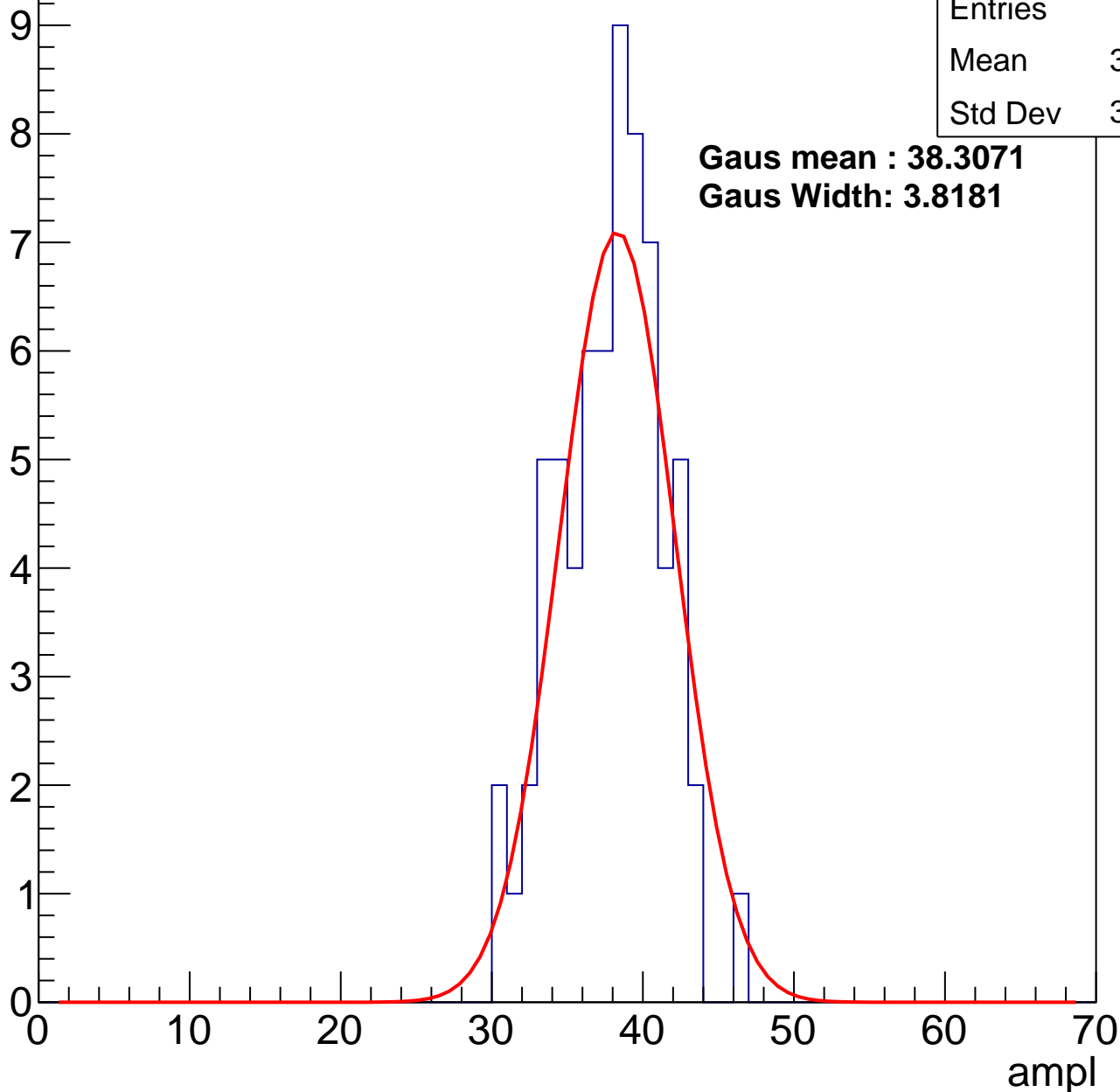
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	37.43
Std Dev	3.378

**Gaus mean : 38.3071**

**Gaus Width: 3.8181**



# B1L101S, U16-ch79, adc2

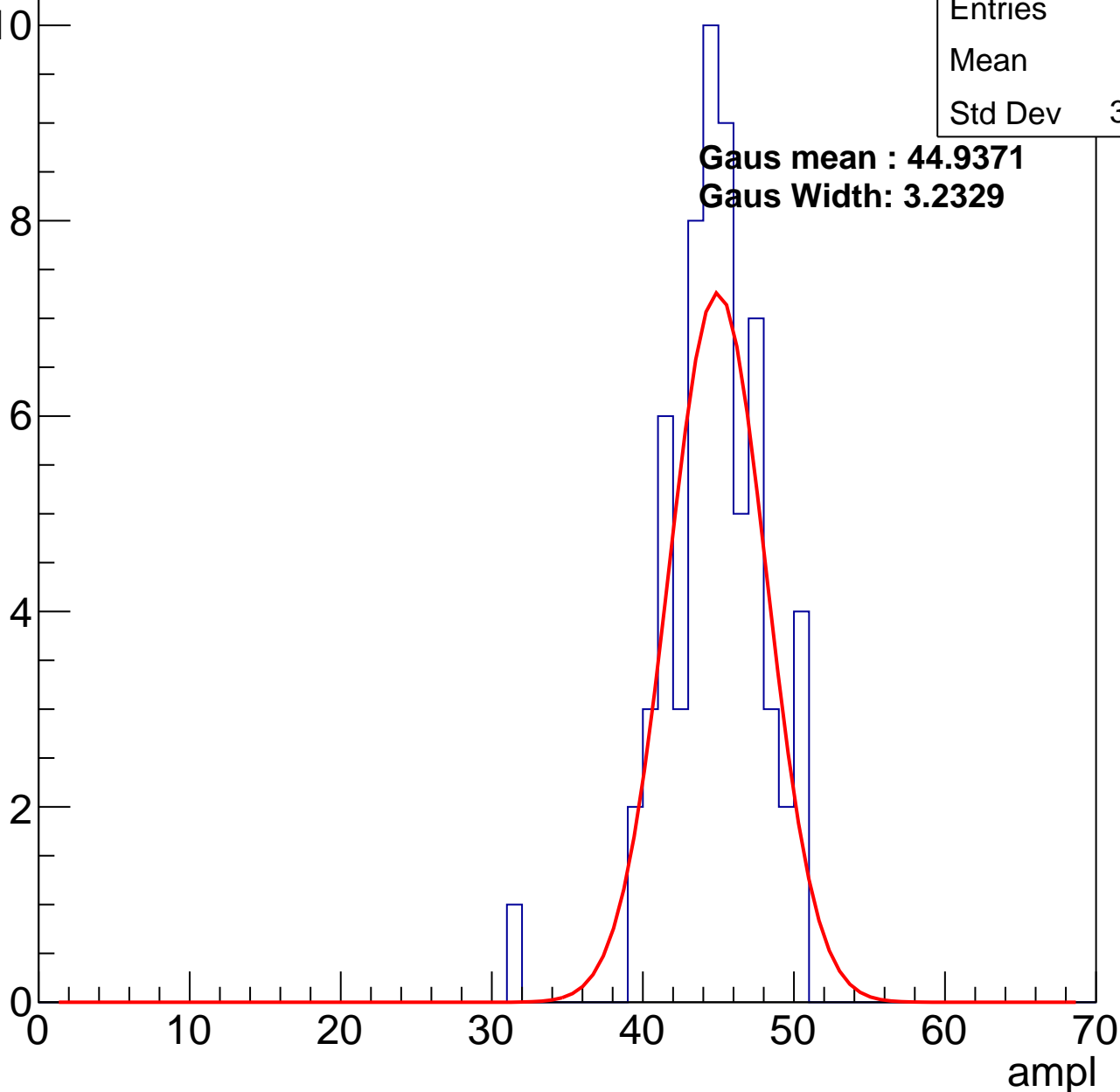
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	44.3
Std Dev	3.259

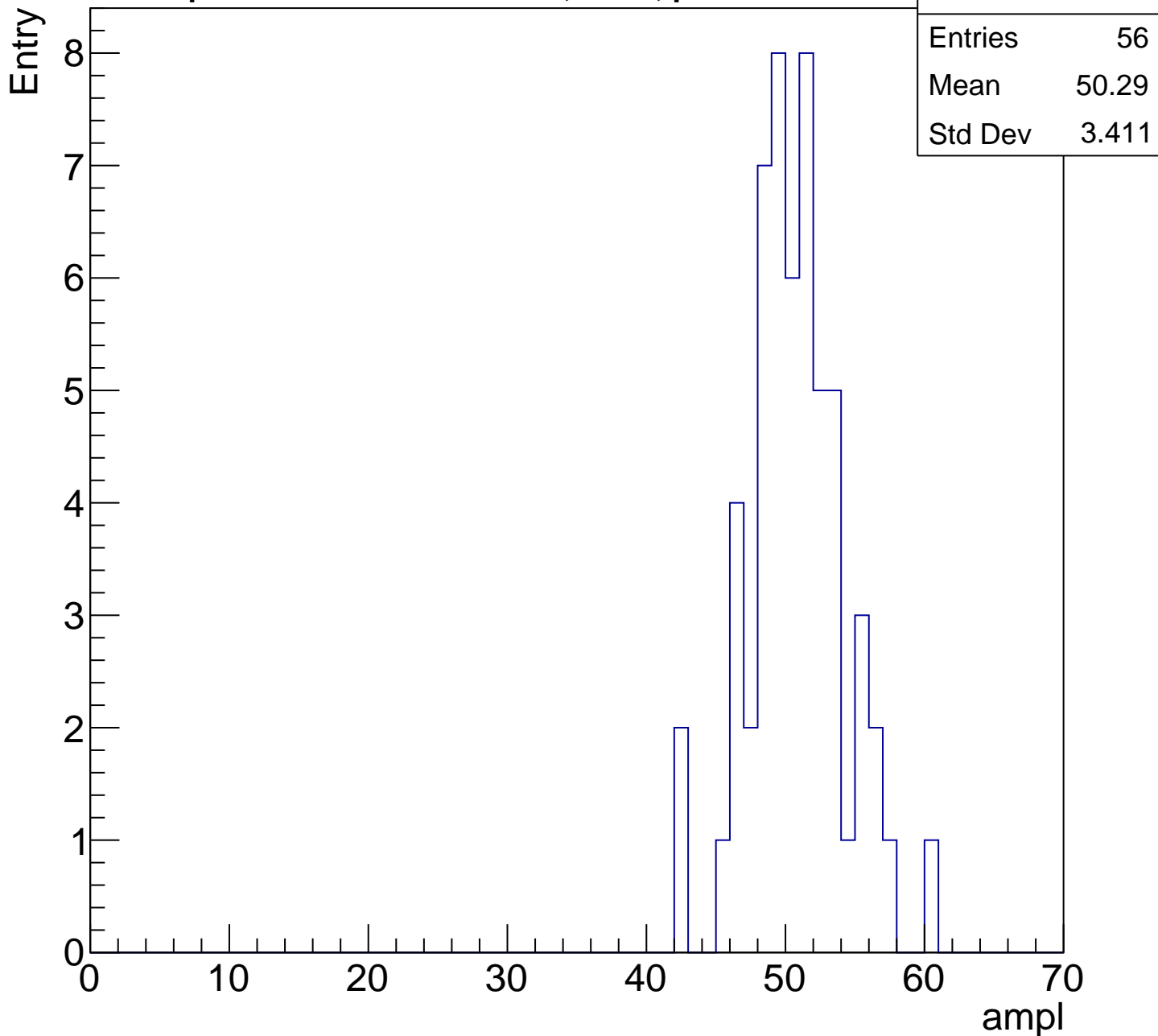
**Gaus mean : 44.9371**

**Gaus Width: 3.2329**



# B1L101S, U16-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

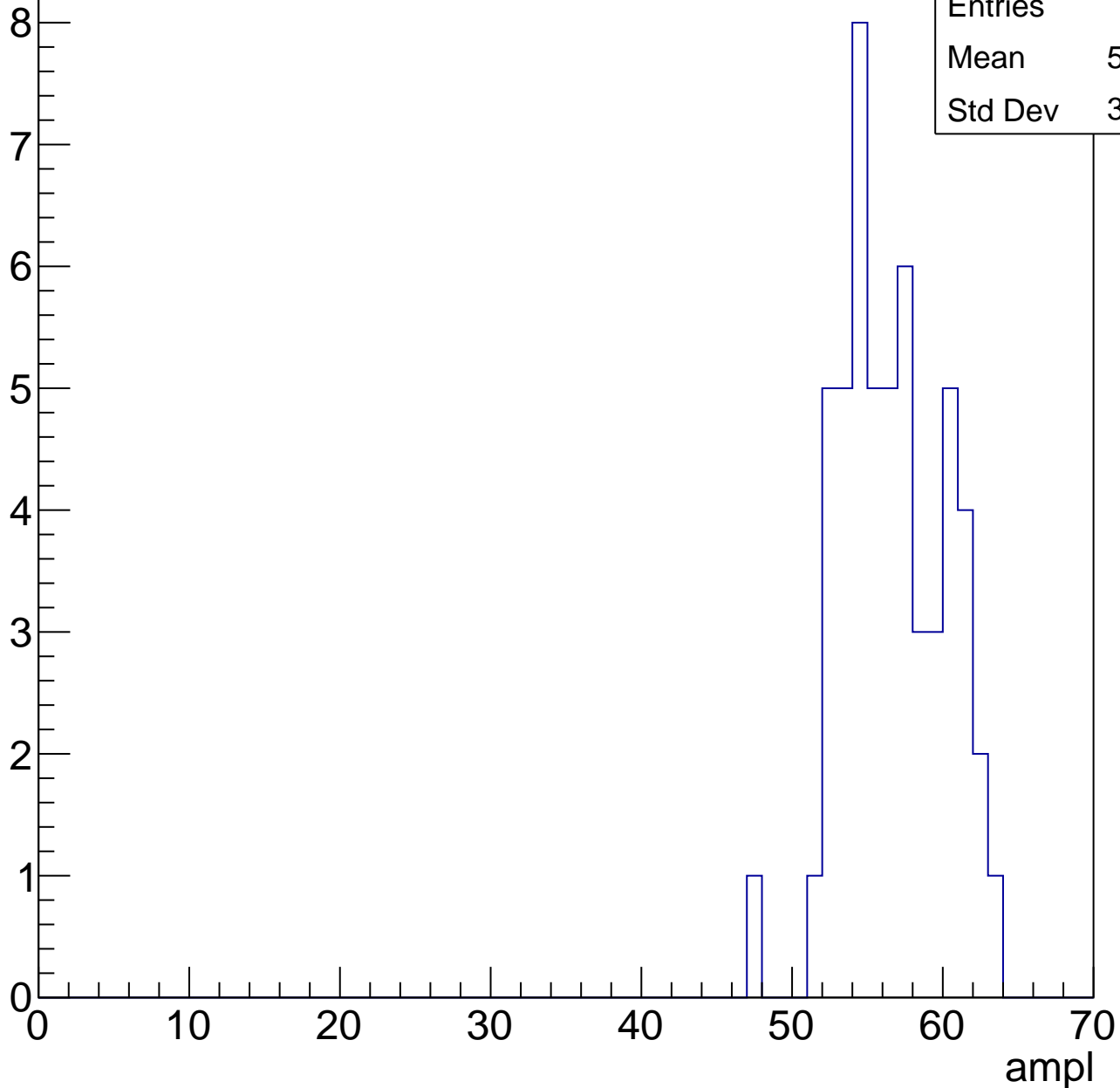


# B1L101S, U16-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

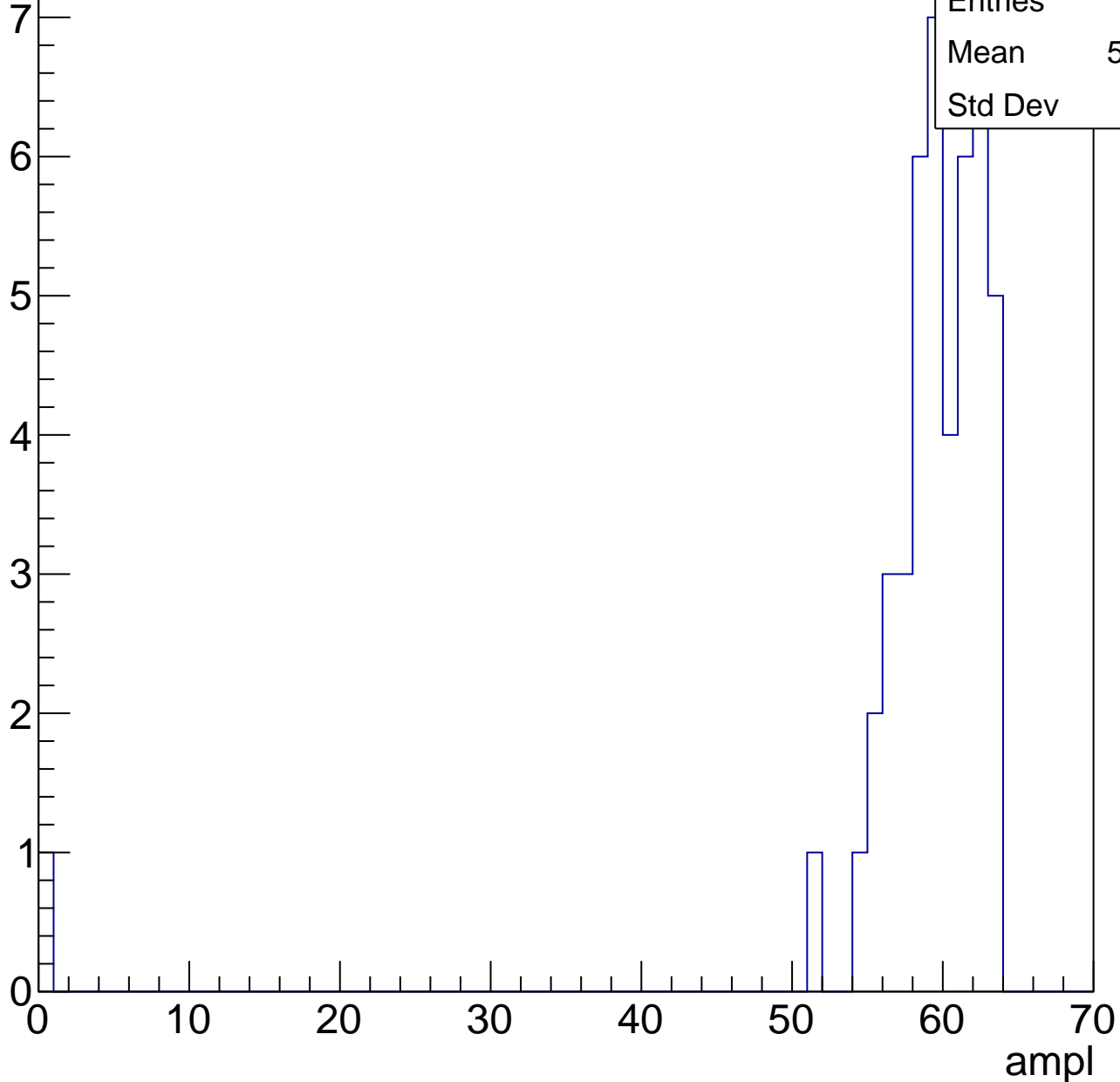
Entries	54
Mean	56.19
Std Dev	3.367



# B1L101S, U16-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

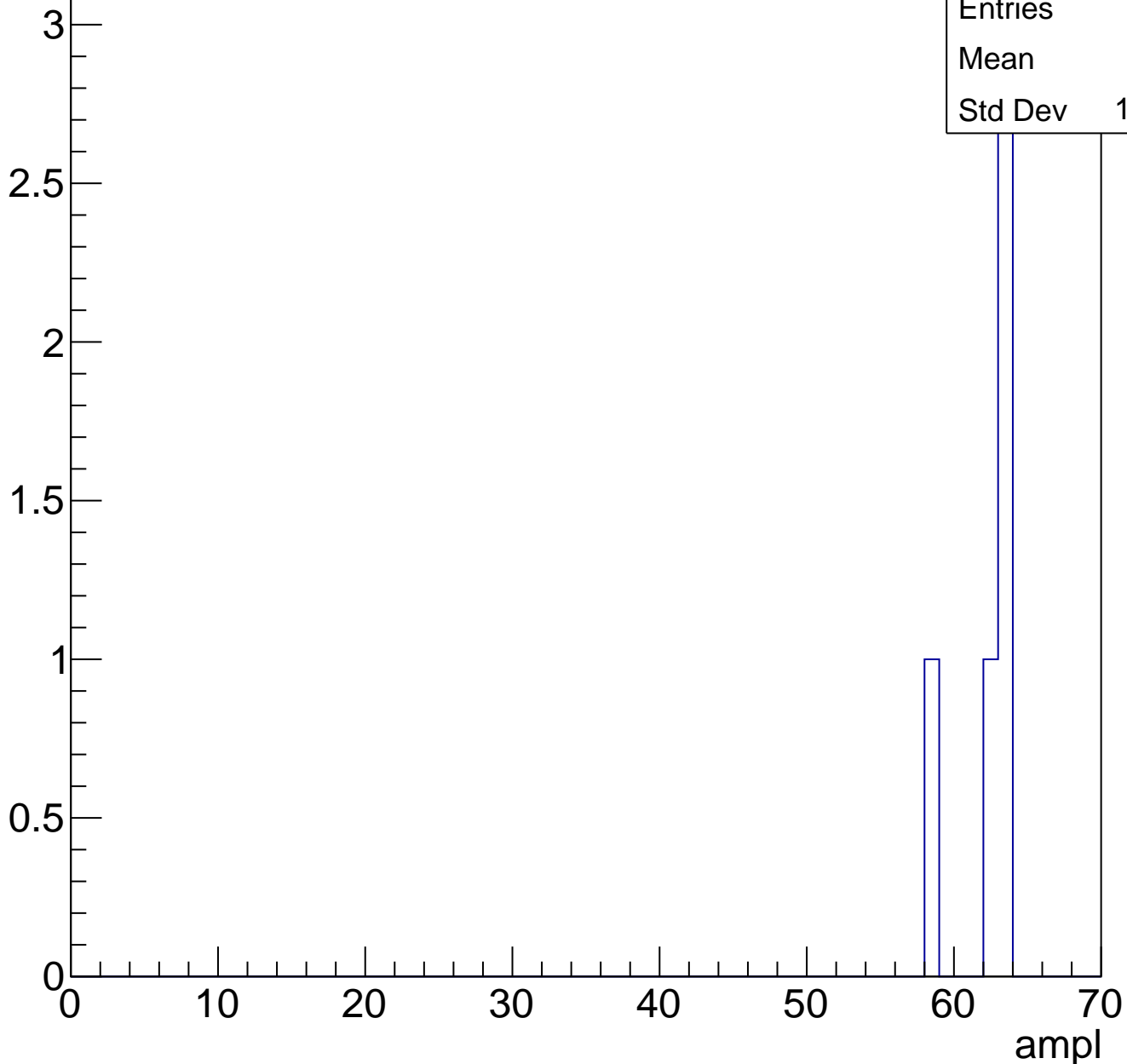
Entry



# B1L101S, U16-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

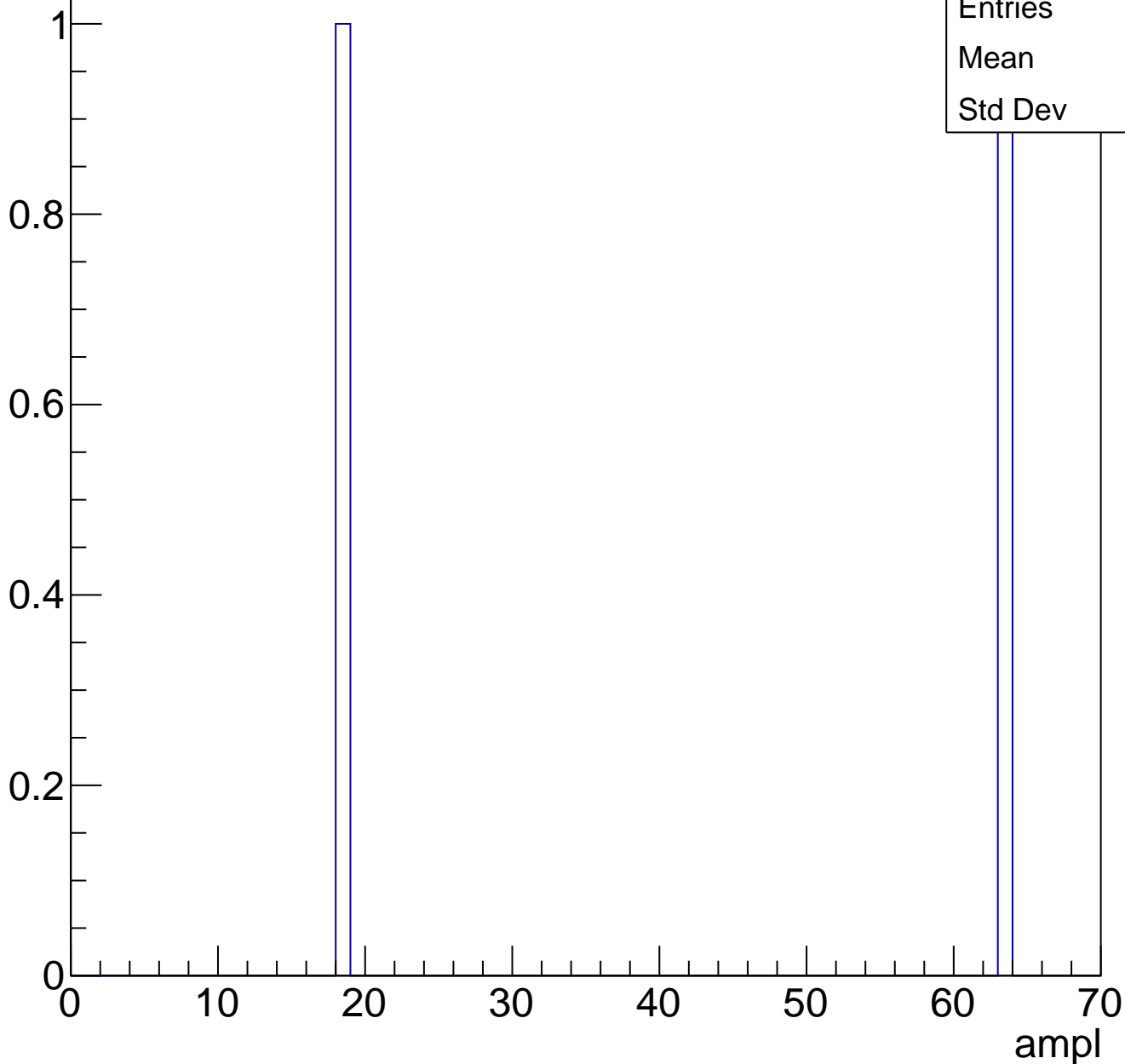




# B1L101S, U16-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch80, adc0

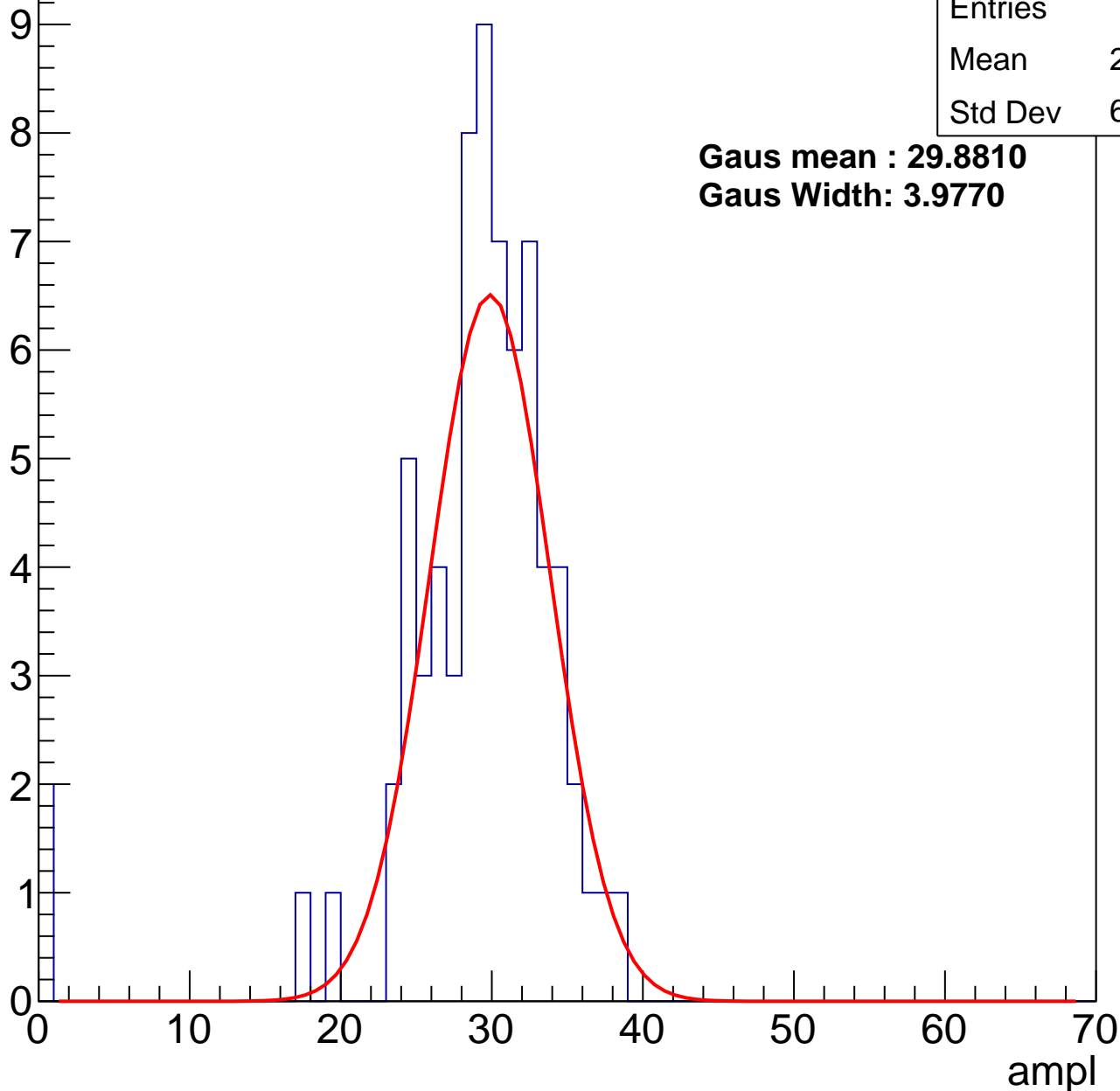
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	28.39
Std Dev	6.195

**Gaus mean : 29.8810**

**Gaus Width: 3.9770**



# B1L101S, U16-ch80, adc1

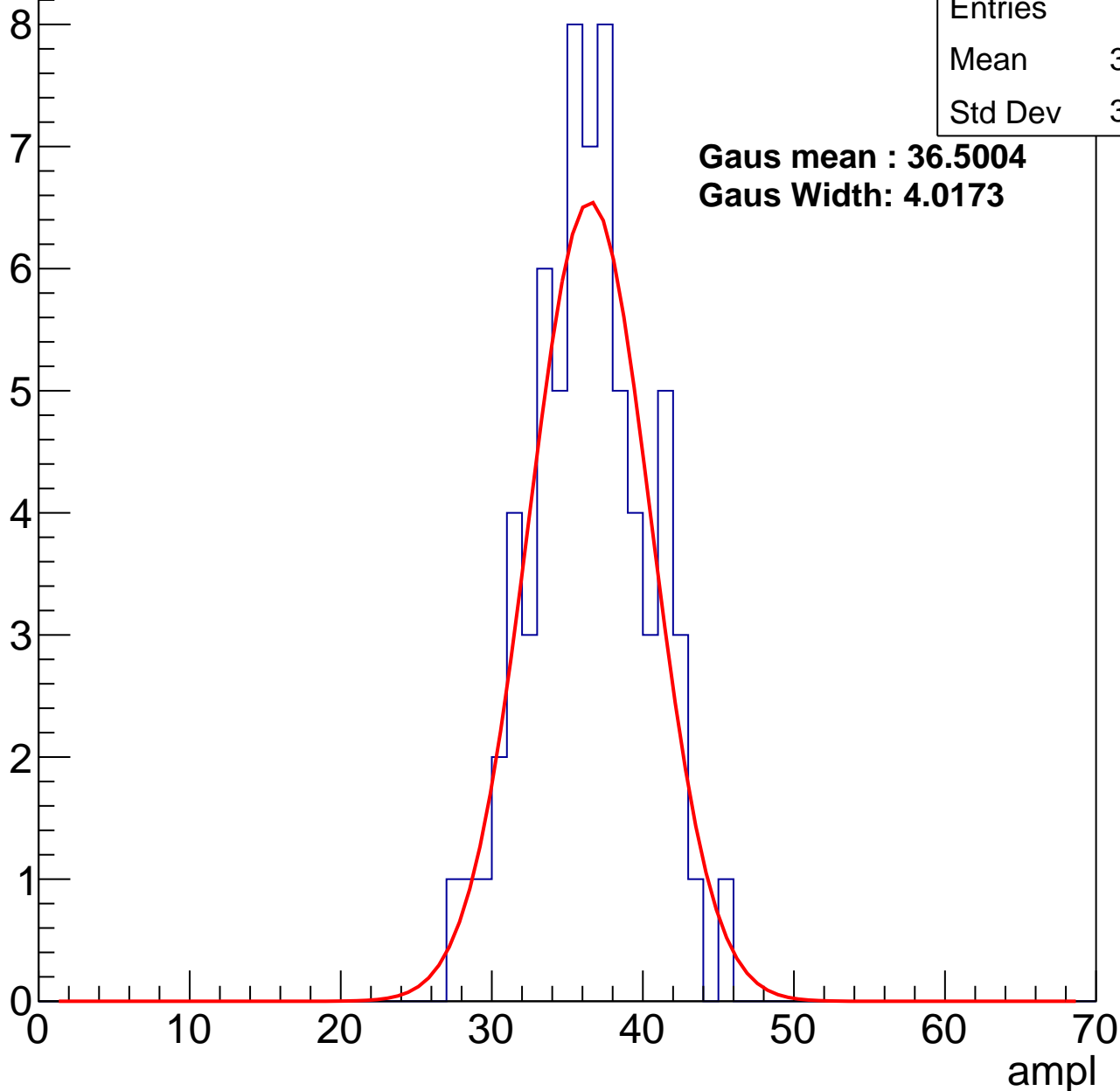
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	35.96
Std Dev	3.779

**Gaus mean : 36.5004**

**Gaus Width: 4.0173**



# B1L101S, U16-ch80, adc2

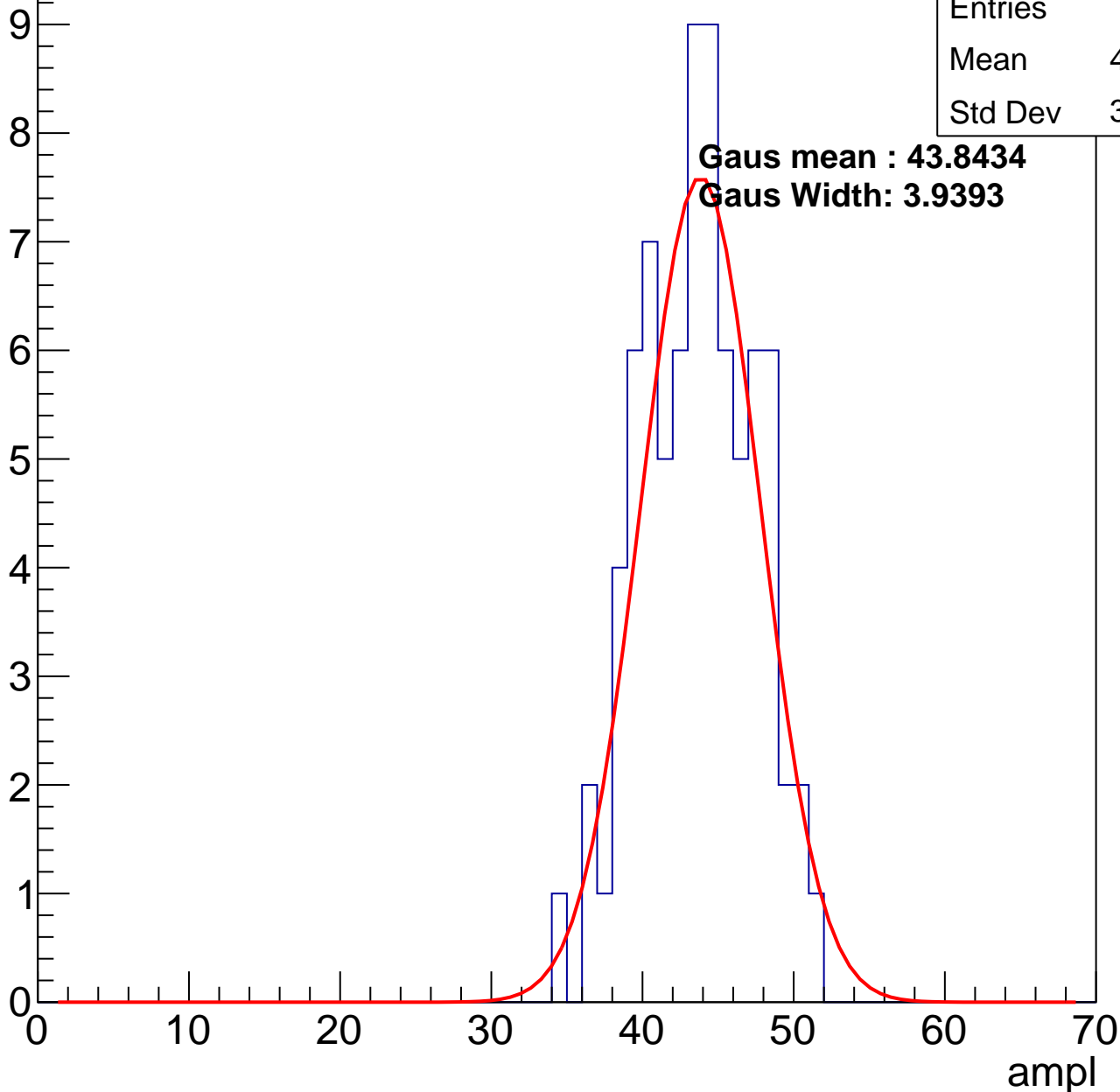
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	43.18
Std Dev	3.679

**Gaus mean : 43.8434**

**Gaus Width: 3.9393**

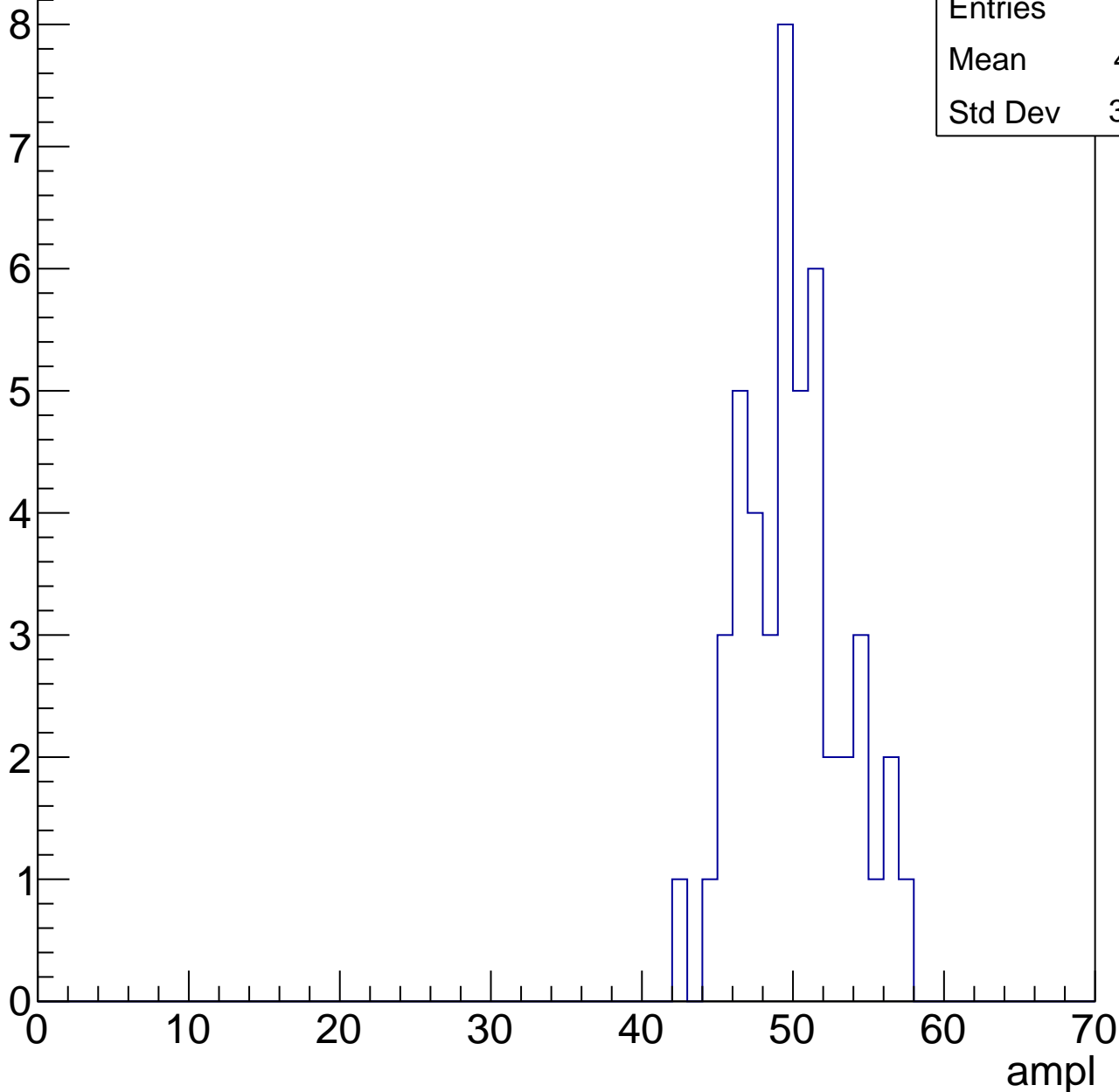


# B1L101S, U16-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

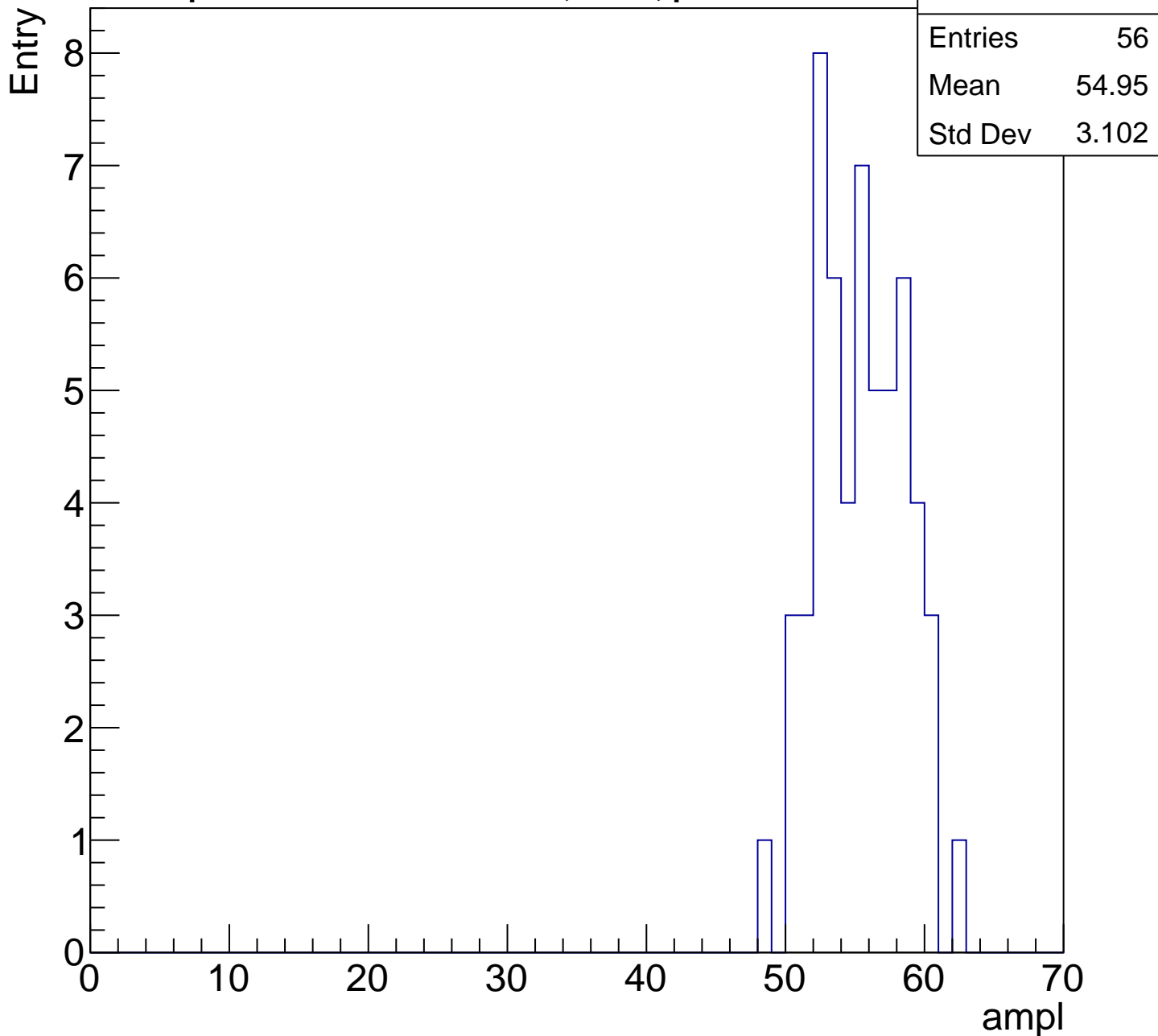
Entry

Entries	47
Mean	49.51
Std Dev	3.345



# B1L101S, U16-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

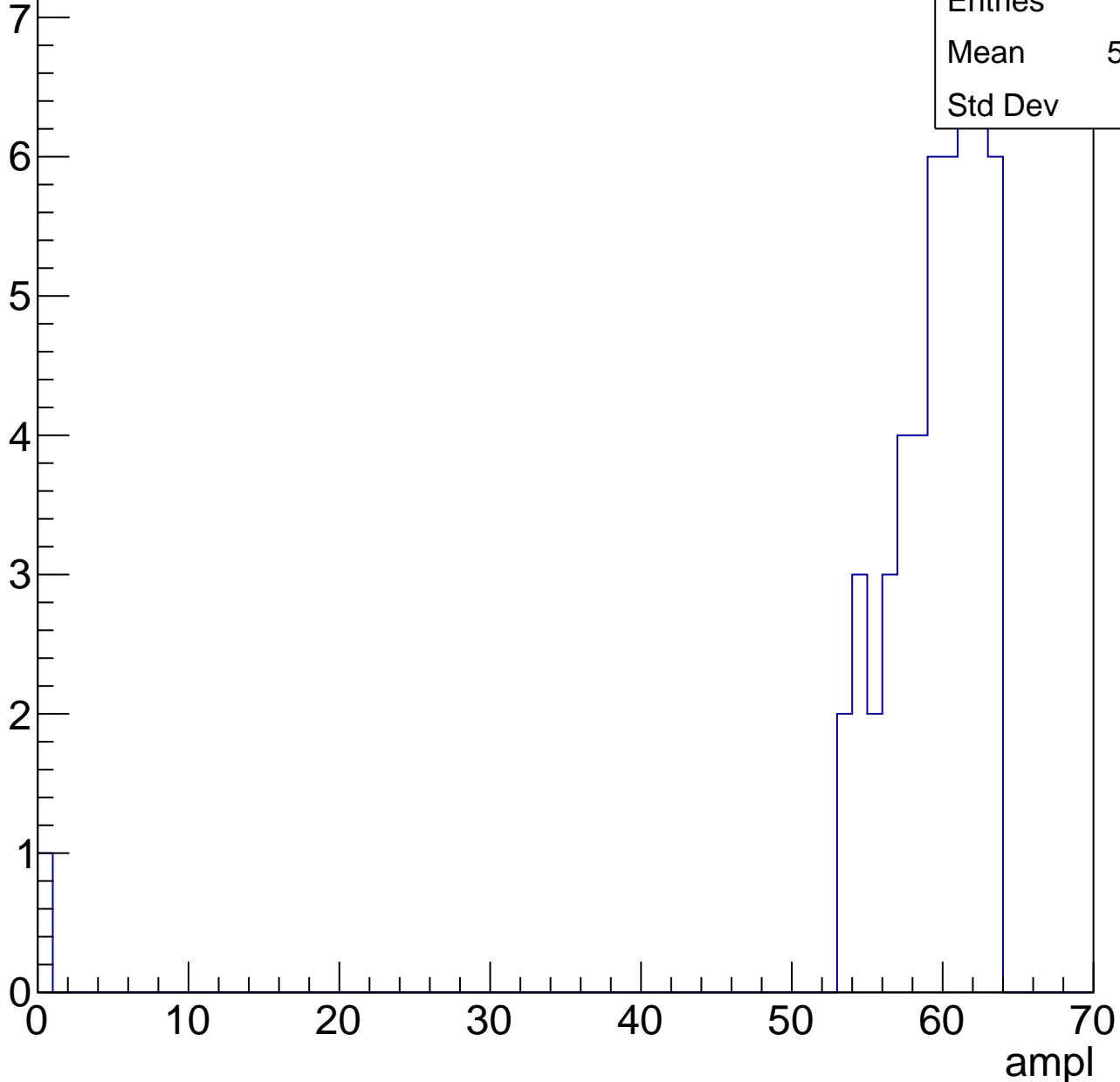


# B1L101S, U16-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

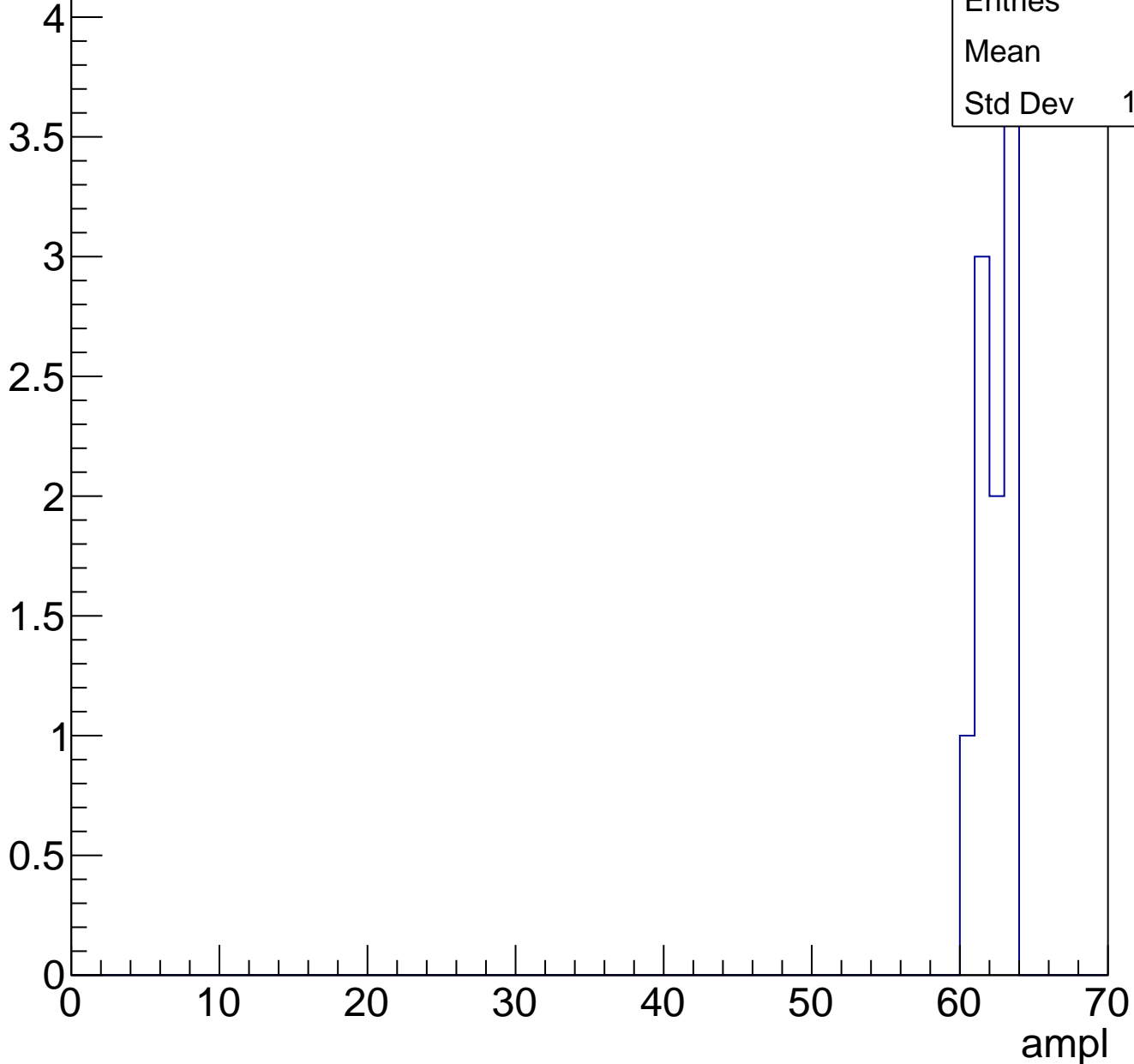
Entries	51
Mean	58.02
Std Dev	8.69



# B1L101S, U16-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U16-ch81, adc0

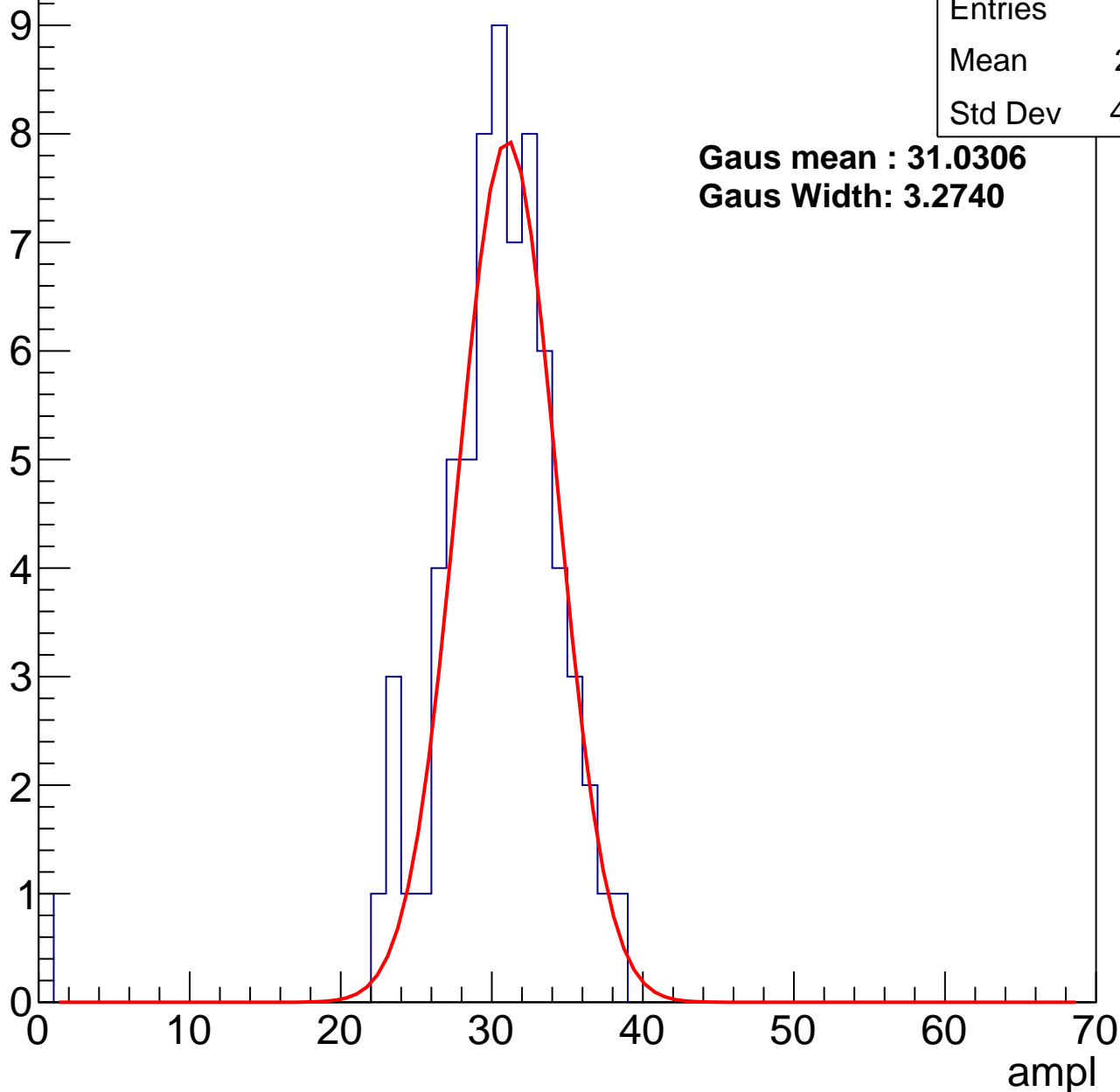
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	29.71
Std Dev	4.957

**Gaus mean : 31.0306**

**Gaus Width: 3.2740**



# B1L101S, U16-ch81, adc1

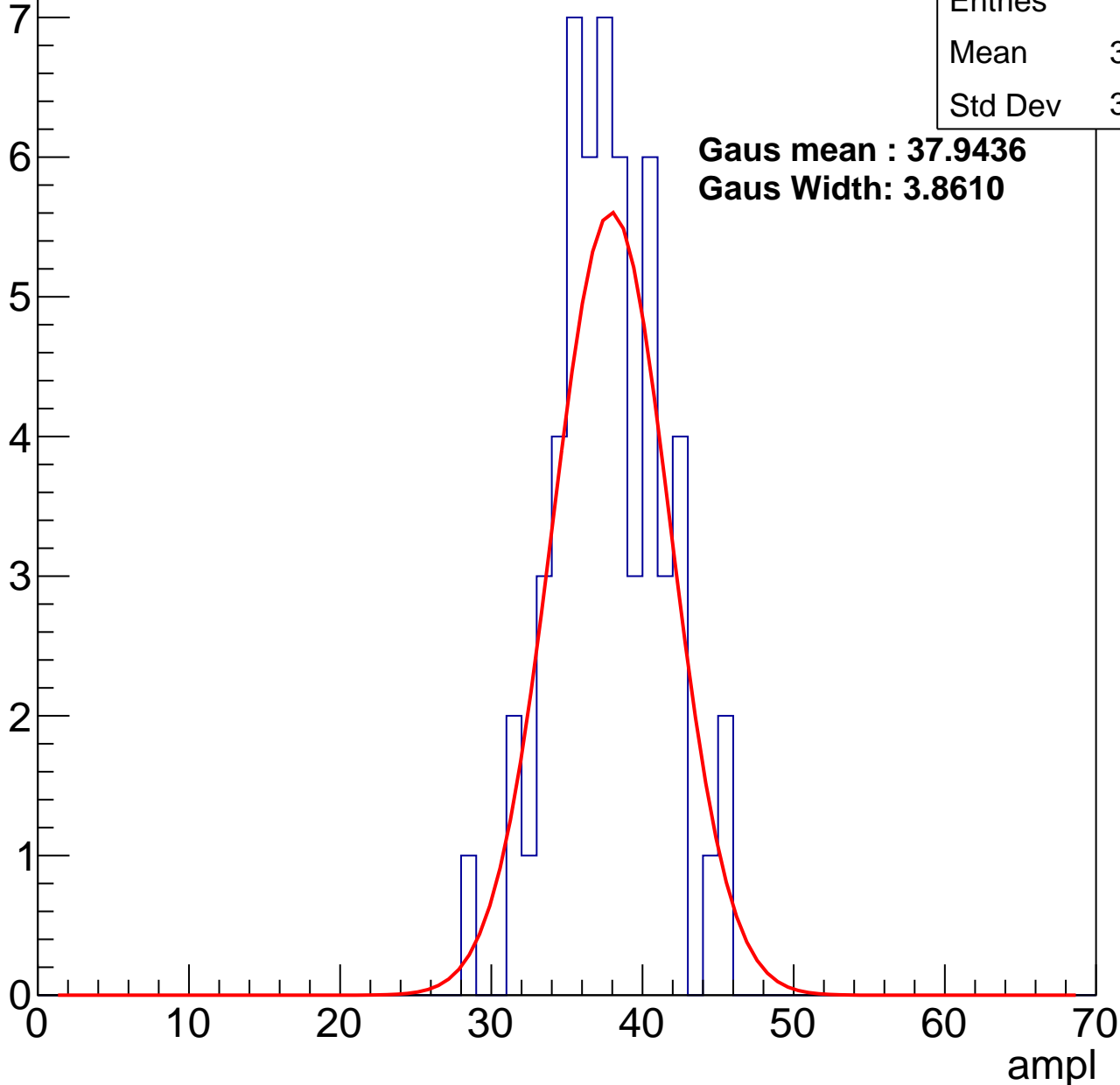
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	37.27
Std Dev	3.508

**Gaus mean : 37.9436**

**Gaus Width: 3.8610**



# B1L101S, U16-ch81, adc2

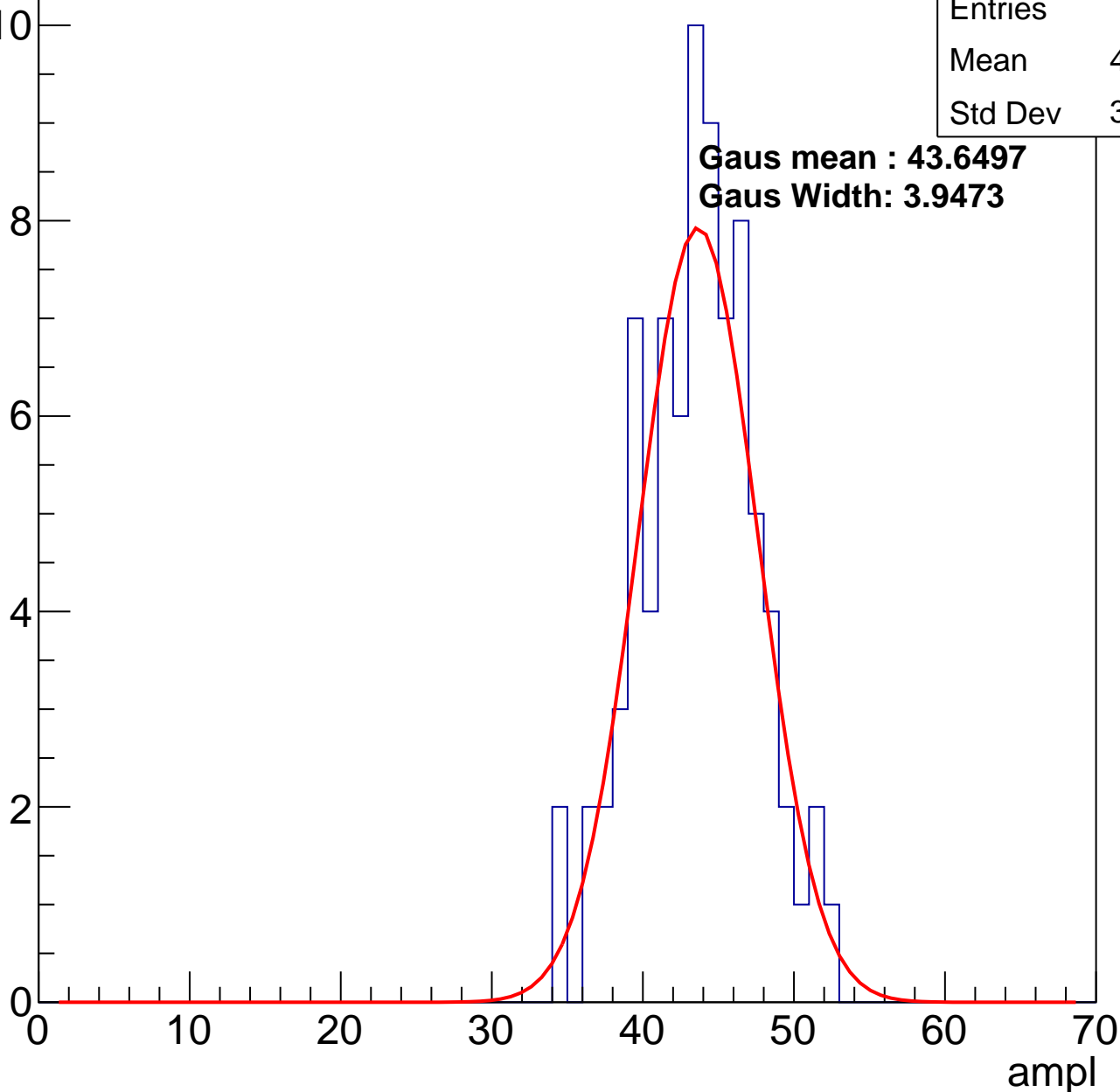
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	43.15
Std Dev	3.835

**Gaus mean : 43.6497**

**Gaus Width: 3.9473**

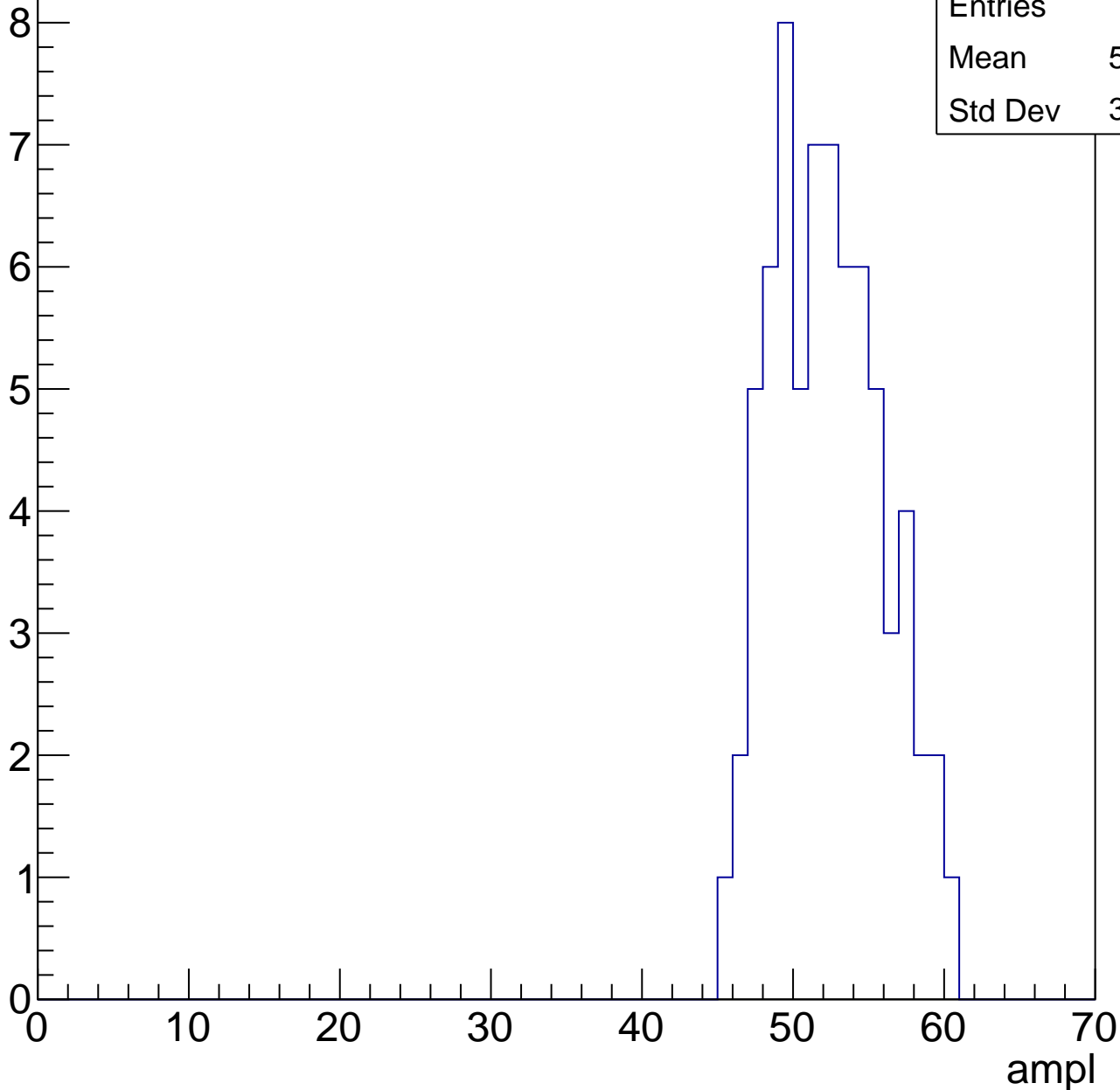


# B1L101S, U16-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	51.86
Std Dev	3.579

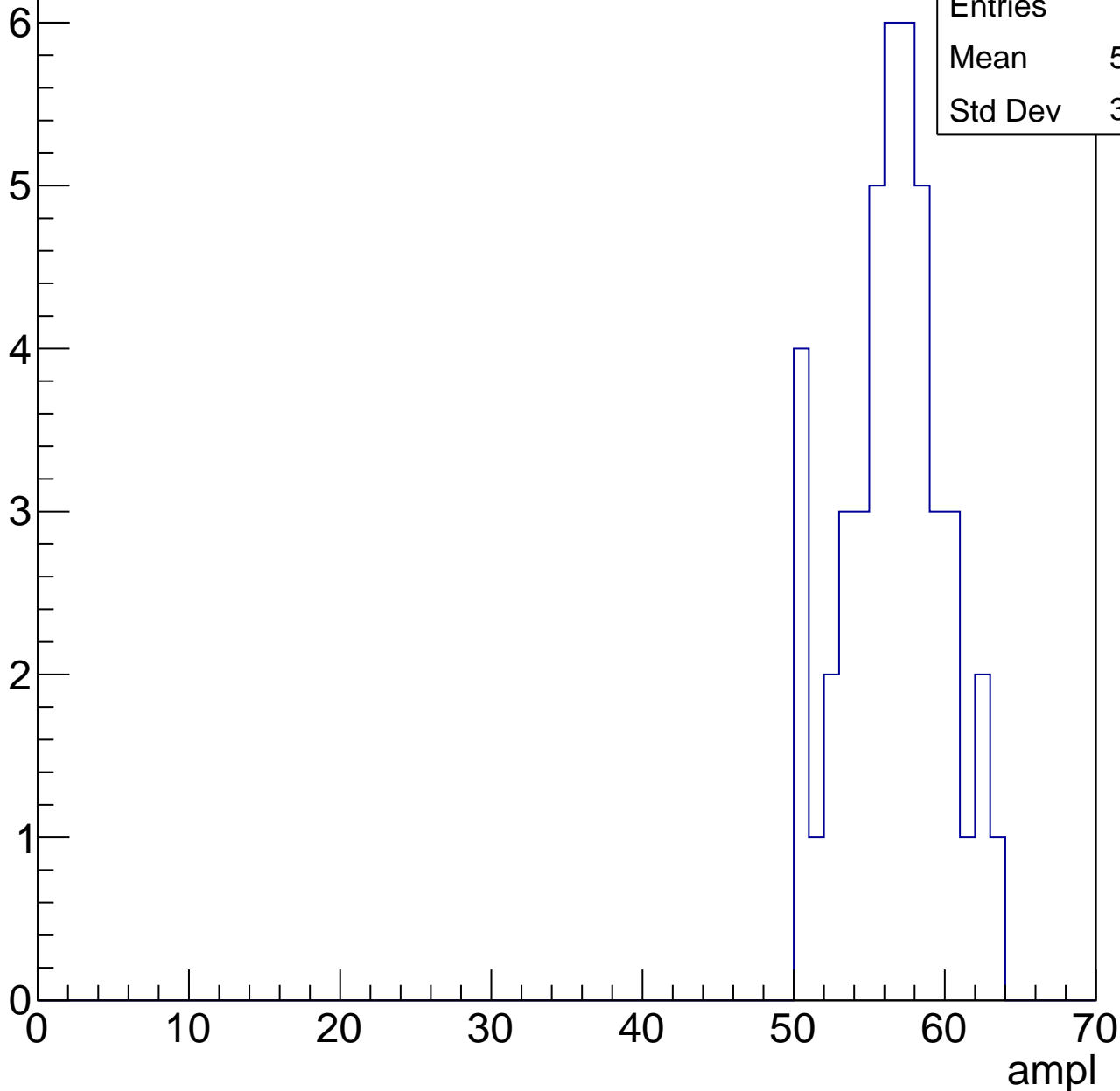


# B1L101S, U16-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	56.09
Std Dev	3.305

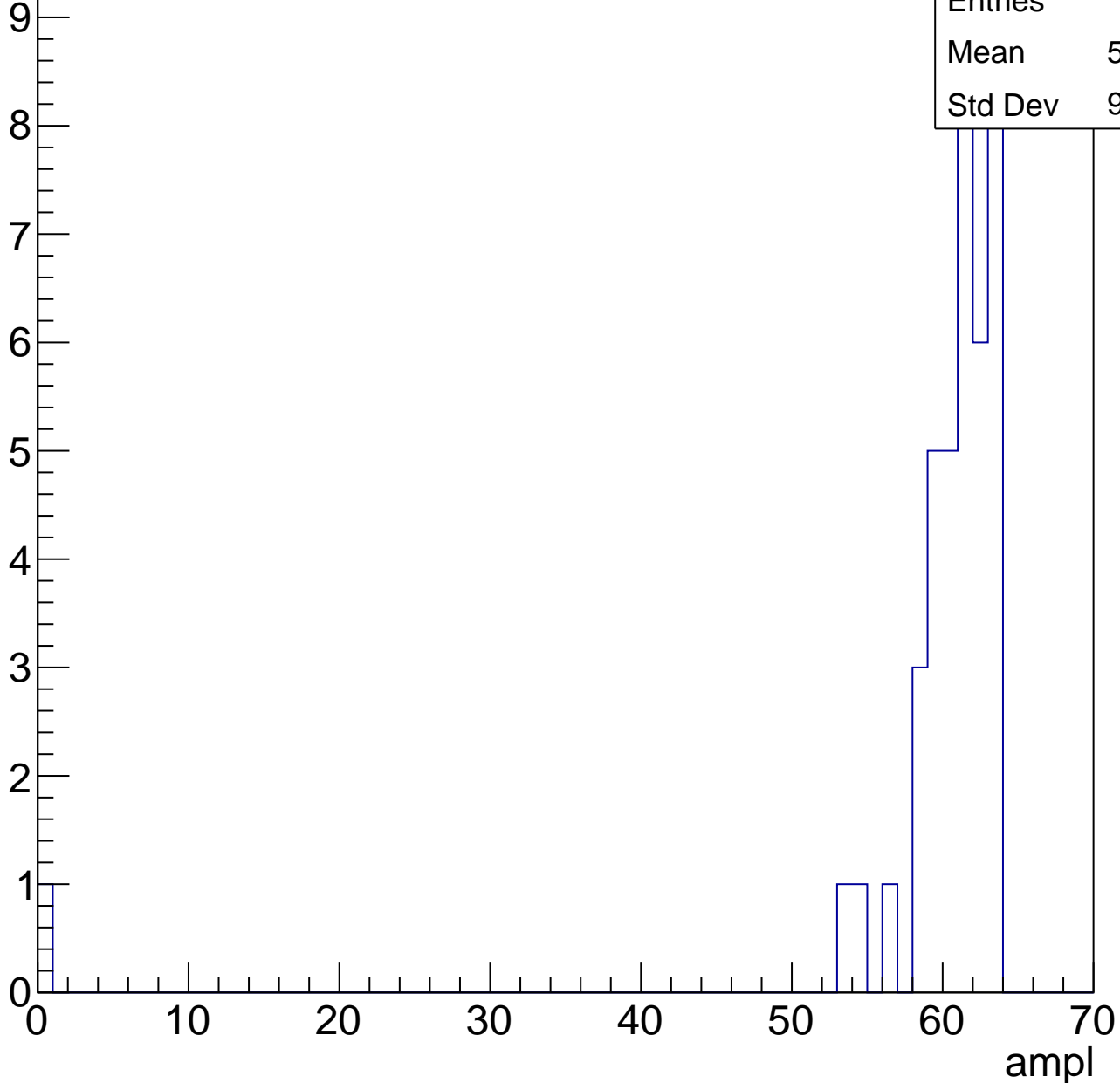


# B1L101S, U16-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

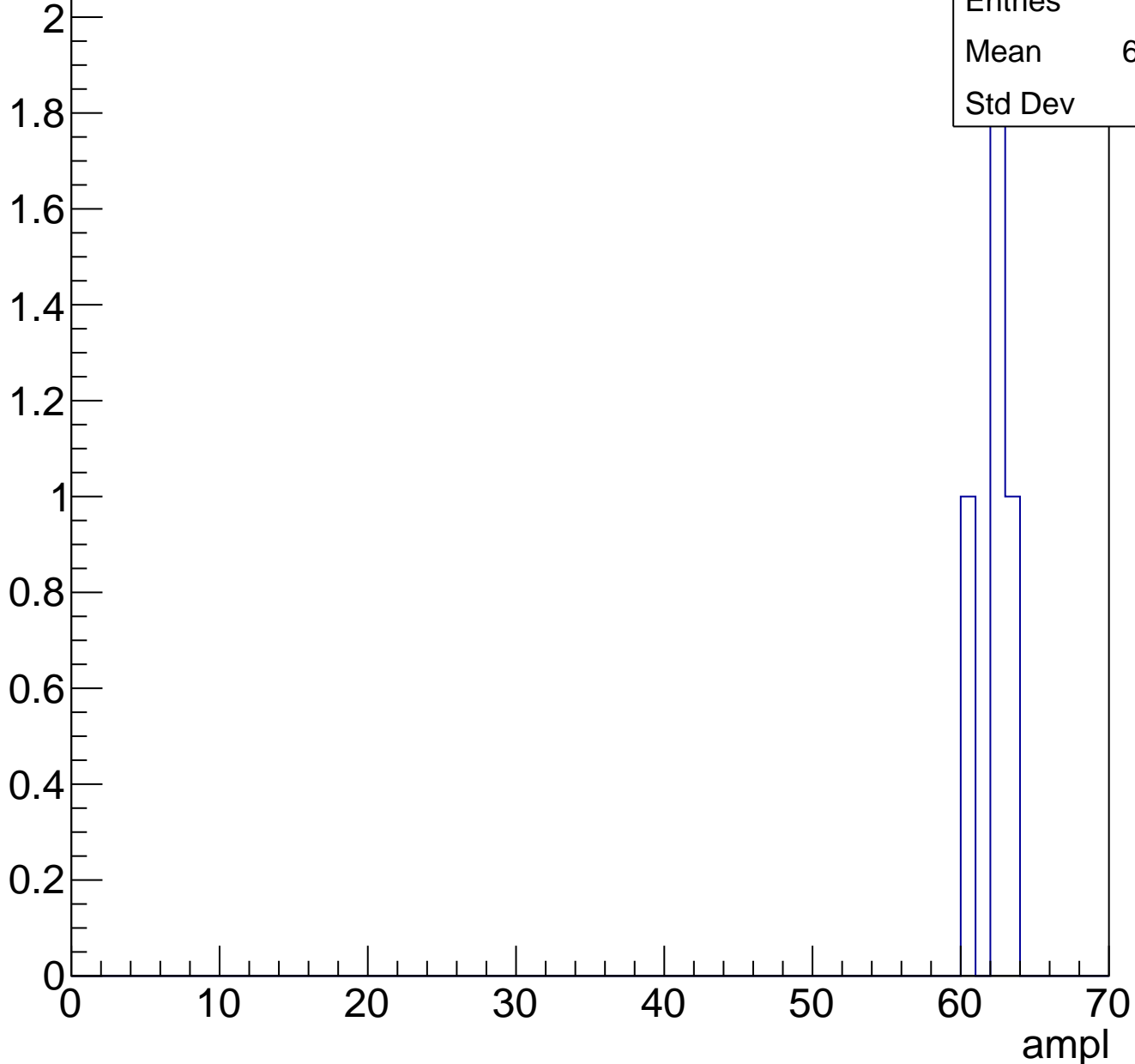
Entries	40
Mean	58.92
Std Dev	9.717



# B1L101S, U16-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch82, adc0

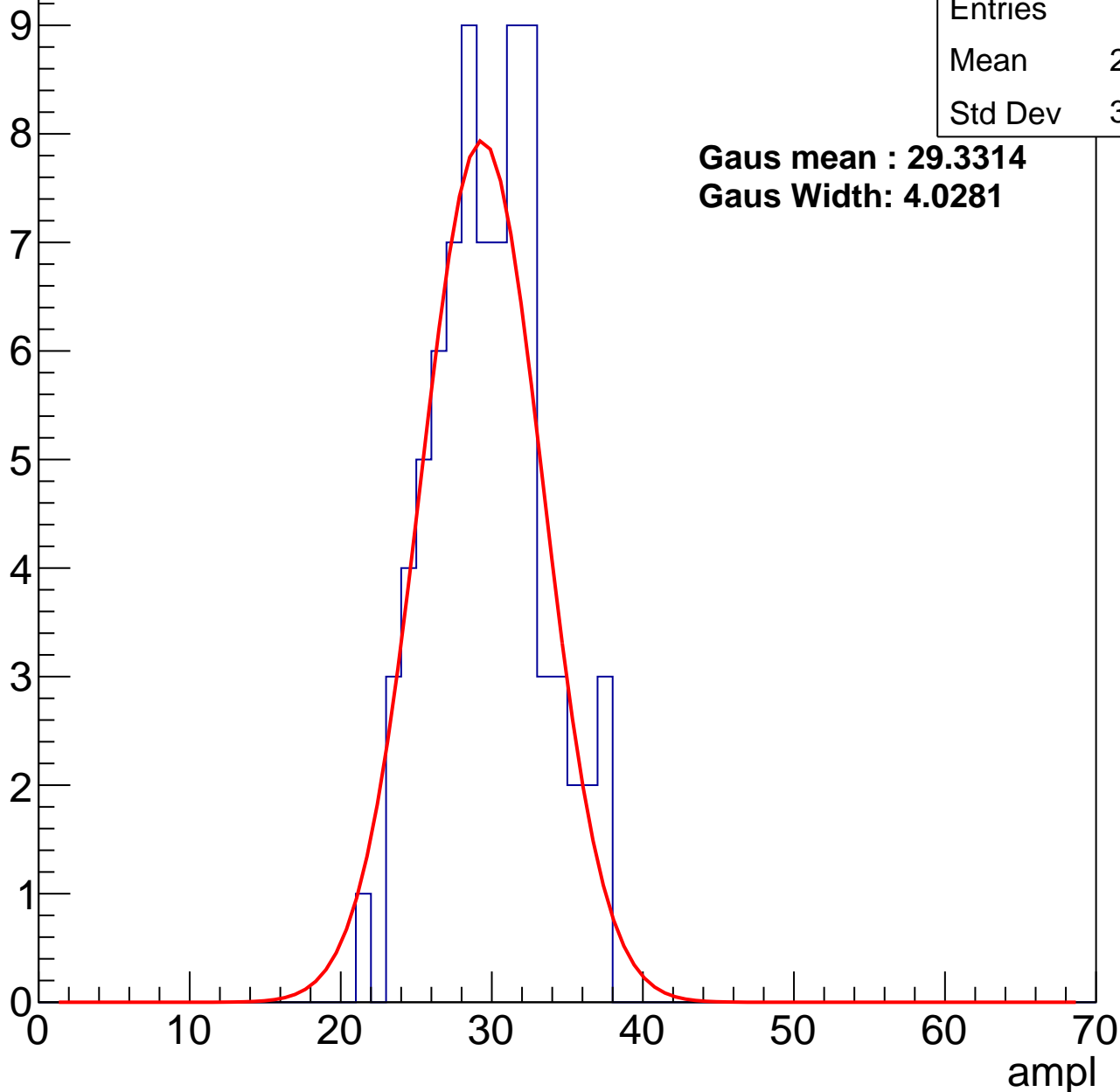
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	29.27
Std Dev	3.616

**Gaus mean : 29.3314**

**Gaus Width: 4.0281**



# B1L101S, U16-ch82, adc1

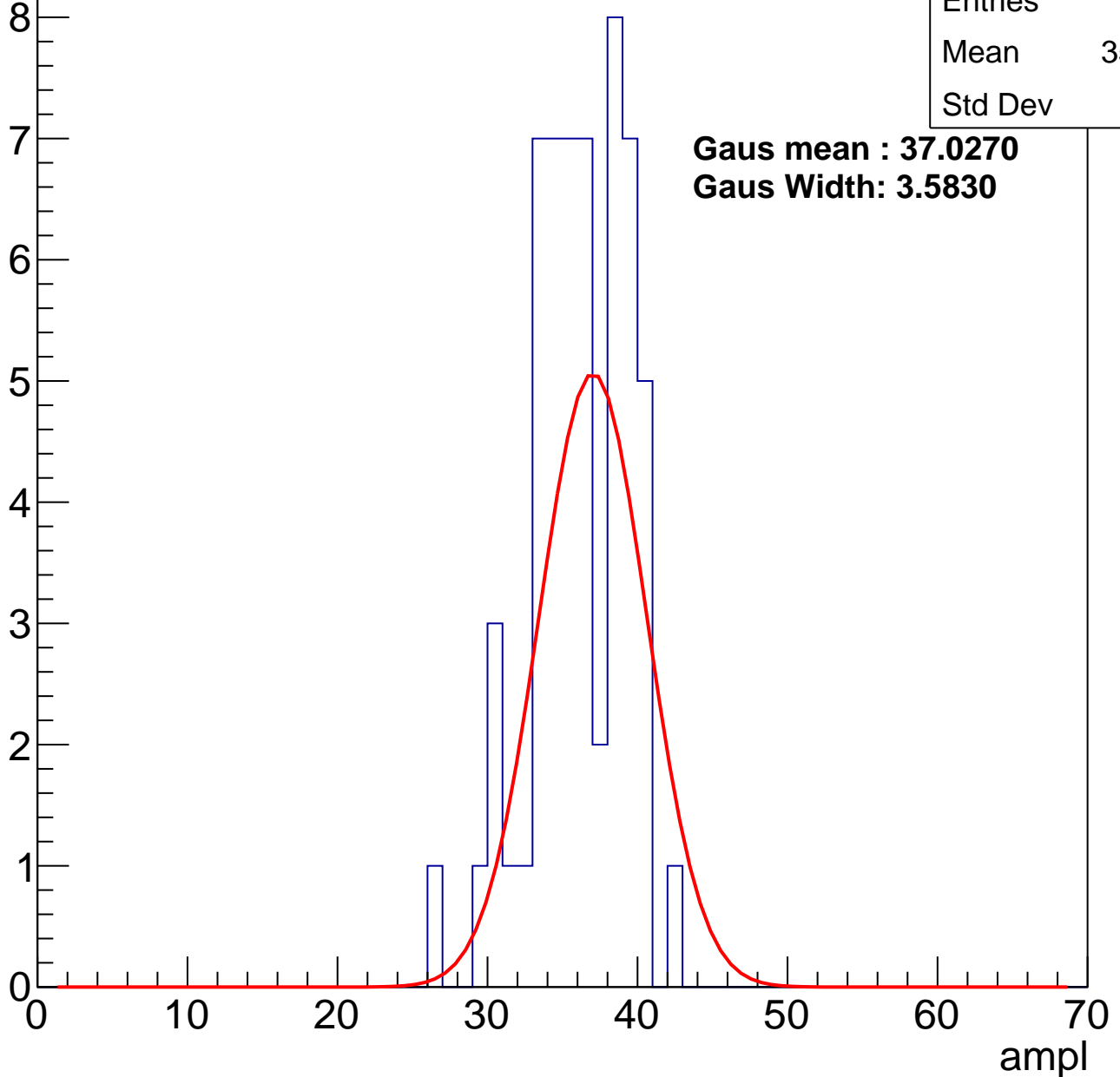
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	35.64
Std Dev	3.22

**Gaus mean : 37.0270**

**Gaus Width: 3.5830**



# B1L101S, U16-ch82, adc2

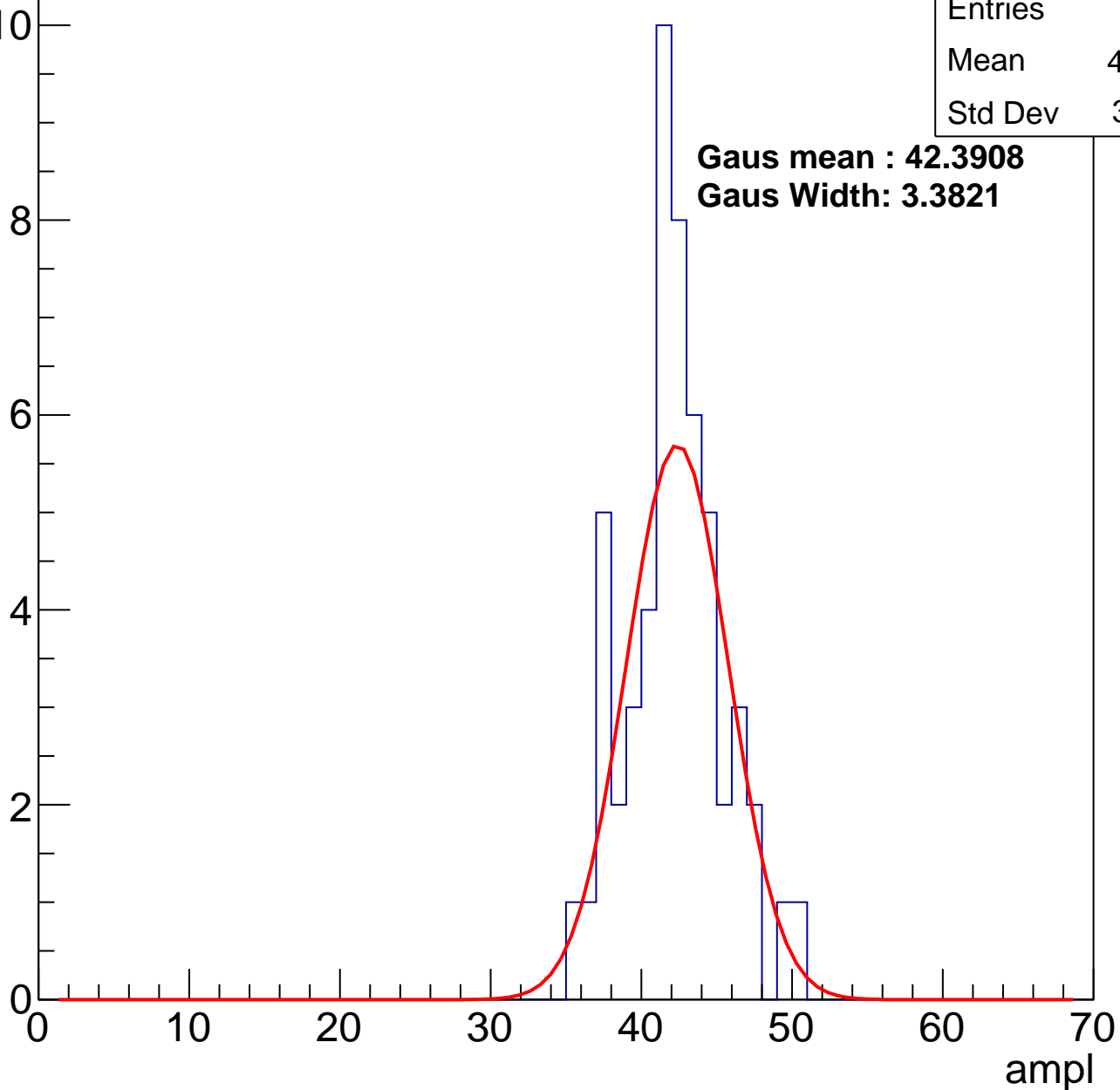
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	41.74
Std Dev	3.181

**Gaus mean : 42.3908**

**Gaus Width: 3.3821**



# B1L101S, U16-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	77
Mean	48.14
Std Dev	3.329

Entry

10

8

6

4

2

0

0

10

20

30

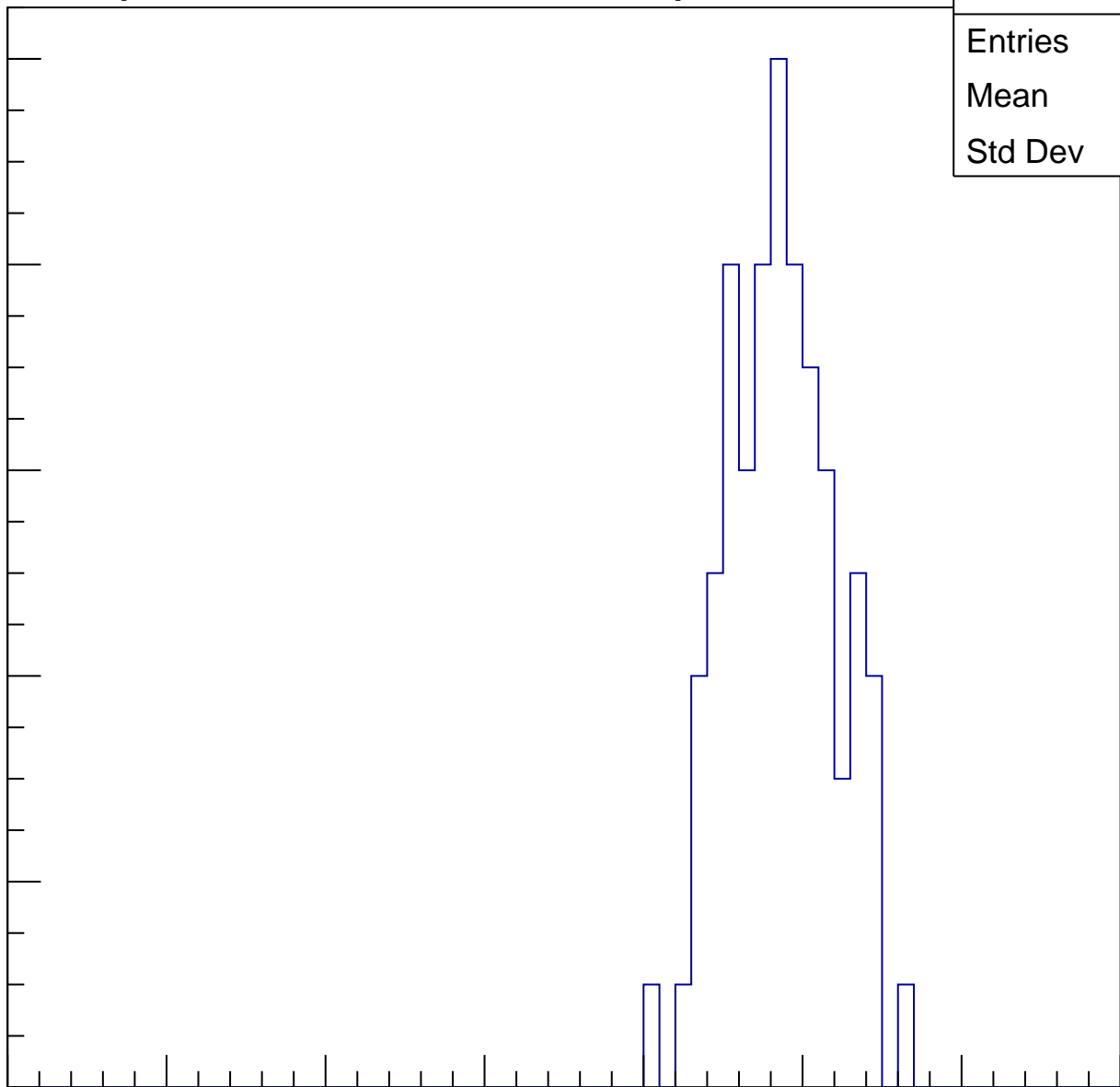
40

50

60

70

ampl



# B1L101S, U16-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

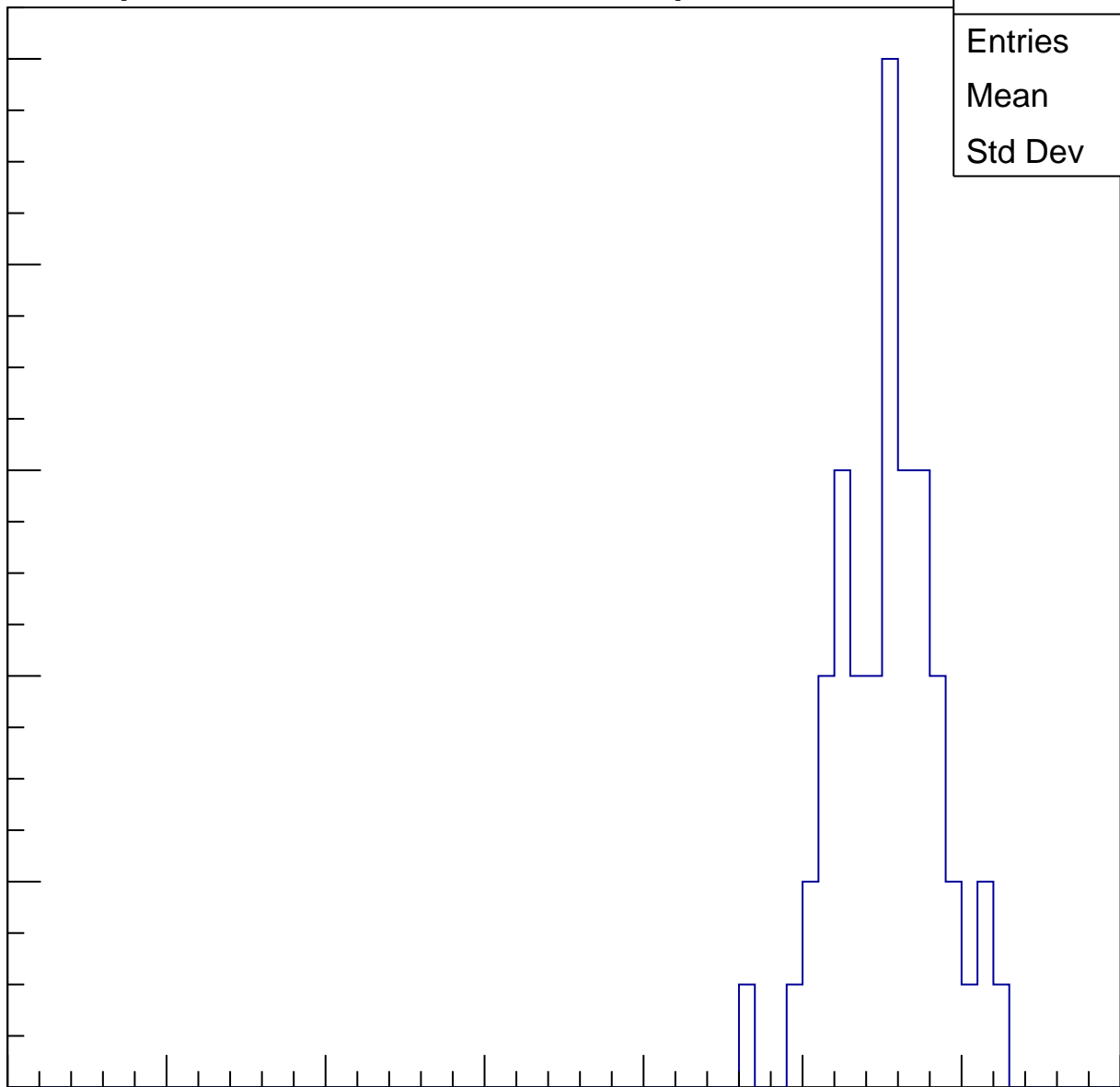
Entries	54
Mean	54.83
Std Dev	3.184

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

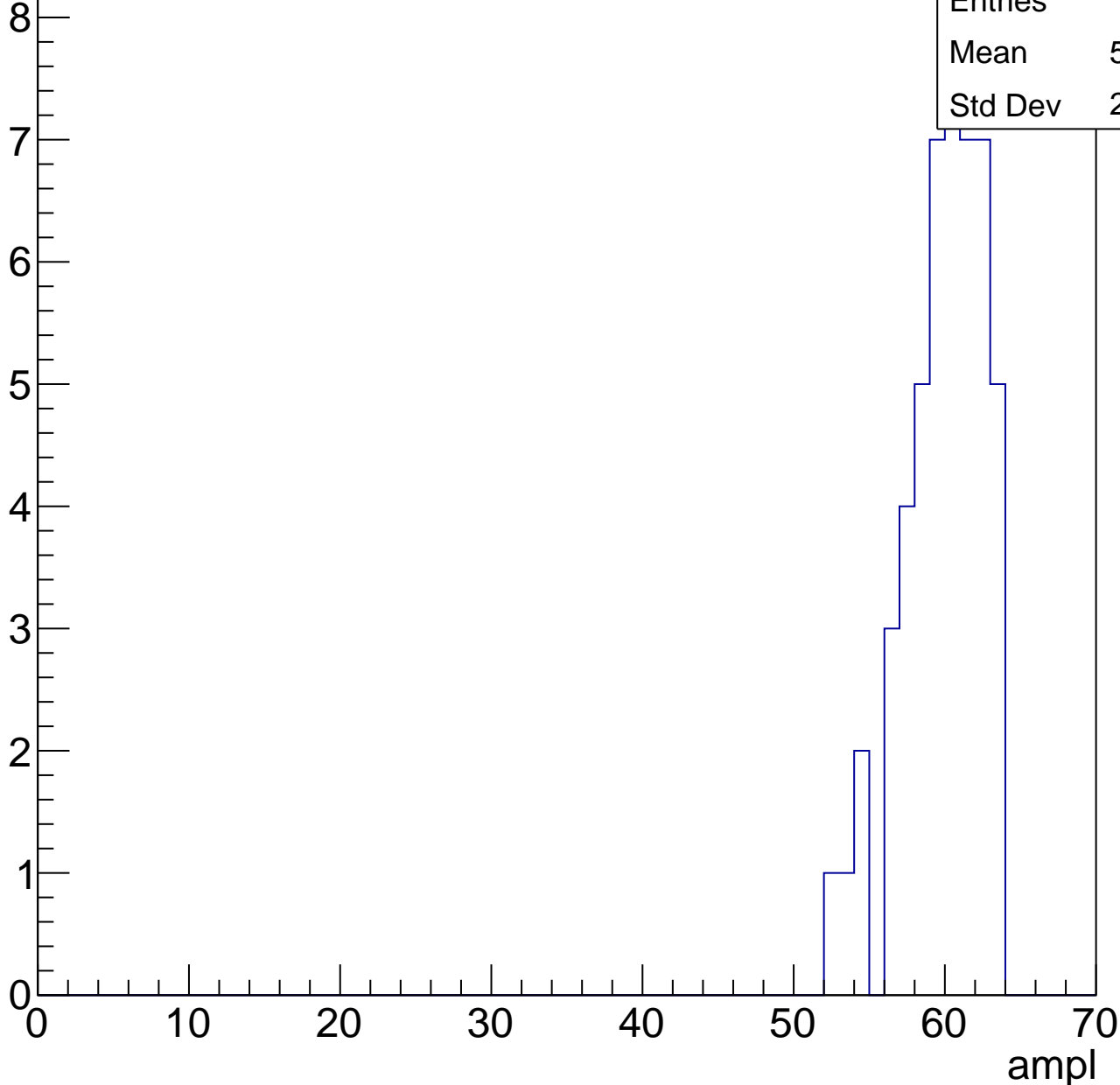


# B1L101S, U16-ch82, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	59.36
Std Dev	2.667

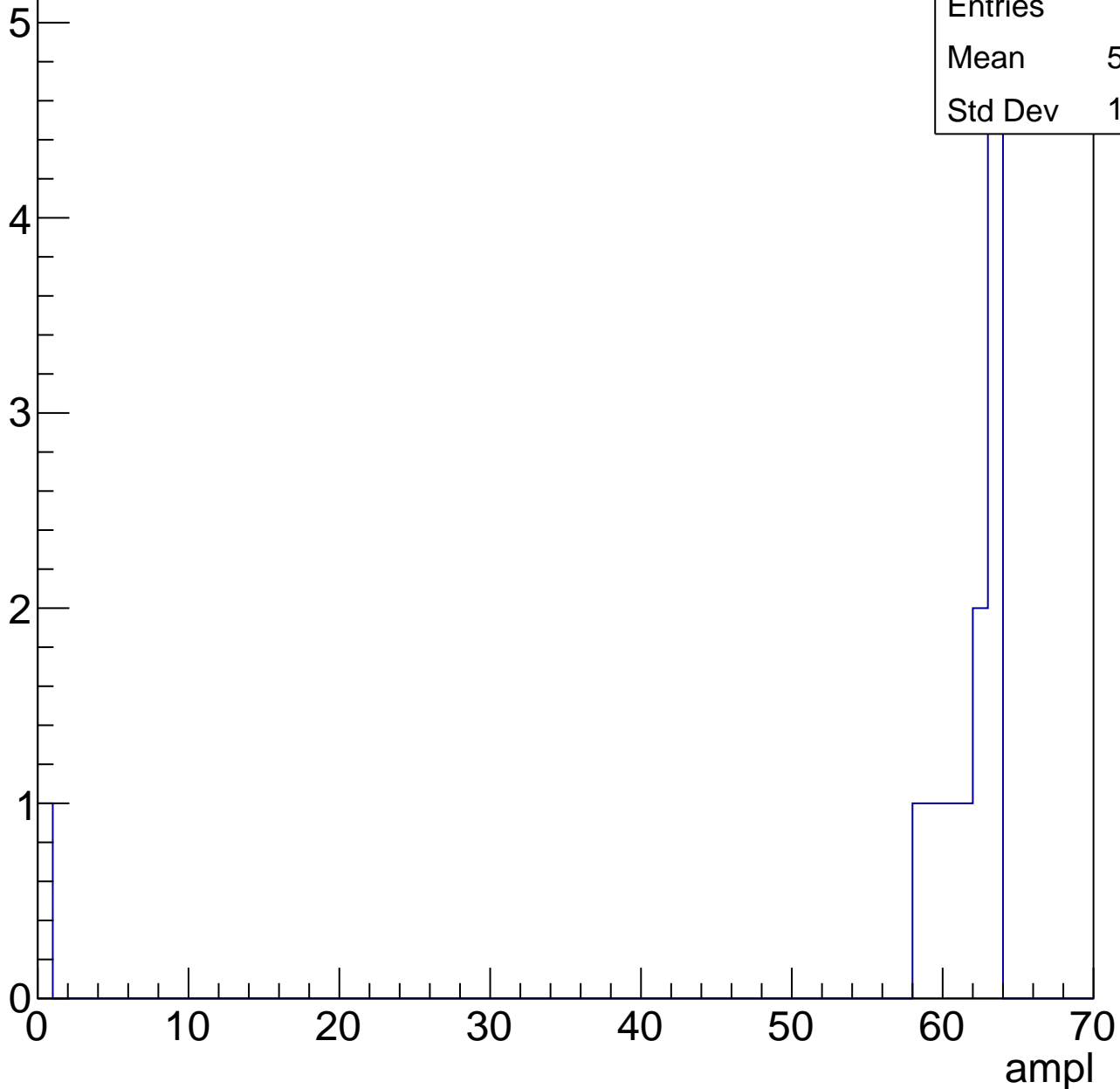


# B1L101S, U16-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	12
Mean	56.42
Std Dev	17.09

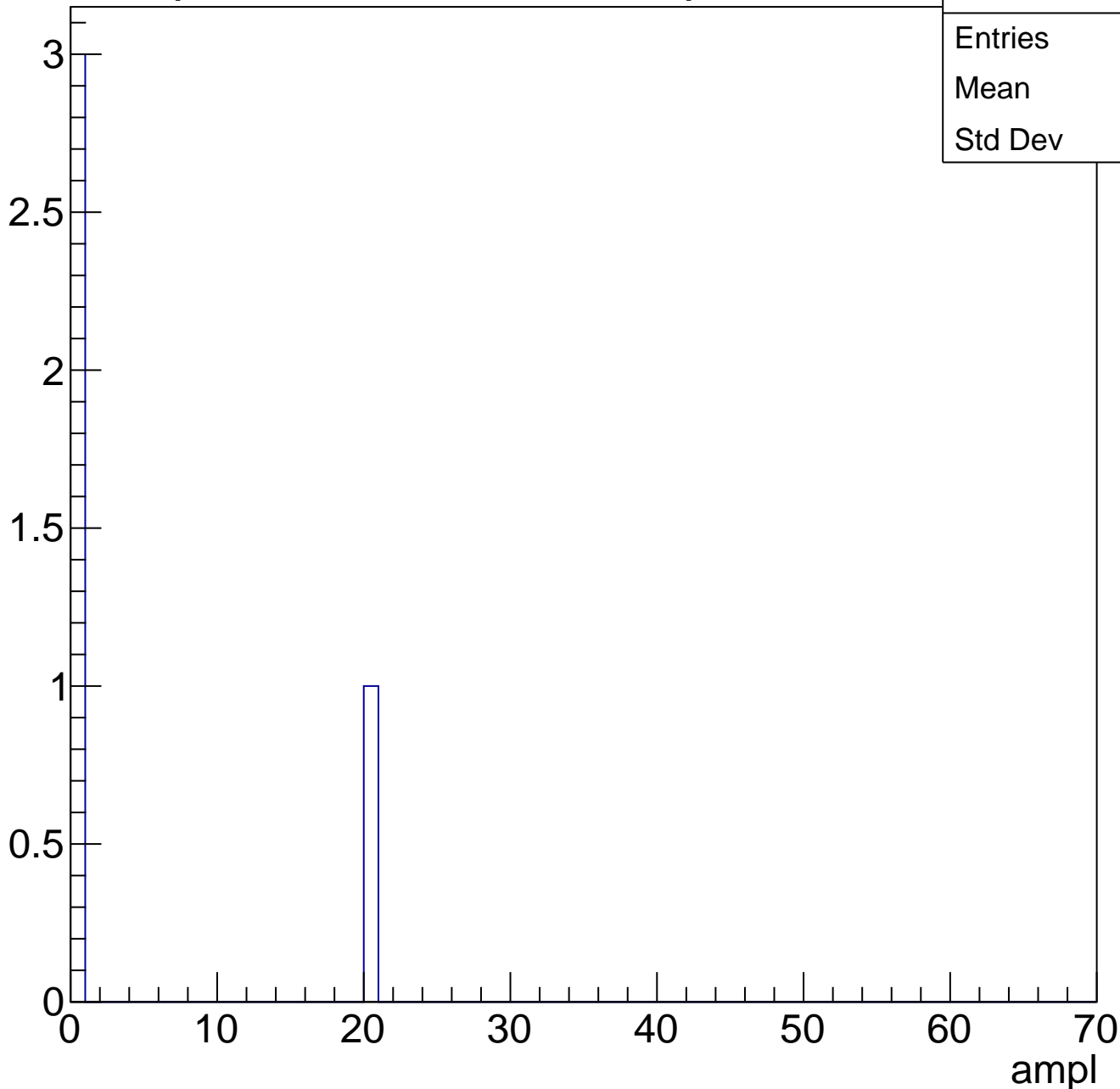




# B1L101S, U16-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	4
Mean	5
Std Dev	8.66

# B1L101S, U16-ch83, adc0

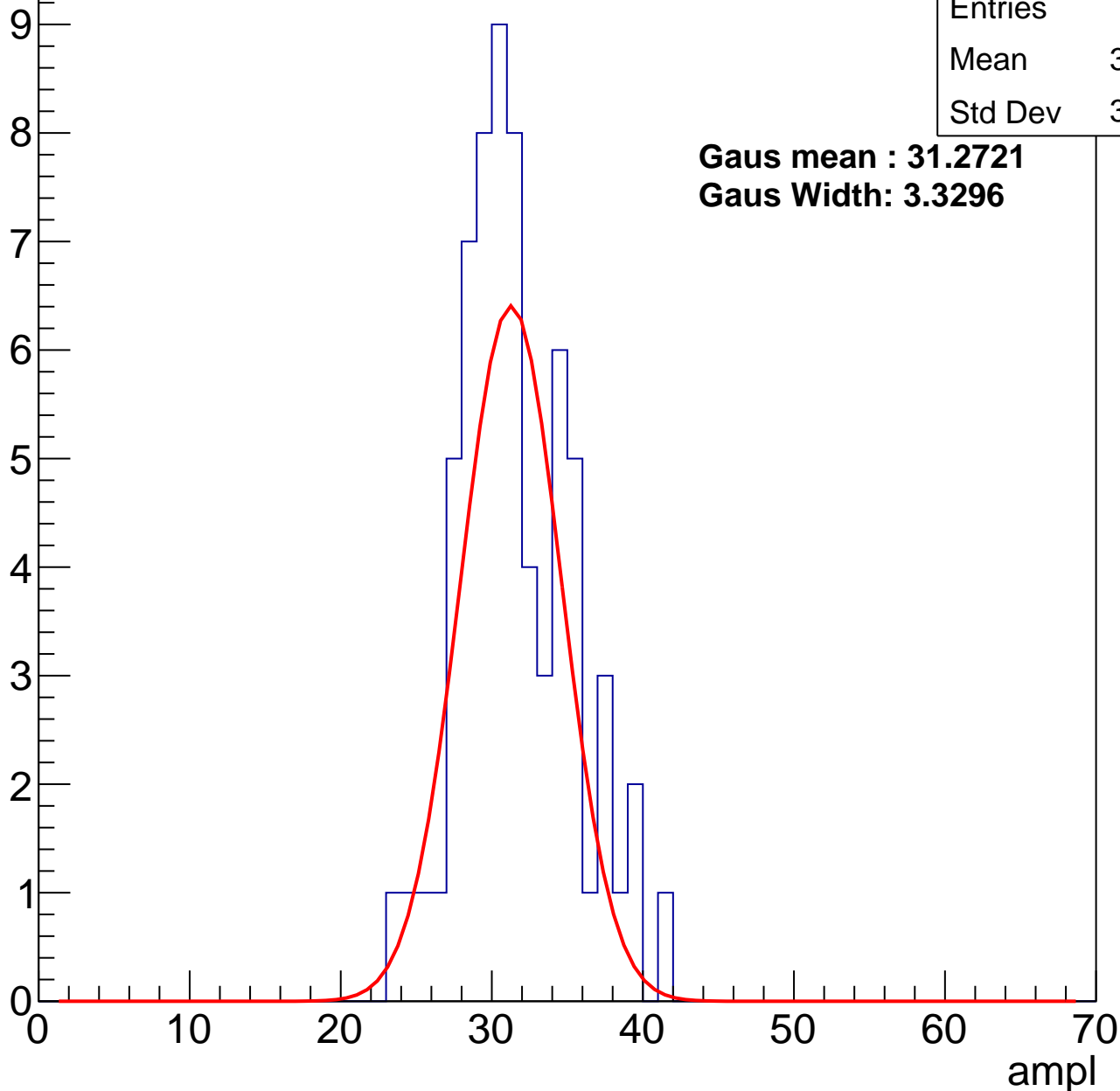
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	31.18
Std Dev	3.697

**Gaus mean : 31.2721**

**Gaus Width: 3.3296**



# B1L101S, U16-ch83, adc1

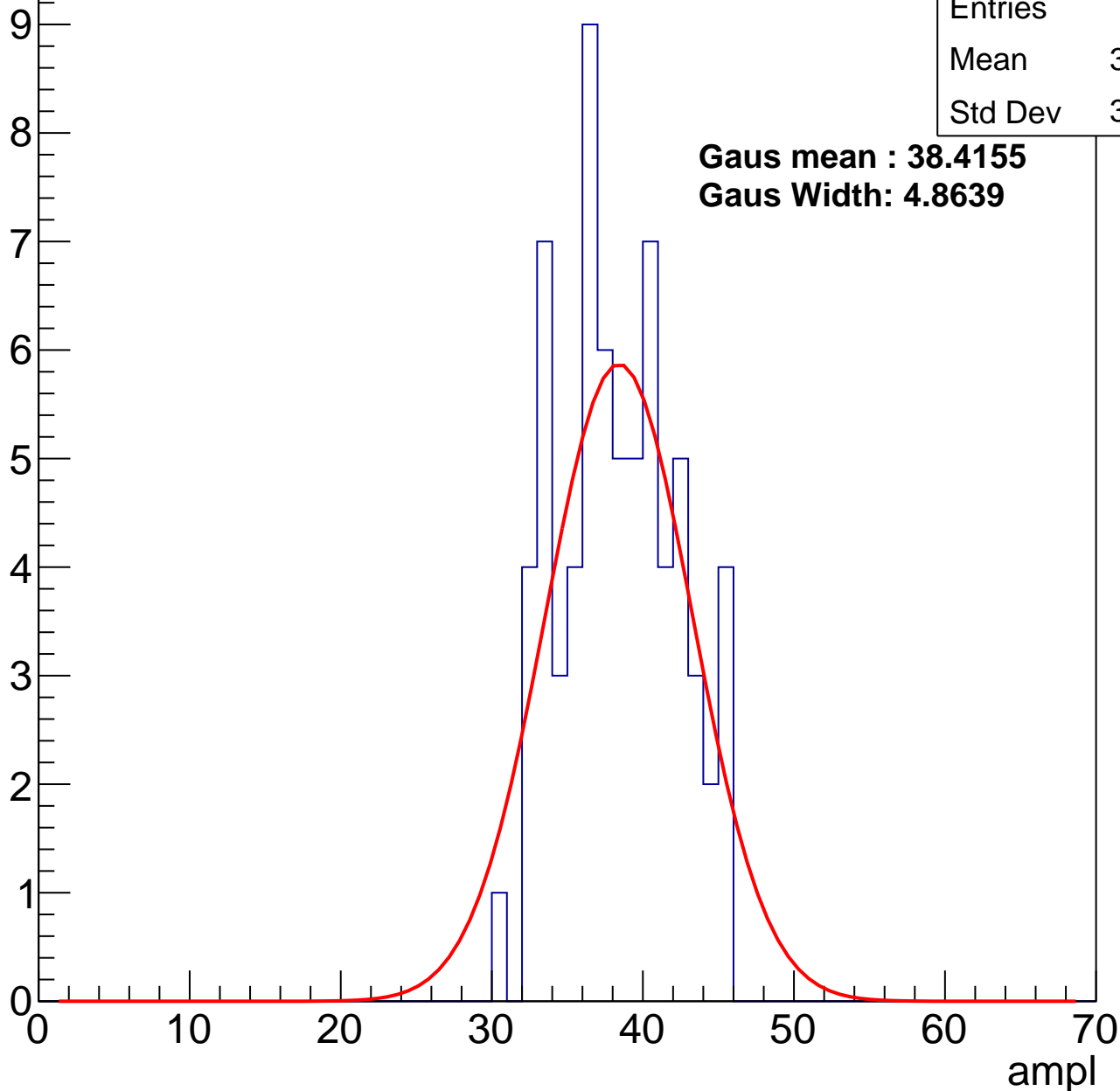
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	37.87
Std Dev	3.807

**Gaus mean : 38.4155**

**Gaus Width: 4.8639**



# B1L101S, U16-ch83, adc2

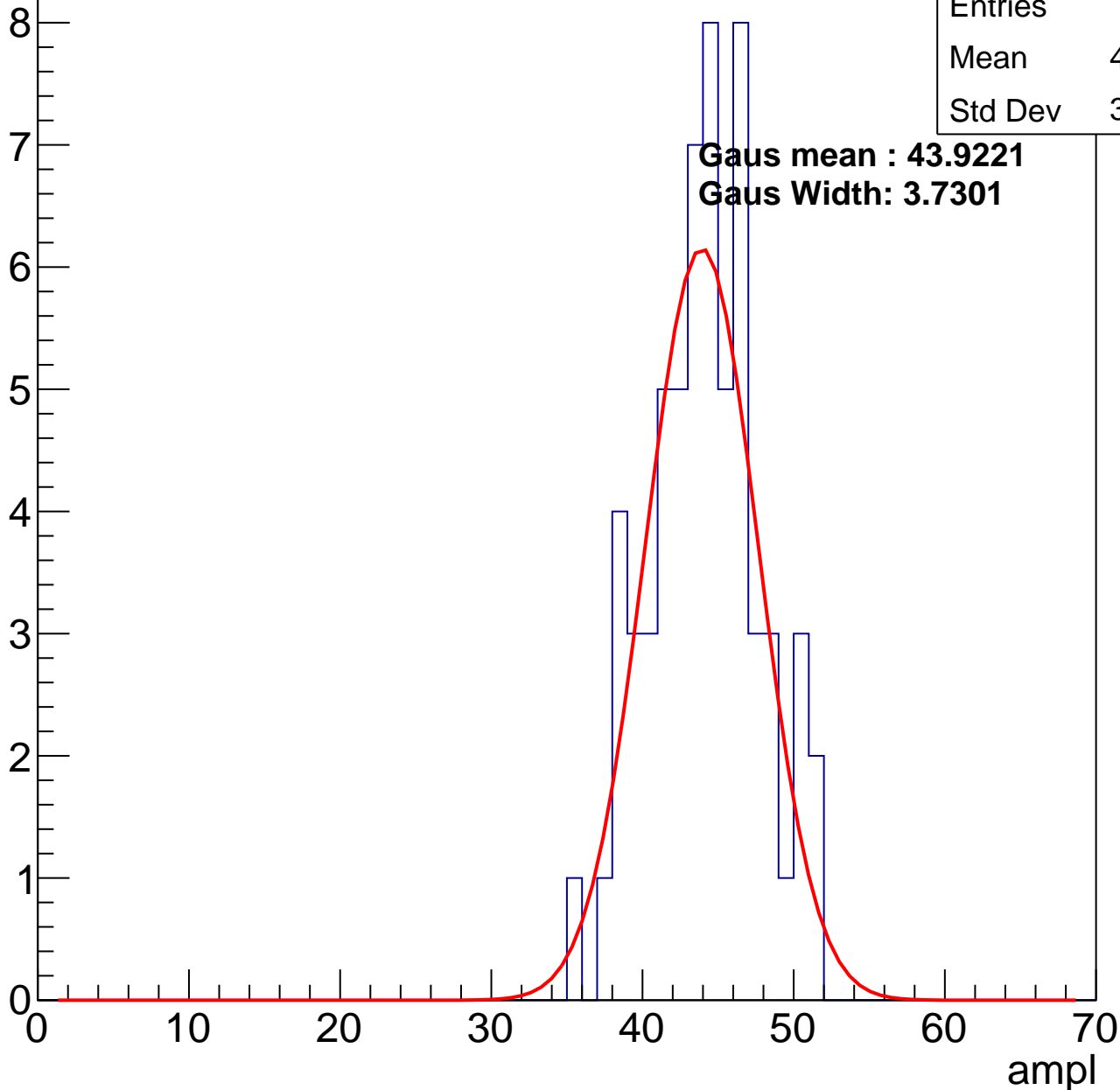
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	43.68
Std Dev	3.605

**Gaus mean : 43.9221**

**Gaus Width: 3.7301**

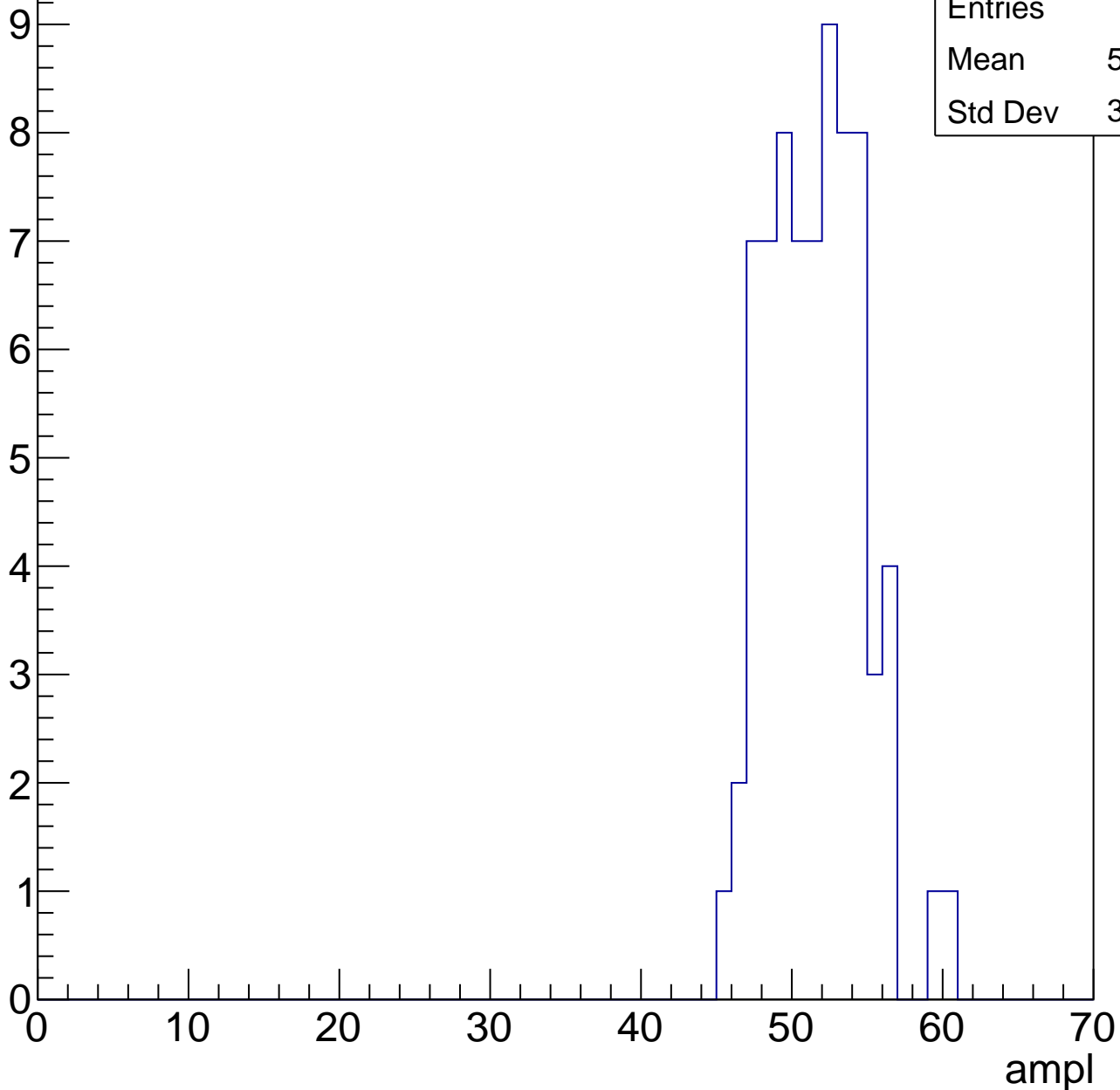


# B1L101S, U16-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	51.14
Std Dev	3.107

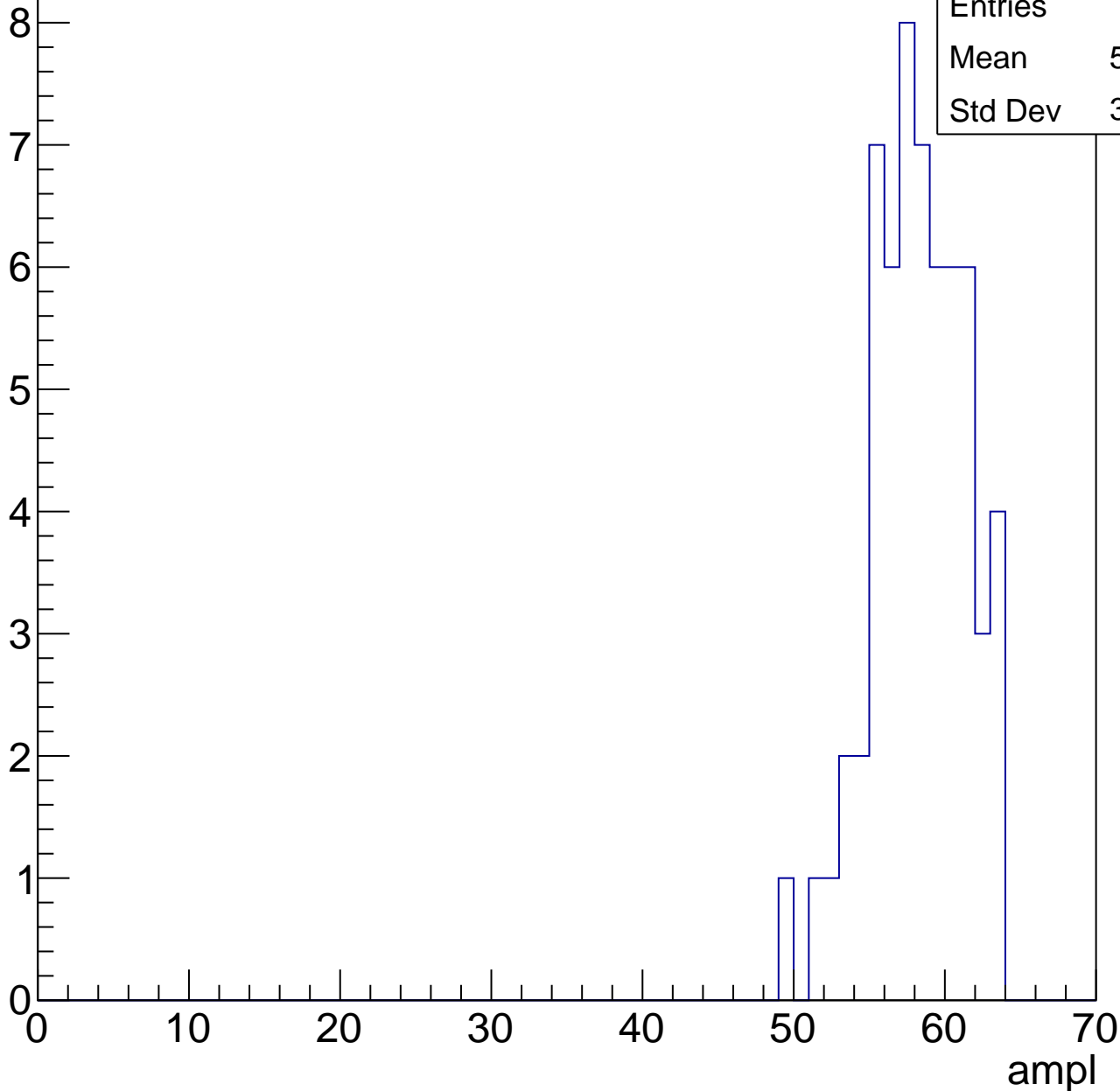


# B1L101S, U16-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	57.78
Std Dev	3.088

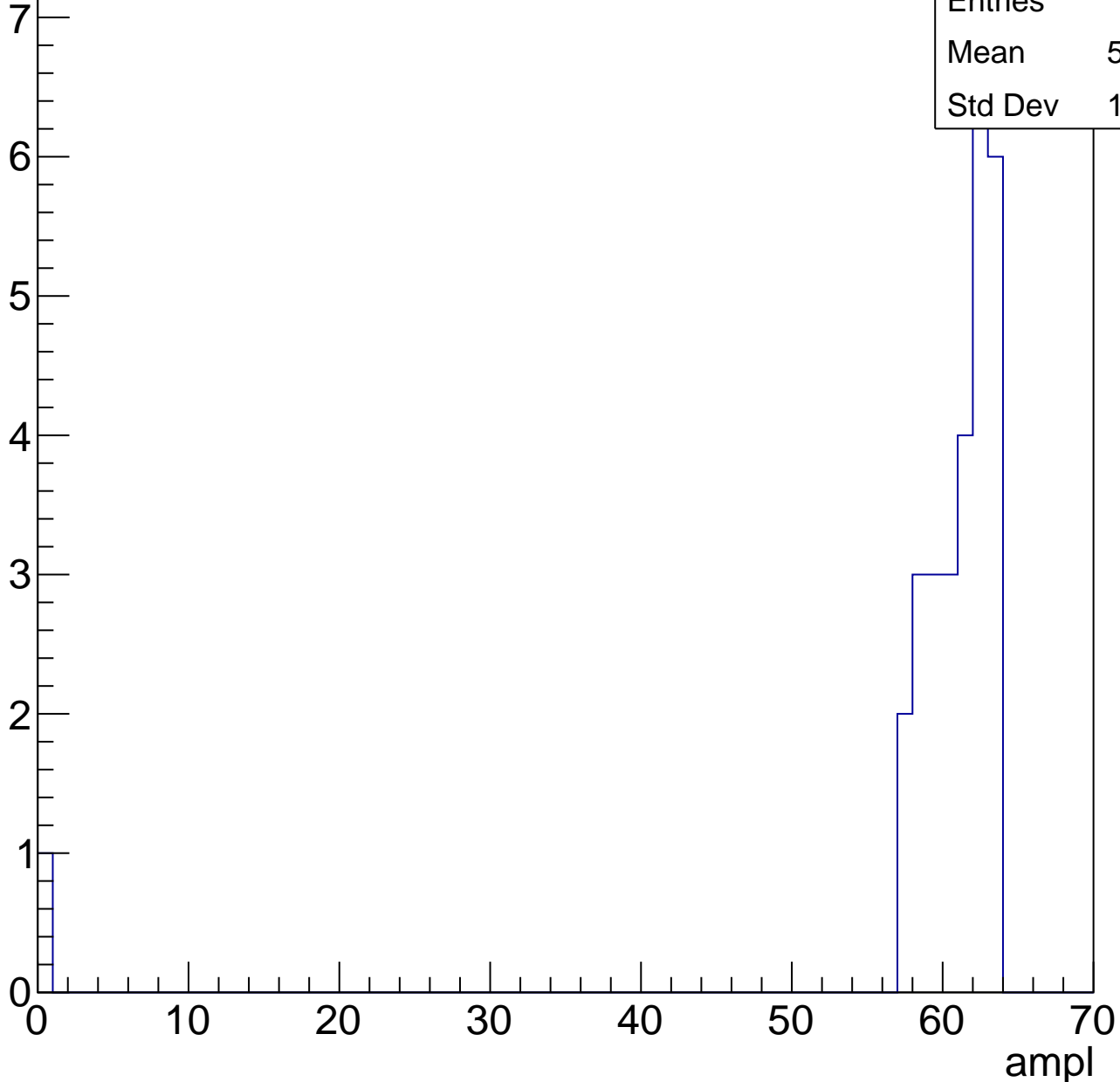


# B1L101S, U16-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	29
Mean	58.66
Std Dev	11.24



# B1L101S, U16-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L101S, U16-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U16-ch84, adc0

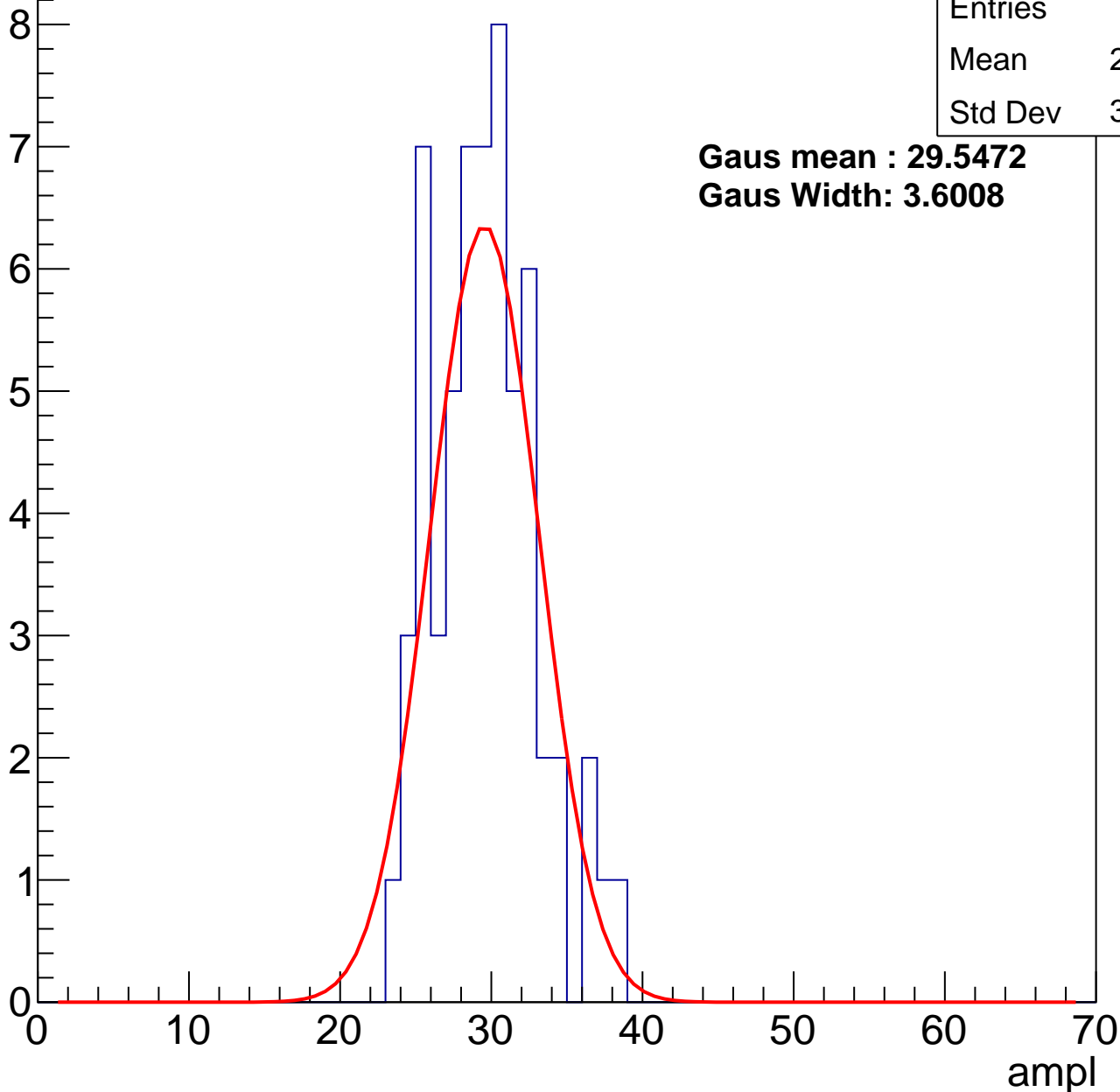
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	29.17
Std Dev	3.372

**Gaus mean : 29.5472**

**Gaus Width: 3.6008**



# B1L101S, U16-ch84, adc1

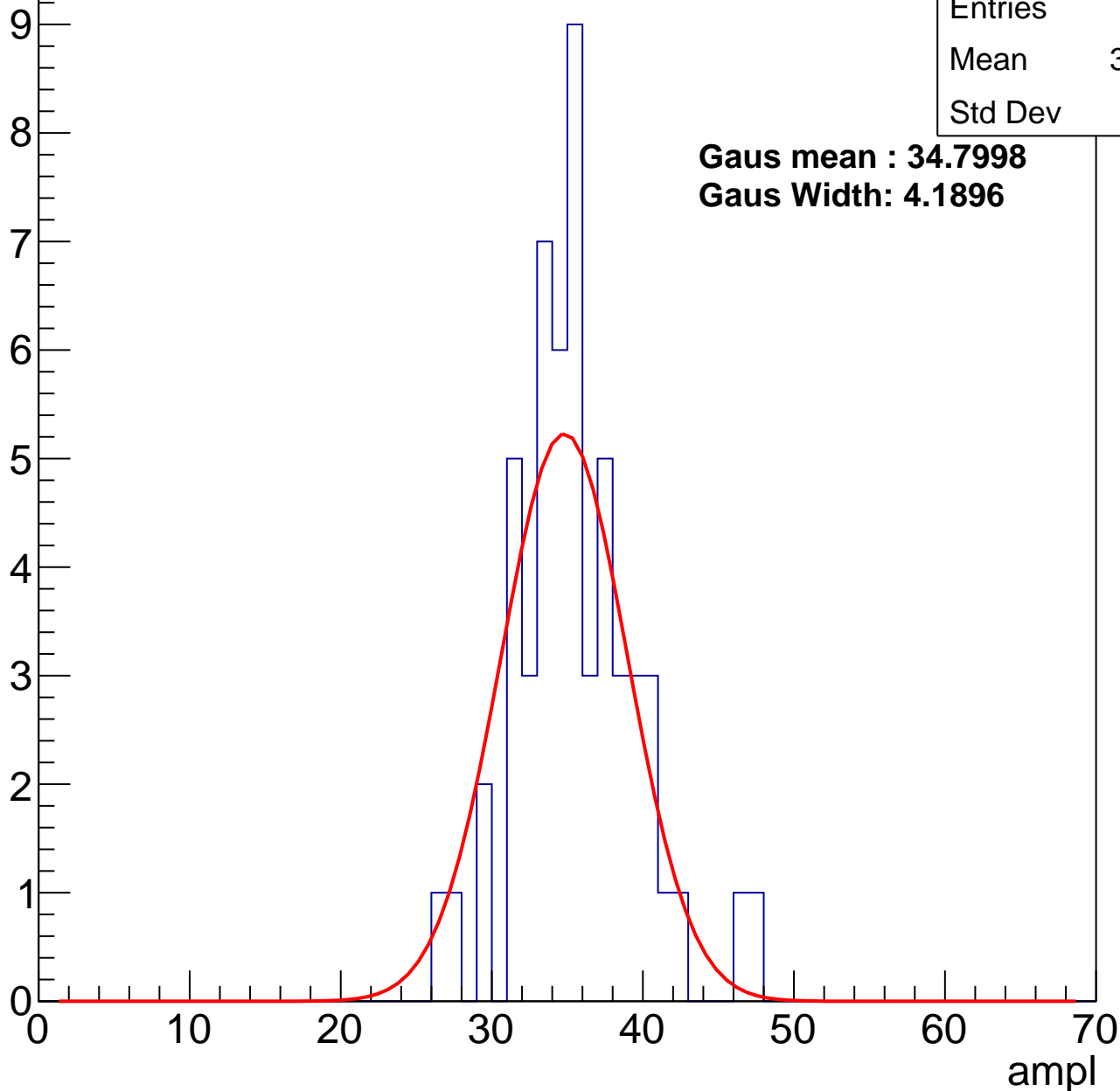
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	35.13
Std Dev	4

**Gaus mean : 34.7998**

**Gaus Width: 4.1896**



# B1L101S, U16-ch84, adc2

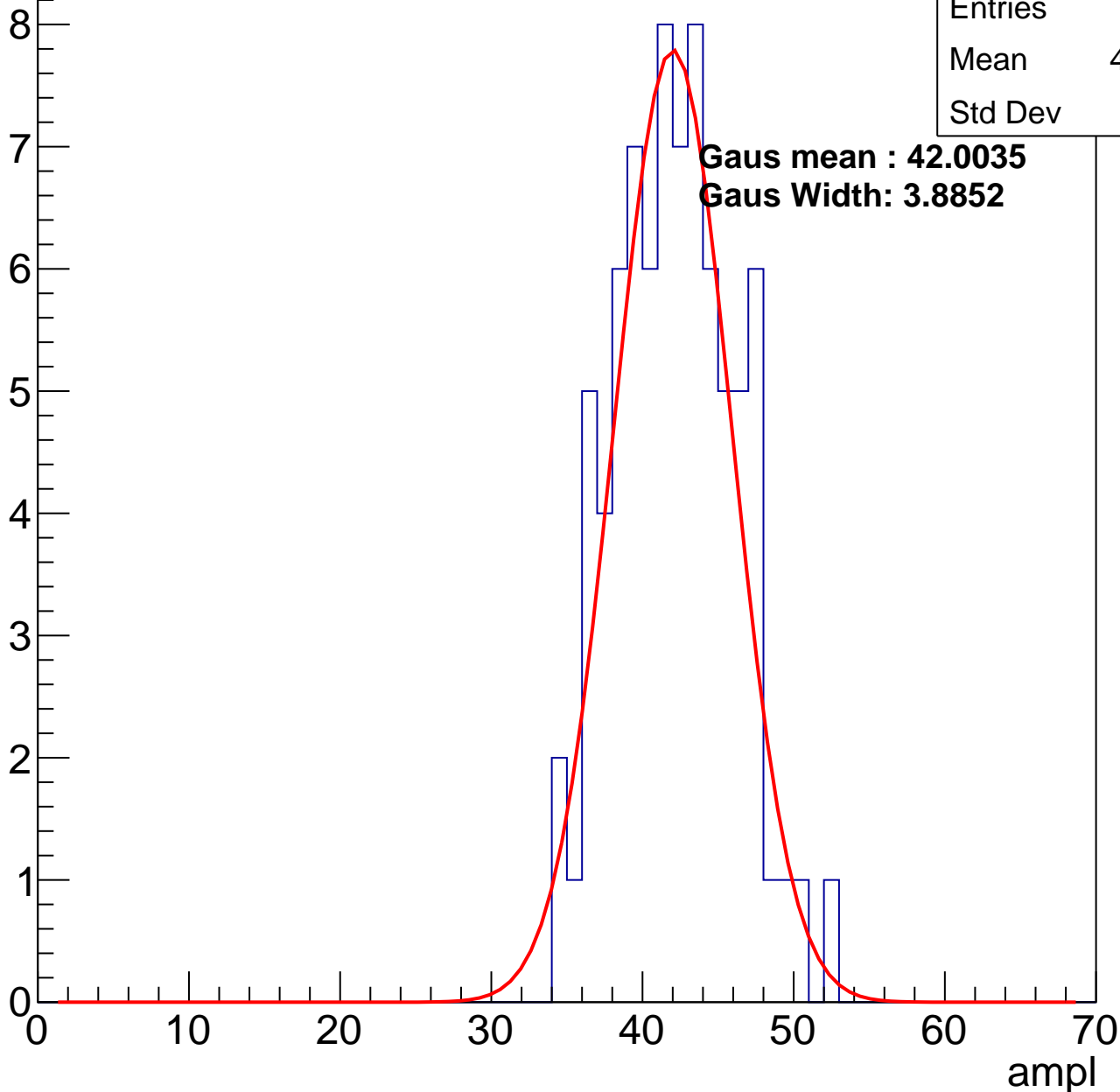
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	41.73
Std Dev	3.87

**Gaus mean : 42.0035**

**Gaus Width: 3.8852**

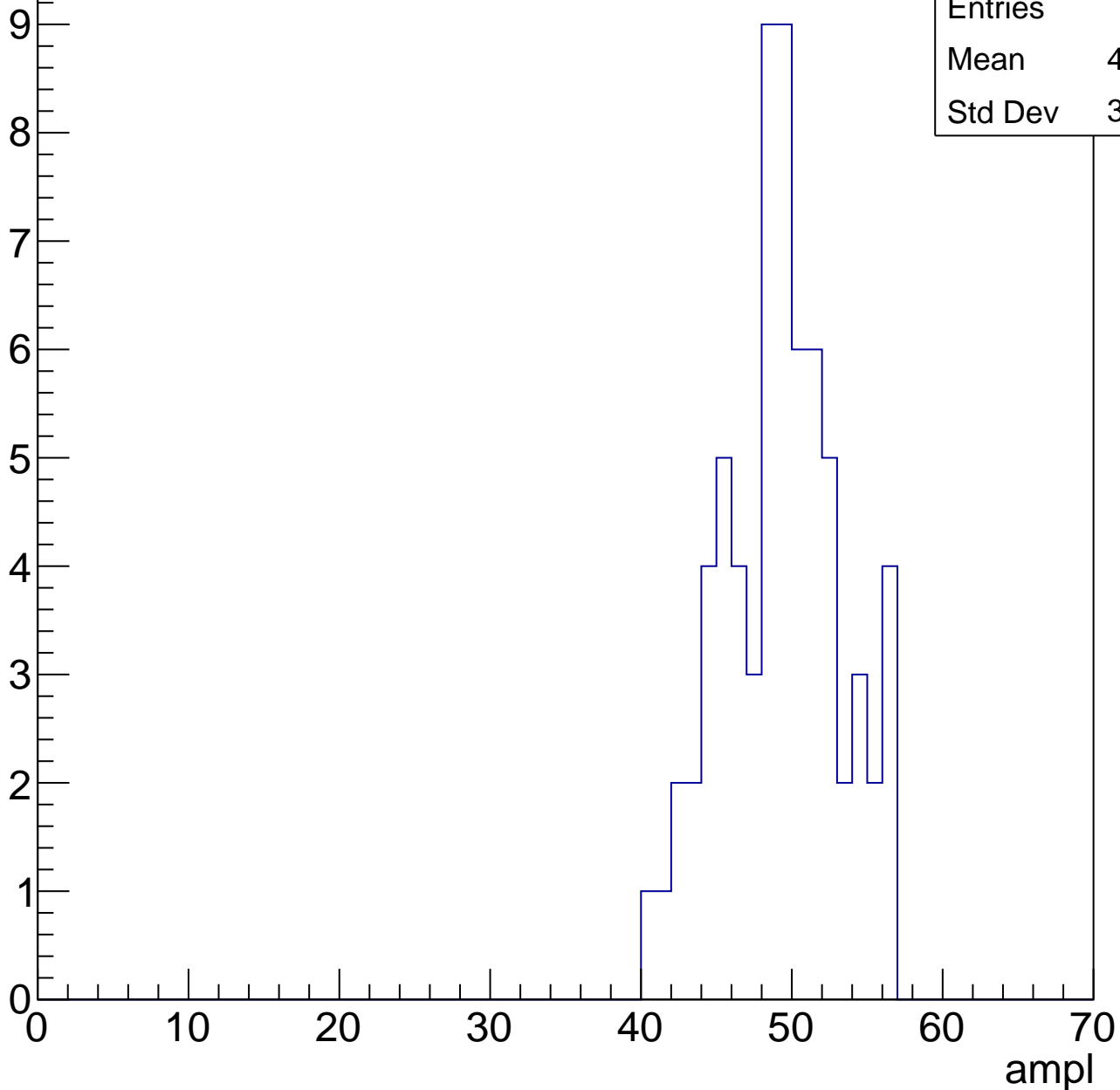


# B1L101S, U16-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	48.79
Std Dev	3.833

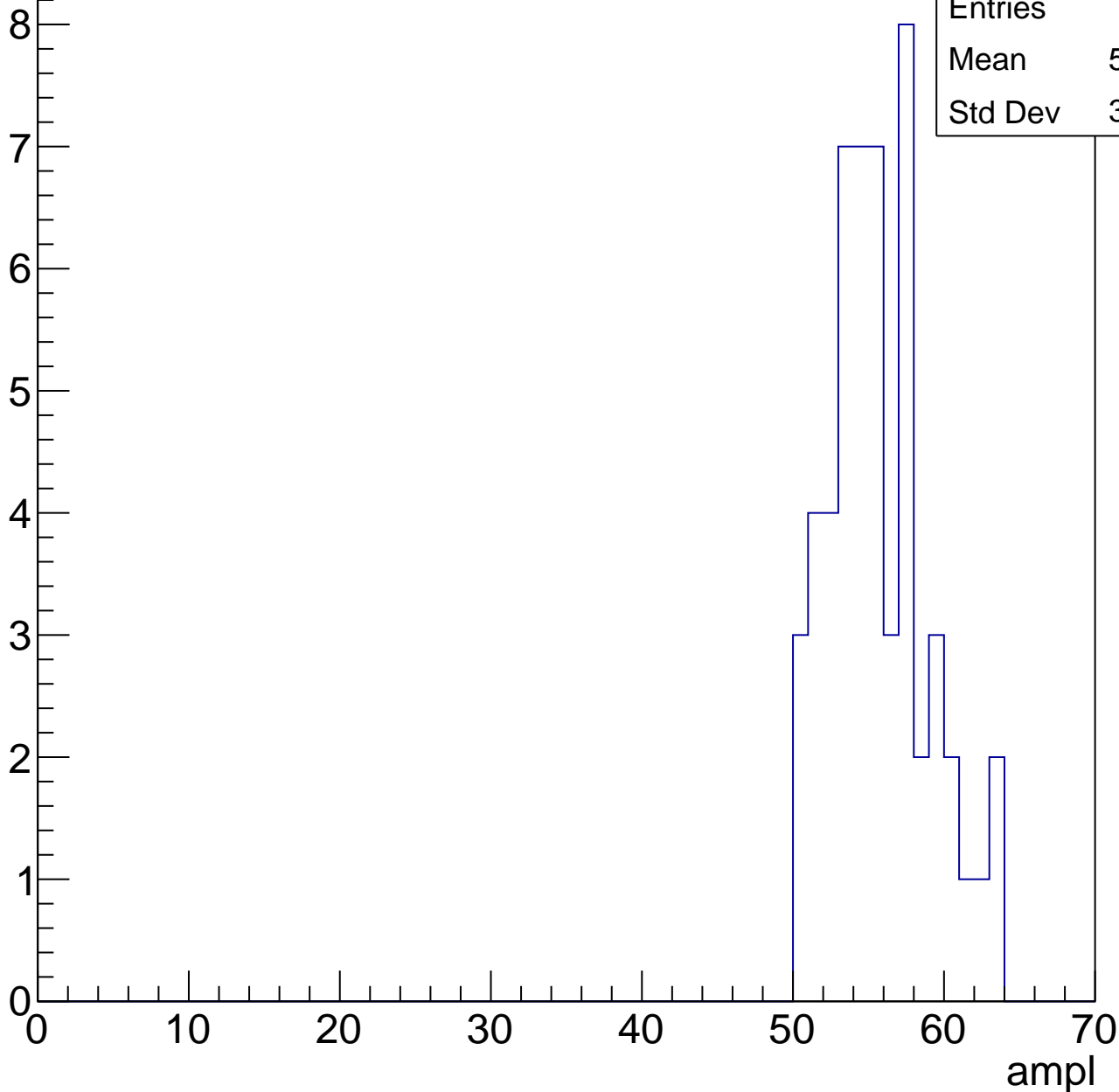


# B1L101S, U16-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	55.22
Std Dev	3.253

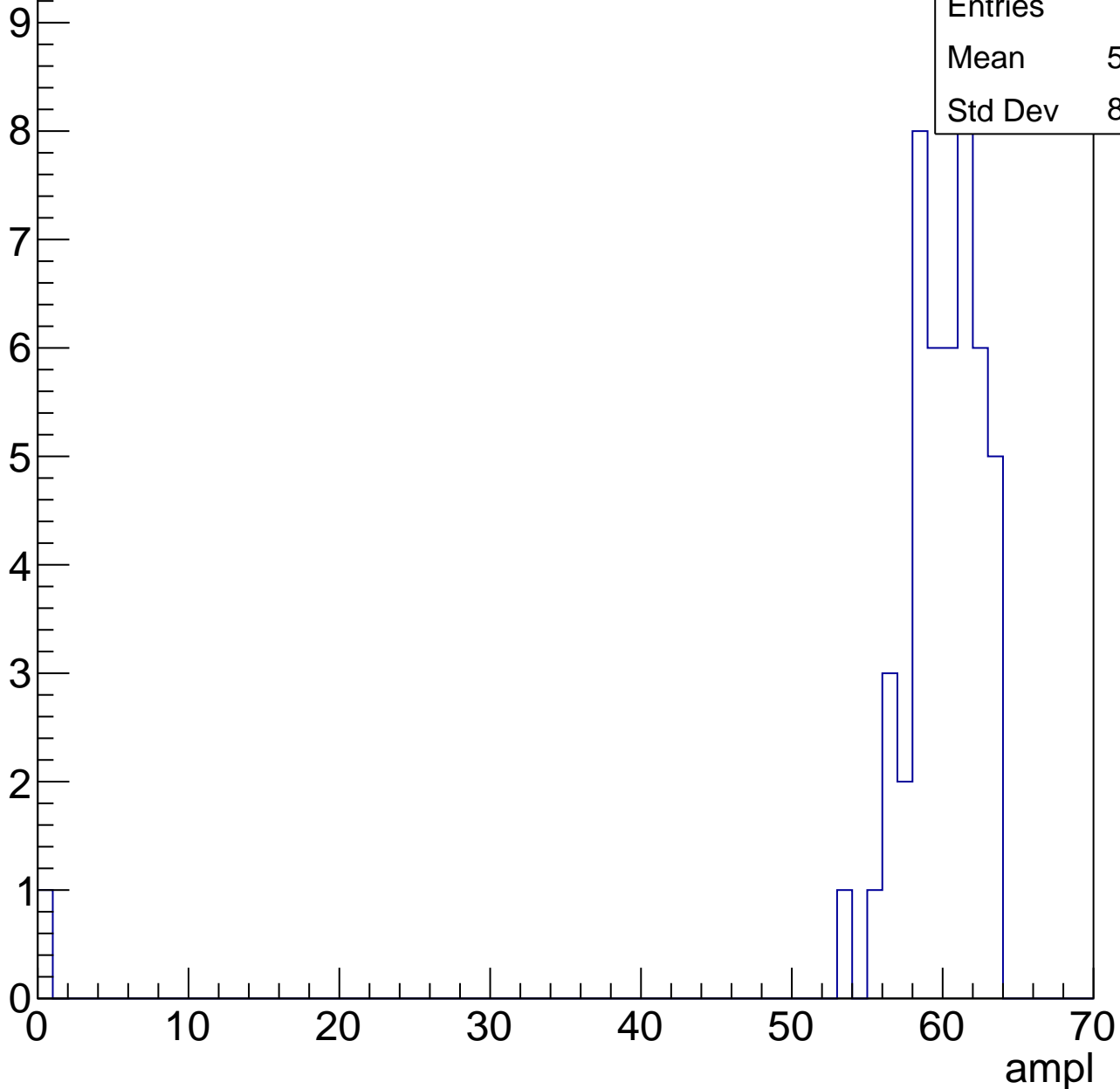


# B1L101S, U16-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

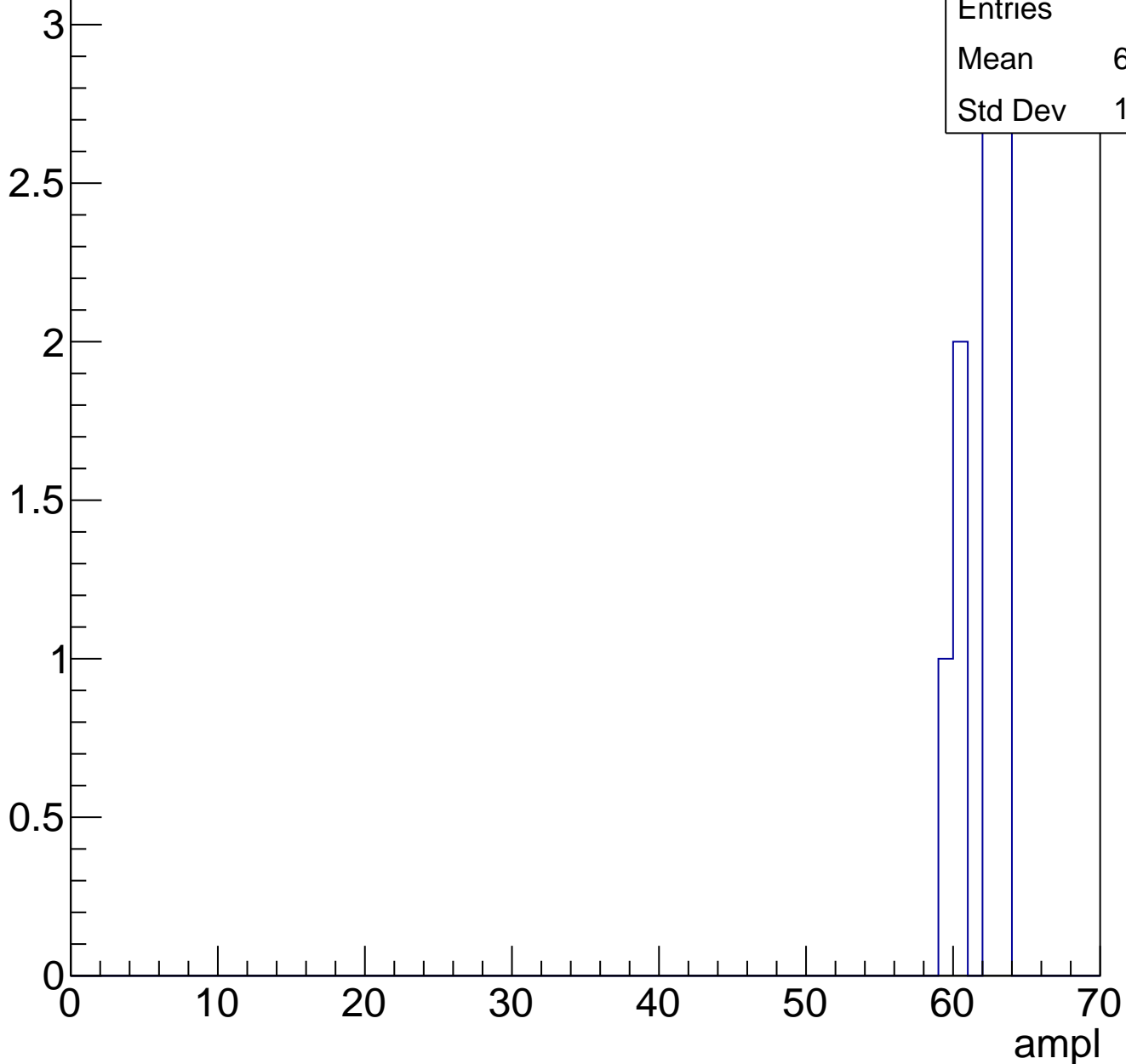
Entries	48
Mean	58.42
Std Dev	8.822



# B1L101S, U16-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U16-ch85, adc0

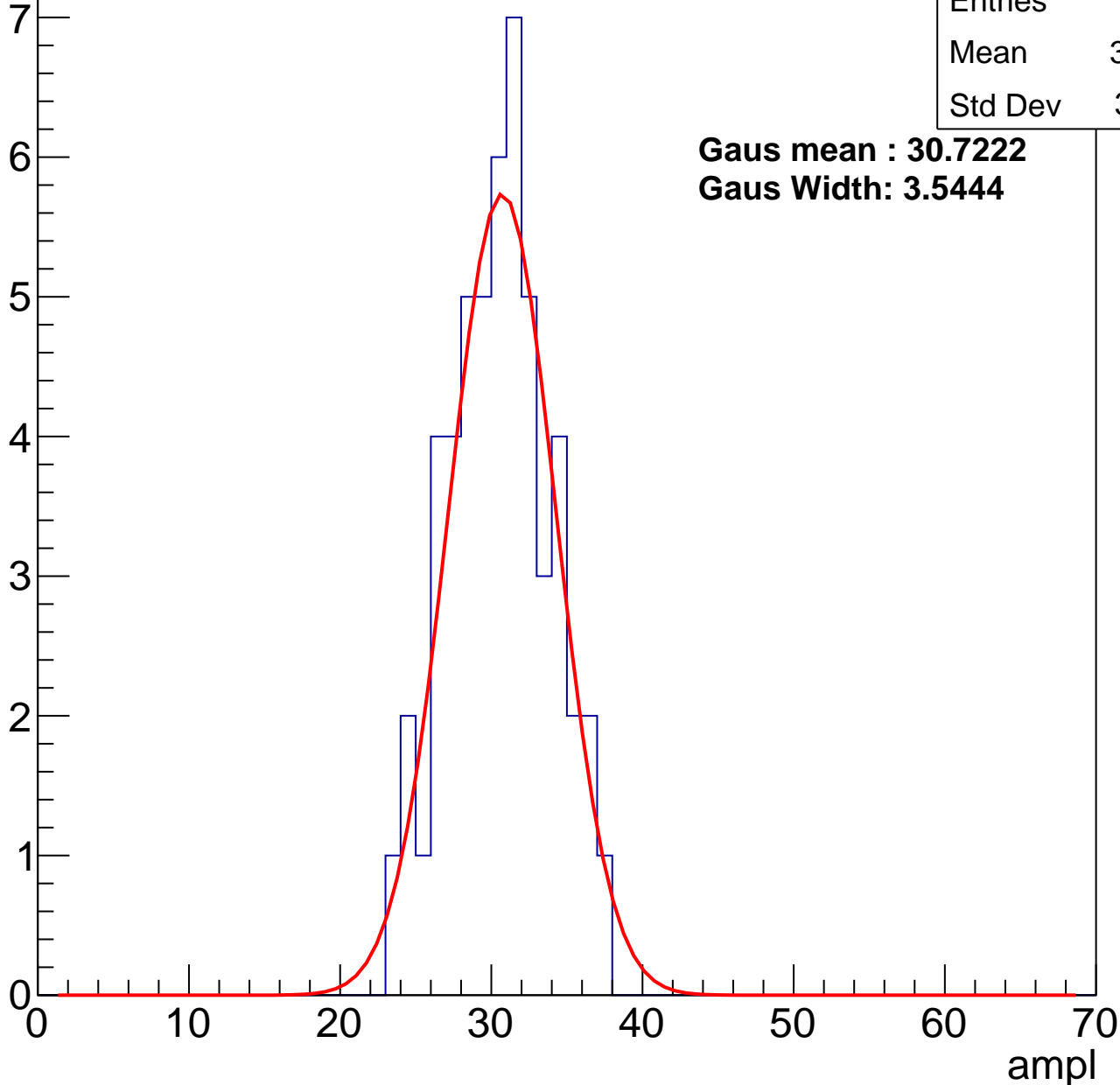
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	30.08
Std Dev	3.281

**Gaus mean : 30.7222**

**Gaus Width: 3.5444**



# B1L101S, U16-ch85, adc1

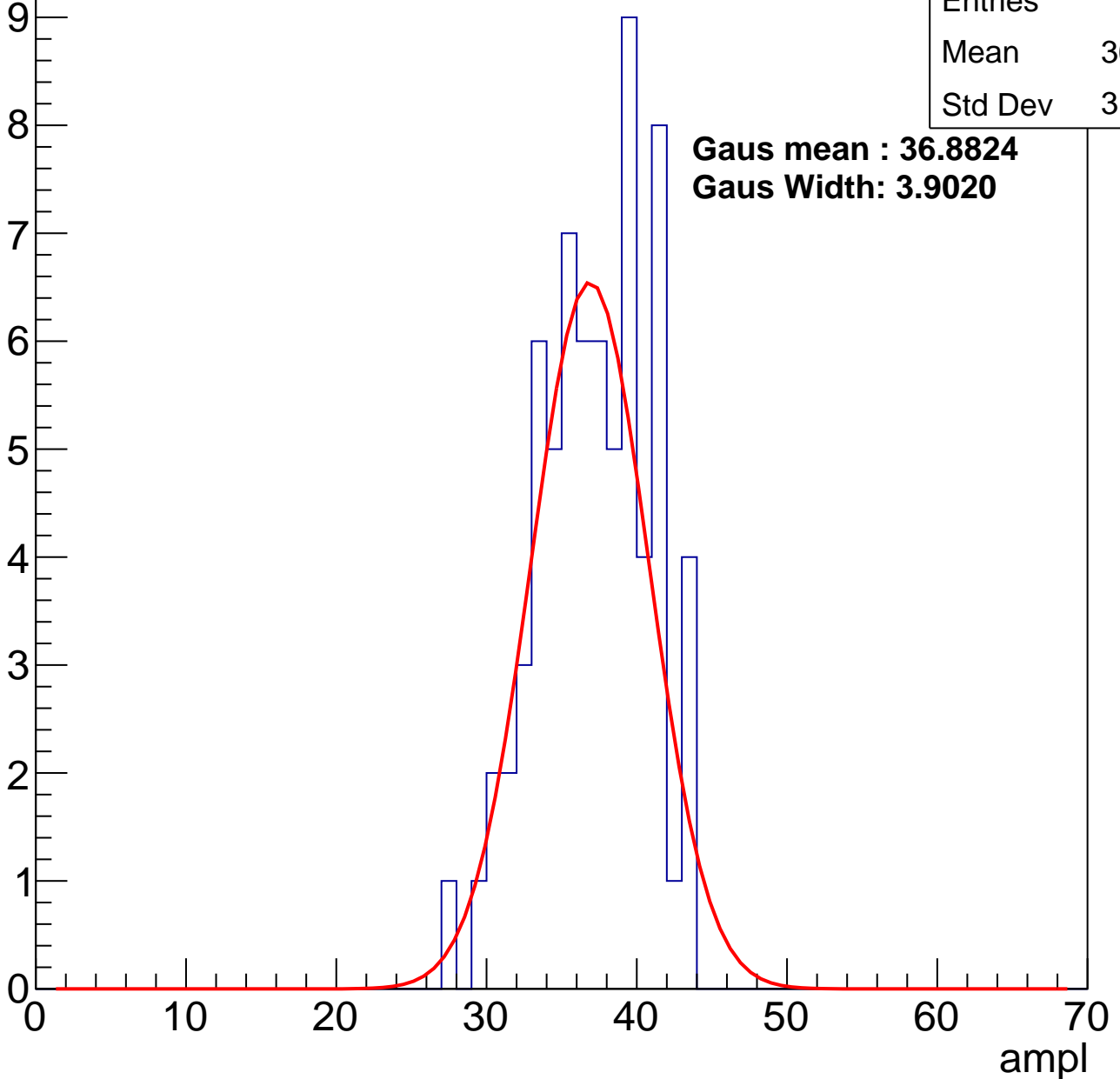
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	36.69
Std Dev	3.686

**Gaus mean : 36.8824**

**Gaus Width: 3.9020**



# B1L101S, U16-ch85, adc2

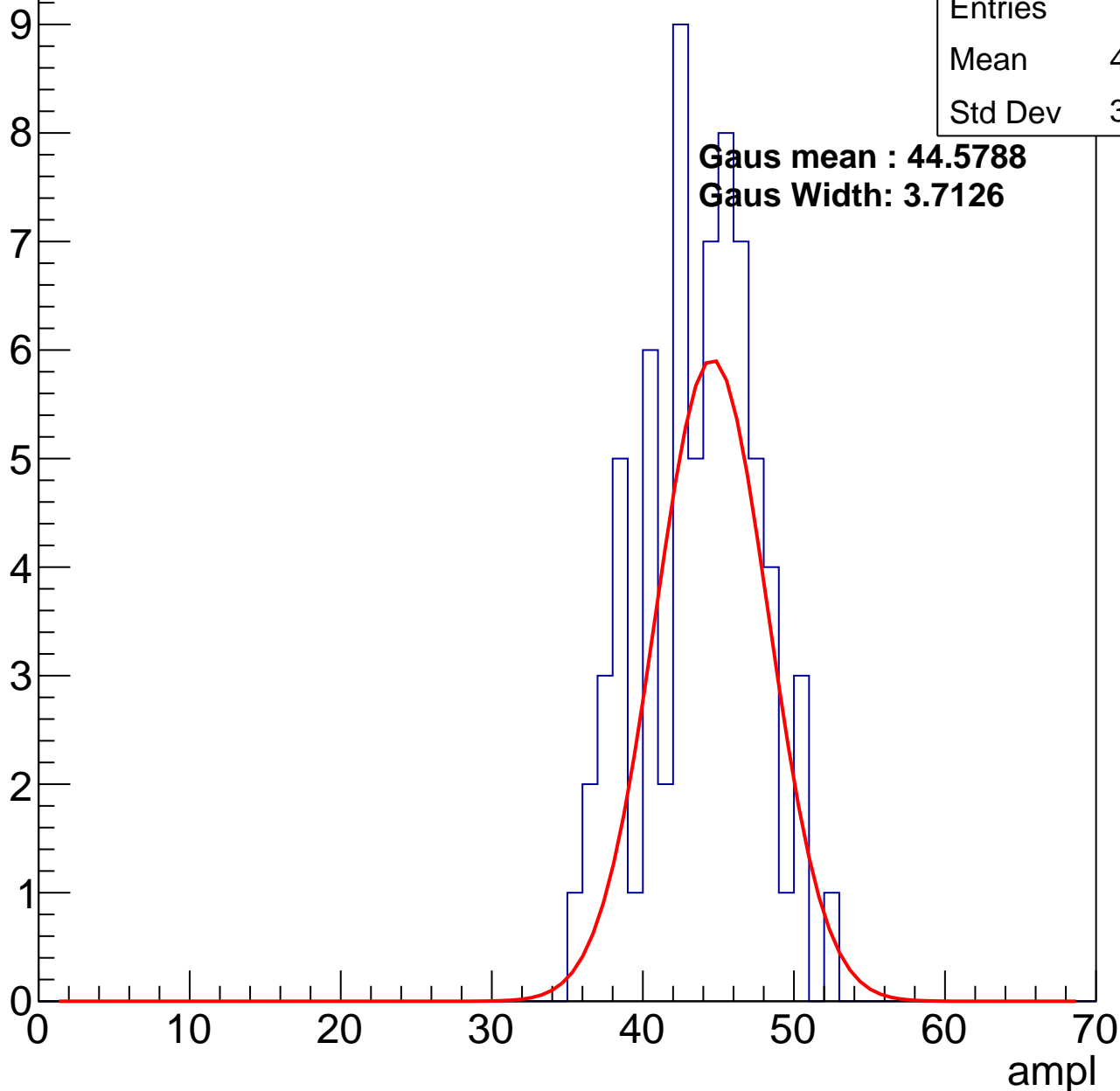
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	43.29
Std Dev	3.822

**Gaus mean : 44.5788**

**Gaus Width: 3.7126**

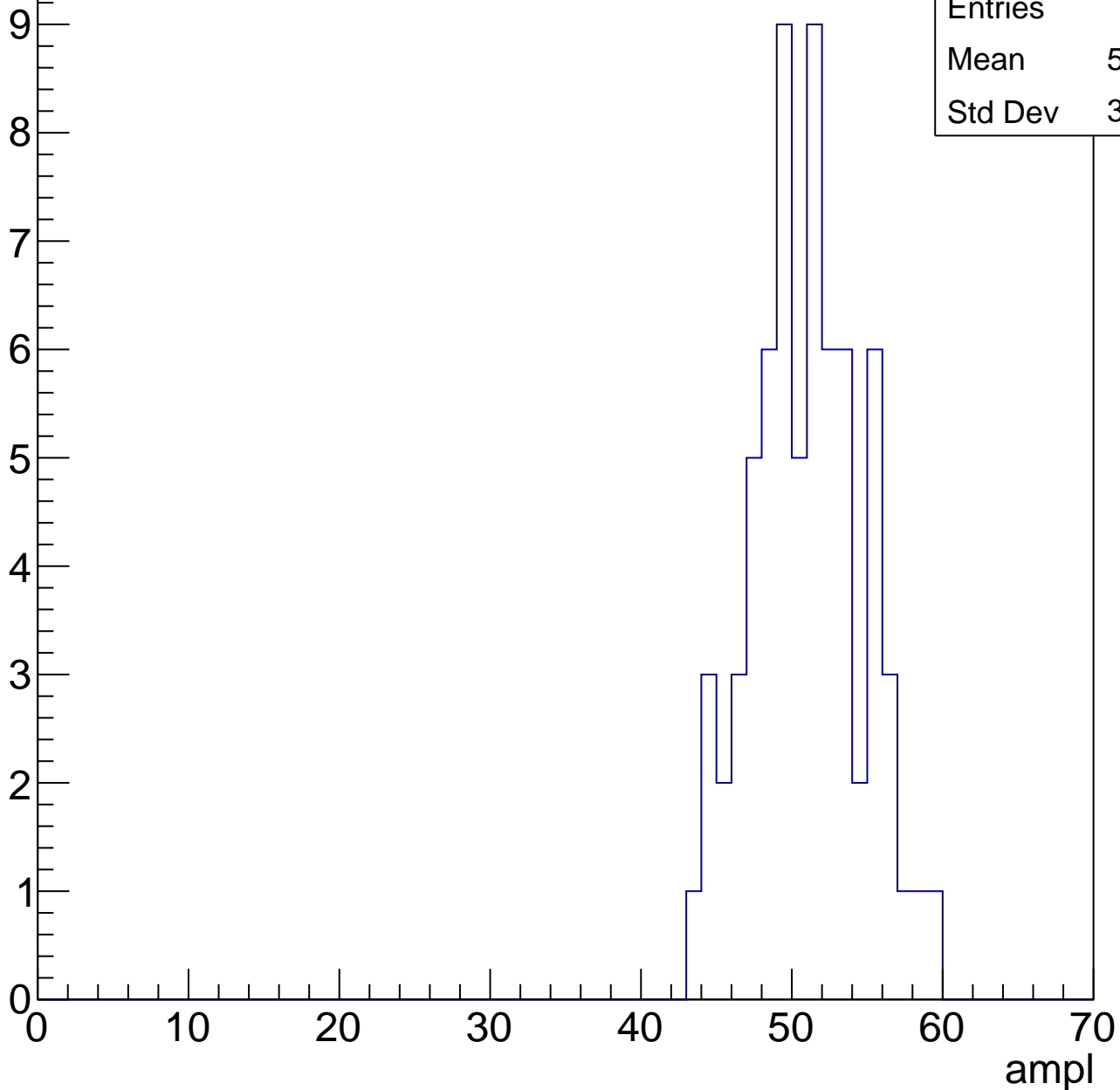


# B1L101S, U16-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	50.52
Std Dev	3.582



# B1L101S, U16-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

6

5

4

3

2

1

0

0

10

20

30

40

50

60

ampl

Entries	51
Mean	56.53
Std Dev	3.07

0

1

2

3

4

5

6

# B1L101S, U16-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	44
Mean	58.75
Std Dev	9.379

Entry

10

8

6

4

2

0

0

10

20

30

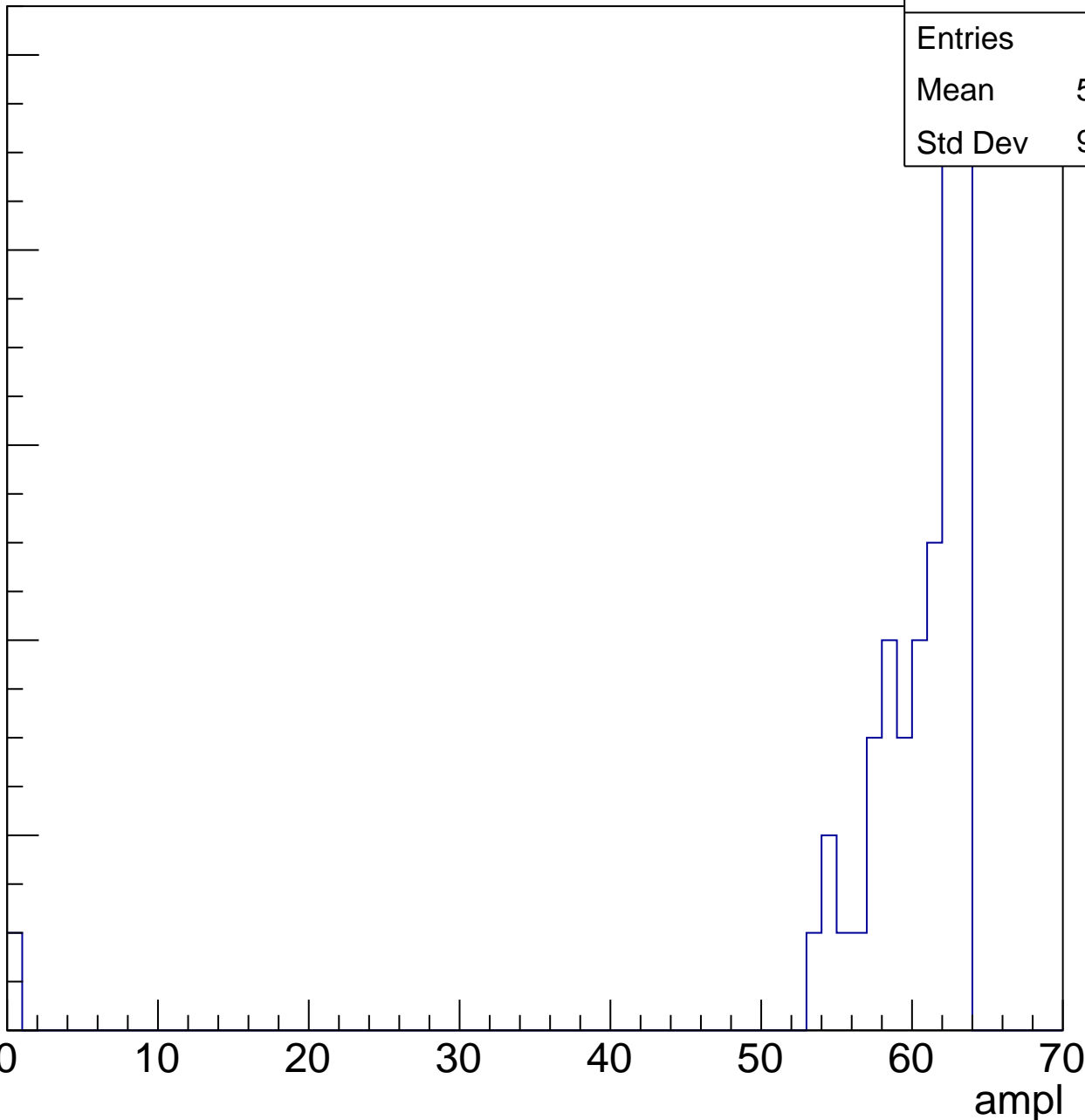
40

50

60

70

ampl



# B1L101S, U16-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U16-ch86, adc0

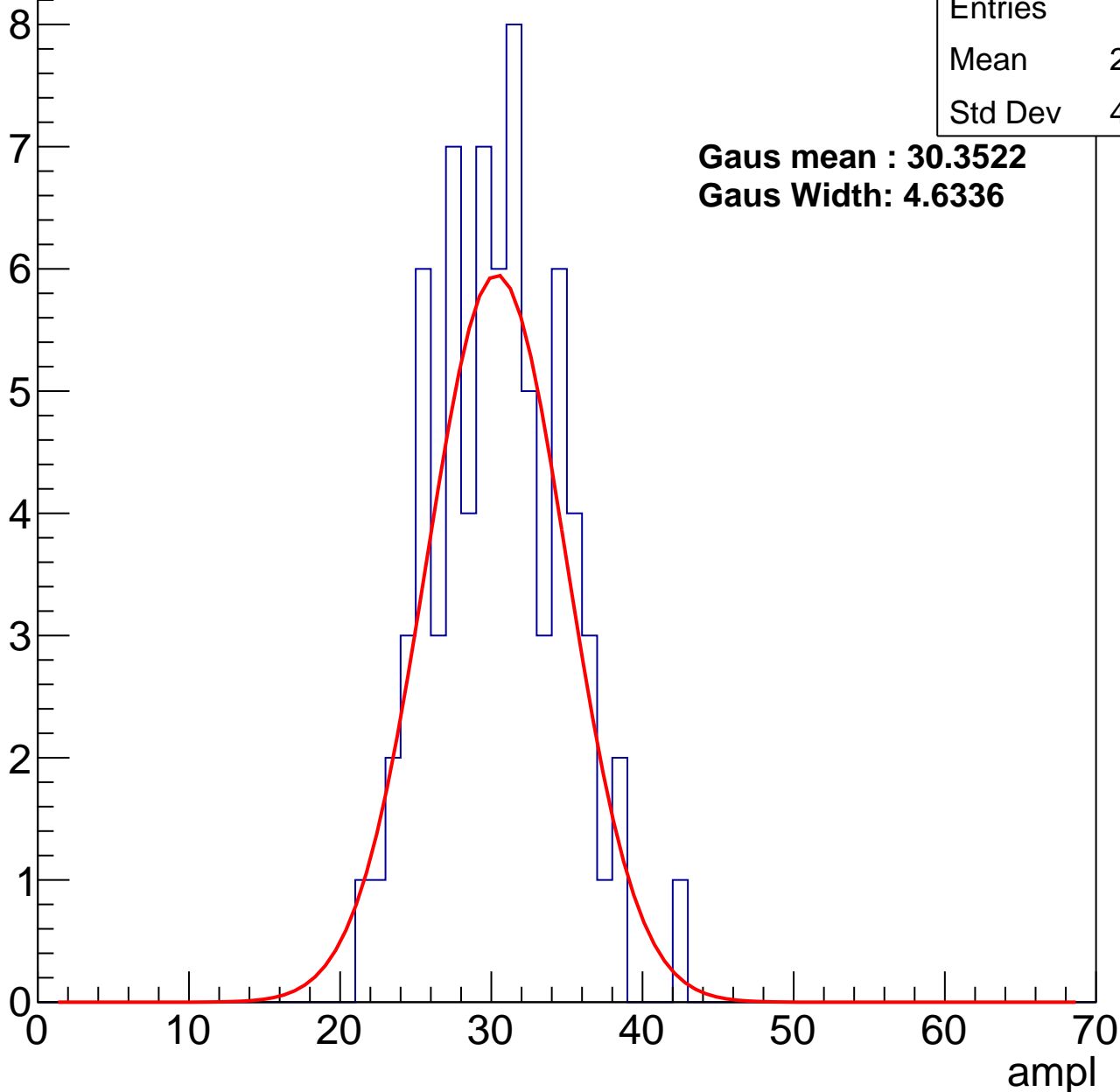
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	29.96
Std Dev	4.244

**Gaus mean : 30.3522**

**Gaus Width: 4.6336**



# B1L101S, U16-ch86, adc1

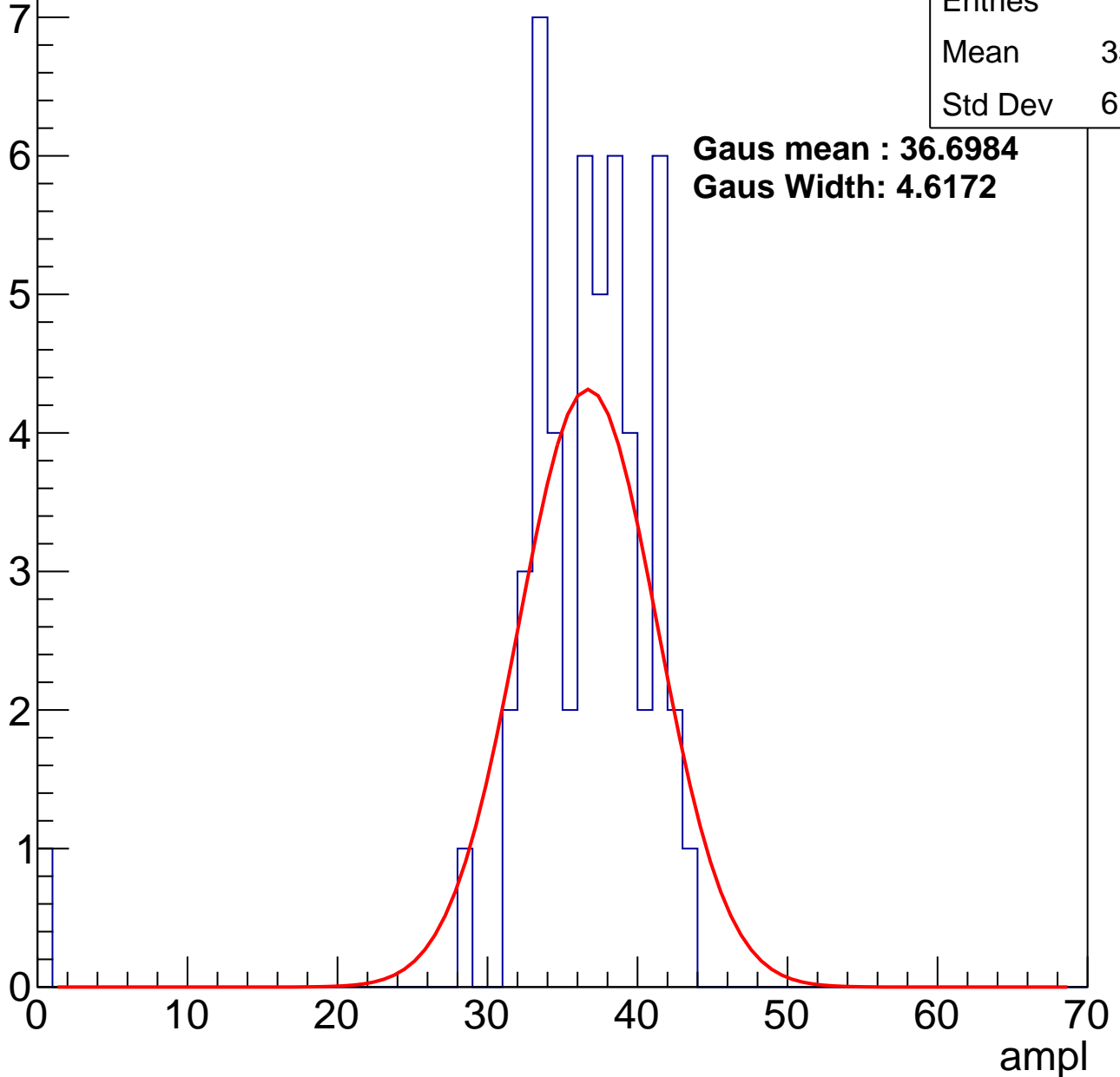
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	35.79
Std Dev	6.052

**Gaus mean : 36.6984**

**Gaus Width: 4.6172**



# B1L101S, U16-ch86, adc2

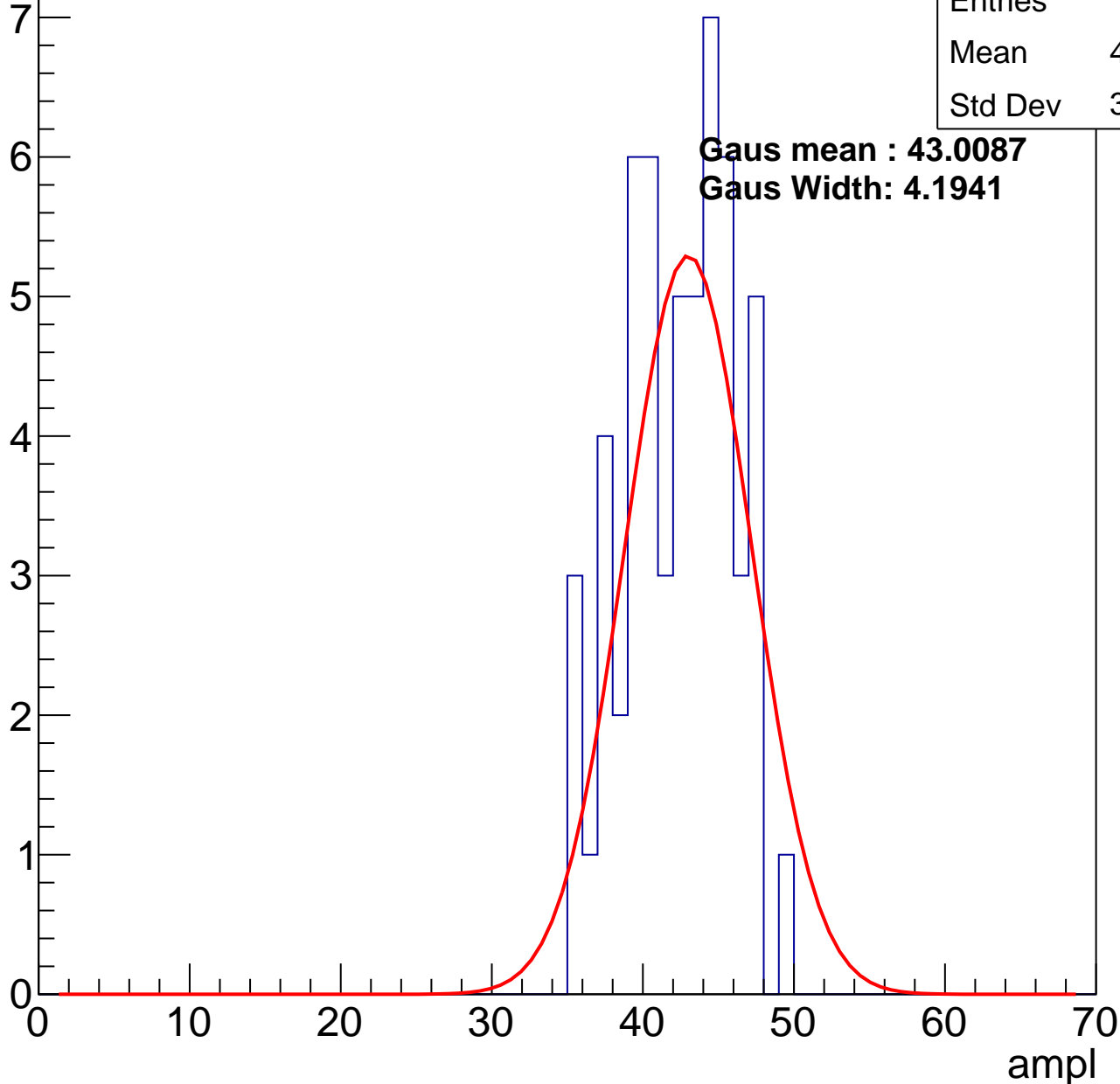
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	41.88
Std Dev	3.515

**Gaus mean : 43.0087**

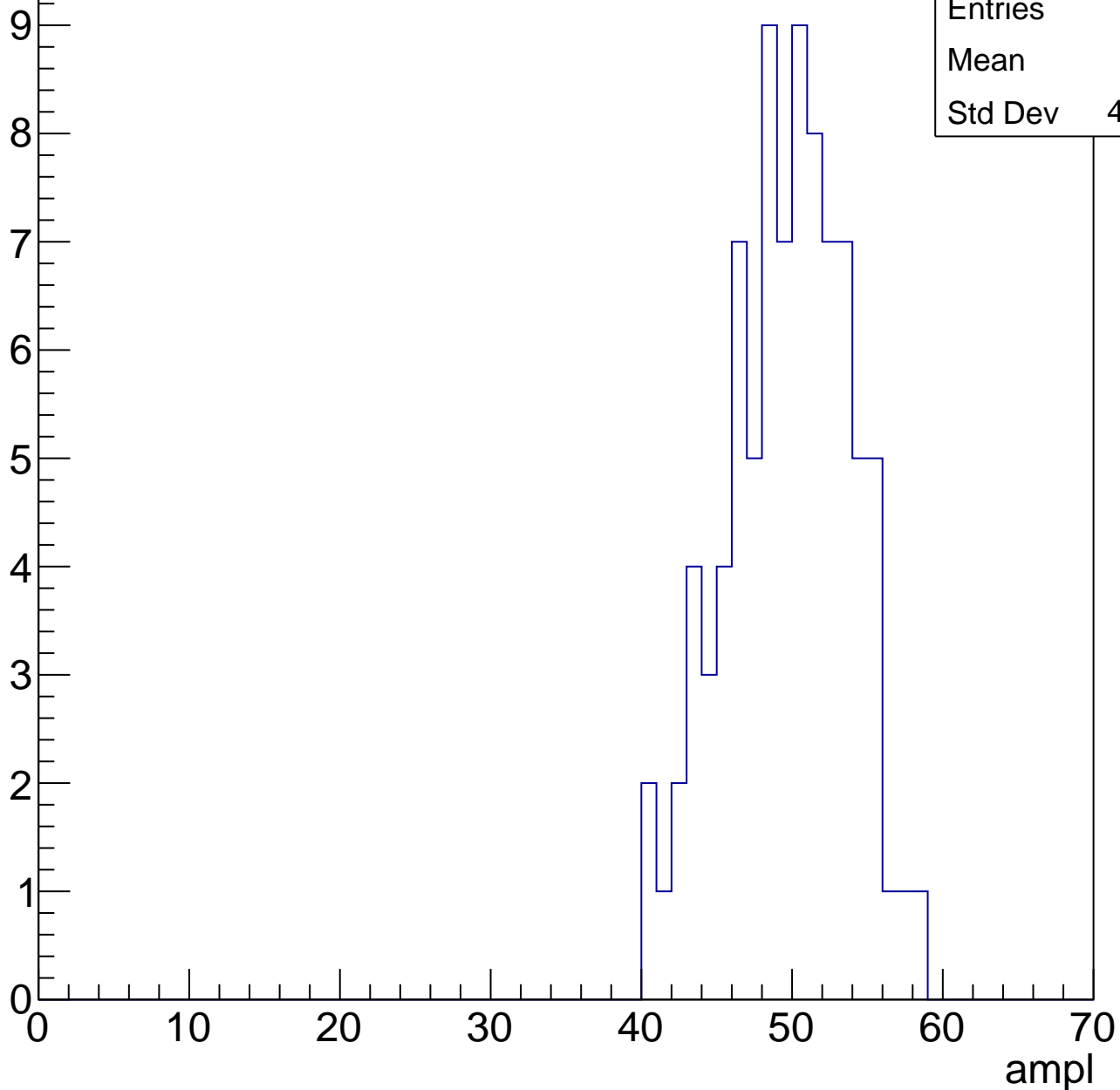
**Gaus Width: 4.1941**



# B1L101S, U16-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



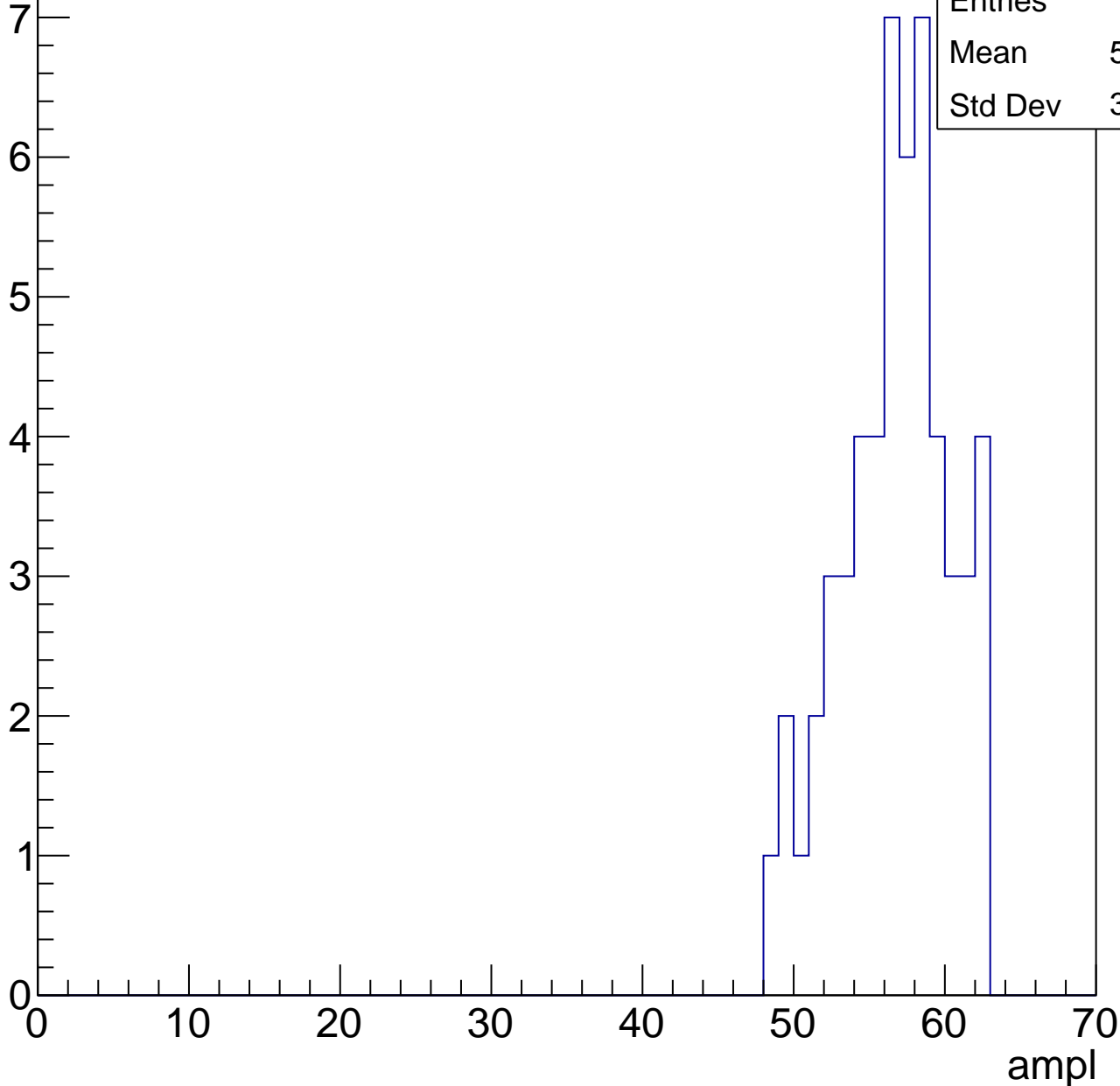
Entries	88
Mean	49.2
Std Dev	4.003

# B1L101S, U16-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	56.22
Std Dev	3.542

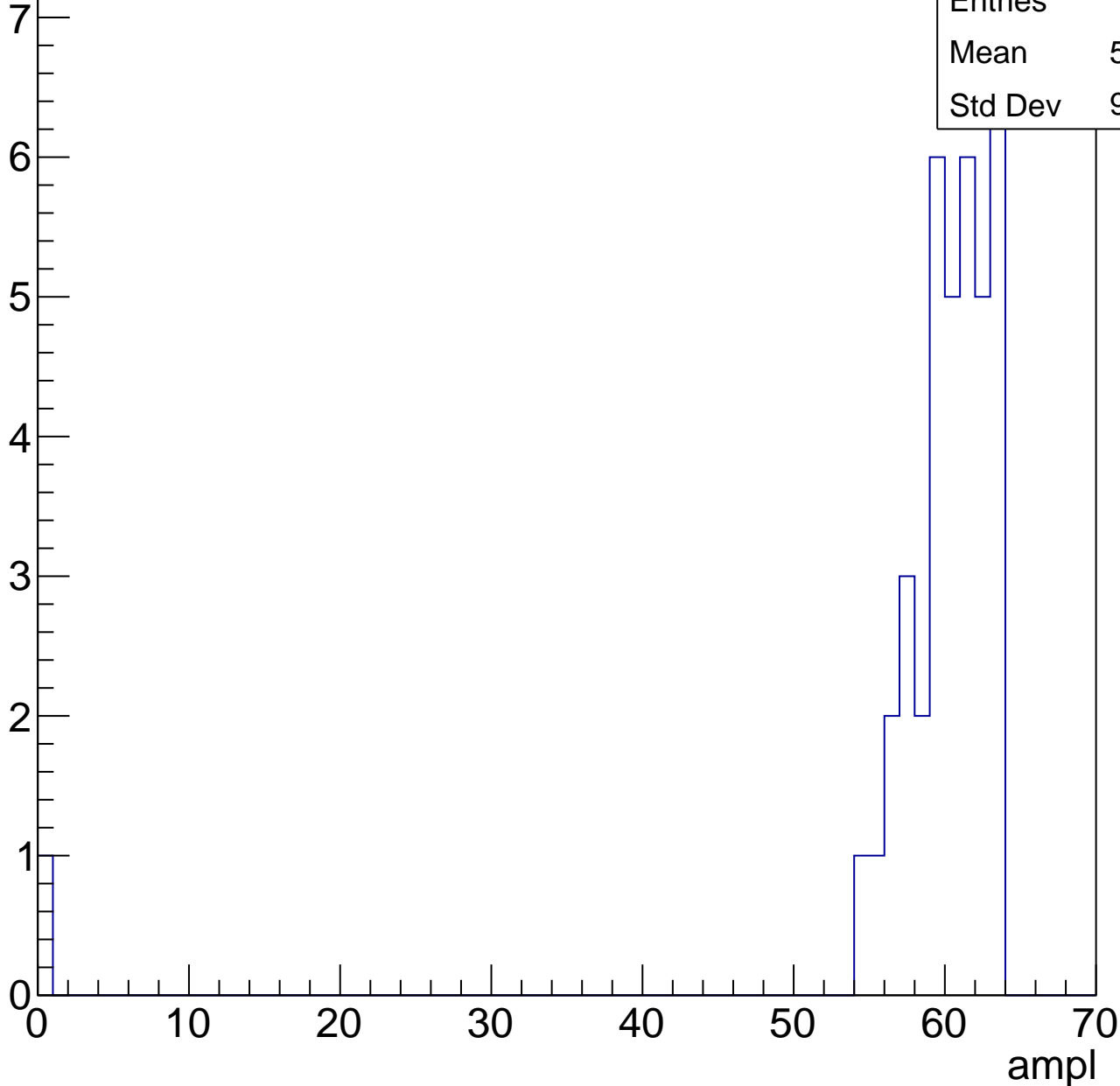


# B1L101S, U16-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

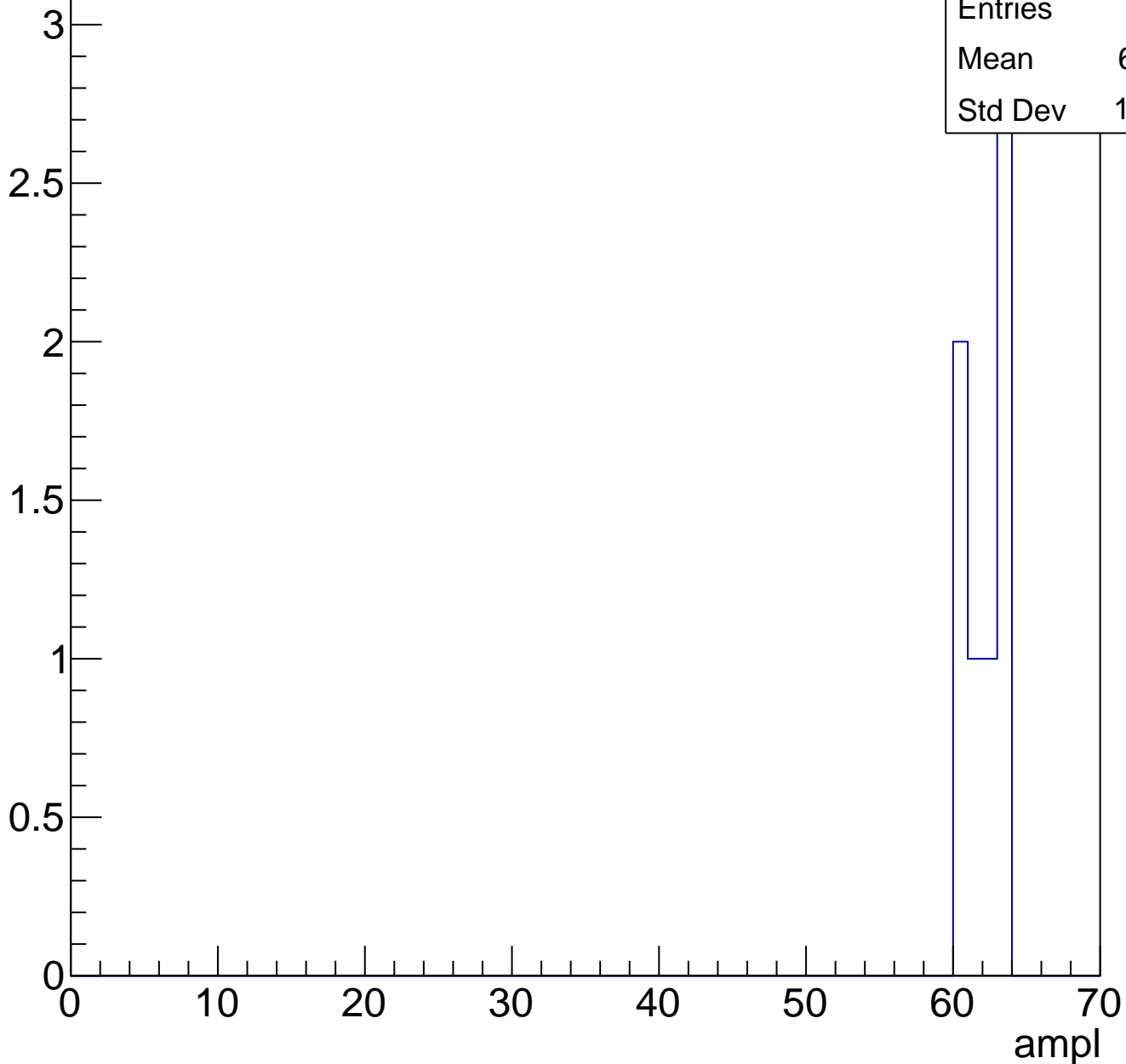
Entries	39
Mean	58.44
Std Dev	9.776



# B1L101S, U16-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U16-ch87, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	76
Mean	31.24
Std Dev	6.121

**Gaus mean : 32.1501**

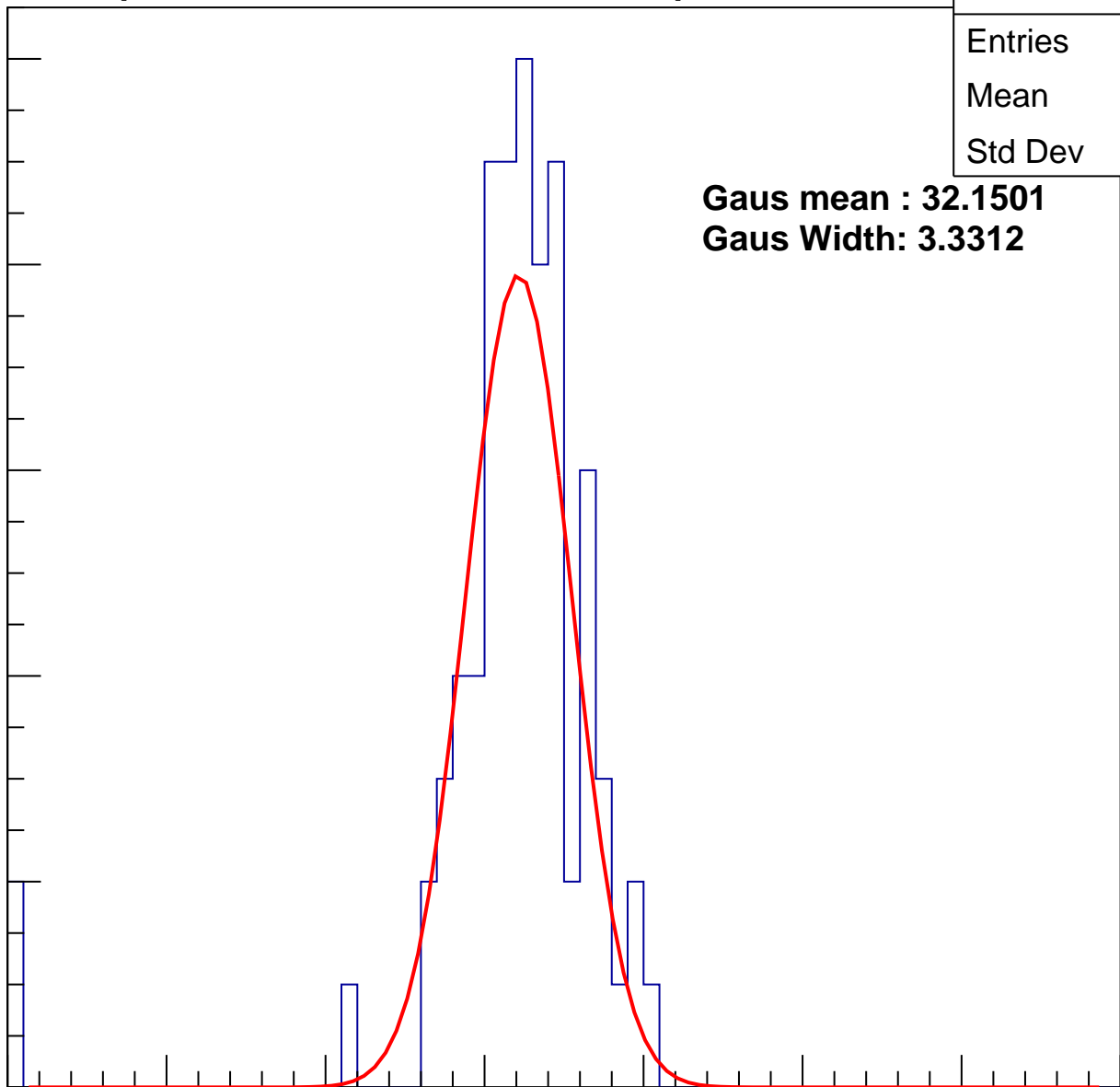
**Gaus Width: 3.3312**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch87, adc1

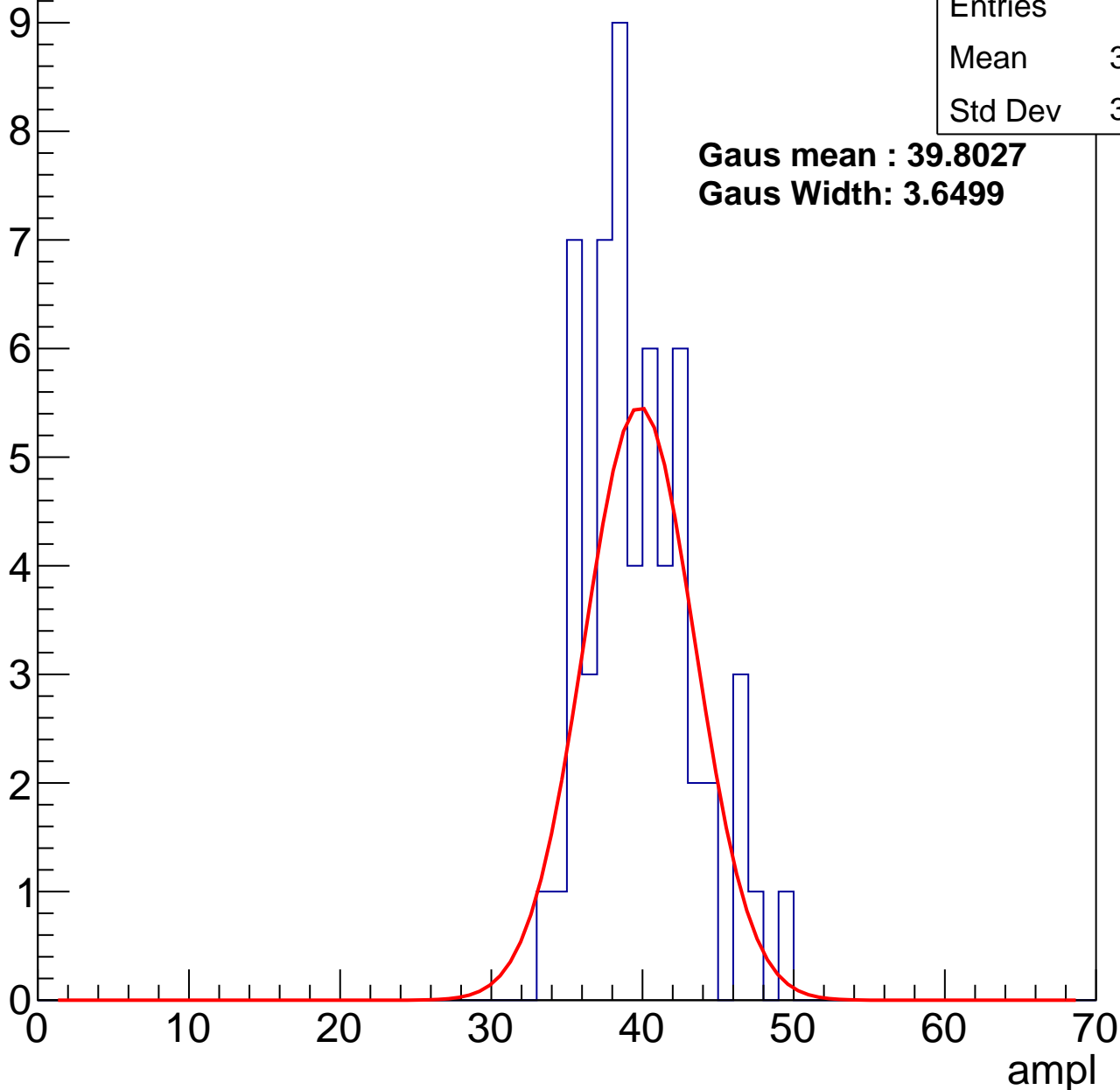
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	39.32
Std Dev	3.505

**Gaus mean : 39.8027**

**Gaus Width: 3.6499**



# B1L101S, U16-ch87, adc2

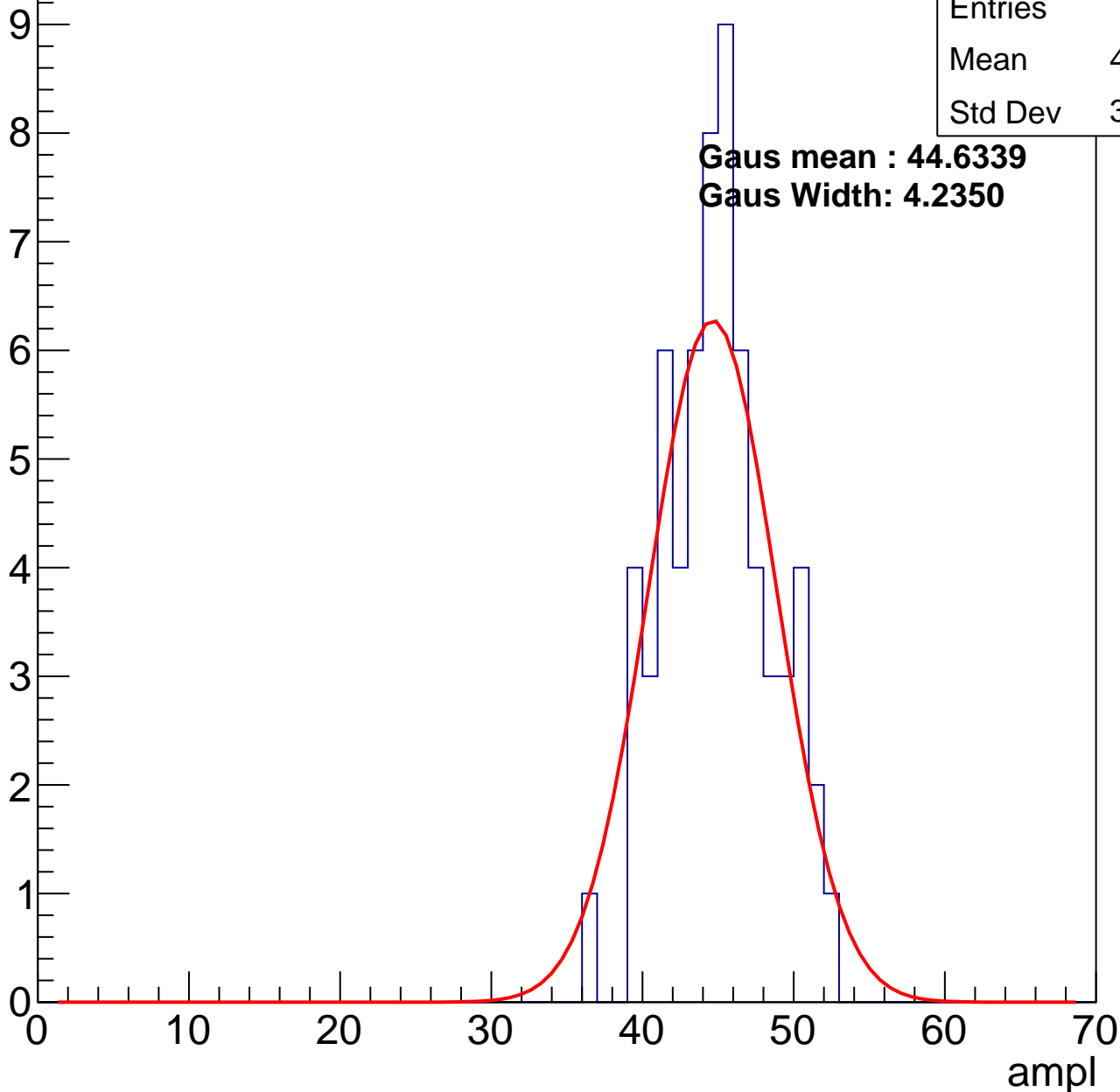
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	44.53
Std Dev	3.464

**Gaus mean : 44.6339**

**Gaus Width: 4.2350**

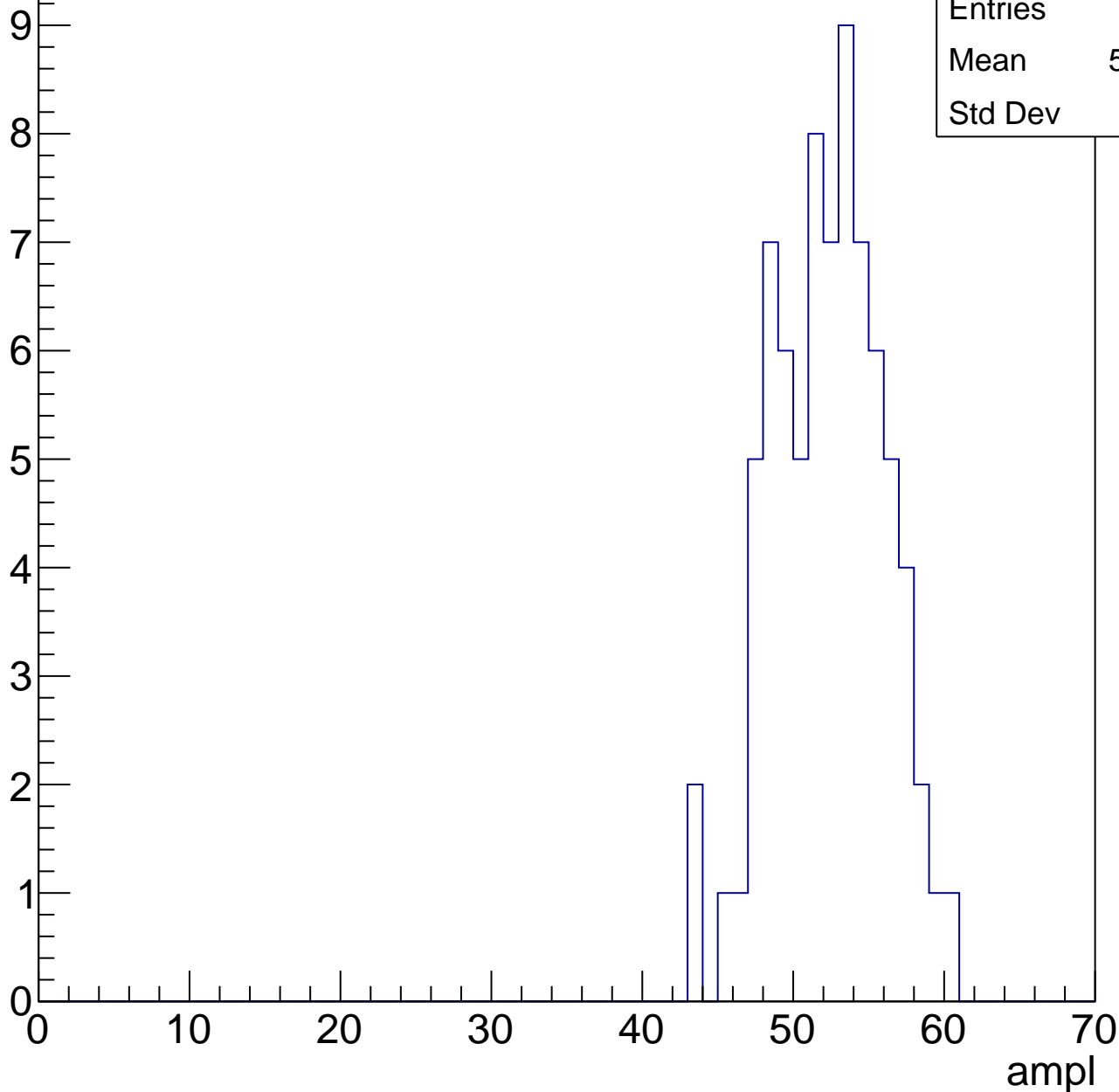


# B1L101S, U16-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

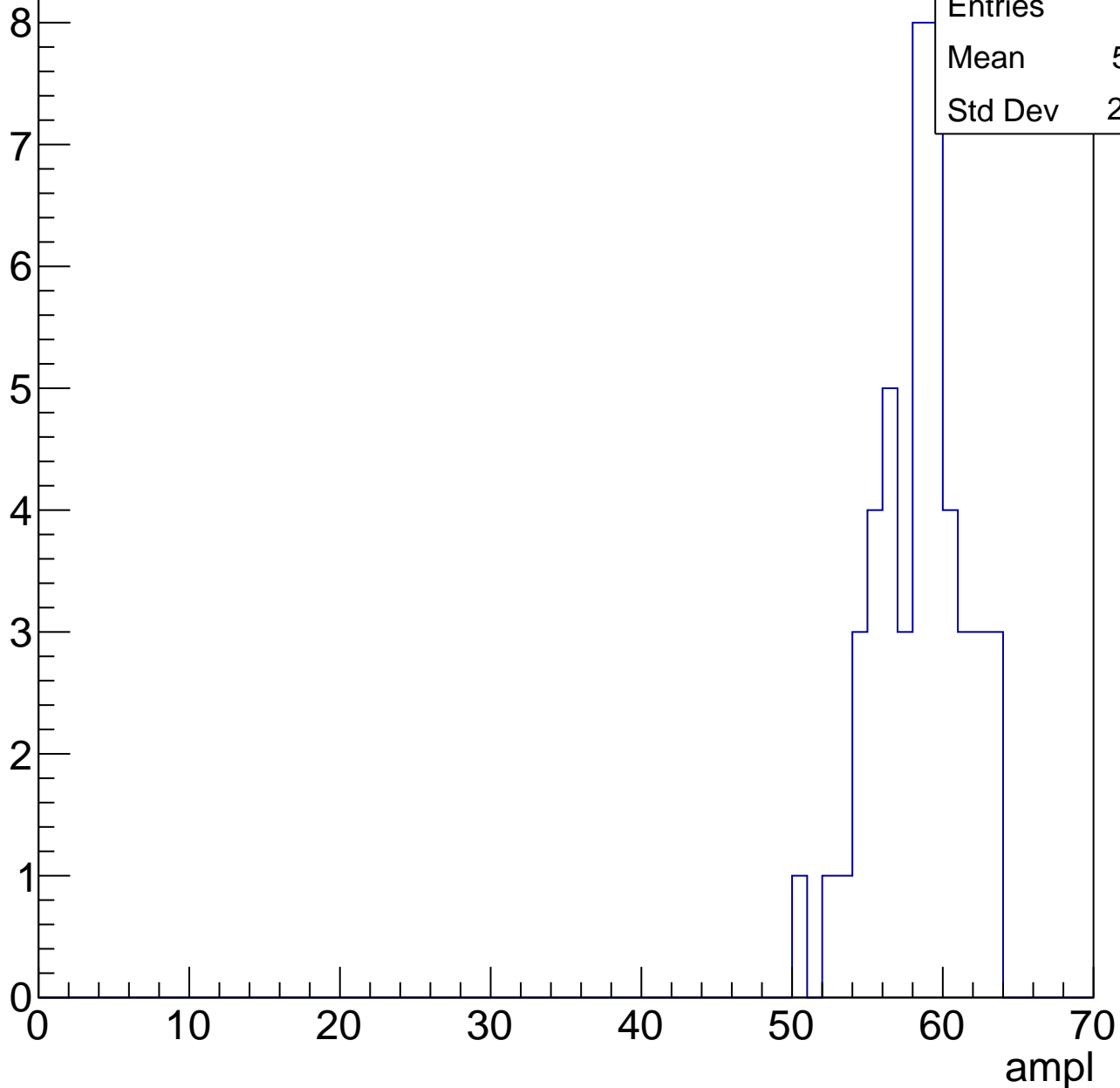
Entries	77
Mean	51.84
Std Dev	3.64



# B1L101S, U16-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

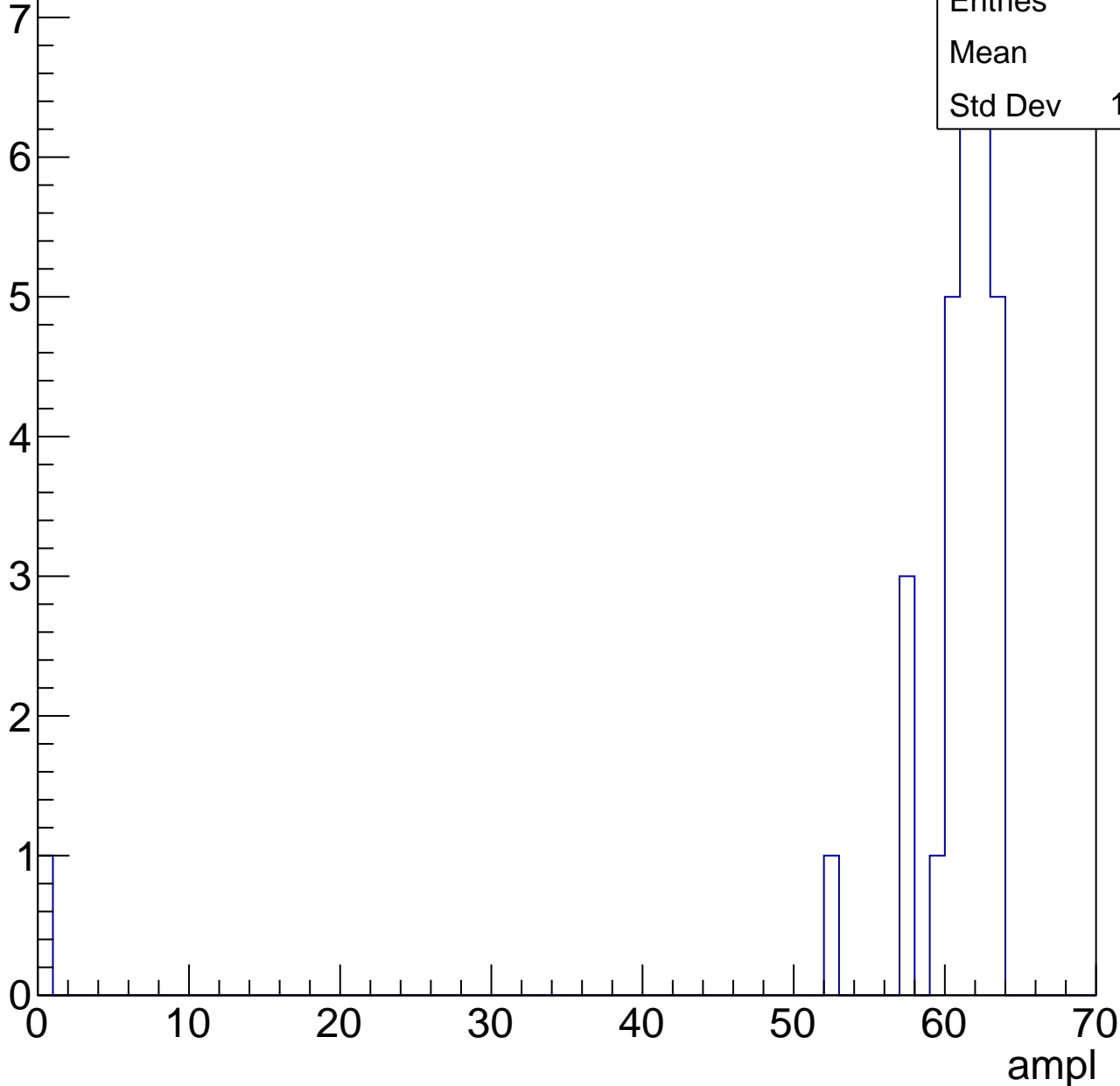


# B1L101S, U16-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	30
Mean	58.6
Std Dev	11.13



# B1L101S, U16-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	2
Mean	63
Std Dev	0

0 10 20 30 40 50 60 70

ampl



# B1L101S, U16-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U16-ch88, adc0

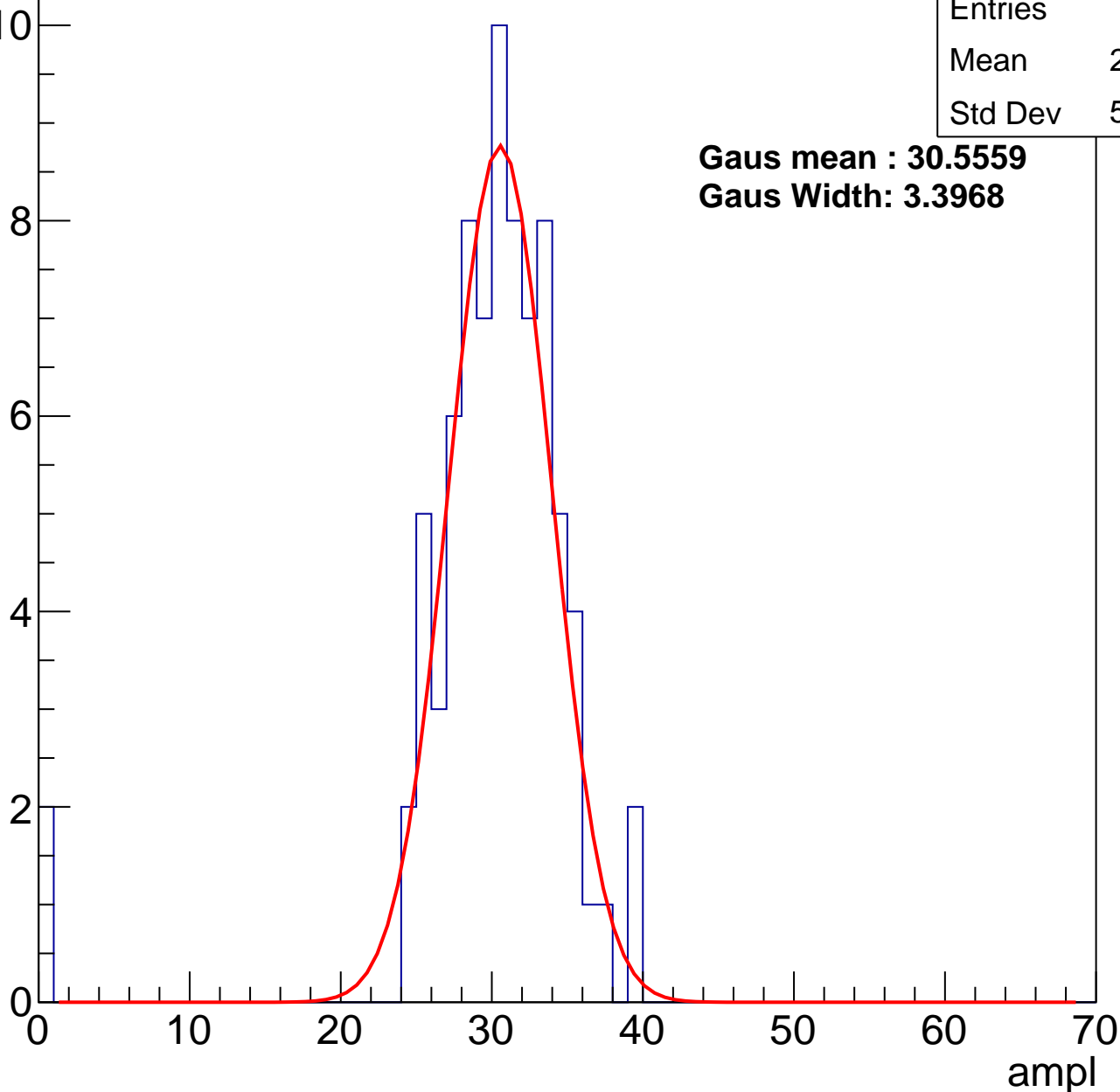
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	29.58
Std Dev	5.802

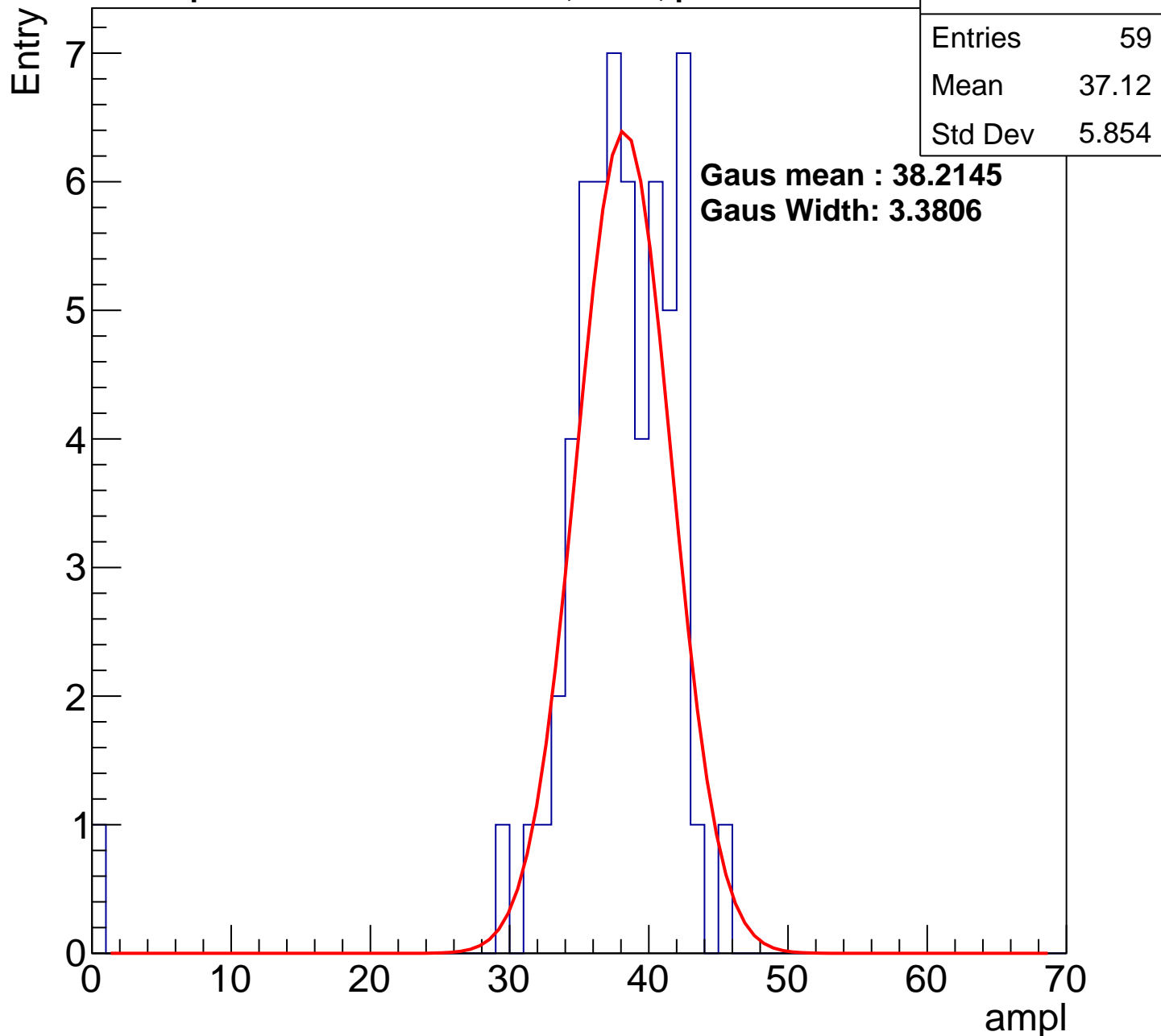
**Gaus mean : 30.5559**

**Gaus Width: 3.3968**



# B1L101S, U16-ch88, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U16-ch88, adc2

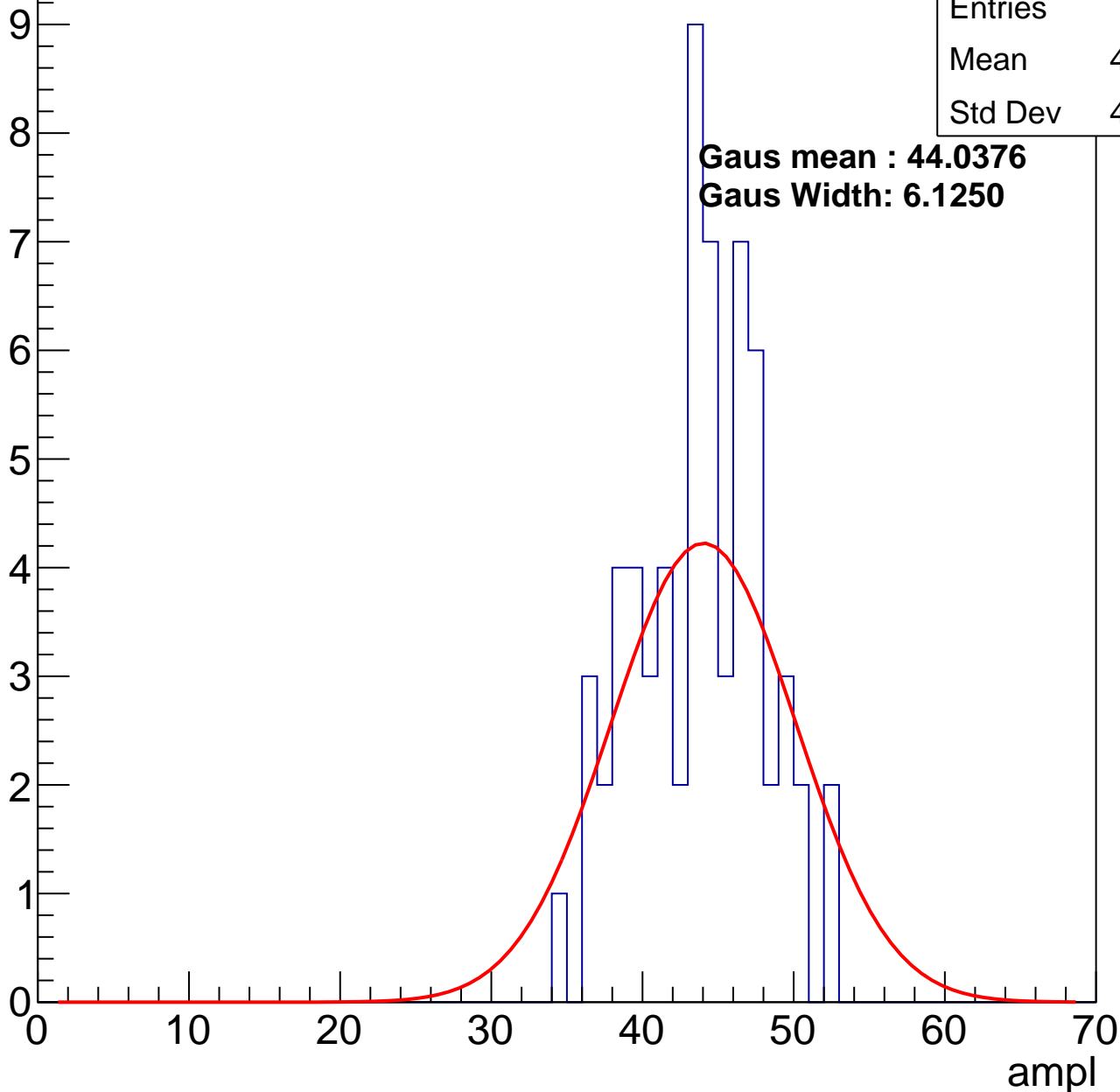
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	43.33
Std Dev	4.142

**Gaus mean : 44.0376**

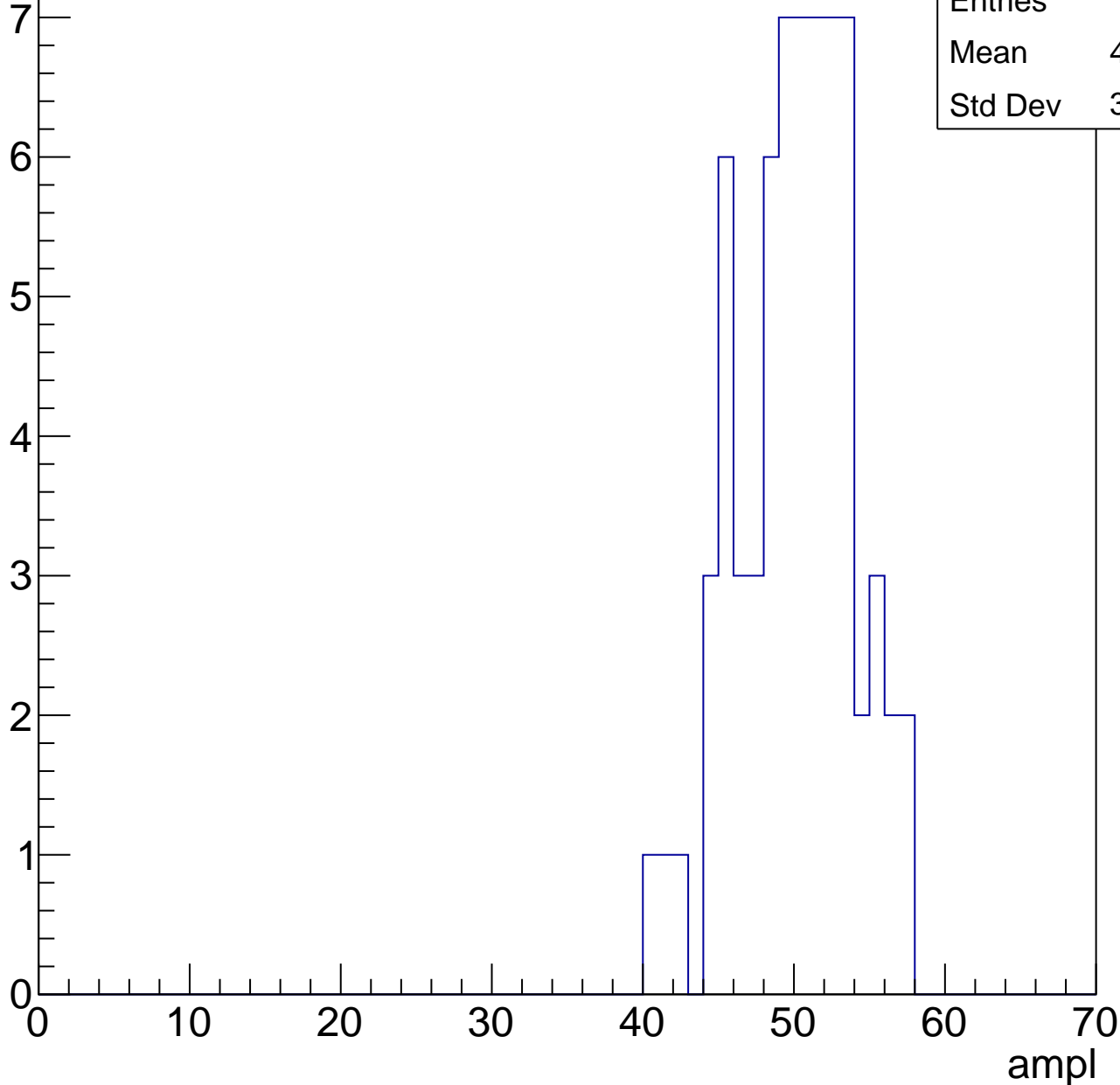
**Gaus Width: 6.1250**



# B1L101S, U16-ch88, adc3

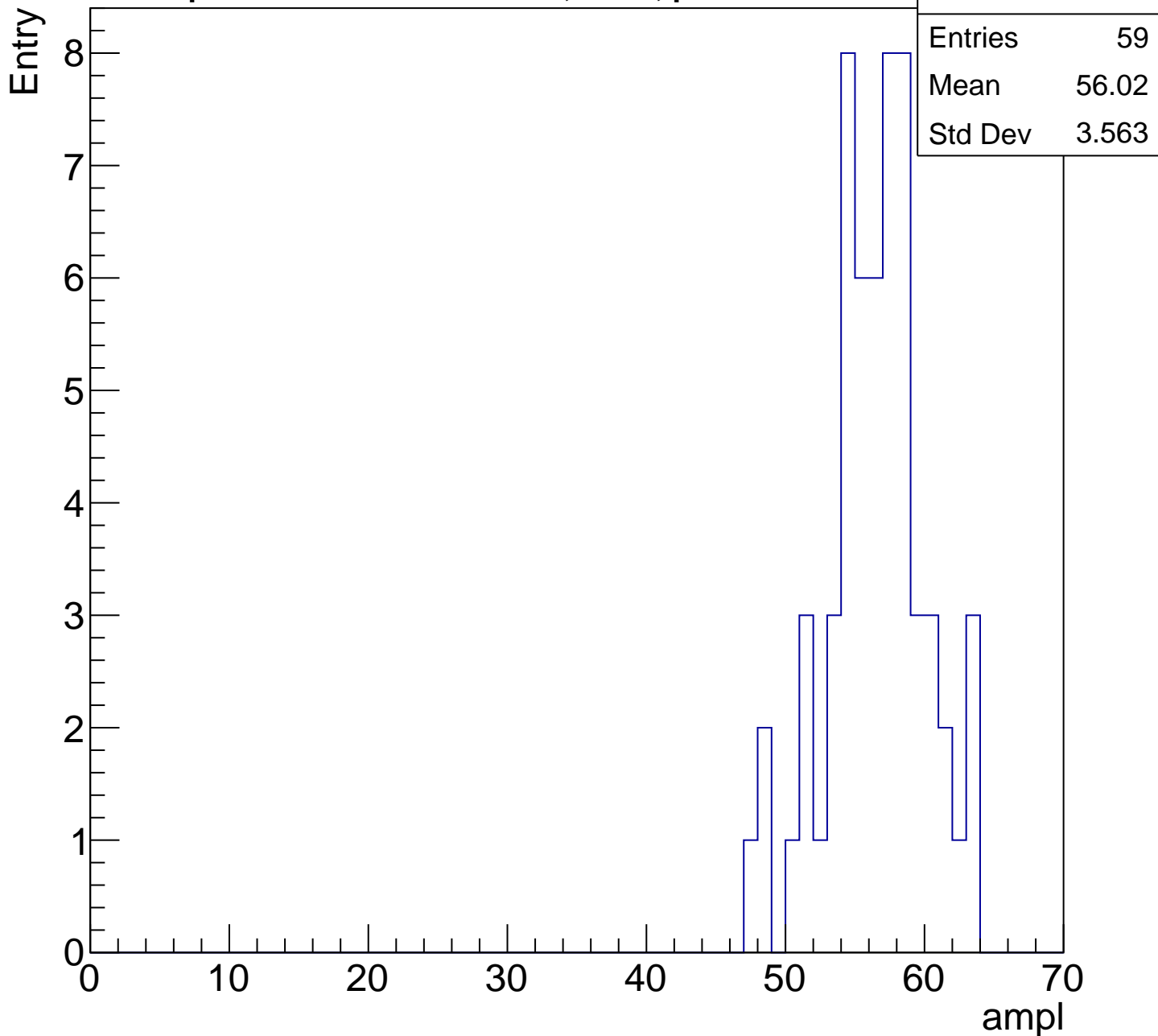
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch88, adc4

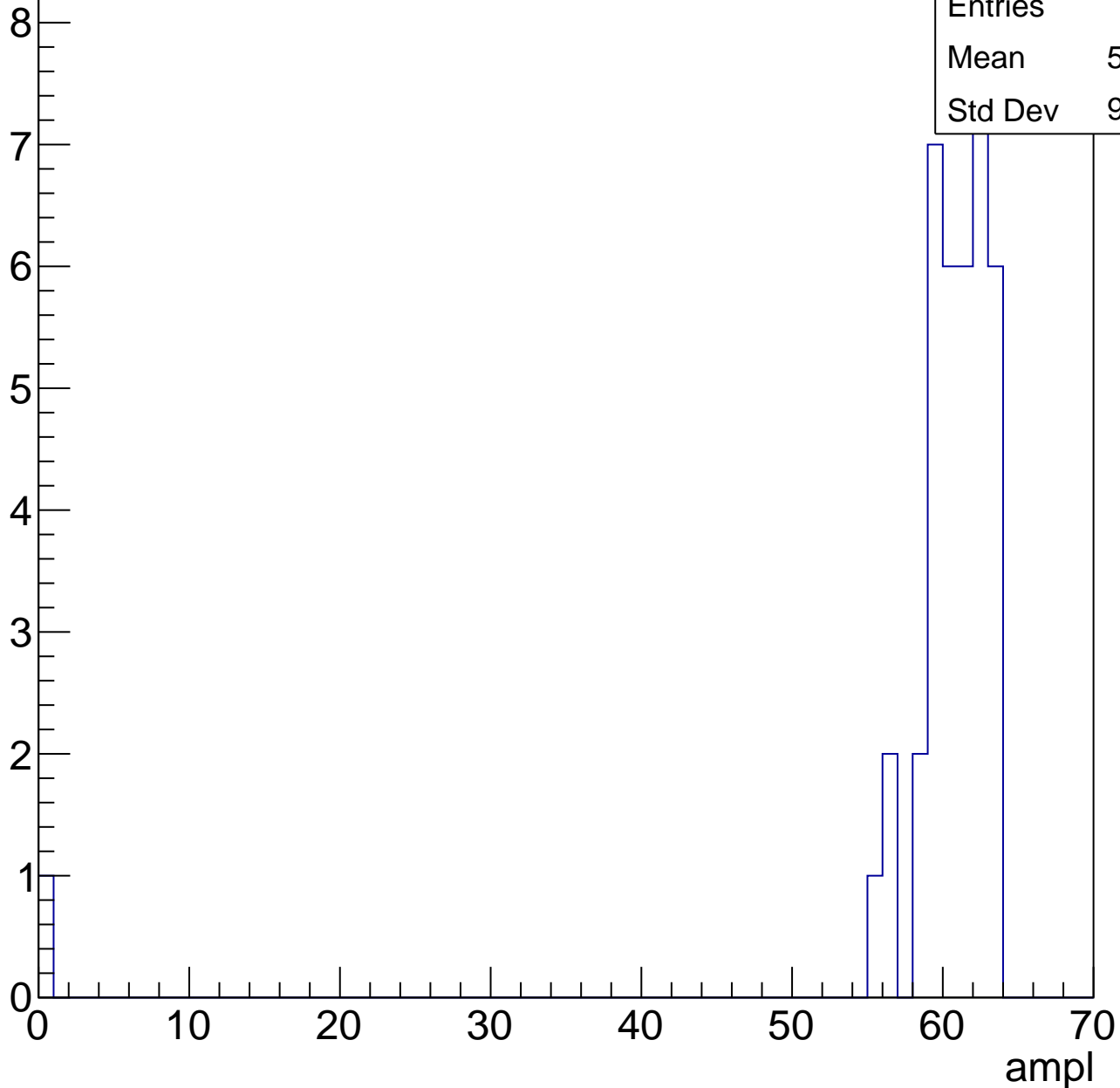
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U16-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

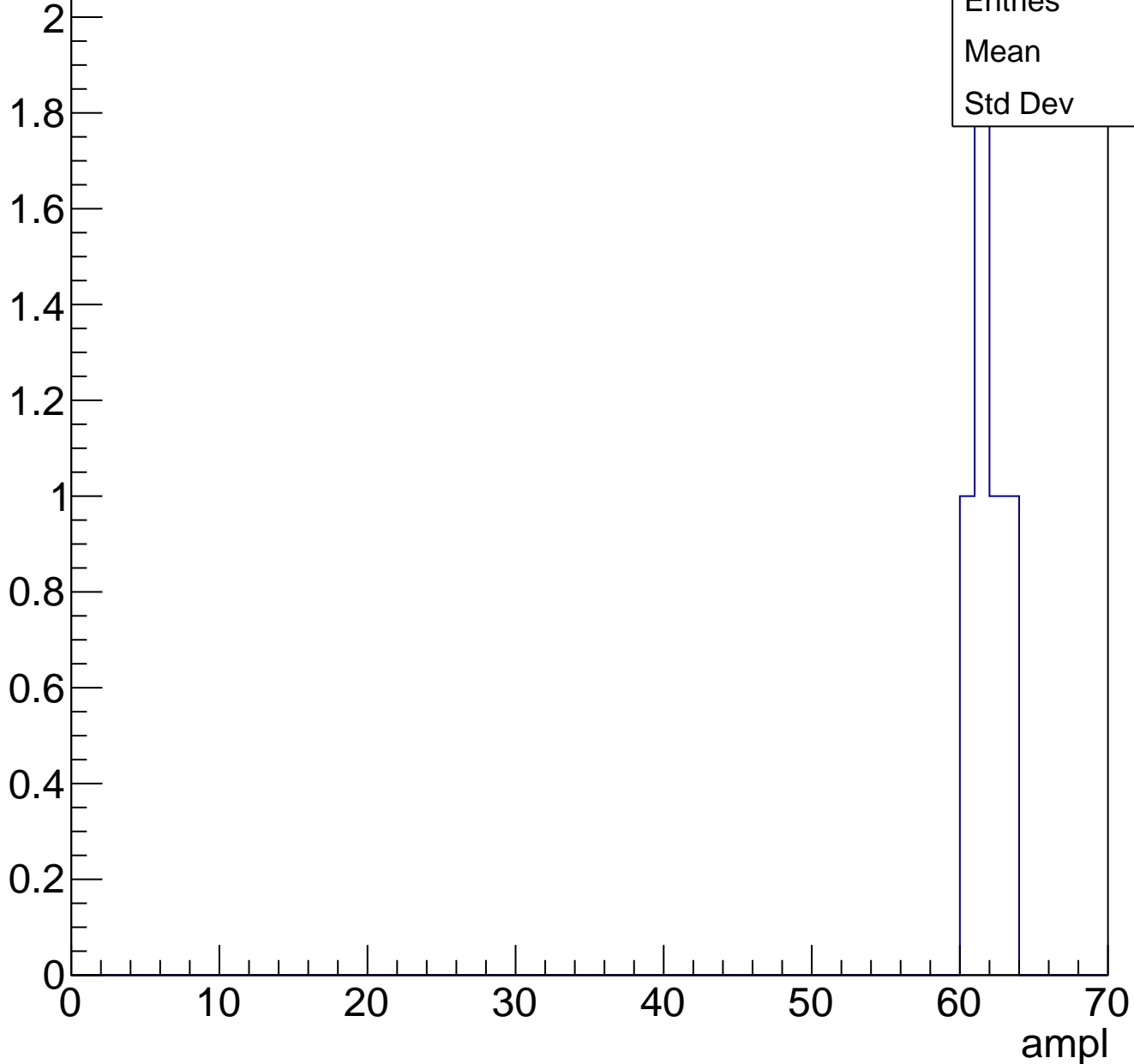
Entry



# B1L101S, U16-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	5
Mean	61.4
Std Dev	1.02



# B1L101S, U16-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U16-ch89, adc0

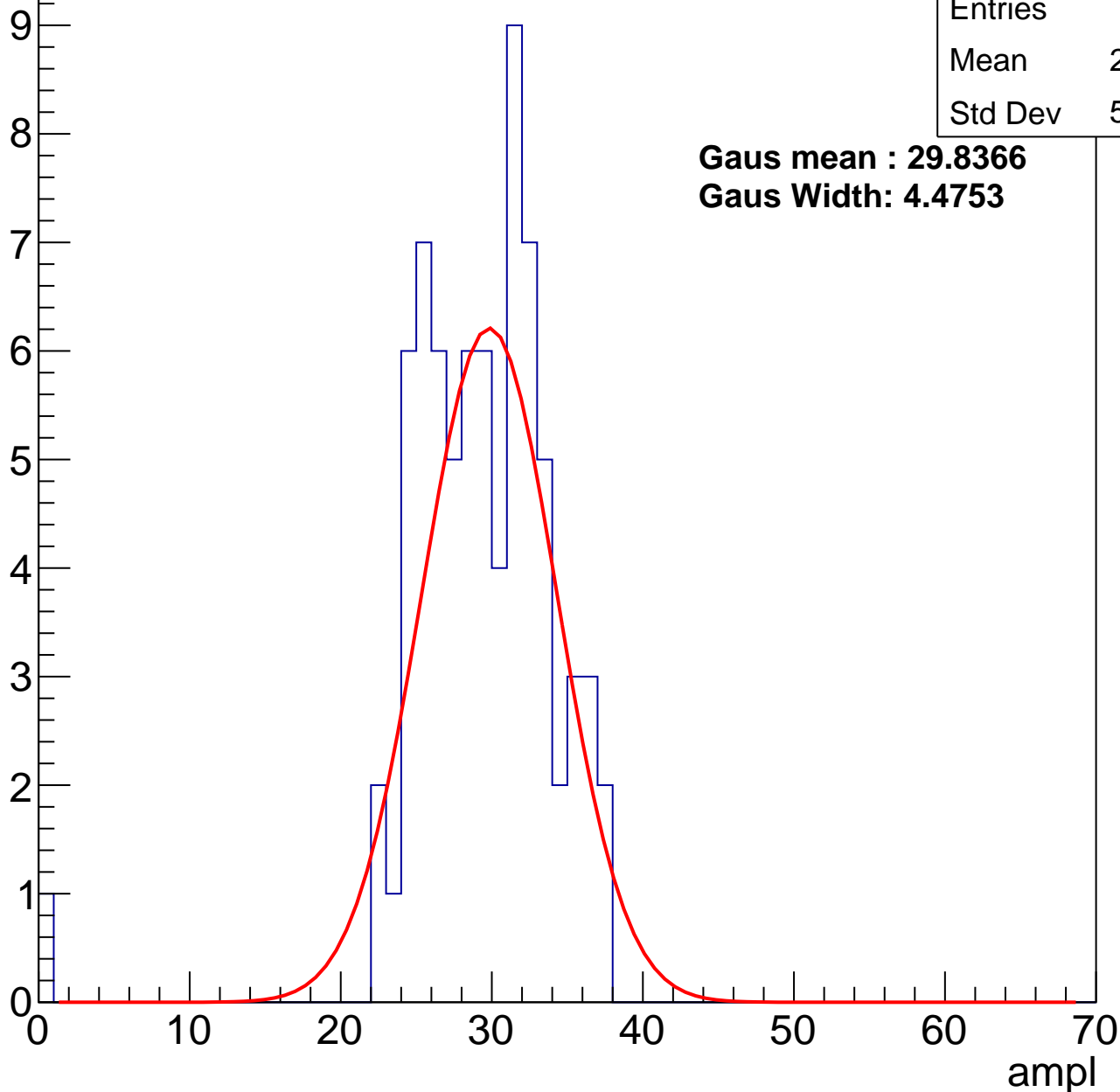
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	28.83
Std Dev	5.074

**Gaus mean : 29.8366**

**Gaus Width: 4.4753**



# B1L101S, U16-ch89, adc1

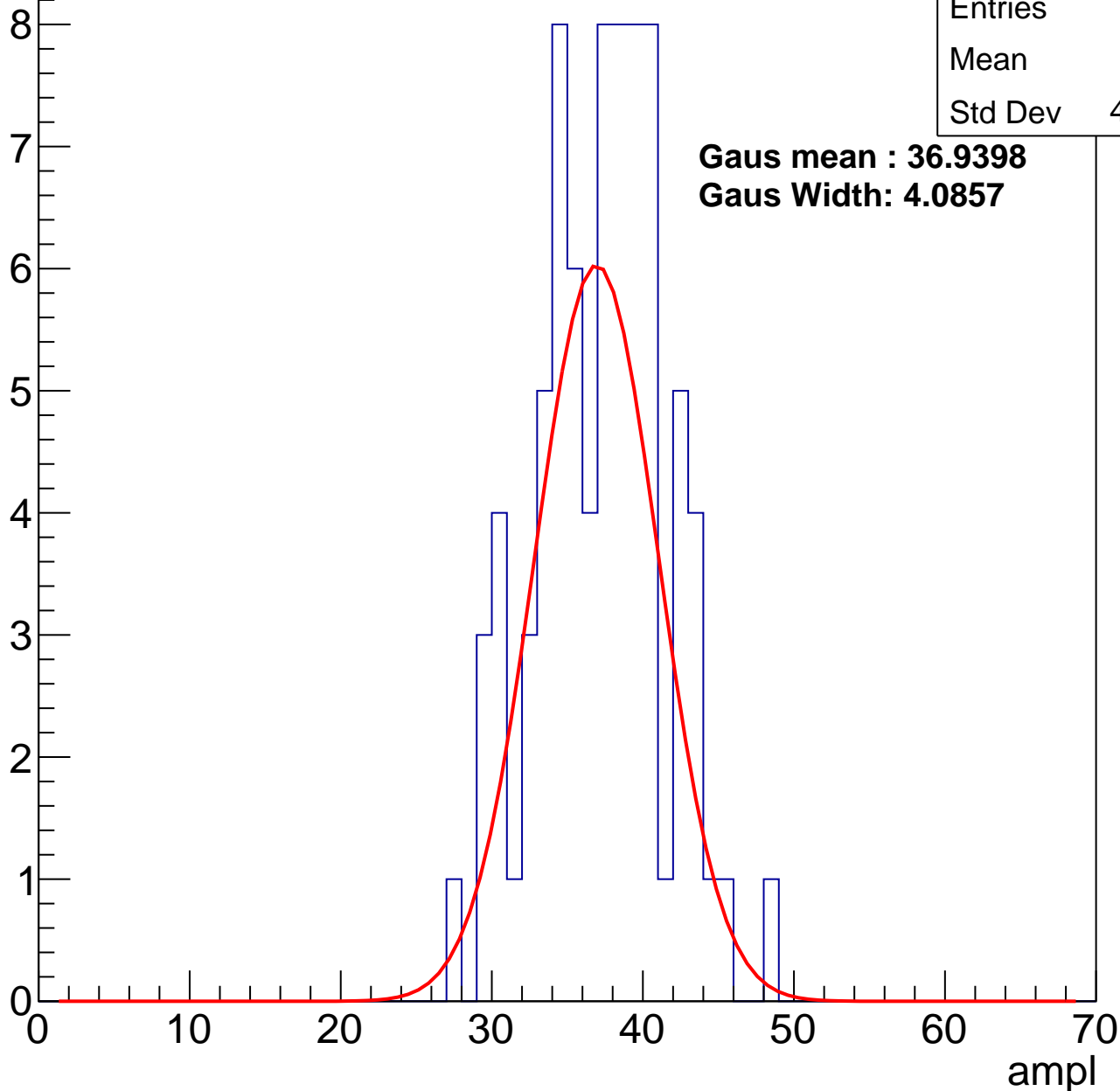
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	36.8
Std Dev	4.193

**Gaus mean : 36.9398**

**Gaus Width: 4.0857**



# B1L101S, U16-ch89, adc2

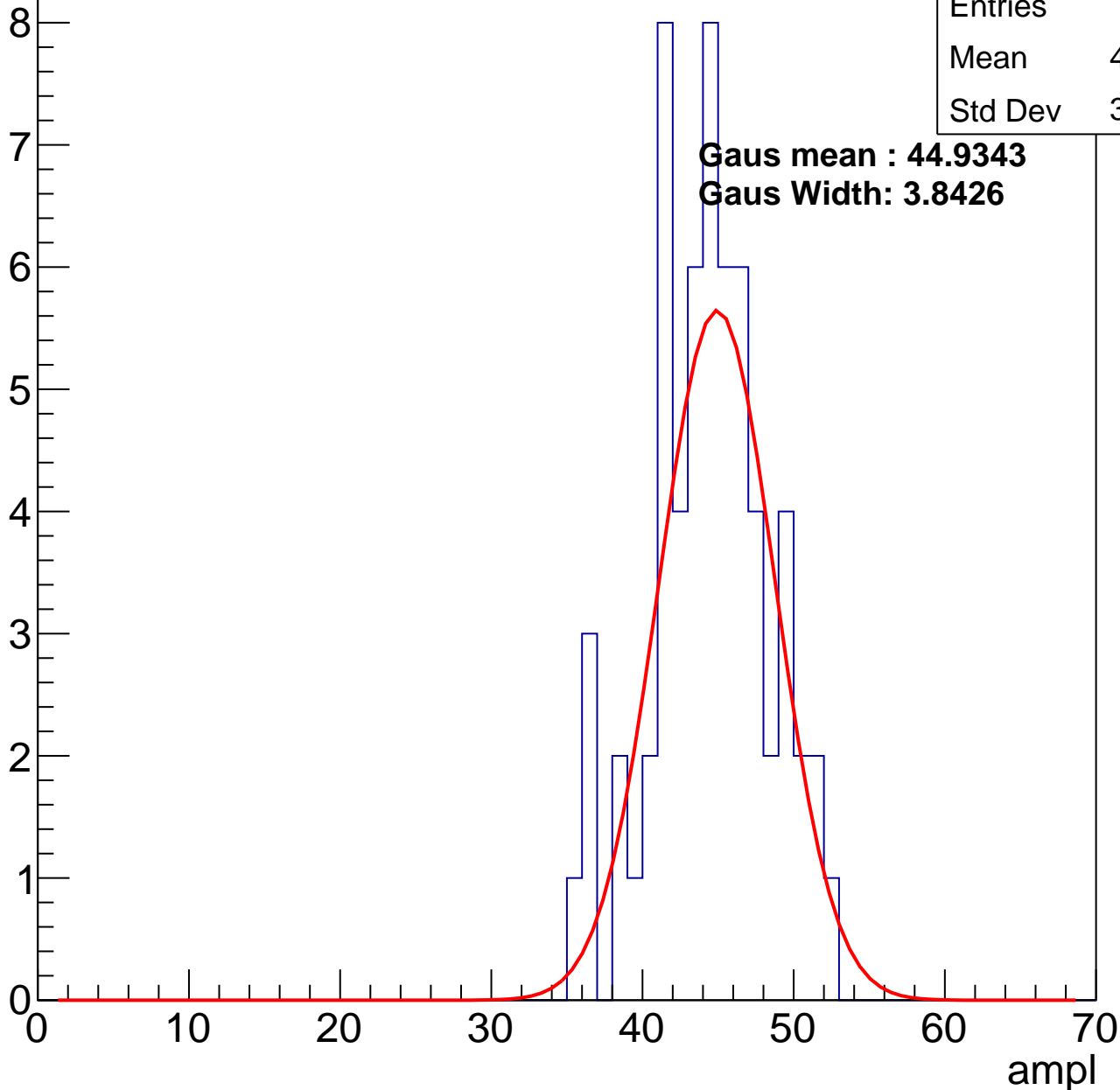
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	43.94
Std Dev	3.868

**Gaus mean : 44.9343**

**Gaus Width: 3.8426**

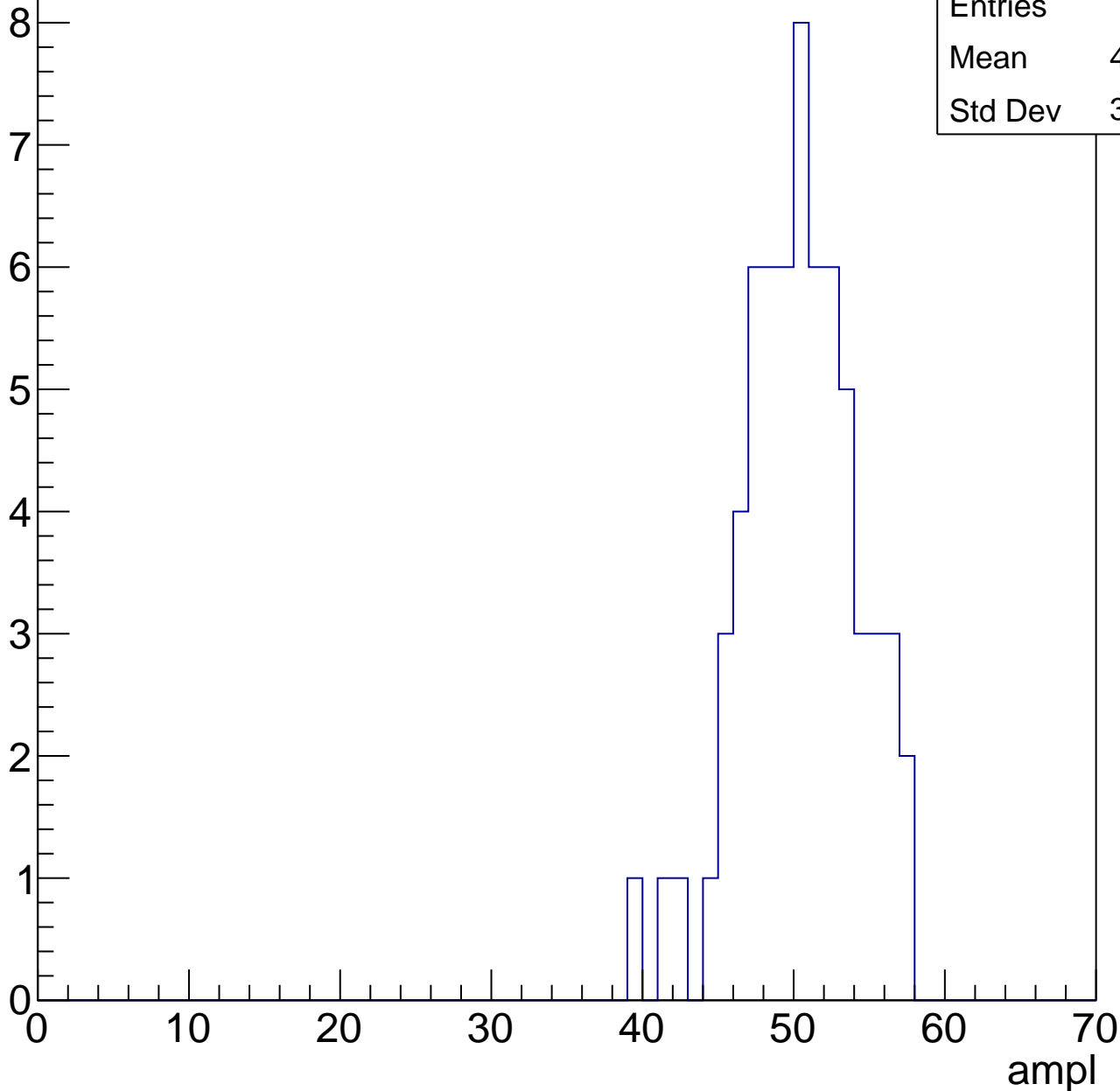


# B1L101S, U16-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	49.86
Std Dev	3.778

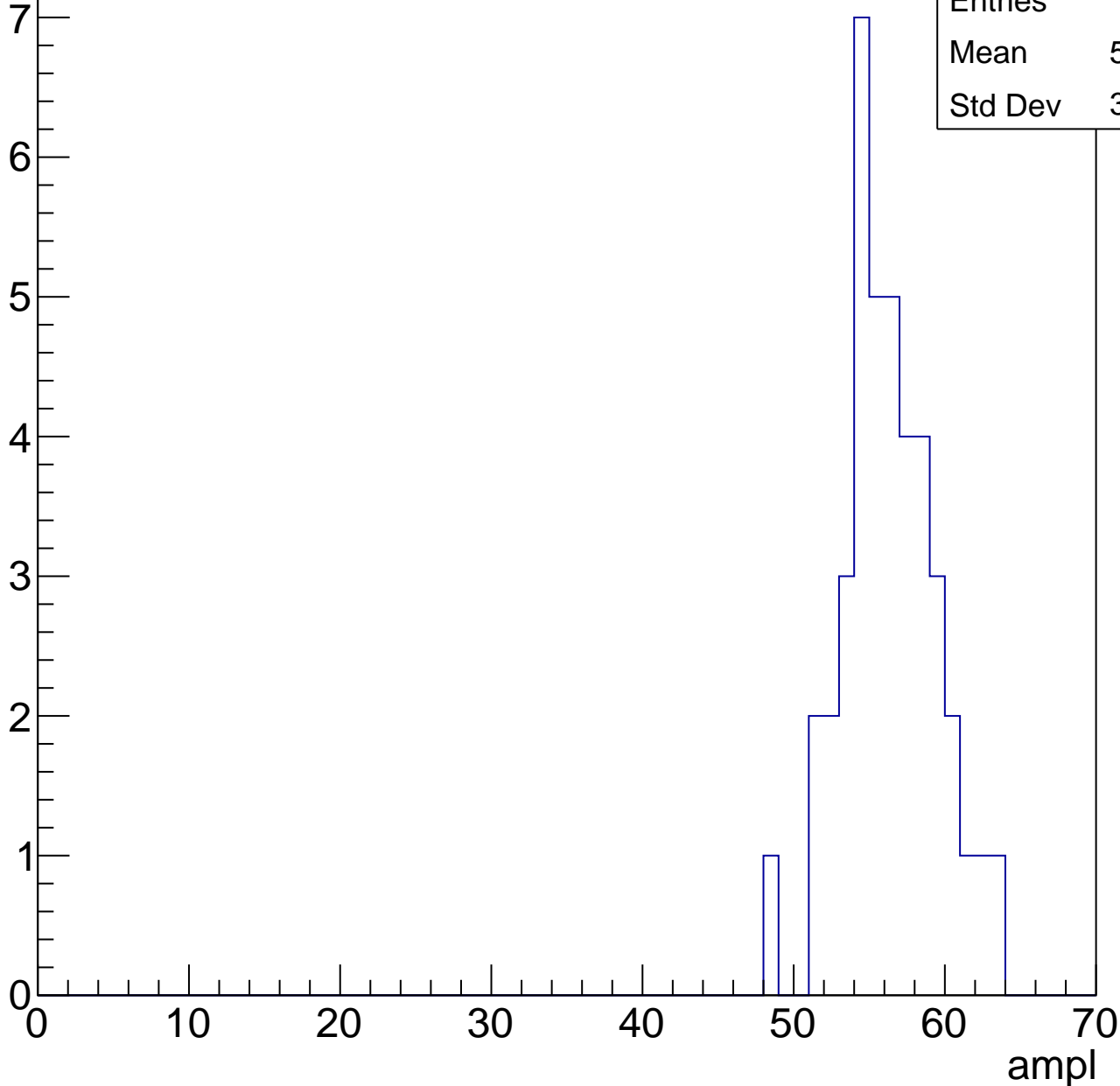


# B1L101S, U16-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

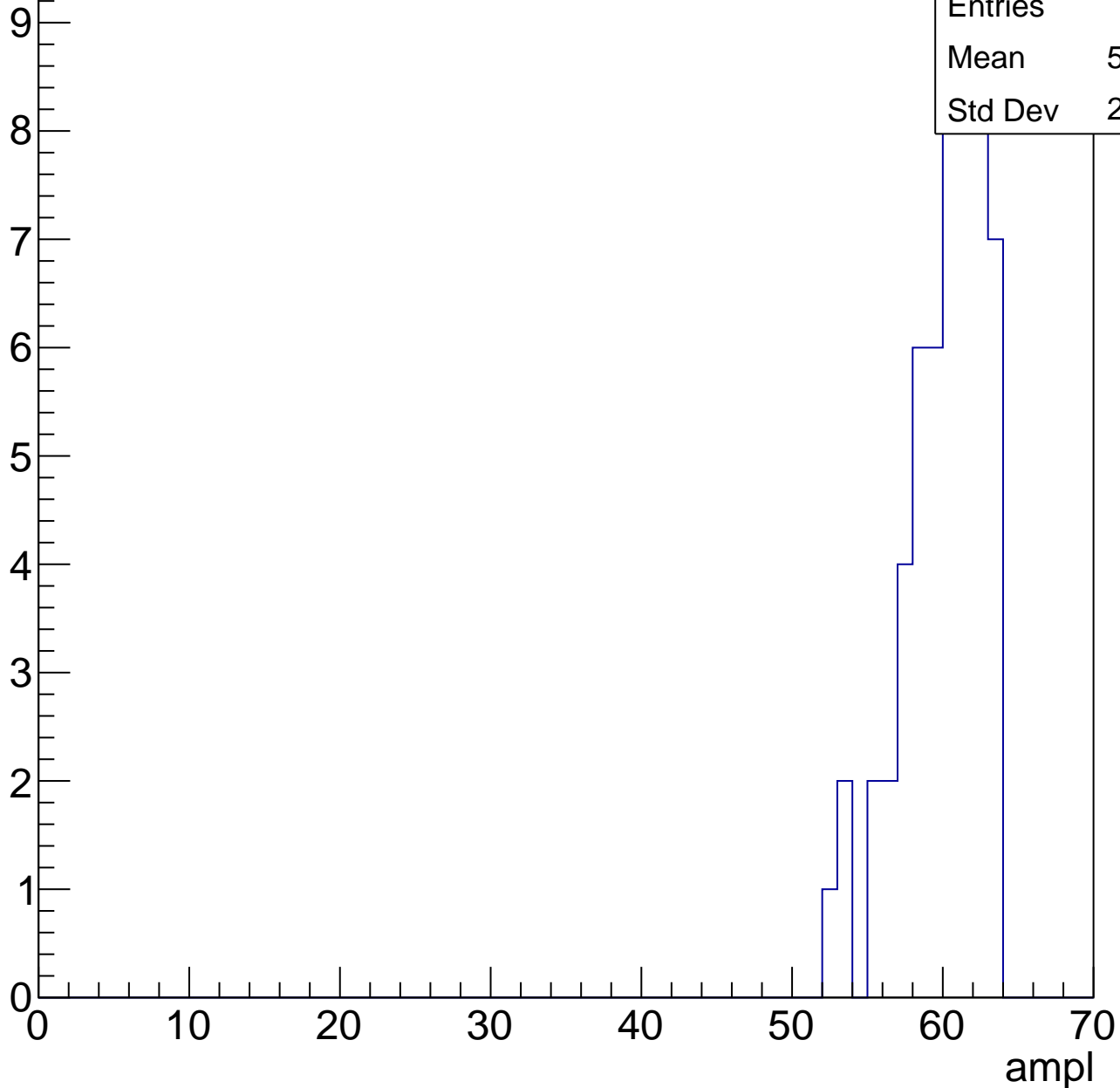
Entries	41
Mean	55.83
Std Dev	3.099



# B1L101S, U16-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

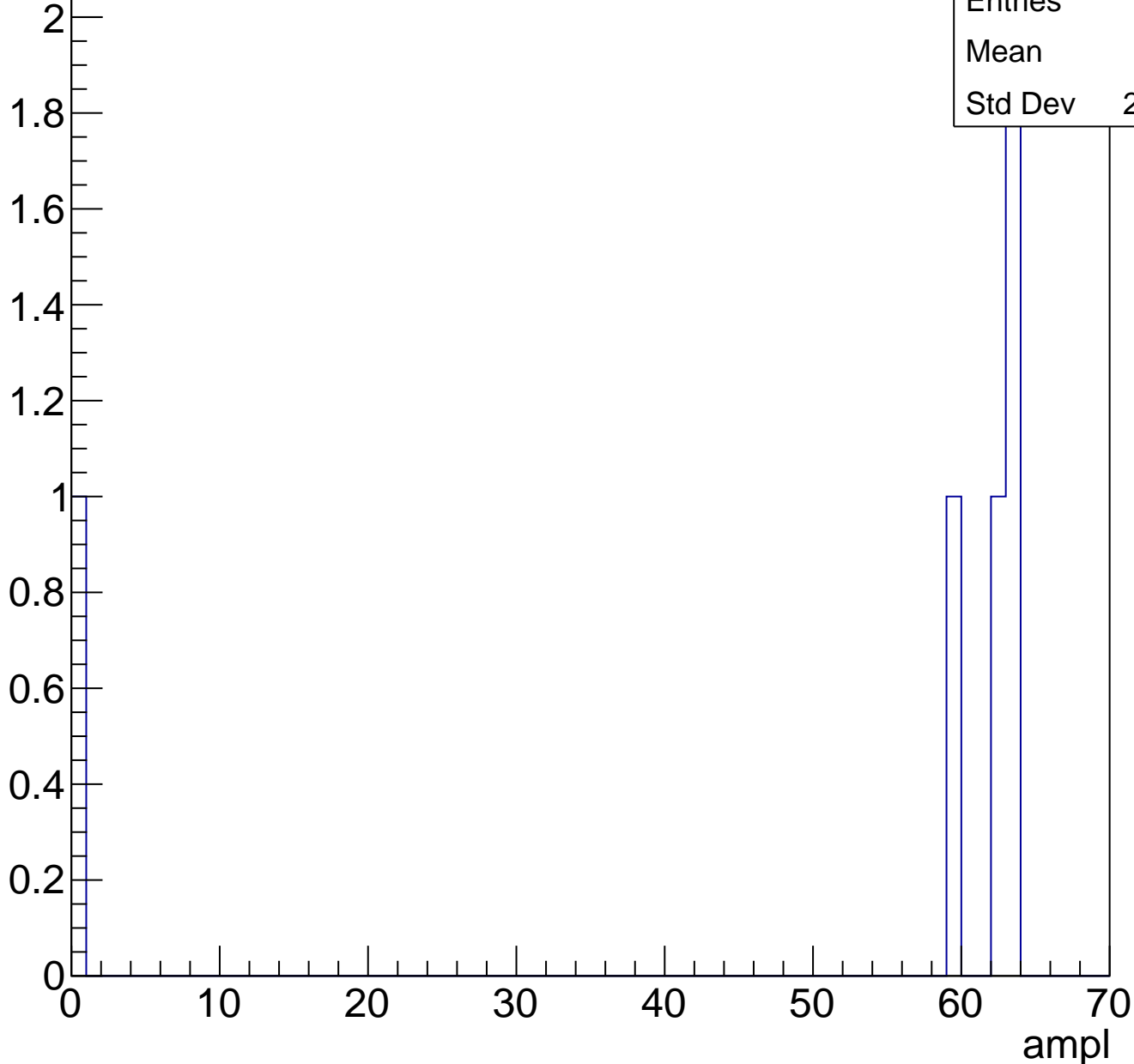
Entry



# B1L101S, U16-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U16-ch90, adc0

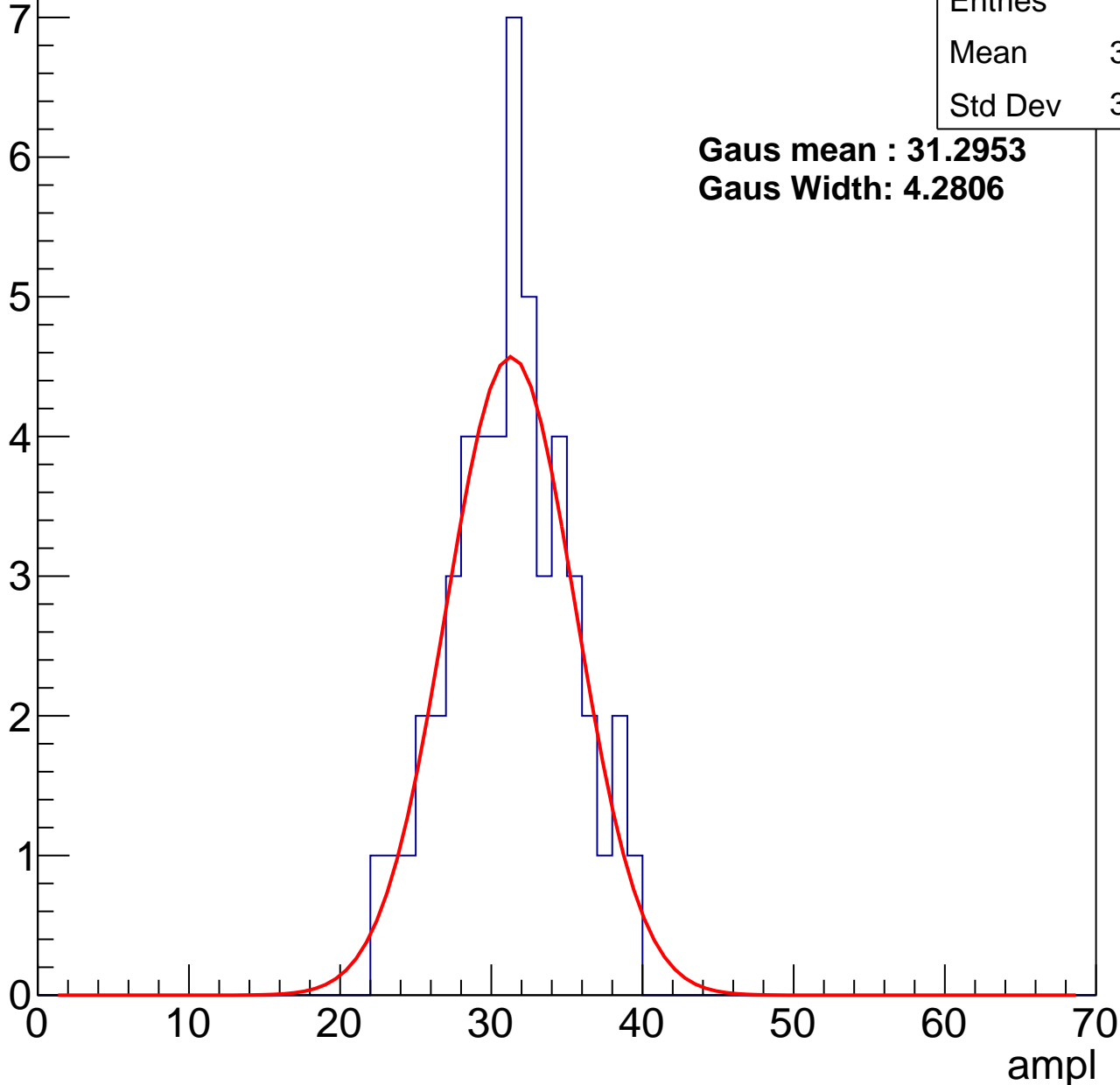
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	30.82
Std Dev	3.918

**Gaus mean : 31.2953**

**Gaus Width: 4.2806**



# B1L101S, U16-ch90, adc1

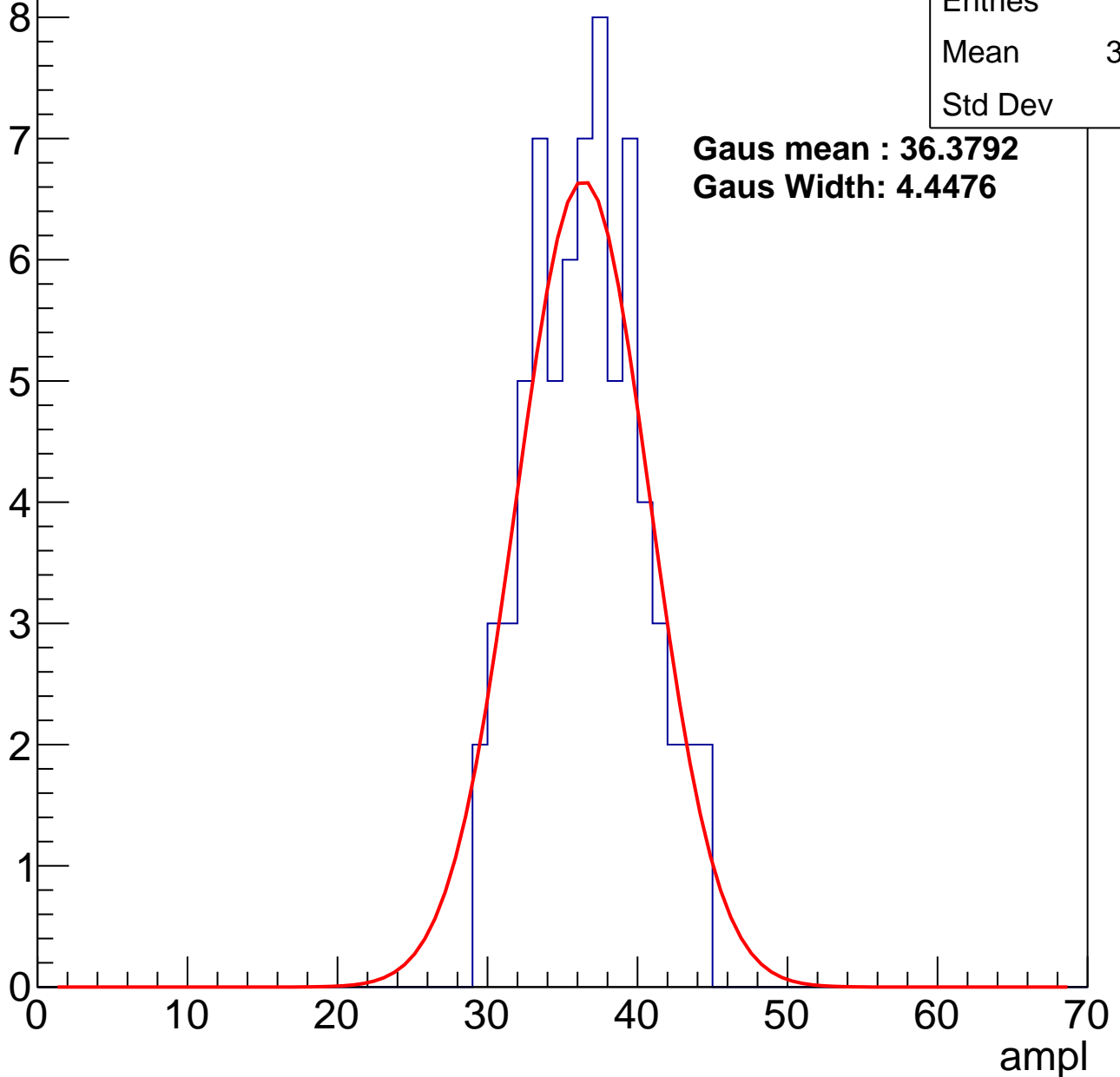
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	36.11
Std Dev	3.71

**Gaus mean : 36.3792**

**Gaus Width: 4.4476**



# B1L101S, U16-ch90, adc2

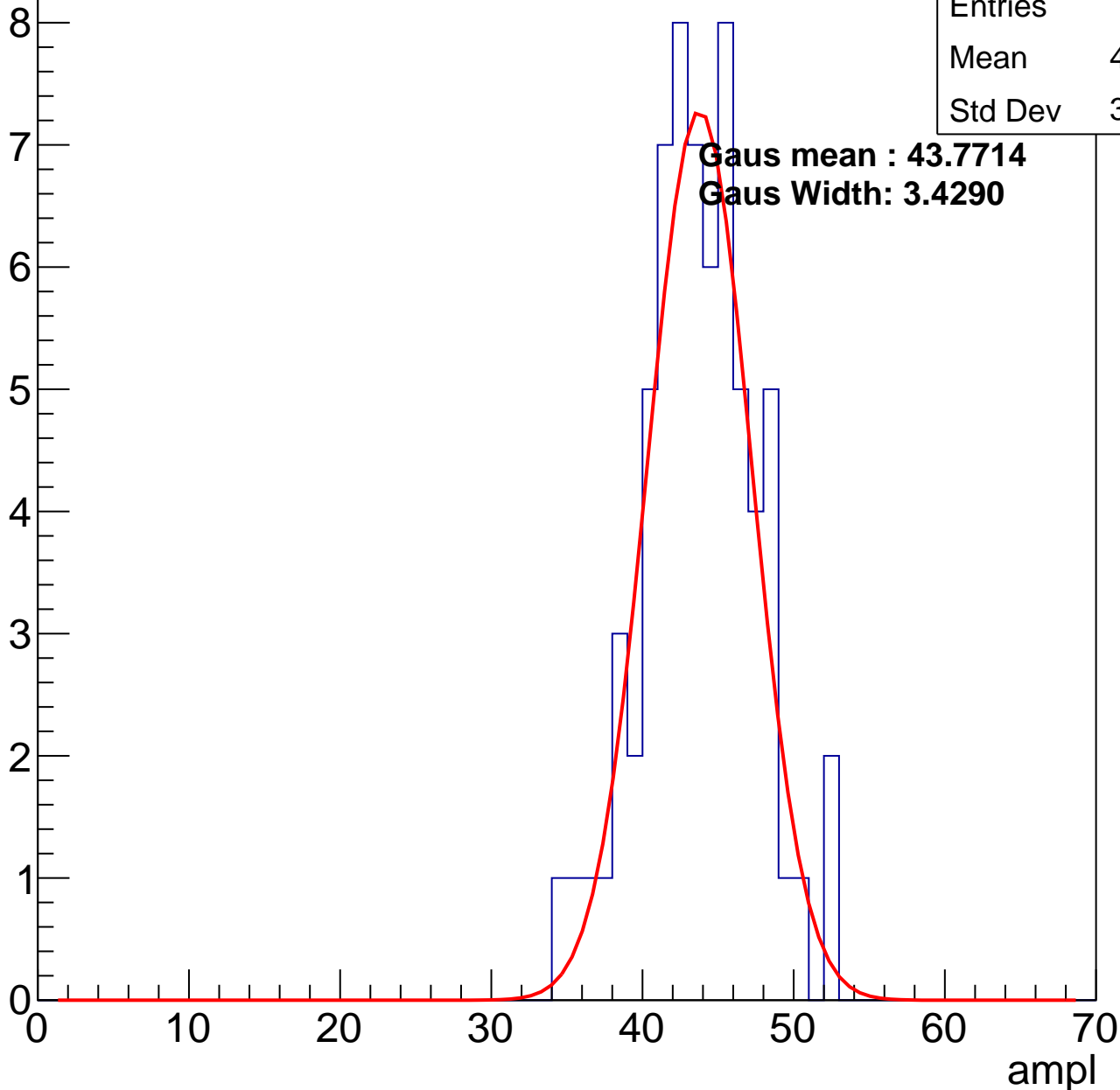
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	43.28
Std Dev	3.702

**Gaus mean : 43.7714**

**Gaus Width: 3.4290**

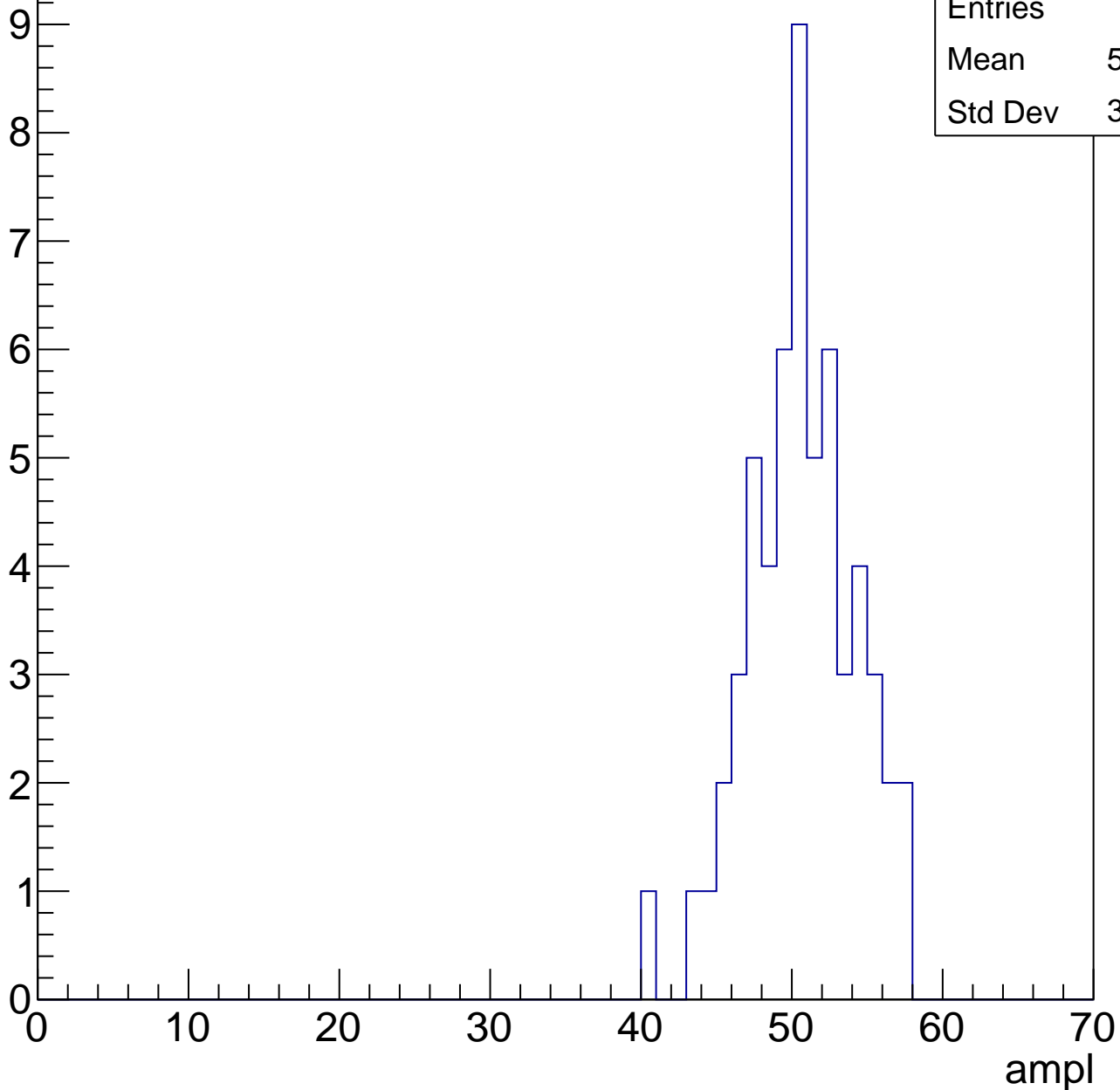


# B1L101S, U16-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	50.16
Std Dev	3.538

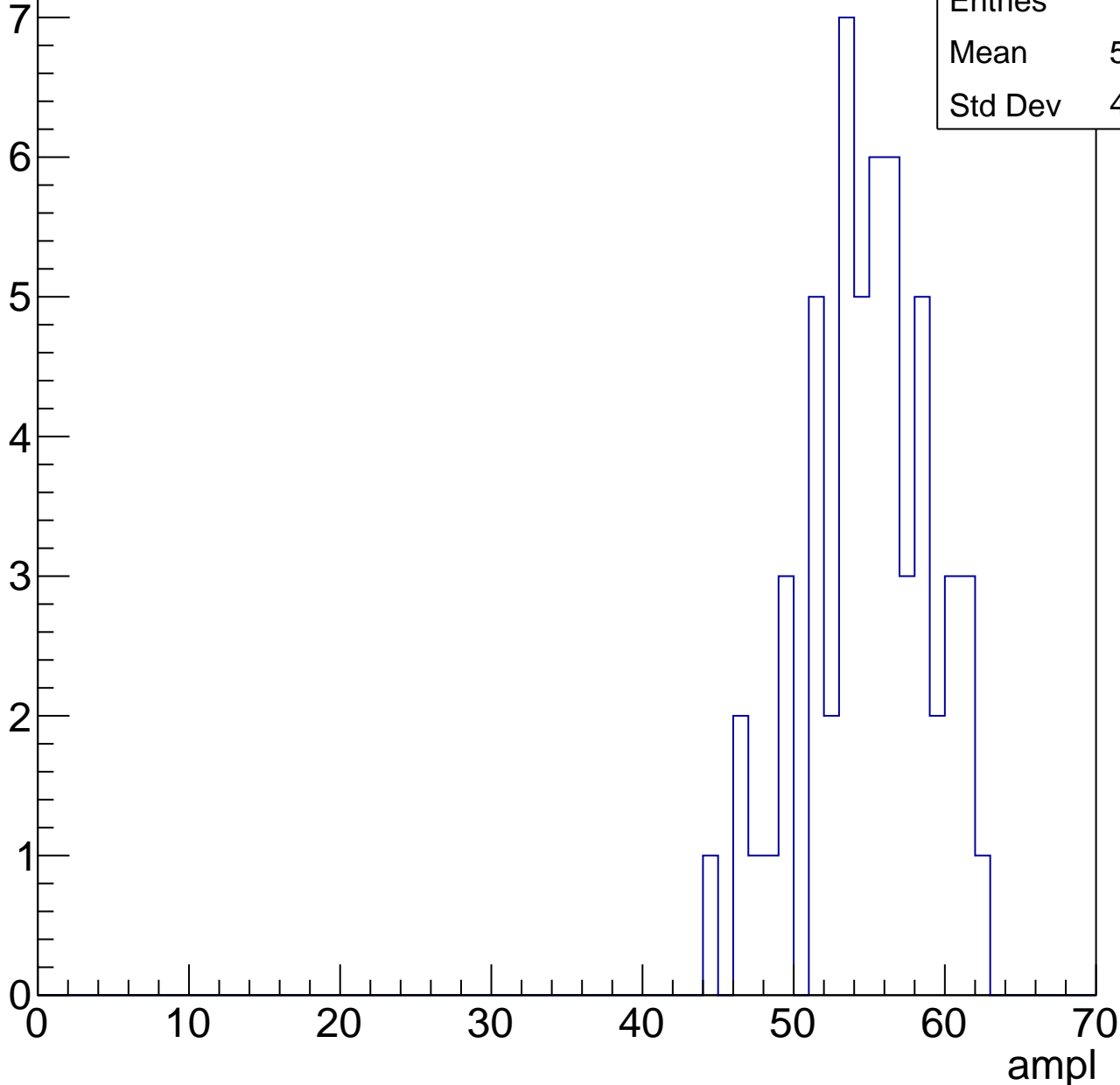


# B1L101S, U16-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

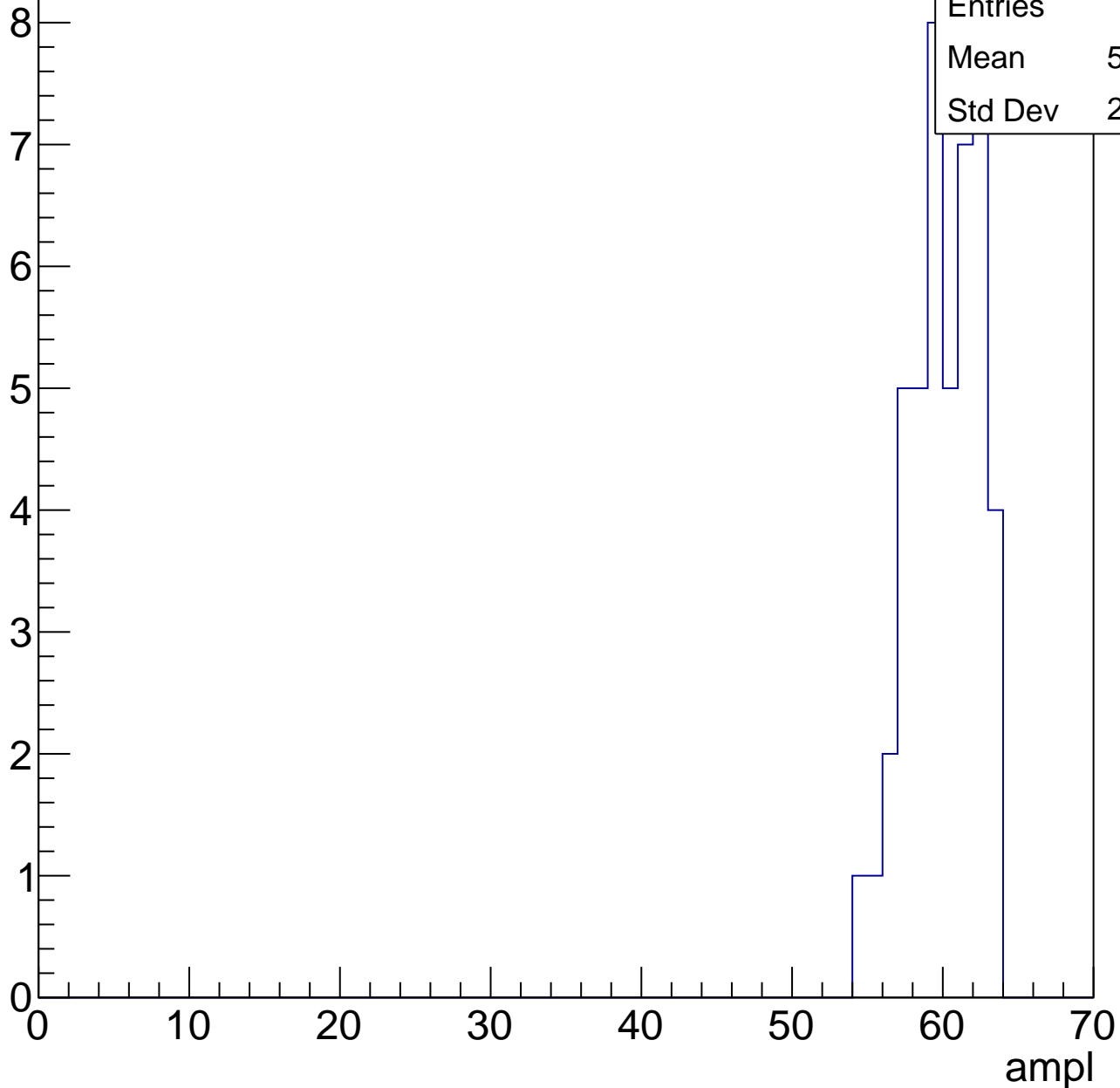
Entries	56
Mean	54.43
Std Dev	4.105



# B1L101S, U16-ch90, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

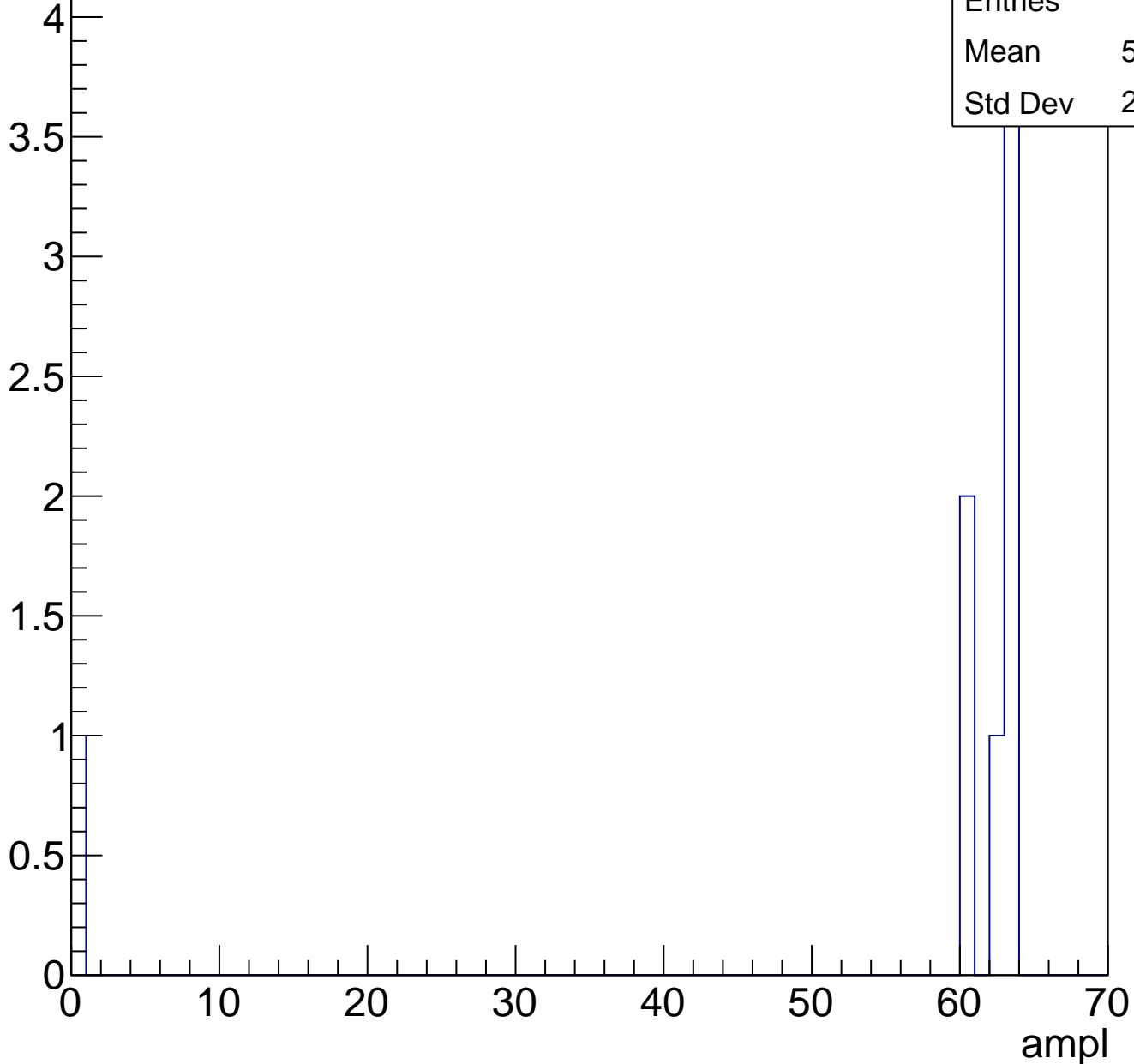
Entry



# B1L101S, U16-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

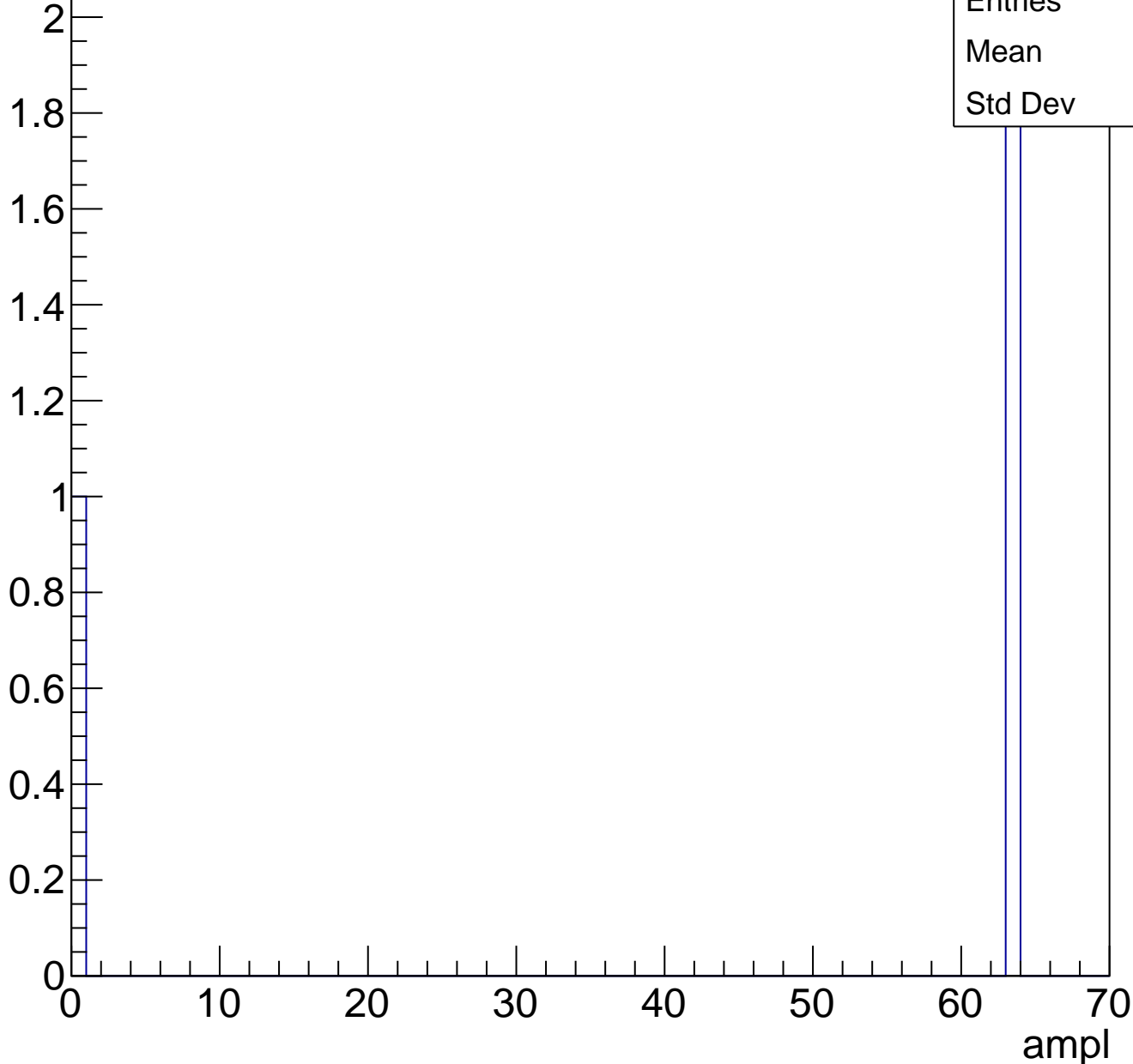




# B1L101S, U16-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch91, adc0

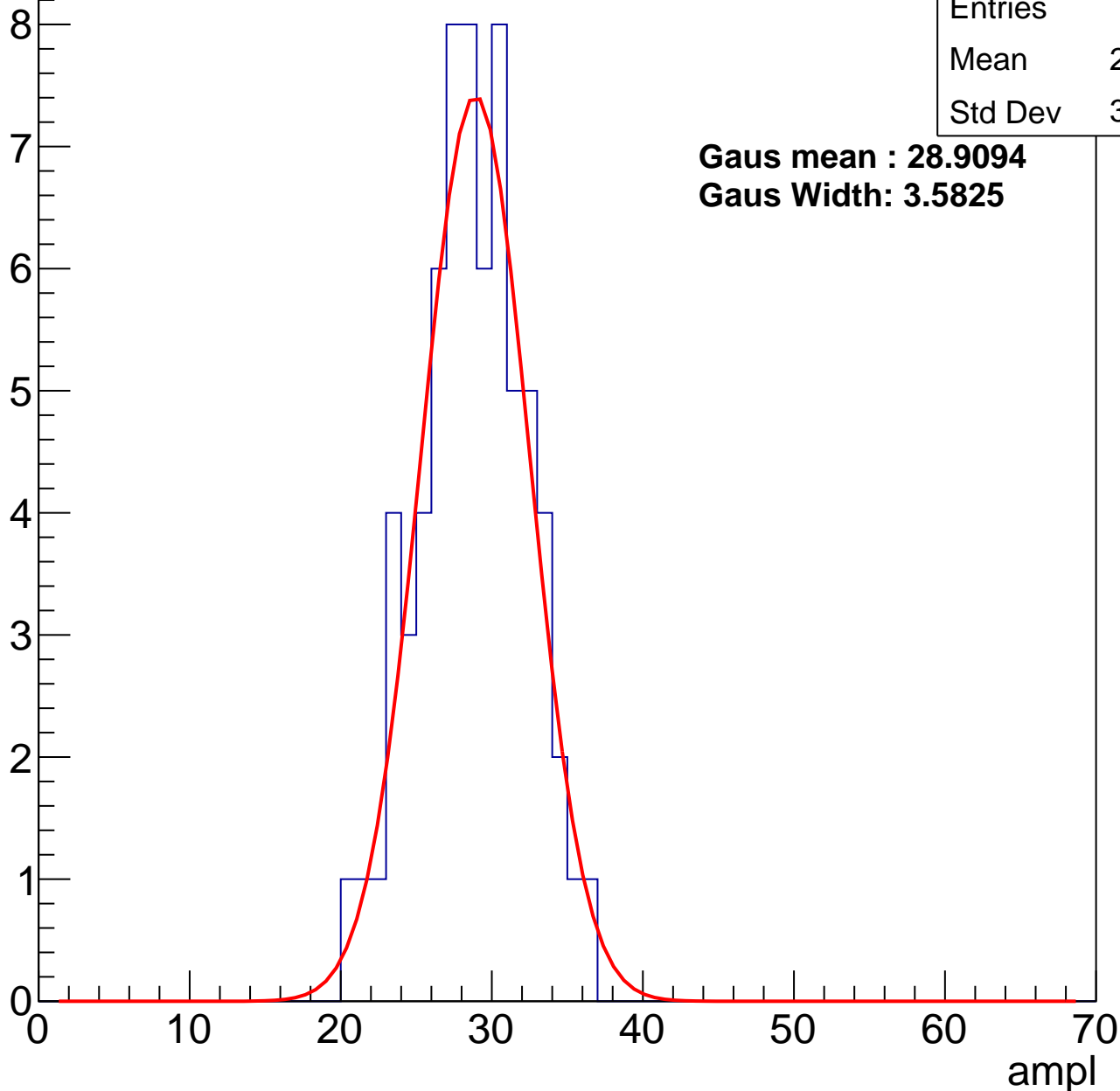
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	28.28
Std Dev	3.446

**Gaus mean : 28.9094**

**Gaus Width: 3.5825**



# B1L101S, U16-ch91, adc1

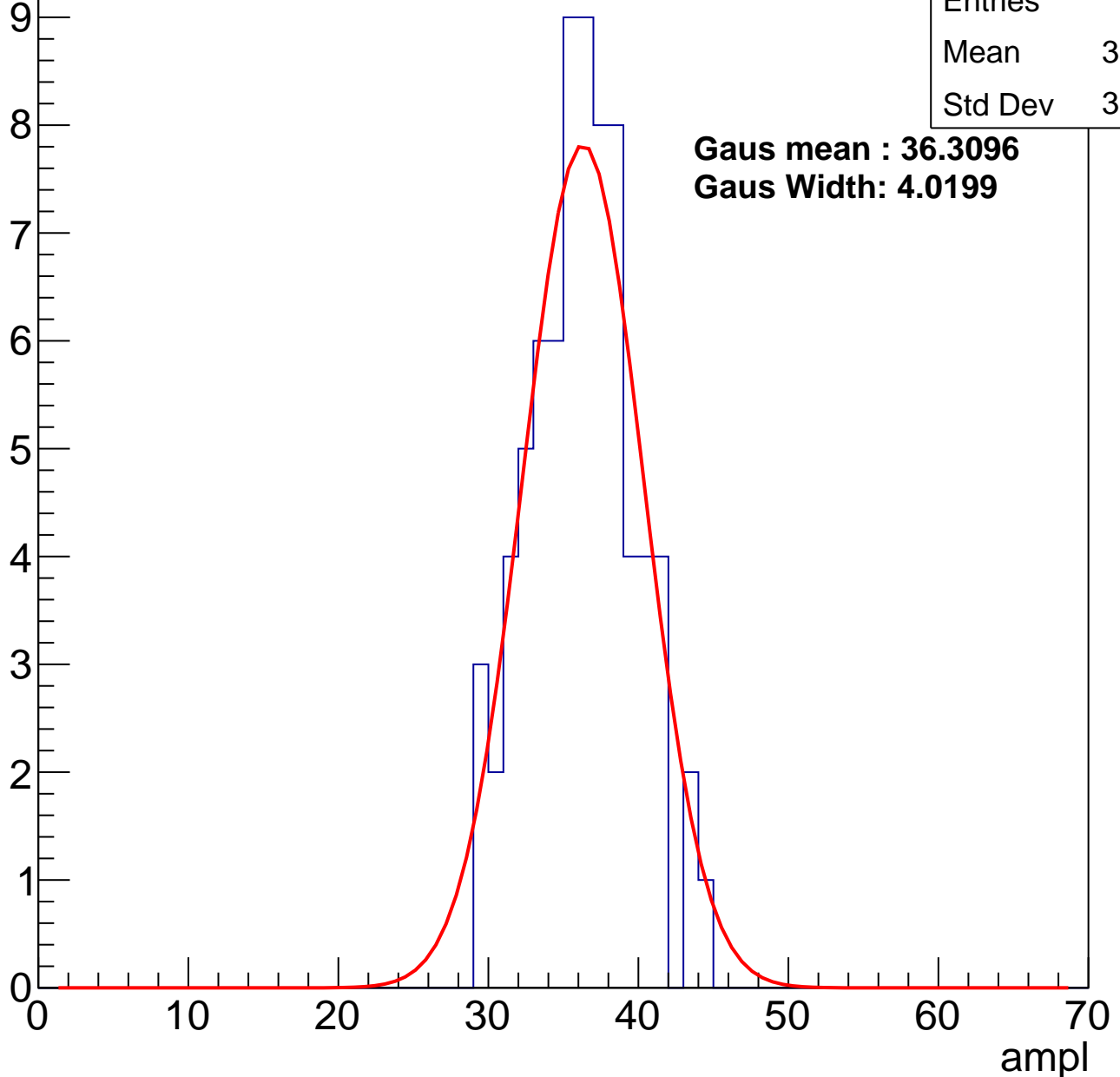
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	35.76
Std Dev	3.433

**Gaus mean : 36.3096**

**Gaus Width: 4.0199**



# B1L101S, U16-ch91, adc2

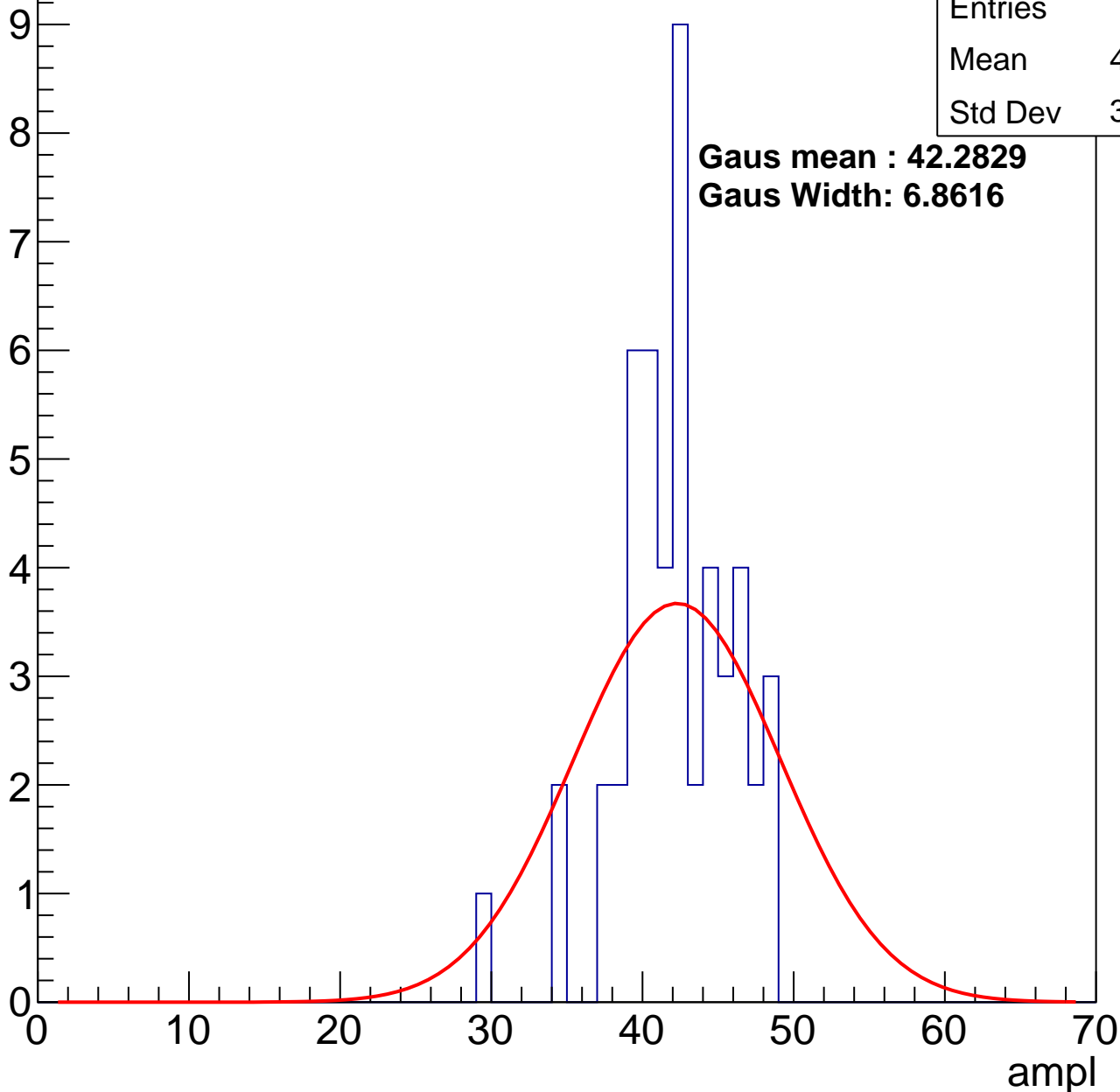
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	41.64
Std Dev	3.799

**Gaus mean : 42.2829**

**Gaus Width: 6.8616**

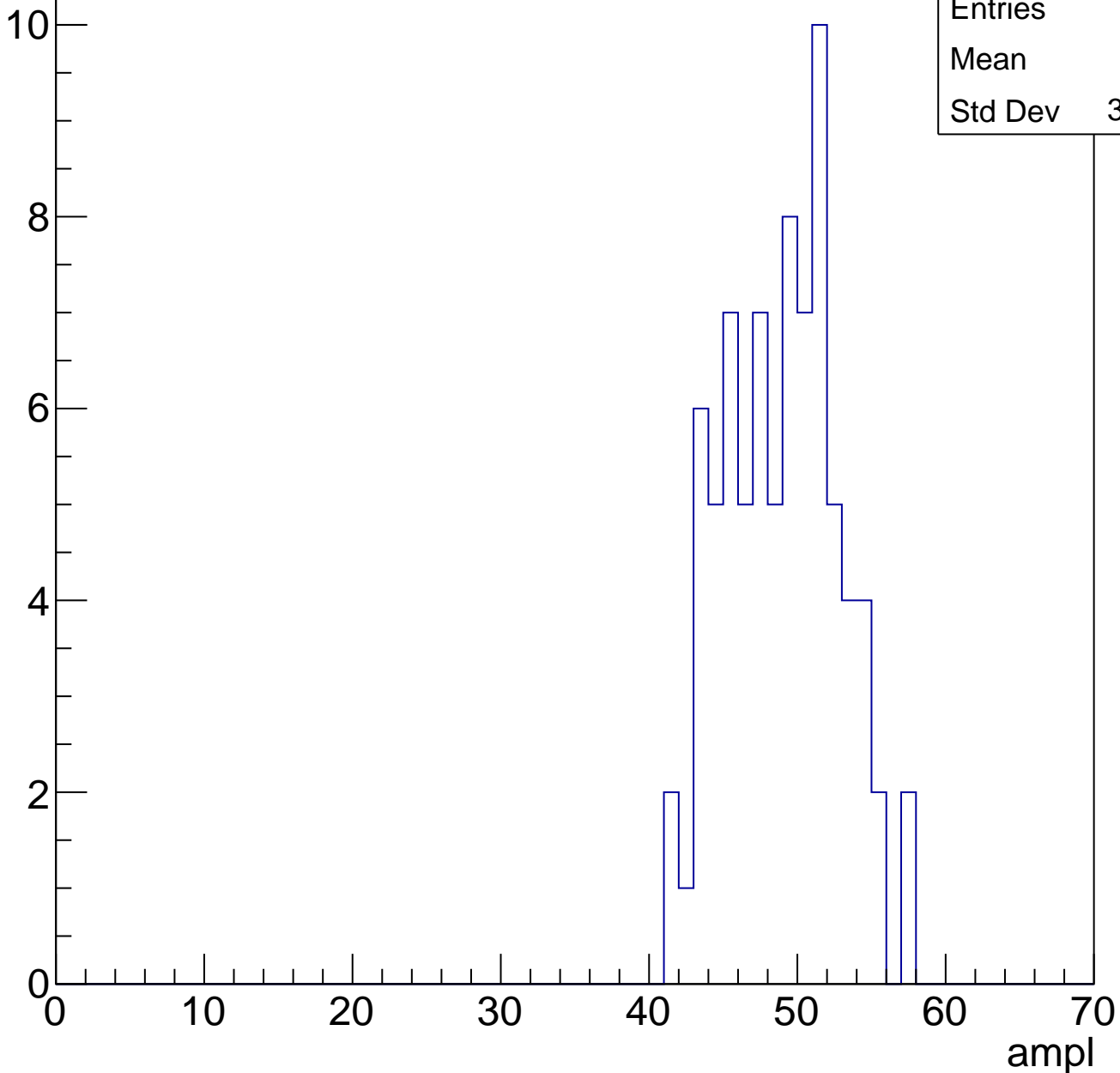


# B1L101S, U16-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

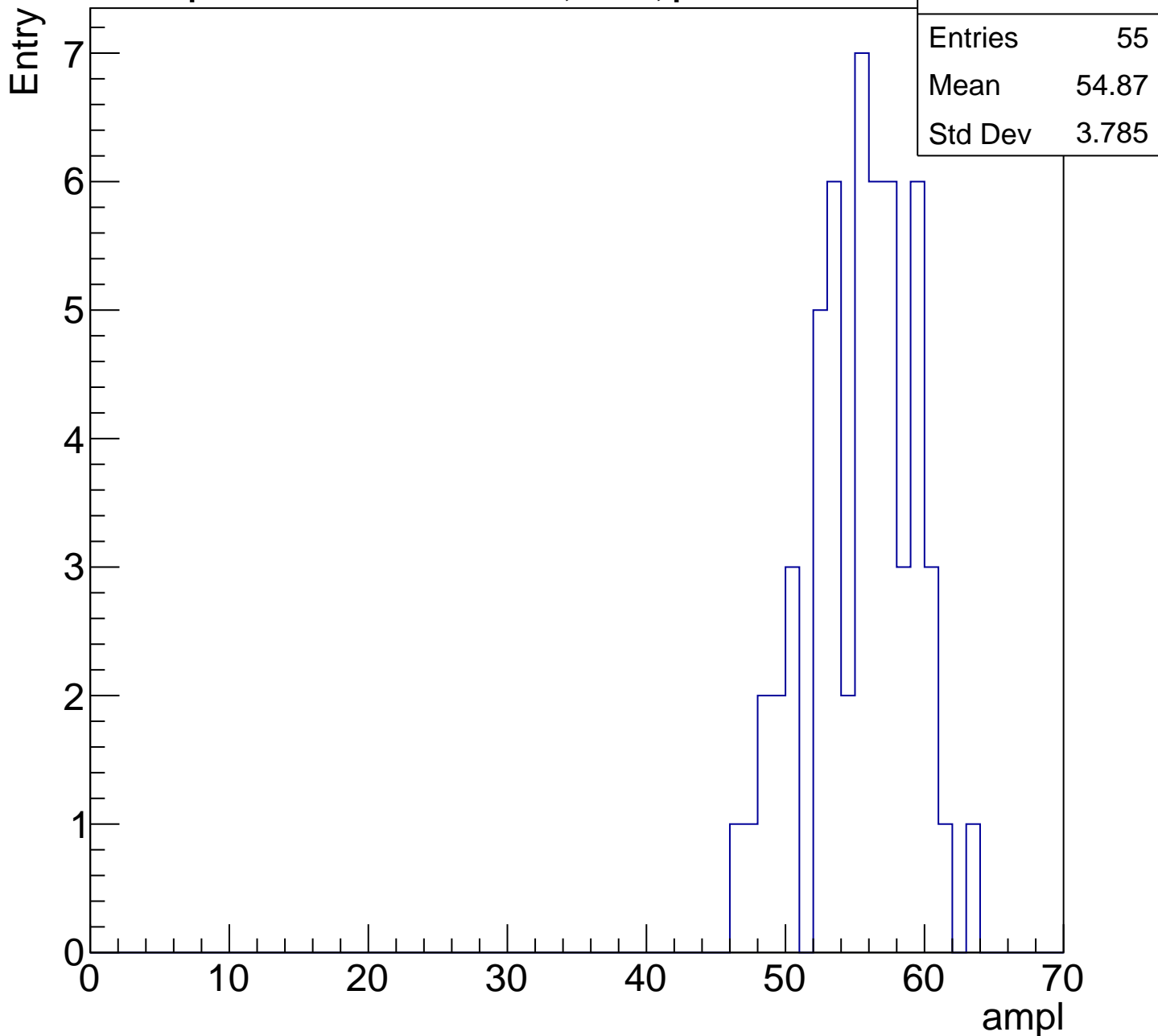
Entry

Entries	80
Mean	48.5
Std Dev	3.782



# B1L101S, U16-ch91, adc4

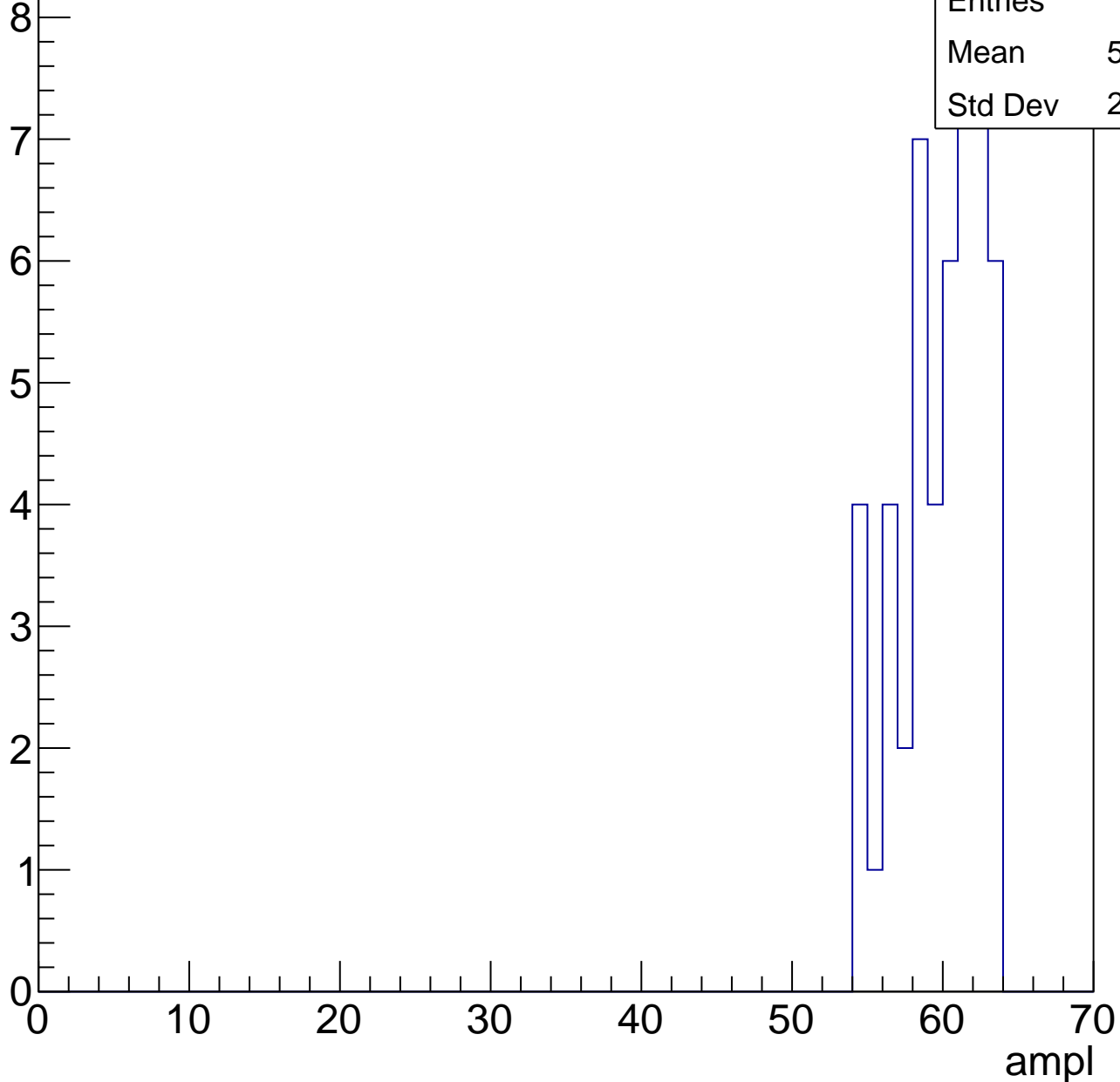
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U16-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



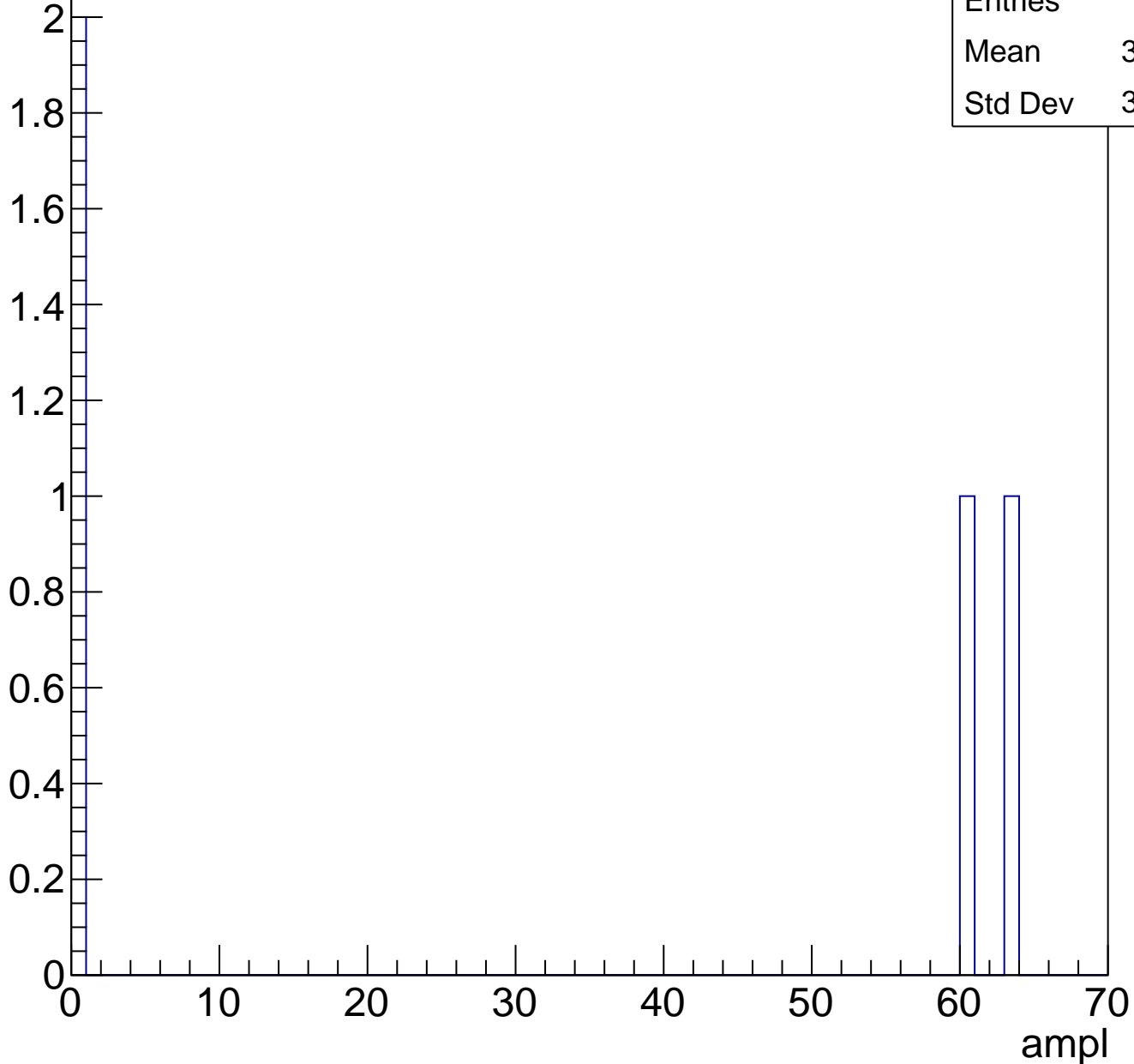
Entries	6
Mean	51.83
Std Dev	23.19



# B1L101S, U16-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	4
Mean	30.75
Std Dev	30.77

# B1L101S, U16-ch92, adc0

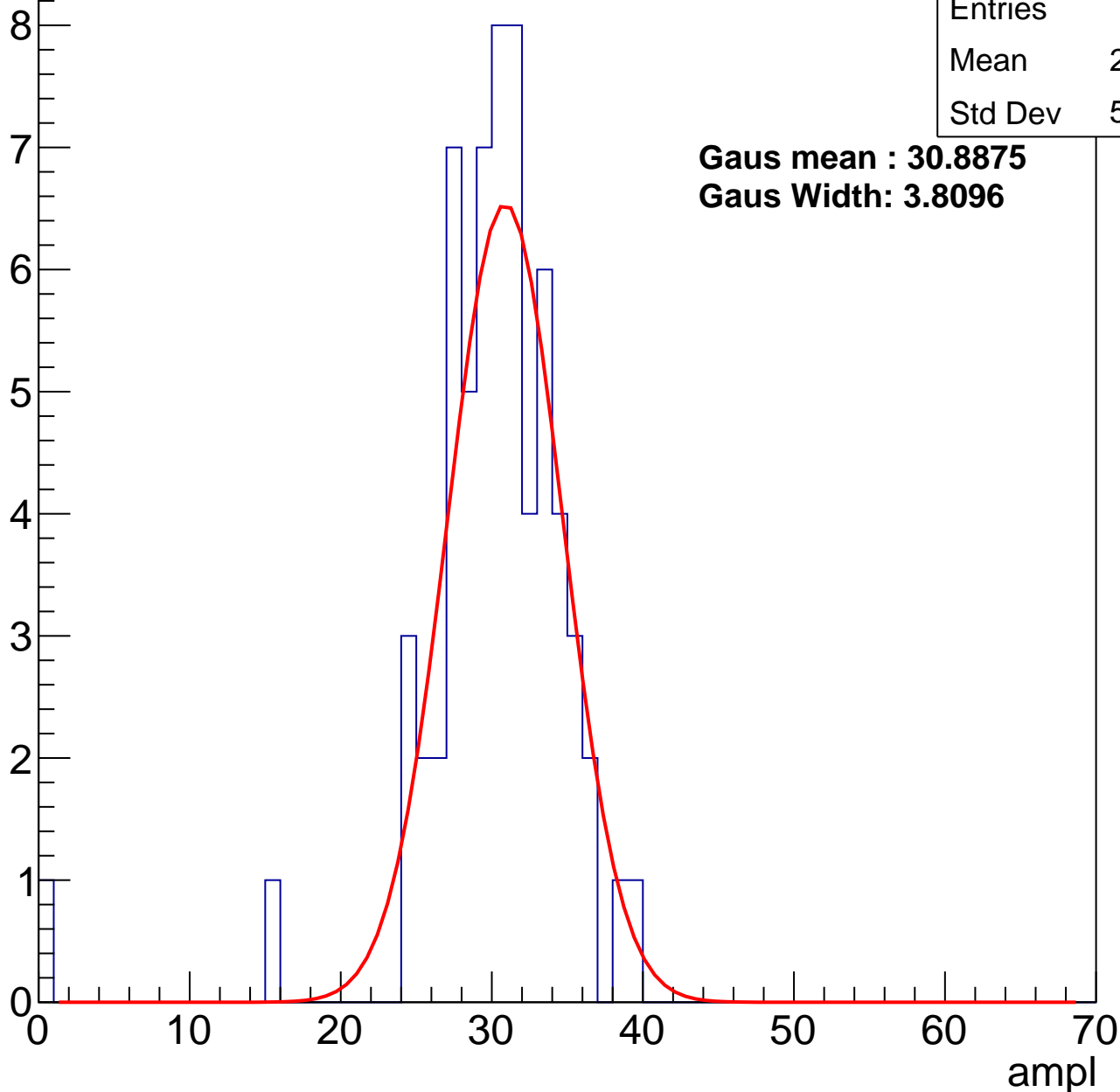
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	29.62
Std Dev	5.305

**Gaus mean : 30.8875**

**Gaus Width: 3.8096**



# B1L101S, U16-ch92, adc1

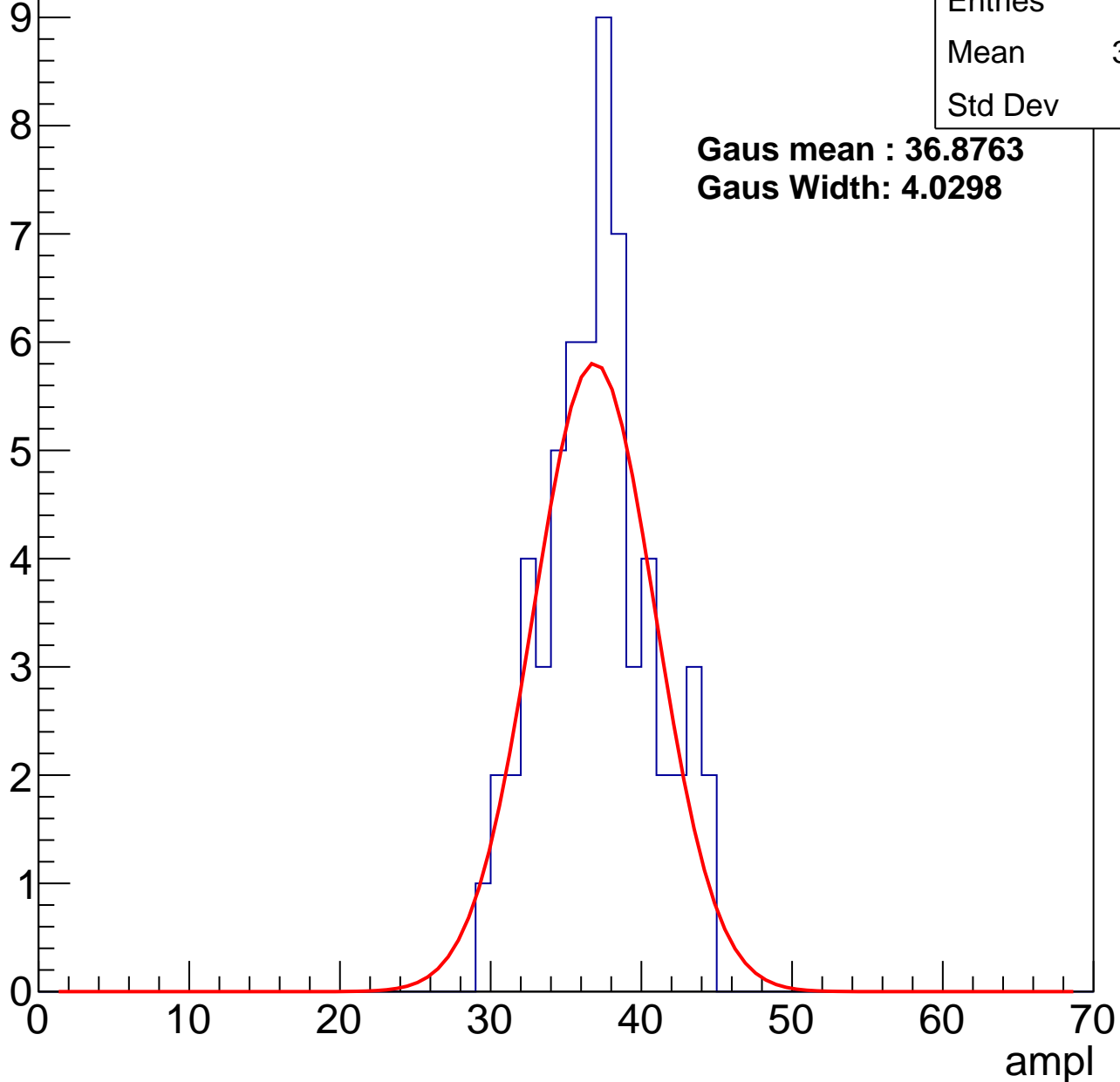
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	36.61
Std Dev	3.6

**Gaus mean : 36.8763**

**Gaus Width: 4.0298**



# B1L101S, U16-ch92, adc2

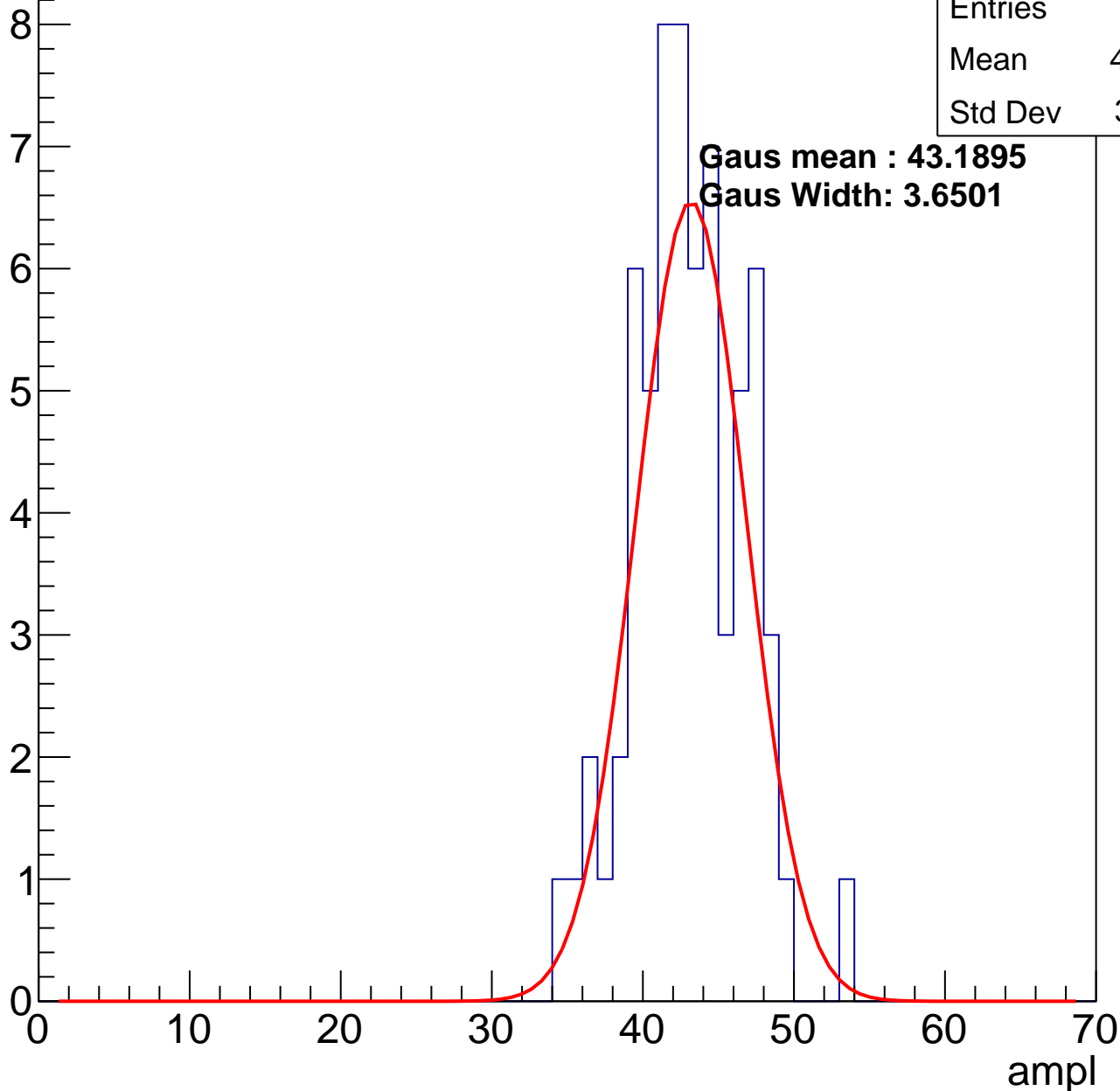
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	42.59
Std Dev	3.631

**Gaus mean : 43.1895**

**Gaus Width: 3.6501**

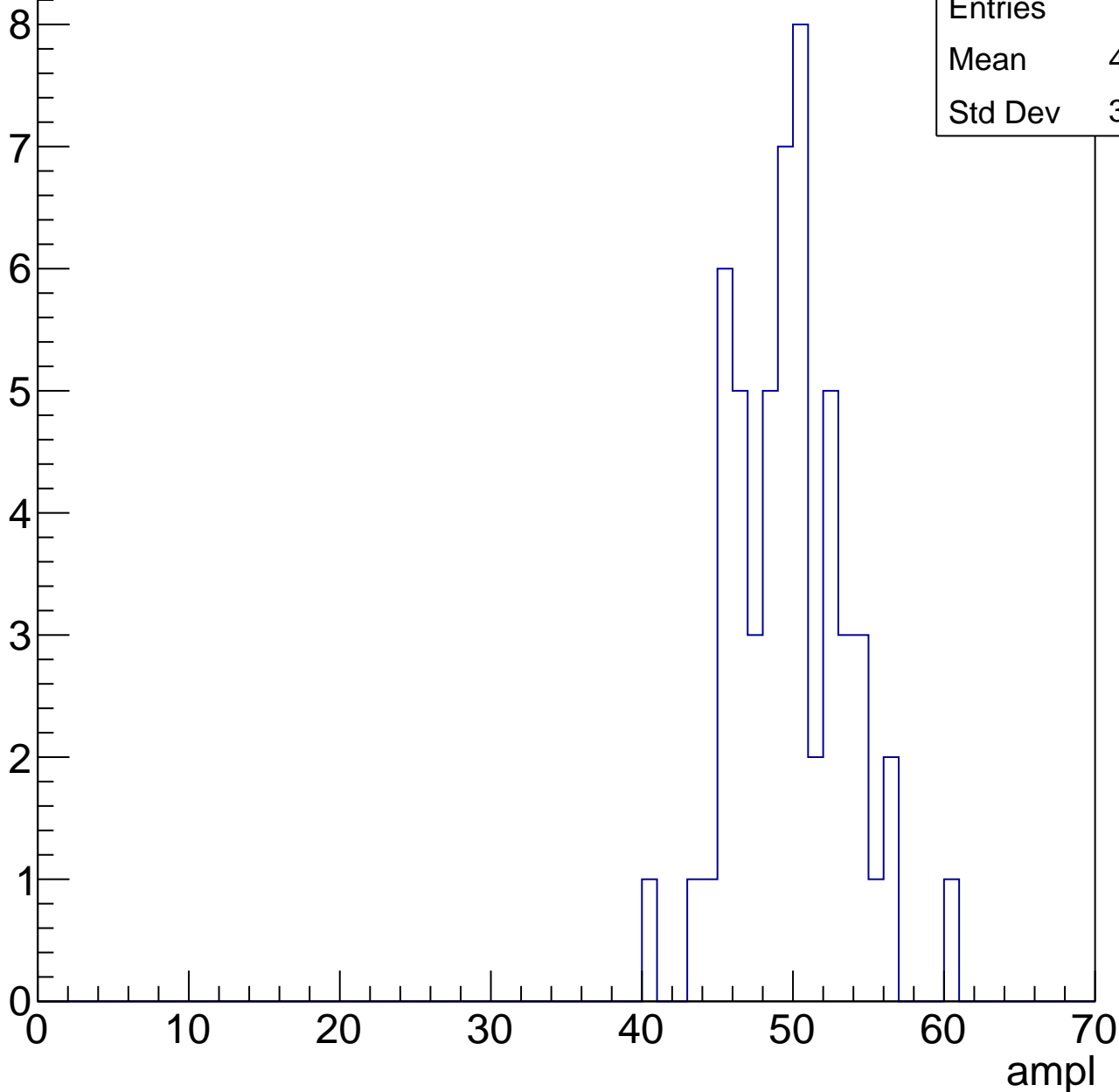


# B1L101S, U16-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	49.28
Std Dev	3.689

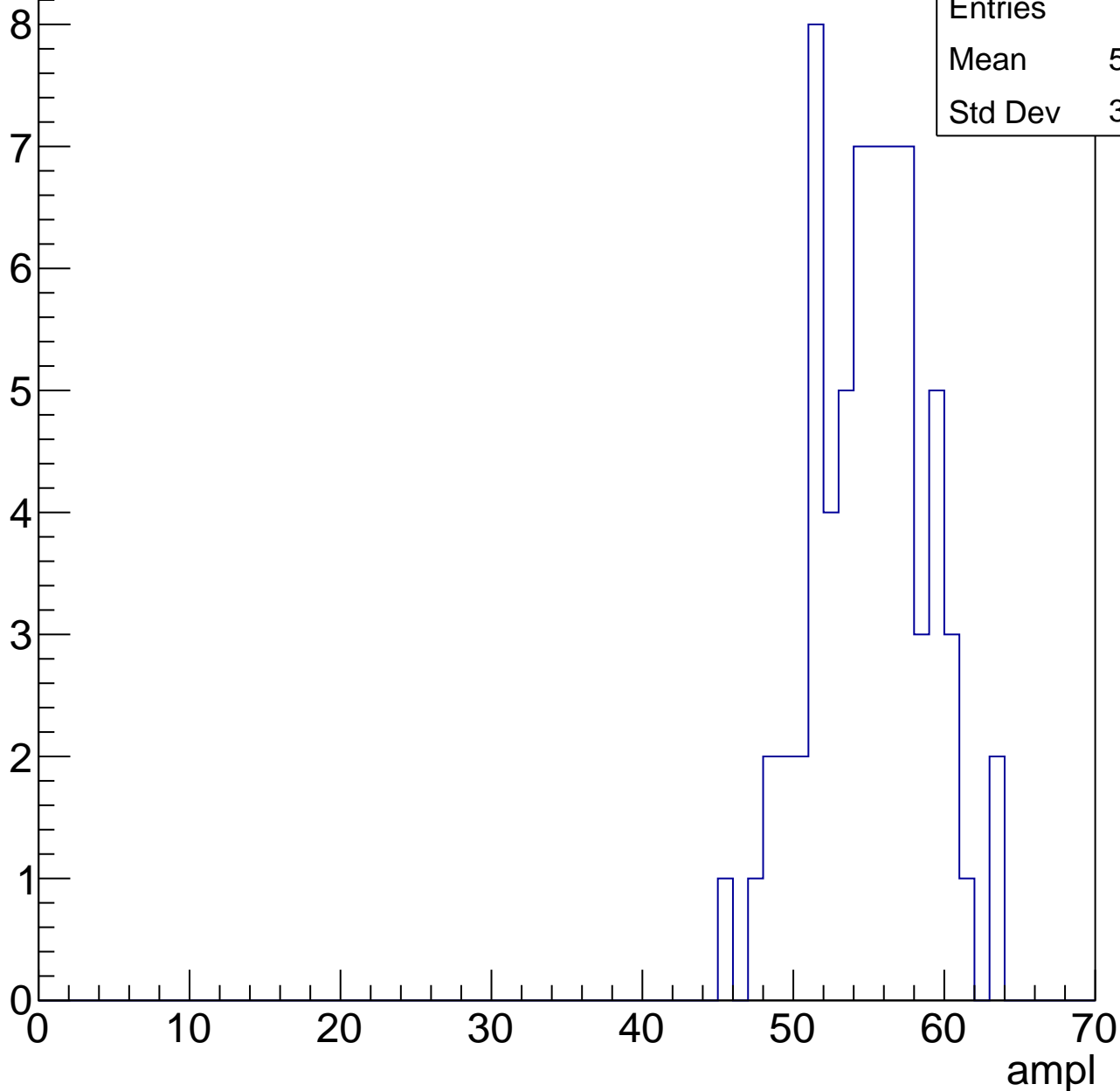


# B1L101S, U16-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	54.58
Std Dev	3.754

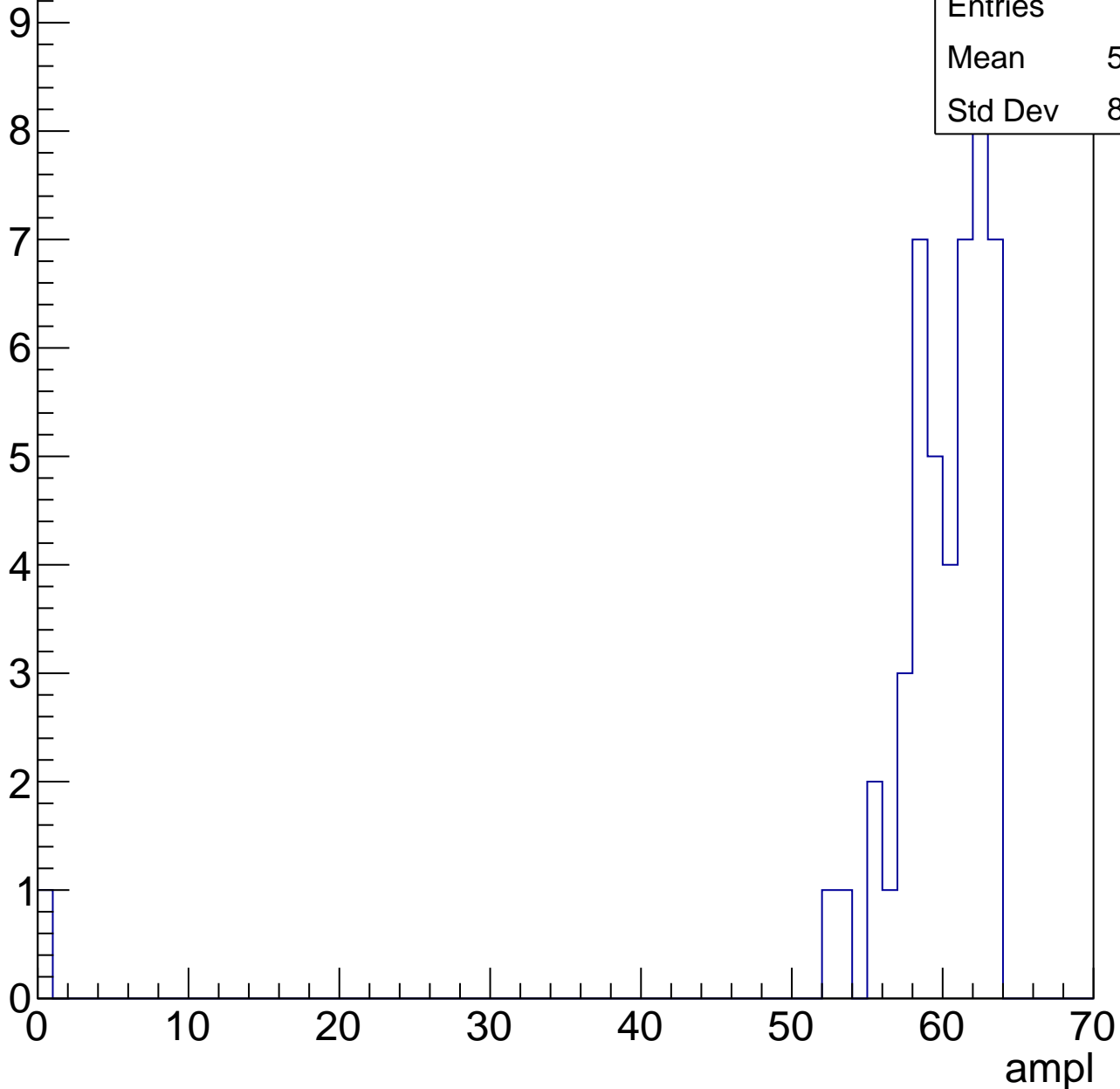


# B1L101S, U16-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	58.52
Std Dev	8.944



# B1L101S, U16-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	61.17
Std Dev	1.067

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U16-ch93, adc0

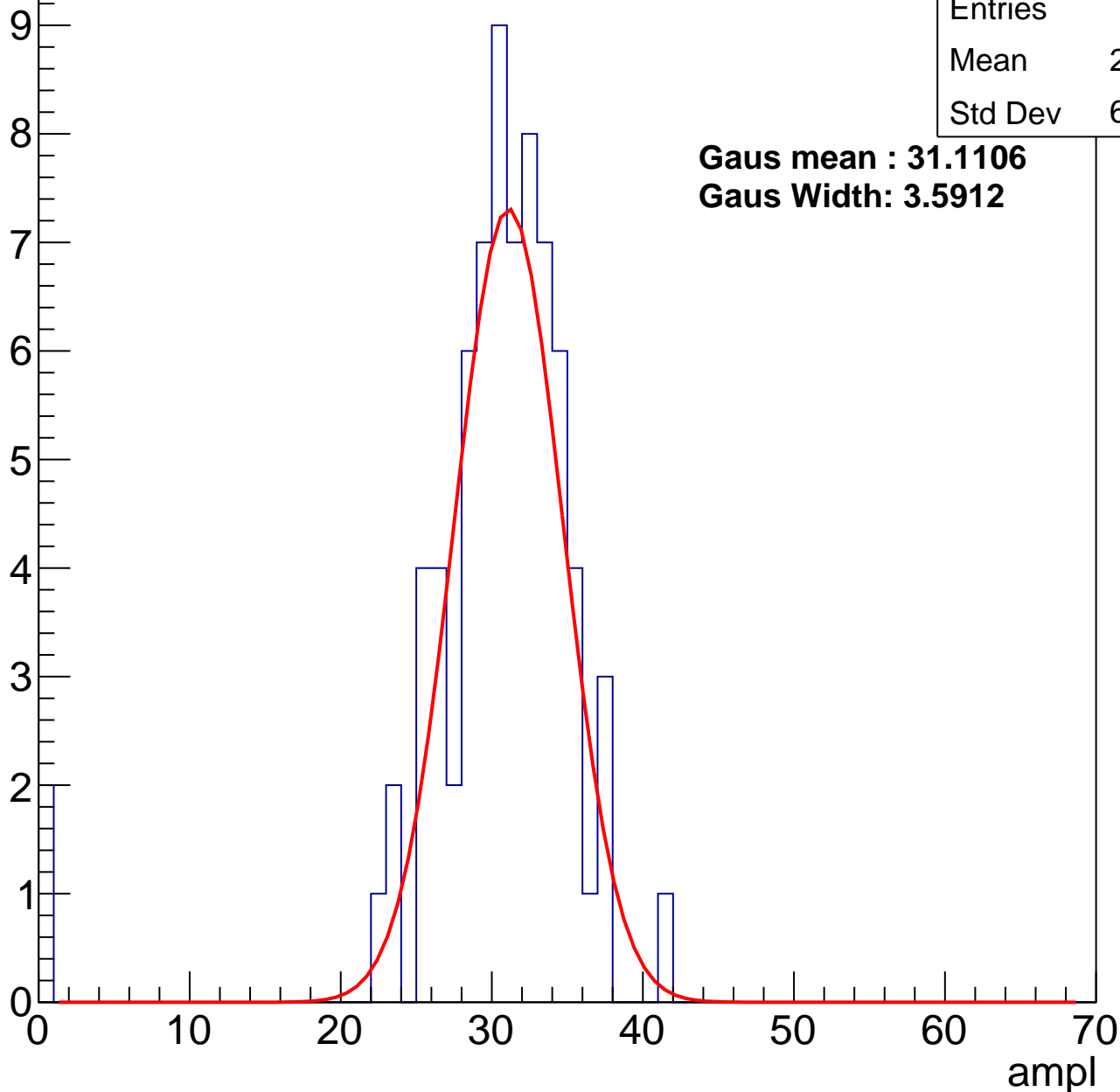
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	29.77
Std Dev	6.122

**Gaus mean : 31.1106**

**Gaus Width: 3.5912**



# B1L101S, U16-ch93, adc1

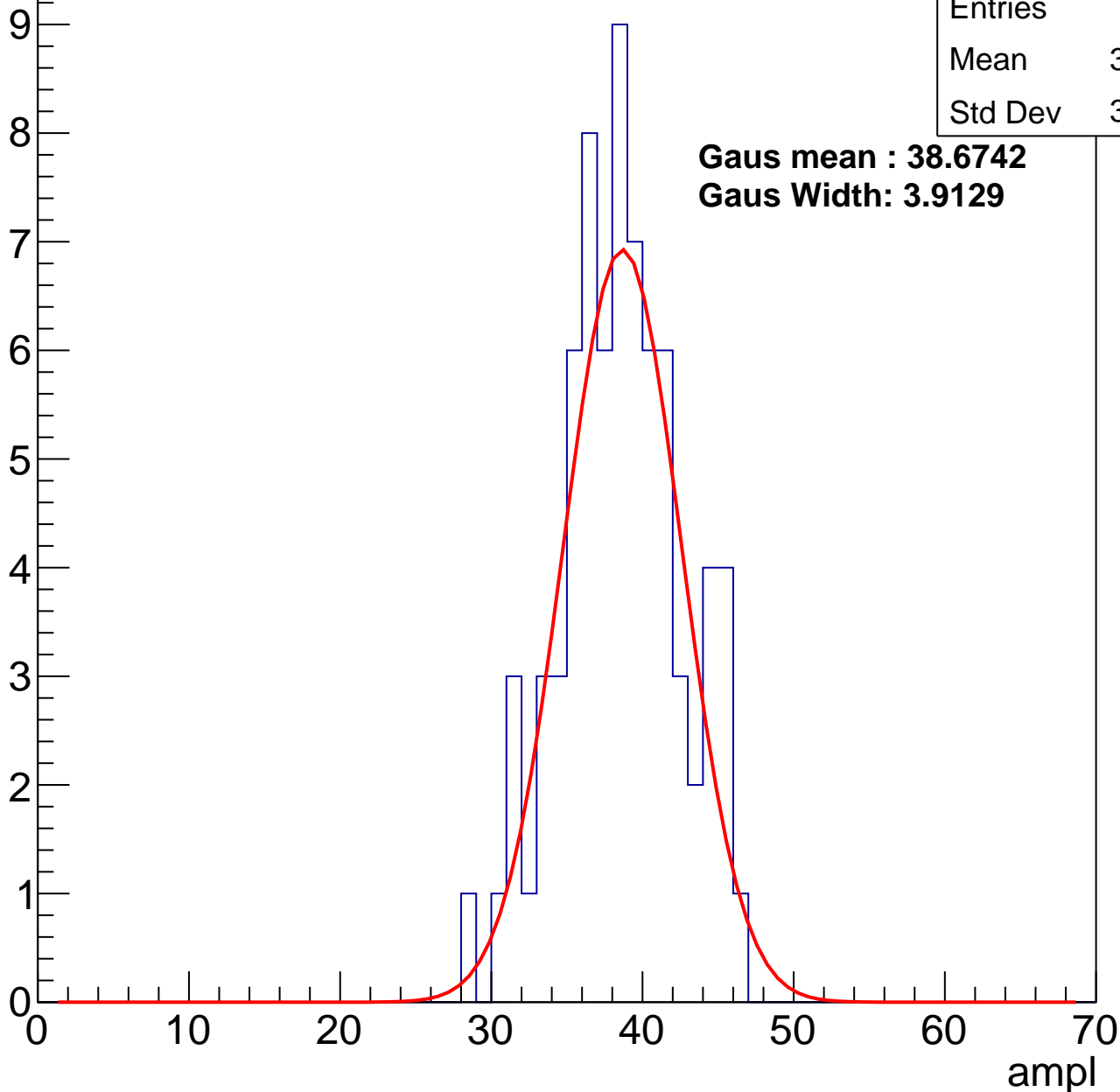
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	38.09
Std Dev	3.939

**Gaus mean : 38.6742**

**Gaus Width: 3.9129**



# B1L101S, U16-ch93, adc2

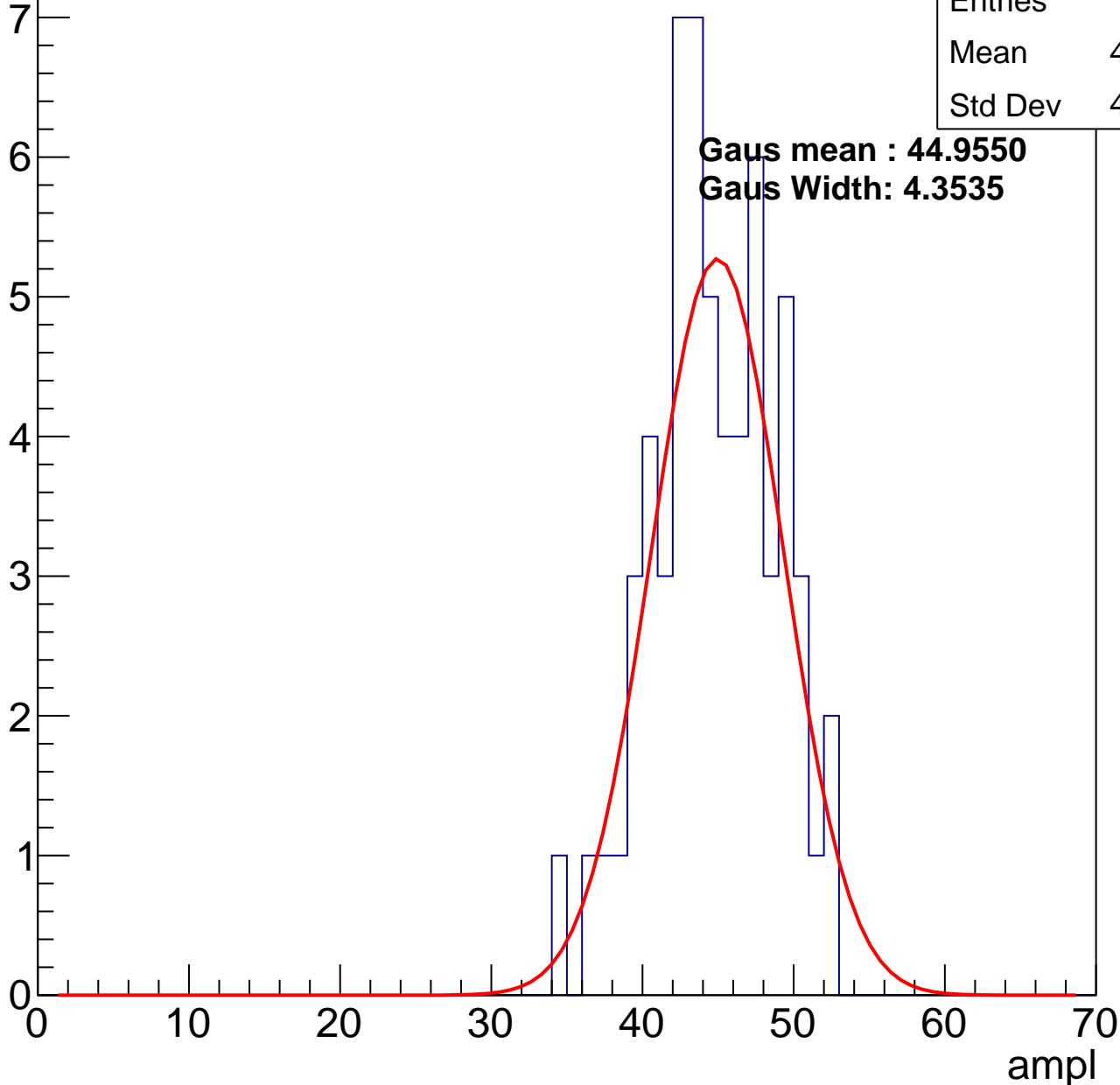
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	44.26
Std Dev	4.004

**Gaus mean : 44.9550**

**Gaus Width: 4.3535**

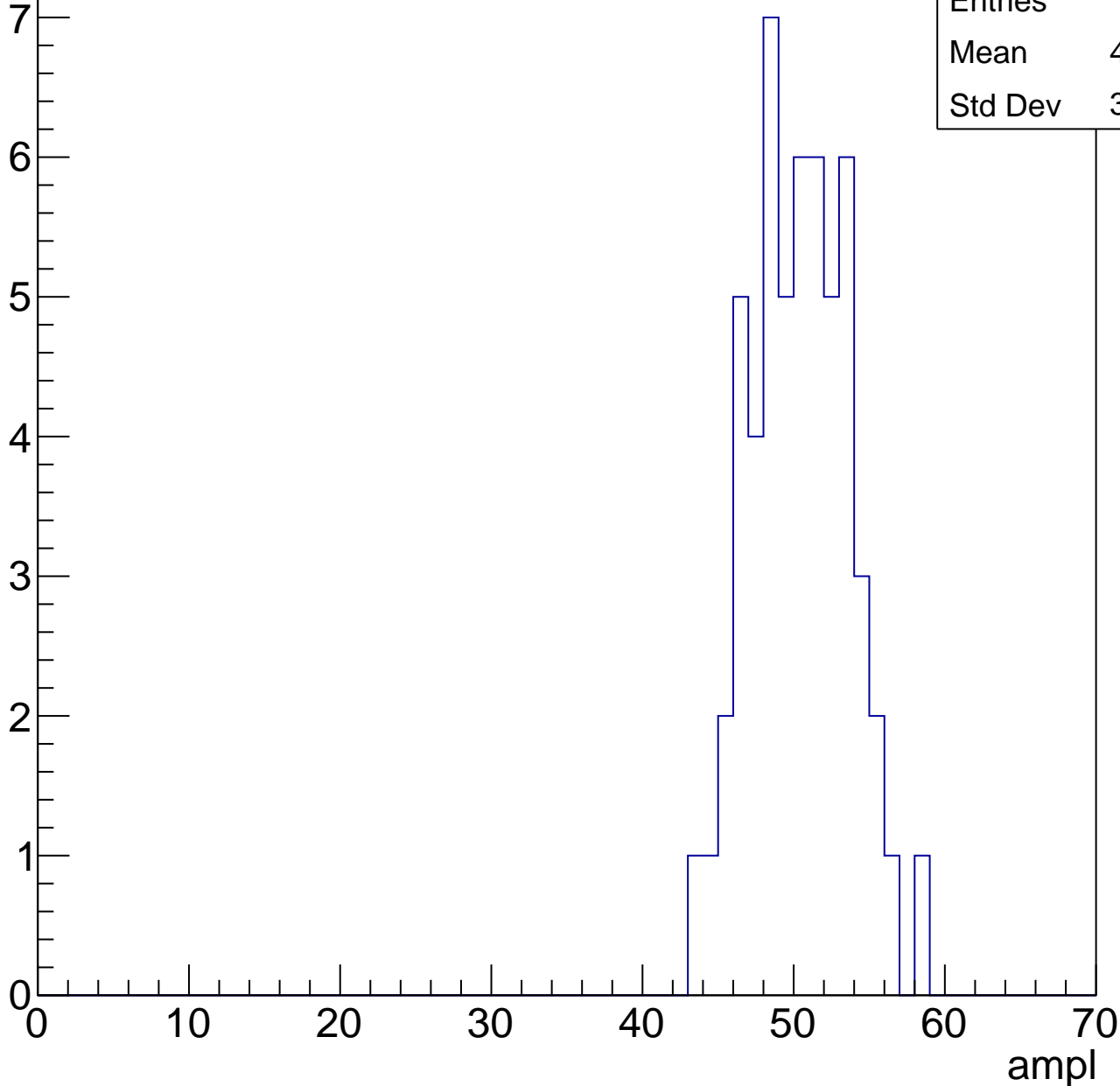


# B1L101S, U16-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	49.93
Std Dev	3.196

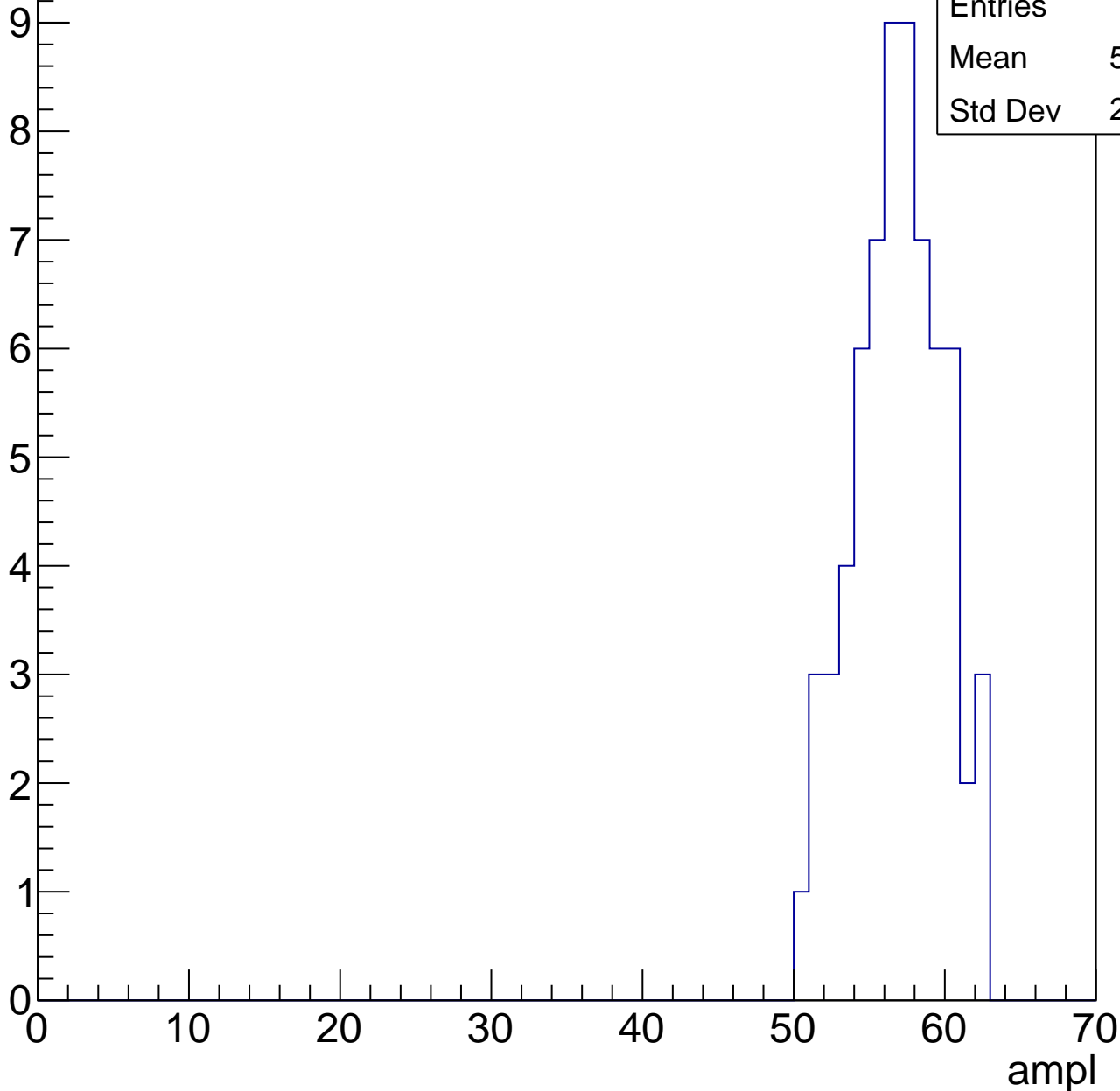


# B1L101S, U16-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	56.44
Std Dev	2.908

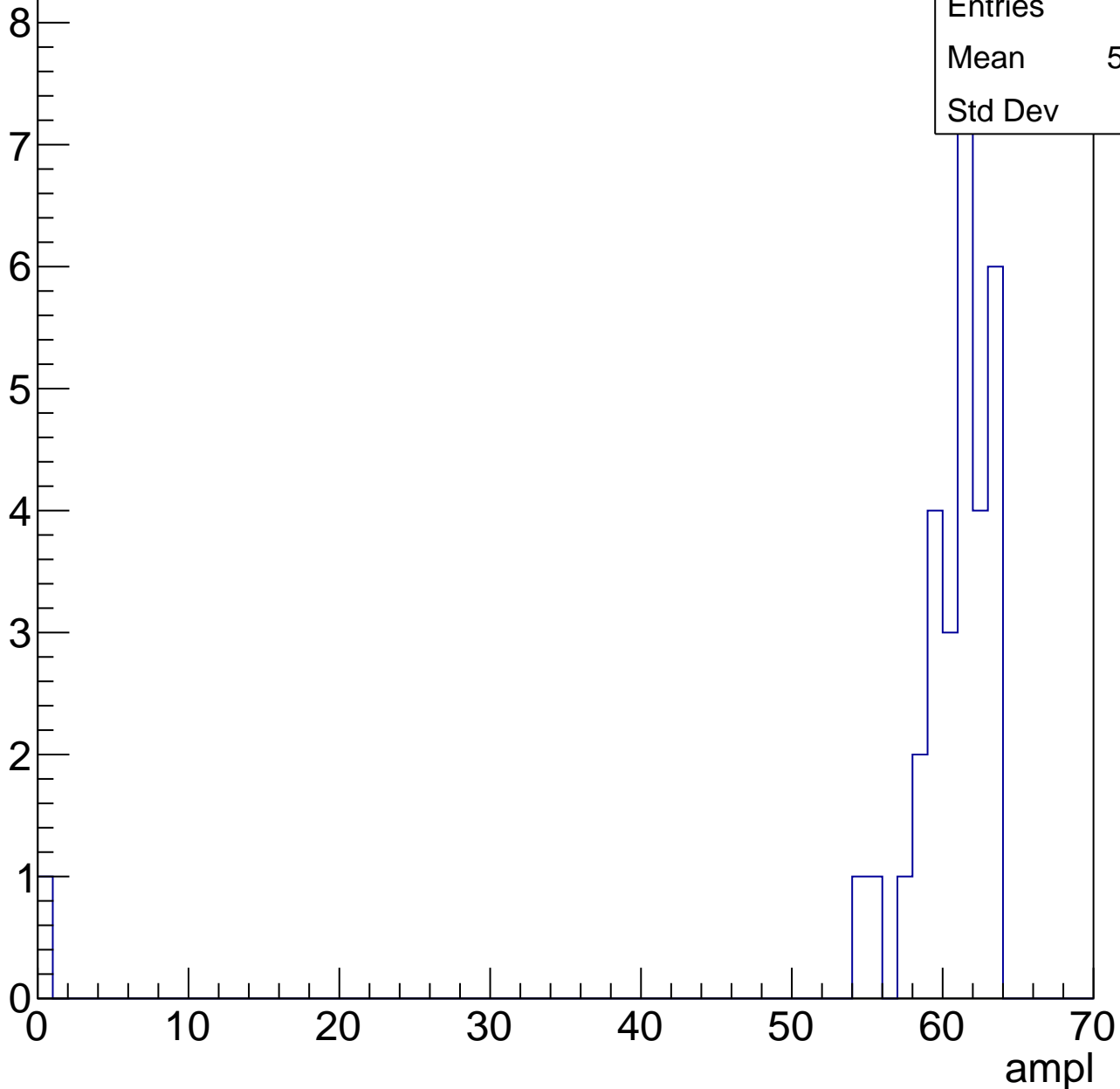


# B1L101S, U16-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

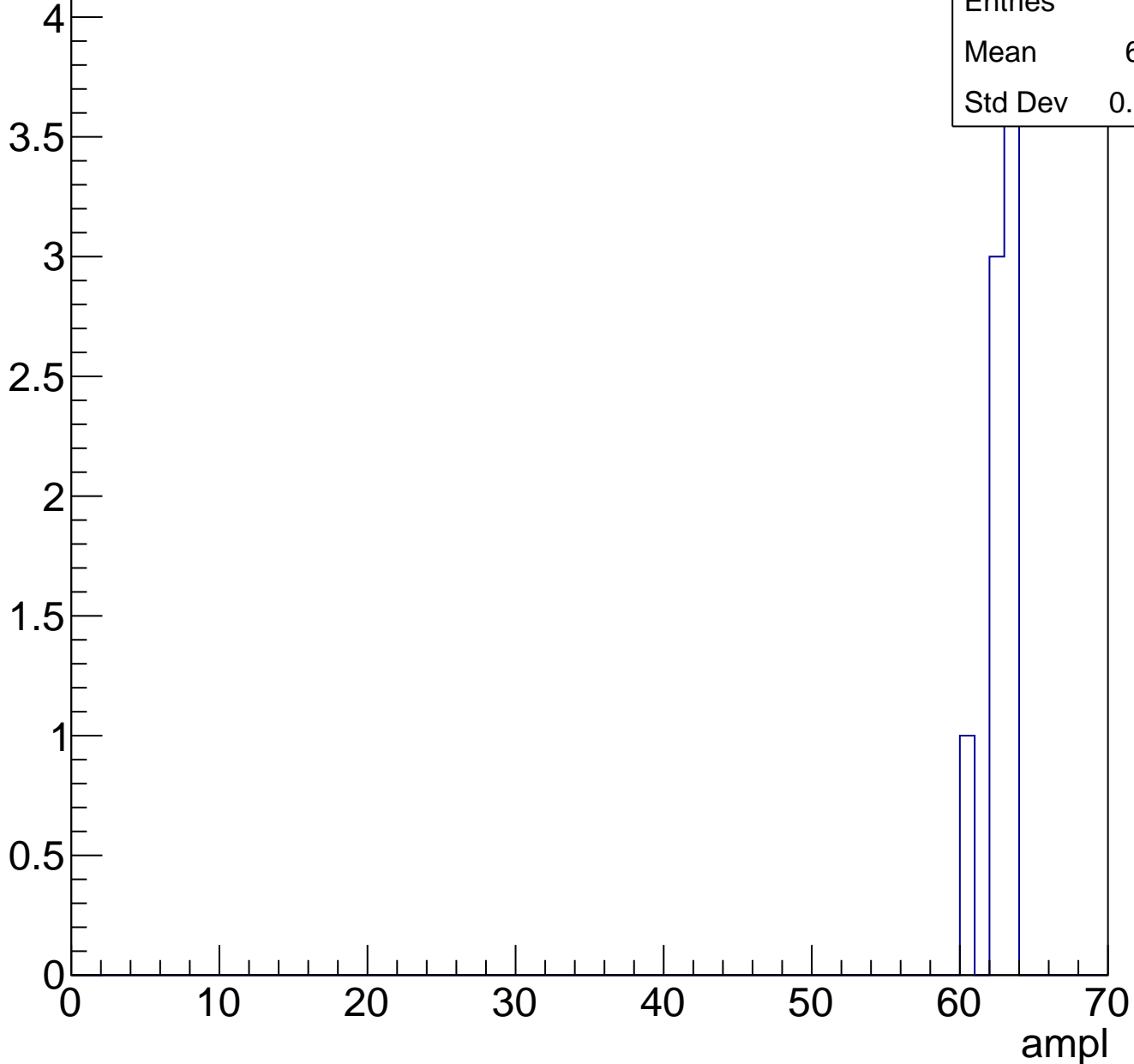
Entries	31
Mean	58.45
Std Dev	10.9



# B1L101S, U16-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U16-ch94, adc0

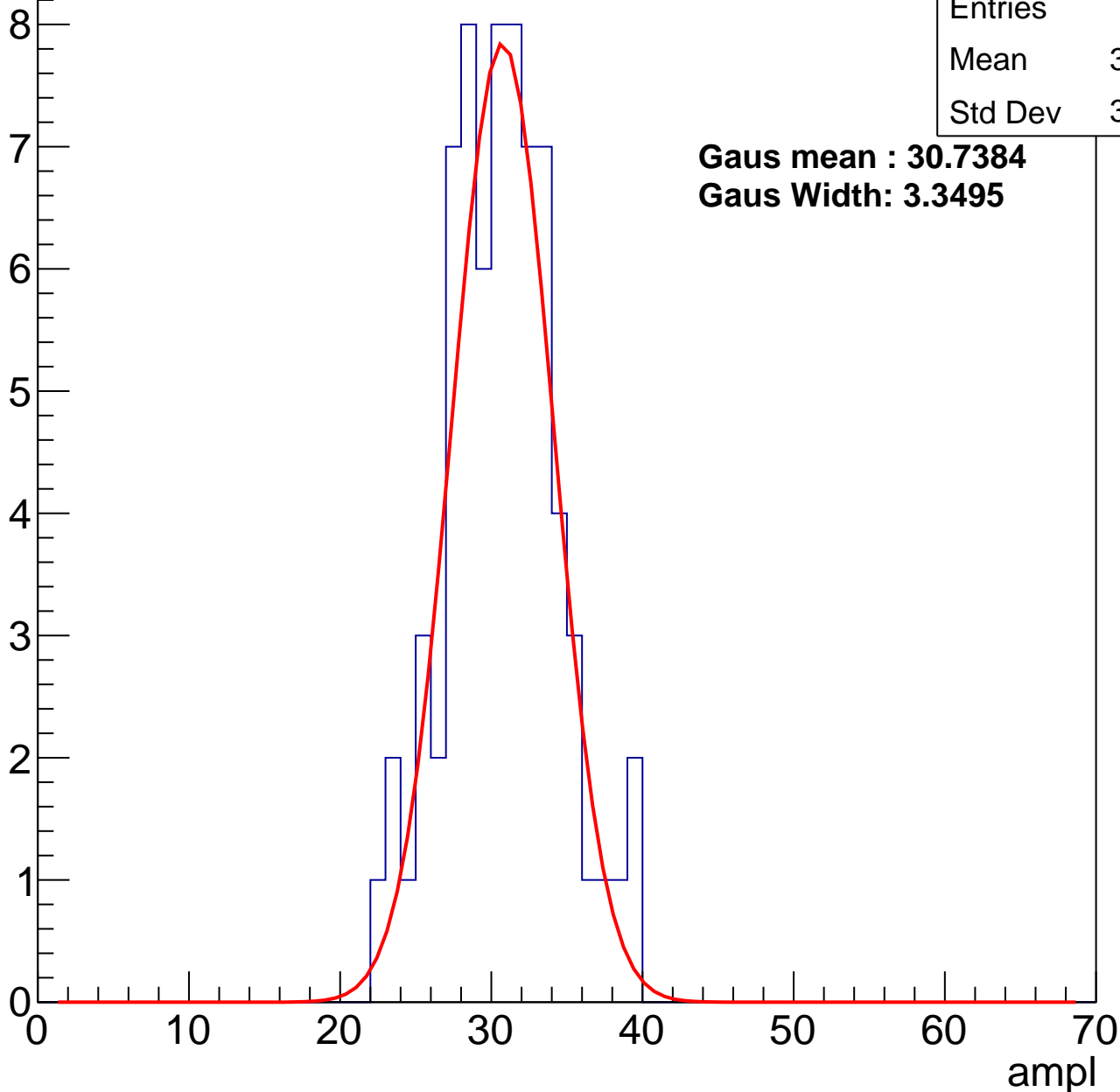
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	30.26
Std Dev	3.632

**Gaus mean : 30.7384**

**Gaus Width: 3.3495**



# B1L101S, U16-ch94, adc1

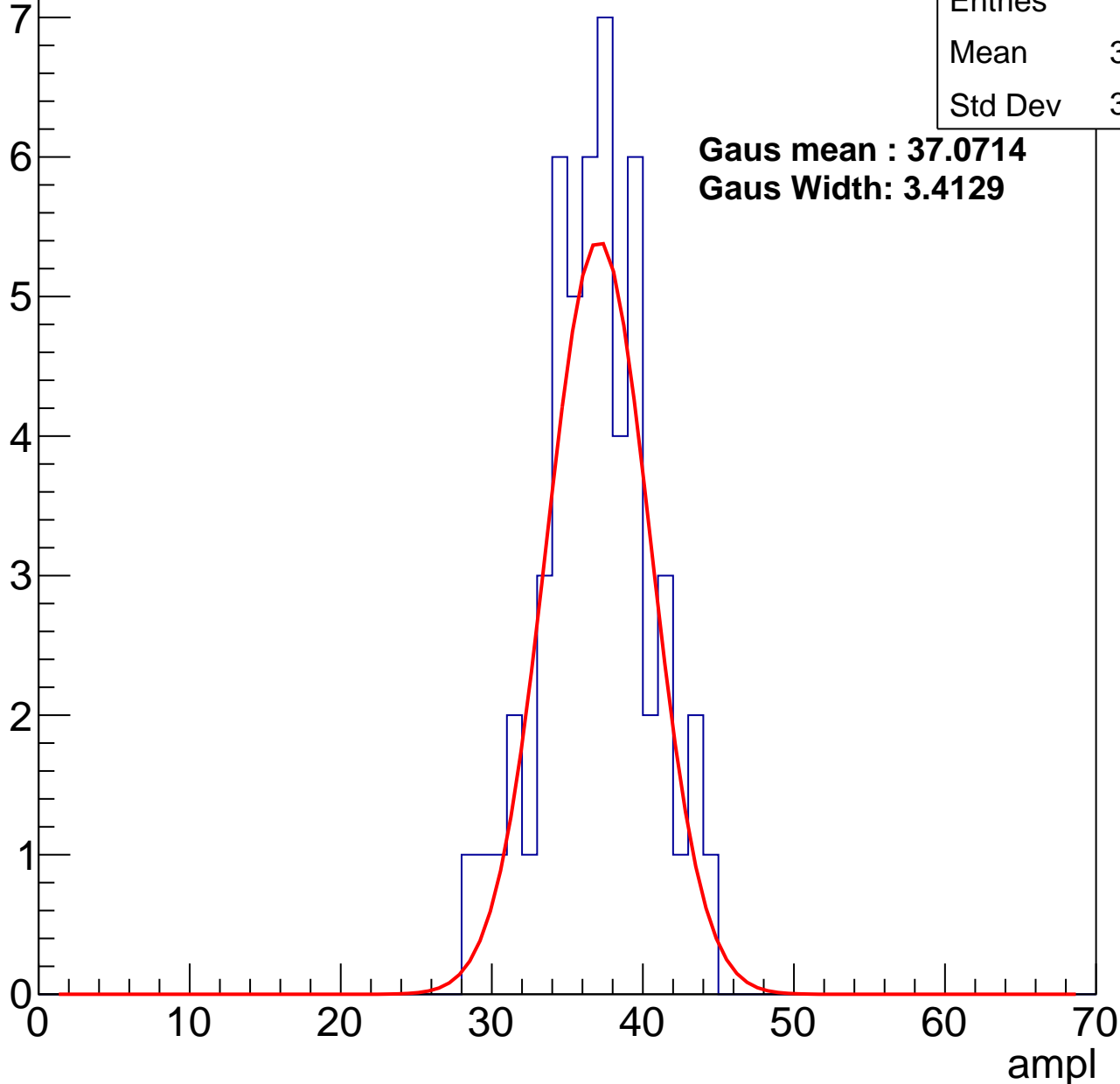
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	36.44
Std Dev	3.516

**Gaus mean : 37.0714**

**Gaus Width: 3.4129**



# B1L101S, U16-ch94, adc2

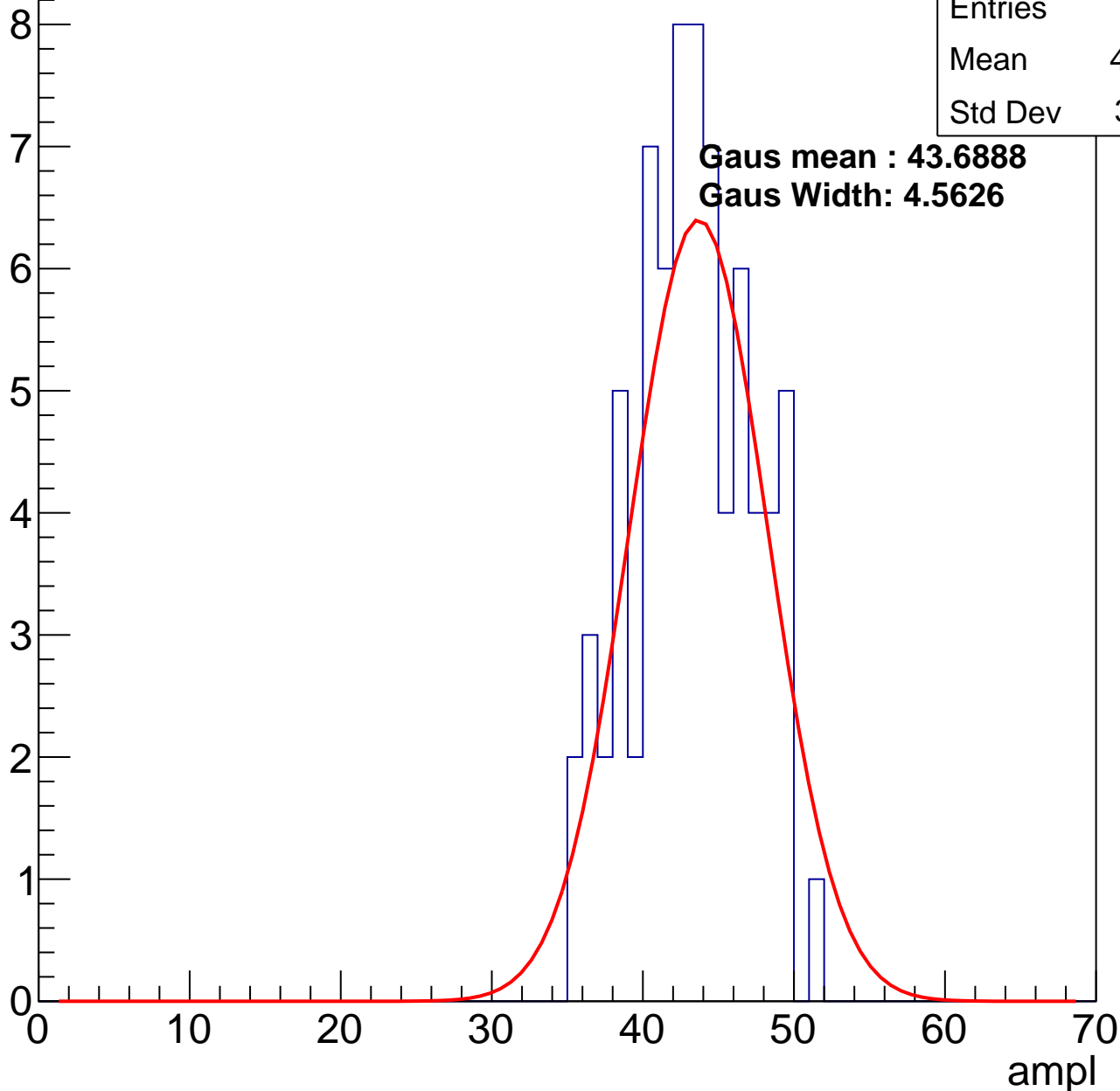
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	42.78
Std Dev	3.821

**Gaus mean : 43.6888**

**Gaus Width: 4.5626**

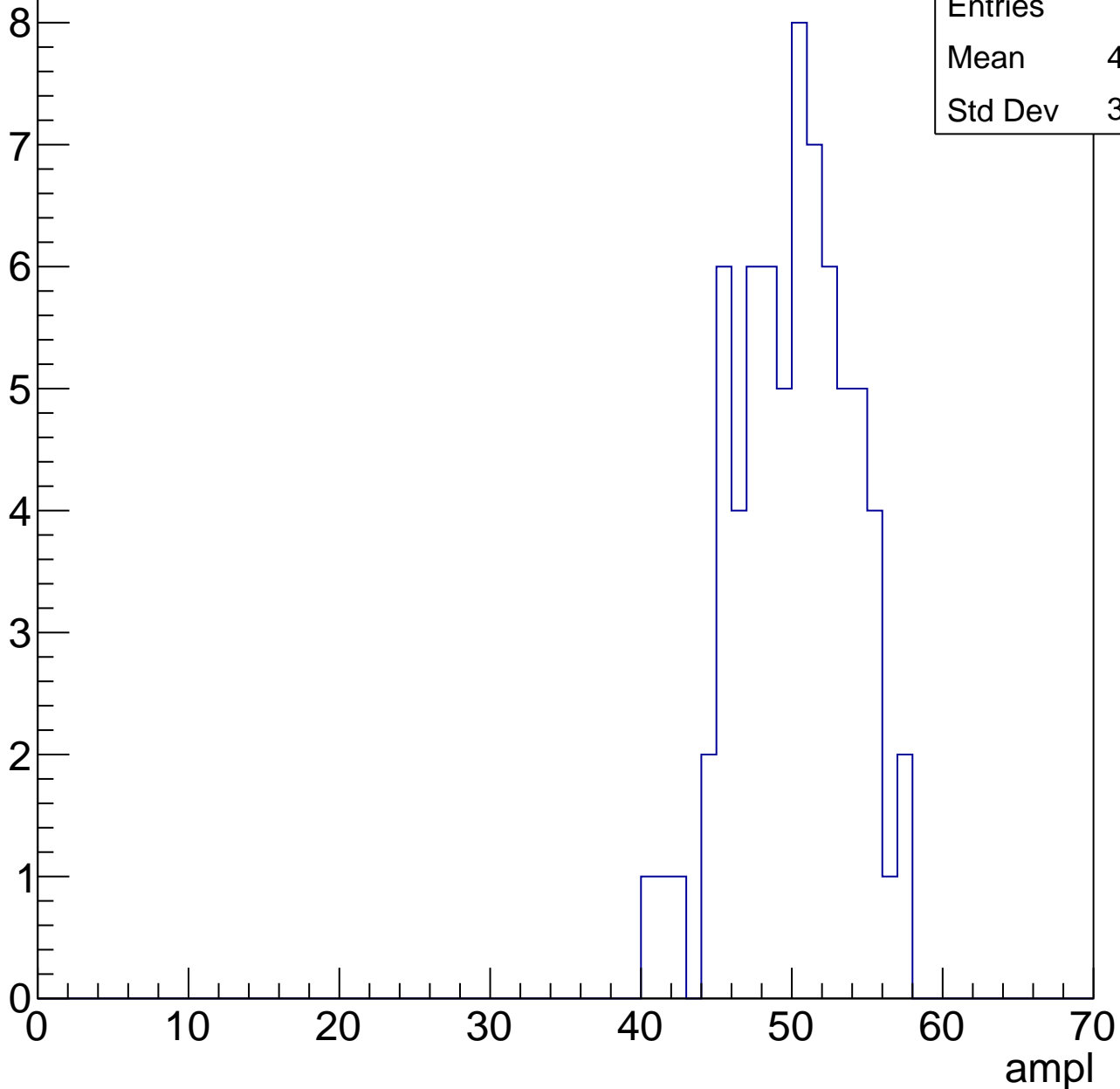


# B1L101S, U16-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

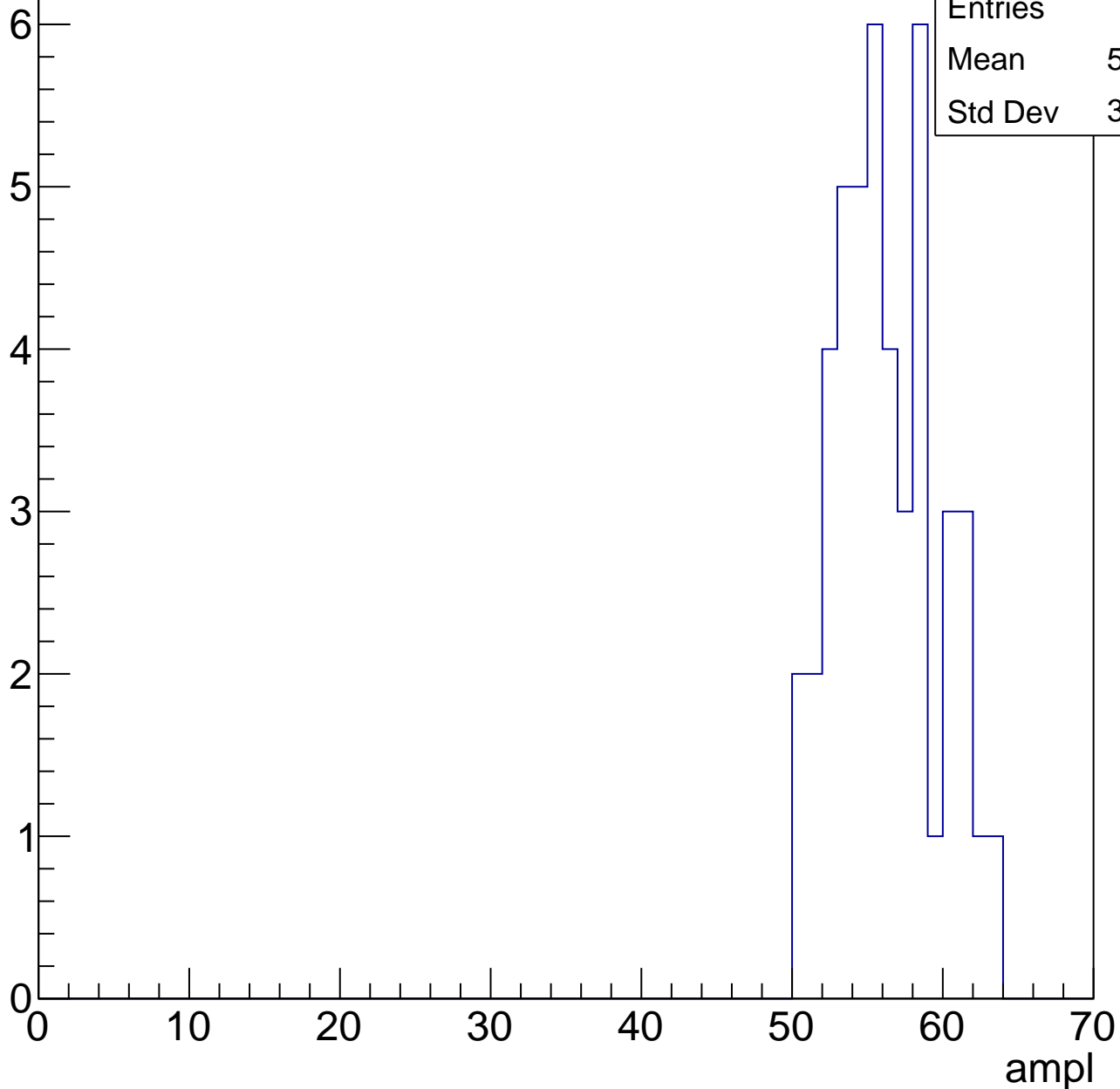
Entries	70
Mean	49.63
Std Dev	3.769



# B1L101S, U16-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

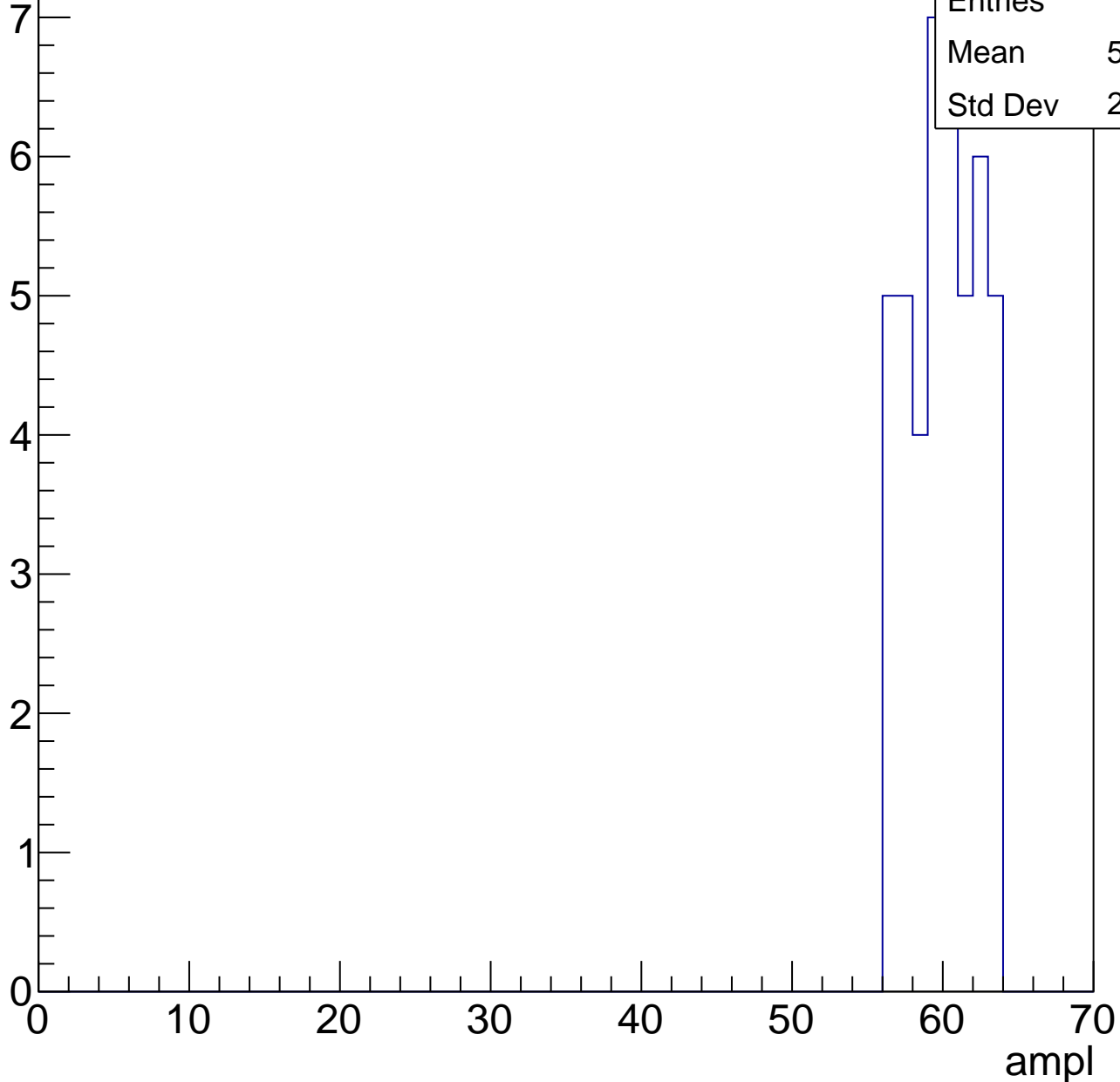


Entries	46
Mean	55.76
Std Dev	3.292

# B1L101S, U16-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

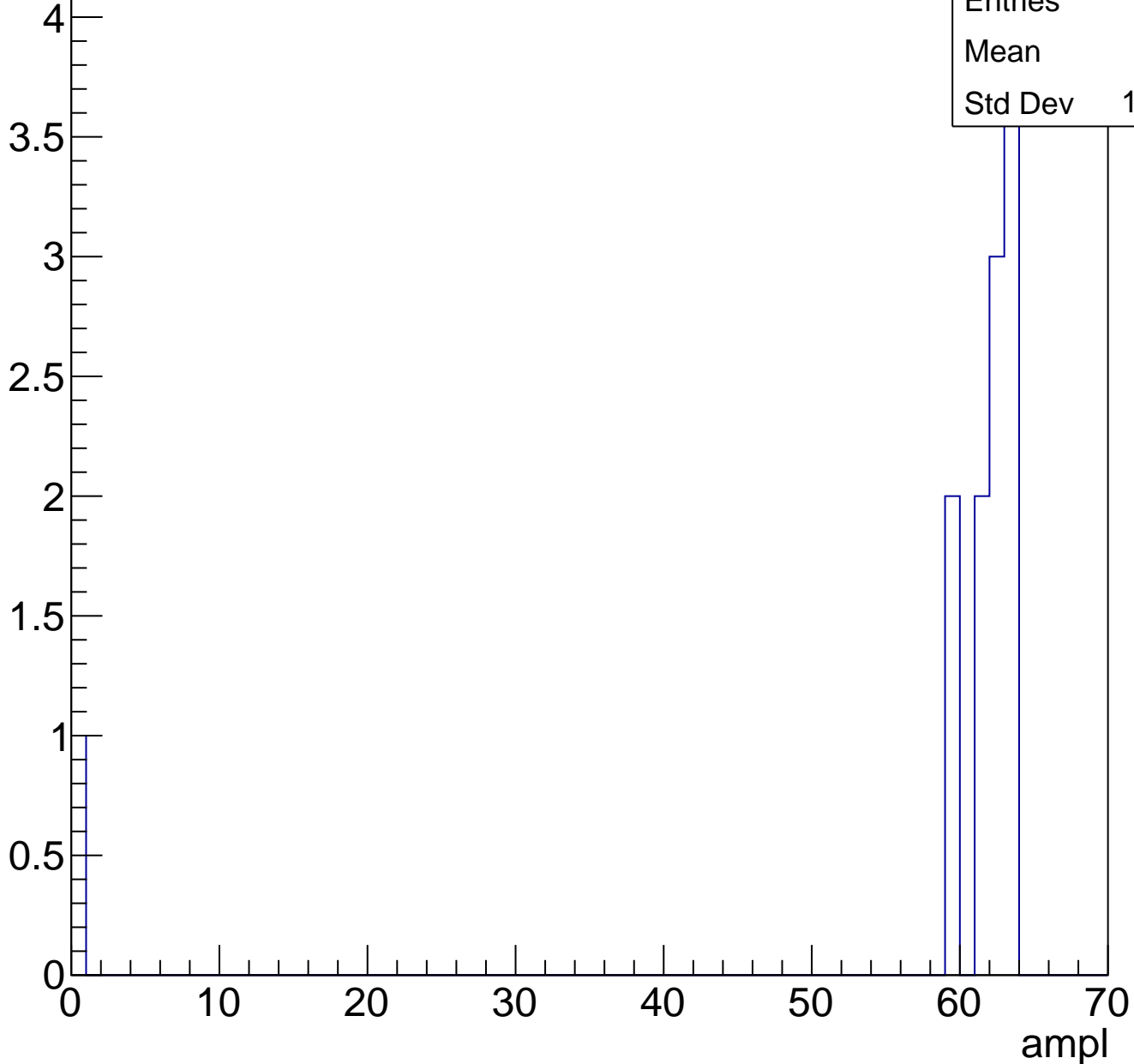
Entry



# B1L101S, U16-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch95, adc0

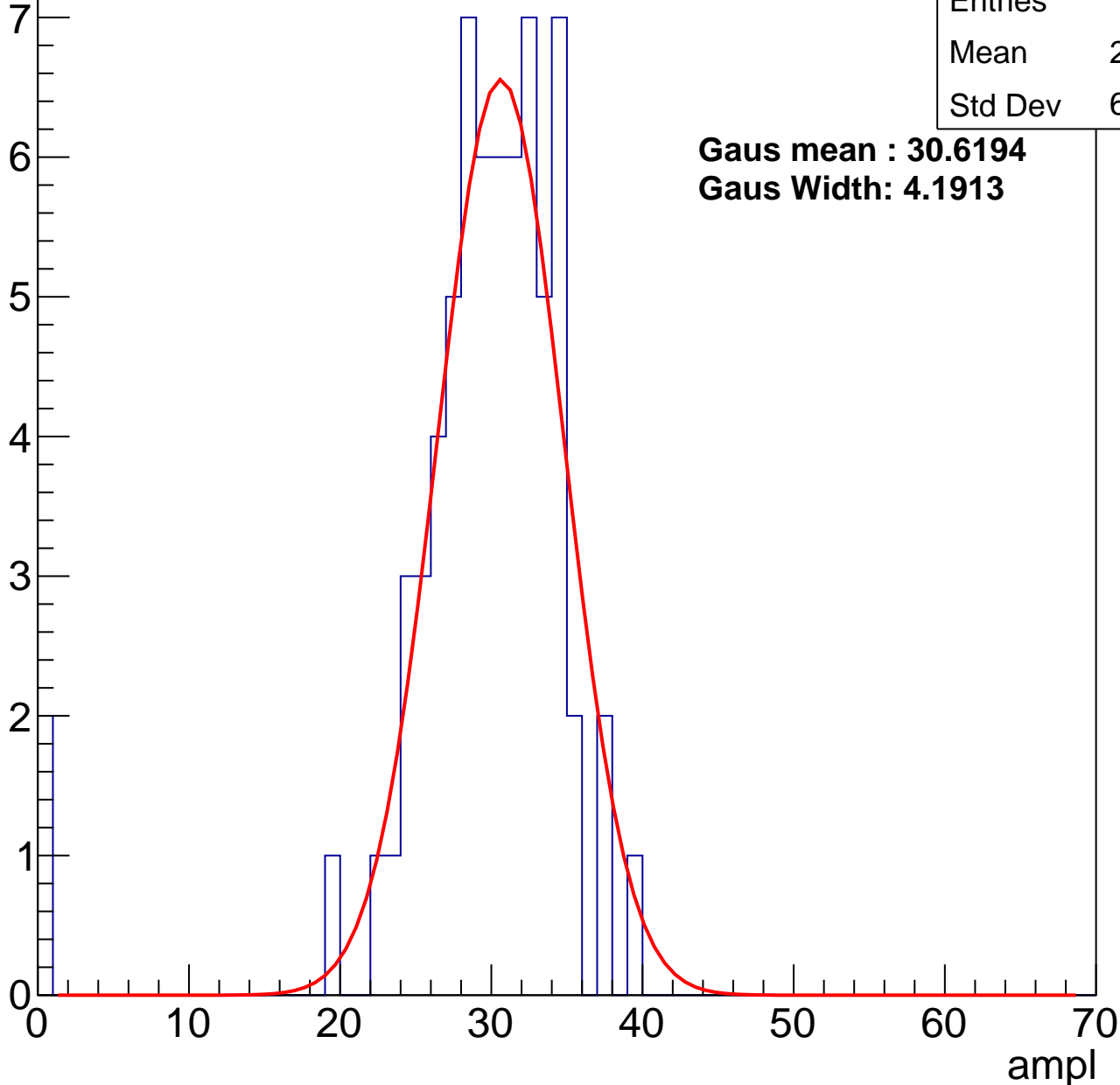
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	28.93
Std Dev	6.256

**Gaus mean : 30.6194**

**Gaus Width: 4.1913**



# B1L101S, U16-ch95, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	75
Mean	36.48
Std Dev	4.237

**Gaus mean : 37.4167**

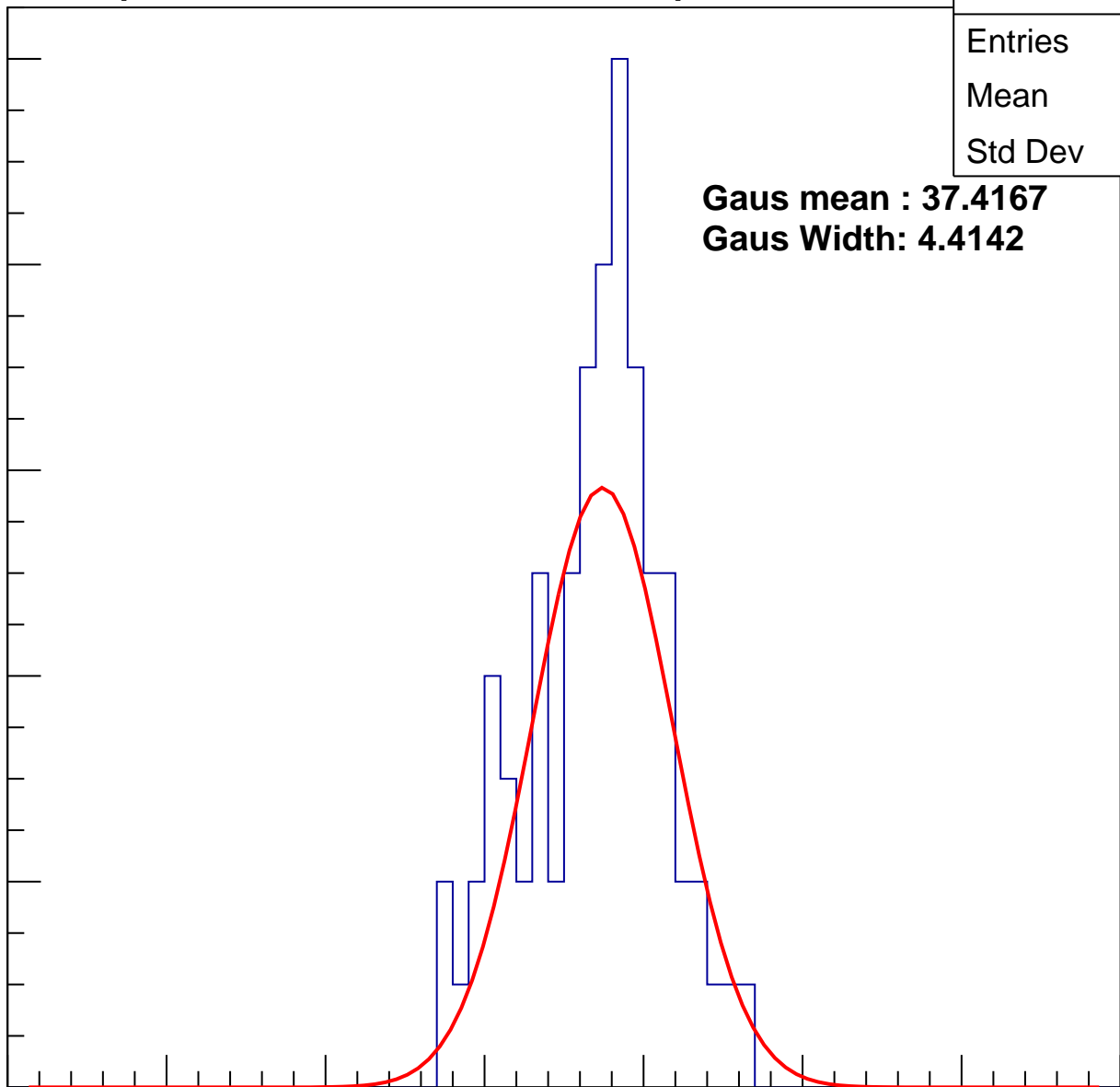
**Gaus Width: 4.4142**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch95, adc2

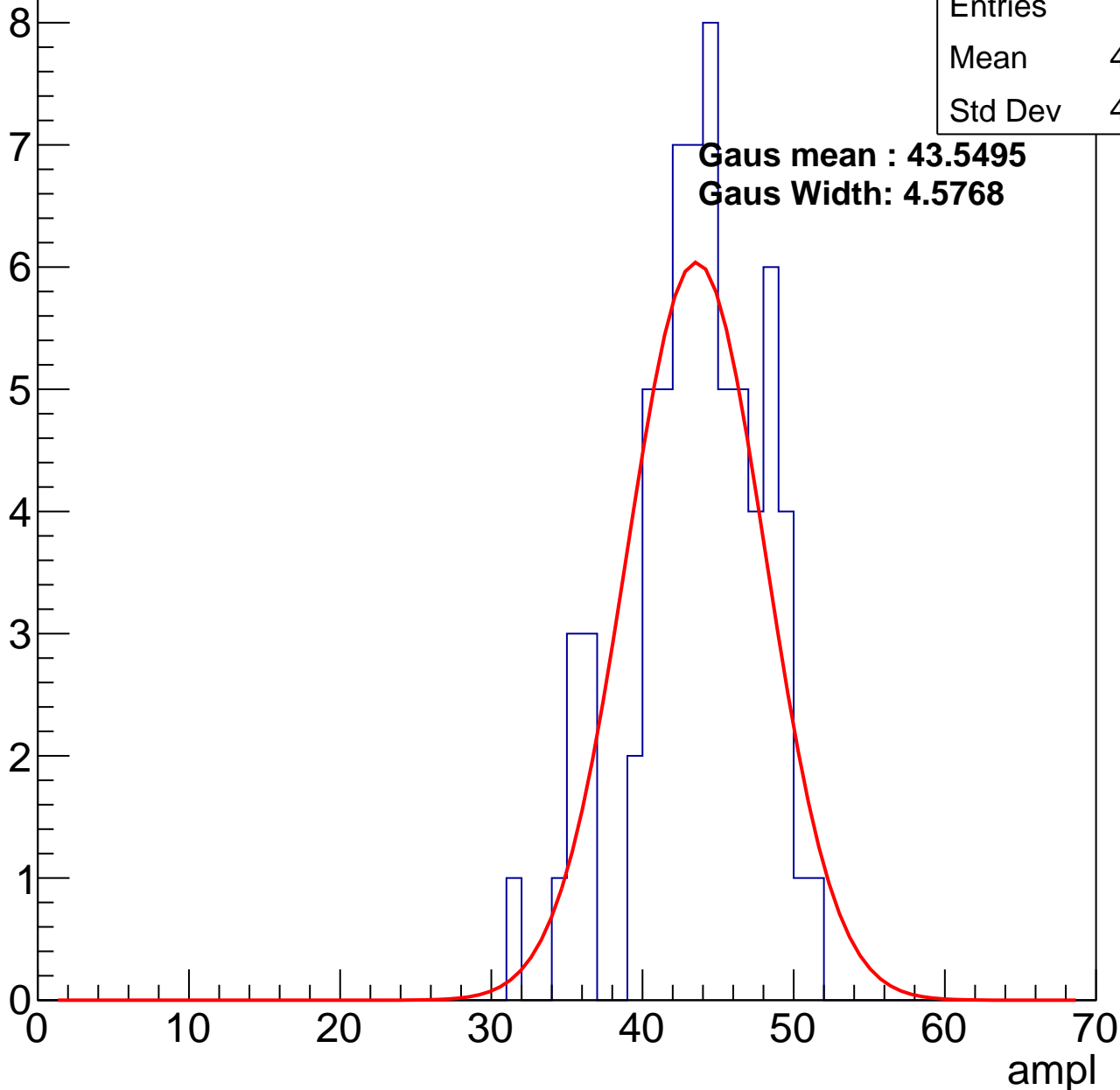
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	43.18
Std Dev	4.218

**Gaus mean : 43.5495**

**Gaus Width: 4.5768**

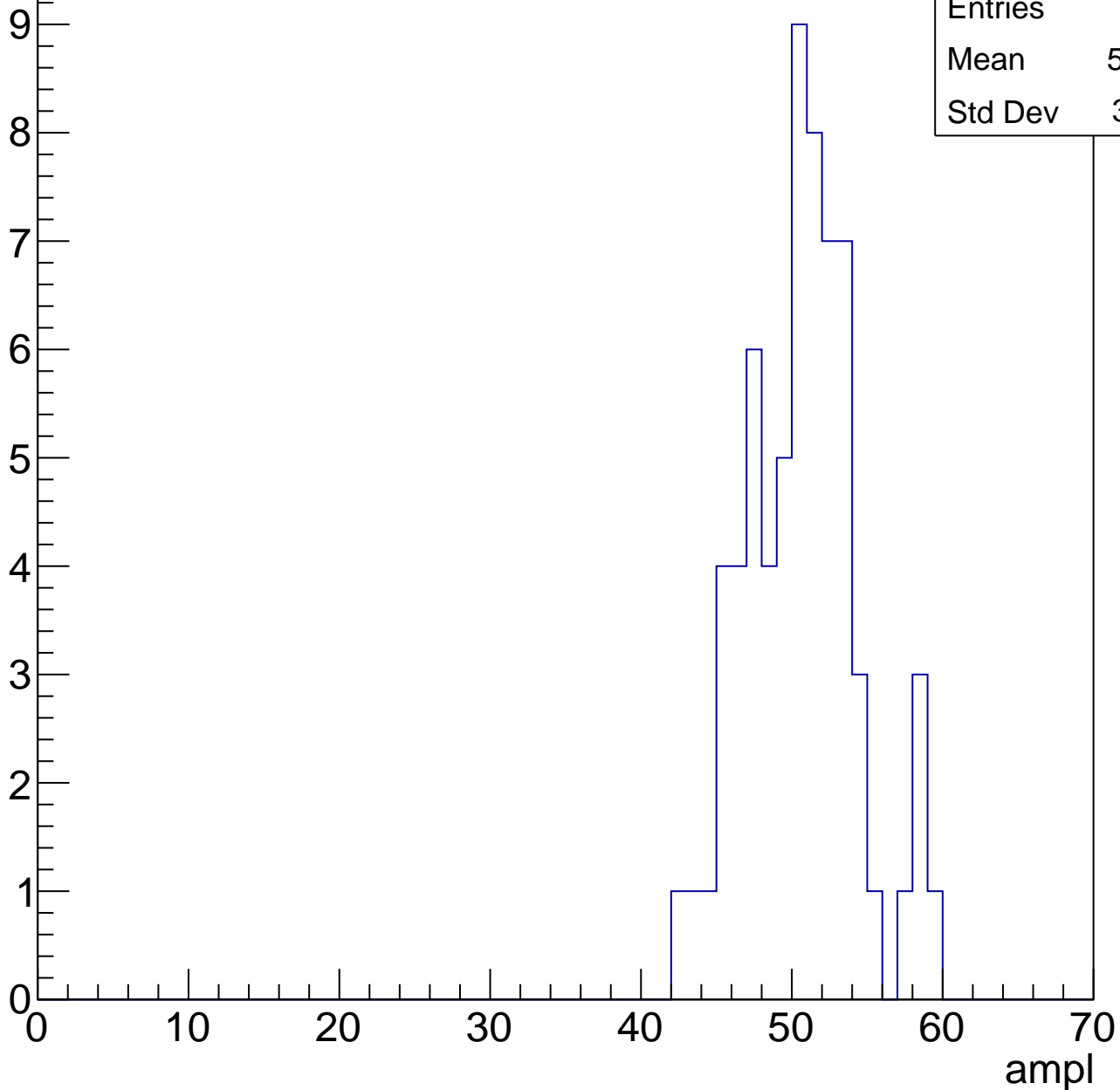


# B1L101S, U16-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	50.18
Std Dev	3.651

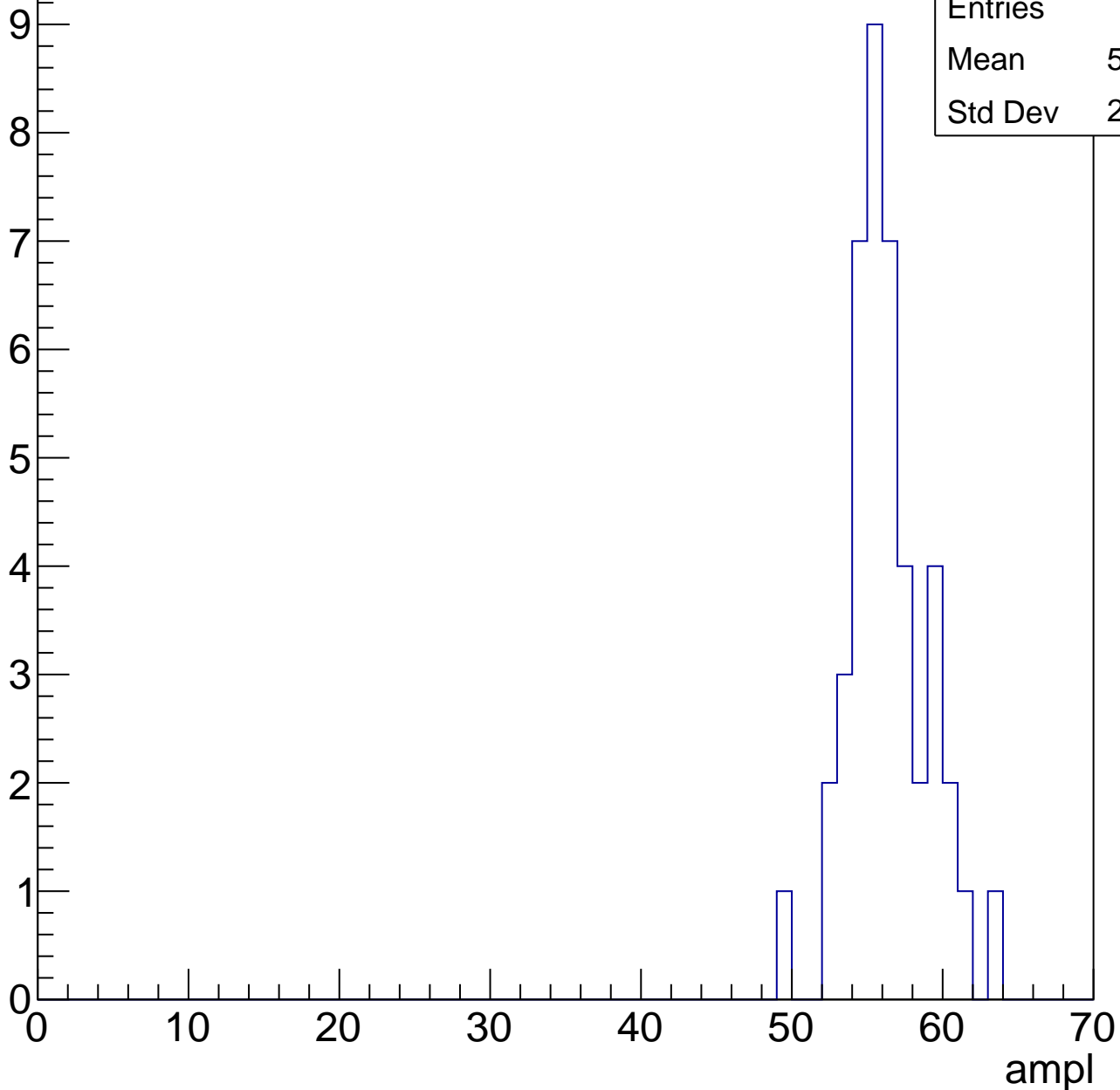


# B1L101S, U16-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	55.84
Std Dev	2.632



# B1L101S, U16-ch95, adc5

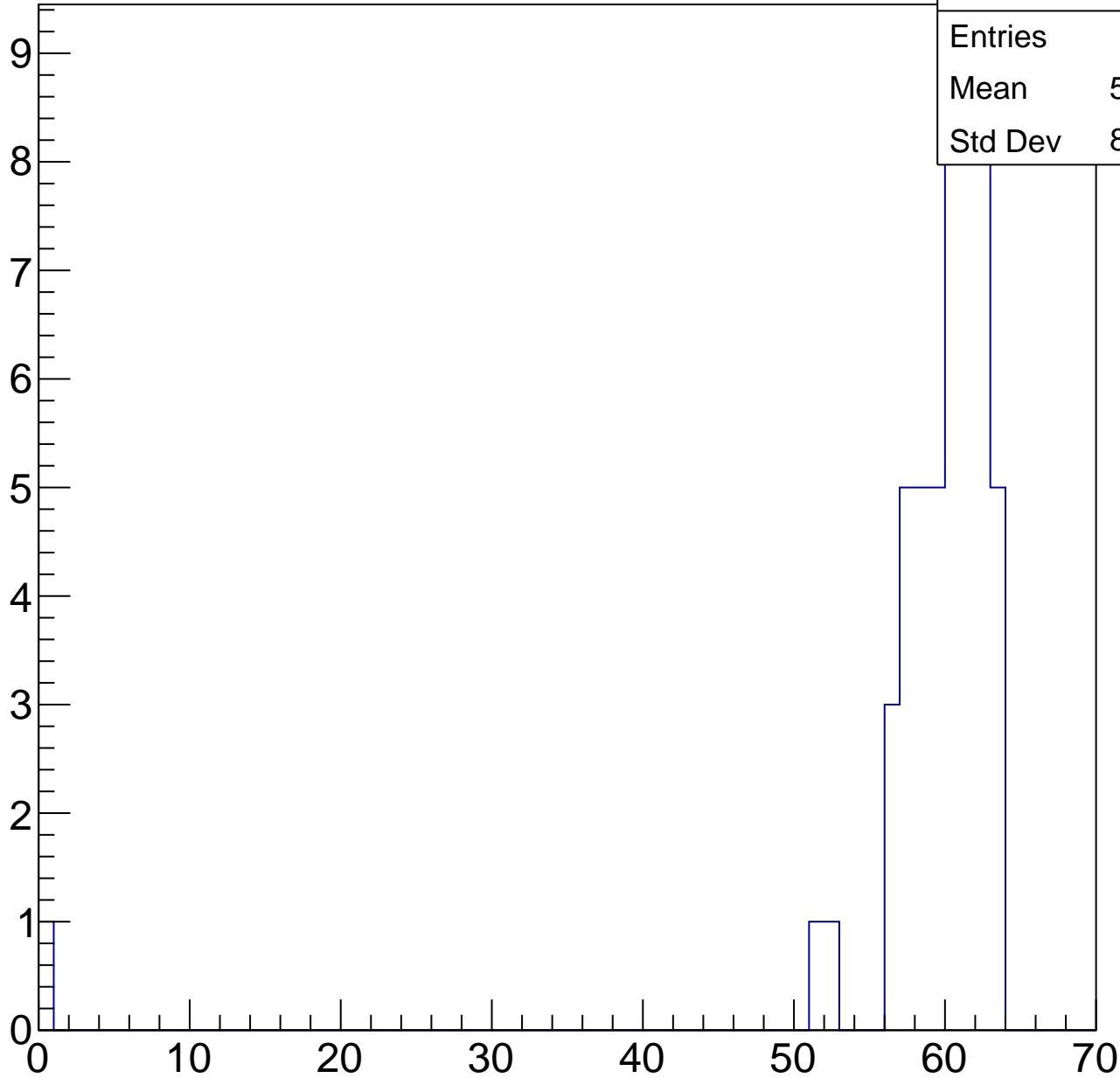
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	58.47
Std Dev	8.669

ampl



# B1L101S, U16-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch96, adc0

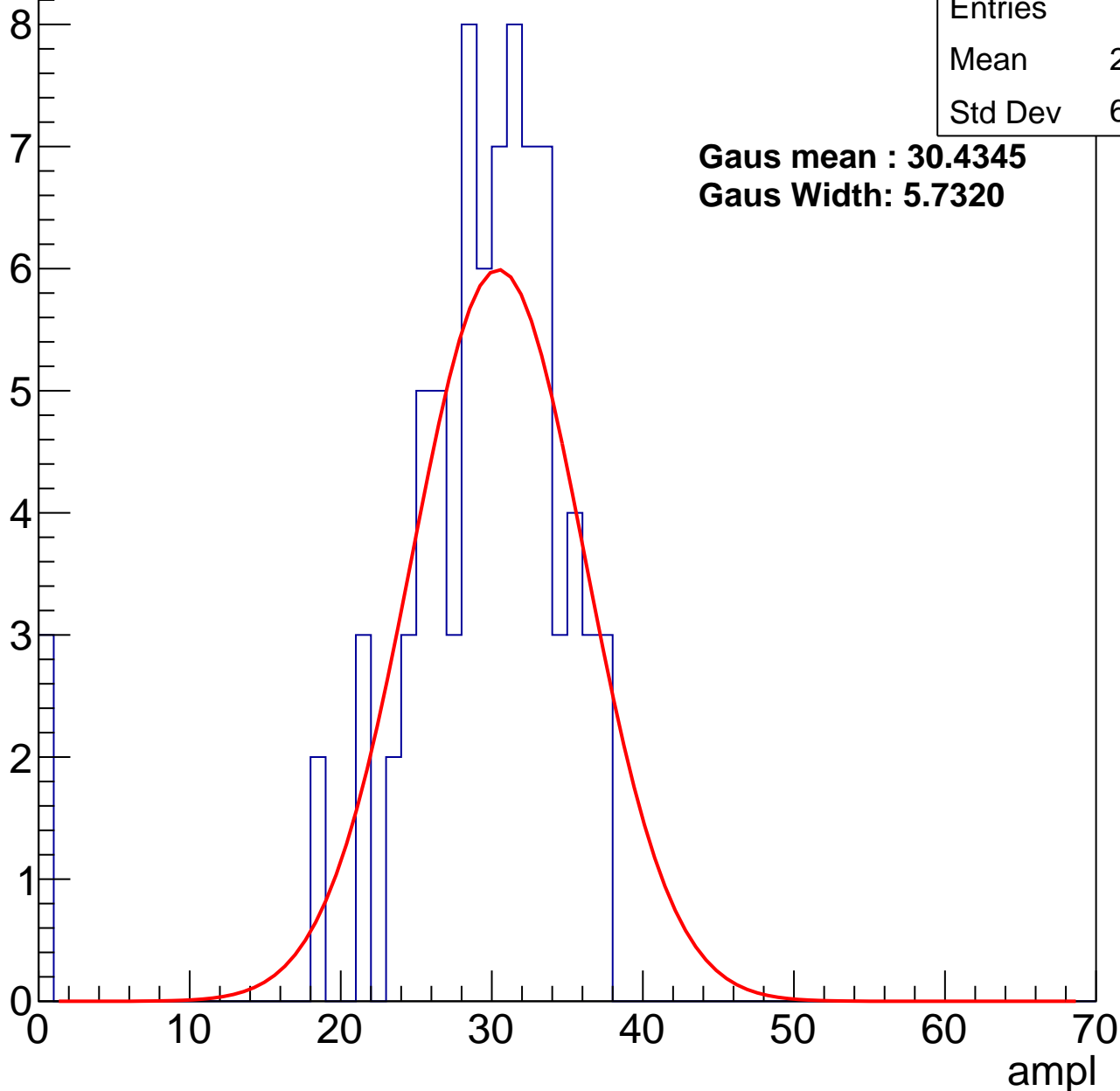
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	28.35
Std Dev	6.973

**Gaus mean : 30.4345**

**Gaus Width: 5.7320**



# B1L101S, U16-ch96, adc1

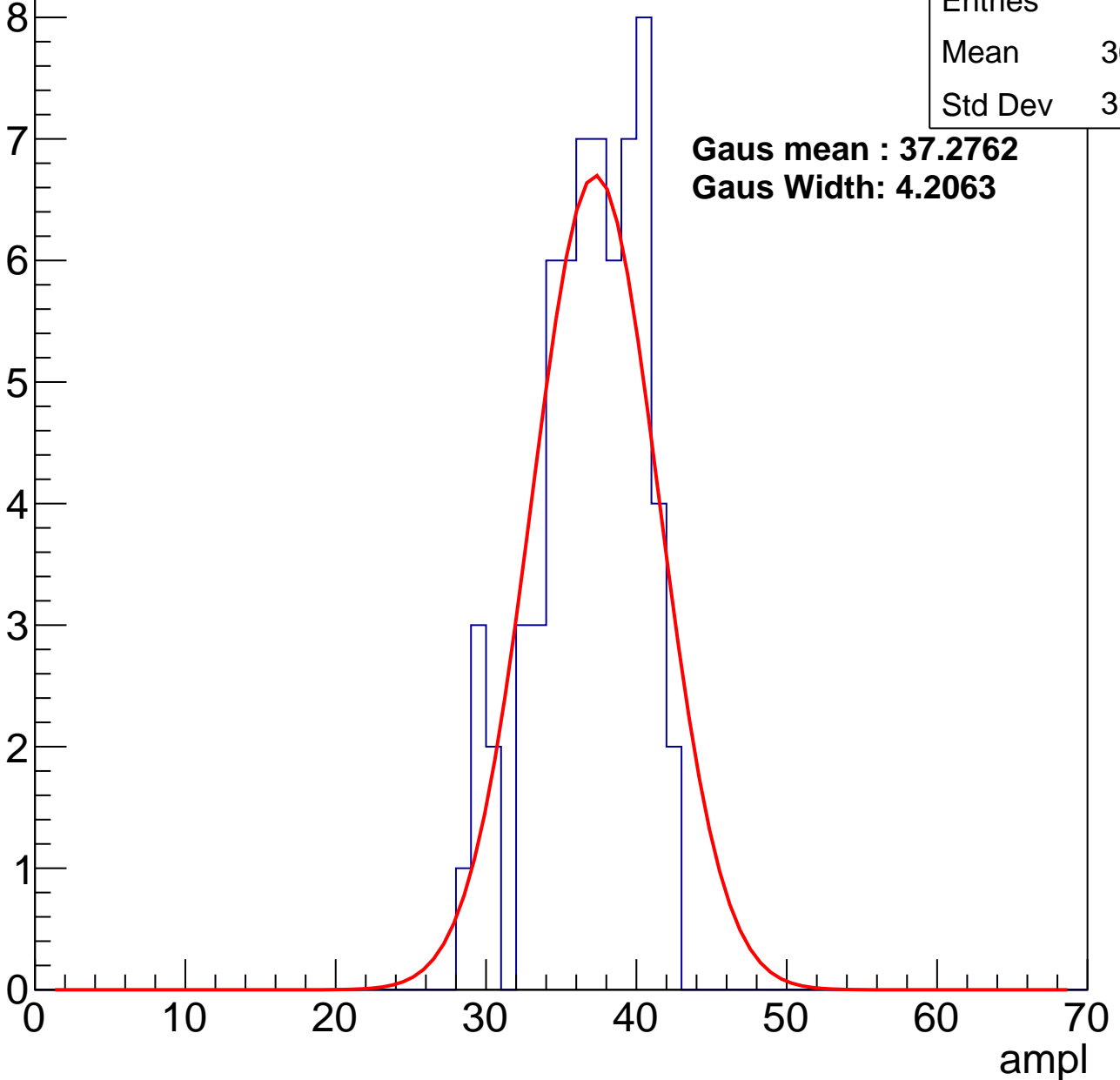
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	36.37
Std Dev	3.449

**Gaus mean : 37.2762**

**Gaus Width: 4.2063**



# B1L101S, U16-ch96, adc2

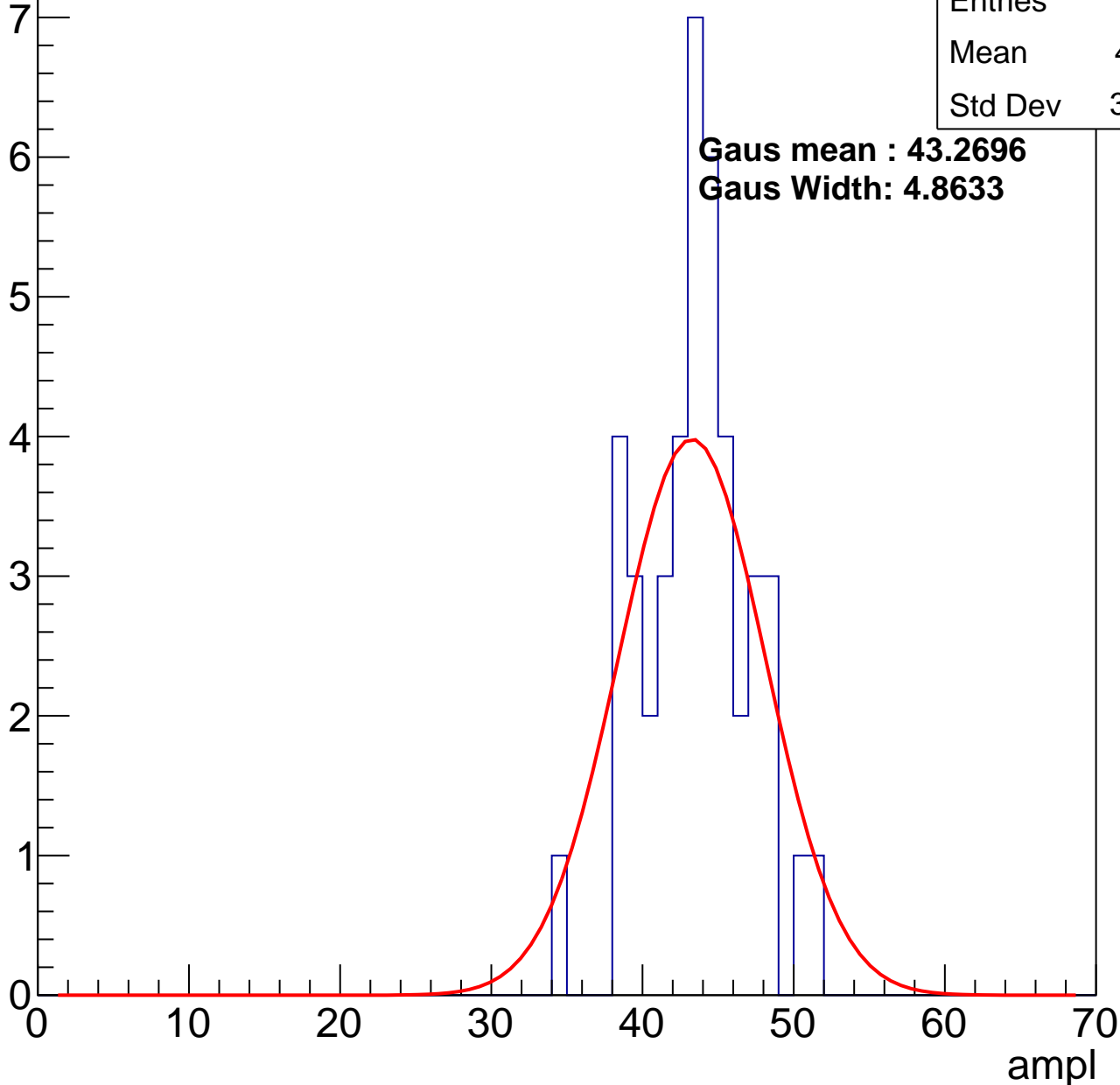
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	44
Mean	43.11
Std Dev	3.498

**Gaus mean : 43.2696**

**Gaus Width: 4.8633**

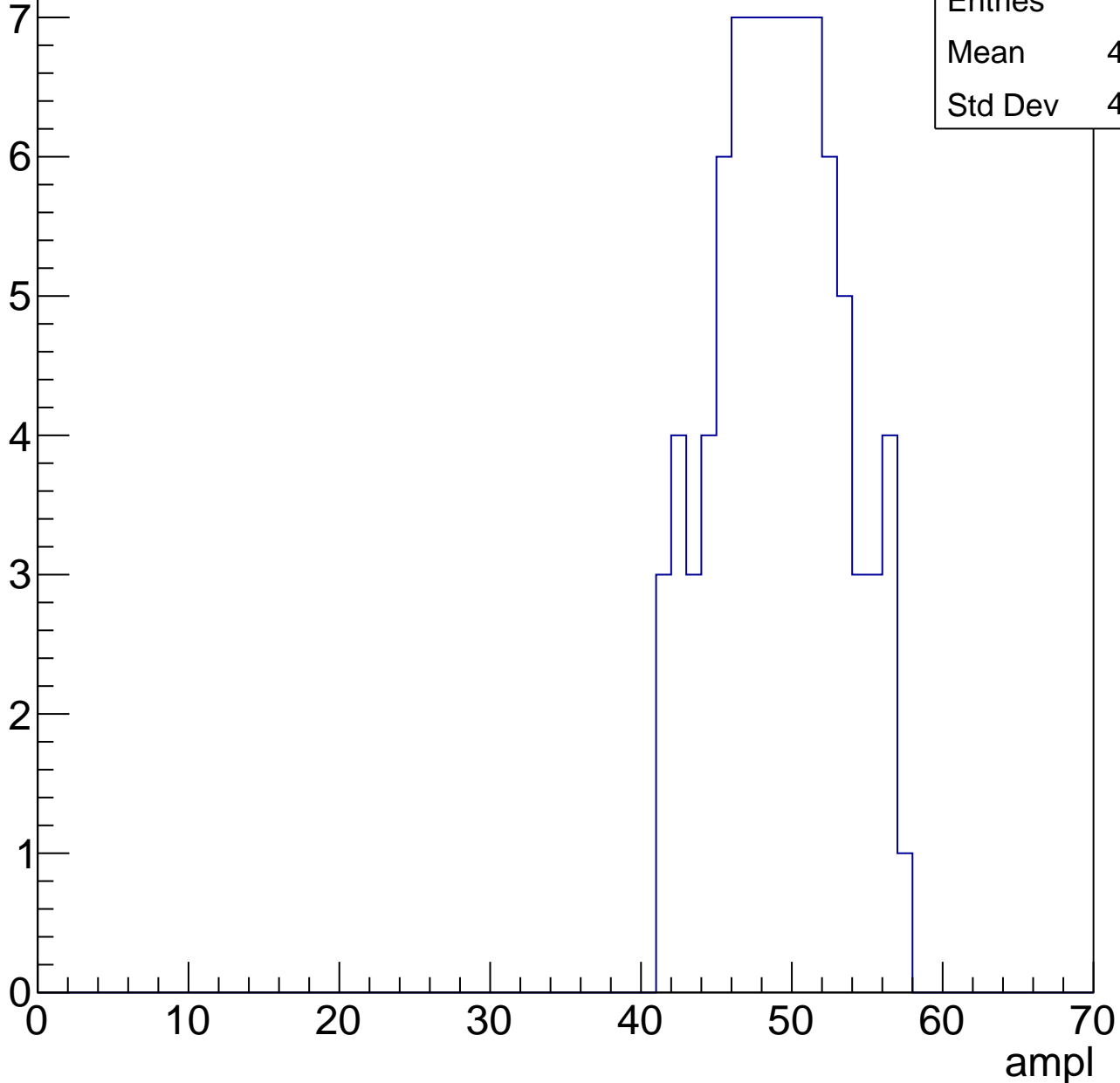


# B1L101S, U16-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	84
Mean	48.67
Std Dev	4.072

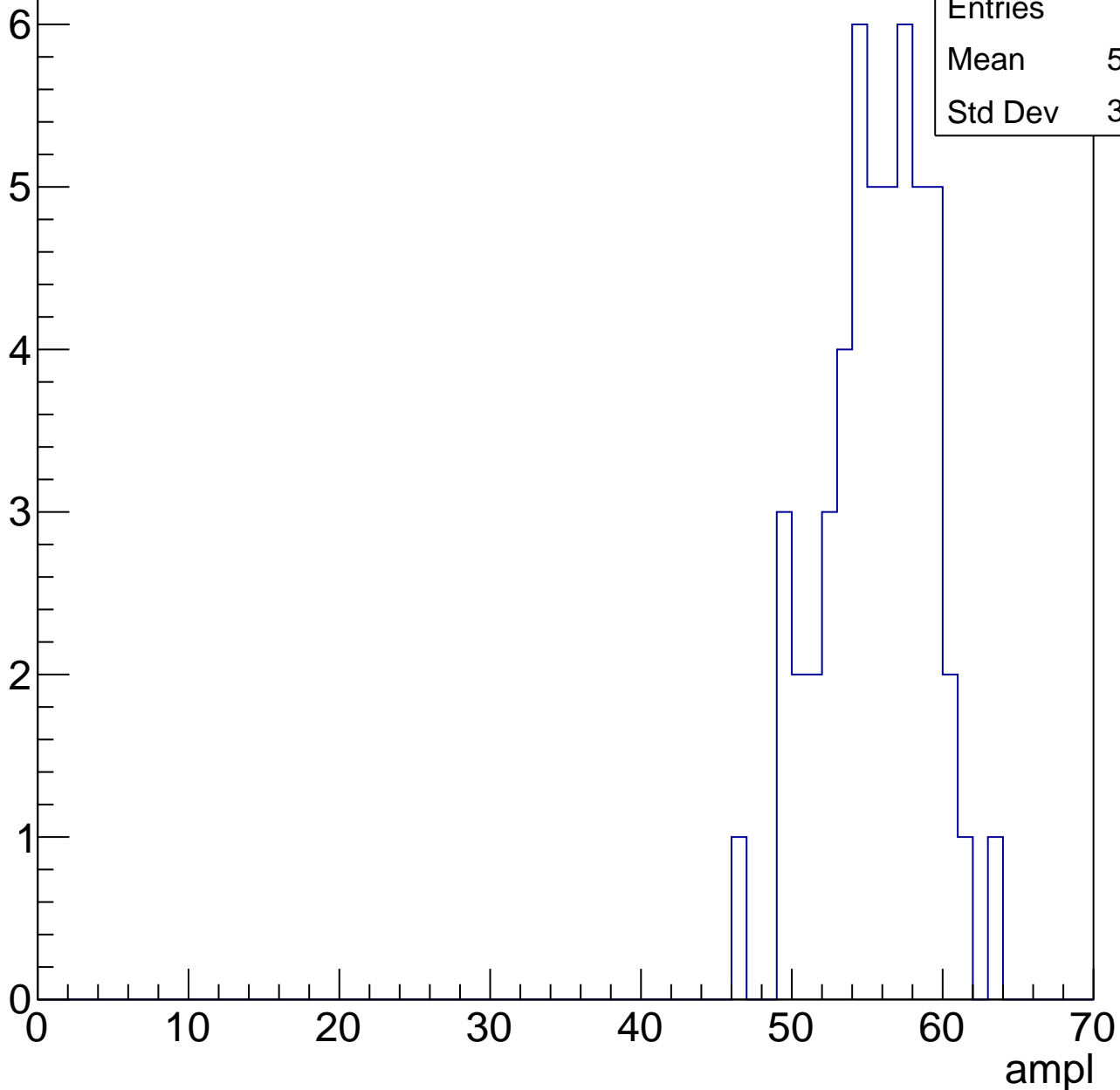


# B1L101S, U16-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	55.16
Std Dev	3.494

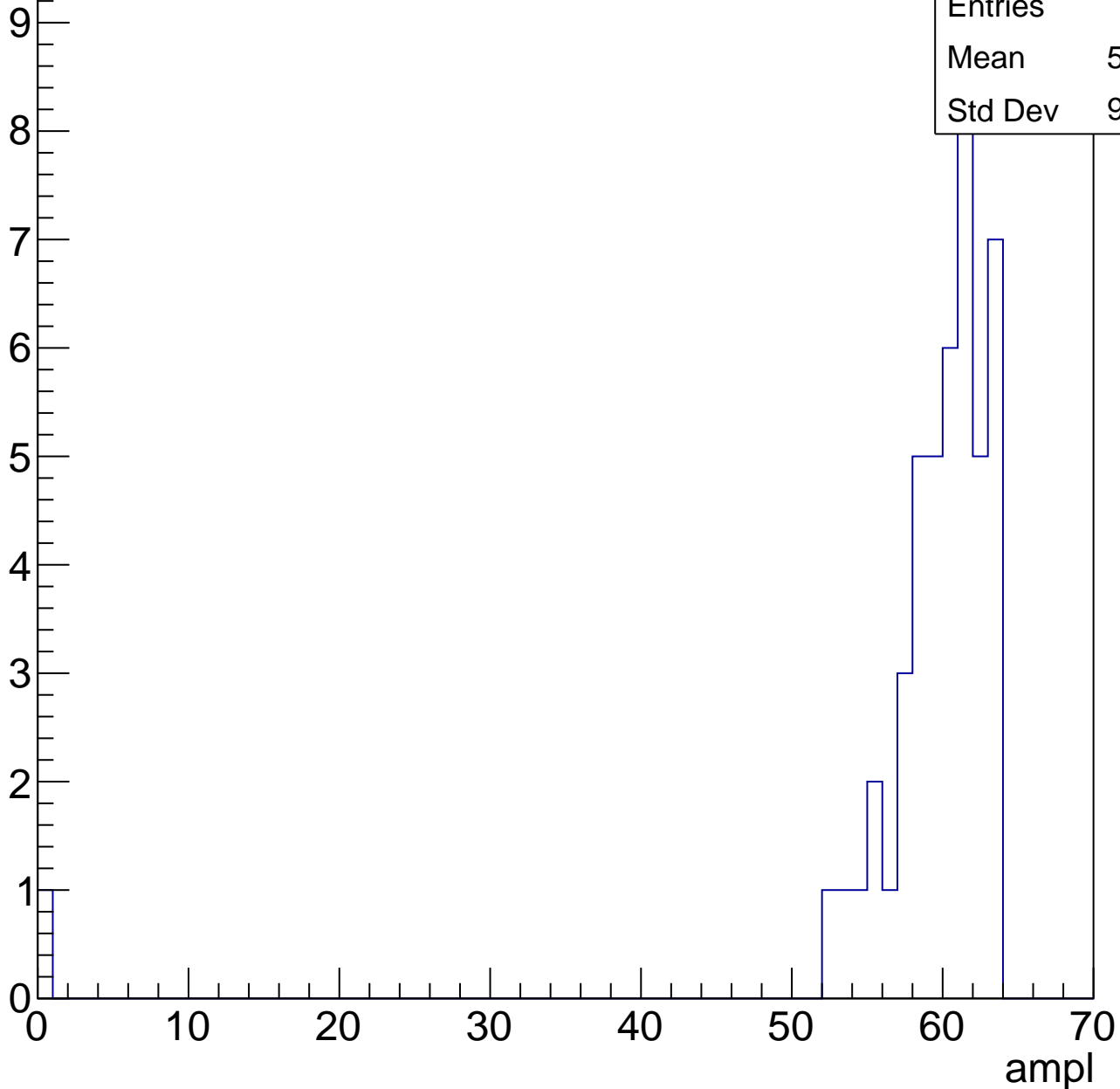


# B1L101S, U16-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	58.32
Std Dev	9.023

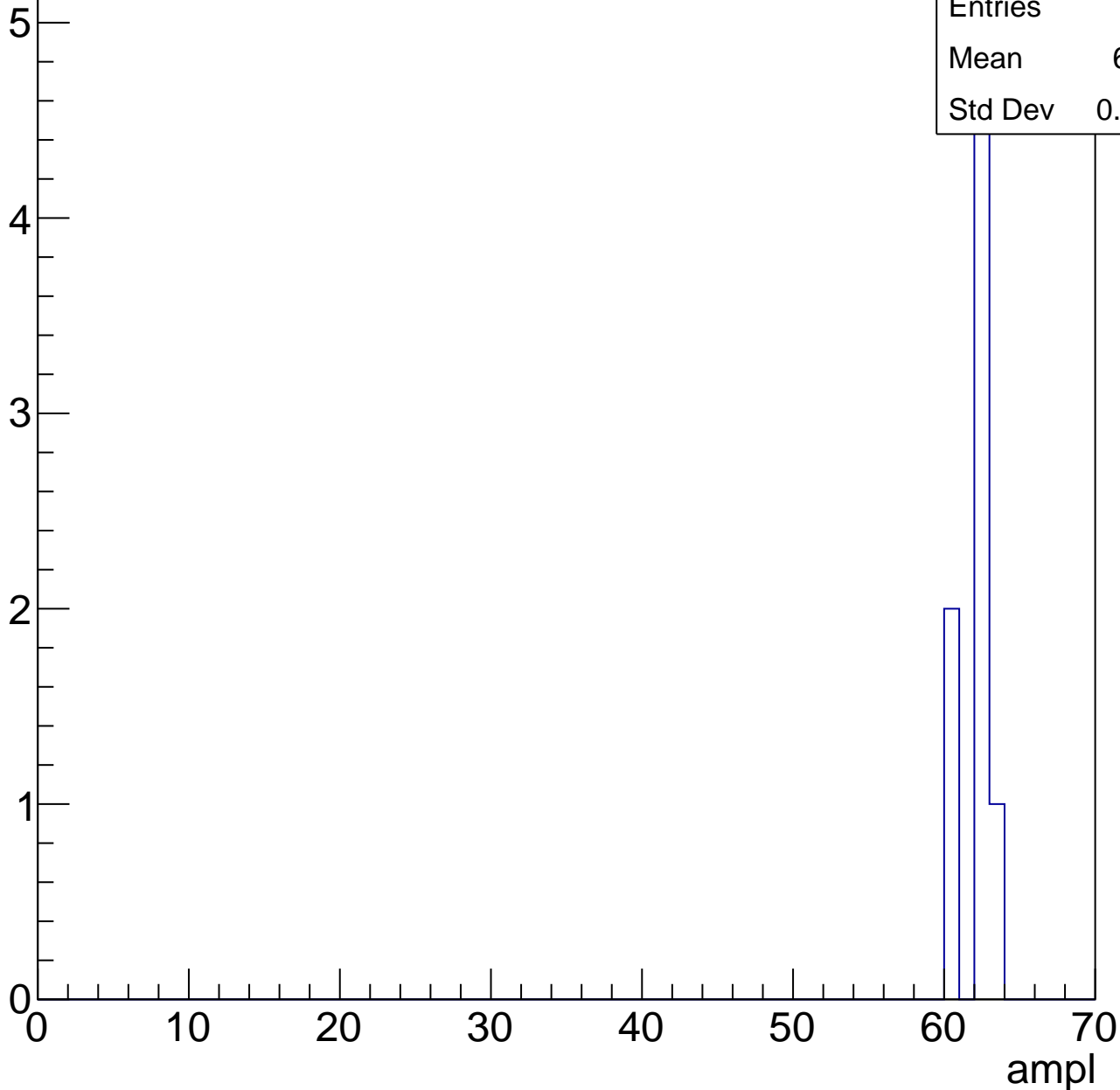


# B1L101S, U16-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	8
Mean	61.62
Std Dev	0.9922





# B1L101S, U16-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

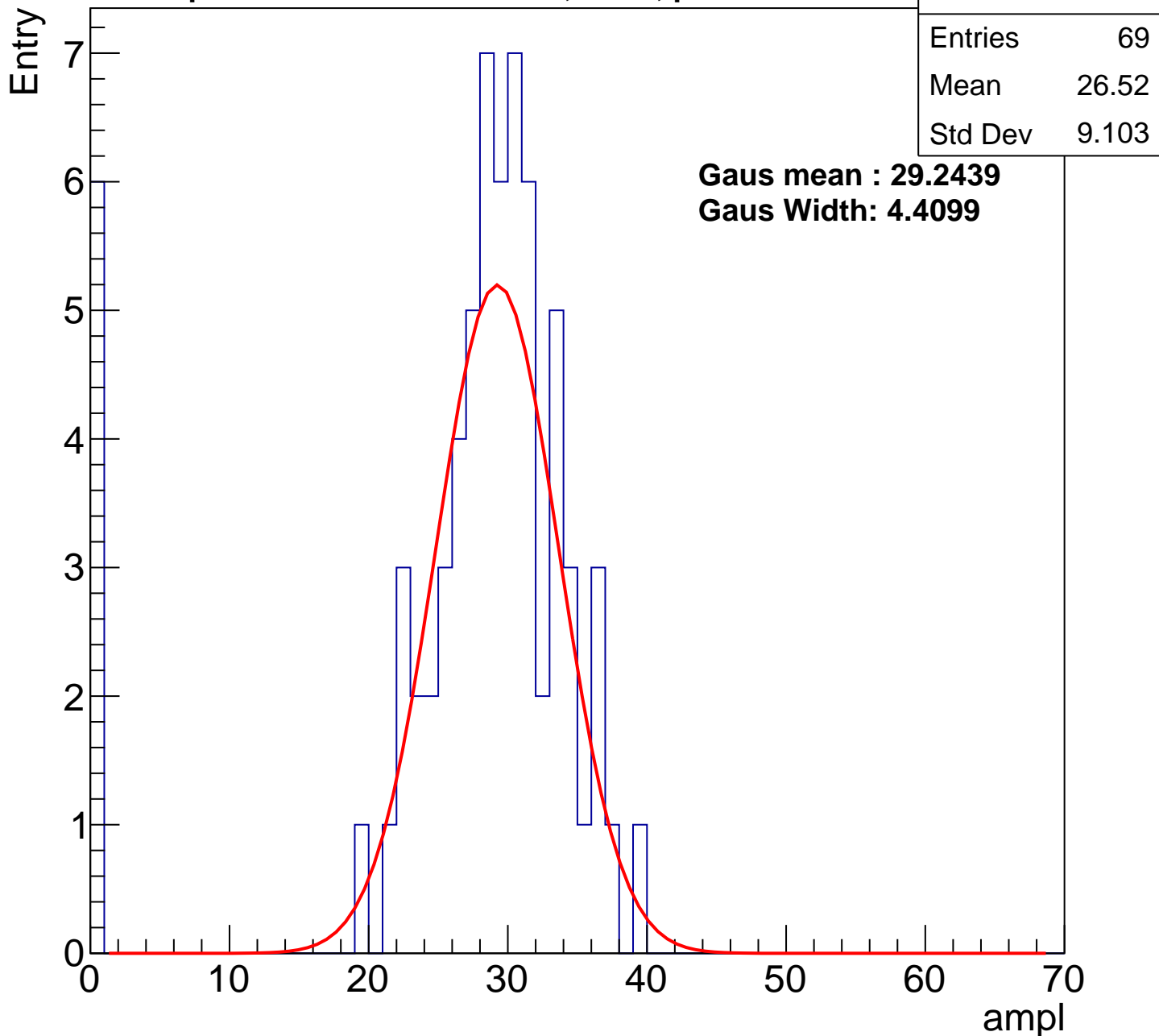
Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L101S, U16-ch97, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U16-ch97, adc1

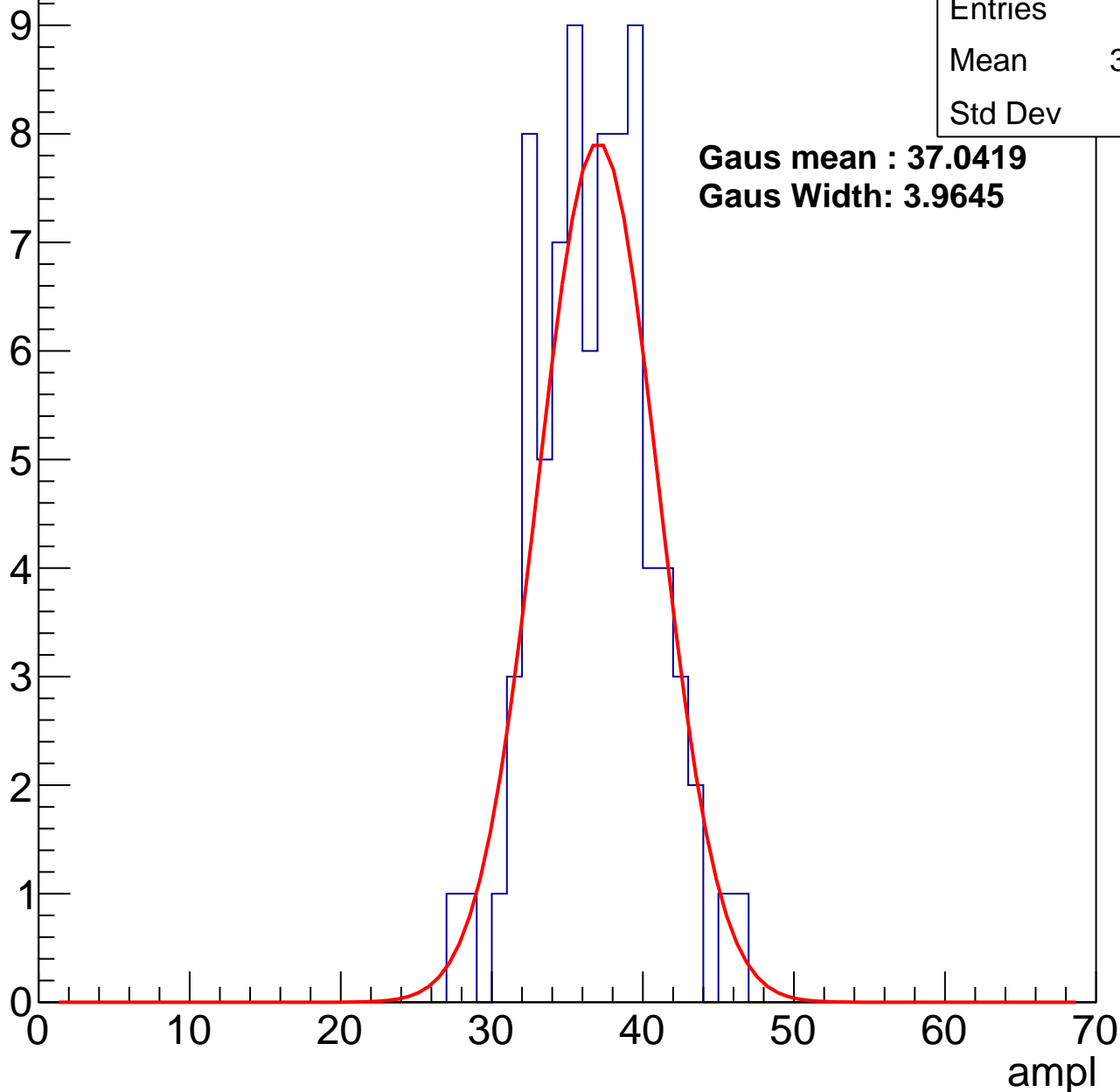
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	36.37
Std Dev	3.73

**Gaus mean : 37.0419**

**Gaus Width: 3.9645**



# B1L101S, U16-ch97, adc2

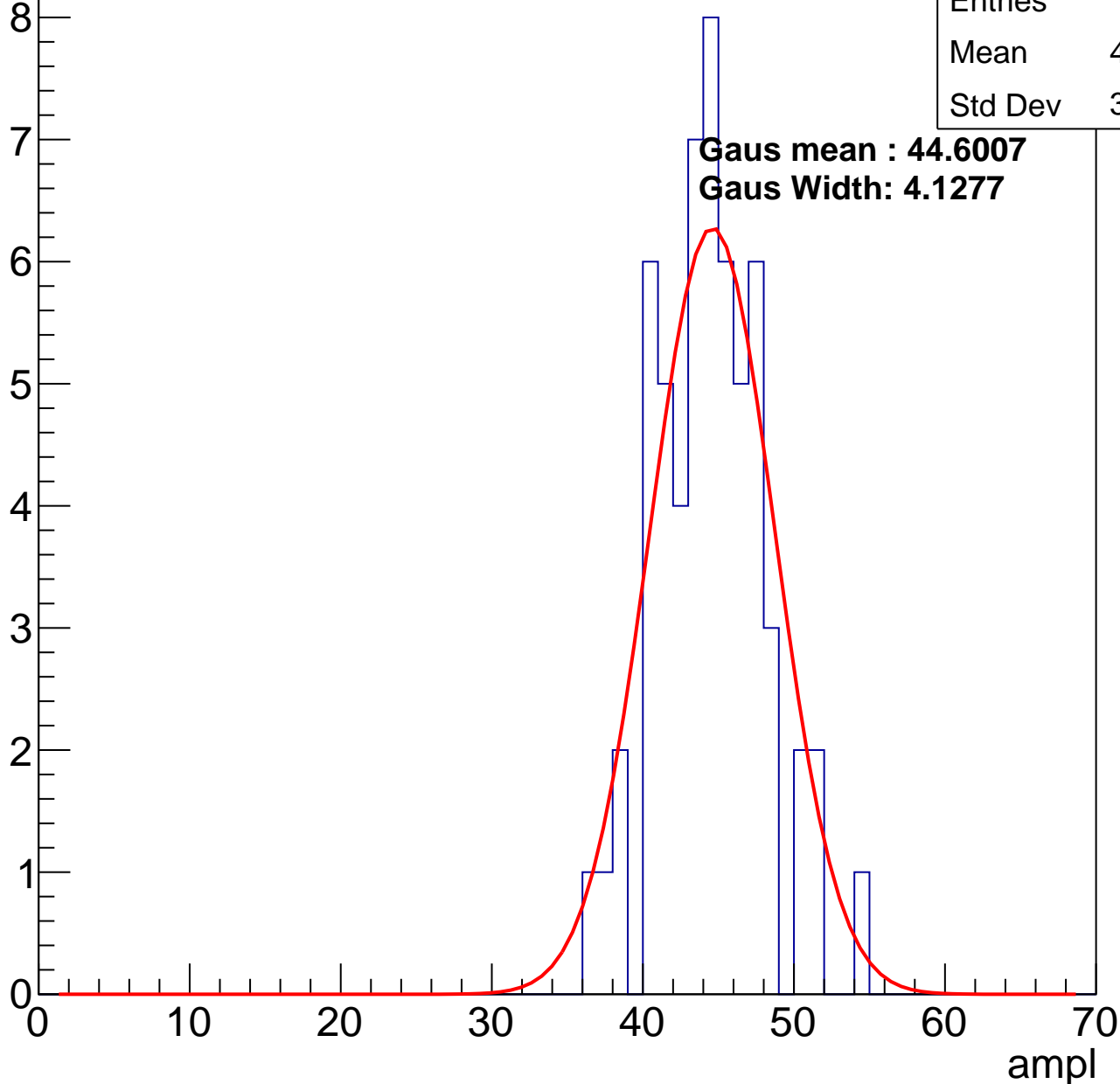
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	44.02
Std Dev	3.558

**Gaus mean : 44.6007**

**Gaus Width: 4.1277**

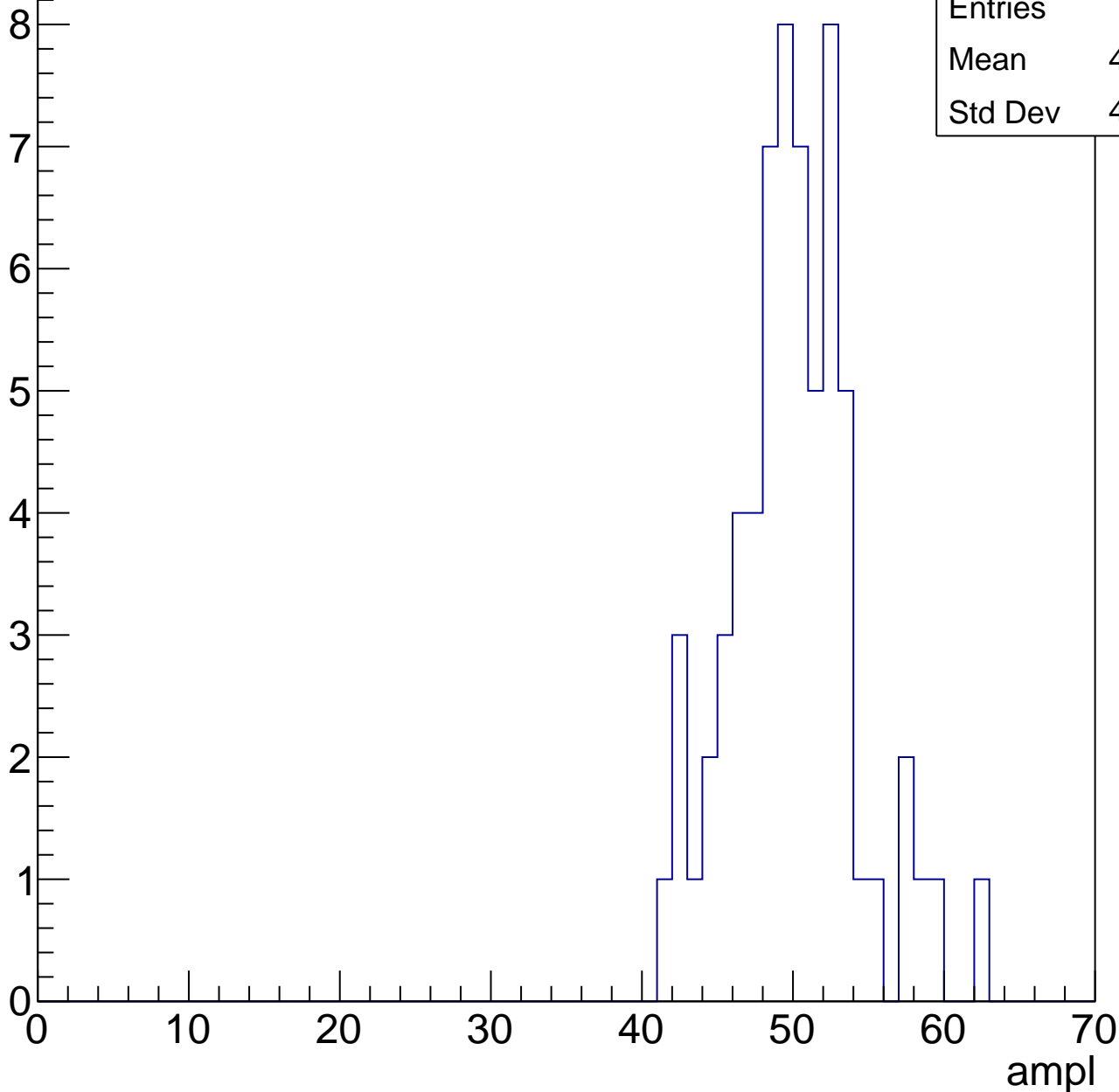


# B1L101S, U16-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

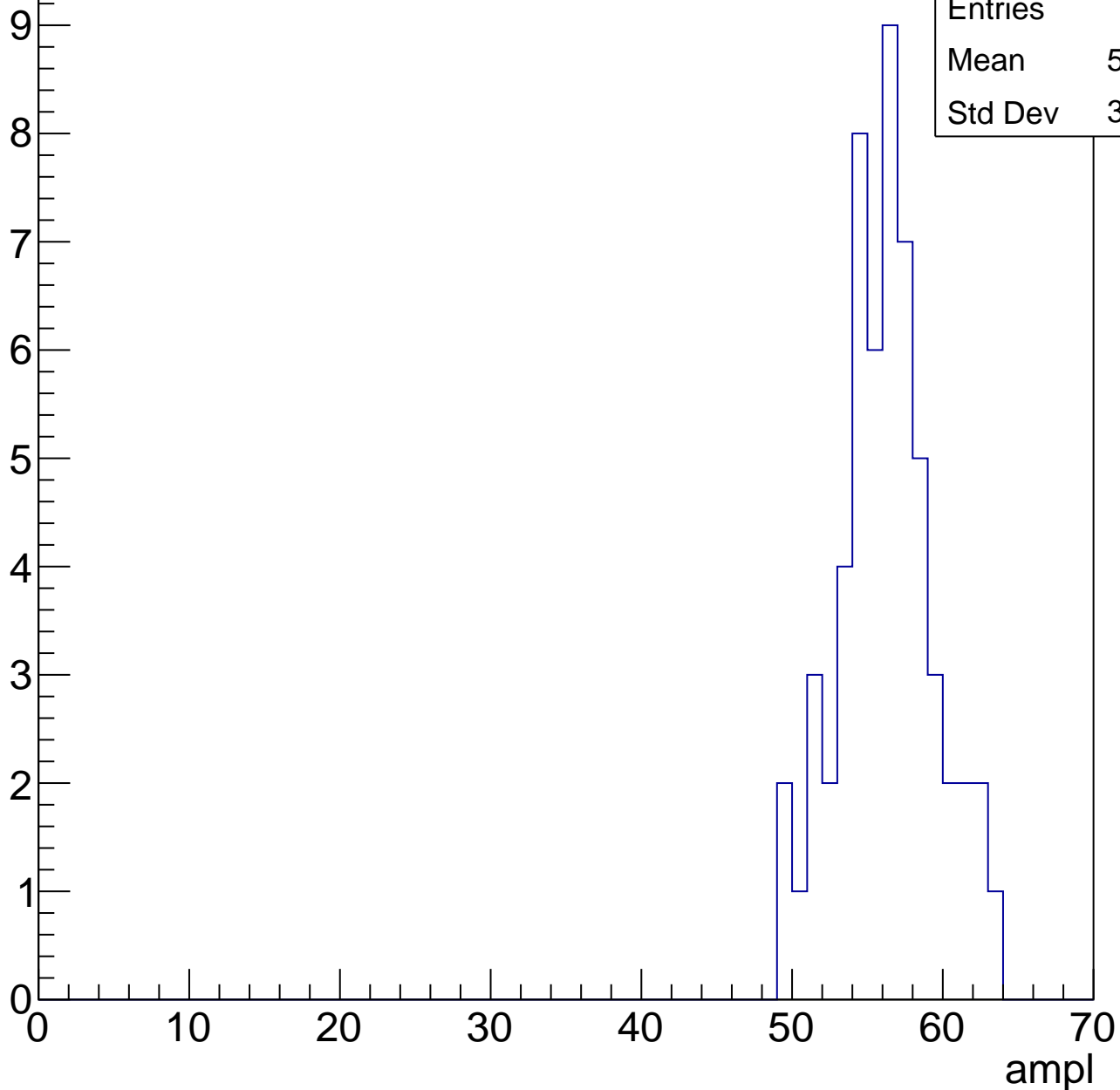
Entries	65
Mean	49.55
Std Dev	4.118



# B1L101S, U16-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

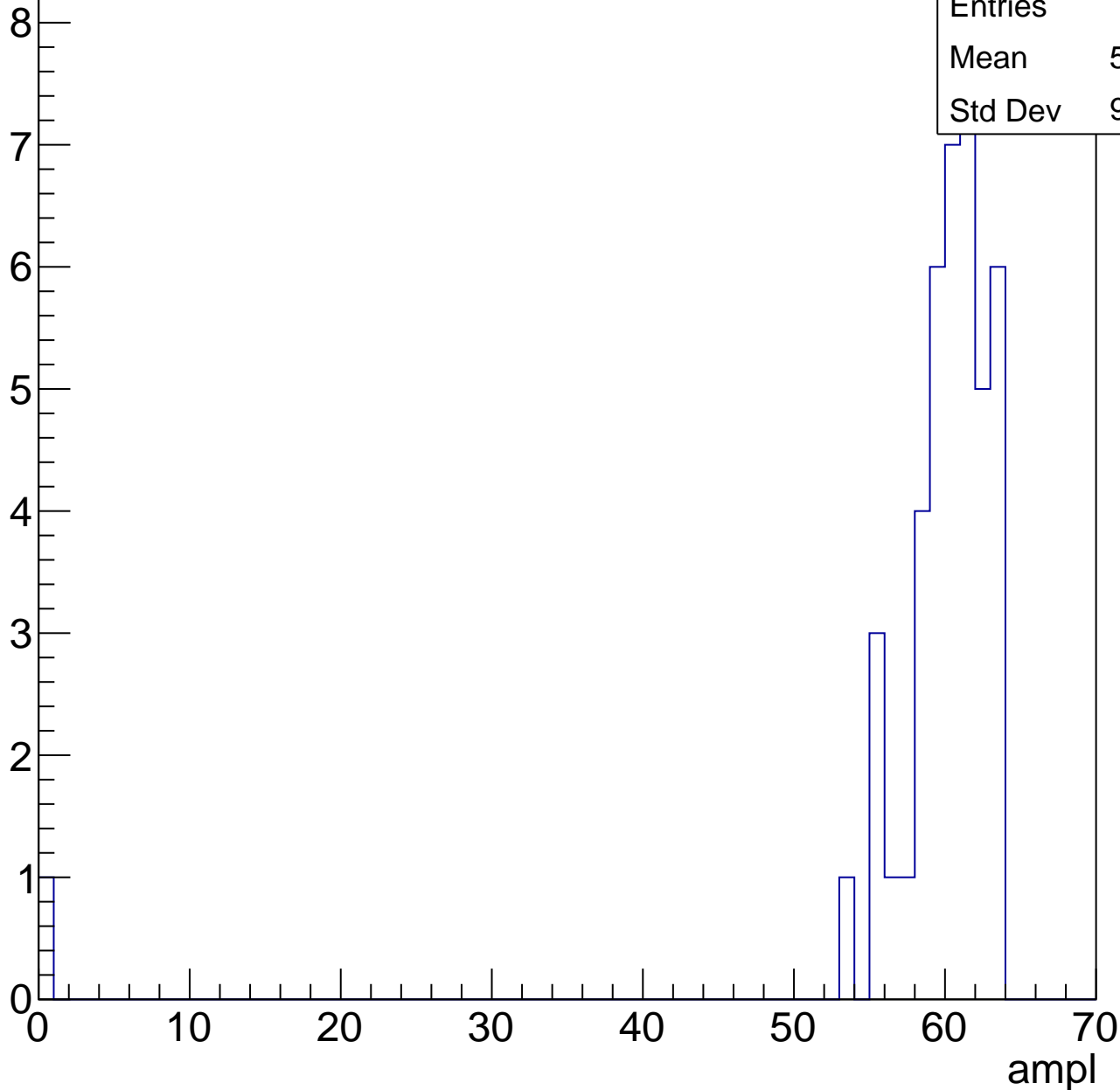


# B1L101S, U16-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	58.44
Std Dev	9.337



# B1L101S, U16-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch98, adc0

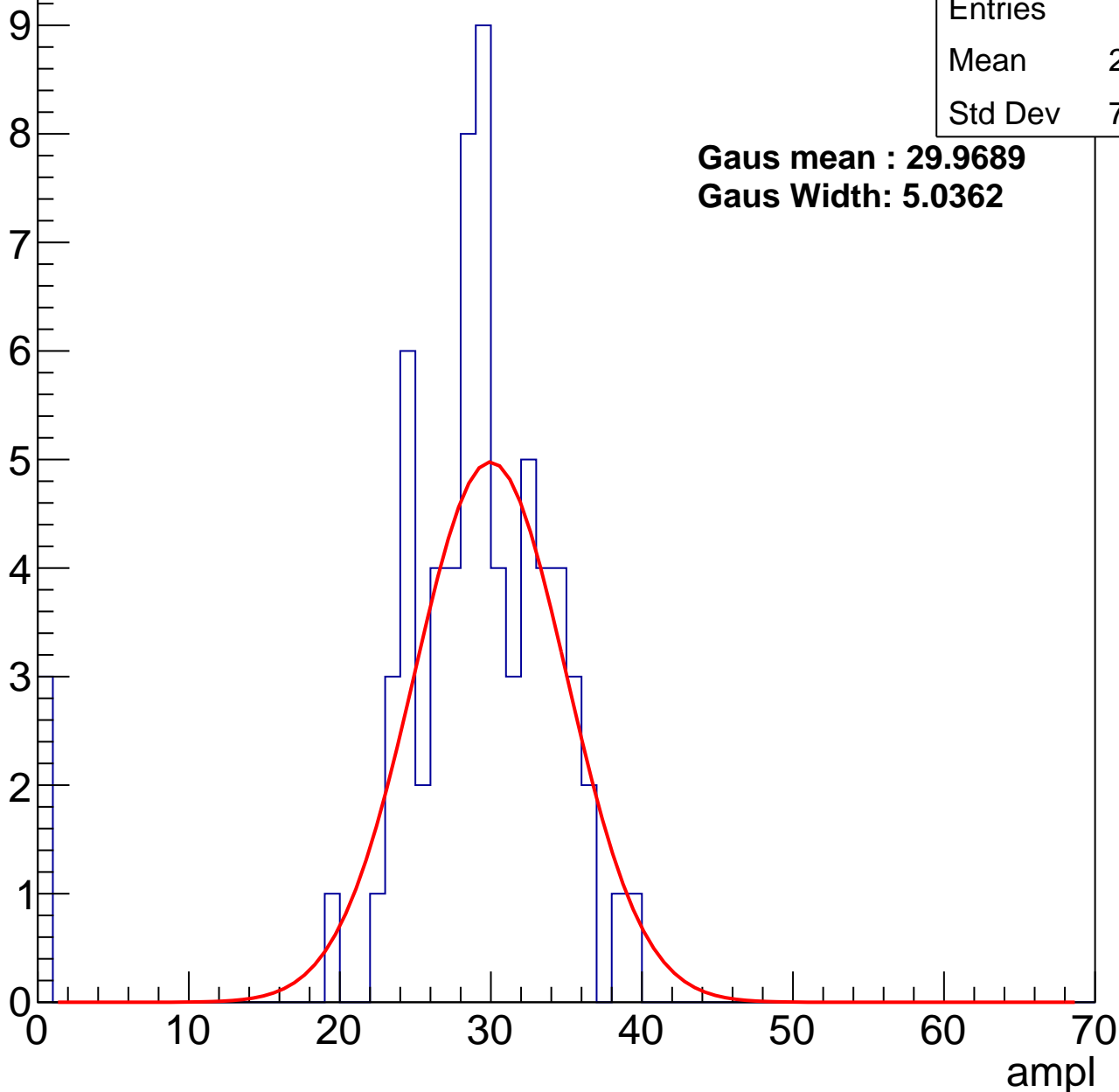
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	27.88
Std Dev	7.224

**Gaus mean : 29.9689**

**Gaus Width: 5.0362**



# B1L101S, U16-ch98, adc1

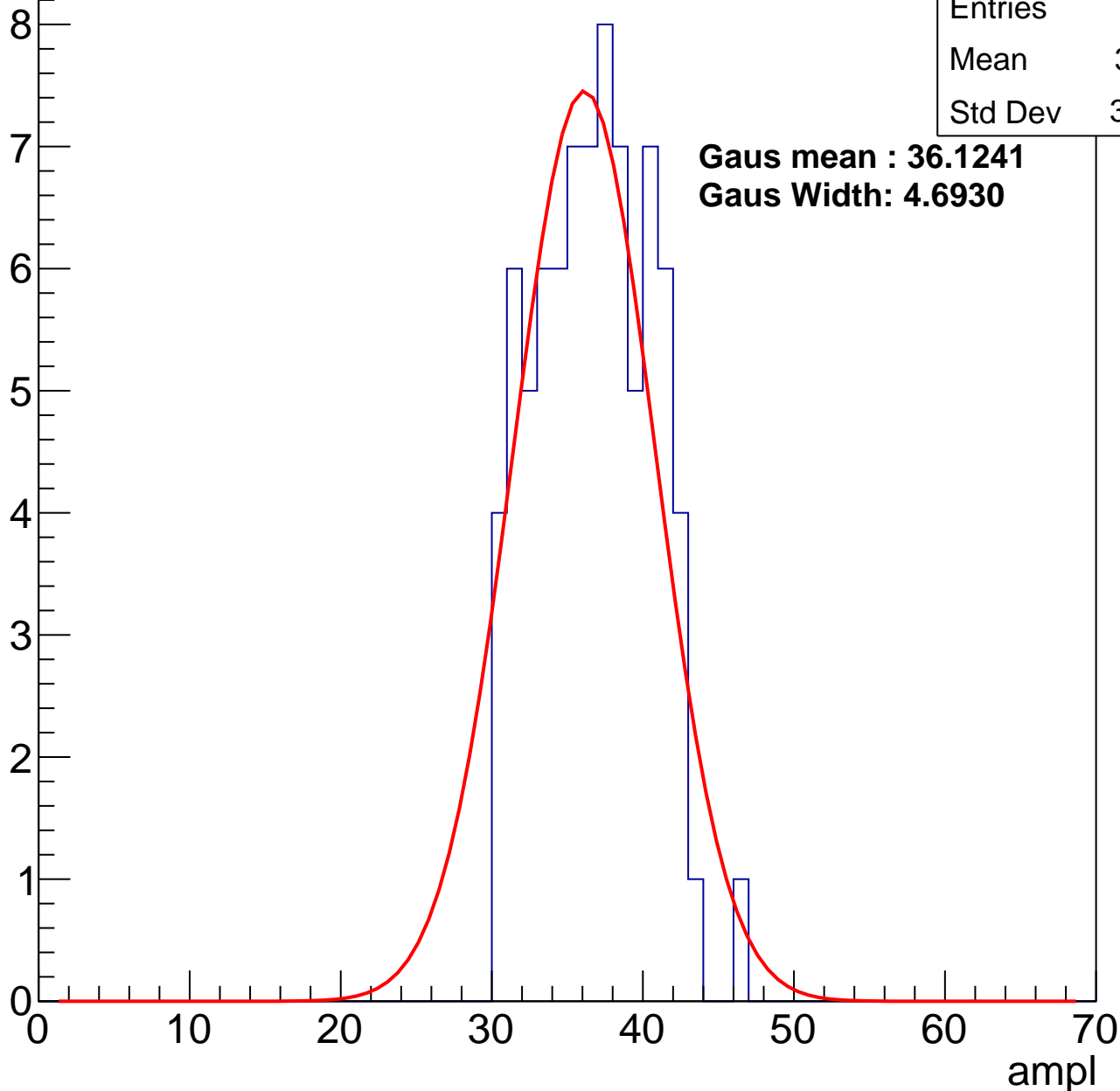
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	36.31
Std Dev	3.686

**Gaus mean : 36.1241**

**Gaus Width: 4.6930**



# B1L101S, U16-ch98, adc2

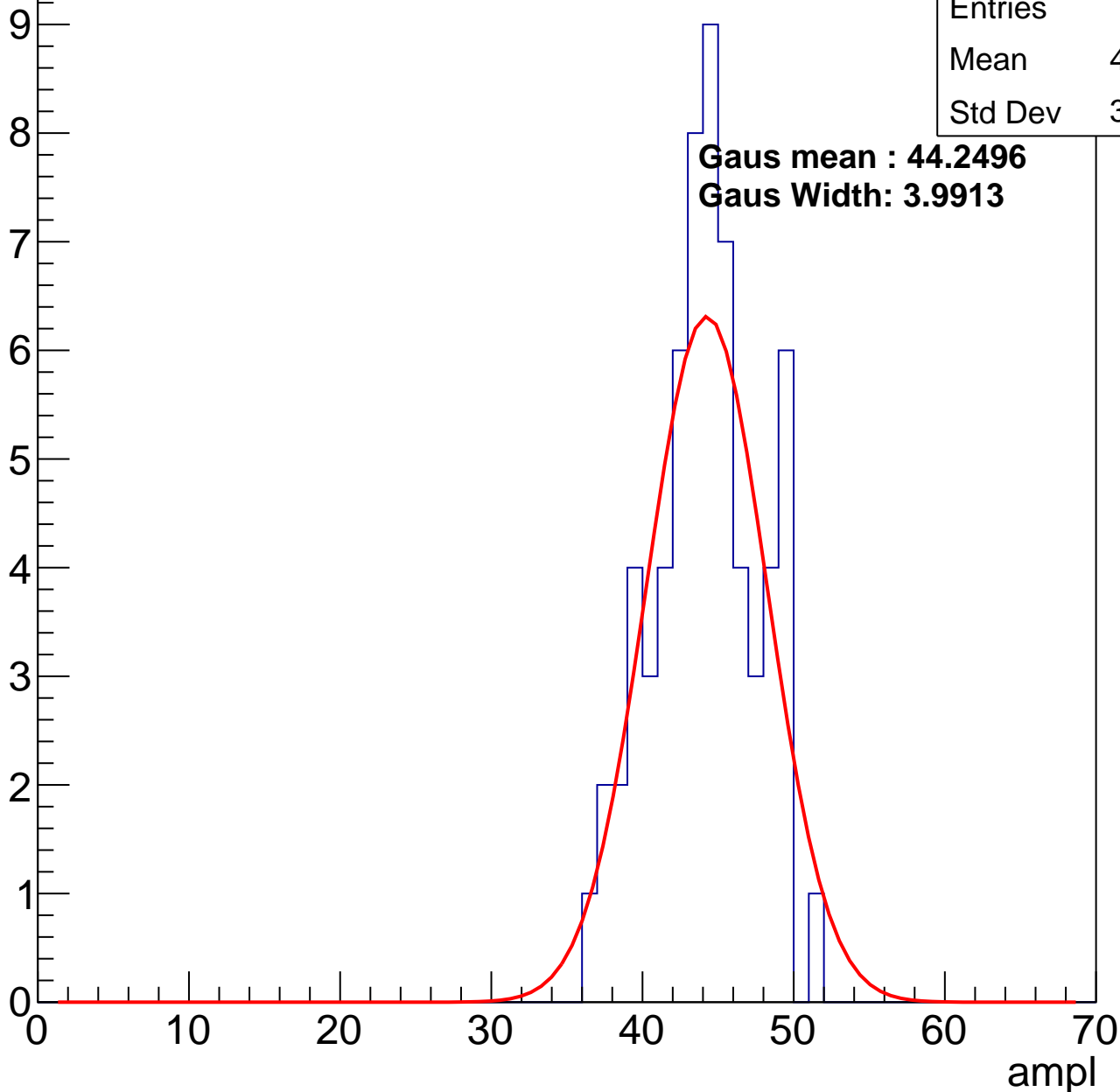
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	43.67
Std Dev	3.437

**Gaus mean : 44.2496**

**Gaus Width: 3.9913**

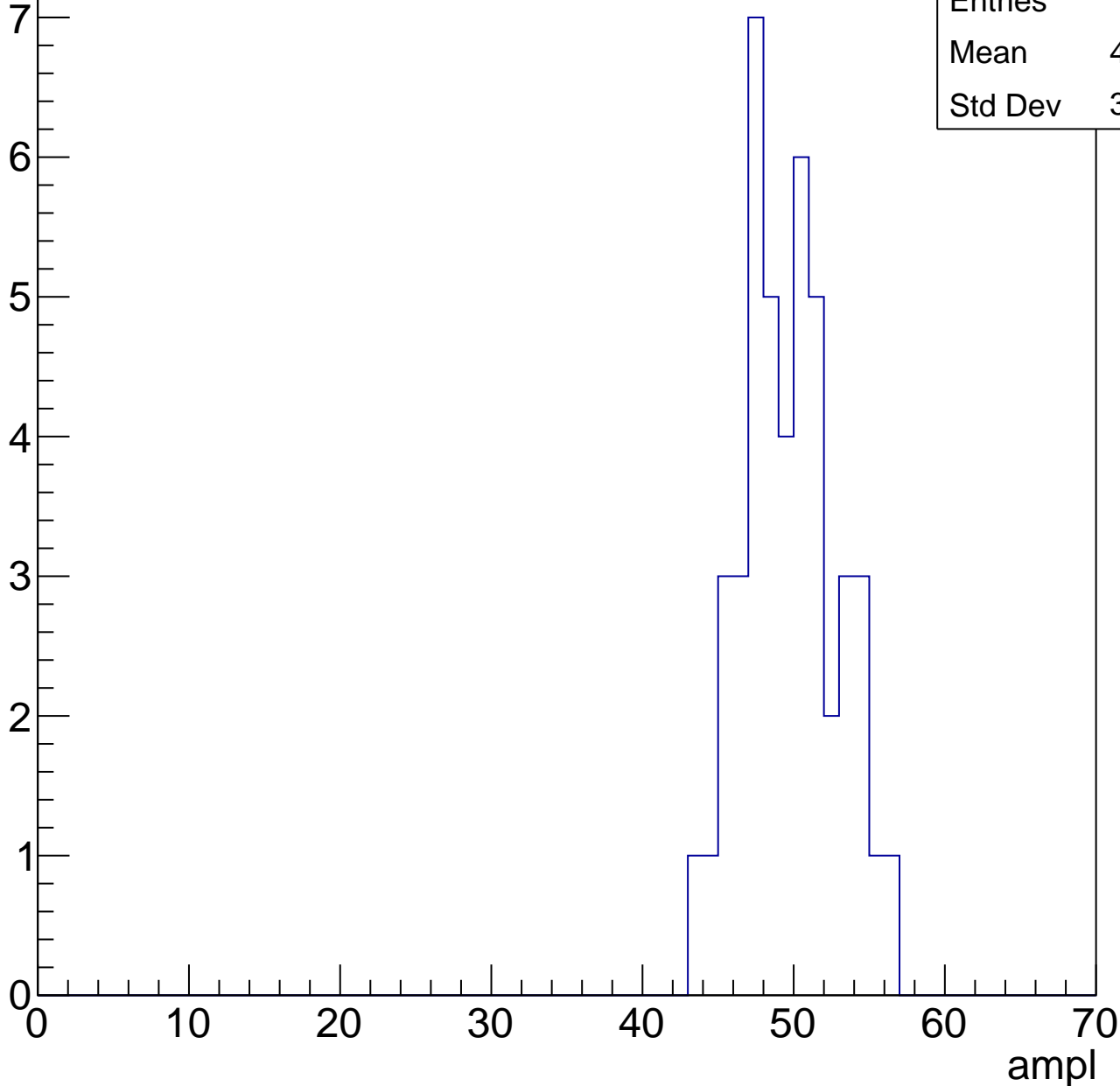


# B1L101S, U16-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

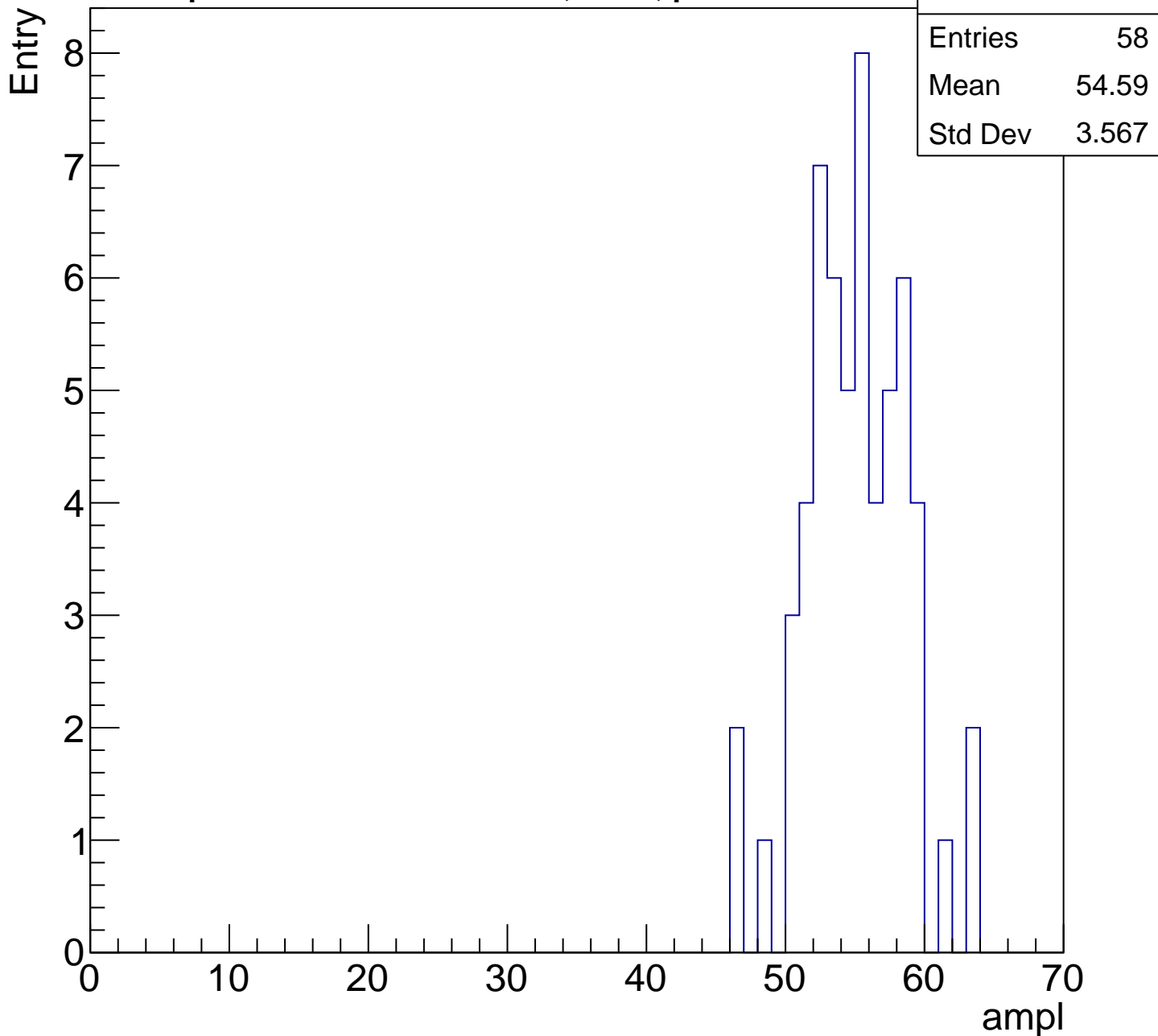
Entry

Entries	45
Mean	49.24
Std Dev	3.049



# B1L101S, U16-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

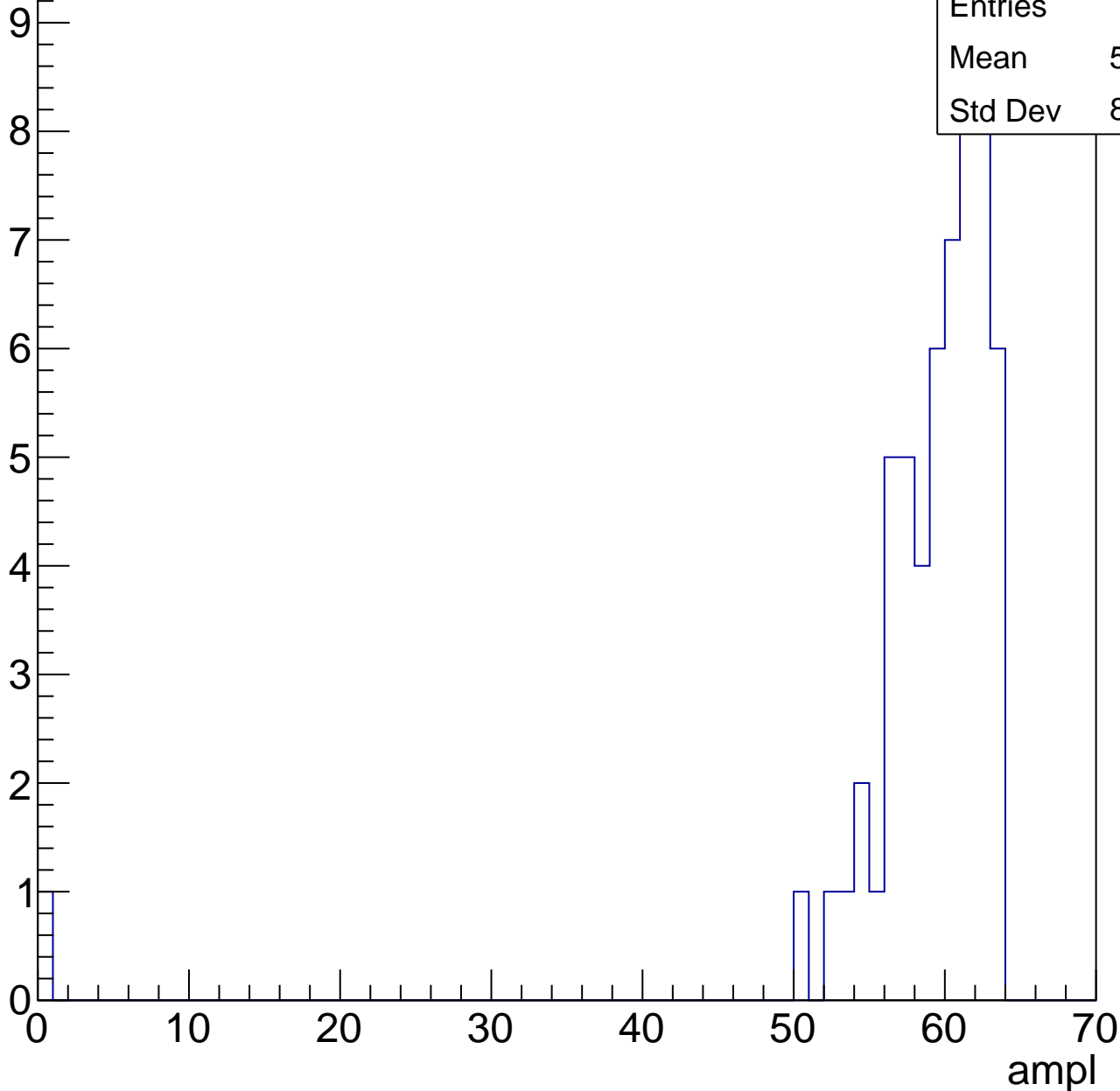


# B1L101S, U16-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

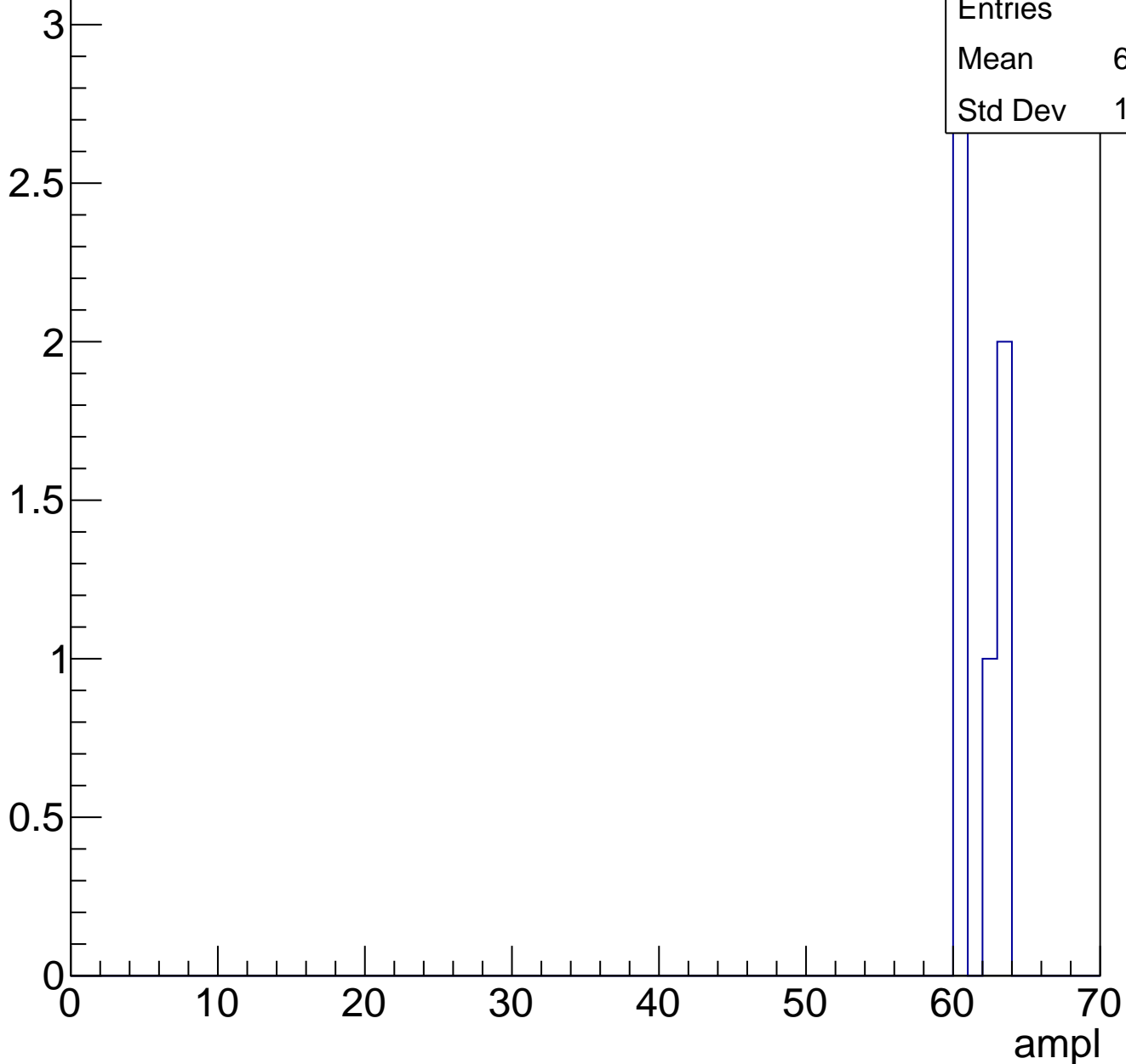
Entries	58
Mean	58.17
Std Dev	8.265



# B1L101S, U16-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U16-ch99, adc0

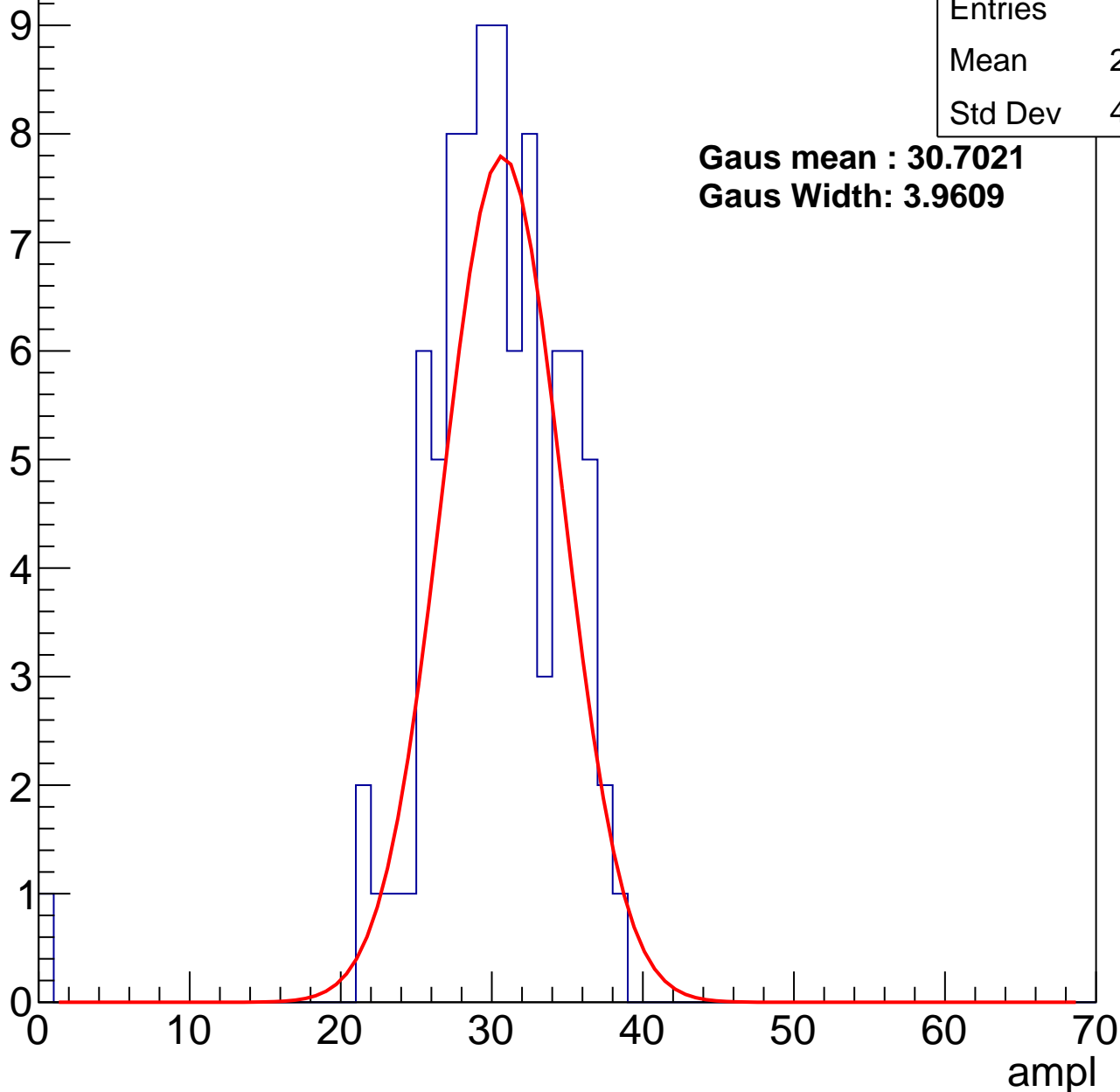
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	88
Mean	29.65
Std Dev	4.996

**Gaus mean : 30.7021**

**Gaus Width: 3.9609**



# B1L101S, U16-ch99, adc1

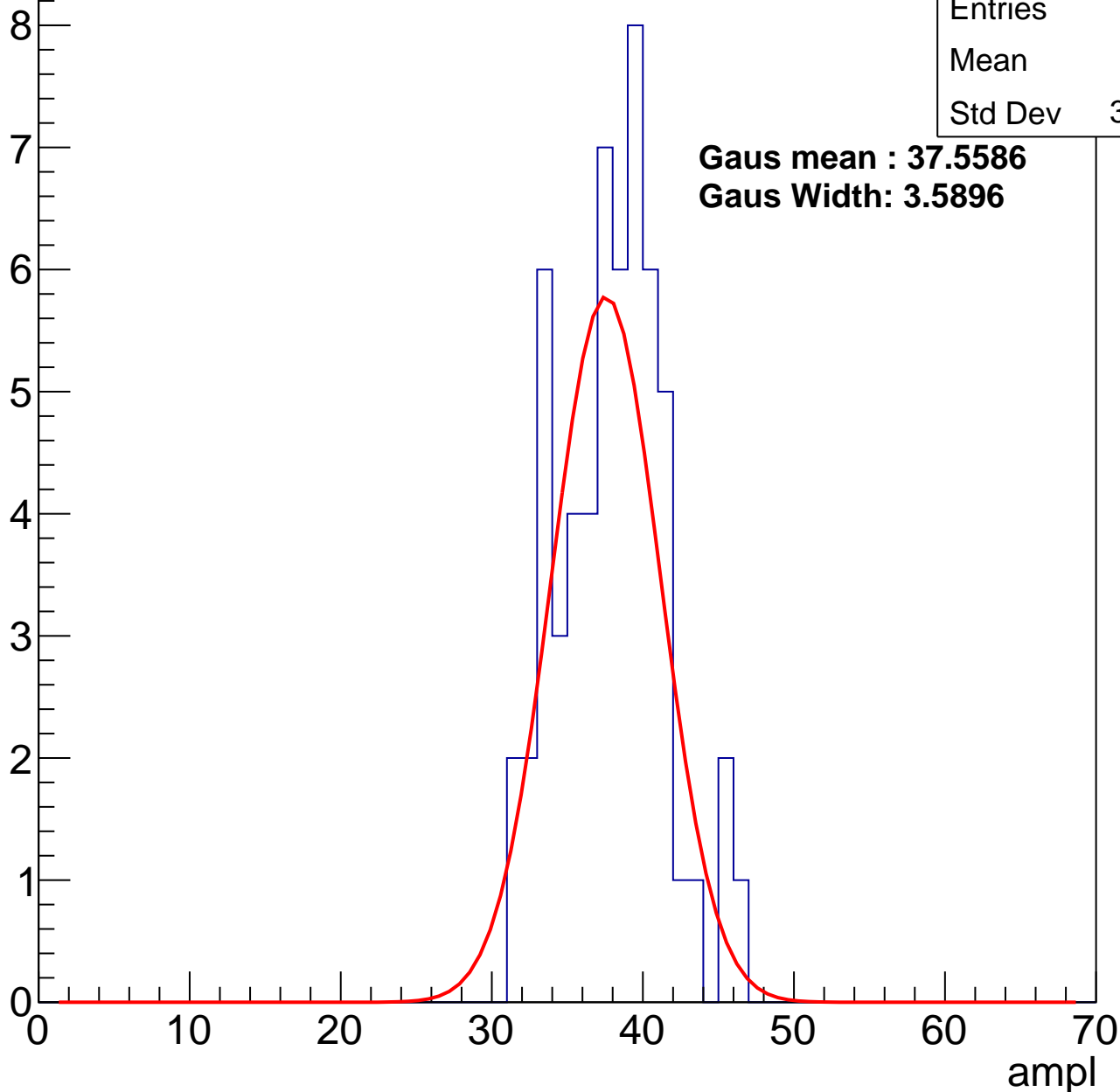
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	37.5
Std Dev	3.455

**Gaus mean : 37.5586**

**Gaus Width: 3.5896**



# B1L101S, U16-ch99, adc2

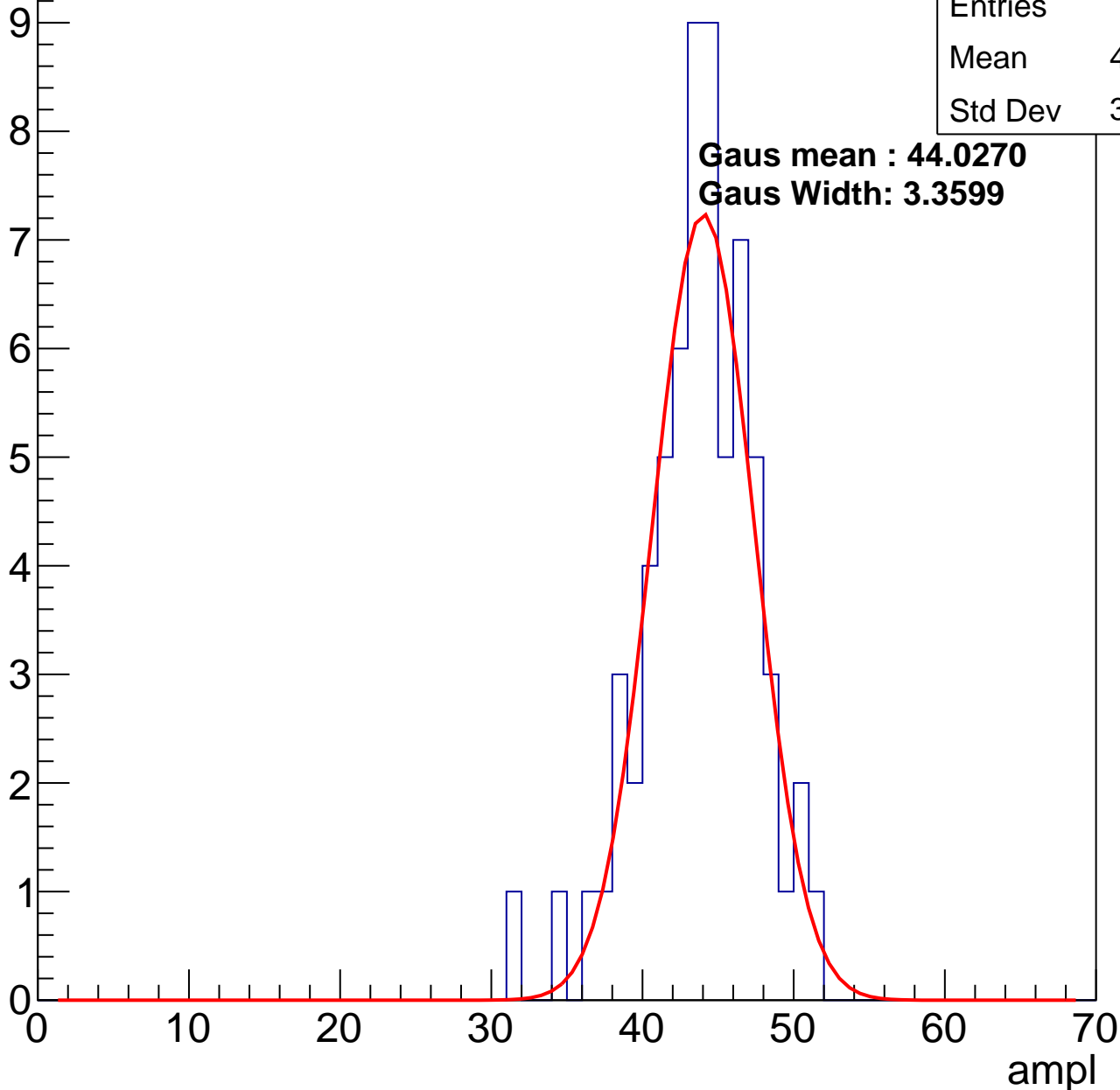
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	43.27
Std Dev	3.732

**Gaus mean : 44.0270**

**Gaus Width: 3.3599**

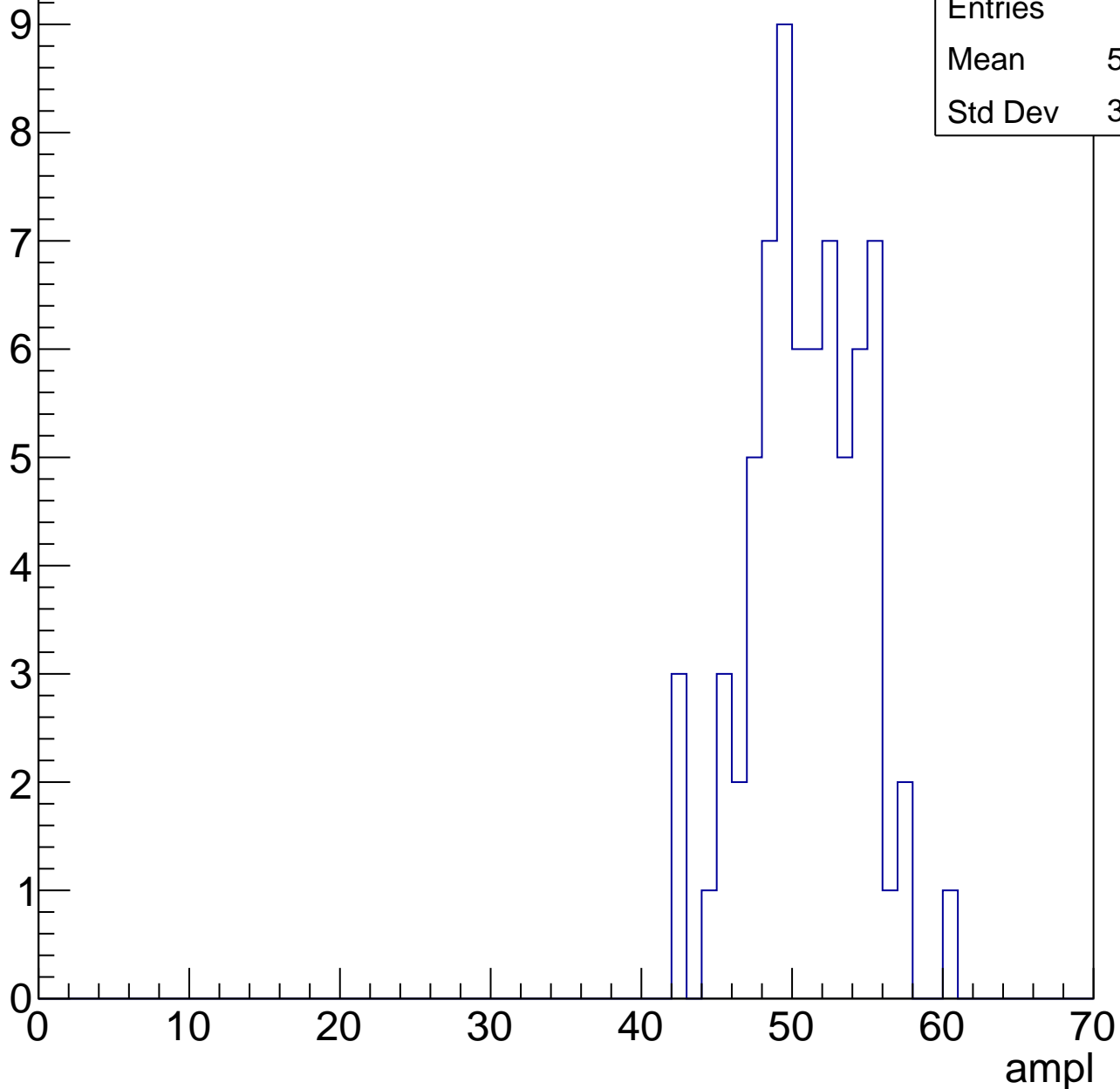


# B1L101S, U16-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	50.46
Std Dev	3.726

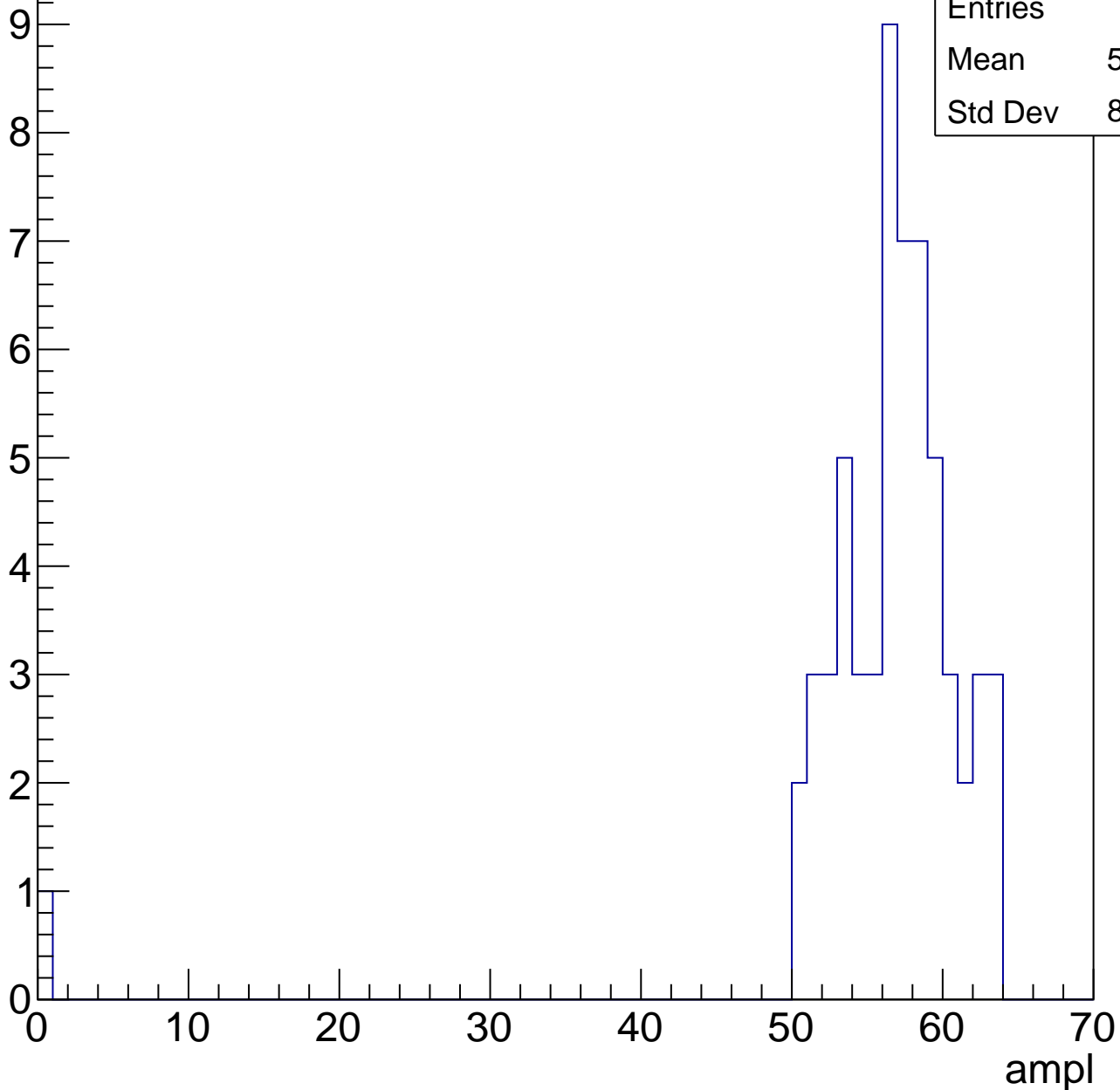


# B1L101S, U16-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

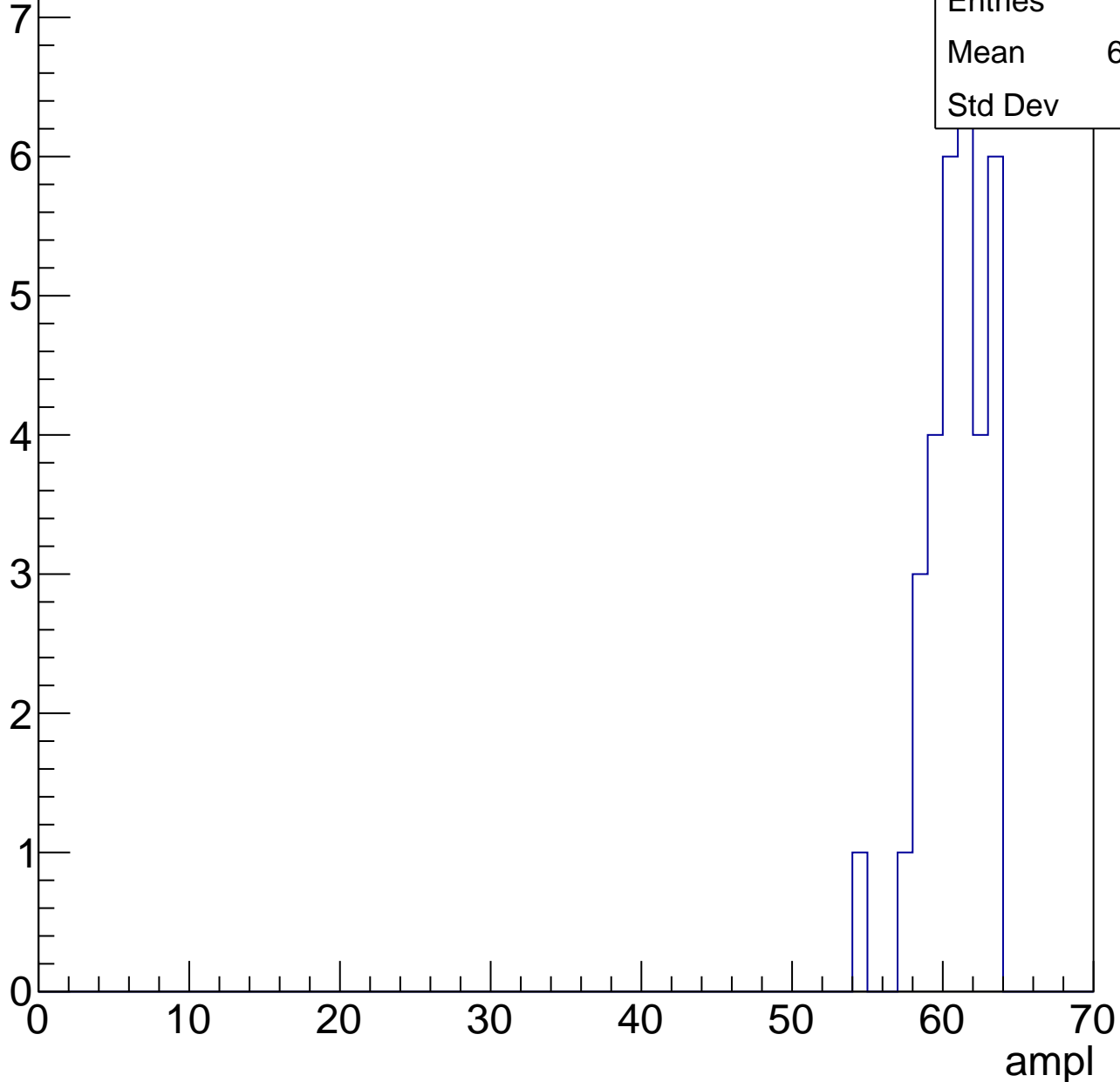
Entries	59
Mean	55.63
Std Dev	8.042



# B1L101S, U16-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

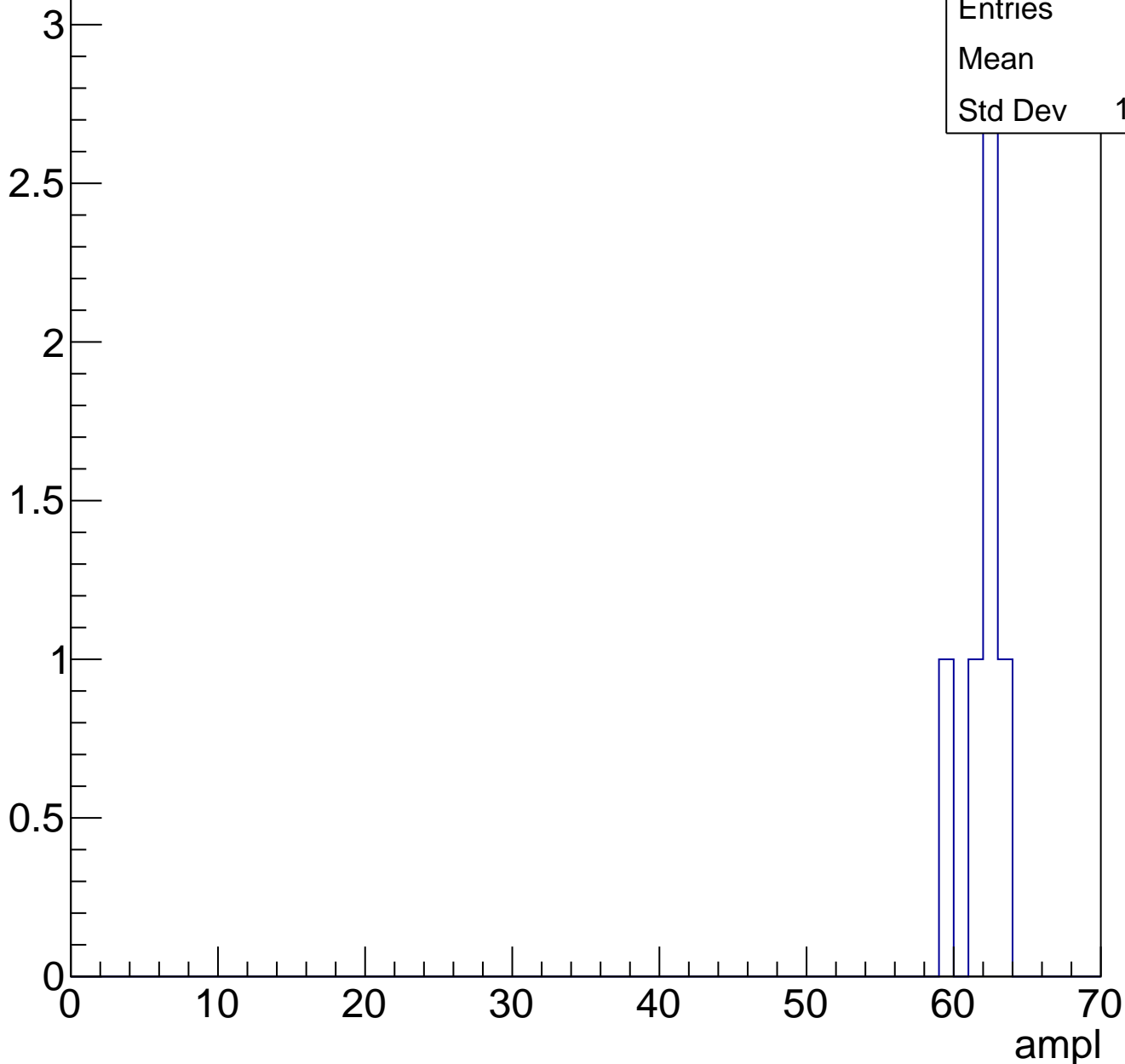
Entry



# B1L101S, U16-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U16-ch100, adc0

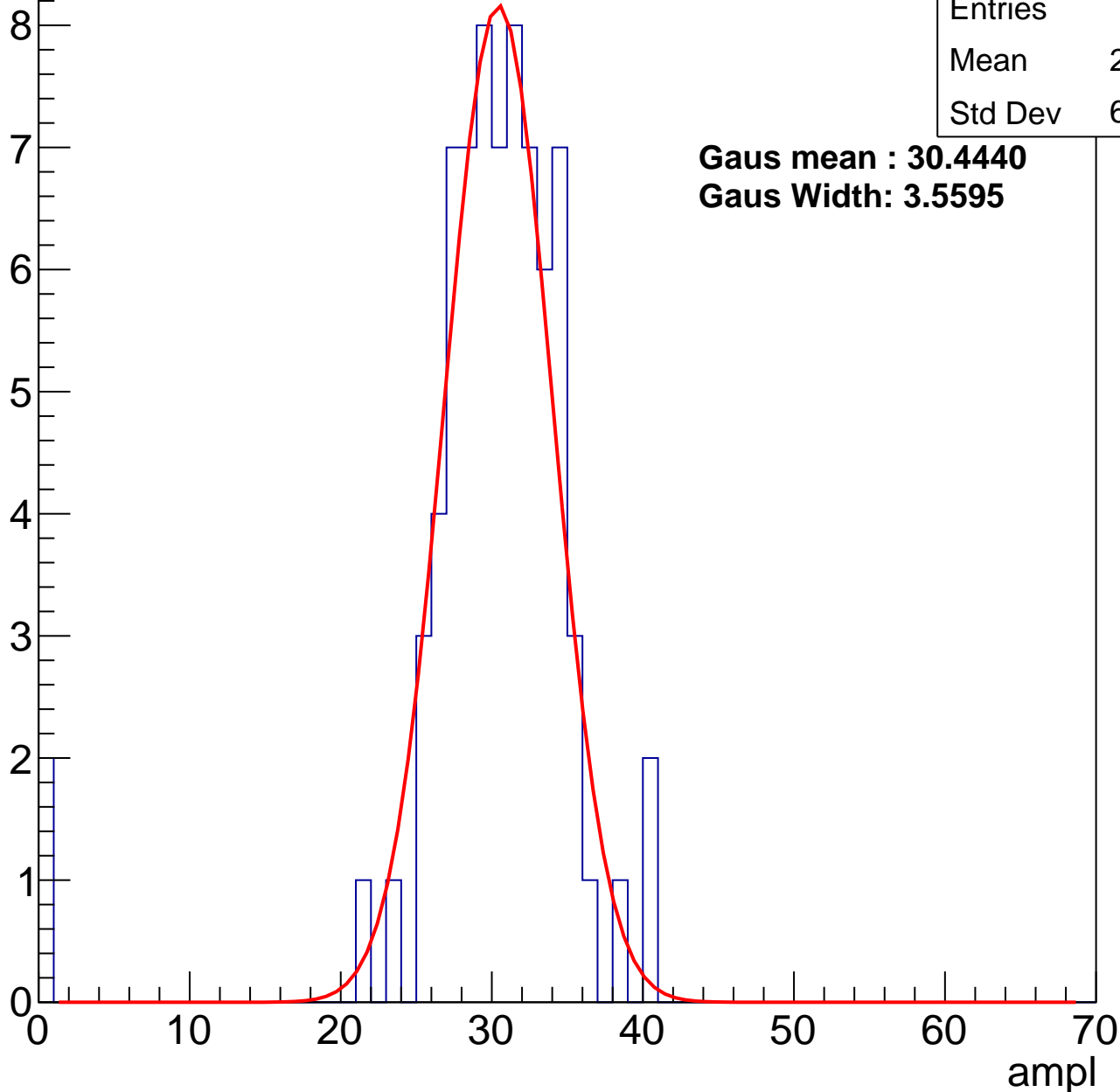
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	29.56
Std Dev	6.034

**Gaus mean : 30.4440**

**Gaus Width: 3.5595**



# B1L101S, U16-ch100, adc1

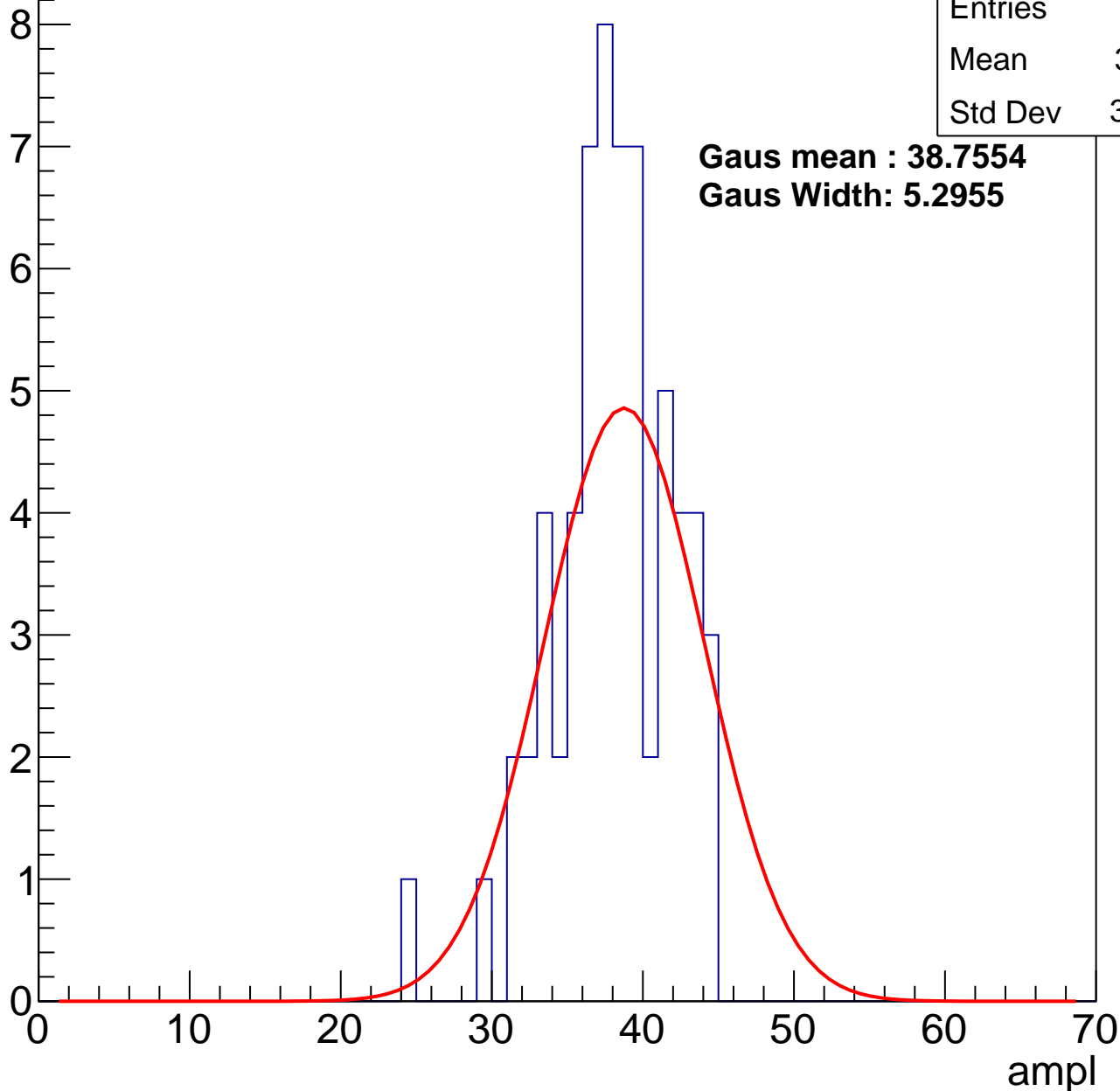
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	37.51
Std Dev	3.919

**Gaus mean : 38.7554**

**Gaus Width: 5.2955**



# B1L101S, U16-ch100, adc2

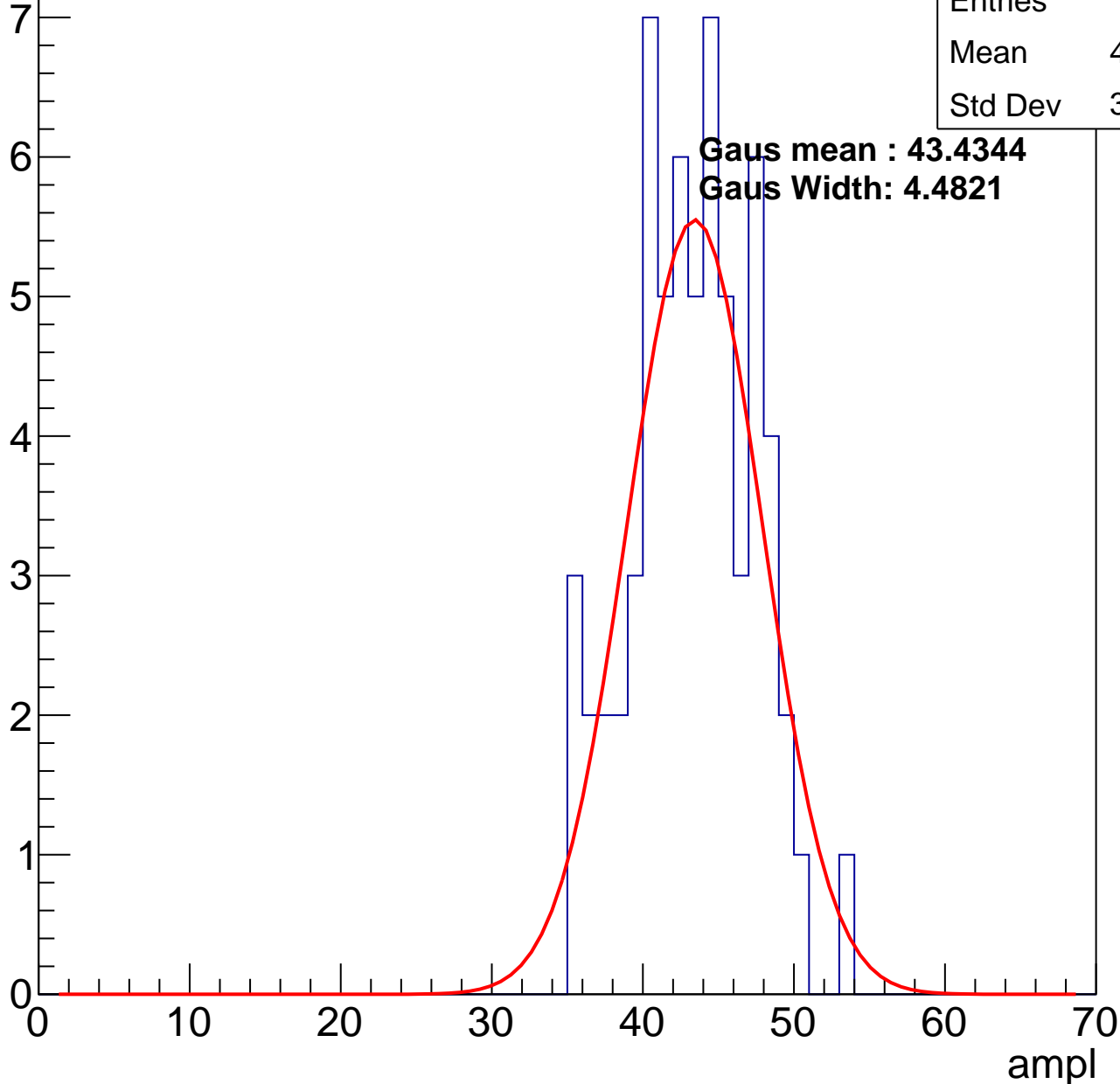
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	42.84
Std Dev	3.989

**Gaus mean : 43.4344**

**Gaus Width: 4.4821**

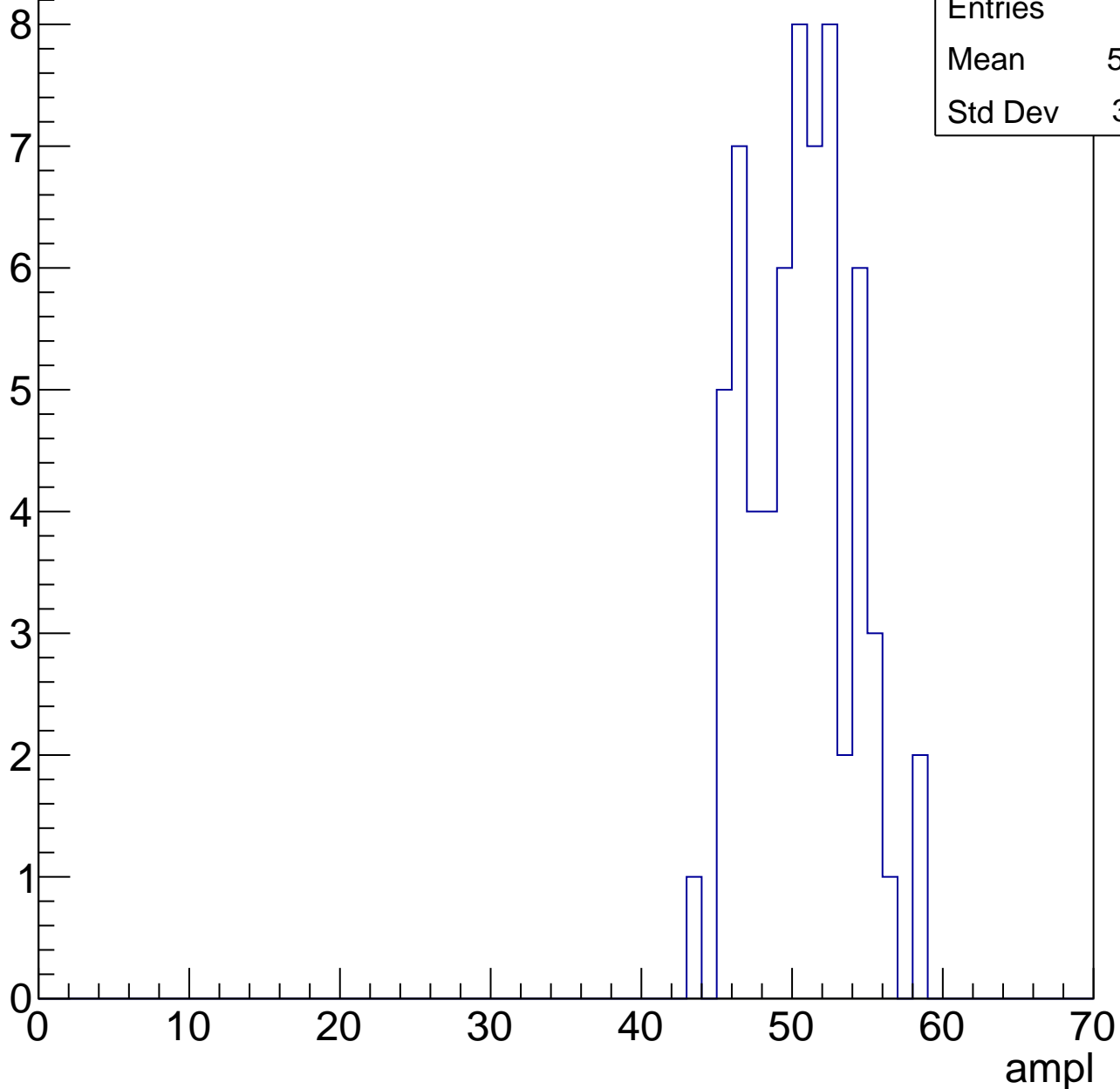


# B1L101S, U16-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	50.06
Std Dev	3.391

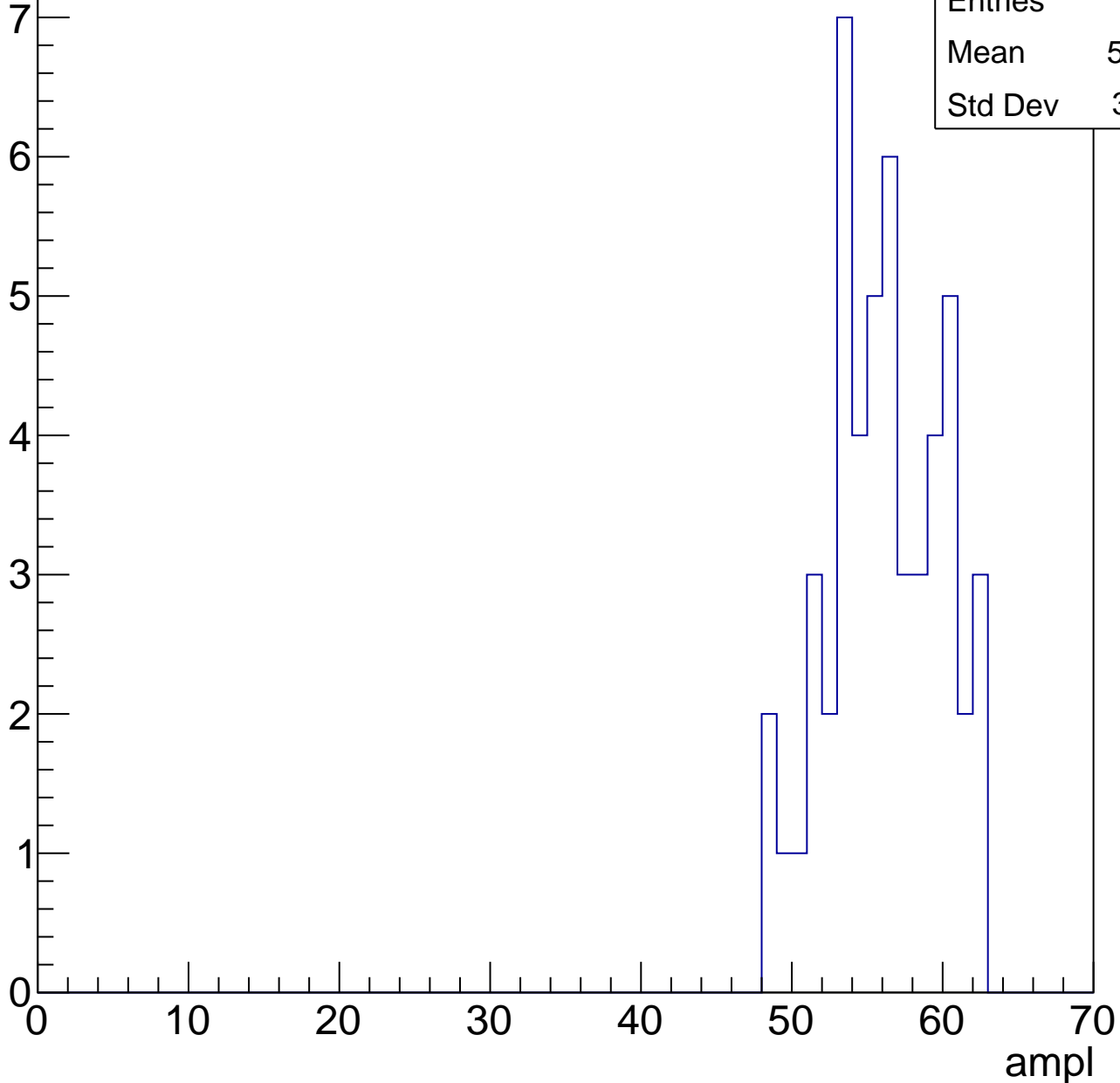


# B1L101S, U16-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	55.67
Std Dev	3.671

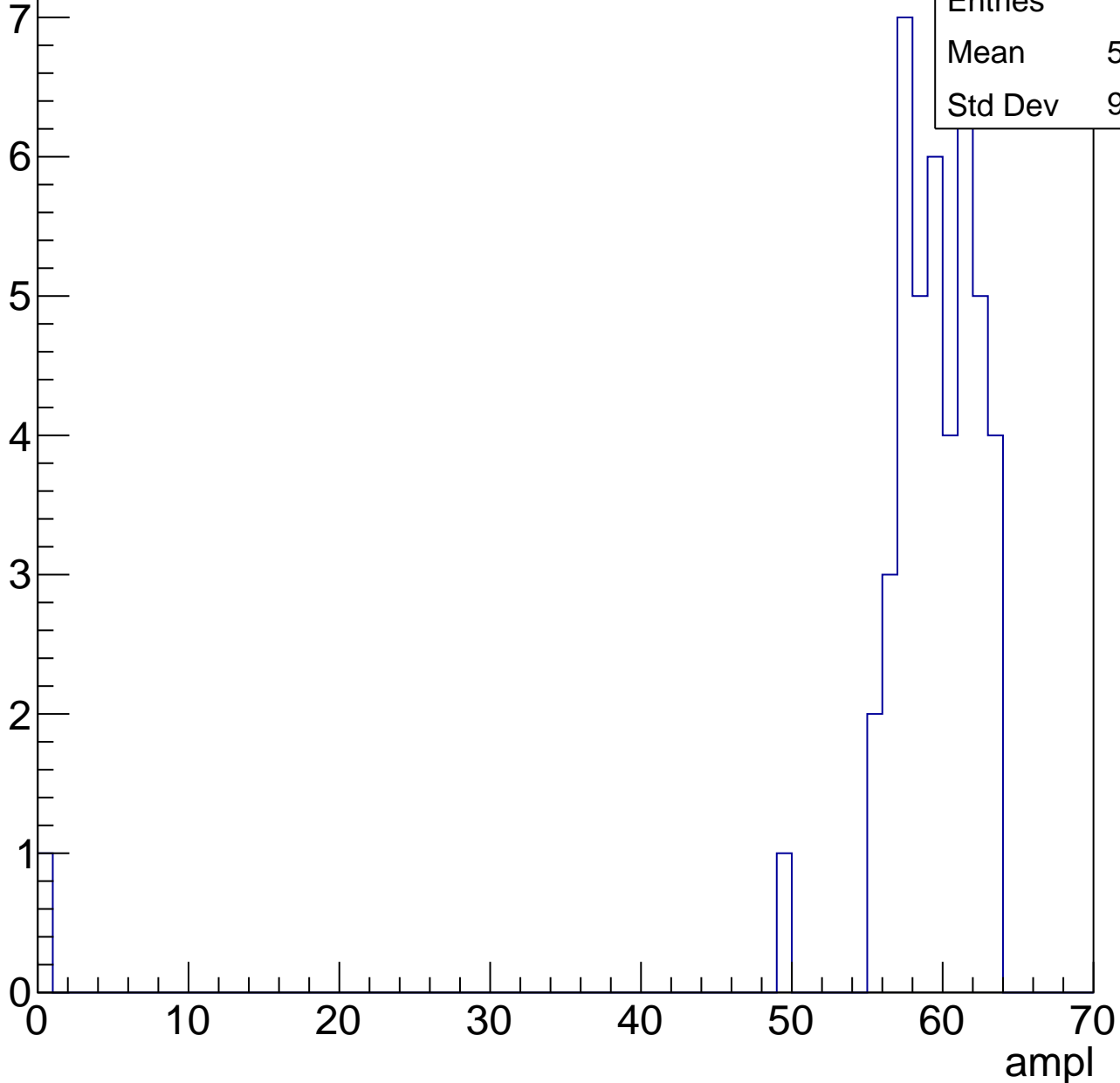


# B1L101S, U16-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	57.76
Std Dev	9.122

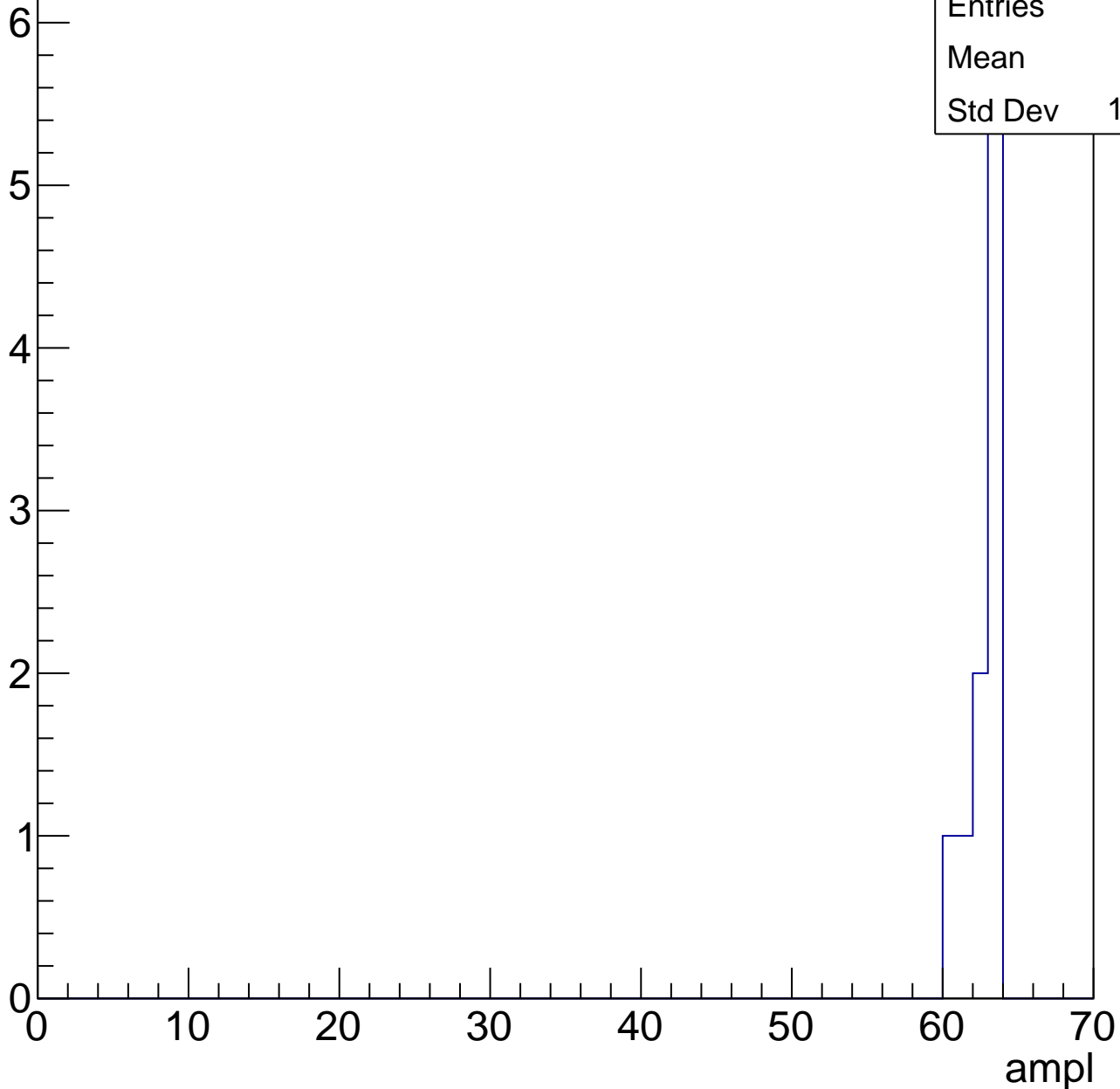


# B1L101S, U16-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	10
Mean	62.3
Std Dev	1.005





# B1L101S, U16-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U16-ch101, adc0

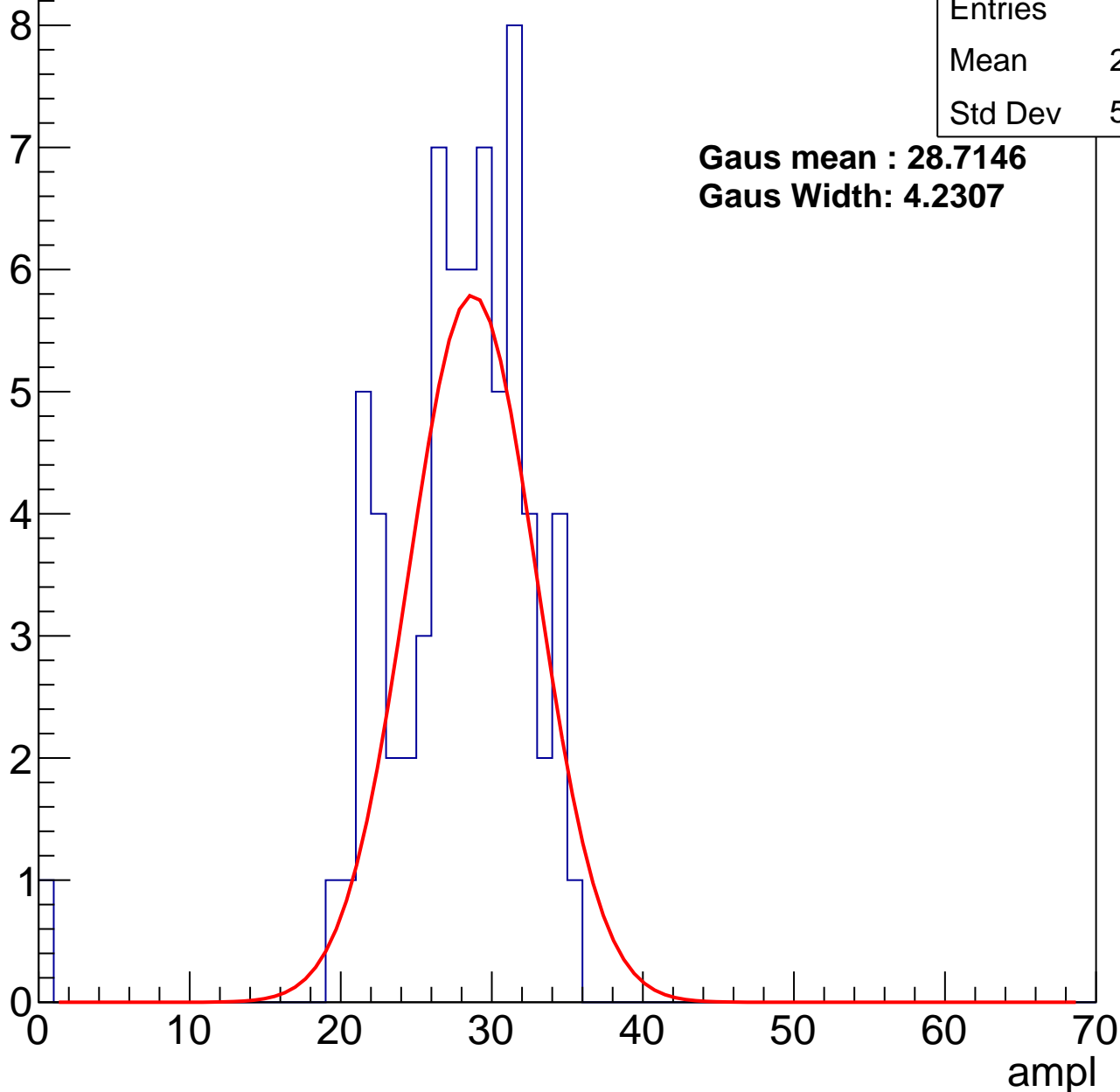
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	27.23
Std Dev	5.145

**Gaus mean : 28.7146**

**Gaus Width: 4.2307**



# B1L101S, U16-ch101, adc1

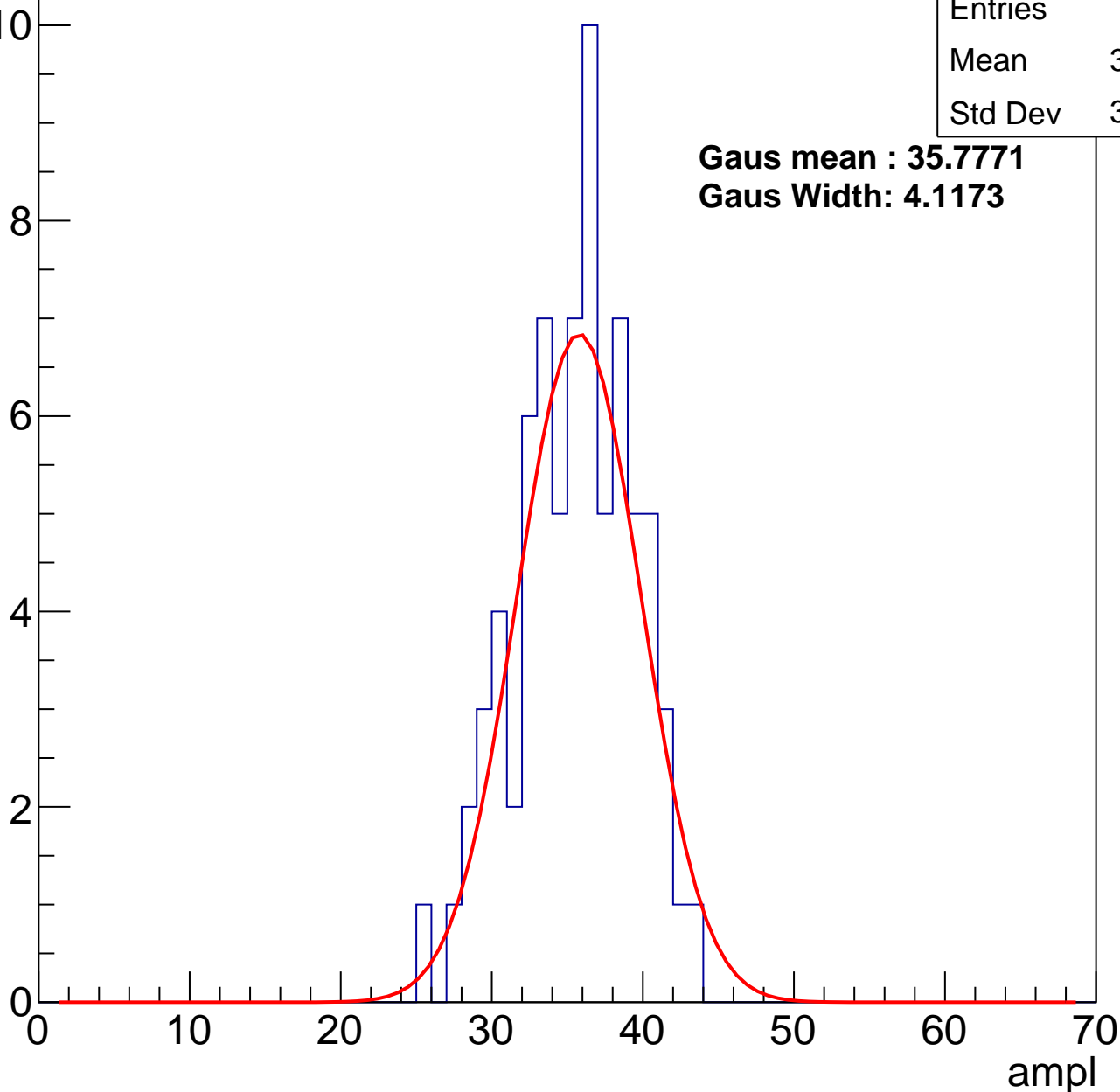
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	35.05
Std Dev	3.843

**Gaus mean : 35.7771**

**Gaus Width: 4.1173**



# B1L101S, U16-ch101, adc2

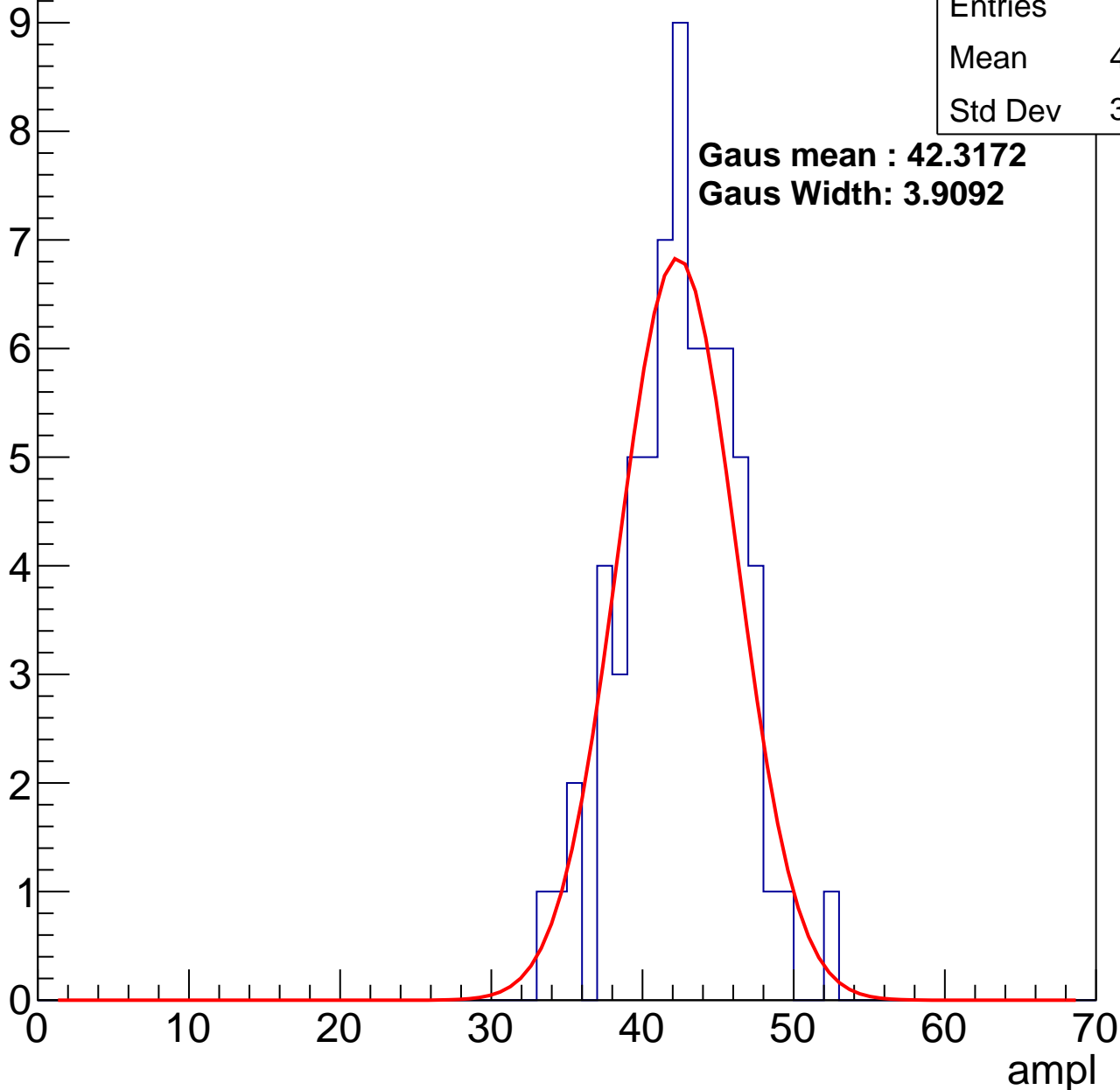
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	42.06
Std Dev	3.689

**Gaus mean : 42.3172**

**Gaus Width: 3.9092**

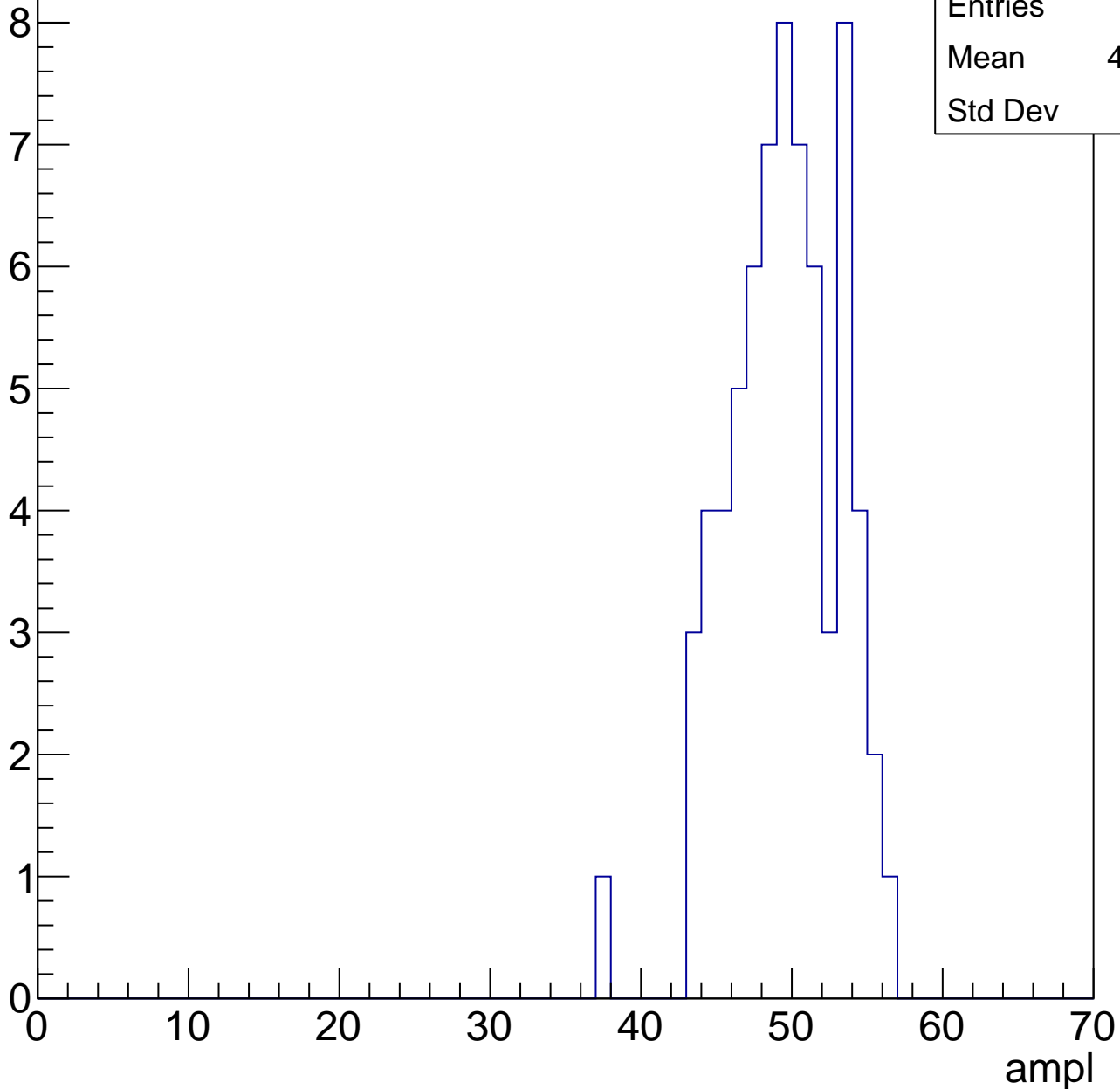


# B1L101S, U16-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

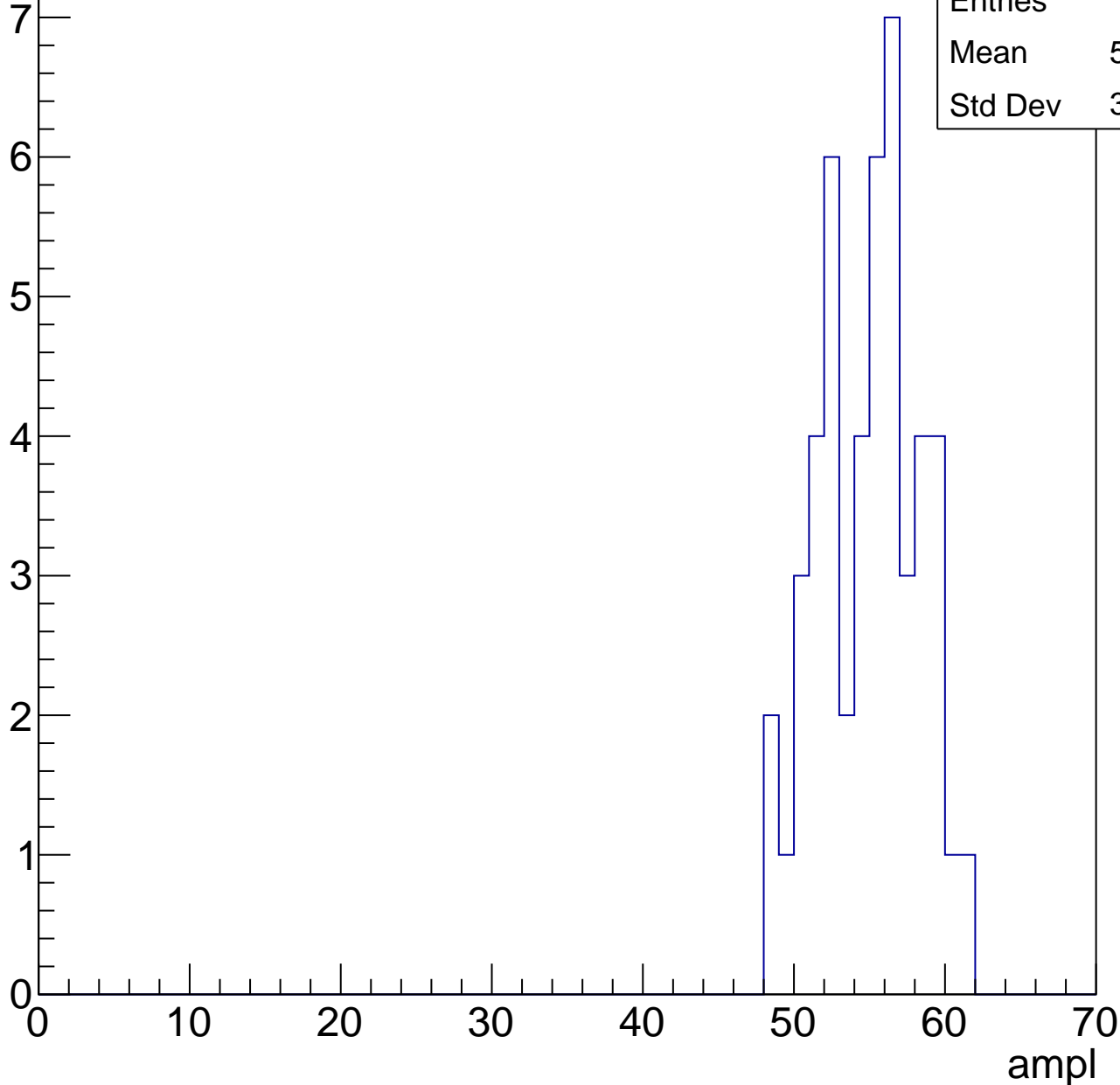
Entries	69
Mean	48.99
Std Dev	3.61



# B1L101S, U16-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

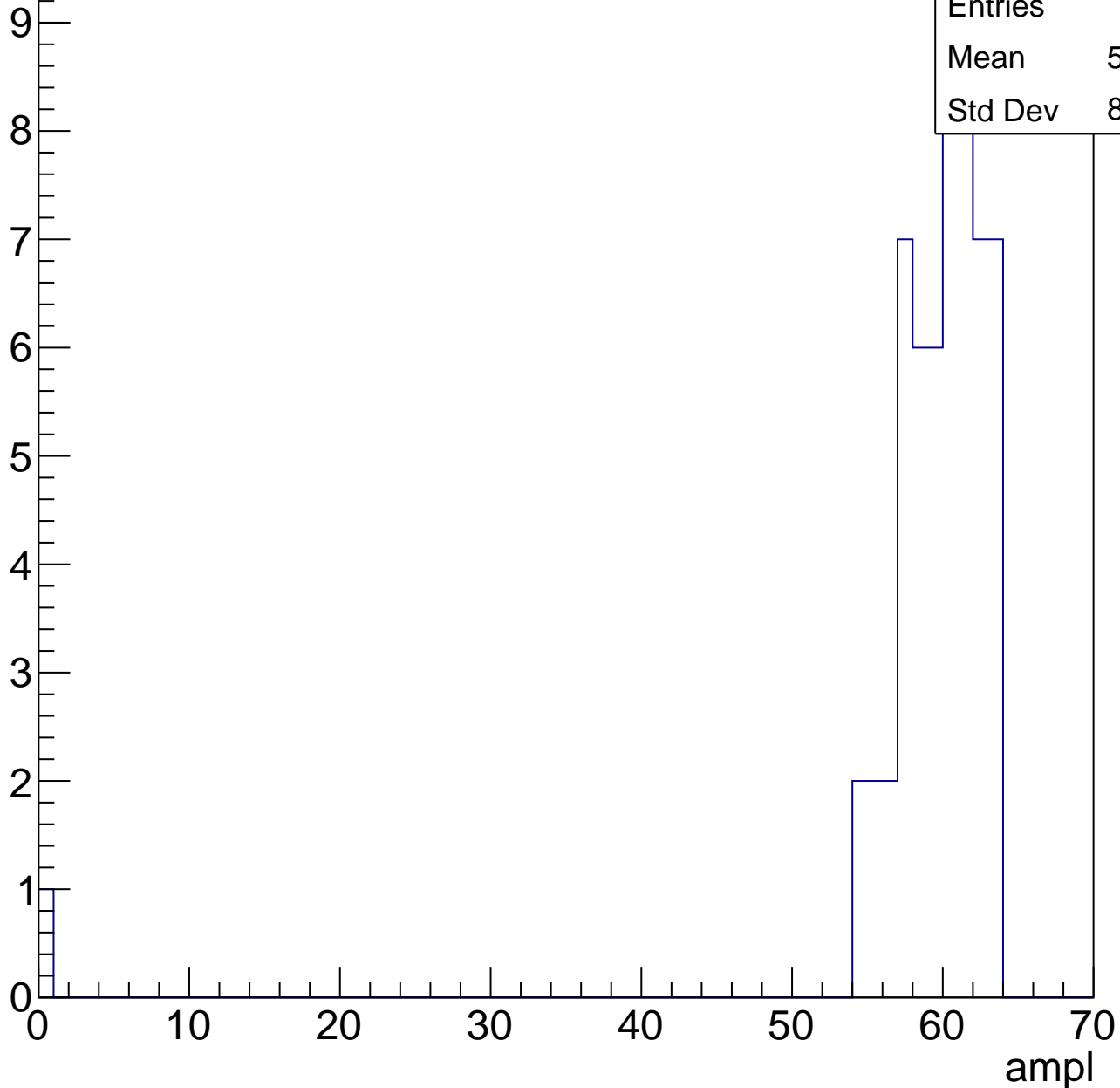
Entry



# B1L101S, U16-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	57
Mean	58.49
Std Dev	8.182

# B1L101S, U16-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch102, adc0

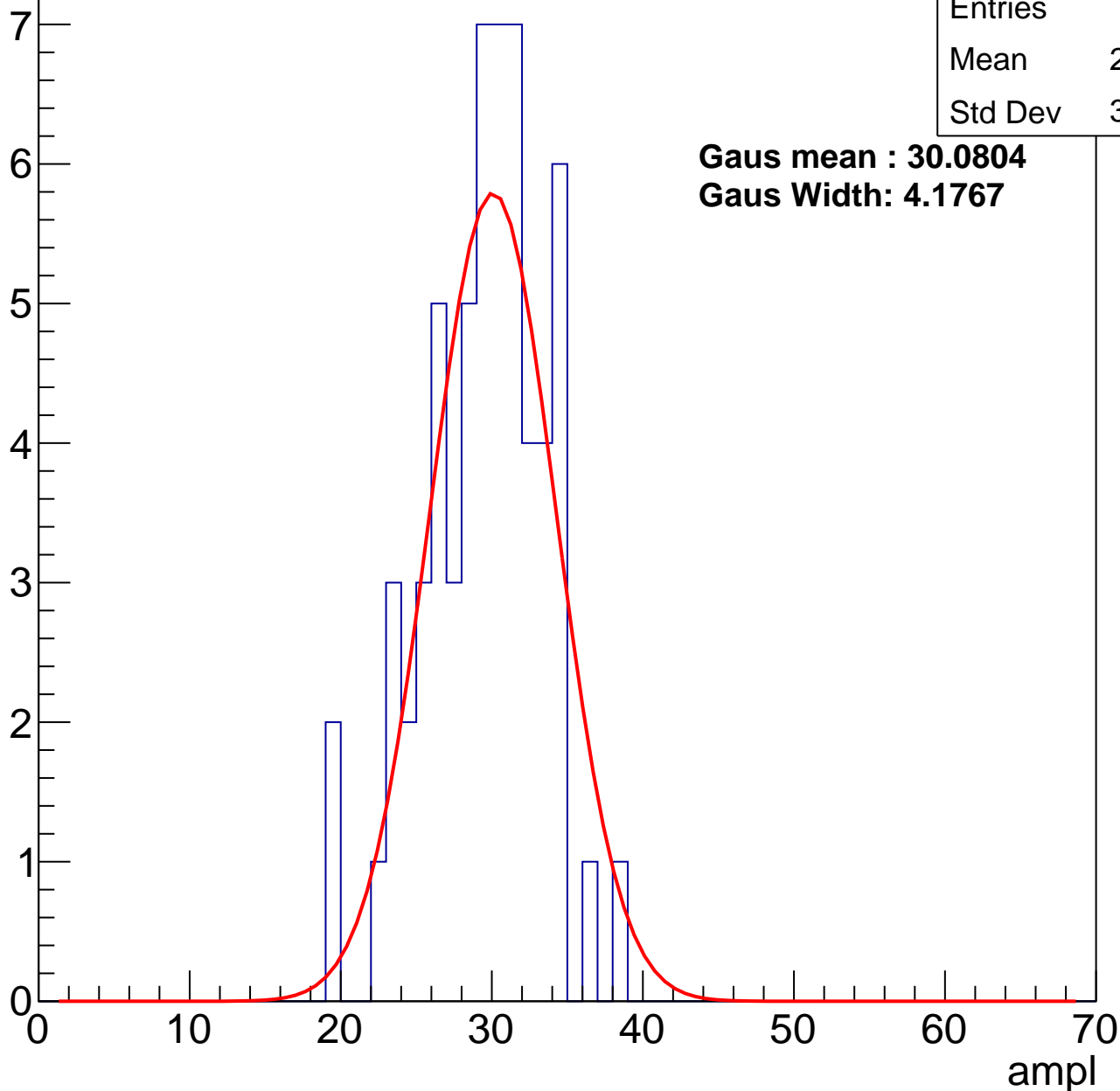
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	29.03
Std Dev	3.909

**Gaus mean : 30.0804**

**Gaus Width: 4.1767**



# B1L101S, U16-ch102, adc1

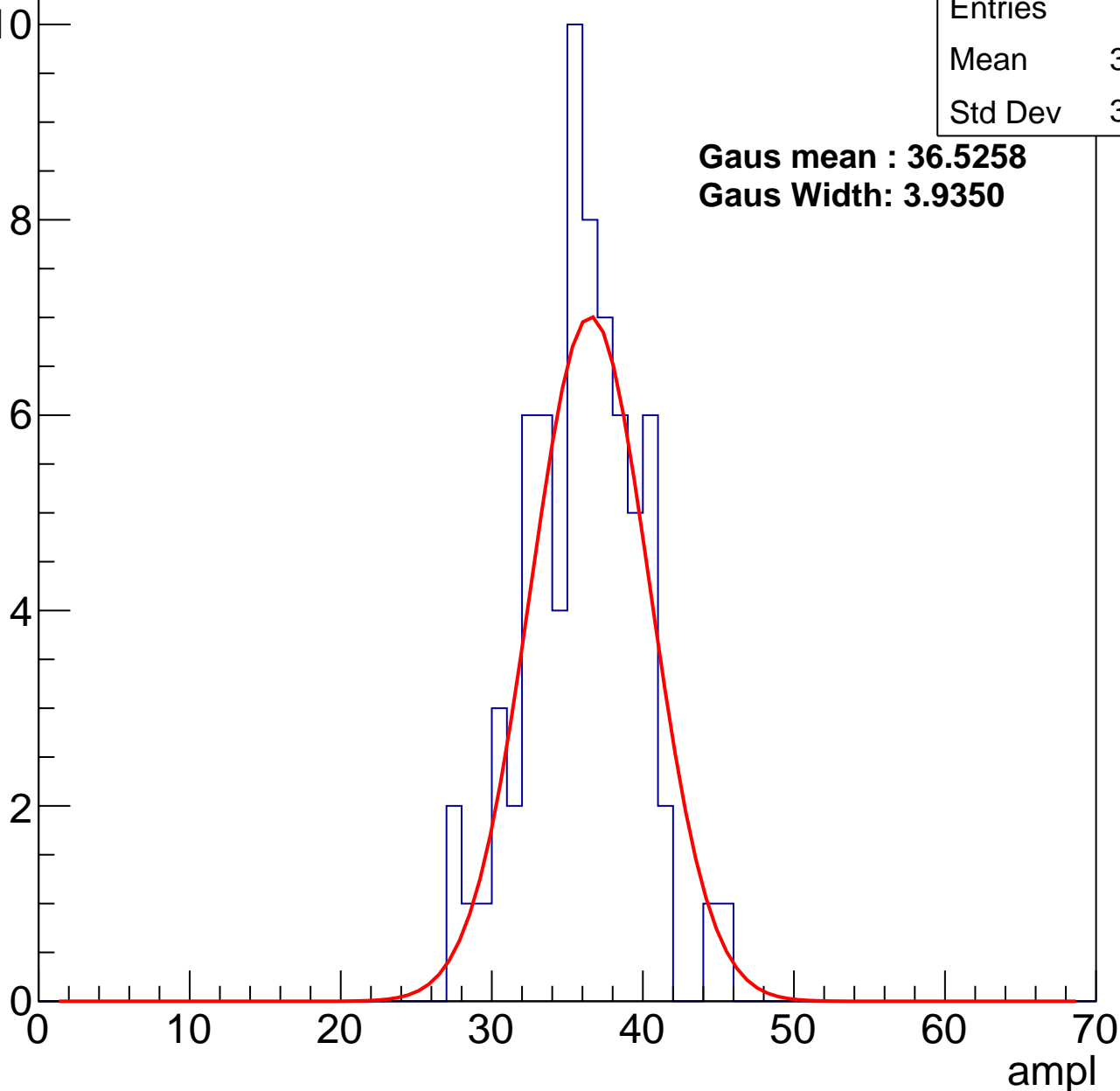
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	35.49
Std Dev	3.673

**Gaus mean : 36.5258**

**Gaus Width: 3.9350**



# B1L101S, U16-ch102, adc2

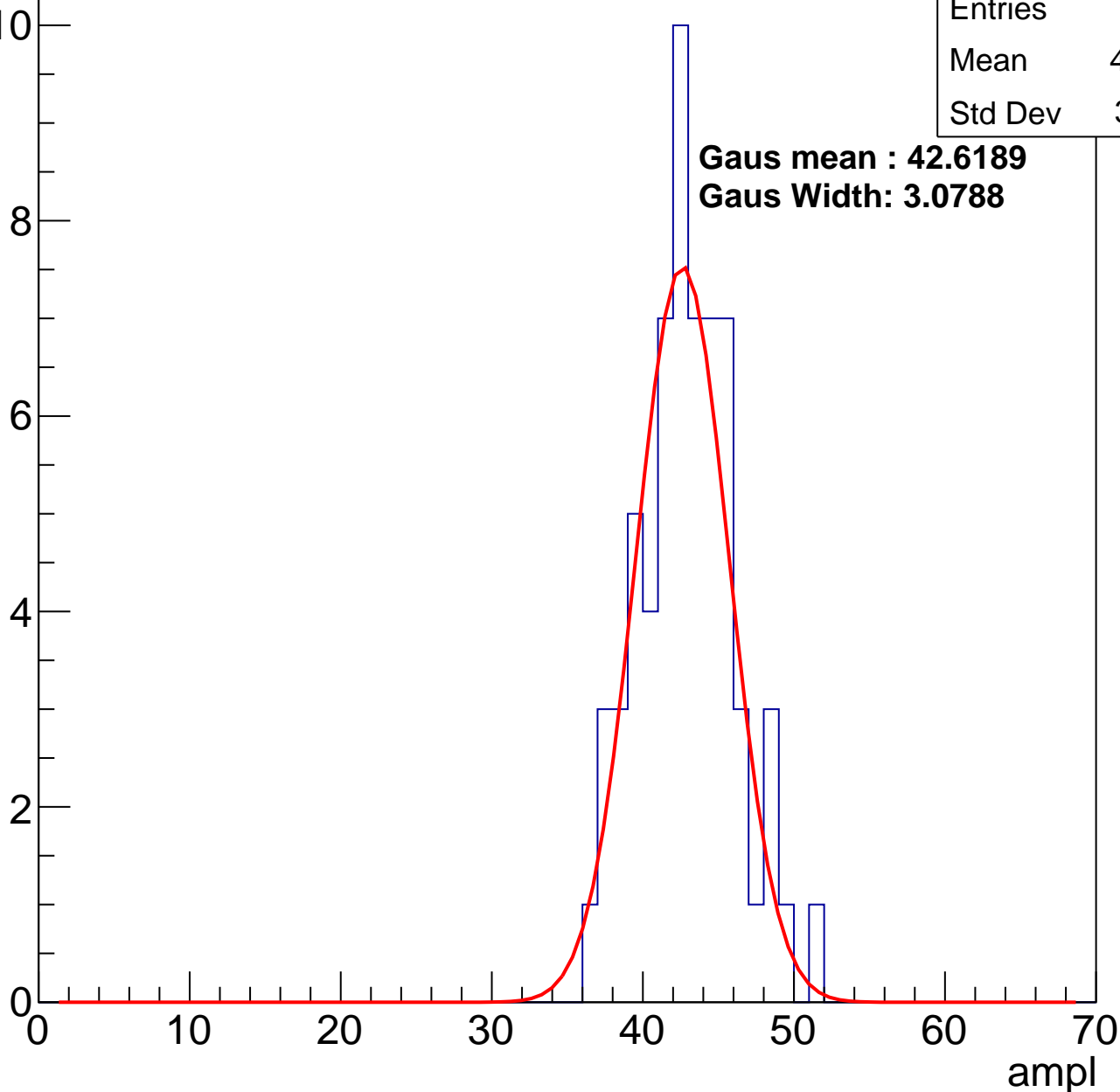
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	42.48
Std Dev	3.141

**Gaus mean : 42.6189**

**Gaus Width: 3.0788**

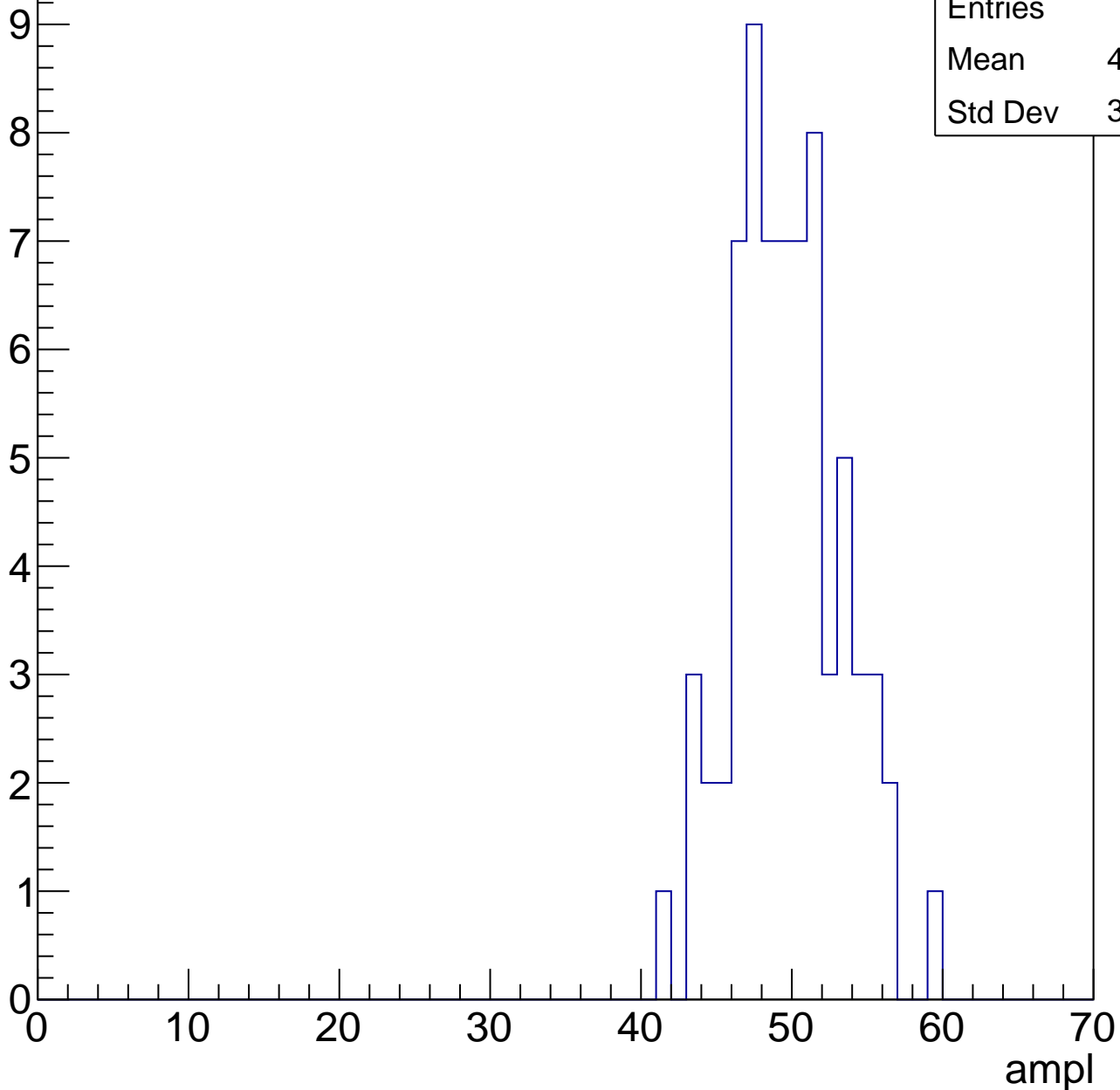


# B1L101S, U16-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	49.27
Std Dev	3.549

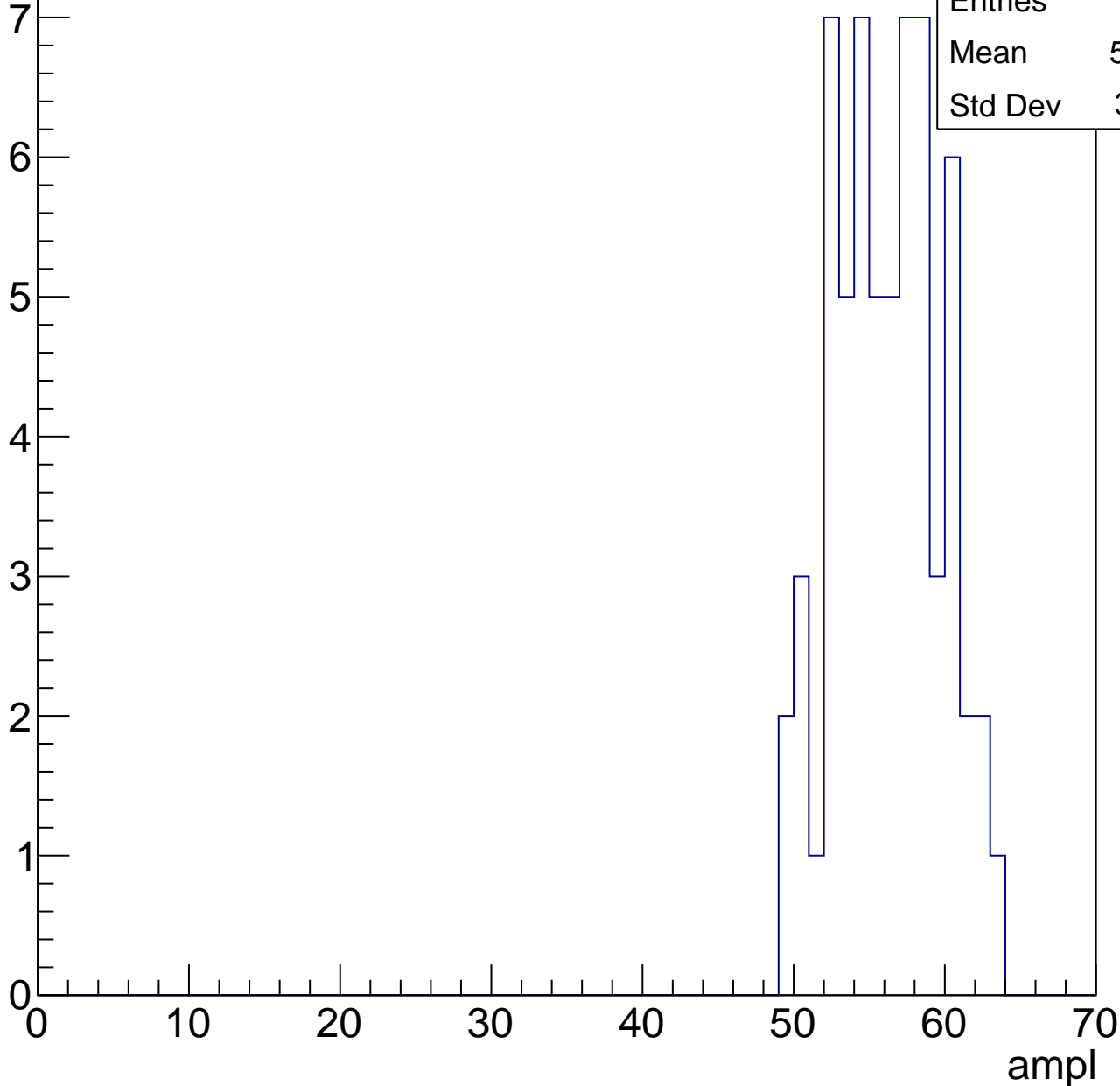


# B1L101S, U16-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	55.75
Std Dev	3.441

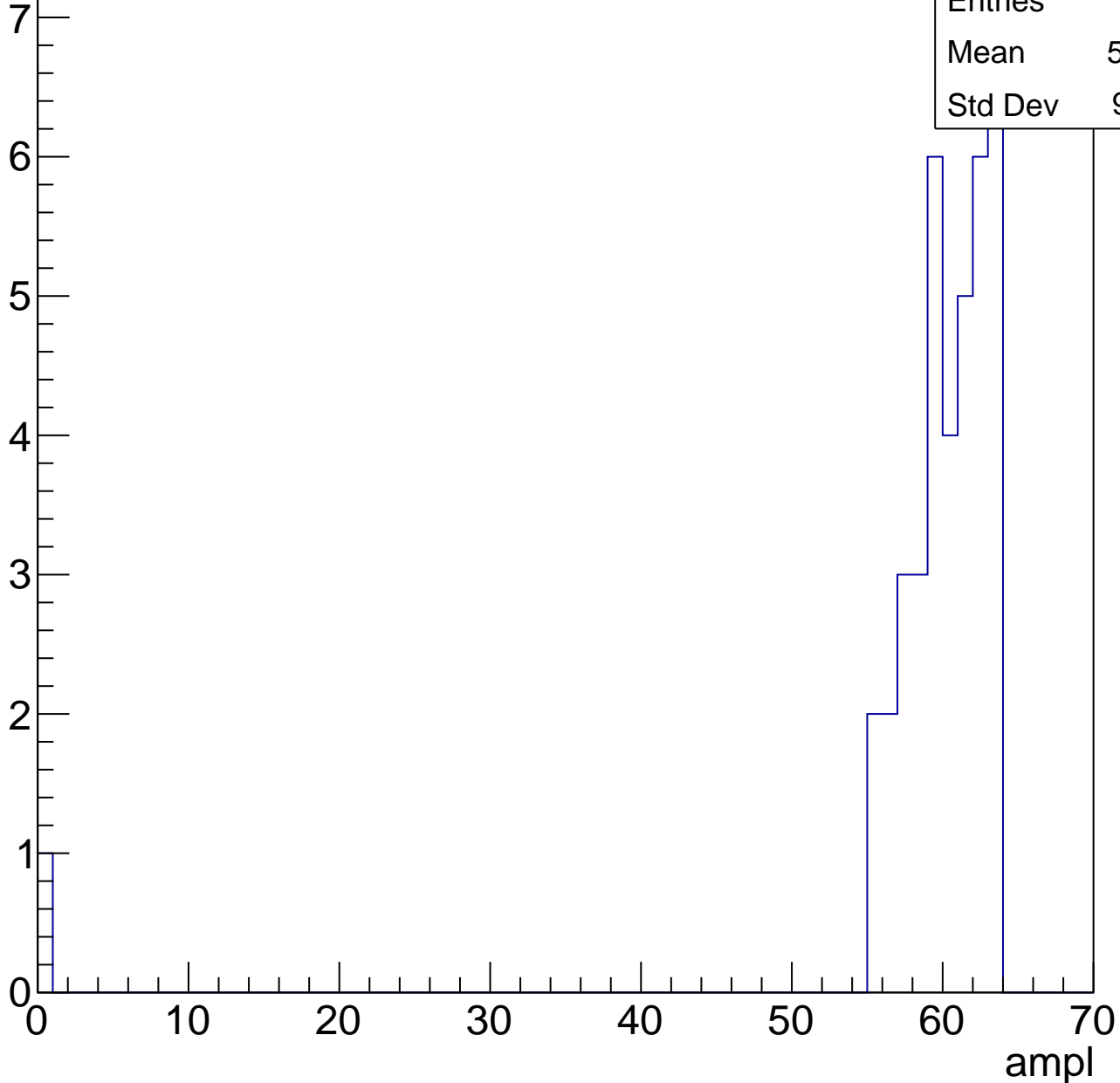


# B1L101S, U16-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

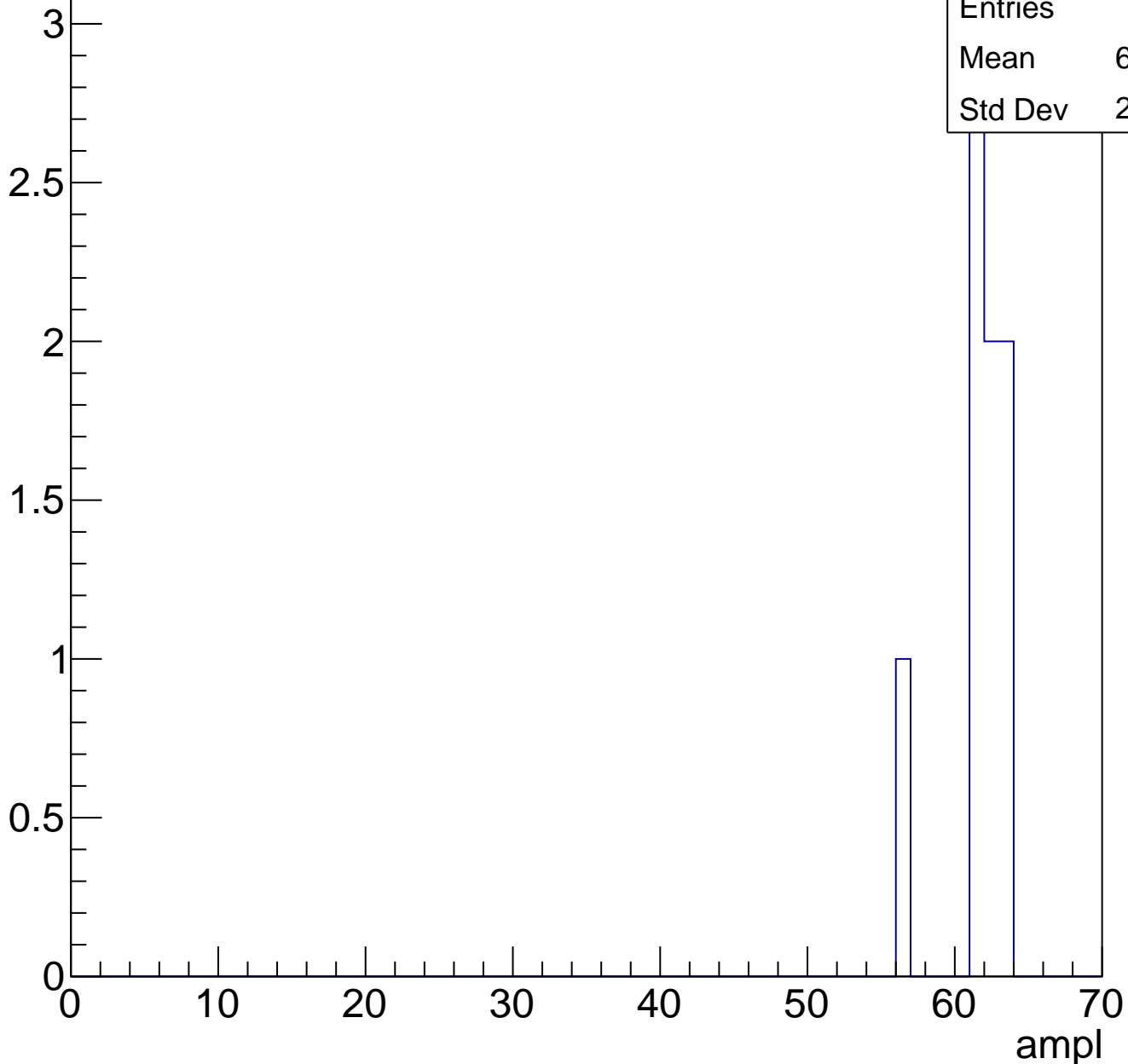
Entries	39
Mean	58.44
Std Dev	9.771



# B1L101S, U16-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch103, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	88
Mean	29.26
Std Dev	3.758

**Gaus mean : 29.9412**

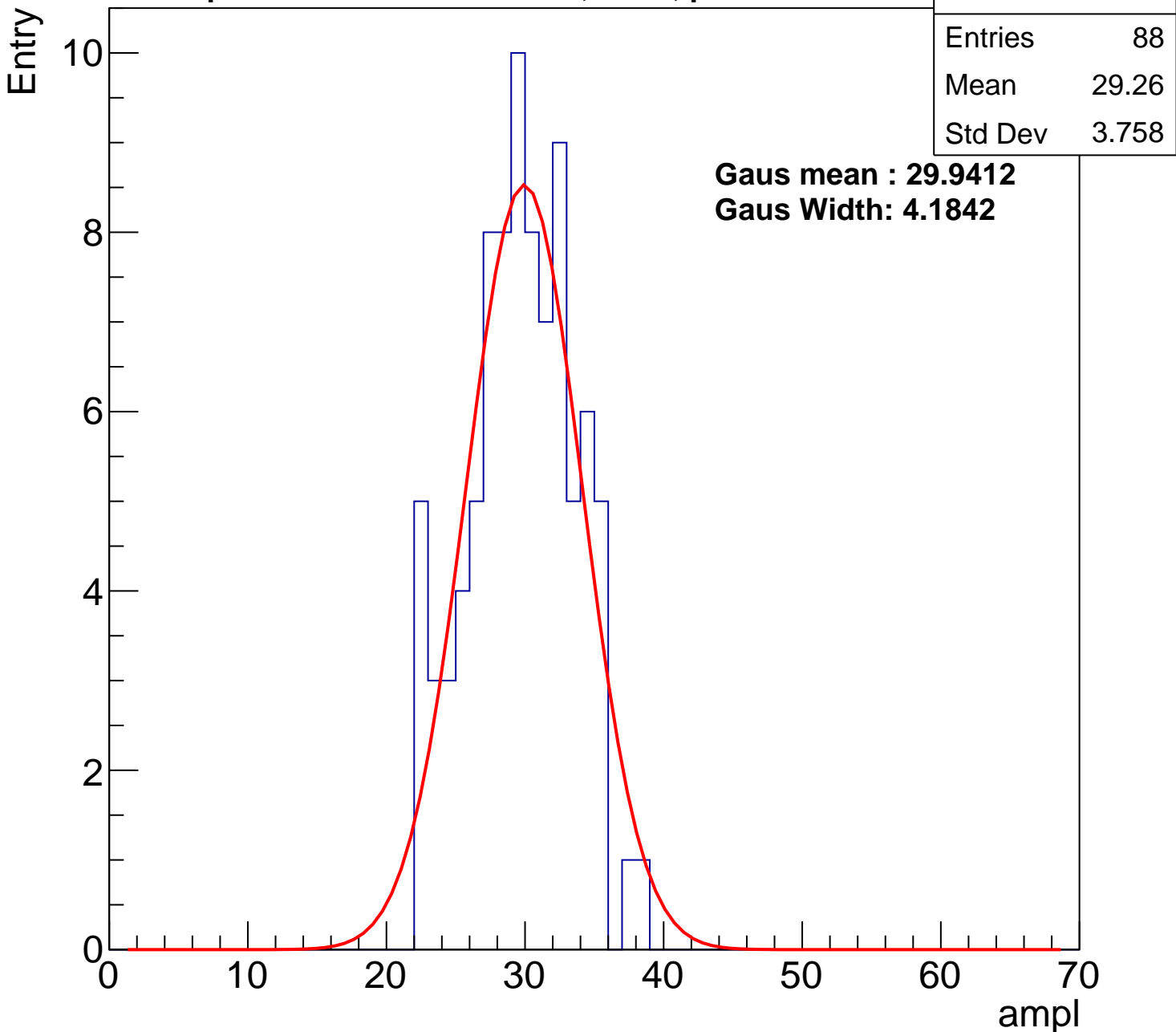
**Gaus Width: 4.1842**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch103, adc1

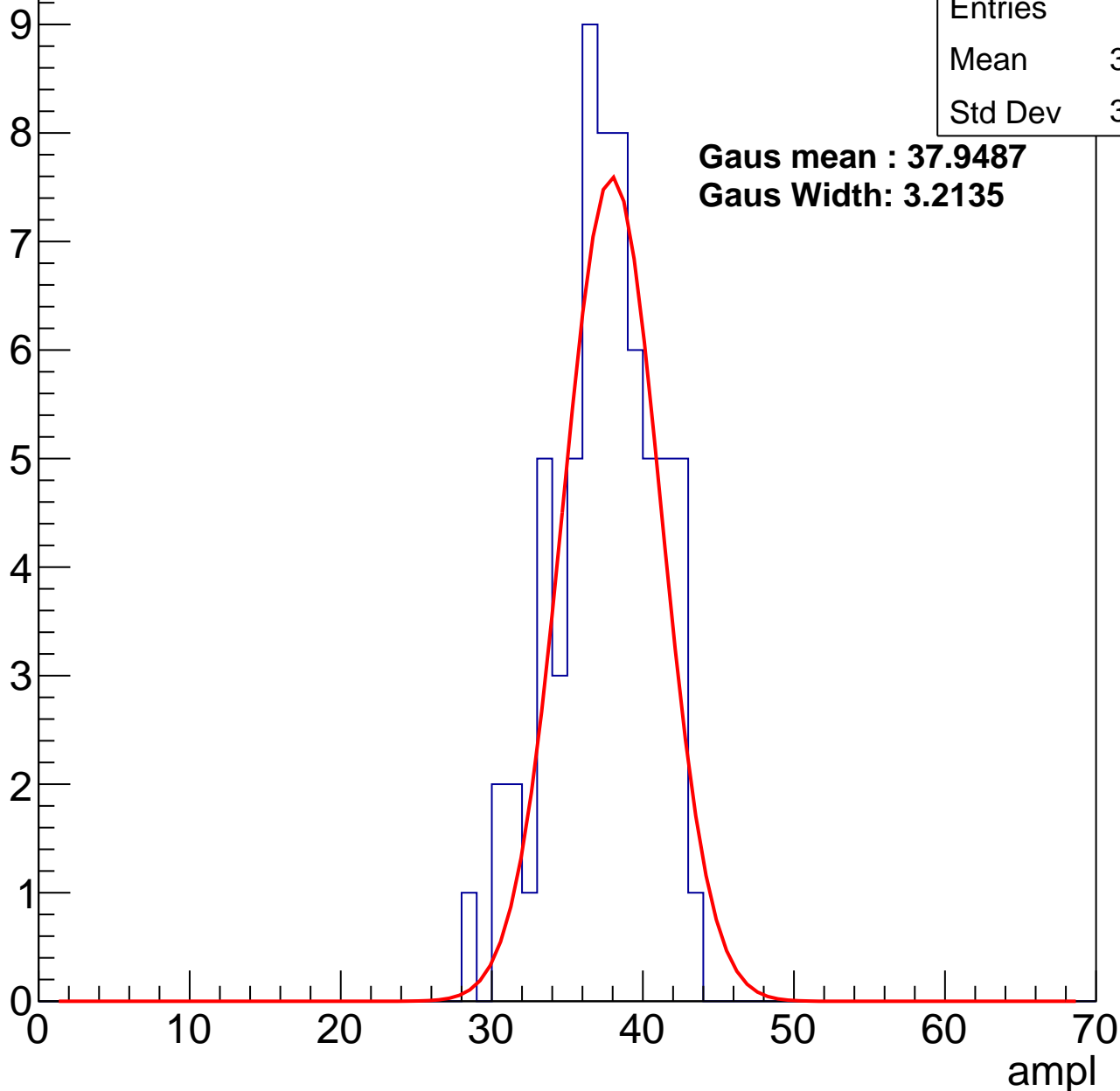
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	36.97
Std Dev	3.326

**Gaus mean : 37.9487**

**Gaus Width: 3.2135**



# B1L101S, U16-ch103, adc2

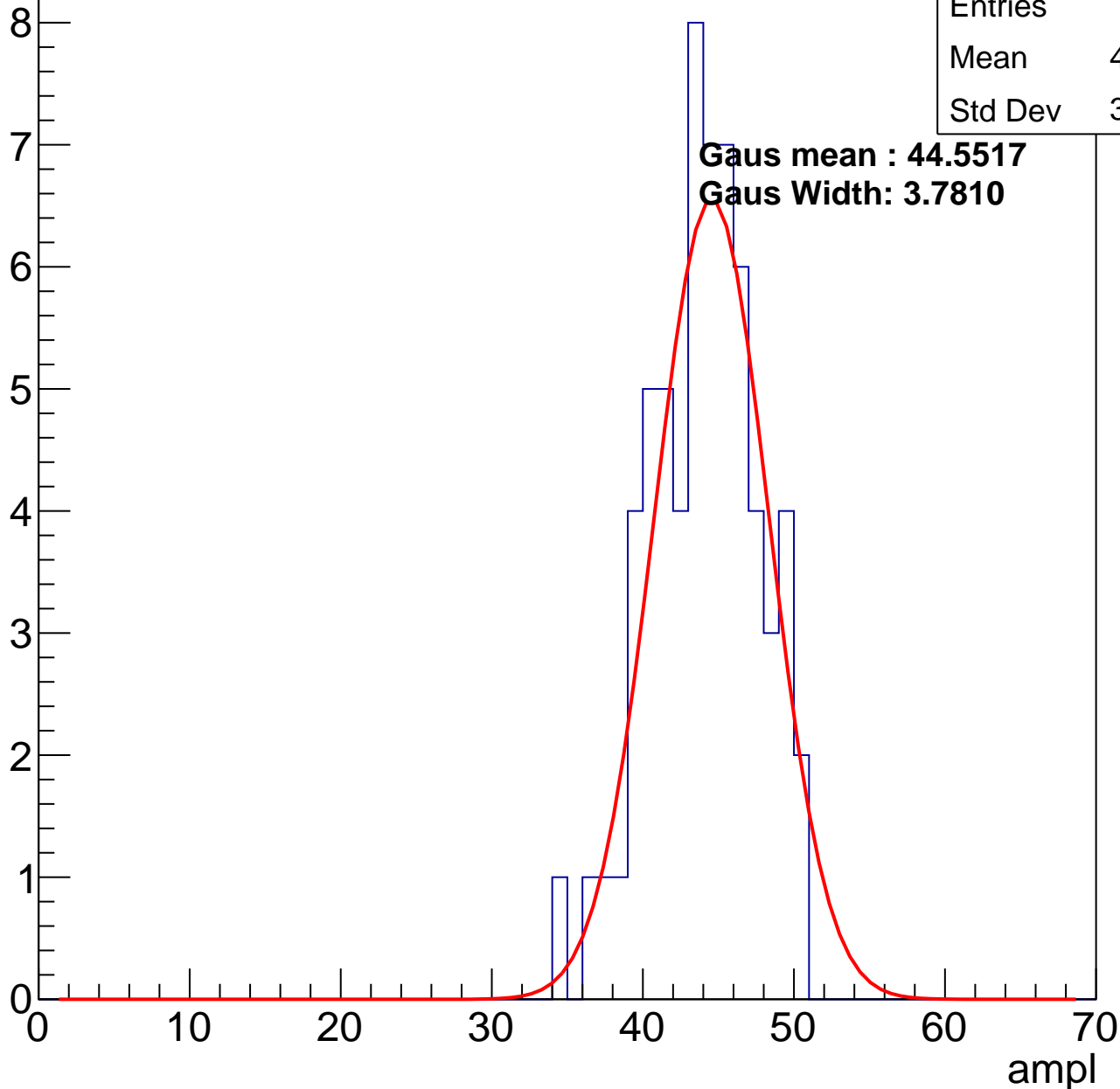
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	43.57
Std Dev	3.504

**Gaus mean : 44.5517**

**Gaus Width: 3.7810**

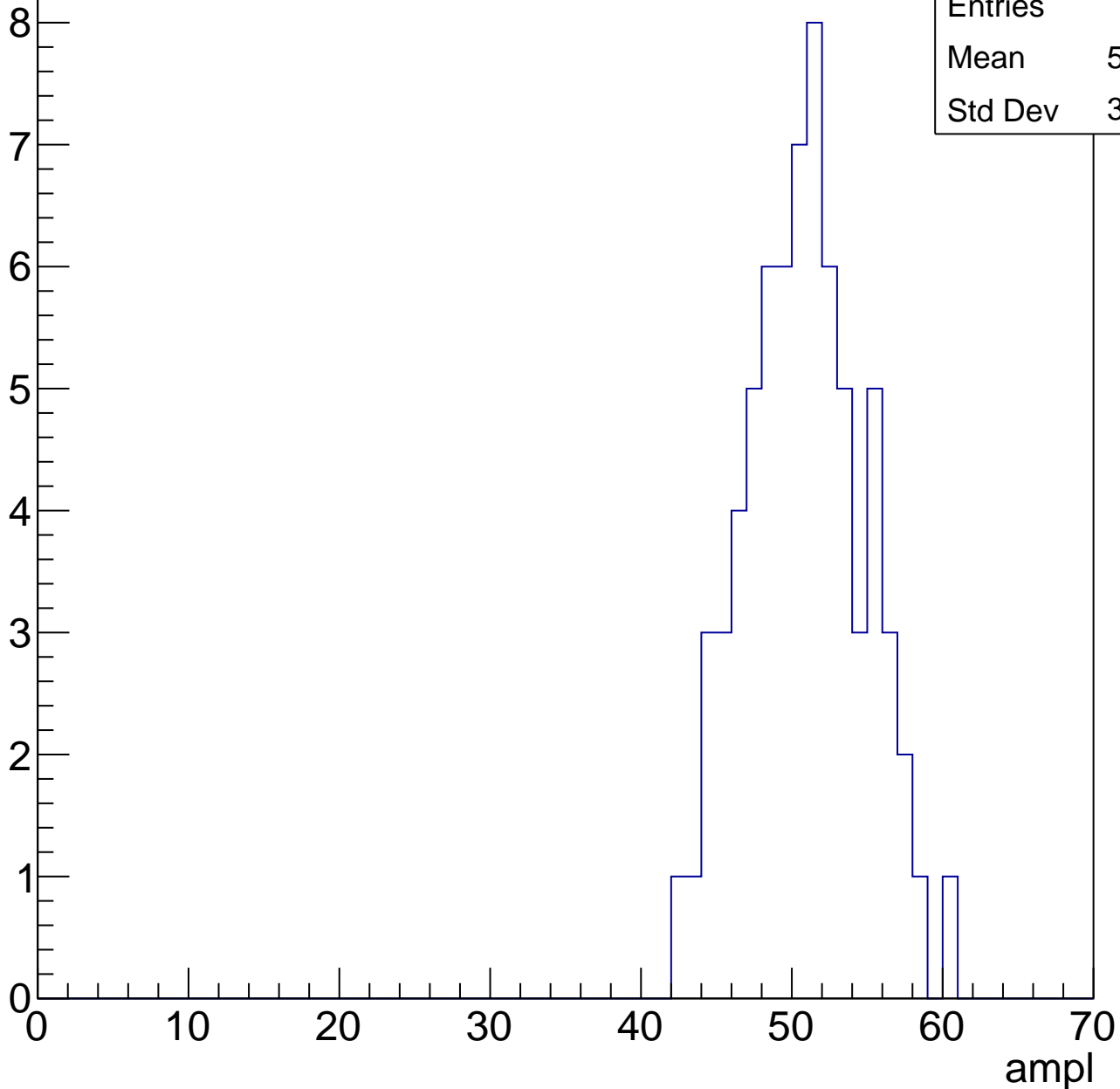


# B1L101S, U16-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	50.36
Std Dev	3.866

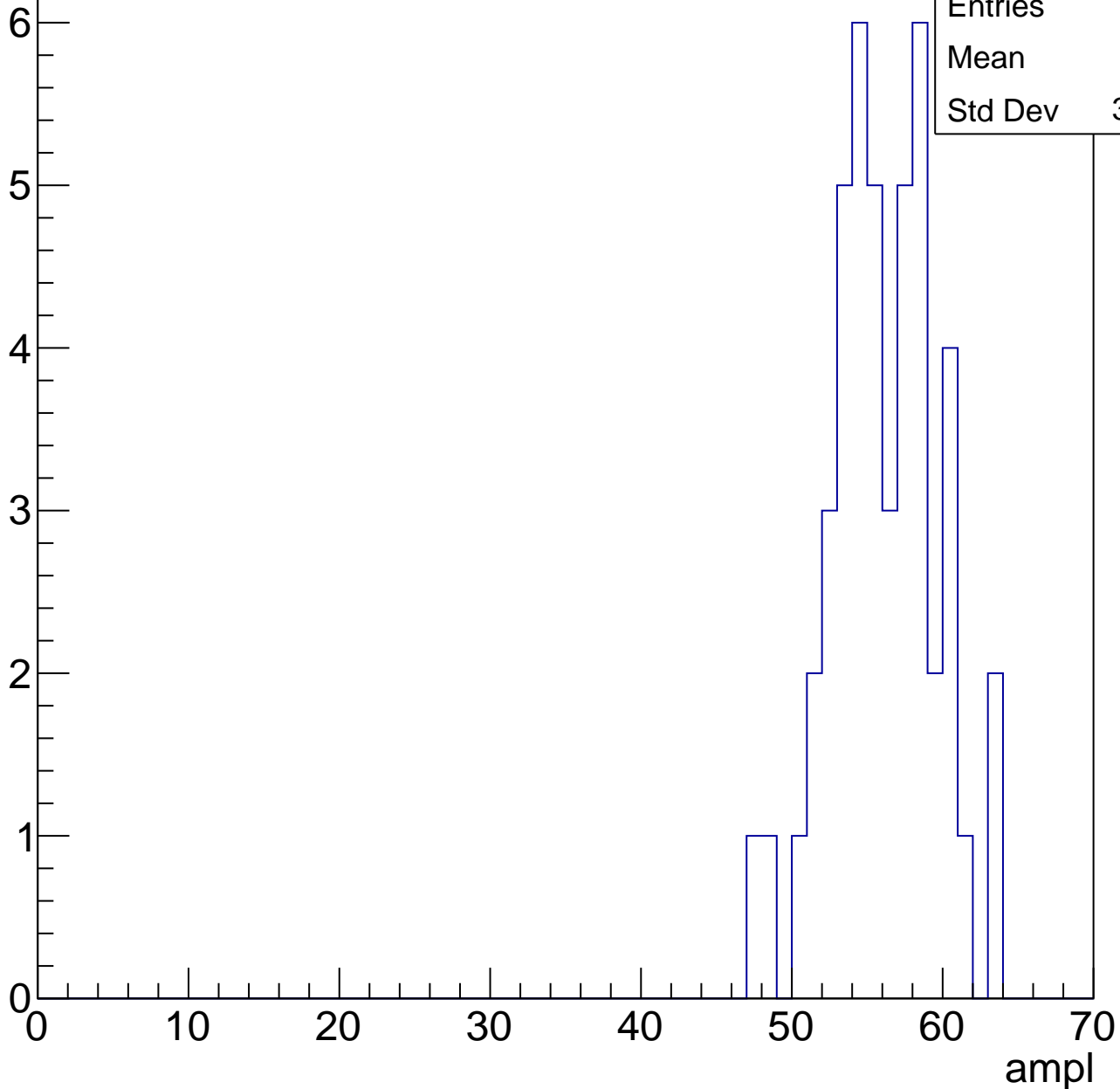


# B1L101S, U16-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

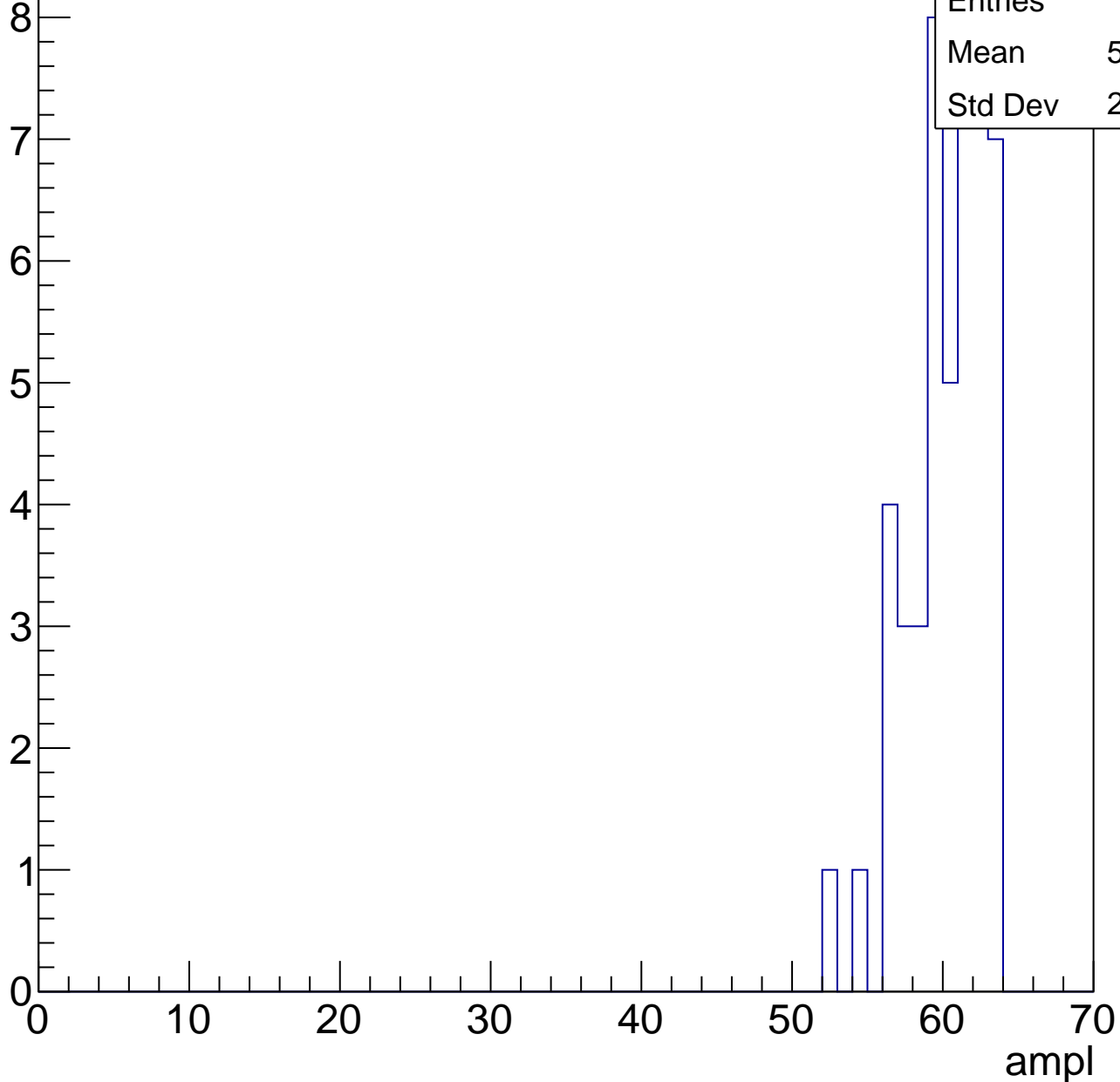
Entries	47
Mean	55.6
Std Dev	3.511



# B1L101S, U16-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

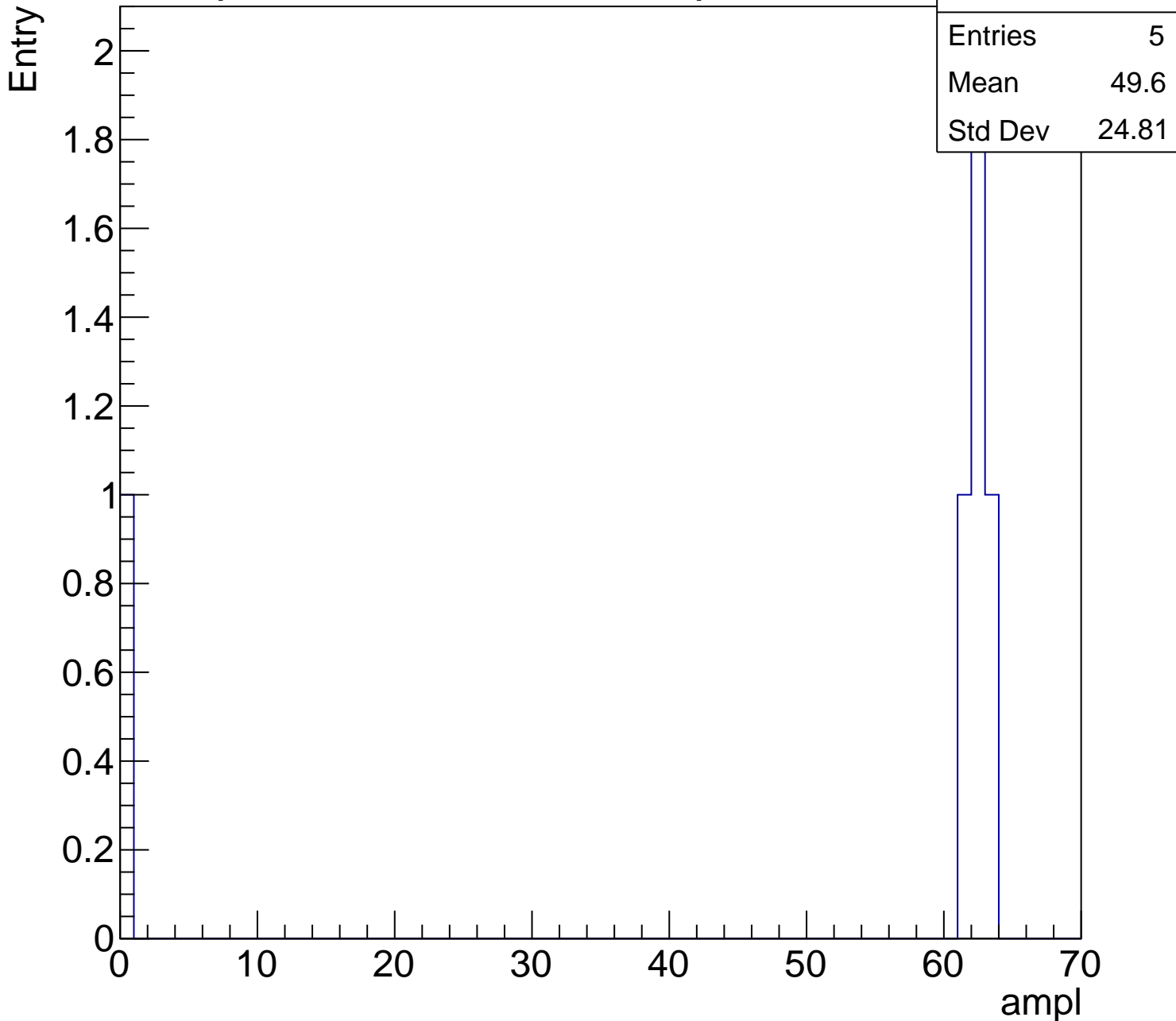
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	49.6
Std Dev	24.81

0 10 20 30 40 50 60 70

ampl





# B1L101S, U16-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U16-ch104, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	77
Mean	29.7
Std Dev	5.215

**Gaus mean : 31.0010**

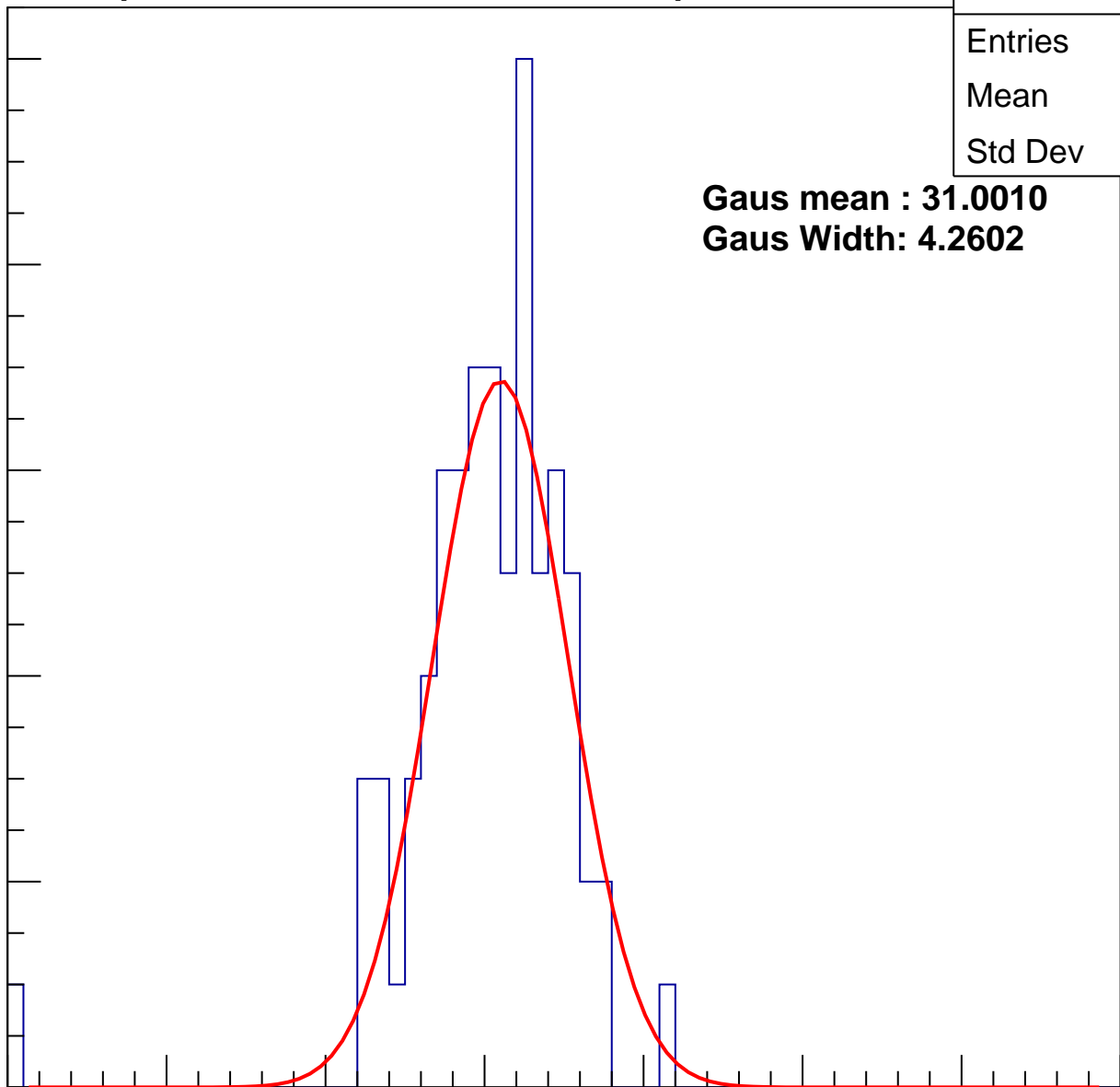
**Gaus Width: 4.2602**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch104, adc1

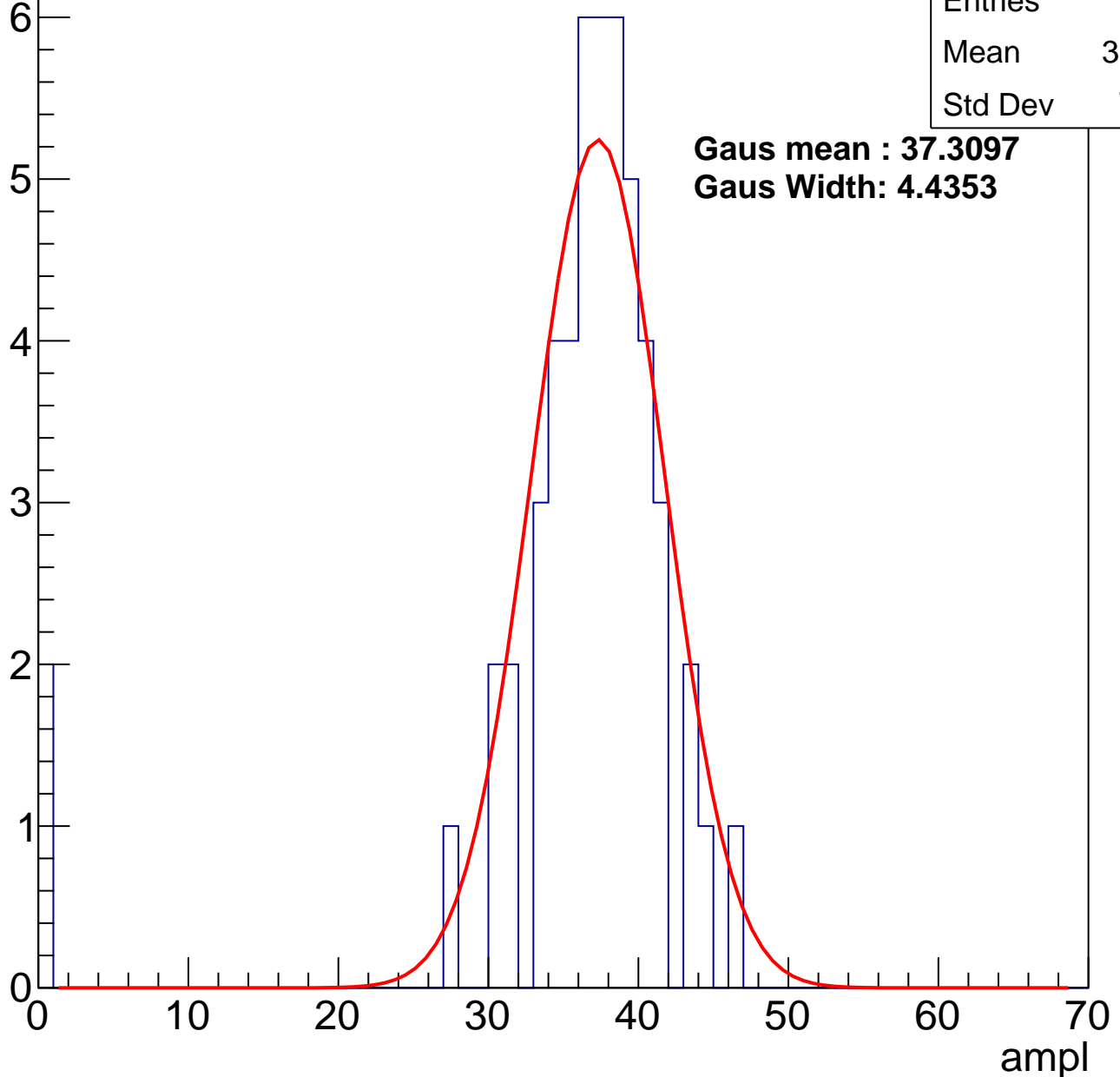
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	35.46
Std Dev	7.97

**Gaus mean : 37.3097**

**Gaus Width: 4.4353**



# B1L101S, U16-ch104, adc2

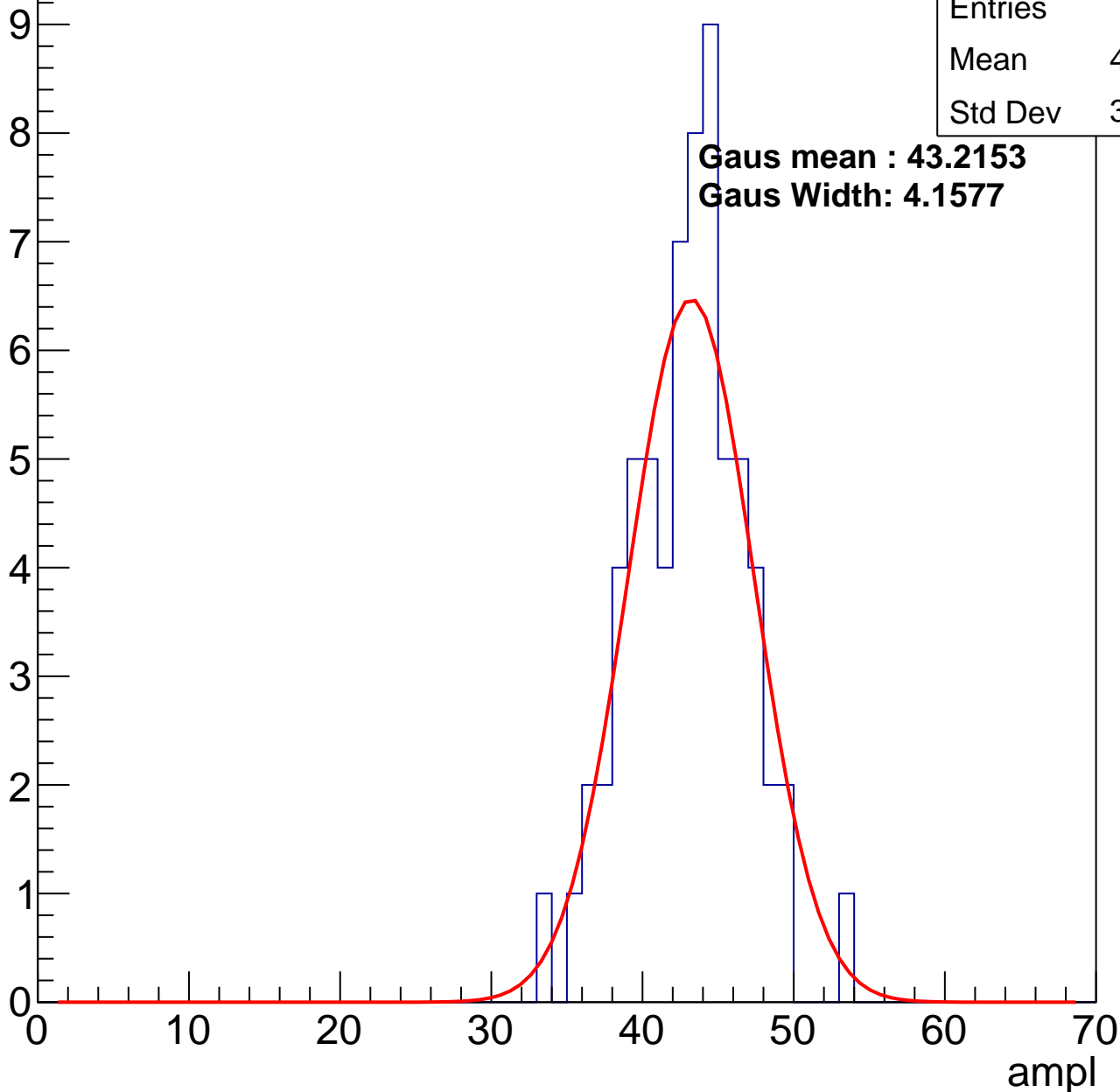
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	42.52
Std Dev	3.719

**Gaus mean : 43.2153**

**Gaus Width: 4.1577**

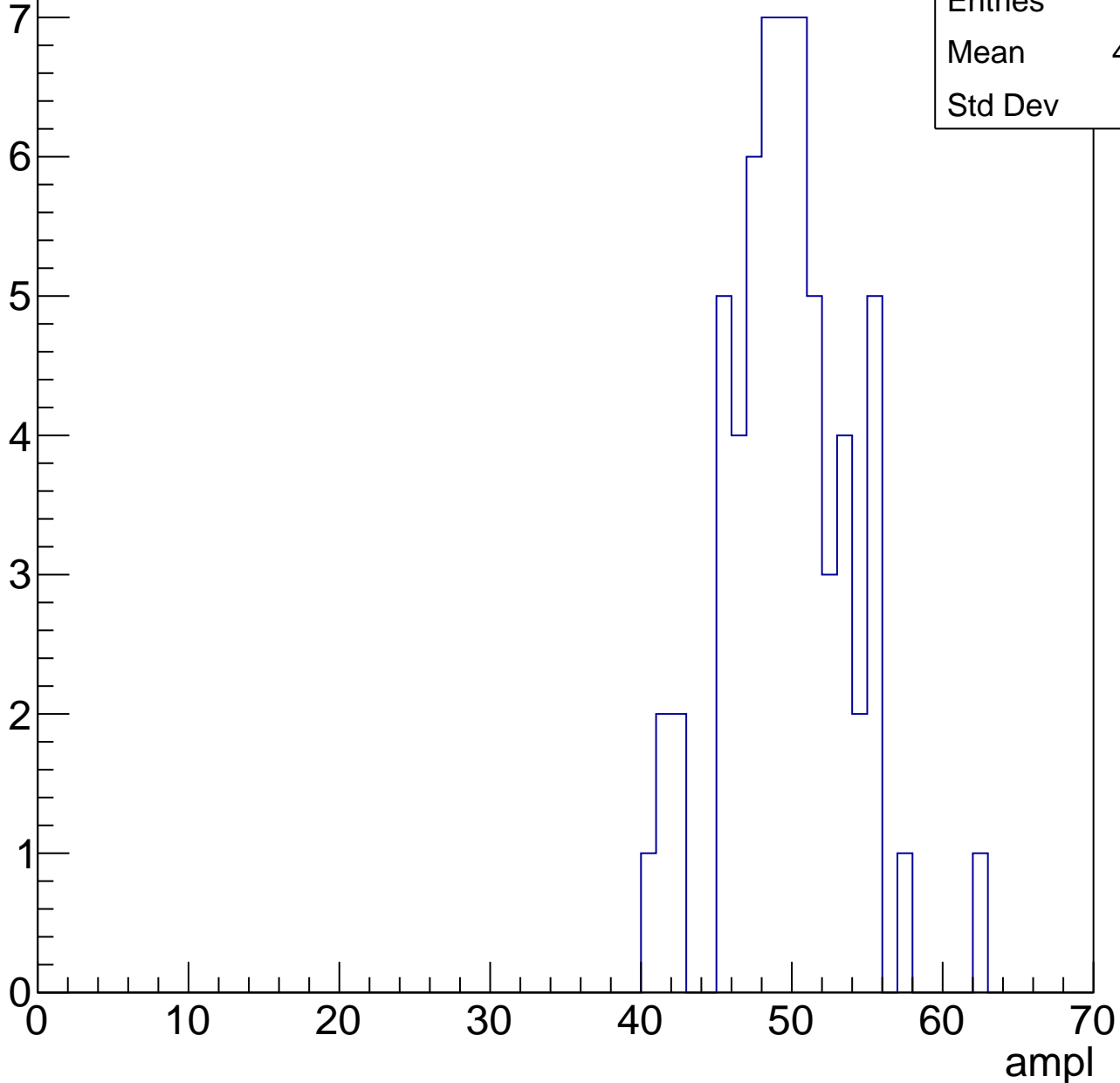


# B1L101S, U16-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	49.21
Std Dev	4.08

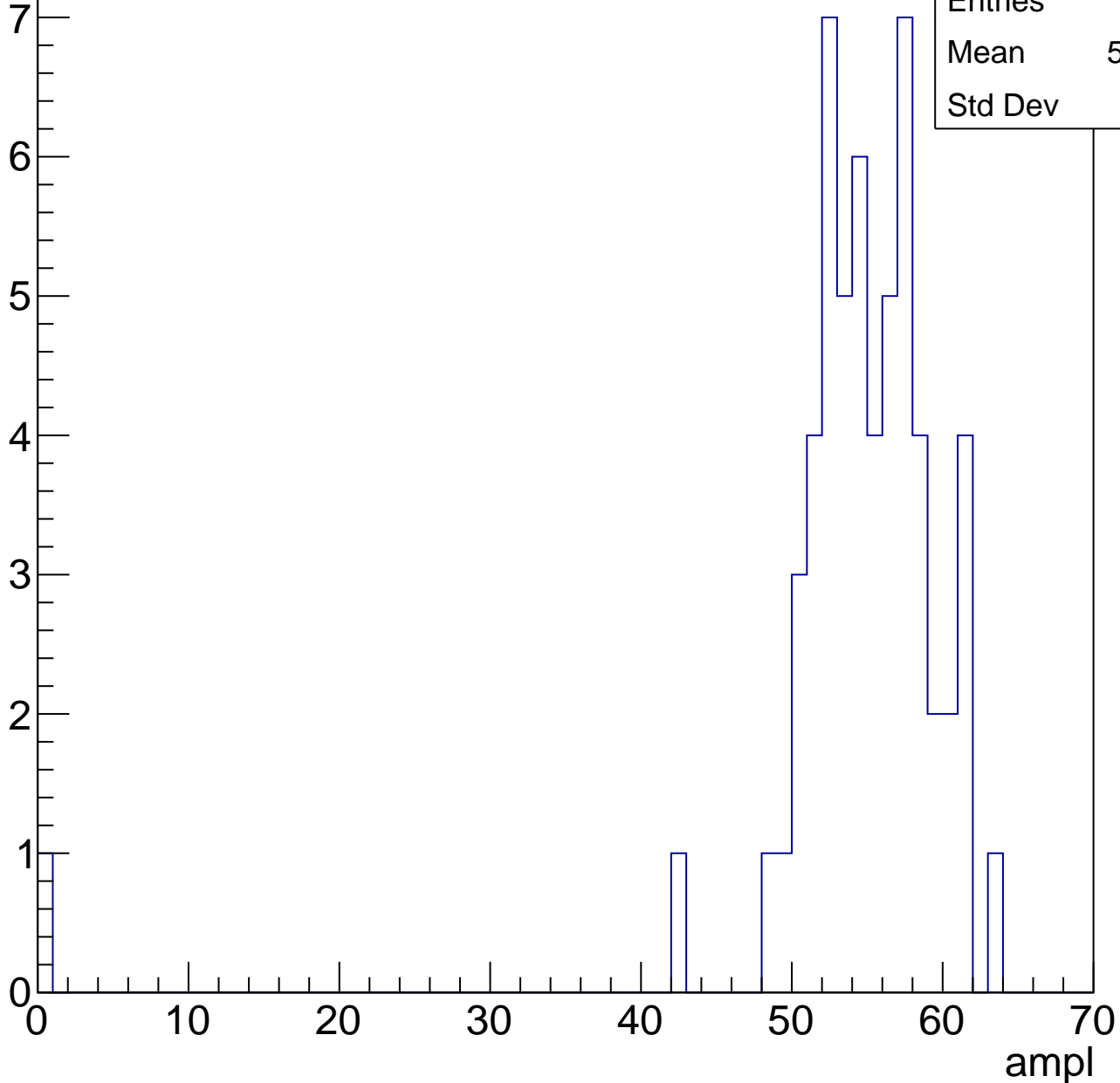


# B1L101S, U16-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

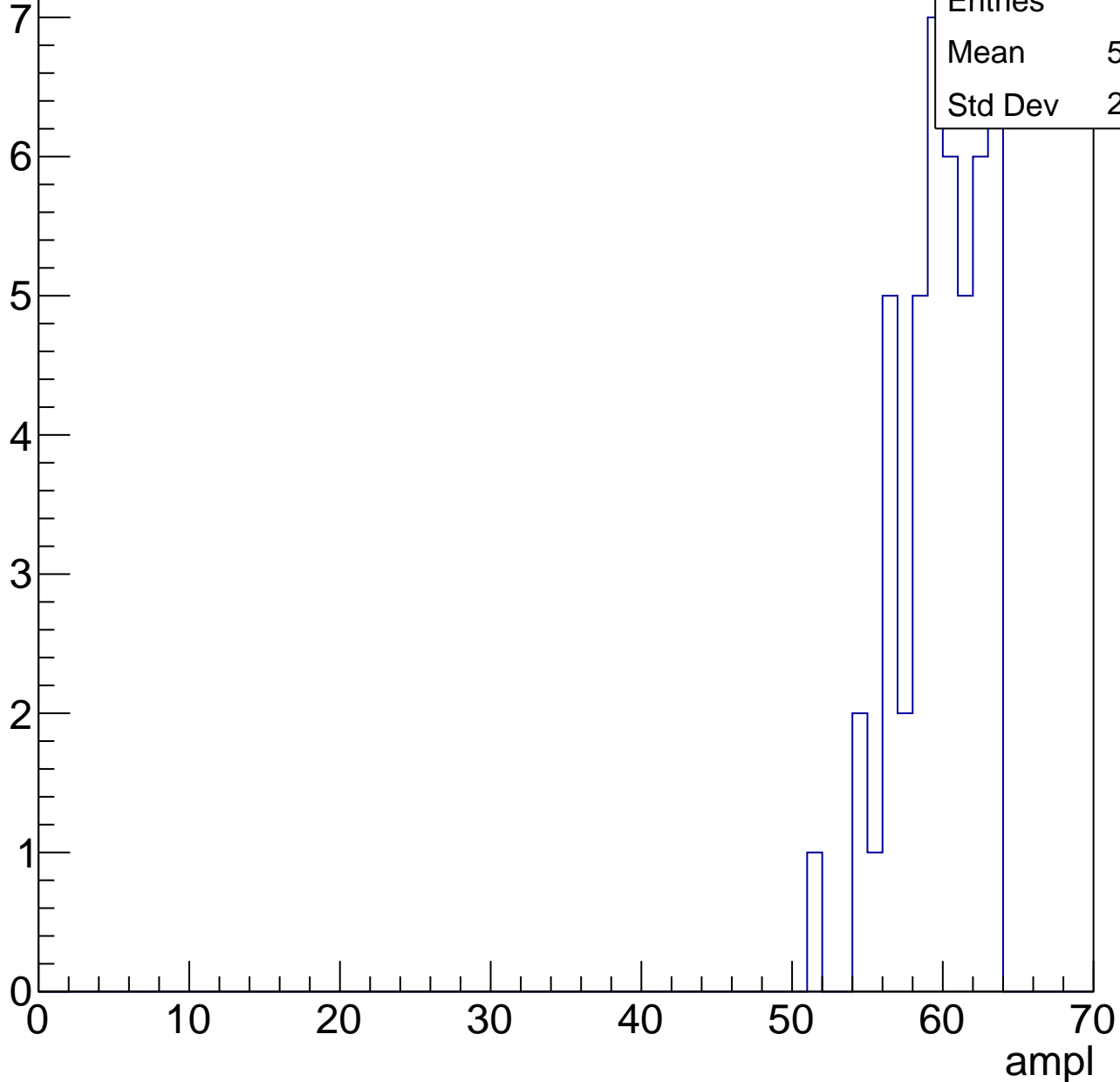
Entries	58
Mean	53.83
Std Dev	8.08



# B1L101S, U16-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

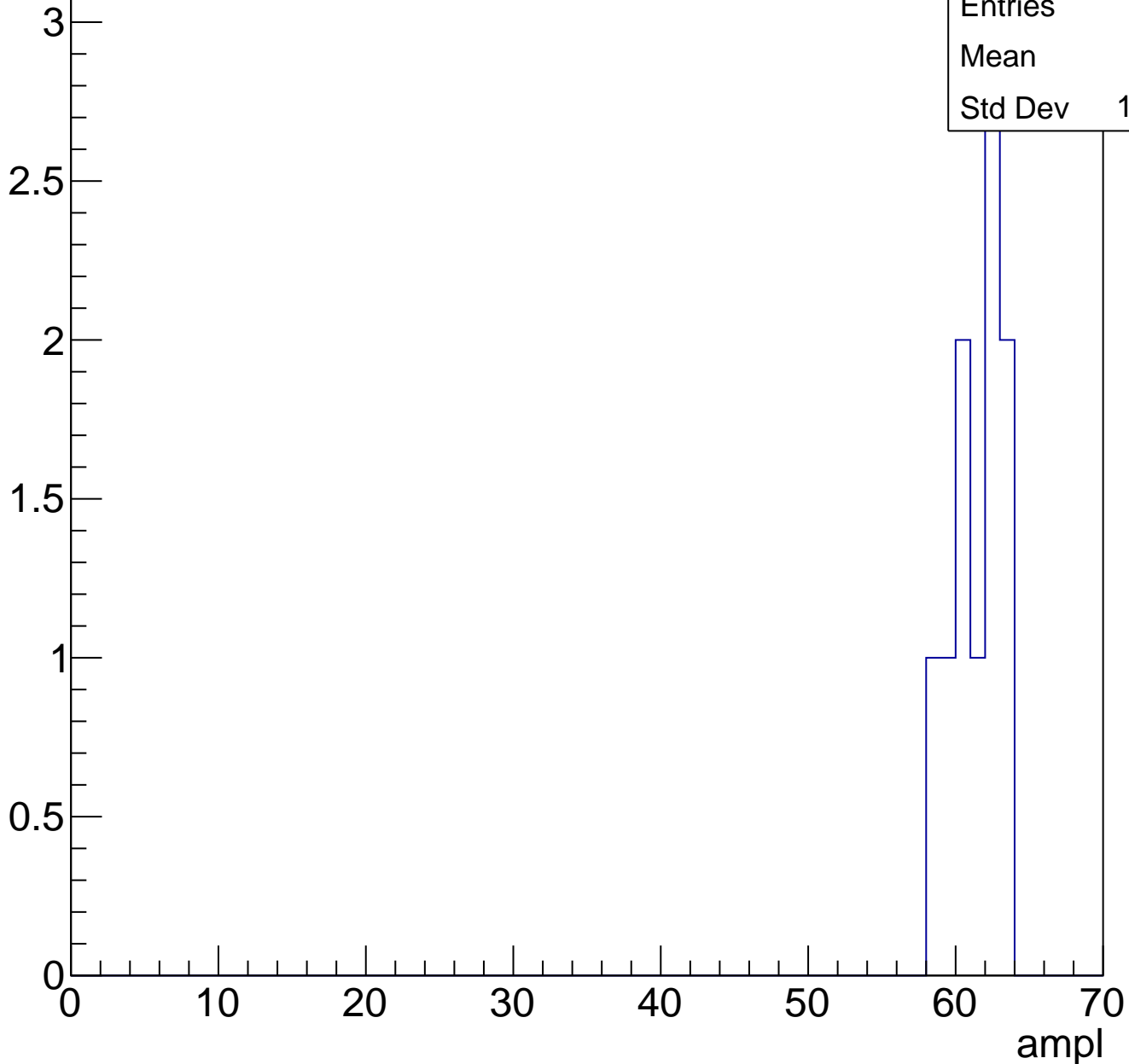
Entry



# B1L101S, U16-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U16-ch105, adc0

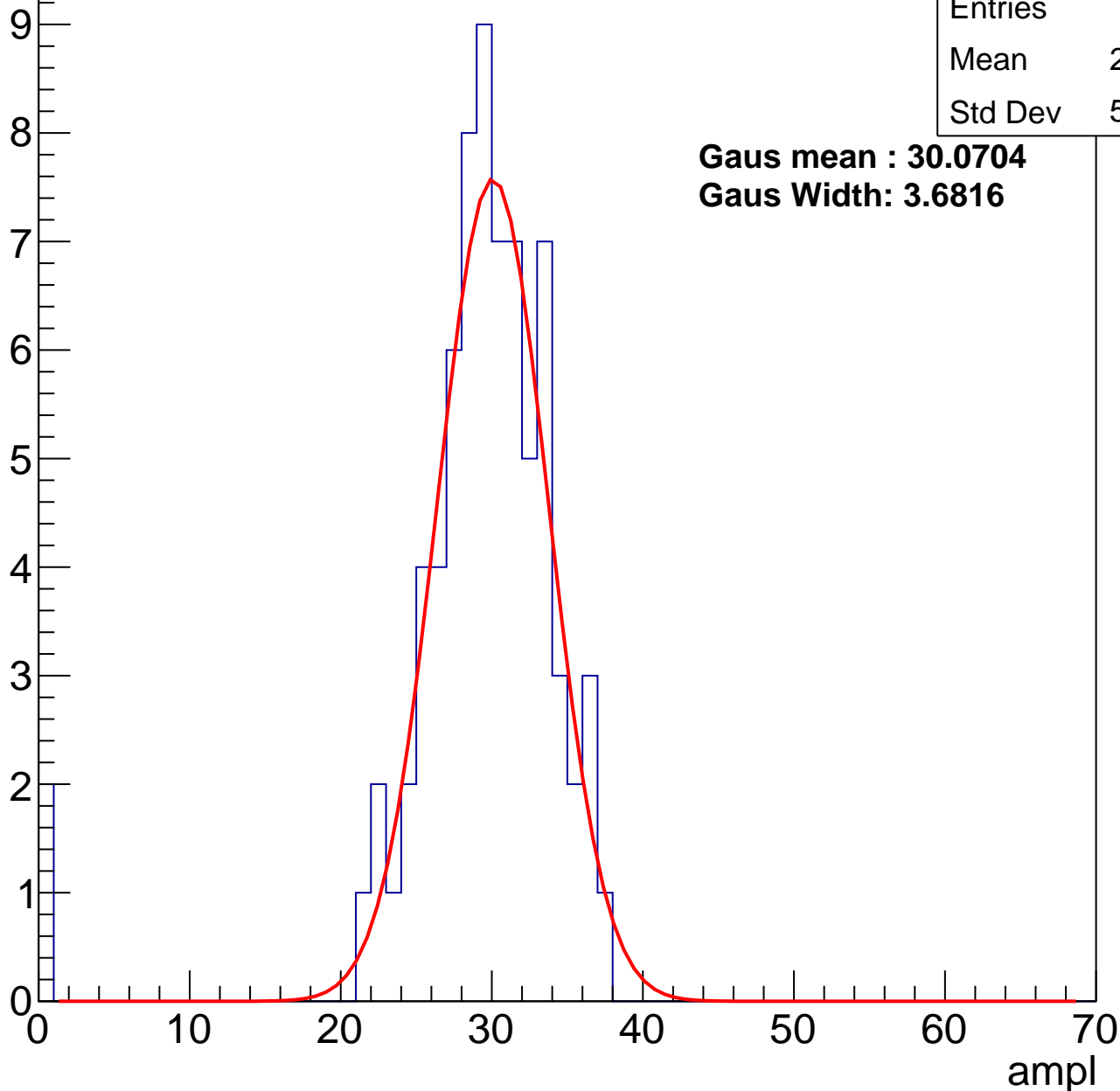
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	28.68
Std Dev	5.932

**Gaus mean : 30.0704**

**Gaus Width: 3.6816**



# B1L101S, U16-ch105, adc1

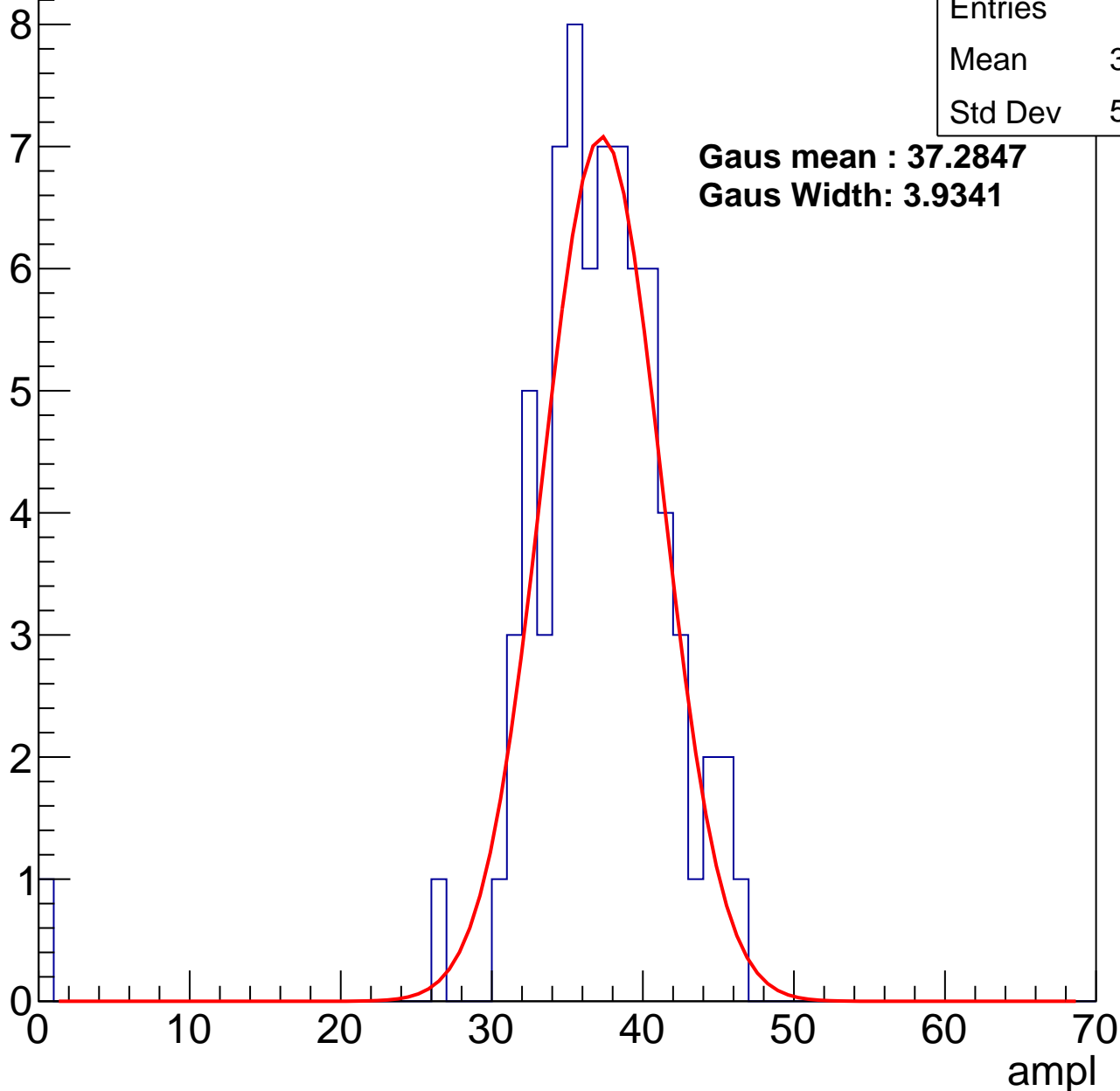
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	36.46
Std Dev	5.773

**Gaus mean : 37.2847**

**Gaus Width: 3.9341**



# B1L101S, U16-ch105, adc2

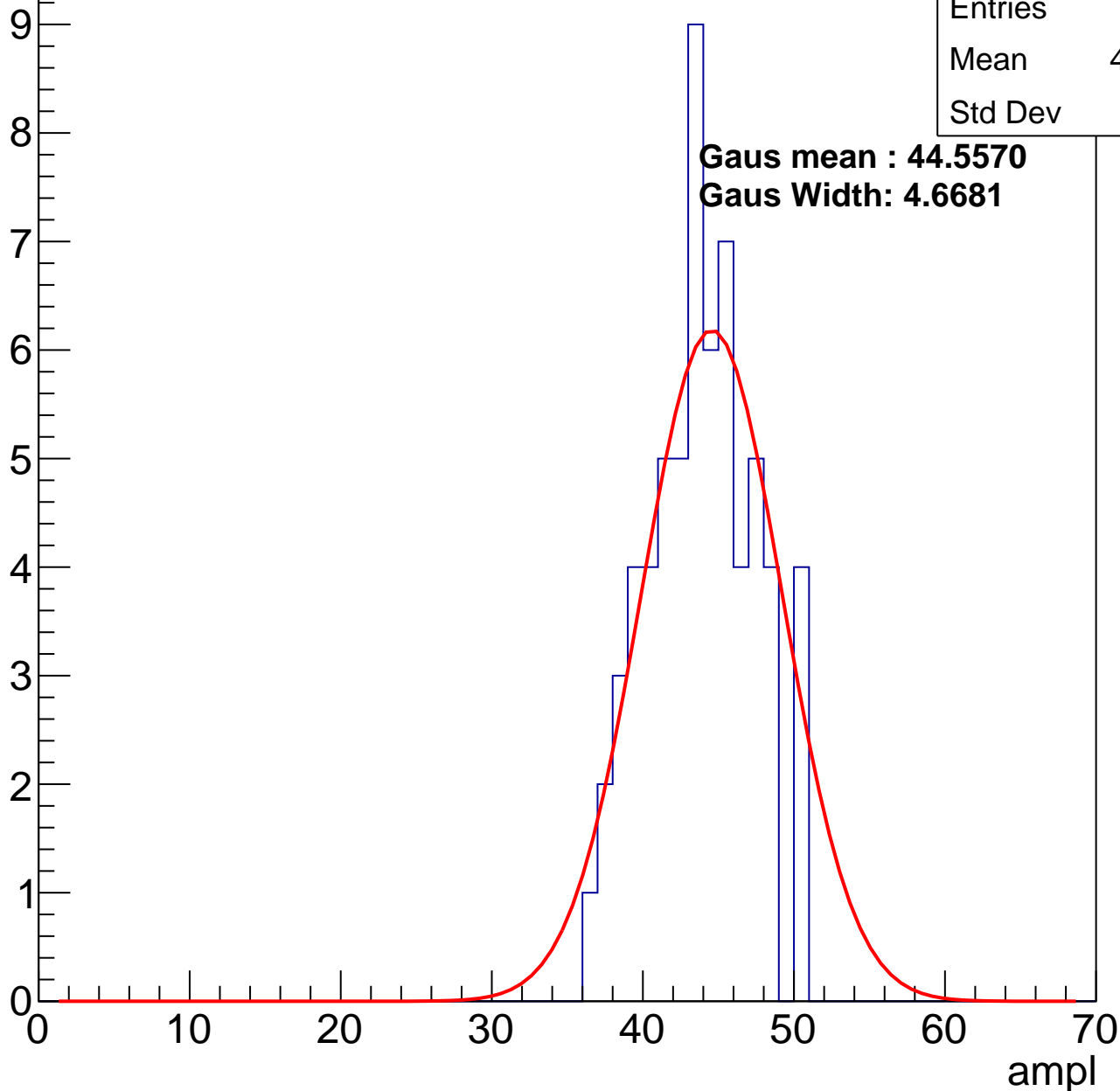
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	43.37
Std Dev	3.47

**Gaus mean : 44.5570**

**Gaus Width: 4.6681**



# B1L101S, U16-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

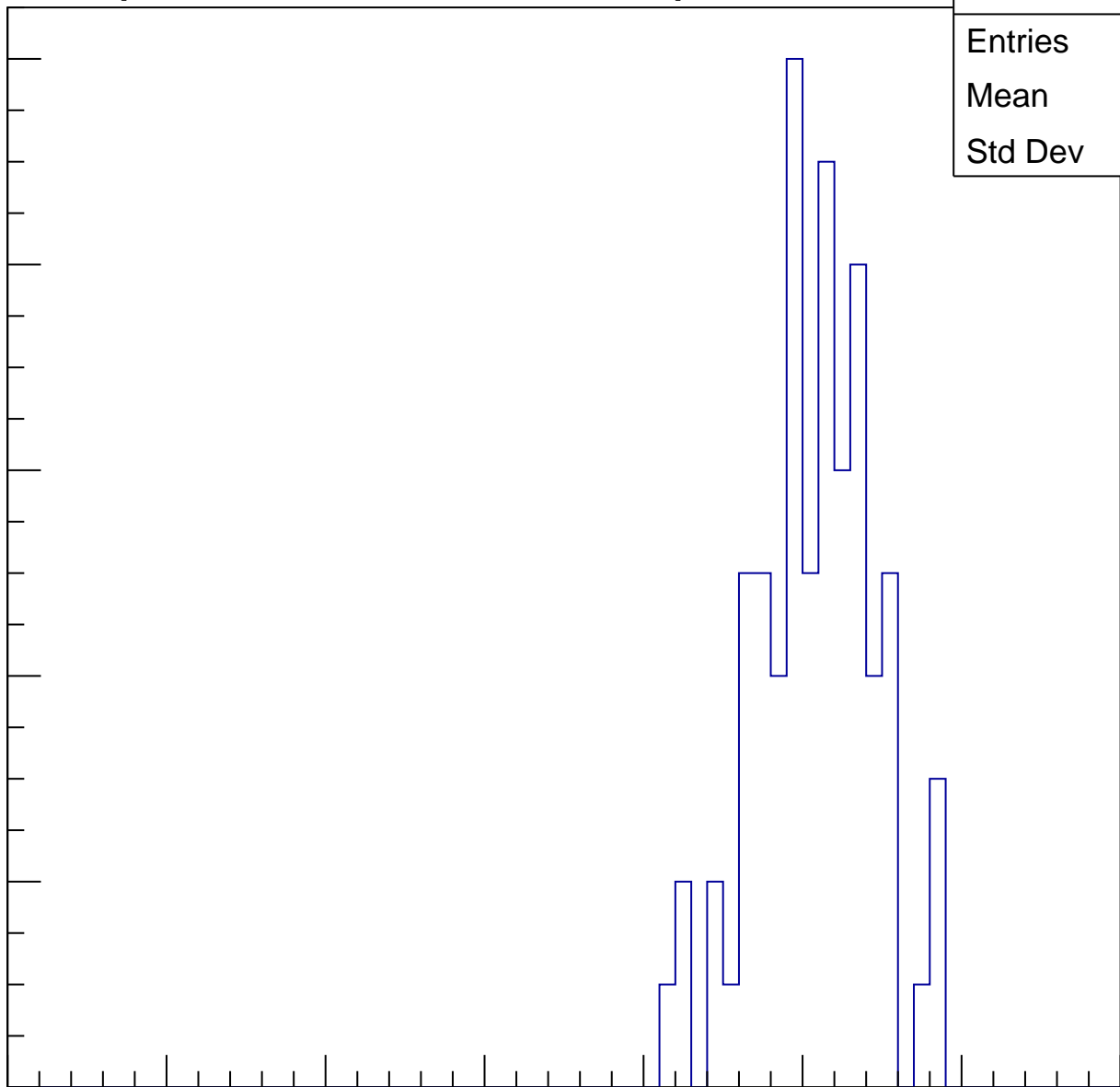
Entries	71
Mean	50.31
Std Dev	3.725

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

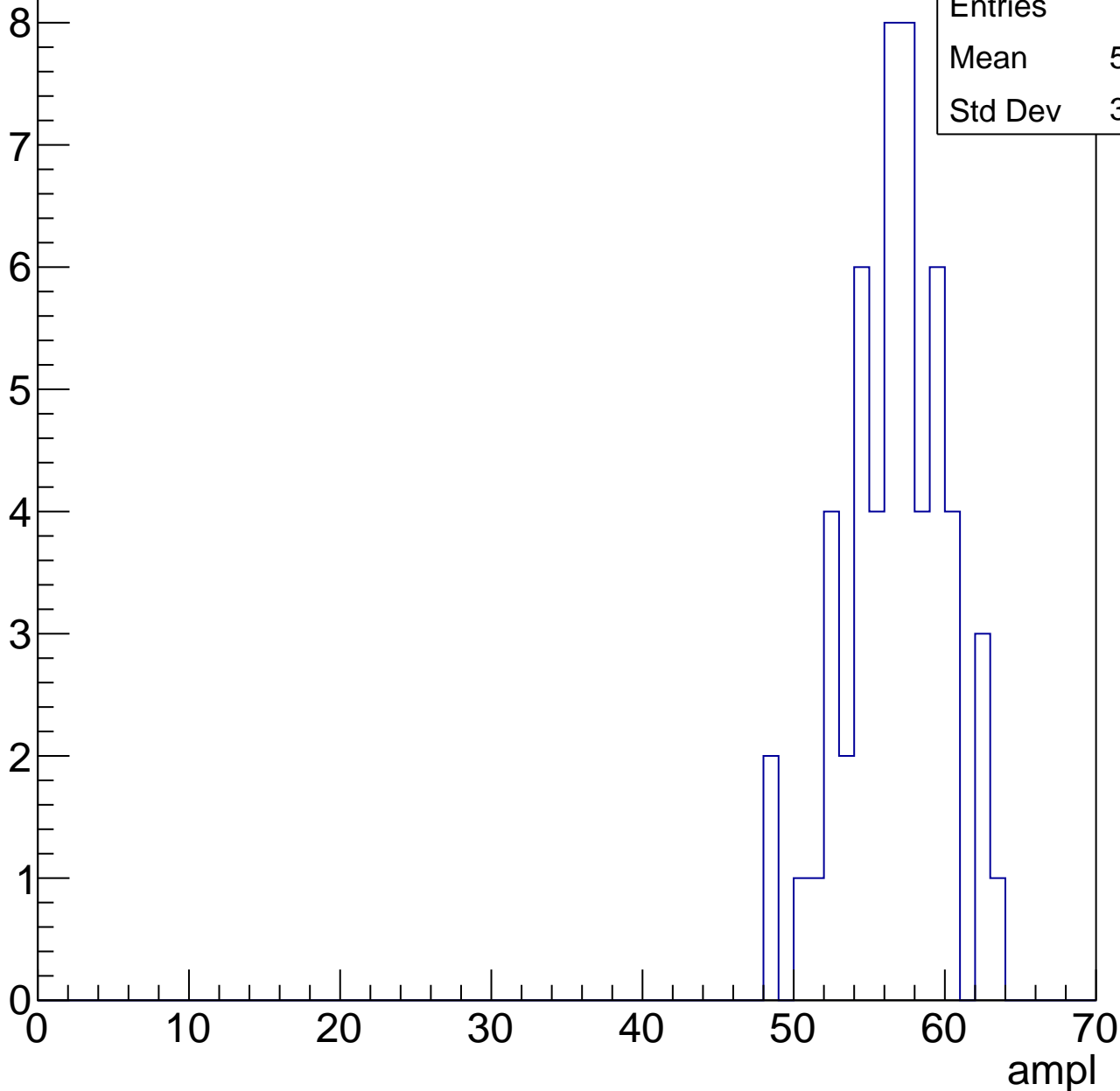


# B1L101S, U16-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	56.19
Std Dev	3.323

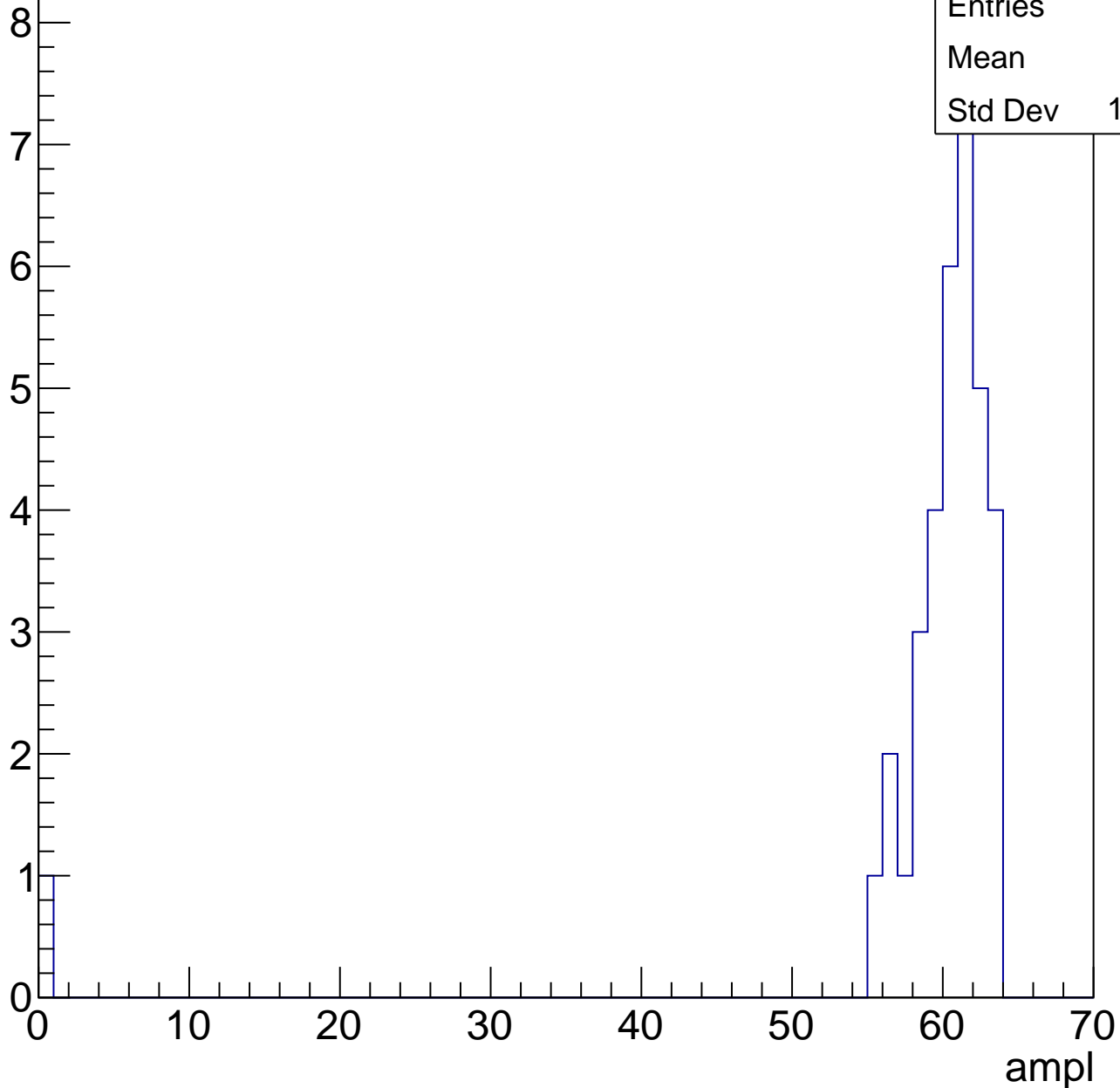


# B1L101S, U16-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	35
Mean	58.4
Std Dev	10.22

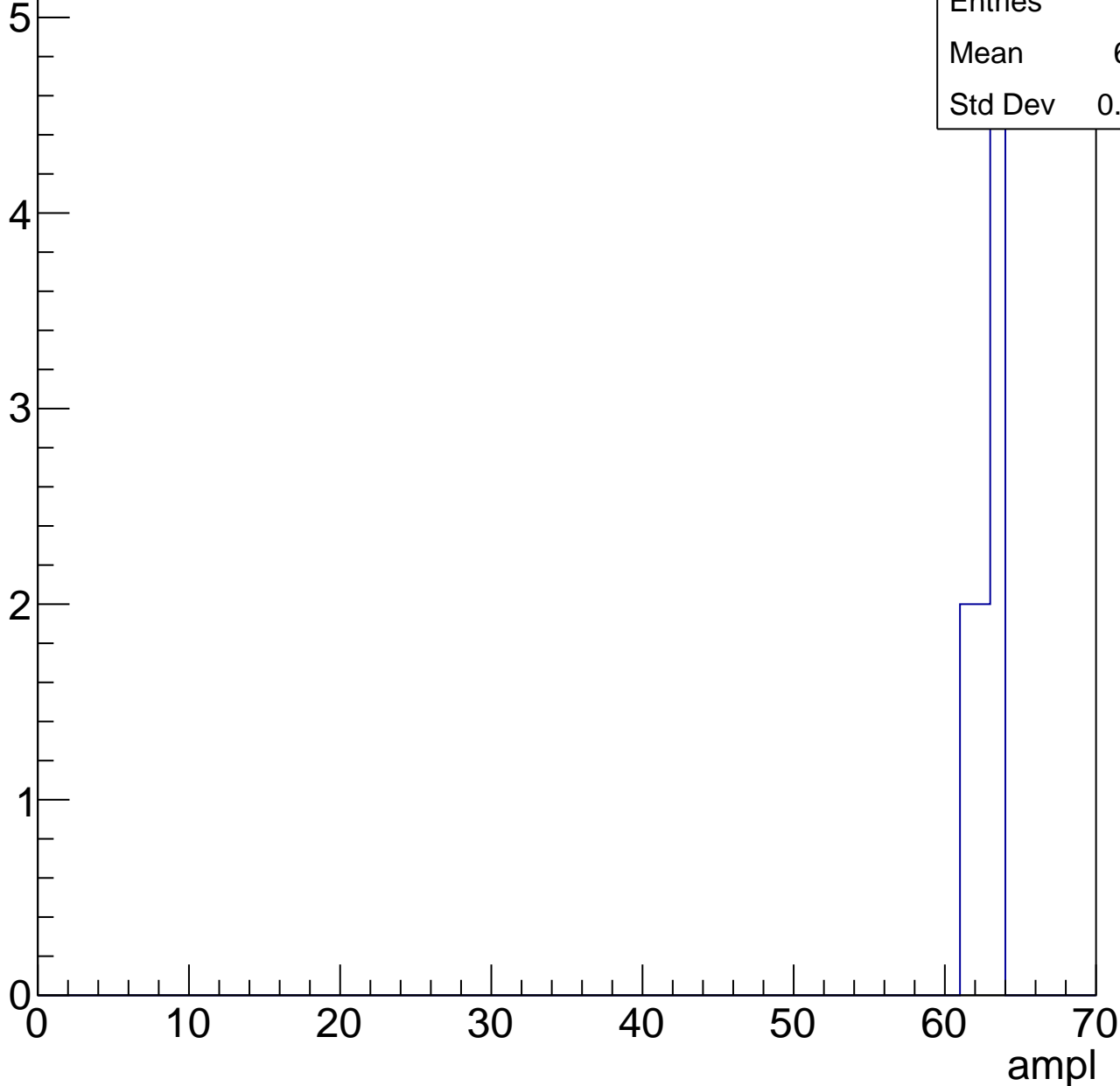


# B1L101S, U16-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	9
Mean	62.33
Std Dev	0.8165





# B1L101S, U16-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U16-ch106, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	86
Mean	28.66
Std Dev	6.847

**Gaus mean : 30.4205**

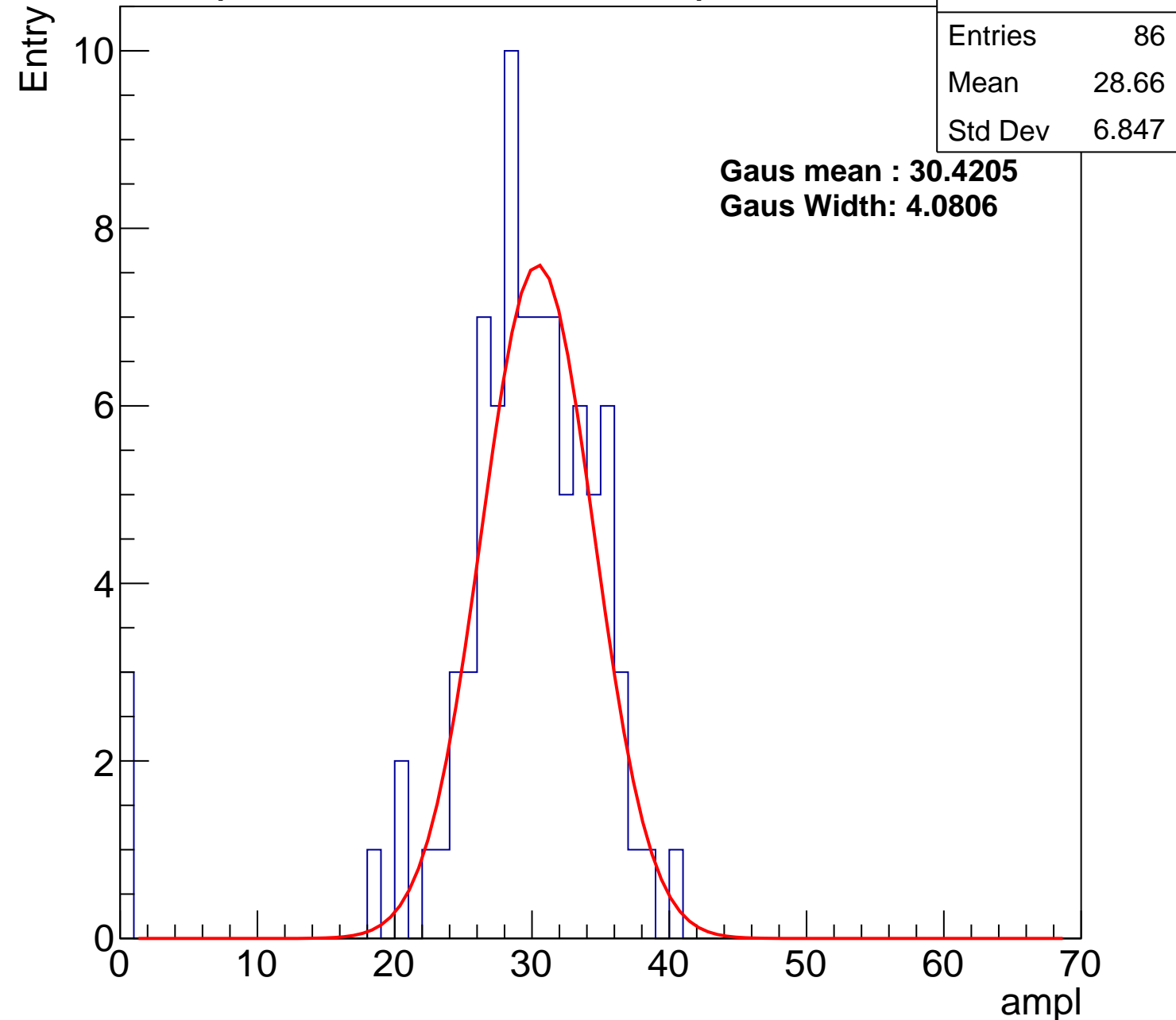
**Gaus Width: 4.0806**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch106, adc1

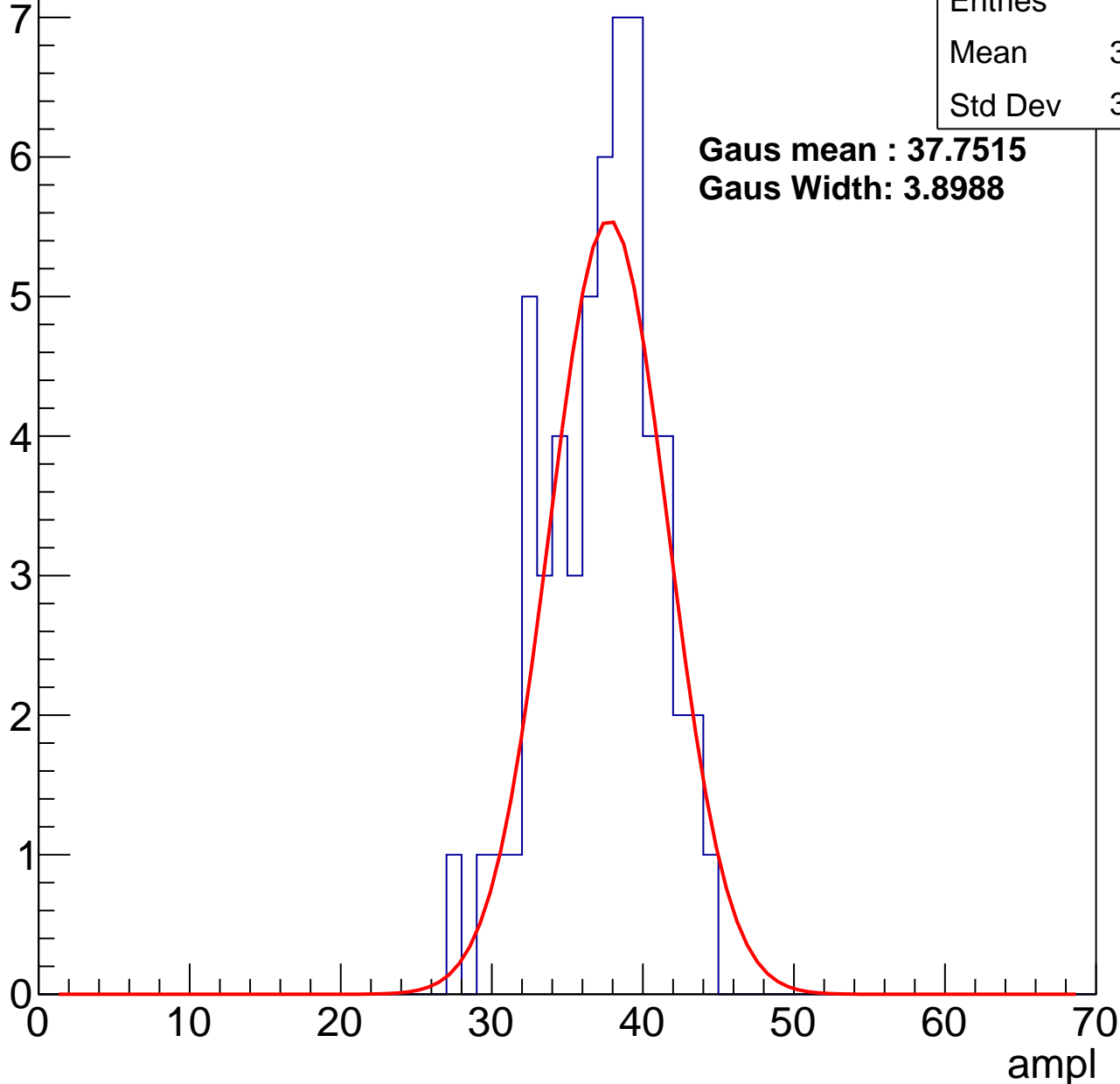
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	36.77
Std Dev	3.695

**Gaus mean : 37.7515**

**Gaus Width: 3.8988**



# B1L101S, U16-ch106, adc2

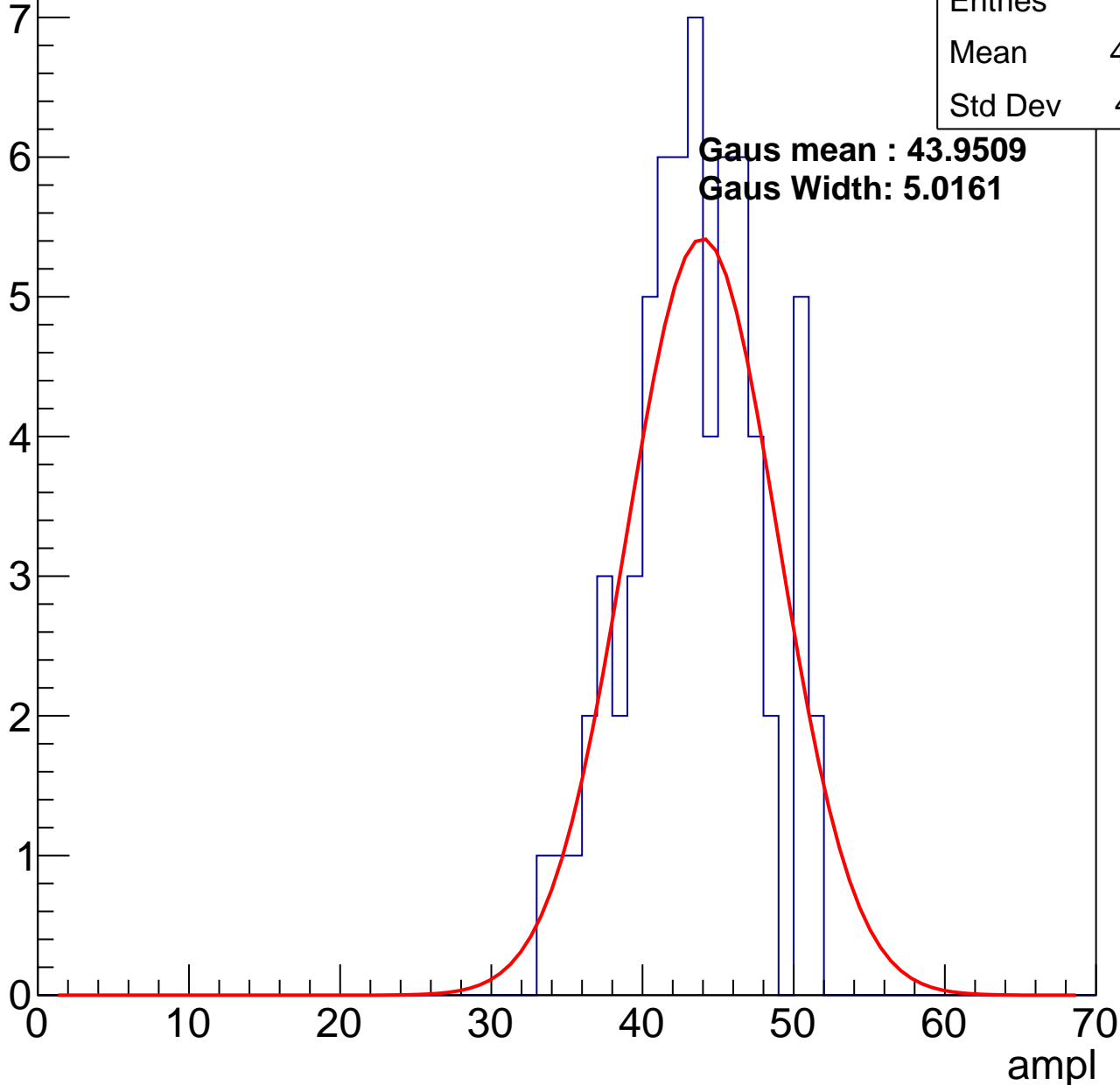
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	42.95
Std Dev	4.251

**Gaus mean : 43.9509**

**Gaus Width: 5.0161**

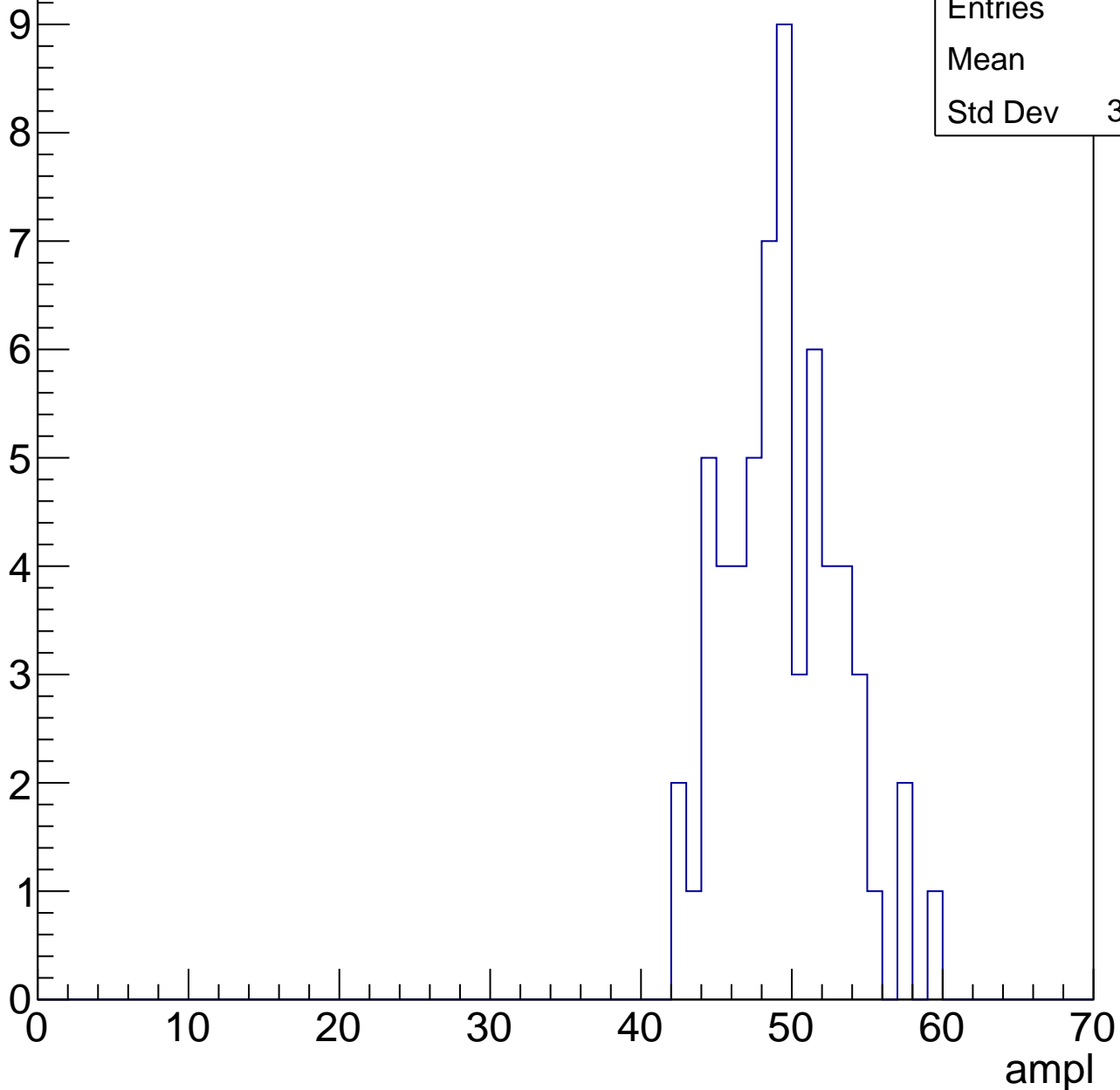


# B1L101S, U16-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	49
Std Dev	3.737

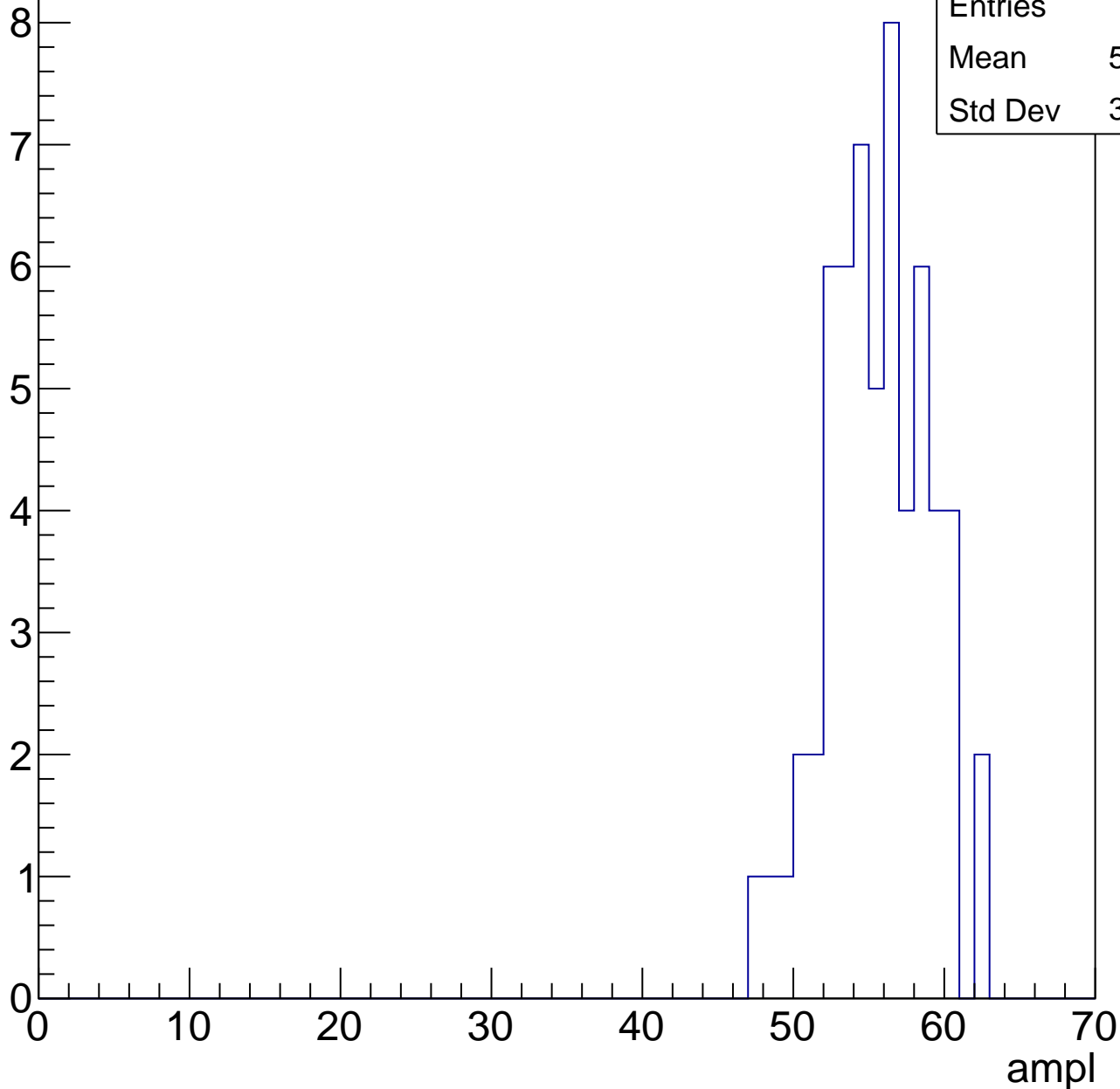


# B1L101S, U16-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	55.14
Std Dev	3.332

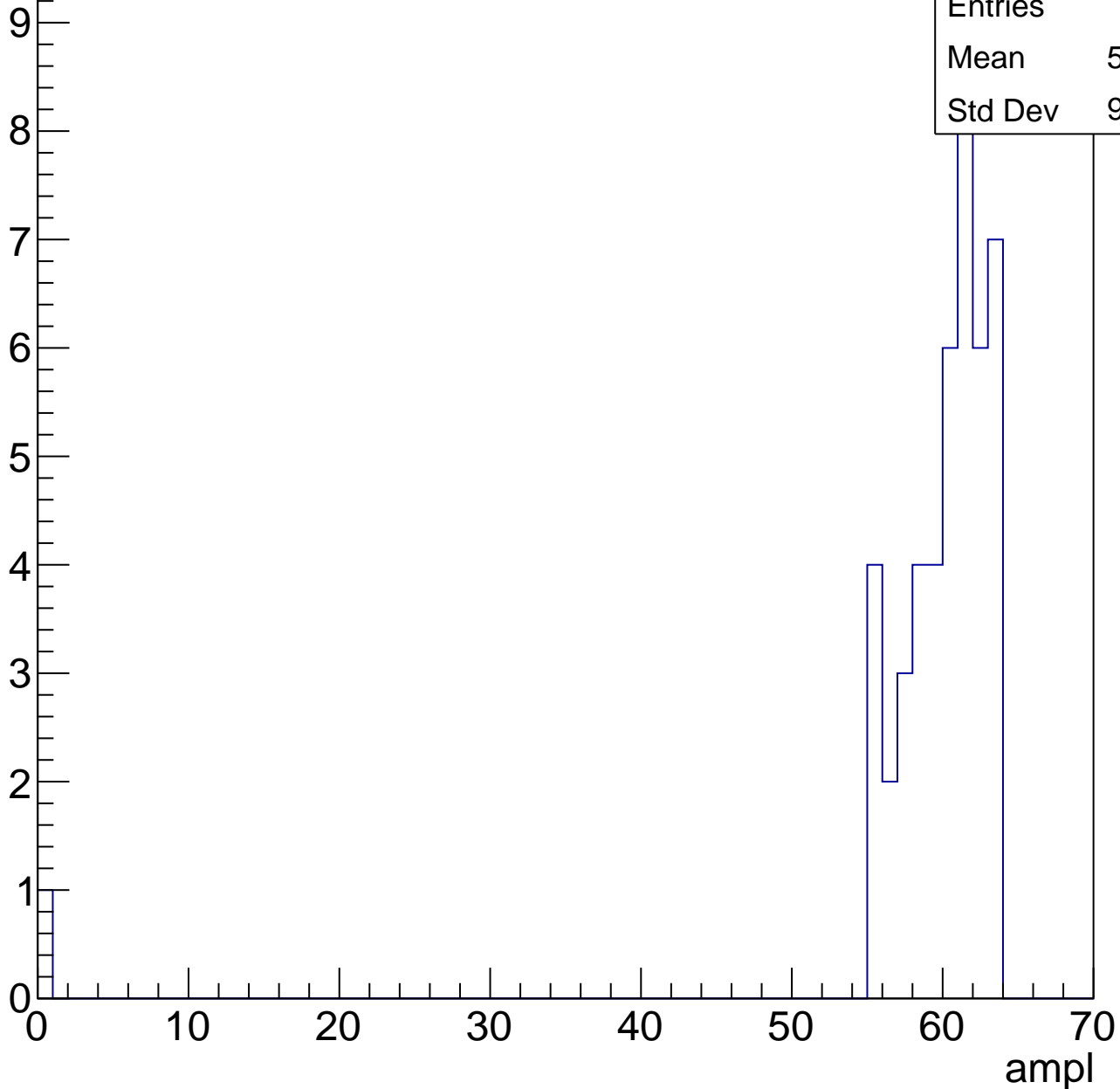


# B1L101S, U16-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

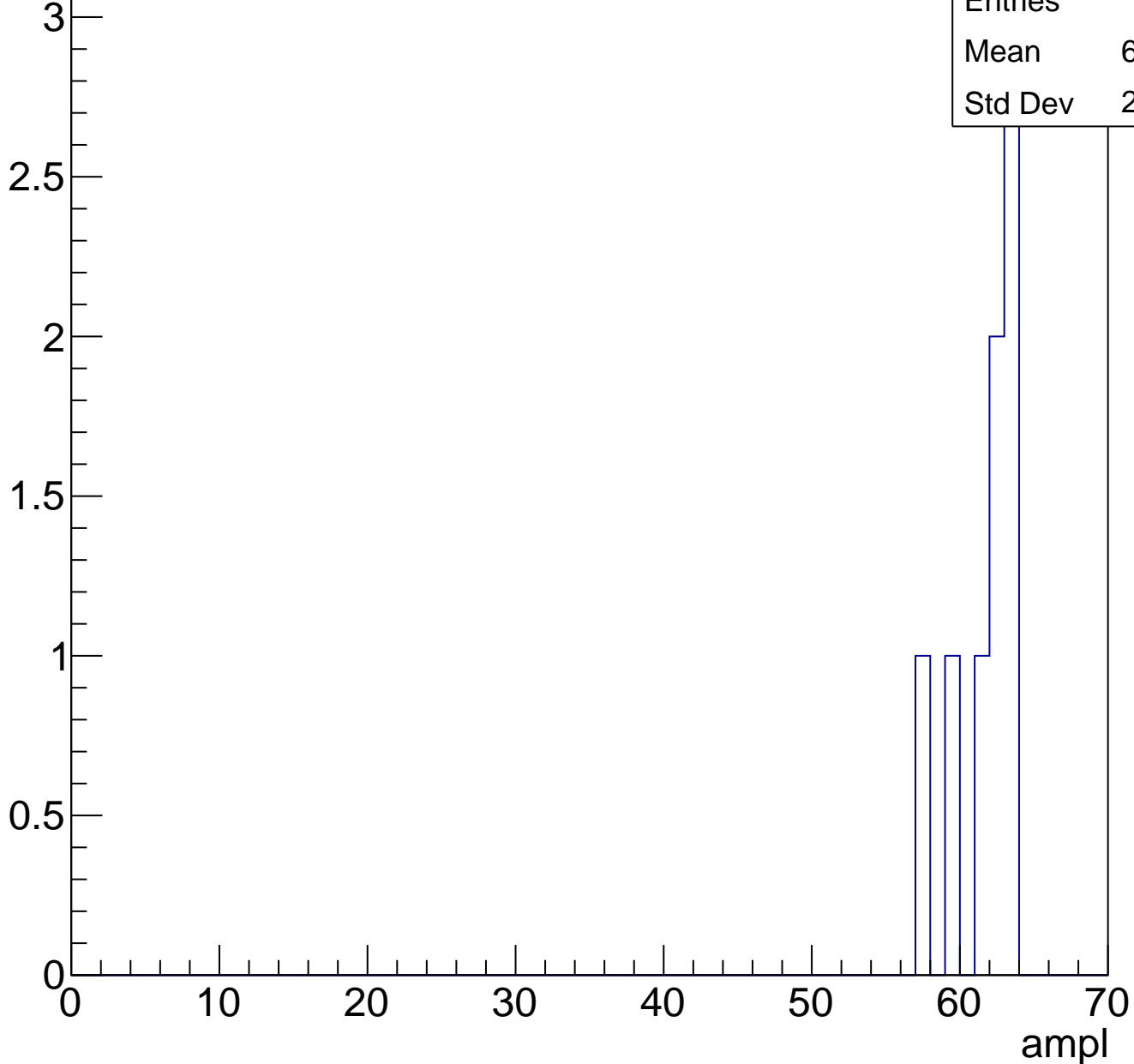
Entries	46
Mean	58.54
Std Dev	9.062



# B1L101S, U16-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U16-ch107, adc0

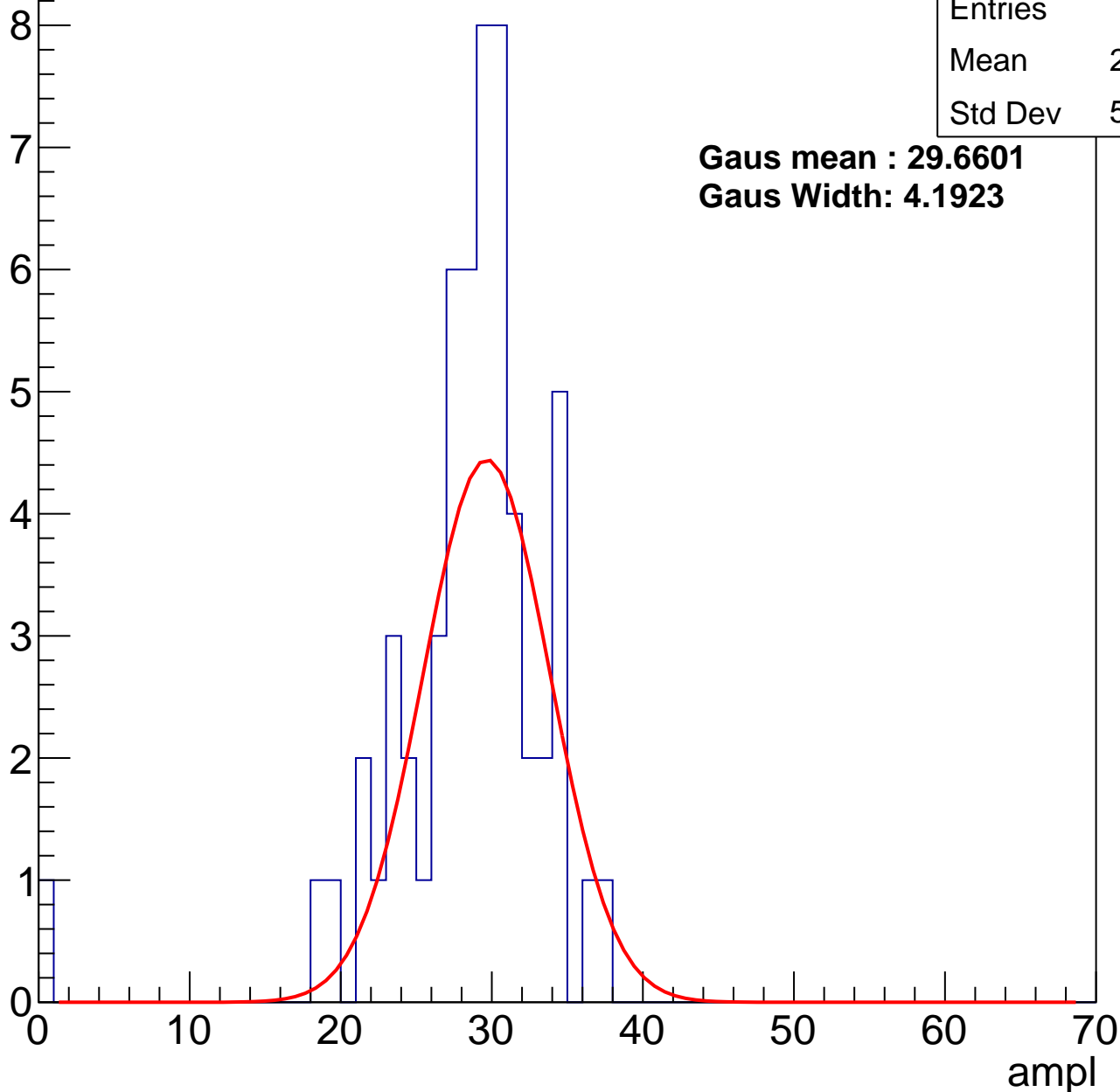
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	27.93
Std Dev	5.439

**Gaus mean : 29.6601**

**Gaus Width: 4.1923**



# B1L101S, U16-ch107, adc1

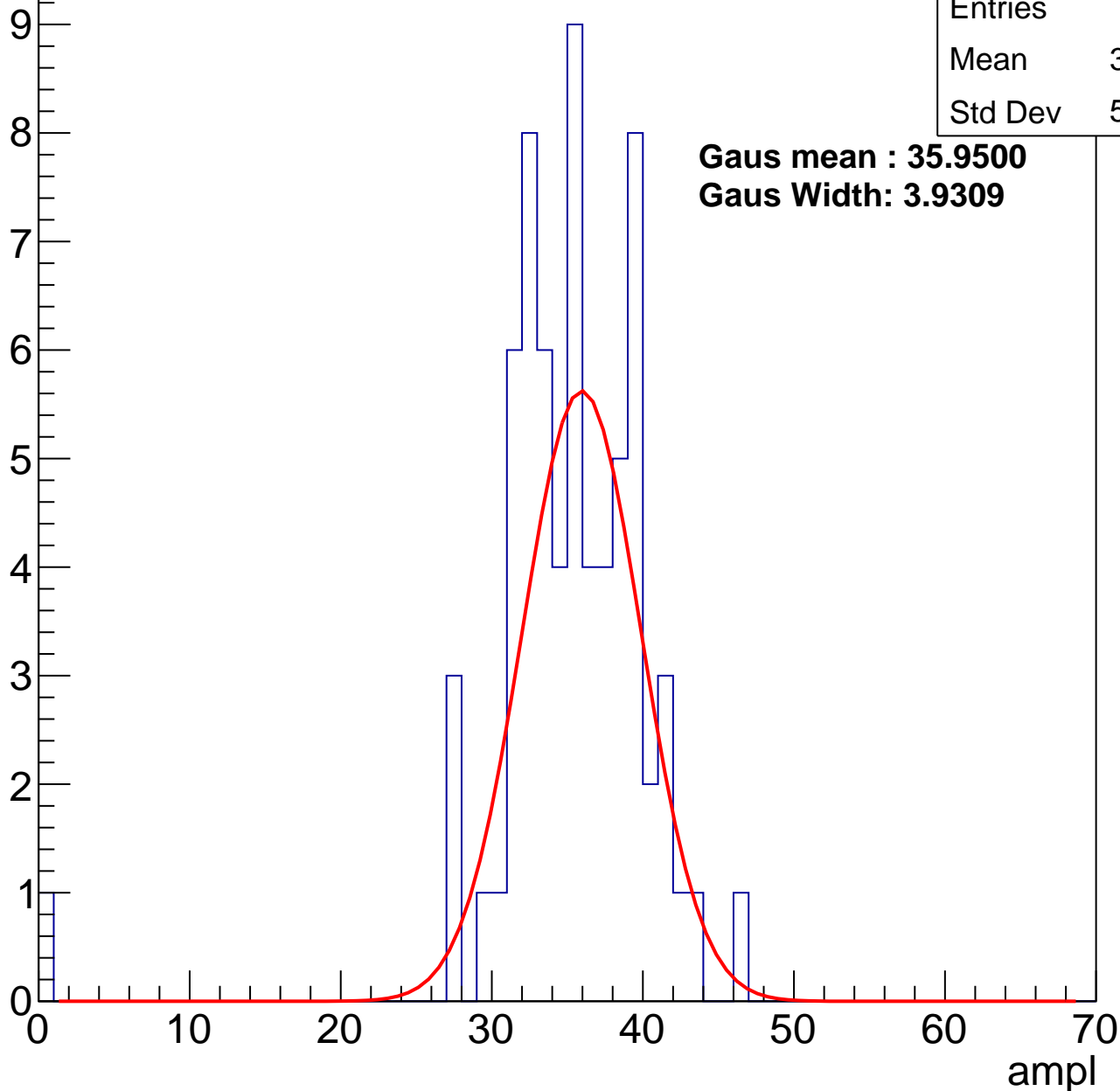
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	34.69
Std Dev	5.755

**Gaus mean : 35.9500**

**Gaus Width: 3.9309**



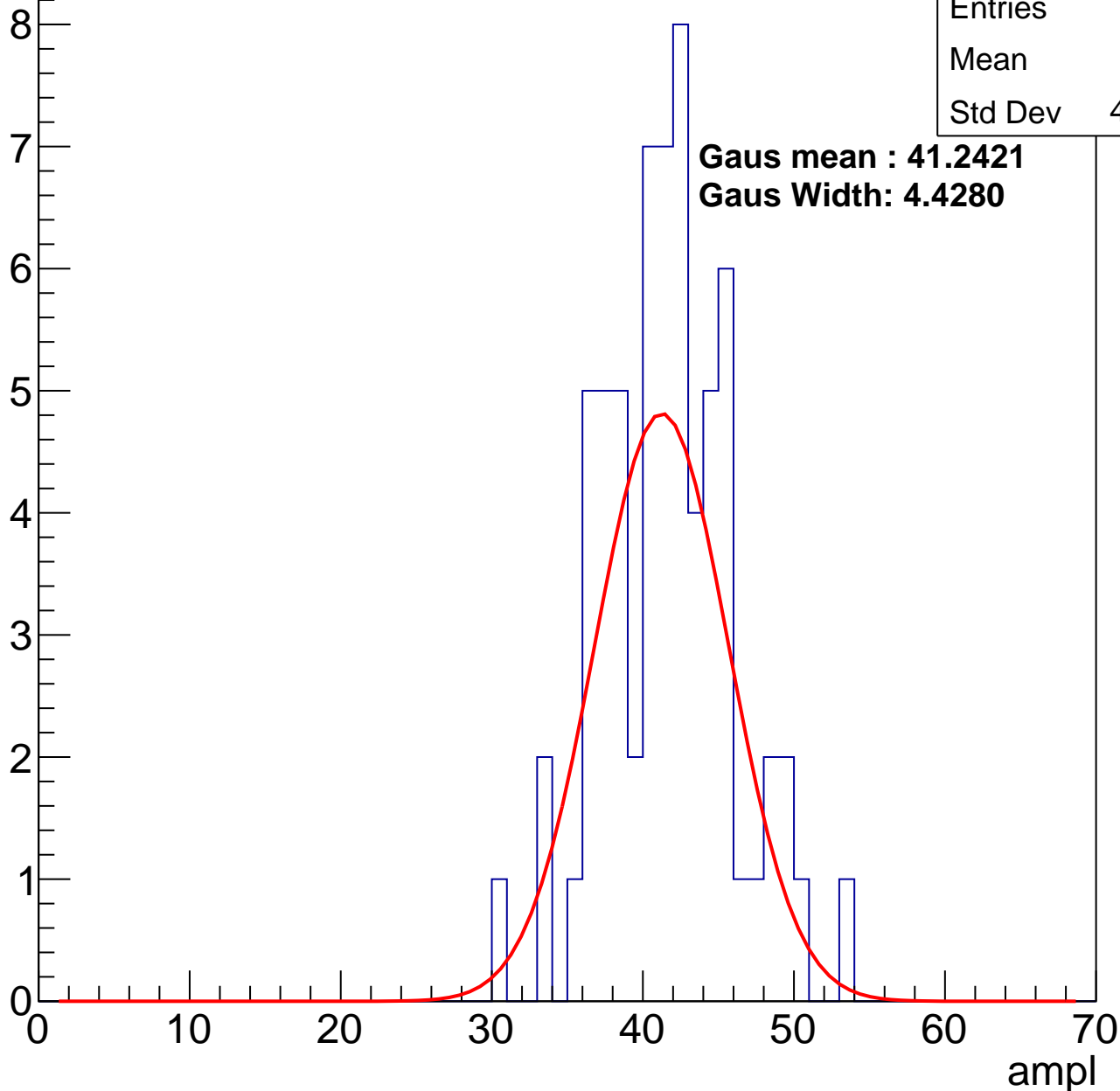
# B1L101S, U16-ch107, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	41.2
Std Dev	4.307

**Gaus mean : 41.2421**  
**Gaus Width: 4.4280**

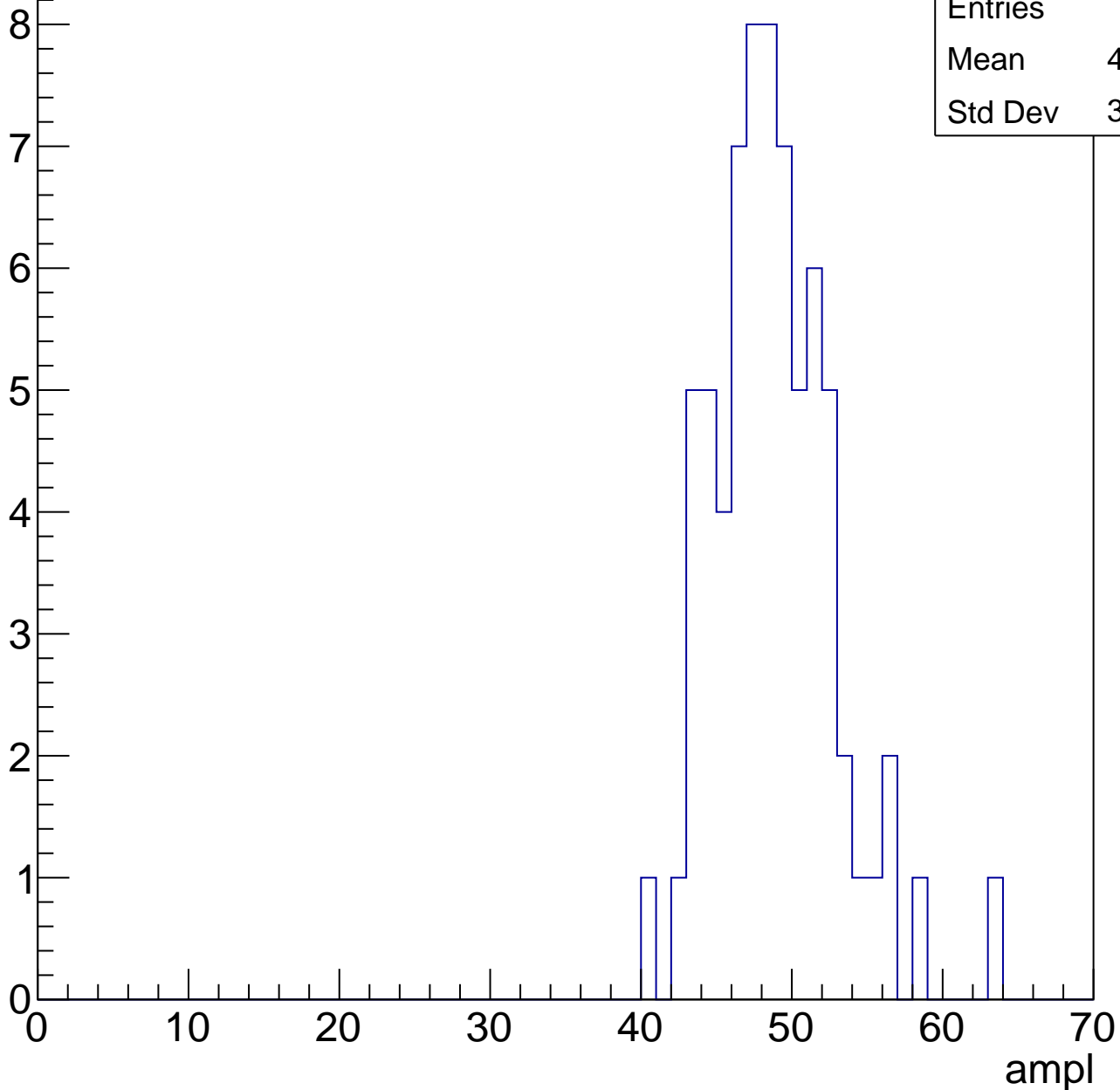


# B1L101S, U16-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	48.37
Std Dev	3.993

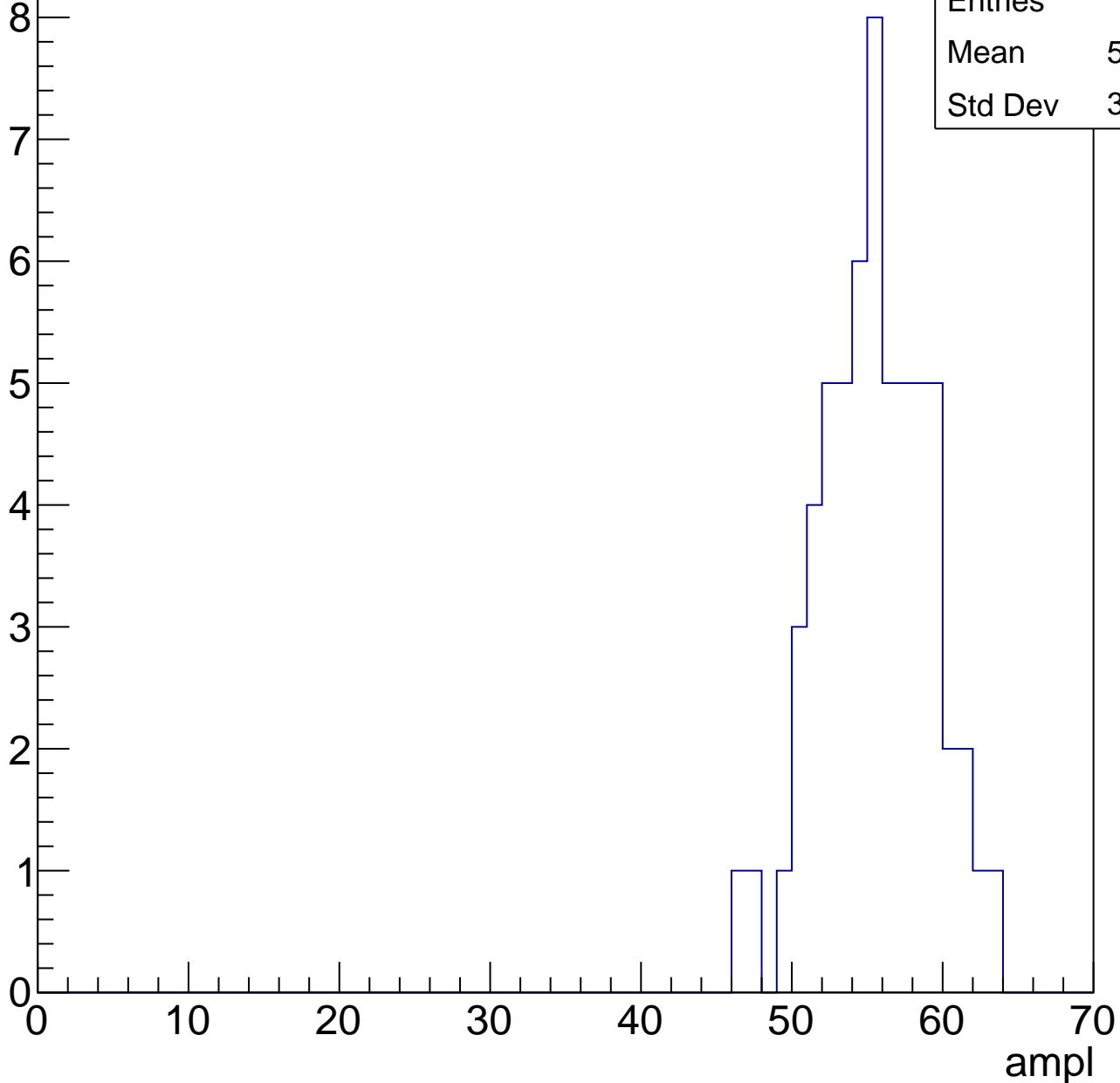


# B1L101S, U16-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	55.03
Std Dev	3.596

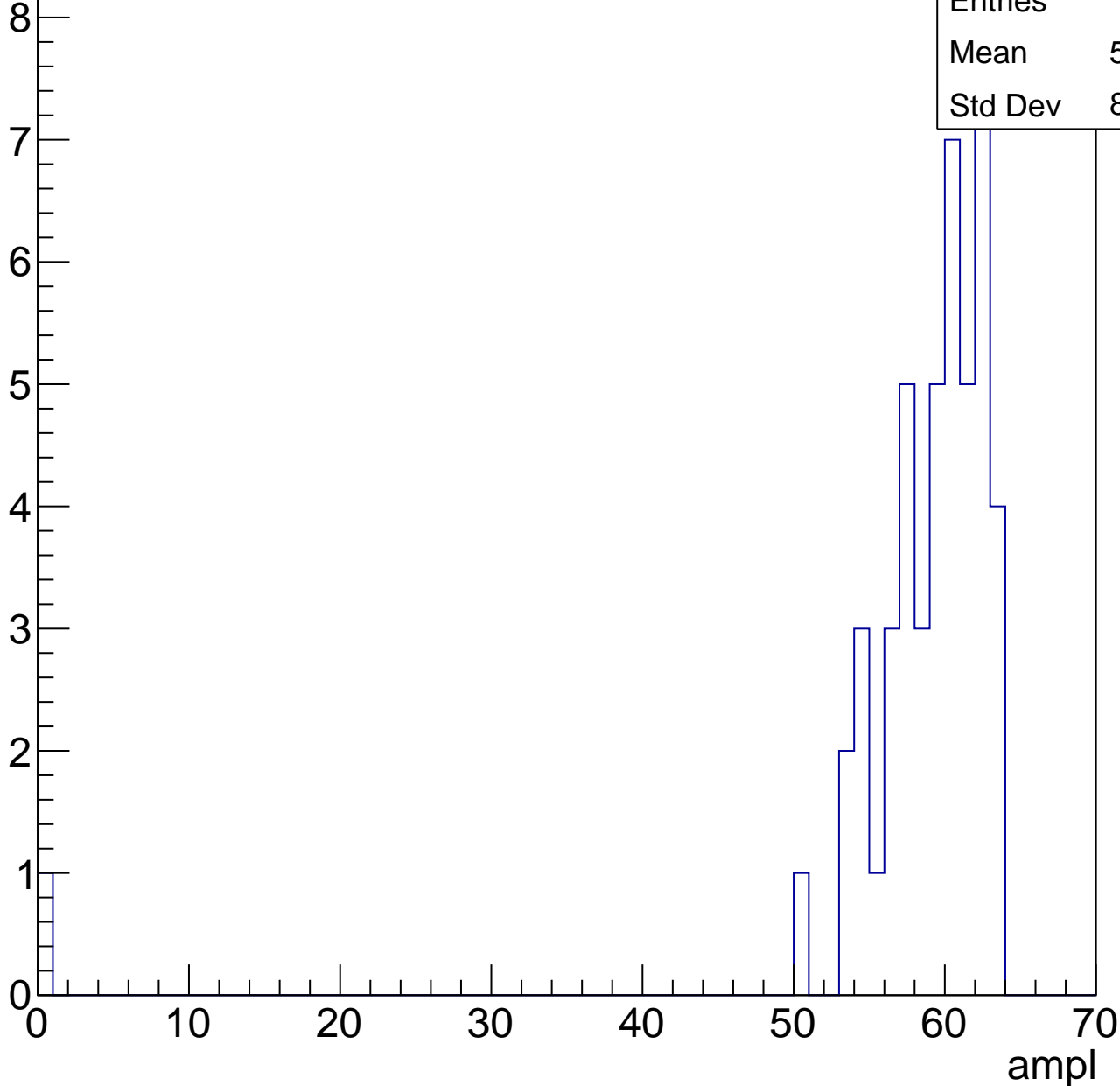


# B1L101S, U16-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

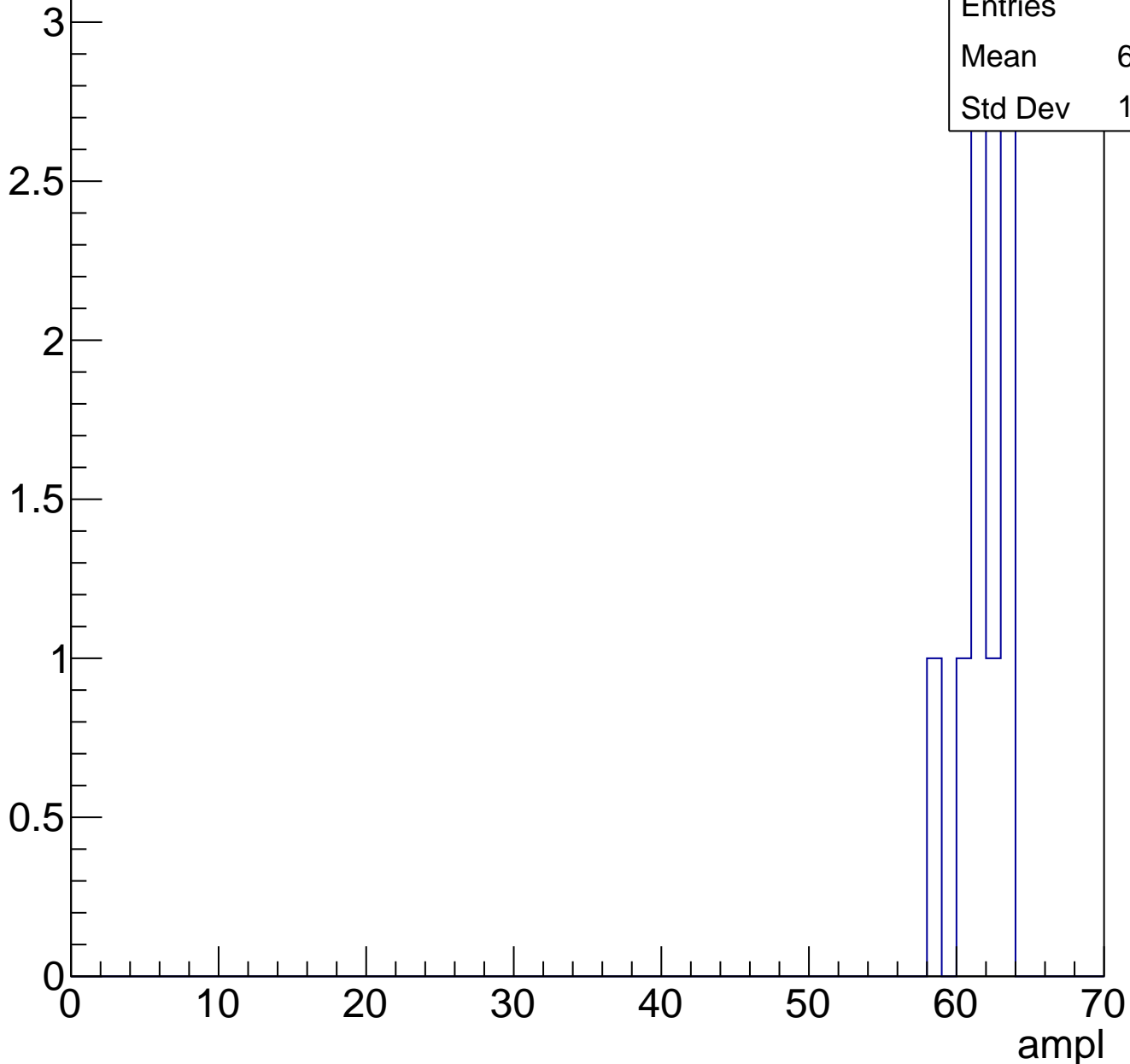
Entries	48
Mean	57.67
Std Dev	8.959



# B1L101S, U16-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	63
Std Dev	0

# B1L101S, U16-ch108, adc0

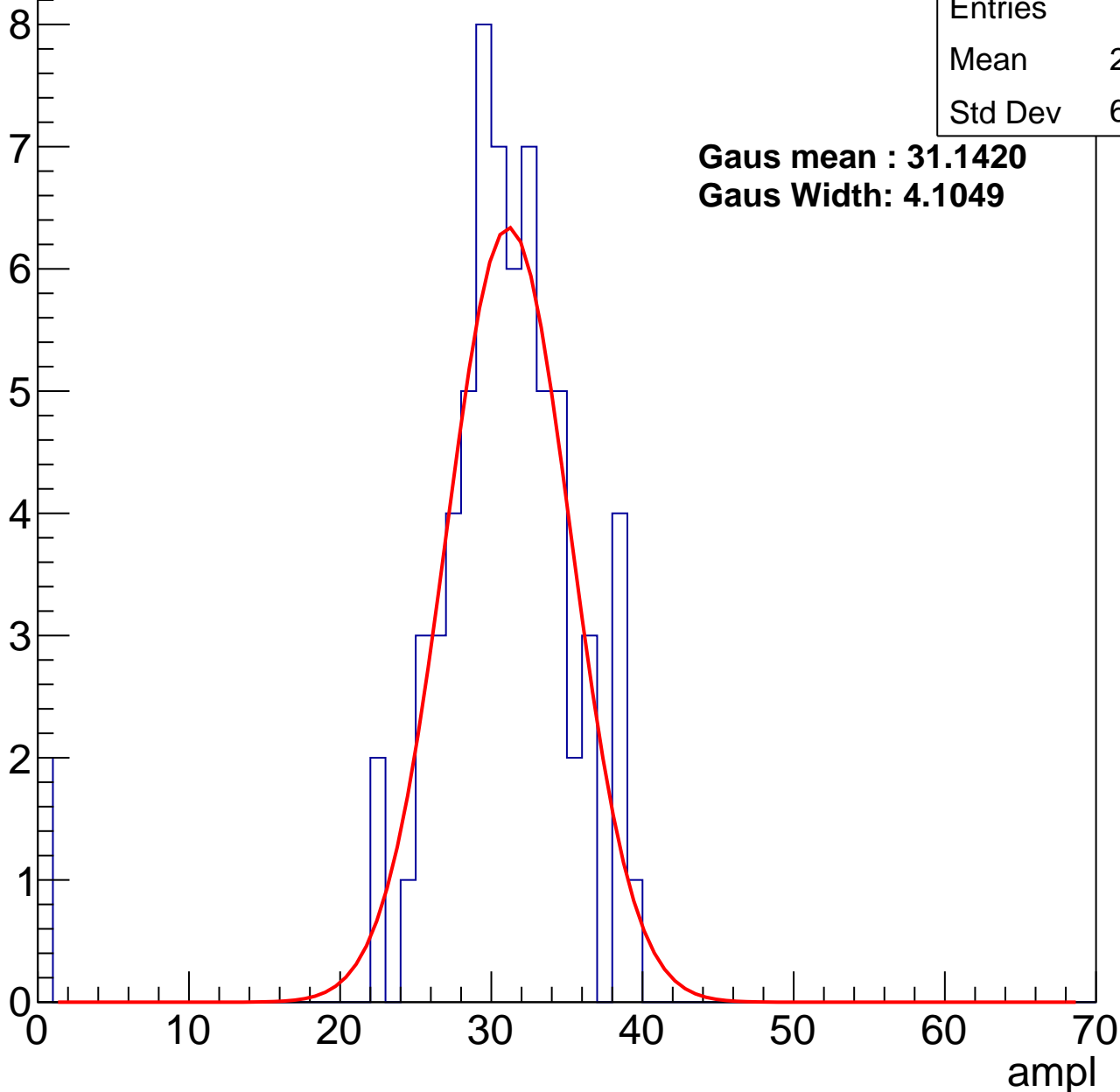
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	29.78
Std Dev	6.419

**Gaus mean : 31.1420**

**Gaus Width: 4.1049**



# B1L101S, U16-ch108, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	70
Mean	36.17
Std Dev	5.796

**Gaus mean : 36.5723**

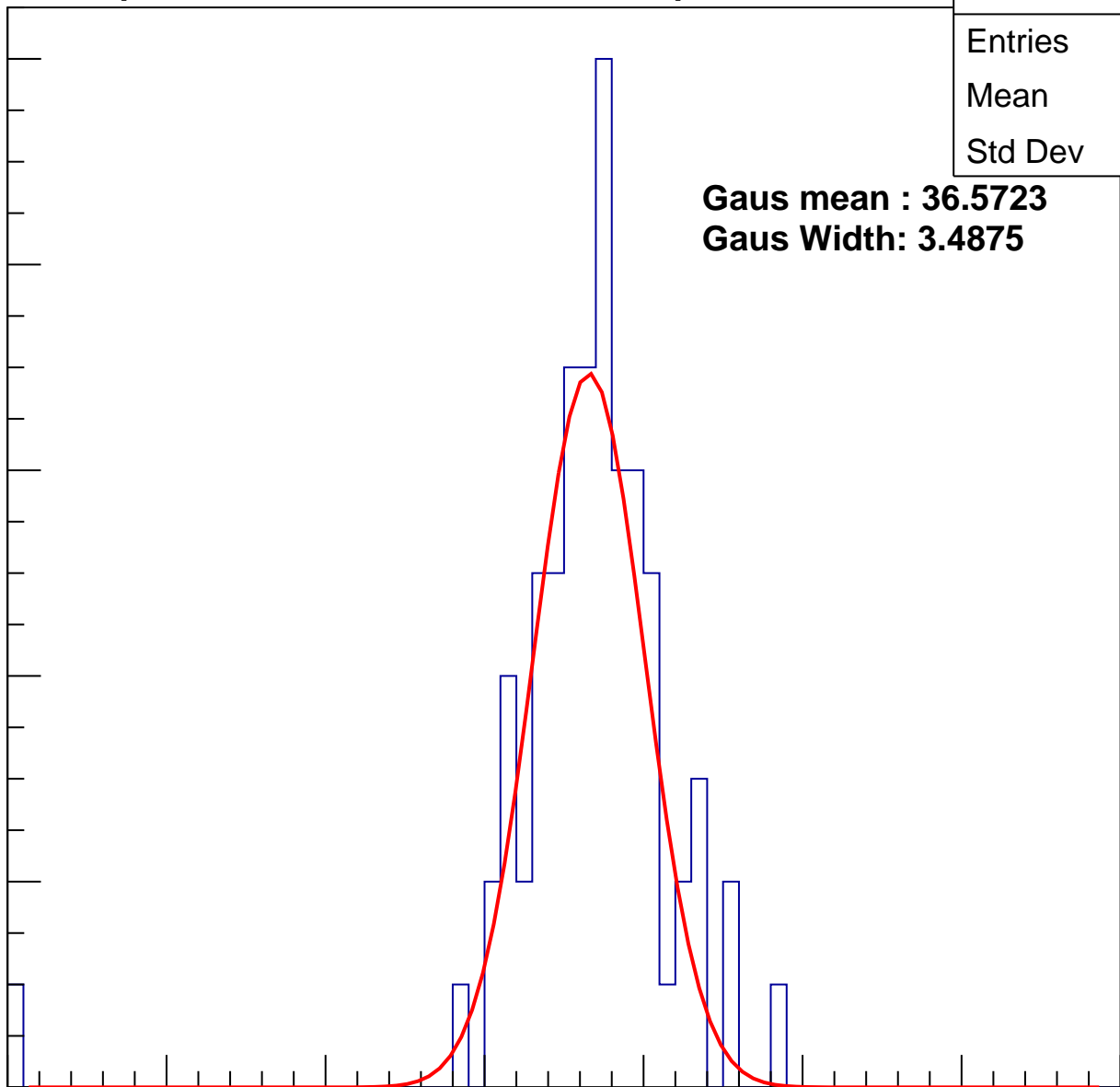
**Gaus Width: 3.4875**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch108, adc2

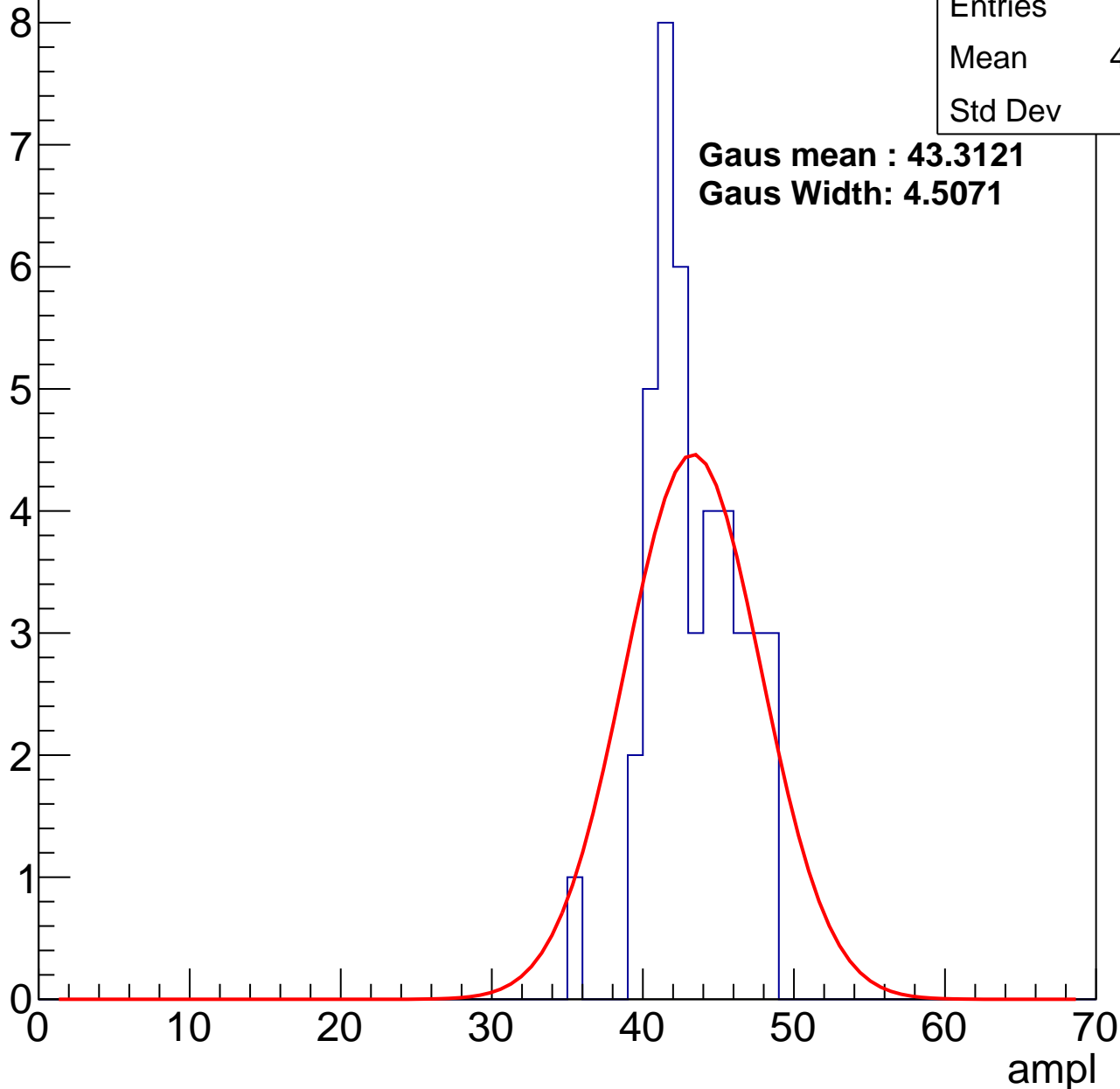
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	42.88
Std Dev	2.88

**Gaus mean : 43.3121**

**Gaus Width: 4.5071**

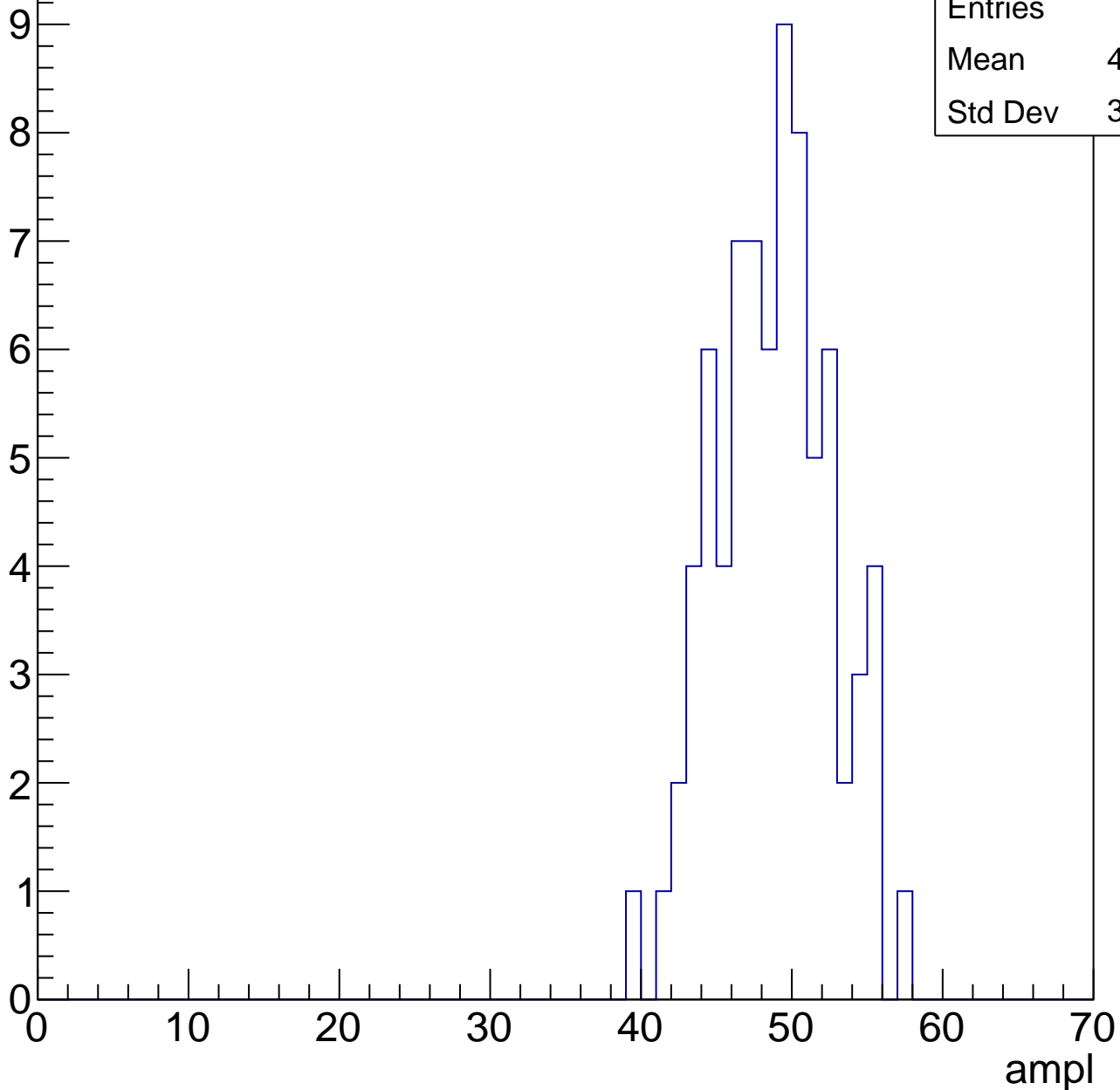


# B1L101S, U16-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	48.32
Std Dev	3.767

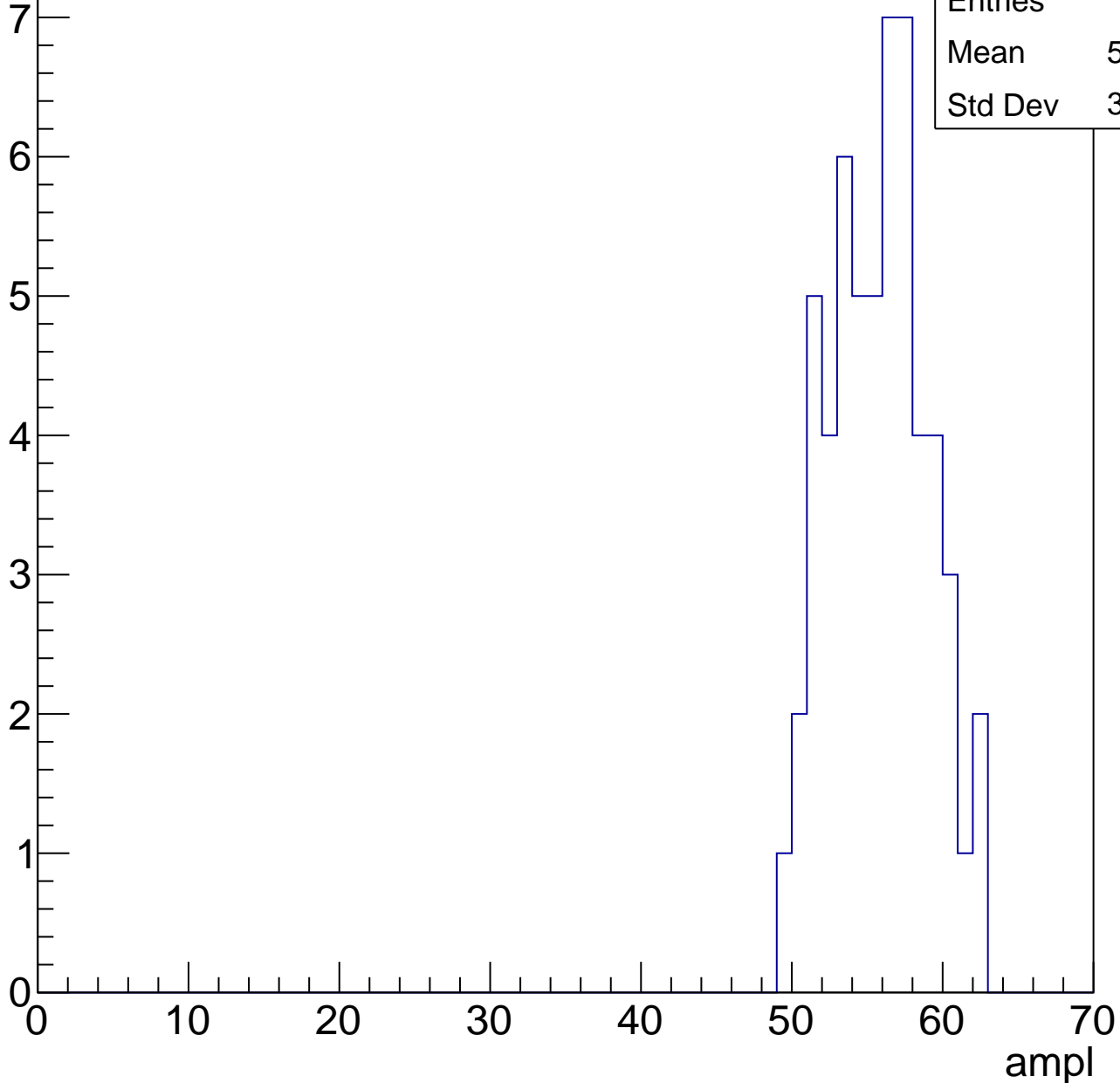


# B1L101S, U16-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	55.34
Std Dev	3.186

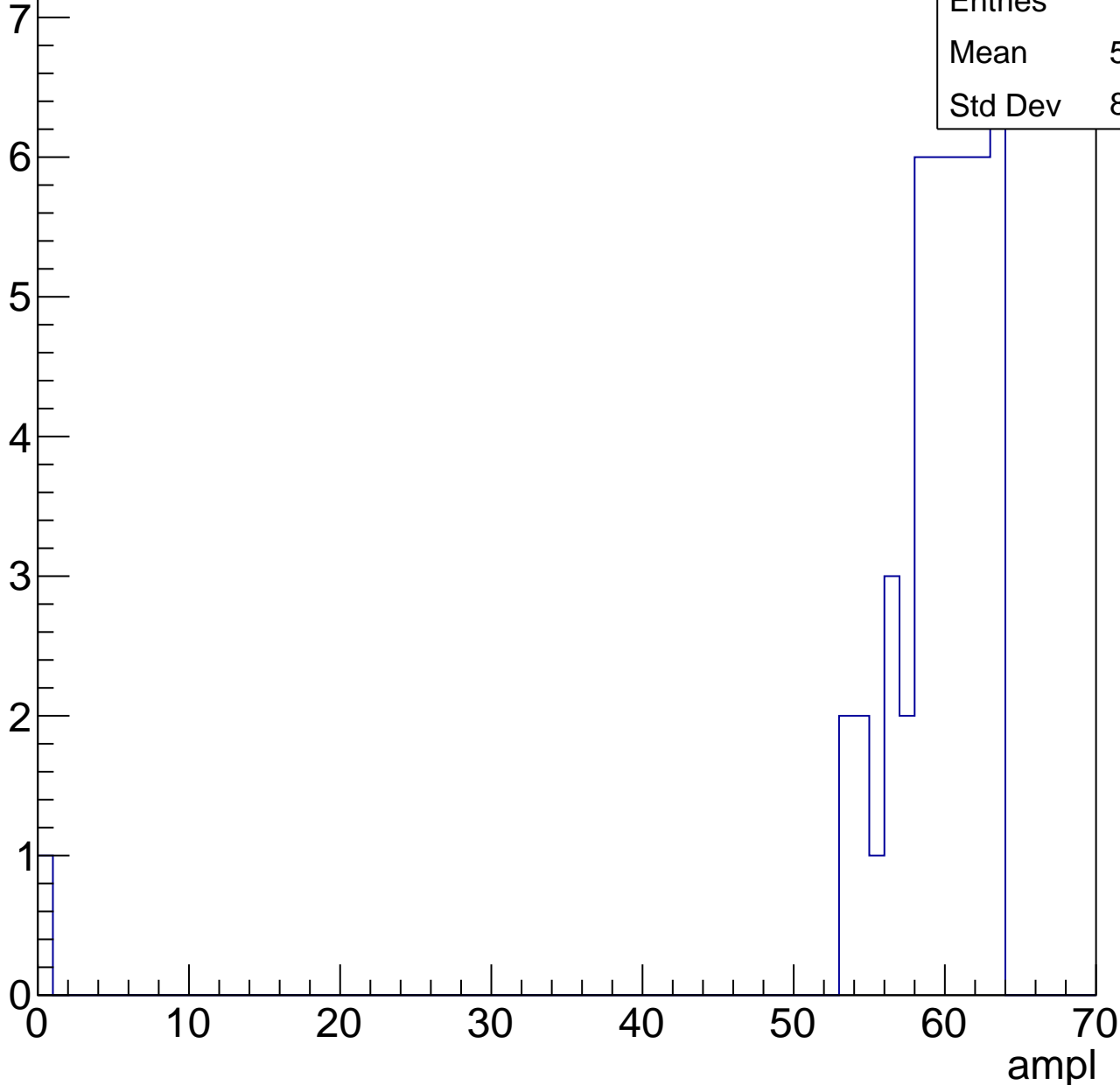


# B1L101S, U16-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

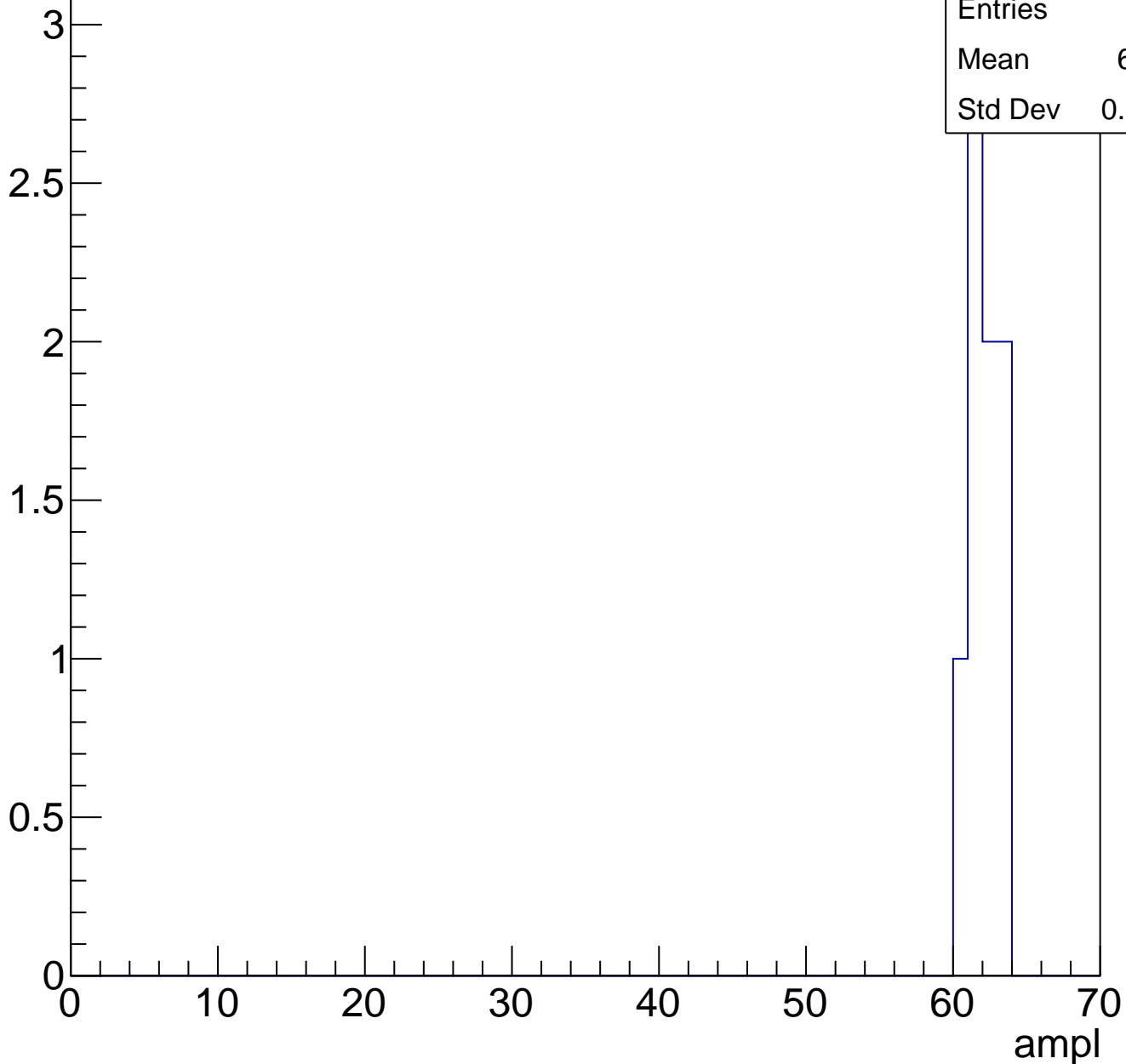
Entries	48
Mean	58.17
Std Dev	8.924



# B1L101S, U16-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch109, adc0

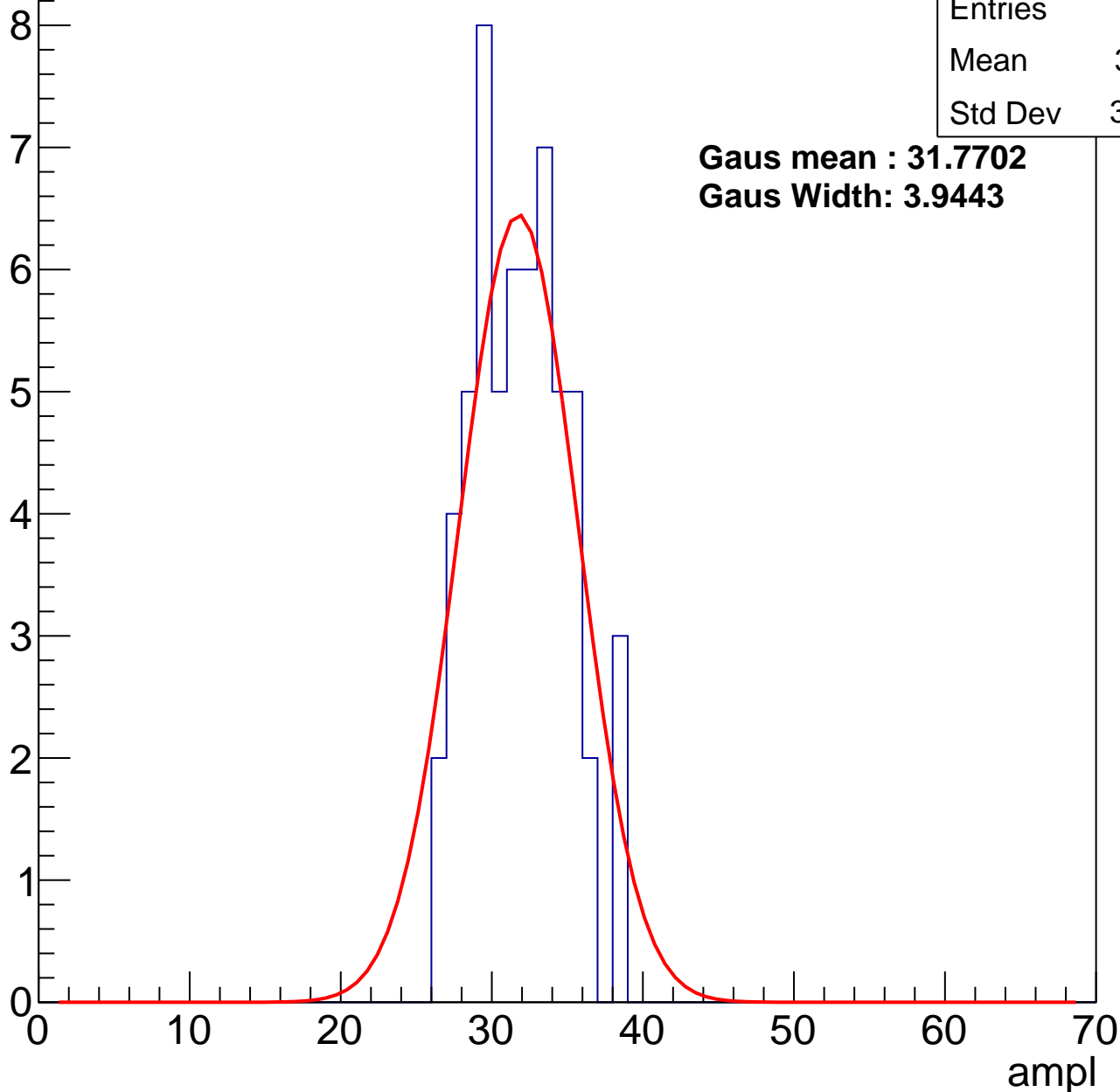
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	31.41
Std Dev	3.057

**Gaus mean : 31.7702**

**Gaus Width: 3.9443**



# B1L101S, U16-ch109, adc1

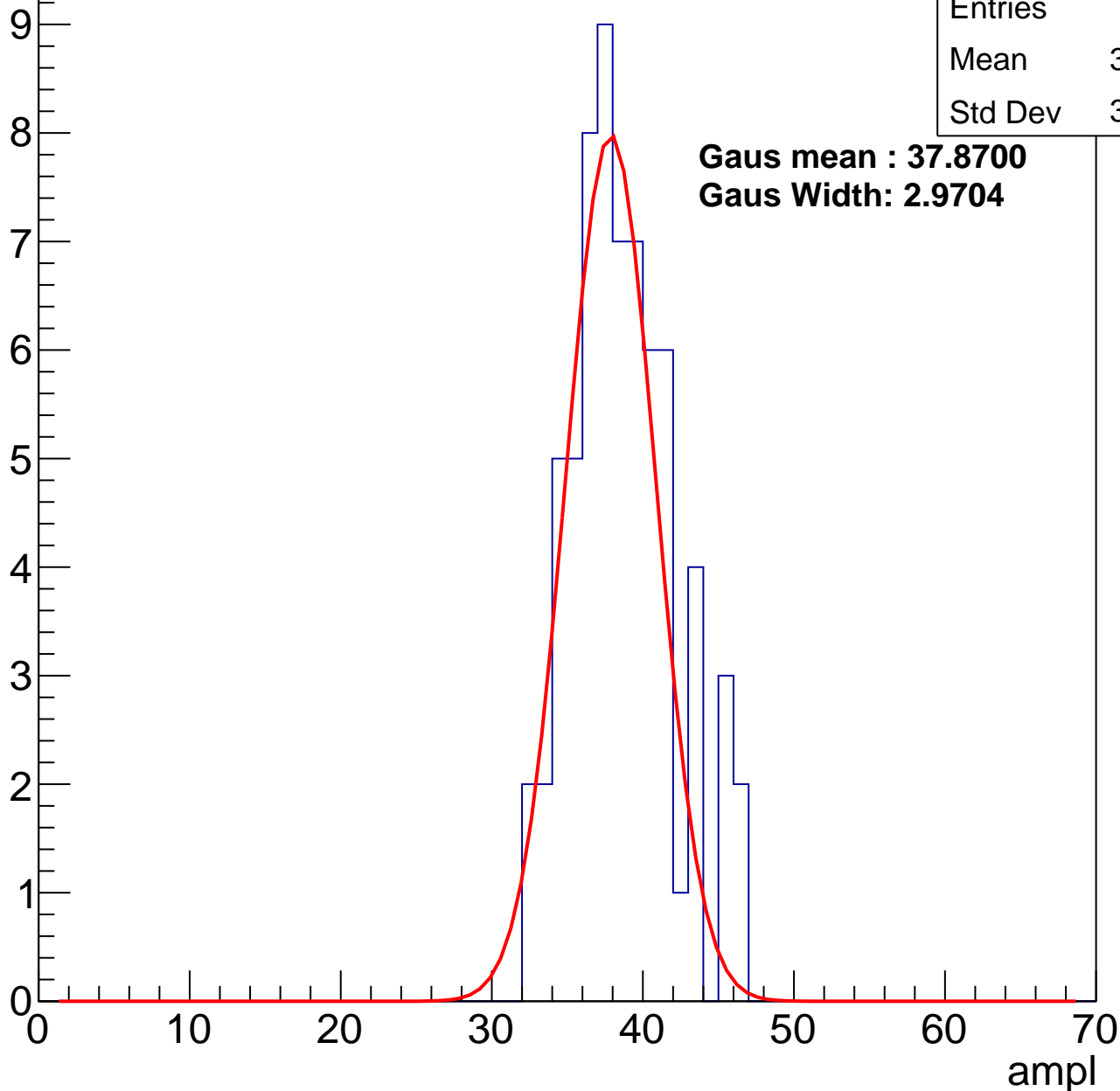
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	38.24
Std Dev	3.368

**Gaus mean : 37.8700**

**Gaus Width: 2.9704**



# B1L101S, U16-ch109, adc2

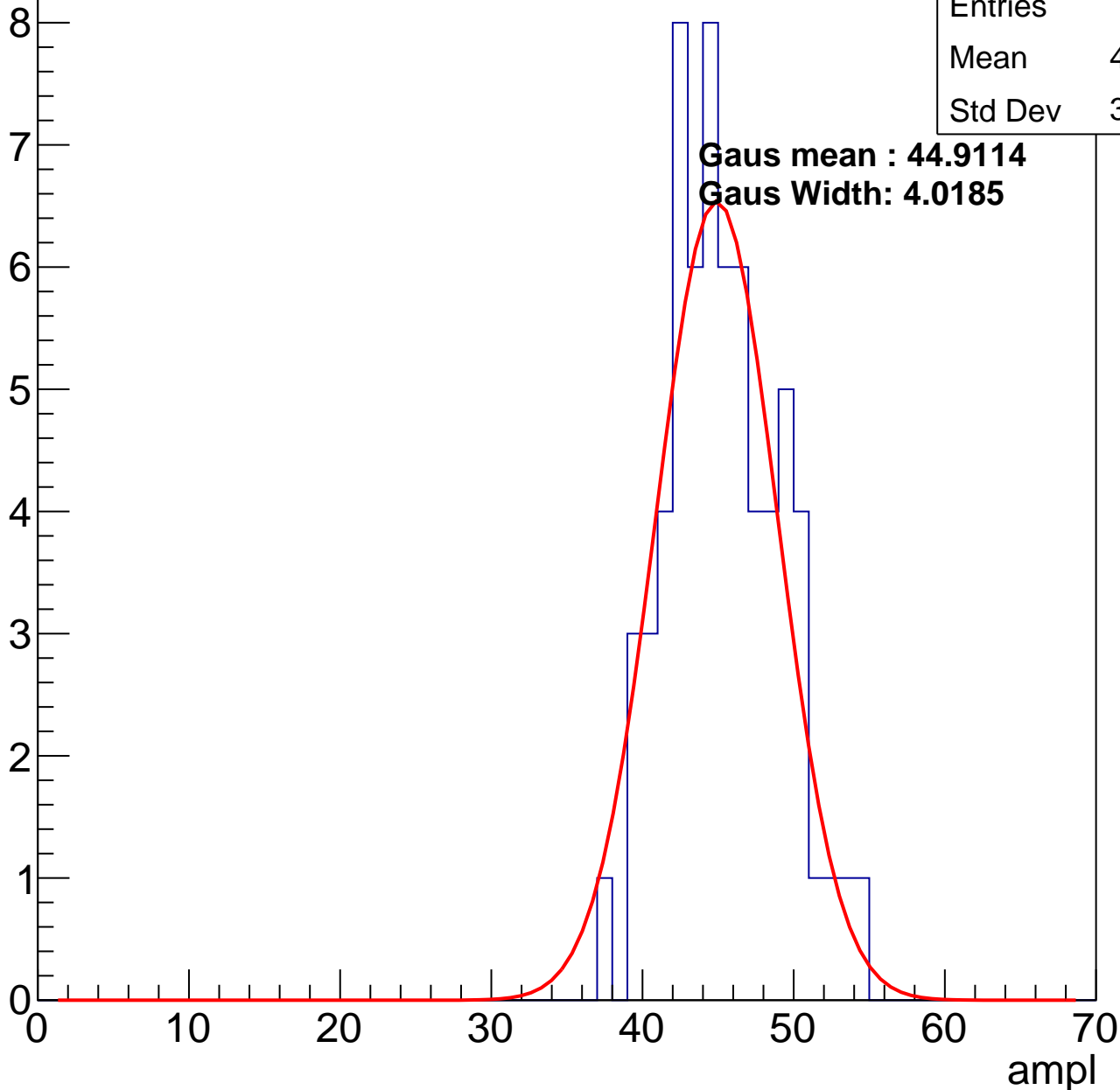
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	44.92
Std Dev	3.657

**Gaus mean : 44.9114**

**Gaus Width: 4.0185**

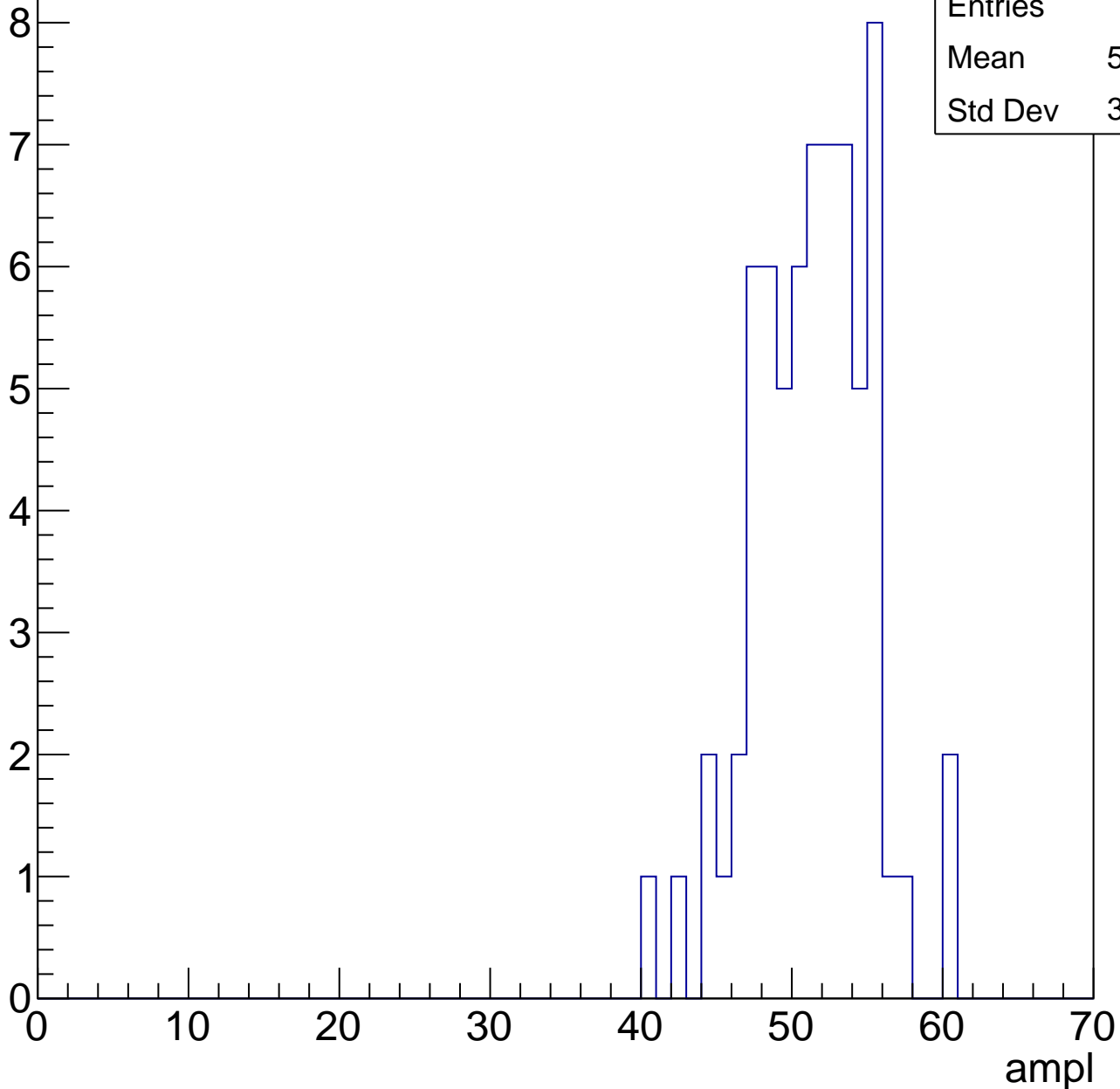


# B1L101S, U16-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	50.84
Std Dev	3.818



# B1L101S, U16-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	58
Mean	57.5
Std Dev	2.984

Entry

10

8

6

4

2

0

0

10

20

30

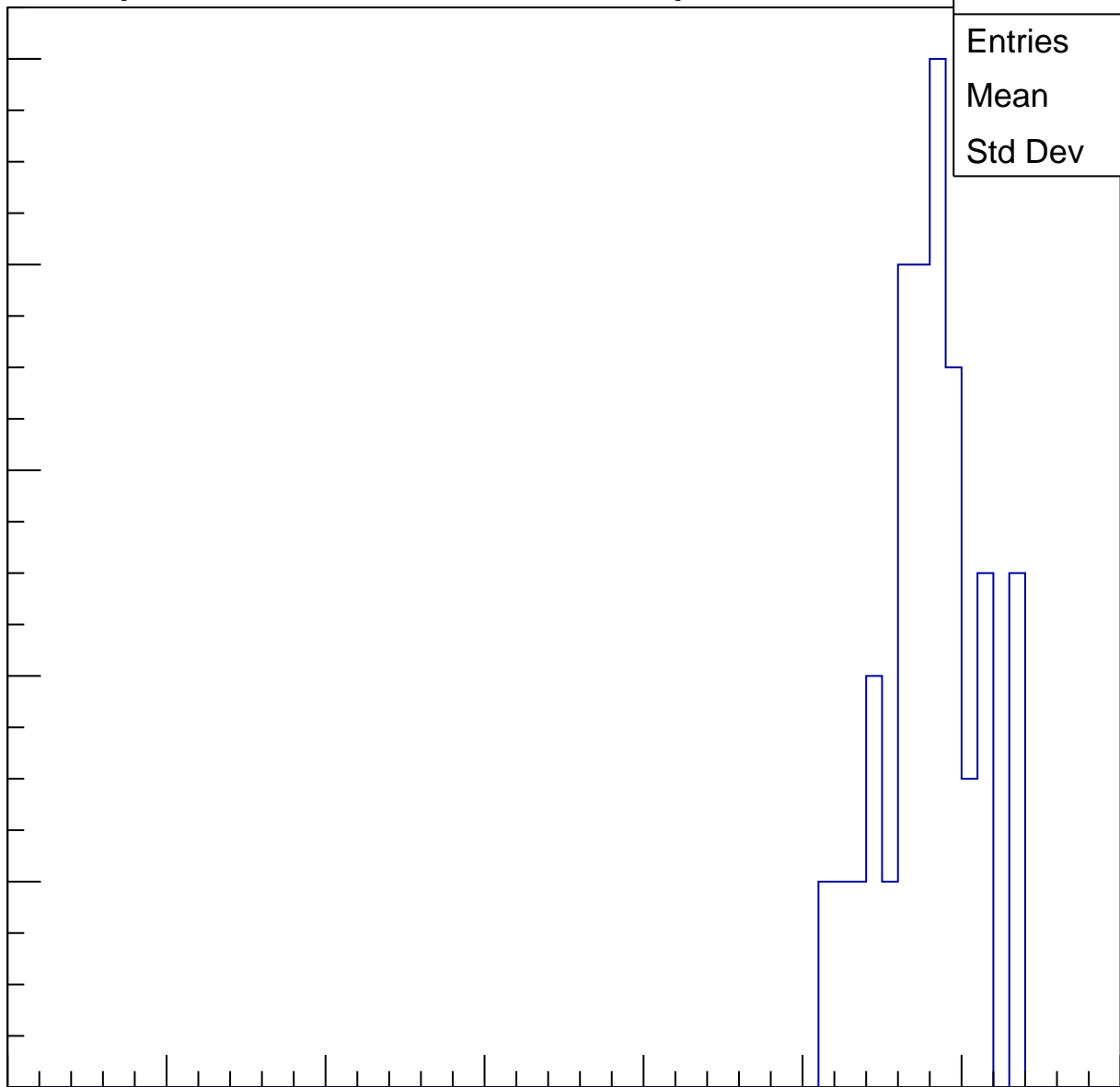
40

50

60

ampl

70

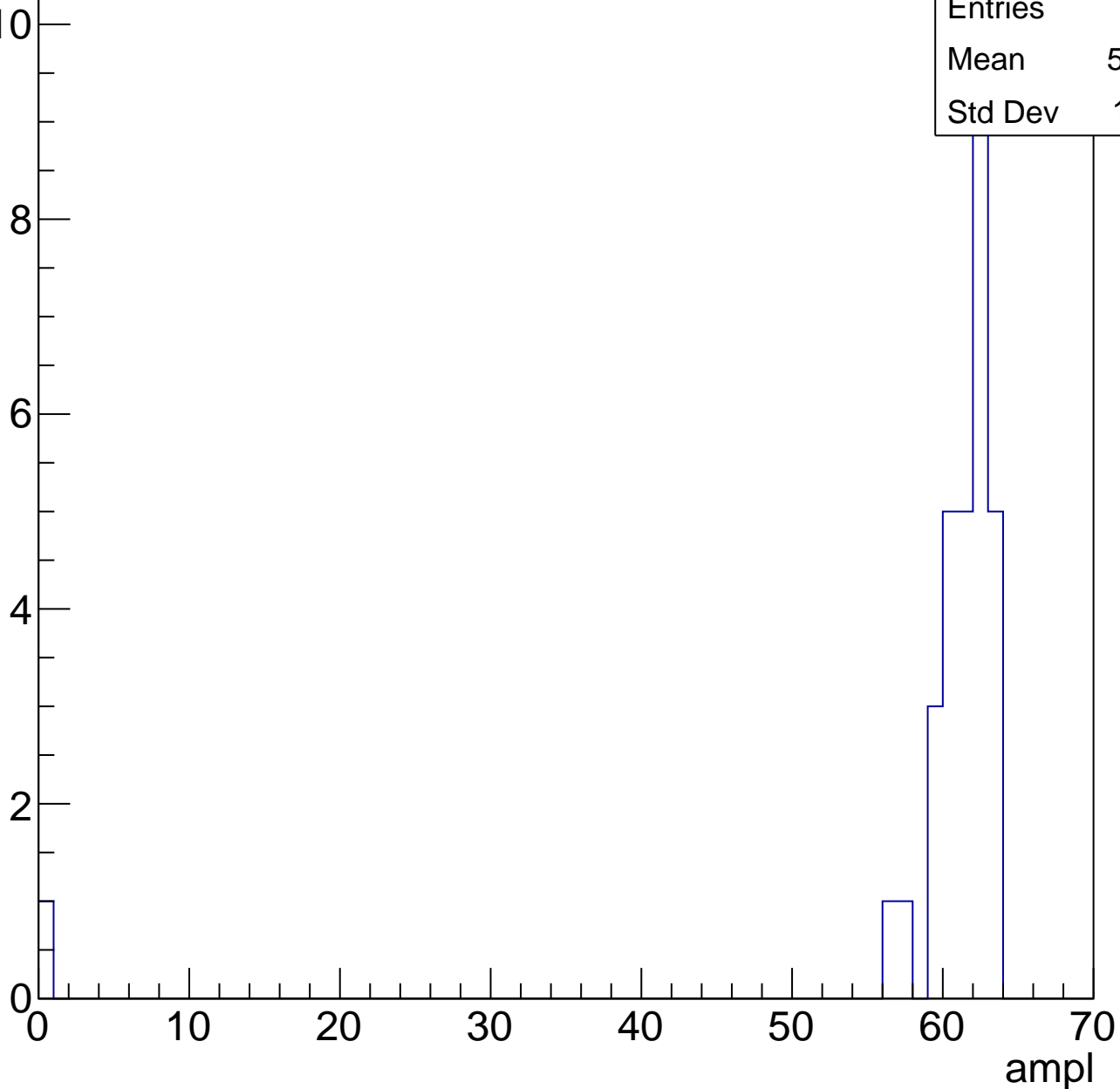


# B1L101S, U16-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	31
Mean	59.03
Std Dev	10.91



# B1L101S, U16-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L101S, U16-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U16-ch110, adc0

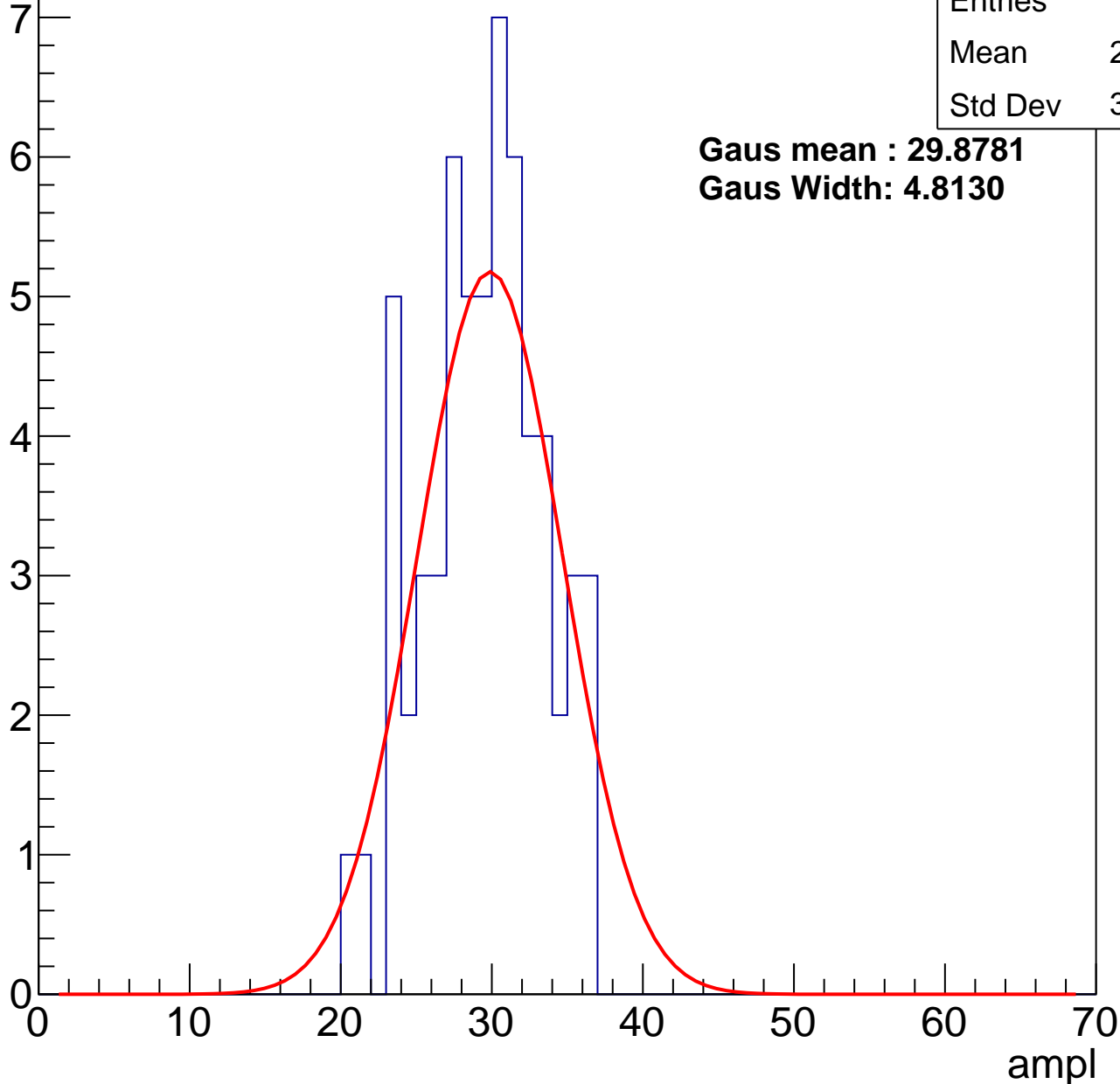
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	29.02
Std Dev	3.905

**Gaus mean : 29.8781**

**Gaus Width: 4.8130**



# B1L101S, U16-ch110, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	80
Mean	36.64
Std Dev	4.047

**Gaus mean : 37.2684**

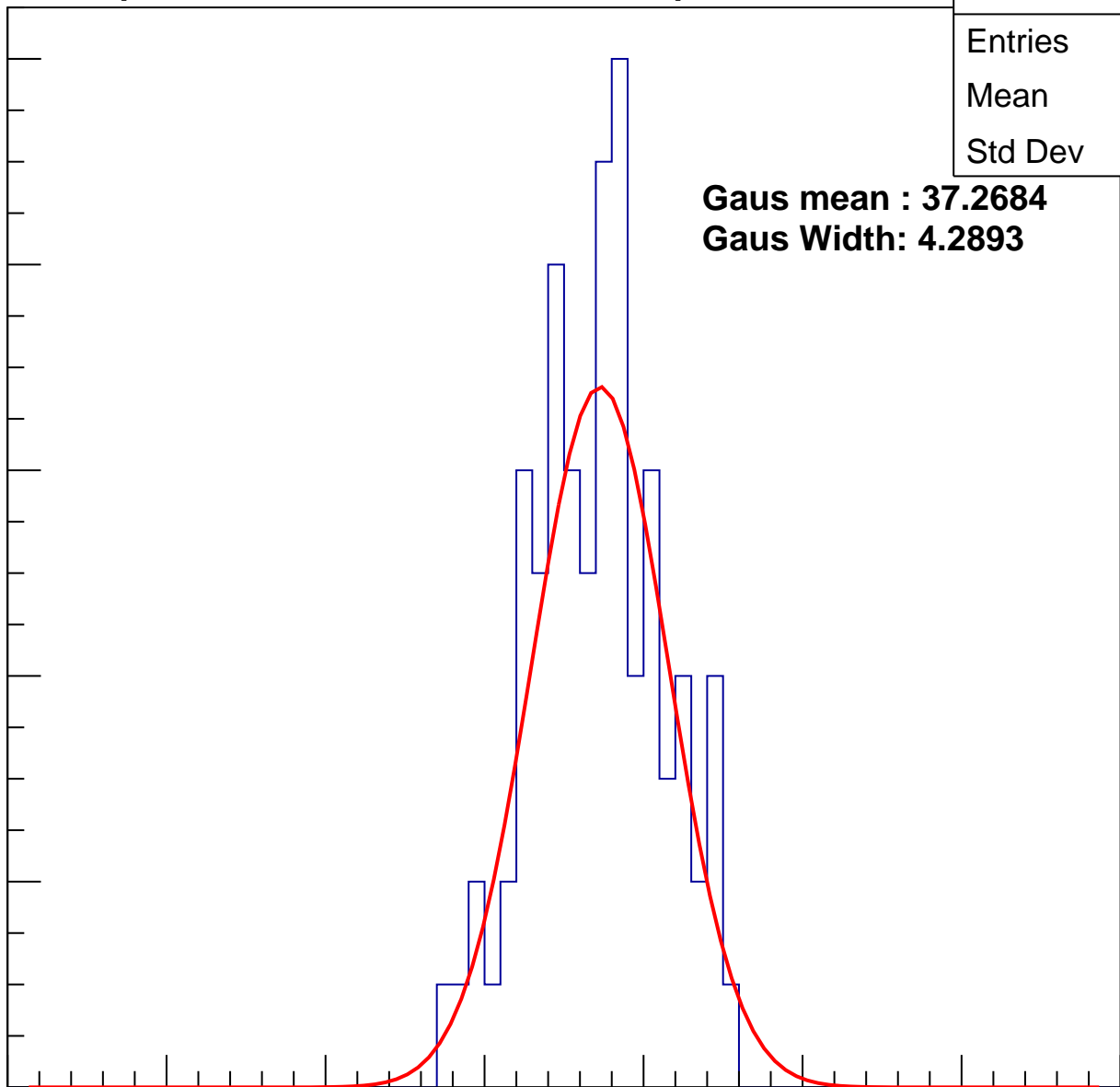
**Gaus Width: 4.2893**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch110, adc2

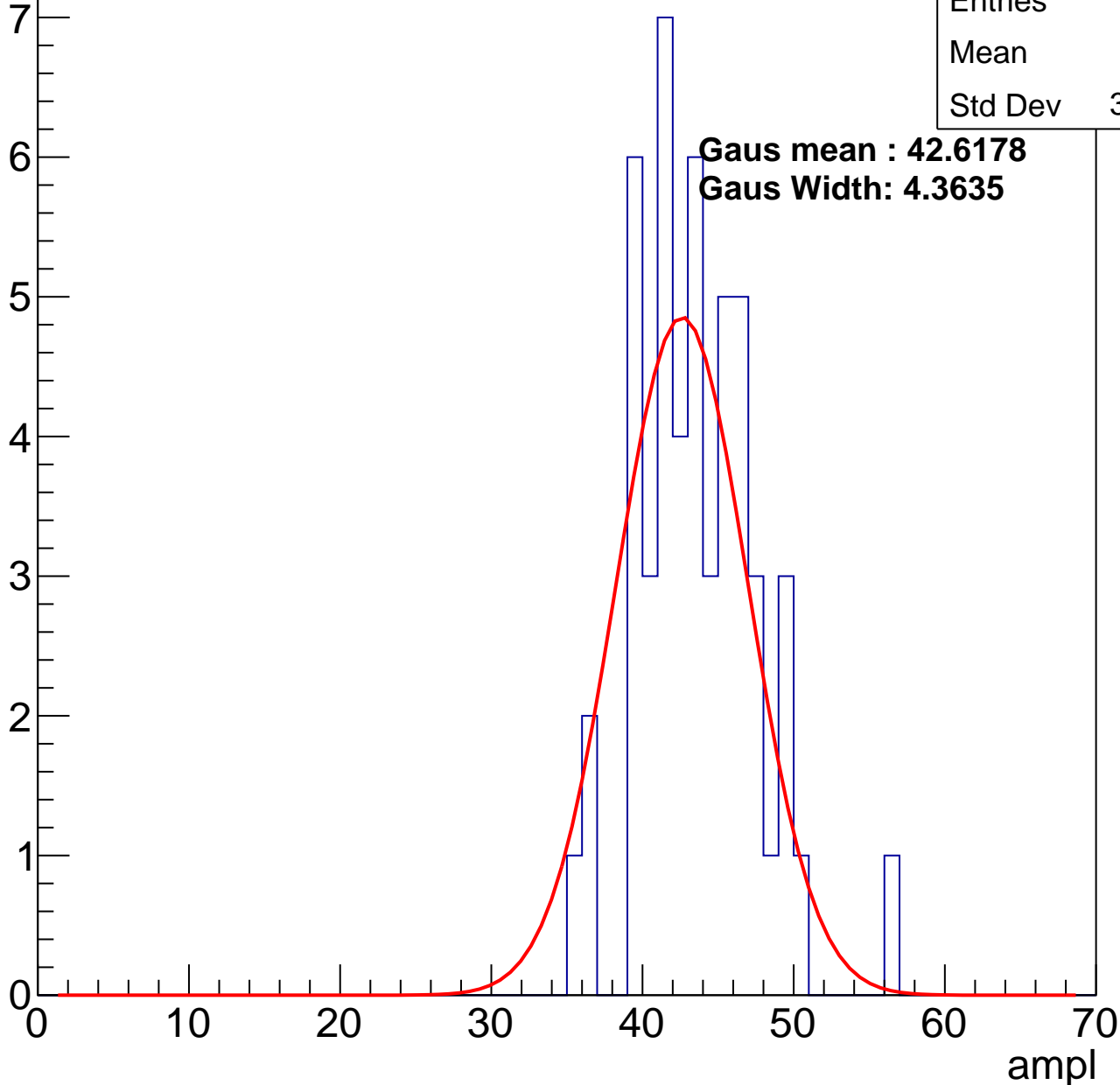
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	43.2
Std Dev	3.916

**Gaus mean : 42.6178**

**Gaus Width: 4.3635**

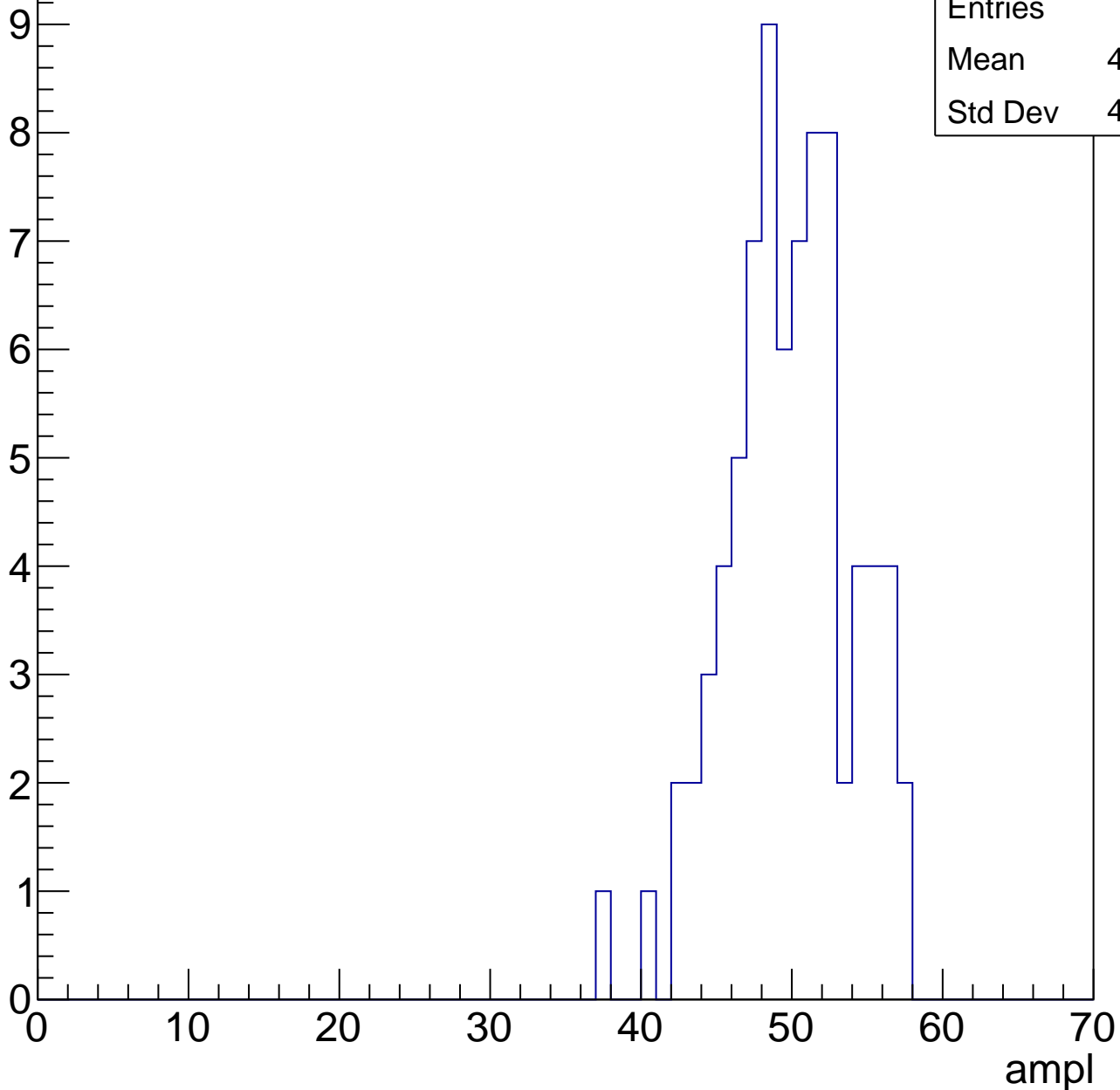


# B1L101S, U16-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

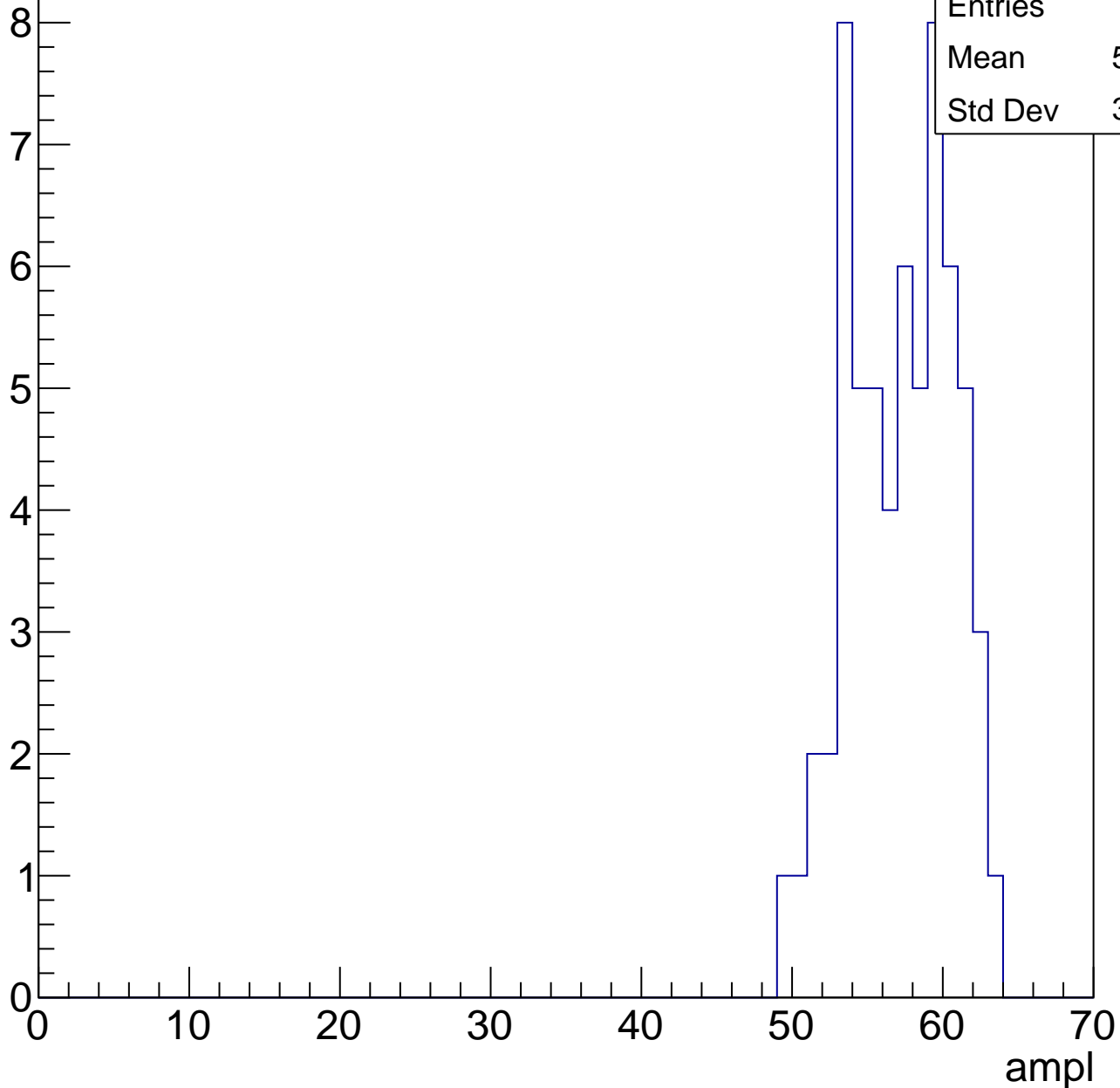
Entries	79
Mean	49.34
Std Dev	4.084



# B1L101S, U16-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



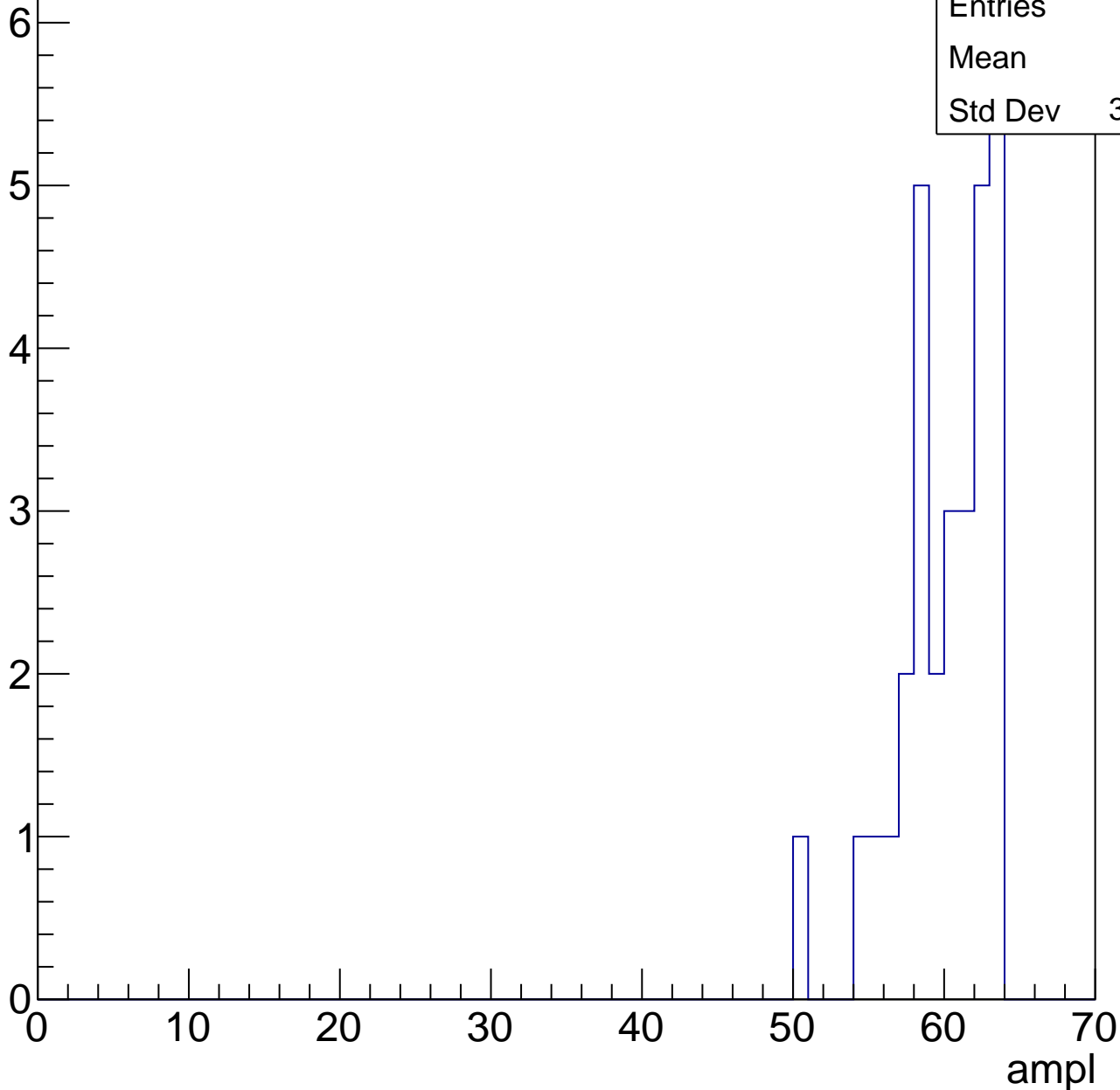
Entries	62
Mean	56.71
Std Dev	3.381

# B1L101S, U16-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

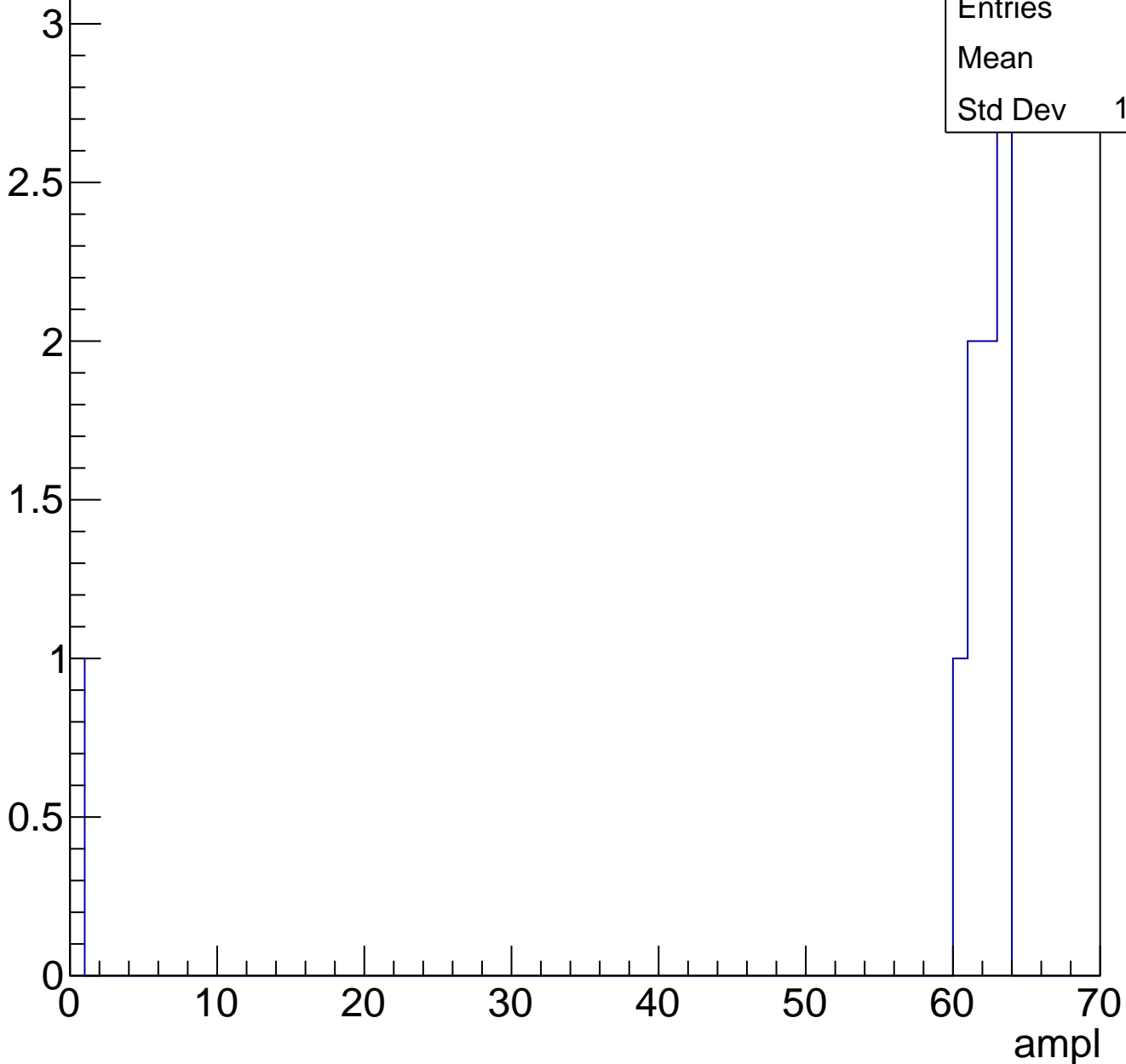
Entries	30
Mean	59.6
Std Dev	3.105



# B1L101S, U16-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch111, adc0

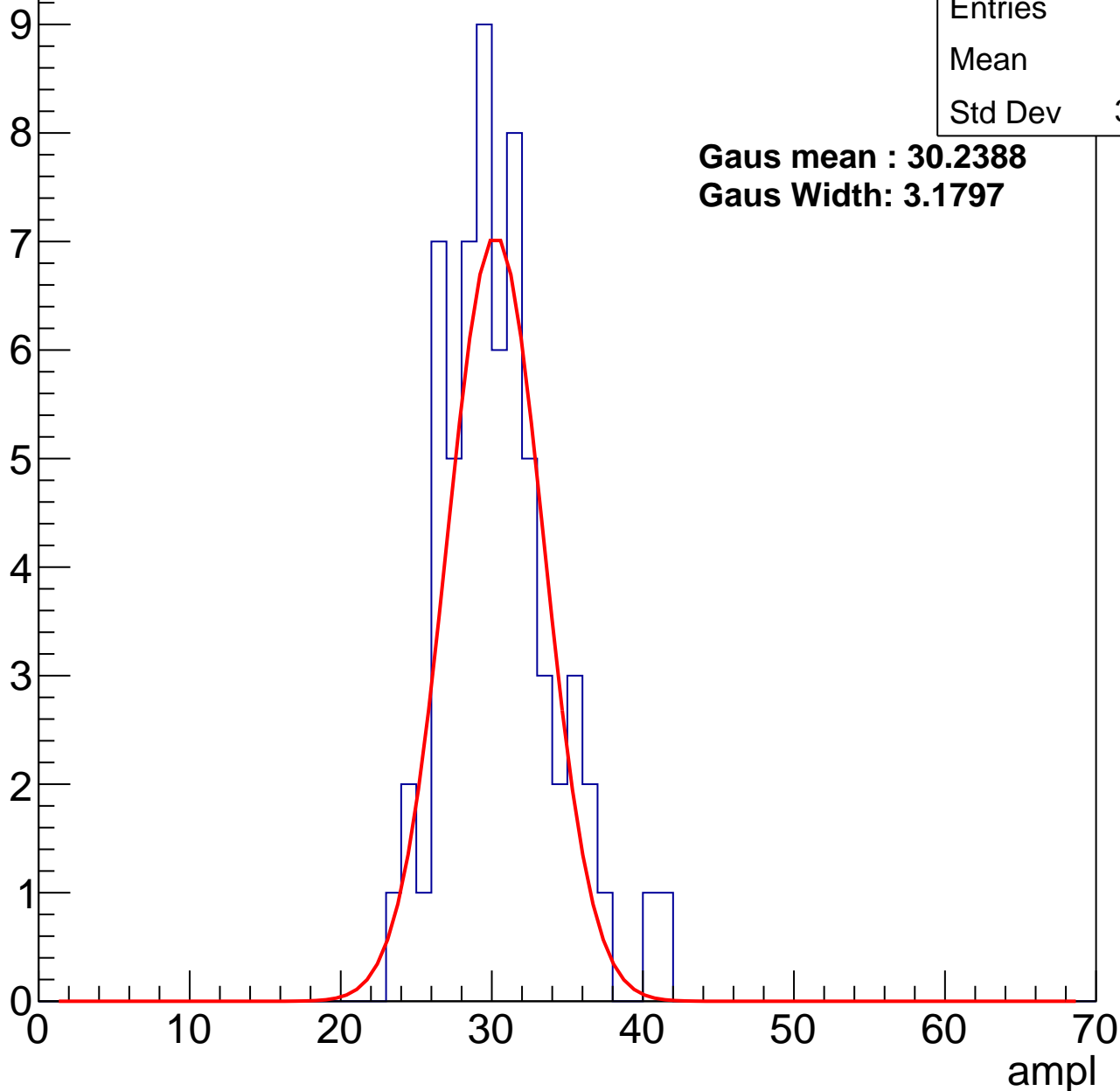
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	30
Std Dev	3.631

**Gaus mean : 30.2388**

**Gaus Width: 3.1797**



# B1L101S, U16-ch111, adc1

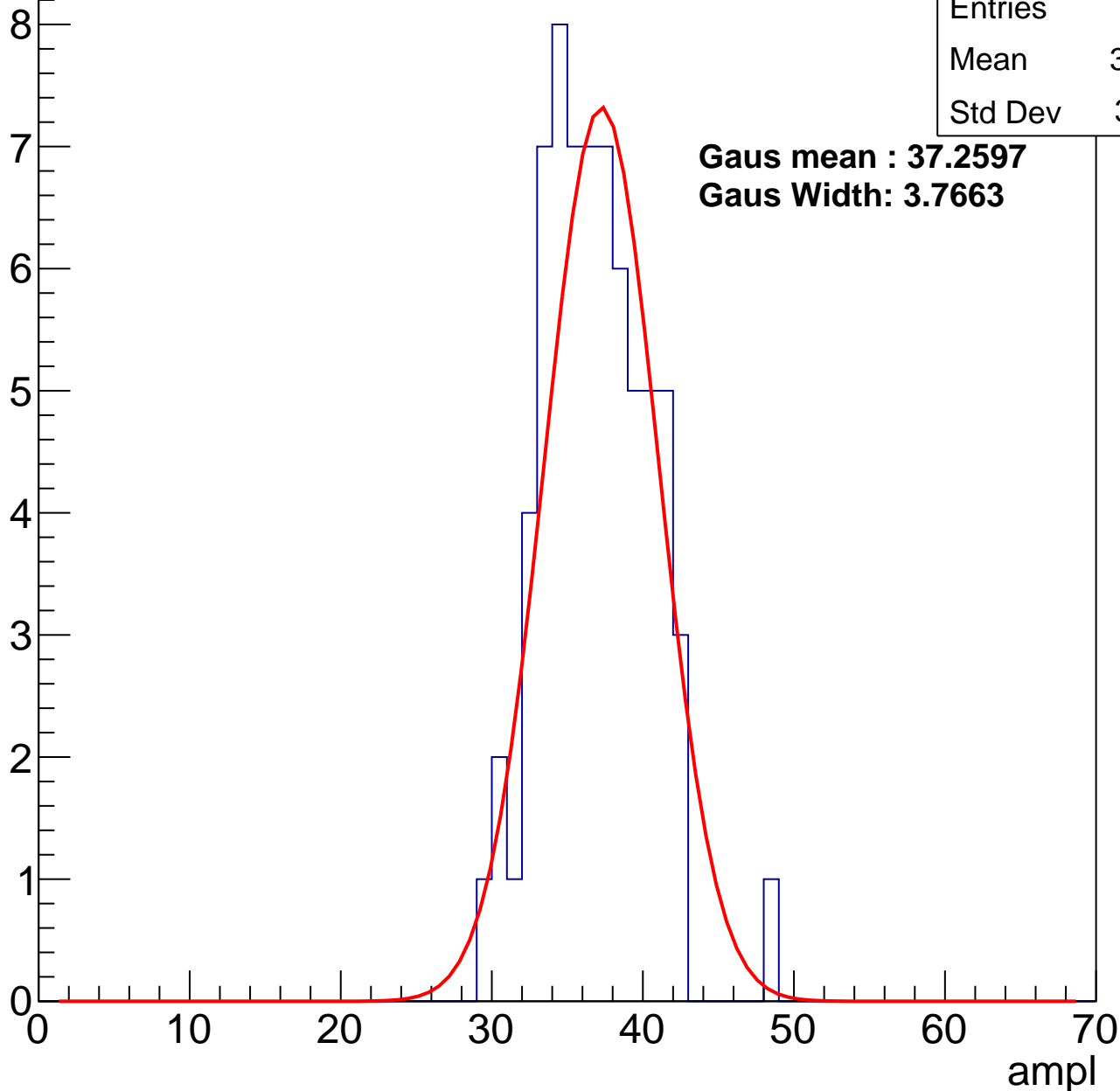
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	36.36
Std Dev	3.481

**Gaus mean : 37.2597**

**Gaus Width: 3.7663**



# B1L101S, U16-ch111, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	78
Mean	43.82
Std Dev	4.141

**Gaus mean : 44.2500**

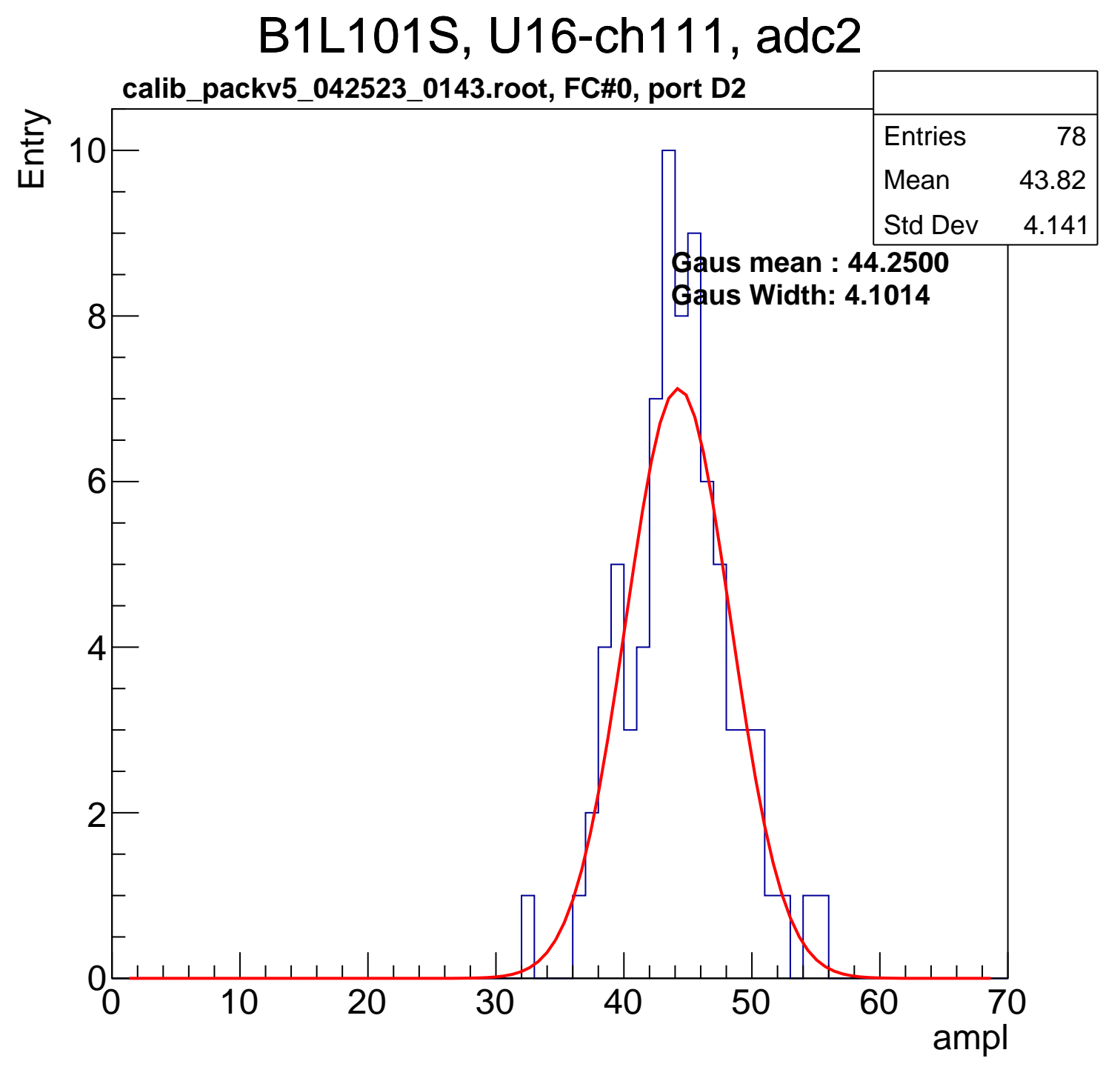
**Gaus Width: 4.1014**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70

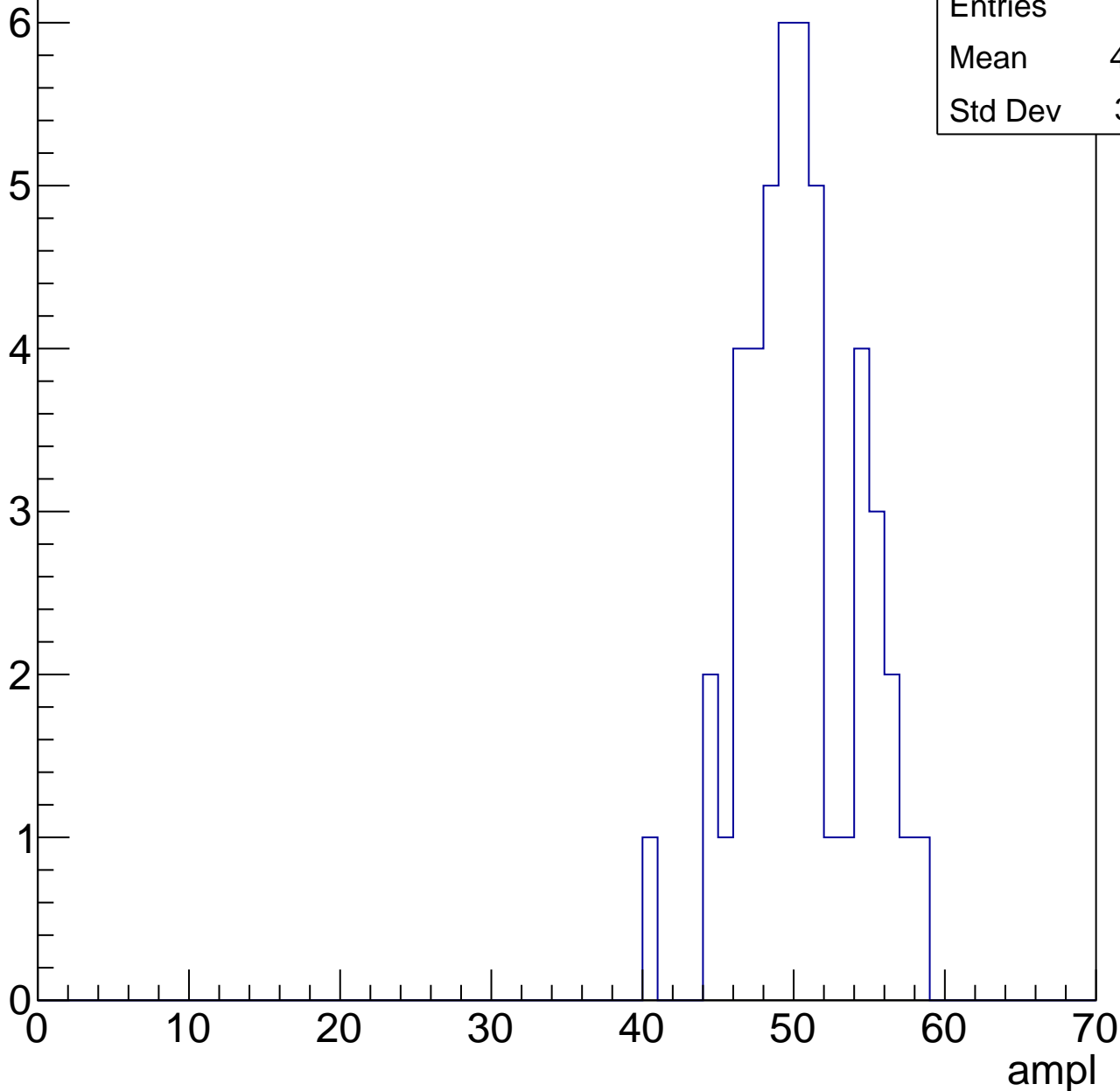


# B1L101S, U16-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	49.94
Std Dev	3.761

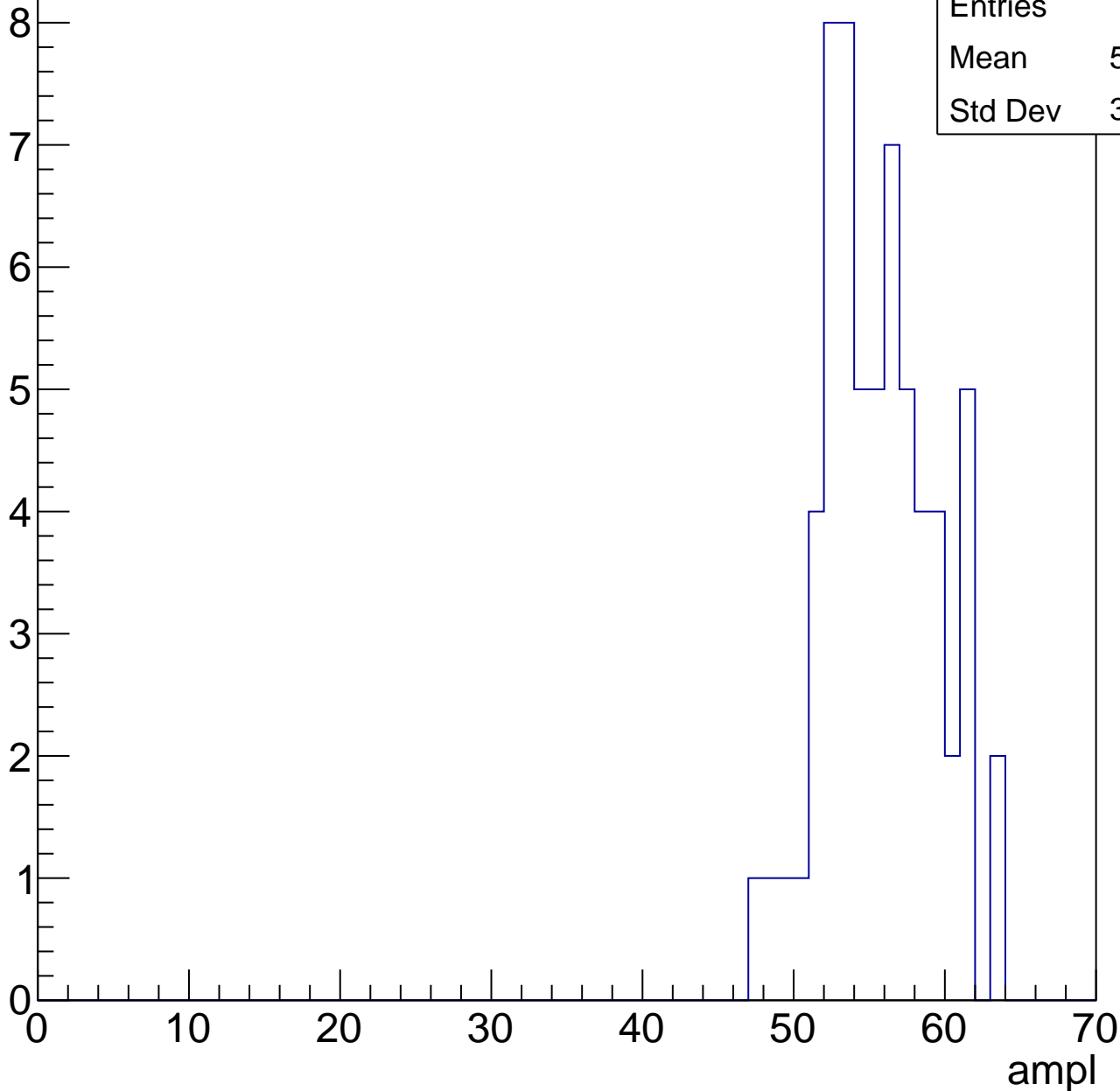


# B1L101S, U16-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	55.22
Std Dev	3.627

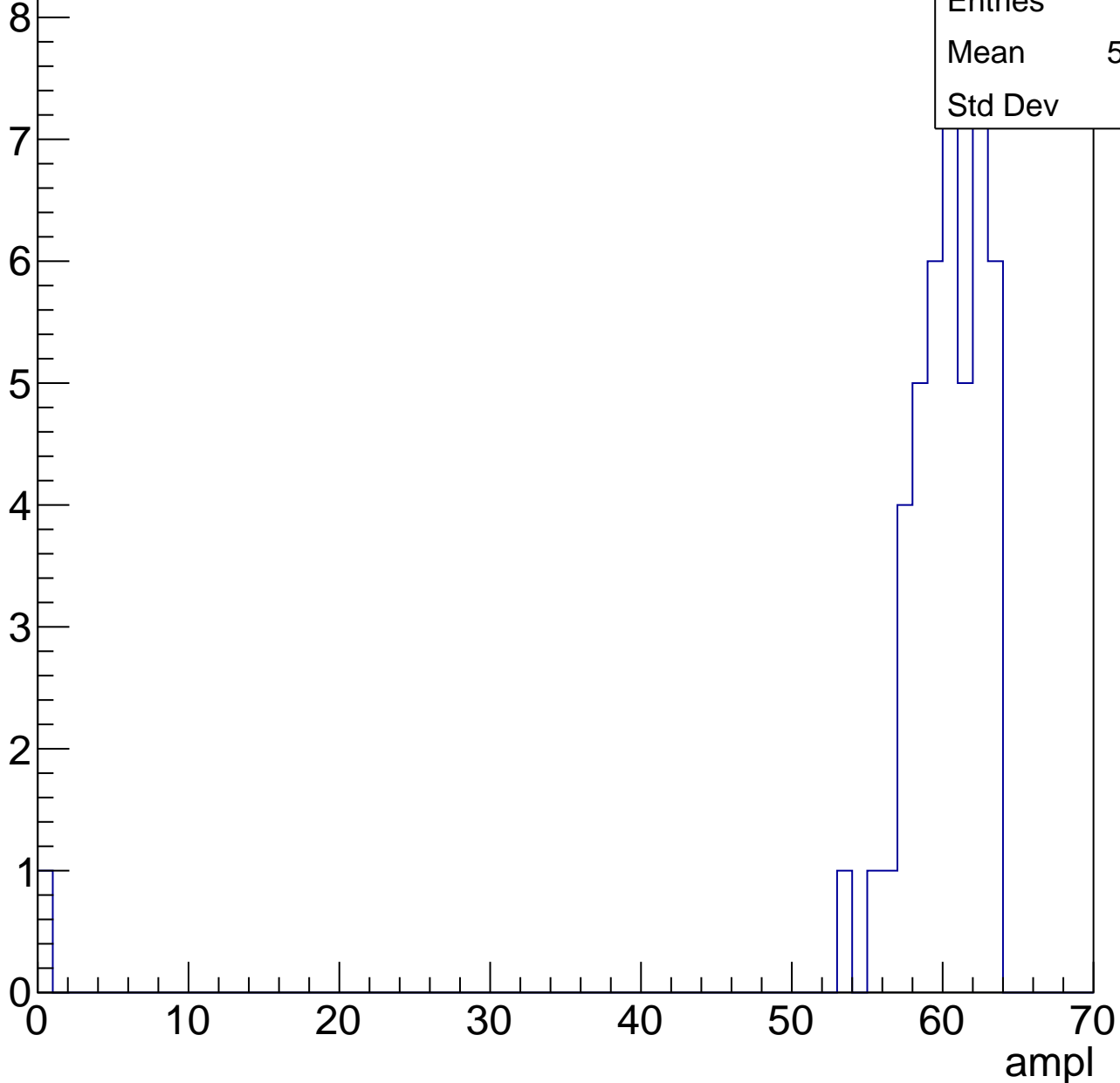


# B1L101S, U16-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	58.59
Std Dev	9.03



# B1L101S, U16-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U16-ch112, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	72
Mean	30.6
Std Dev	4.209

**Gaus mean : 31.4153**

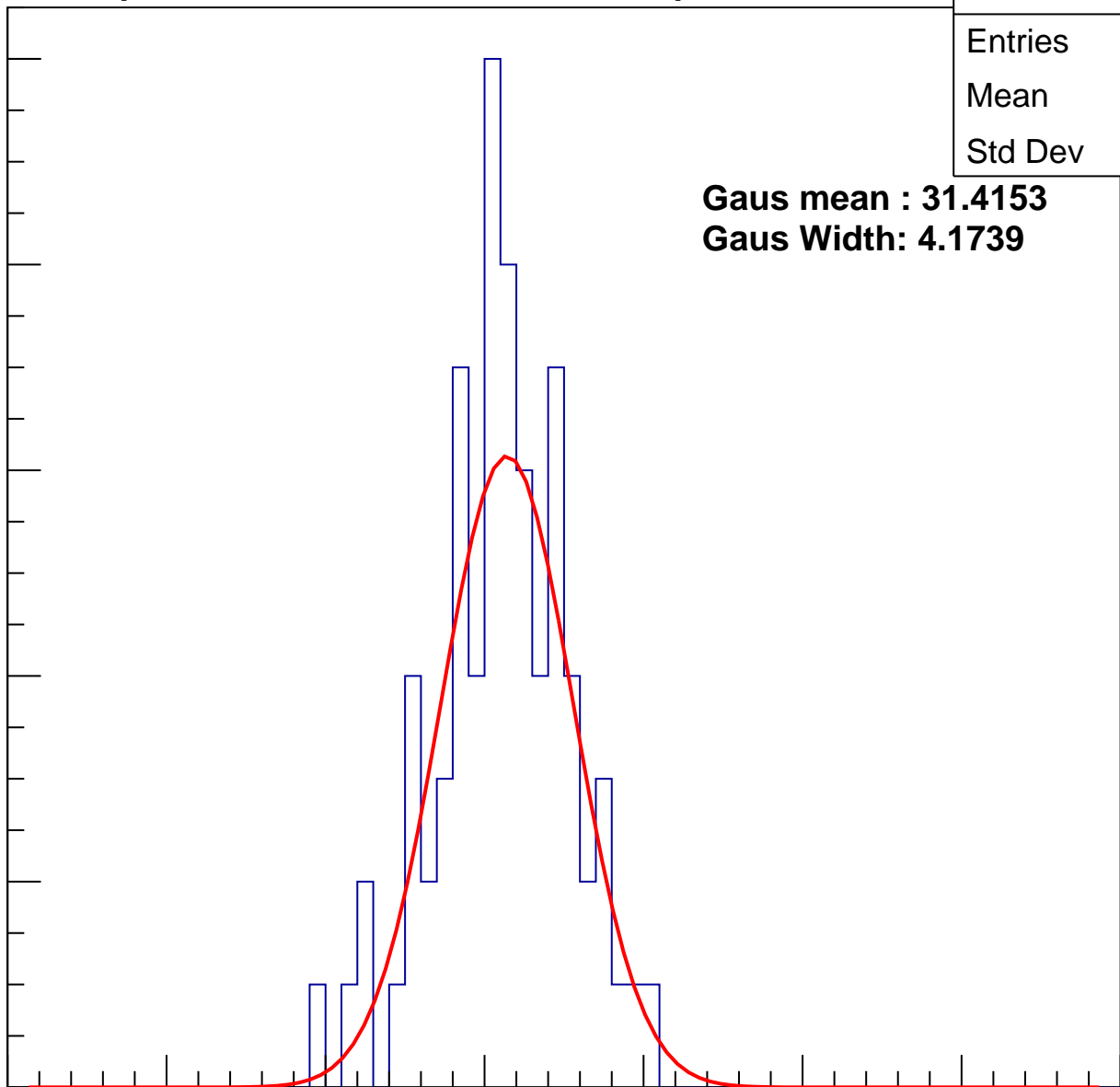
**Gaus Width: 4.1739**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch112, adc1

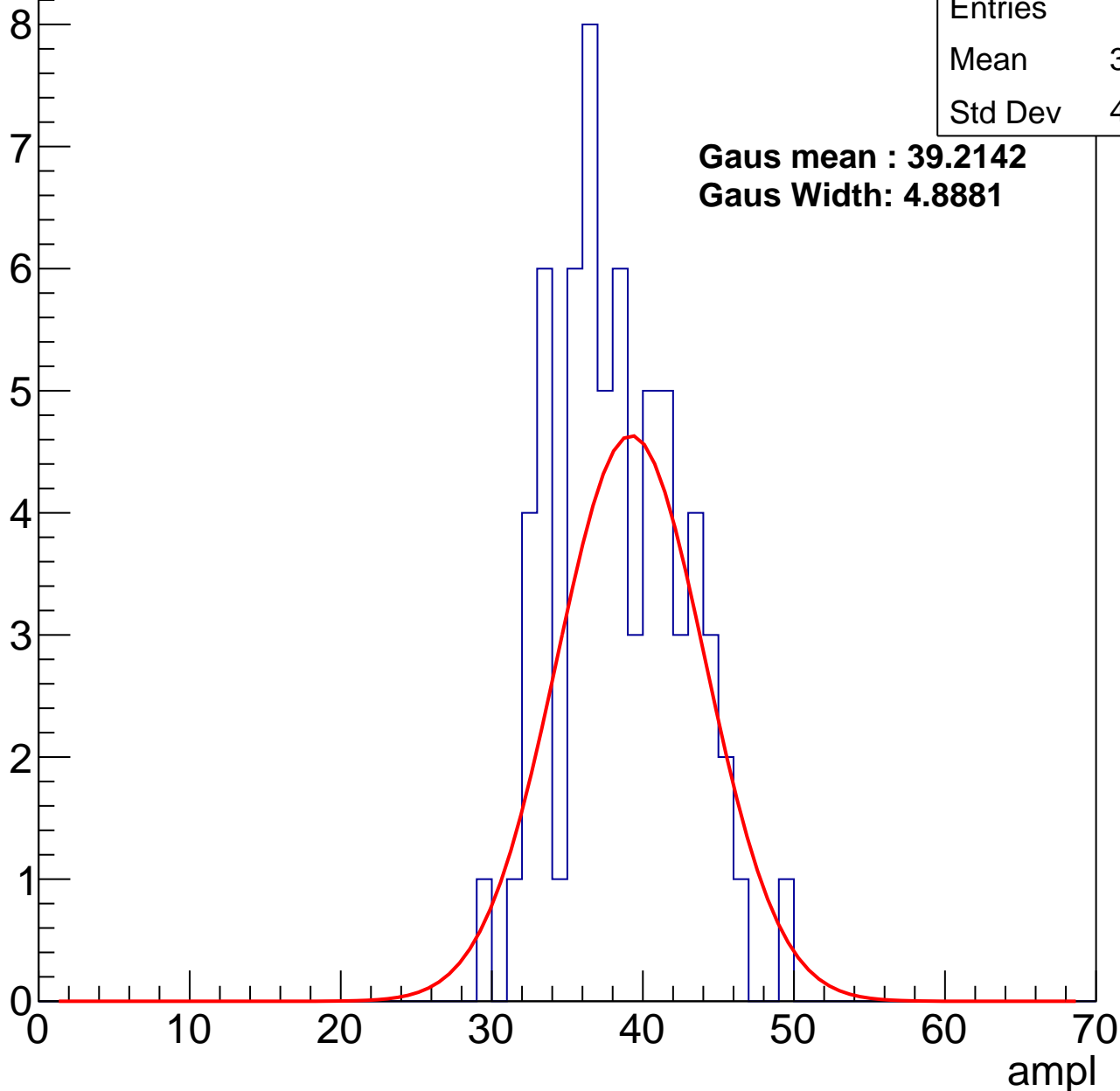
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	37.97
Std Dev	4.184

**Gaus mean : 39.2142**

**Gaus Width: 4.8881**



# B1L101S, U16-ch112, adc2

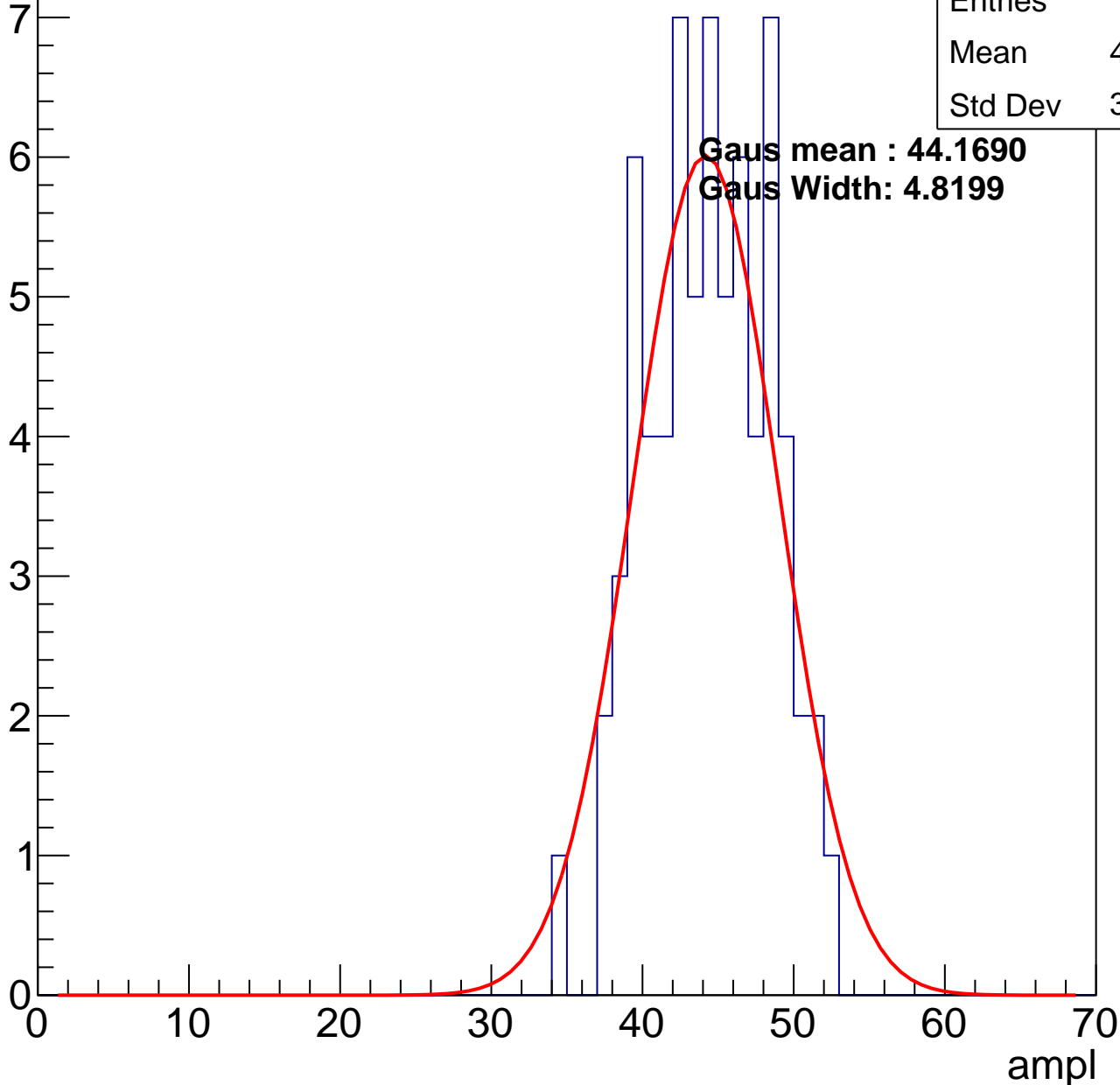
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	43.89
Std Dev	3.962

**Gaus mean : 44.1690**

**Gaus Width: 4.8199**

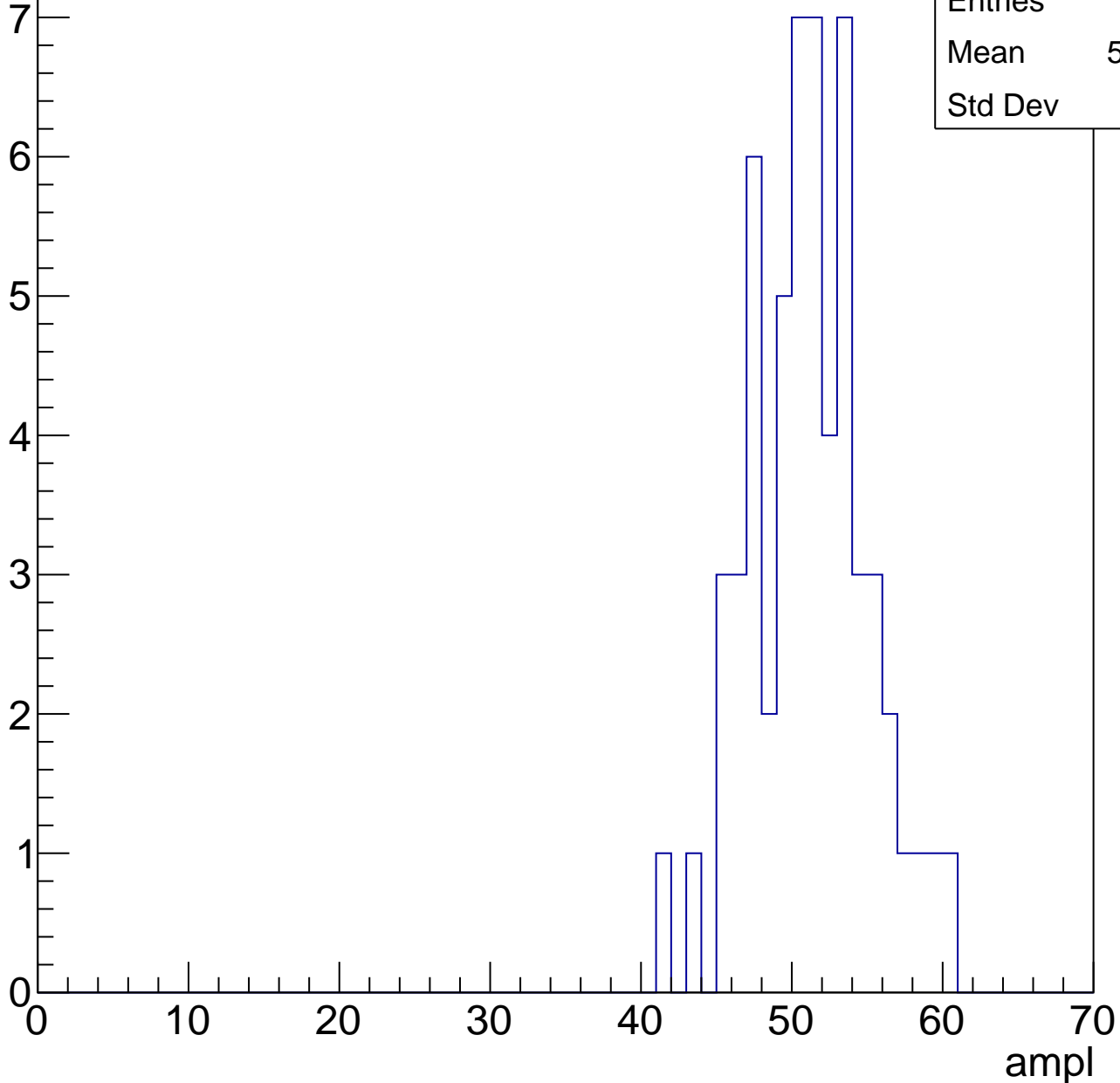


# B1L101S, U16-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	50.67
Std Dev	3.87

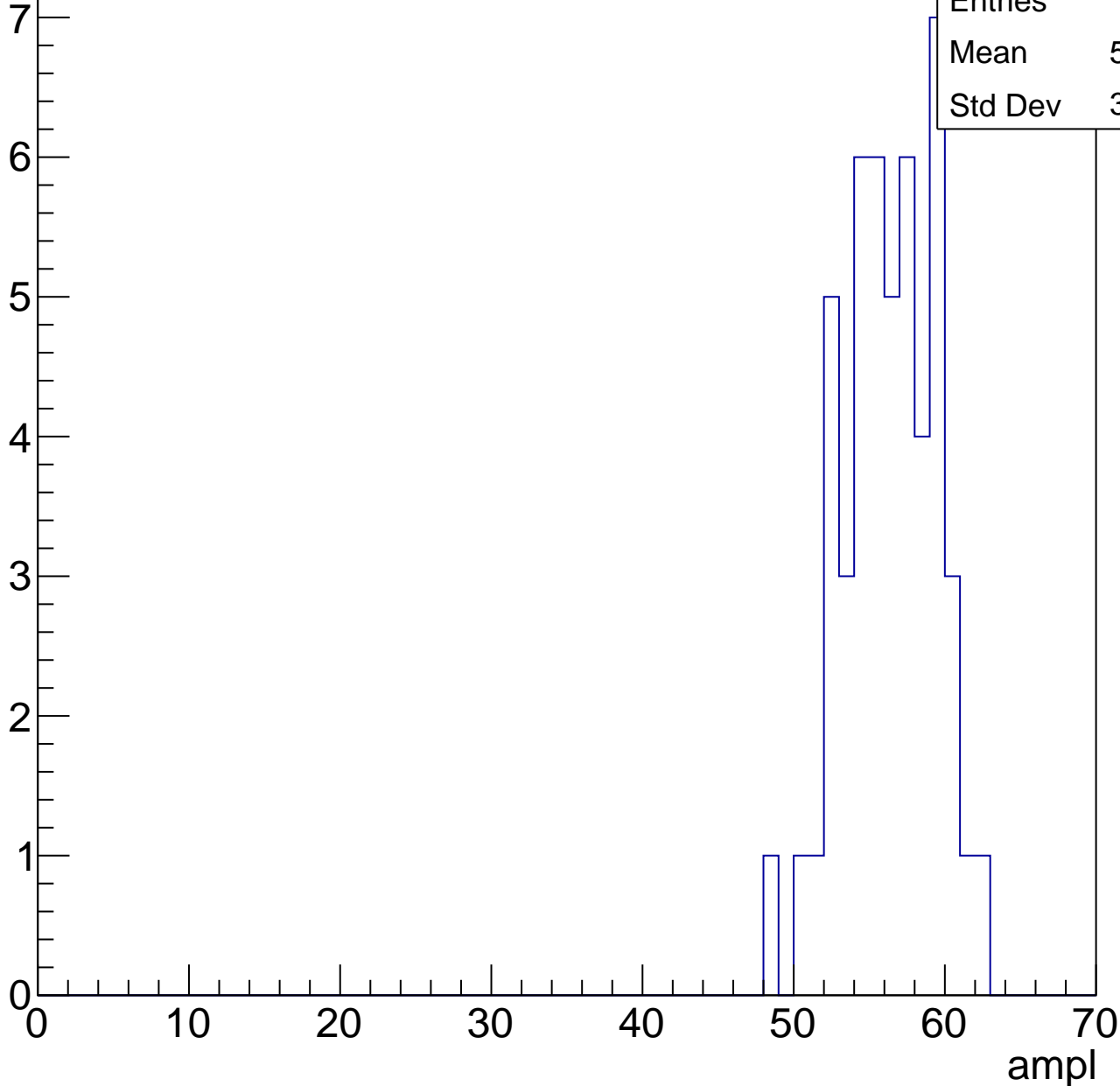


# B1L101S, U16-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	55.84
Std Dev	3.016

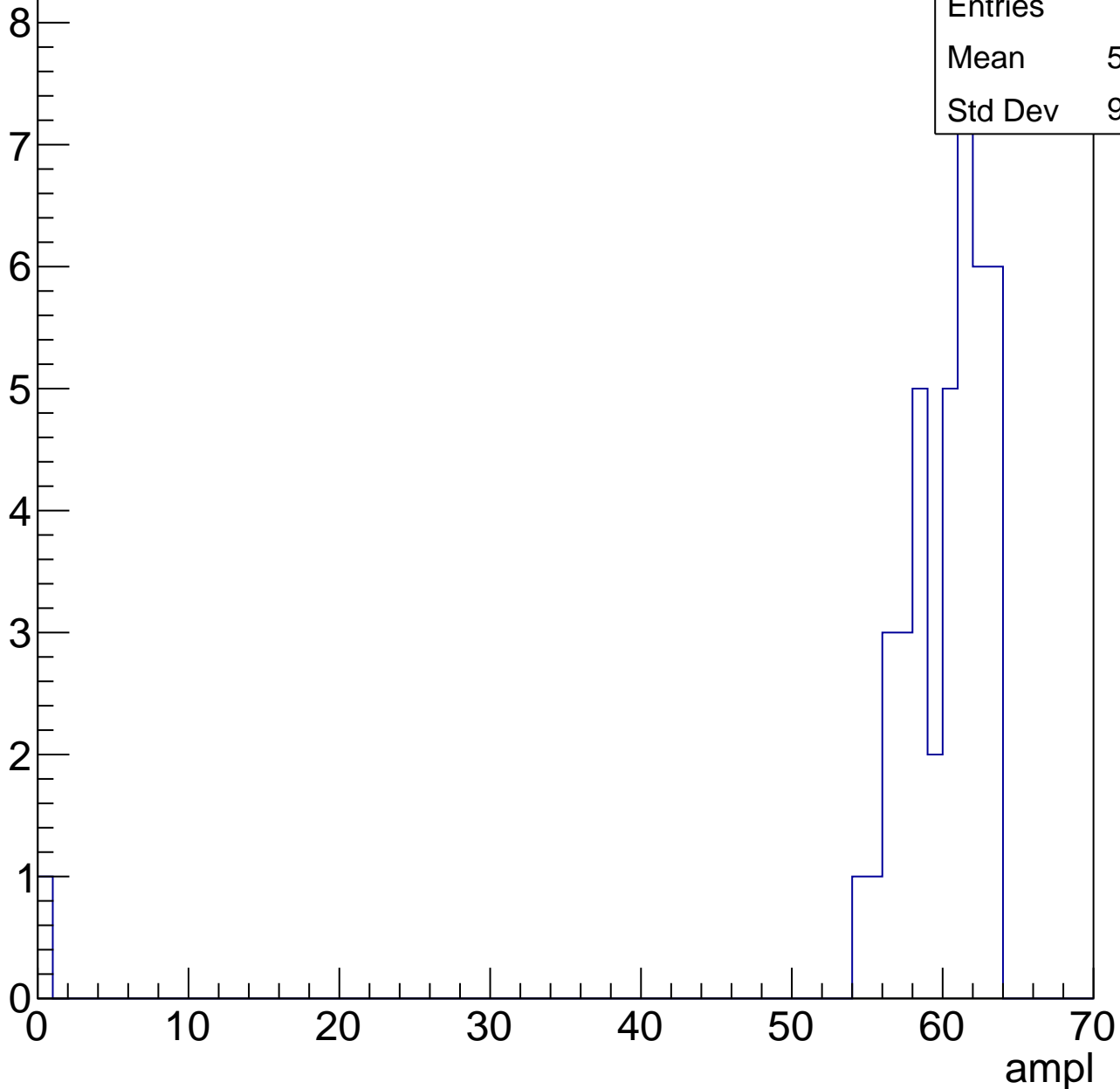


# B1L101S, U16-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	41
Mean	58.39
Std Dev	9.548



# B1L101S, U16-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch113, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	66
Mean	30.59
Std Dev	3.233

**Gaus mean : 31.6133**

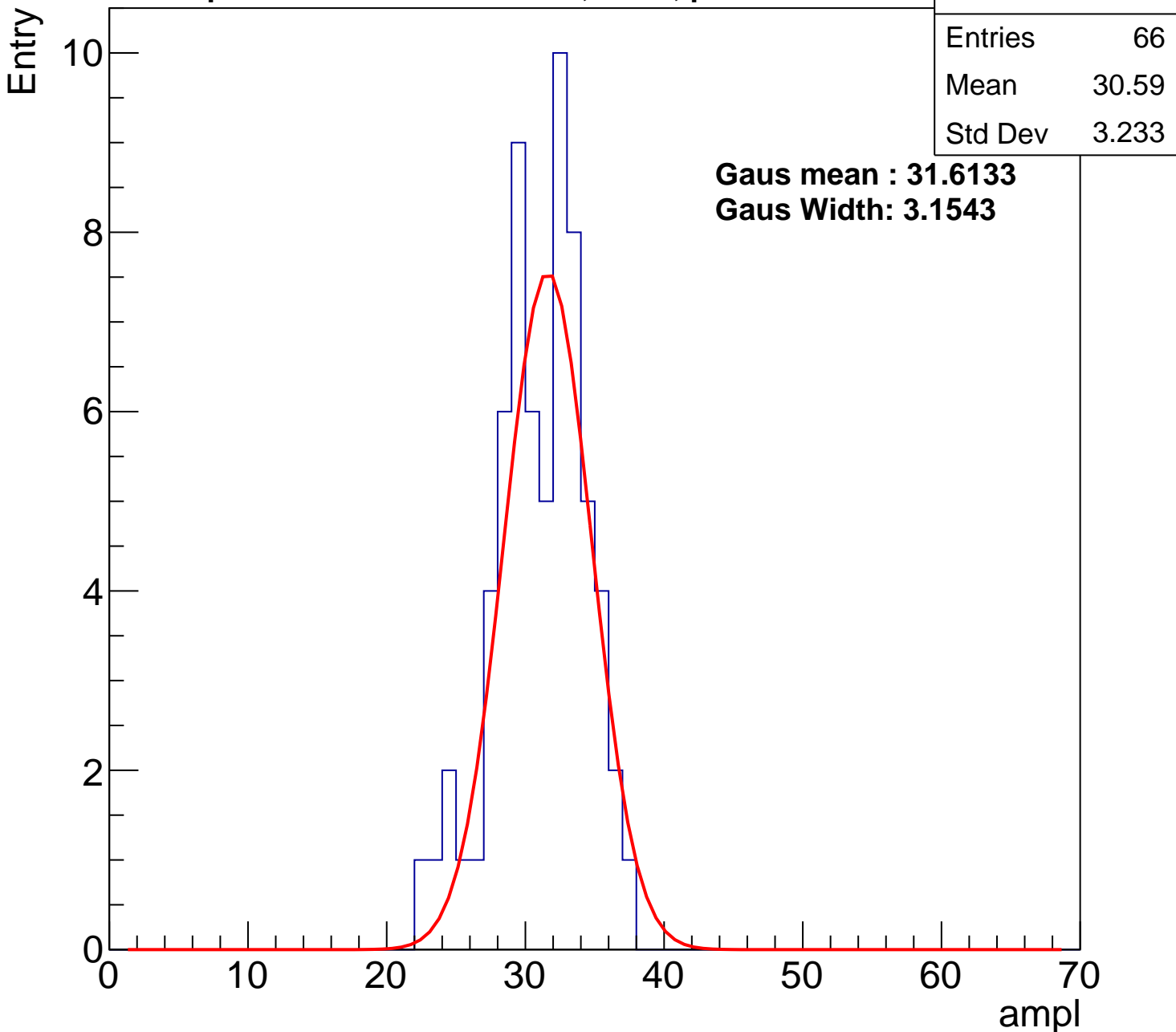
**Gaus Width: 3.1543**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch113, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	89
Mean	38.21
Std Dev	3.876

**Gaus mean : 38.4053**

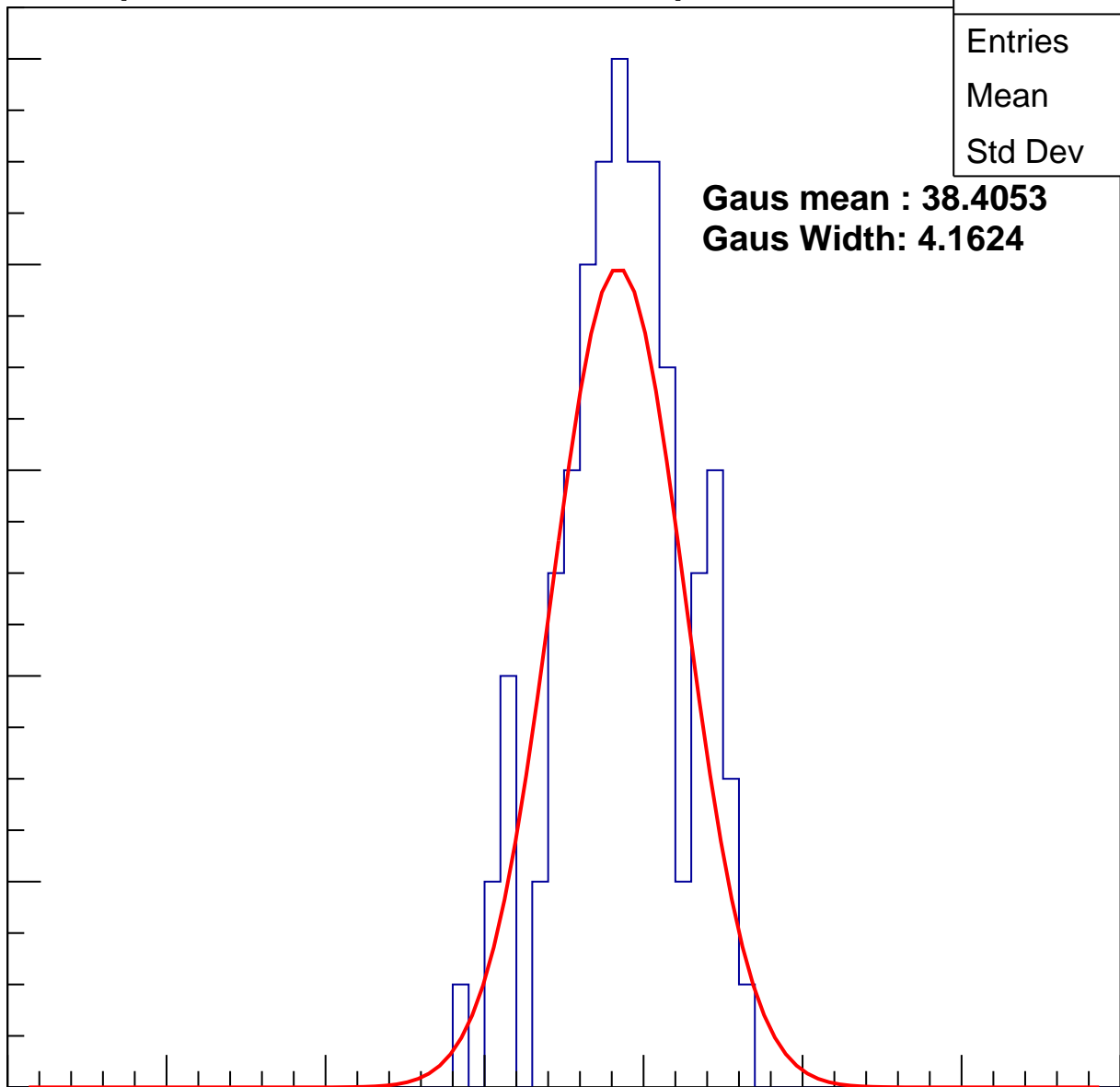
**Gaus Width: 4.1624**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch113, adc2

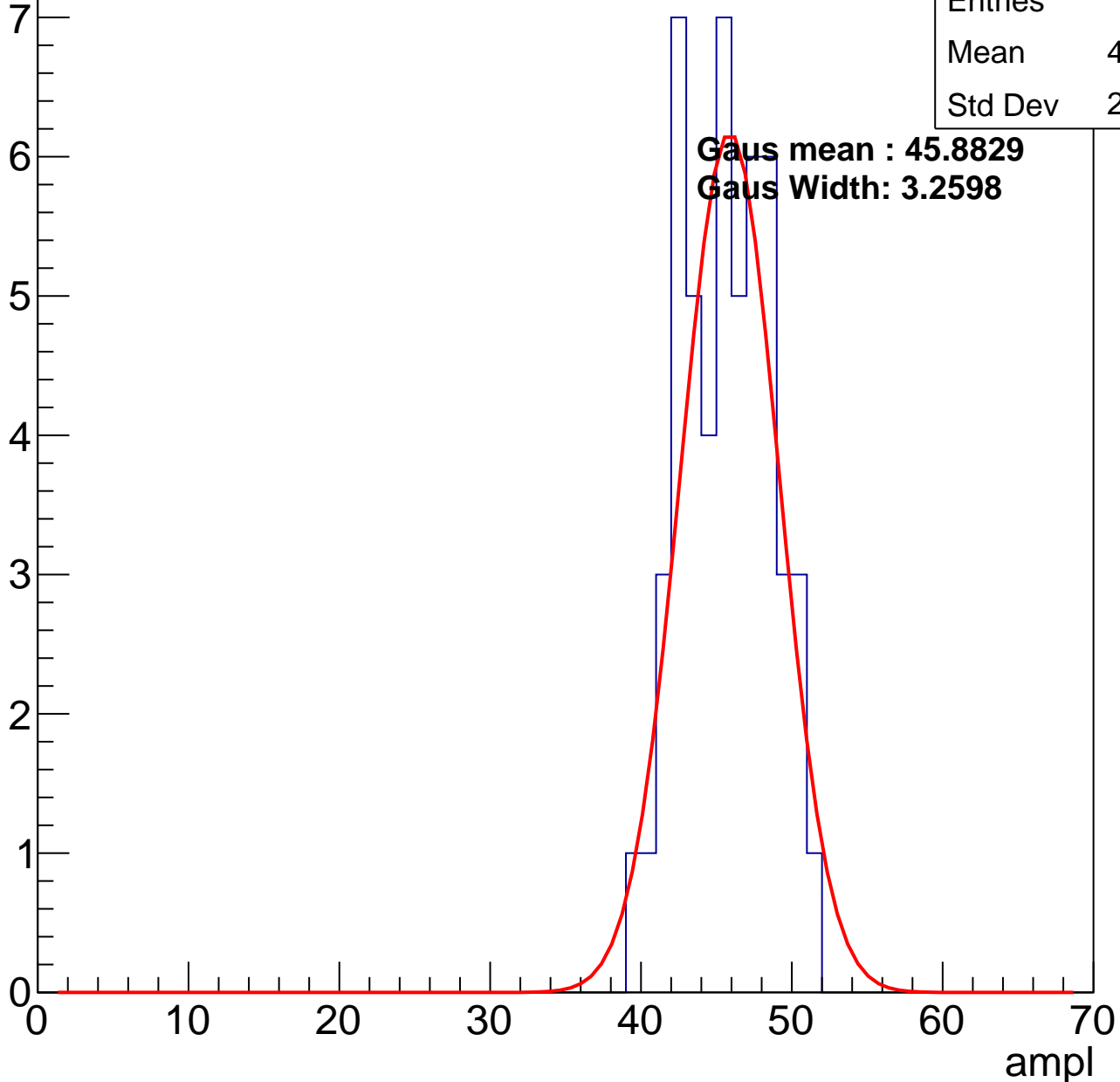
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	45.19
Std Dev	2.896

**Gaus mean : 45.8829**

**Gaus Width: 3.2598**

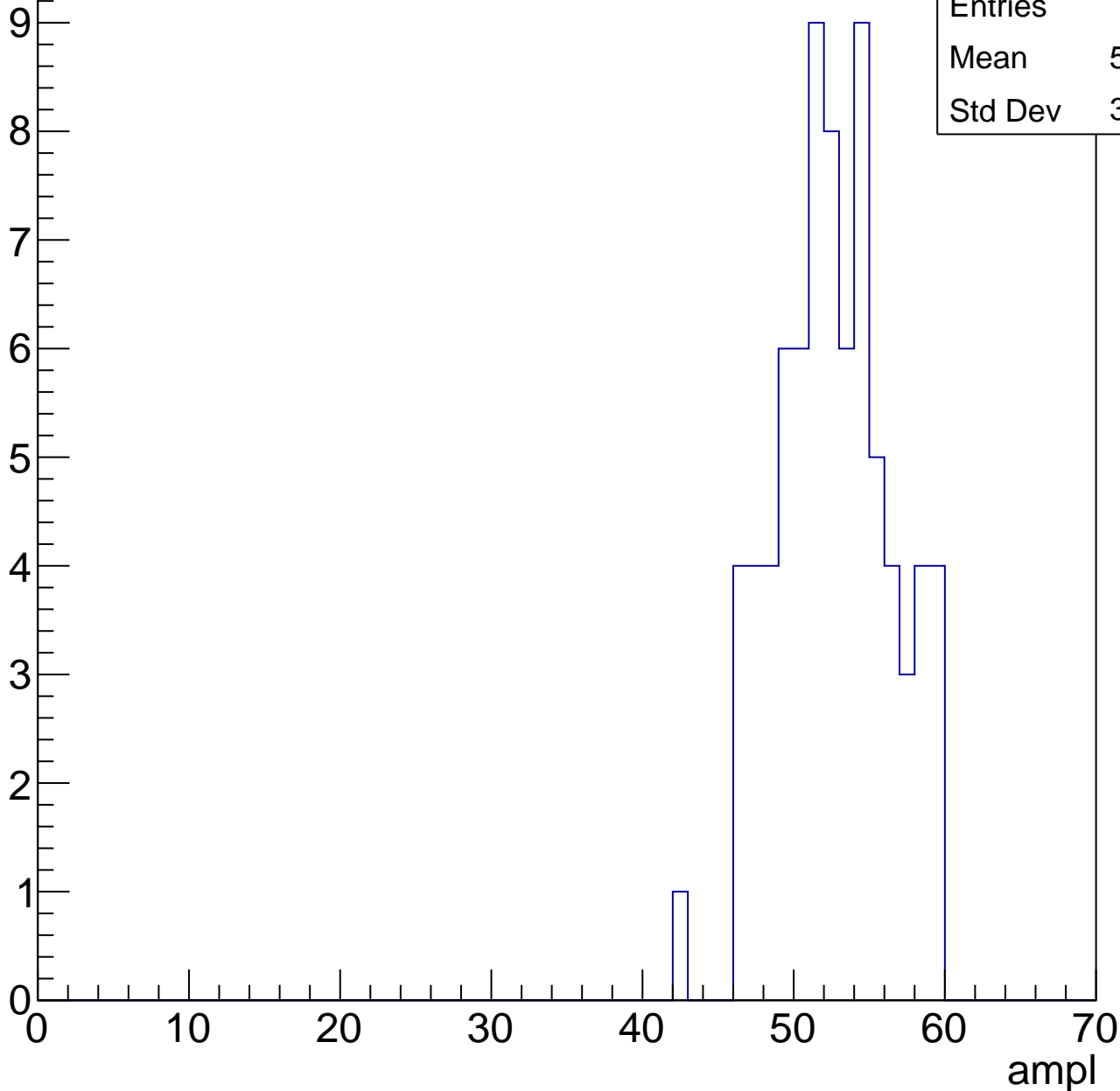


# B1L101S, U16-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	52.17
Std Dev	3.708

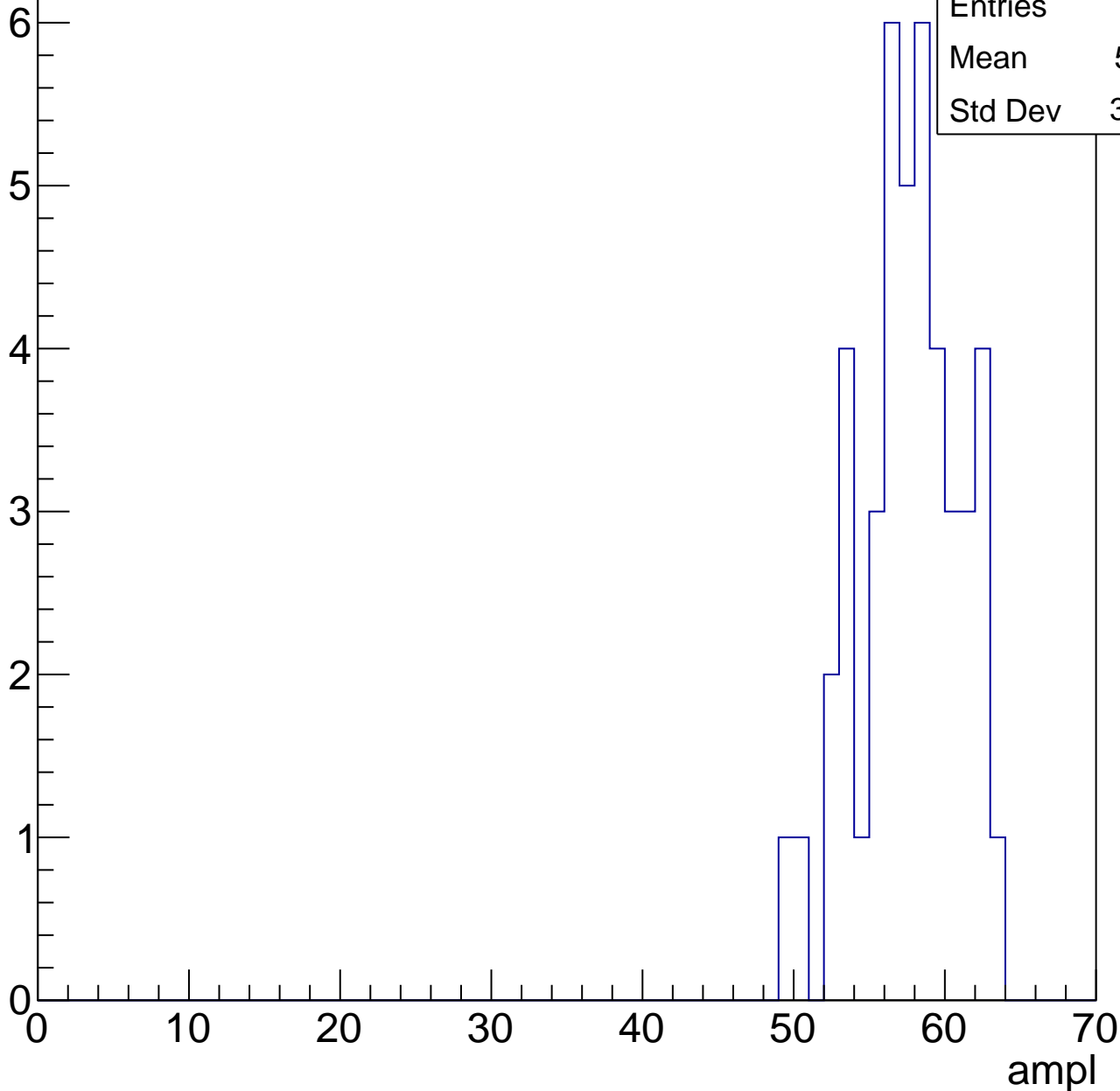


# B1L101S, U16-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	44
Mean	57.11
Std Dev	3.325

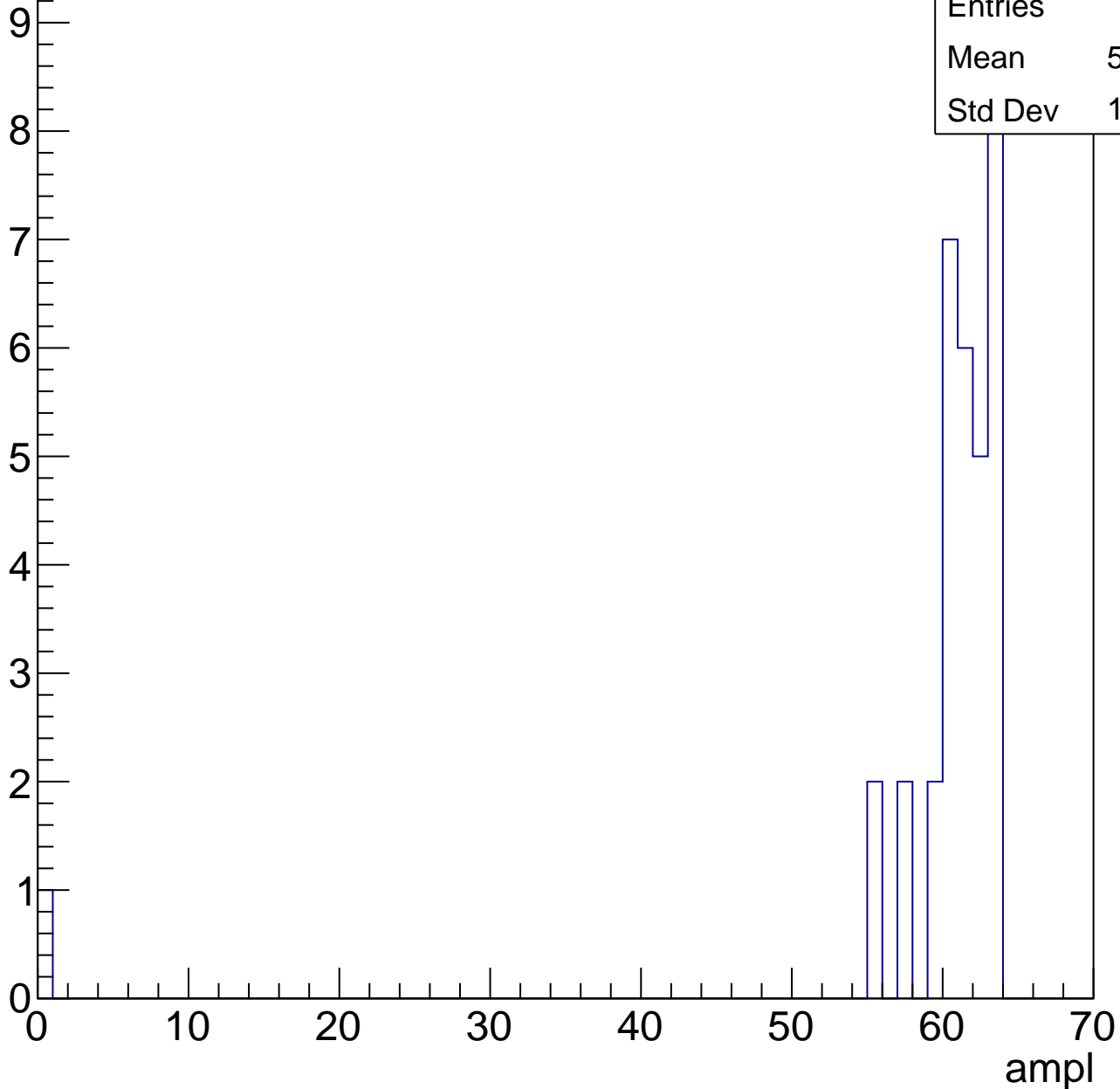


# B1L101S, U16-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	34
Mean	58.97
Std Dev	10.49



# B1L101S, U16-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U16-ch114, adc0

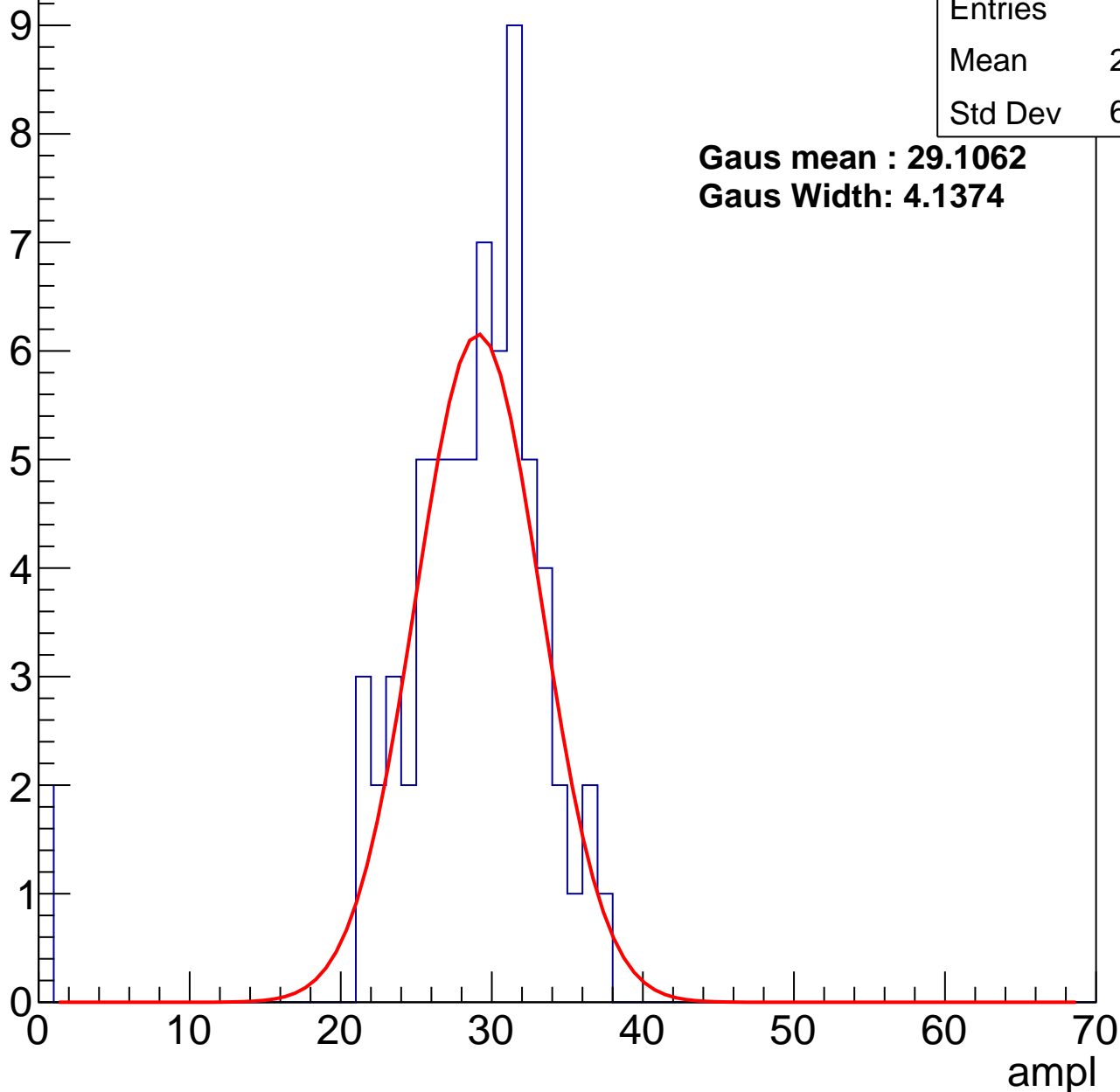
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	27.83
Std Dev	6.119

**Gaus mean : 29.1062**

**Gaus Width: 4.1374**



# B1L101S, U16-ch114, adc1

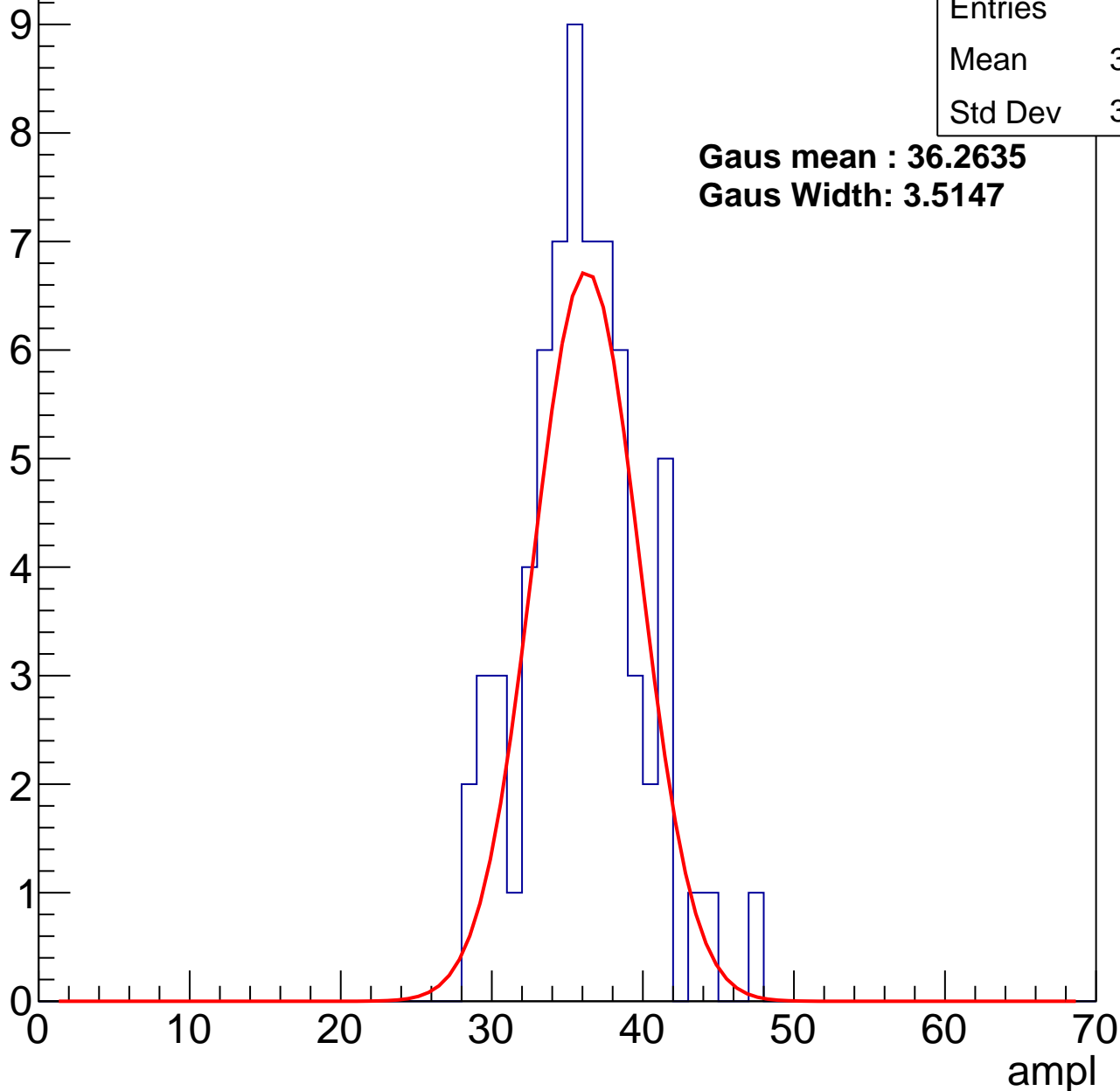
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	35.56
Std Dev	3.832

**Gaus mean : 36.2635**

**Gaus Width: 3.5147**



# B1L101S, U16-ch114, adc2

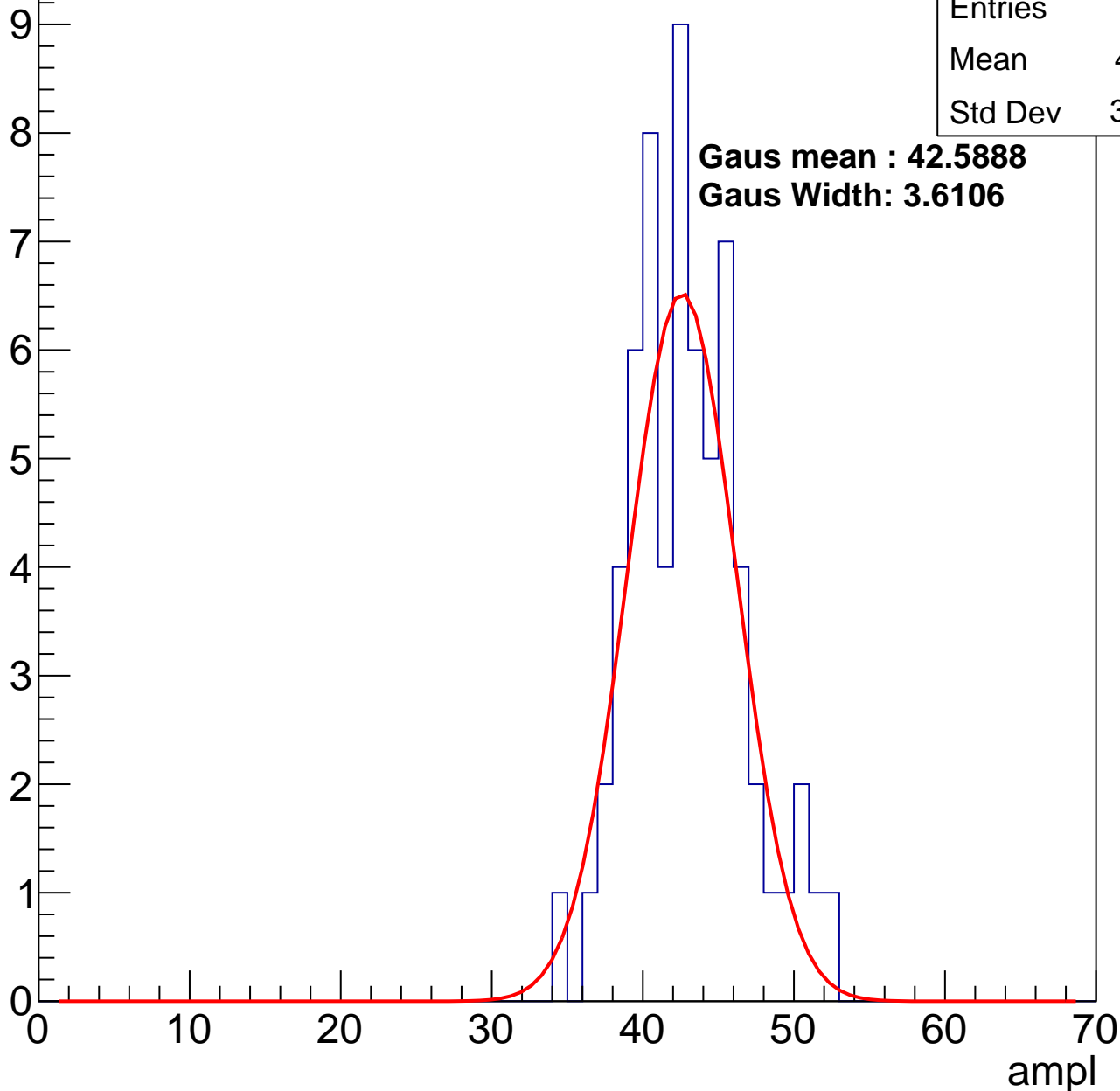
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	42.51
Std Dev	3.688

**Gaus mean : 42.5888**

**Gaus Width: 3.6106**

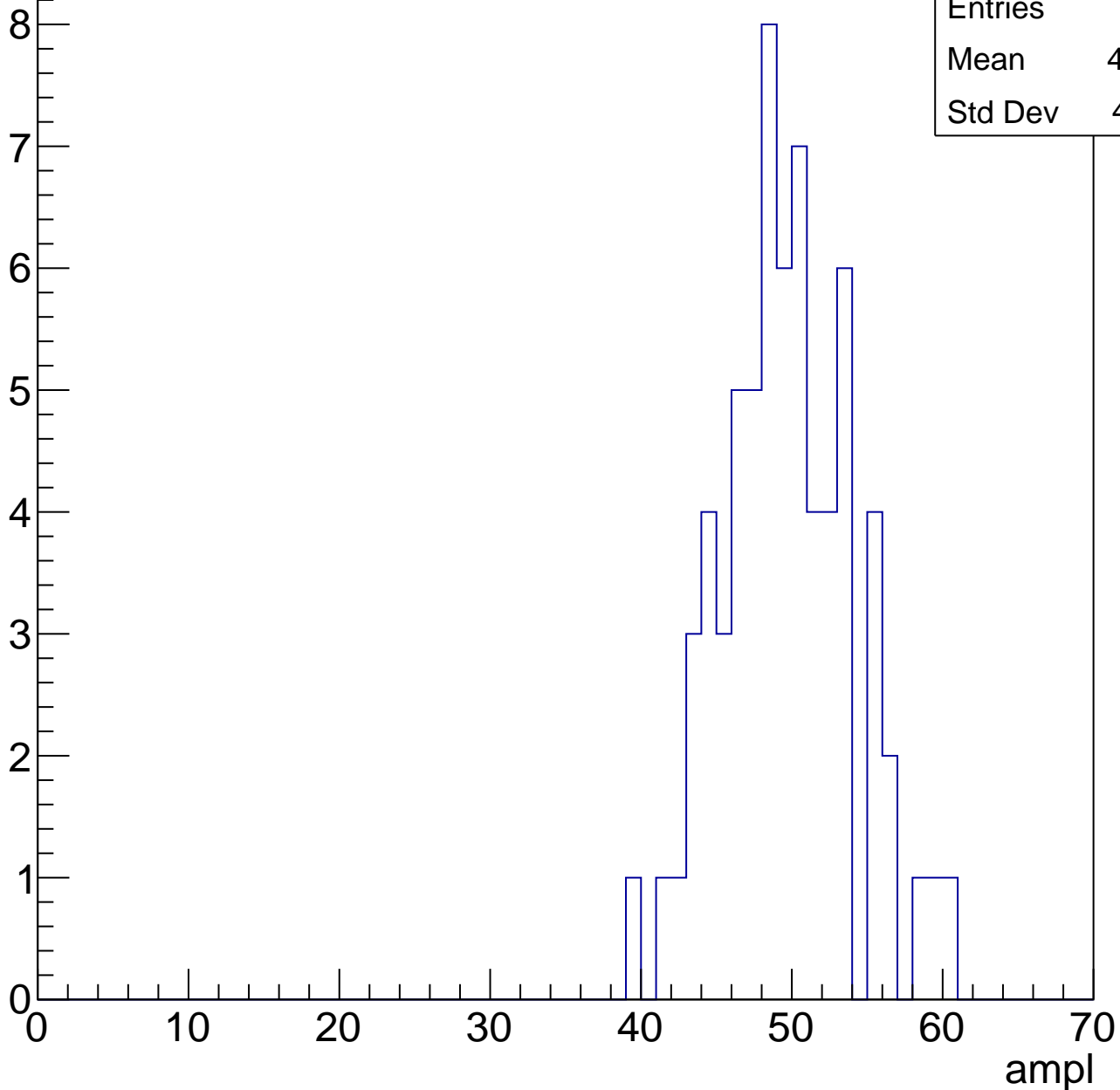


# B1L101S, U16-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	49.16
Std Dev	4.301

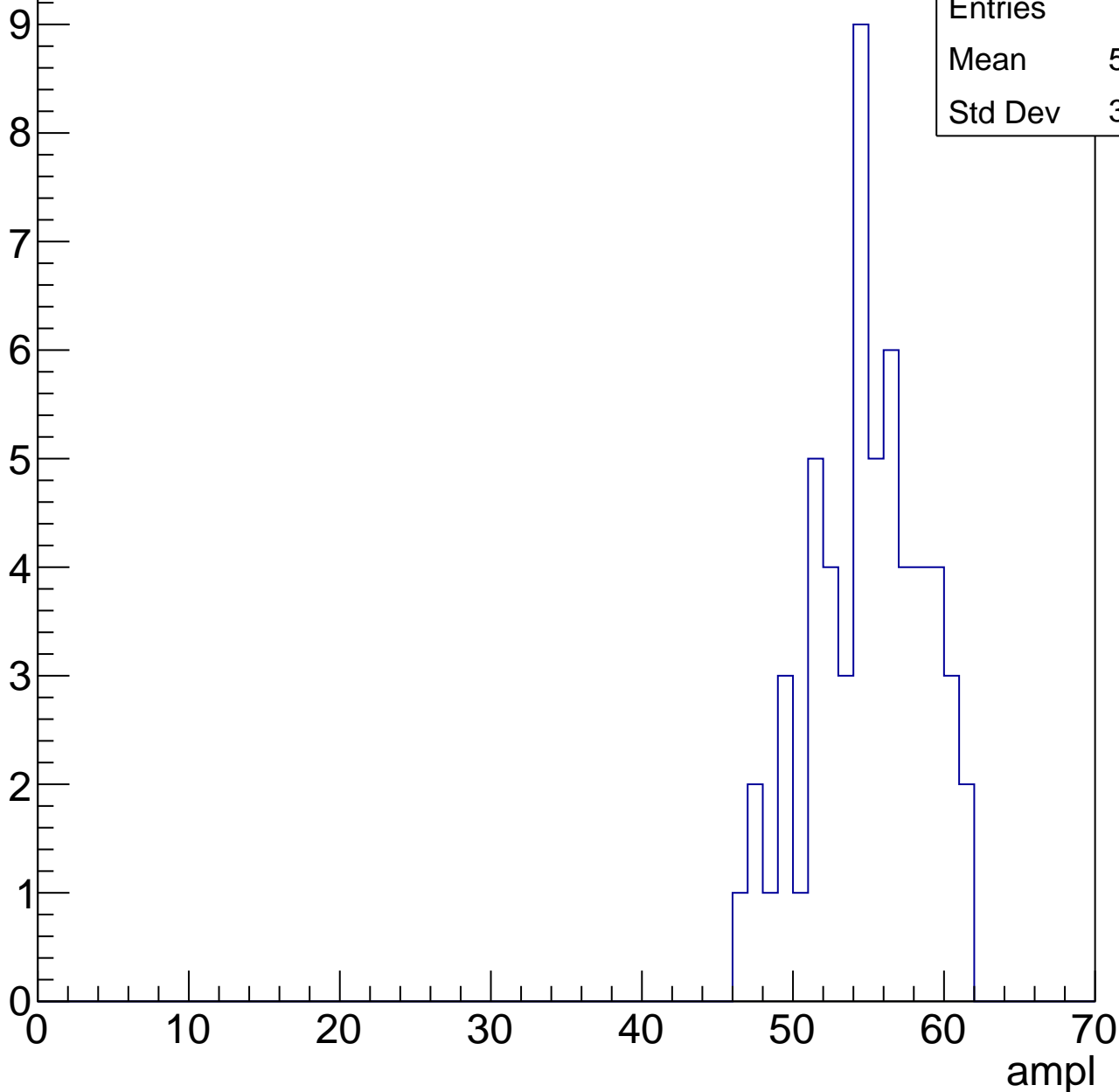


# B1L101S, U16-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	54.42
Std Dev	3.694

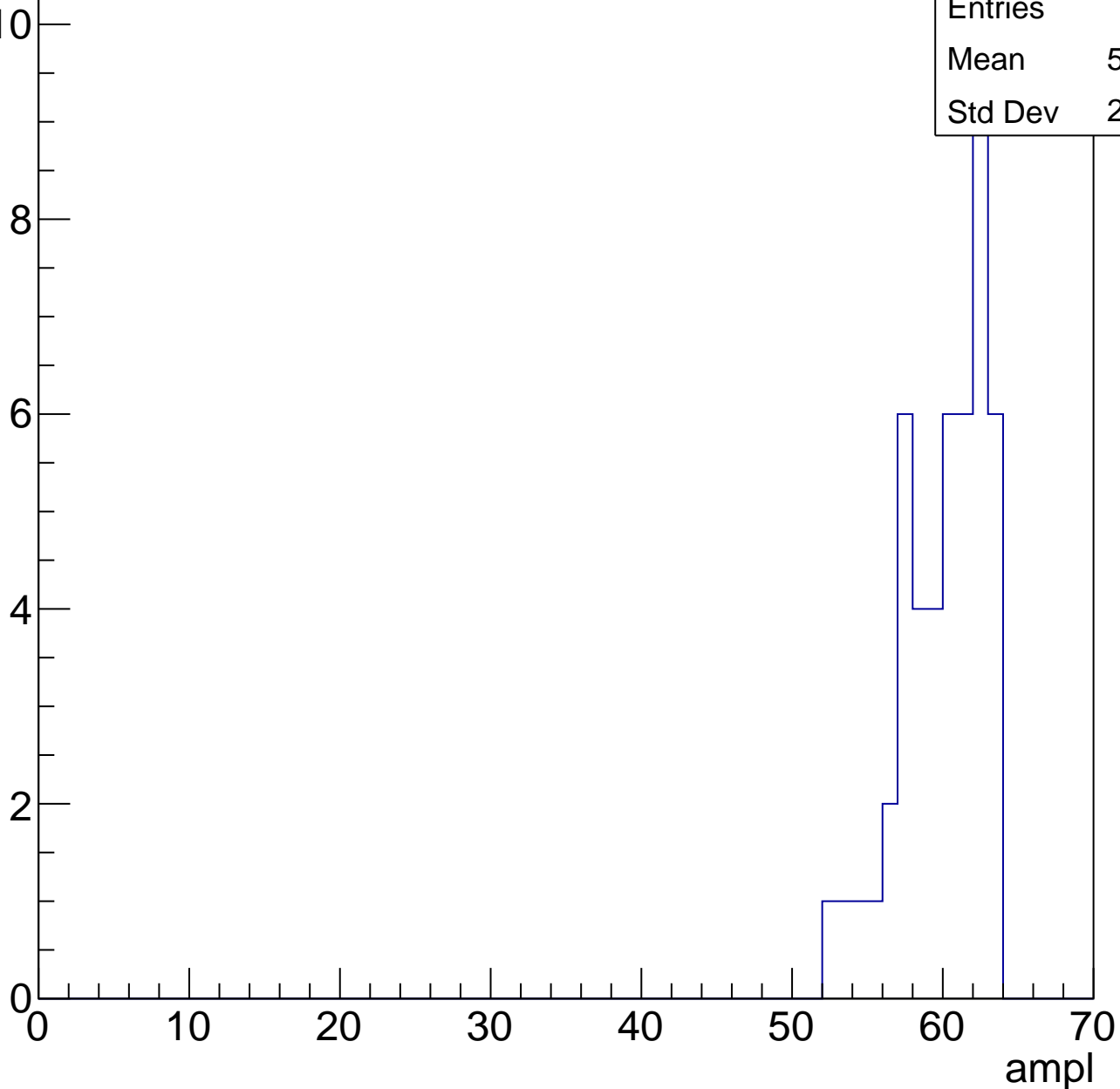


# B1L101S, U16-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

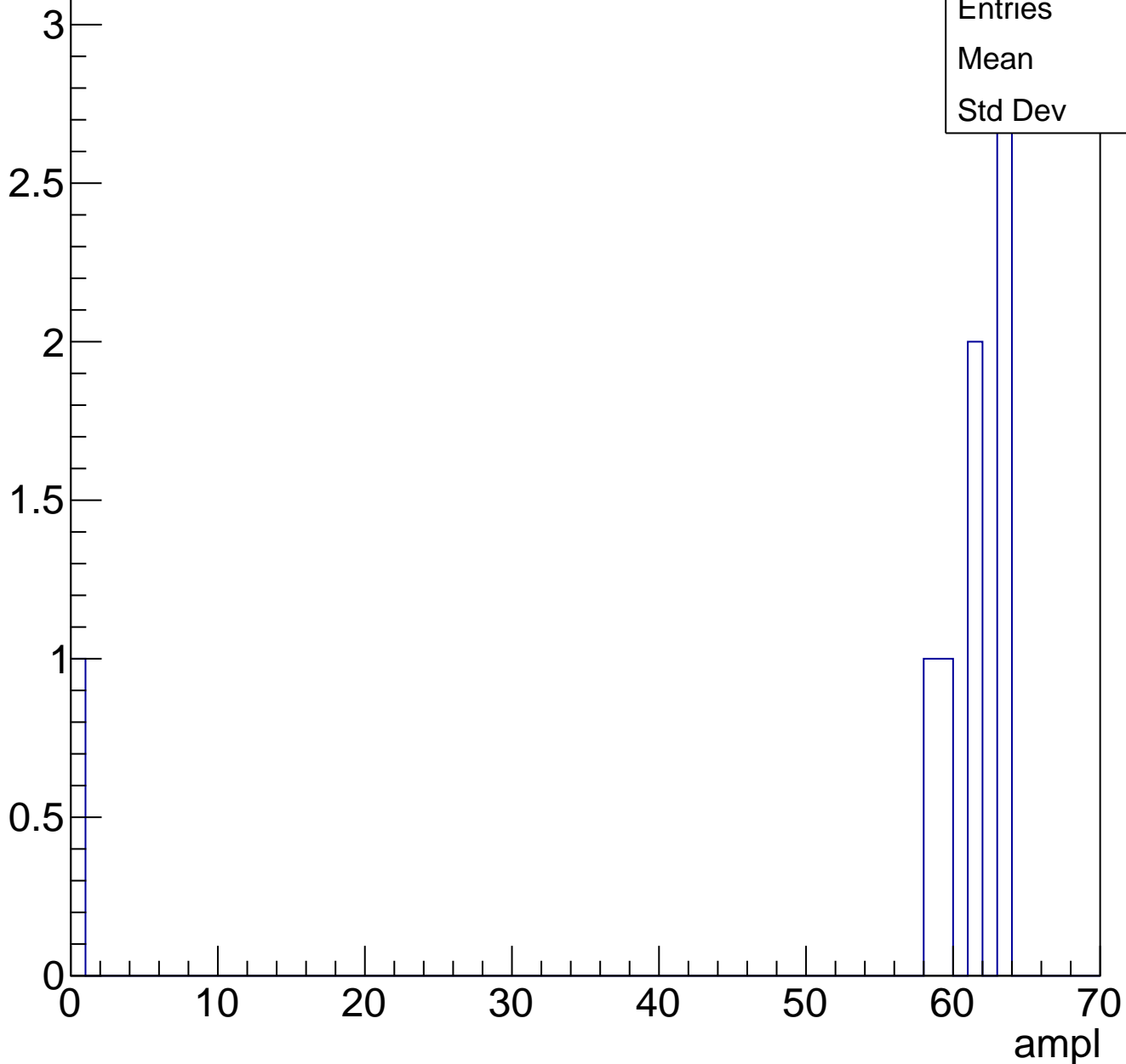
Entries	48
Mean	59.58
Std Dev	2.783



# B1L101S, U16-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L101S, U16-ch115, adc0

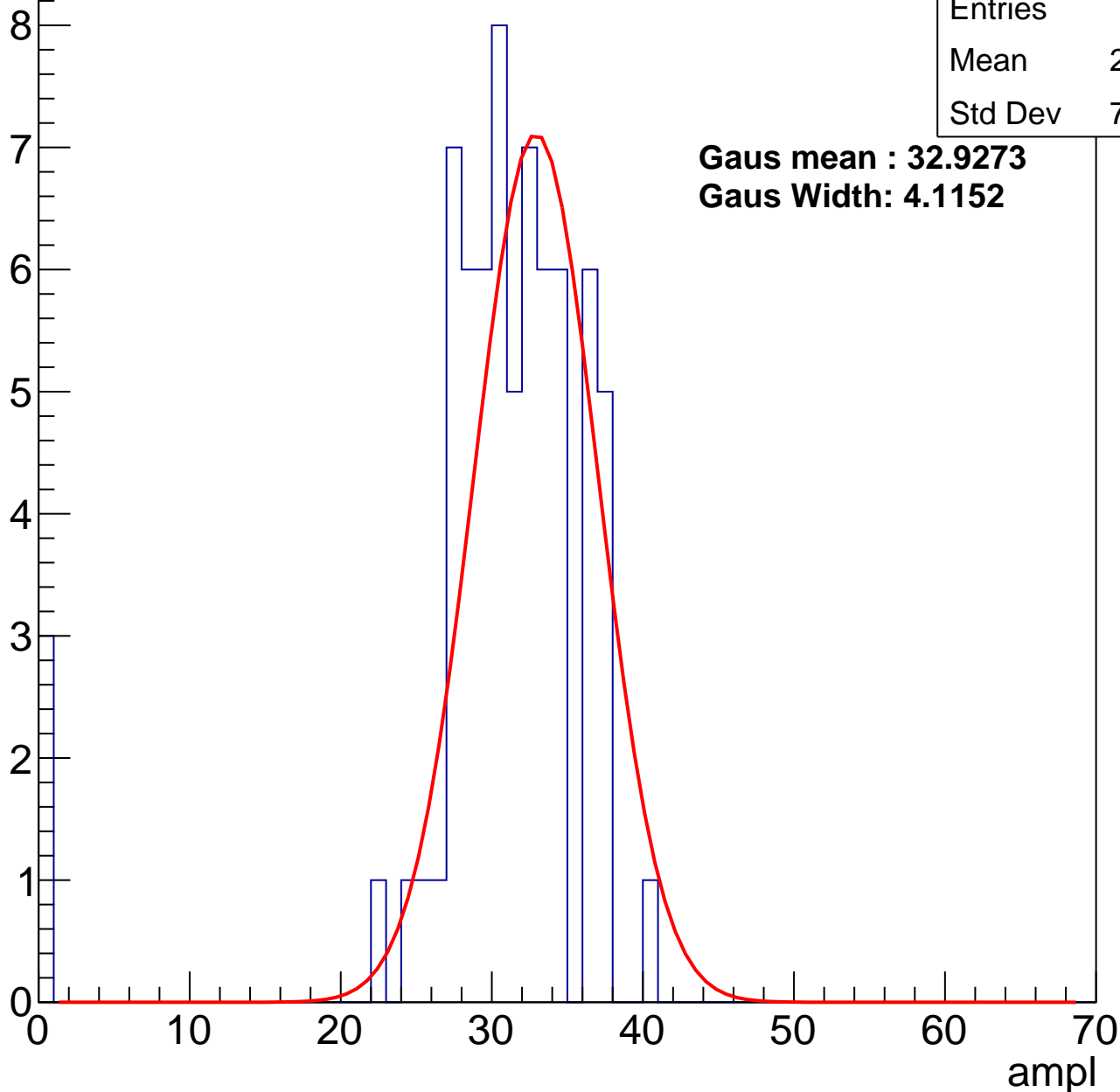
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	29.86
Std Dev	7.247

**Gaus mean : 32.9273**

**Gaus Width: 4.1152**



# B1L101S, U16-ch115, adc1

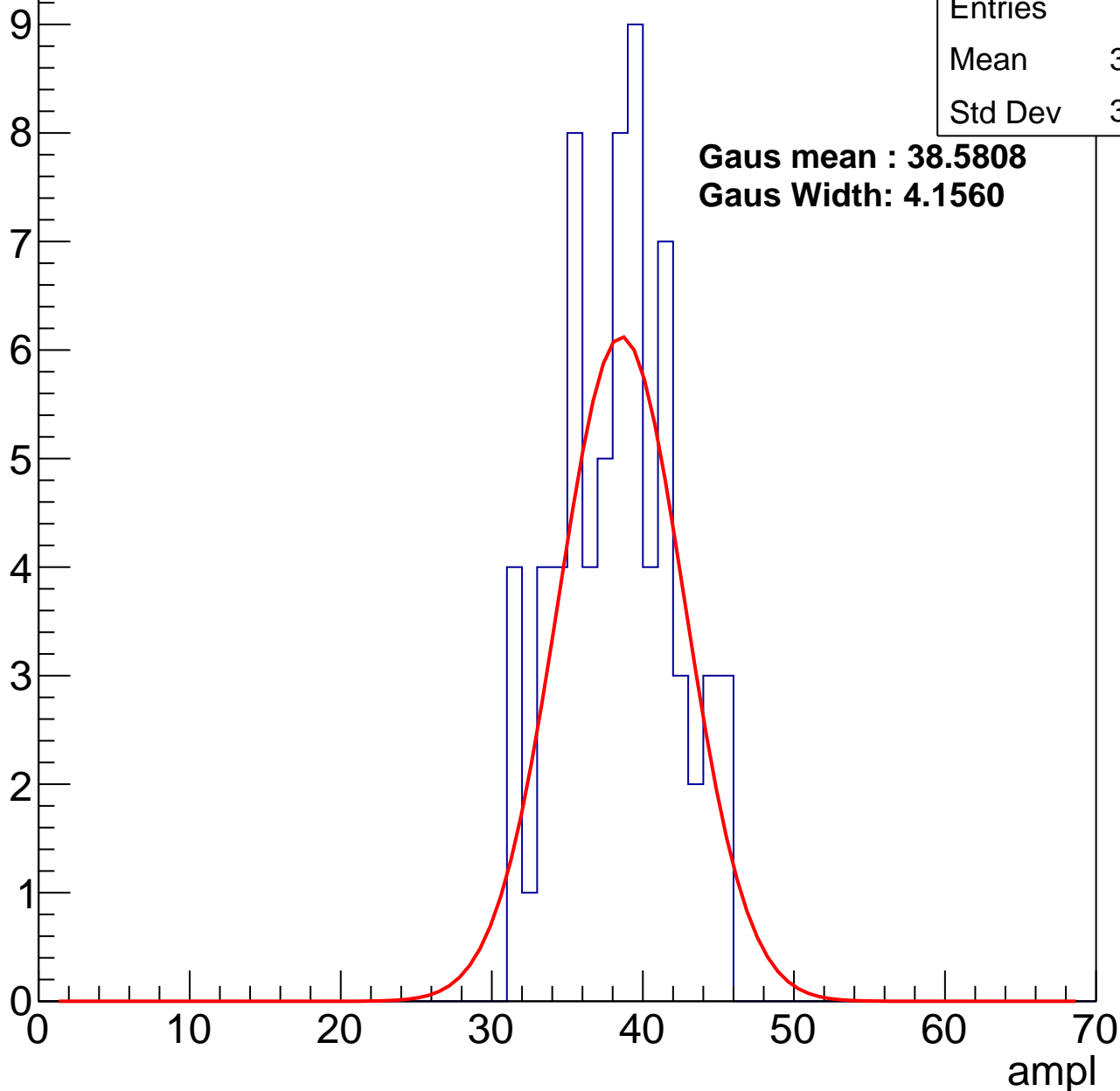
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	37.88
Std Dev	3.669

**Gaus mean : 38.5808**

**Gaus Width: 4.1560**



# B1L101S, U16-ch115, adc2

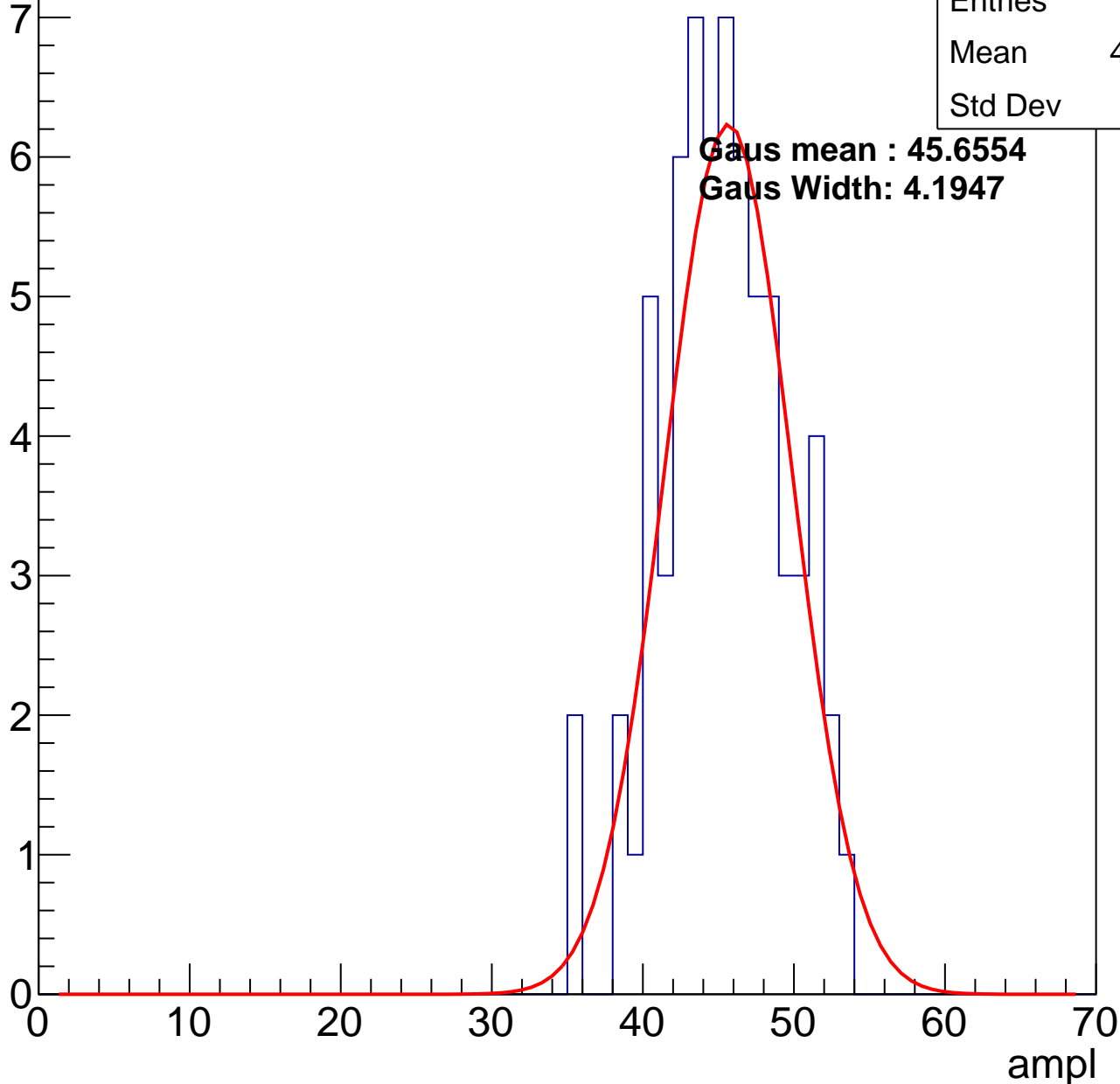
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	44.84
Std Dev	4.01

**Gaus mean : 45.6554**

**Gaus Width: 4.1947**

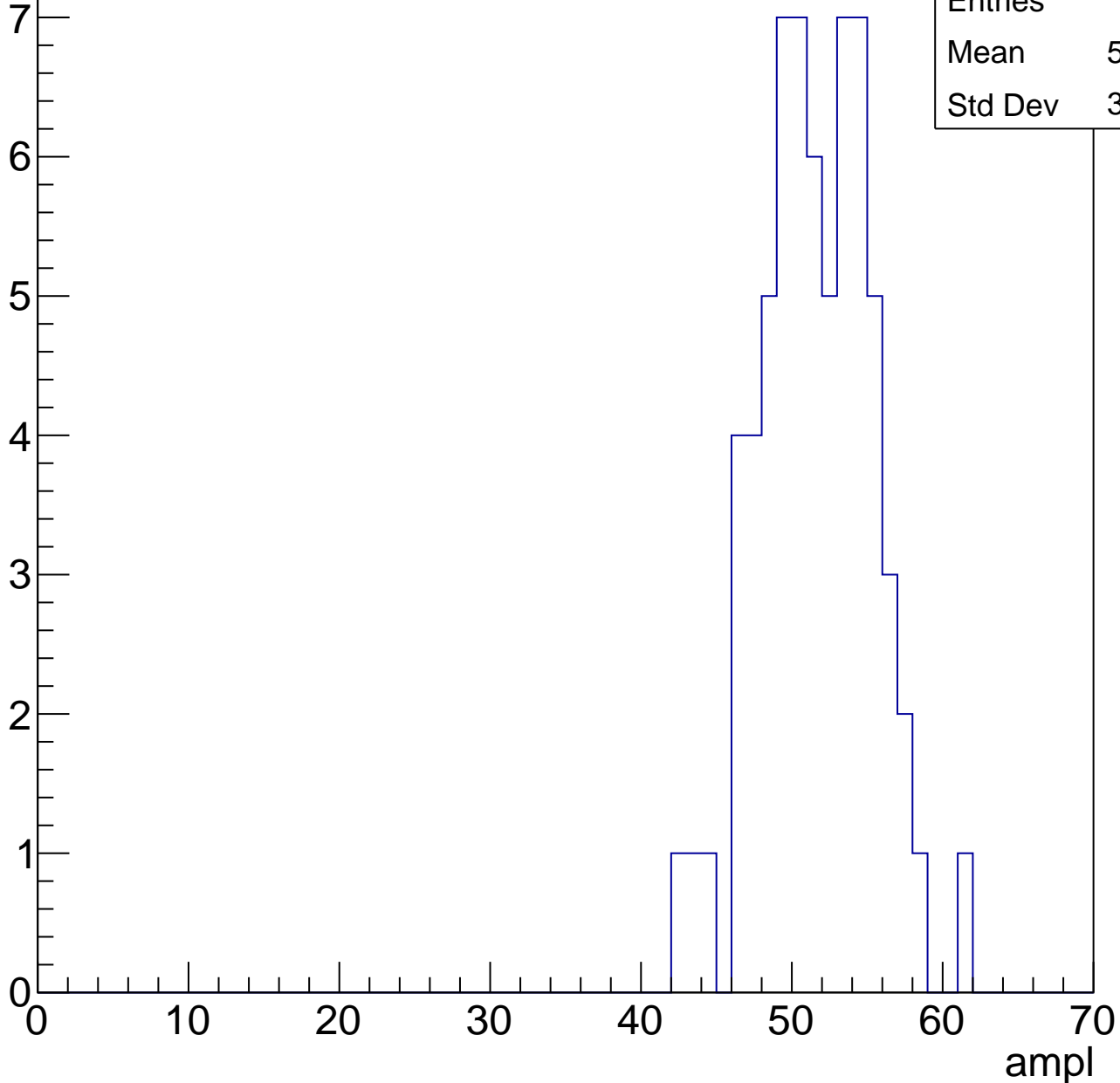


# B1L101S, U16-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

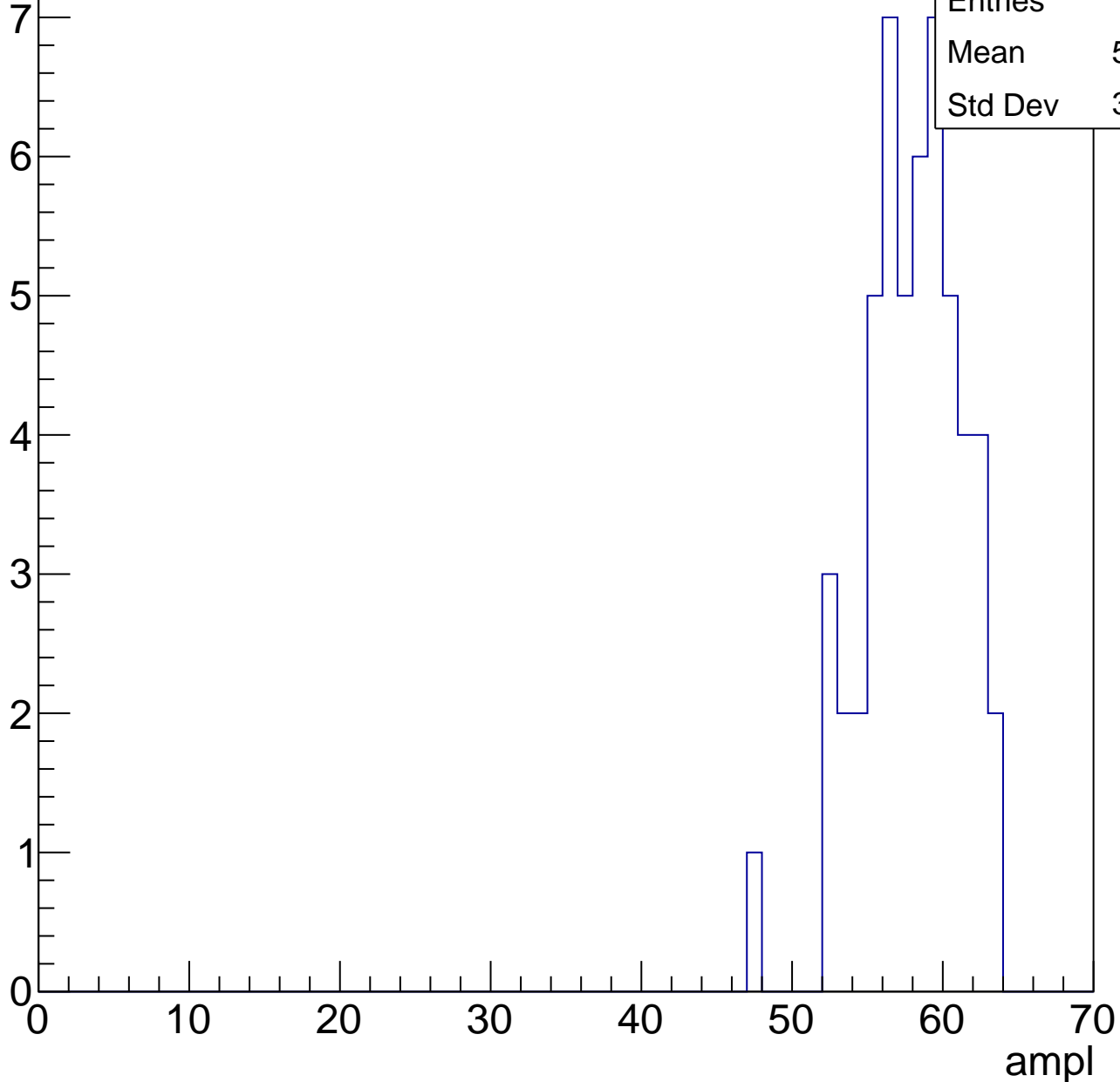
Entries	67
Mean	51.12
Std Dev	3.683



# B1L101S, U16-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



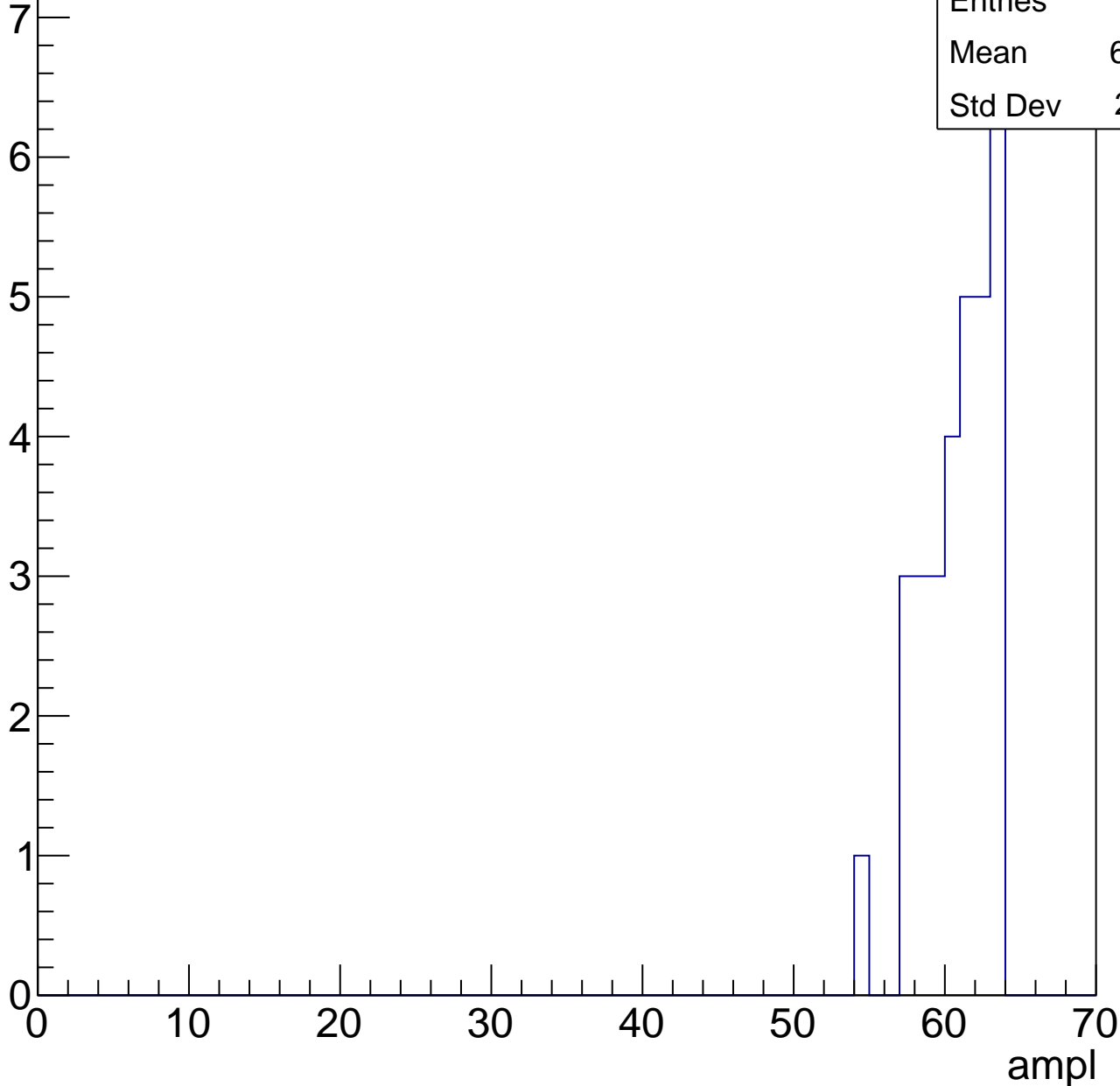
Entries	53
Mean	57.51
Std Dev	3.231

# B1L101S, U16-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

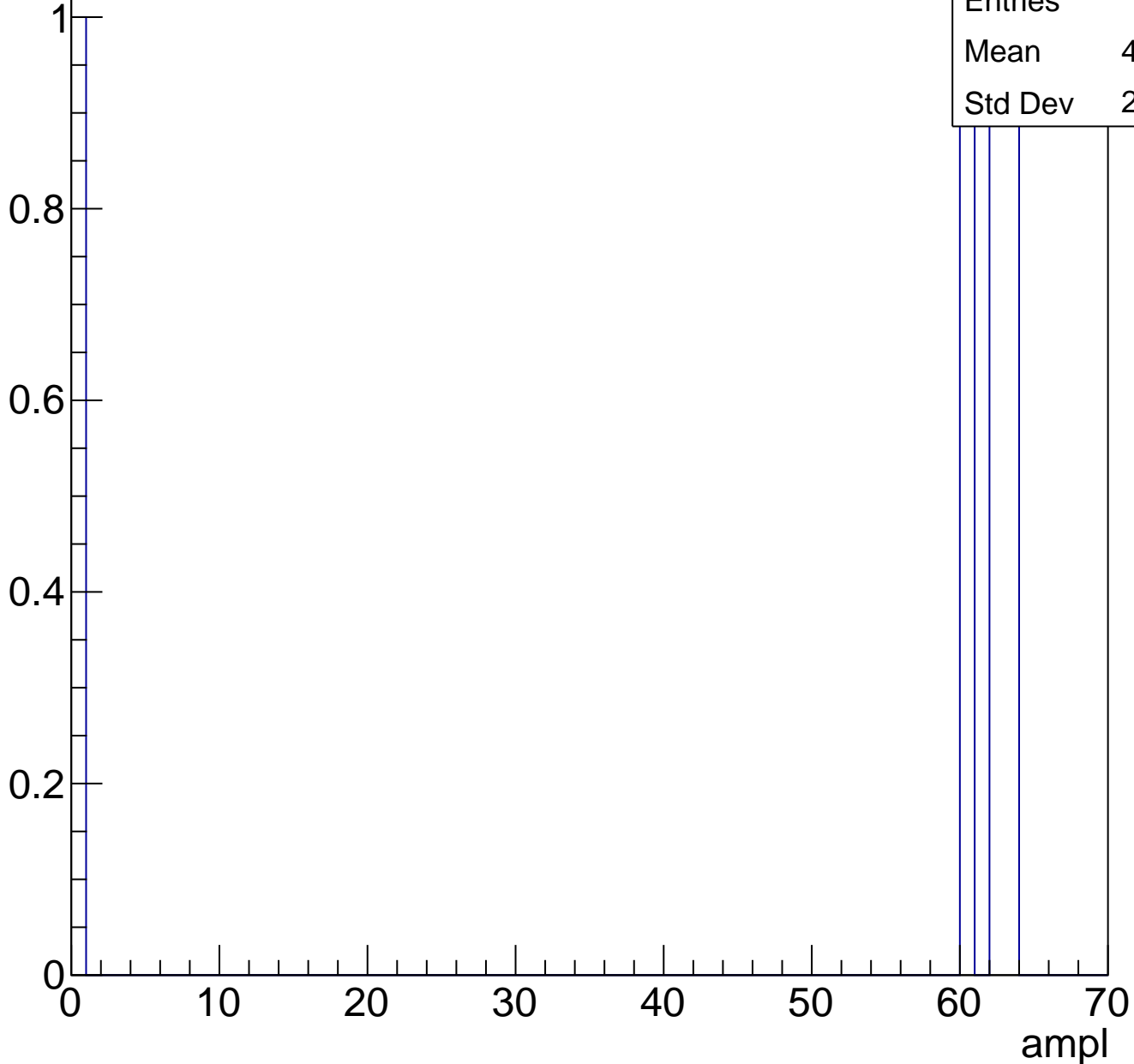
Entries	31
Mean	60.39
Std Dev	2.281



# B1L101S, U16-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U16-ch116, adc0

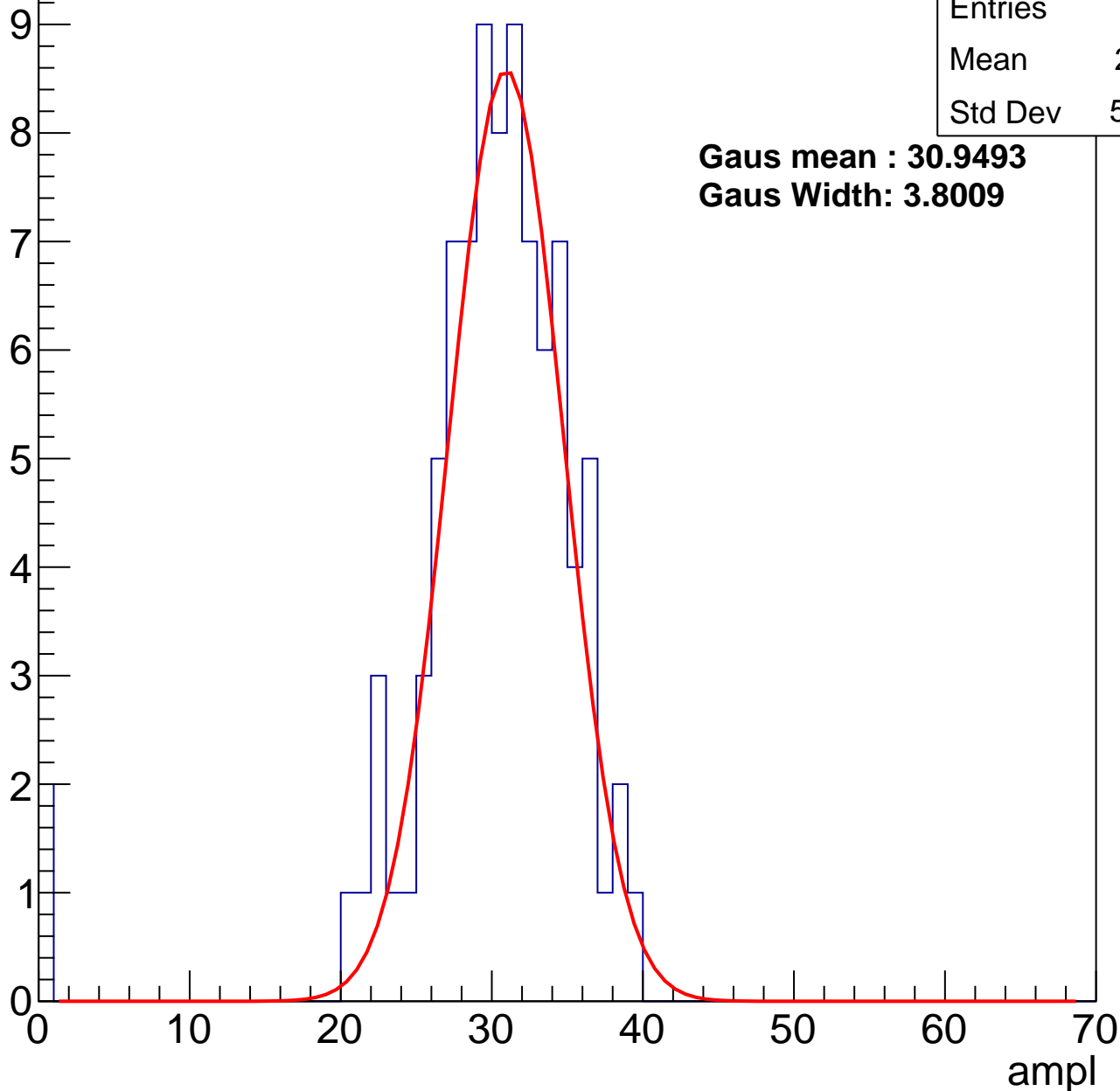
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	90
Mean	29.51
Std Dev	5.993

**Gaus mean : 30.9493**

**Gaus Width: 3.8009**



# B1L101S, U16-ch116, adc1

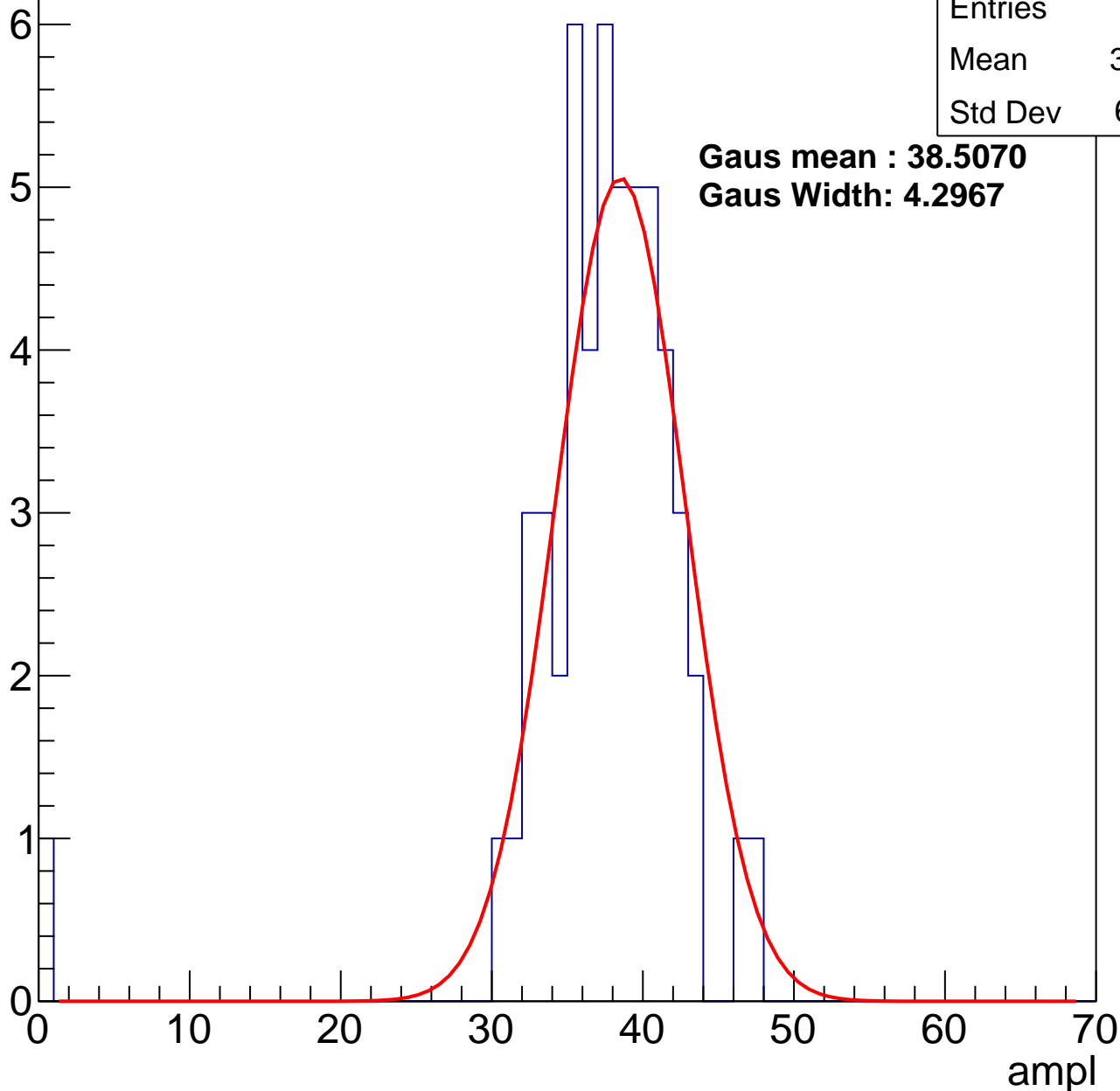
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	36.87
Std Dev	6.271

**Gaus mean : 38.5070**

**Gaus Width: 4.2967**



# B1L101S, U16-ch116, adc2

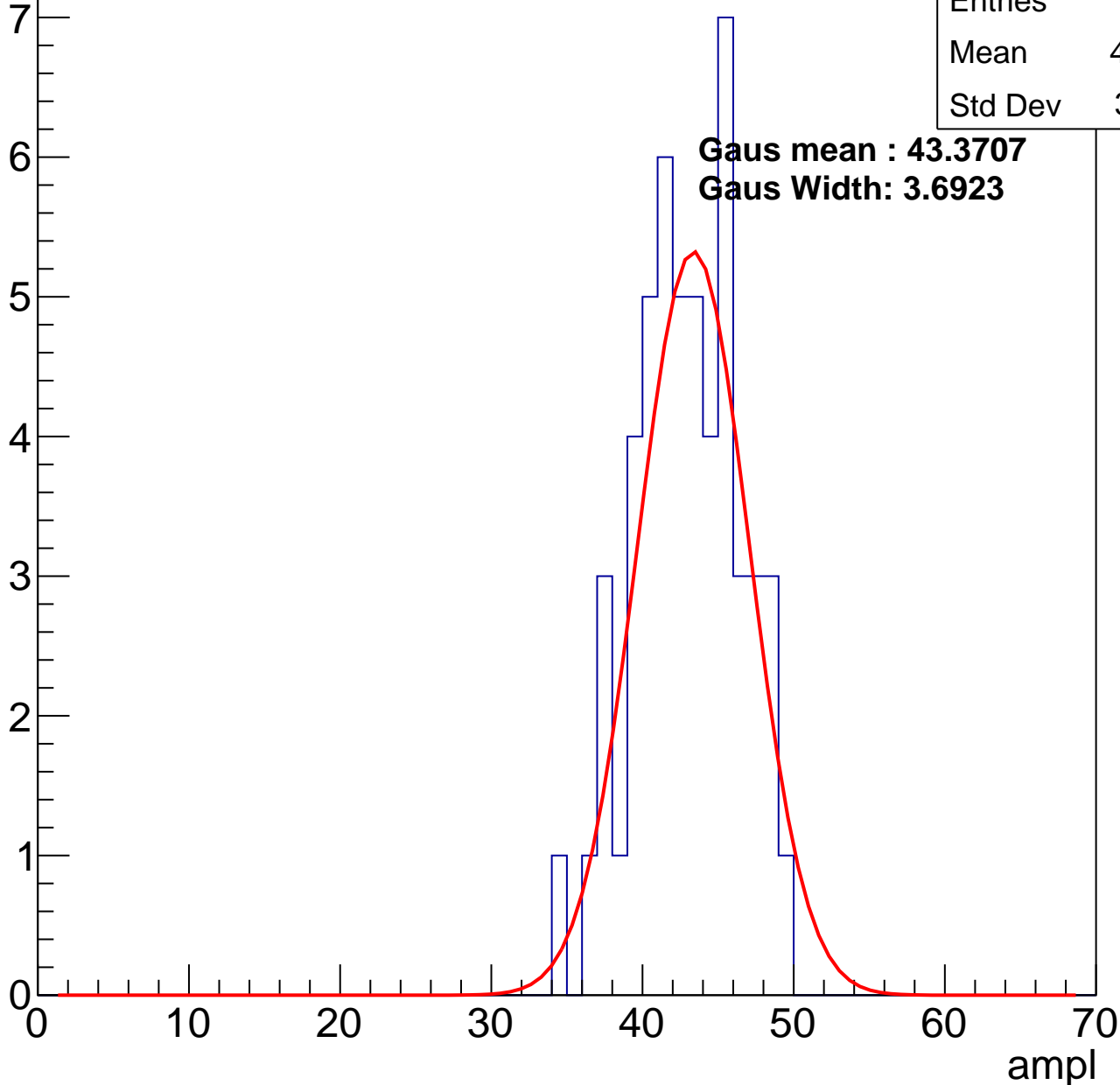
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	42.48
Std Dev	3.411

**Gaus mean : 43.3707**

**Gaus Width: 3.6923**

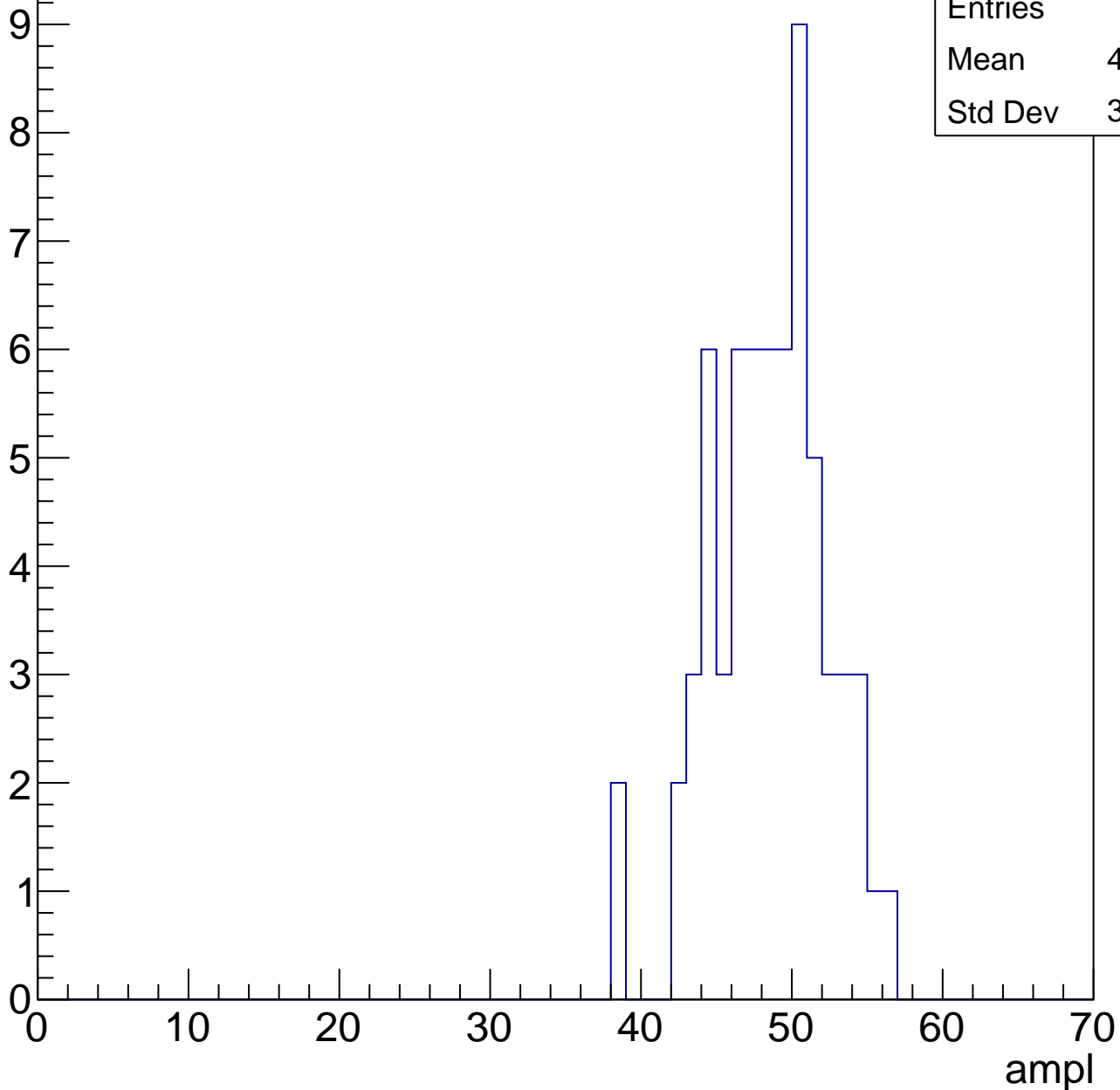


# B1L101S, U16-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	48.02
Std Dev	3.785

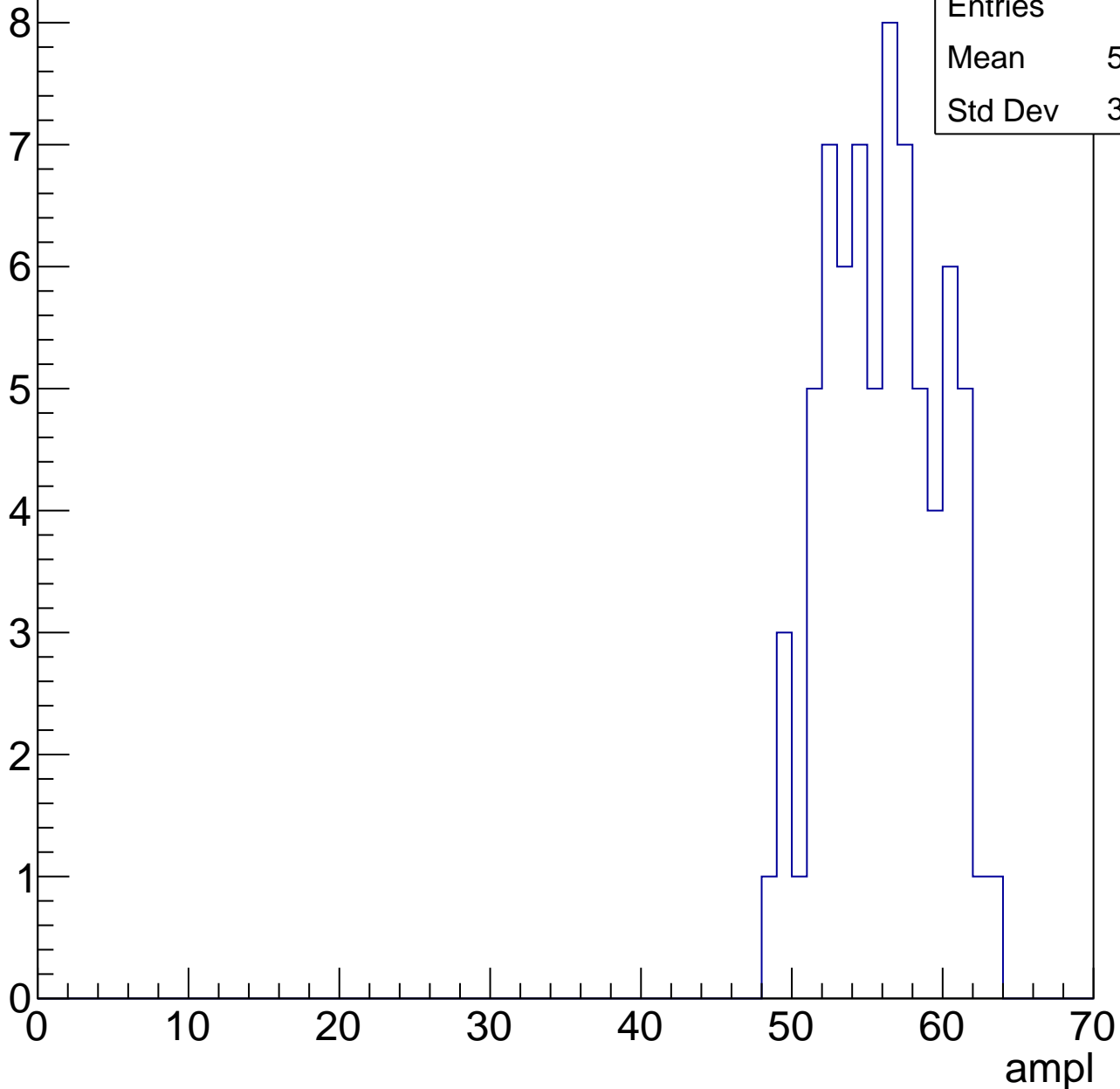


# B1L101S, U16-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	55.53
Std Dev	3.582

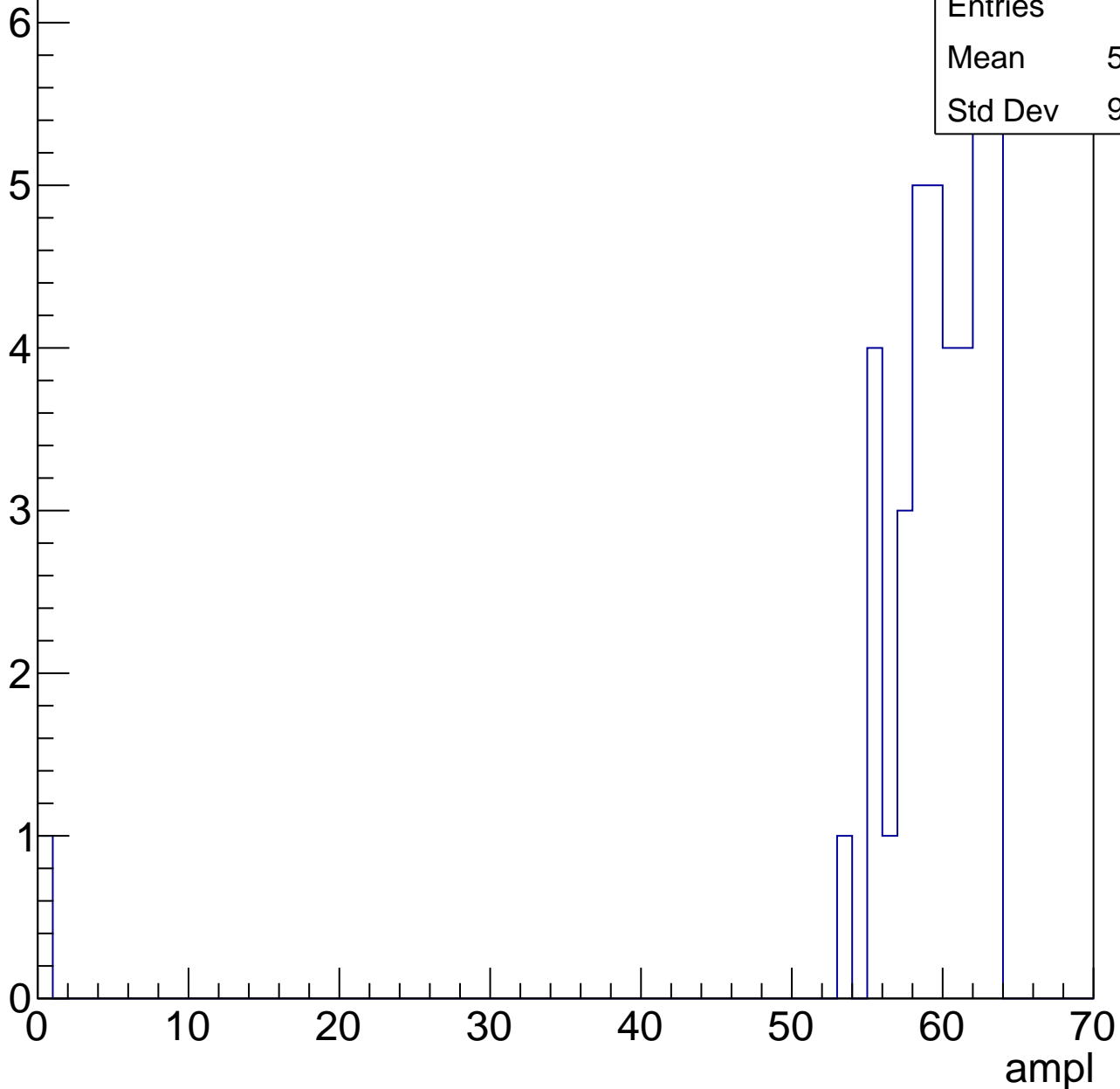


# B1L101S, U16-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

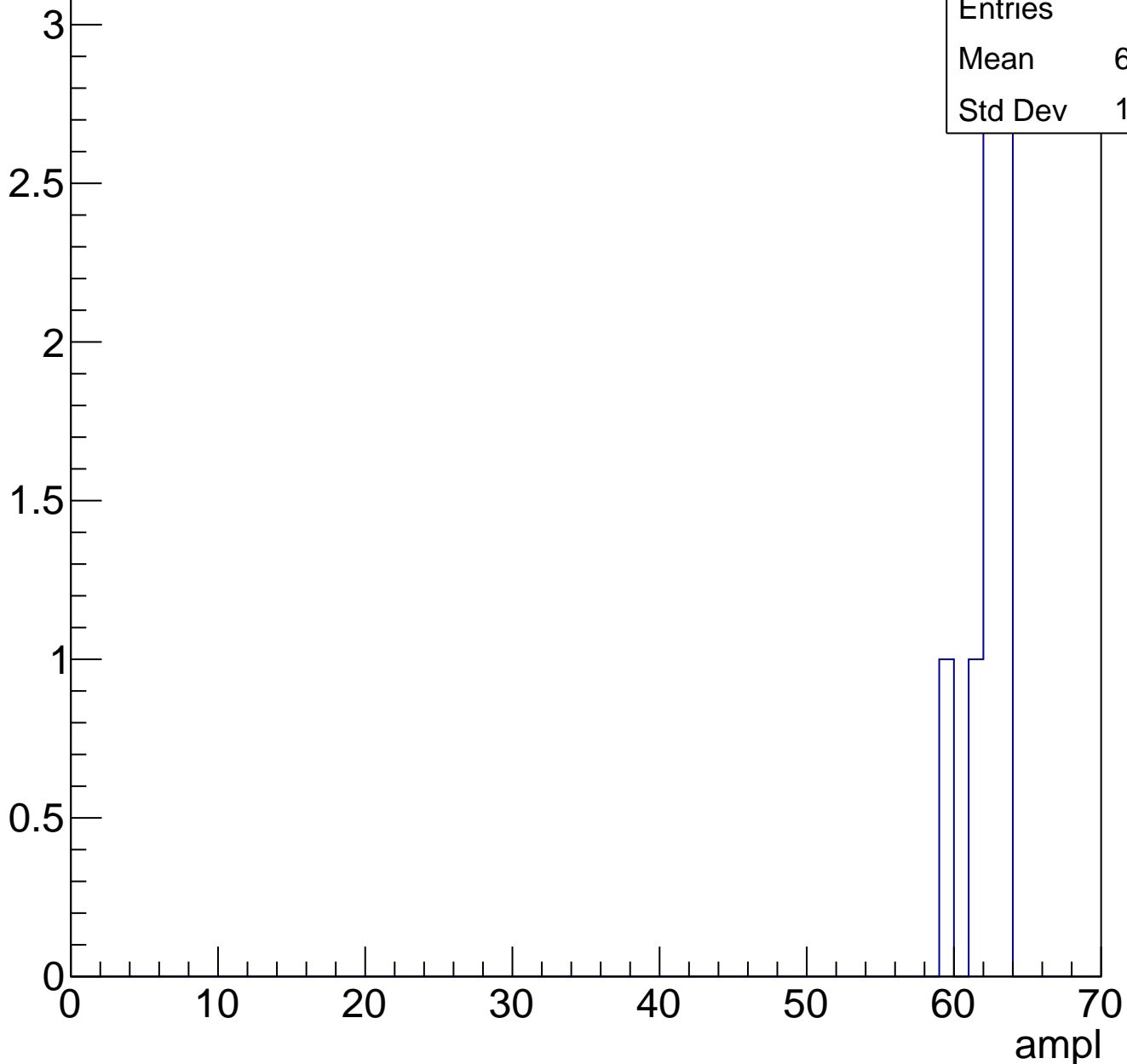
Entries	40
Mean	57.98
Std Dev	9.663



# B1L101S, U16-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U16-ch117, adc0

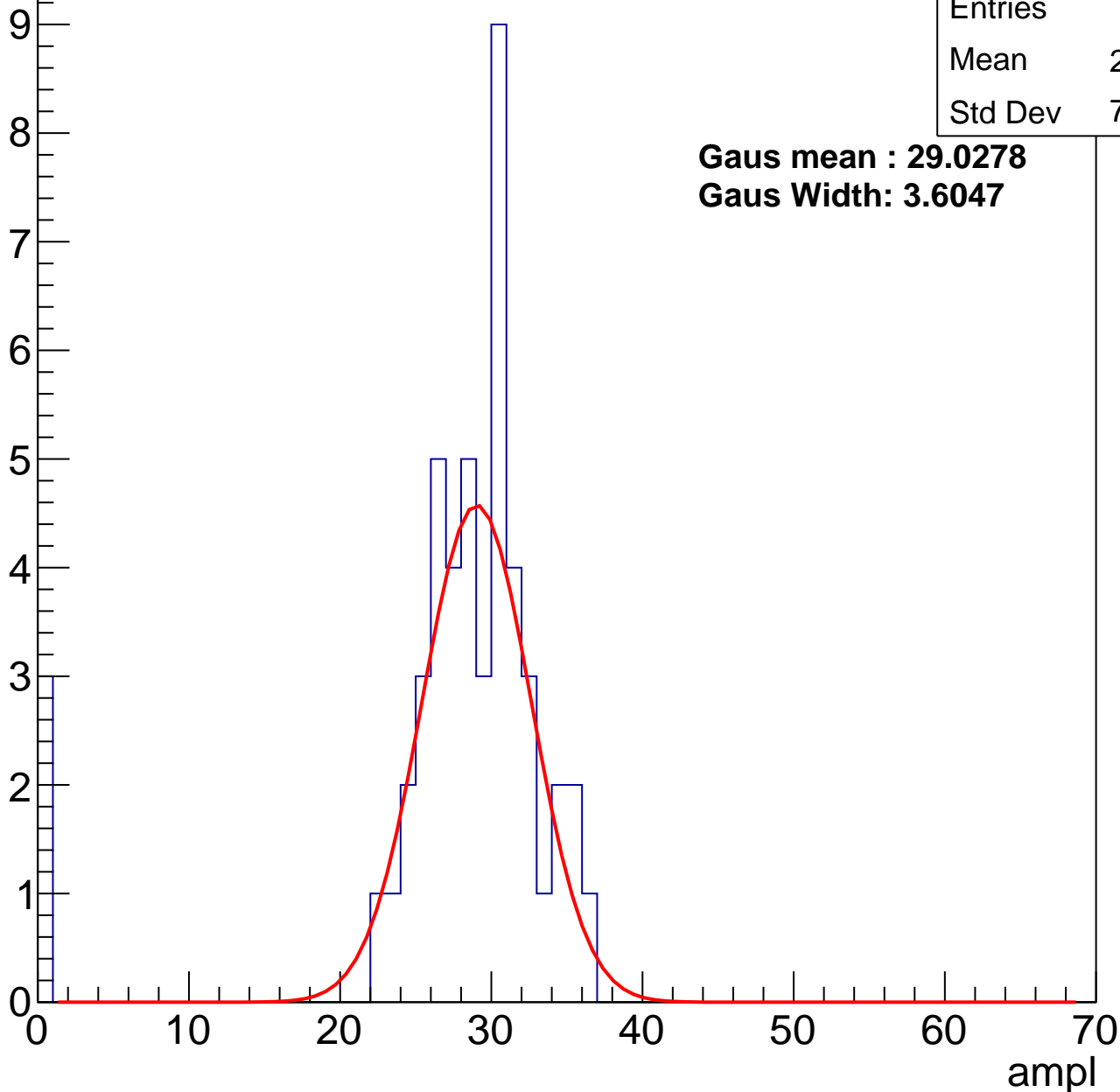
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	27.14
Std Dev	7.616

**Gaus mean : 29.0278**

**Gaus Width: 3.6047**



# B1L101S, U16-ch117, adc1

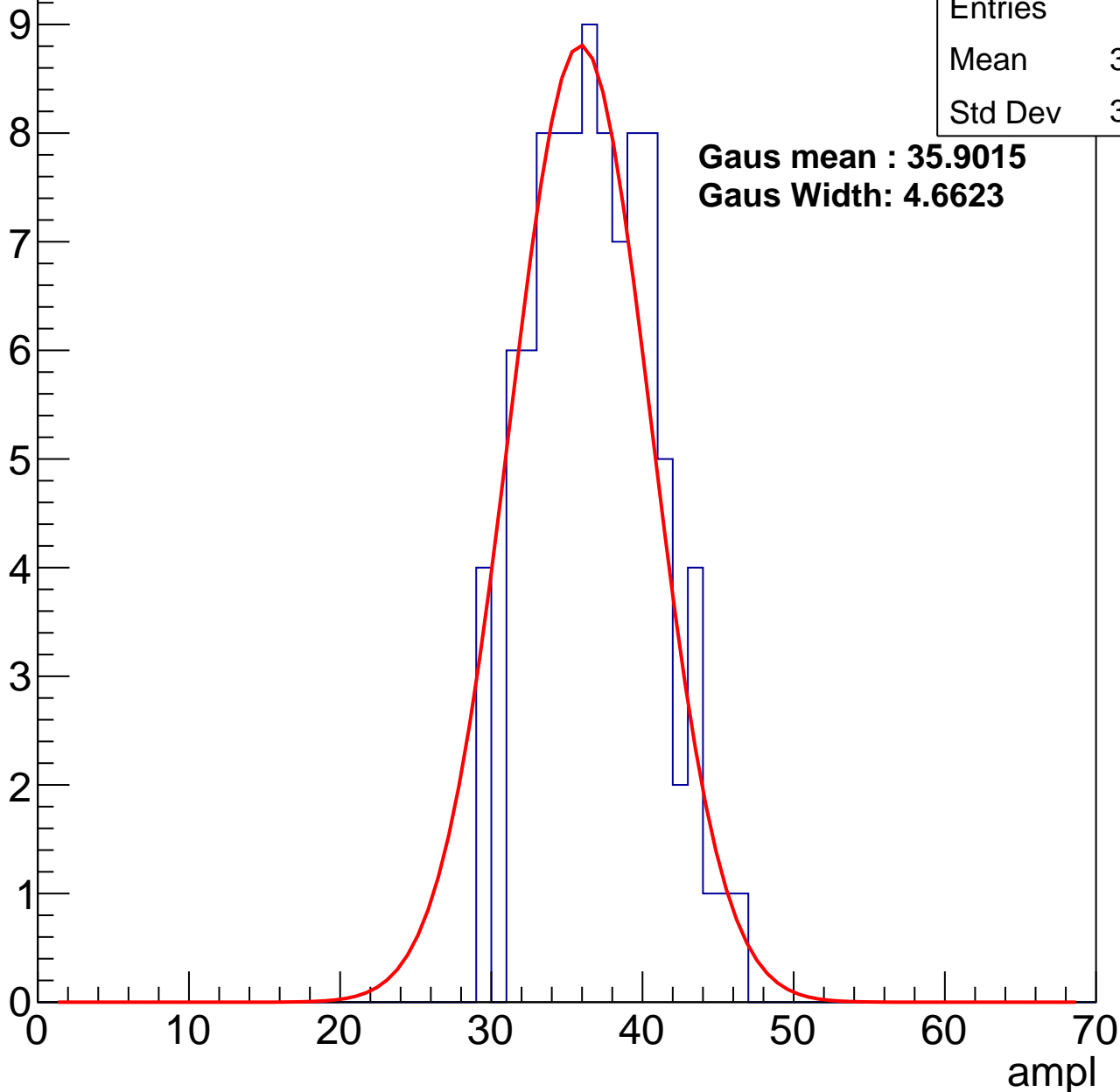
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	94
Mean	36.43
Std Dev	3.874

**Gaus mean : 35.9015**

**Gaus Width: 4.6623**



# B1L101S, U16-ch117, adc2

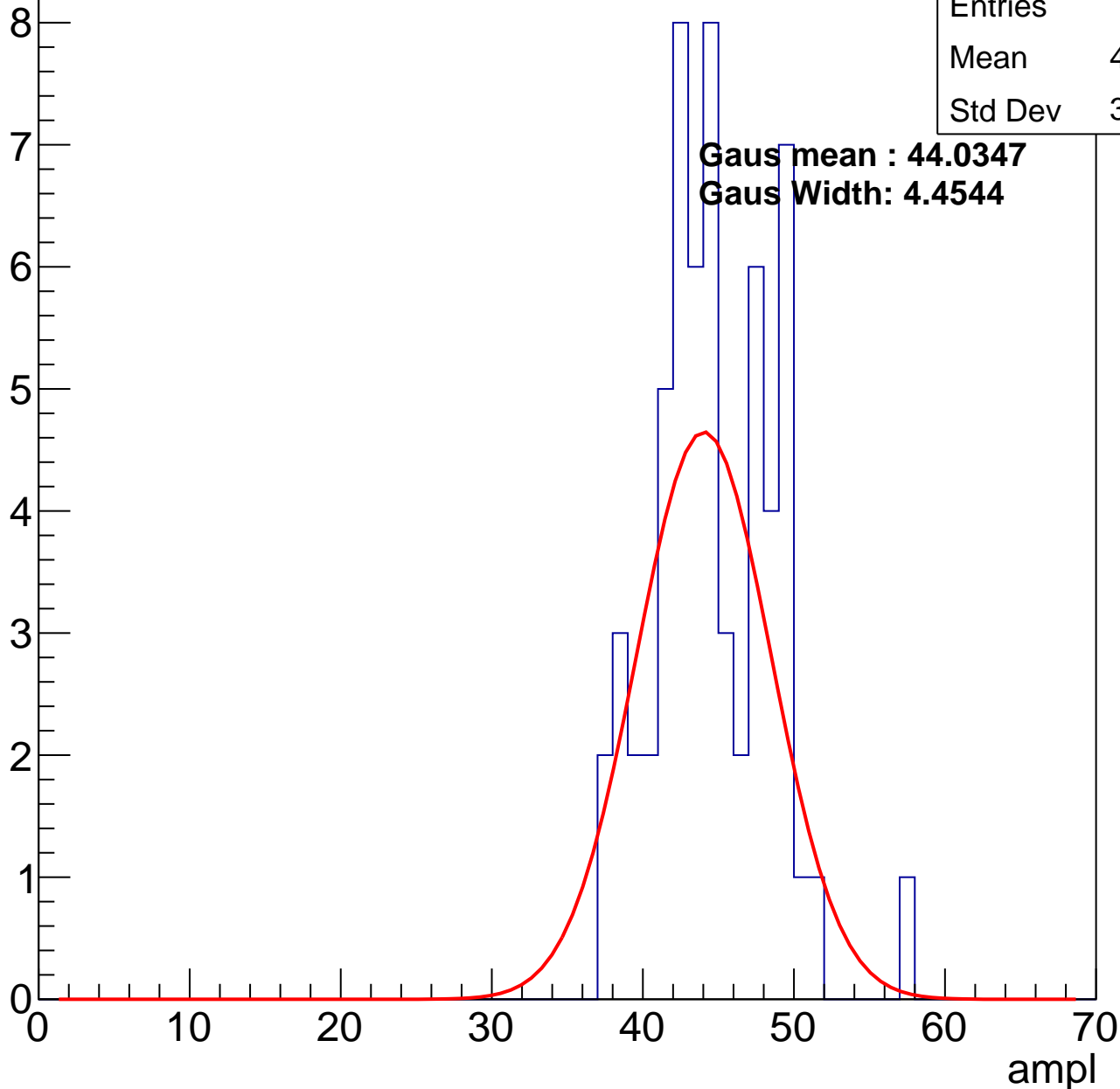
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	44.25
Std Dev	3.895

**Gaus mean : 44.0347**

**Gaus Width: 4.4544**

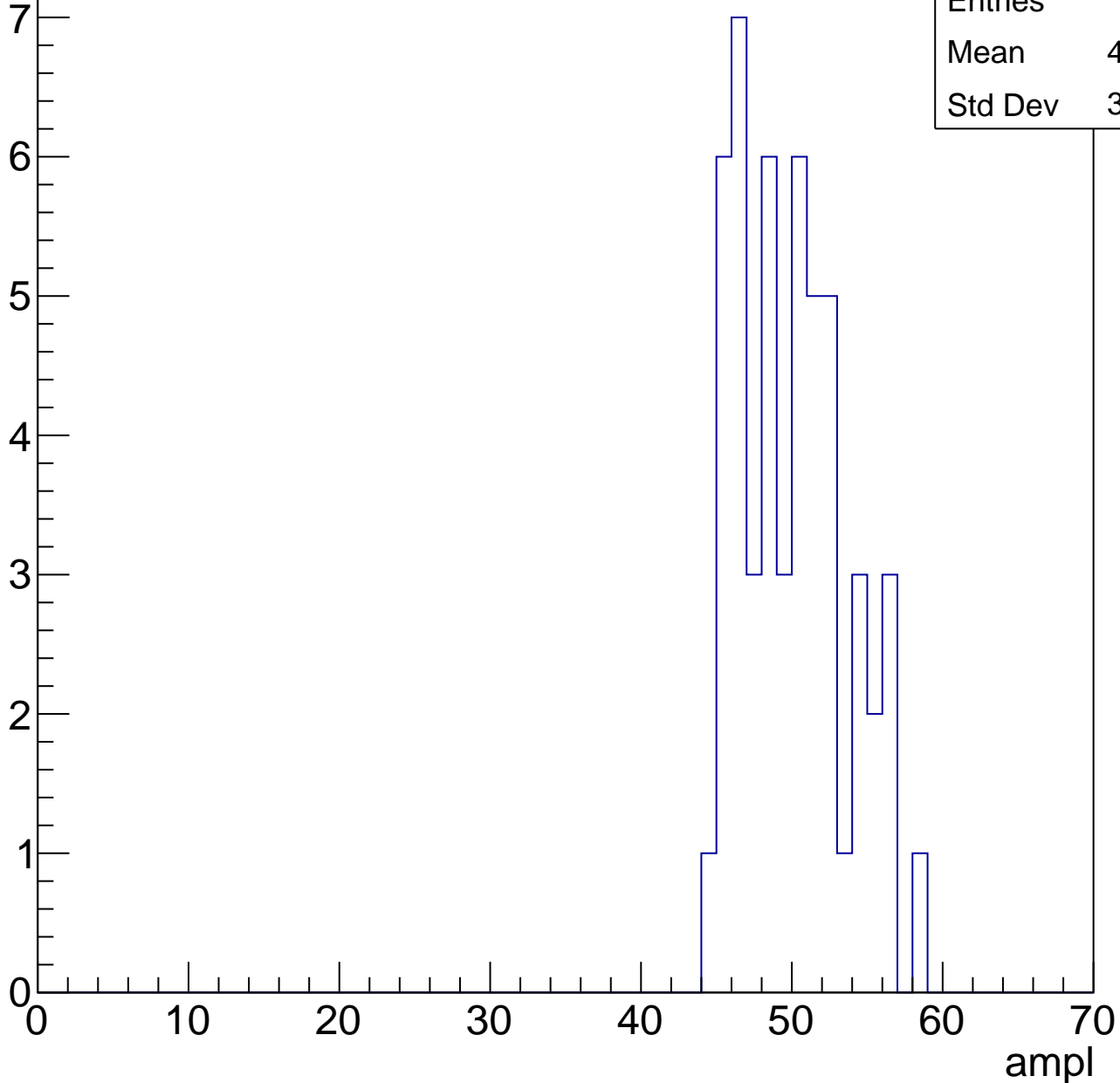


# B1L101S, U16-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	49.58
Std Dev	3.527

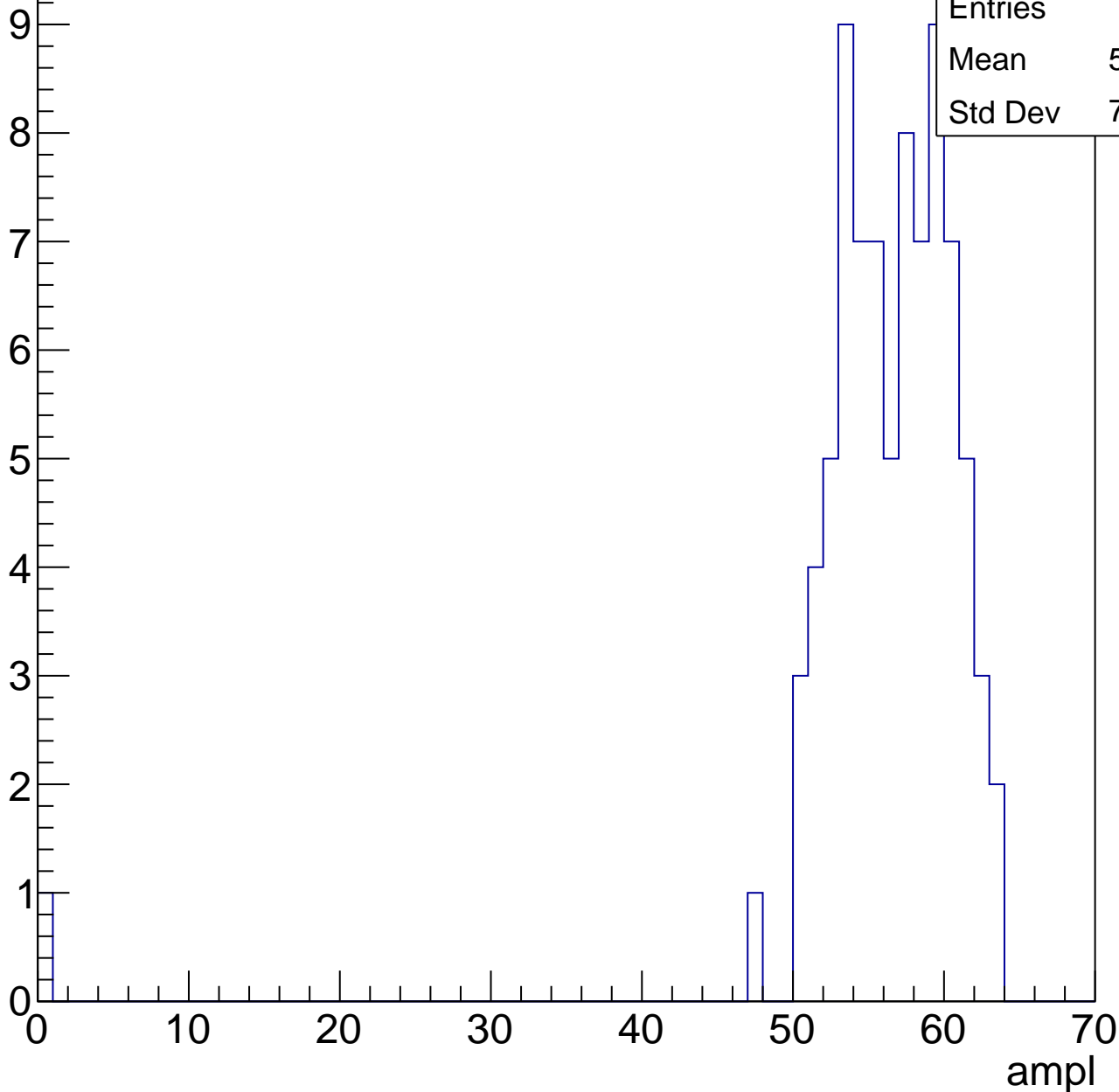


# B1L101S, U16-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	83
Mean	55.55
Std Dev	7.083

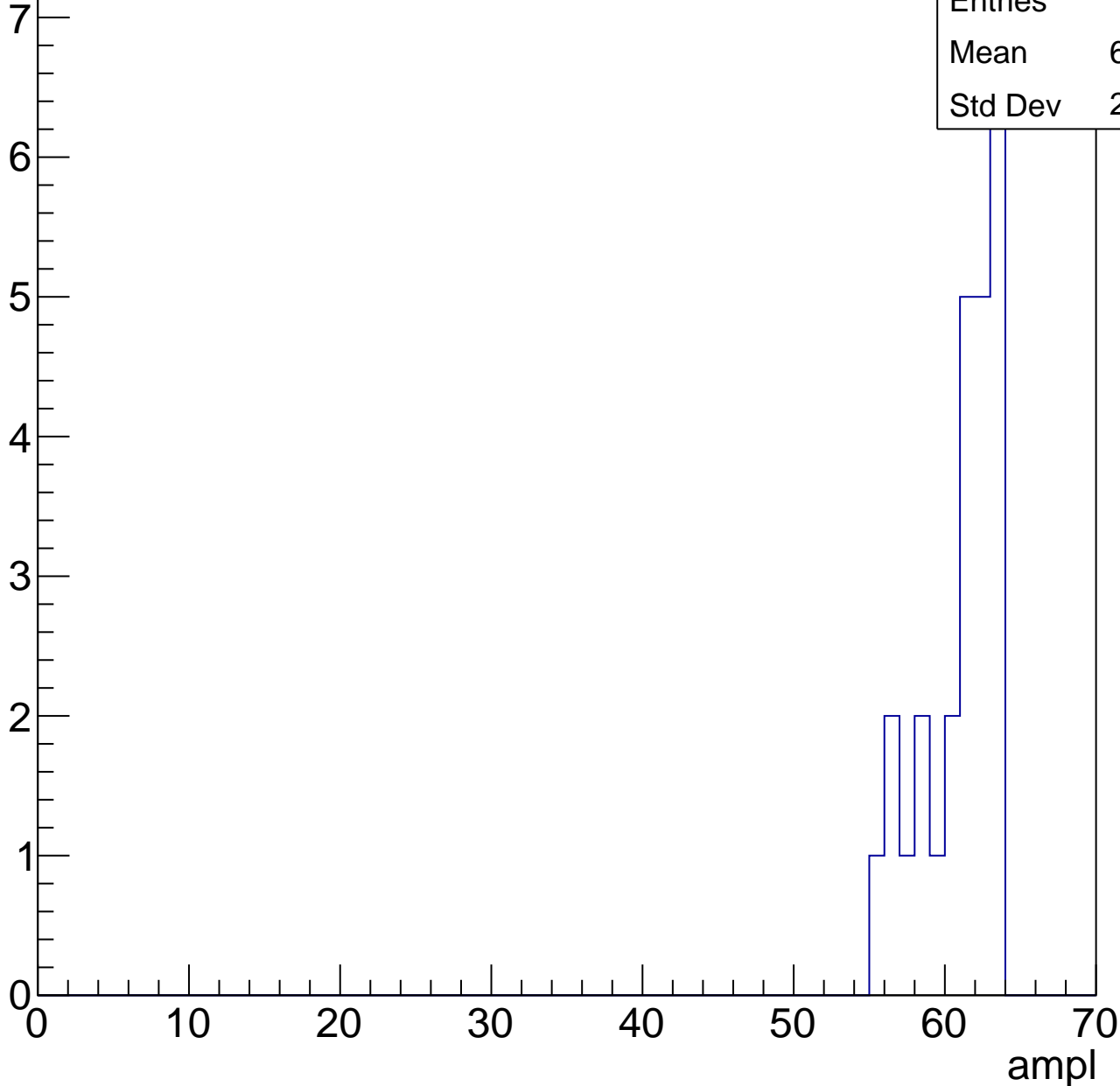


# B1L101S, U16-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	26
Mean	60.58
Std Dev	2.436



# B1L101S, U16-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	61.75
Std Dev	1.09

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U16-ch118, adc0

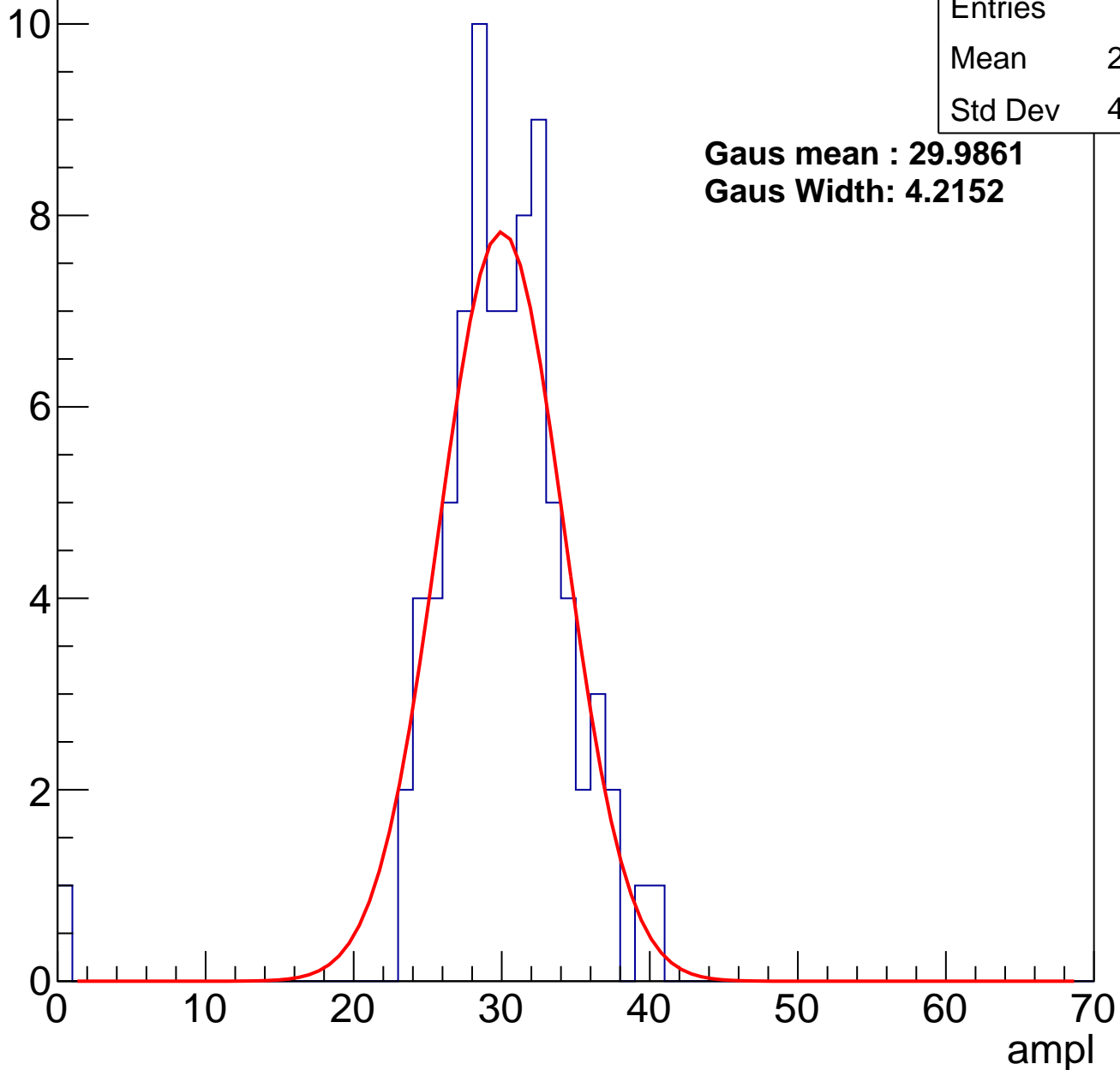
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	82
Mean	29.54
Std Dev	4.944

**Gaus mean : 29.9861**

**Gaus Width: 4.2152**

Entry



# B1L101S, U16-ch118, adc1

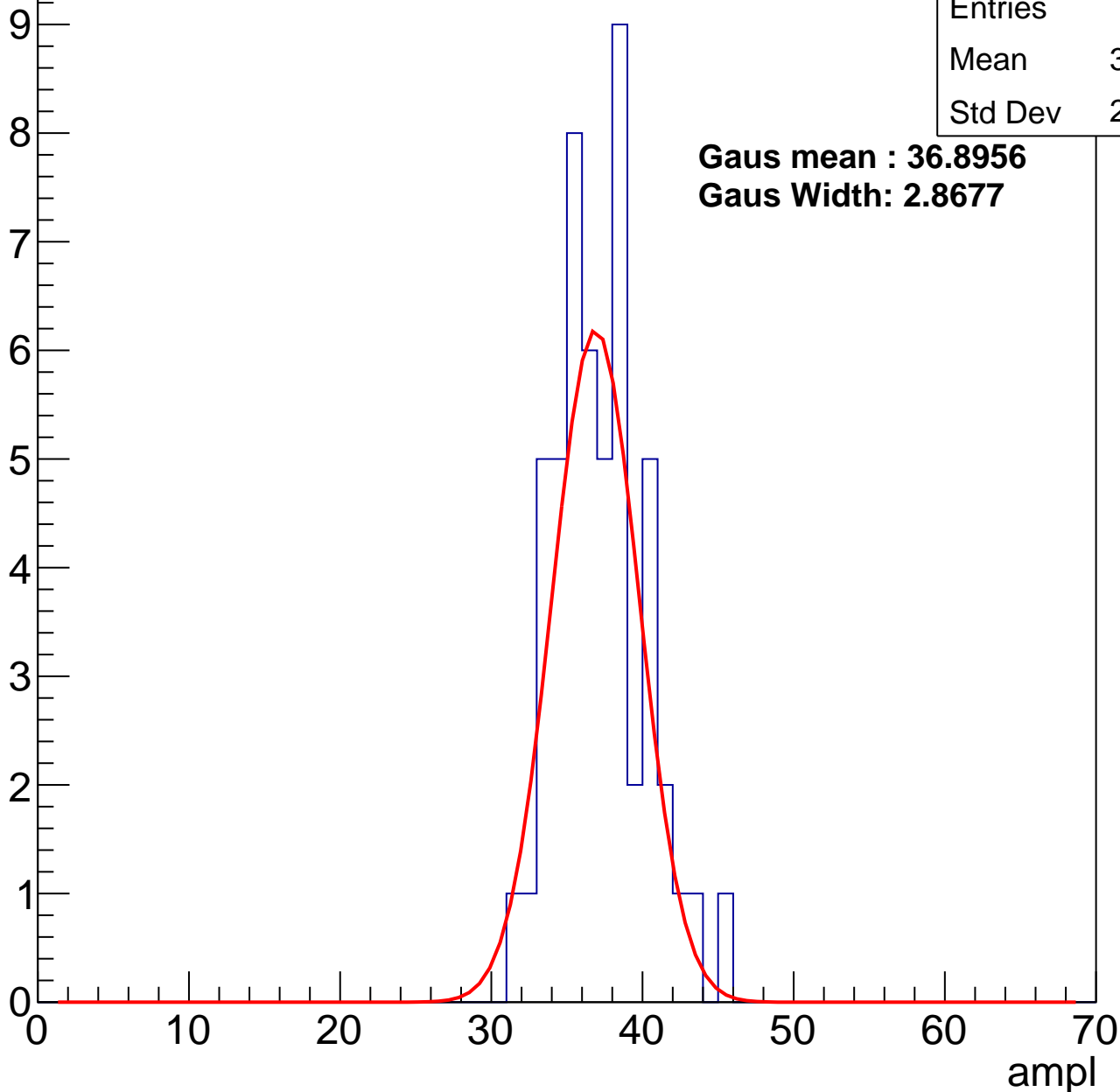
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	36.75
Std Dev	2.908

**Gaus mean : 36.8956**

**Gaus Width: 2.8677**



# B1L101S, U16-ch118, adc2

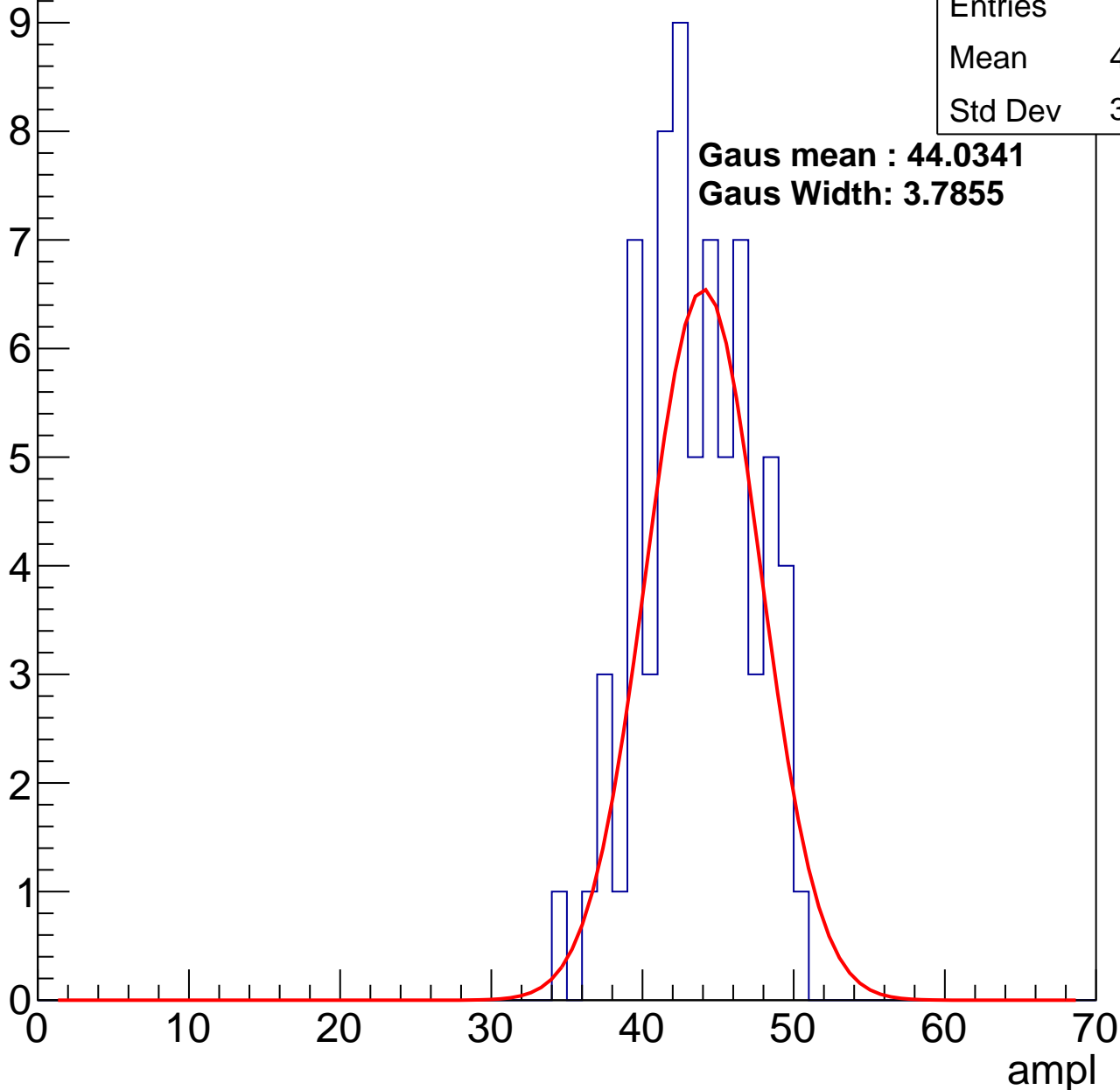
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	43.07
Std Dev	3.583

**Gaus mean : 44.0341**

**Gaus Width: 3.7855**

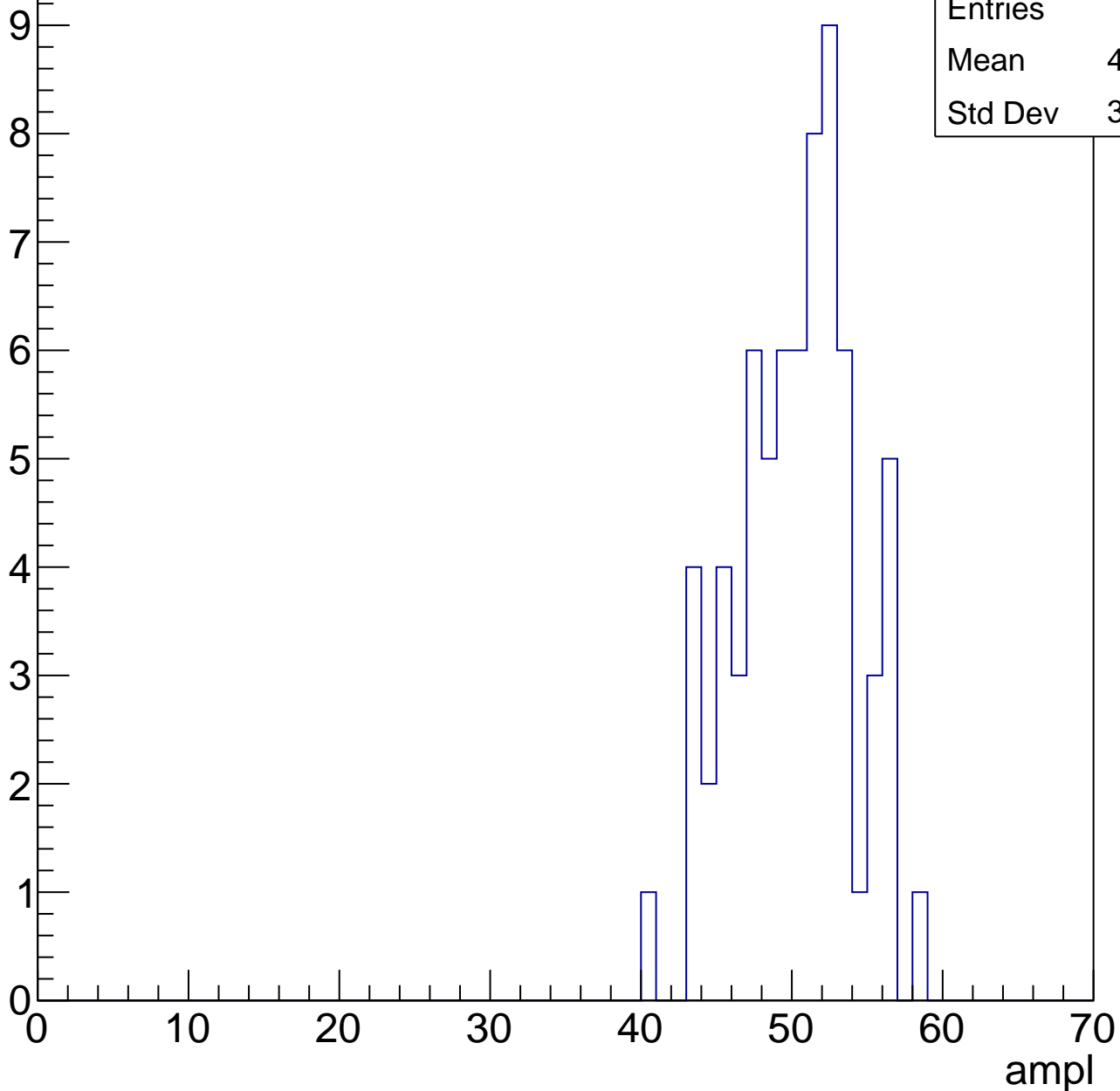


# B1L101S, U16-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	49.79
Std Dev	3.828

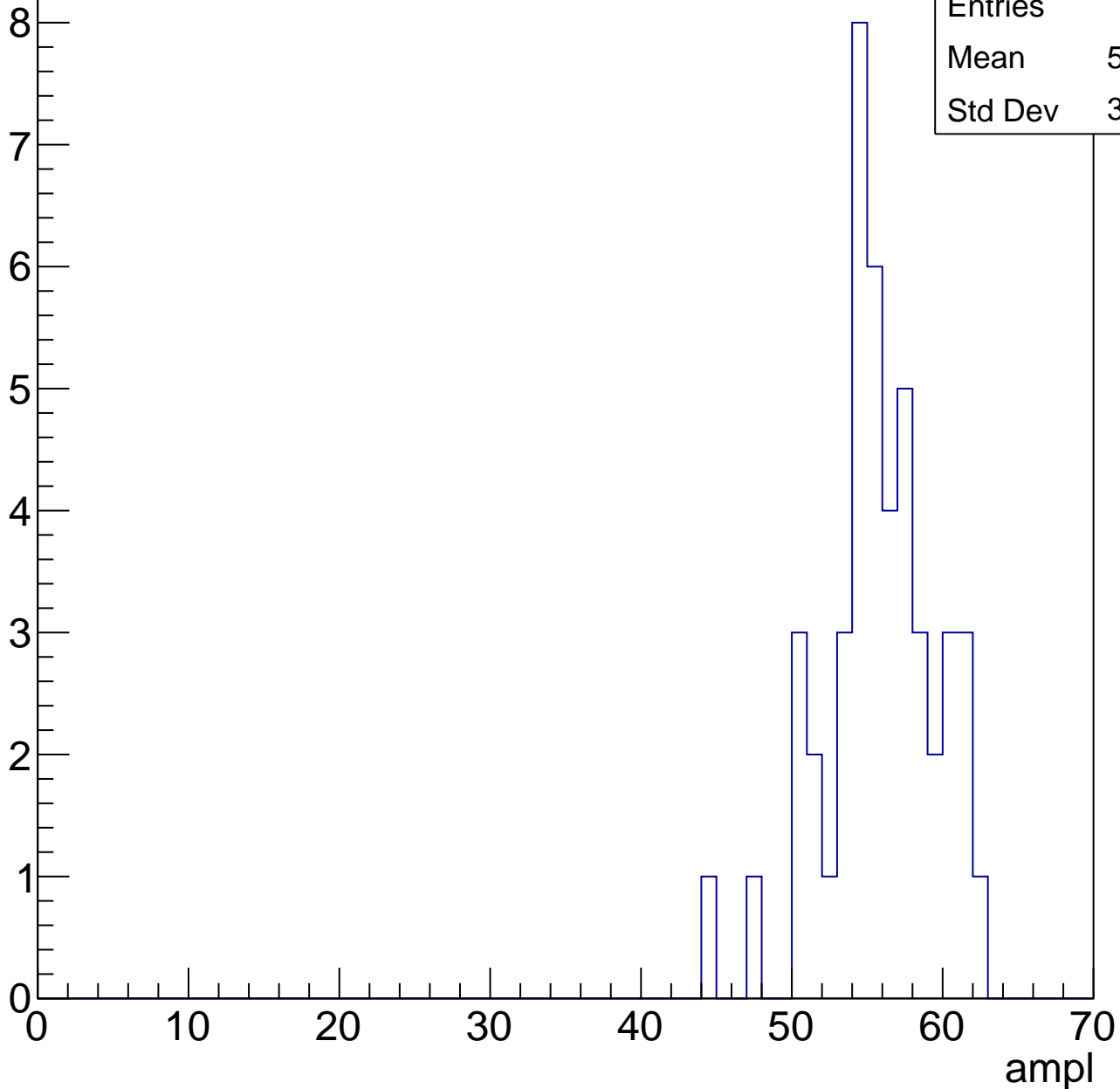


# B1L101S, U16-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	55.26
Std Dev	3.709



# B1L101S, U16-ch118, adc5

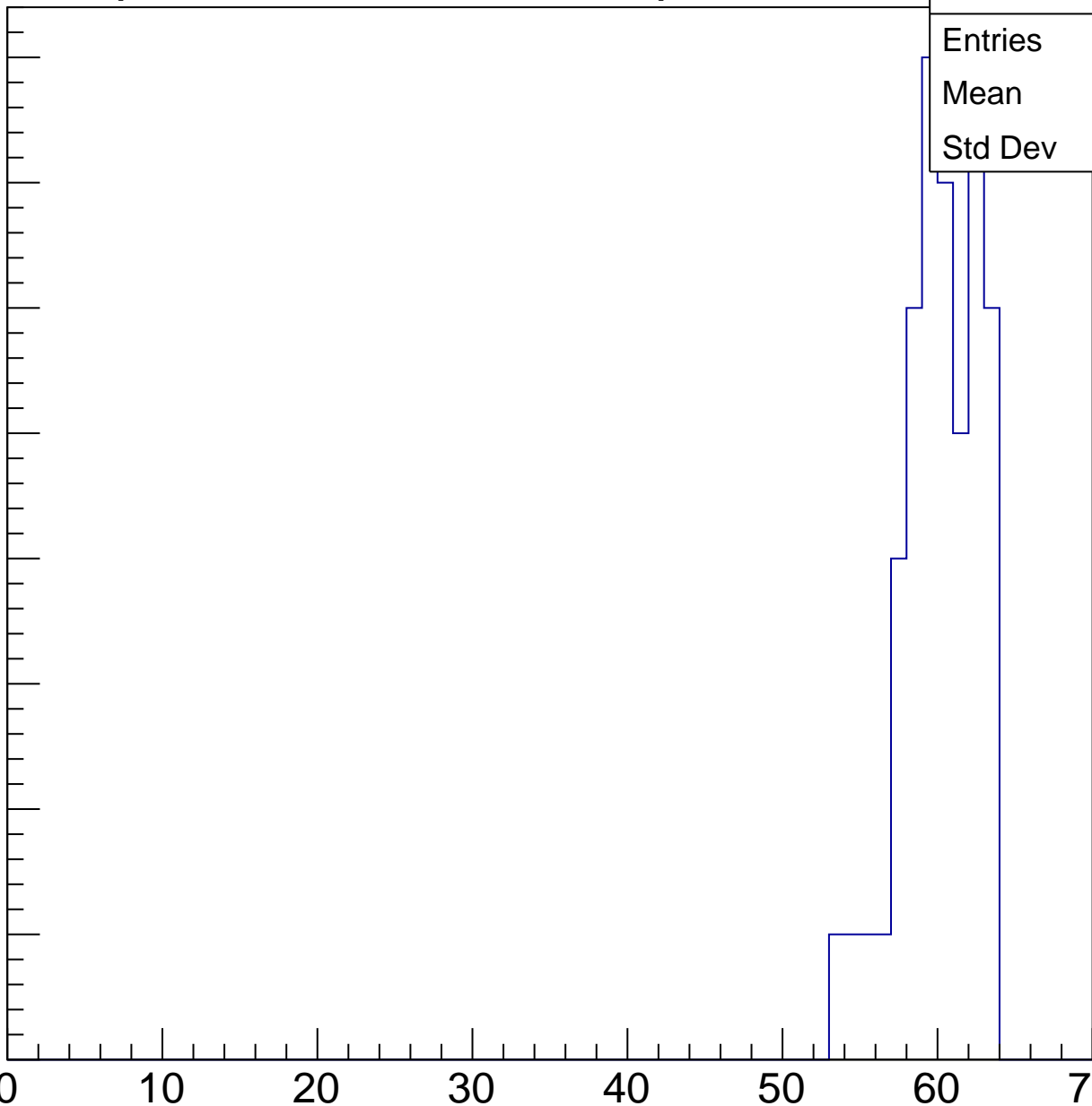
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	59.69
Std Dev	2.417

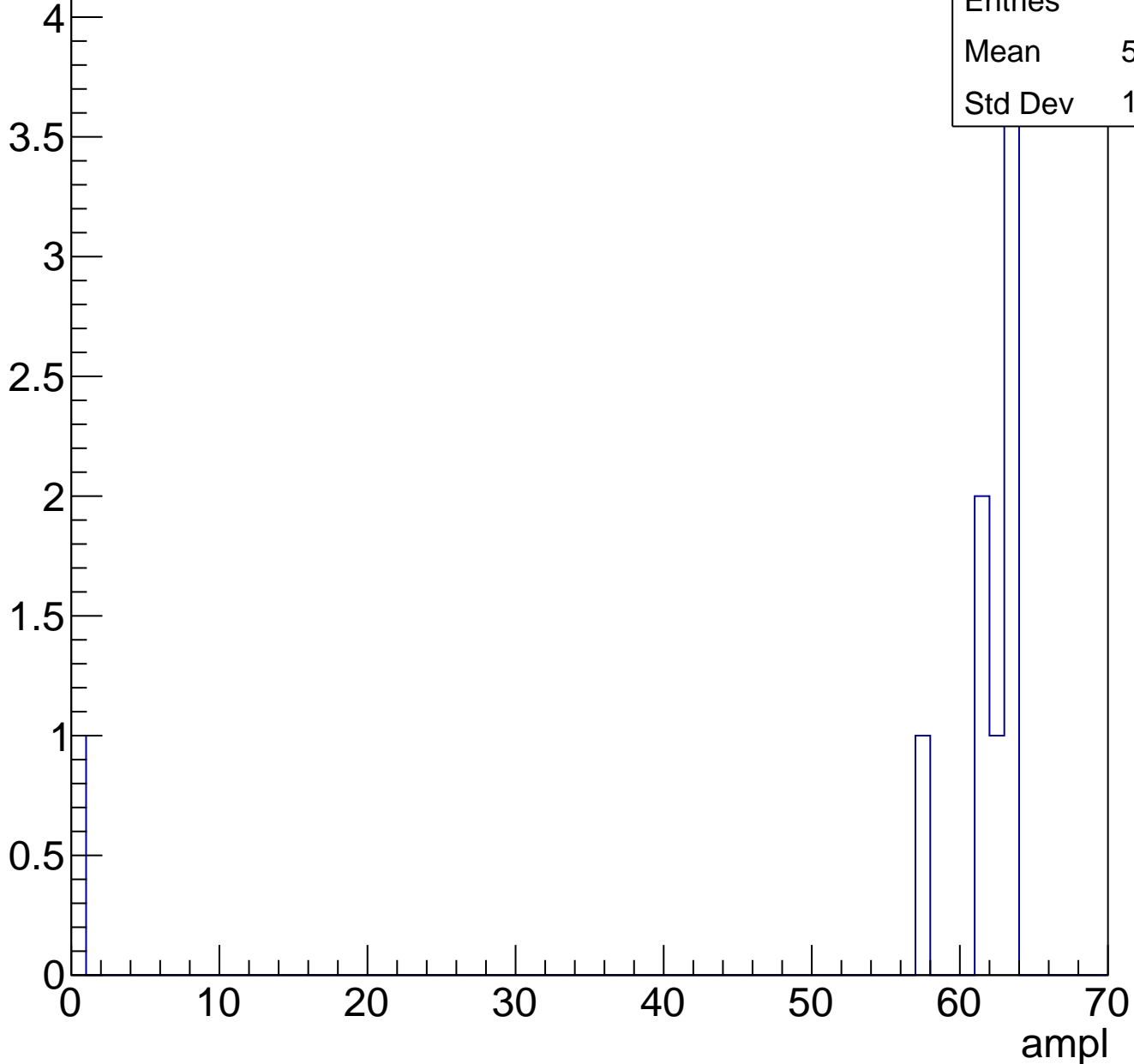
ampl



# B1L101S, U16-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U16-ch119, adc0

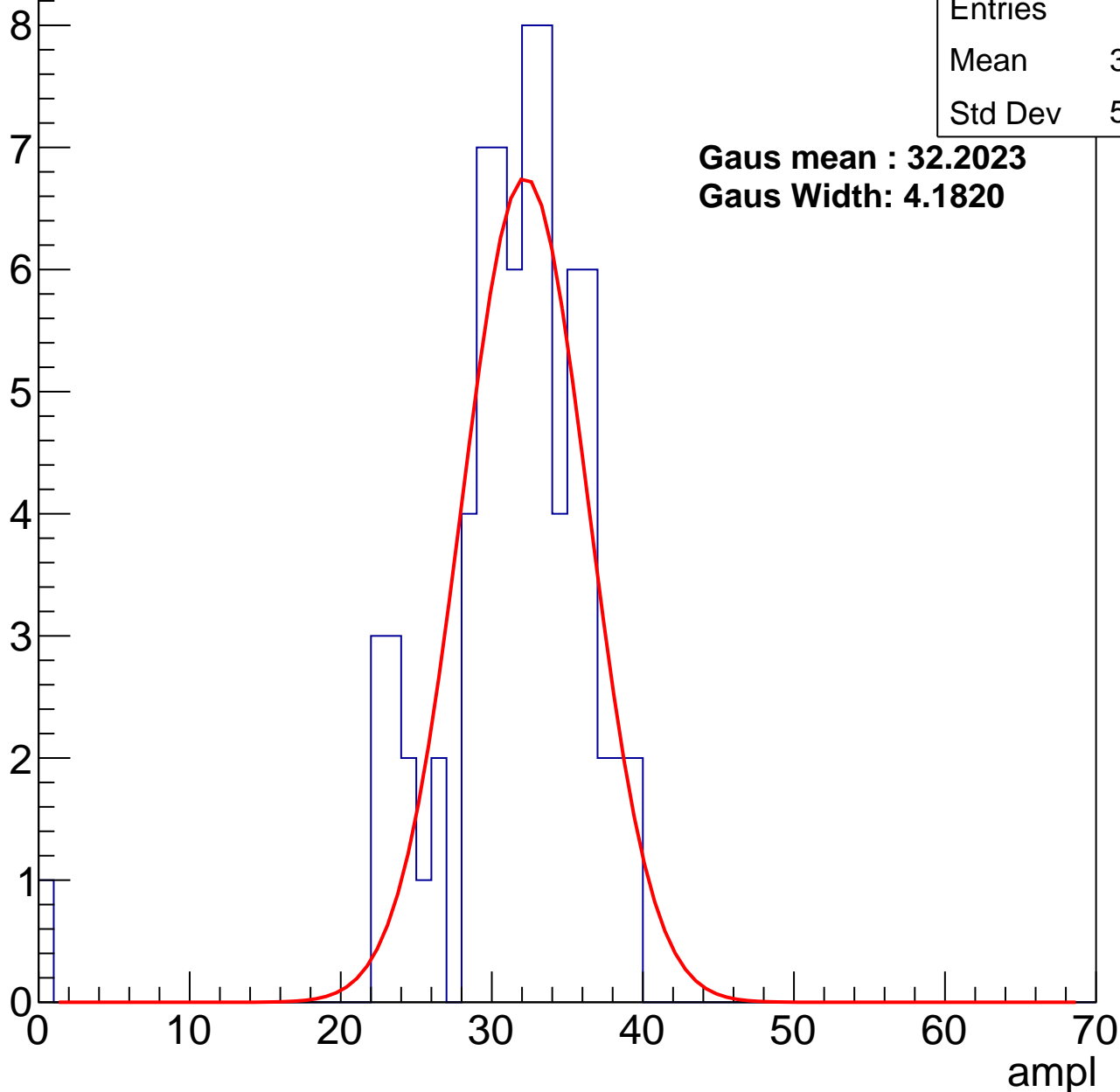
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	30.82
Std Dev	5.537

**Gaus mean : 32.2023**

**Gaus Width: 4.1820**



# B1L101S, U16-ch119, adc1

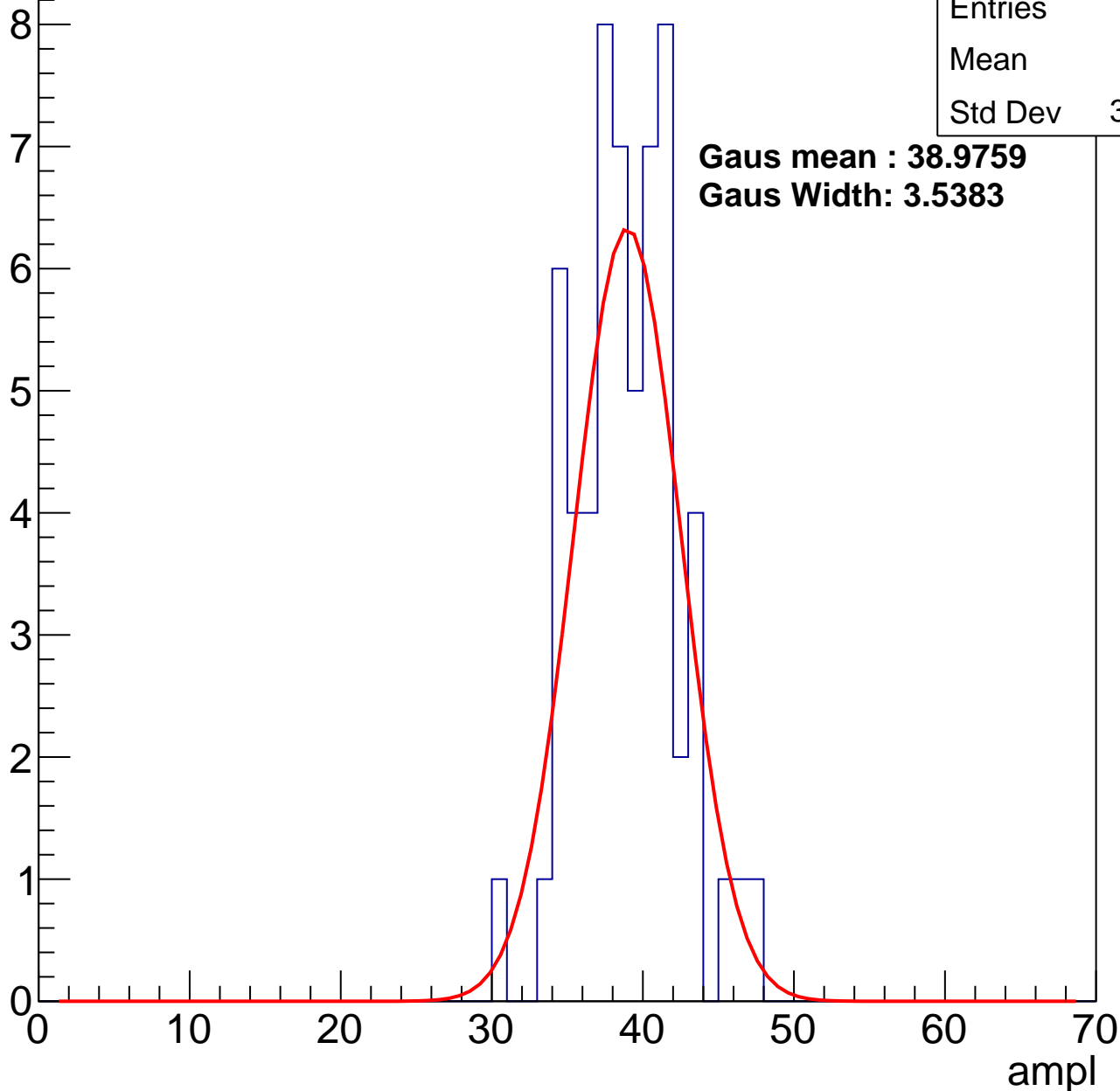
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	38.5
Std Dev	3.319

**Gaus mean : 38.9759**

**Gaus Width: 3.5383**



# B1L101S, U16-ch119, adc2

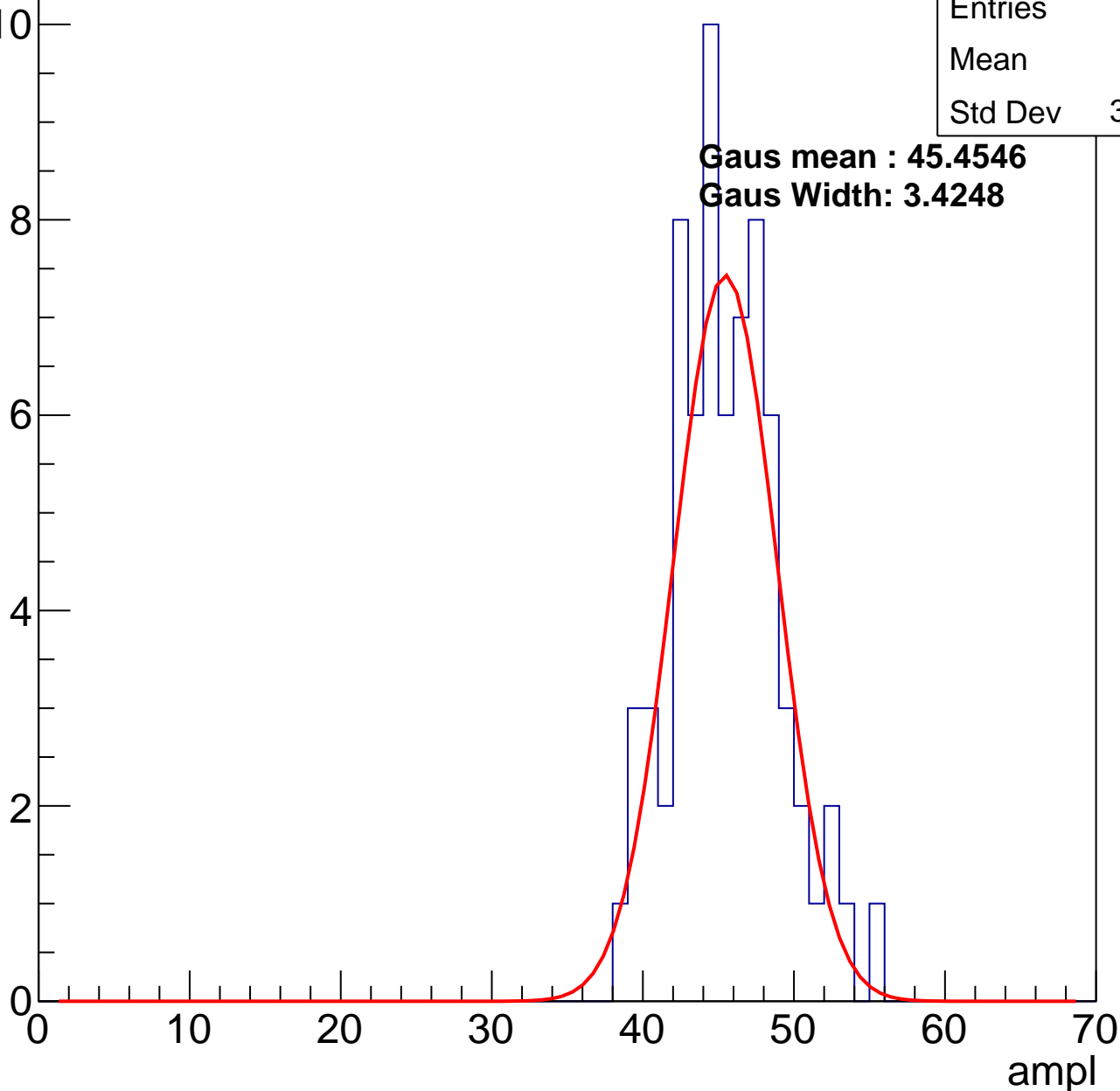
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	45.1
Std Dev	3.502

**Gaus mean : 45.4546**

**Gaus Width: 3.4248**

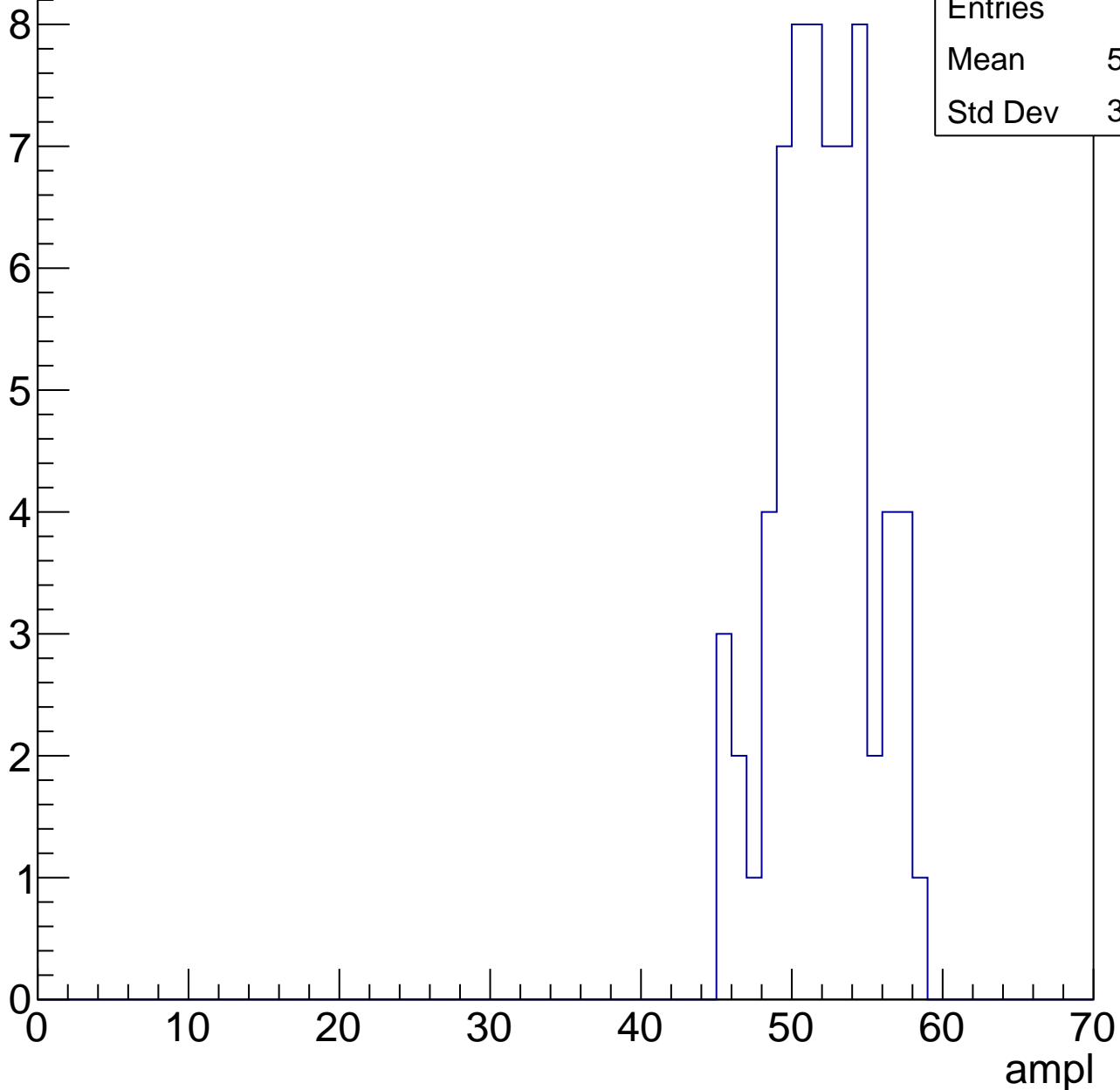


# B1L101S, U16-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	51.58
Std Dev	3.153

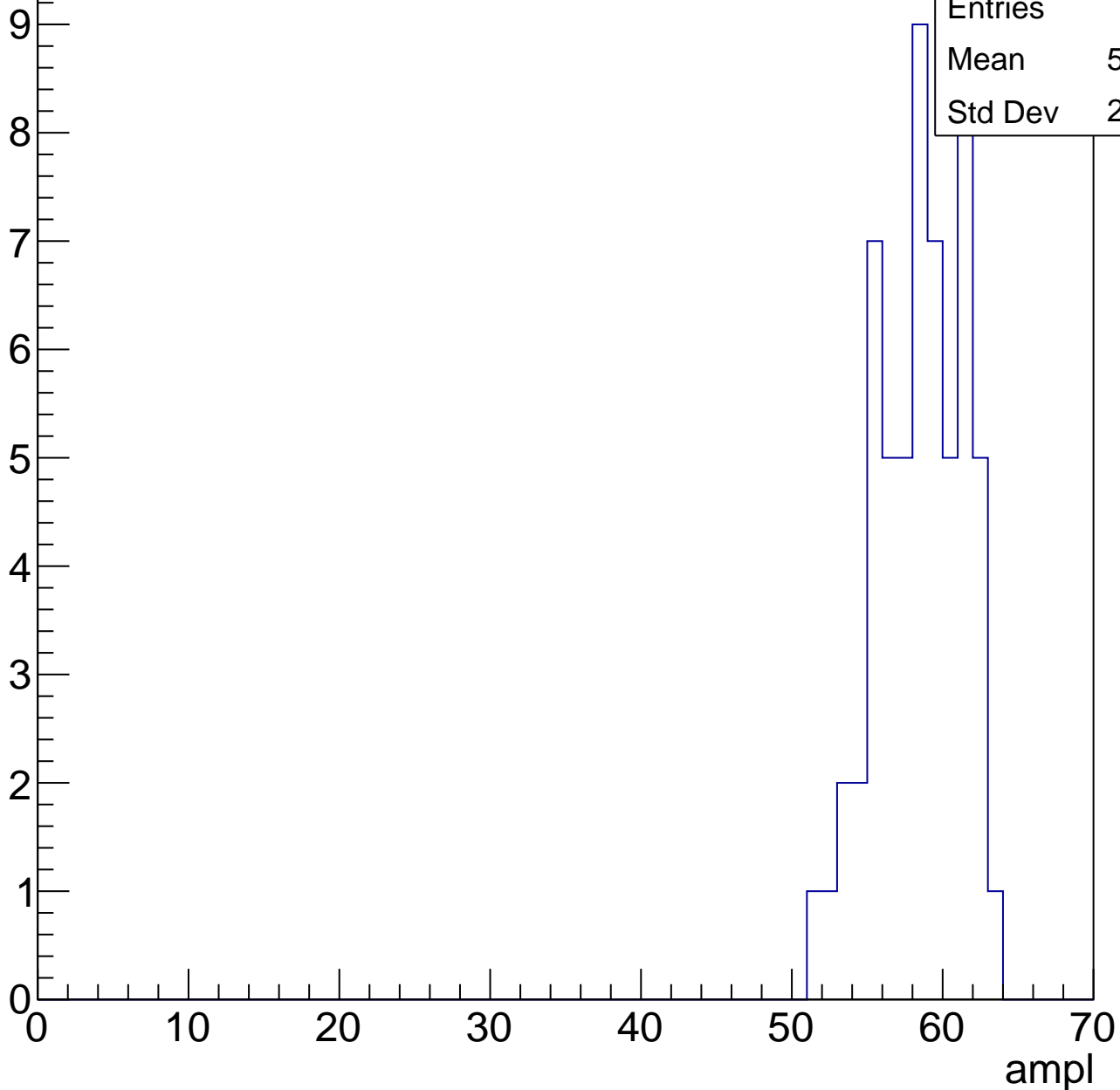


# B1L101S, U16-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	58.03
Std Dev	2.816

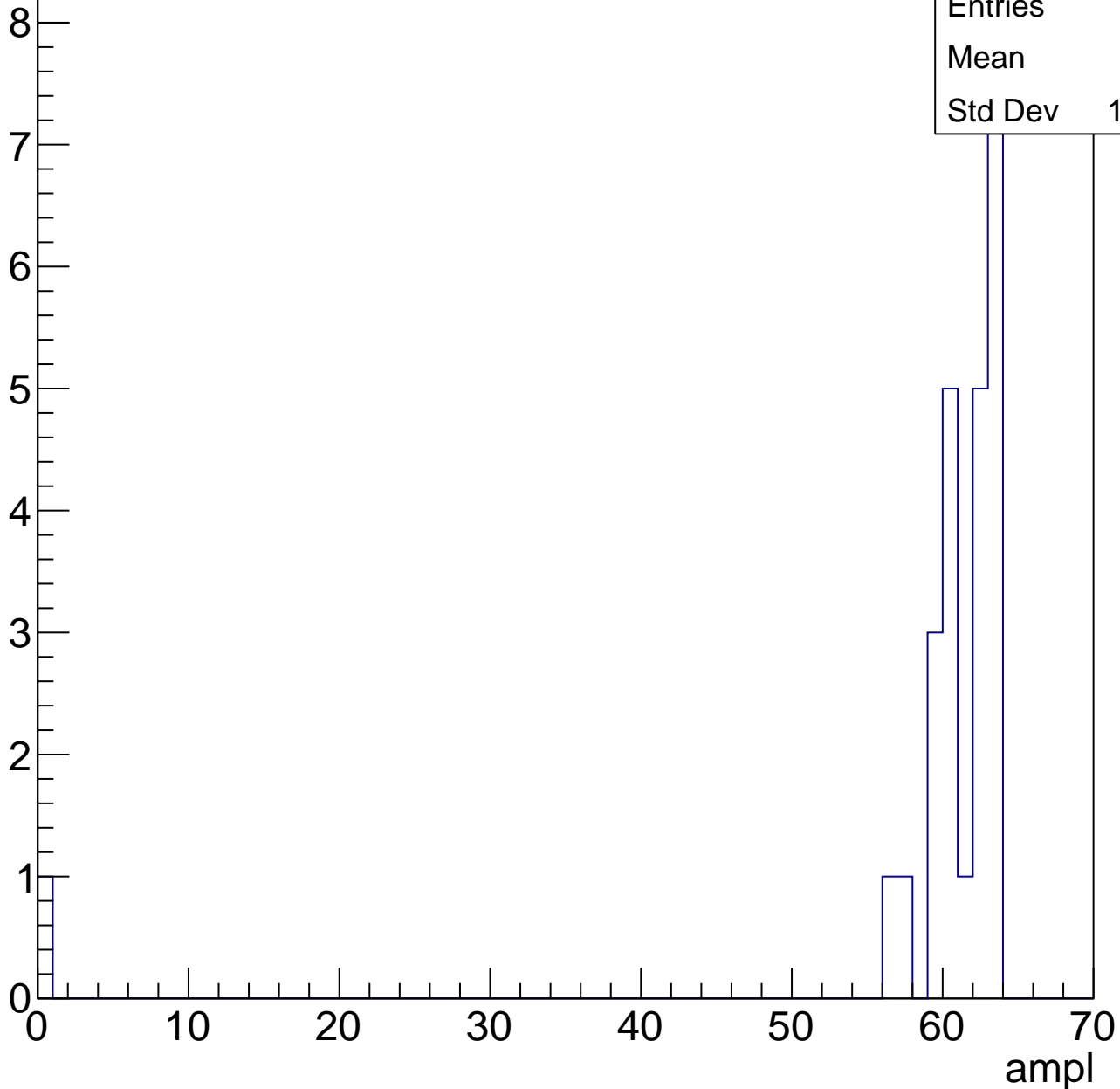


# B1L101S, U16-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	25
Mean	58.6
Std Dev	12.12



# B1L101S, U16-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

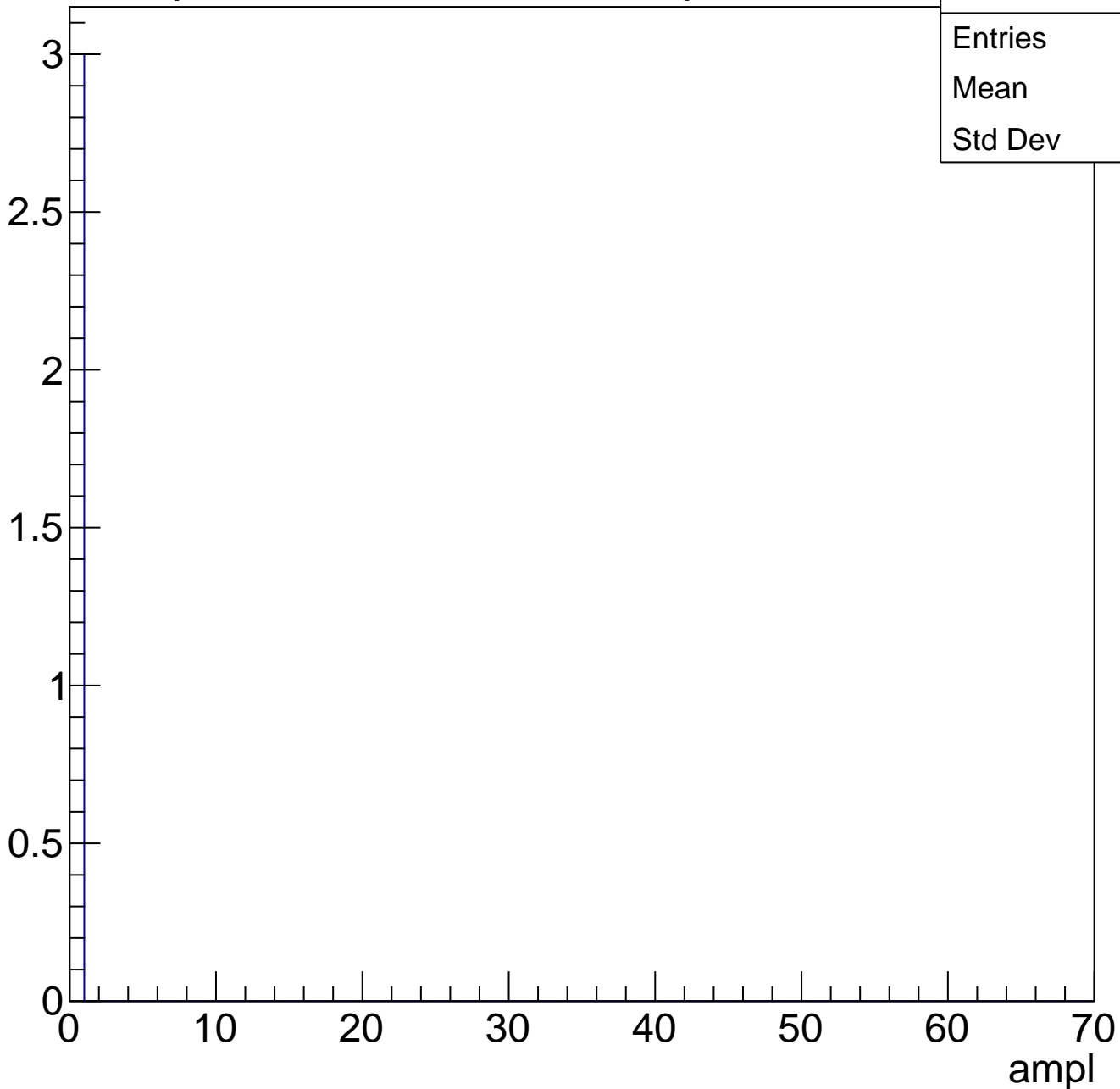




# B1L101S, U16-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U16-ch120, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	94
Mean	28.01
Std Dev	6.696

**Gaus mean : 28.8359**

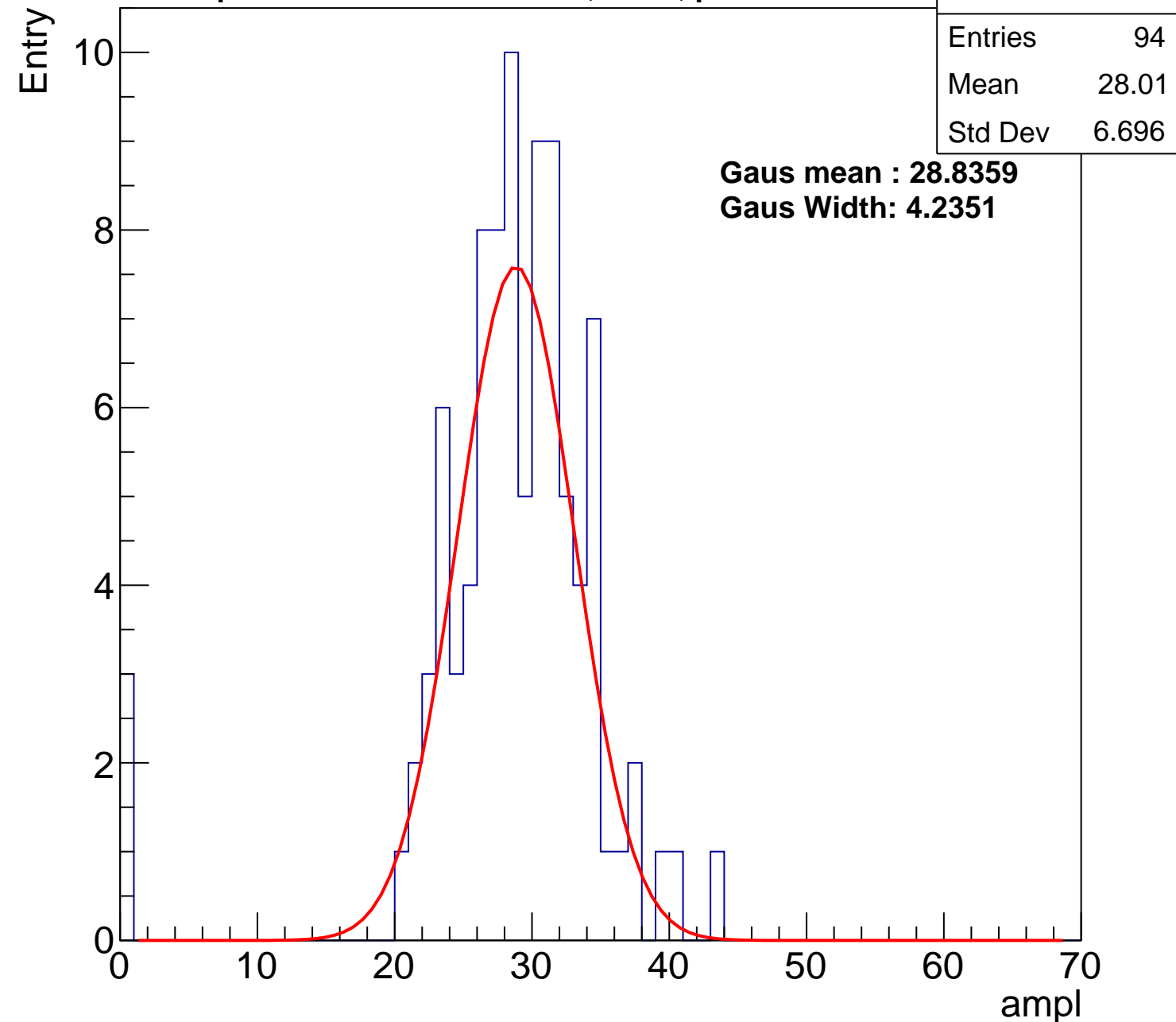
**Gaus Width: 4.2351**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch120, adc1

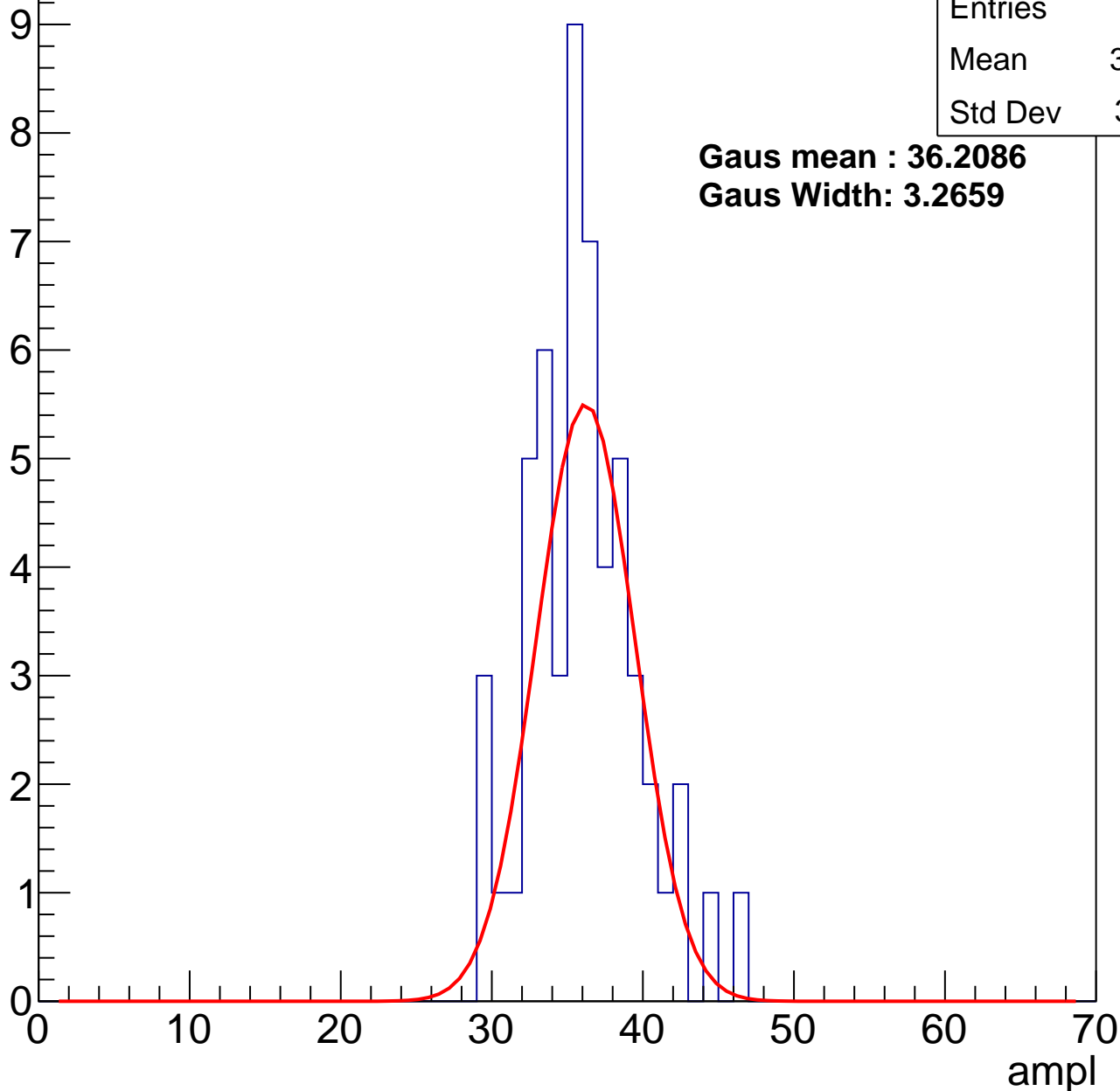
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	35.65
Std Dev	3.601

**Gaus mean : 36.2086**

**Gaus Width: 3.2659**



# B1L101S, U16-ch120, adc2

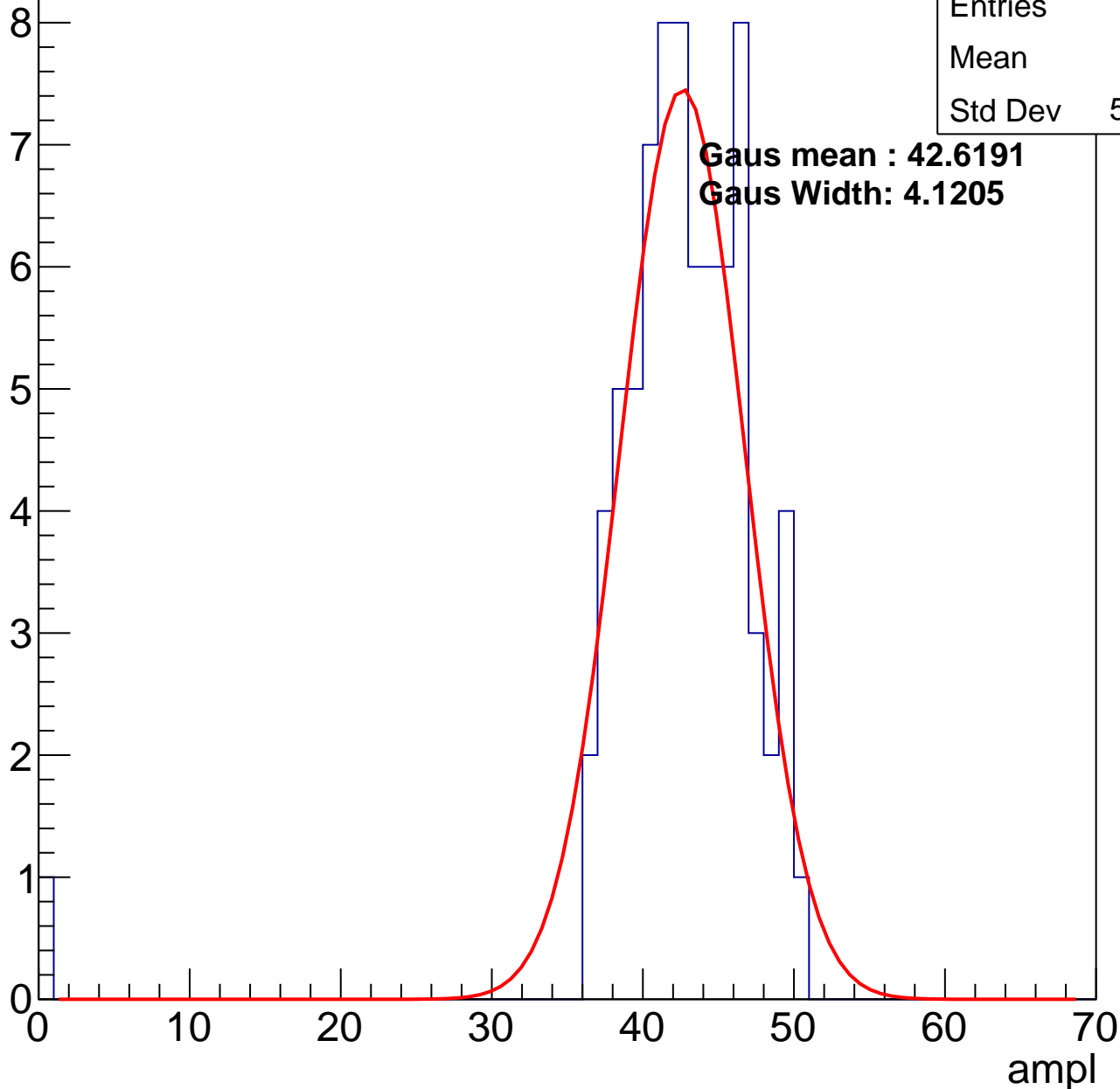
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	42
Std Dev	5.978

**Gaus mean : 42.6191**

**Gaus Width: 4.1205**

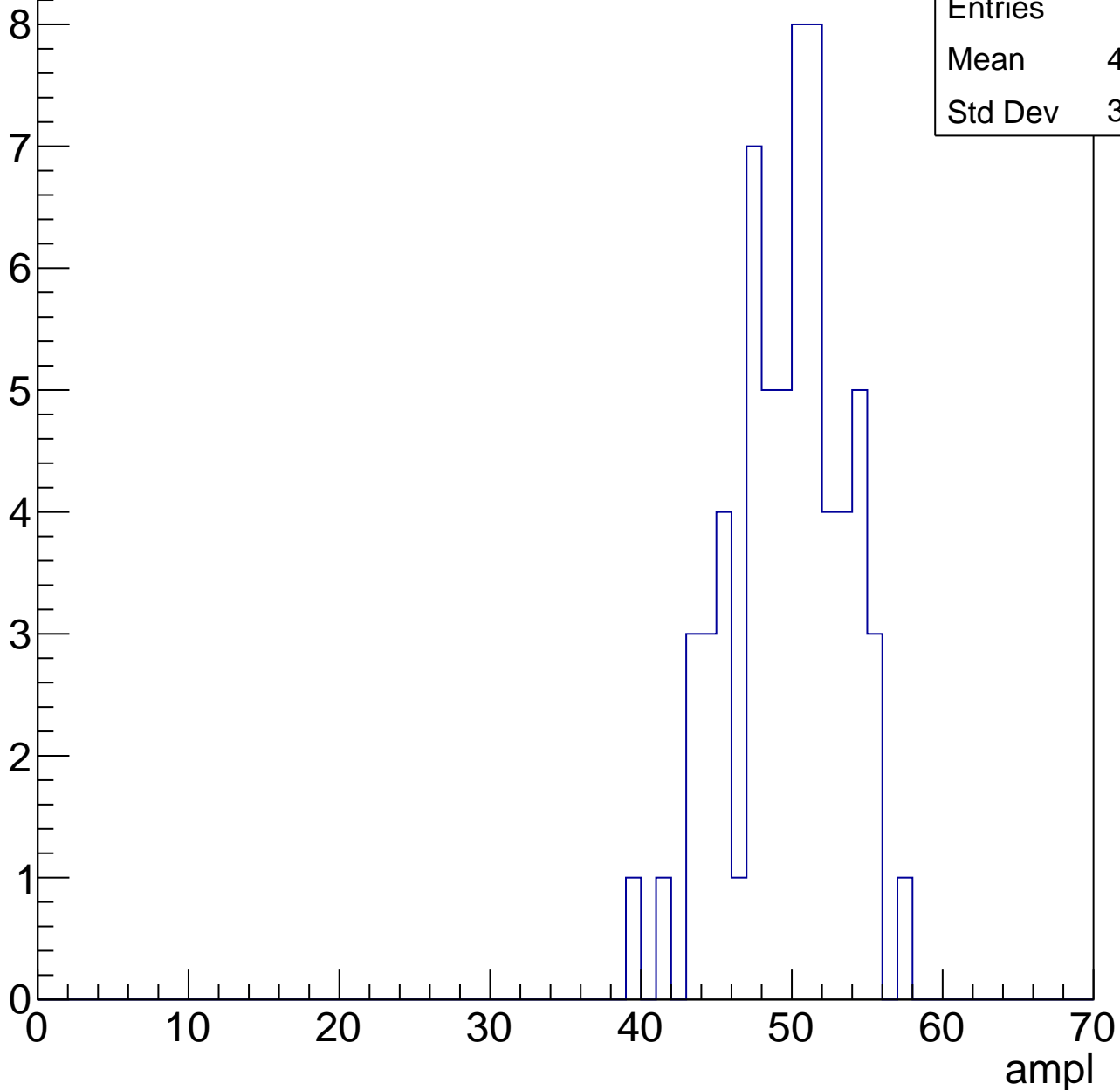


# B1L101S, U16-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	49.22
Std Dev	3.752



# B1L101S, U16-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

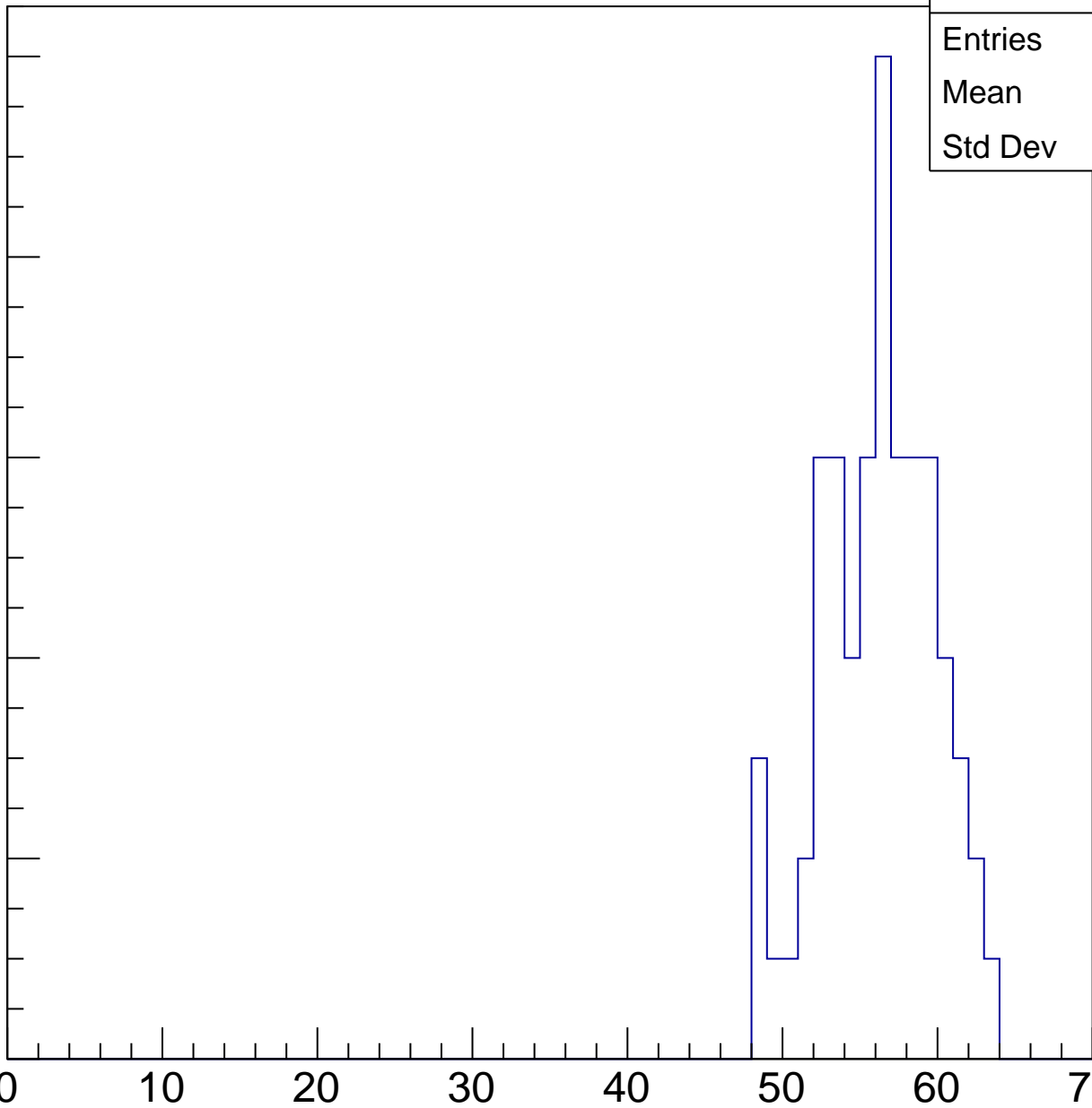
Entries	67
Mean	55.75
Std Dev	3.538

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

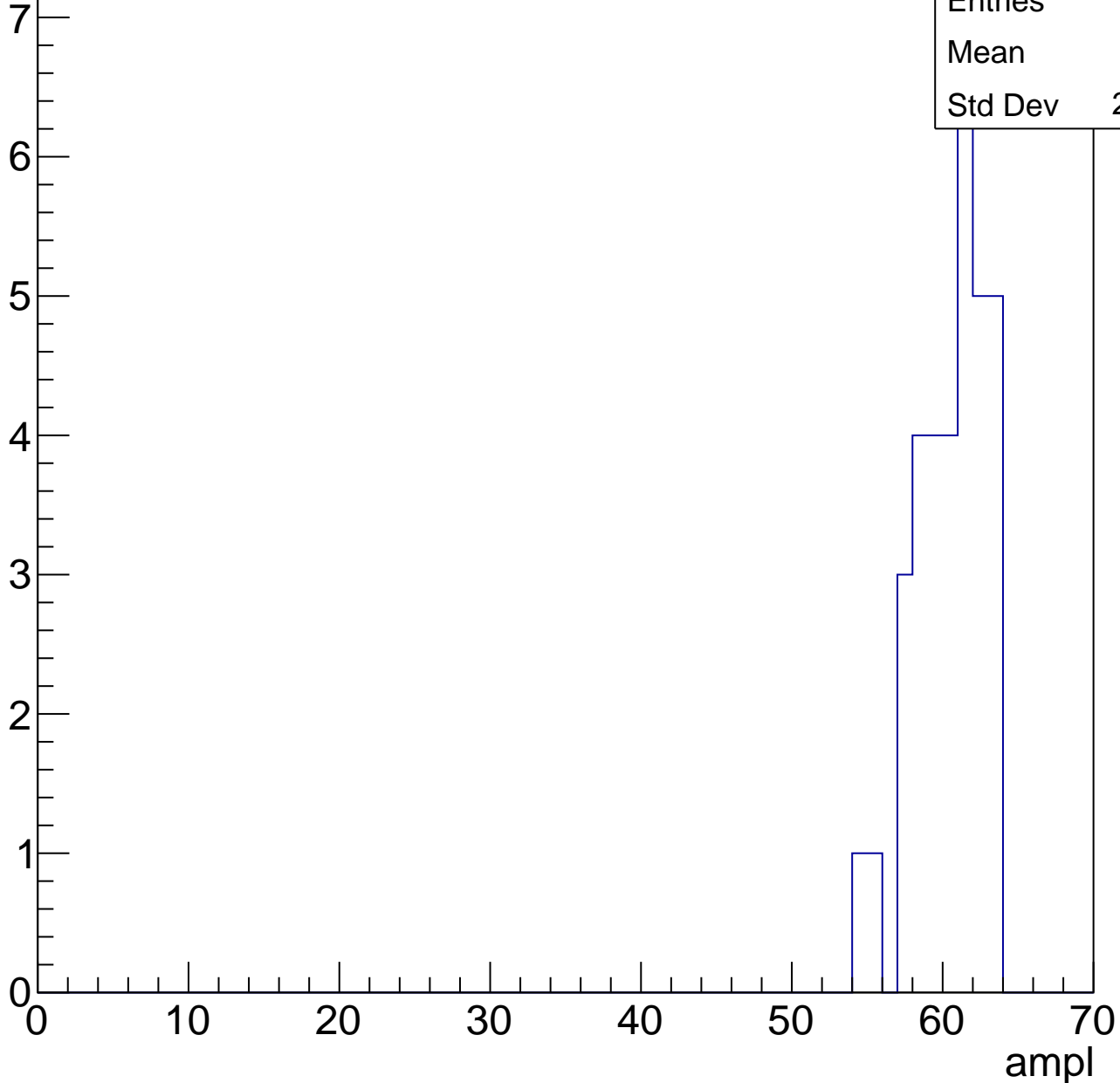


# B1L101S, U16-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

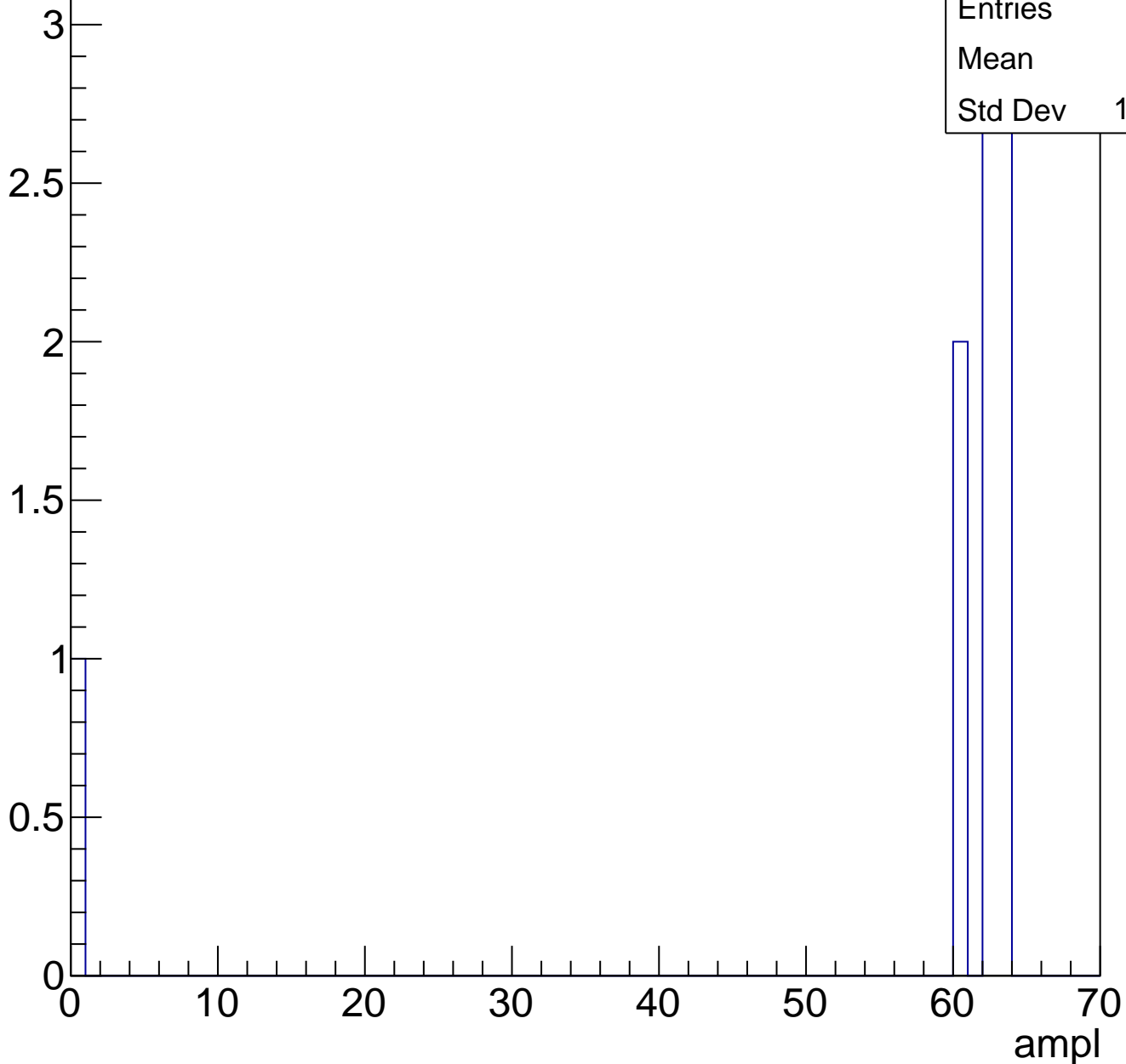
Entries	34
Mean	60
Std Dev	2.301



# B1L101S, U16-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch121, adc0

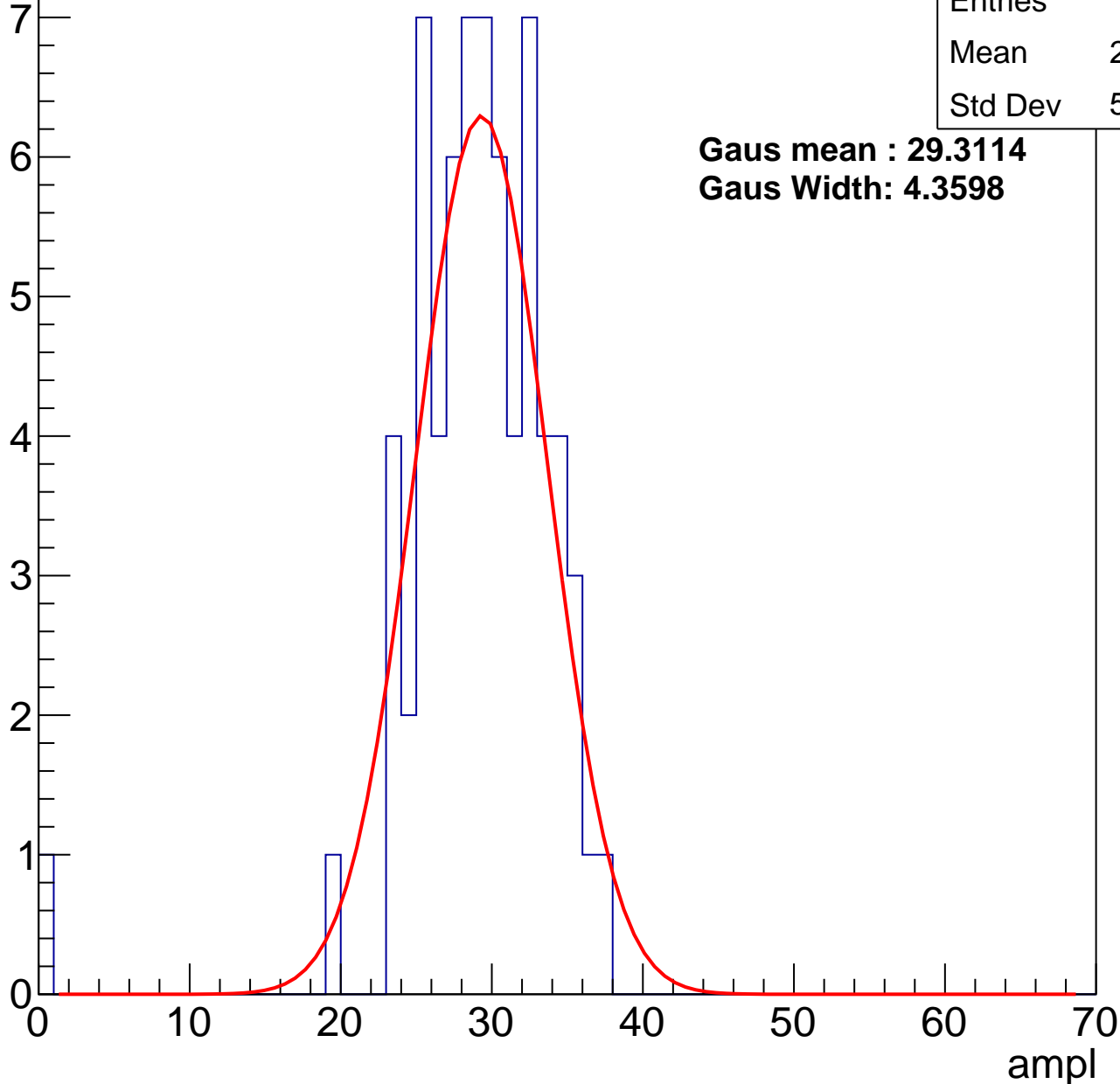
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	28.59
Std Dev	5.069

**Gaus mean : 29.3114**

**Gaus Width: 4.3598**



# B1L101S, U16-ch121, adc1

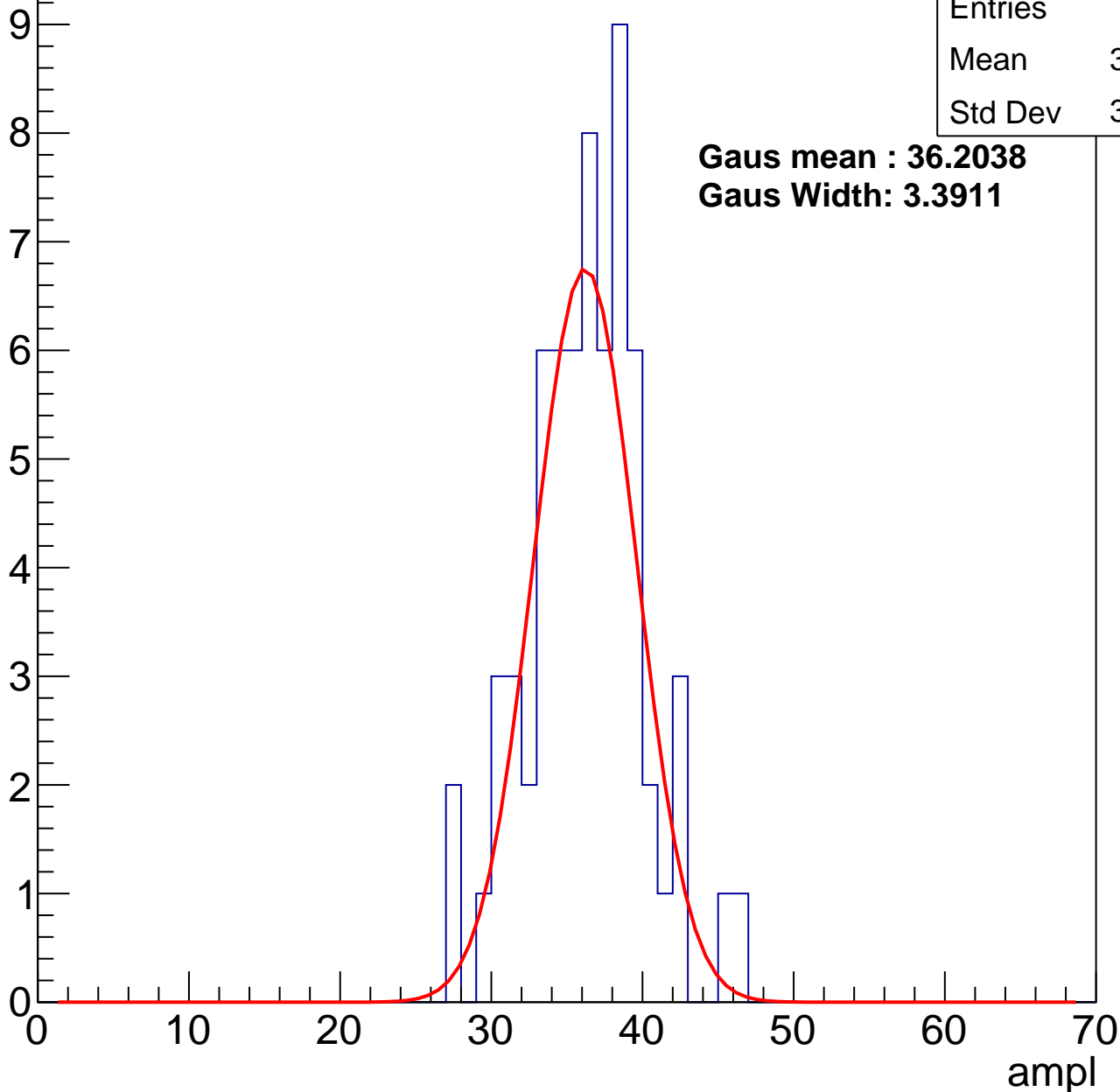
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	35.85
Std Dev	3.795

**Gaus mean : 36.2038**

**Gaus Width: 3.3911**



# B1L101S, U16-ch121, adc2

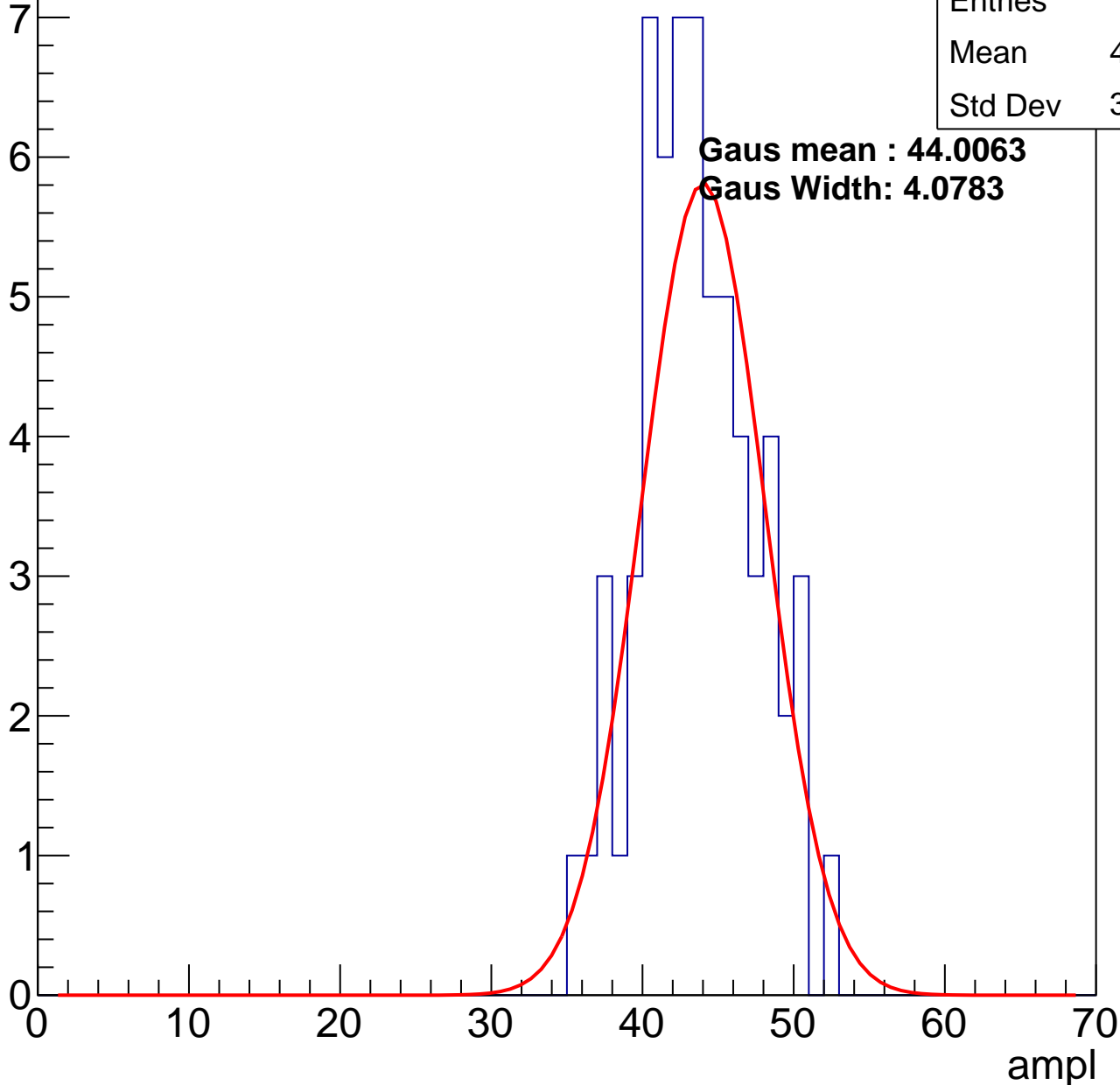
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	43.17
Std Dev	3.769

**Gaus mean : 44.0063**

**Gaus Width: 4.0783**

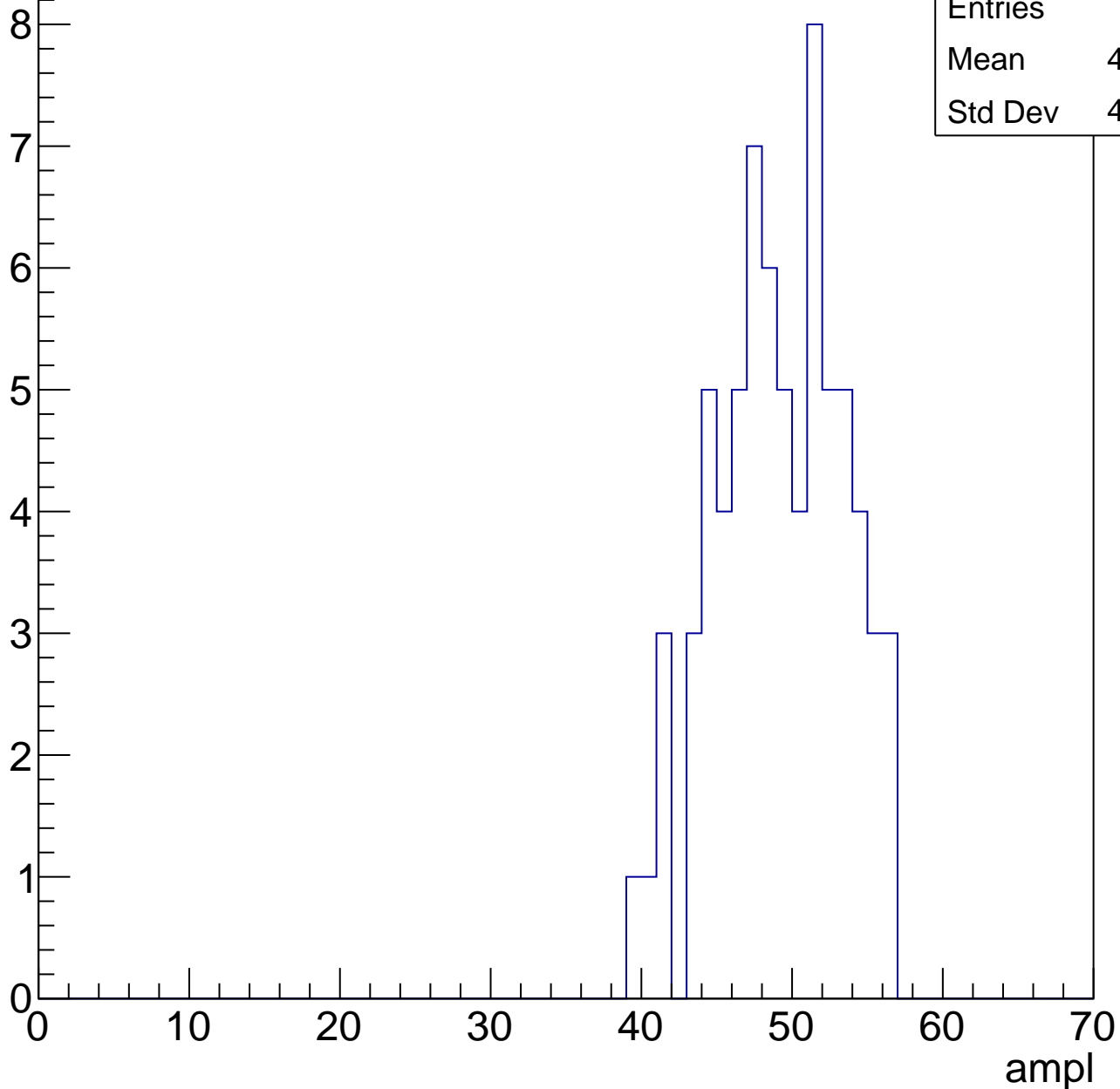


# B1L101S, U16-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	48.68
Std Dev	4.179

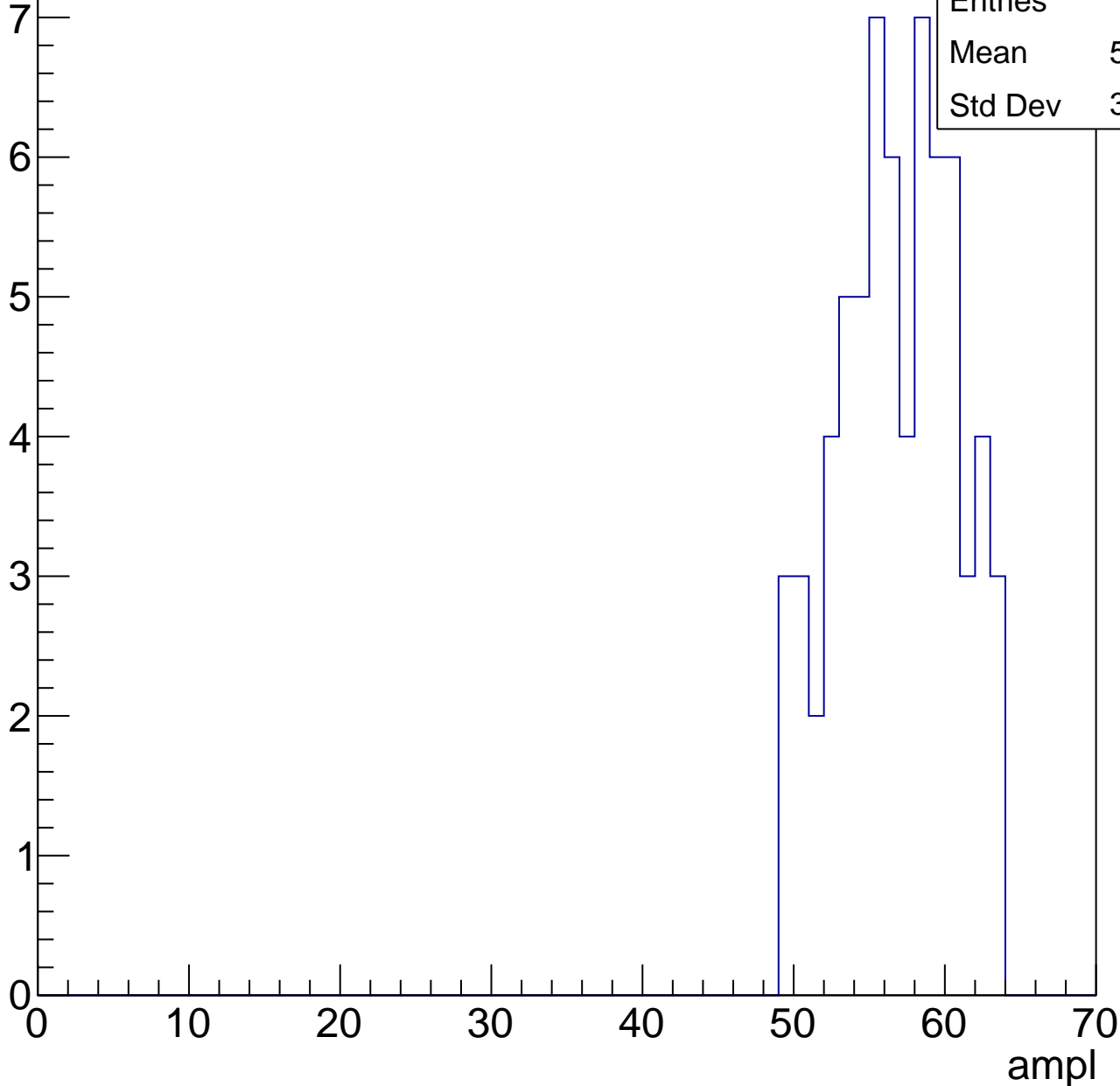


# B1L101S, U16-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	56.34
Std Dev	3.799

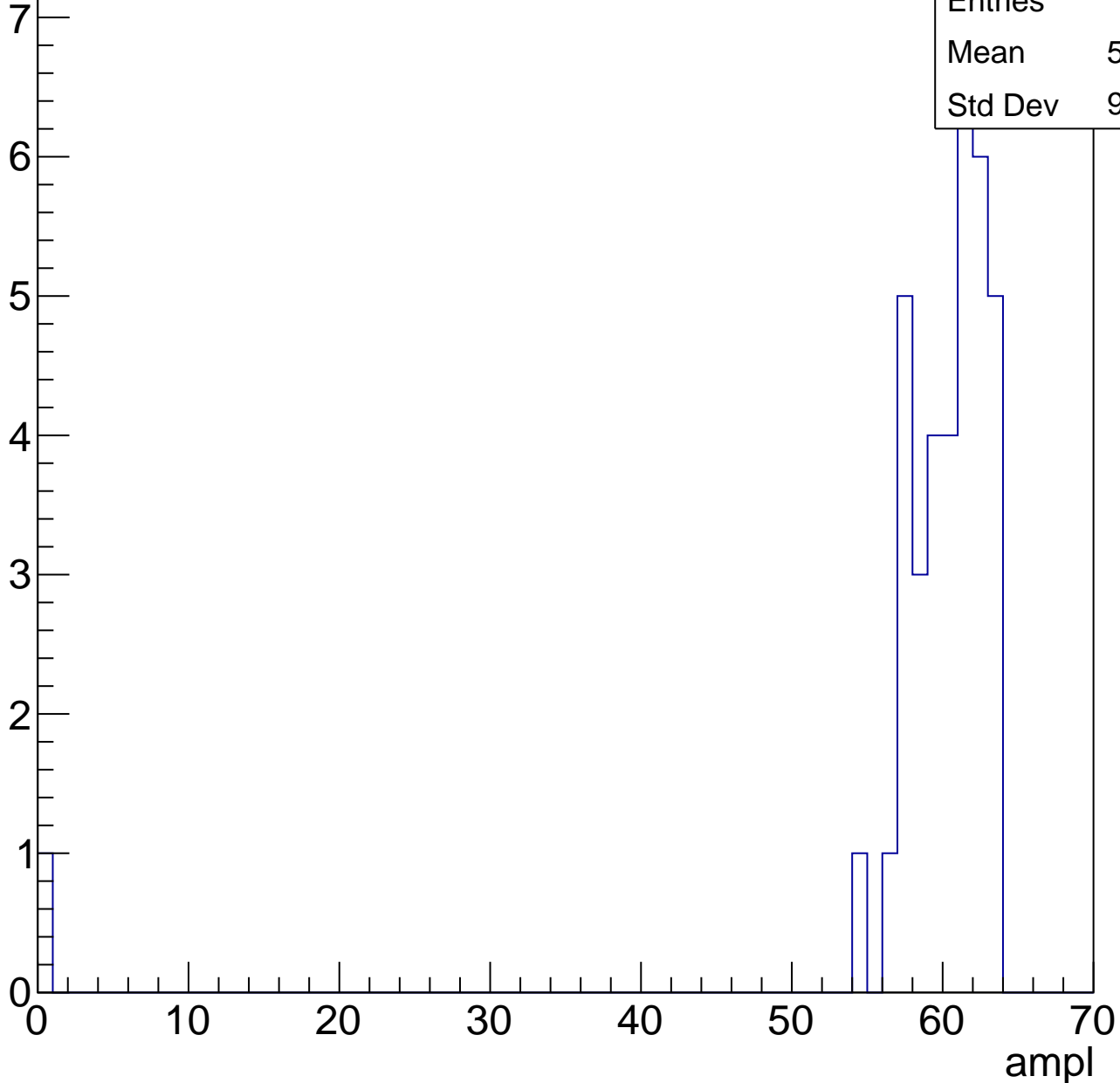


# B1L101S, U16-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

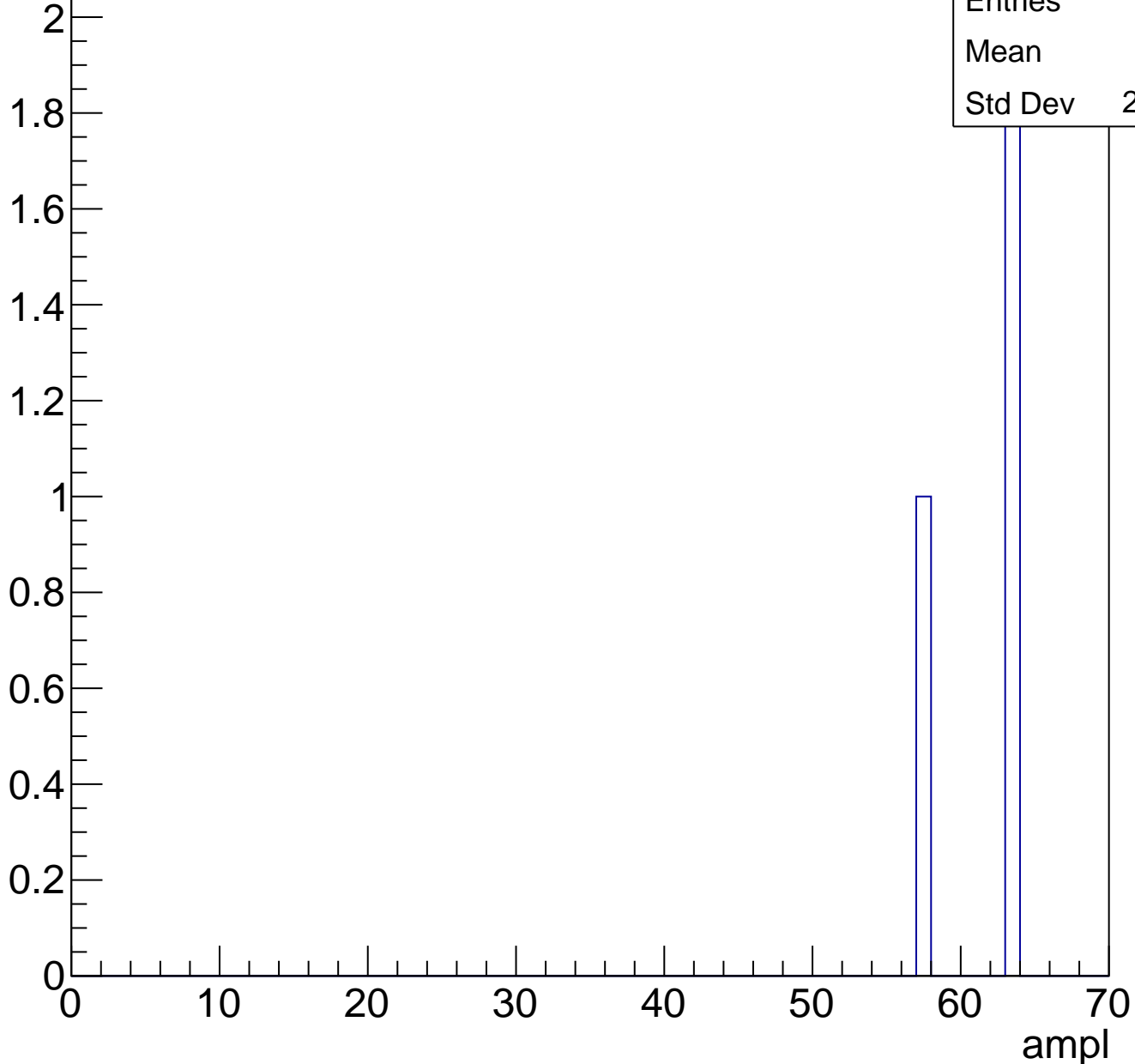
Entries	37
Mean	58.35
Std Dev	9.984



# B1L101S, U16-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U16-ch122, adc0

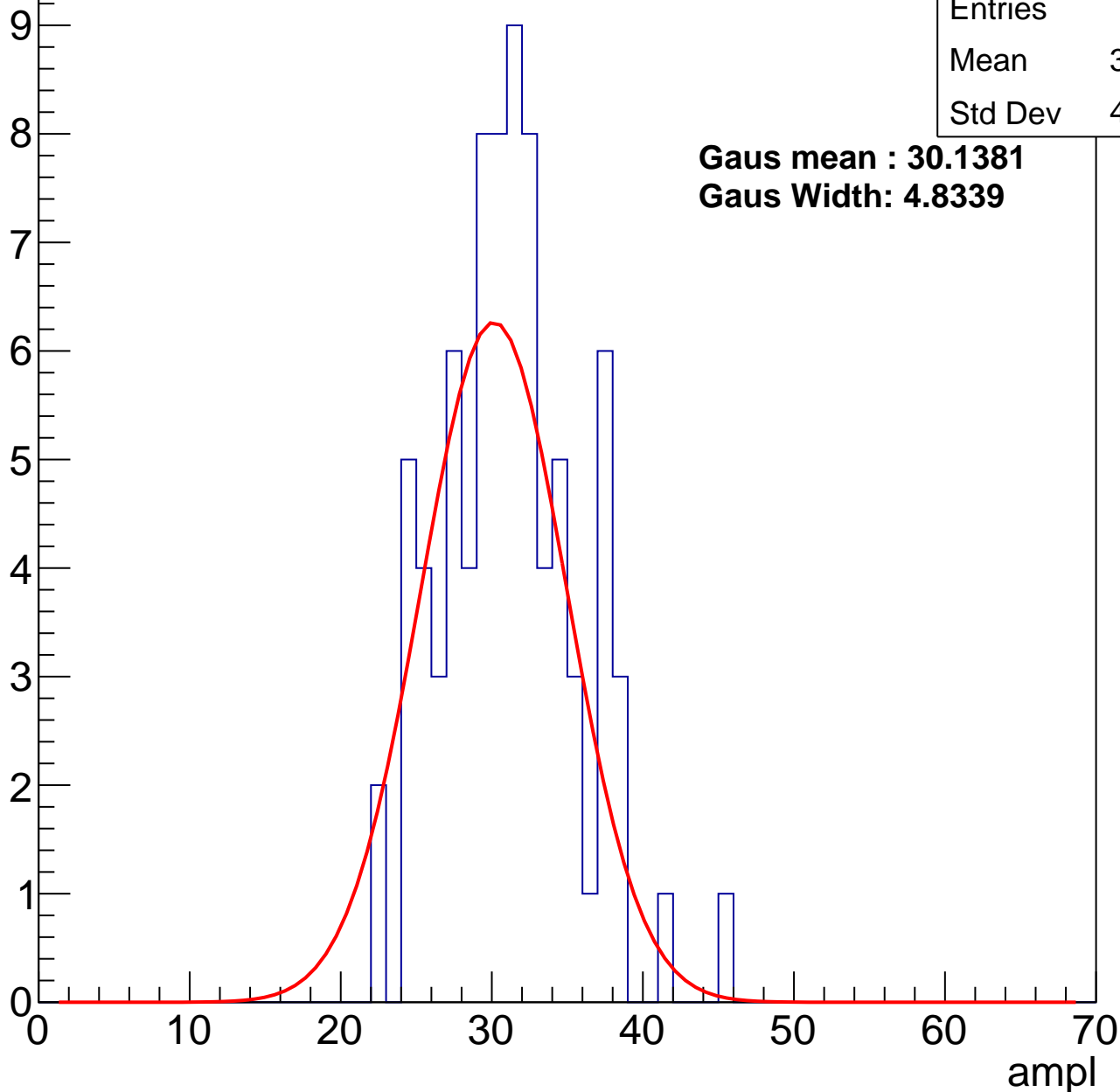
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	30.72
Std Dev	4.434

**Gaus mean : 30.1381**

**Gaus Width: 4.8339**



# B1L101S, U16-ch122, adc1

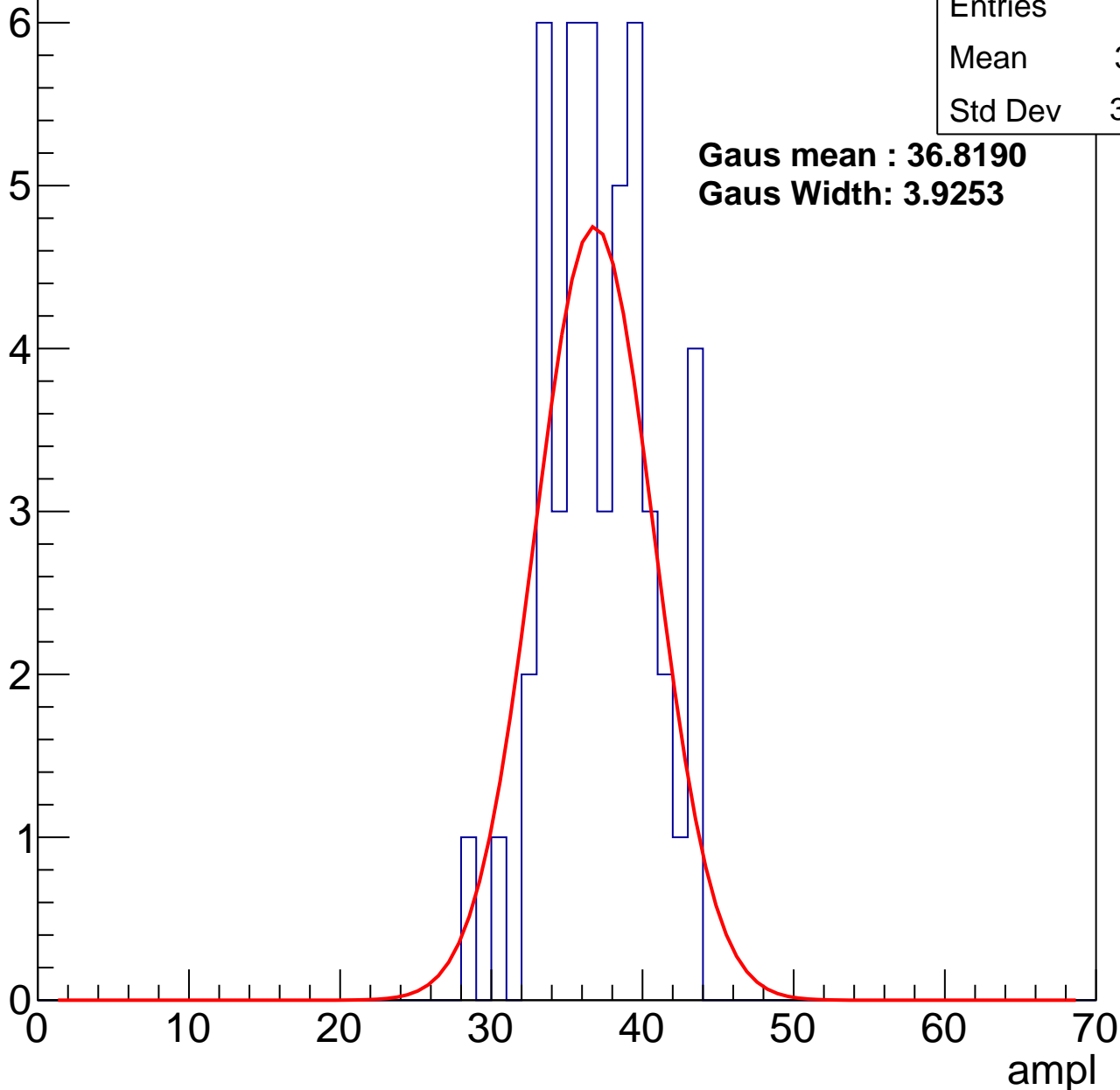
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	36.71
Std Dev	3.458

**Gaus mean : 36.8190**

**Gaus Width: 3.9253**



# B1L101S, U16-ch122, adc2

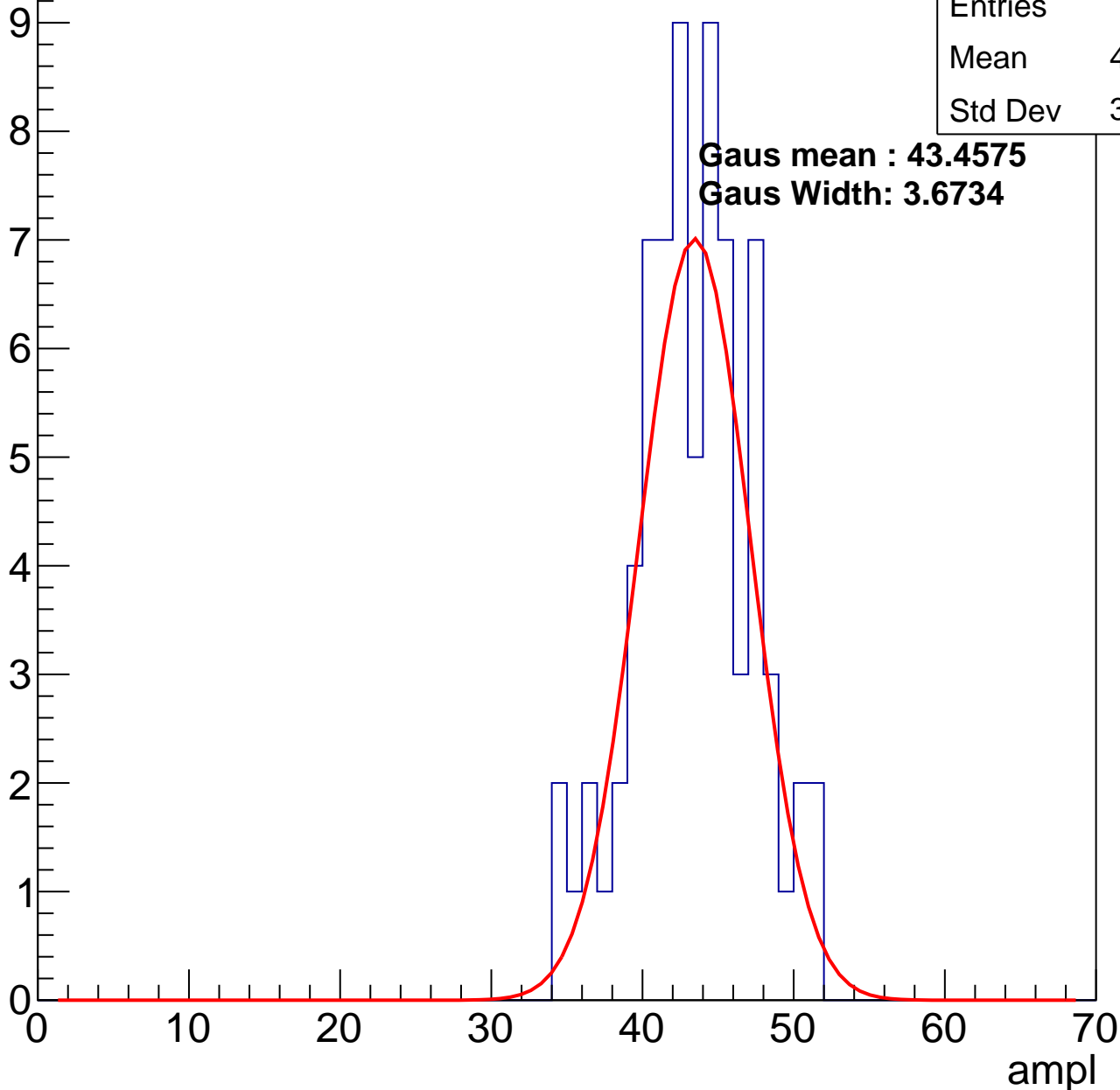
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	42.93
Std Dev	3.832

**Gaus mean : 43.4575**

**Gaus Width: 3.6734**

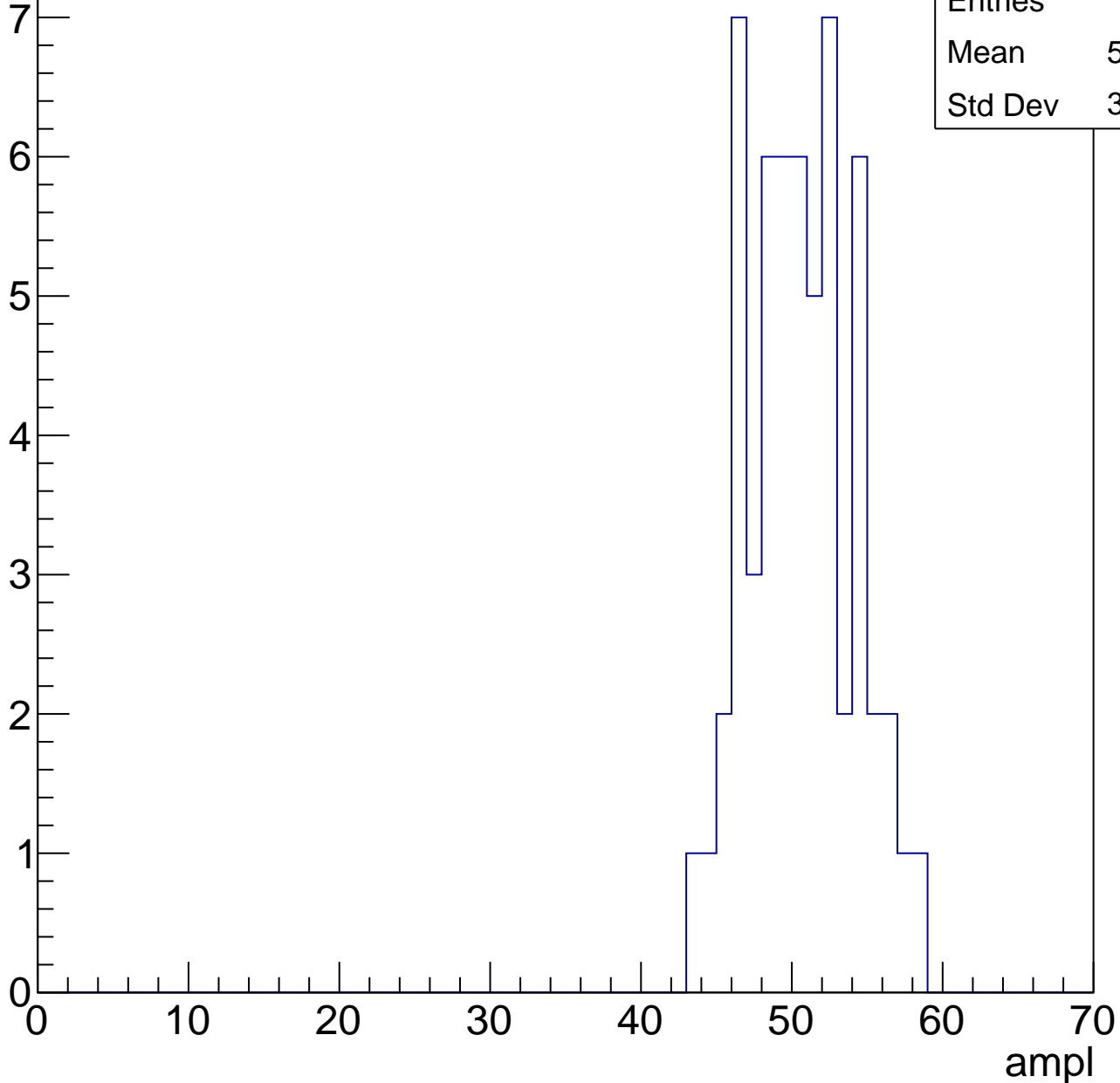


# B1L101S, U16-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	50.14
Std Dev	3.436

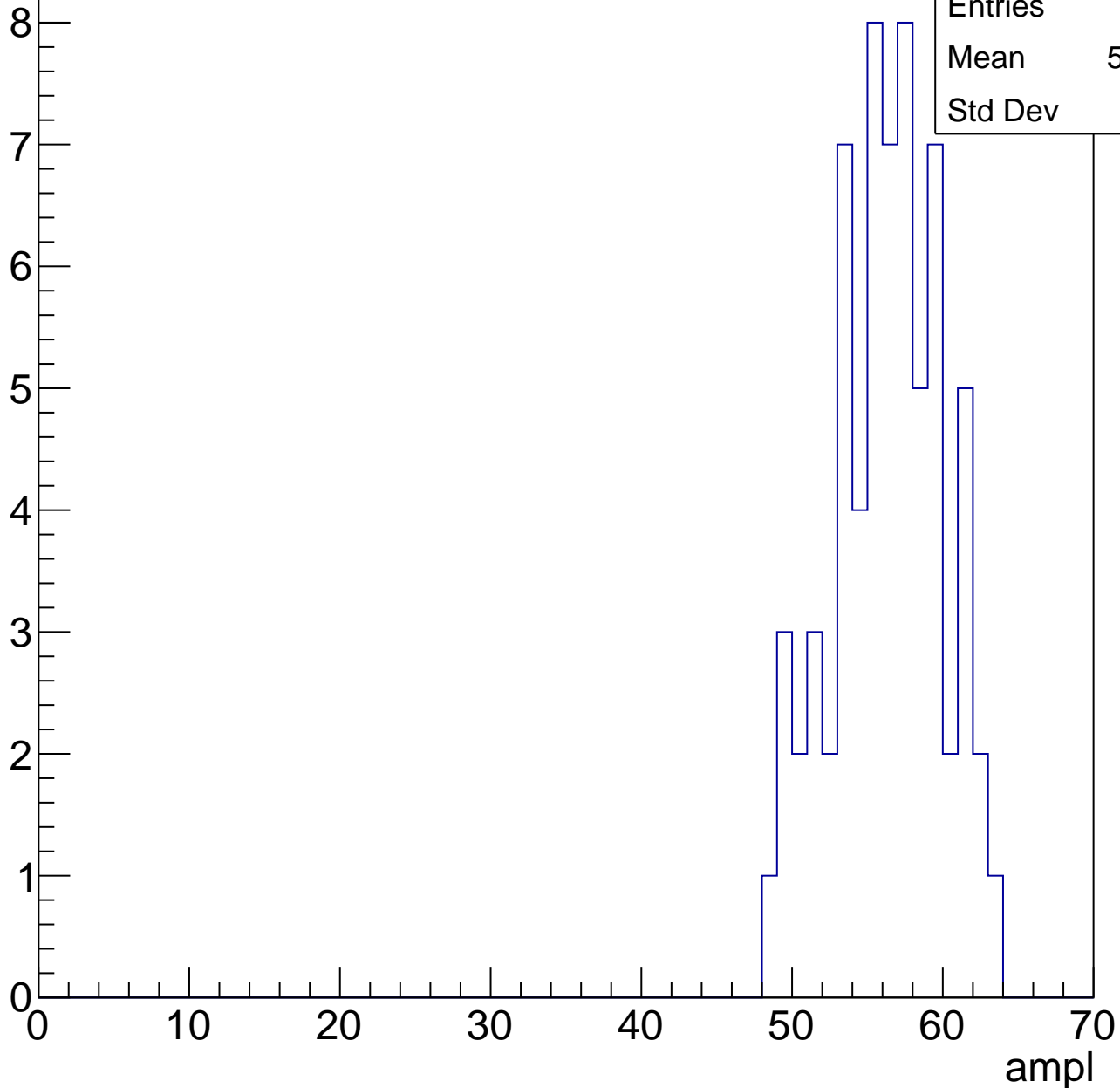


# B1L101S, U16-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	55.85
Std Dev	3.55

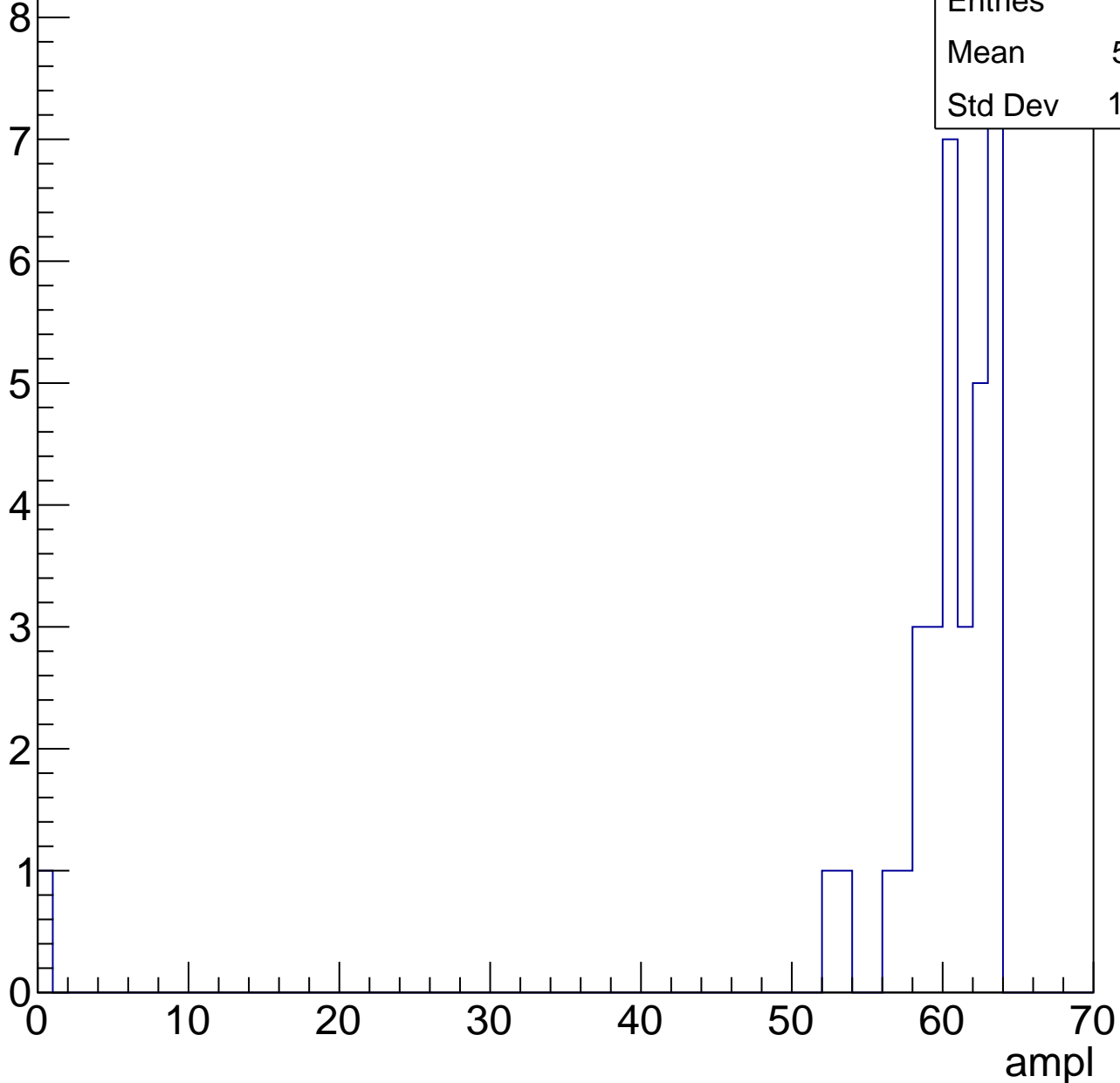


# B1L101S, U16-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

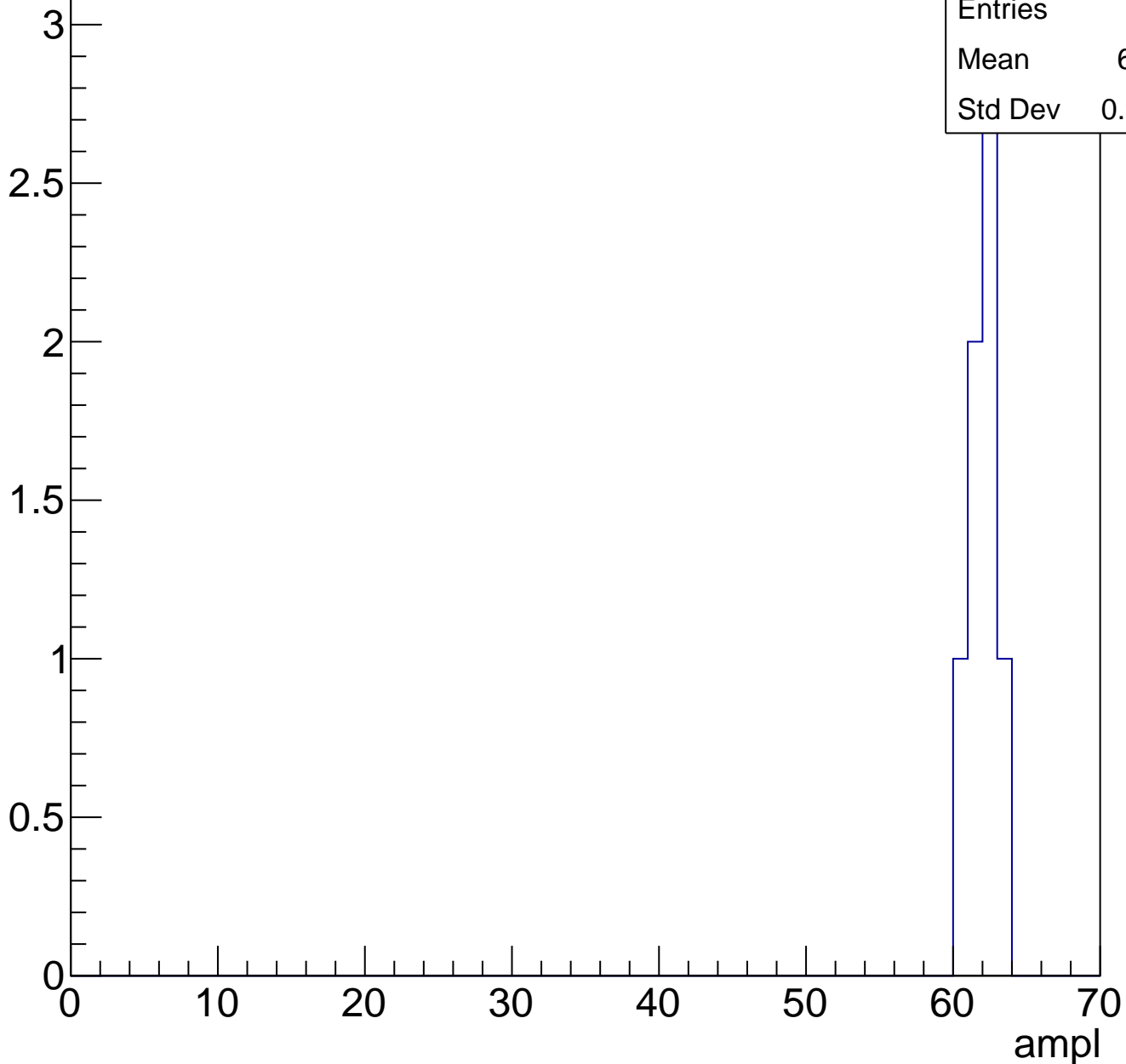
Entries	34
Mean	58.41
Std Dev	10.52



# B1L101S, U16-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

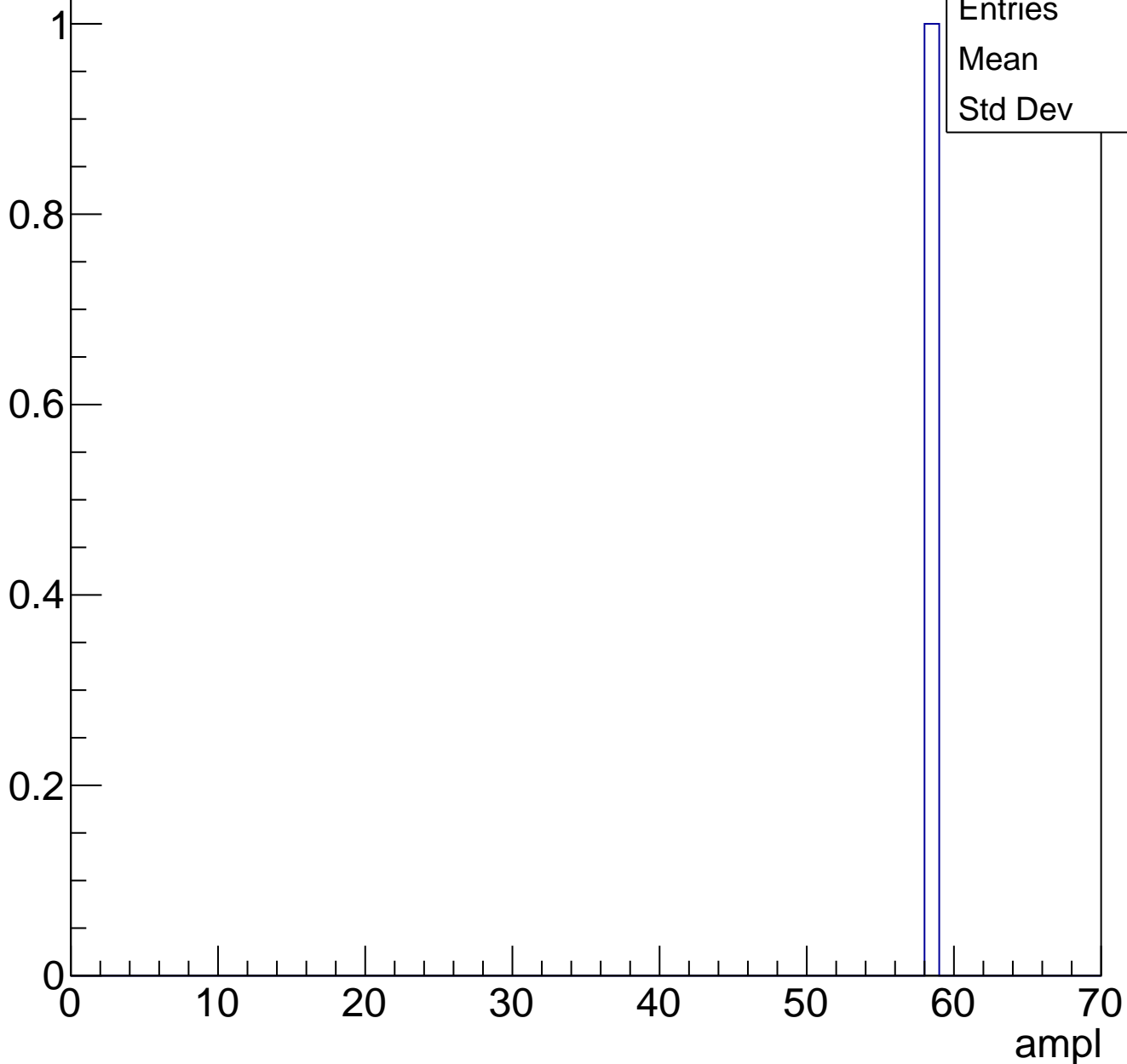




# B1L101S, U16-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U16-ch123, adc0

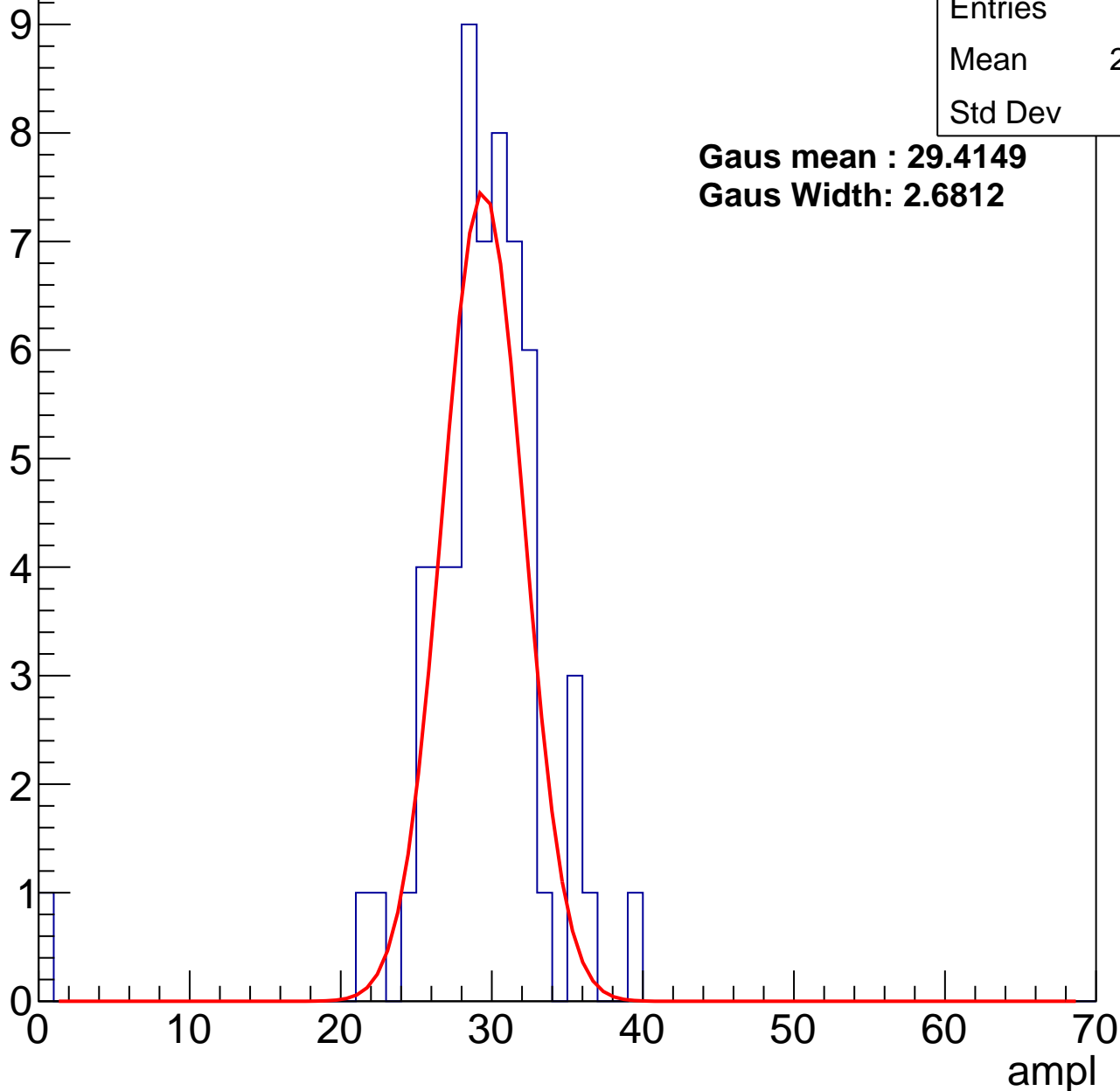
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	28.75
Std Dev	4.98

**Gaus mean : 29.4149**

**Gaus Width: 2.6812**



# B1L101S, U16-ch123, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	92
Mean	36.85
Std Dev	3.668

**Gaus mean : 37.0310**

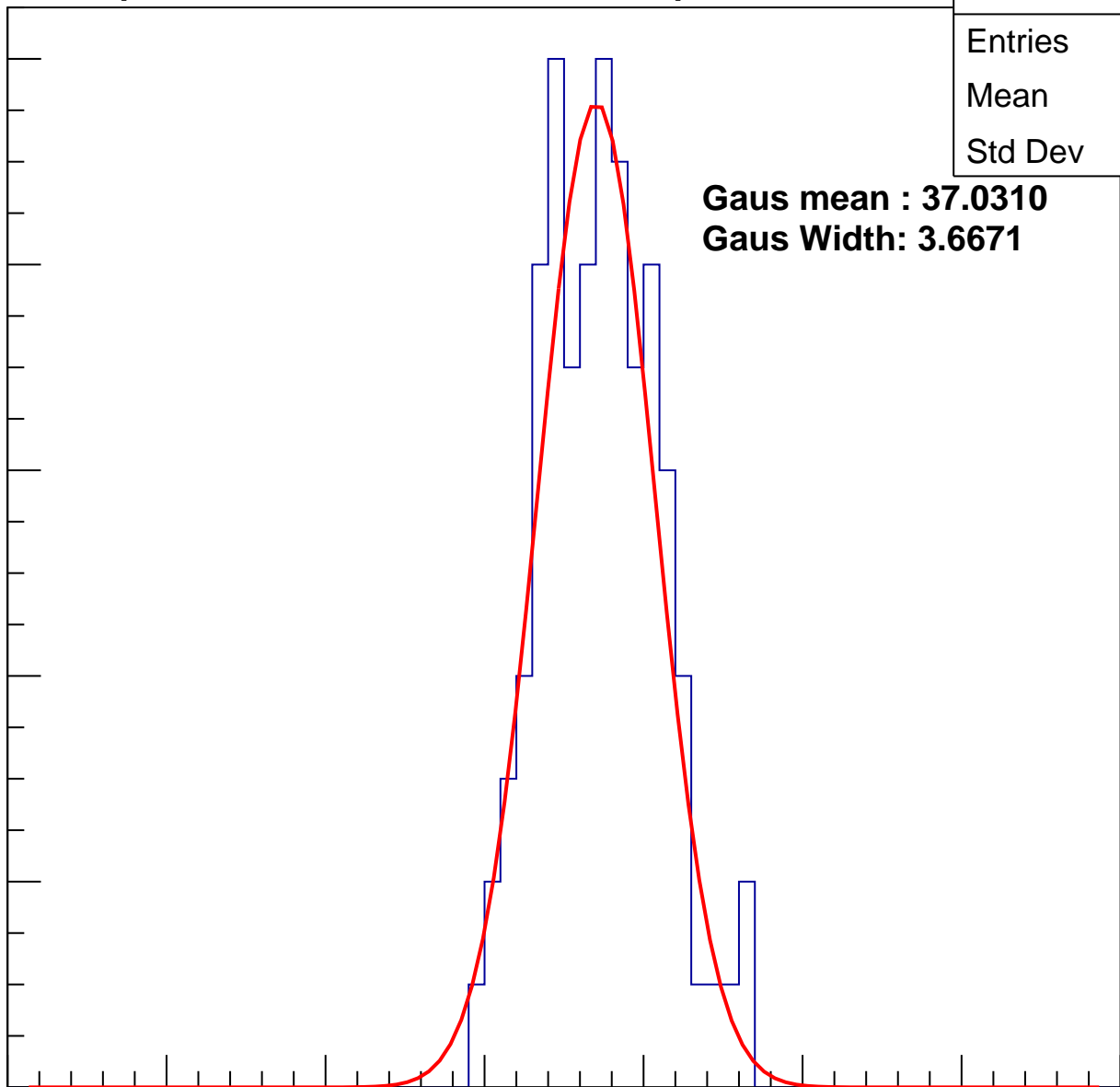
**Gaus Width: 3.6671**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch123, adc2

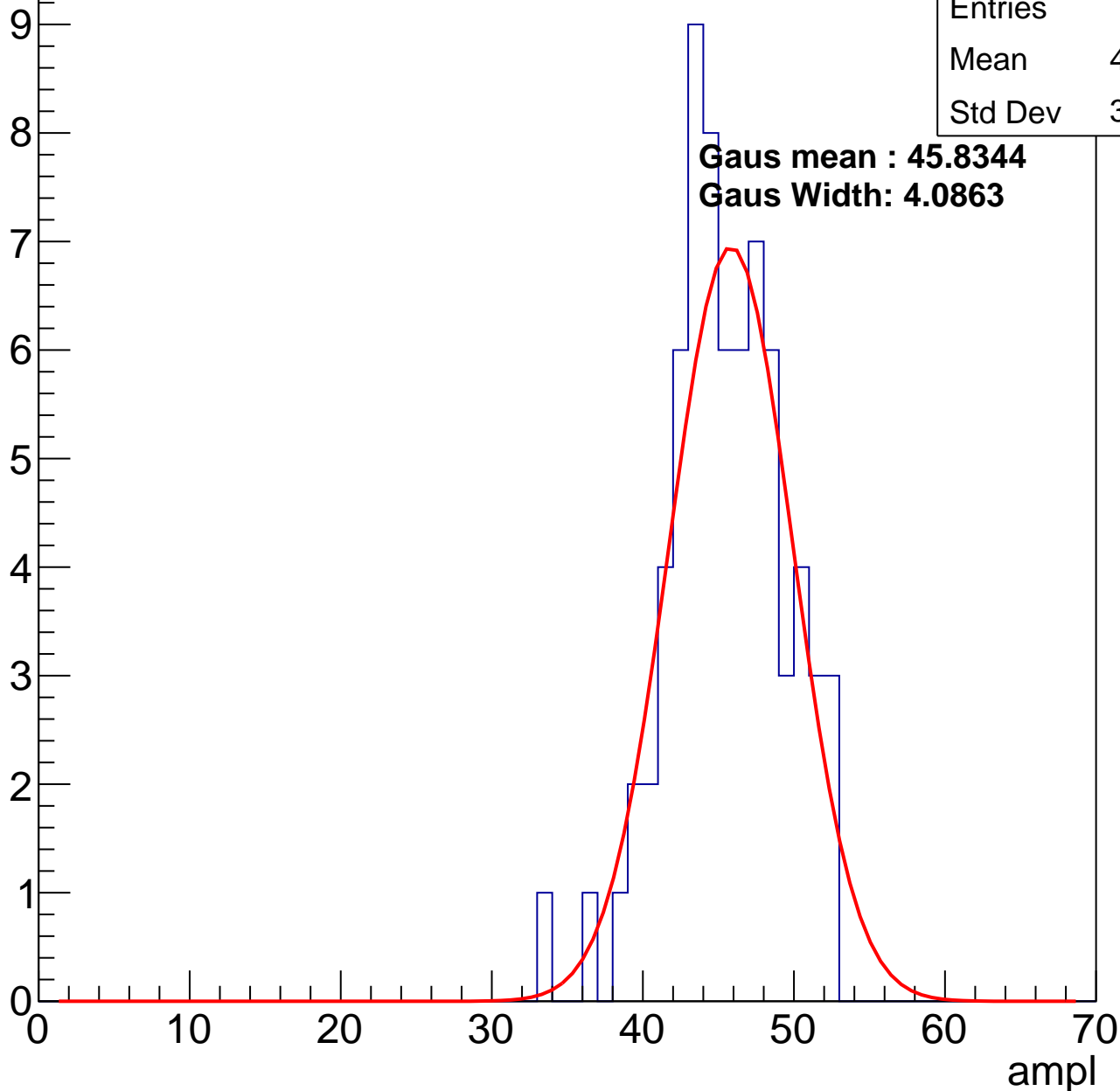
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	44.99
Std Dev	3.817

**Gaus mean : 45.8344**

**Gaus Width: 4.0863**

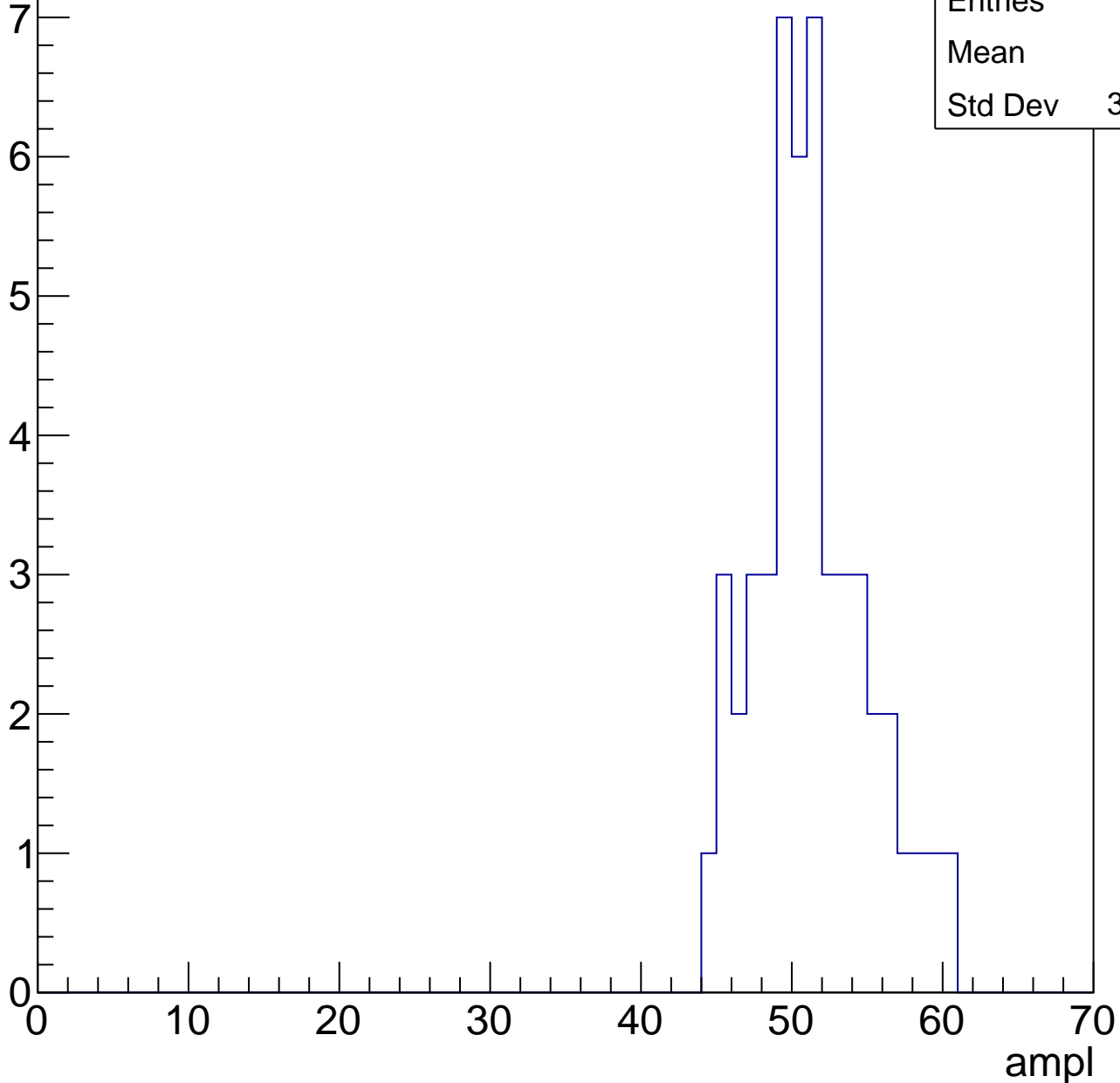


# B1L101S, U16-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	50.8
Std Dev	3.692

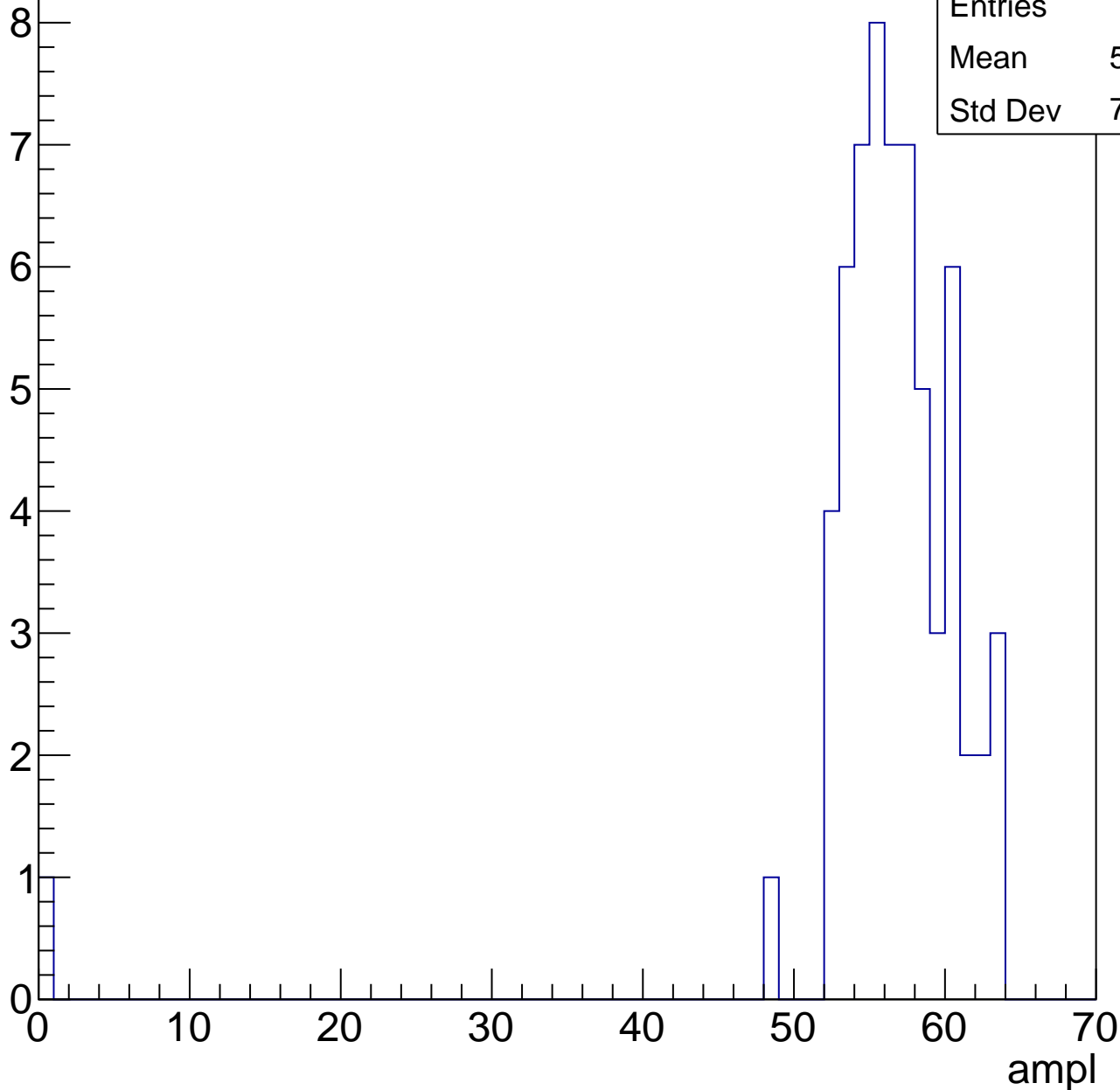


# B1L101S, U16-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	55.56
Std Dev	7.789

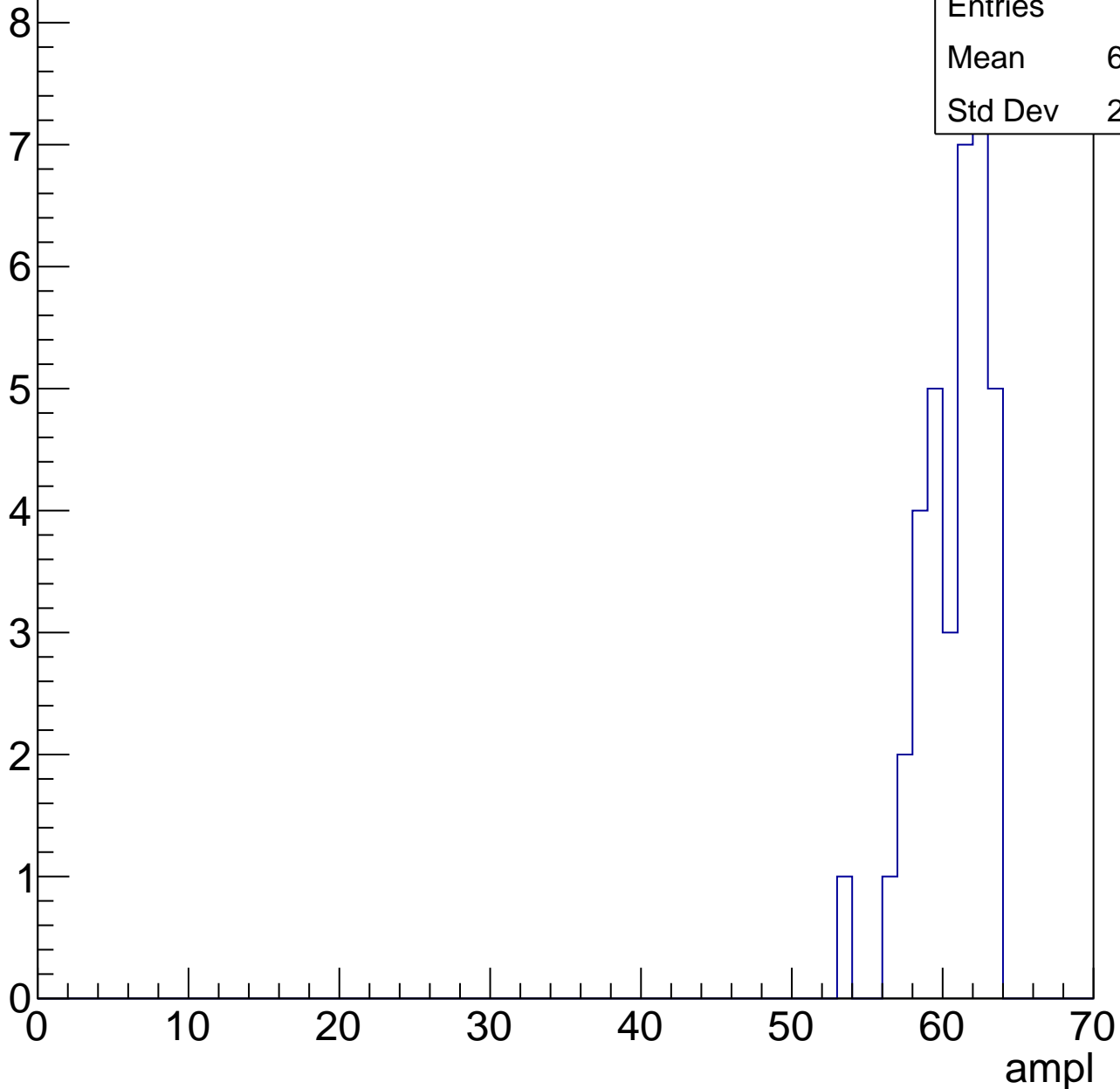


# B1L101S, U16-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

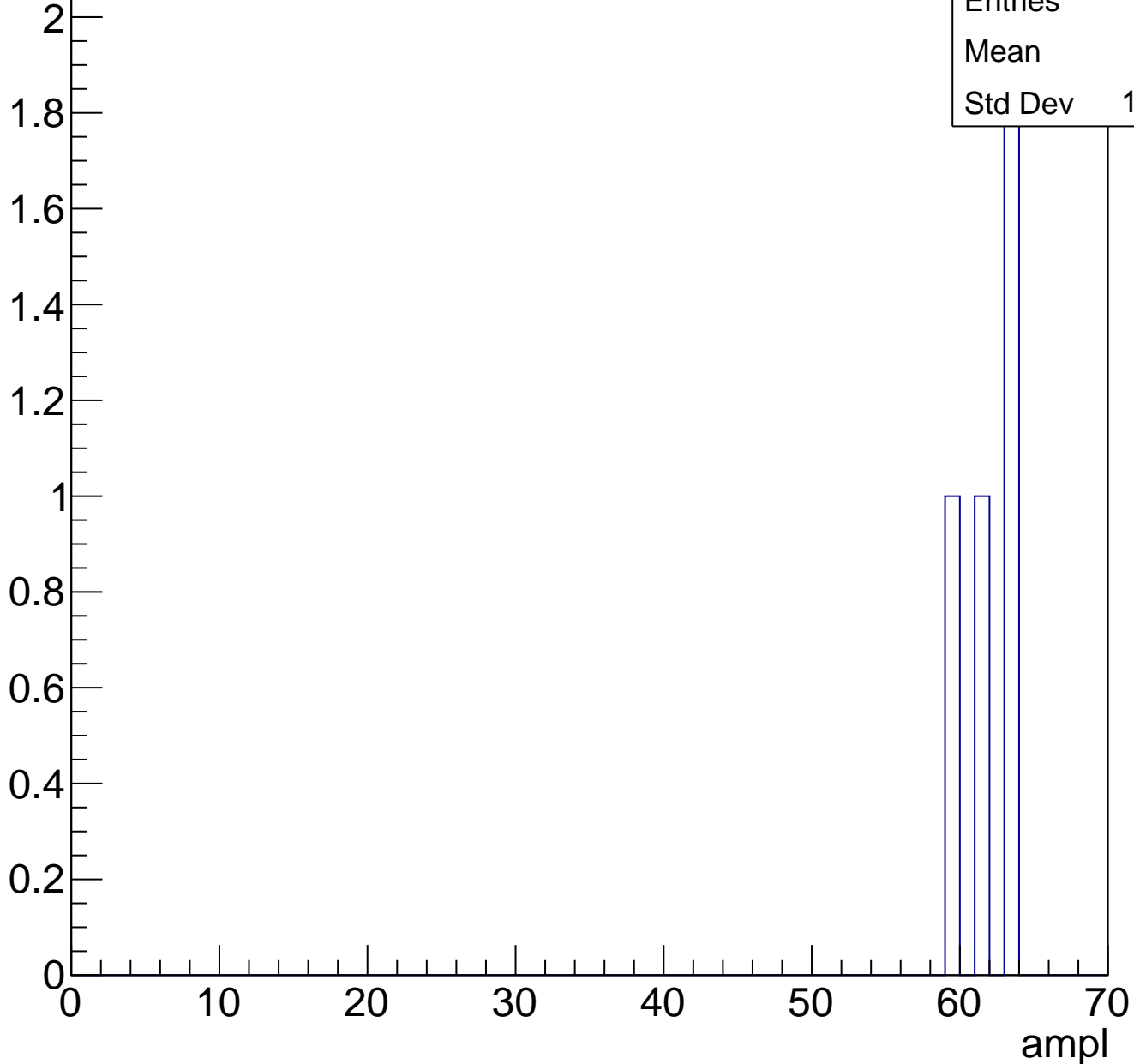
Entries	36
Mean	60.22
Std Dev	2.274



# B1L101S, U16-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

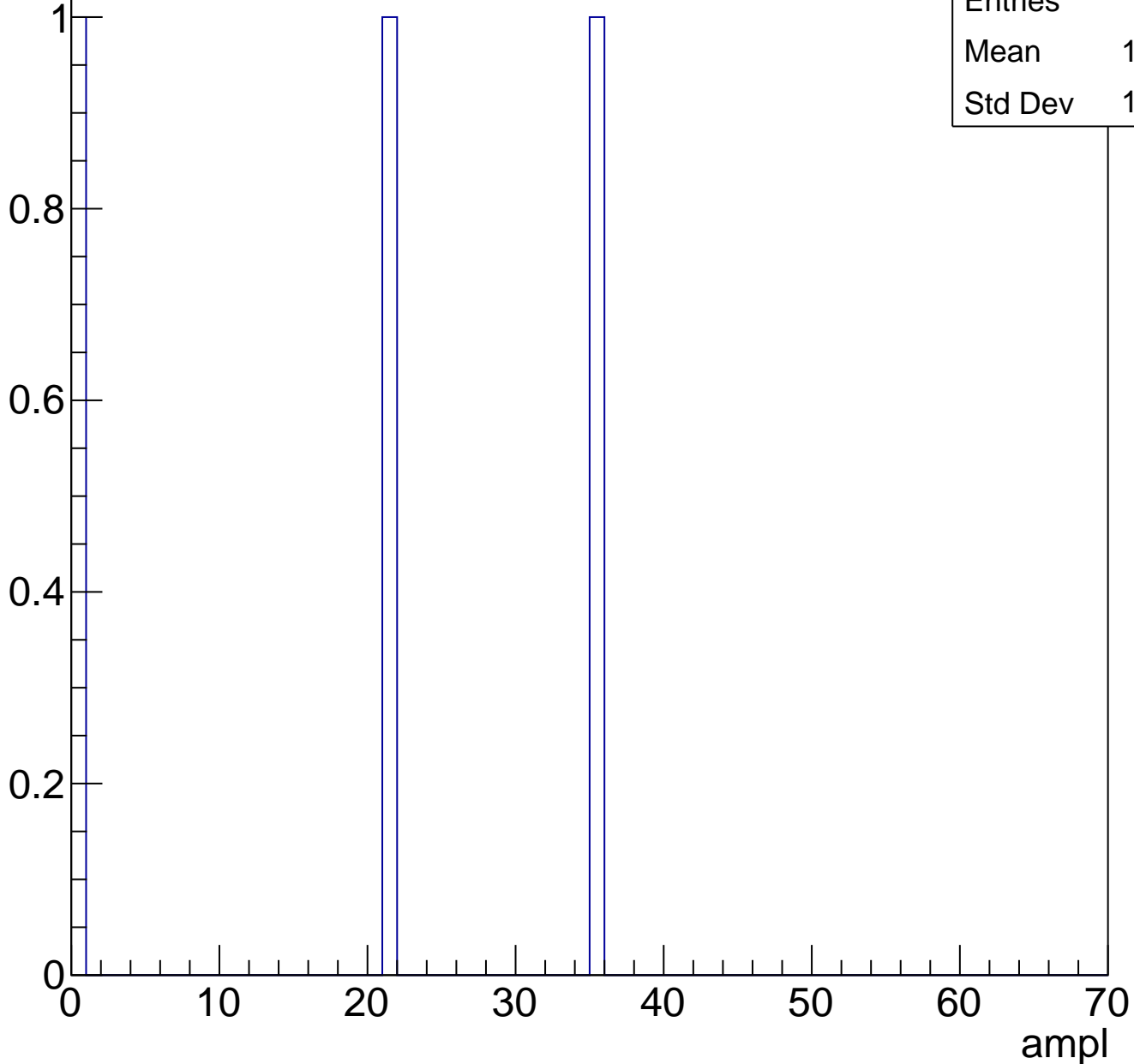




# B1L101S, U16-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	18.67
Std Dev	14.38

# B1L101S, U16-ch124, adc0

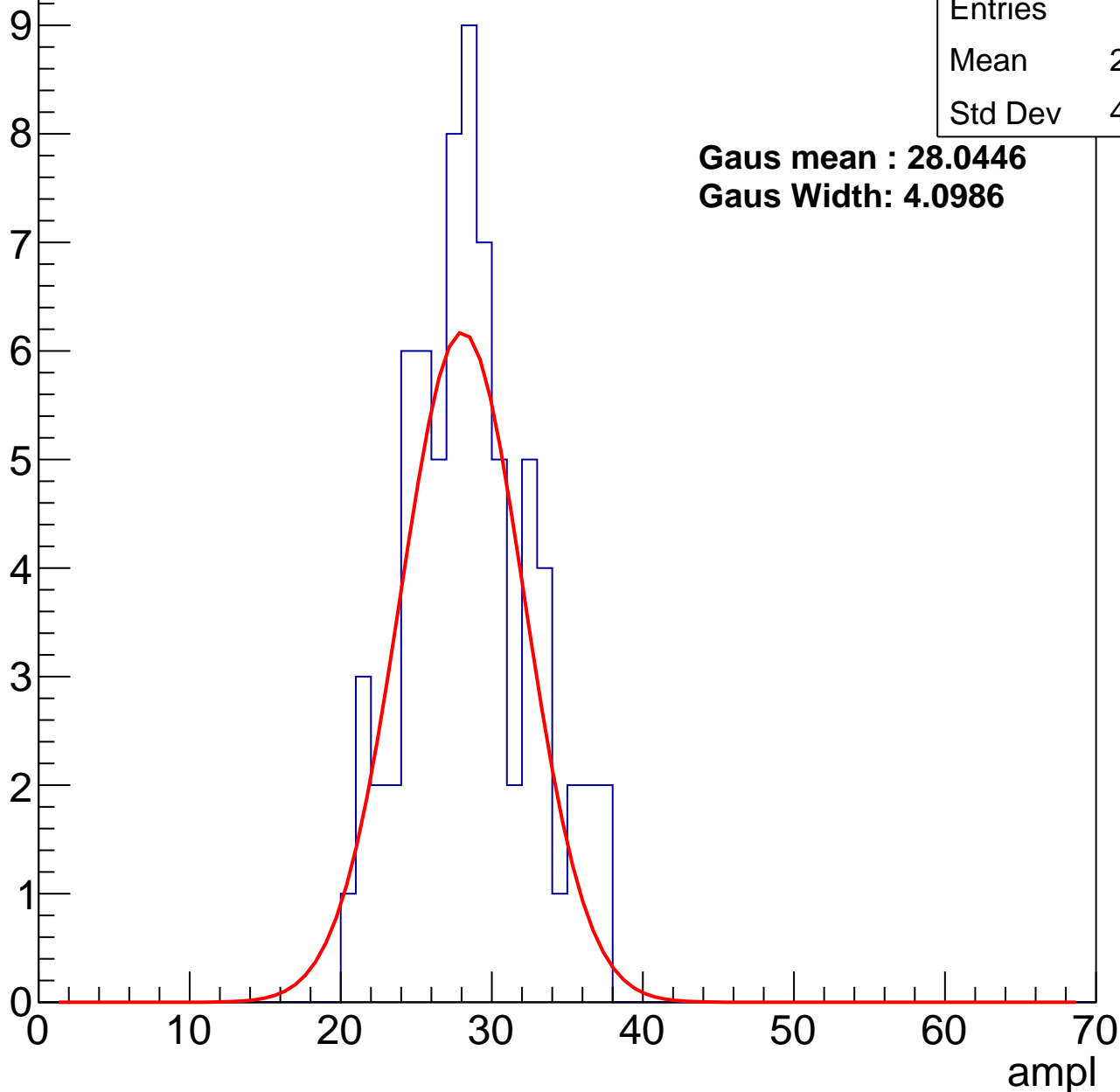
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	28.08
Std Dev	4.013

**Gaus mean : 28.0446**

**Gaus Width: 4.0986**



# B1L101S, U16-ch124, adc1

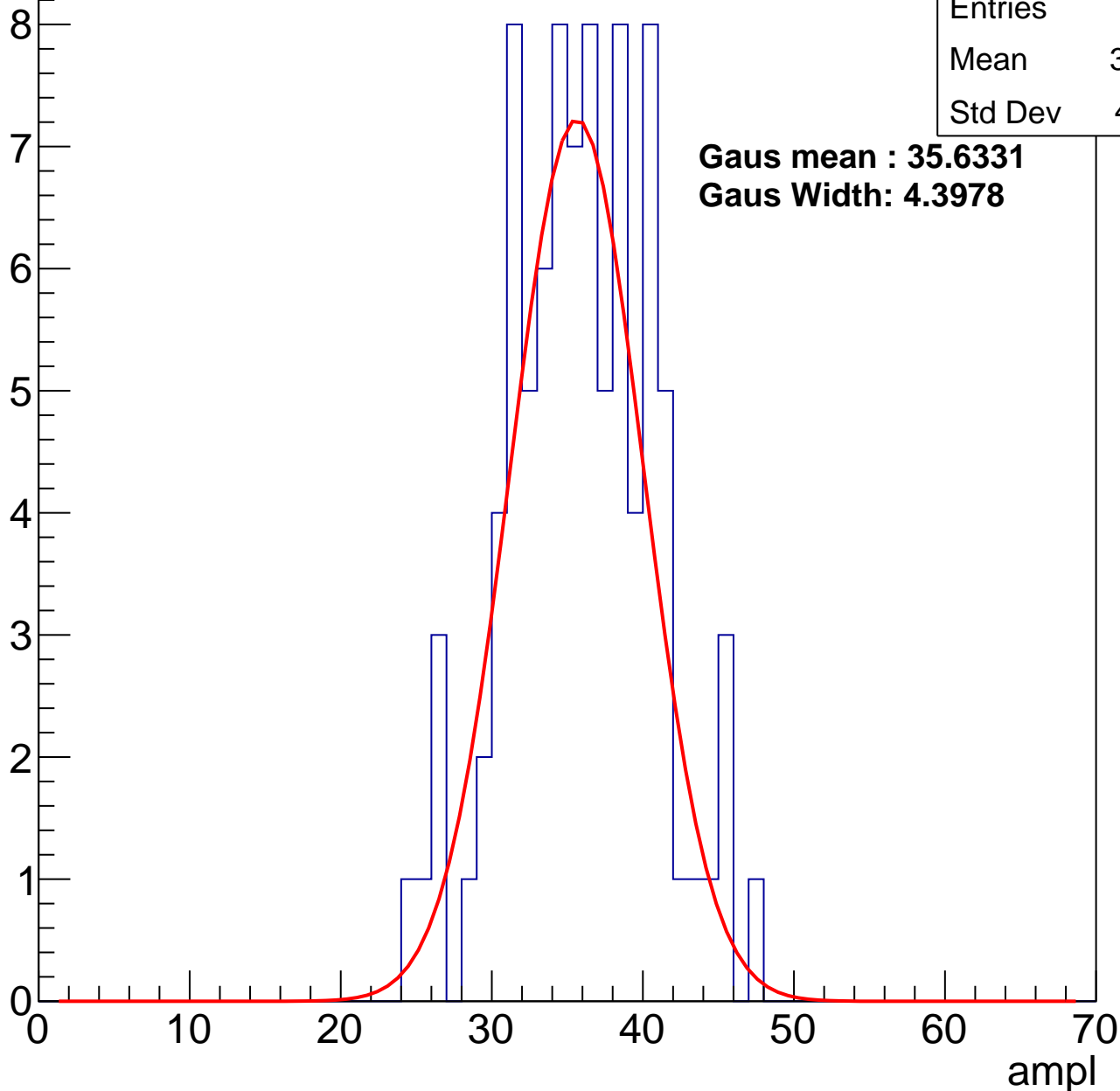
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	91
Mean	35.44
Std Dev	4.751

**Gaus mean : 35.6331**

**Gaus Width: 4.3978**



# B1L101S, U16-ch124, adc2

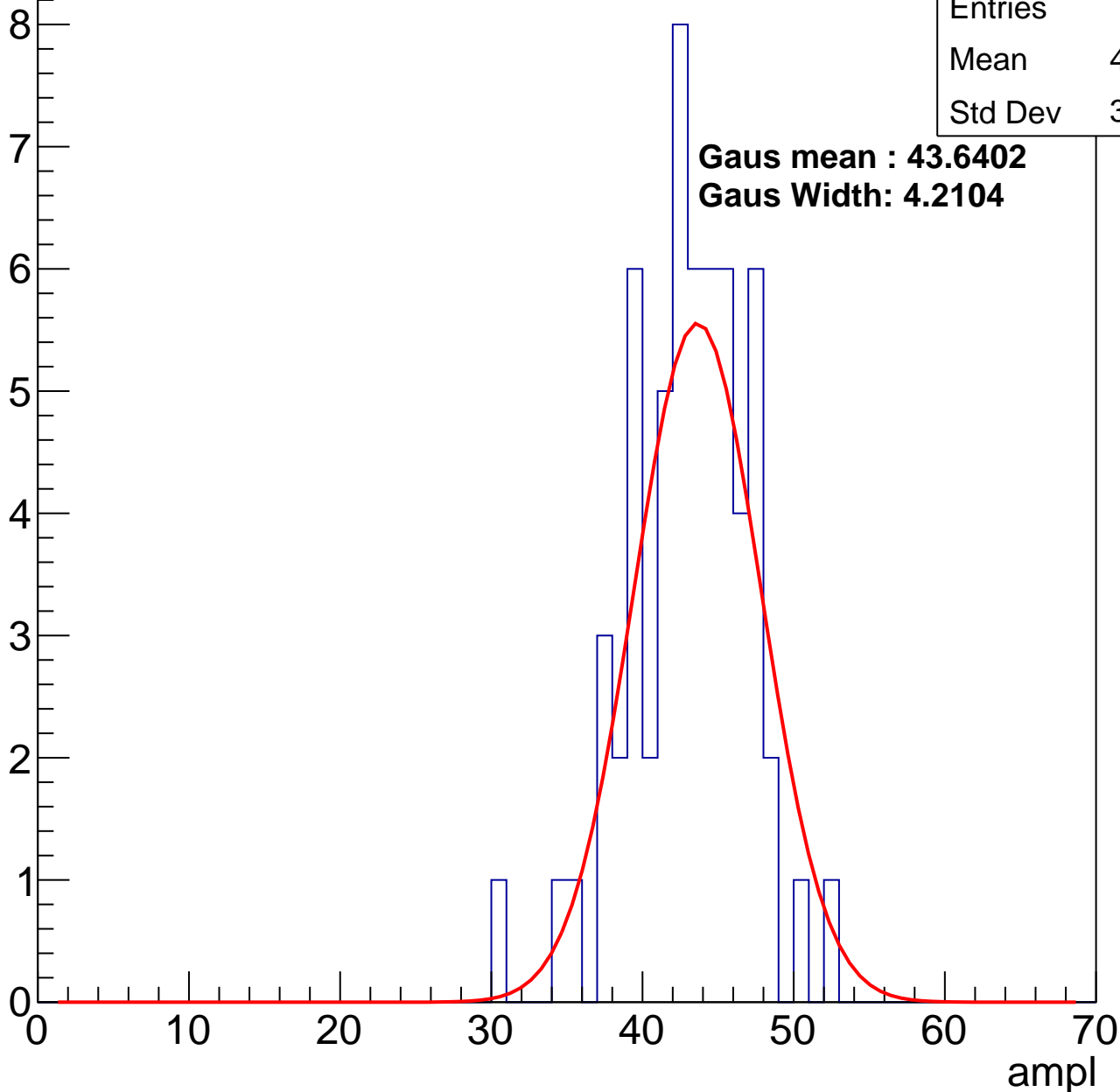
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	42.57
Std Dev	3.936

**Gaus mean : 43.6402**

**Gaus Width: 4.2104**

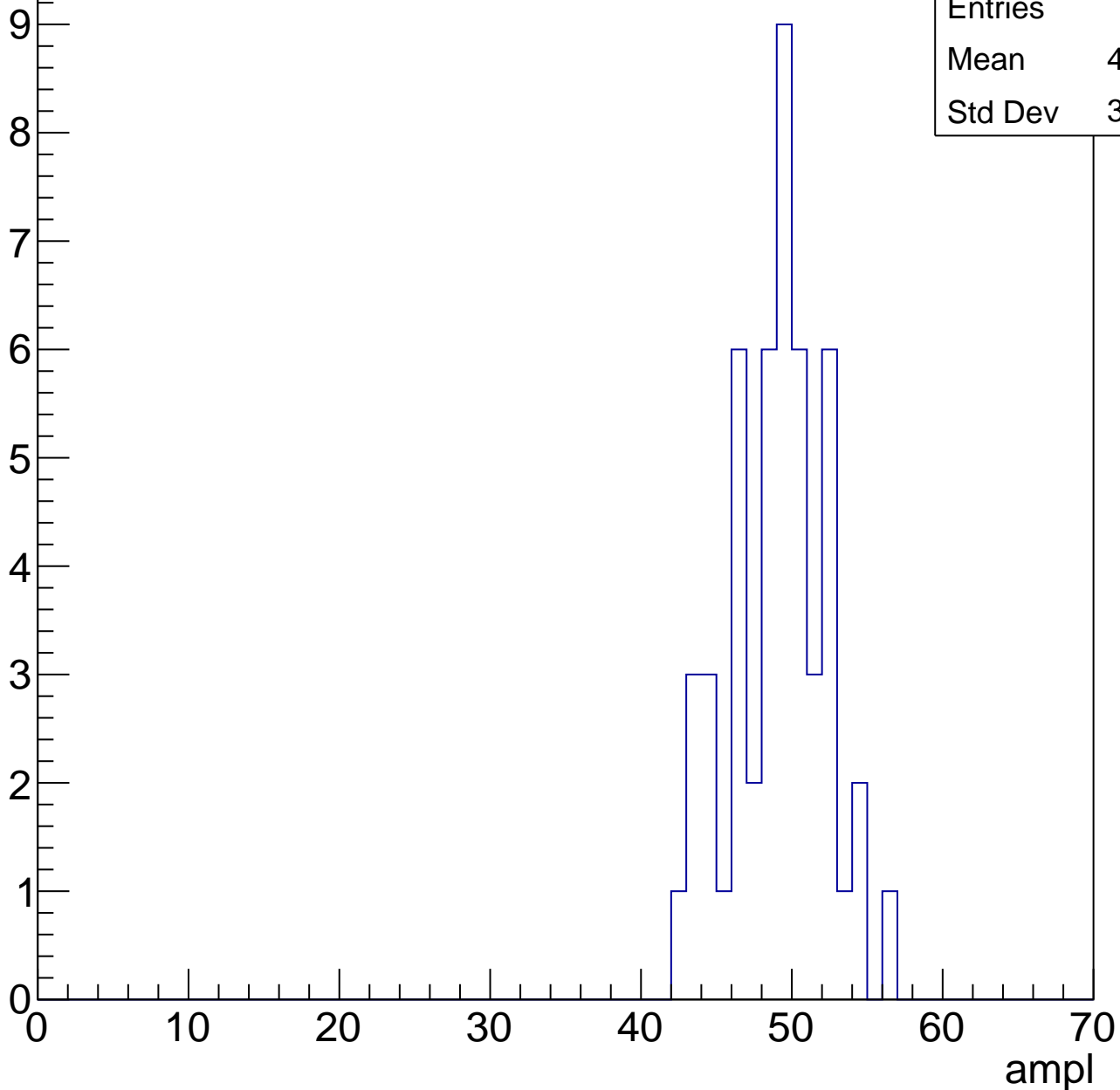


# B1L101S, U16-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

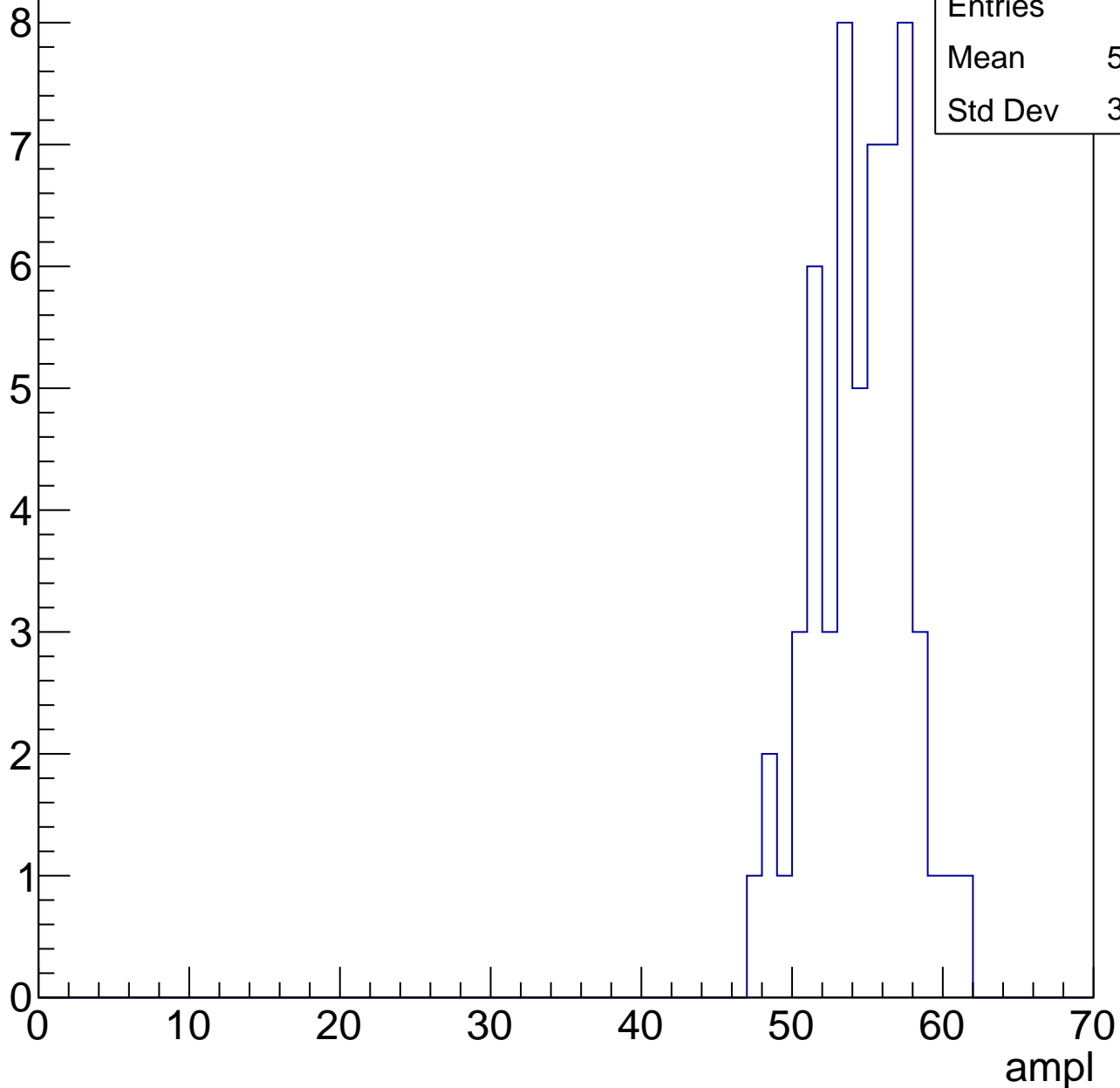
Entries	50
Mean	48.58
Std Dev	3.144



# B1L101S, U16-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

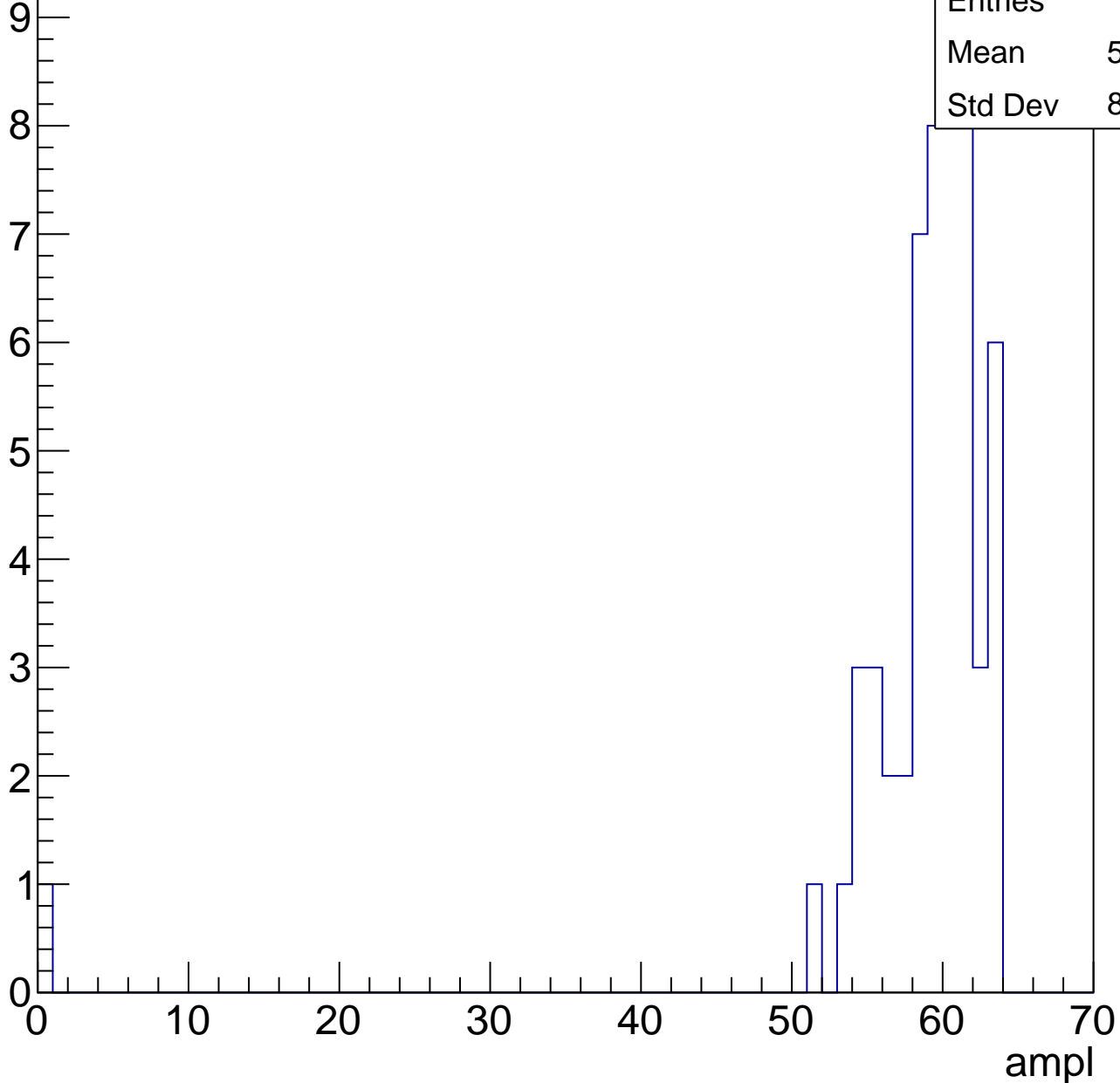


# B1L101S, U16-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	57.96
Std Dev	8.362

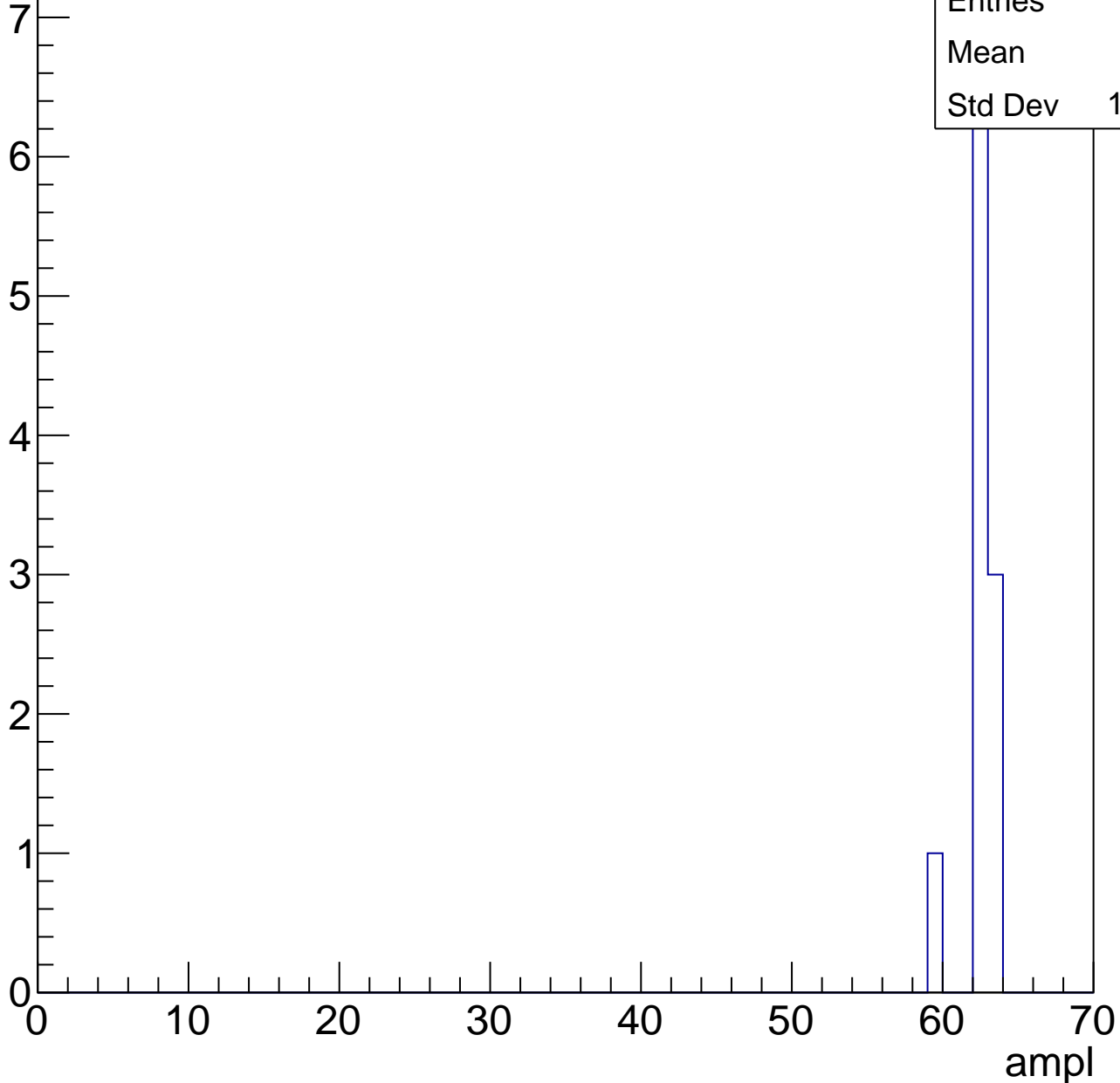


# B1L101S, U16-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	11
Mean	62
Std Dev	1.044





# B1L101S, U16-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L101S, U16-ch125, adc0

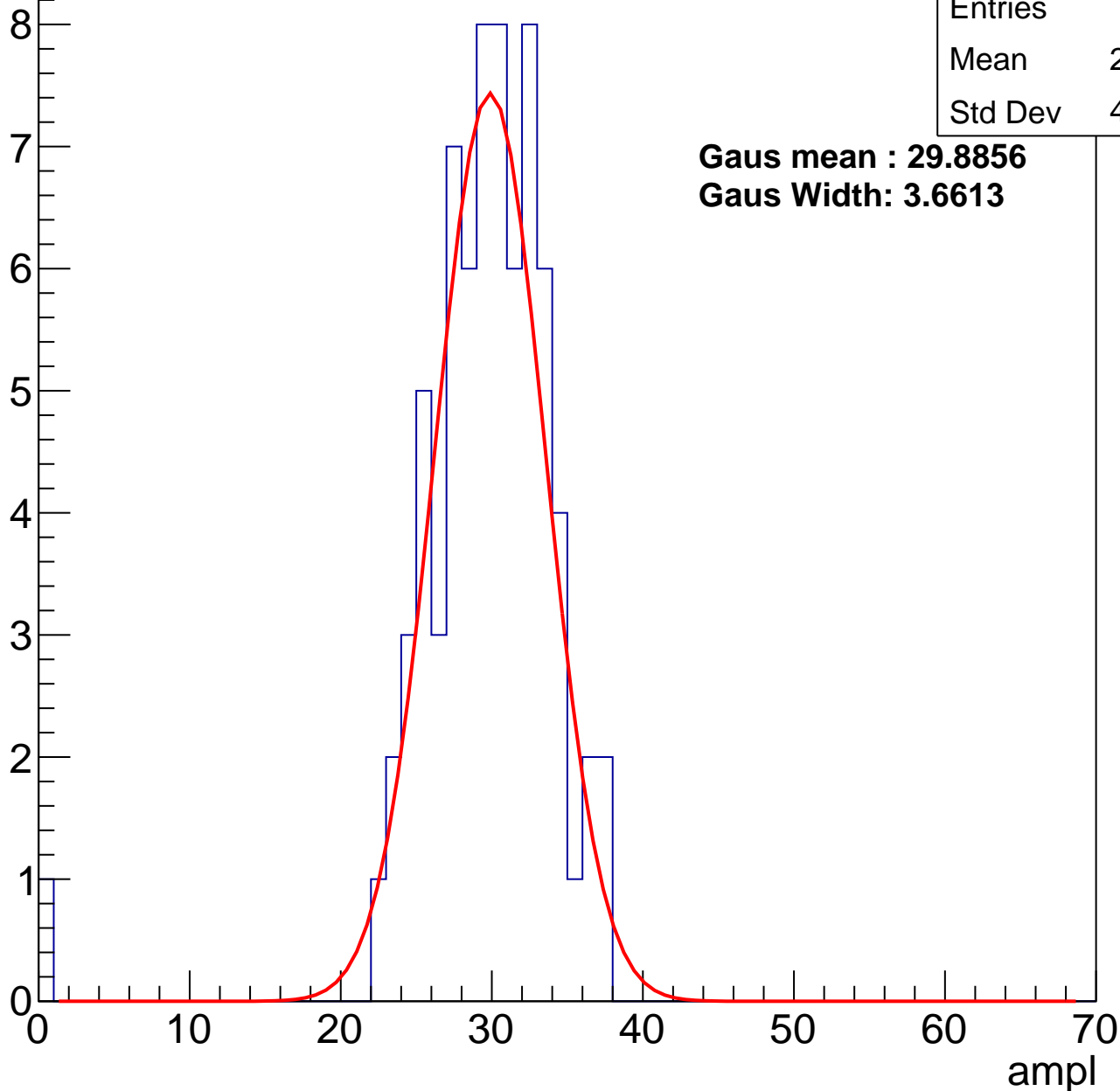
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	29.16
Std Dev	4.879

**Gaus mean : 29.8856**

**Gaus Width: 3.6613**



# B1L101S, U16-ch125, adc1

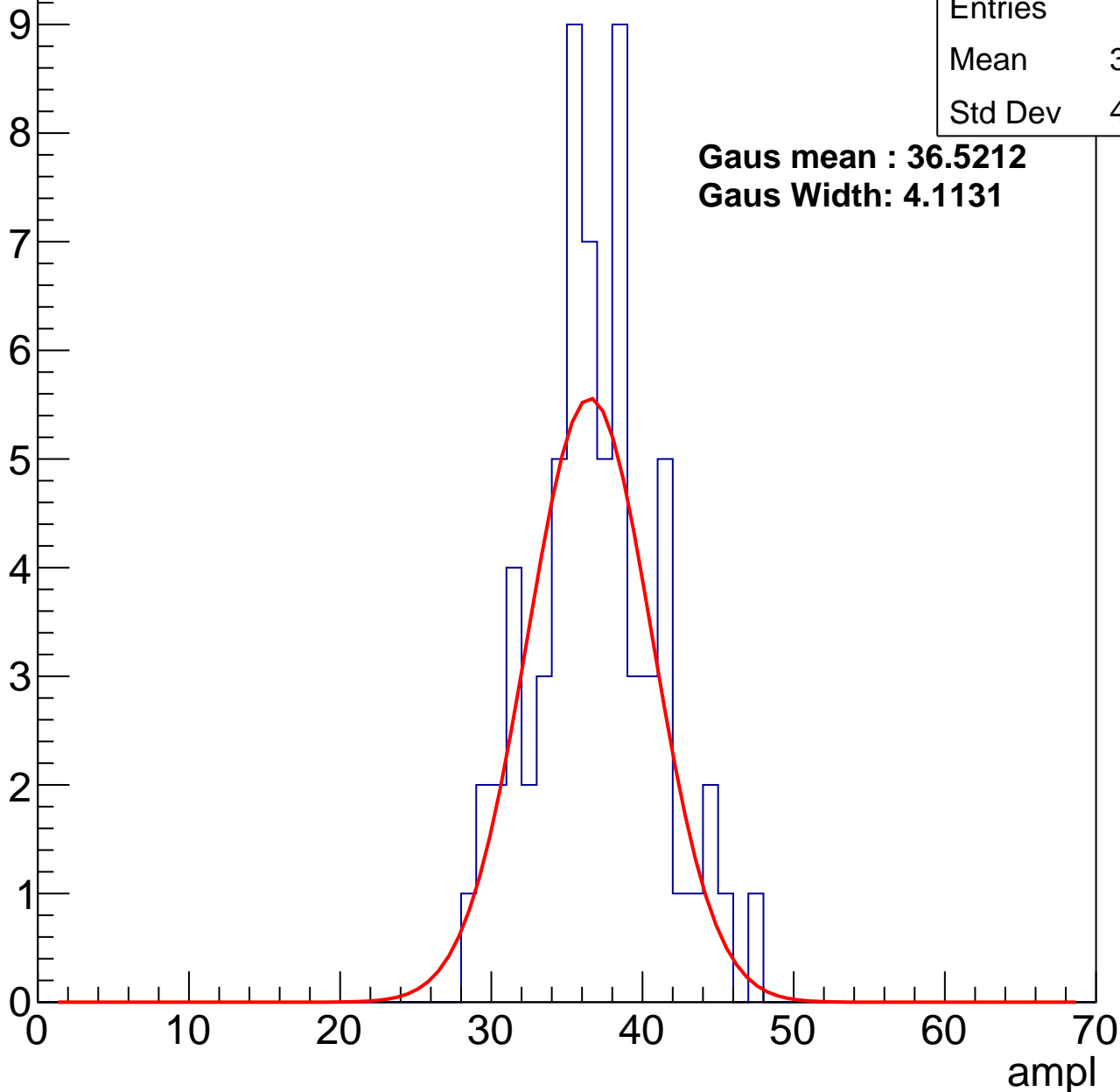
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	36.42
Std Dev	4.019

**Gaus mean : 36.5212**

**Gaus Width: 4.1131**



# B1L101S, U16-ch125, adc2

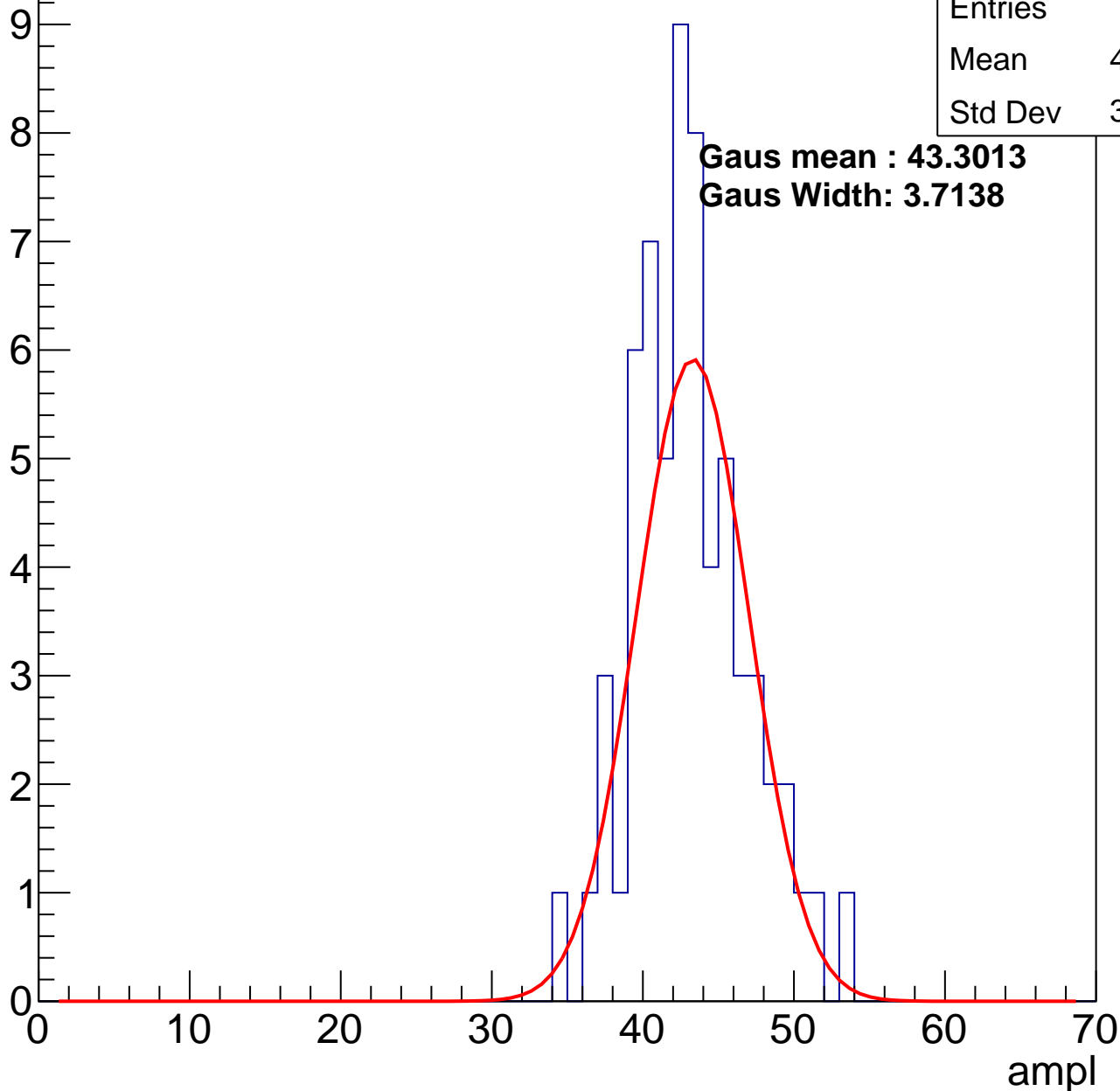
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	42.67
Std Dev	3.733

**Gaus mean : 43.3013**

**Gaus Width: 3.7138**

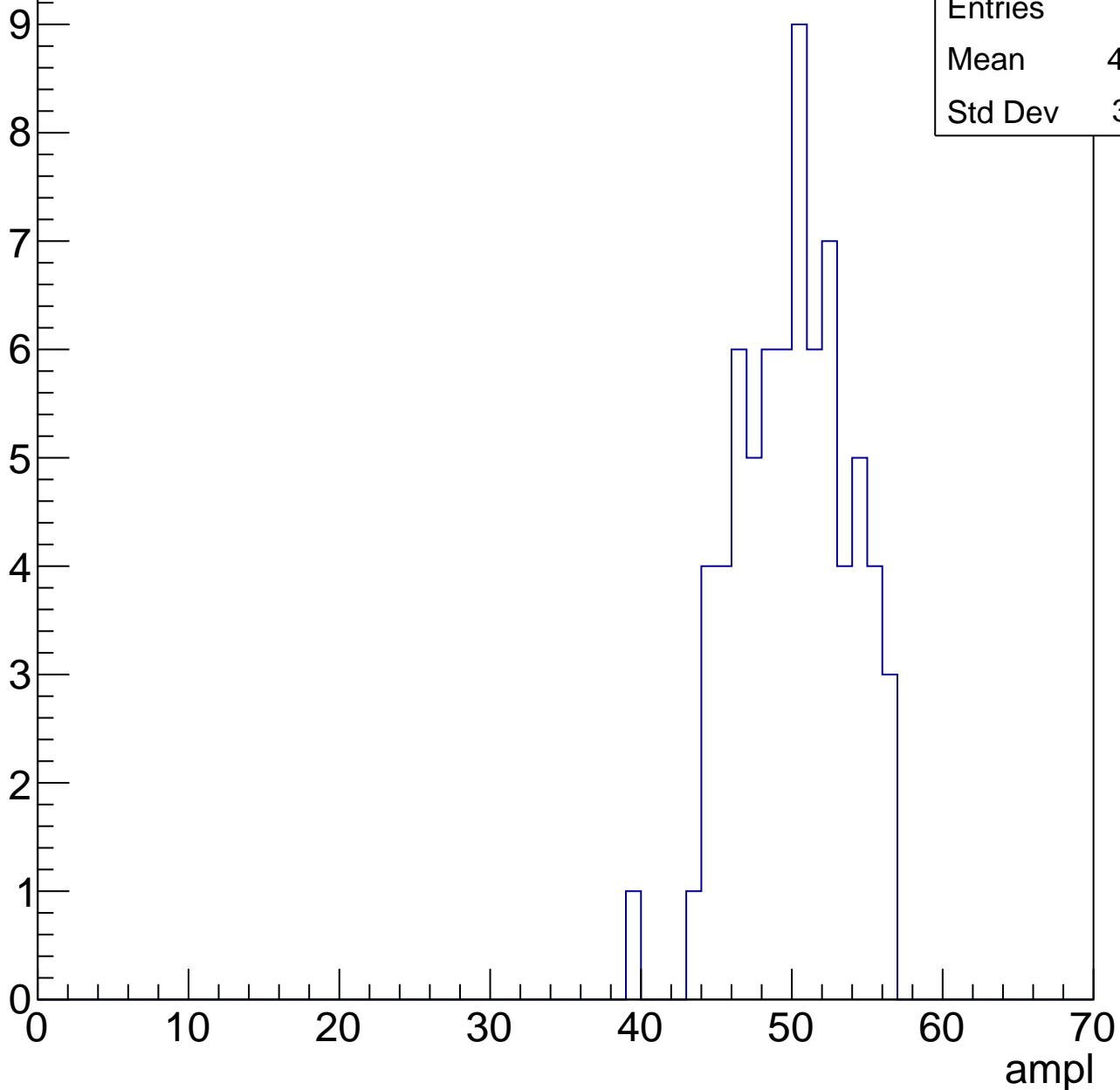


# B1L101S, U16-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	49.59
Std Dev	3.621

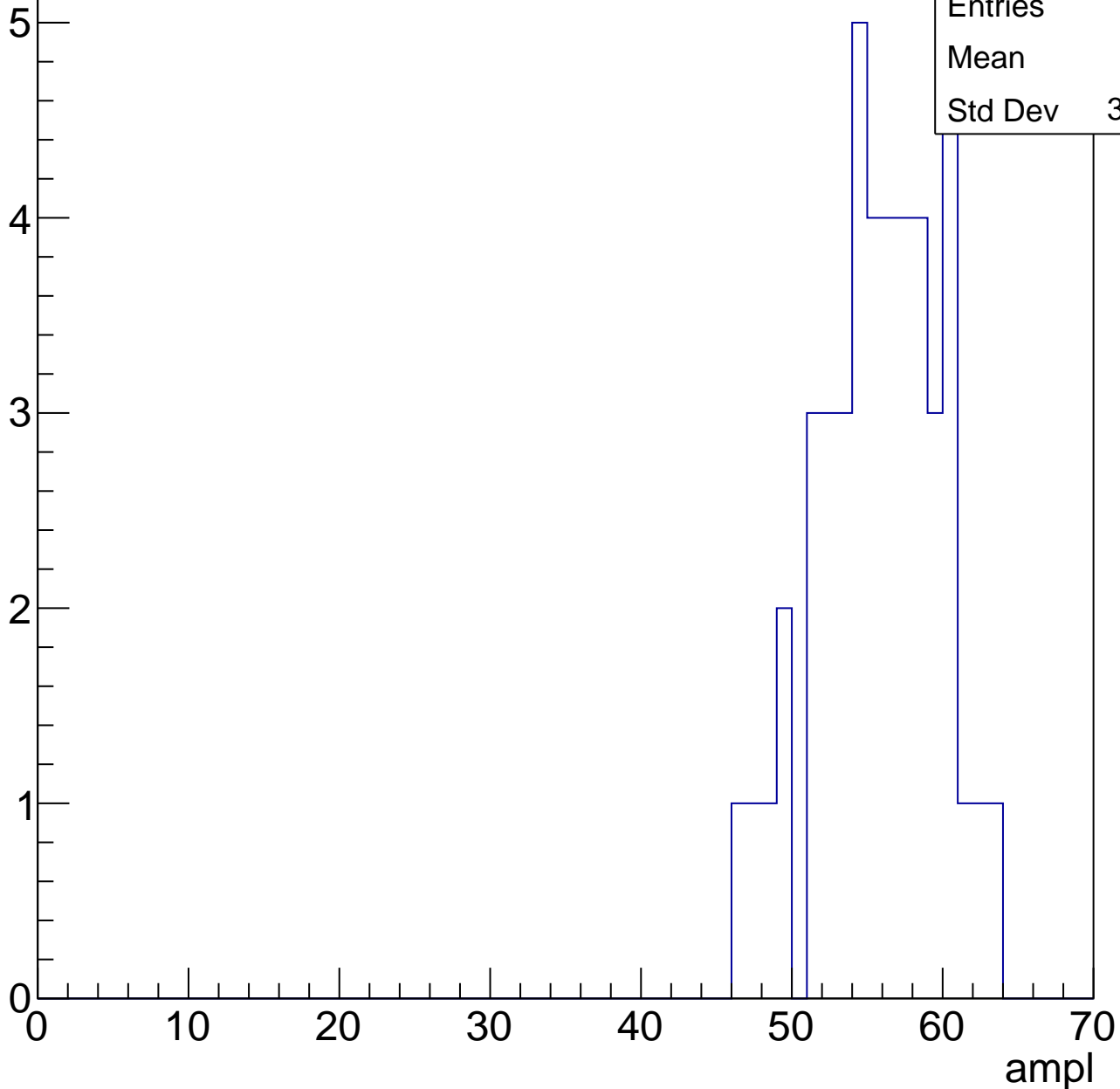


# B1L101S, U16-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	55.3
Std Dev	3.988

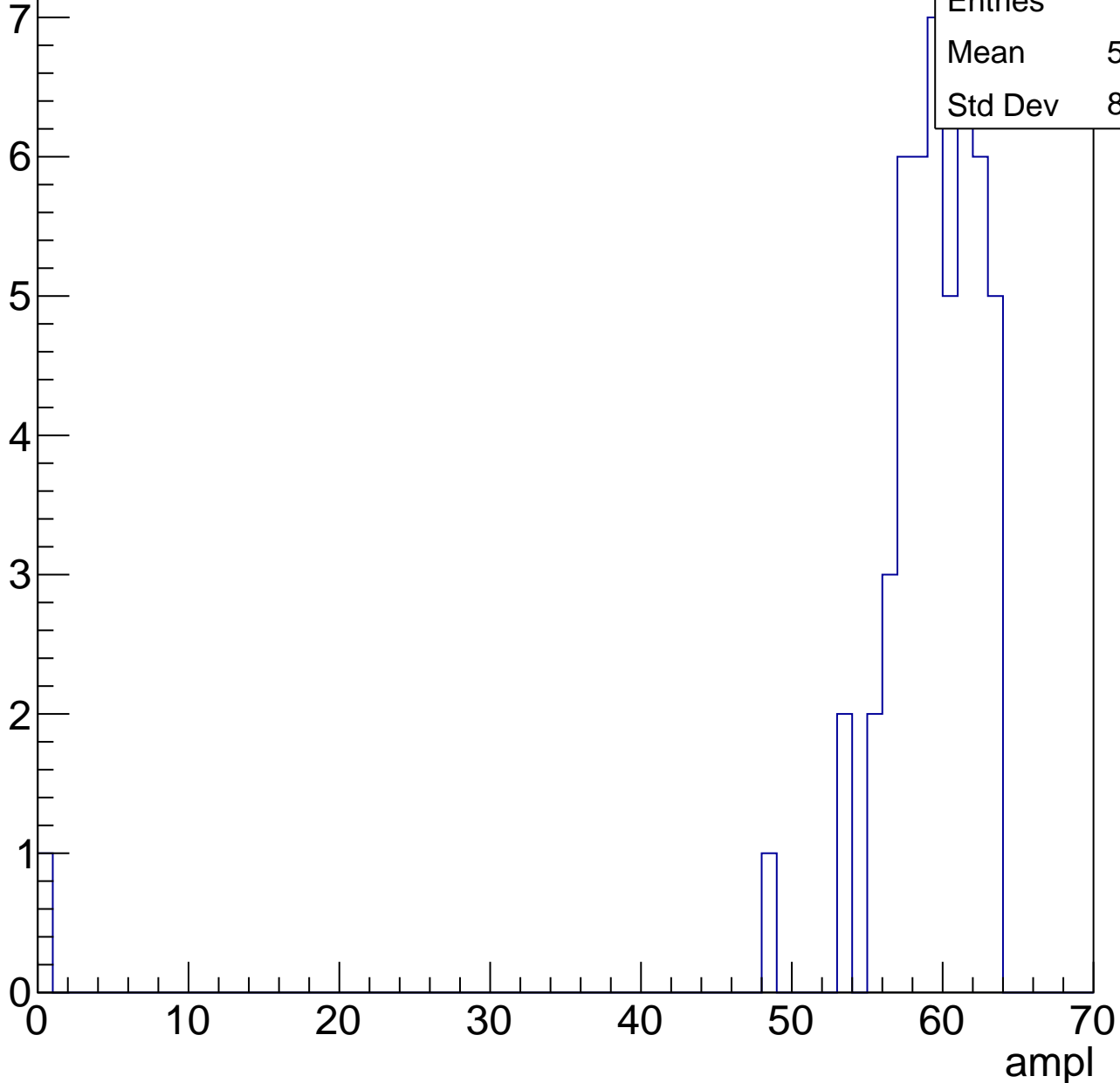


# B1L101S, U16-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	57.82
Std Dev	8.699



# B1L101S, U16-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U16-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U16-ch126, adc0

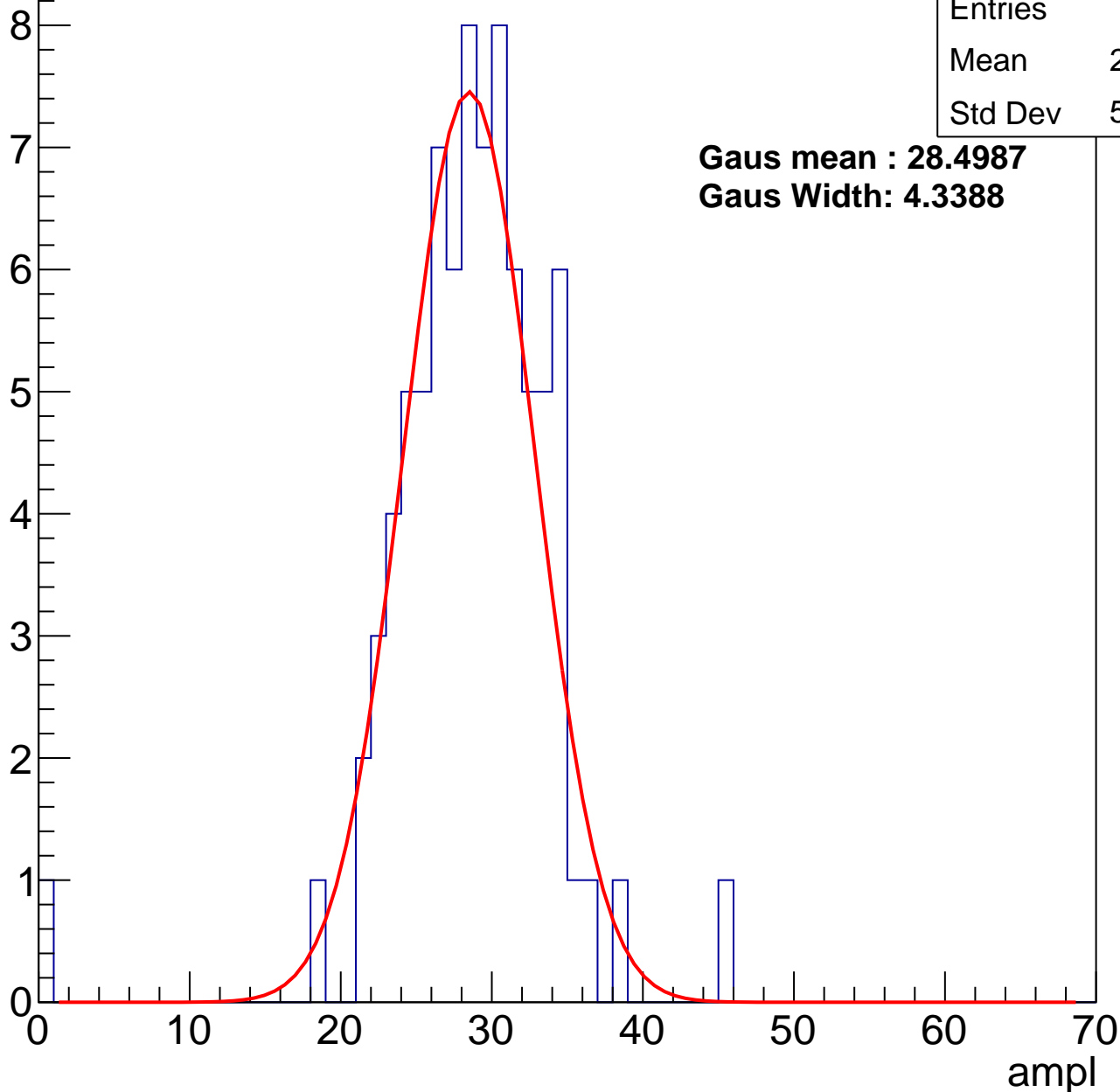
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	83
Mean	28.23
Std Dev	5.333

**Gaus mean : 28.4987**

**Gaus Width: 4.3388**



# B1L101S, U16-ch126, adc1

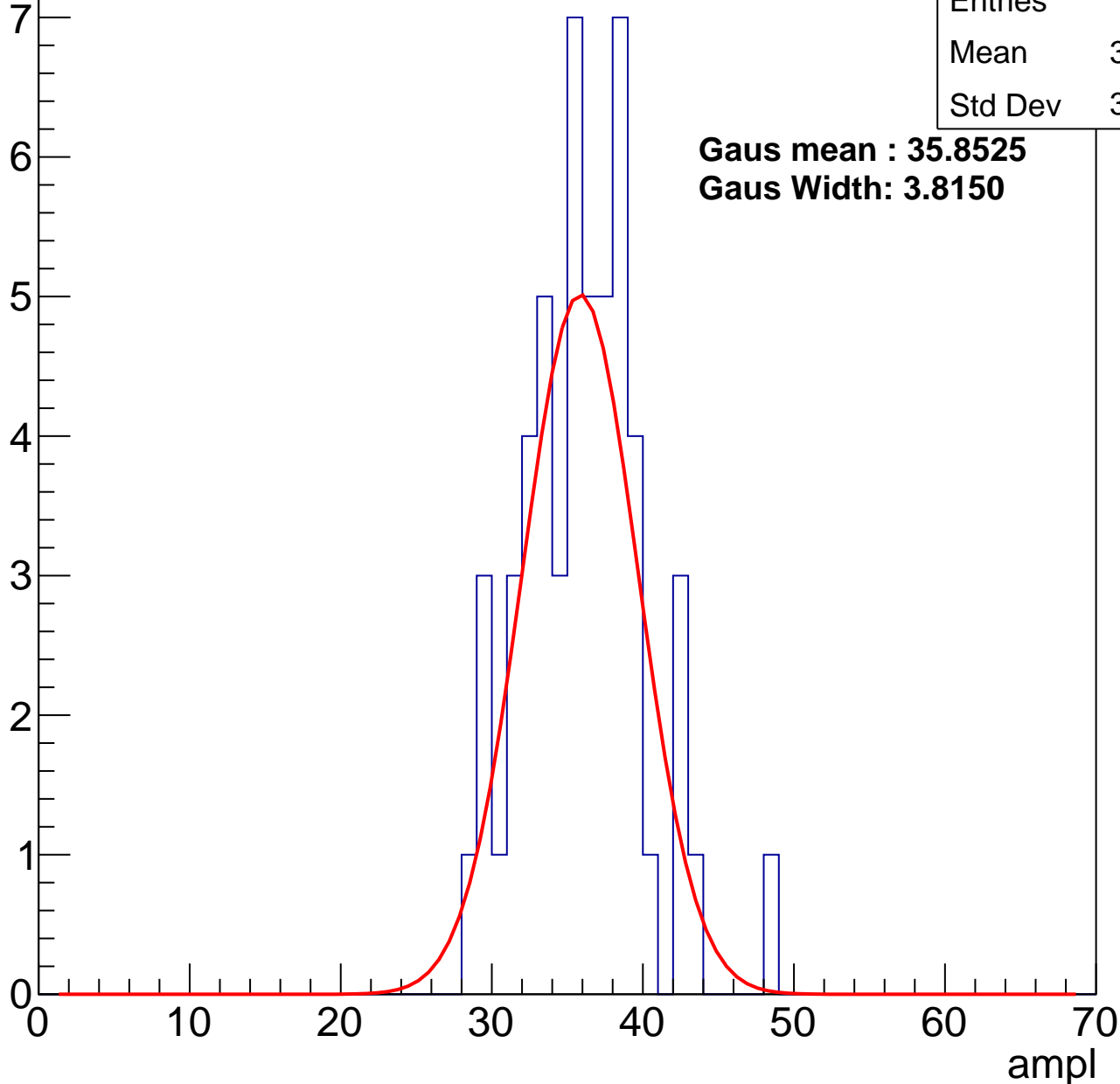
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	35.59
Std Dev	3.914

**Gaus mean : 35.8525**

**Gaus Width: 3.8150**



# B1L101S, U16-ch126, adc2

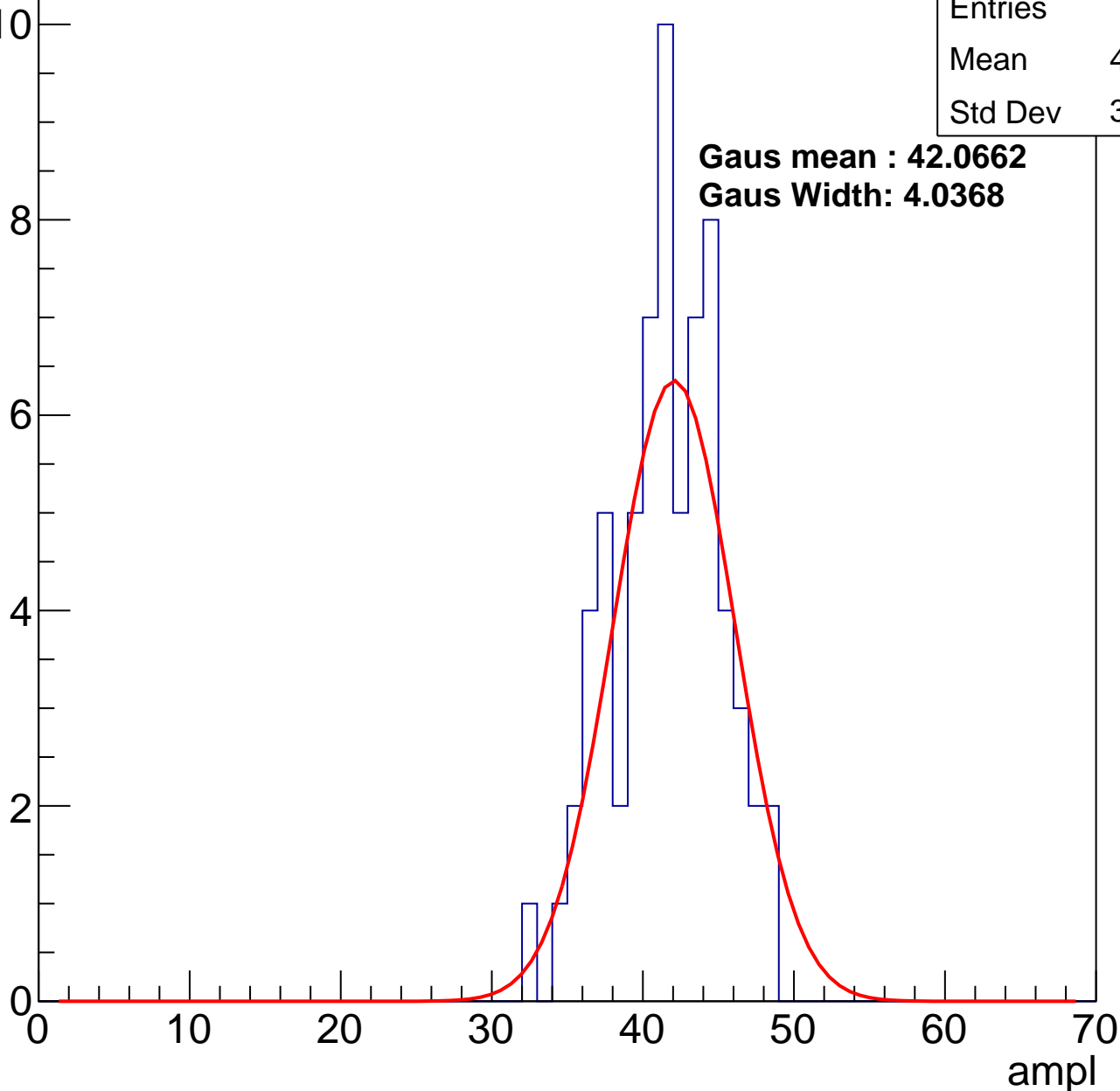
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	41.13
Std Dev	3.514

**Gaus mean : 42.0662**

**Gaus Width: 4.0368**

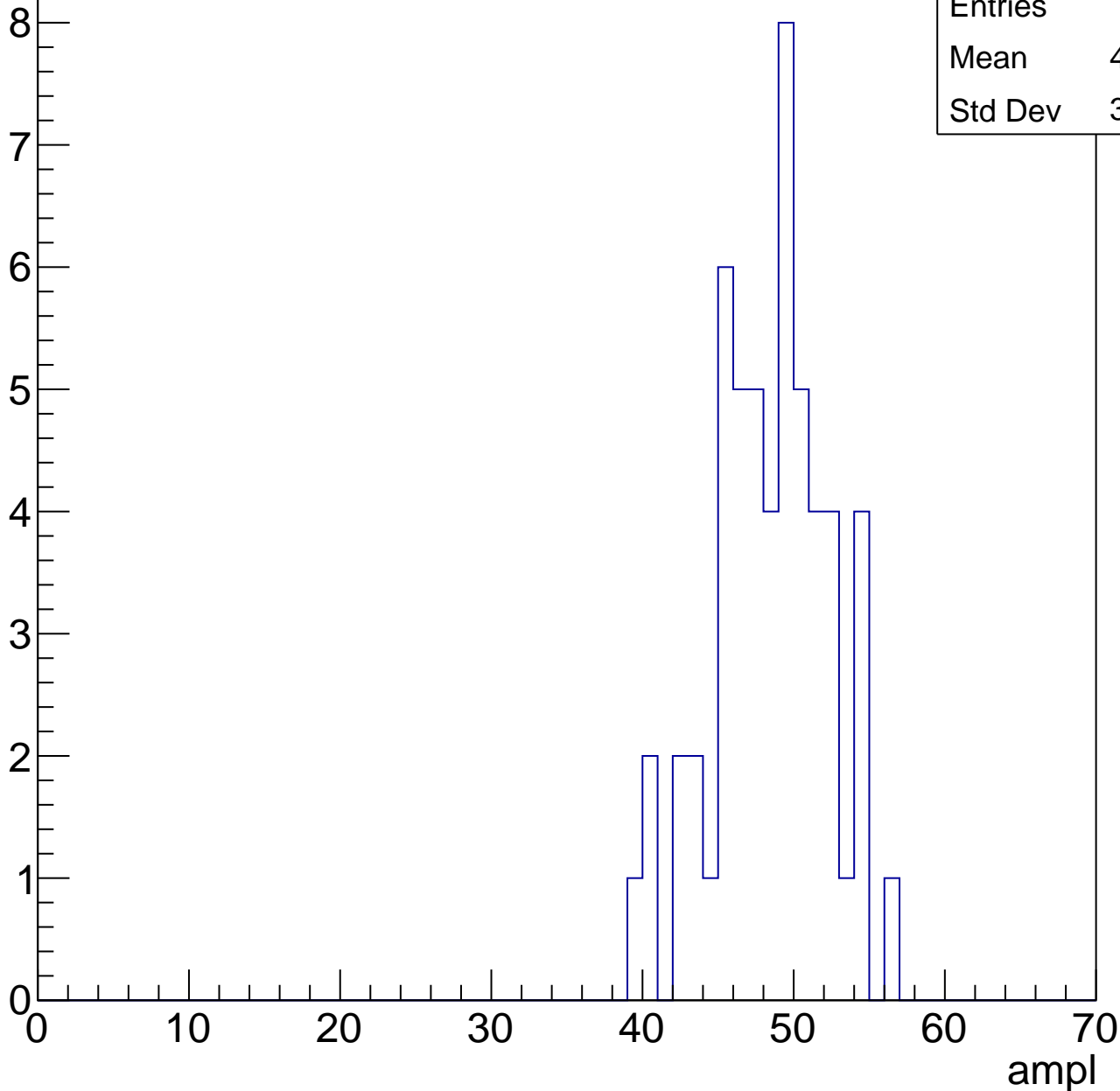


# B1L101S, U16-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	47.98
Std Dev	3.783

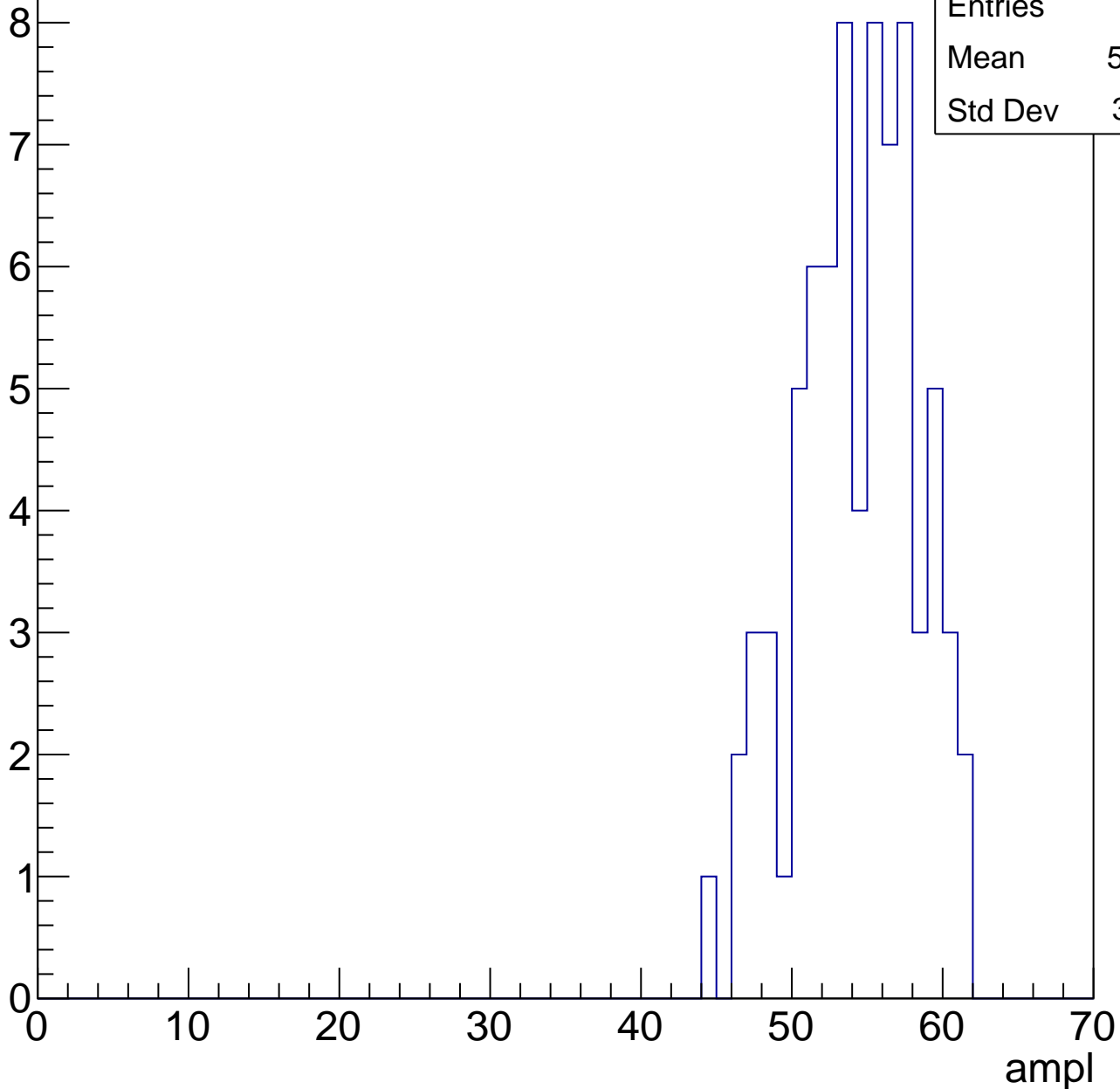


# B1L101S, U16-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

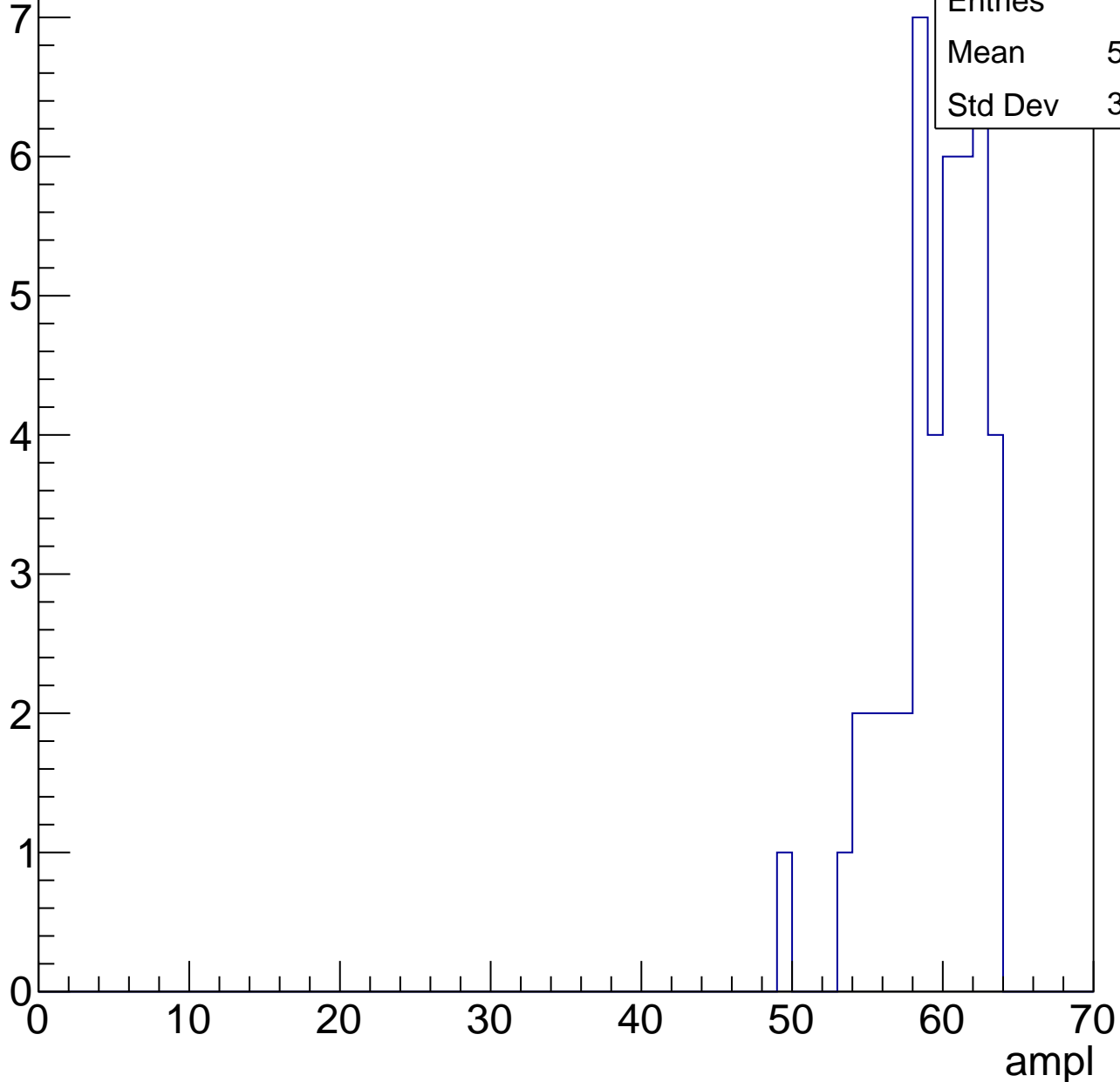
Entries	75
Mean	53.83
Std Dev	3.931



# B1L101S, U16-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

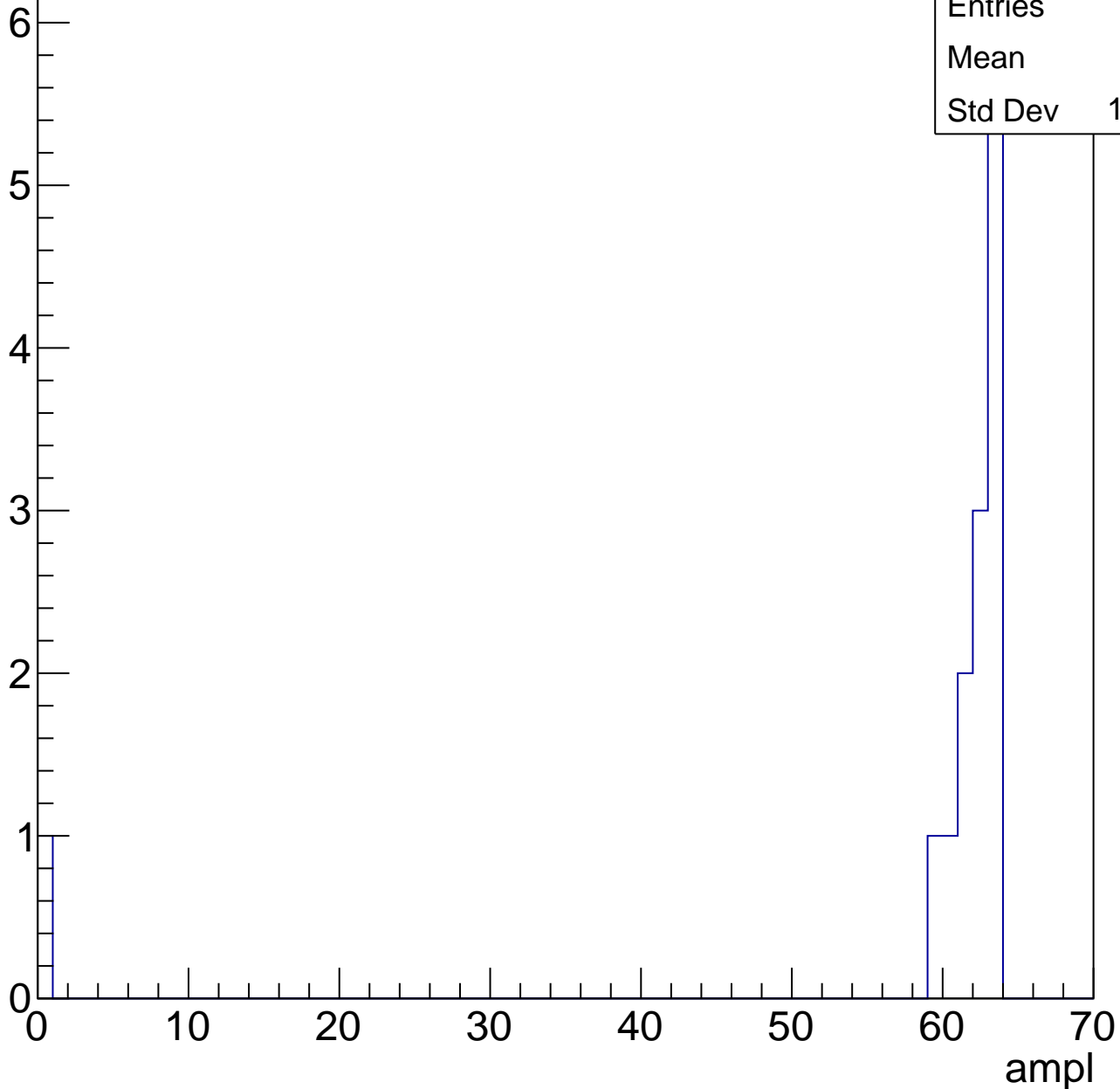


# B1L101S, U16-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	14
Mean	57.5
Std Dev	15.99

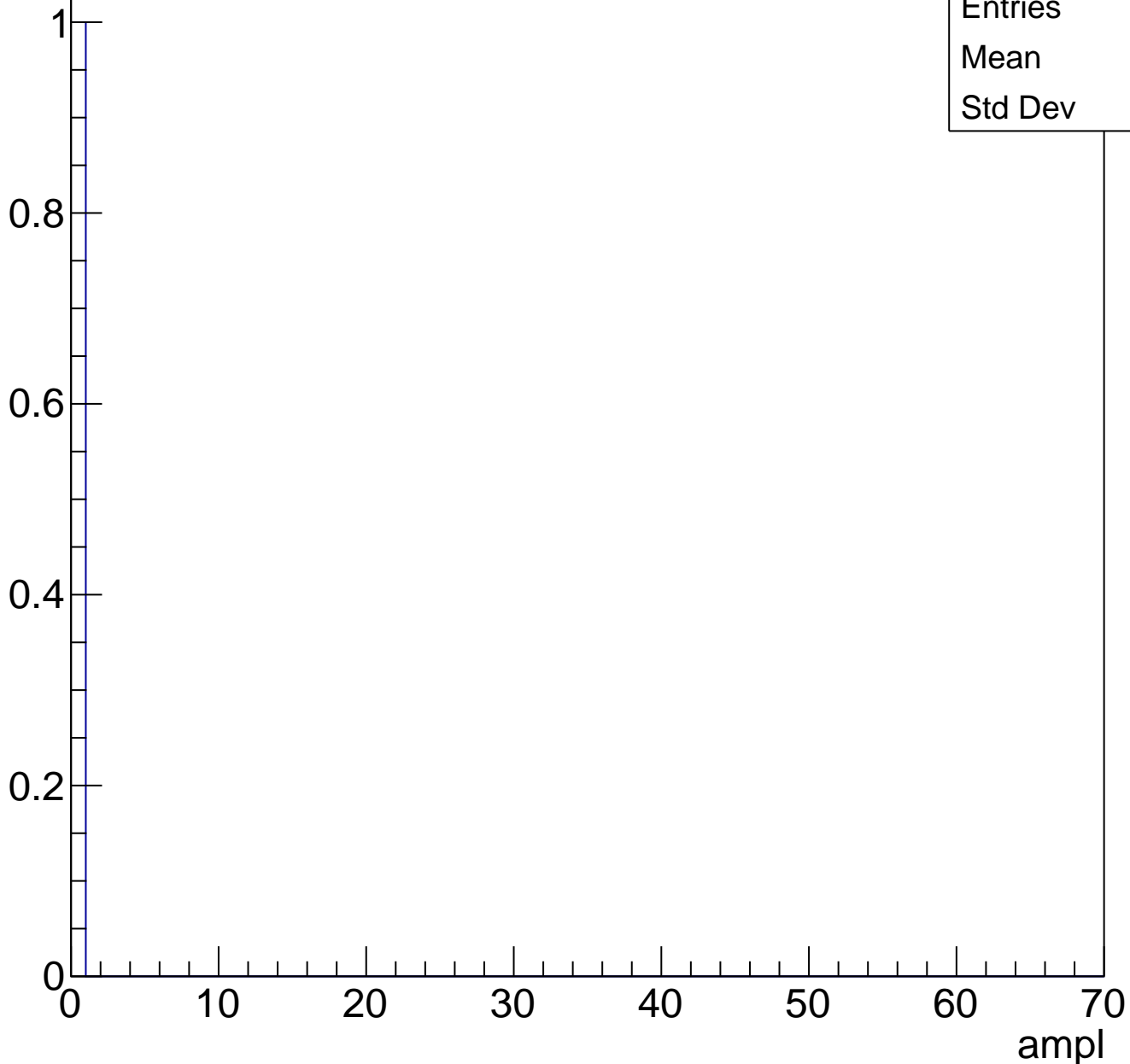




# B1L101S, U16-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U16-ch127, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	69
Mean	31.1
Std Dev	6.418

**Gaus mean : 33.0220**

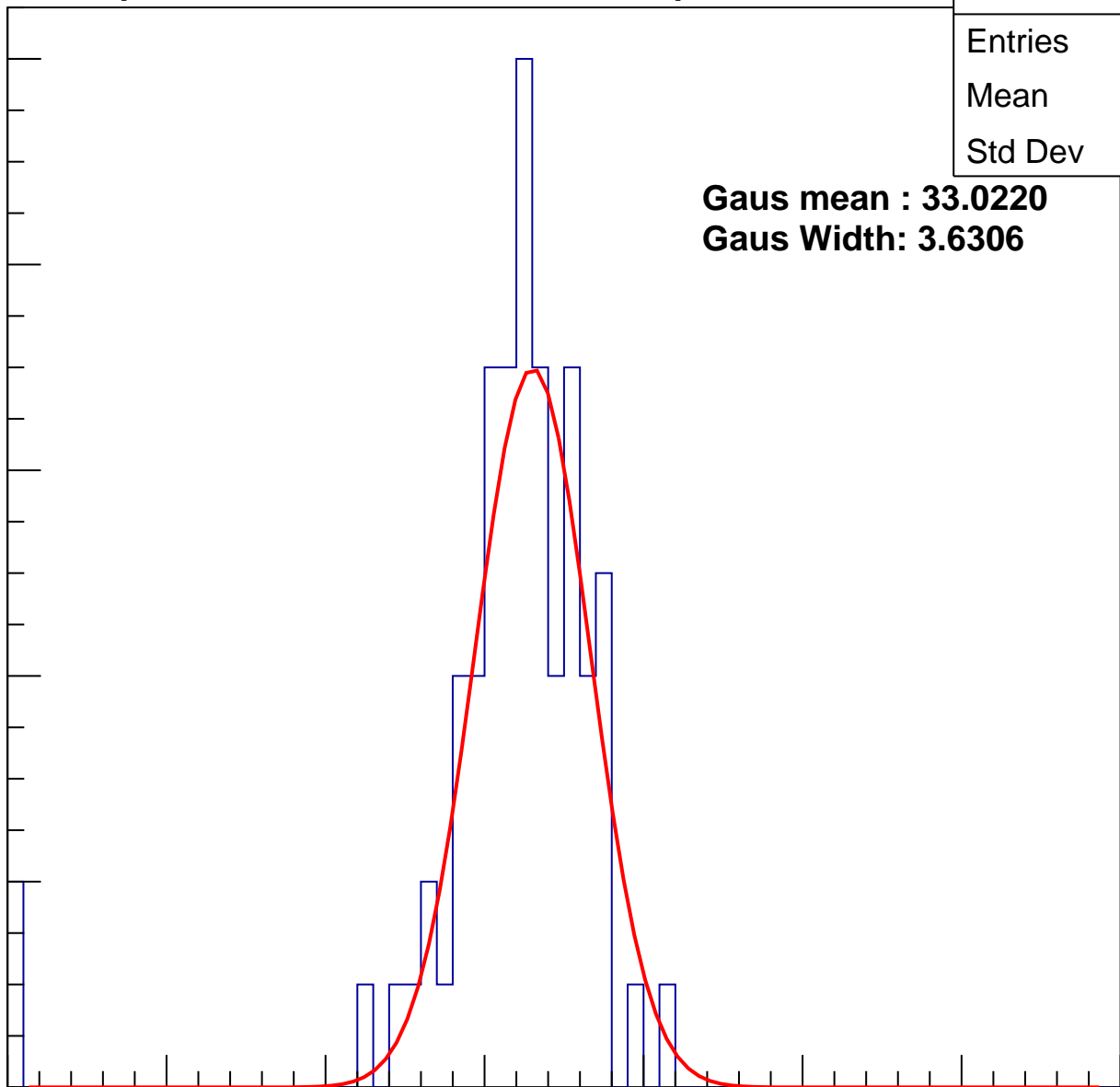
**Gaus Width: 3.6306**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U16-ch127, adc1

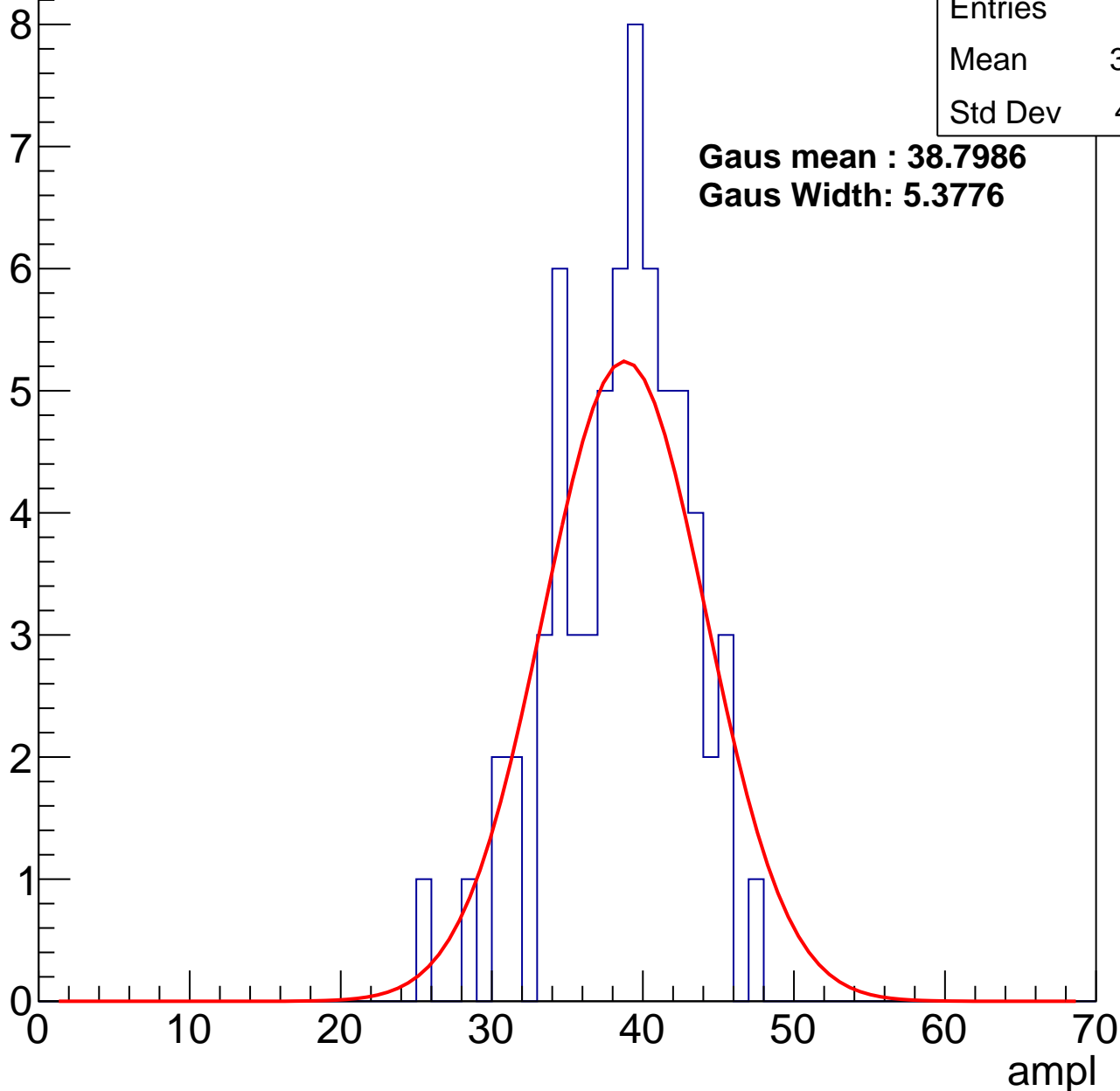
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	38.08
Std Dev	4.381

**Gaus mean : 38.7986**

**Gaus Width: 5.3776**



# B1L101S, U16-ch127, adc2

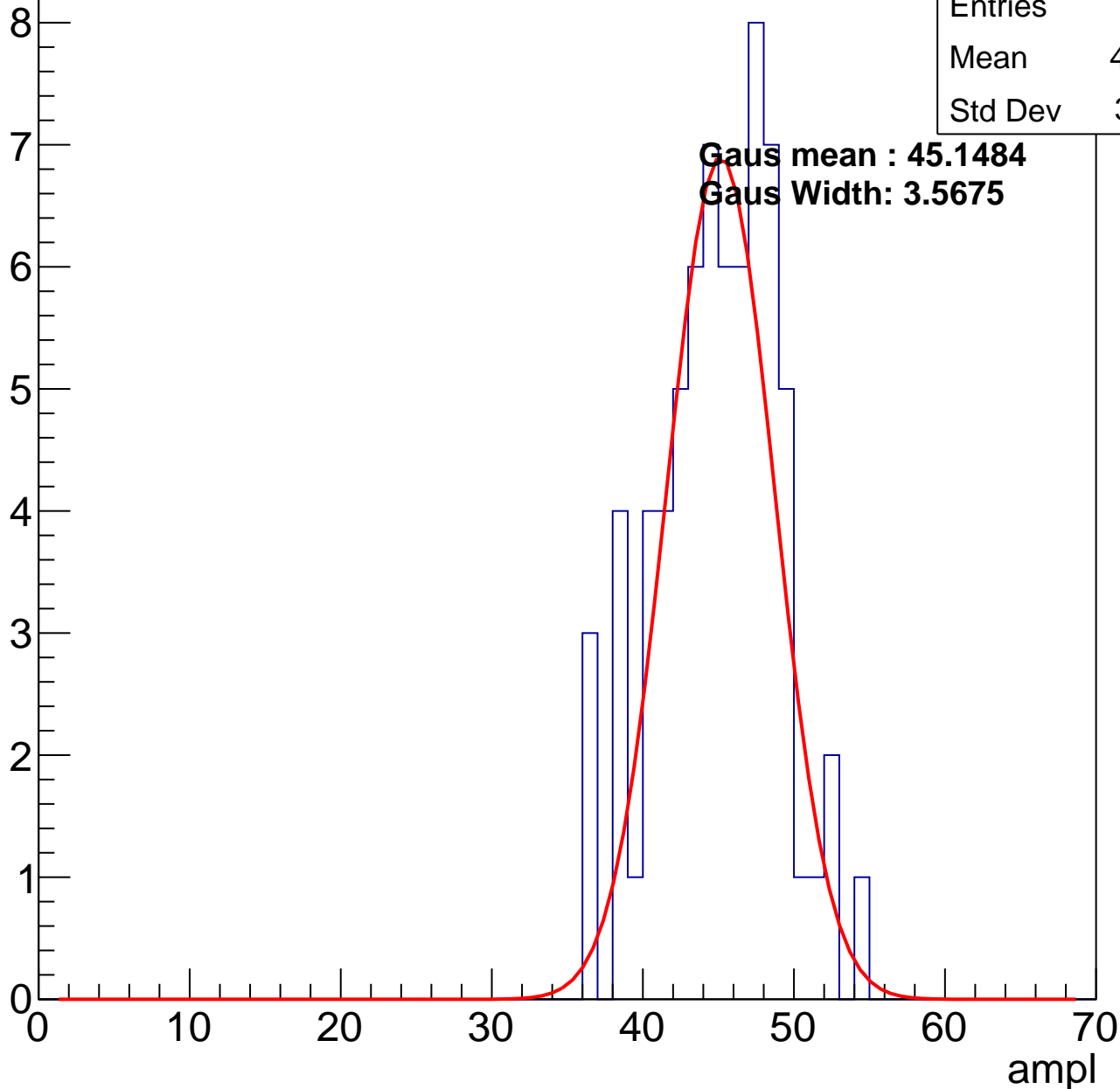
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	44.52
Std Dev	3.971

Gaus mean : 45.1484

Gaus Width: 3.5675

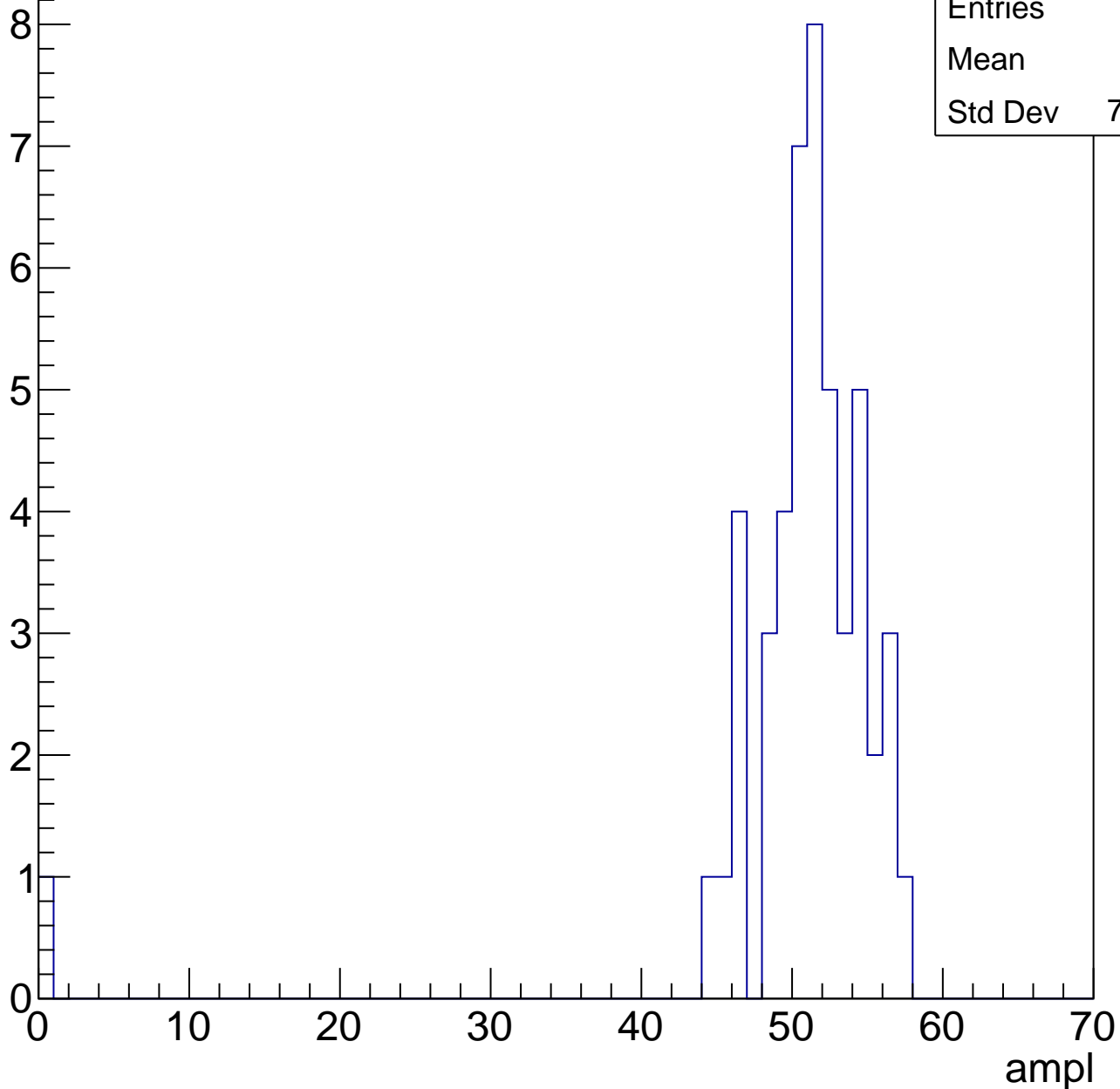


# B1L101S, U16-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	49.9
Std Dev	7.883

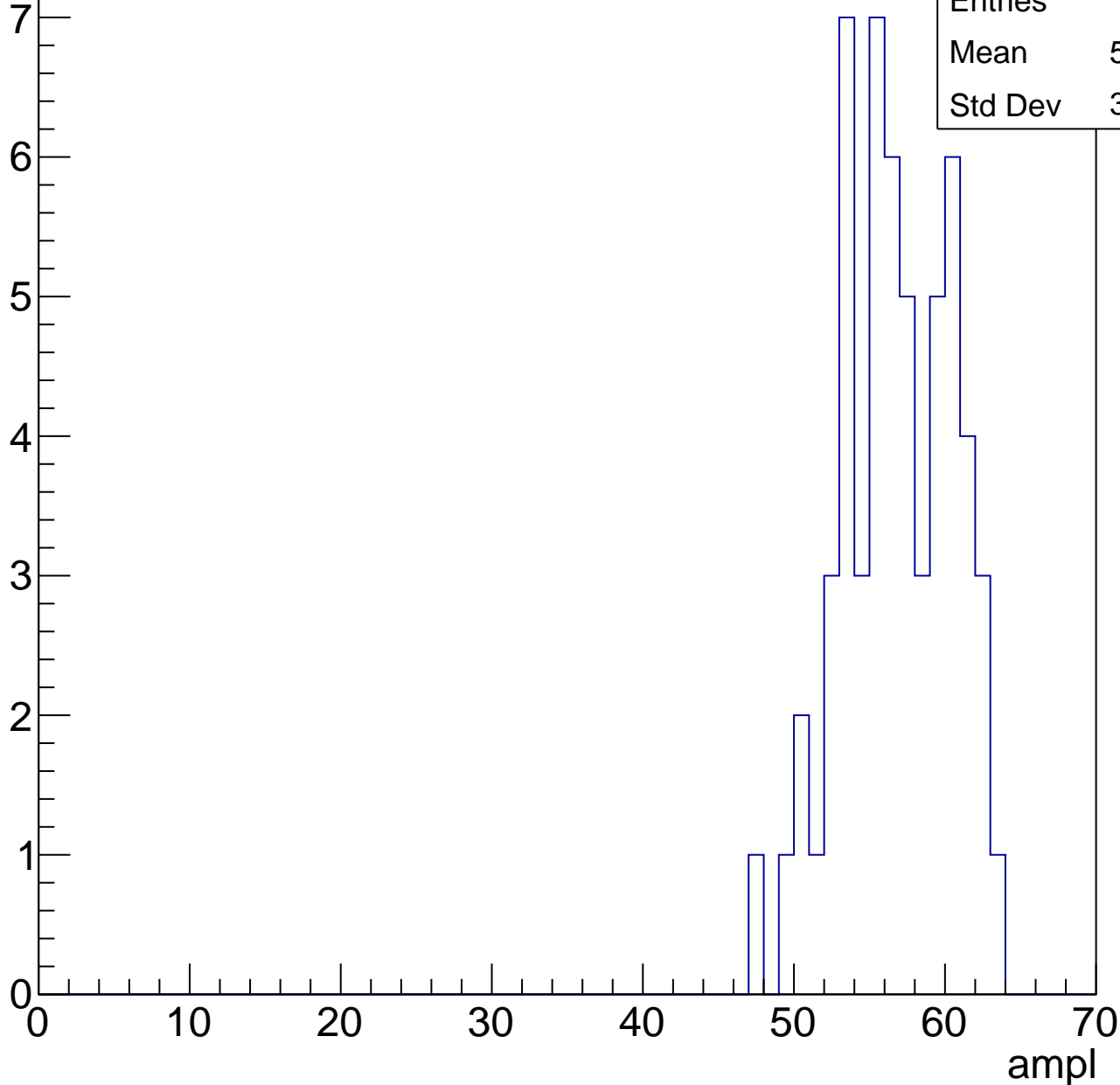


# B1L101S, U16-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

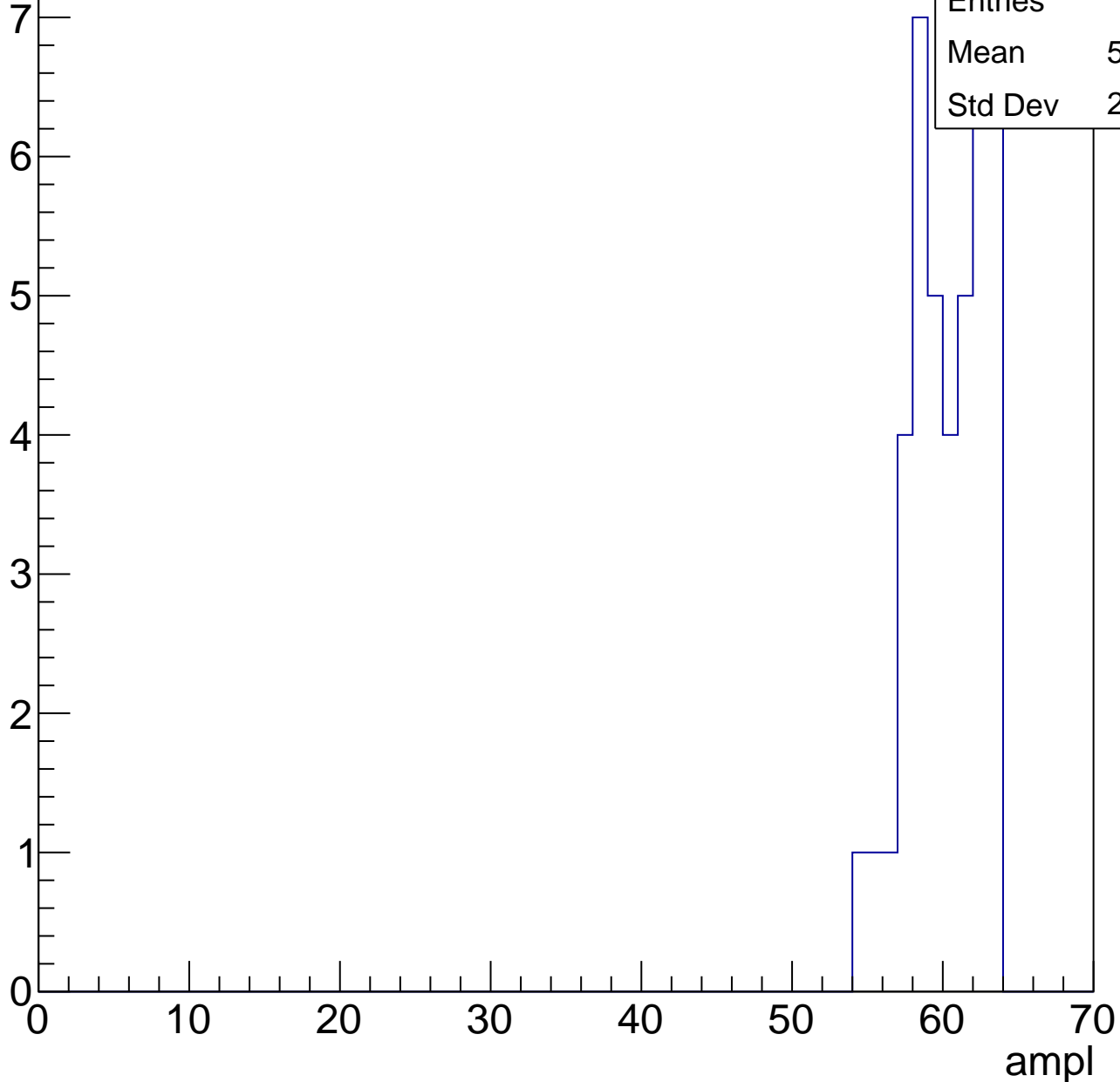
Entries	58
Mean	56.28
Std Dev	3.638



# B1L101S, U16-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	42
Mean	59.86
Std Dev	2.396

# B1L101S, U16-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

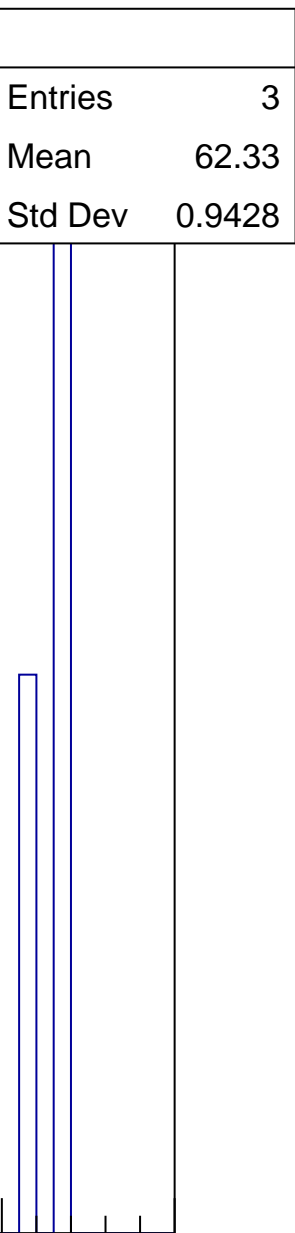
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.9428

0 10 20 30 40 50 60 70

ampl





# B1L101S, U16-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U16-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0