

B0L002S, U7-ch0

calib_packv5_042523_0143.root, FC#8, port C1

Entries	371
Mean	44.64
Std Dev	11.47

Turn on : 27.0087

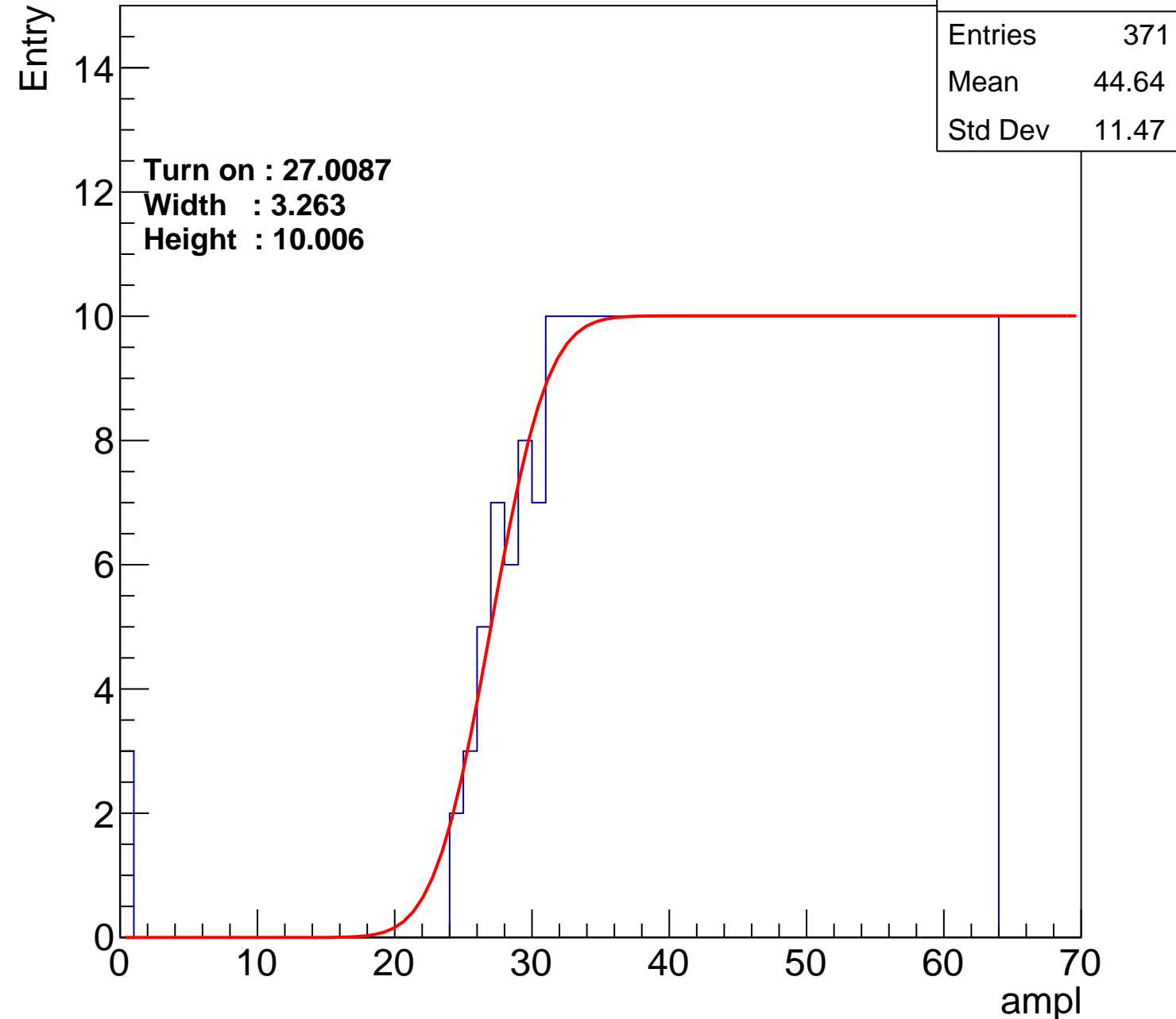
Width : 3.263

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch1

calib_packv5_042523_0143.root, FC#8, port C1

Entries	359
Mean	45.37
Std Dev	10.77

Turn on : 28.7455

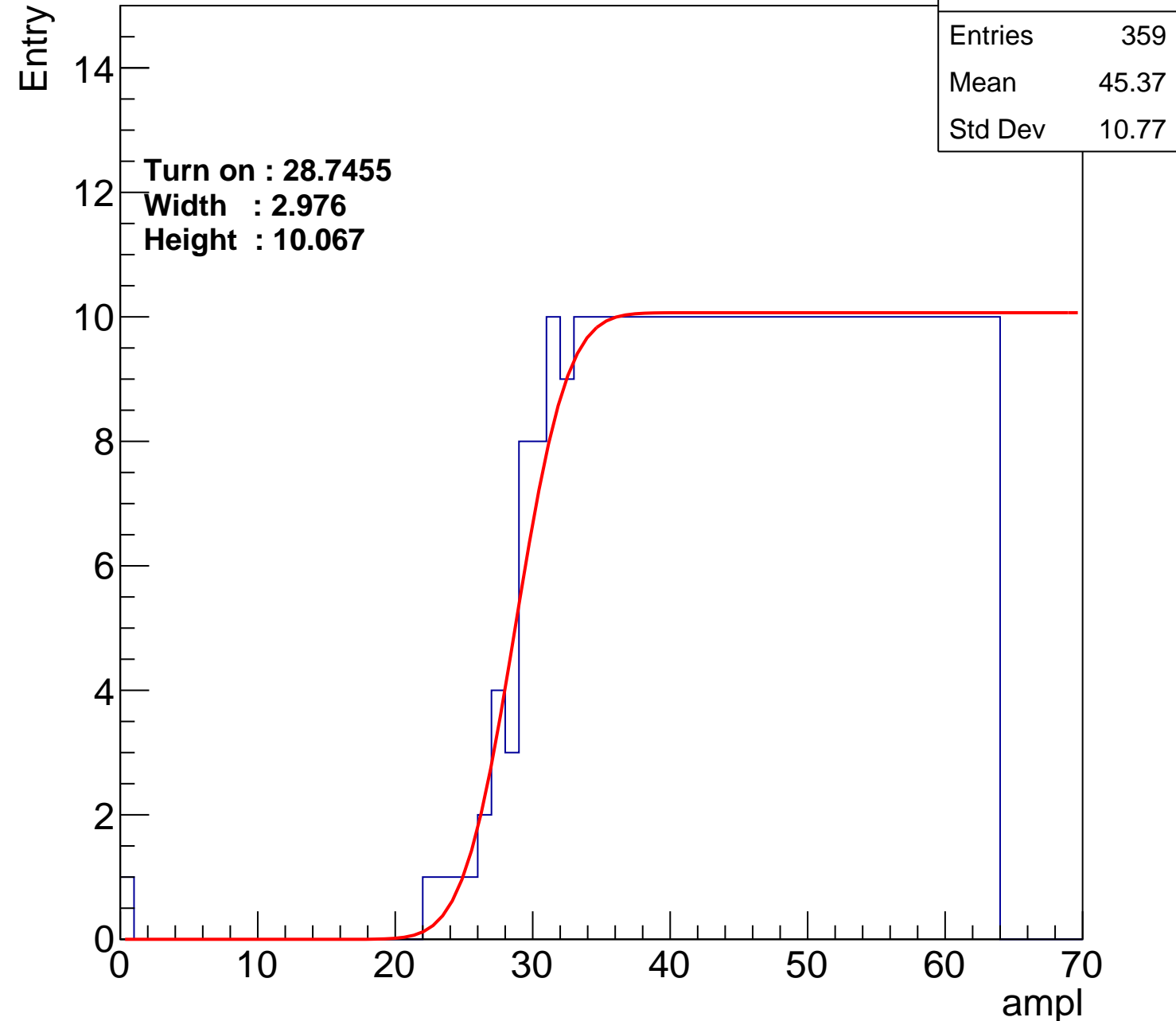
Width : 2.976

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch2

calib_packv5_042523_0143.root, FC#8, port C1

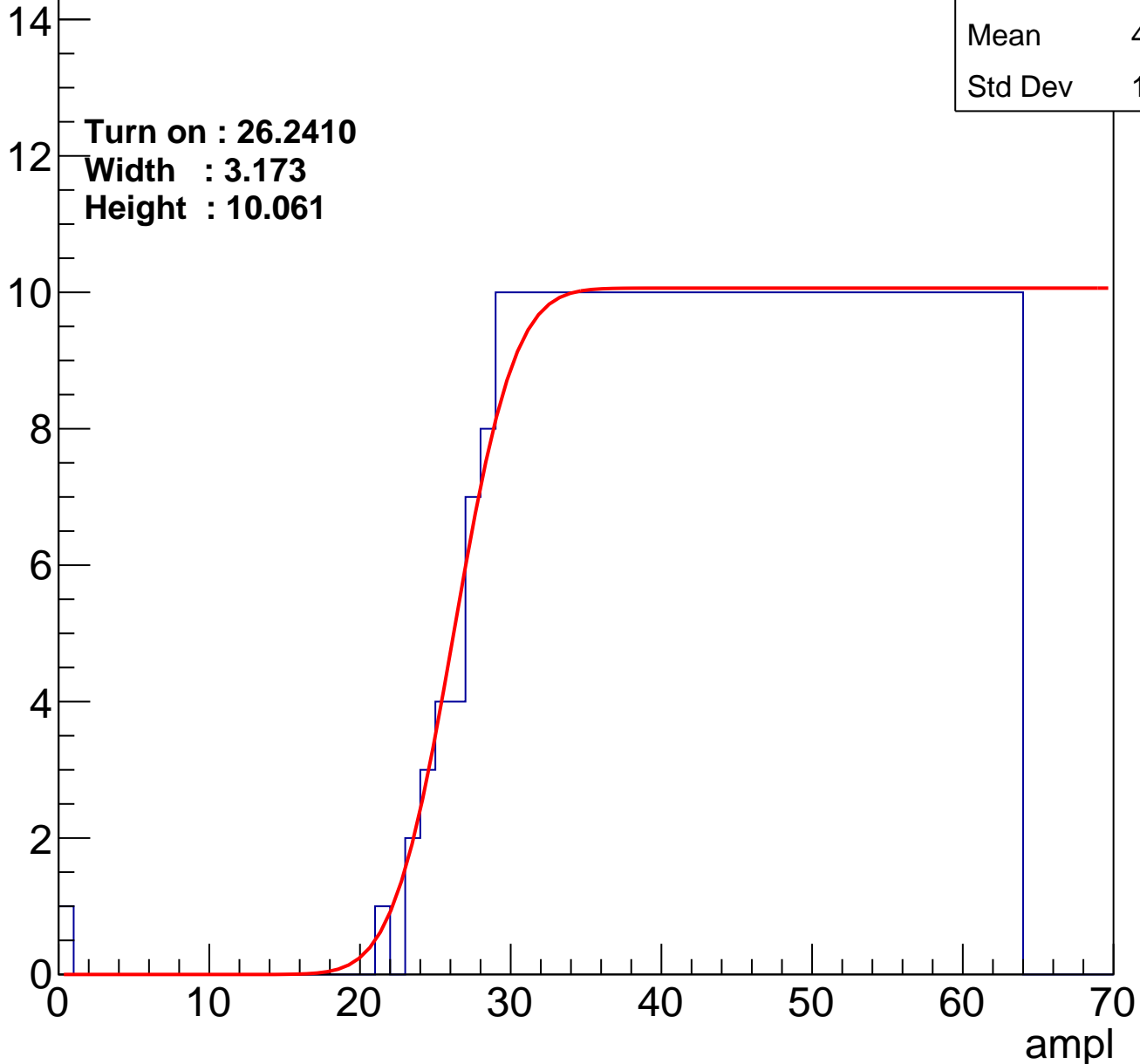
Entries	380
Mean	44.36
Std Dev	11.29

Turn on : 26.2410

Width : 3.173

Height : 10.061

Entry



B0L002S, U7-ch3

calib_packv5_042523_0143.root, FC#8, port C1

Entries	367
Mean	44.95
Std Dev	11.02

Turn on : 27.6445

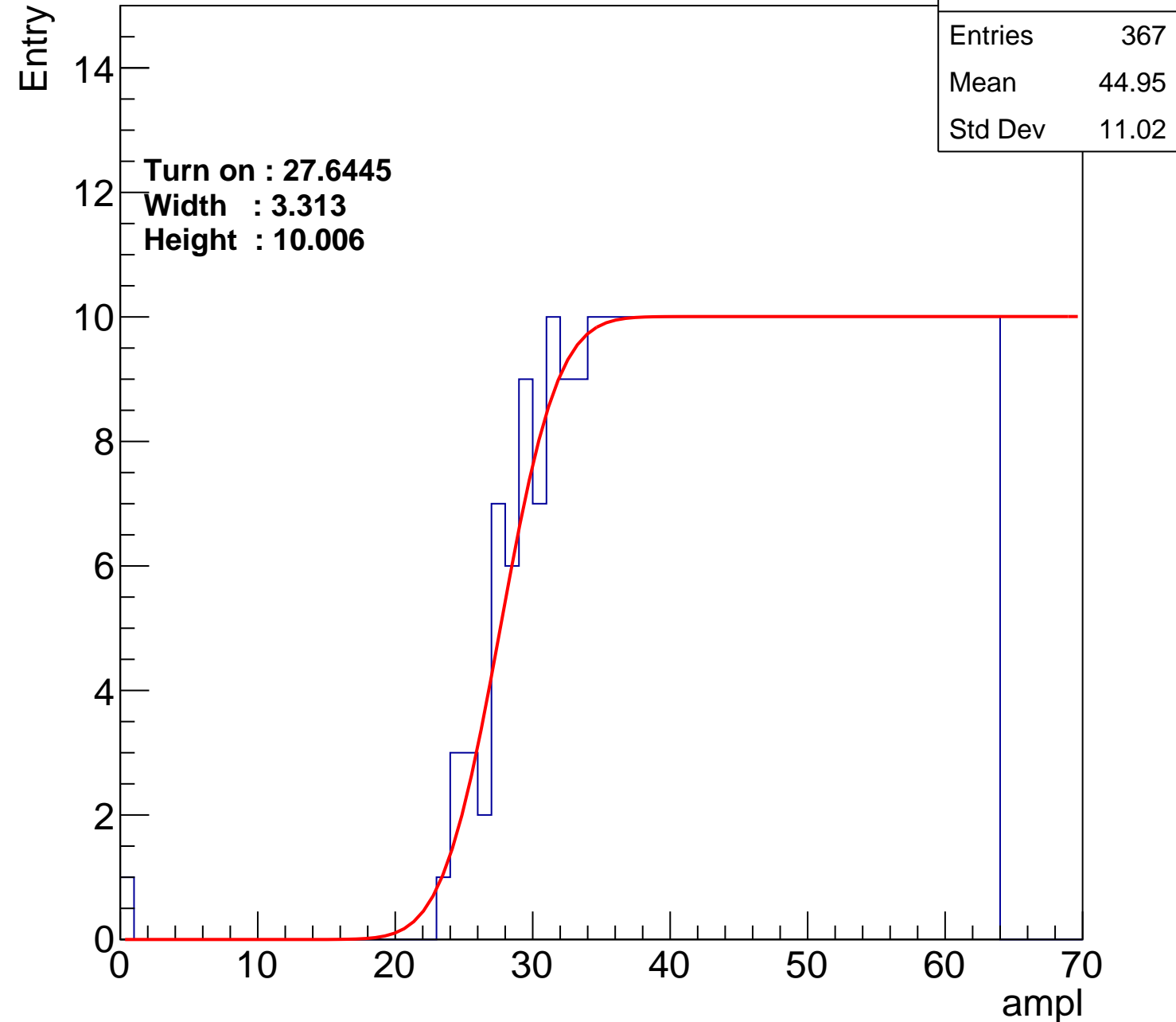
Width : 3.313

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch4

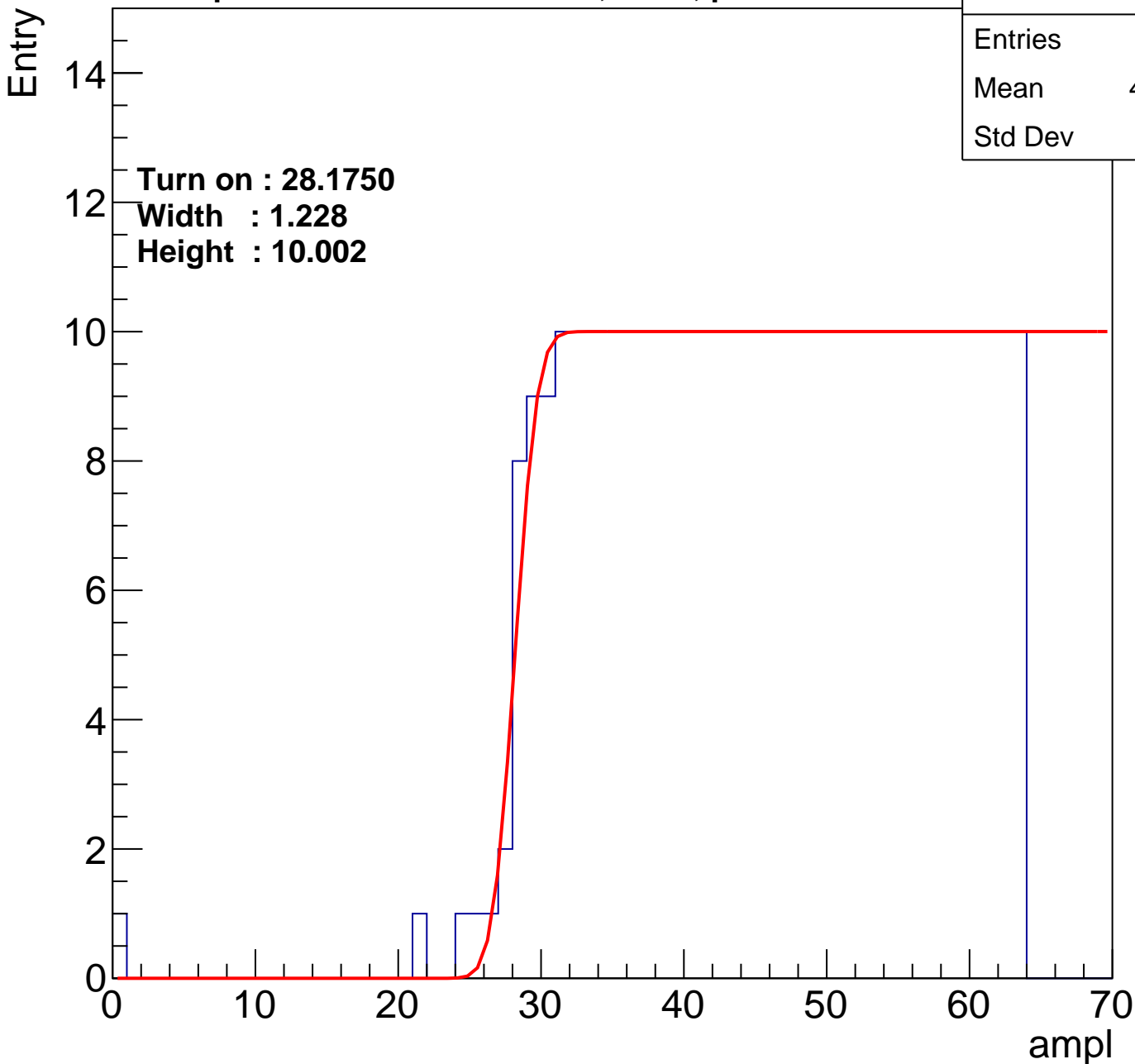
calib_packv5_042523_0143.root, FC#8, port C1

Entries	363
Mean	45.22
Std Dev	10.8

Turn on : 28.1750

Width : 1.228

Height : 10.002



B0L002S, U7-ch5

calib_packv5_042523_0143.root, FC#8, port C1

Entries	340
Mean	46.18
Std Dev	10.59

Turn on : 30.2898

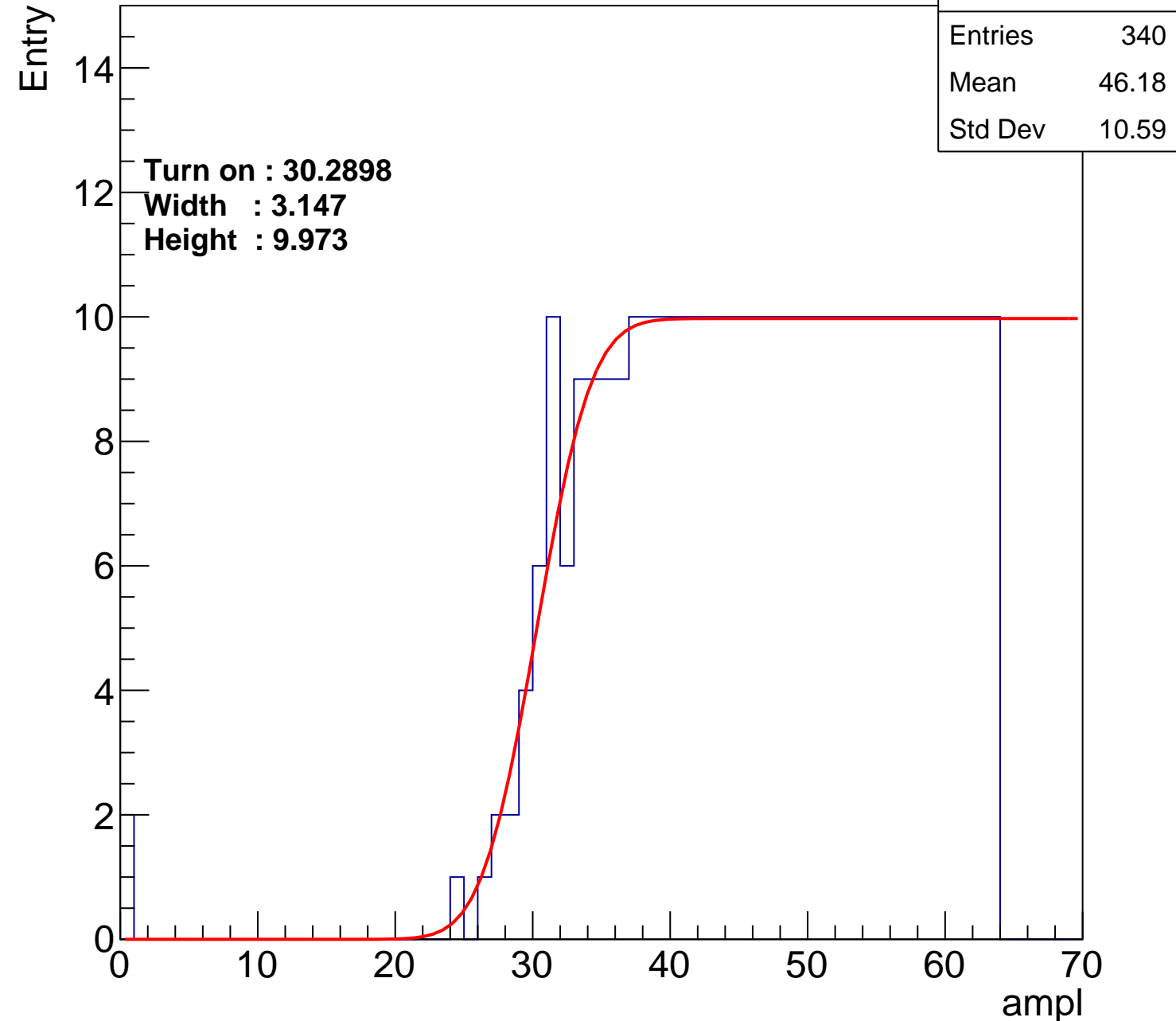
Width : 3.147

Height : 9.973

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch6

calib_packv5_042523_0143.root, FC#8, port C1

Entries	355
Mean	45.53
Std Dev	10.72

Turn on : 28.9401

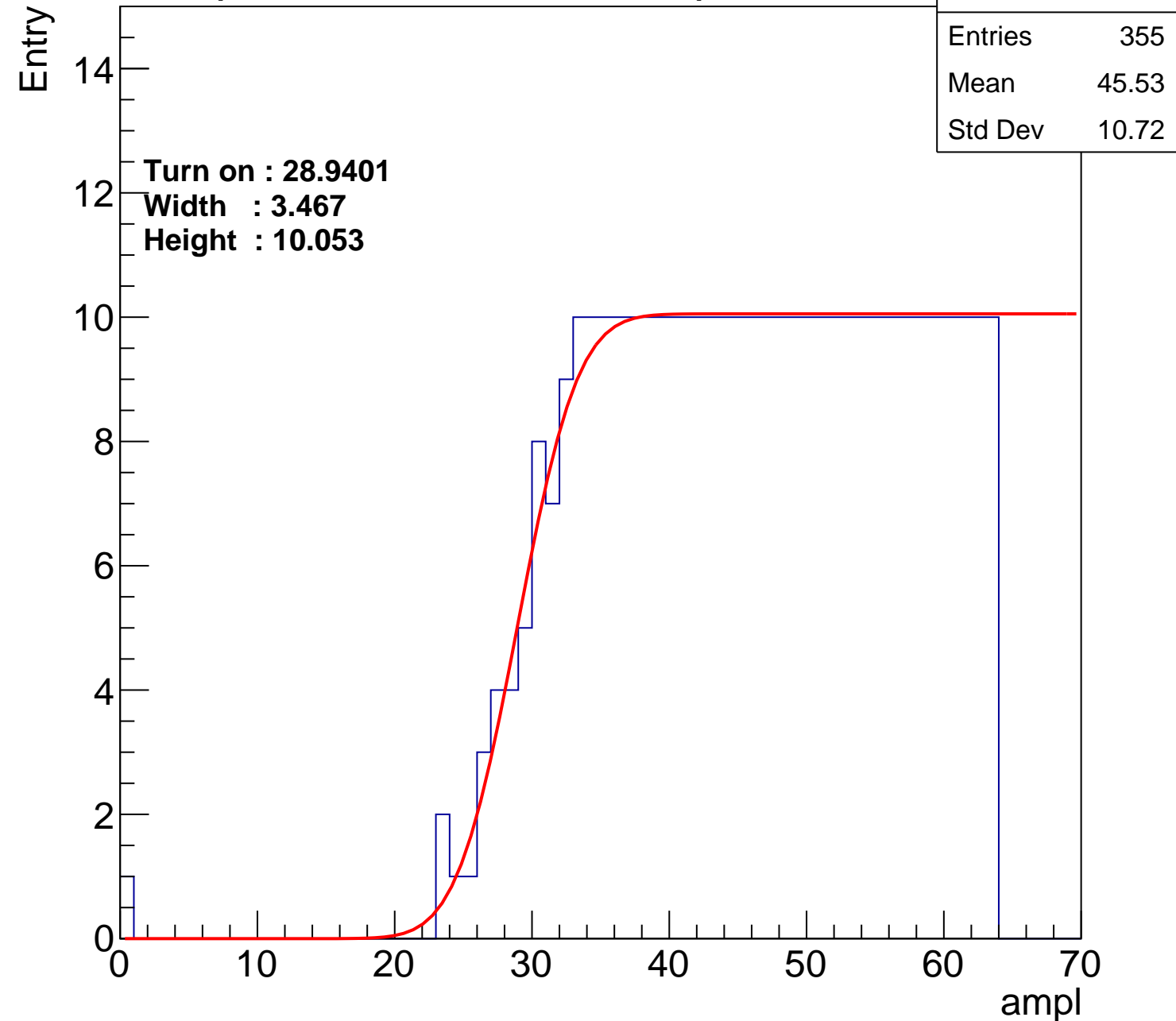
Width : 3.467

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch7

calib_packv5_042523_0143.root, FC#8, port C1

Entries	381
Mean	44.24
Std Dev	11.5

Turn on : 26.2632

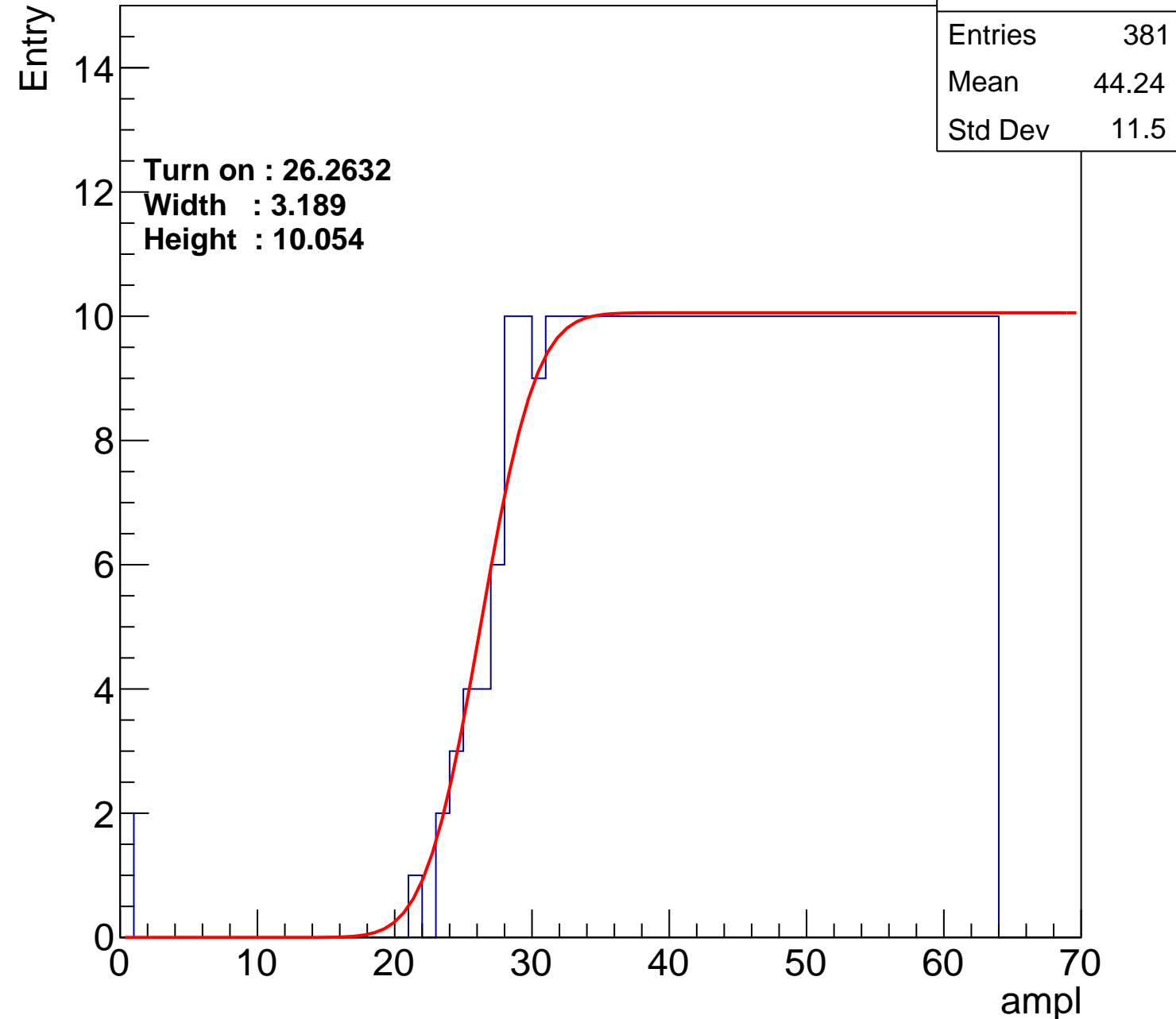
Width : 3.189

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch8

calib_packv5_042523_0143.root, FC#8, port C1

Entries	367
Mean	44.98
Std Dev	10.98

Turn on : 27.6495

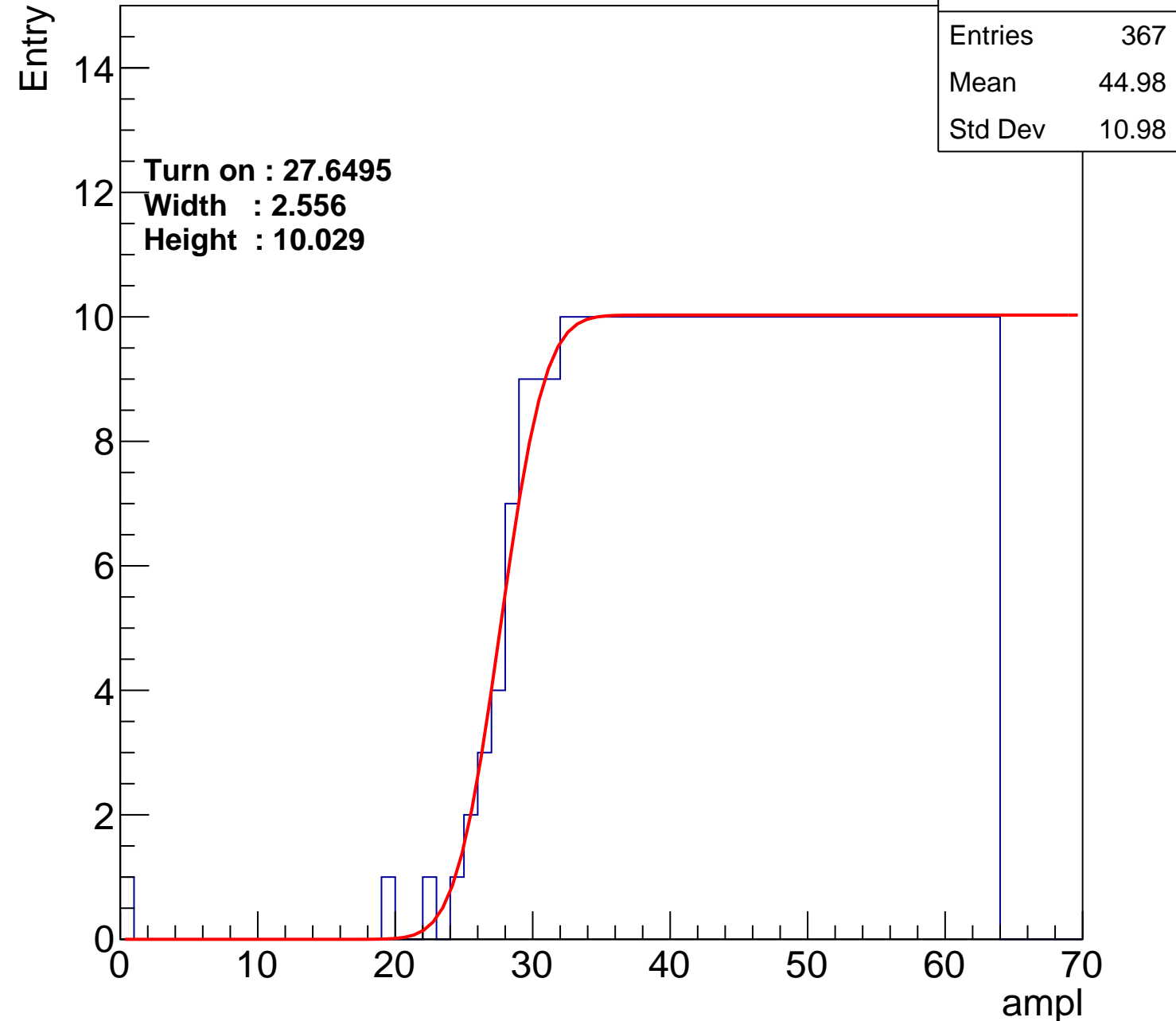
Width : 2.556

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch9

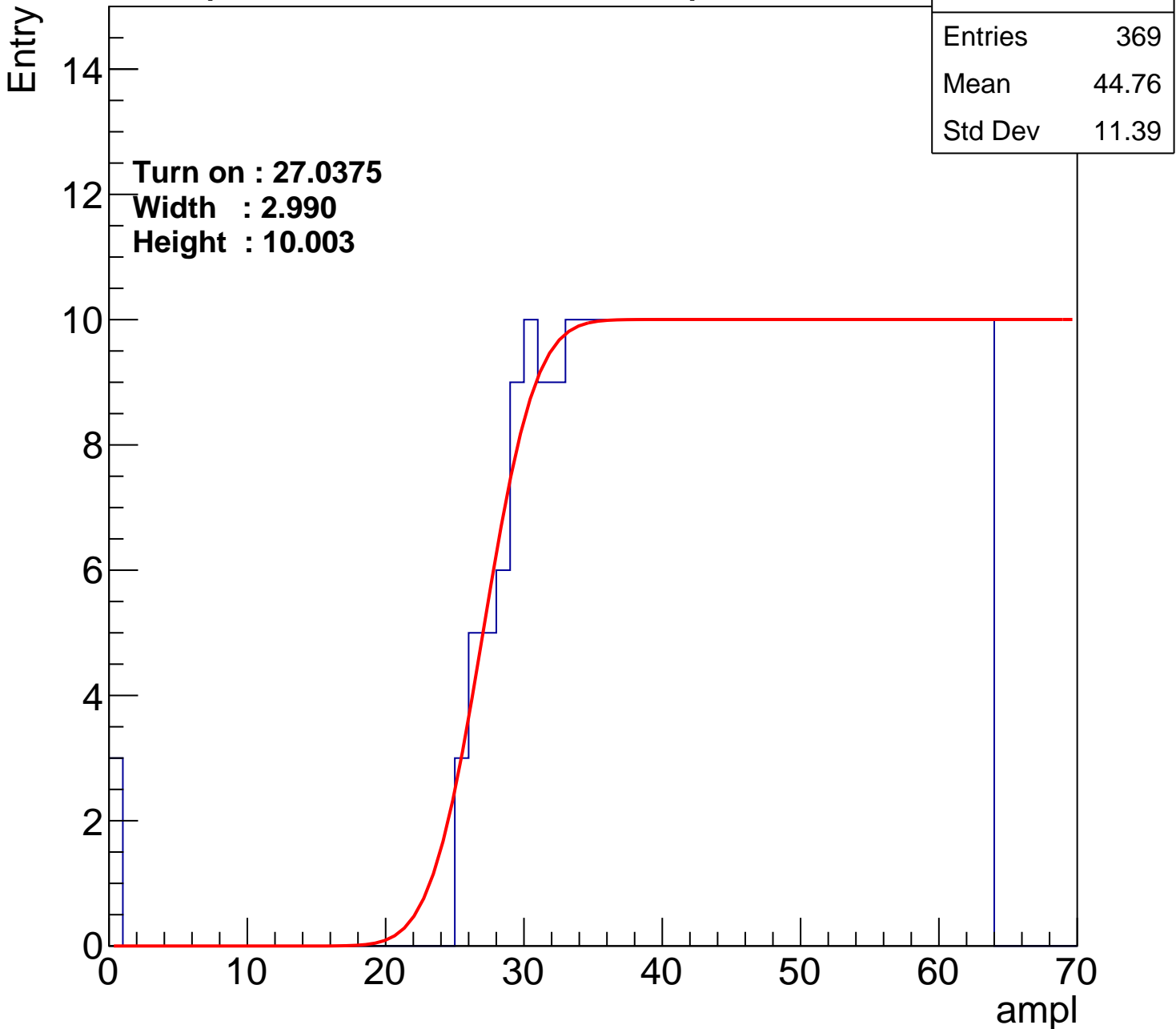
calib_packv5_042523_0143.root, FC#8, port C1

Entries	369
Mean	44.76
Std Dev	11.39

Turn on : 27.0375

Width : 2.990

Height : 10.003



B0L002S, U7-ch10

calib_packv5_042523_0143.root, FC#8, port C1

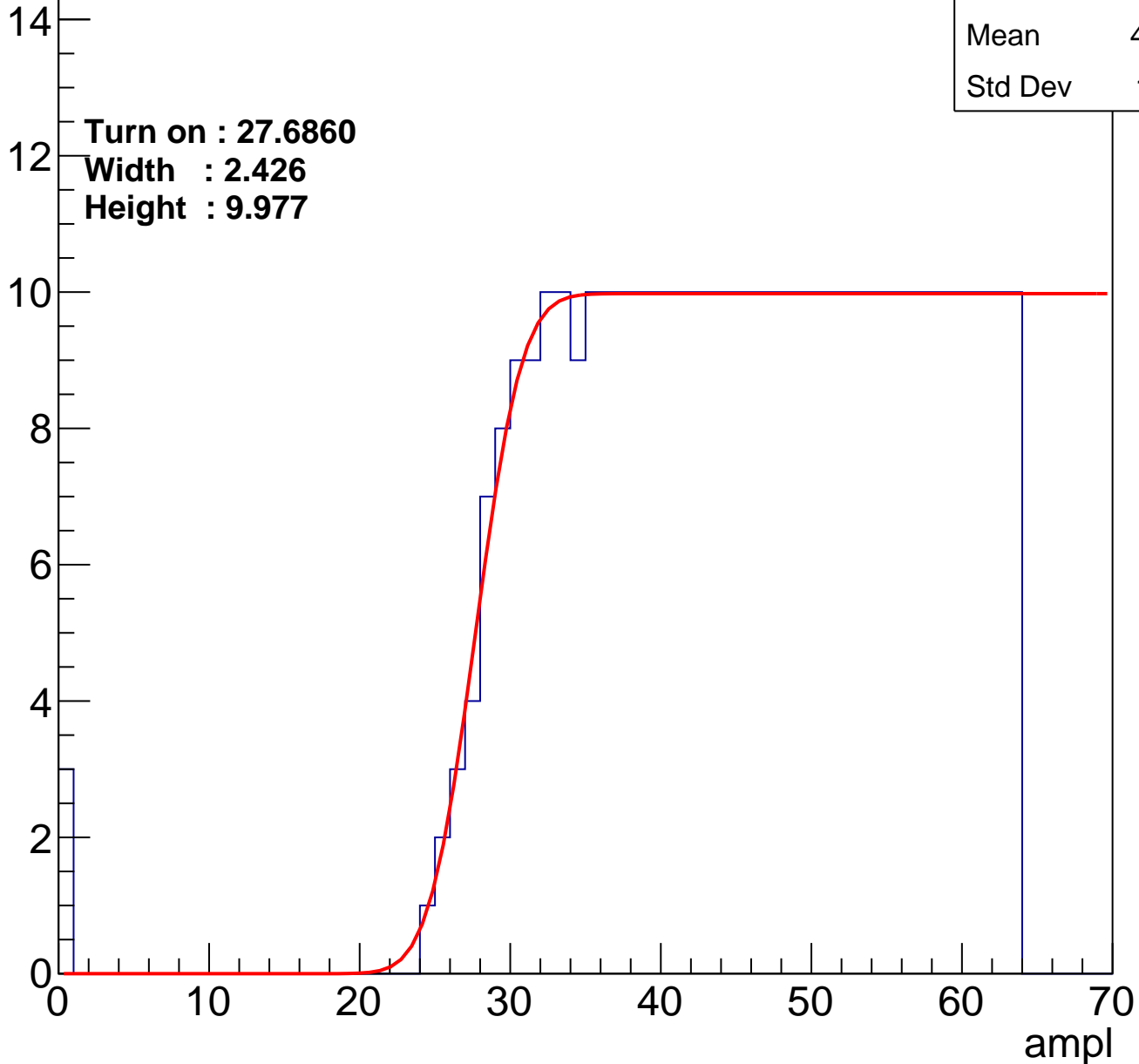
Entries	365
Mean	44.94
Std Dev	11.31

Turn on : 27.6860

Width : 2.426

Height : 9.977

Entry



B0L002S, U7-ch11

calib_packv5_042523_0143.root, FC#8, port C1

Entries	354
Mean	45.64
Std Dev	10.6

Turn on : 29.0918

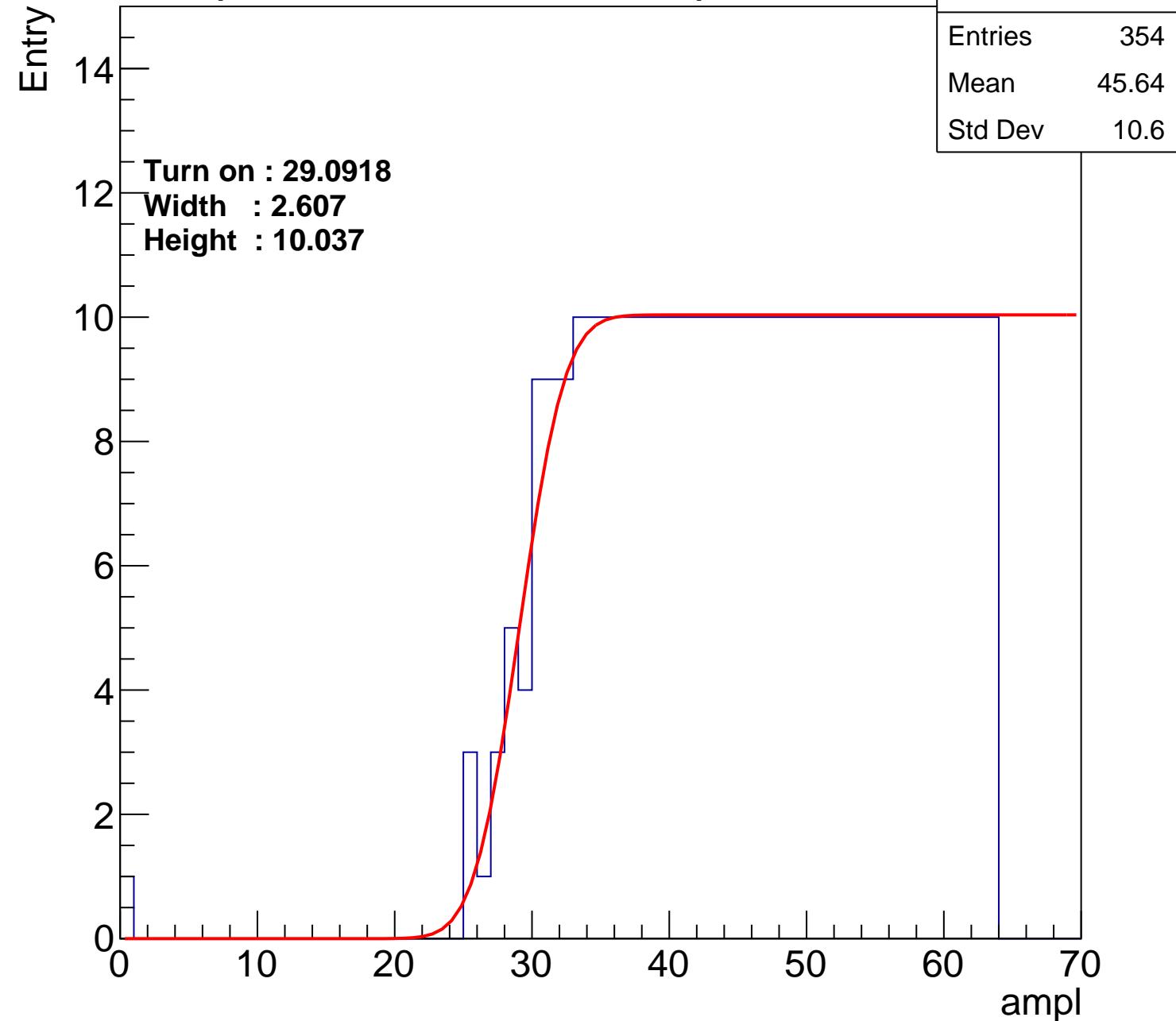
Width : 2.607

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch12

calib_packv5_042523_0143.root, FC#8, port C1

Entries	359
Mean	45.42
Std Dev	10.69

Turn on : 28.3902

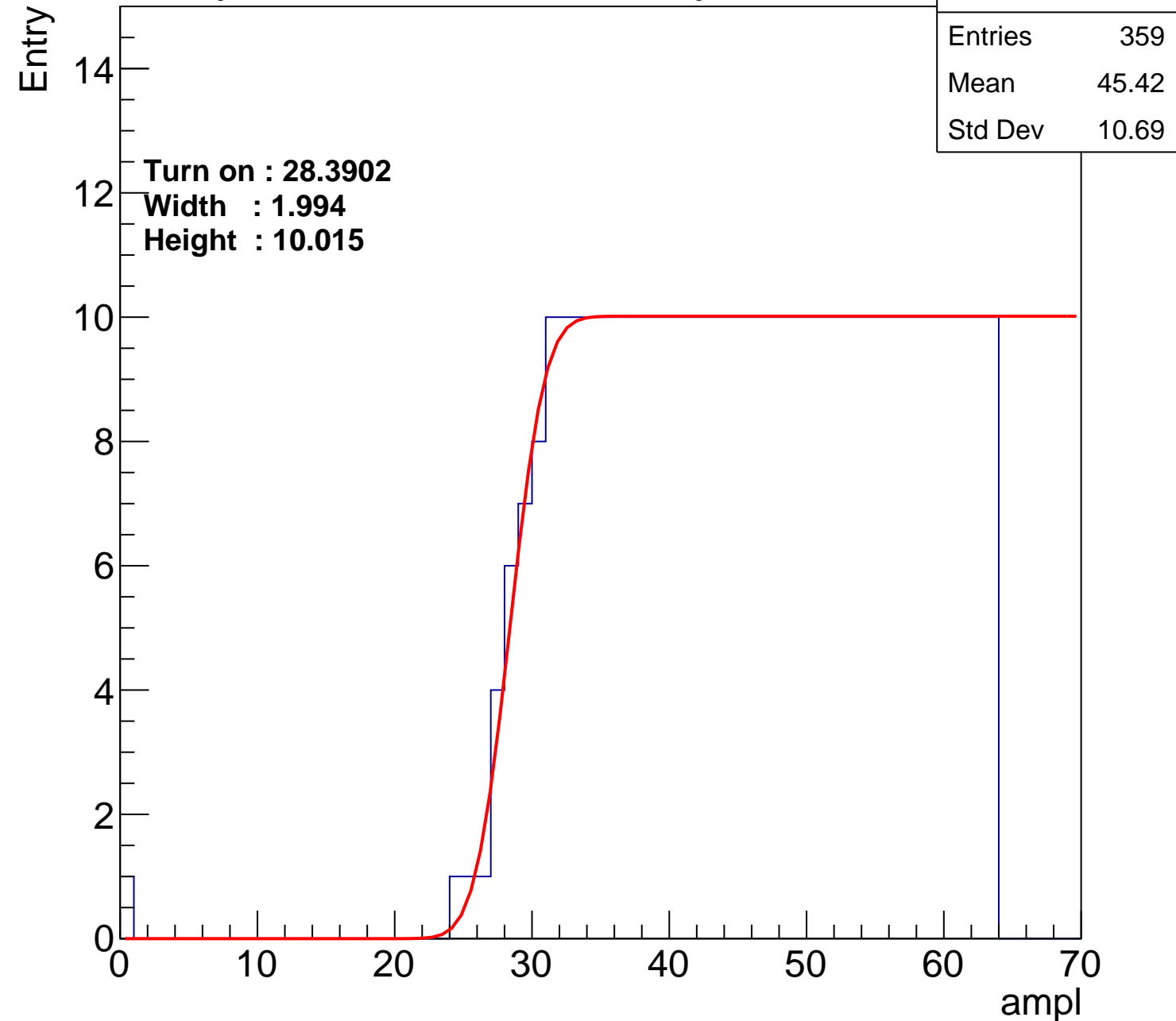
Width : 1.994

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch13

calib_packv5_042523_0143.root, FC#8, port C1

Entries	342
Mean	46.22
Std Dev	10.31

Turn on : 30.1785

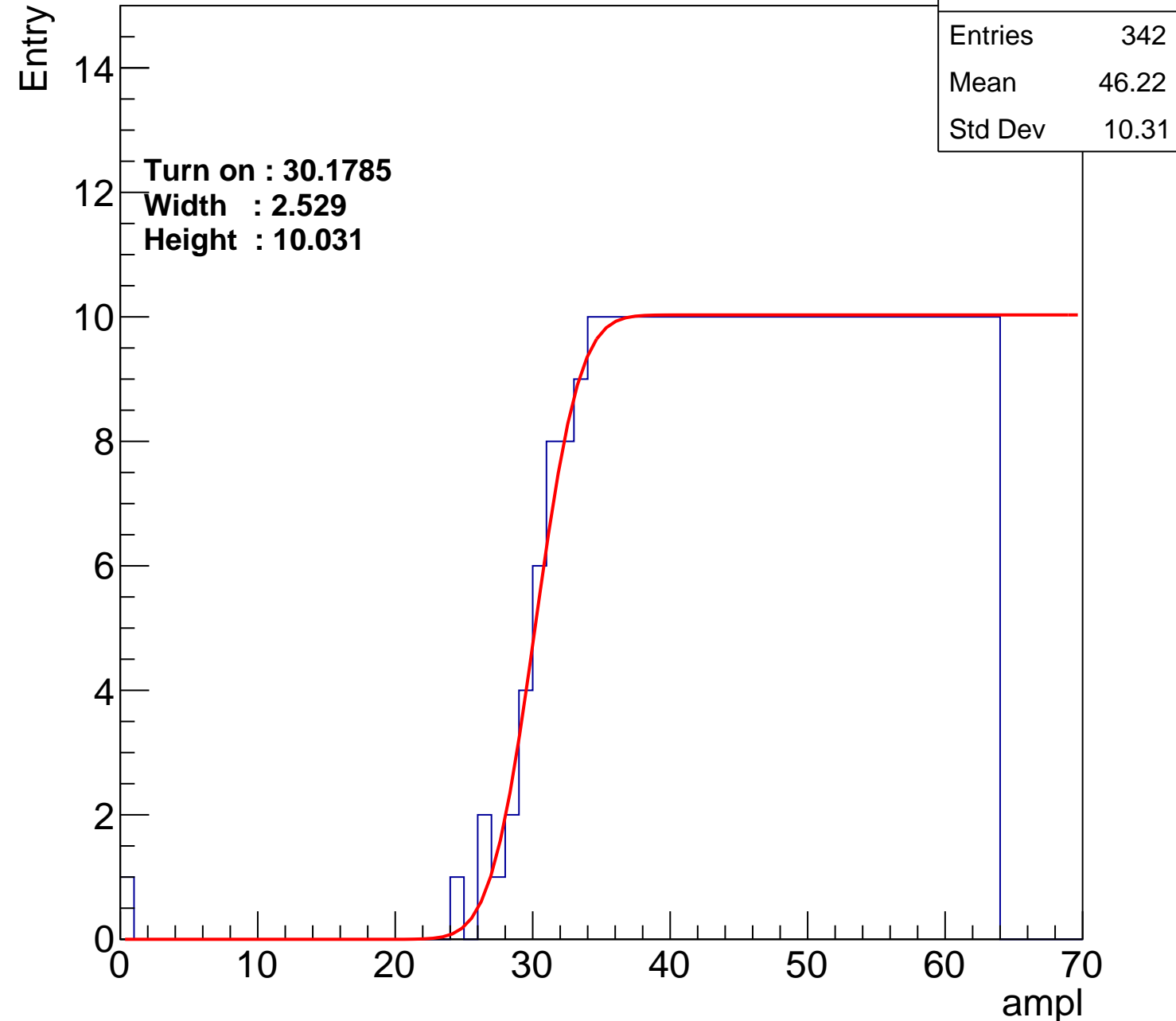
Width : 2.529

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch14

calib_packv5_042523_0143.root, FC#8, port C1

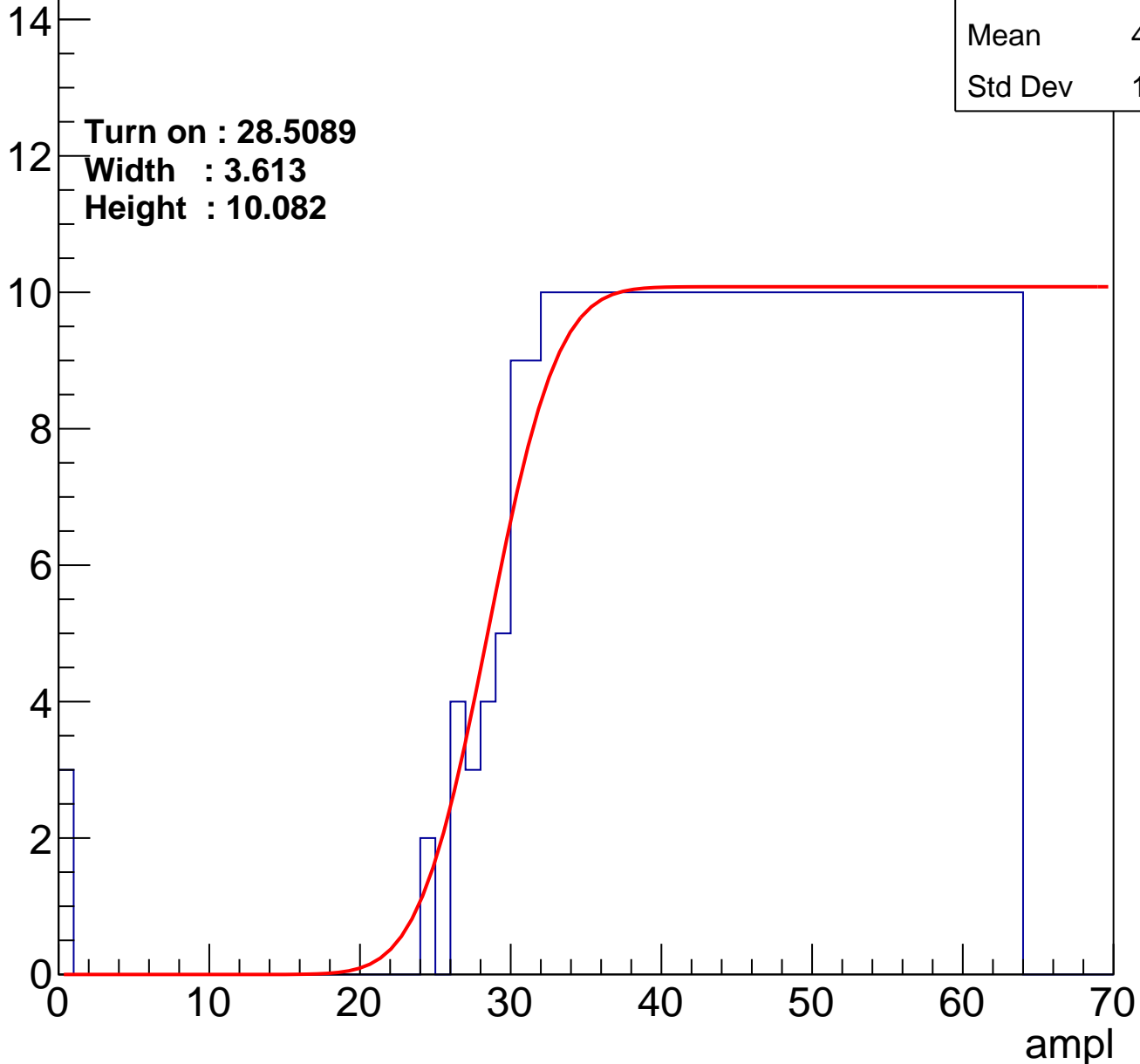
Entries	359
Mean	45.23
Std Dev	11.18

Turn on : 28.5089

Width : 3.613

Height : 10.082

Entry



B0L002S, U7-ch15

calib_packv5_042523_0143.root, FC#8, port C1

Entries	342
Mean	46.13
Std Dev	10.55

Turn on : 29.5079

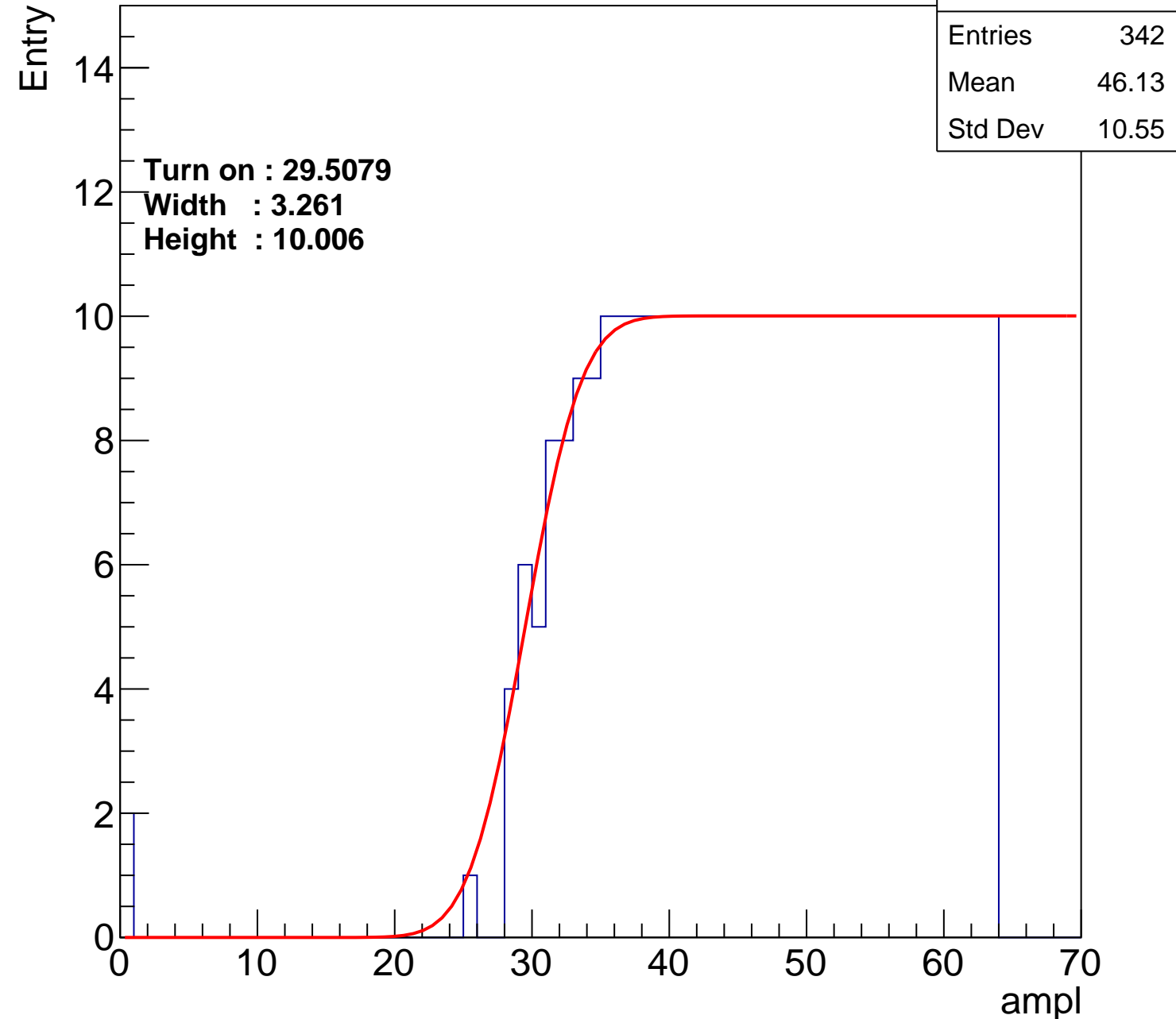
Width : 3.261

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch16

calib_packv5_042523_0143.root, FC#8, port C1

Entries	369
Mean	44.82
Std Dev	11.21

Turn on : 27.2407

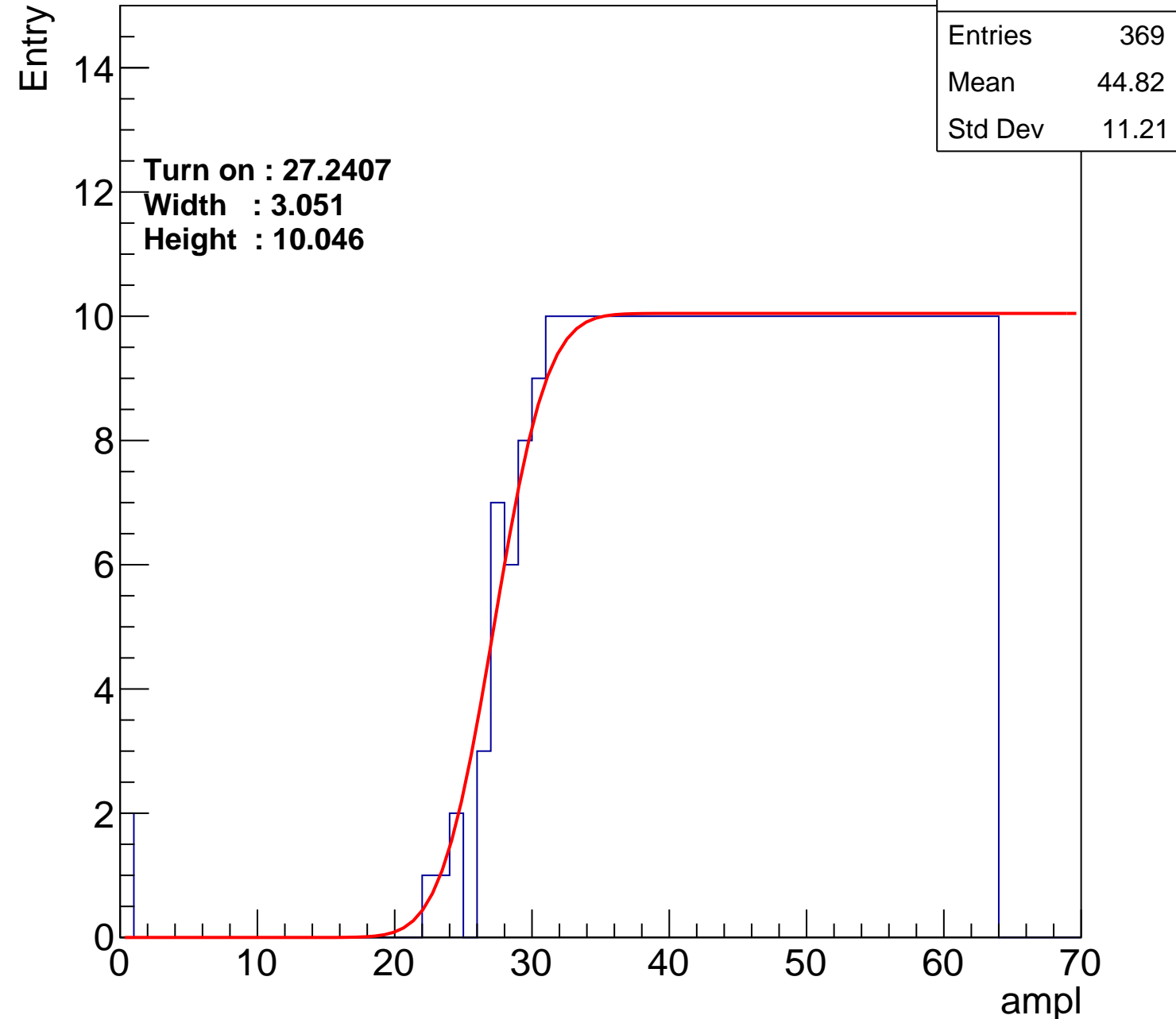
Width : 3.051

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch17

calib_packv5_042523_0143.root, FC#8, port C1

Entries	373
Mean	44.66
Std Dev	11.17

Turn on : 27.1331

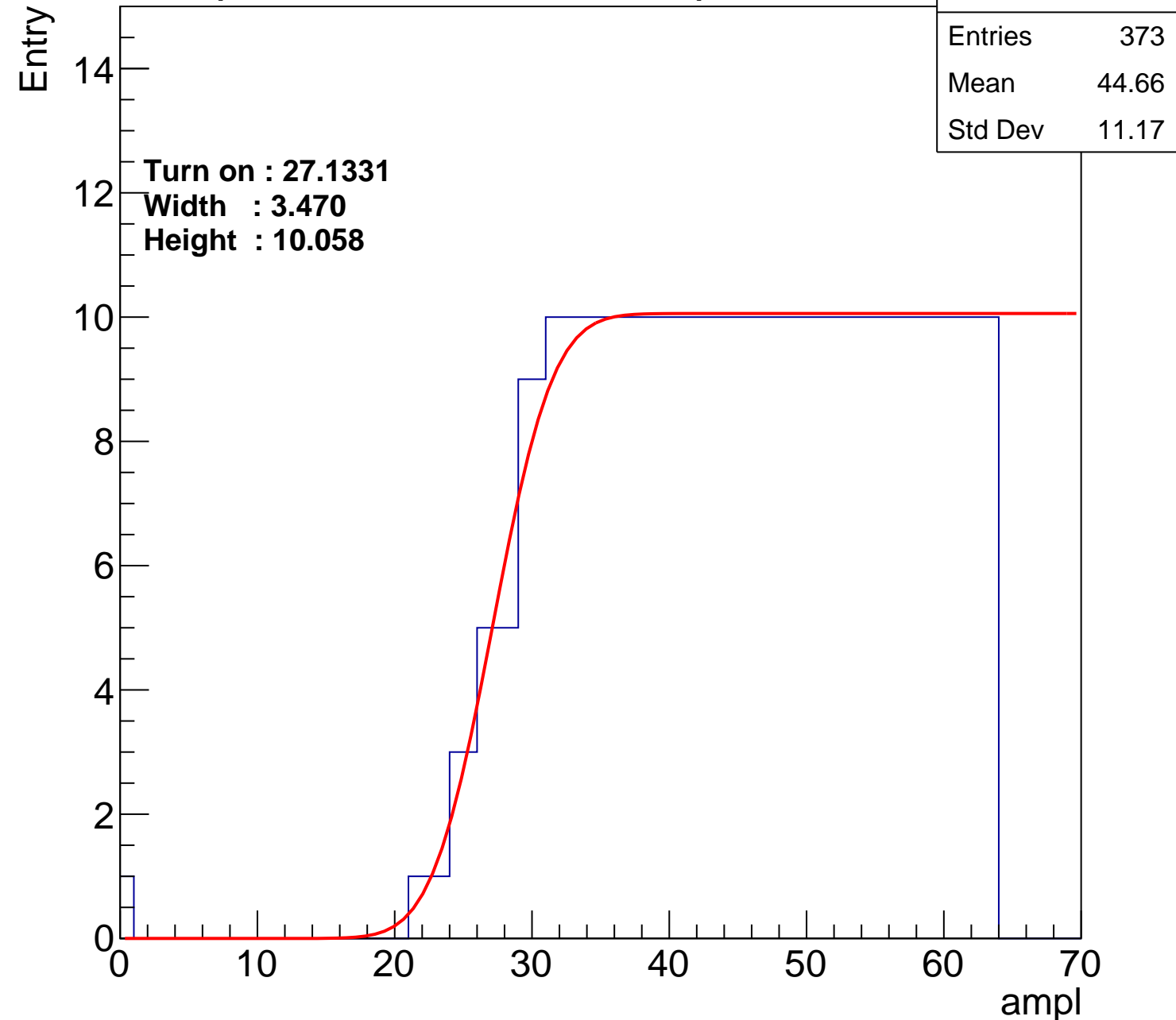
Width : 3.470

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch18

calib_packv5_042523_0143.root, FC#8, port C1

Entries	370
Mean	44.84
Std Dev	11.03

Turn on : 27.1589

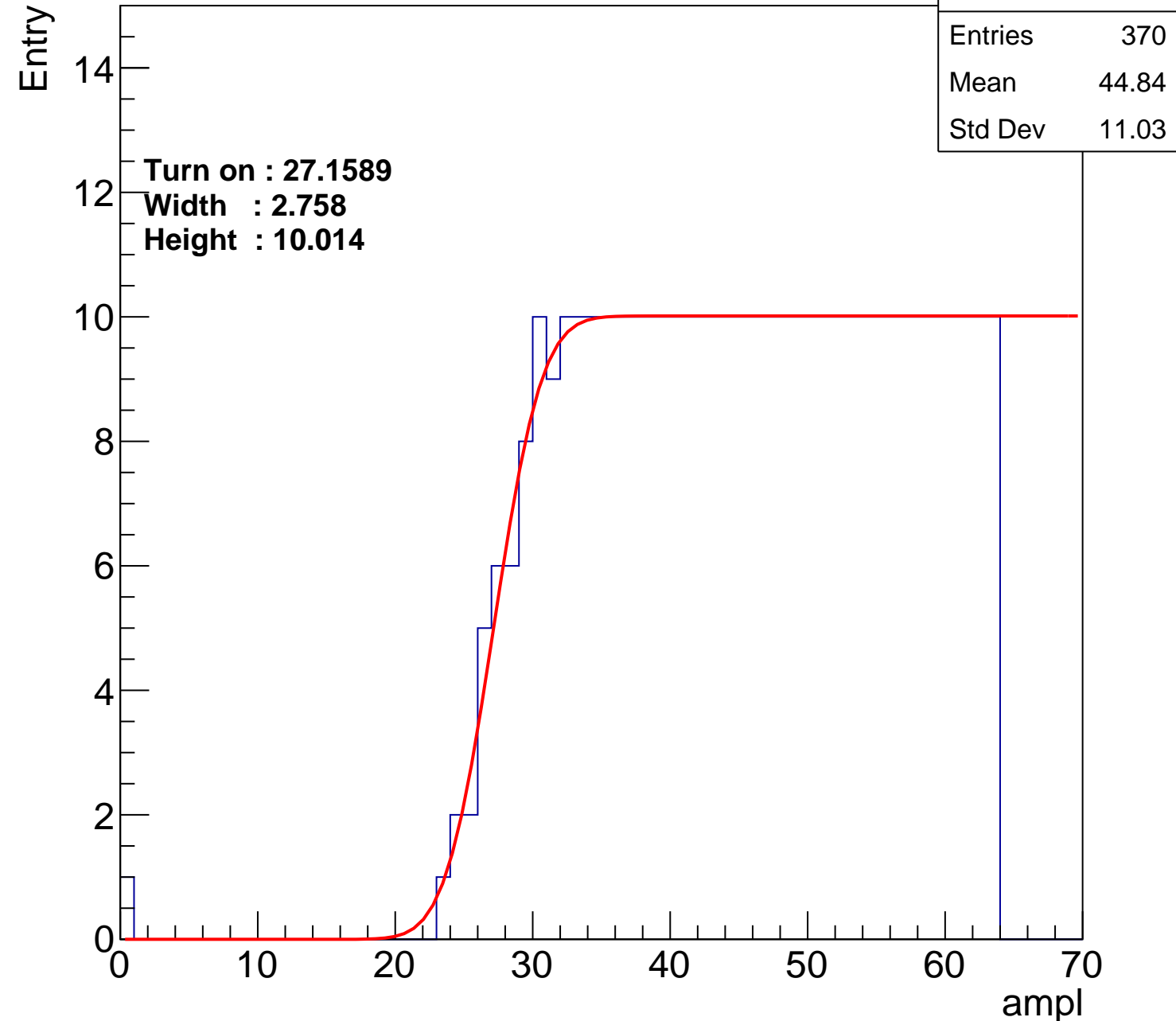
Width : 2.758

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch19

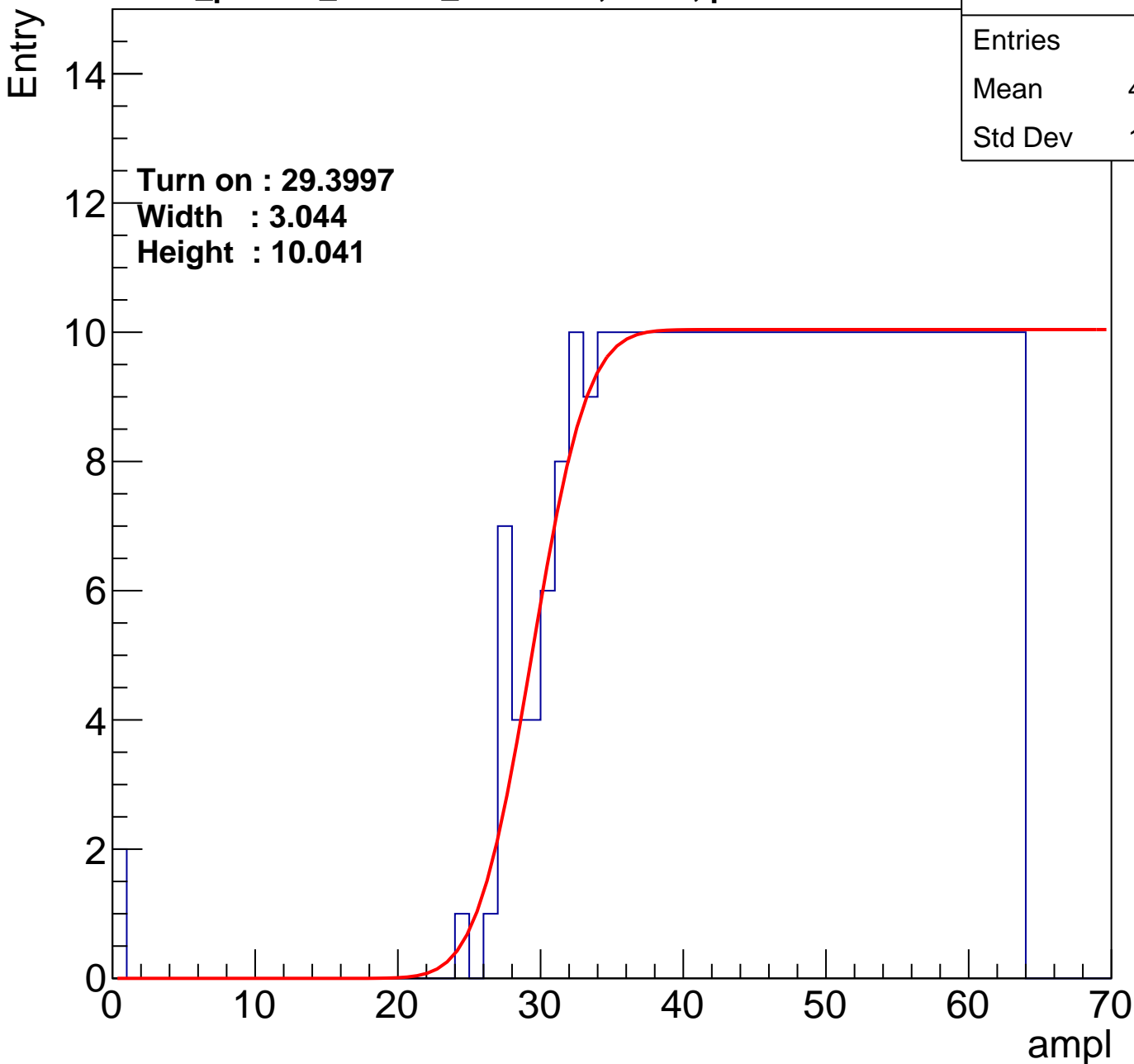
calib_packv5_042523_0143.root, FC#8, port C1

Turn on : 29.3997

Width : 3.044

Height : 10.041

Entries	352
Mean	45.63
Std Dev	10.82



B0L002S, U7-ch20

calib_packv5_042523_0143.root, FC#8, port C1

Entries	363
Mean	45.05
Std Dev	11.26

Turn on : 27.9641

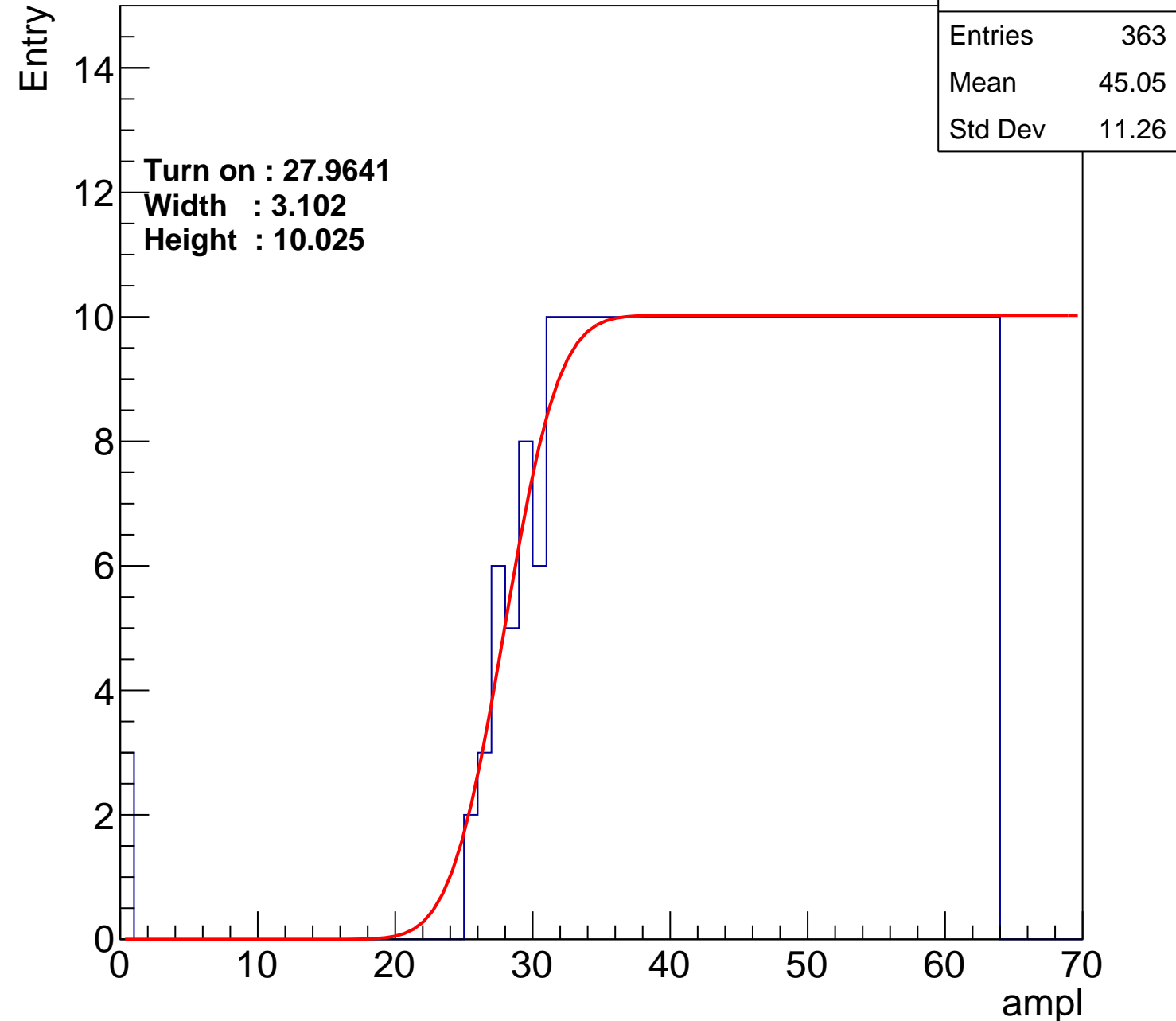
Width : 3.102

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch21

calib_packv5_042523_0143.root, FC#8, port C1

Entries	378
Mean	44.29
Std Dev	11.66

Turn on : 26.8776

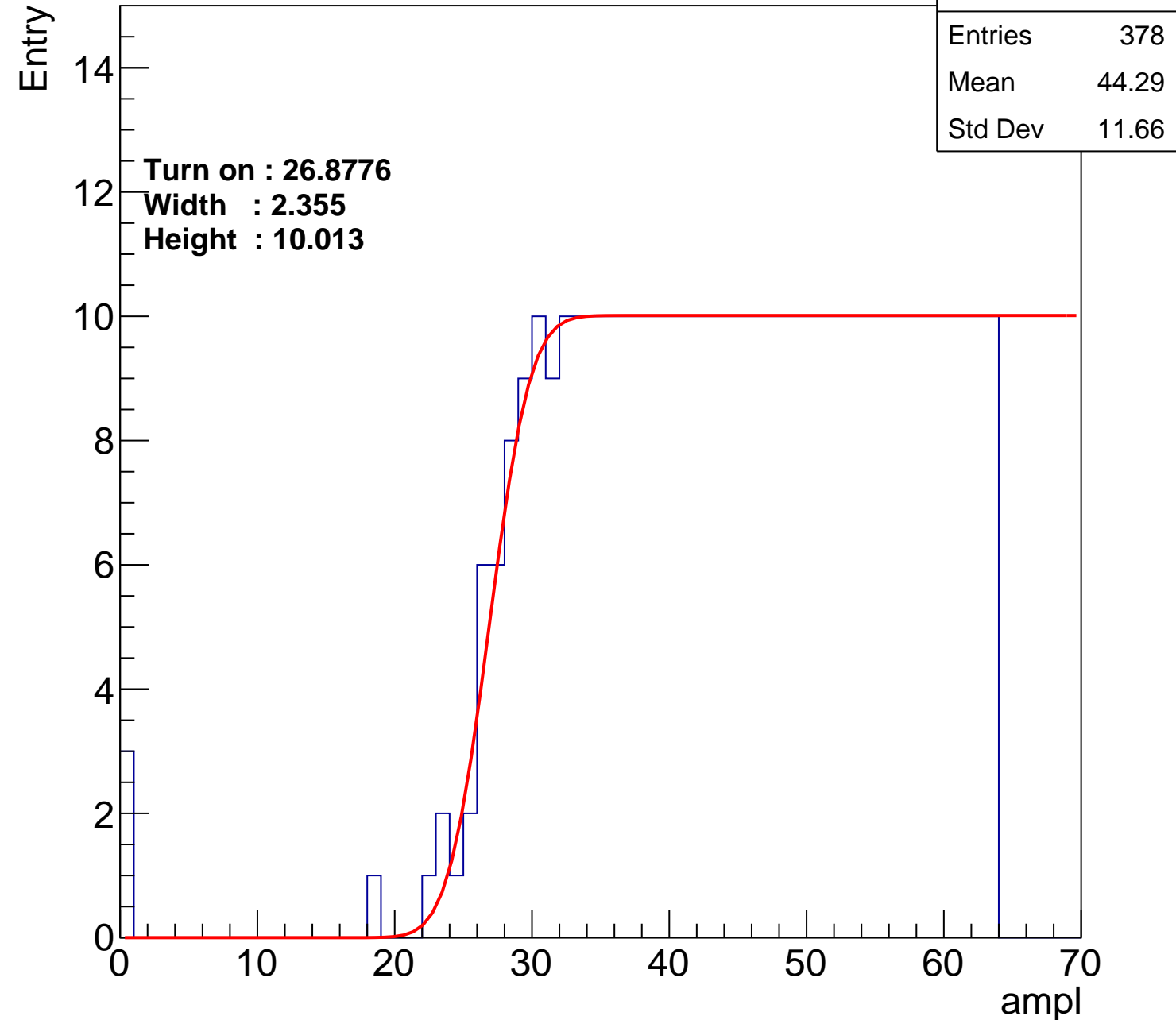
Width : 2.355

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch22

calib_packv5_042523_0143.root, FC#8, port C1

Entries	355
Mean	45.58
Std Dev	10.64

Turn on : 28.6361

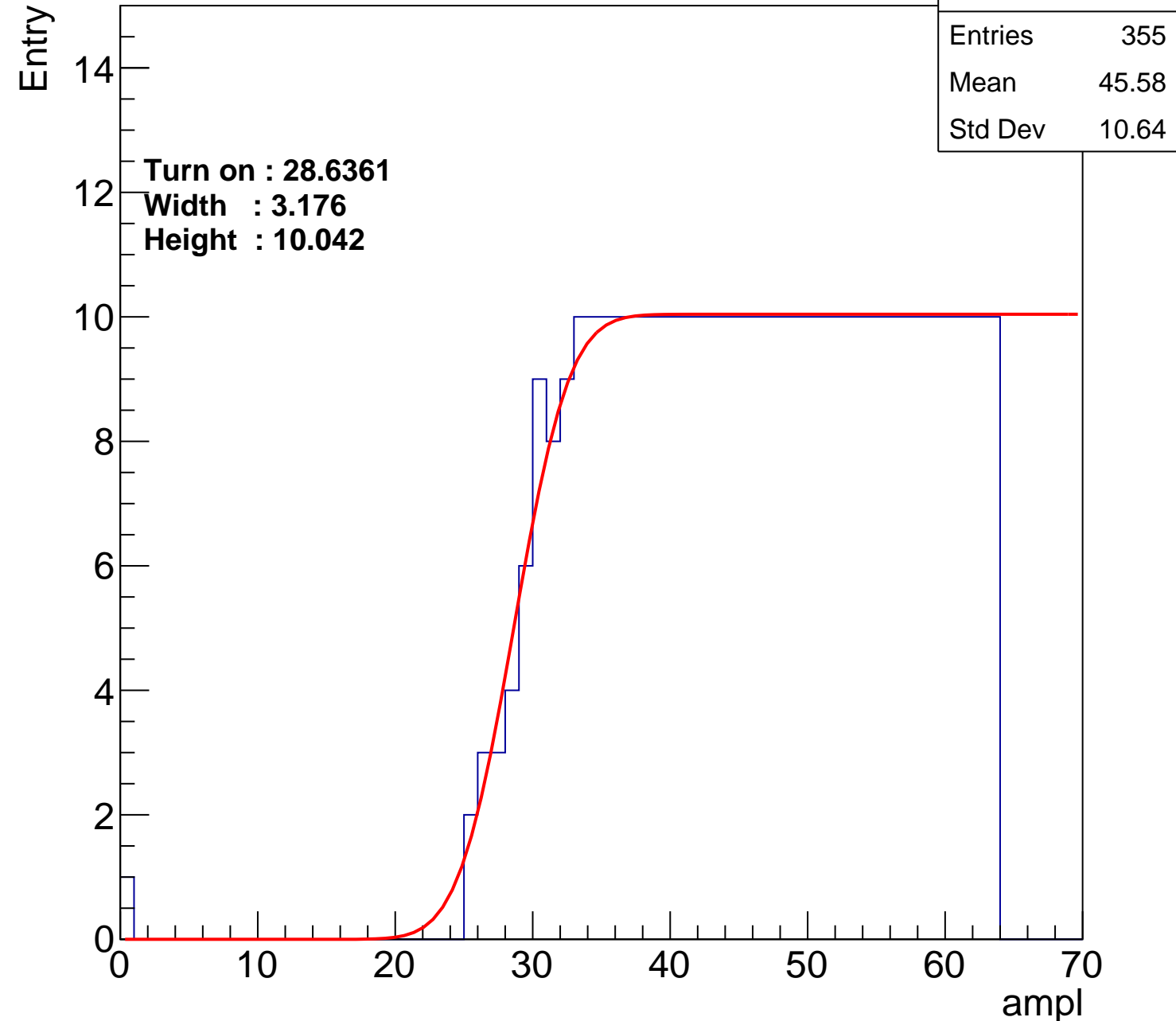
Width : 3.176

Height : 10.042

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch23

calib_packv5_042523_0143.root, FC#8, port C1

Entries	367
Mean	44.77
Std Dev	11.57

Turn on : 27.9836

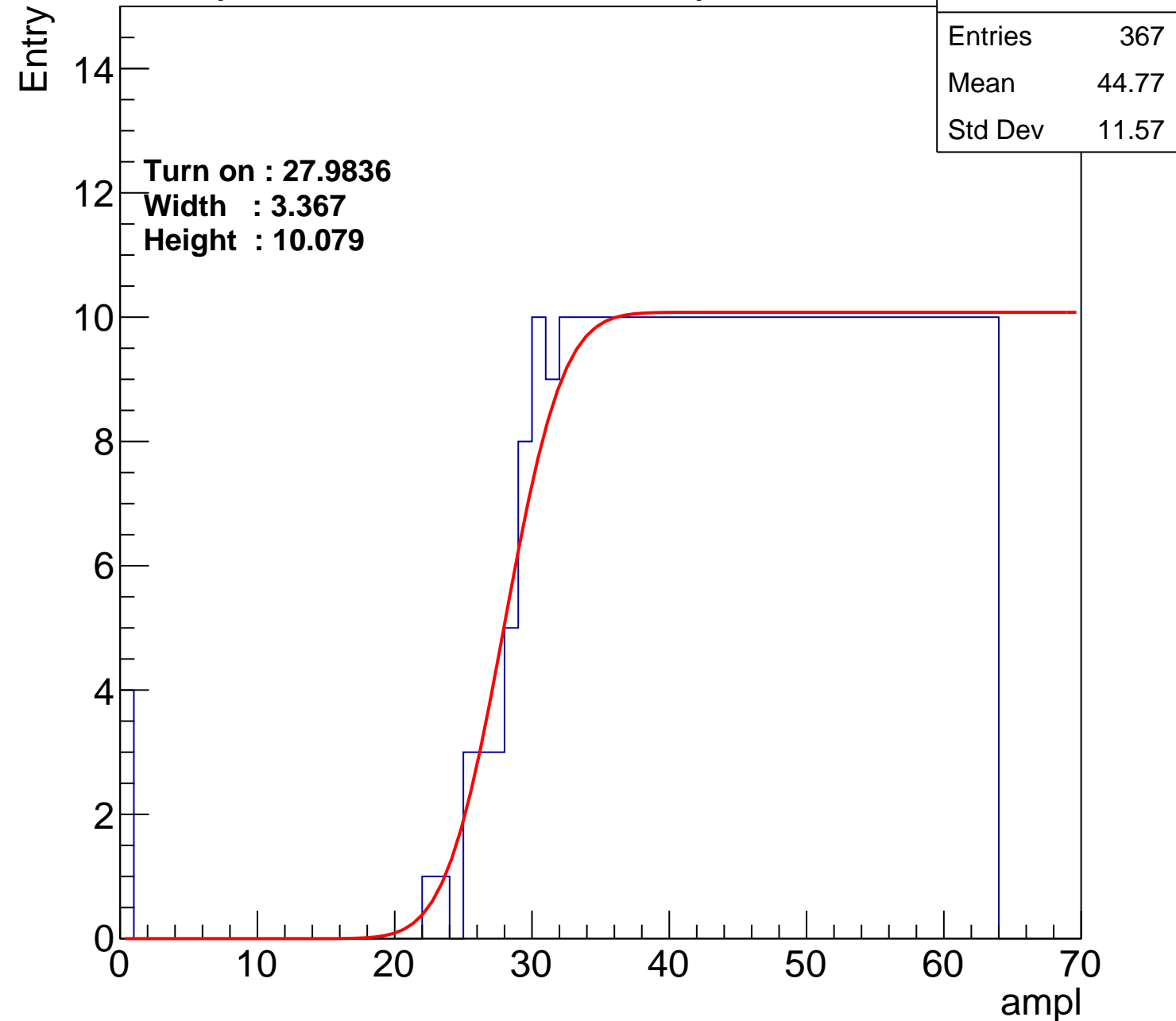
Width : 3.367

Height : 10.079

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch24

calib_packv5_042523_0143.root, FC#8, port C1

Entries	368
Mean	44.99
Std Dev	10.9

Turn on : 27.0399

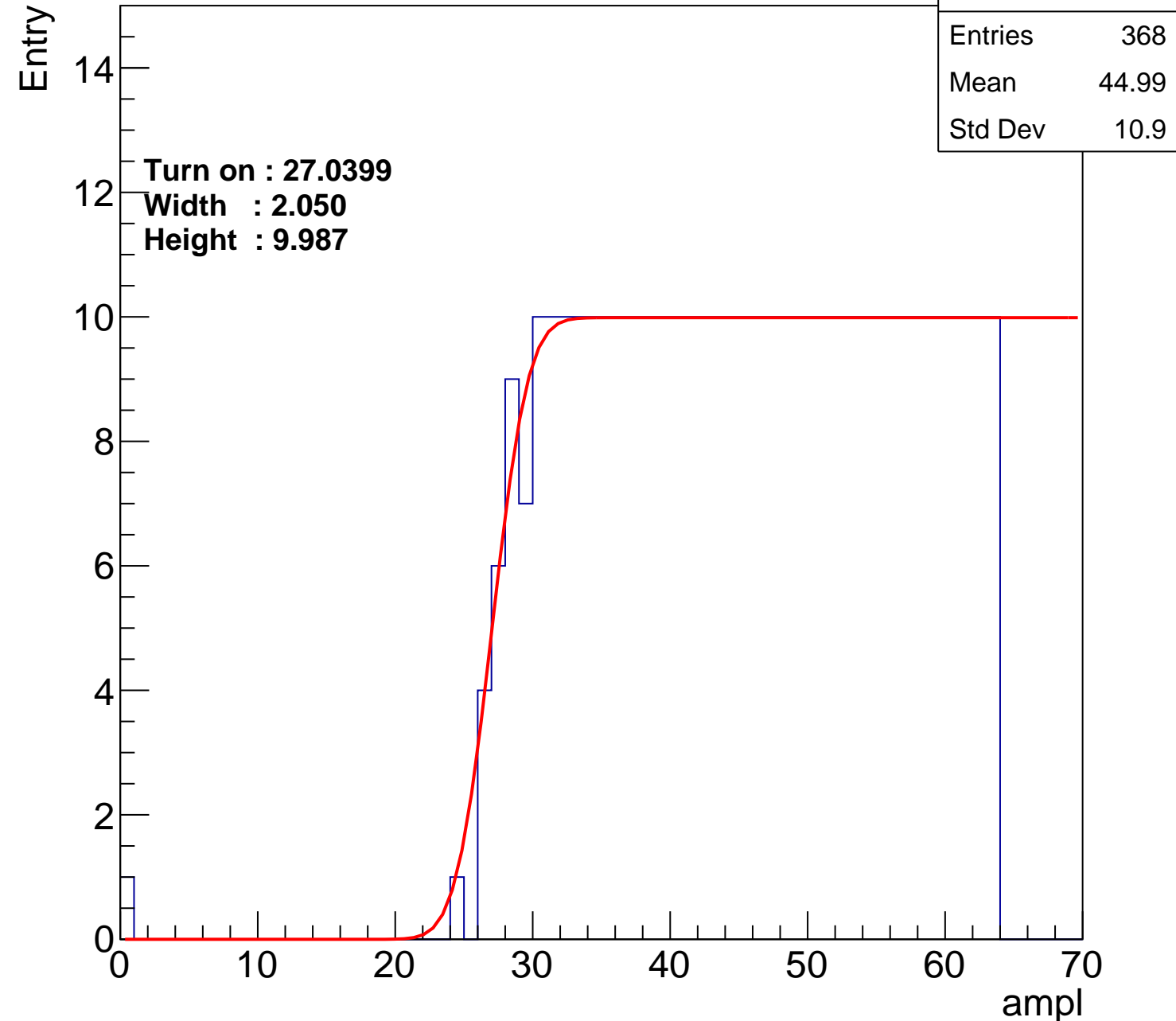
Width : 2.050

Height : 9.987

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch25

calib_packv5_042523_0143.root, FC#8, port C1

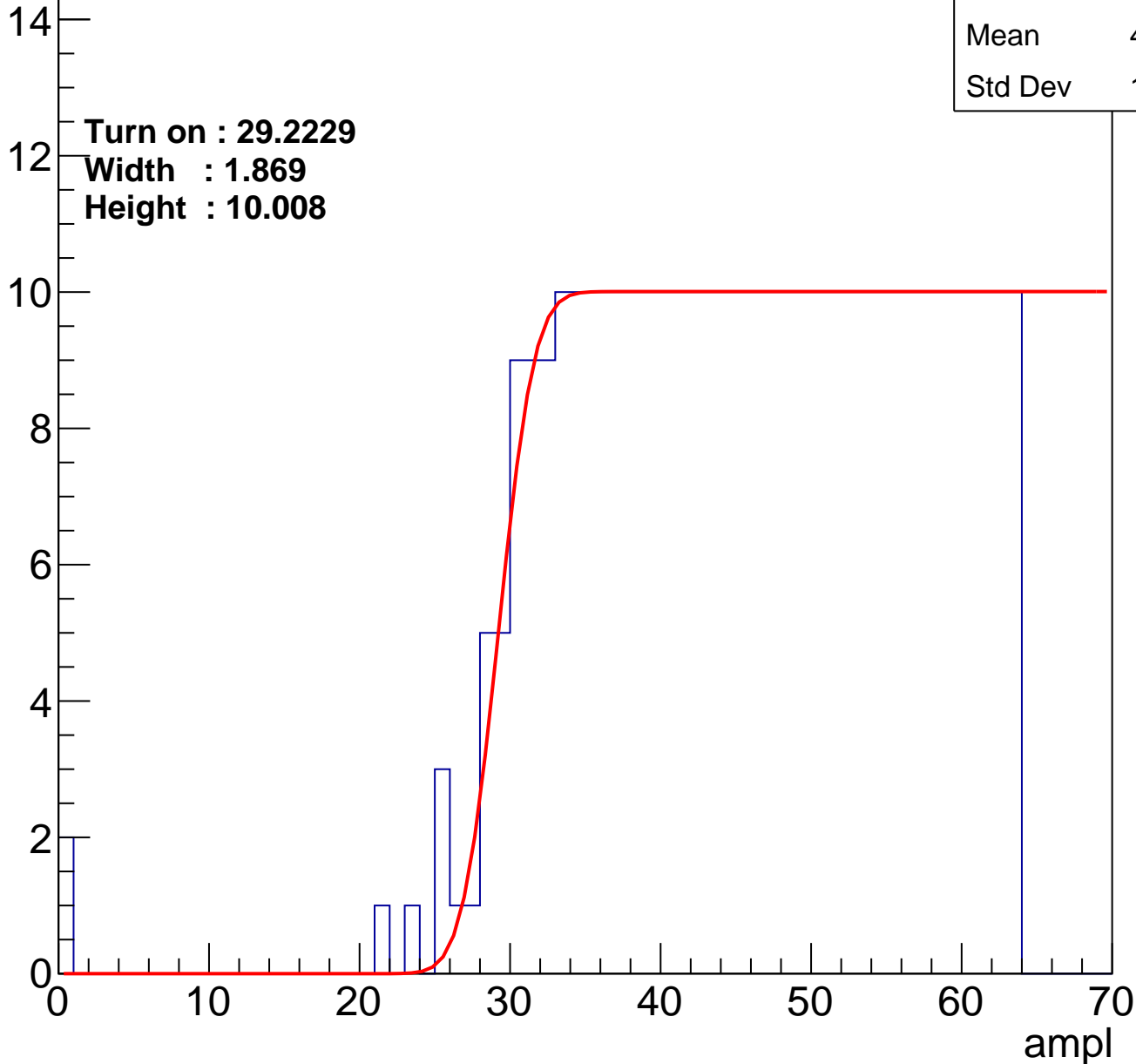
Entries	356
Mean	45.43
Std Dev	10.93

Turn on : 29.2229

Width : 1.869

Height : 10.008

Entry



B0L002S, U7-ch26

calib_packv5_042523_0143.root, FC#8, port C1

Entries	362
Mean	45.13
Std Dev	11.09

Turn on : 28.0759

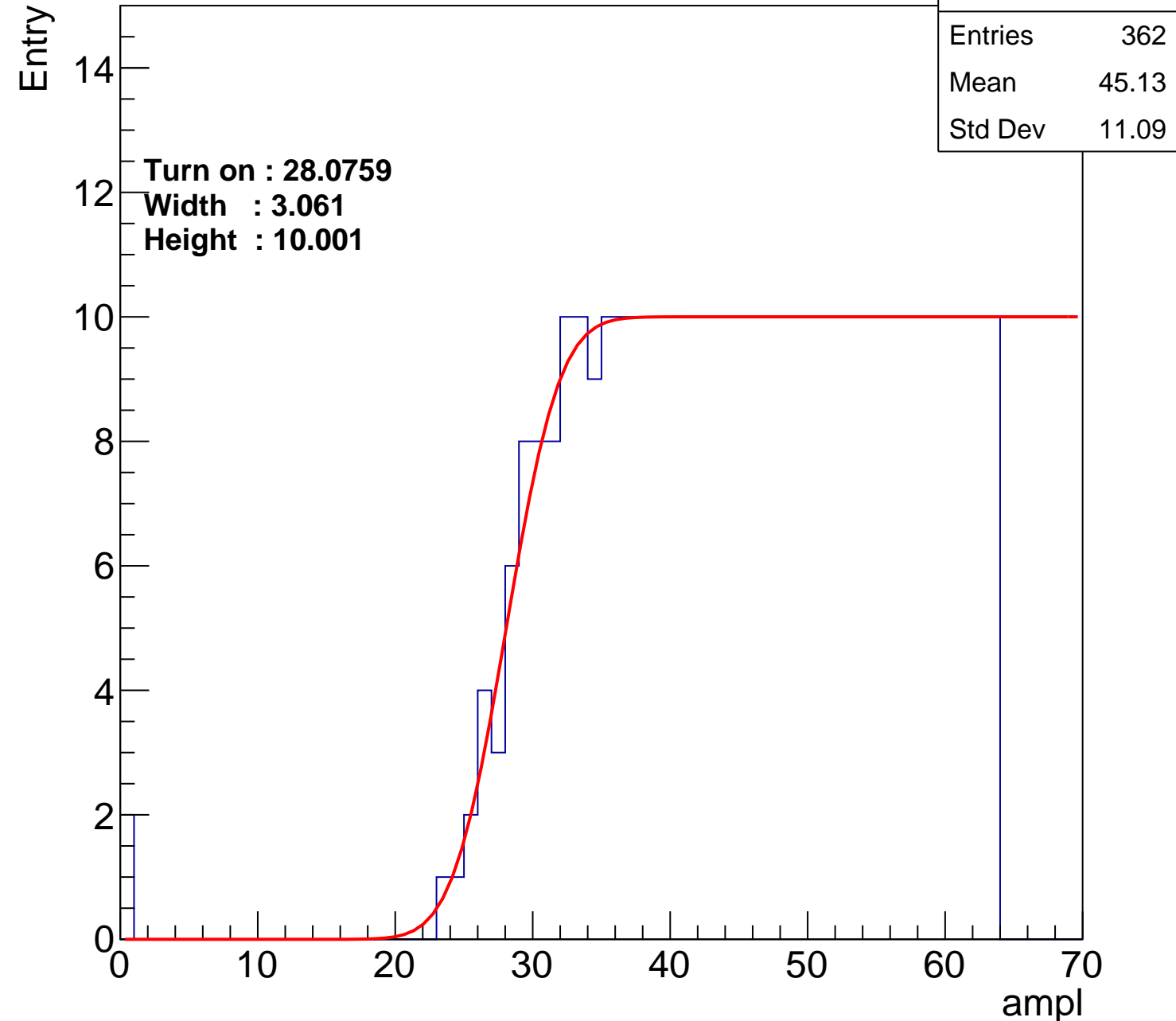
Width : 3.061

Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch27

calib_packv5_042523_0143.root, FC#8, port C1

Entries	361
Mean	45.29
Std Dev	10.79

Turn on : 27.4665

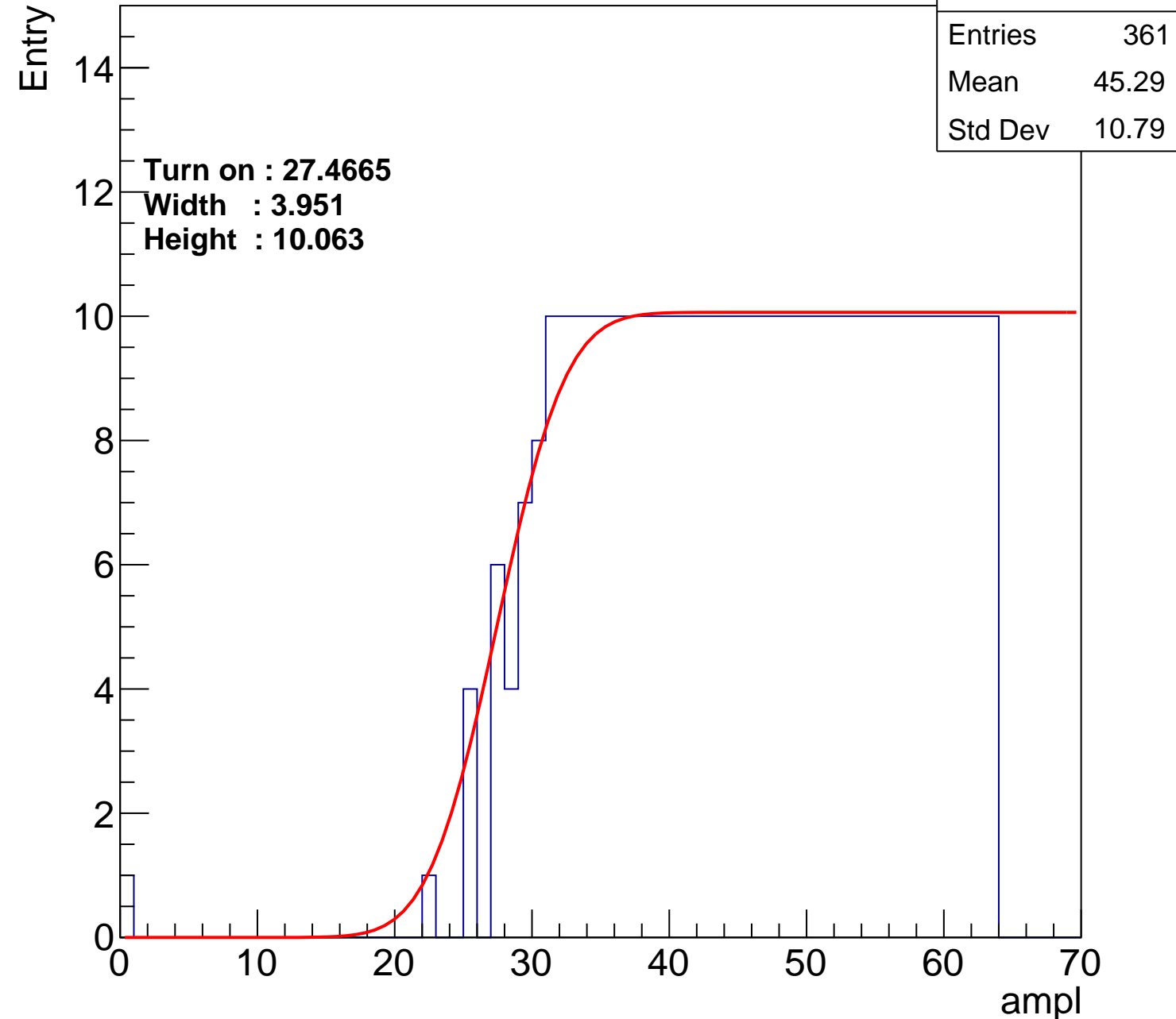
Width : 3.951

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch28

calib_packv5_042523_0143.root, FC#8, port C1

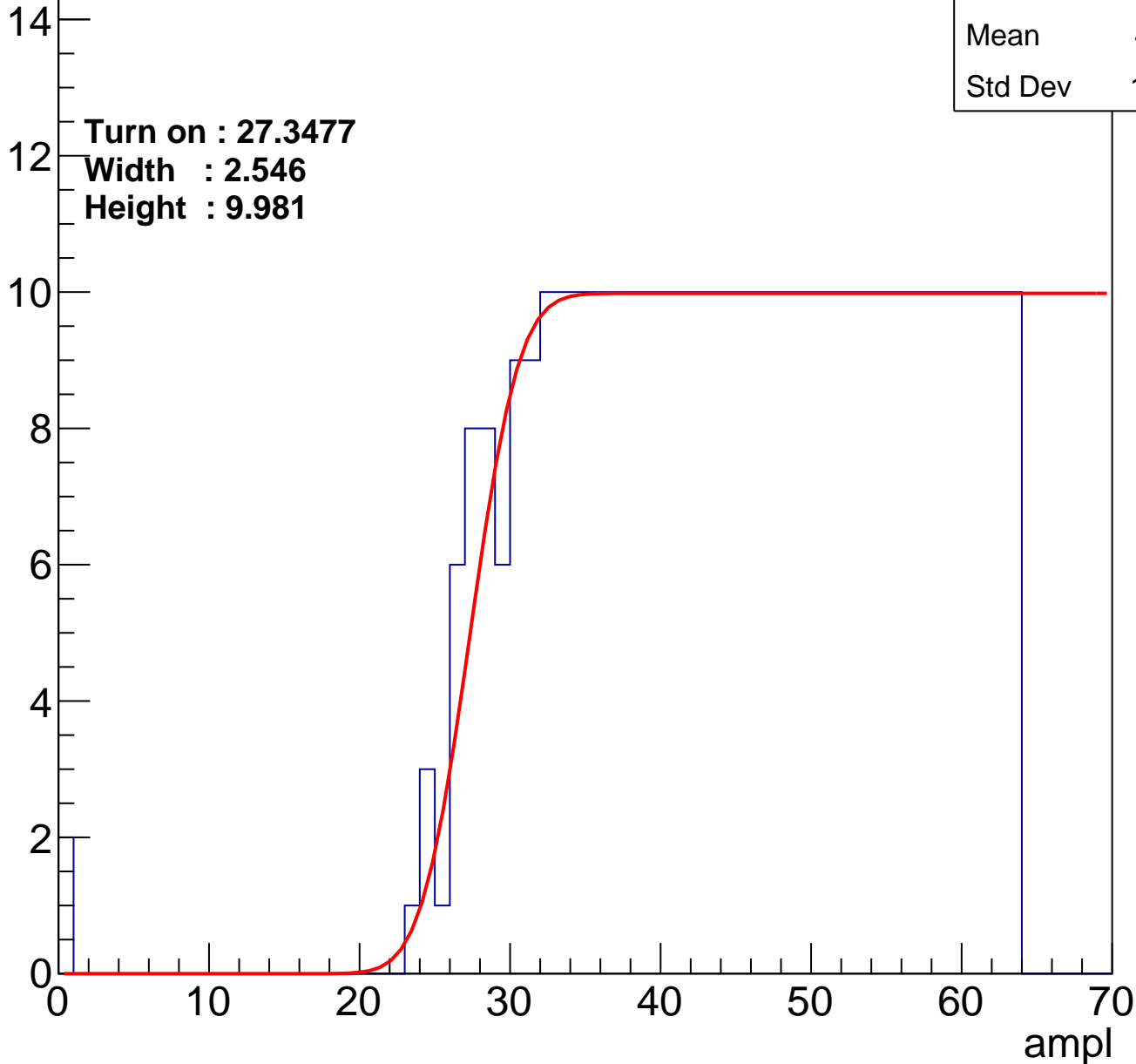
Entry

Entries	373
Mean	44.61
Std Dev	11.33

Turn on : 27.3477

Width : 2.546

Height : 9.981



B0L002S, U7-ch29

calib_packv5_042523_0143.root, FC#8, port C1

Entries	352
Mean	45.64
Std Dev	10.81

Turn on : 28.9251

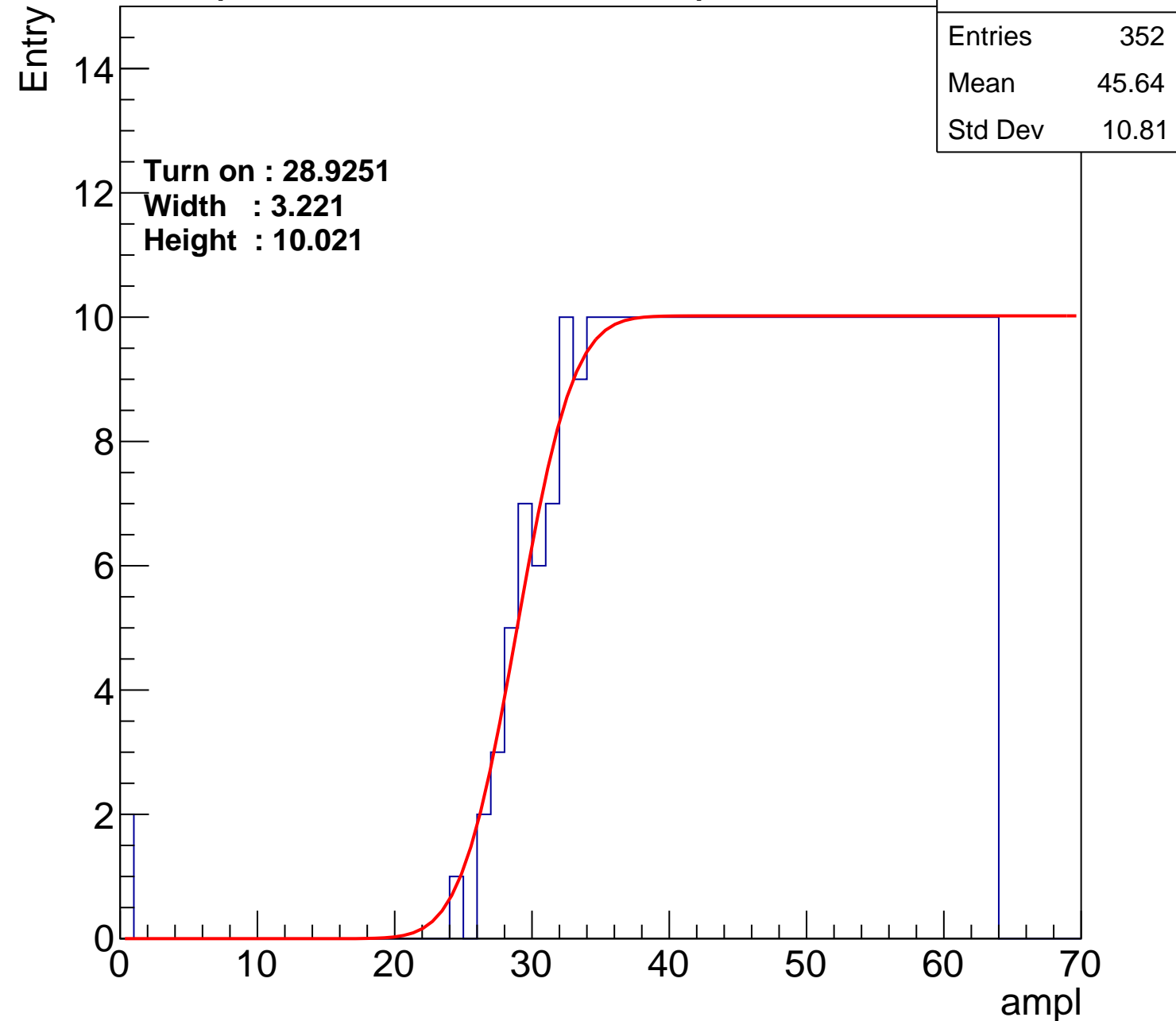
Width : 3.221

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch30

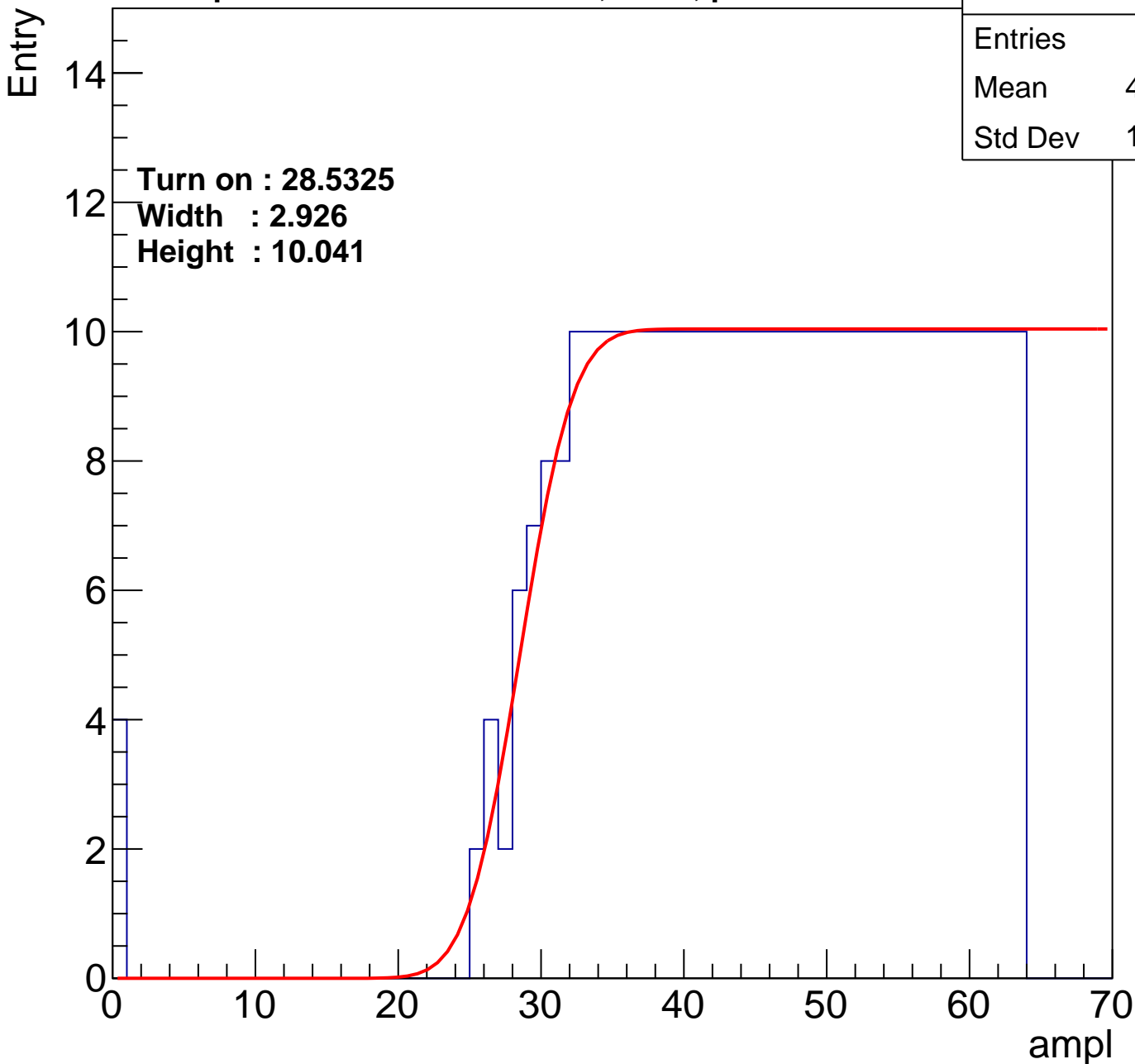
calib_packv5_042523_0143.root, FC#8, port C1

Entries	361
Mean	45.06
Std Dev	11.43

Turn on : 28.5325

Width : 2.926

Height : 10.041



B0L002S, U7-ch31

calib_packv5_042523_0143.root, FC#8, port C1

Entries	367
Mean	44.8
Std Dev	11.44

Turn on : 27.9452

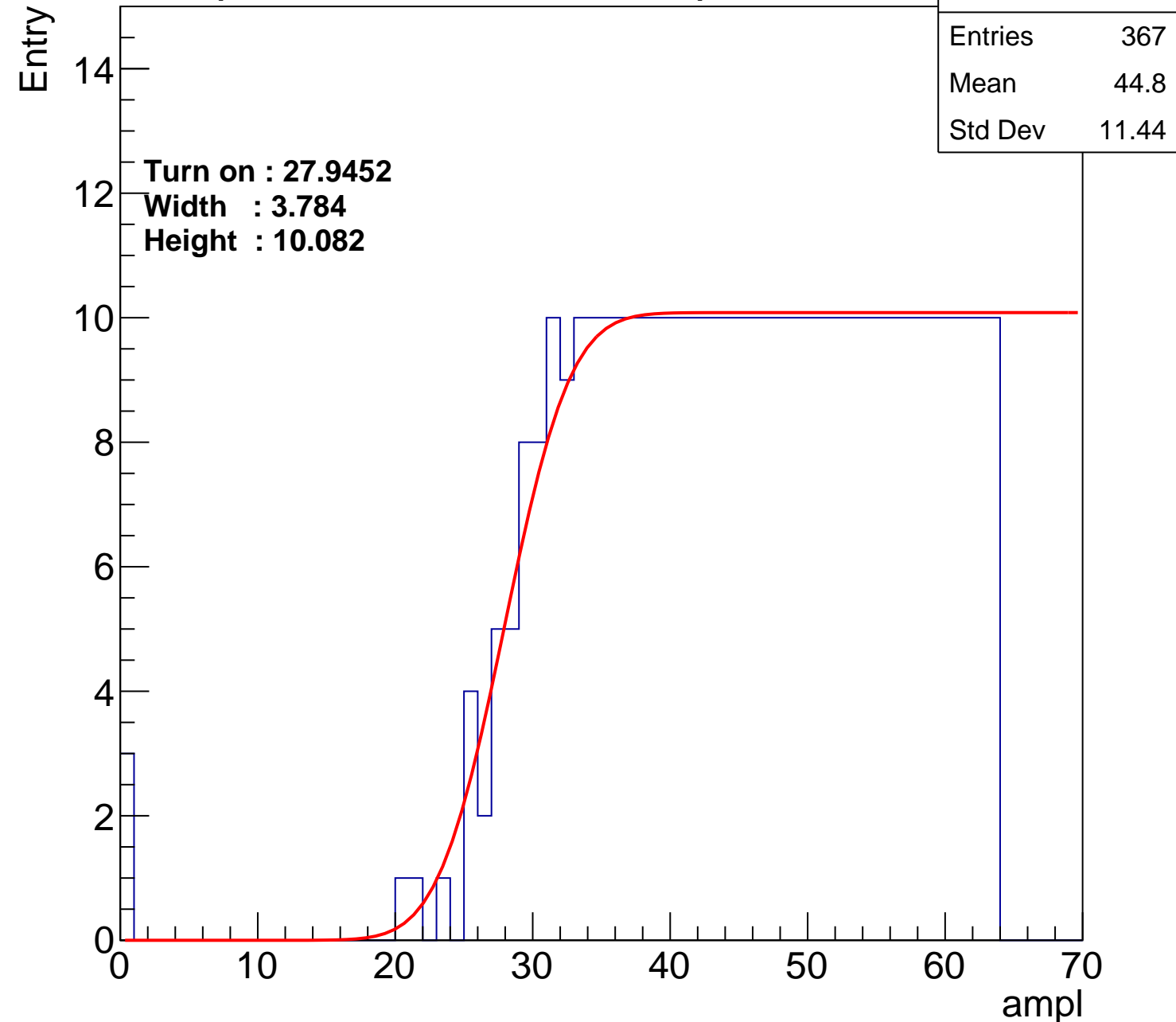
Width : 3.784

Height : 10.082

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch32

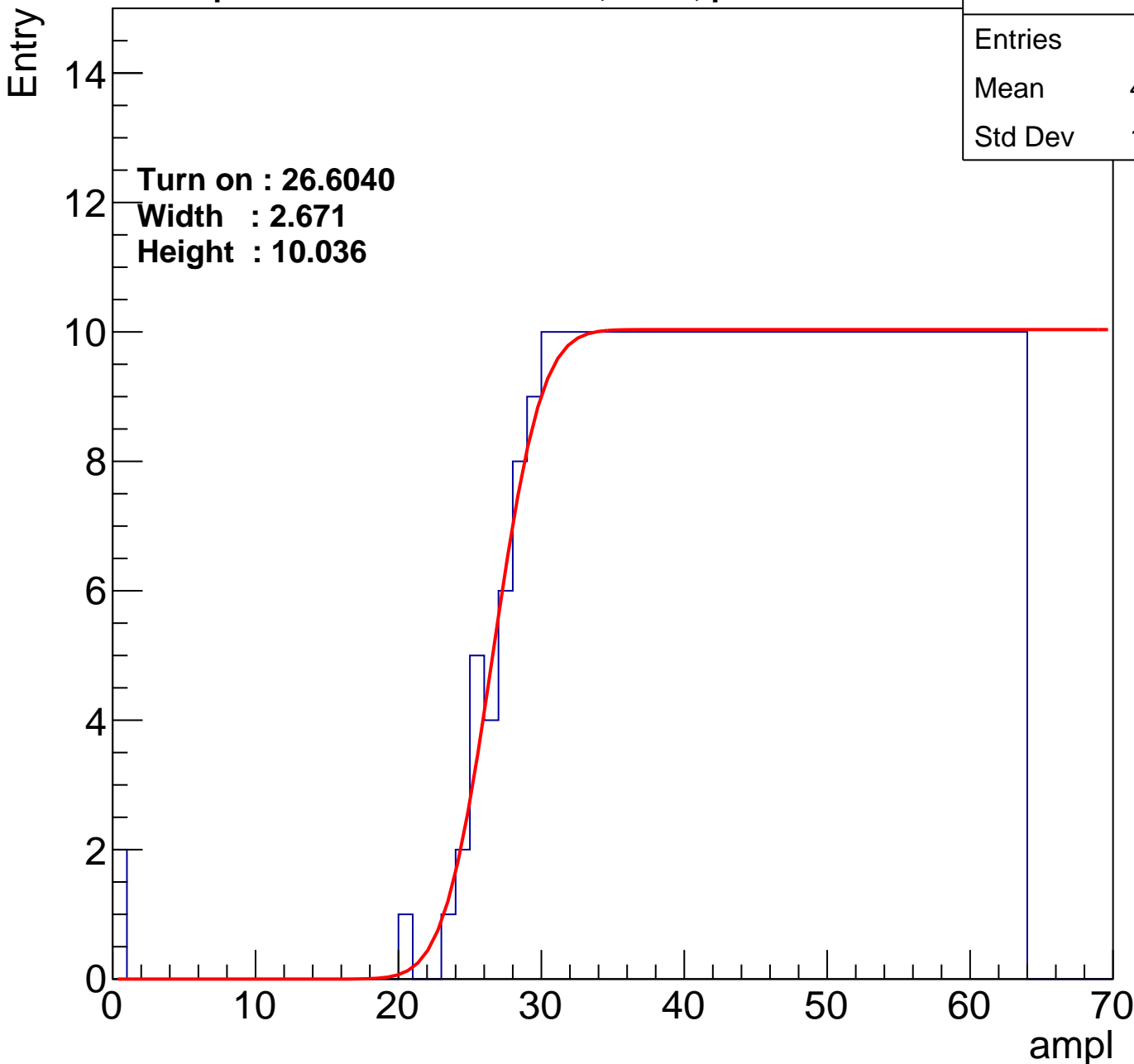
calib_packv5_042523_0143.root, FC#8, port C1

Entries	378
Mean	44.38
Std Dev	11.43

Turn on : 26.6040

Width : 2.671

Height : 10.036



B0L002S, U7-ch33

calib_packv5_042523_0143.root, FC#8, port C1

Entries	384
Mean	44.01
Std Dev	11.77

Turn on : 25.7986

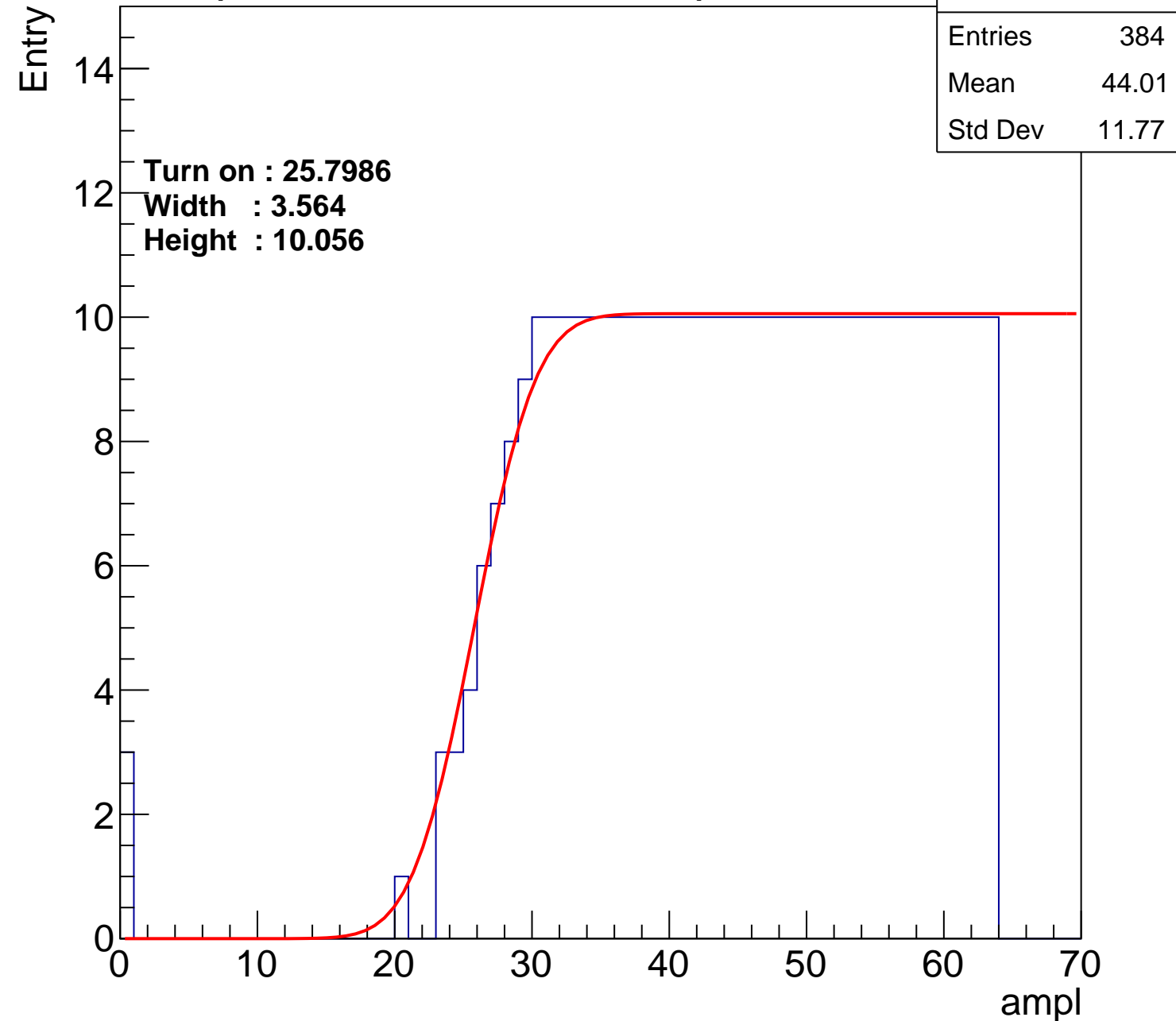
Width : 3.564

Height : 10.056

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch34

calib_packv5_042523_0143.root, FC#8, port C1

Entries	361
Mean	45.17
Std Dev	11.08

Turn on : 28.2435

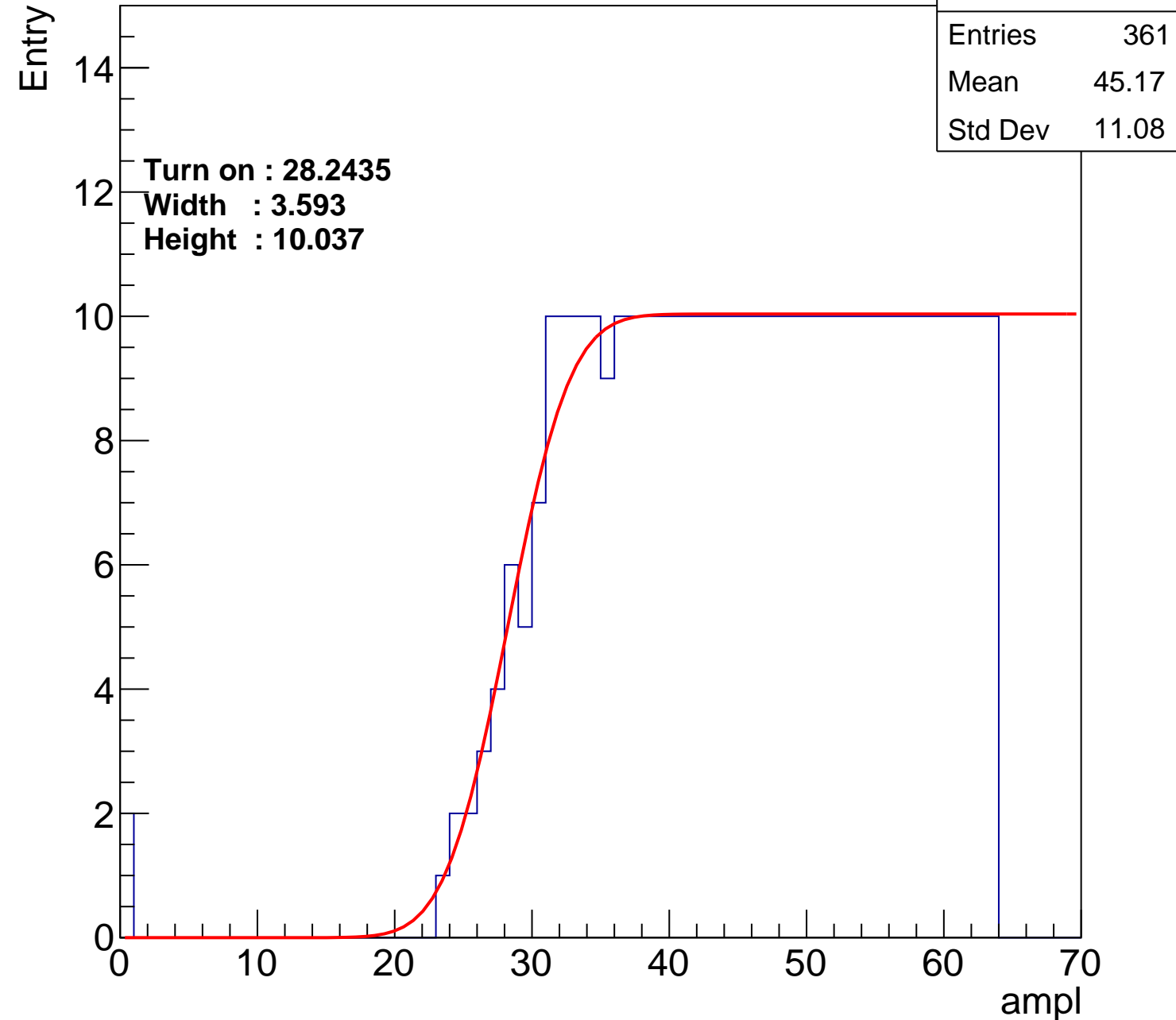
Width : 3.593

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch35

calib_packv5_042523_0143.root, FC#8, port C1

Entries	355
Mean	45.6
Std Dev	10.61

Turn on : 28.5995

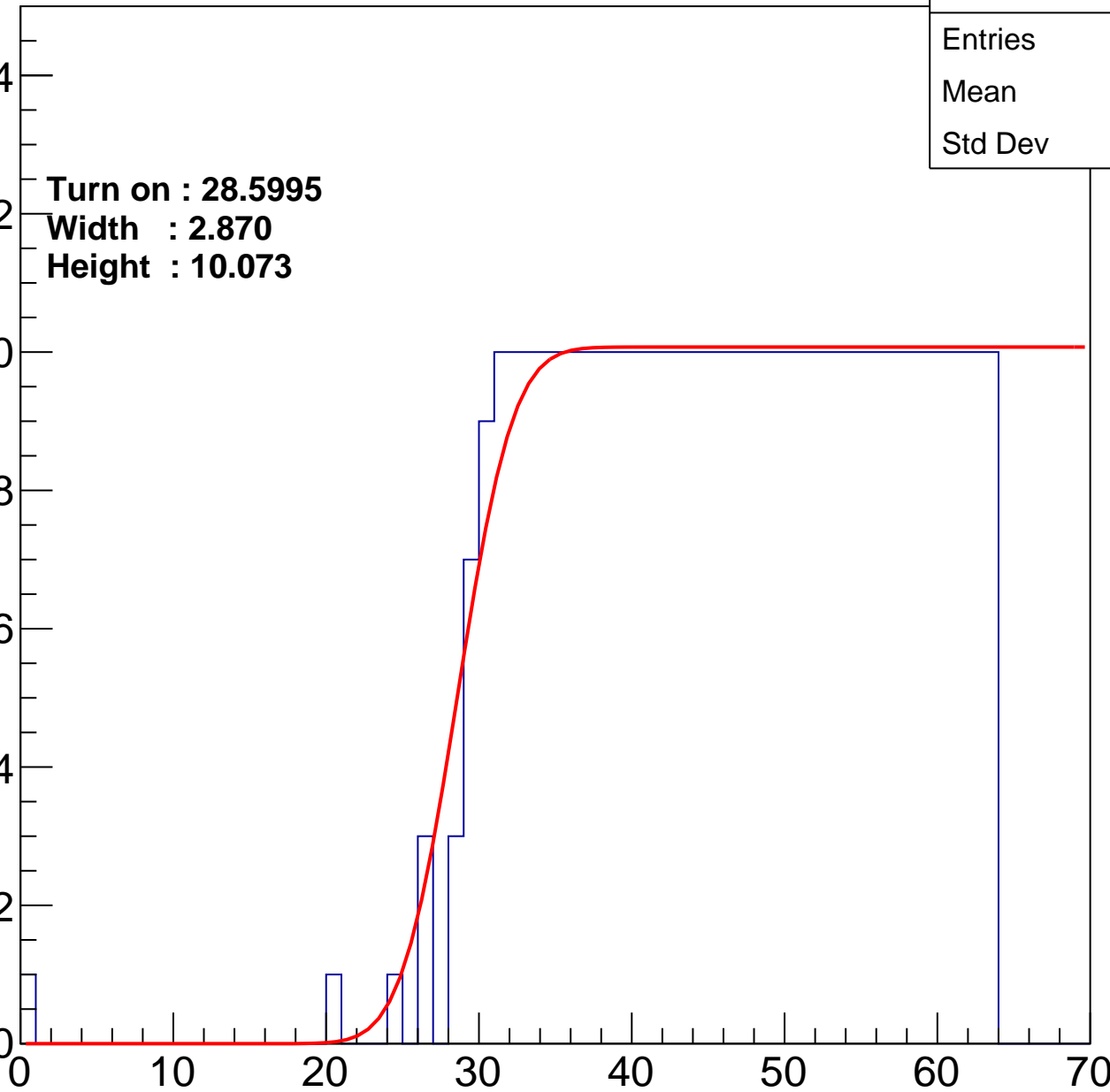
Width : 2.870

Height : 10.073

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch36

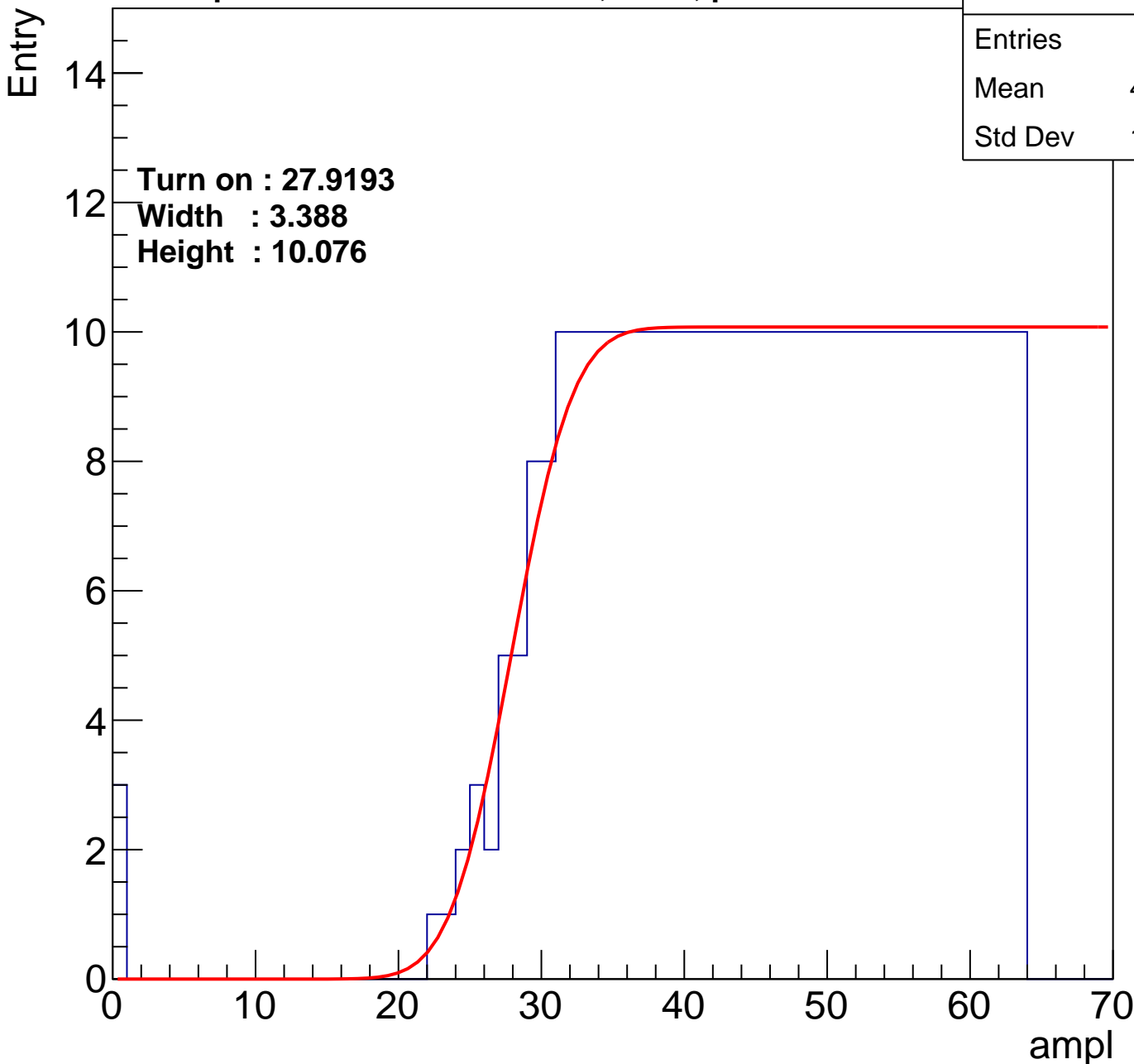
calib_packv5_042523_0143.root, FC#8, port C1

Entries	368
Mean	44.77
Std Dev	11.42

Turn on : 27.9193

Width : 3.388

Height : 10.076



B0L002S, U7-ch37

calib_packv5_042523_0143.root, FC#8, port C1

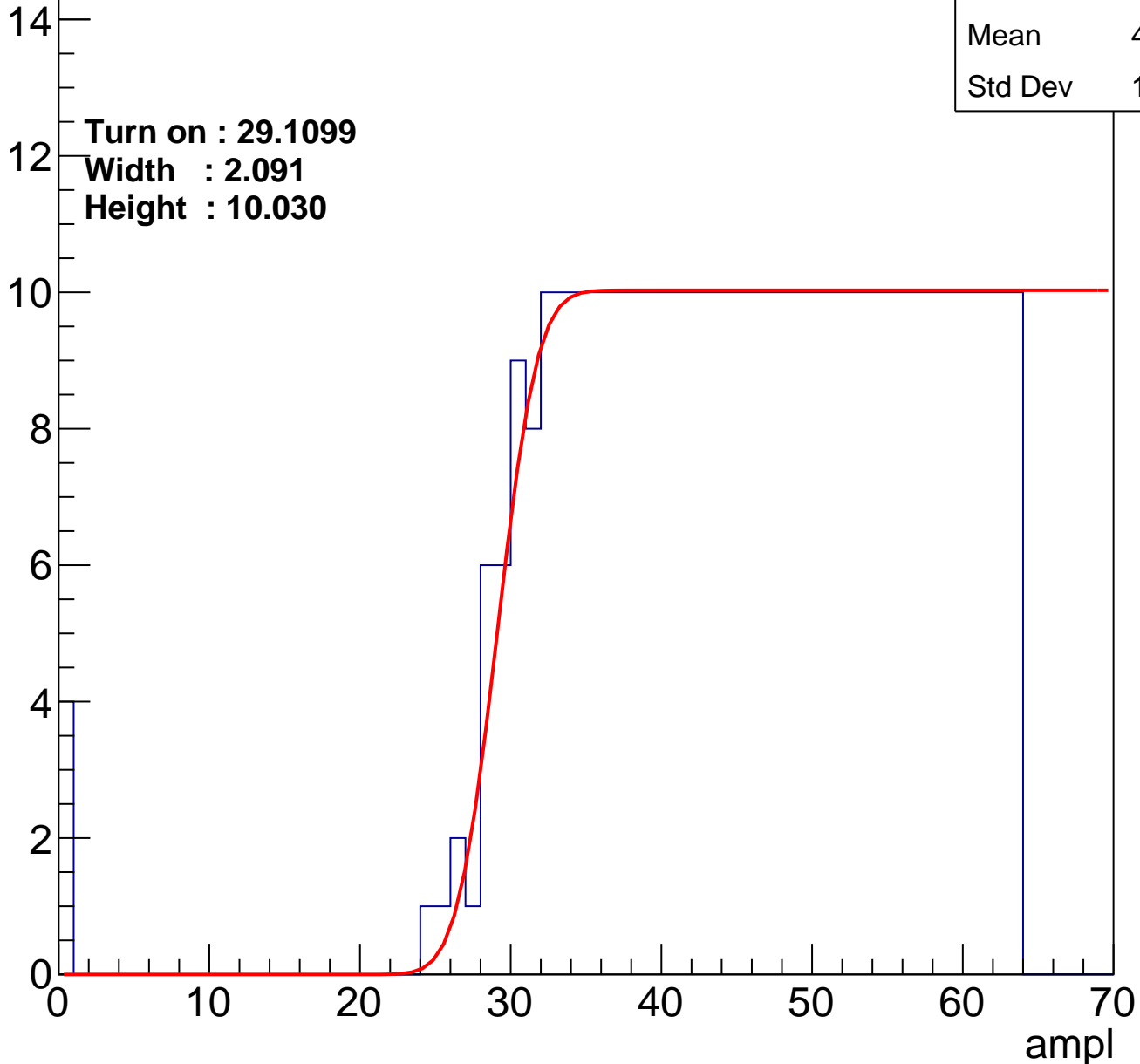
Entries	358
Mean	45.22
Std Dev	11.35

Turn on : 29.1099

Width : 2.091

Height : 10.030

Entry



B0L002S, U7-ch38

calib_packv5_042523_0143.root, FC#8, port C1

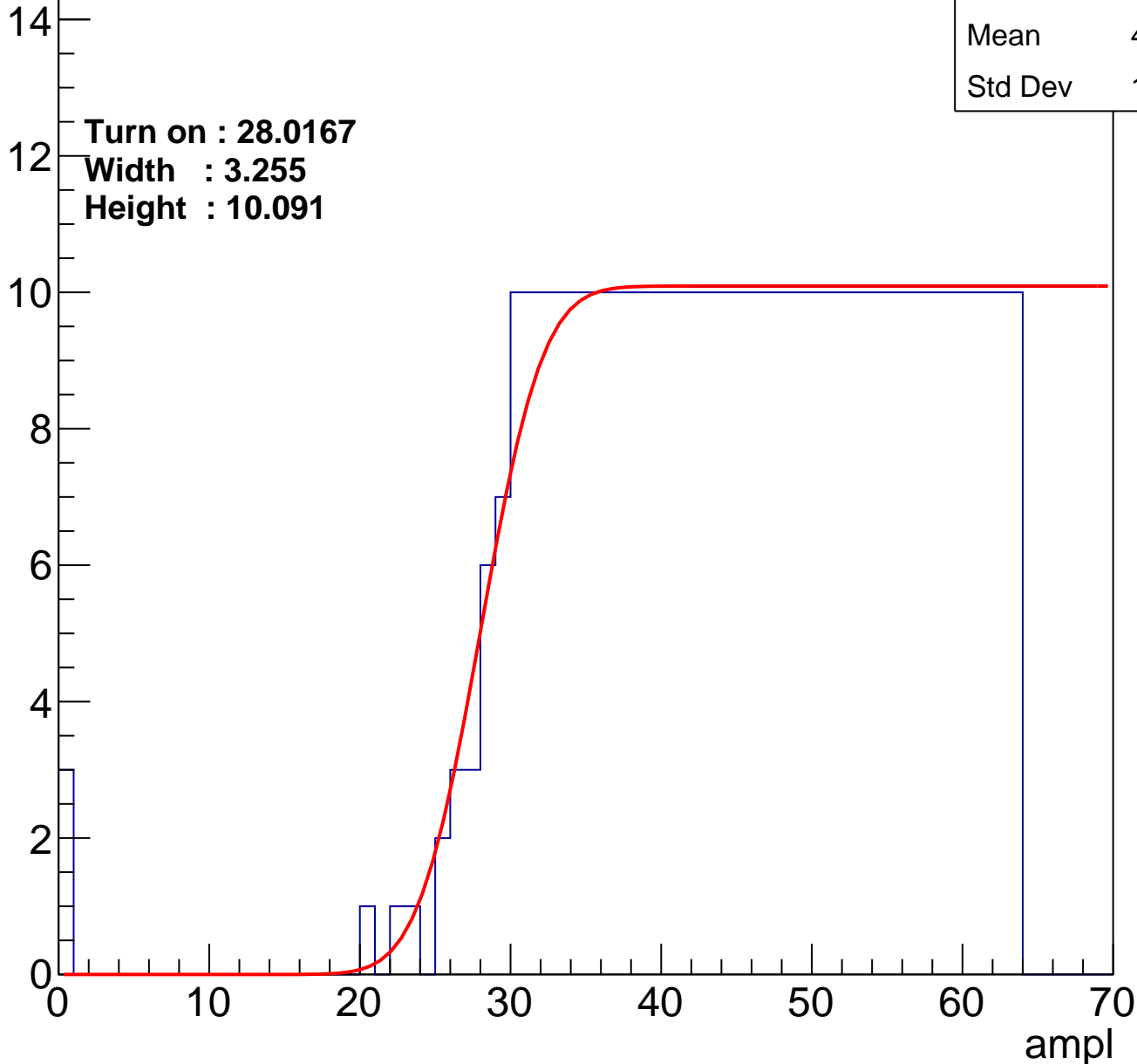
Entry

Entries	367
Mean	44.84
Std Dev	11.39

Turn on : 28.0167

Width : 3.255

Height : 10.091



B0L002S, U7-ch39

calib_packv5_042523_0143.root, FC#8, port C1

Entries	374
Mean	44.52
Std Dev	11.42

Turn on : 27.3498

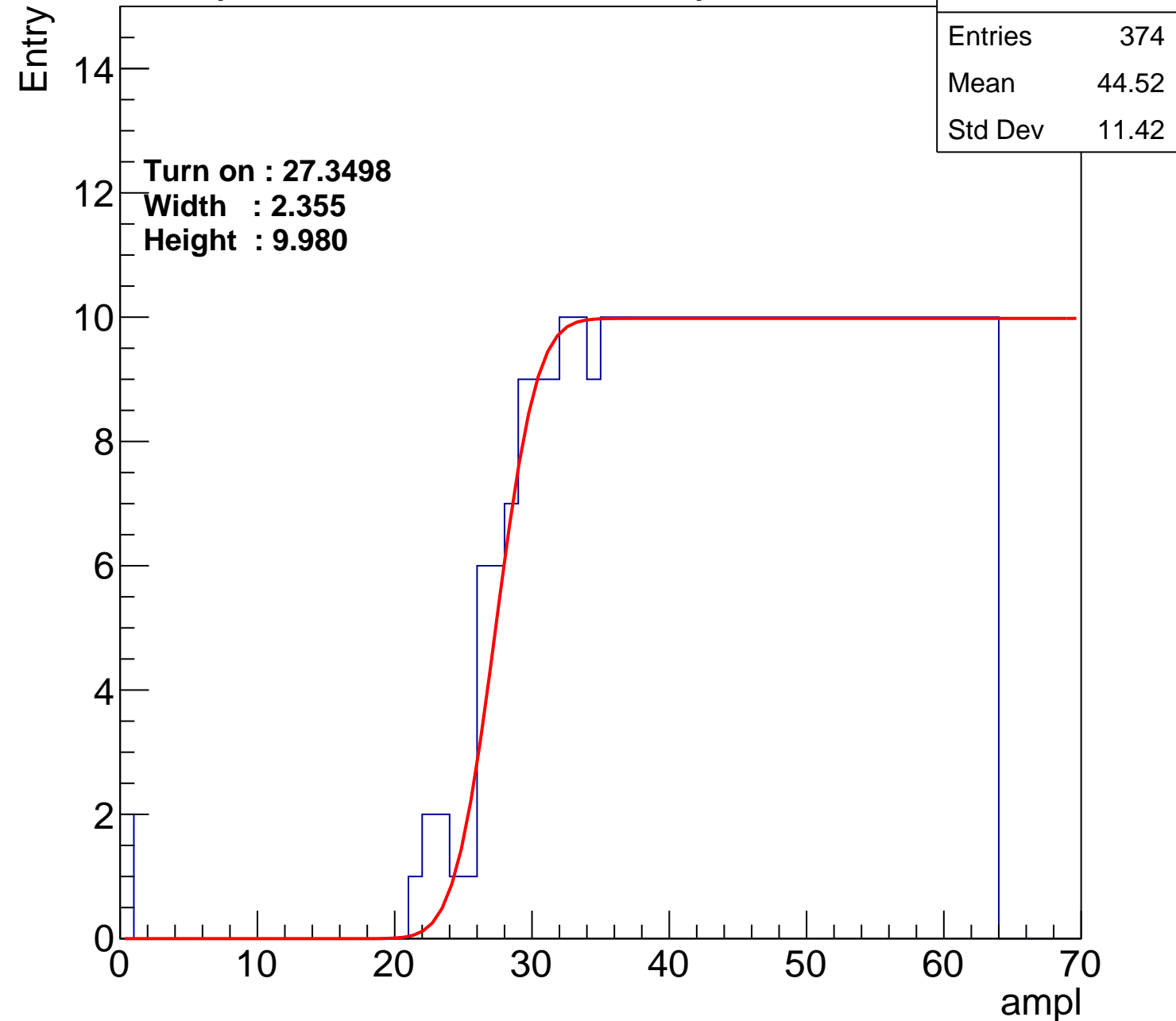
Width : 2.355

Height : 9.980

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch40

calib_packv5_042523_0143.root, FC#8, port C1

Entries	376
Mean	44.47
Std Dev	11.4

Turn on : 25.1591

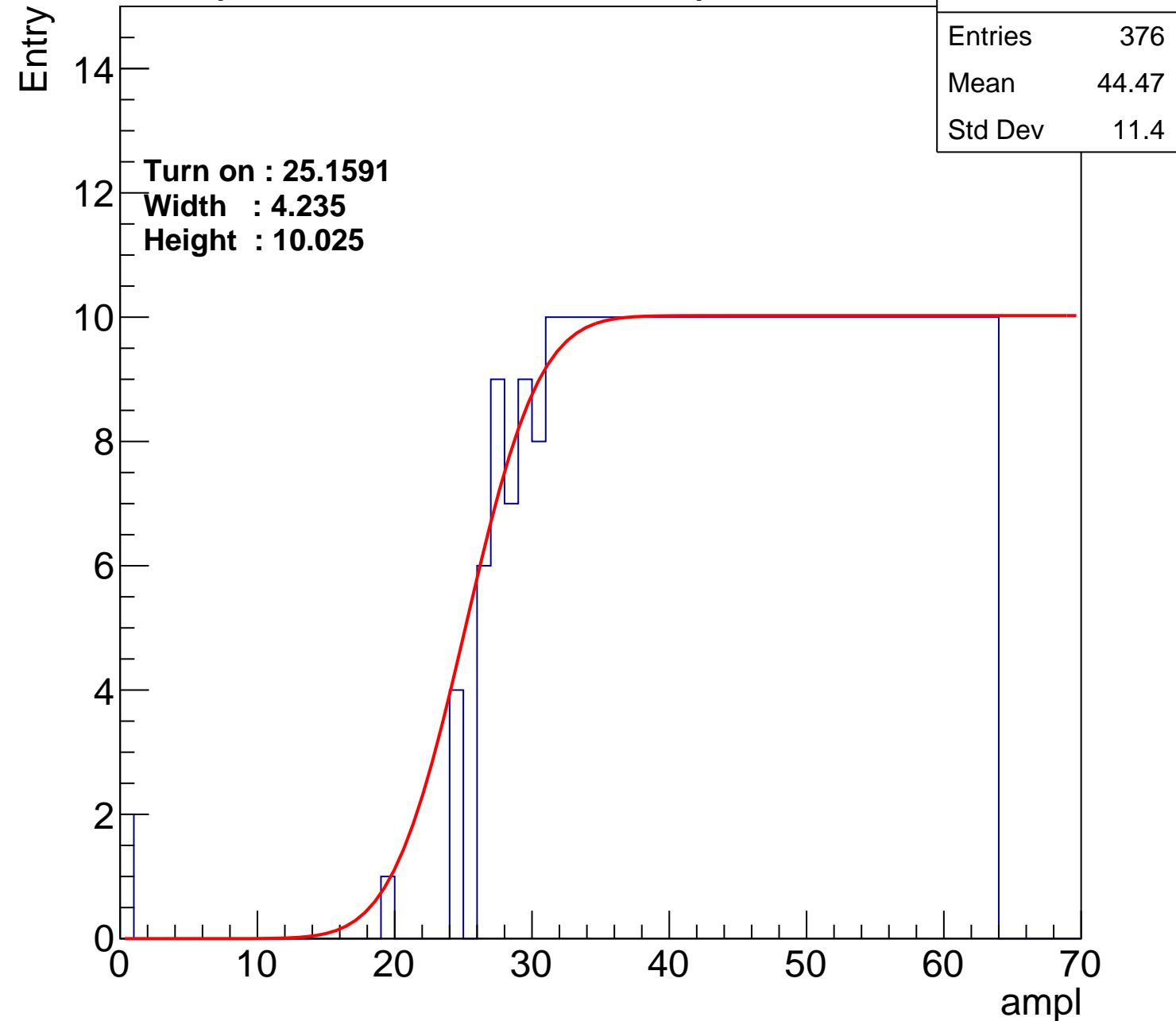
Width : 4.235

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch41

calib_packv5_042523_0143.root, FC#8, port C1

Entries	360
Mean	45.35
Std Dev	10.74

Turn on : 28.2526

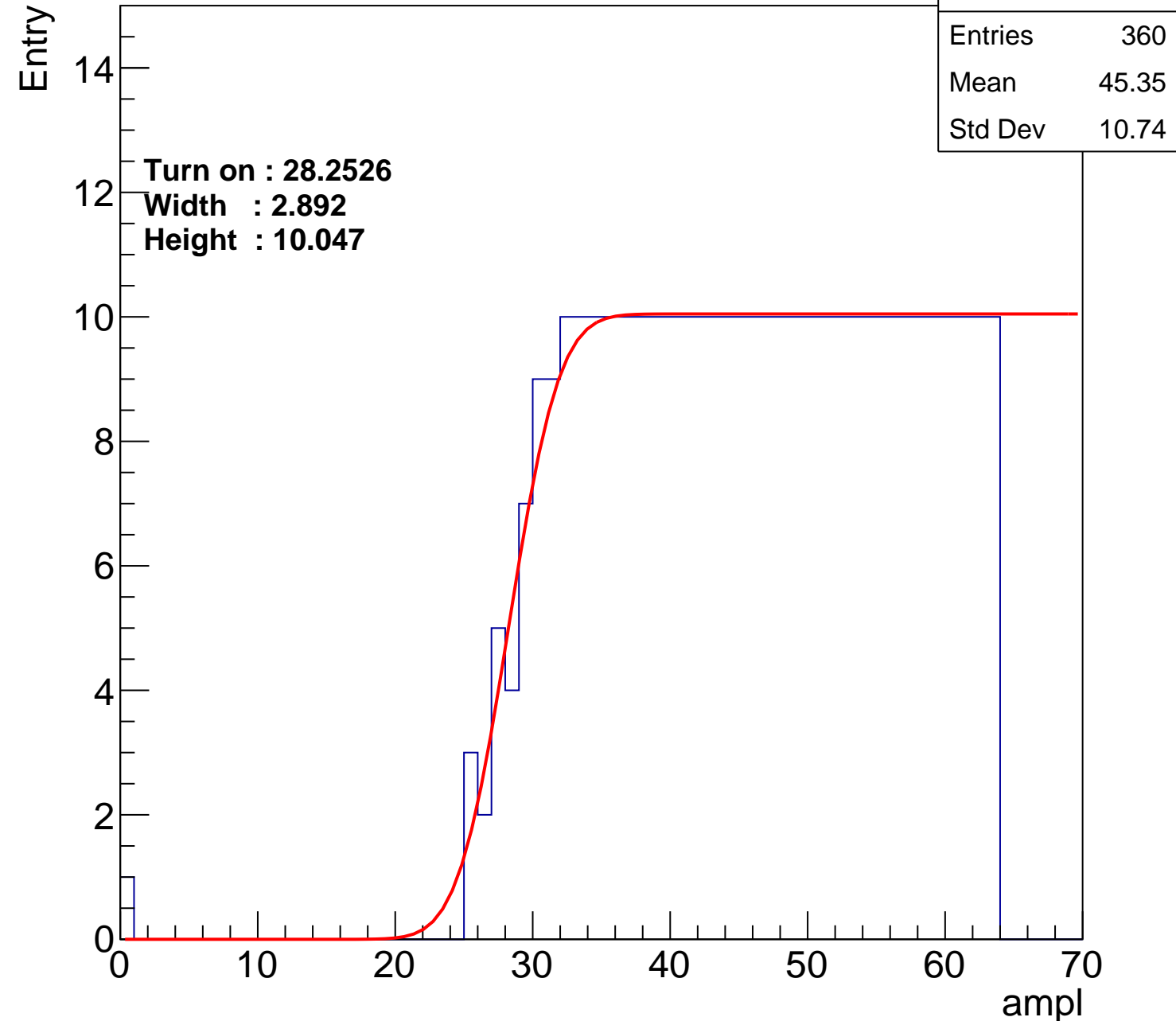
Width : 2.892

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch42

calib_packv5_042523_0143.root, FC#8, port C1

Entries	363
Mean	45.03
Std Dev	11.29

Turn on : 28.4057

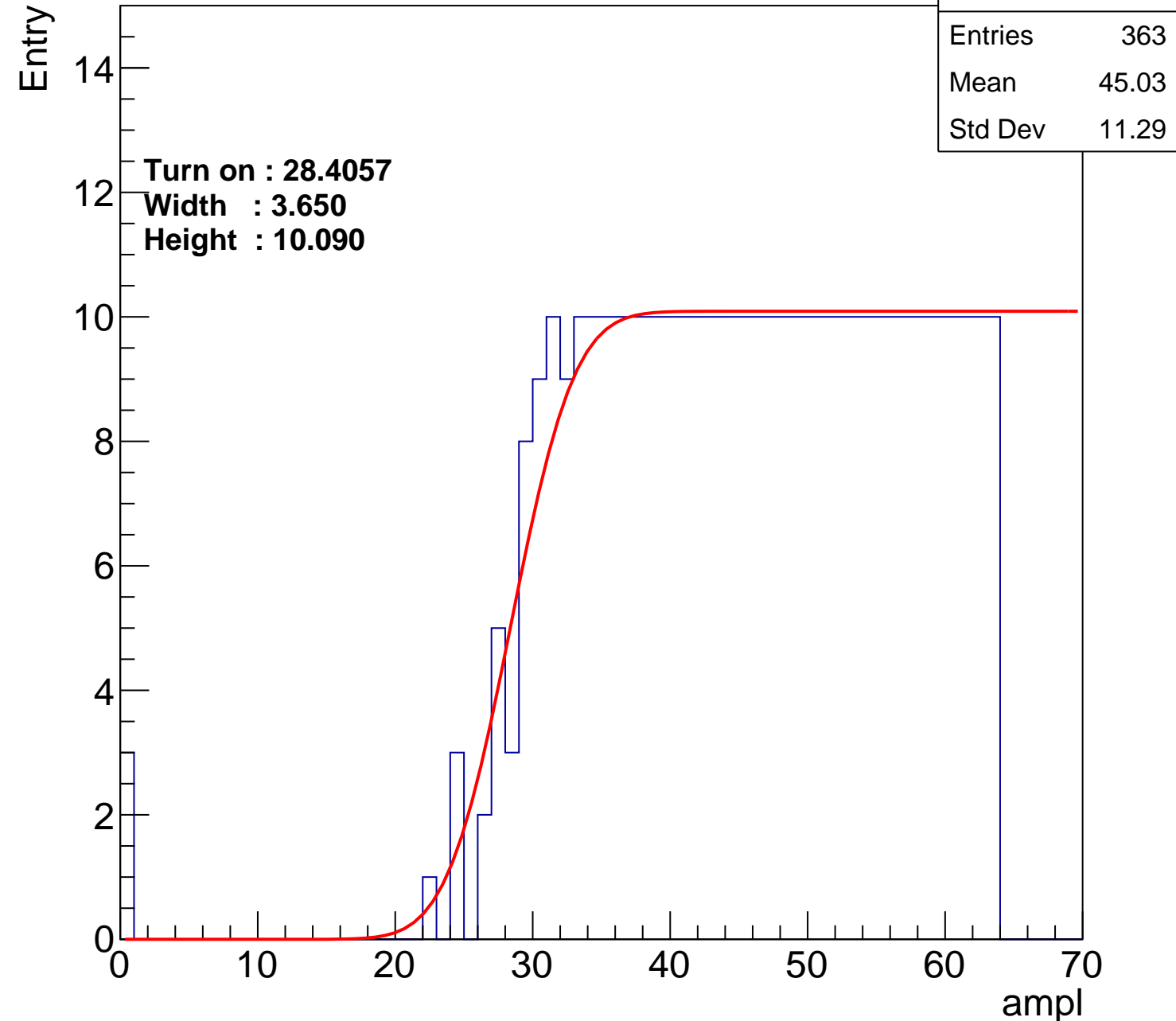
Width : 3.650

Height : 10.090

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch43

calib_packv5_042523_0143.root, FC#8, port C1

Entries	359
Mean	45.35
Std Dev	10.8

Turn on : 28.9128

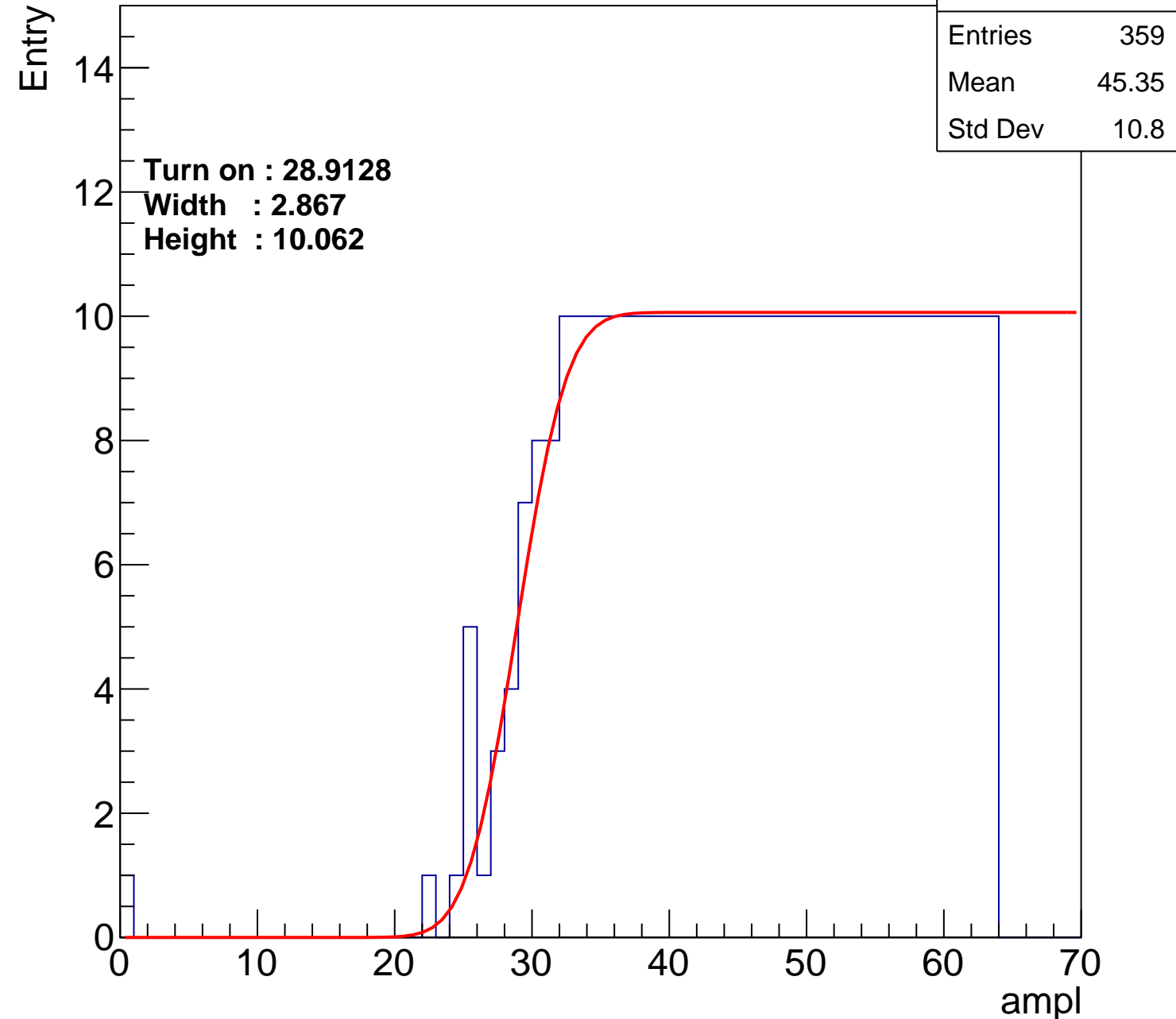
Width : 2.867

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch44

calib_packv5_042523_0143.root, FC#8, port C1

Entries	355
Mean	45.61
Std Dev	10.57

Turn on : 28.3649

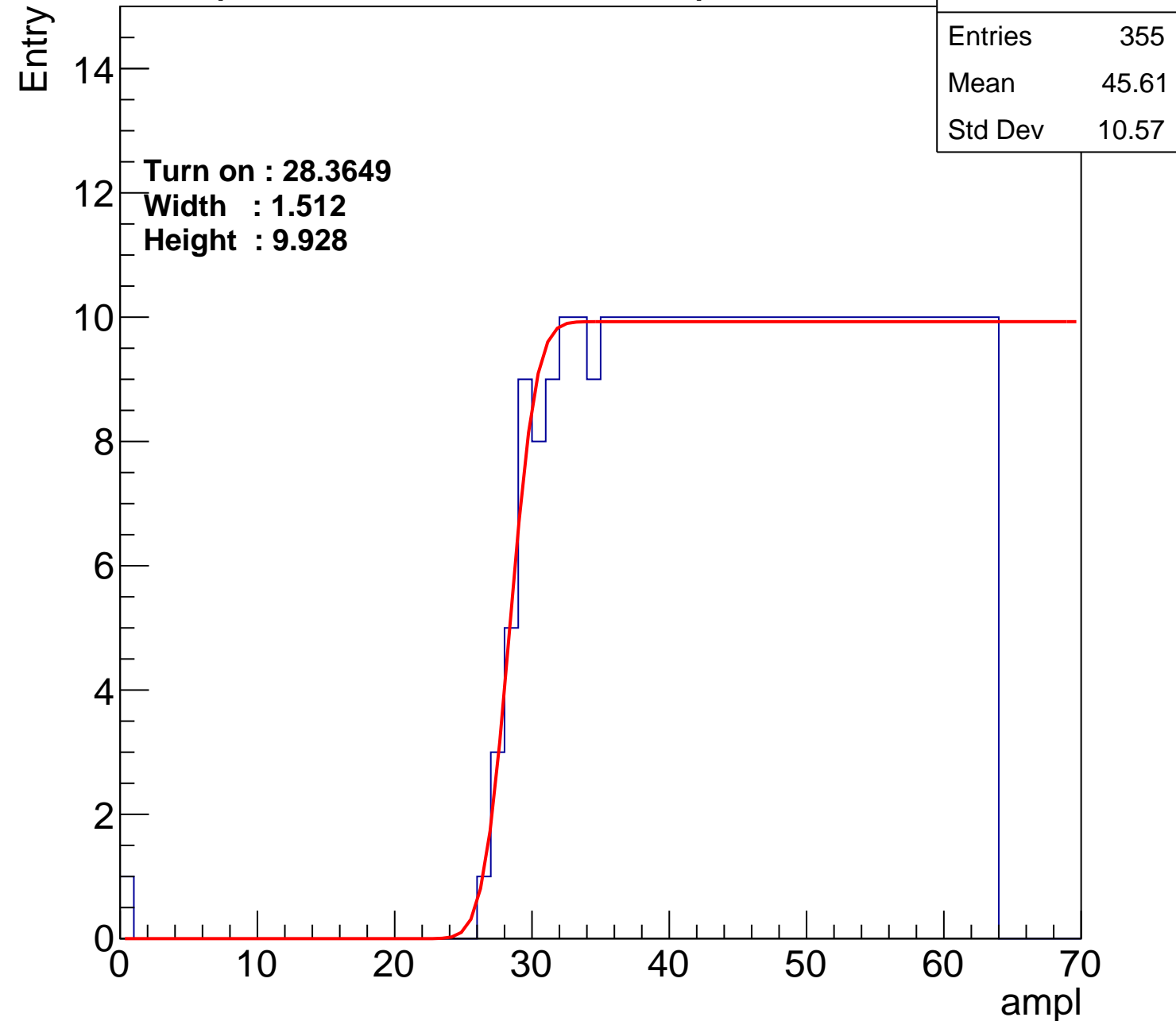
Width : 1.512

Height : 9.928

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch45

calib_packv5_042523_0143.root, FC#8, port C1

Entries	358
Mean	45.27
Std Dev	11.18

Turn on : 28.7649

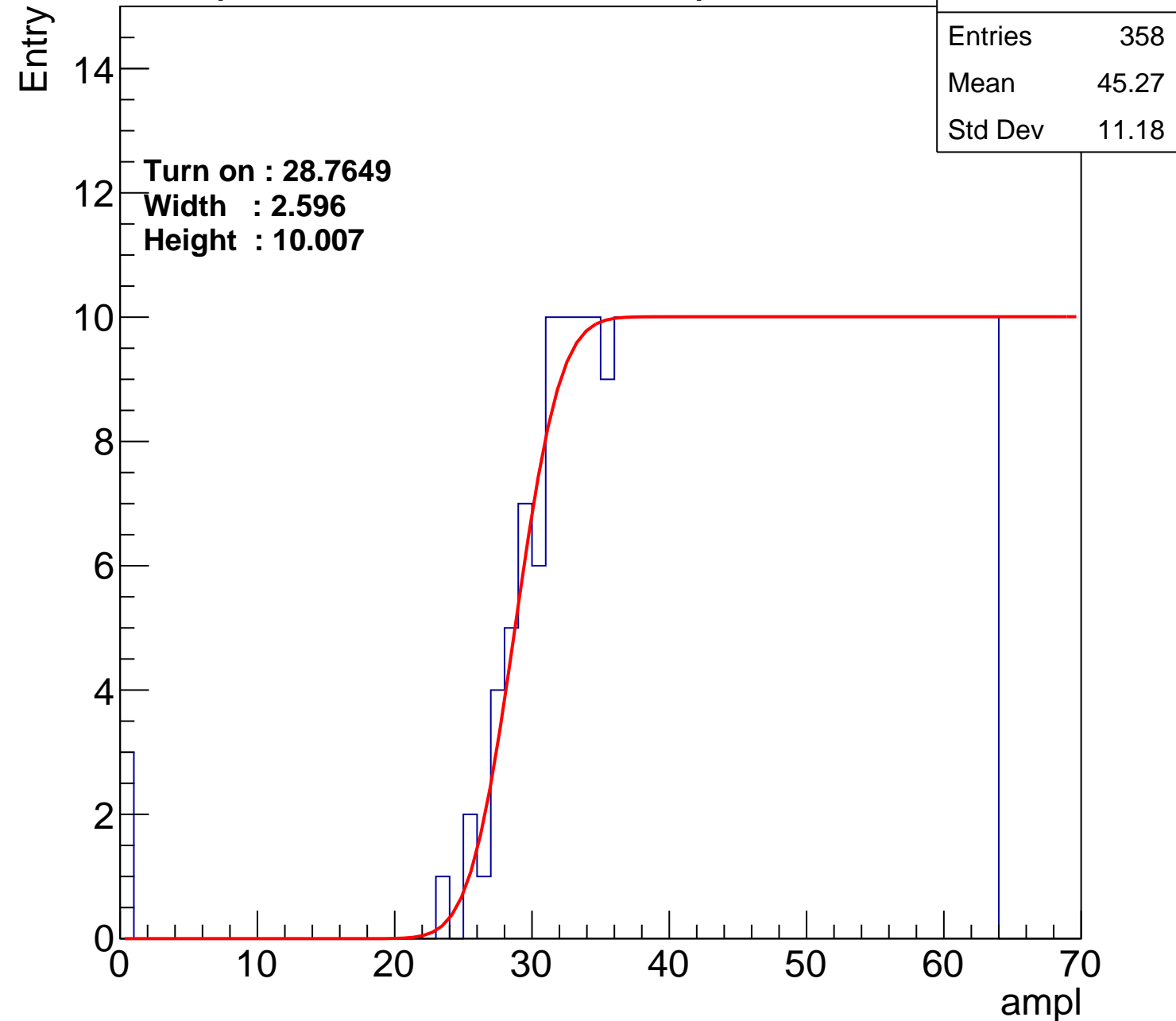
Width : 2.596

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch46

calib_packv5_042523_0143.root, FC#8, port C1

Entries	379
Mean	44.31
Std Dev	11.48

Turn on : 26.4250

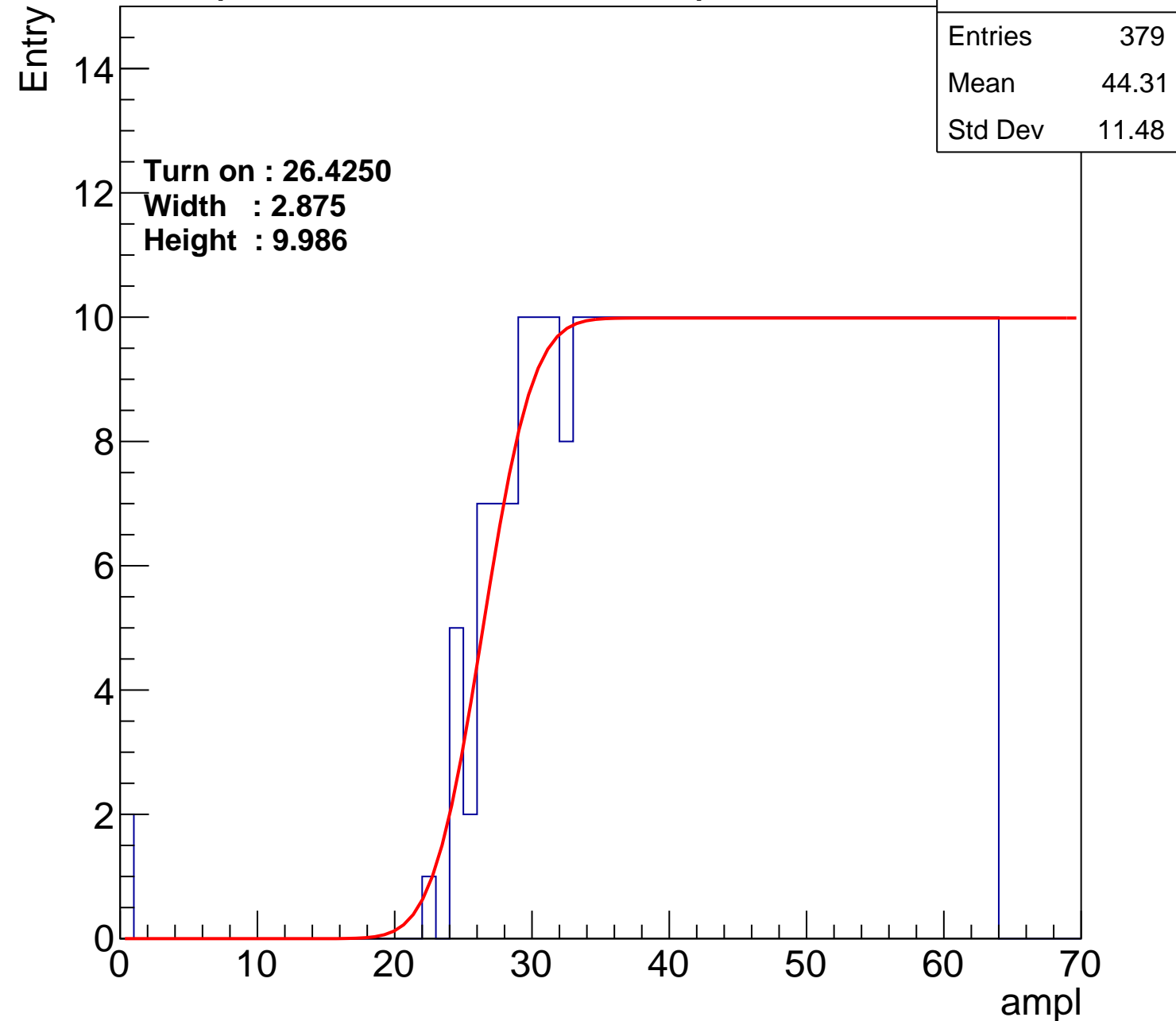
Width : 2.875

Height : 9.986

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch47

calib_packv5_042523_0143.root, FC#8, port C1

Entries	351
Mean	45.7
Std Dev	10.75

Turn on : 28.7558

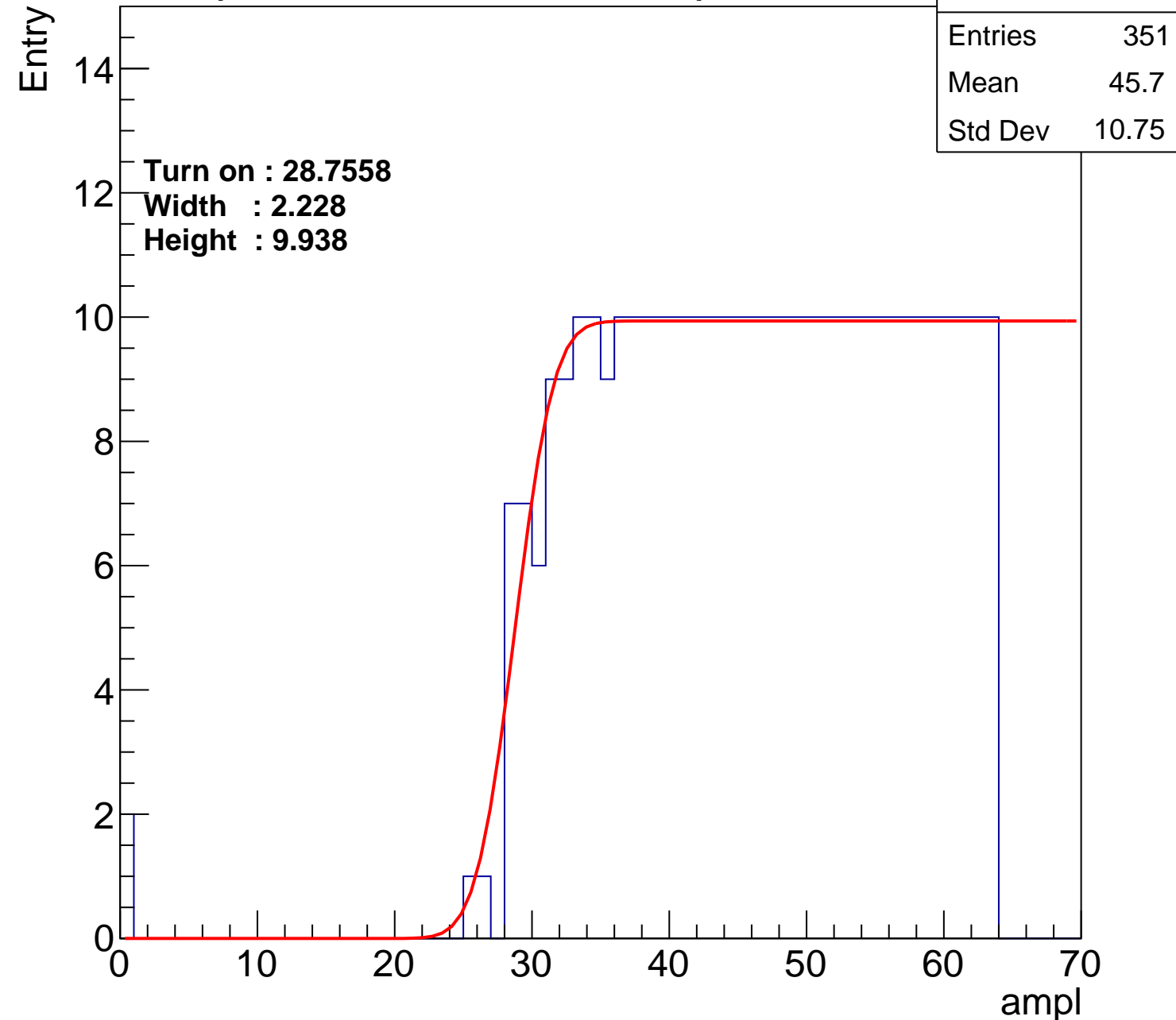
Width : 2.228

Height : 9.938

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch48

calib_packv5_042523_0143.root, FC#8, port C1

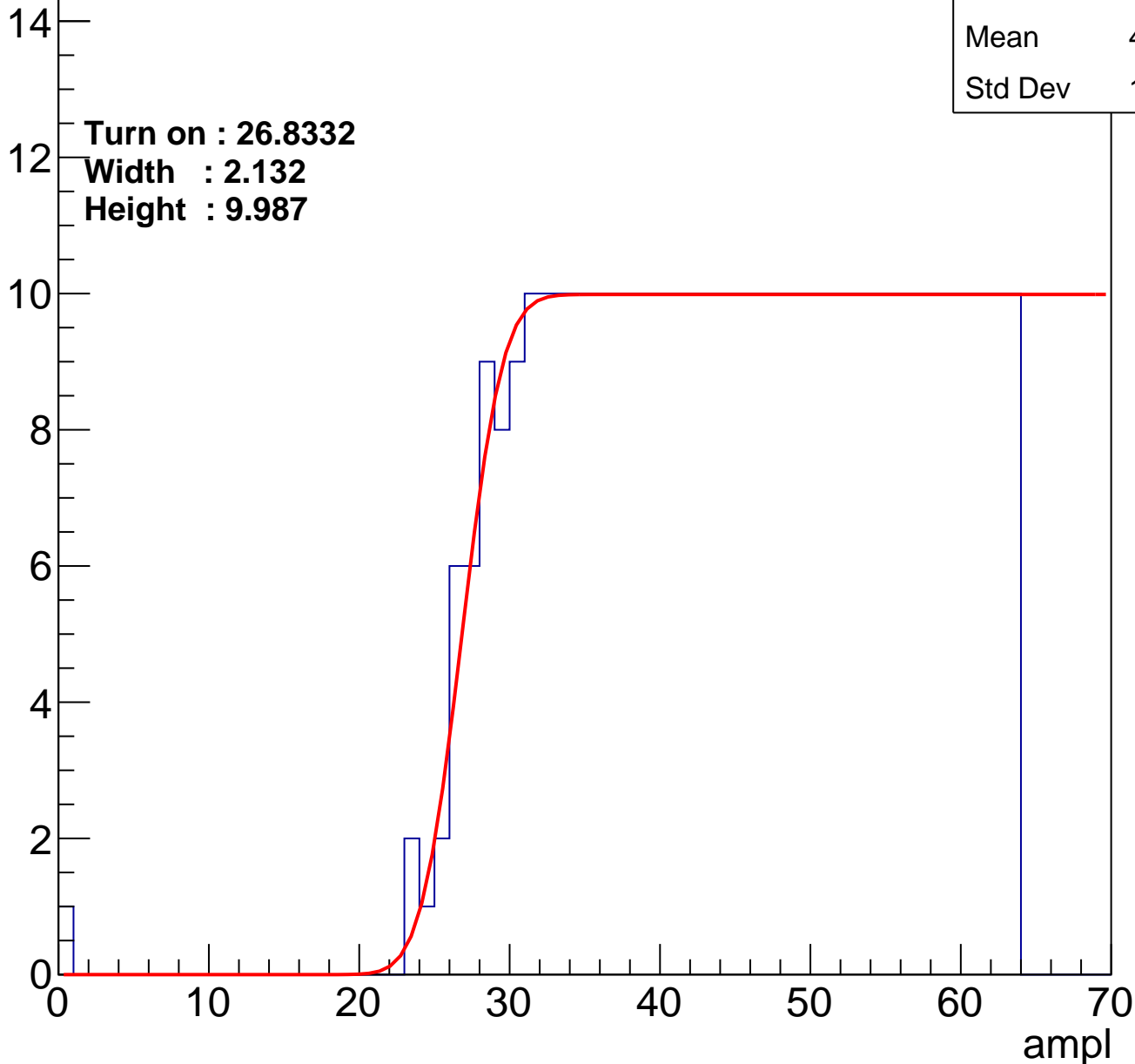
Entry

Entries	374
Mean	44.66
Std Dev	11.12

Turn on : 26.8332

Width : 2.132

Height : 9.987



B0L002S, U7-ch49

calib_packv5_042523_0143.root, FC#8, port C1

Entries	364
Mean	44.88
Std Dev	11.55

Turn on : 28.3222

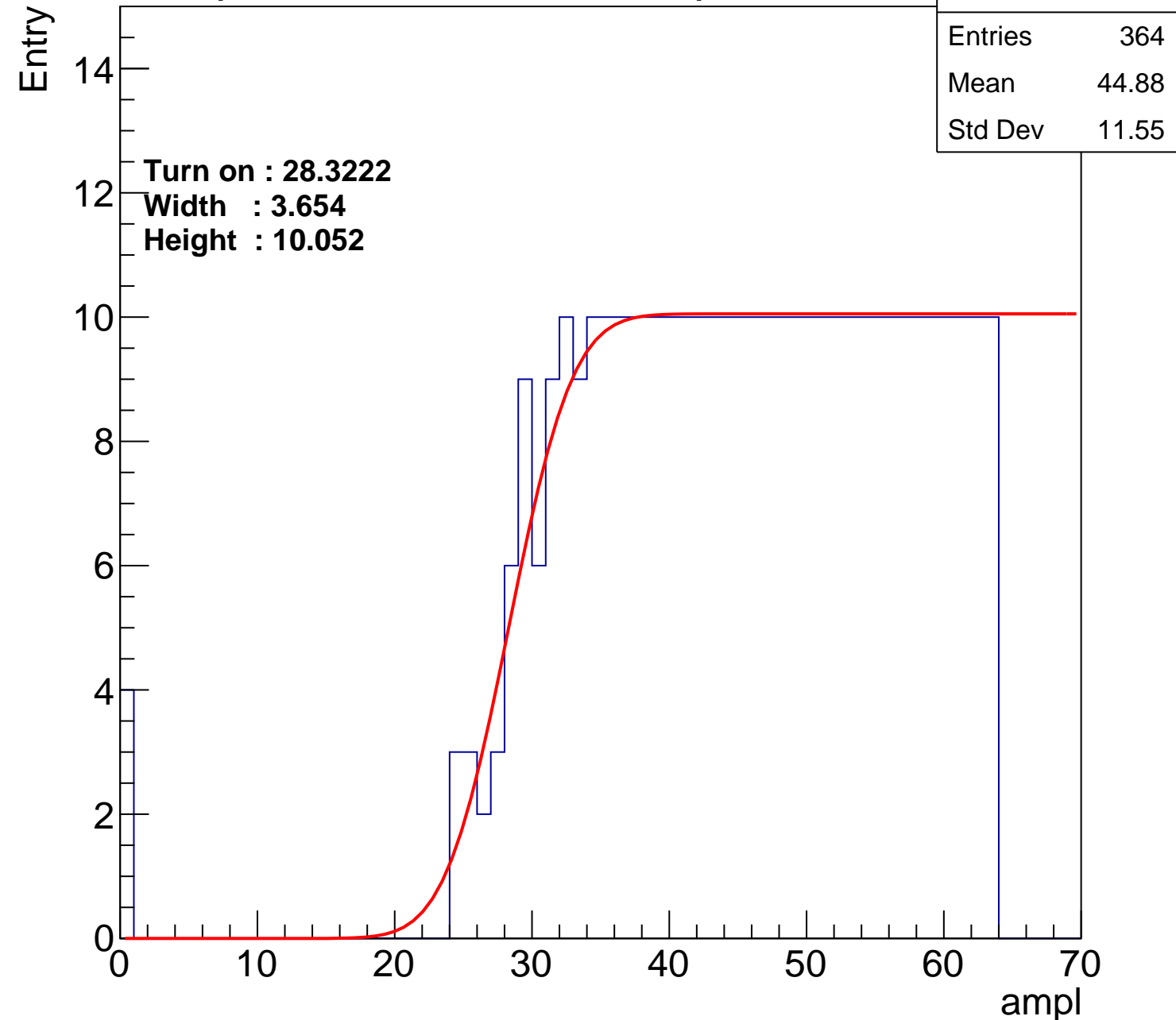
Width : 3.654

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch50

calib_packv5_042523_0143.root, FC#8, port C1

Entries	349
Mean	45.86
Std Dev	10.5

Turn on : 28.9371

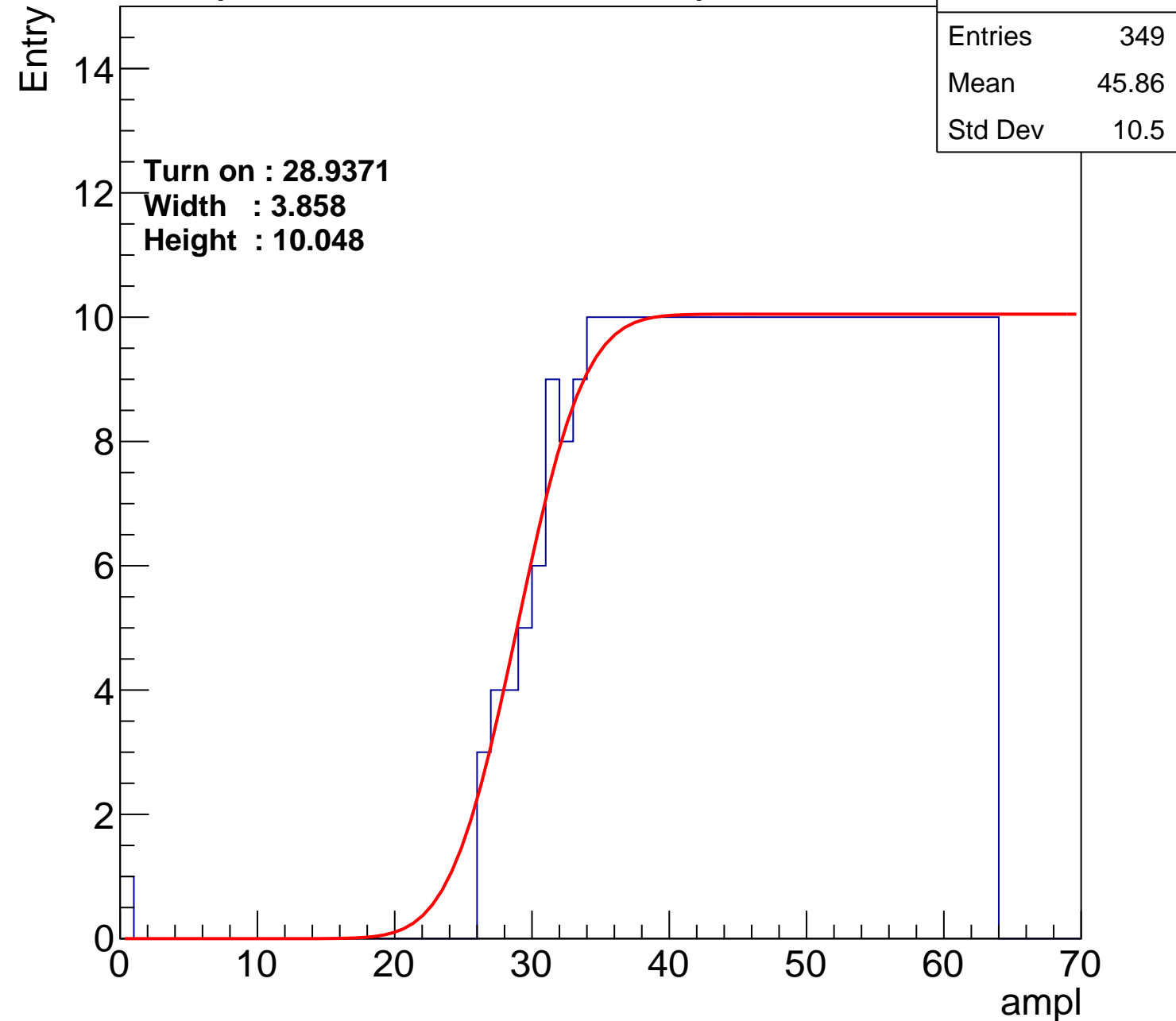
Width : 3.858

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch51

calib_packv5_042523_0143.root, FC#8, port C1

Entries	350
Mean	45.7
Std Dev	10.81

Turn on : 29.2273

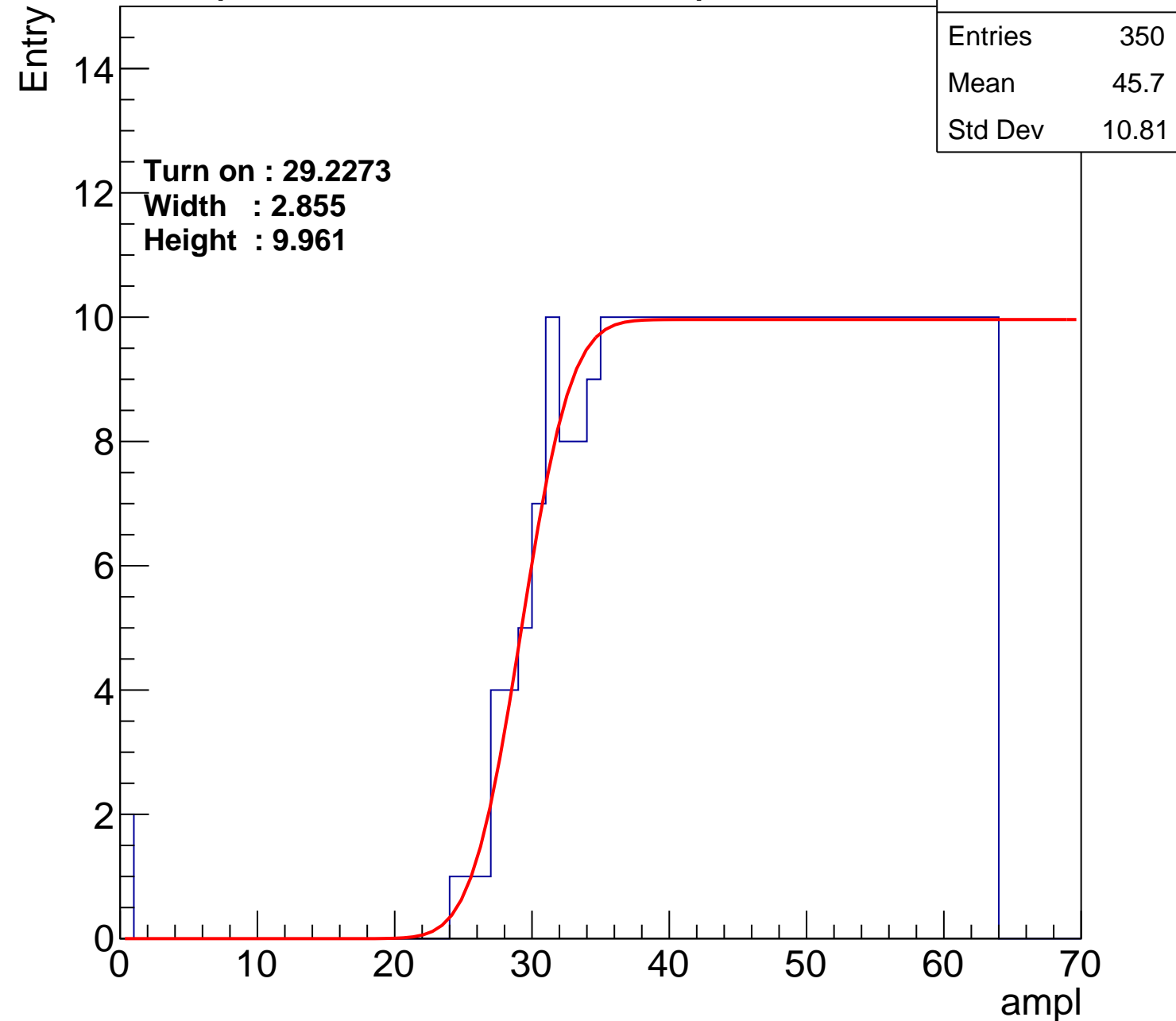
Width : 2.855

Height : 9.961

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch52

calib_packv5_042523_0143.root, FC#8, port C1

Entries	363
Mean	45.08
Std Dev	11.13

Turn on : 28.2229

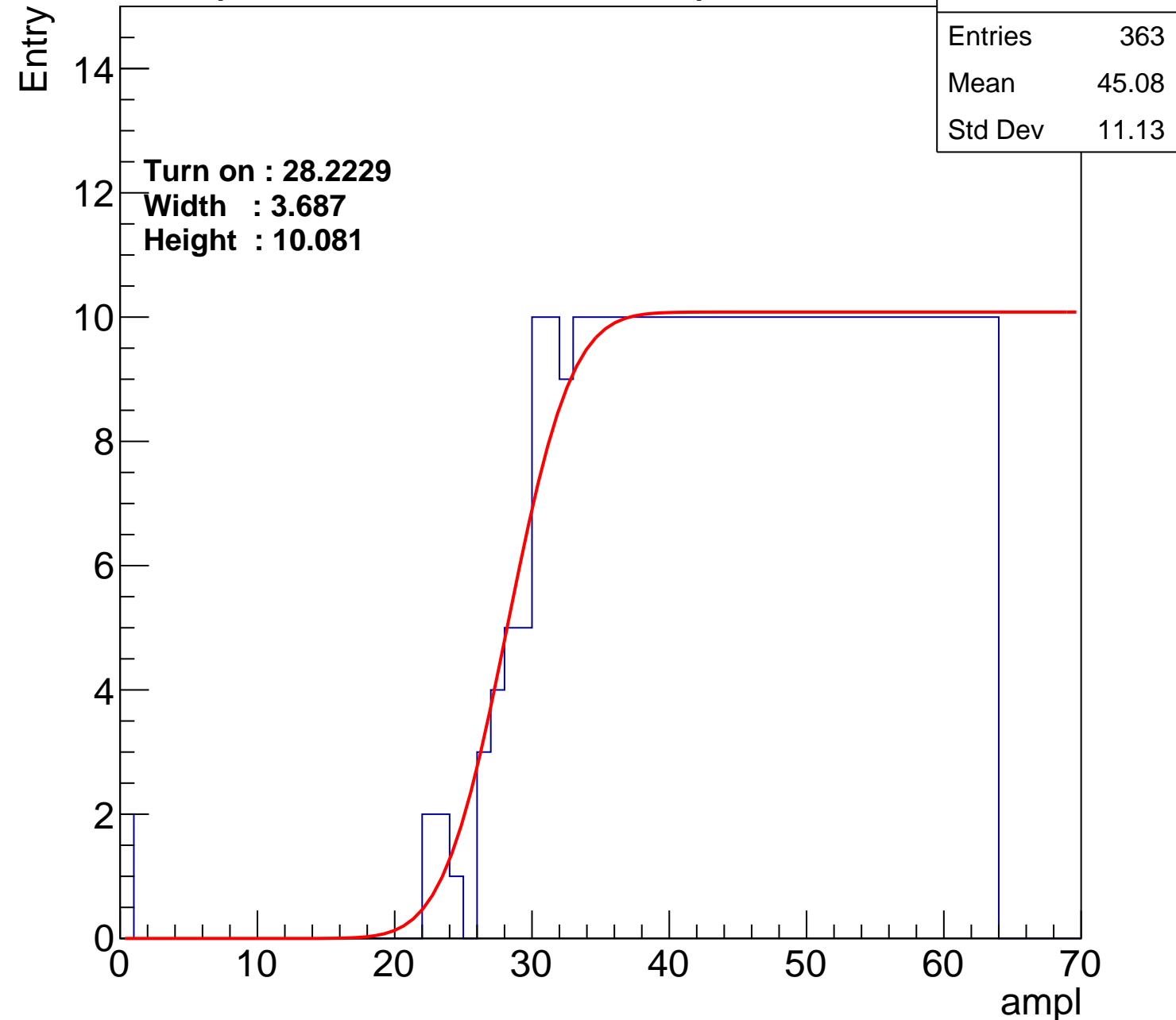
Width : 3.687

Height : 10.081

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch53

calib_packv5_042523_0143.root, FC#8, port C1

Entries	370
Mean	44.79
Std Dev	11.2

Turn on : 26.8724

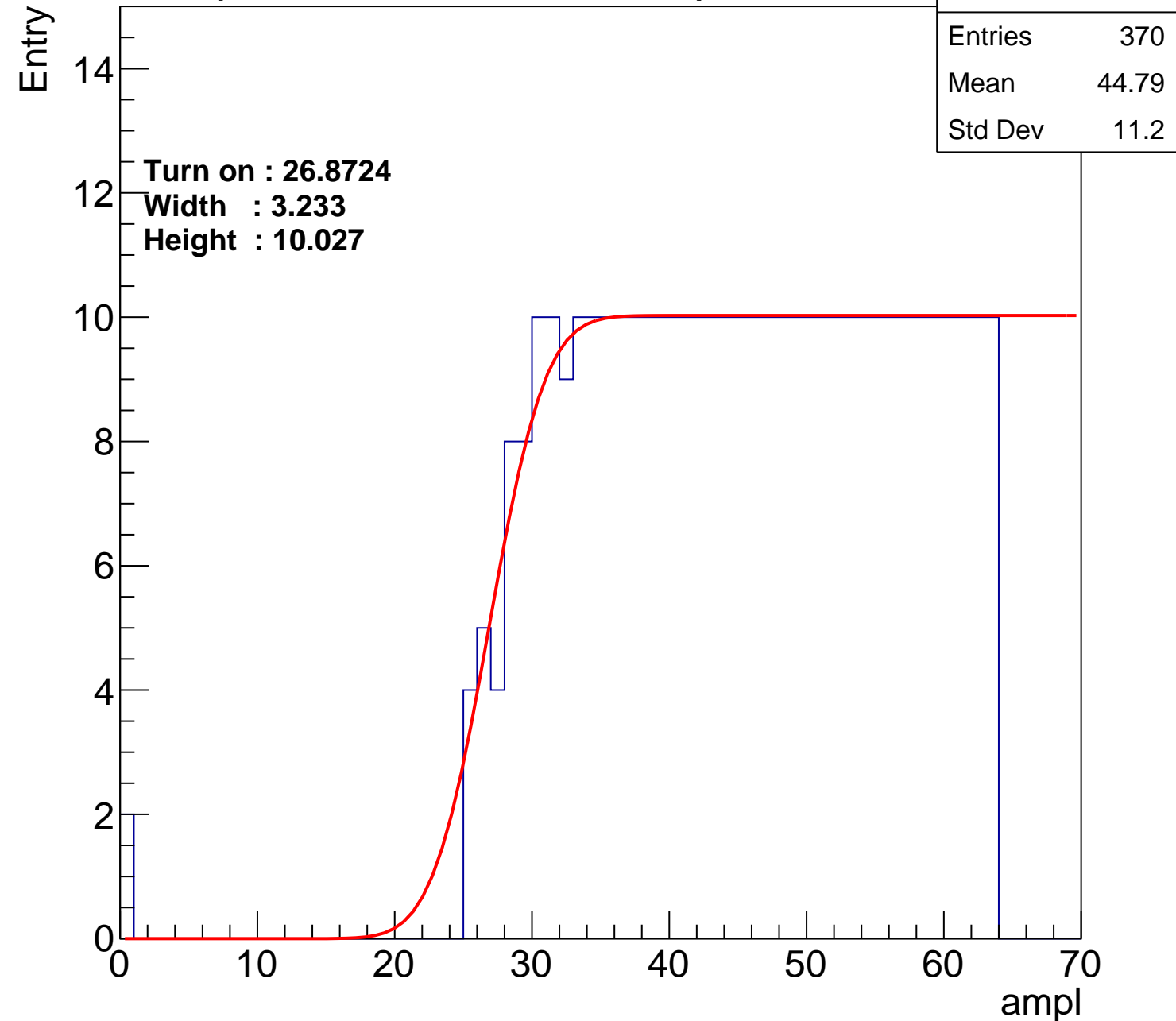
Width : 3.233

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch54

calib_packv5_042523_0143.root, FC#8, port C1

Entries	379
Mean	44.27
Std Dev	11.63

Turn on : 26.7435

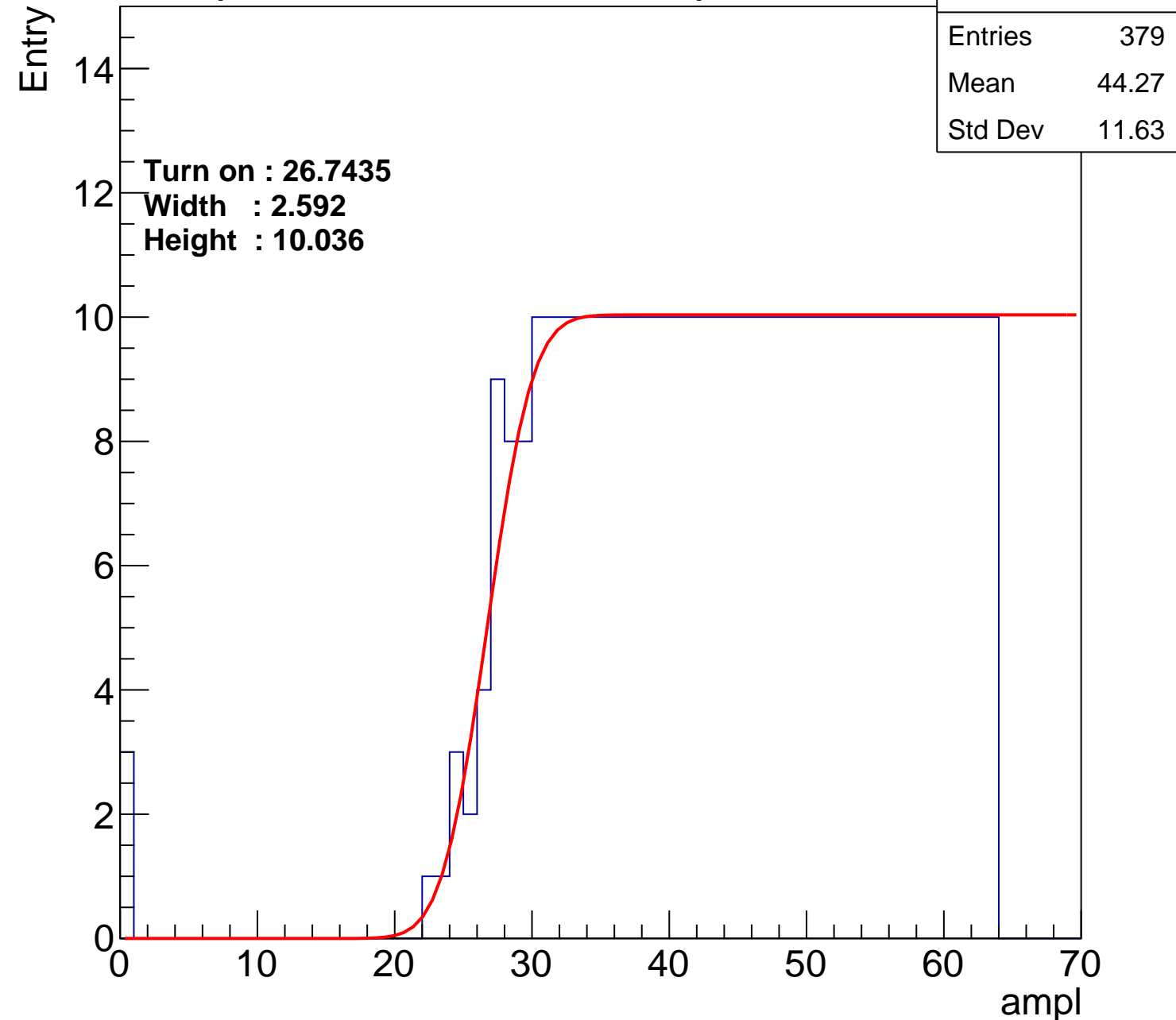
Width : 2.592

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch55

calib_packv5_042523_0143.root, FC#8, port C1

Entries	366
Mean	44.89
Std Dev	11.26

Turn on : 28.2104

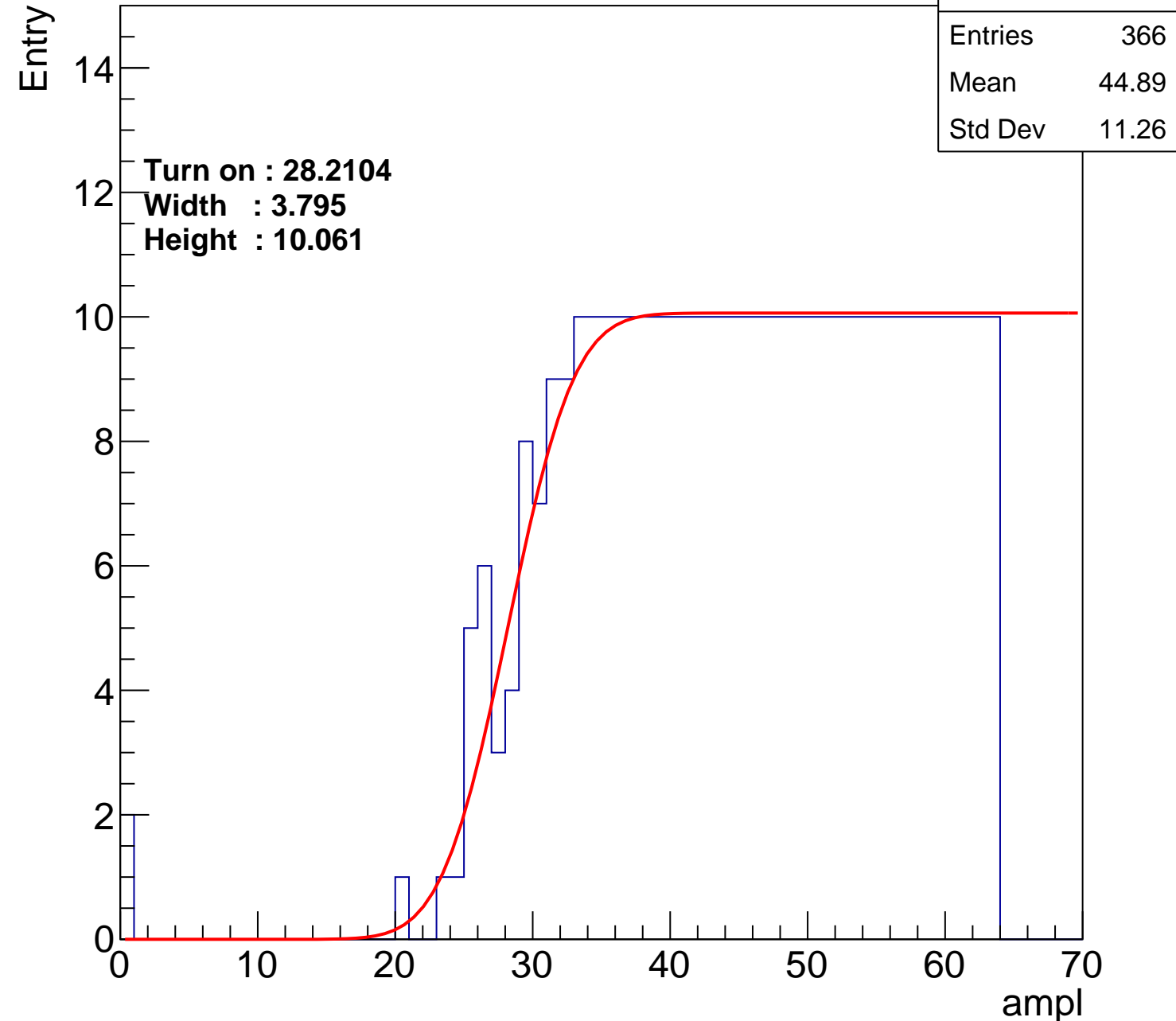
Width : 3.795

Height : 10.061

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch56

calib_packv5_042523_0143.root, FC#8, port C1

Entries	381
Mean	44.16
Std Dev	11.7

Turn on : 26.6645

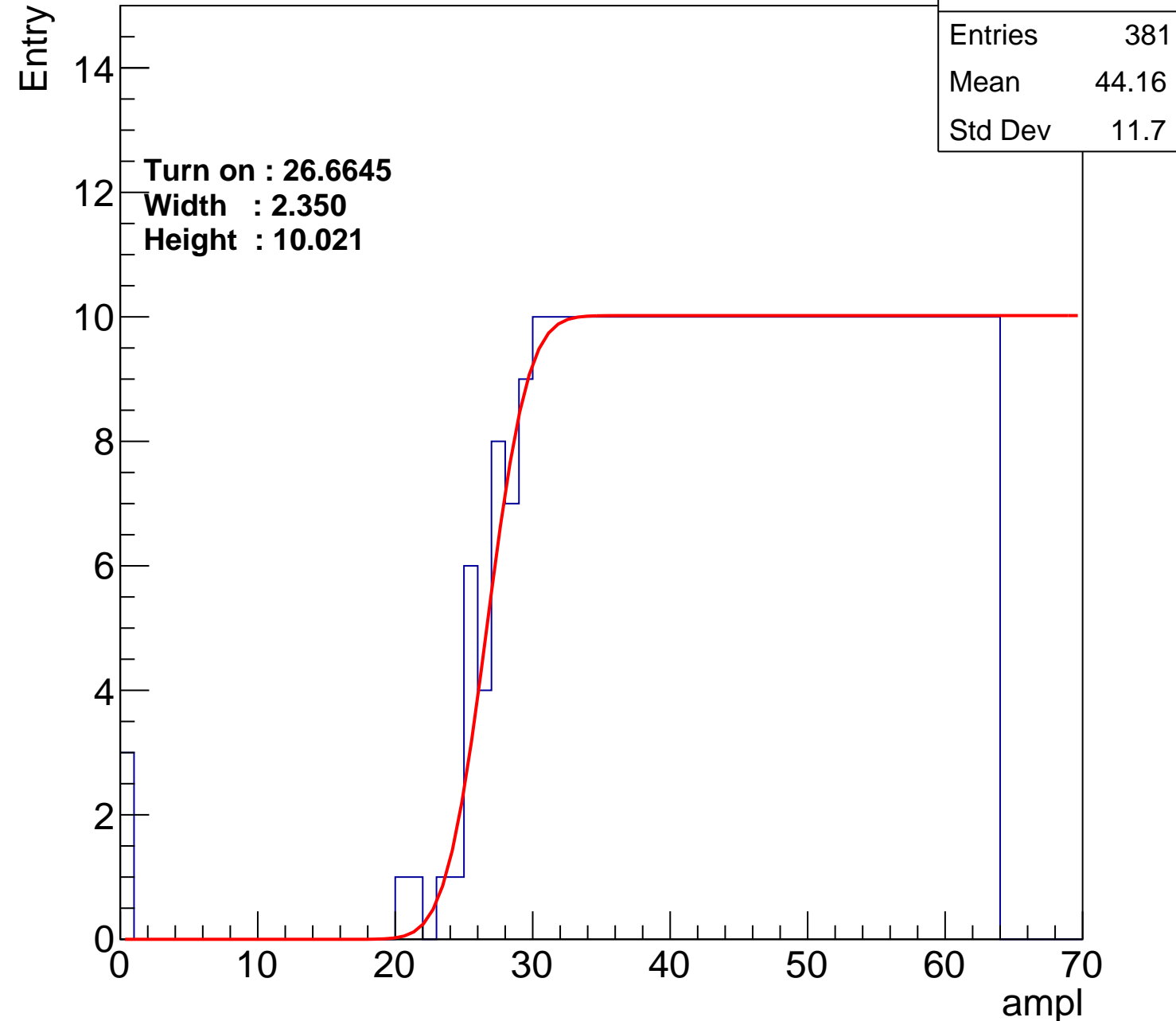
Width : 2.350

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch57

calib_packv5_042523_0143.root, FC#8, port C1

Entries	361
Mean	45.24
Std Dev	10.97

Turn on : 28.8685

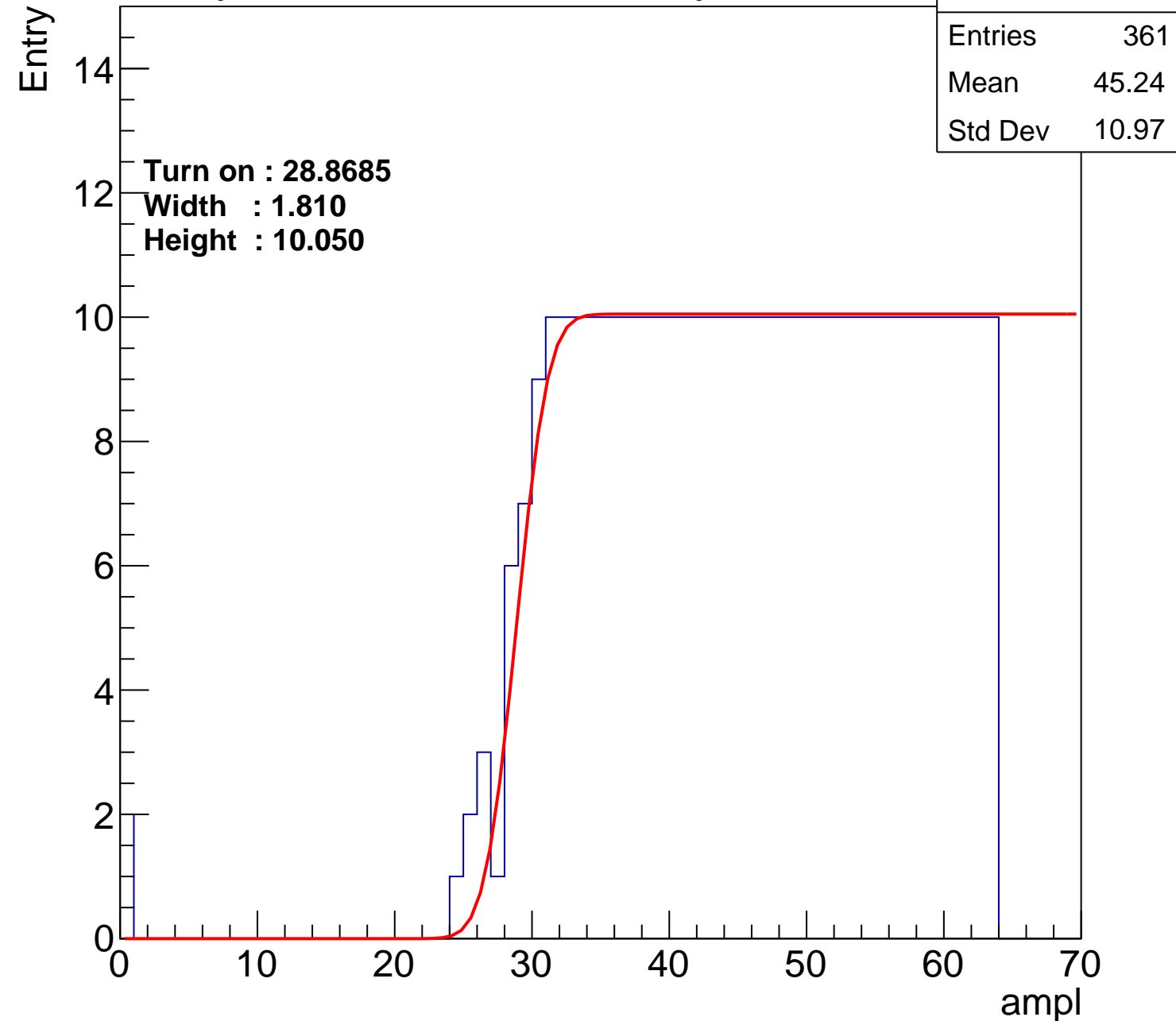
Width : 1.810

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch58

calib_packv5_042523_0143.root, FC#8, port C1

Entries	373
Mean	44.71
Std Dev	11.09

Turn on : 26.8097

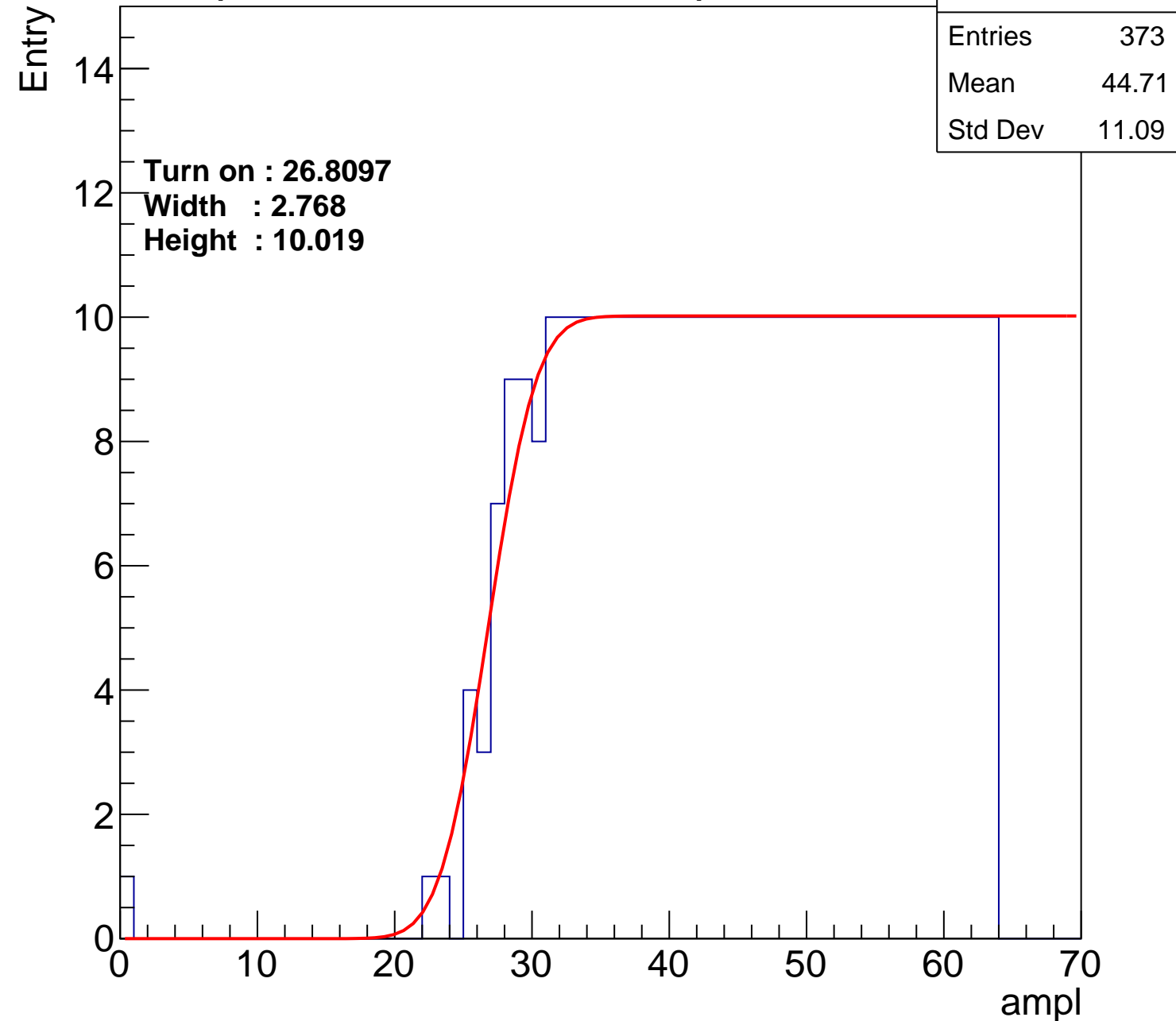
Width : 2.768

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch59

calib_packv5_042523_0143.root, FC#8, port C1

Entries	366
Mean	44.94
Std Dev	11.17

Turn on : 27.8447

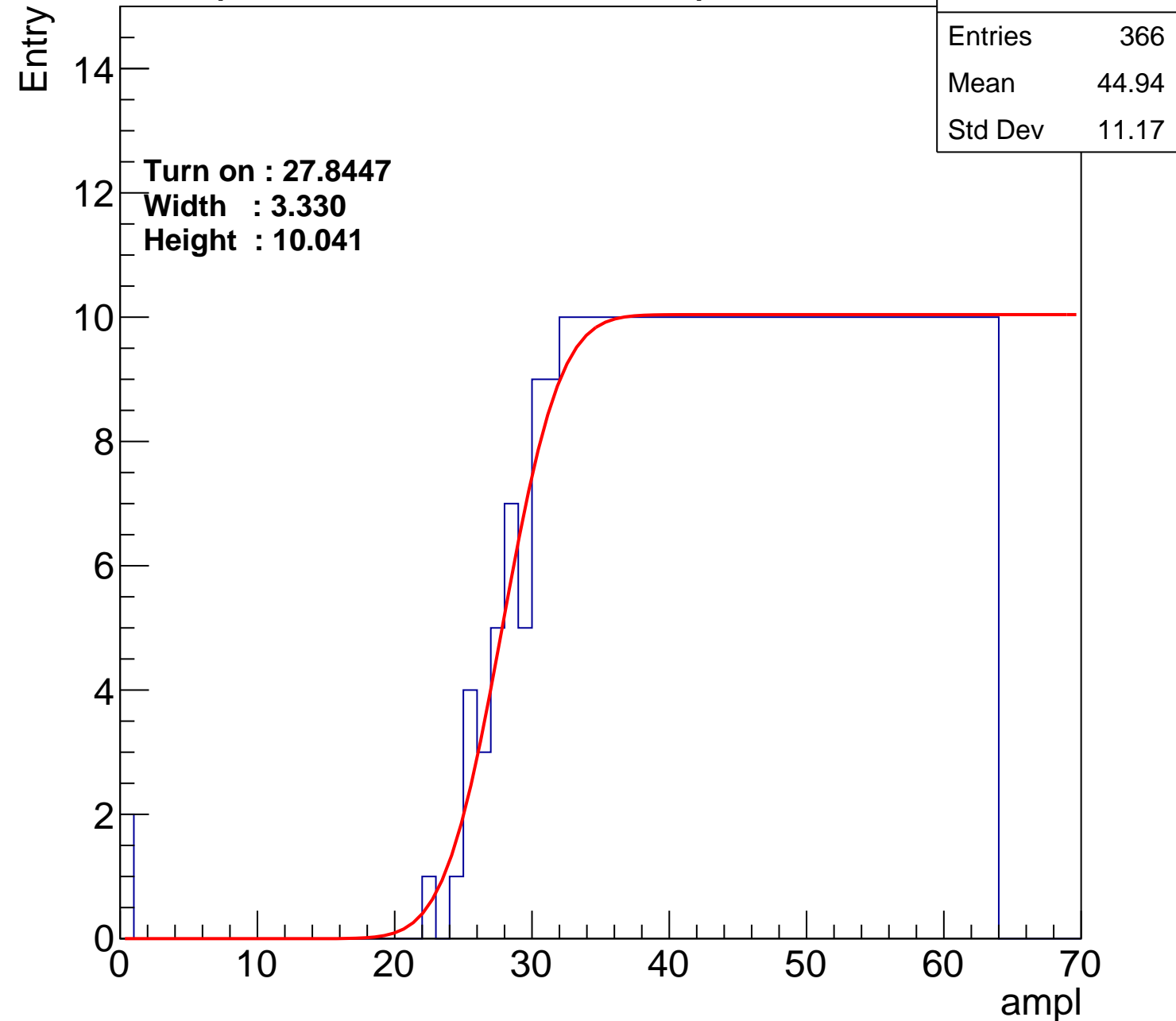
Width : 3.330

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch60

calib_packv5_042523_0143.root, FC#8, port C1

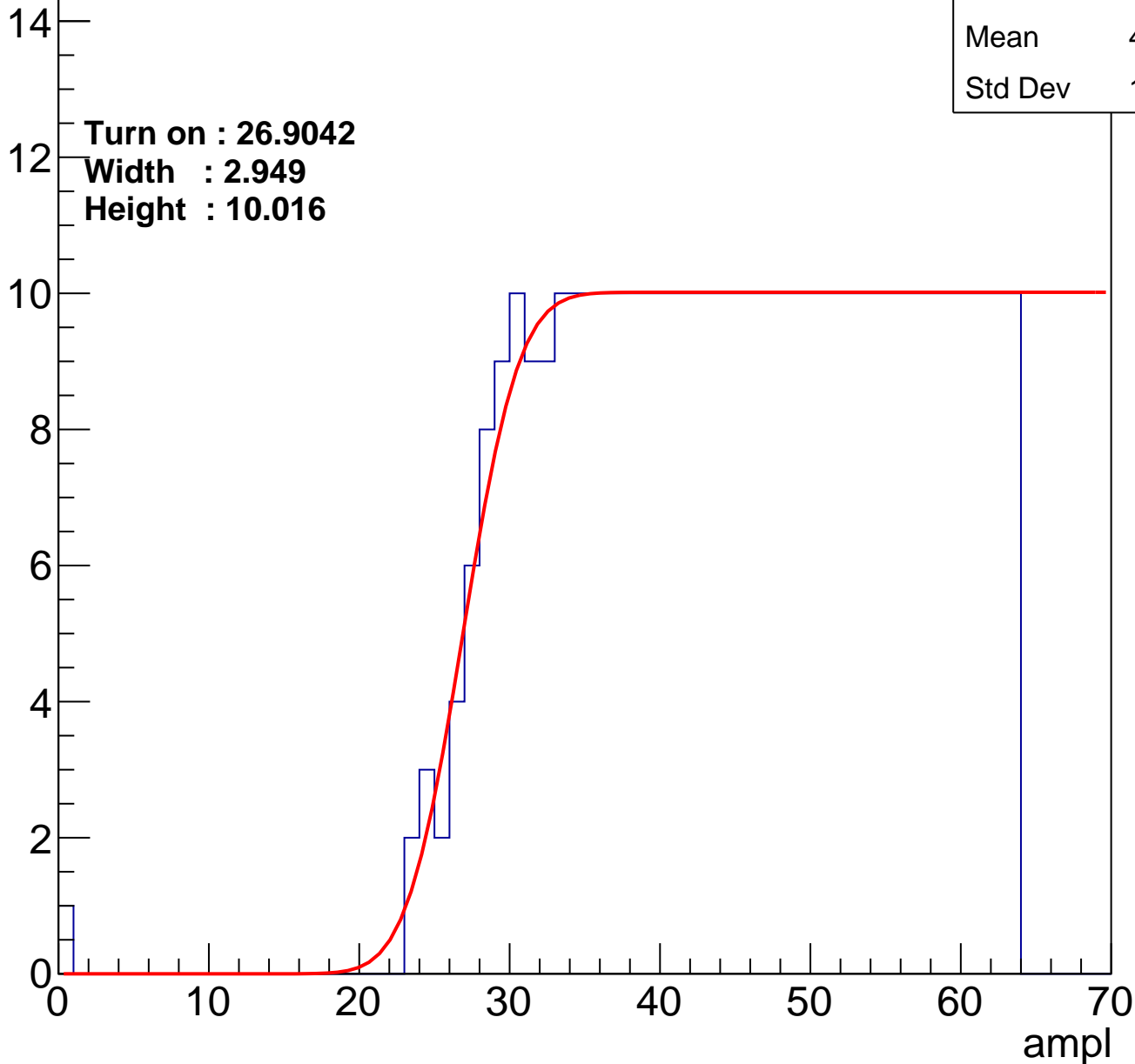
Entry

Entries	373
Mean	44.68
Std Dev	11.13

Turn on : 26.9042

Width : 2.949

Height : 10.016



B0L002S, U7-ch61

calib_packv5_042523_0143.root, FC#8, port C1

Entries	374
Mean	44.65
Std Dev	11.13

Turn on : 26.6452

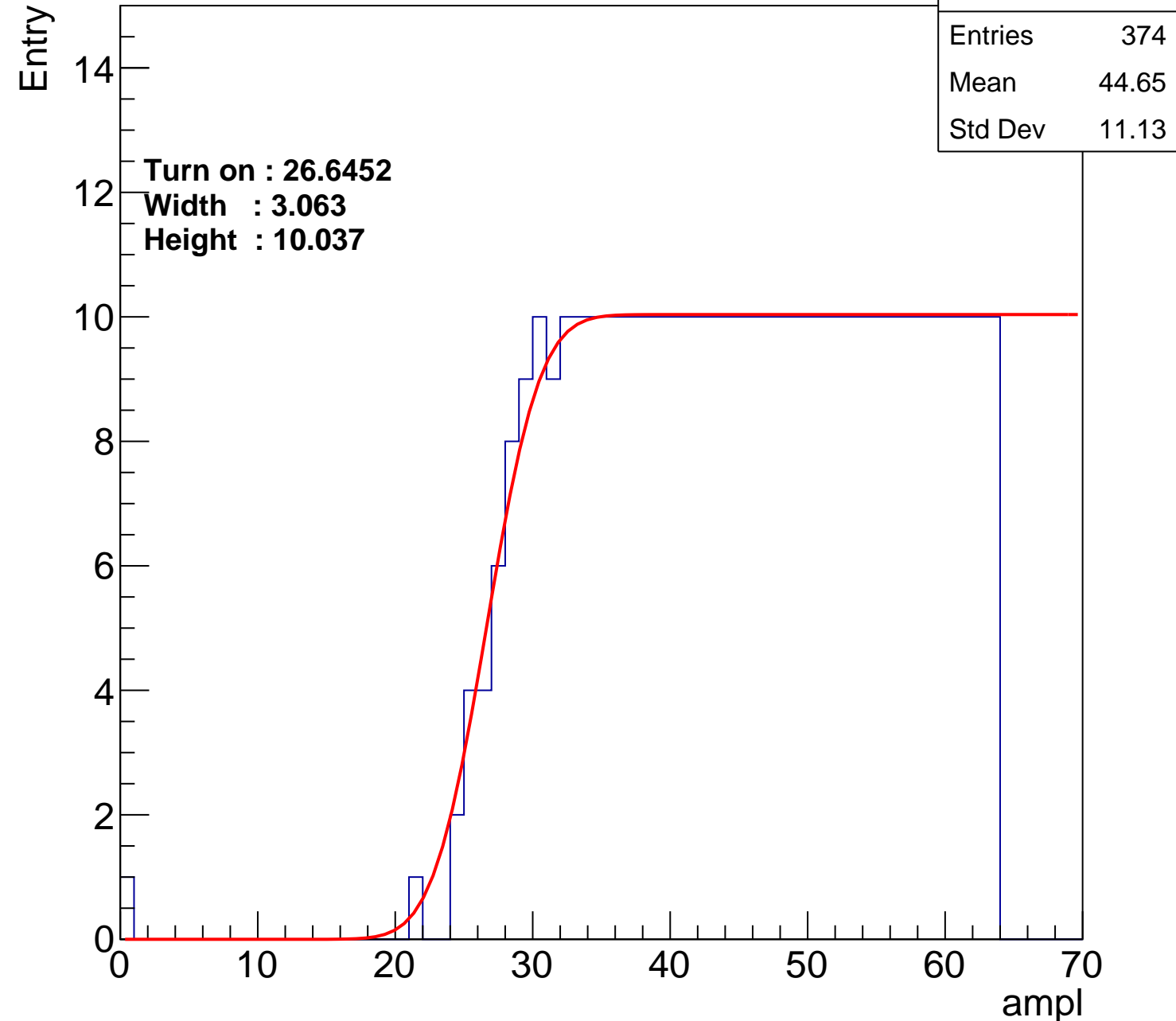
Width : 3.063

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch62

calib_packv5_042523_0143.root, FC#8, port C1

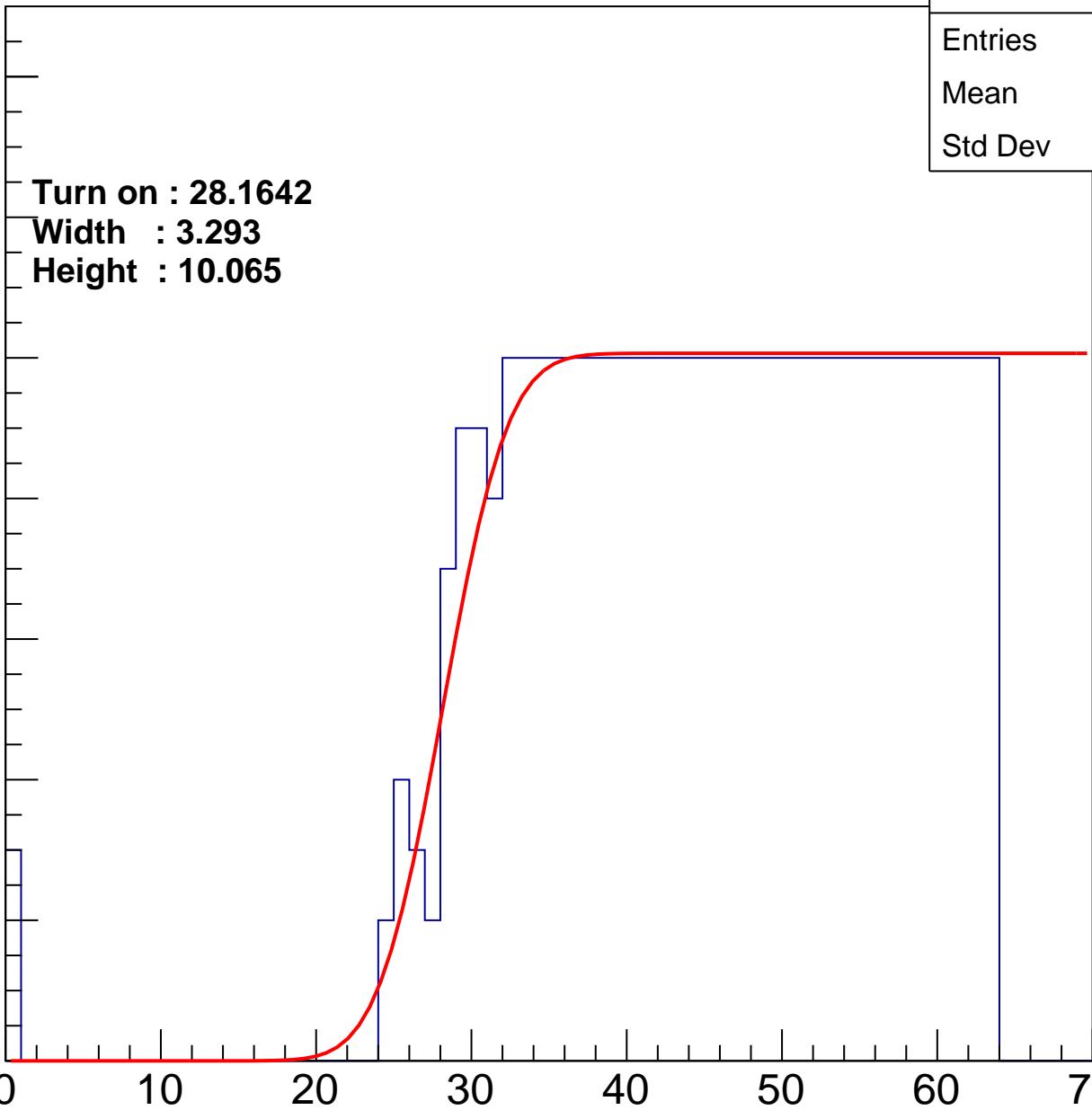
Entry

14
12
10
8
6
4
2
0

Turn on : 28.1642
Width : 3.293
Height : 10.065

Entries	367
Mean	44.84
Std Dev	11.37

ampl



B0L002S, U7-ch63

calib_packv5_042523_0143.root, FC#8, port C1

Entries	390
Mean	43.89
Std Dev	11.51

Turn on : 24.9305

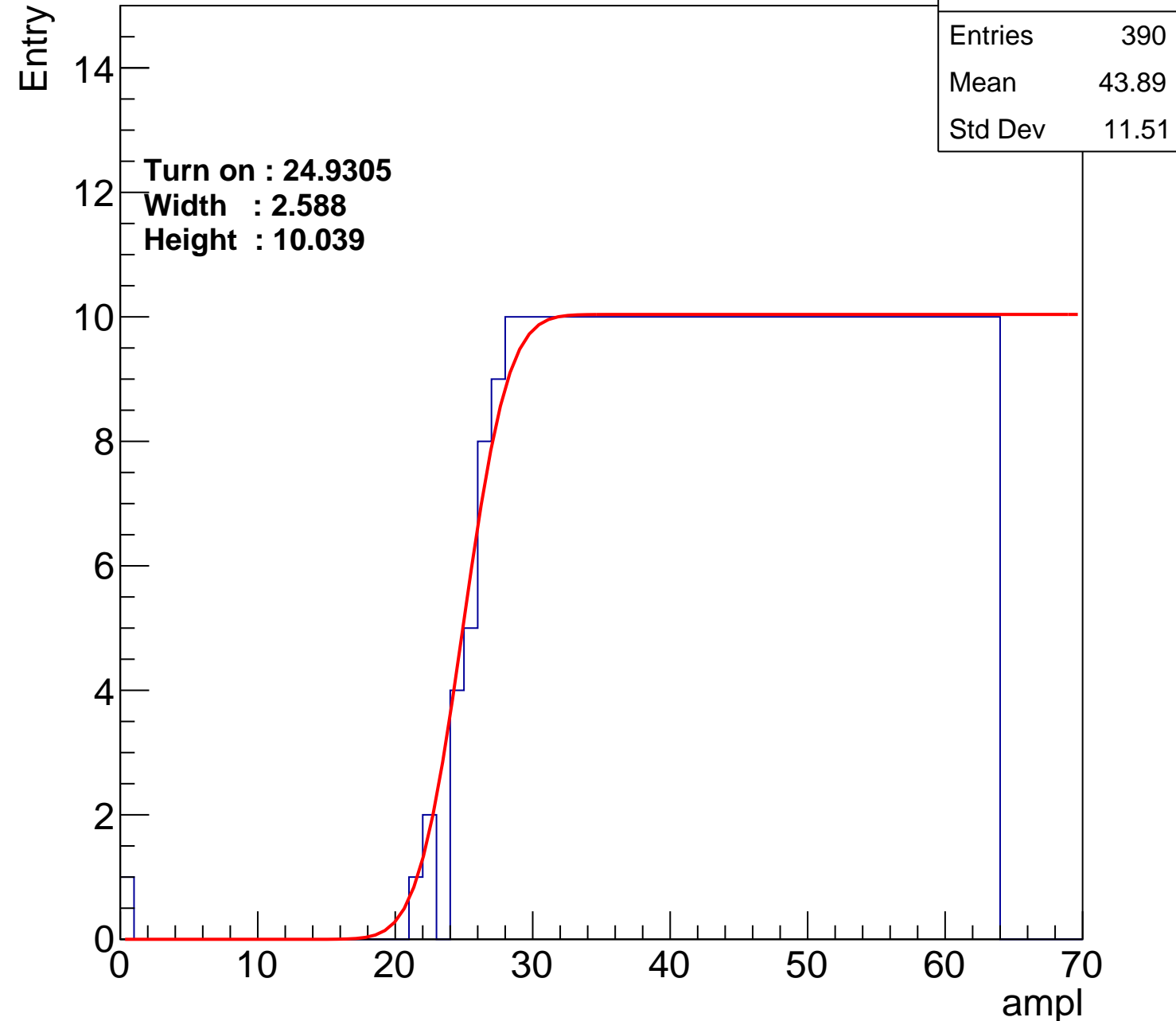
Width : 2.588

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch64

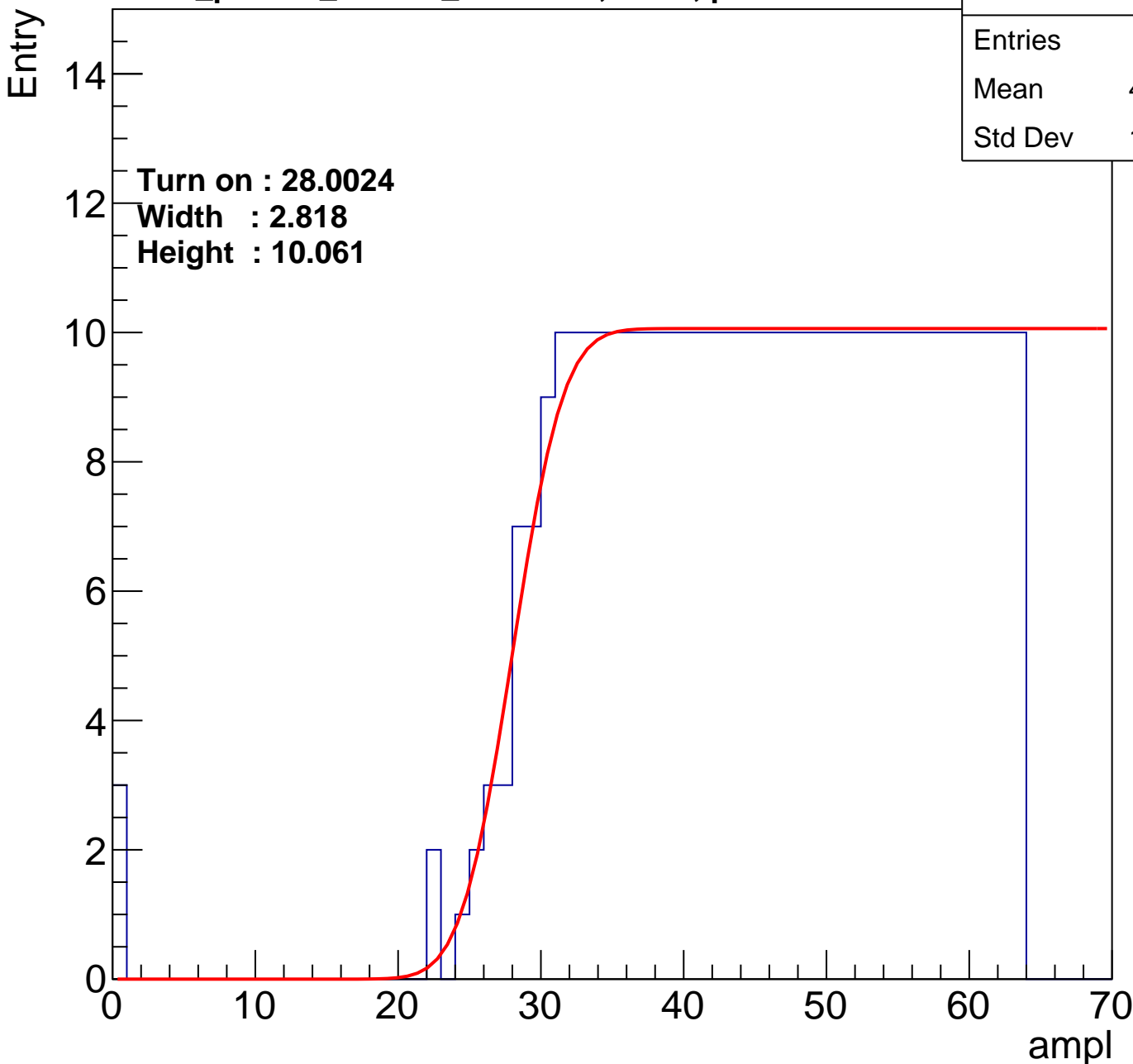
calib_packv5_042523_0143.root, FC#8, port C1

Turn on : 28.0024

Width : 2.818

Height : 10.061

Entries	367
Mean	44.84
Std Dev	11.38



B0L002S, U7-ch65

calib_packv5_042523_0143.root, FC#8, port C1

Entries	367
Mean	45
Std Dev	10.94

Turn on : 27.5134

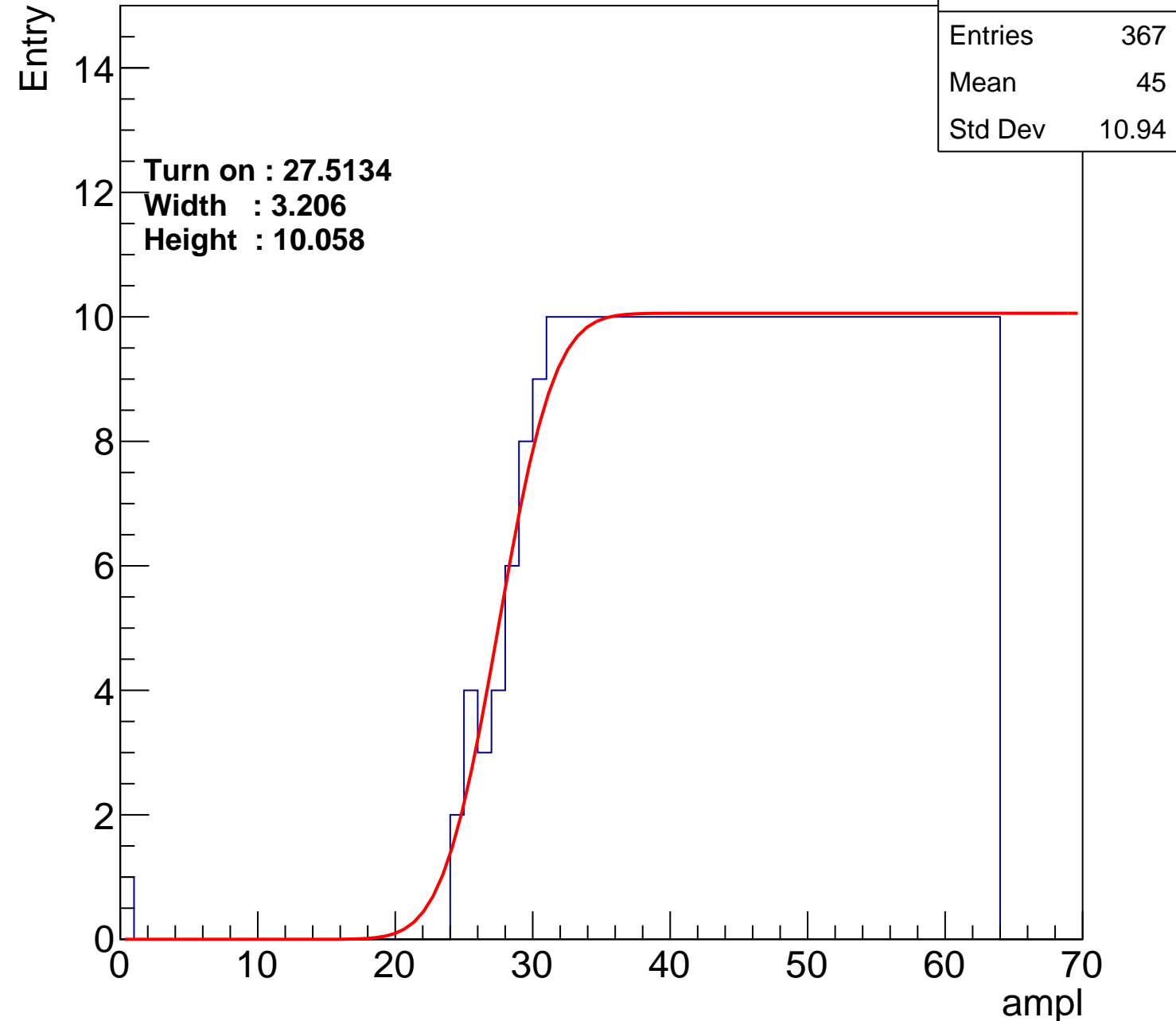
Width : 3.206

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch66

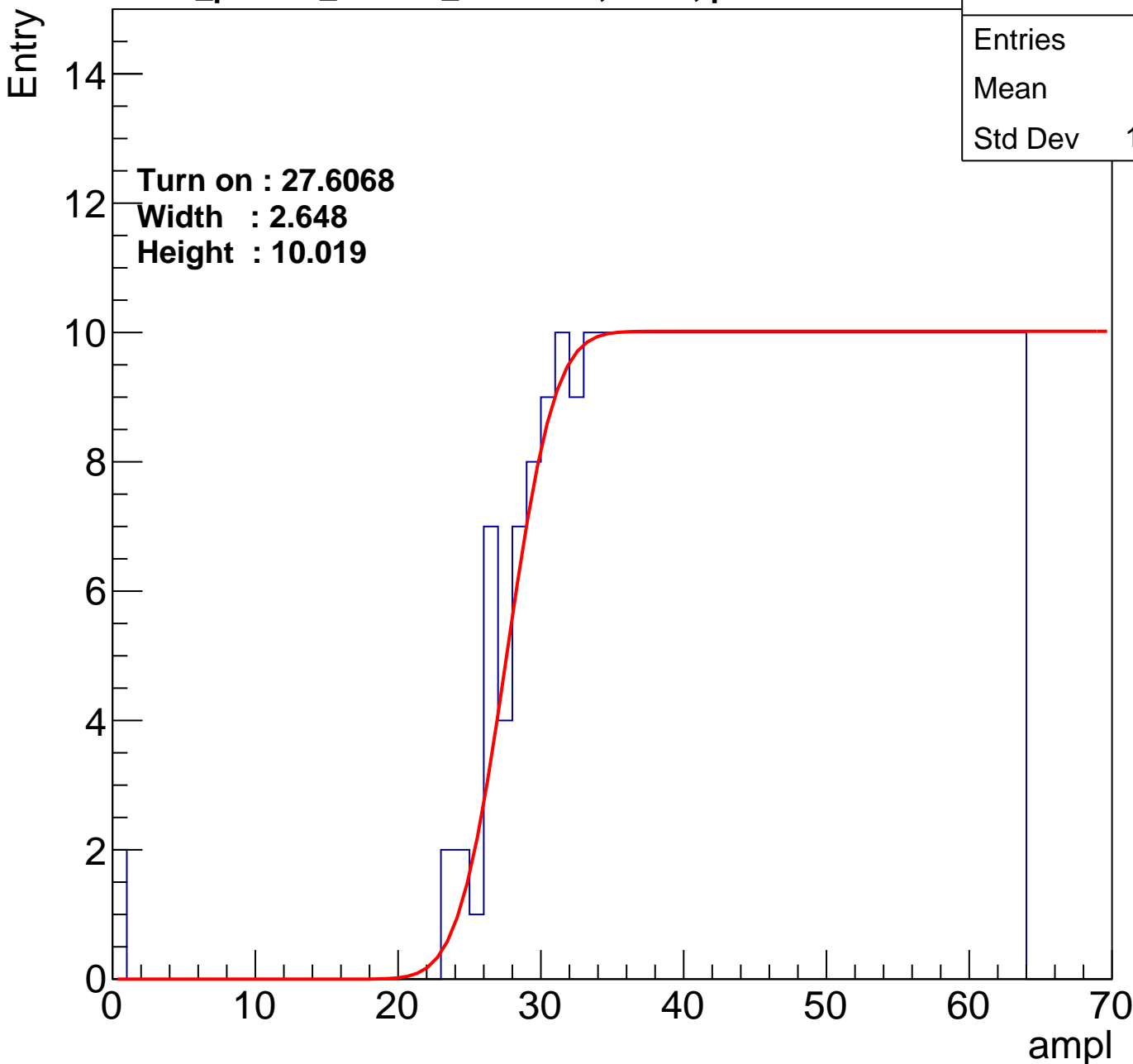
calib_packv5_042523_0143.root, FC#8, port C1

Entries	371
Mean	44.7
Std Dev	11.29

Turn on : 27.6068

Width : 2.648

Height : 10.019



B0L002S, U7-ch67

calib_packv5_042523_0143.root, FC#8, port C1

Entries	362
Mean	45.17
Std Dev	11.02

Turn on : 27.9526

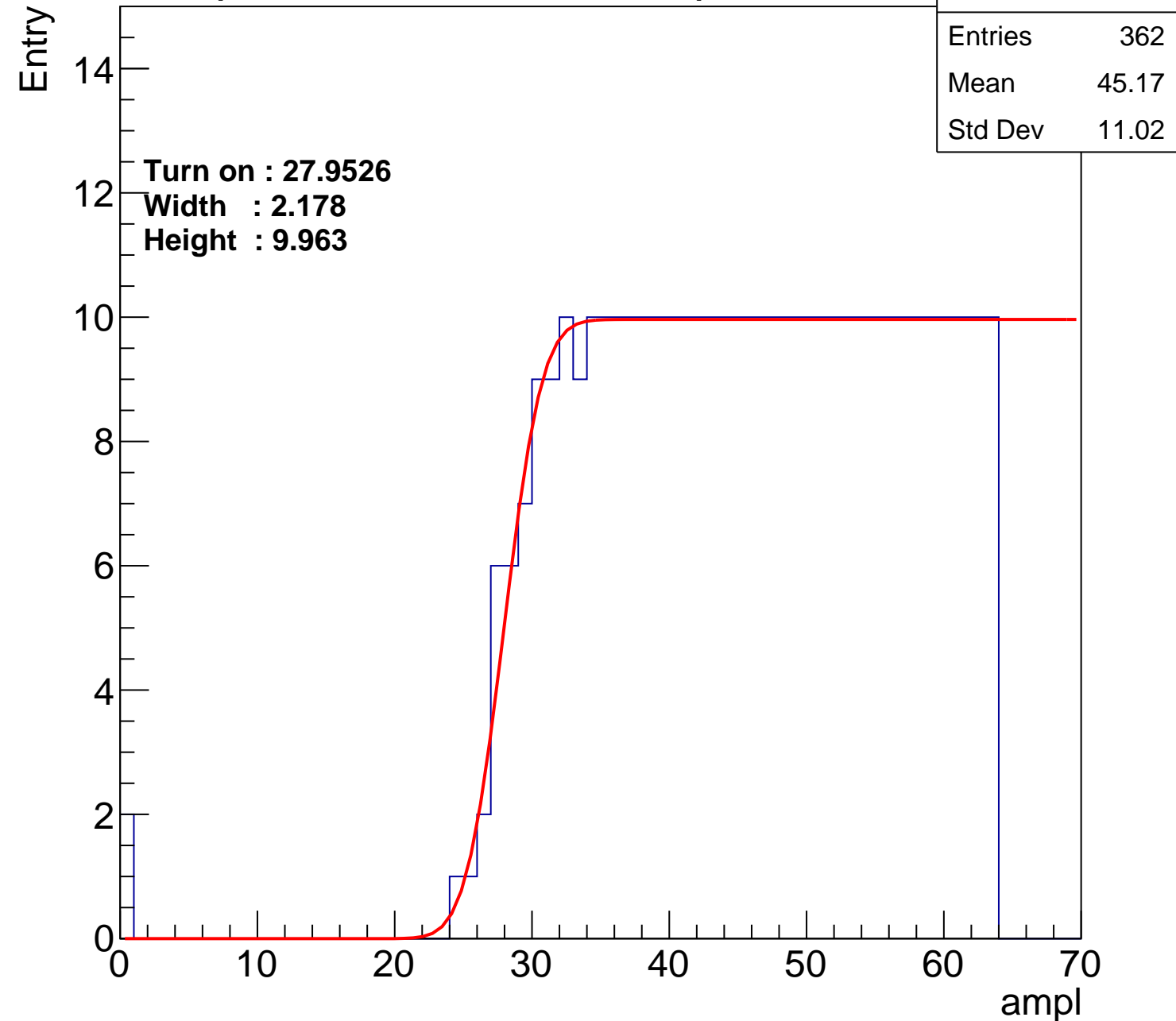
Width : 2.178

Height : 9.963

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch68

calib_packv5_042523_0143.root, FC#8, port C1

Entries	363
Mean	44.99
Std Dev	11.35

Turn on : 28.1716

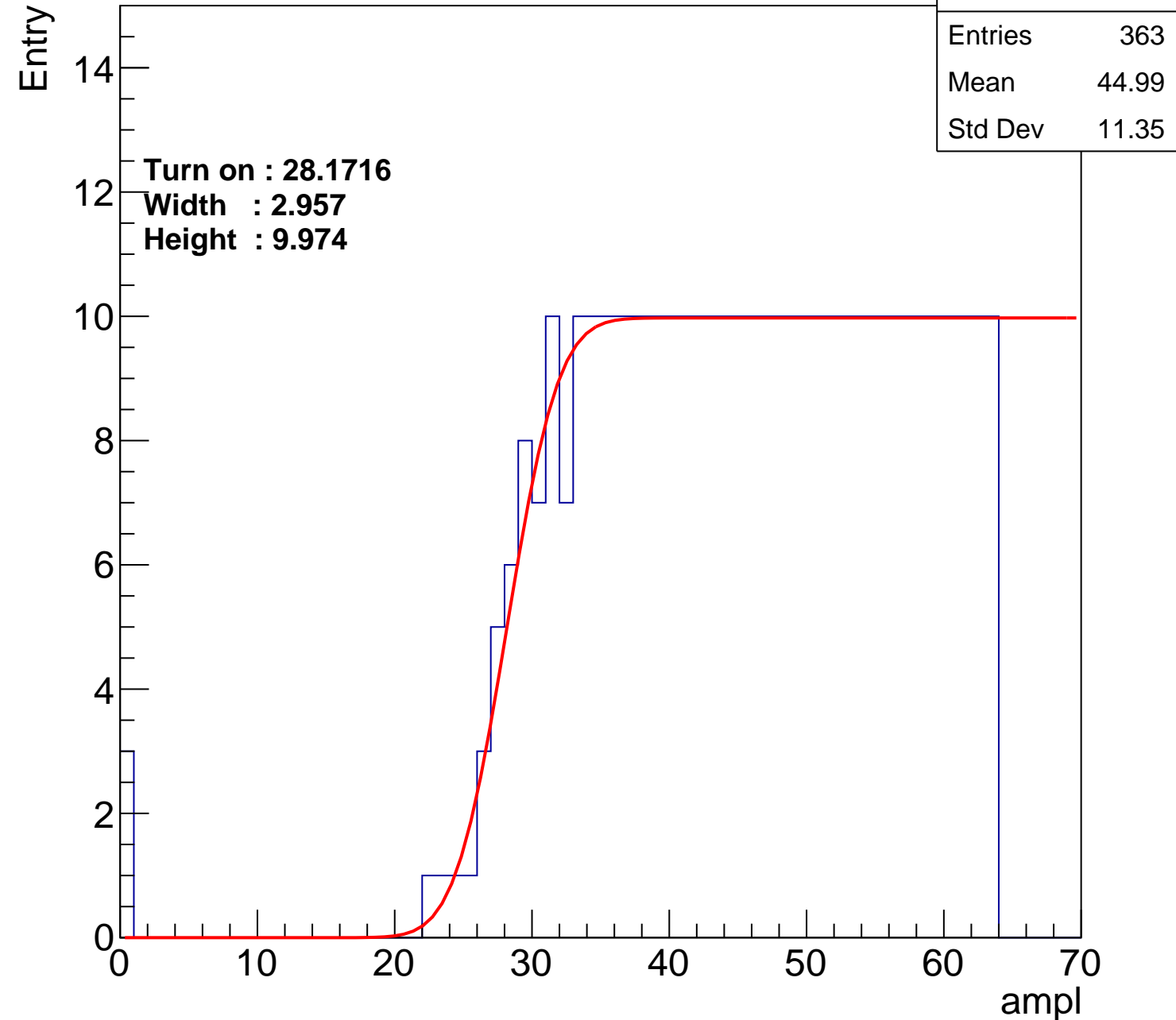
Width : 2.957

Height : 9.974

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch69

calib_packv5_042523_0143.root, FC#8, port C1

Entries	355
Mean	45.39
Std Dev	11.15

Turn on : 29.1710

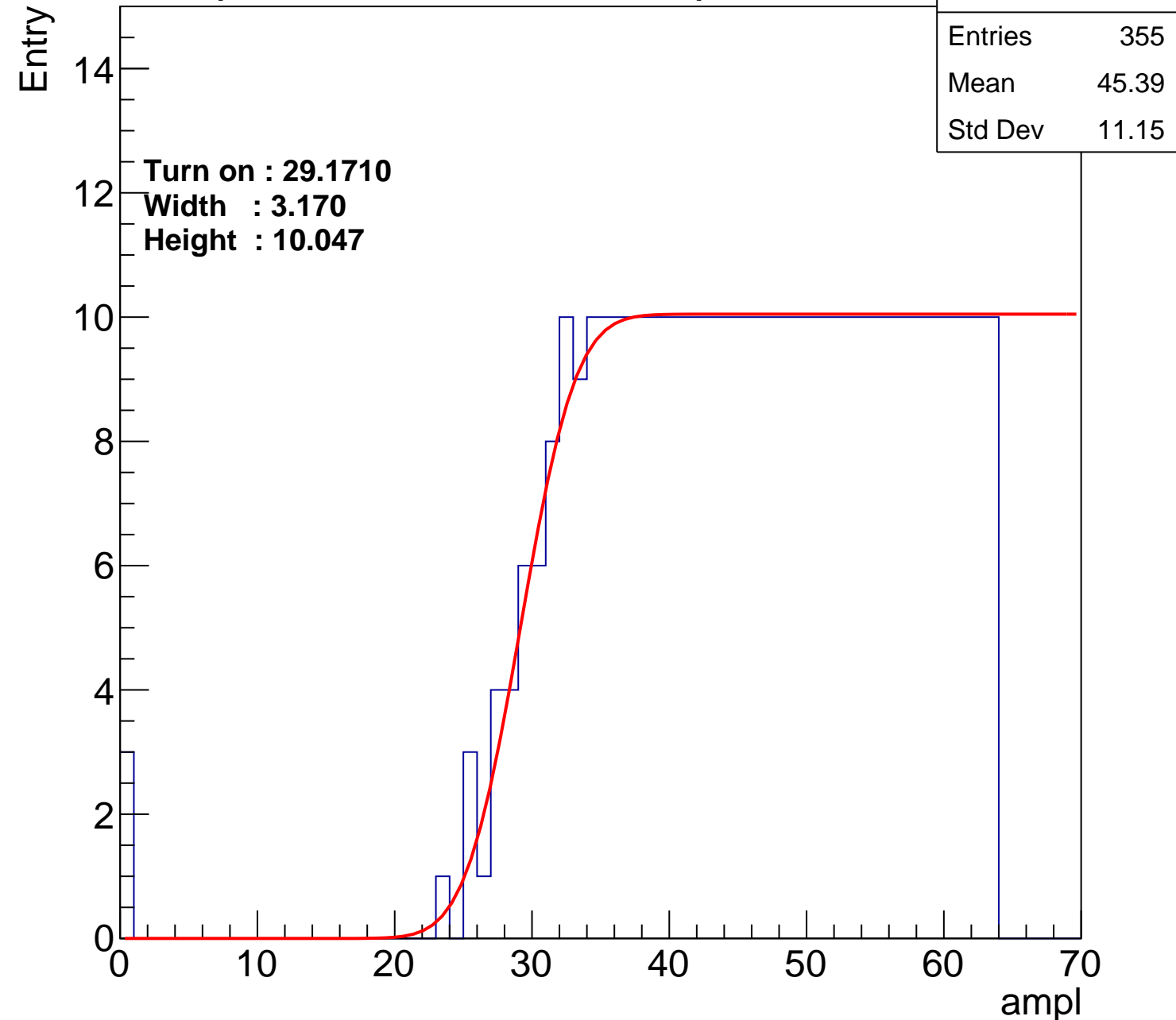
Width : 3.170

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch70

calib_packv5_042523_0143.root, FC#8, port C1

Entries	364
Mean	44.94
Std Dev	11.38

Turn on : 28.4305

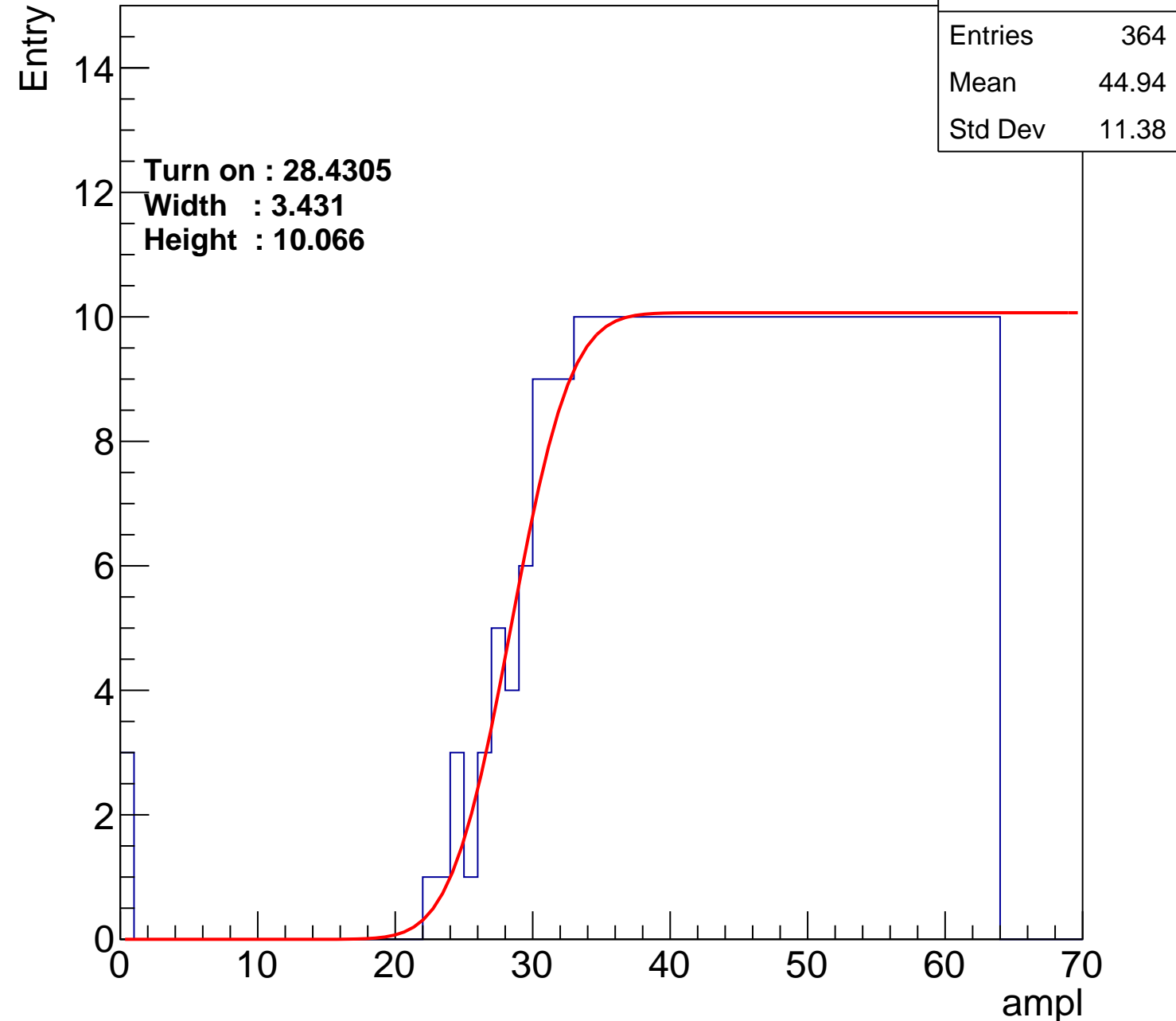
Width : 3.431

Height : 10.066

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch71

calib_packv5_042523_0143.root, FC#8, port C1

Entries	363
Mean	45.11
Std Dev	11.06

Turn on : 27.6980

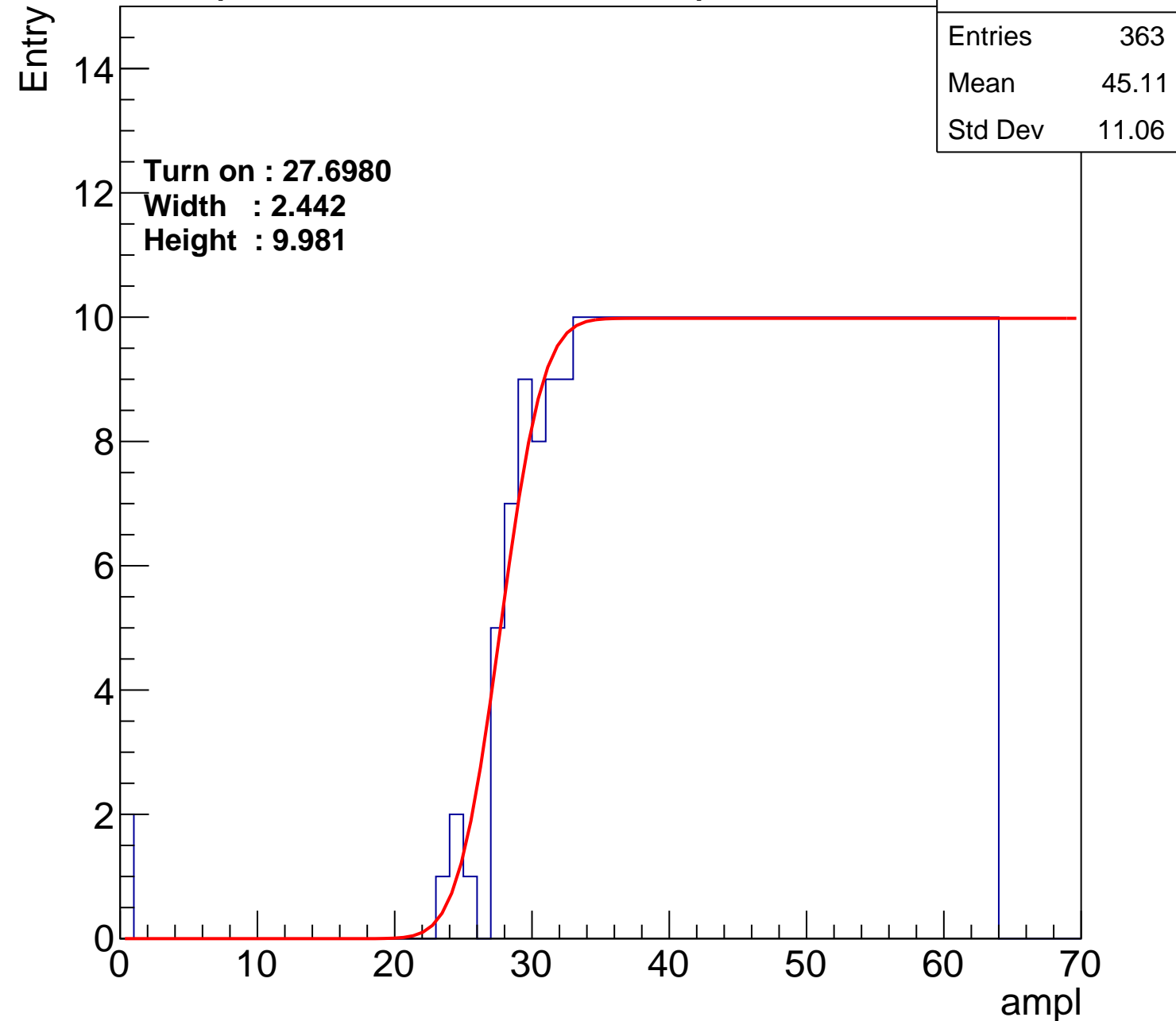
Width : 2.442

Height : 9.981

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch72

calib_packv5_042523_0143.root, FC#8, port C1

Entries	372
Mean	44.72
Std Dev	11.13

Turn on : 27.7173

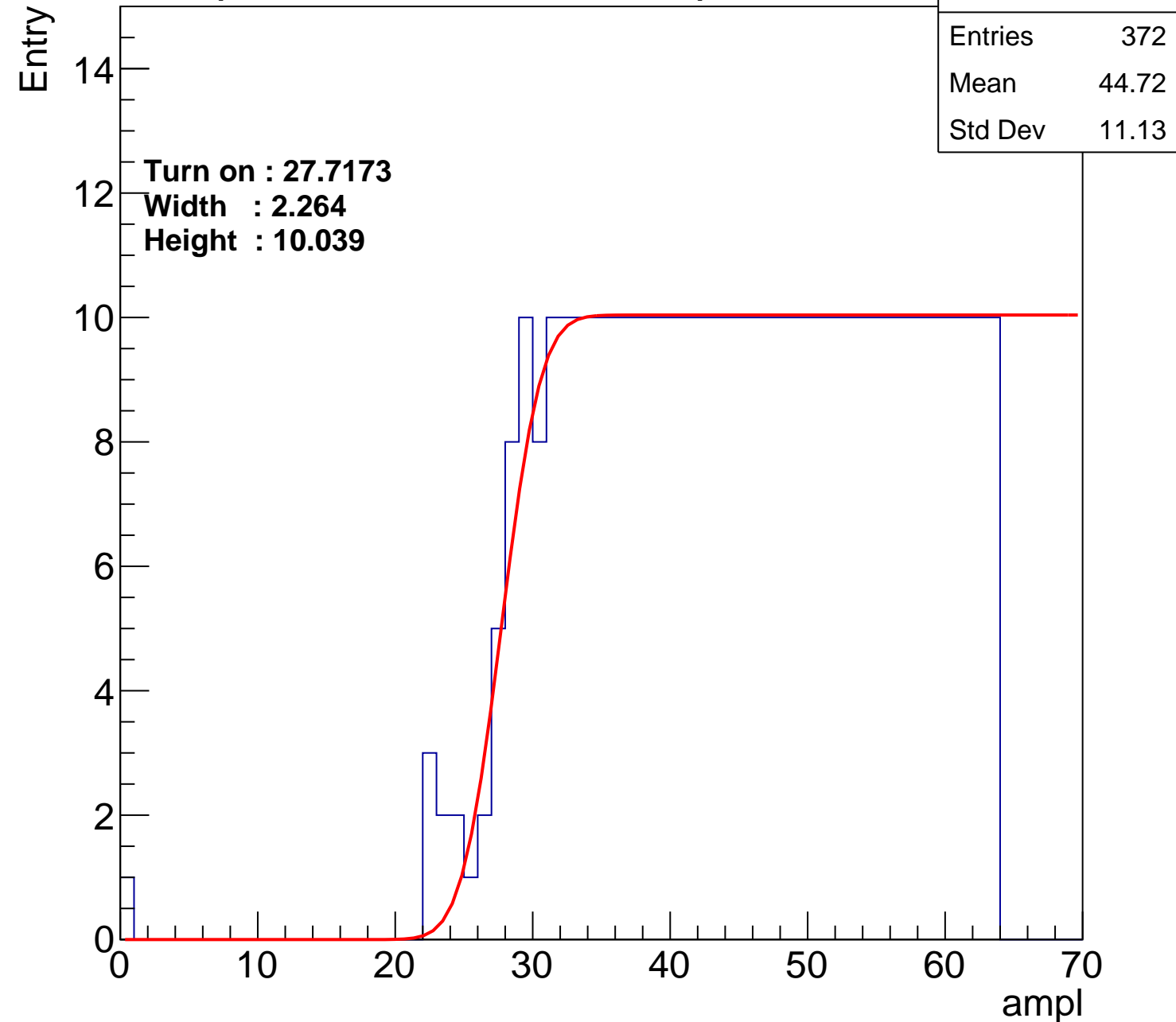
Width : 2.264

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch73

calib_packv5_042523_0143.root, FC#8, port C1

Entries	362
Mean	45.09
Std Dev	11.15

Turn on : 28.2644

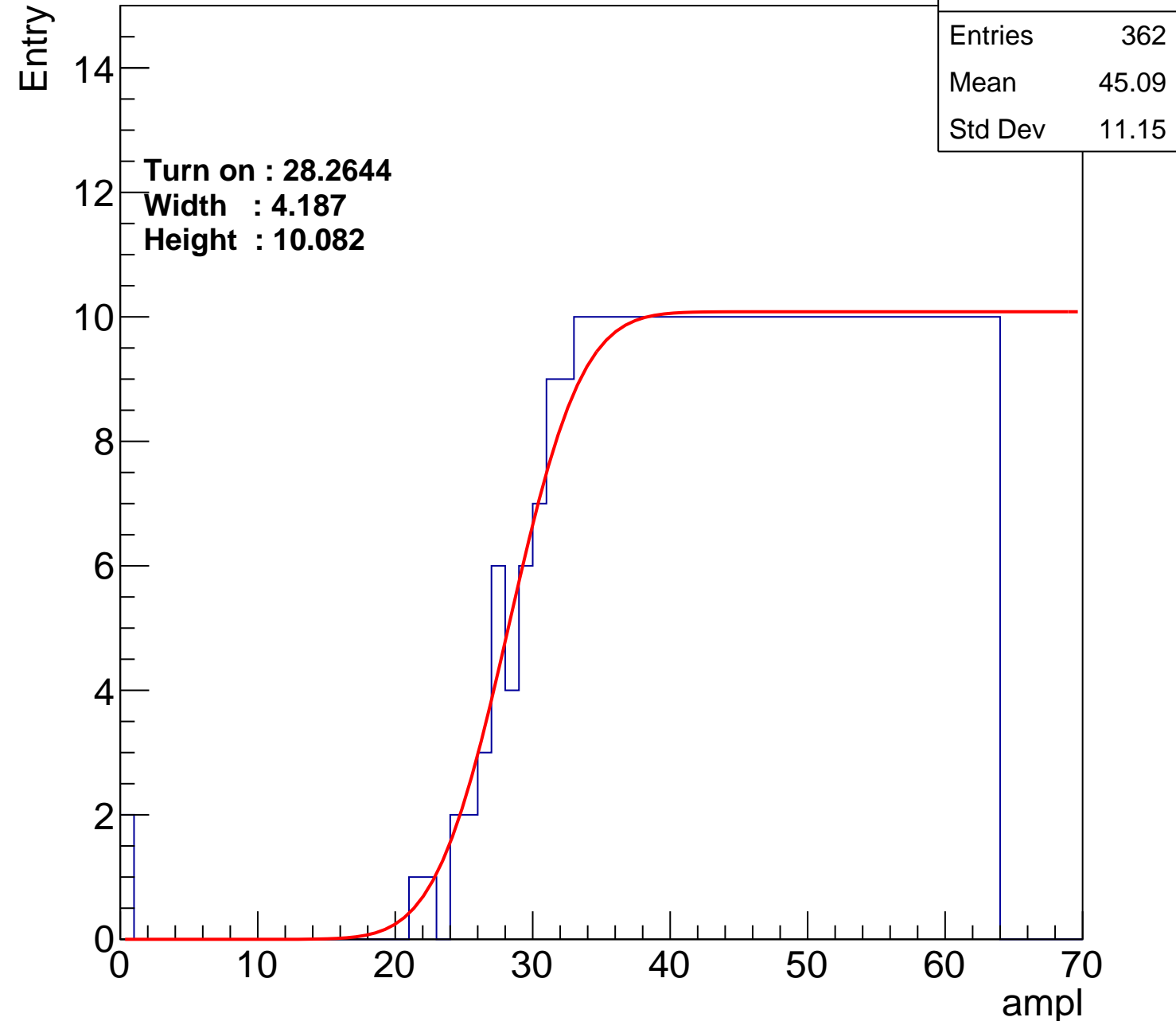
Width : 4.187

Height : 10.082

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch74

calib_packv5_042523_0143.root, FC#8, port C1

Entries	375
Mean	44.6
Std Dev	11.15

Turn on : 26.7478

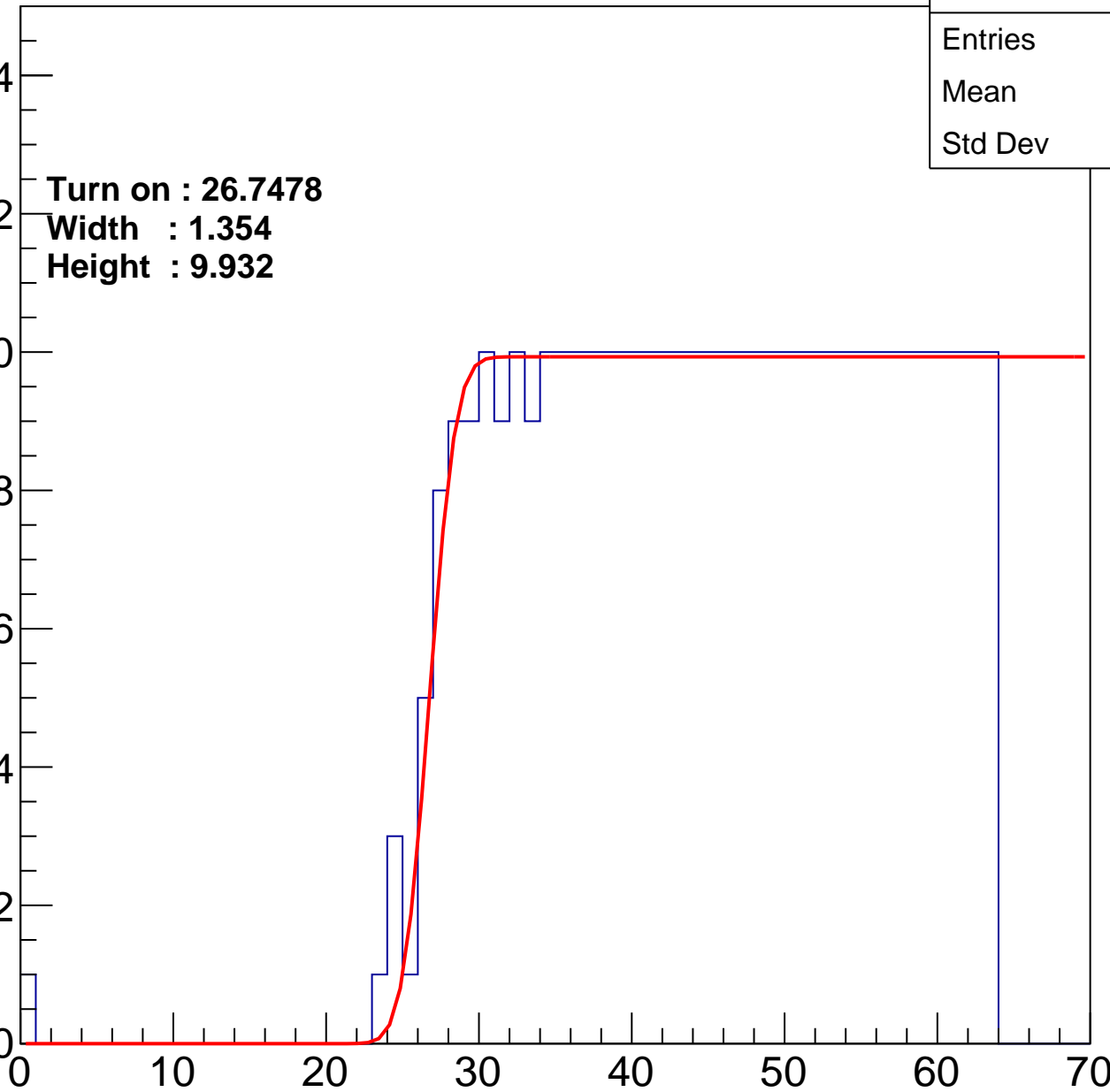
Width : 1.354

Height : 9.932

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch75

calib_packv5_042523_0143.root, FC#8, port C1

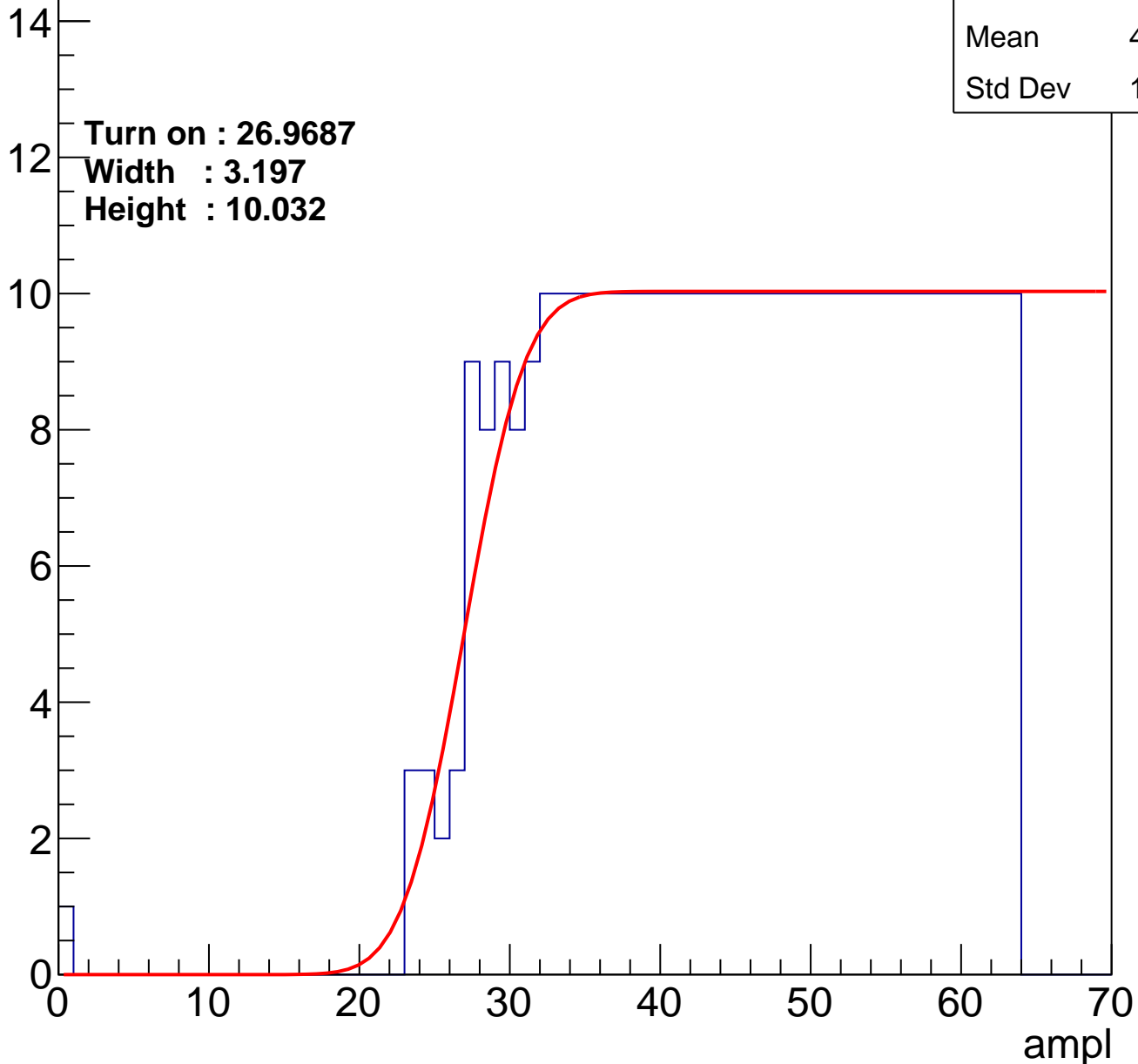
Entries	375
Mean	44.58
Std Dev	11.19

Turn on : 26.9687

Width : 3.197

Height : 10.032

Entry



B0L002S, U7-ch76

calib_packv5_042523_0143.root, FC#8, port C1

Entries	379
Mean	44.34
Std Dev	11.44

Turn on : 25.9558

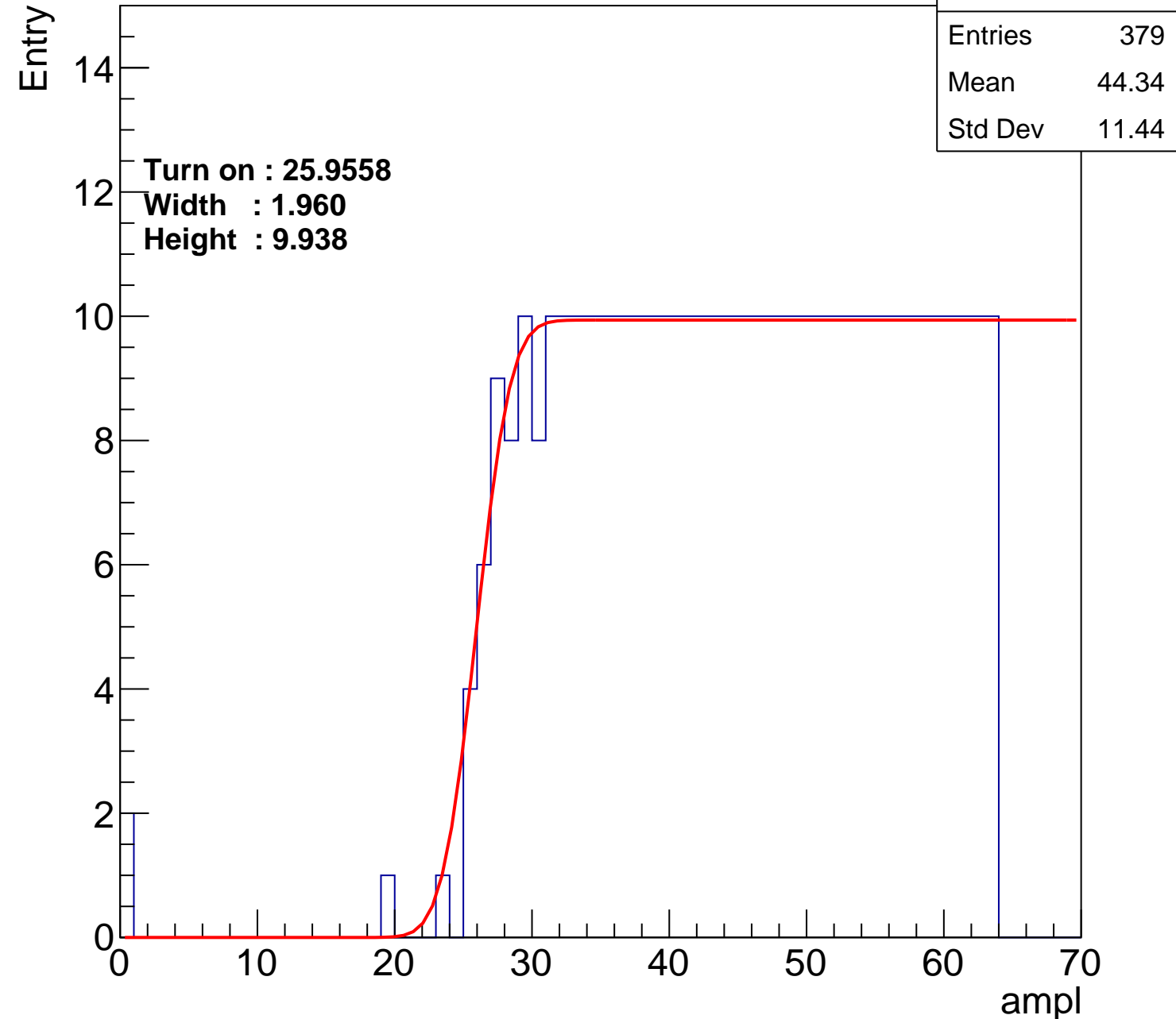
Width : 1.960

Height : 9.938

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch77

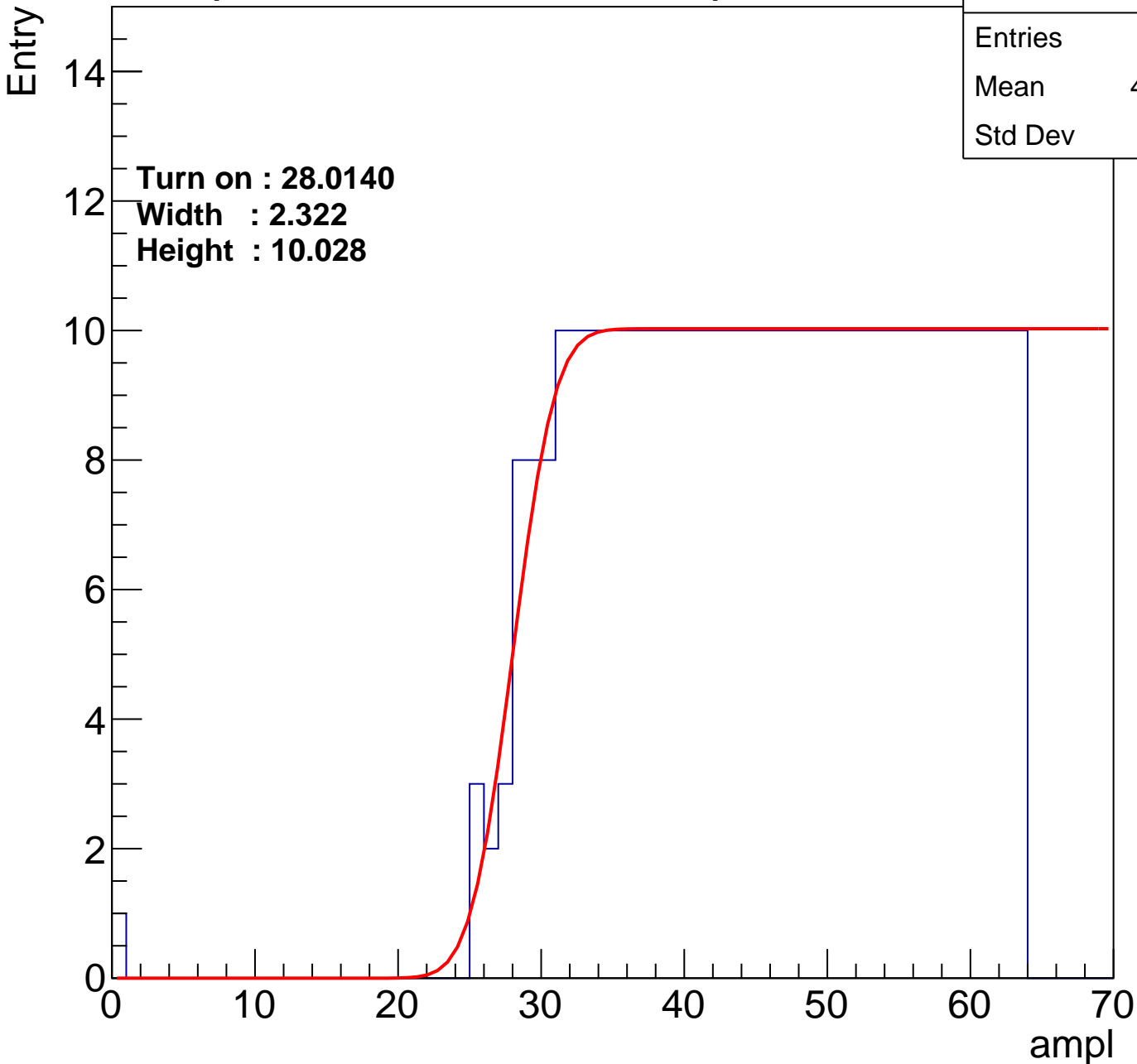
calib_packv5_042523_0143.root, FC#8, port C1

Turn on : 28.0140

Width : 2.322

Height : 10.028

Entries	363
Mean	45.22
Std Dev	10.8



B0L002S, U7-ch78

calib_packv5_042523_0143.root, FC#8, port C1

Entries	382
Mean	44.2
Std Dev	11.51

Turn on : 26.0681

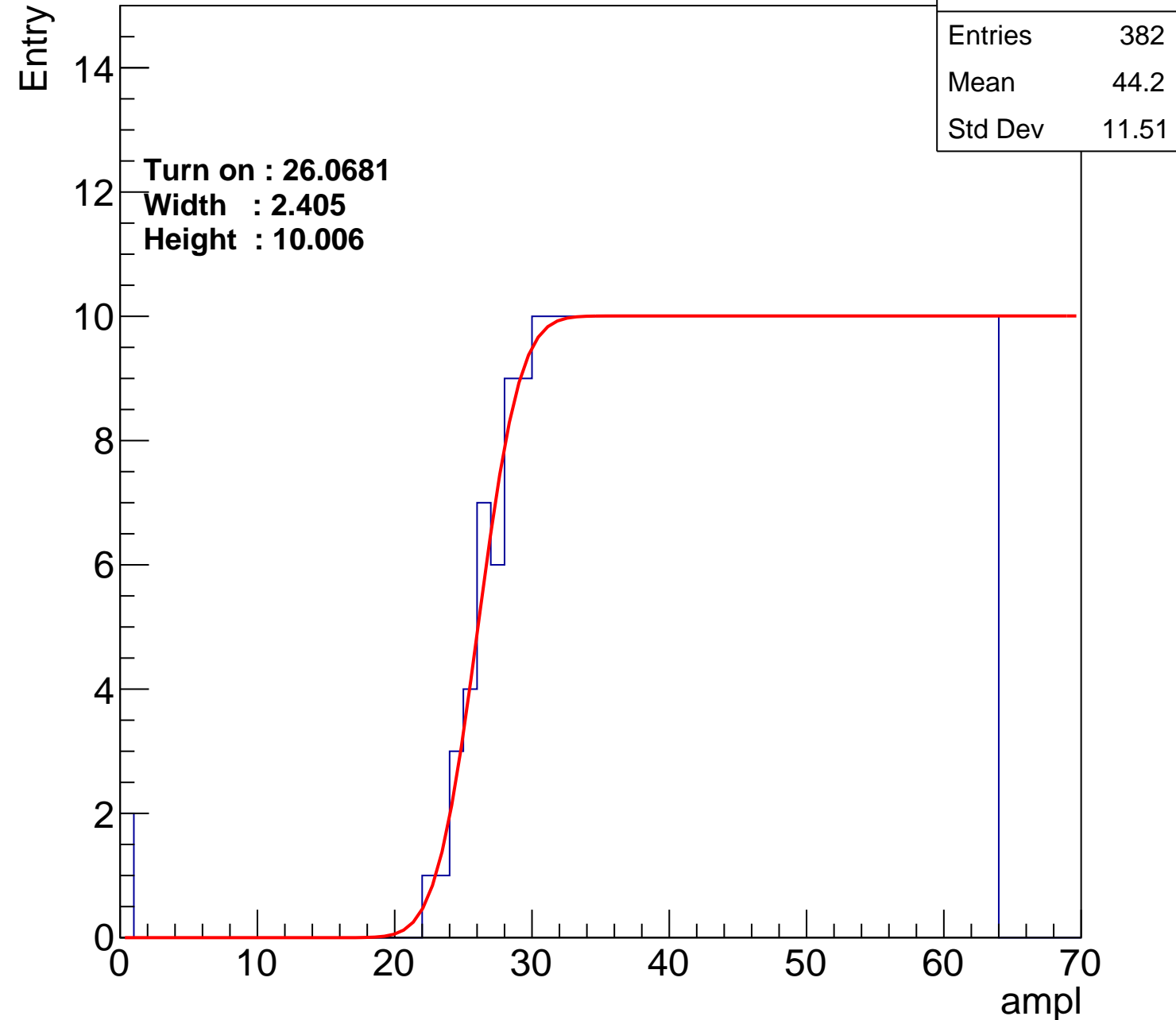
Width : 2.405

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch79

calib_packv5_042523_0143.root, FC#8, port C1

Entries	365
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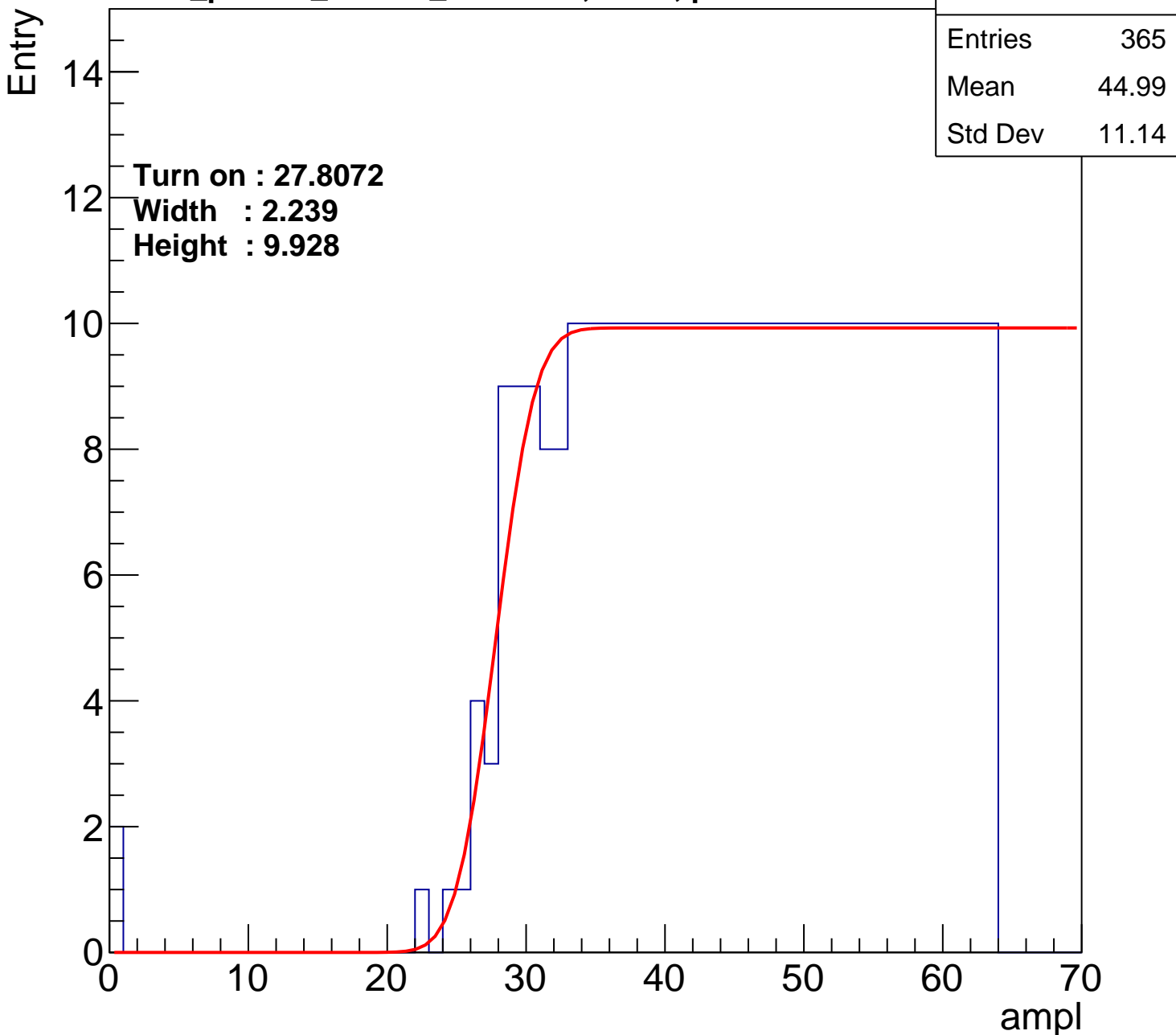
Mean	44.99
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Std Dev	11.14
---------	-------

Turn on : 27.8072

Width : 2.239

Height : 9.928



B0L002S, U7-ch80

calib_packv5_042523_0143.root, FC#8, port C1

Entries	374
Mean	44.58
Std Dev	11.32

Turn on : 26.7579

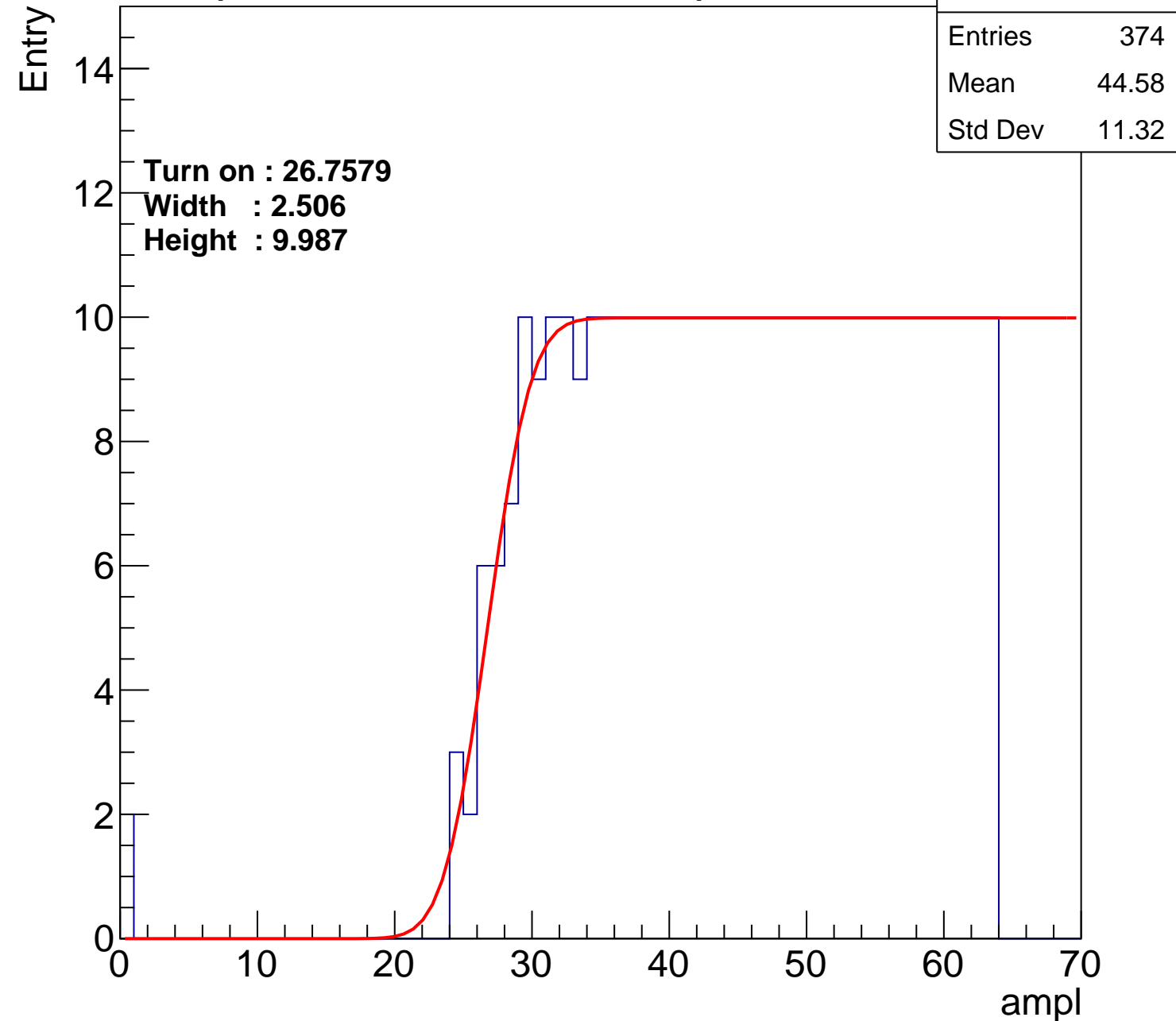
Width : 2.506

Height : 9.987

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch81

calib_packv5_042523_0143.root, FC#8, port C1

Entries	383
Mean	44.05
Std Dev	11.7

Turn on : 25.9564

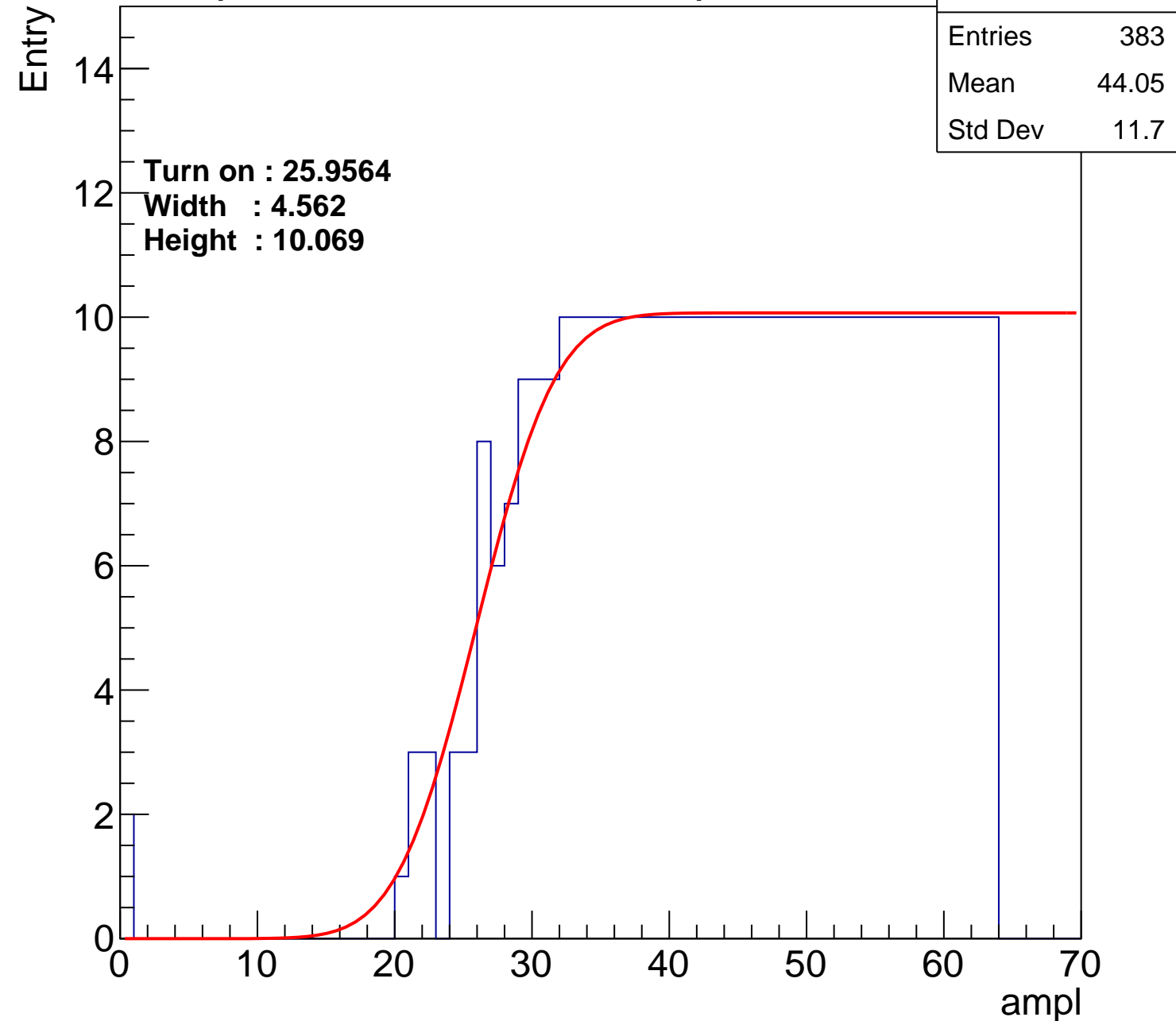
Width : 4.562

Height : 10.069

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch82

calib_packv5_042523_0143.root, FC#8, port C1

Entries	362
Mean	45.27
Std Dev	10.77

Turn on : 28.1369

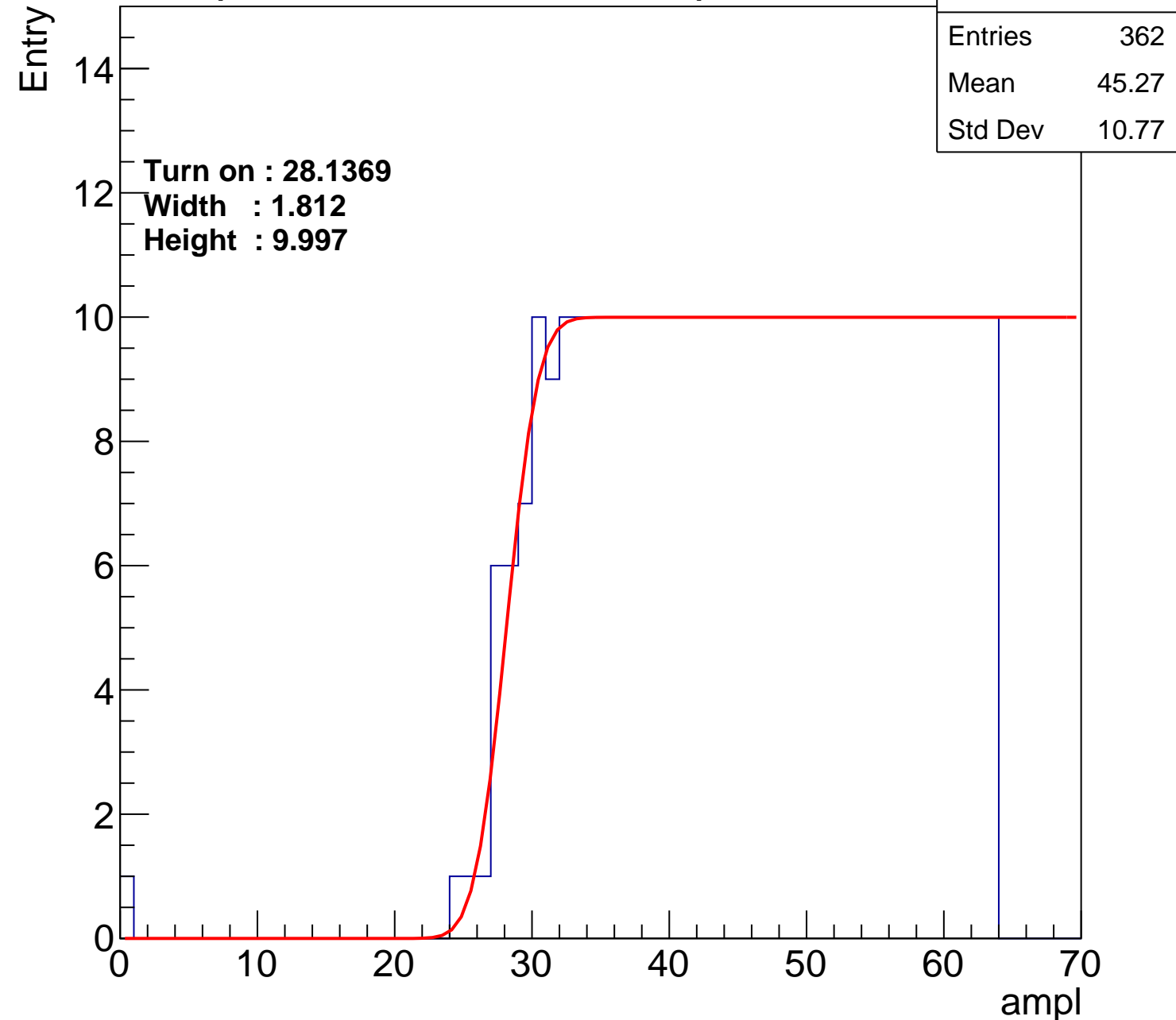
Width : 1.812

Height : 9.997

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch83

calib_packv5_042523_0143.root, FC#8, port C1

Entries	362
Mean	45.17
Std Dev	11.02

Turn on : 28.0106

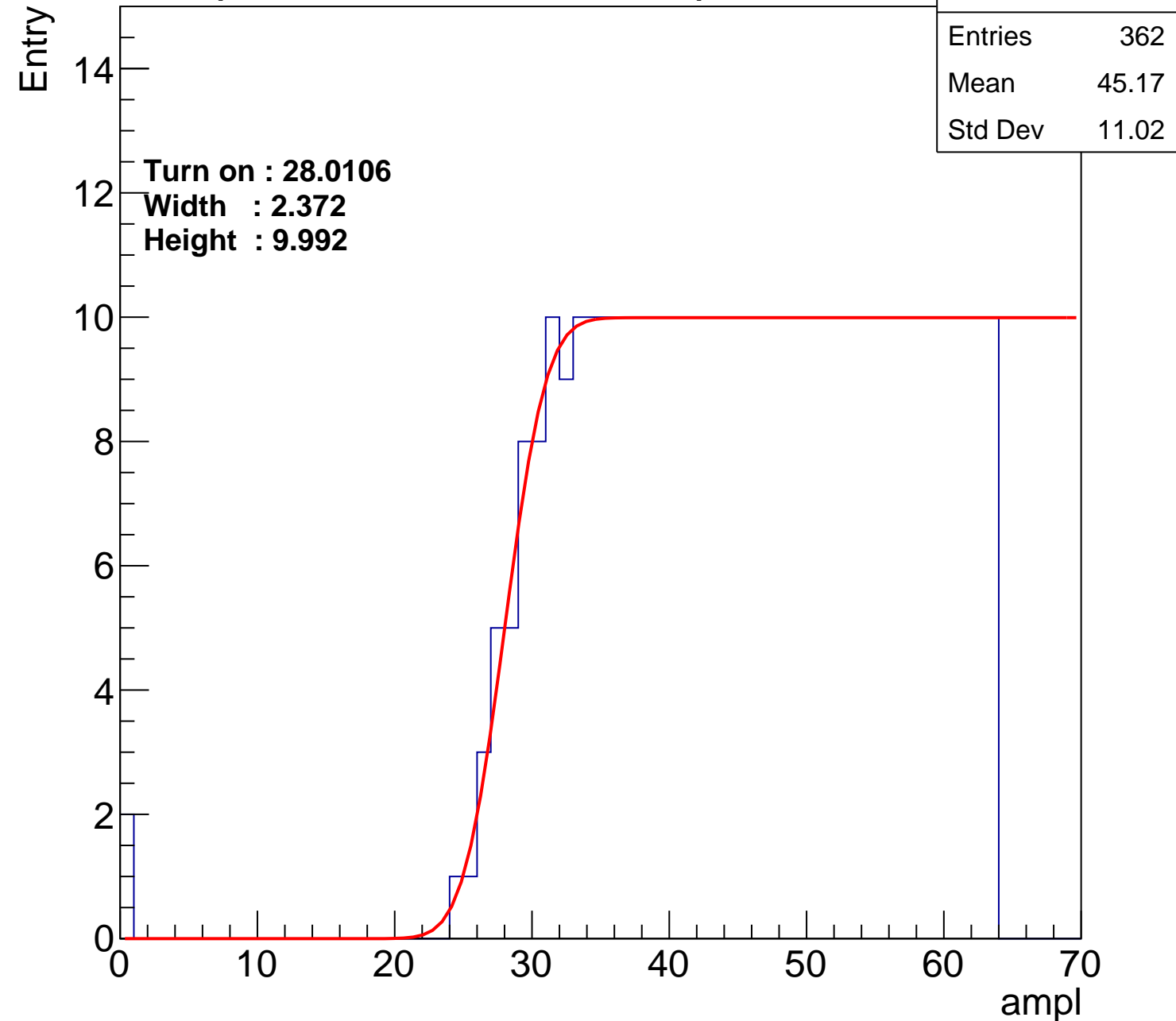
Width : 2.372

Height : 9.992

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch84

calib_packv5_042523_0143.root, FC#8, port C1

Entries	354
Mean	45.63
Std Dev	10.6

Turn on : 28.5849

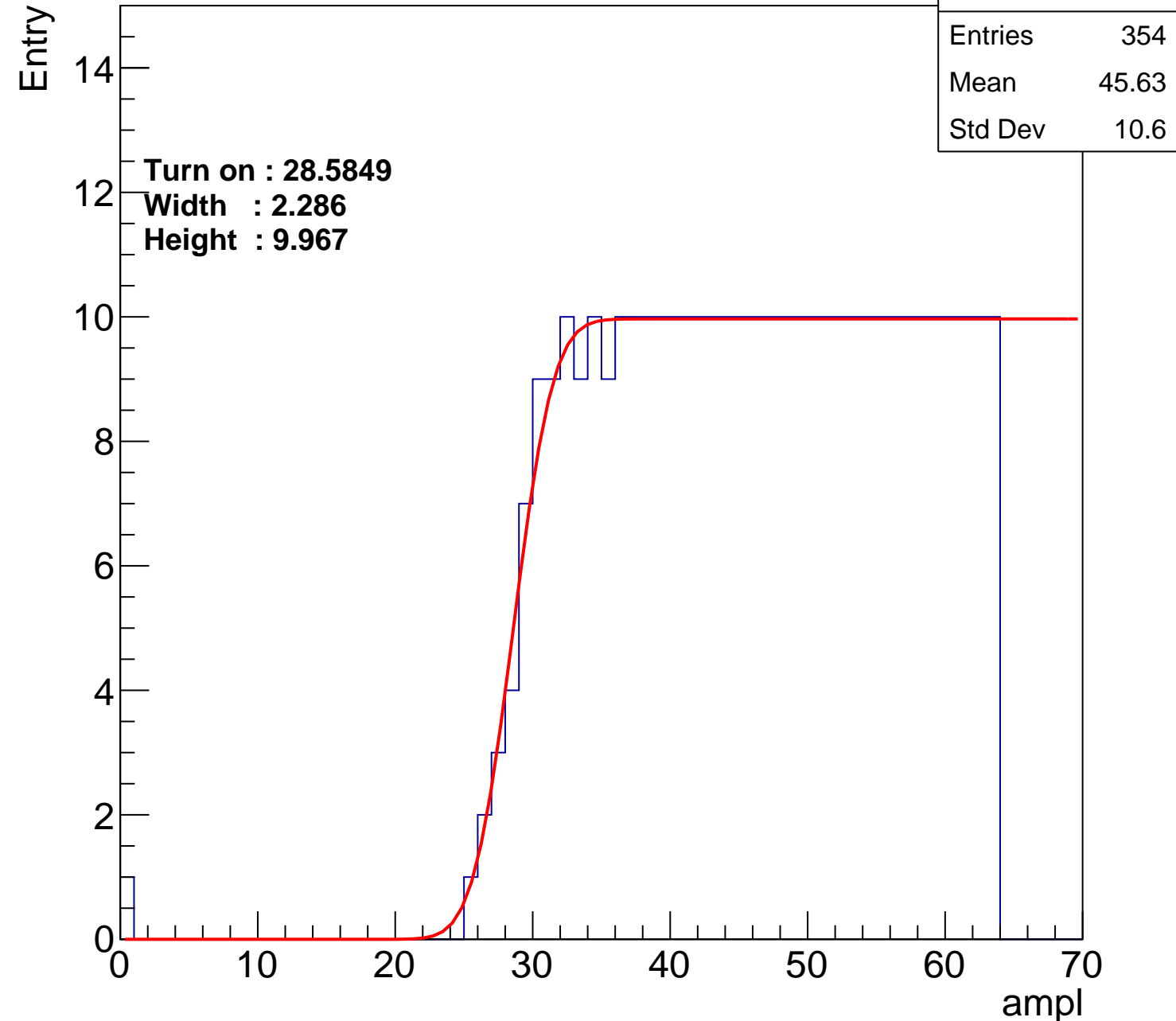
Width : 2.286

Height : 9.967

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch85

calib_packv5_042523_0143.root, FC#8, port C1

Entries	378
Mean	44.26
Std Dev	11.78

Turn on : 26.6107

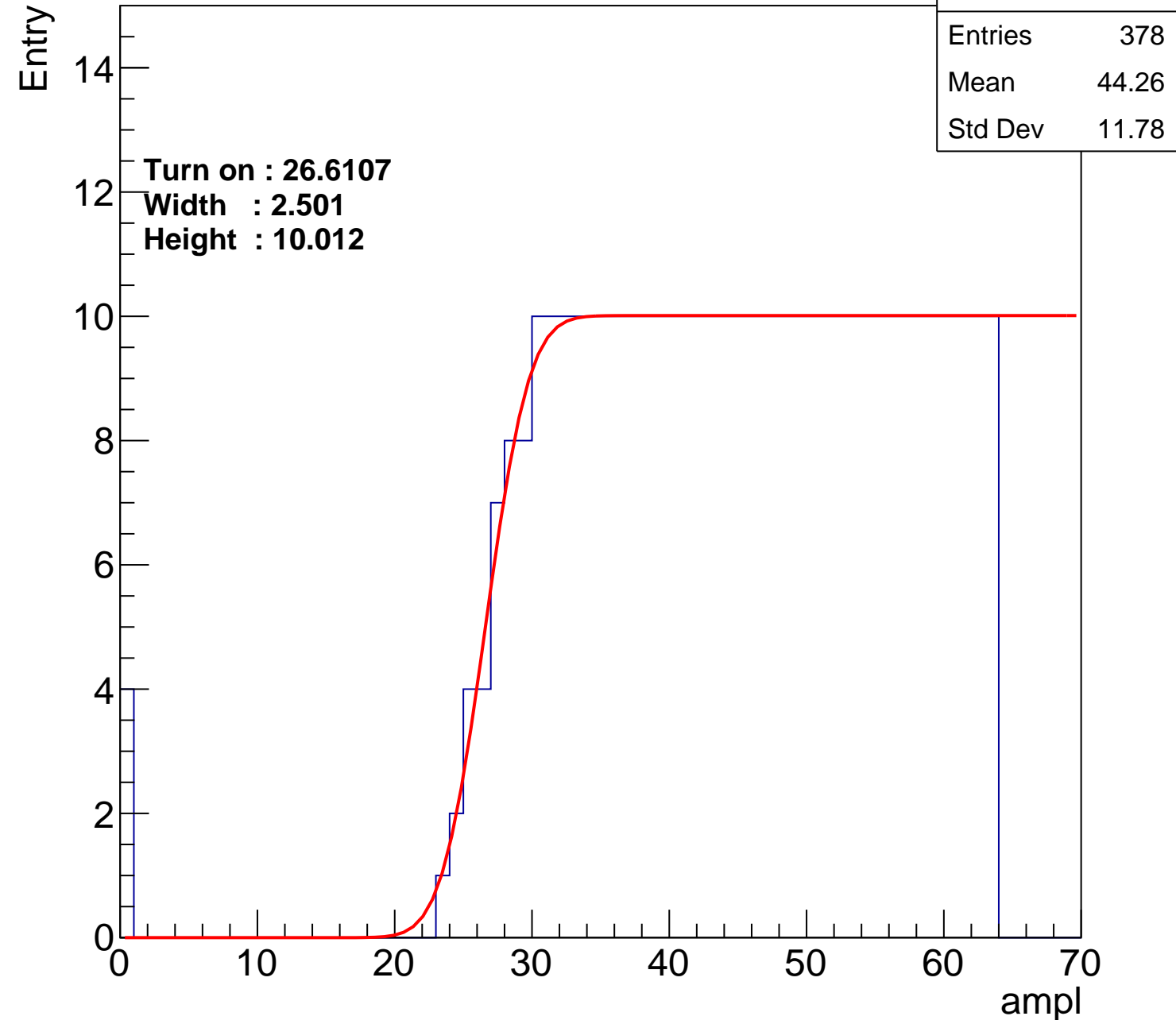
Width : 2.501

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch86

calib_packv5_042523_0143.root, FC#8, port C1

Entries	384
Mean	44.13
Std Dev	11.44

Turn on : 25.6584

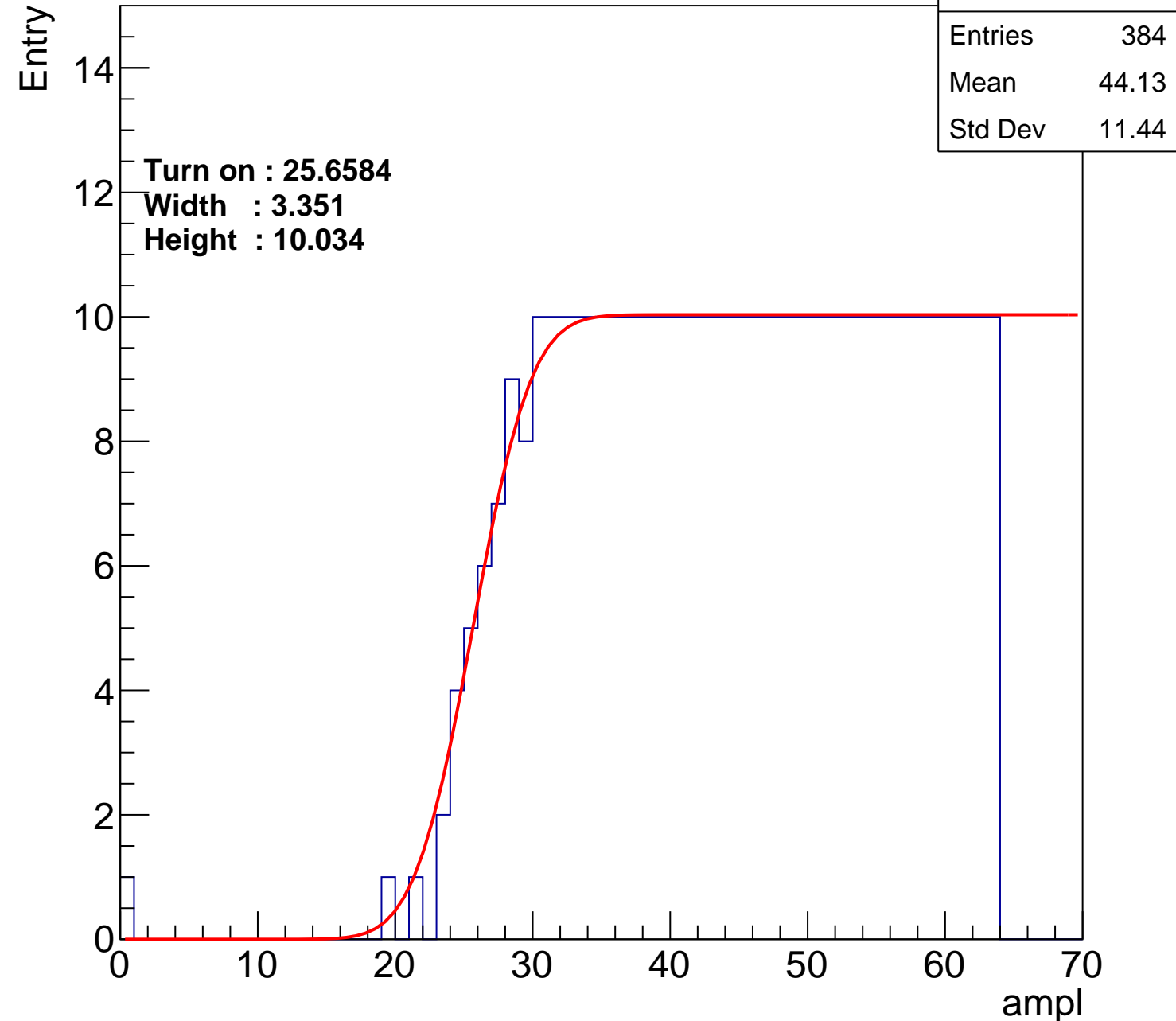
Width : 3.351

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch87

calib_packv5_042523_0143.root, FC#8, port C1

Entries	377
Mean	44.35
Std Dev	11.61

Turn on : 26.8605

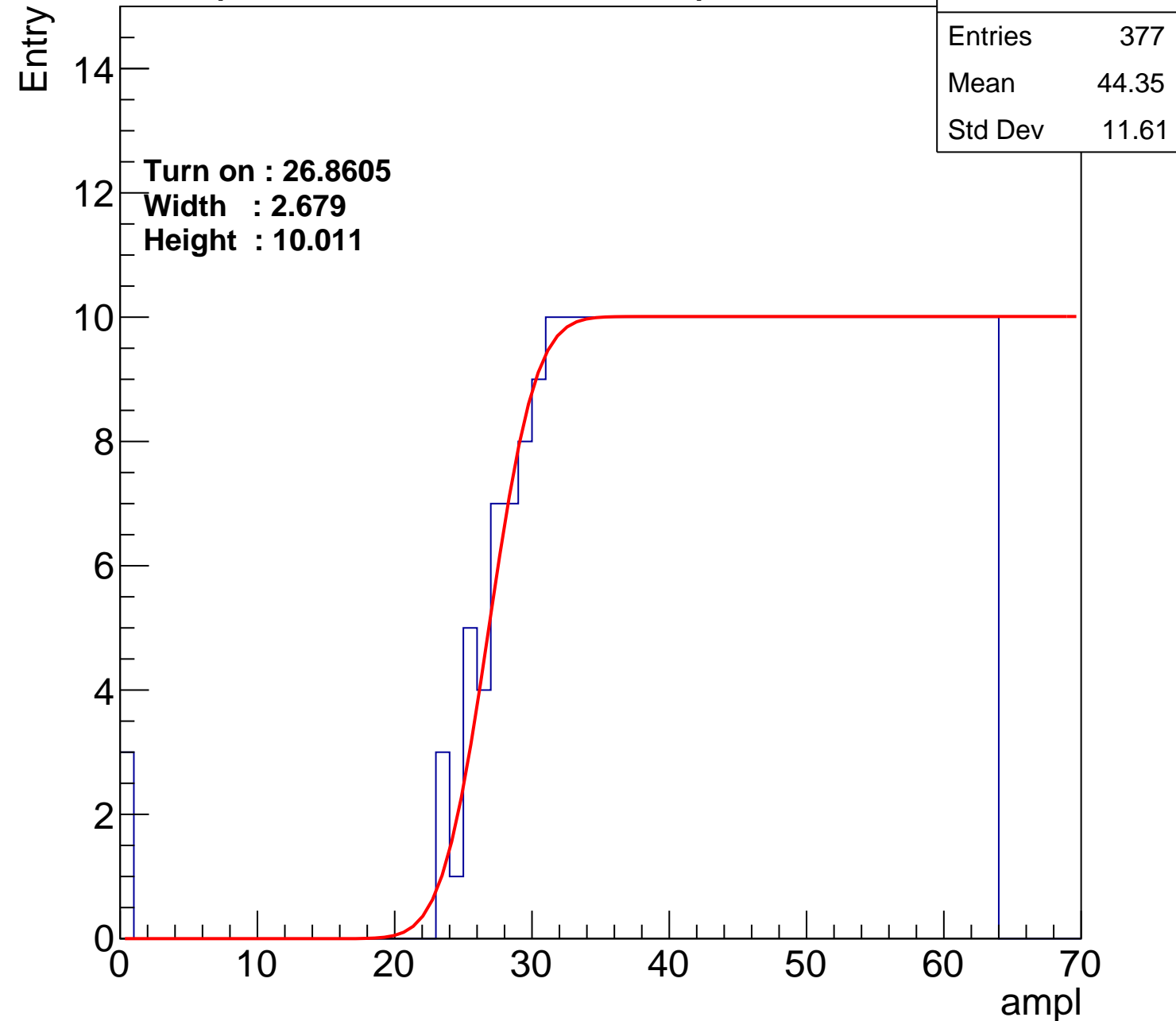
Width : 2.679

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch88

calib_packv5_042523_0143.root, FC#8, port C1

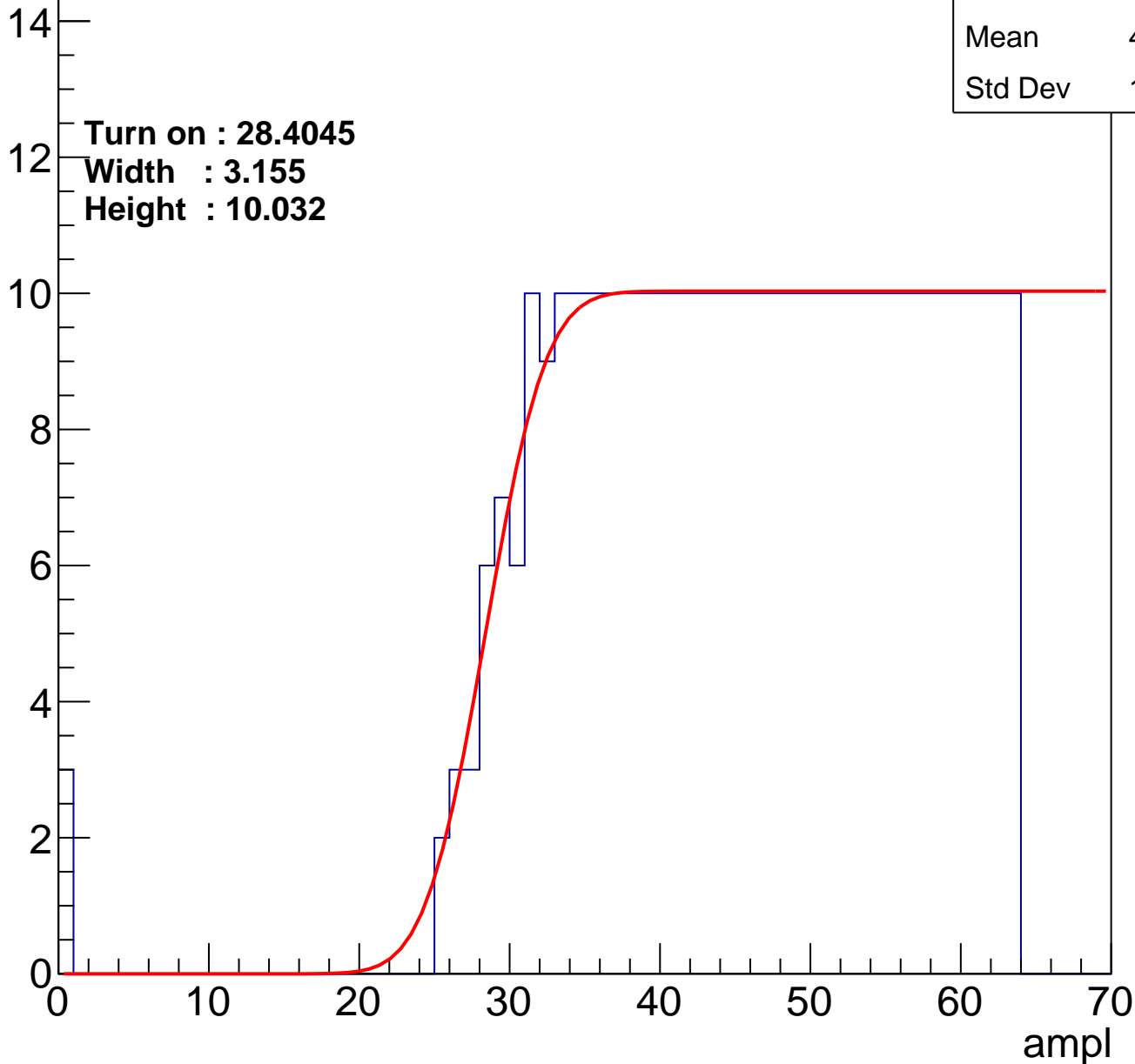
Entry

Entries	359
Mean	45.23
Std Dev	11.18

Turn on : 28.4045

Width : 3.155

Height : 10.032



B0L002S, U7-ch89

calib_packv5_042523_0143.root, FC#8, port C1

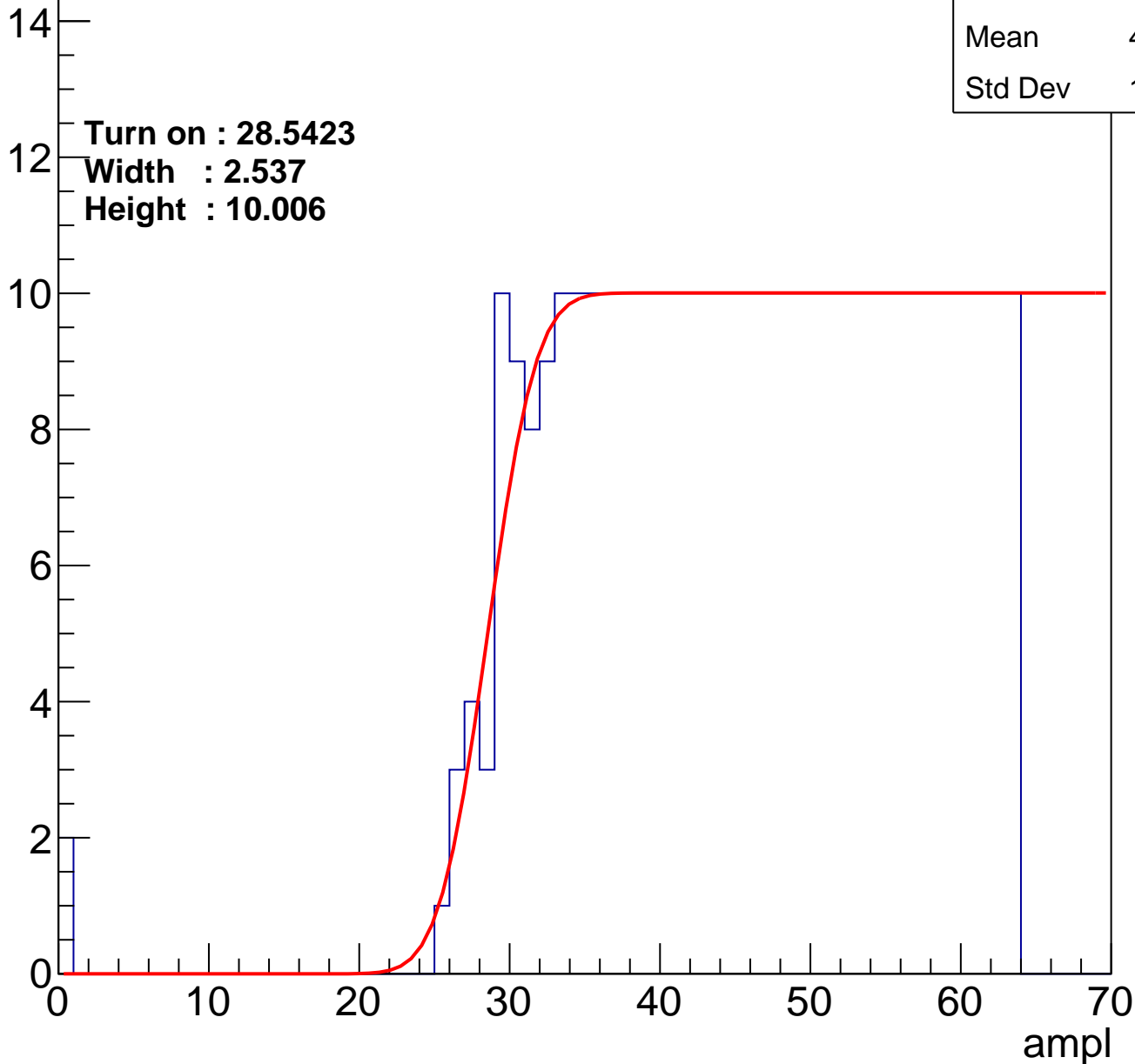
Entry

Entries	359
Mean	45.32
Std Dev	10.93

Turn on : 28.5423

Width : 2.537

Height : 10.006



B0L002S, U7-ch90

calib_packv5_042523_0143.root, FC#8, port C1

Entries	374
Mean	44.55
Std Dev	11.38

Turn on : 27.4083

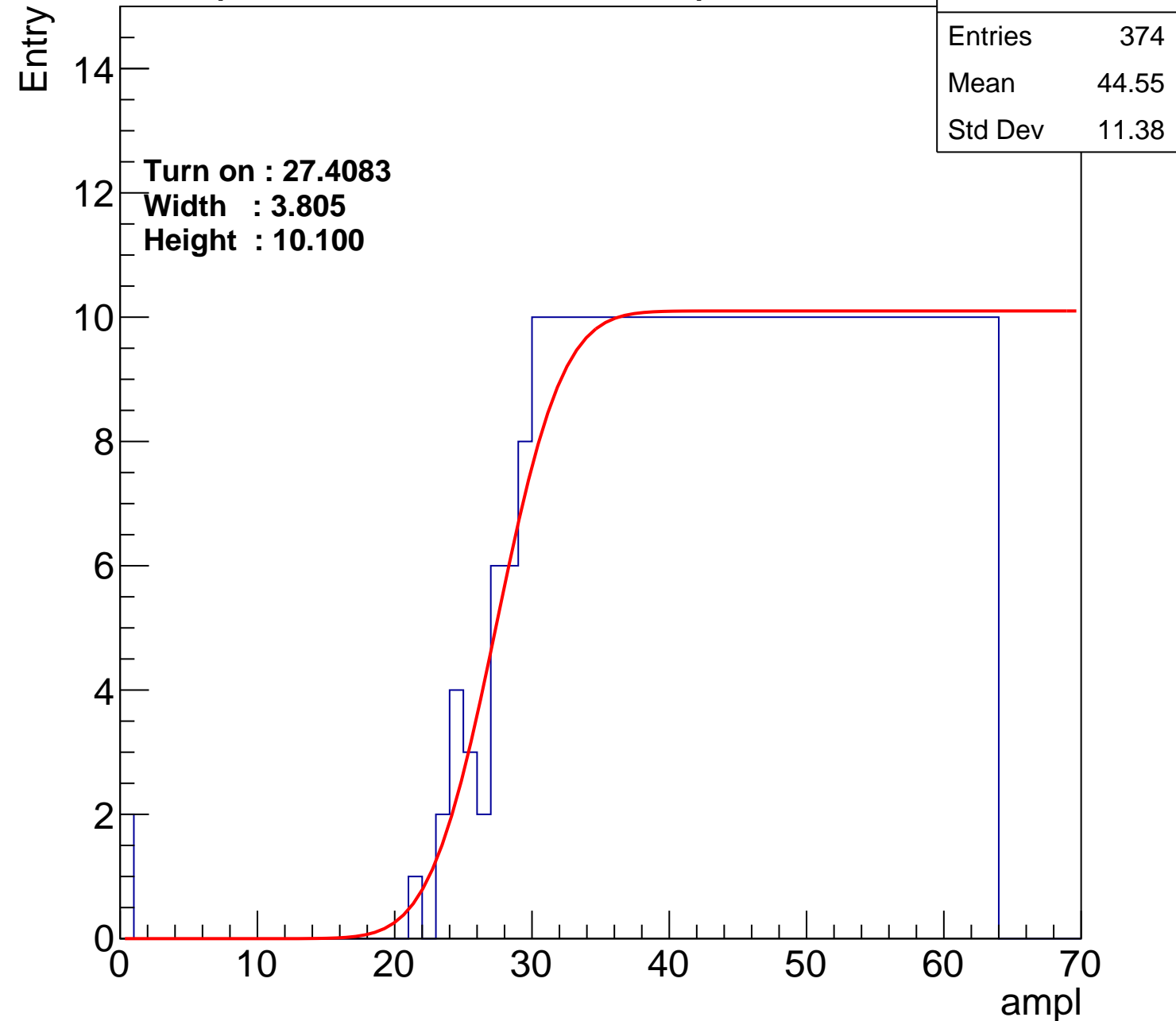
Width : 3.805

Height : 10.100

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch91

calib_packv5_042523_0143.root, FC#8, port C1

Entries	354
Mean	45.49
Std Dev	11.04

Turn on : 29.5607

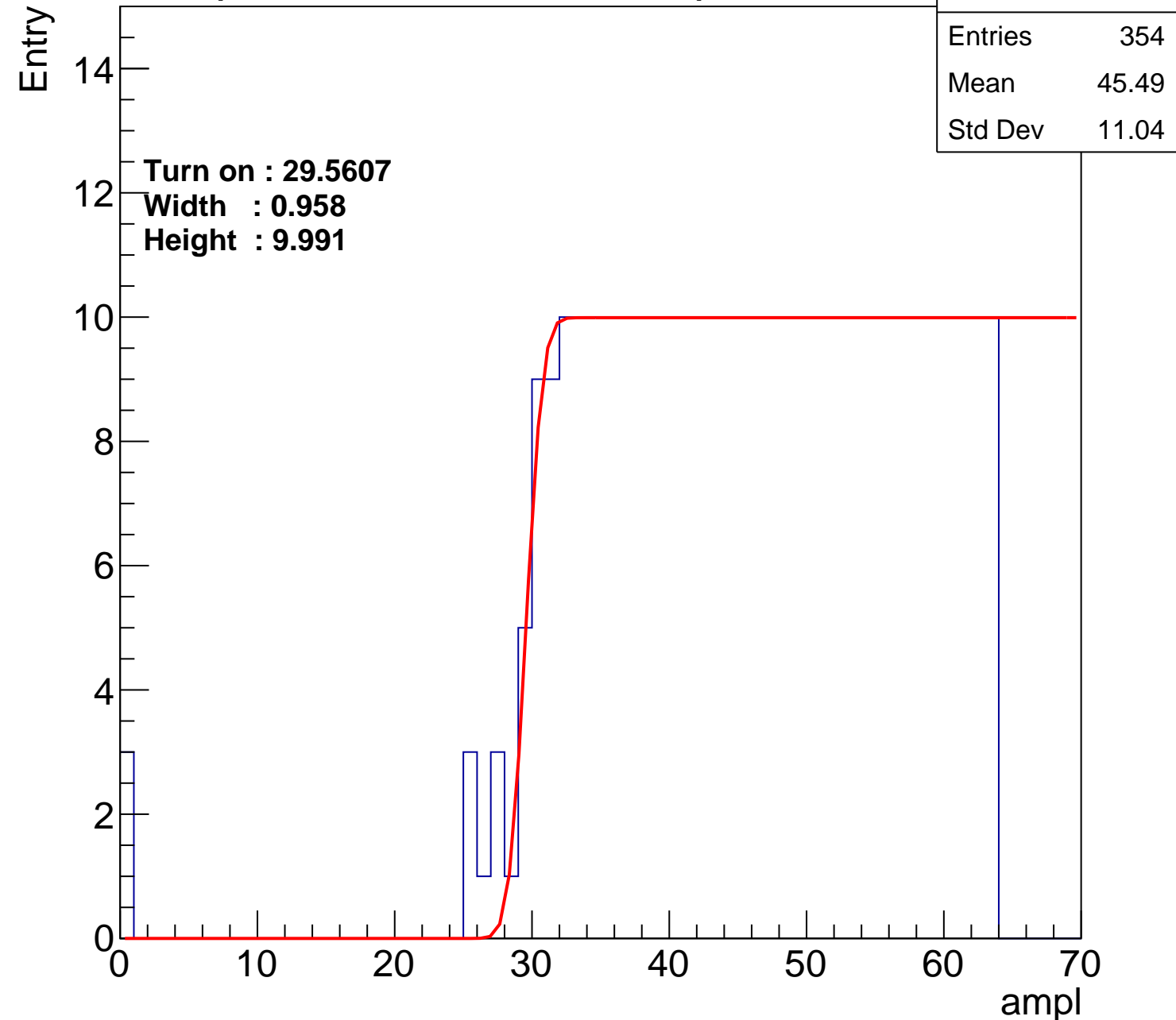
Width : 0.958

Height : 9.991

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch92

calib_packv5_042523_0143.root, FC#8, port C1

Entries	355
Mean	45.51
Std Dev	10.85

Turn on : 29.2183

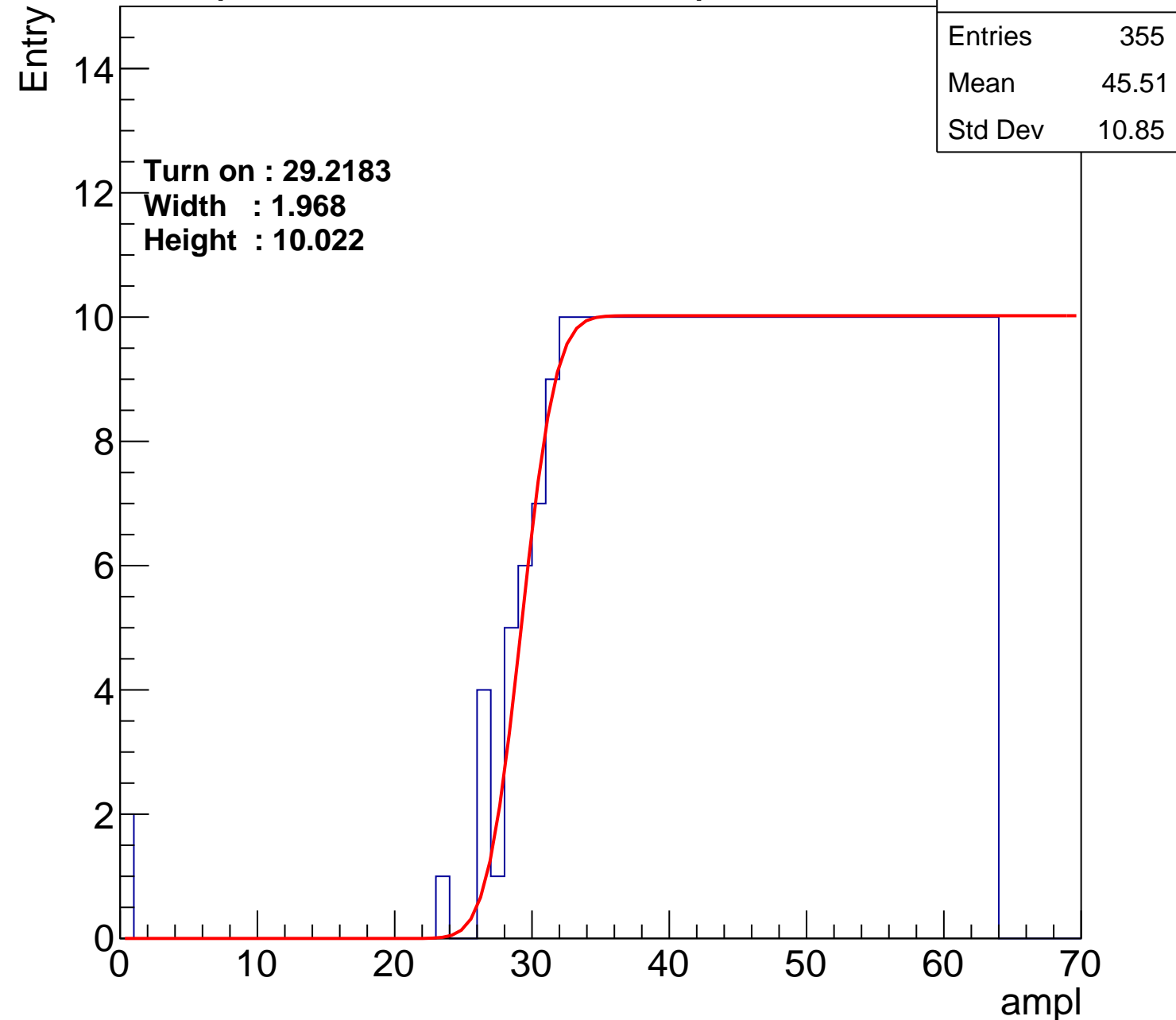
Width : 1.968

Height : 10.022

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch93

calib_packv5_042523_0143.root, FC#8, port C1

Entries	359
Mean	45.18
Std Dev	11.26

Turn on : 29.2109

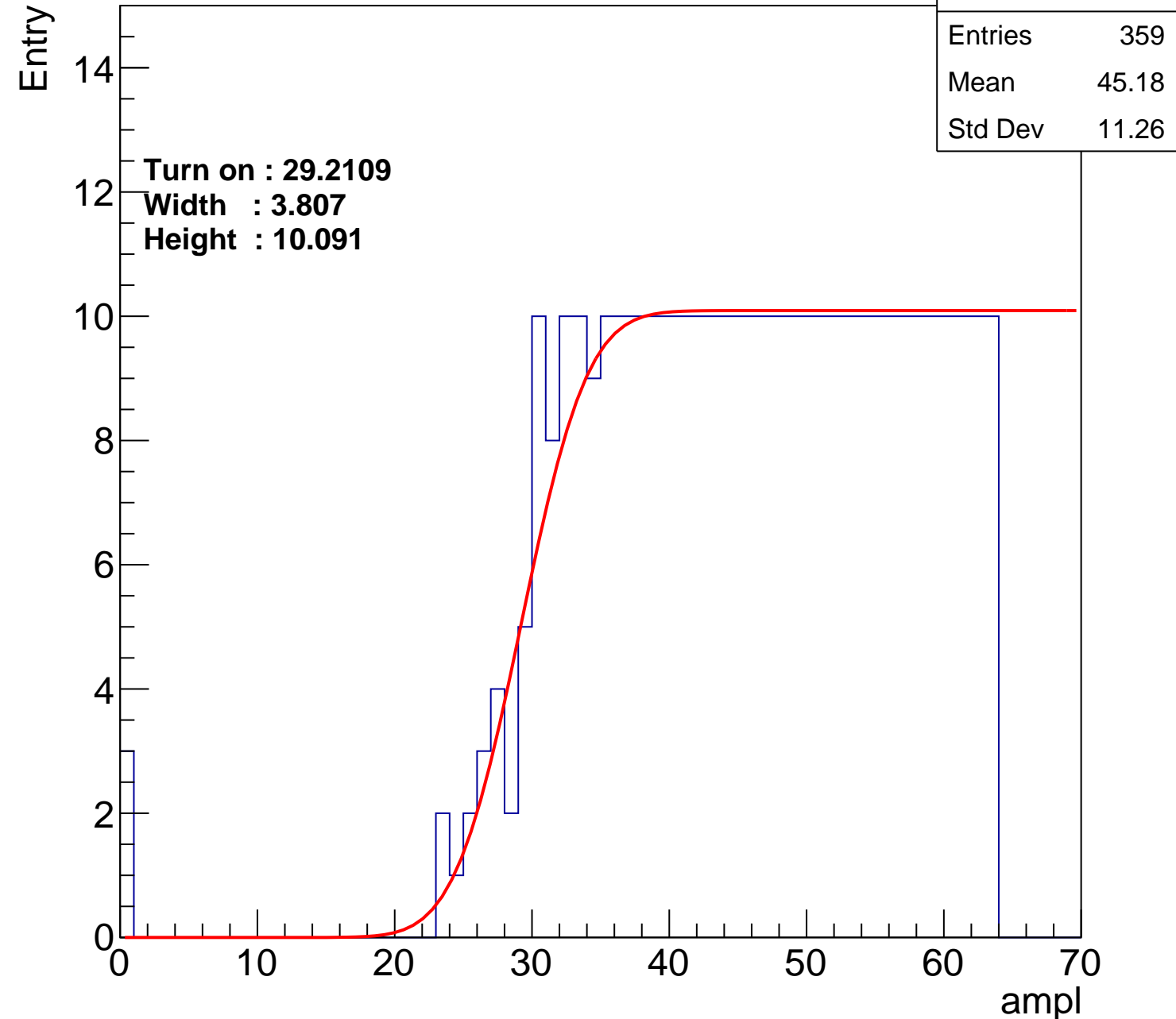
Width : 3.807

Height : 10.091

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch94

calib_packv5_042523_0143.root, FC#8, port C1

Entries	363
Mean	45.03
Std Dev	11.29

Turn on : 28.4345

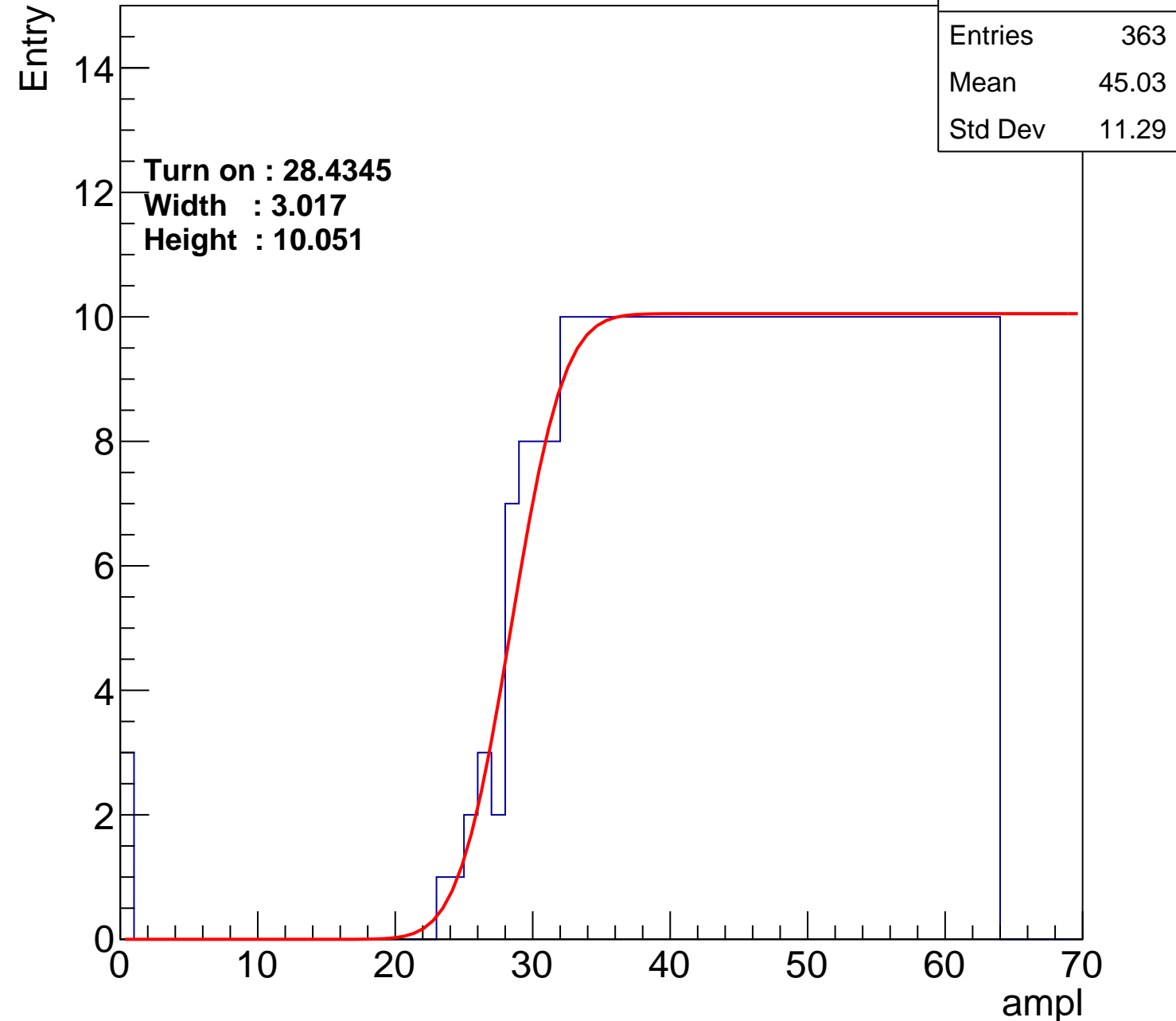
Width : 3.017

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch95

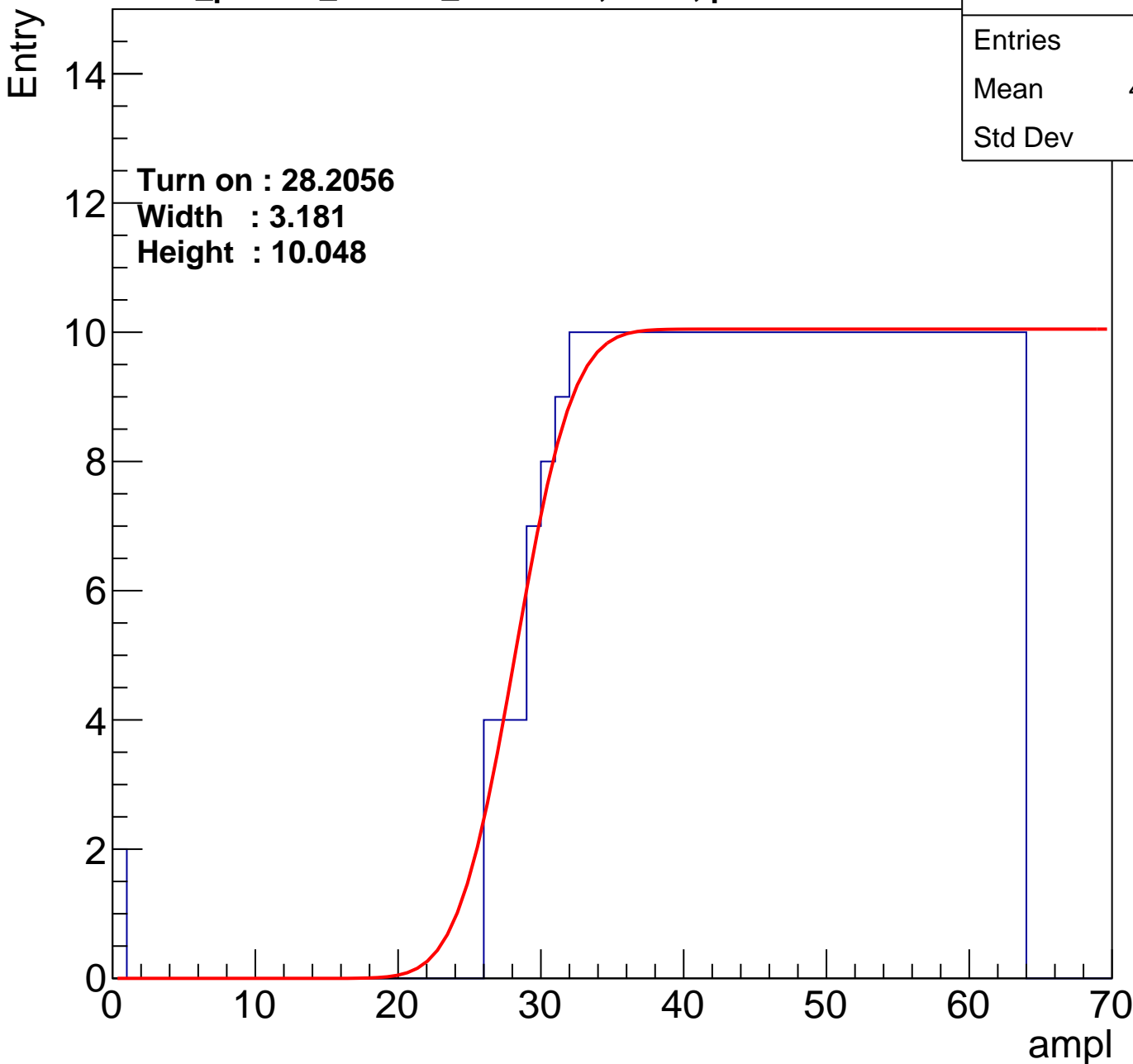
calib_packv5_042523_0143.root, FC#8, port C1

Turn on : 28.2056

Width : 3.181

Height : 10.048

Entries	358
Mean	45.38
Std Dev	10.9



B0L002S, U7-ch96

calib_packv5_042523_0143.root, FC#8, port C1

Entries	358
Mean	45.29
Std Dev	11.14

Turn on : 28.4898

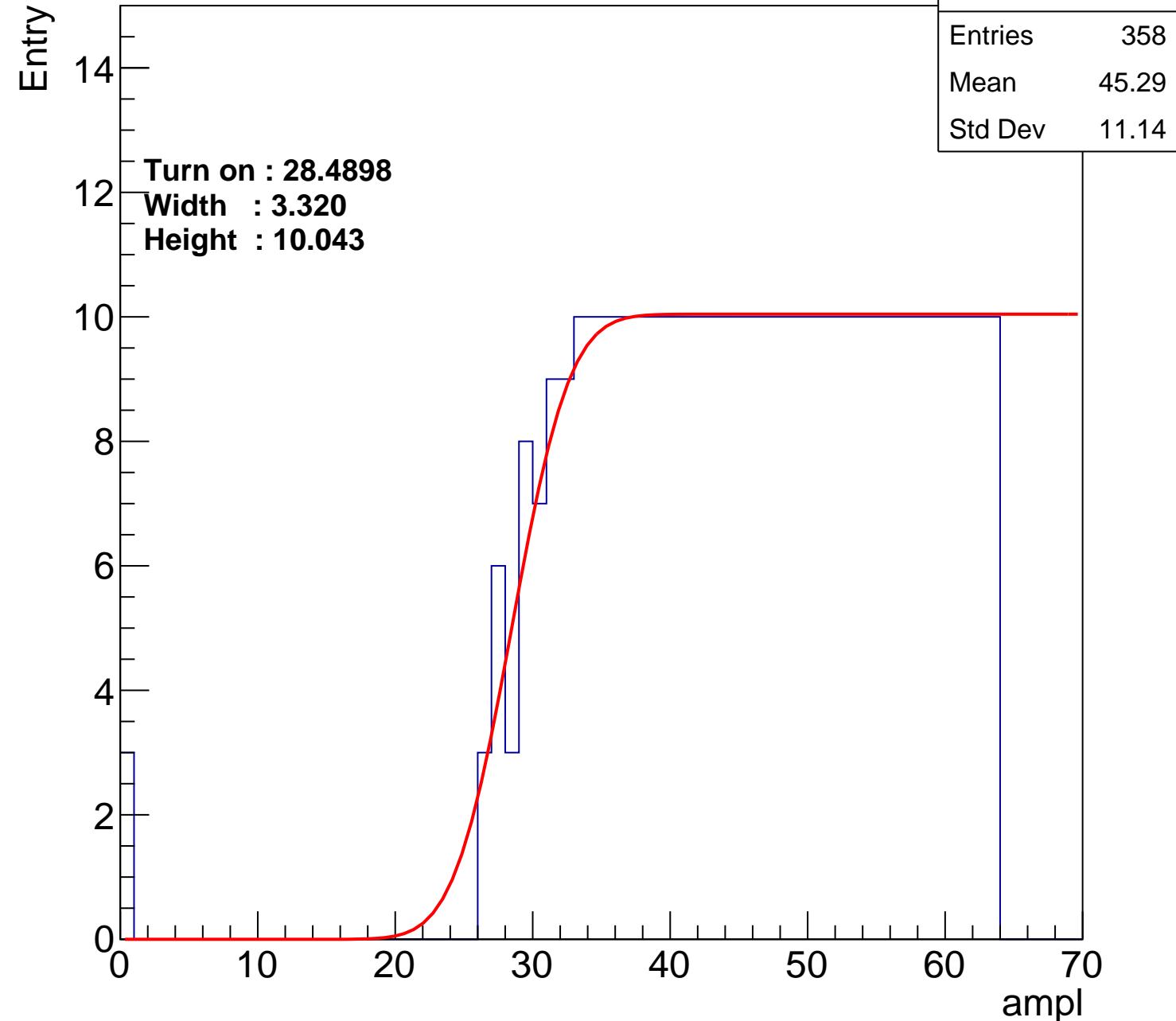
Width : 3.320

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch97

calib_packv5_042523_0143.root, FC#8, port C1

Entries	364
Mean	44.85
Std Dev	11.6

Turn on : 27.6136

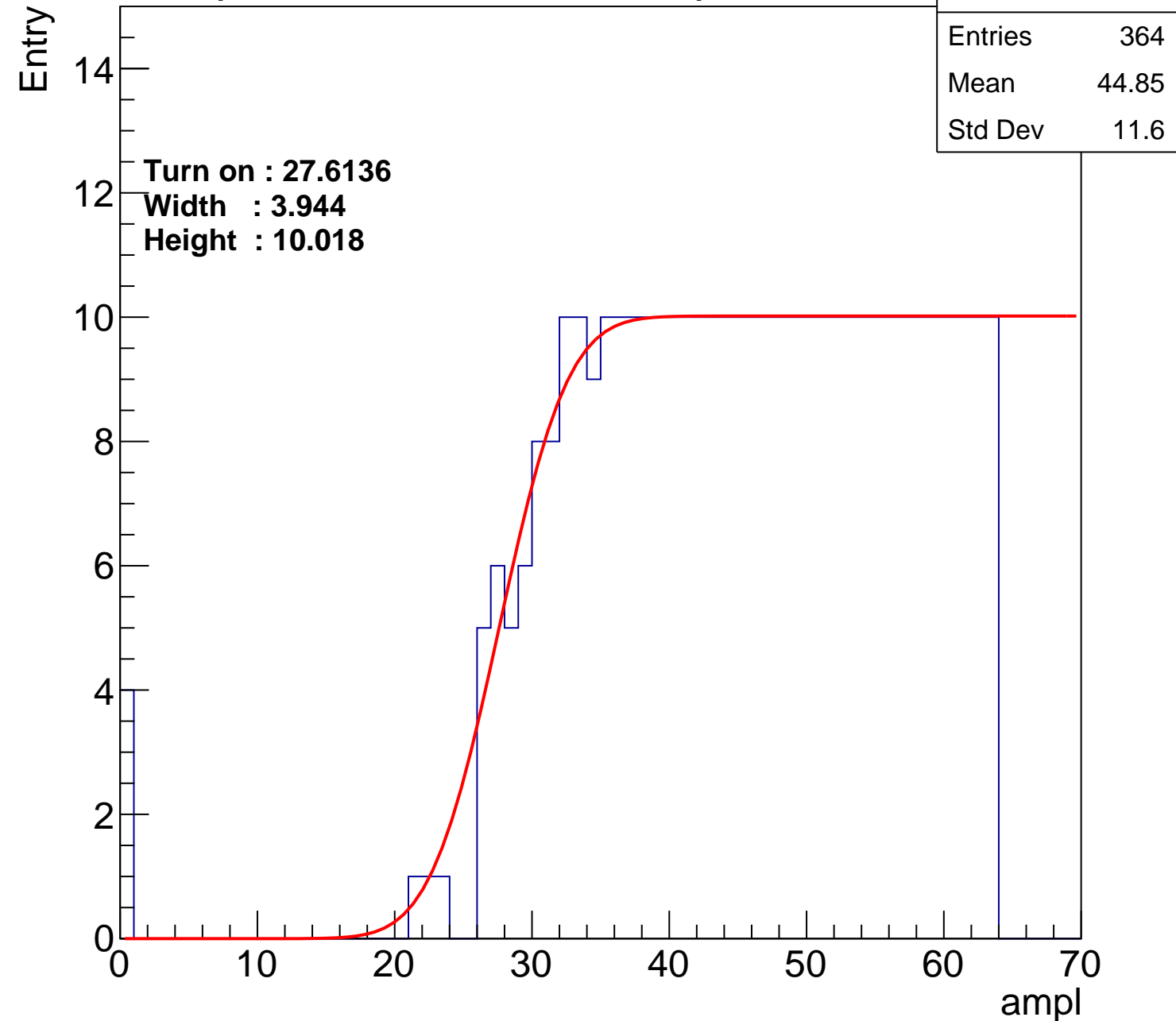
Width : 3.944

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch98

calib_packv5_042523_0143.root, FC#8, port C1

Entries	364
Mean	45.14
Std Dev	10.86

Turn on : 27.8196

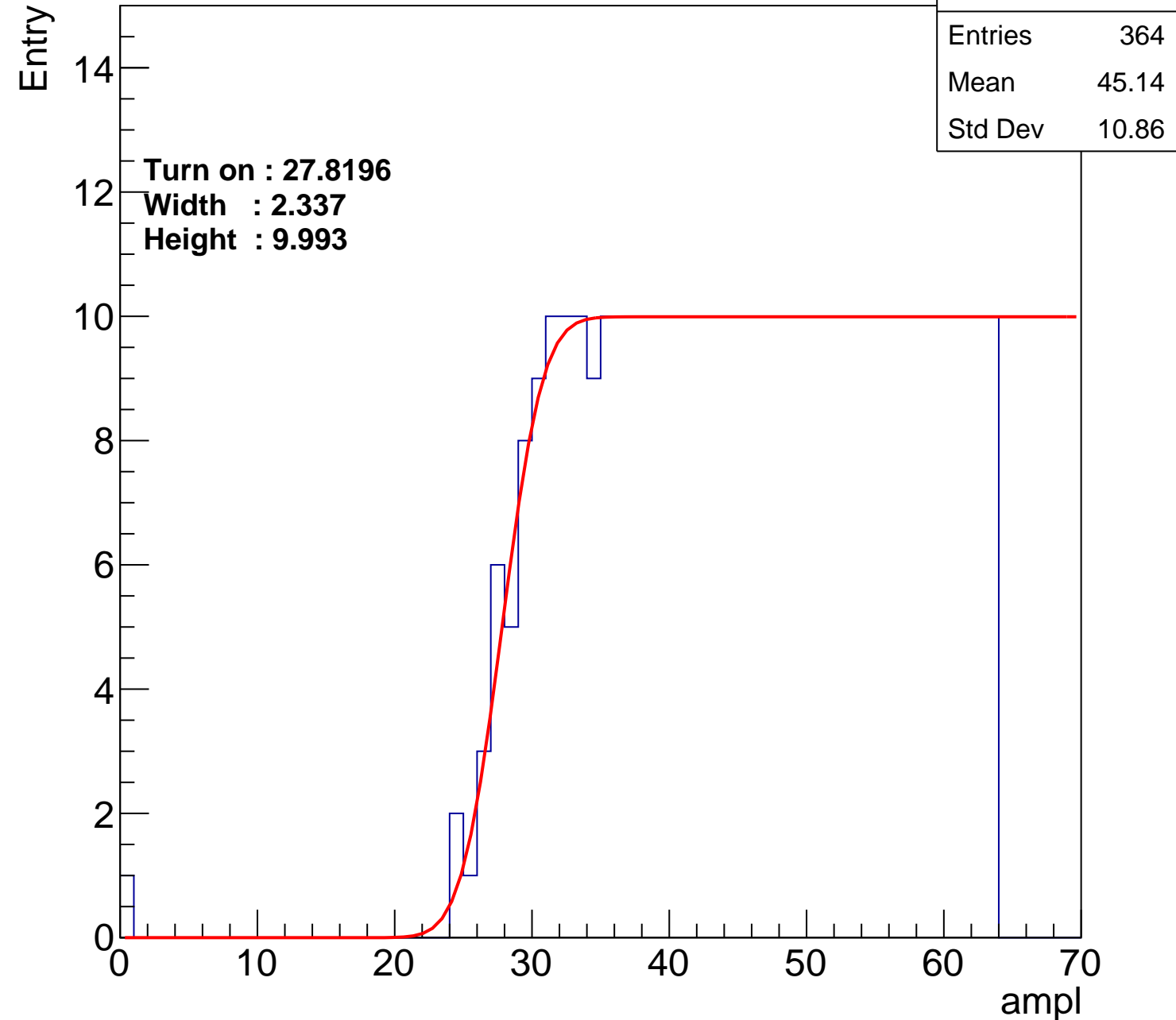
Width : 2.337

Height : 9.993

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch99

calib_packv5_042523_0143.root, FC#8, port C1

Entries	348
Mean	45.91
Std Dev	10.47

Turn on : 29.4061

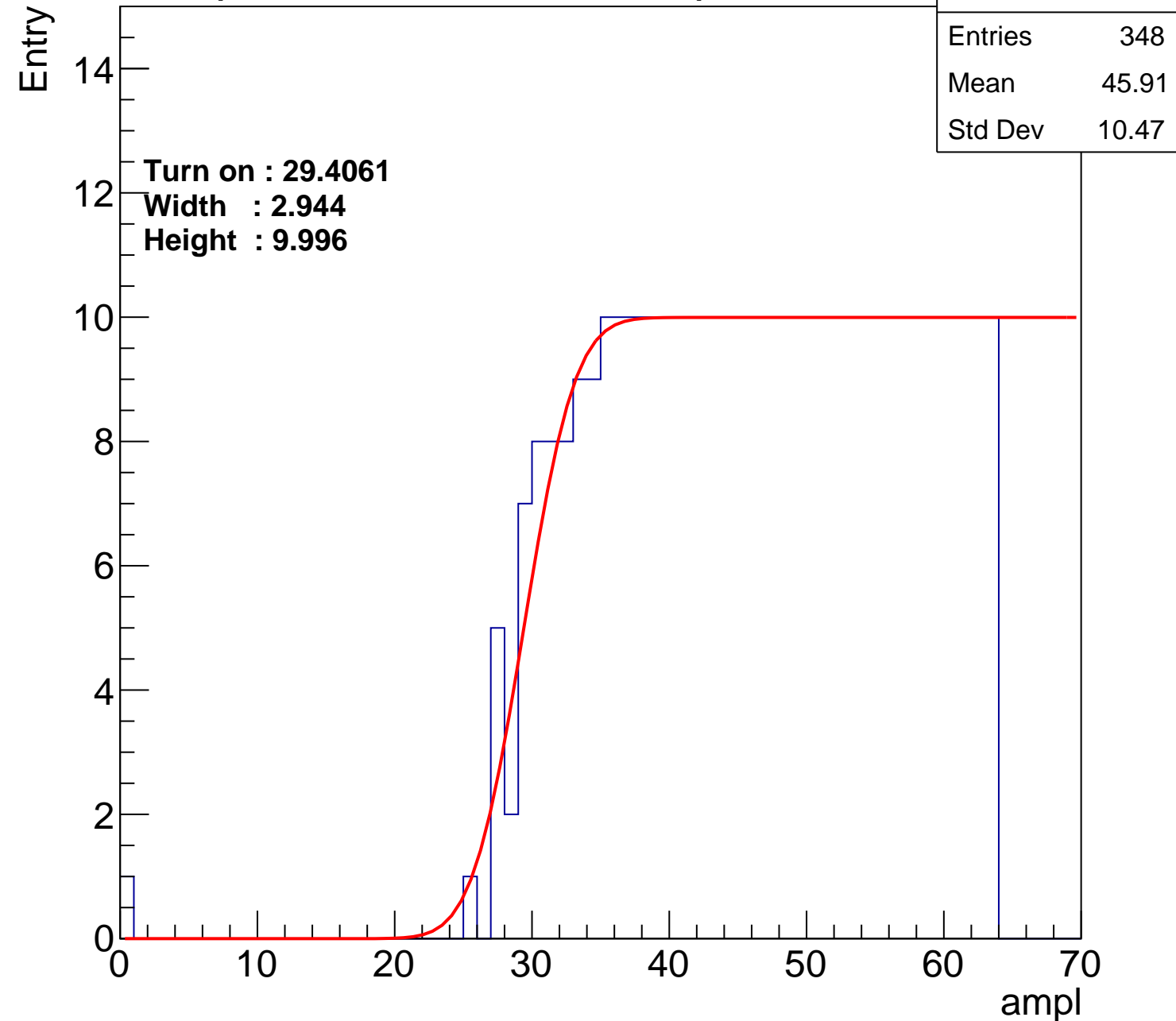
Width : 2.944

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch100

calib_packv5_042523_0143.root, FC#8, port C1

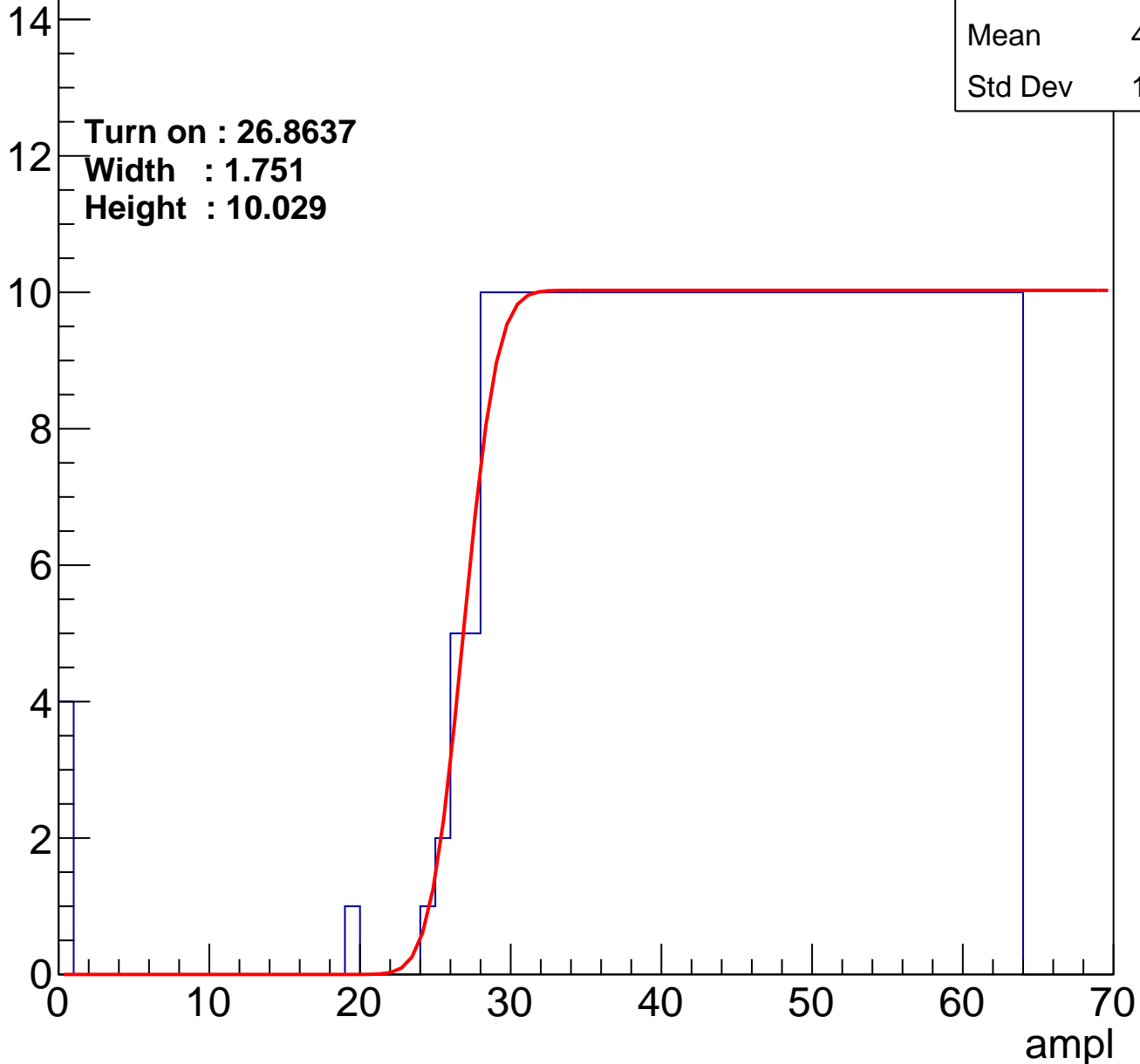
Entries	378
Mean	44.28
Std Dev	11.75

Turn on : 26.8637

Width : 1.751

Height : 10.029

Entry



B0L002S, U7-ch101

calib_packv5_042523_0143.root, FC#8, port C1

Entries	368
Mean	44.82
Std Dev	11.35

Turn on : 27.9804

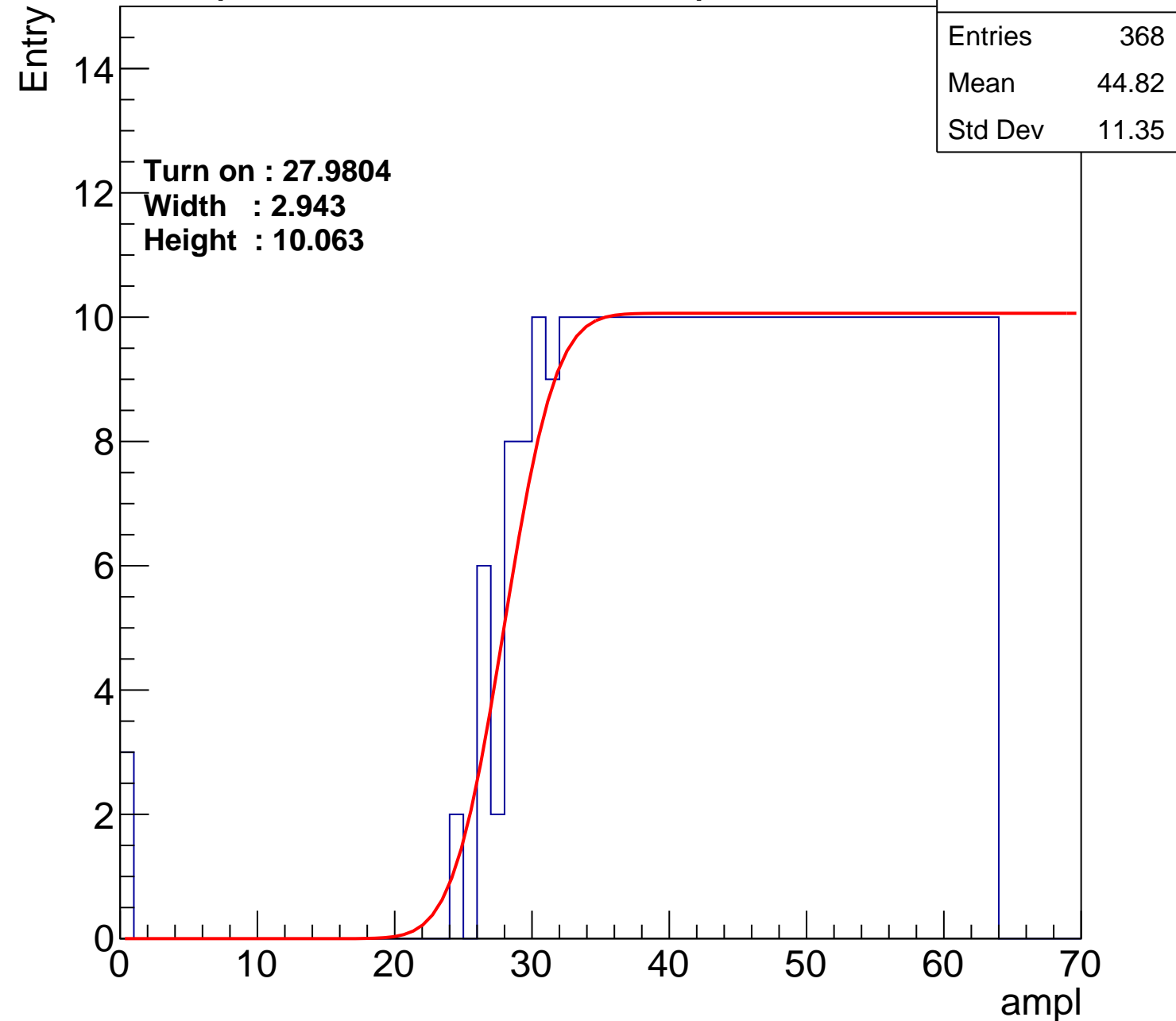
Width : 2.943

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch102

calib_packv5_042523_0143.root, FC#8, port C1

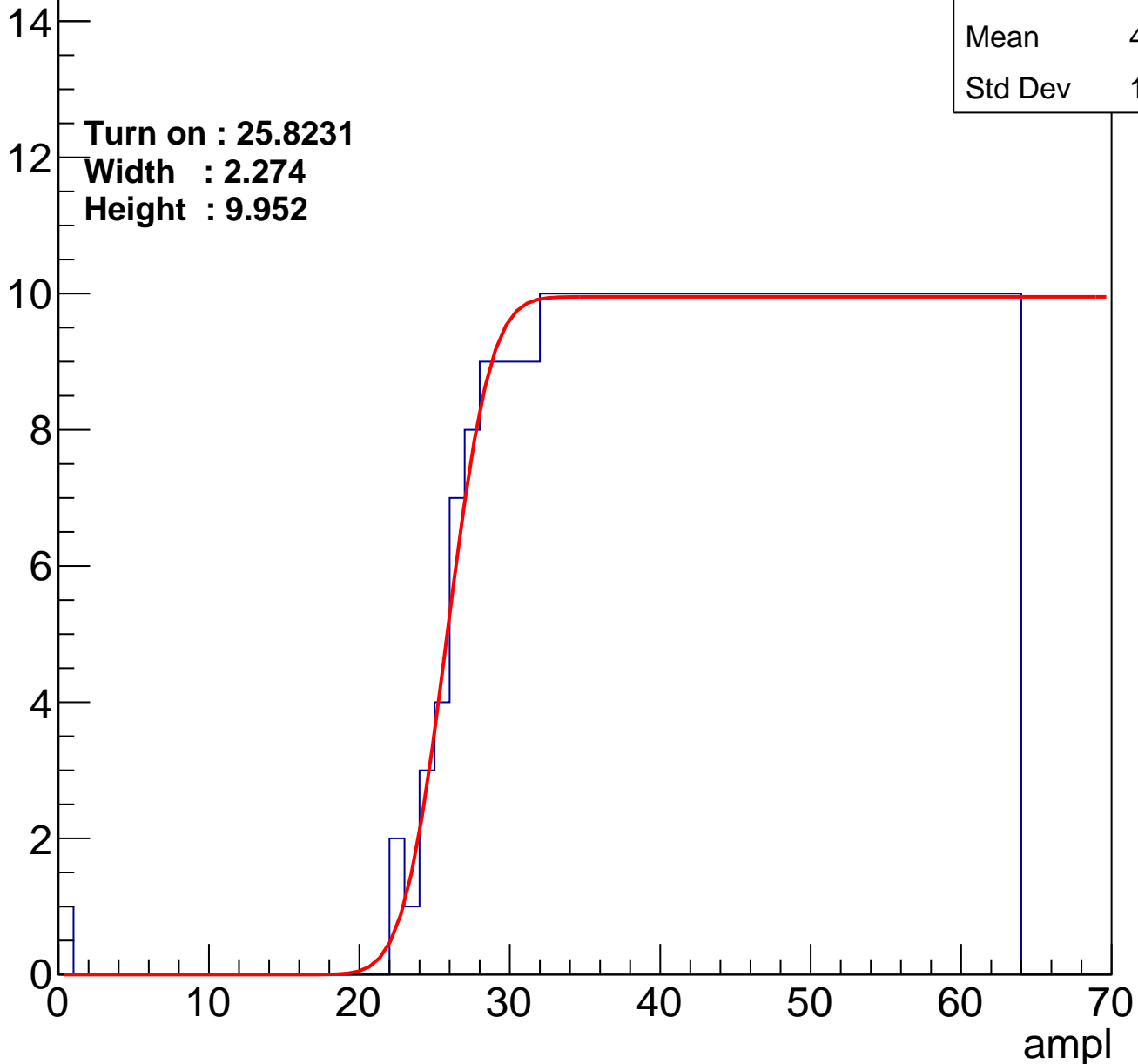
Entries	382
Mean	44.24
Std Dev	11.37

Turn on : 25.8231

Width : 2.274

Height : 9.952

Entry



B0L002S, U7-ch103

calib_packv5_042523_0143.root, FC#8, port C1

Entries	378
Mean	44.27
Std Dev	11.68

Turn on : 26.3519

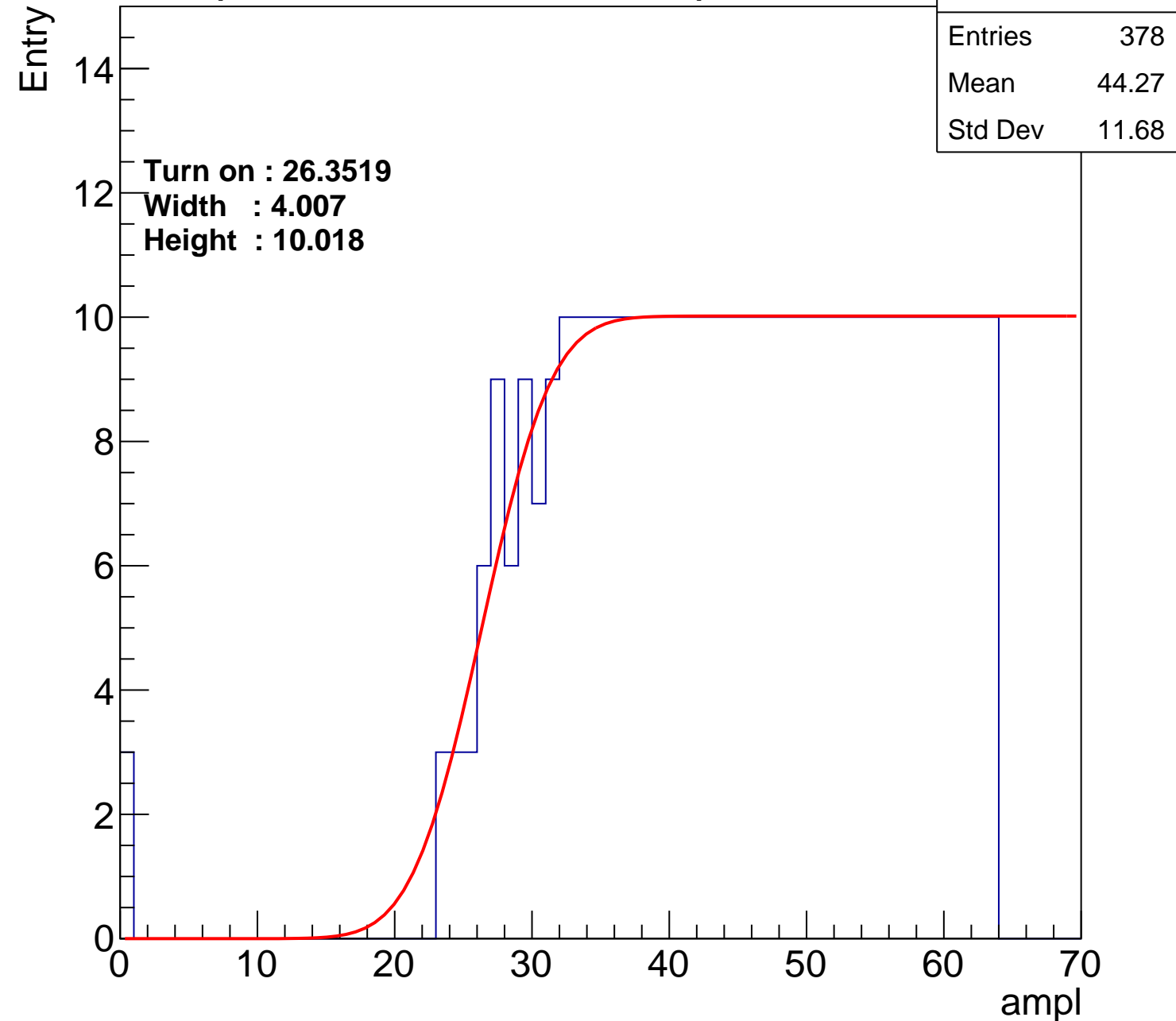
Width : 4.007

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch104

calib_packv5_042523_0143.root, FC#8, port C1

Entries	377
Mean	44.47
Std Dev	11.25

Turn on : 26.7166

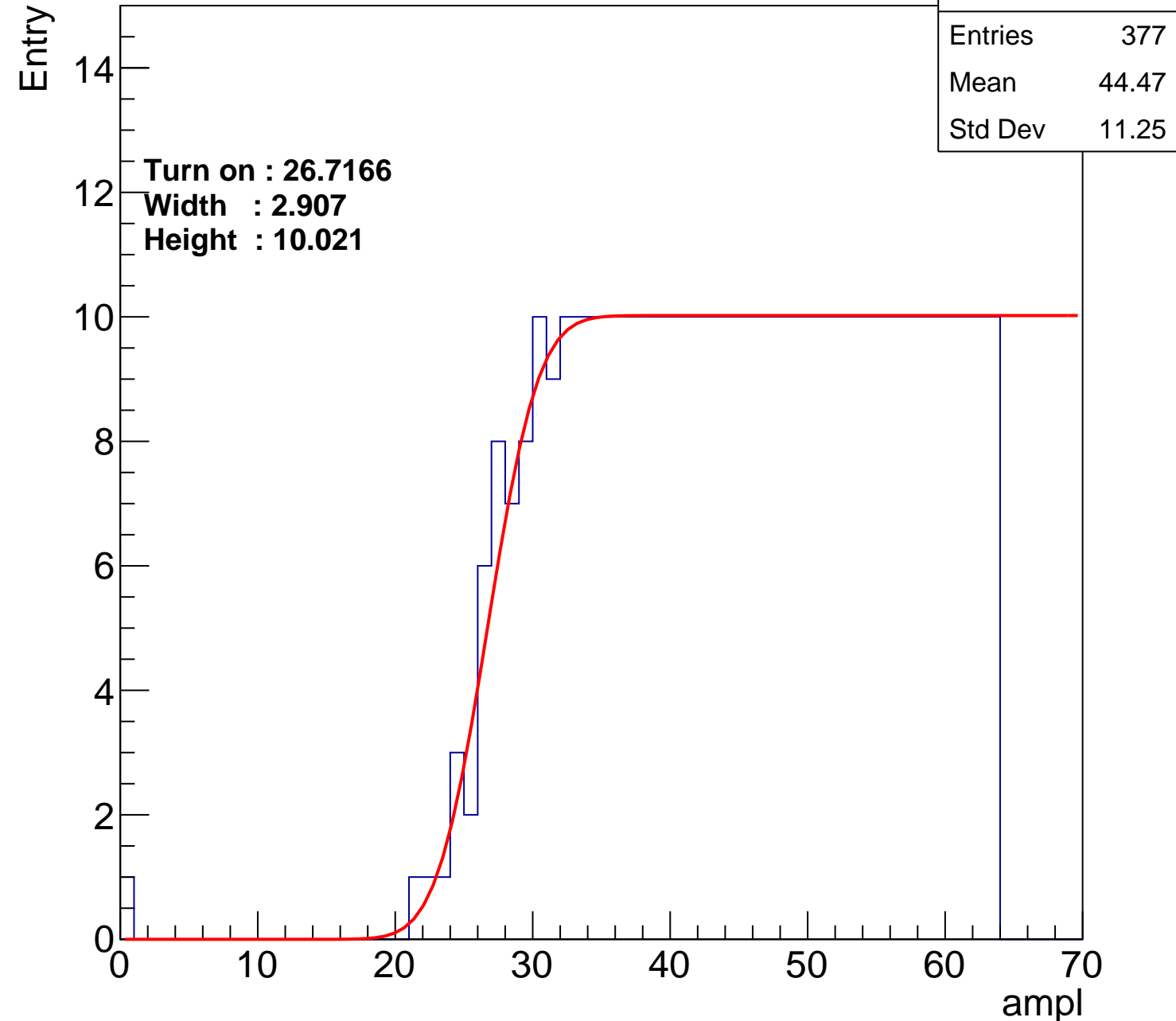
Width : 2.907

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch105

calib_packv5_042523_0143.root, FC#8, port C1

Entries	363
Mean	45.11
Std Dev	11.06

Turn on : 27.9542

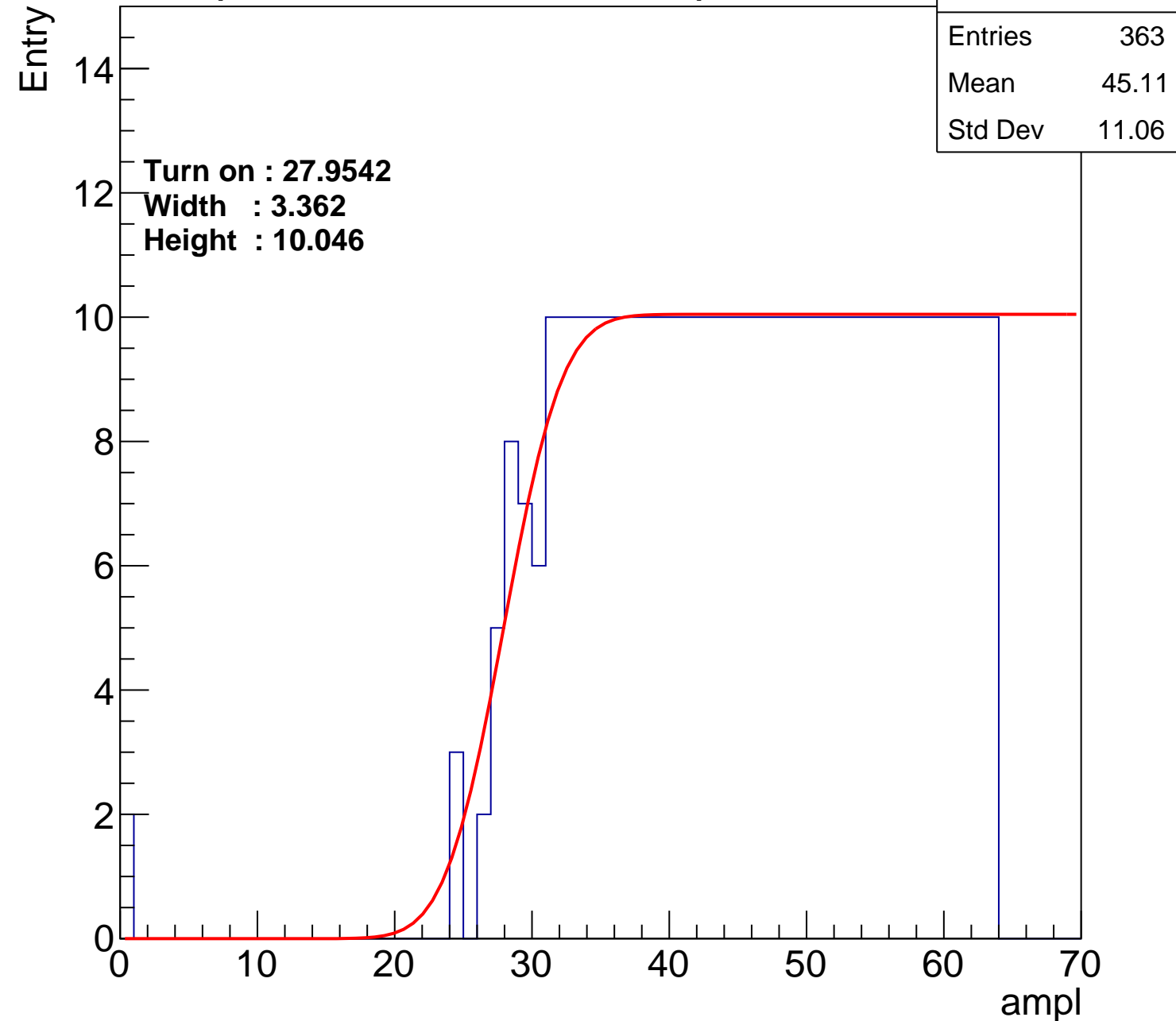
Width : 3.362

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch106

calib_packv5_042523_0143.root, FC#8, port C1

Entries	377
Mean	44.32
Std Dev	11.74

Turn on : 26.7381

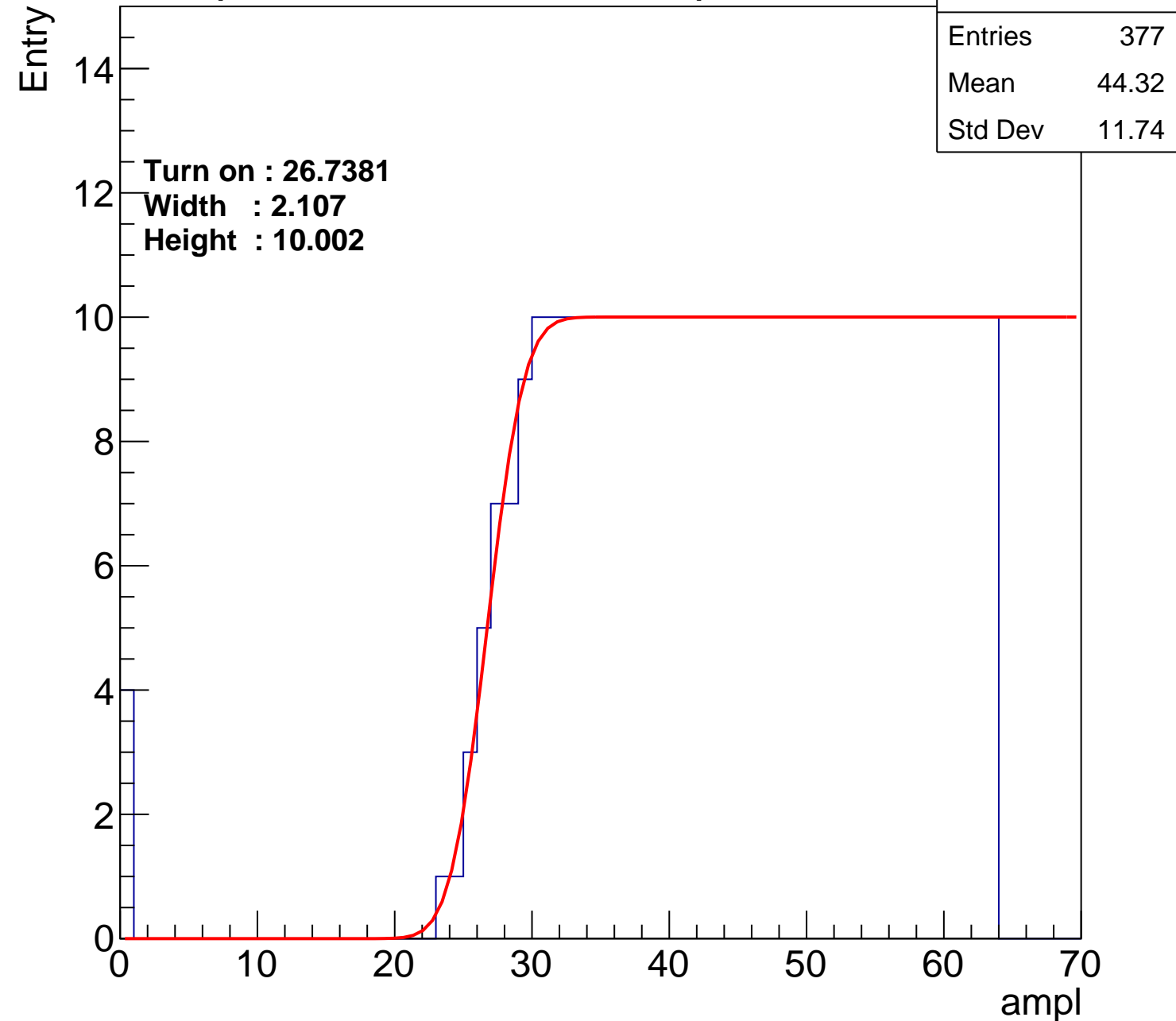
Width : 2.107

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch107

calib_packv5_042523_0143.root, FC#8, port C1

Entries	373
Mean	44.6
Std Dev	11.36

Turn on : 26.9289

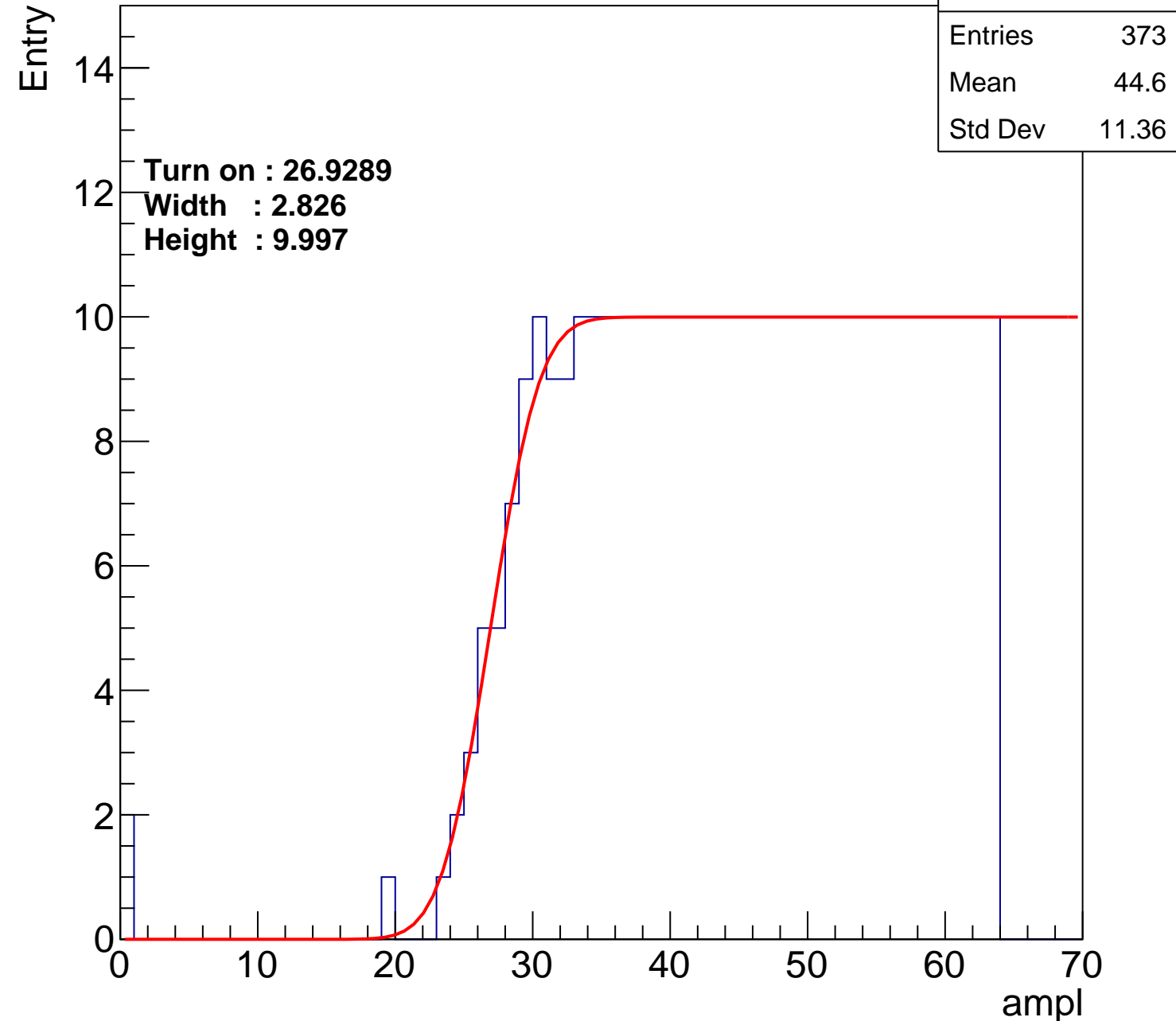
Width : 2.826

Height : 9.997

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch108

calib_packv5_042523_0143.root, FC#8, port C1

Entries	354
Mean	45.39
Std Dev	11.29

Turn on : 29.3104

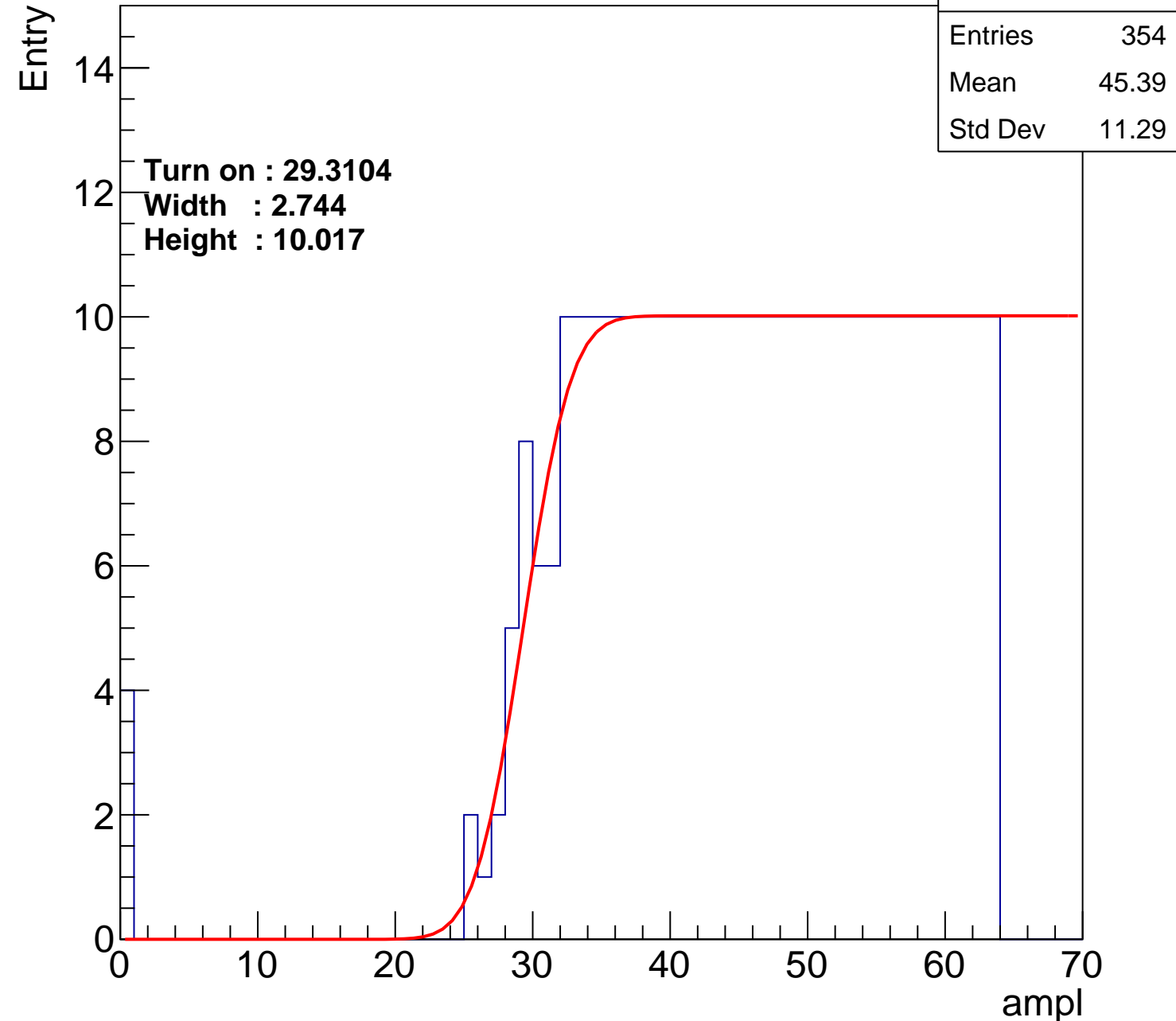
Width : 2.744

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch109

calib_packv5_042523_0143.root, FC#8, port C1

Entries	375
Mean	44.41
Std Dev	11.62

Turn on : 26.8728

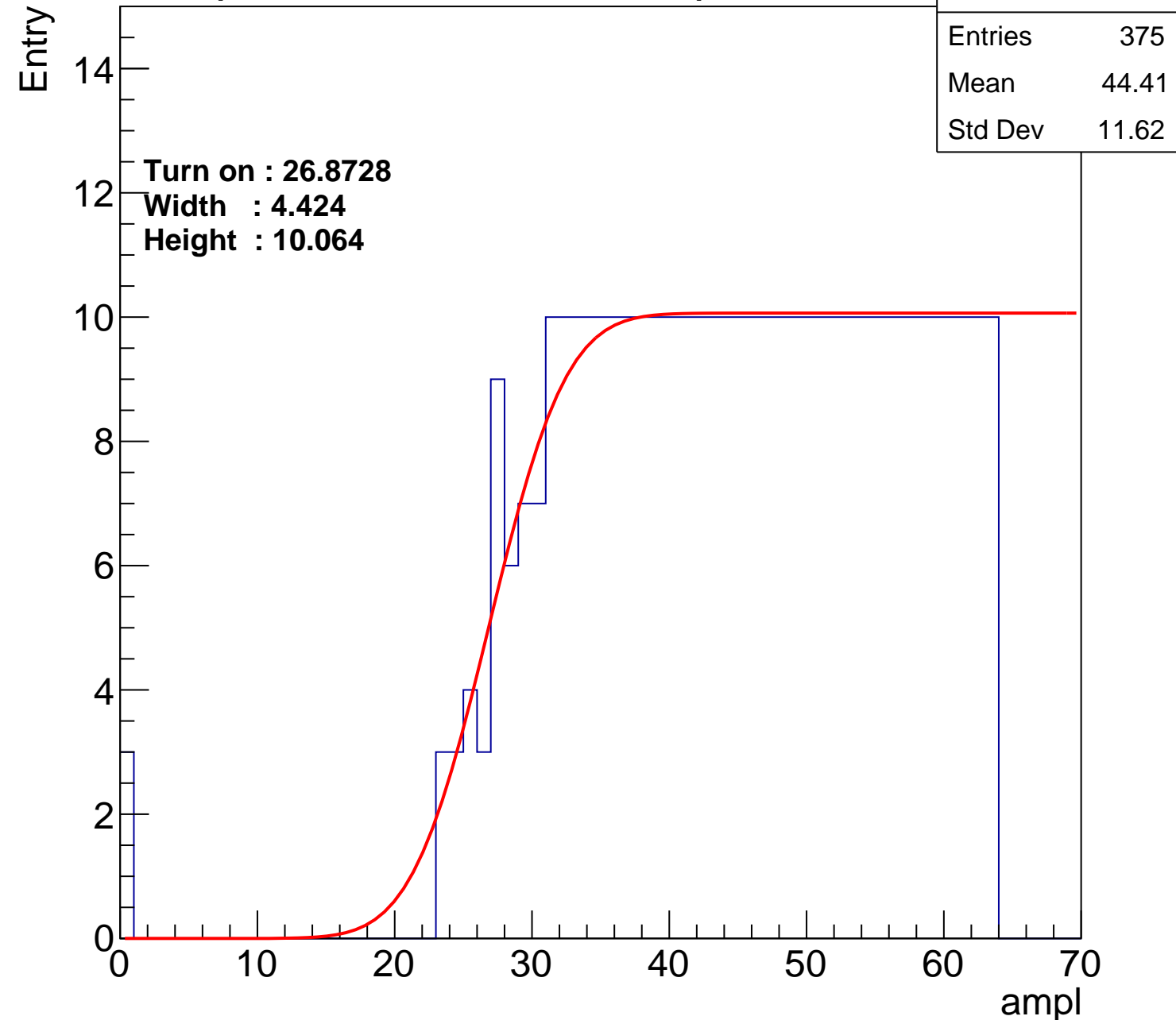
Width : 4.424

Height : 10.064

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch110

calib_packv5_042523_0143.root, FC#8, port C1

Entries	348
Mean	45.95
Std Dev	10.41

Turn on : 28.7373

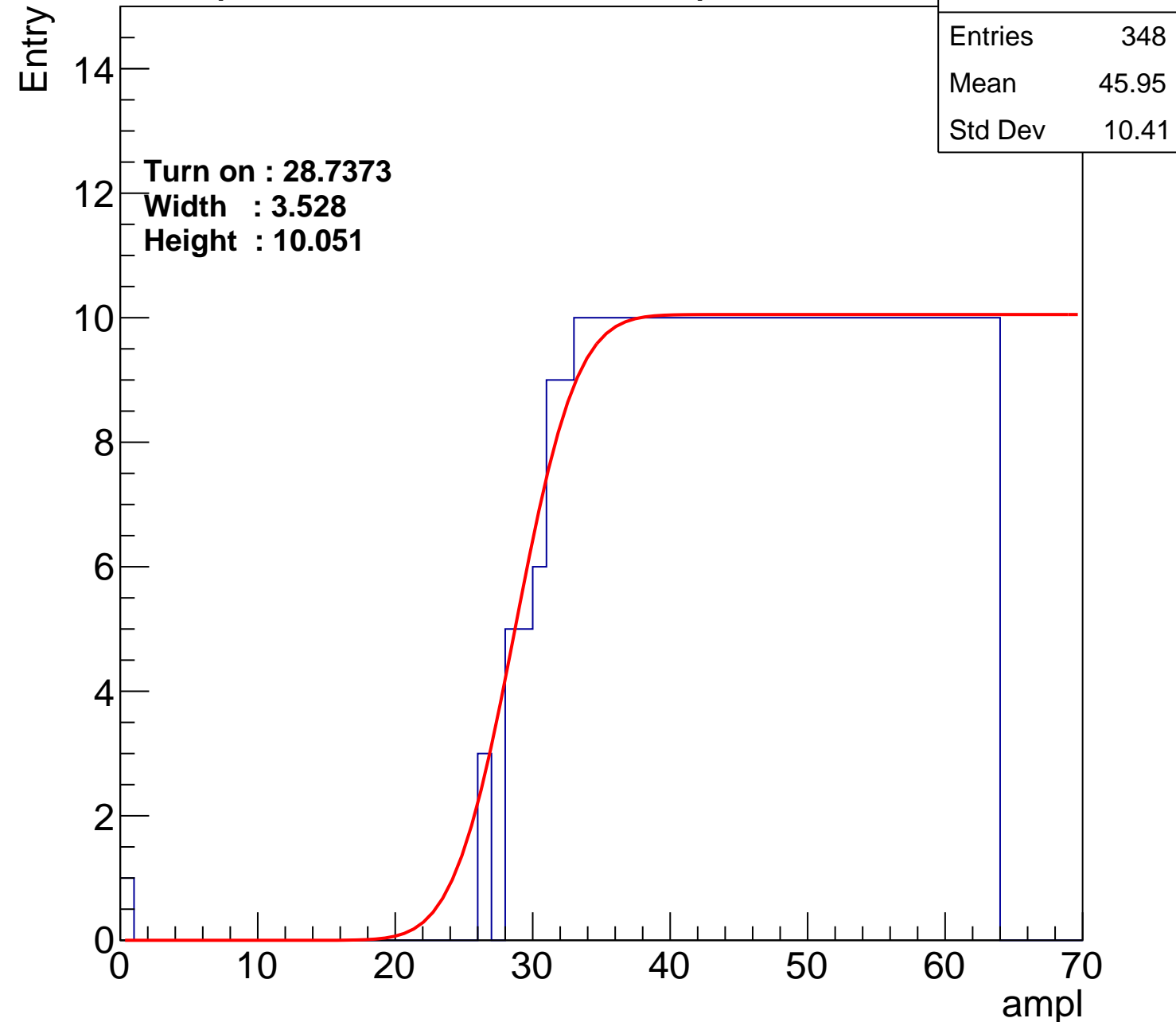
Width : 3.528

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch111

calib_packv5_042523_0143.root, FC#8, port C1

Entries	342
Mean	46.14
Std Dev	10.55

Turn on : 30.1226

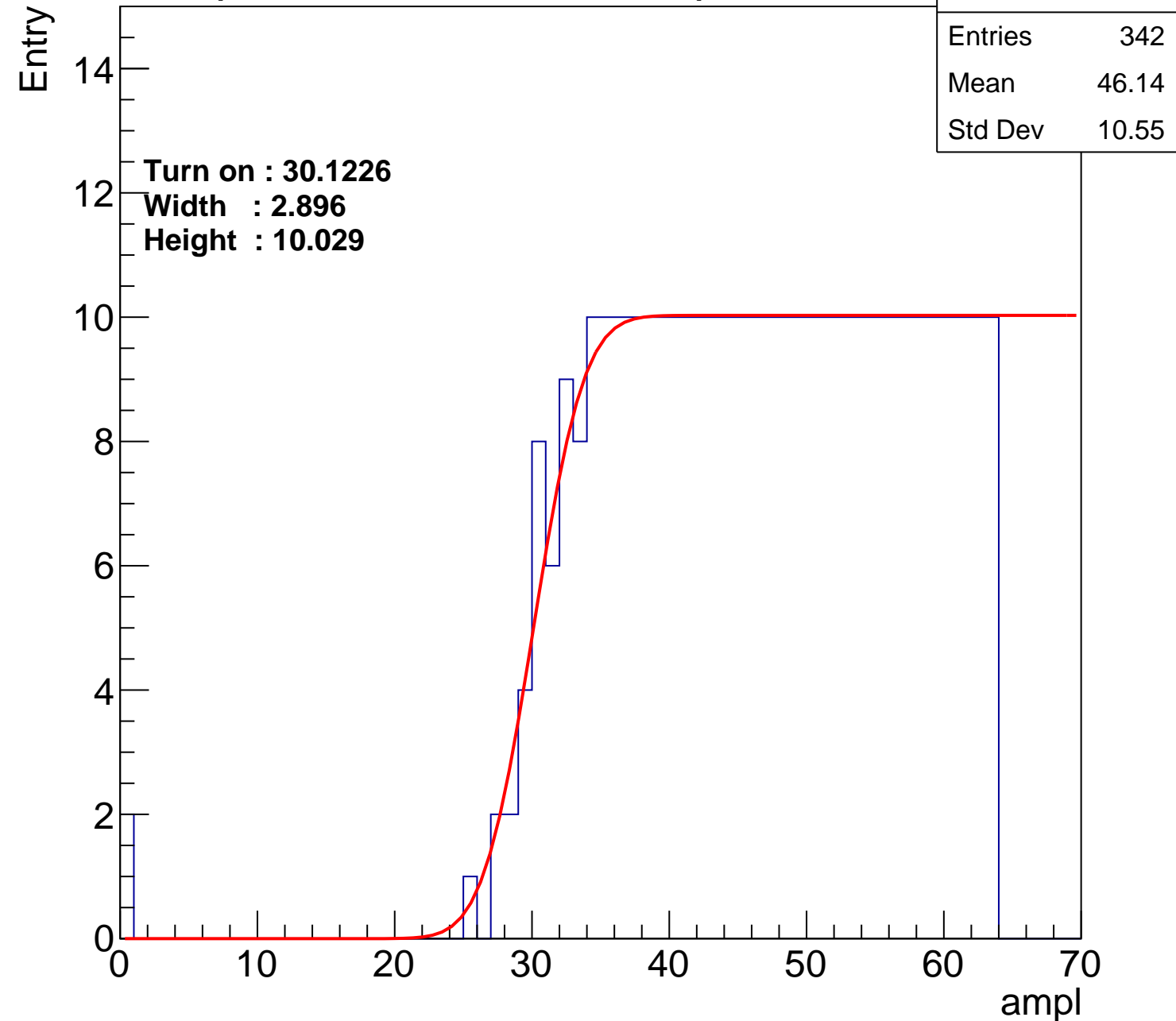
Width : 2.896

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch112

calib_packv5_042523_0143.root, FC#8, port C1

Entries	385
Mean	43.91
Std Dev	11.88

Turn on : 25.9847

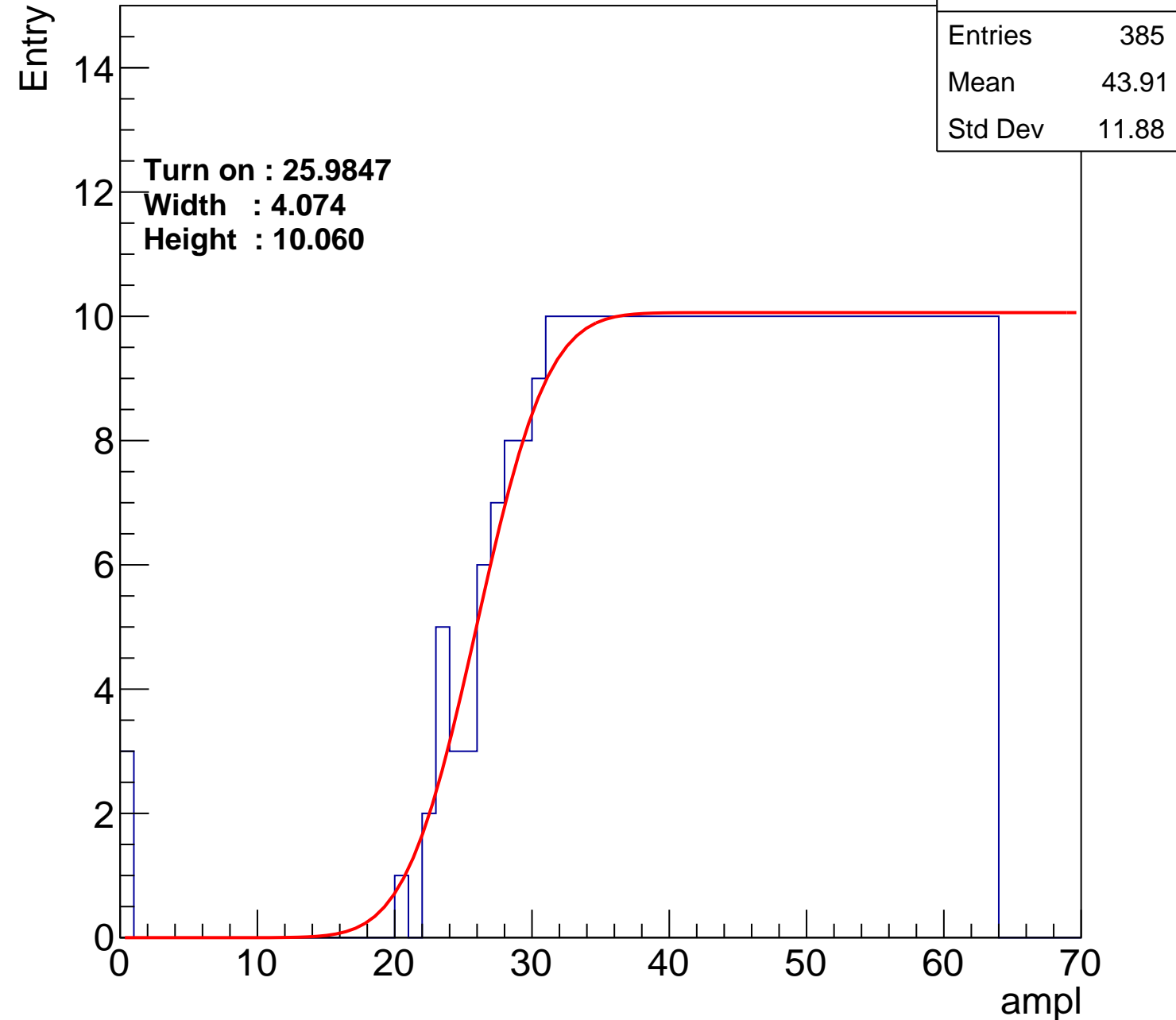
Width : 4.074

Height : 10.060

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch113

calib_packv5_042523_0143.root, FC#8, port C1

Entries	368
Mean	44.85
Std Dev	11.23

Turn on : 28.0649

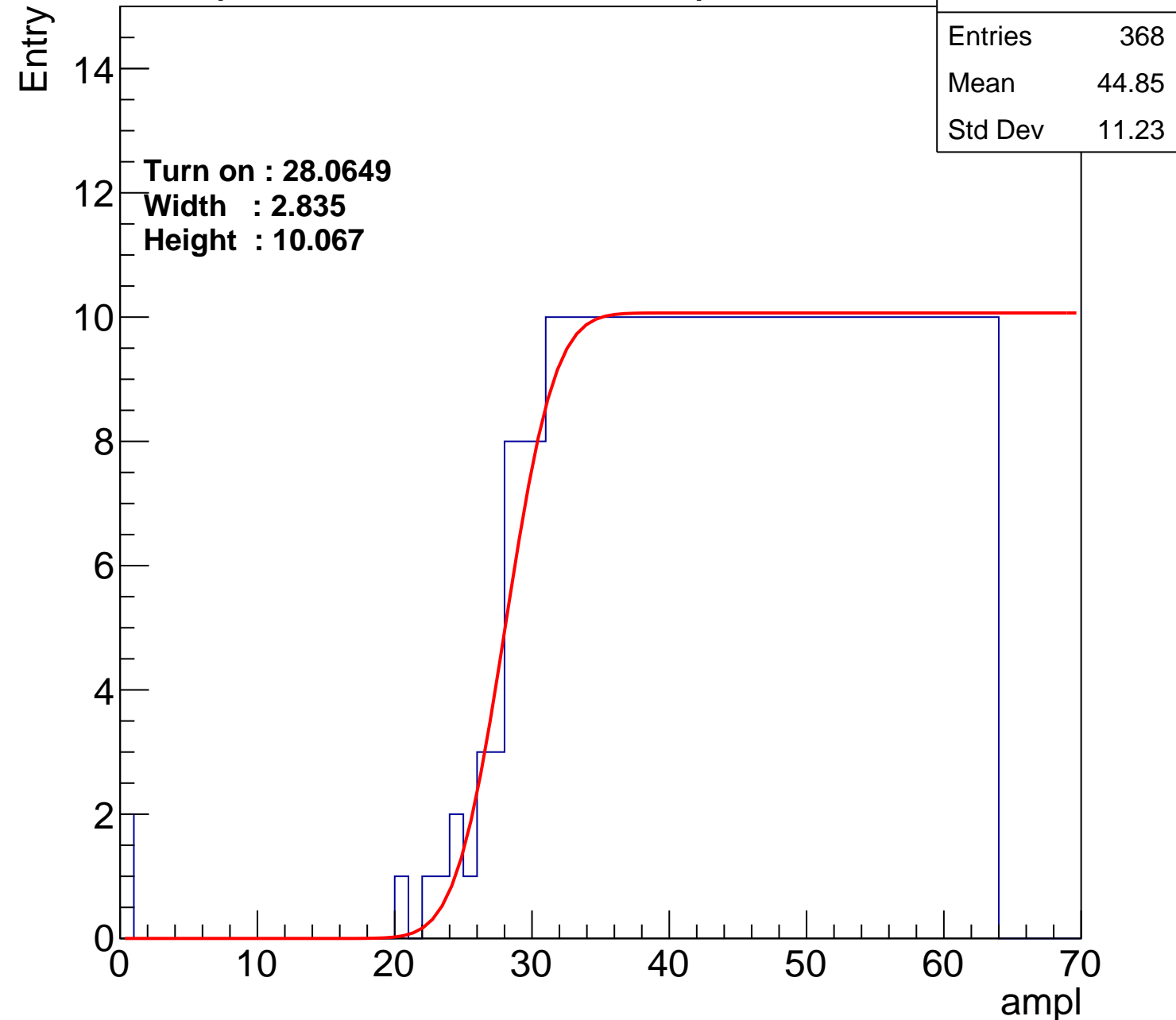
Width : 2.835

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch114

calib_packv5_042523_0143.root, FC#8, port C1

Entries	381
Mean	44.13
Std Dev	11.74

Turn on : 26.6809

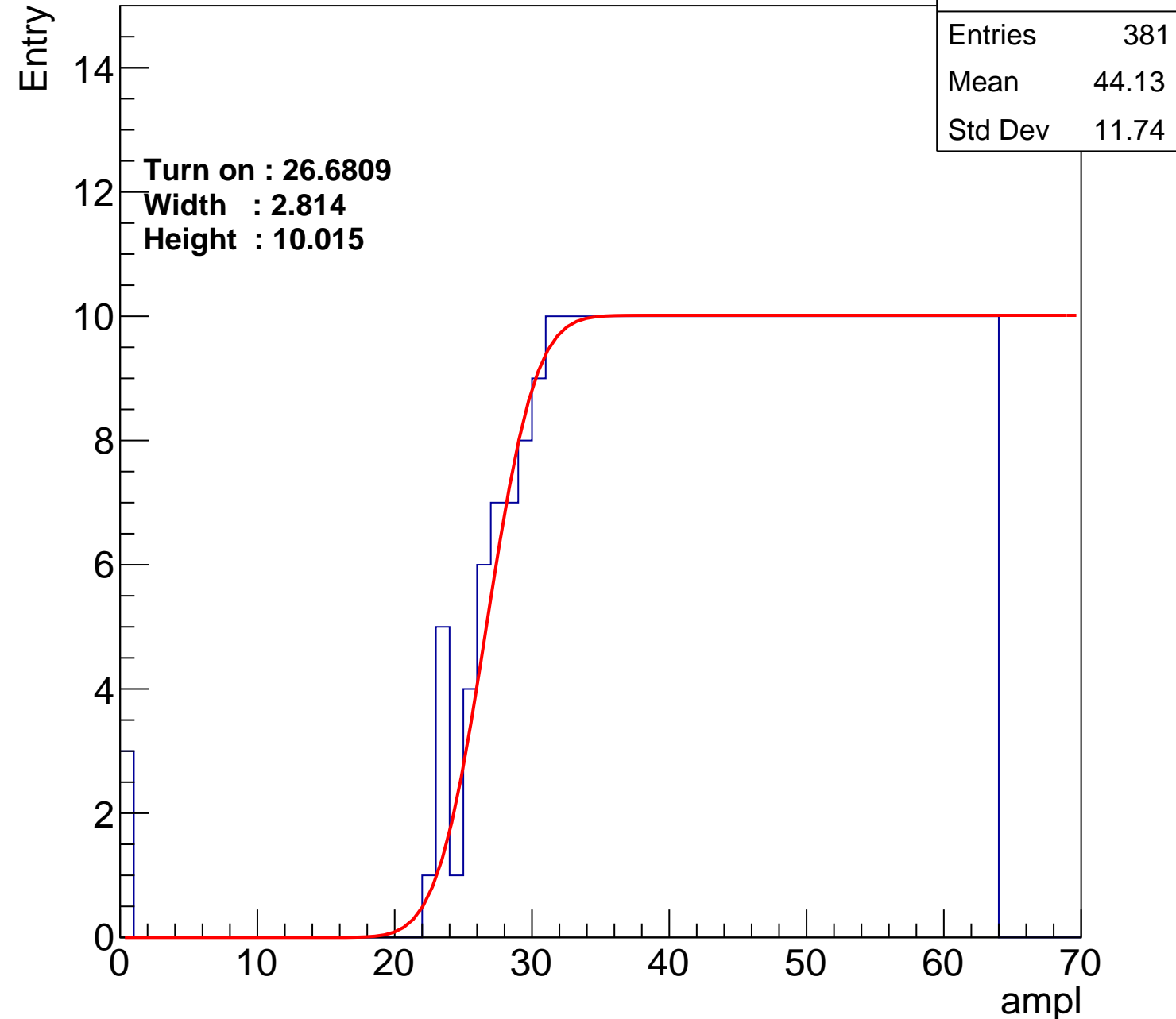
Width : 2.814

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



calib_packv5_042523_0143.root, FC#8, port C1

calib_packv5_042523_0143.root, FC#8, port C1

Turn on : 29.4117
Width : 2.165
Height : 10.002



B0L002S, U7-ch116

calib_packv5_042523_0143.root, FC#8, port C1

Entries	366
Mean	45.08
Std Dev	10.86

Turn on : 27.5946

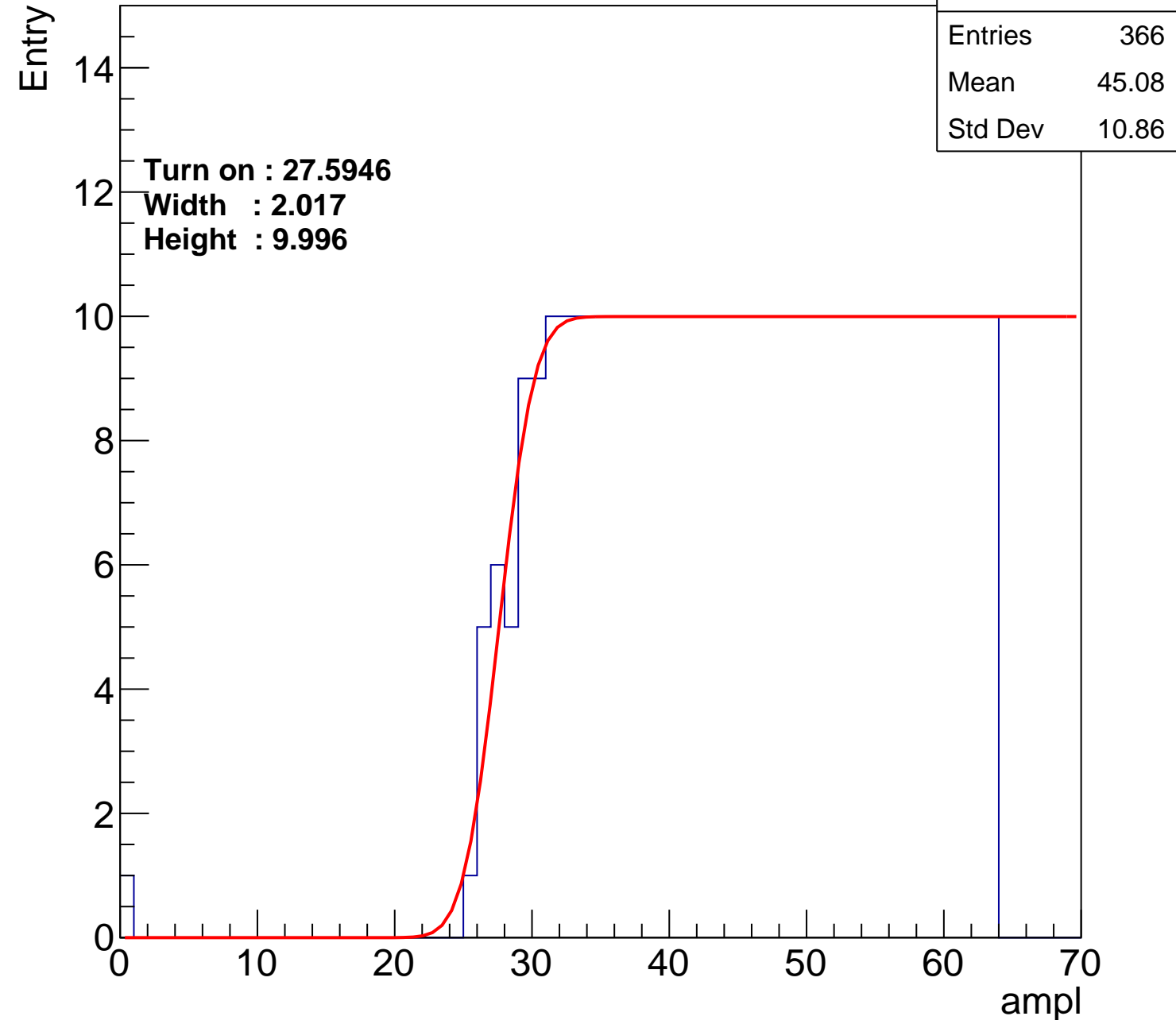
Width : 2.017

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl



calib_packv5_042523_0143.root, FC#8, port C1

calib_packv5_042523_0143.root, FC#8, port C1

Turn on : 29.2630
Width : 3.120
Height : 10.046



B0L002S, U7-ch118

calib_packv5_042523_0143.root, FC#8, port C1

Entries	368
Mean	44.87
Std Dev	11.18

Turn on : 27.6362

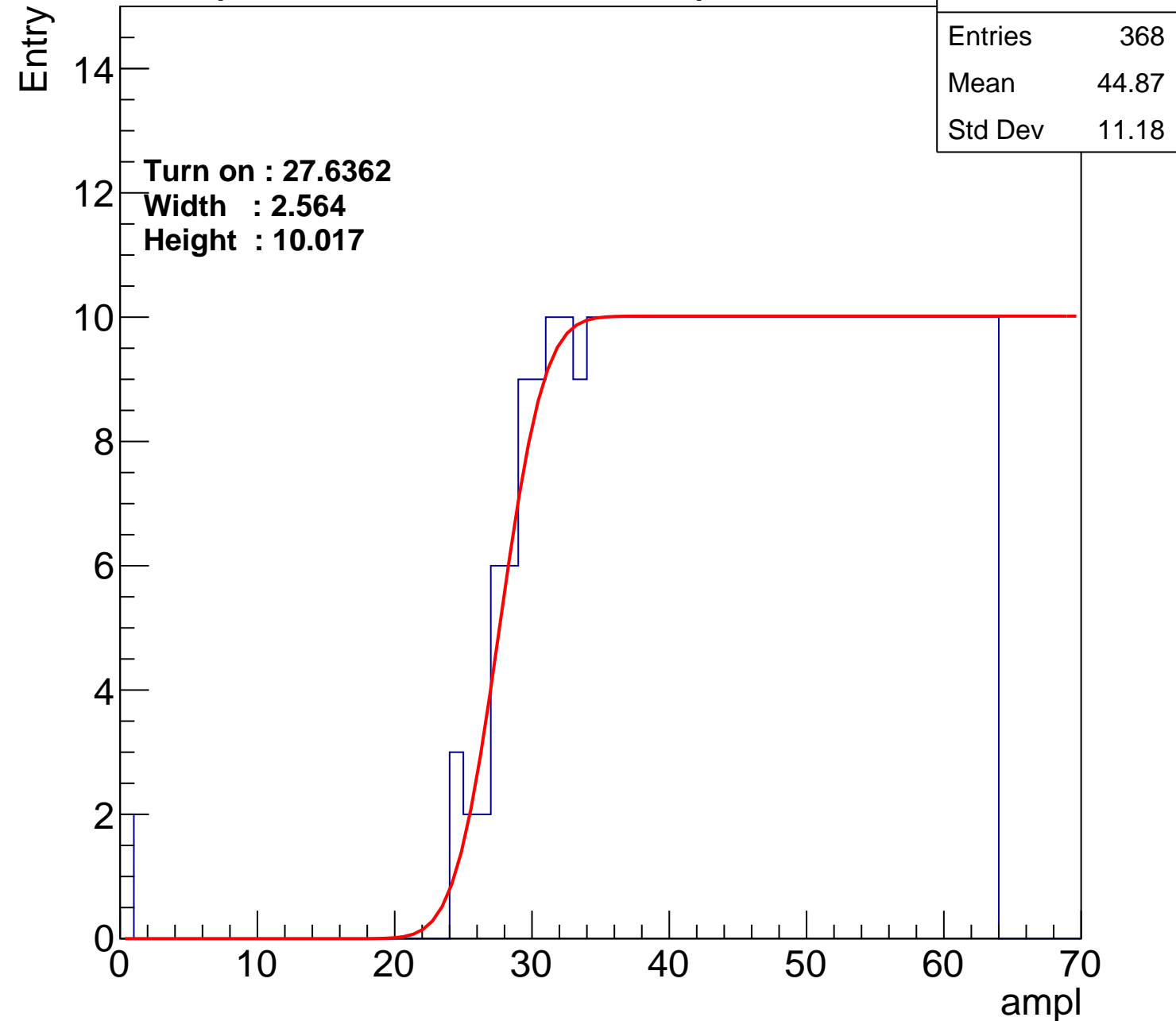
Width : 2.564

Height : 10.017

Entry

14
12
10
8
6
4
2
0

ampl



calib_packv5_042523_0143.root, FC#8, port C1

calib_packv5_042523_0143.root, FC#8, port C1

Turn on : 27.8028
Width : 3.450
Height : 10.047



B0L002S, U7-ch120

calib_packv5_042523_0143.root, FC#8, port C1

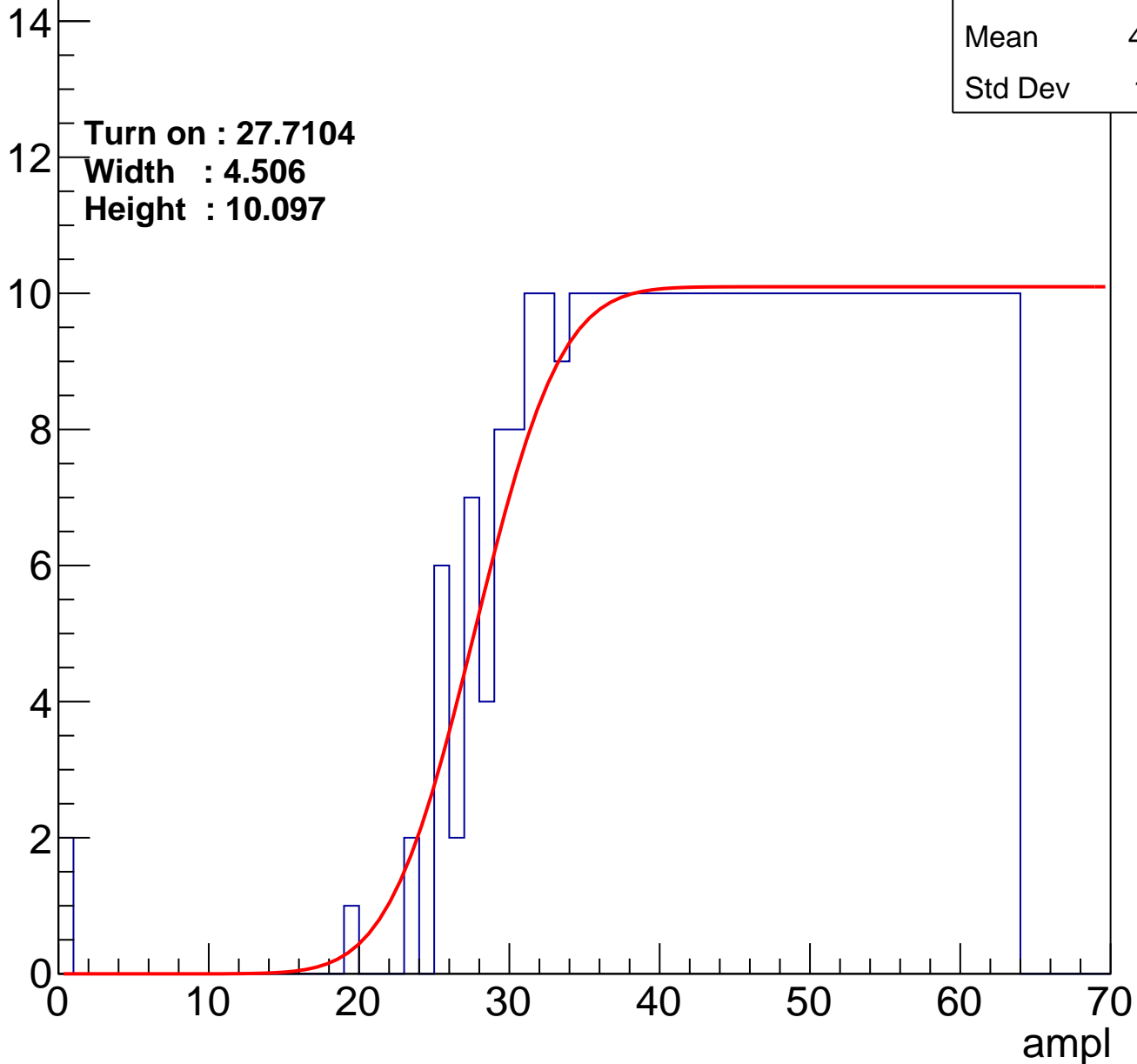
Entries	369
Mean	44.76
Std Dev	11.31

Turn on : 27.7104

Width : 4.506

Height : 10.097

Entry



B0L002S, U7-ch121

calib_packv5_042523_0143.root, FC#8, port C1

Entries	379
Mean	44.3
Std Dev	11.51

Turn on : 26.5289

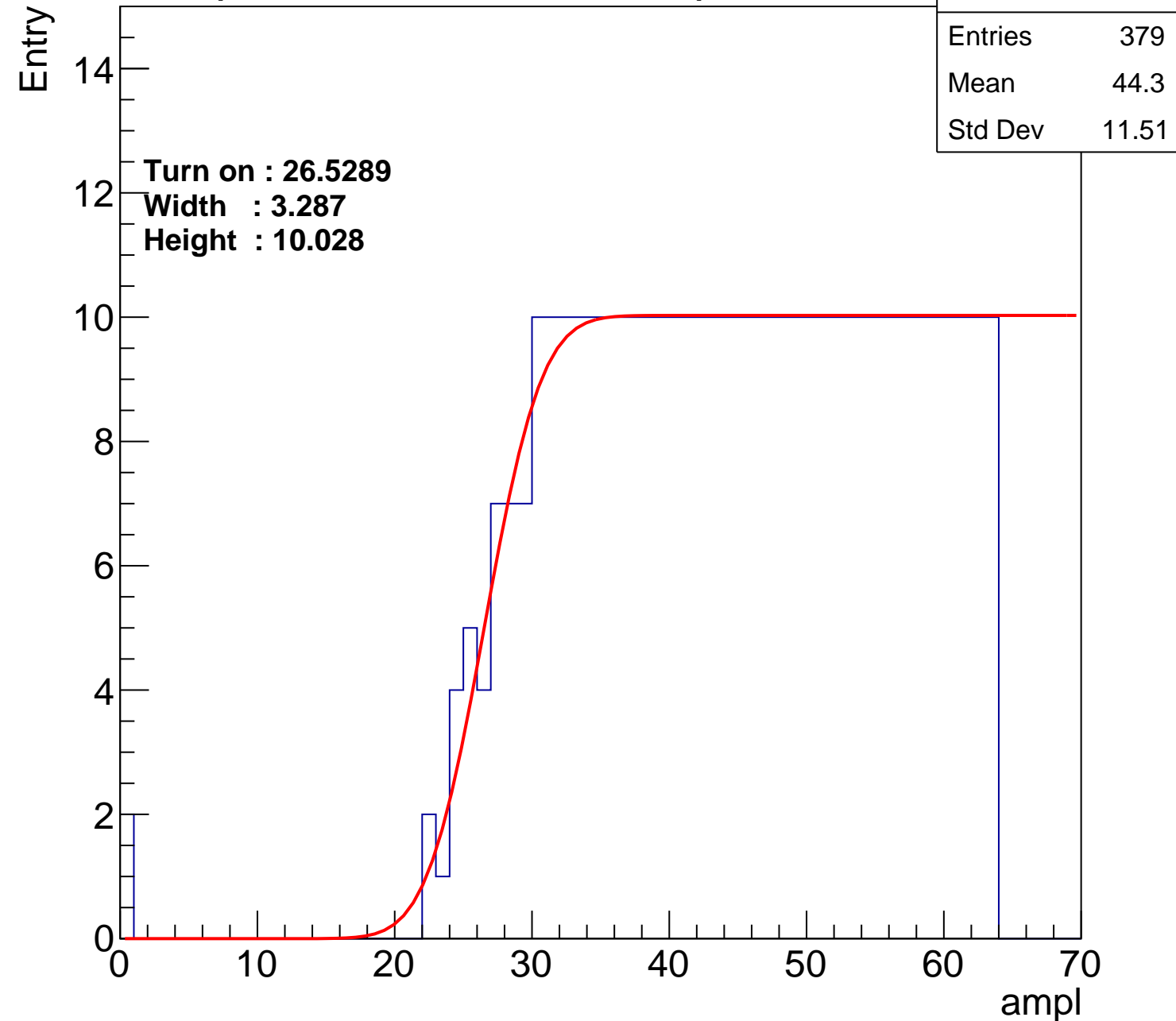
Width : 3.287

Height : 10.028

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch122

calib_packv5_042523_0143.root, FC#8, port C1

Entries	364
Mean	45.12
Std Dev	10.9

Turn on : 28.0676

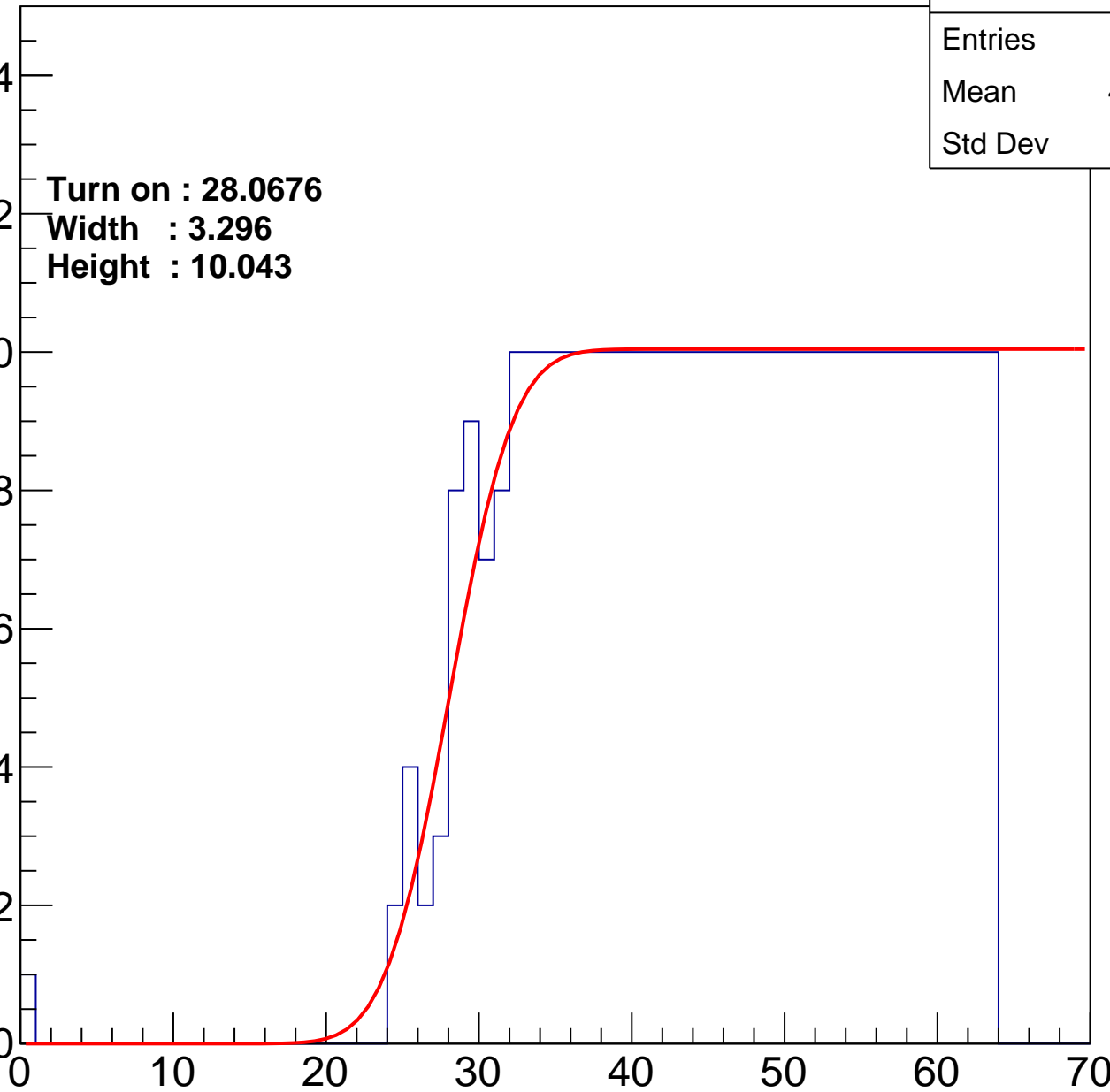
Width : 3.296

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch123

calib_packv5_042523_0143.root, FC#8, port C1

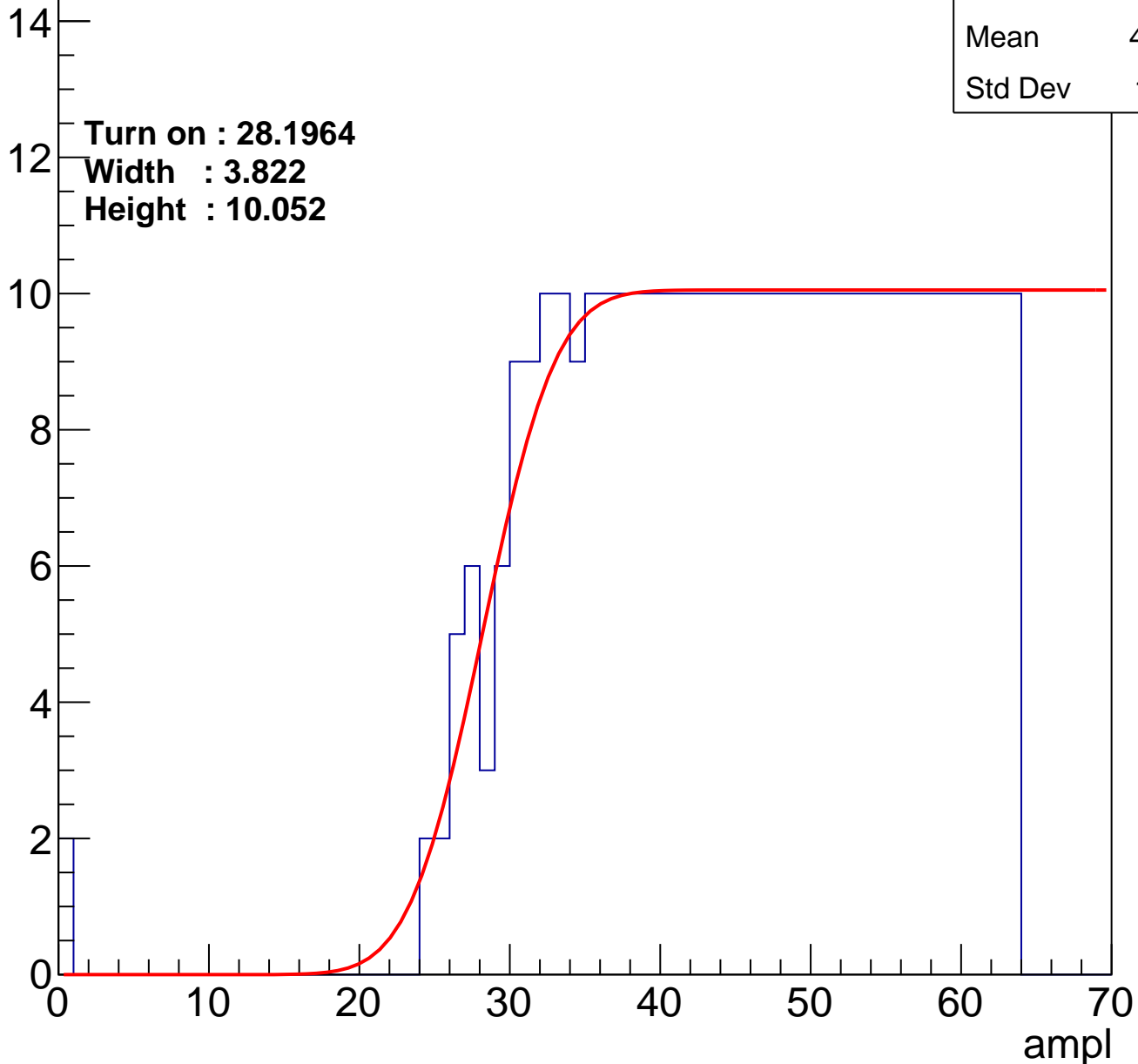
Entries	363
Mean	45.08
Std Dev	11.11

Turn on : 28.1964

Width : 3.822

Height : 10.052

Entry



B0L002S, U7-ch124

calib_packv5_042523_0143.root, FC#8, port C1

Entries	361
Mean	45.15
Std Dev	11.1

Turn on : 28.1614

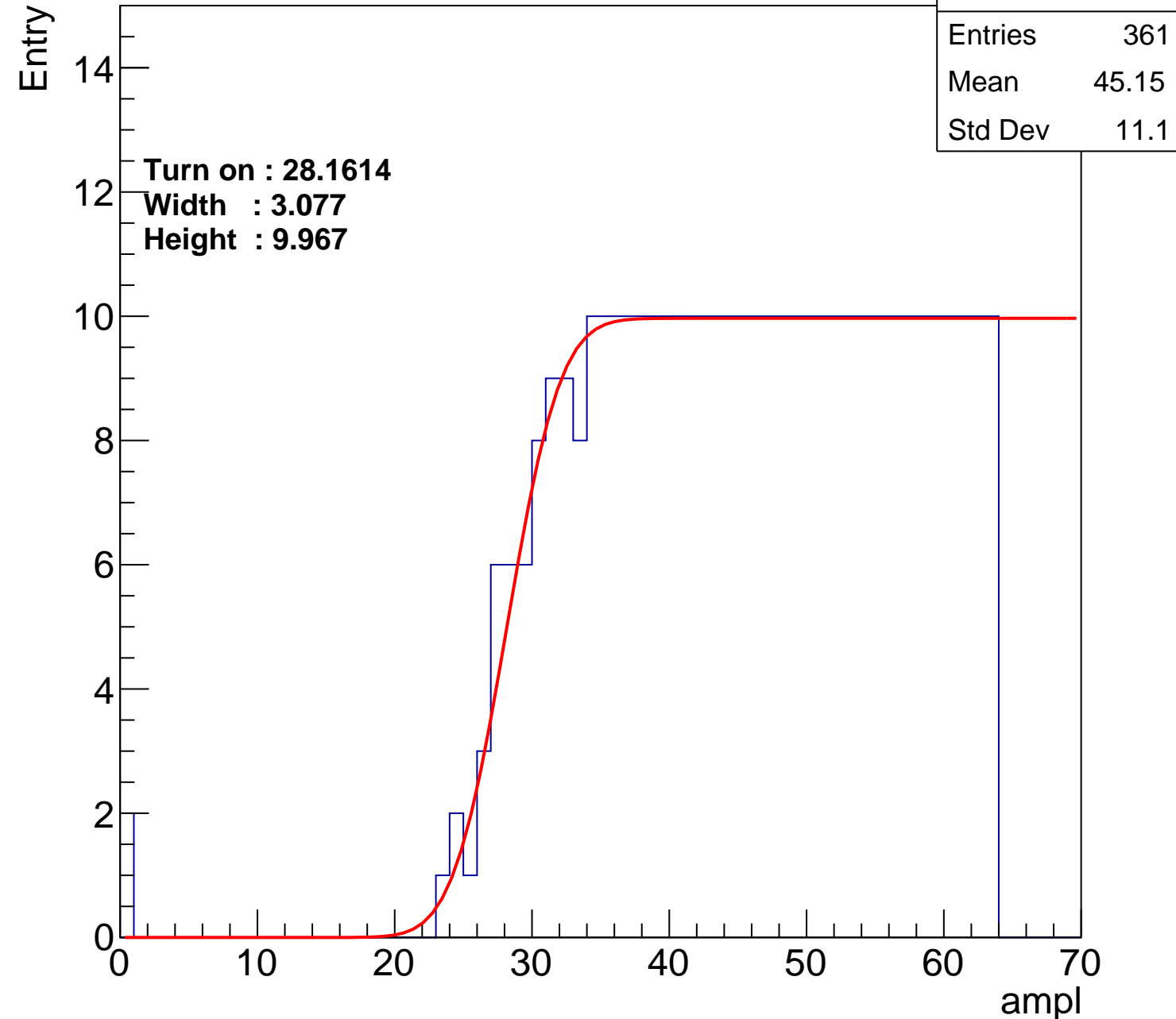
Width : 3.077

Height : 9.967

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch125

calib_packv5_042523_0143.root, FC#8, port C1

Entries	363
Mean	45.12
Std Dev	11.04

Turn on : 27.5839

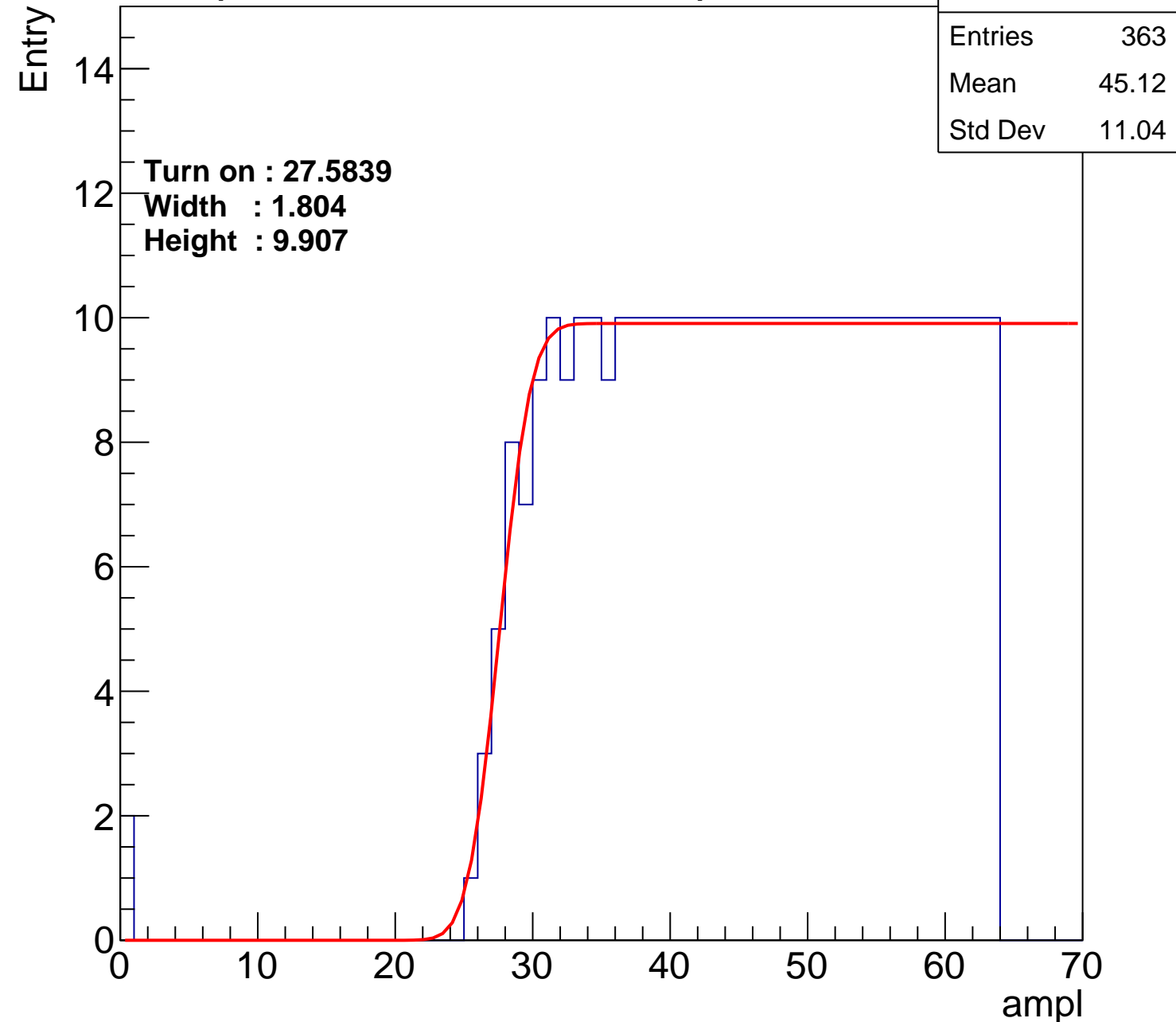
Width : 1.804

Height : 9.907

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch126

calib_packv5_042523_0143.root, FC#8, port C1

Entries	363
Mean	45.19
Std Dev	10.84

Turn on : 27.8208

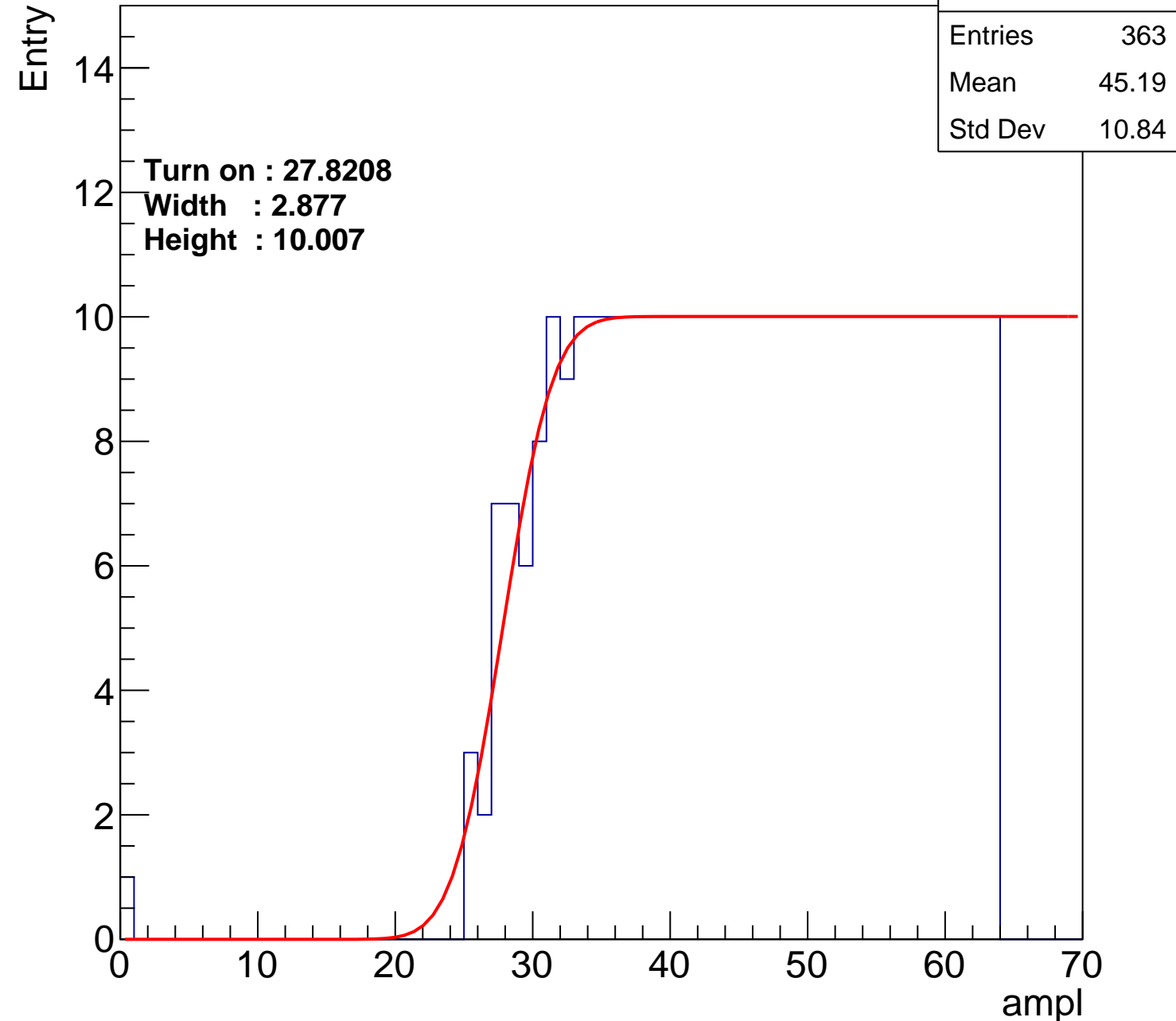
Width : 2.877

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch127

calib_packv5_042523_0143.root, FC#8, port C1

Entries	365
Mean	44.72
Std Dev	11.84

Turn on : 28.3297

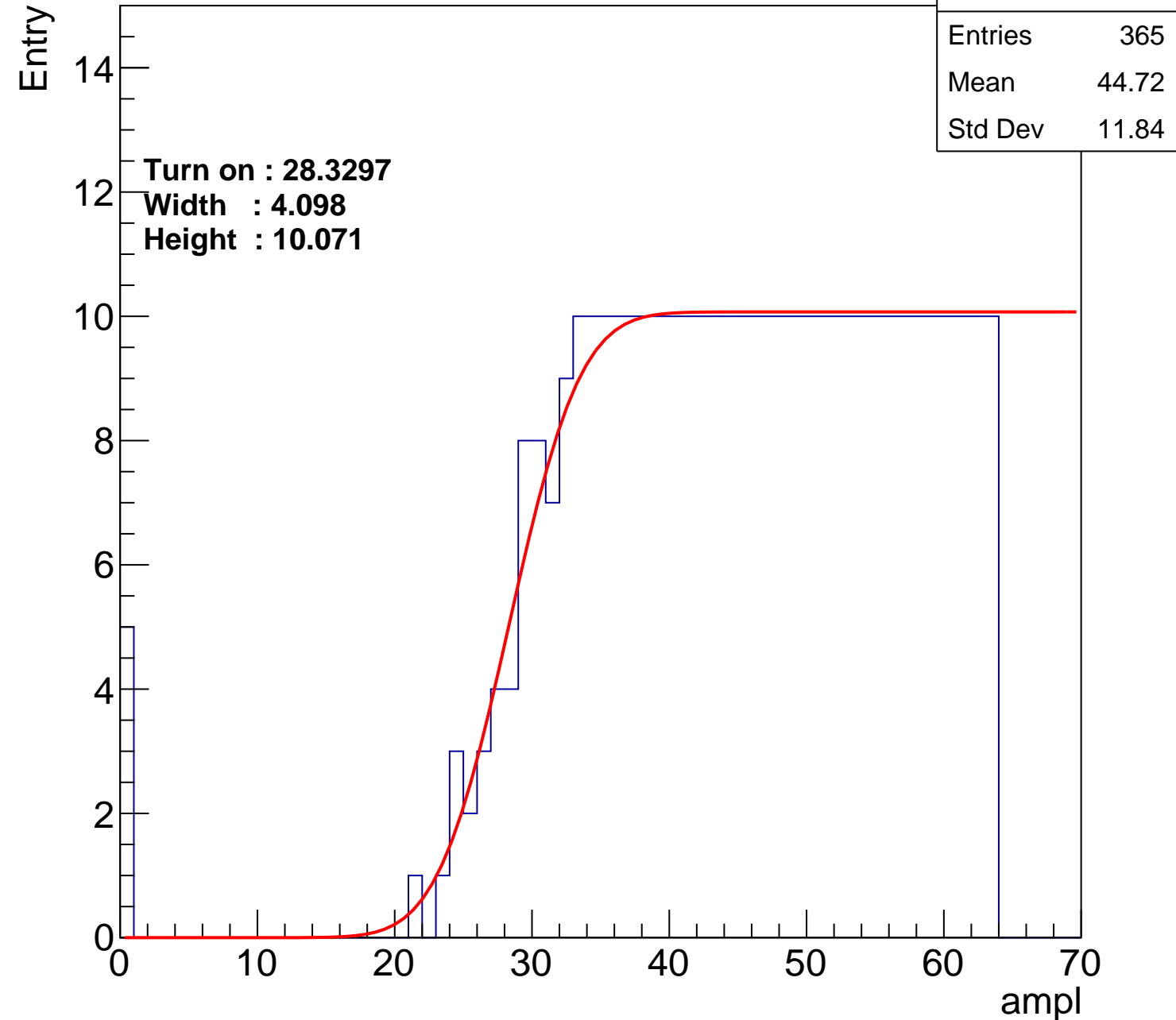
Width : 4.098

Height : 10.071

Entry

14
12
10
8
6
4
2
0

ampl



B0L002S, U7-ch127

calib_packv5_042523_0143.root, FC#8, port C1

Entries	365
Mean	44.72
Std Dev	11.84

Turn on : 28.3297

Width : 4.098

Height : 10.071

Entry

14
12
10
8
6
4
2
0

ampl

