



# B1L103S, U26-ch0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	468
Mean	37.88
Std Dev	17.77

Turn on : 22.9858

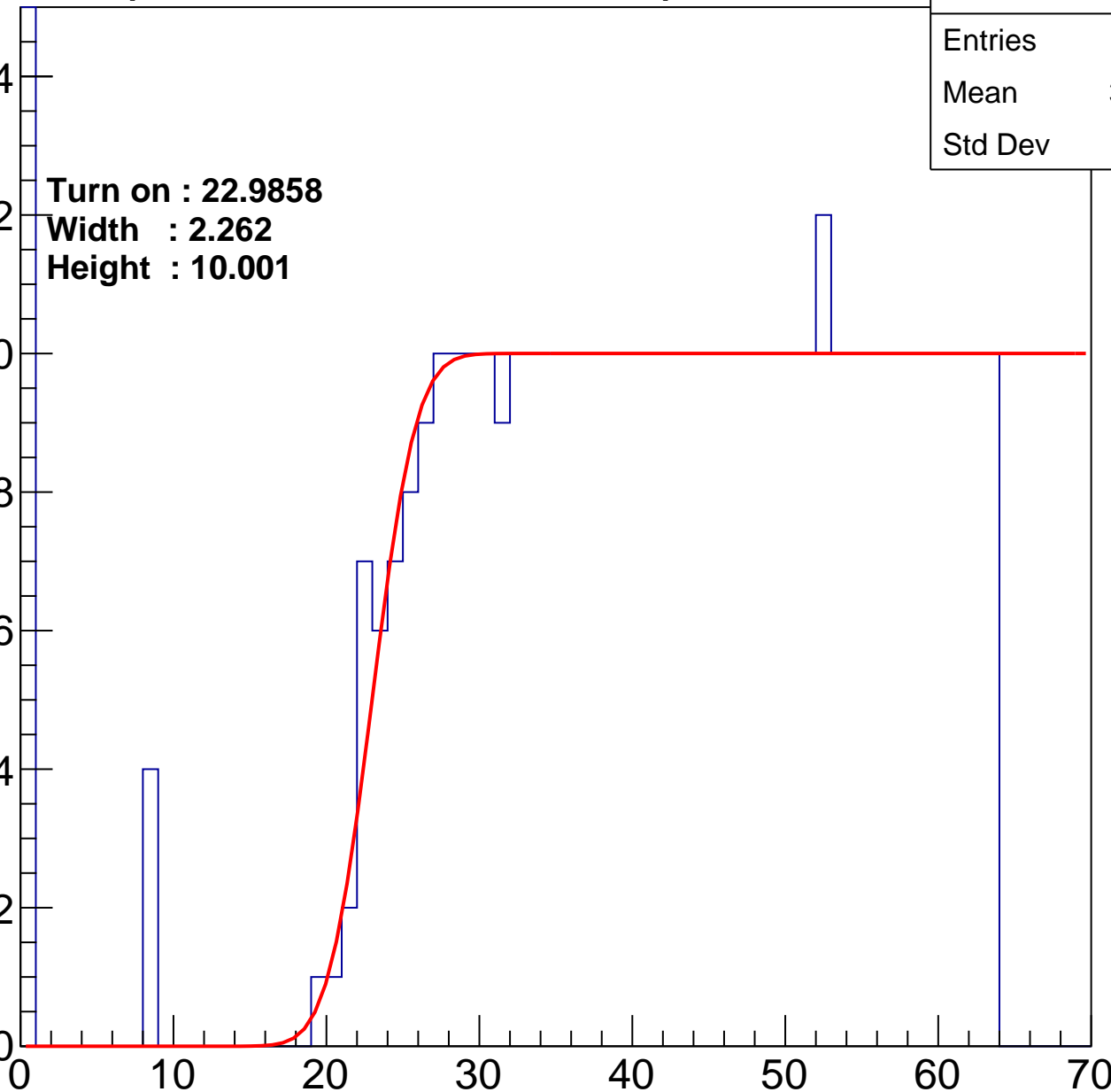
Width : 2.262

Height : 10.001

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch1

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	406
Mean	40.43
Std Dev	17.2

Turn on : 27.9239

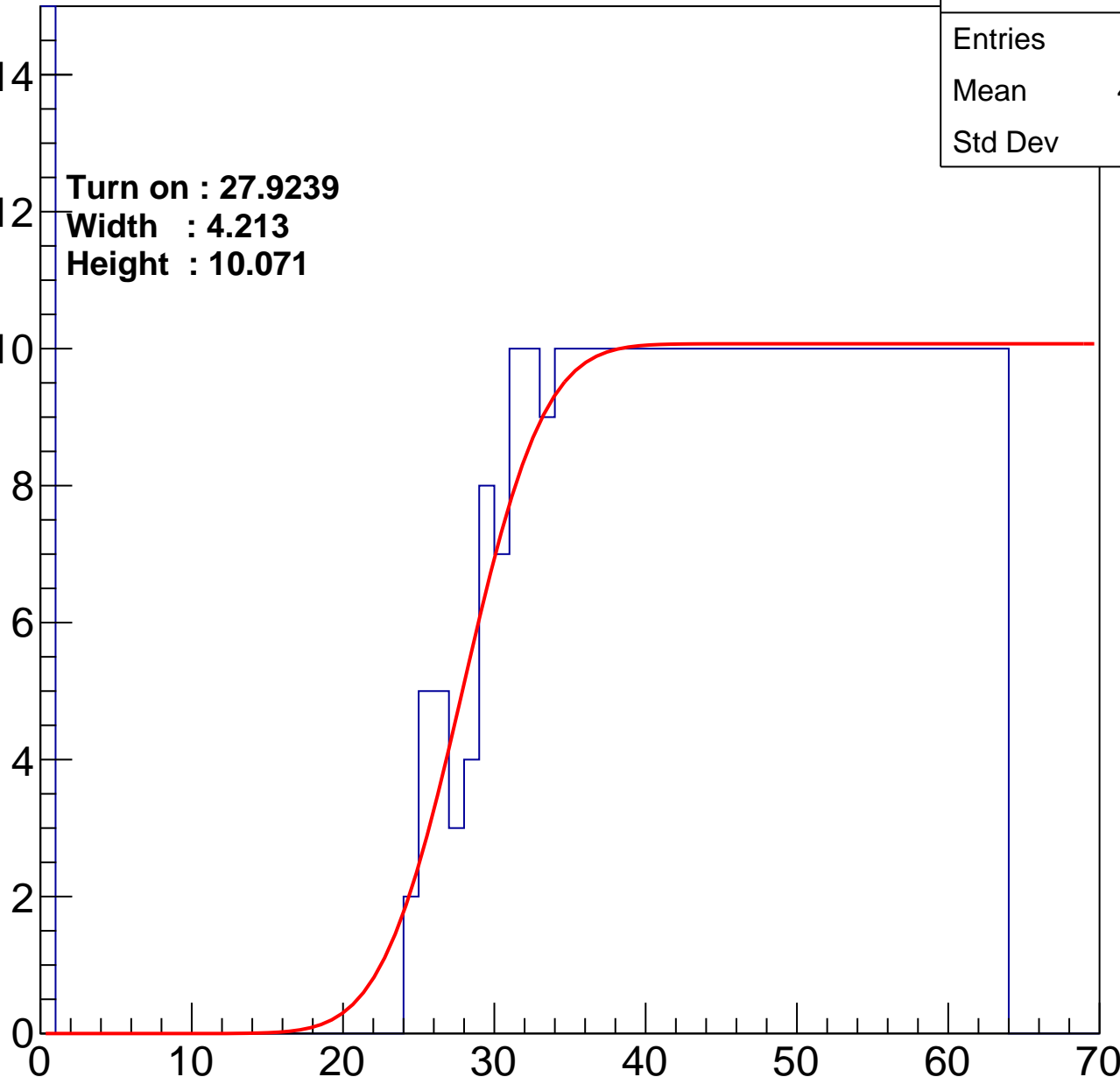
Width : 4.213

Height : 10.071

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch2

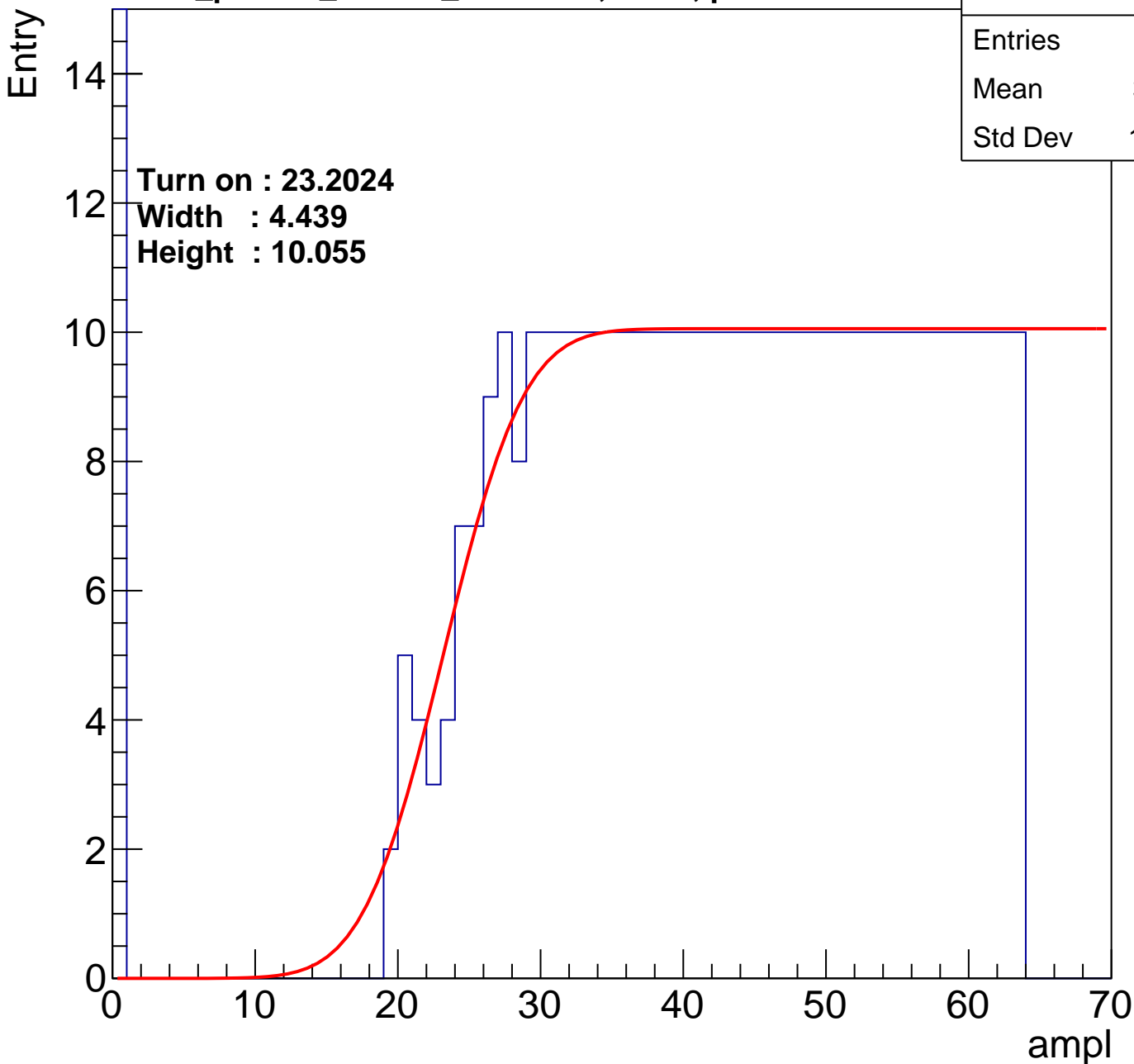
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	473
Mean	37.11
Std Dev	18.46

Turn on : 23.2024

Width : 4.439

Height : 10.055



# B1L103S, U26-ch3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	444
Mean	37.95
Std Dev	18.76

**Turn on : 26.7917**

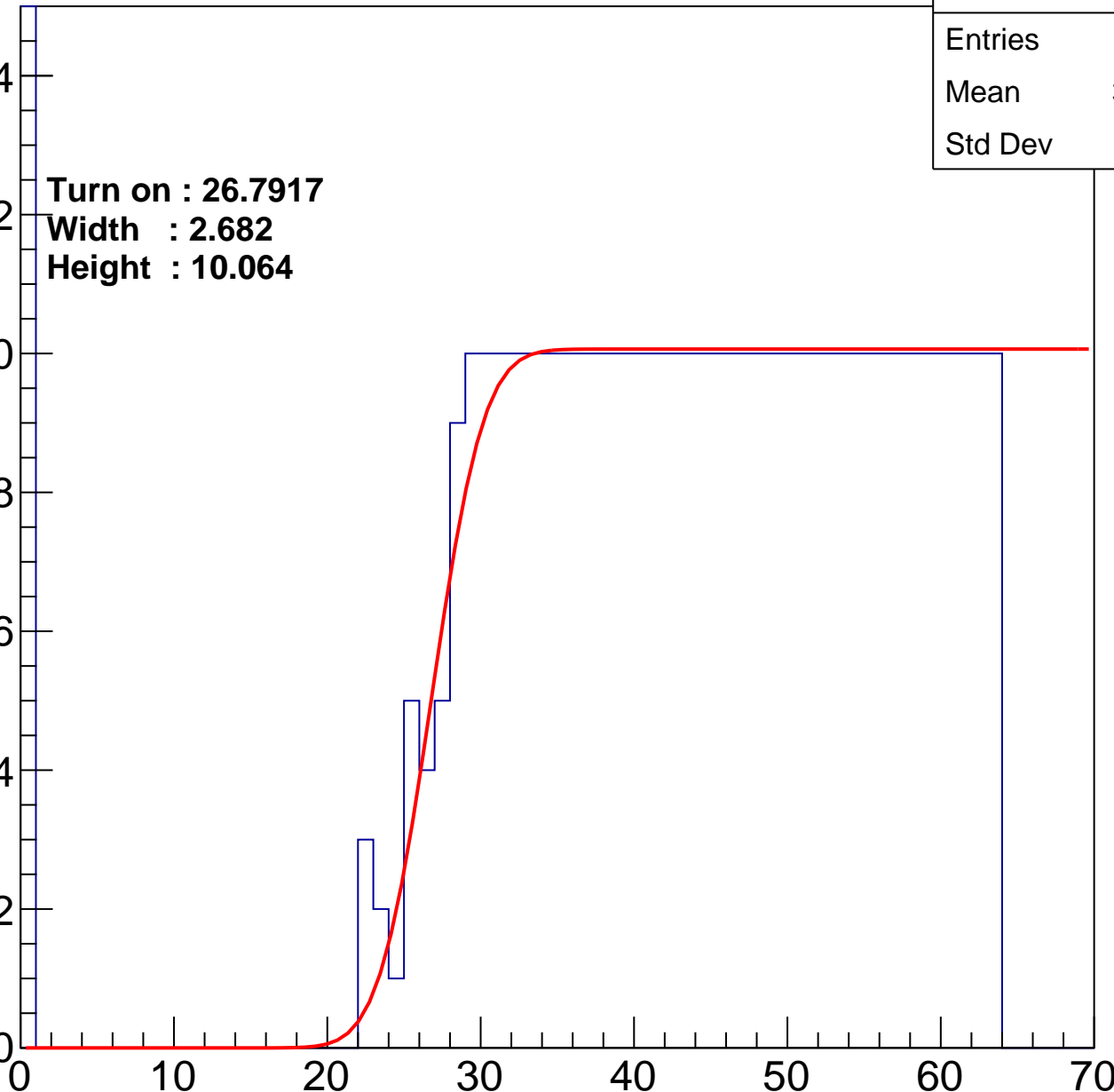
**Width : 2.682**

**Height : 10.064**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	424
Mean	39.89
Std Dev	17

Turn on : 25.5369

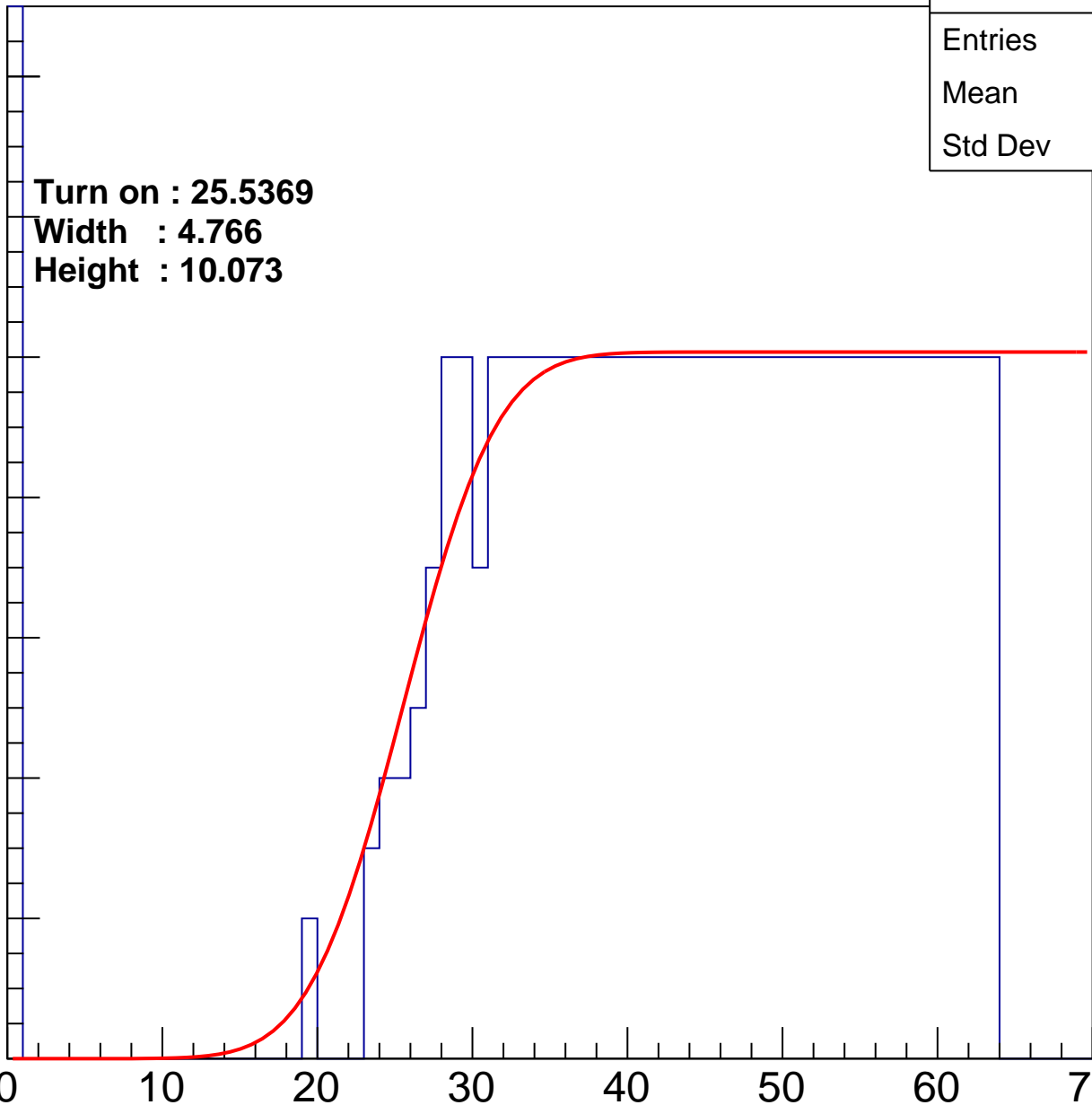
Width : 4.766

Height : 10.073

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch5

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	421
Mean	40.23
Std Dev	16.62

**Turn on : 26.0285**

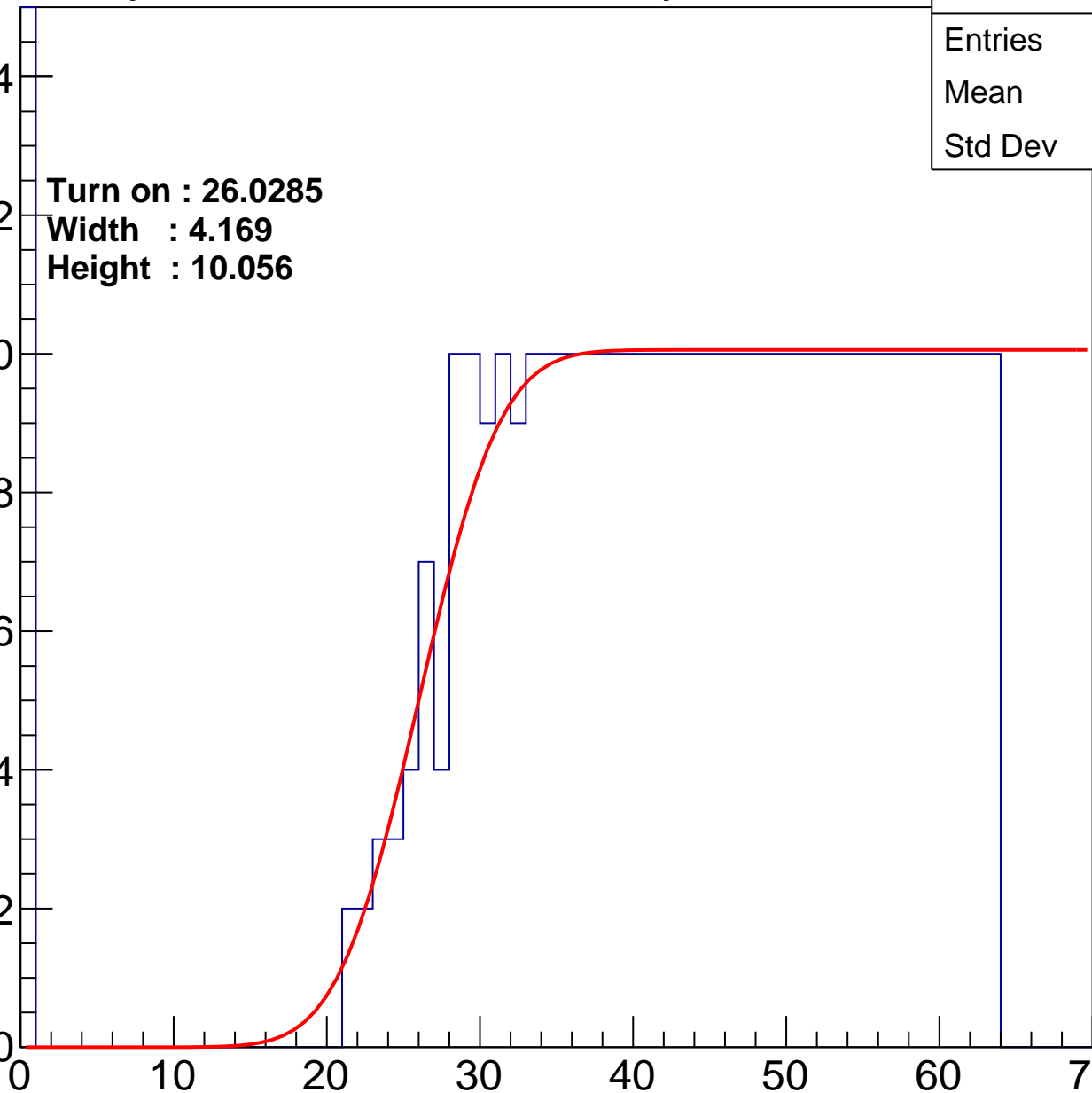
**Width : 4.169**

**Height : 10.056**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	422
Mean	39.65
Std Dev	17.52

Turn on : 26.5951

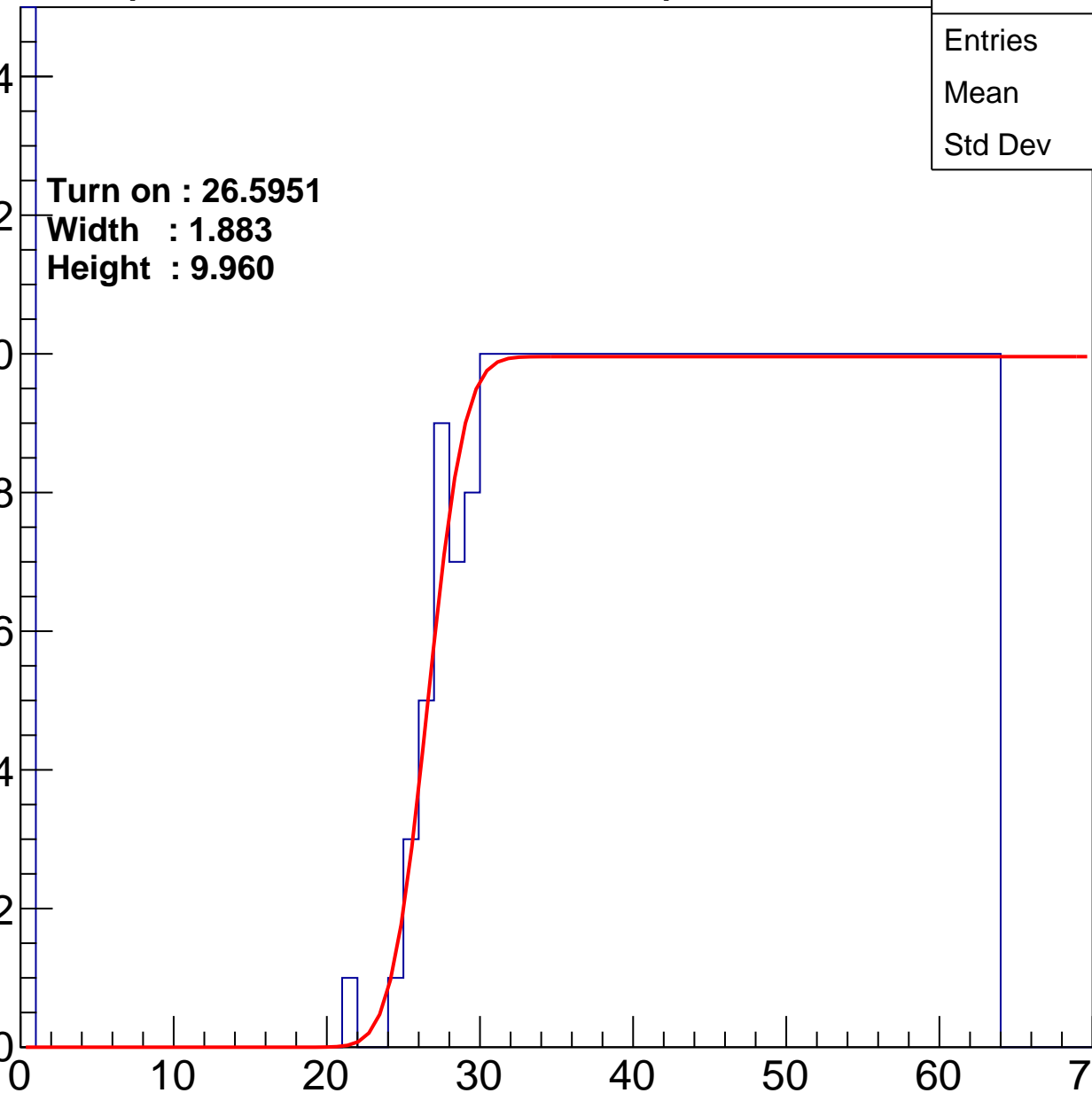
Width : 1.883

Height : 9.960

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U26-ch7

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	403
Mean	41.17
Std Dev	16.22

Turn on : 27.3915

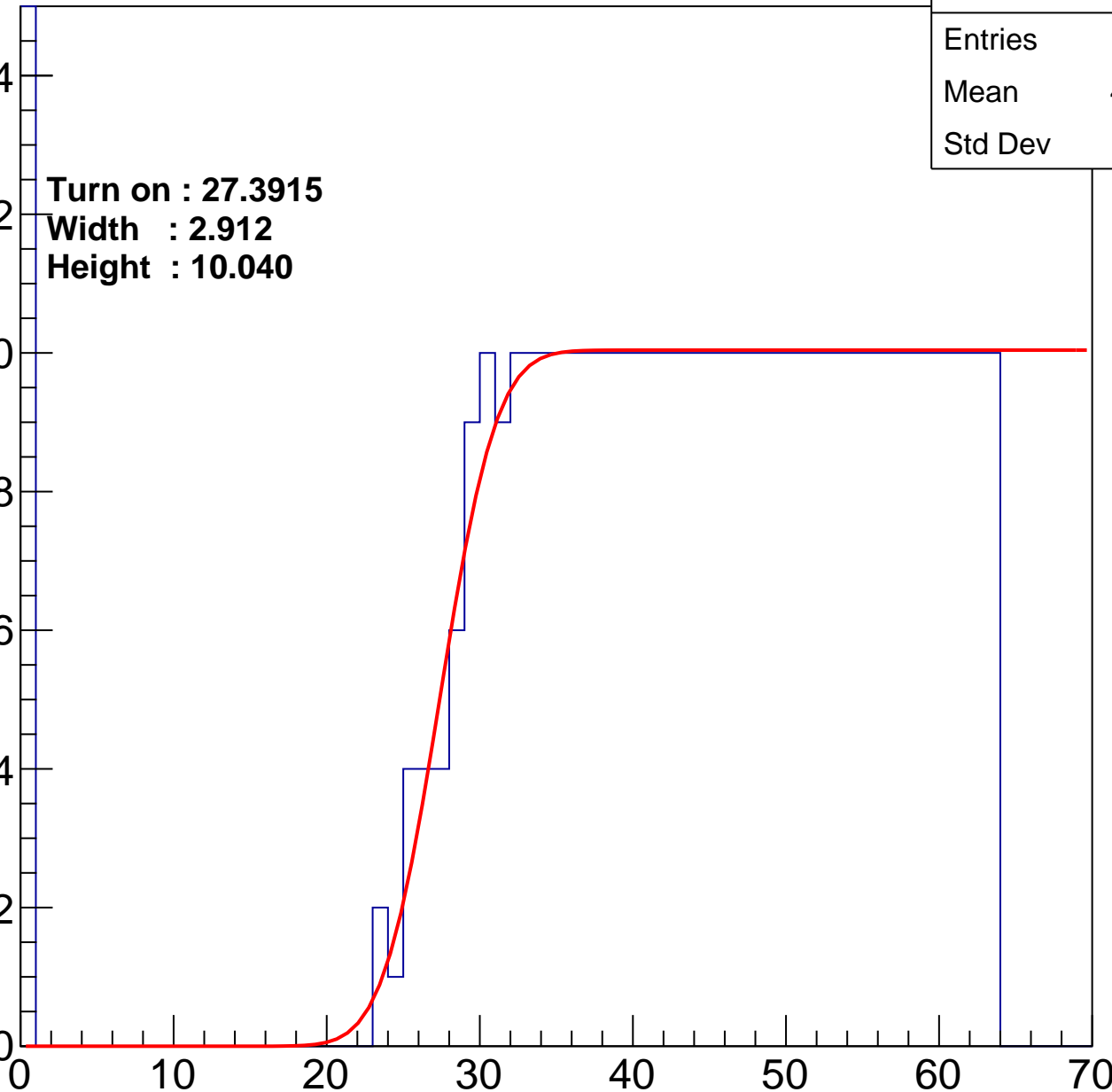
Width : 2.912

Height : 10.040

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch8

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	452
Mean	37.98
Std Dev	18.31

Turn on : 24.8156

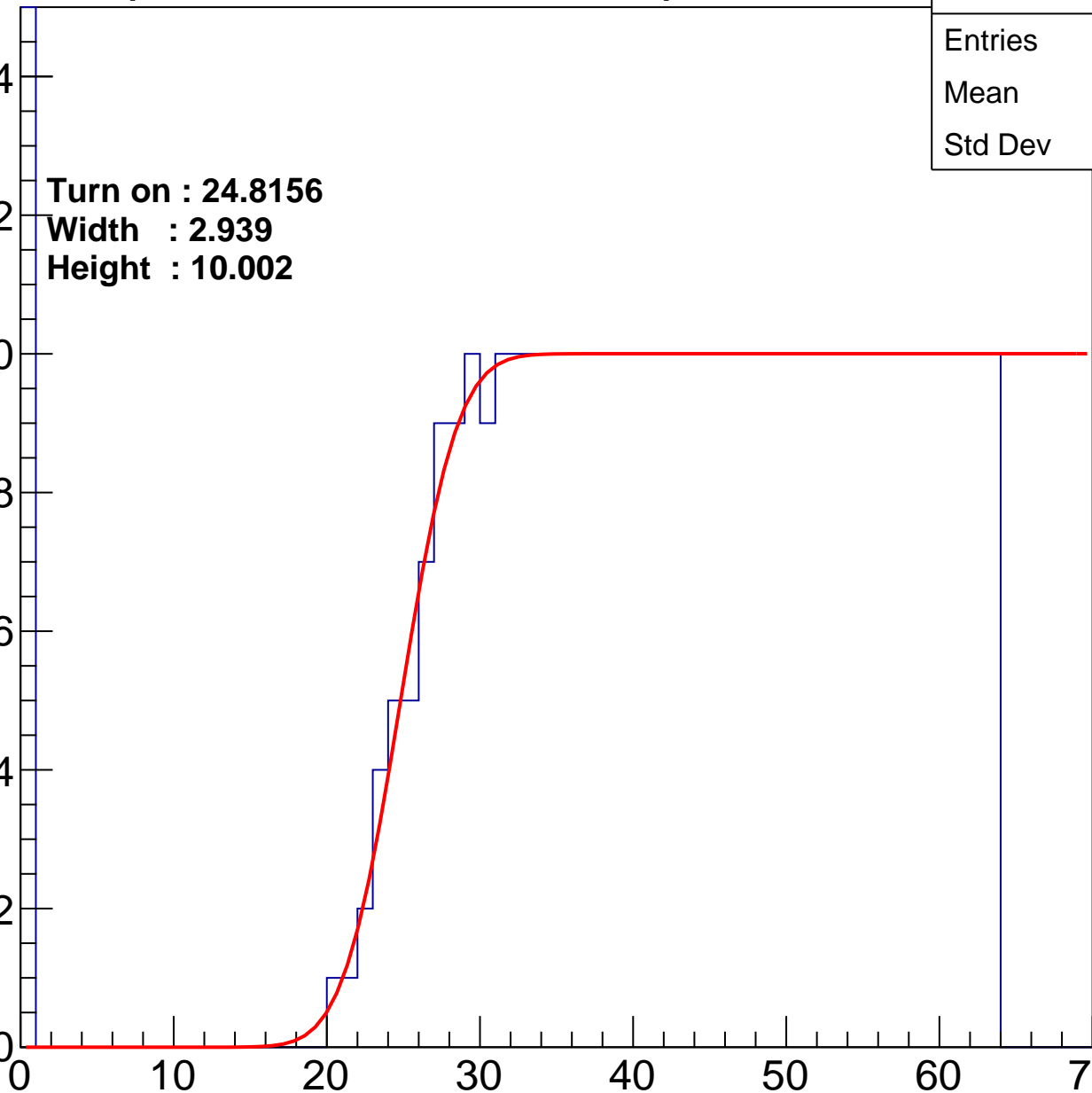
Width : 2.939

Height : 10.002

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch9

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	448
Mean	39
Std Dev	17.03

Turn on : 23.5365

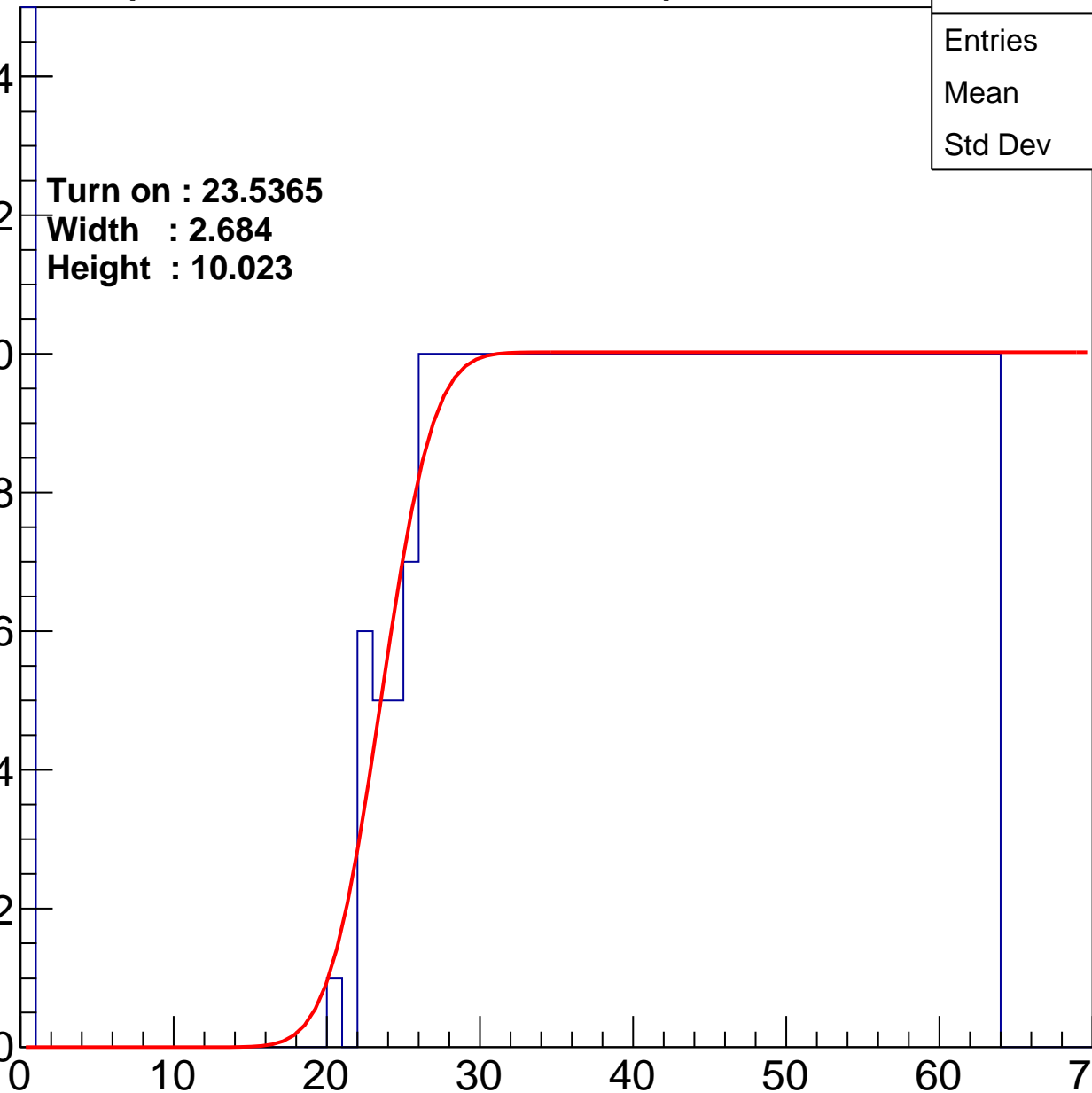
Width : 2.684

Height : 10.023

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch10

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	426
Mean	39.51
Std Dev	17.42

Turn on : 26.2042

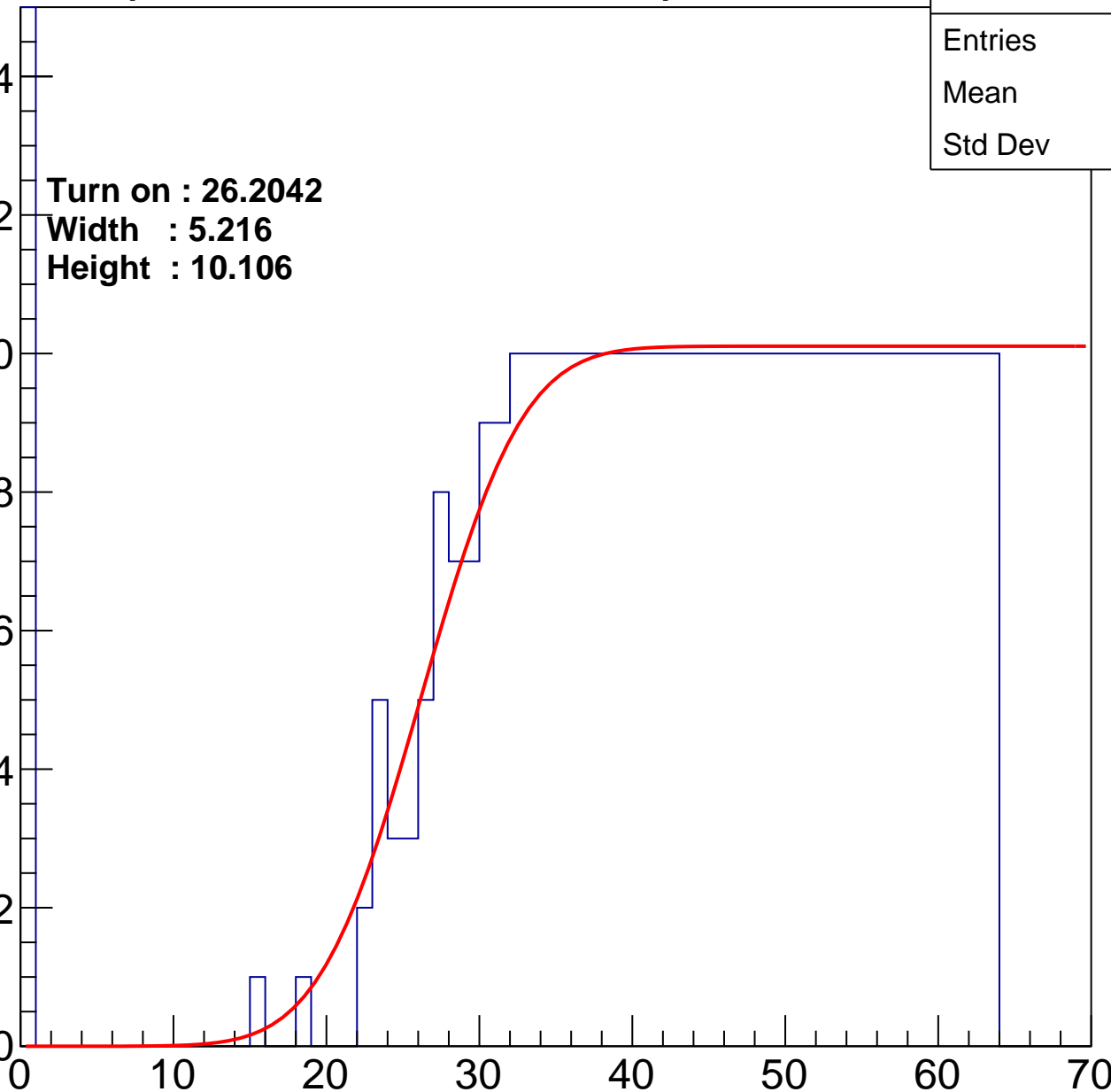
Width : 5.216

Height : 10.106

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch11

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	430
Mean	39.39
Std Dev	17.46

**Turn on : 26.2256**

**Width : 0.586**

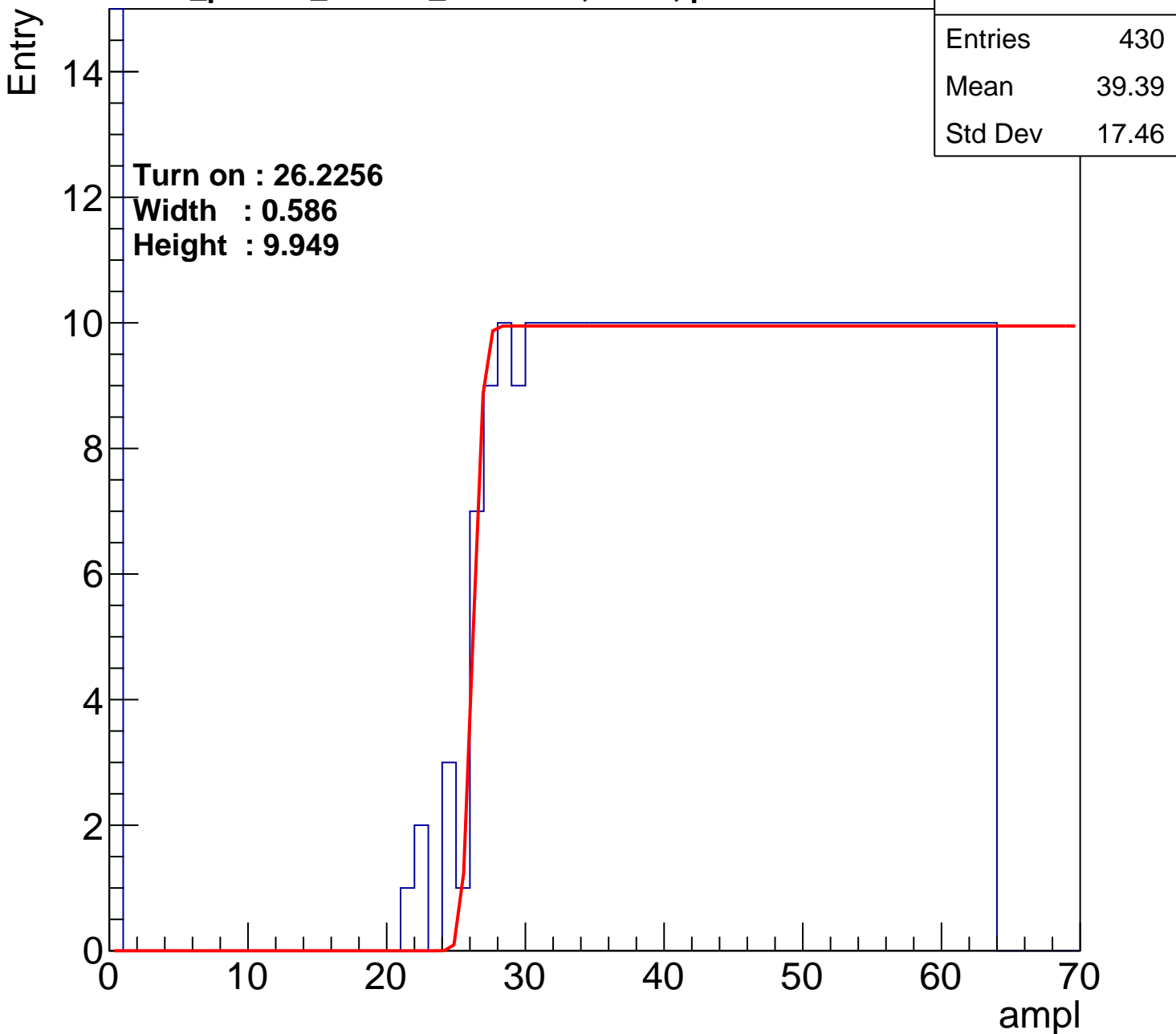
**Height : 9.949**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch12

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	451
Mean	37.91
Std Dev	18.47

Turn on : 25.0996

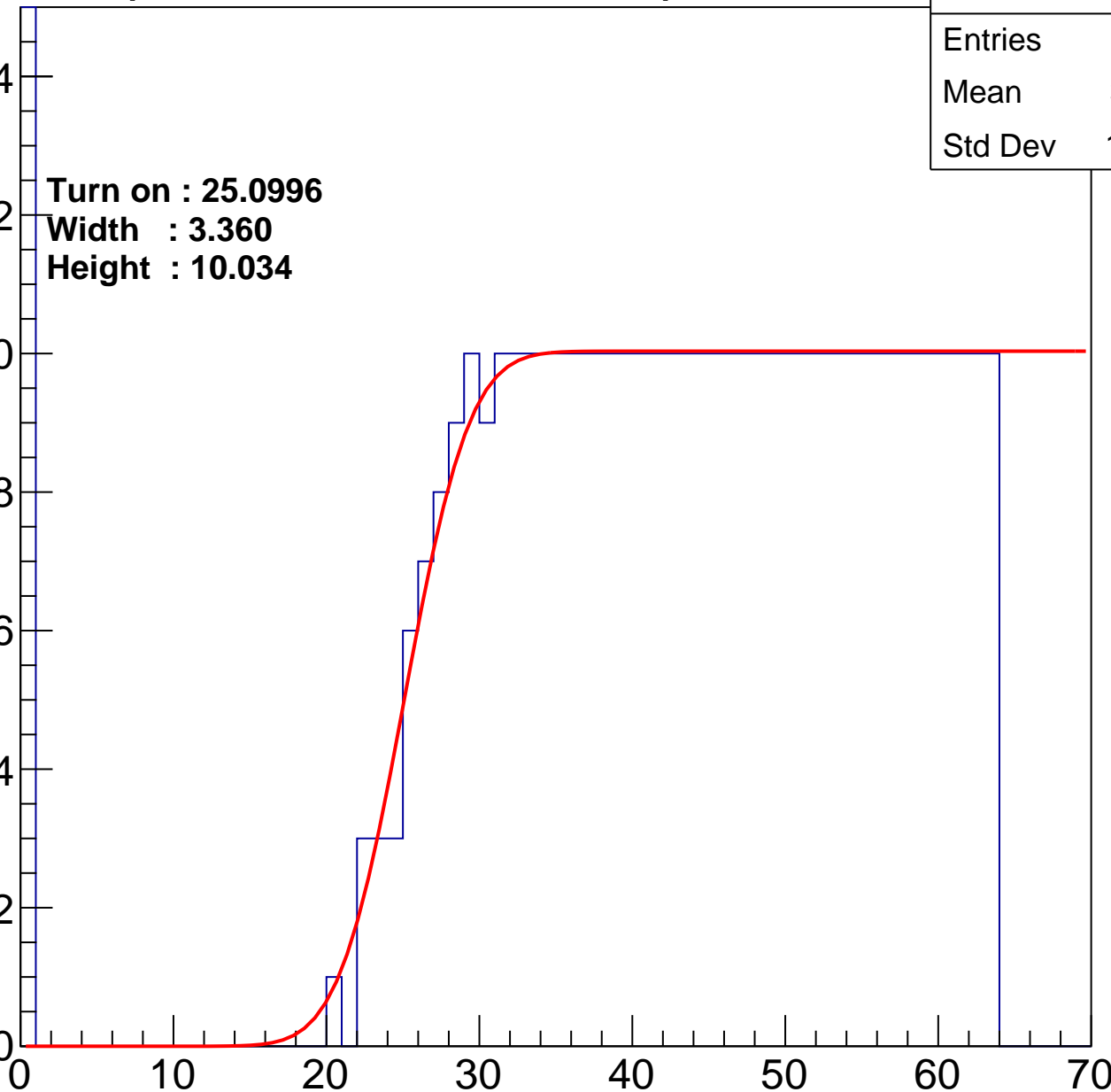
Width : 3.360

Height : 10.034

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch13

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	390
Mean	41.06
Std Dev	17.2

Turn on : 29.5314

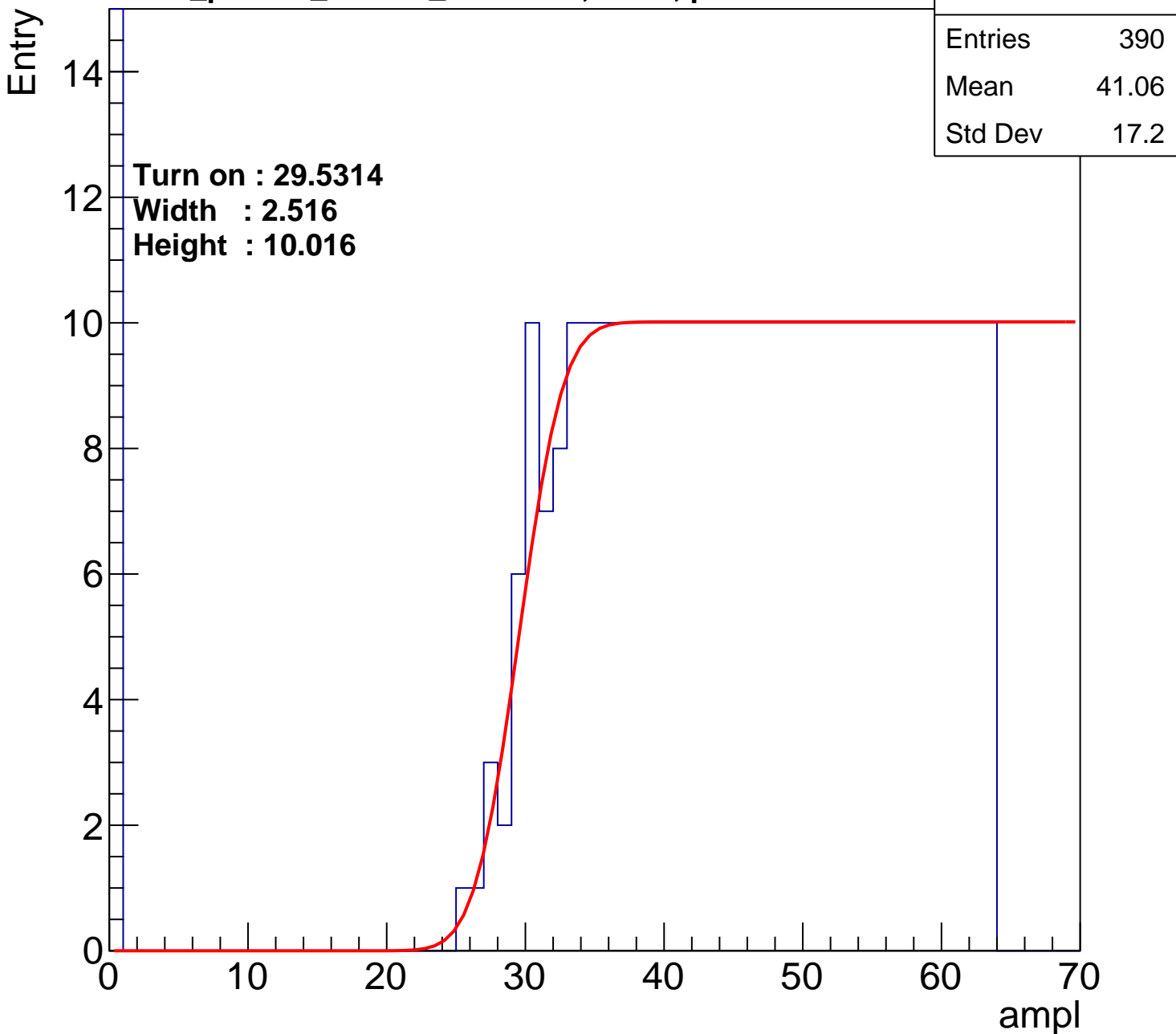
Width : 2.516

Height : 10.016

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch14

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	440
Mean	38.47
Std Dev	18.25

**Turn on : 26.2105**

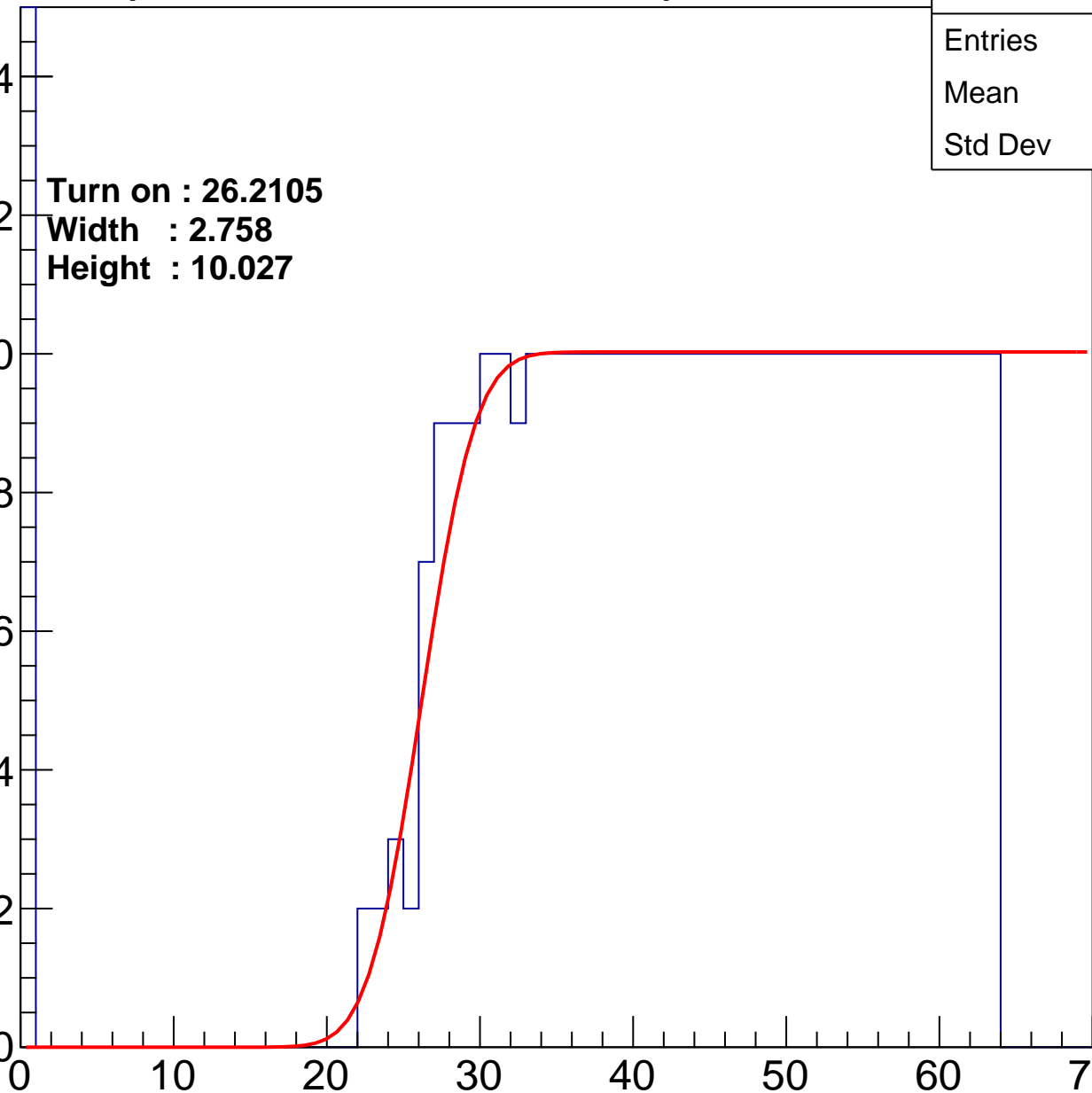
**Width : 2.758**

**Height : 10.027**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U26-ch15

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	429
Mean	39.29
Std Dev	17.66

Turn on : 26.9294

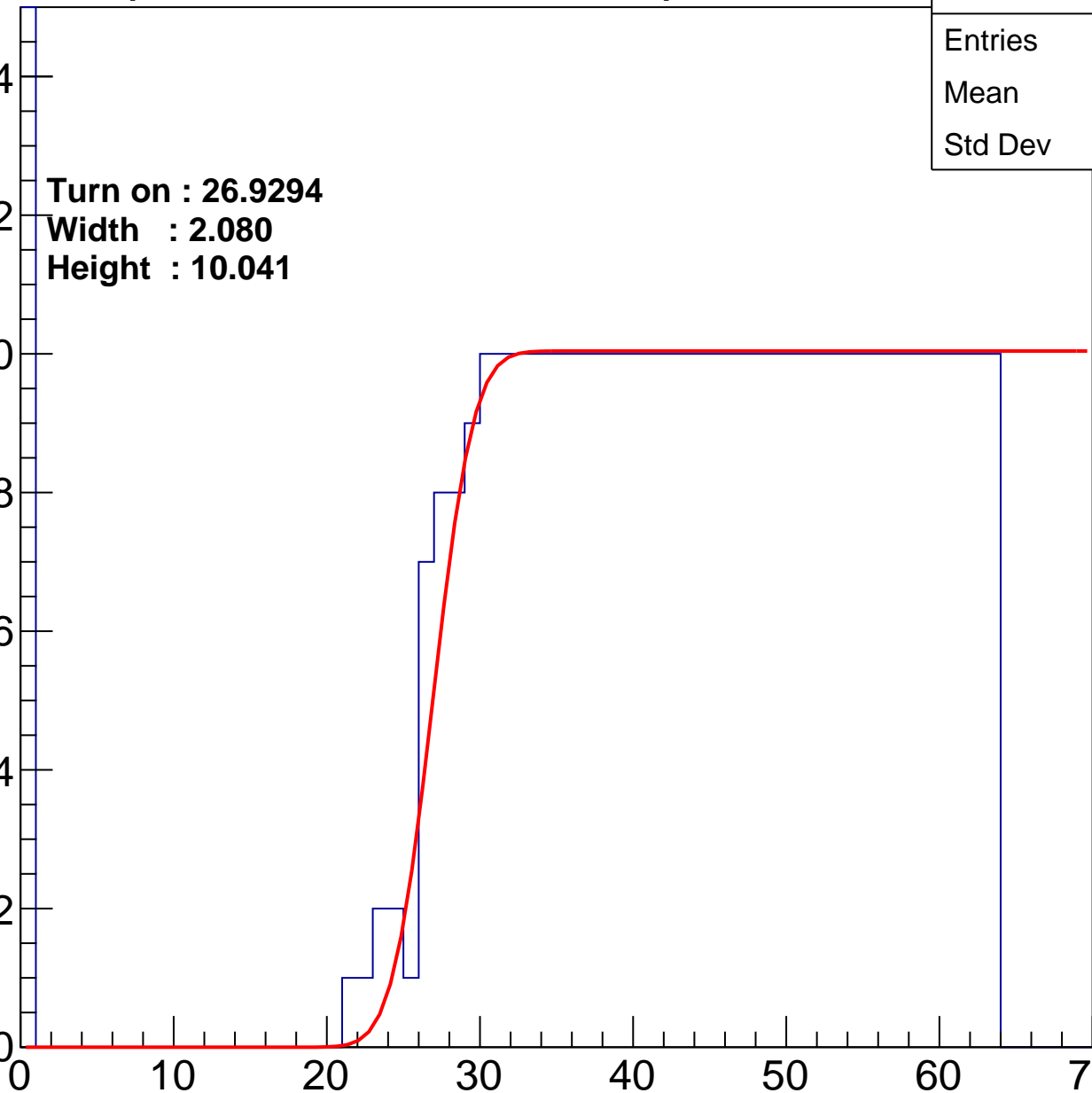
Width : 2.080

Height : 10.041

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch16

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	436
Mean	39.98
Std Dev	16.26

Turn on : 25.2142

Width : 3.134

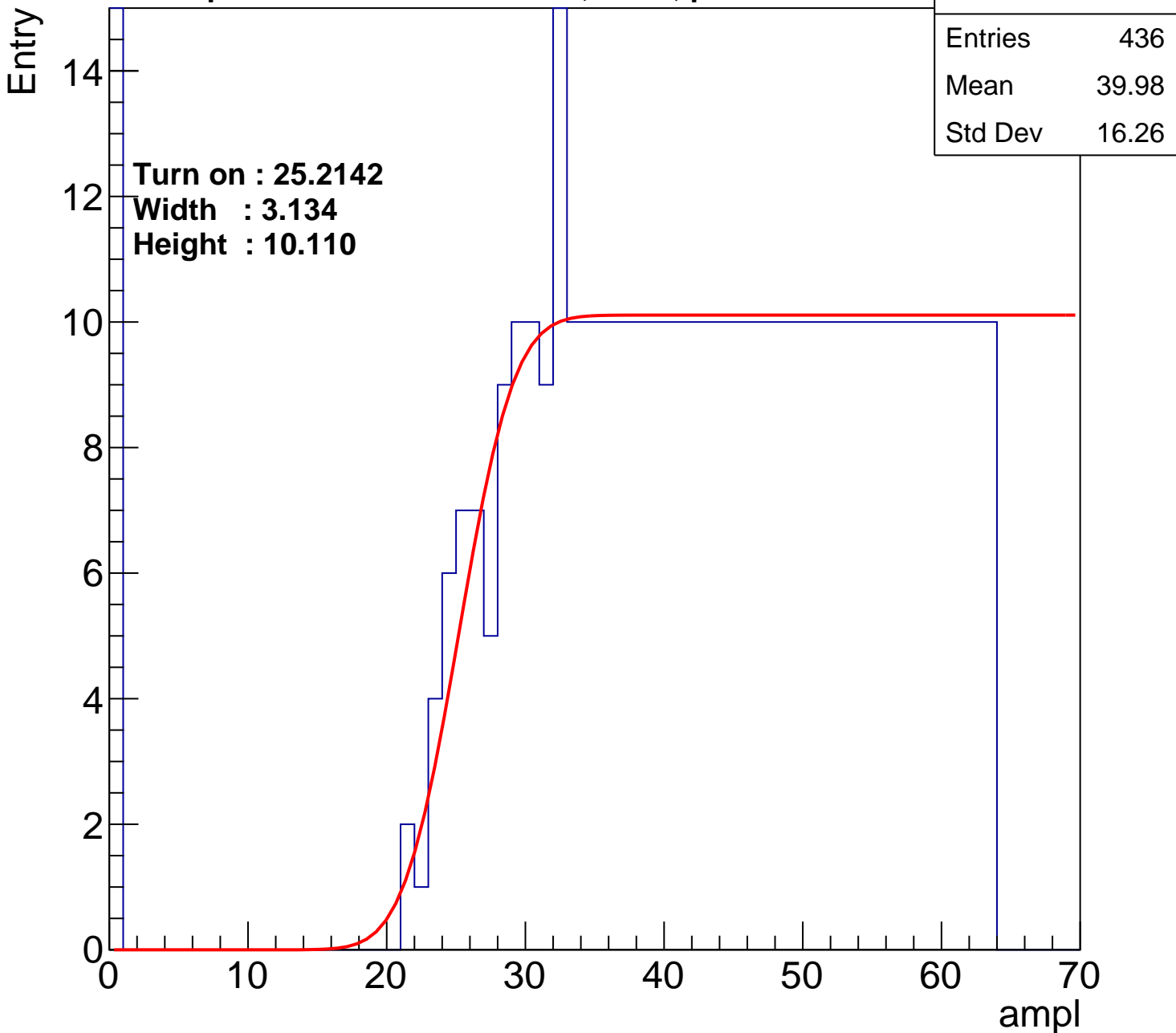
Height : 10.110

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch17

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	406
Mean	40.5
Std Dev	17.09

Turn on : 26.8968

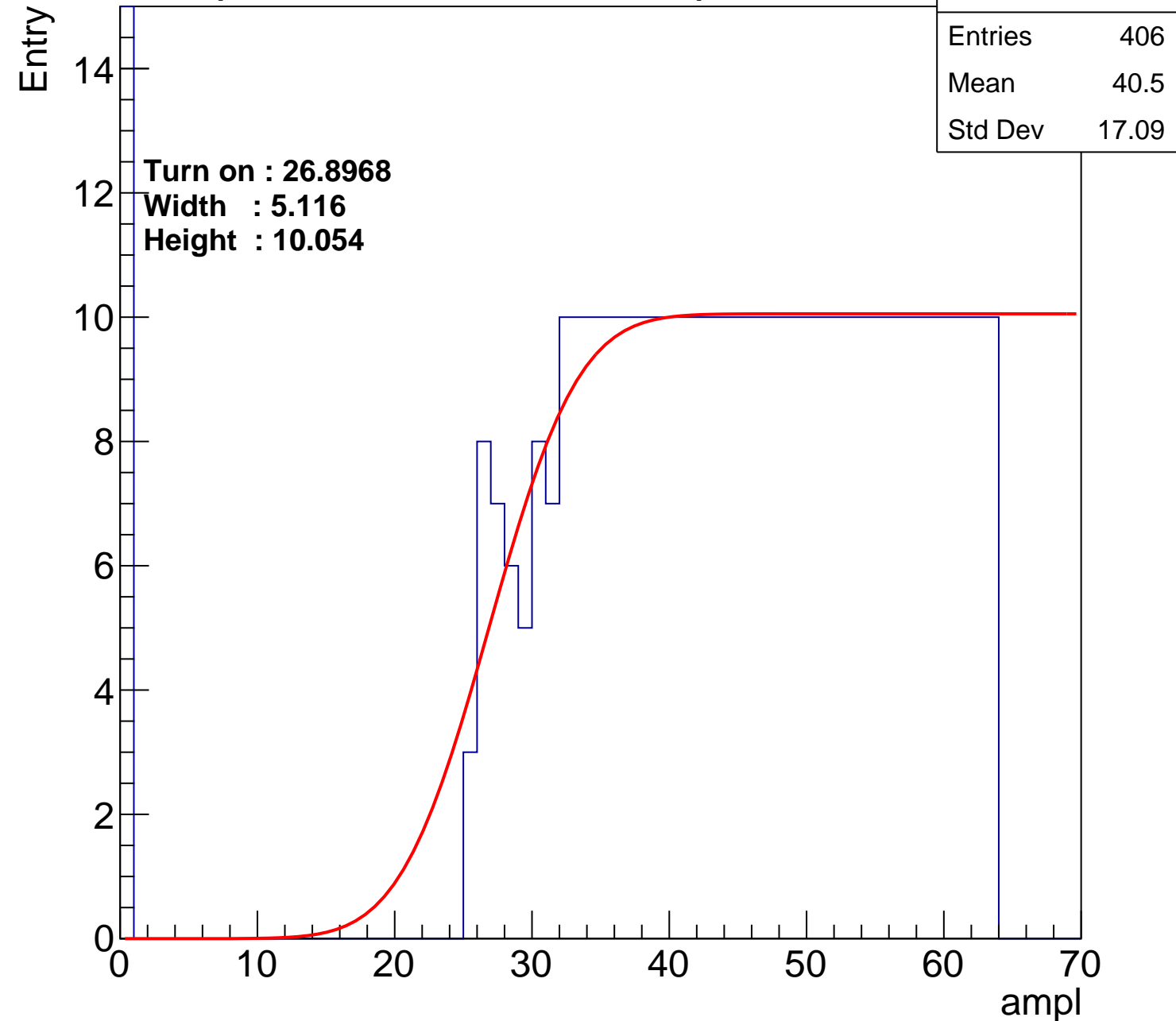
Width : 5.116

Height : 10.054

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch18

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	420
Mean	39.92
Std Dev	17.19

Turn on : 26.7960

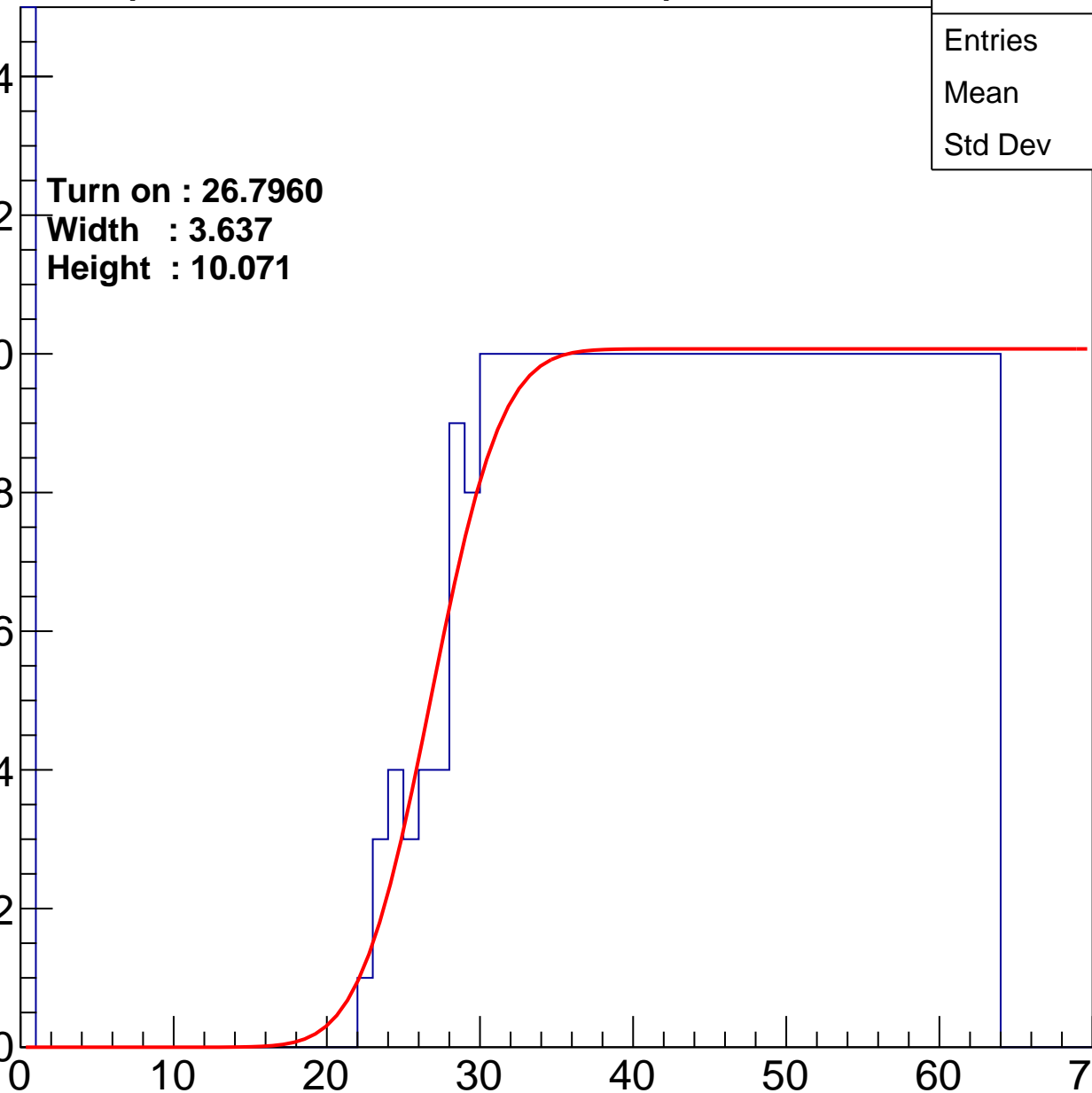
Width : 3.637

Height : 10.071

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch19

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	411
Mean	39.97
Std Dev	17.64

Turn on : 27.8789

Width : 2.743

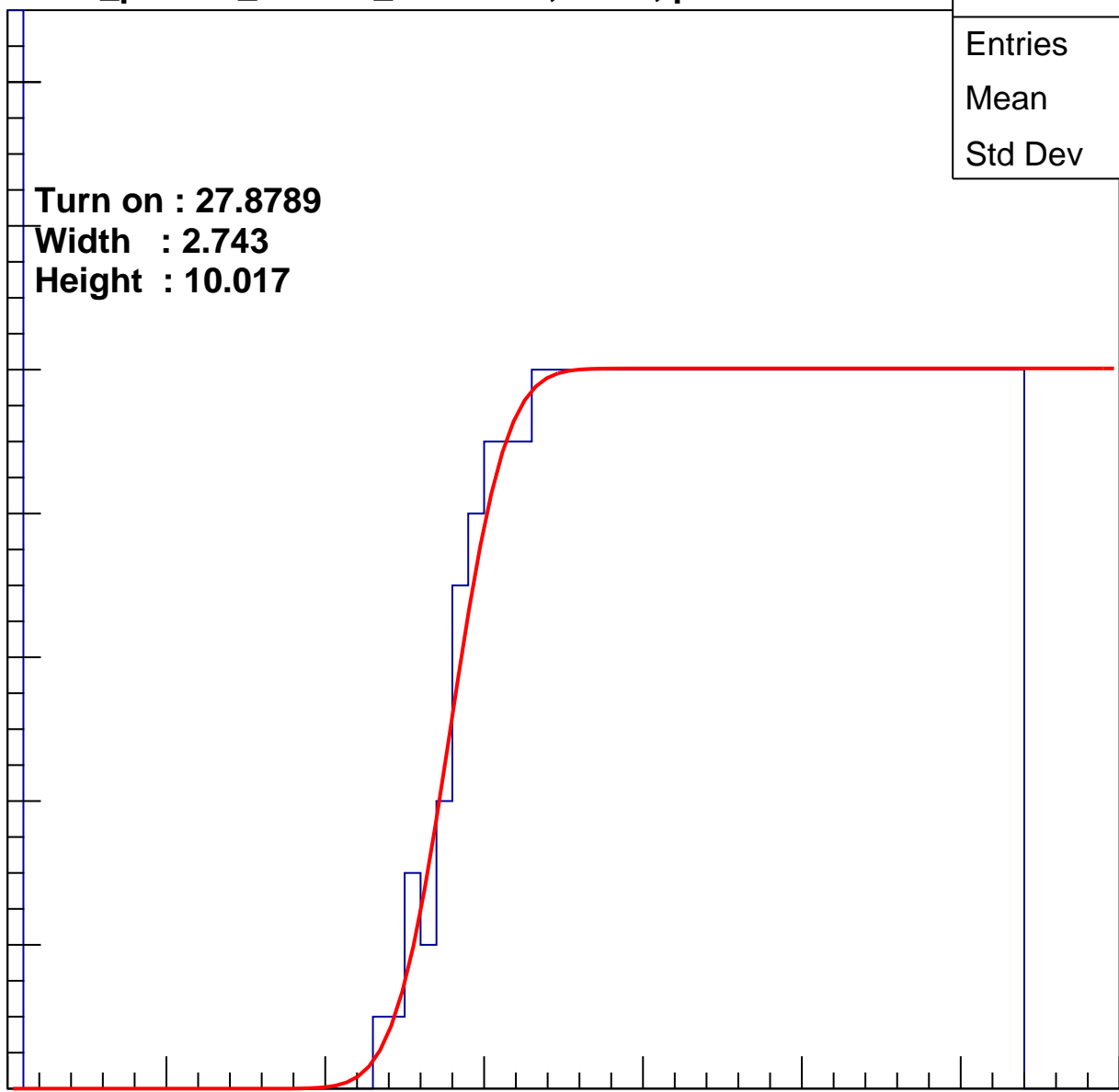
Height : 10.017

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U26-ch20

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	444
Mean	39.09
Std Dev	17.05

Turn on : 25.2217

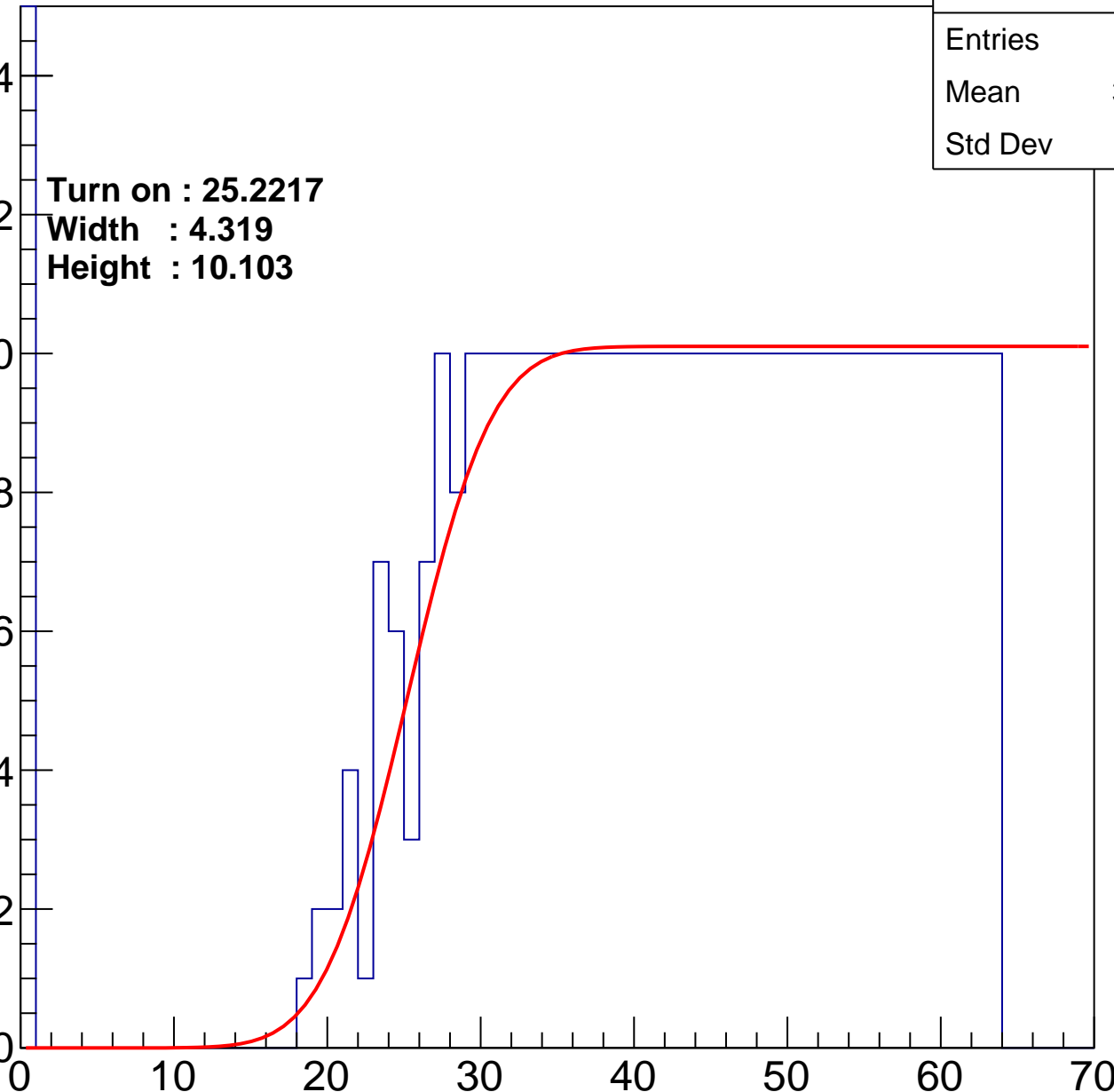
Width : 4.319

Height : 10.103

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch21

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	401
Mean	40.96
Std Dev	16.68

Turn on : 27.8655

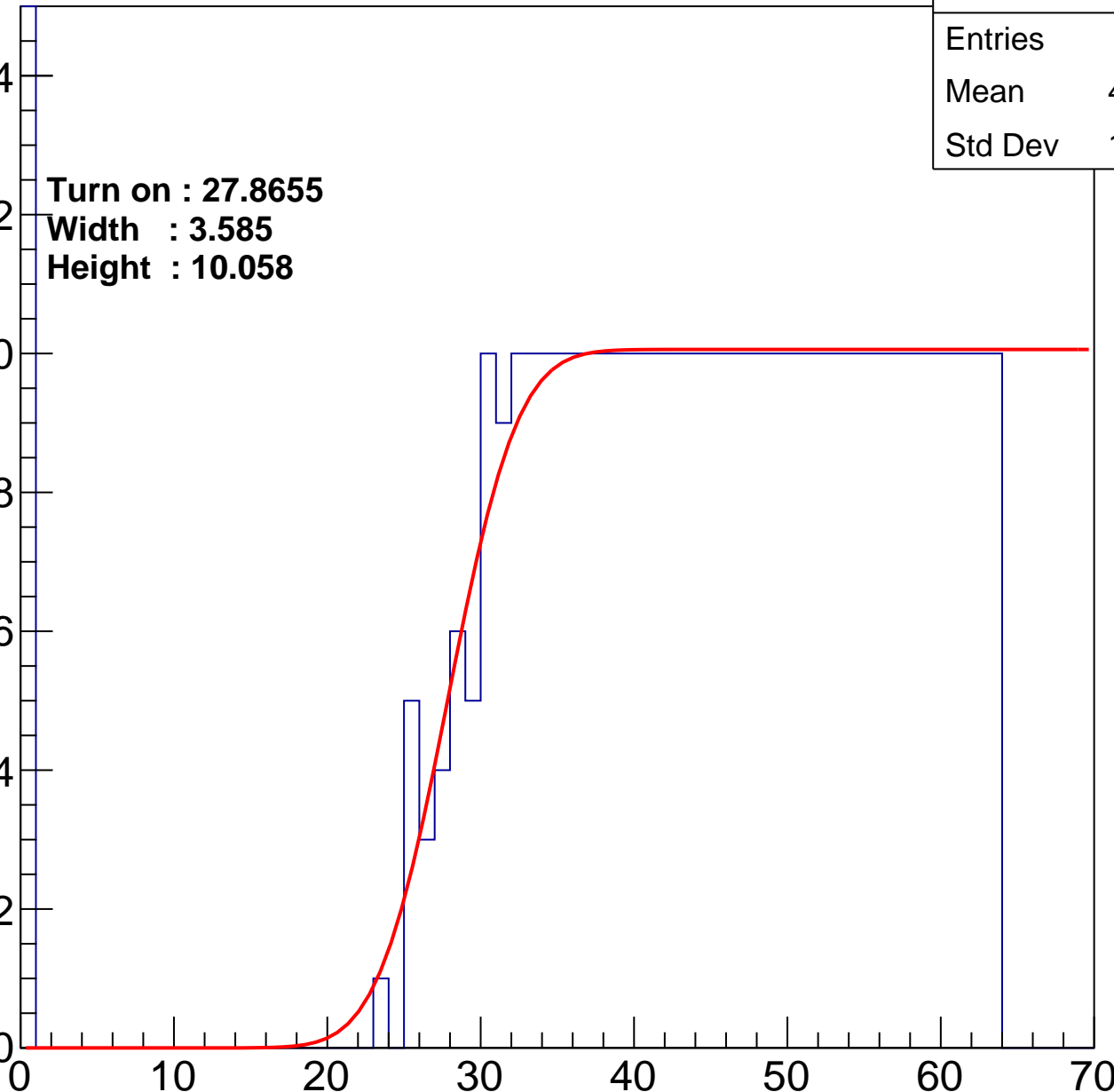
Width : 3.585

Height : 10.058

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch22

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	443
Mean	38.49
Std Dev	18.06

**Turn on : 25.3300**

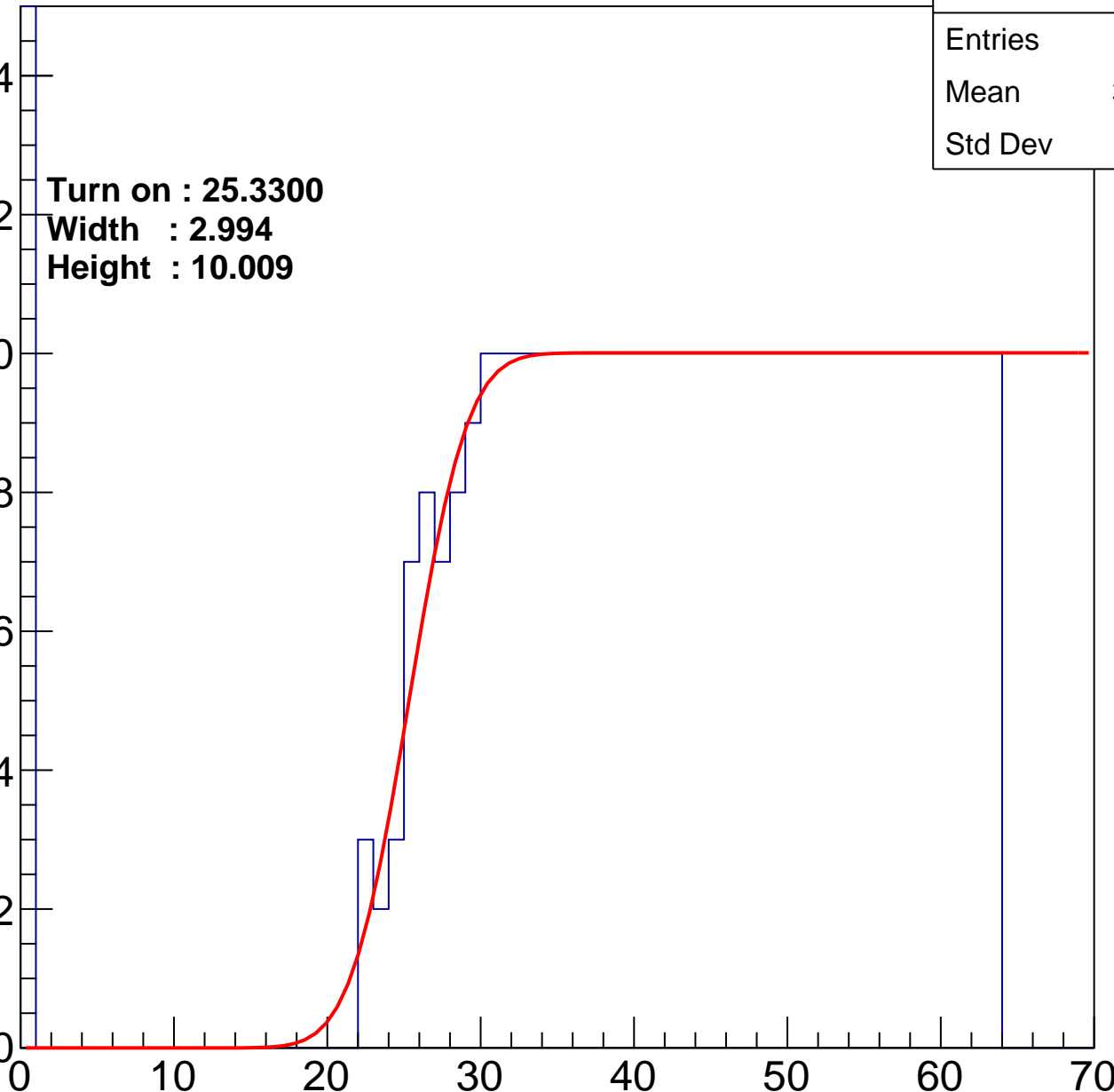
**Width : 2.994**

**Height : 10.009**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U26-ch23

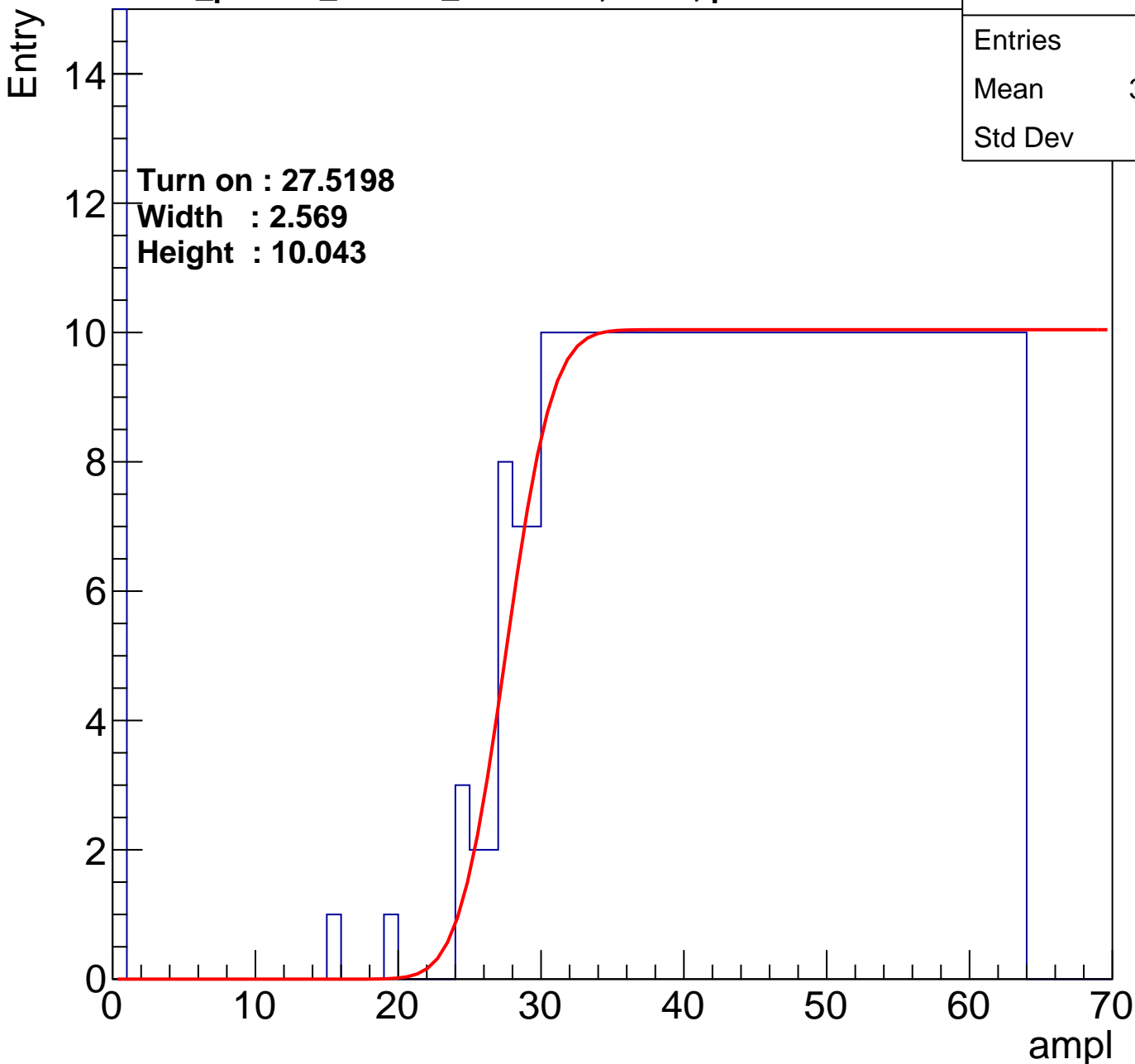
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	418
Mean	39.79
Std Dev	17.51

Turn on : 27.5198

Width : 2.569

Height : 10.043



# B1L103S, U26-ch24

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	467
Mean	37.82
Std Dev	17.81

Turn on : 23.0376

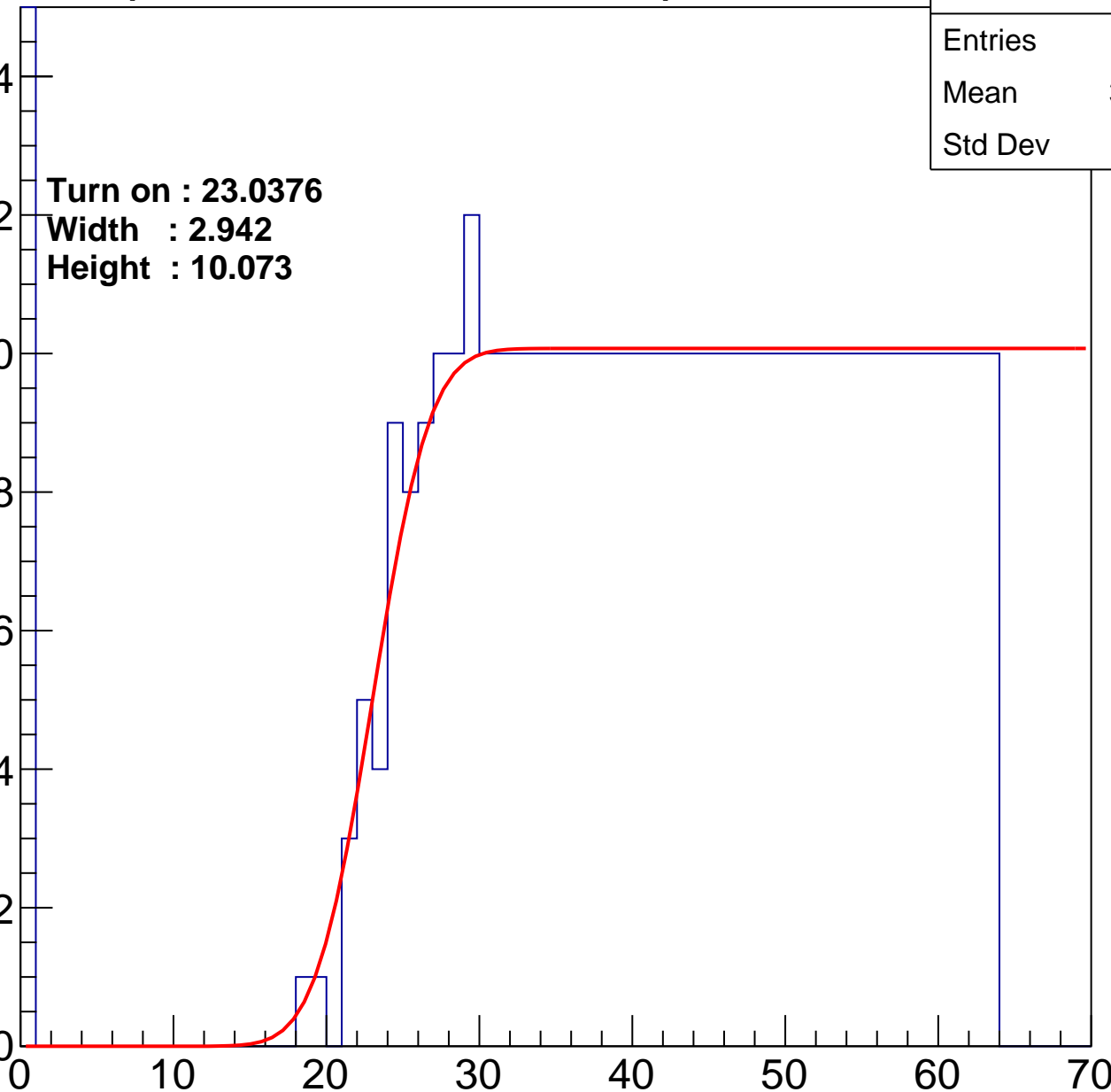
Width : 2.942

Height : 10.073

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch25

calib\_packv5\_041523\_1651.root, FC#0, port C2

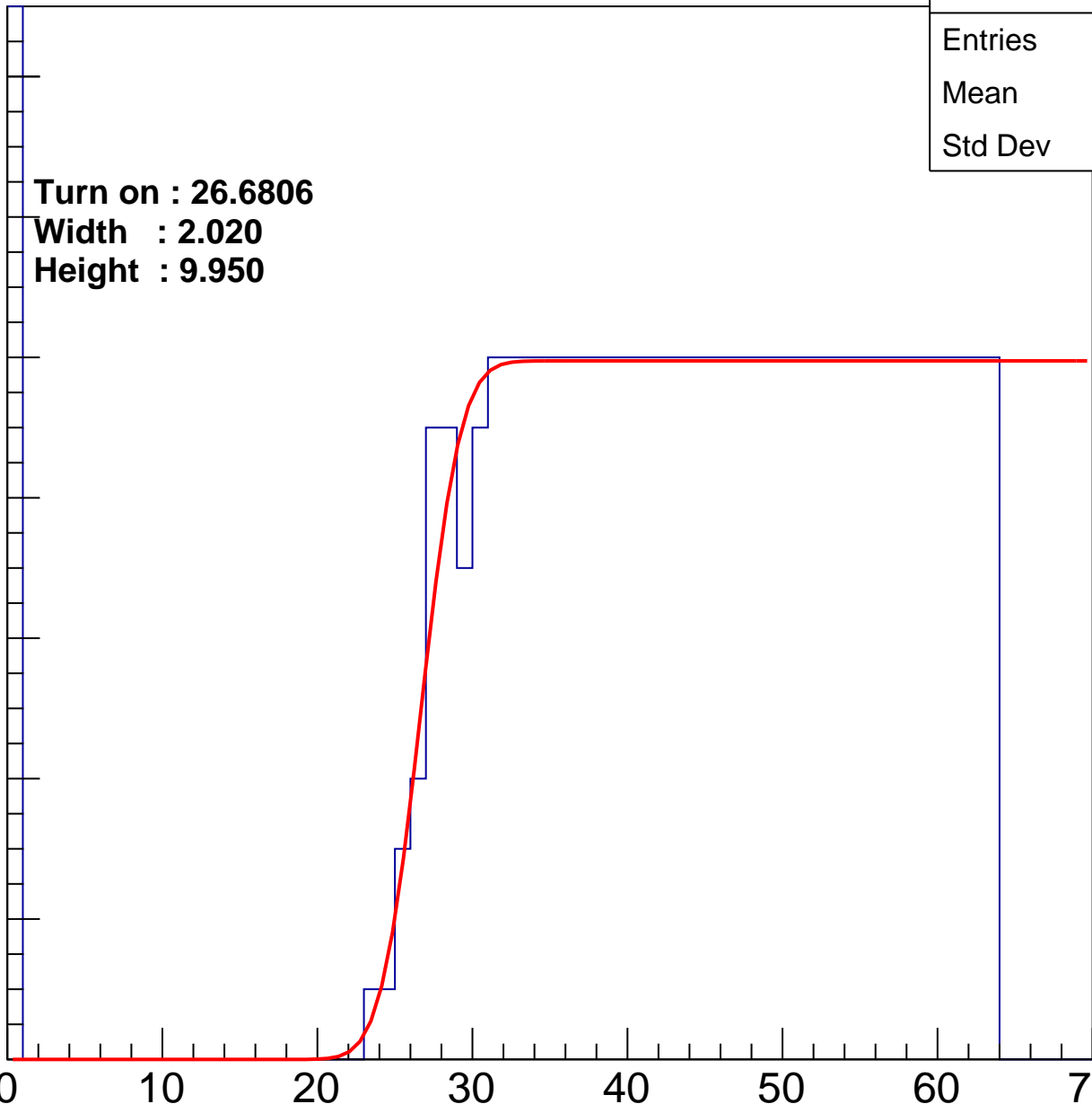
Entry

14  
12  
10  
8  
6  
4  
2  
0

Turn on : 26.6806  
Width : 2.020  
Height : 9.950

Entries	408
Mean	40.94
Std Dev	16.29

ampl



# B1L103S, U26-ch26

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	442
Mean	38.75
Std Dev	17.71

Turn on : 26.2061

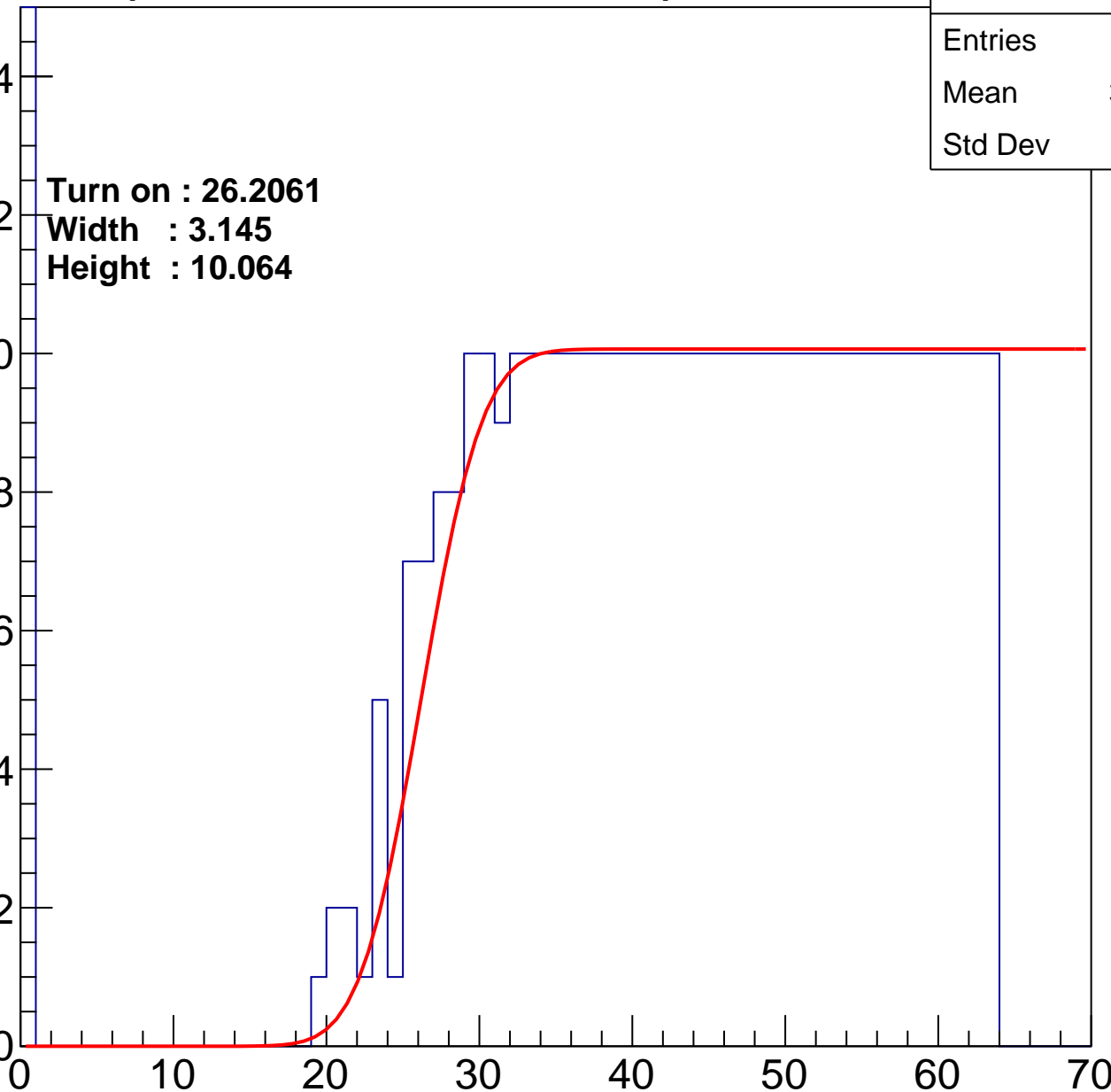
Width : 3.145

Height : 10.064

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch27

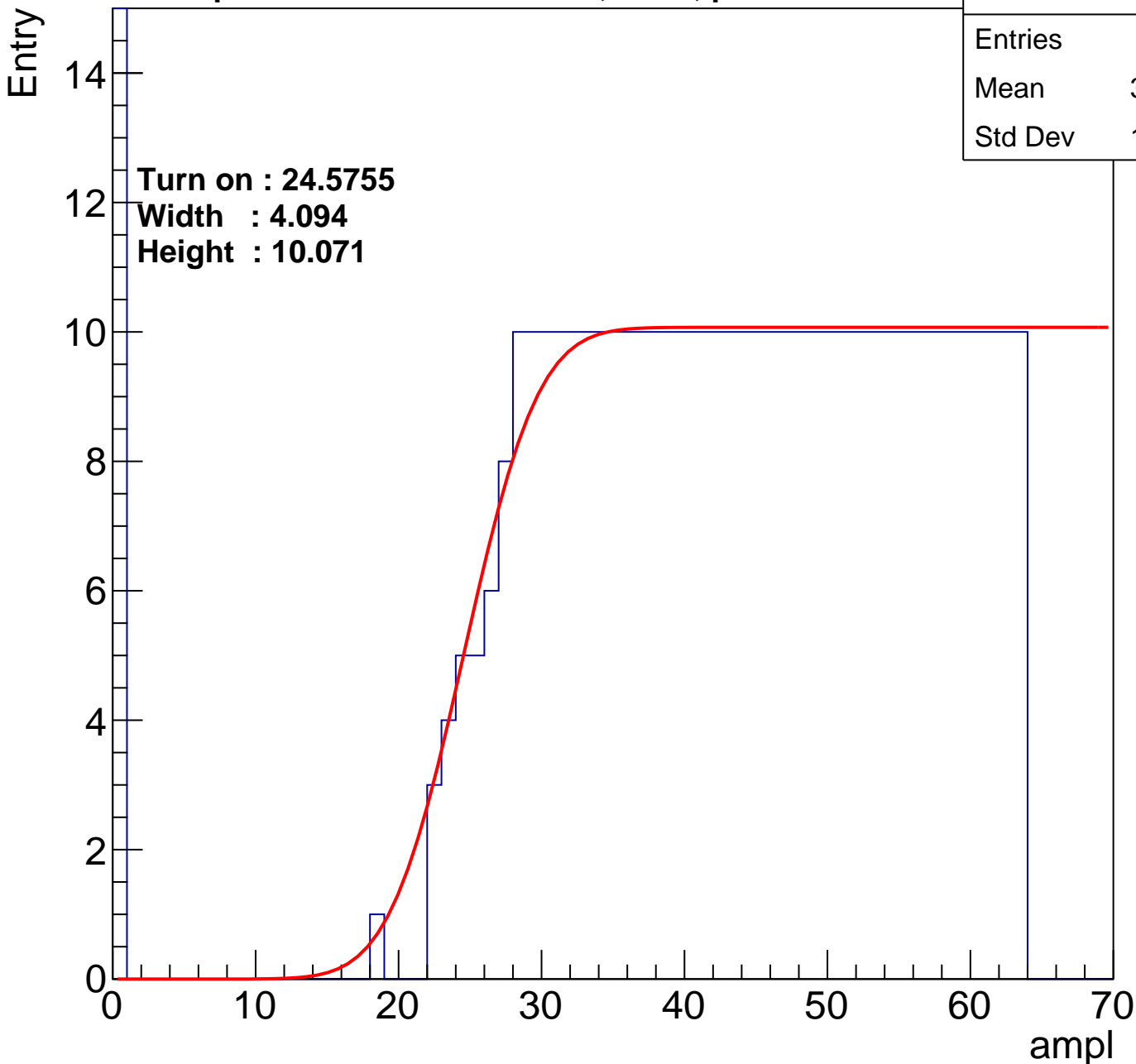
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	439
Mean	39.12
Std Dev	17.35

Turn on : 24.5755

Width : 4.094

Height : 10.071



# B1L103S, U26-ch28

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	434
Mean	38.68
Std Dev	18.25

**Turn on : 26.1605**

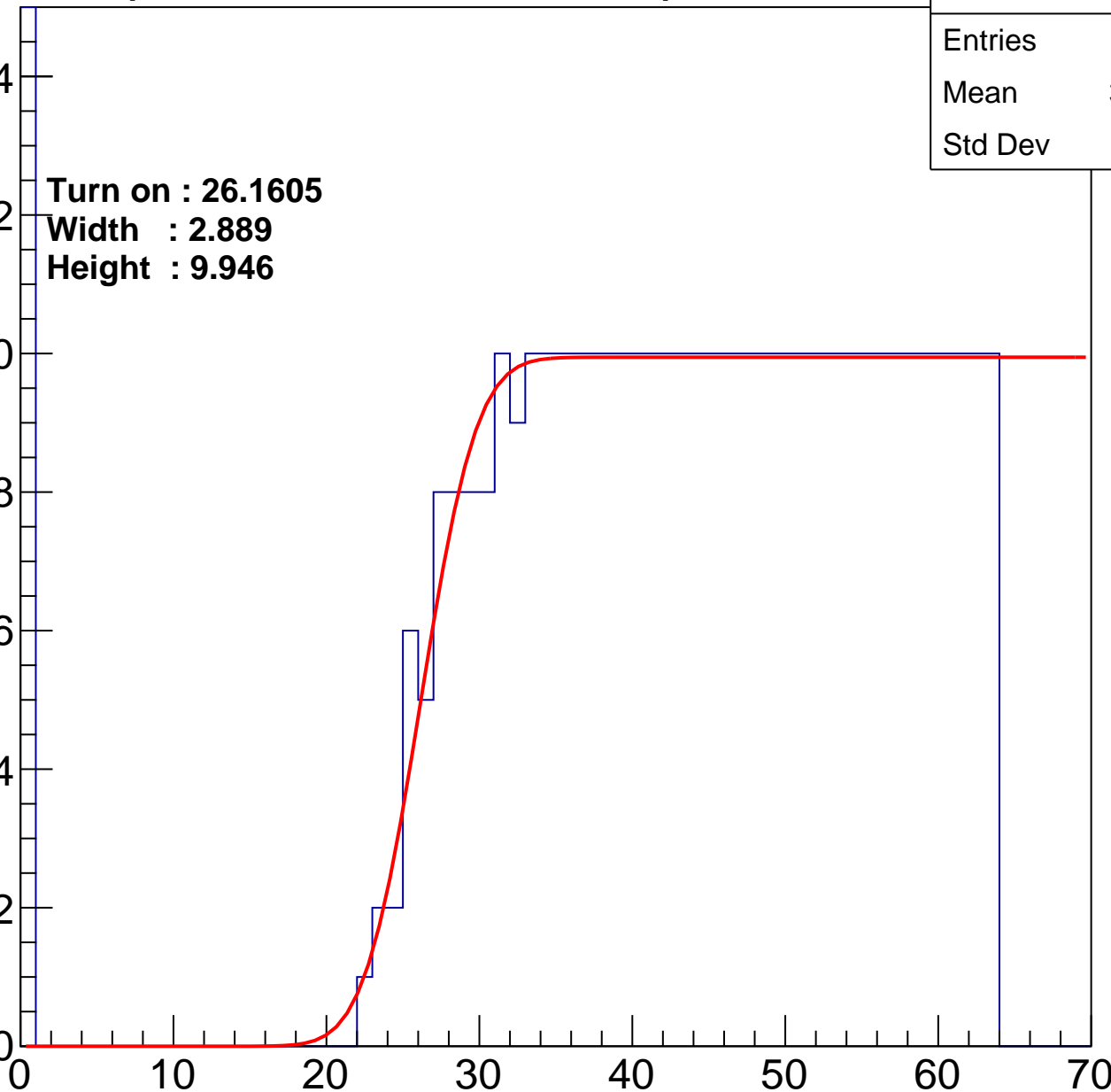
**Width : 2.889**

**Height : 9.946**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch29

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	443
Mean	39.55
Std Dev	16.4

Turn on : 23.9741

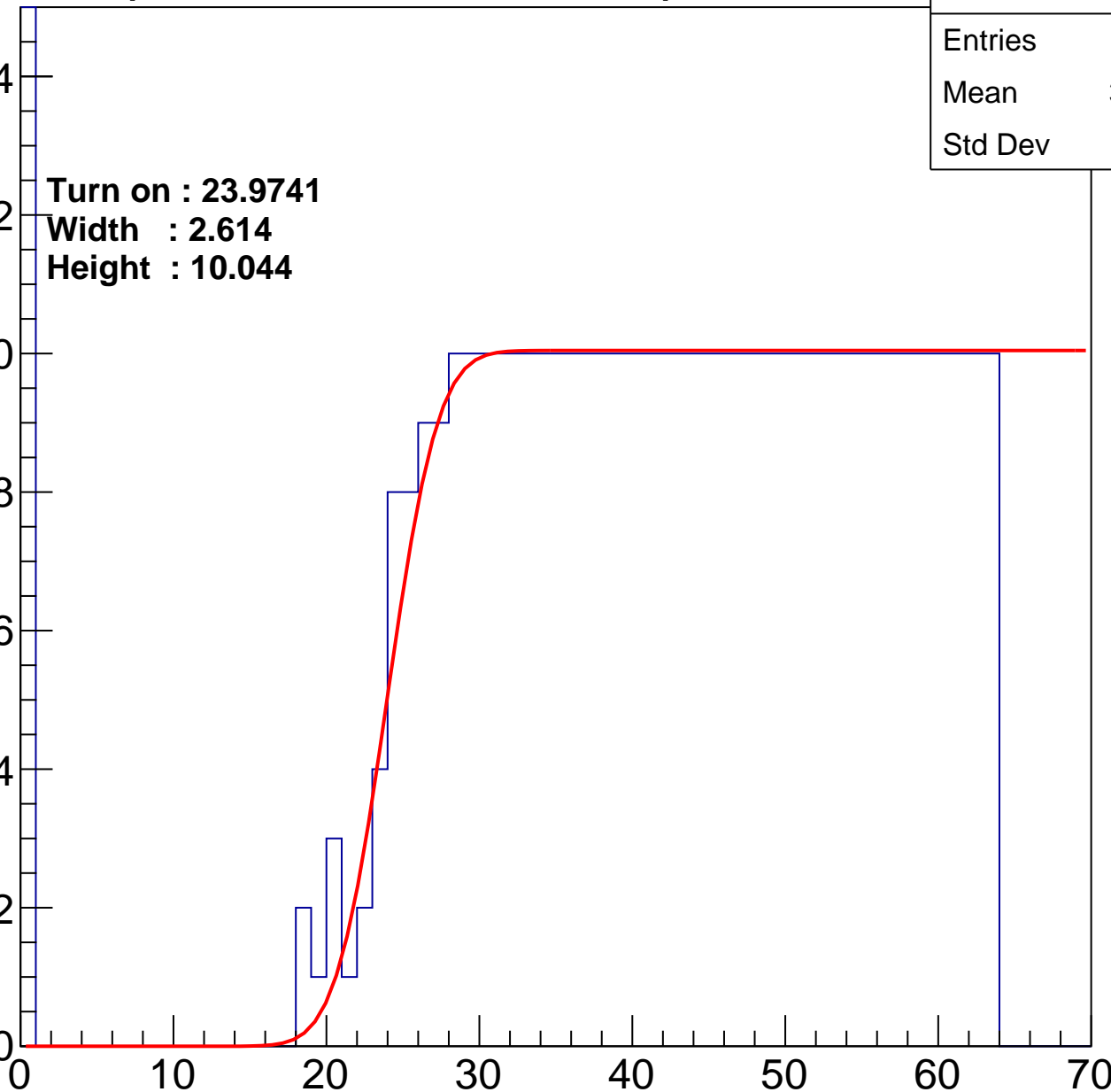
Width : 2.614

Height : 10.044

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch30

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	409
Mean	41.01
Std Dev	16.09

**Turn on : 26.6753**

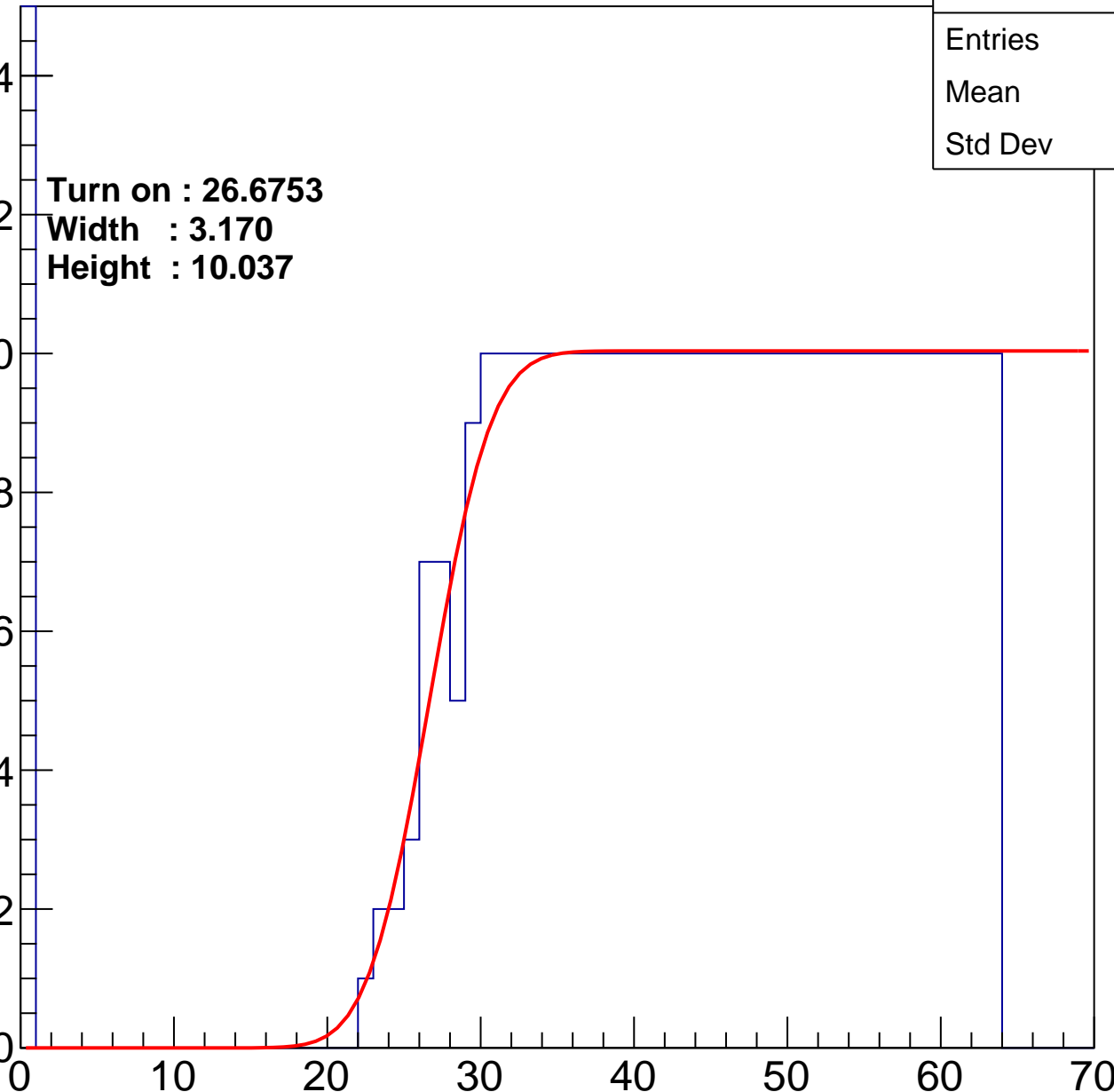
**Width : 3.170**

**Height : 10.037**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U26-ch31

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	412
Mean	40.39
Std Dev	16.93

Turn on : 26.7821

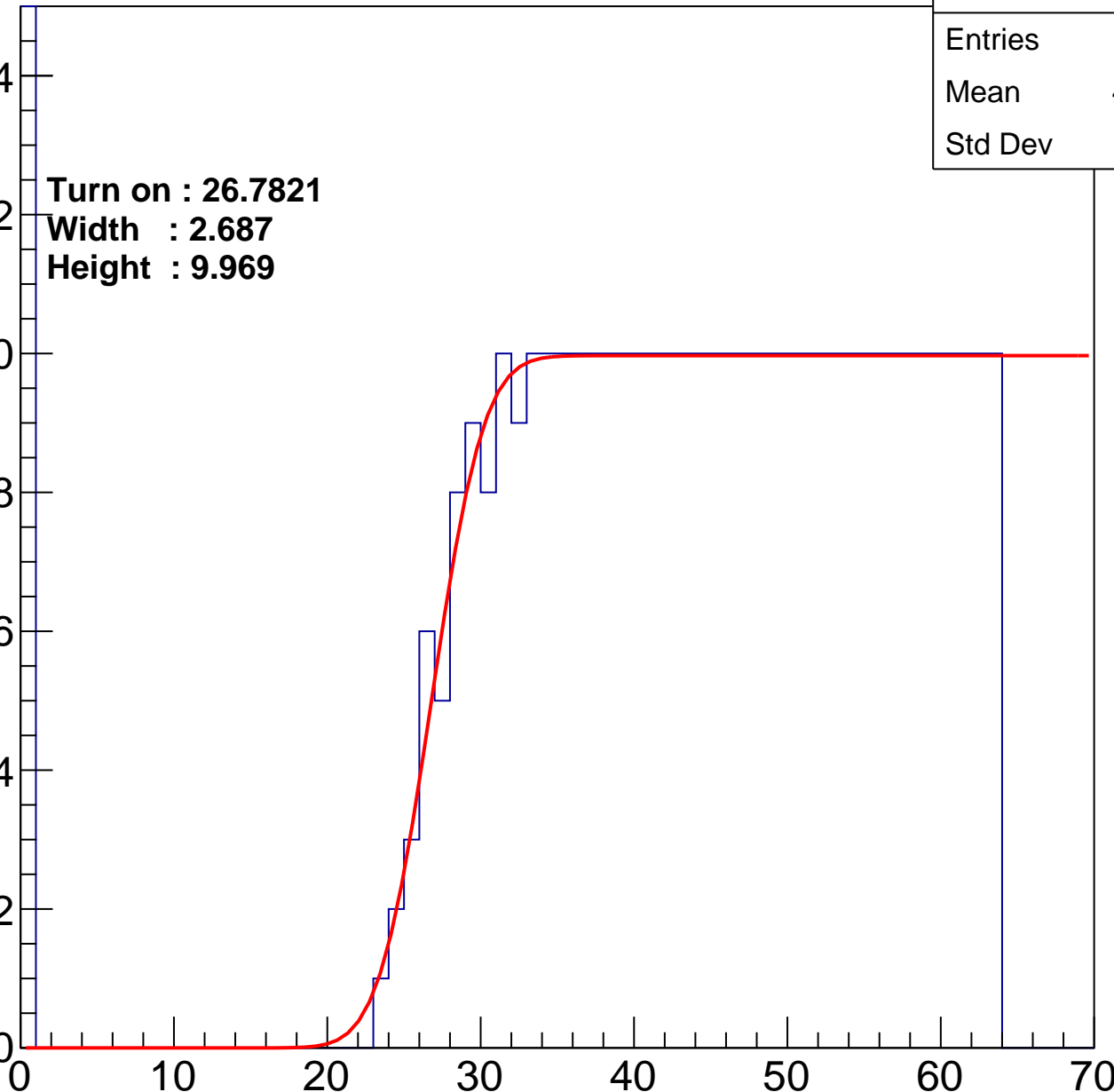
Width : 2.687

Height : 9.969

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch32

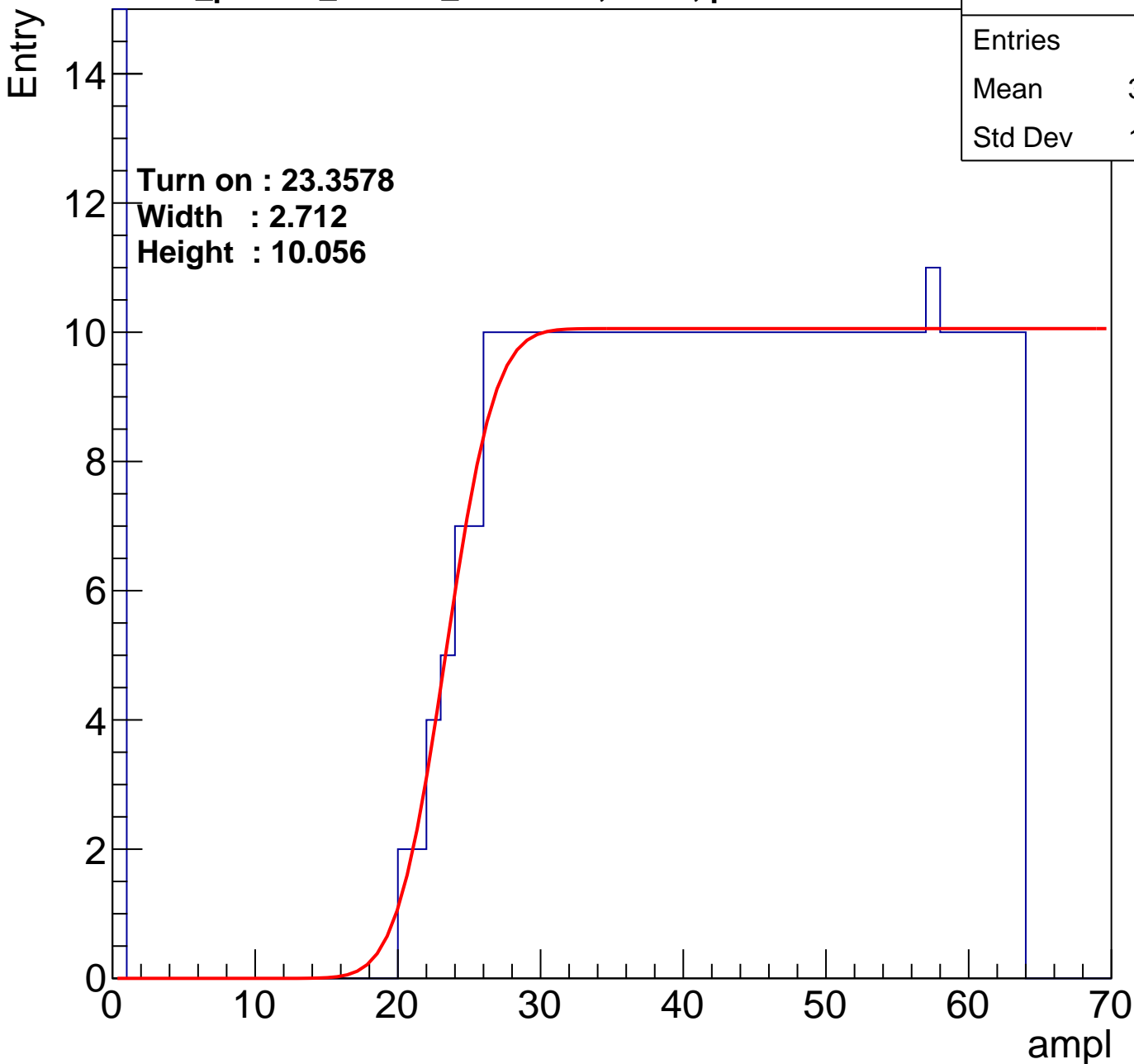
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	460
Mean	38.25
Std Dev	17.64

Turn on : 23.3578

Width : 2.712

Height : 10.056



# B1L103S, U26-ch33

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	412
Mean	40.12
Std Dev	17.34

Turn on : 27.1186

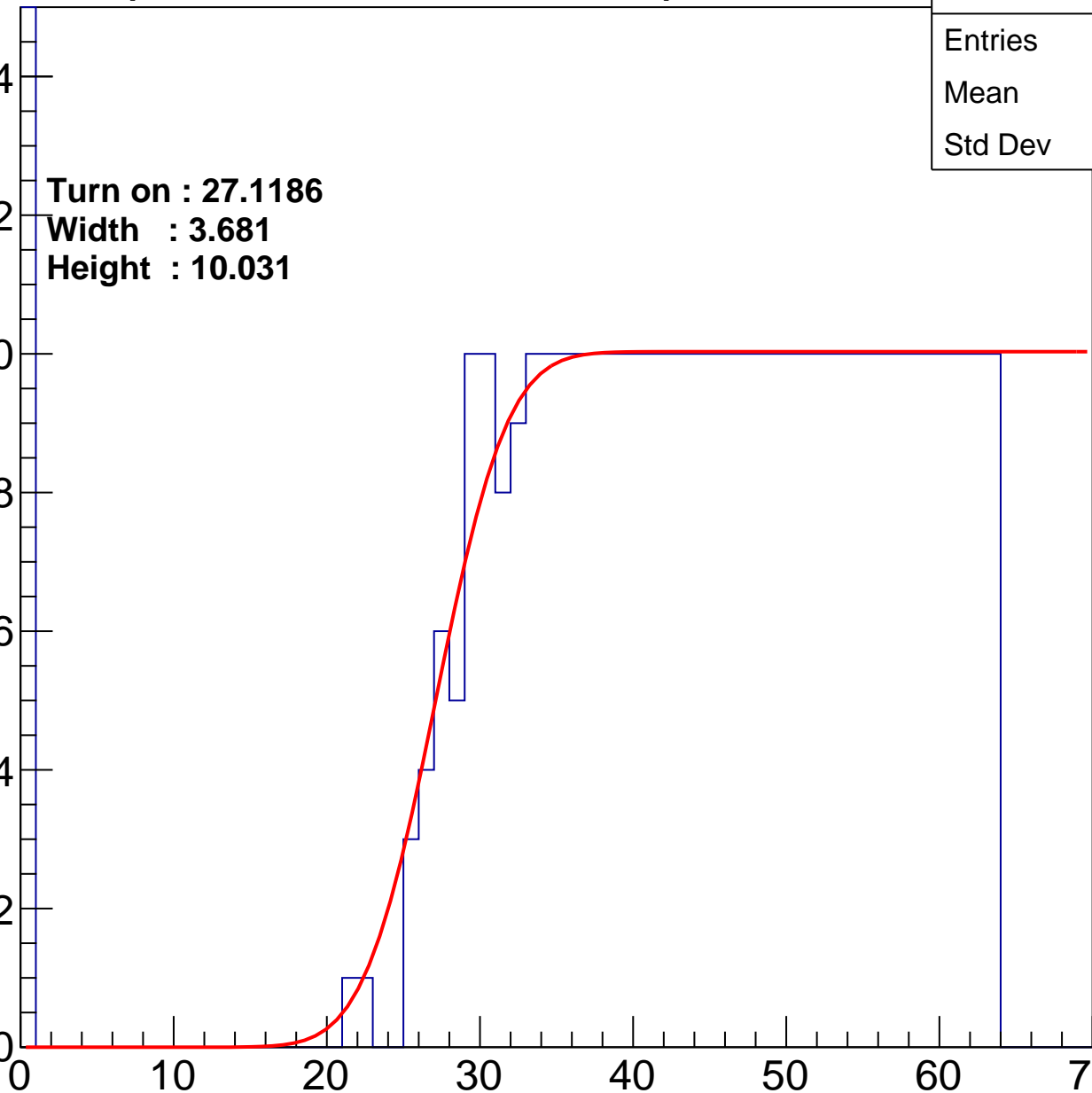
Width : 3.681

Height : 10.031

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch34

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	448
Mean	38.5
Std Dev	17.74

Turn on : 24.3542

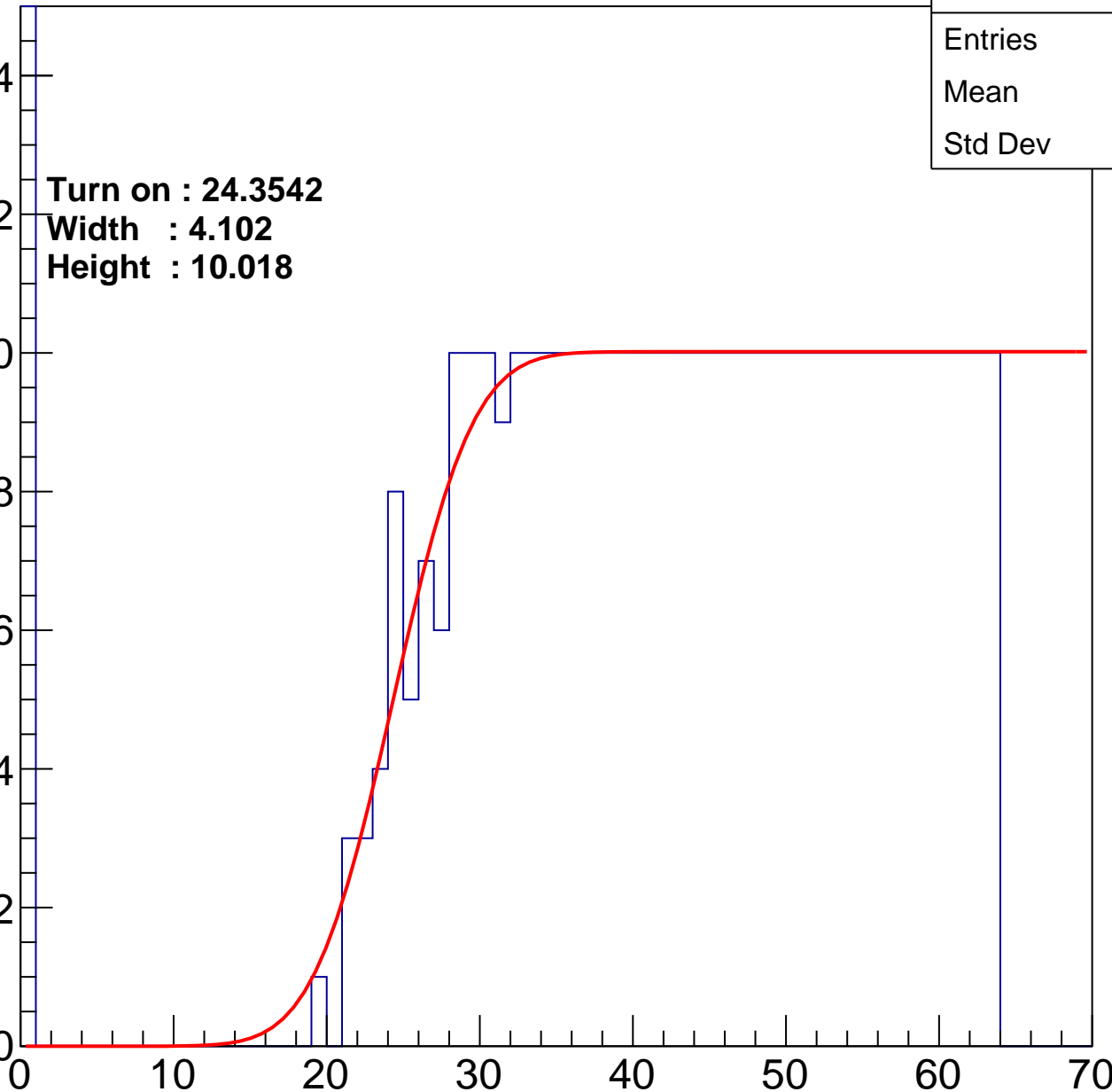
Width : 4.102

Height : 10.018

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch35

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	409
Mean	39.3
Std Dev	18.7

Turn on : 29.0839

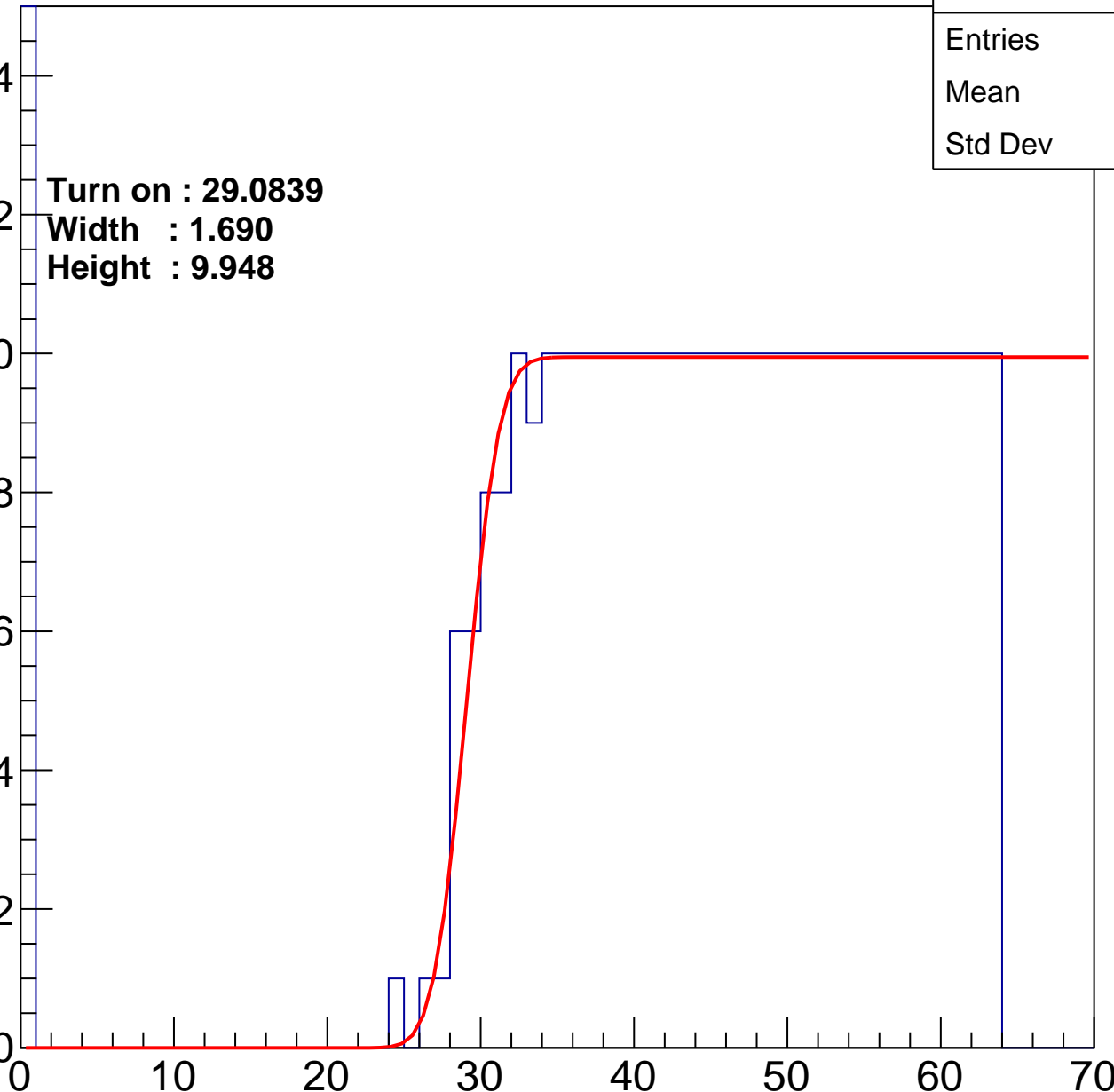
Width : 1.690

Height : 9.948

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch36

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	411
Mean	40.13
Std Dev	17.37

**Turn on : 26.9428**

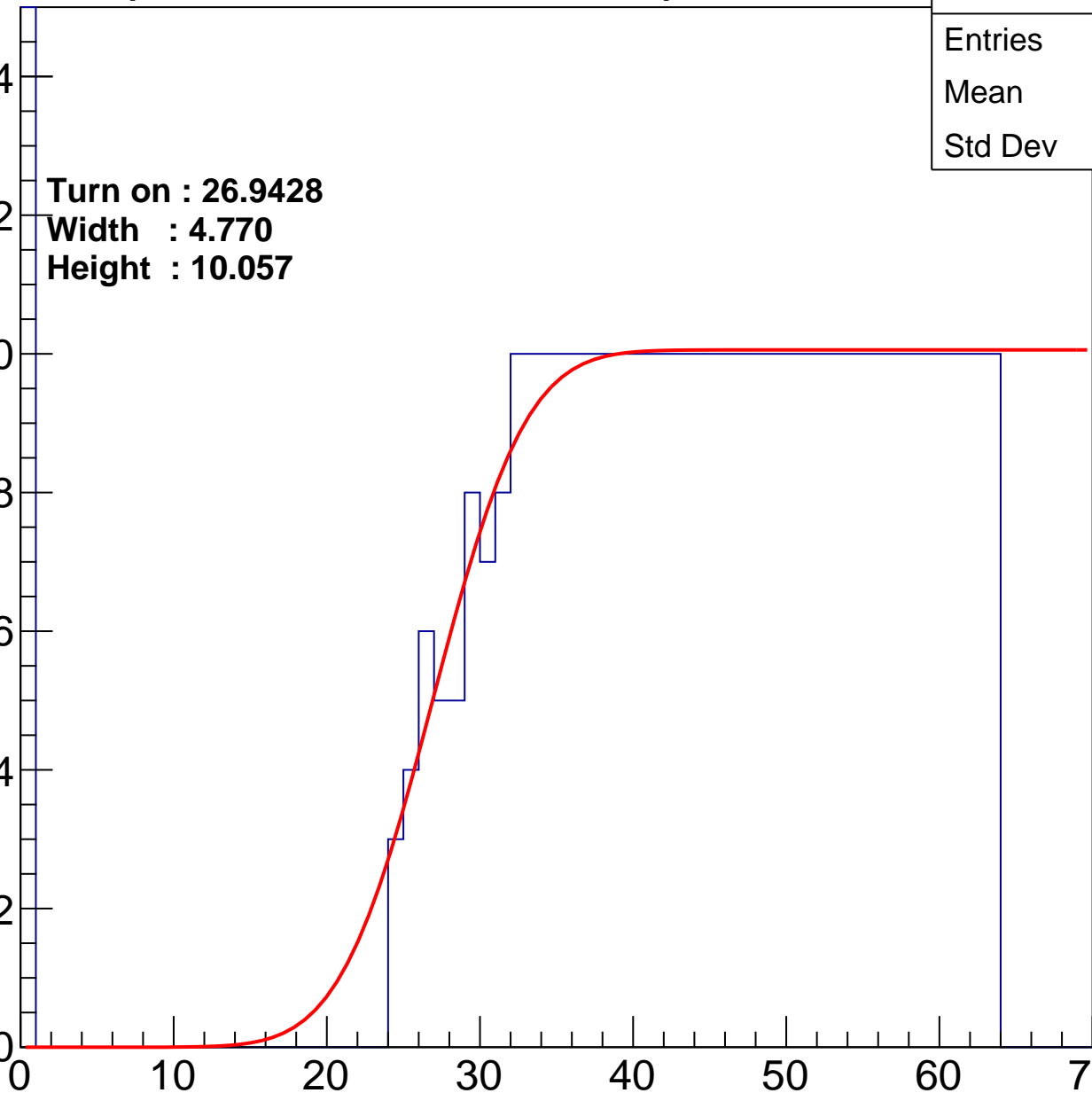
**Width : 4.770**

**Height : 10.057**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch37

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	425
Mean	39.41
Std Dev	17.7

**Turn on : 26.7587**

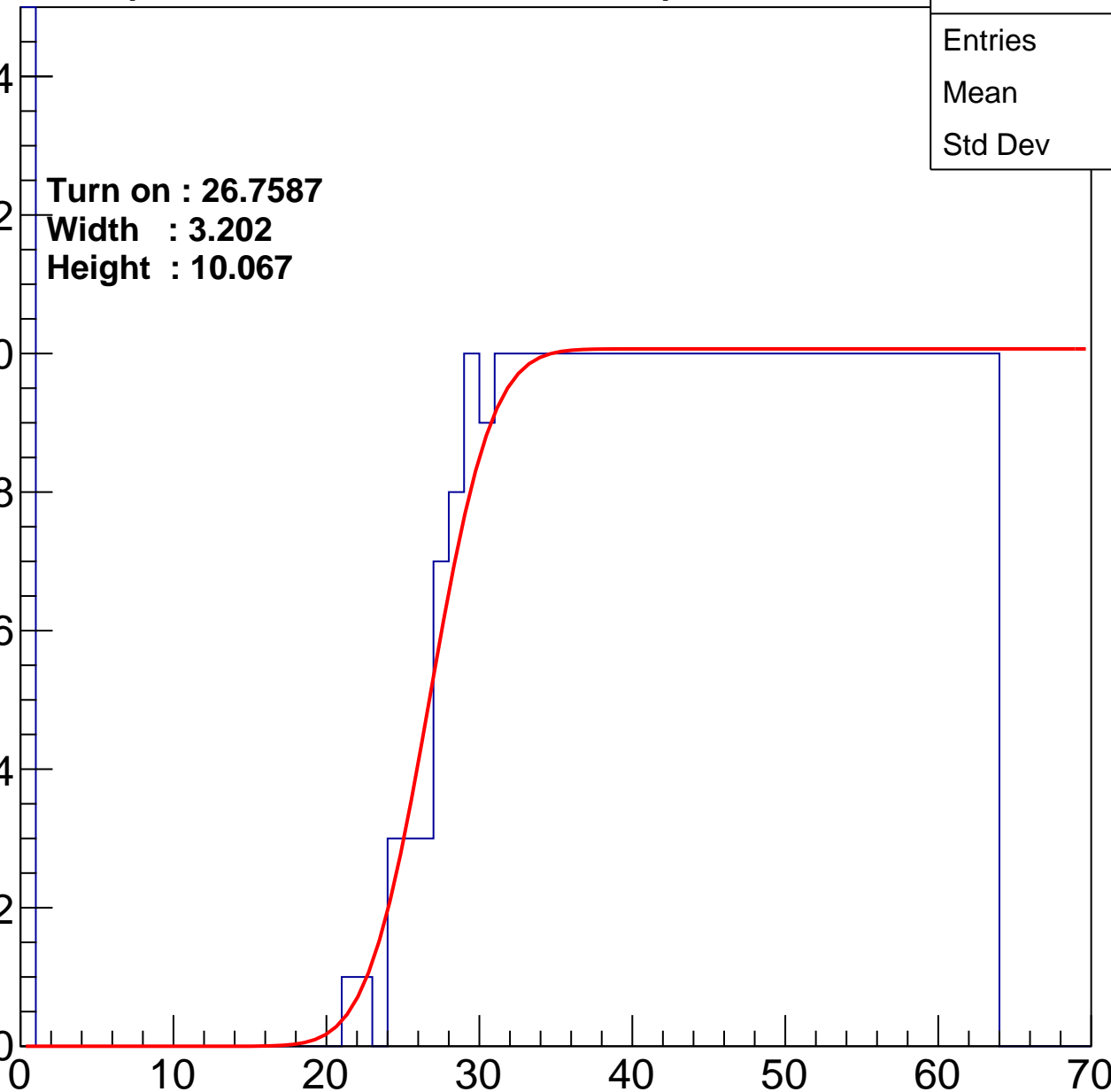
**Width : 3.202**

**Height : 10.067**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch38

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	403
Mean	41.59
Std Dev	15.44

Turn on : 26.3288

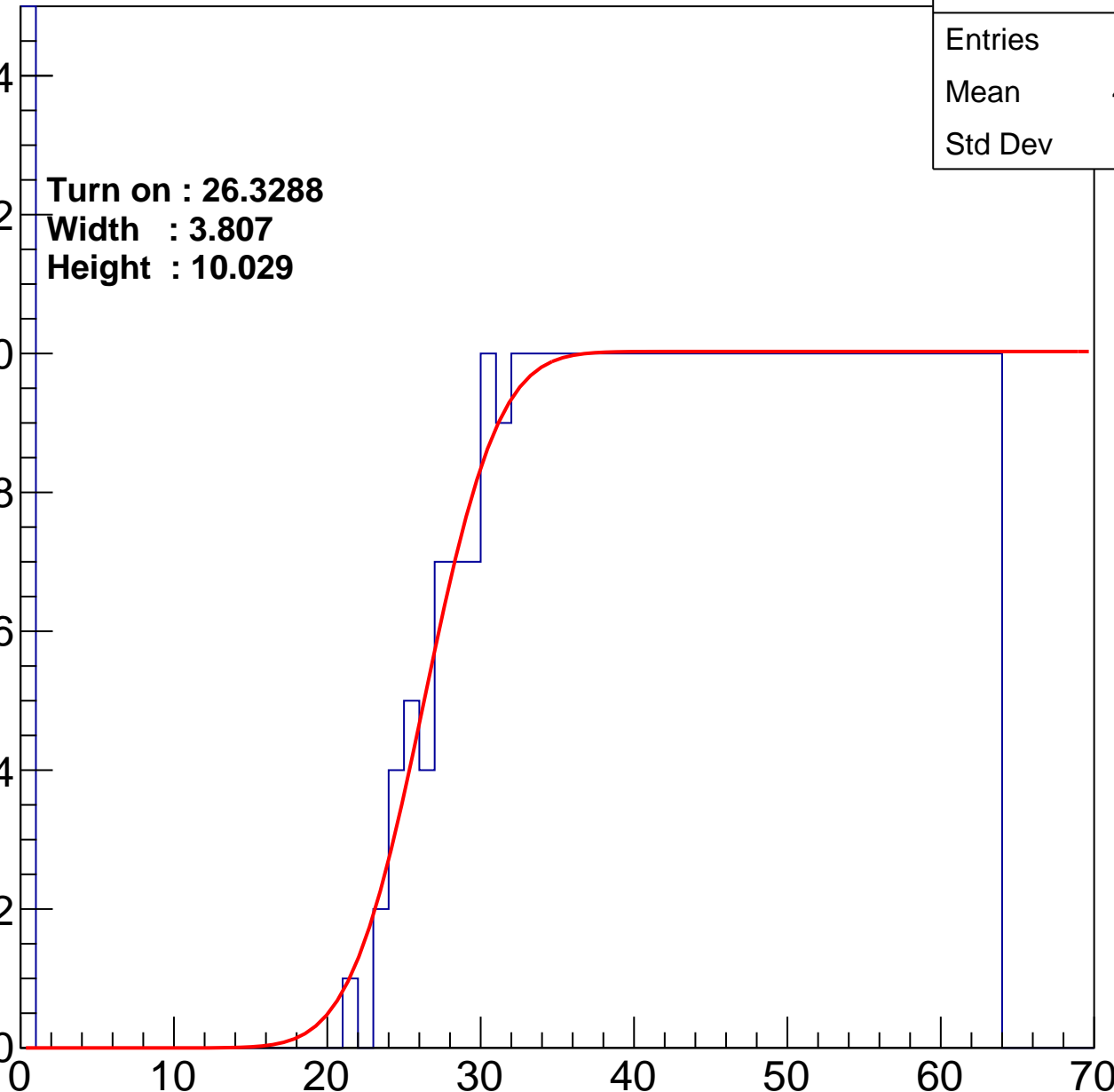
Width : 3.807

Height : 10.029

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U26-ch39

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	427
Mean	39.42
Std Dev	17.54

Turn on : 26.6310

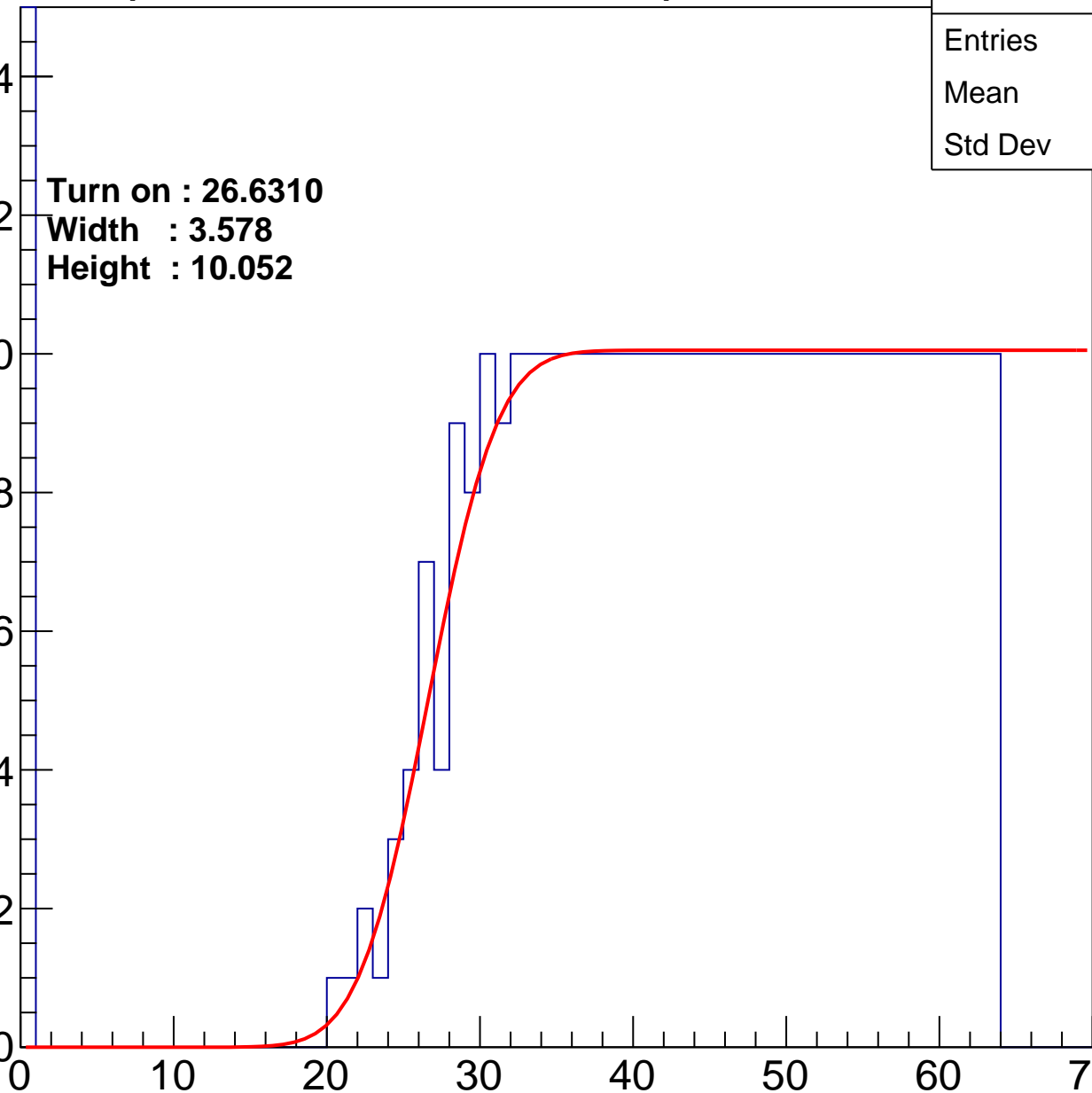
Width : 3.578

Height : 10.052

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch40

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	461
Mean	37.64
Std Dev	18.6

Turn on : 24.1905

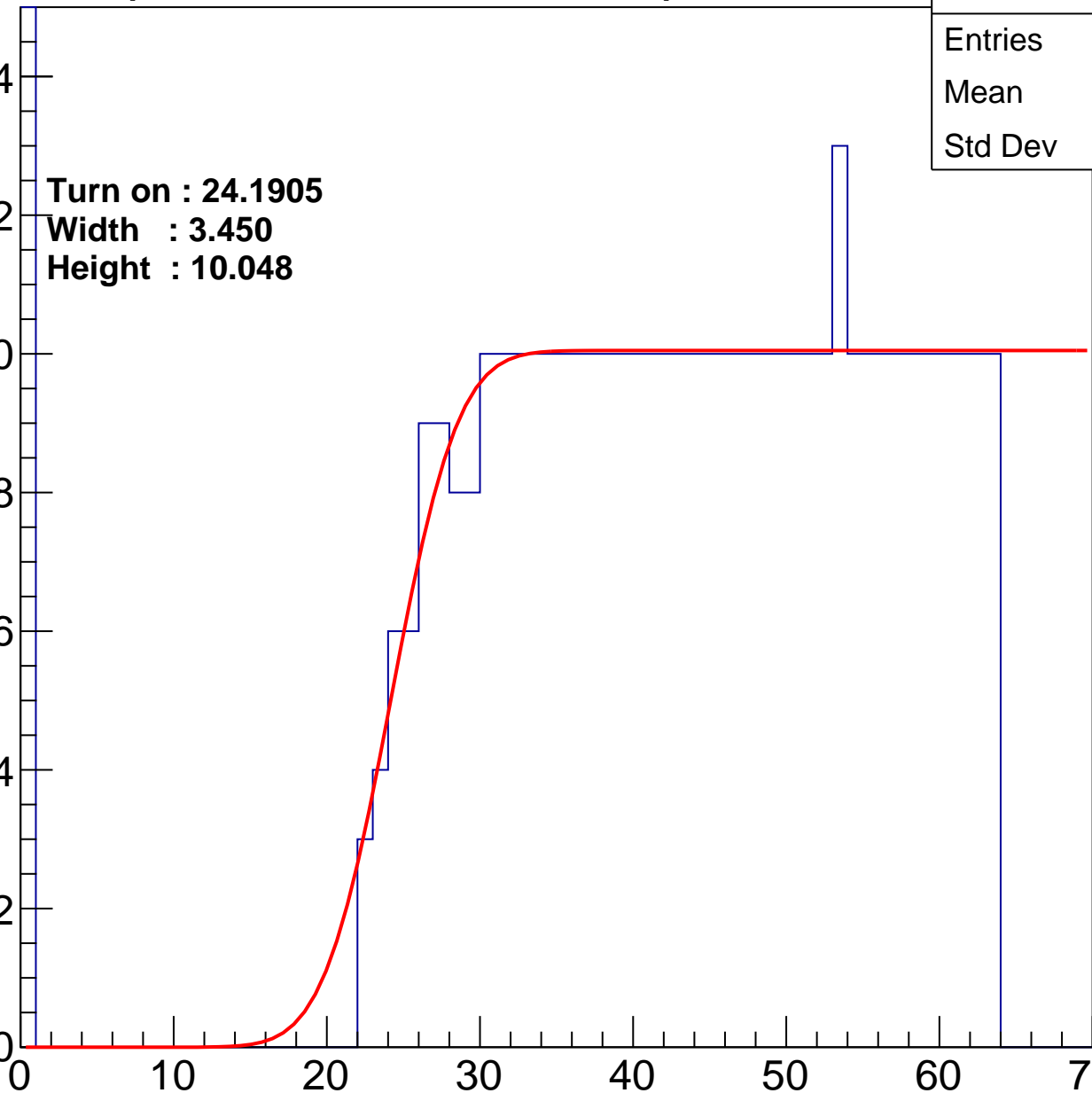
Width : 3.450

Height : 10.048

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch41

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	409
Mean	41.06
Std Dev	15.99

**Turn on : 26.2544**

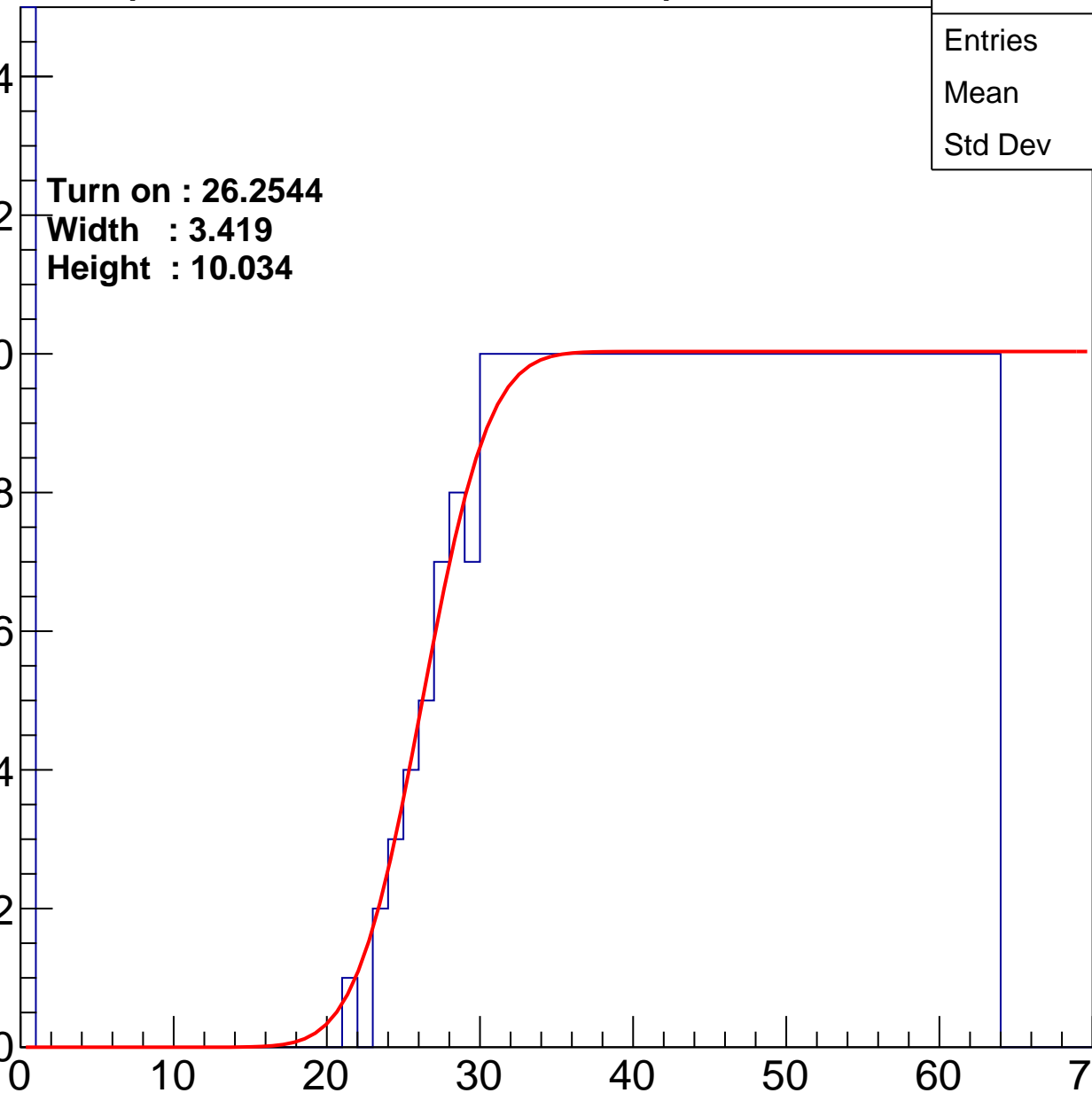
**Width : 3.419**

**Height : 10.034**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch42

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	450
Mean	37.68
Std Dev	18.84

Turn on : 25.6172

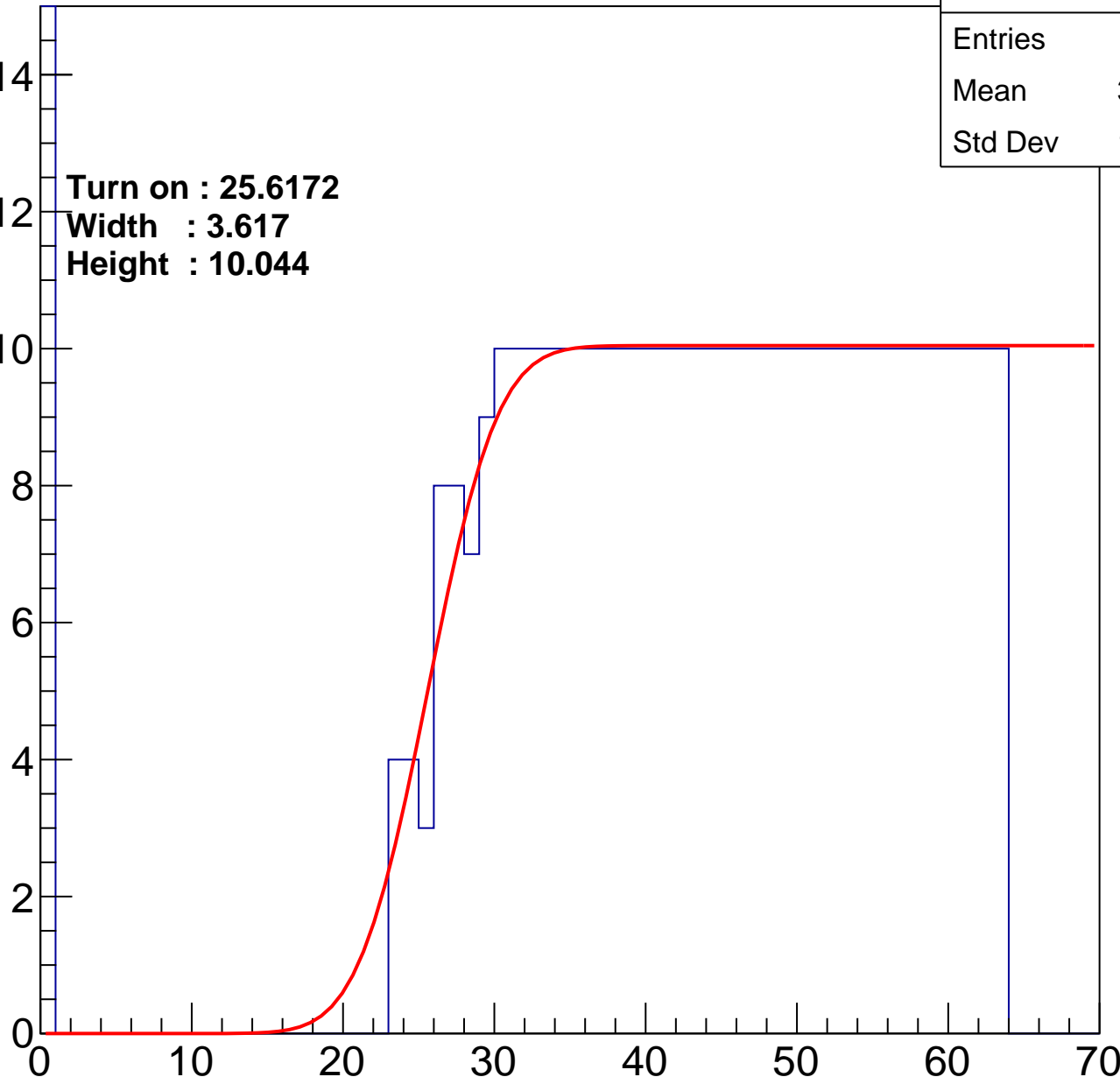
Width : 3.617

Height : 10.044

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch43

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	425
Mean	39.37
Std Dev	17.73

Turn on : 26.3905

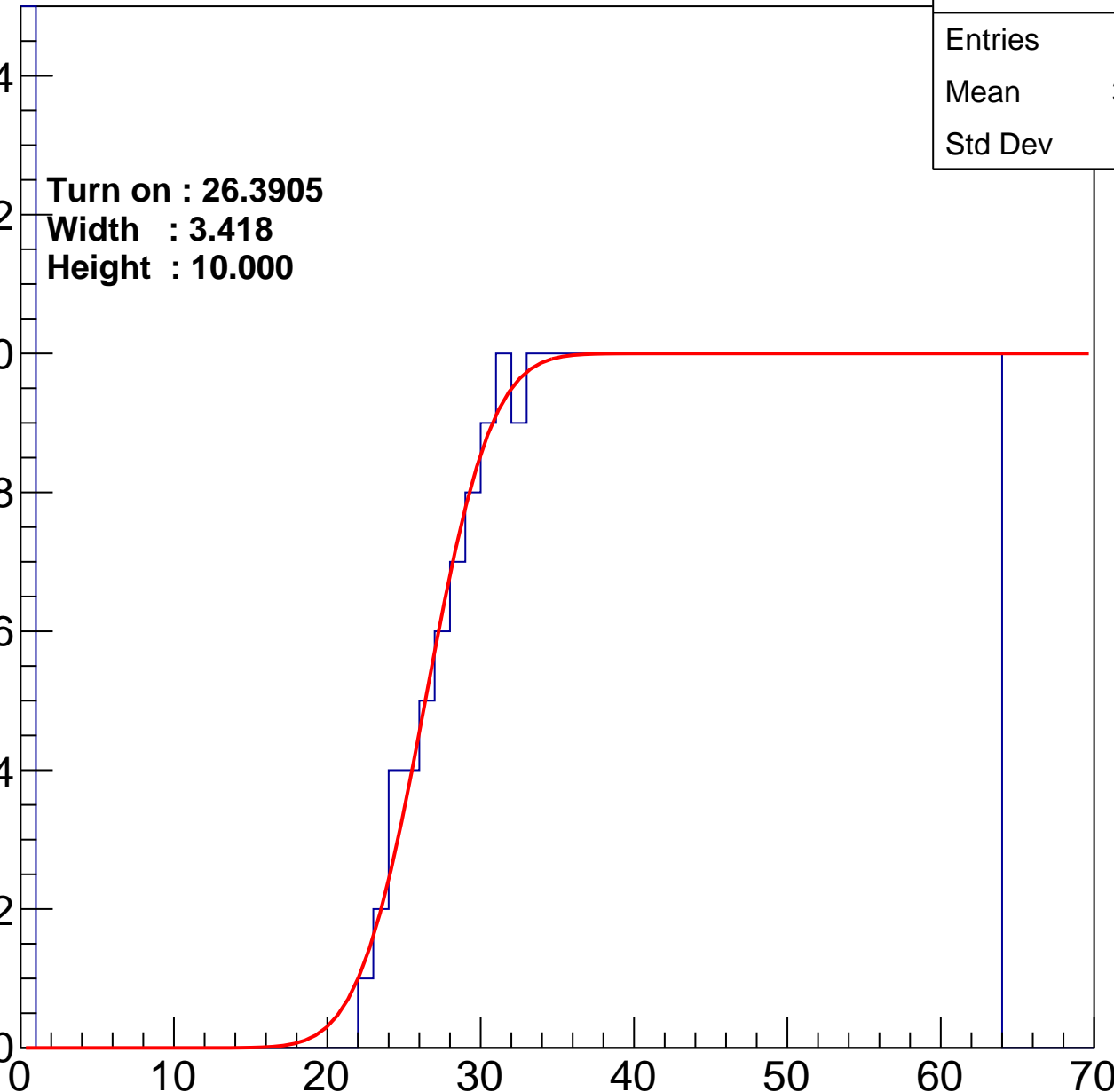
Width : 3.418

Height : 10.000

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch44

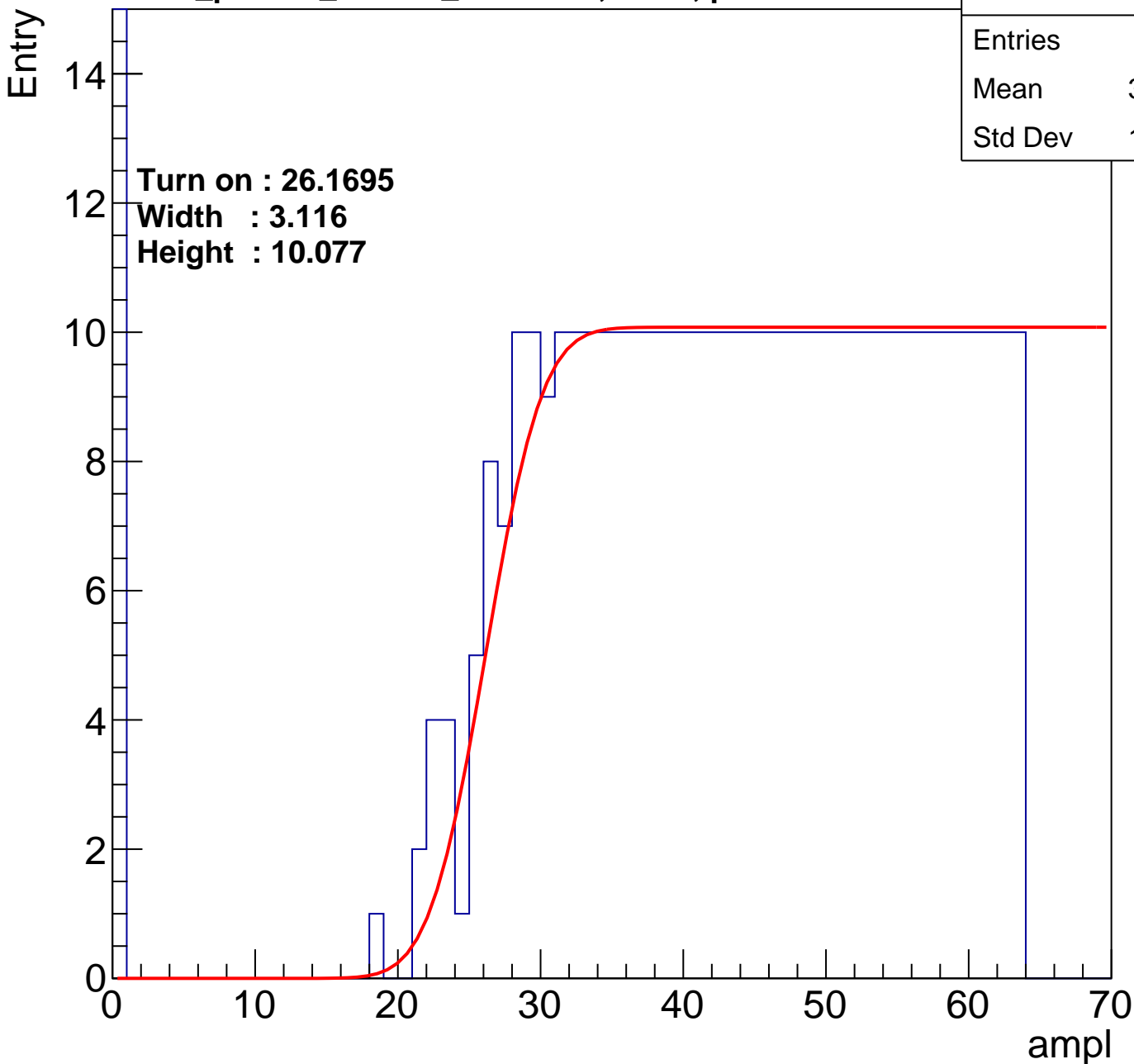
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	440
Mean	38.95
Std Dev	17.54

Turn on : 26.1695

Width : 3.116

Height : 10.077



# B1L103S, U26-ch45

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	405
Mean	40.51
Std Dev	17.18

Turn on : 27.9586

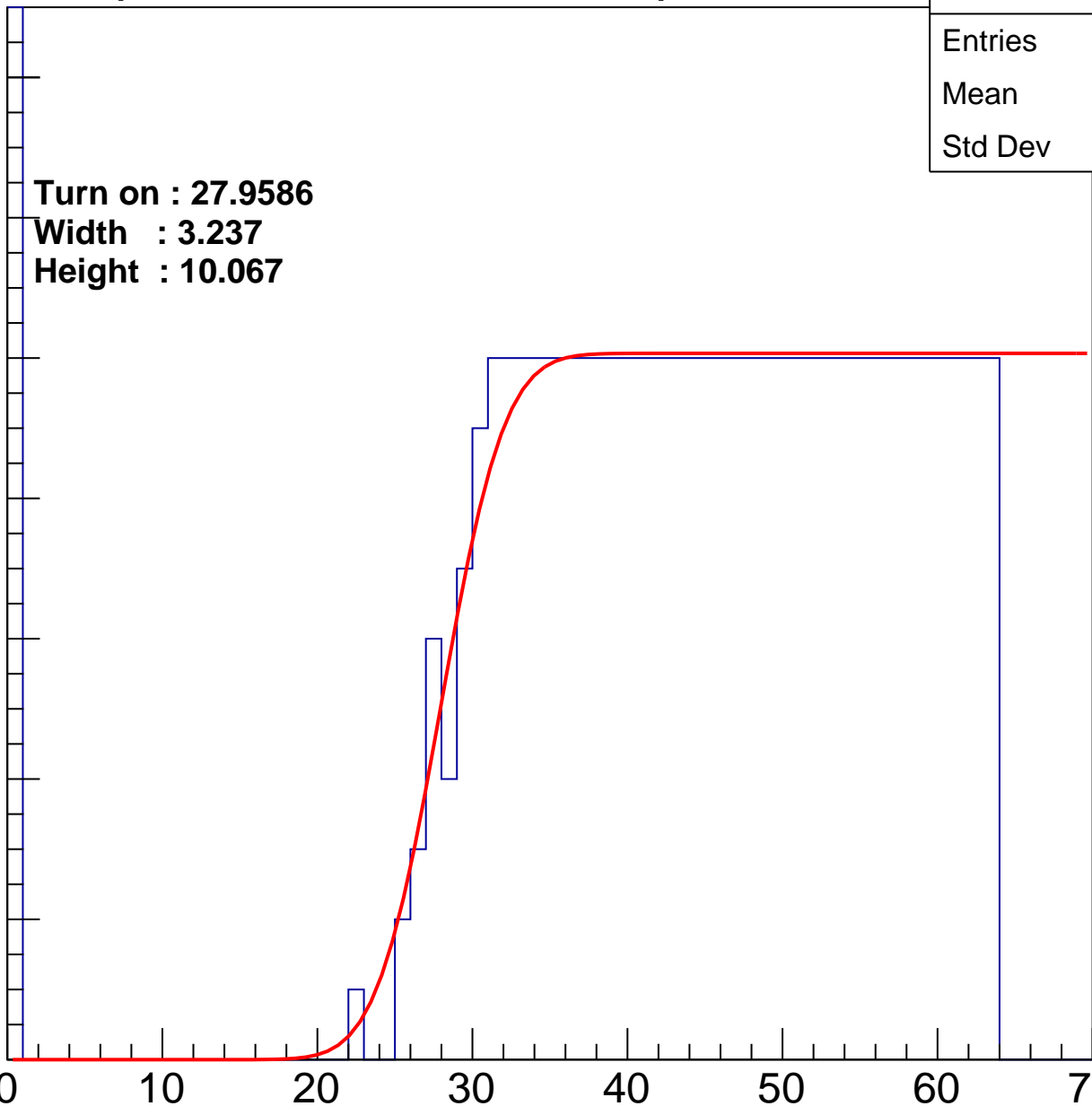
Width : 3.237

Height : 10.067

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch46

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	422
Mean	40.1
Std Dev	16.91

Turn on : 26.8037

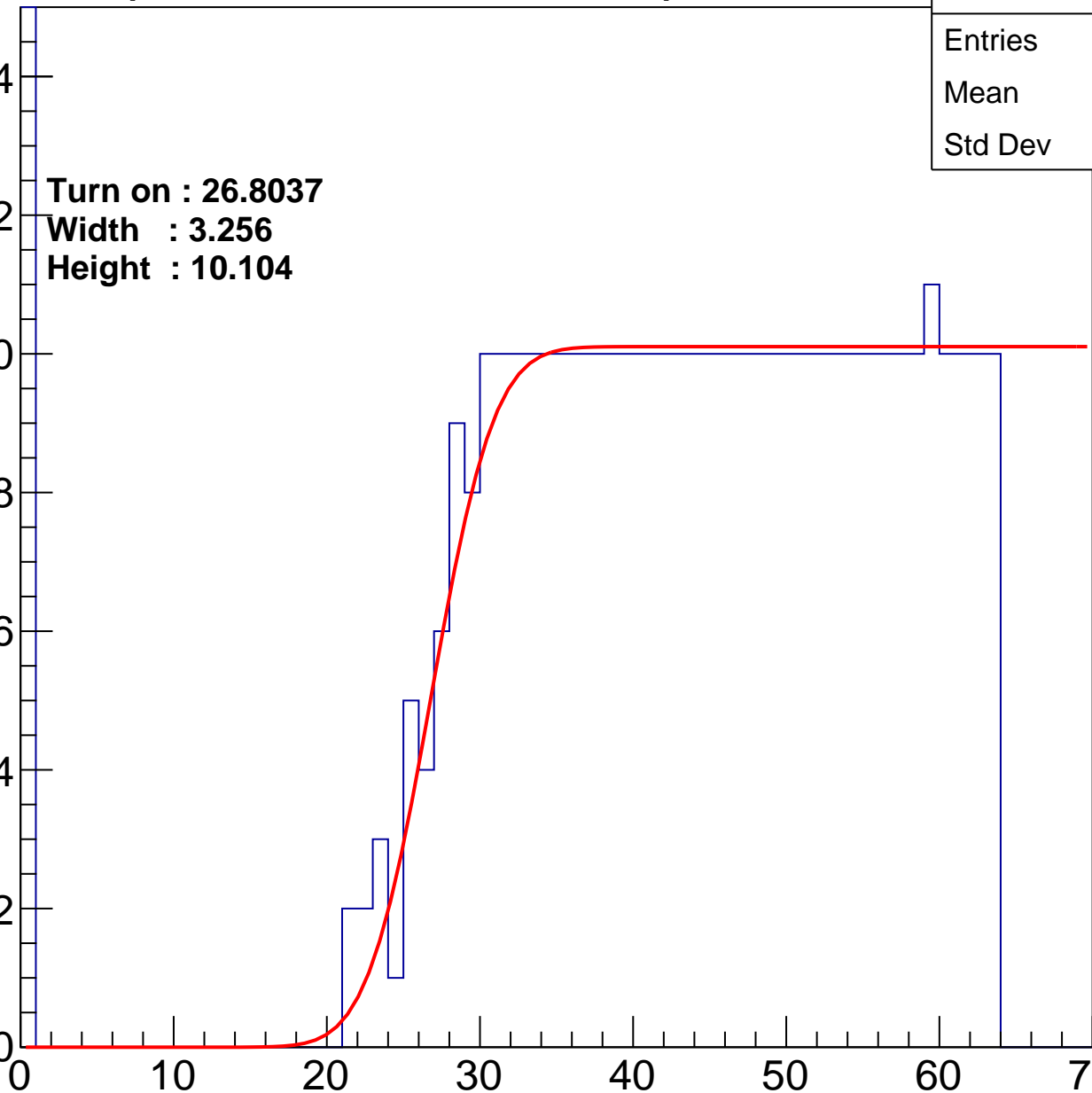
Width : 3.256

Height : 10.104

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U26-ch47

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	442
Mean	38.75
Std Dev	17.74

Turn on : 24.9029

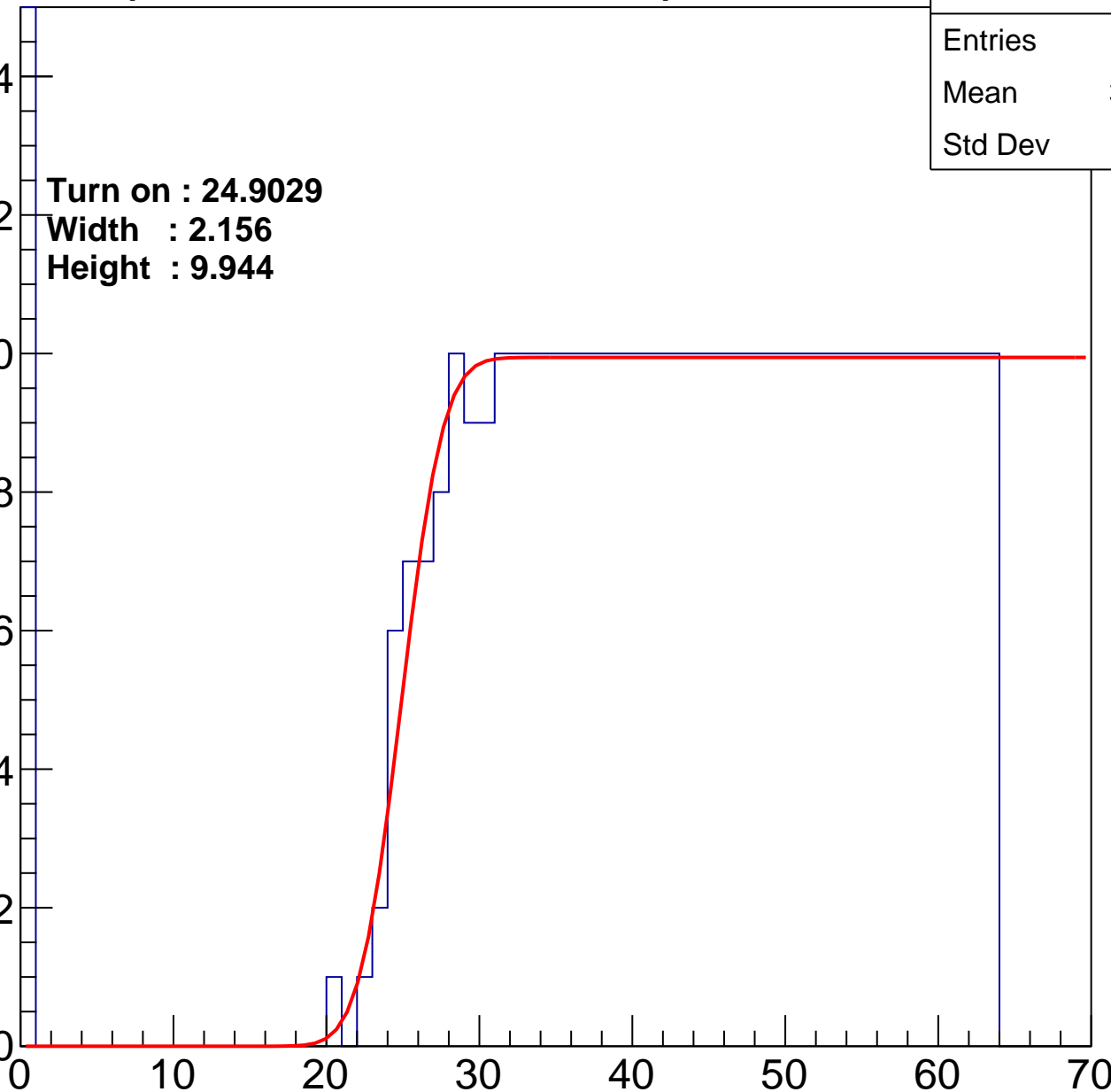
Width : 2.156

Height : 9.944

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch48

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	437
Mean	39.32
Std Dev	17.12

Turn on : 25.5677

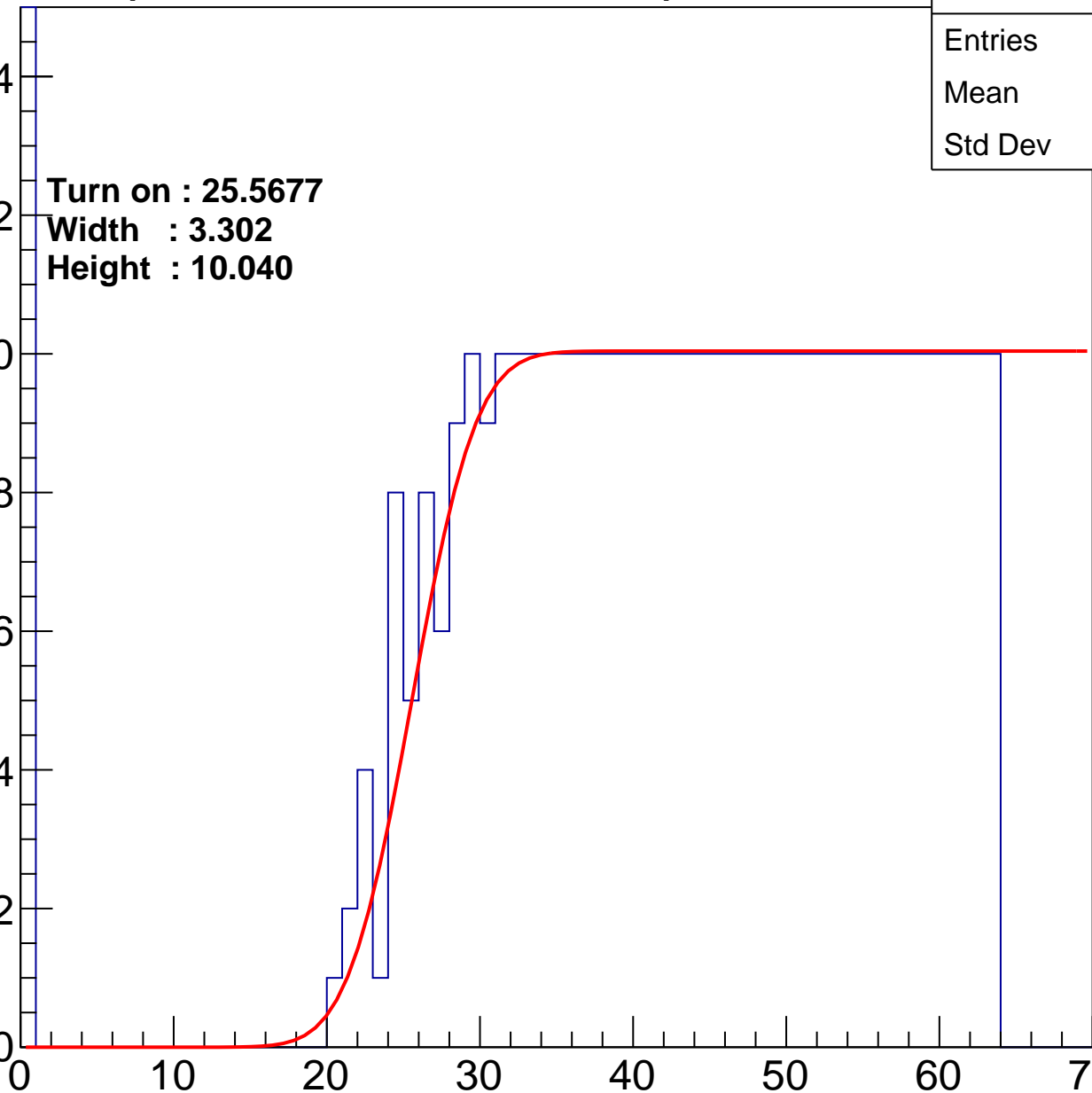
Width : 3.302

Height : 10.040

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch49

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	436
Mean	39.54
Std Dev	17.12

Turn on : 25.3357

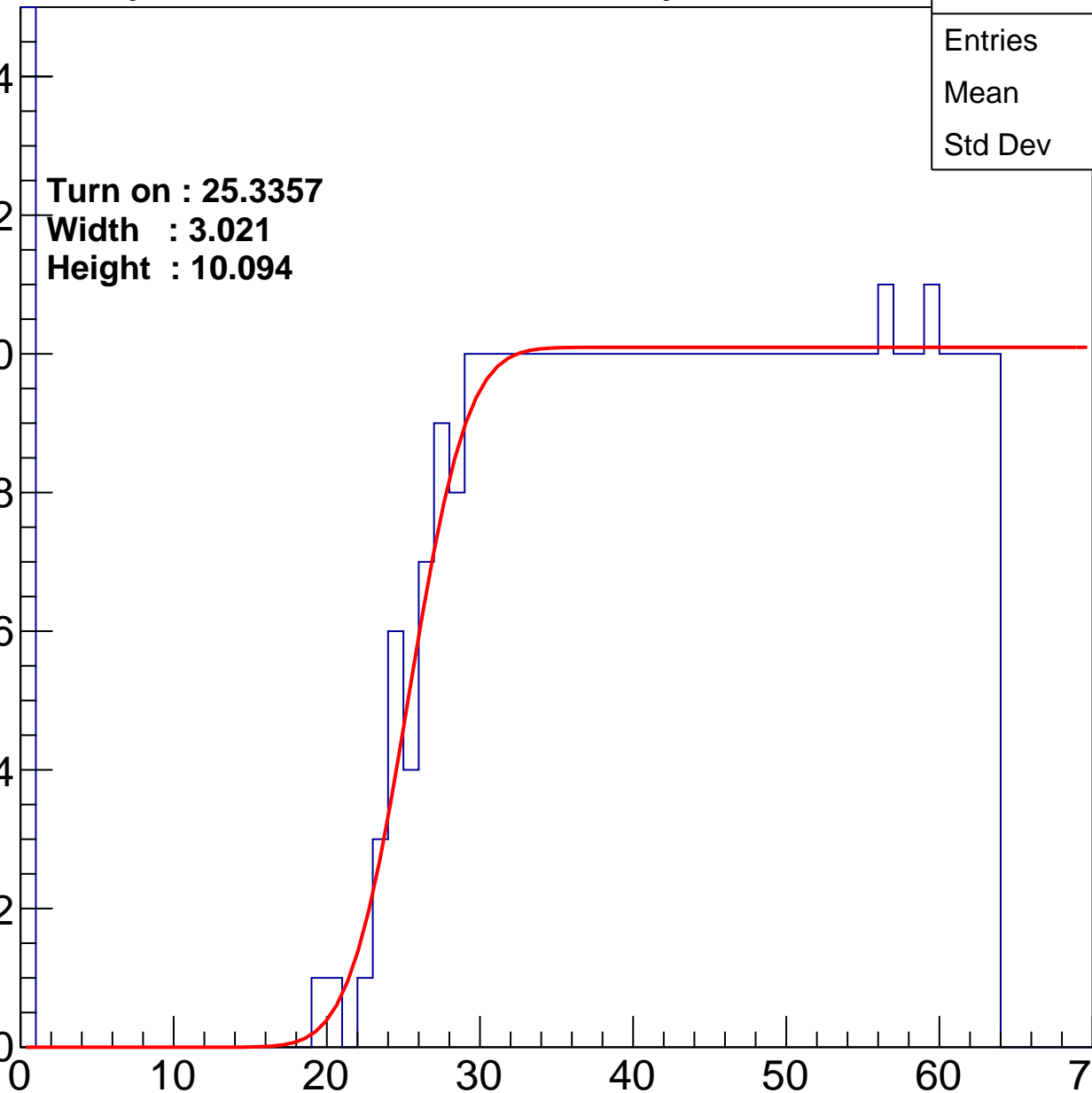
Width : 3.021

Height : 10.094

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch50

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	427
Mean	40.2
Std Dev	16.3

Turn on : 25.3404

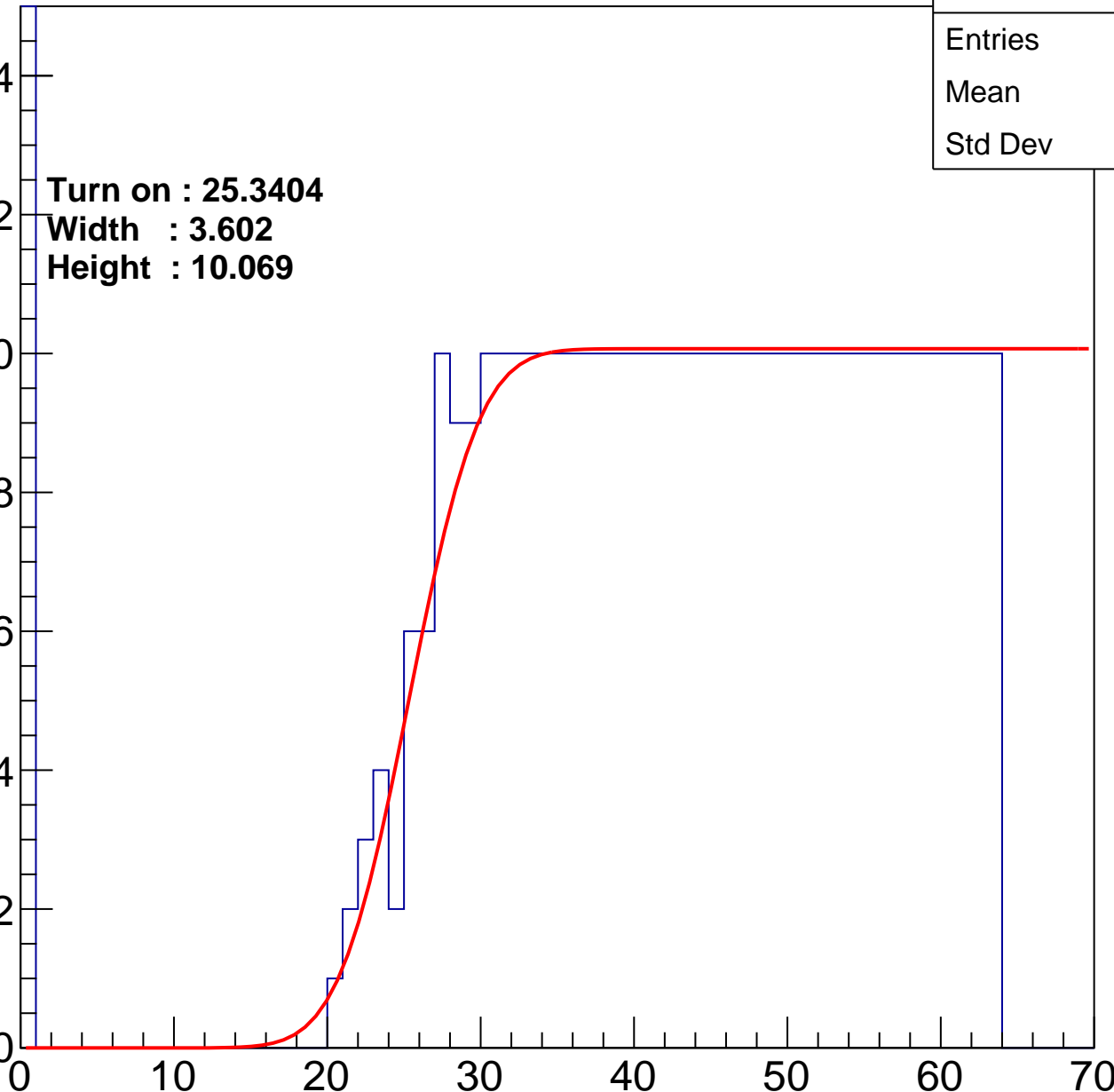
Width : 3.602

Height : 10.069

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch51

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	444
Mean	38.01
Std Dev	18.69

Turn on : 26.3007

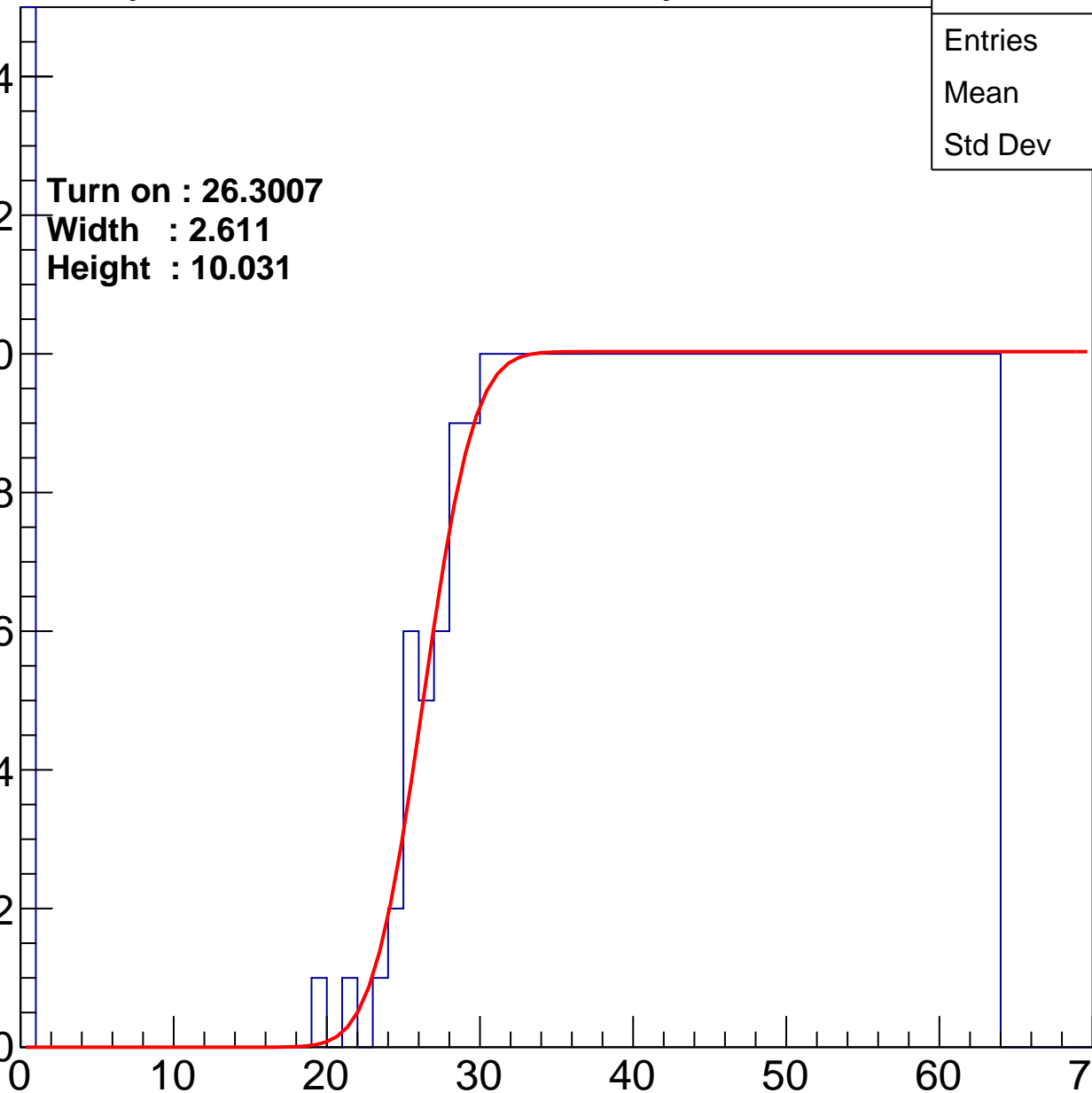
Width : 2.611

Height : 10.031

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch52

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	415
Mean	39.71
Std Dev	17.8

Turn on : 27.6559

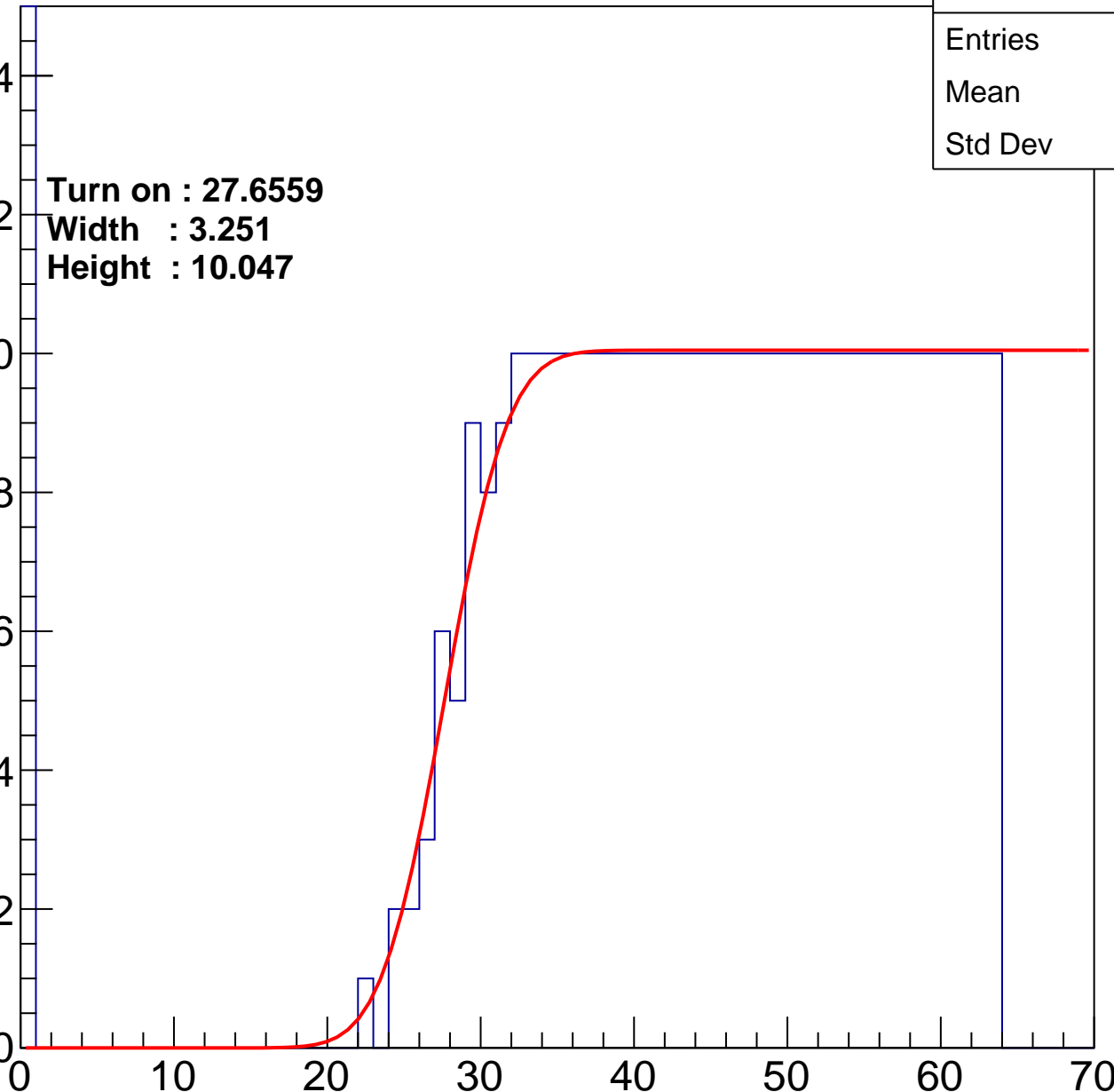
Width : 3.251

Height : 10.047

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch53

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	398
Mean	41.27
Std Dev	16.36

Turn on : 28.3967

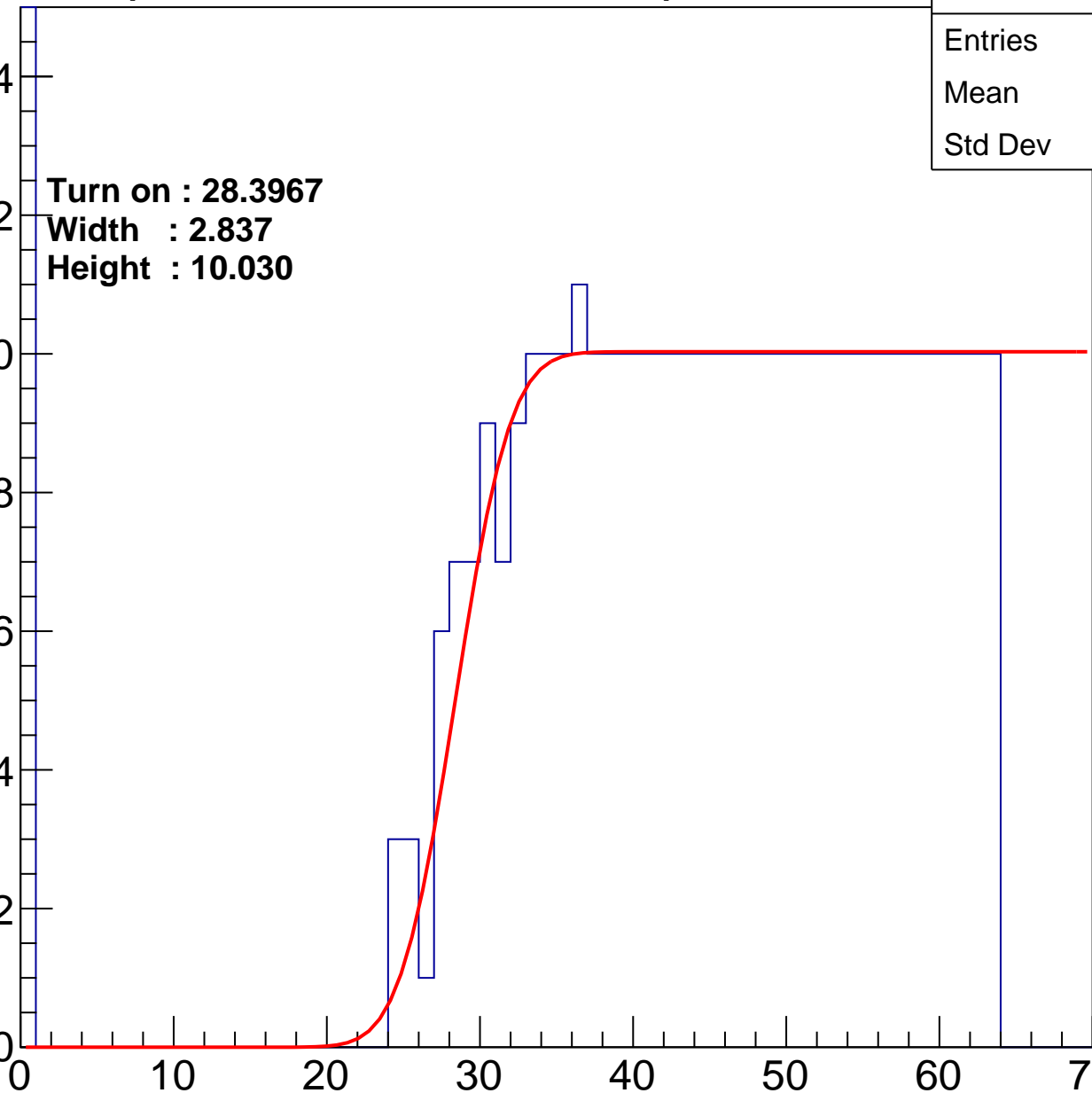
Width : 2.837

Height : 10.030

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch54

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	444
Mean	39.11
Std Dev	17.04

Turn on : 24.4374

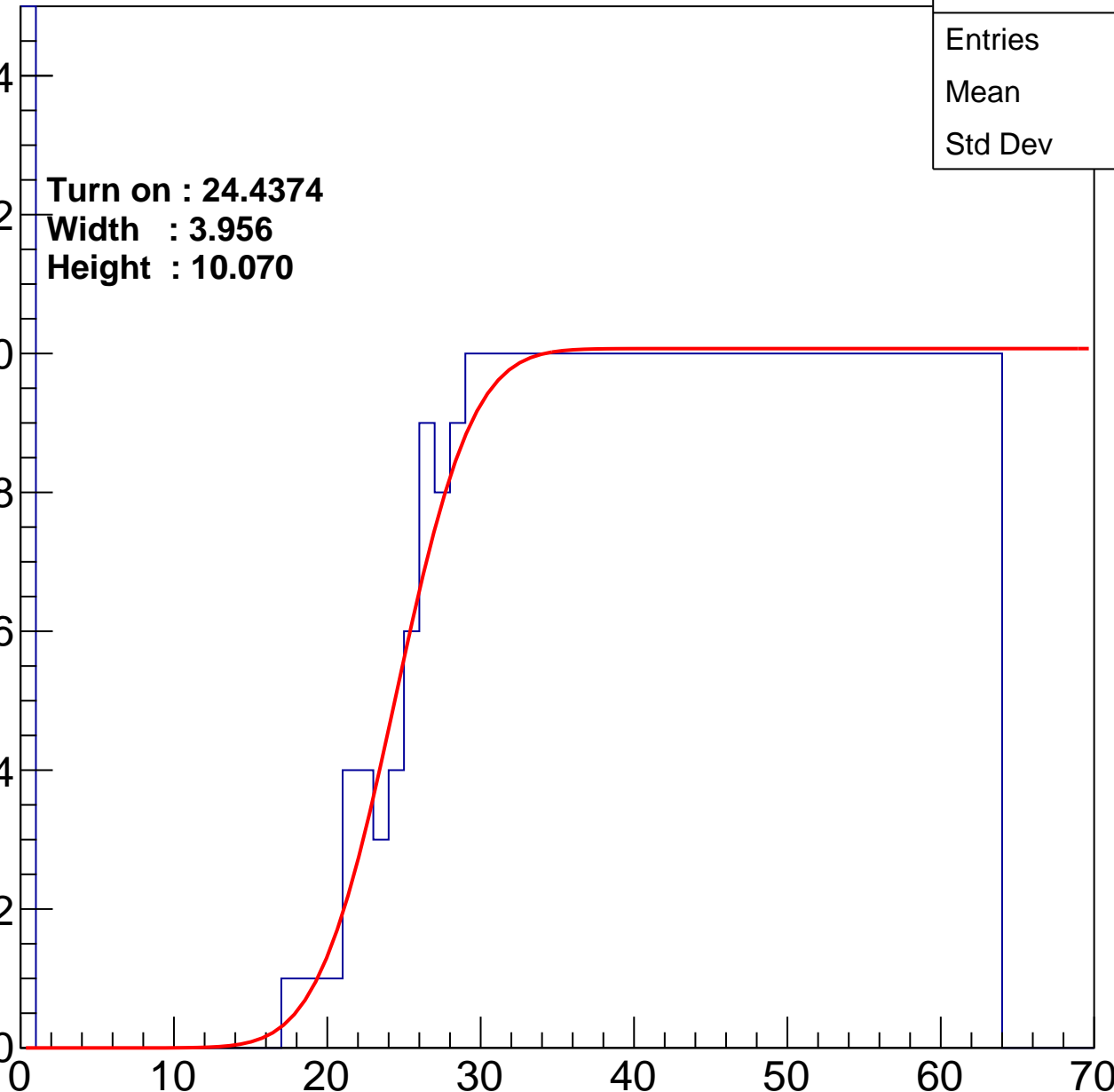
Width : 3.956

Height : 10.070

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U26-ch55

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	423
Mean	39.87
Std Dev	17.07

Turn on : 25.6300

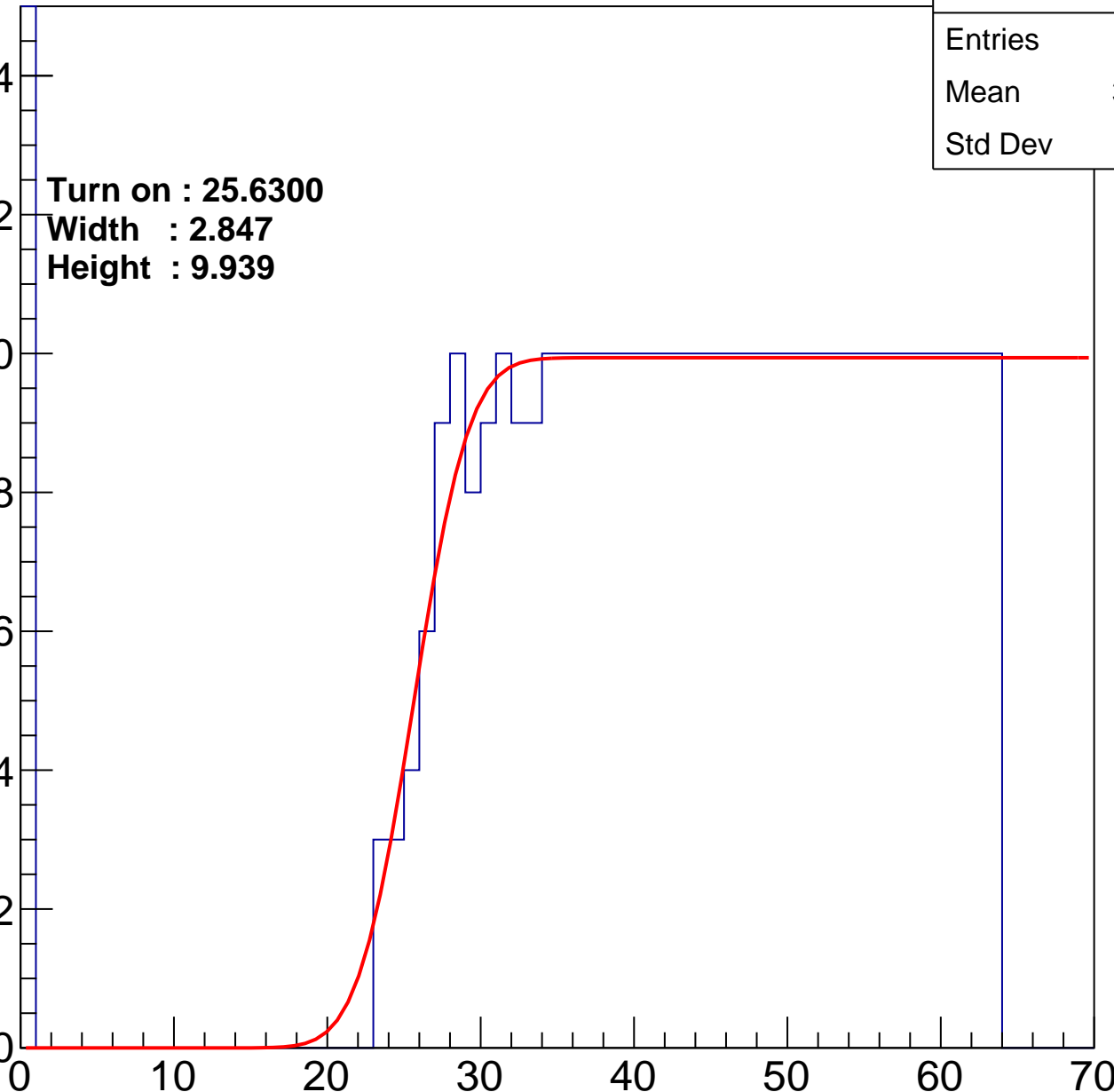
Width : 2.847

Height : 9.939

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch56

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	412
Mean	40.43
Std Dev	16.86

Turn on : 27.3323

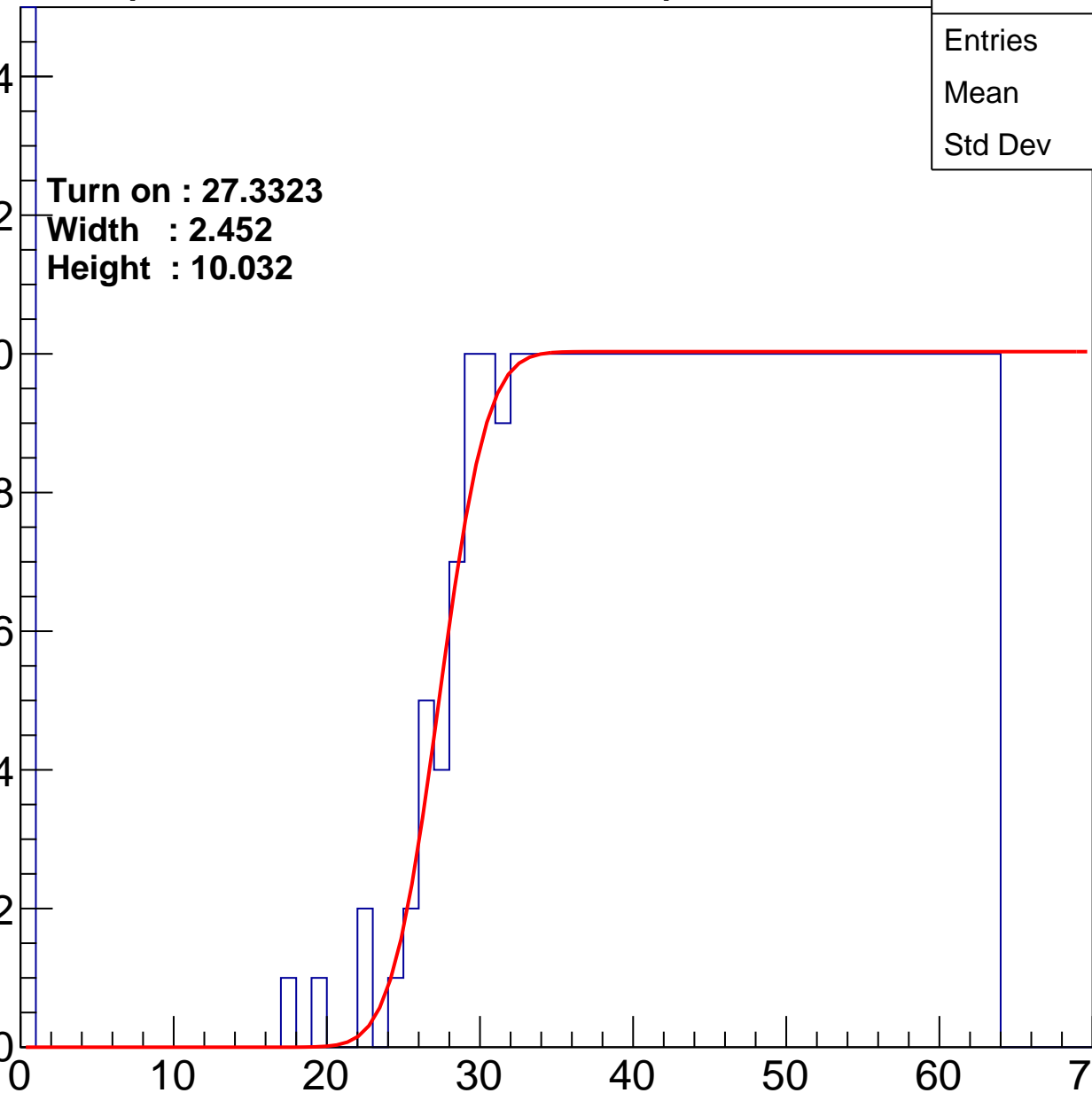
Width : 2.452

Height : 10.032

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch57

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	420
Mean	40.08
Std Dev	16.97

Turn on : 26.3150

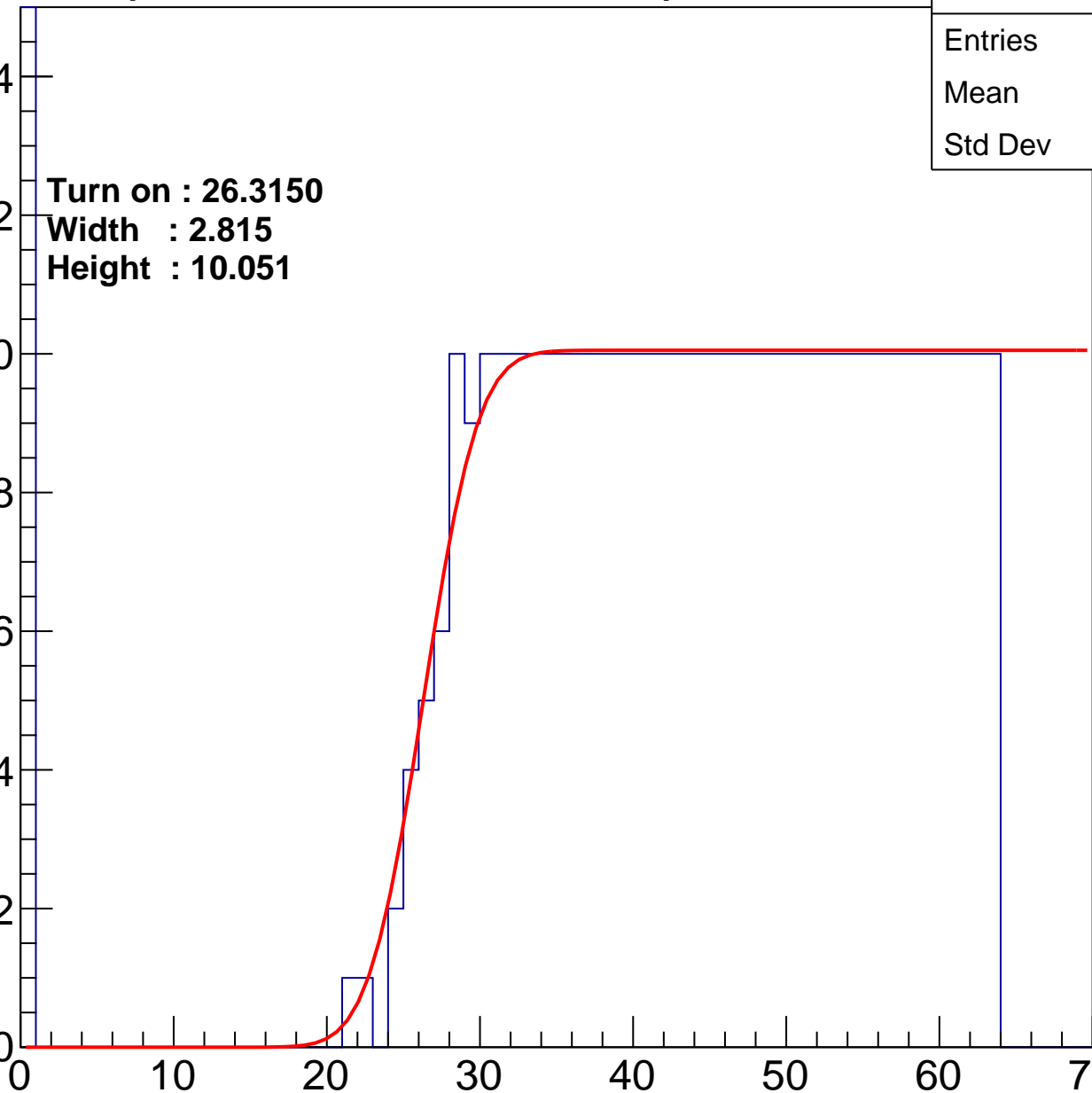
Width : 2.815

Height : 10.051

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch58

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	444
Mean	39.3
Std Dev	16.74

Turn on : 23.2900

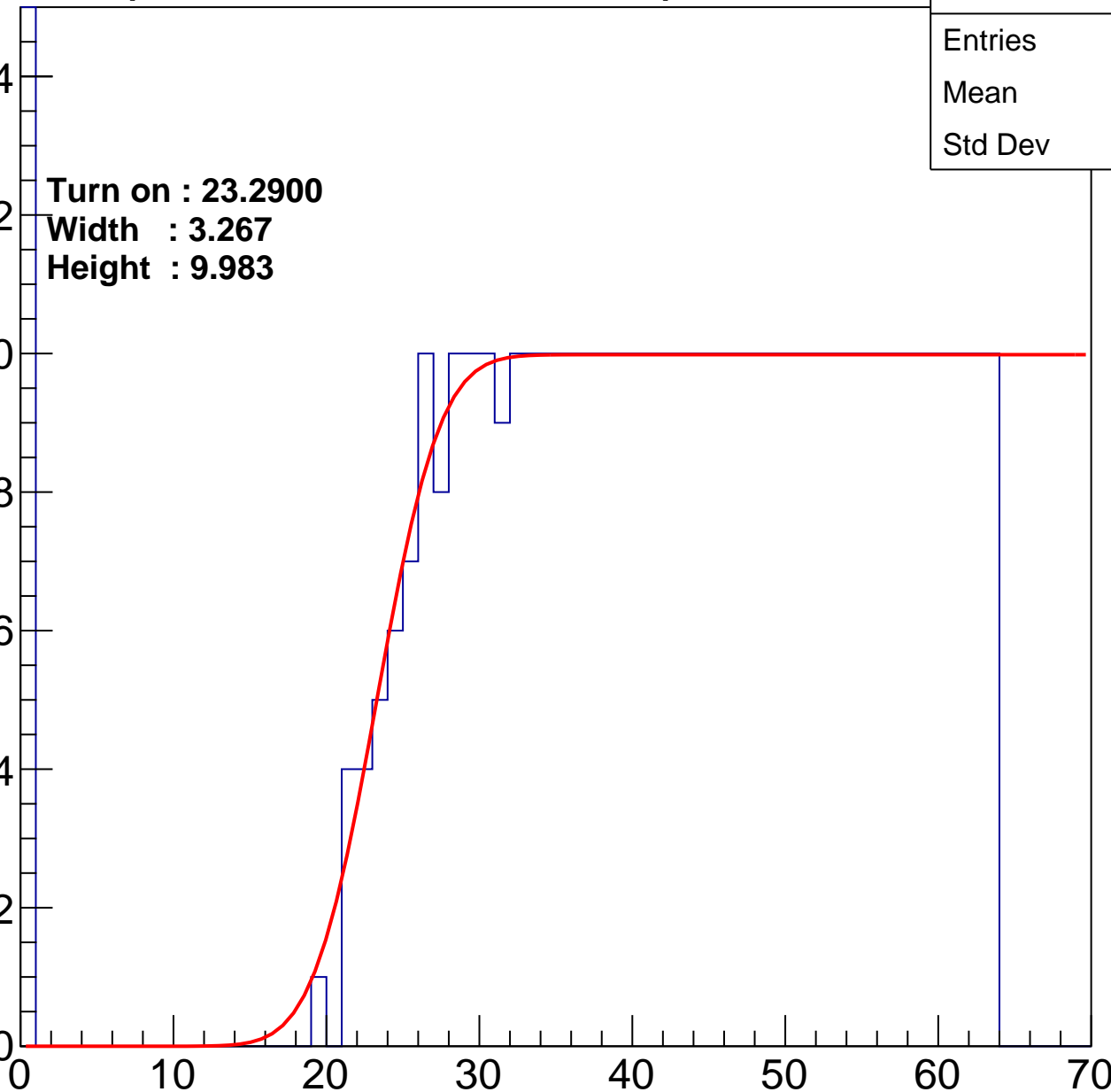
Width : 3.267

Height : 9.983

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch59

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	405
Mean	40.8
Std Dev	16.67

Turn on : 27.2550

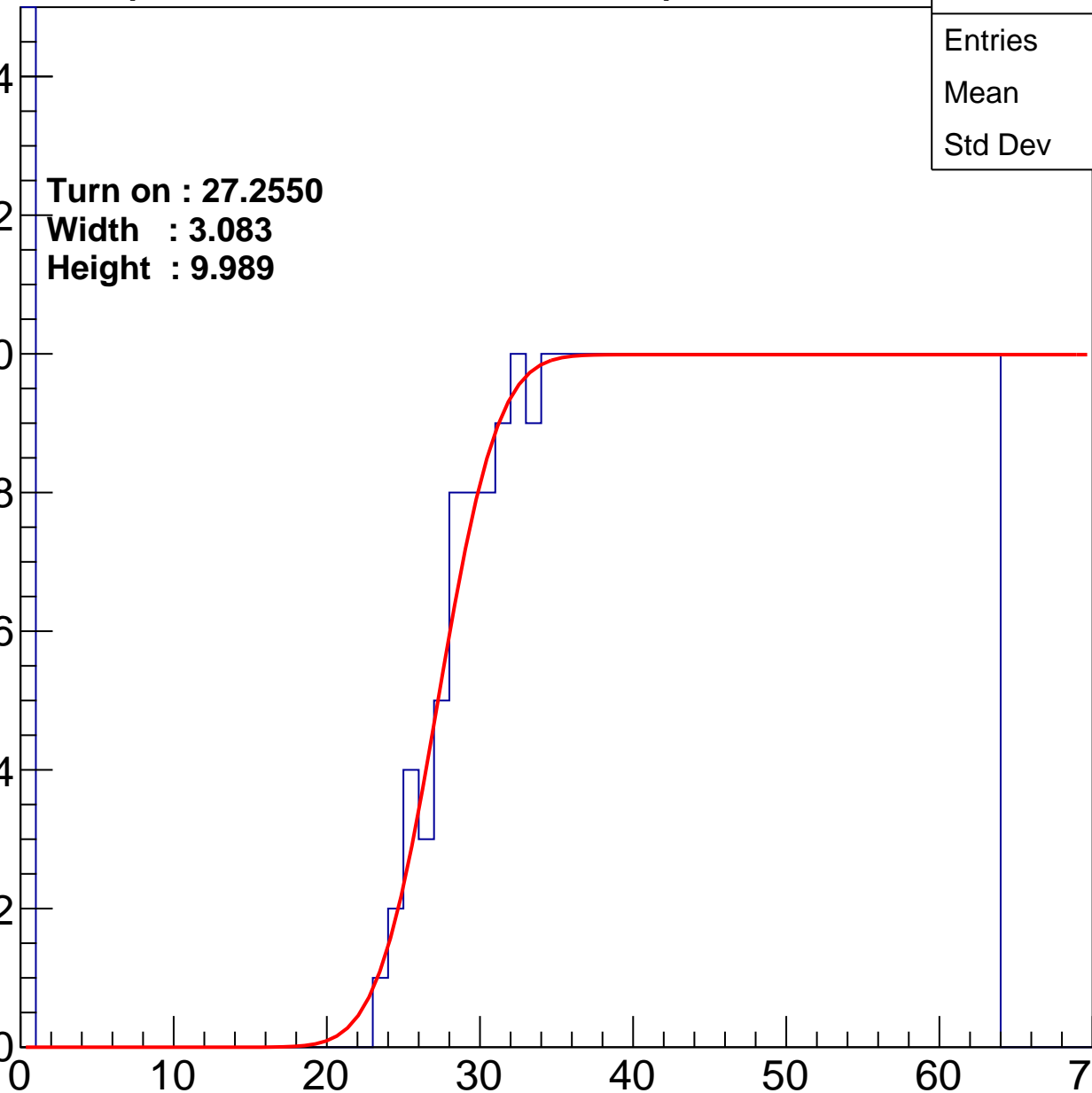
Width : 3.083

Height : 9.989

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch60

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	439
Mean	39.22
Std Dev	17.19

Turn on : 25.0061

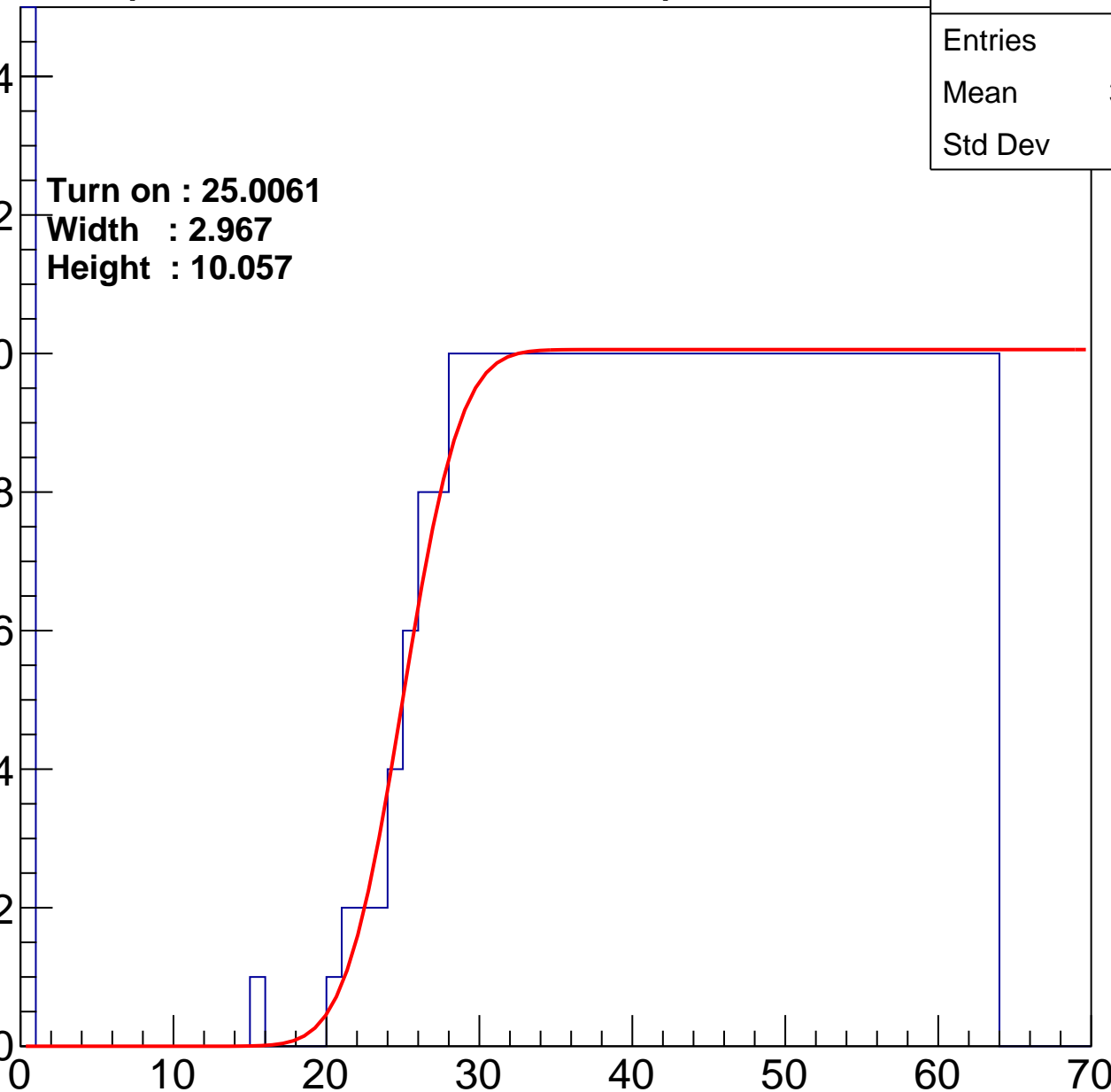
Width : 2.967

Height : 10.057

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch61

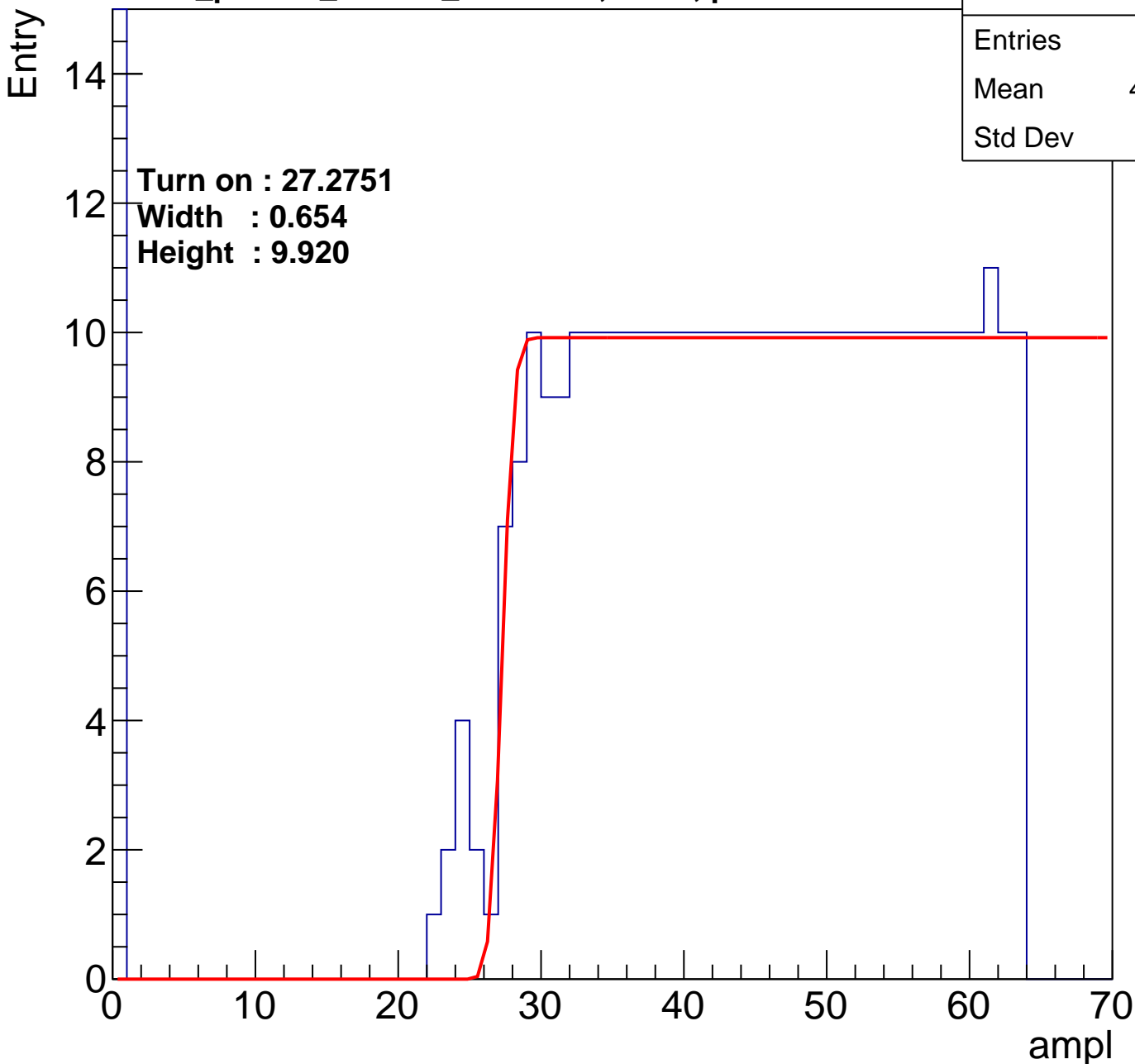
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	406
Mean	41.26
Std Dev	16.01

Turn on : 27.2751

Width : 0.654

Height : 9.920



# B1L103S, U26-ch62

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	445
Mean	38.79
Std Dev	17.47

Turn on : 25.0314

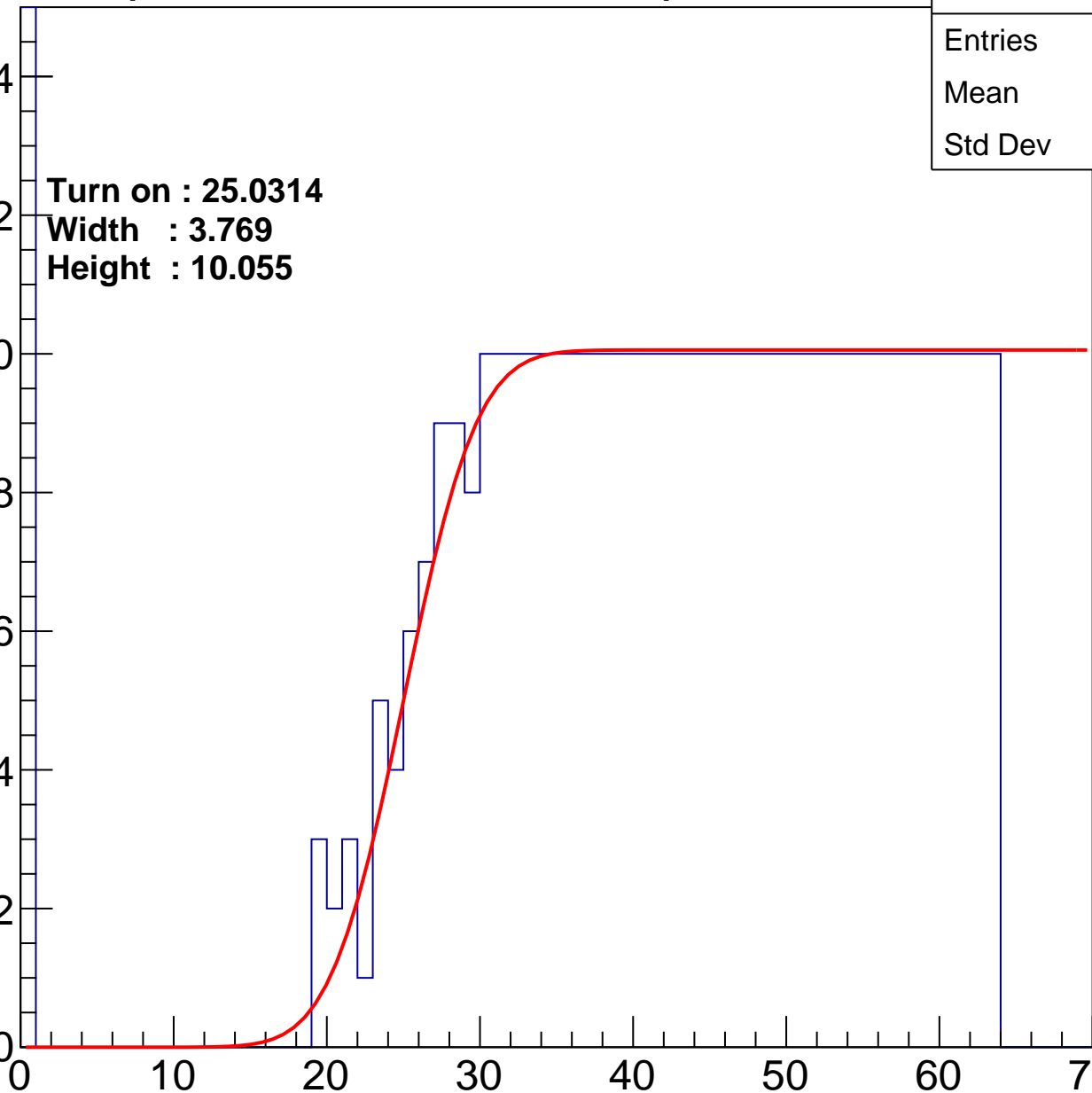
Width : 3.769

Height : 10.055

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U26-ch63

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	421
Mean	39.98
Std Dev	17.06

Turn on : 26.1524

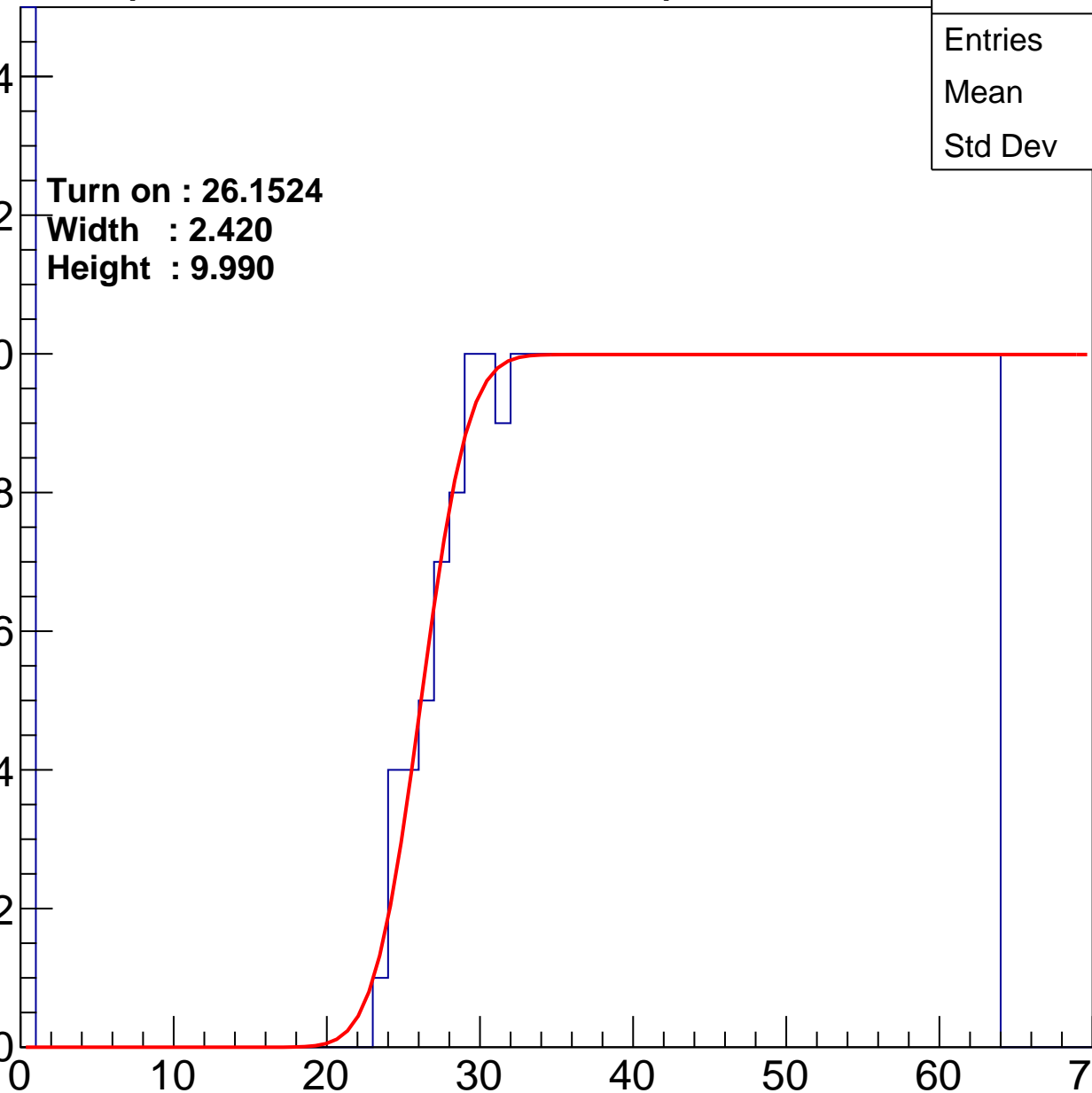
Width : 2.420

Height : 9.990

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch64

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	428
Mean	39.57
Std Dev	17.26

Turn on : 26.1244

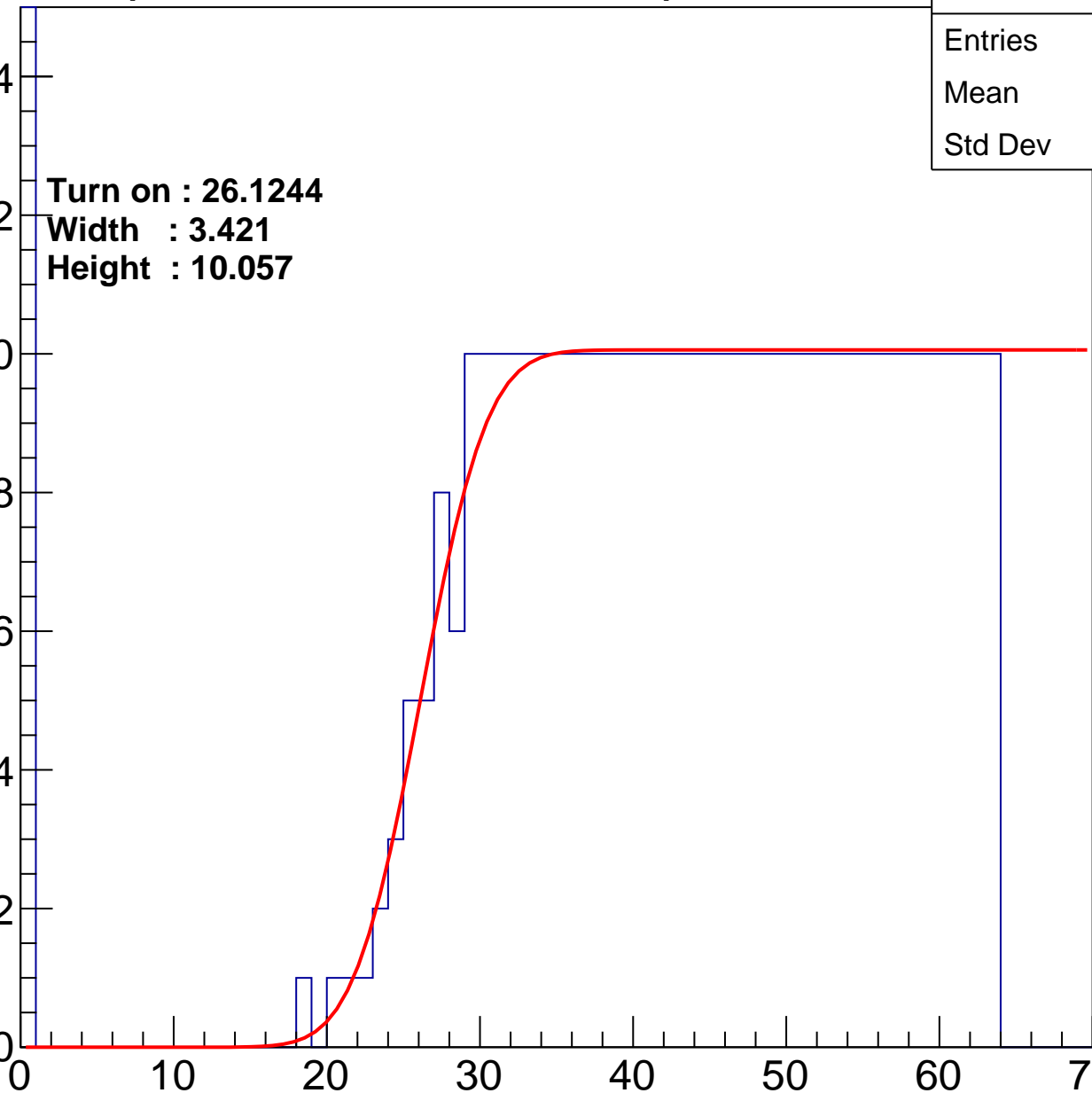
Width : 3.421

Height : 10.057

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch65

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	410
Mean	40.57
Std Dev	16.75

Turn on : 27.1346

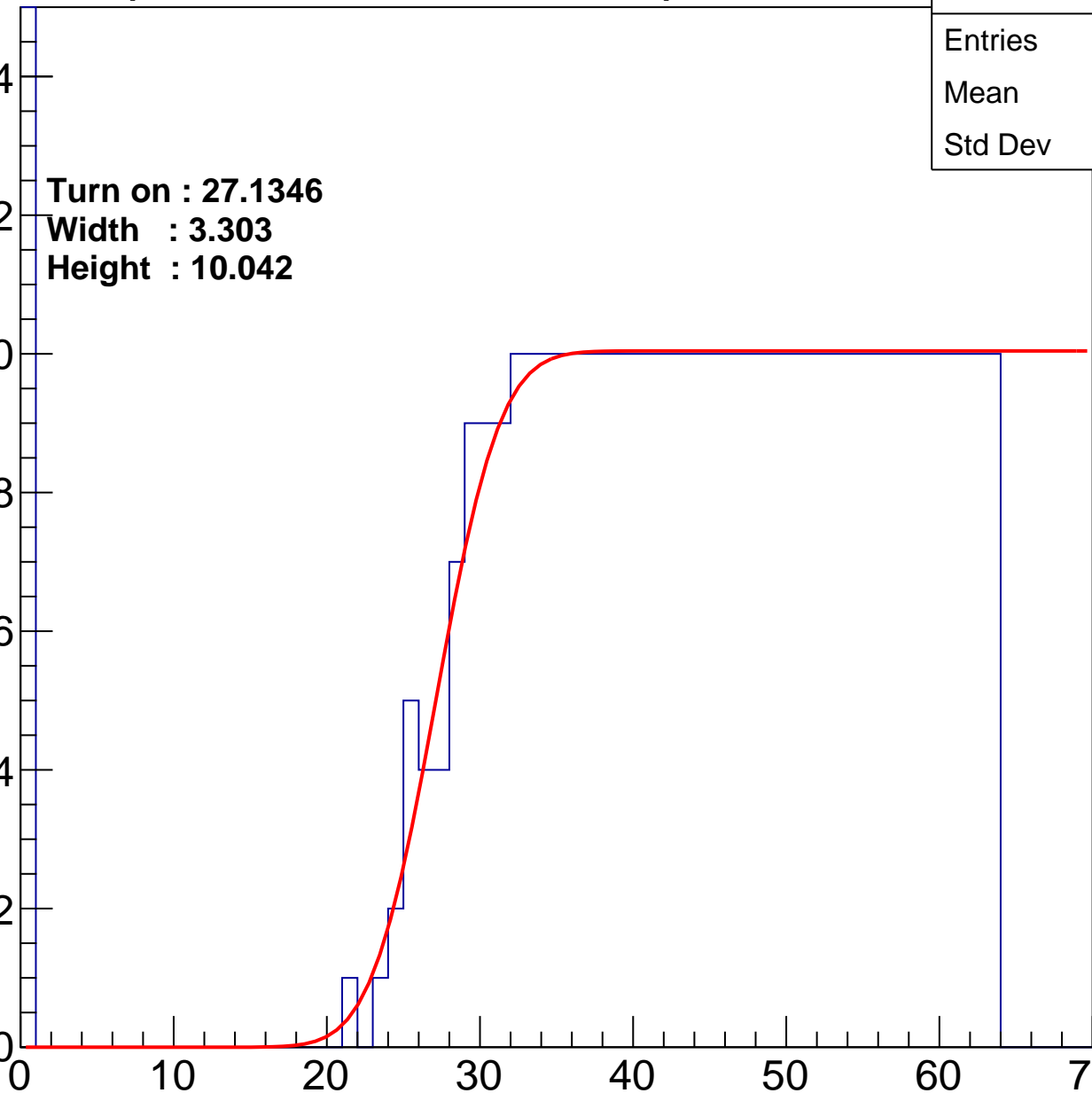
Width : 3.303

Height : 10.042

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch66

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	431
Mean	39.19
Std Dev	17.68

**Turn on : 26.2849**

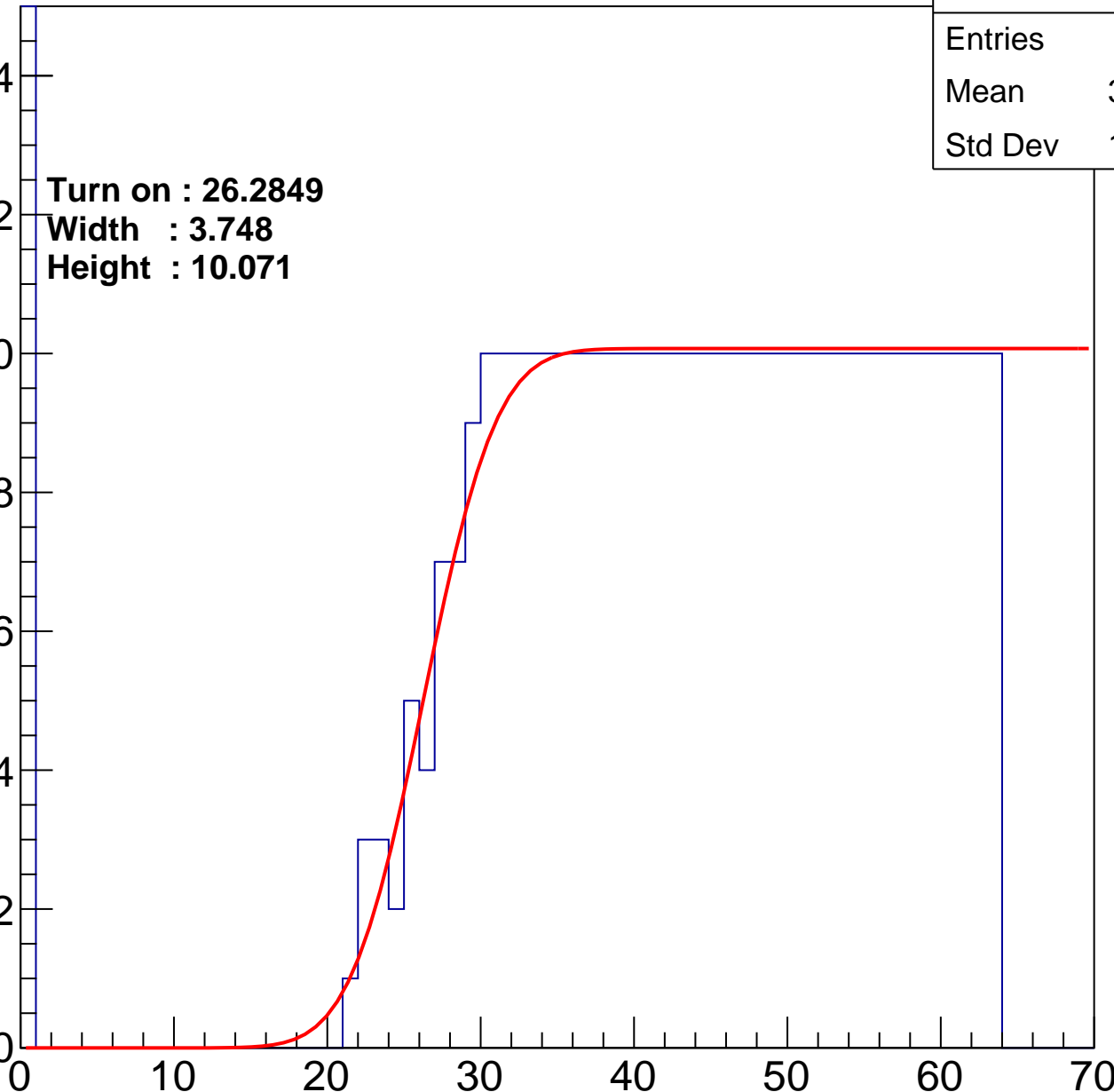
**Width : 3.748**

**Height : 10.071**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch67

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	439
Mean	39.53
Std Dev	16.67

Turn on : 23.8238

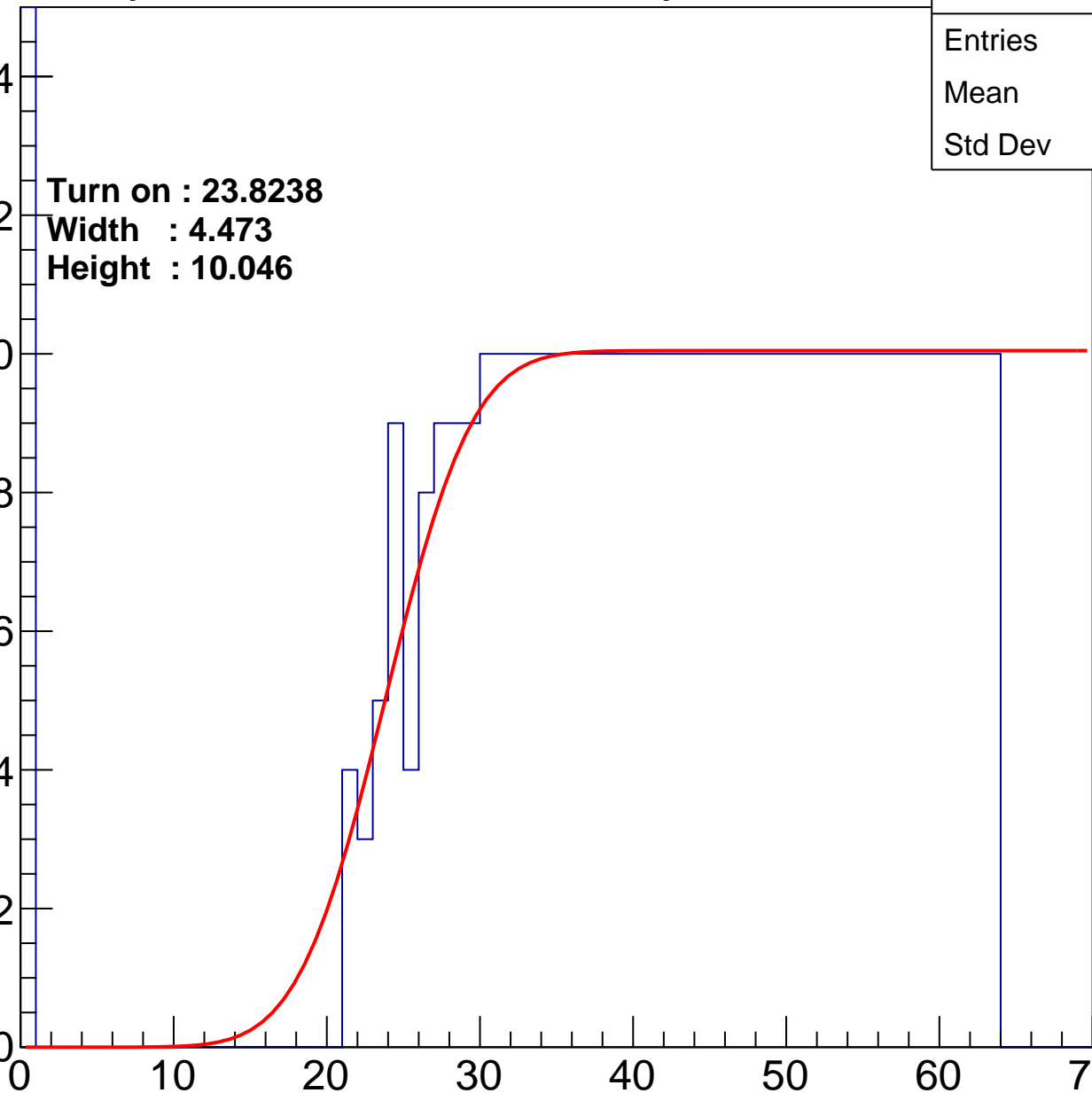
Width : 4.473

Height : 10.046

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch68

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	454
Mean	38.09
Std Dev	18.03

Turn on : 24.3833

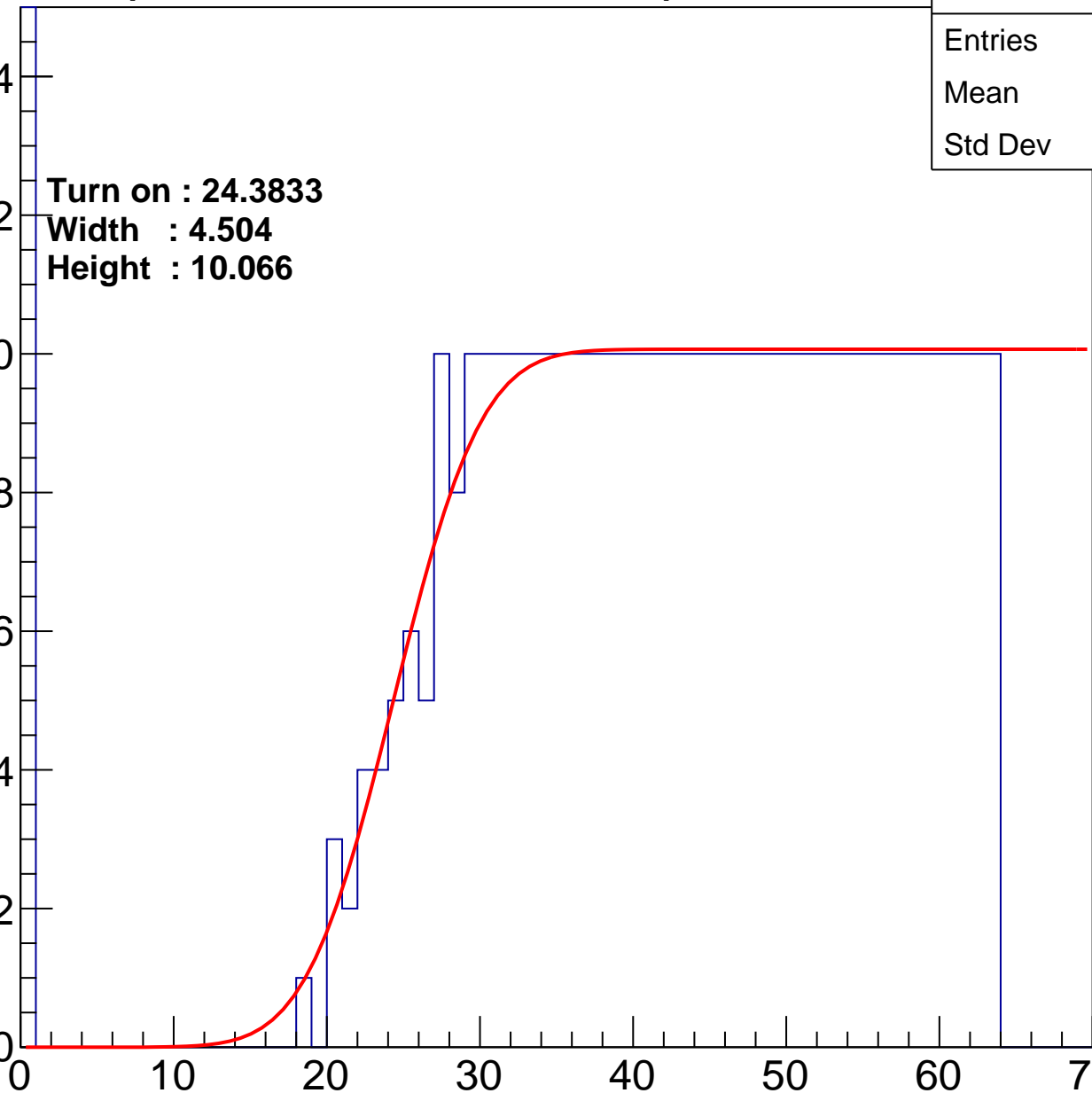
Width : 4.504

Height : 10.066

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch69

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	429
Mean	39.61
Std Dev	17.14

Turn on : 24.9223

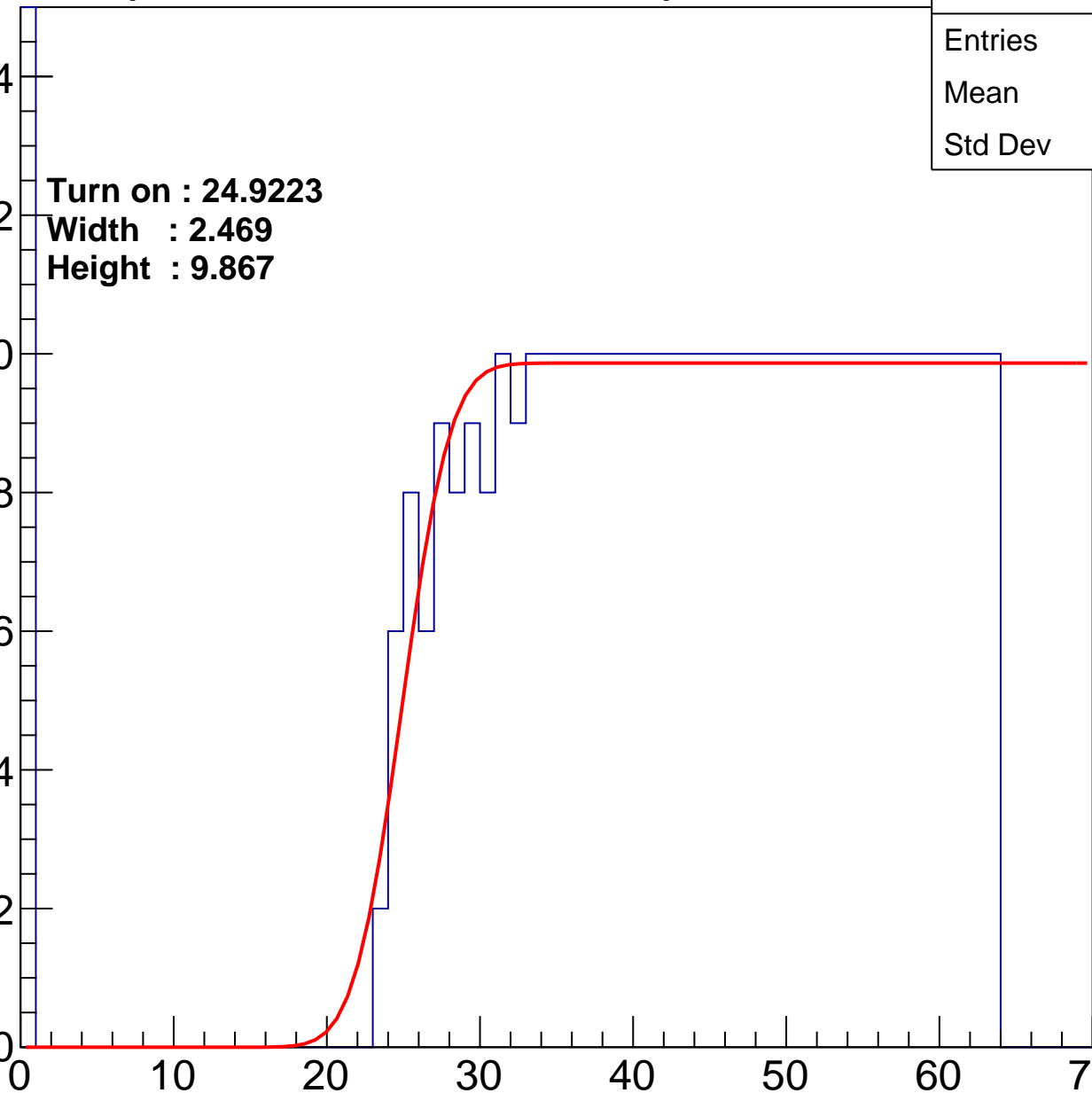
Width : 2.469

Height : 9.867

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch70

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	440
Mean	39.23
Std Dev	17.1

Turn on : 24.6337

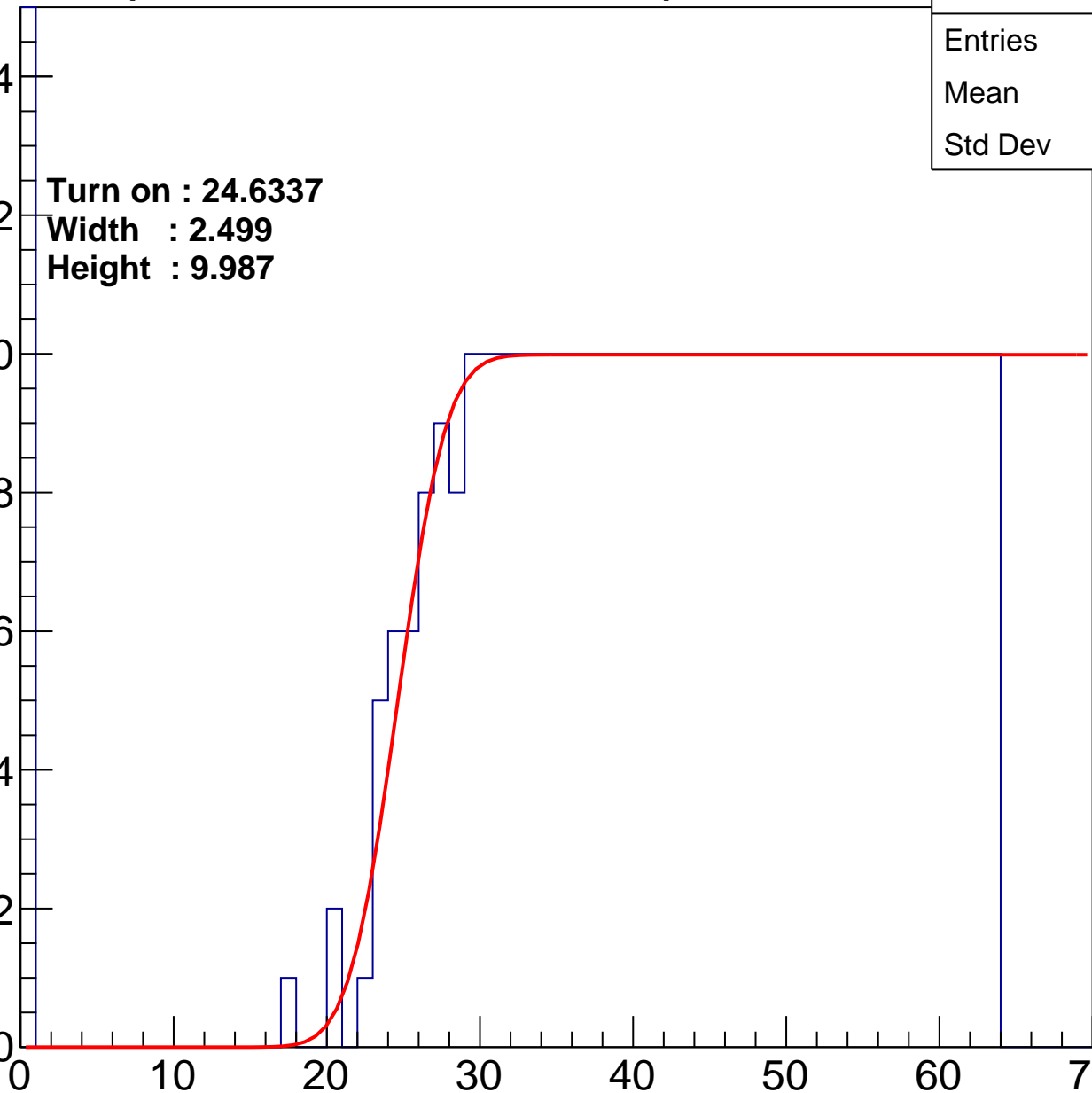
Width : 2.499

Height : 9.987

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U26-ch71

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	424
Mean	39.71
Std Dev	17.27

**Turn on : 26.9587**

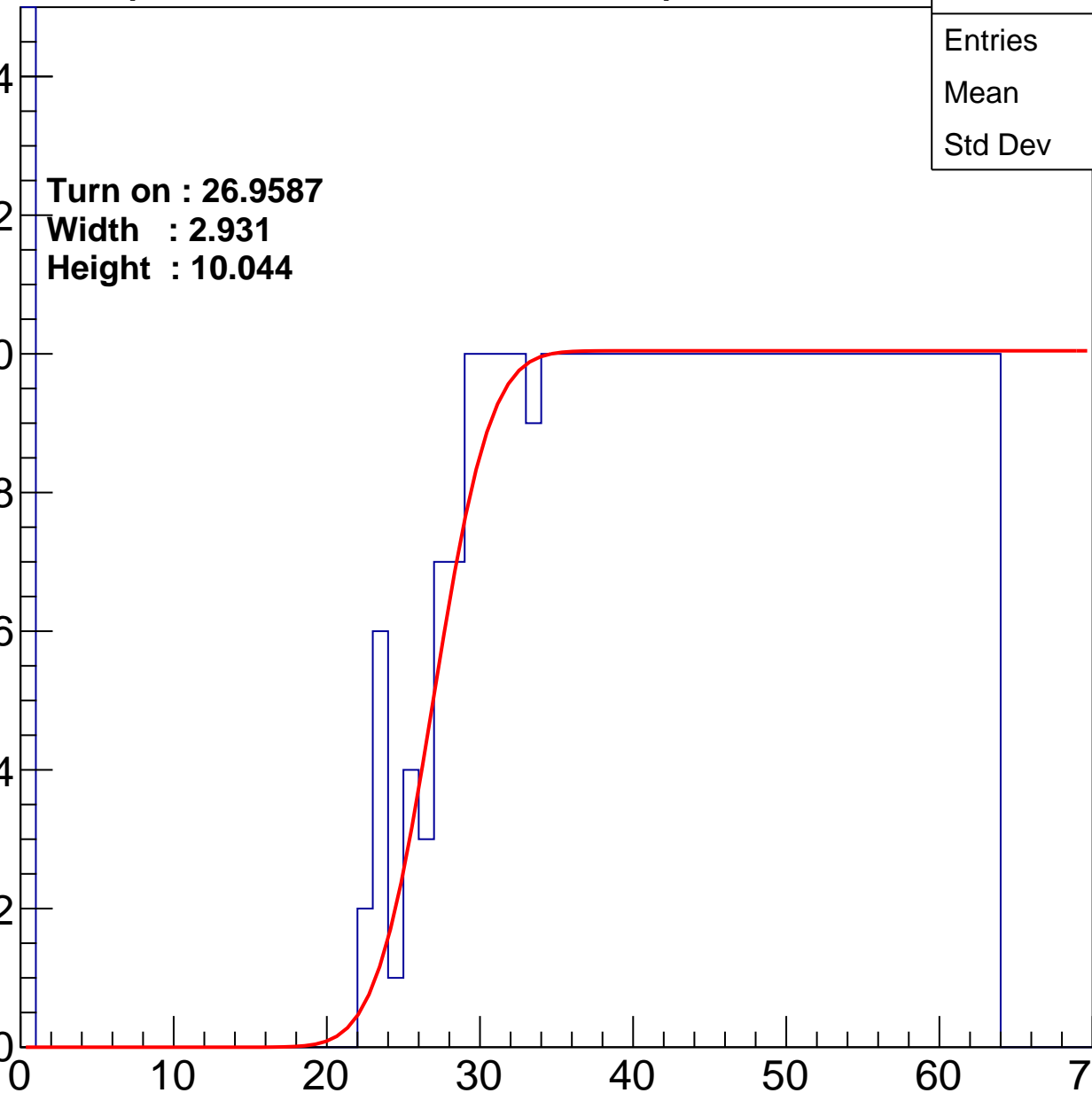
**Width : 2.931**

**Height : 10.044**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch72

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	459
Mean	38.13
Std Dev	17.74

Turn on : 23.8100

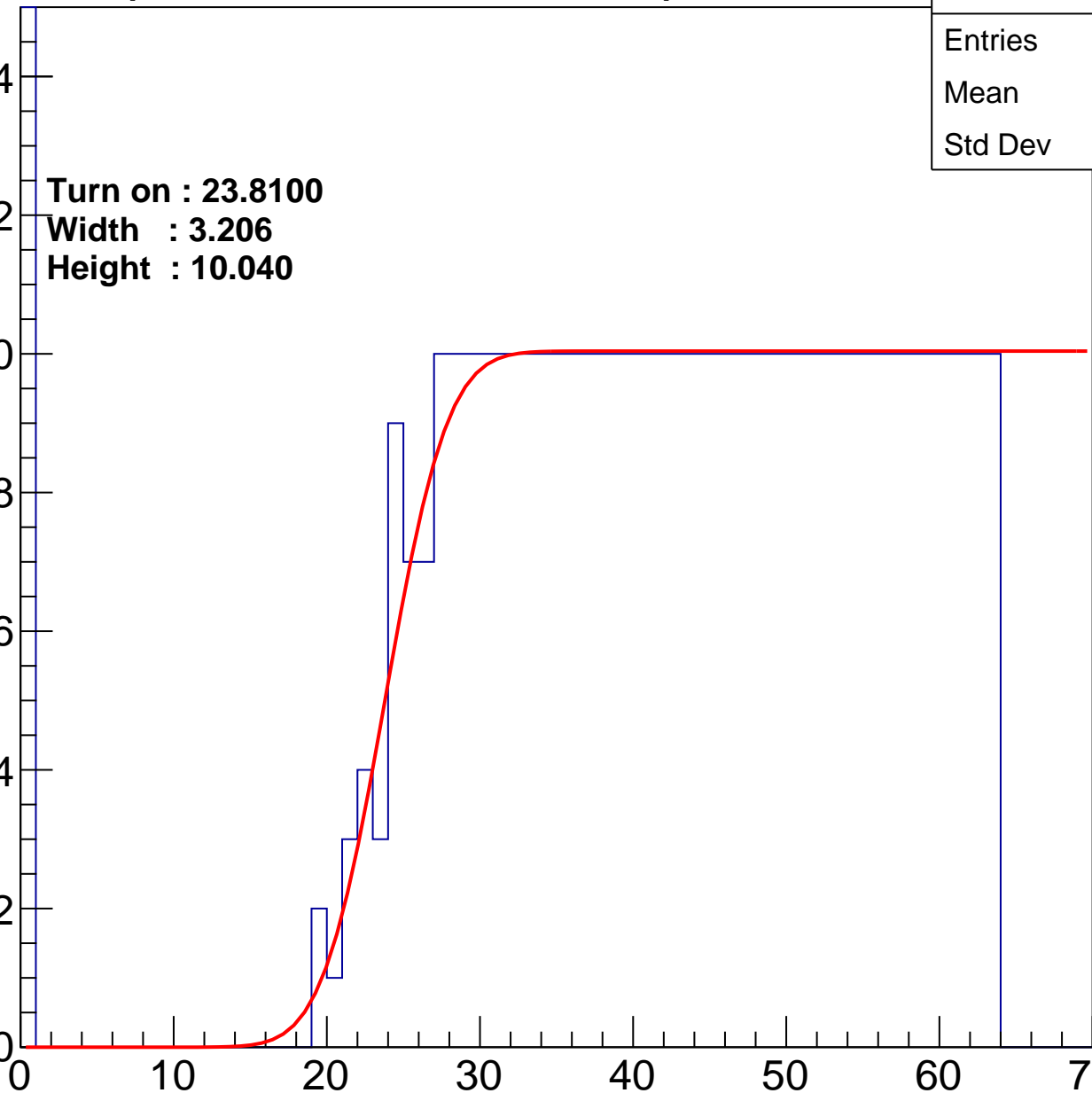
Width : 3.206

Height : 10.040

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch73

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	420
Mean	40.3
Std Dev	16.59

Turn on : 25.8216

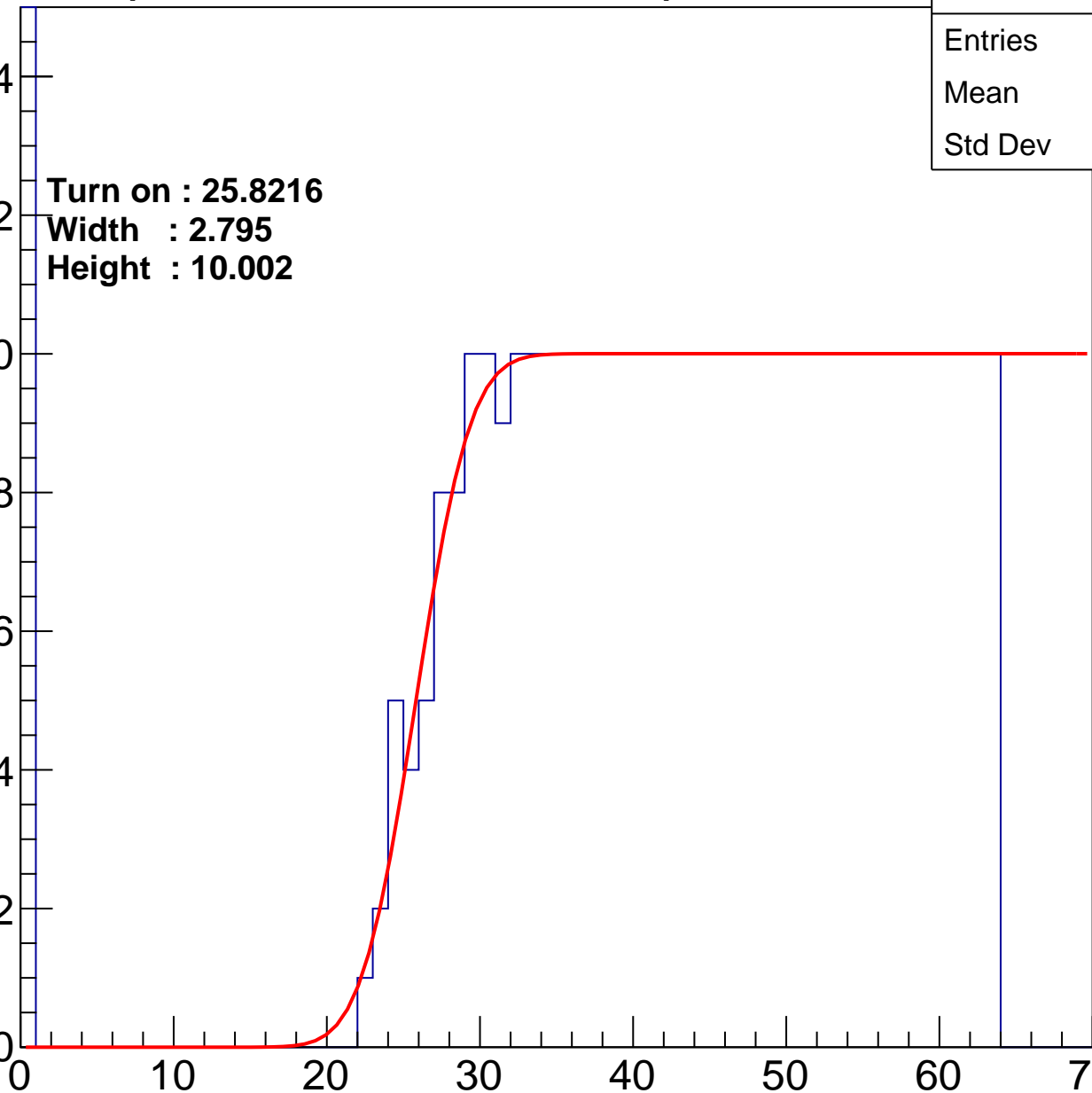
Width : 2.795

Height : 10.002

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch74

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	432
Mean	39.73
Std Dev	16.82

Turn on : 24.9540

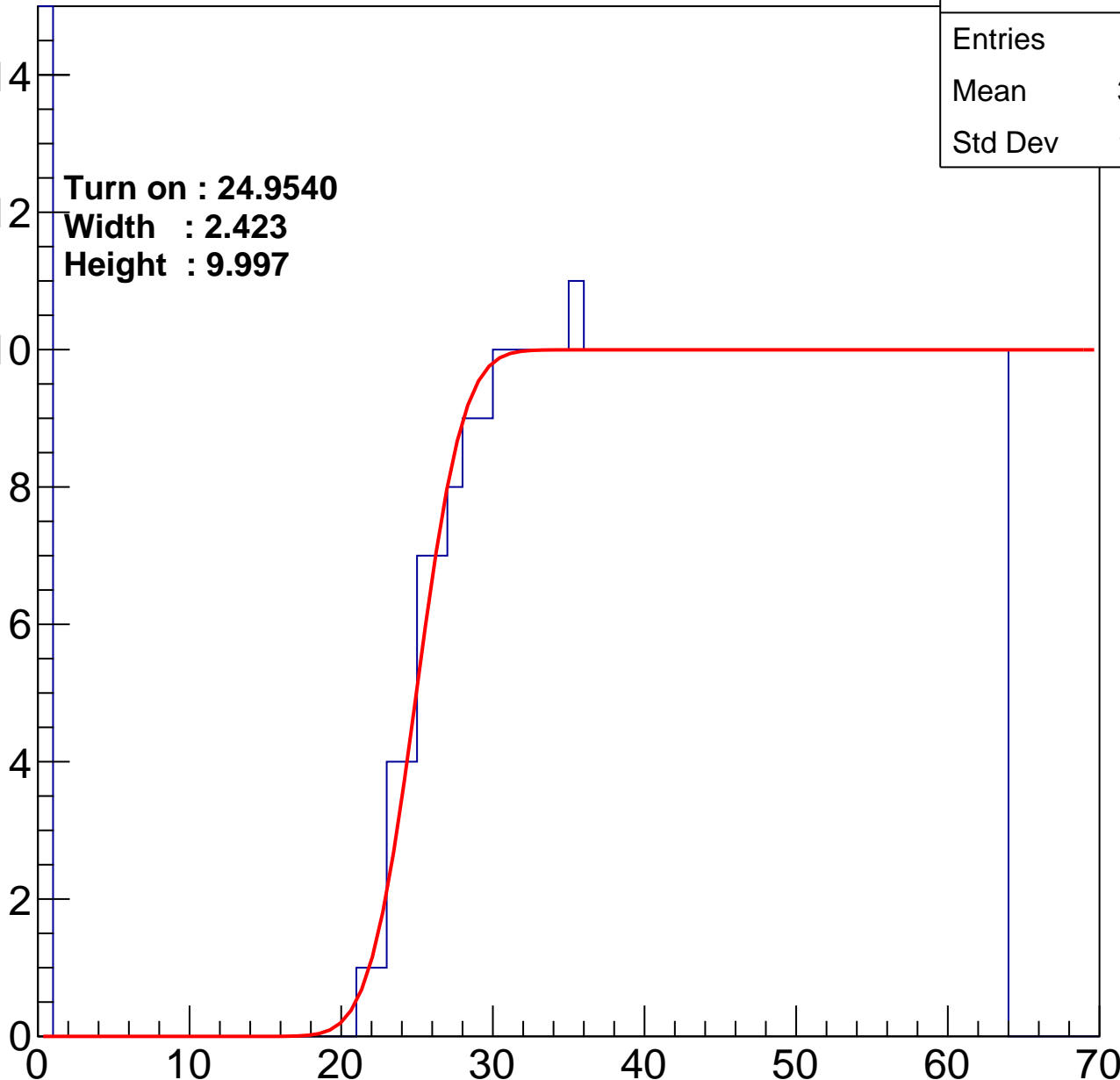
Width : 2.423

Height : 9.997

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch75

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	416
Mean	40.37
Std Dev	16.72

**Turn on : 26.8263**

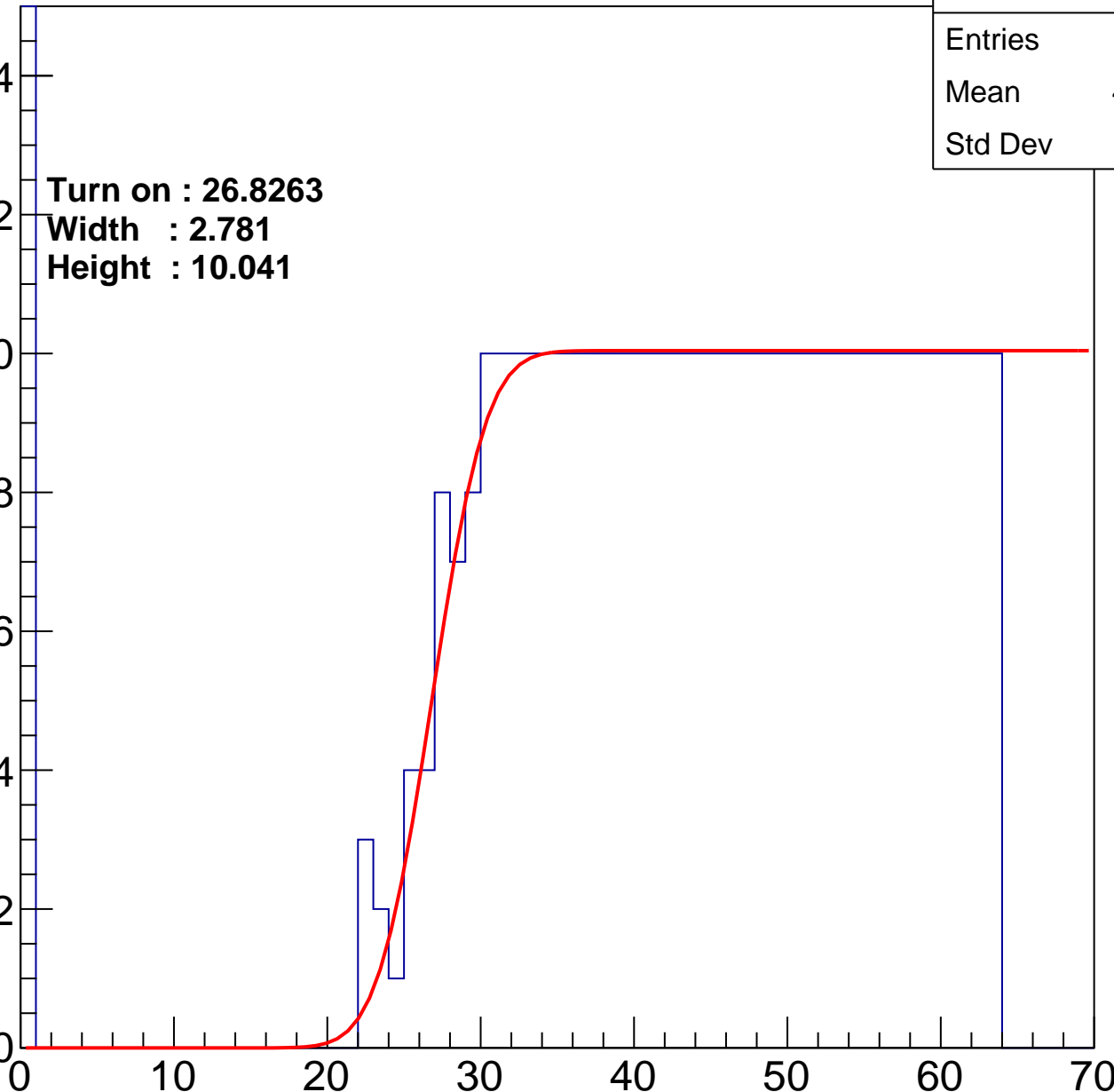
**Width : 2.781**

**Height : 10.041**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch76

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	458
Mean	38.14
Std Dev	17.8

Turn on : 23.7923

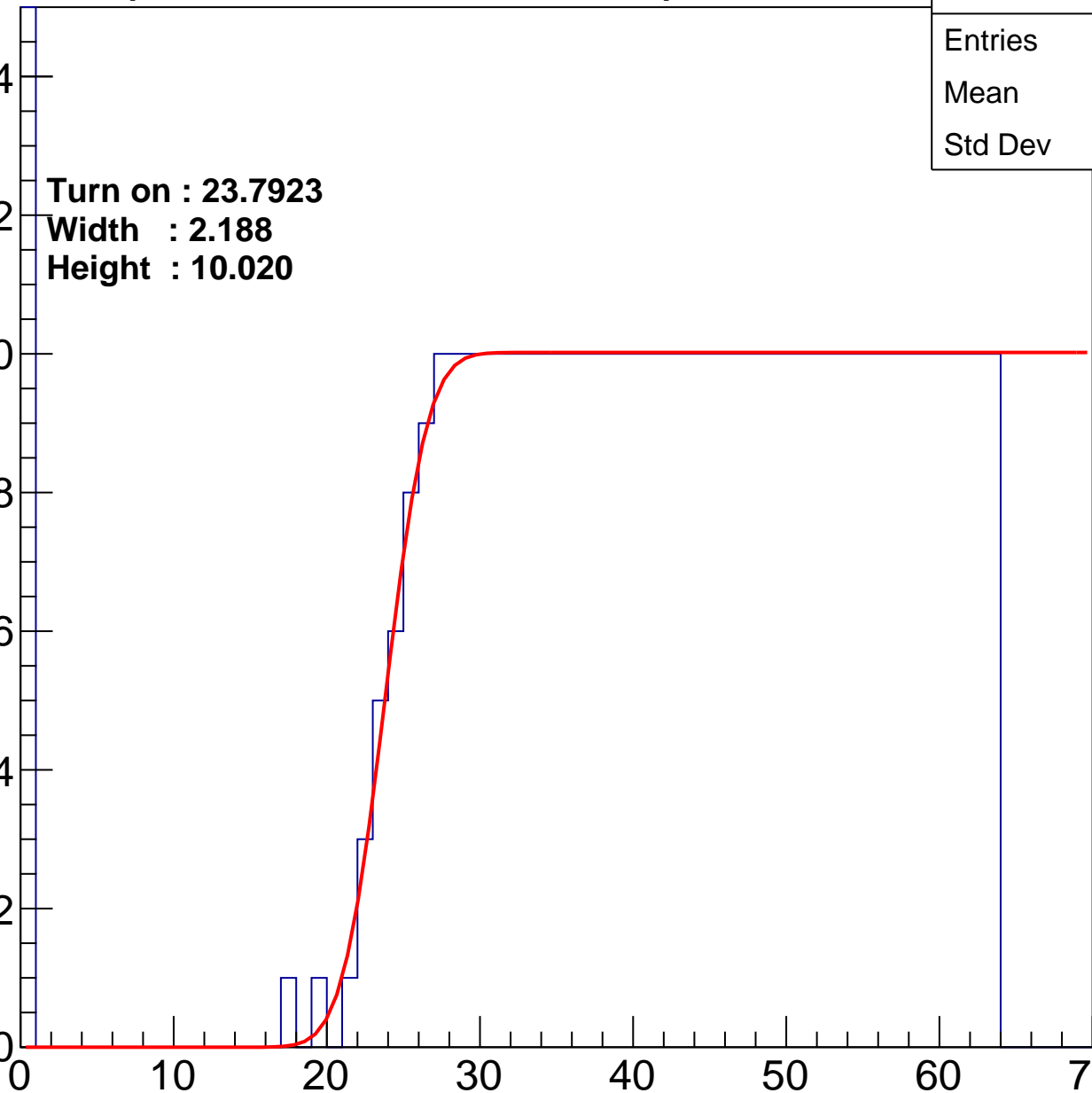
Width : 2.188

Height : 10.020

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch77

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	418
Mean	39.7
Std Dev	17.66

**Turn on : 27.2744**

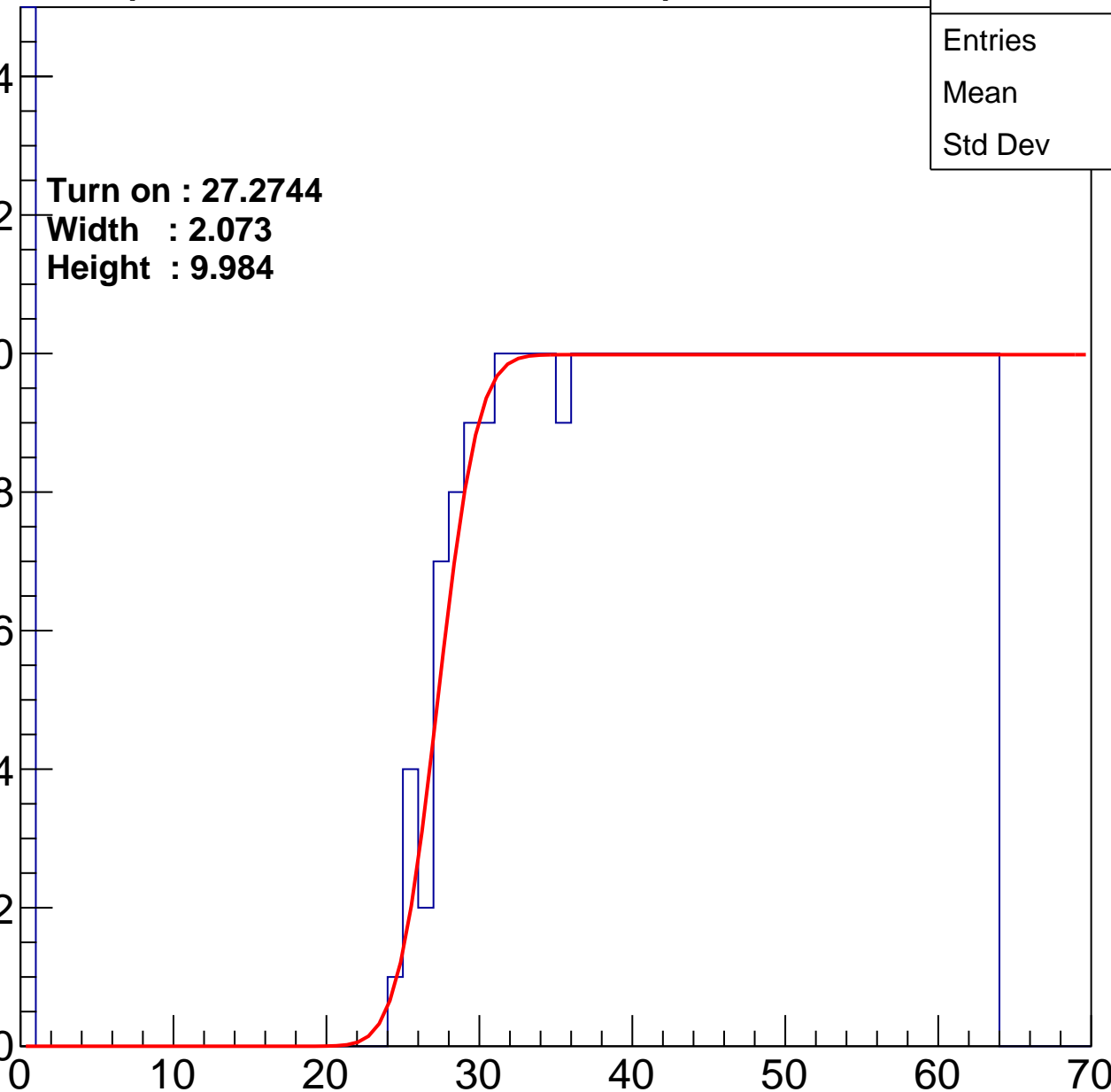
**Width : 2.073**

**Height : 9.984**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch78

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	448
Mean	39.29
Std Dev	16.51

**Turn on : 22.9938**

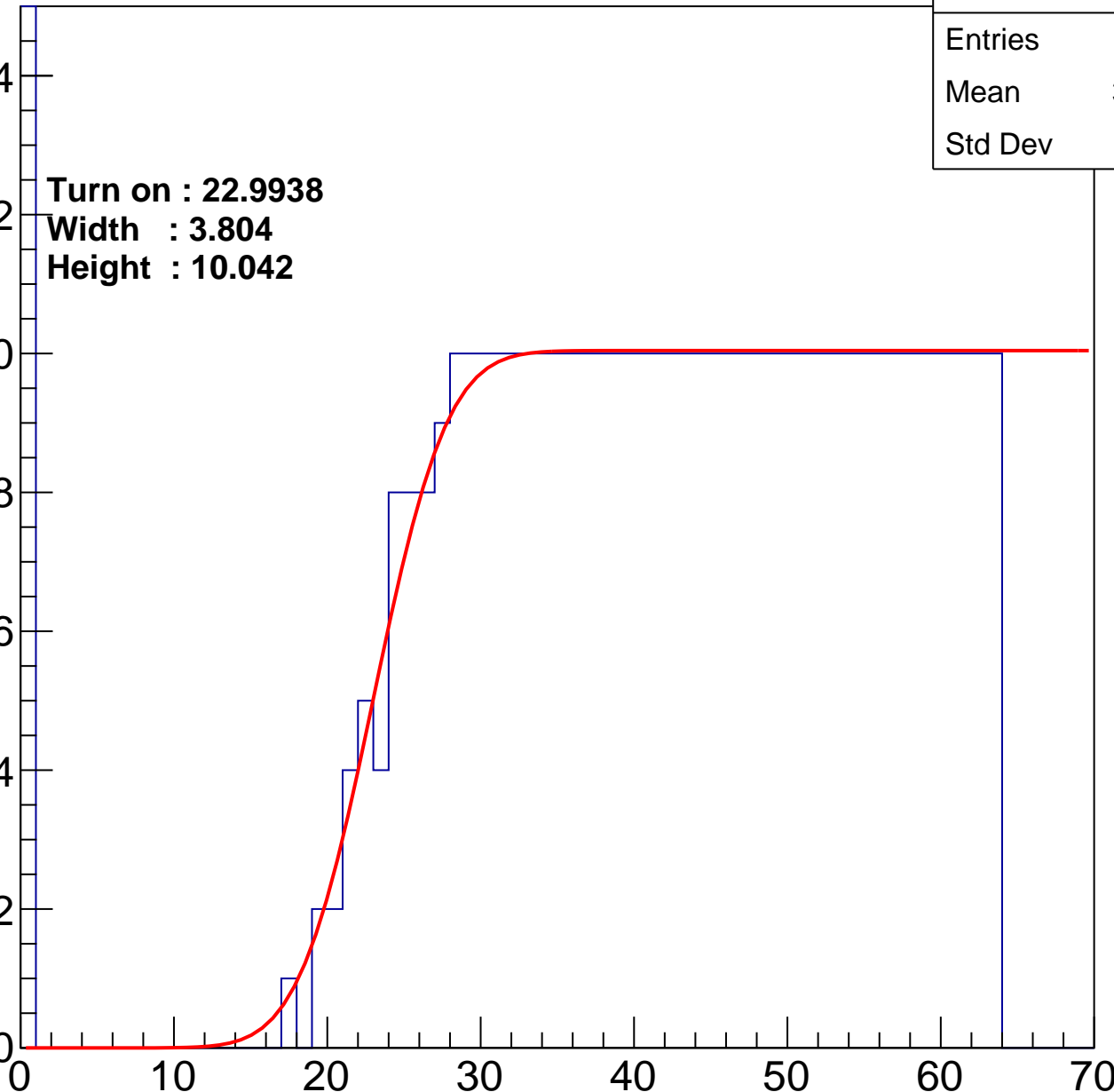
**Width : 3.804**

**Height : 10.042**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U26-ch79

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	432
Mean	39.24
Std Dev	17.58

Turn on : 25.6296

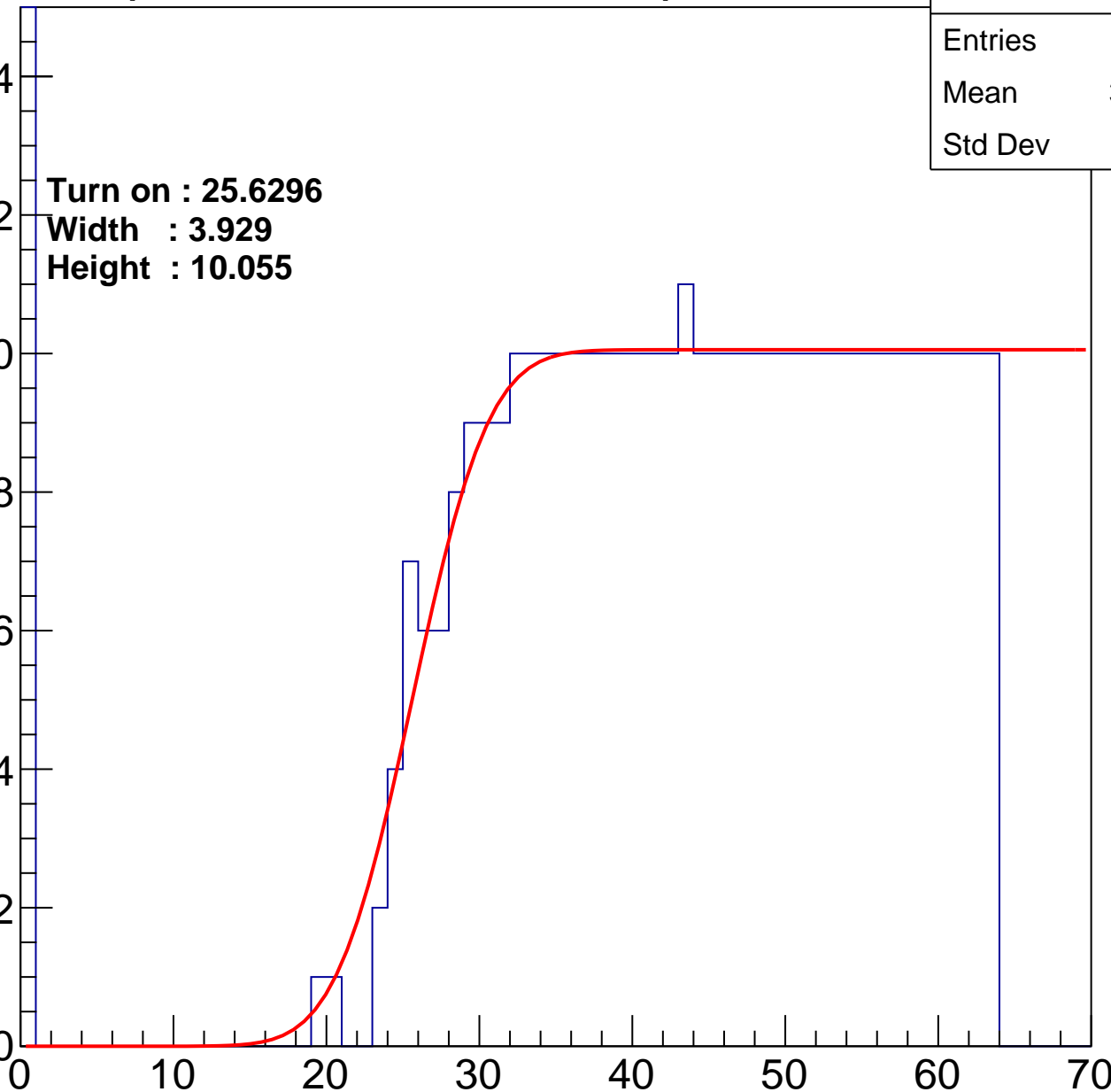
Width : 3.929

Height : 10.055

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch80

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	448
Mean	38.39
Std Dev	17.91

Turn on : 25.1833

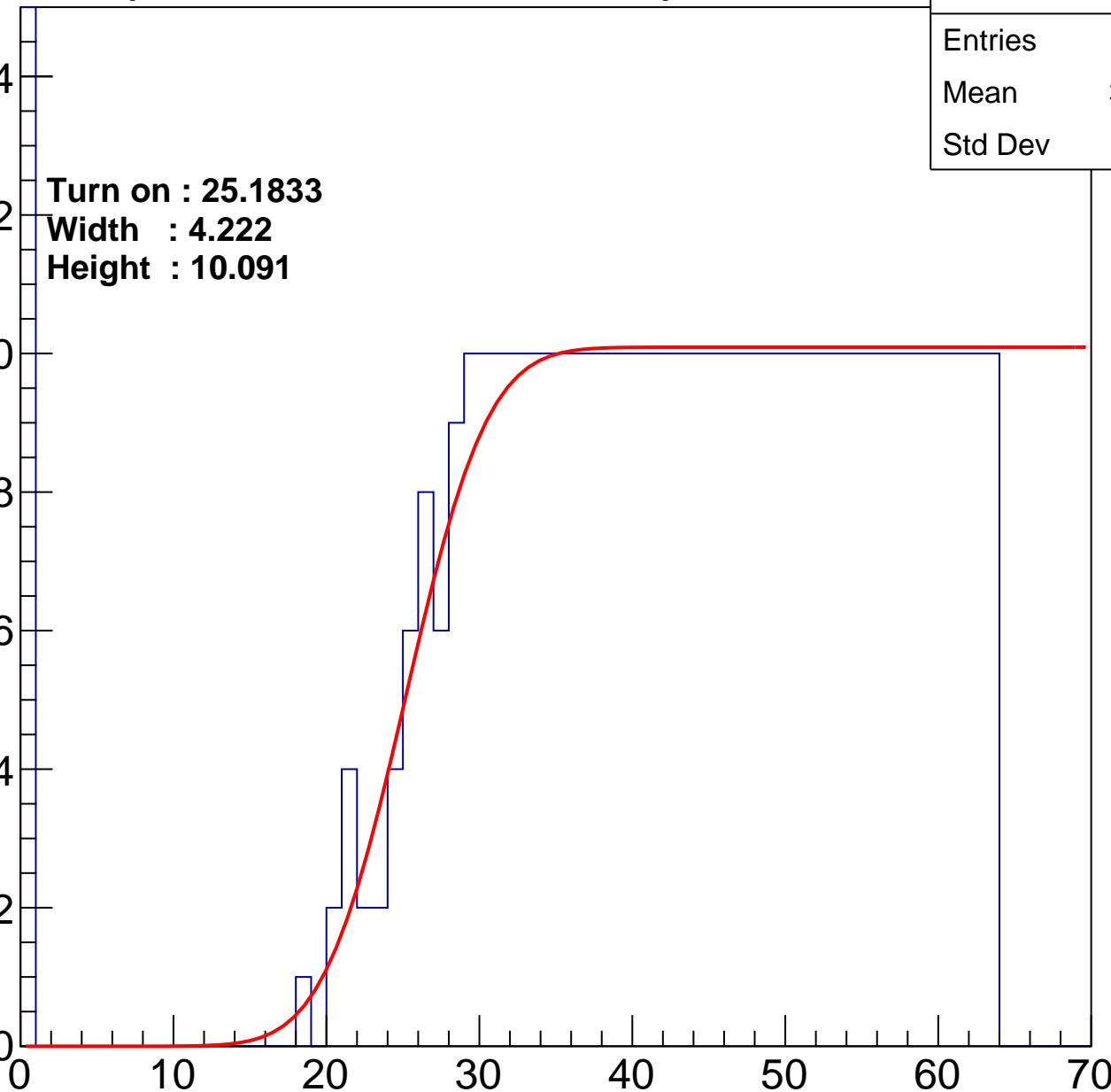
Width : 4.222

Height : 10.091

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch81

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	429
Mean	39.95
Std Dev	16.56

**Turn on : 24.7533**

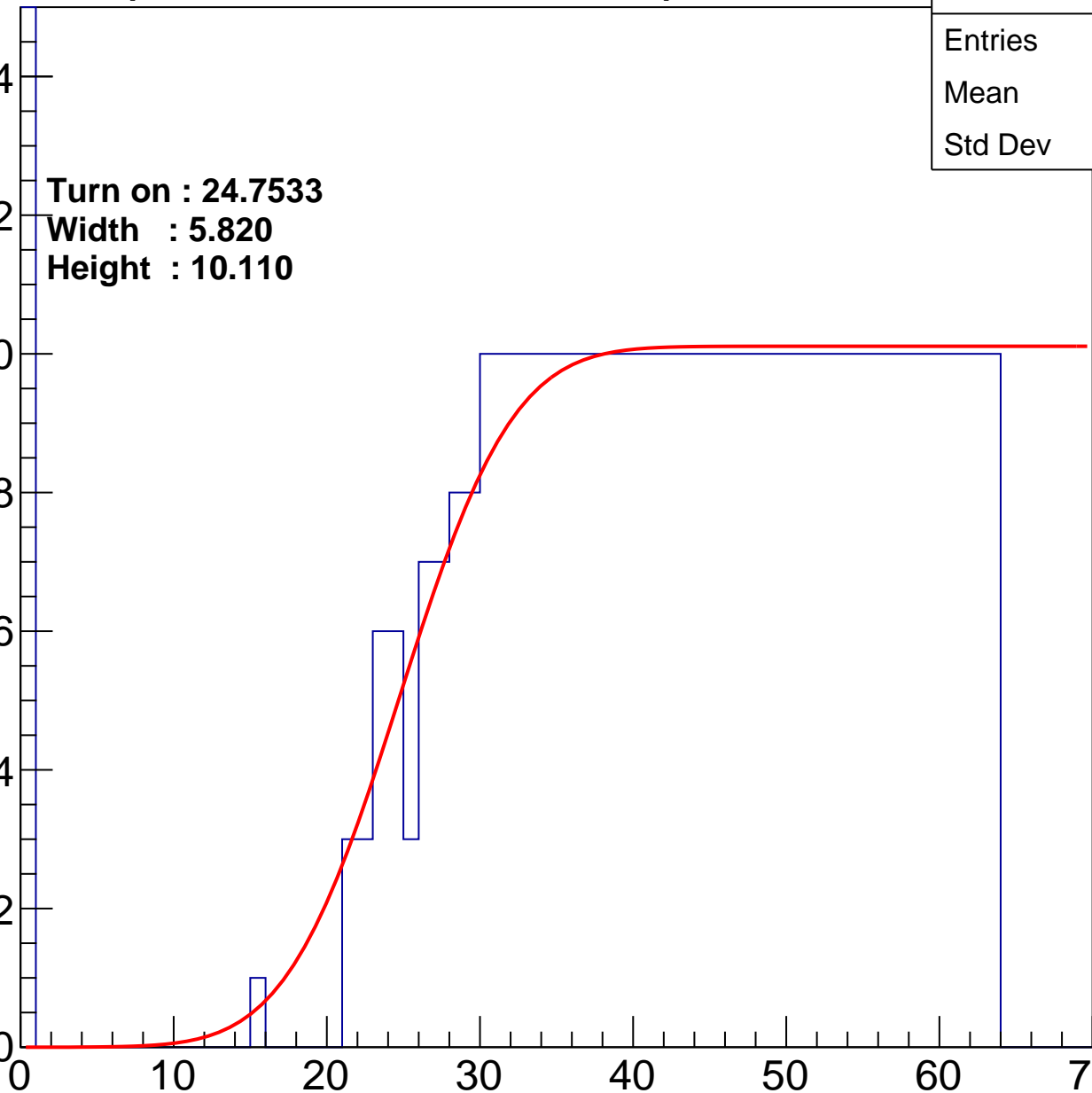
**Width : 5.820**

**Height : 10.110**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch82

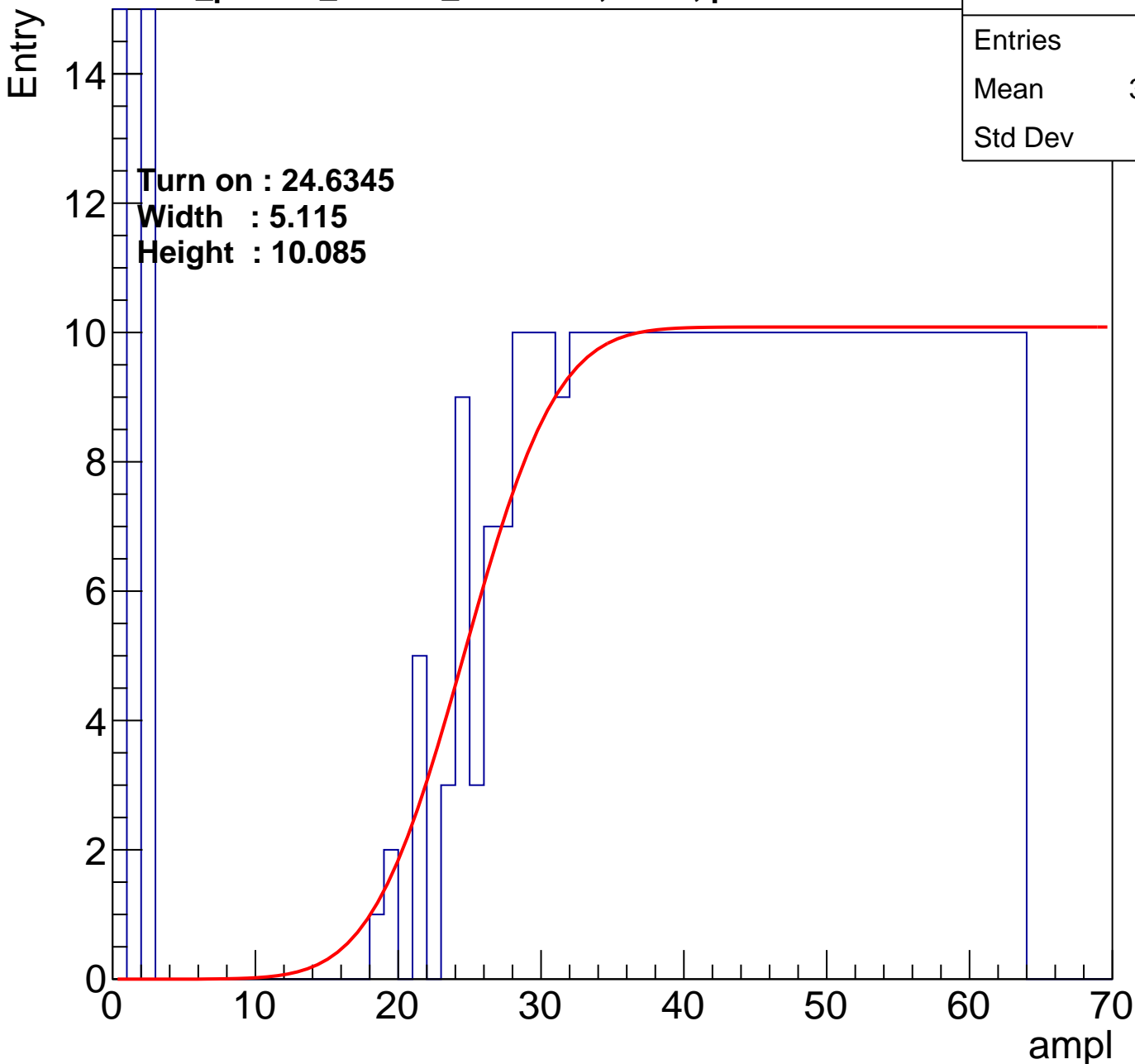
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	486
Mean	35.67
Std Dev	19.6

Turn on : 24.6345

Width : 5.115

Height : 10.085



# B1L103S, U26-ch83

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	425
Mean	39.69
Std Dev	17.26

Turn on : 26.2751

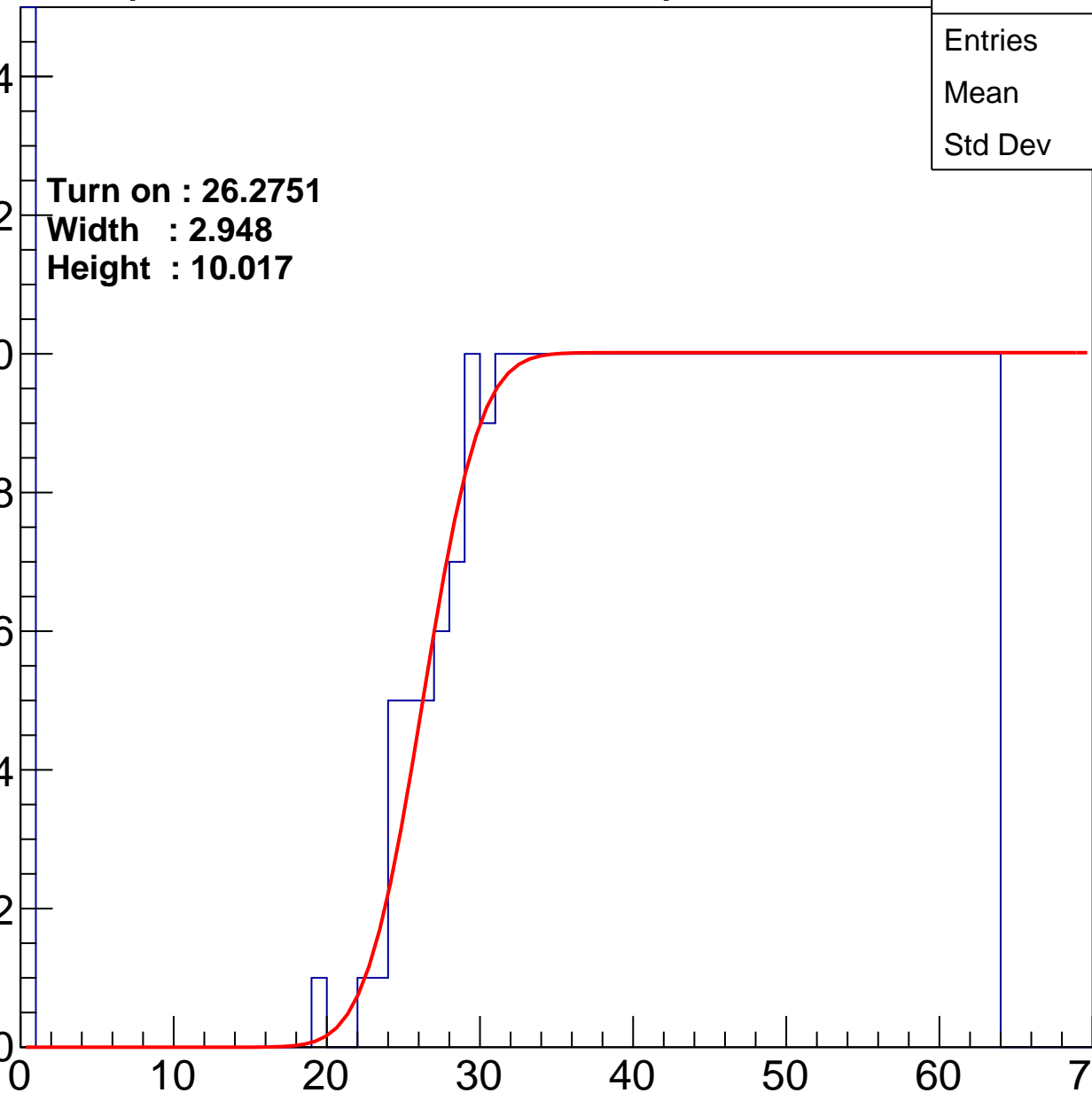
Width : 2.948

Height : 10.017

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch84

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	433
Mean	38.84
Std Dev	18.08

Turn on : 26.6320

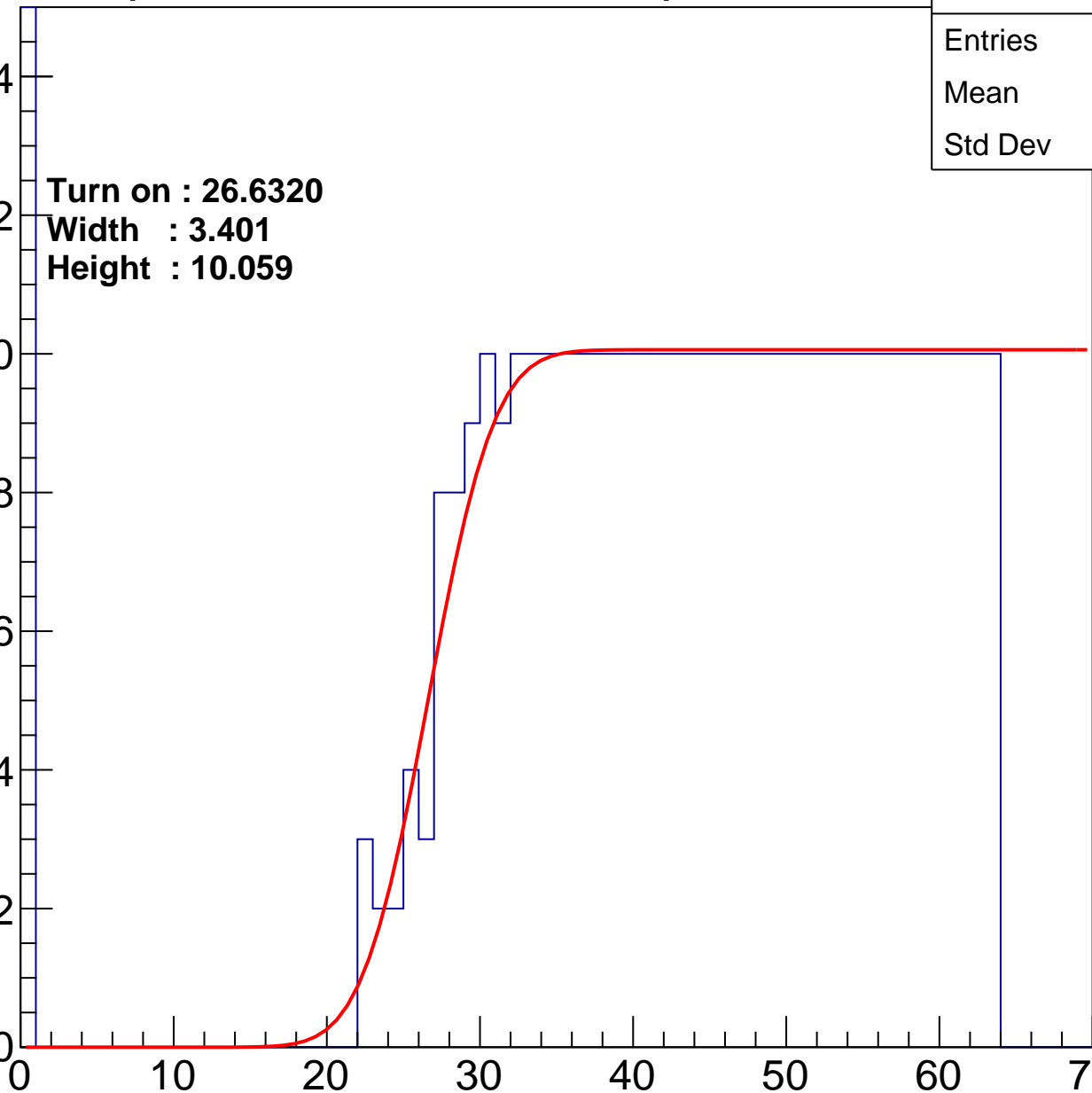
Width : 3.401

Height : 10.059

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch85

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	424
Mean	40.2
Std Dev	16.5

Turn on : 25.3328

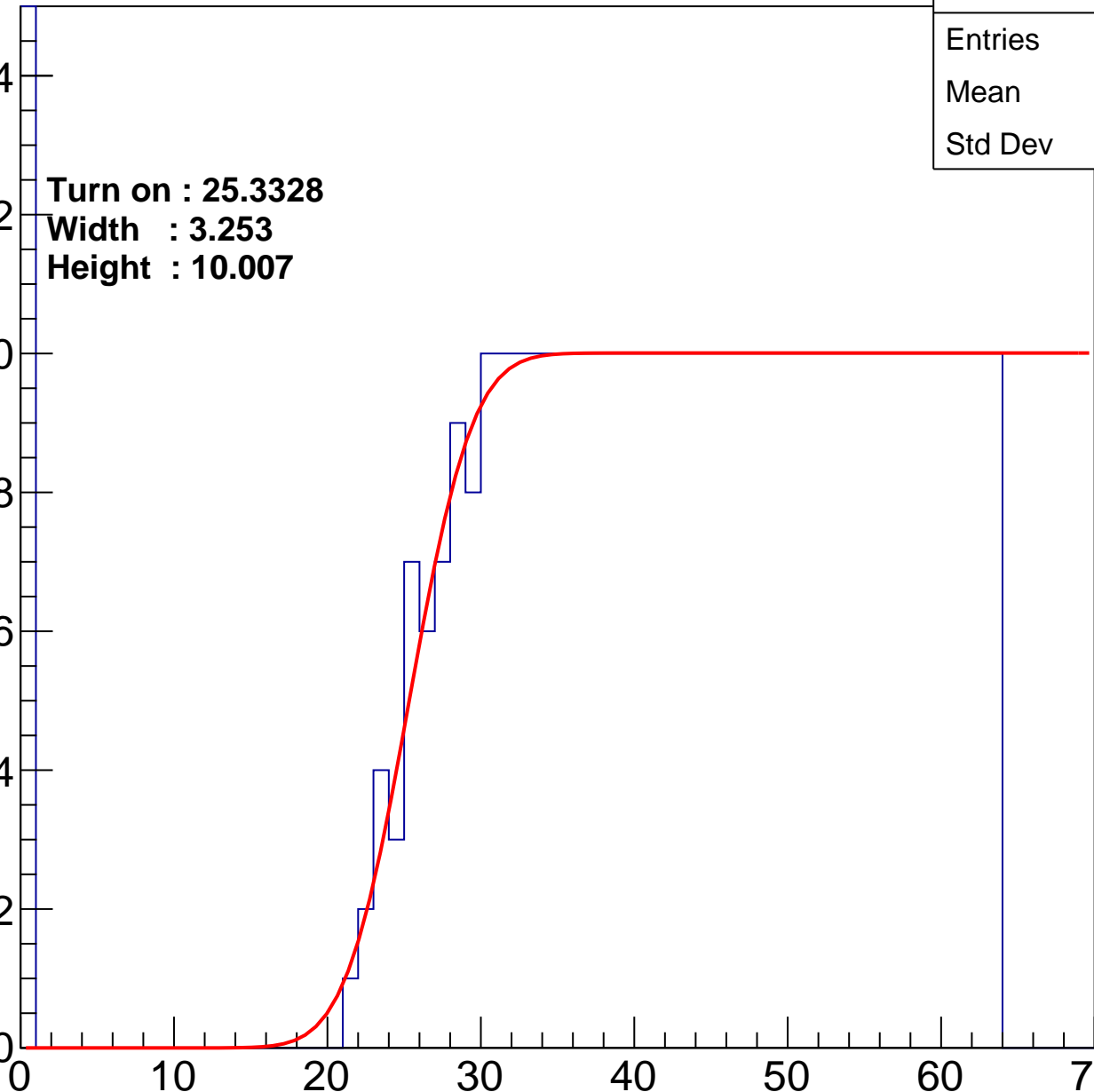
Width : 3.253

Height : 10.007

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch86

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	443
Mean	38.86
Std Dev	17.5

Turn on : 24.2595

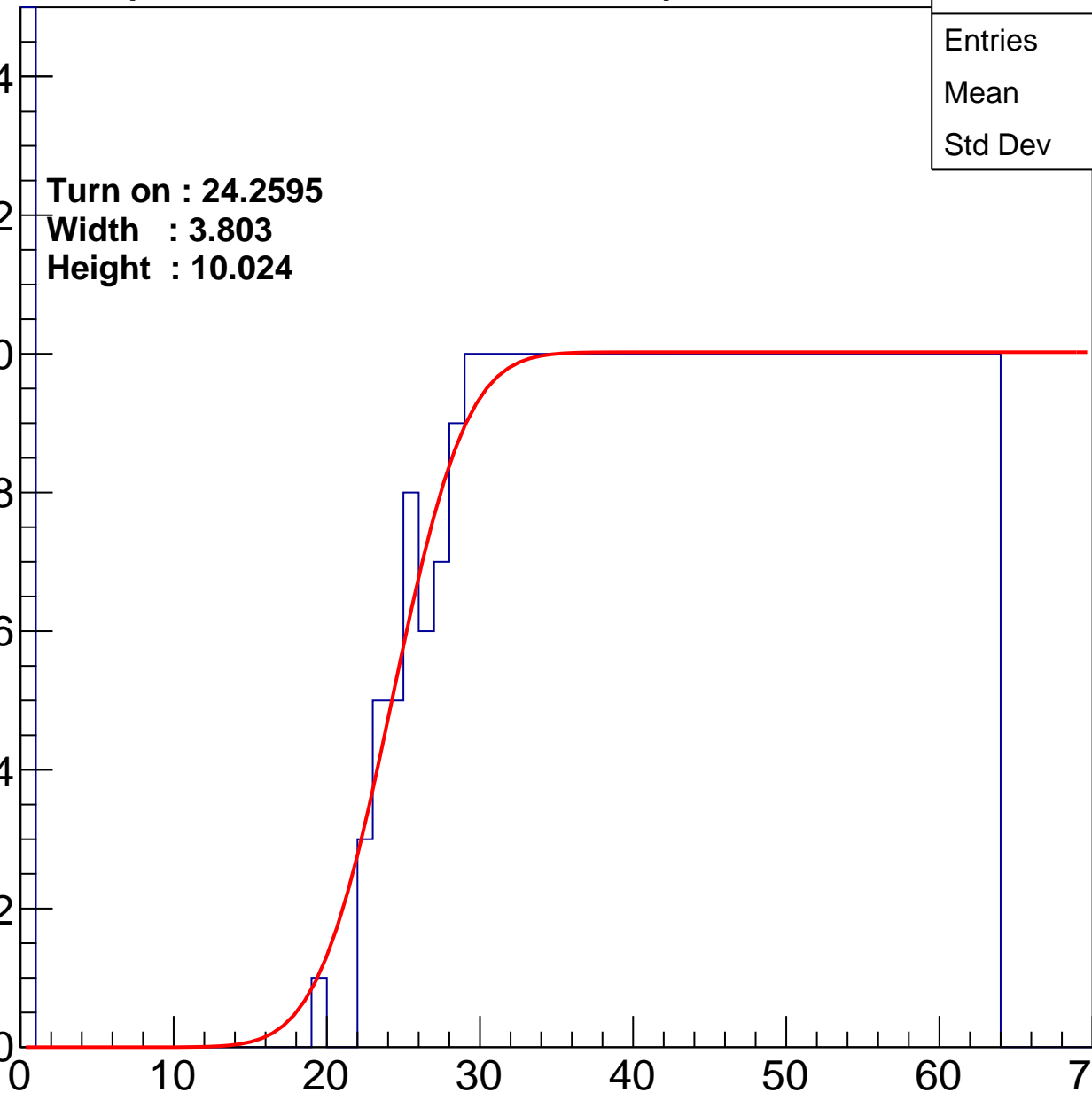
Width : 3.803

Height : 10.024

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U26-ch87

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	423
Mean	39.91
Std Dev	17

Turn on : 25.5913

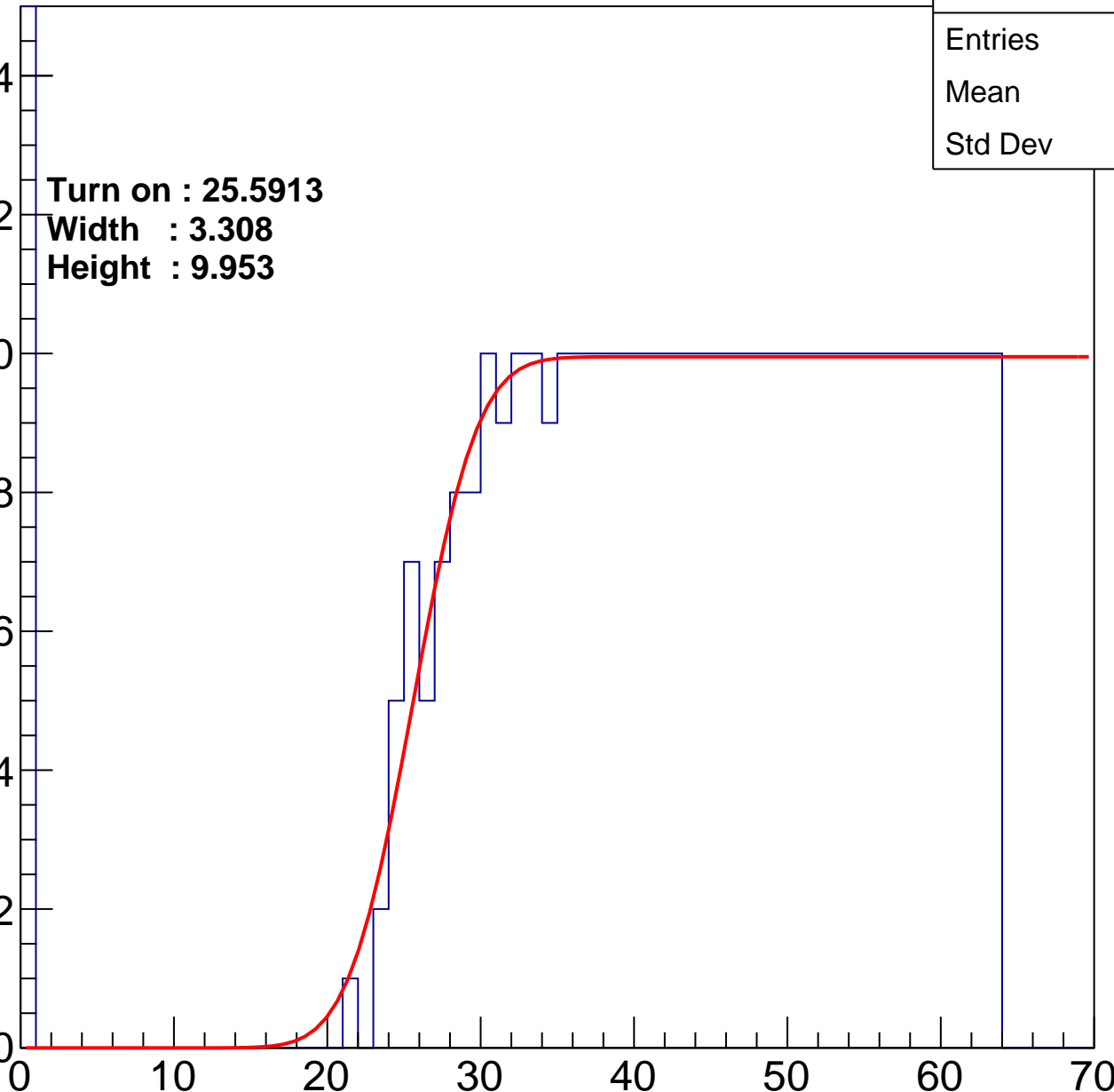
Width : 3.308

Height : 9.953

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch88

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	469
Mean	37.35
Std Dev	18.33

Turn on : 23.6387

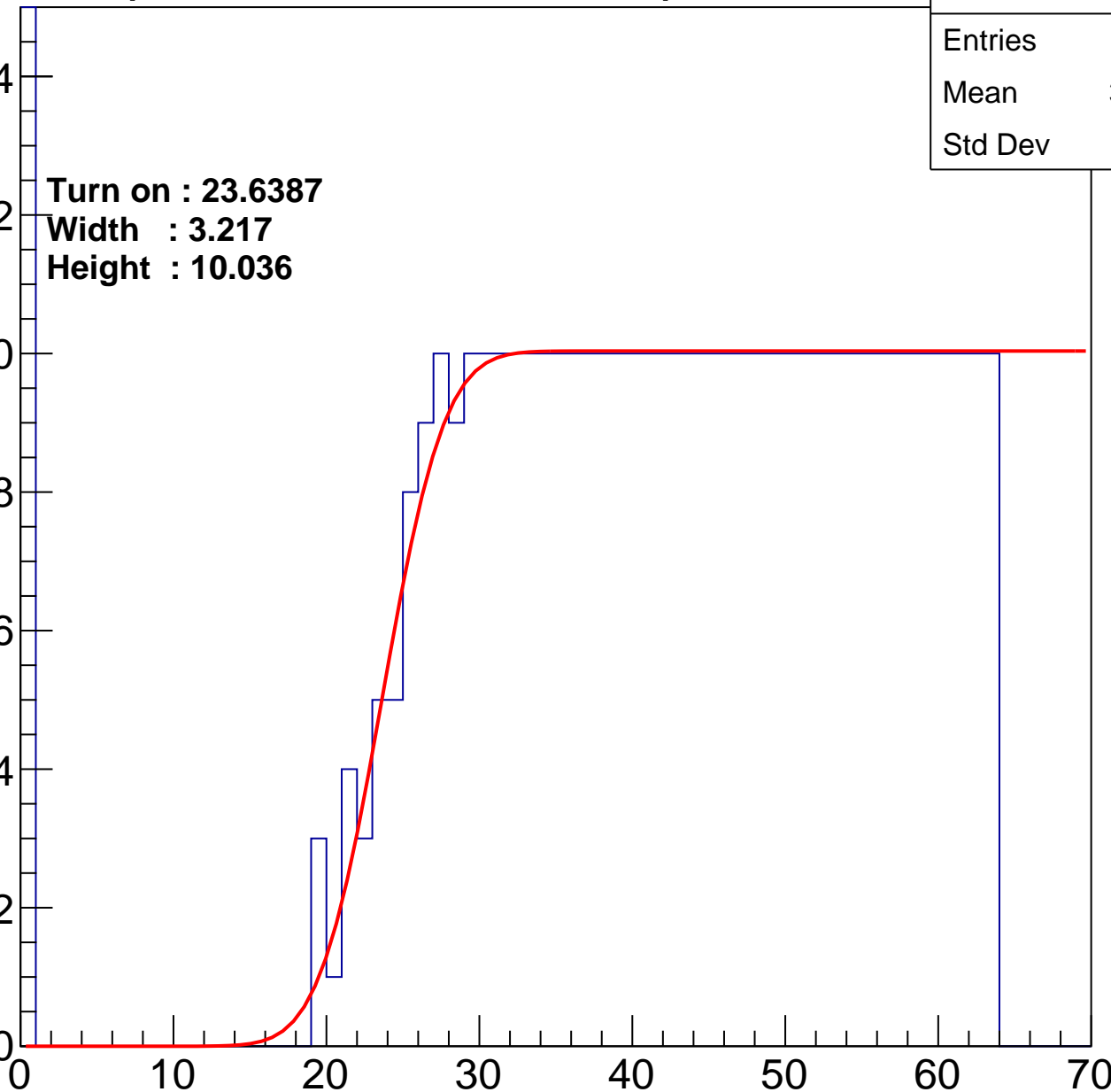
Width : 3.217

Height : 10.036

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch89

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	428
Mean	39.94
Std Dev	16.68

Turn on : 24.9674

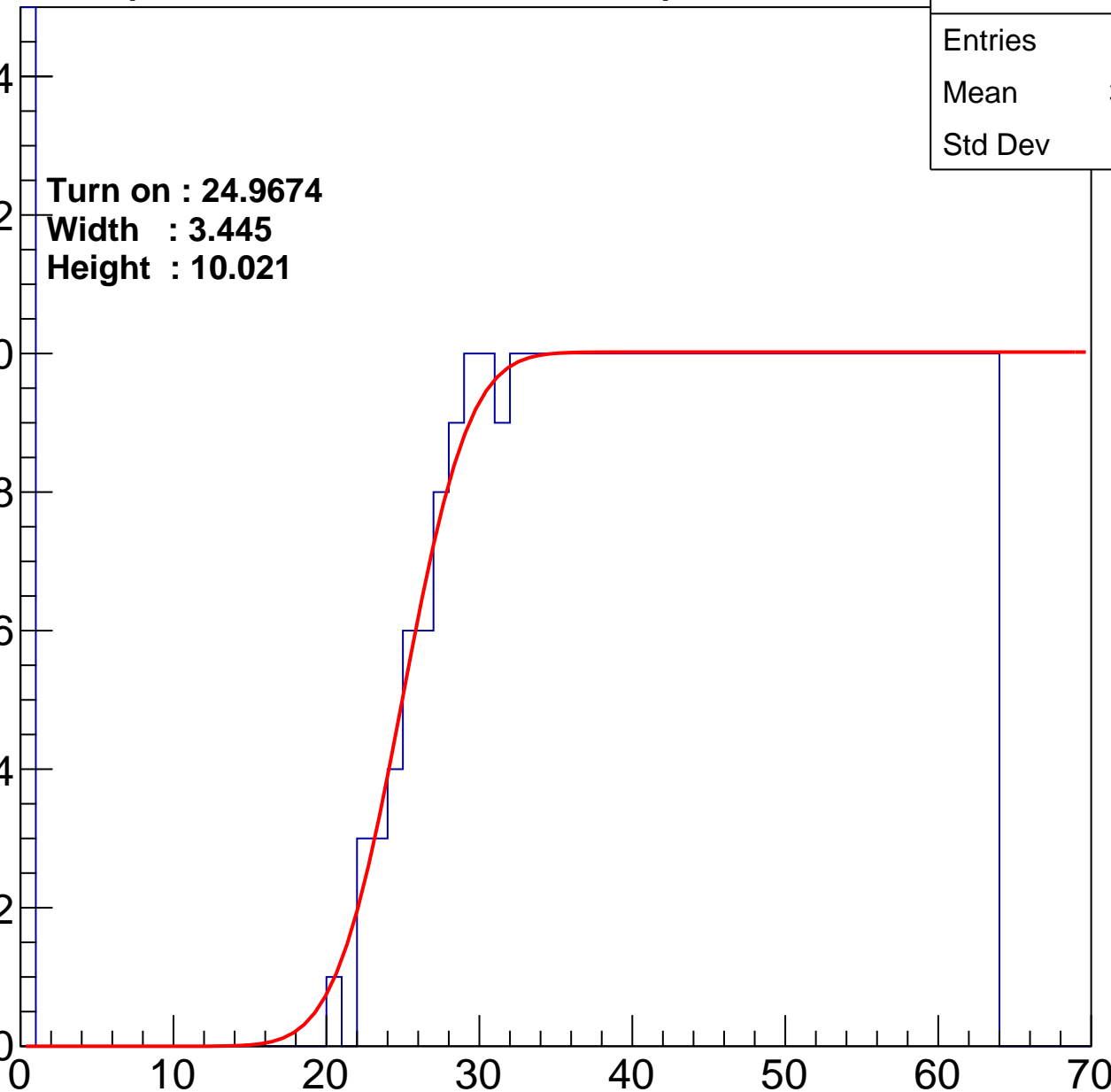
Width : 3.445

Height : 10.021

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch90

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	475
Mean	36.41
Std Dev	19.29

Turn on : 24.8762

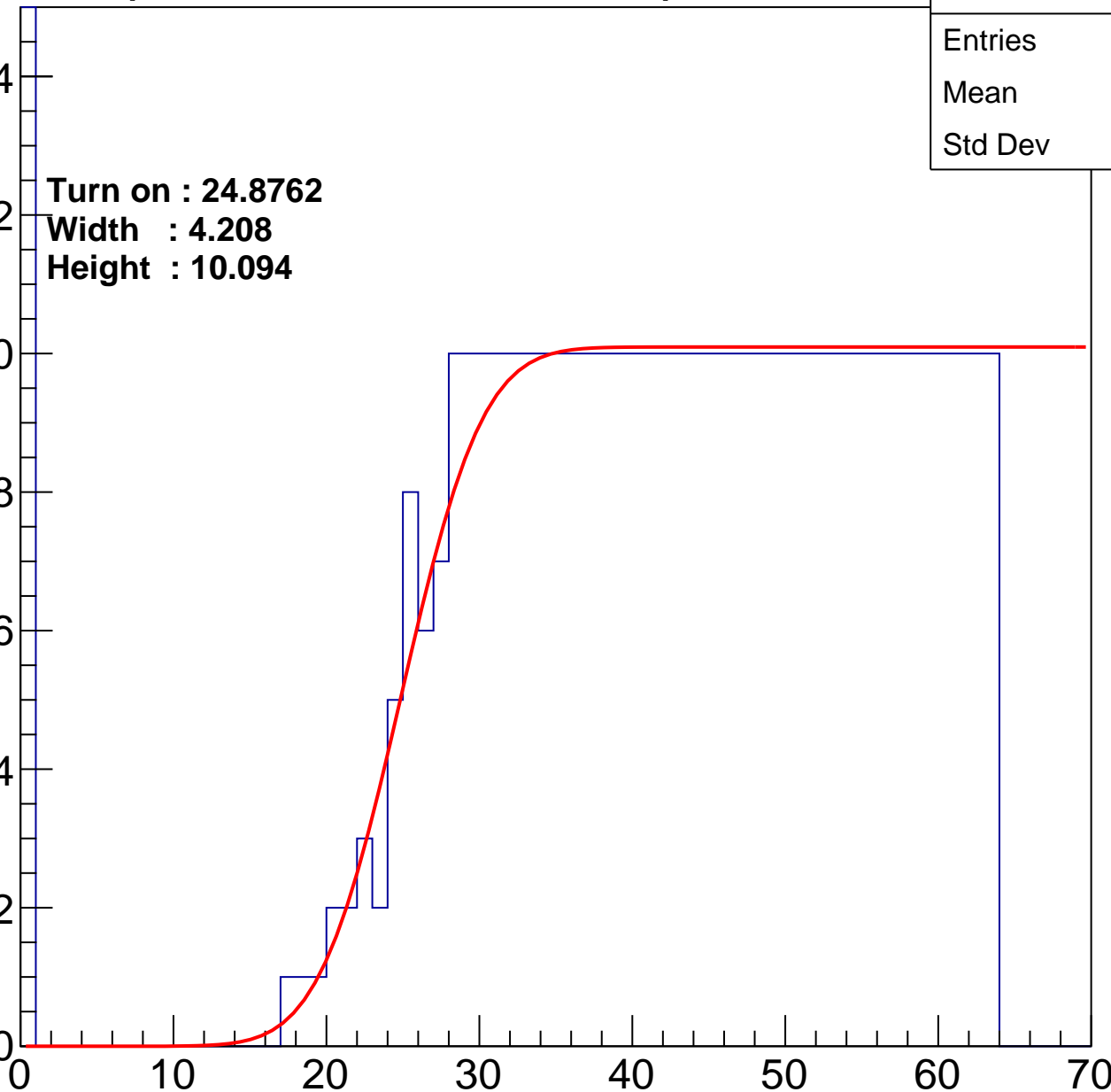
Width : 4.208

Height : 10.094

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch91

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	431
Mean	39.54
Std Dev	17.14

Turn on : 26.0161

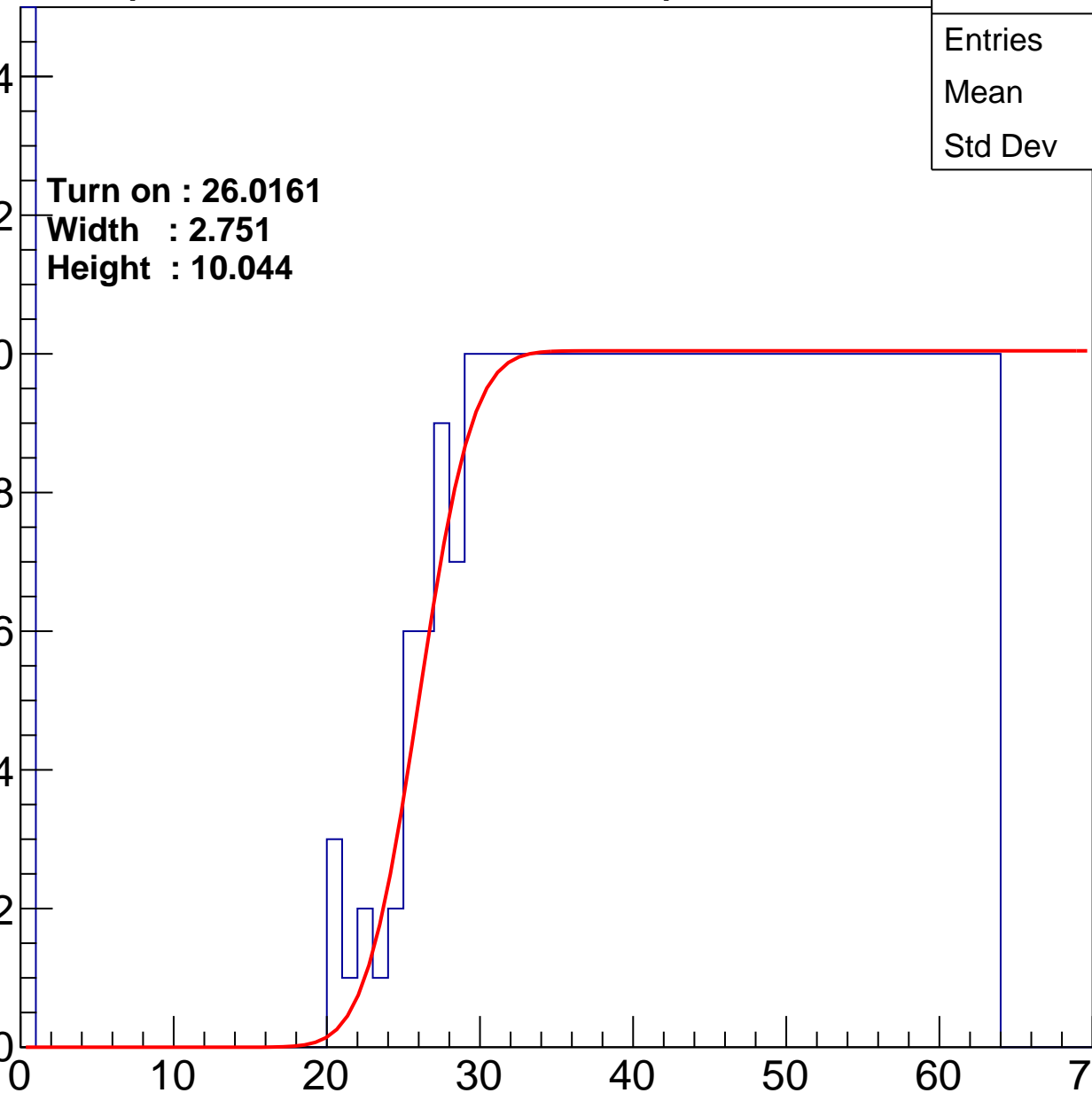
Width : 2.751

Height : 10.044

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch92

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	447
Mean	38.75
Std Dev	17.43

Turn on : 24.6792

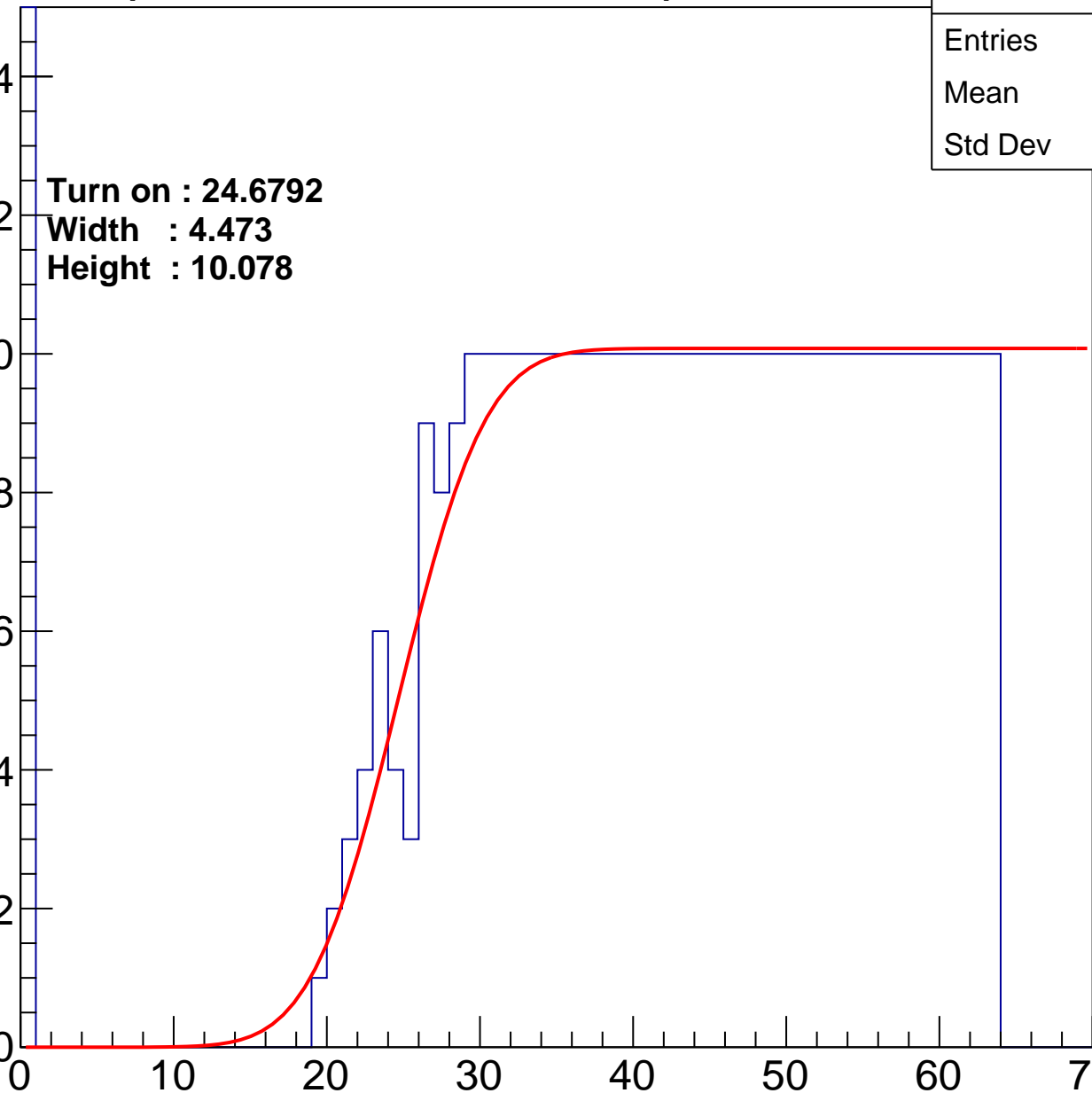
Width : 4.473

Height : 10.078

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch93

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	420
Mean	40.56
Std Dev	16.11

Turn on : 25.3957

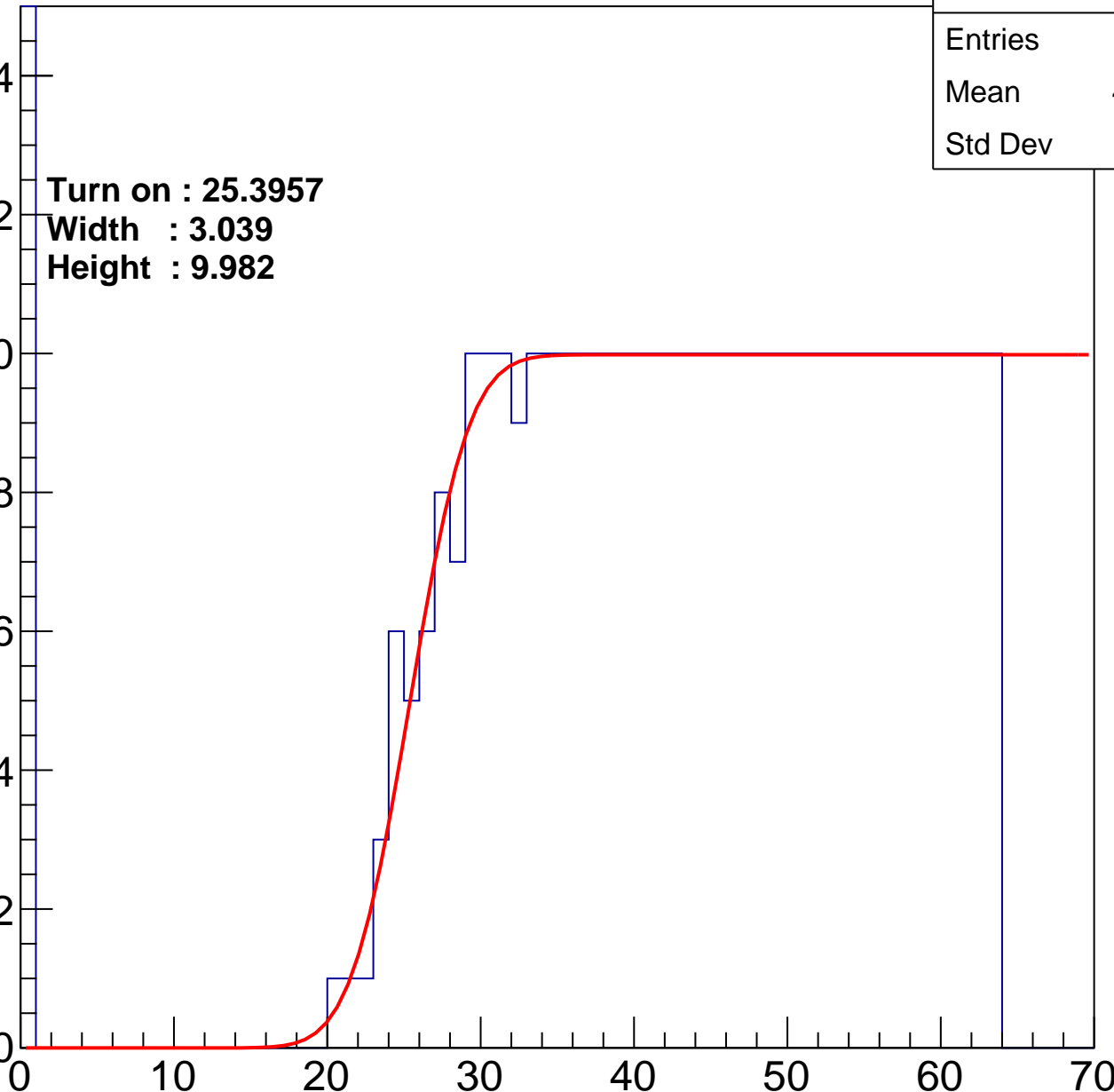
Width : 3.039

Height : 9.982

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch94

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	432
Mean	39.11
Std Dev	17.75

Turn on : 26.4387

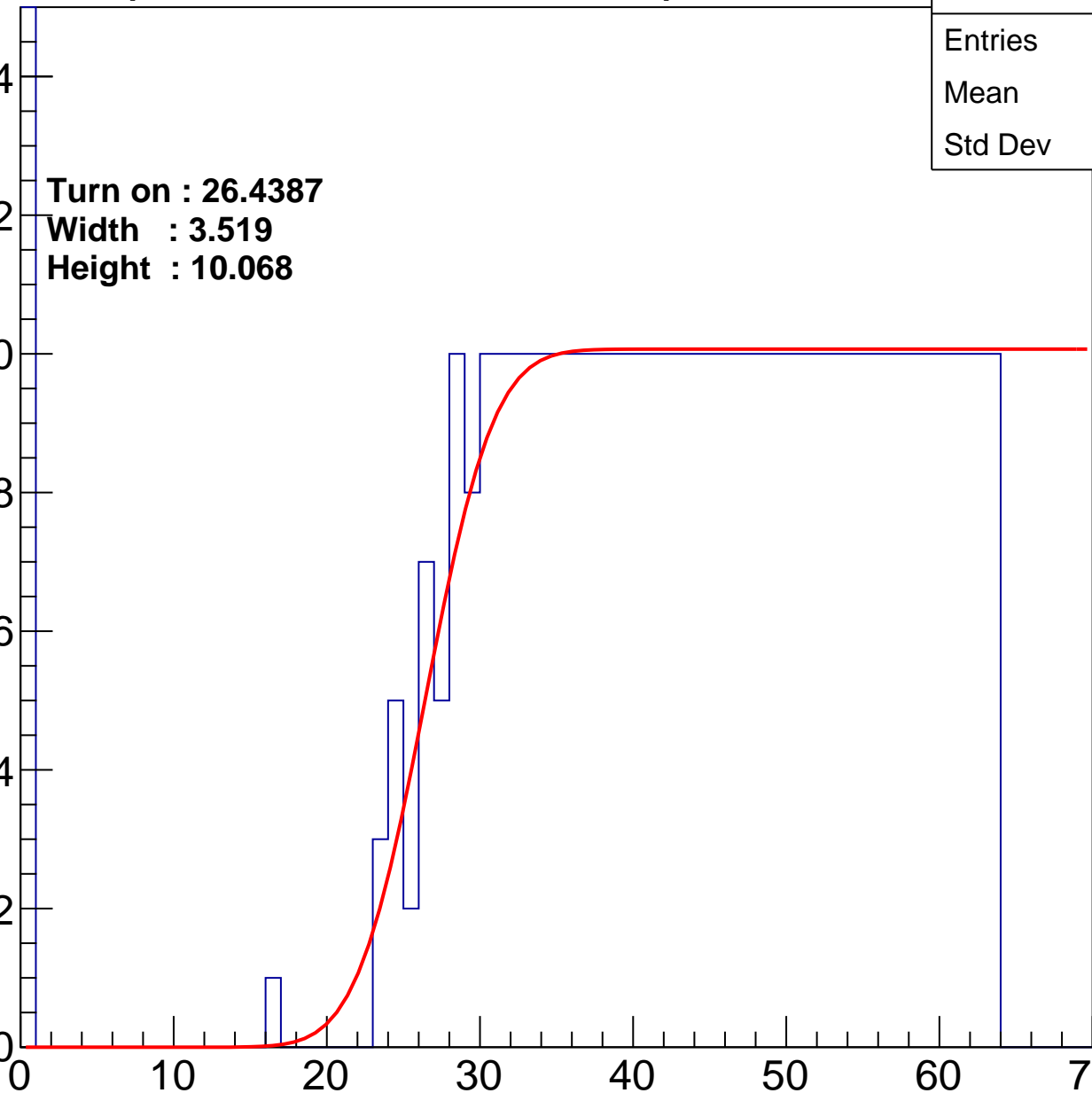
Width : 3.519

Height : 10.068

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U26-ch95

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	416
Mean	40.47
Std Dev	16.54

**Turn on : 26.7472**

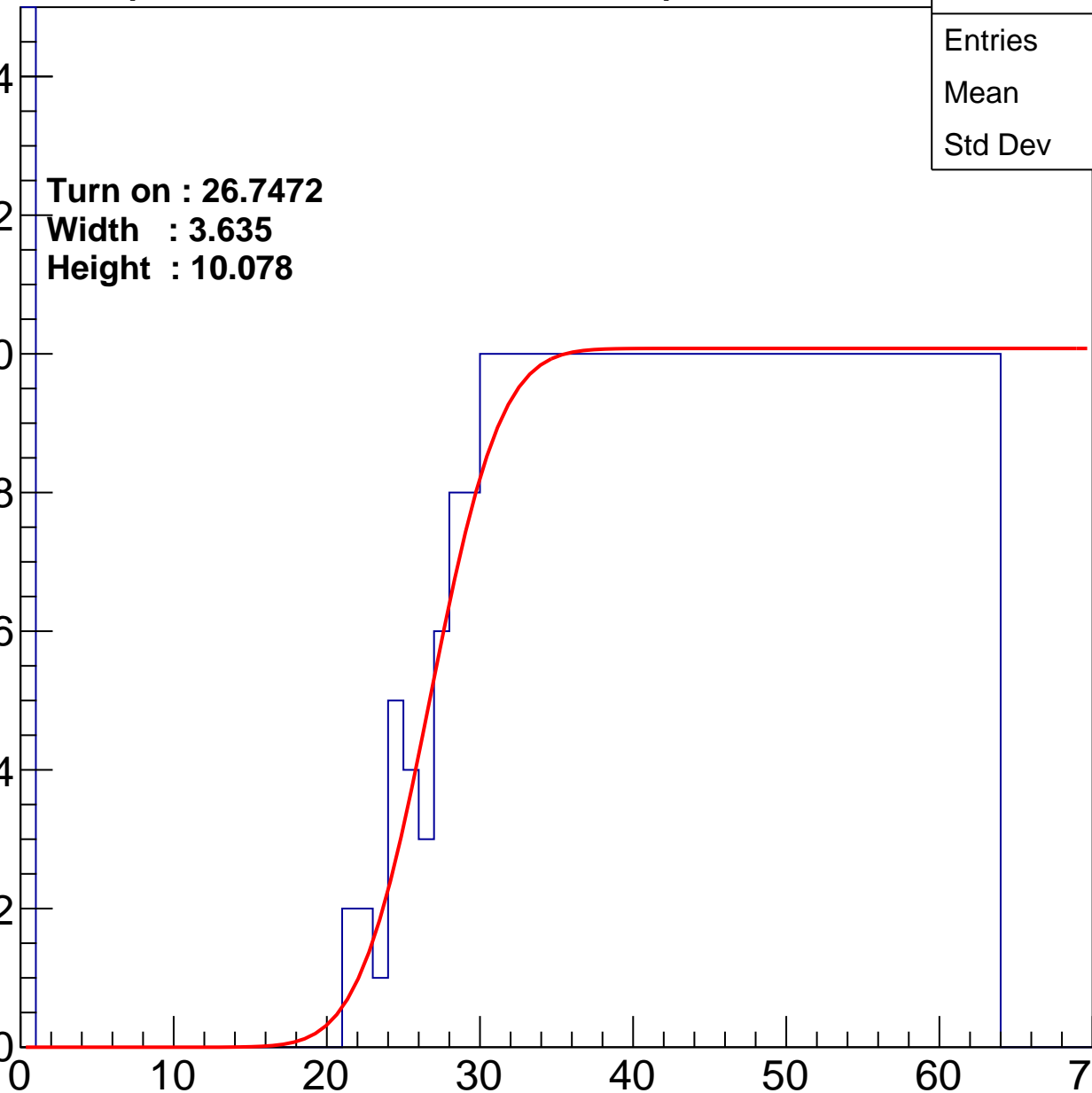
**Width : 3.635**

**Height : 10.078**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch96

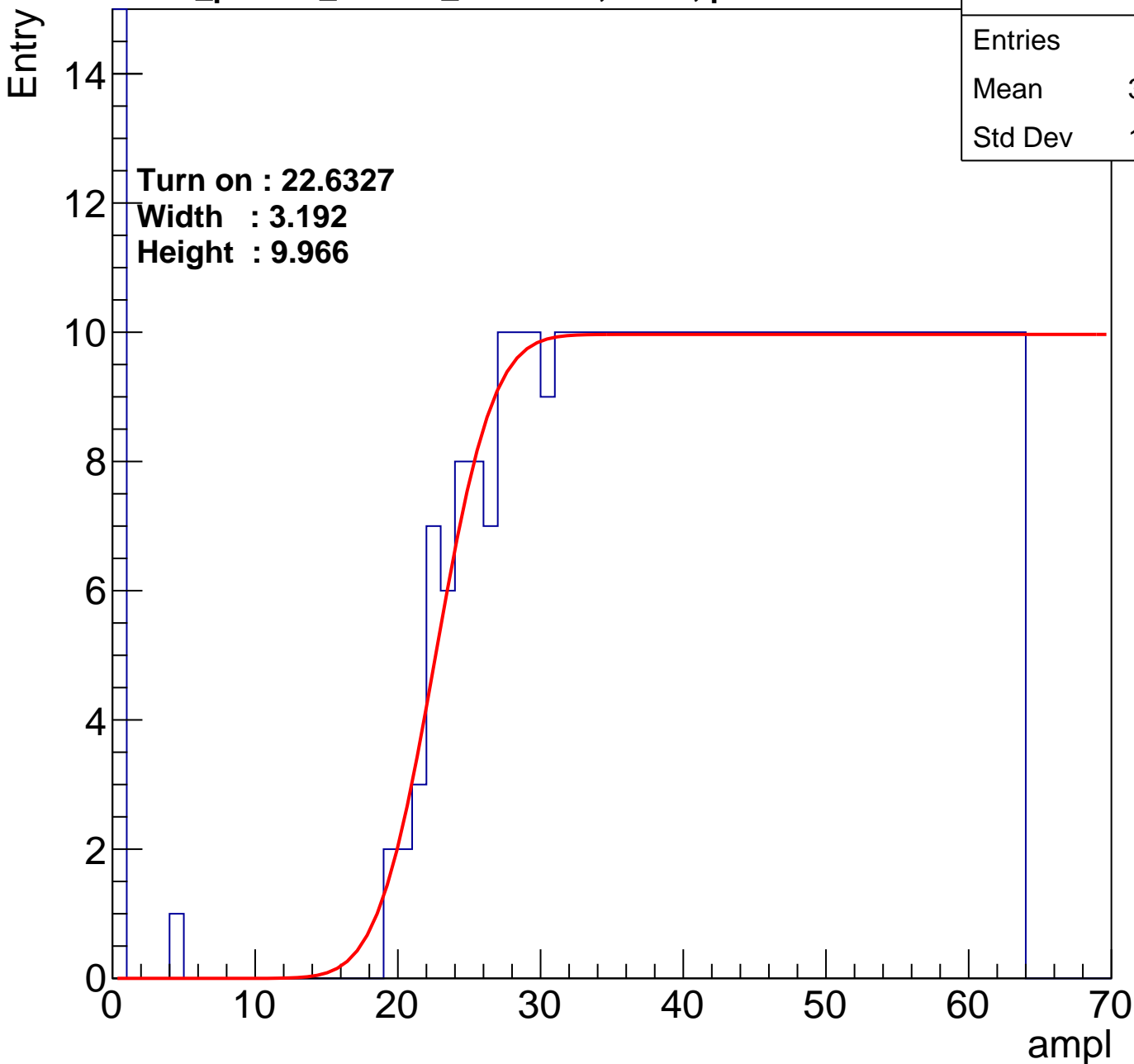
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	449
Mean	39.27
Std Dev	16.48

Turn on : 22.6327

Width : 3.192

Height : 9.966



# B1L103S, U26-ch97

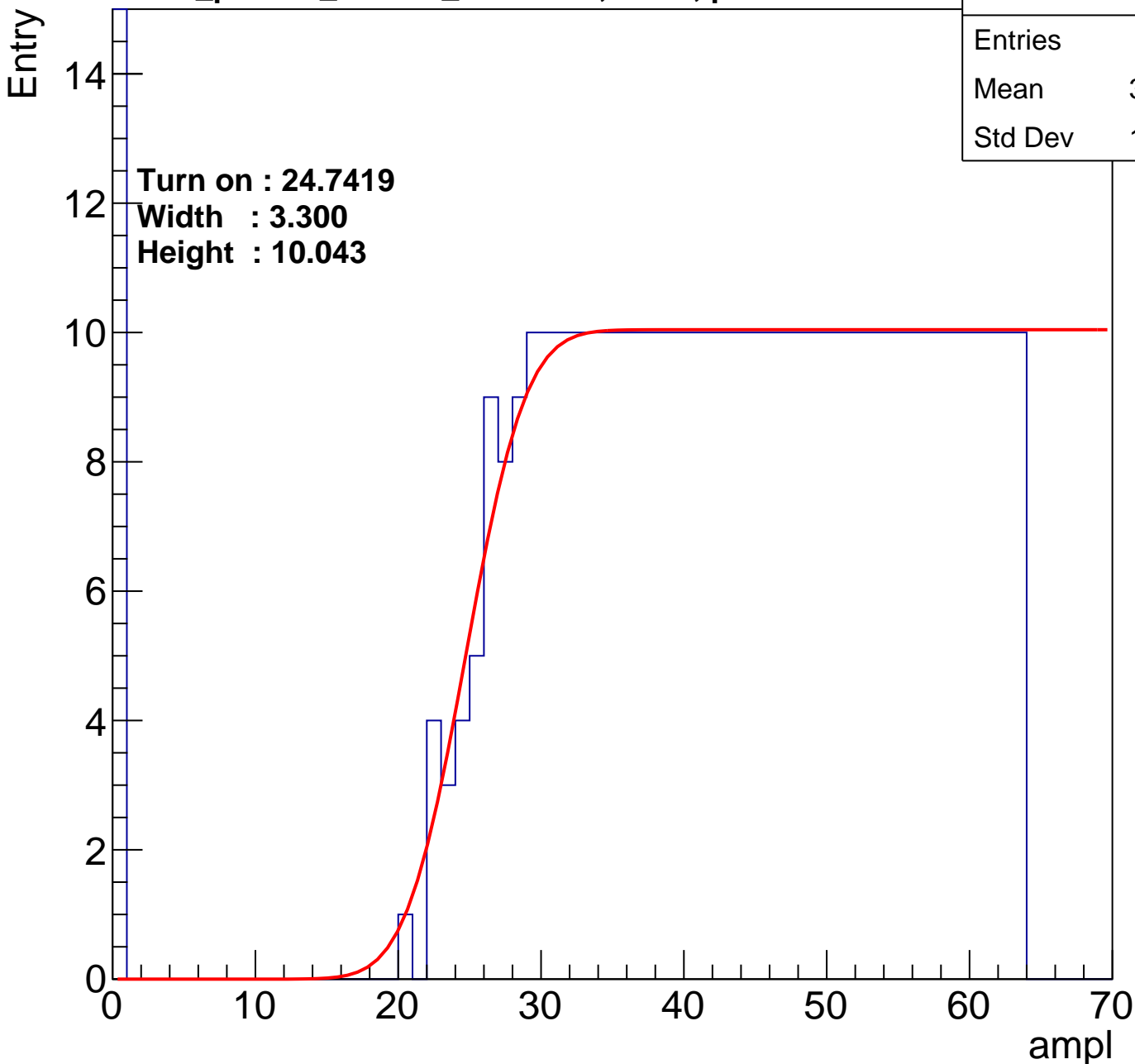
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	439
Mean	39.18
Std Dev	17.26

Turn on : 24.7419

Width : 3.300

Height : 10.043



# B1L103S, U26-ch98

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	483
Mean	37.95
Std Dev	16.84

Turn on : 22.8248

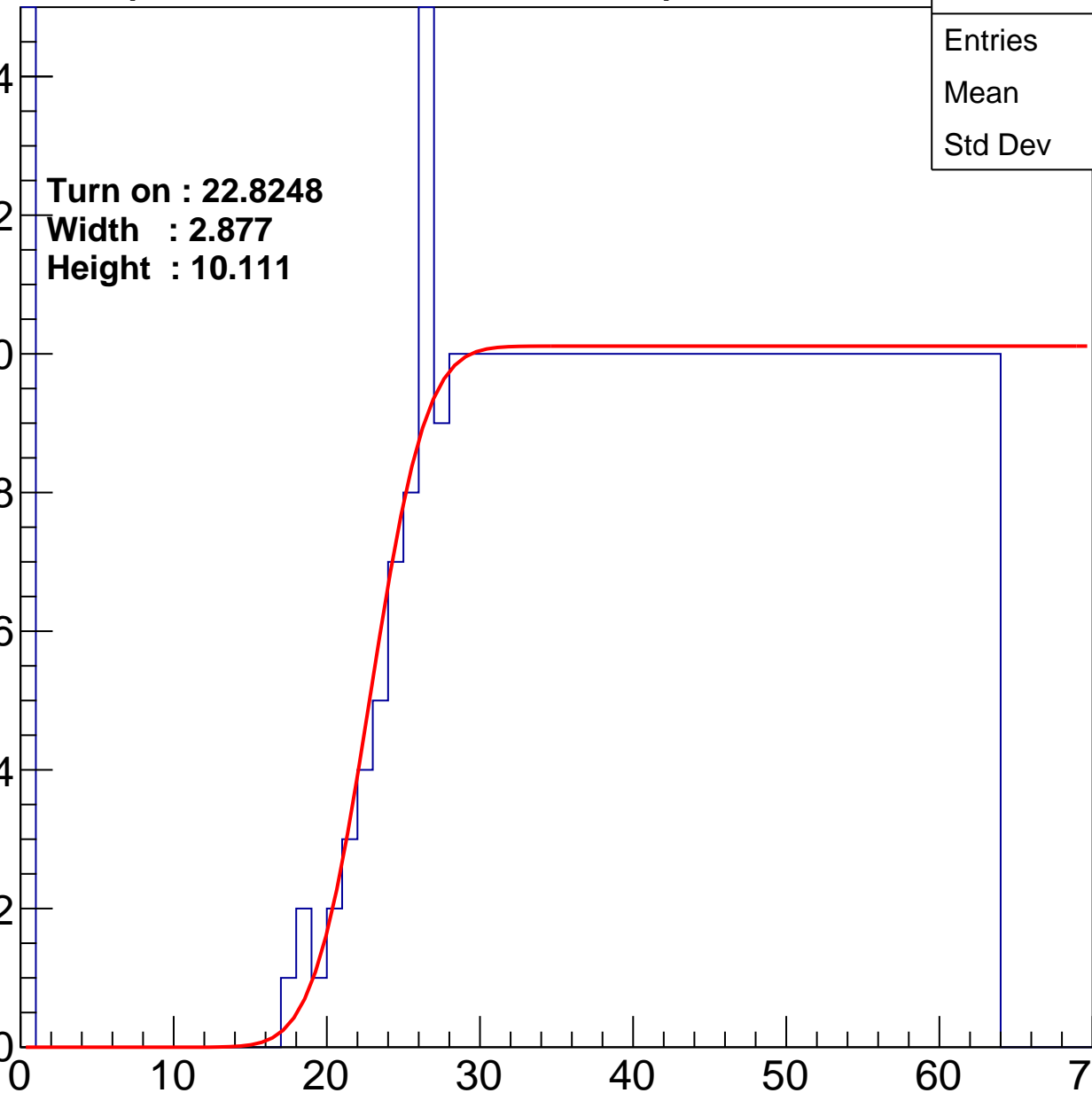
Width : 2.877

Height : 10.111

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch99

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	417
Mean	39.41
Std Dev	18.09

Turn on : 27.9567

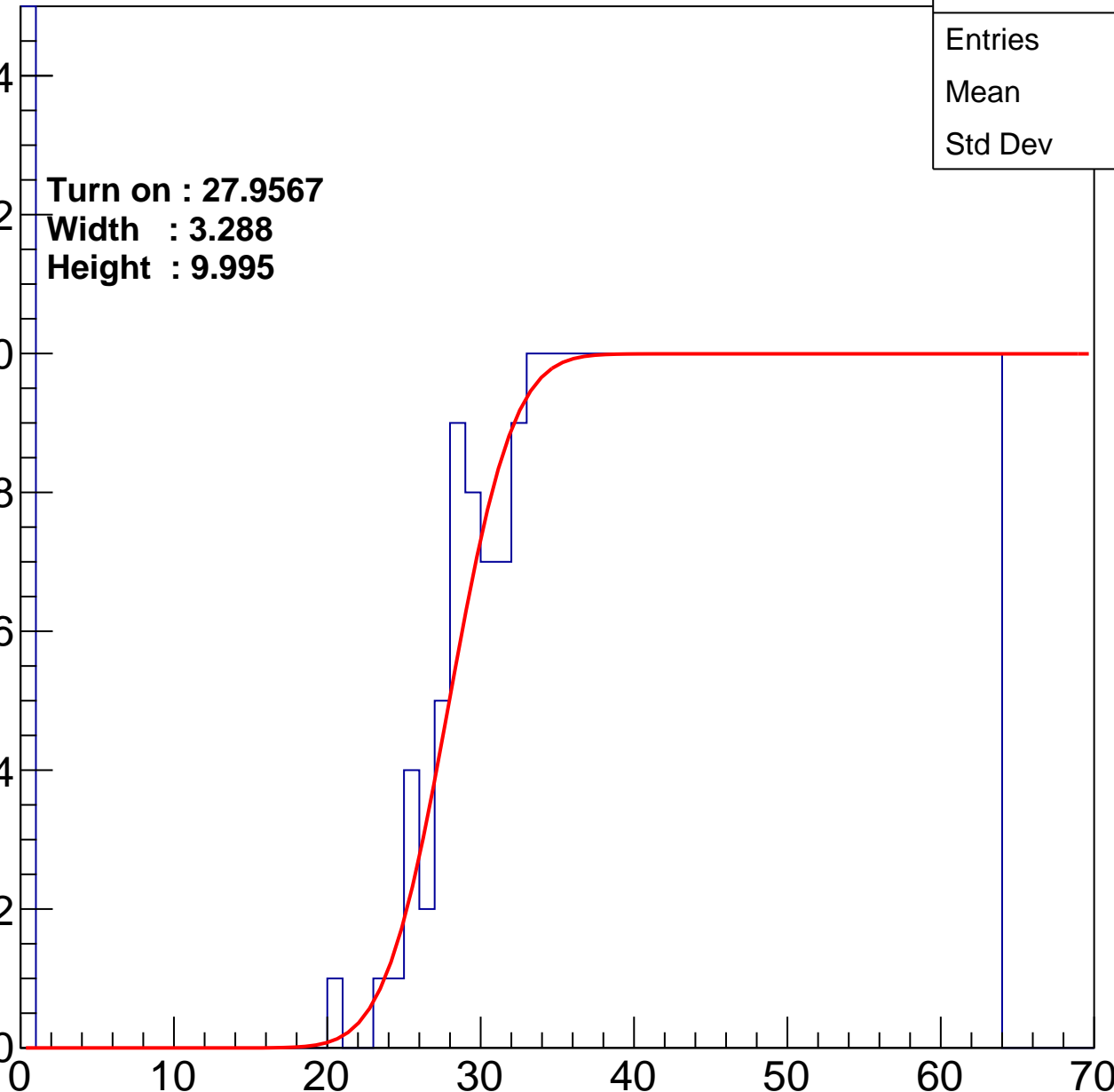
Width : 3.288

Height : 9.995

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch100

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	444
Mean	39.22
Std Dev	16.86

**Turn on : 23.9941**

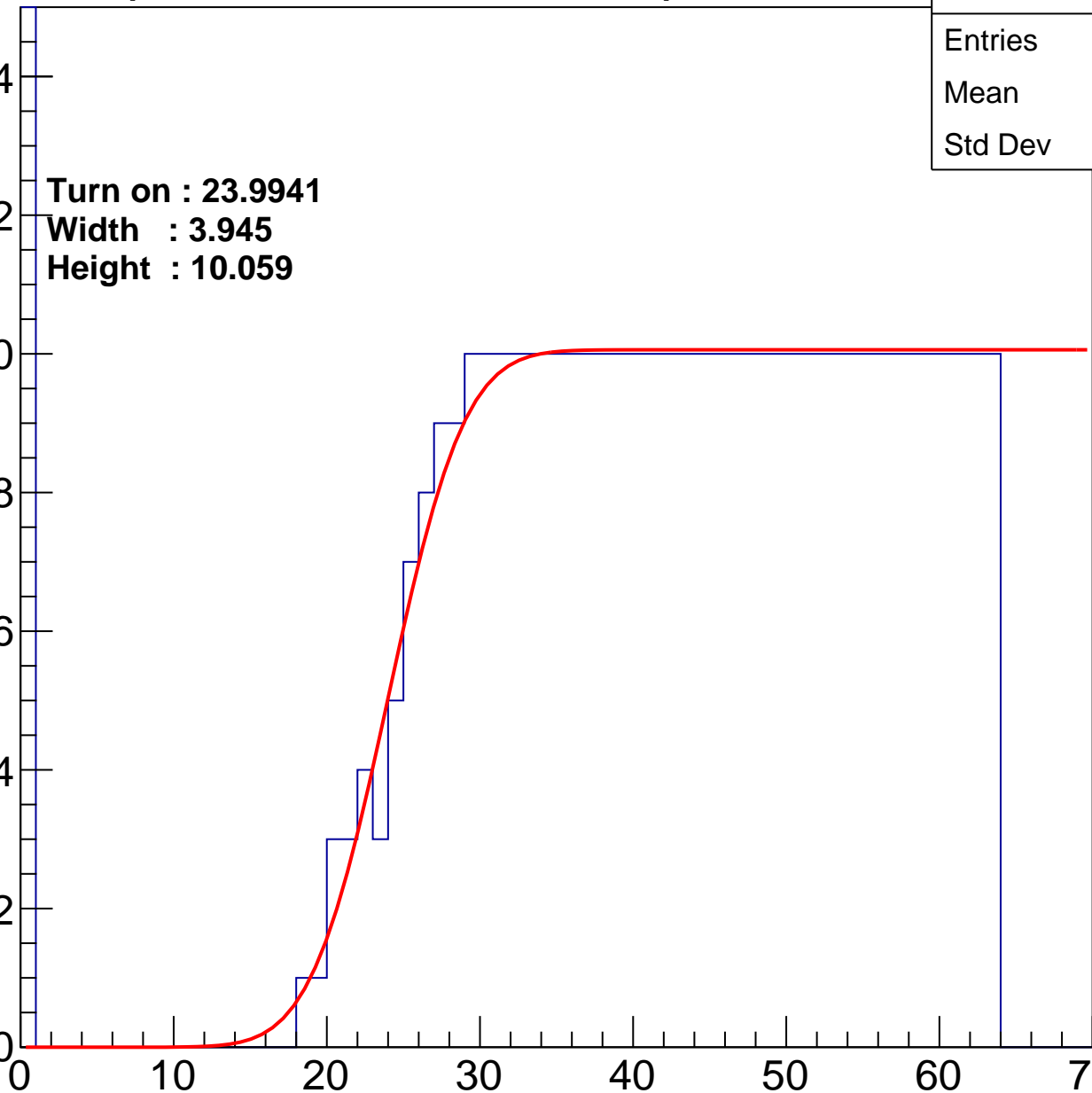
**Width : 3.945**

**Height : 10.059**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch101

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	418
Mean	40.11
Std Dev	16.96

**Turn on : 25.8834**

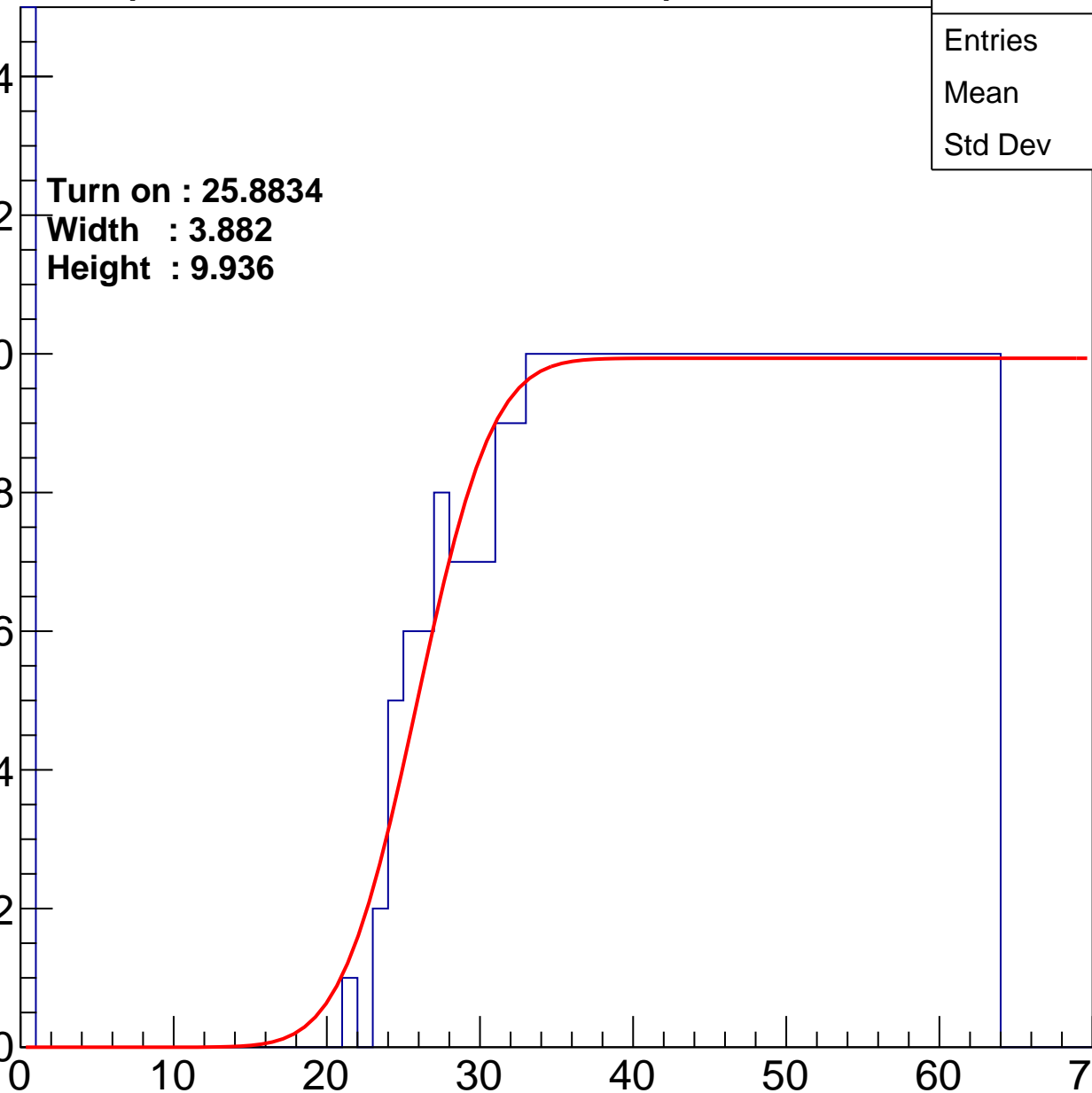
**Width : 3.882**

**Height : 9.936**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch102

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	430
Mean	39.1
Std Dev	17.86

**Turn on : 26.6765**

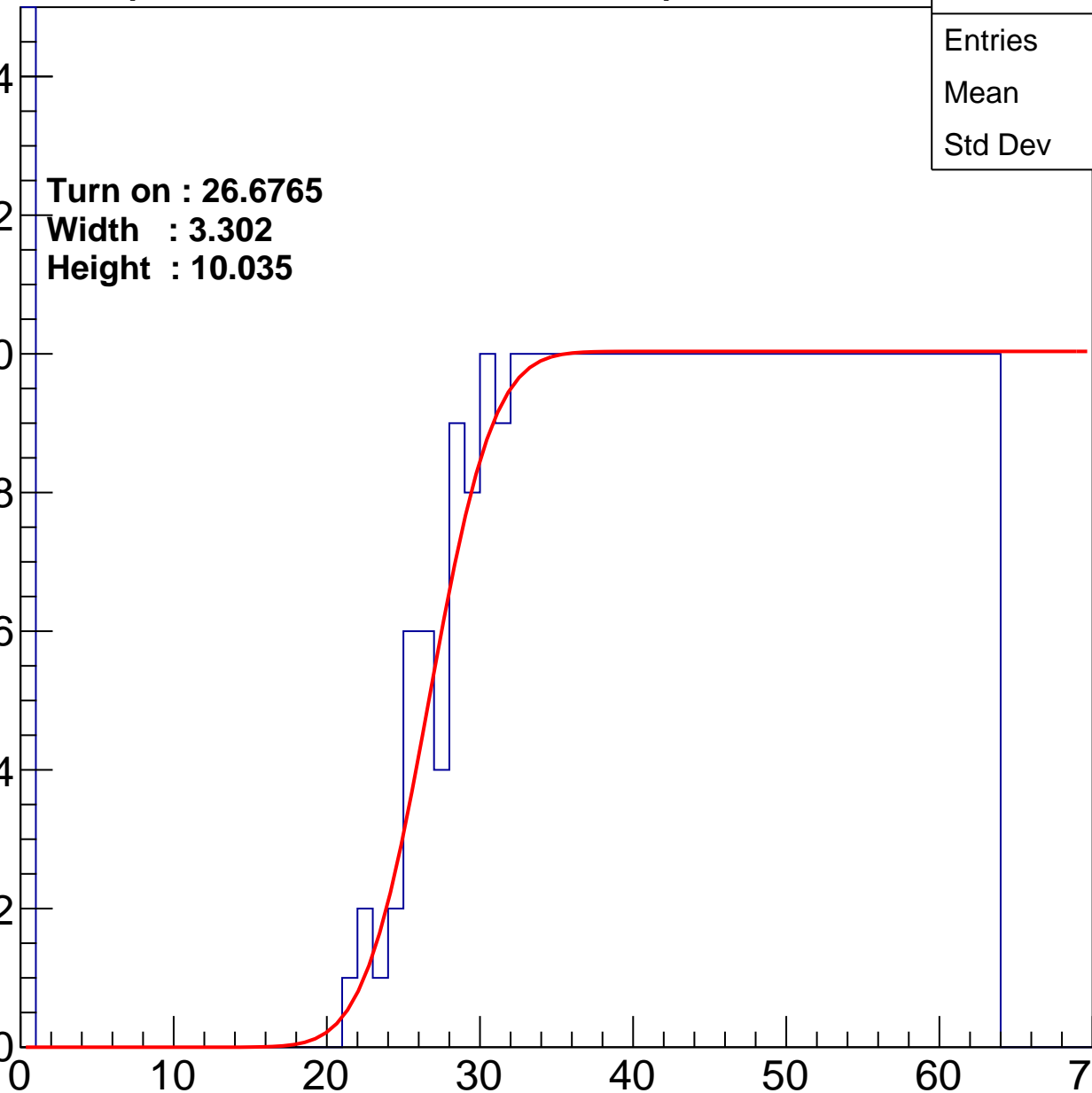
**Width : 3.302**

**Height : 10.035**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U26-ch103

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	427
Mean	39.81
Std Dev	16.96

Turn on : 25.6483

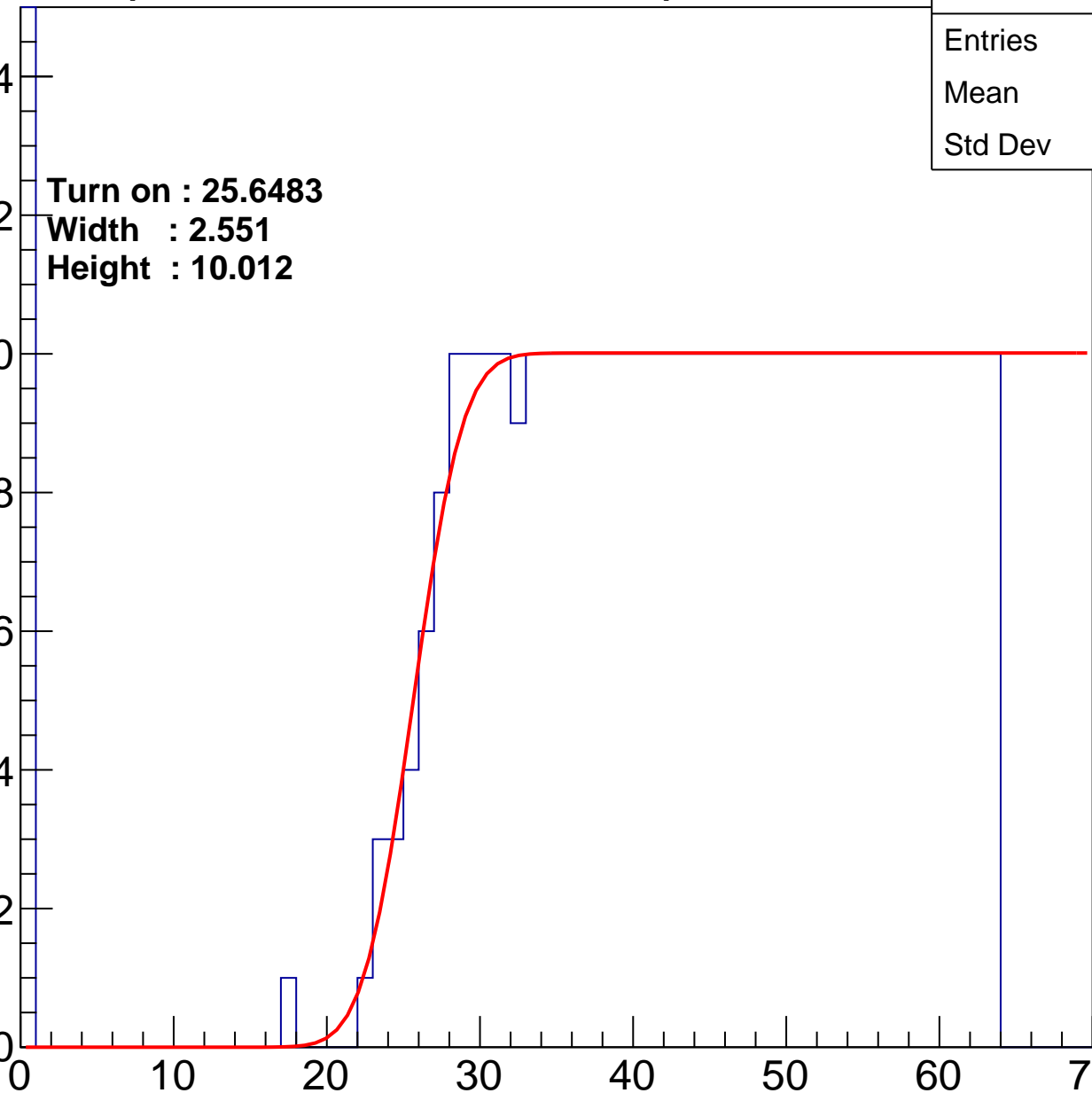
Width : 2.551

Height : 10.012

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch104

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	430
Mean	39.71
Std Dev	16.94

Turn on : 25.1590

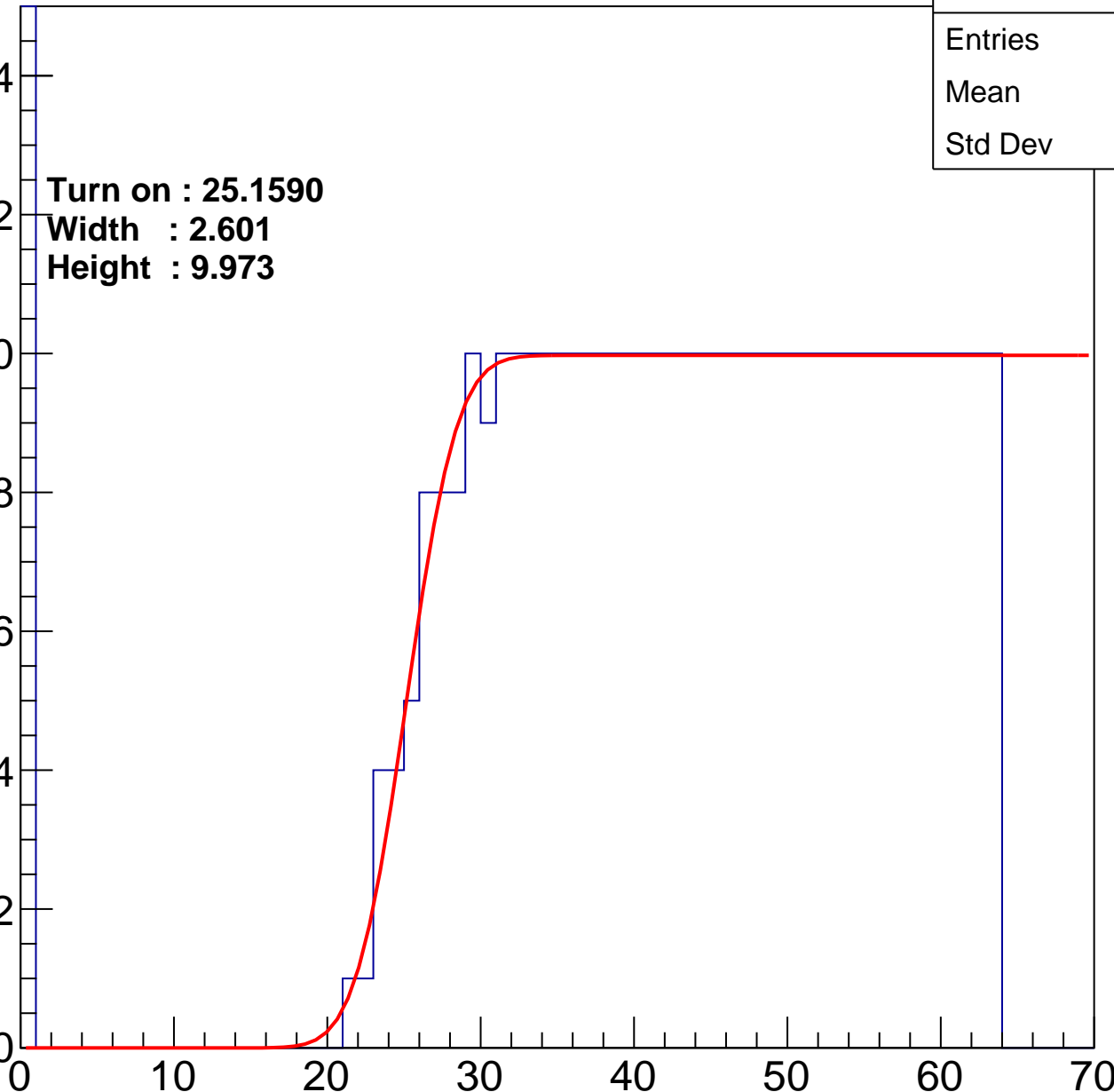
Width : 2.601

Height : 9.973

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch105

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	435
Mean	39.2
Std Dev	17.44

Turn on : 25.0646

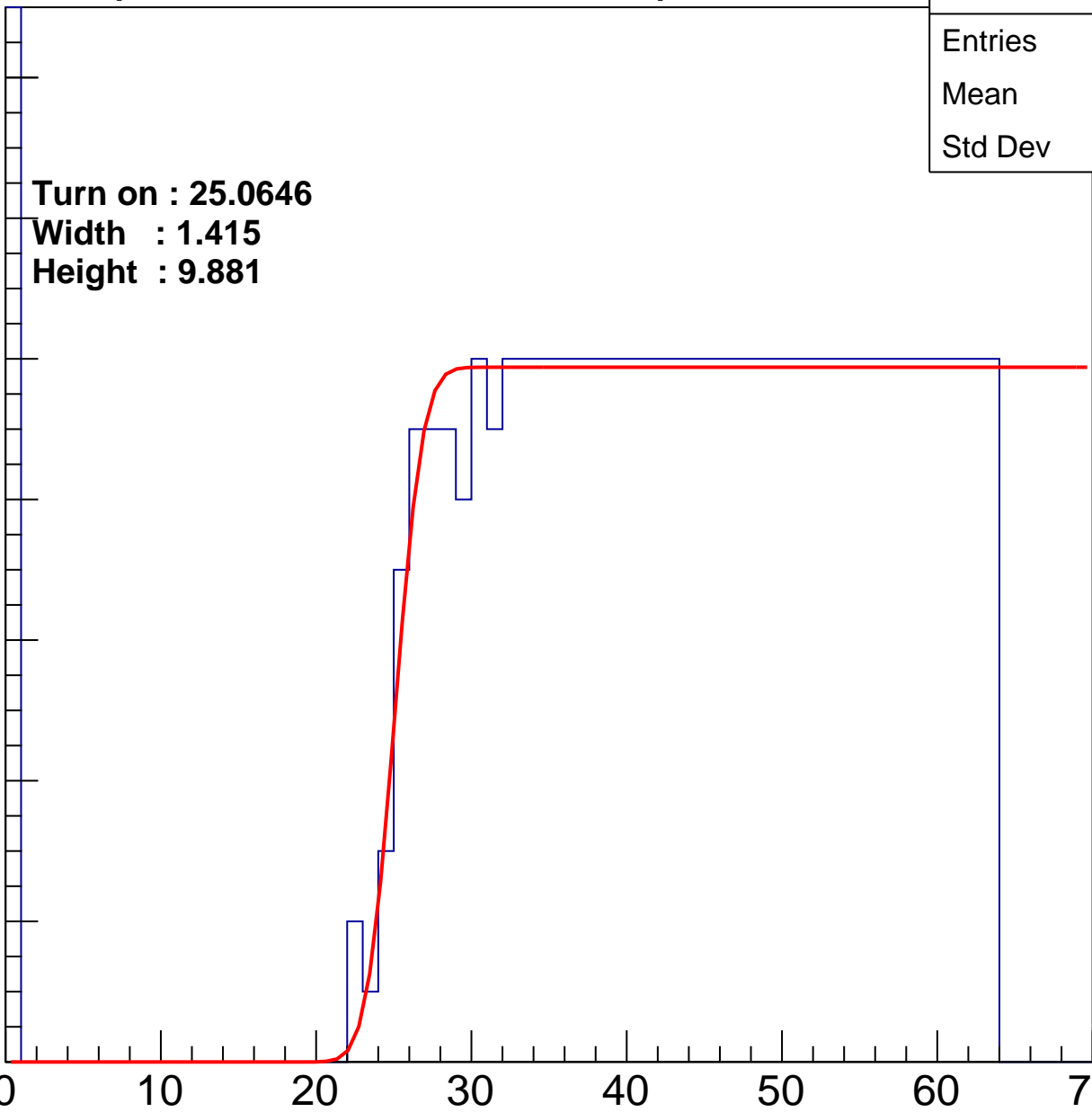
Width : 1.415

Height : 9.881

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch106

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	457
Mean	38.13
Std Dev	17.83

**Turn on : 23.8930**

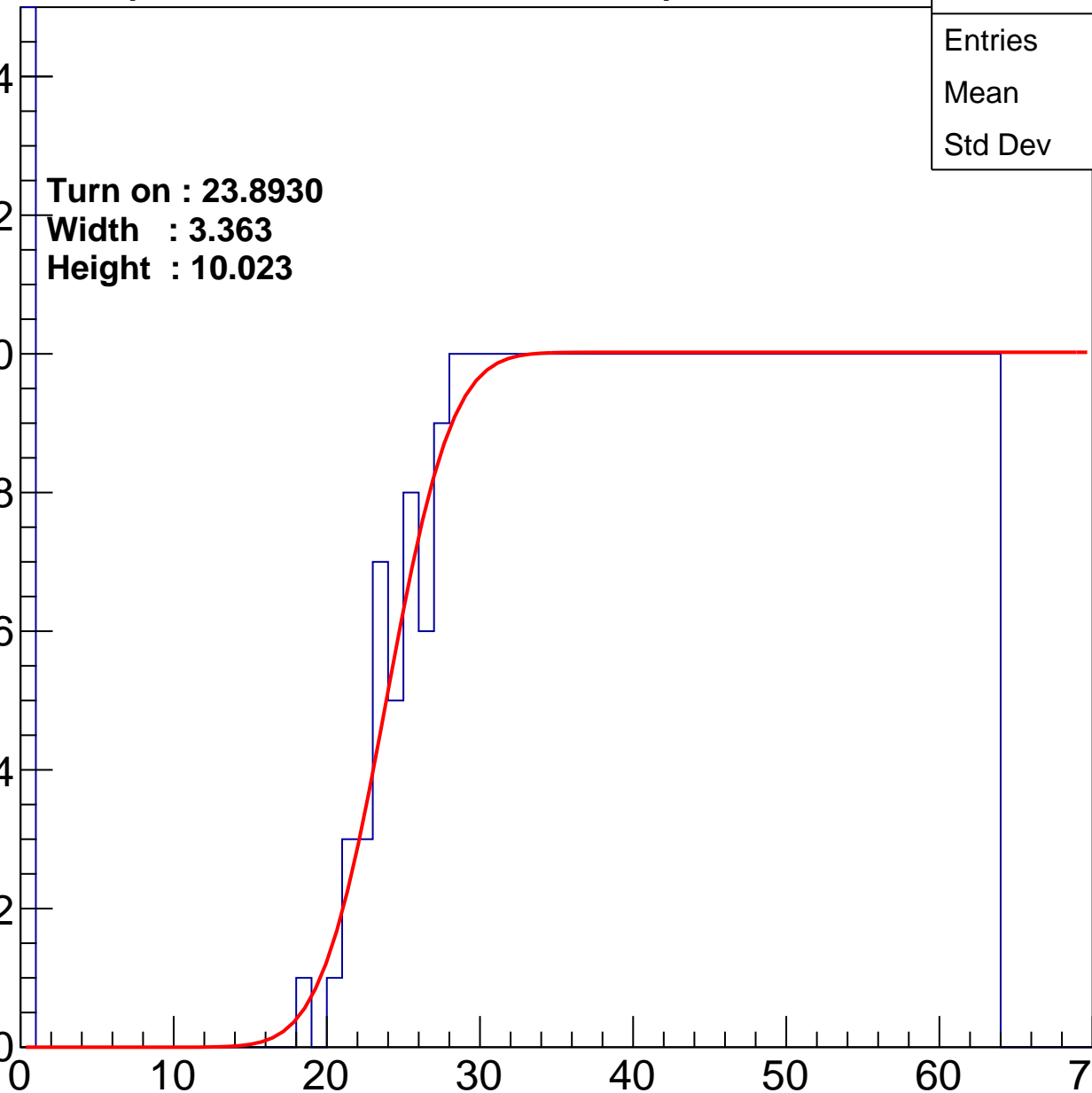
**Width : 3.363**

**Height : 10.023**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch107

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	412
Mean	40.5
Std Dev	16.74

Turn on : 27.5194

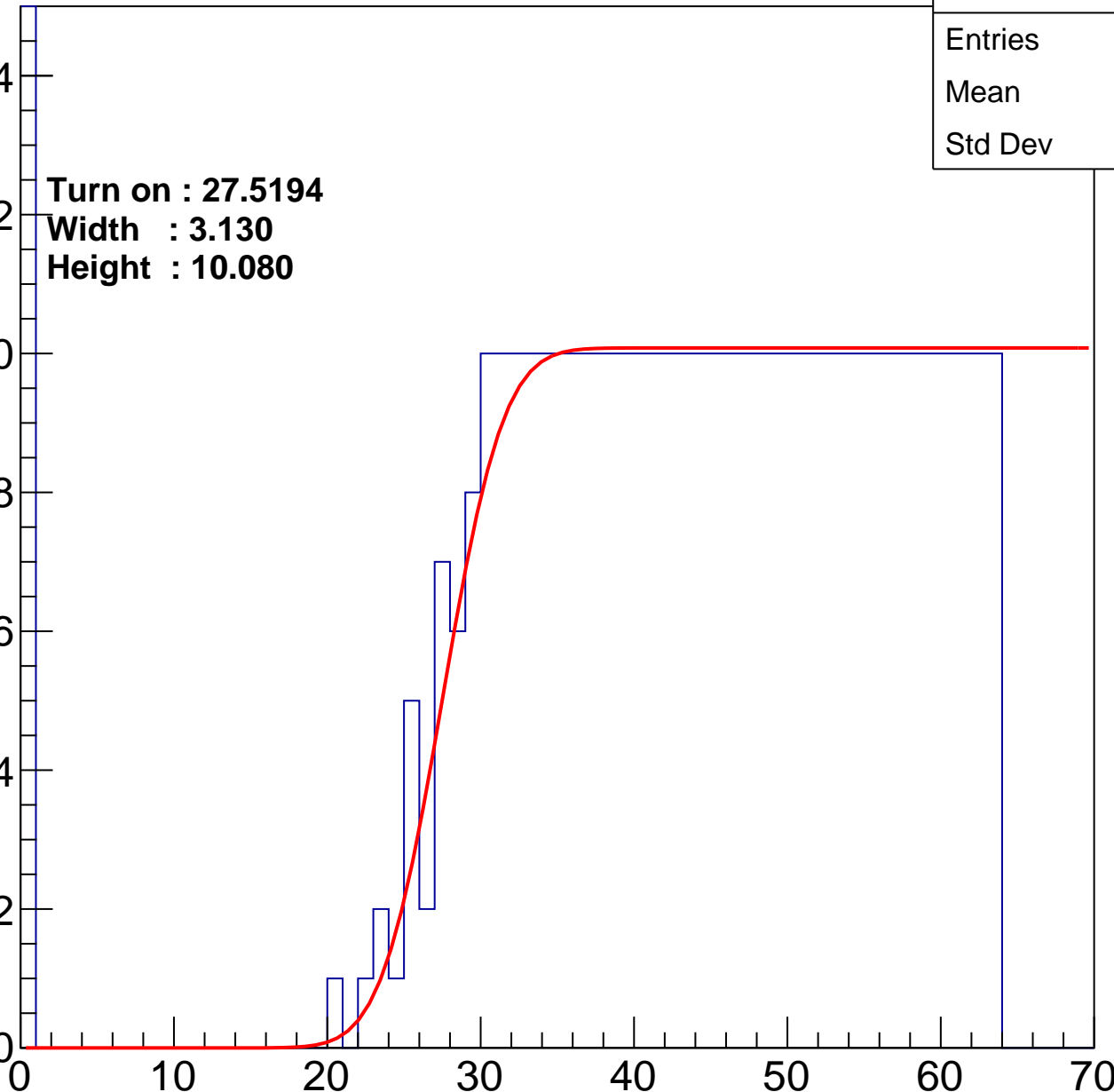
Width : 3.130

Height : 10.080

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch108

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	448
Mean	38.75
Std Dev	17.4

Turn on : 24.5322

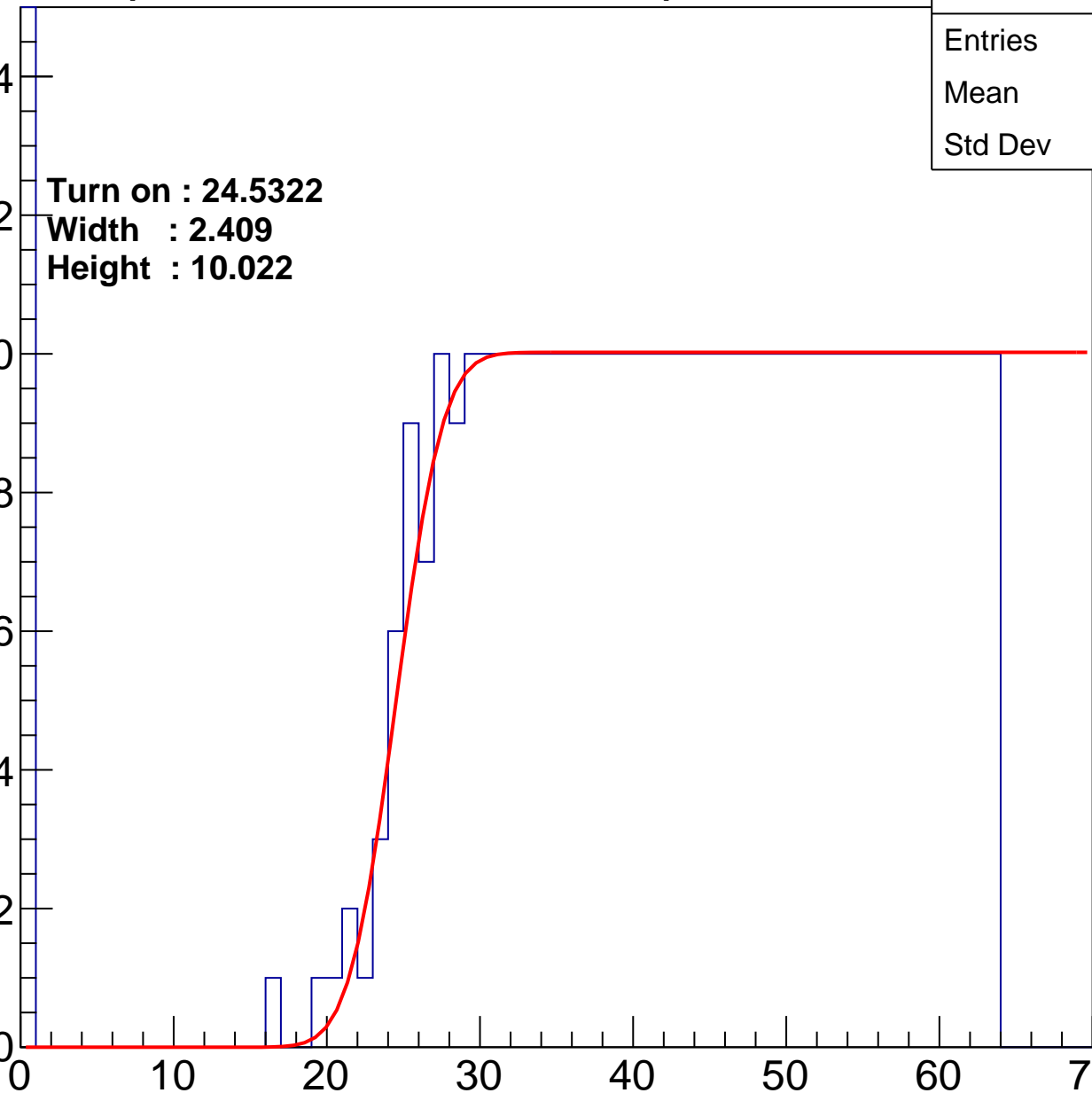
Width : 2.409

Height : 10.022

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch109

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	416
Mean	40.71
Std Dev	16.12

**Turn on : 26.1302**

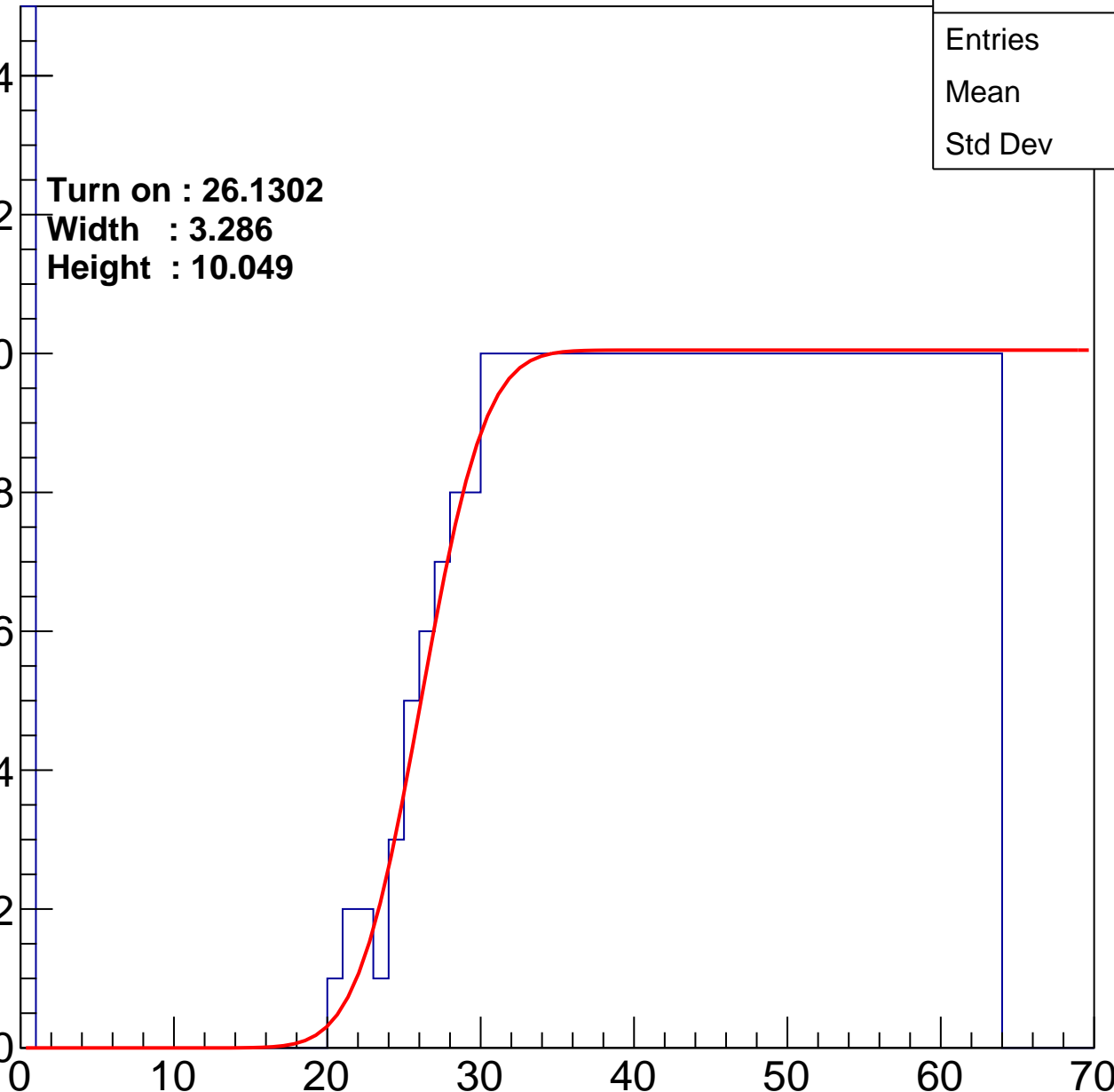
**Width : 3.286**

**Height : 10.049**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch110

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	426
Mean	39.29
Std Dev	17.8

**Turn on : 26.7089**

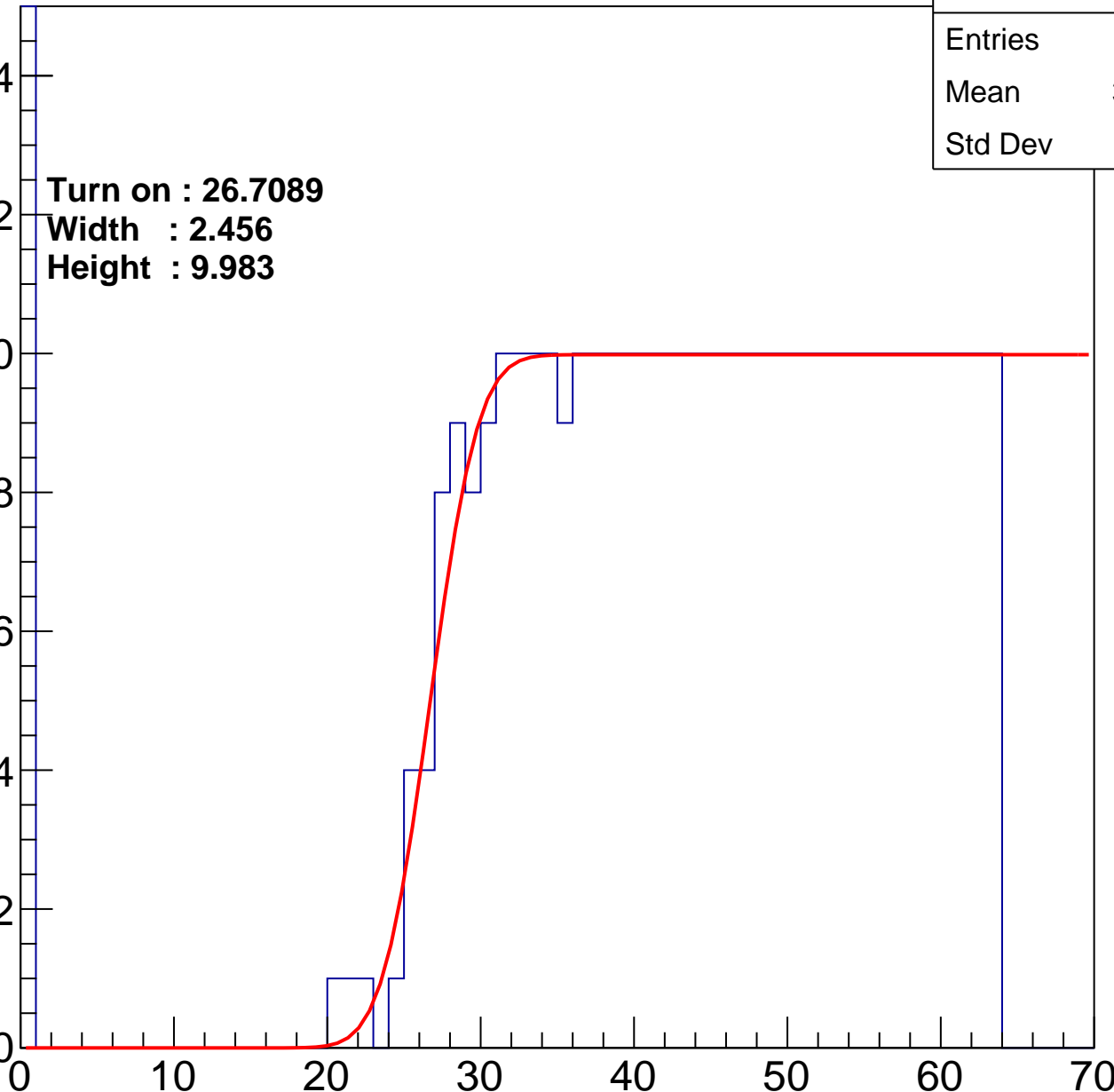
**Width : 2.456**

**Height : 9.983**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U26-ch111

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	440
Mean	39.04
Std Dev	17.42

**Turn on : 24.9839**

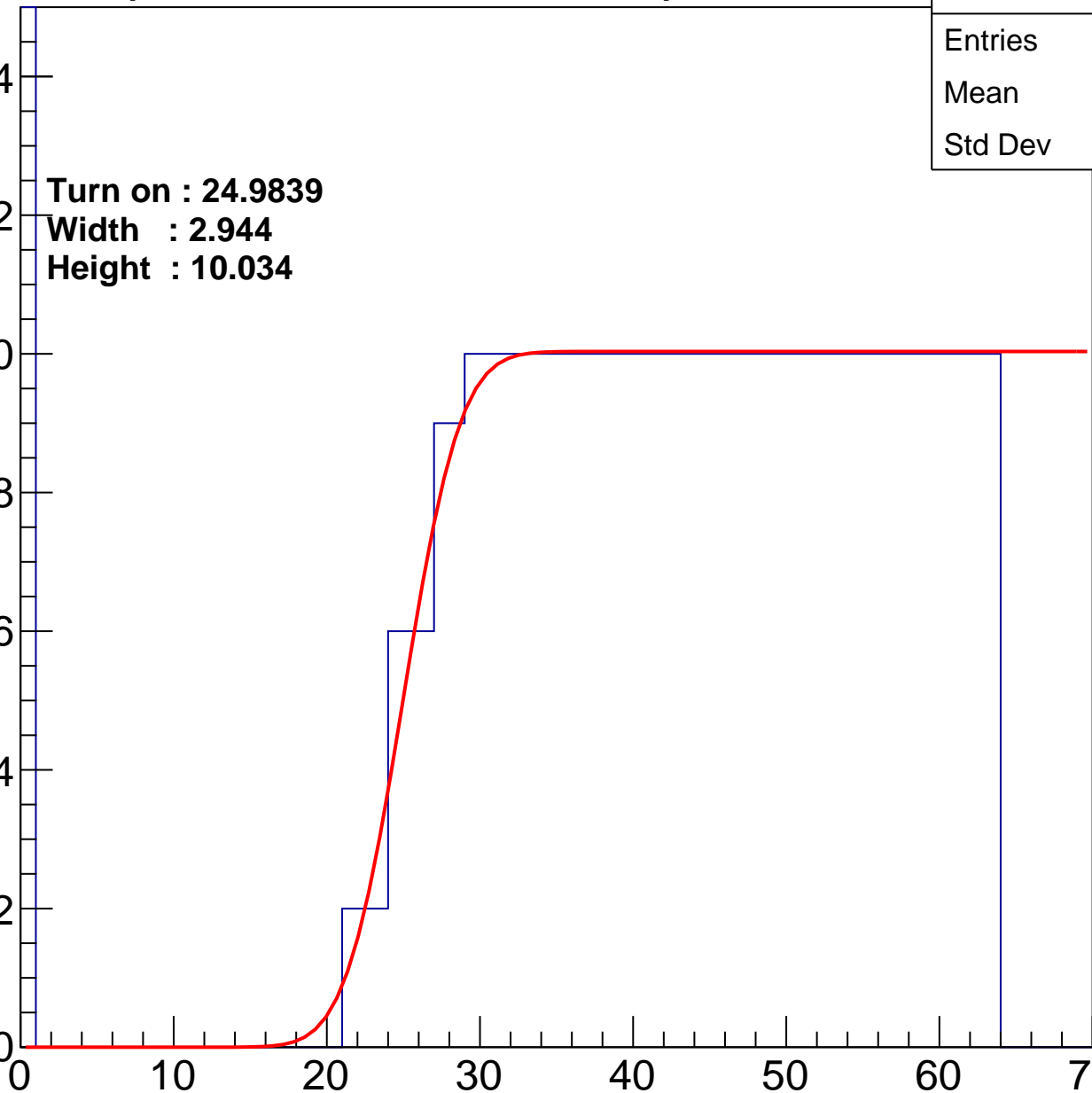
**Width : 2.944**

**Height : 10.034**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch112

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	444
Mean	39.58
Std Dev	16.71

Turn on : 24.3782

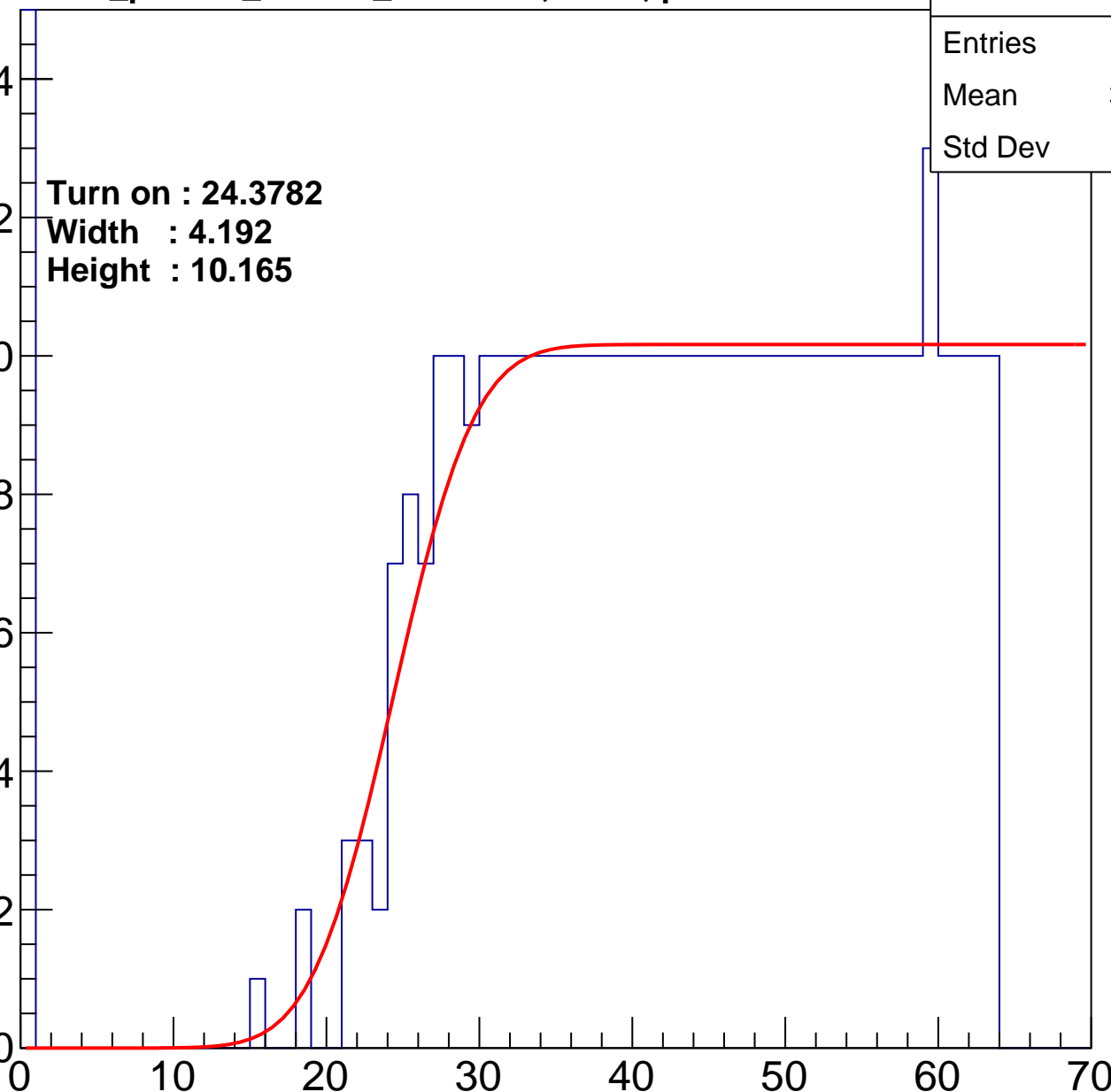
Width : 4.192

Height : 10.165

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch113

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	440
Mean	38.49
Std Dev	18.19

Turn on : 25.4904

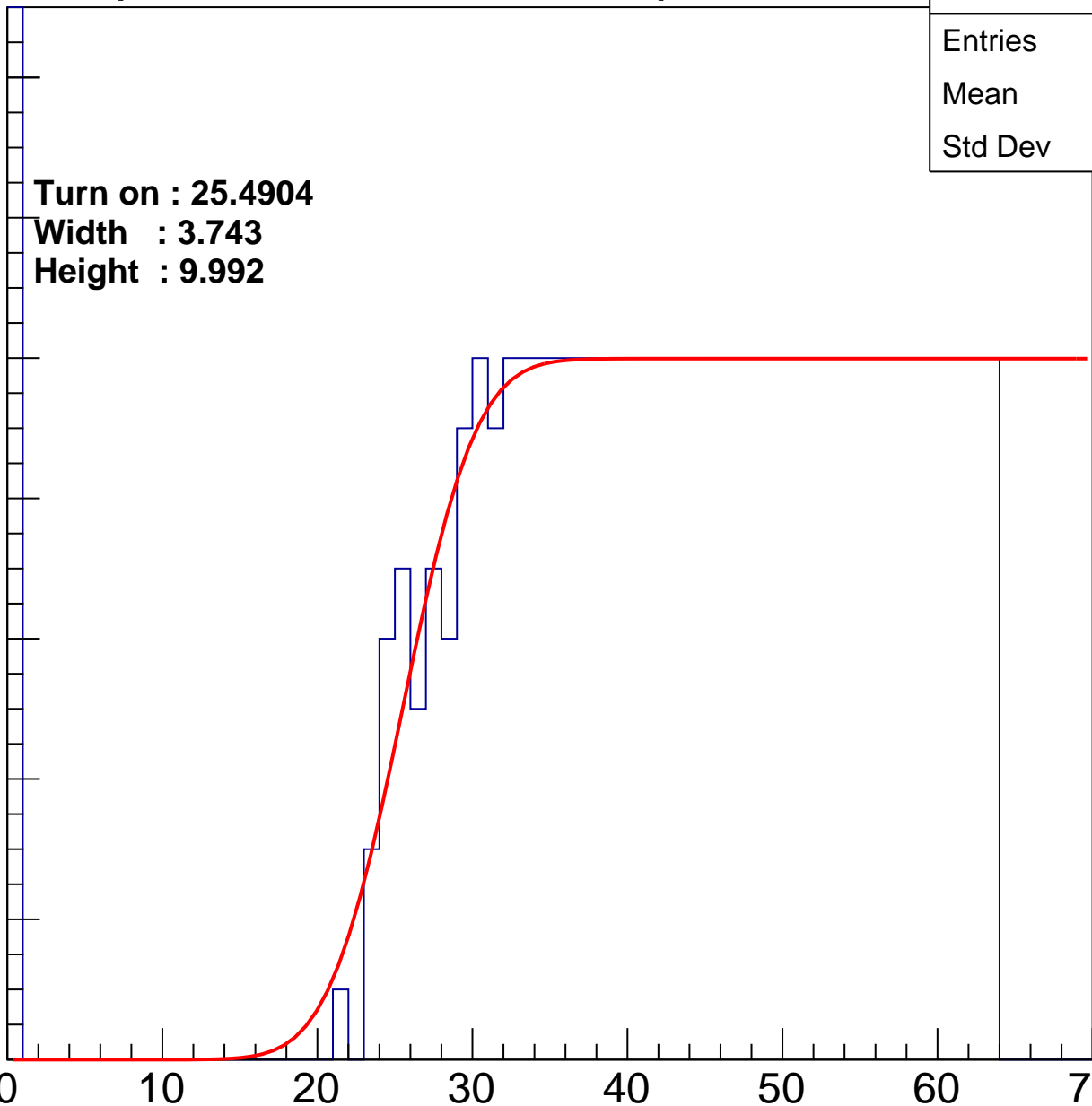
Width : 3.743

Height : 9.992

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch114

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	453
Mean	38.97
Std Dev	16.75

Turn on : 23.4197

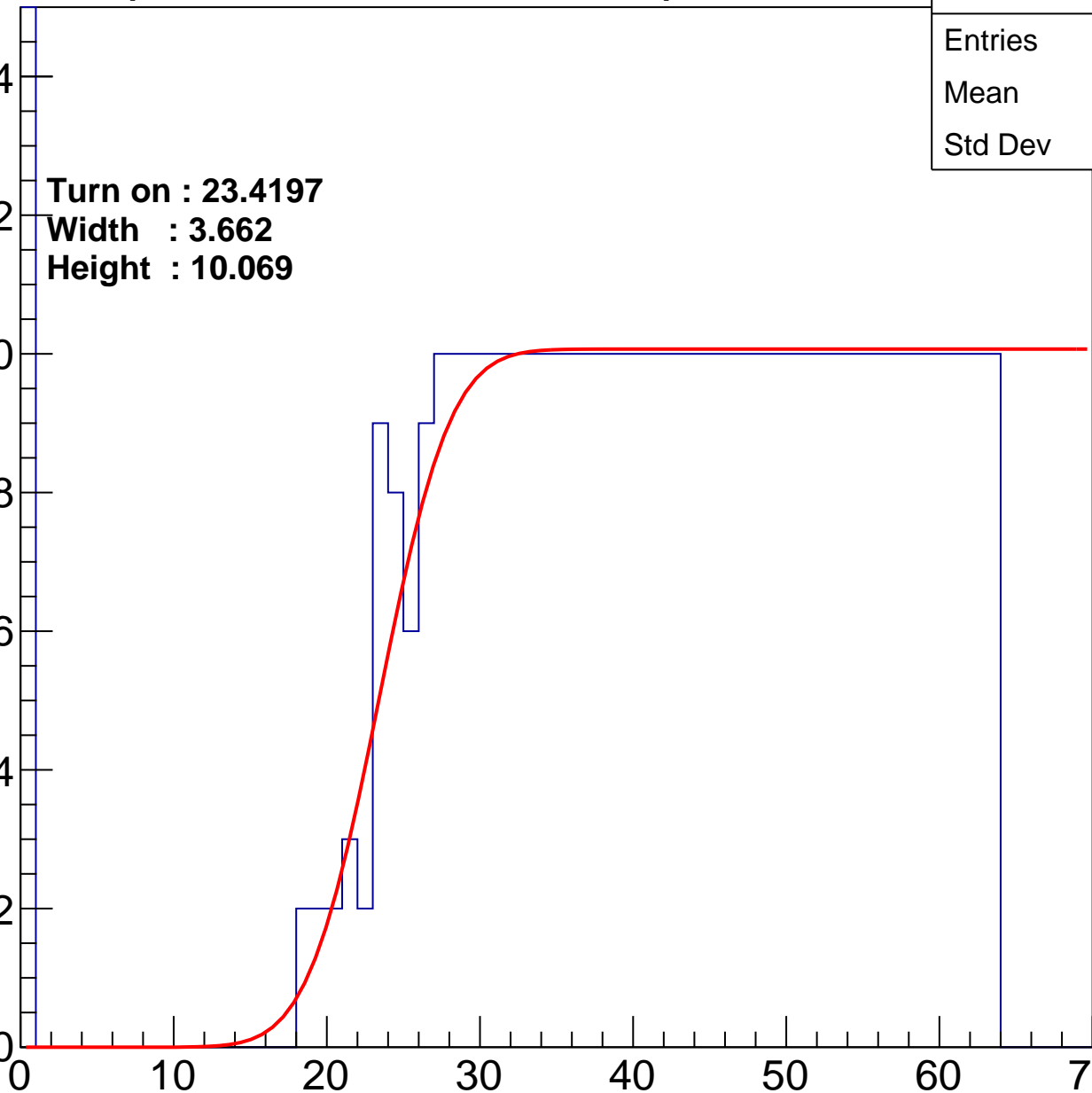
Width : 3.662

Height : 10.069

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch115

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	440
Mean	38.76
Std Dev	17.84

Turn on : 25.5361

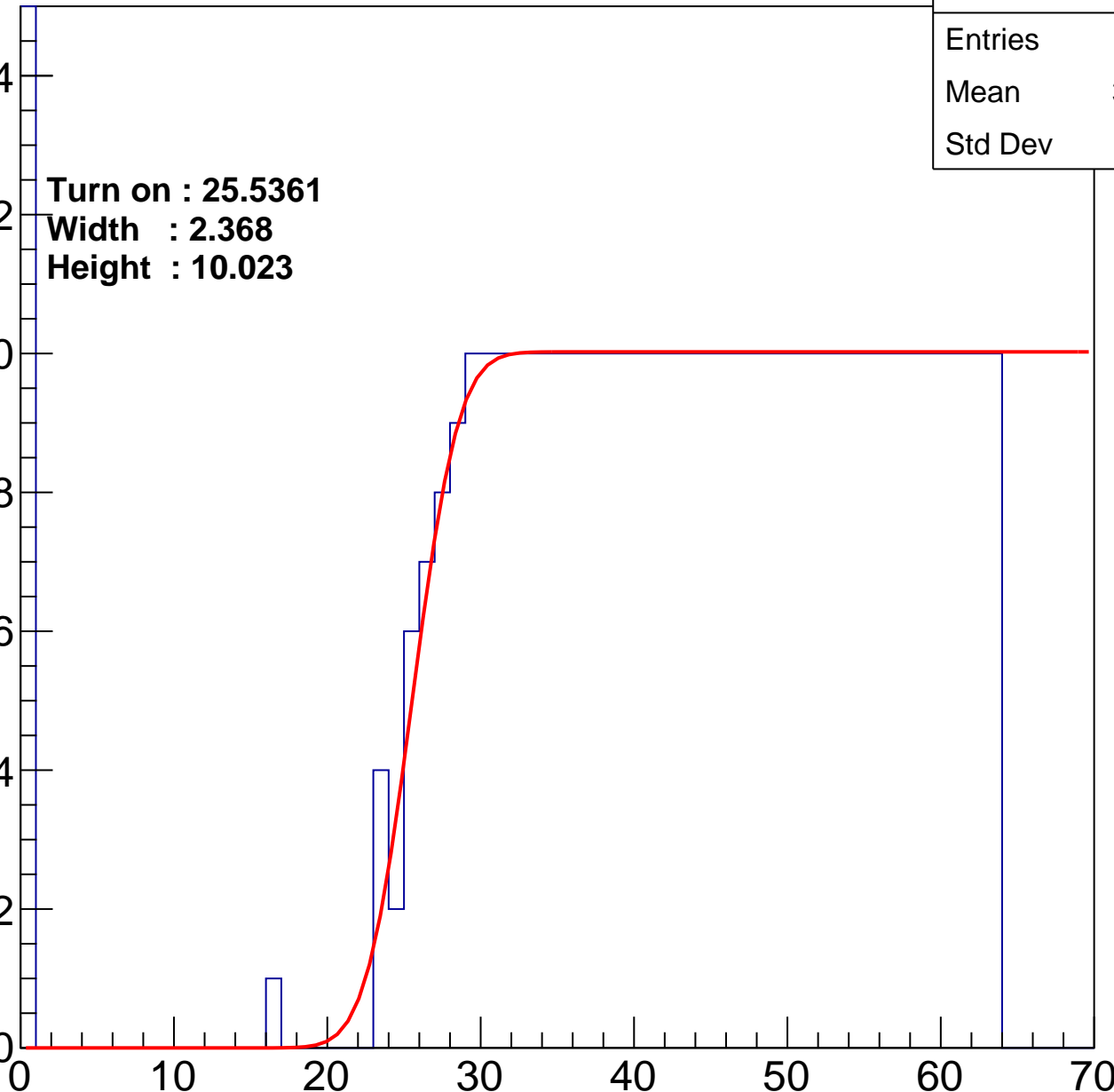
Width : 2.368

Height : 10.023

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch116

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	460
Mean	38.63
Std Dev	16.86

Turn on : 22.2472

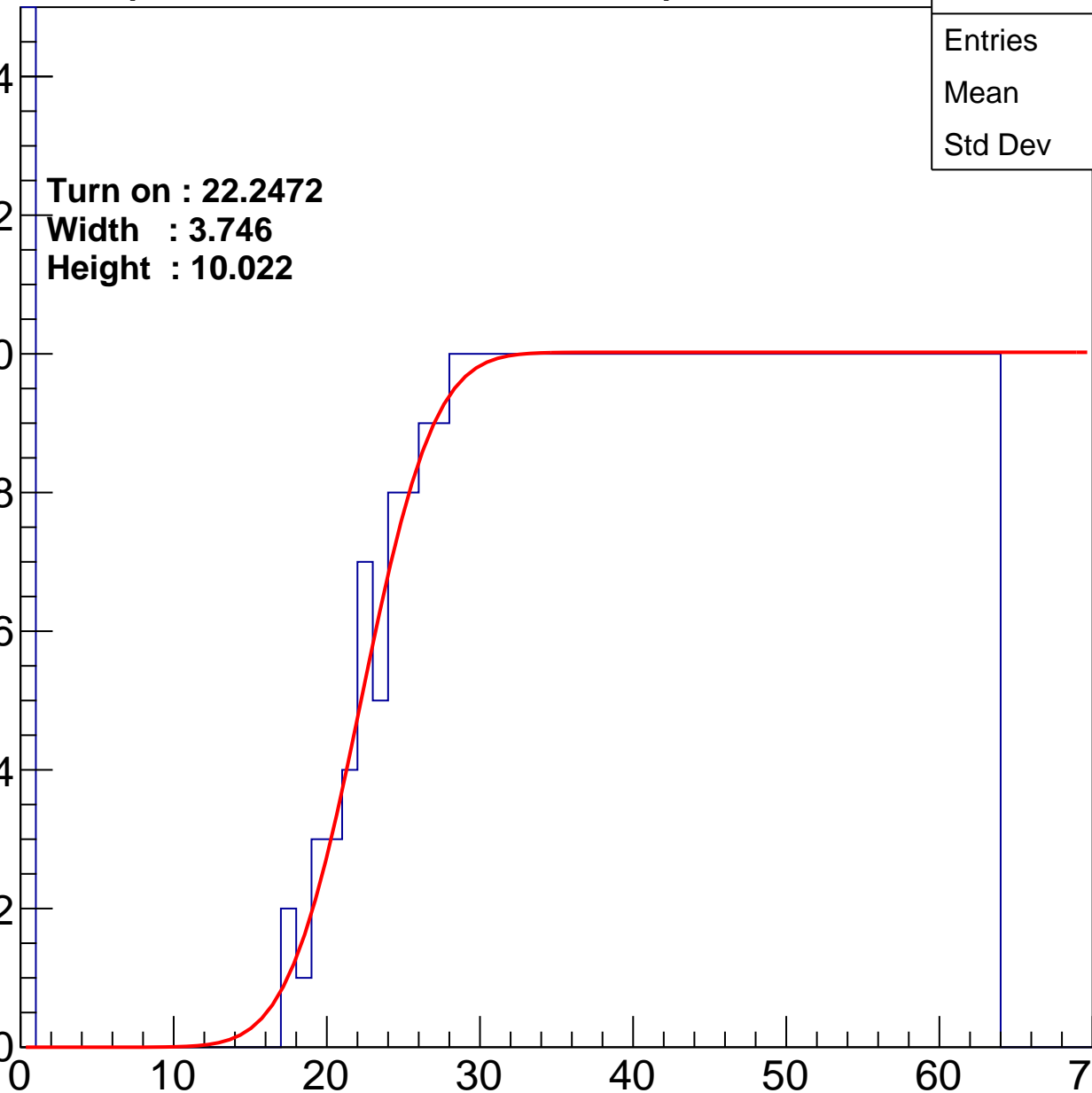
Width : 3.746

Height : 10.022

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch117

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	422
Mean	39.56
Std Dev	17.64

**Turn on : 26.7757**

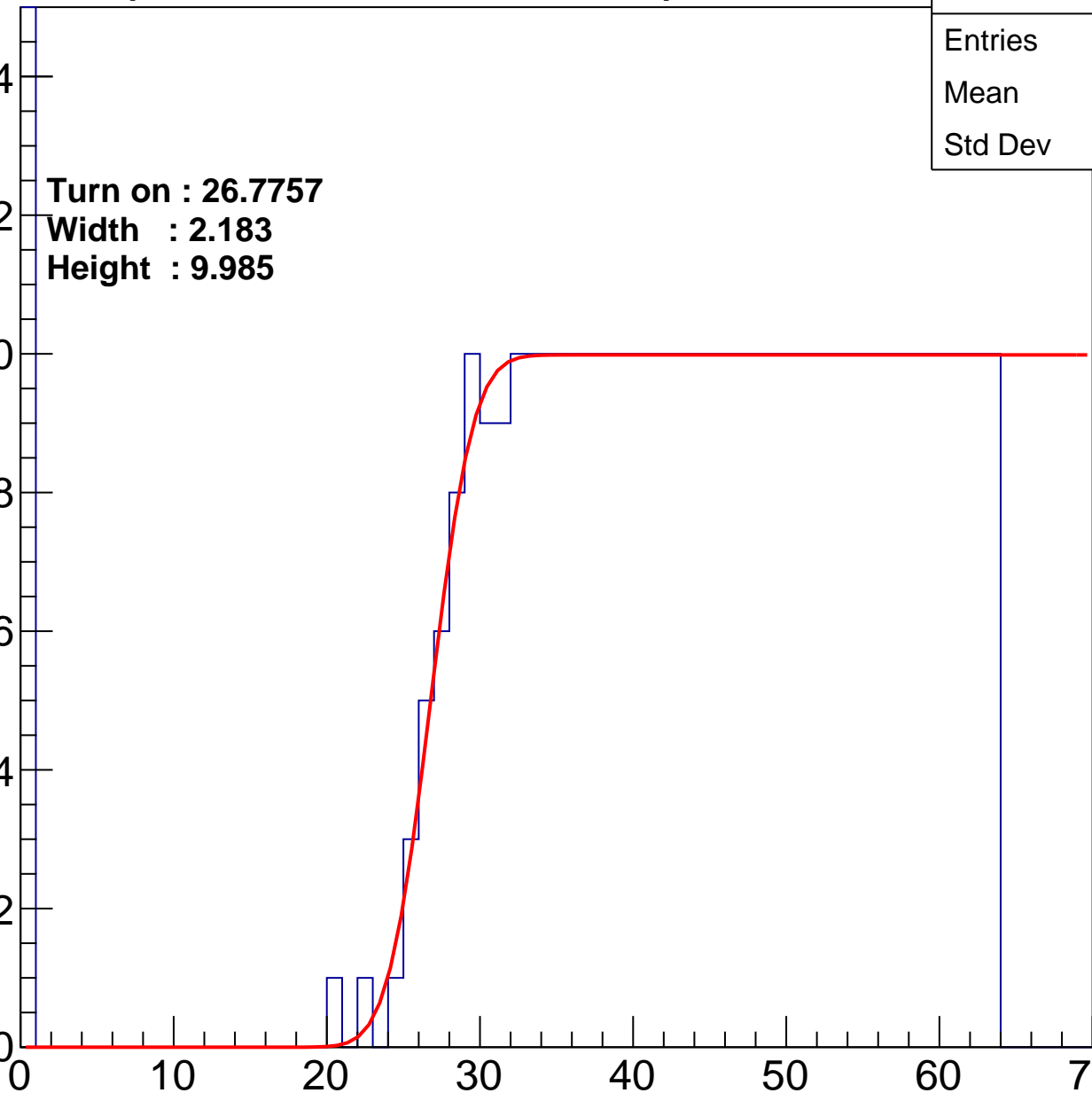
**Width : 2.183**

**Height : 9.985**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch118

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	428
Mean	39.25
Std Dev	17.71

Turn on : 26.1445

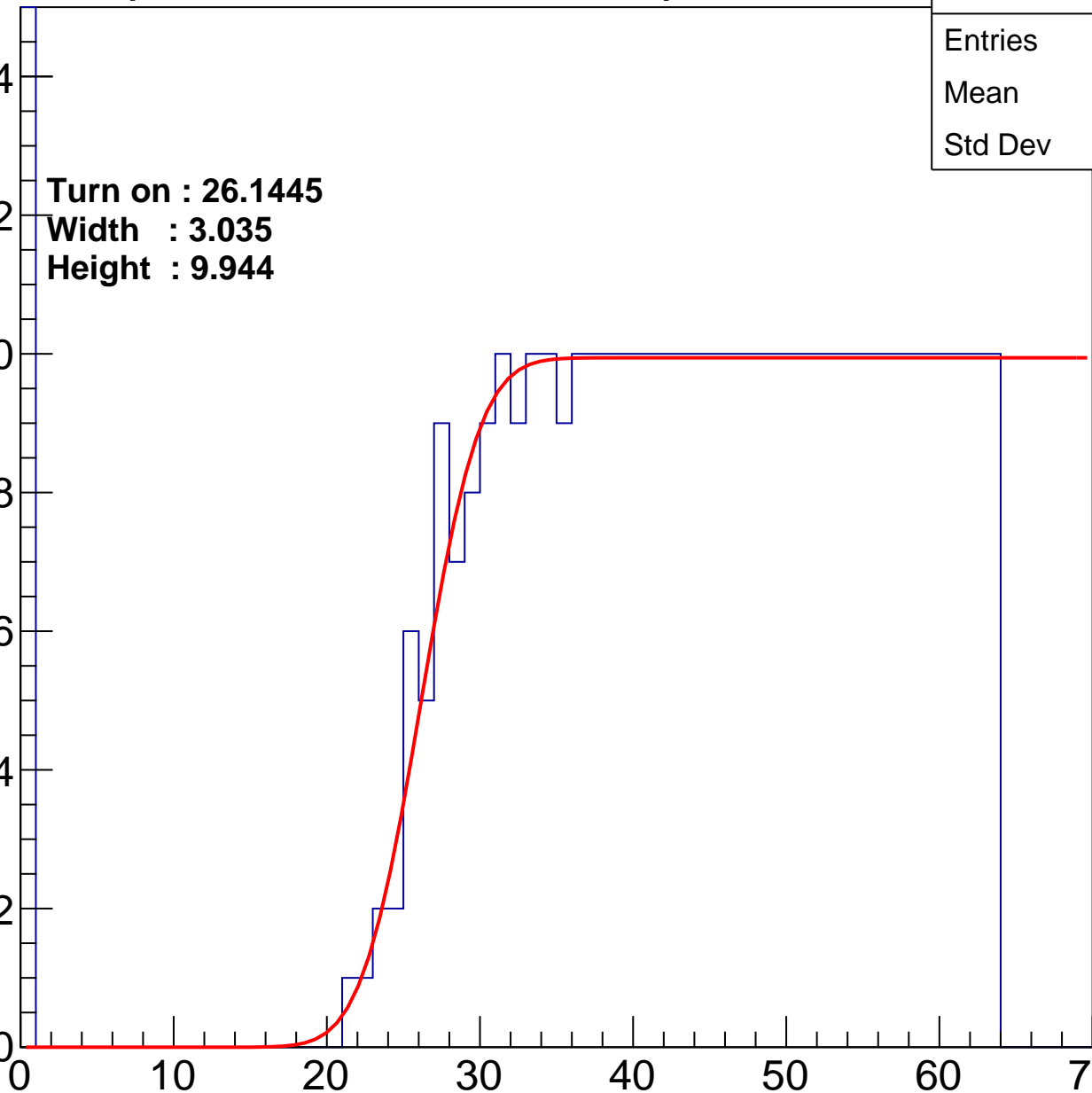
Width : 3.035

Height : 9.944

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U26-ch119

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	429
Mean	39.79
Std Dev	16.87

Turn on : 25.9354

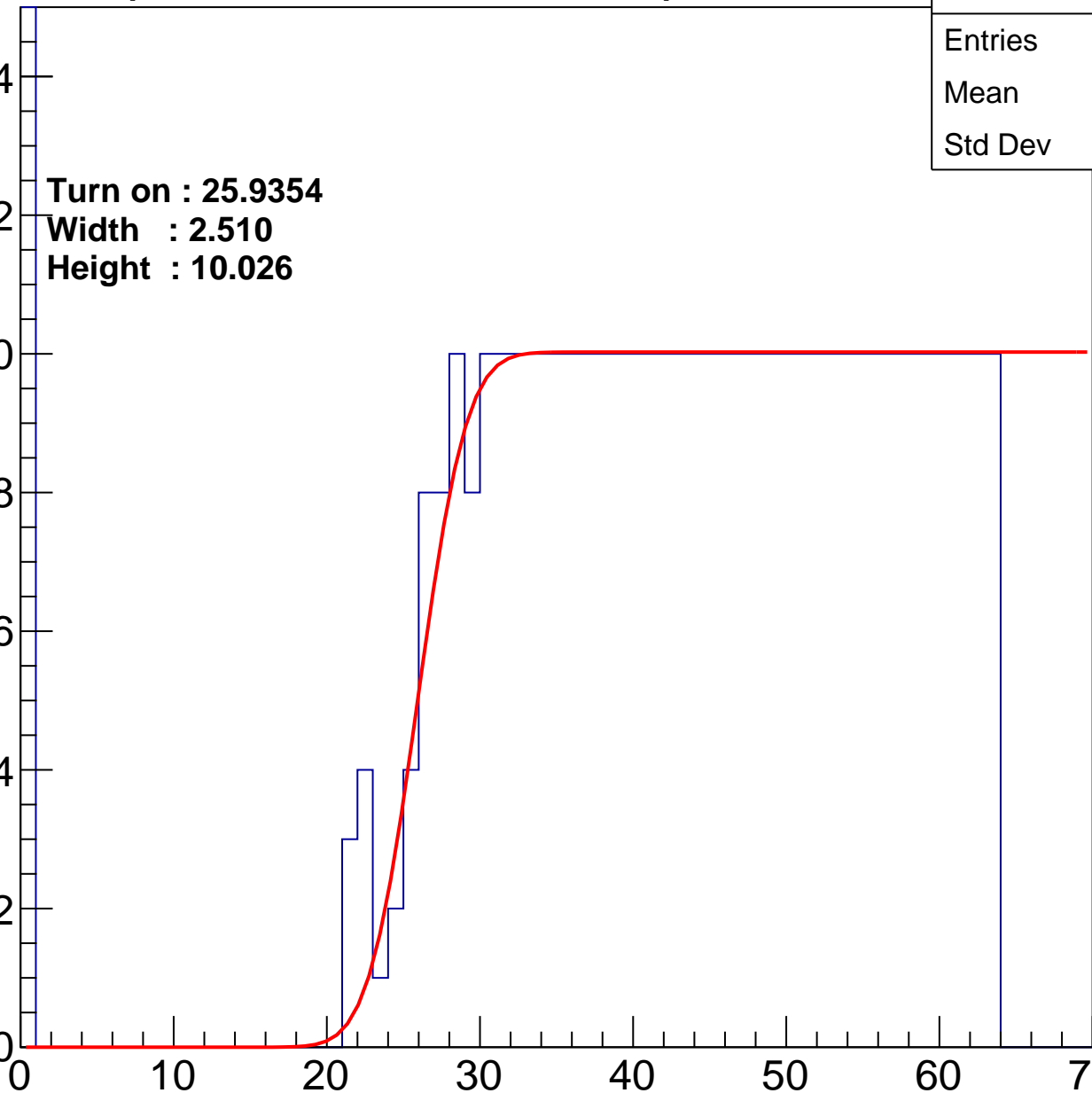
Width : 2.510

Height : 10.026

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch120

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	453
Mean	38.55
Std Dev	17.41

Turn on : 23.8939

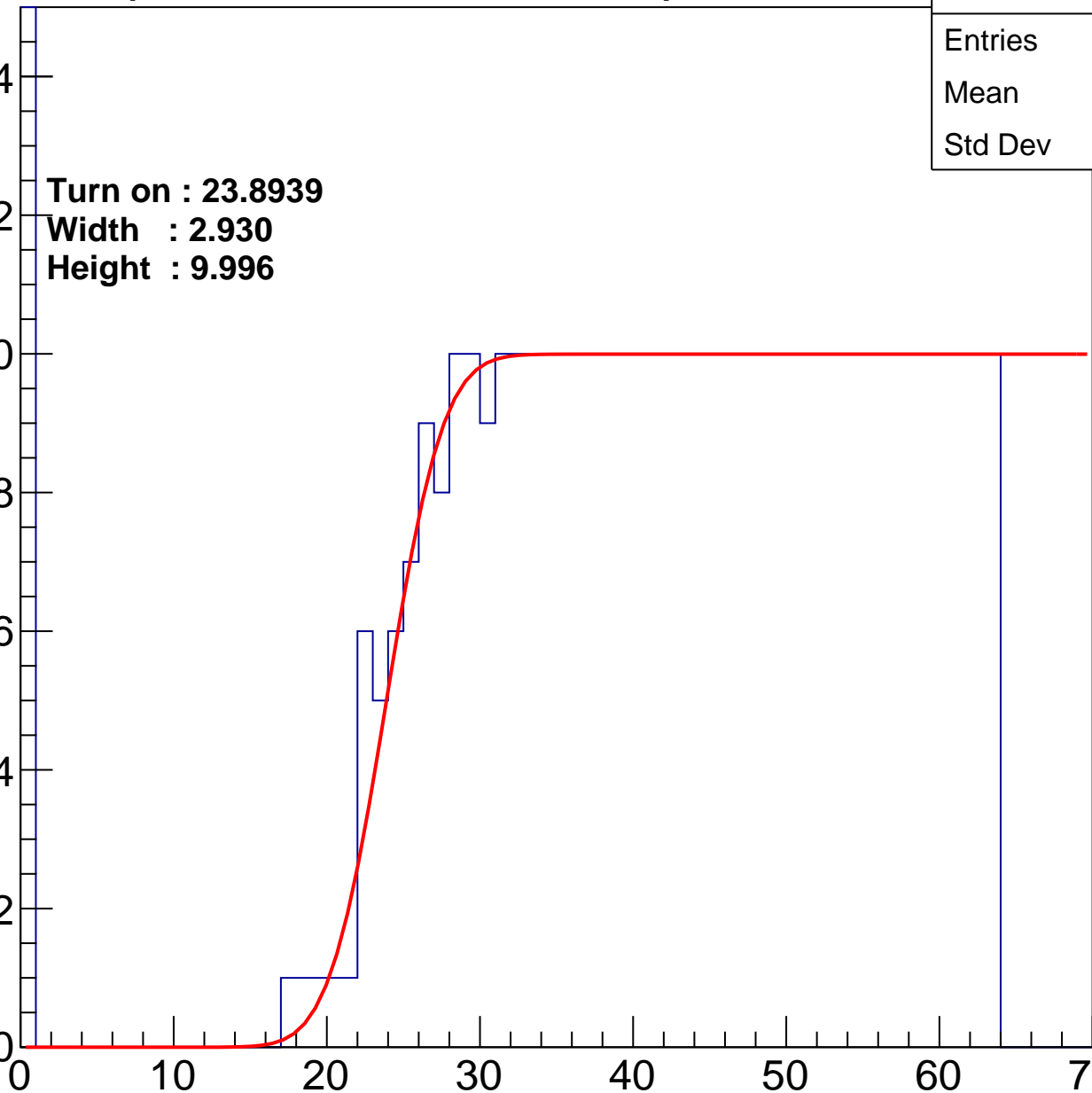
Width : 2.930

Height : 9.996

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch121

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	420
Mean	40.18
Std Dev	16.75

Turn on : 26.1659

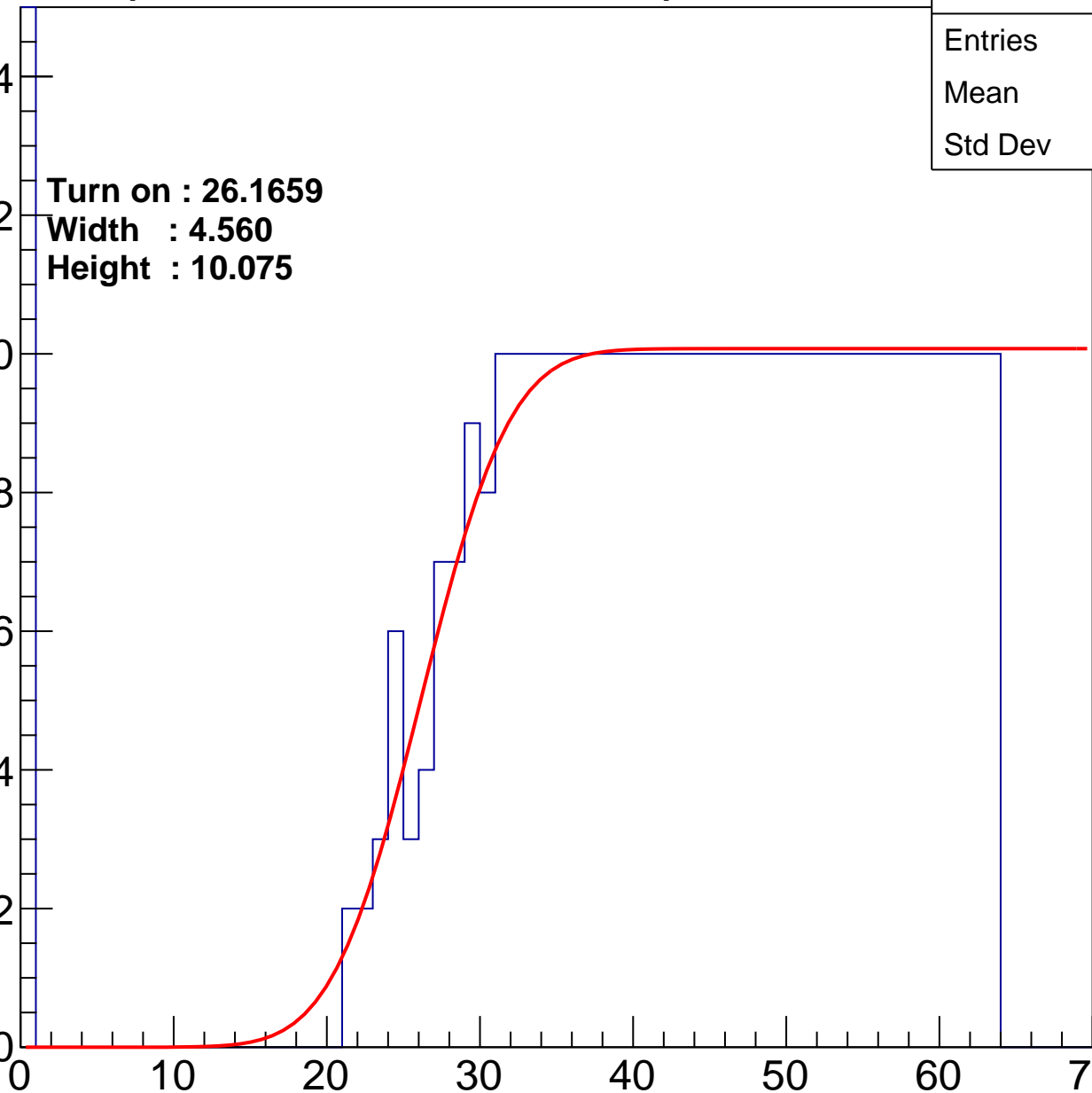
Width : 4.560

Height : 10.075

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch122

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	427
Mean	39.36
Std Dev	17.69

Turn on : 26.1921

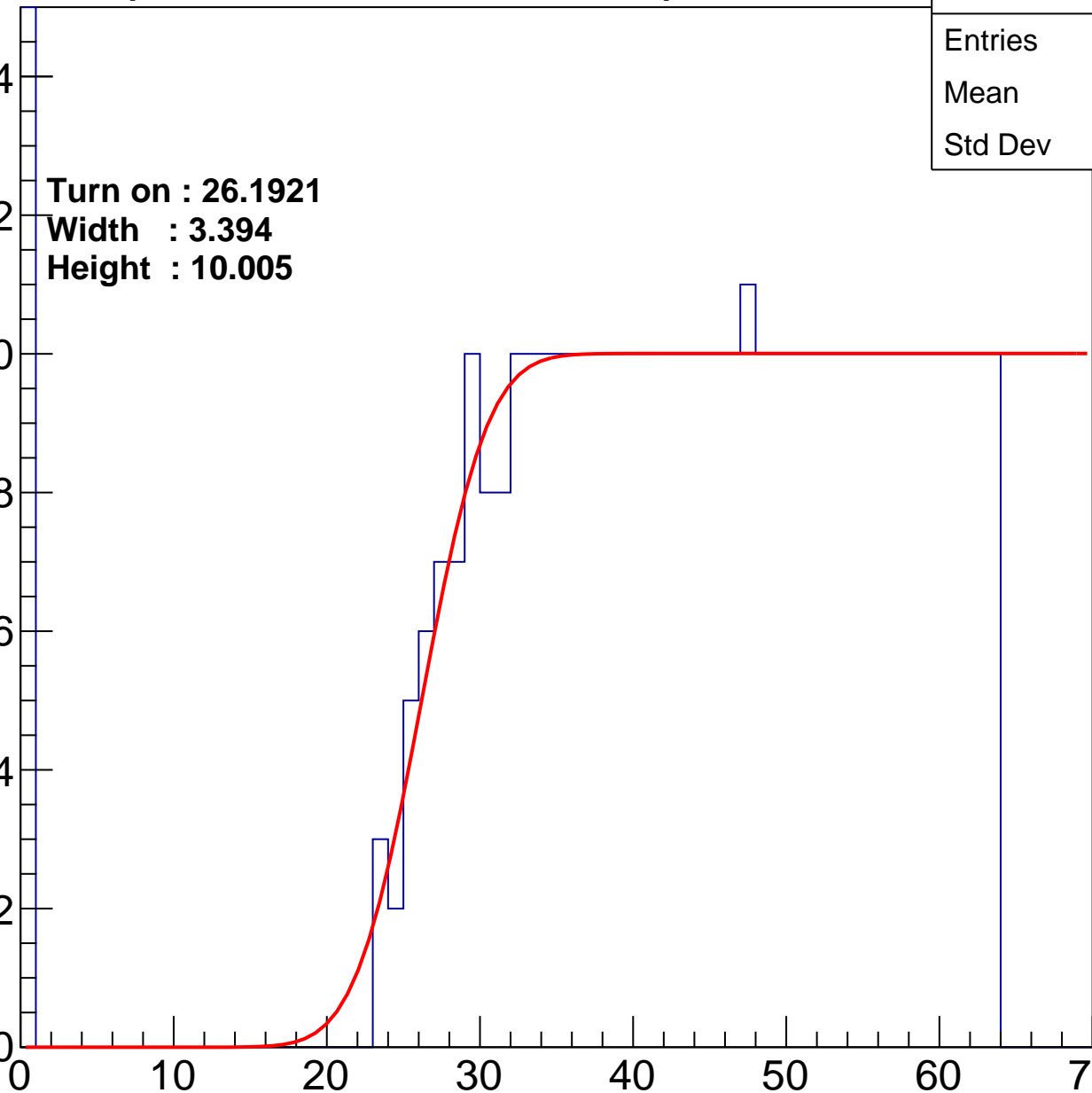
Width : 3.394

Height : 10.005

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch123

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	428
Mean	39.03
Std Dev	18.06

Turn on : 26.8416

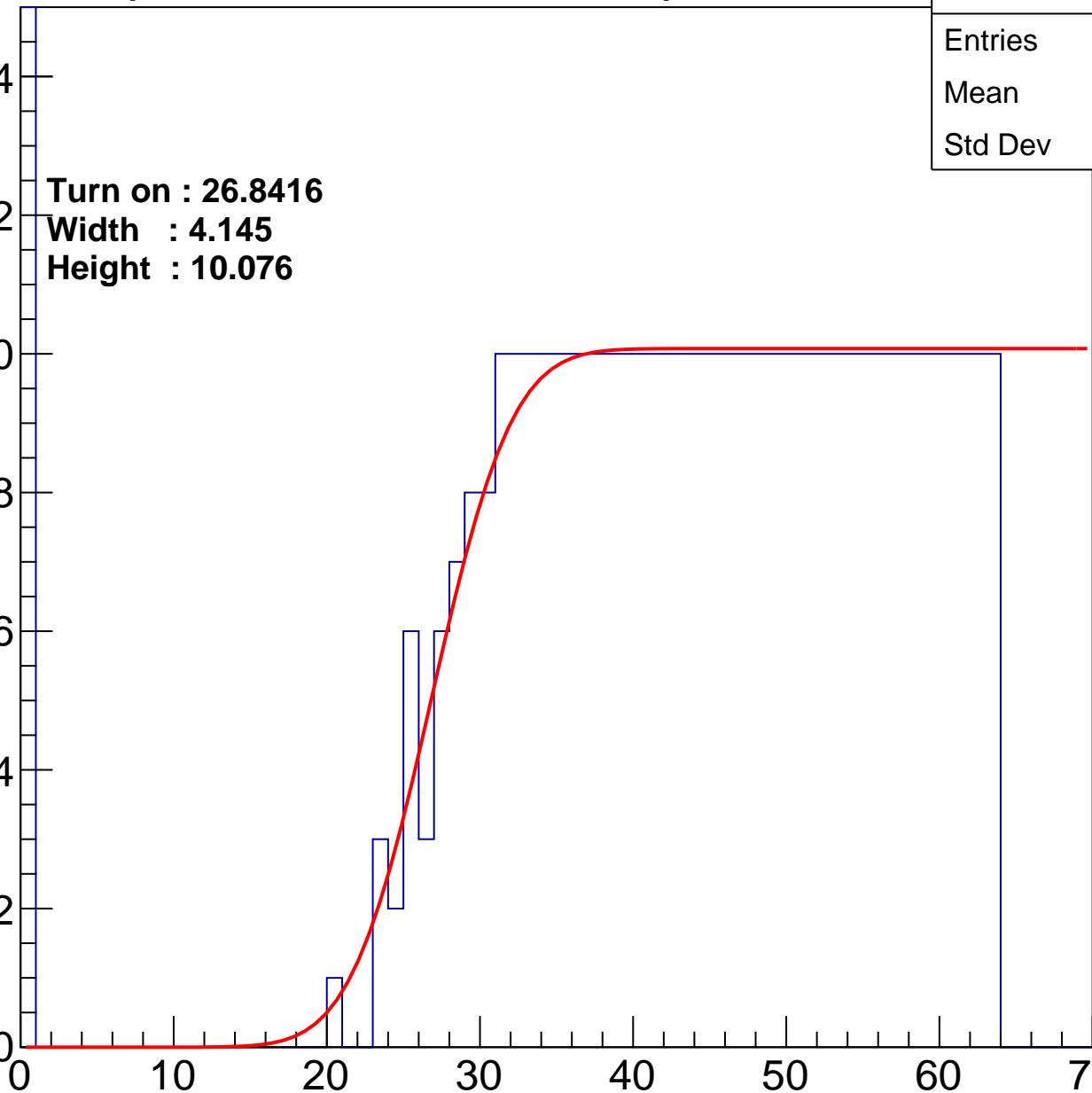
Width : 4.145

Height : 10.076

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch124

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	442
Mean	38.64
Std Dev	17.87

Turn on : 25.2906

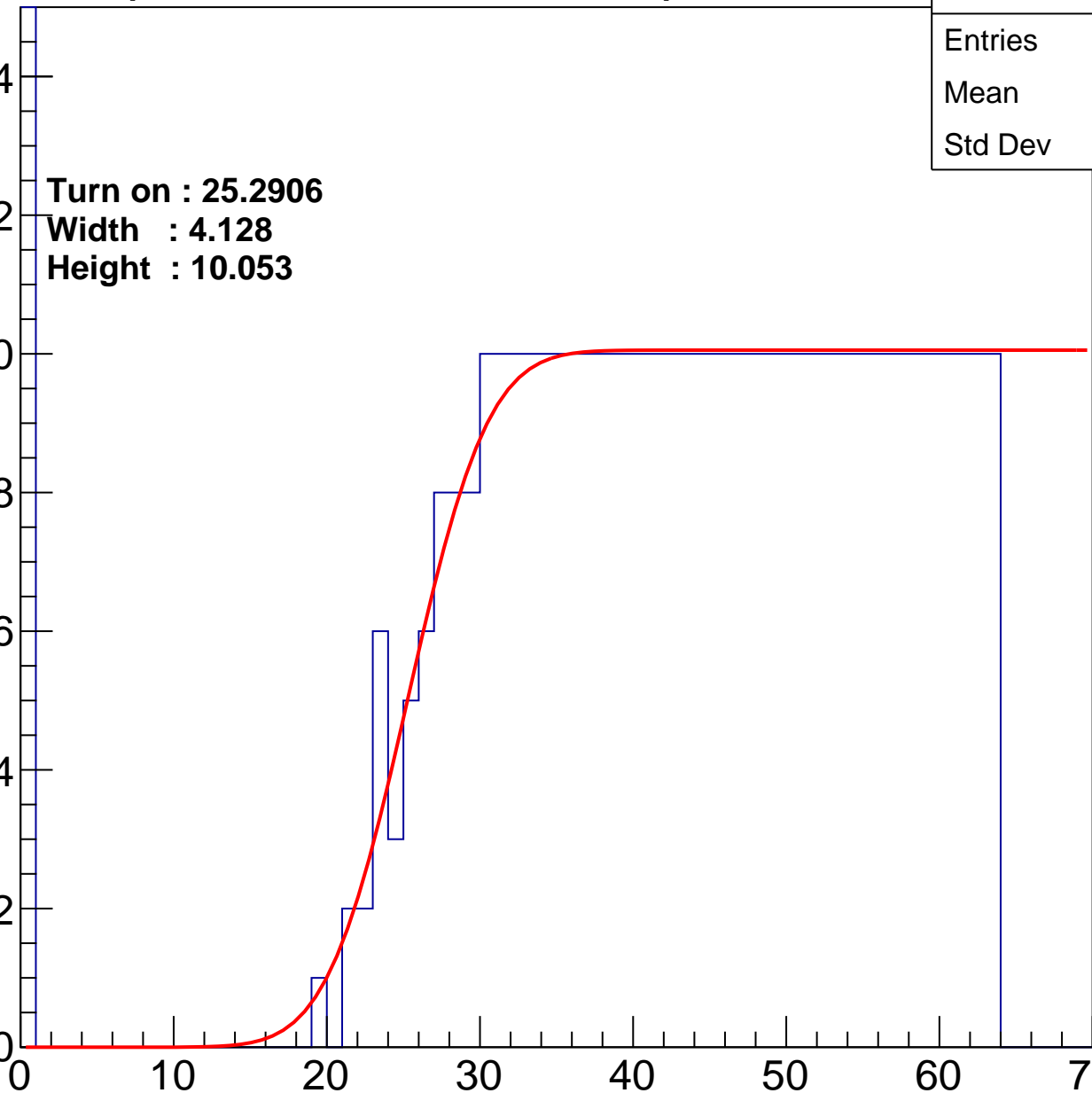
Width : 4.128

Height : 10.053

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch125

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	465
Mean	38.05
Std Dev	17.51

Turn on : 22.6041

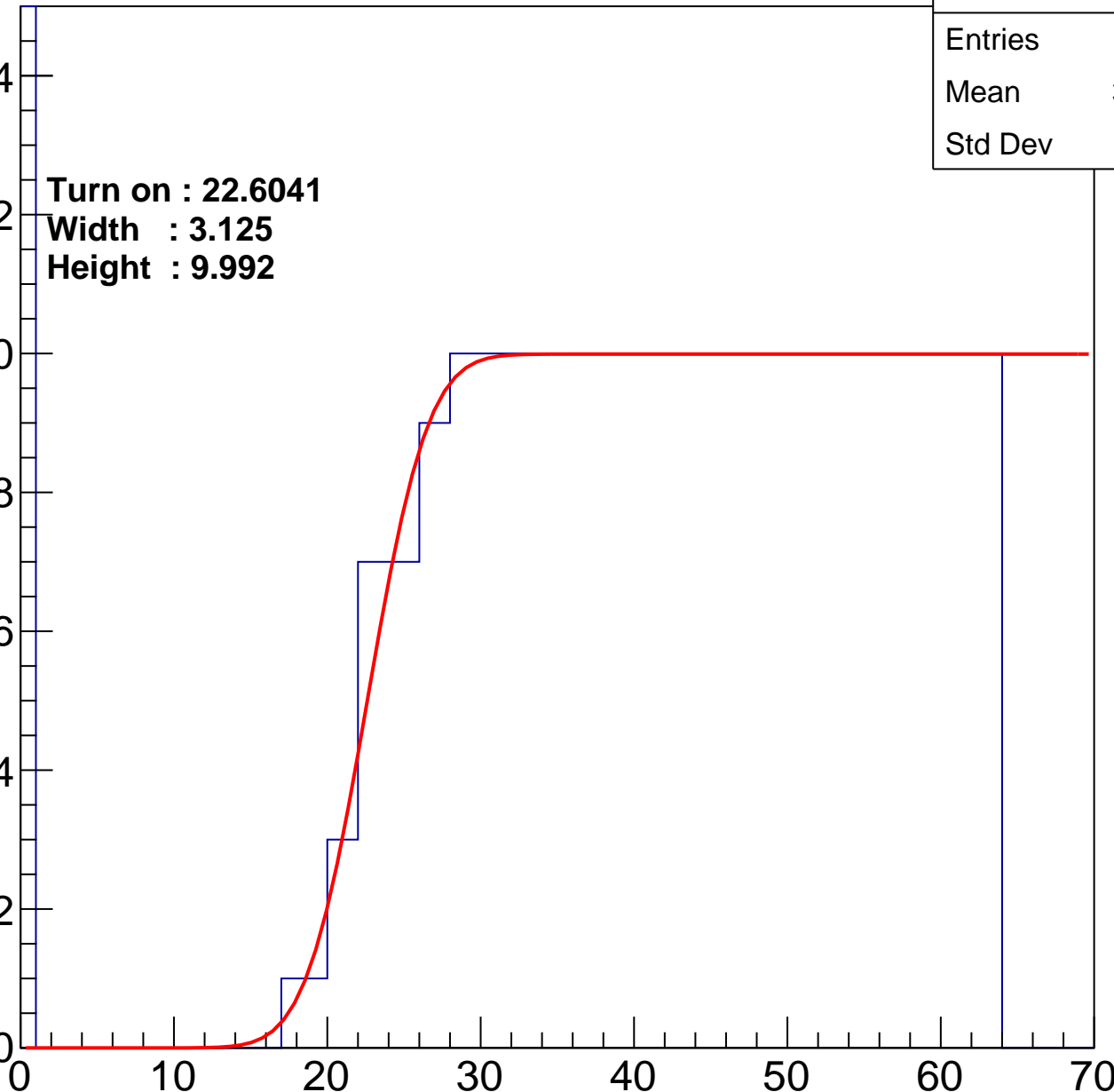
Width : 3.125

Height : 9.992

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch126

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	484
Mean	37.67
Std Dev	17.04

**Turn on : 19.8943**

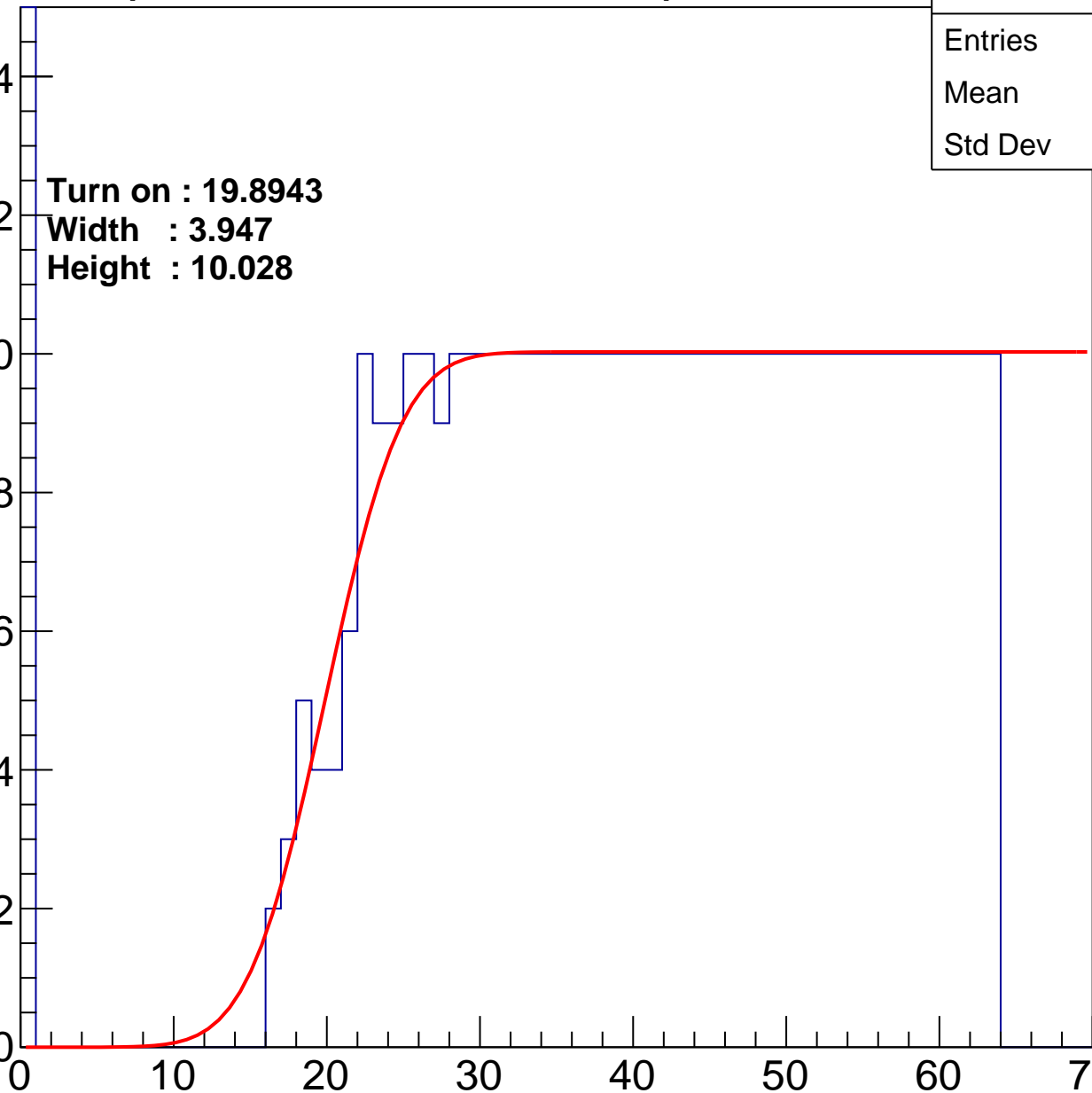
**Width : 3.947**

**Height : 10.028**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B1L103S, U26-ch127

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	459
Mean	37.66
Std Dev	18.41

Turn on : 24.4790

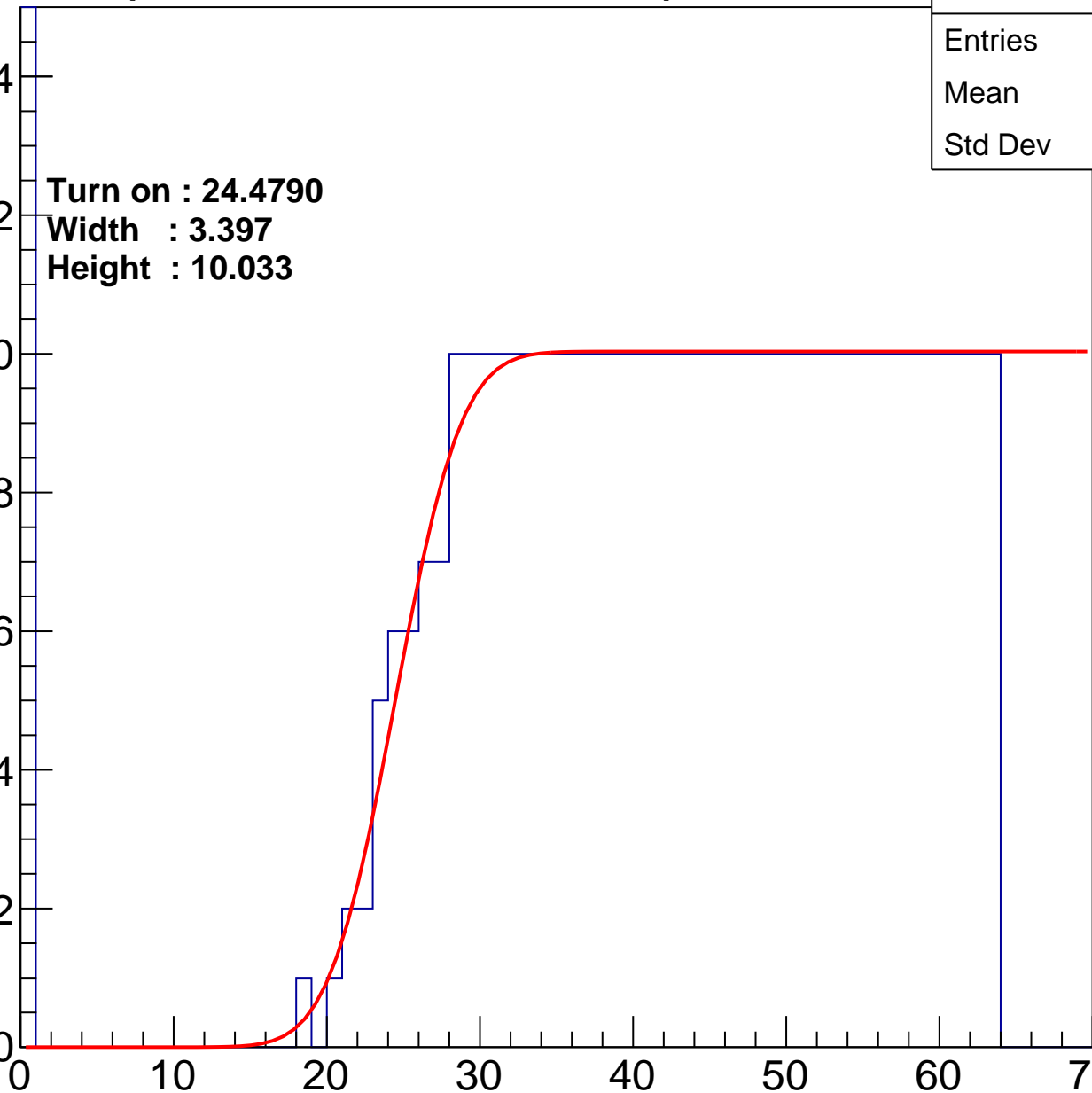
Width : 3.397

Height : 10.033

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B1L103S, U26-ch127

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	459
Mean	37.66
Std Dev	18.41

Turn on : 24.4790

Width : 3.397

Height : 10.033

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

