



# B1L101S, U3-ch0, adc0

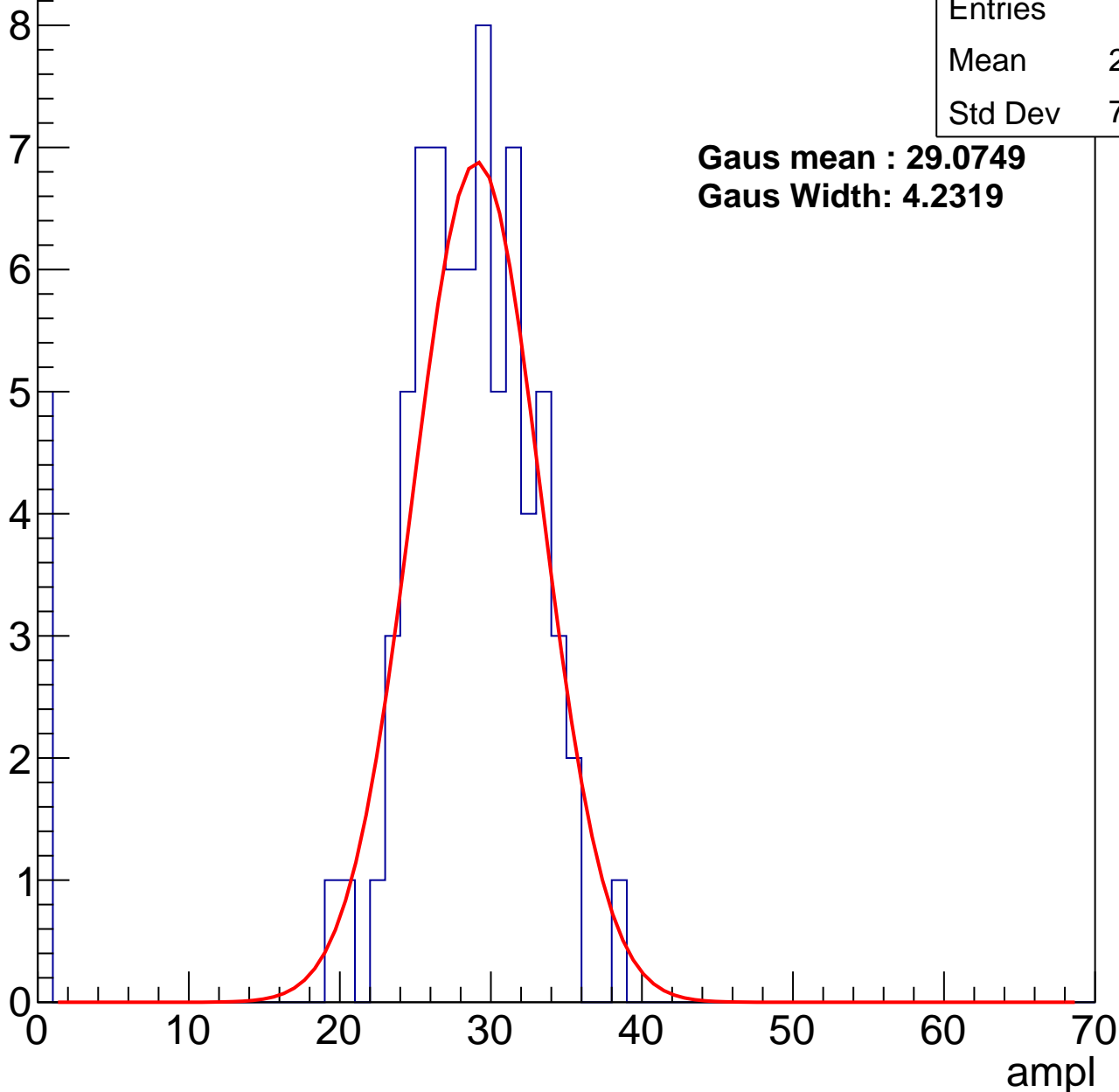
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	26.48
Std Dev	7.863

**Gaus mean : 29.0749**

**Gaus Width: 4.2319**



# B1L101S, U3-ch0, adc1

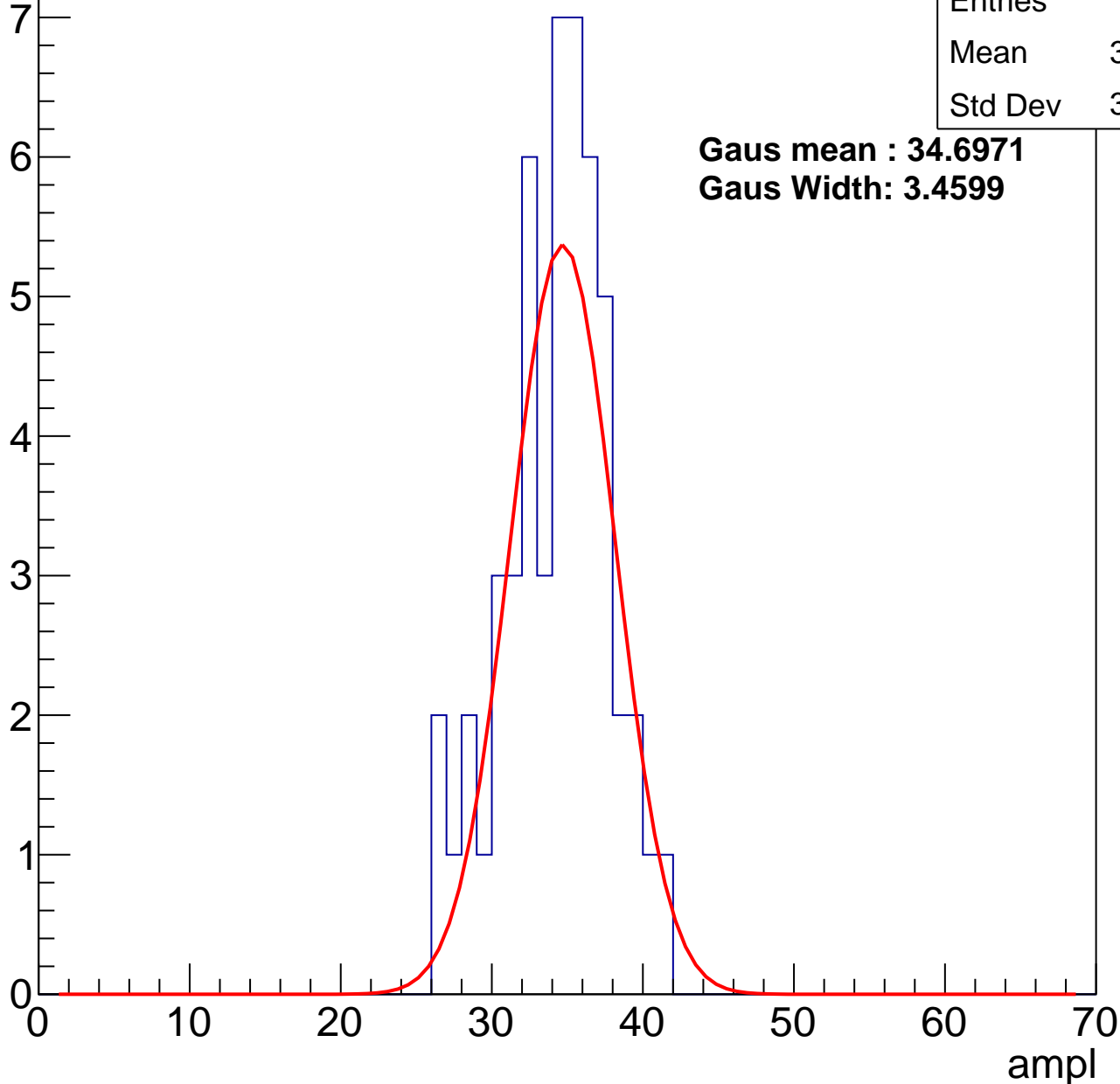
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	33.79
Std Dev	3.444

**Gaus mean : 34.6971**

**Gaus Width: 3.4599**



# B1L101S, U3-ch0, adc2

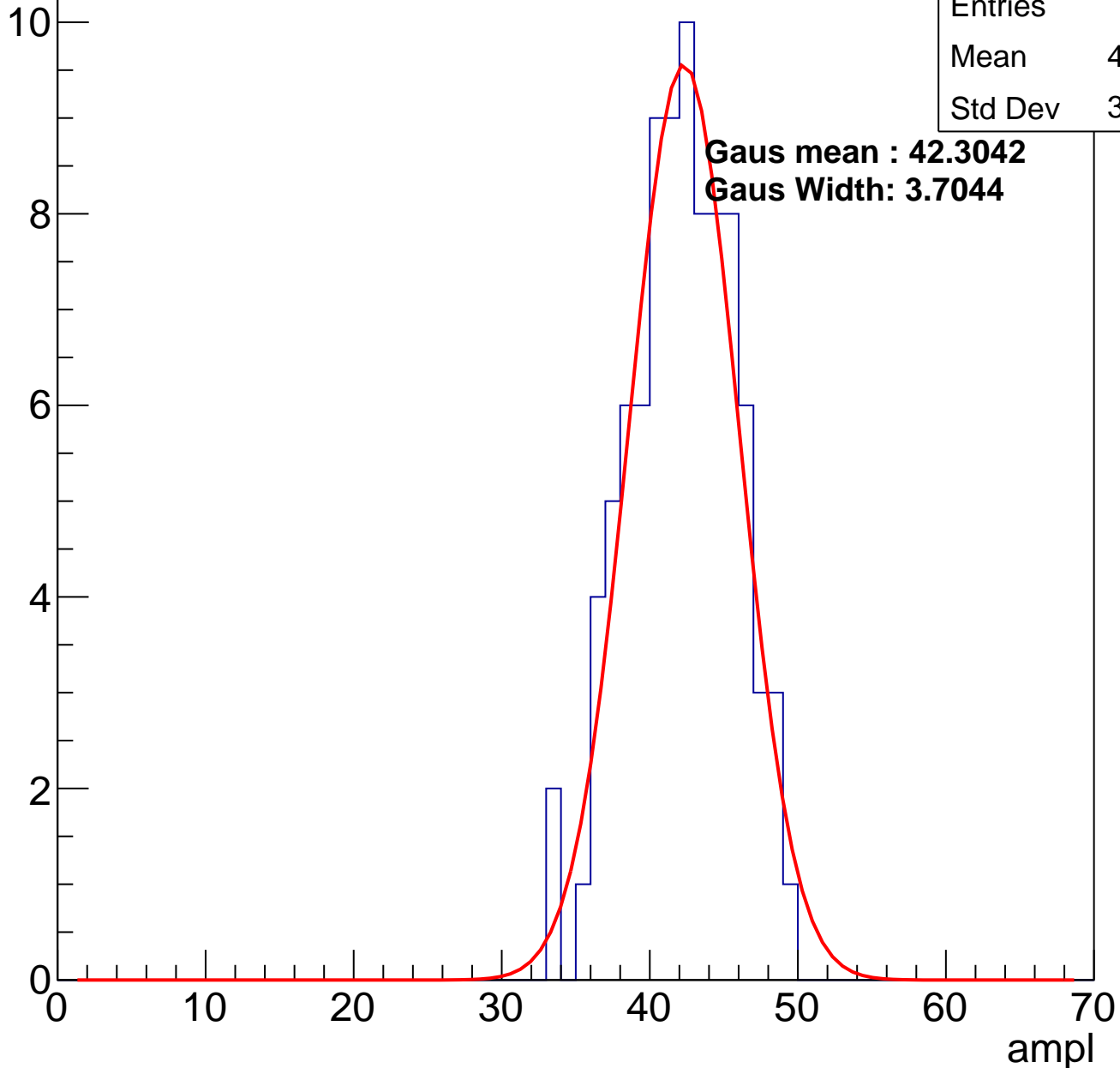
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	89
Mean	41.65
Std Dev	3.522

**Gaus mean : 42.3042**

**Gaus Width: 3.7044**

Entry

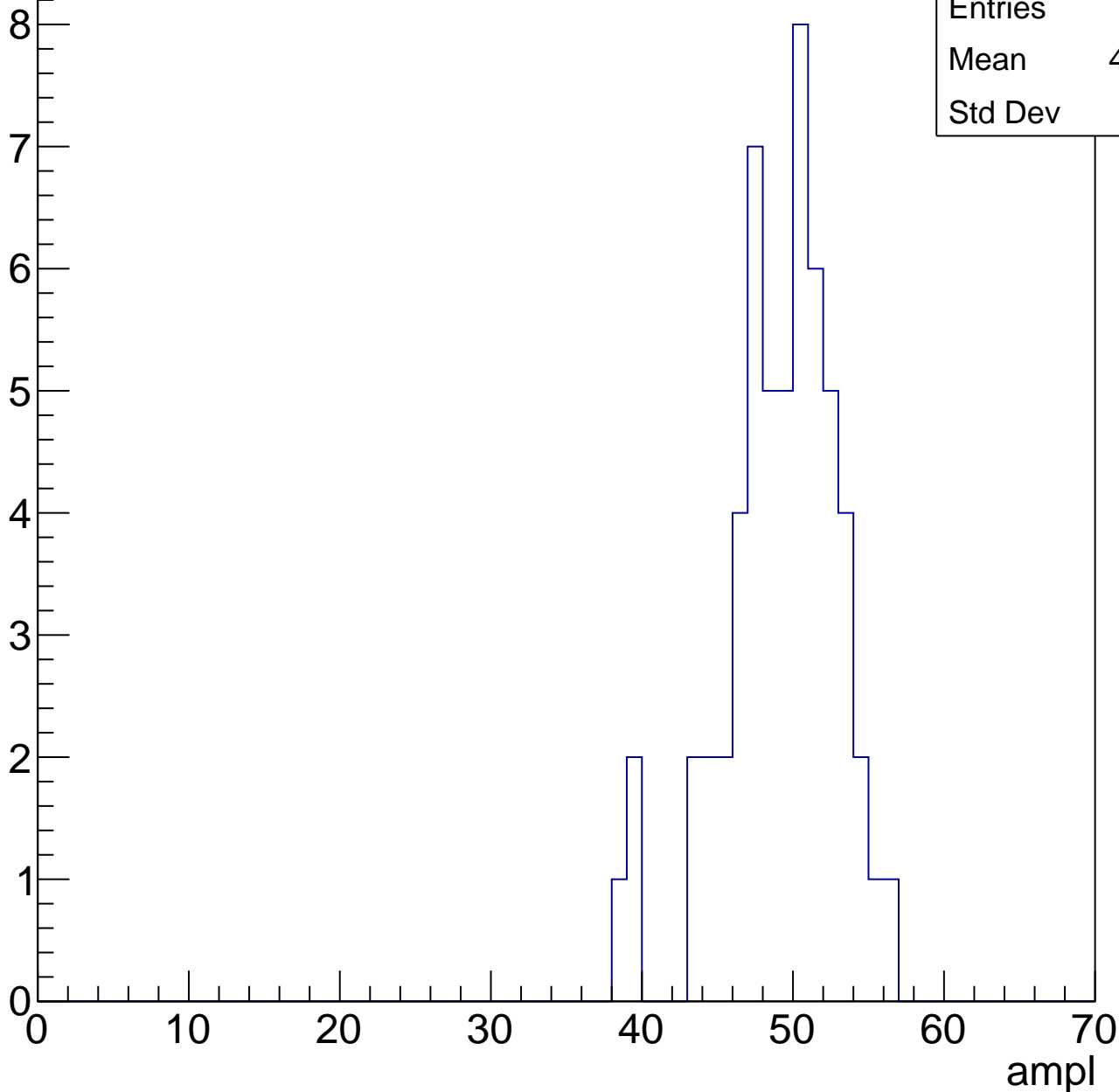


# B1L101S, U3-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

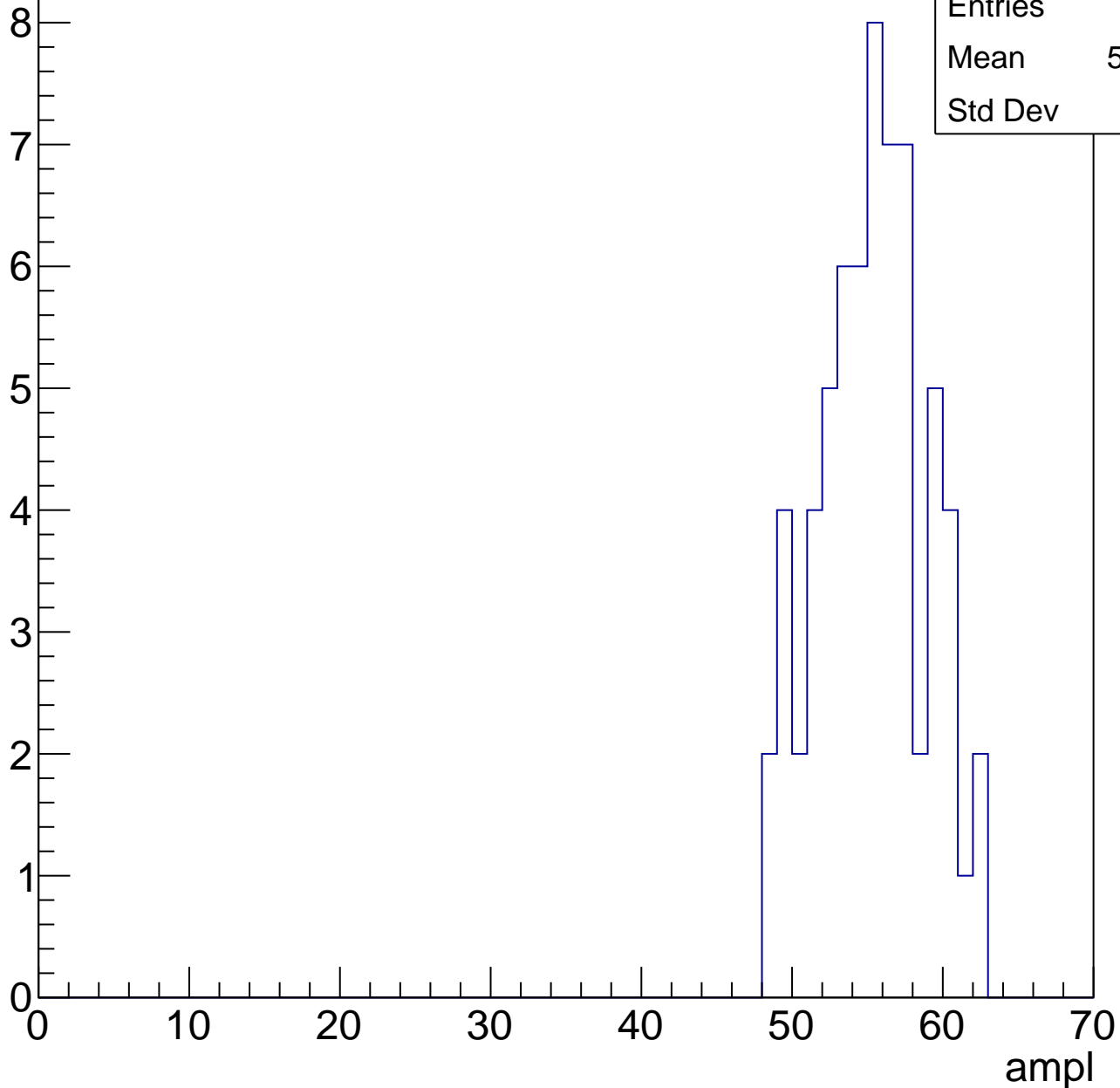
Entries	57
Mean	48.68
Std Dev	3.78



# B1L101S, U3-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

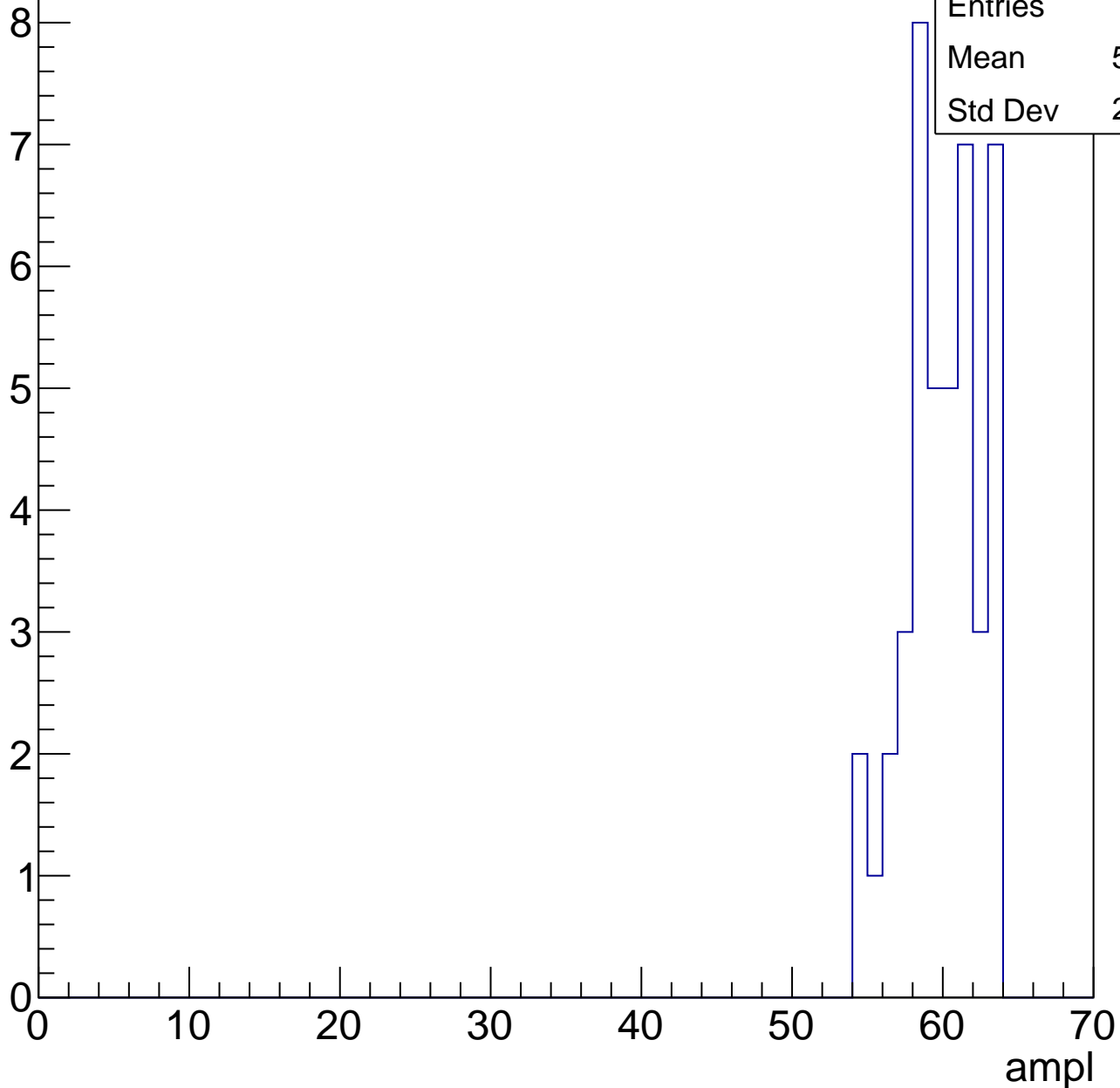
Entry



# B1L101S, U3-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



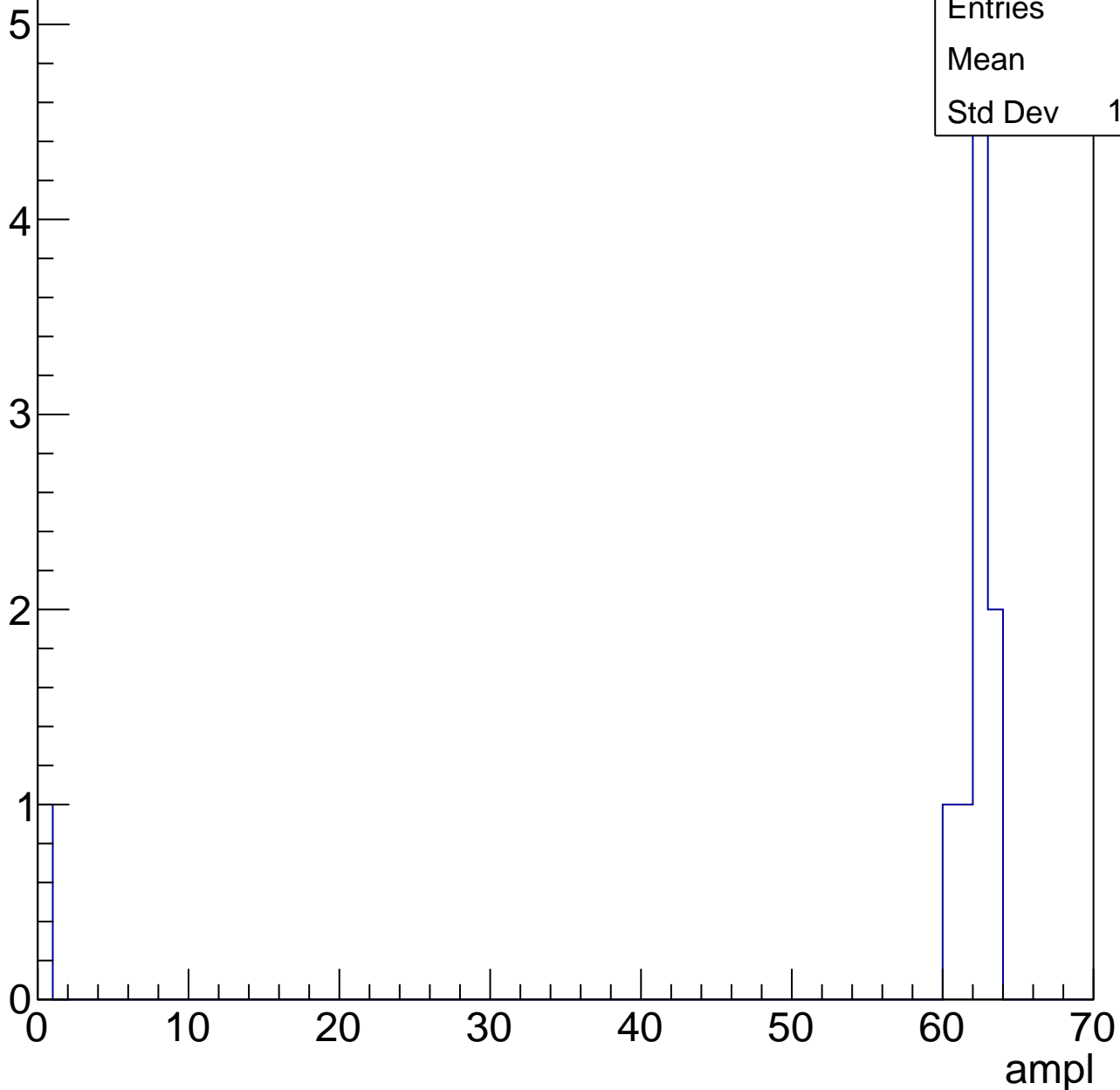
Entries	43
Mean	59.51
Std Dev	2.481

# B1L101S, U3-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	10
Mean	55.7
Std Dev	18.59





# B1L101S, U3-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch1, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	86
Mean	30.29
Std Dev	5.89

**Gaus mean : 31.2260**

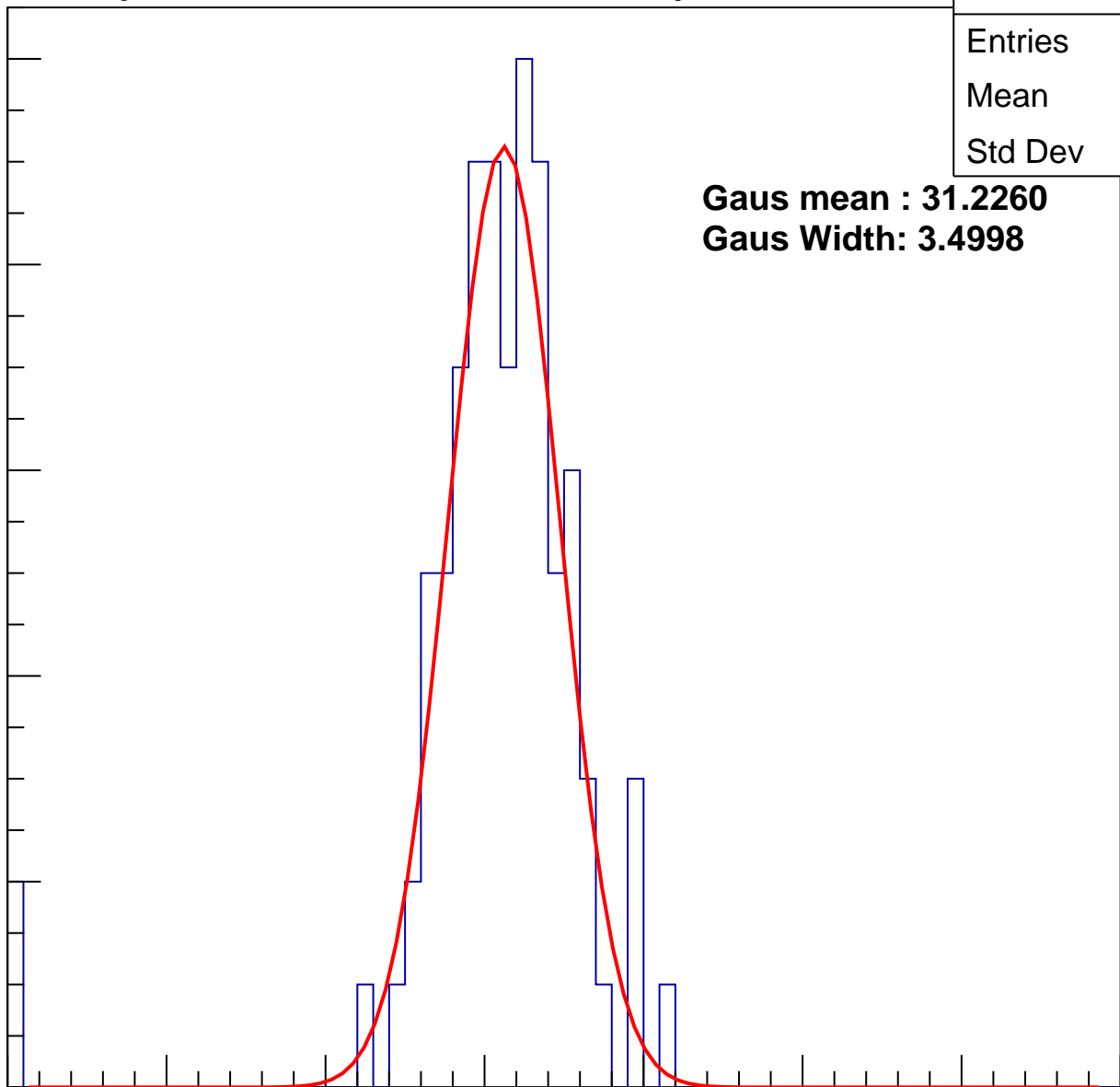
**Gaus Width: 3.4998**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U3-ch1, adc1

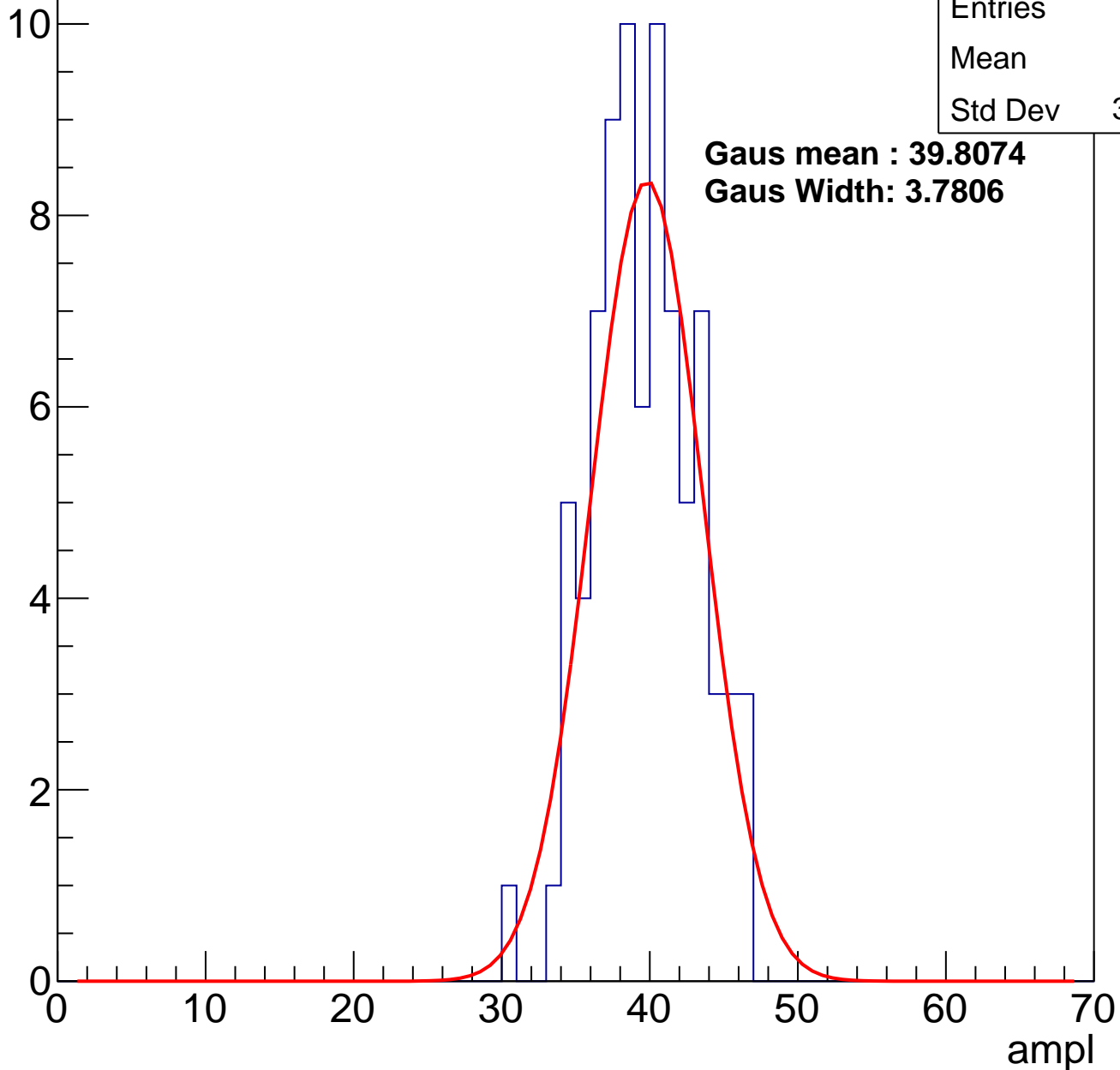
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	81
Mean	39.2
Std Dev	3.401

**Gaus mean : 39.8074**

**Gaus Width: 3.7806**

Entry



# B1L101S, U3-ch1, adc2

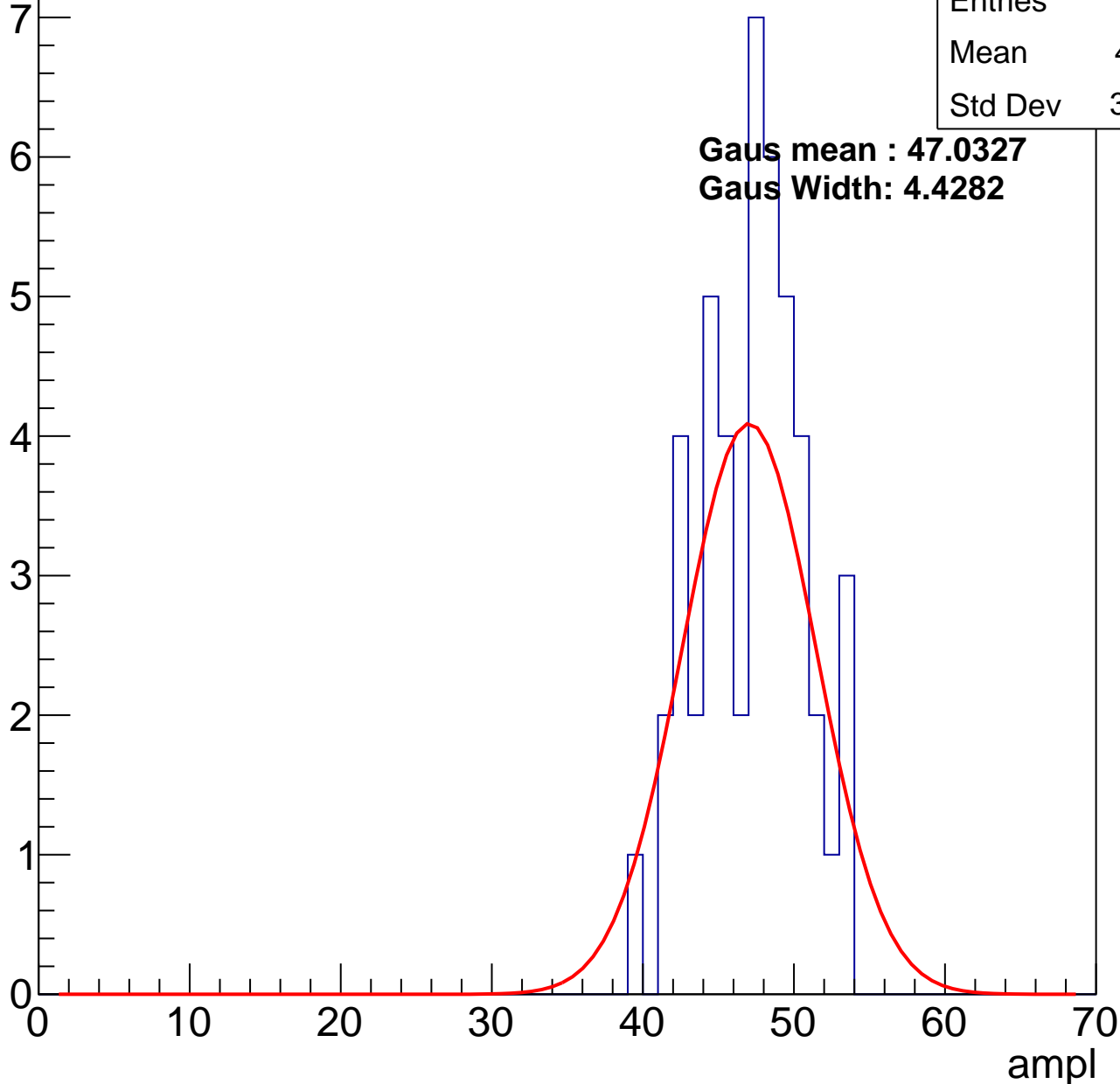
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	46.71
Std Dev	3.397

**Gaus mean : 47.0327**

**Gaus Width: 4.4282**

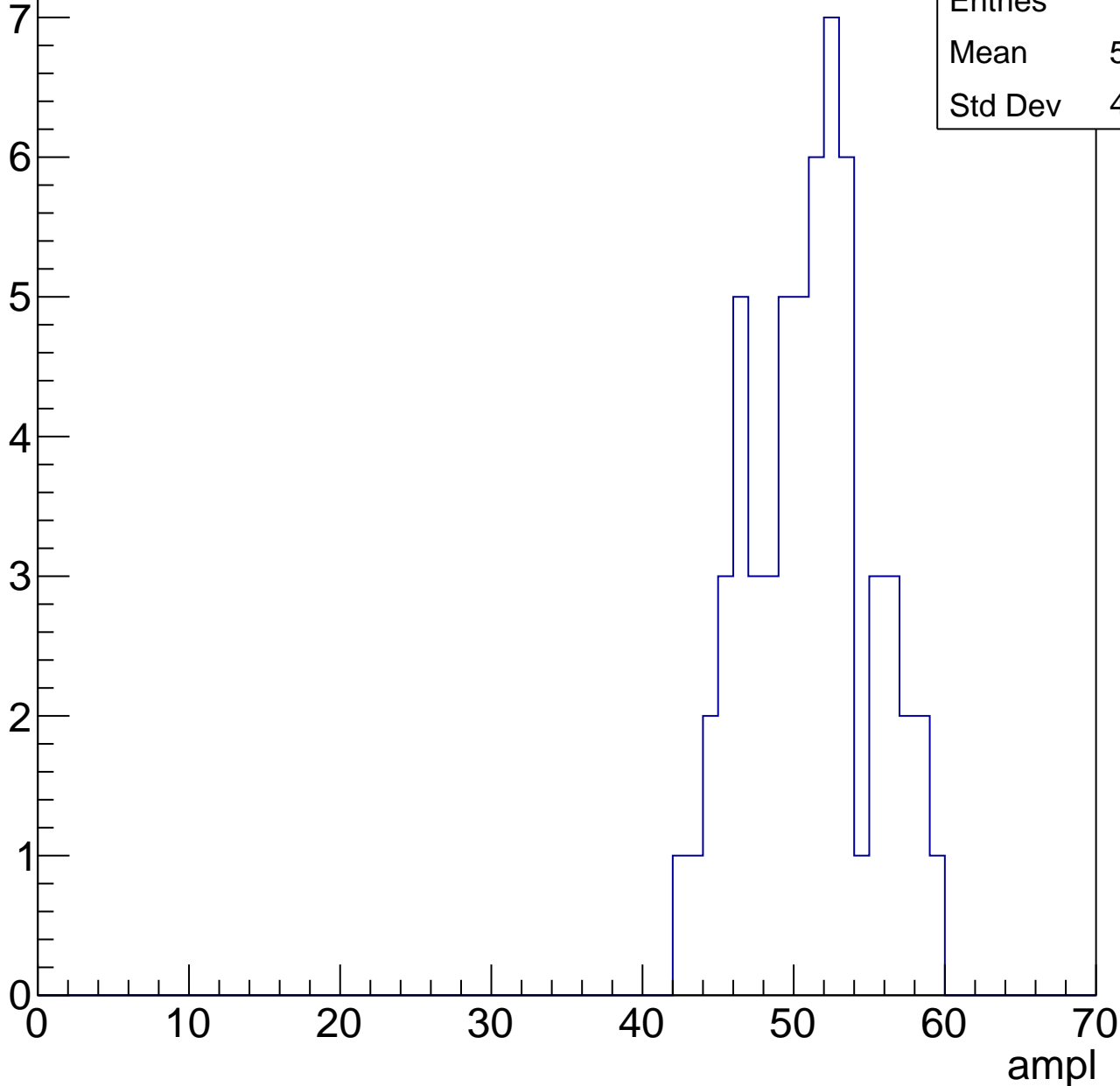


# B1L101S, U3-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	50.54
Std Dev	4.035

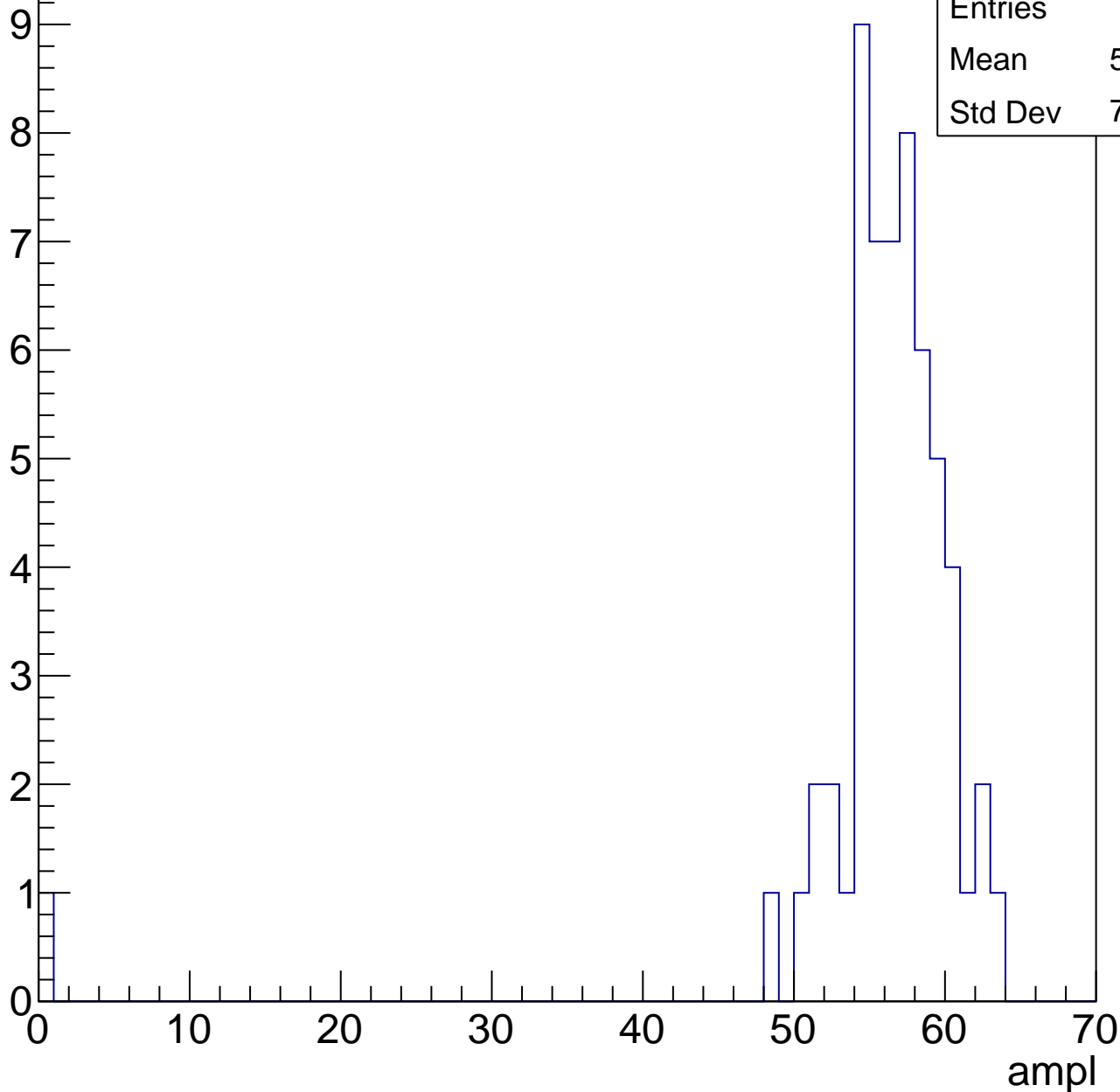


# B1L101S, U3-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

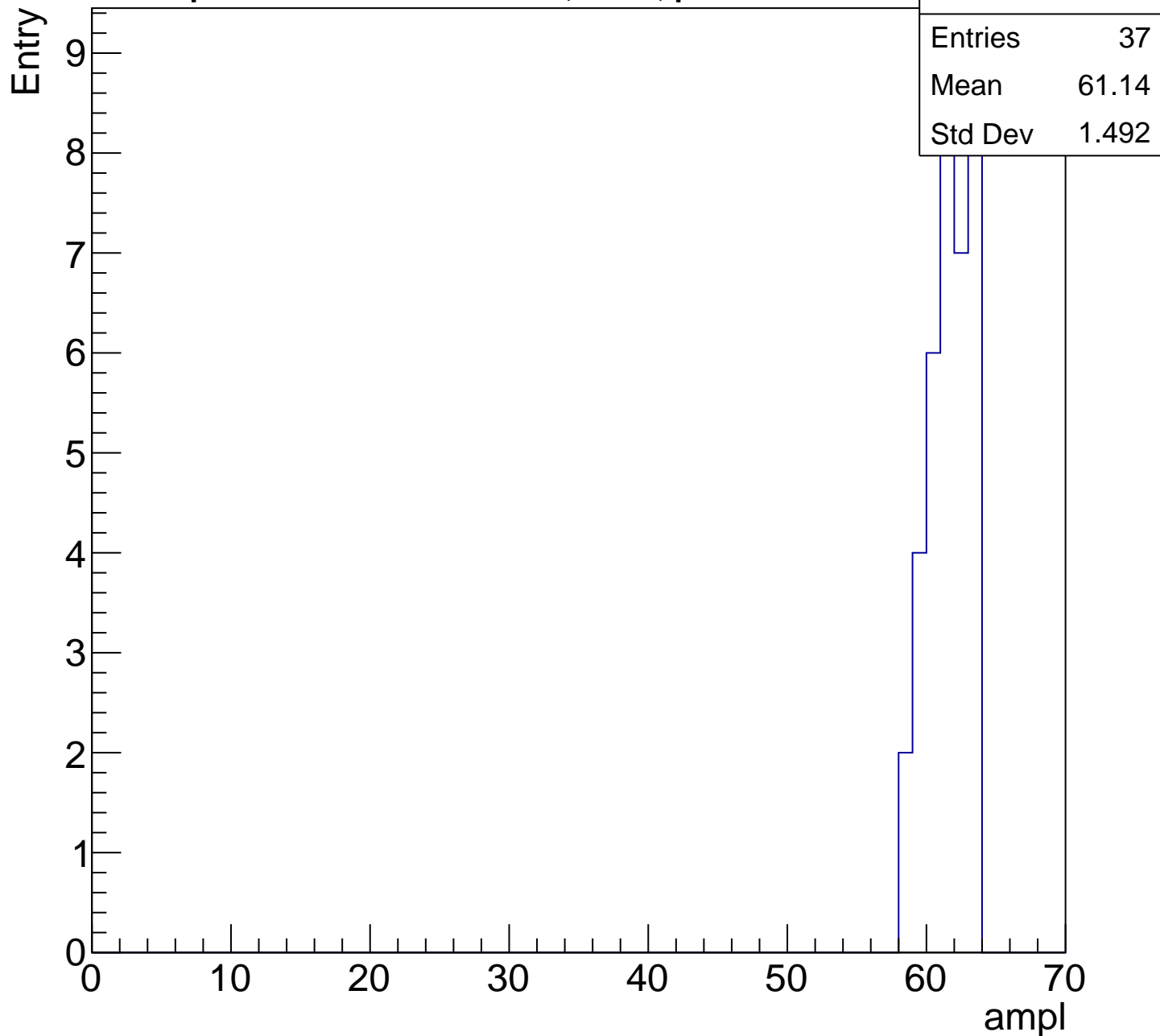
Entry

Entries	58
Mean	55.29
Std Dev	7.909



# B1L101S, U3-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U3-ch2, adc0

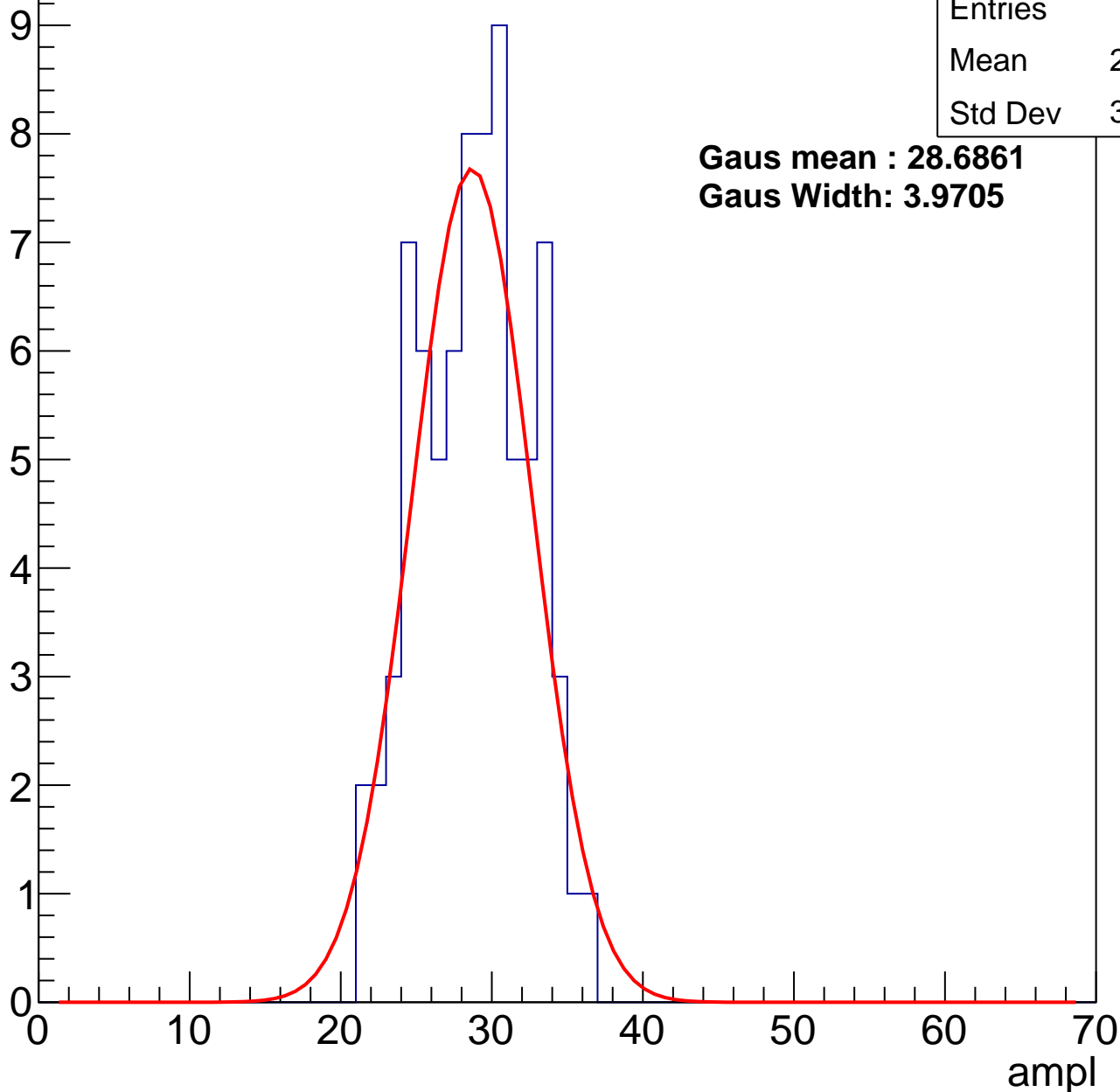
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	28.33
Std Dev	3.569

**Gaus mean : 28.6861**

**Gaus Width: 3.9705**



# B1L101S, U3-ch2, adc1

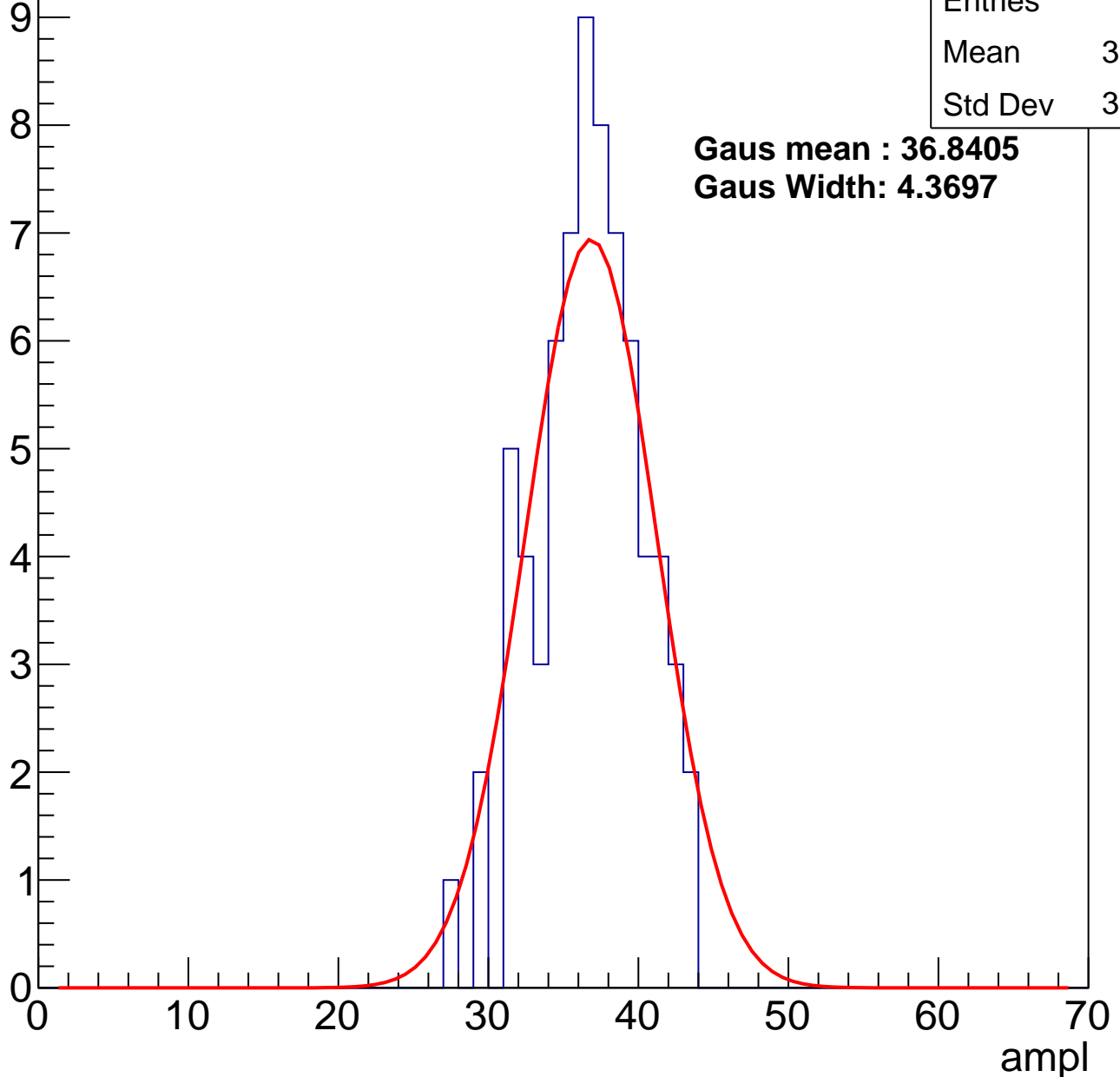
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	36.23
Std Dev	3.525

**Gaus mean : 36.8405**

**Gaus Width: 4.3697**



# B1L101S, U3-ch2, adc2

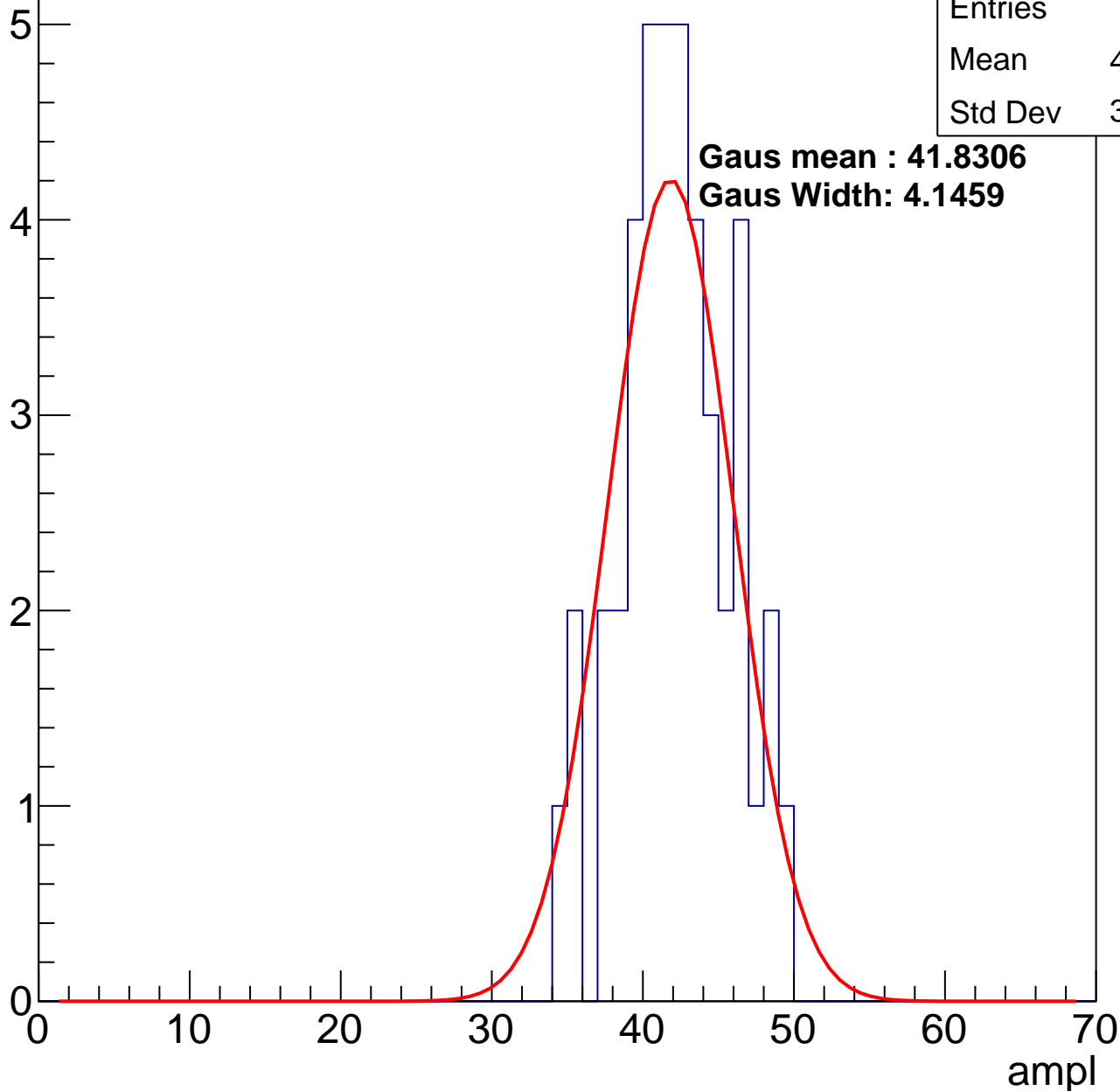
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	41.74
Std Dev	3.564

**Gaus mean : 41.8306**

**Gaus Width: 4.1459**

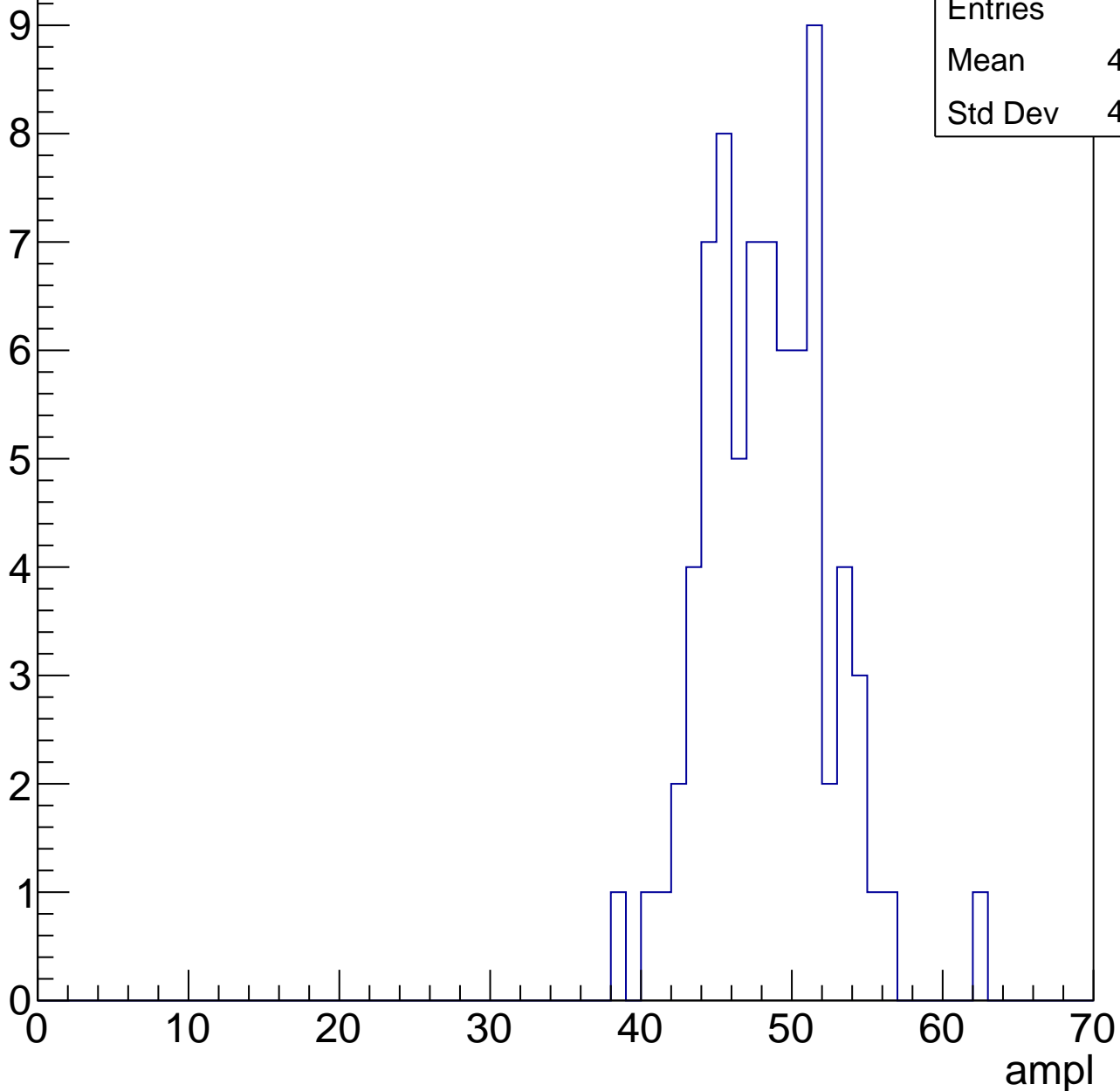


# B1L101S, U3-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	47.92
Std Dev	4.064

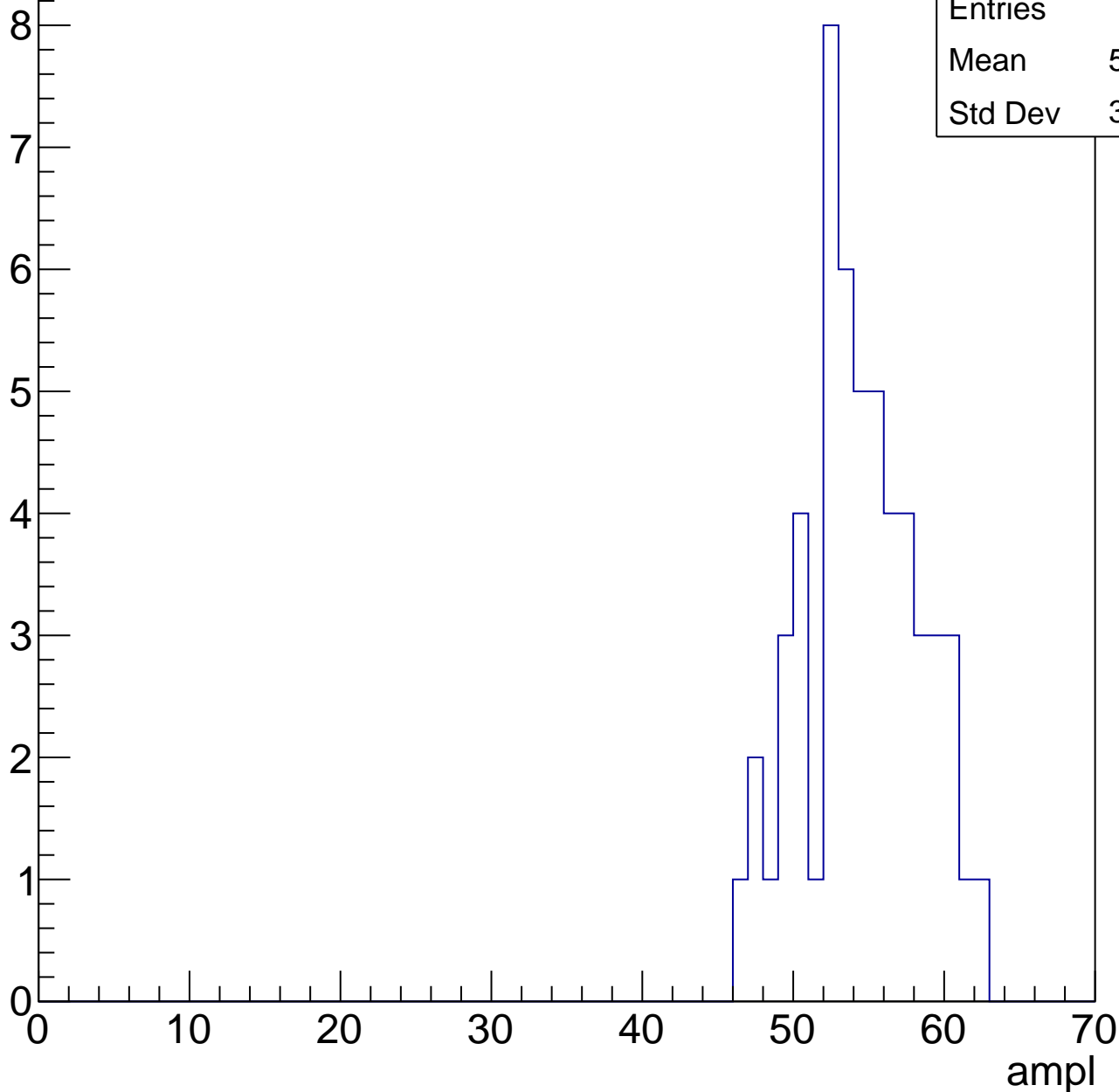


# B1L101S, U3-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	54.02
Std Dev	3.778

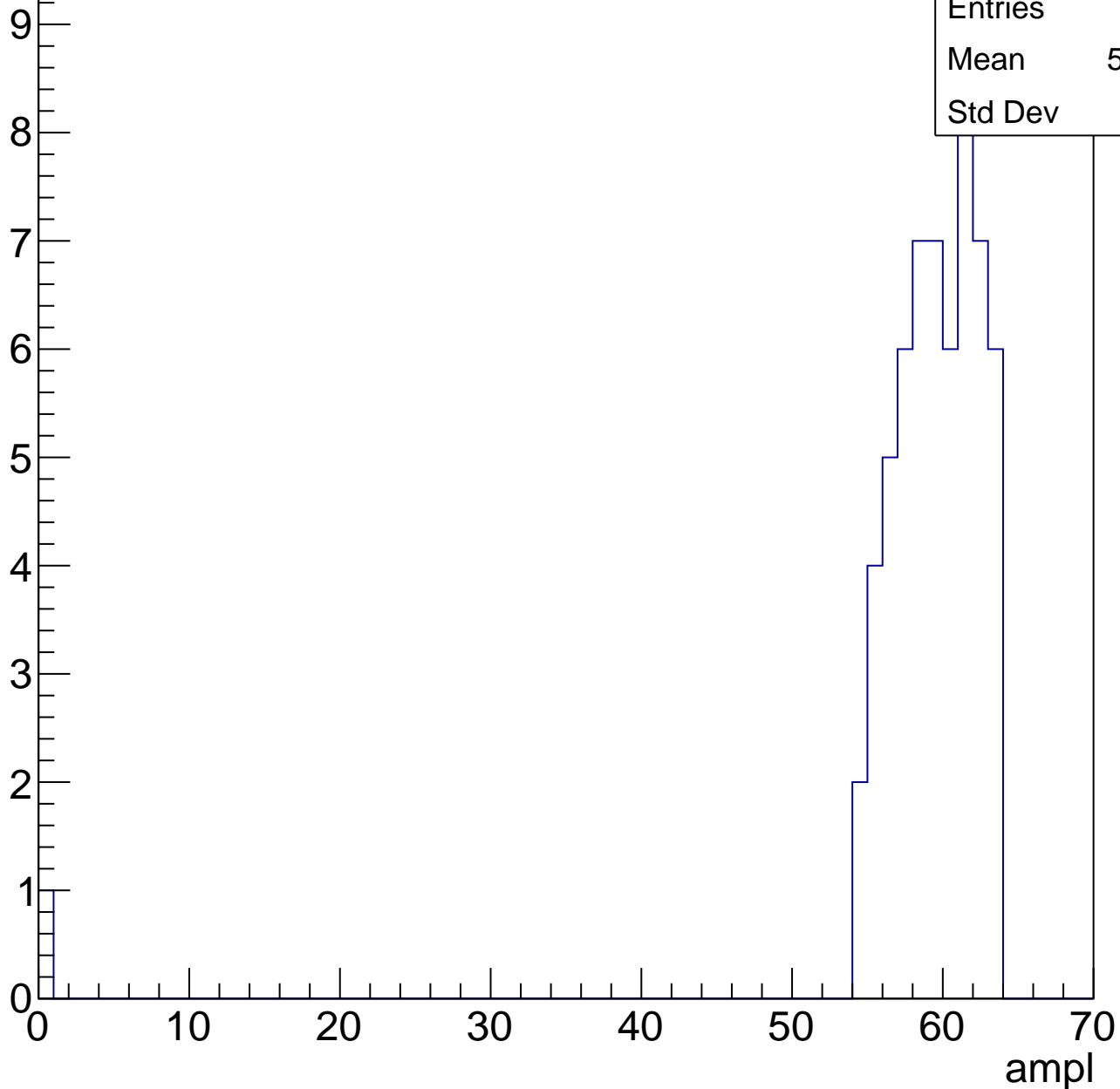


# B1L101S, U3-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

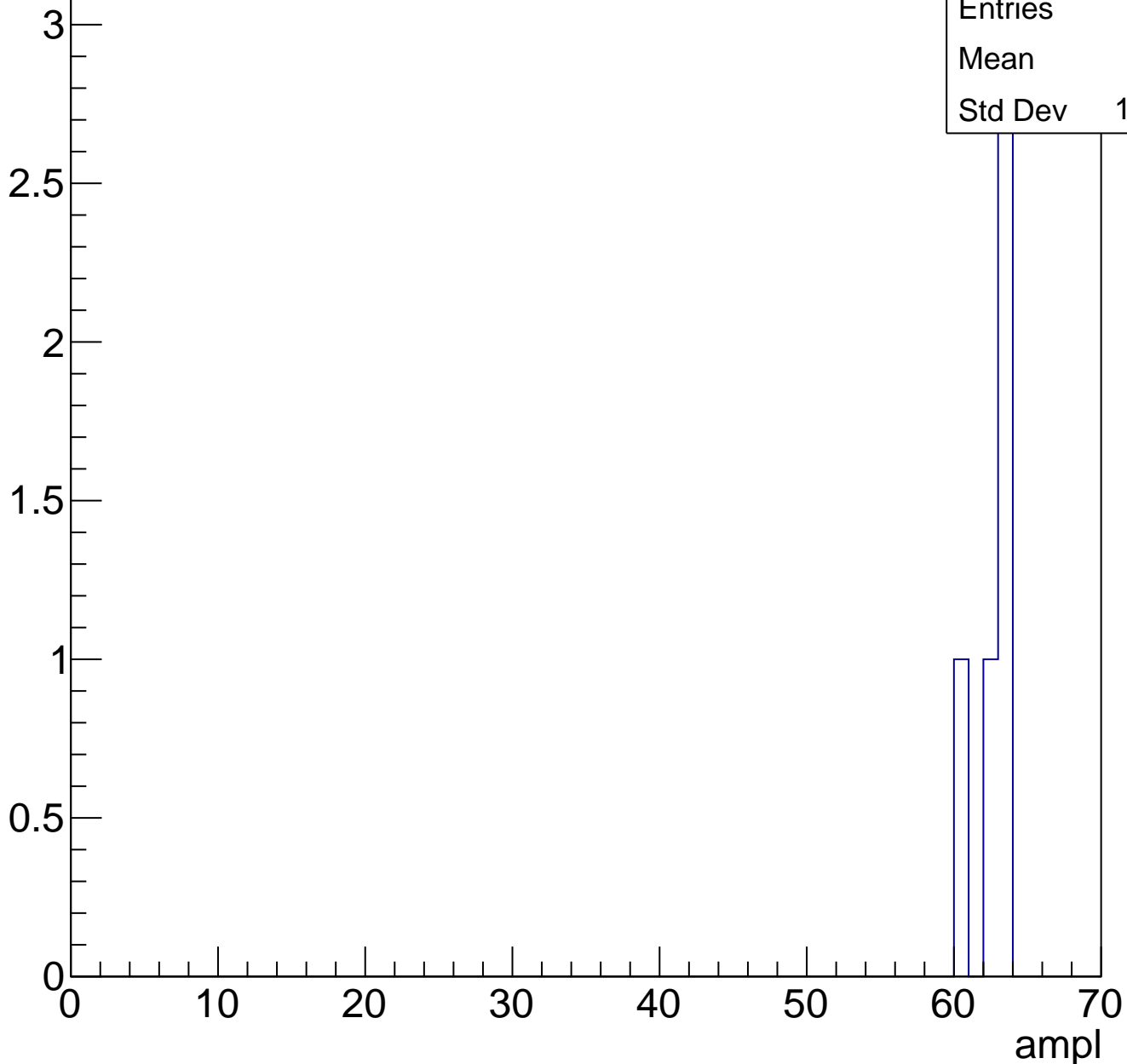
Entries	60
Mean	58.17
Std Dev	7.99



# B1L101S, U3-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	5
Mean	62.2
Std Dev	1.166



# B1L101S, U3-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch3, adc0

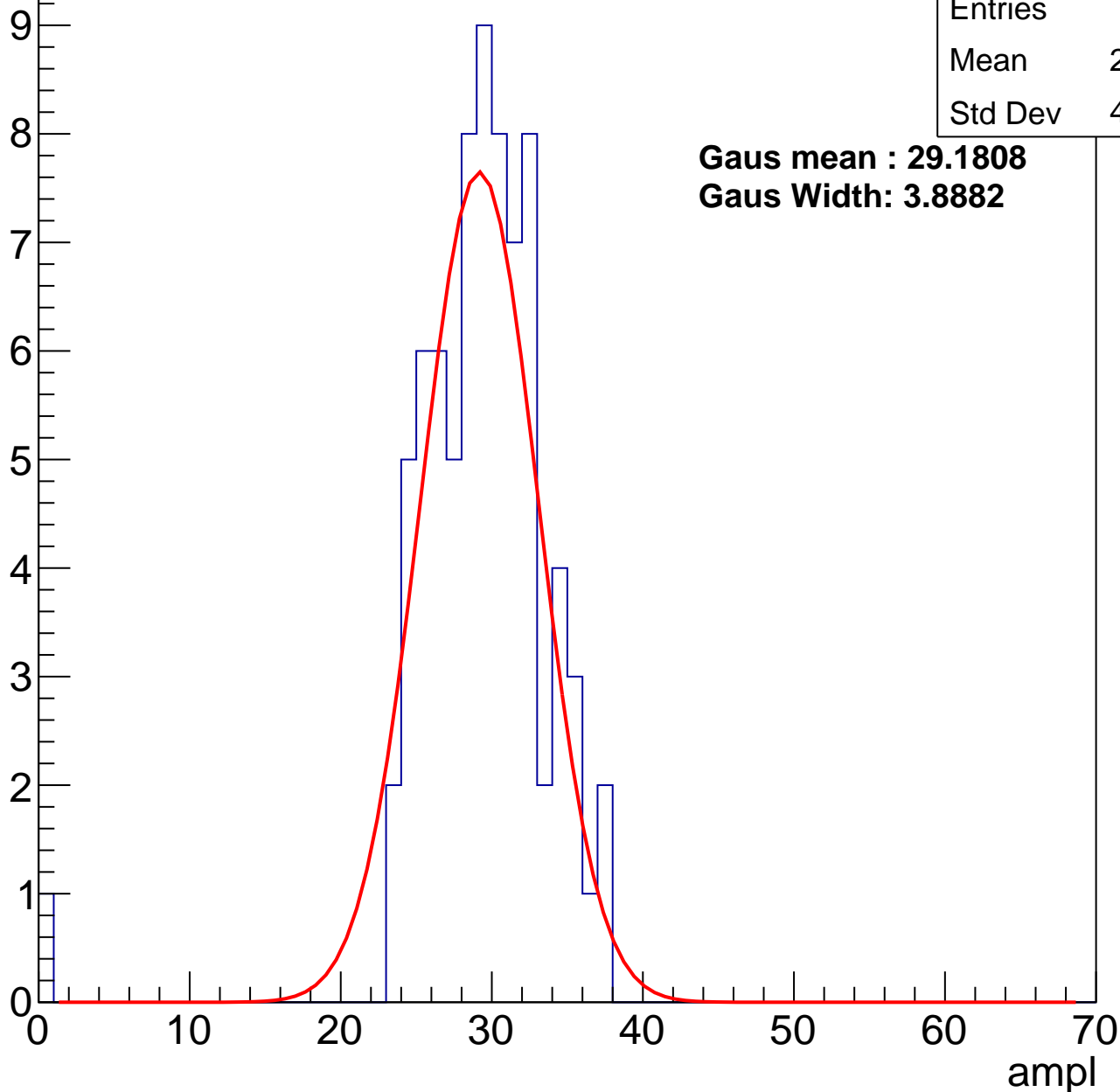
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	28.86
Std Dev	4.753

**Gaus mean : 29.1808**

**Gaus Width: 3.8882**



# B1L101S, U3-ch3, adc1

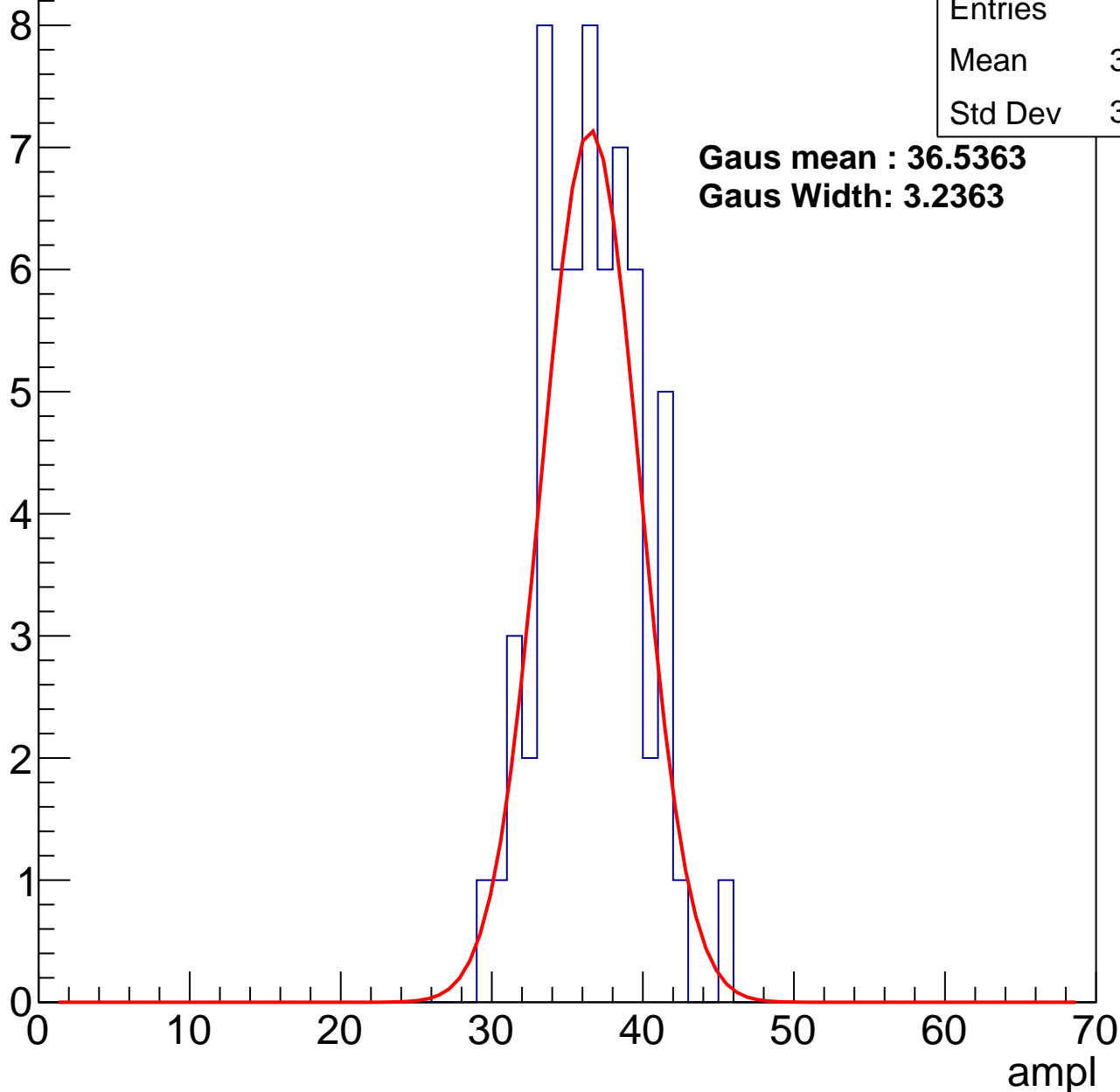
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	36.13
Std Dev	3.224

**Gaus mean : 36.5363**

**Gaus Width: 3.2363**



# B1L101S, U3-ch3, adc2

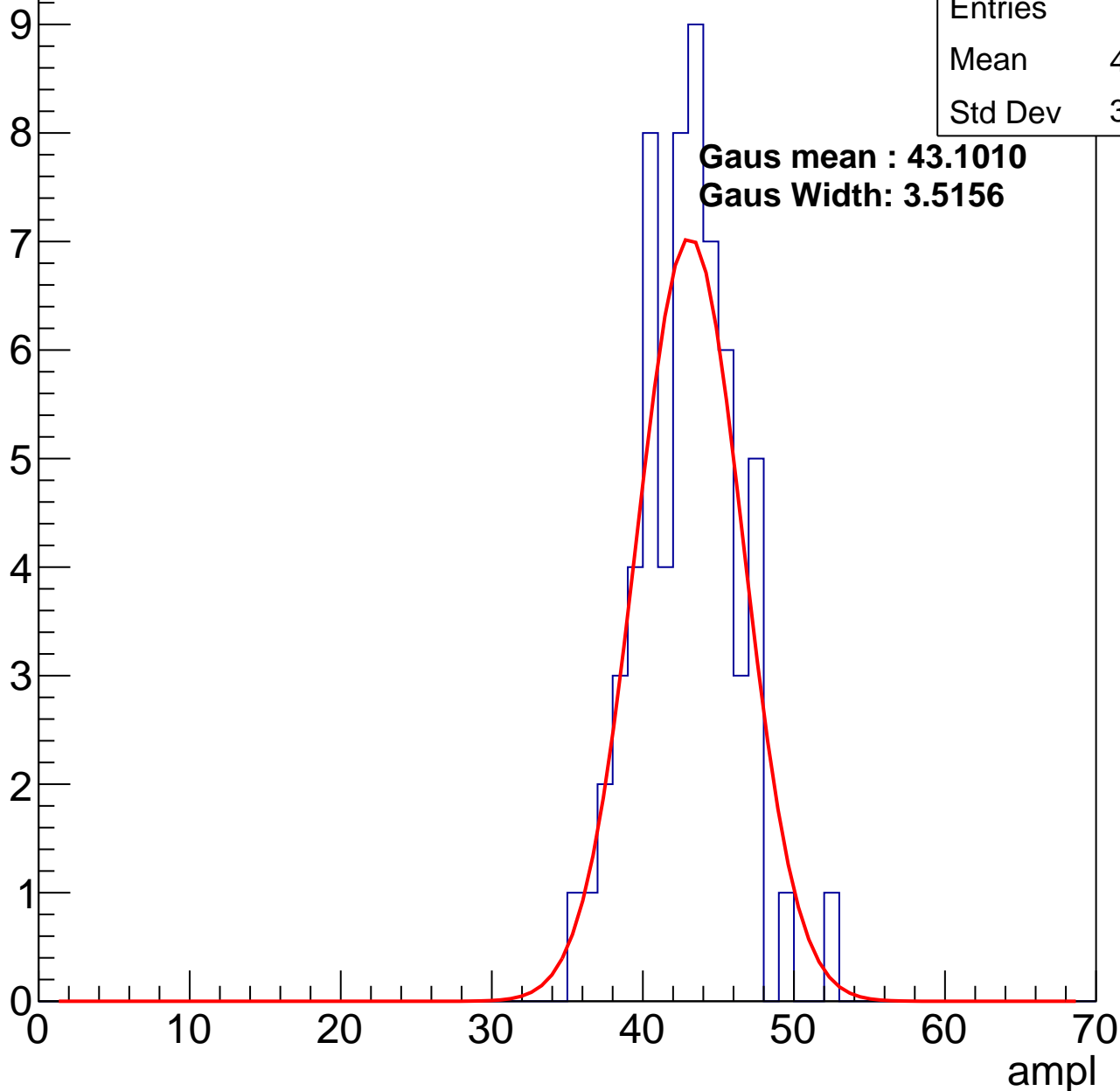
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	42.44
Std Dev	3.226

**Gaus mean : 43.1010**

**Gaus Width: 3.5156**

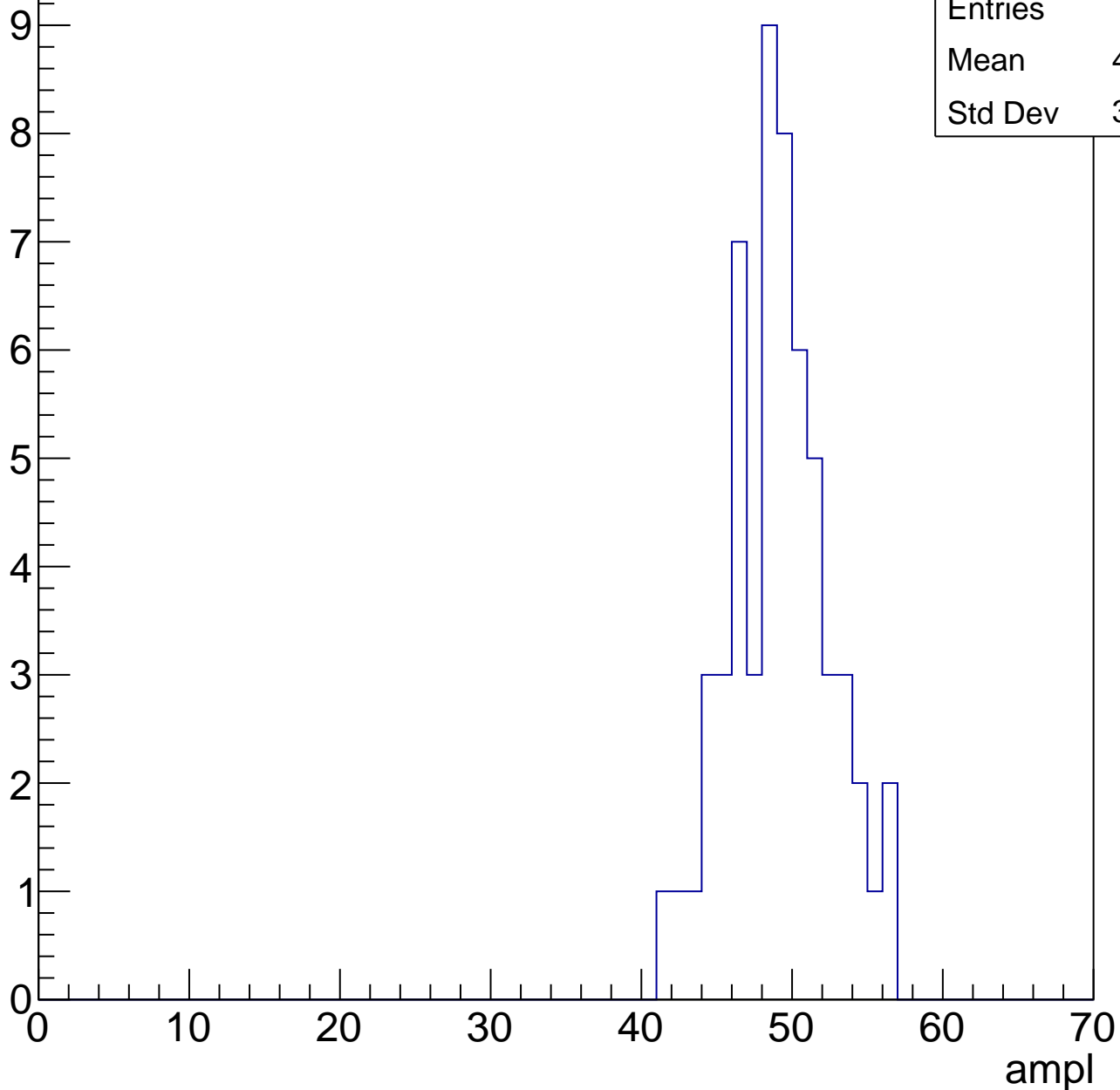


# B1L101S, U3-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

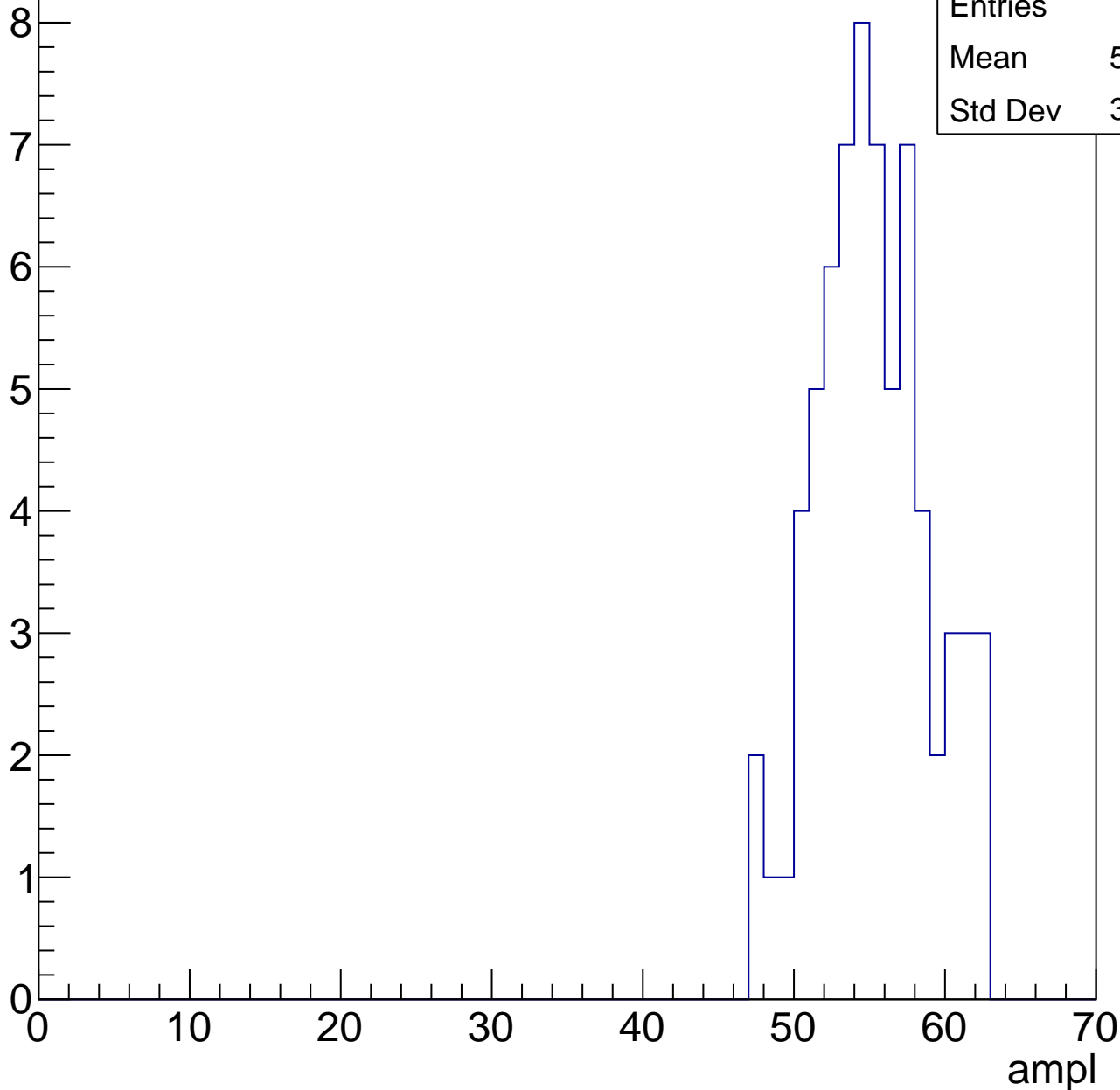
Entries	58
Mean	48.71
Std Dev	3.311



# B1L101S, U3-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

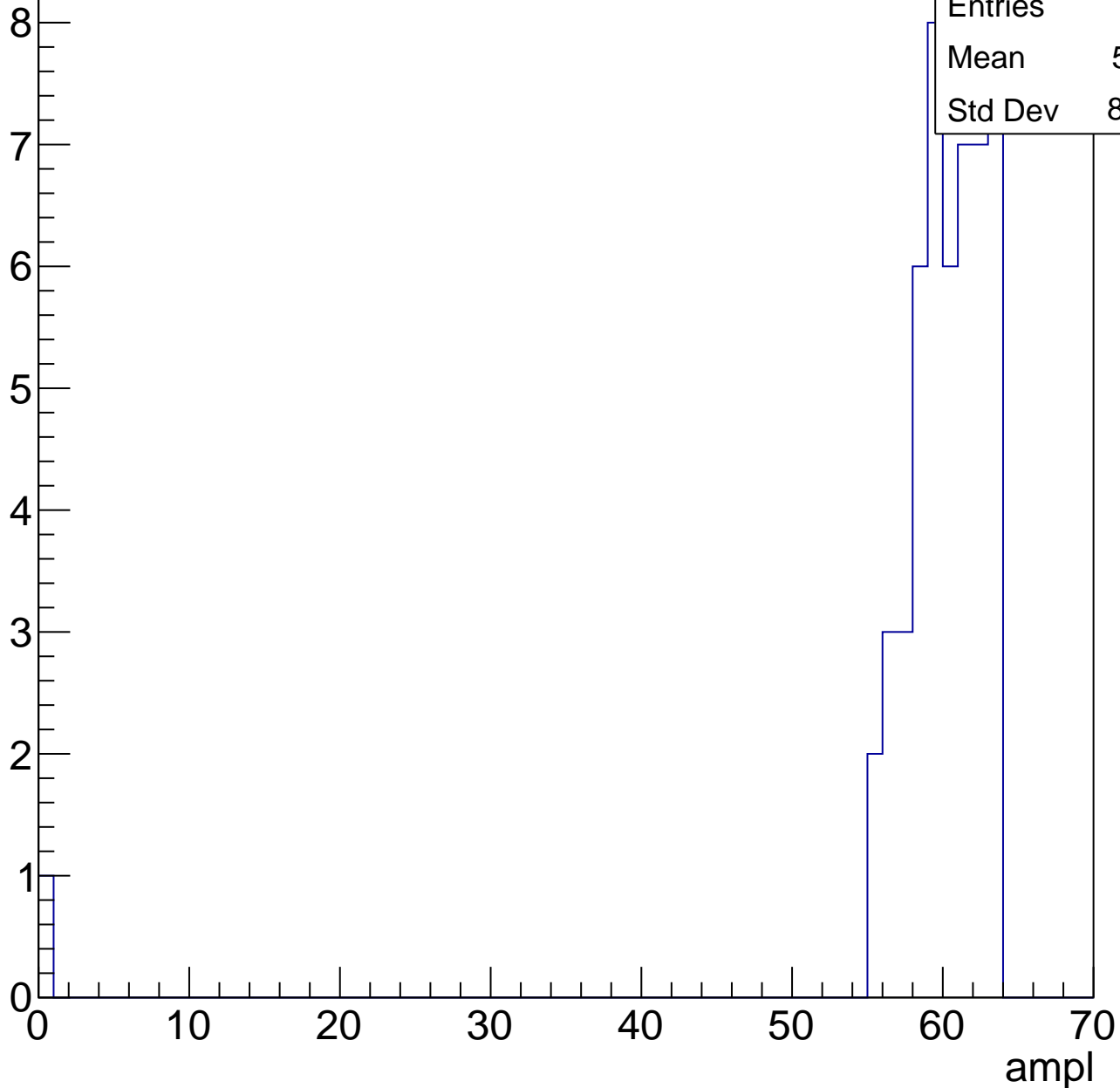


Entries	68
Mean	54.76
Std Dev	3.659

# B1L101S, U3-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch3, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U3-ch4, adc0

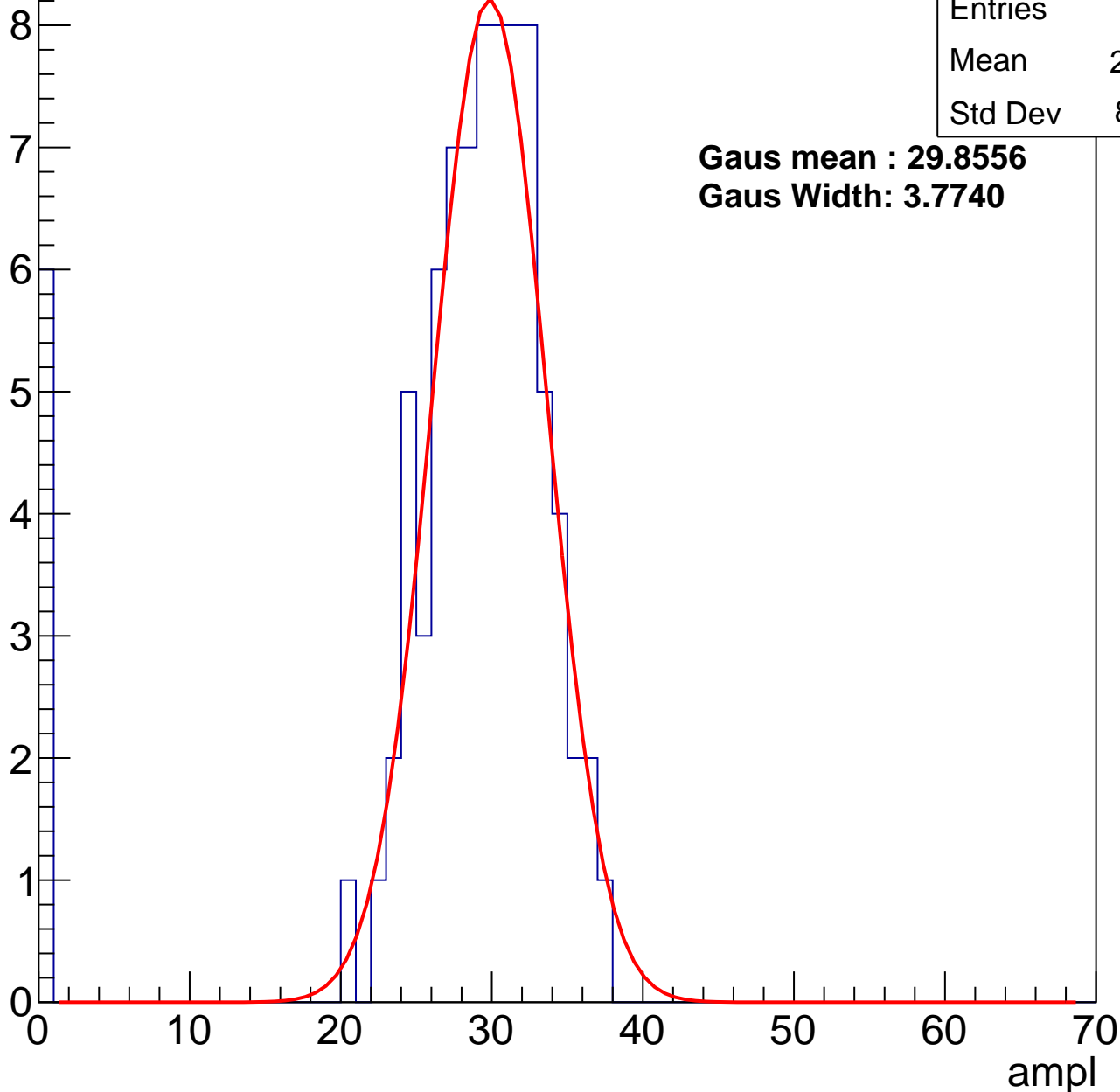
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	84
Mean	27.14
Std Dev	8.271

**Gaus mean : 29.8556**

**Gaus Width: 3.7740**



# B1L101S, U3-ch4, adc1

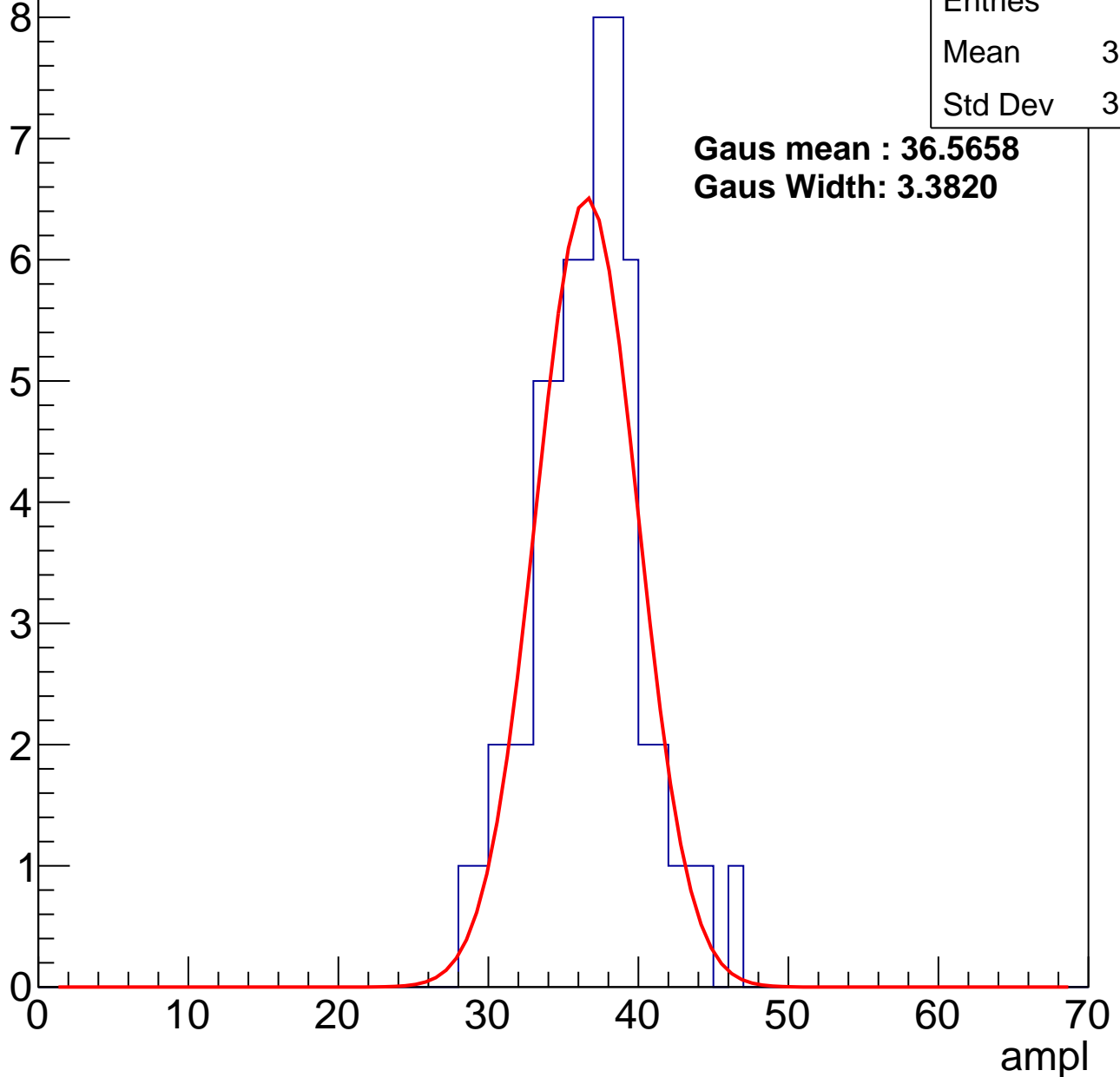
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	36.25
Std Dev	3.557

**Gaus mean : 36.5658**

**Gaus Width: 3.3820**



# B1L101S, U3-ch4, adc2

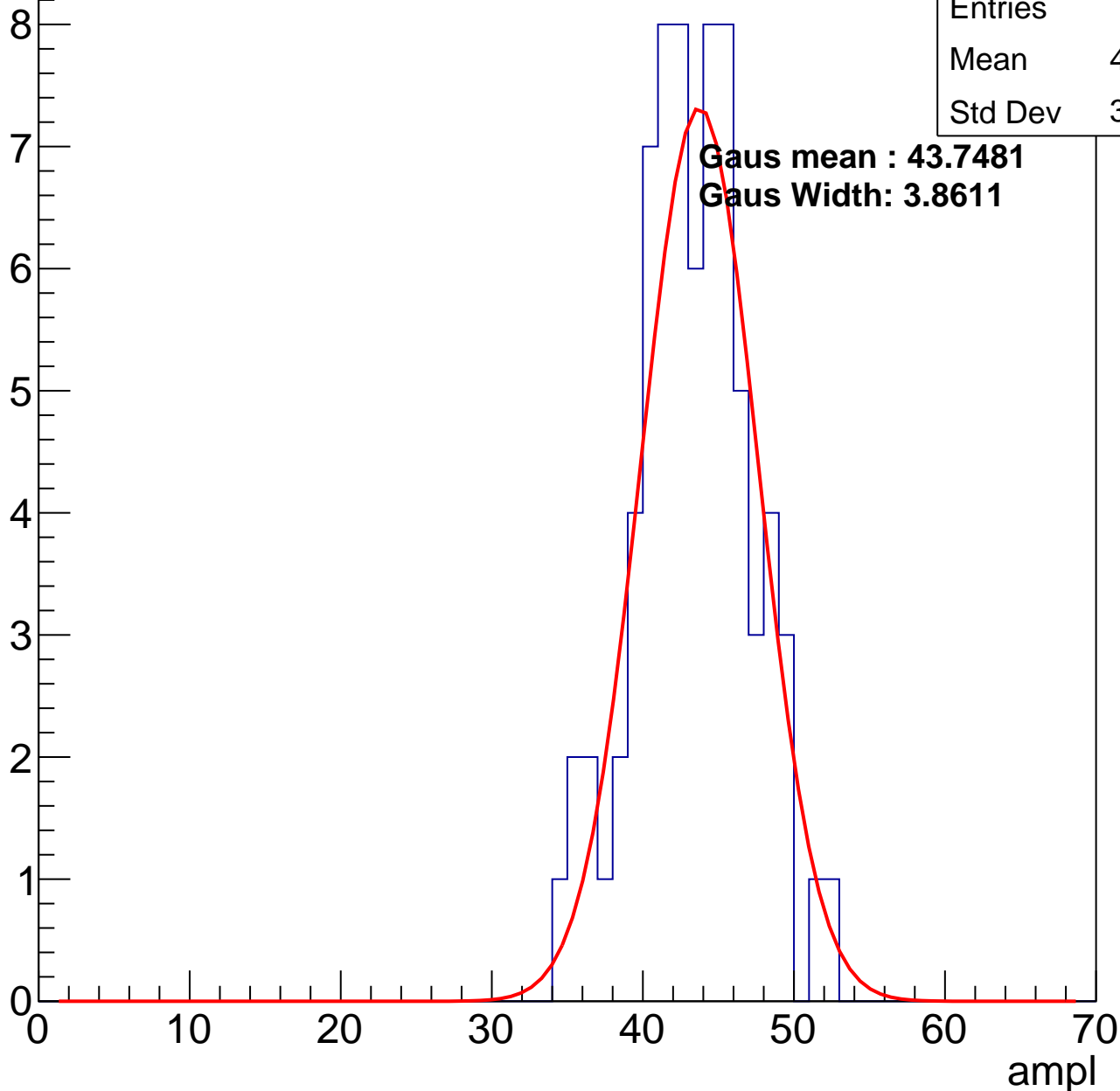
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	42.86
Std Dev	3.757

**Gaus mean : 43.7481**

**Gaus Width: 3.8611**

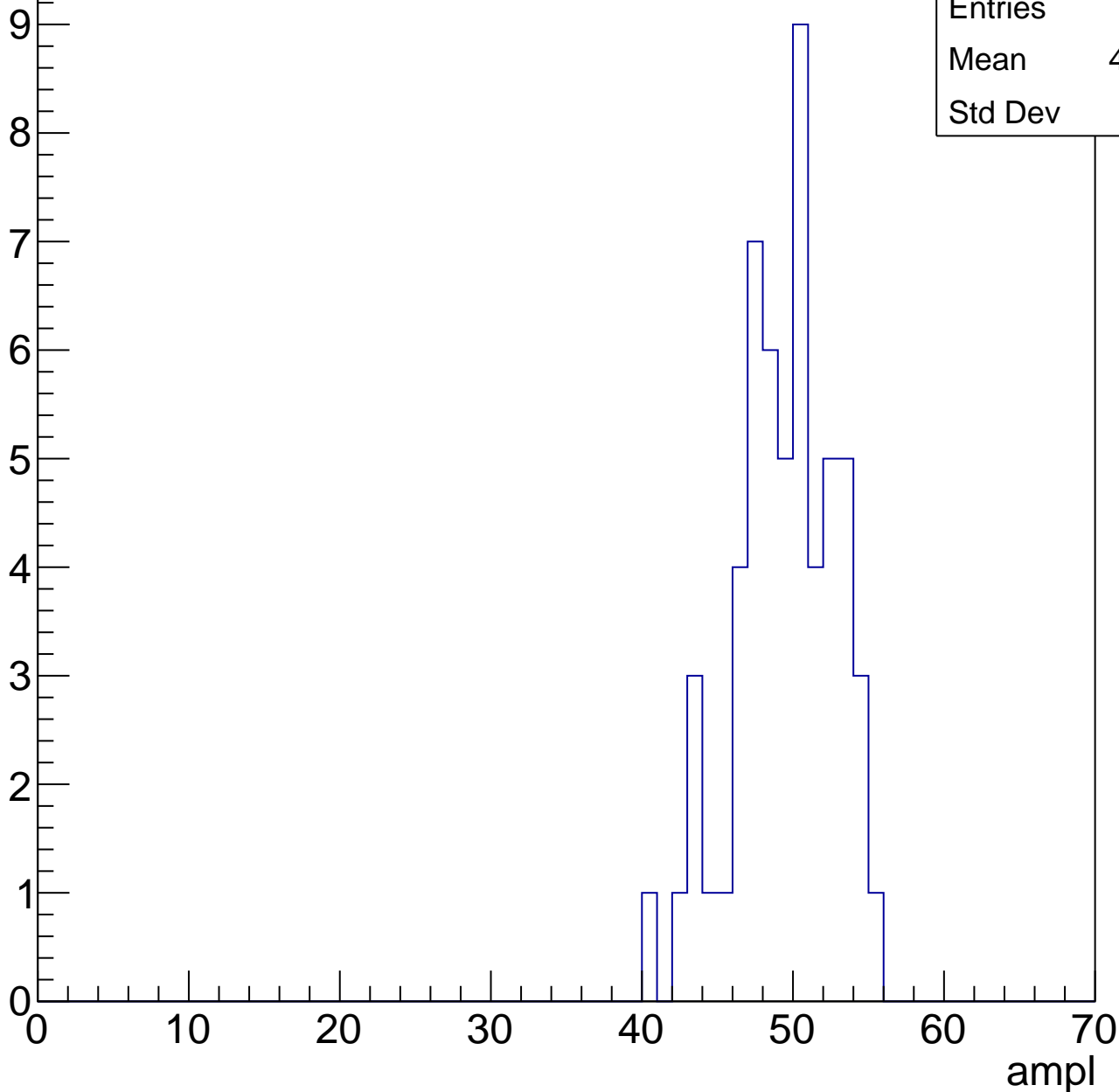


# B1L101S, U3-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

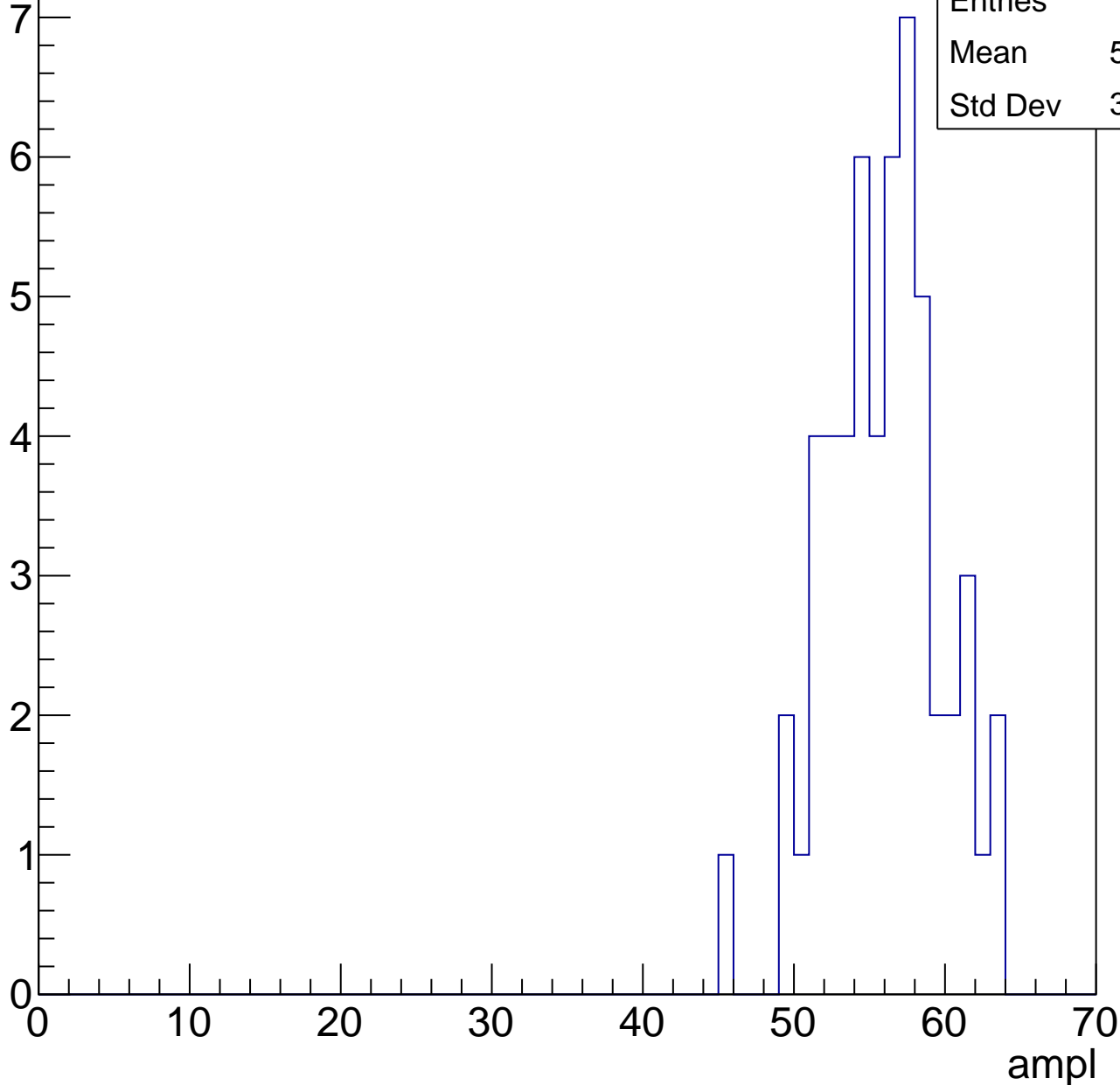
Entries	56
Mean	48.96
Std Dev	3.3



# B1L101S, U3-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

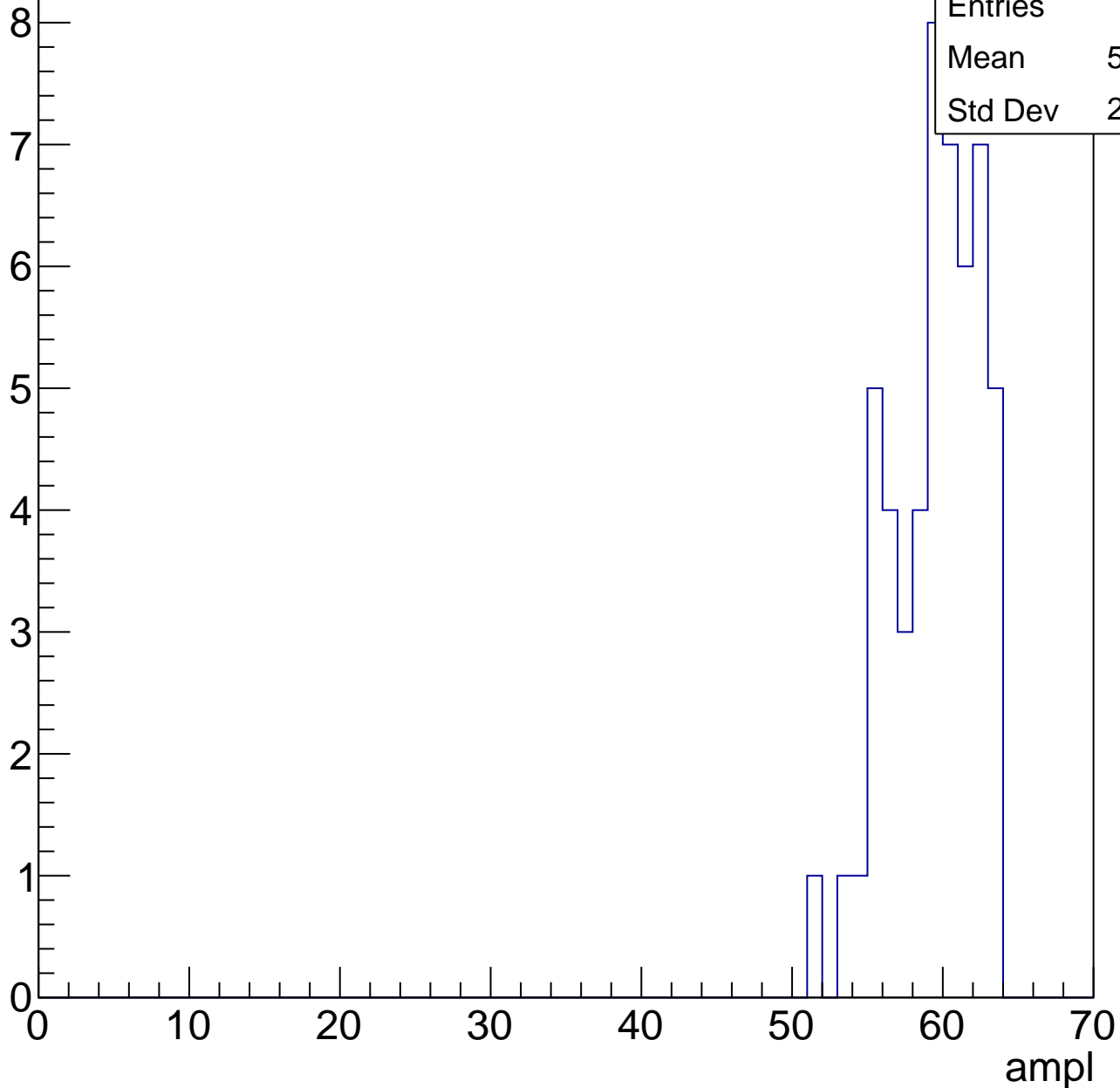


Entries	54
Mean	55.46
Std Dev	3.735

# B1L101S, U3-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

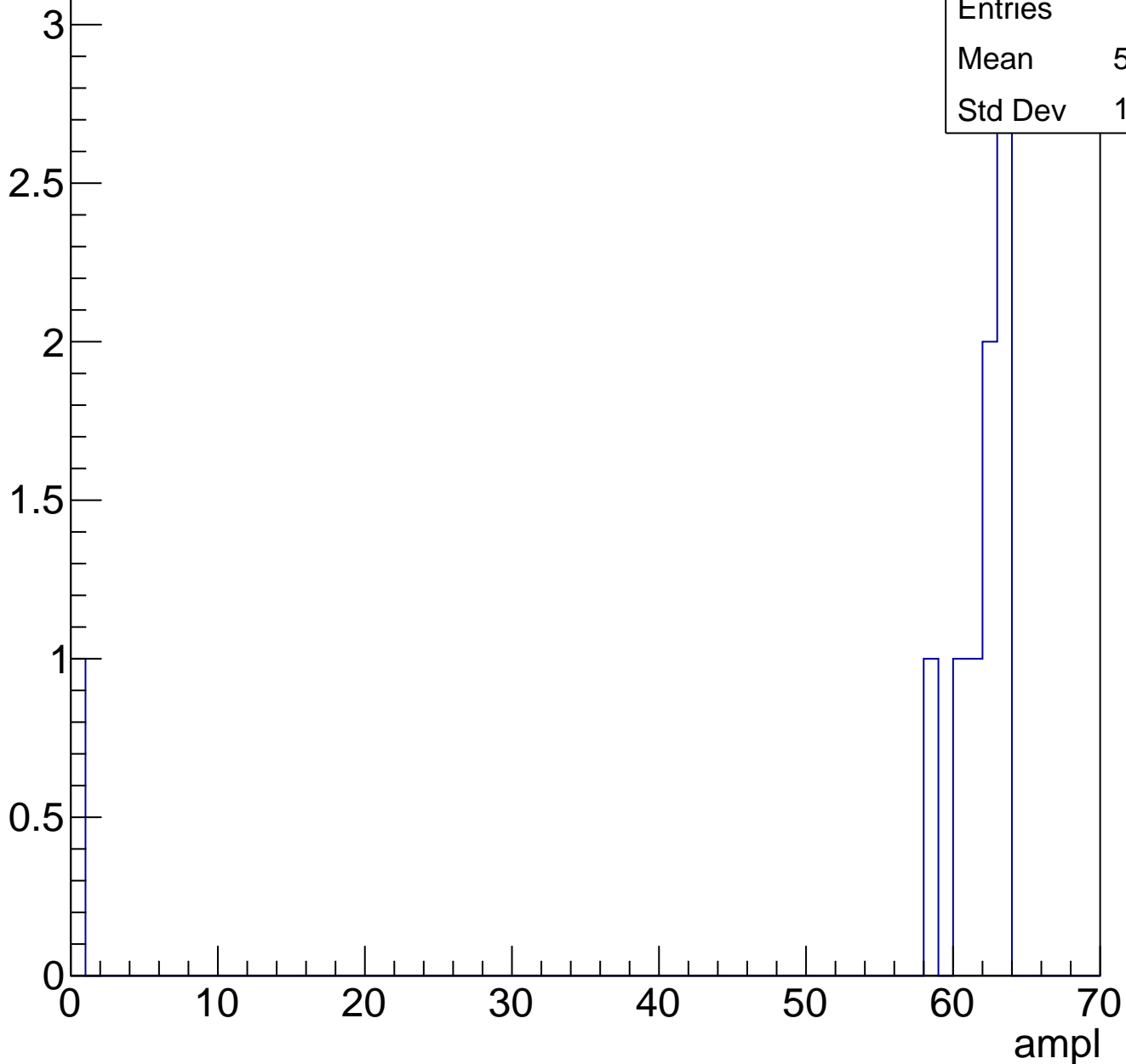
Entry



# B1L101S, U3-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

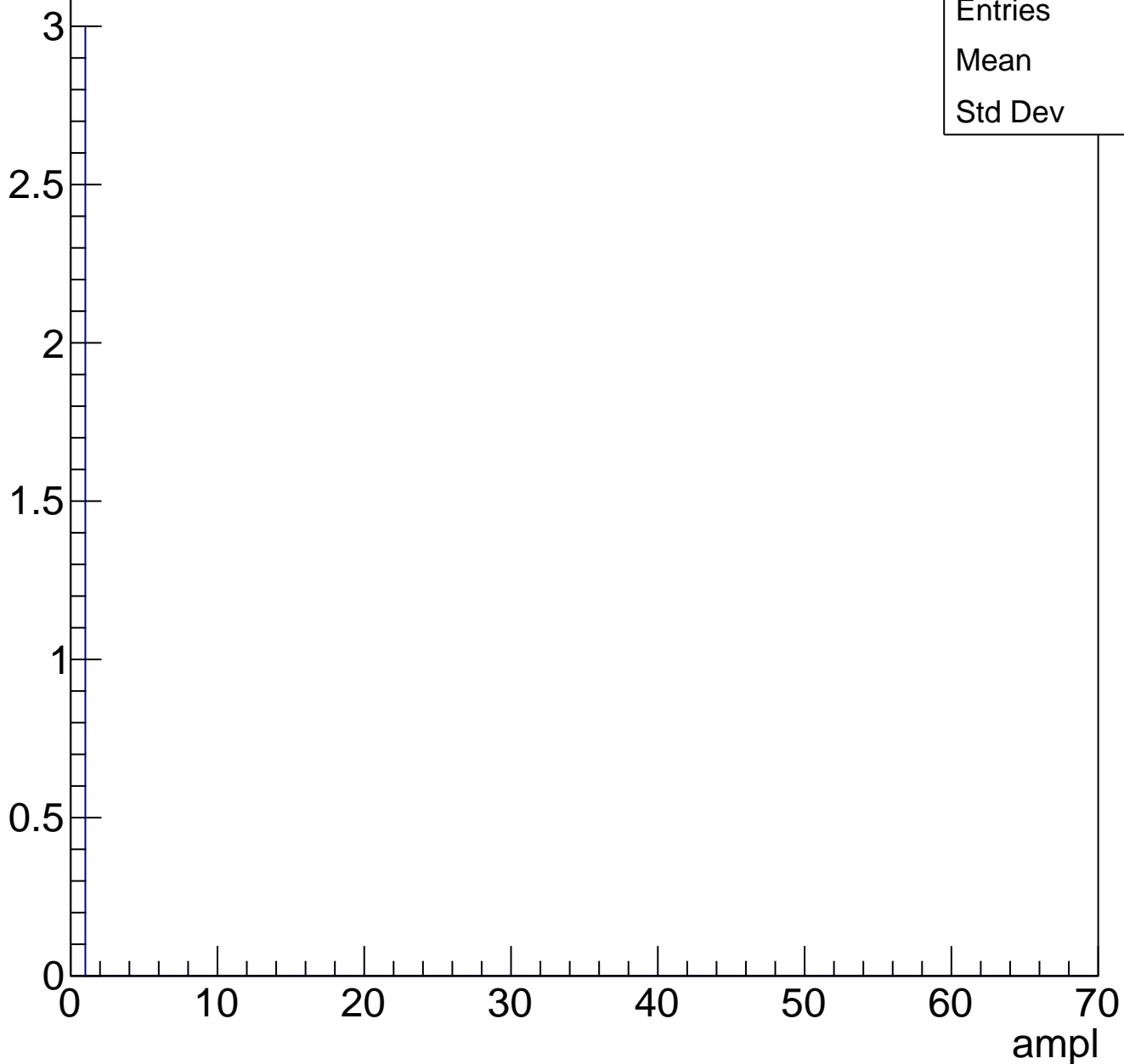




# B1L101S, U3-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U3-ch5, adc0

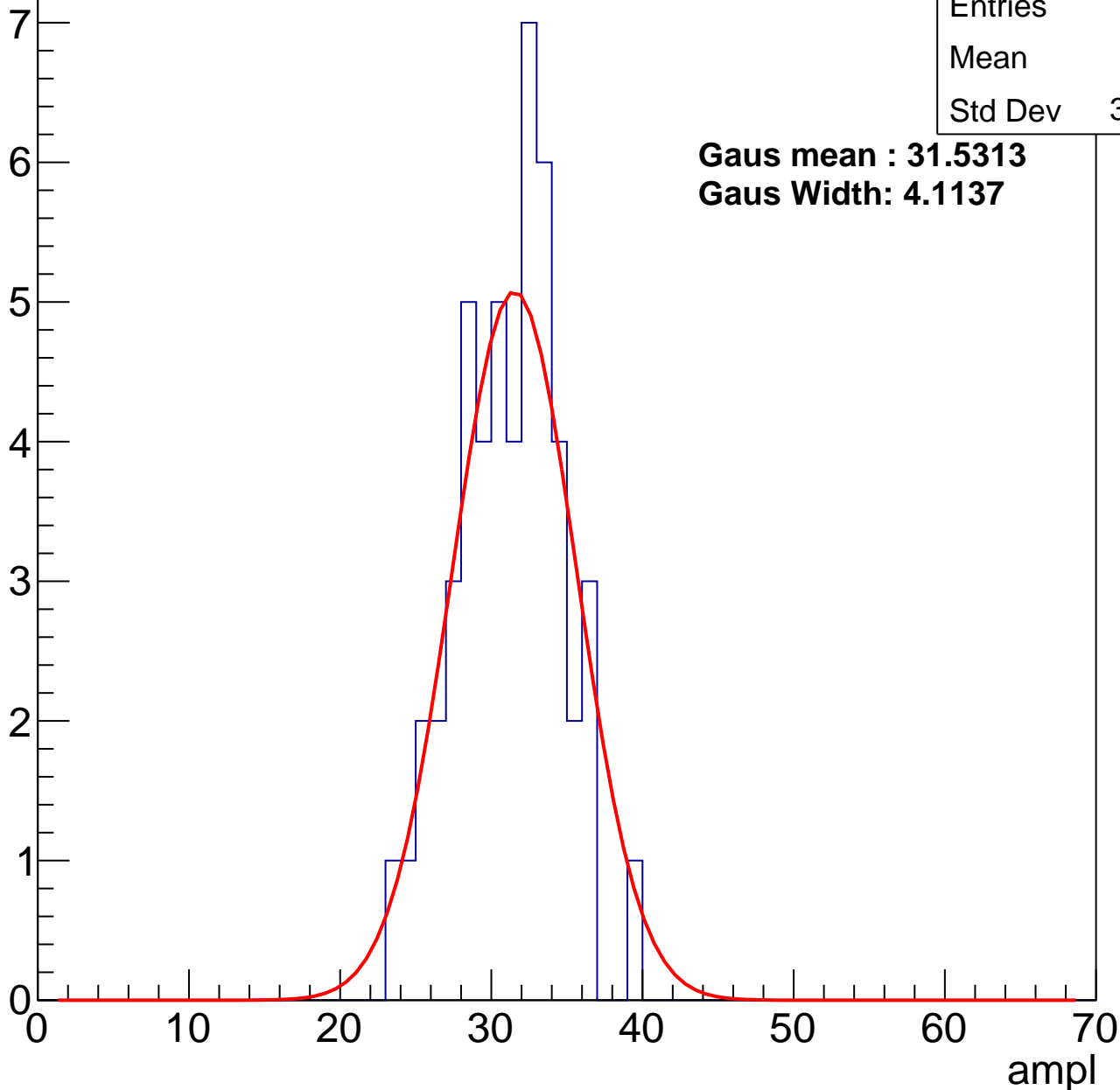
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	30.7
Std Dev	3.413

**Gaus mean : 31.5313**

**Gaus Width: 4.1137**



# B1L101S, U3-ch5, adc1

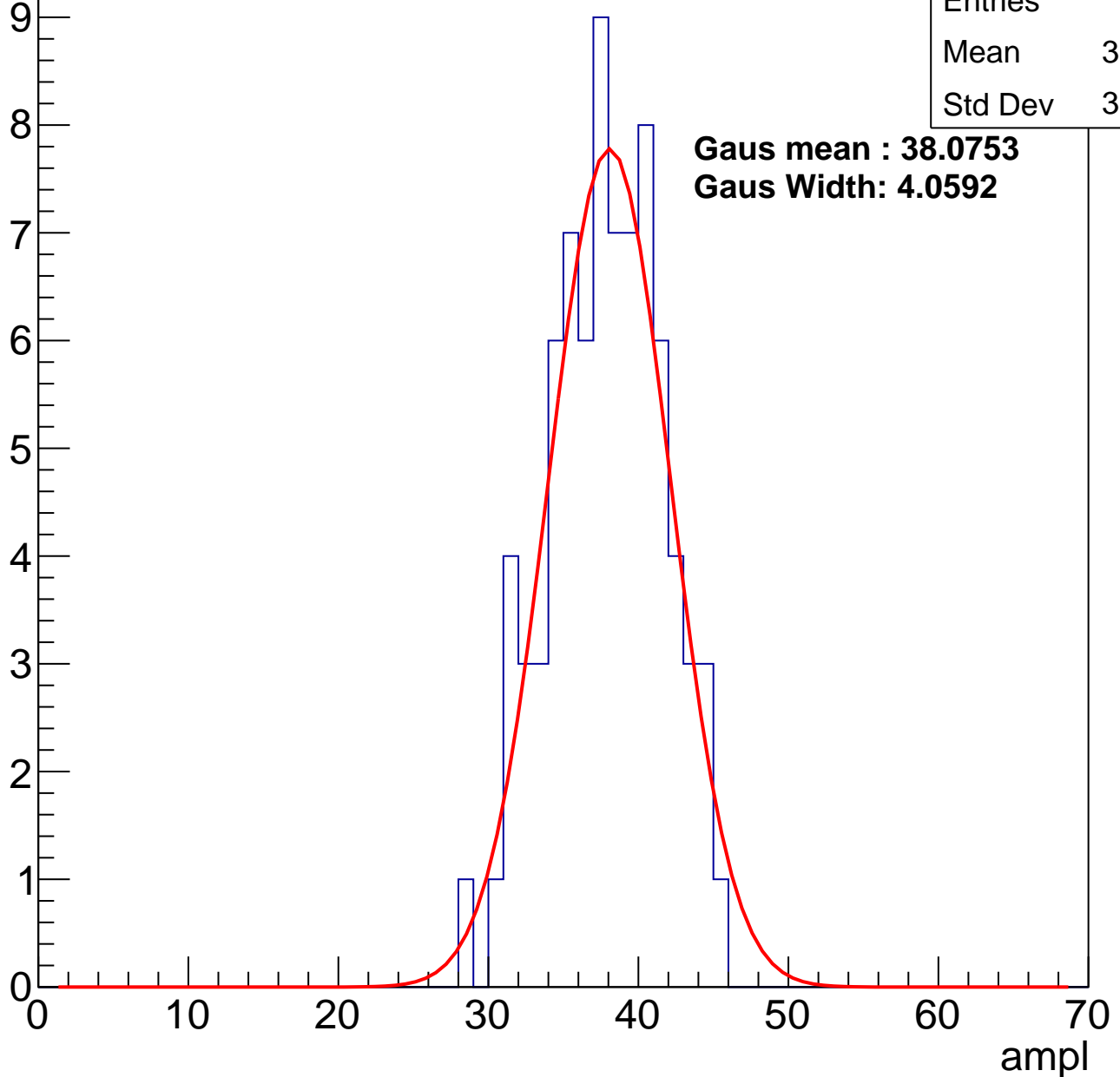
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	37.39
Std Dev	3.723

**Gaus mean : 38.0753**

**Gaus Width: 4.0592**



# B1L101S, U3-ch5, adc2

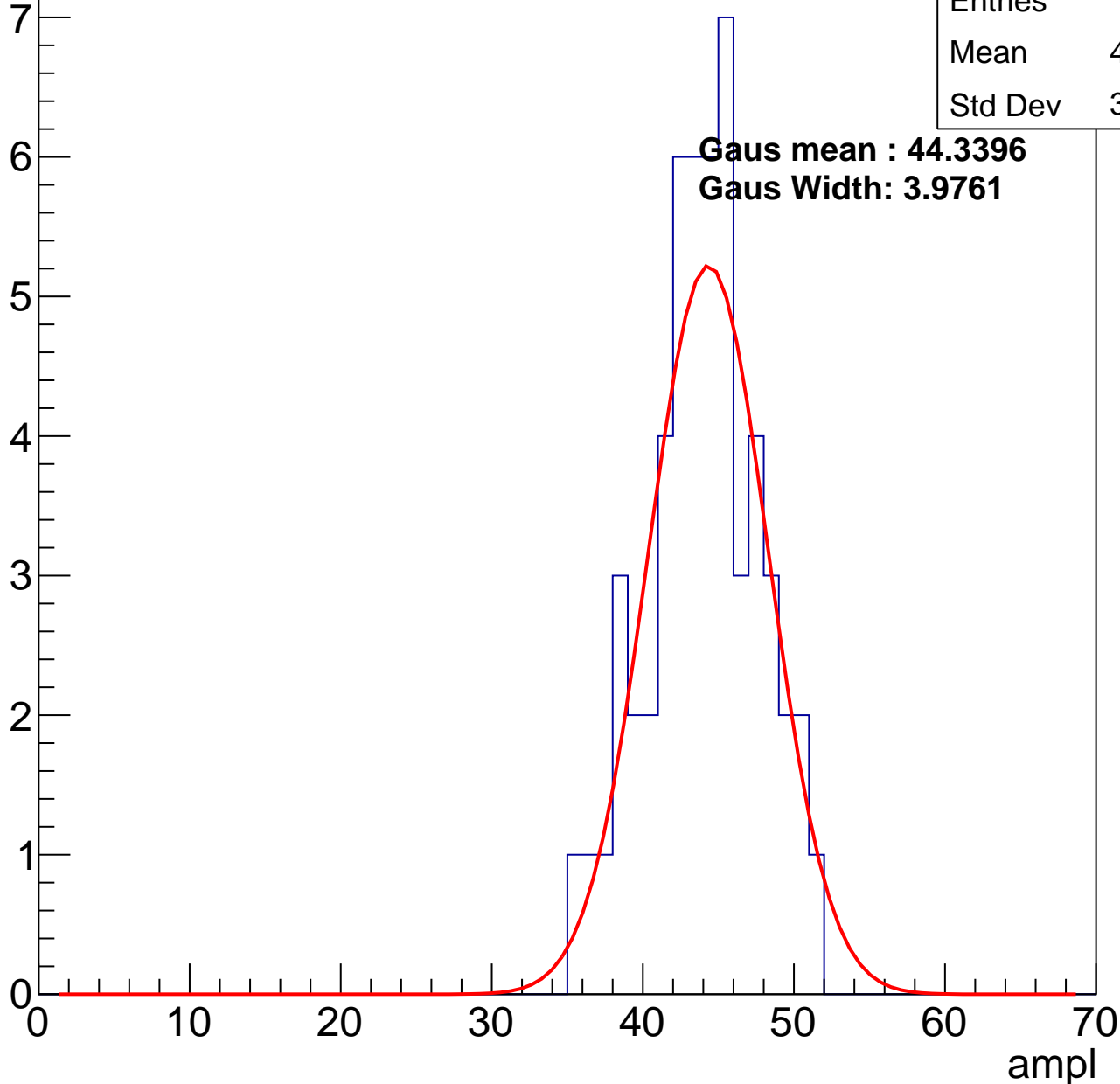
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	43.56
Std Dev	3.635

**Gaus mean : 44.3396**

**Gaus Width: 3.9761**

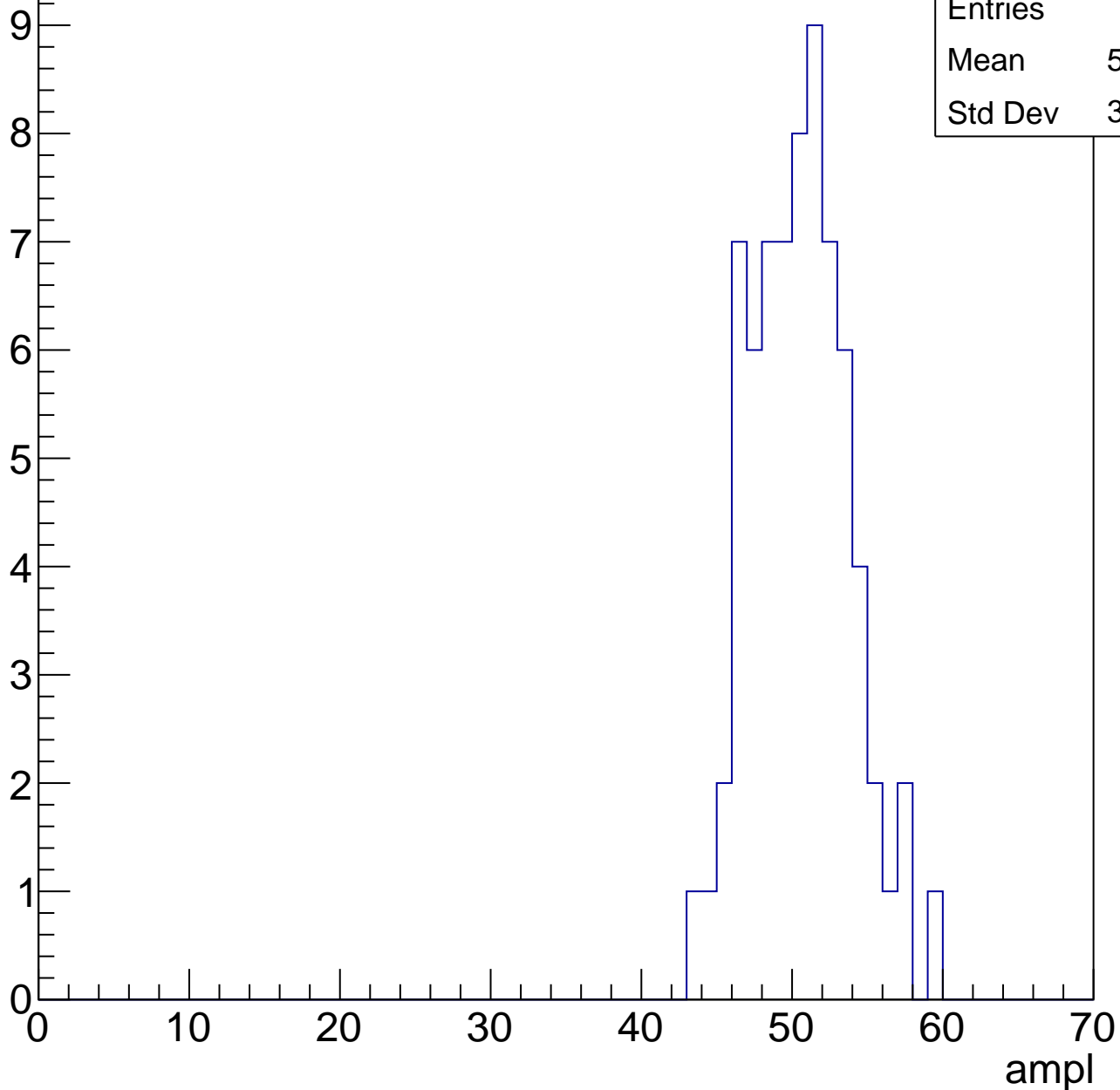


# B1L101S, U3-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

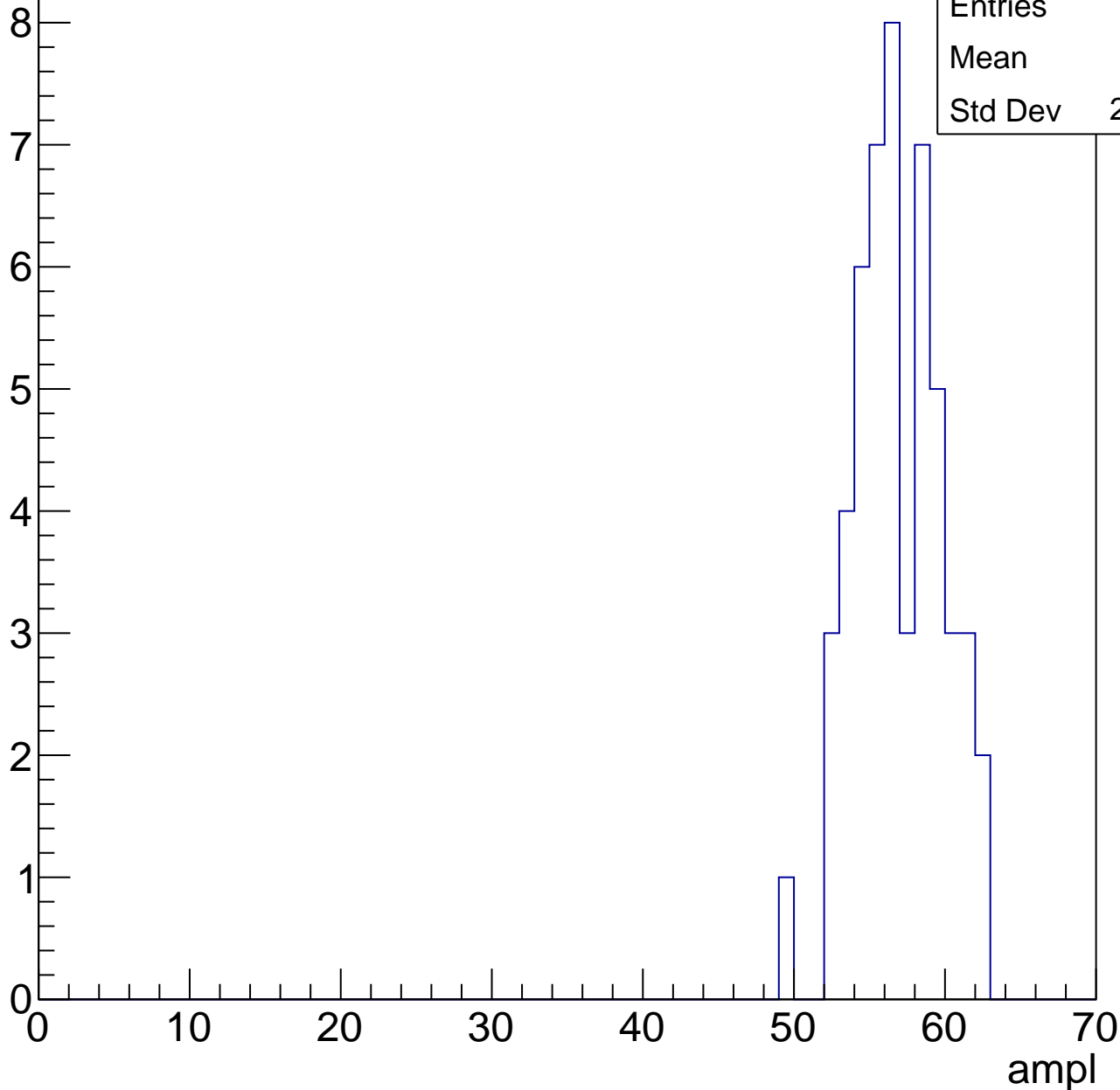
Entries	71
Mean	50.08
Std Dev	3.262



# B1L101S, U3-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch5, adc5

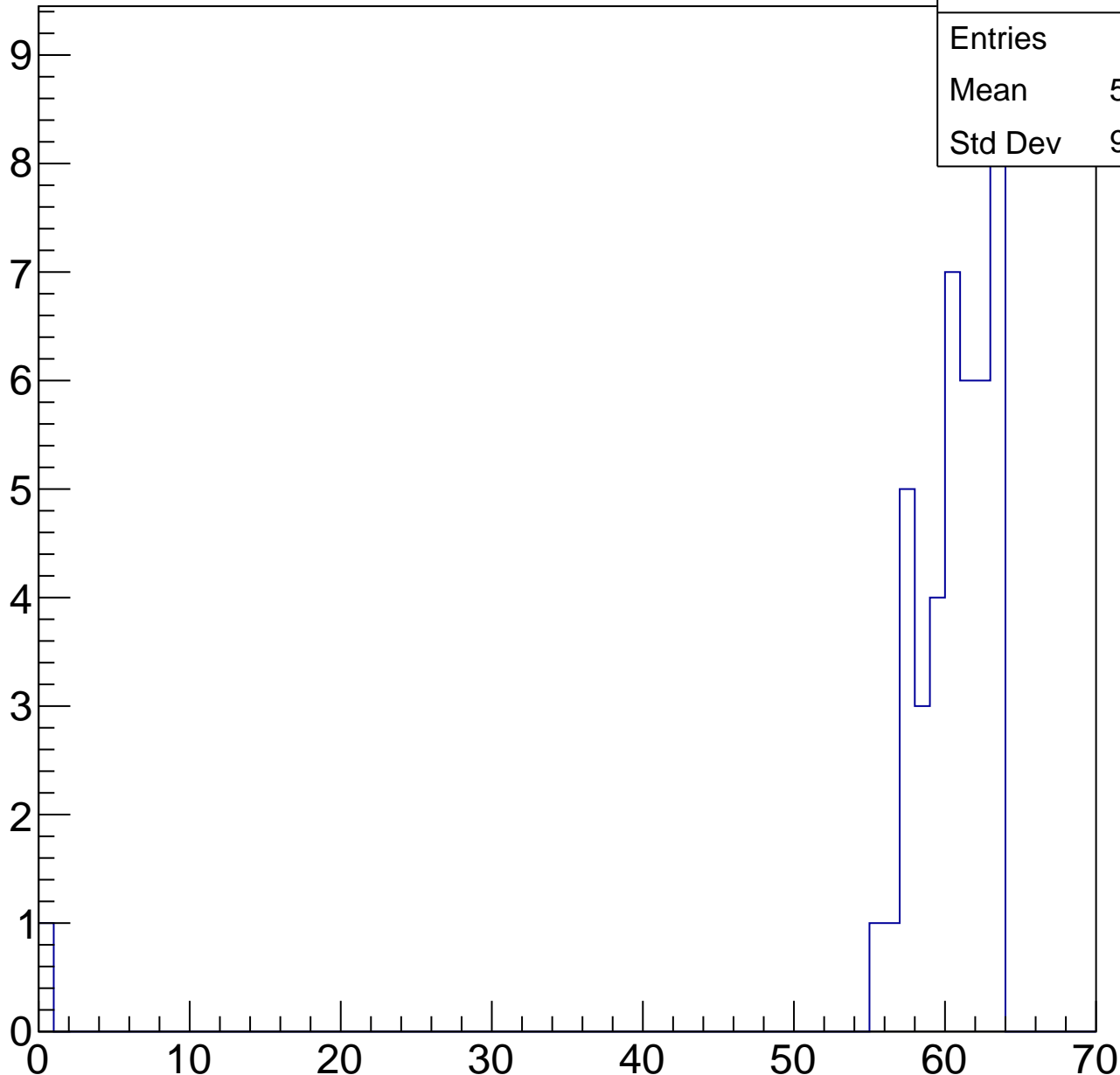
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	43
Mean	58.86
Std Dev	9.348

ampl



# B1L101S, U3-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	4
Mean	62
Std Dev	0.7071

ampl

0 10 20 30 40 50 60 70



# B1L101S, U3-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch6, adc0

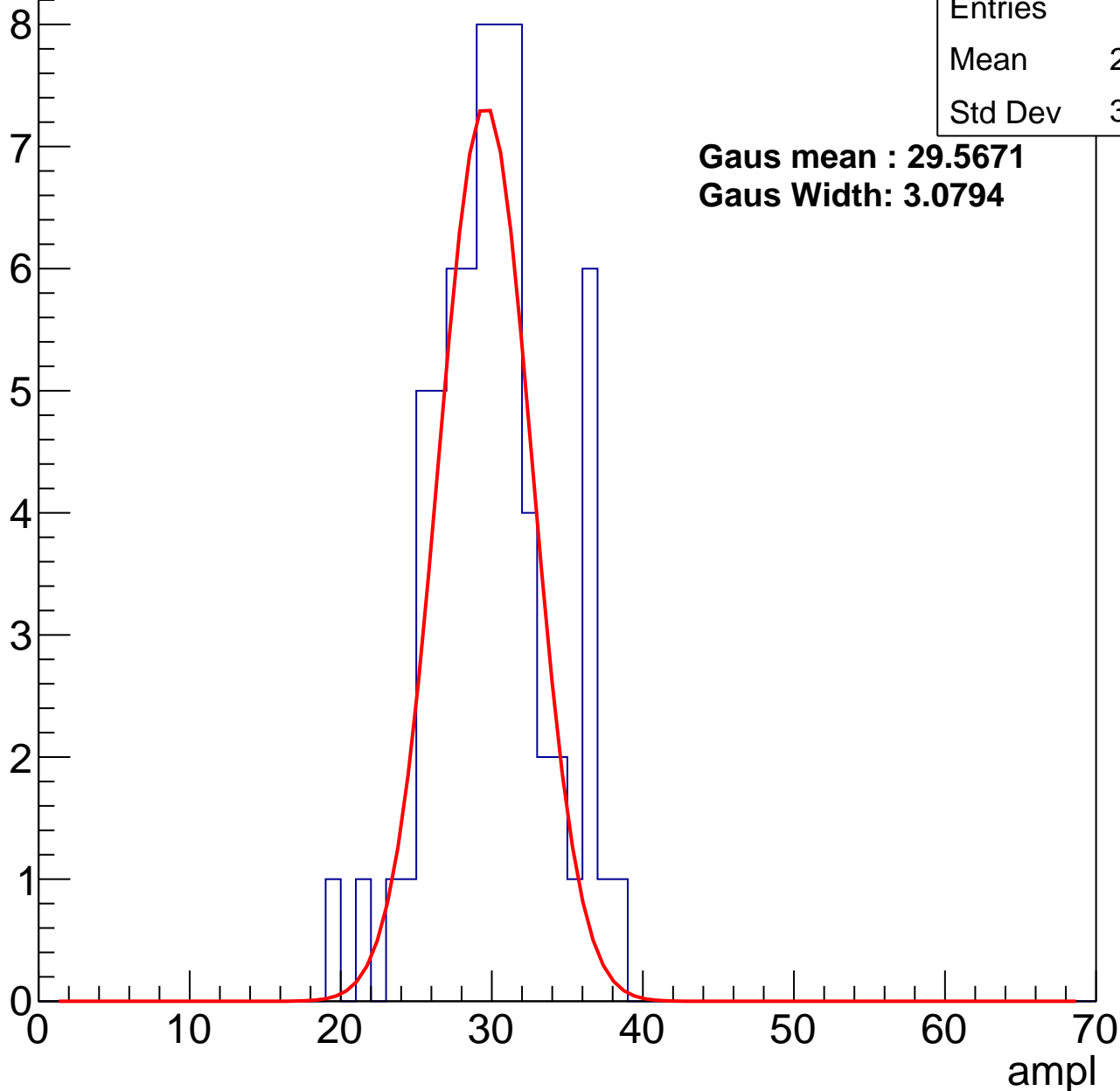
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	29.55
Std Dev	3.849

**Gaus mean : 29.5671**

**Gaus Width: 3.0794**



# B1L101S, U3-ch6, adc1

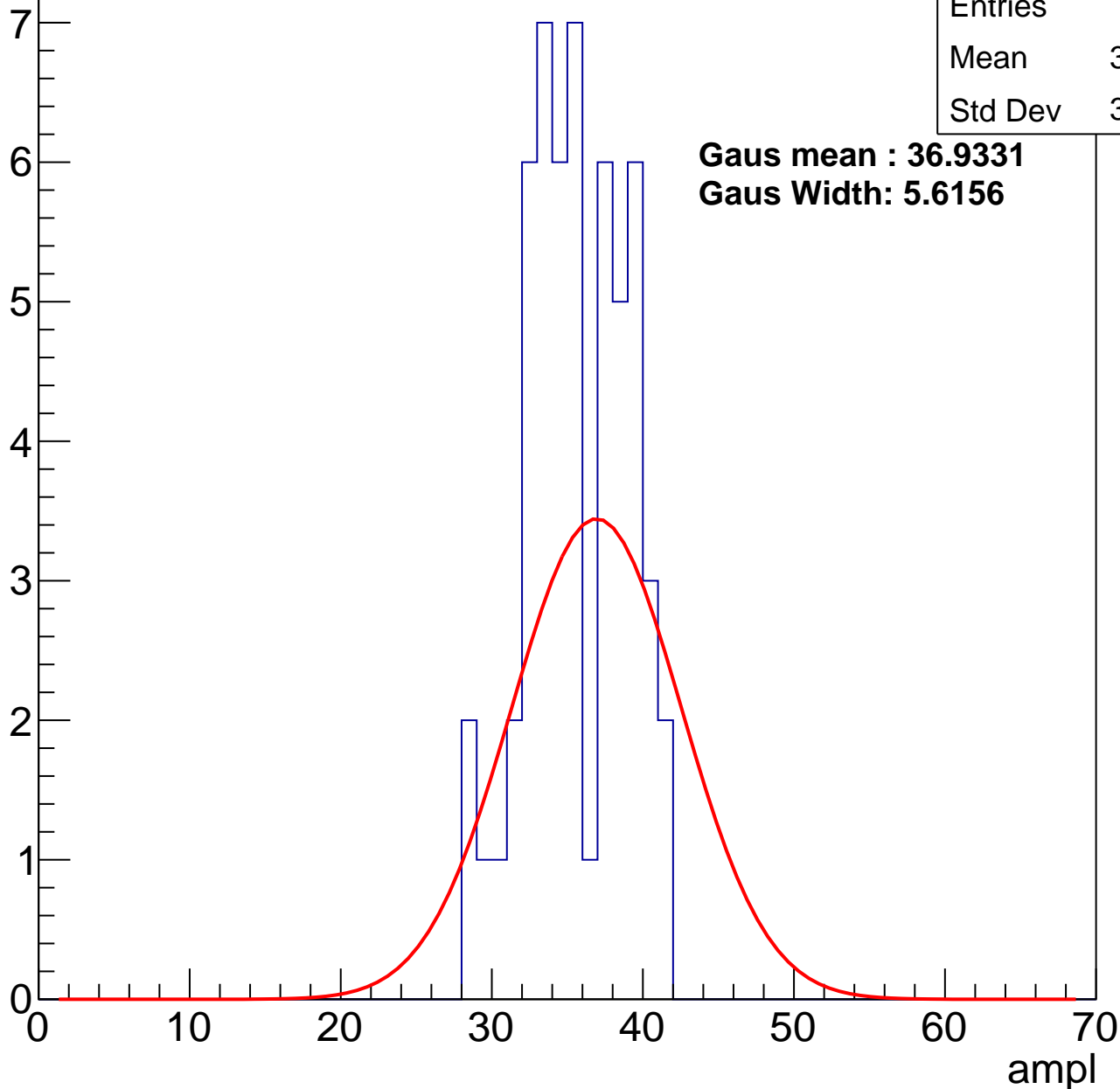
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	35.15
Std Dev	3.278

**Gaus mean : 36.9331**

**Gaus Width: 5.6156**



# B1L101S, U3-ch6, adc2

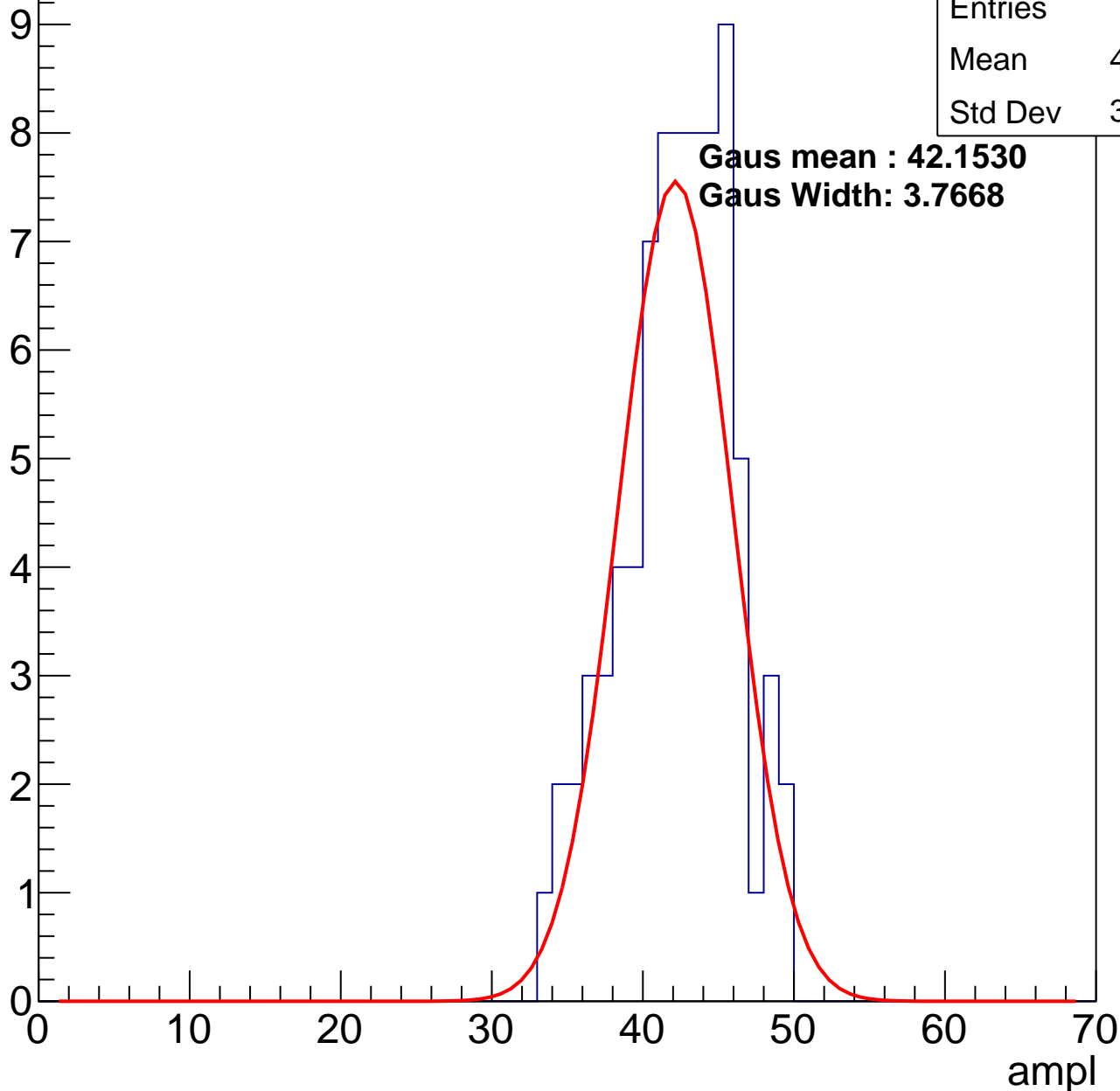
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	41.82
Std Dev	3.679

**Gaus mean : 42.1530**

**Gaus Width: 3.7668**

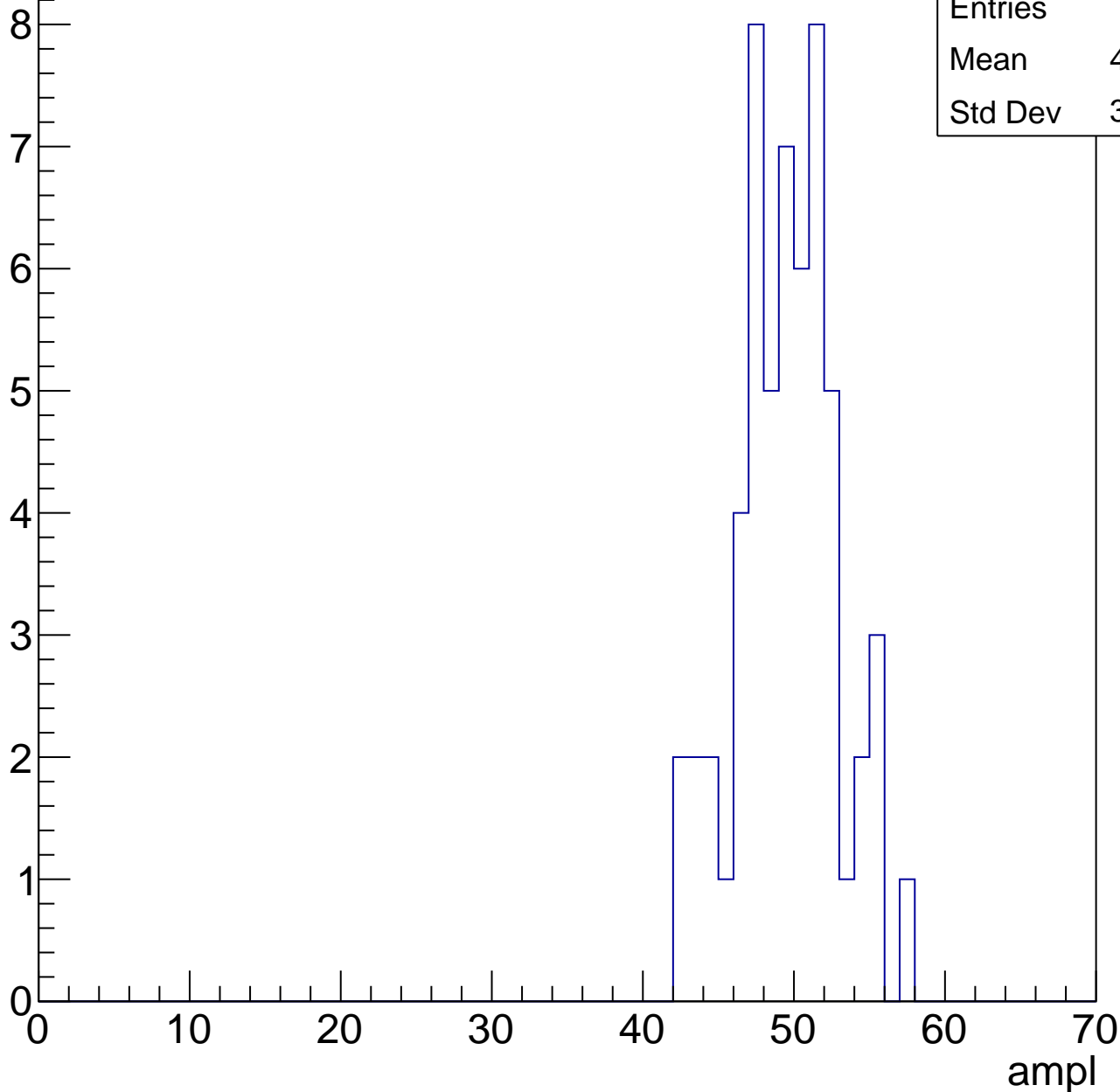


# B1L101S, U3-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	49.07
Std Dev	3.324

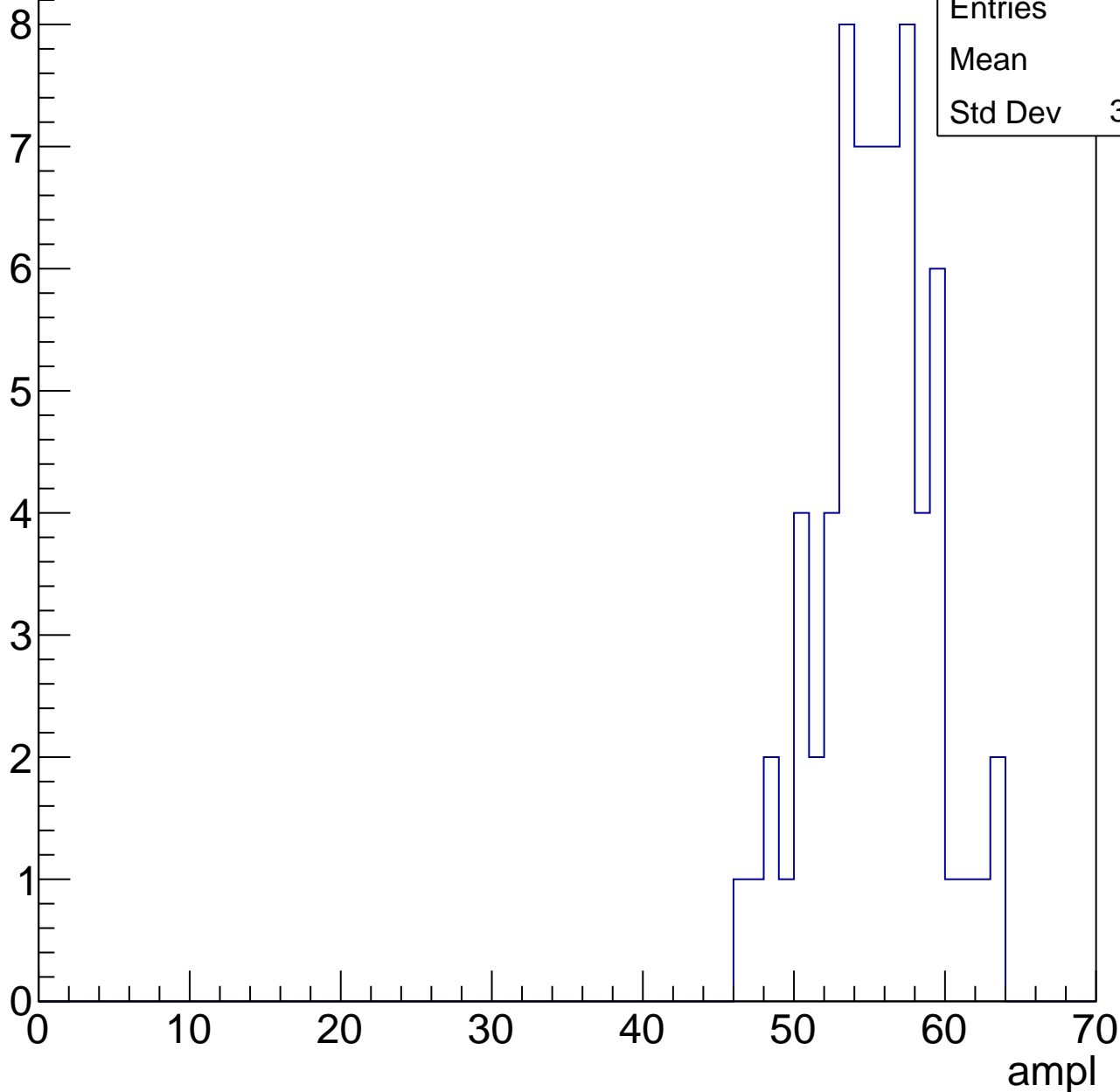


# B1L101S, U3-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

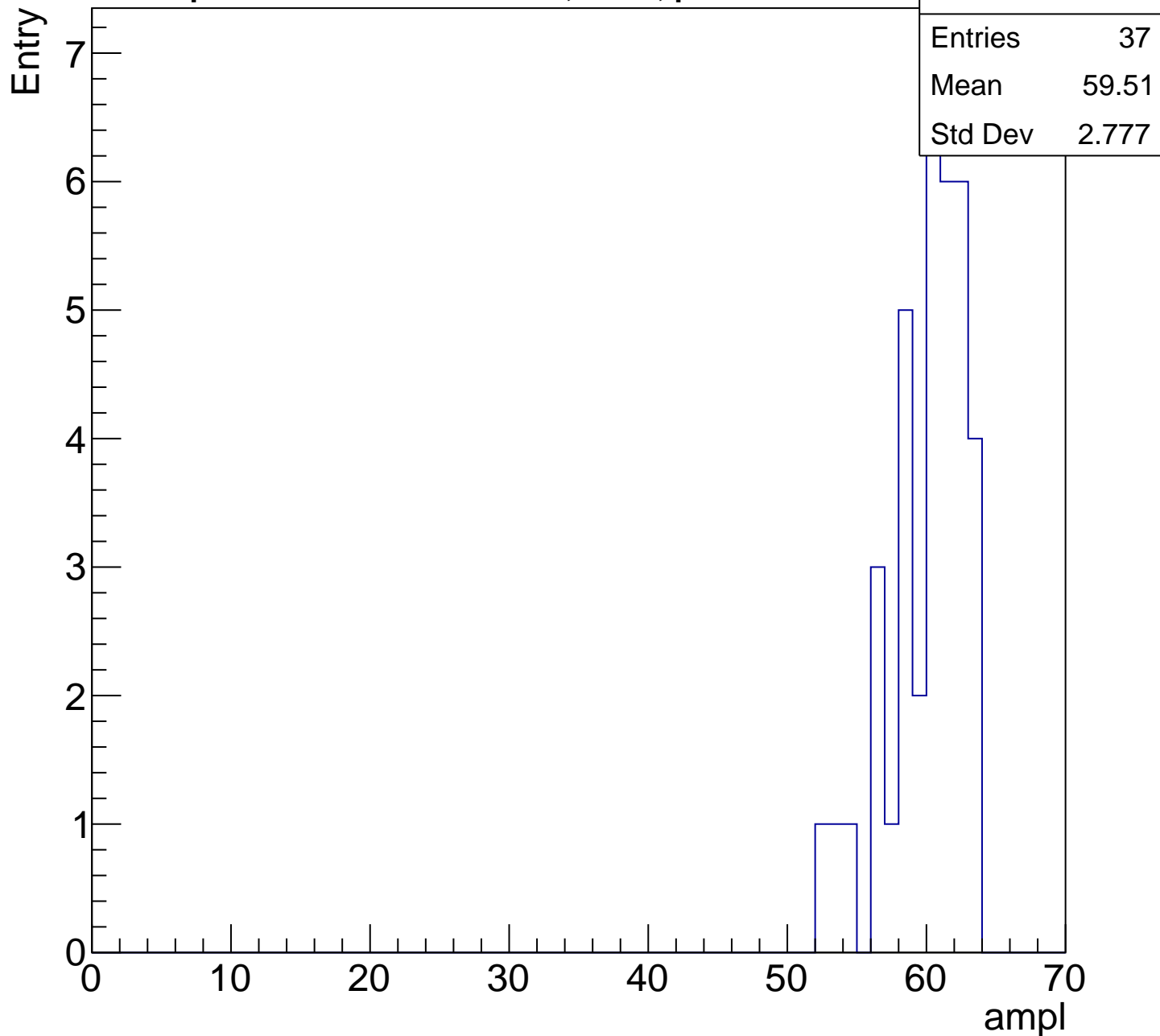
Entry

Entries	67
Mean	54.9
Std Dev	3.653



# B1L101S, U3-ch6, adc5

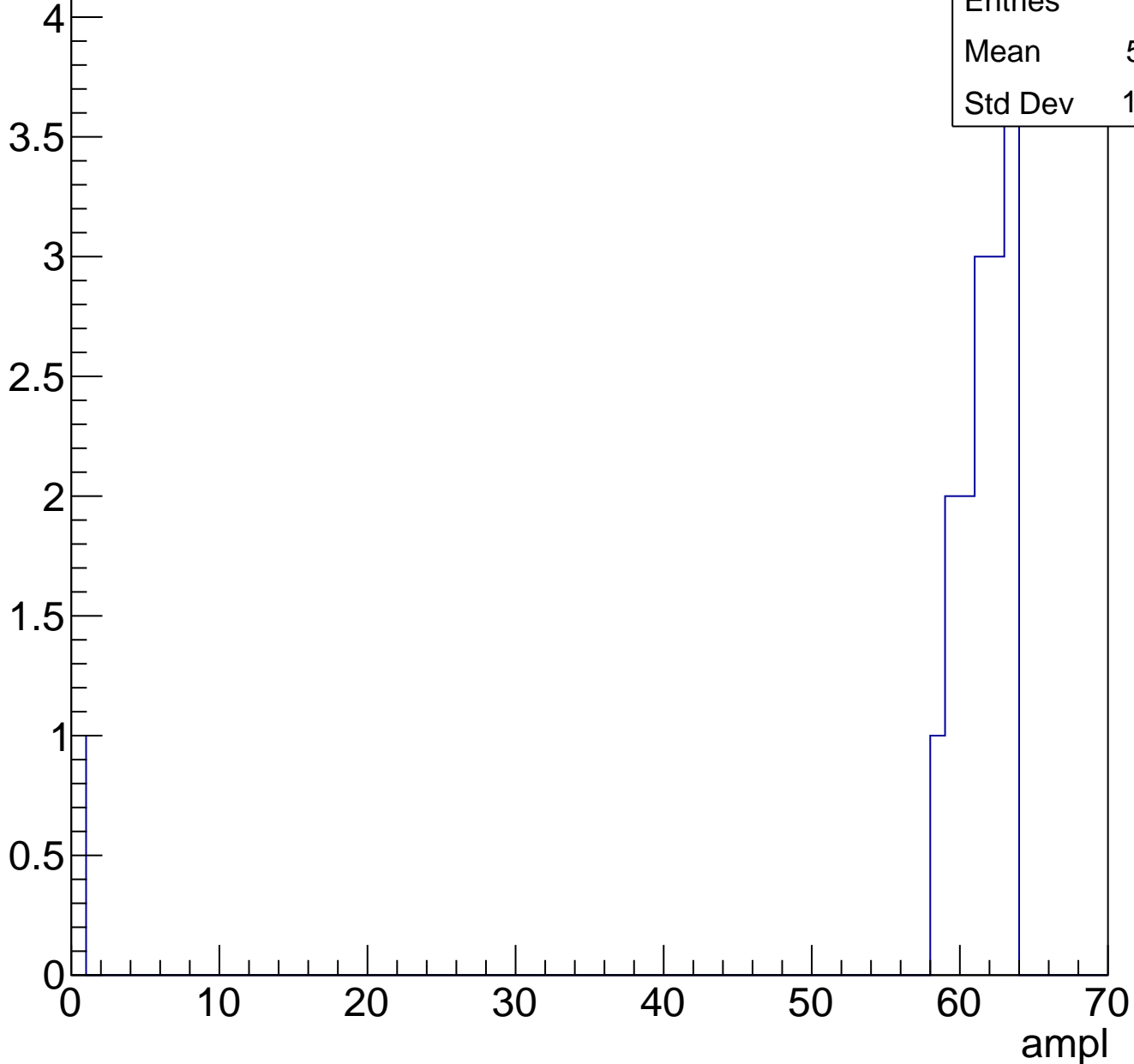
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	16
Mean	57.31
Std Dev	14.88



# B1L101S, U3-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

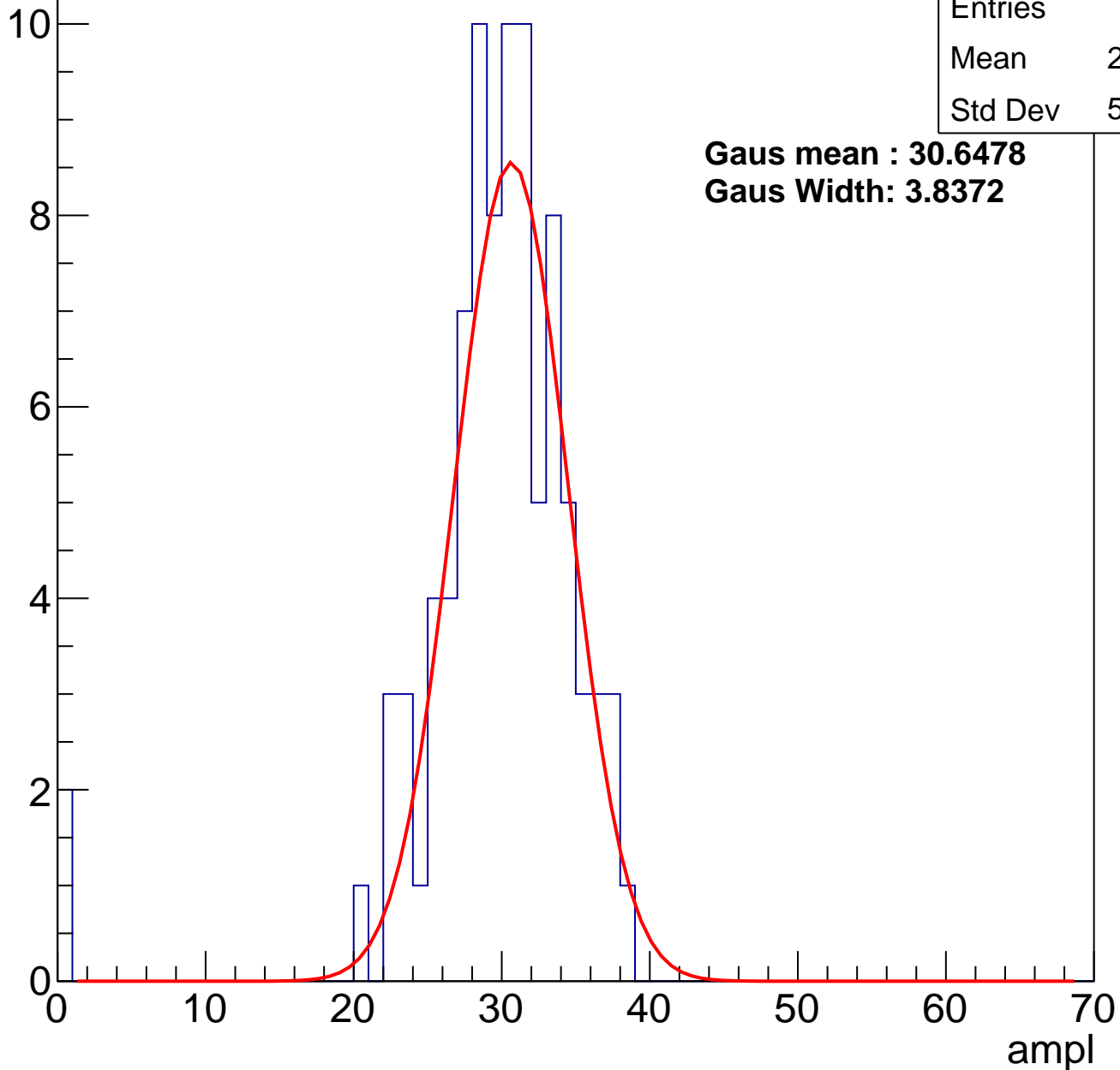
# B1L101S, U3-ch7, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	91
Mean	29.12
Std Dev	5.795

**Gaus mean : 30.6478**  
**Gaus Width: 3.8372**

Entry



# B1L101S, U3-ch7, adc1

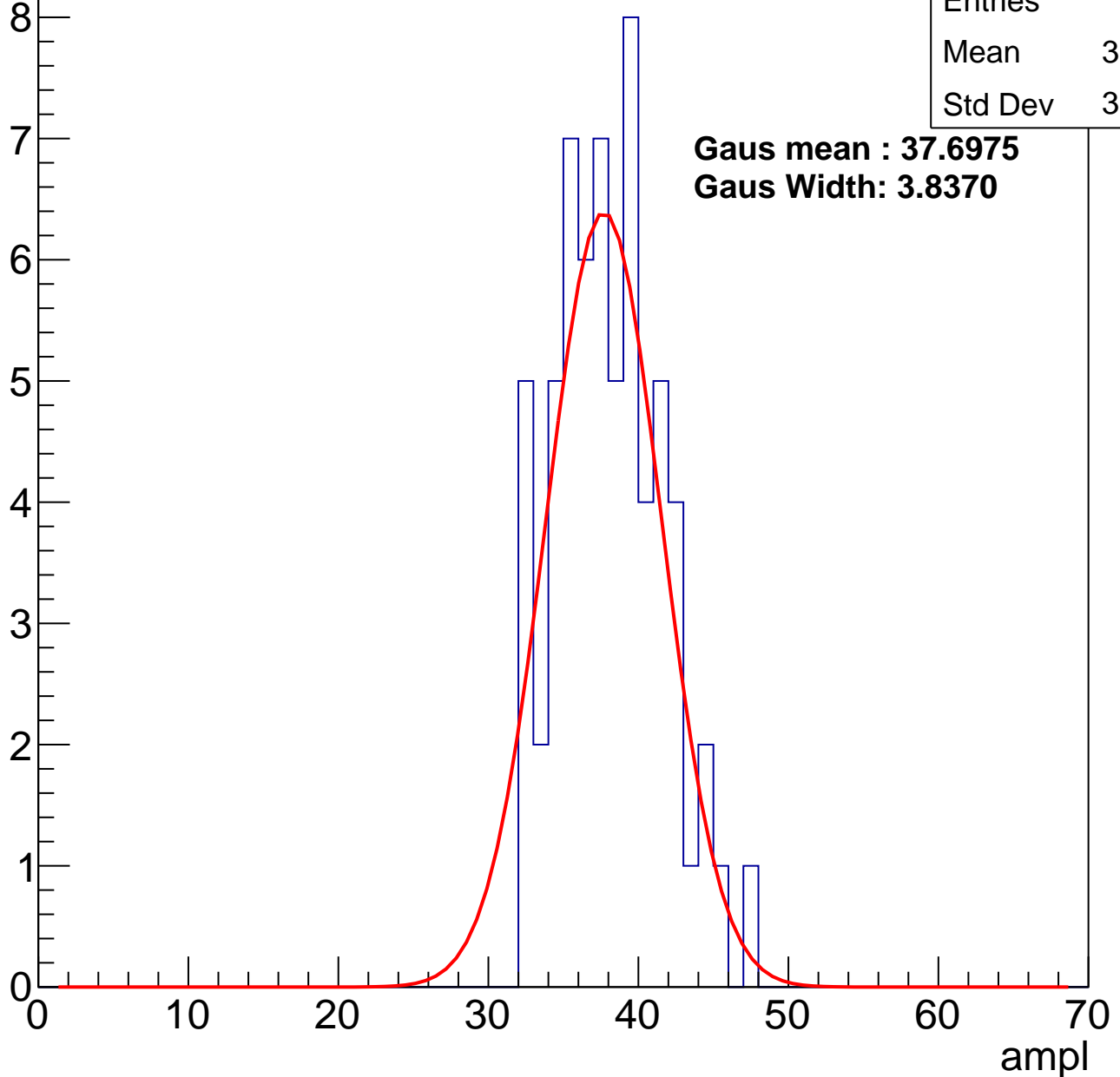
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	37.68
Std Dev	3.468

**Gaus mean : 37.6975**

**Gaus Width: 3.8370**



# B1L101S, U3-ch7, adc2

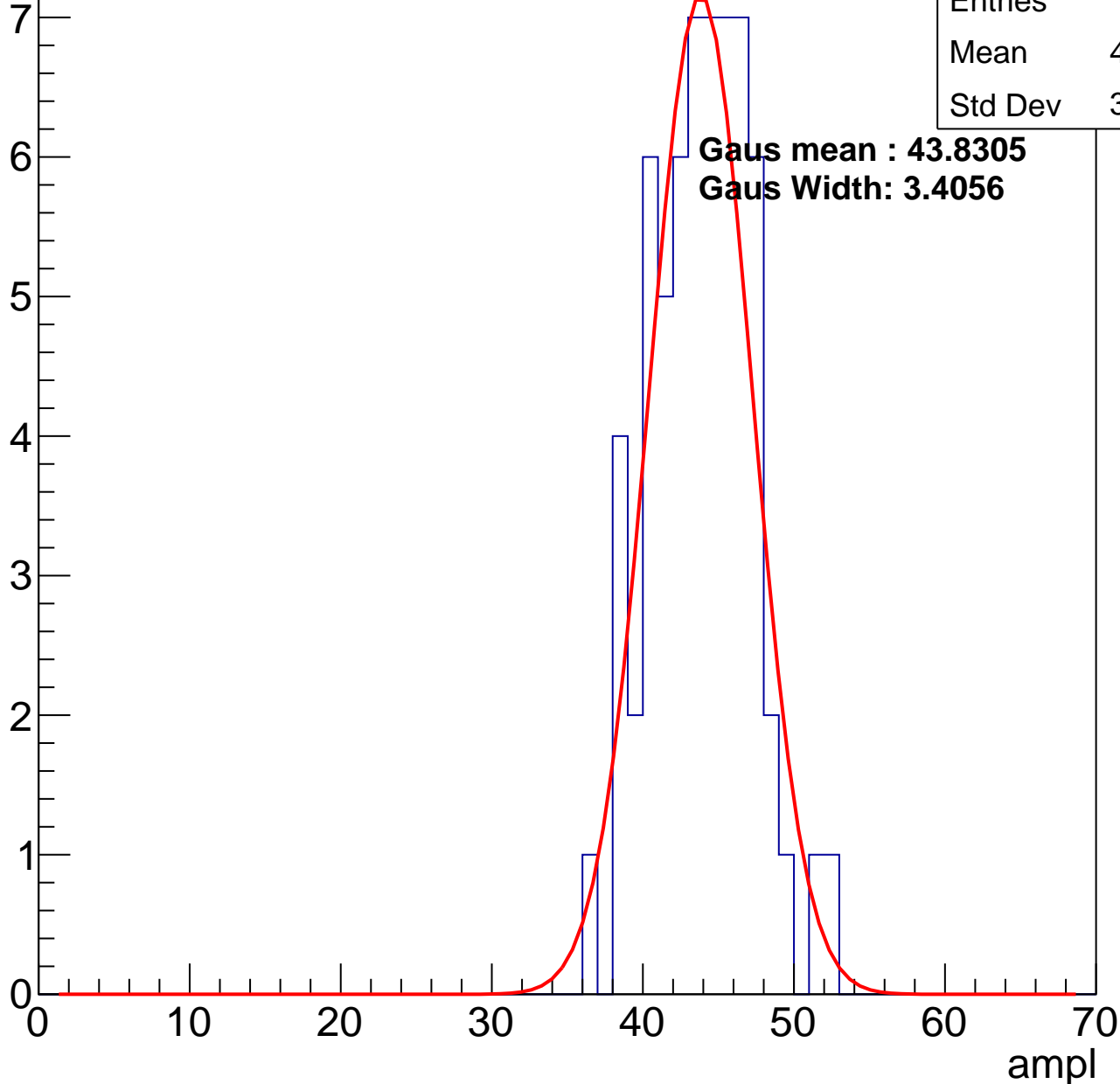
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	43.48
Std Dev	3.265

**Gaus mean : 43.8305**

**Gaus Width: 3.4056**

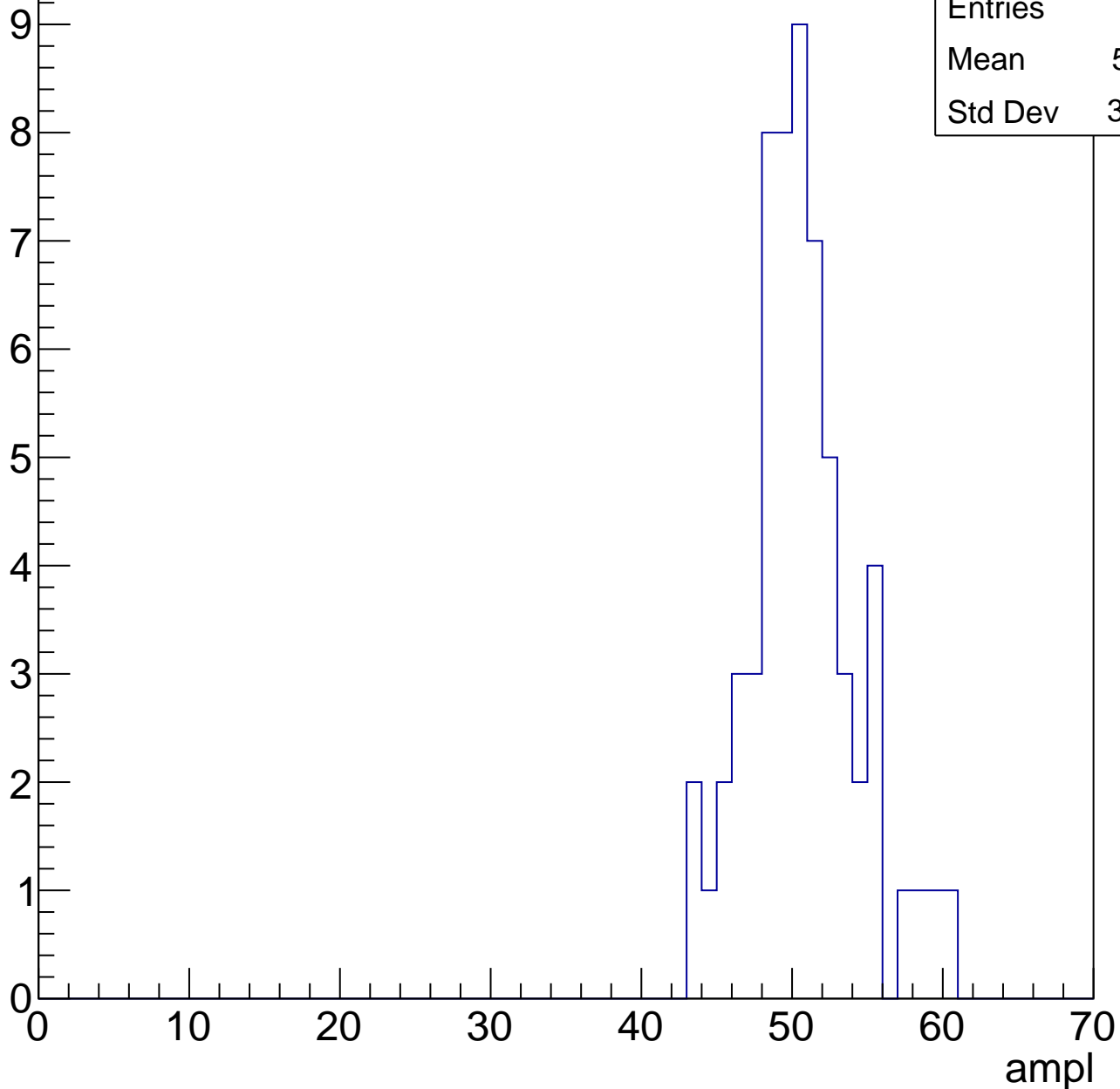


# B1L101S, U3-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	50.21
Std Dev	3.567

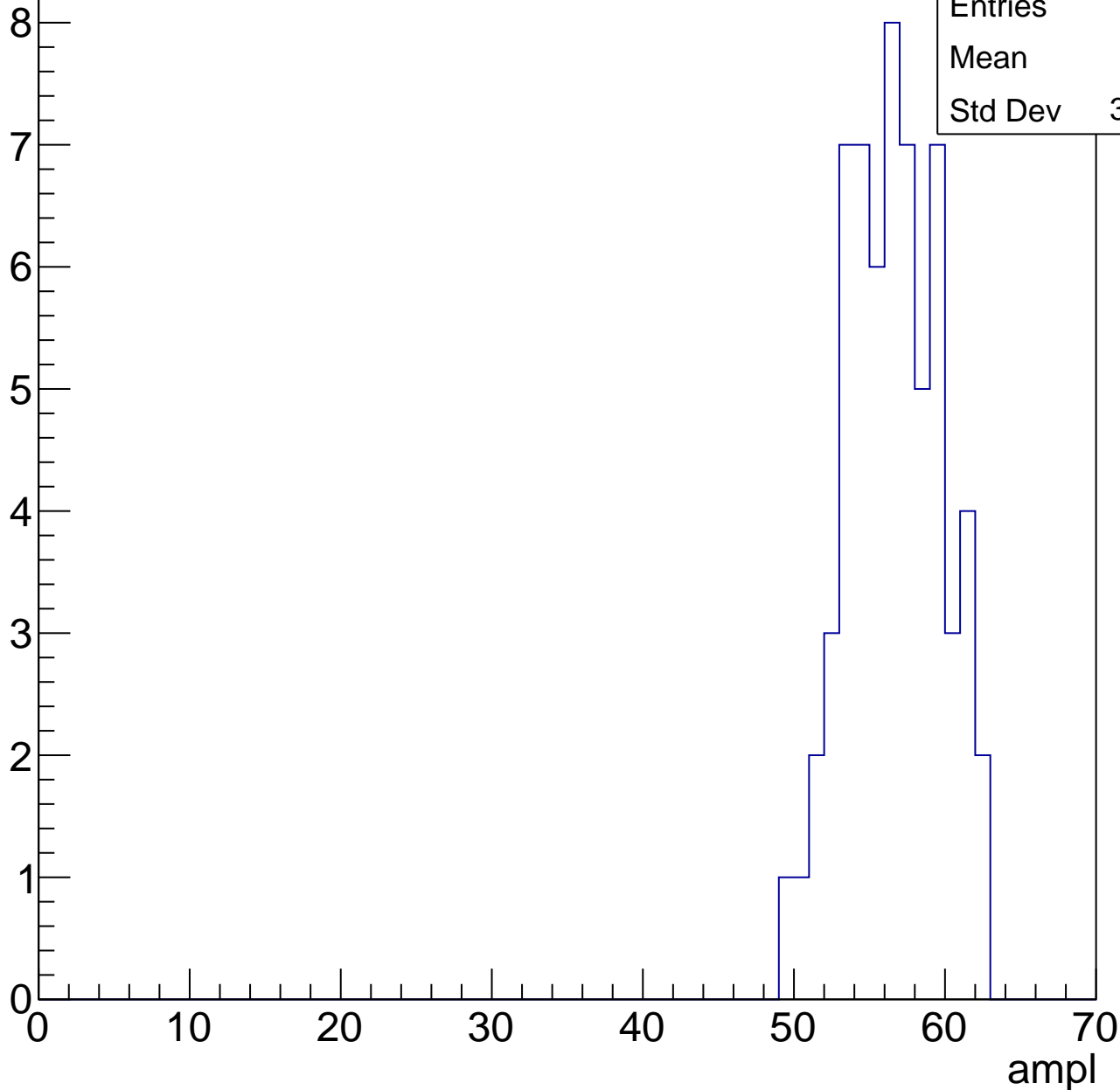


# B1L101S, U3-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	56.1
Std Dev	3.059

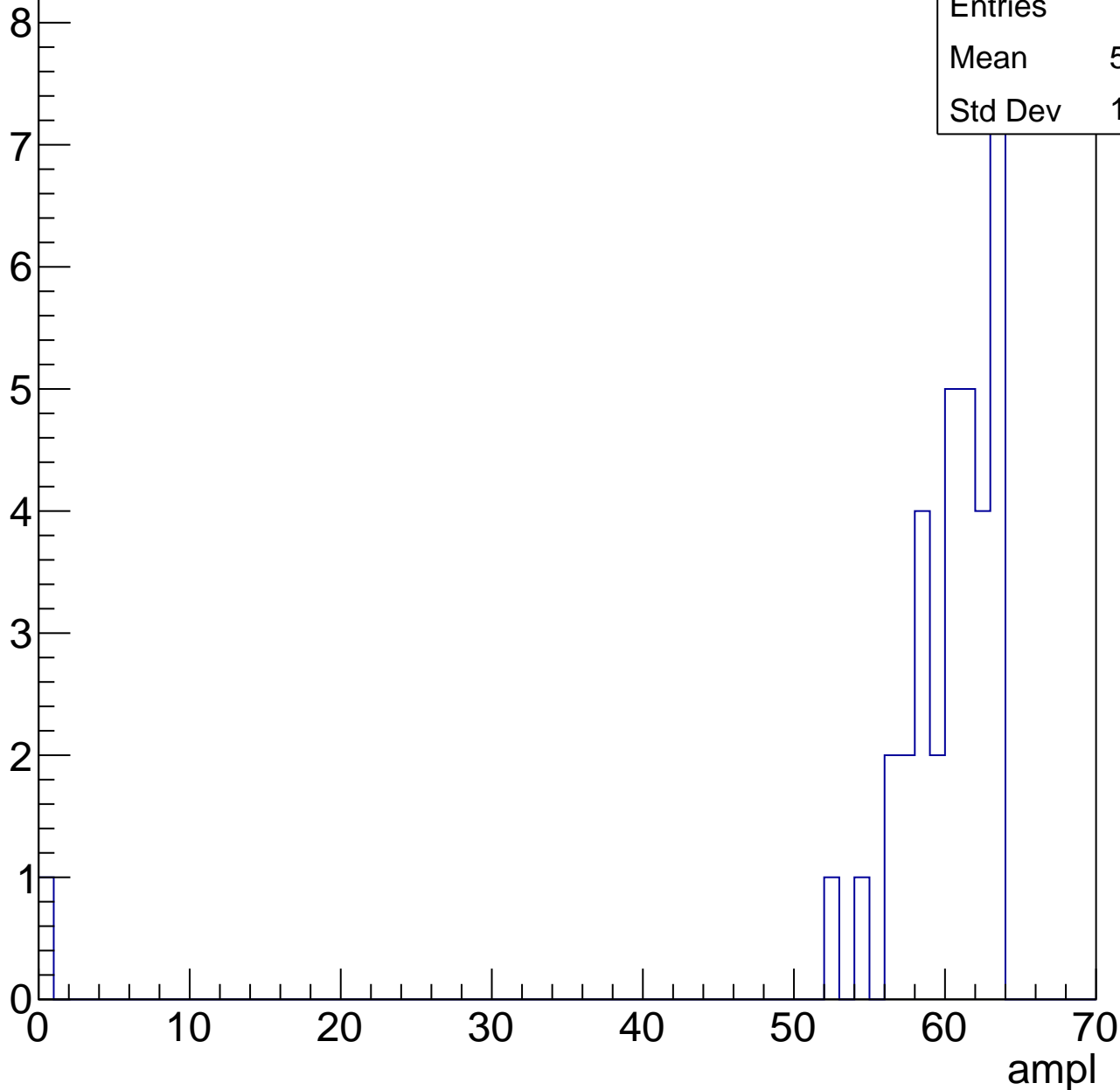


# B1L101S, U3-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

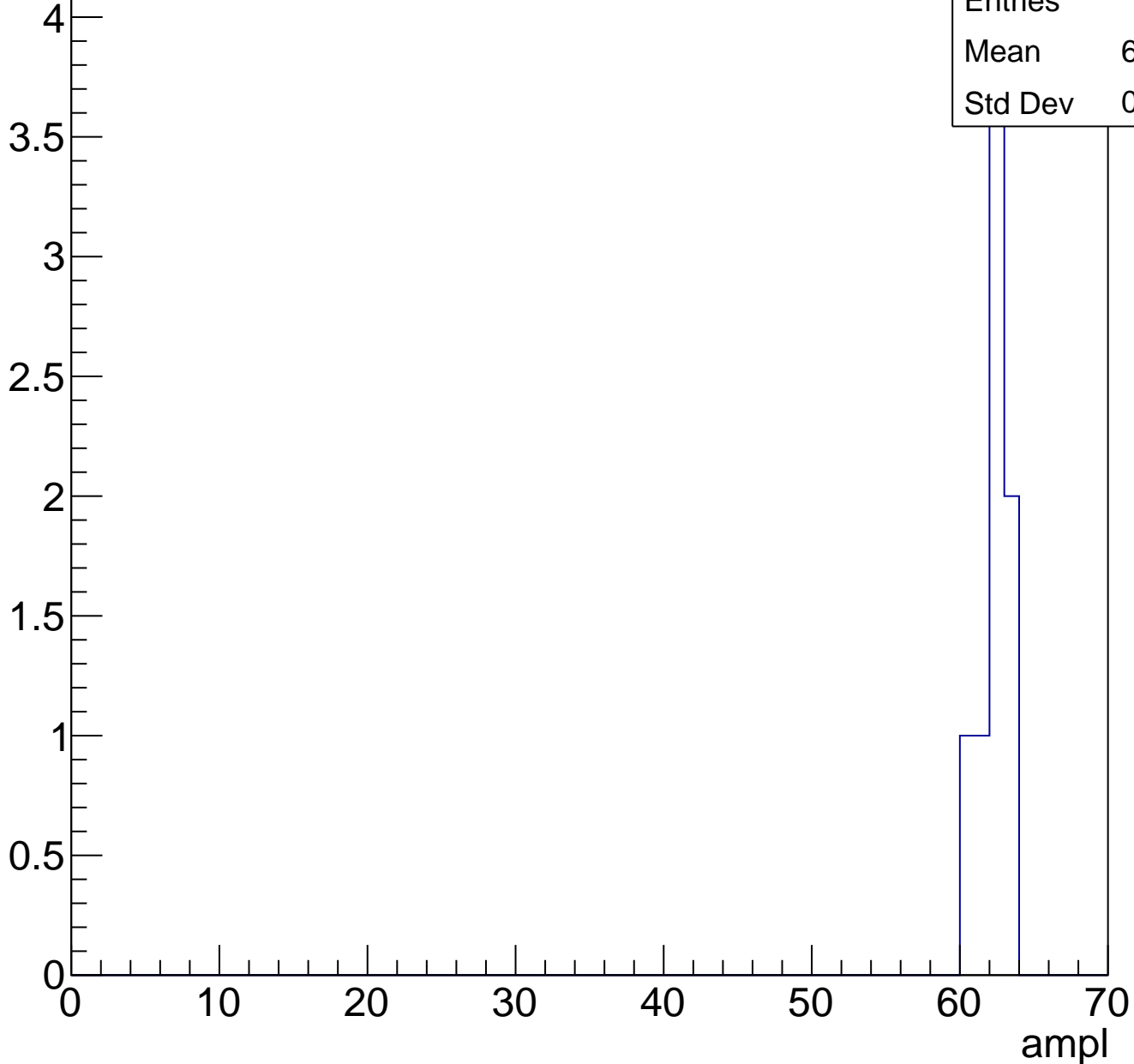
Entries	35
Mean	58.26
Std Dev	10.36



# B1L101S, U3-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U3-ch8, adc0

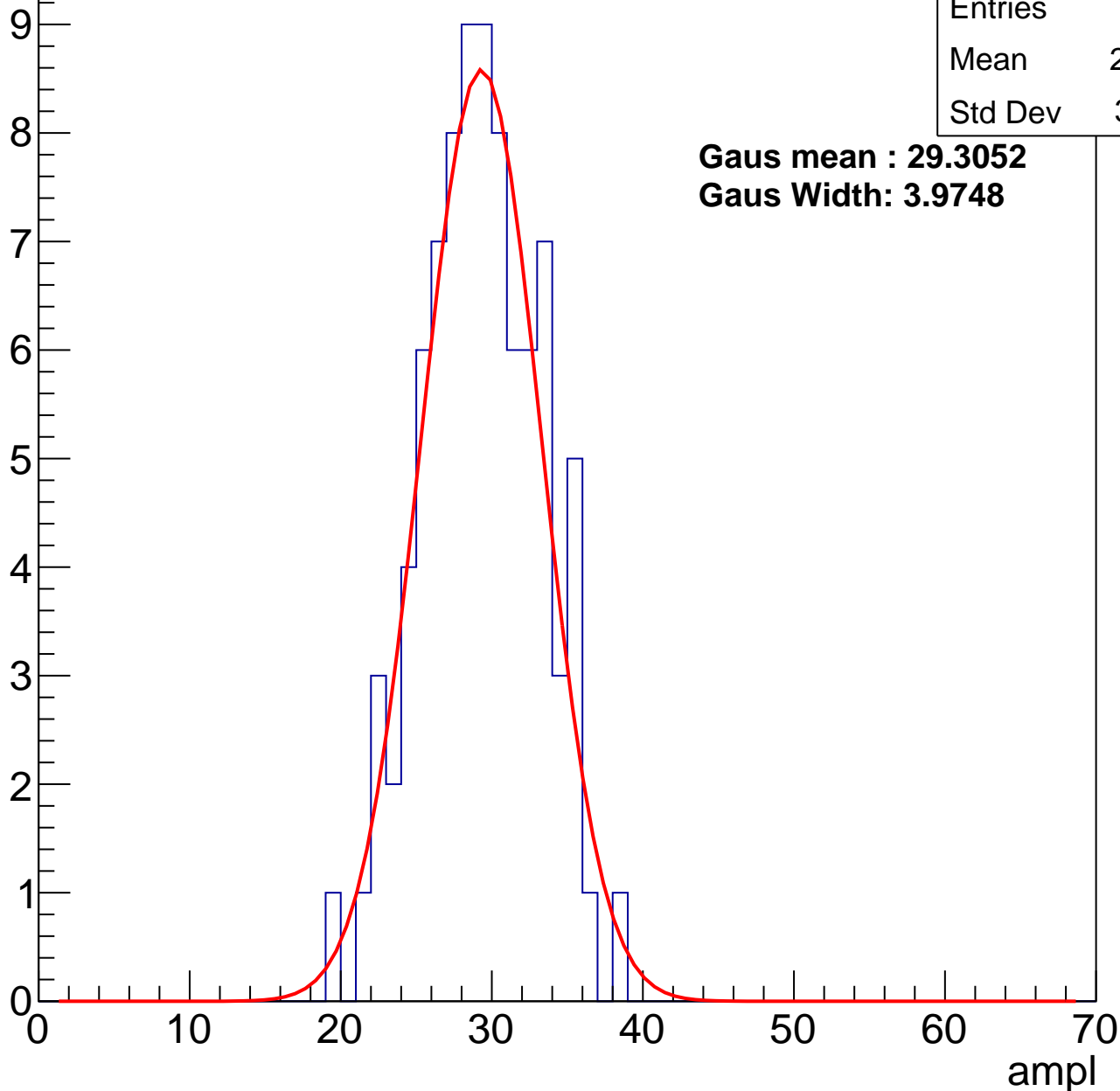
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	87
Mean	28.84
Std Dev	3.811

**Gaus mean : 29.3052**

**Gaus Width: 3.9748**



# B1L101S, U3-ch8, adc1

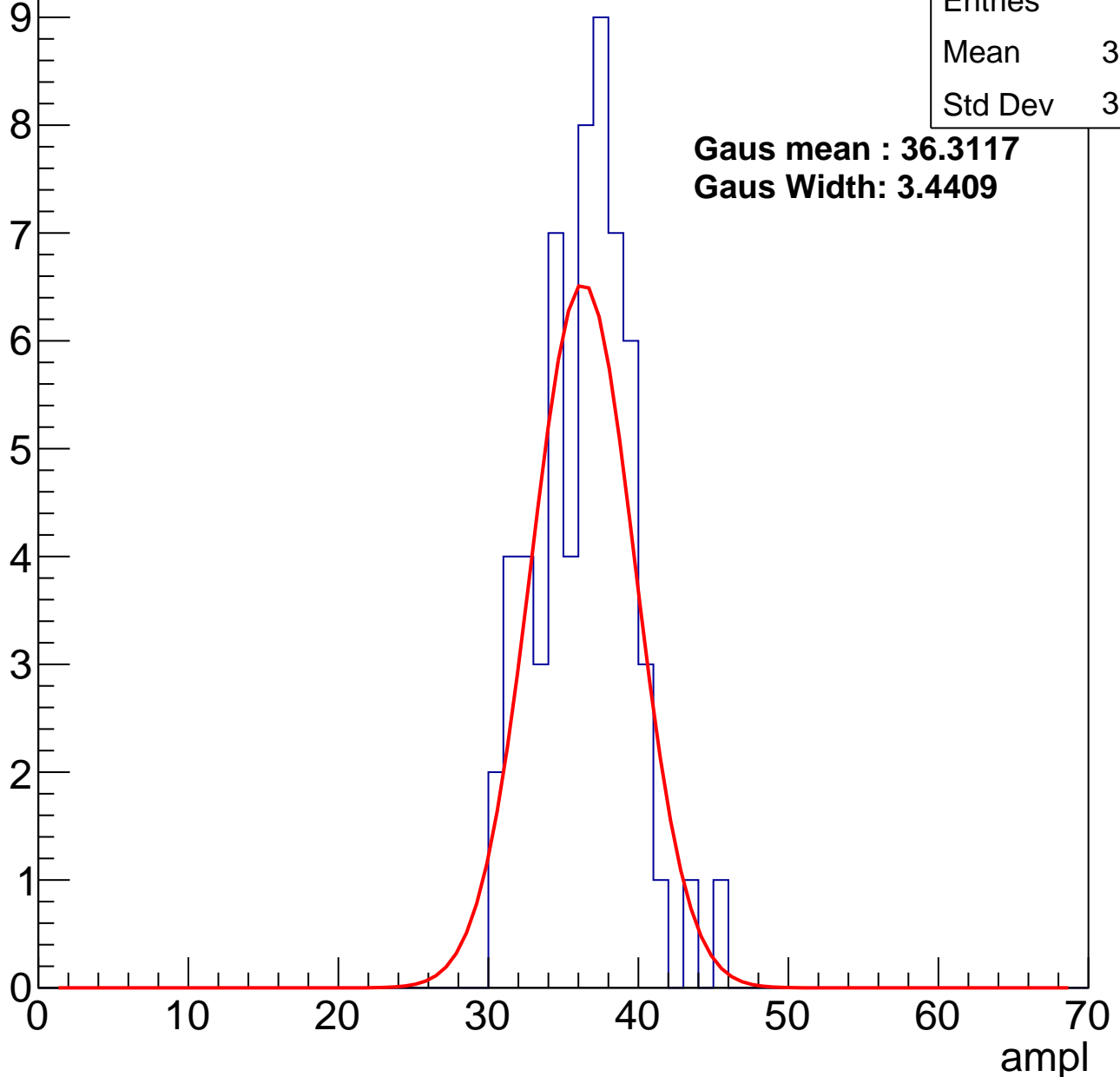
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	35.98
Std Dev	3.133

**Gaus mean : 36.3117**

**Gaus Width: 3.4409**



# B1L101S, U3-ch8, adc2

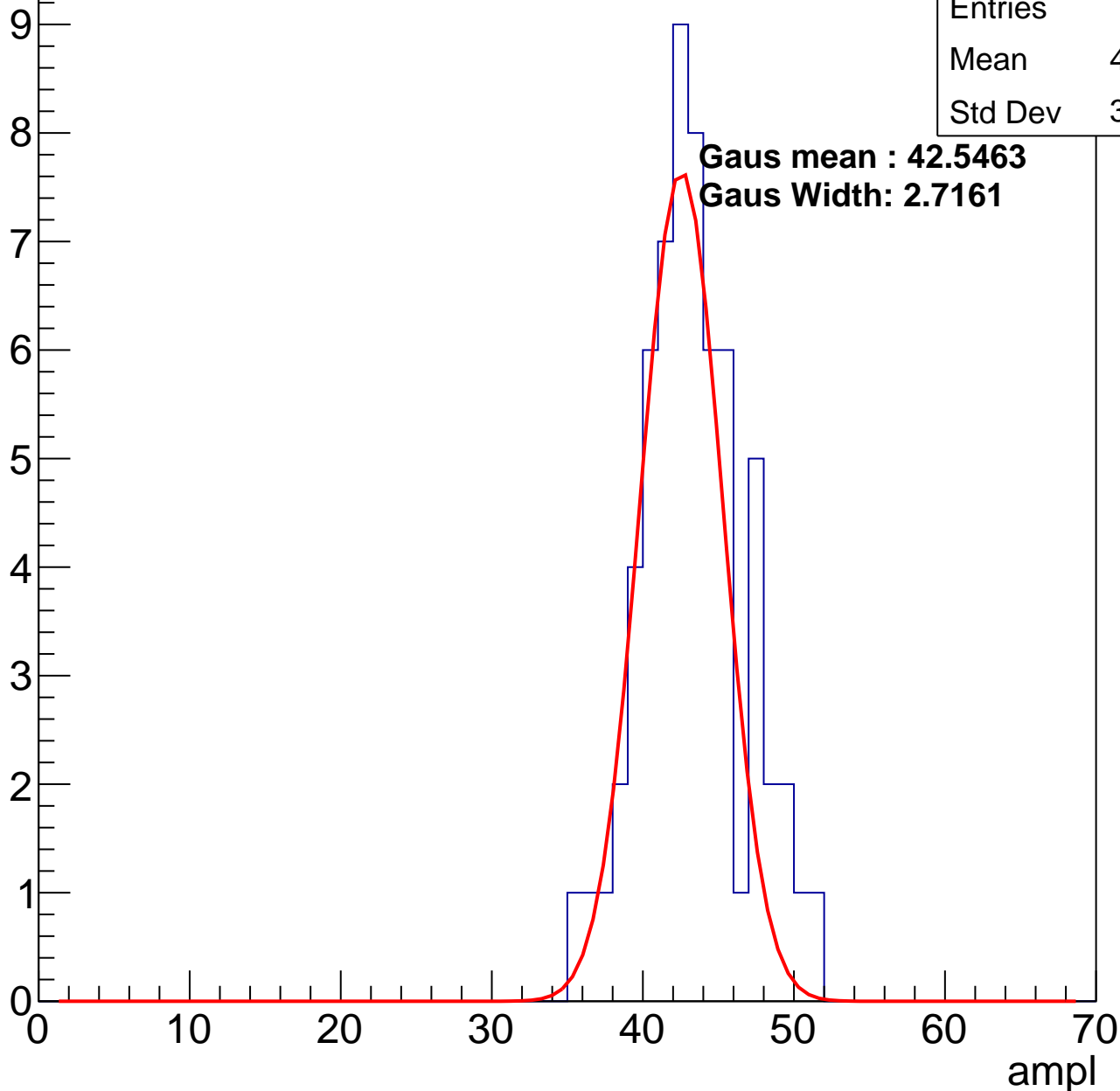
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	42.84
Std Dev	3.349

**Gaus mean : 42.5463**

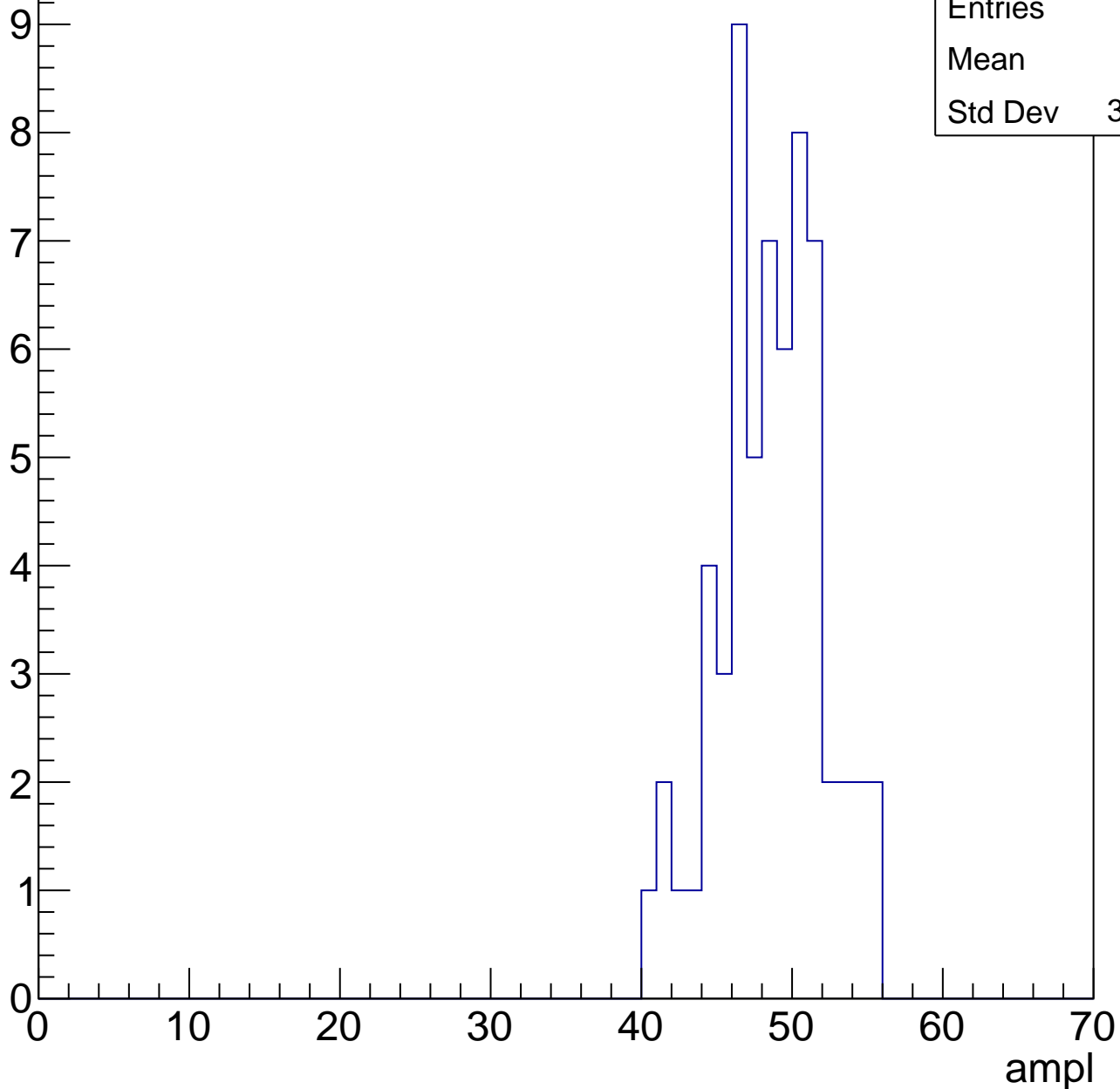
**Gaus Width: 2.7161**



# B1L101S, U3-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



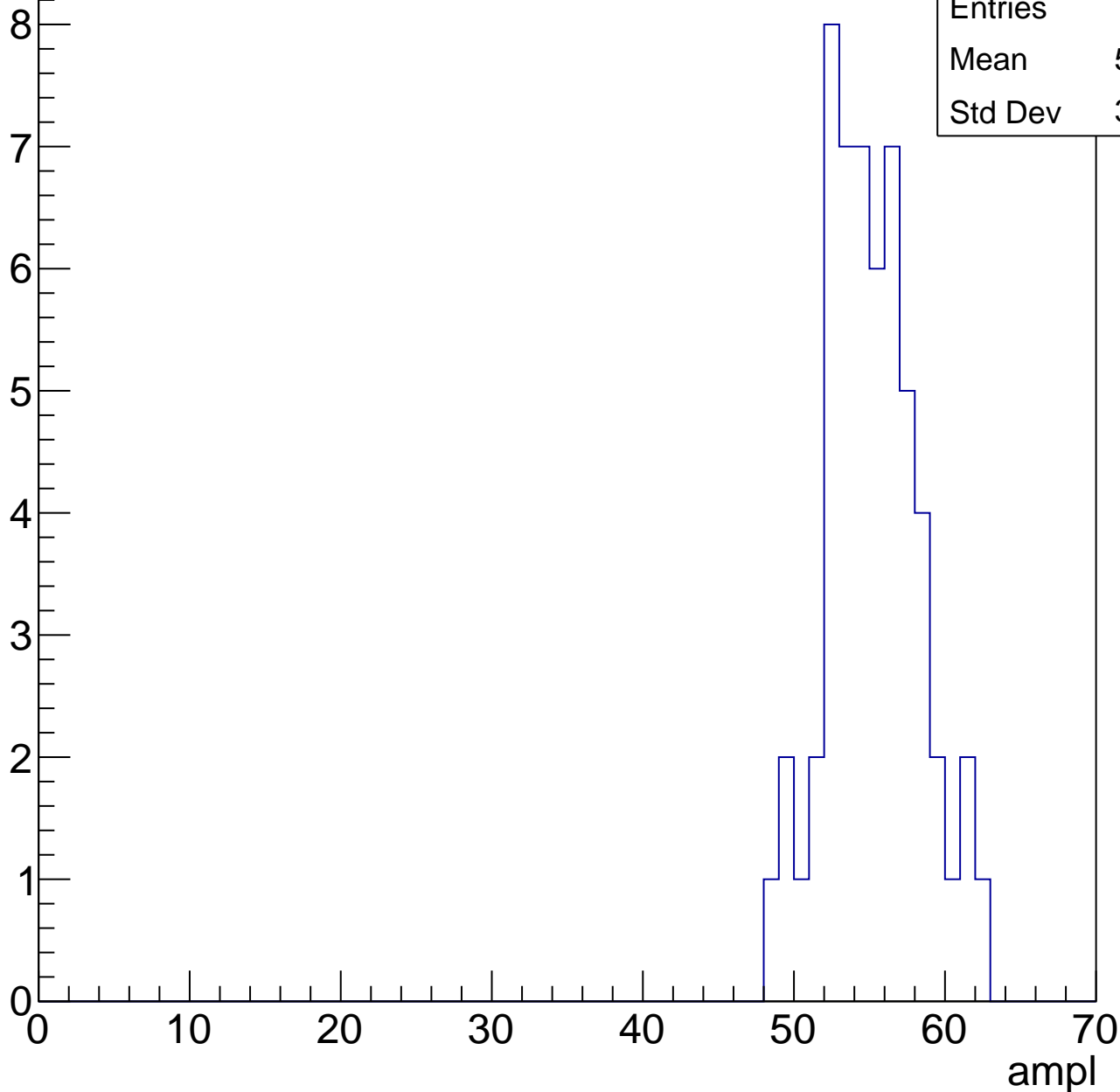
Entries	62
Mean	48.1
Std Dev	3.378

# B1L101S, U3-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	54.71
Std Dev	3.051

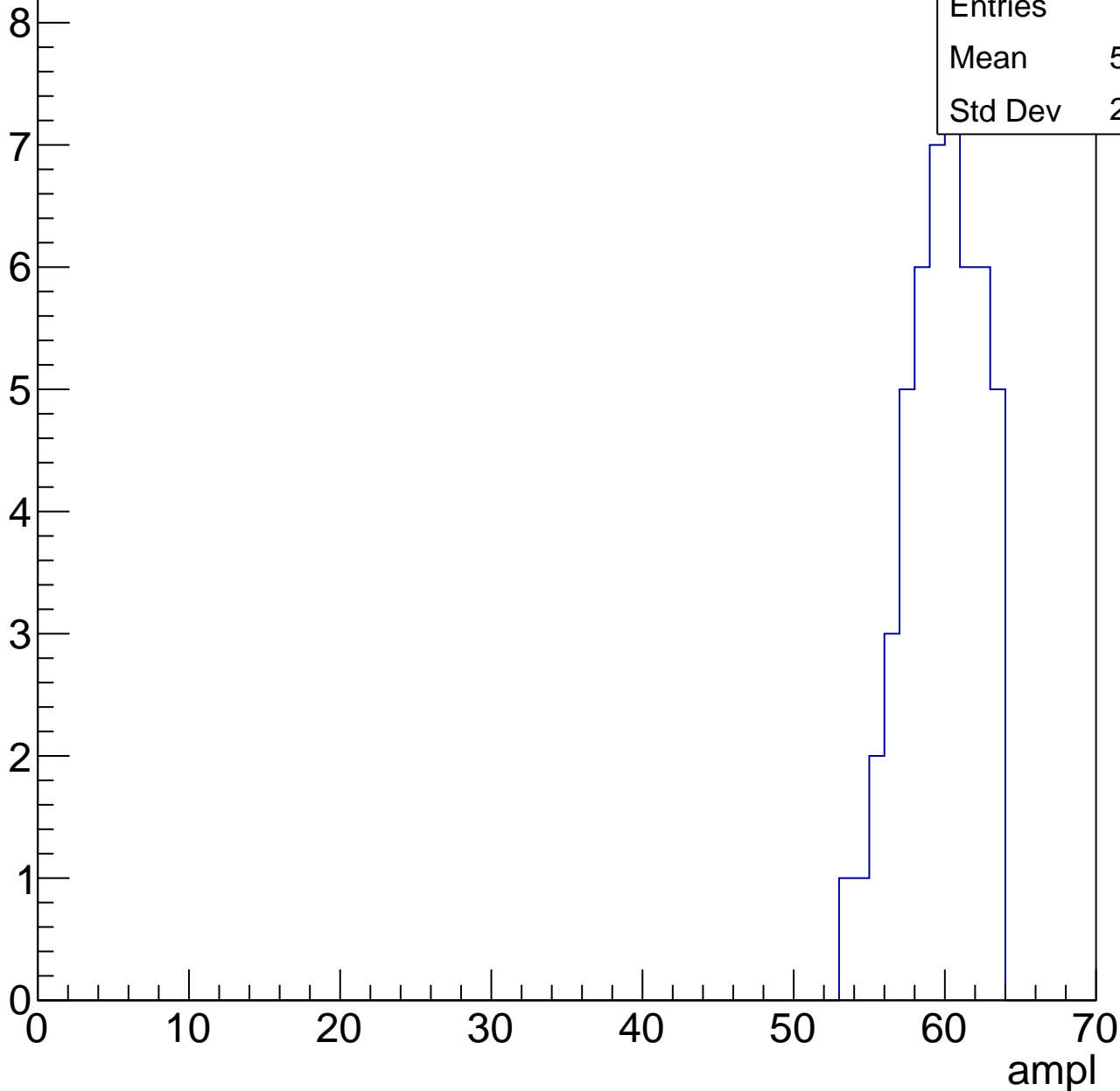


# B1L101S, U3-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	59.28
Std Dev	2.482

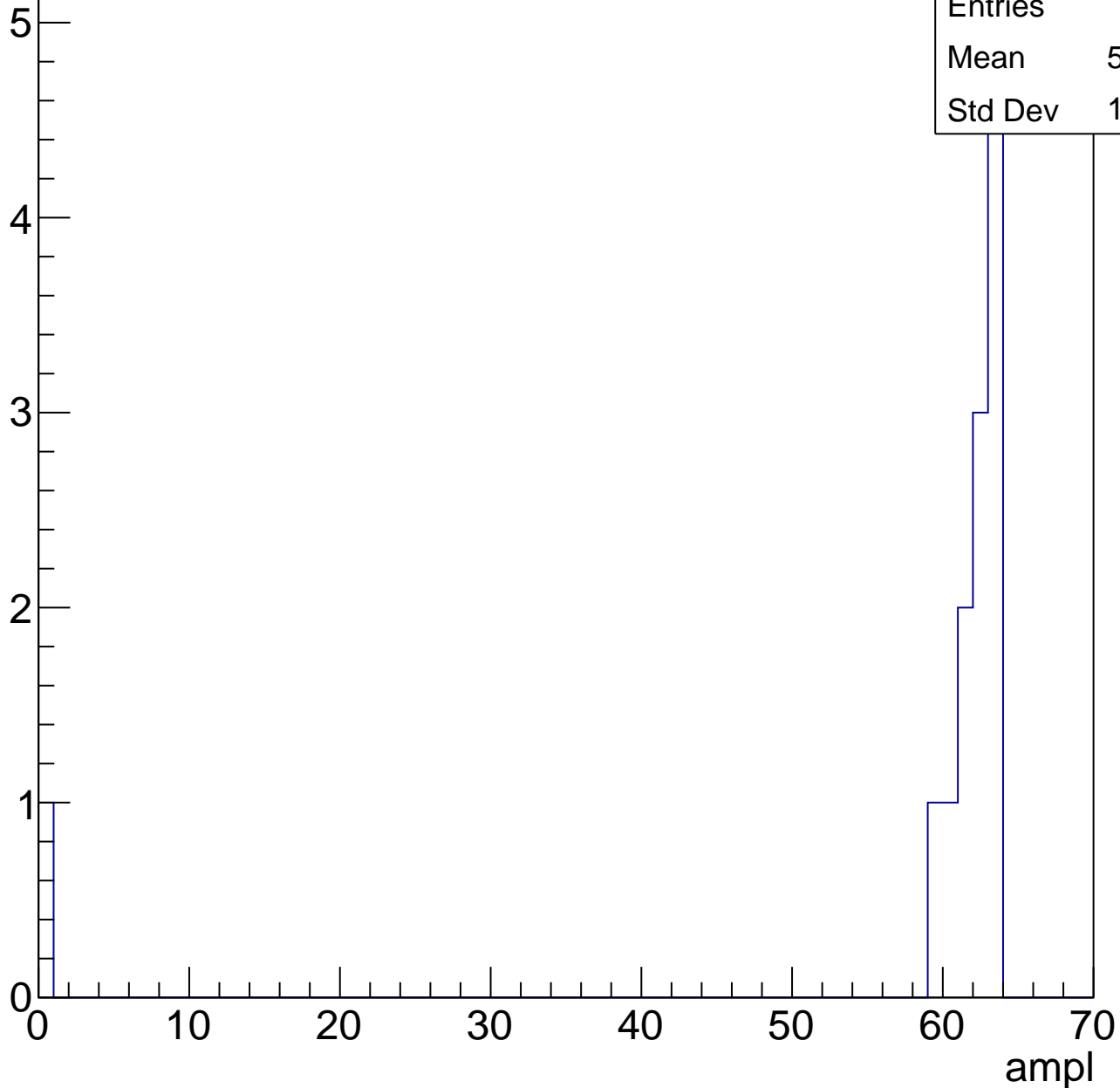


# B1L101S, U3-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	13
Mean	57.08
Std Dev	16.52





# B1L101S, U3-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch9, adc0

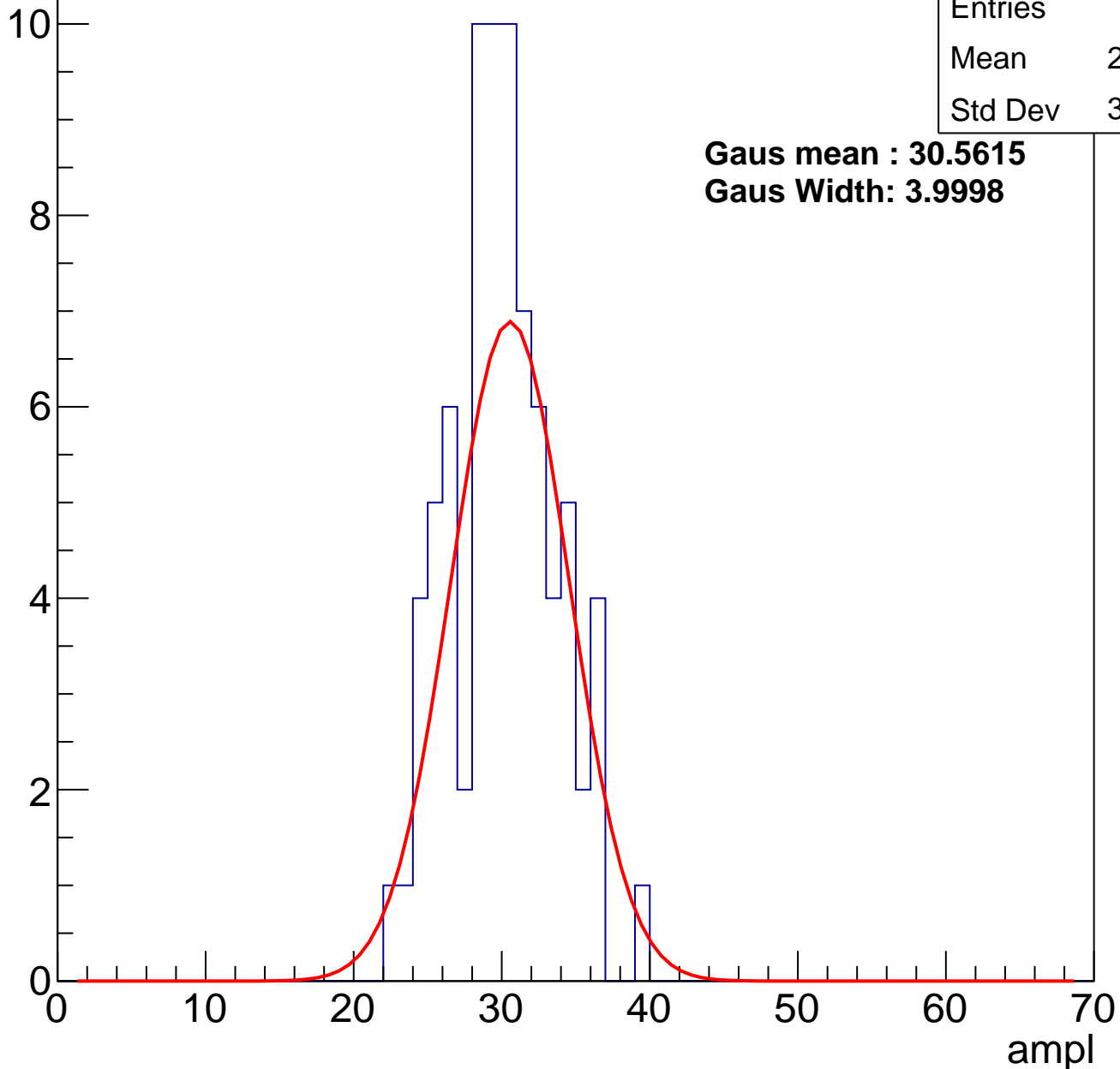
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	78
Mean	29.62
Std Dev	3.502

**Gaus mean : 30.5615**

**Gaus Width: 3.9998**

Entry



# B1L101S, U3-ch9, adc1

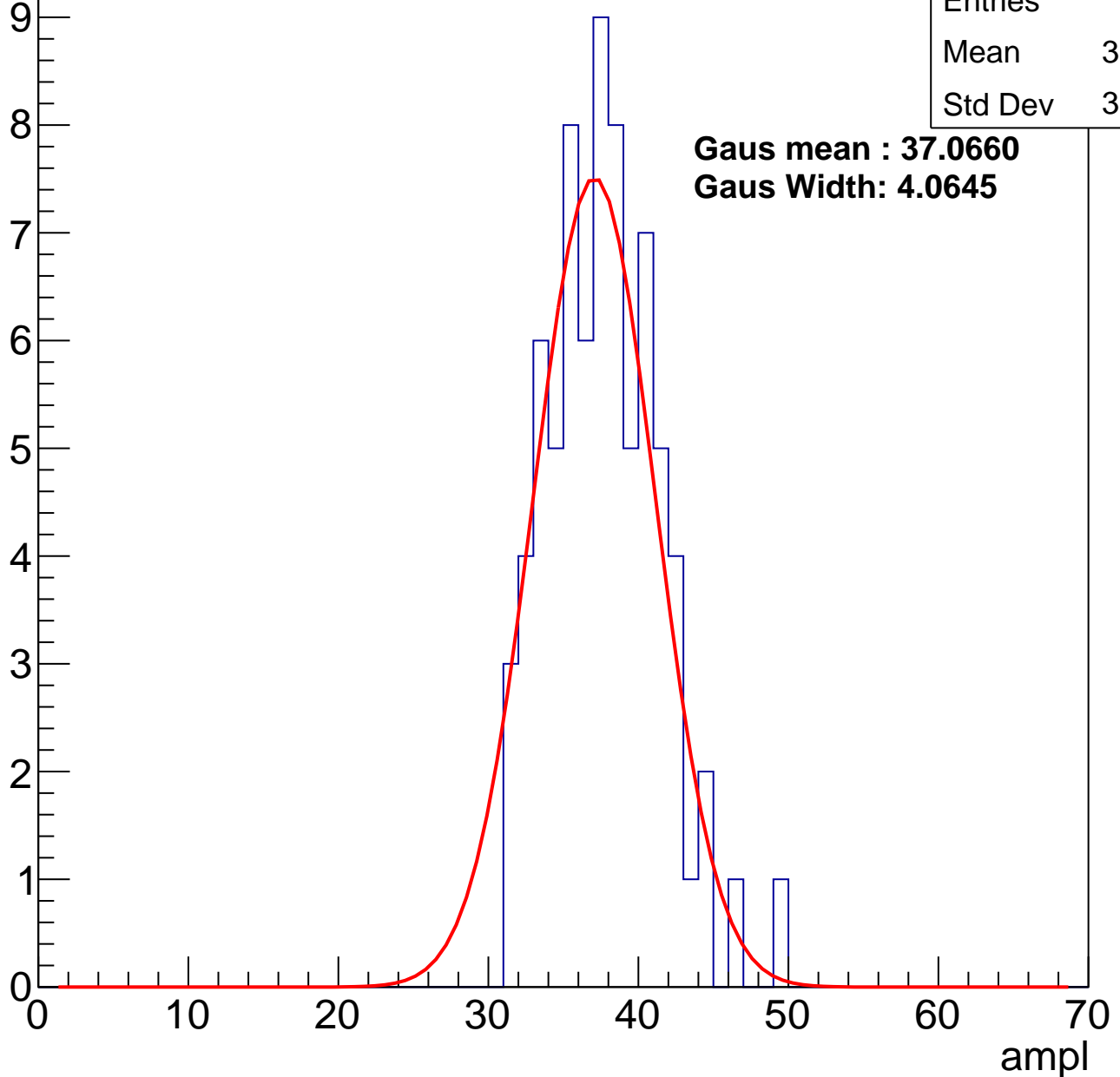
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	37.28
Std Dev	3.672

**Gaus mean : 37.0660**

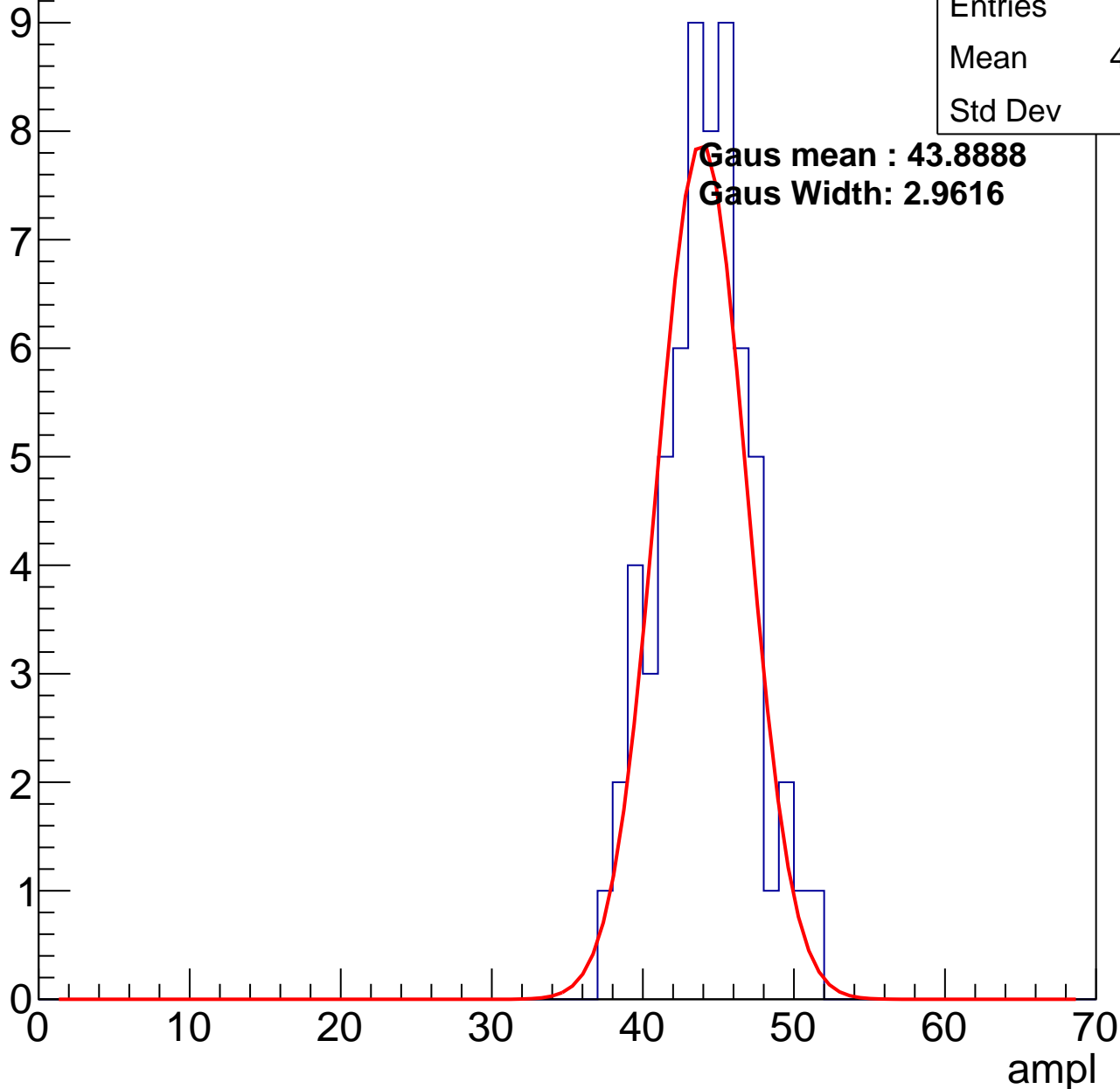
**Gaus Width: 4.0645**



# B1L101S, U3-ch9, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

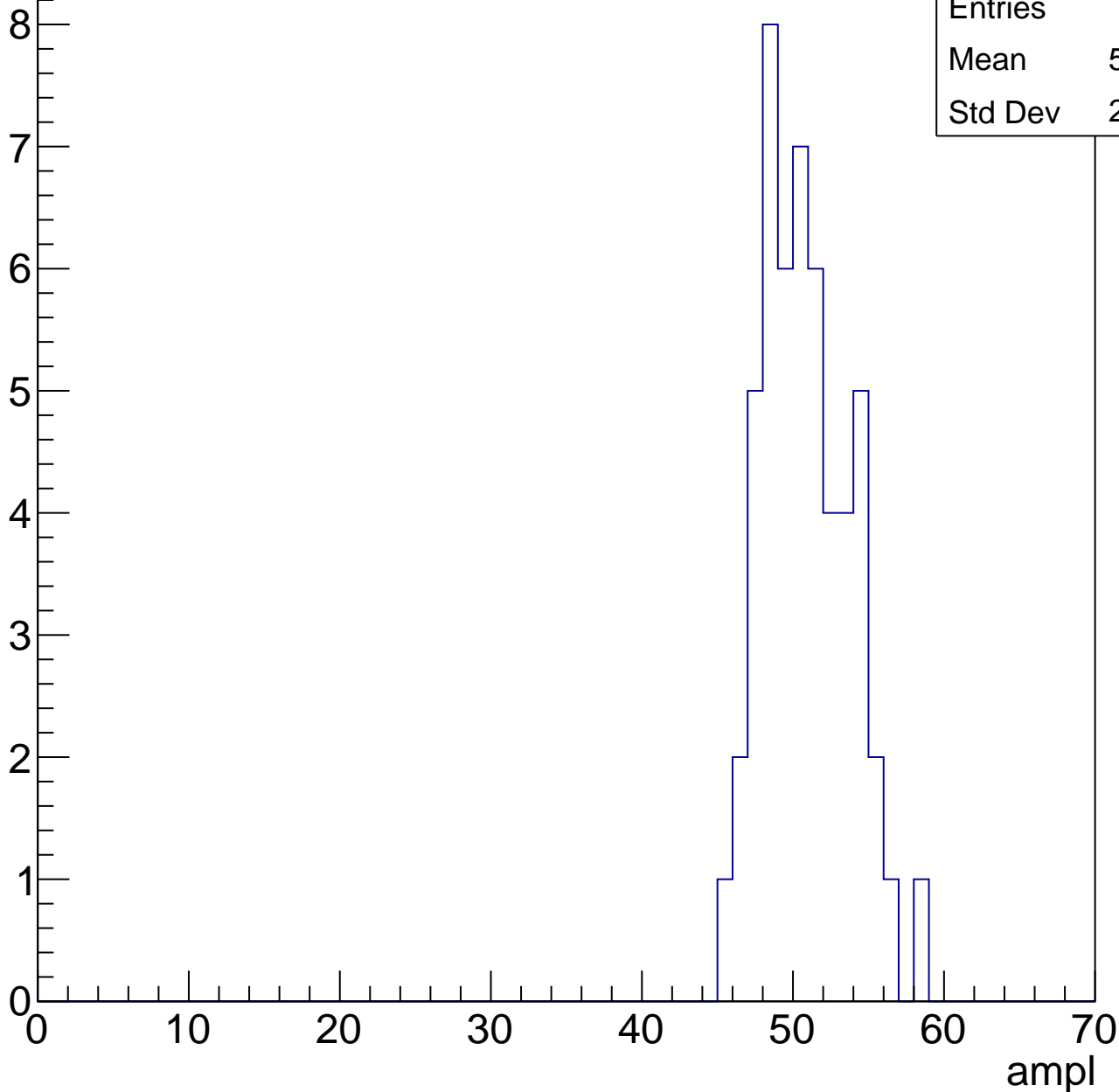


# B1L101S, U3-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

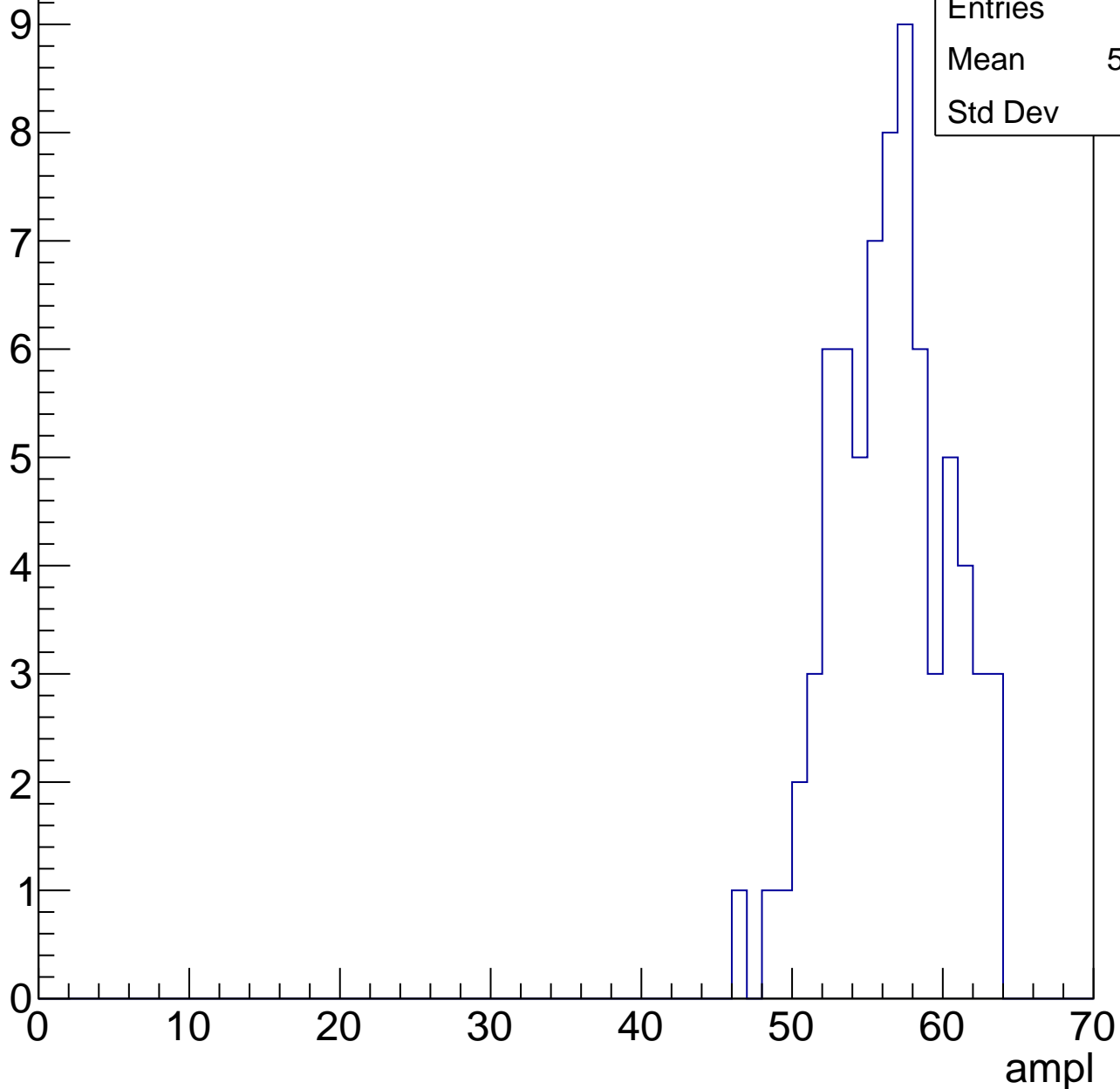
Entries	52
Mean	50.38
Std Dev	2.843



# B1L101S, U3-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

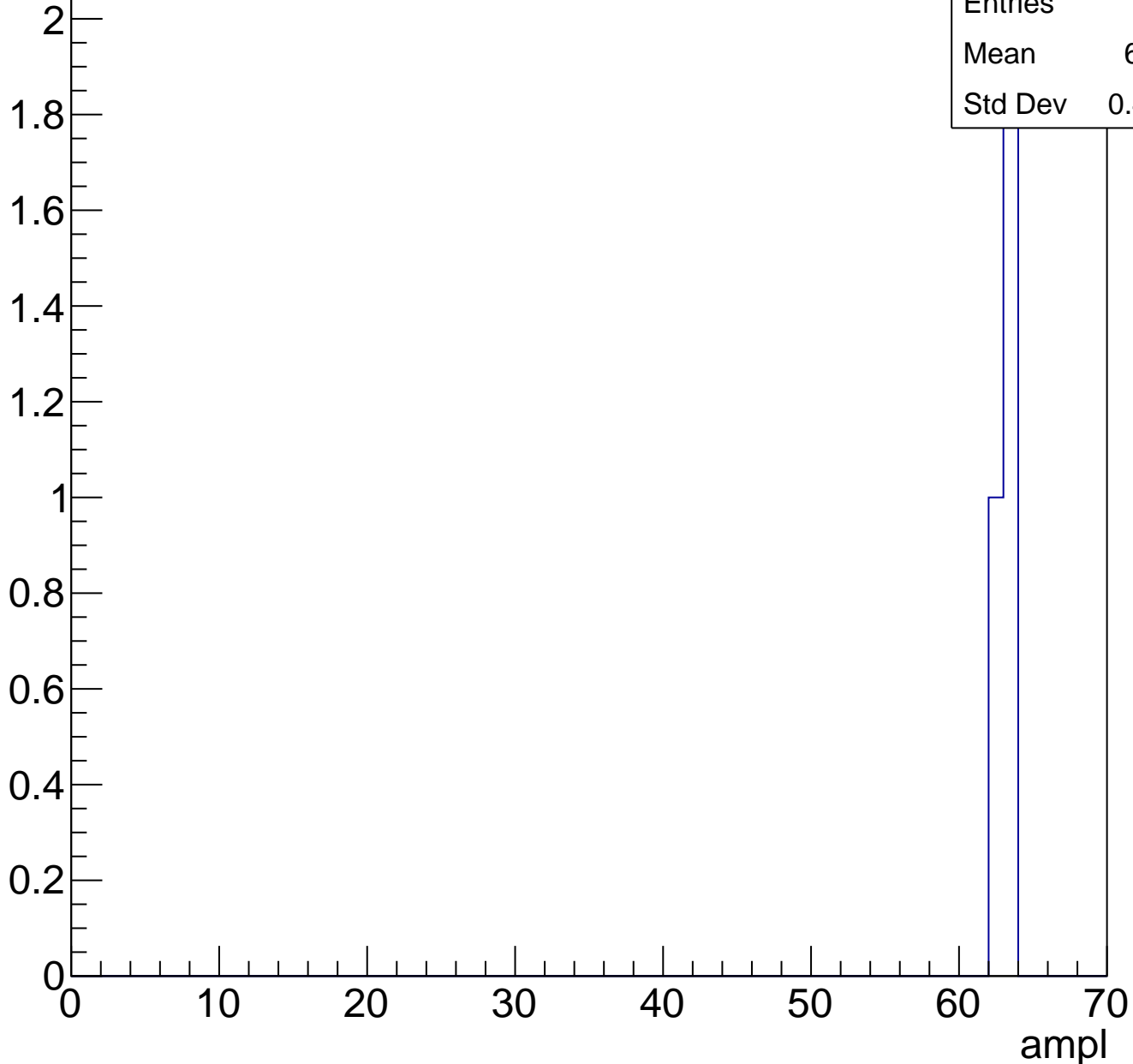




# B1L101S, U3-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	21
Std Dev	0

ampl

0 10 20 30 40 50 60 70

# B1L101S, U3-ch10, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	65
Mean	27.58
Std Dev	5.881

**Gaus mean : 29.2039**

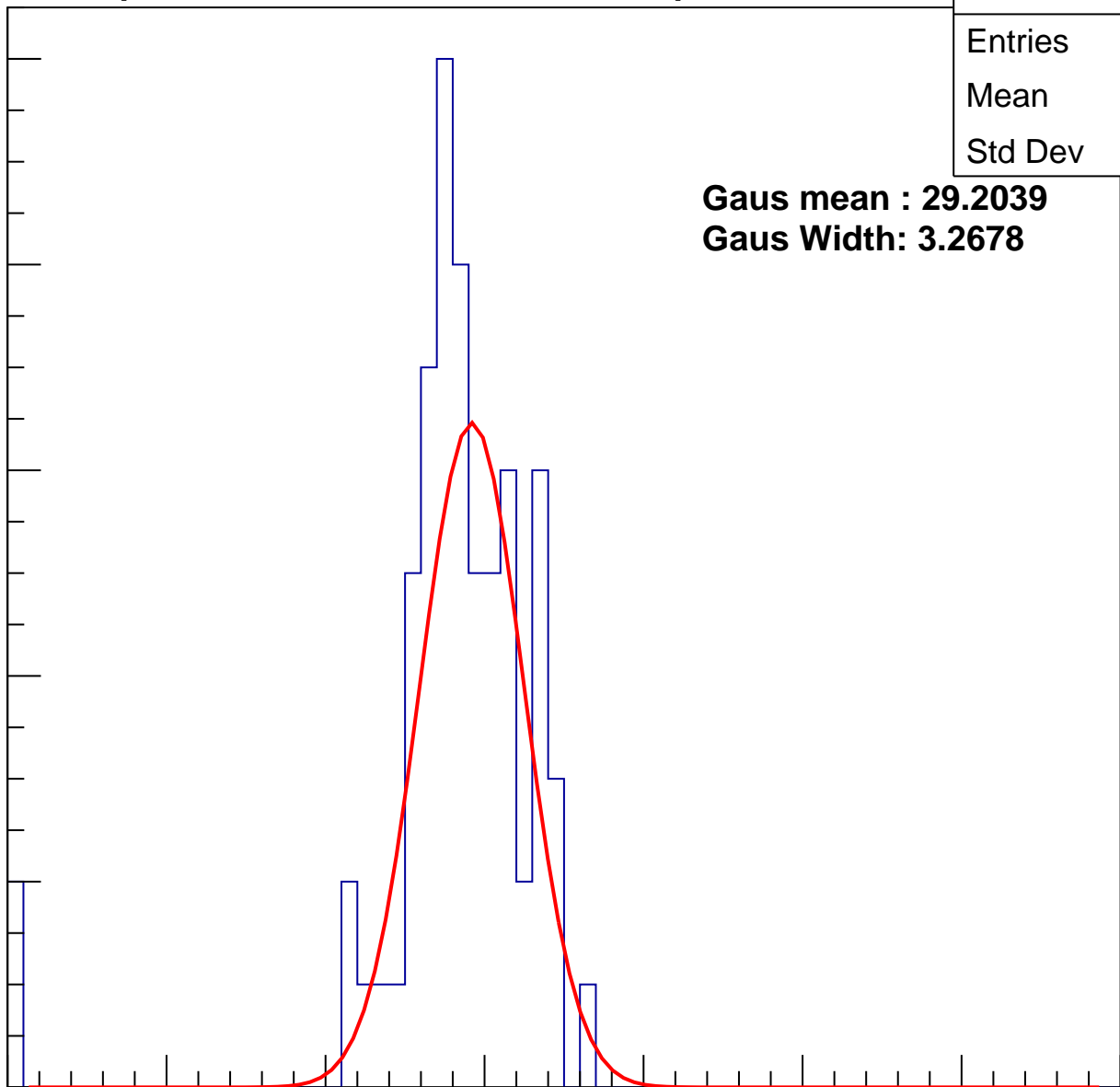
**Gaus Width: 3.2678**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U3-ch10, adc1

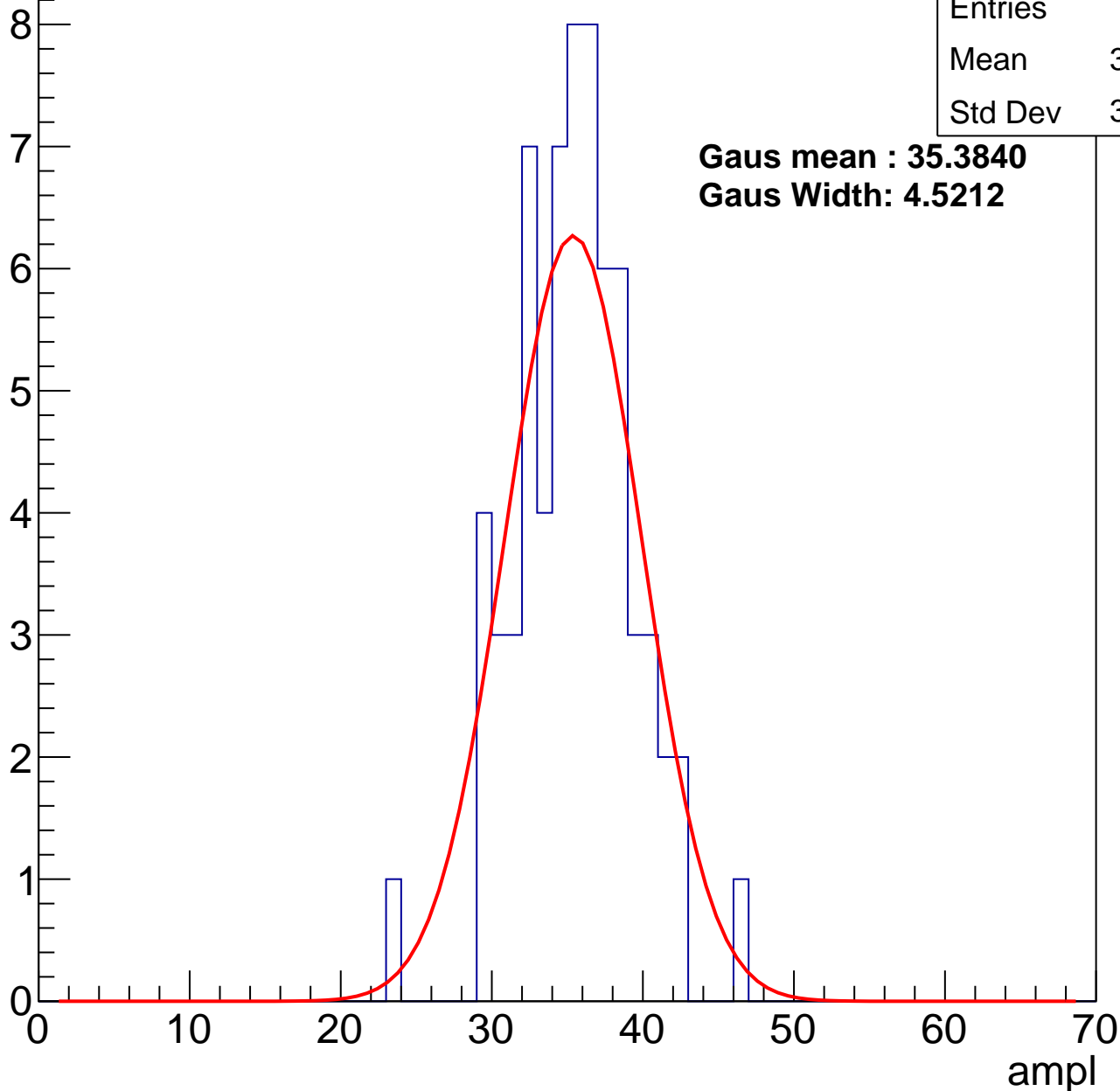
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	35.04
Std Dev	3.829

**Gaus mean : 35.3840**

**Gaus Width: 4.5212**

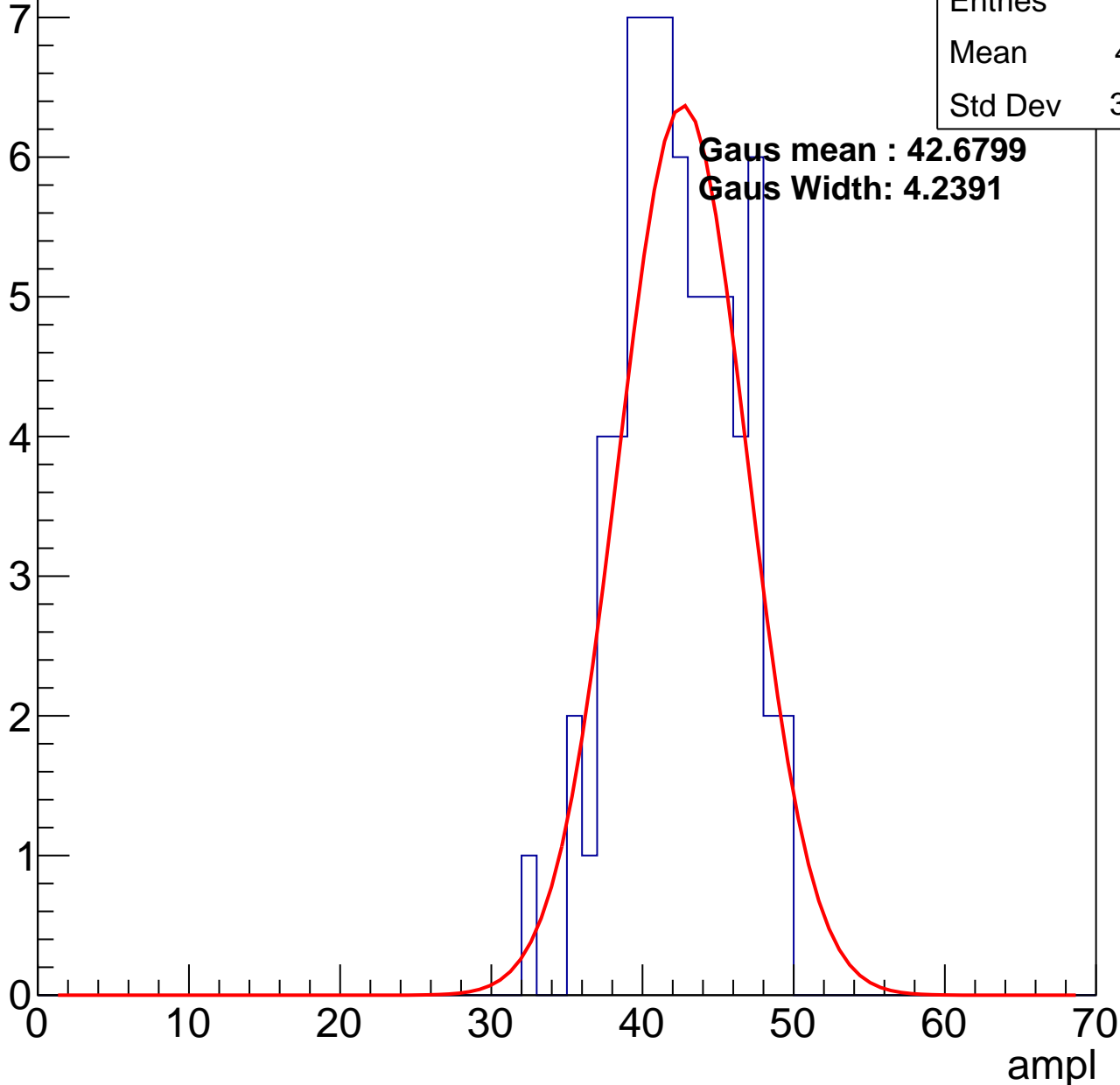


# B1L101S, U3-ch10, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	41.91
Std Dev	3.737

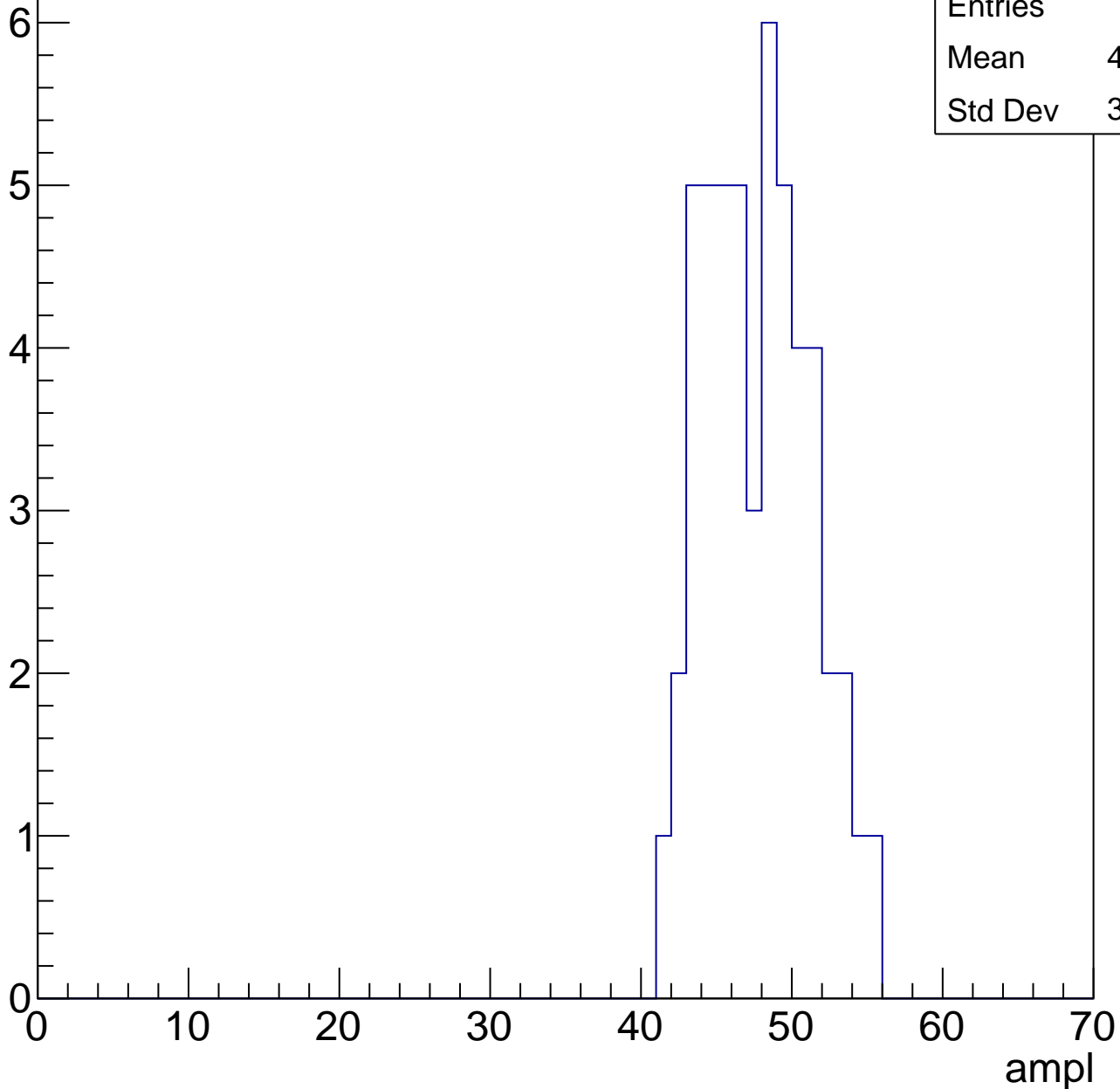


# B1L101S, U3-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	47.29
Std Dev	3.409

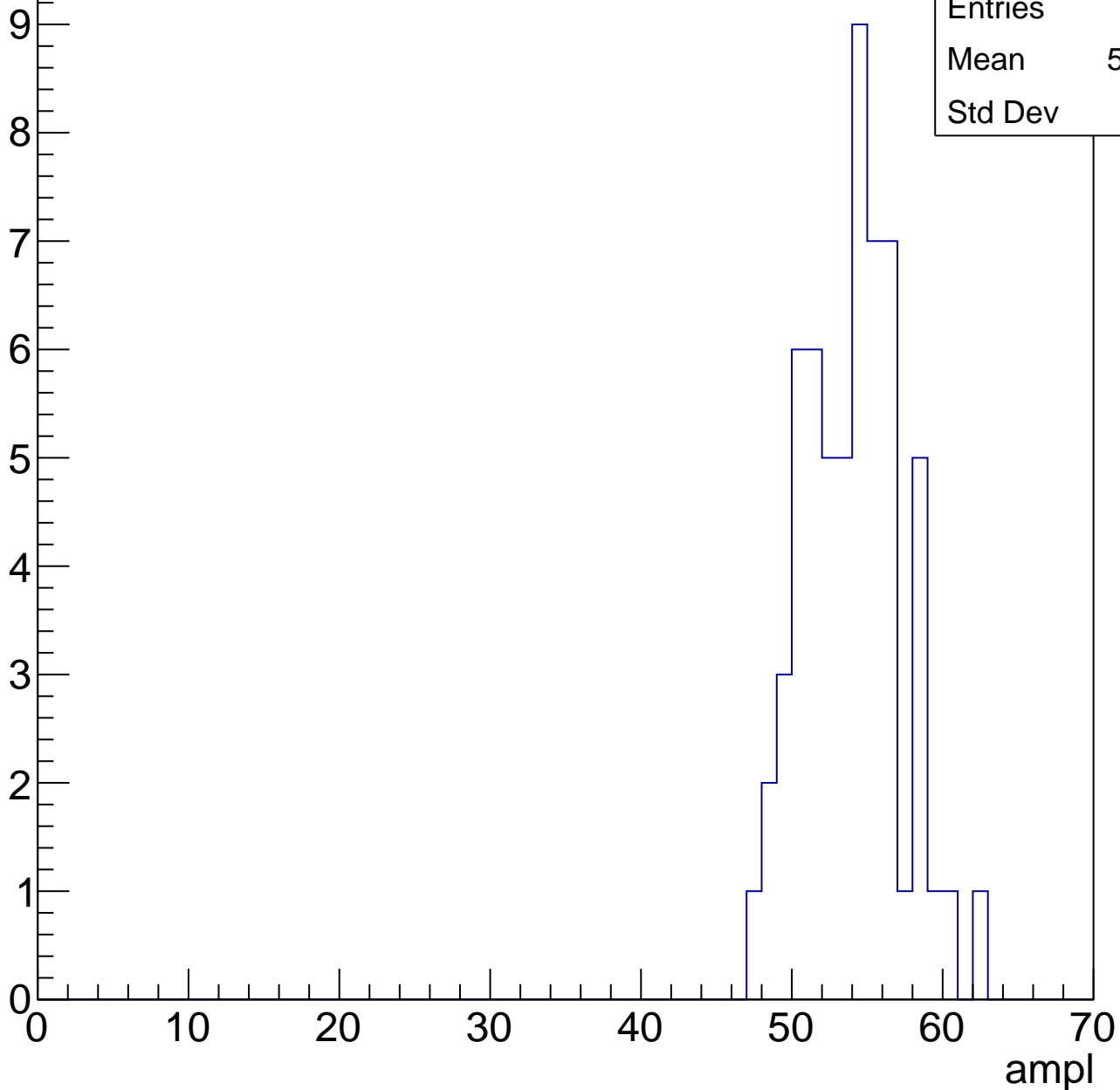


# B1L101S, U3-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

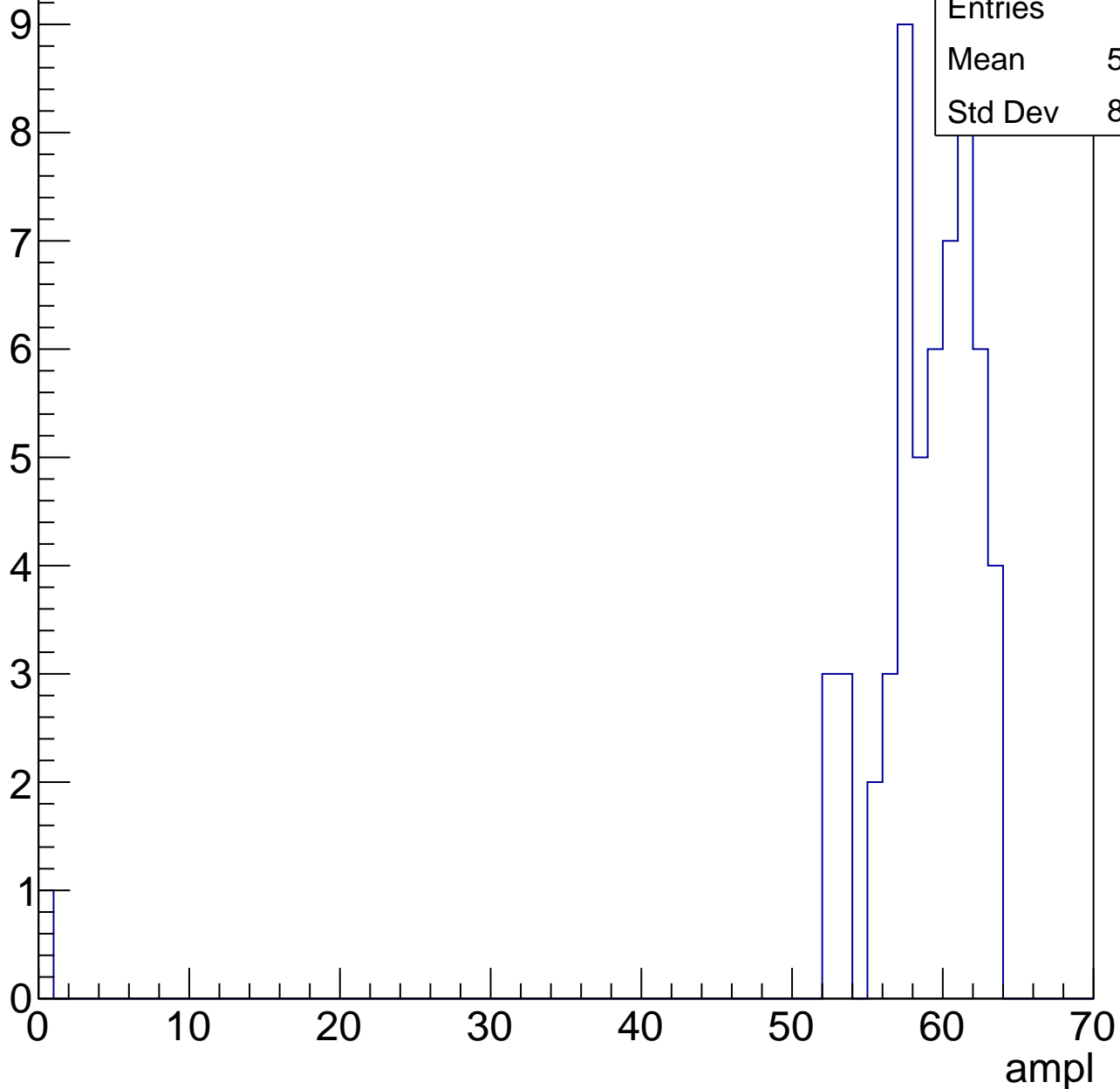
Entries	60
Mean	53.53
Std Dev	3.18



# B1L101S, U3-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

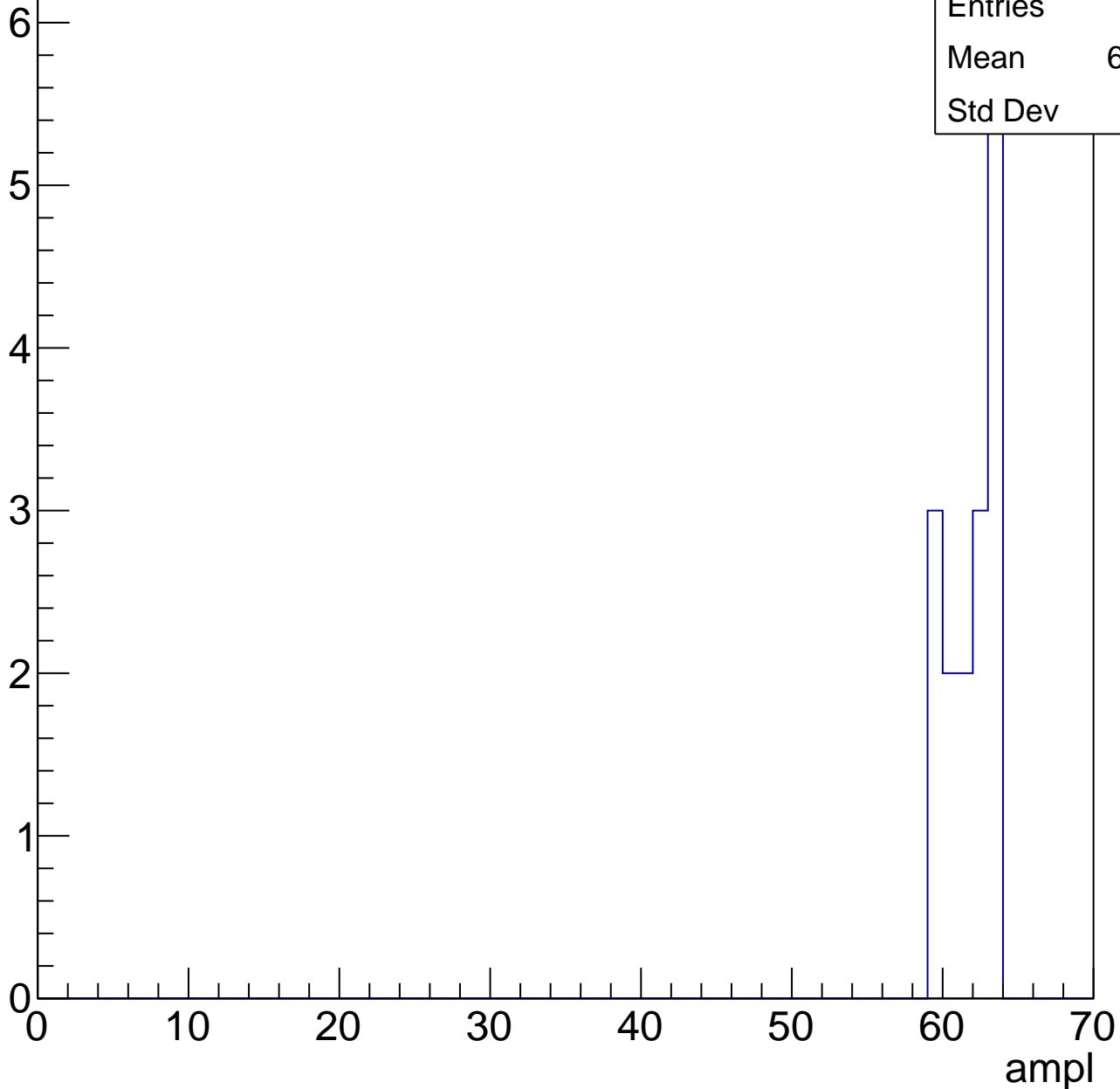


# B1L101S, U3-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	16
Mean	61.44
Std Dev	1.54





# B1L101S, U3-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch11, adc0

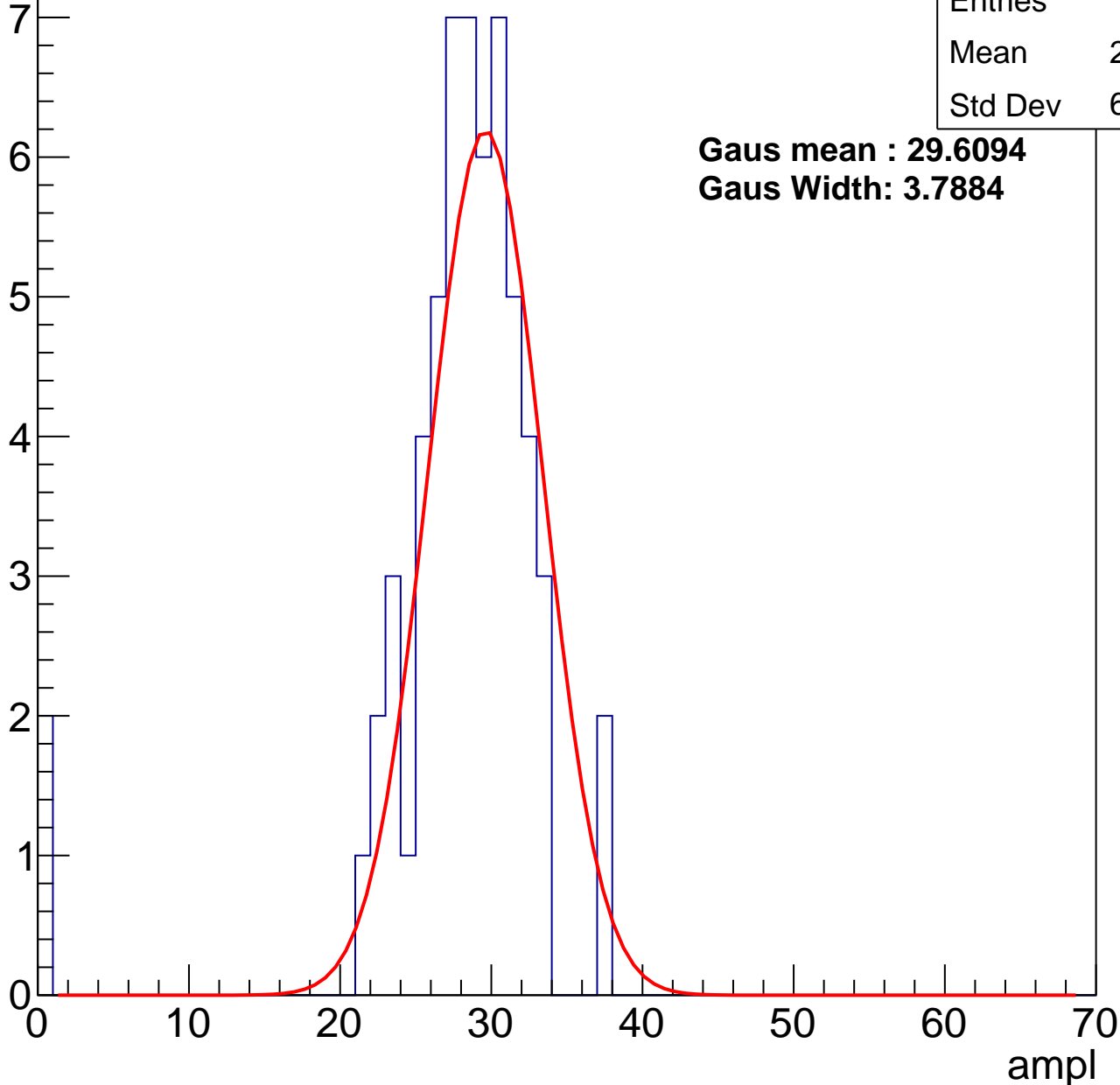
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	27.34
Std Dev	6.103

**Gaus mean : 29.6094**

**Gaus Width: 3.7884**



# B1L101S, U3-ch11, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	66
Mean	34.41
Std Dev	5.222

**Gaus mean : 35.2421**

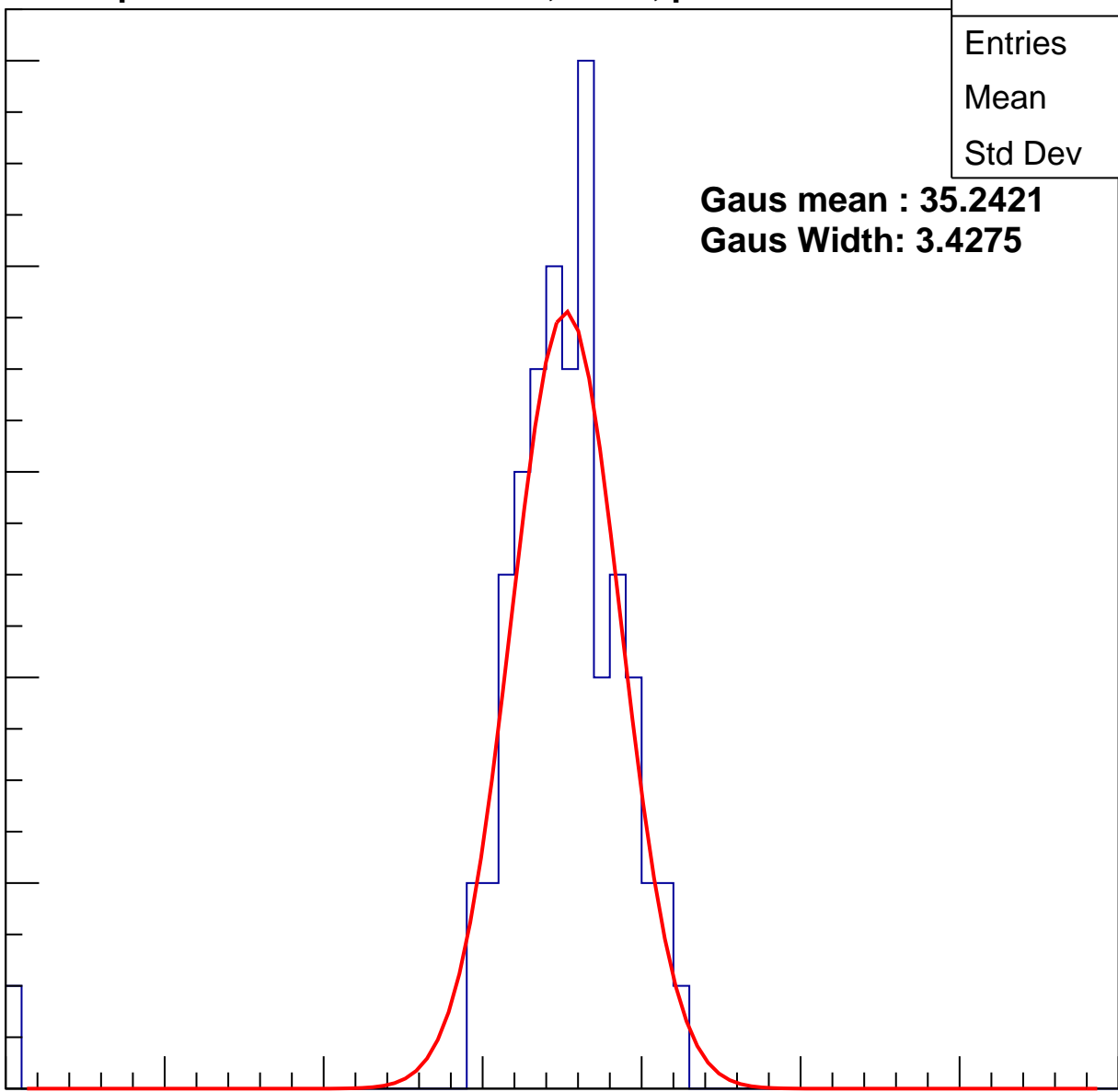
**Gaus Width: 3.4275**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U3-ch11, adc2

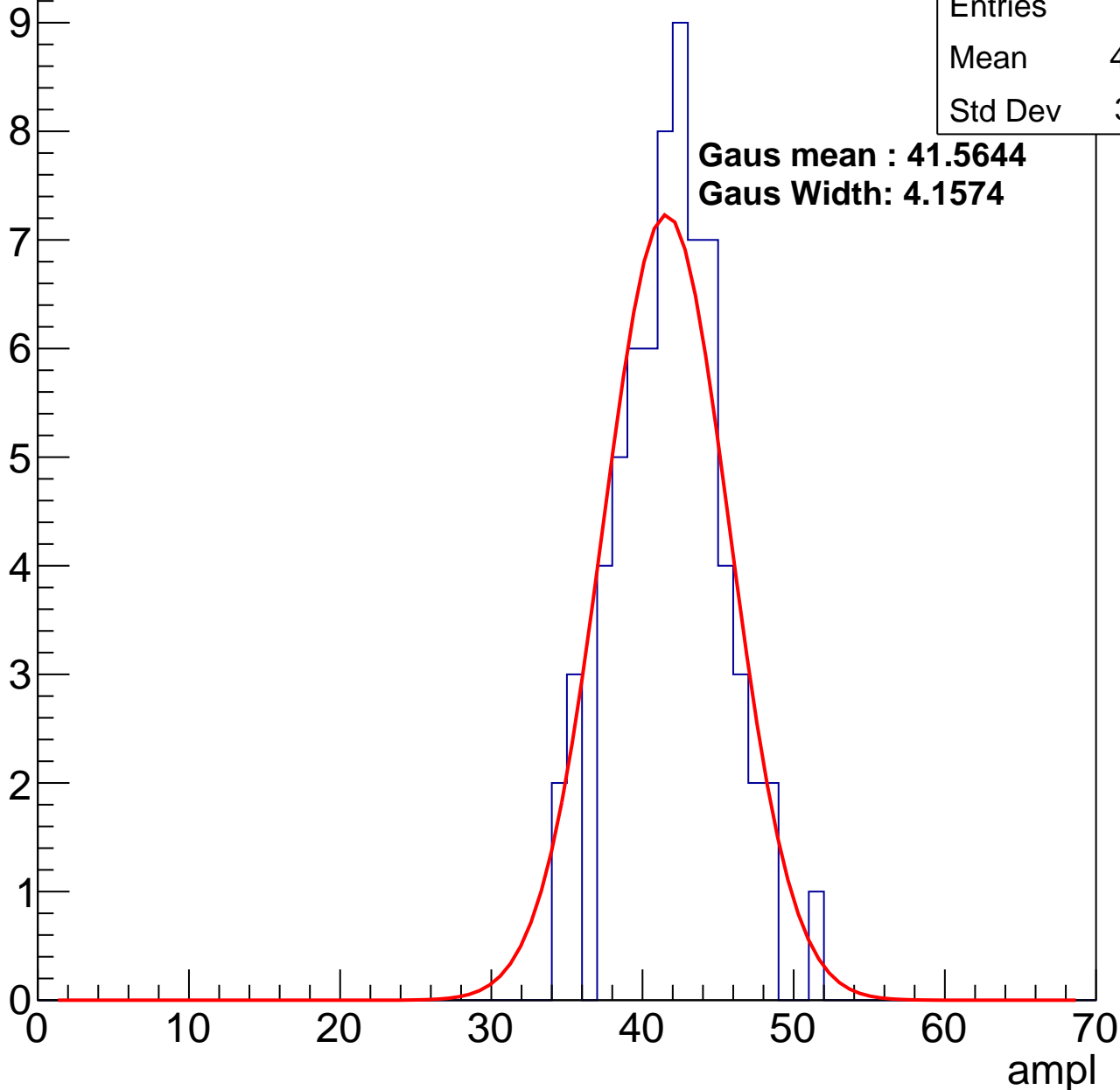
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	41.43
Std Dev	3.491

**Gaus mean : 41.5644**

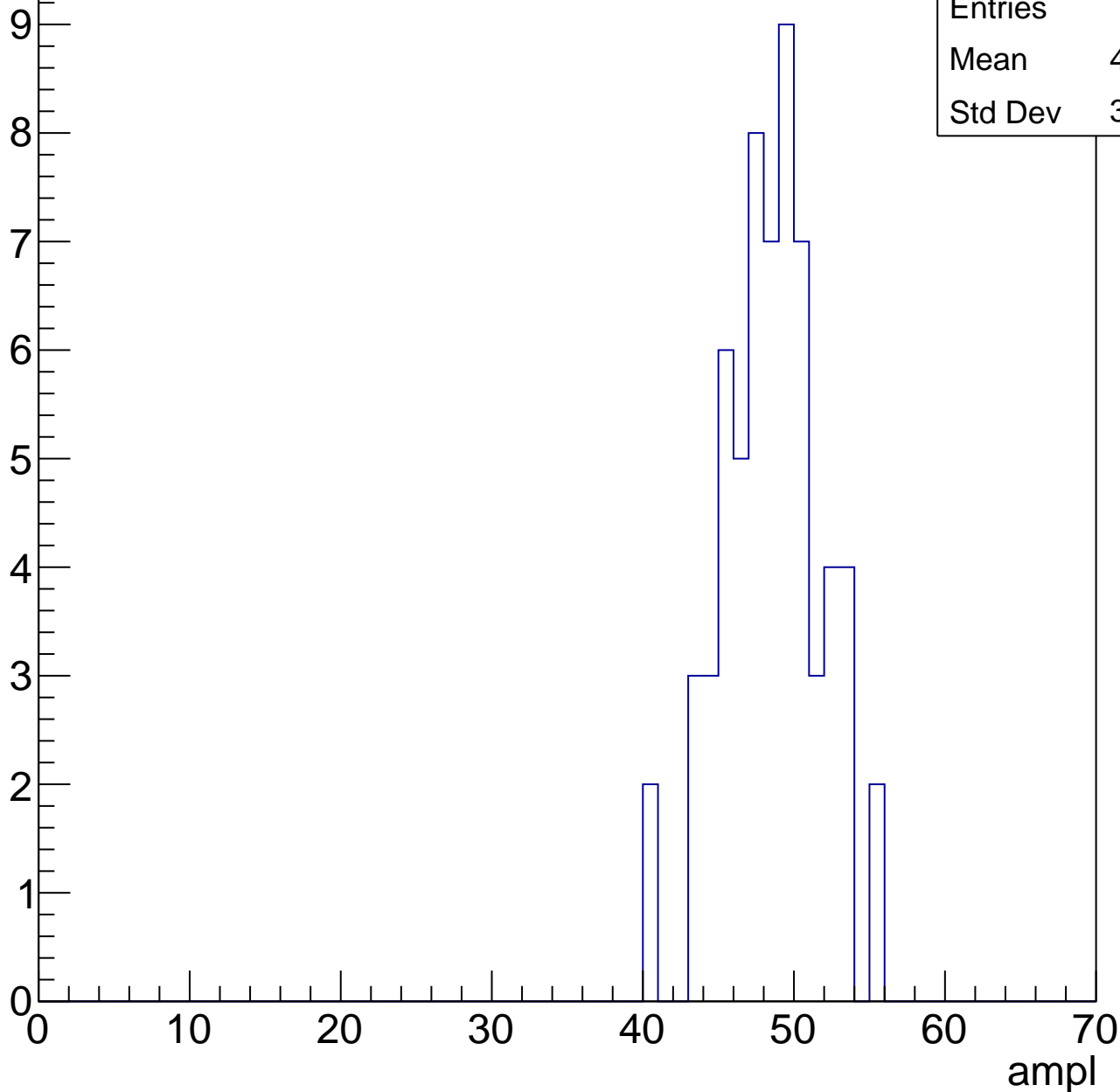
**Gaus Width: 4.1574**



# B1L101S, U3-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	59
Mean	53.92
Std Dev	3.071

Entry

10

8

6

4

2

0

0

10

20

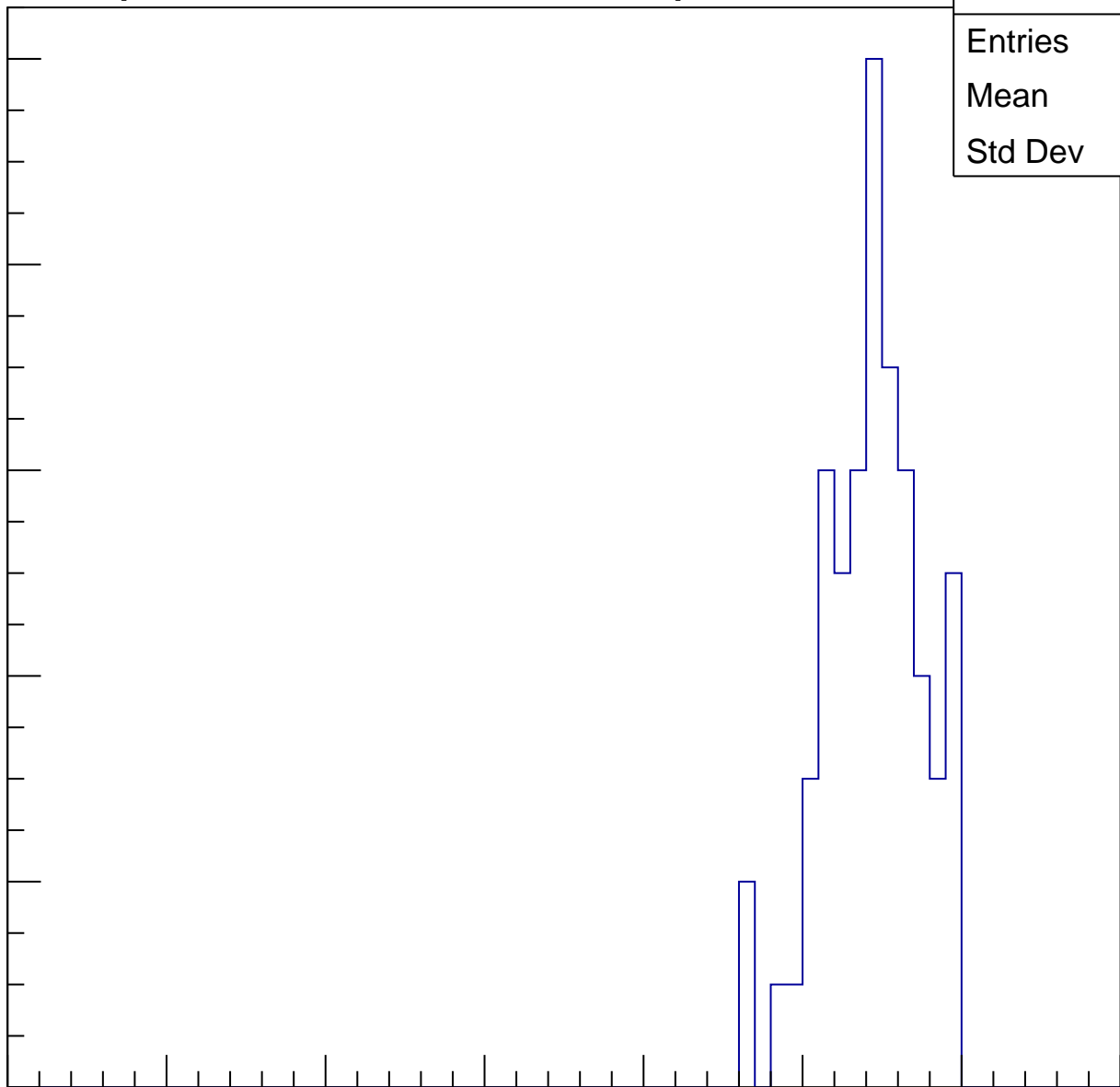
30

40

50

60

ampl

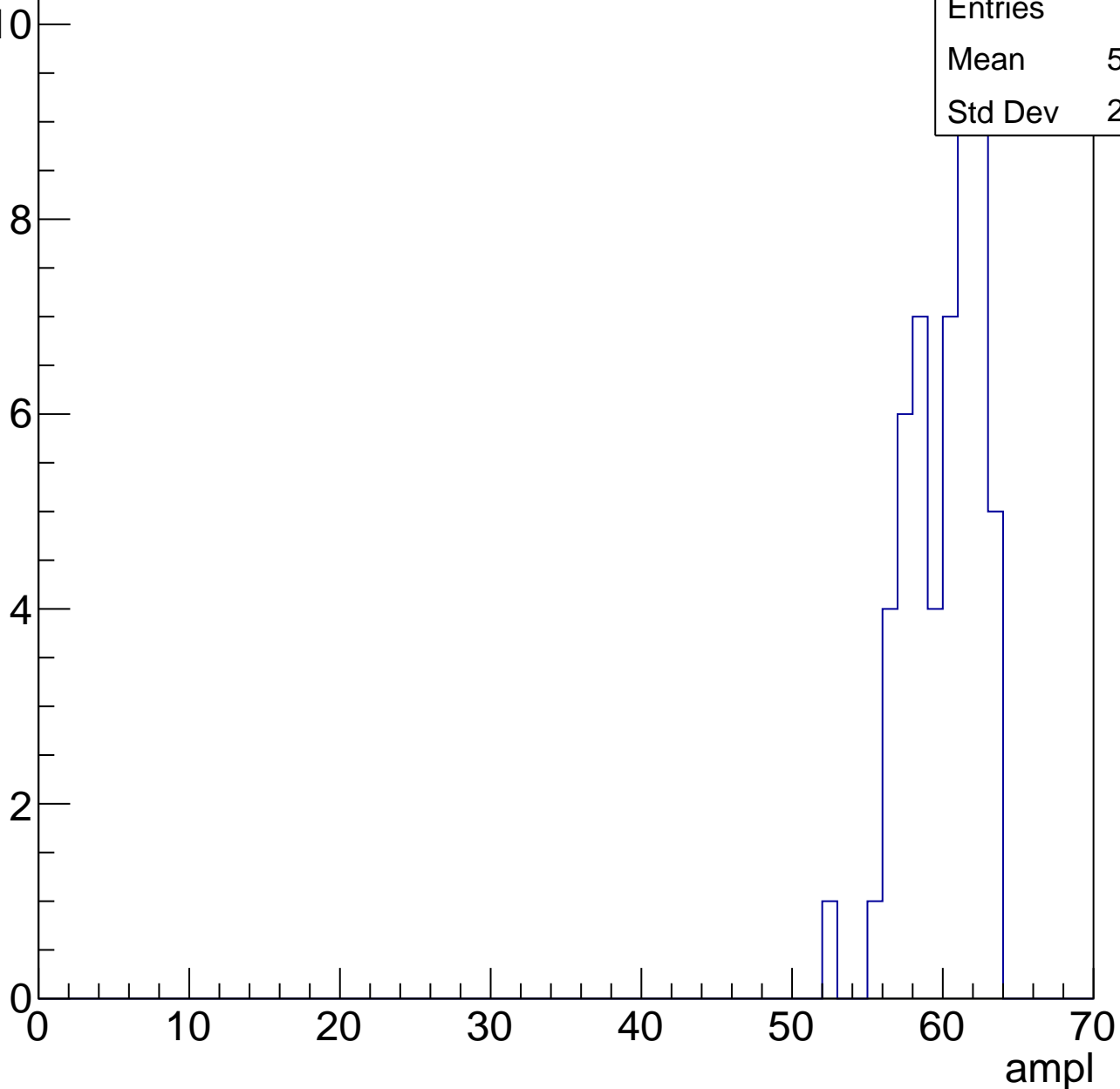


# B1L101S, U3-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	59.59
Std Dev	2.438

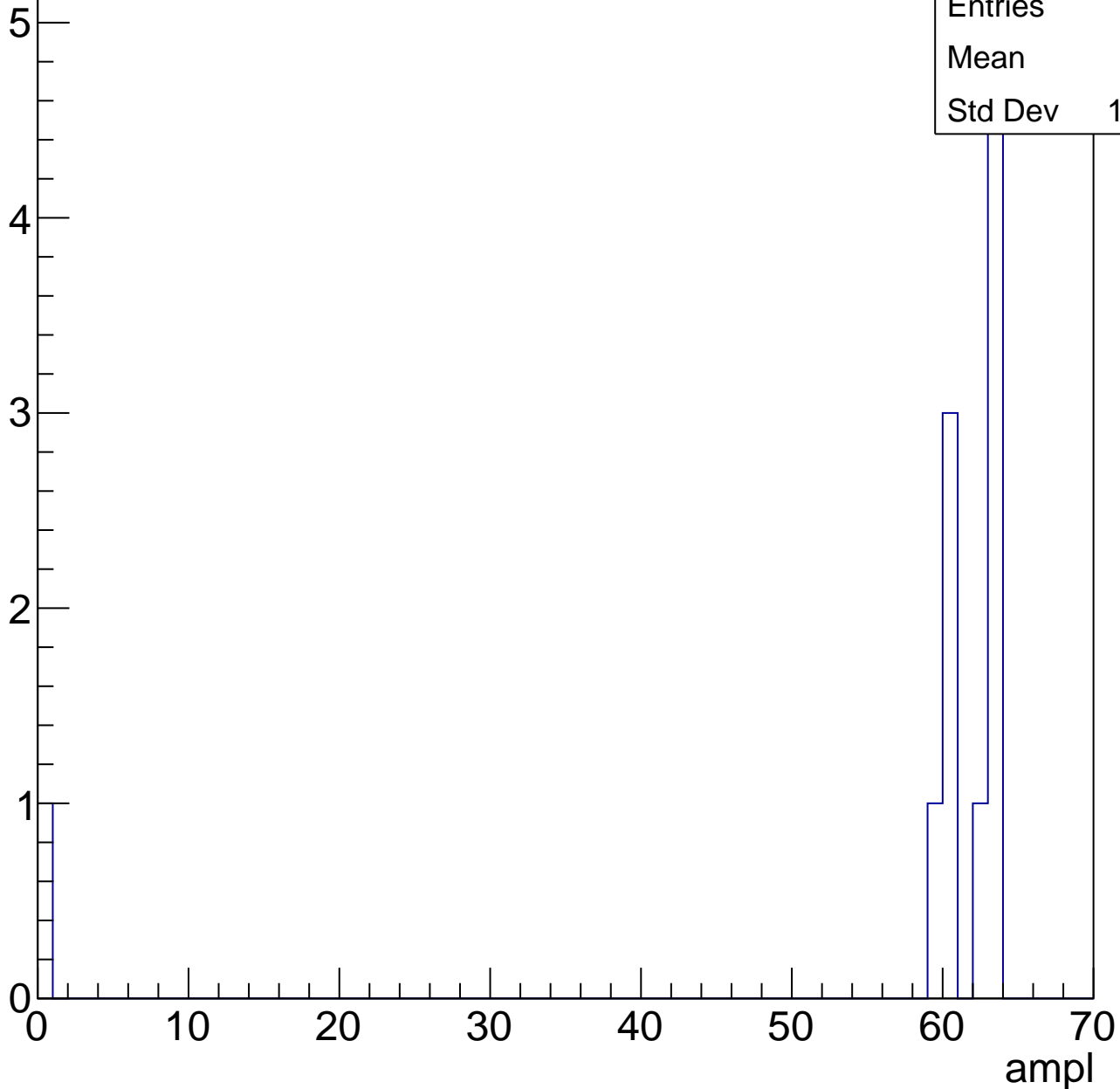


# B1L101S, U3-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	11
Mean	56
Std Dev	17.77





# B1L101S, U3-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch12, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	74
Mean	28.28
Std Dev	3.47

**Gaus mean : 29.1772**

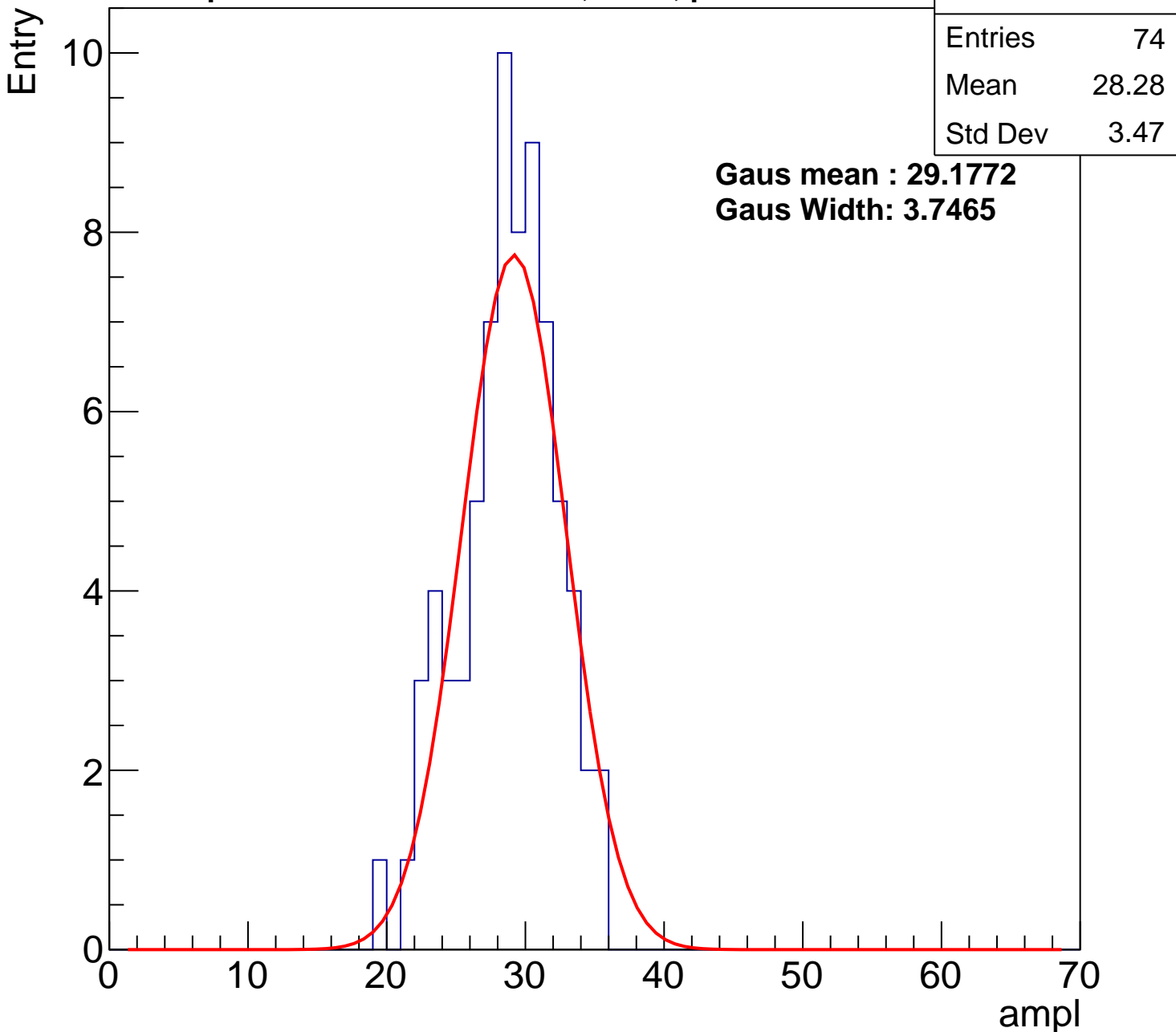
**Gaus Width: 3.7465**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U3-ch12, adc1

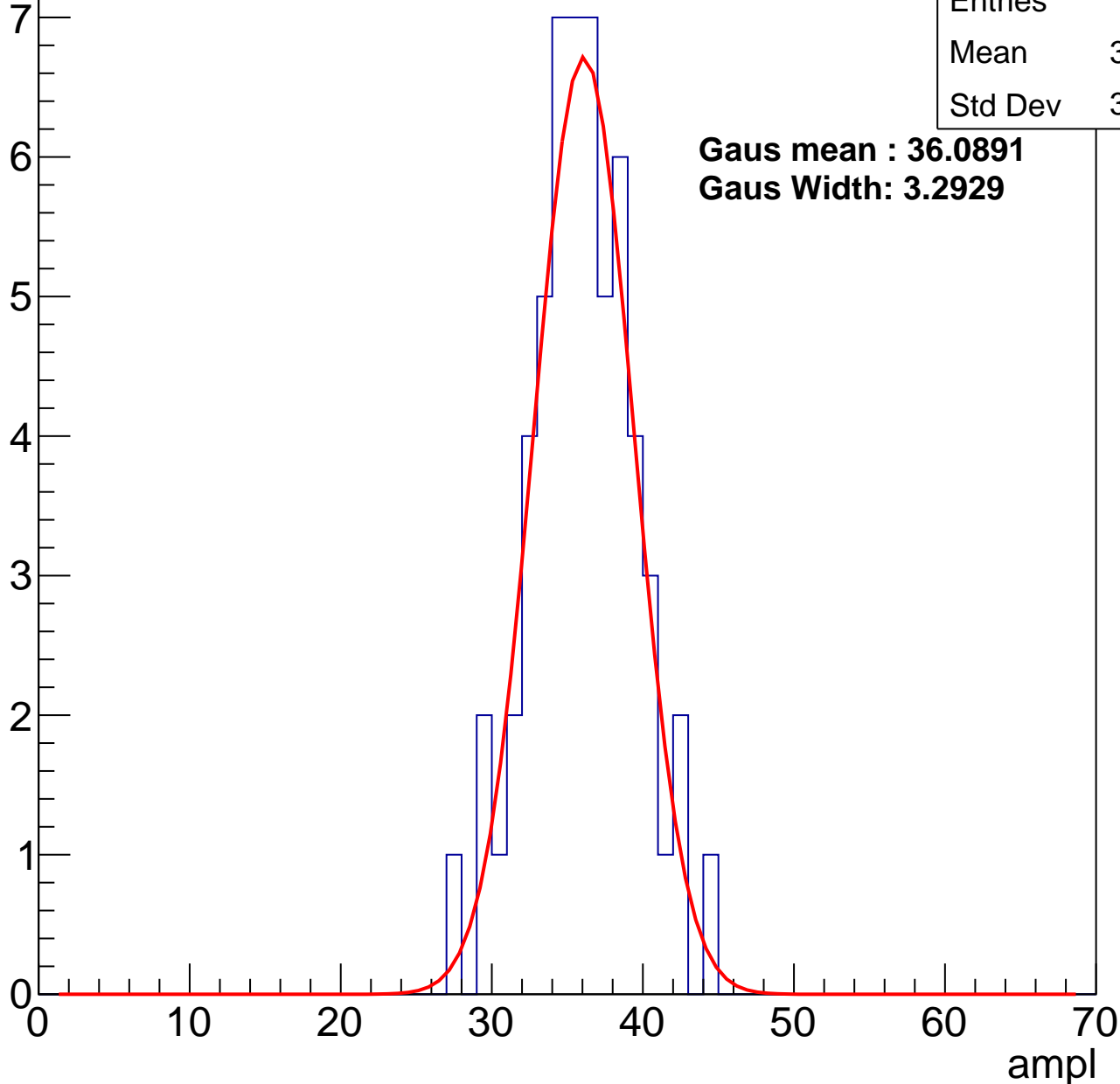
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	35.57
Std Dev	3.404

**Gaus mean : 36.0891**

**Gaus Width: 3.2929**



# B1L101S, U3-ch12, adc2

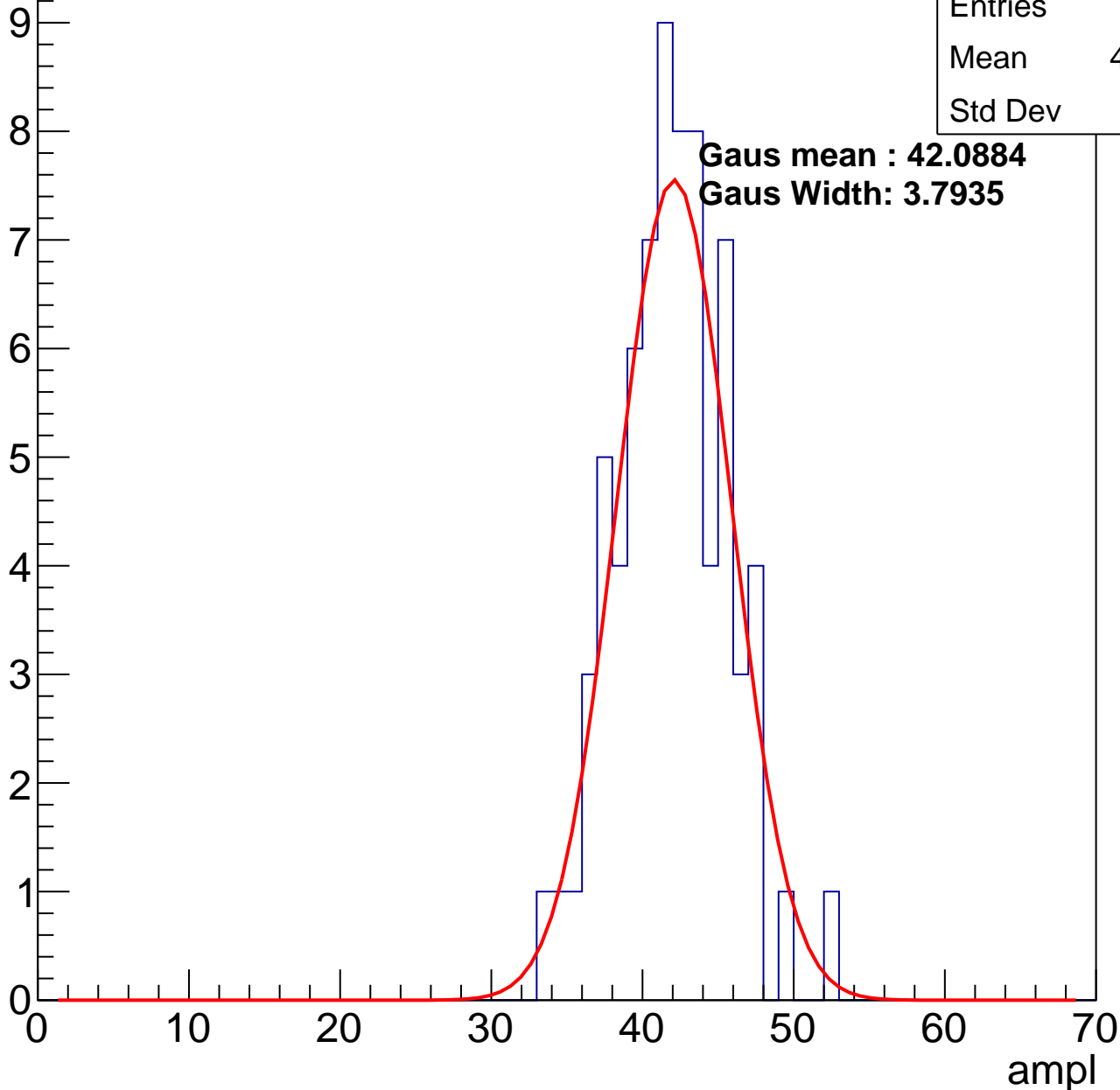
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	41.48
Std Dev	3.6

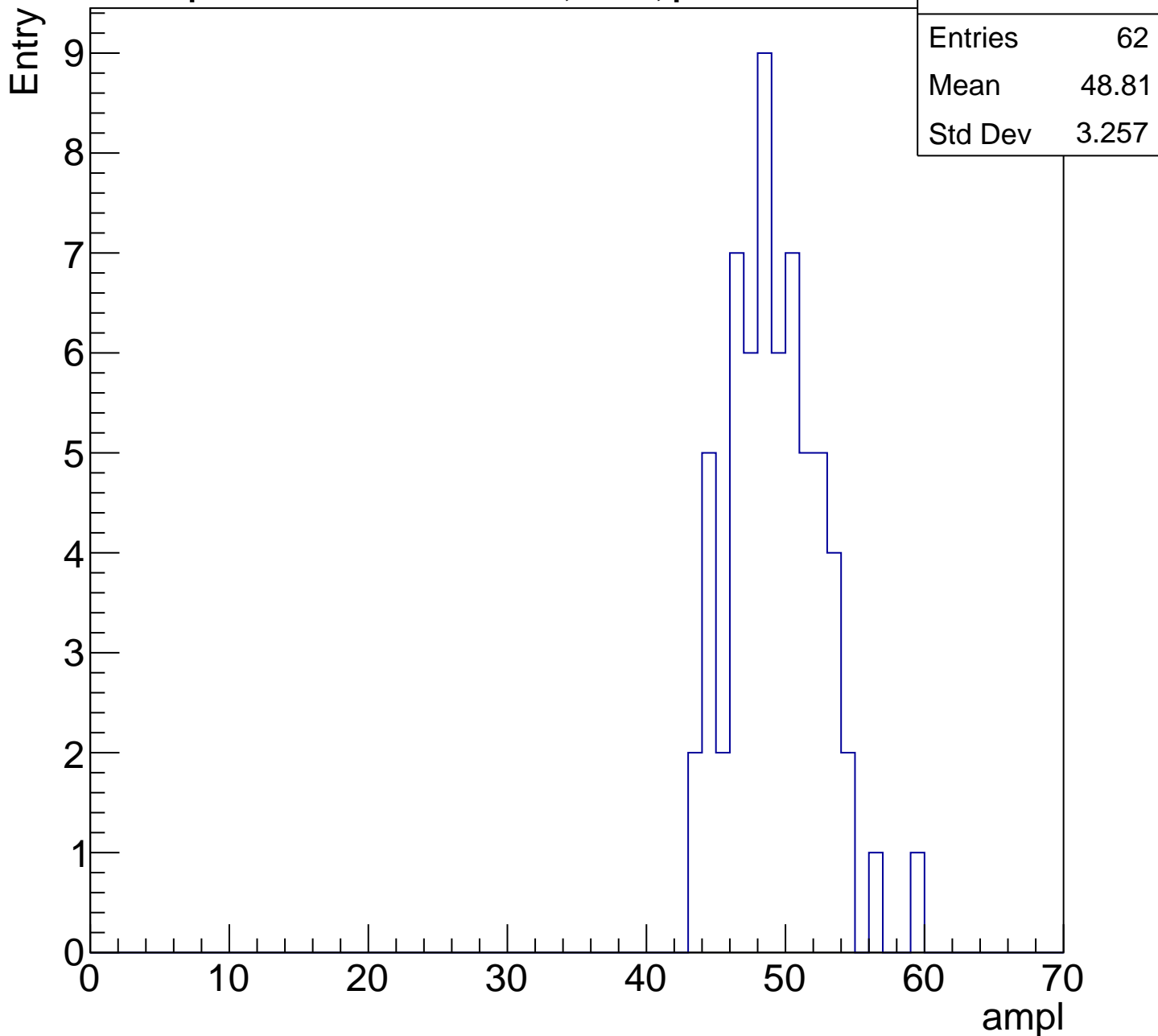
**Gaus mean : 42.0884**

**Gaus Width: 3.7935**



# B1L101S, U3-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

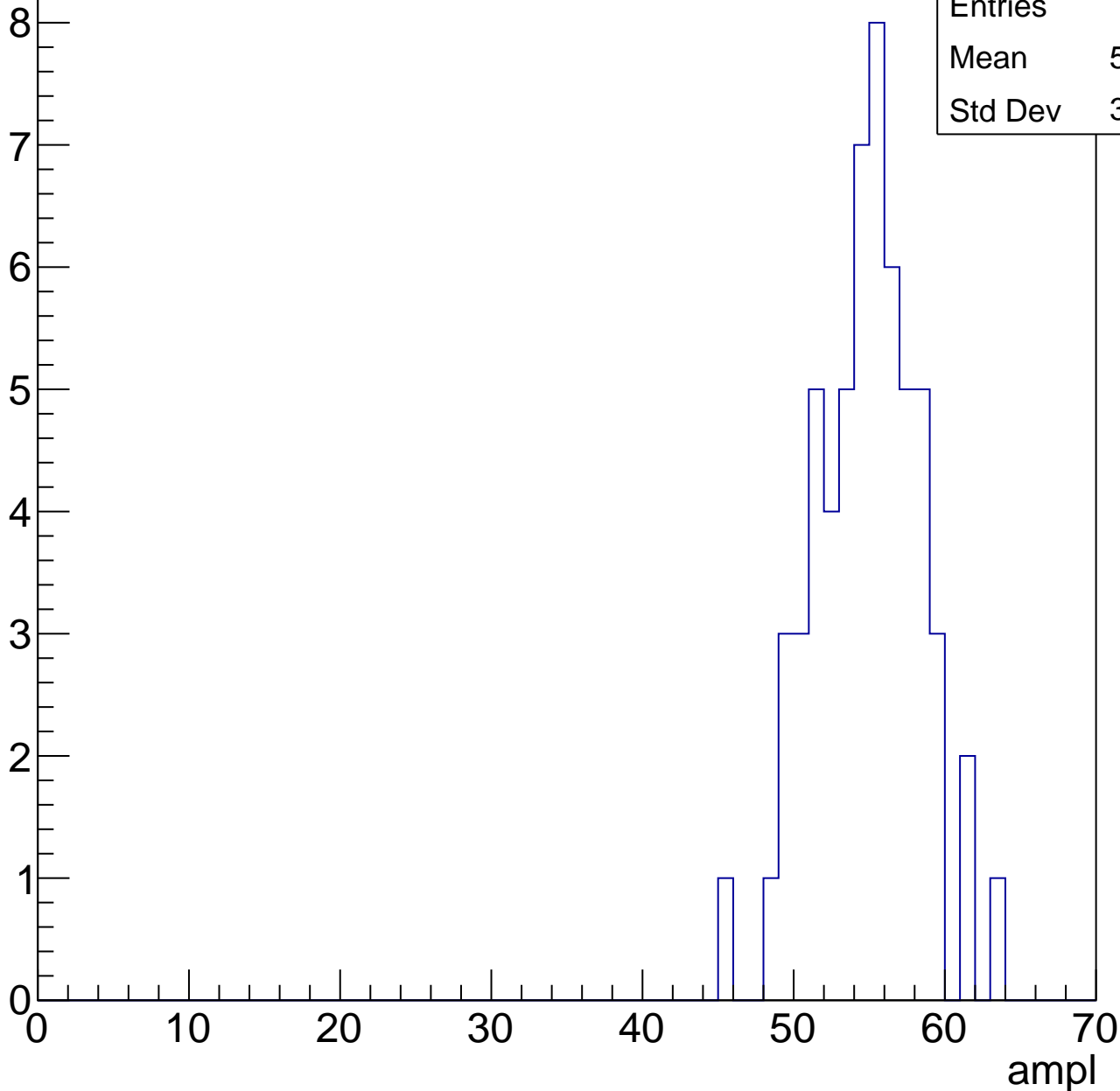


# B1L101S, U3-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	54.39
Std Dev	3.464

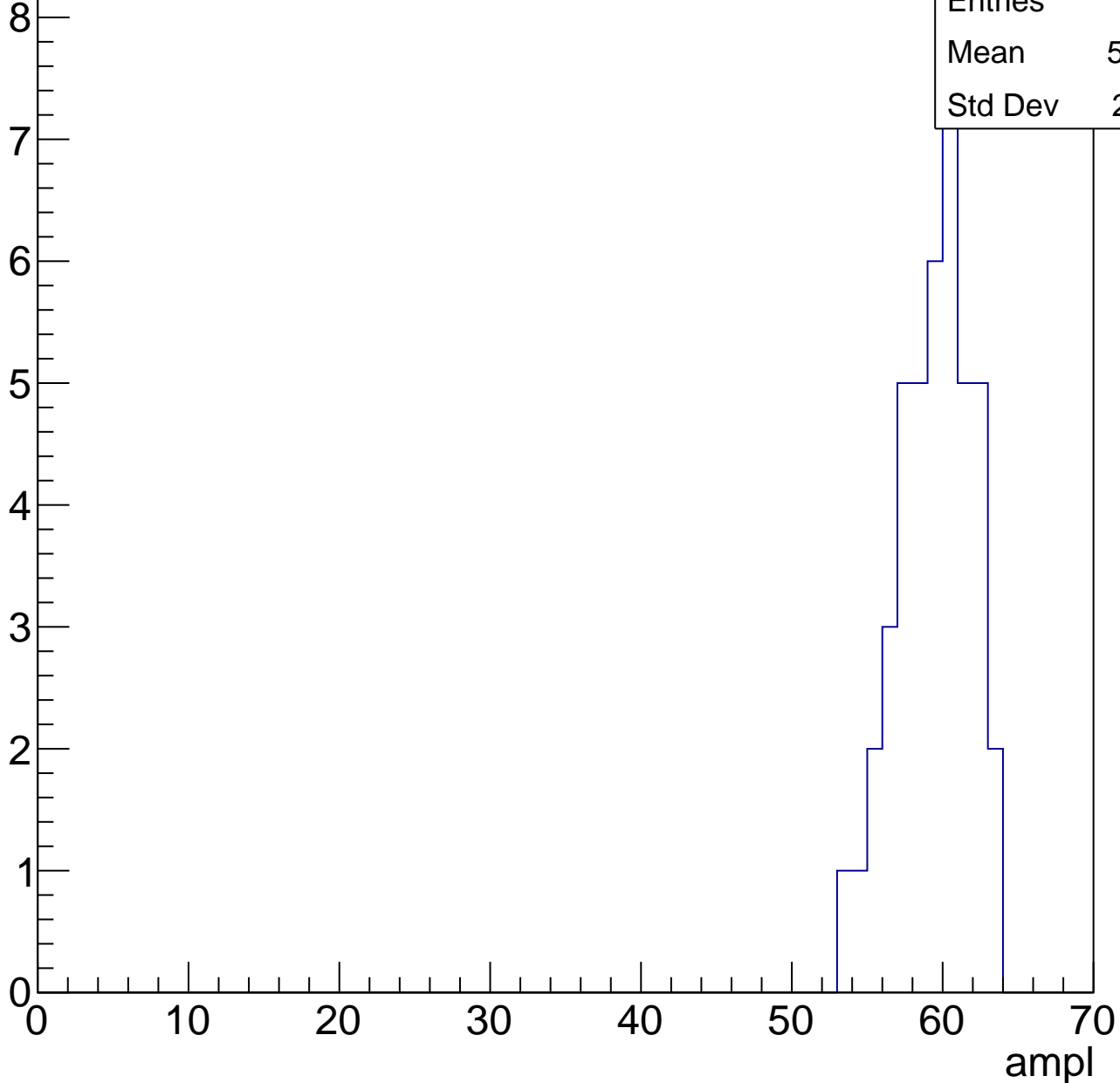


# B1L101S, U3-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	58.95
Std Dev	2.411

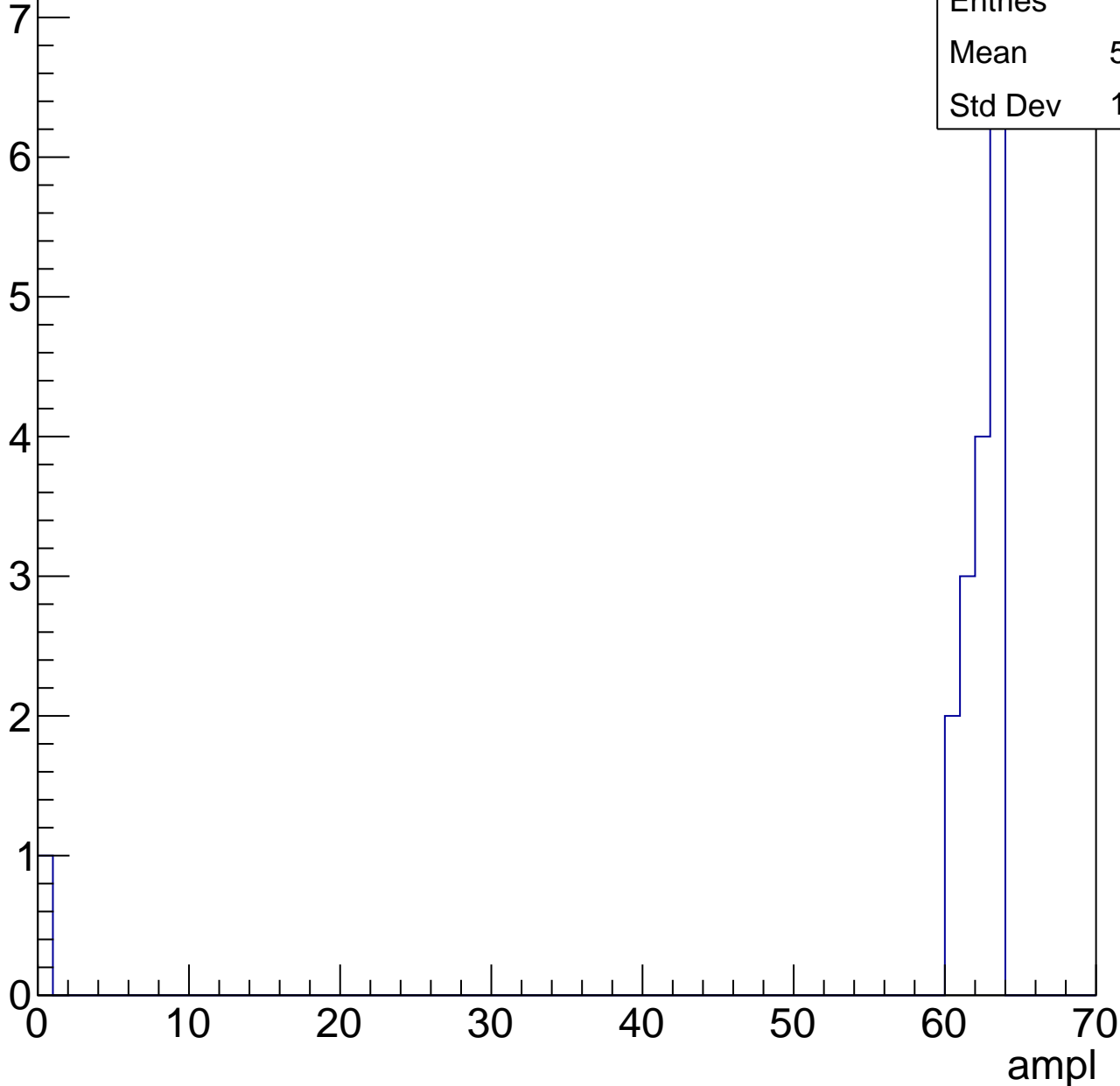


# B1L101S, U3-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	17
Mean	58.35
Std Dev	14.62

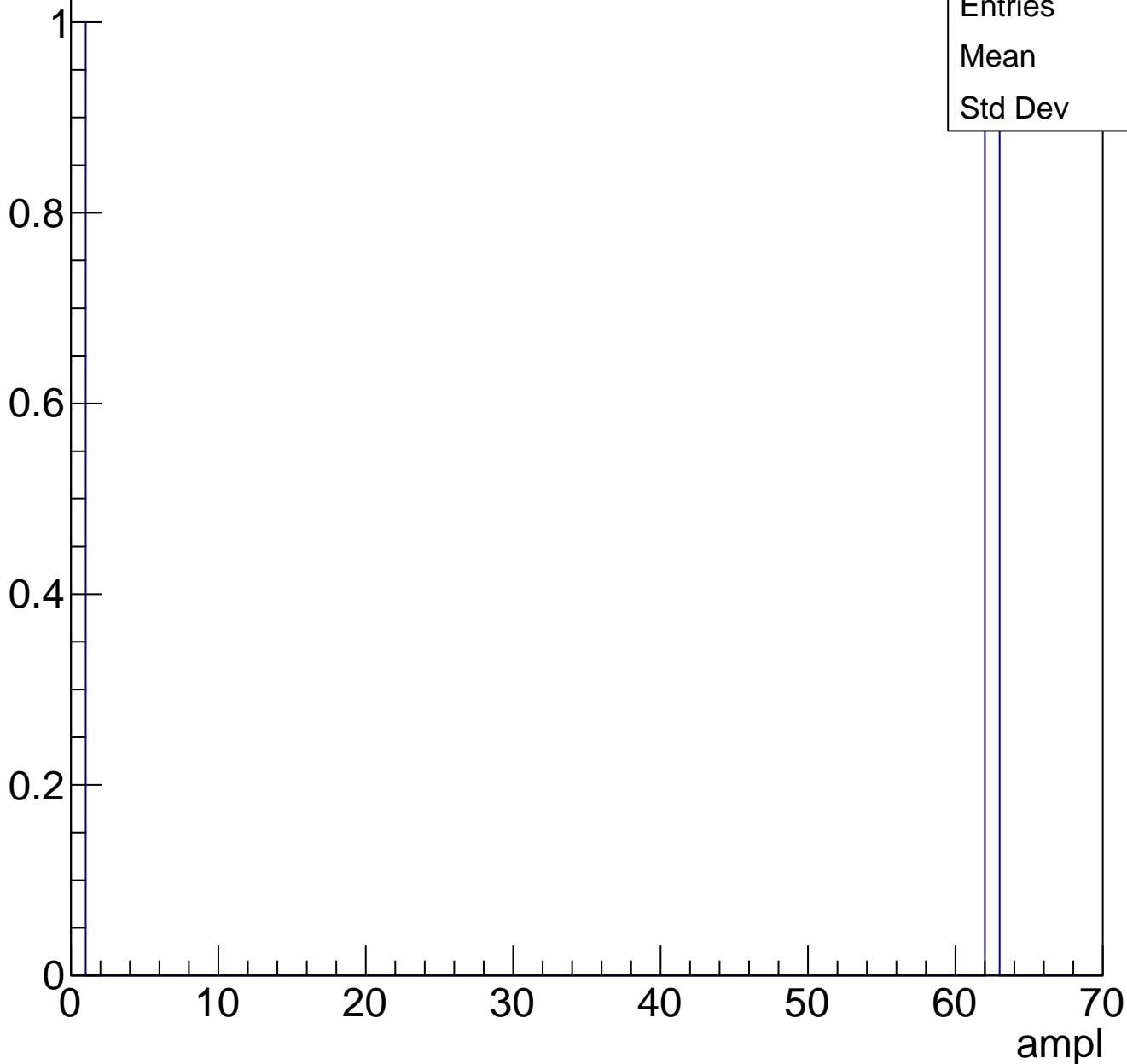




# B1L101S, U3-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch13, adc0

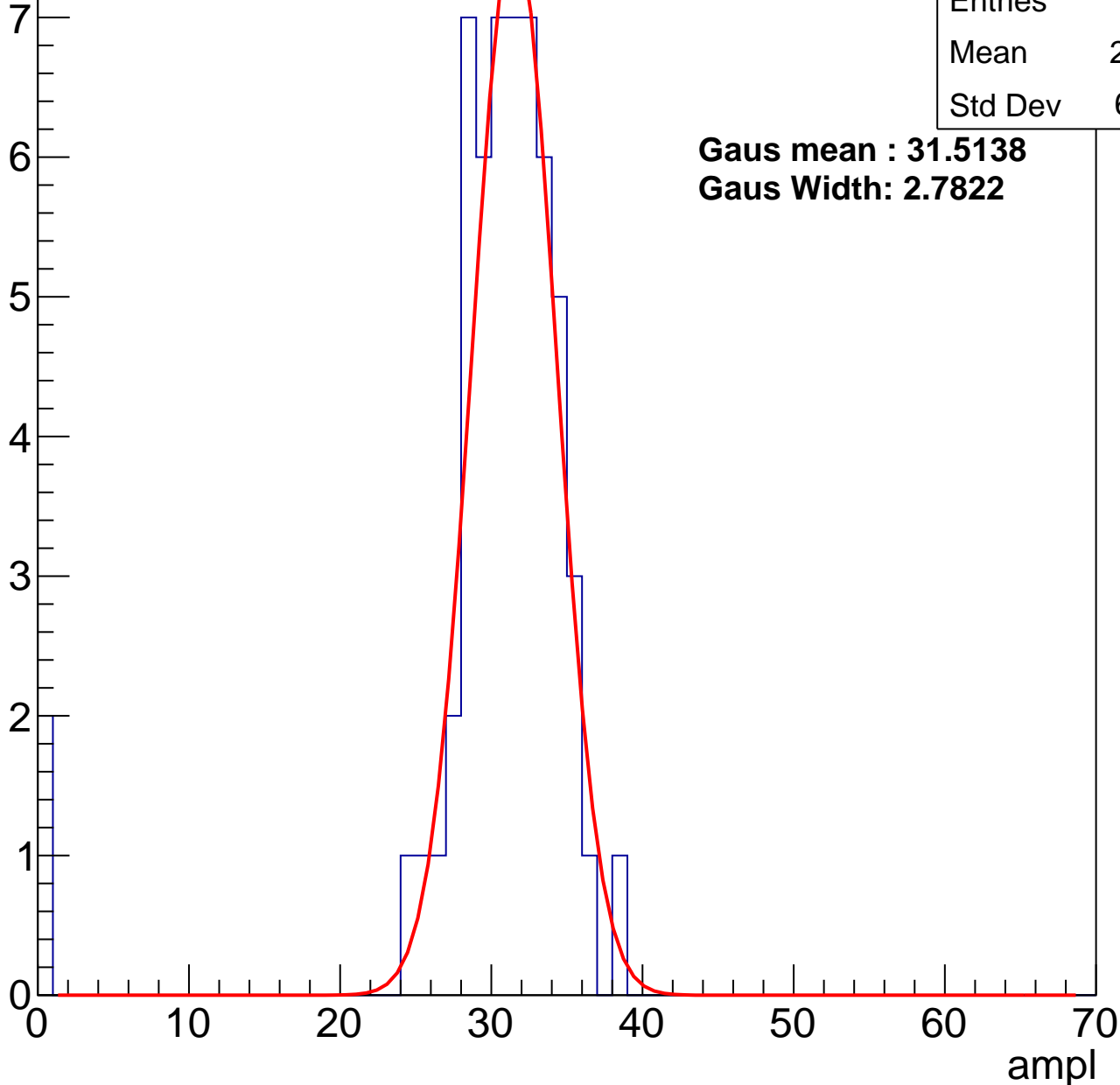
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	29.77
Std Dev	6.311

**Gaus mean : 31.5138**

**Gaus Width: 2.7822**



# B1L101S, U3-ch13, adc1

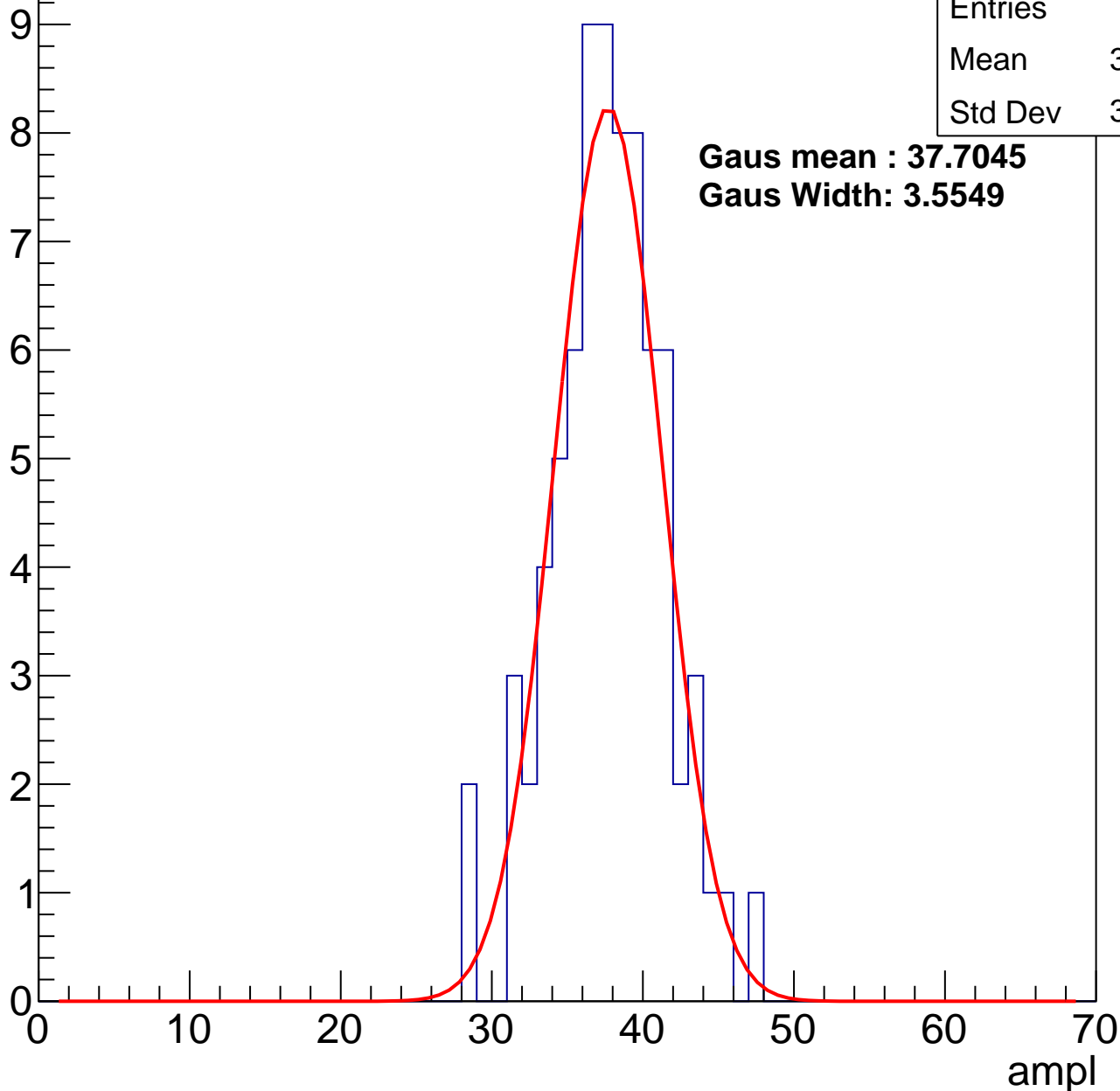
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	37.28
Std Dev	3.658

**Gaus mean : 37.7045**

**Gaus Width: 3.5549**



# B1L101S, U3-ch13, adc2

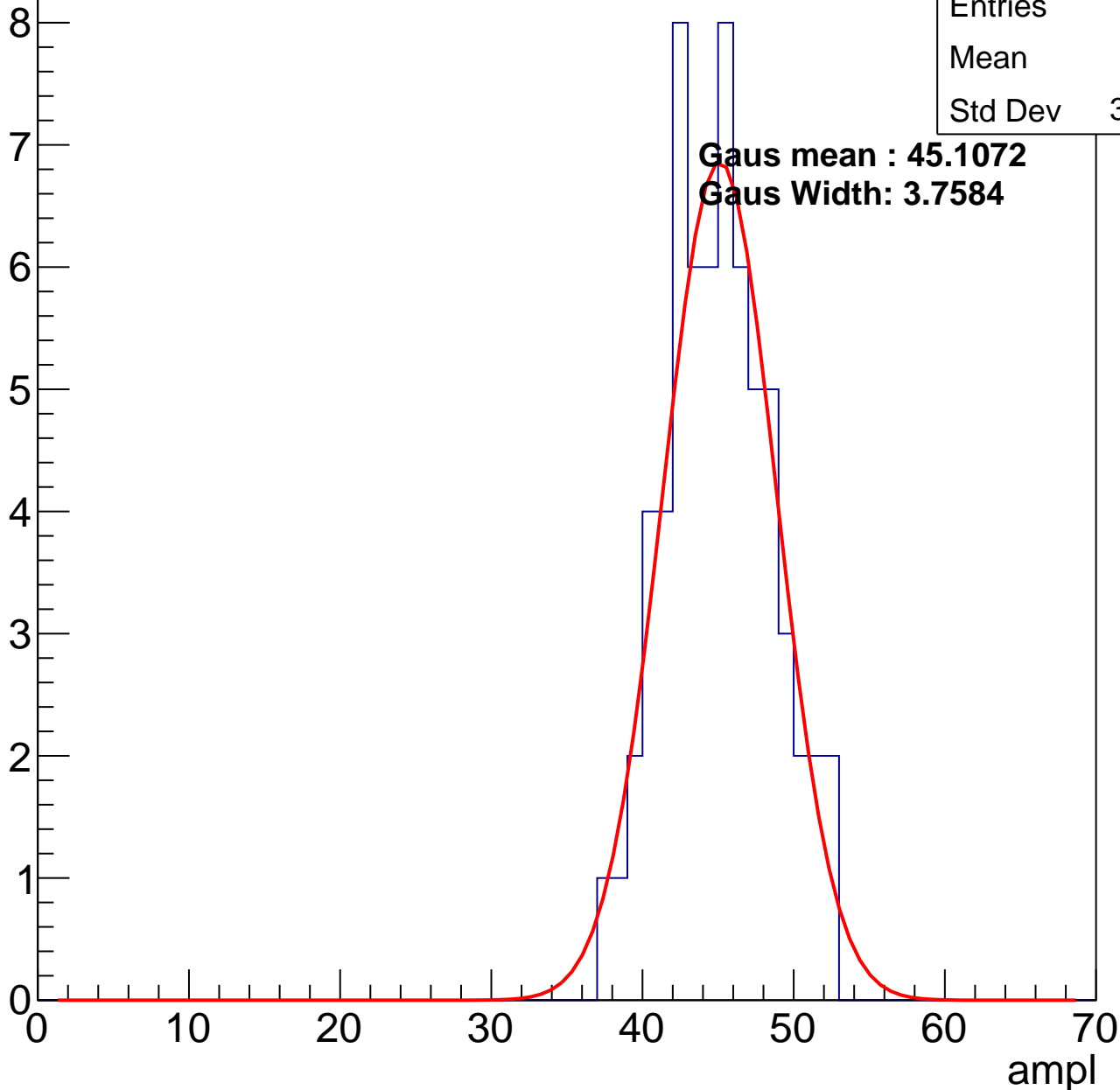
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	44.6
Std Dev	3.463

**Gaus mean : 45.1072**

**Gaus Width: 3.7584**

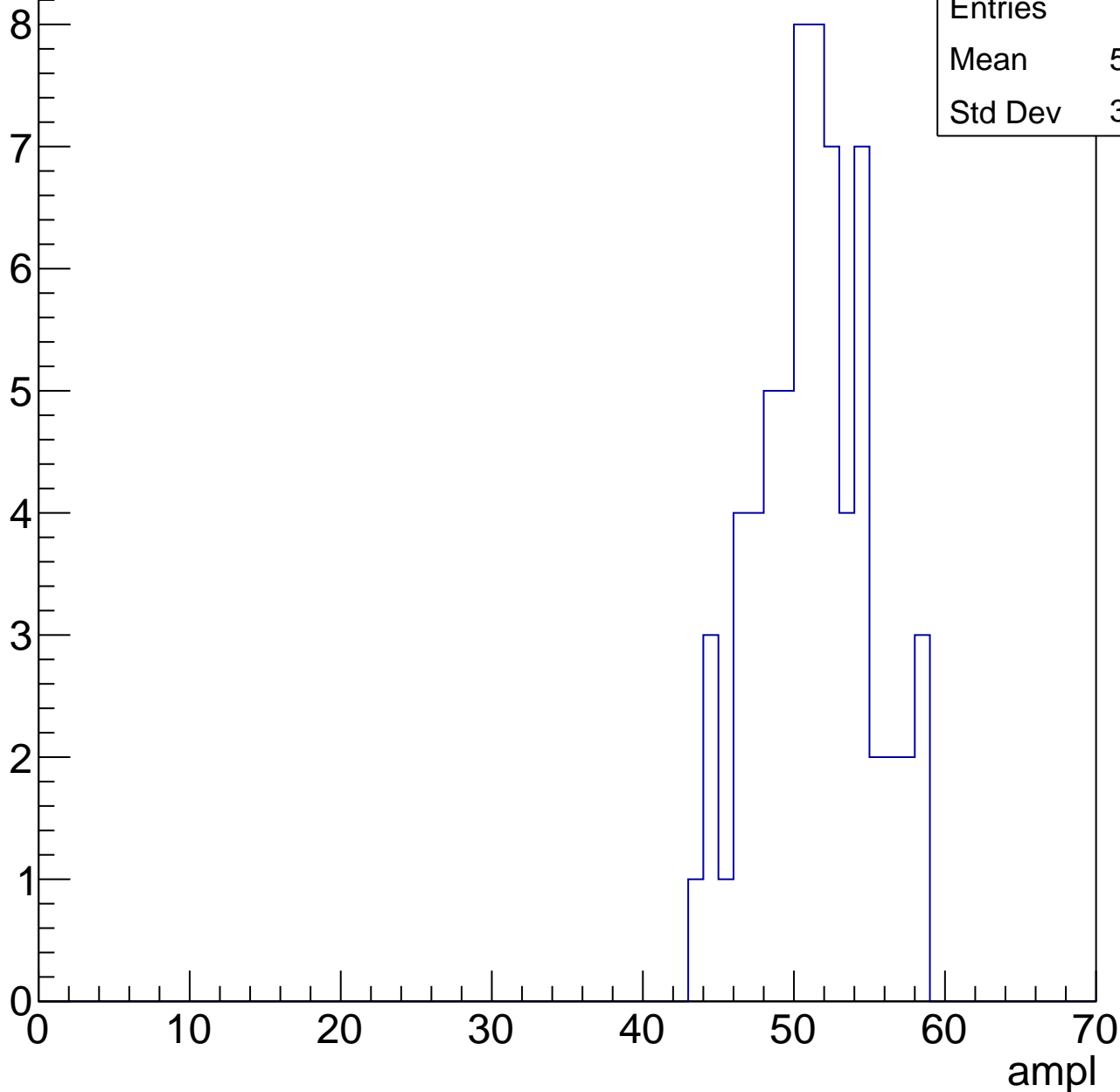


# B1L101S, U3-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	50.74
Std Dev	3.624

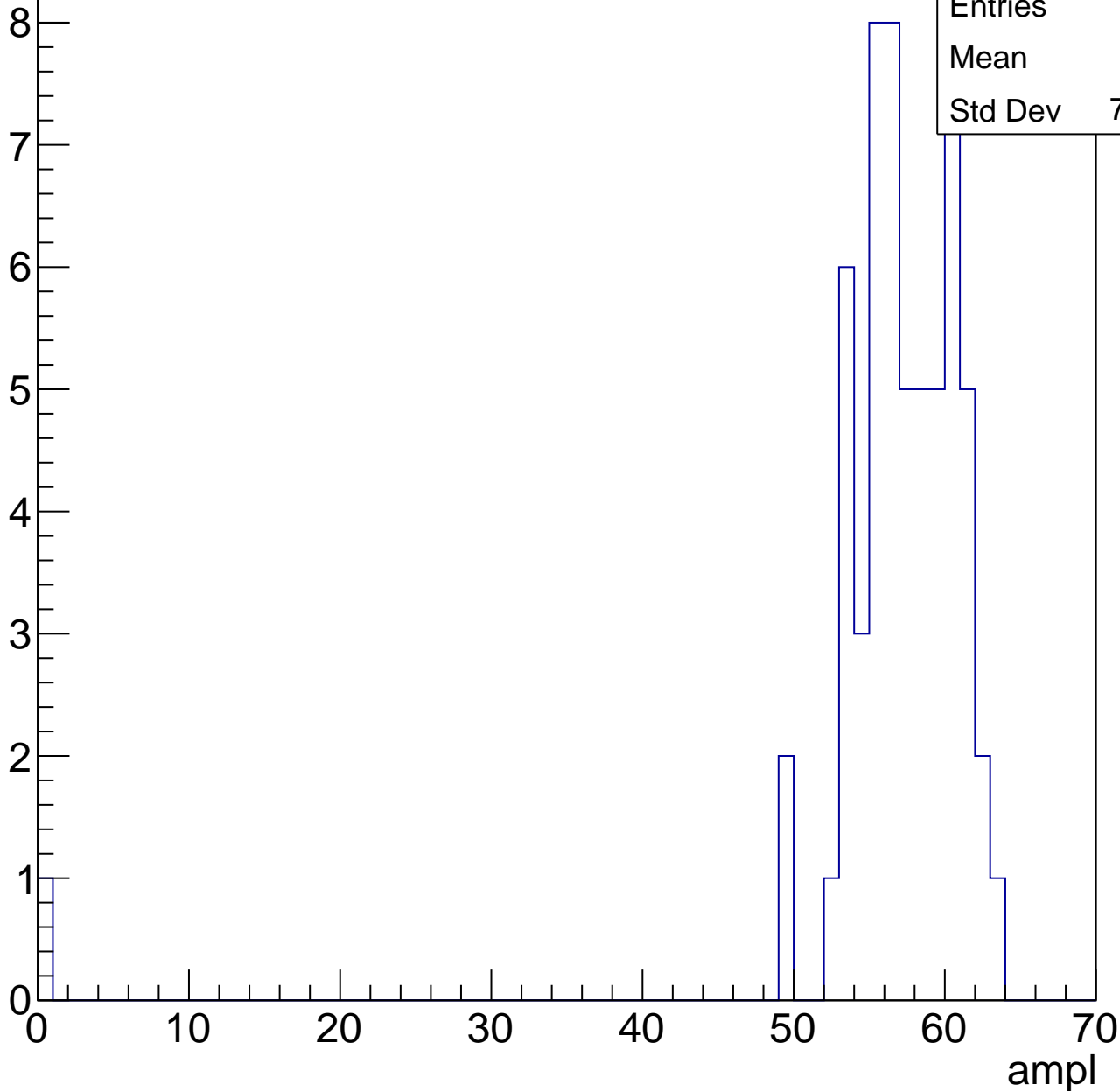


# B1L101S, U3-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

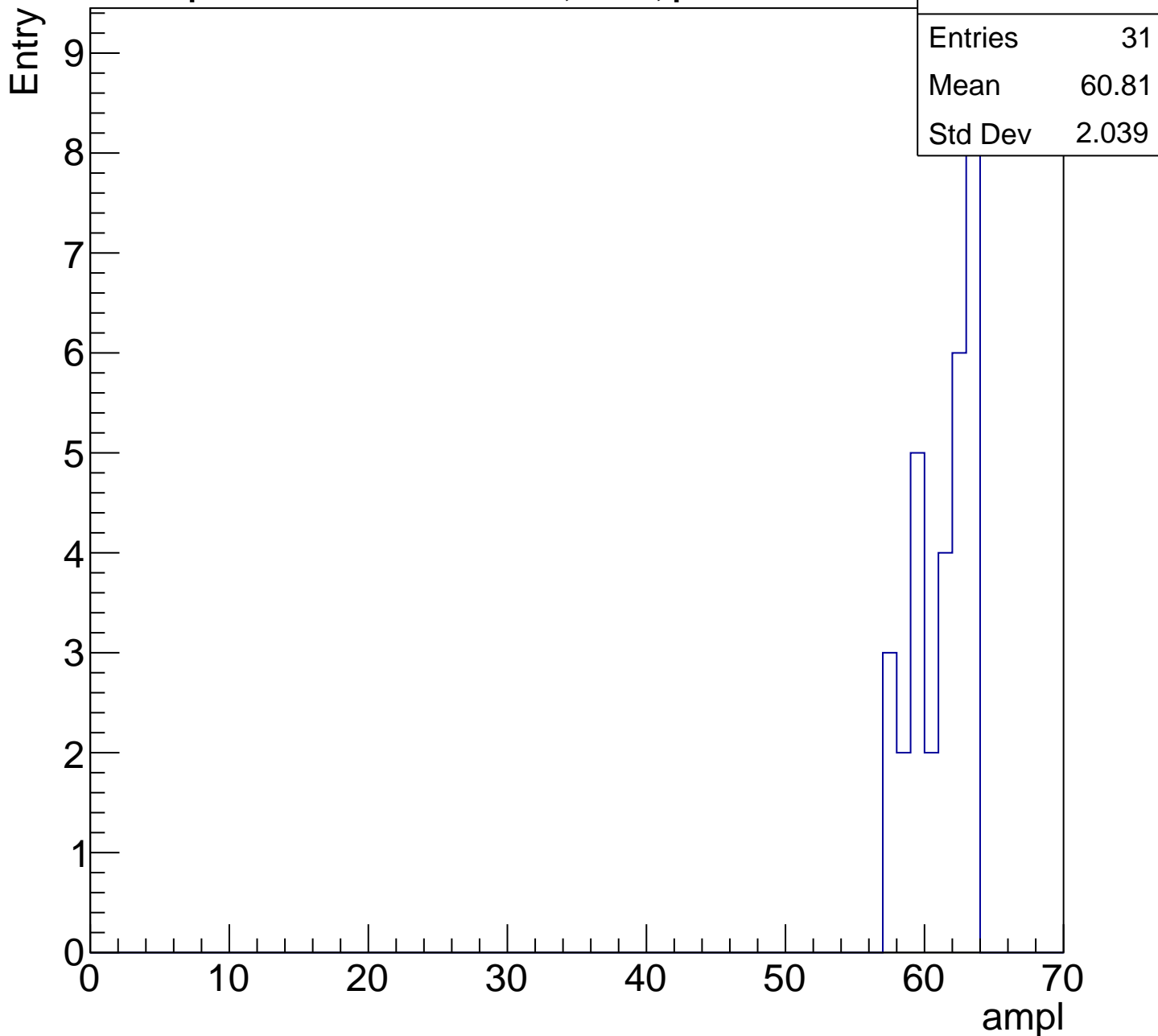
Entry

Entries	60
Mean	56
Std Dev	7.925



# B1L101S, U3-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	61.67
Std Dev	0.4714

ampl



# B1L101S, U3-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U3-ch14, adc0

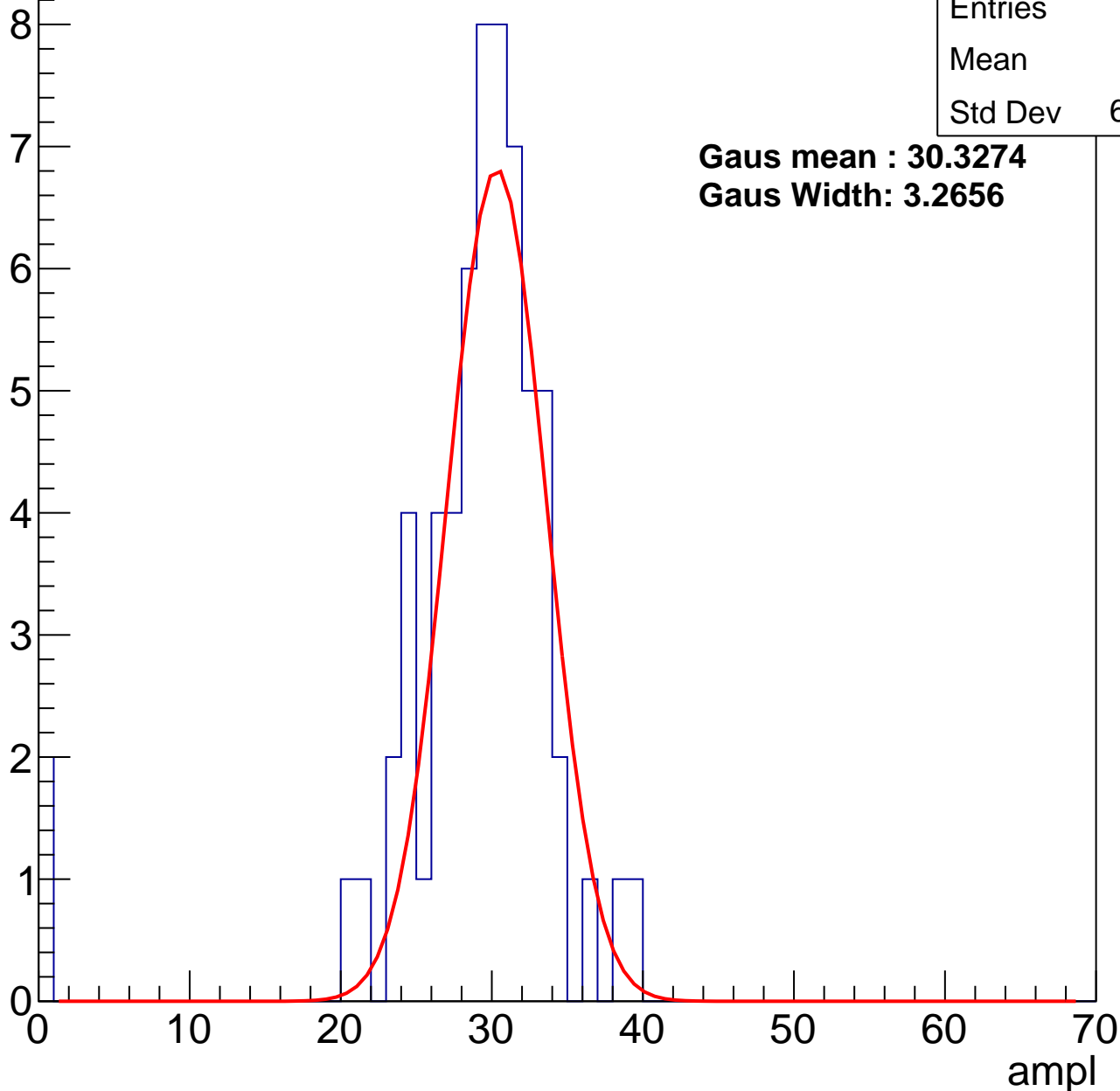
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	28.3
Std Dev	6.278

**Gaus mean : 30.3274**

**Gaus Width: 3.2656**



# B1L101S, U3-ch14, adc1

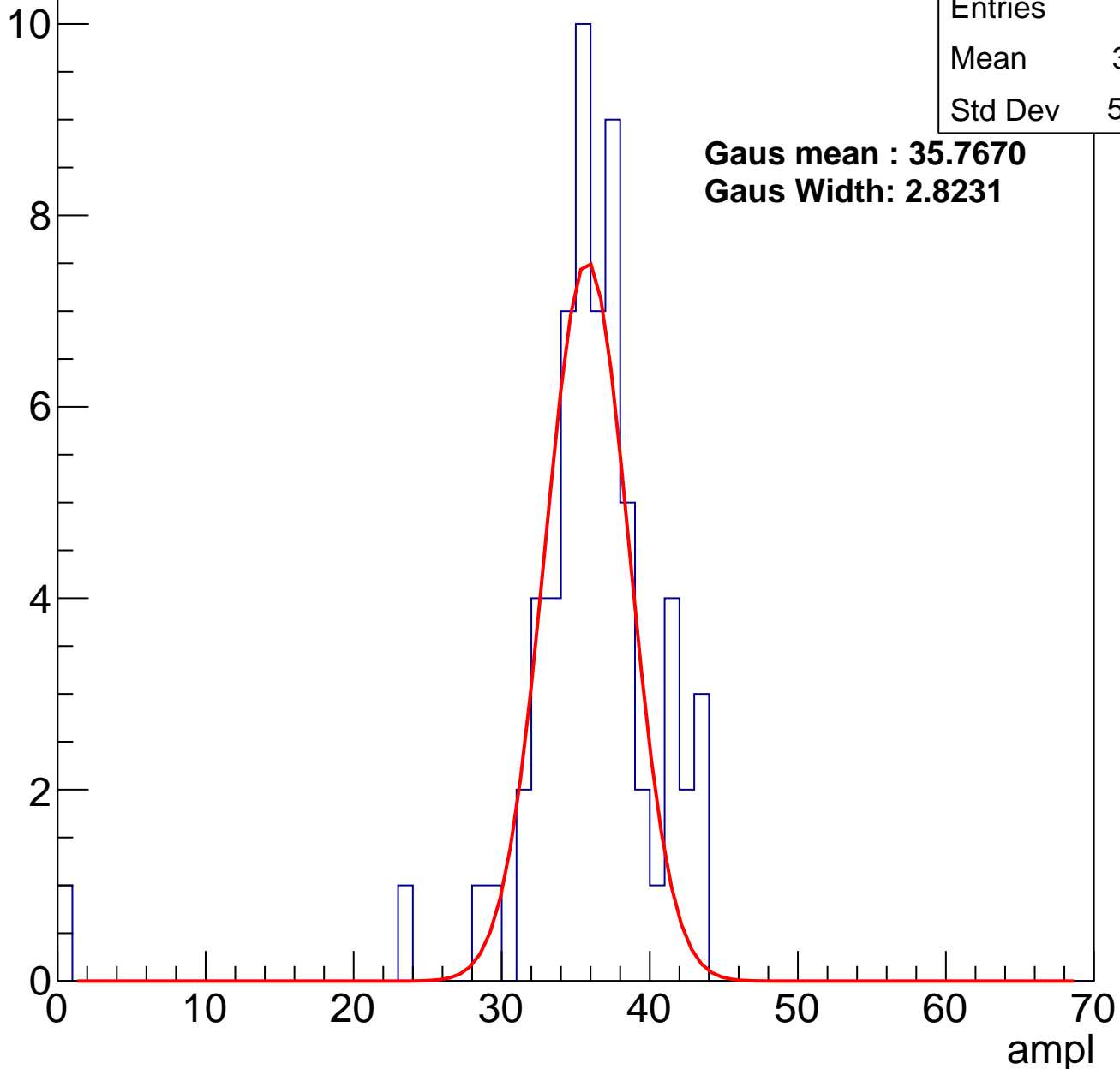
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	64
Mean	35.31
Std Dev	5.752

**Gaus mean : 35.7670**

**Gaus Width: 2.8231**

Entry



# B1L101S, U3-ch14, adc2

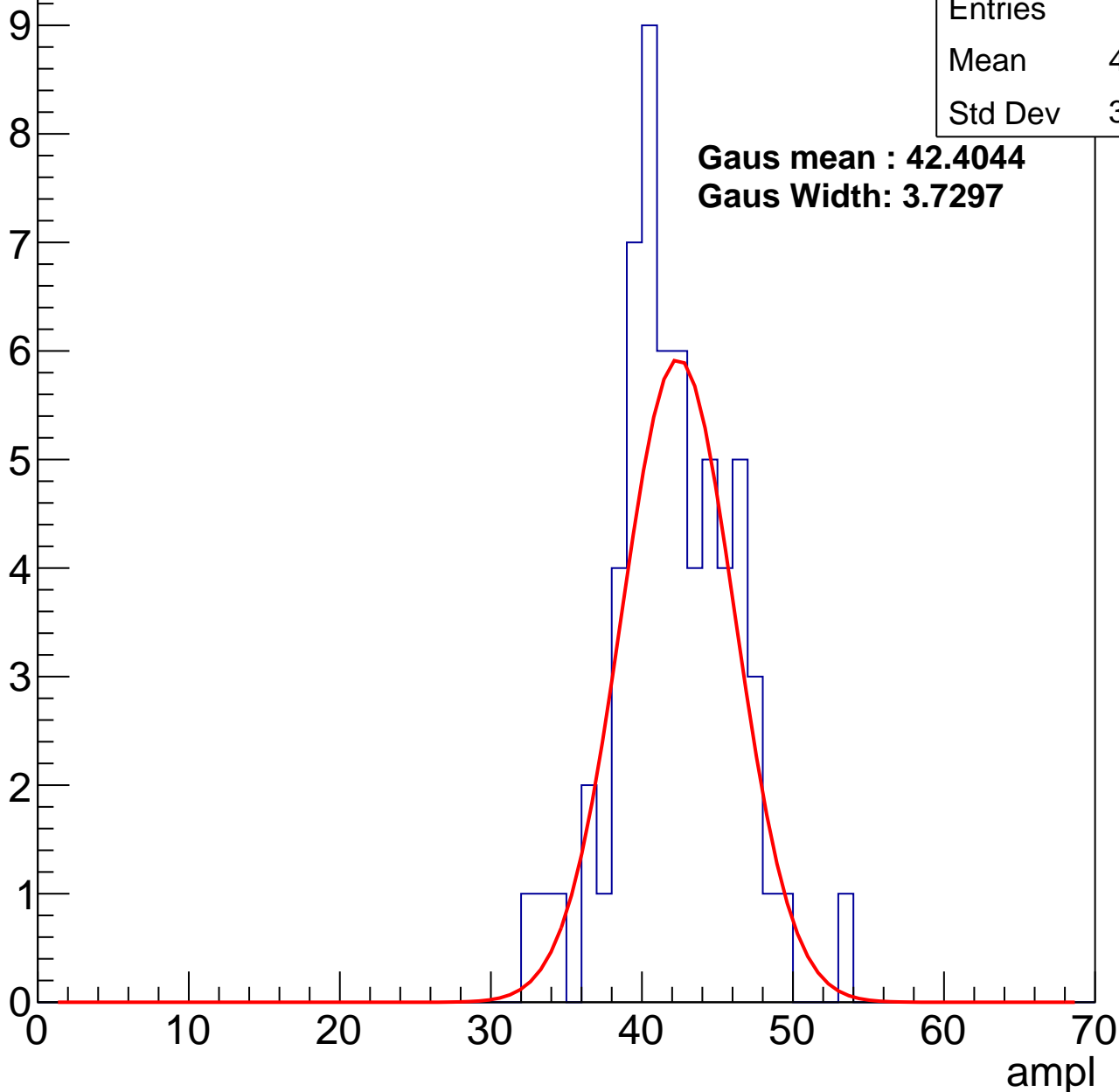
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	41.68
Std Dev	3.864

**Gaus mean : 42.4044**

**Gaus Width: 3.7297**

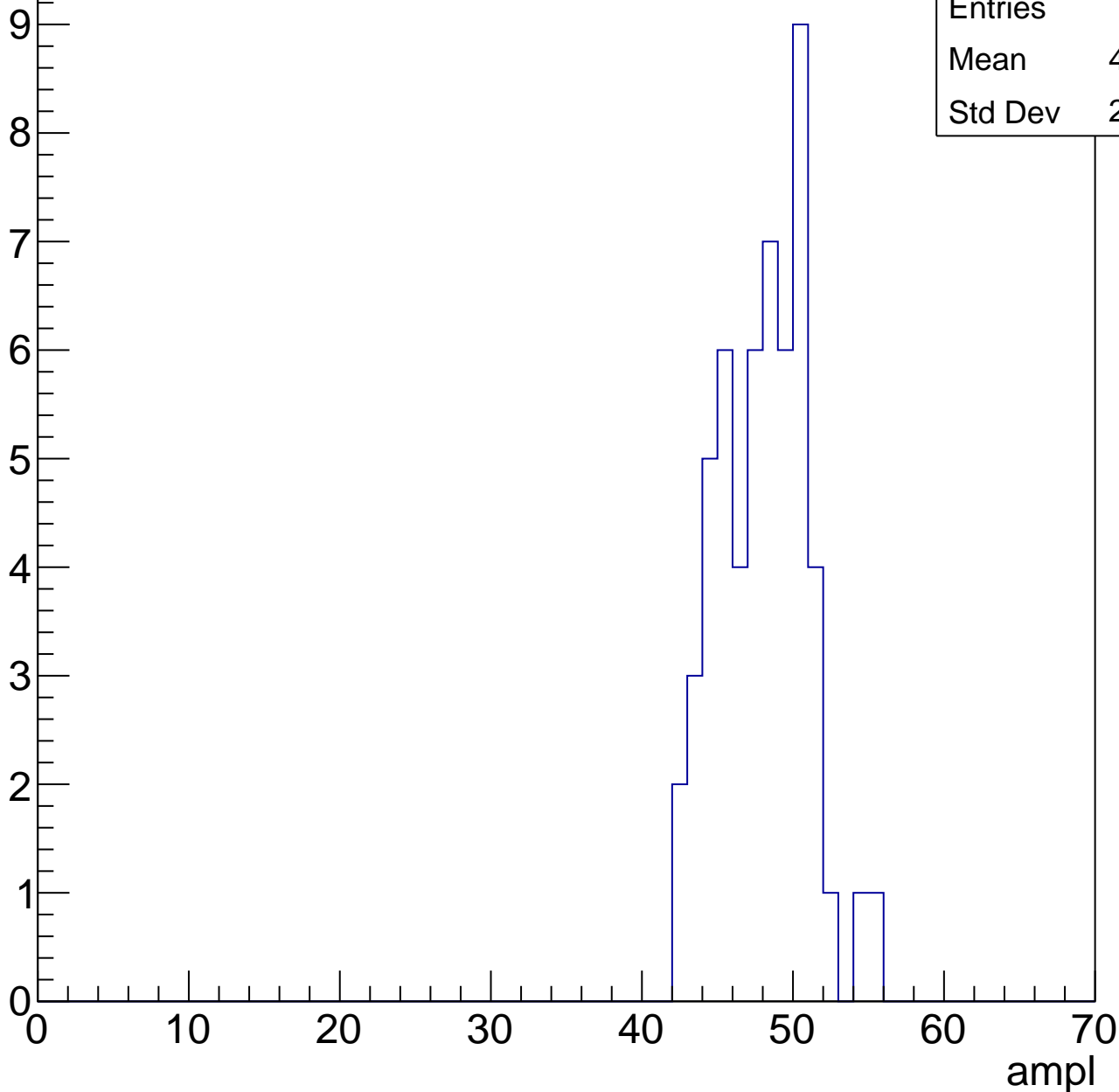


# B1L101S, U3-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	47.53
Std Dev	2.922

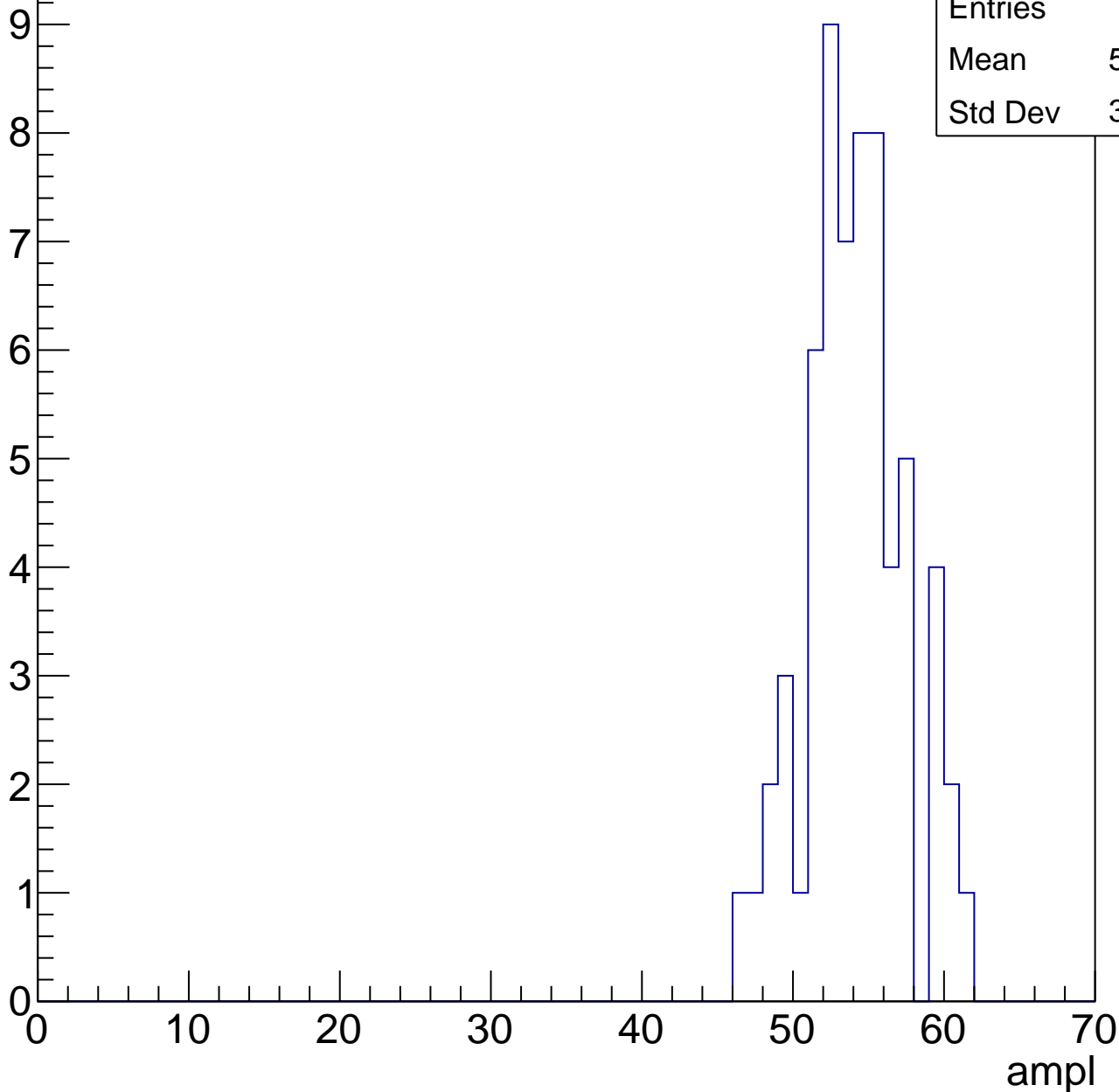


# B1L101S, U3-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	53.69
Std Dev	3.256

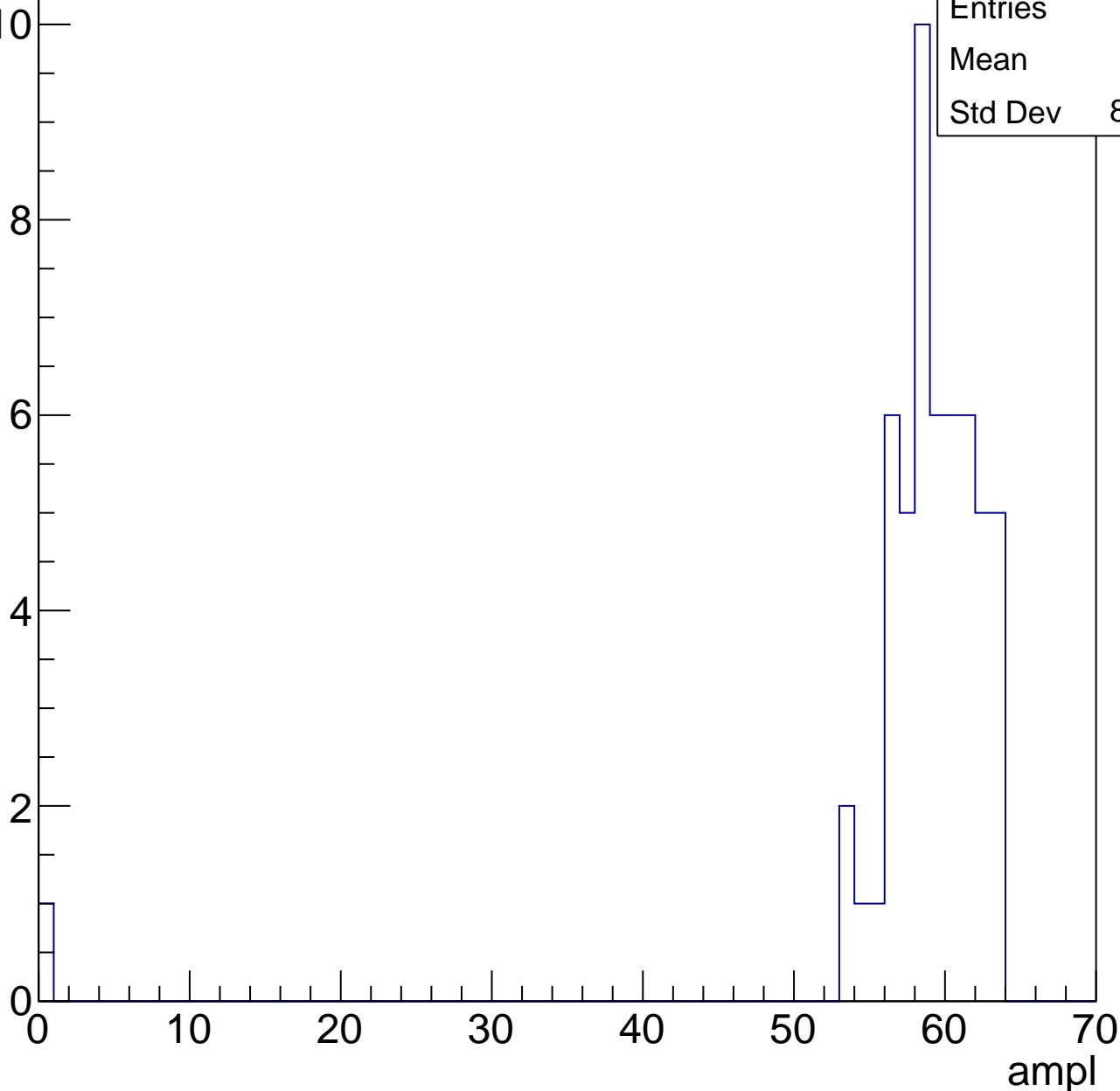


# B1L101S, U3-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	57.8
Std Dev	8.339

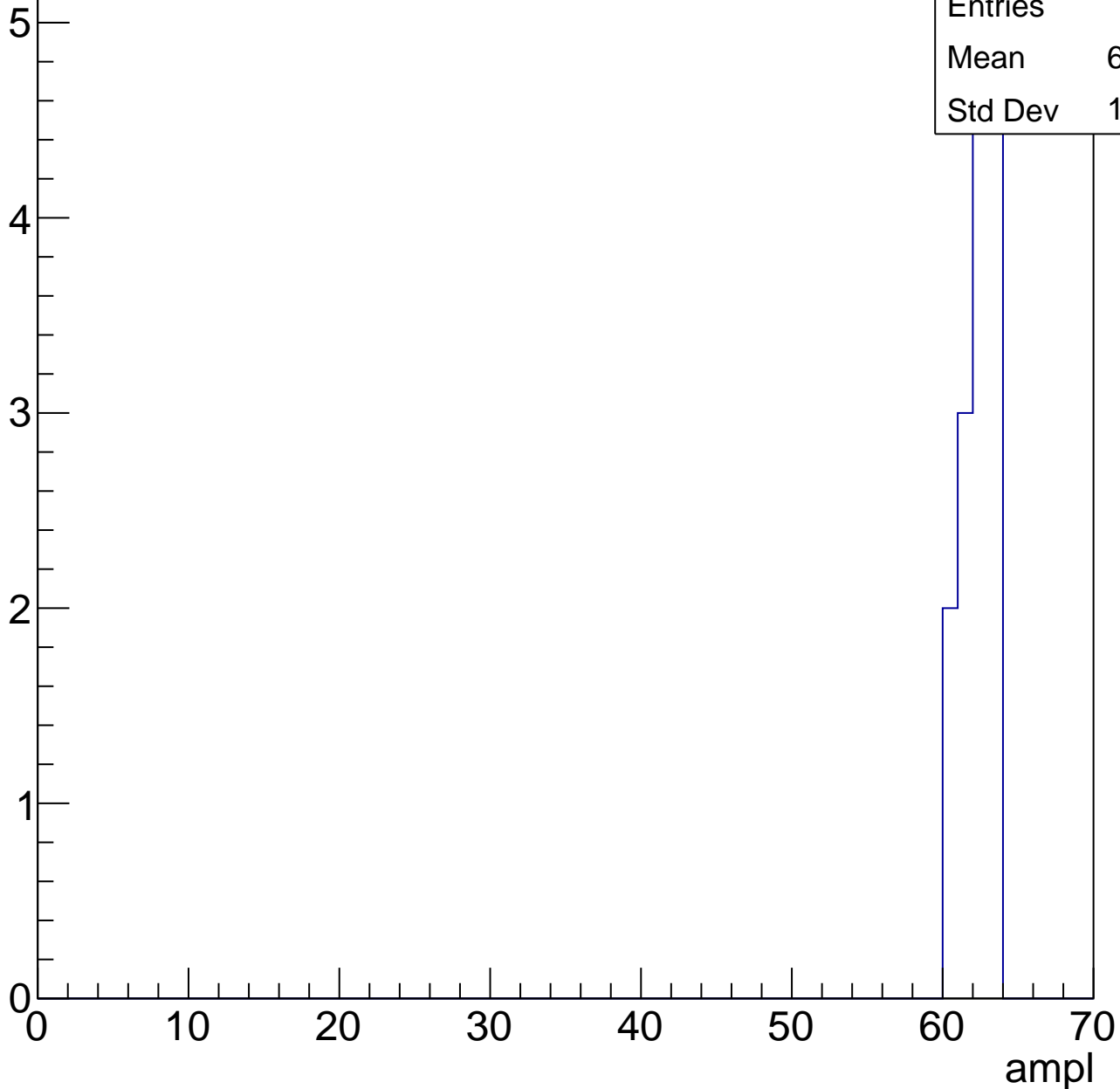


# B1L101S, U3-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	15
Mean	61.87
Std Dev	1.024





# B1L101S, U3-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U3-ch15, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	75
Mean	28.21
Std Dev	7.888

**Gaus mean : 29.0204**

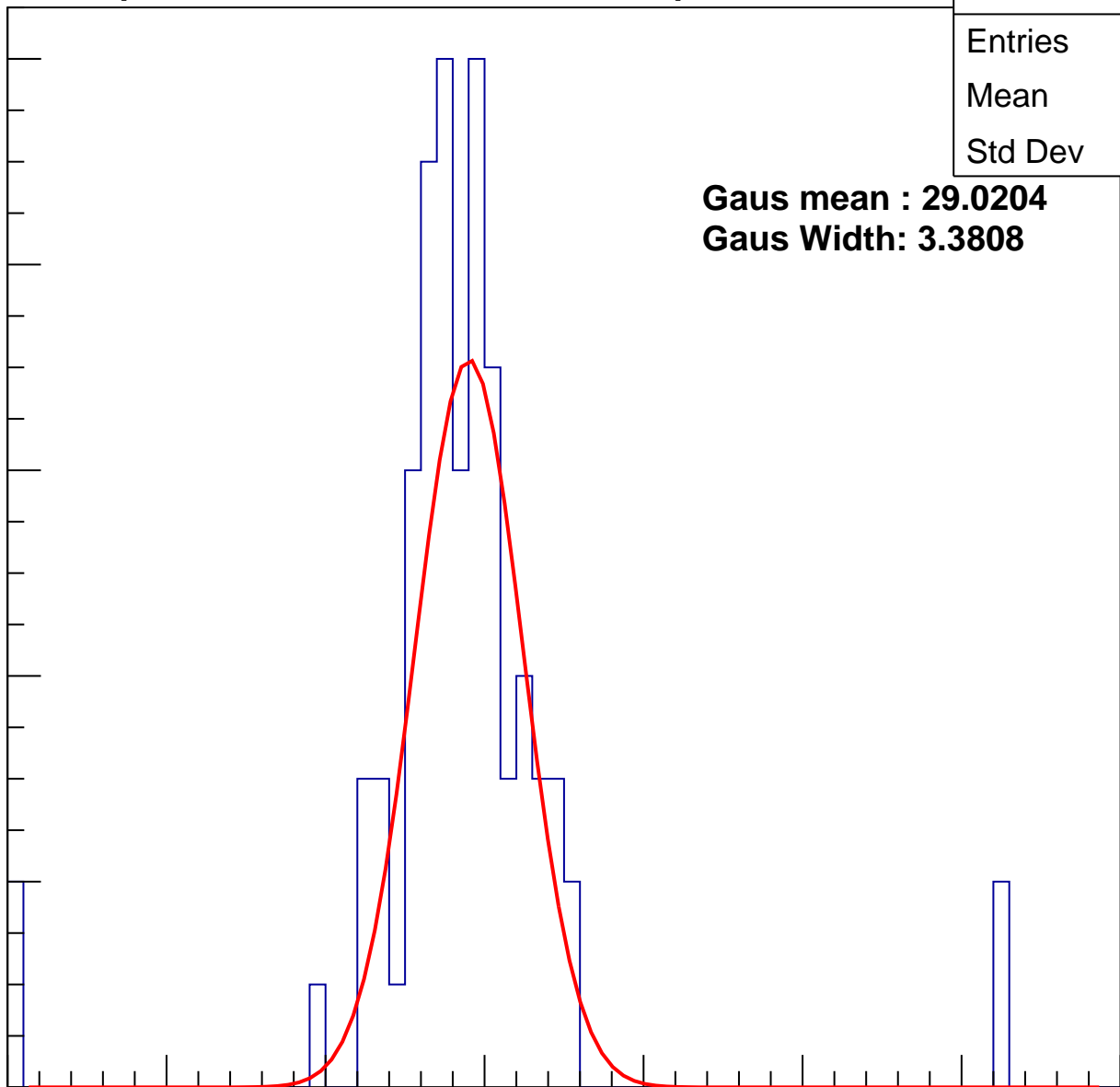
**Gaus Width: 3.3808**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U3-ch15, adc1

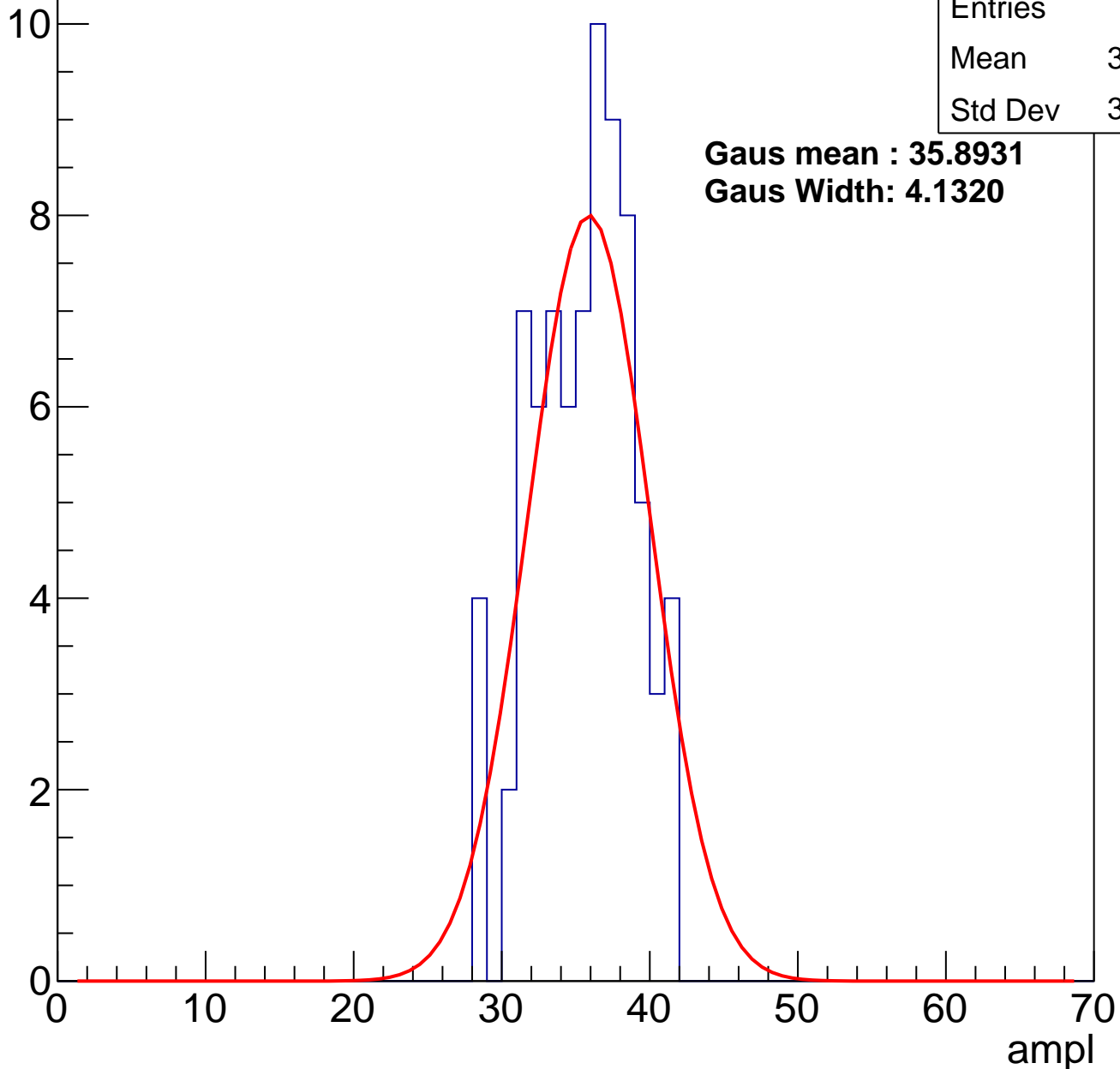
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	78
Mean	35.09
Std Dev	3.325

**Gaus mean : 35.8931**

**Gaus Width: 4.1320**

Entry



# B1L101S, U3-ch15, adc2

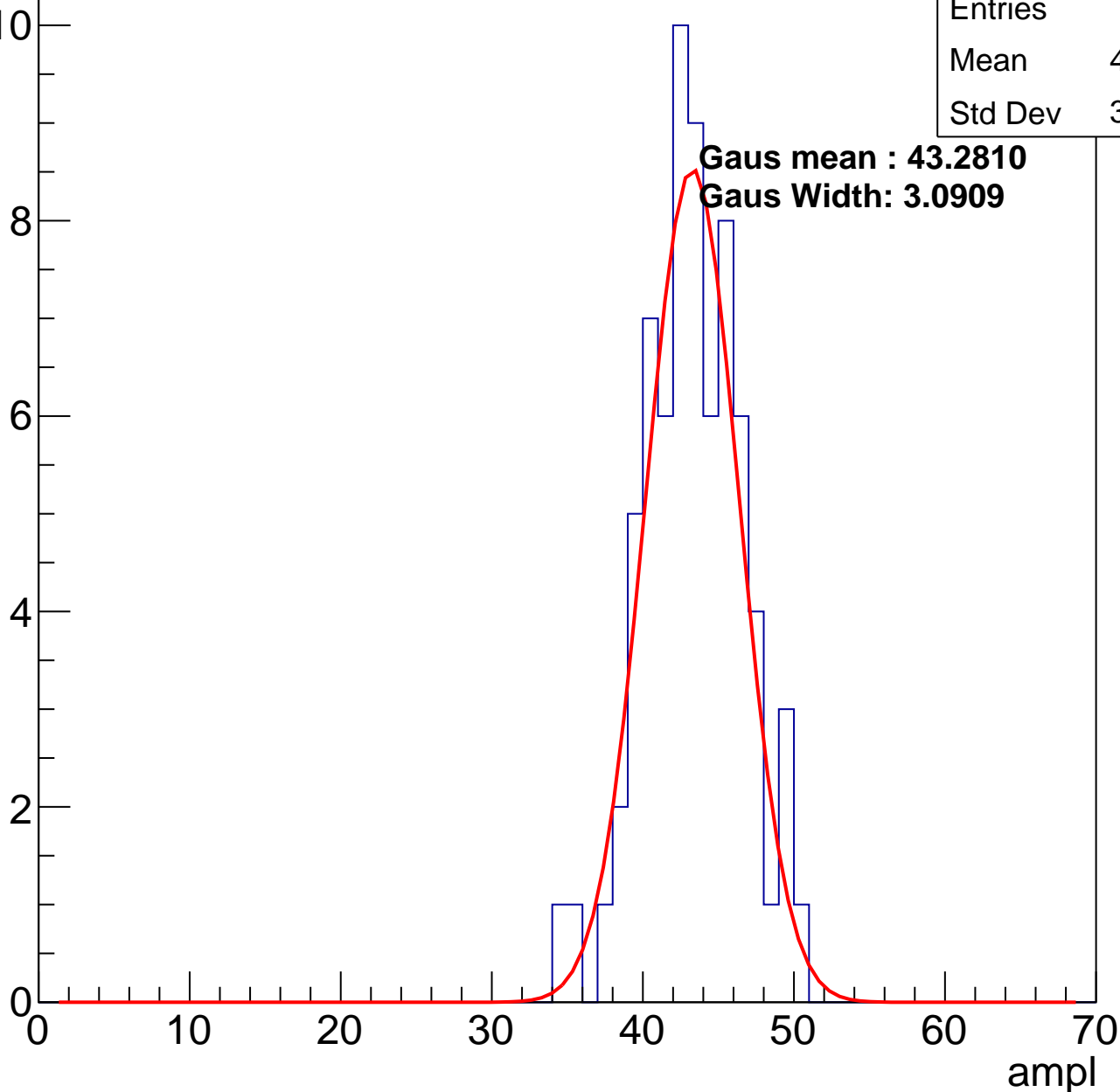
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	42.86
Std Dev	3.238

**Gaus mean : 43.2810**

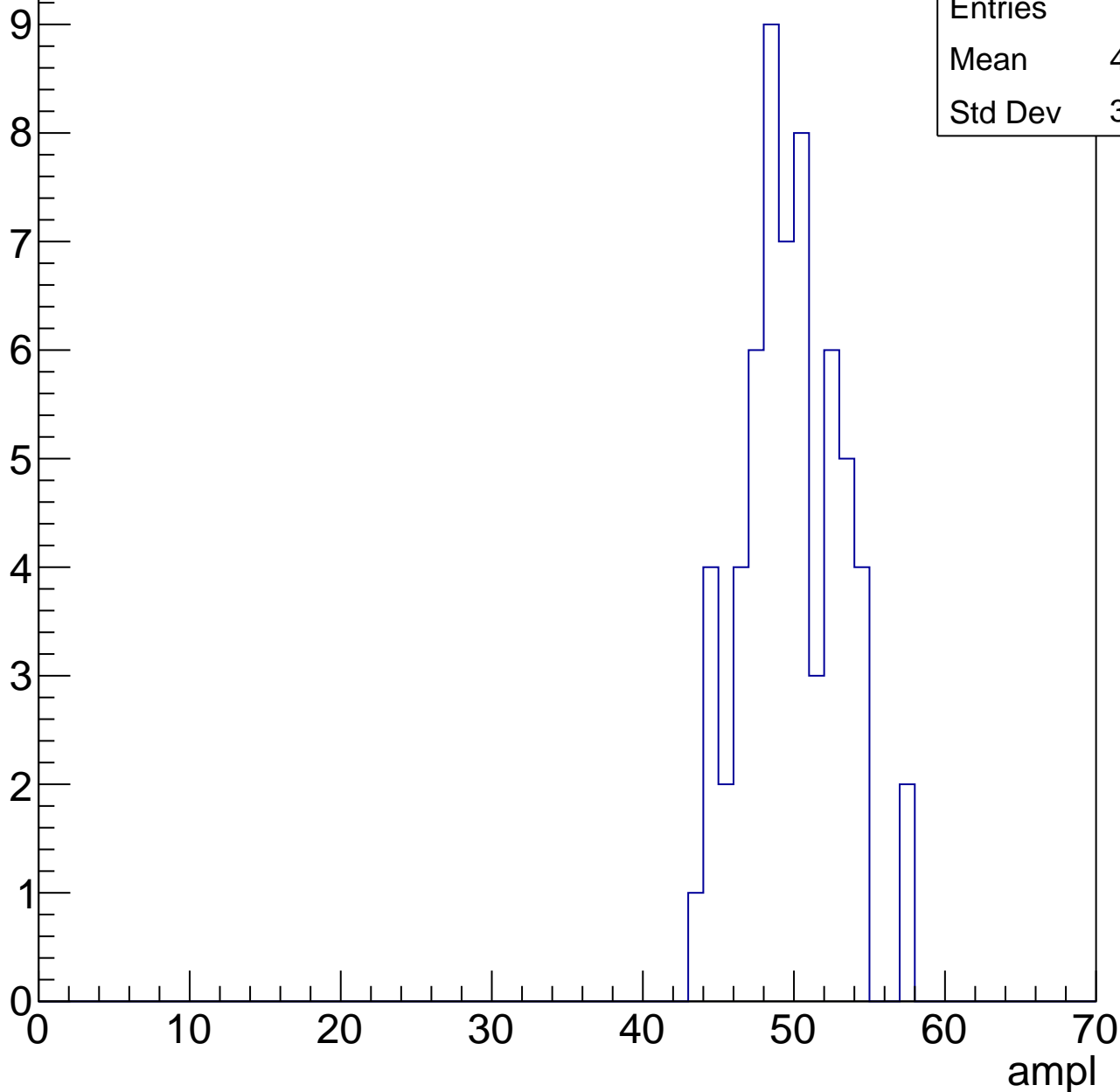
**Gaus Width: 3.0909**



# B1L101S, U3-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

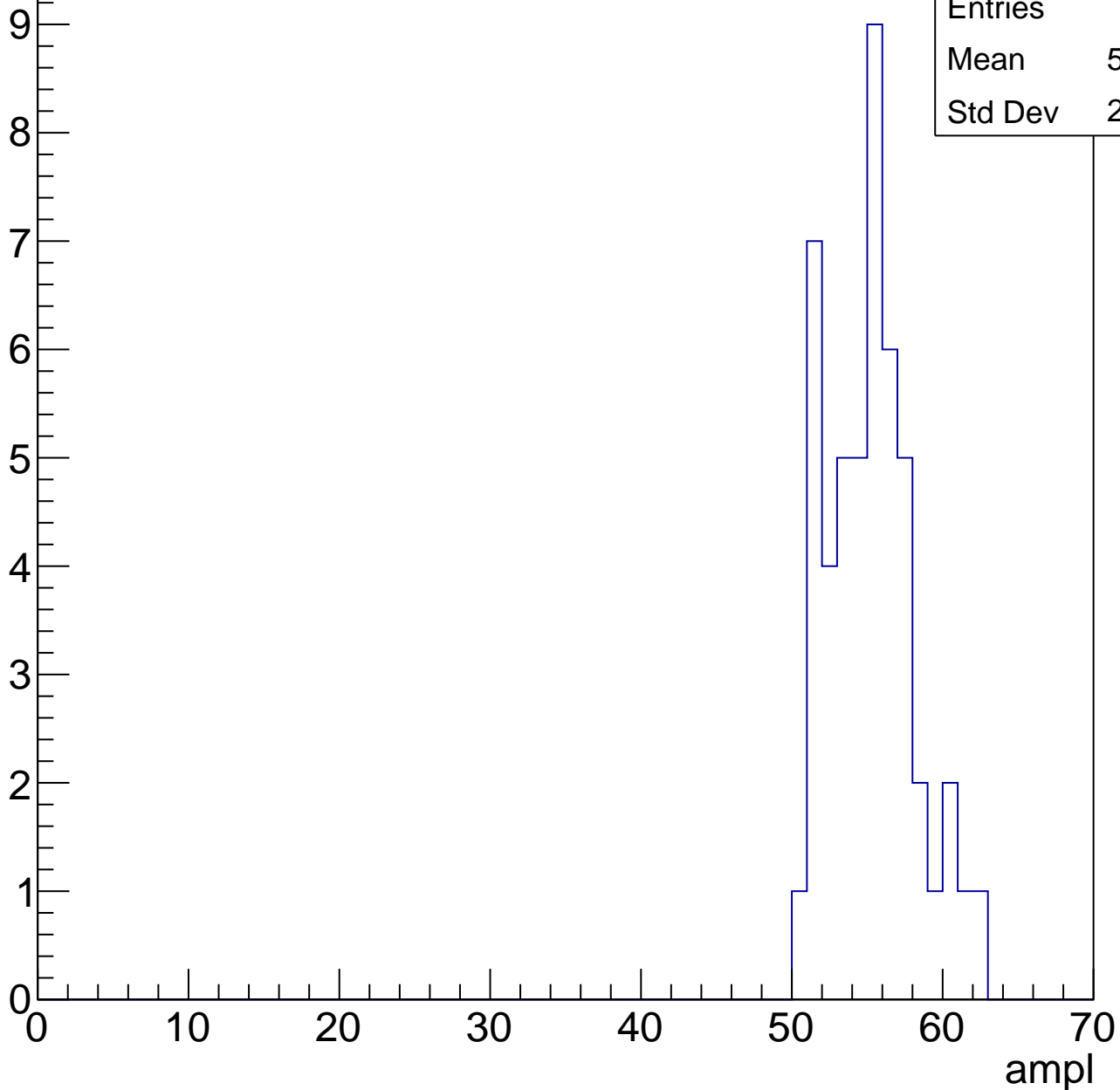


Entries	61
Mean	49.34
Std Dev	3.167

# B1L101S, U3-ch15, adc4

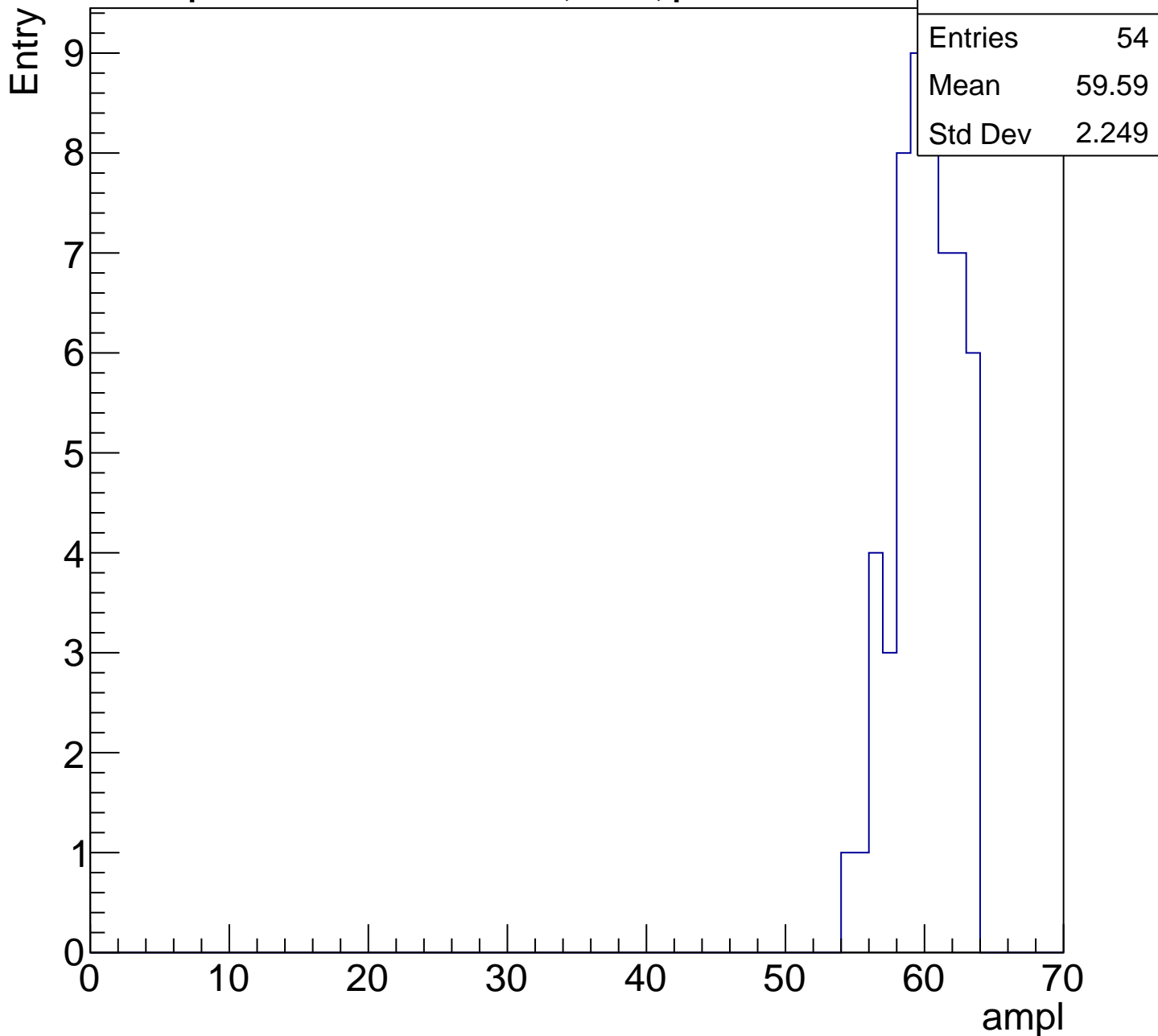
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch15, adc5

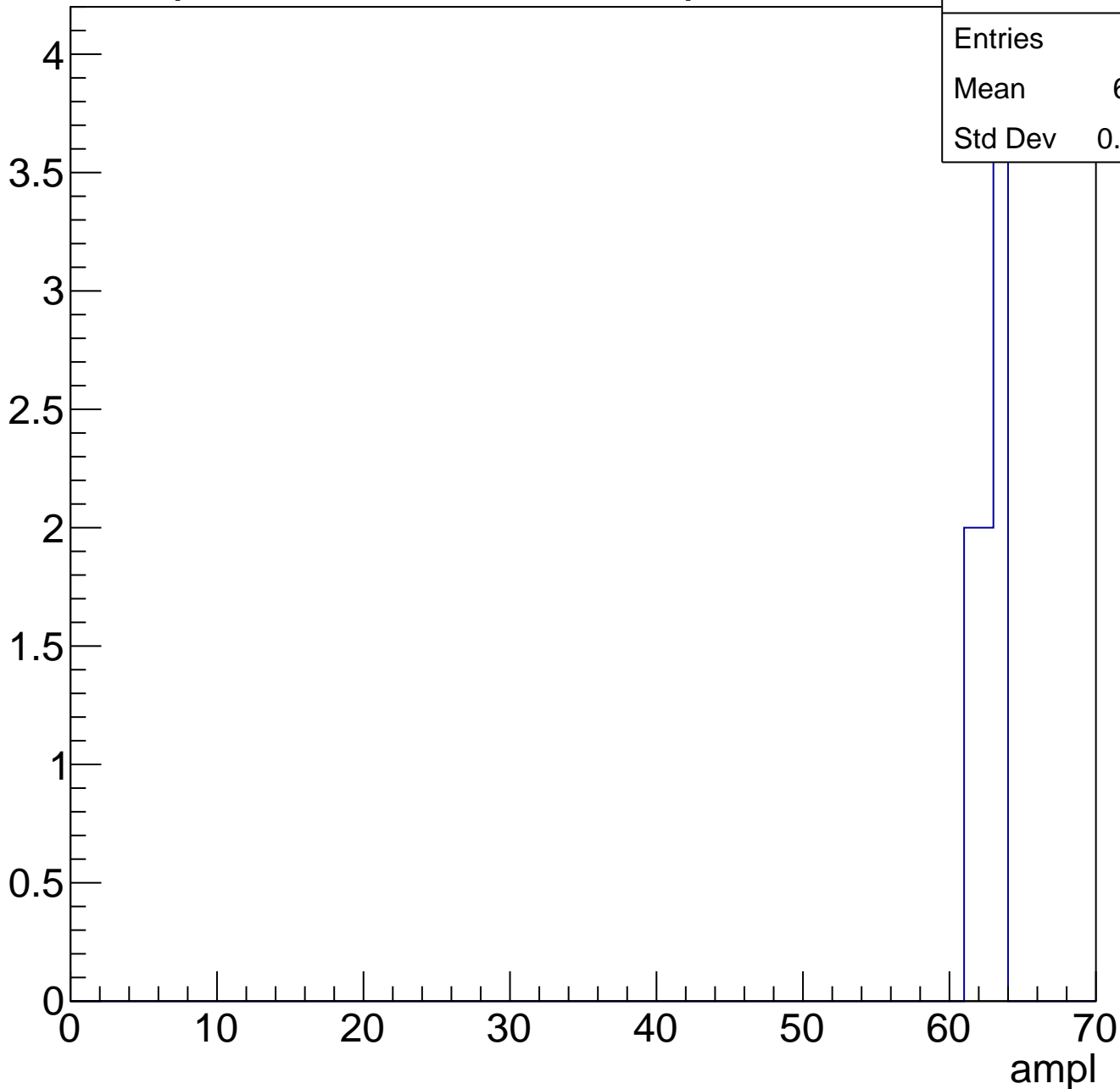
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U3-ch16, adc0

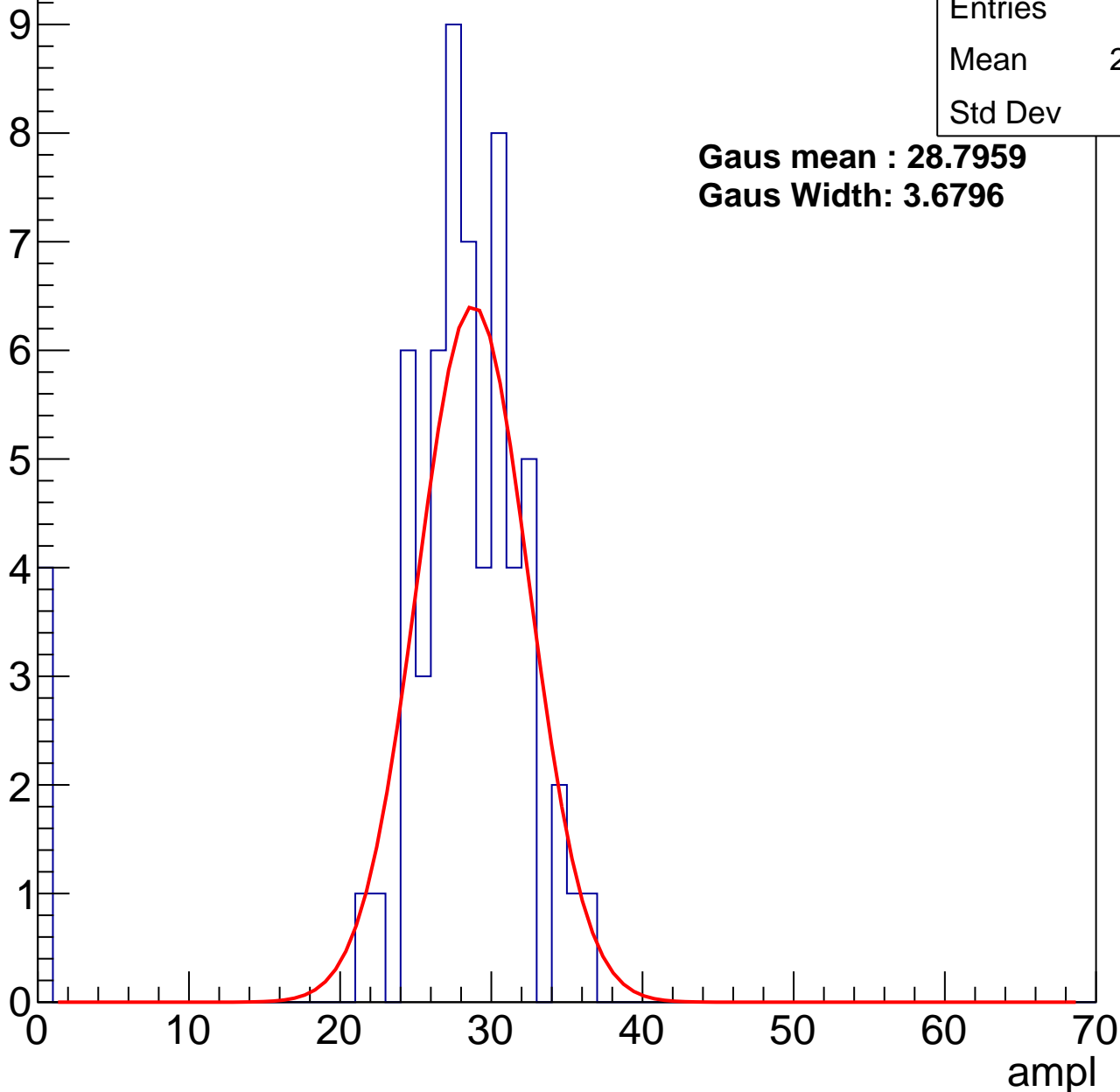
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	26.39
Std Dev	7.57

**Gaus mean : 28.7959**

**Gaus Width: 3.6796**



# B1L101S, U3-ch16, adc1

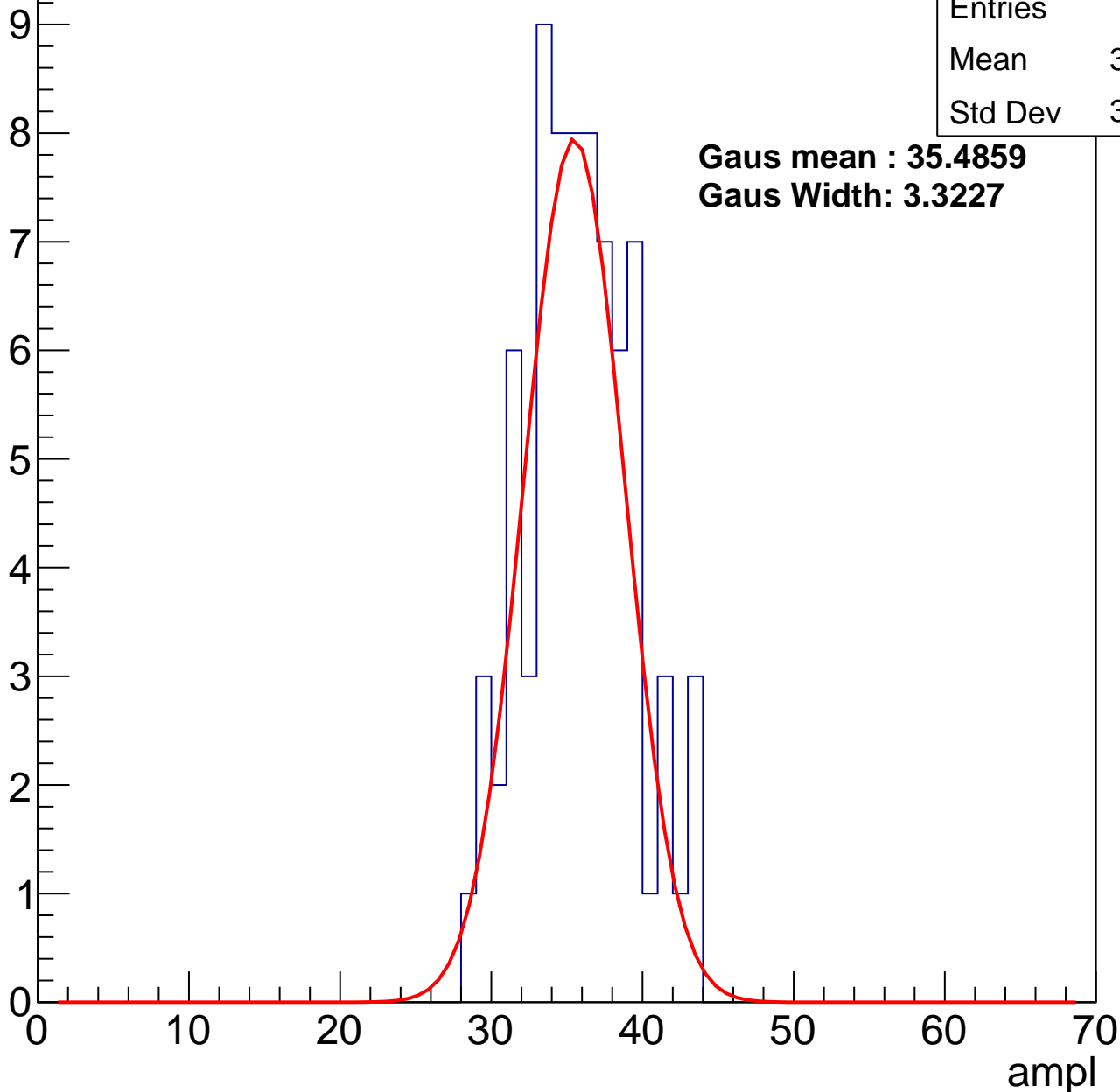
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	35.37
Std Dev	3.516

**Gaus mean : 35.4859**

**Gaus Width: 3.3227**



# B1L101S, U3-ch16, adc2

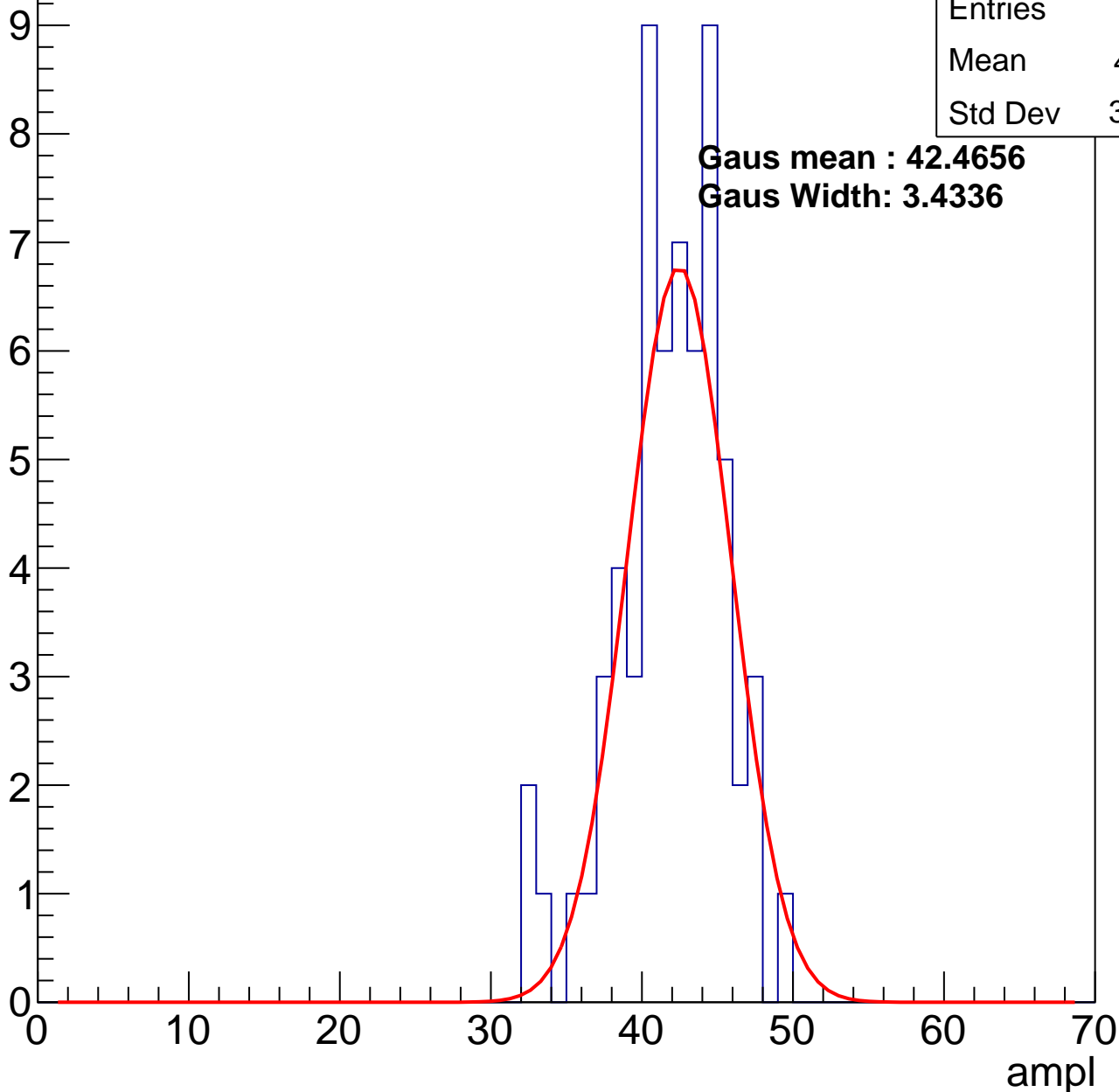
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	41.41
Std Dev	3.553

**Gaus mean : 42.4656**

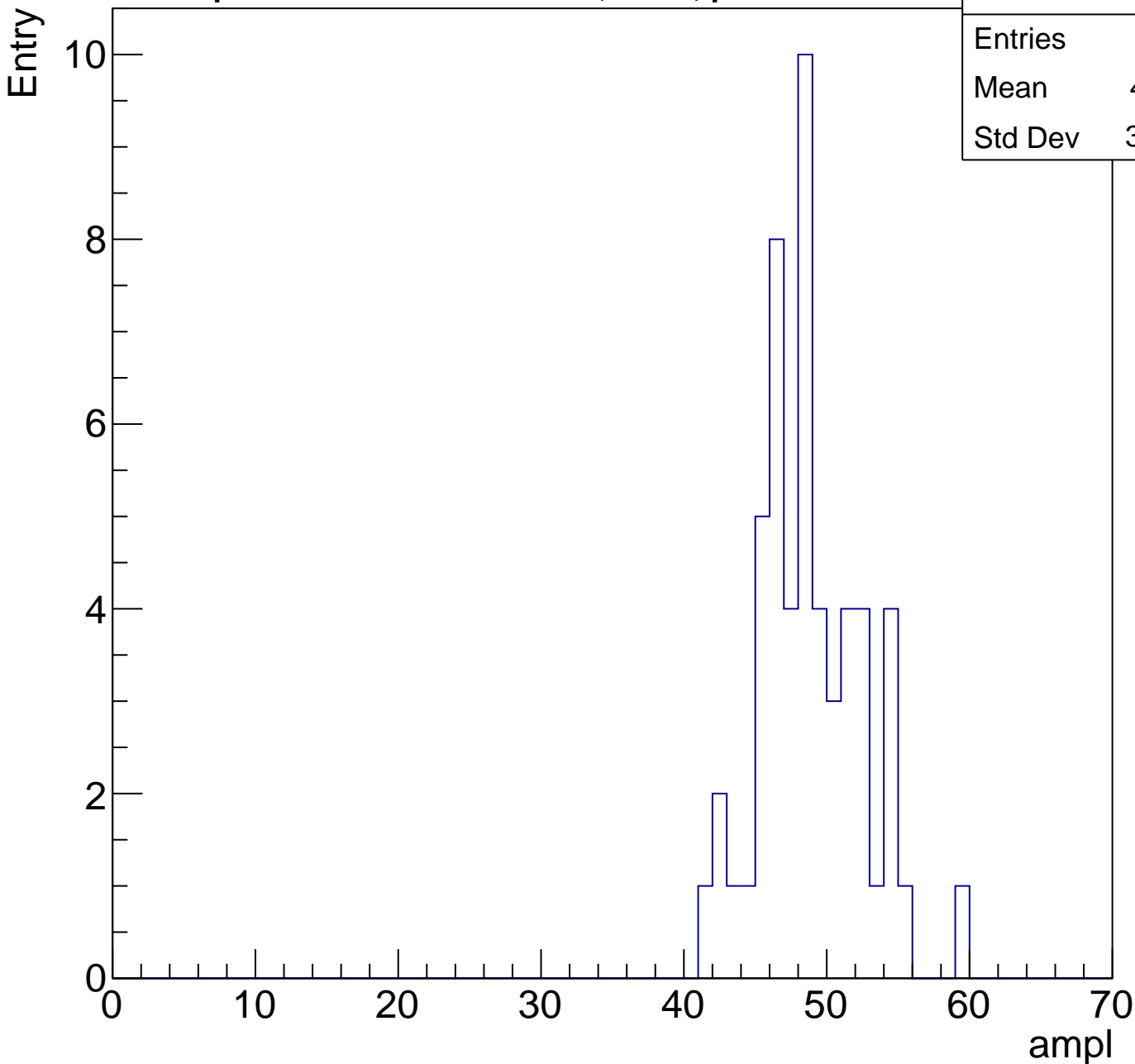
**Gaus Width: 3.4336**



# B1L101S, U3-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	54
Mean	48.41
Std Dev	3.572

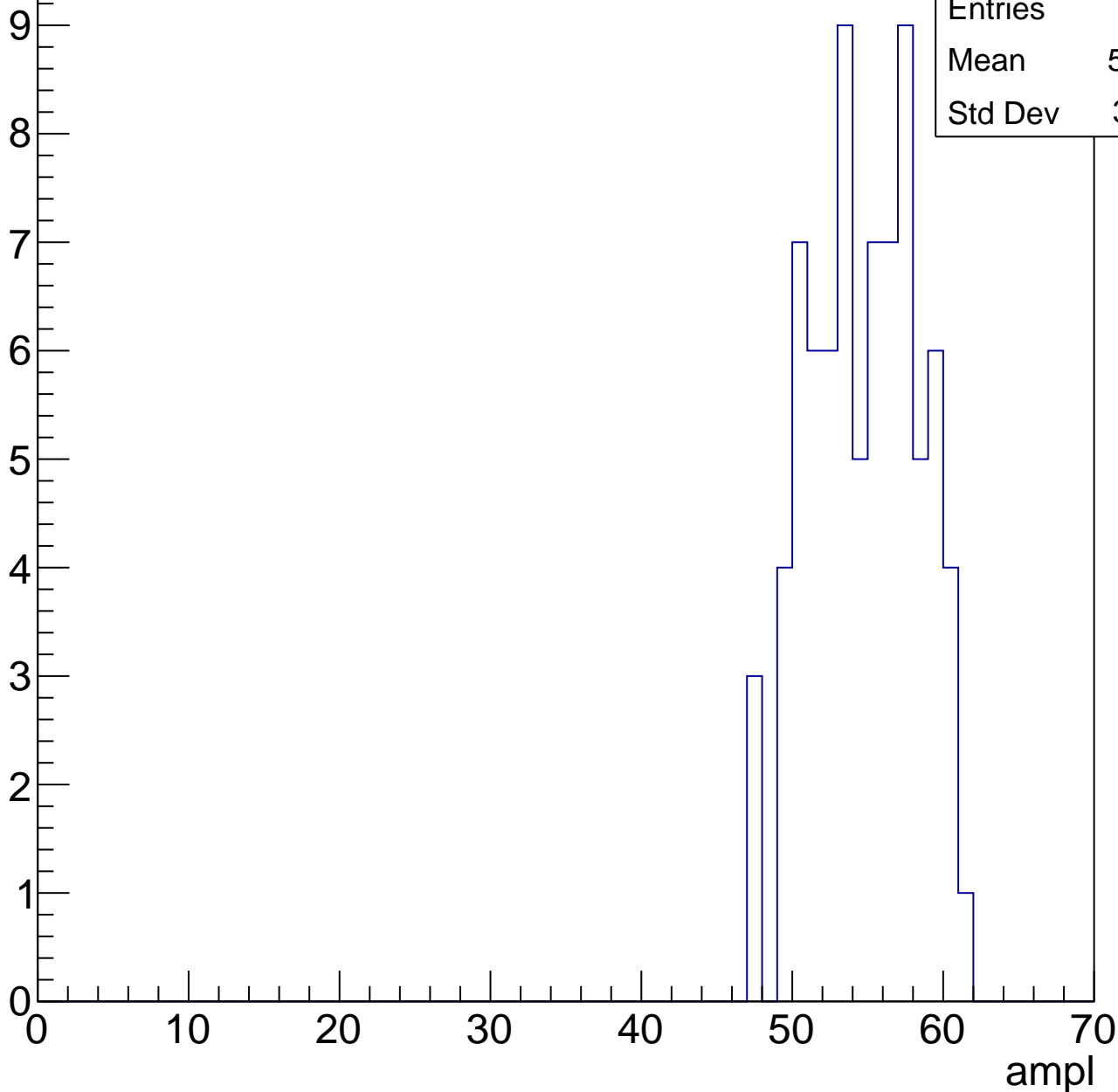


# B1L101S, U3-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	54.27
Std Dev	3.521

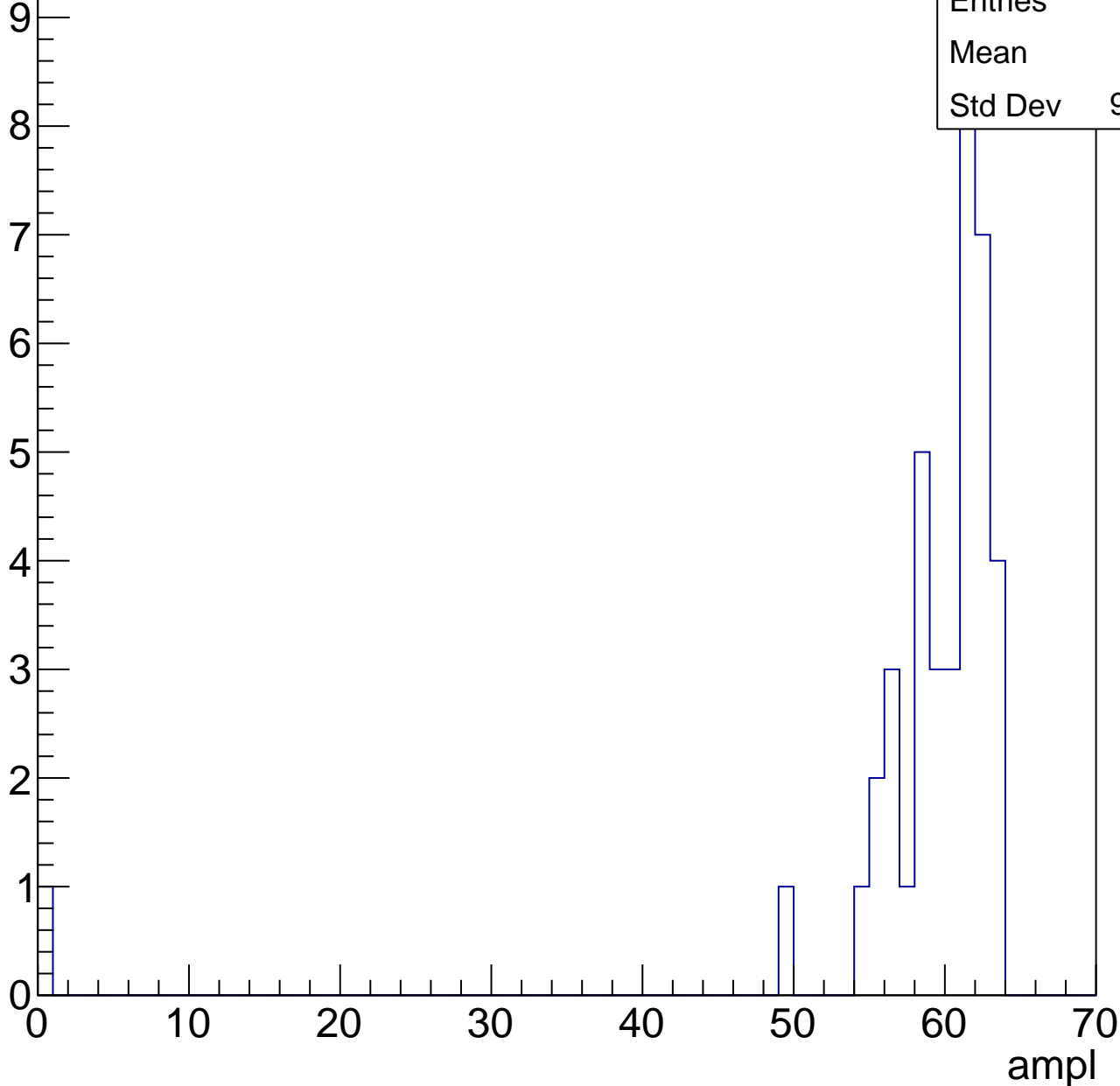


# B1L101S, U3-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	40
Mean	58
Std Dev	9.747

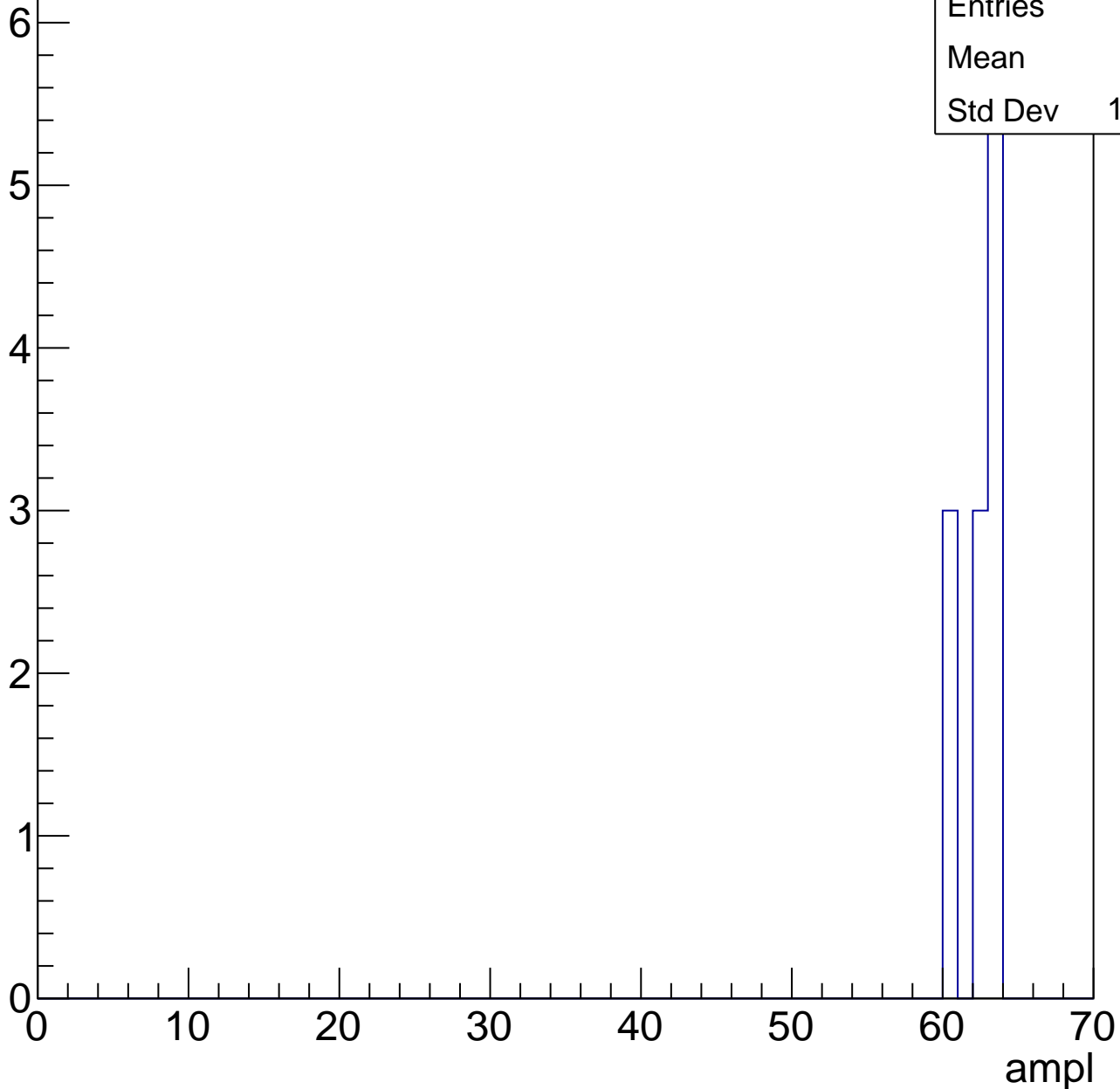


# B1L101S, U3-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	12
Mean	62
Std Dev	1.225





# B1L101S, U3-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U3-ch17, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	80
Mean	29.88
Std Dev	5.088

**Gaus mean : 30.4295**

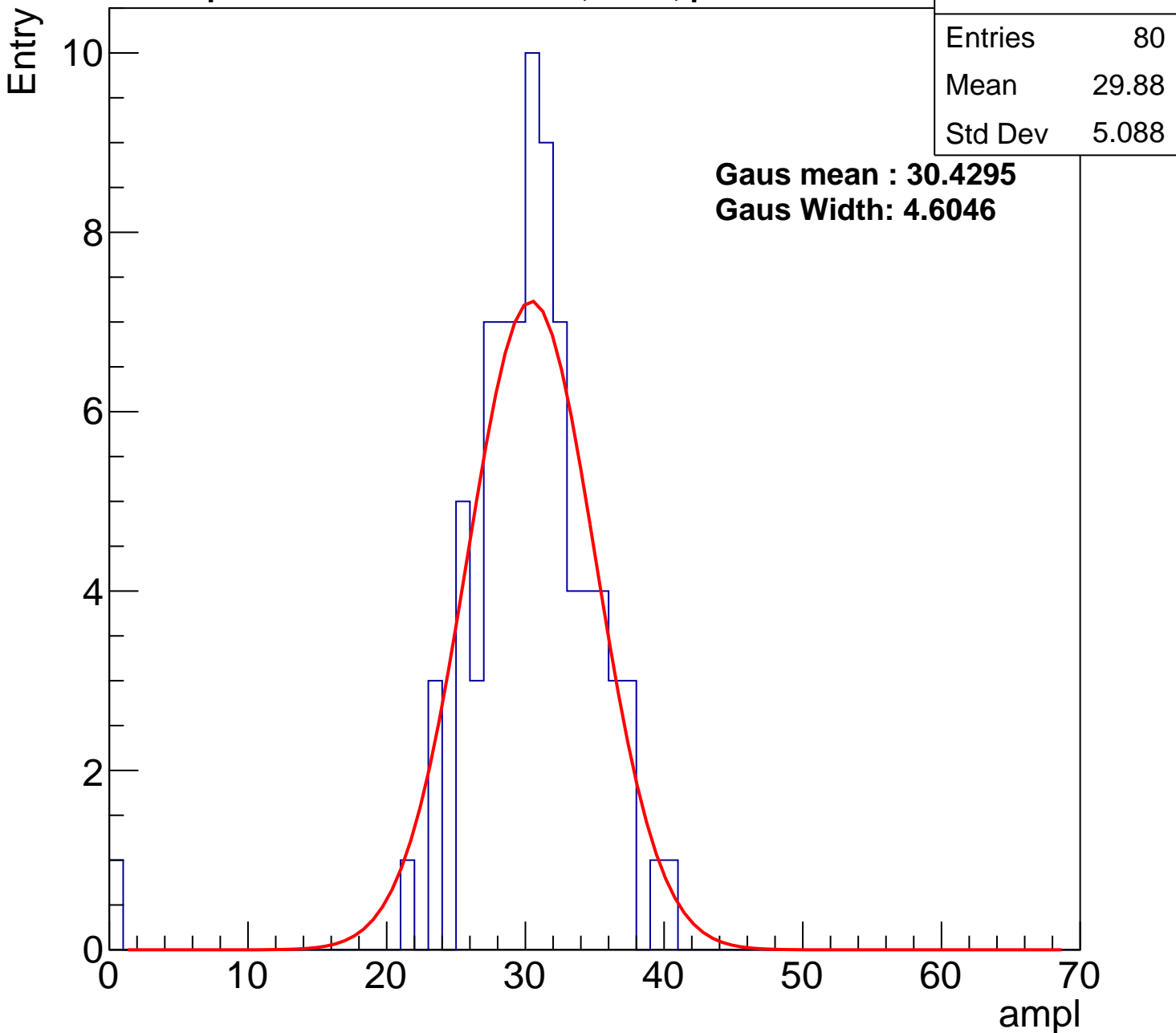
**Gaus Width: 4.6046**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U3-ch17, adc1

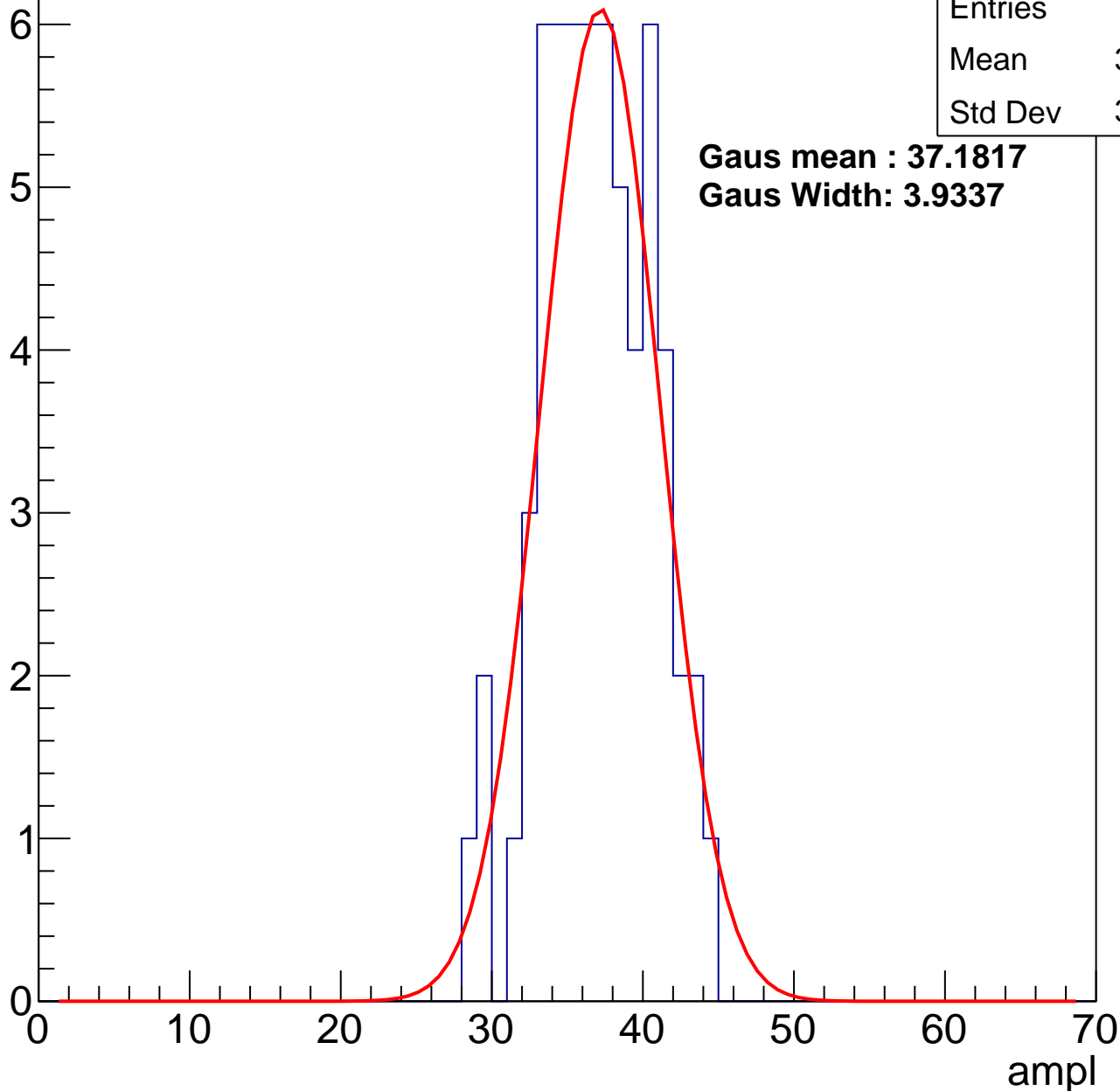
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	36.51
Std Dev	3.611

**Gaus mean : 37.1817**

**Gaus Width: 3.9337**



# B1L101S, U3-ch17, adc2

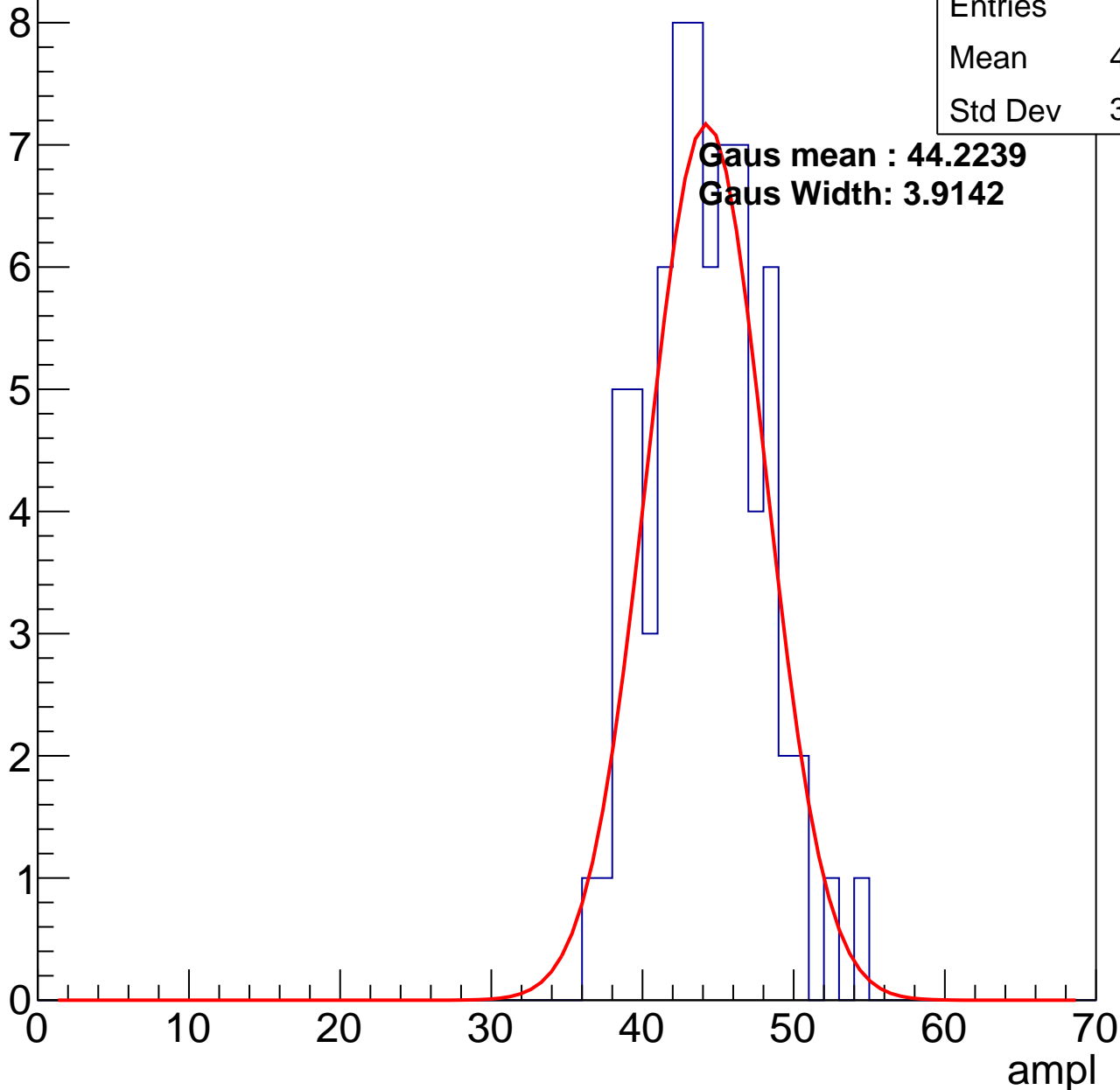
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	43.63
Std Dev	3.707

**Gaus mean : 44.2239**

**Gaus Width: 3.9142**



# B1L101S, U3-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	62
Mean	50.11
Std Dev	3.163

Entry

10

8

6

4

2

0

0

10

20

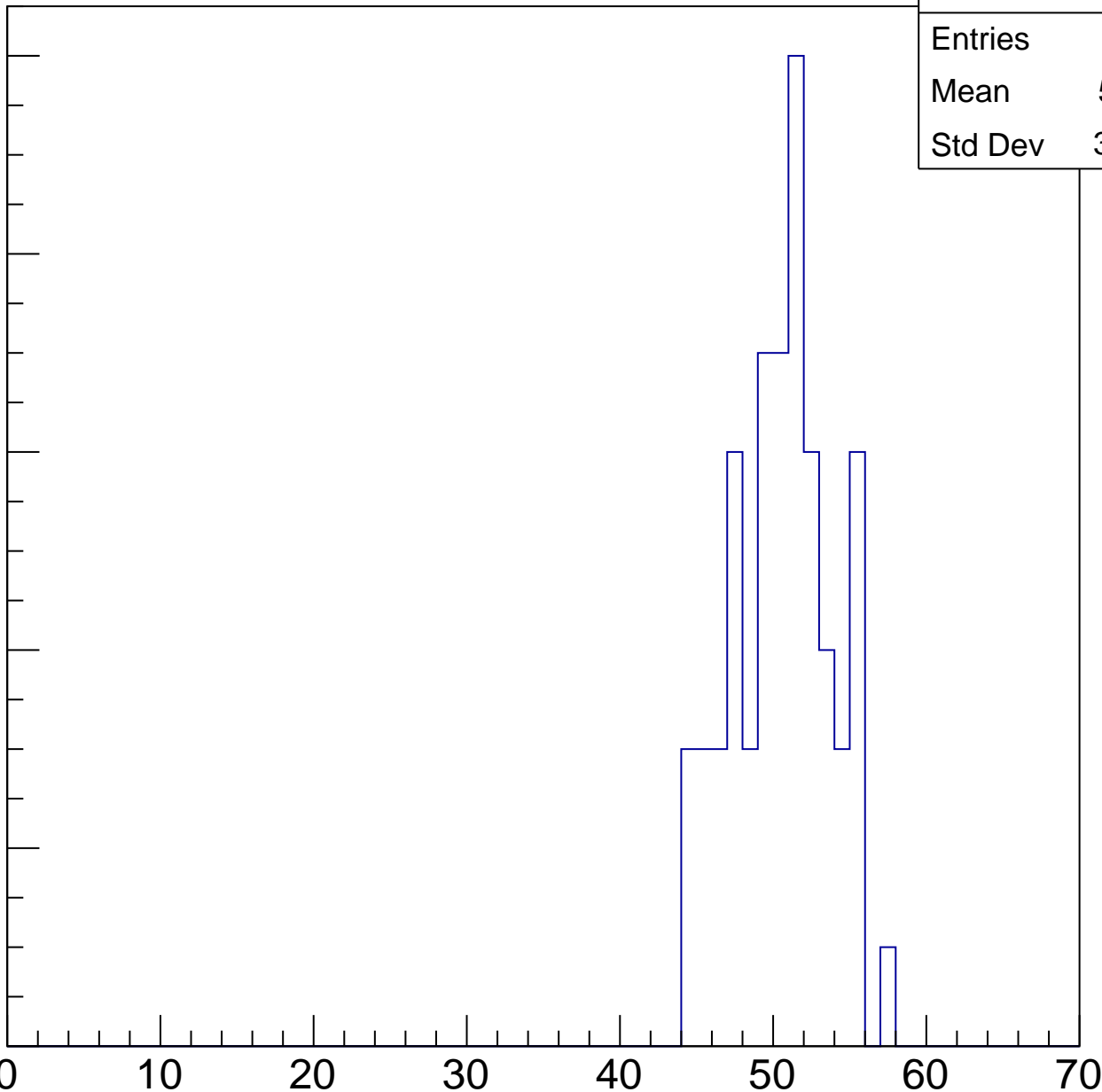
30

40

50

60

ampl



# B1L101S, U3-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

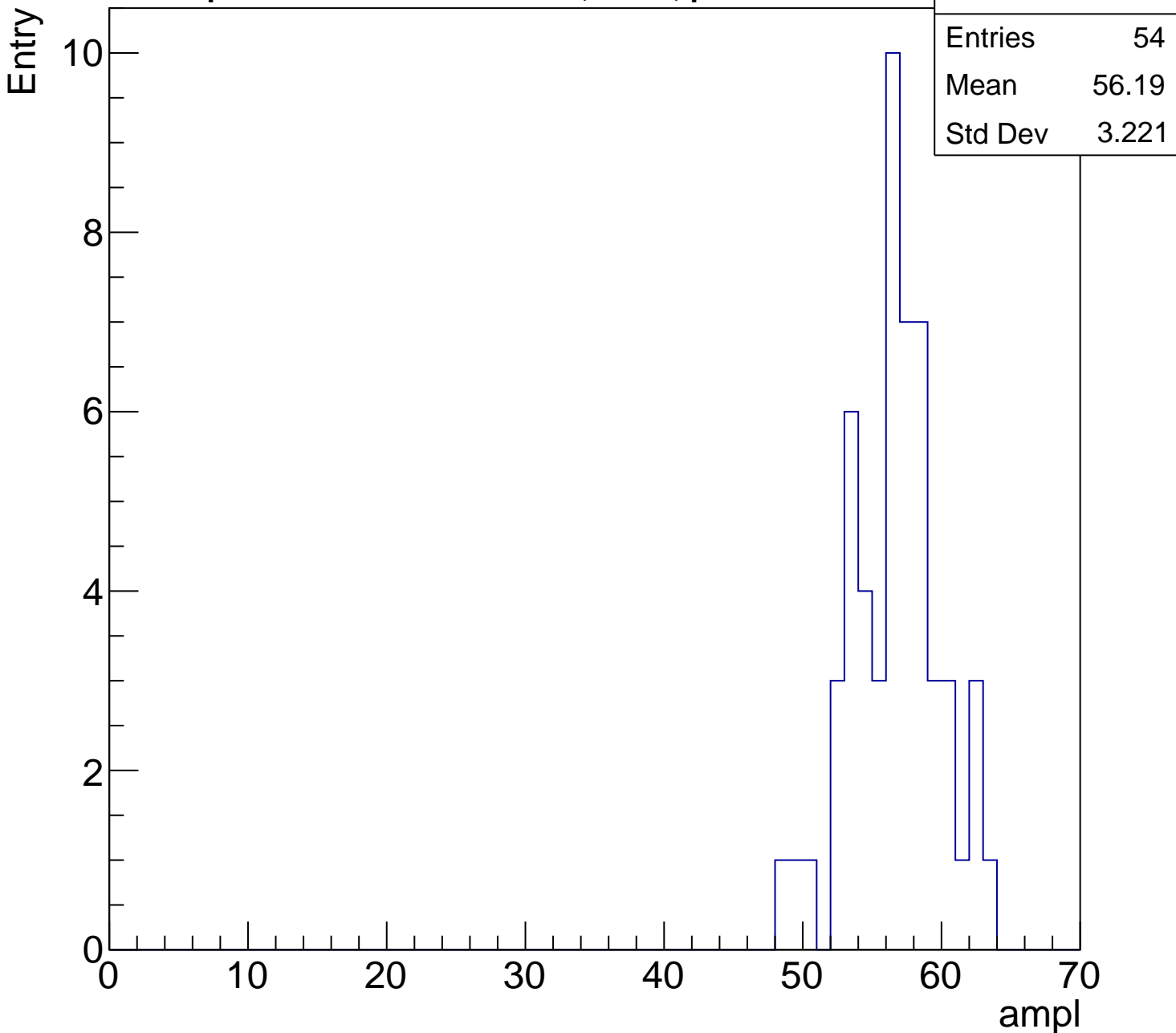
Entries	54
Mean	56.19
Std Dev	3.221

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

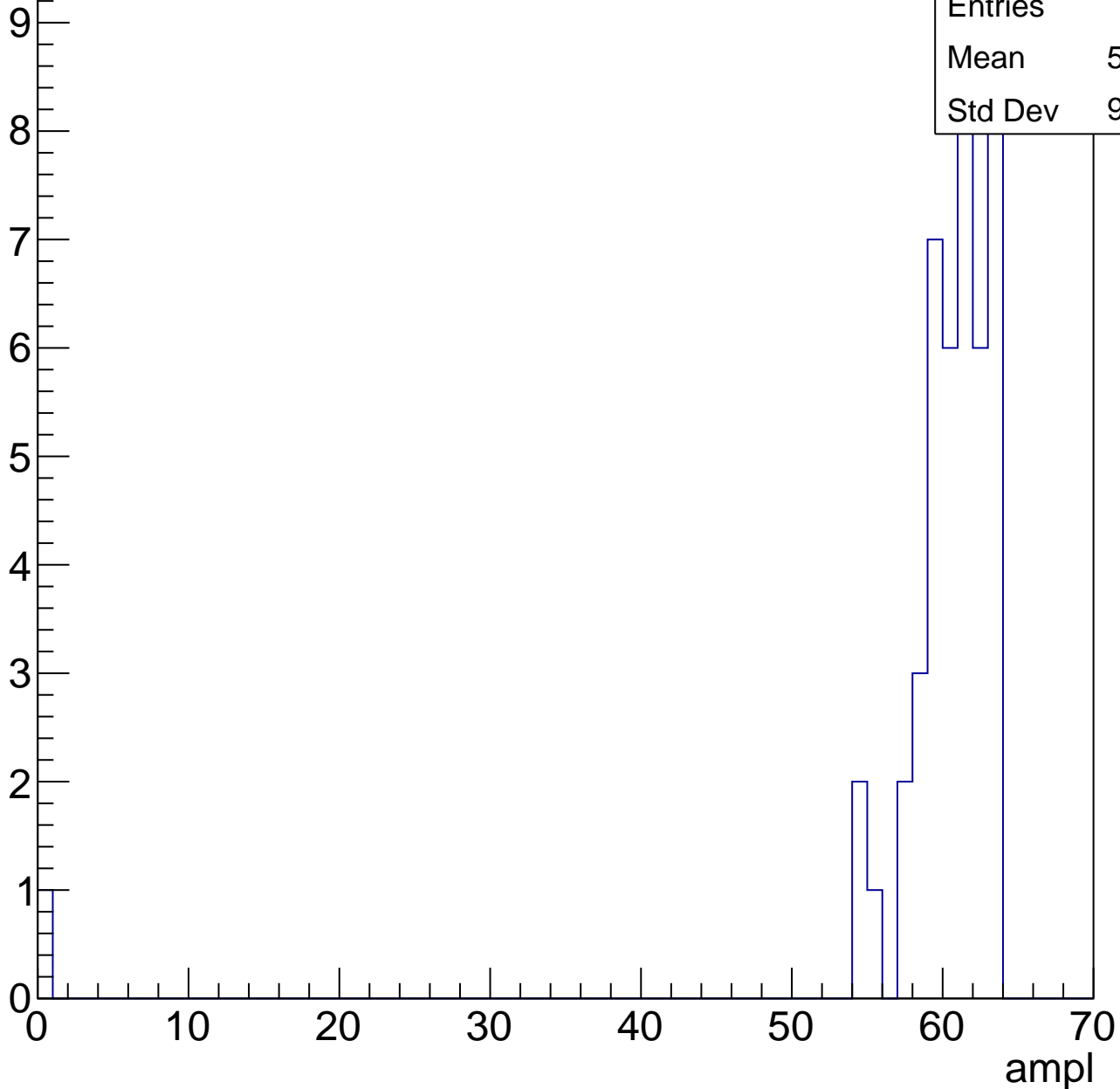


# B1L101S, U3-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

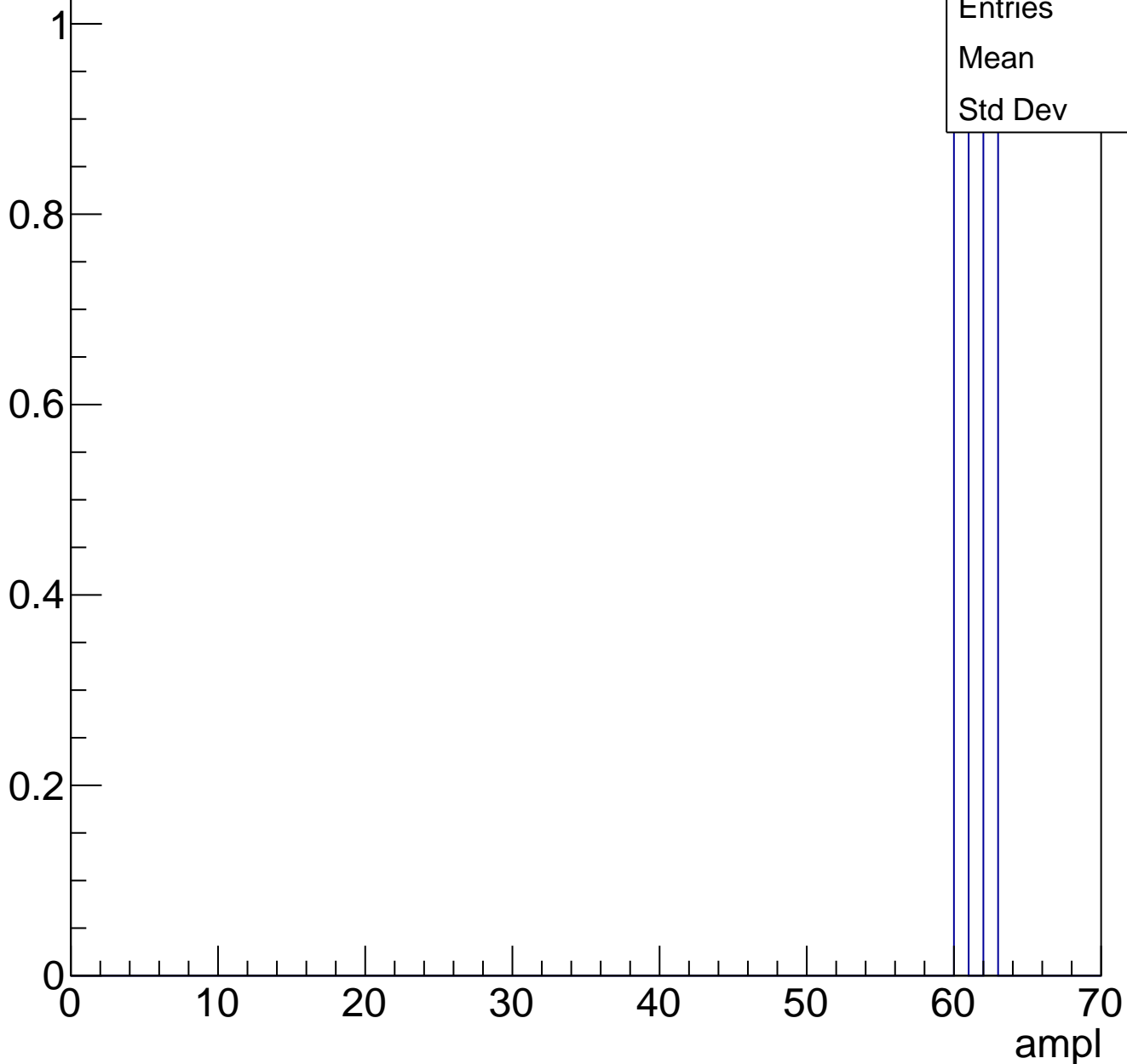
Entries	46
Mean	58.96
Std Dev	9.086



# B1L101S, U3-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U3-ch18, adc0

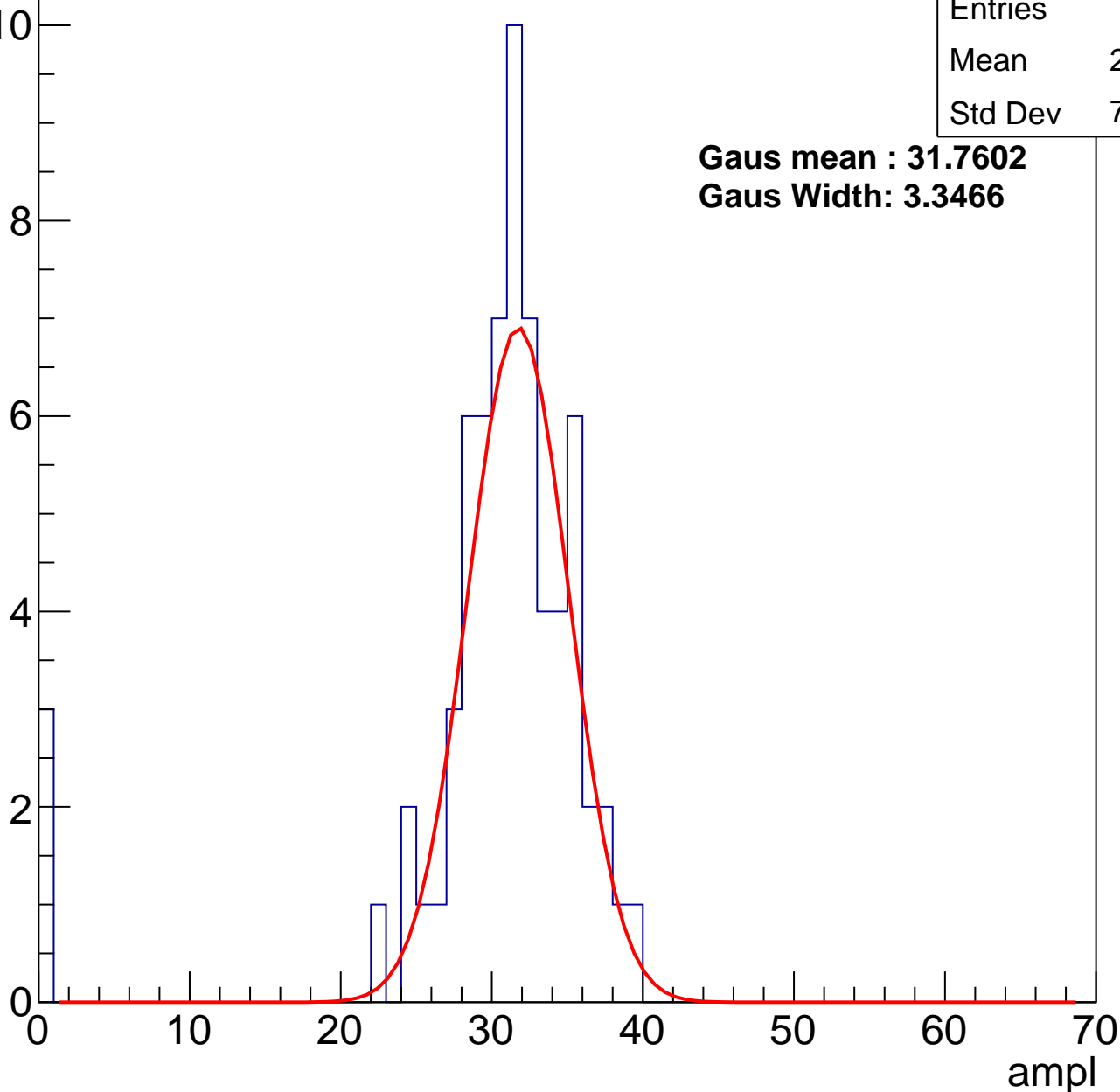
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	29.69
Std Dev	7.259

**Gaus mean : 31.7602**

**Gaus Width: 3.3466**



# B1L101S, U3-ch18, adc1

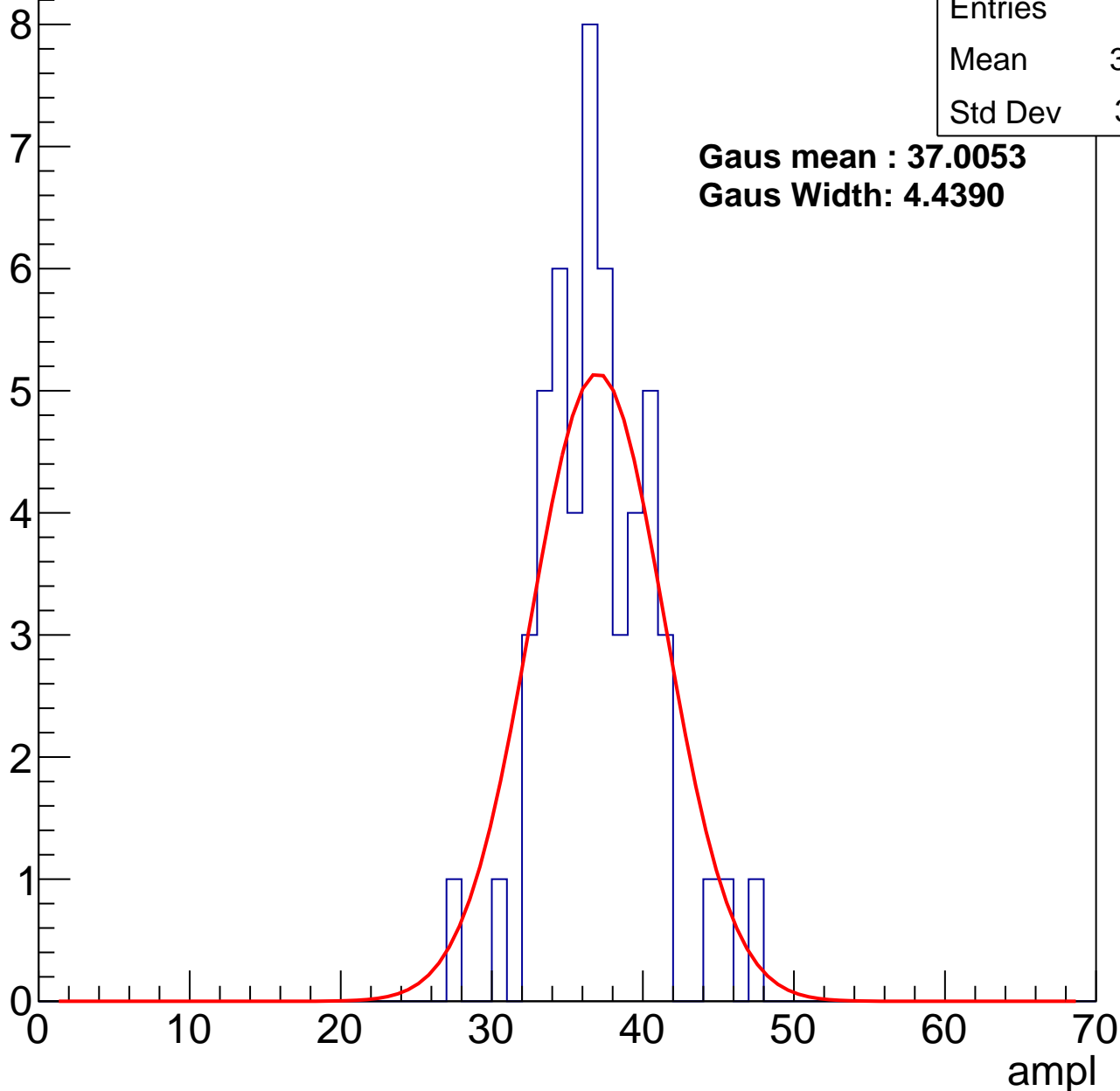
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	36.56
Std Dev	3.661

**Gaus mean : 37.0053**

**Gaus Width: 4.4390**



# B1L101S, U3-ch18, adc2

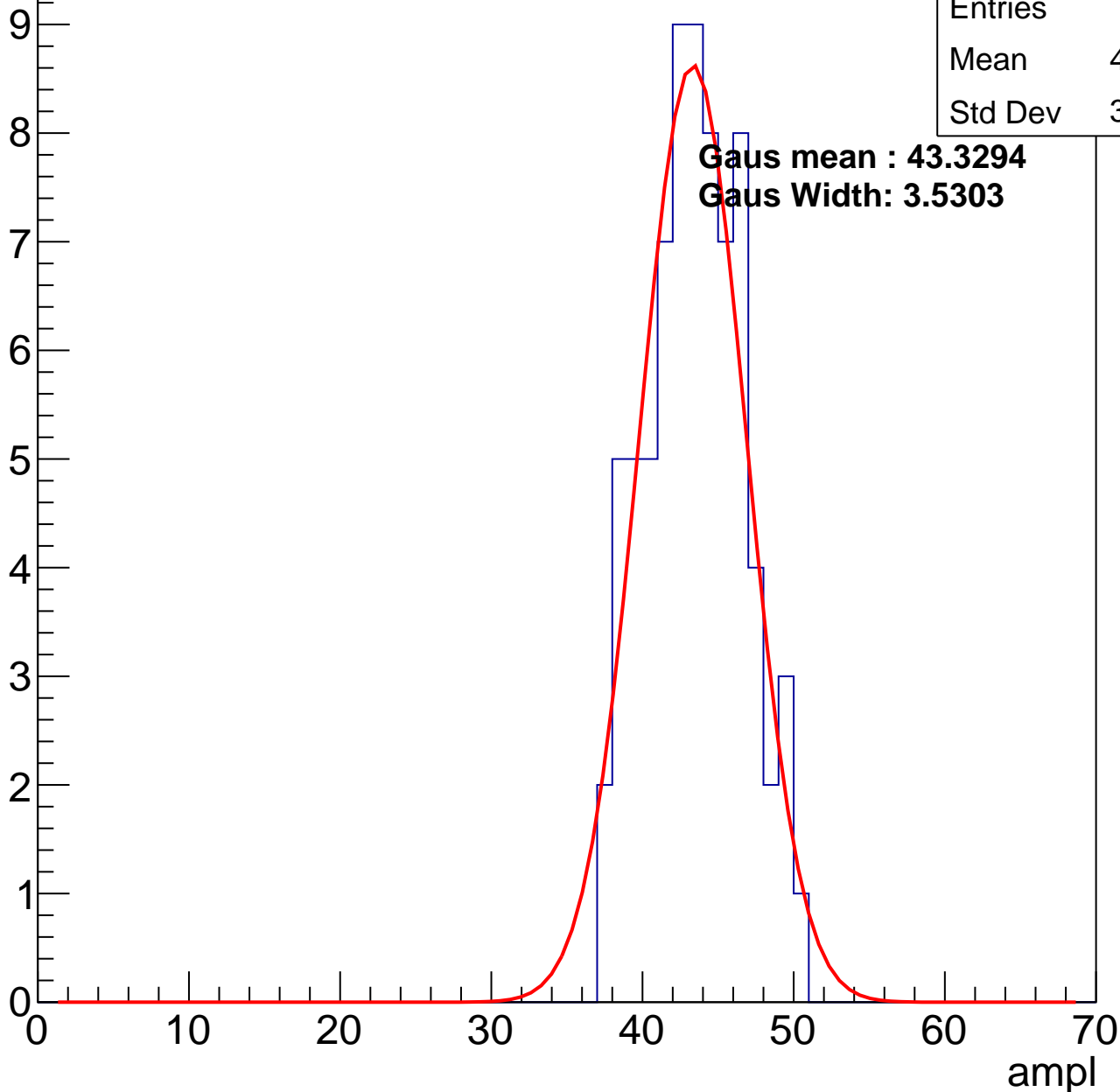
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	43.03
Std Dev	3.137

**Gaus mean : 43.3294**

**Gaus Width: 3.5303**

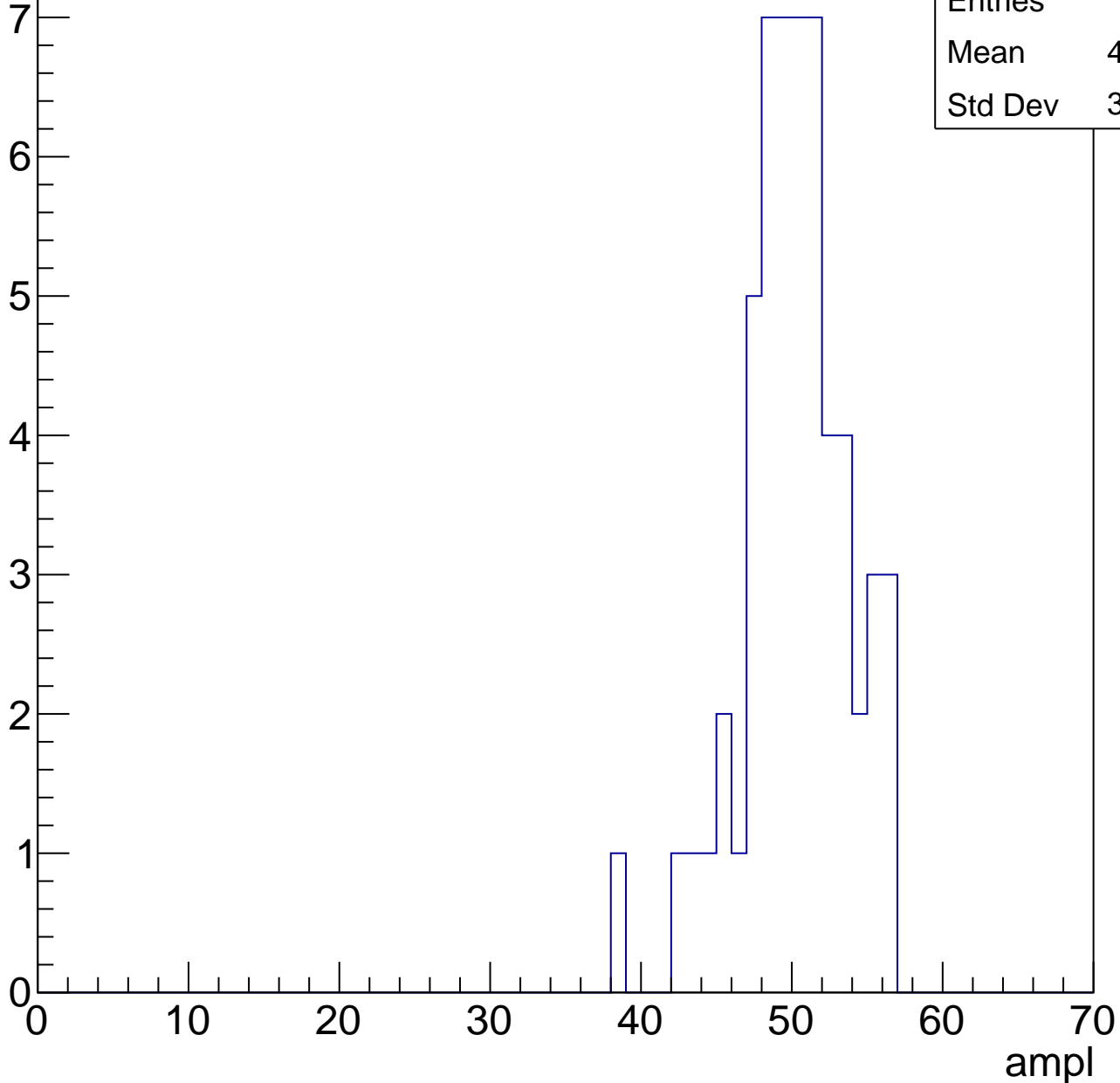


# B1L101S, U3-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	49.73
Std Dev	3.558

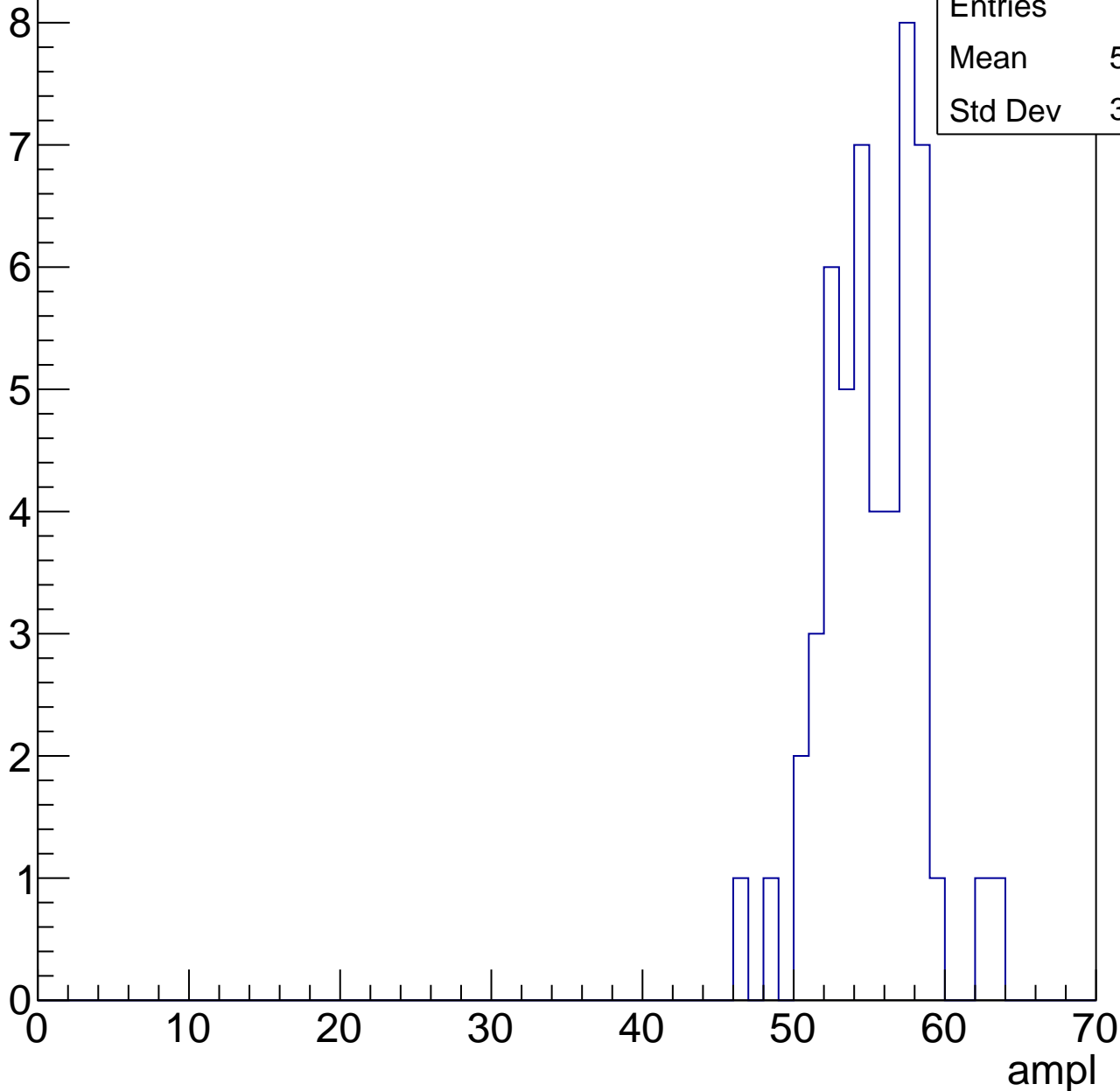


# B1L101S, U3-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	54.75
Std Dev	3.235



# B1L101S, U3-ch18, adc5

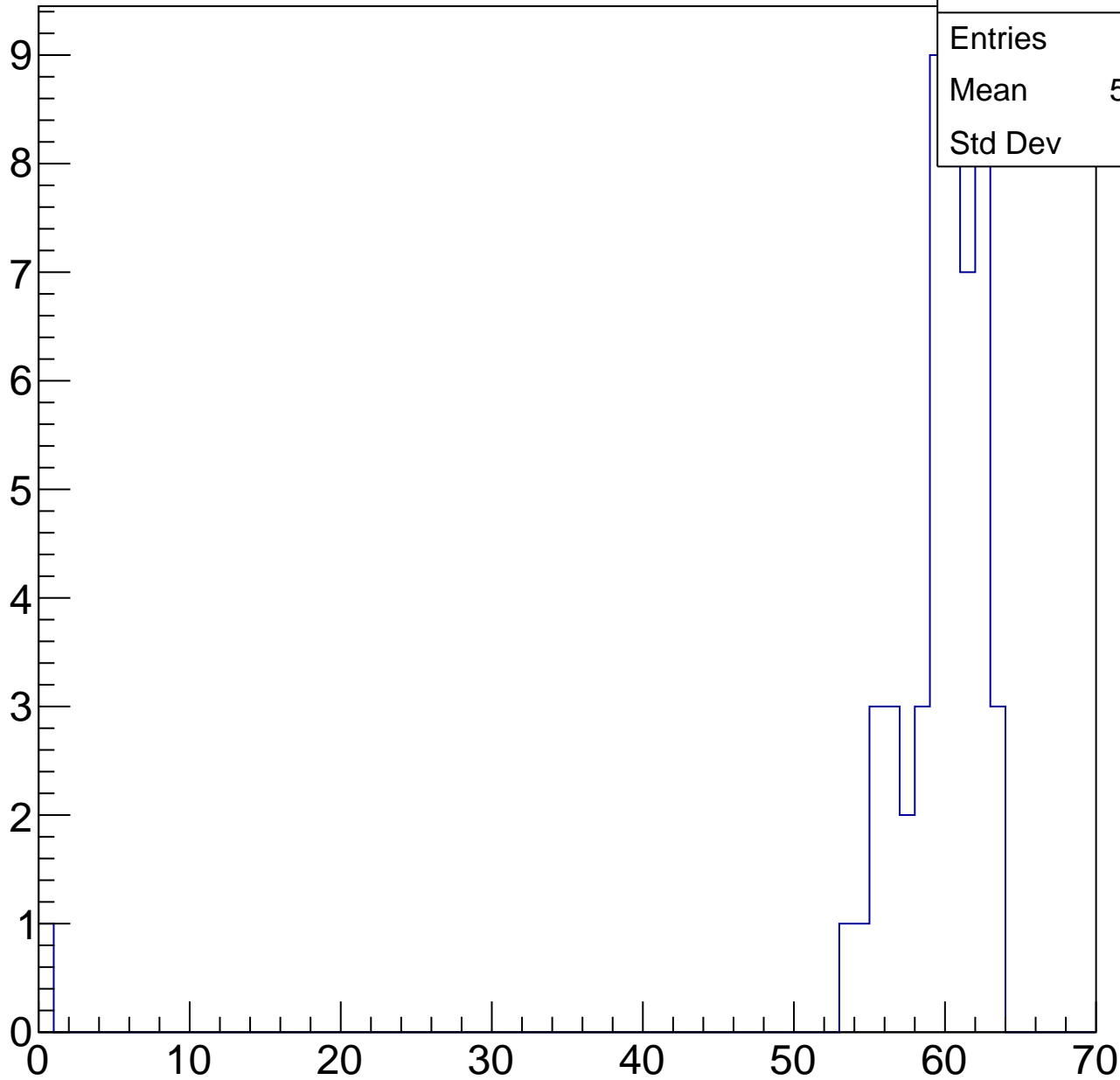
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	58.18
Std Dev	8.75

ampl

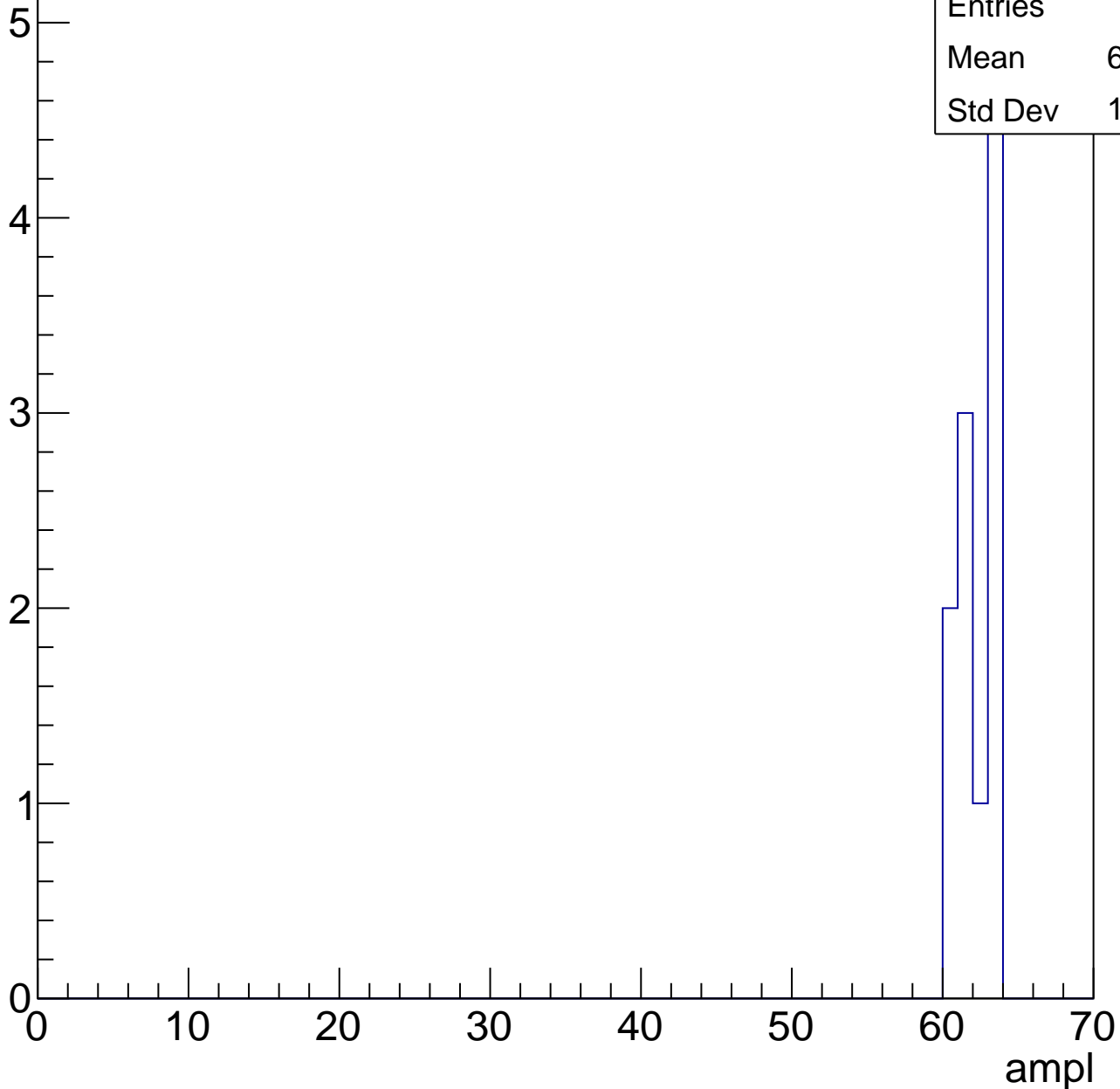


# B1L101S, U3-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	11
Mean	61.82
Std Dev	1.192





# B1L101S, U3-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L101S, U3-ch19, adc0

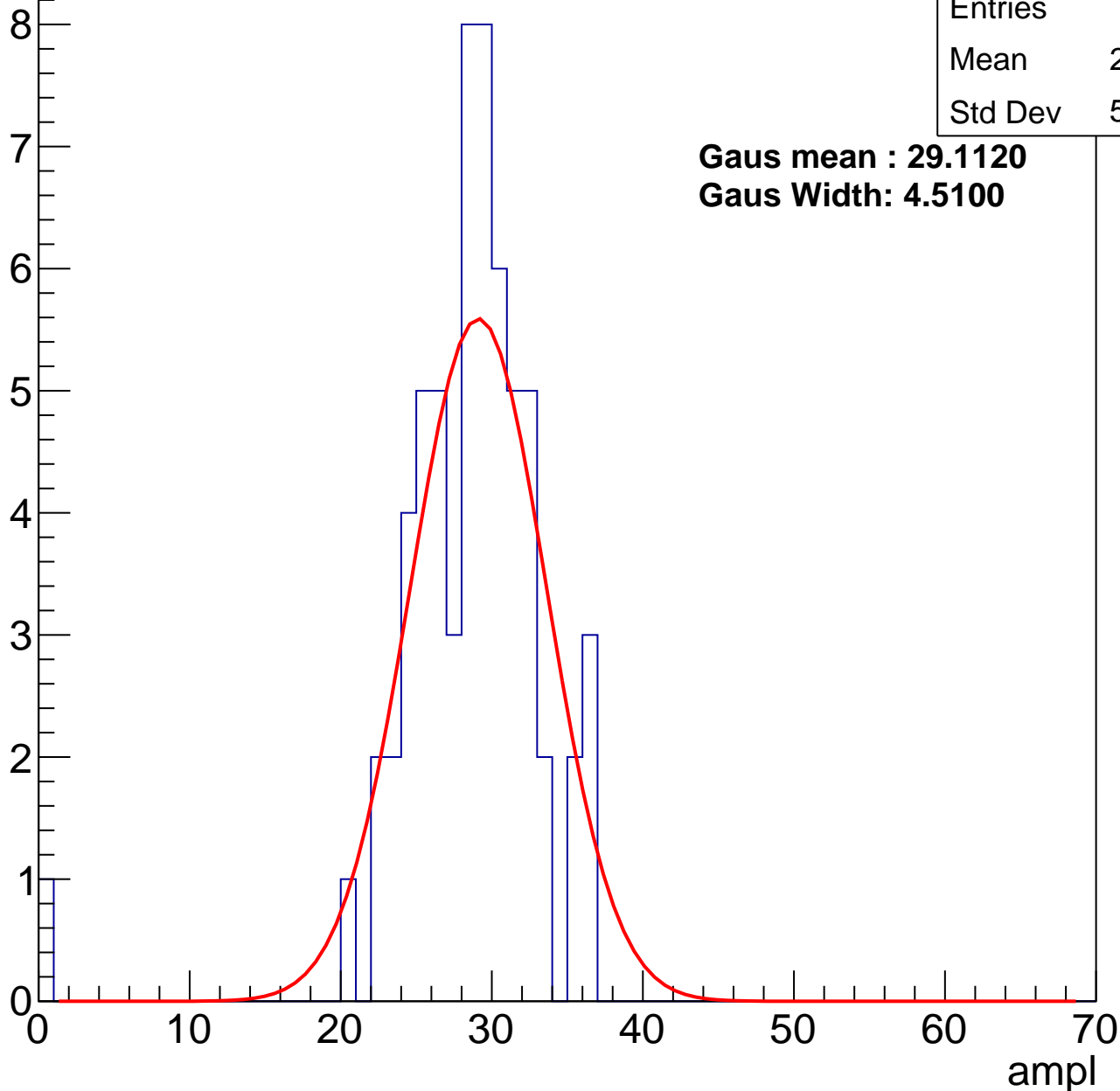
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	28.02
Std Dev	5.078

**Gaus mean : 29.120**

**Gaus Width: 4.5100**



# B1L101S, U3-ch19, adc1

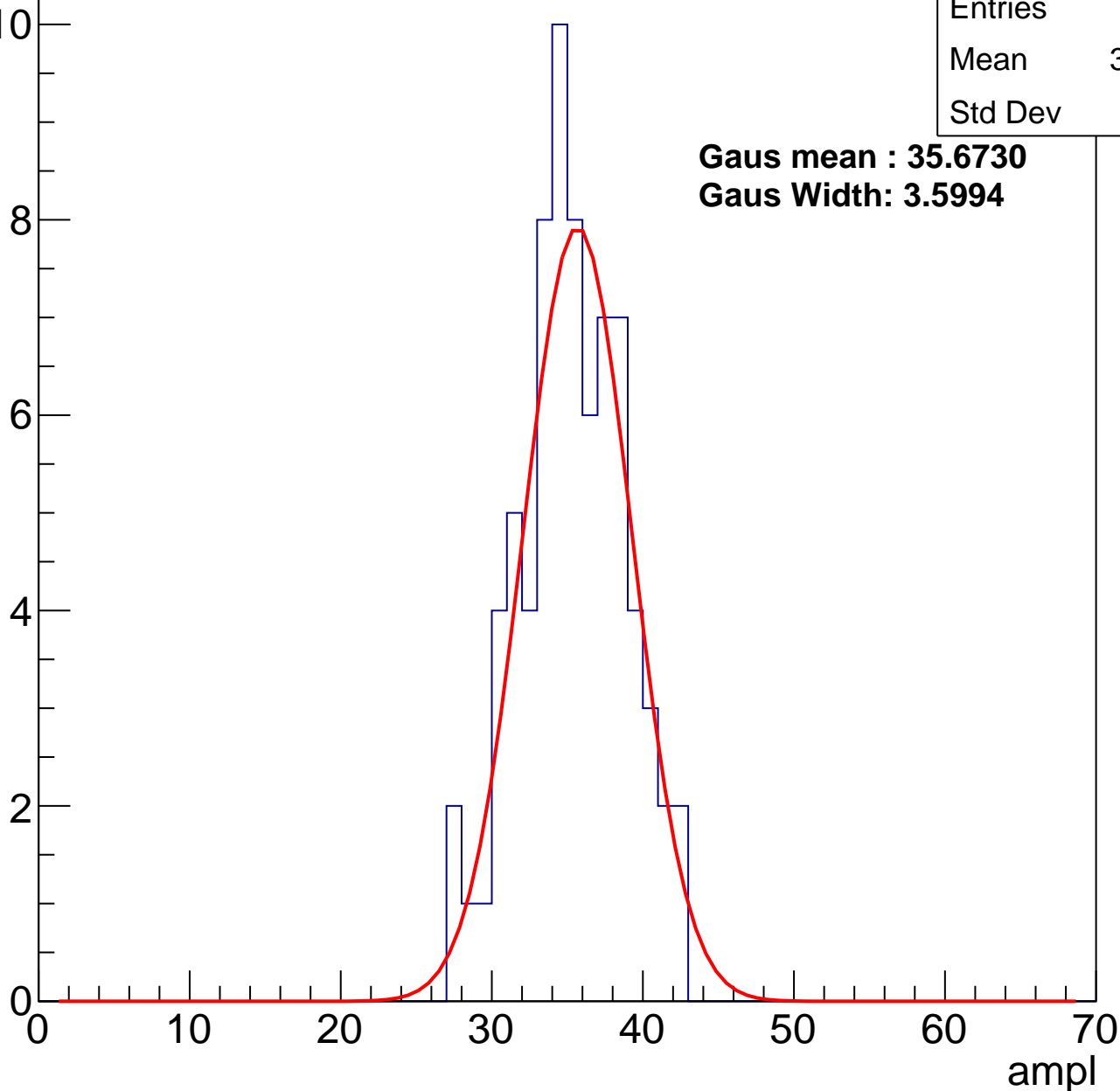
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	34.88
Std Dev	3.44

**Gaus mean : 35.6730**

**Gaus Width: 3.5994**



# B1L101S, U3-ch19, adc2

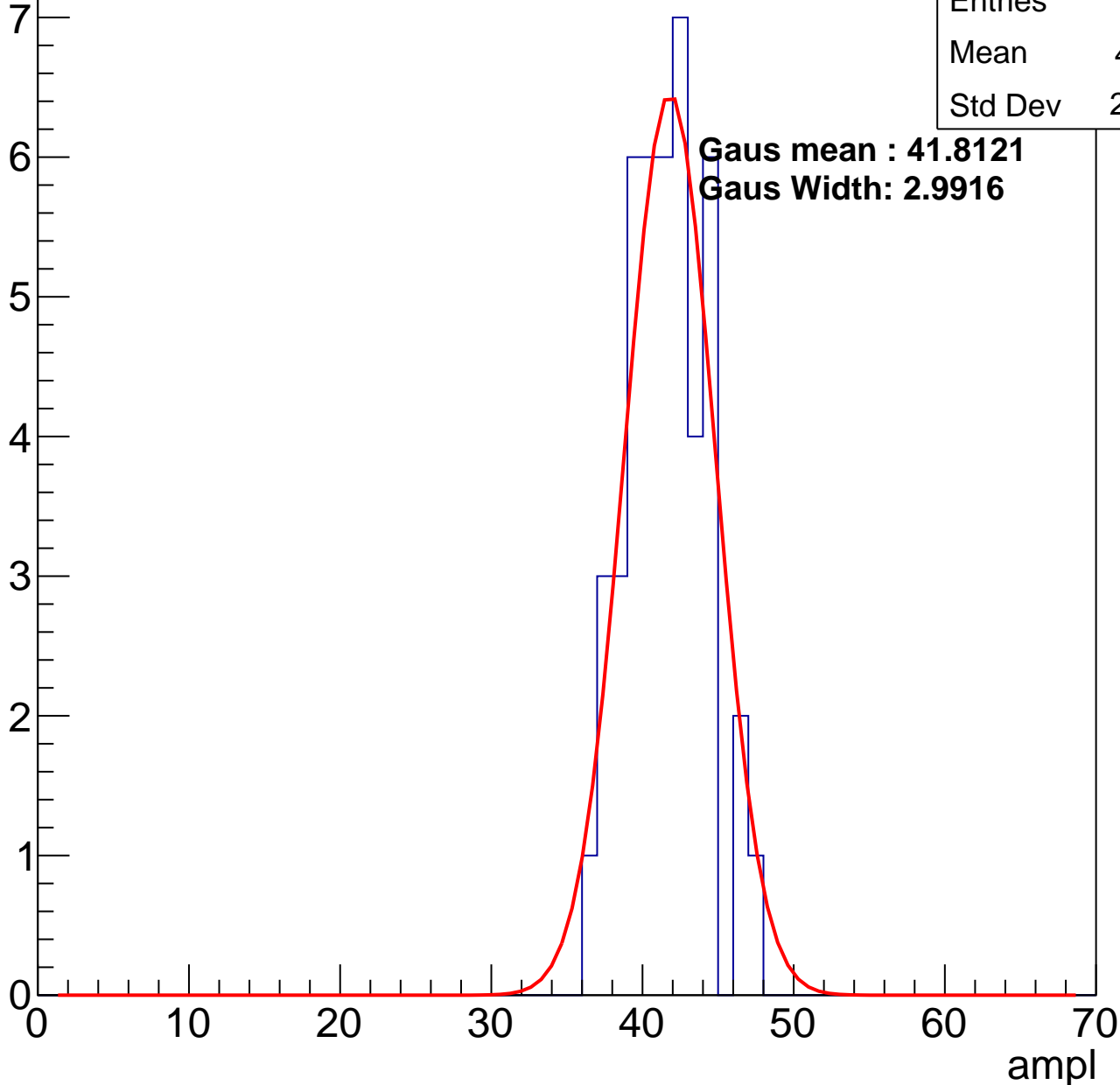
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	41.11
Std Dev	2.549

**Gaus mean : 41.8121**

**Gaus Width: 2.9916**

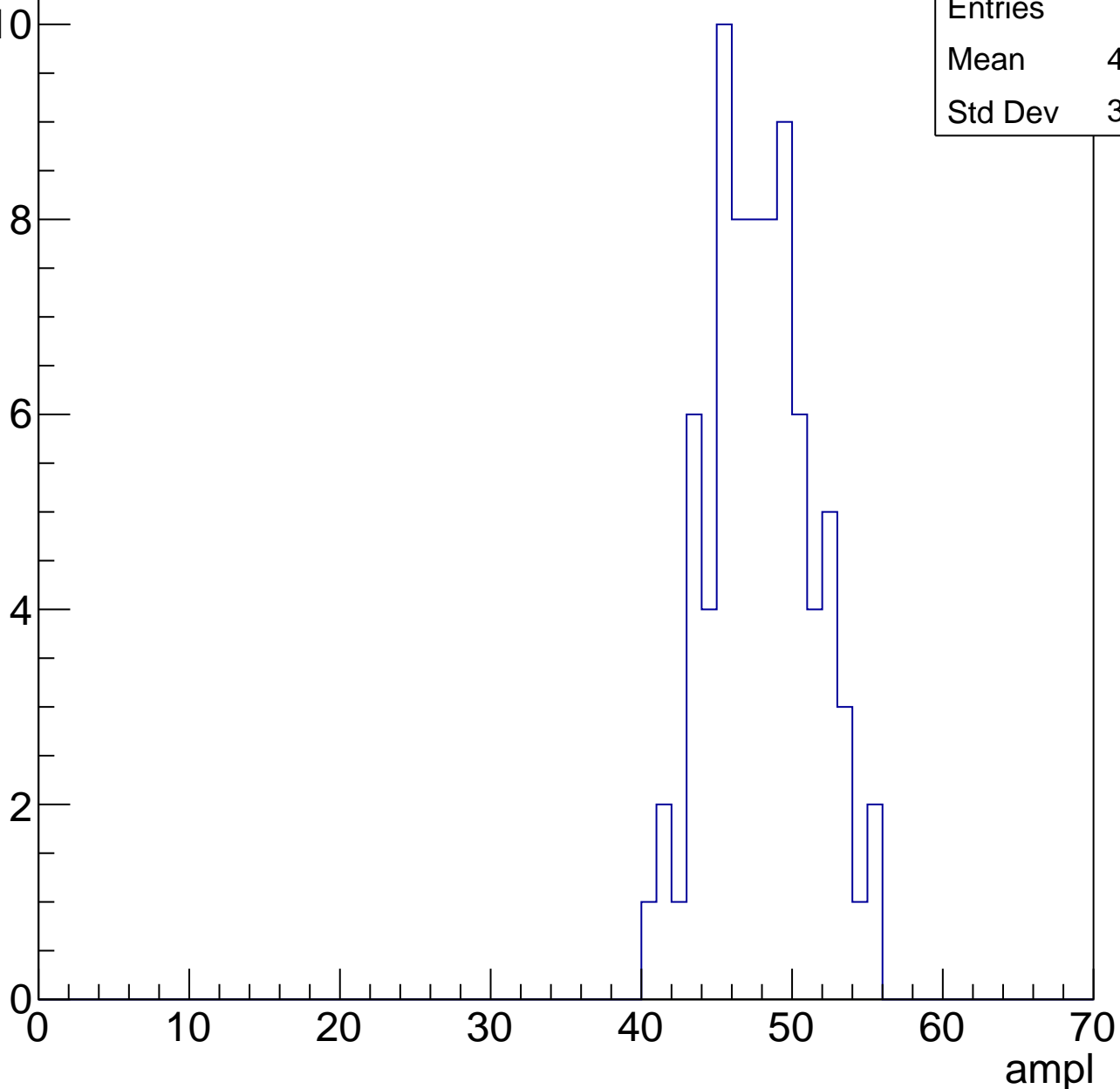


# B1L101S, U3-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	47.49
Std Dev	3.358

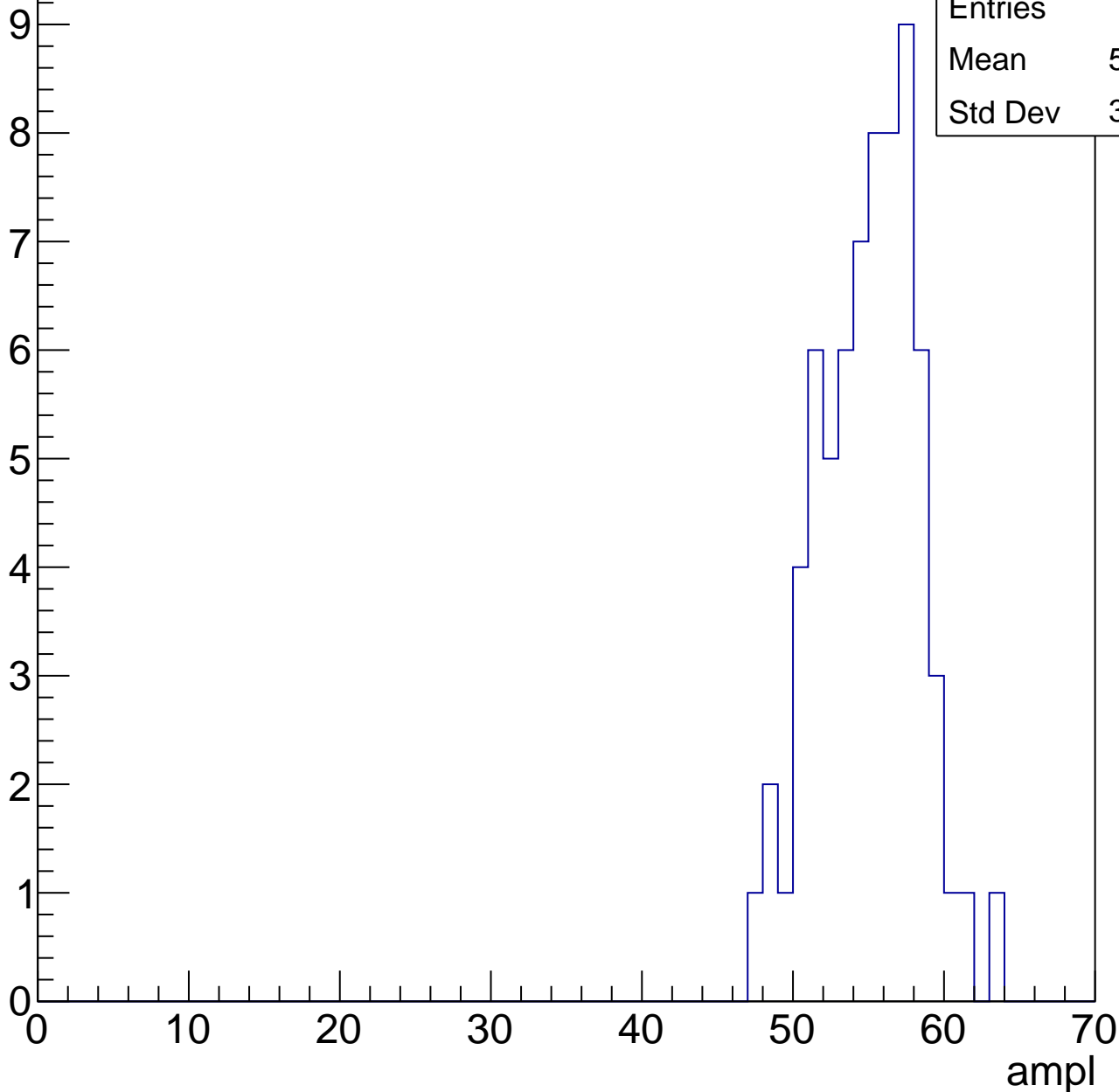


# B1L101S, U3-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

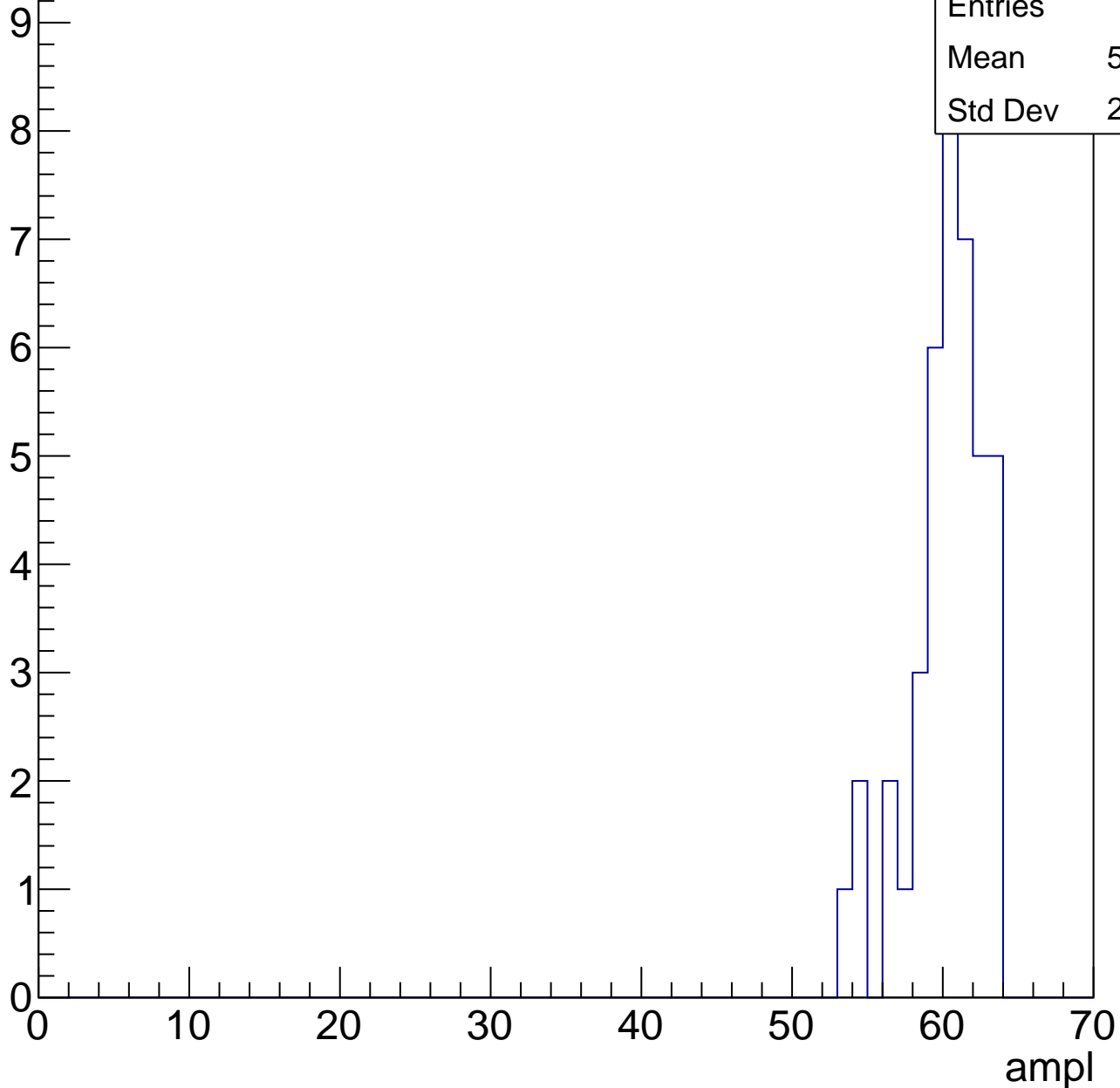
Entries	69
Mean	54.55
Std Dev	3.246



# B1L101S, U3-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

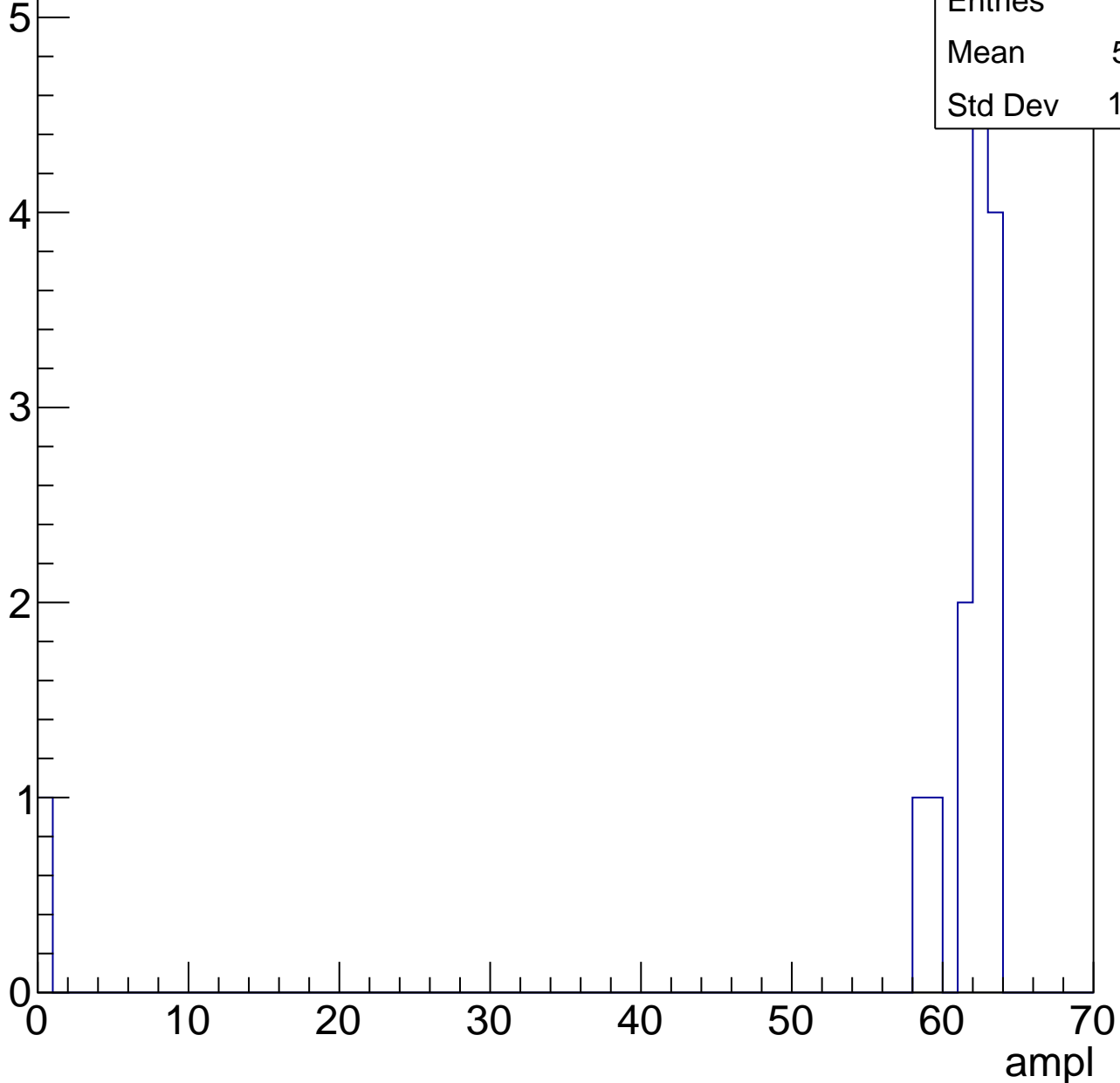


# B1L101S, U3-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	14
Mean	57.21
Std Dev	15.93





# B1L101S, U3-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U3-ch20, adc0

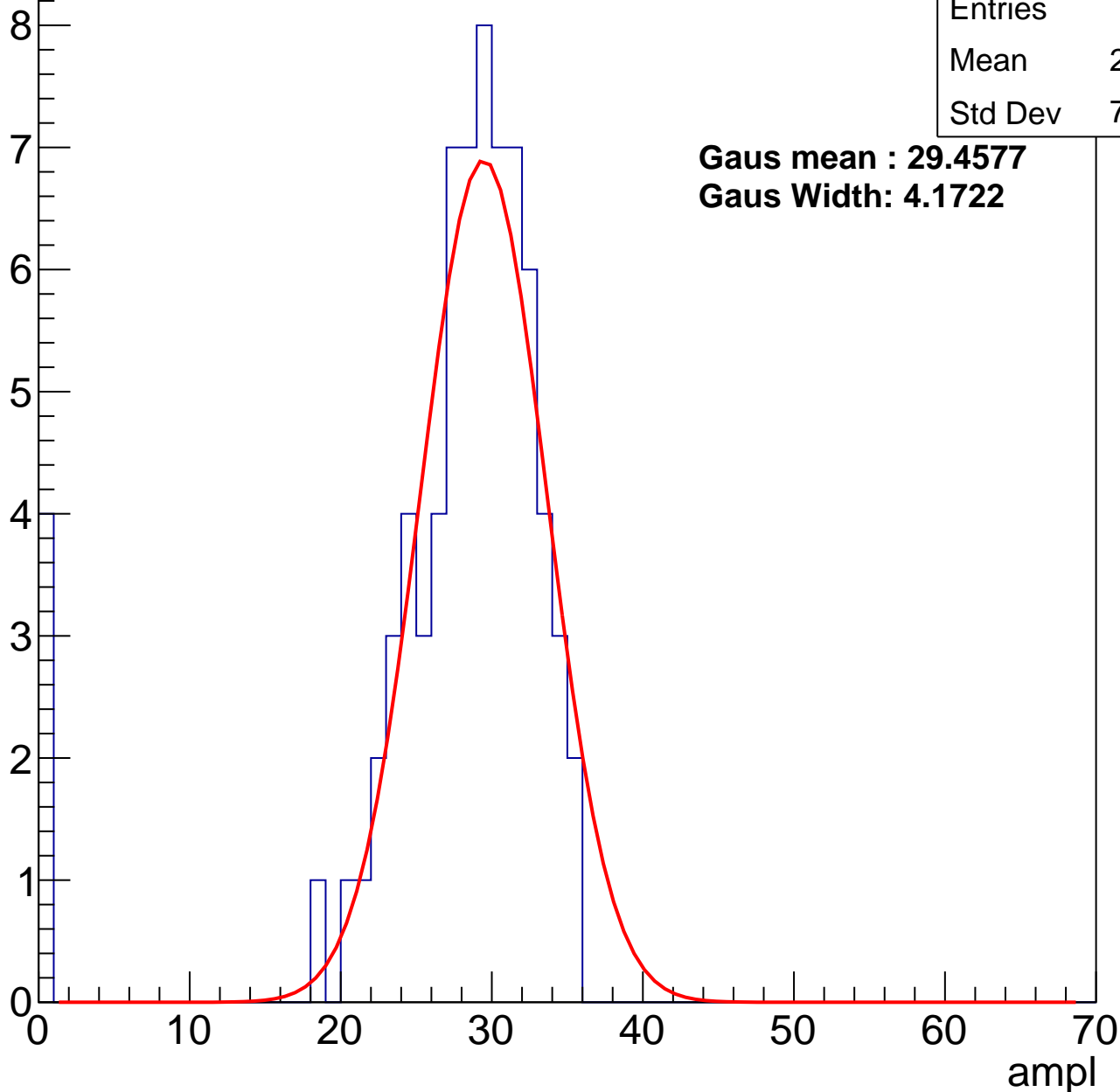
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	26.85
Std Dev	7.364

**Gaus mean : 29.4577**

**Gaus Width: 4.1722**



# B1L101S, U3-ch20, adc1

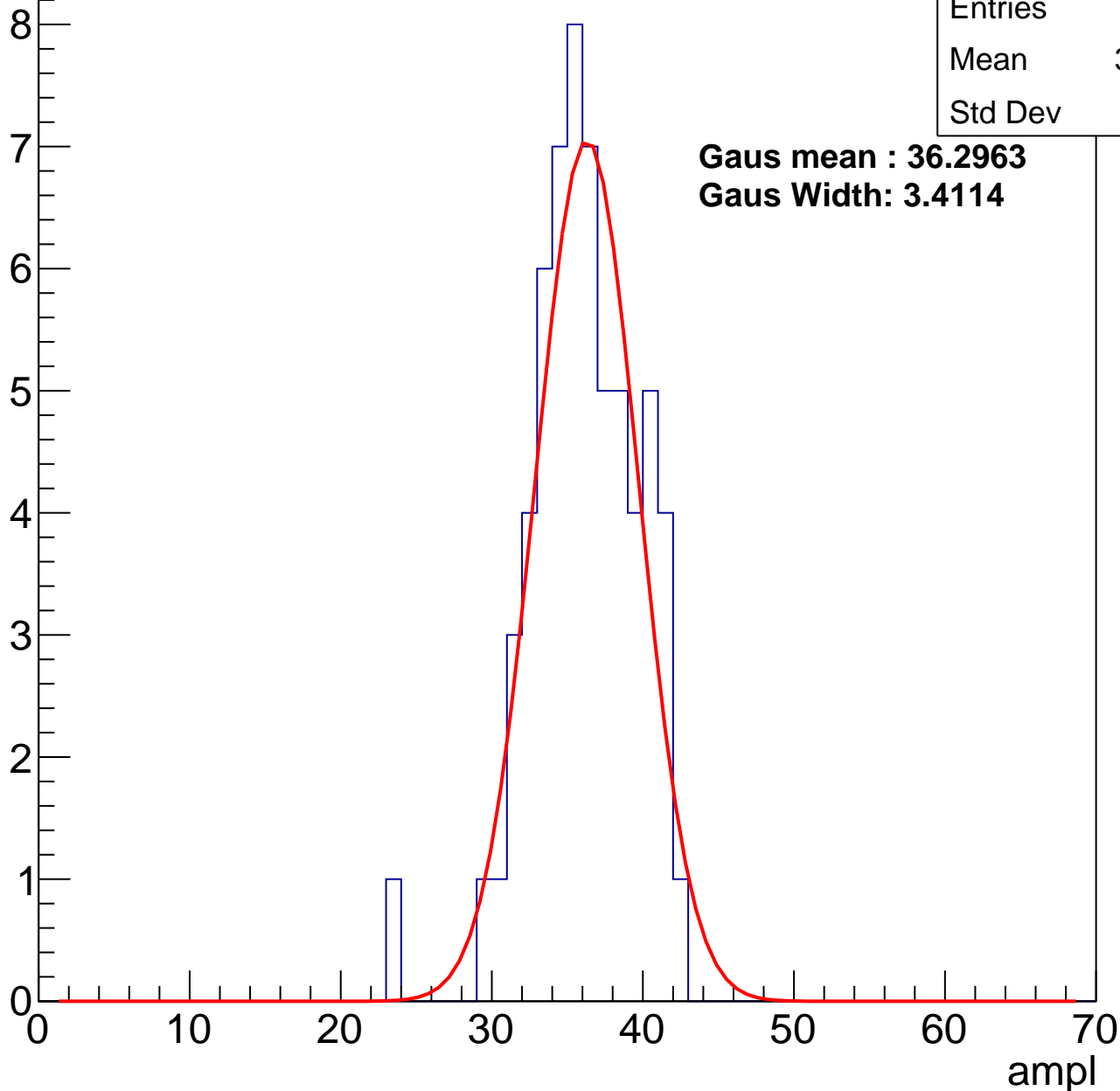
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	35.61
Std Dev	3.48

**Gaus mean : 36.2963**

**Gaus Width: 3.4114**



# B1L101S, U3-ch20, adc2

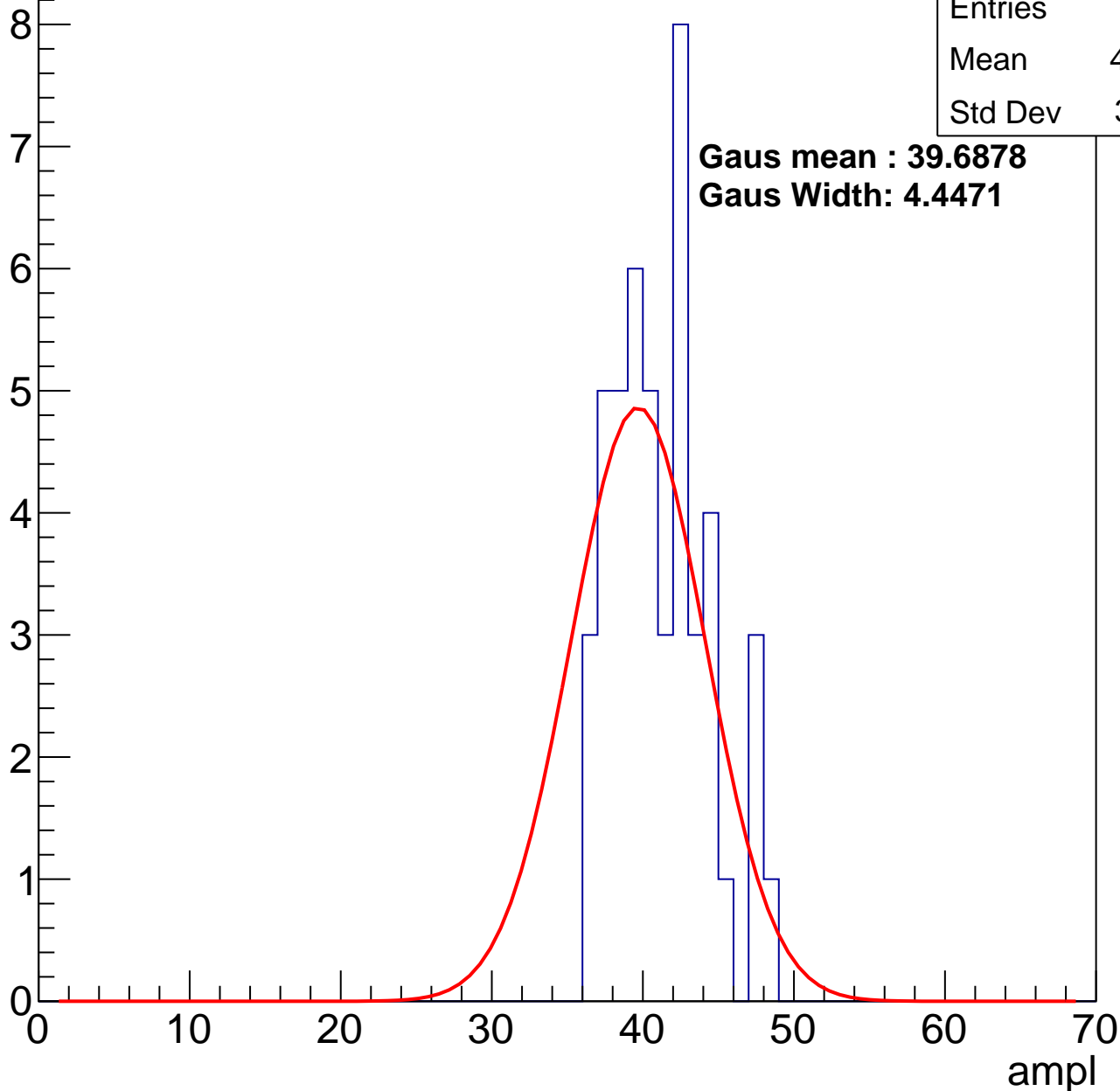
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	40.74
Std Dev	3.111

**Gaus mean : 39.6878**

**Gaus Width: 4.4471**

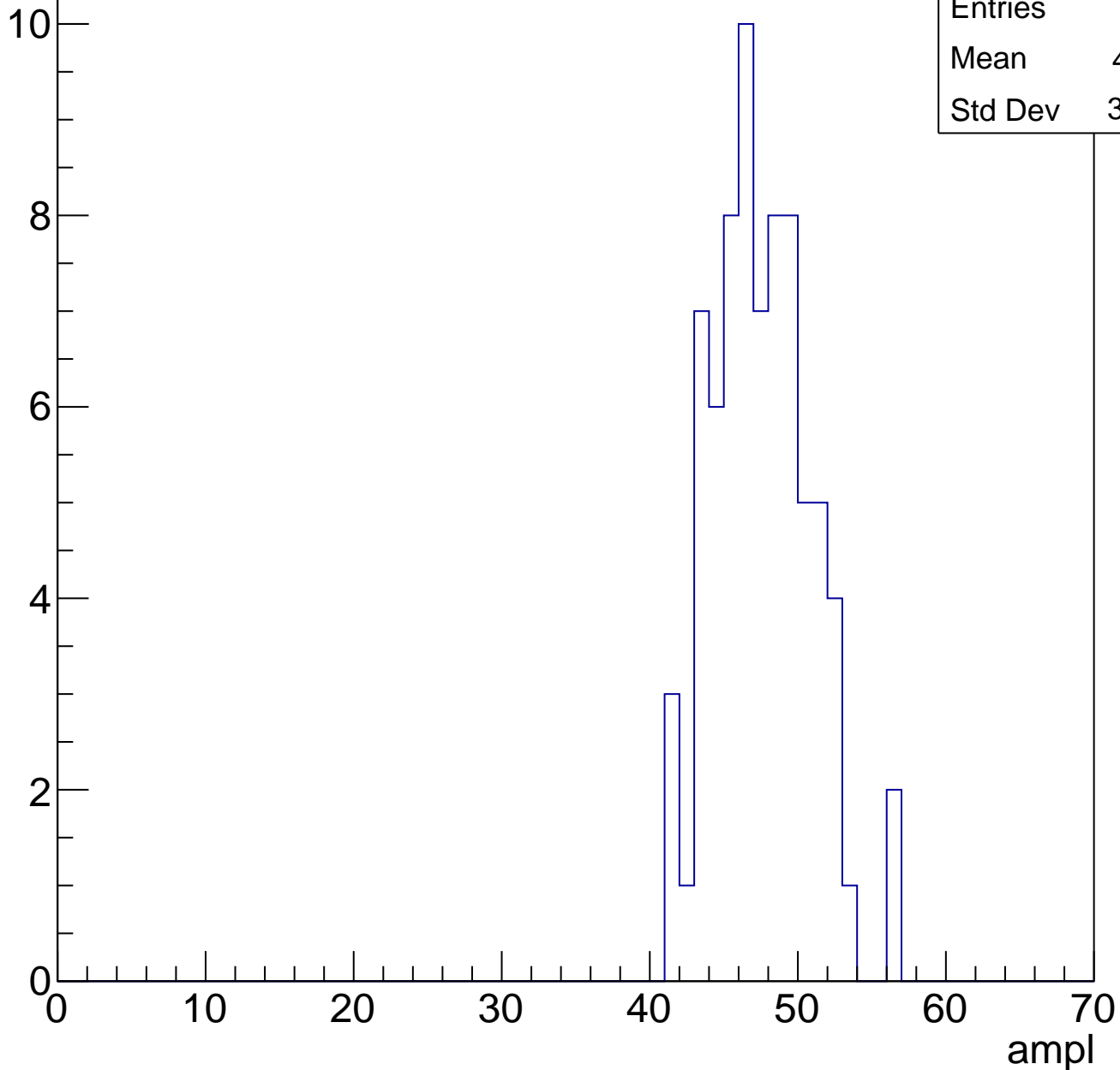


# B1L101S, U3-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

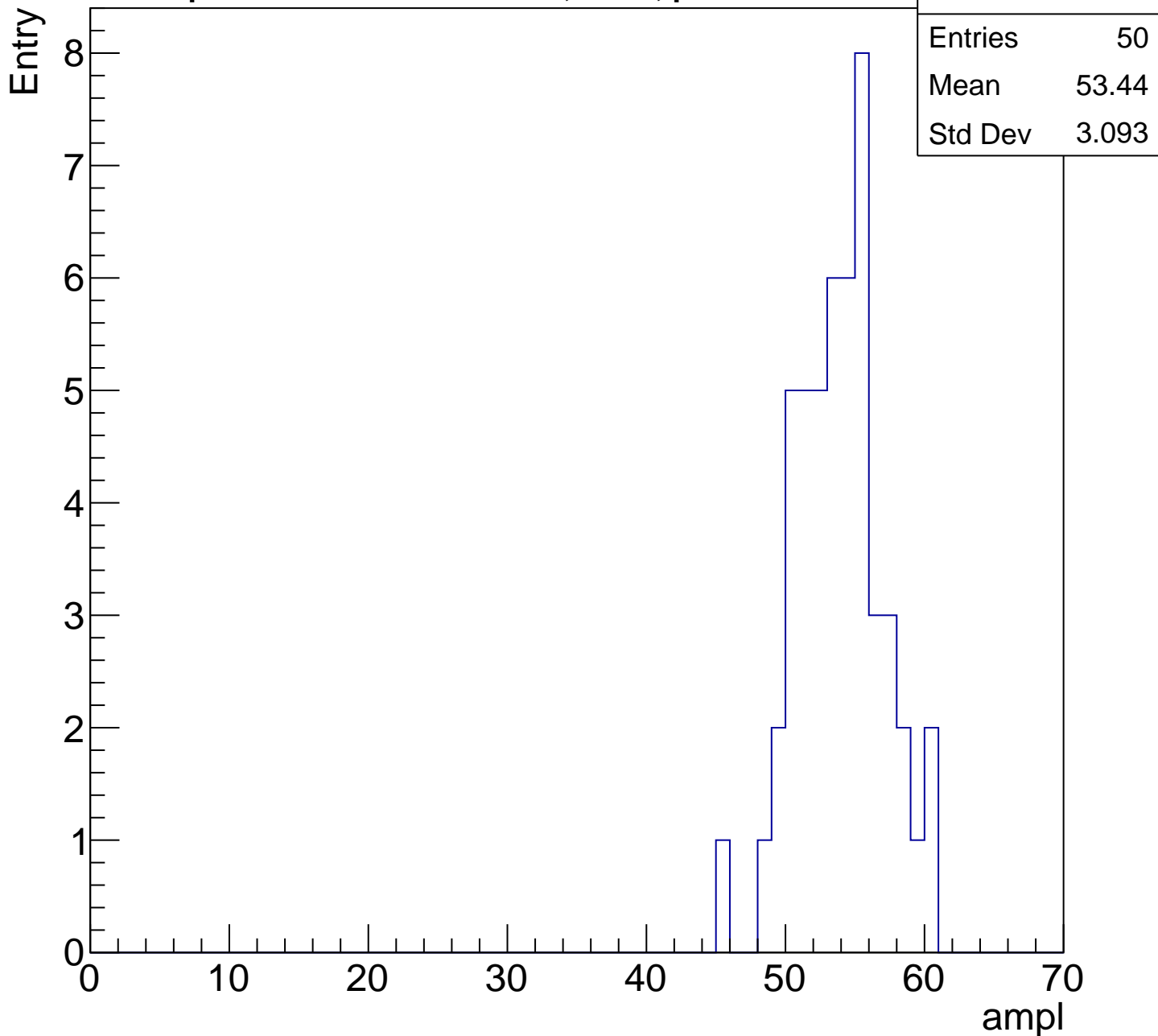
Entries	75
Mean	47.11
Std Dev	3.272

Entry



# B1L101S, U3-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch20, adc5

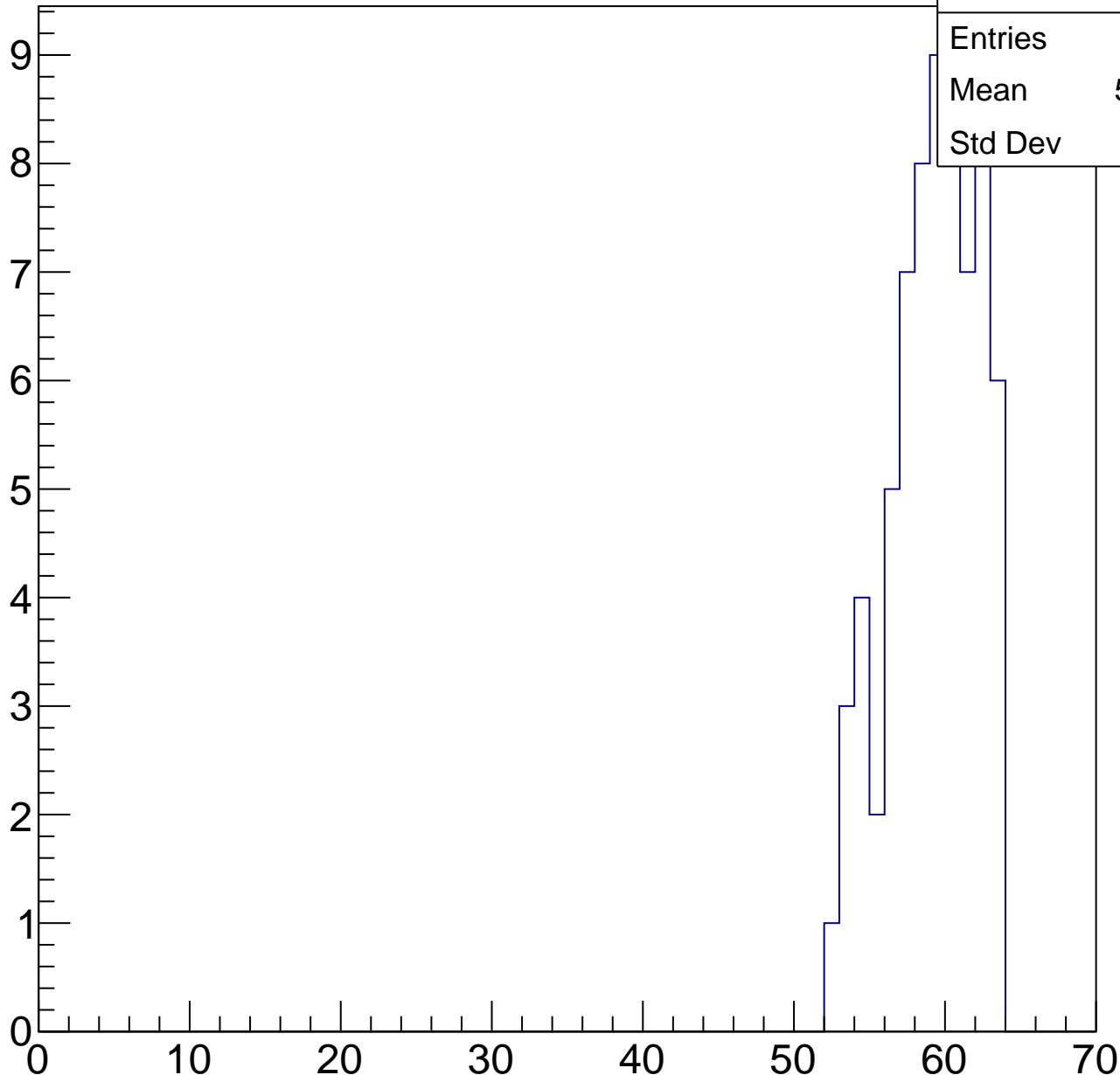
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	68
Mean	58.71
Std Dev	2.89

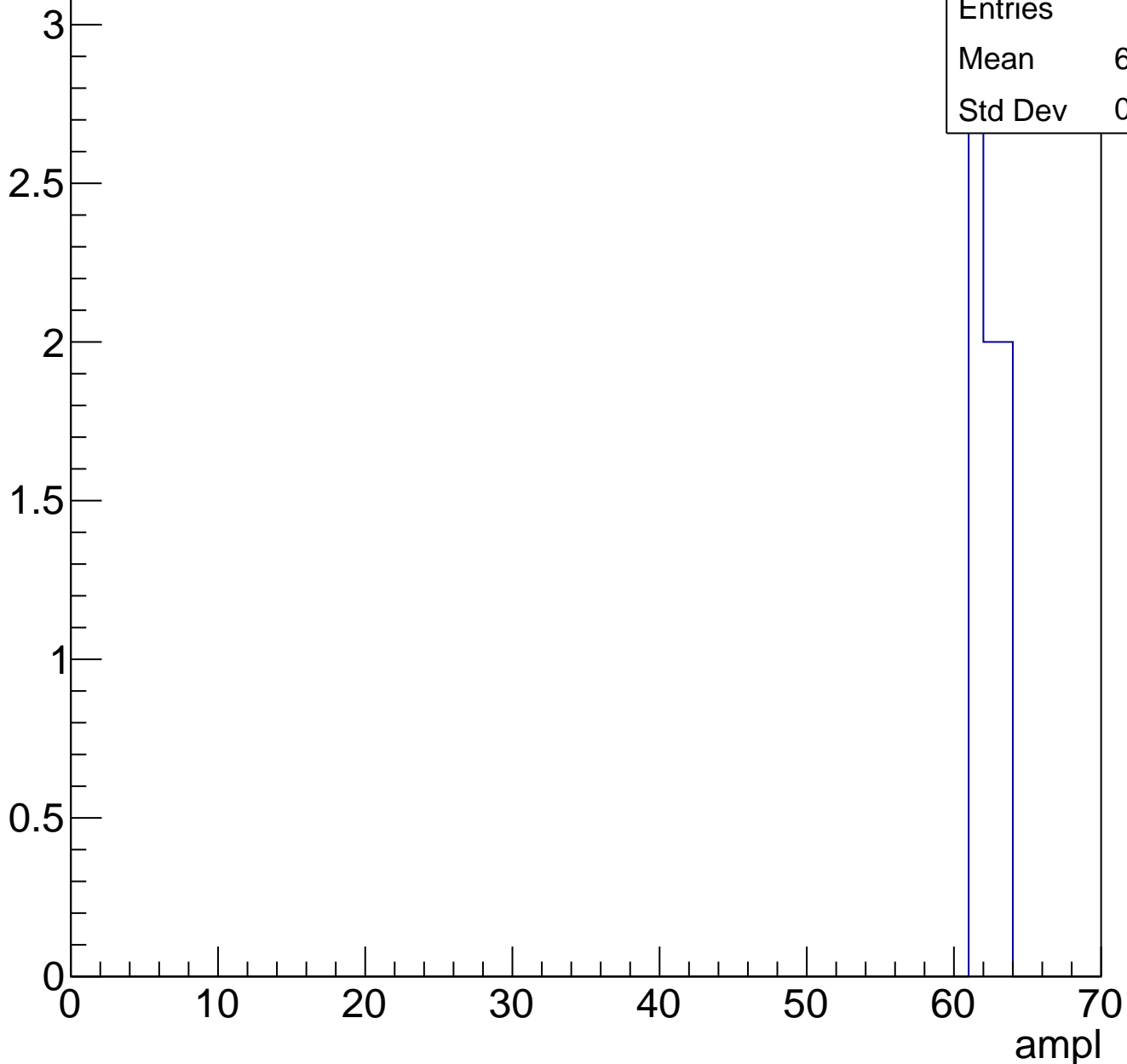
ampl



# B1L101S, U3-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

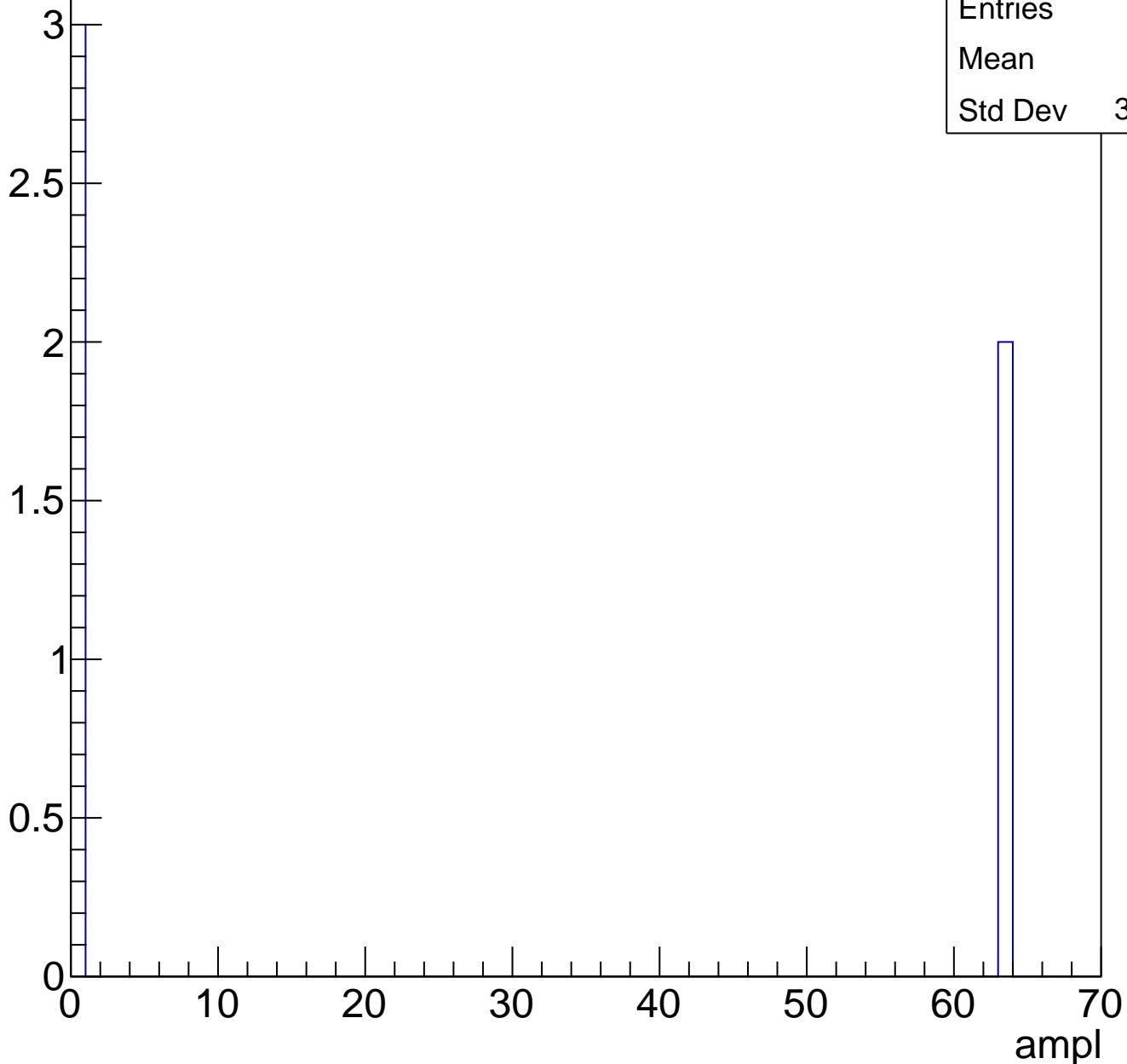




# B1L101S, U3-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	5
Mean	25.2
Std Dev	30.86

# B1L101S, U3-ch21, adc0

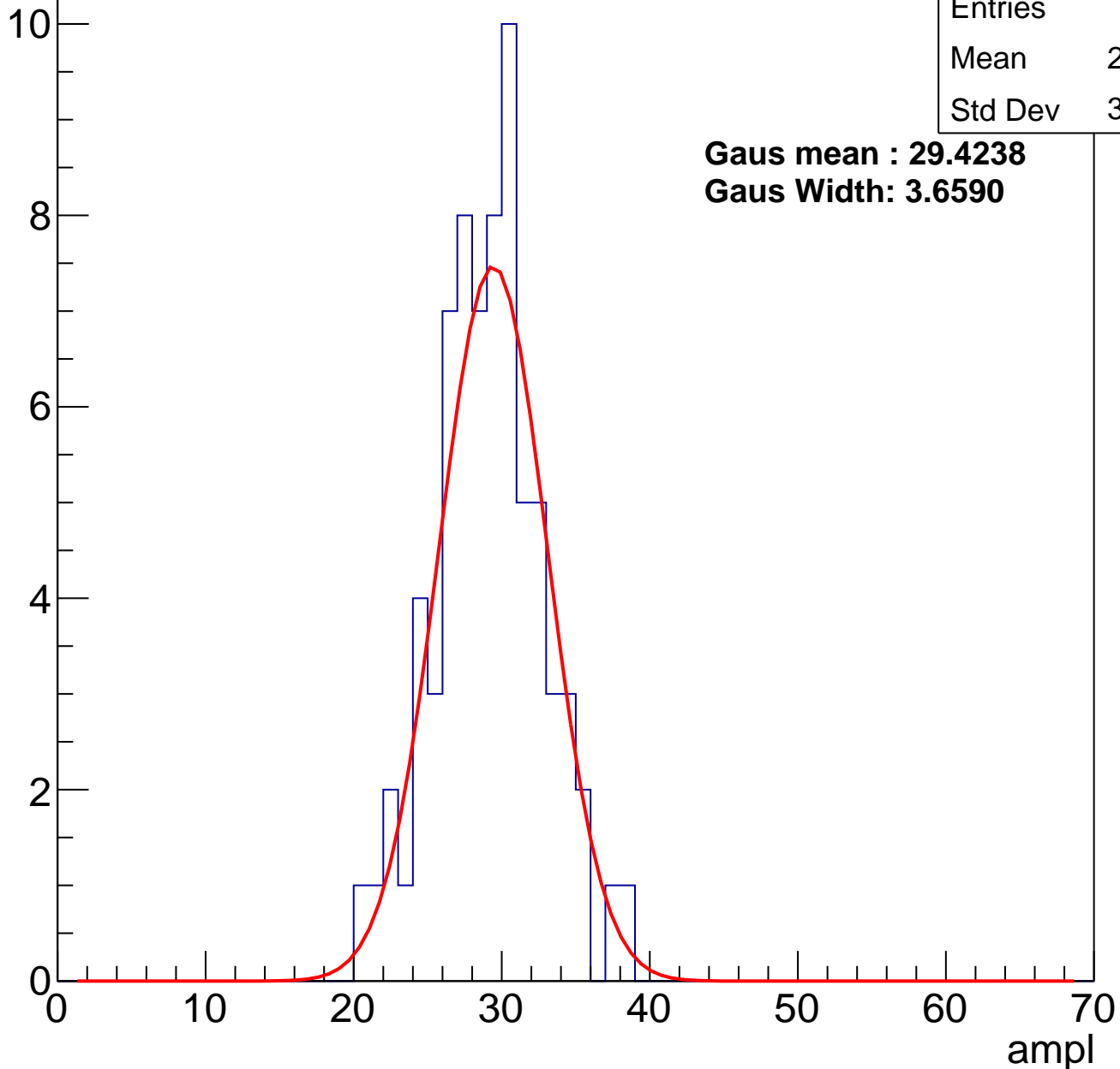
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	72
Mean	28.69
Std Dev	3.608

**Gaus mean : 29.4238**

**Gaus Width: 3.6590**

Entry



# B1L101S, U3-ch21, adc1

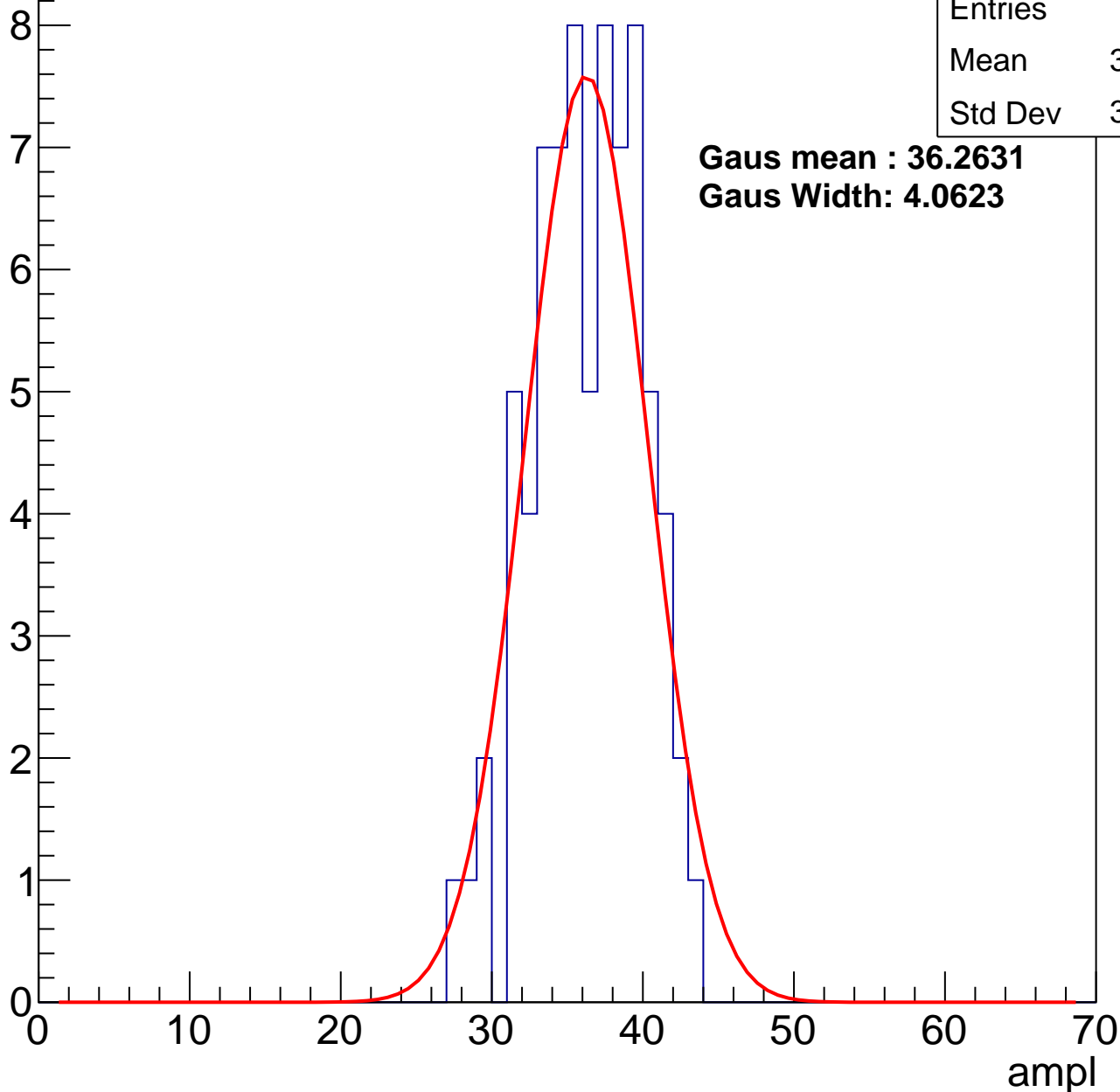
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	35.87
Std Dev	3.538

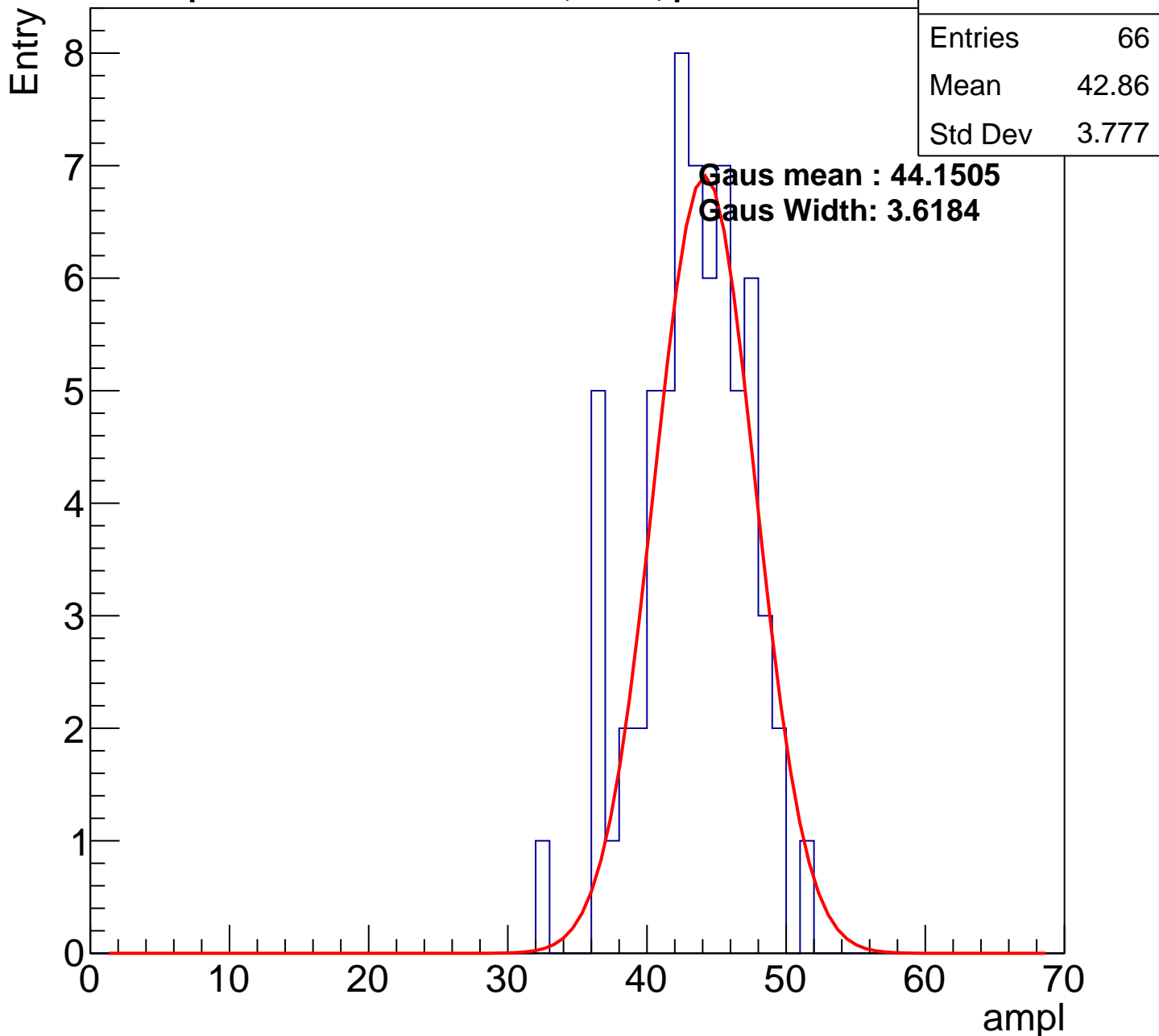
**Gaus mean : 36.2631**

**Gaus Width: 4.0623**



# B1L101S, U3-ch21, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

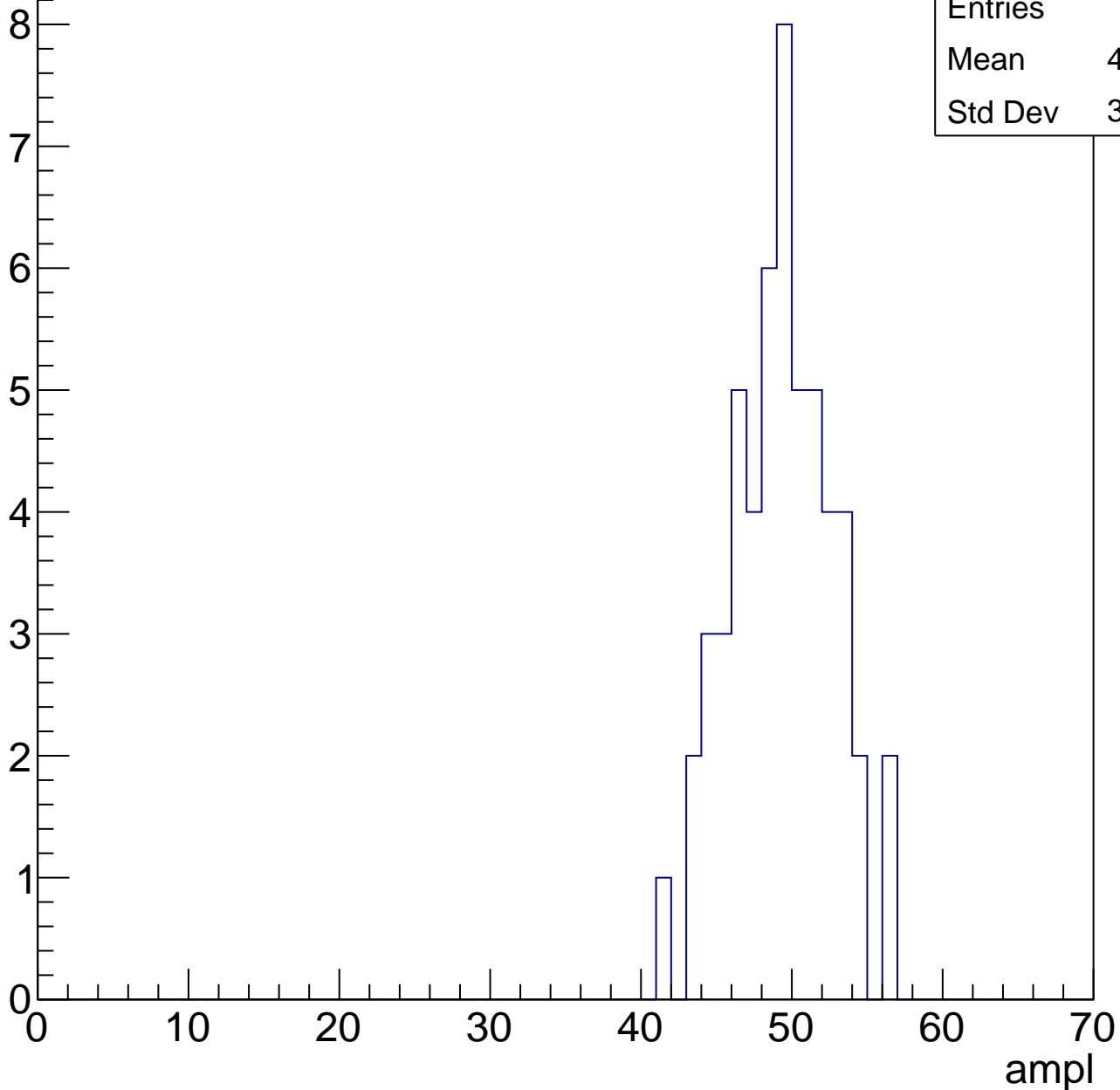


# B1L101S, U3-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

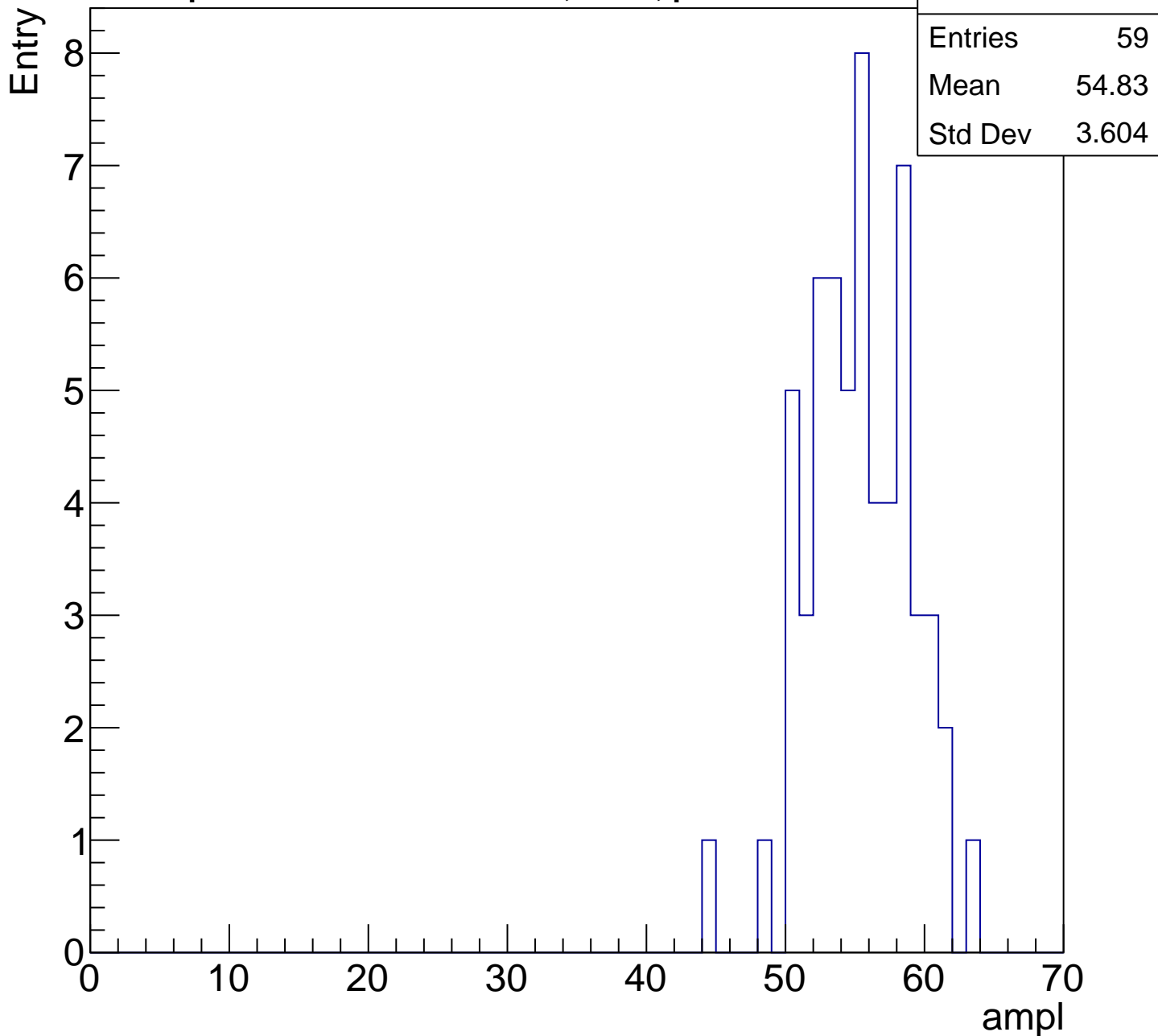
Entry

Entries	54
Mean	48.83
Std Dev	3.326



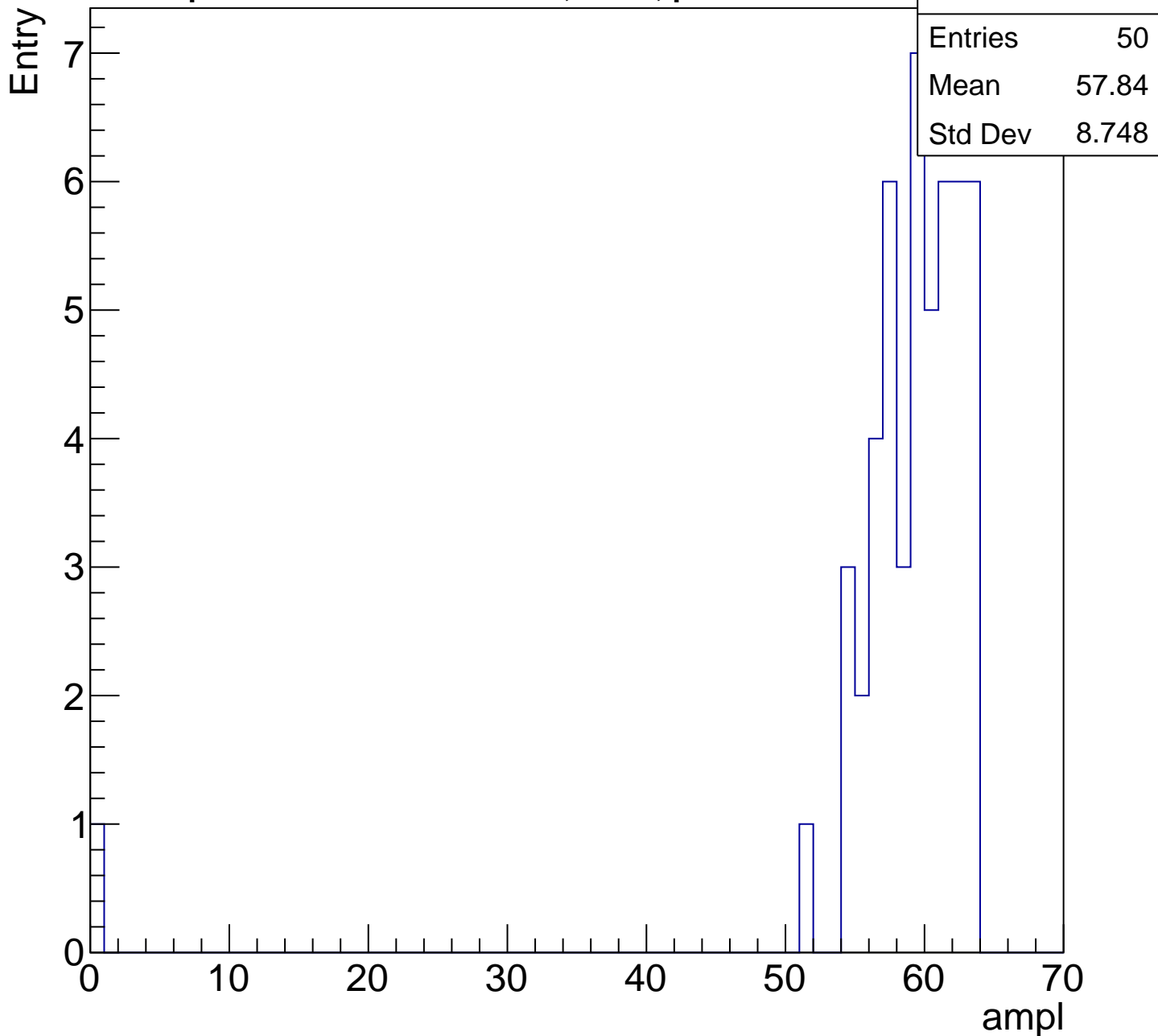
# B1L101S, U3-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch21, adc5

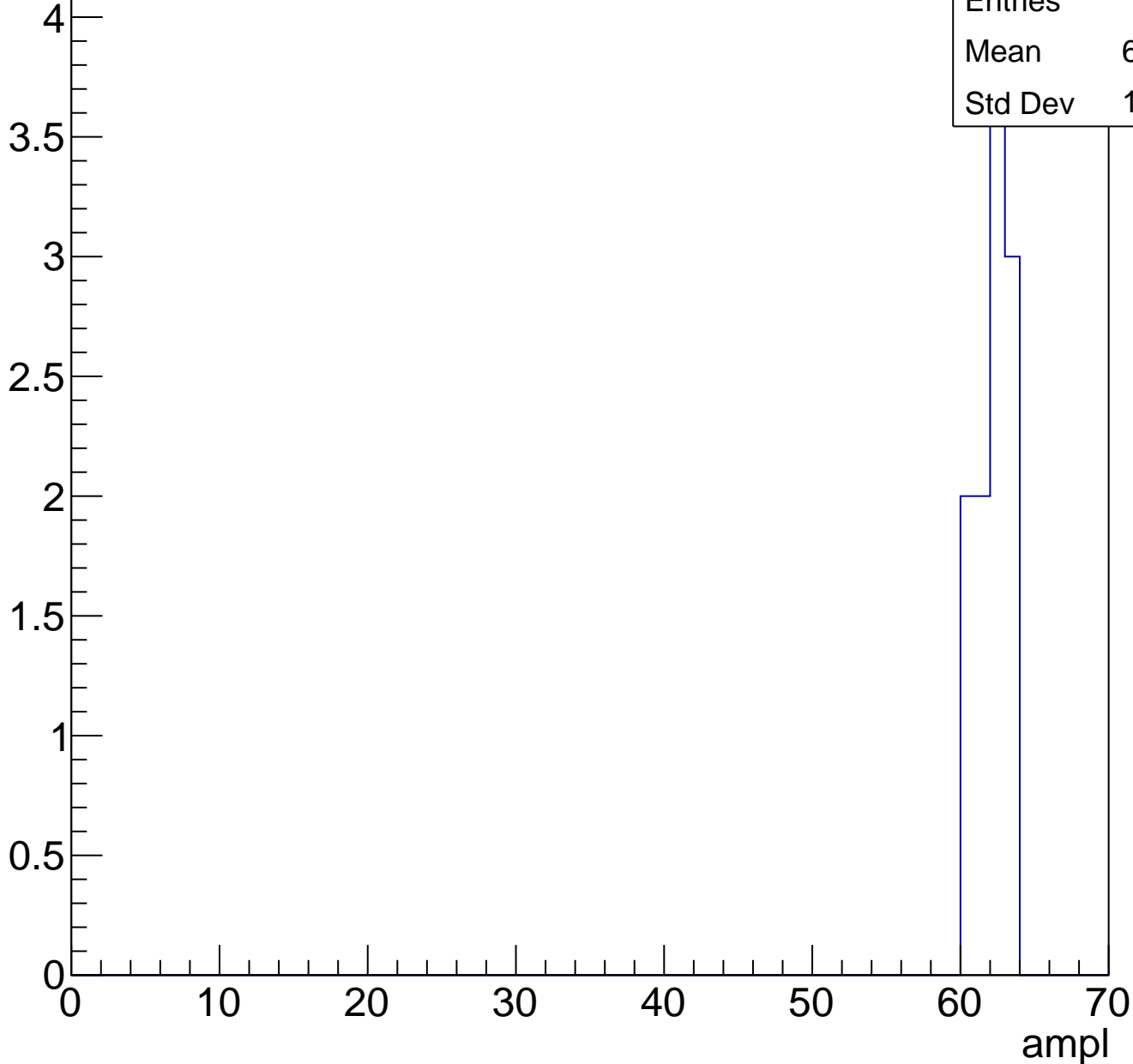
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U3-ch22, adc0

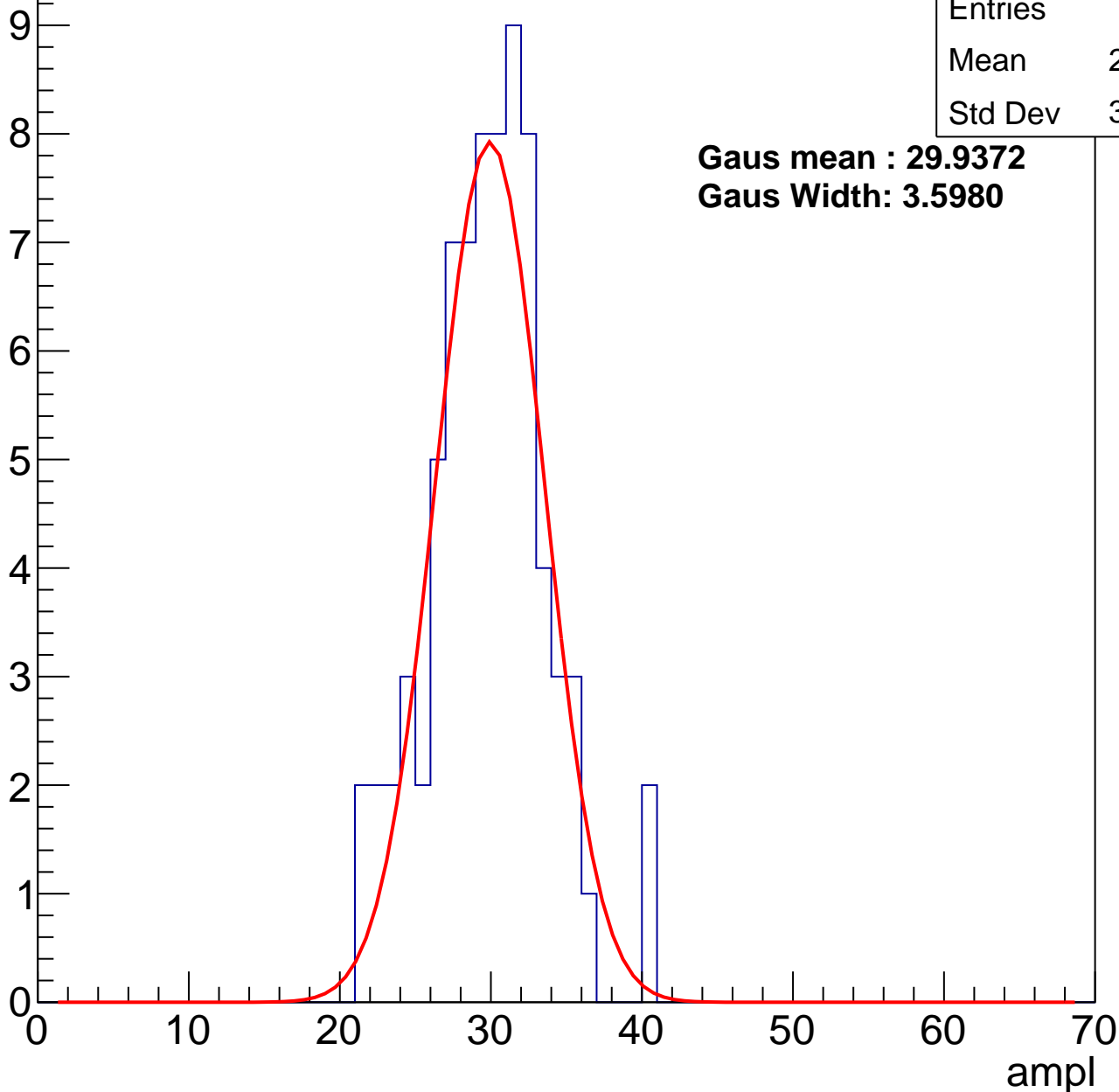
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	29.36
Std Dev	3.855

**Gaus mean : 29.9372**

**Gaus Width: 3.5980**



# B1L101S, U3-ch22, adc1

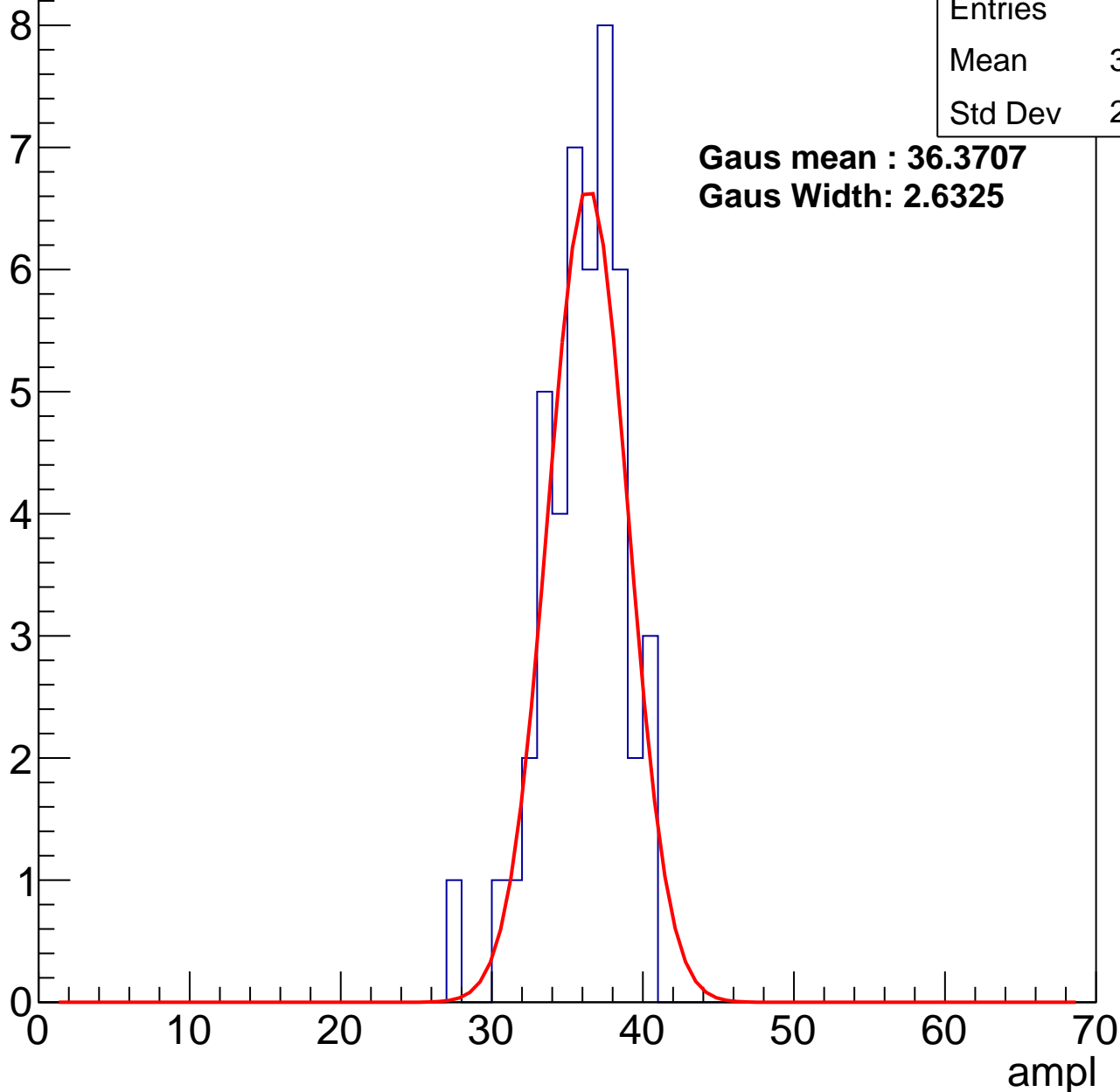
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	35.57
Std Dev	2.684

**Gaus mean : 36.3707**

**Gaus Width: 2.6325**



# B1L101S, U3-ch22, adc2

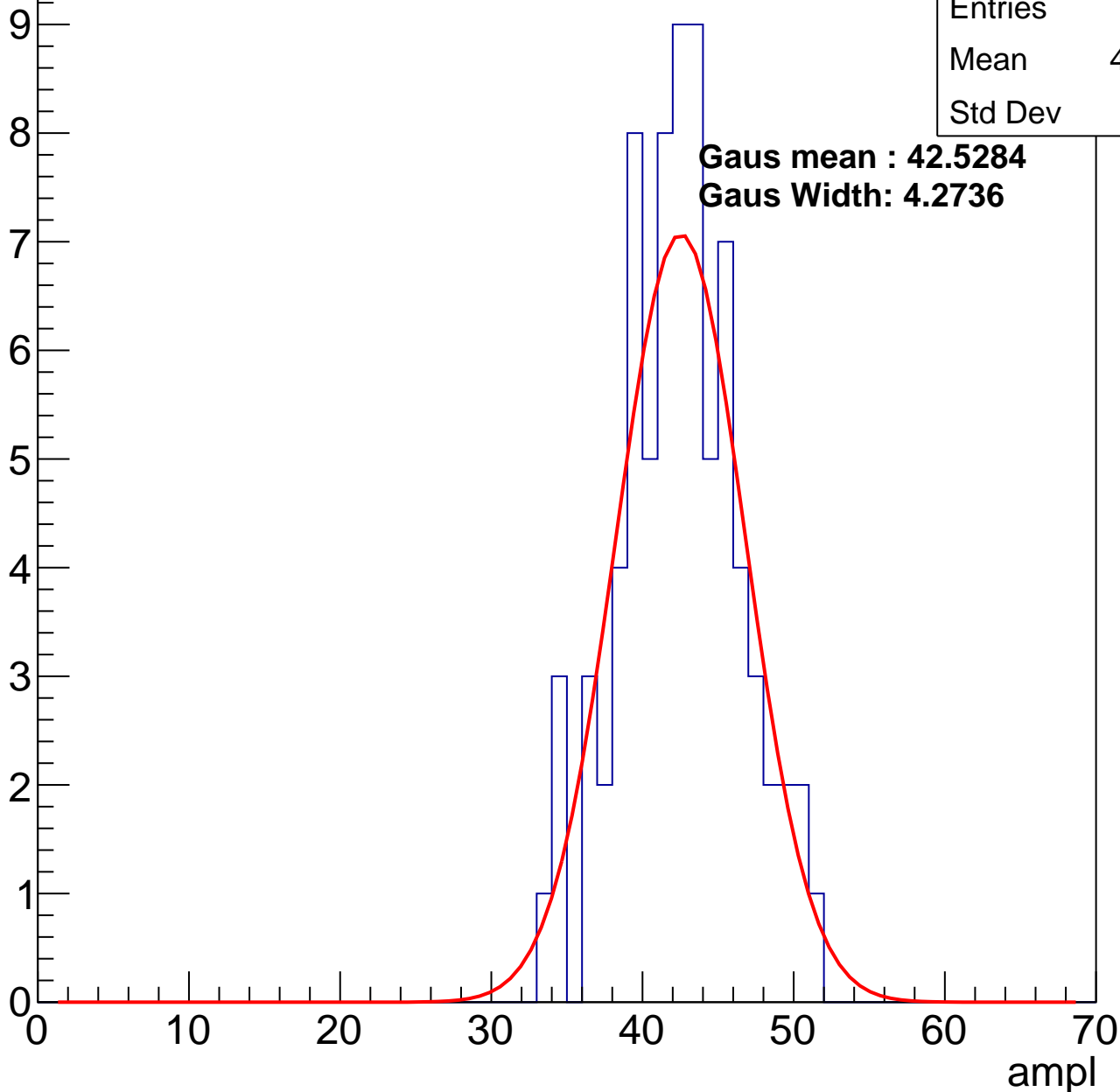
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	42.04
Std Dev	3.93

**Gaus mean : 42.5284**

**Gaus Width: 4.2736**

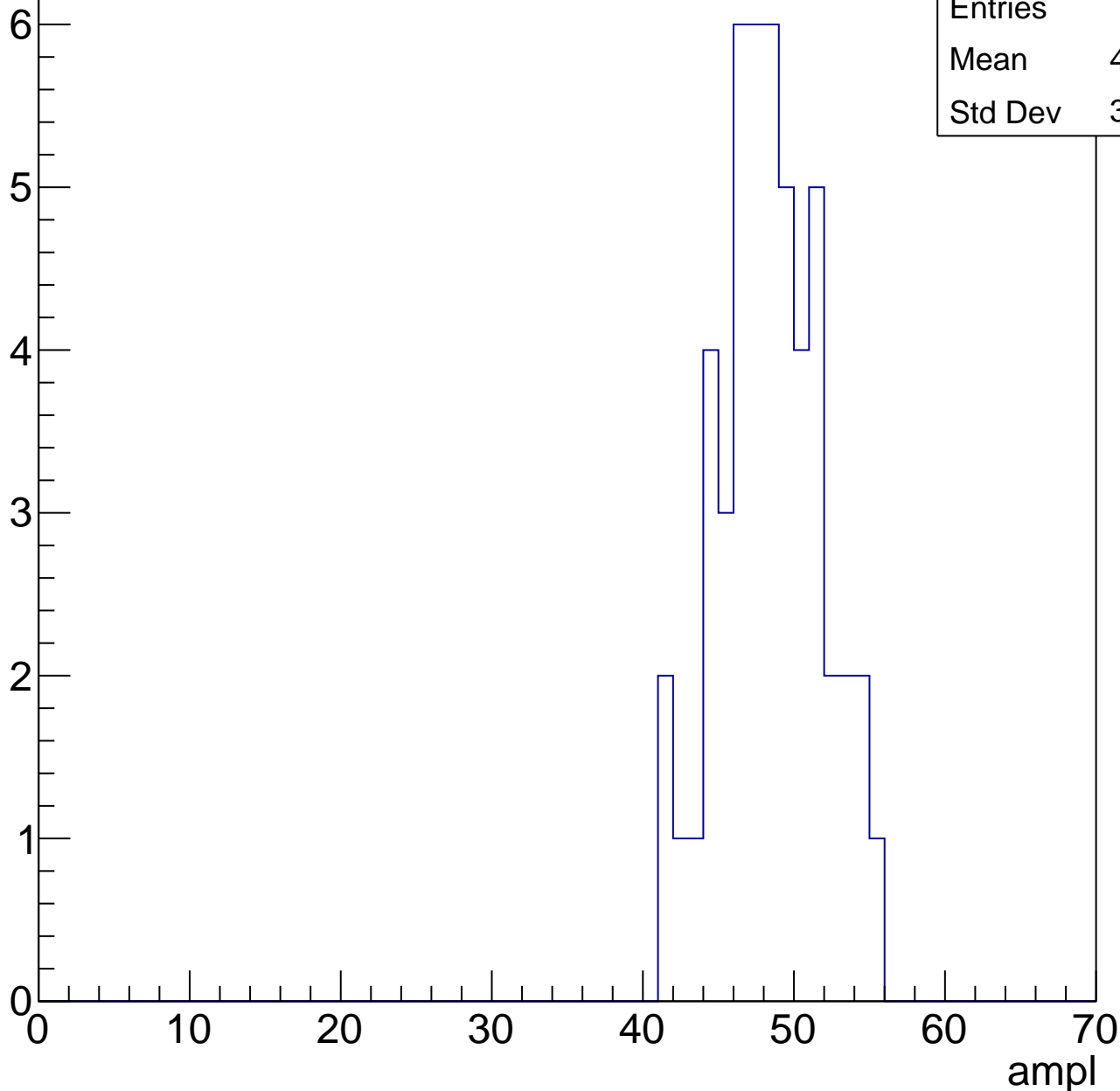


# B1L101S, U3-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	47.94
Std Dev	3.313

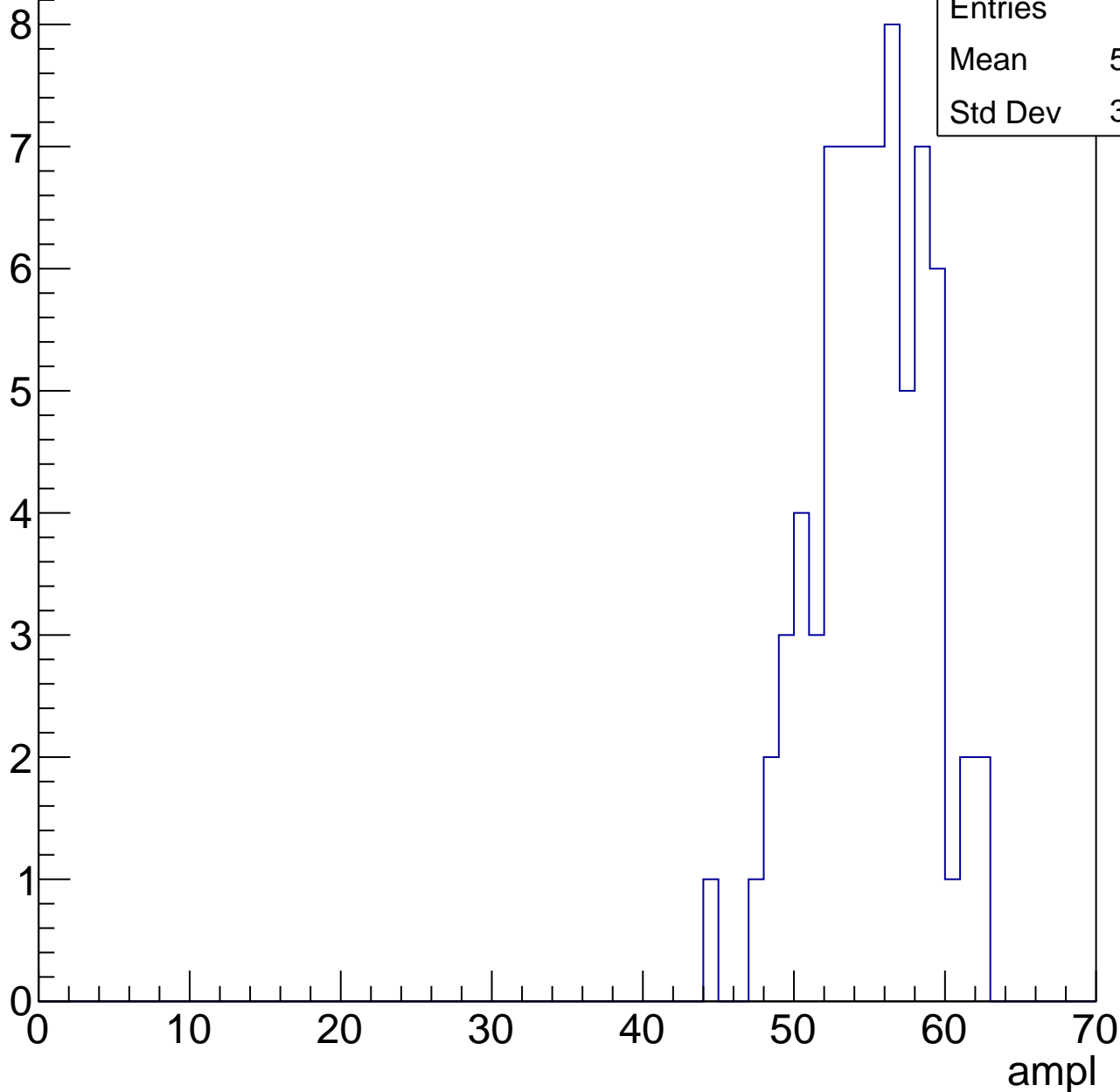


# B1L101S, U3-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	54.58
Std Dev	3.712



# B1L101S, U3-ch22, adc5

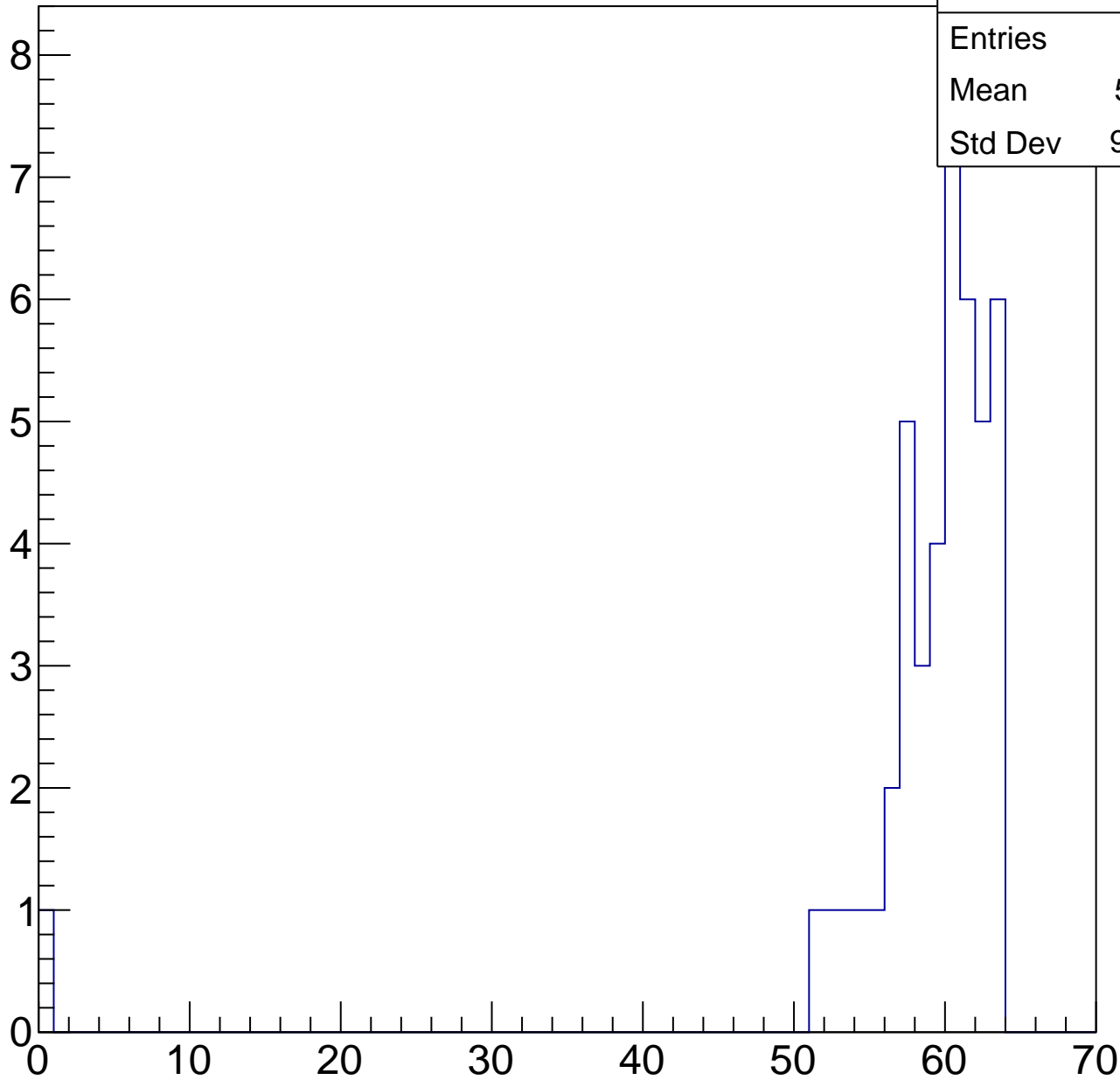
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	45
Mean	57.91
Std Dev	9.228

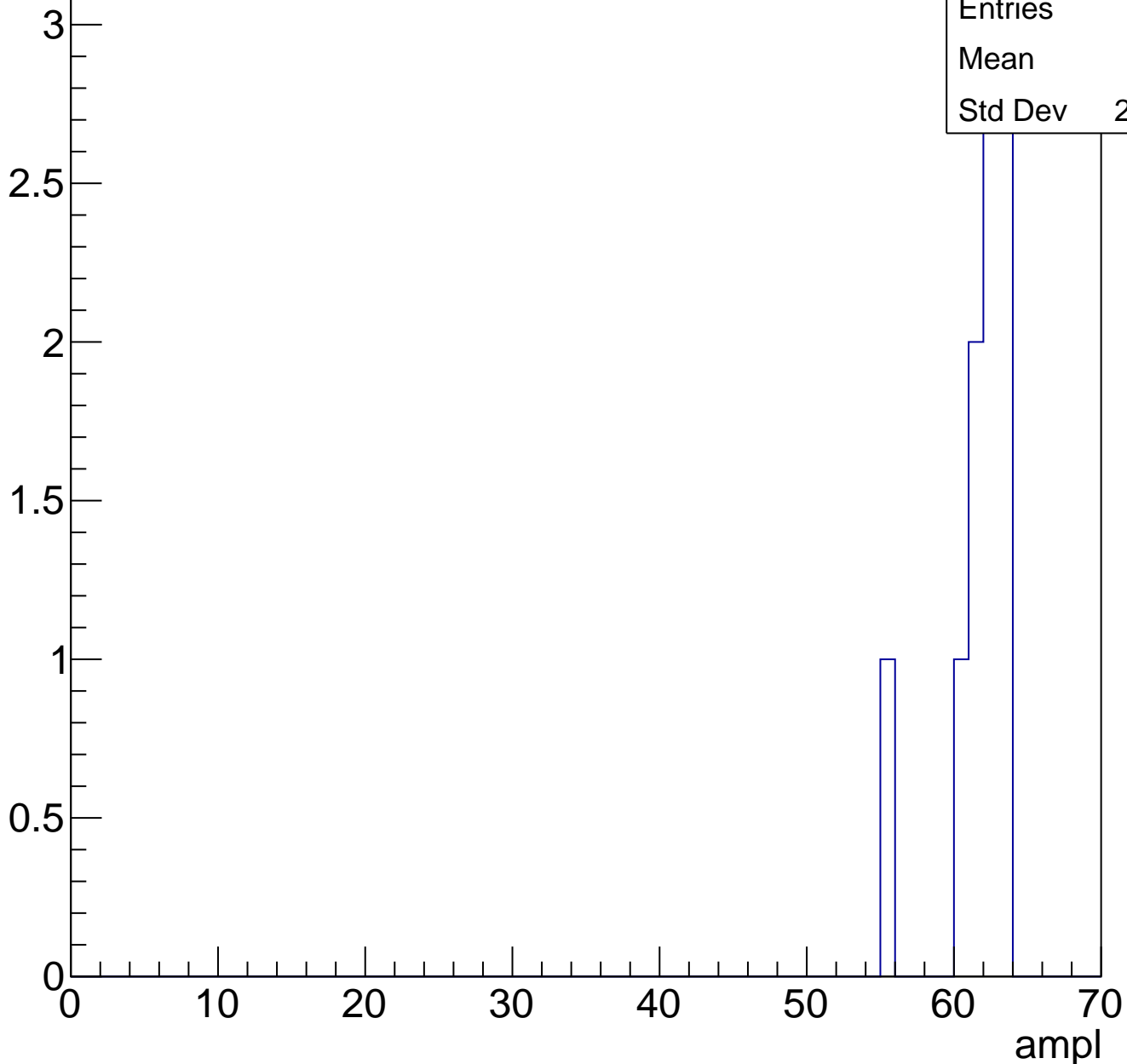
ampl



# B1L101S, U3-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

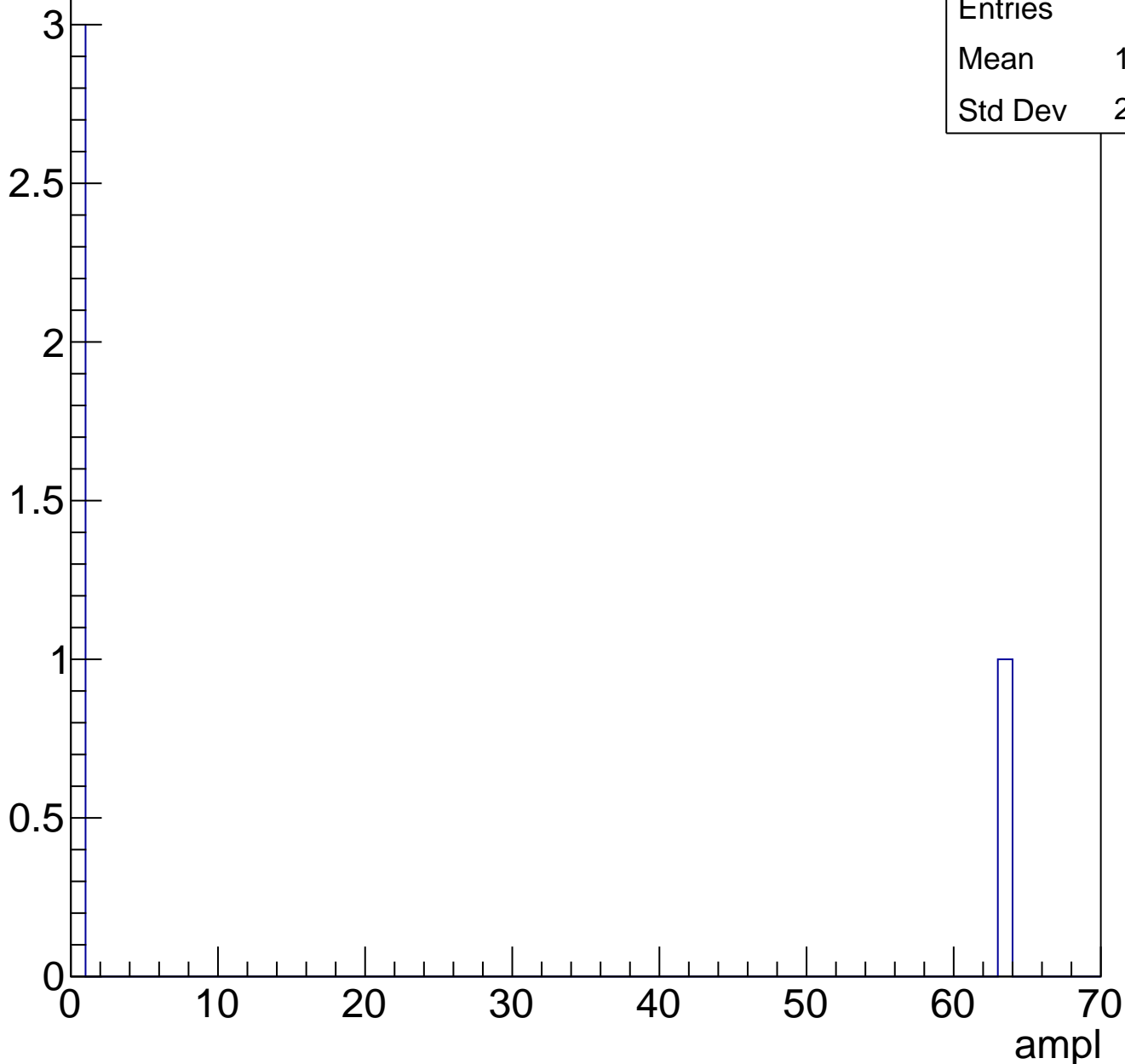




# B1L101S, U3-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch23, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	69
Mean	30.13
Std Dev	5.013

**Gaus mean : 31.3768**

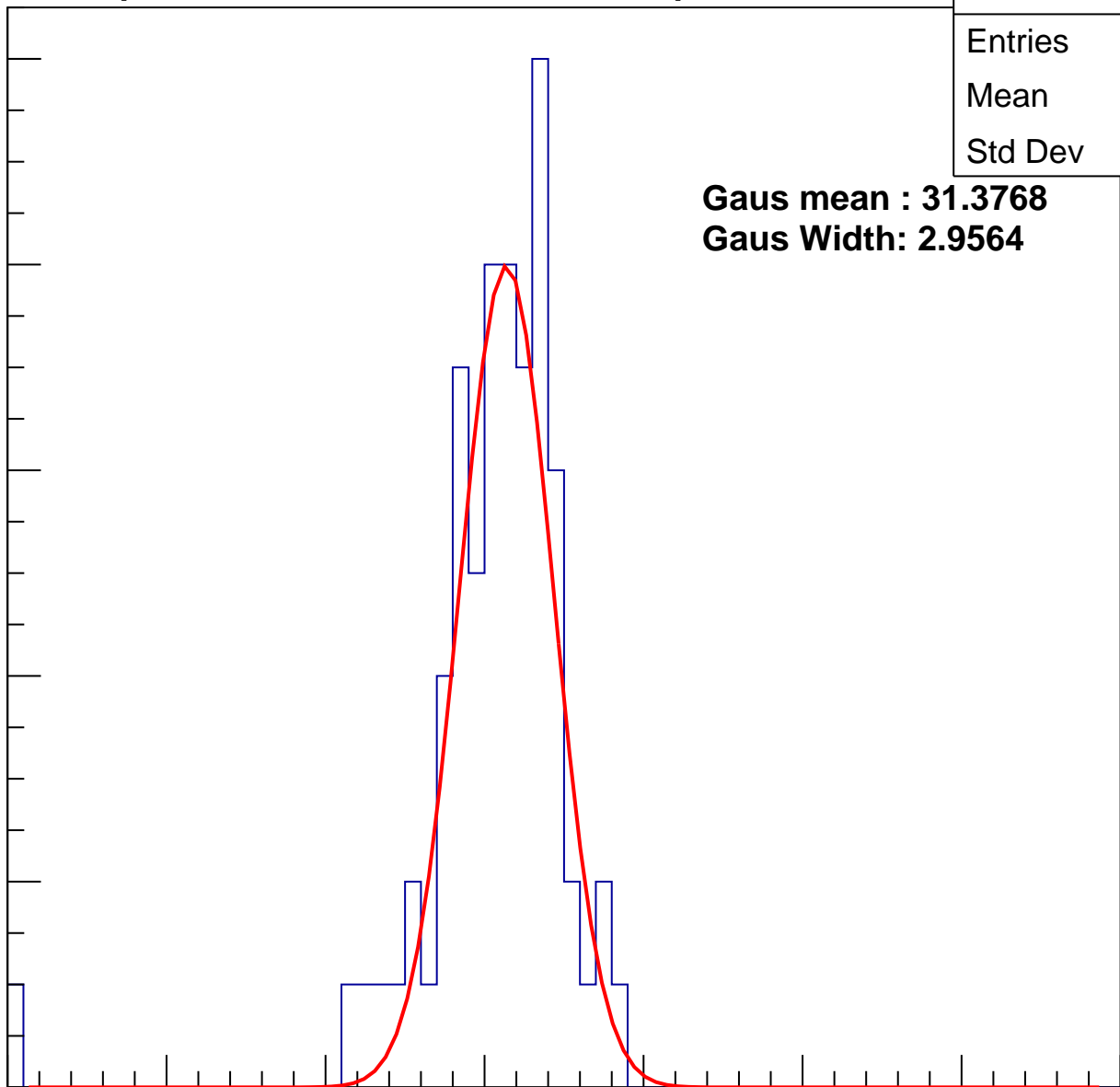
**Gaus Width: 2.9564**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U3-ch23, adc1

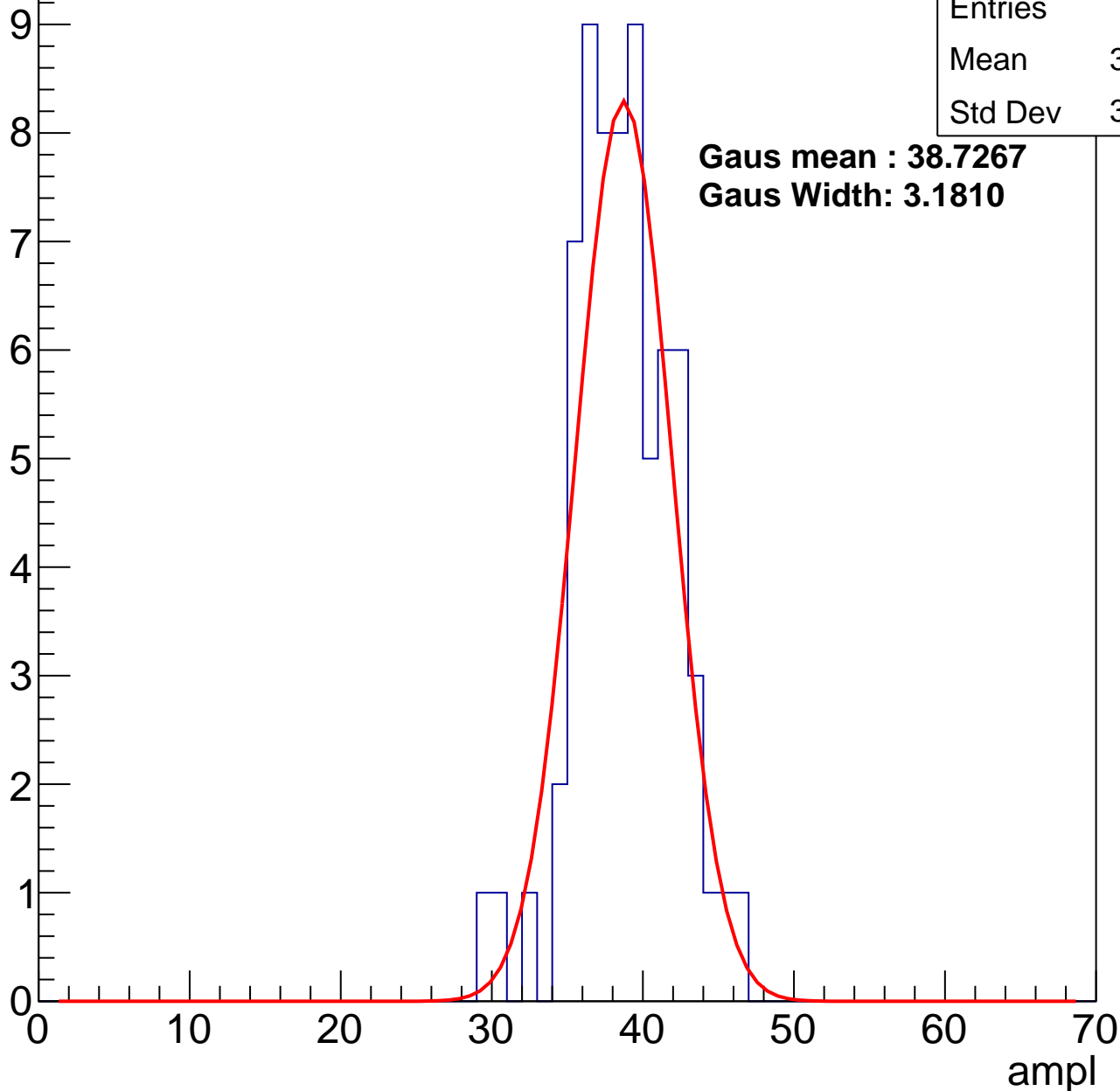
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	38.28
Std Dev	3.225

**Gaus mean : 38.7267**

**Gaus Width: 3.1810**



# B1L101S, U3-ch23, adc2

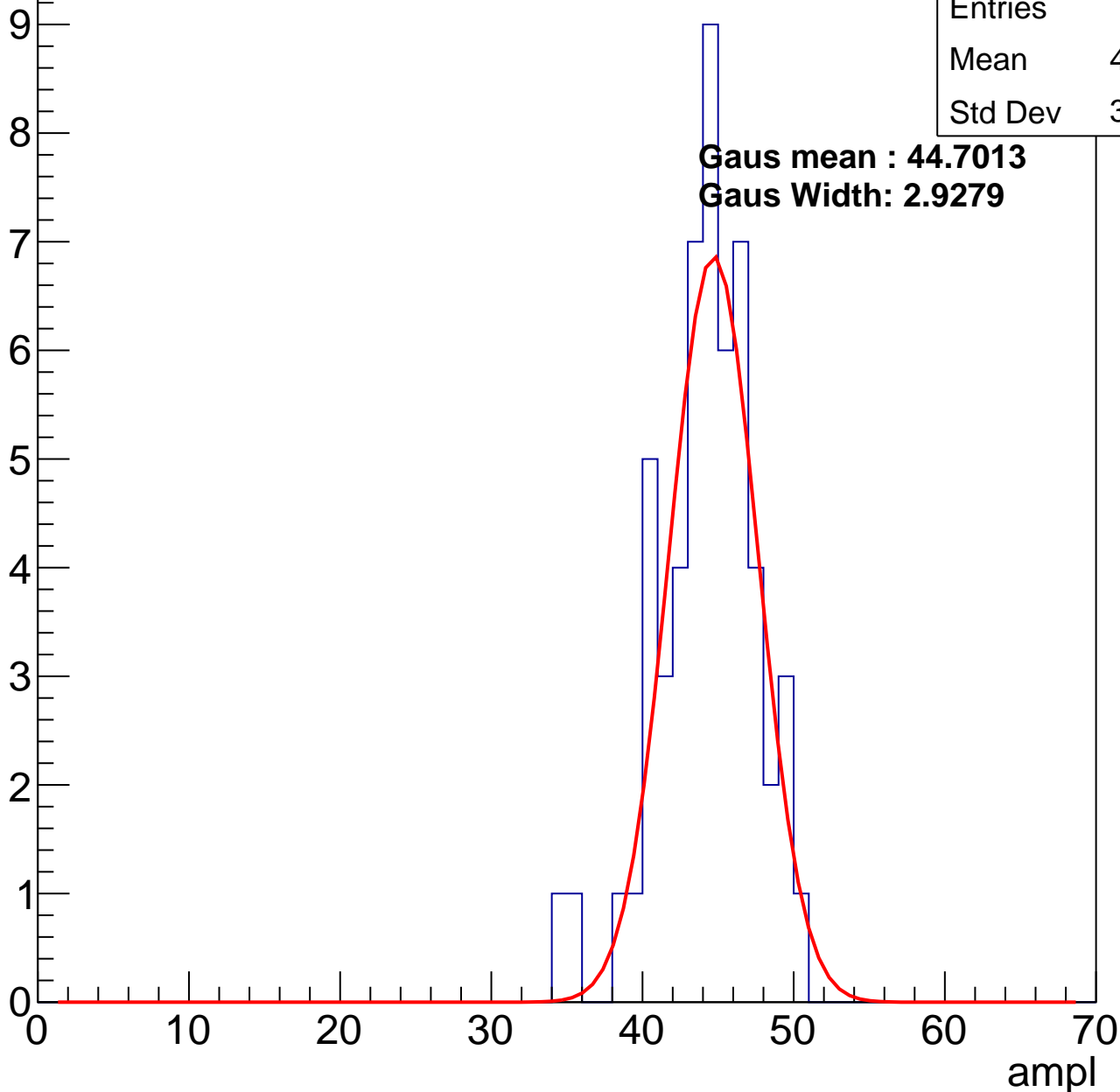
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	43.76
Std Dev	3.253

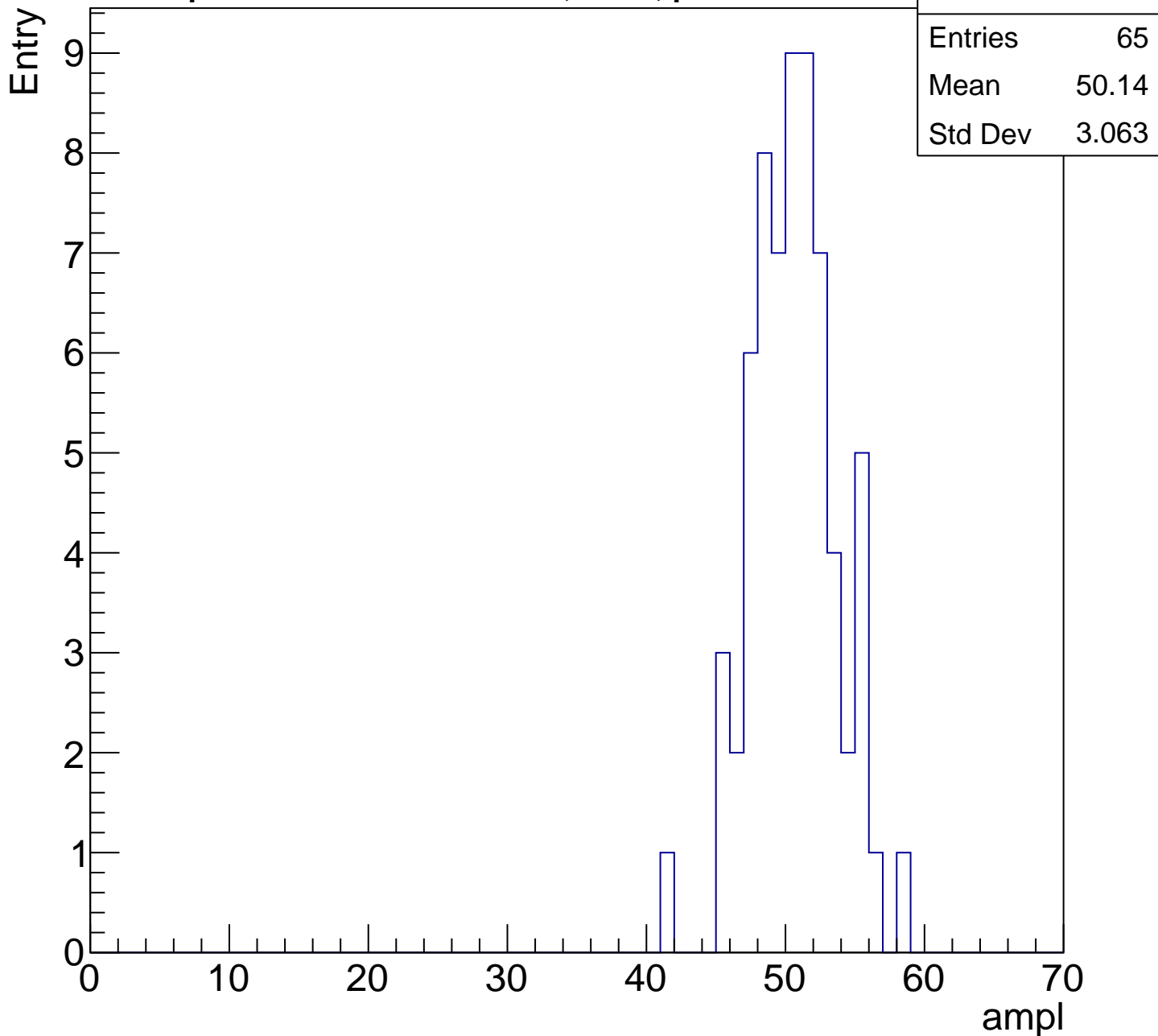
**Gaus mean : 44.7013**

**Gaus Width: 2.9279**



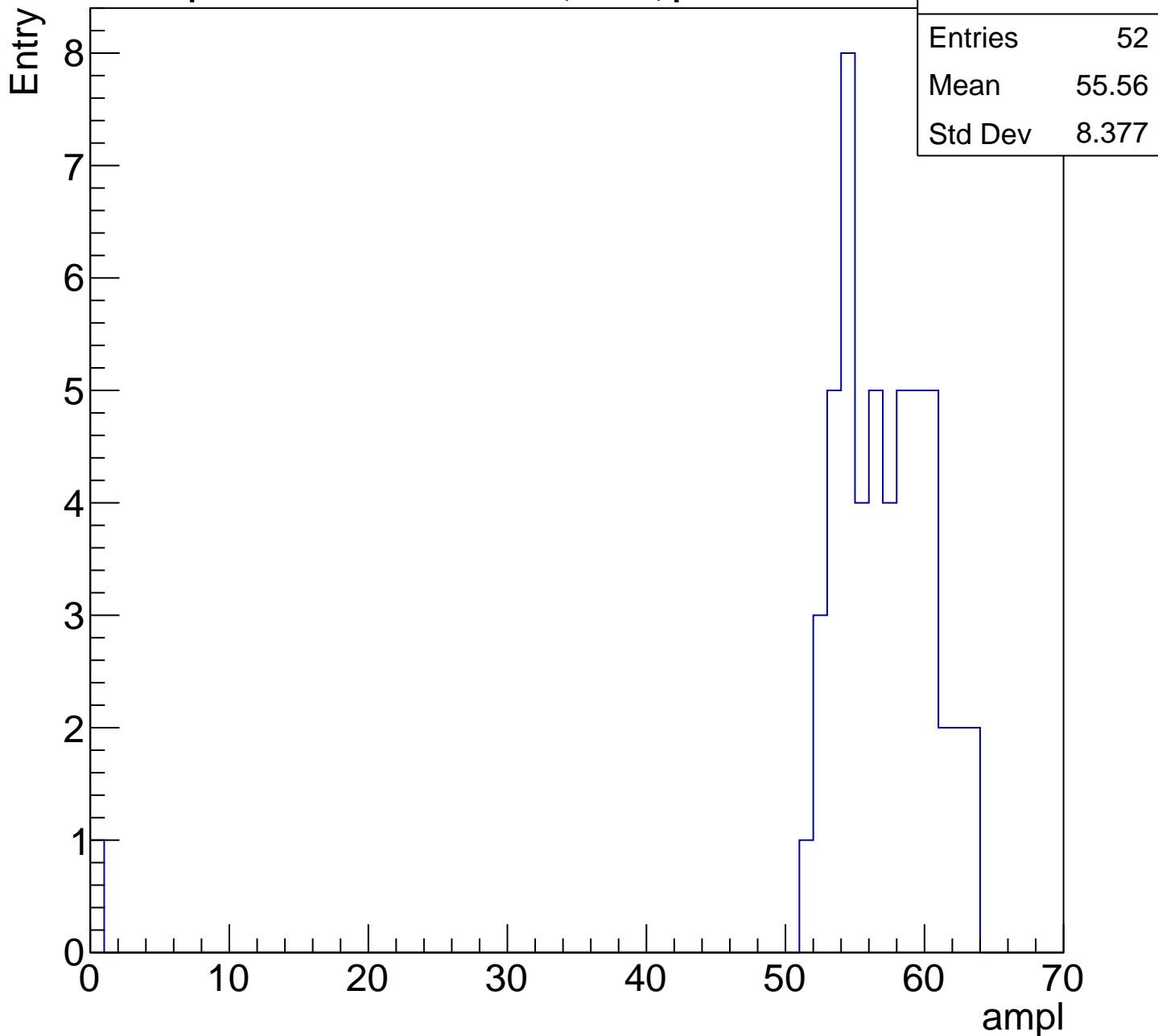
# B1L101S, U3-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

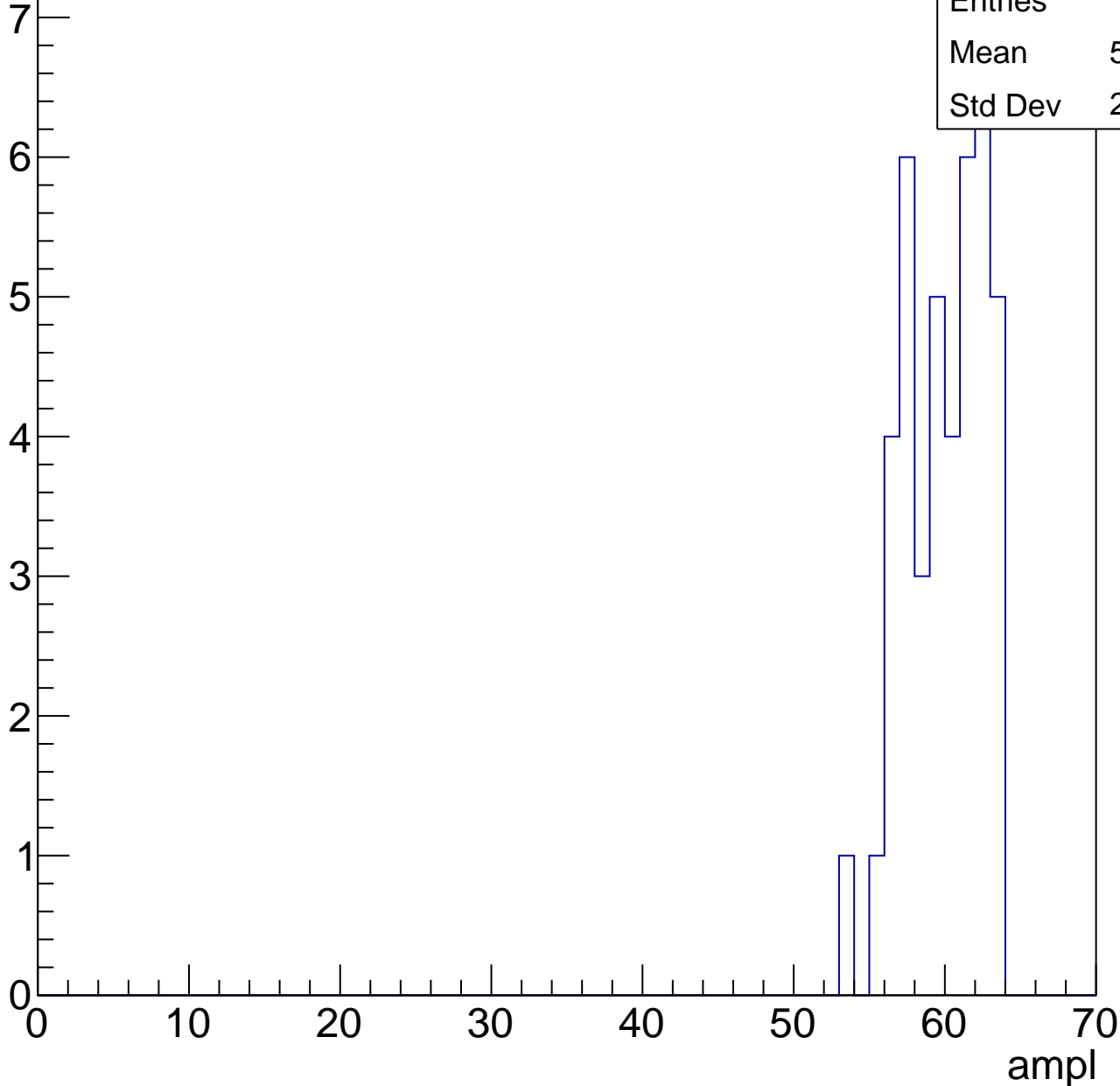


# B1L101S, U3-ch23, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

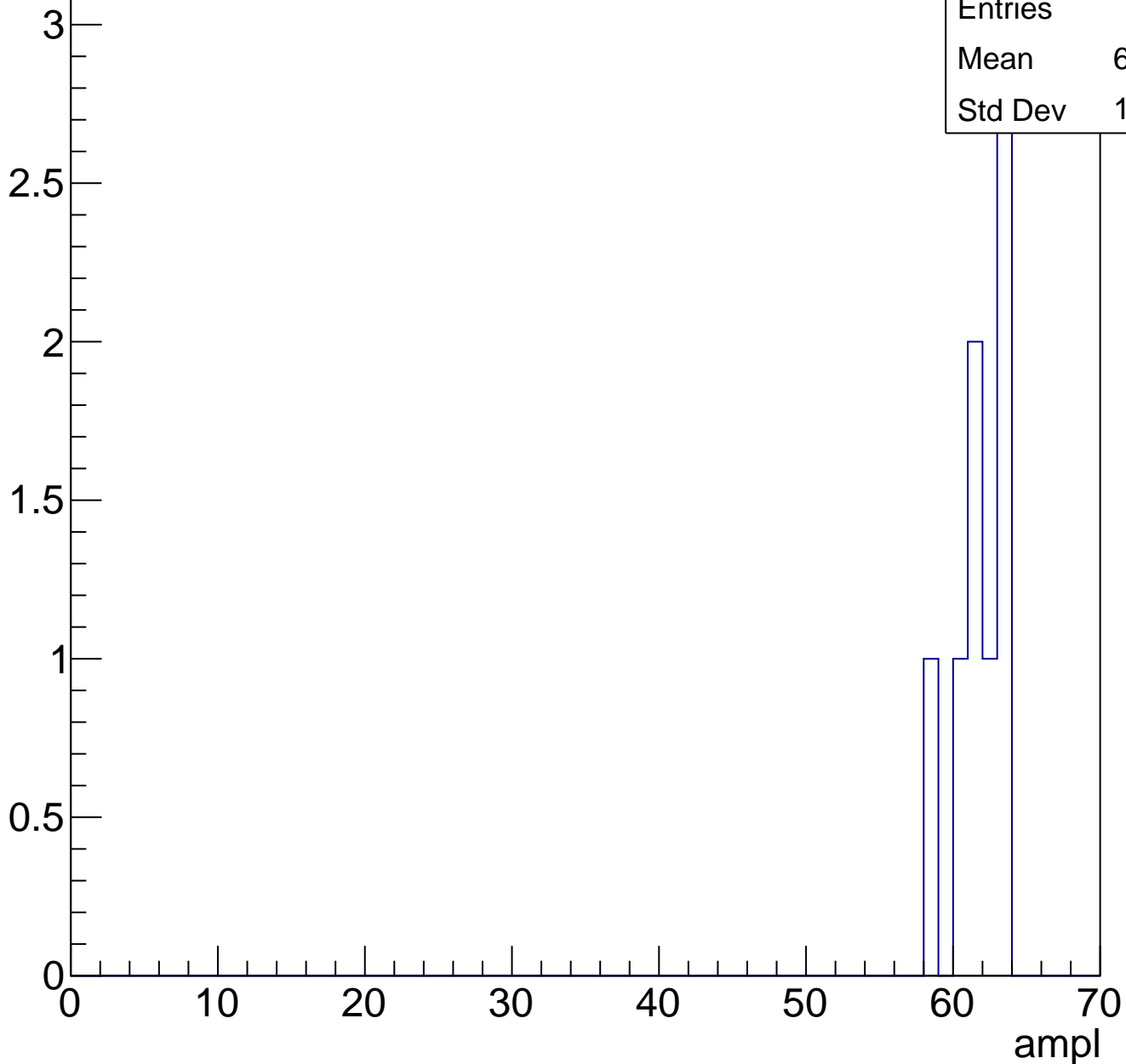
Entries	42
Mean	59.48
Std Dev	2.566



# B1L101S, U3-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U3-ch24, adc0

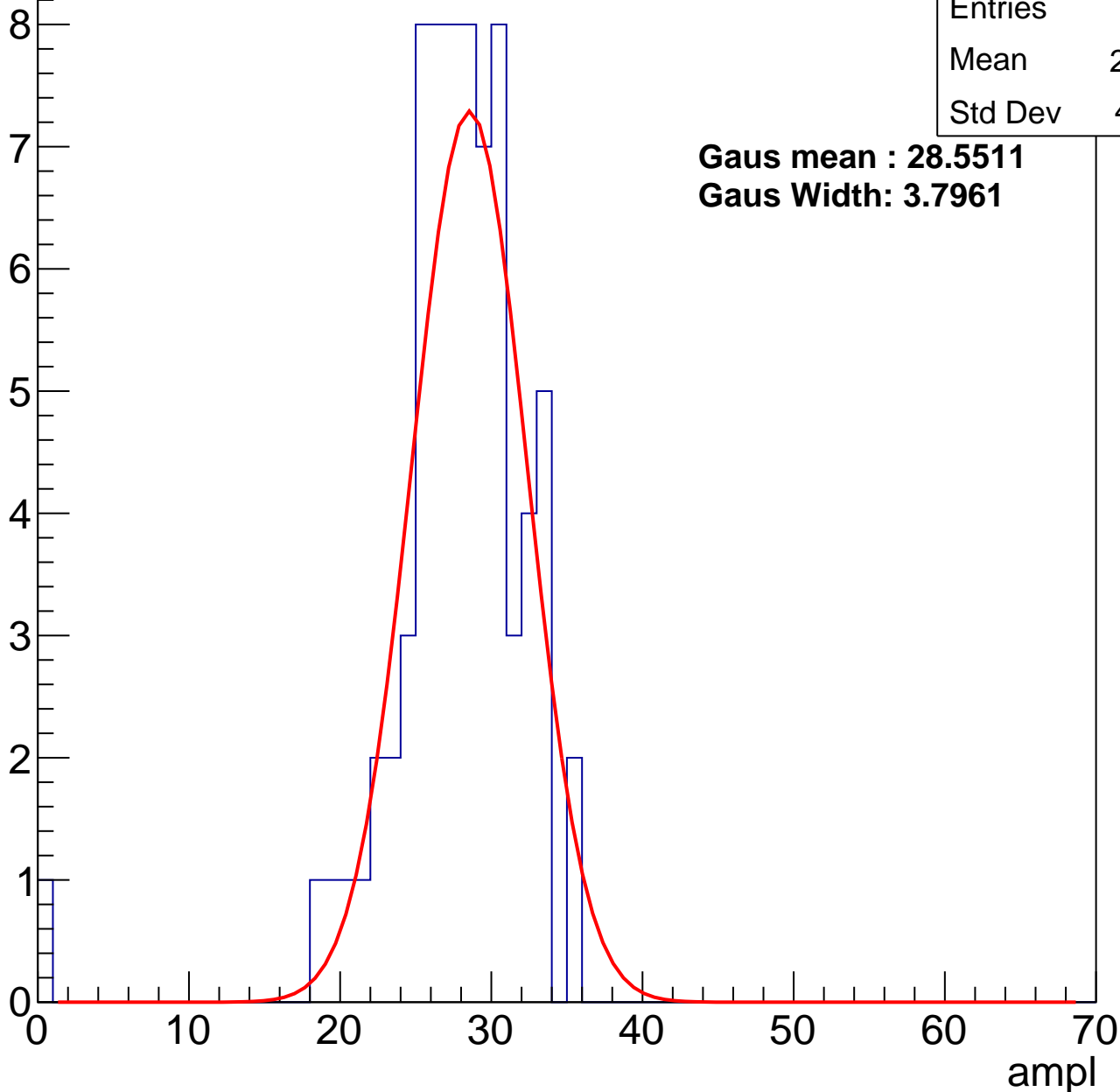
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	27.22
Std Dev	4.781

**Gaus mean : 28.5511**

**Gaus Width: 3.7961**



# B1L101S, U3-ch24, adc1

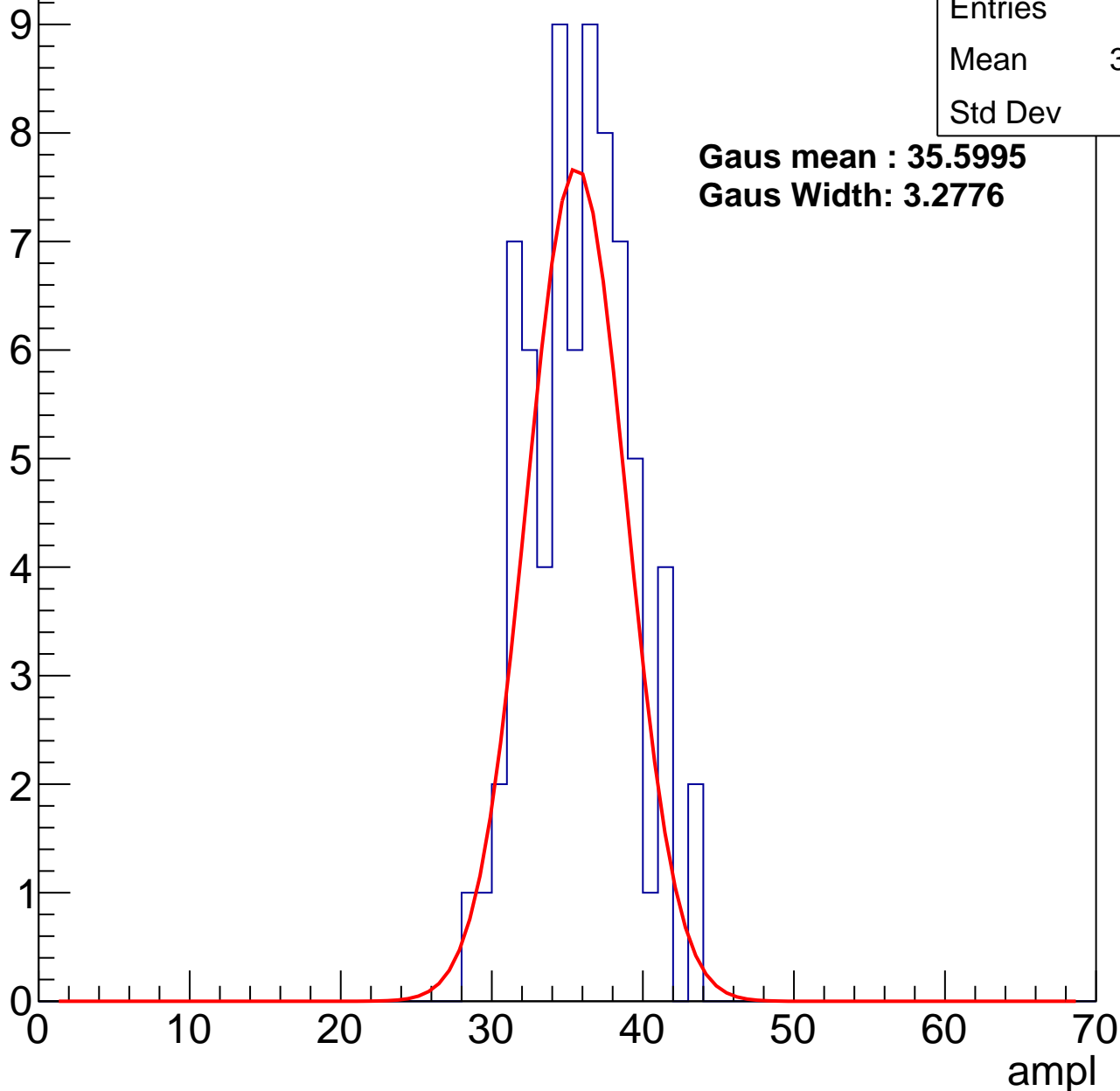
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	35.35
Std Dev	3.33

**Gaus mean : 35.5995**

**Gaus Width: 3.2776**



# B1L101S, U3-ch24, adc2

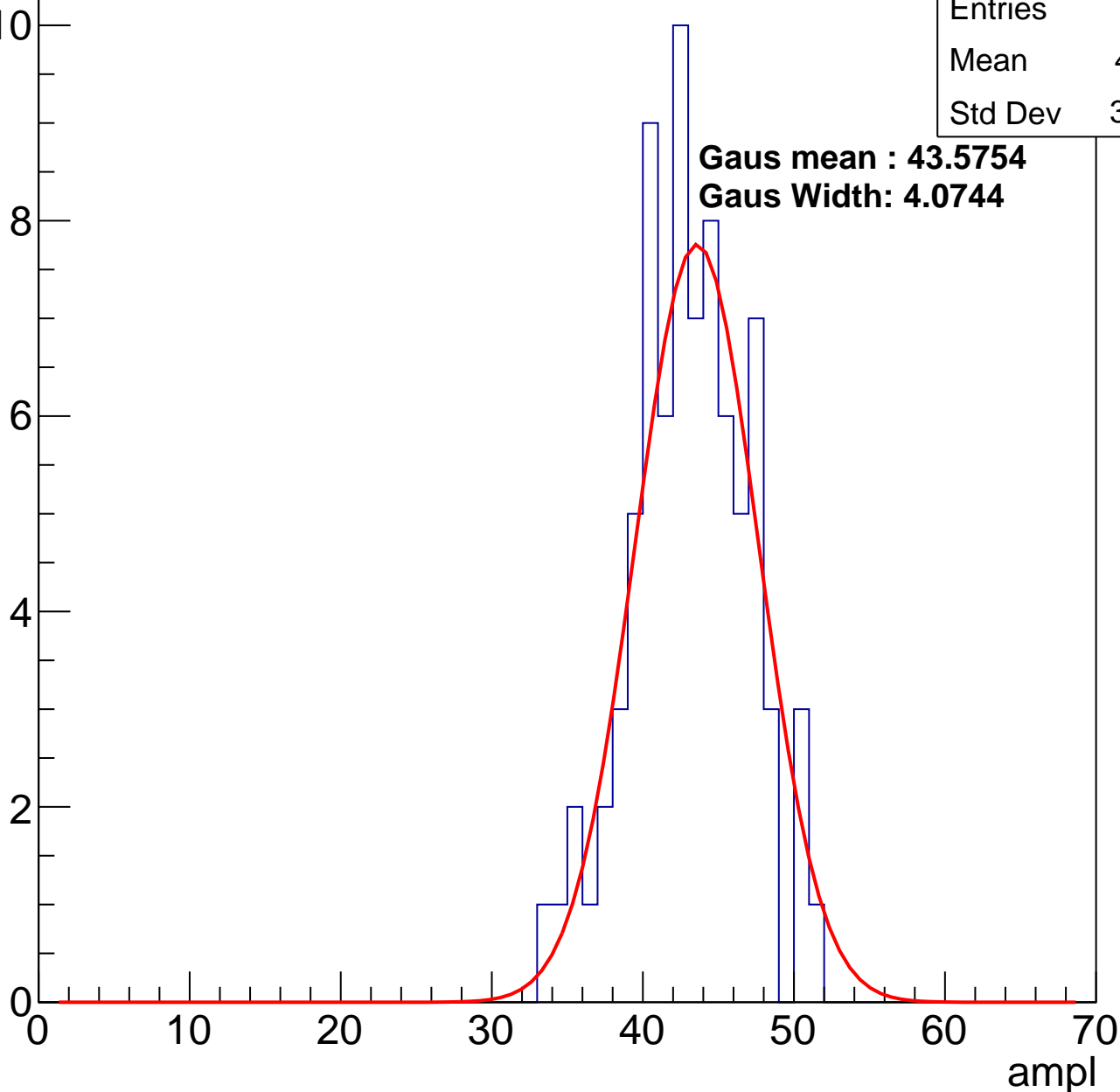
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	42.61
Std Dev	3.813

**Gaus mean : 43.5754**

**Gaus Width: 4.0744**

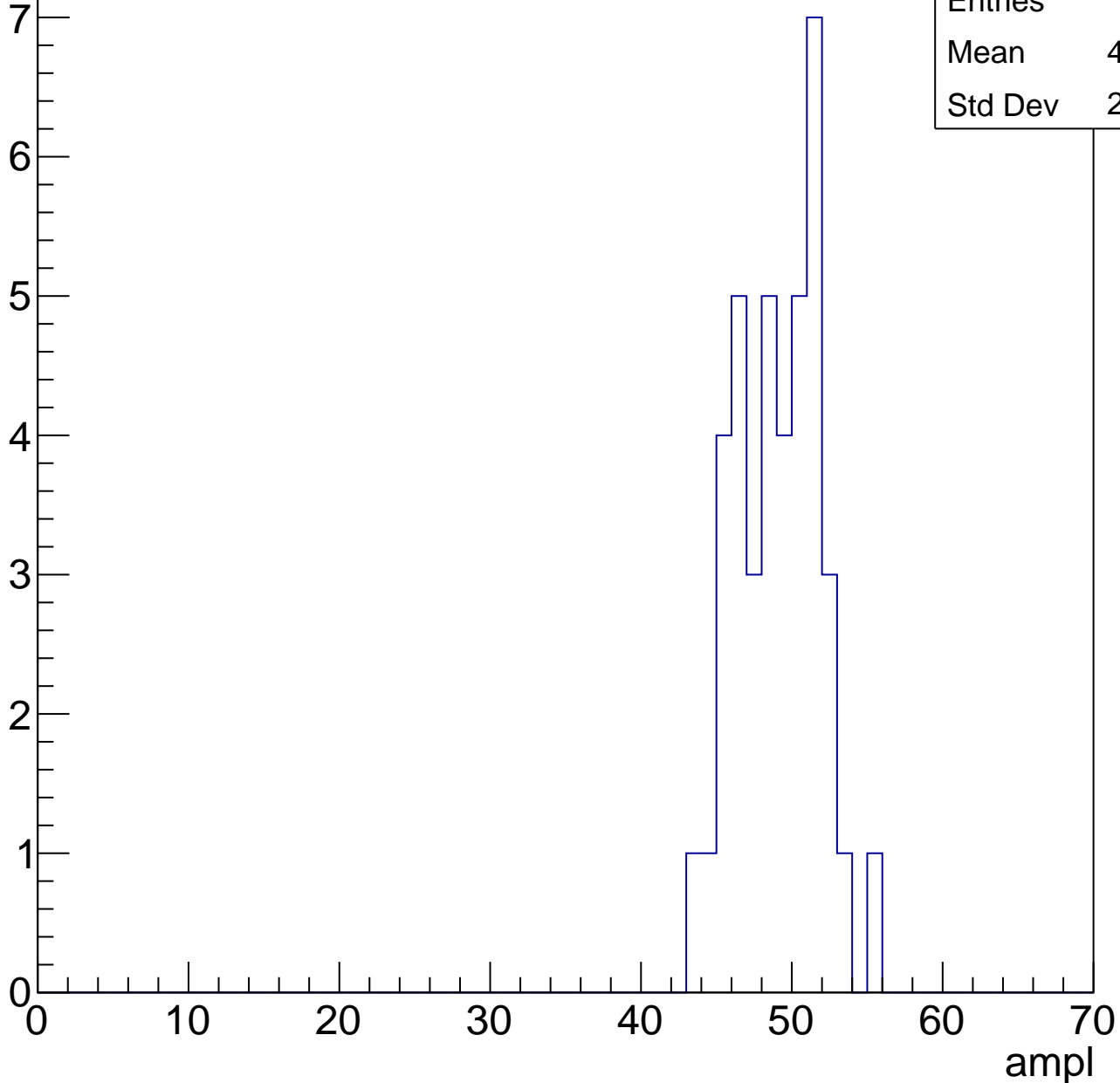


# B1L101S, U3-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	40
Mean	48.62
Std Dev	2.708

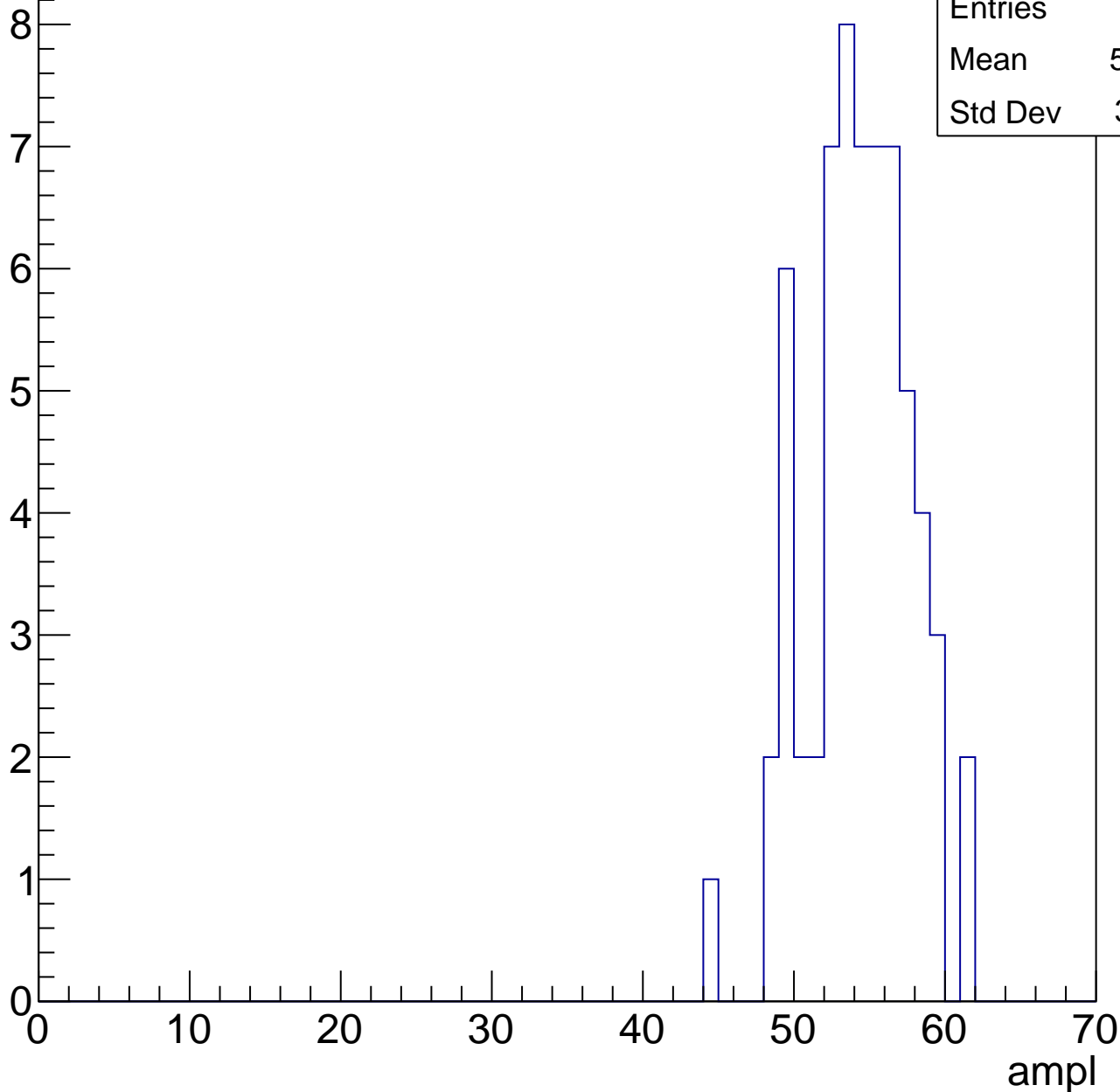


# B1L101S, U3-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

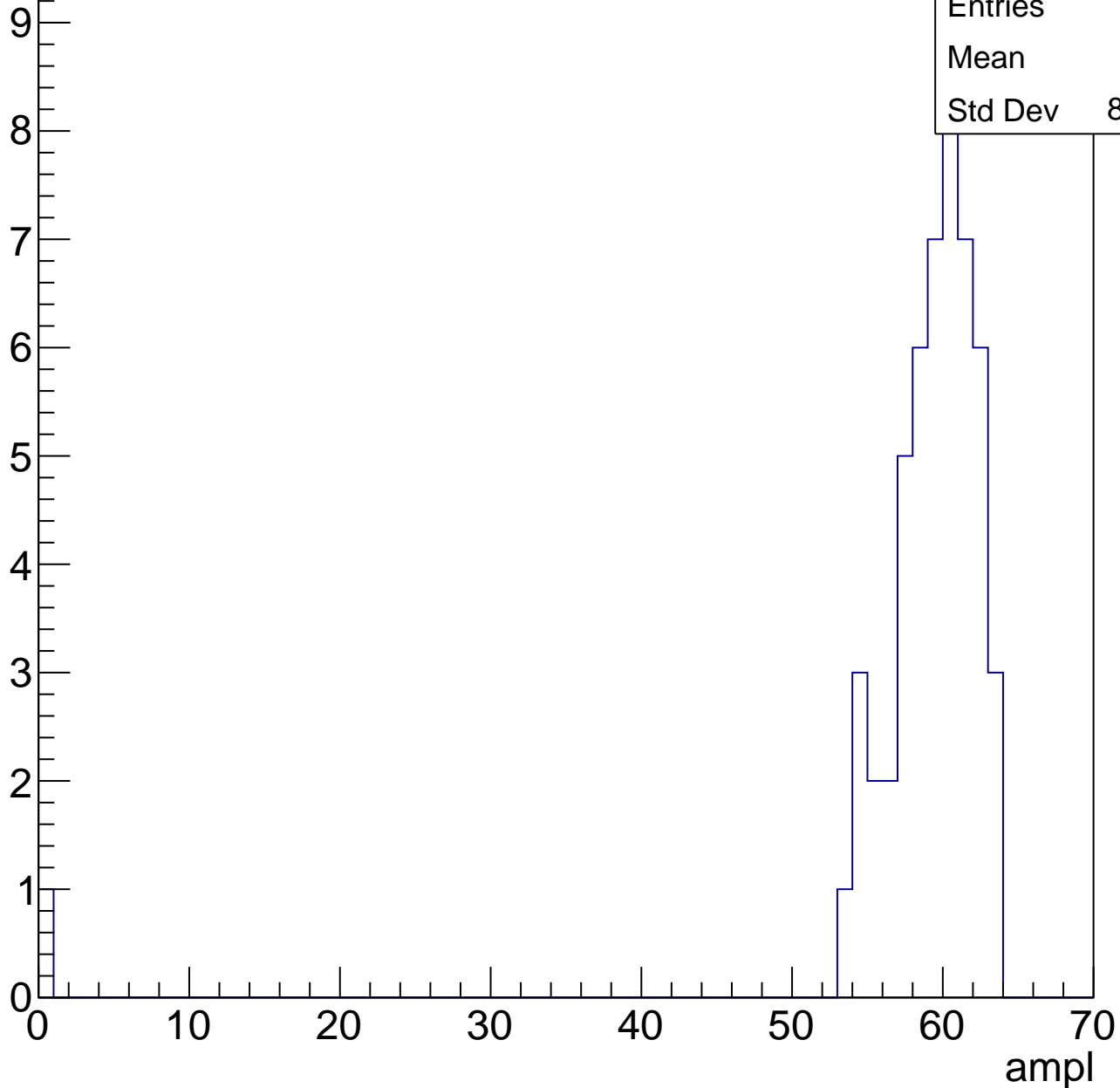
Entries	63
Mean	53.89
Std Dev	3.391



# B1L101S, U3-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

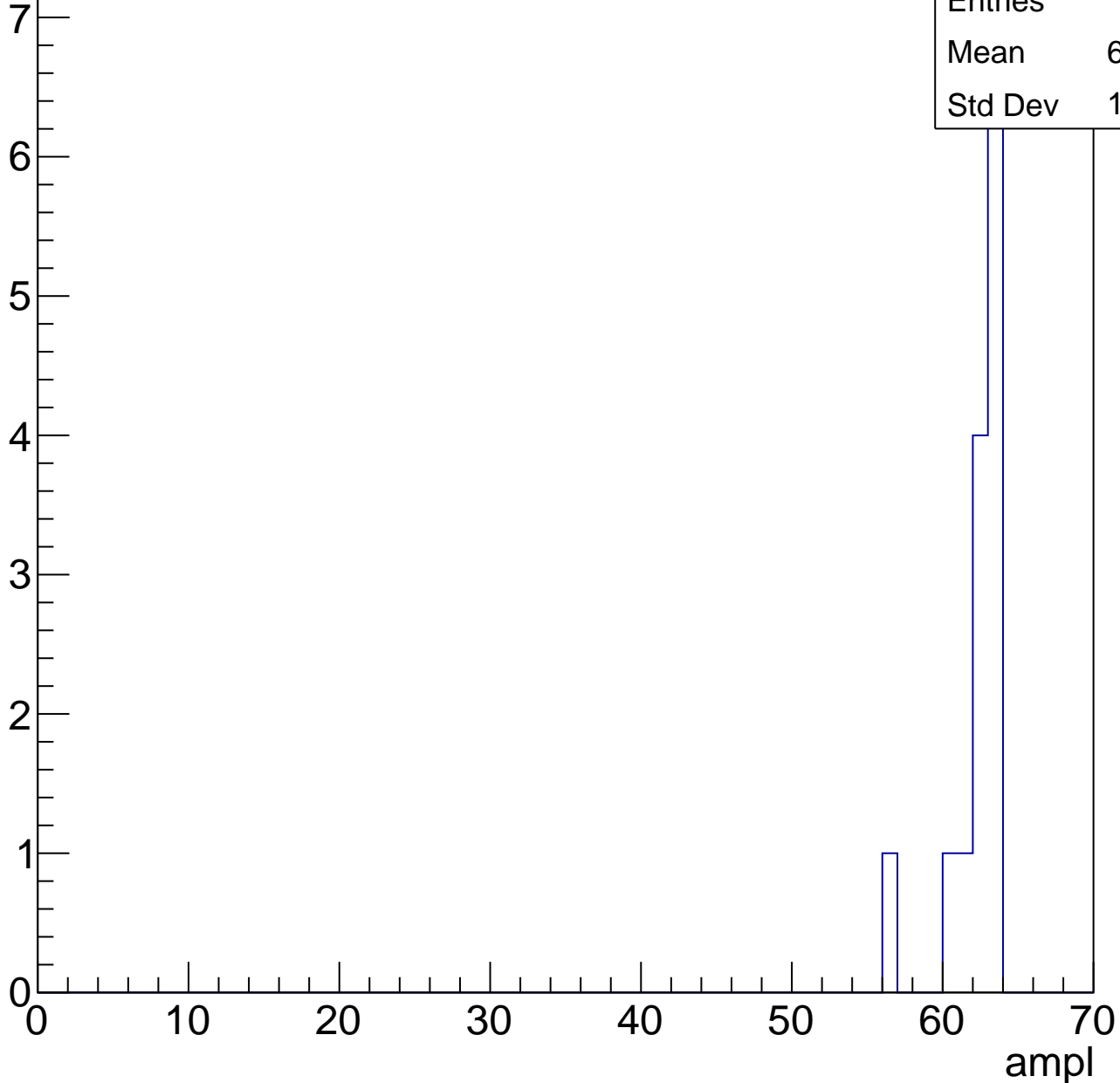


# B1L101S, U3-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	14
Mean	61.86
Std Dev	1.846





# B1L101S, U3-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U3-ch25, adc0

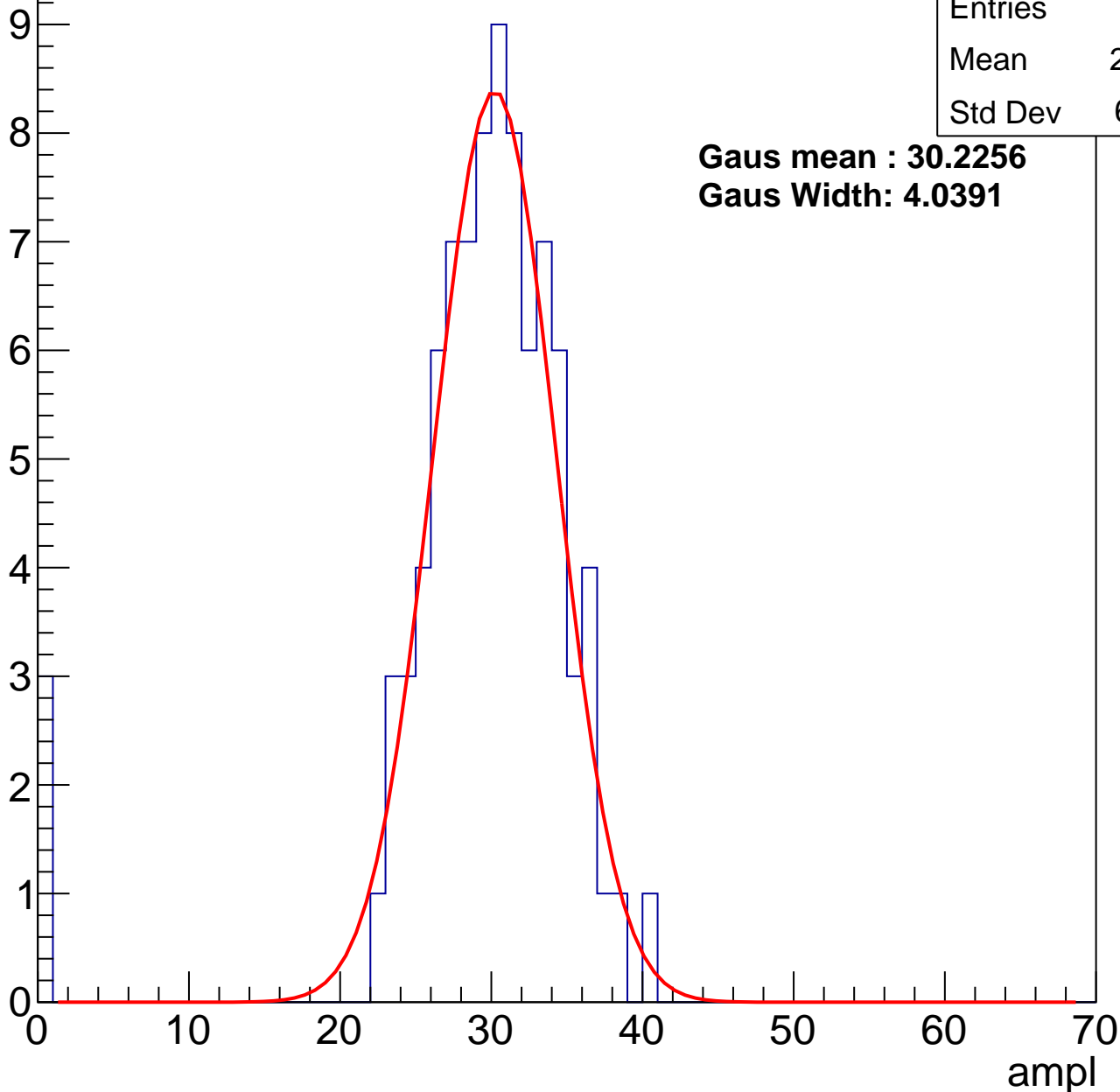
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	88
Mean	28.92
Std Dev	6.601

**Gaus mean : 30.2256**

**Gaus Width: 4.0391**



# B1L101S, U3-ch25, adc1

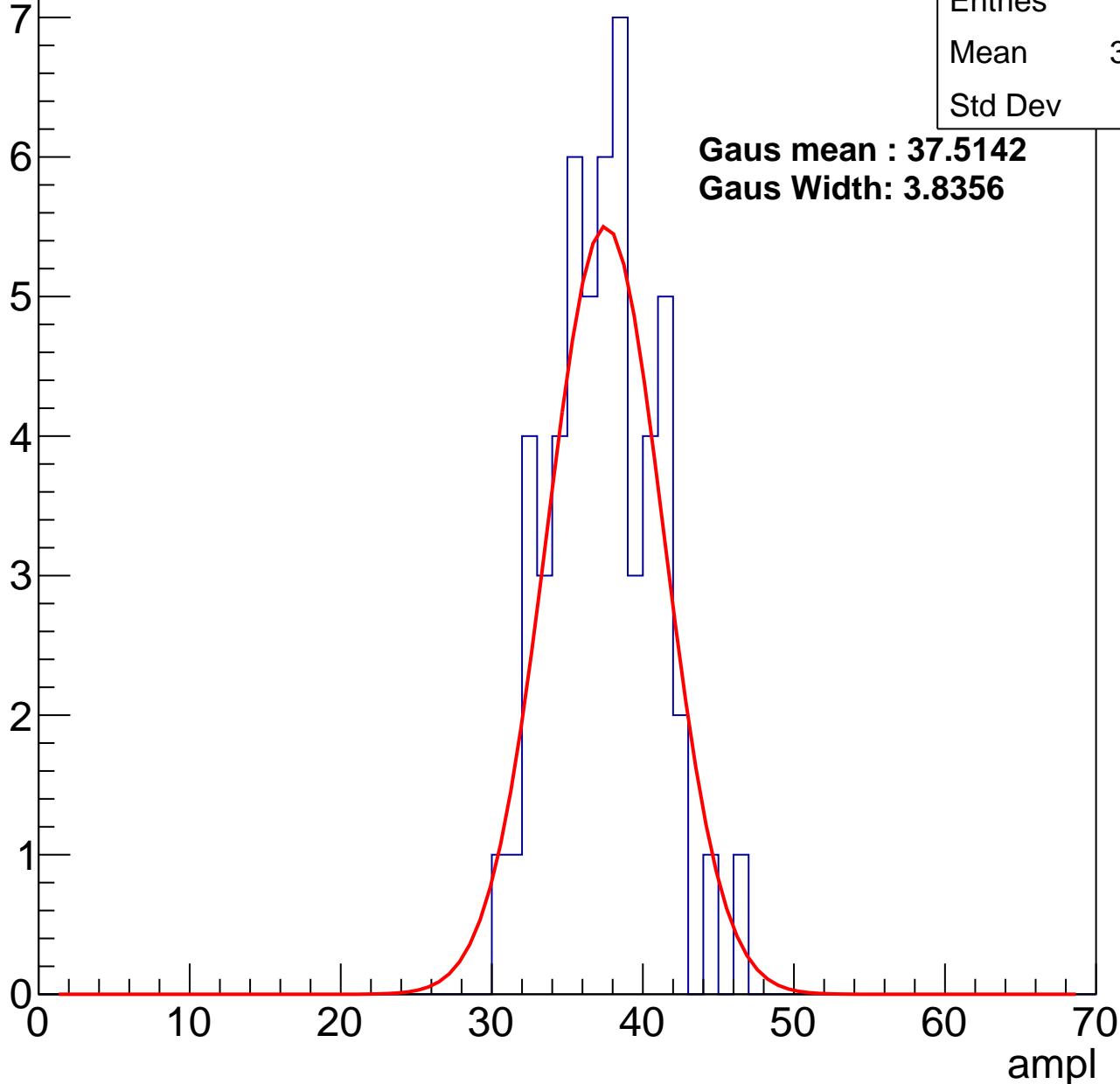
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	36.94
Std Dev	3.4

**Gaus mean : 37.5142**

**Gaus Width: 3.8356**



# B1L101S, U3-ch25, adc2

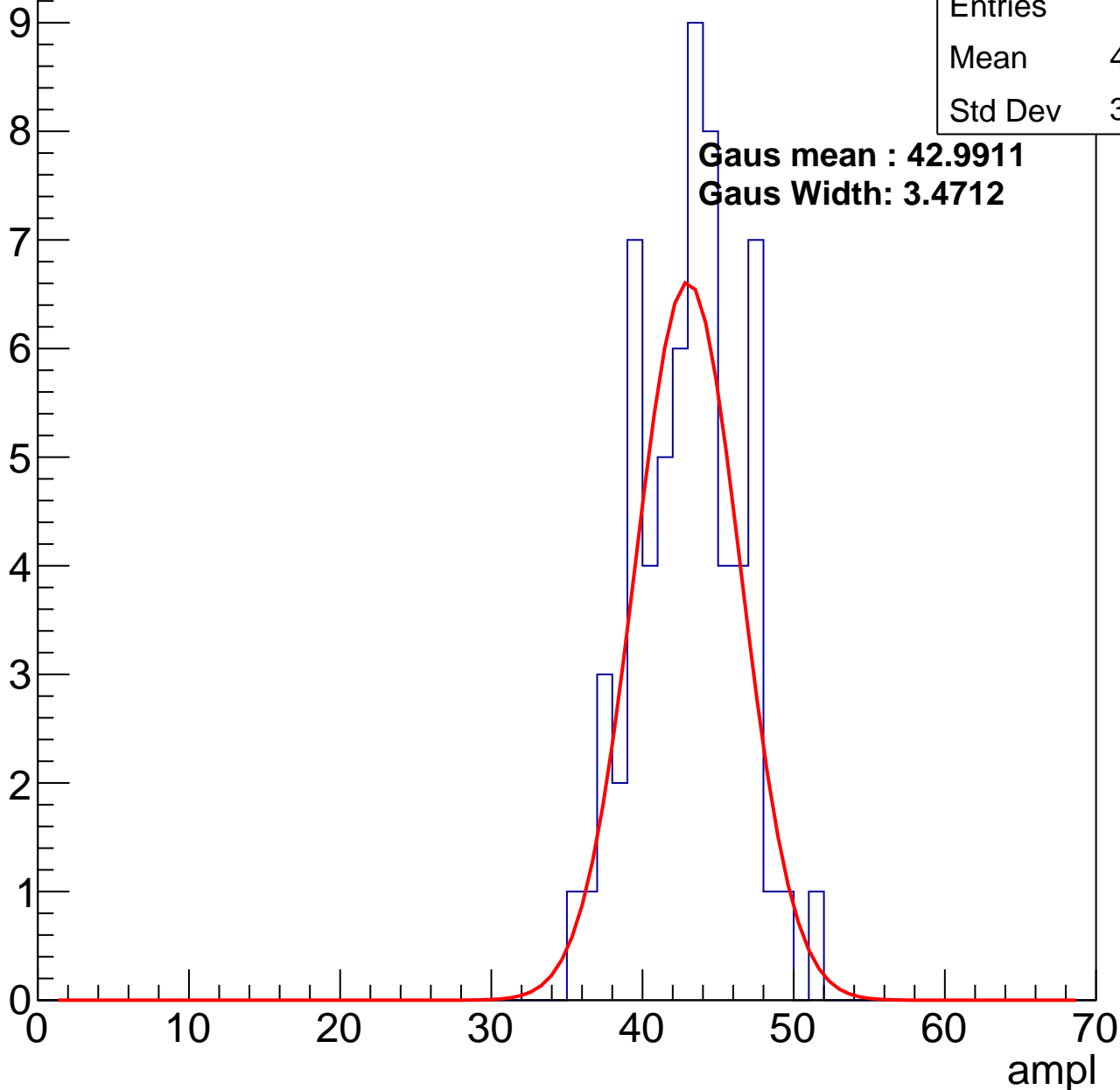
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	42.62
Std Dev	3.384

**Gaus mean : 42.9911**

**Gaus Width: 3.4712**



# B1L101S, U3-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	80
Mean	49.9
Std Dev	3.807

Entry

10

8

6

4

2

0

0

10

20

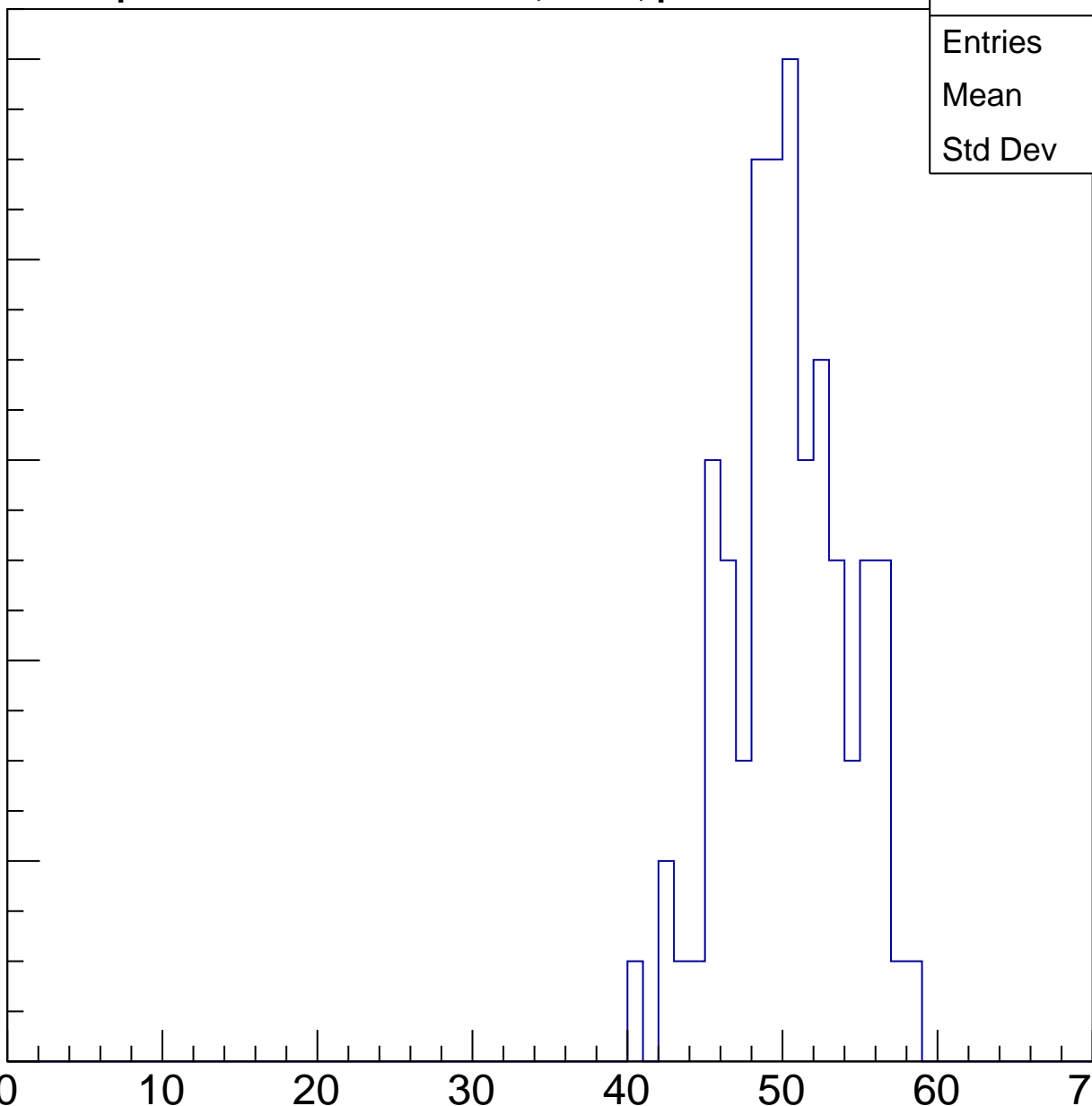
30

40

50

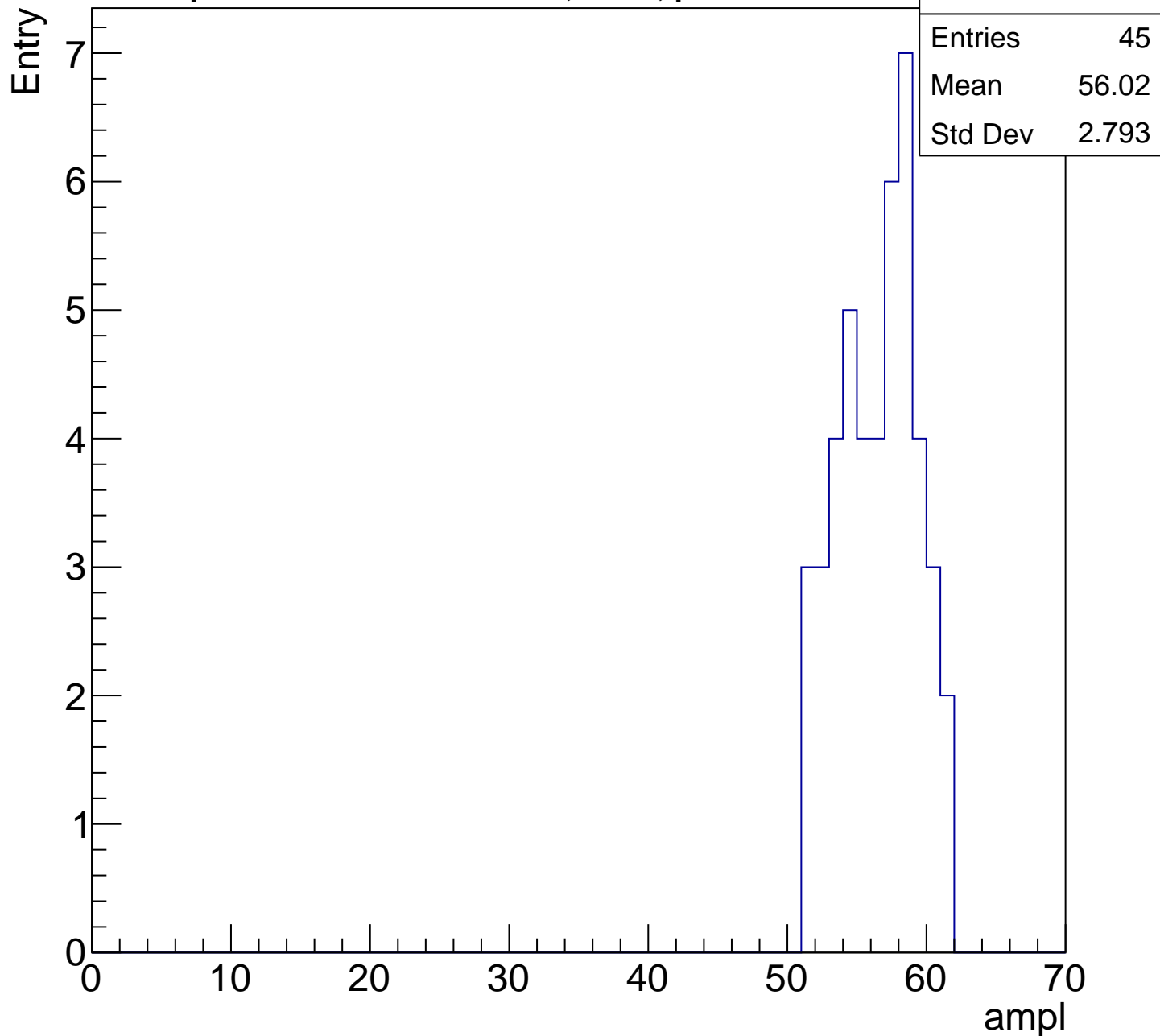
60

ampl



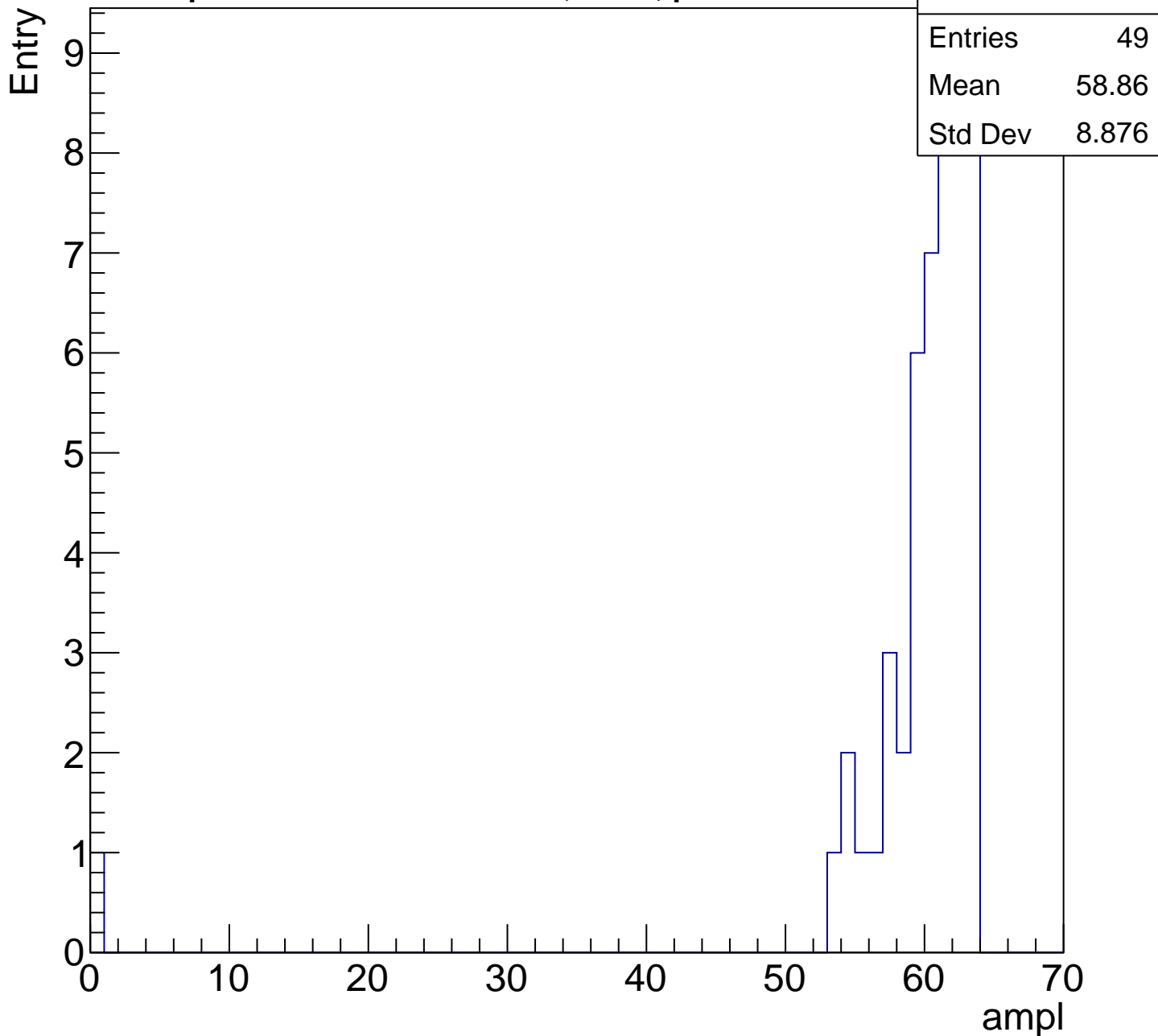
# B1L101S, U3-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch25, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U3-ch26, adc0

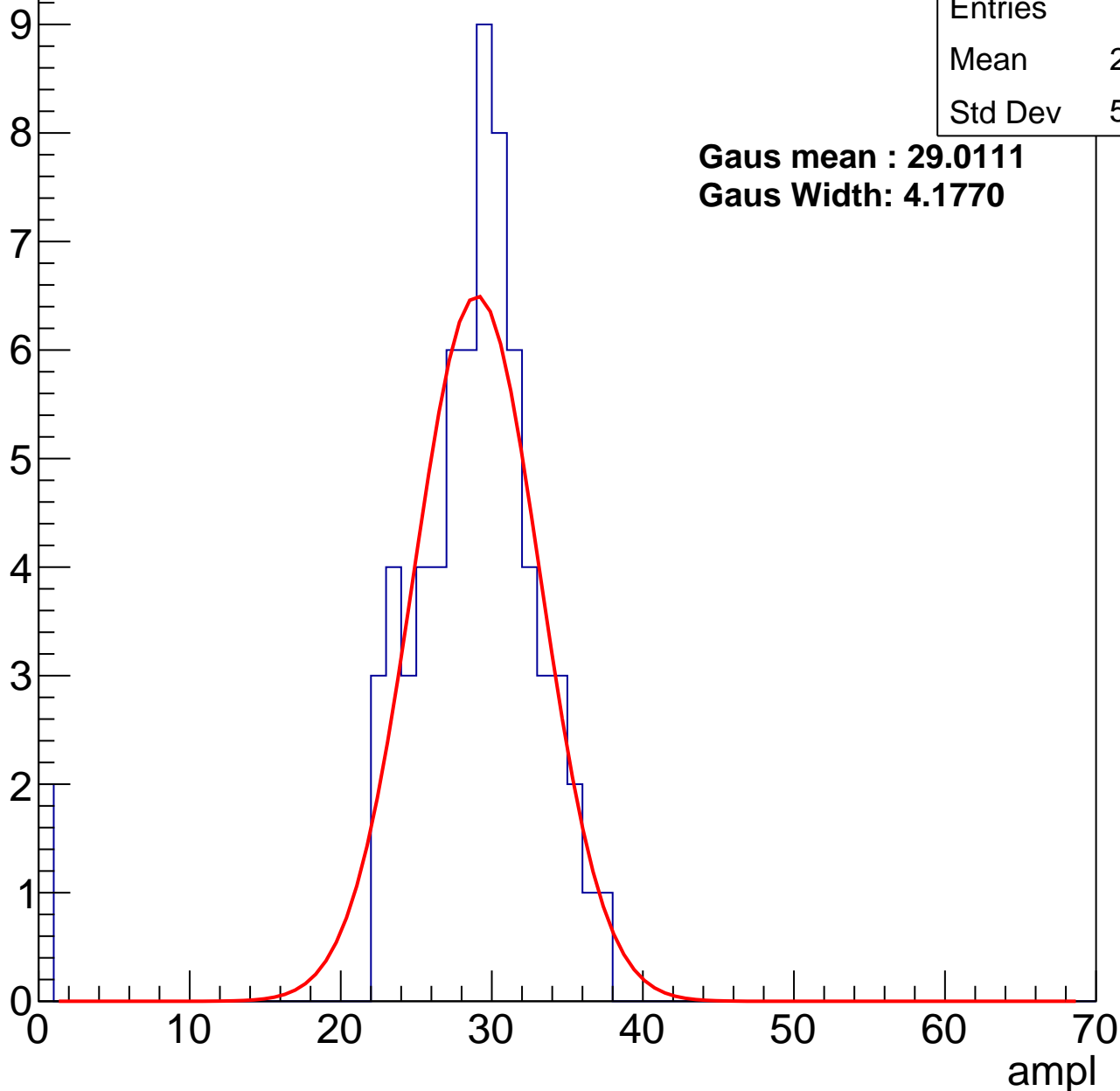
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	27.87
Std Dev	5.978

**Gaus mean : 29.0111**

**Gaus Width: 4.1770**



# B1L101S, U3-ch26, adc1

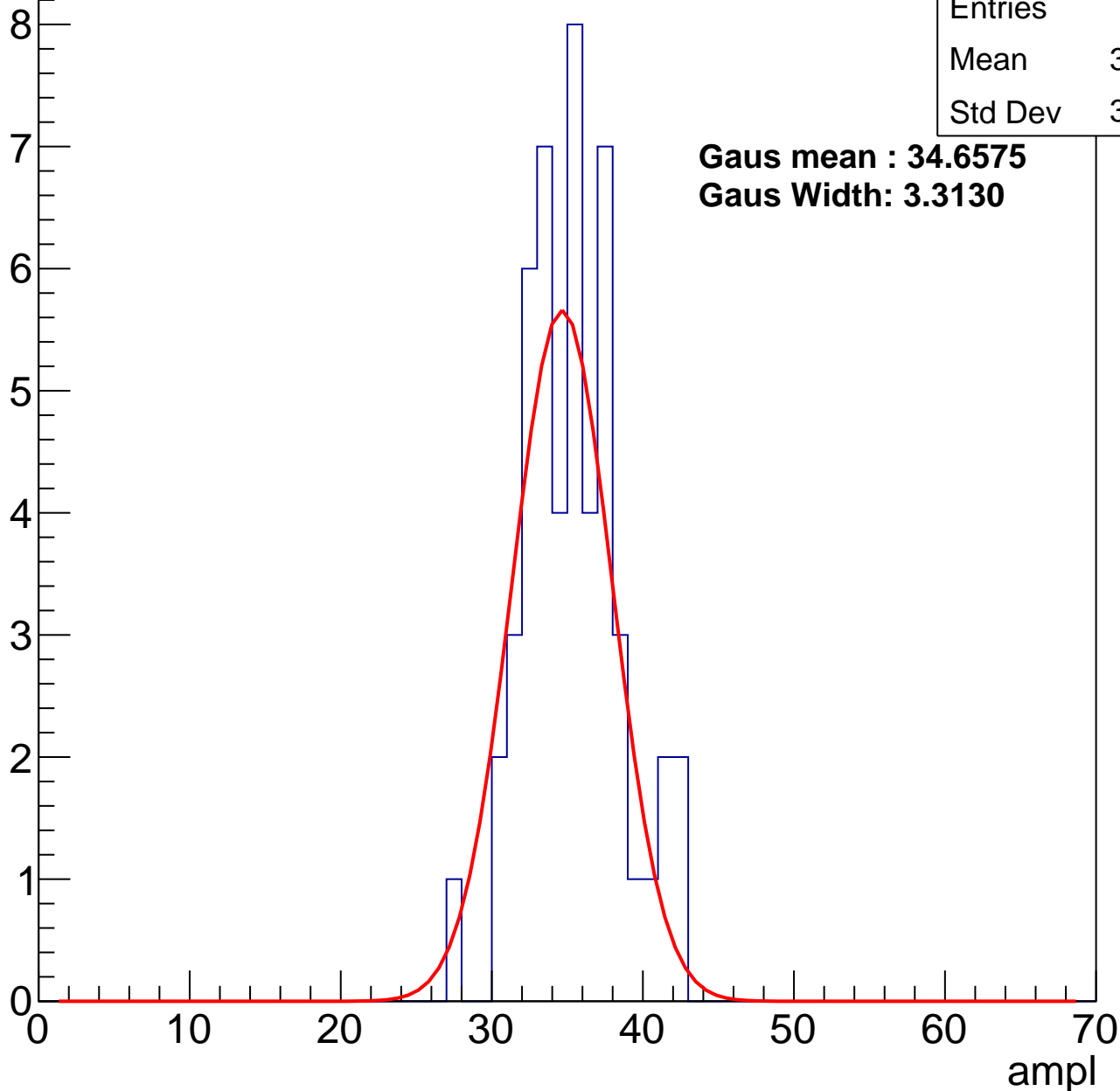
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	34.92
Std Dev	3.186

**Gaus mean : 34.6575**

**Gaus Width: 3.3130**



# B1L101S, U3-ch26, adc2

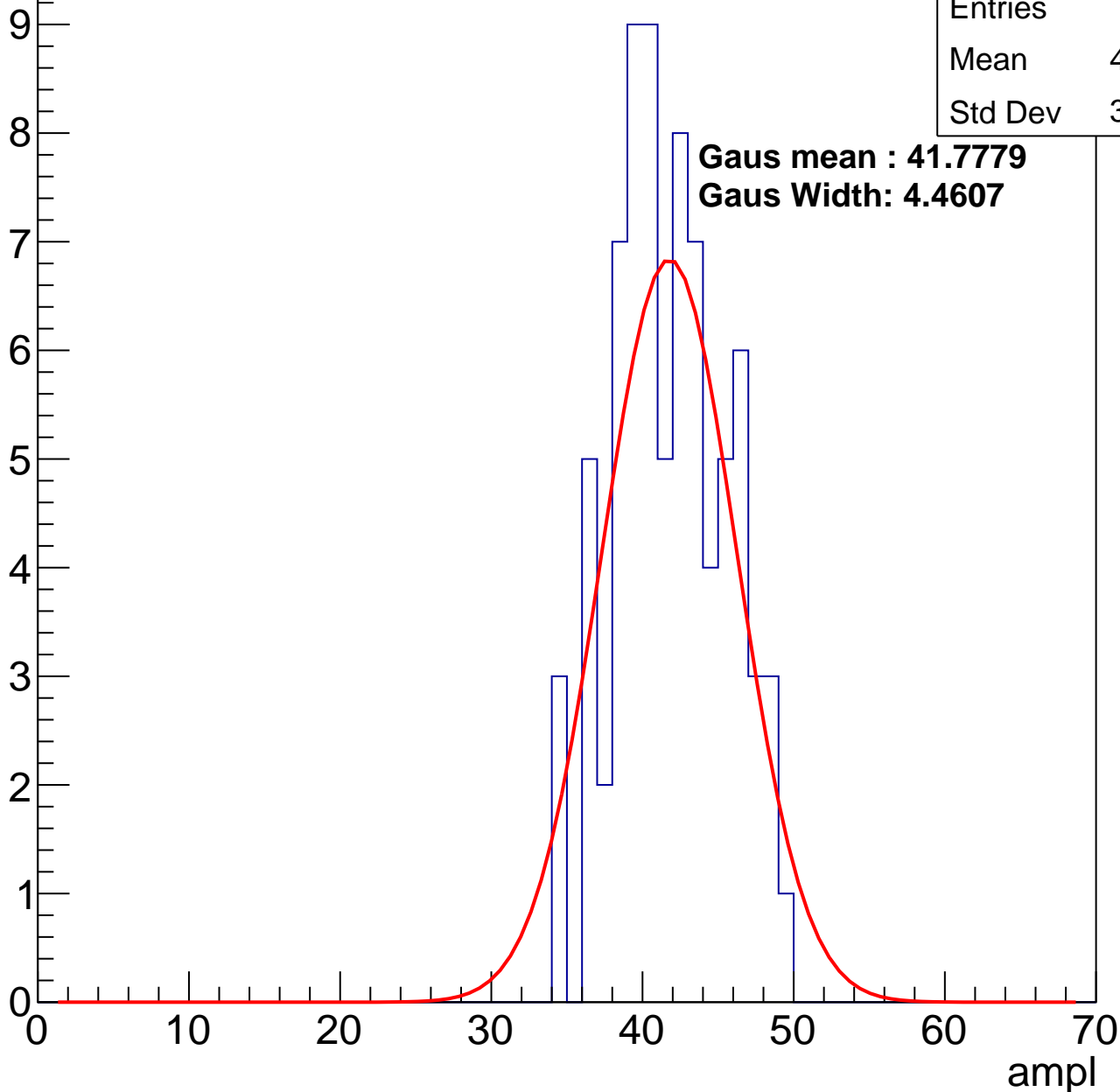
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	41.38
Std Dev	3.643

**Gaus mean : 41.7779**

**Gaus Width: 4.4607**

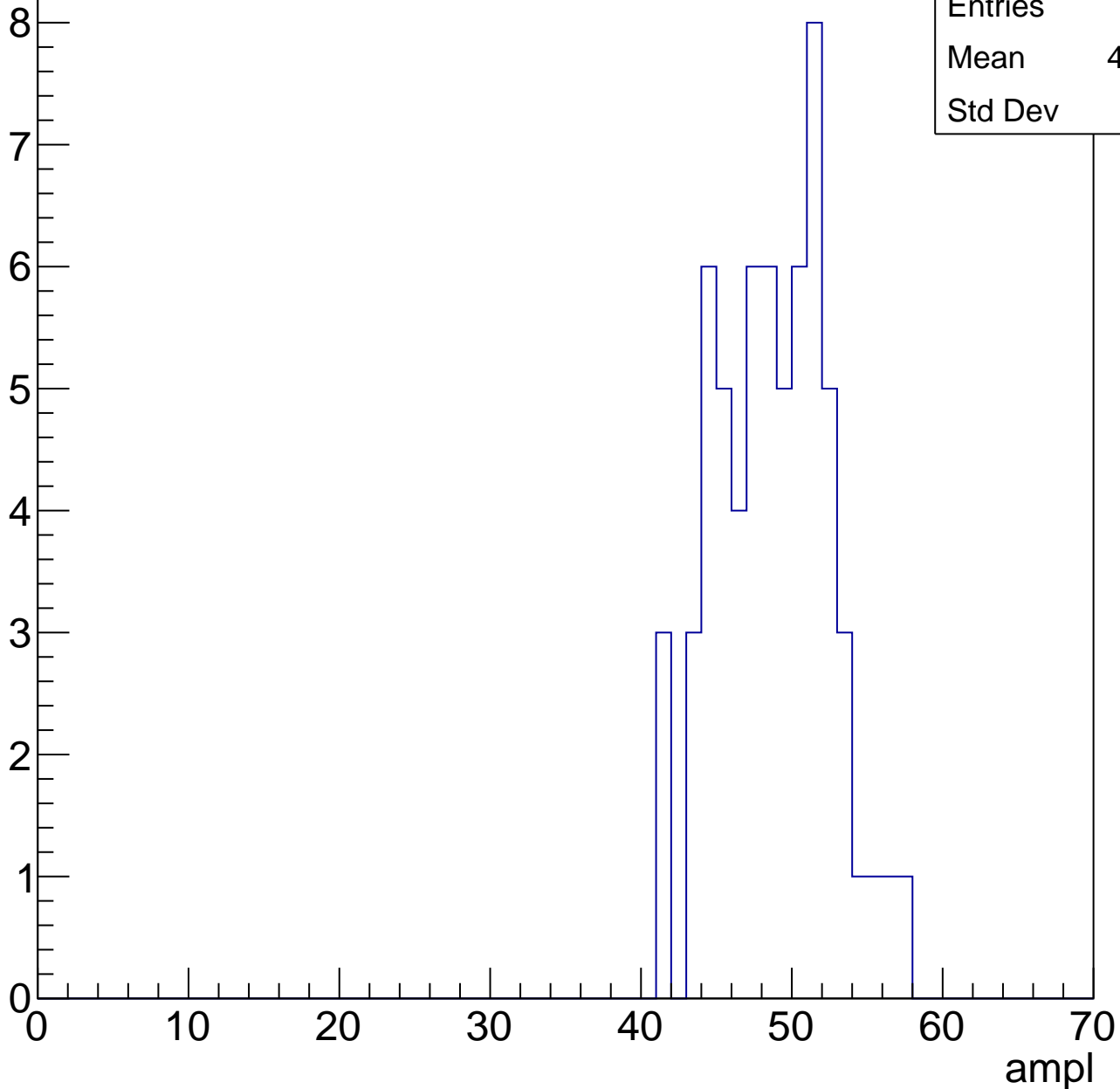


# B1L101S, U3-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	48.27
Std Dev	3.68

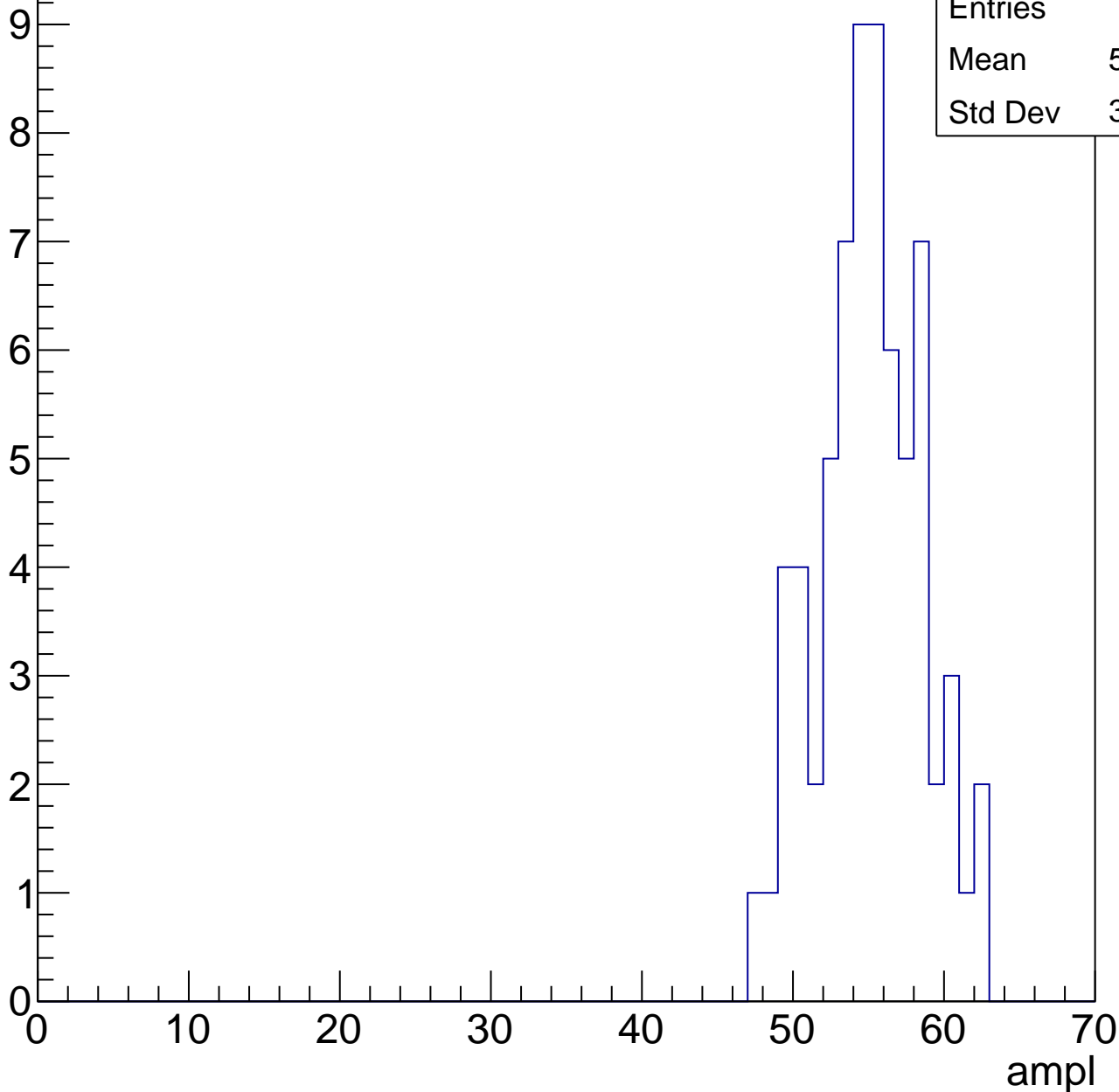


# B1L101S, U3-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

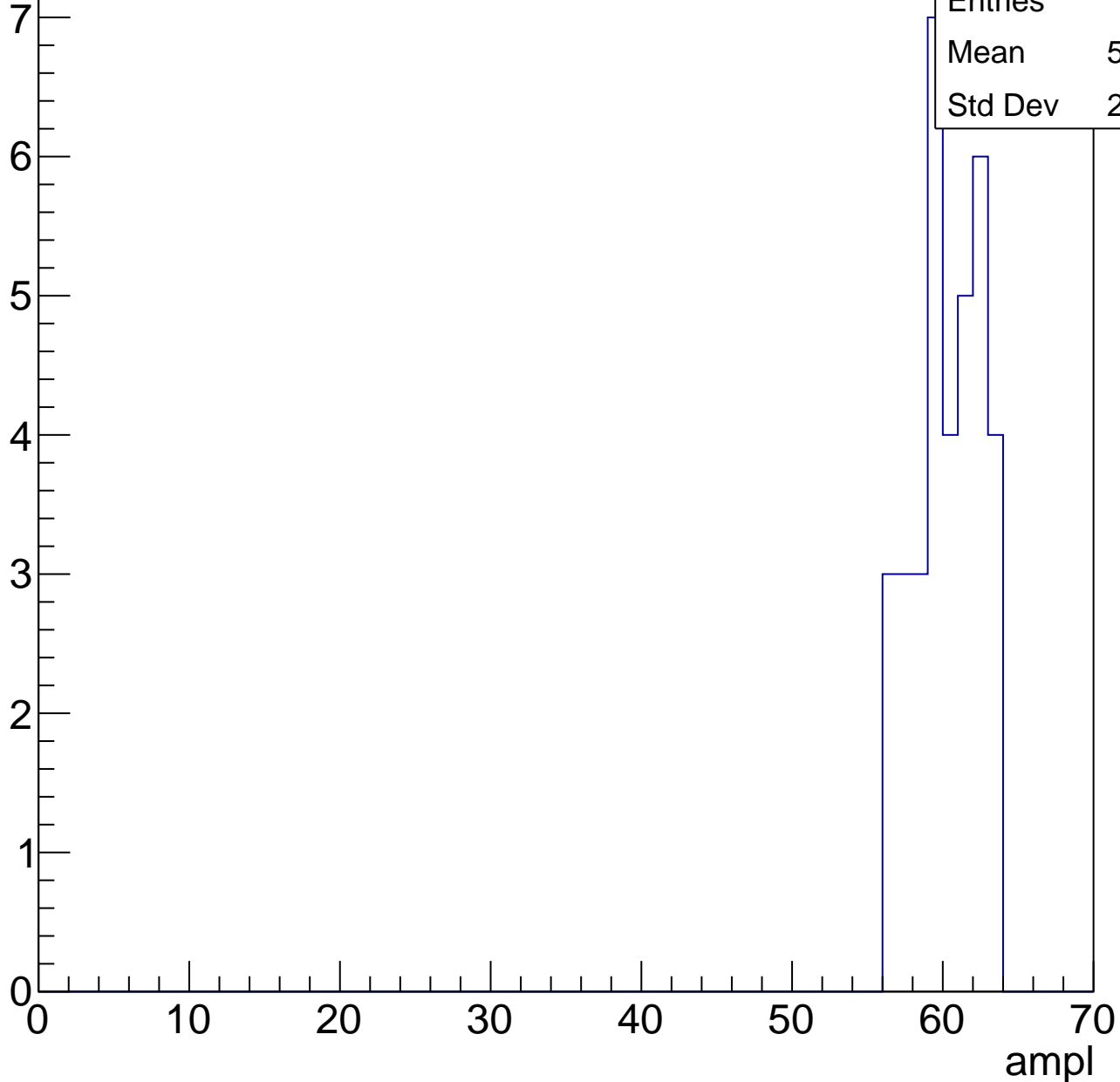
Entries	68
Mean	54.63
Std Dev	3.412



# B1L101S, U3-ch26, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

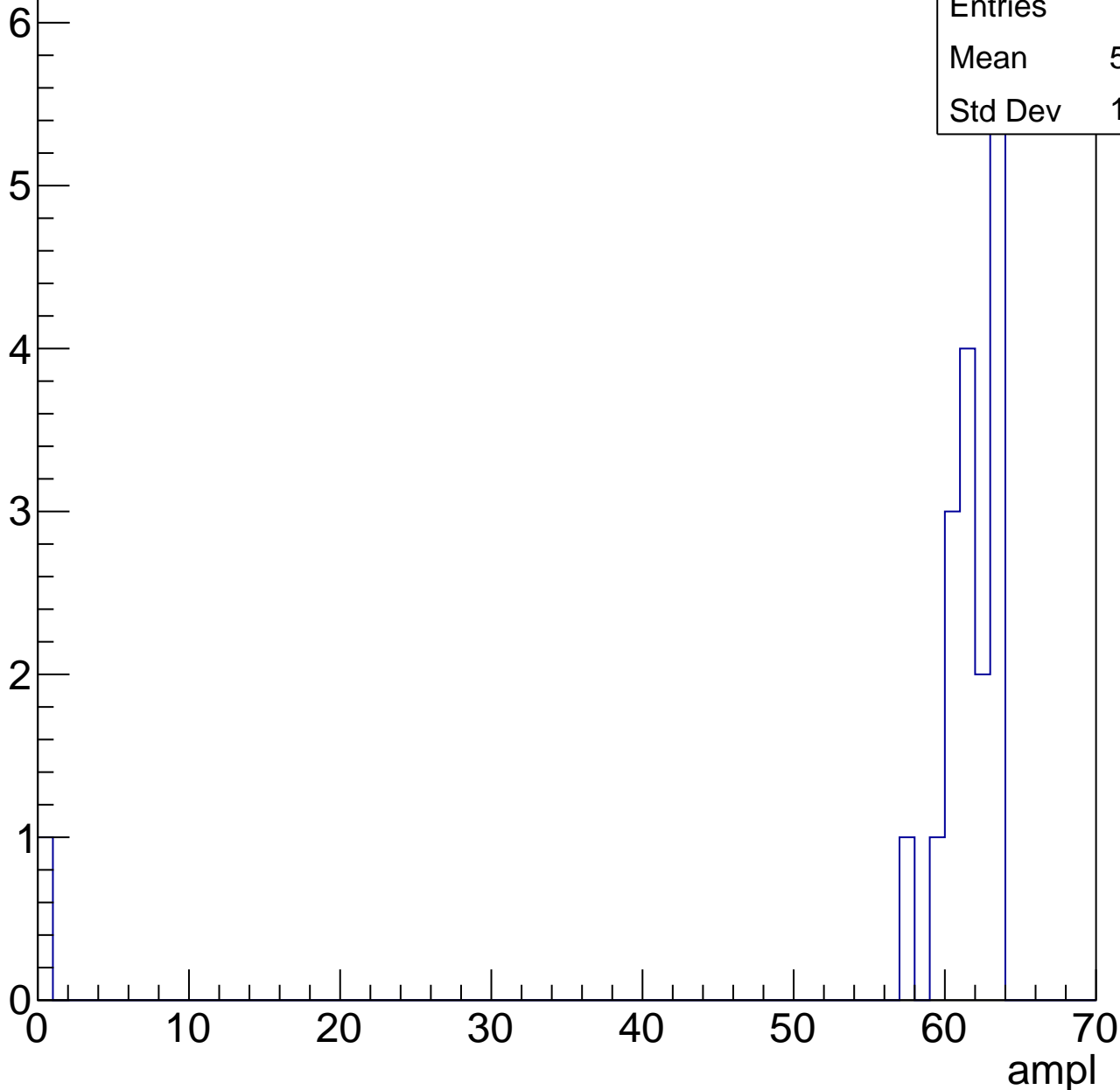


# B1L101S, U3-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	18
Mean	57.89
Std Dev	14.13





# B1L101S, U3-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	20
Std Dev	0

# B1L101S, U3-ch27, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	76
Mean	29.01
Std Dev	5.809

**Gaus mean : 29.7564**

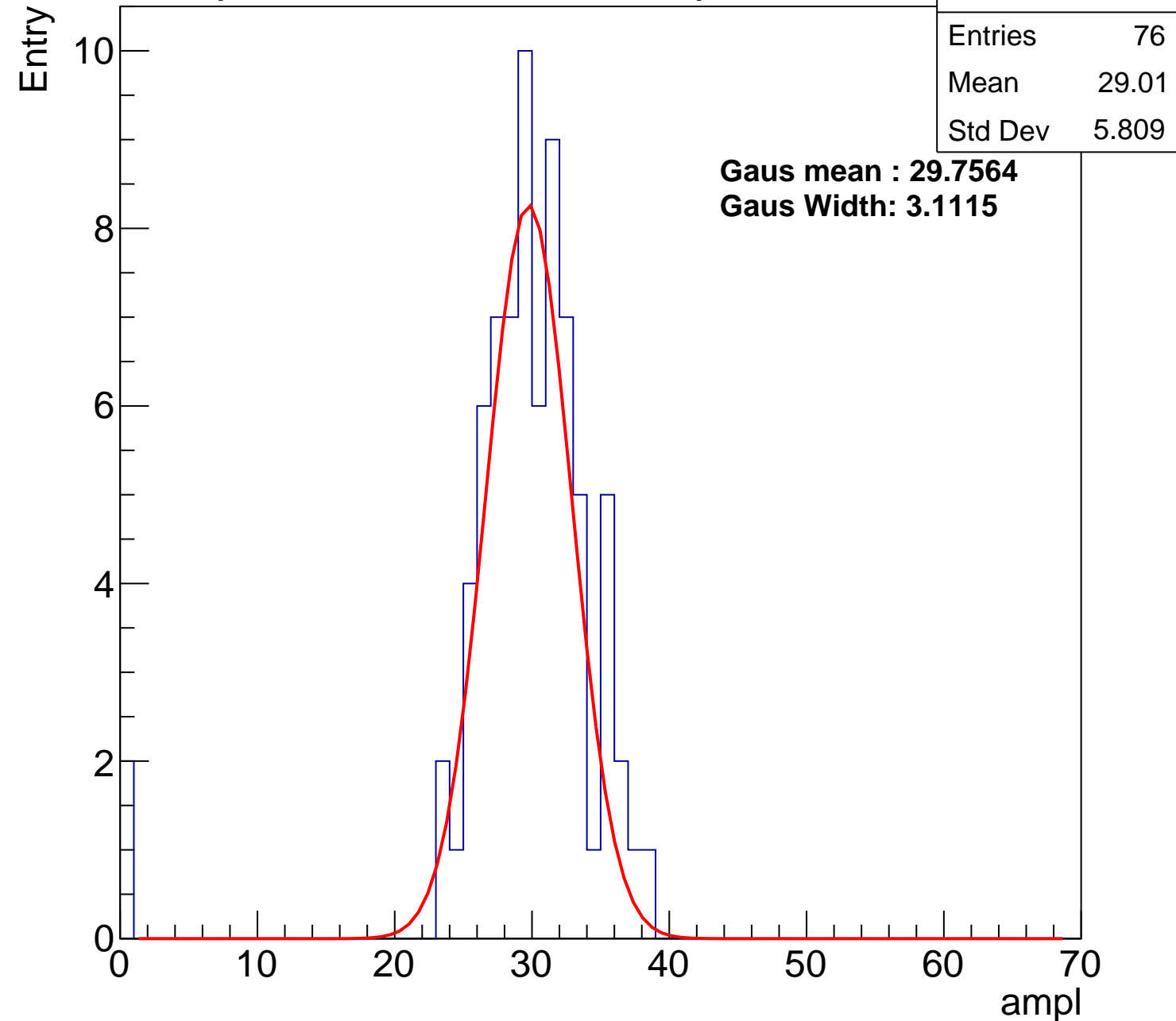
**Gaus Width: 3.1115**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U3-ch27, adc1

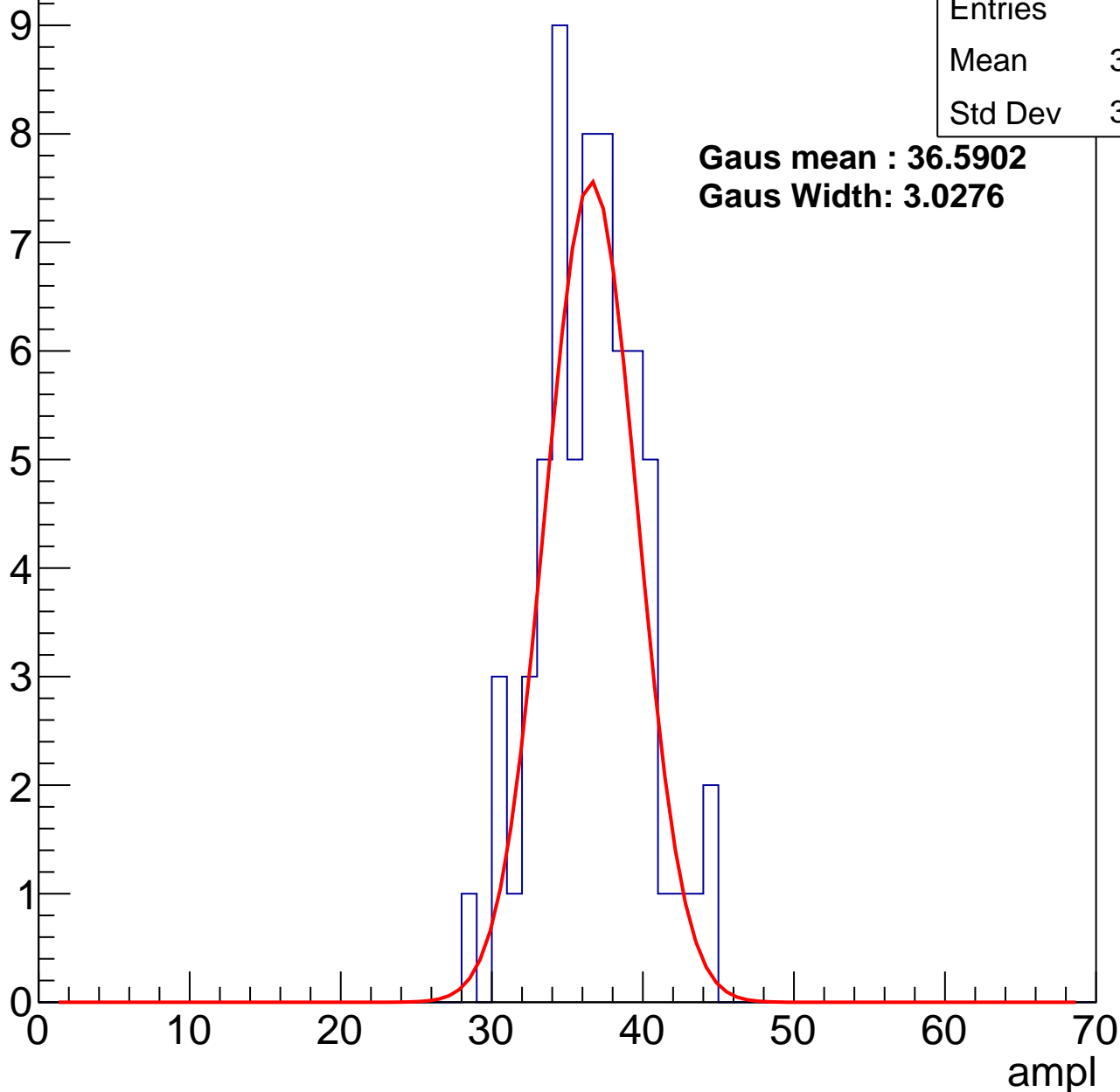
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	36.17
Std Dev	3.358

**Gaus mean : 36.5902**

**Gaus Width: 3.0276**



# B1L101S, U3-ch27, adc2

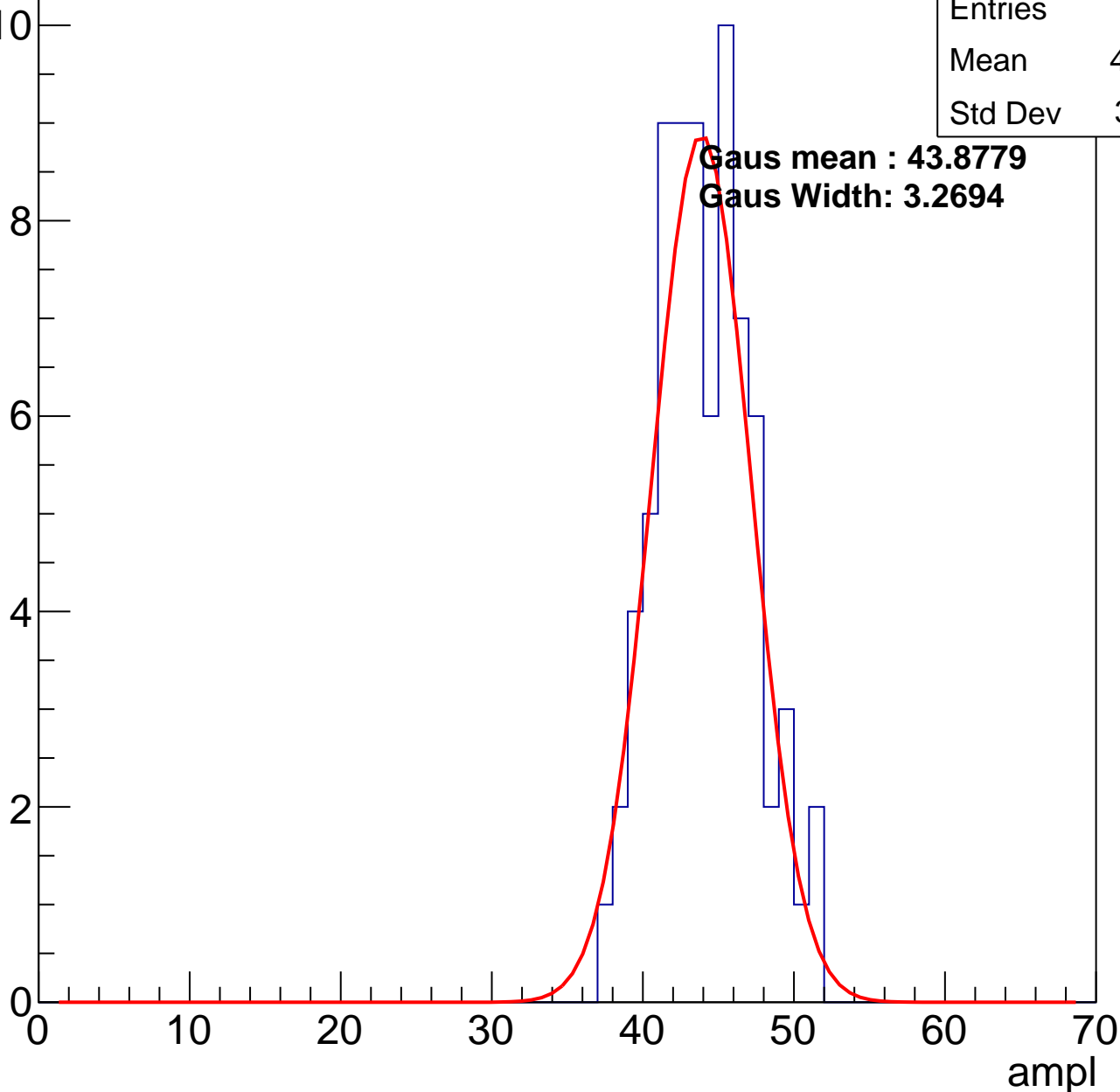
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	43.63
Std Dev	3.141

**Gaus mean : 43.8779**

**Gaus Width: 3.2694**

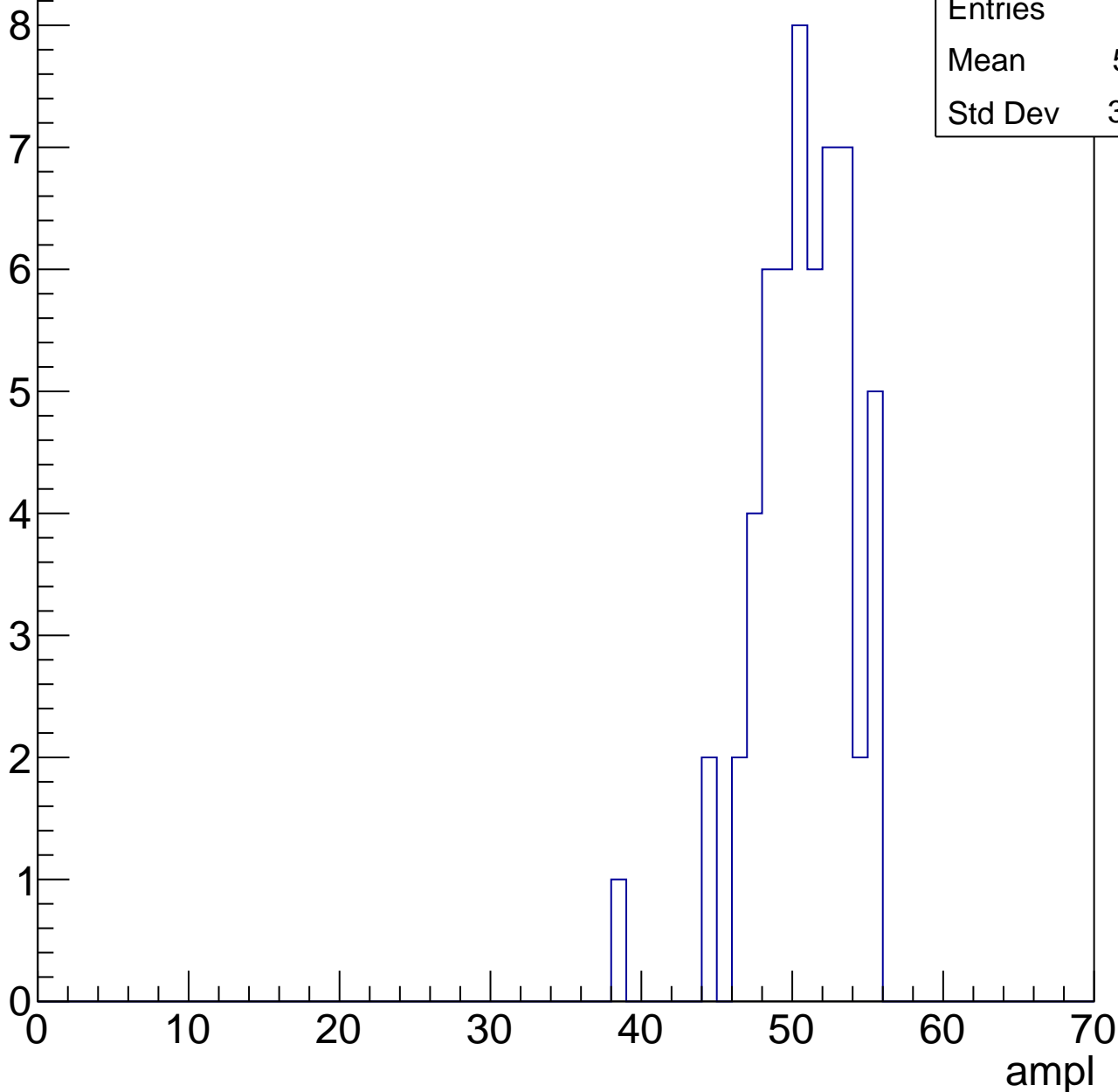


# B1L101S, U3-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	50.21
Std Dev	3.178

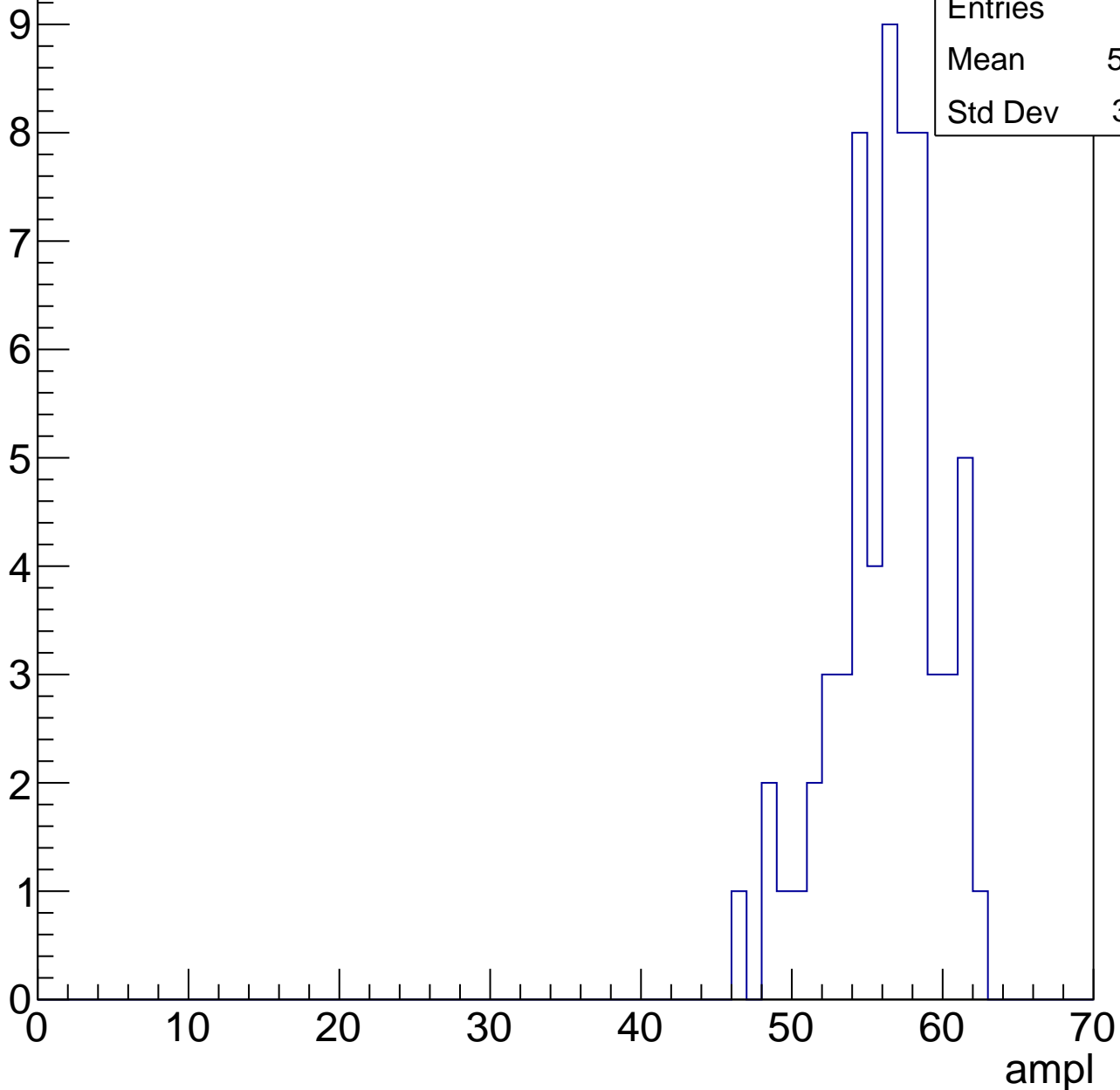


# B1L101S, U3-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

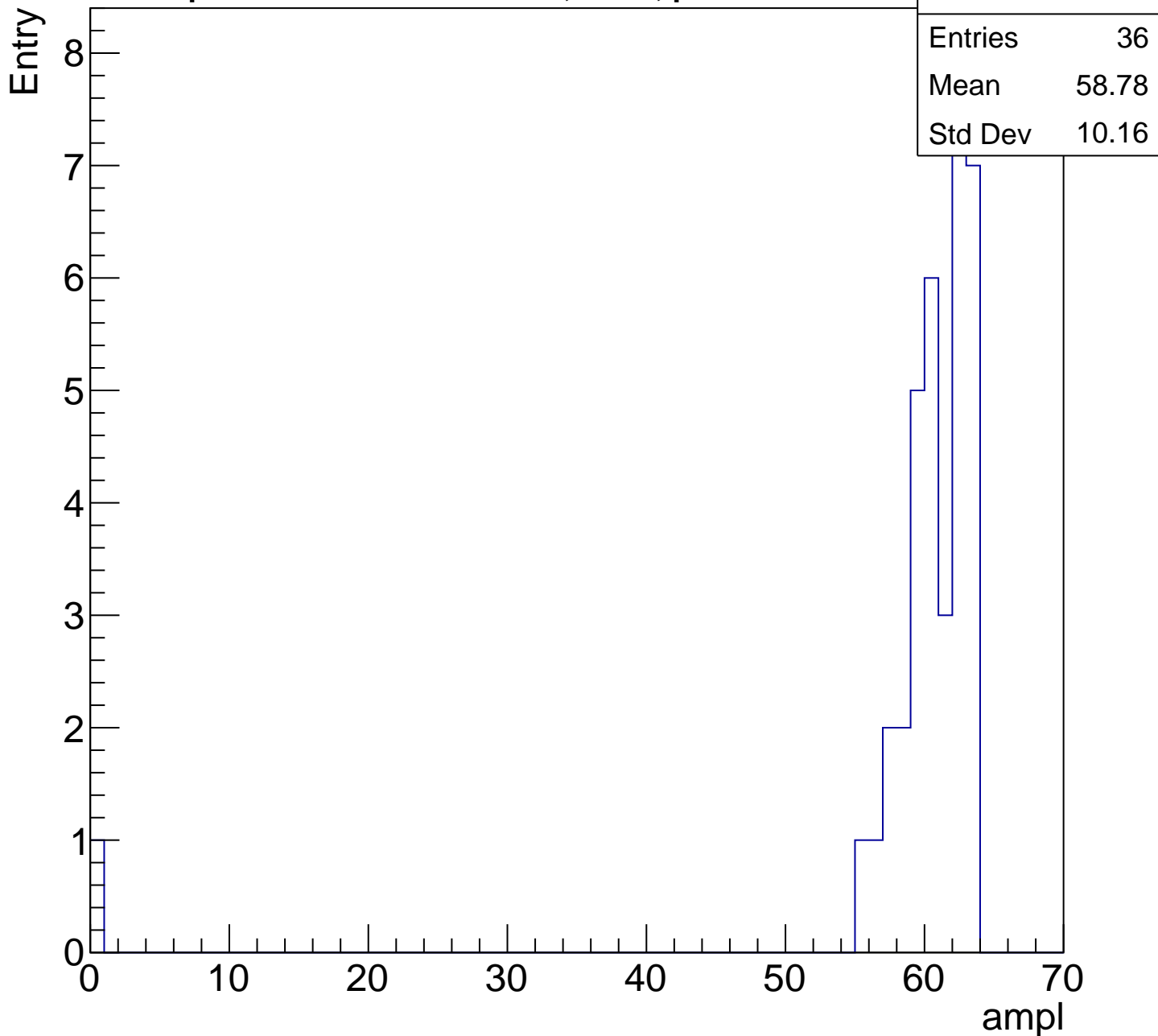
Entry

Entries	62
Mean	55.77
Std Dev	3.471



# B1L101S, U3-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

3

2.5

2

1.5

1

0.5

0

Entries

9

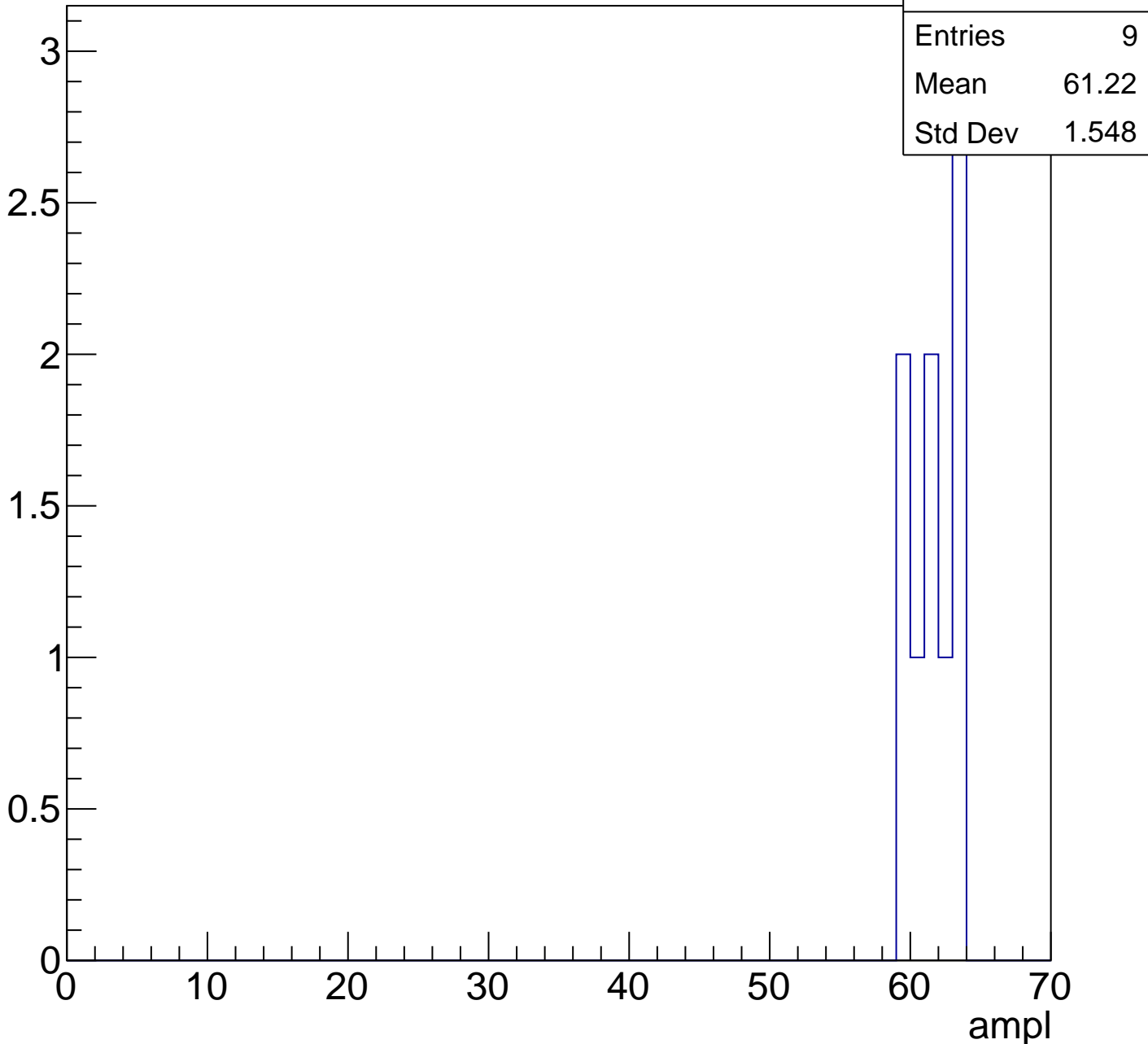
Mean

61.22

Std Dev

1.548

ampl





# B1L101S, U3-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U3-ch28, adc0

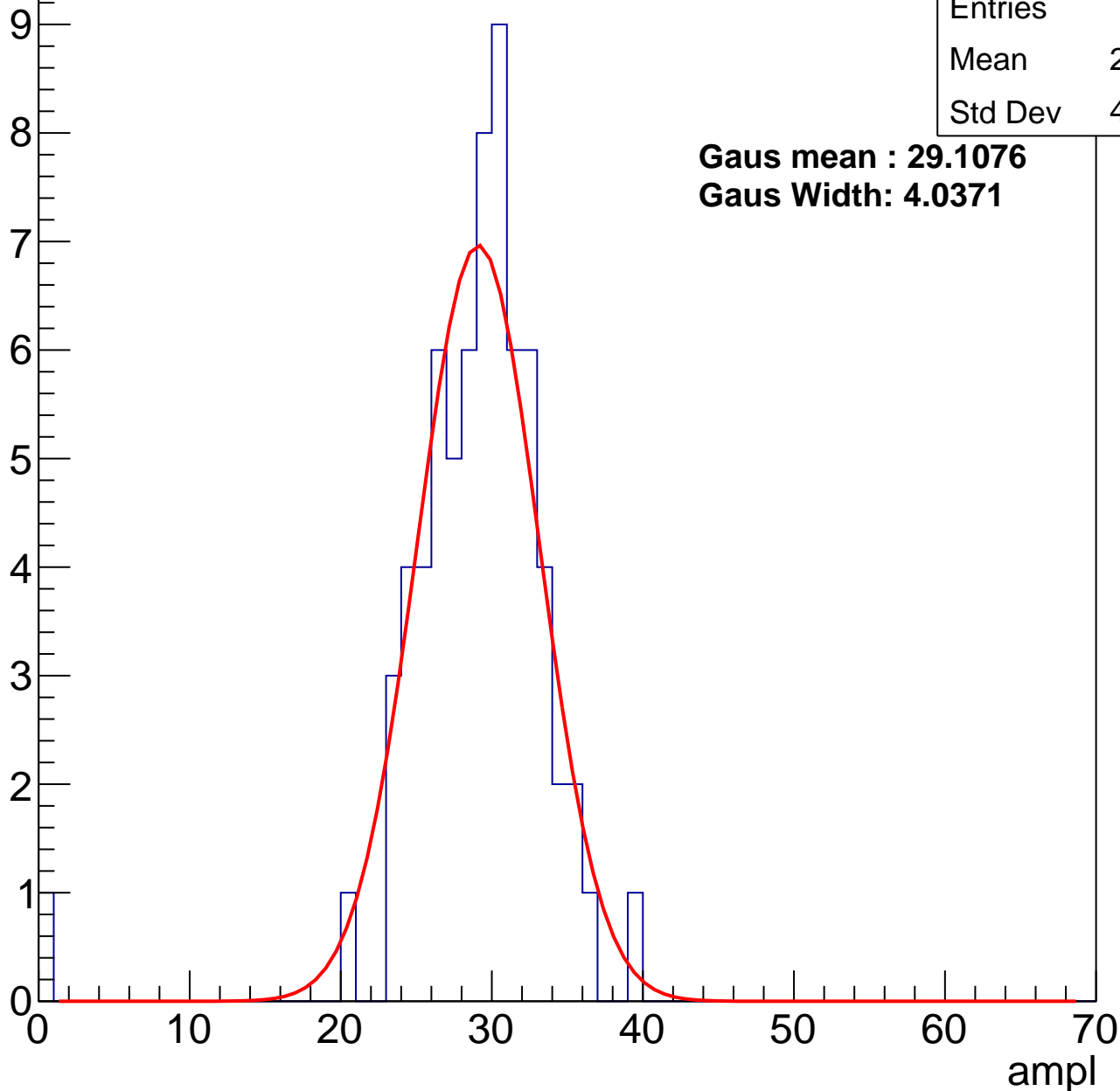
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	28.54
Std Dev	4.936

**Gaus mean : 29.1076**

**Gaus Width: 4.0371**



# B1L101S, U3-ch28, adc1

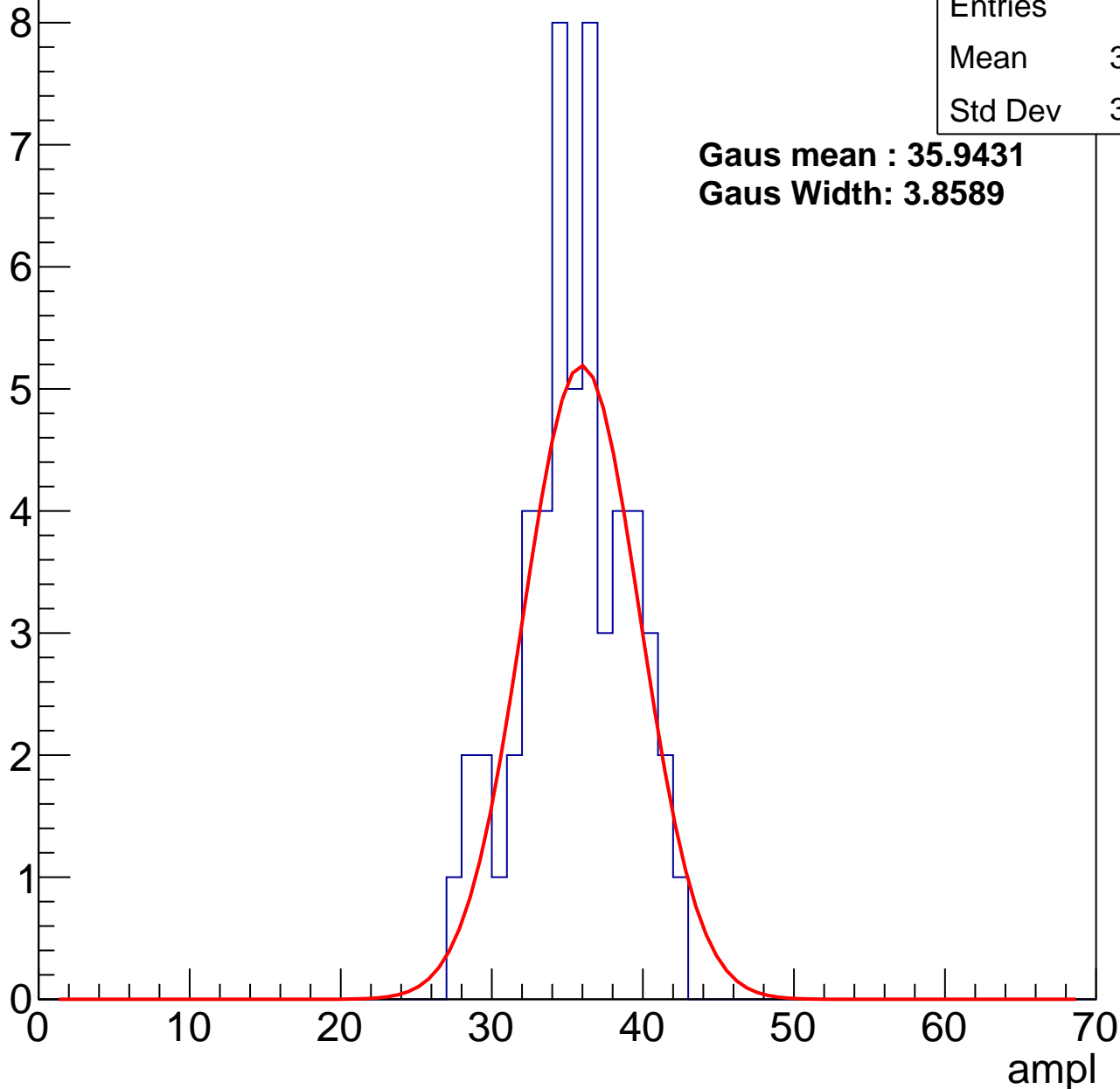
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	35.02
Std Dev	3.514

**Gaus mean : 35.9431**

**Gaus Width: 3.8589**



# B1L101S, U3-ch28, adc2

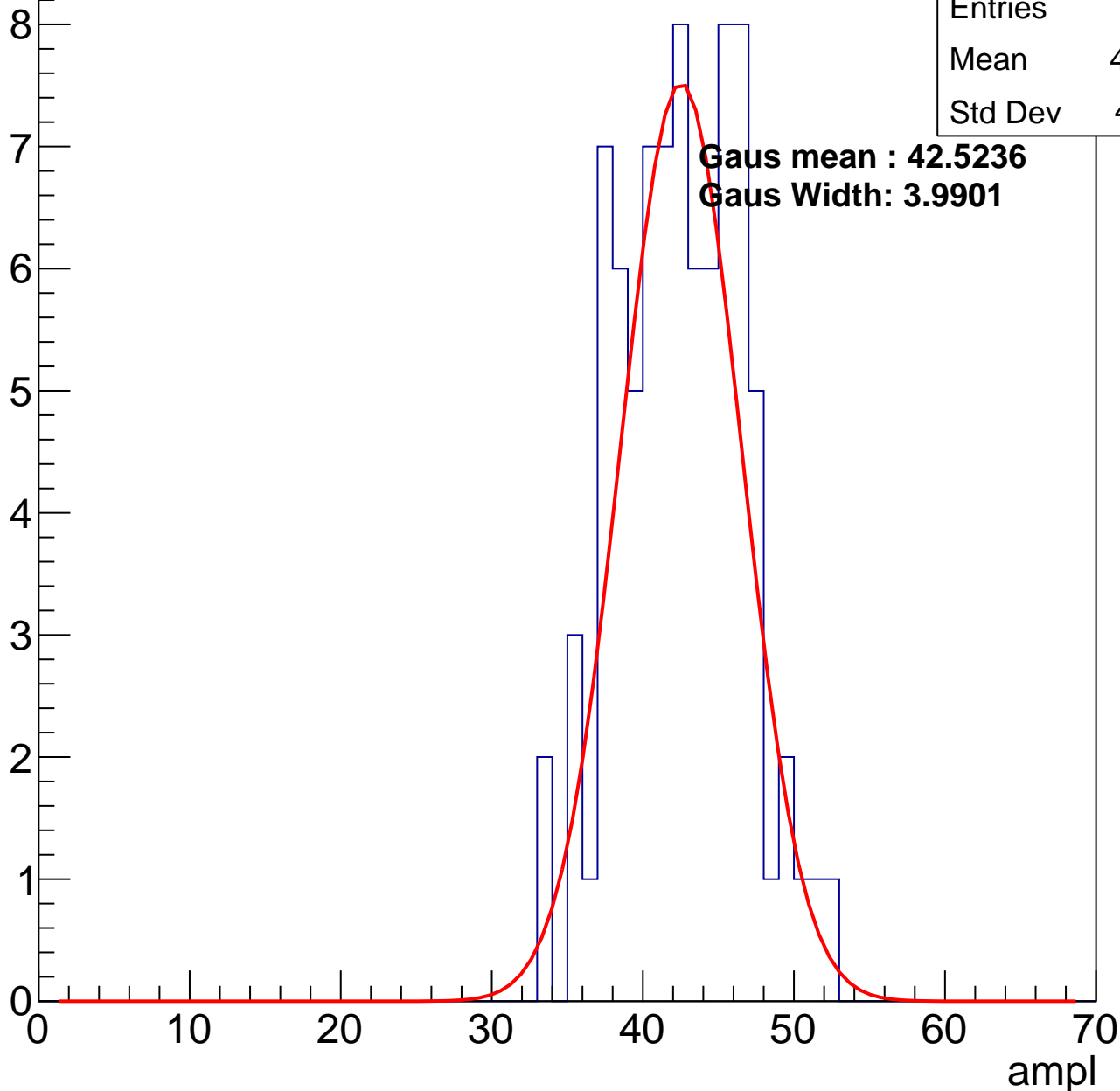
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	85
Mean	42.07
Std Dev	4.101

**Gaus mean : 42.5236**

**Gaus Width: 3.9901**

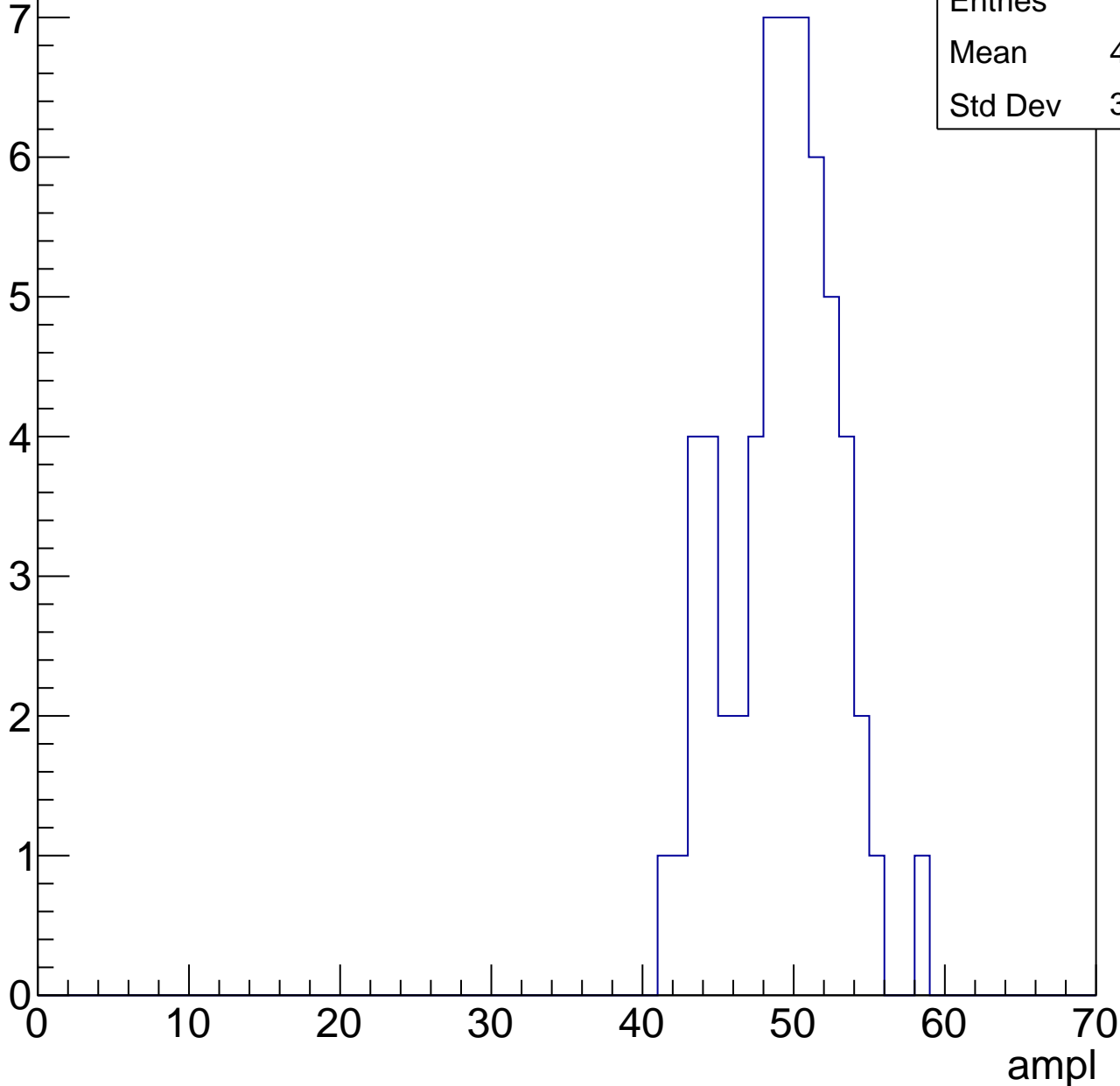


# B1L101S, U3-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	48.78
Std Dev	3.558

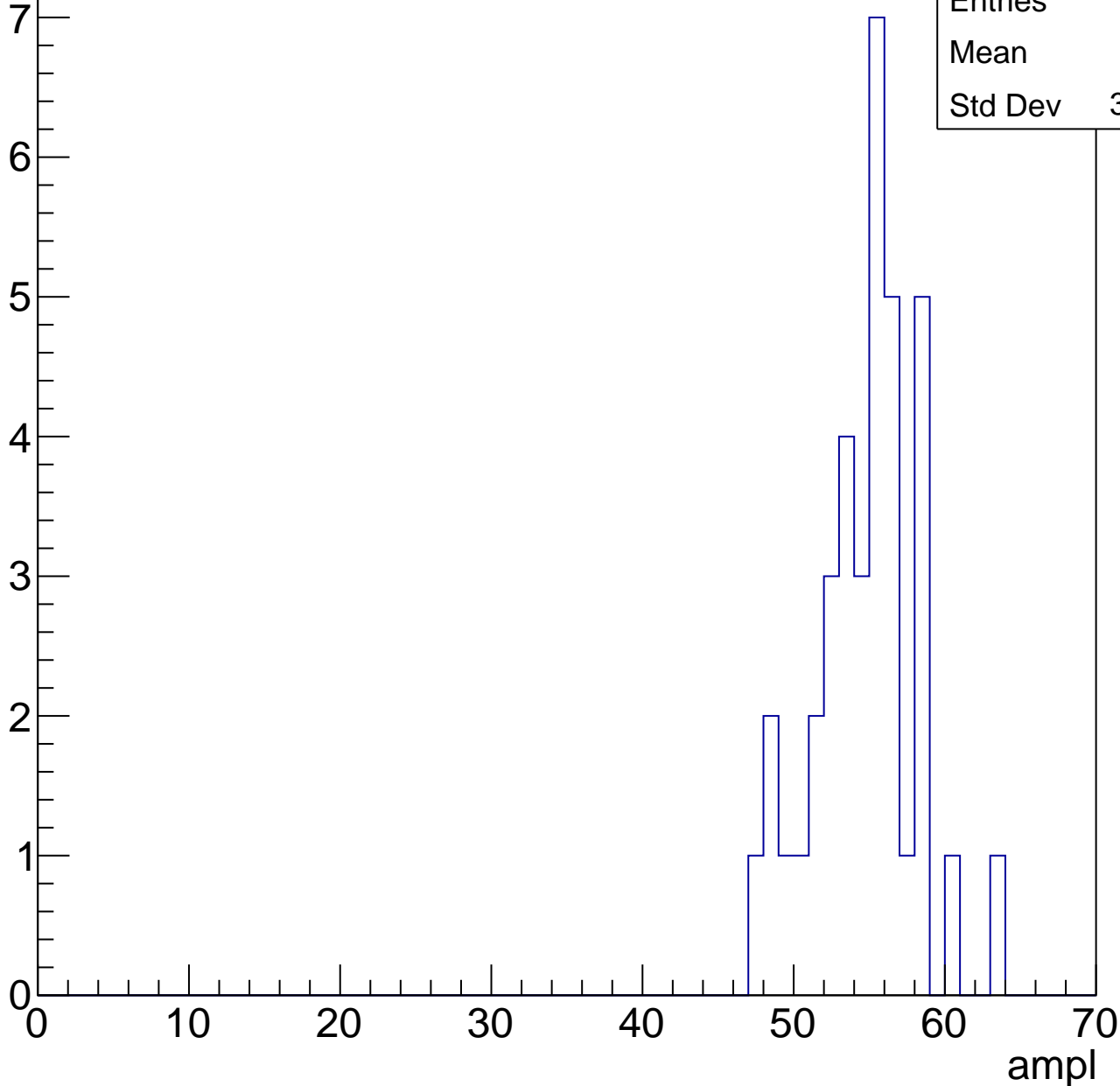


# B1L101S, U3-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	37
Mean	54.3
Std Dev	3.392



# B1L101S, U3-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

10

Entries 73

Mean 57.81

Std Dev 7.508

8

6

4

2

0

0

10

20

30

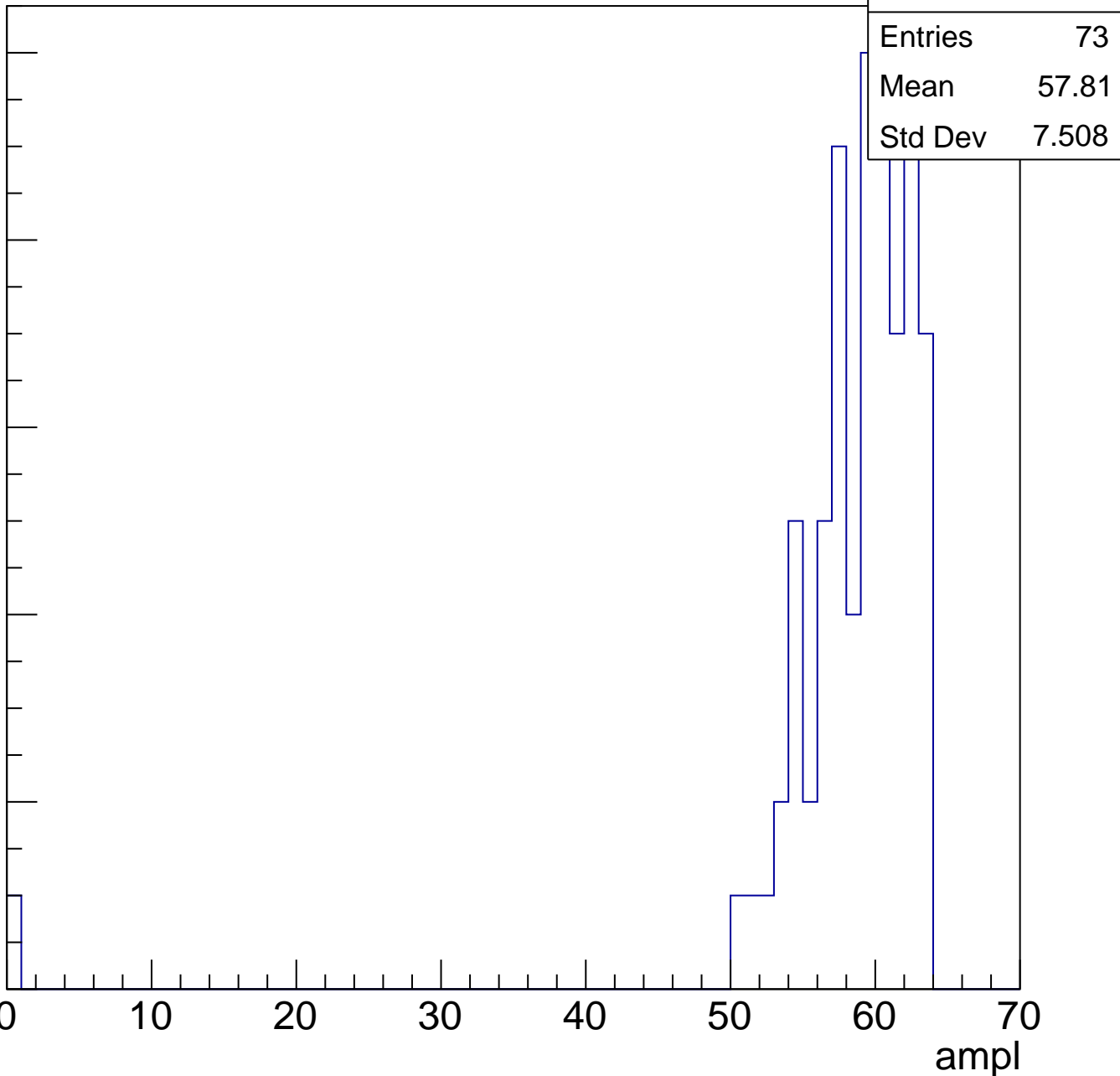
40

50

60

70

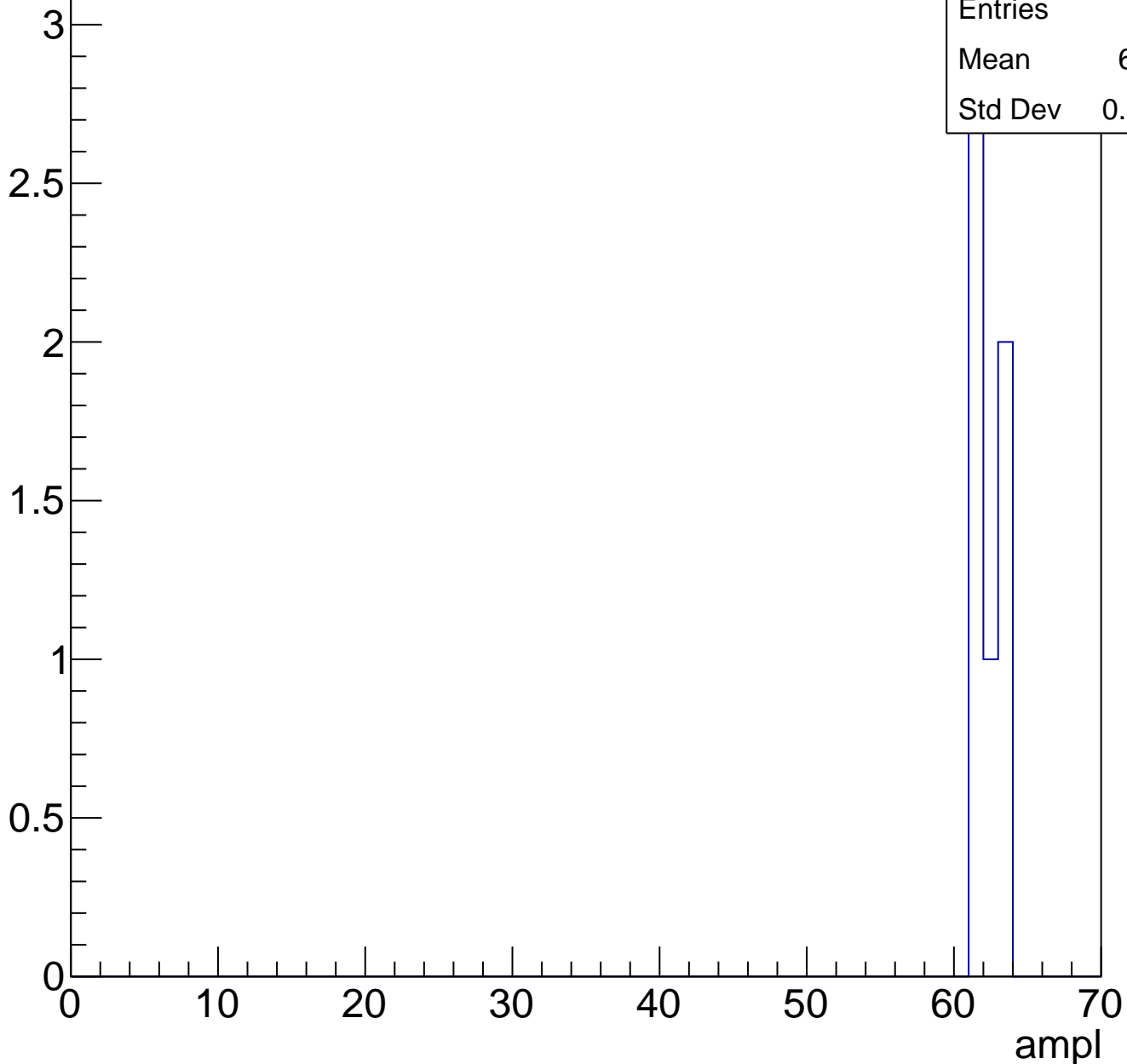
ampl



# B1L101S, U3-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch29, adc0

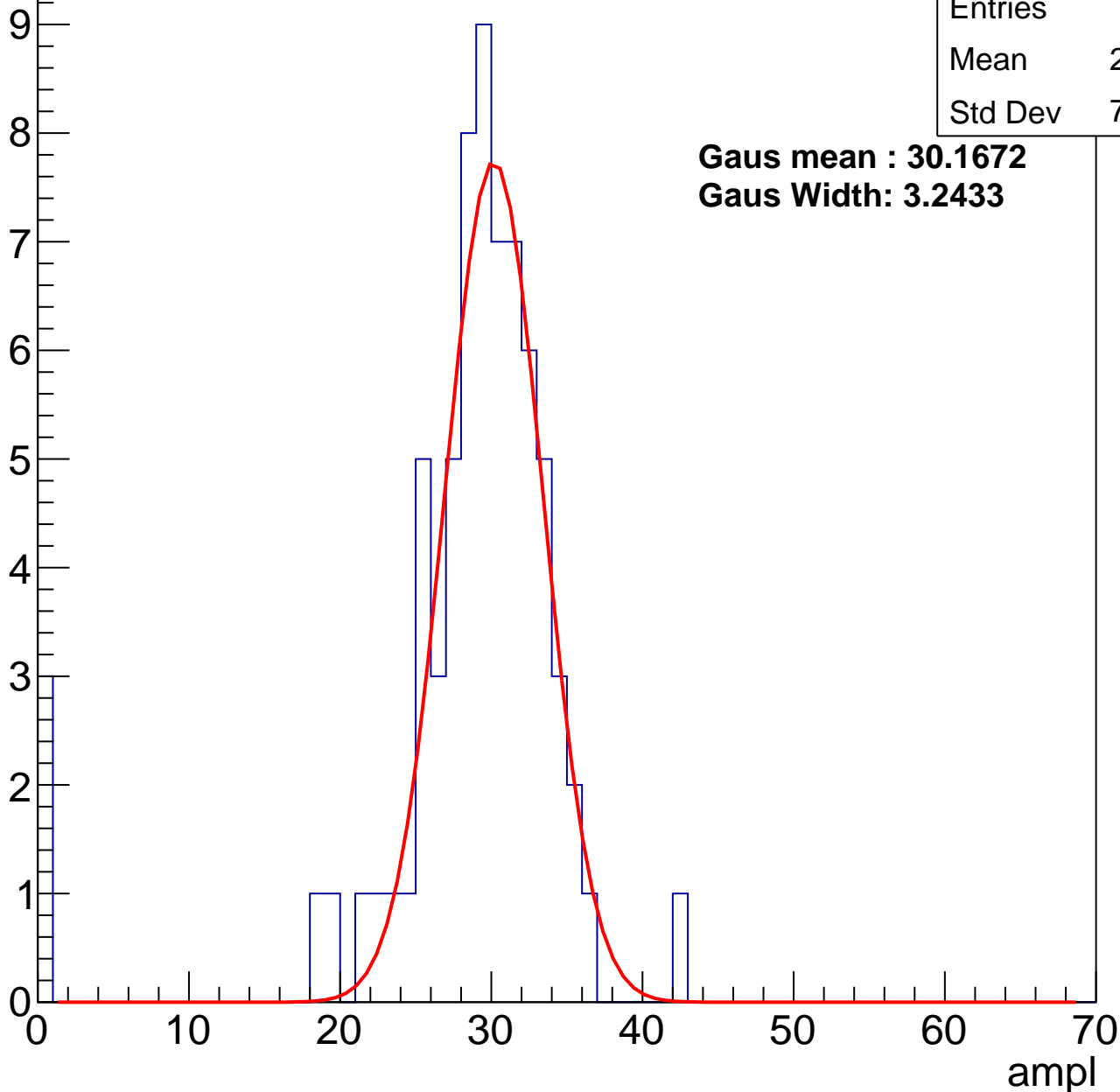
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	27.94
Std Dev	7.029

**Gaus mean : 30.1672**

**Gaus Width: 3.2433**



# B1L101S, U3-ch29, adc1

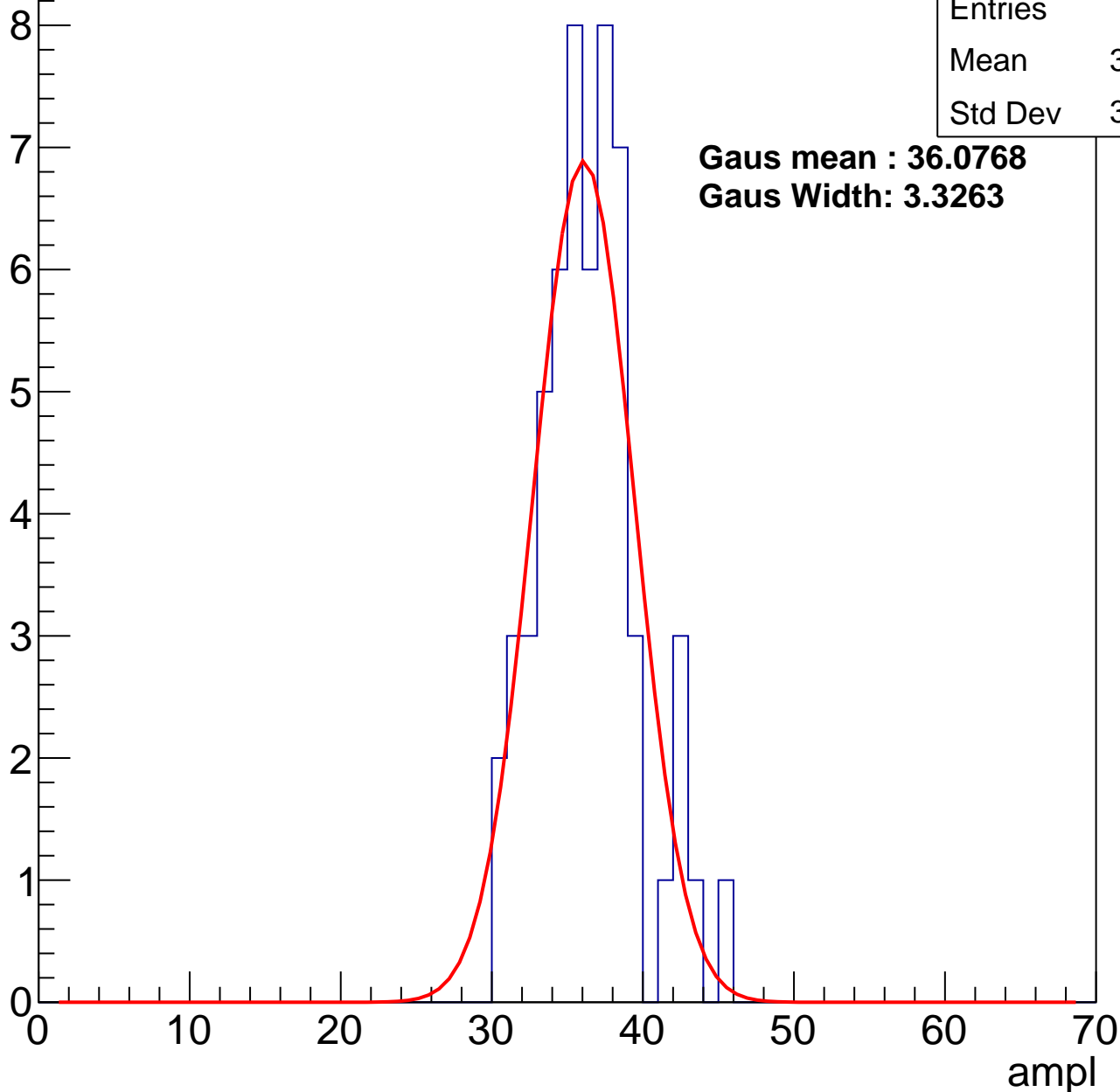
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	35.93
Std Dev	3.238

**Gaus mean : 36.0768**

**Gaus Width: 3.3263**



# B1L101S, U3-ch29, adc2

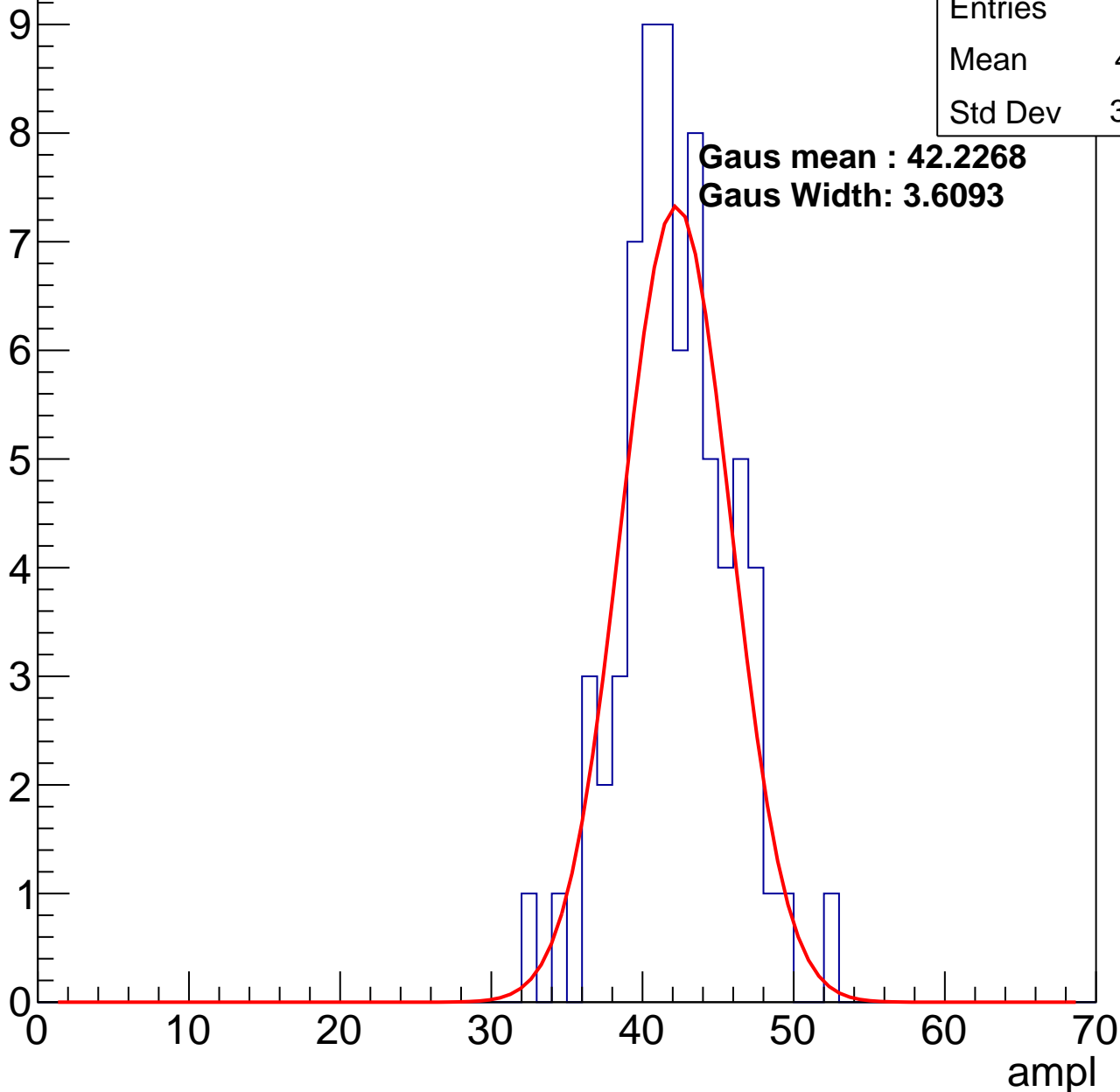
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	41.81
Std Dev	3.595

**Gaus mean : 42.2268**

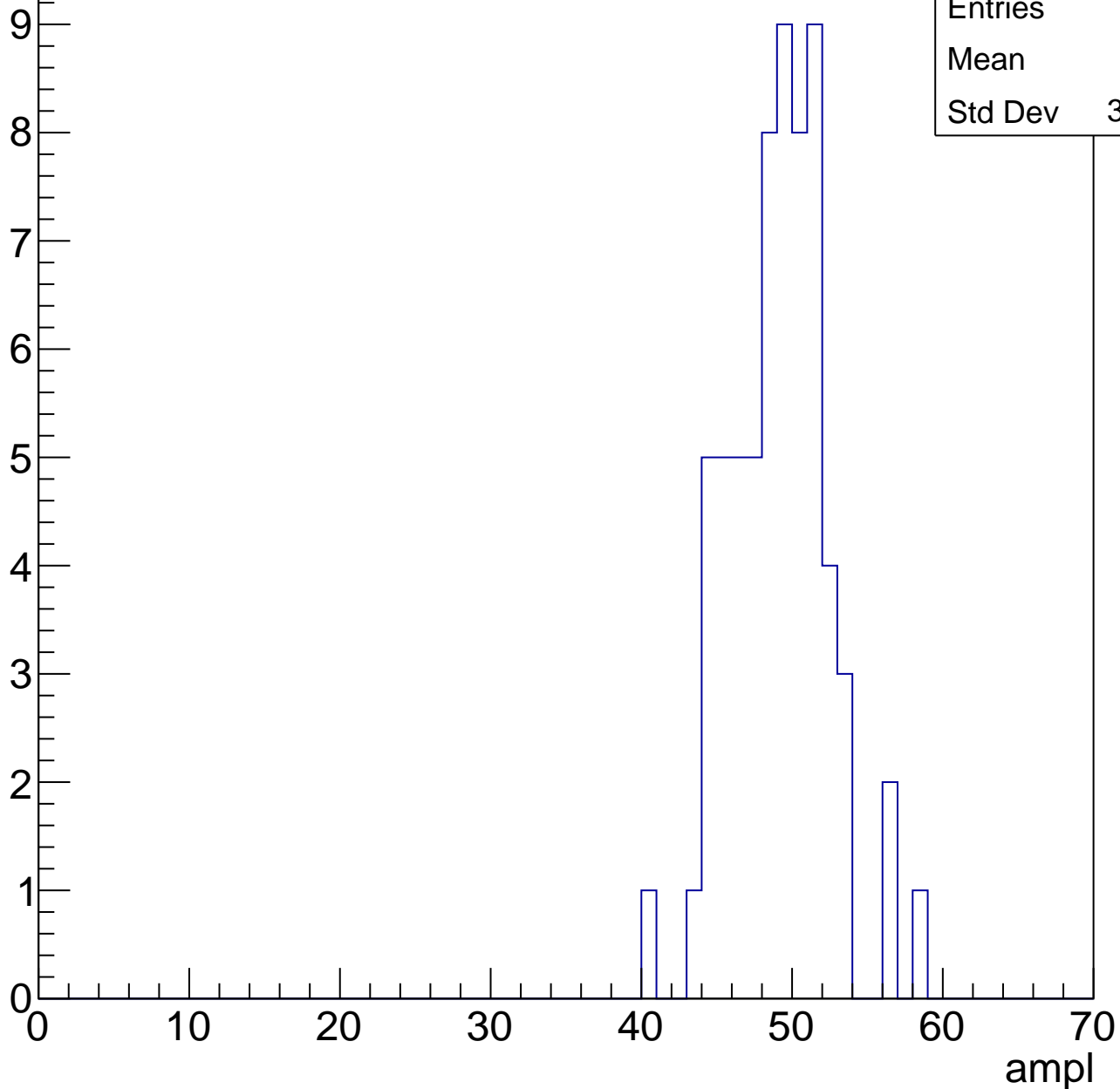
**Gaus Width: 3.6093**



# B1L101S, U3-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

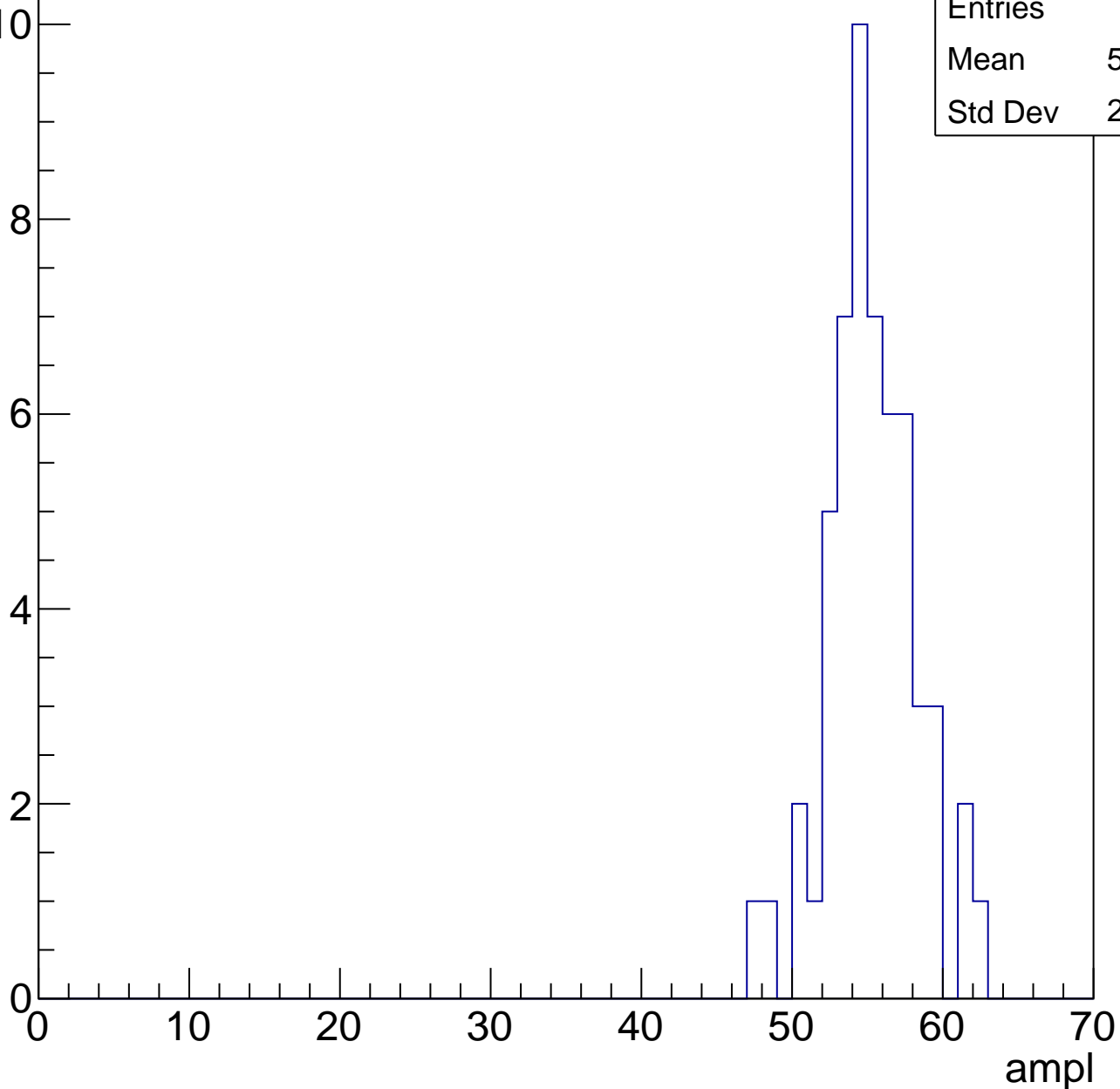


# B1L101S, U3-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	54.82
Std Dev	2.973

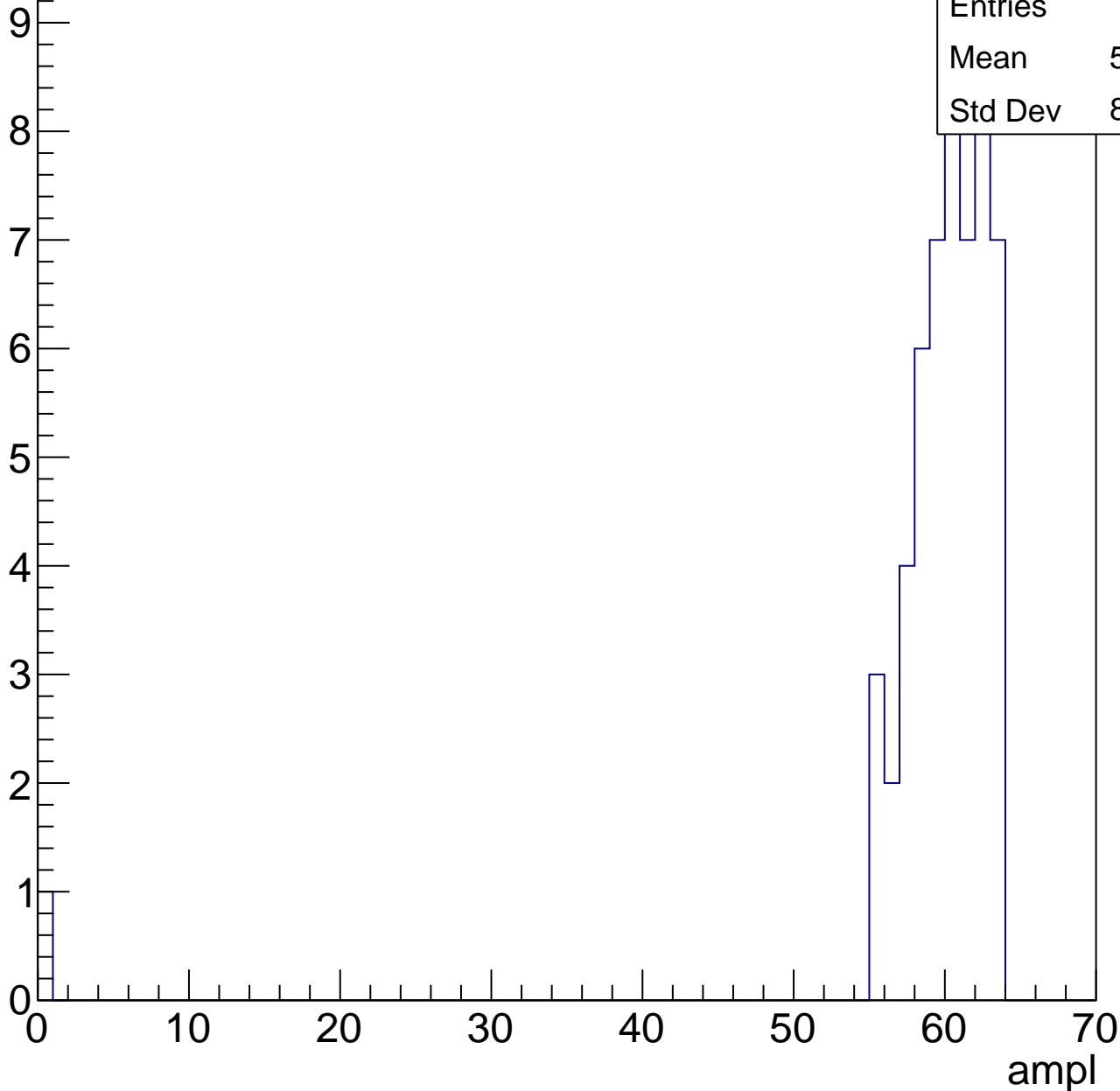


# B1L101S, U3-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

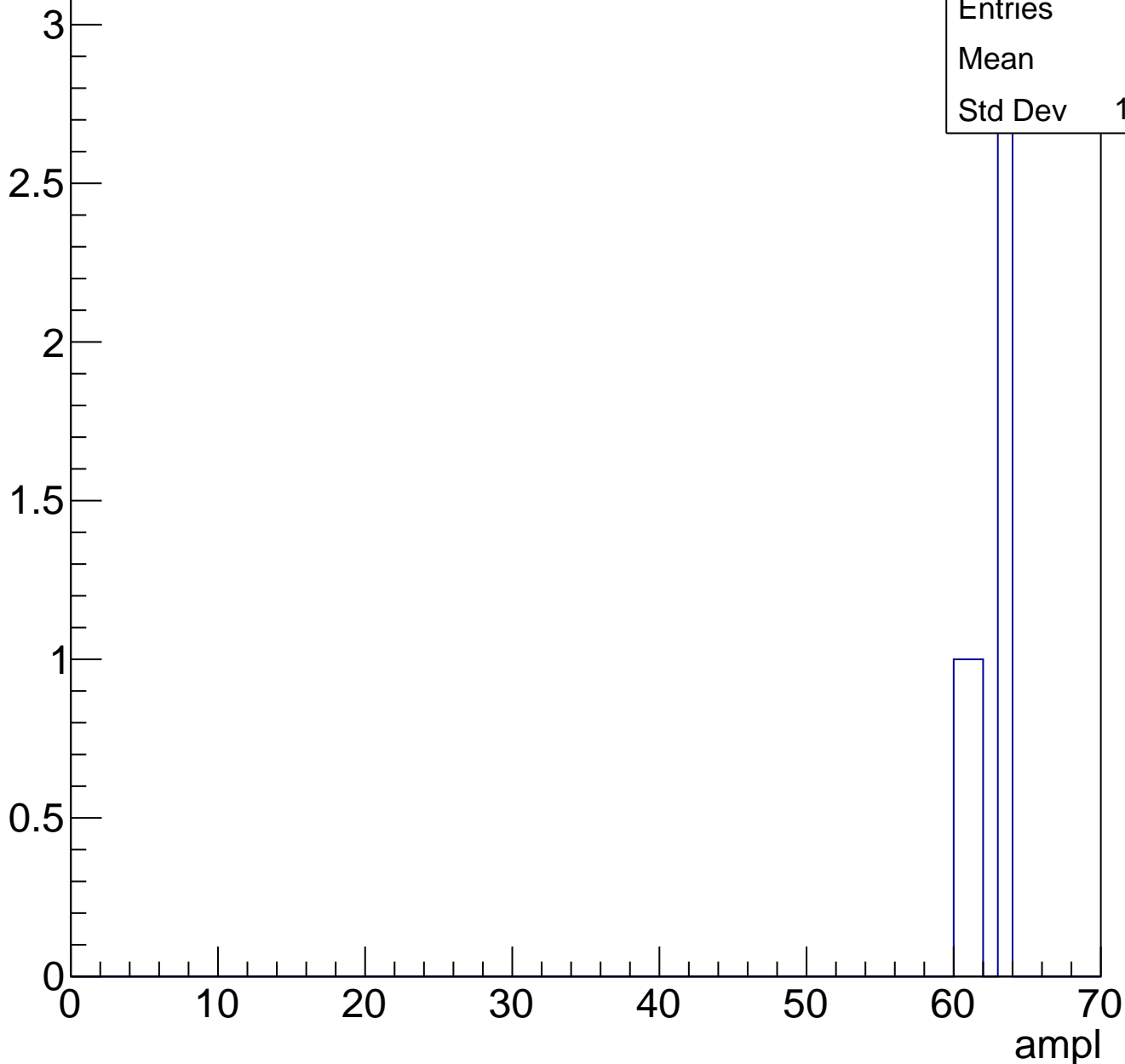
Entries	55
Mean	58.76
Std Dev	8.308



# B1L101S, U3-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U3-ch30, adc0

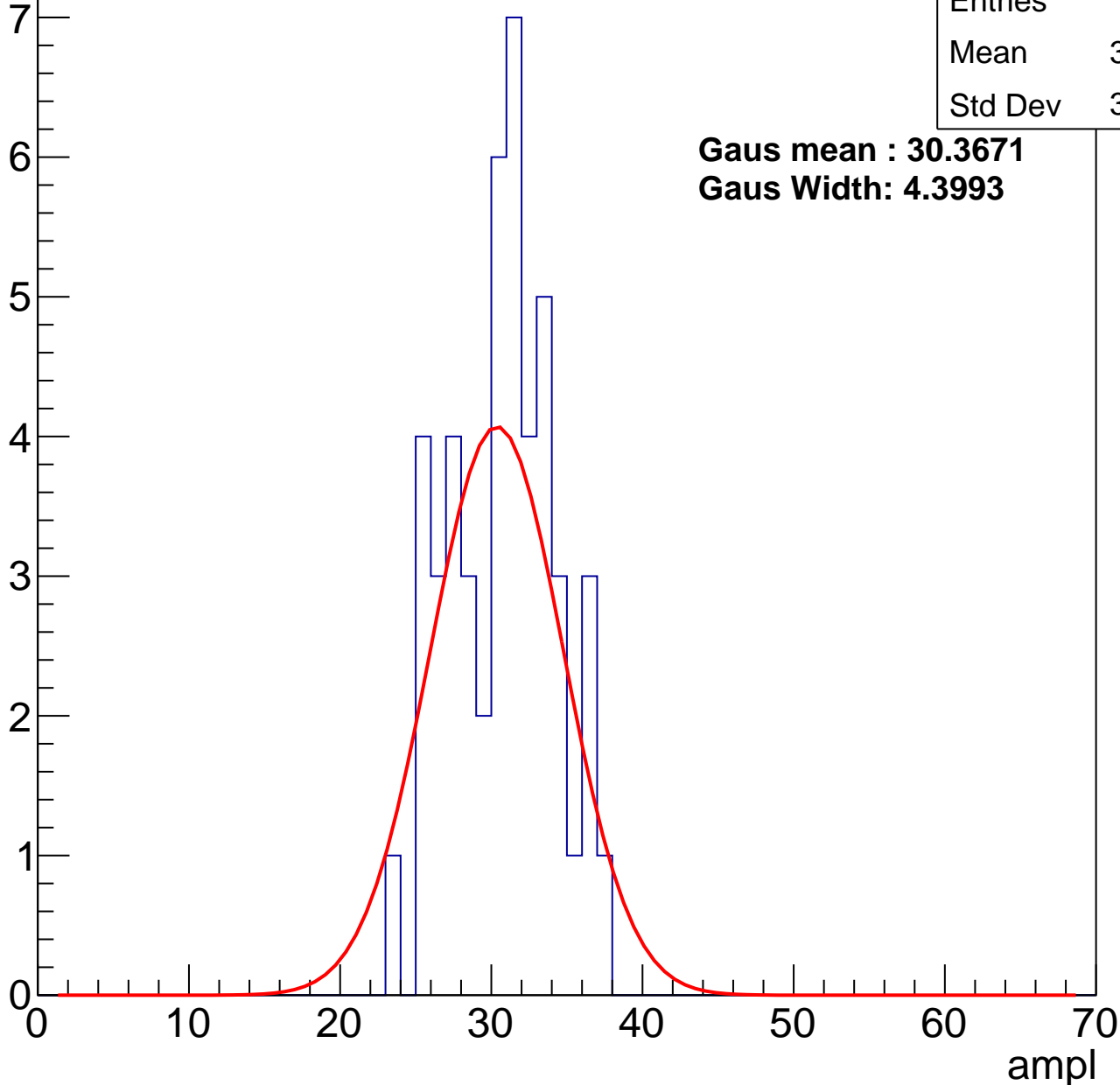
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	30.28
Std Dev	3.394

**Gaus mean : 30.3671**

**Gaus Width: 4.3993**



# B1L101S, U3-ch30, adc1

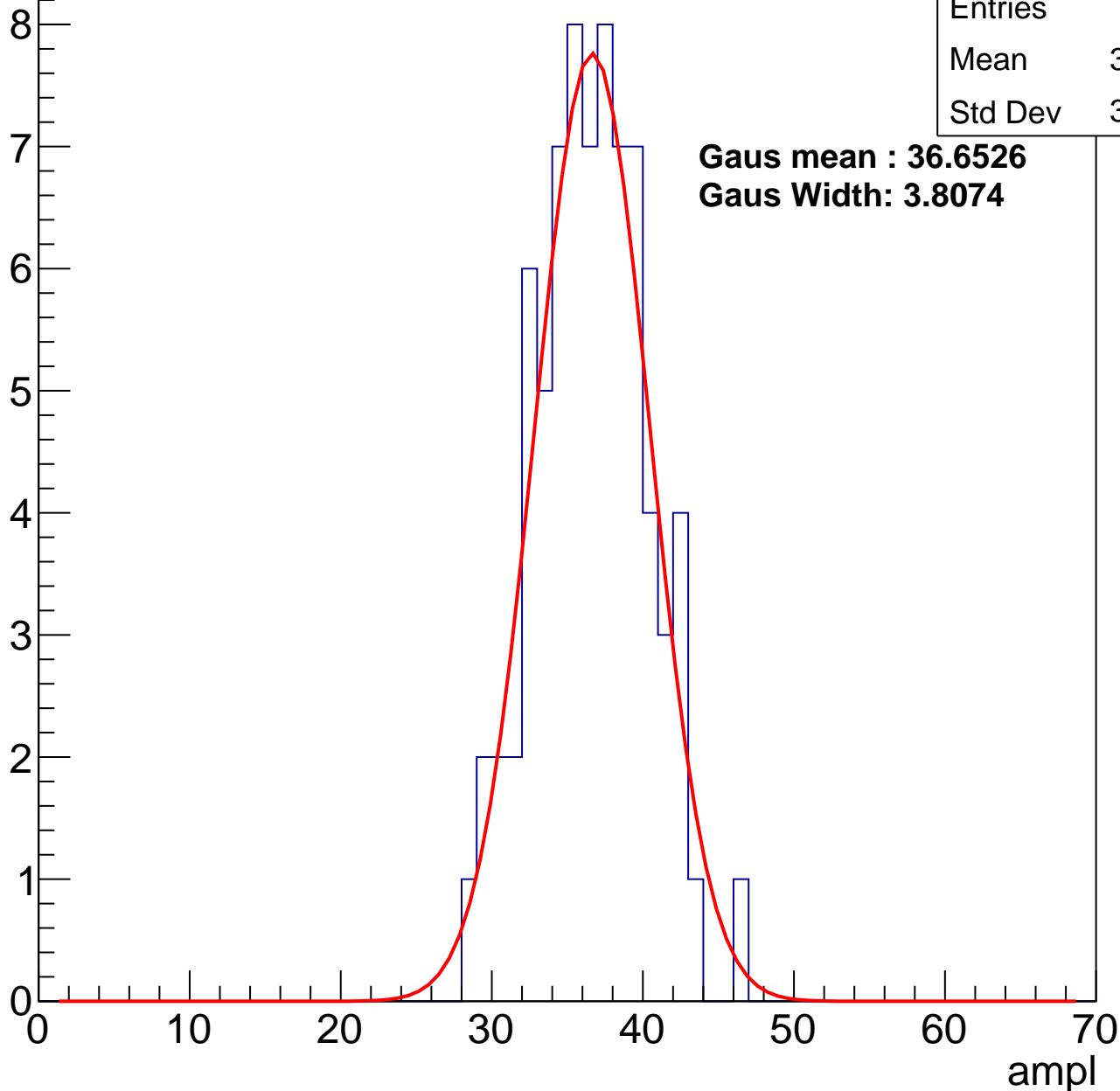
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	36.13
Std Dev	3.634

**Gaus mean : 36.6526**

**Gaus Width: 3.8074**



# B1L101S, U3-ch30, adc2

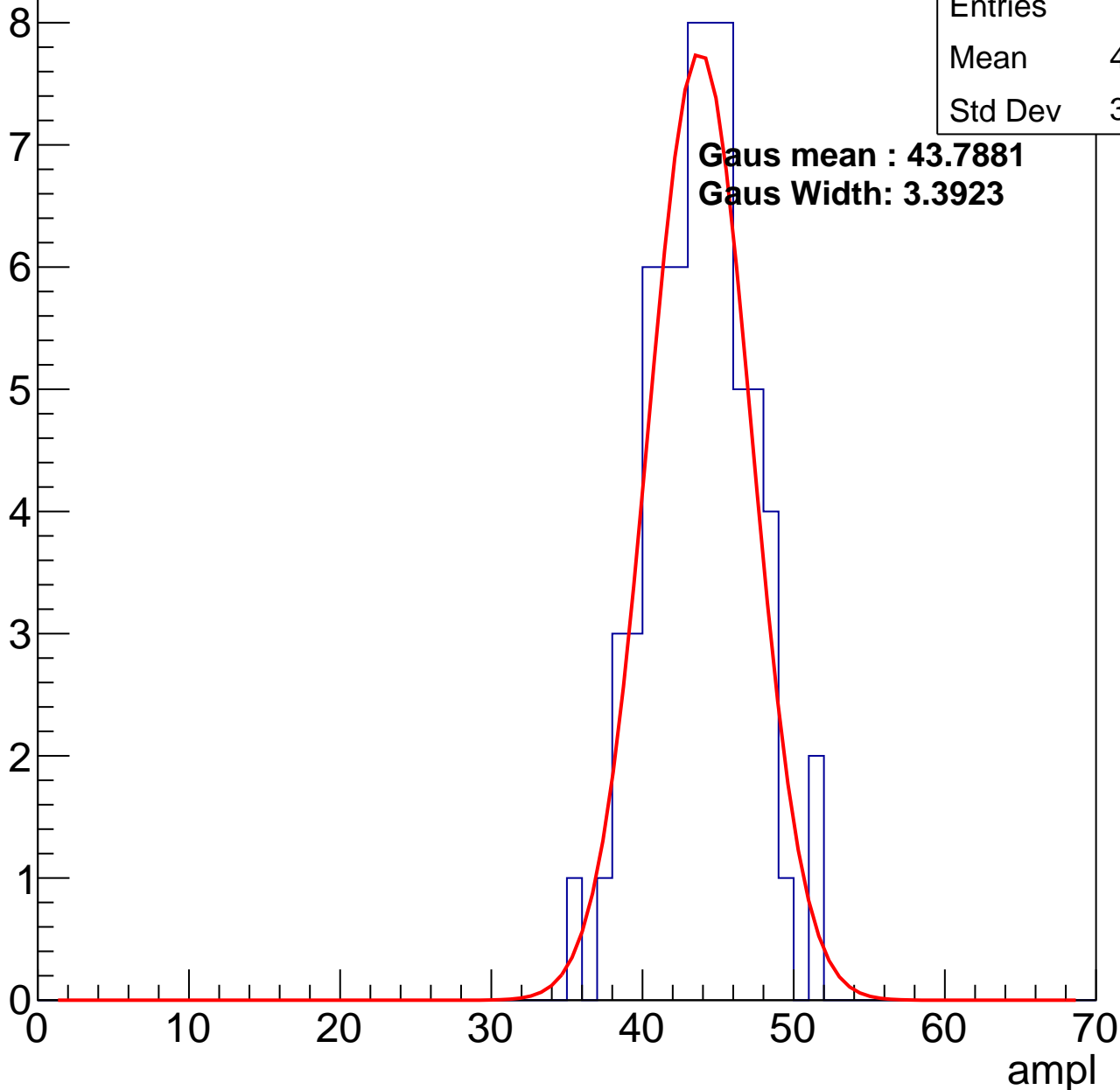
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	43.36
Std Dev	3.295

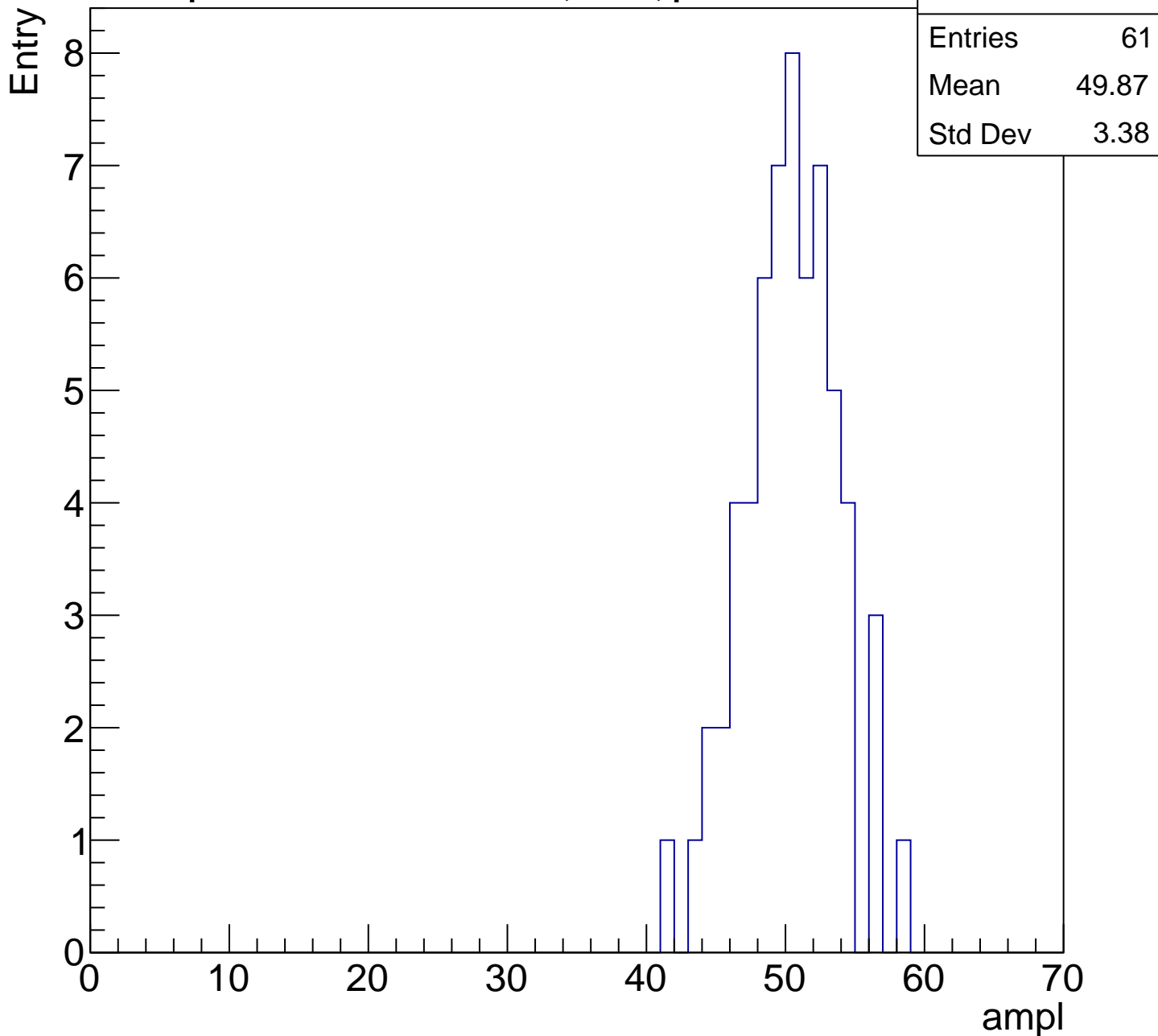
**Gaus mean : 43.7881**

**Gaus Width: 3.3923**



# B1L101S, U3-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

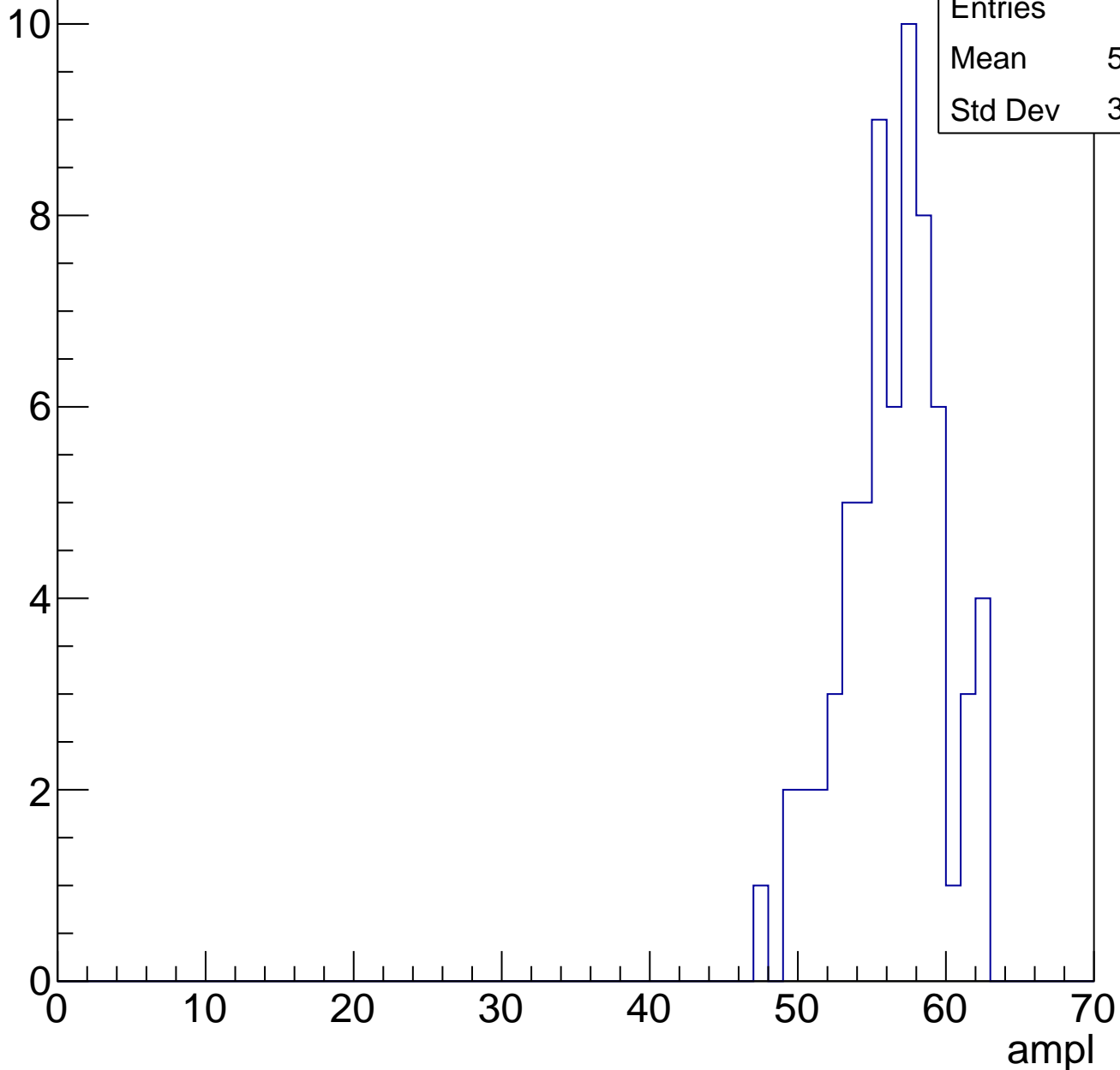


# B1L101S, U3-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	67
Mean	55.94
Std Dev	3.354

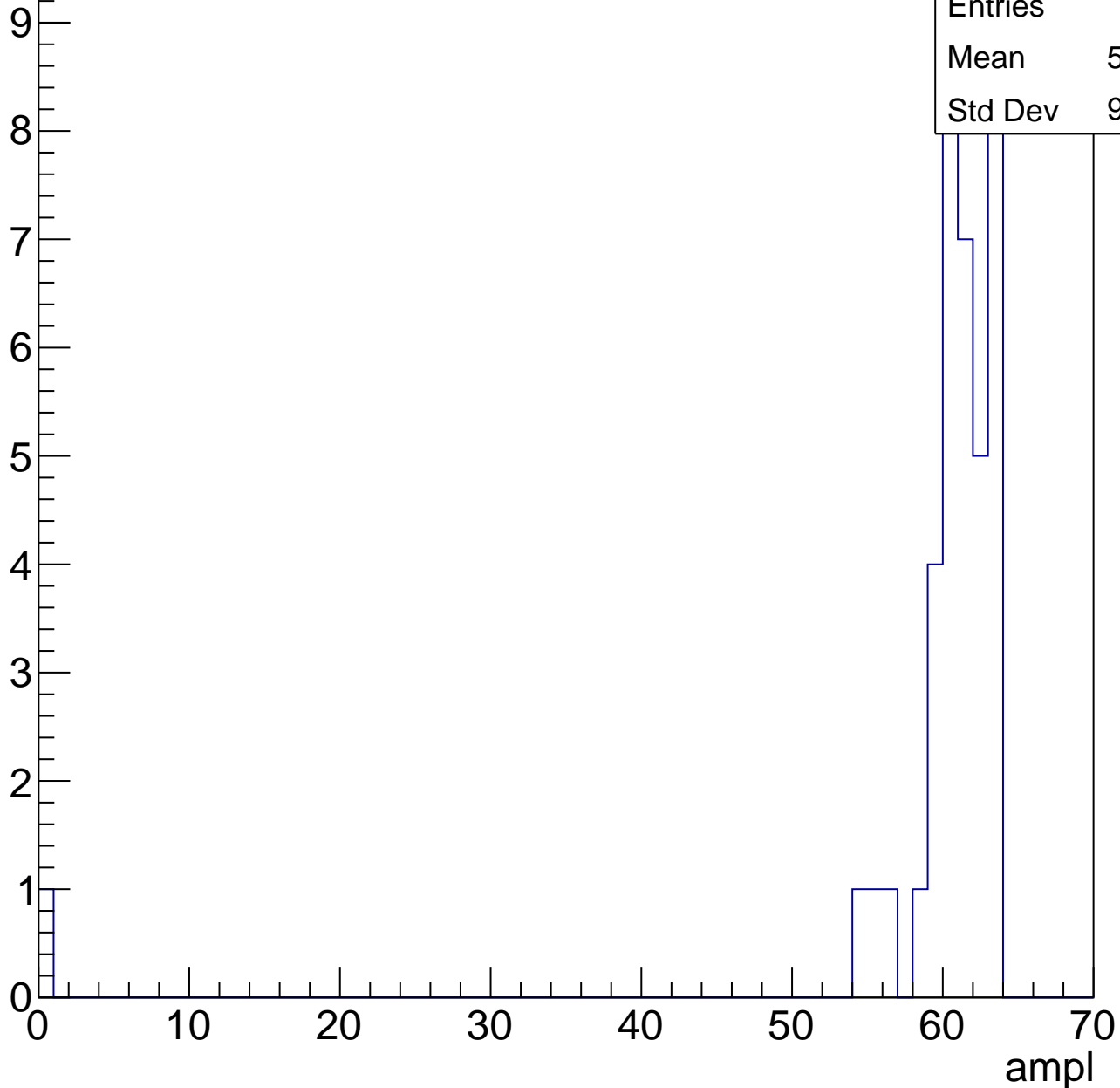
Entry



# B1L101S, U3-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

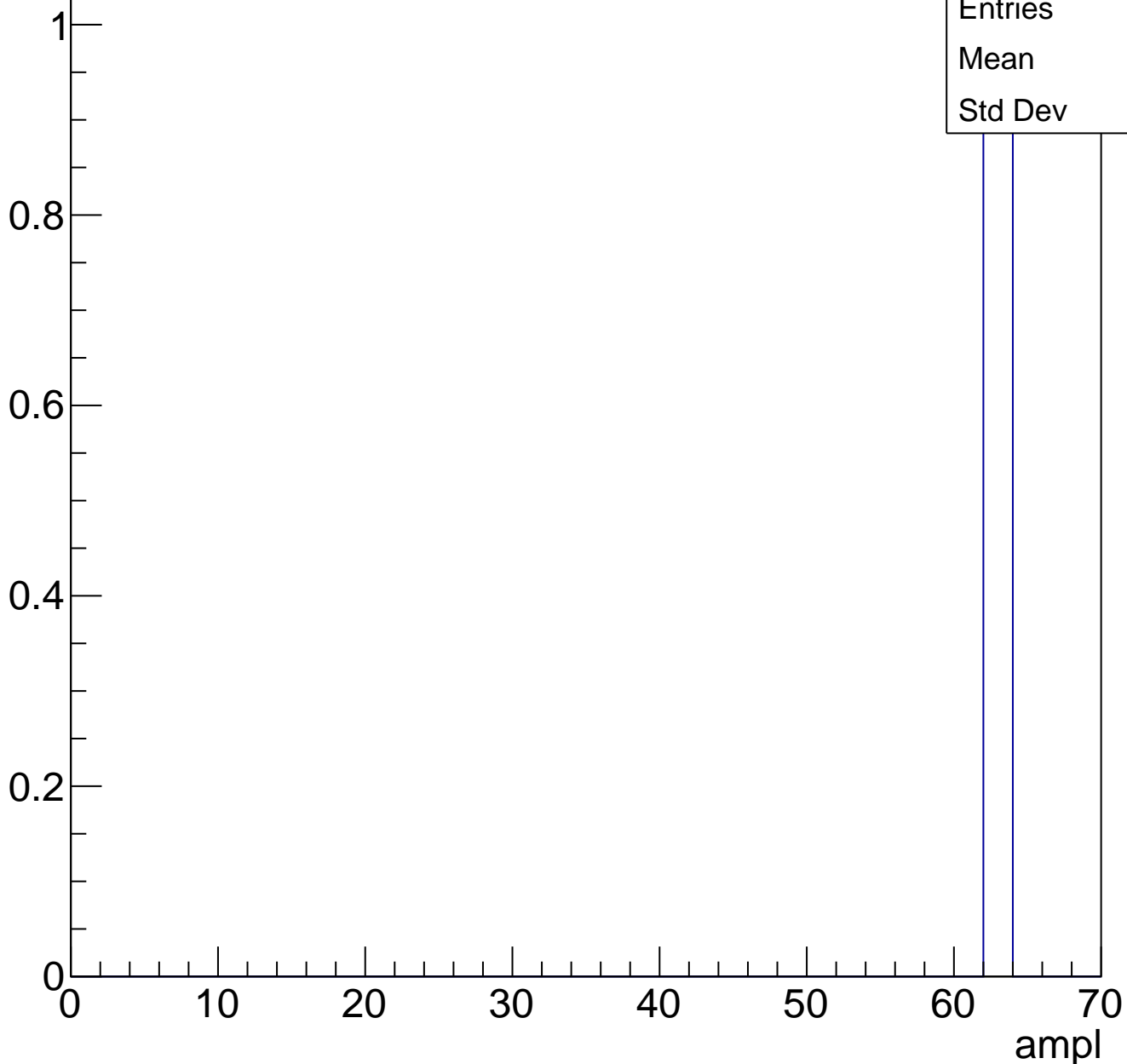
Entry



# B1L101S, U3-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch31, adc0

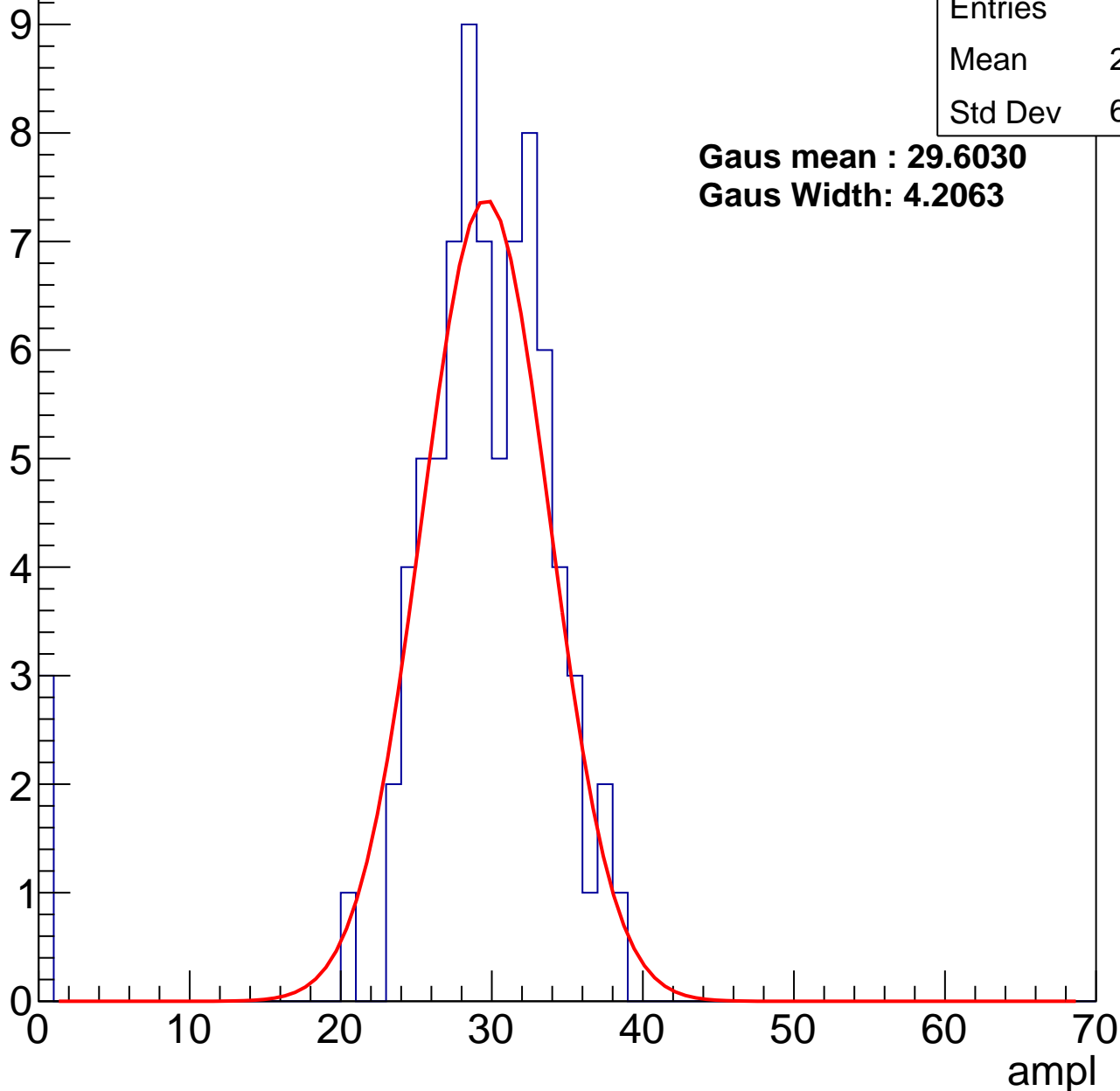
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	28.39
Std Dev	6.685

**Gaus mean : 29.6030**

**Gaus Width: 4.2063**



# B1L101S, U3-ch31, adc1

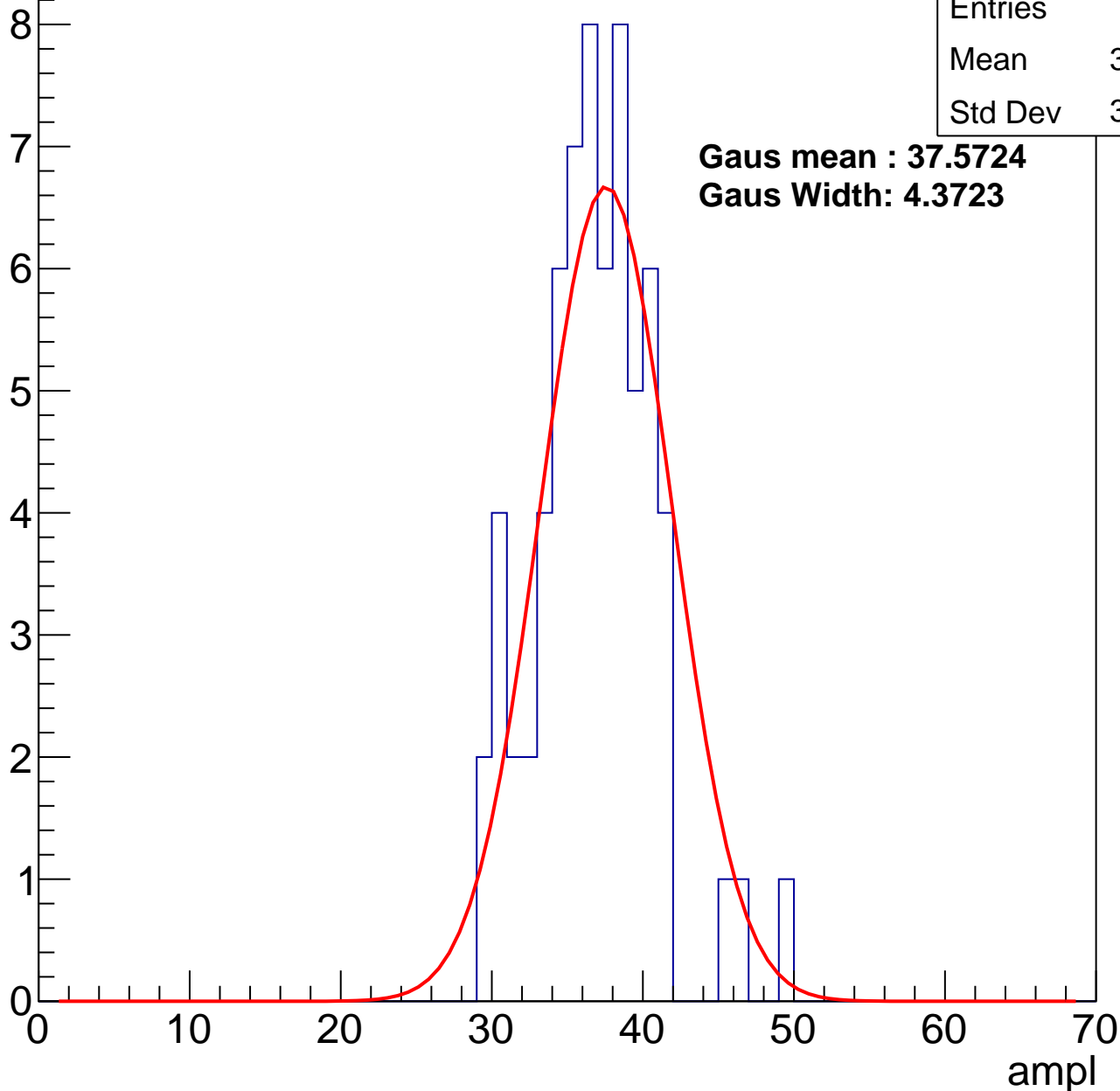
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	36.39
Std Dev	3.882

**Gaus mean : 37.5724**

**Gaus Width: 4.3723**



# B1L101S, U3-ch31, adc2

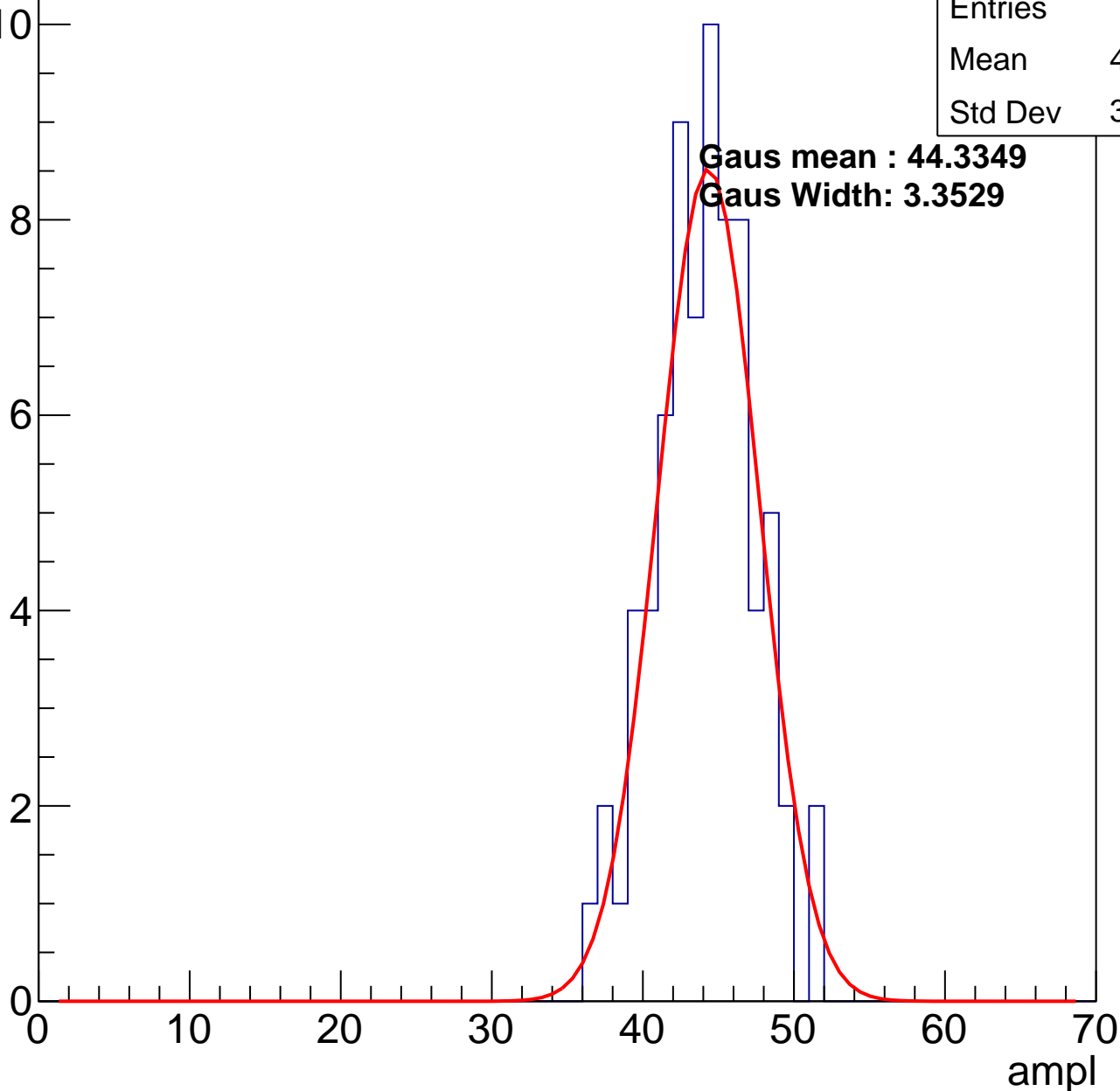
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	43.63
Std Dev	3.212

**Gaus mean : 44.3349**

**Gaus Width: 3.3529**

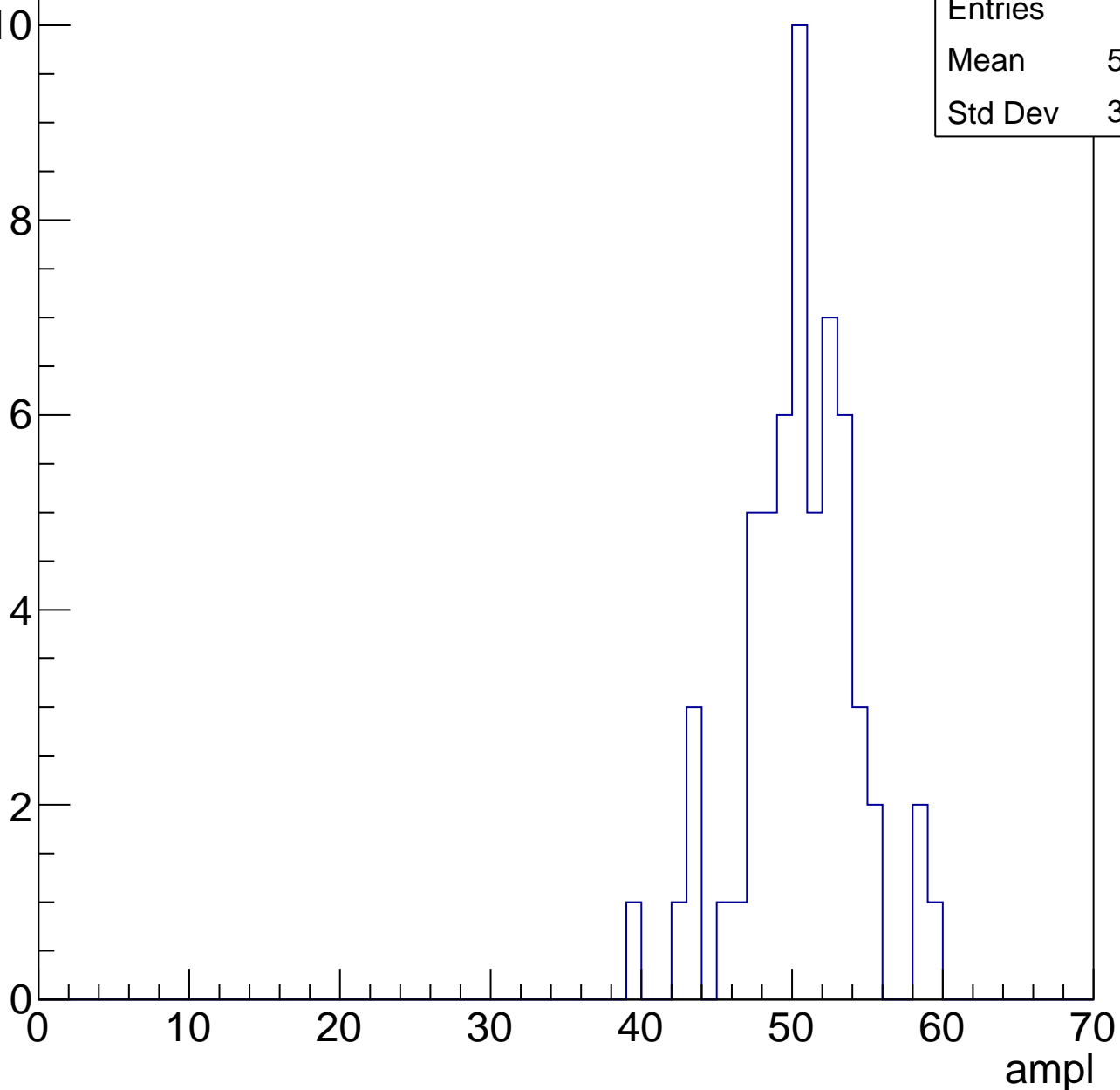


# B1L101S, U3-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	50.07
Std Dev	3.768

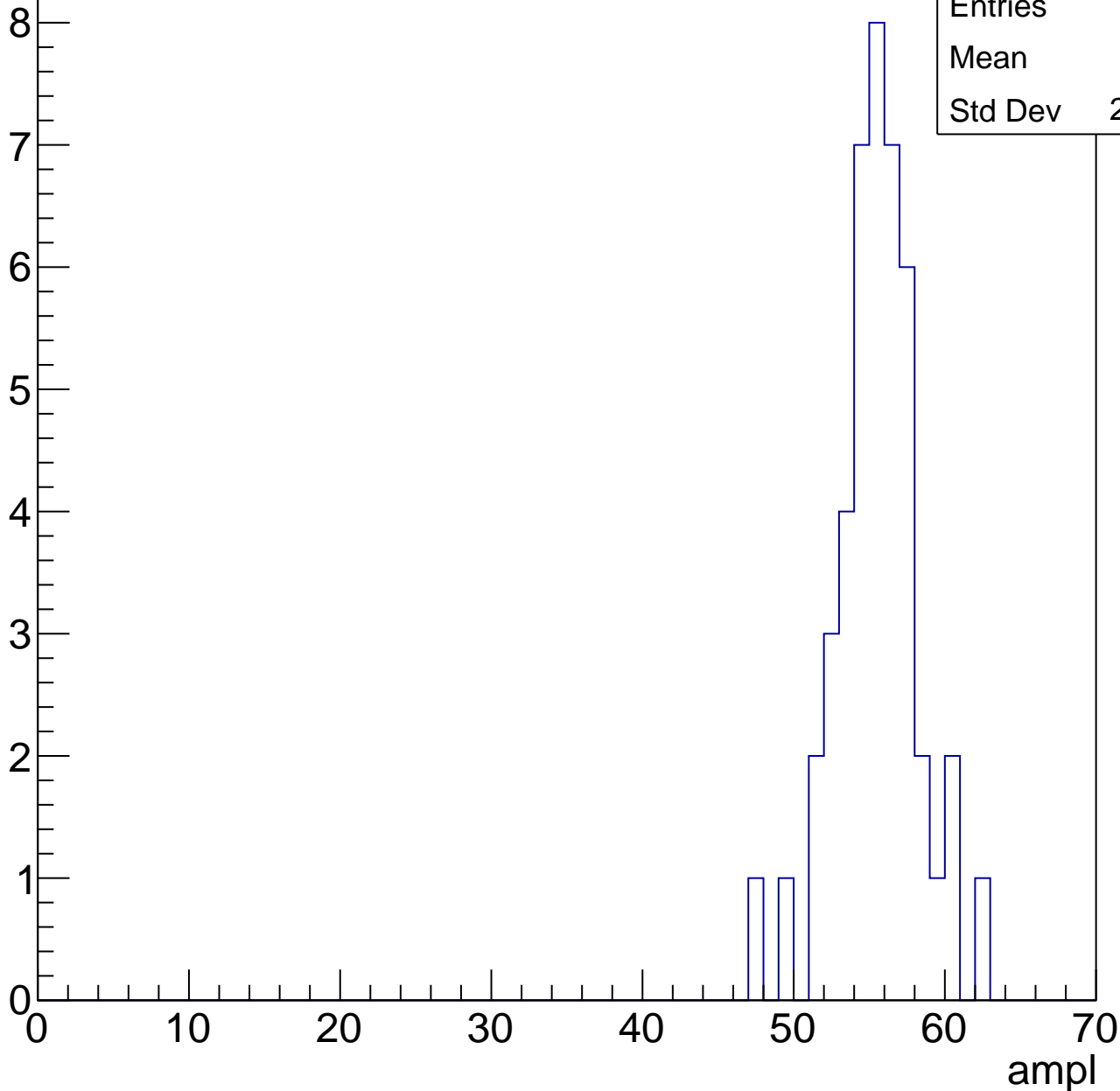


# B1L101S, U3-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	55
Std Dev	2.773

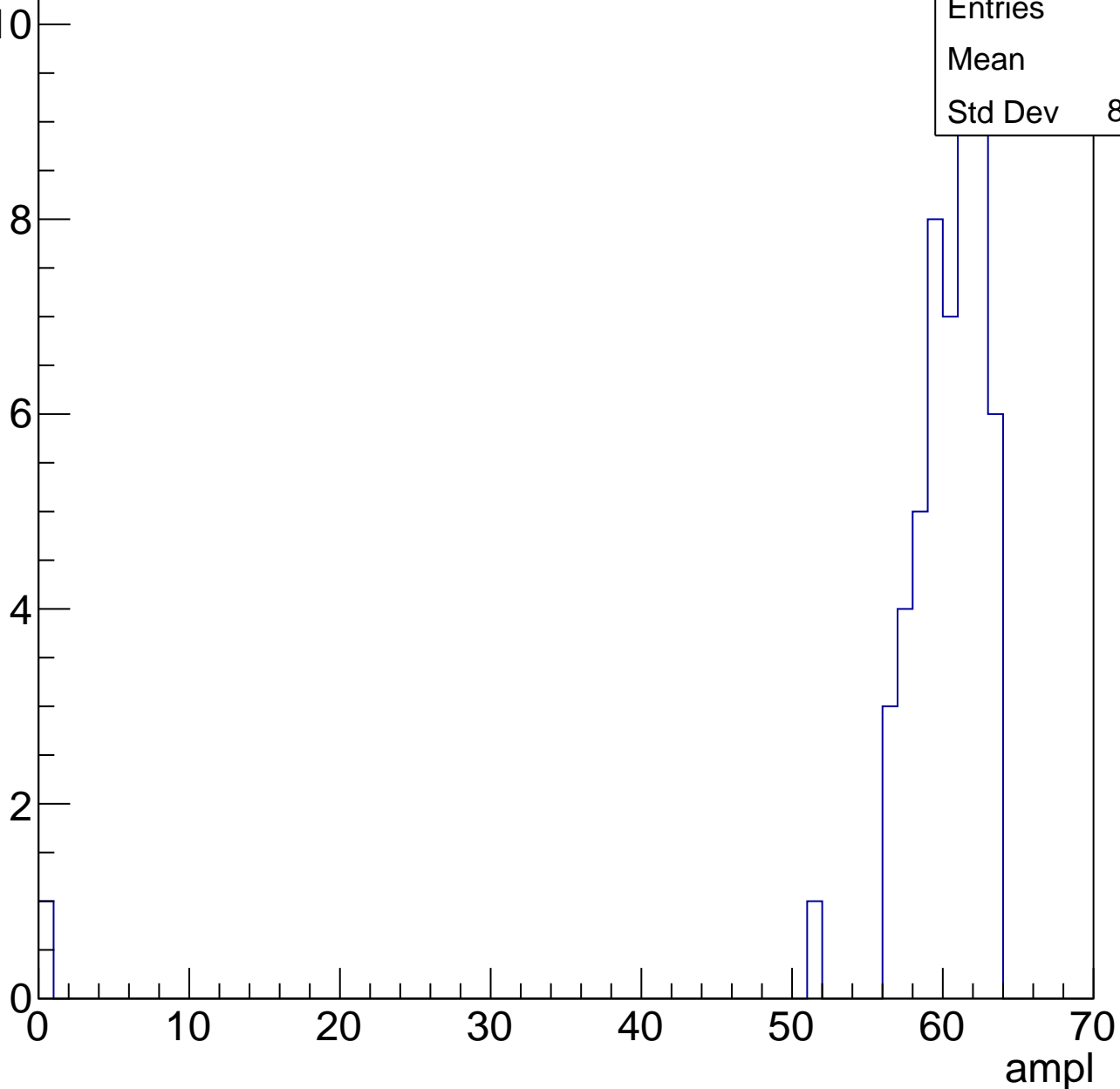


# B1L101S, U3-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

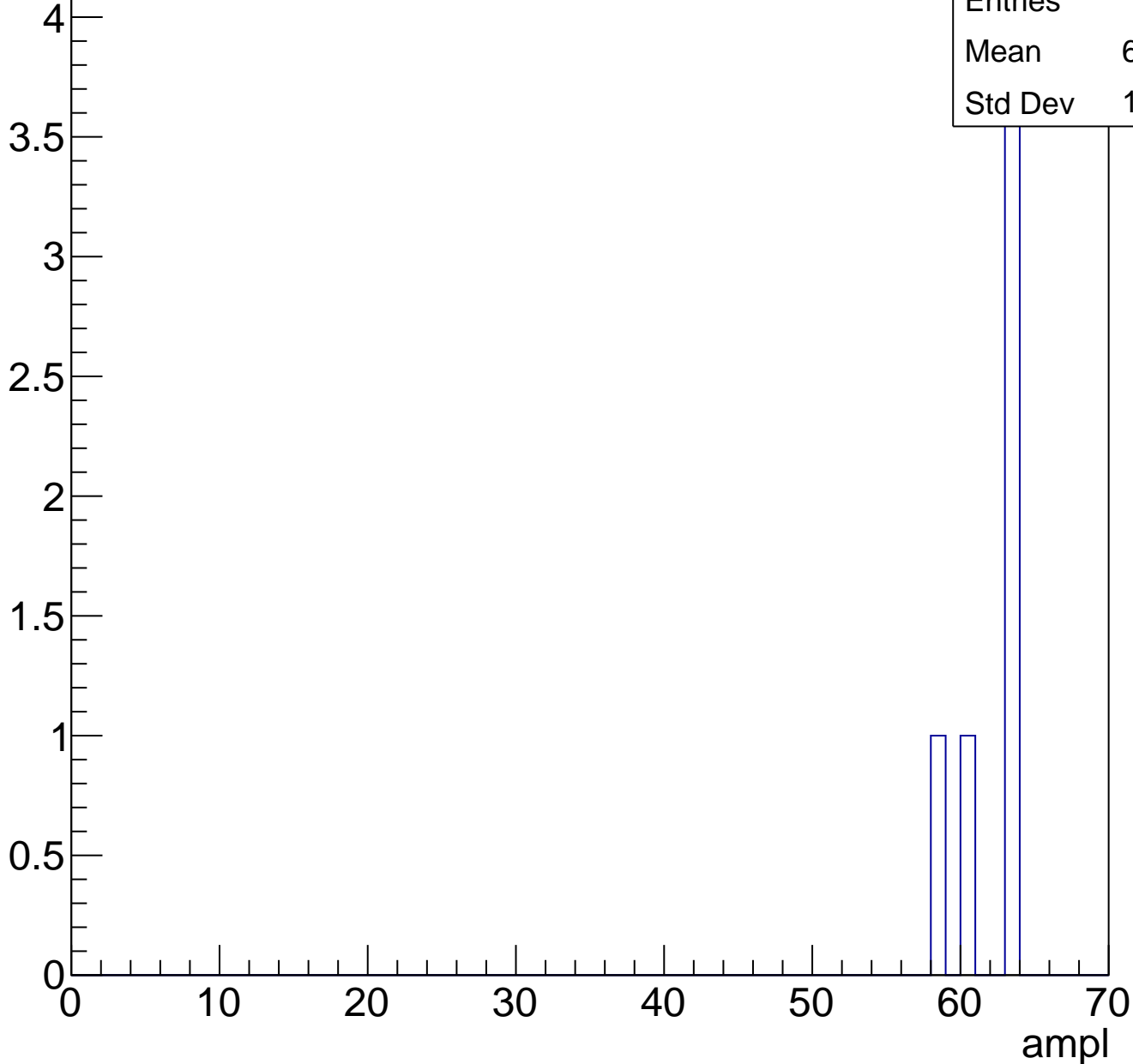
Entries	54
Mean	58.8
Std Dev	8.405



# B1L101S, U3-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

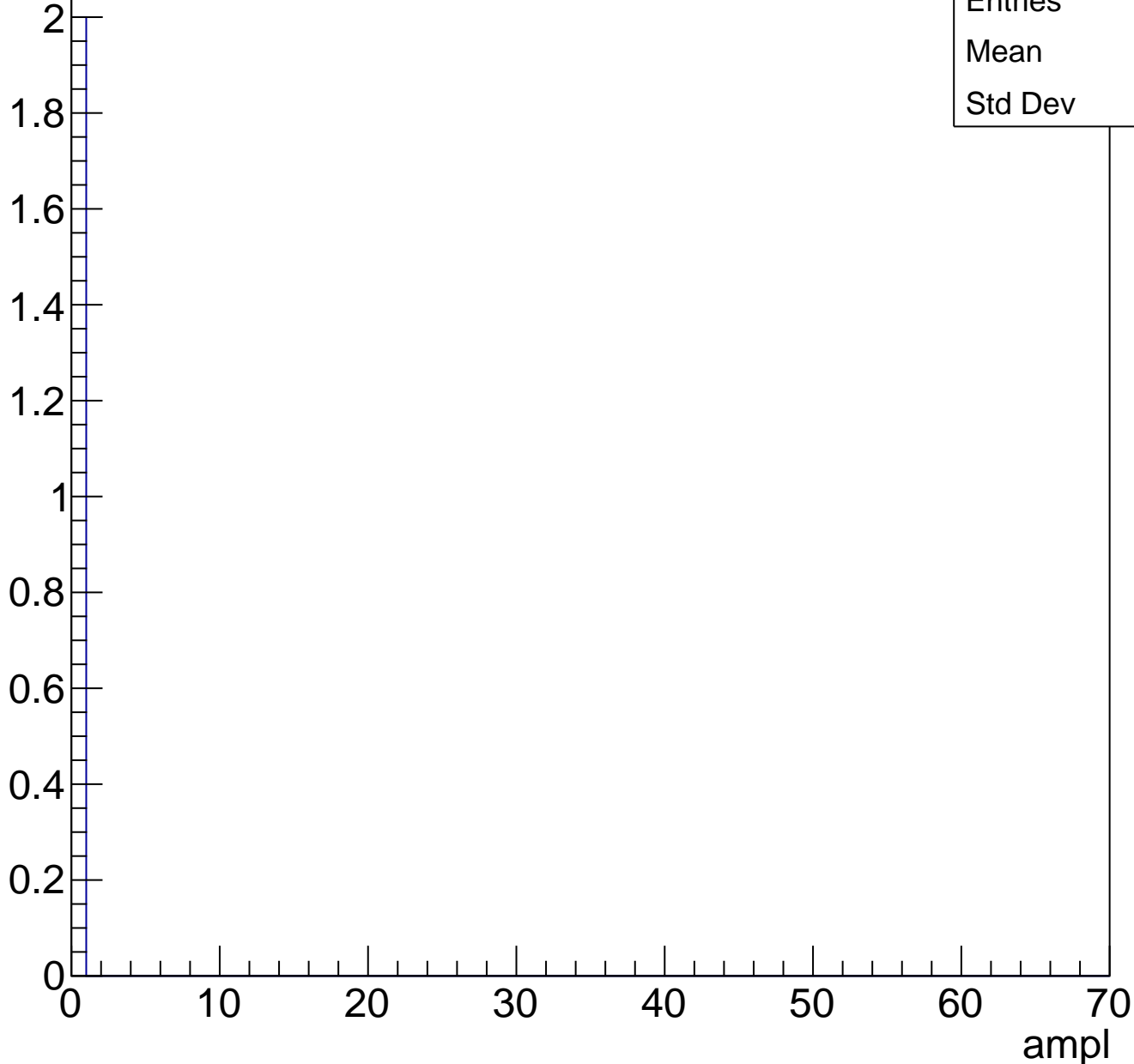




# B1L101S, U3-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch32, adc0

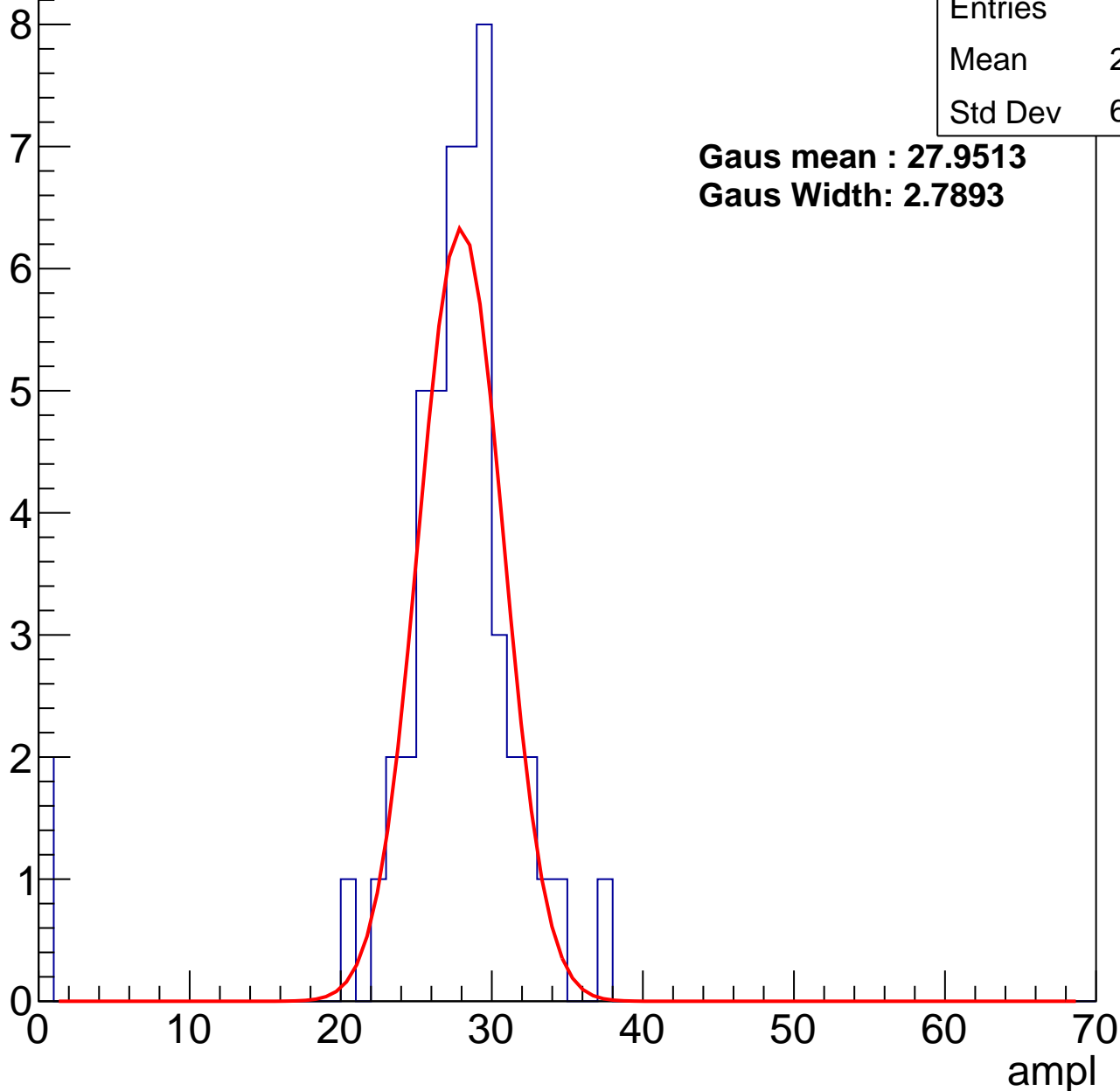
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	26.56
Std Dev	6.213

**Gaus mean : 27.9513**

**Gaus Width: 2.7893**



# B1L101S, U3-ch32, adc1

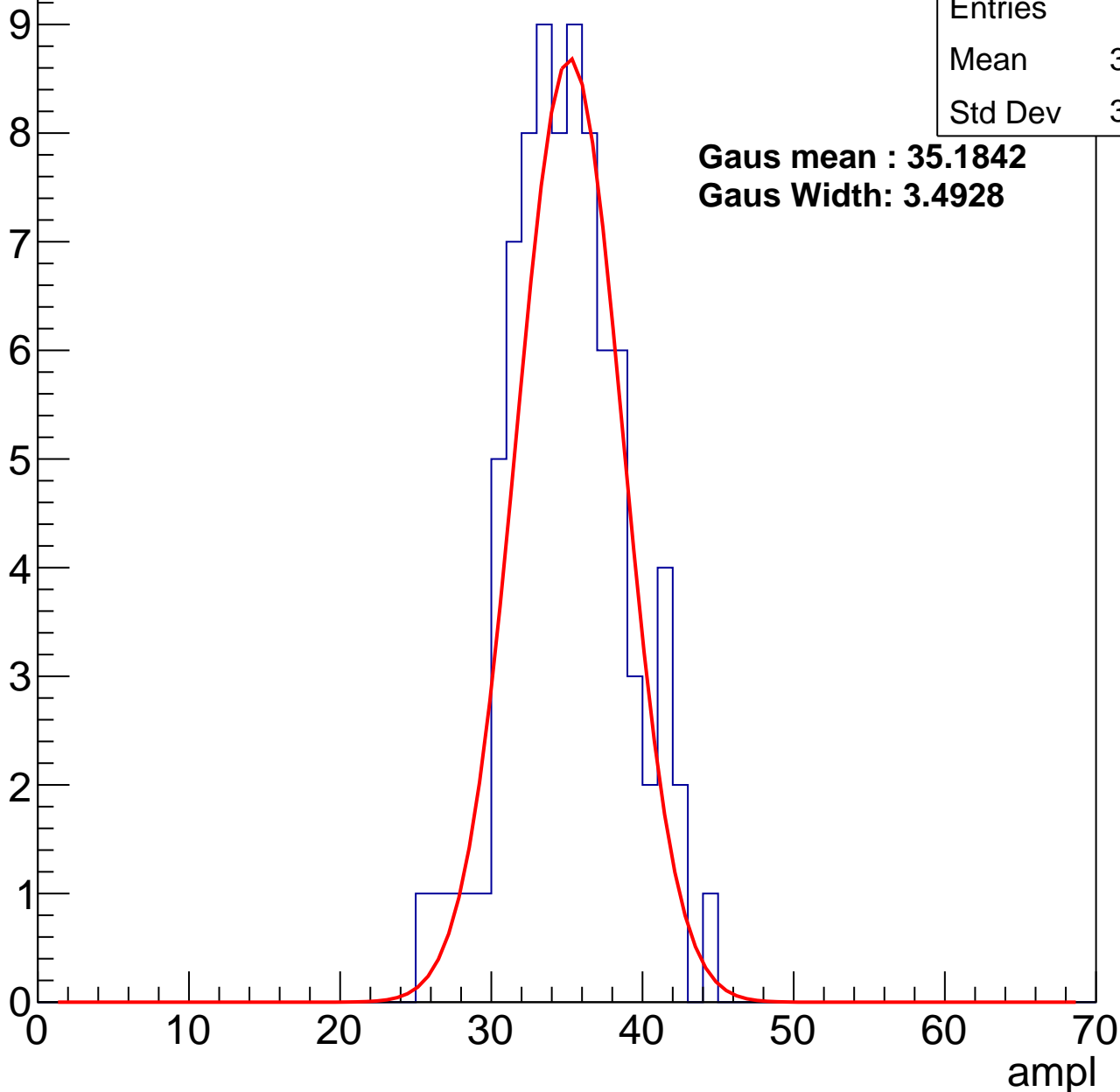
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	83
Mean	34.57
Std Dev	3.762

**Gaus mean : 35.1842**

**Gaus Width: 3.4928**



# B1L101S, U3-ch32, adc2

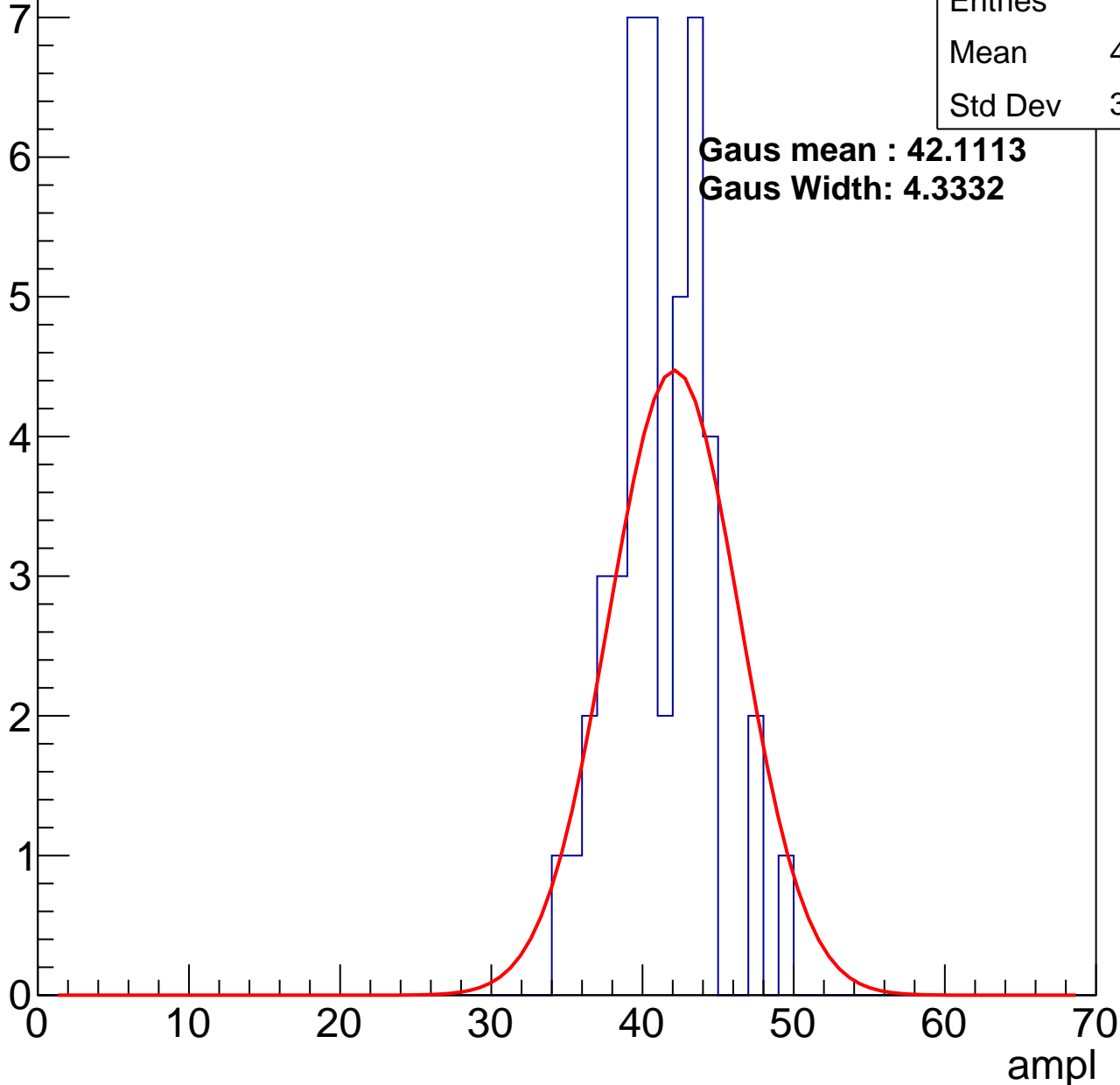
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	40.69
Std Dev	3.147

**Gaus mean : 42.1113**

**Gaus Width: 4.3332**

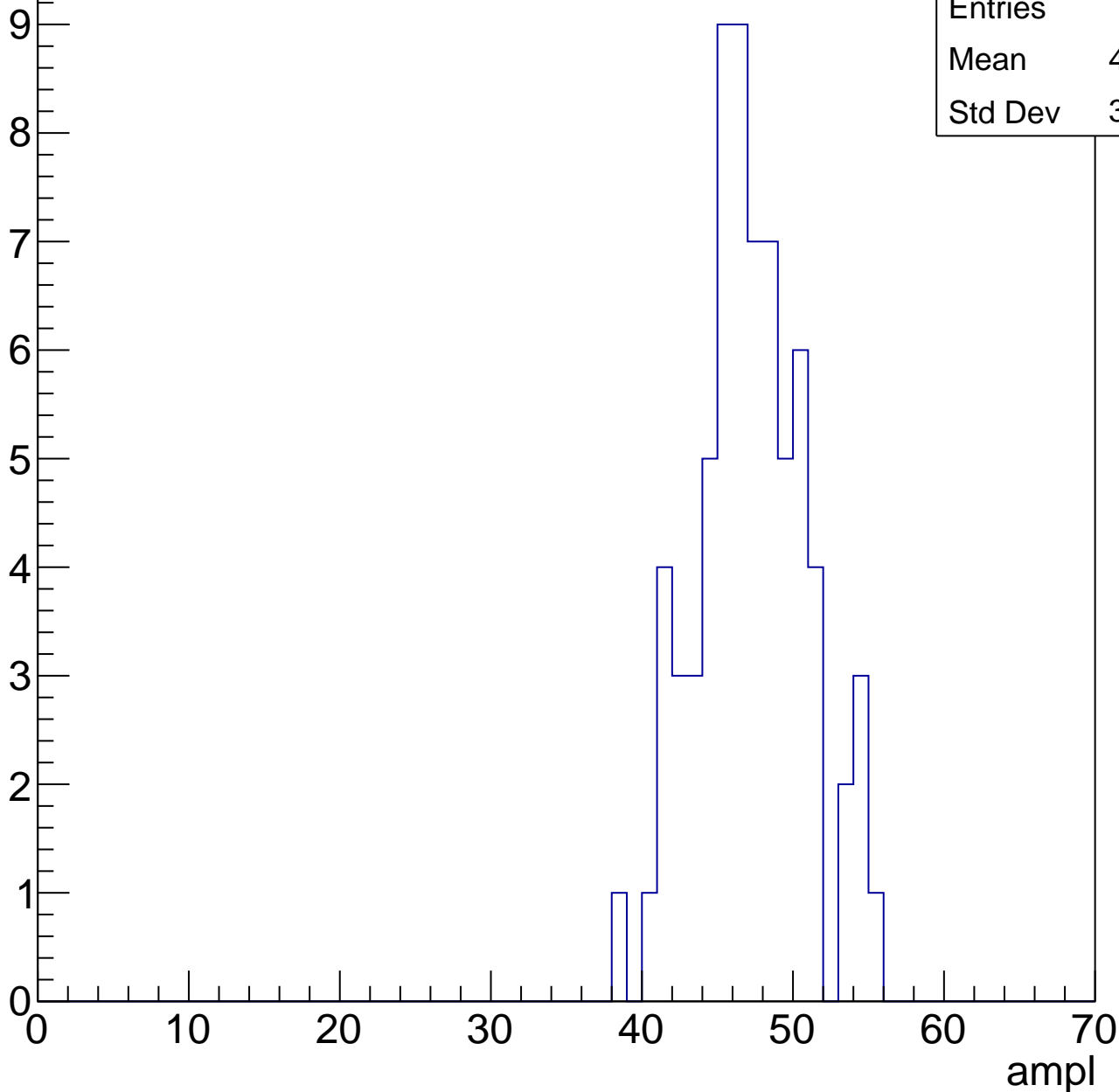


# B1L101S, U3-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	46.76
Std Dev	3.607

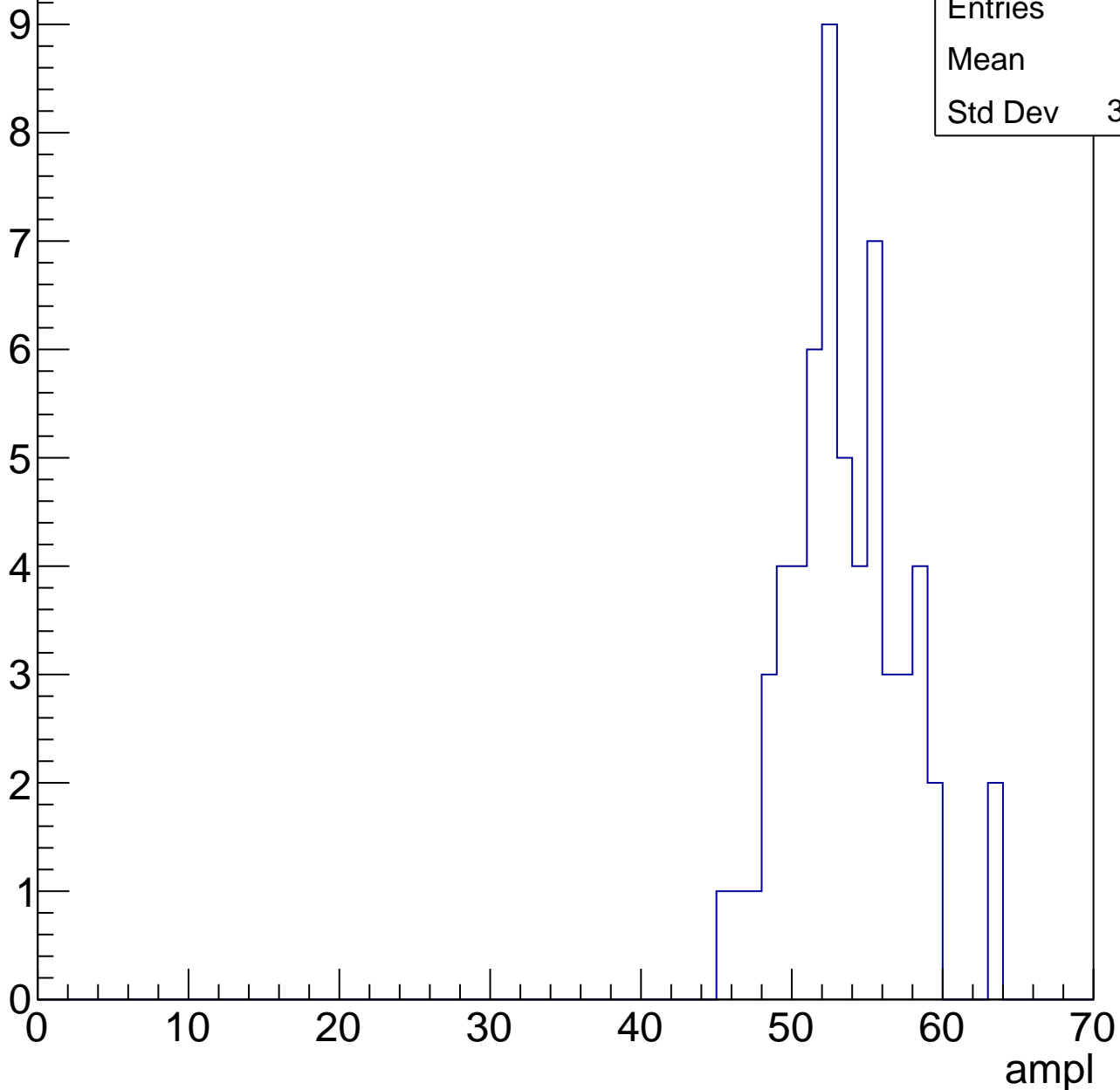


# B1L101S, U3-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	53.1
Std Dev	3.763

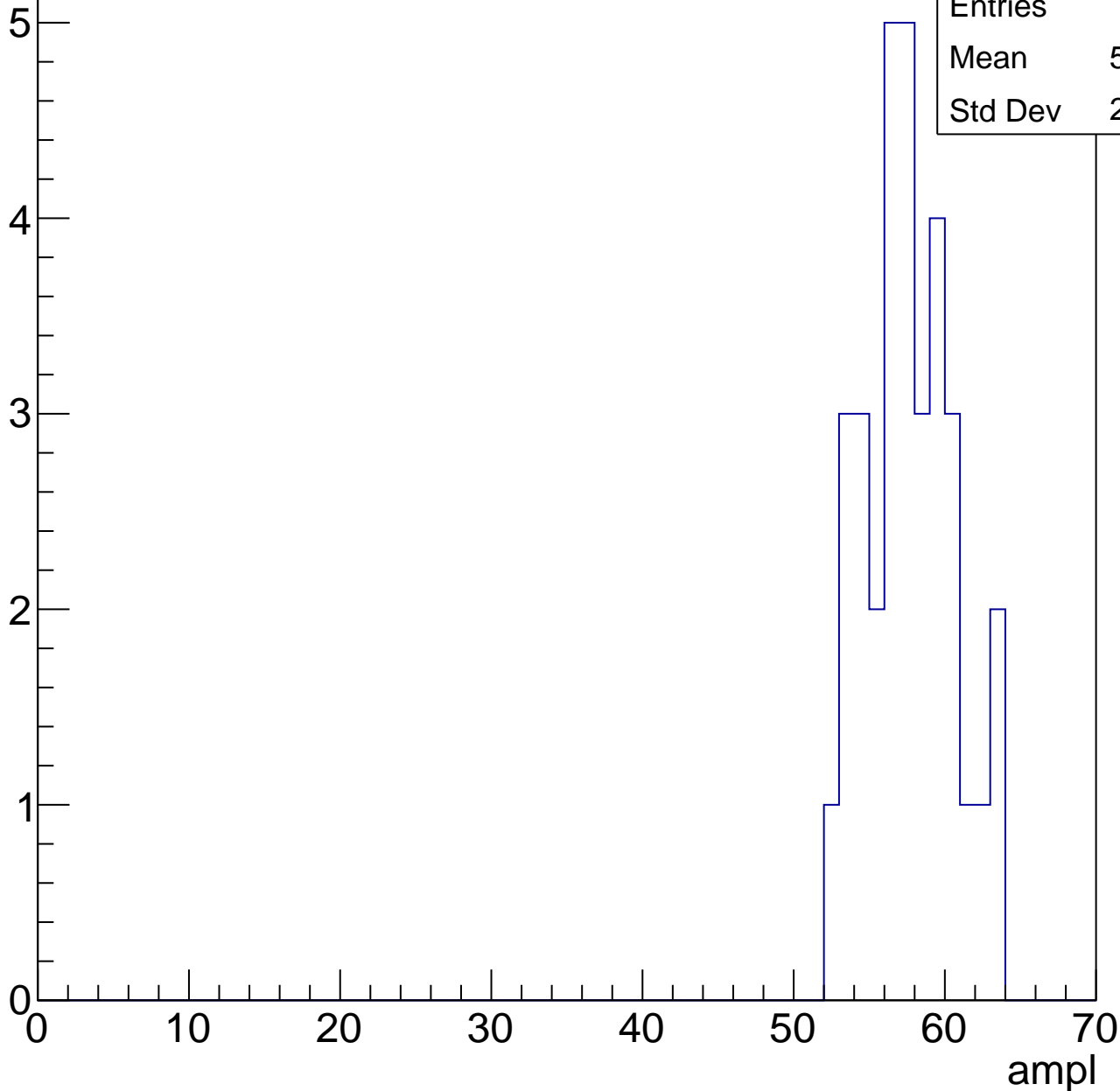


# B1L101S, U3-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	33
Mean	57.18
Std Dev	2.865

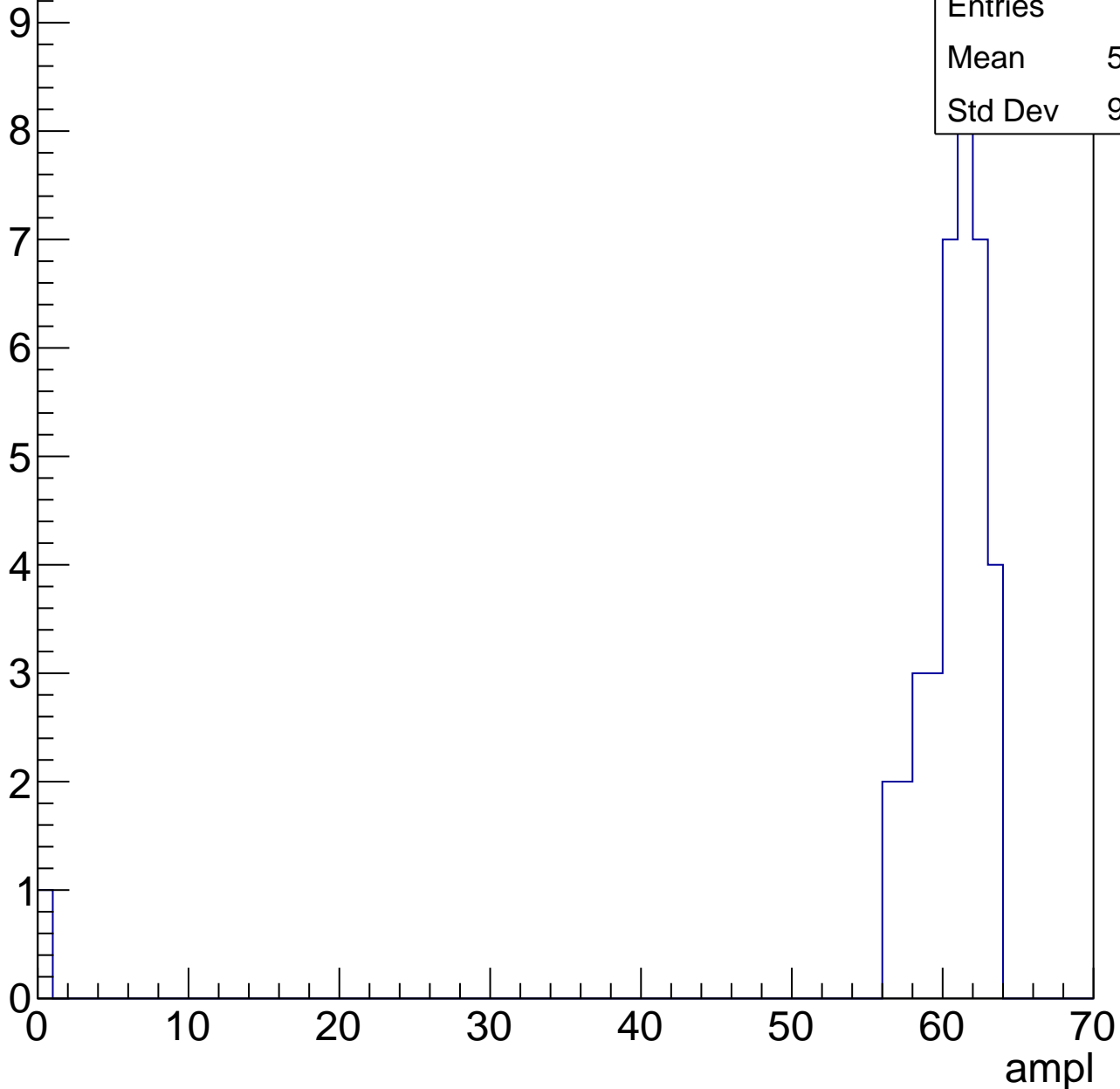


# B1L101S, U3-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	38
Mean	58.74
Std Dev	9.837

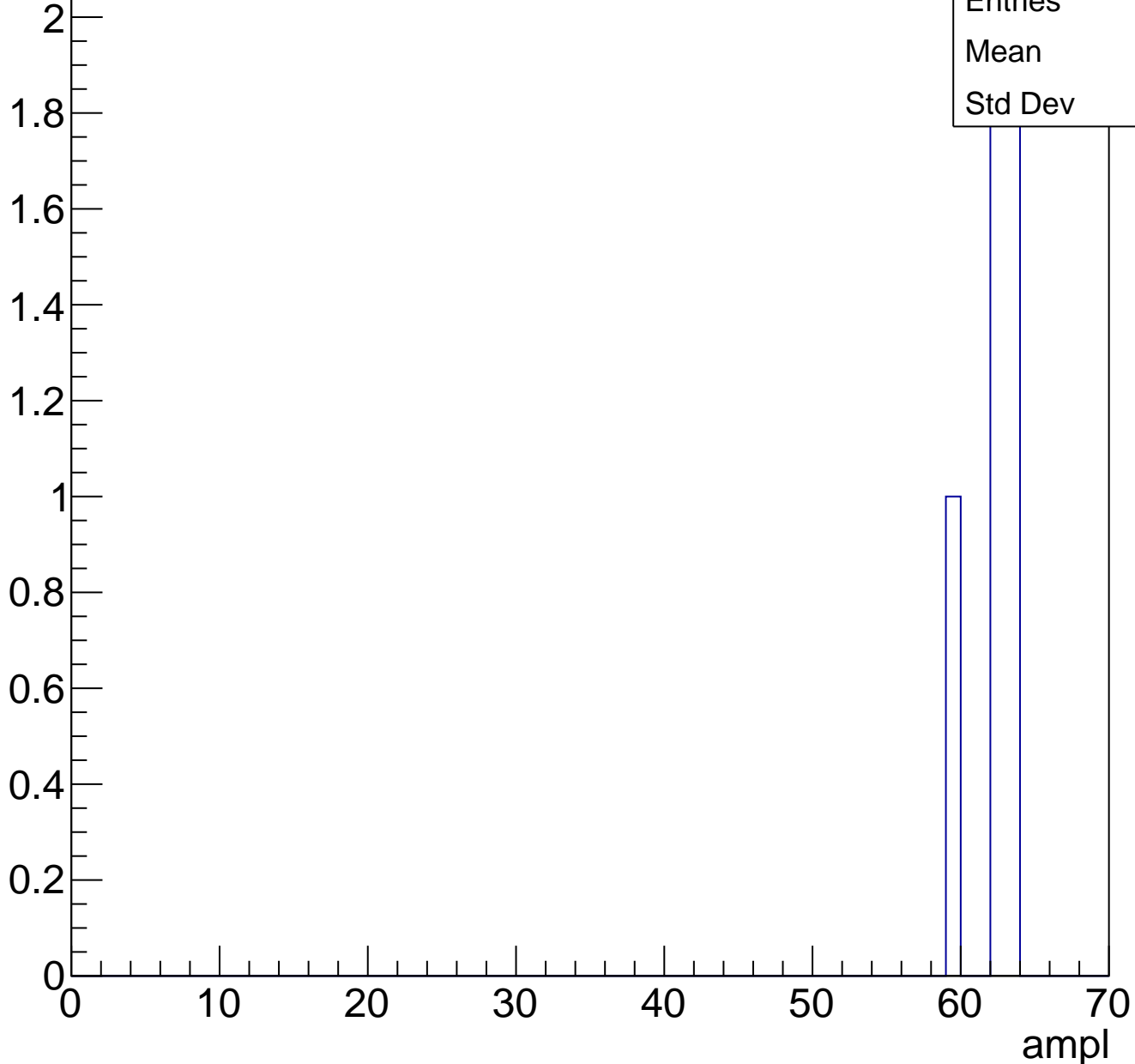




# B1L101S, U3-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch33, adc0

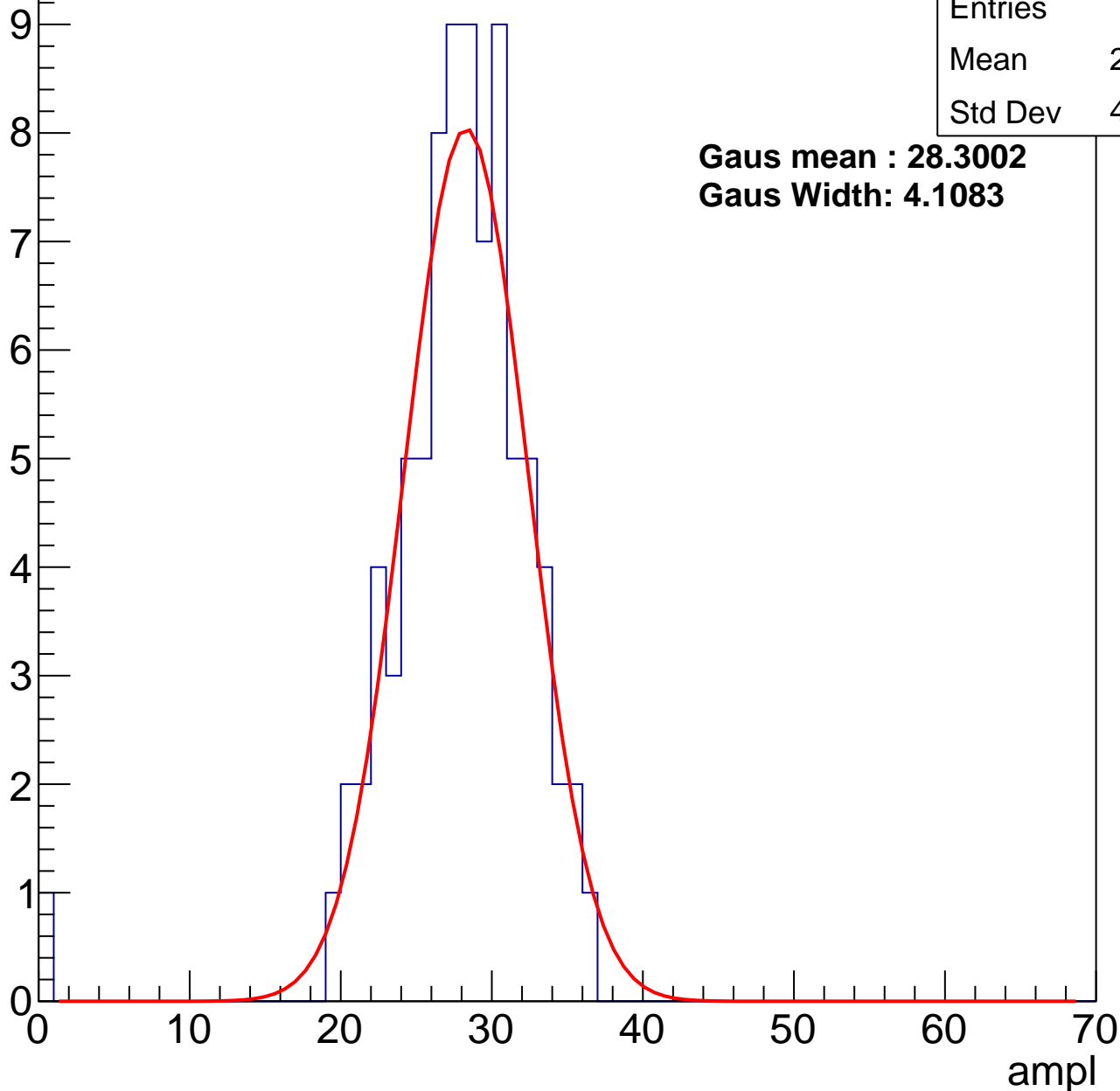
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	84
Mean	27.38
Std Dev	4.813

**Gaus mean : 28.3002**

**Gaus Width: 4.1083**



# B1L101S, U3-ch33, adc1

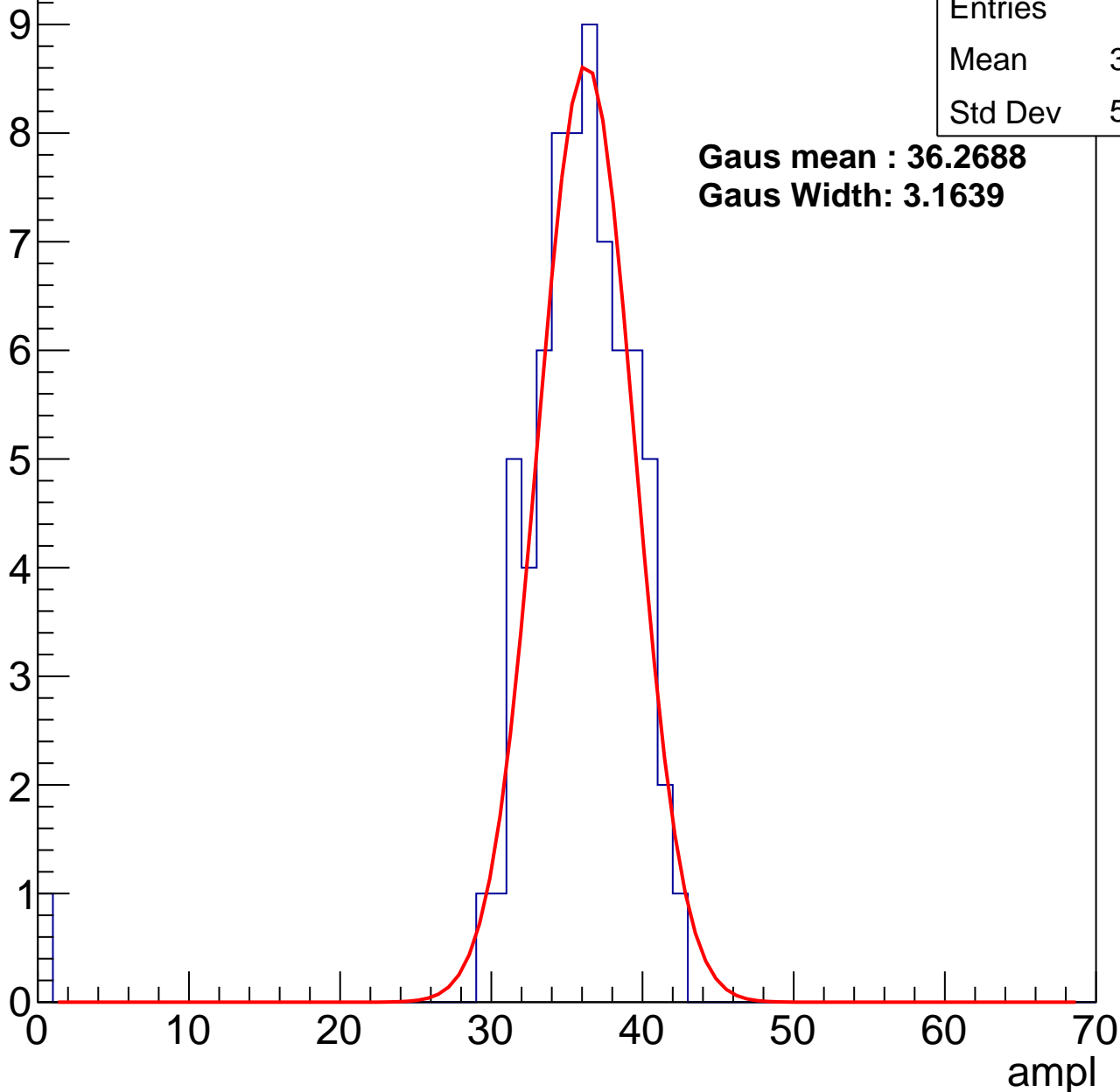
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	35.16
Std Dev	5.162

**Gaus mean : 36.2688**

**Gaus Width: 3.1639**



# B1L101S, U3-ch33, adc2

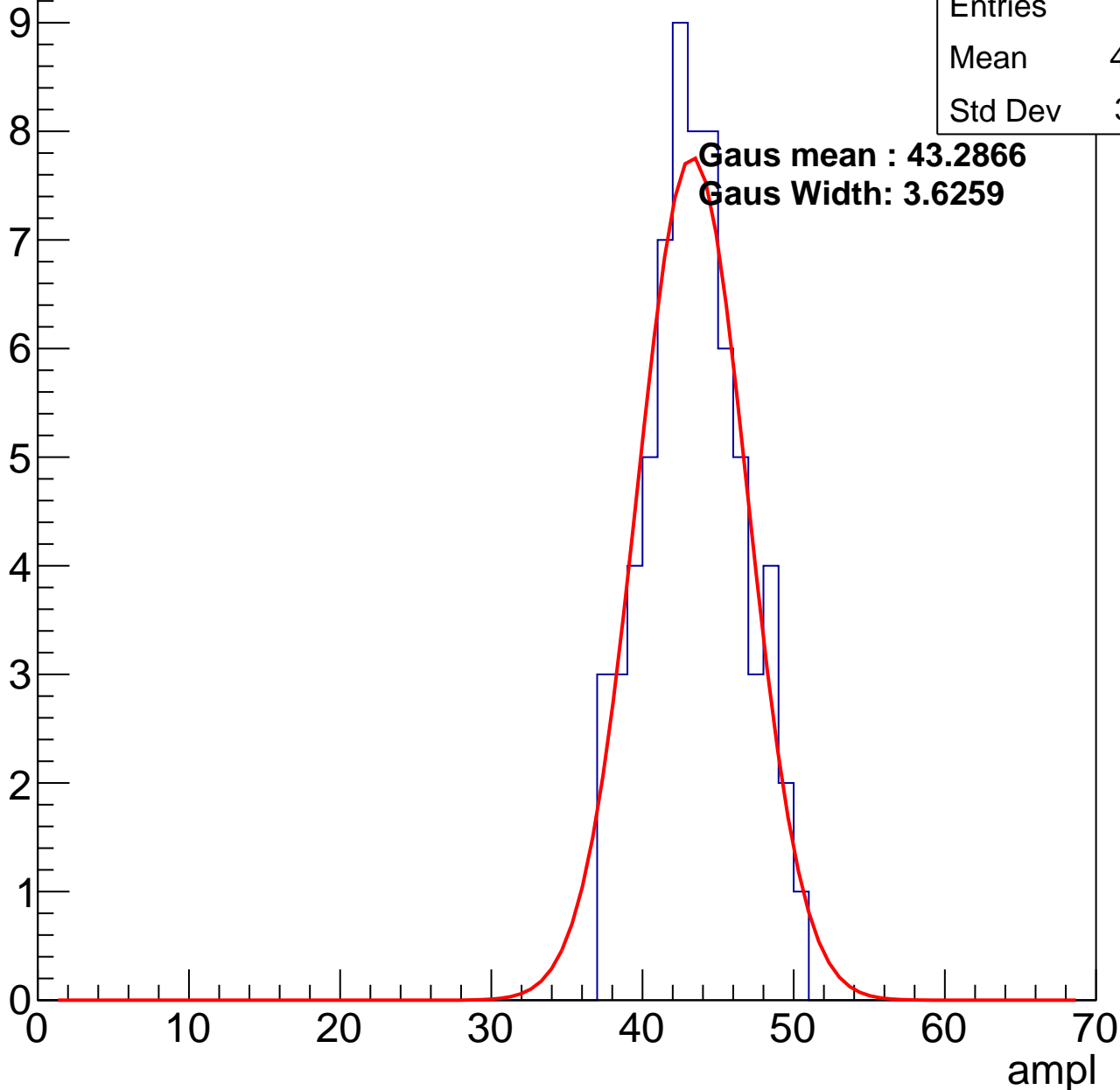
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	42.99
Std Dev	3.151

**Gaus mean : 43.2866**

**Gaus Width: 3.6259**

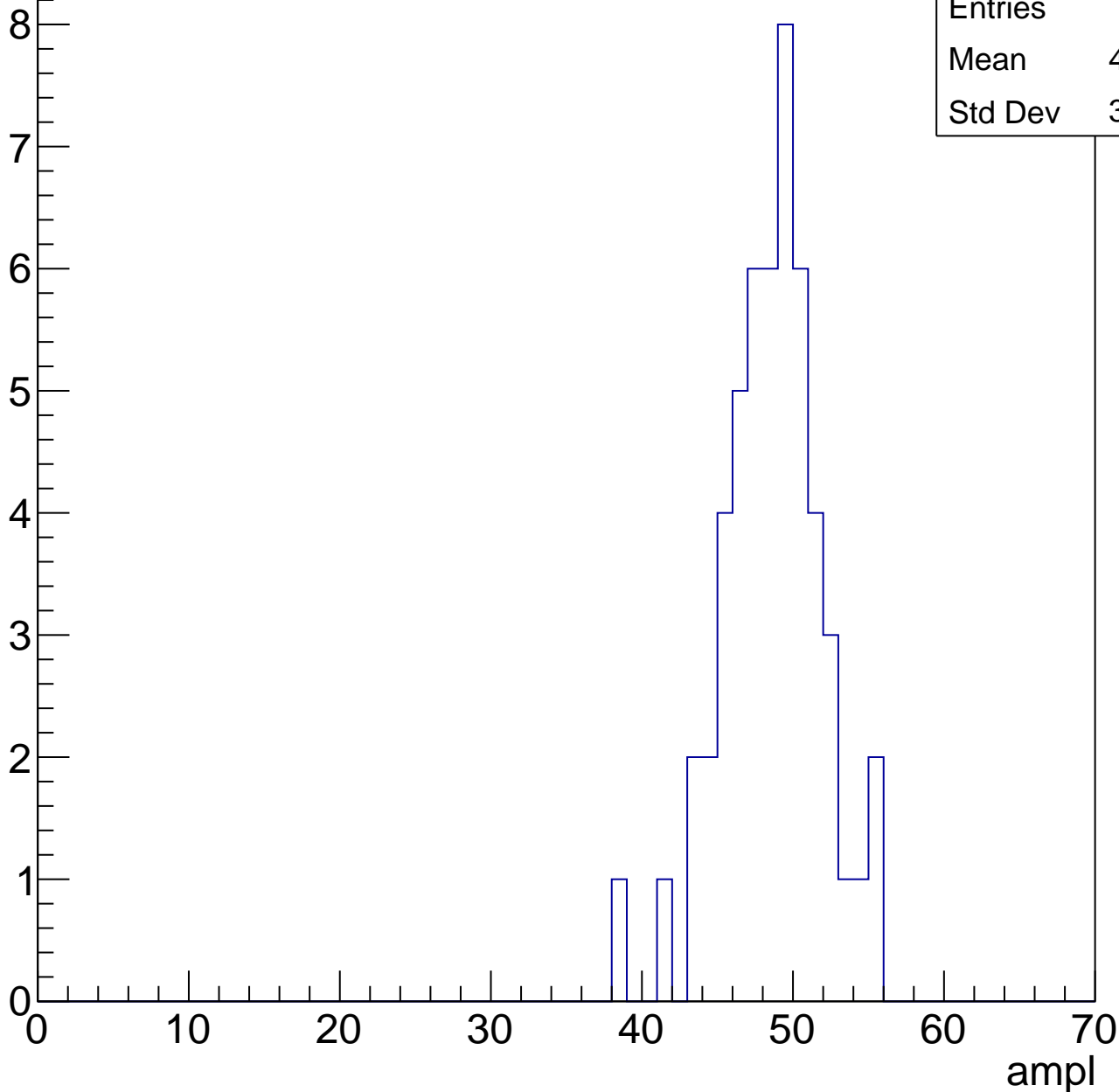


# B1L101S, U3-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

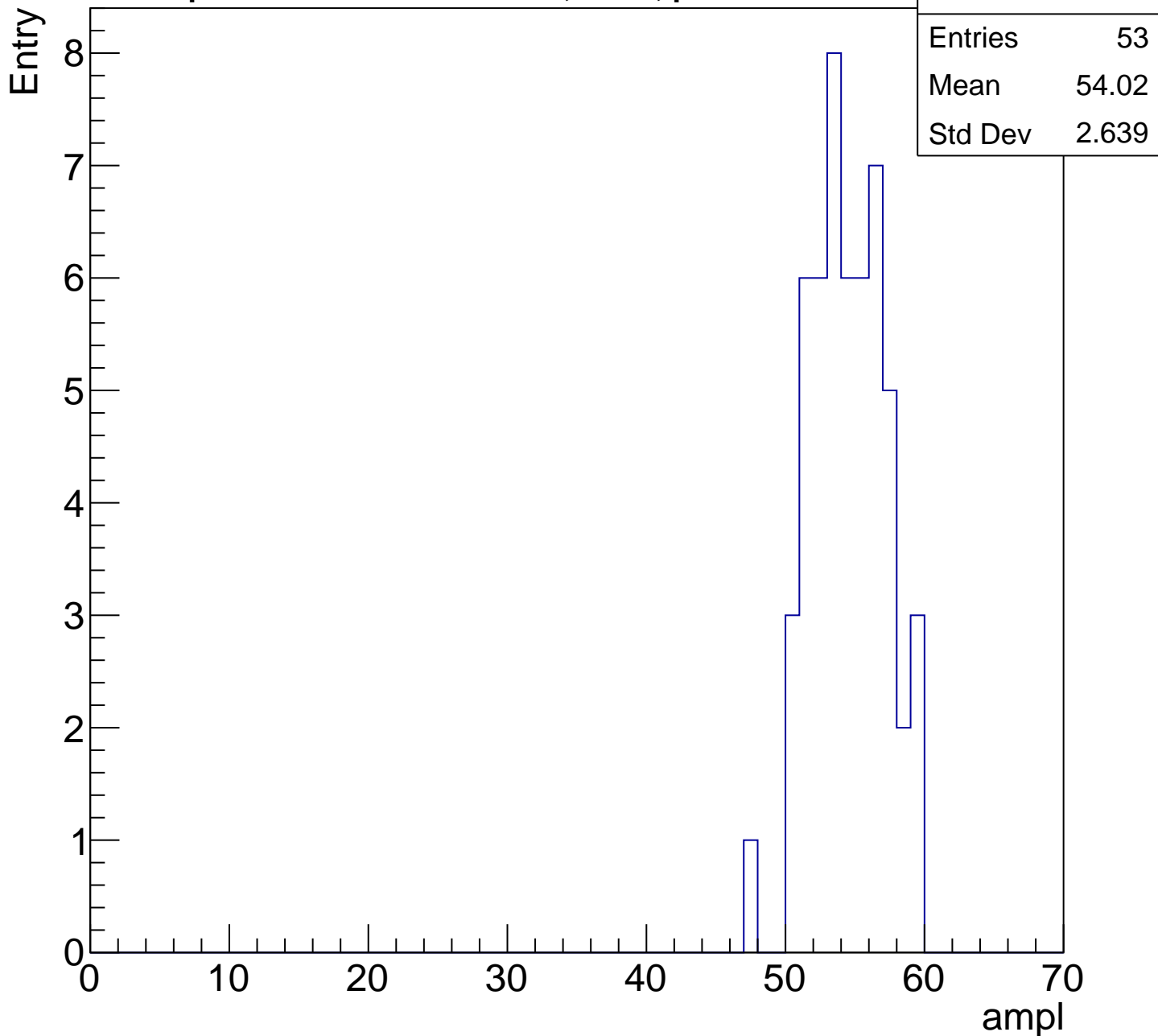
Entry

Entries	52
Mean	48.12
Std Dev	3.303



# B1L101S, U3-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

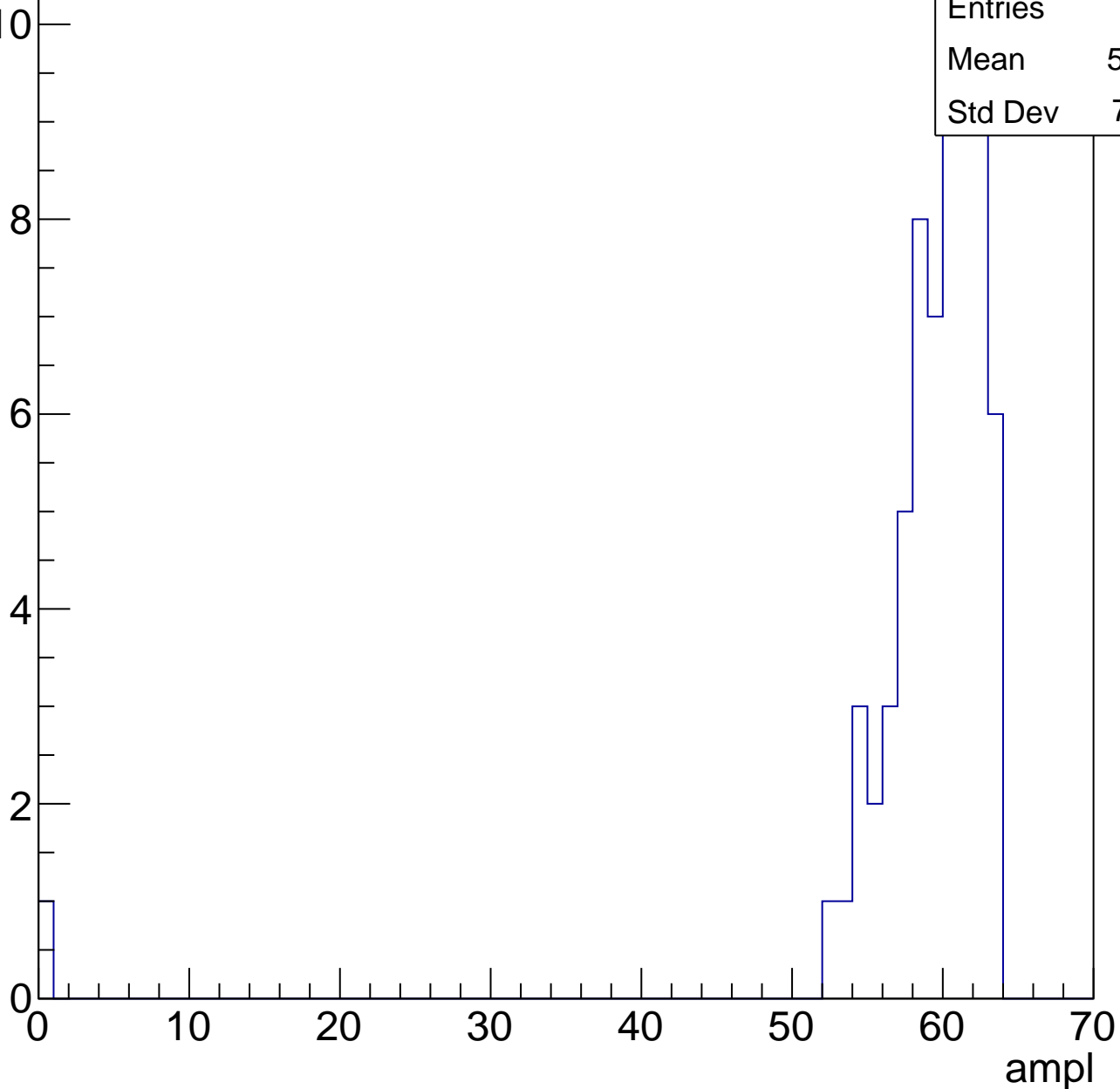


# B1L101S, U3-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

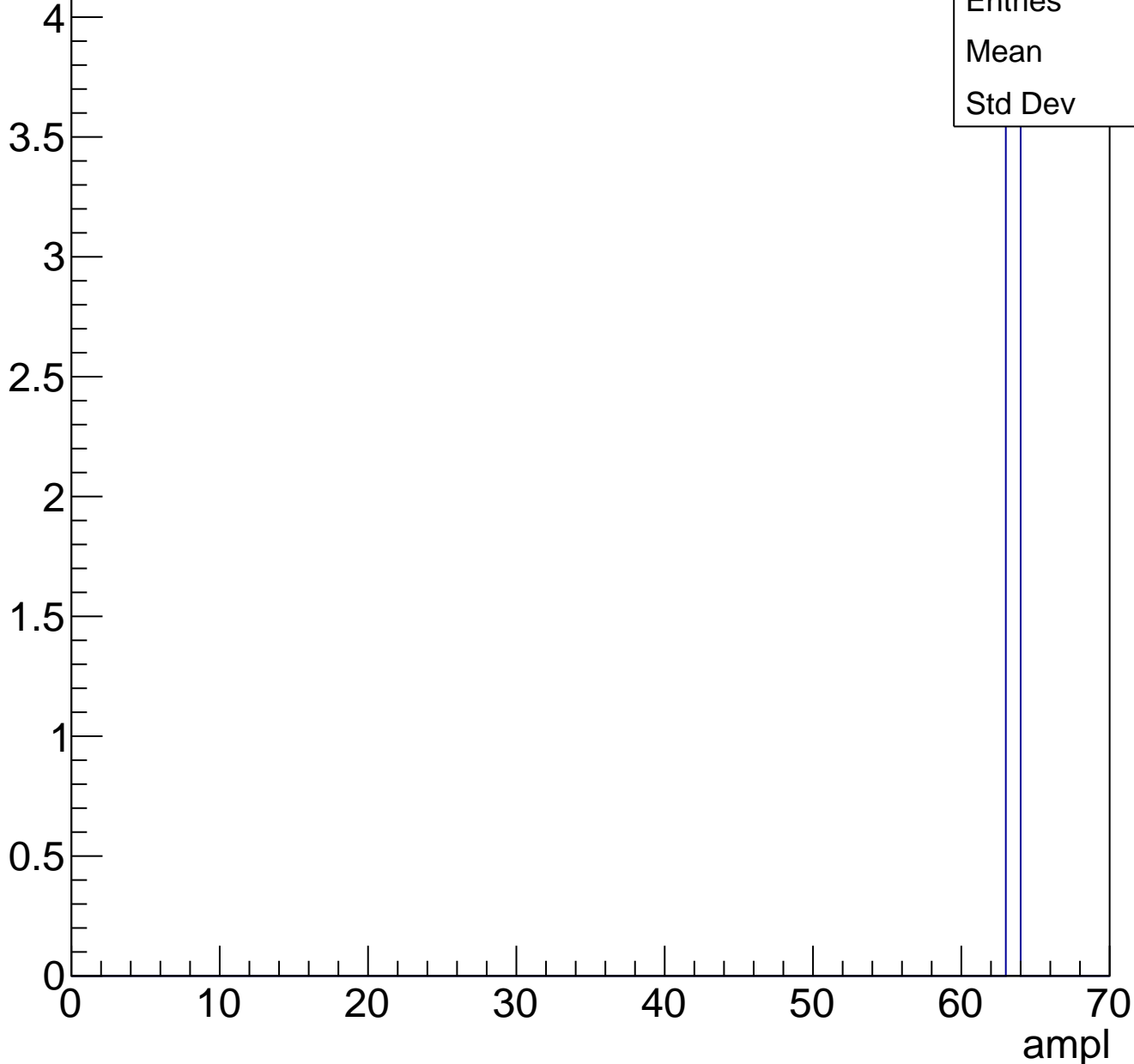
Entries	67
Mean	58.43
Std Dev	7.671



# B1L101S, U3-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U3-ch34, adc0

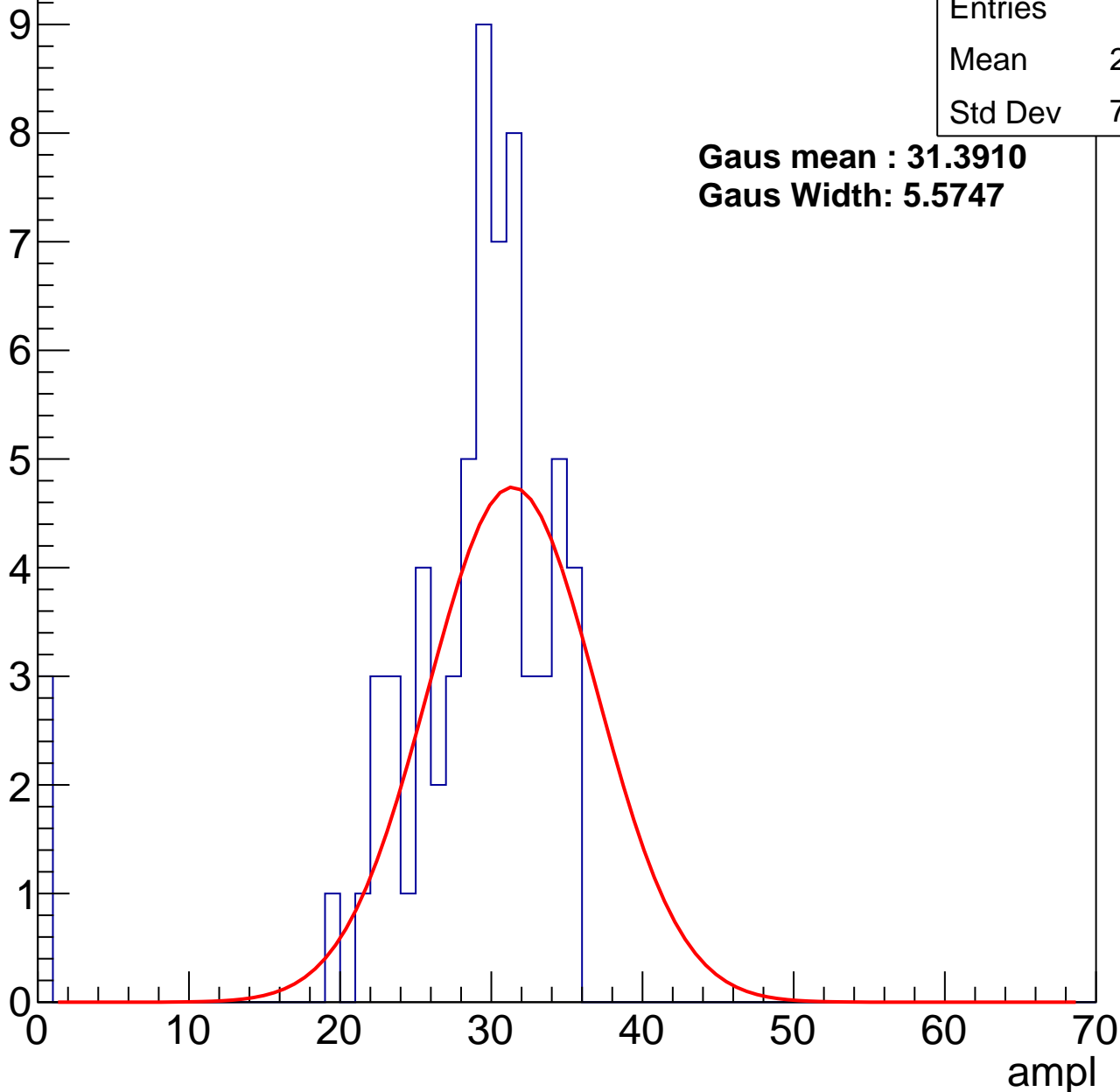
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	27.63
Std Dev	7.154

**Gaus mean : 31.3910**

**Gaus Width: 5.5747**



# B1L101S, U3-ch34, adc1

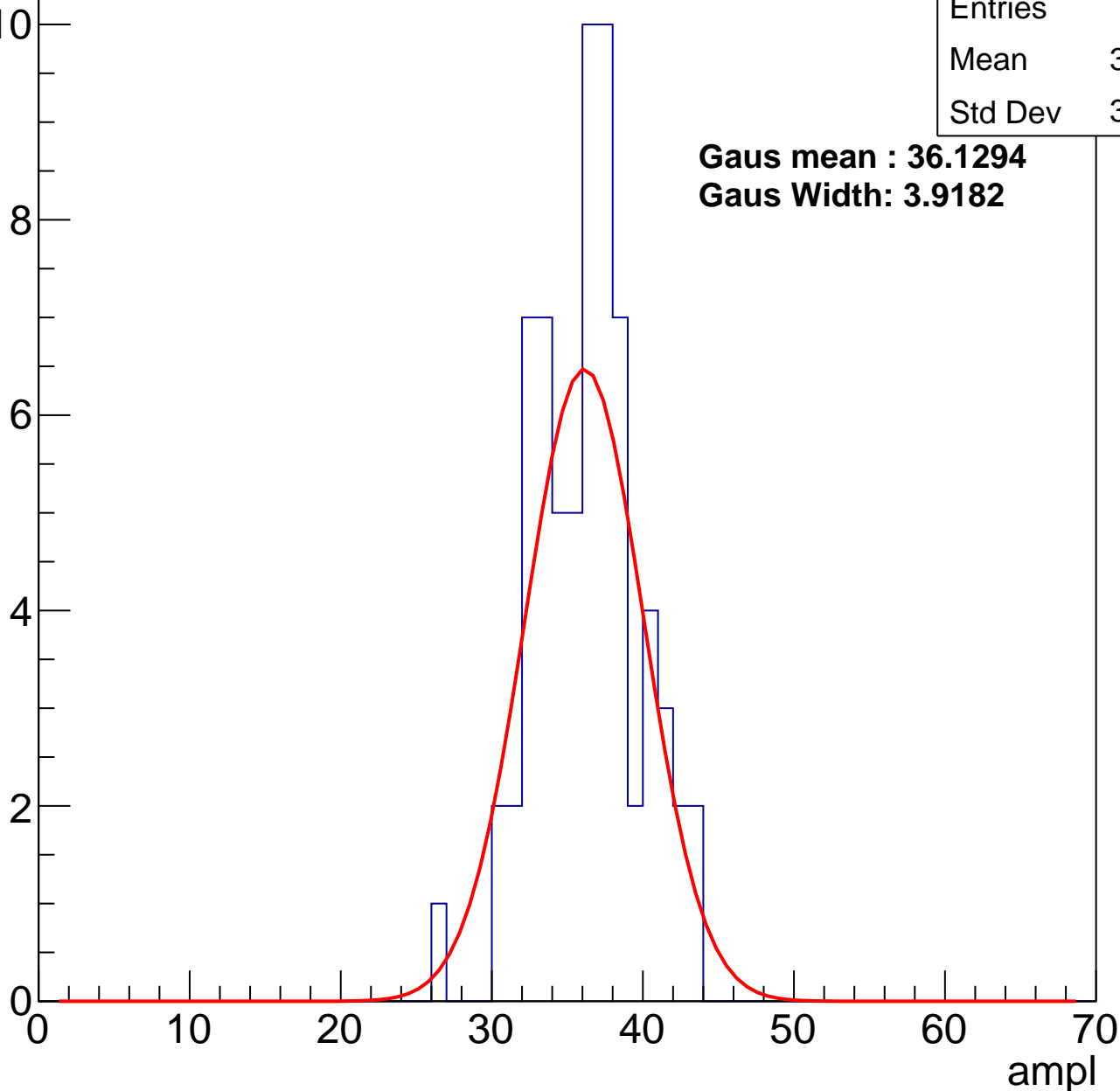
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	35.87
Std Dev	3.375

**Gaus mean : 36.1294**

**Gaus Width: 3.9182**



# B1L101S, U3-ch34, adc2

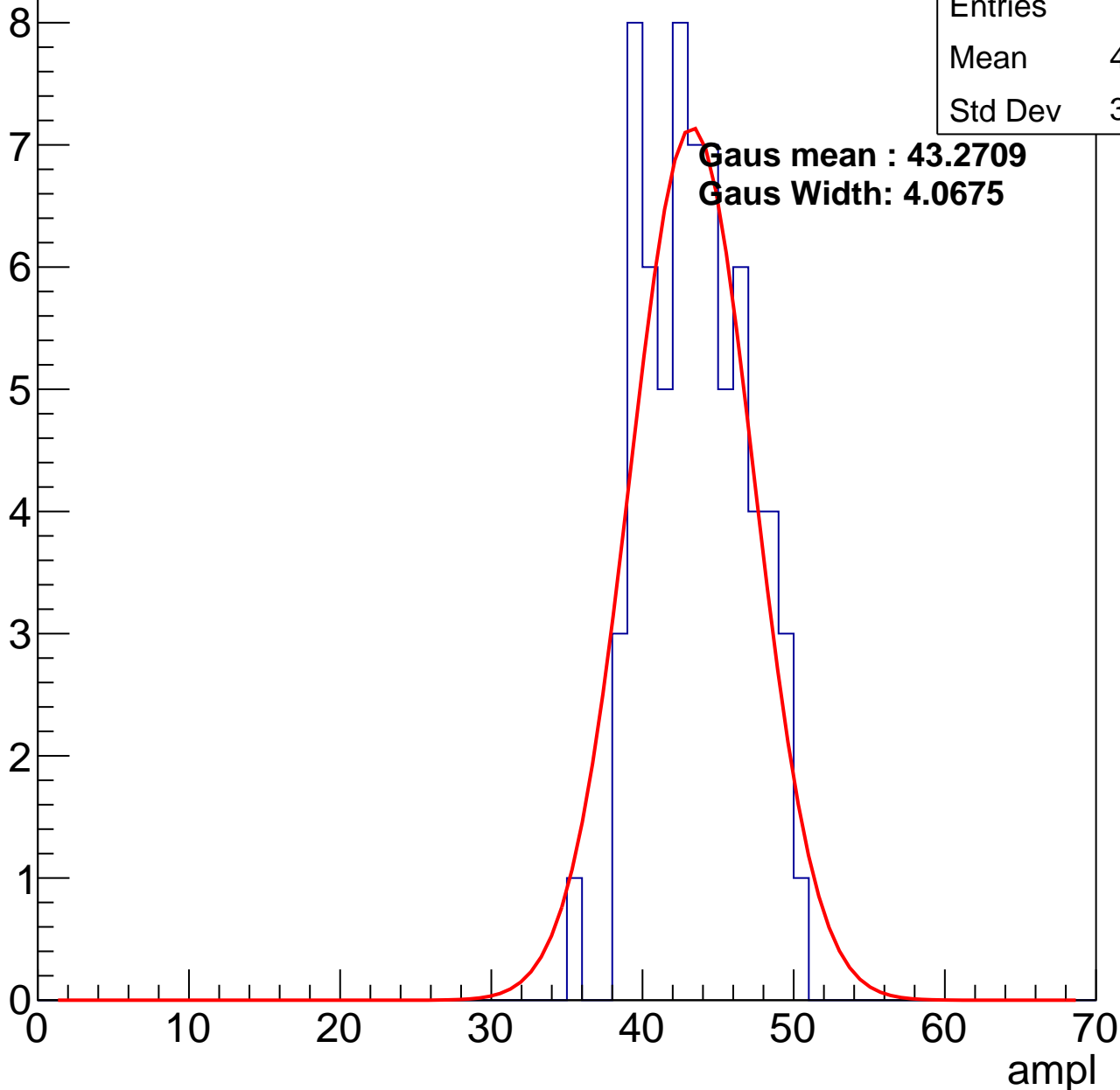
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	43.07
Std Dev	3.322

**Gaus mean : 43.2709**

**Gaus Width: 4.0675**

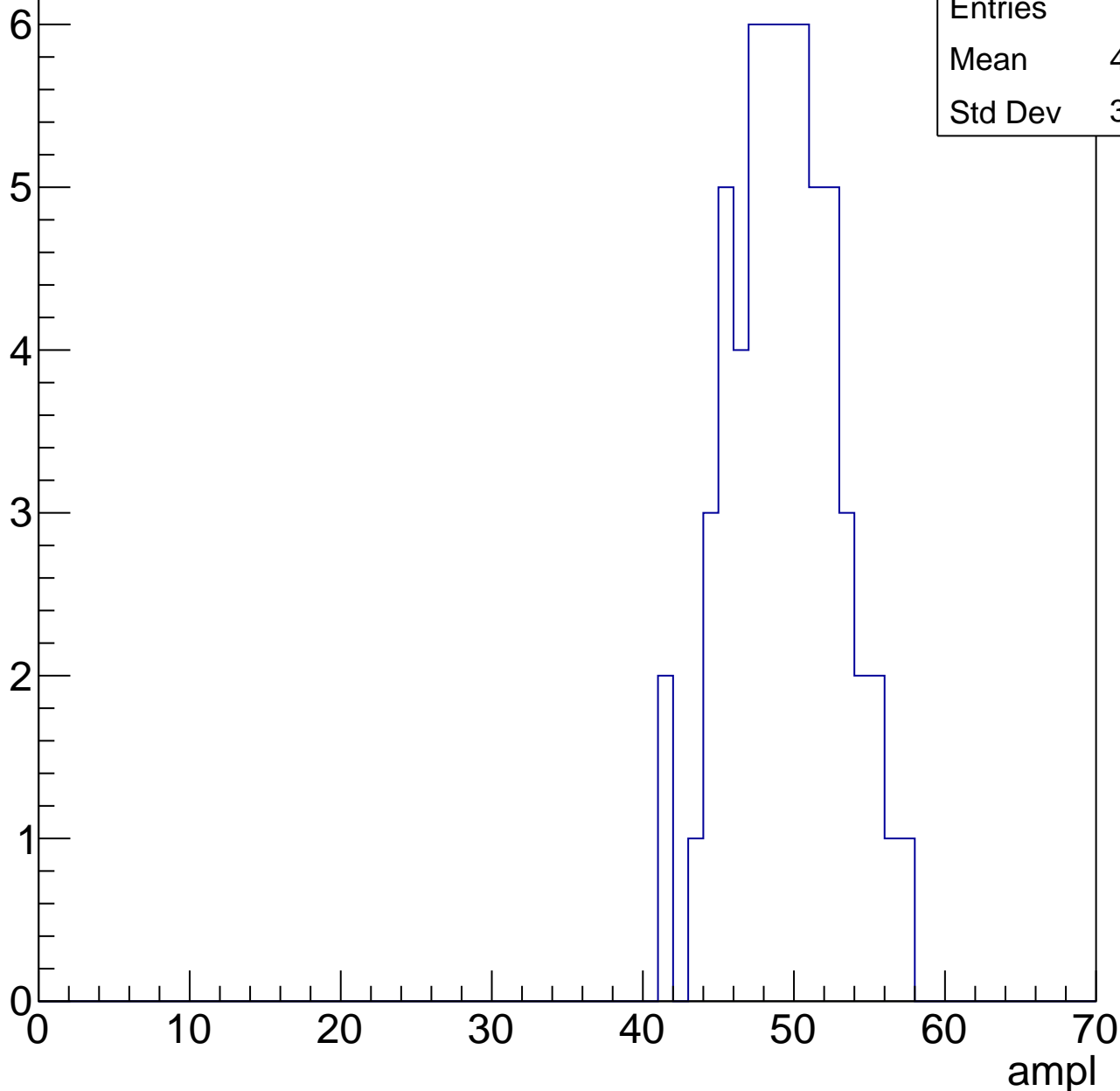


# B1L101S, U3-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

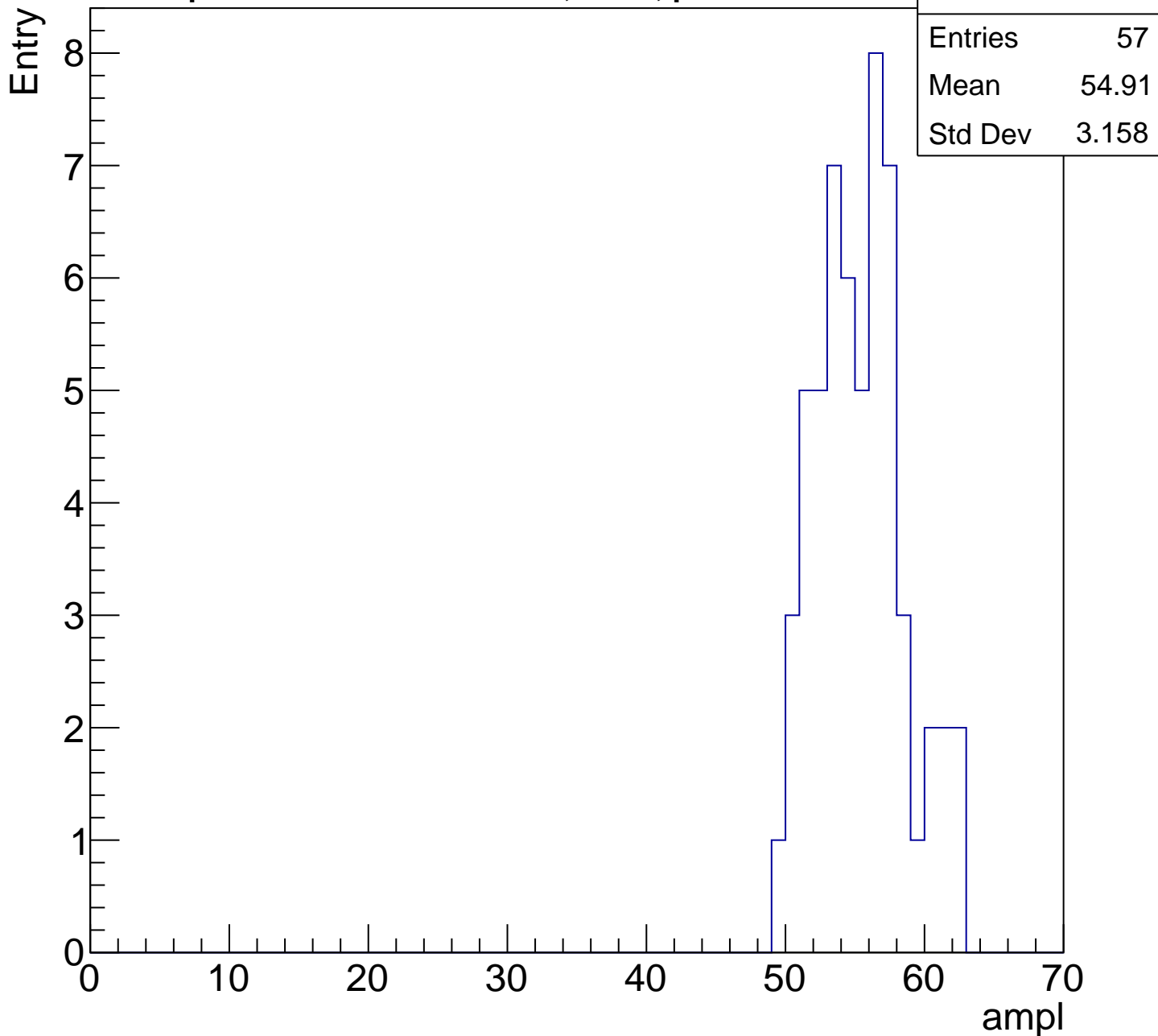
Entry

Entries	58
Mean	48.88
Std Dev	3.567



# B1L101S, U3-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch34, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

Entries	45
Mean	59.47
Std Dev	2.409

0

10

20

30

40

50

60

70

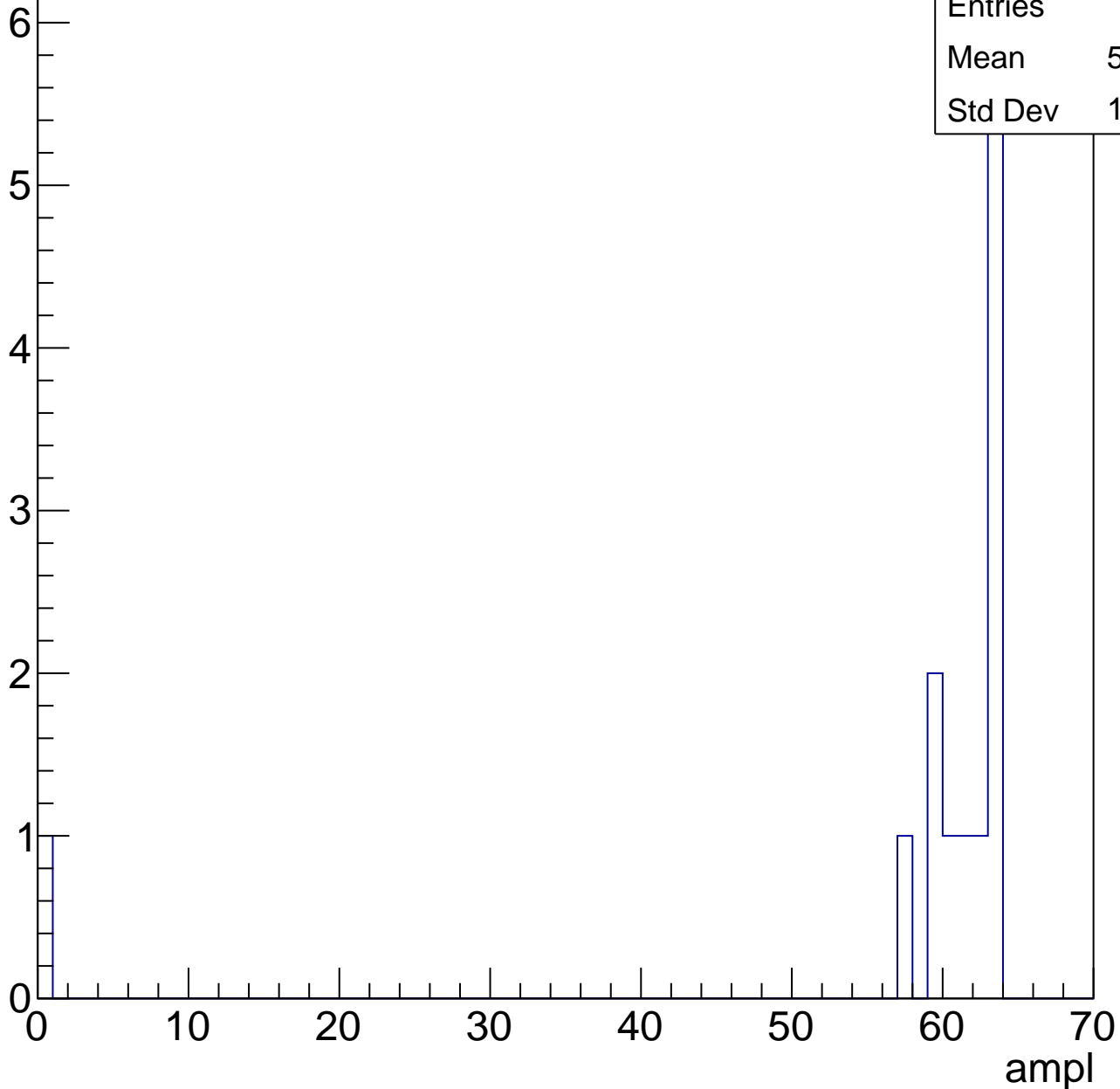
ampl

# B1L101S, U3-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	13
Mean	56.62
Std Dev	16.46





# B1L101S, U3-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch35, adc0

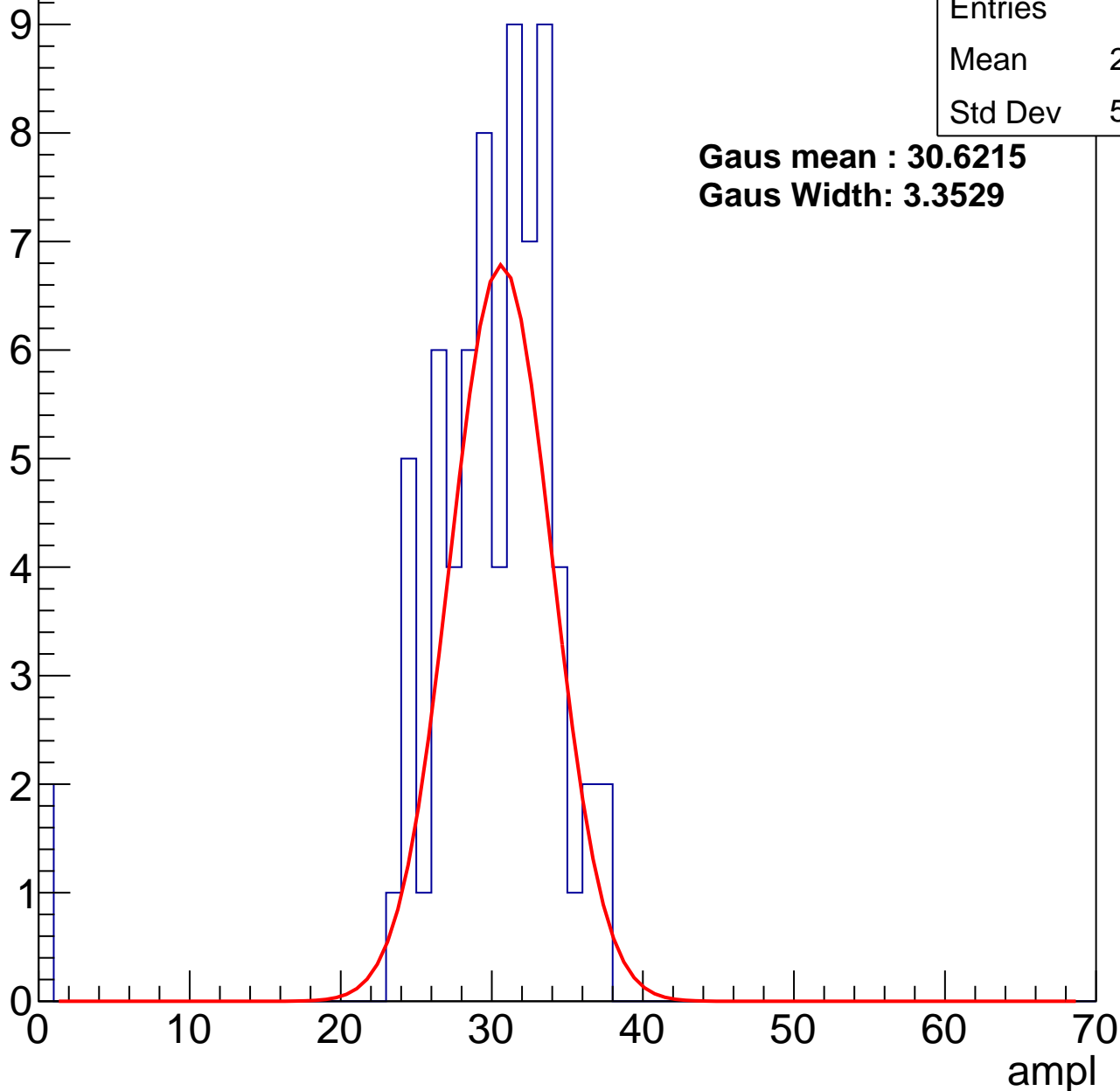
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	29.14
Std Dev	5.984

**Gaus mean : 30.6215**

**Gaus Width: 3.3529**



# B1L101S, U3-ch35, adc1

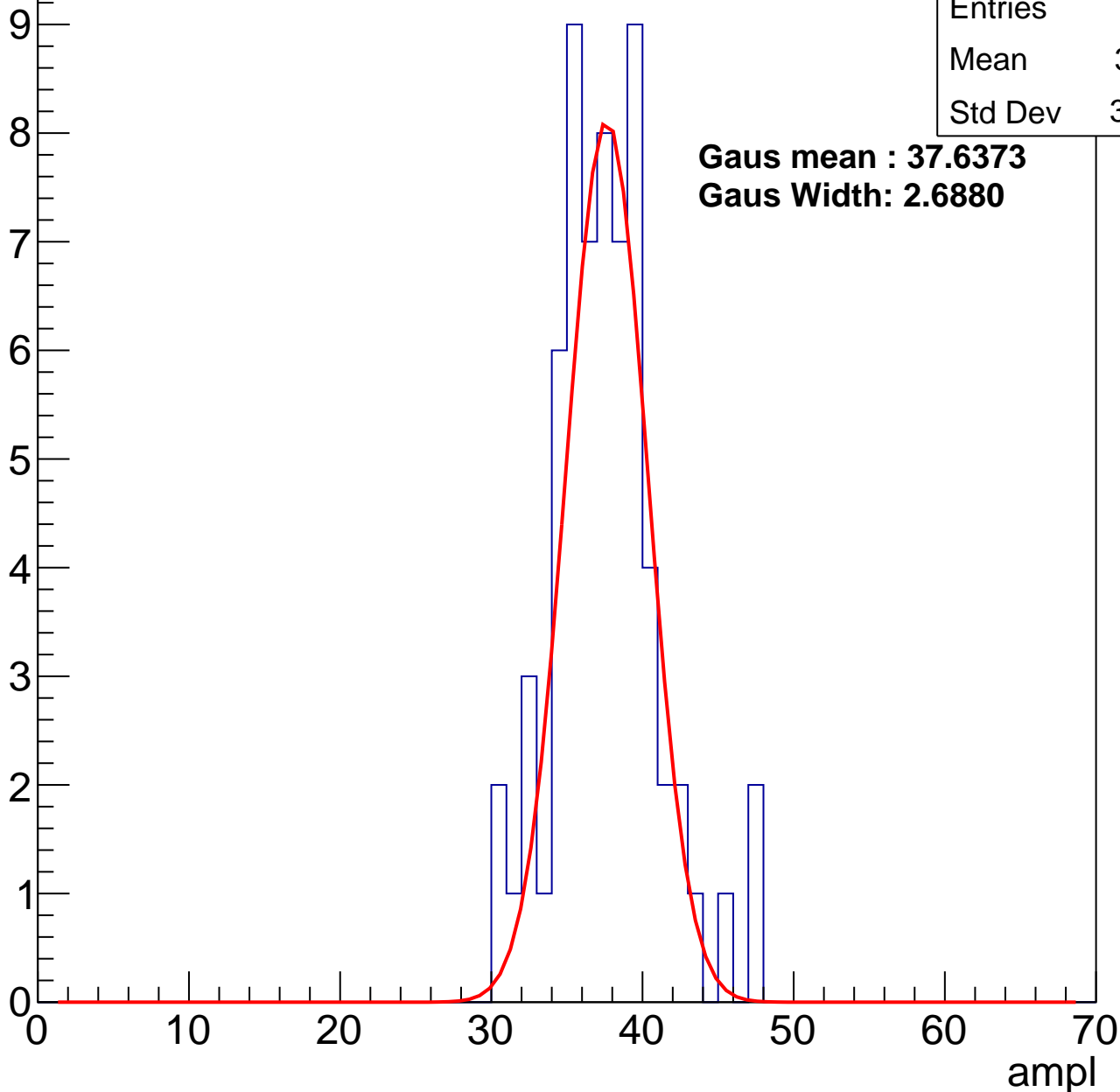
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	37.11
Std Dev	3.469

**Gaus mean : 37.6373**

**Gaus Width: 2.6880**



# B1L101S, U3-ch35, adc2

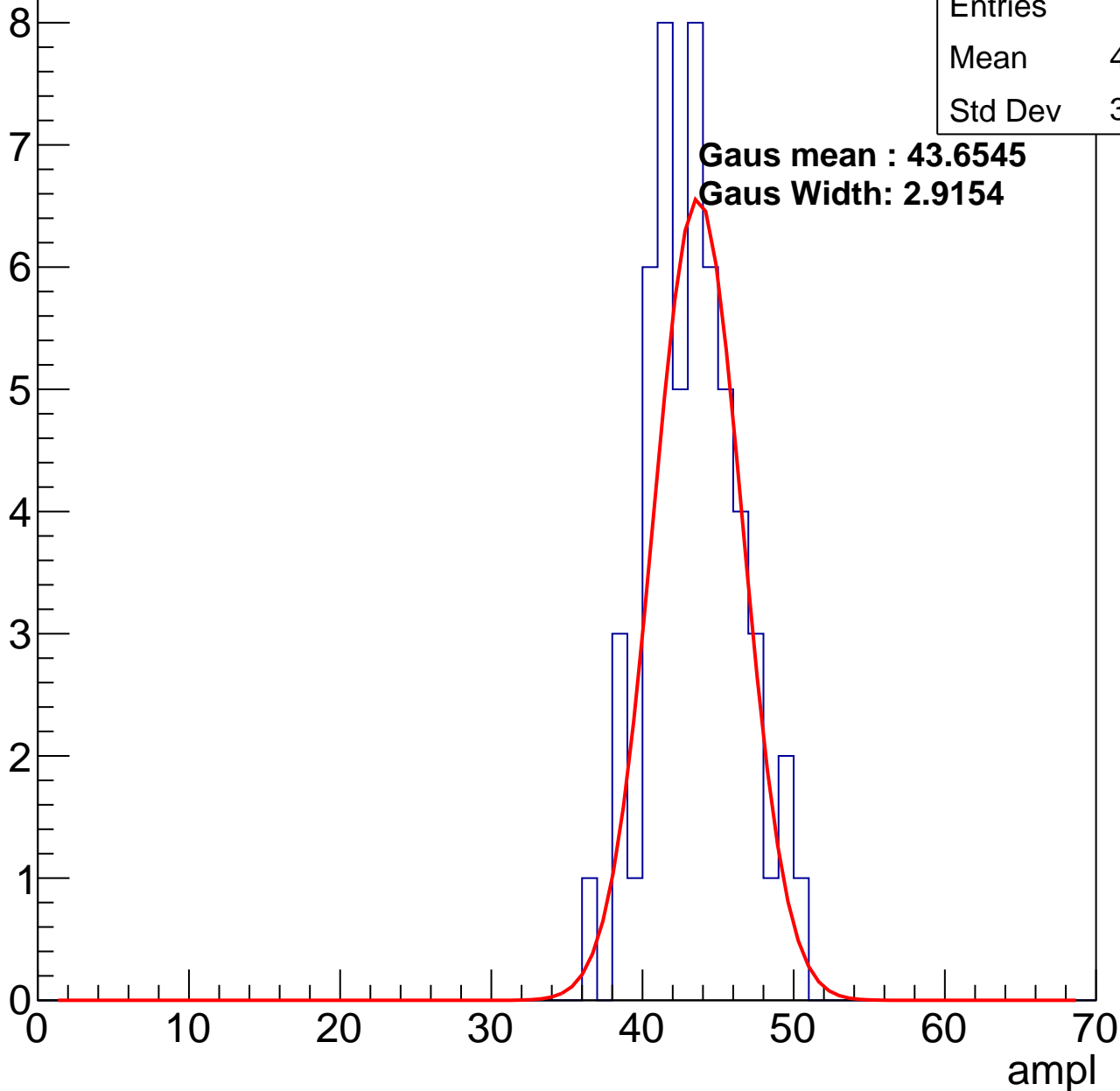
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	42.98
Std Dev	3.003

**Gaus mean : 43.6545**

**Gaus Width: 2.9154**

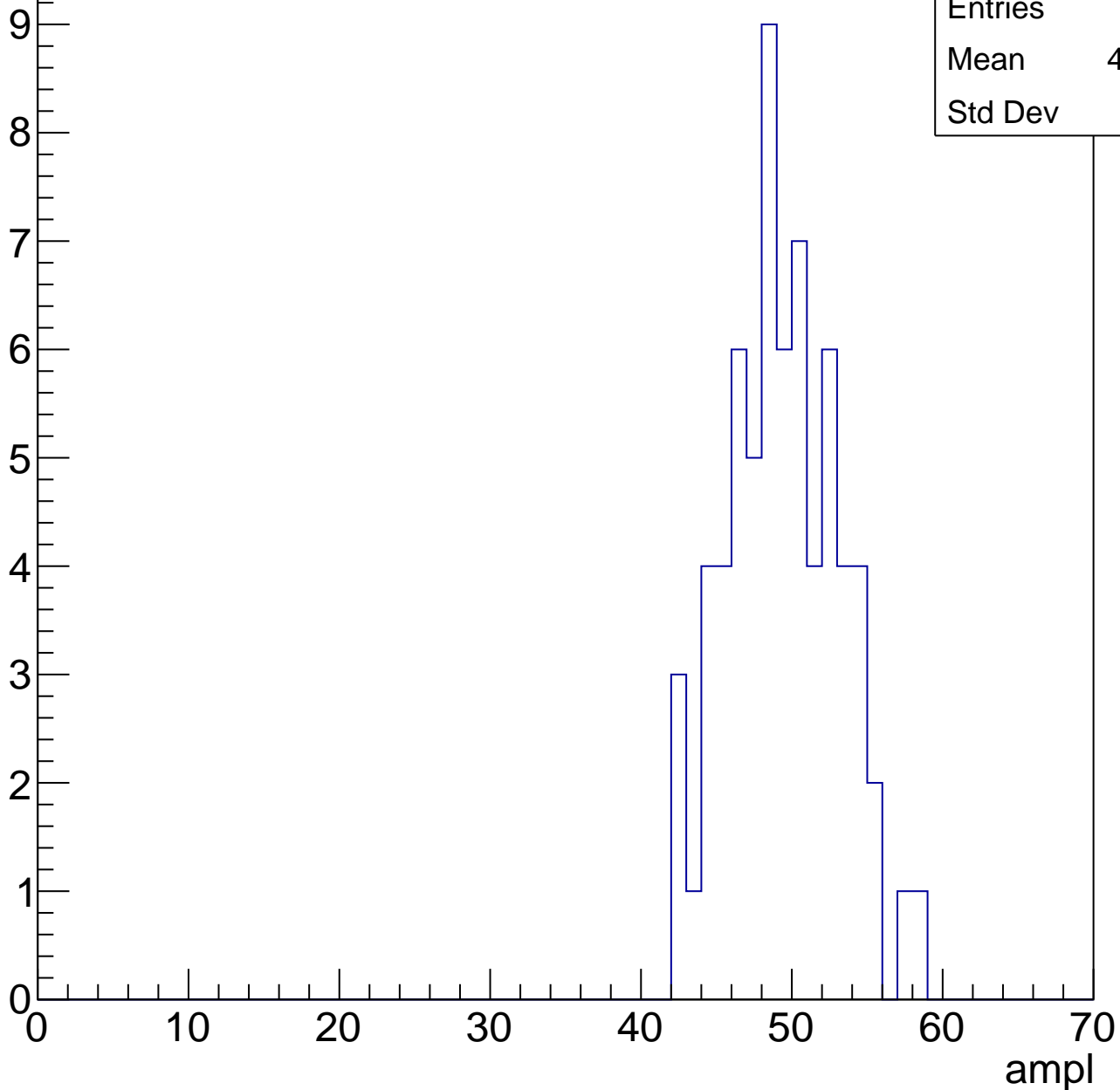


# B1L101S, U3-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

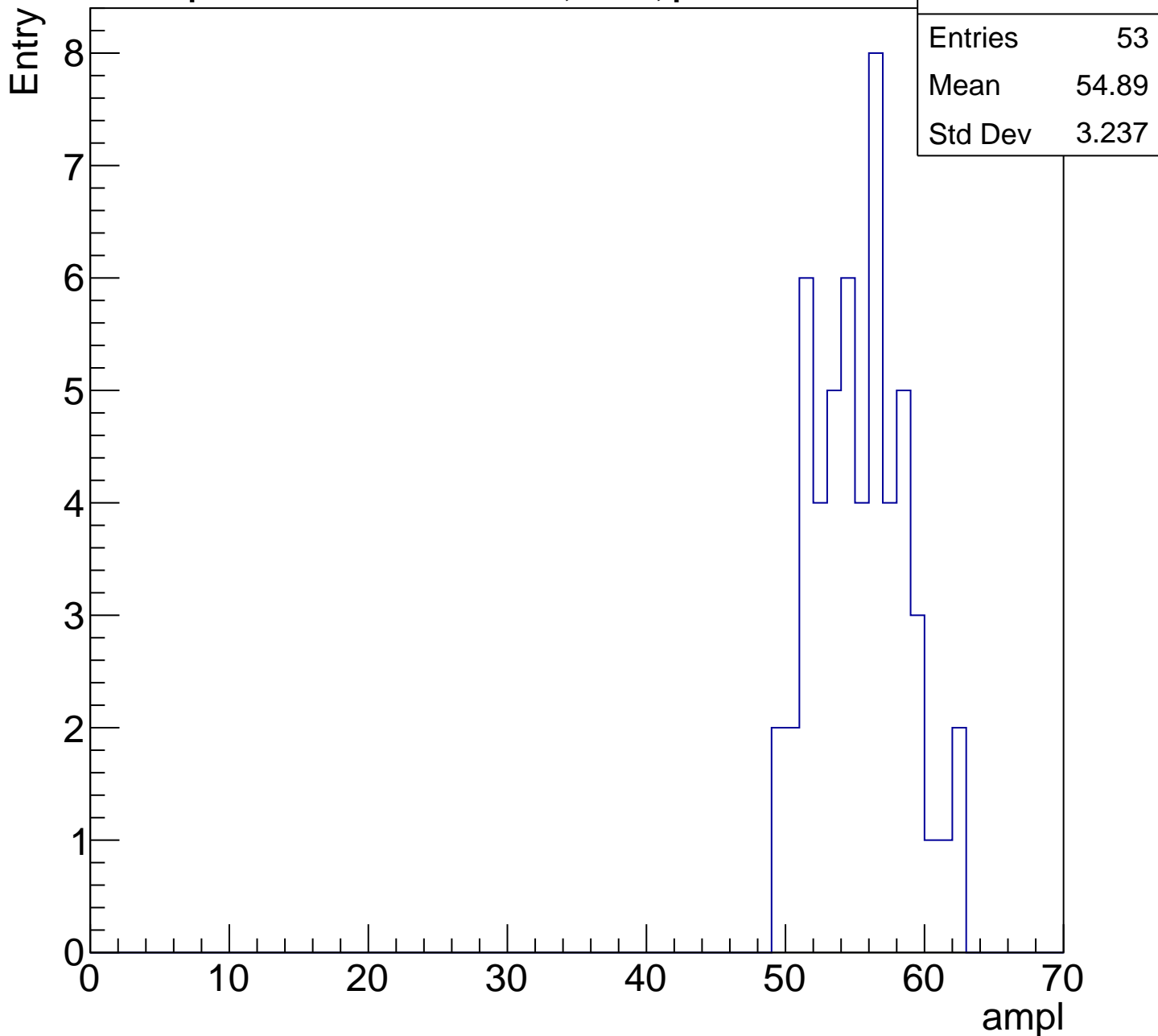
Entry

Entries	67
Mean	48.97
Std Dev	3.64



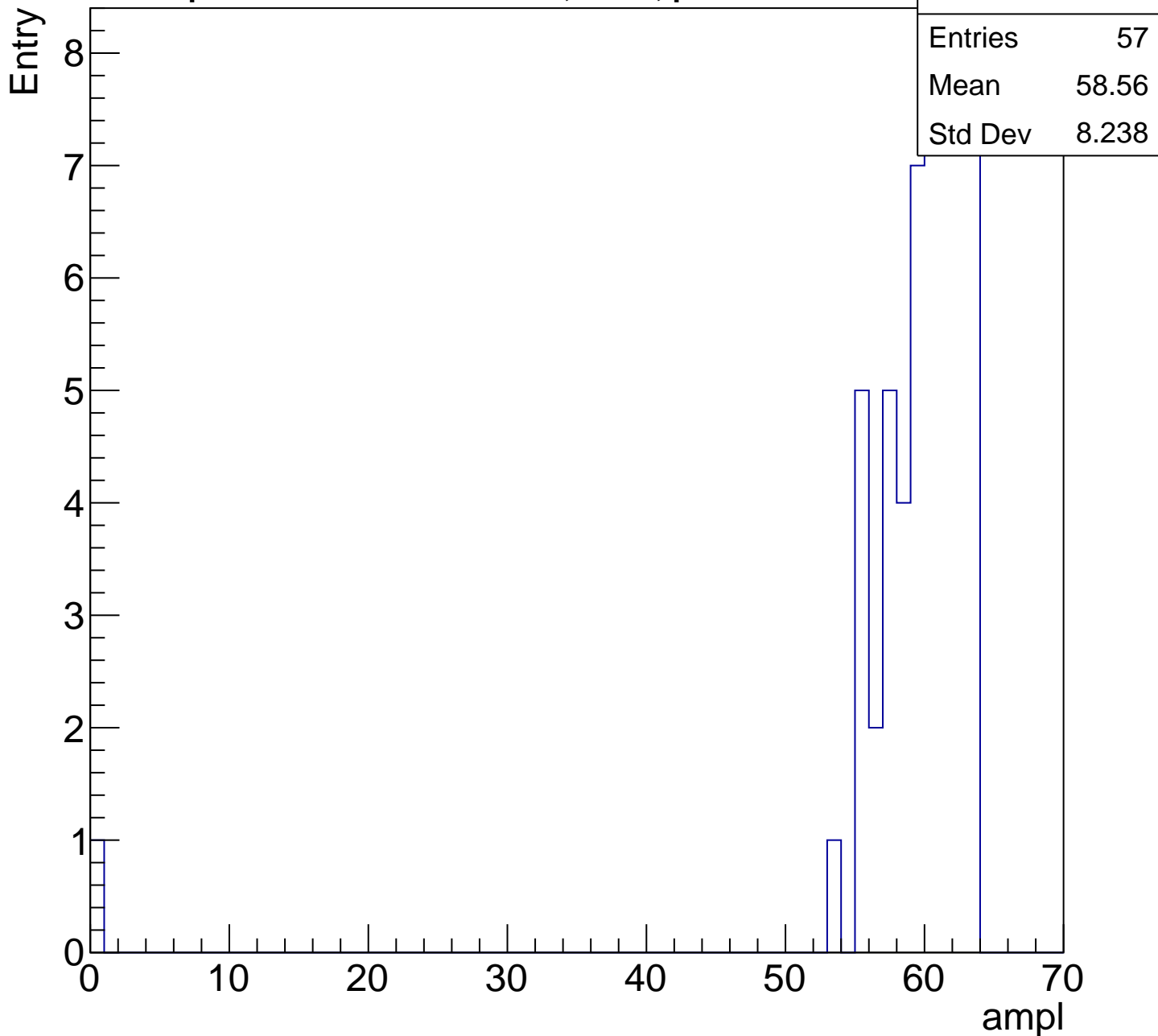
# B1L101S, U3-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U3-ch36, adc0

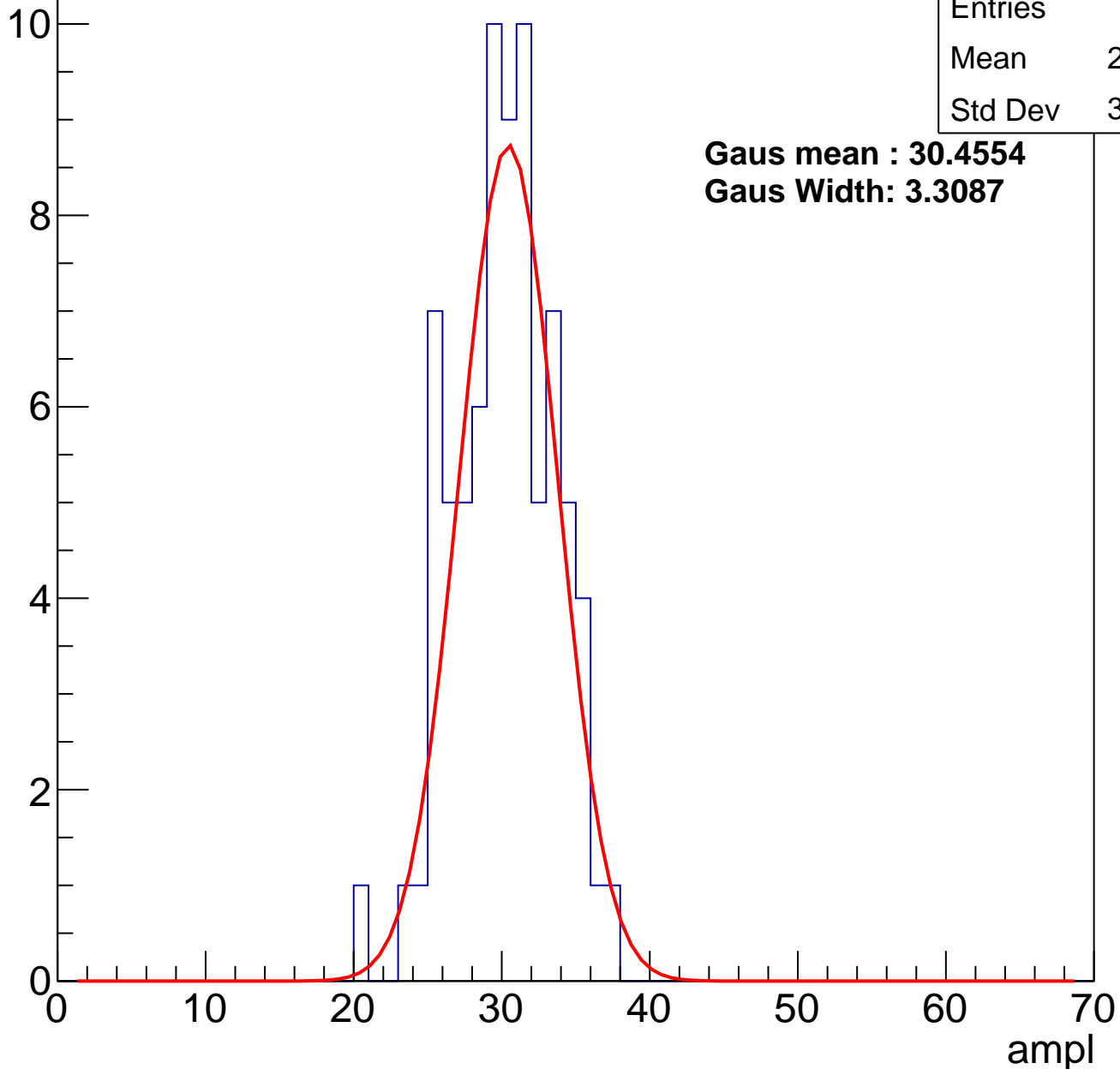
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	78
Mean	29.73
Std Dev	3.342

**Gaus mean : 30.4554**

**Gaus Width: 3.3087**

Entry



# B1L101S, U3-ch36, adc1

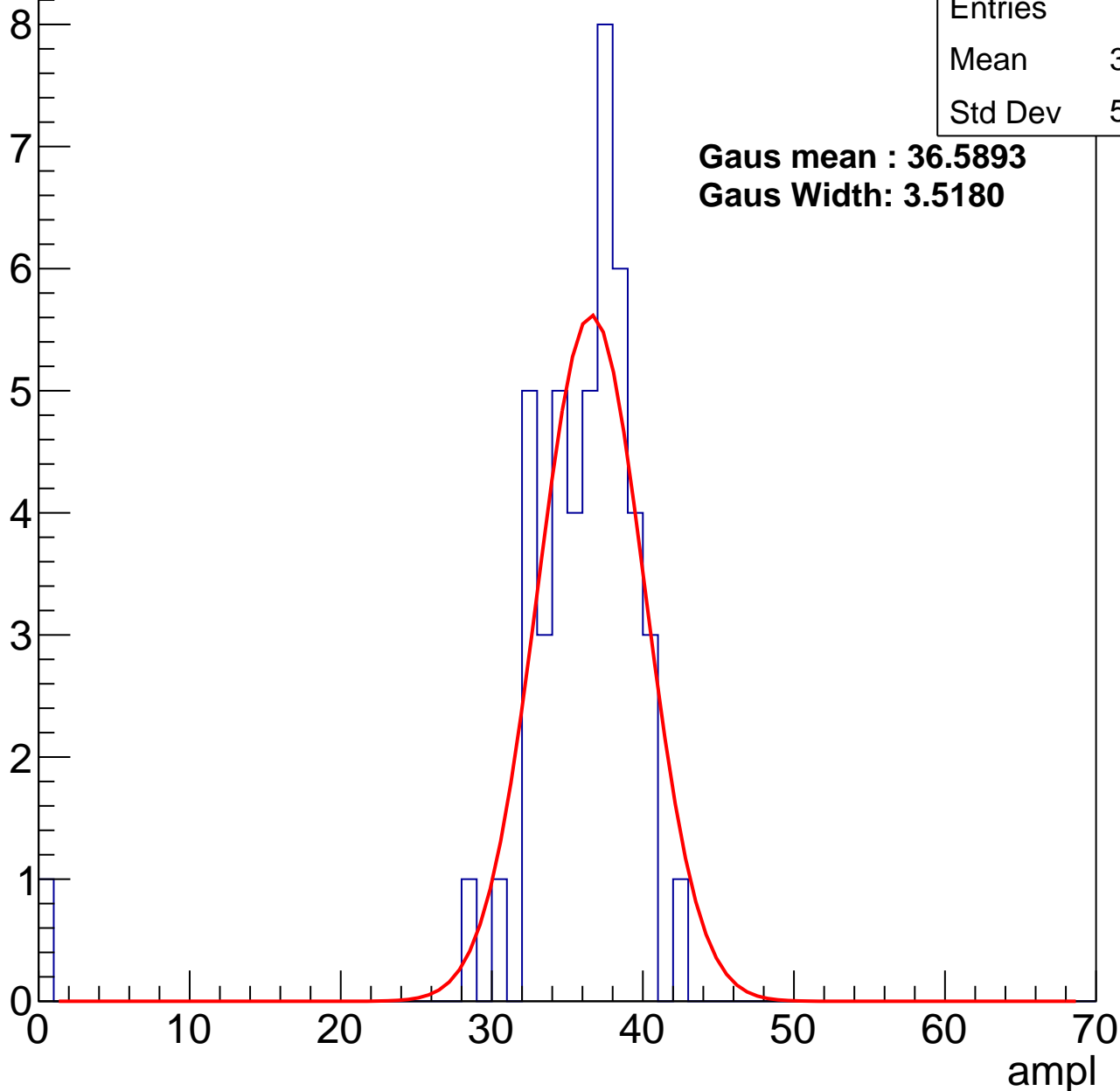
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	35.09
Std Dev	5.906

**Gaus mean : 36.5893**

**Gaus Width: 3.5180**



# B1L101S, U3-ch36, adc2

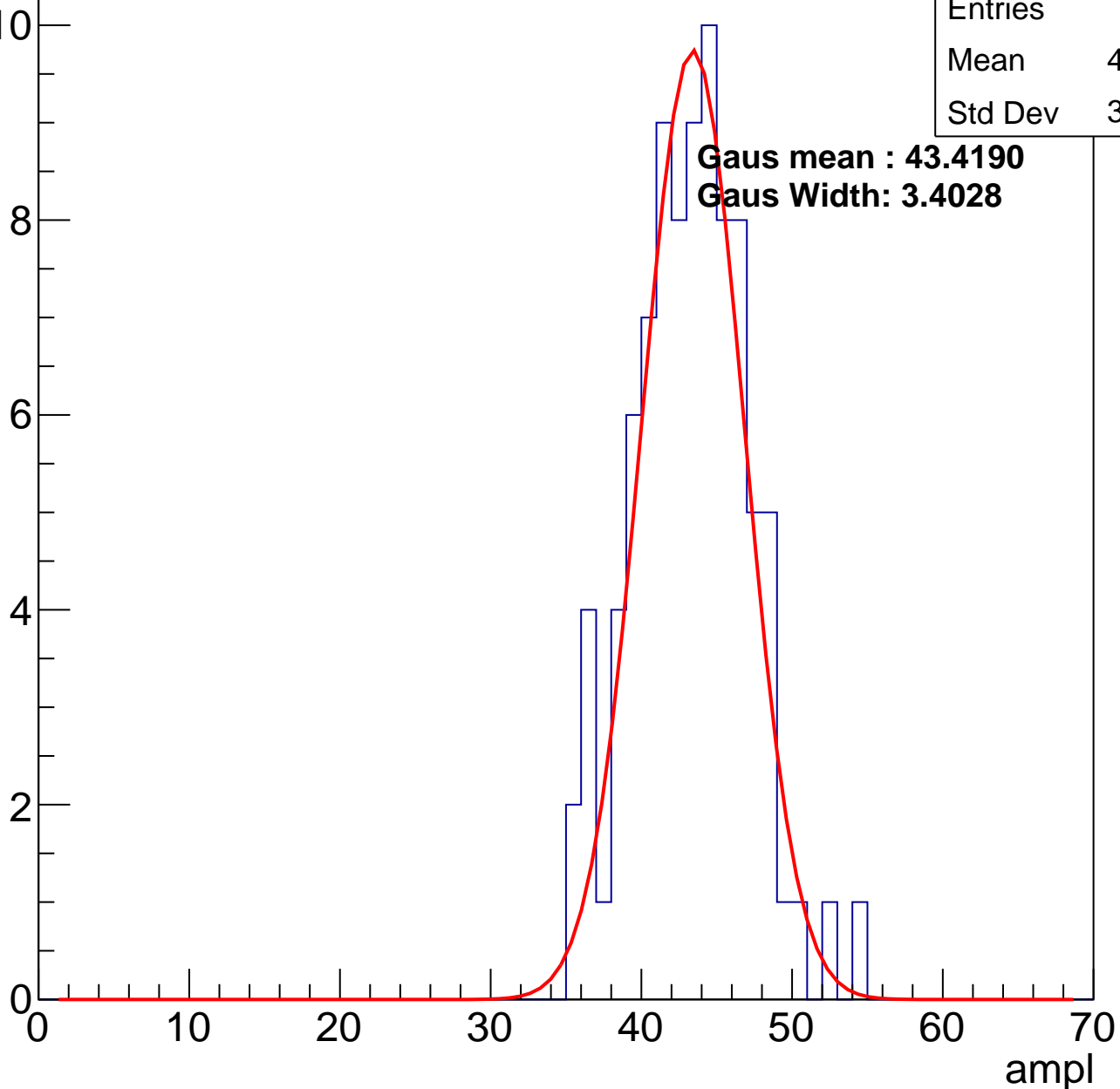
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	90
Mean	42.86
Std Dev	3.752

**Gaus mean : 43.4190**

**Gaus Width: 3.4028**

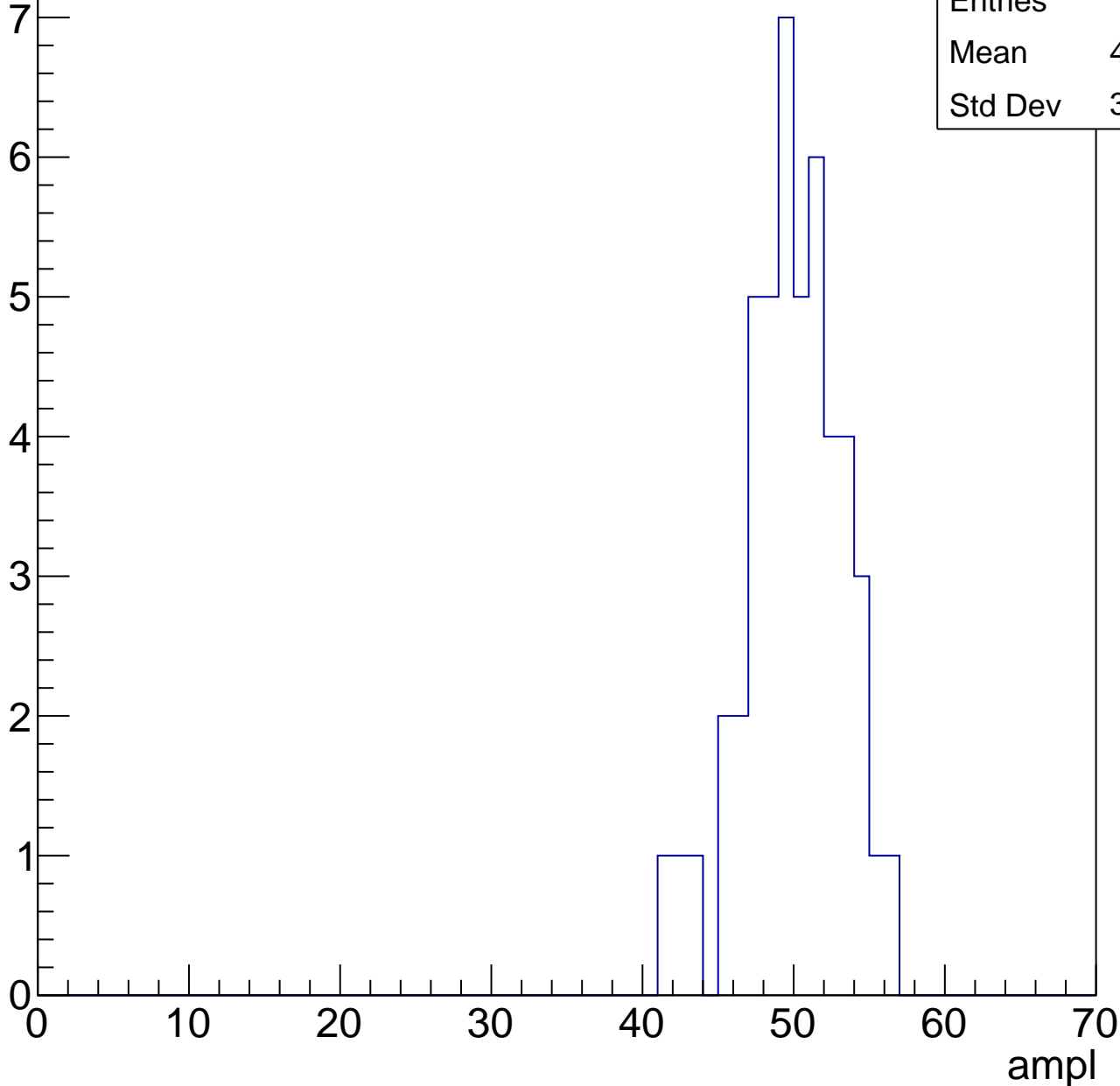


# B1L101S, U3-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

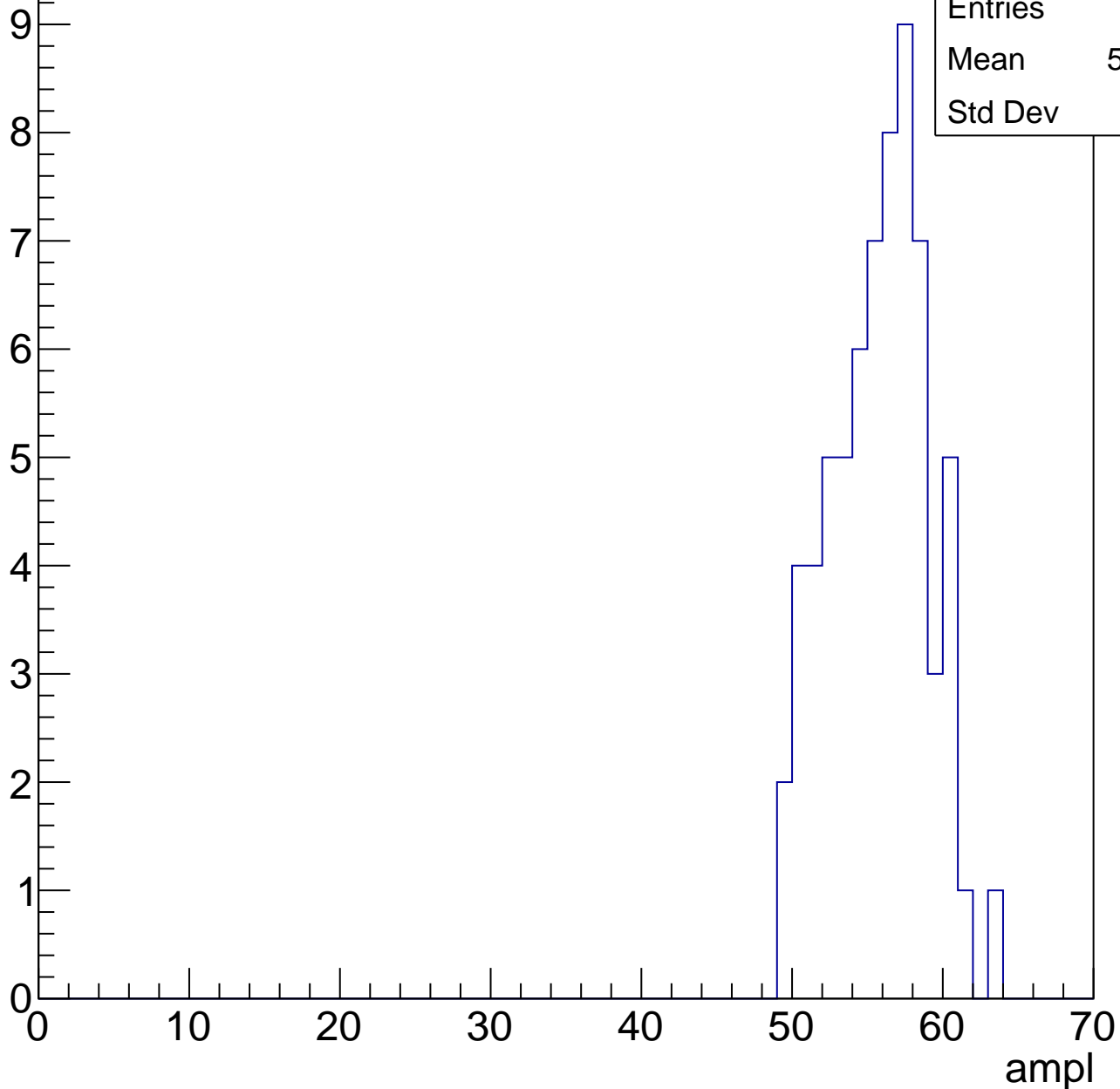
Entries	48
Mean	49.48
Std Dev	3.234



# B1L101S, U3-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



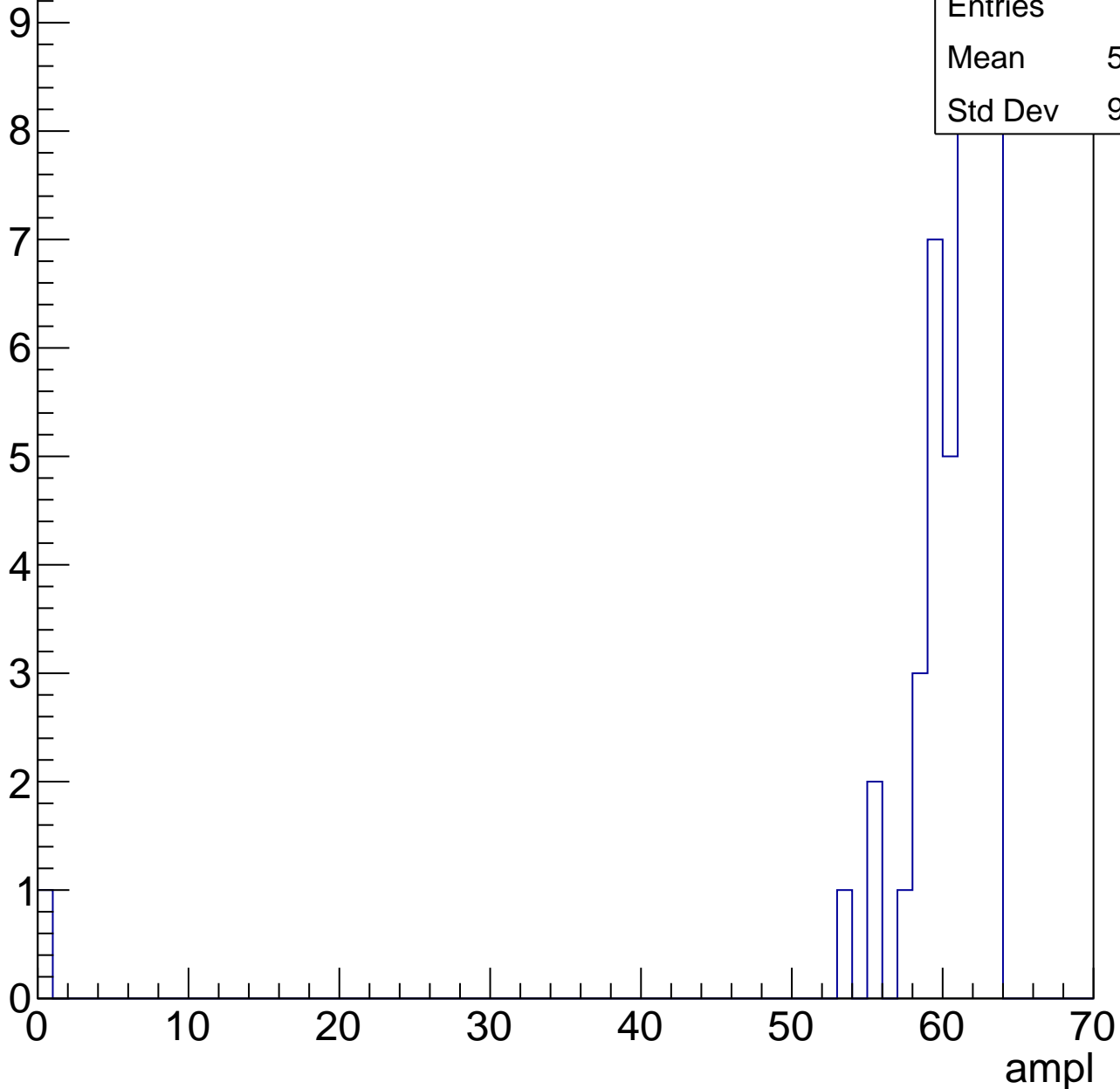
Entries	67
Mean	55.28
Std Dev	3.19

# B1L101S, U3-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

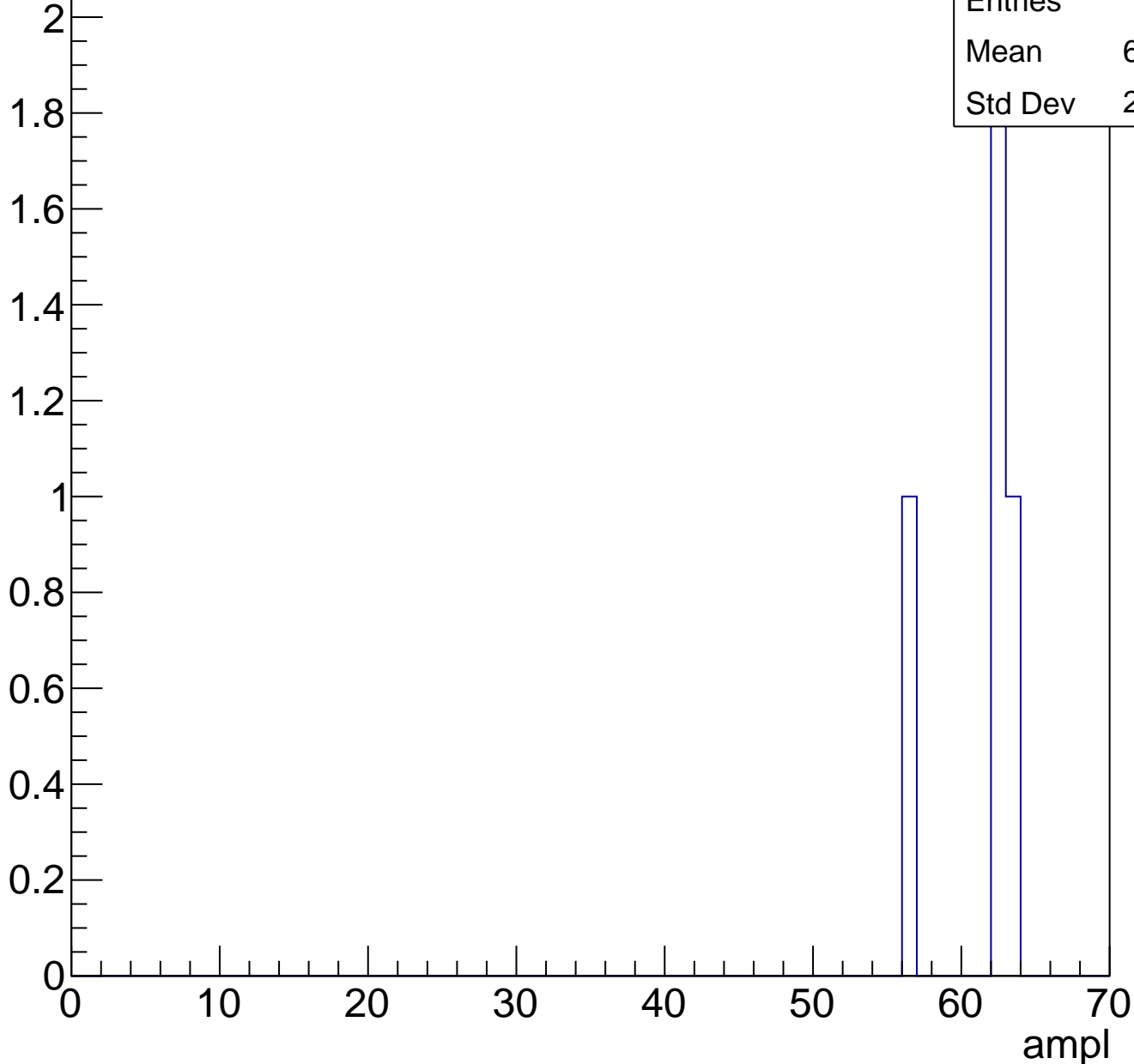
Entries	45
Mean	59.02
Std Dev	9.186



# B1L101S, U3-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch37, adc0

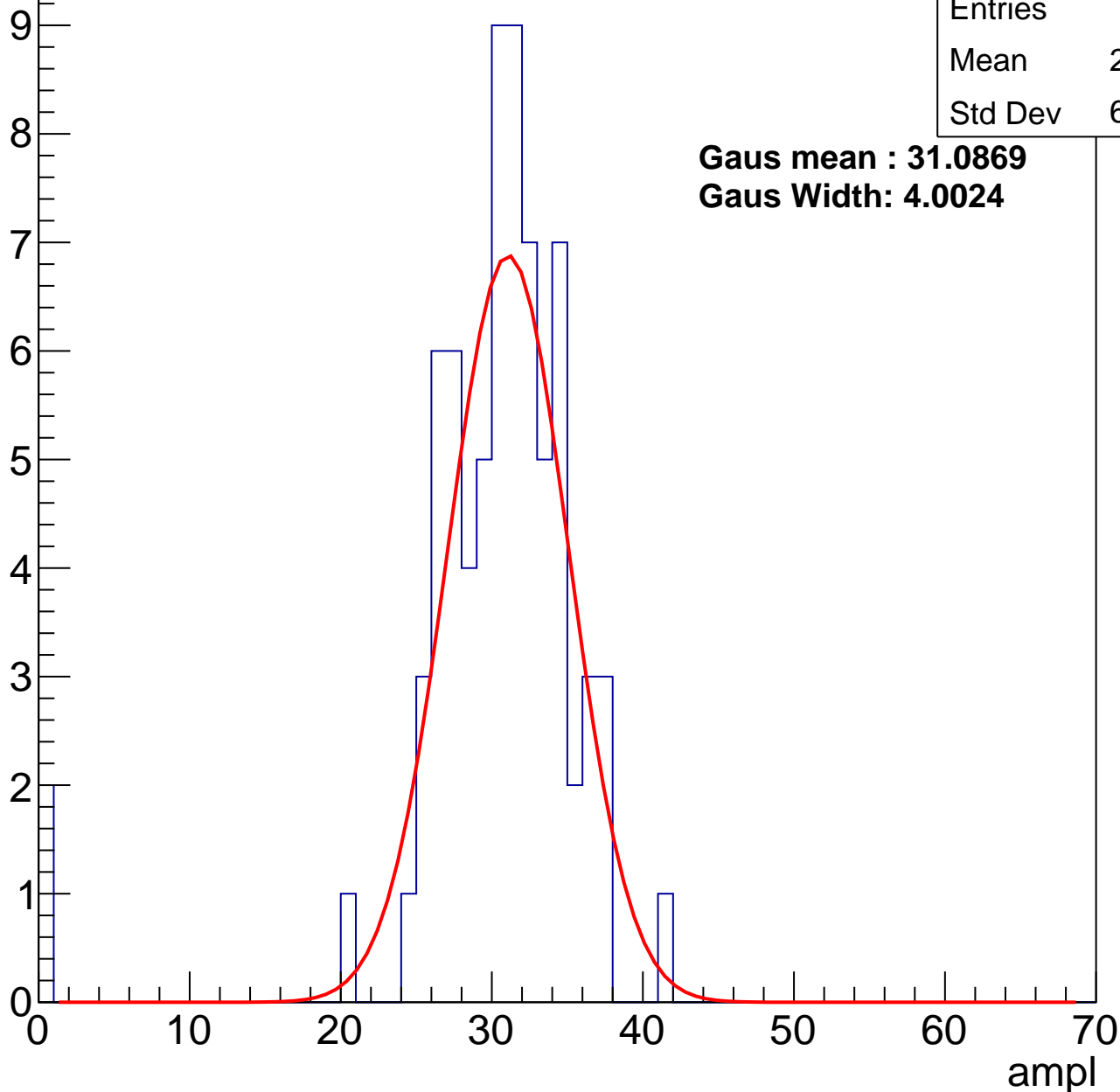
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	29.73
Std Dev	6.148

**Gaus mean : 31.0869**

**Gaus Width: 4.0024**



# B1L101S, U3-ch37, adc1

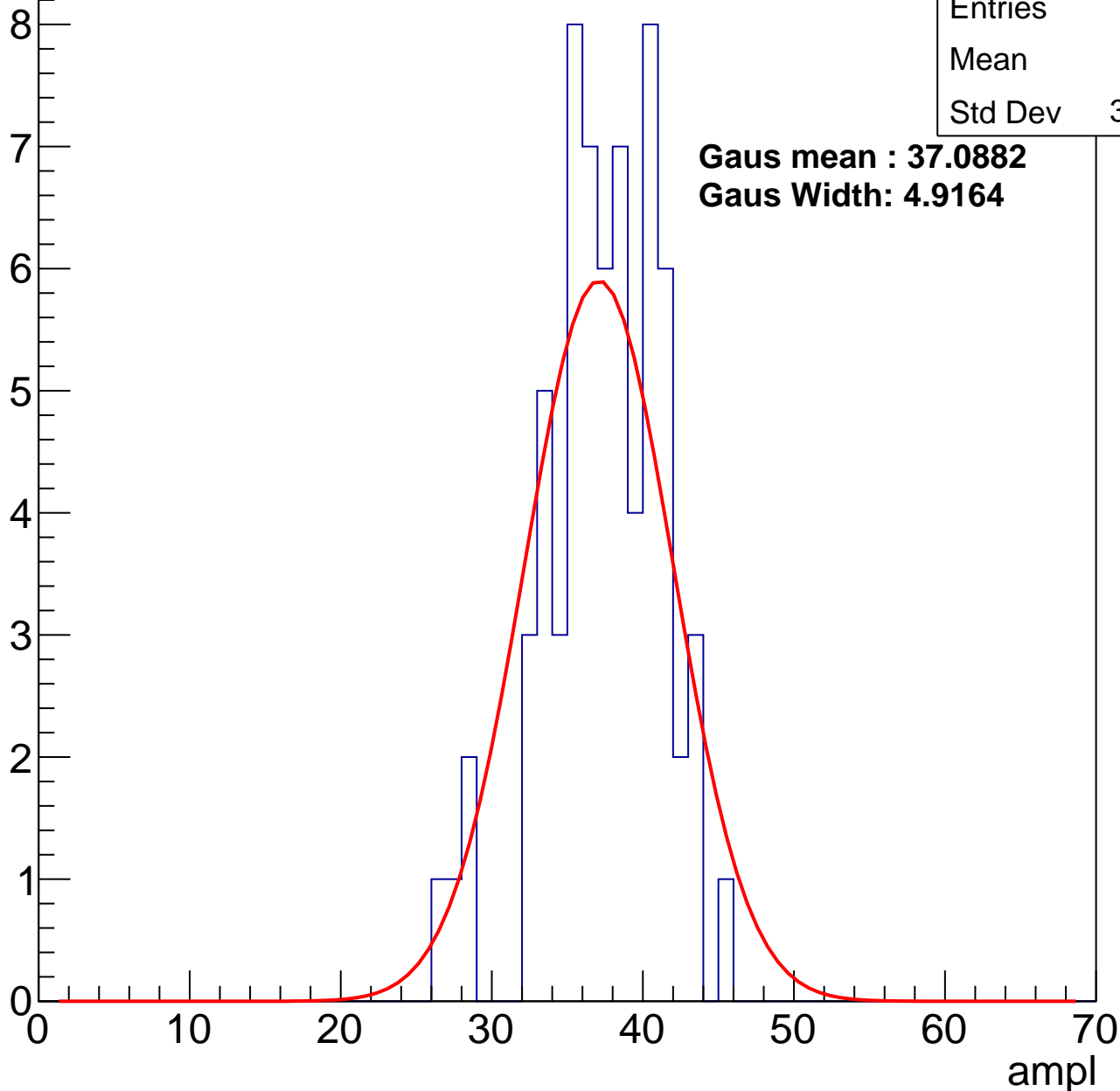
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	36.9
Std Dev	3.895

**Gaus mean : 37.0882**

**Gaus Width: 4.9164**



# B1L101S, U3-ch37, adc2

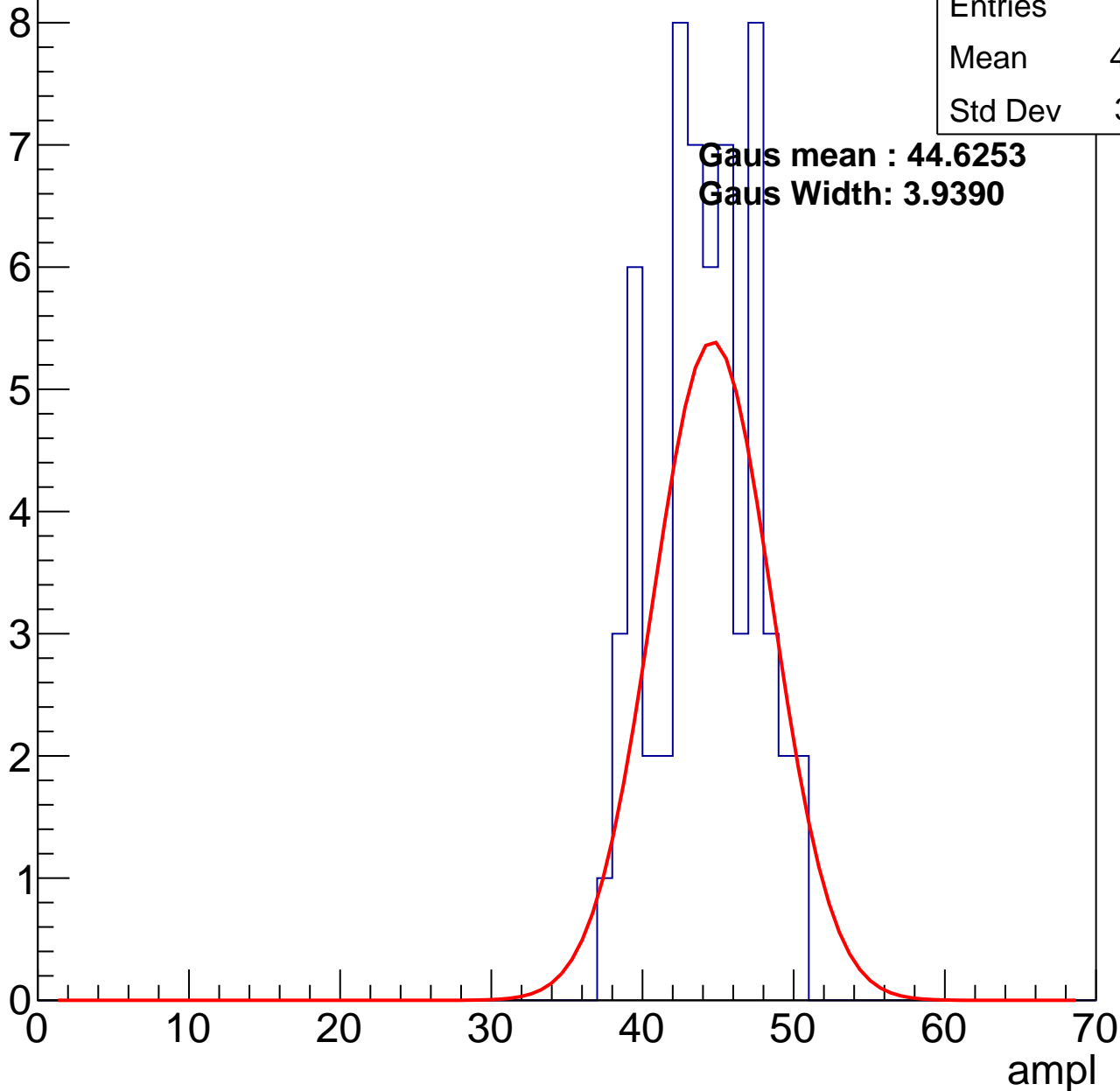
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	43.65
Std Dev	3.291

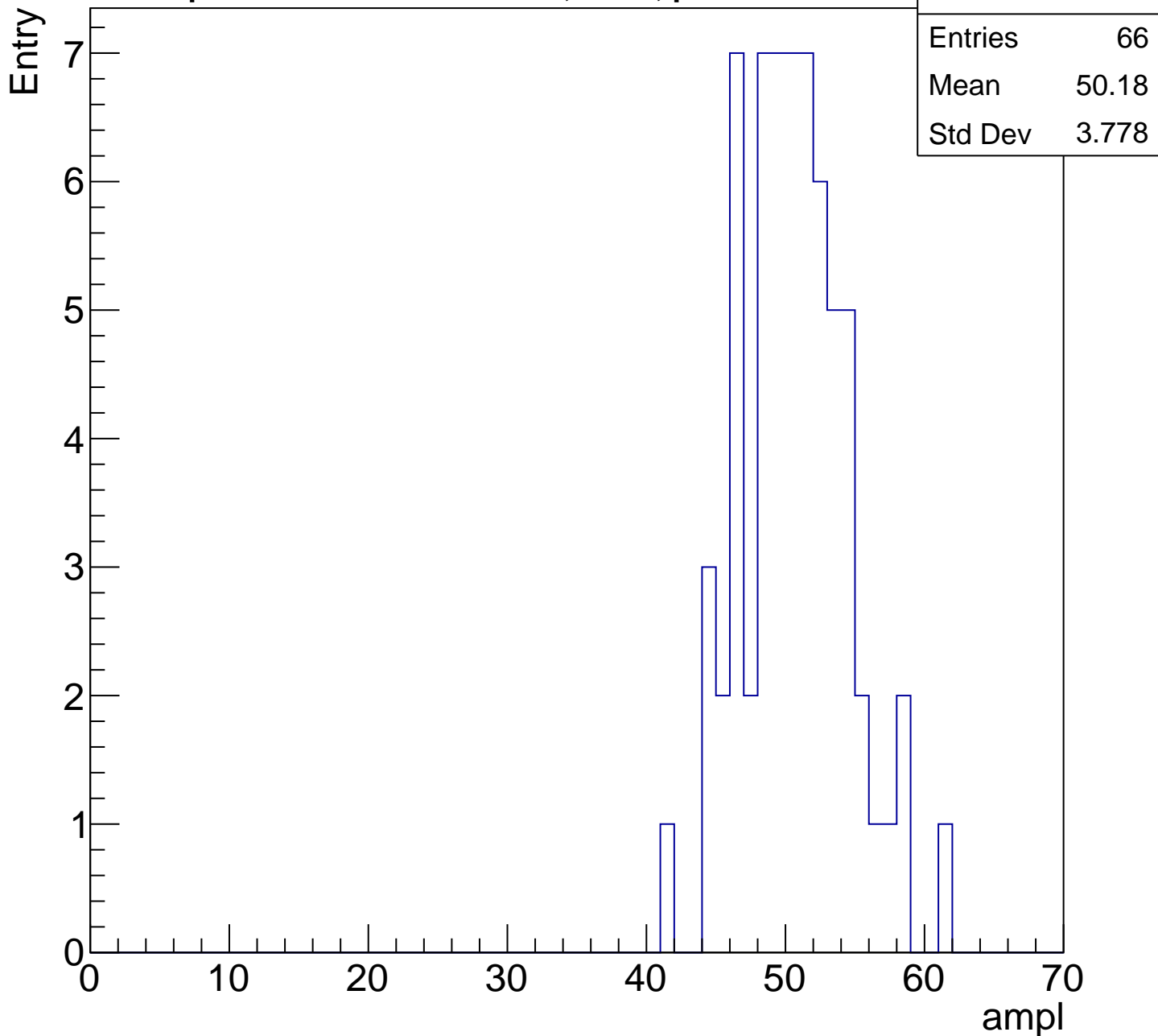
**Gaus mean : 44.6253**

**Gaus Width: 3.9390**



# B1L101S, U3-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

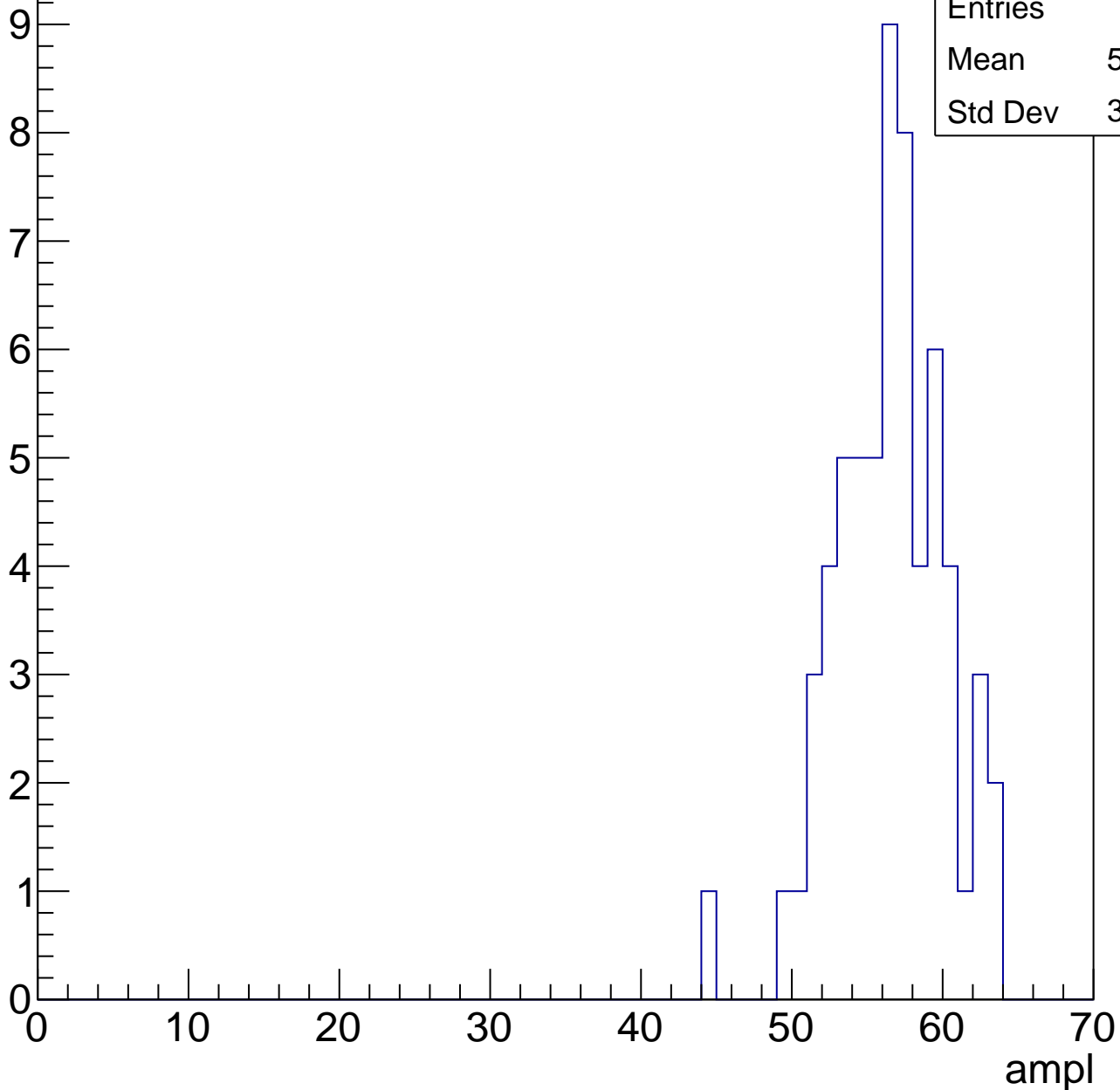


# B1L101S, U3-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	56.02
Std Dev	3.617

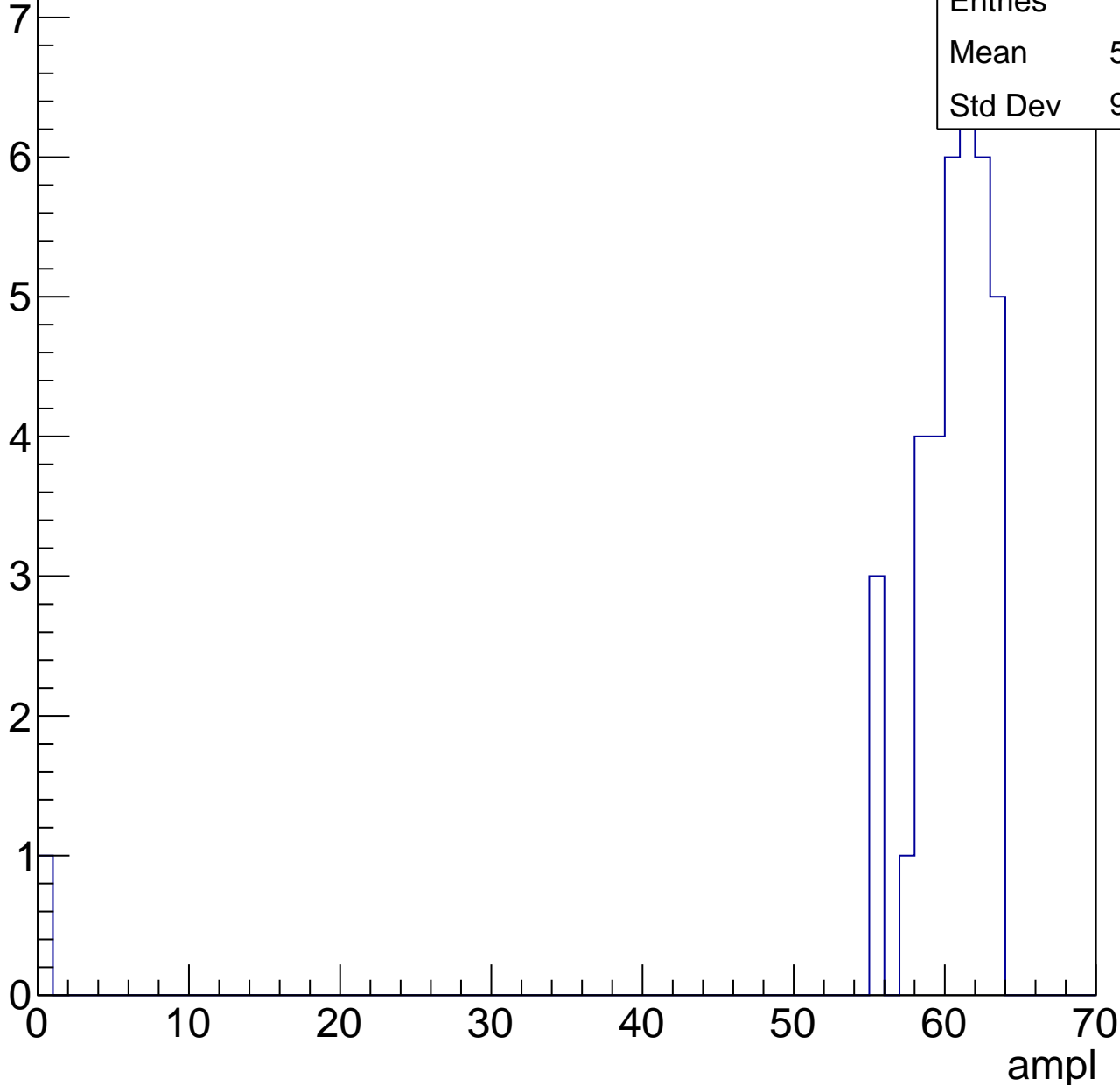


# B1L101S, U3-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	37
Mean	58.49
Std Dev	9.994



# B1L101S, U3-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch38, adc0

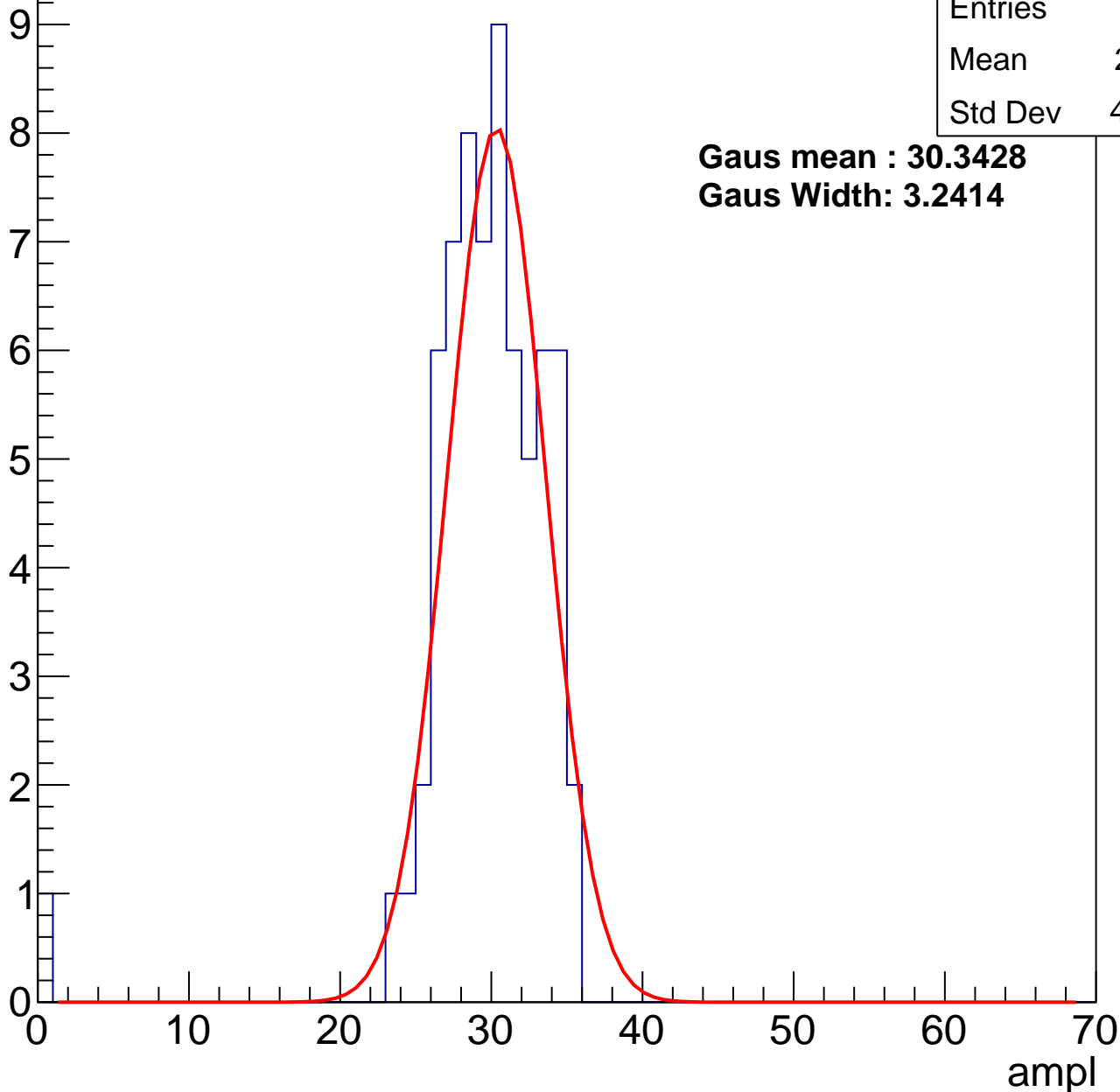
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	29.21
Std Dev	4.599

**Gaus mean : 30.3428**

**Gaus Width: 3.2414**



# B1L101S, U3-ch38, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	81
Mean	36.27
Std Dev	5.513

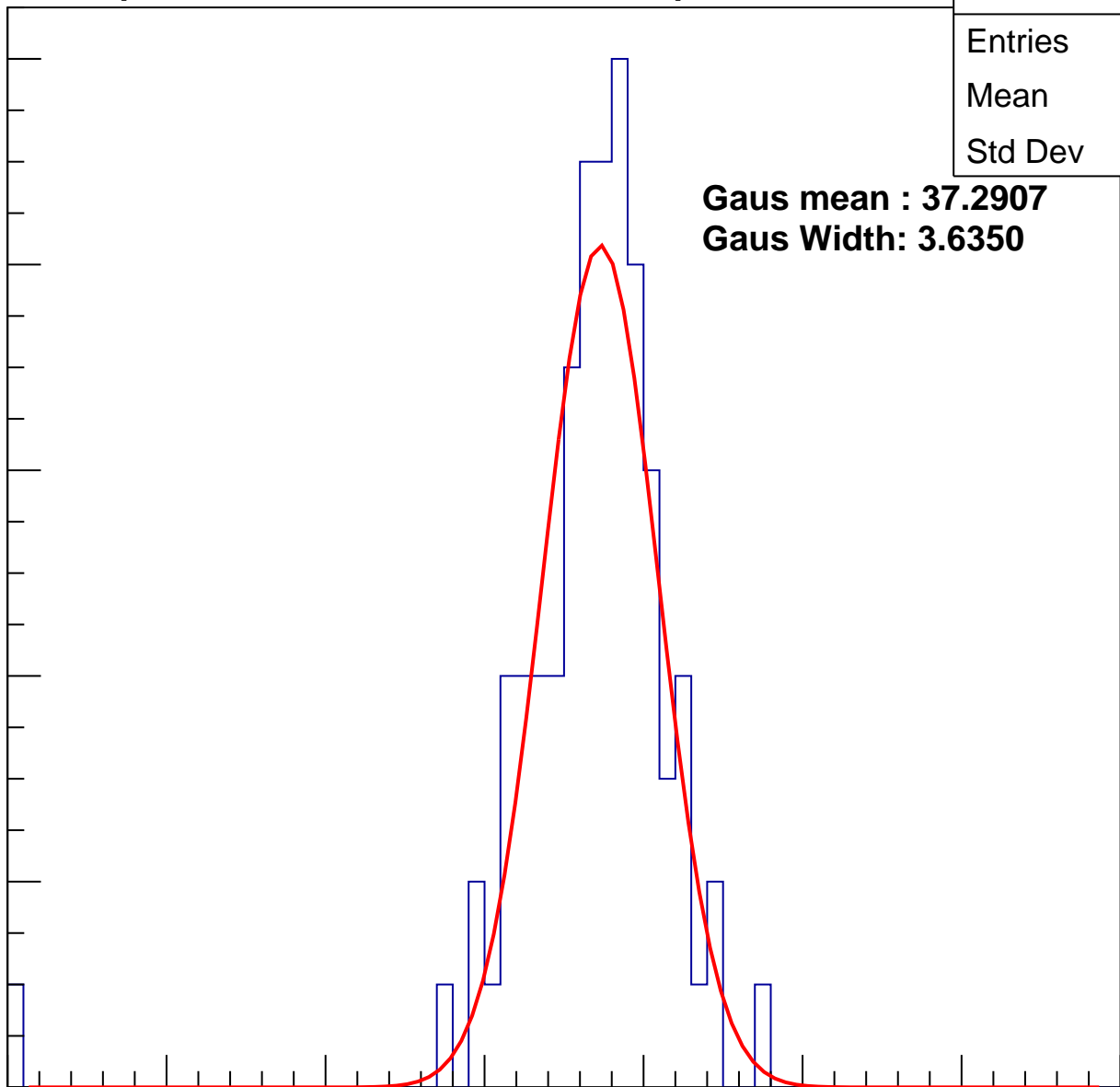
**Gaus mean : 37.2907**  
**Gaus Width: 3.6350**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U3-ch38, adc2

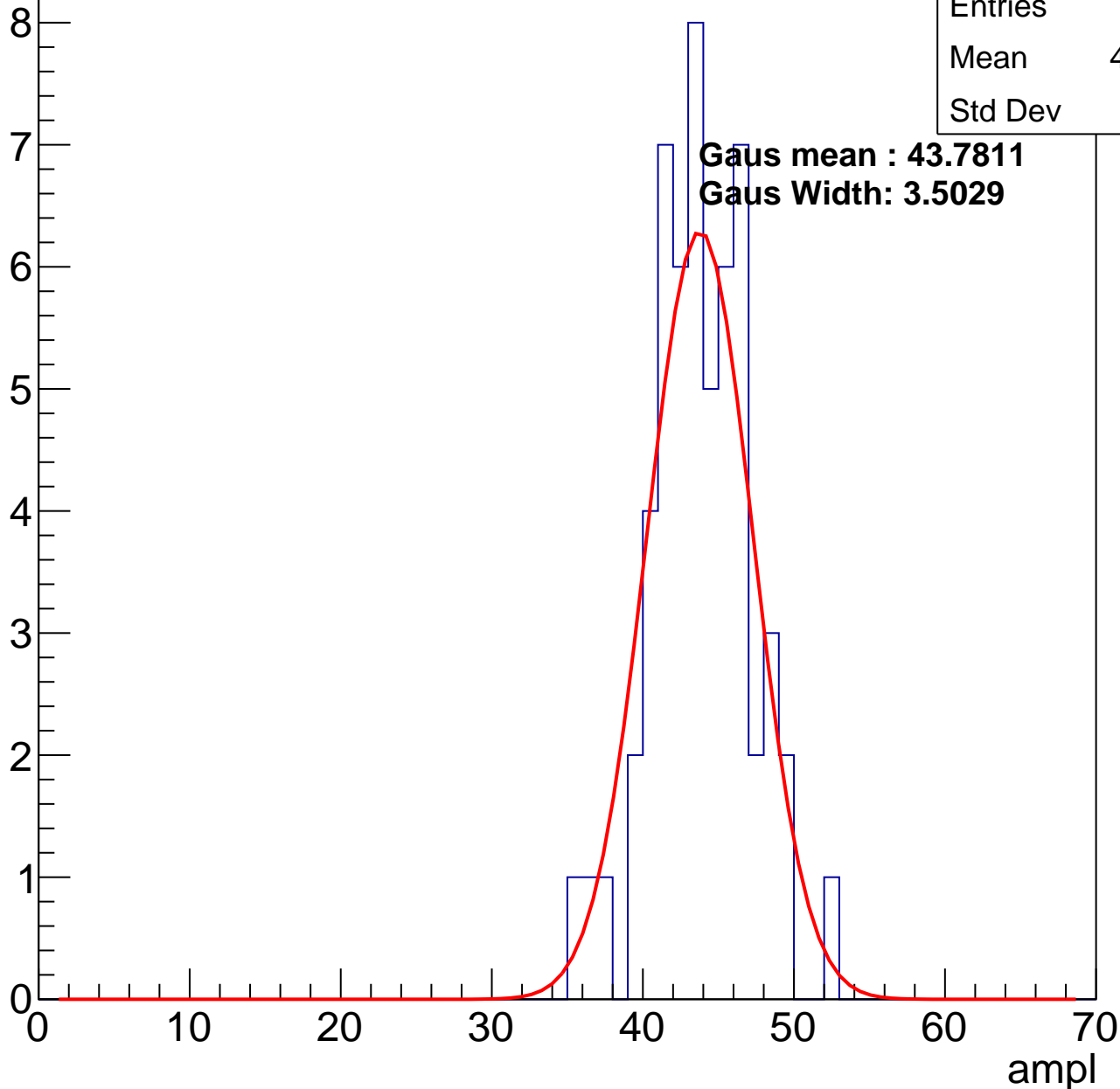
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	43.38
Std Dev	3.26

**Gaus mean : 43.7811**

**Gaus Width: 3.5029**

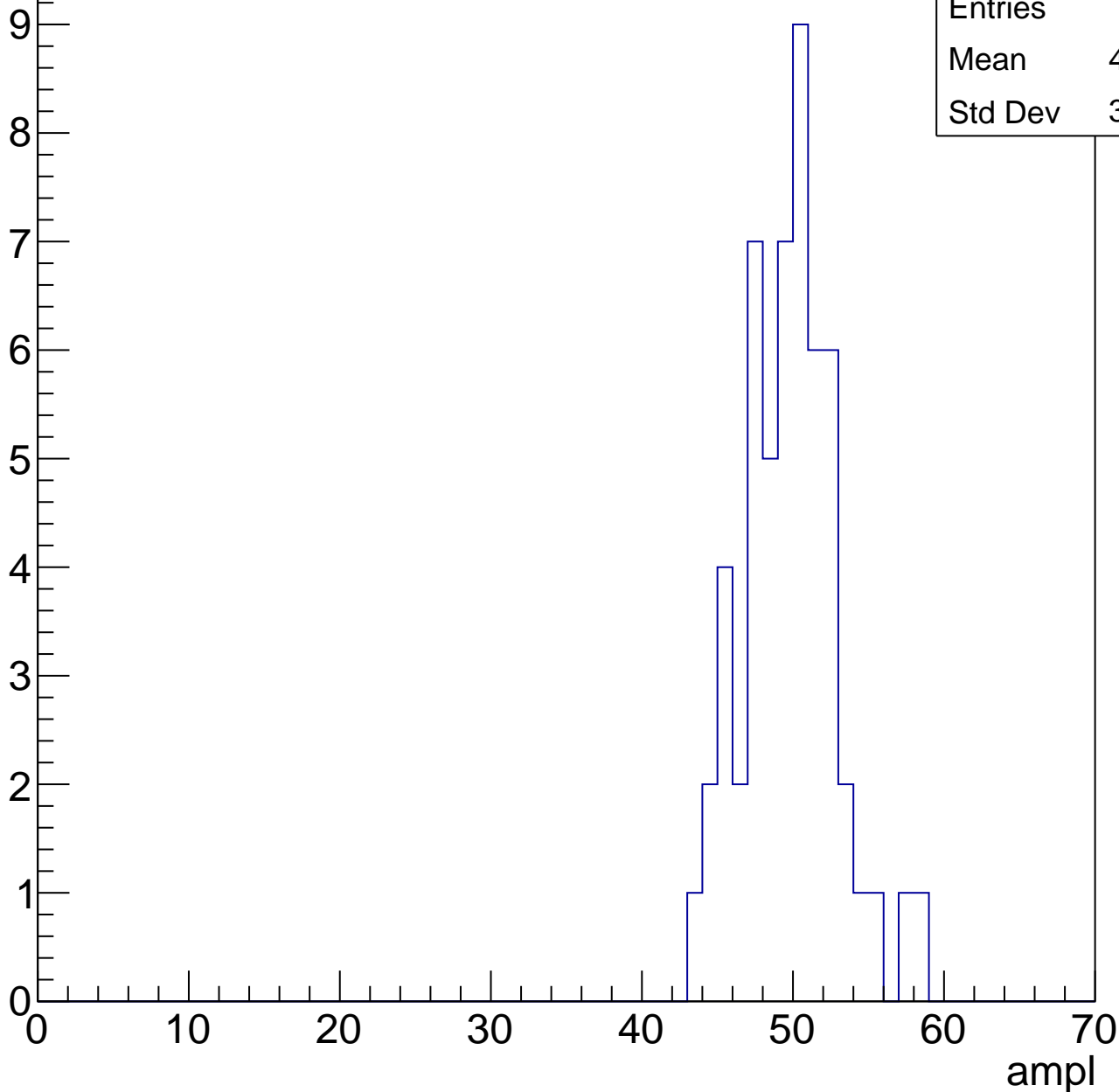


# B1L101S, U3-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	49.33
Std Dev	3.075

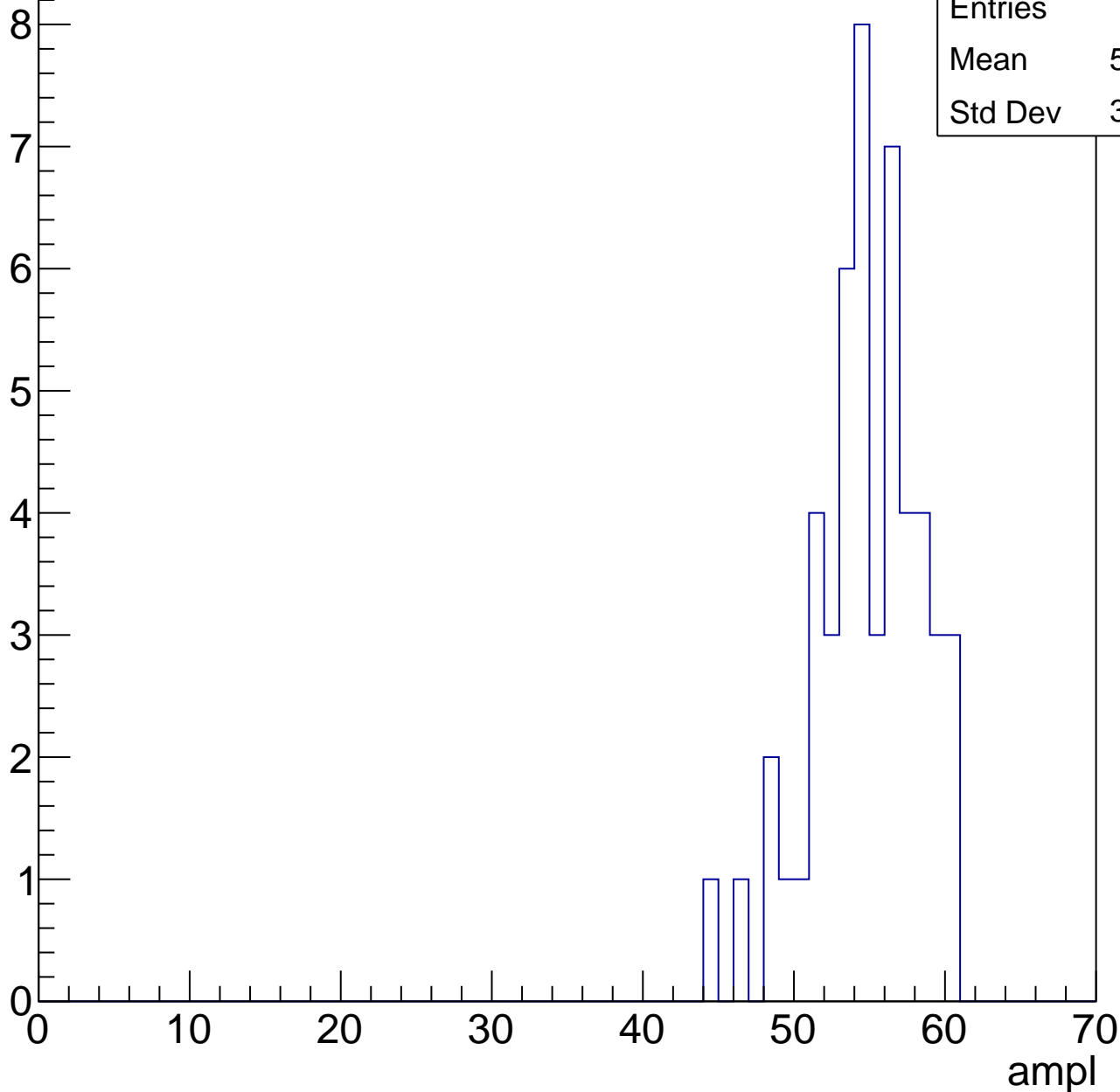


# B1L101S, U3-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	54.29
Std Dev	3.544

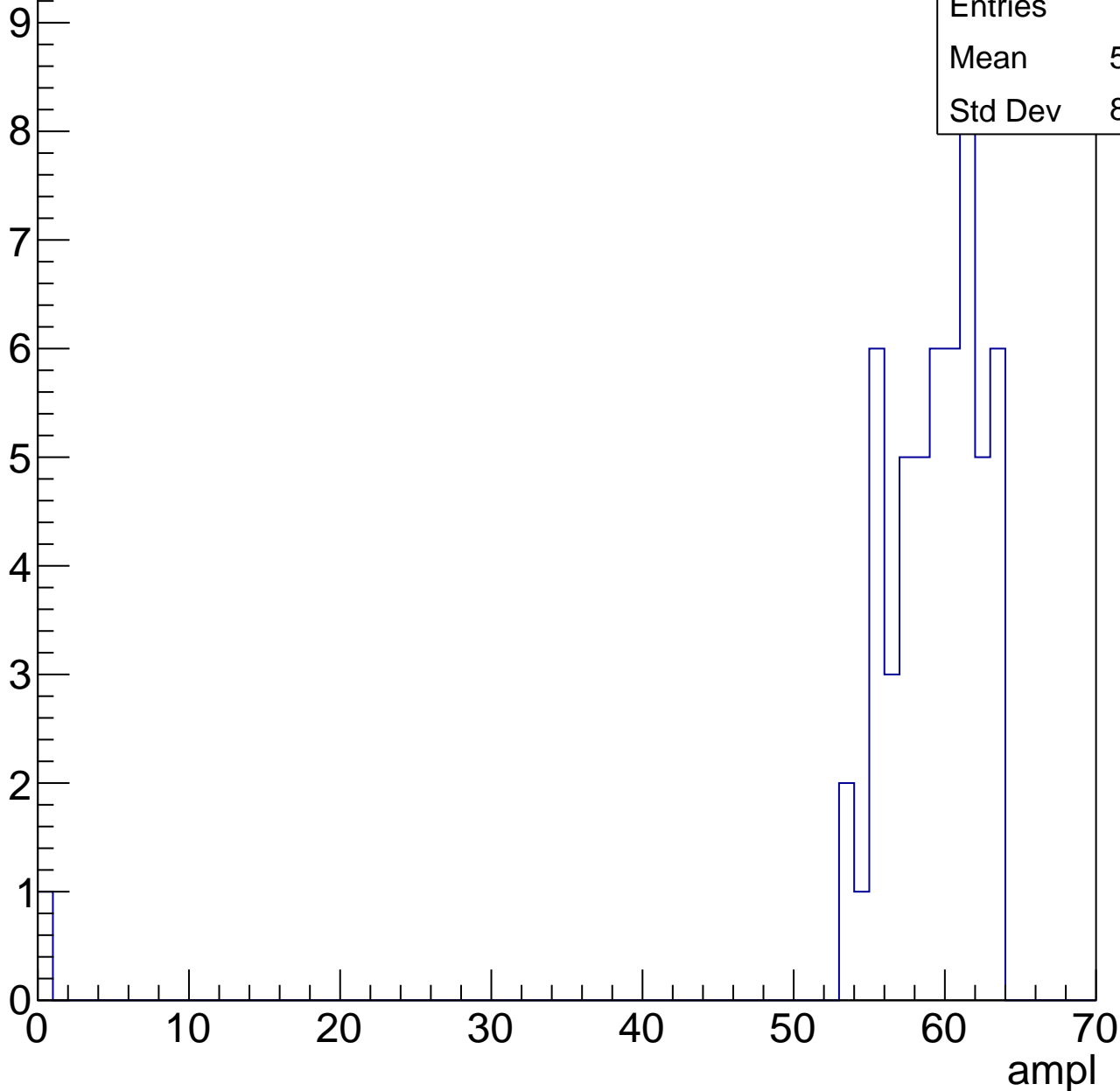


# B1L101S, U3-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	57.89
Std Dev	8.357

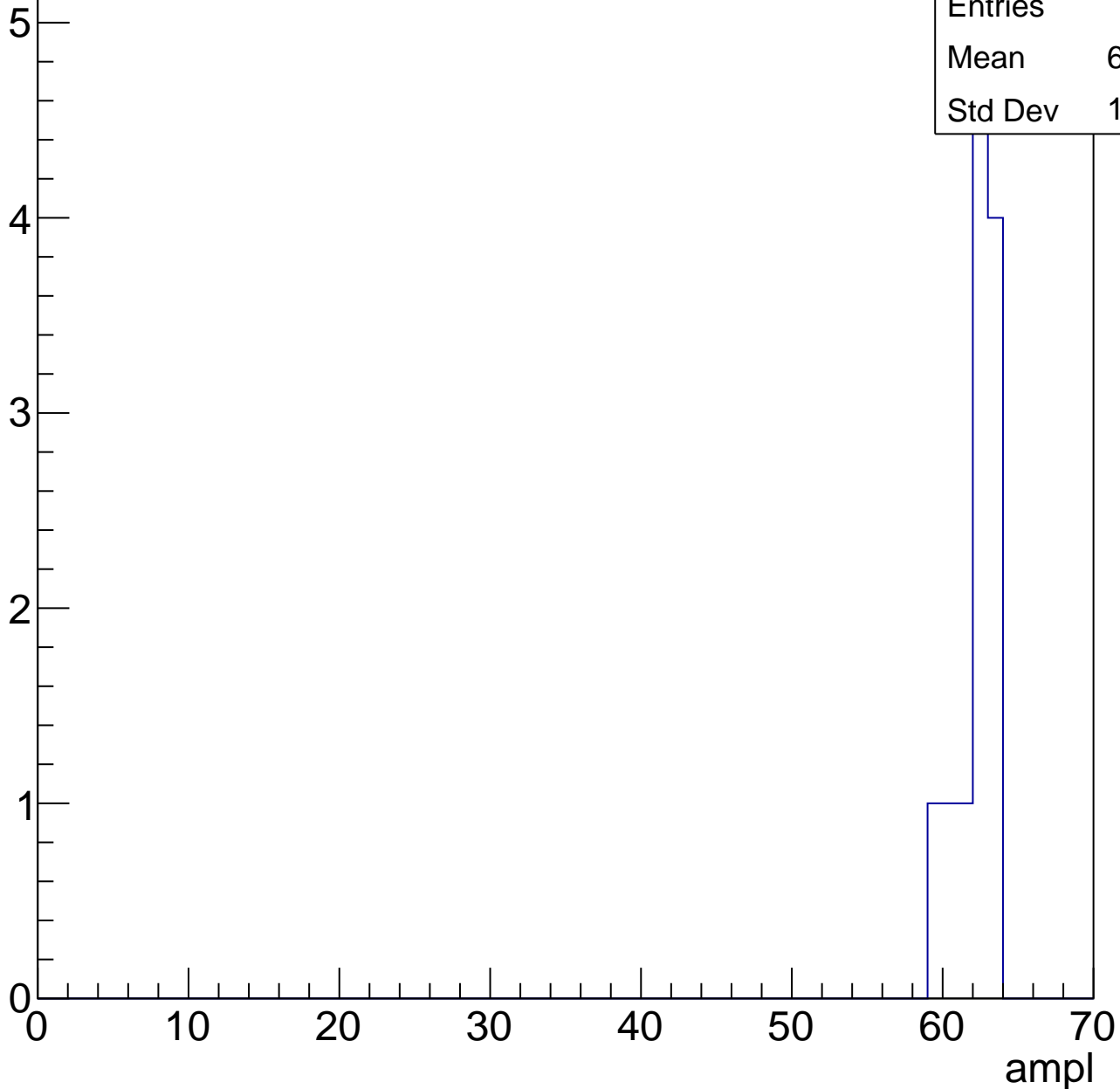


# B1L101S, U3-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	12
Mean	61.83
Std Dev	1.213





# B1L101S, U3-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch39, adc0

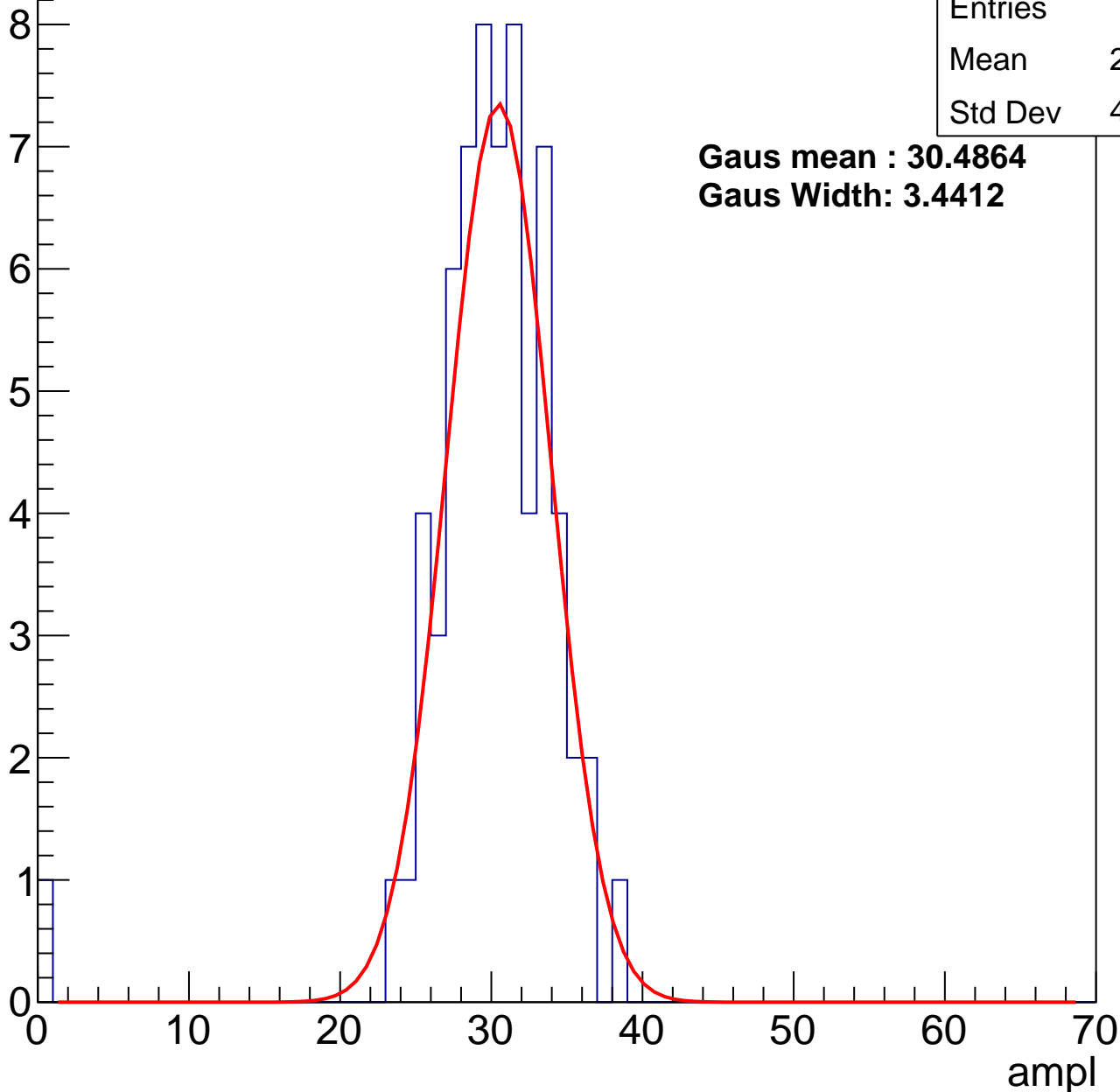
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	29.52
Std Dev	4.837

**Gaus mean : 30.4864**

**Gaus Width: 3.4412**



# B1L101S, U3-ch39, adc1

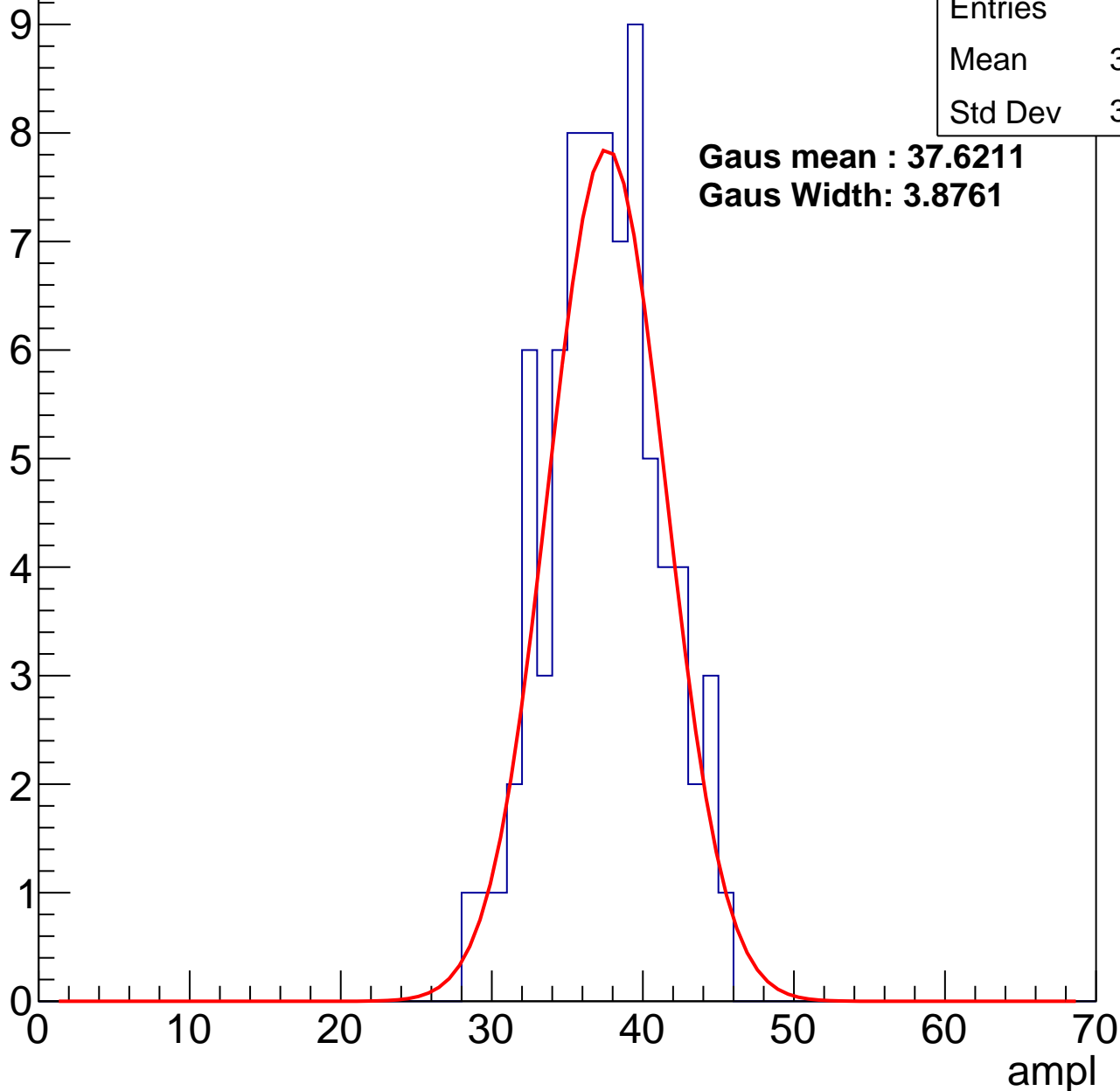
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	36.96
Std Dev	3.719

**Gaus mean : 37.6211**

**Gaus Width: 3.8761**



# B1L101S, U3-ch39, adc2

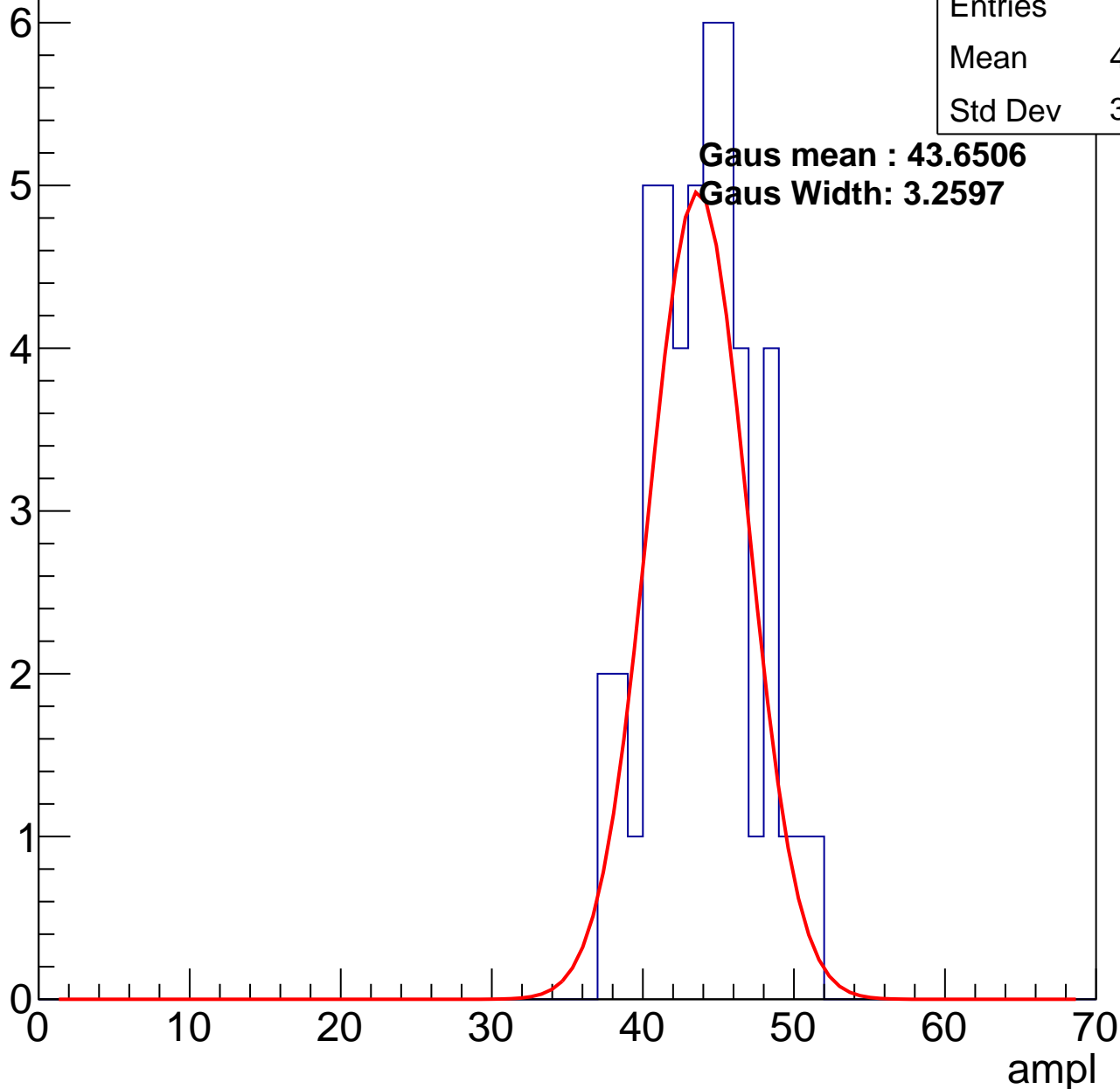
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	43.42
Std Dev	3.322

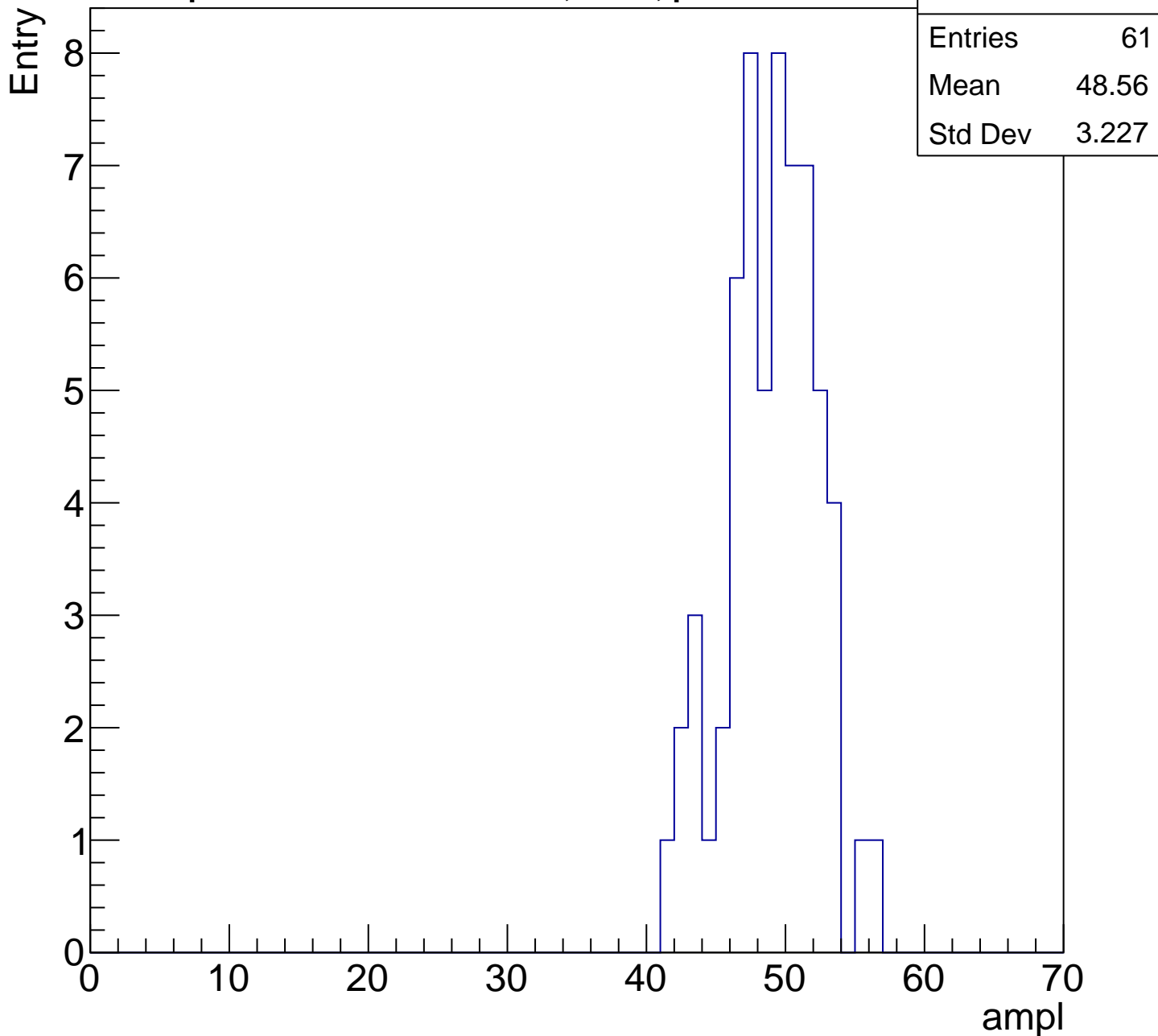
**Gaus mean : 43.6506**

**Gaus Width: 3.2597**



# B1L101S, U3-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

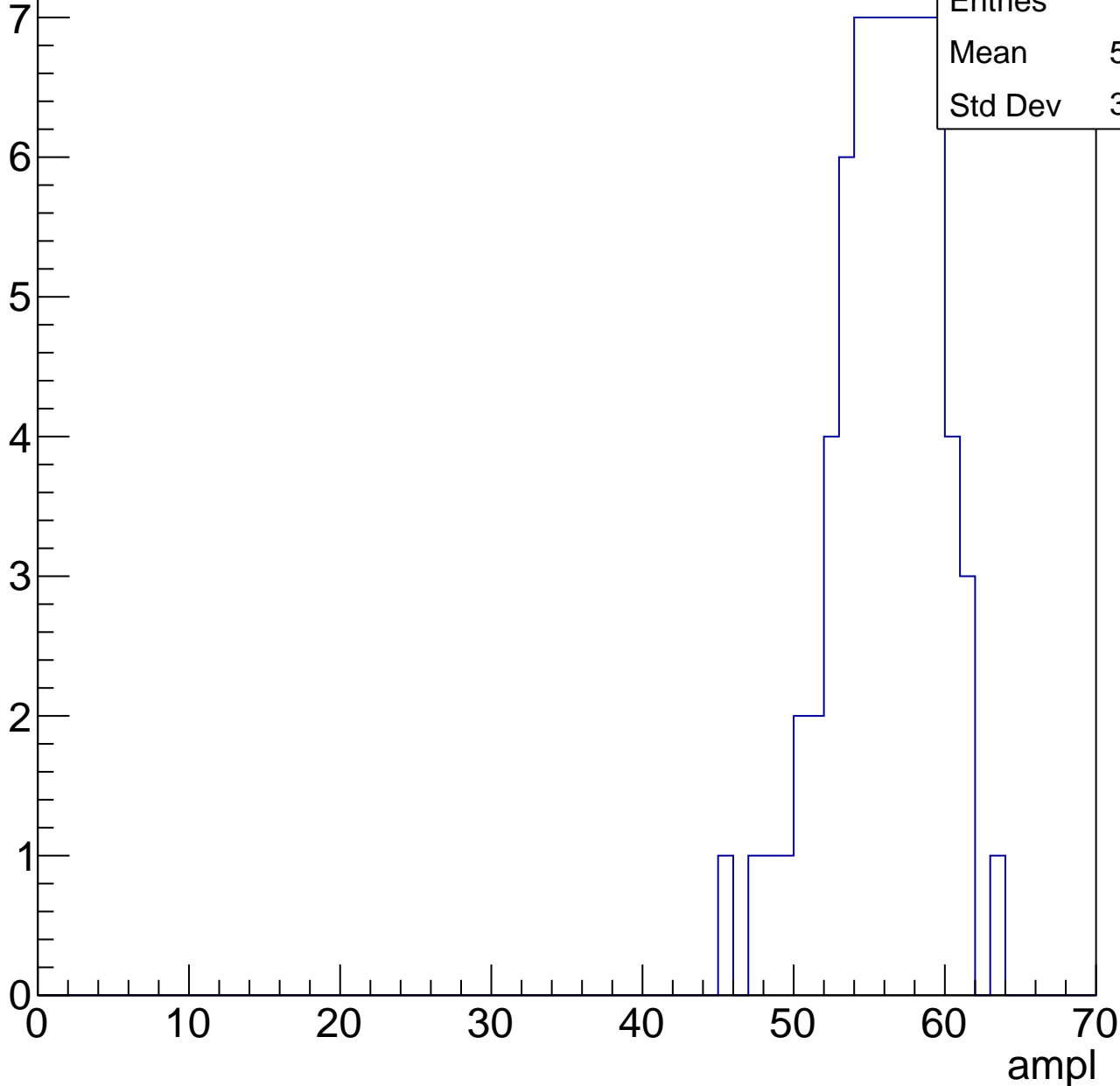


# B1L101S, U3-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	55.53
Std Dev	3.558

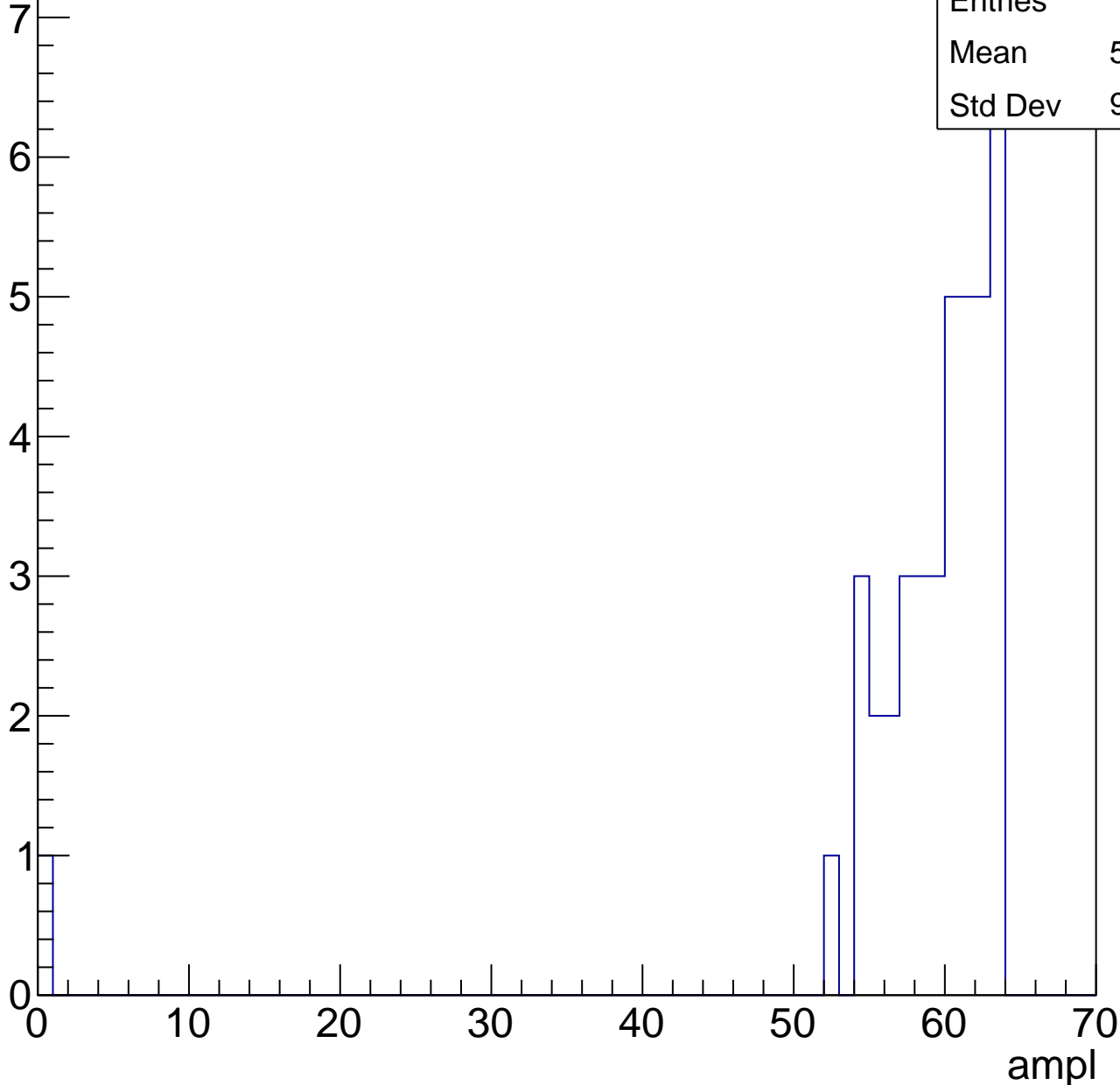


# B1L101S, U3-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	40
Mean	57.85
Std Dev	9.746

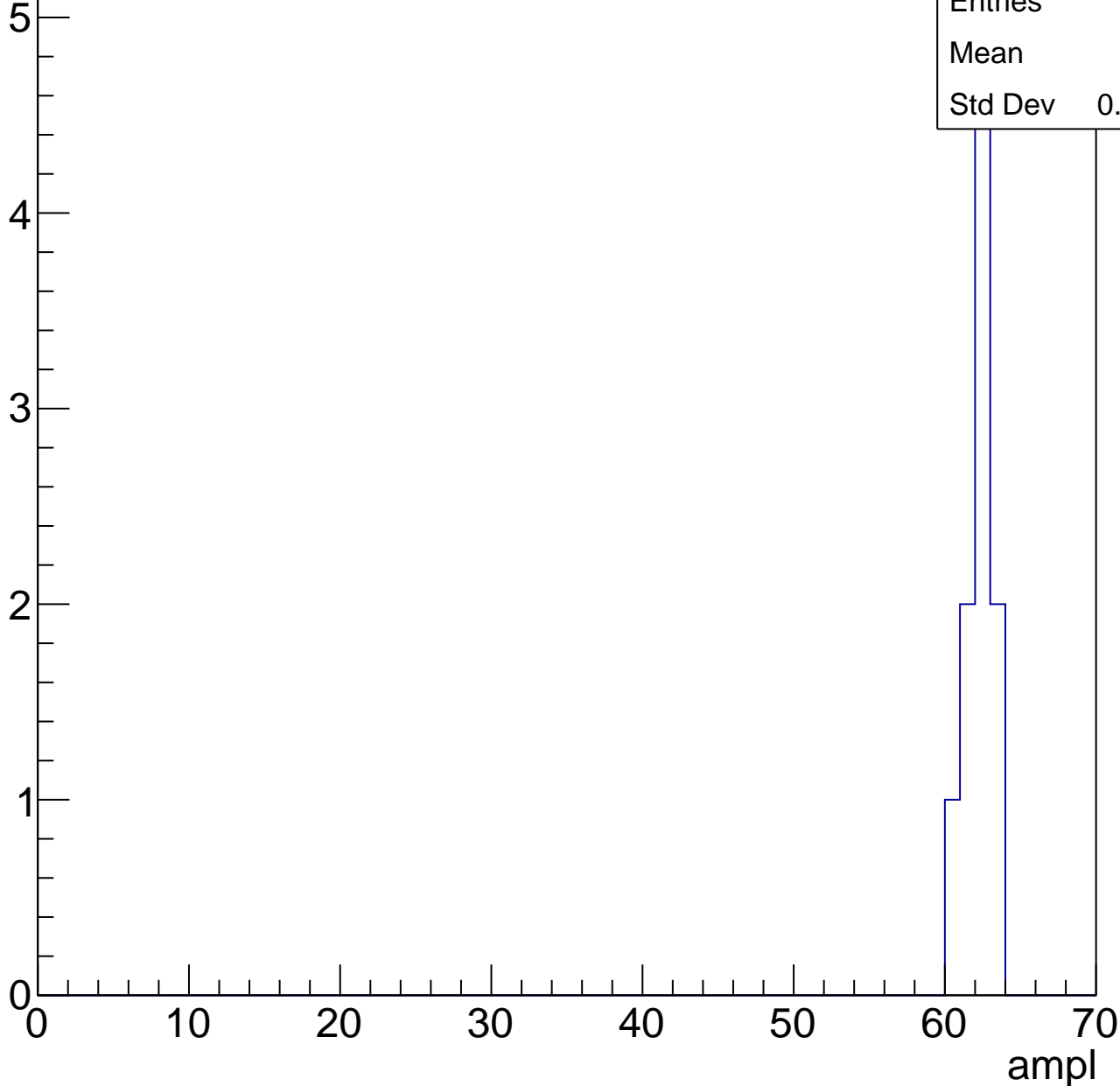


# B1L101S, U3-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	10
Mean	61.8
Std Dev	0.8718





# B1L101S, U3-ch39, adc7

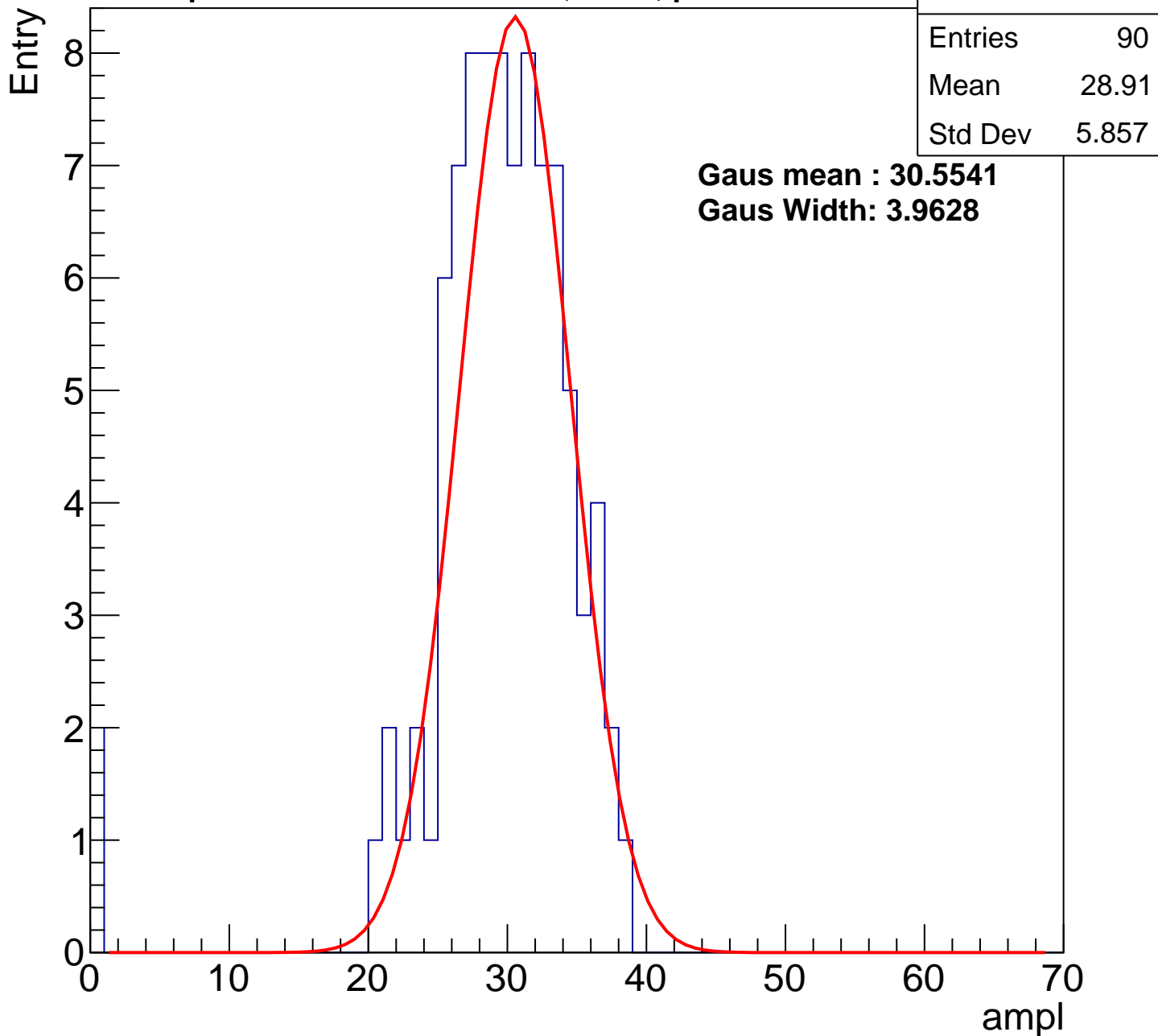
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch40, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch40, adc1

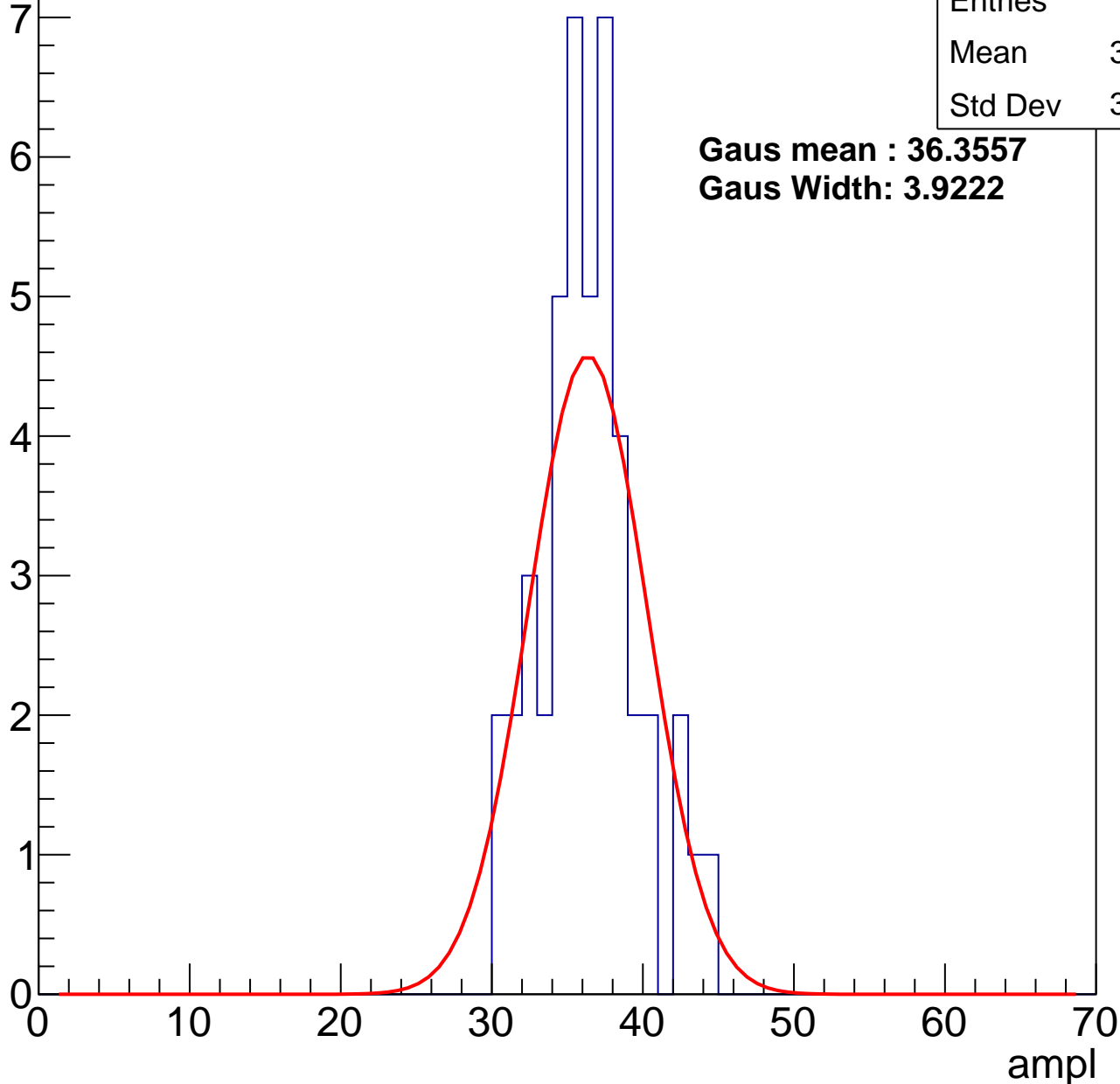
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	45
Mean	35.98
Std Dev	3.242

**Gaus mean : 36.3557**

**Gaus Width: 3.9222**



# B1L101S, U3-ch40, adc2

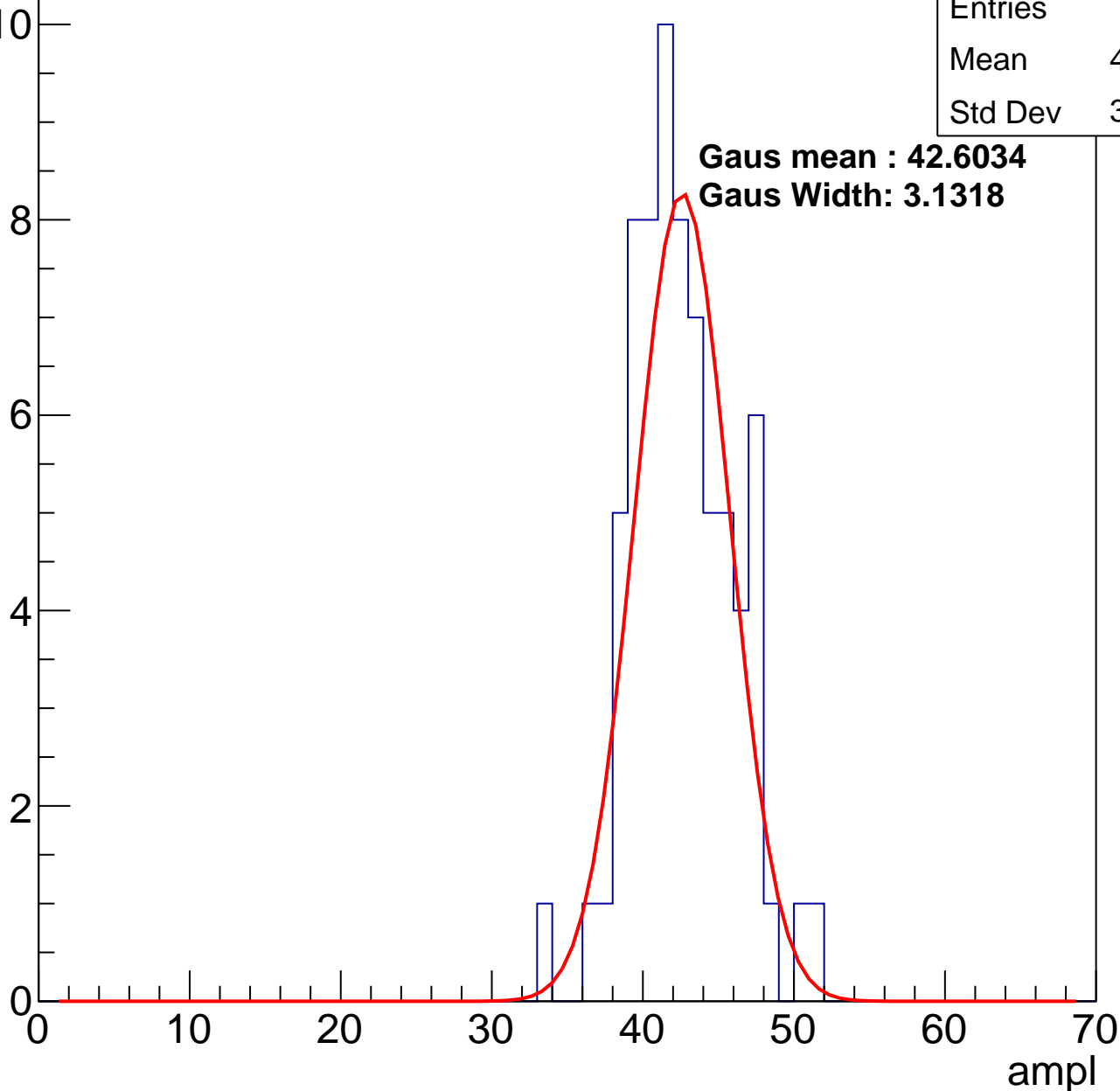
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	42.15
Std Dev	3.336

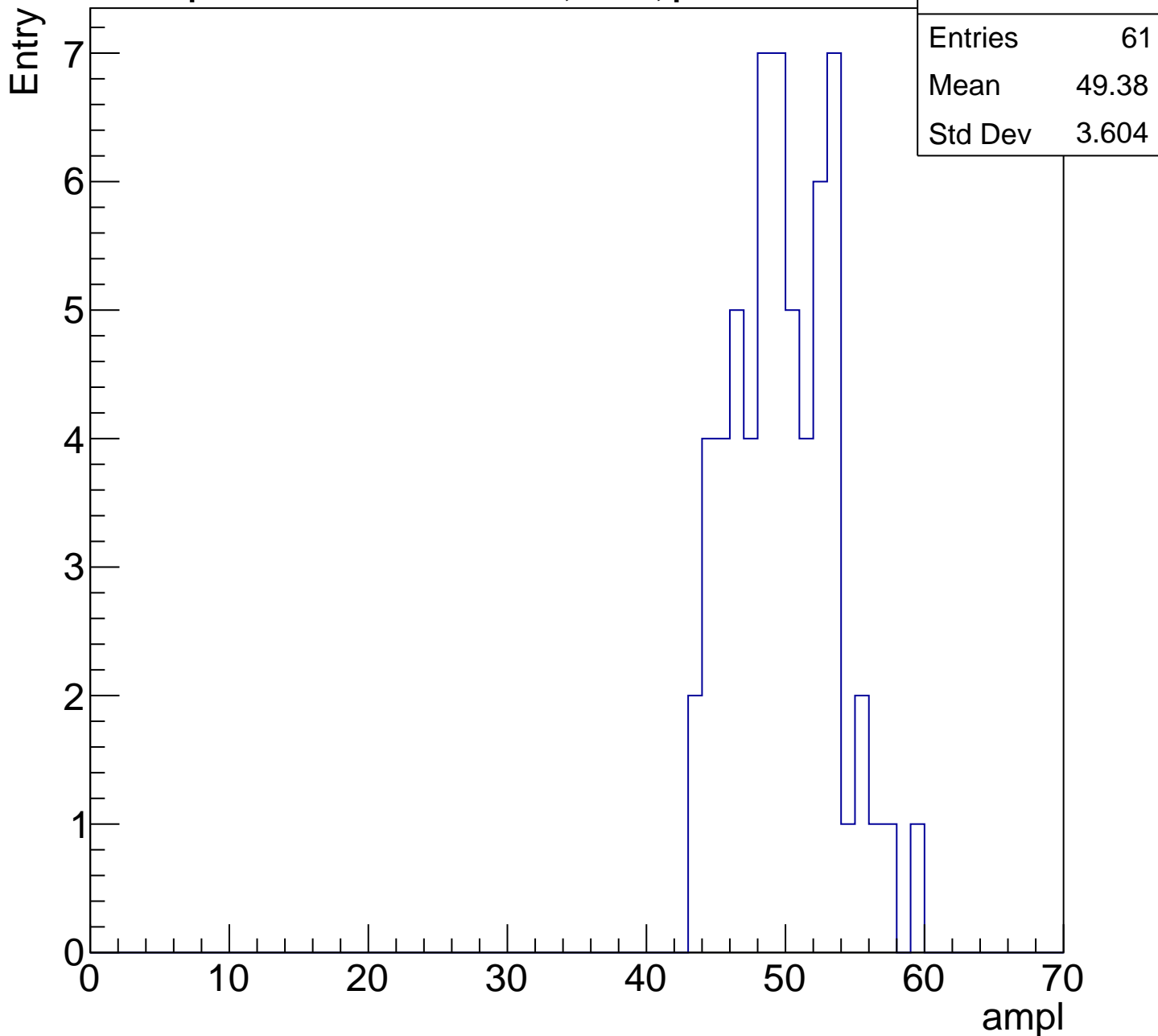
**Gaus mean : 42.6034**

**Gaus Width: 3.1318**



# B1L101S, U3-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

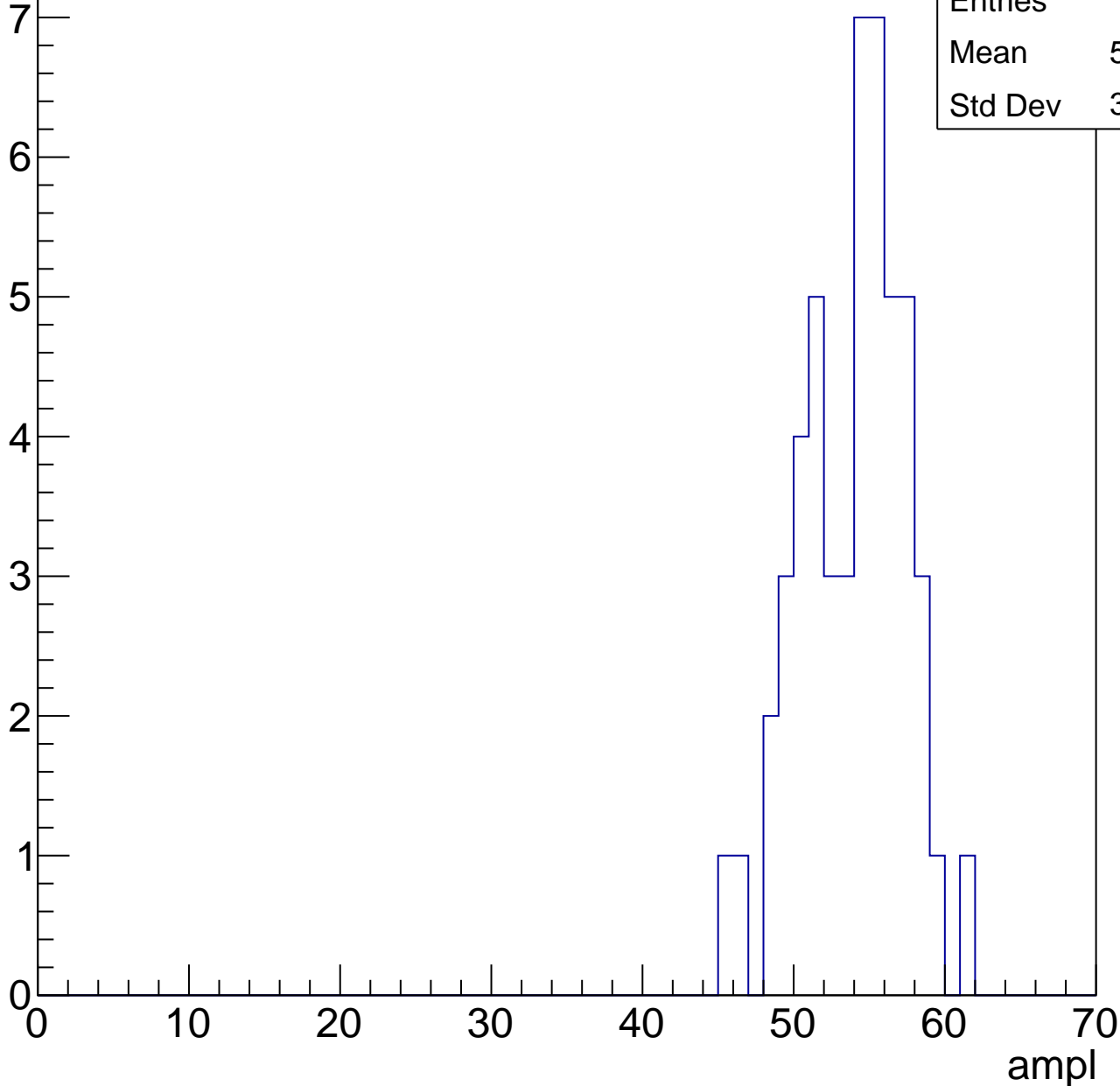


# B1L101S, U3-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

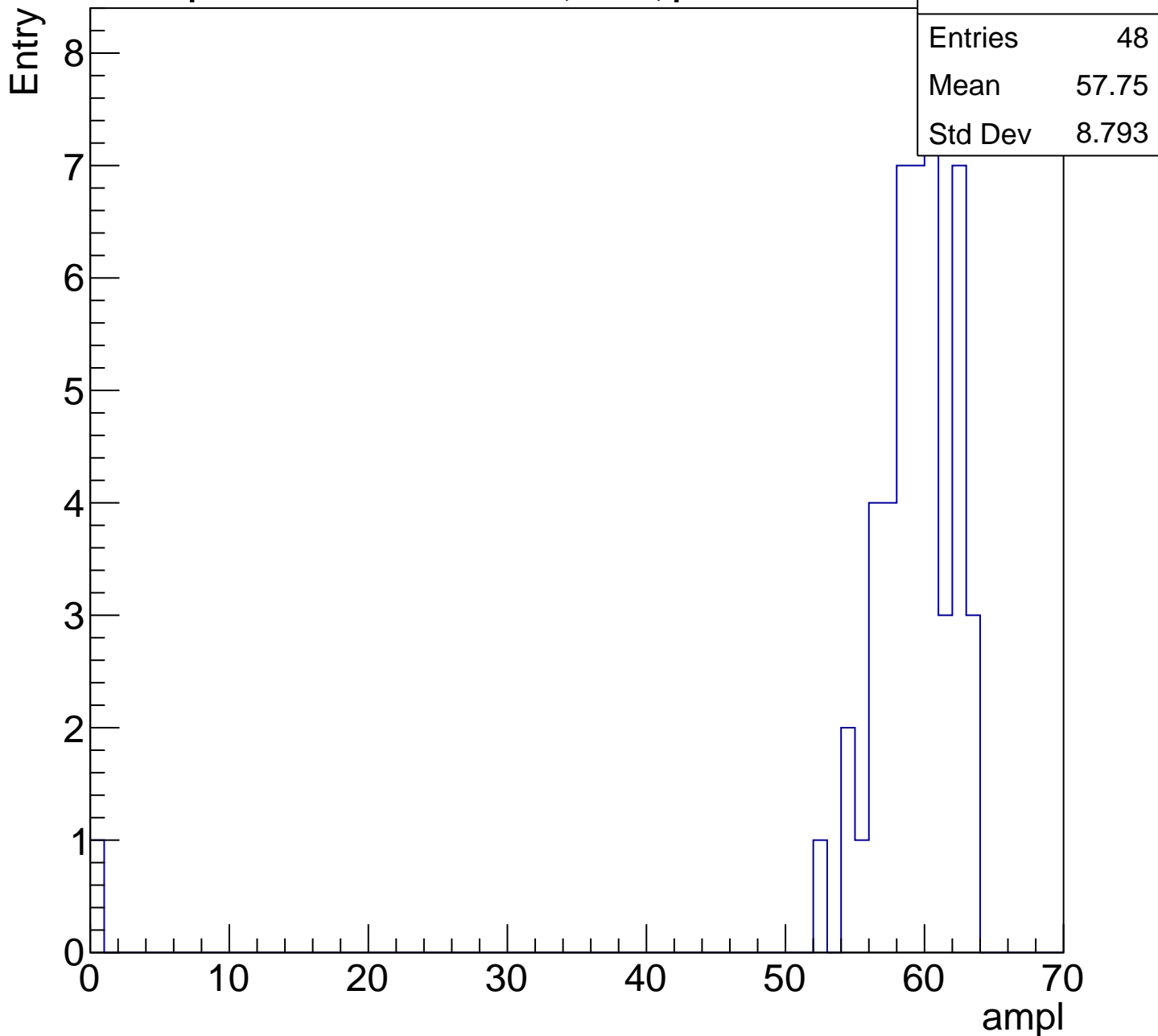
Entry

Entries	51
Mean	53.45
Std Dev	3.415



# B1L101S, U3-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

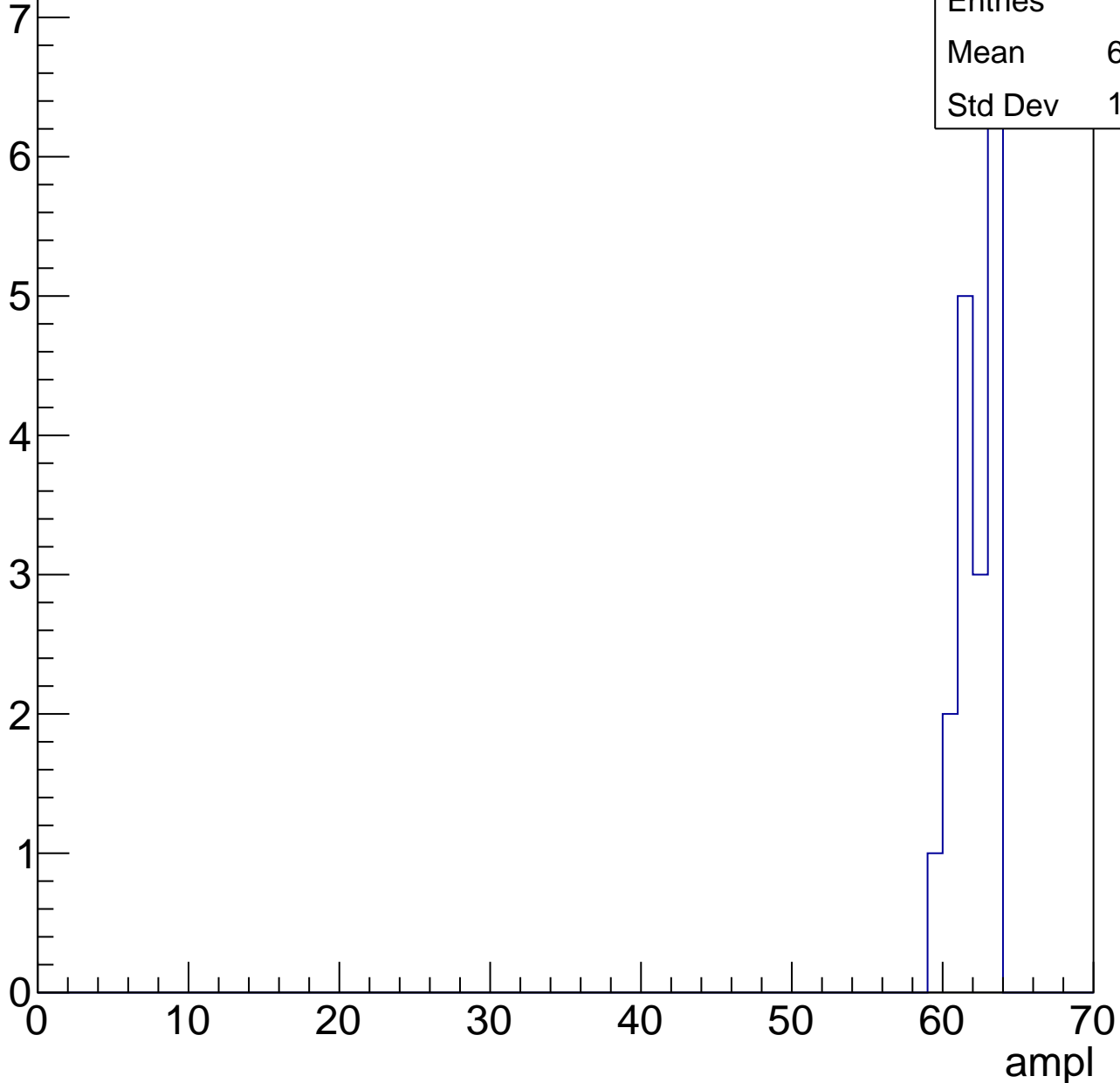


# B1L101S, U3-ch40, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	18
Mean	61.72
Std Dev	1.239





# B1L101S, U3-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch41, adc0

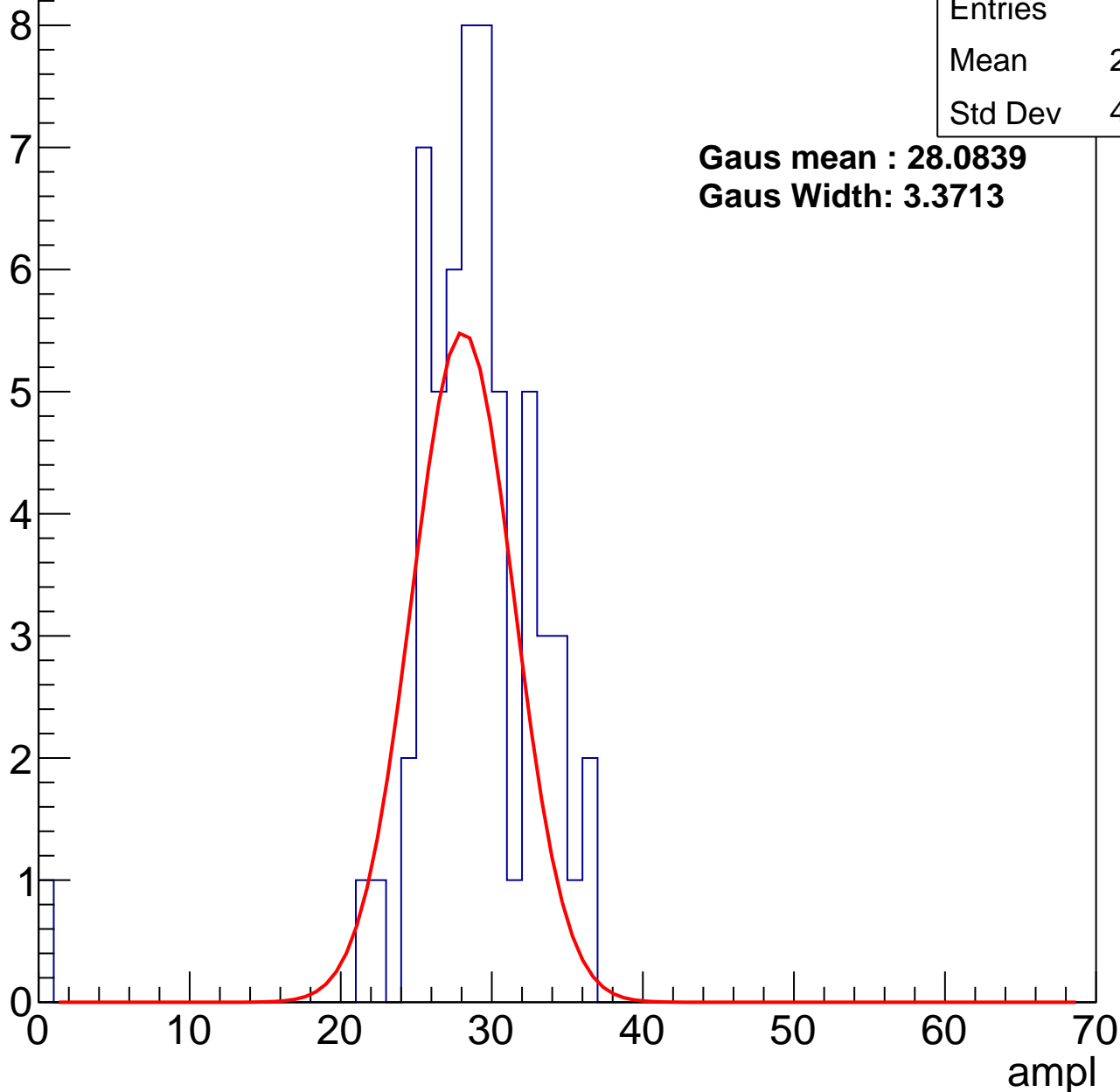
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	28.19
Std Dev	4.983

**Gaus mean : 28.0839**

**Gaus Width: 3.3713**



# B1L101S, U3-ch41, adc1

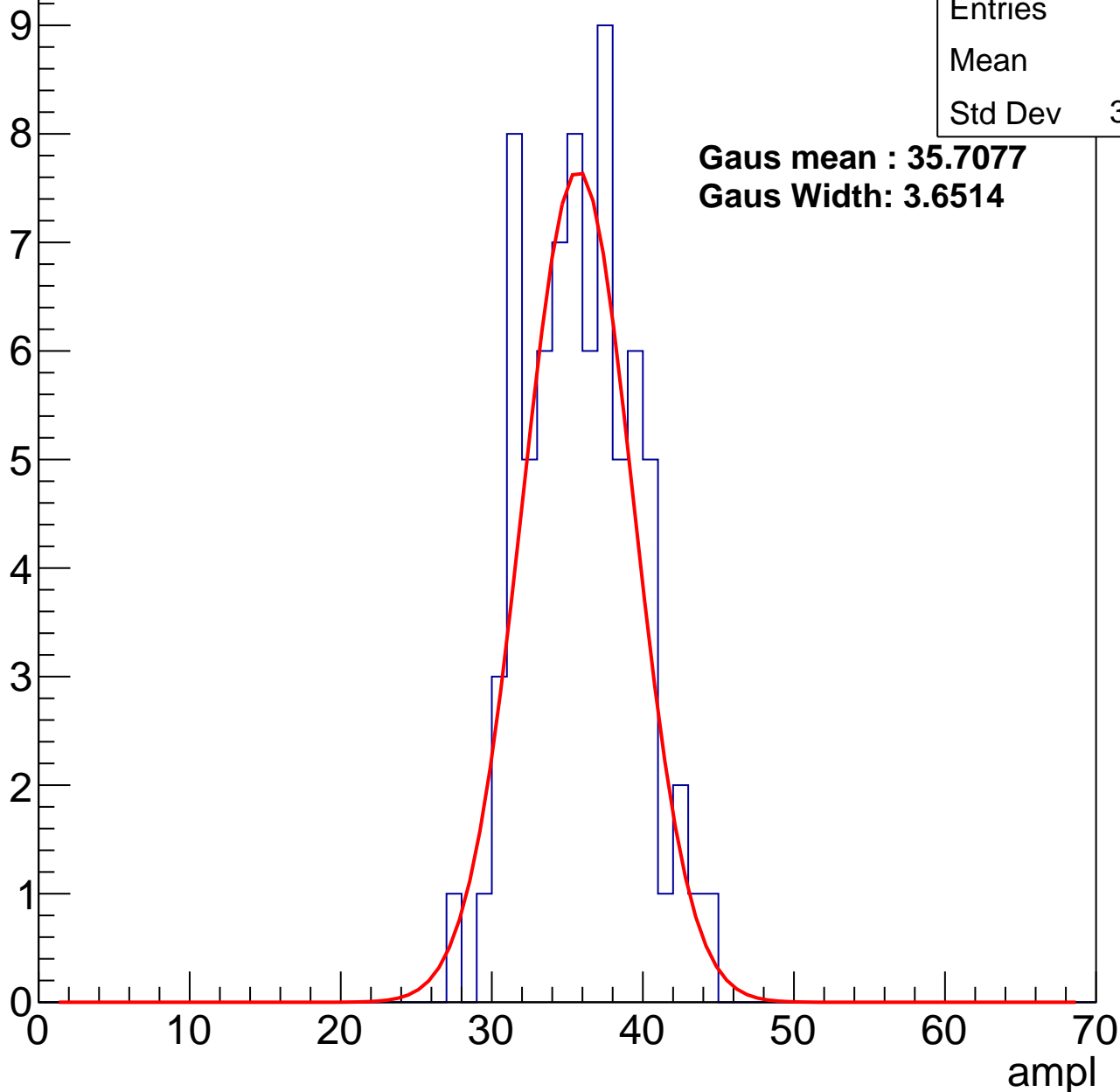
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	35.4
Std Dev	3.567

**Gaus mean : 35.7077**

**Gaus Width: 3.6514**



# B1L101S, U3-ch41, adc2

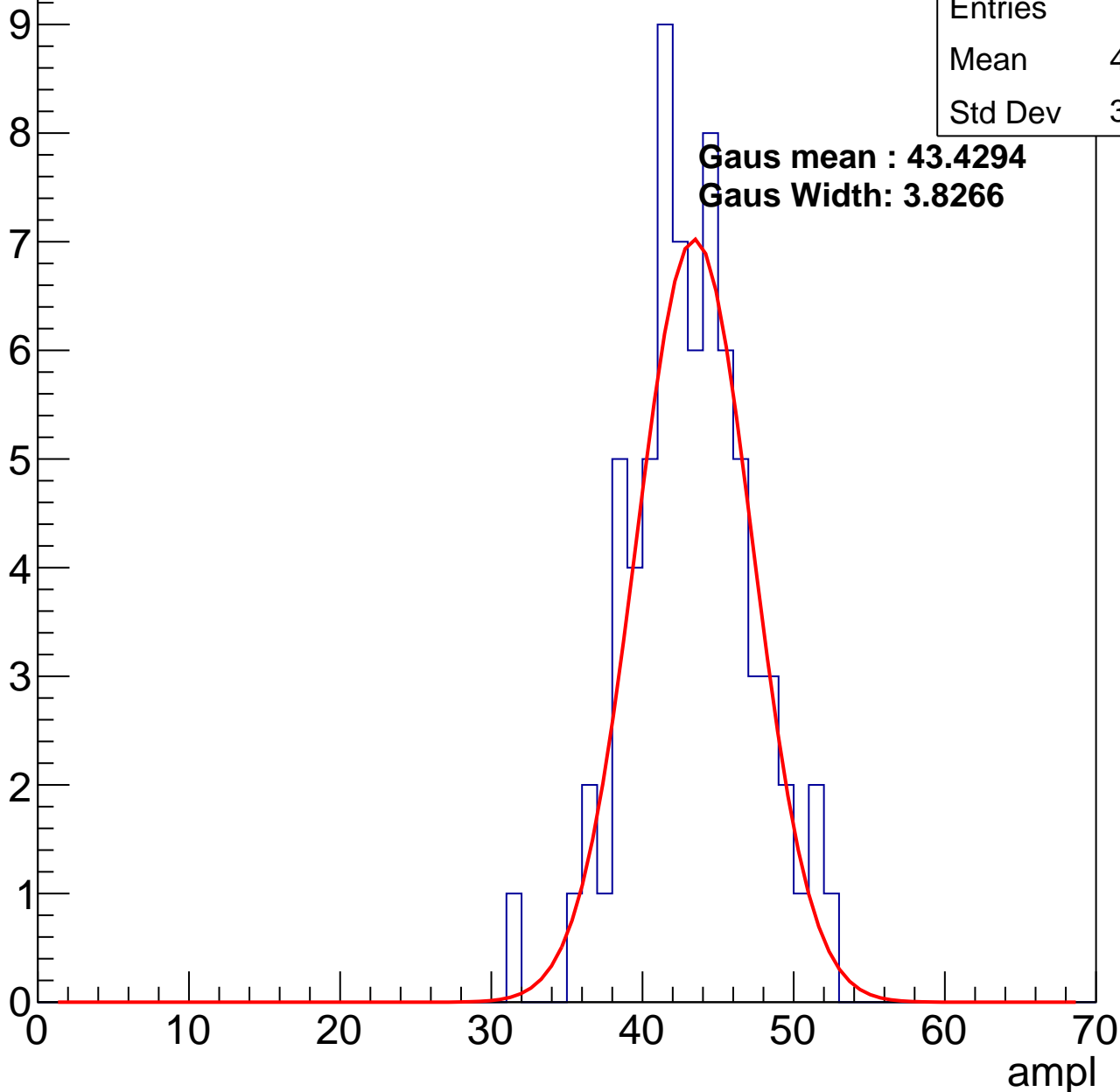
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	42.79
Std Dev	3.989

**Gaus mean : 43.4294**

**Gaus Width: 3.8266**

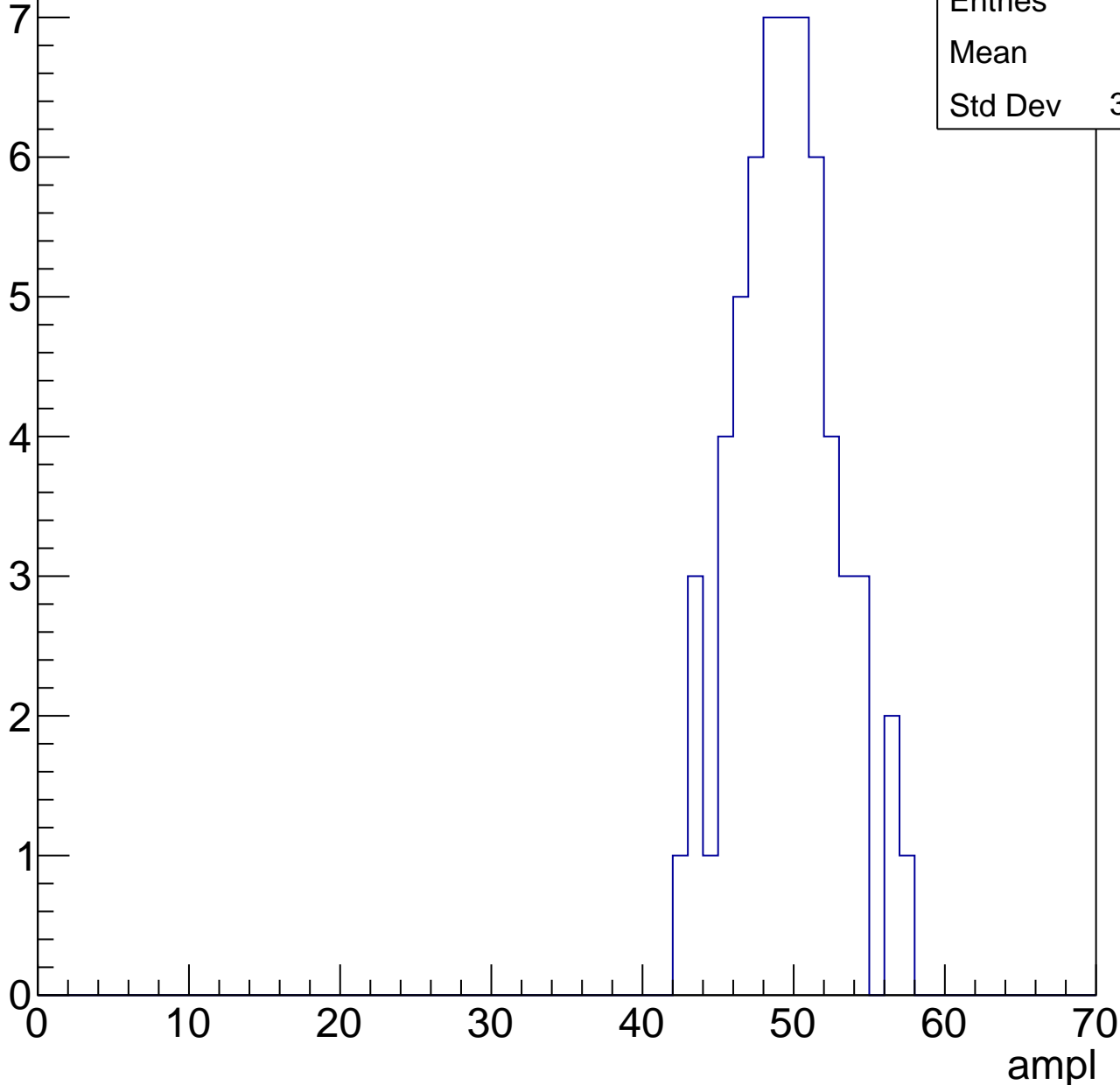


# B1L101S, U3-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	49
Std Dev	3.352

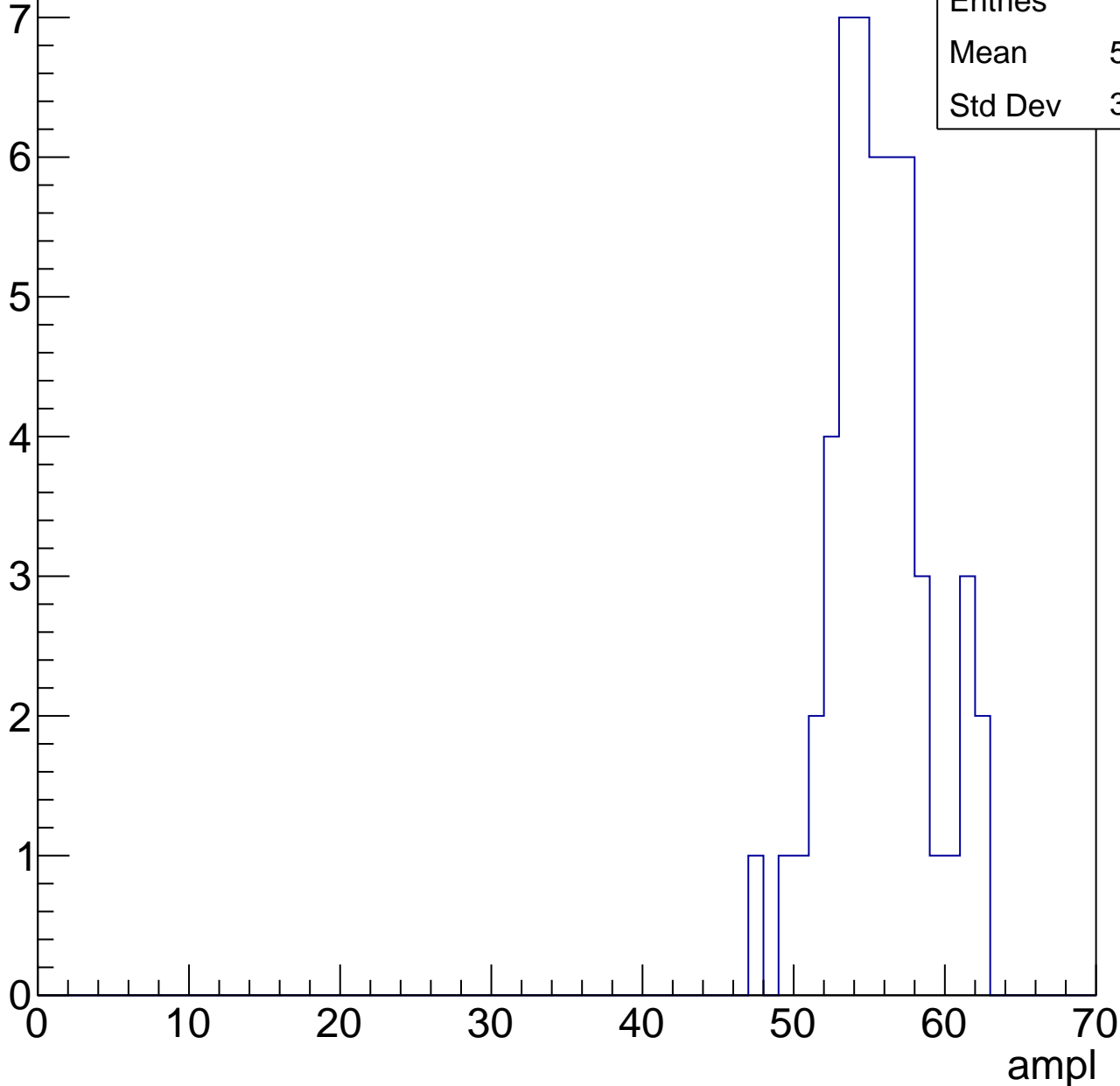


# B1L101S, U3-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	55.16
Std Dev	3.226

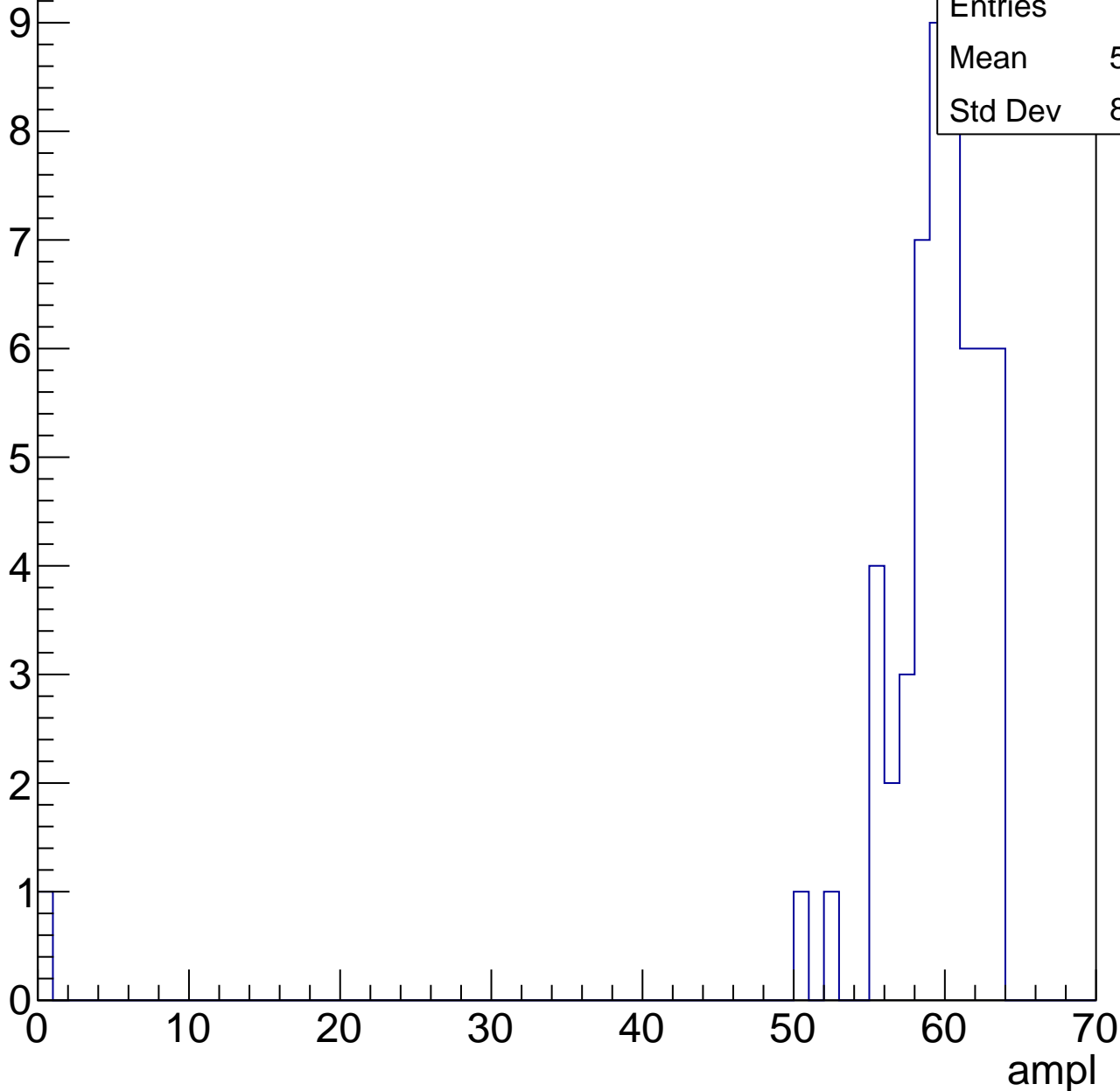


# B1L101S, U3-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

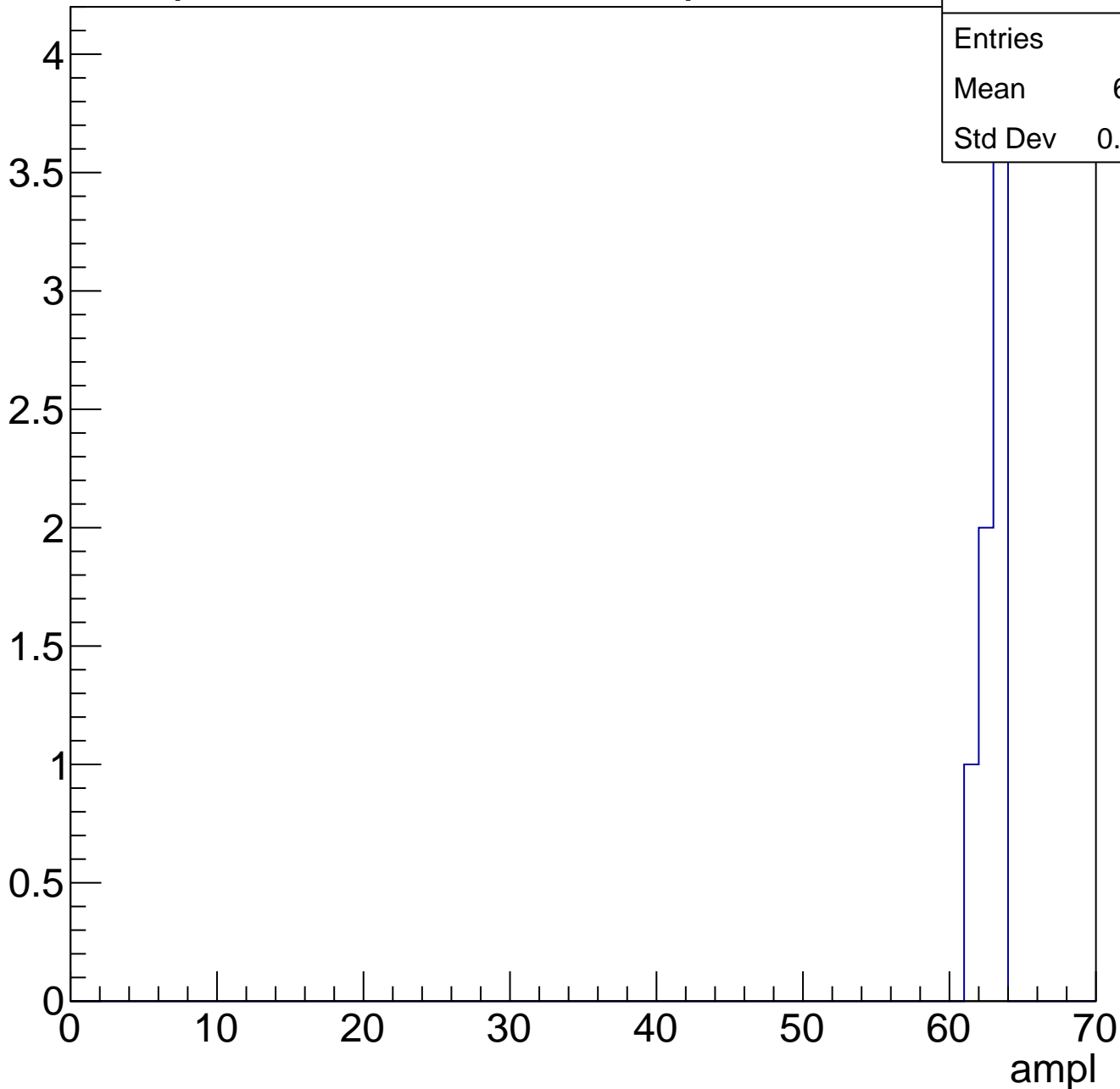
Entries	55
Mean	58.15
Std Dev	8.372



# B1L101S, U3-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U3-ch42, adc0

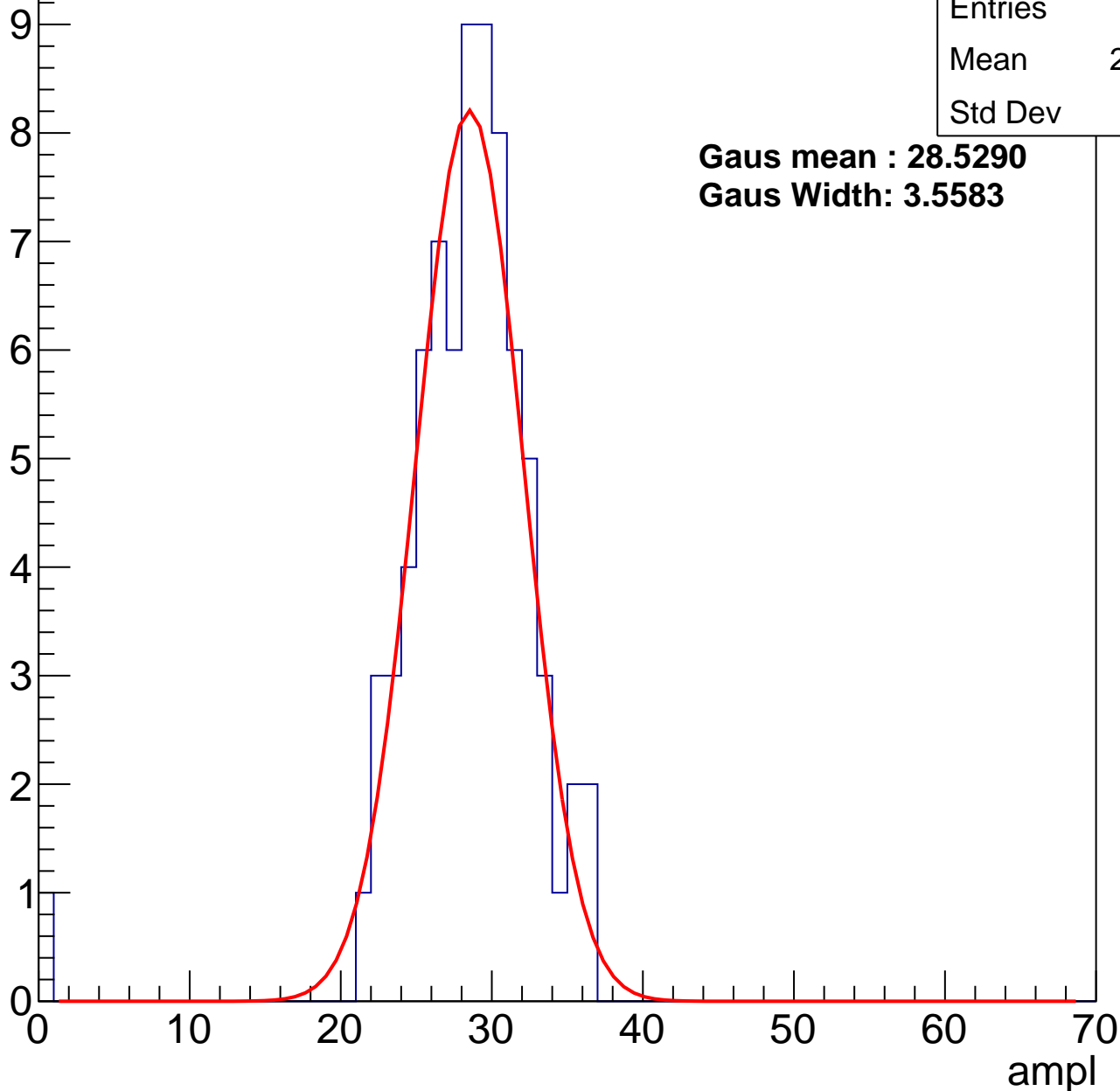
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	27.89
Std Dev	4.7

**Gaus mean : 28.5290**

**Gaus Width: 3.5583**



# B1L101S, U3-ch42, adc1

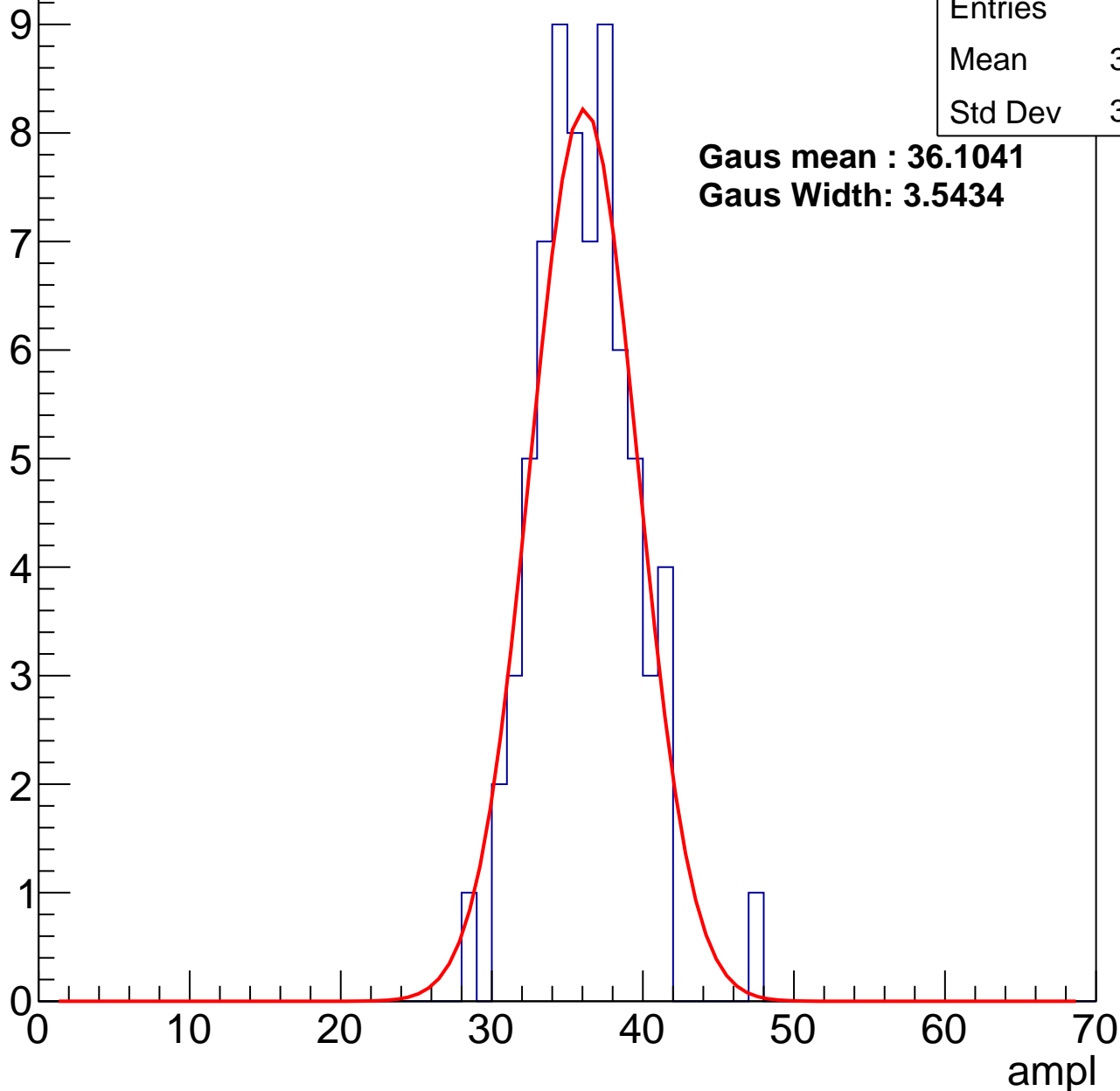
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	35.67
Std Dev	3.246

**Gaus mean : 36.1041**

**Gaus Width: 3.5434**



# B1L101S, U3-ch42, adc2

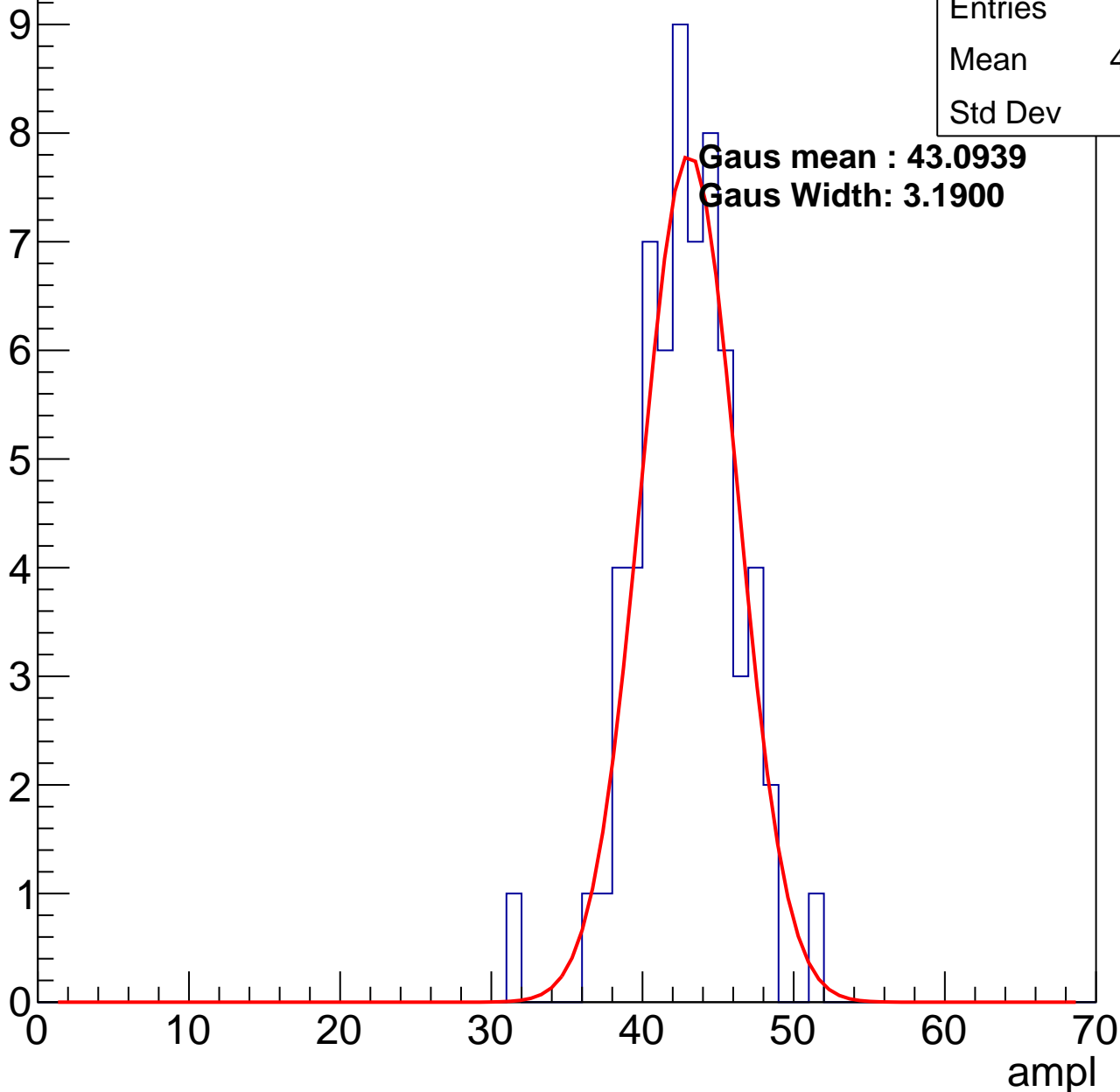
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	42.38
Std Dev	3.31

**Gaus mean : 43.0939**

**Gaus Width: 3.1900**

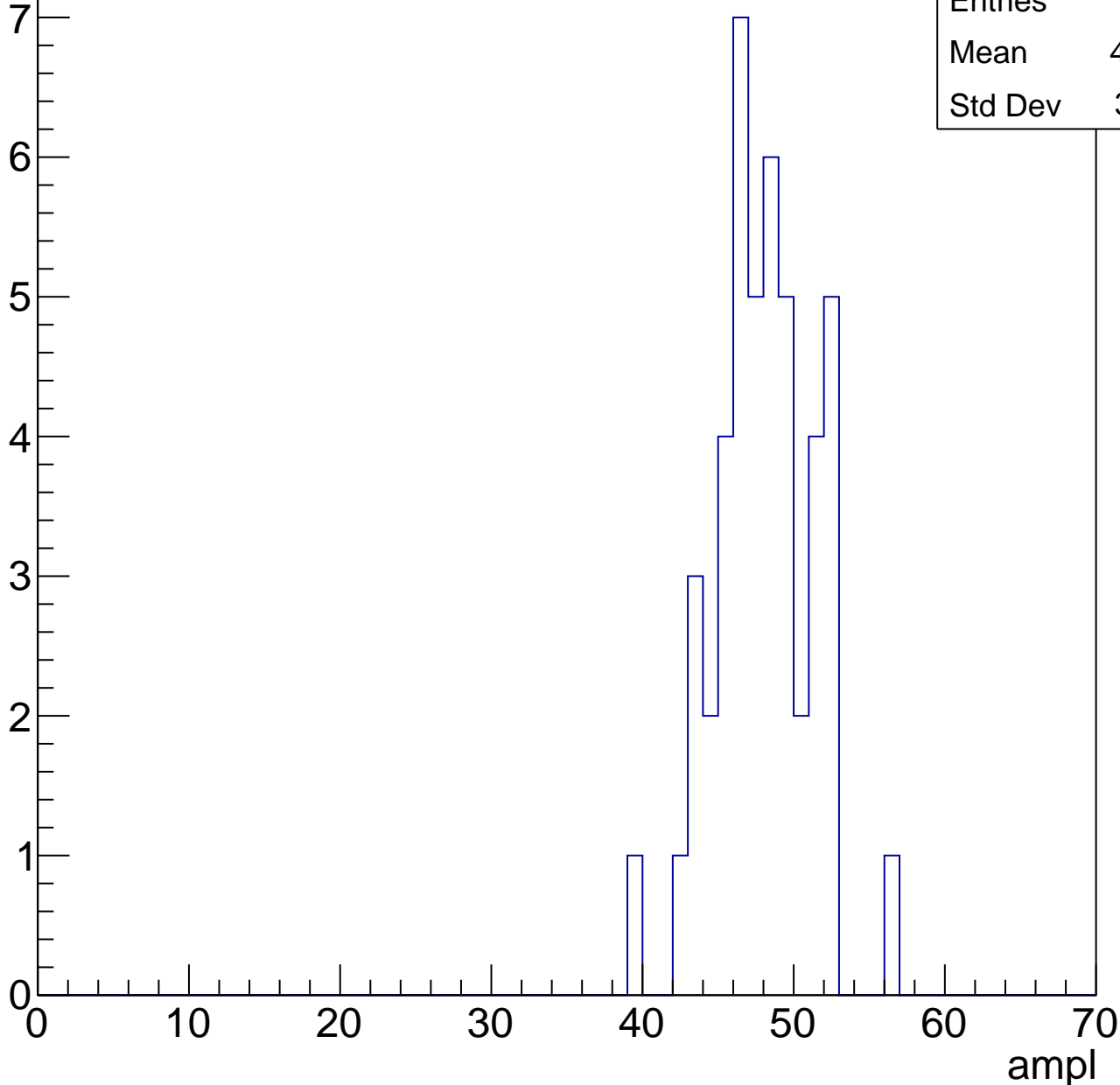


# B1L101S, U3-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	47.57
Std Dev	3.221



# B1L101S, U3-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	76
Mean	53.96
Std Dev	3.258

Entry

10

8

6

4

2

0

0

10

20

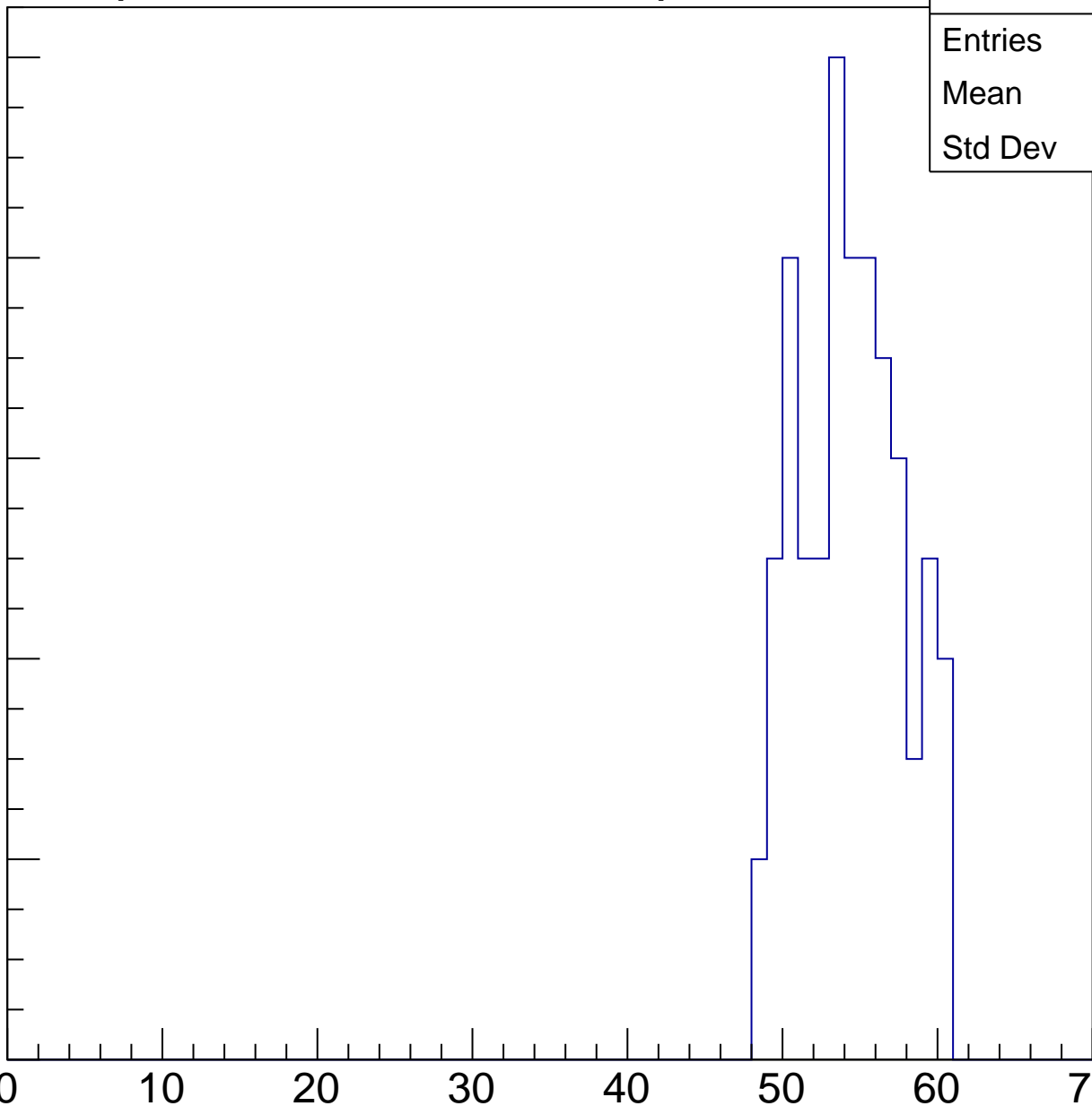
30

40

50

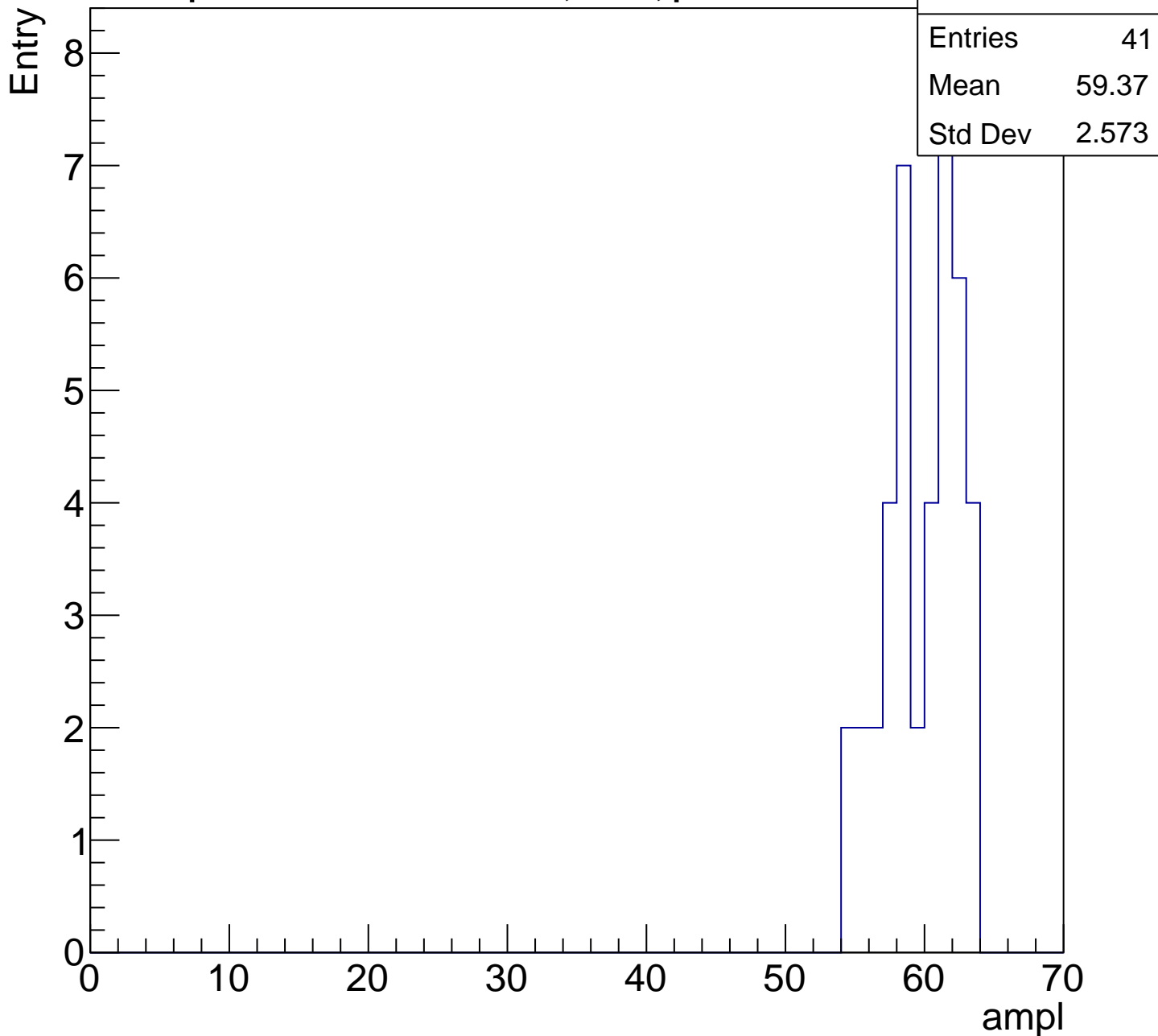
60

ampl



# B1L101S, U3-ch42, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

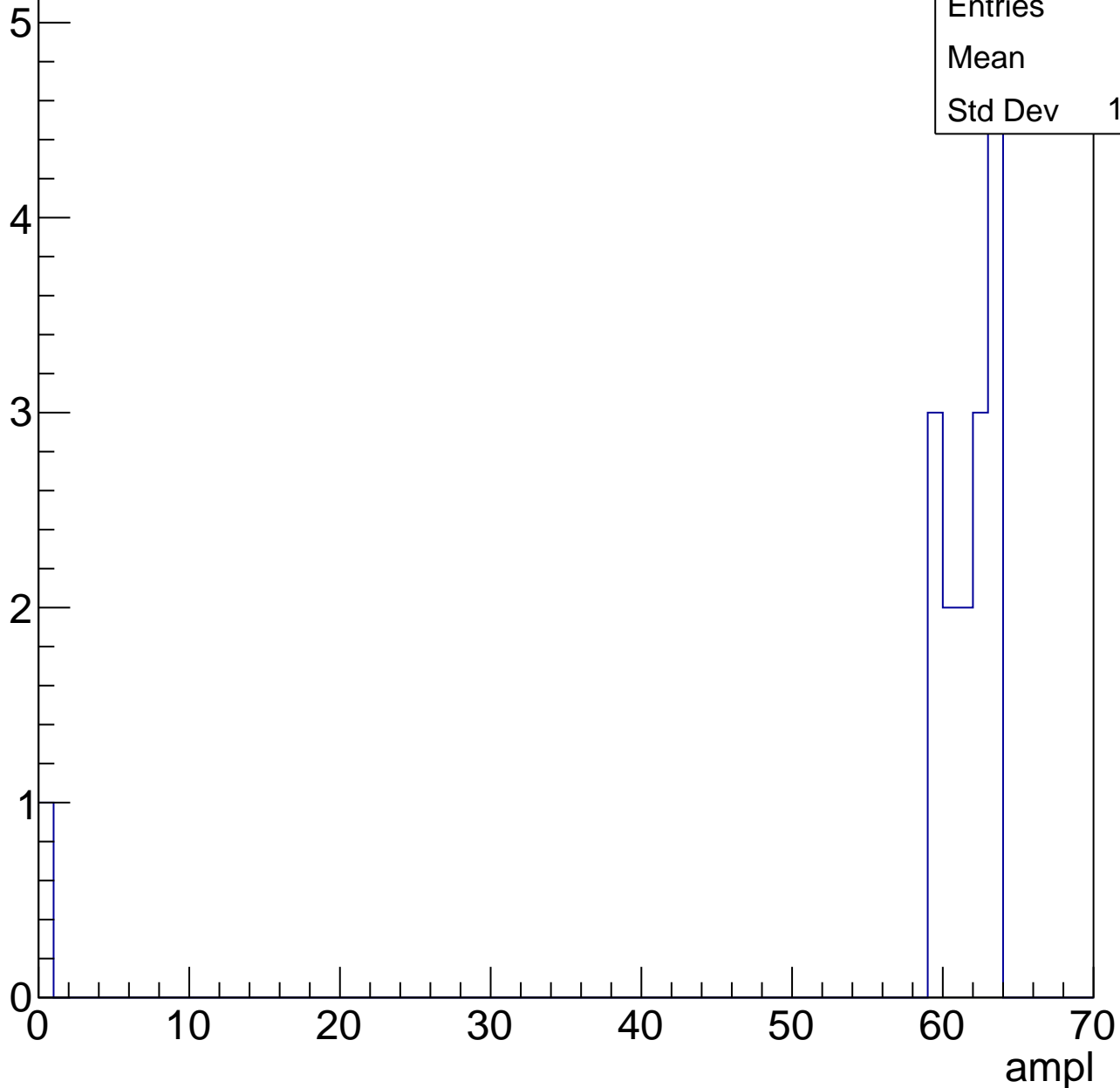


# B1L101S, U3-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	16
Mean	57.5
Std Dev	14.92





# B1L101S, U3-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch43, adc0

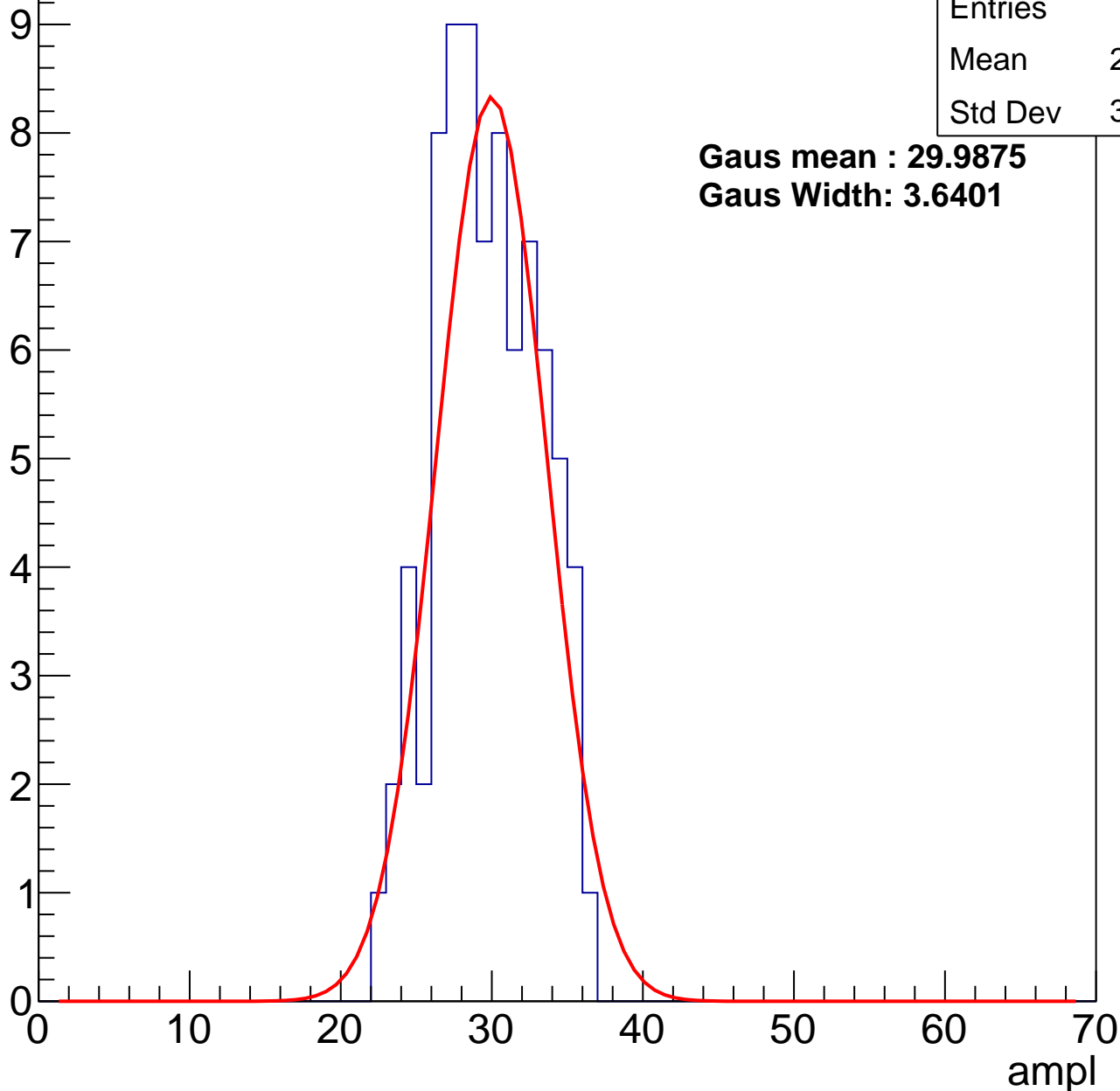
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	29.29
Std Dev	3.323

**Gaus mean : 29.9875**

**Gaus Width: 3.6401**



# B1L101S, U3-ch43, adc1

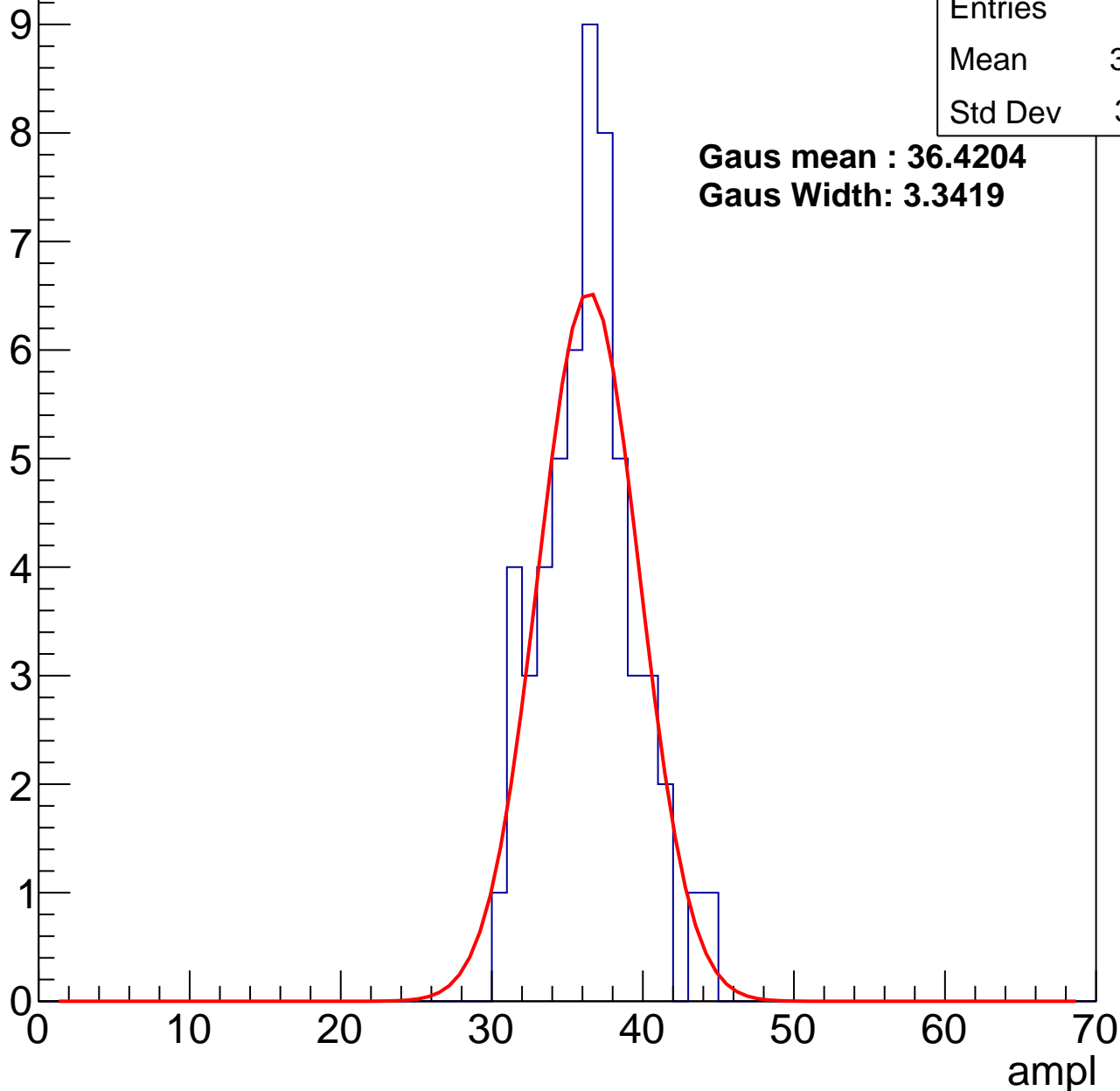
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	35.96
Std Dev	3.051

**Gaus mean : 36.4204**

**Gaus Width: 3.3419**



# B1L101S, U3-ch43, adc2

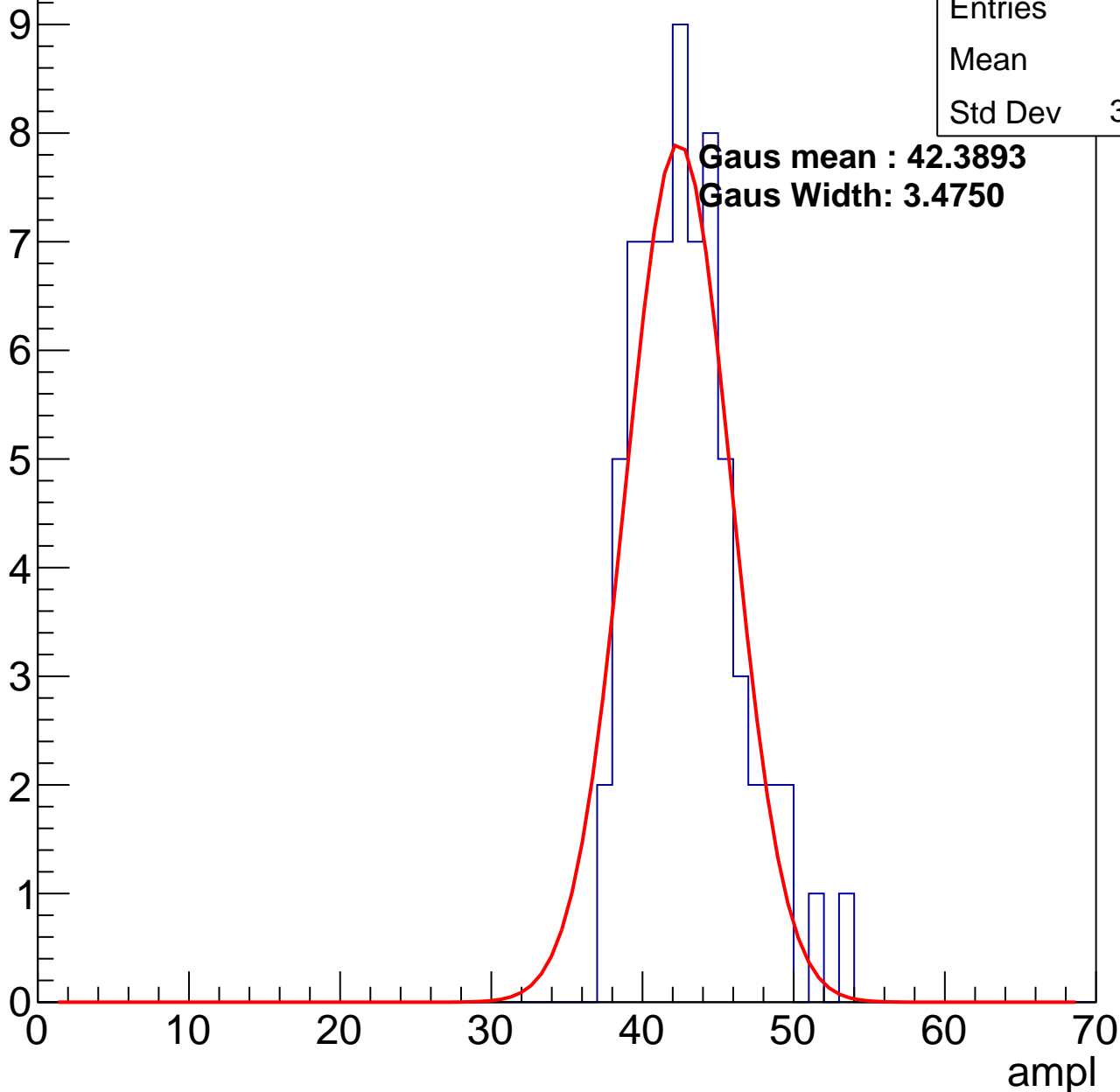
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	42.5
Std Dev	3.354

**Gaus mean : 42.3893**

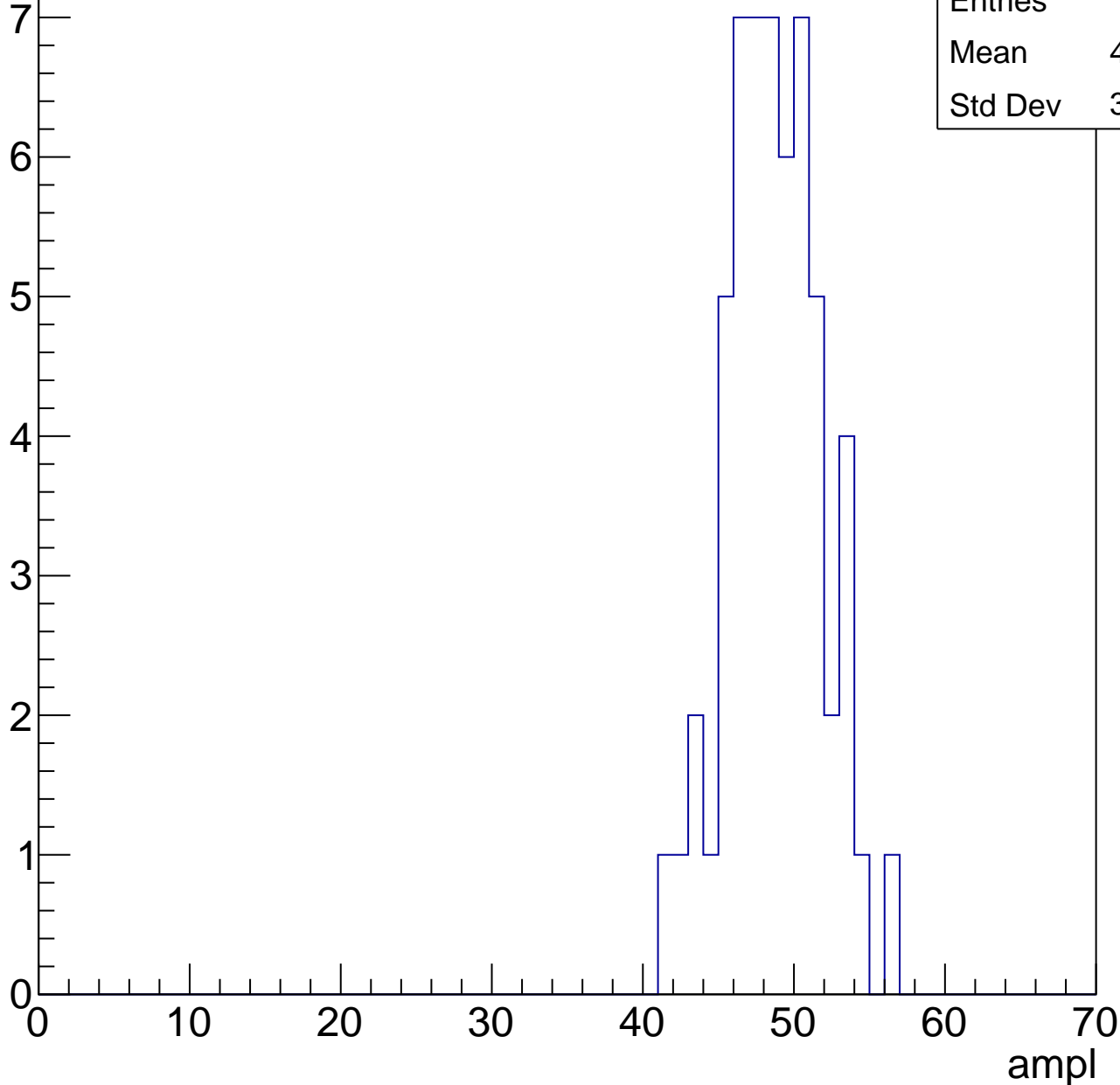
**Gaus Width: 3.4750**



# B1L101S, U3-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

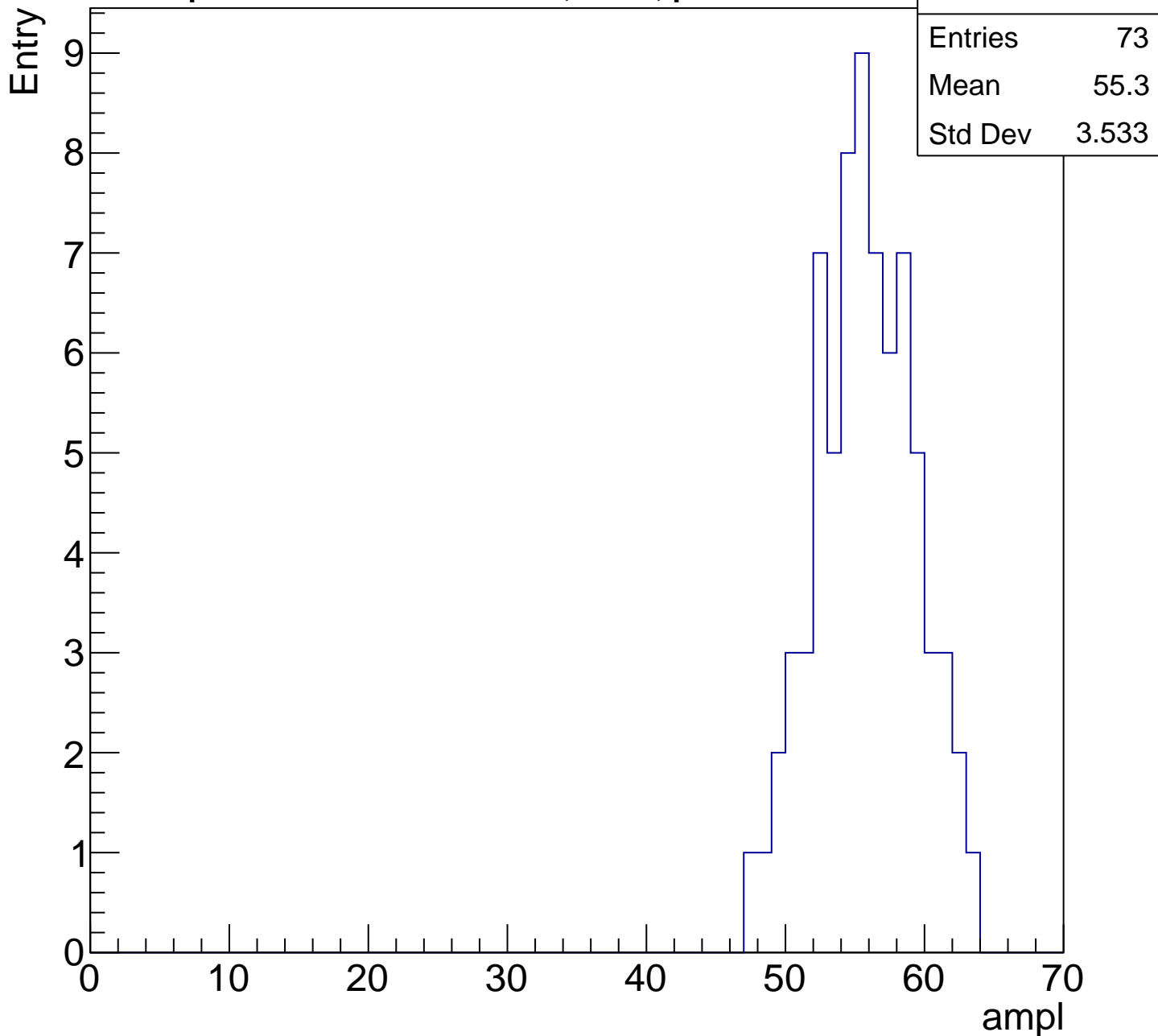
Entry



Entries	57
Mean	48.25
Std Dev	3.074

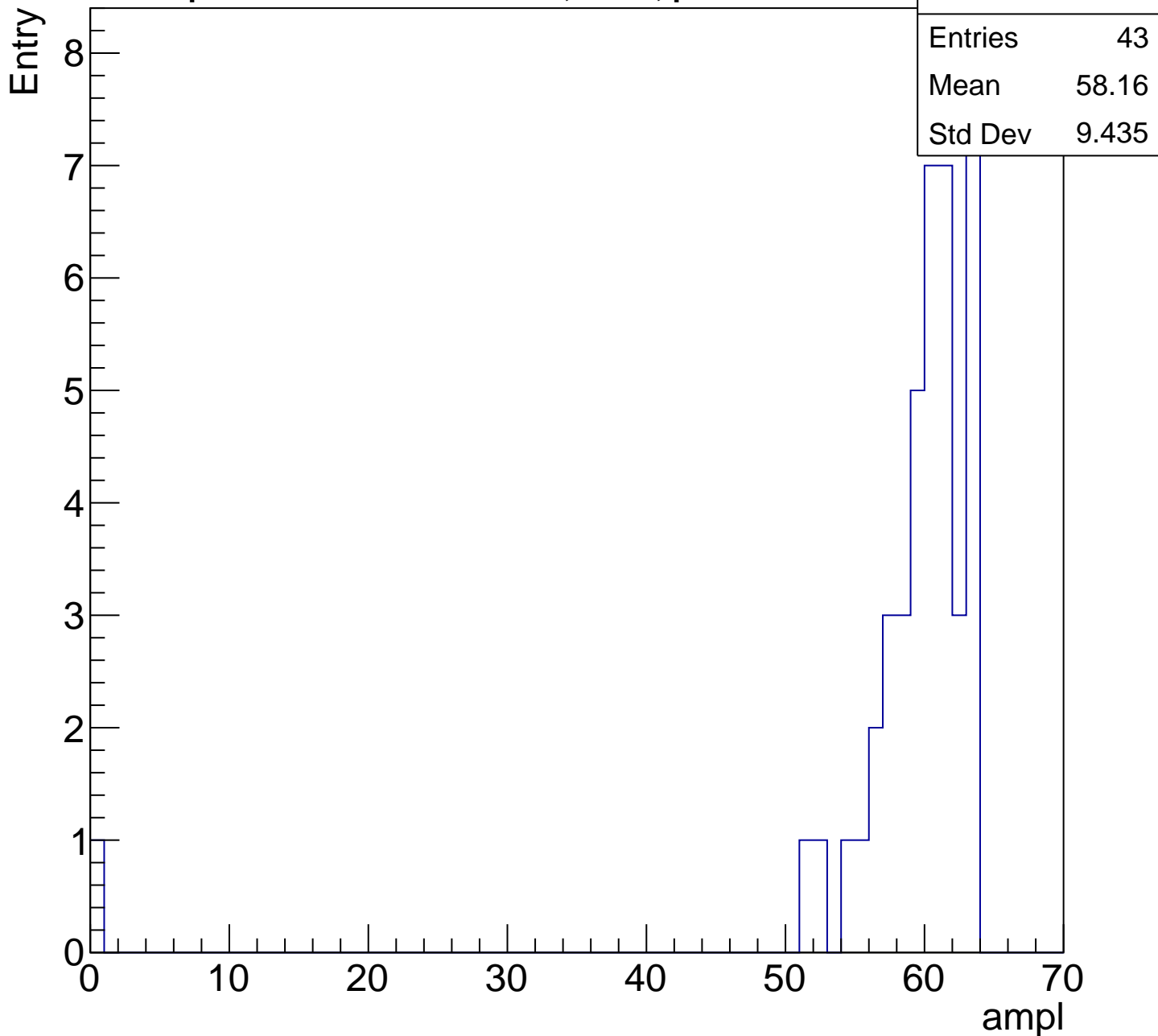
# B1L101S, U3-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

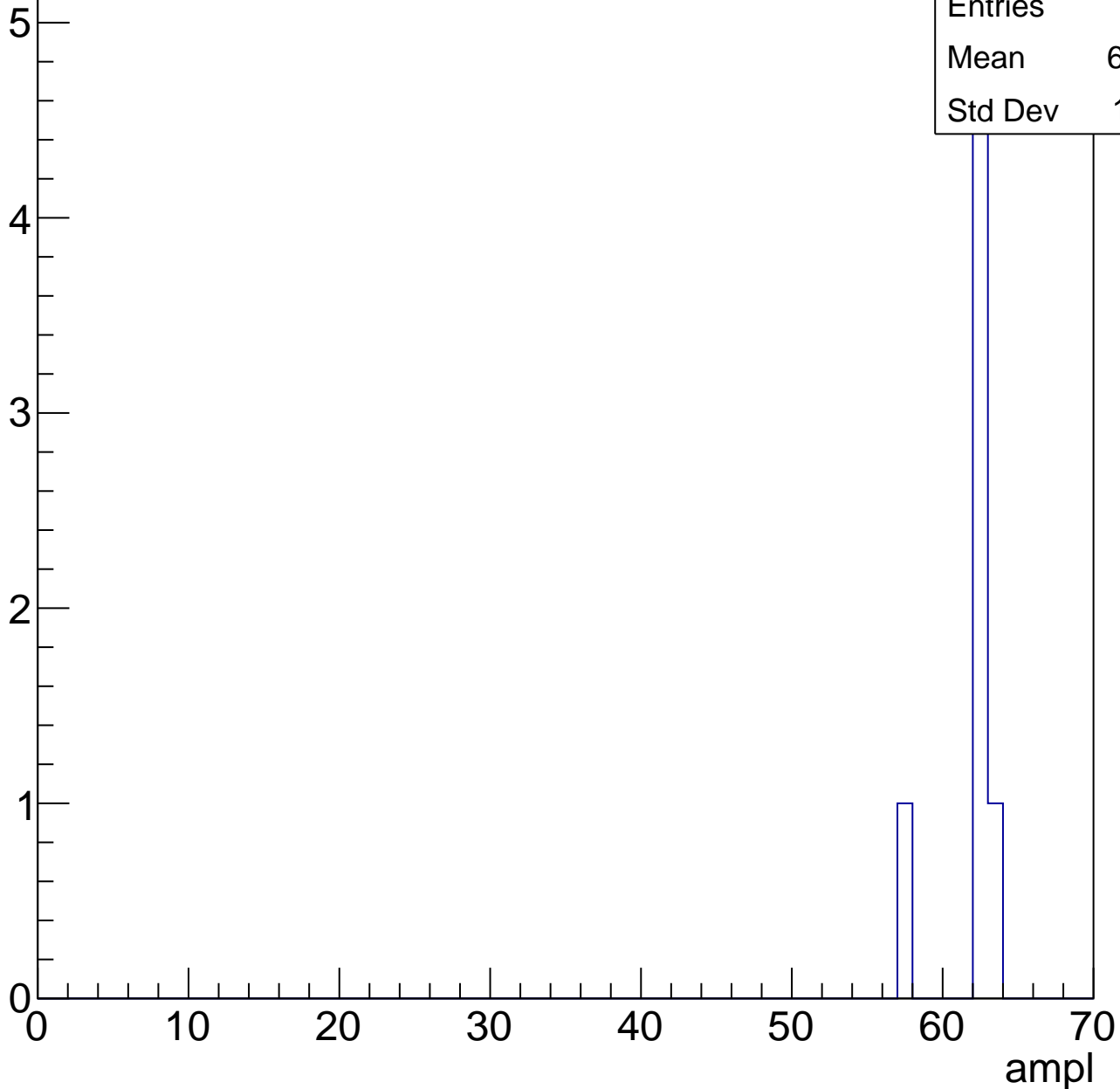


# B1L101S, U3-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	7
Mean	61.43
Std Dev	1.841





# B1L101S, U3-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U3-ch44, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	87
Mean	27.98
Std Dev	7.227

**Gaus mean : 29.7231**

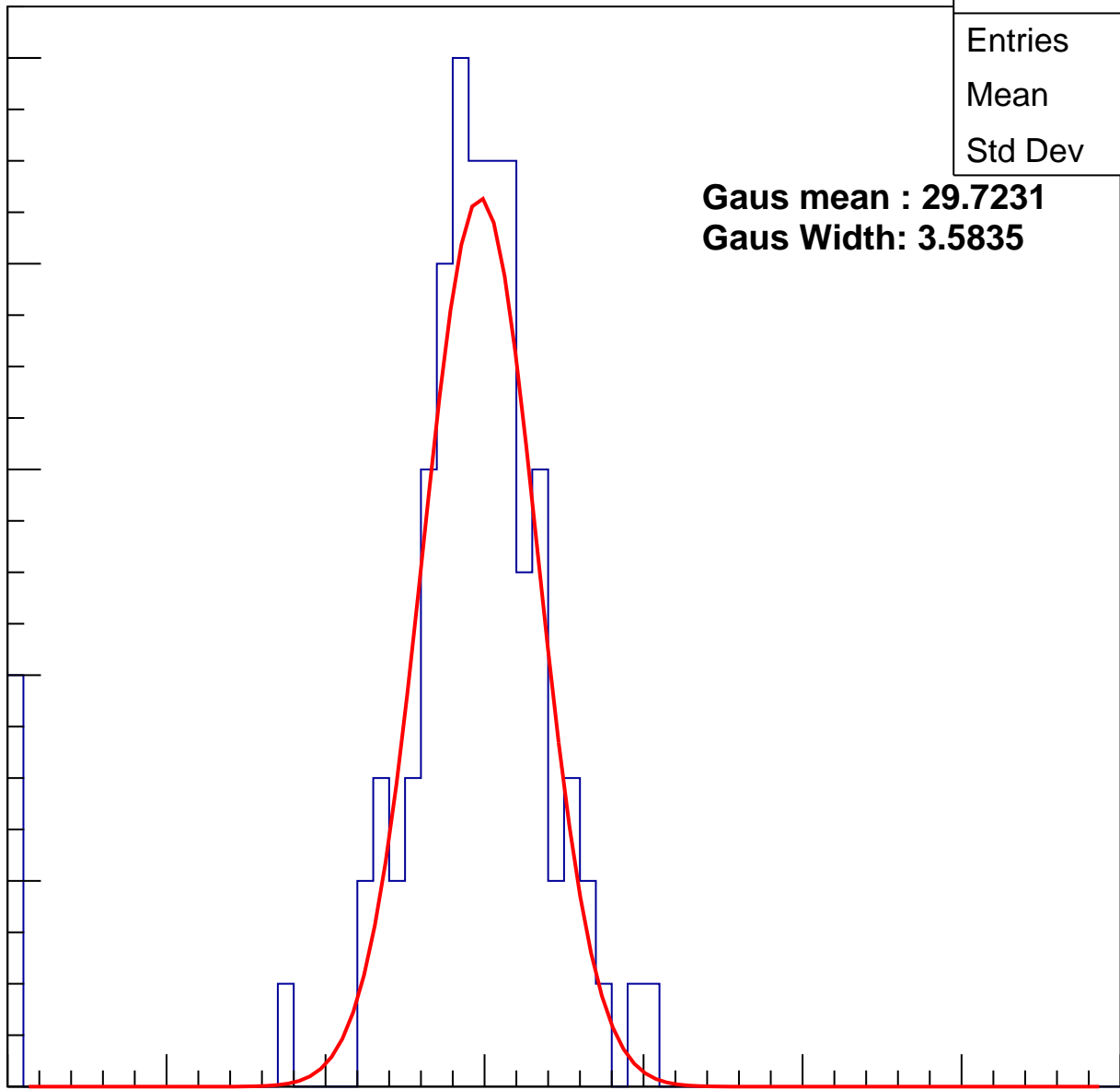
**Gaus Width: 3.5835**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U3-ch44, adc1

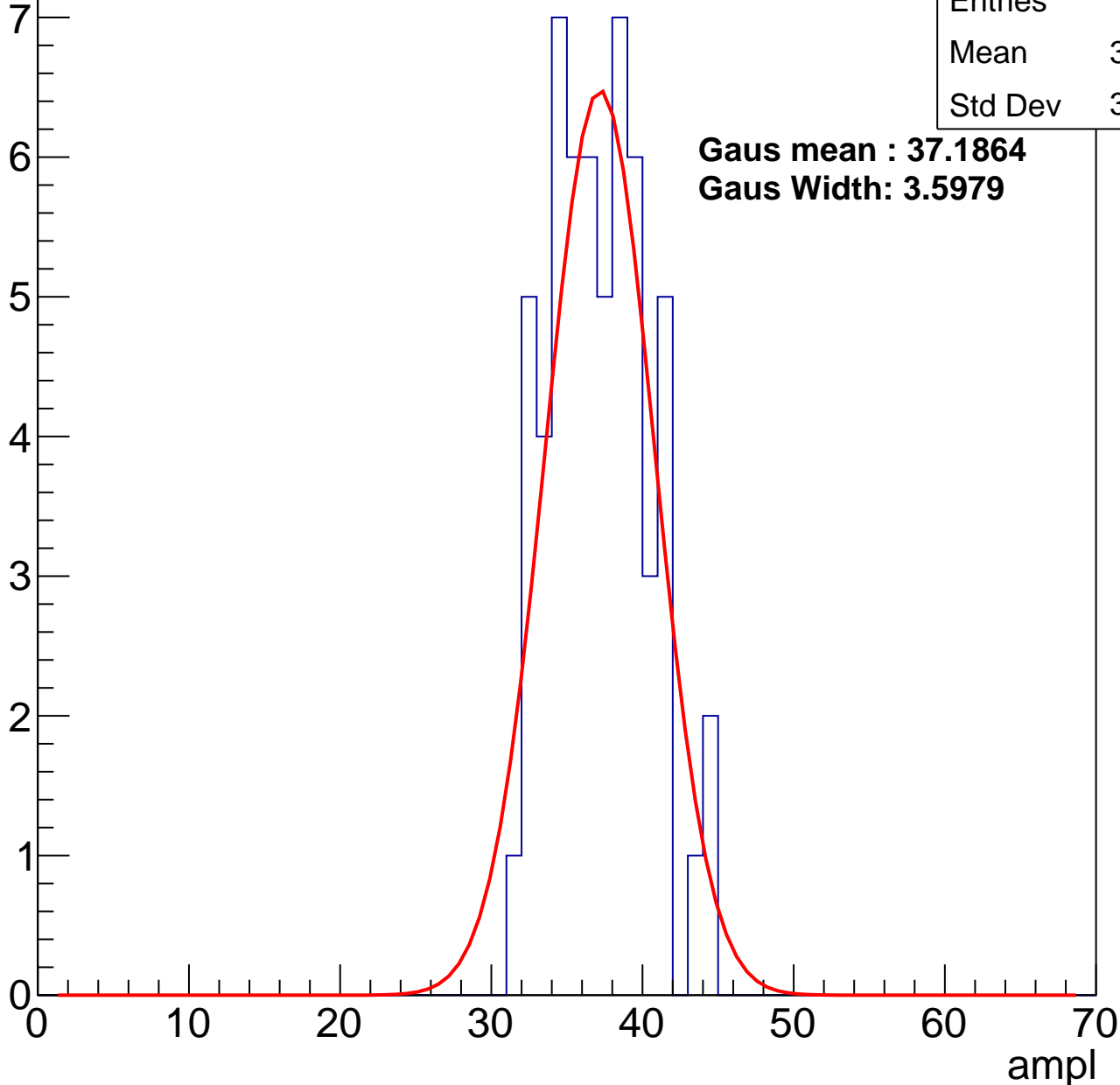
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	36.69
Std Dev	3.174

**Gaus mean : 37.1864**

**Gaus Width: 3.5979**



# B1L101S, U3-ch44, adc2

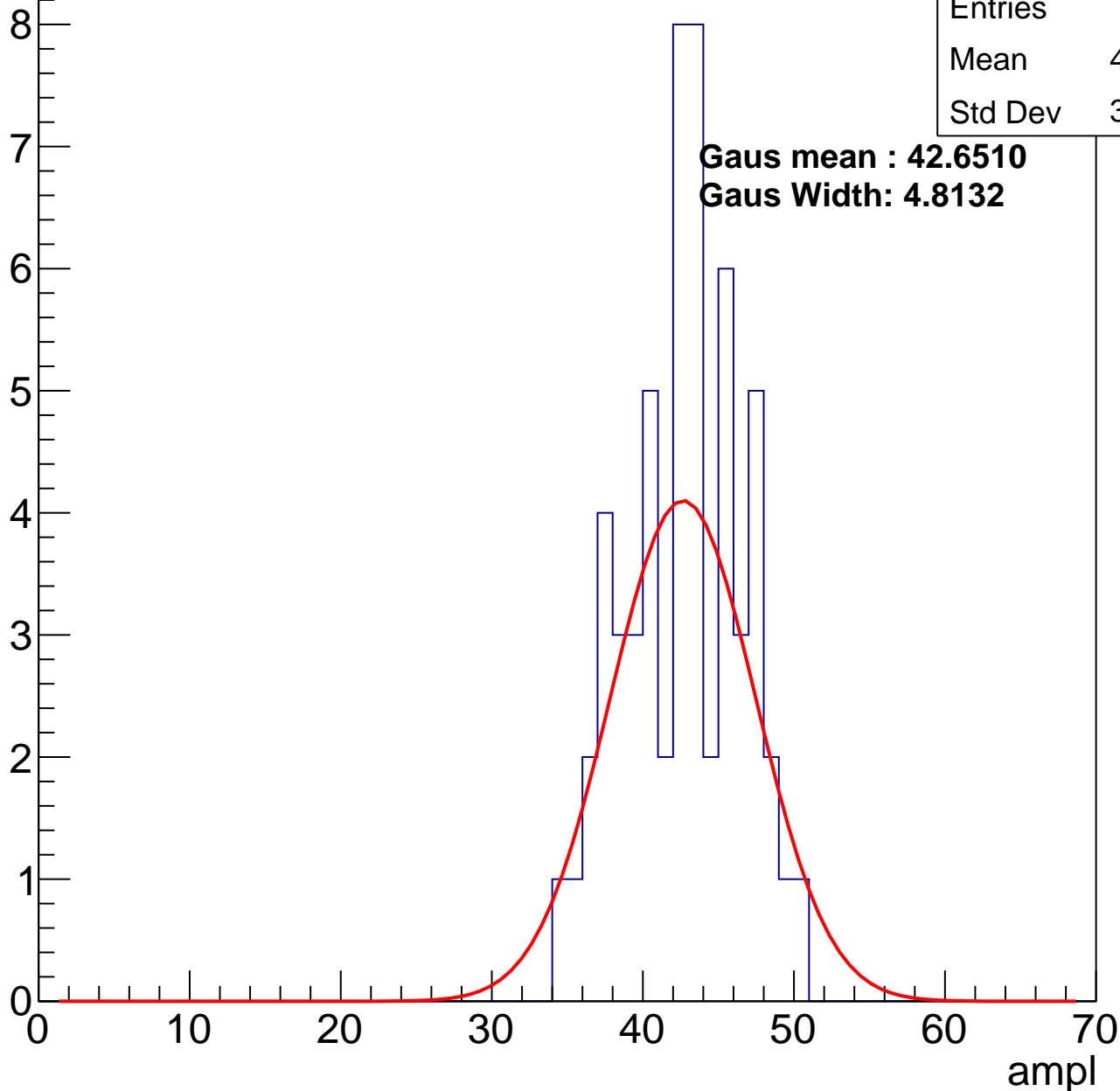
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	42.25
Std Dev	3.762

**Gaus mean : 42.6510**

**Gaus Width: 4.8132**

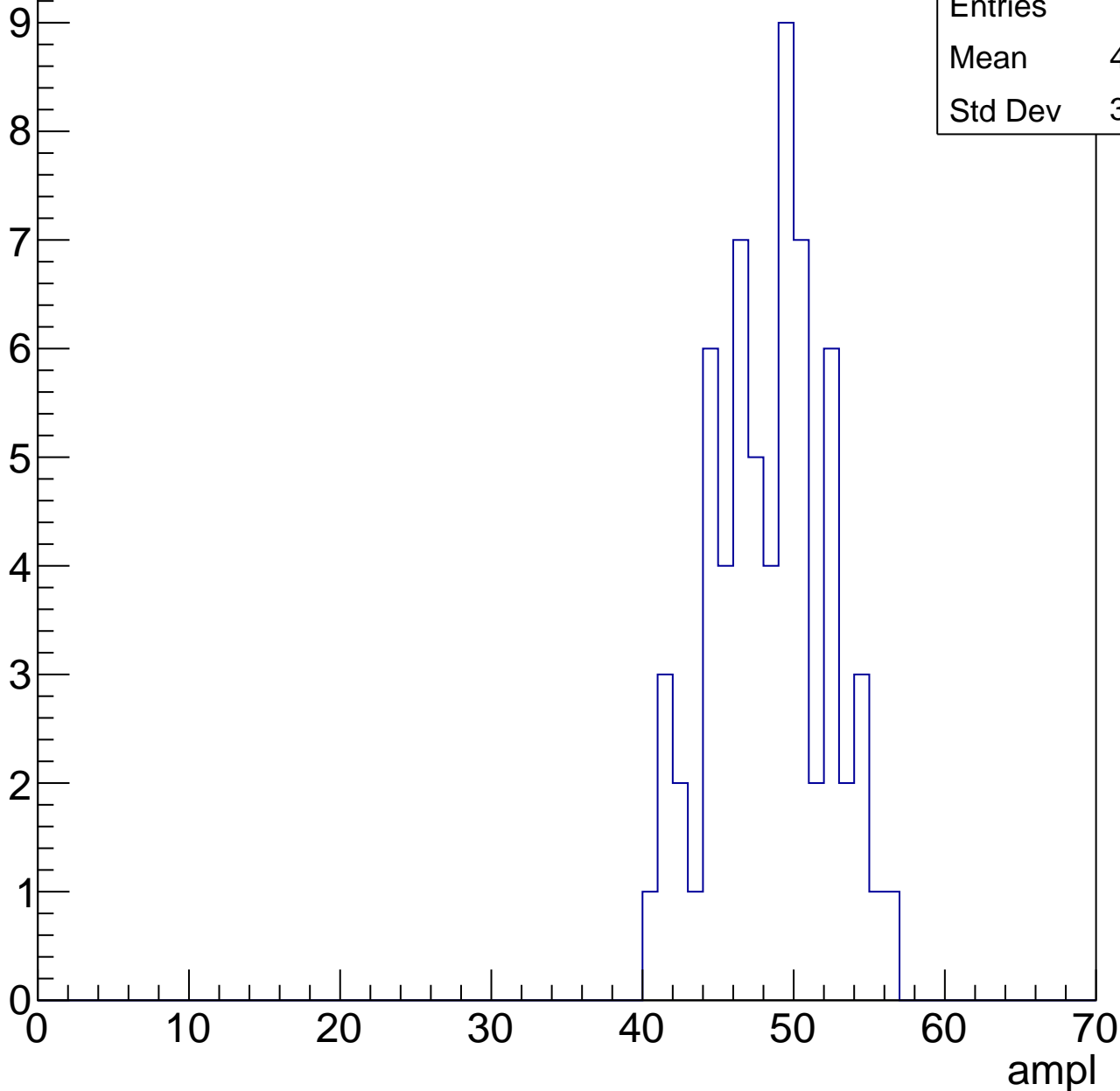


# B1L101S, U3-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	47.92
Std Dev	3.739

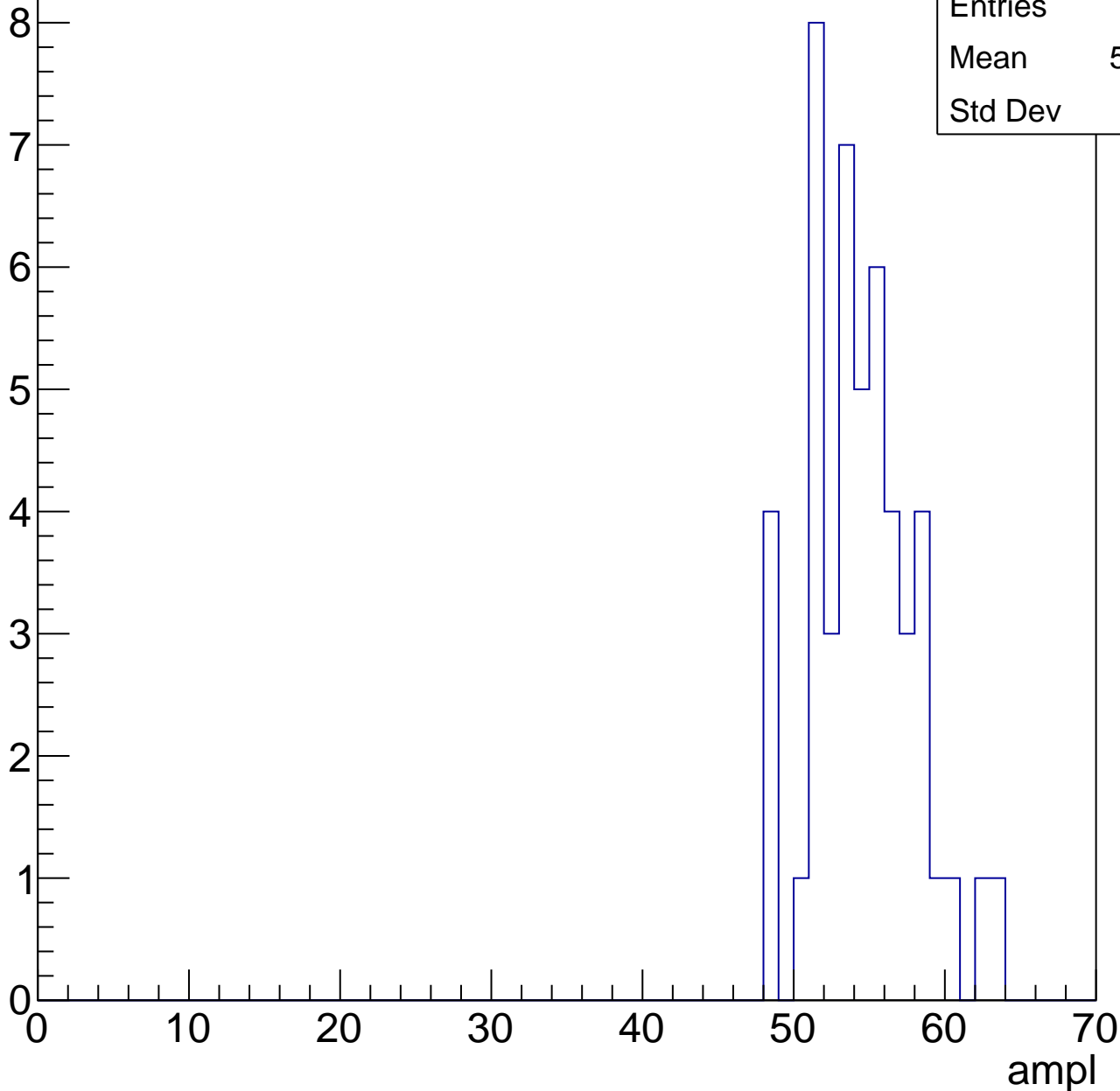


# B1L101S, U3-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	54.04
Std Dev	3.41

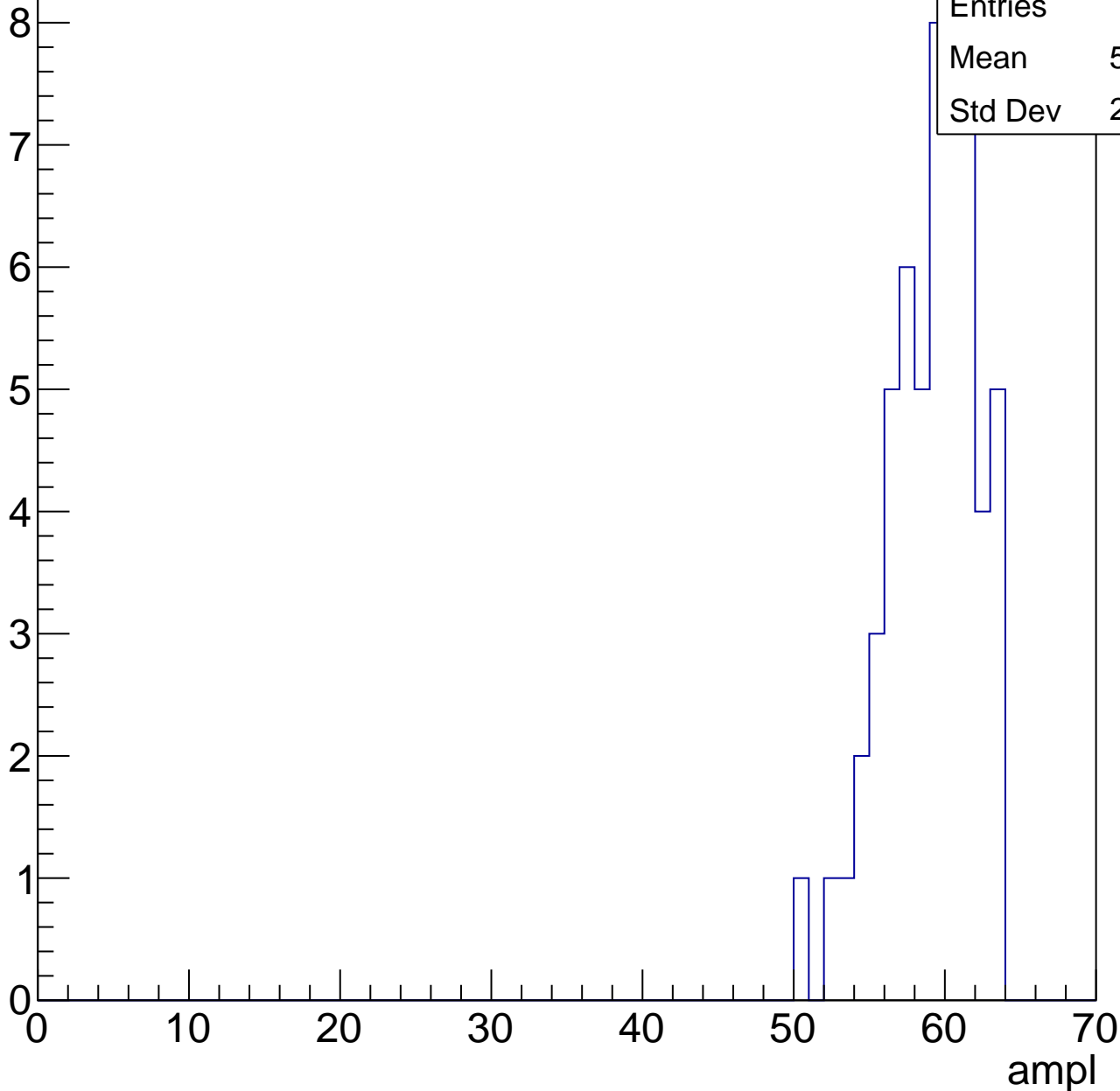


# B1L101S, U3-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	58.65
Std Dev	2.923

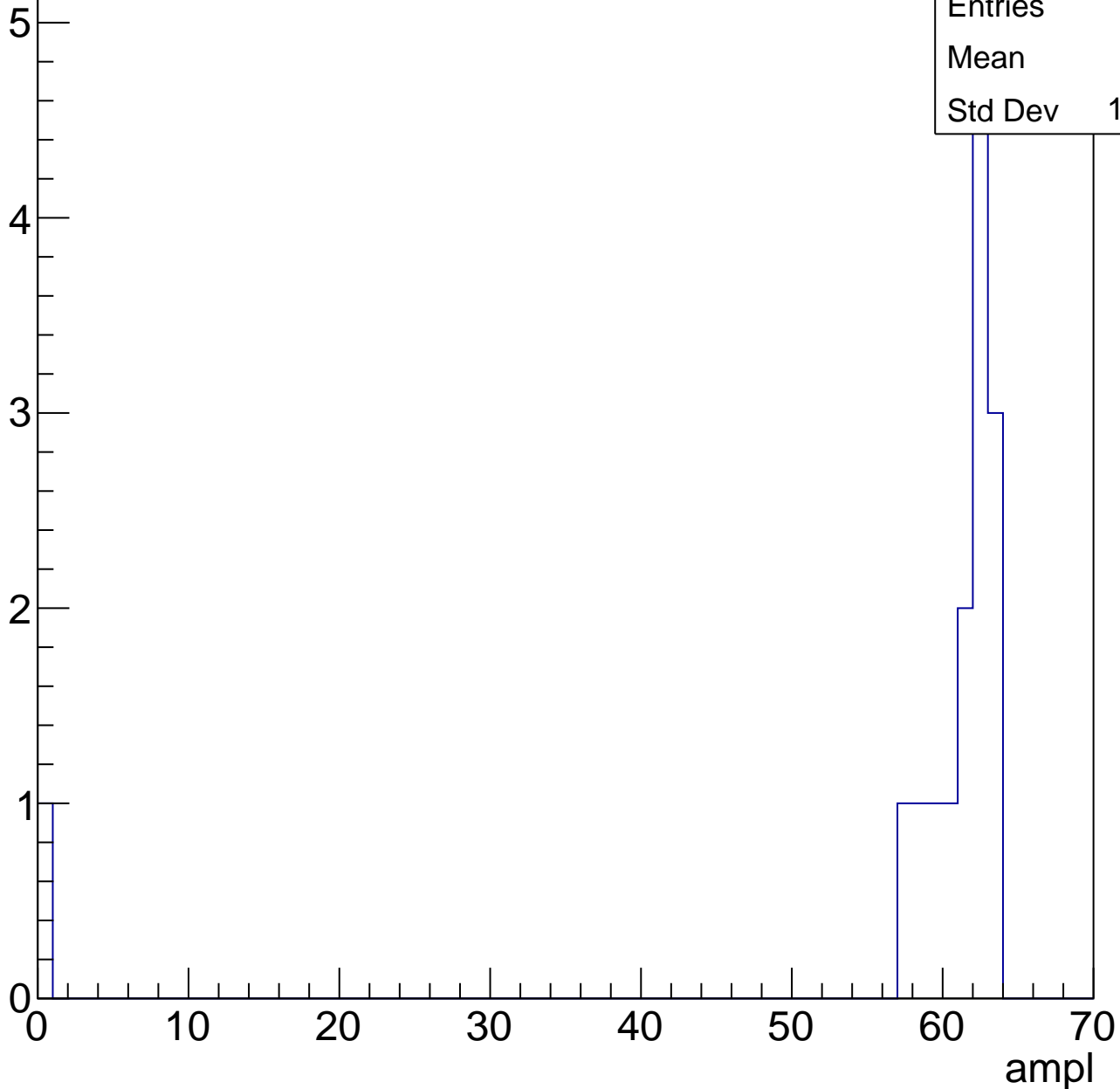


# B1L101S, U3-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	15
Mean	57
Std Dev	15.34





# B1L101S, U3-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch45, adc0

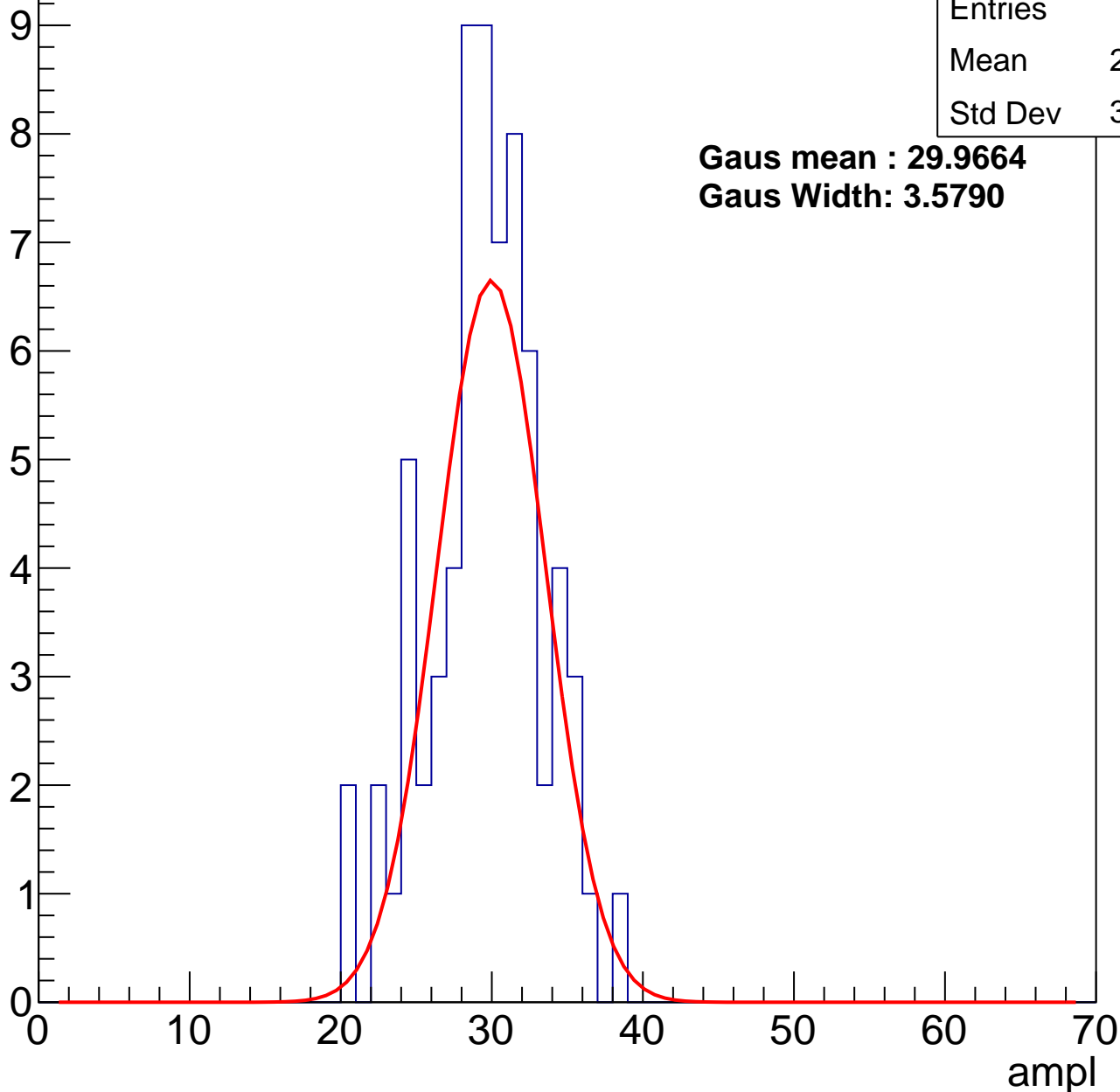
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	29.09
Std Dev	3.745

**Gaus mean : 29.9664**

**Gaus Width: 3.5790**



# B1L101S, U3-ch45, adc1

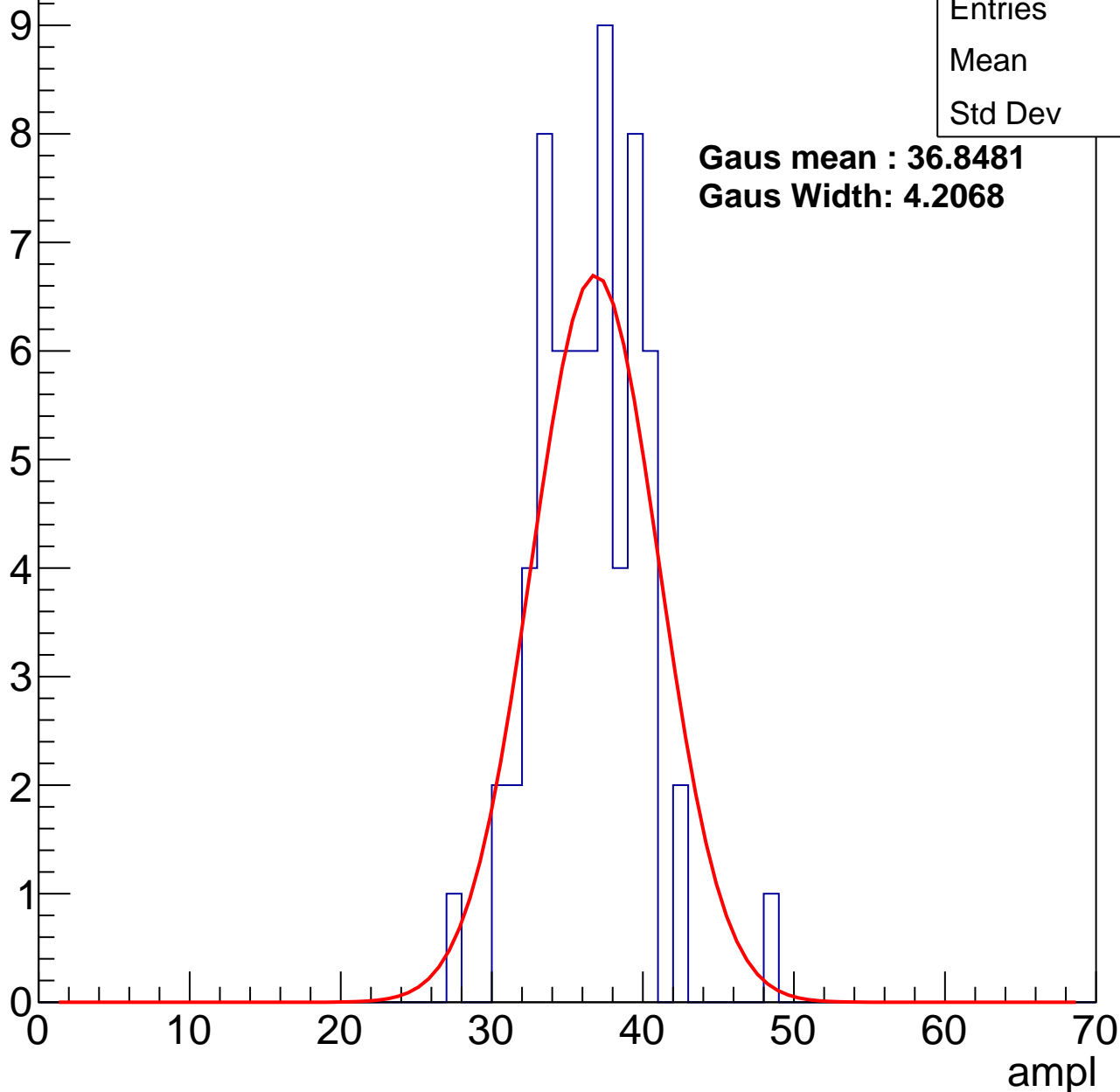
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	36
Std Dev	3.46

**Gaus mean : 36.8481**

**Gaus Width: 4.2068**



# B1L101S, U3-ch45, adc2

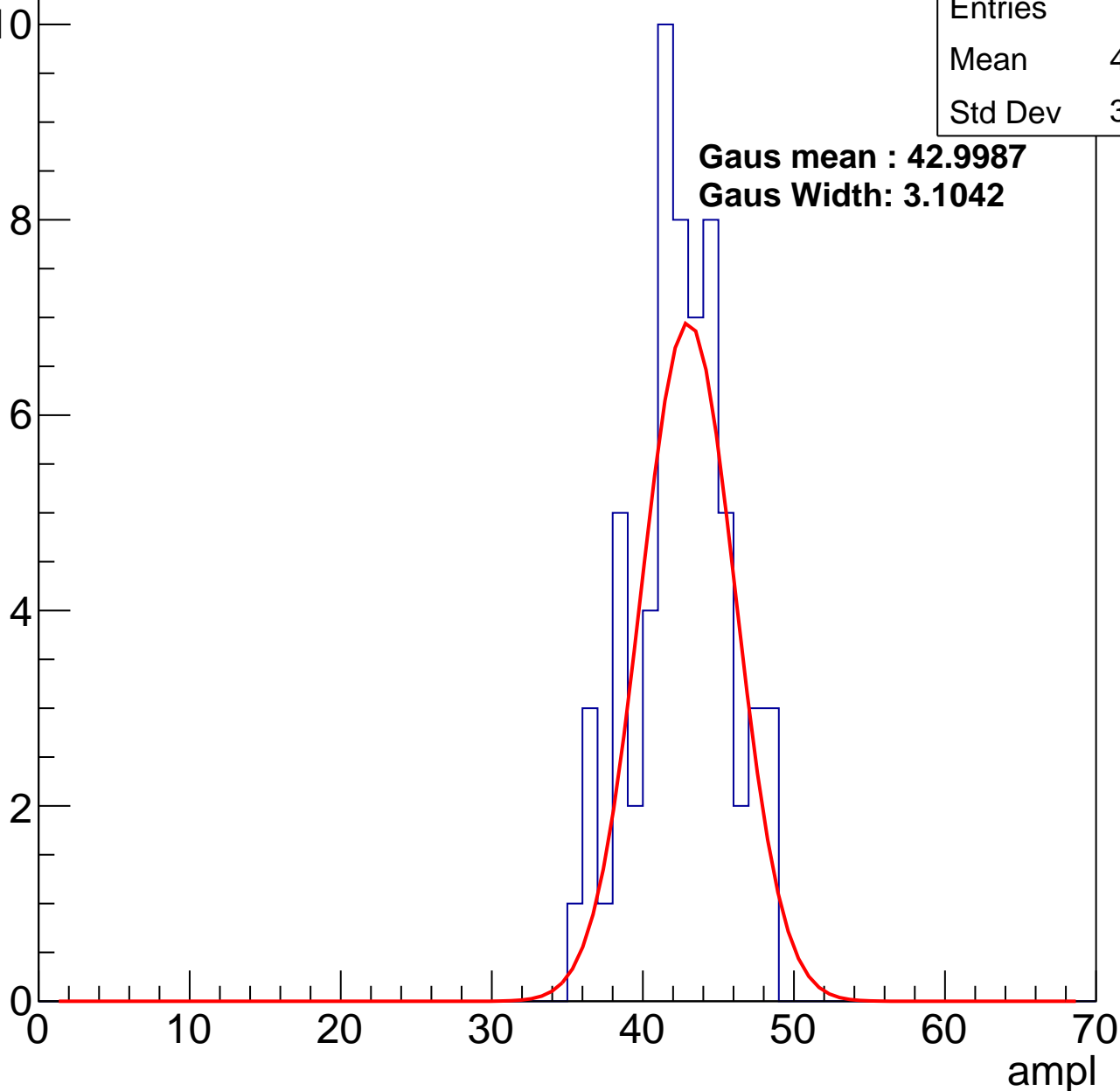
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	42.08
Std Dev	3.123

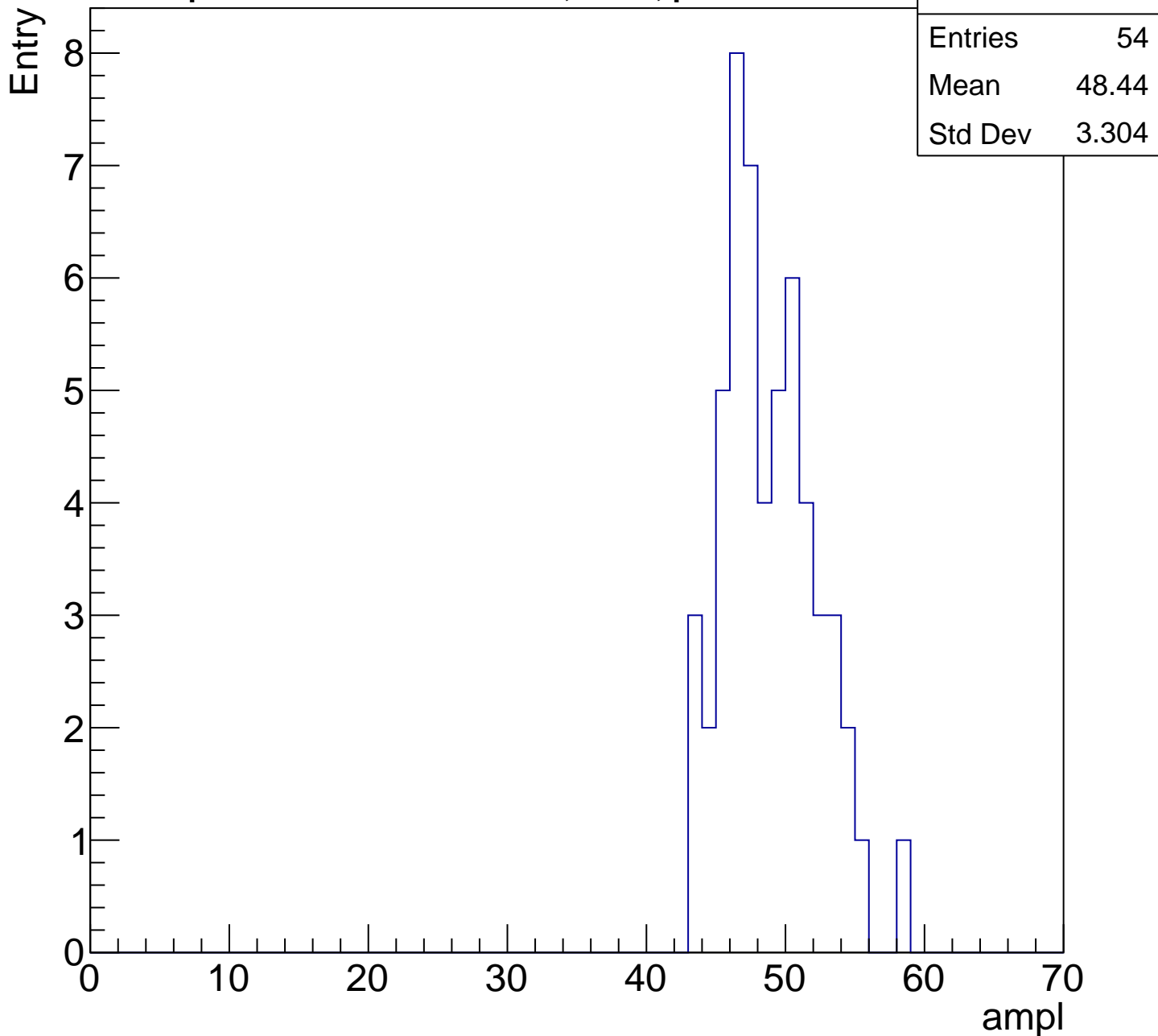
**Gaus mean : 42.9987**

**Gaus Width: 3.1042**



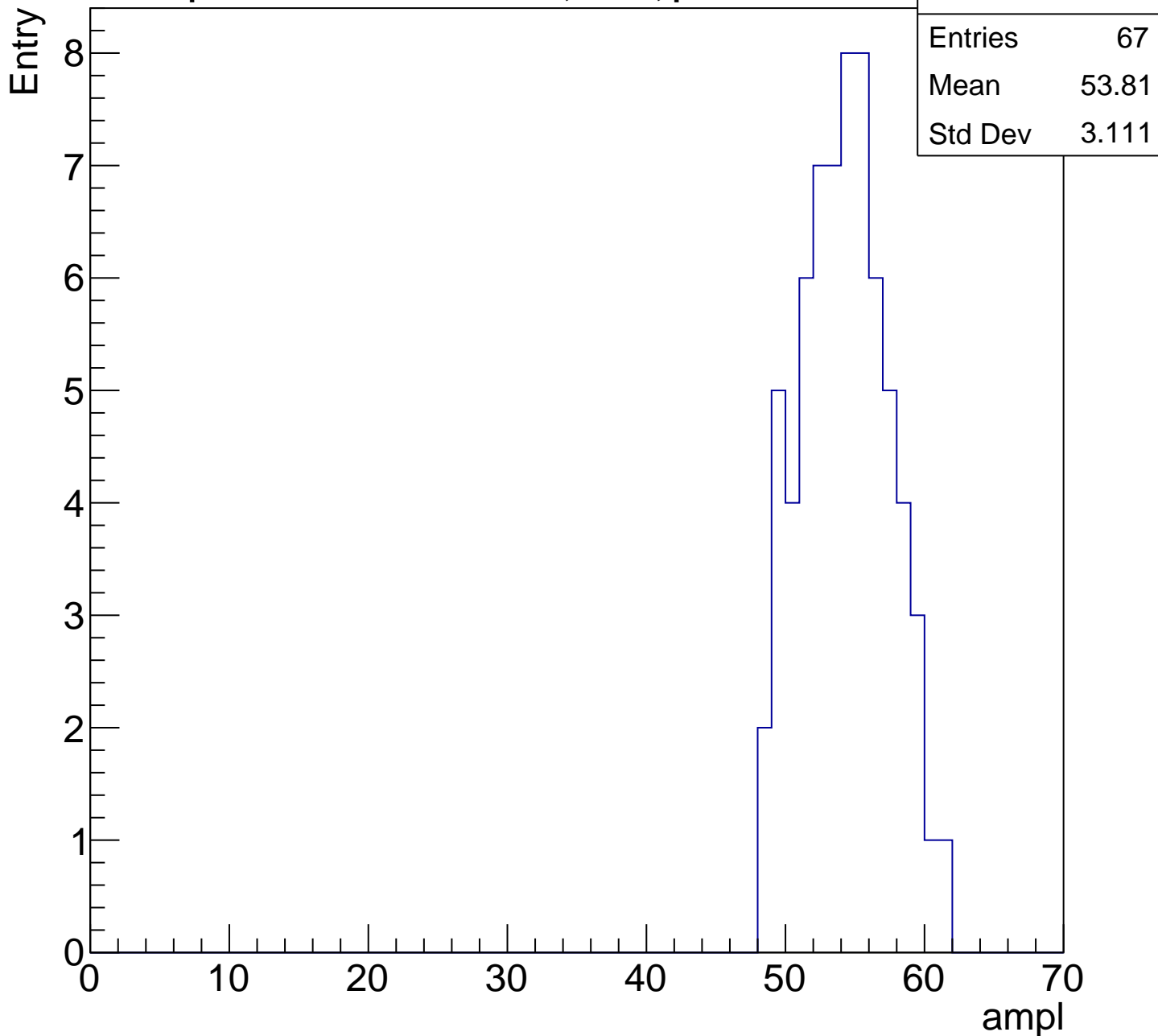
# B1L101S, U3-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch45, adc4

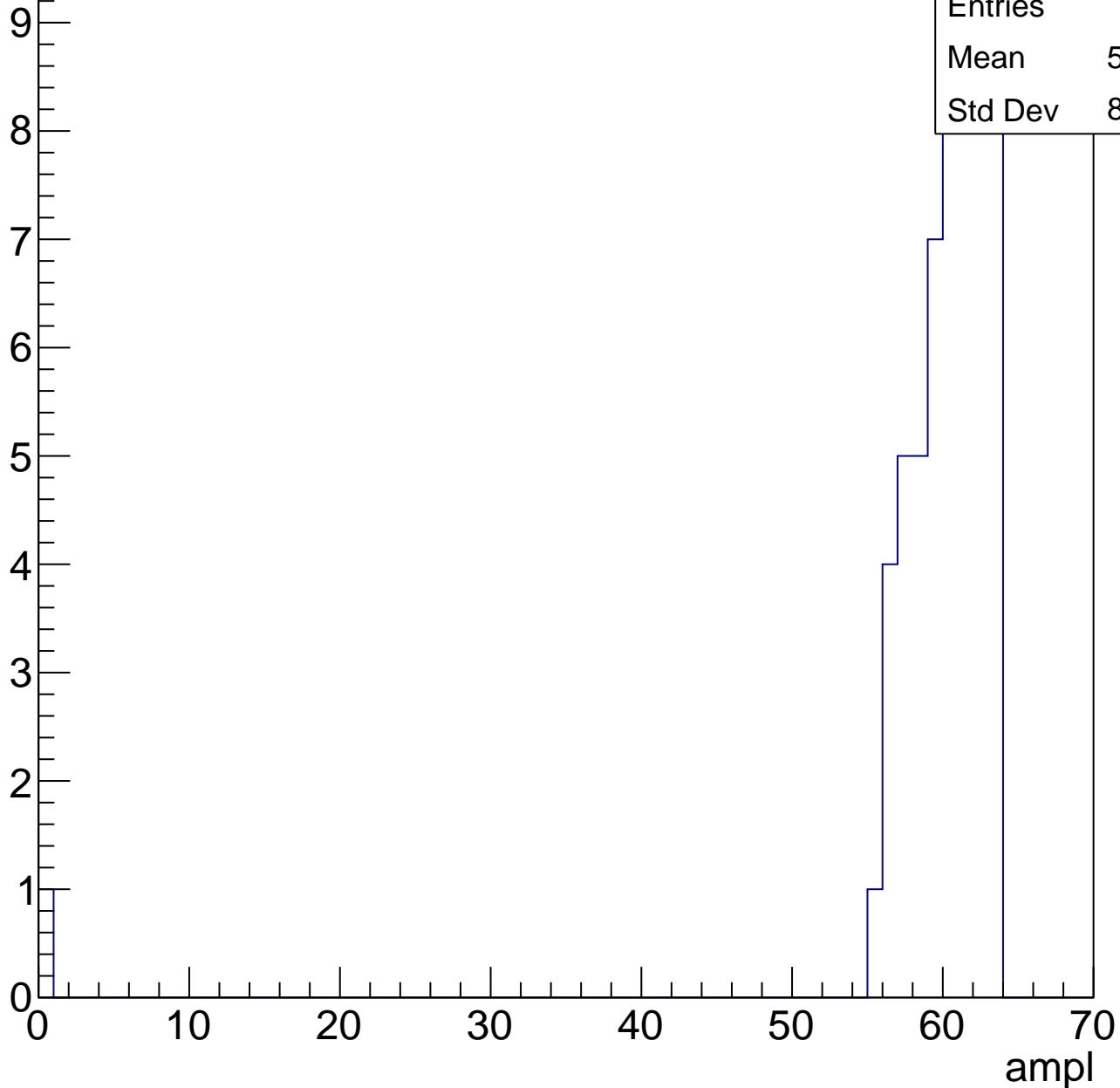
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

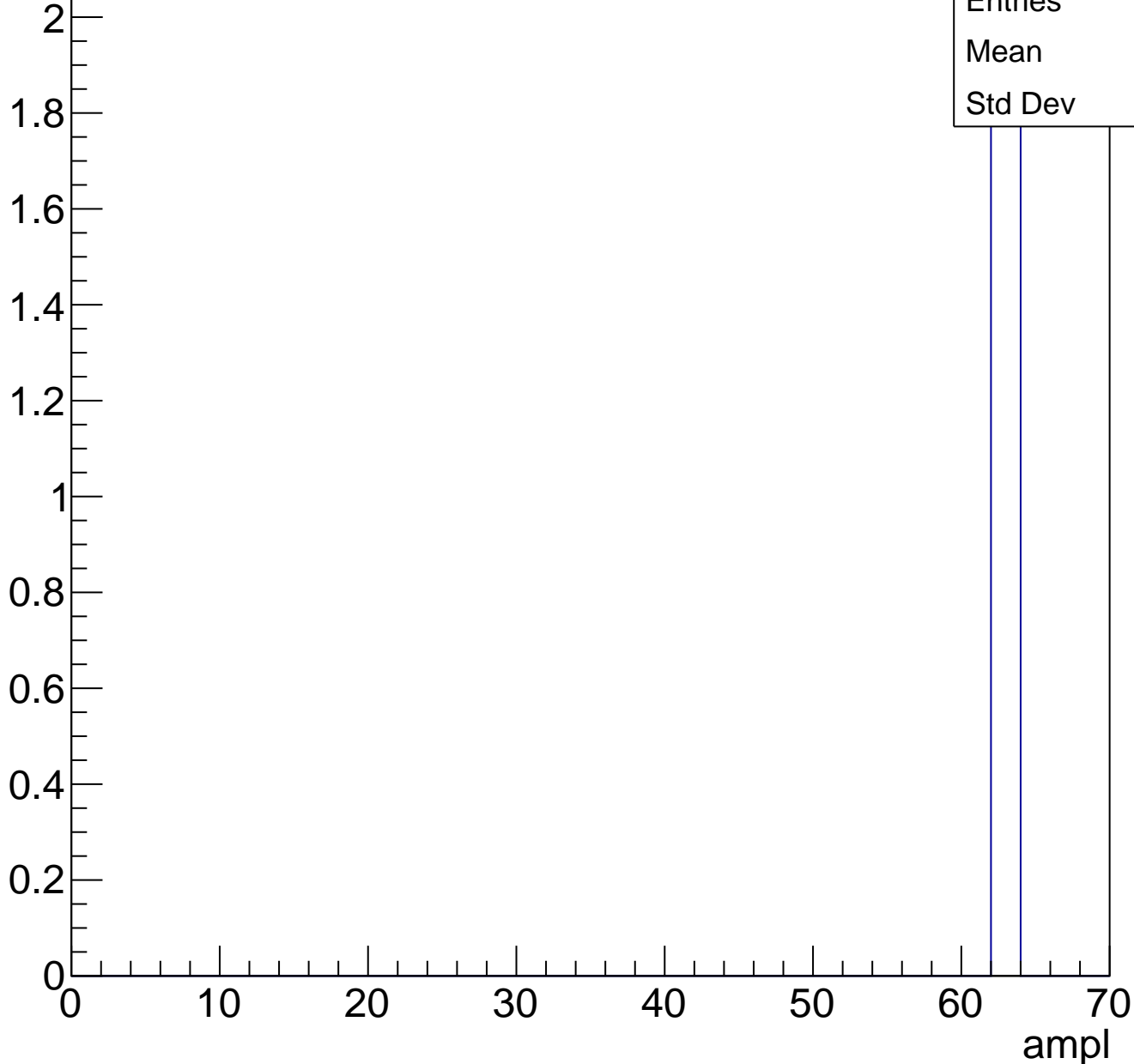
Entry



# B1L101S, U3-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U3-ch46, adc0

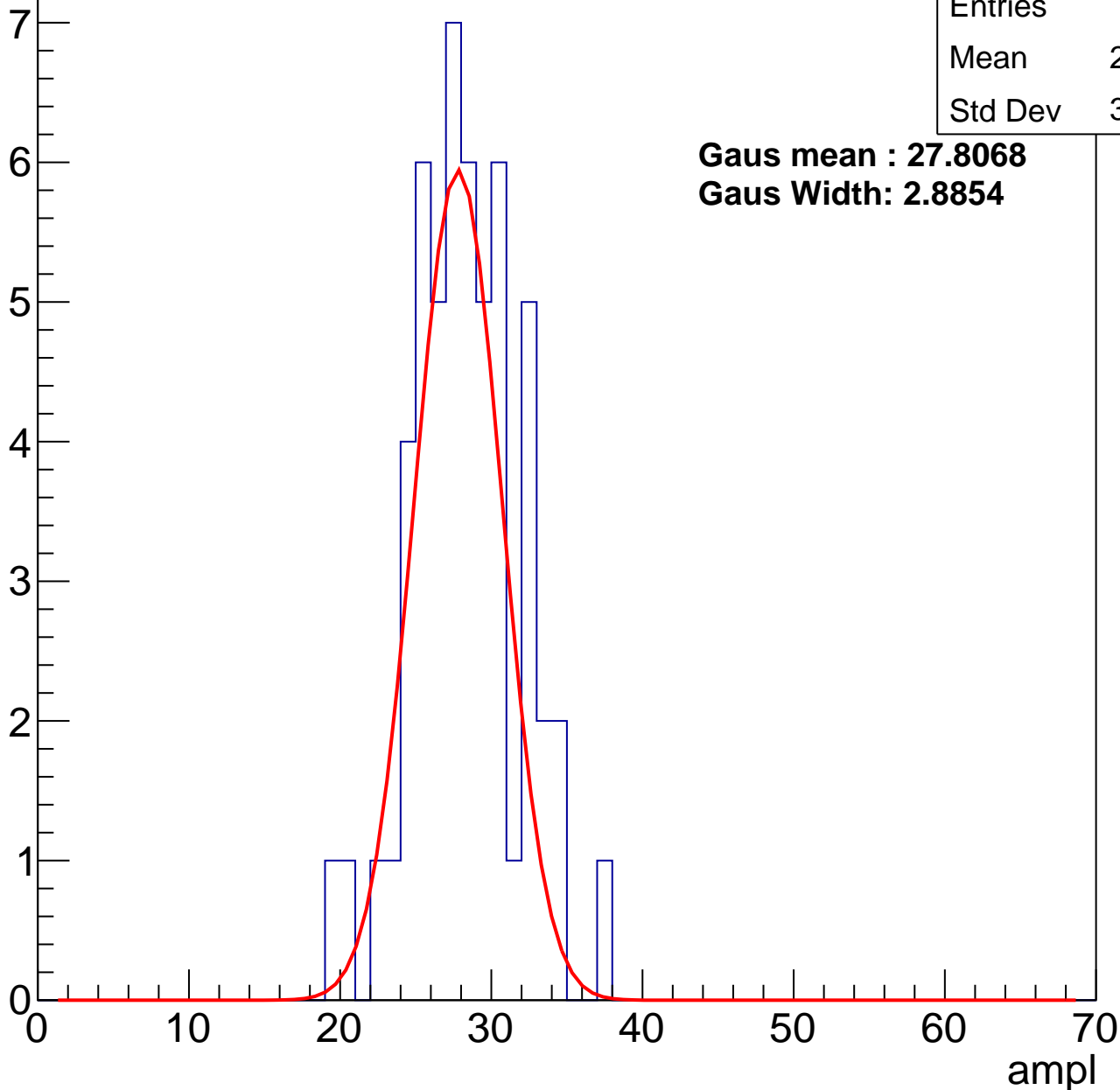
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	27.85
Std Dev	3.525

**Gaus mean : 27.8068**

**Gaus Width: 2.8854**



# B1L101S, U3-ch46, adc1

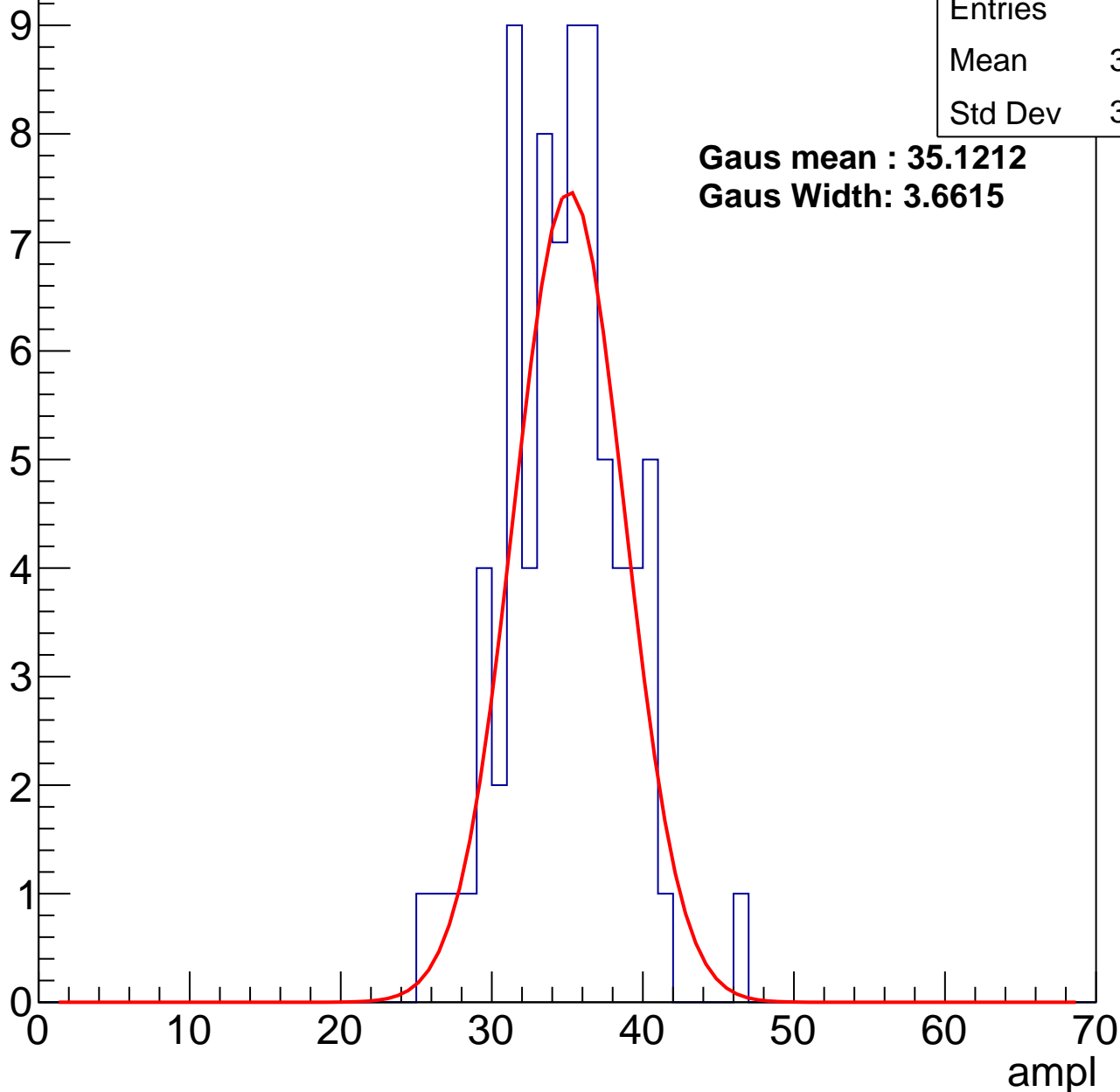
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	34.34
Std Dev	3.779

**Gaus mean : 35.1212**

**Gaus Width: 3.6615**



# B1L101S, U3-ch46, adc2

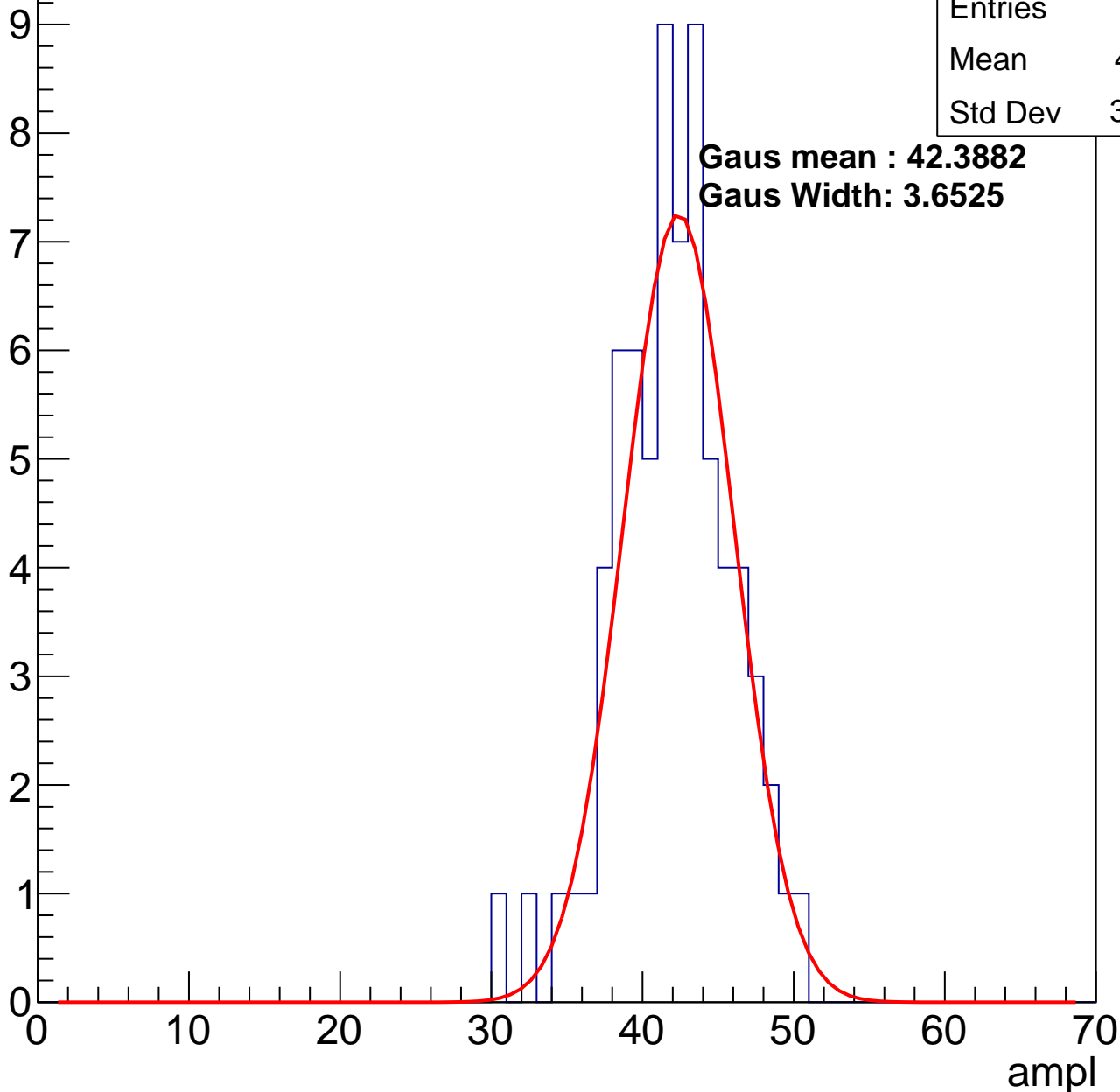
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	41.51
Std Dev	3.834

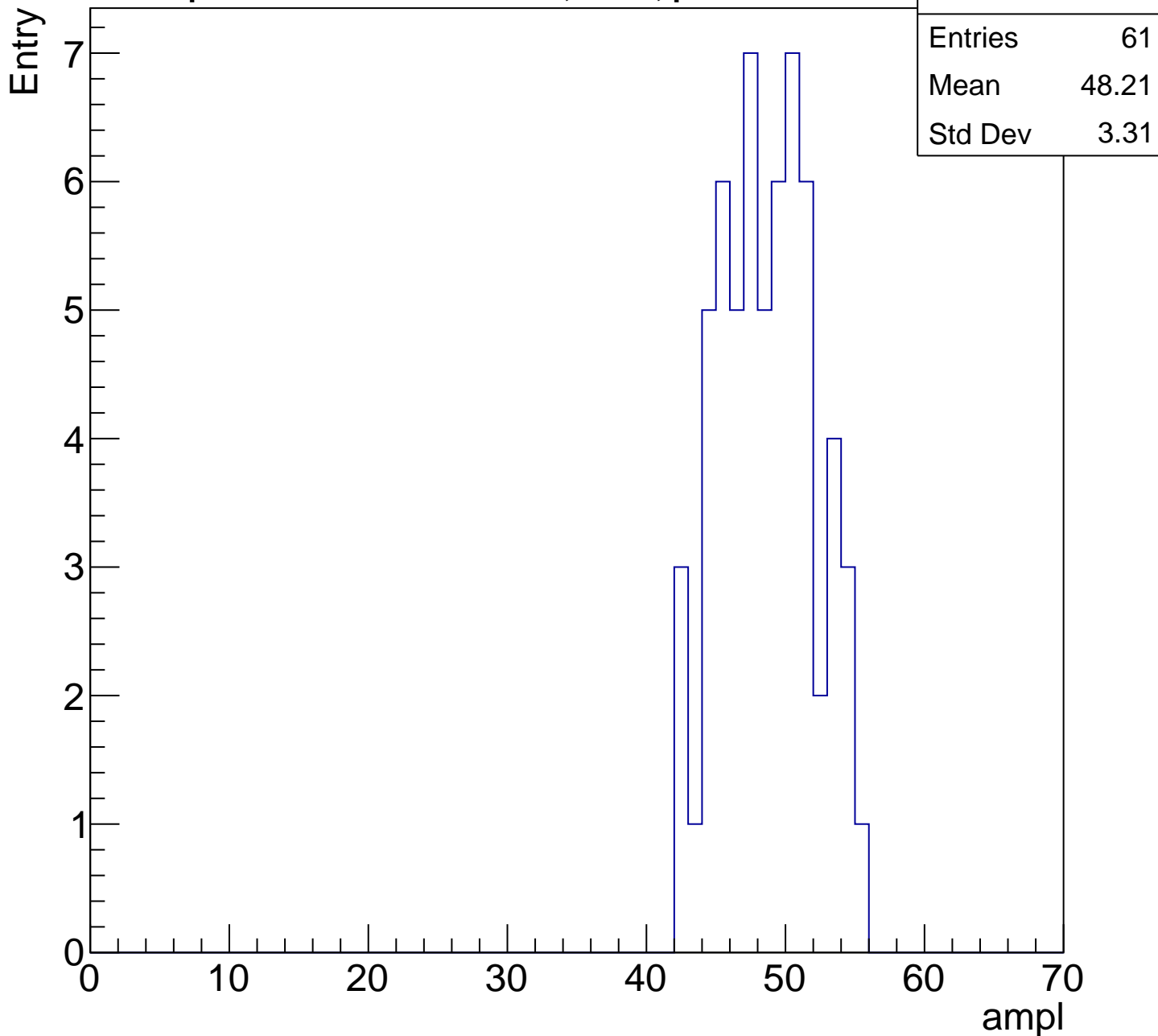
**Gaus mean : 42.3882**

**Gaus Width: 3.6525**



# B1L101S, U3-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

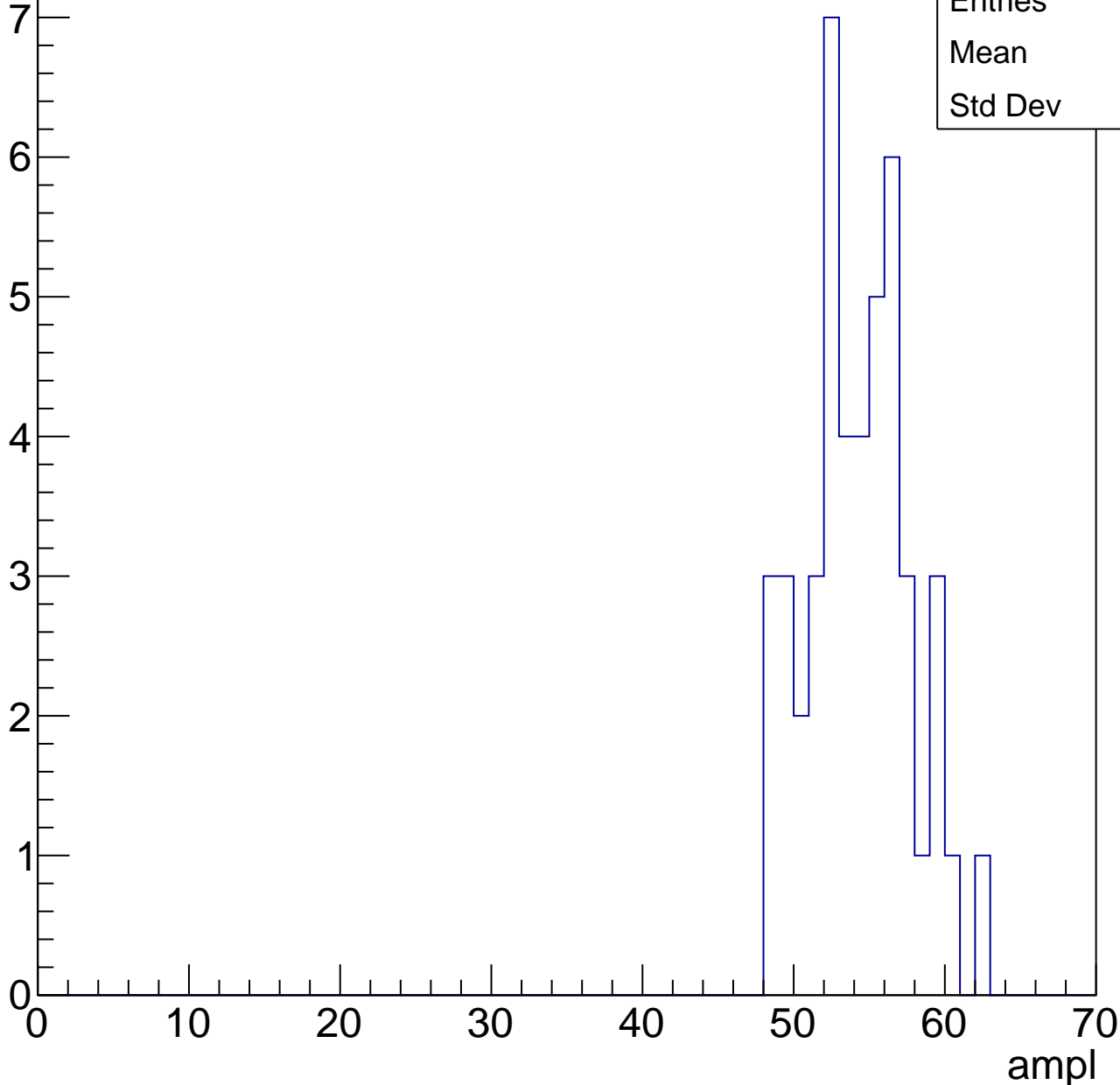


# B1L101S, U3-ch46, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	53.8
Std Dev	3.36

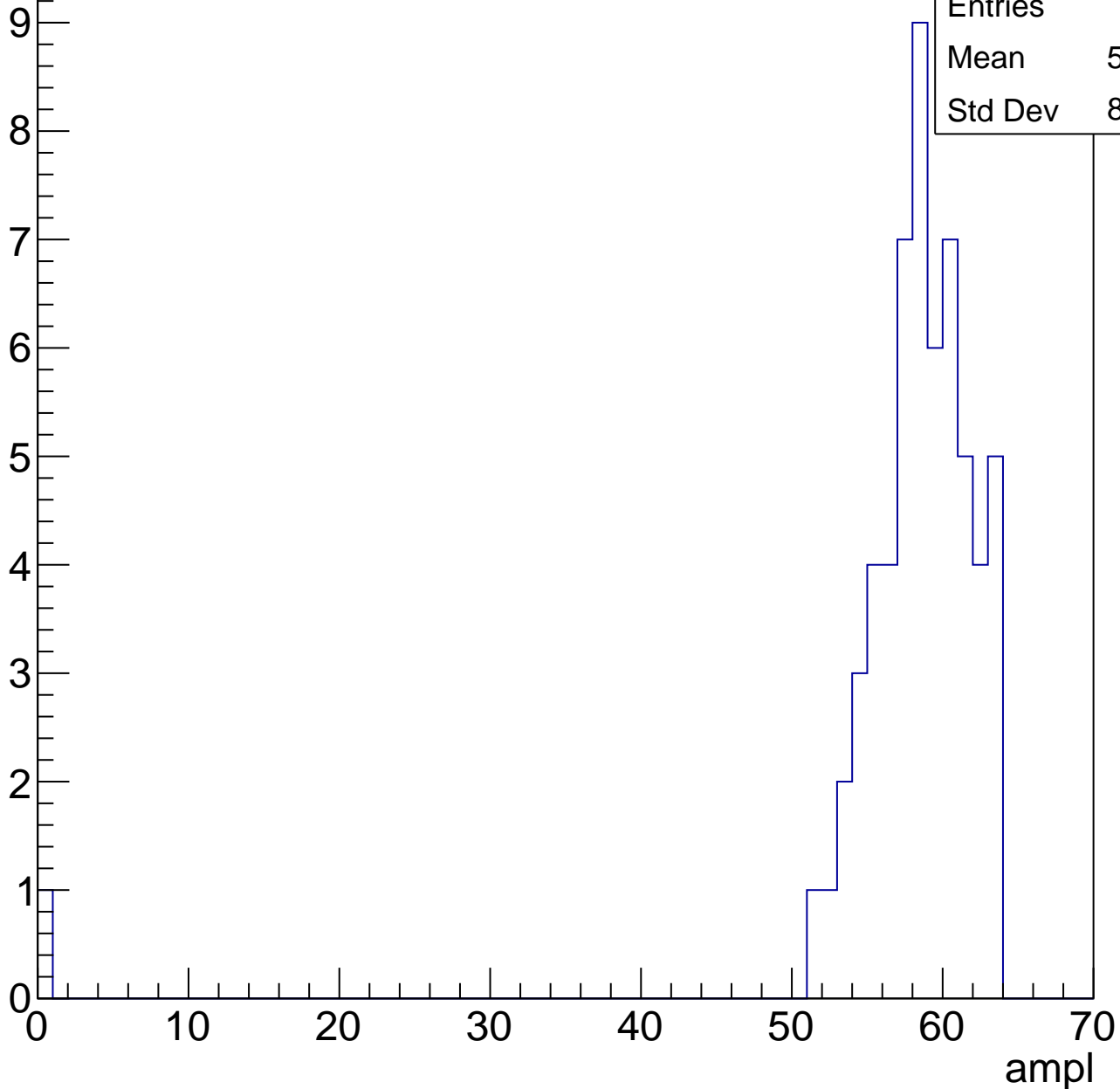


# B1L101S, U3-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	57.25
Std Dev	8.069

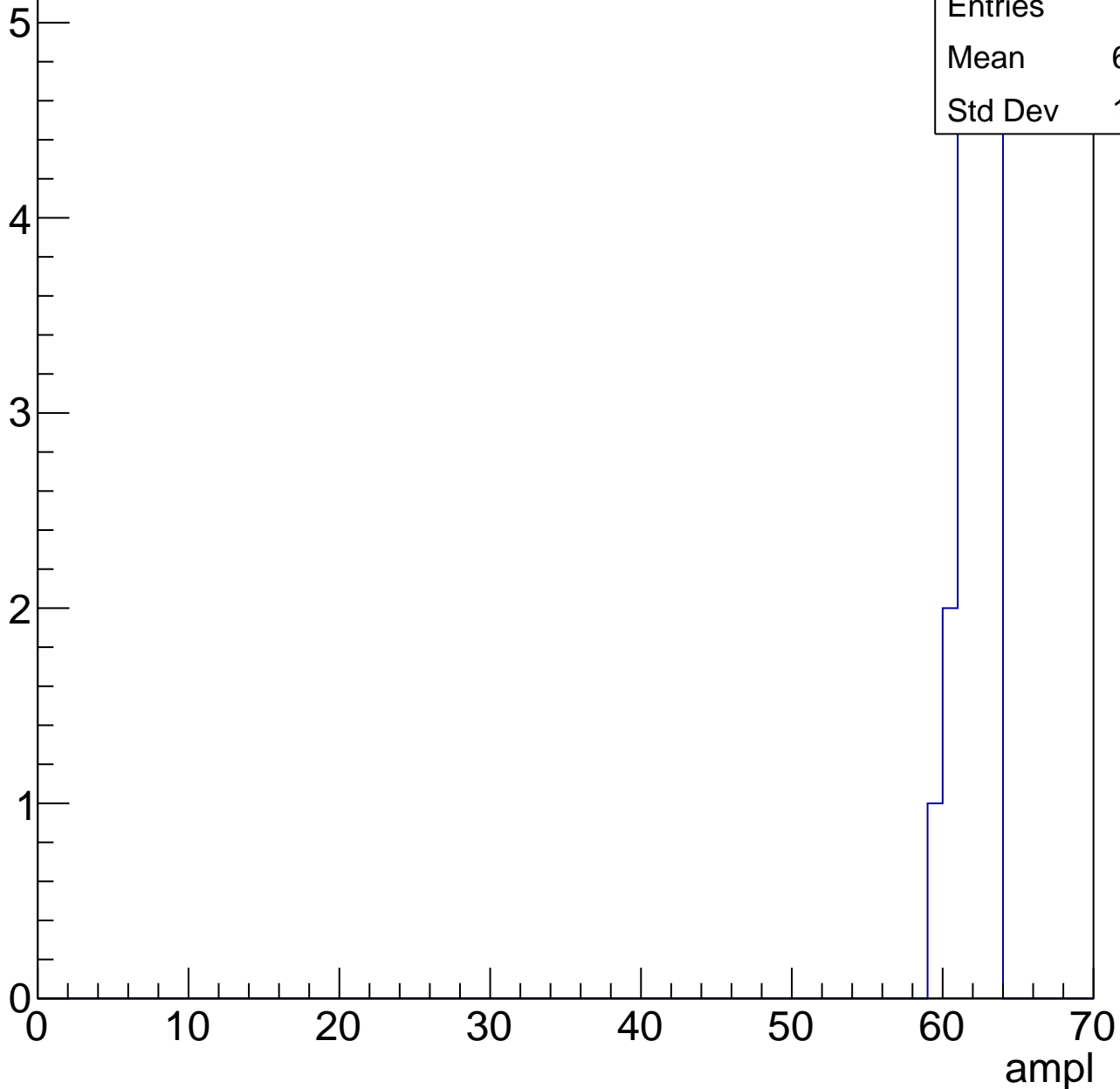


# B1L101S, U3-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	18
Mean	61.61
Std Dev	1.161





# B1L101S, U3-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	9.5
Std Dev	9.5

# B1L101S, U3-ch47, adc0

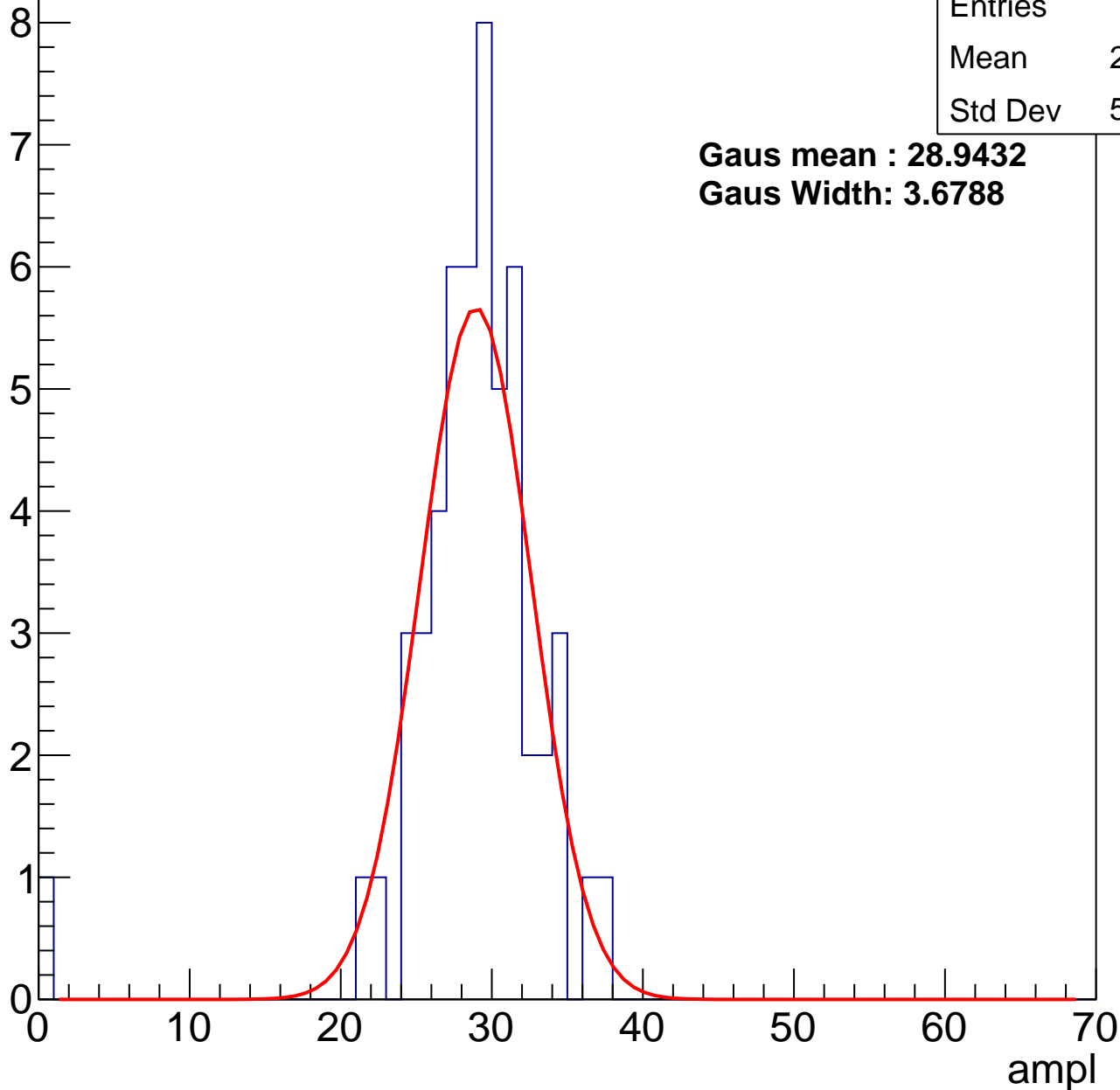
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	28.25
Std Dev	5.102

**Gaus mean : 28.9432**

**Gaus Width: 3.6788**



# B1L101S, U3-ch47, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	81
Mean	35.2
Std Dev	3.901

**Gaus mean : 35.7985**

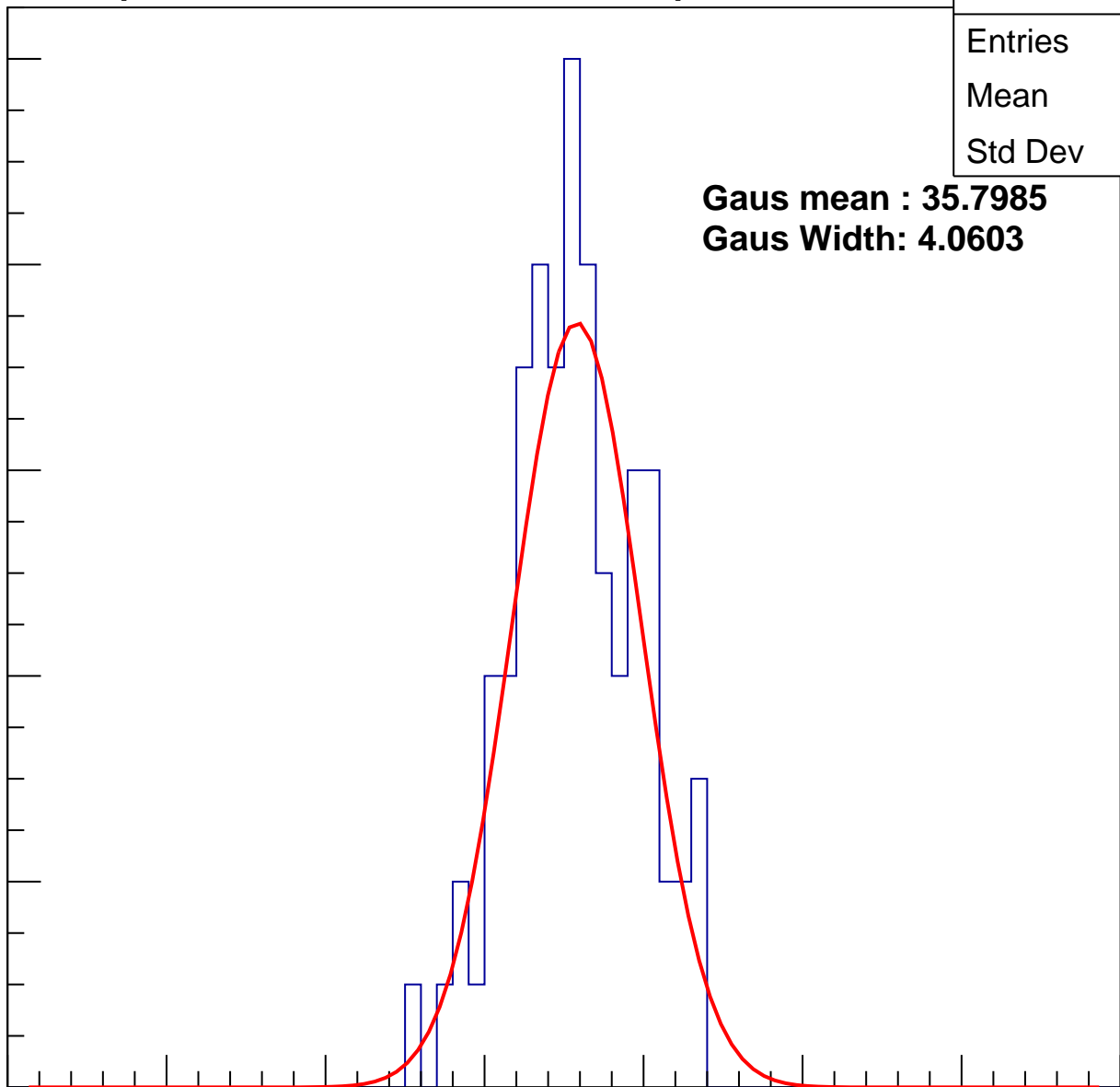
**Gaus Width: 4.0603**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U3-ch47, adc2

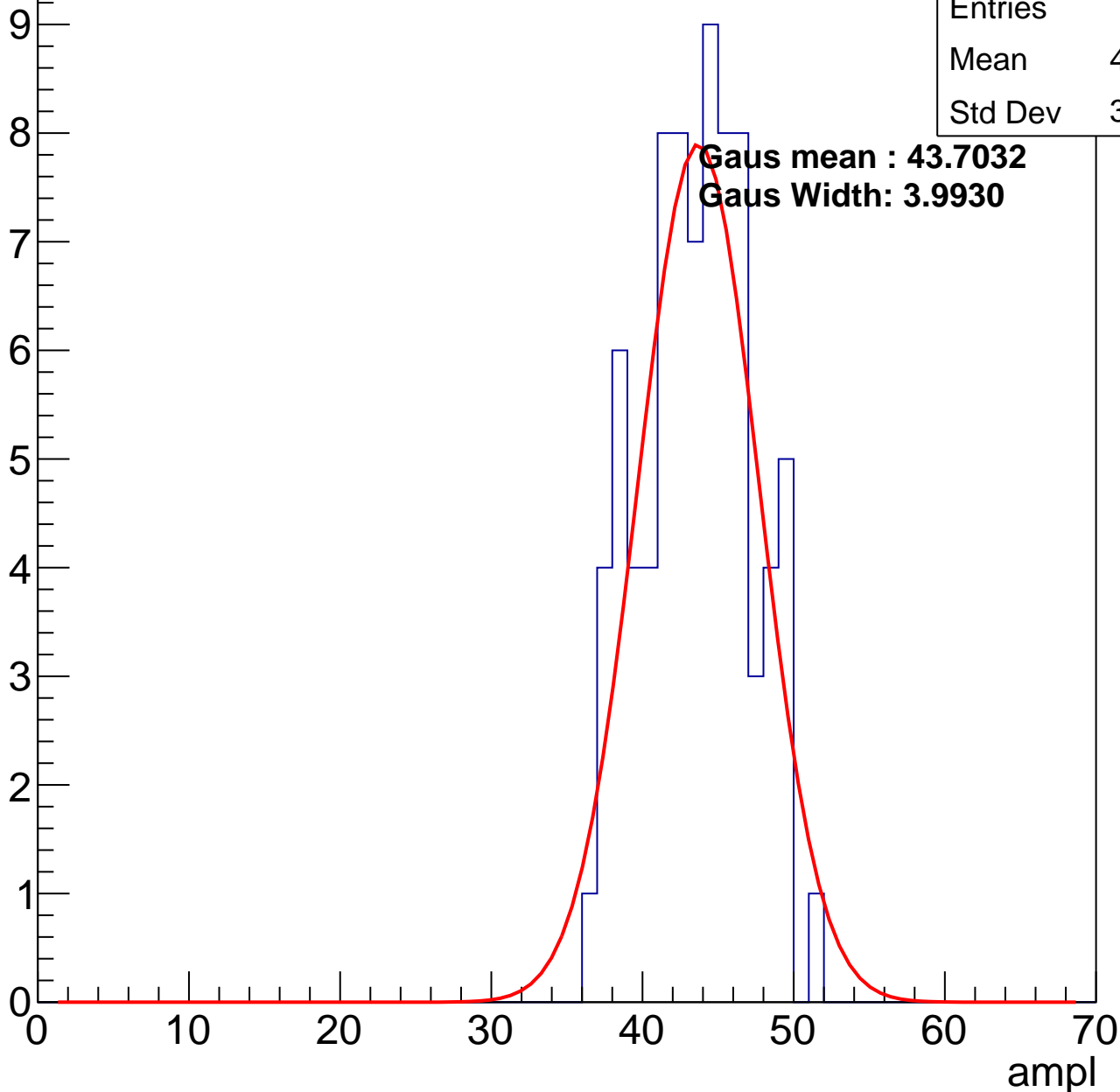
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	43.08
Std Dev	3.513

**Gaus mean : 43.7032**

**Gaus Width: 3.9930**

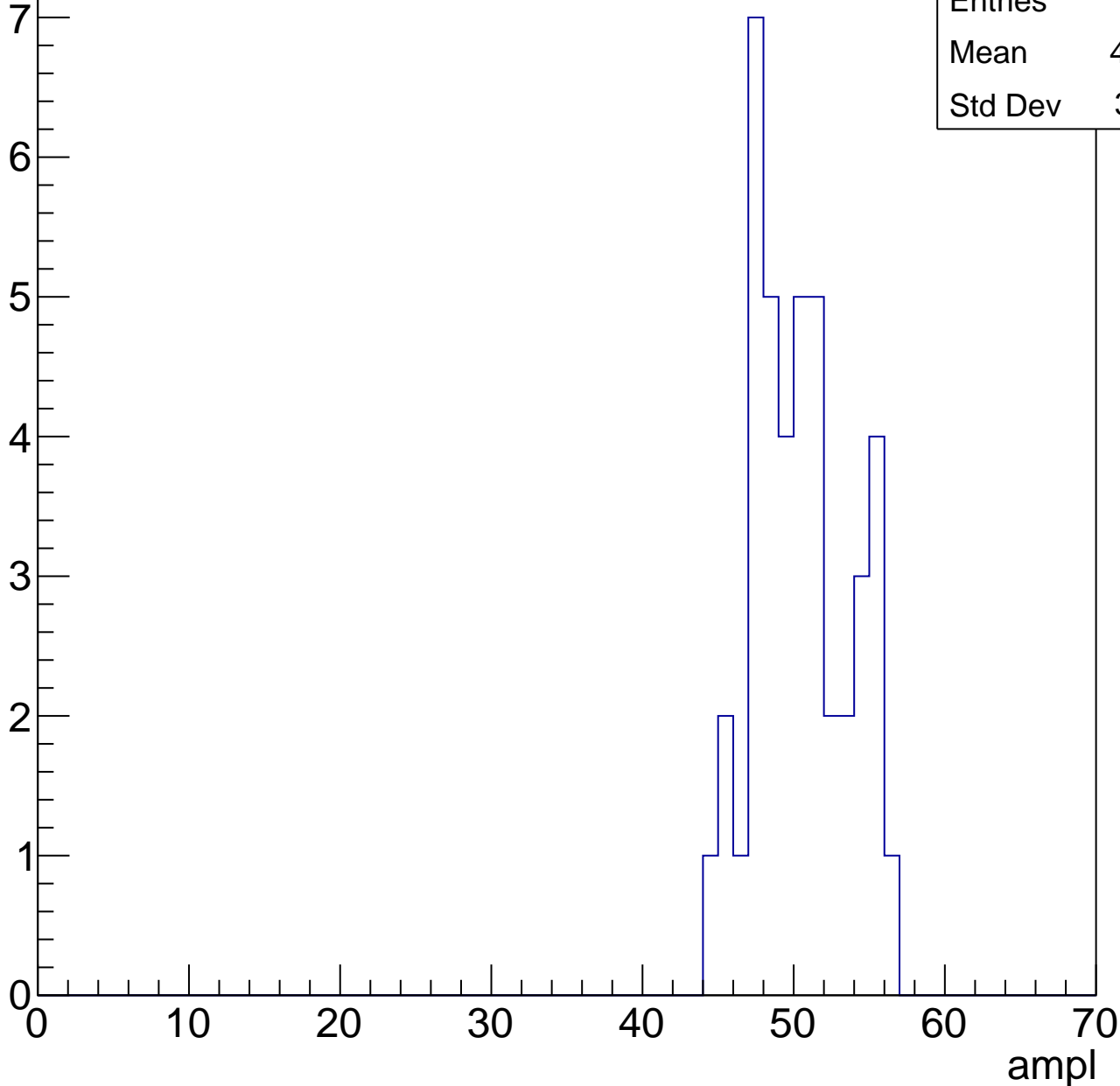


# B1L101S, U3-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	49.95
Std Dev	3.101

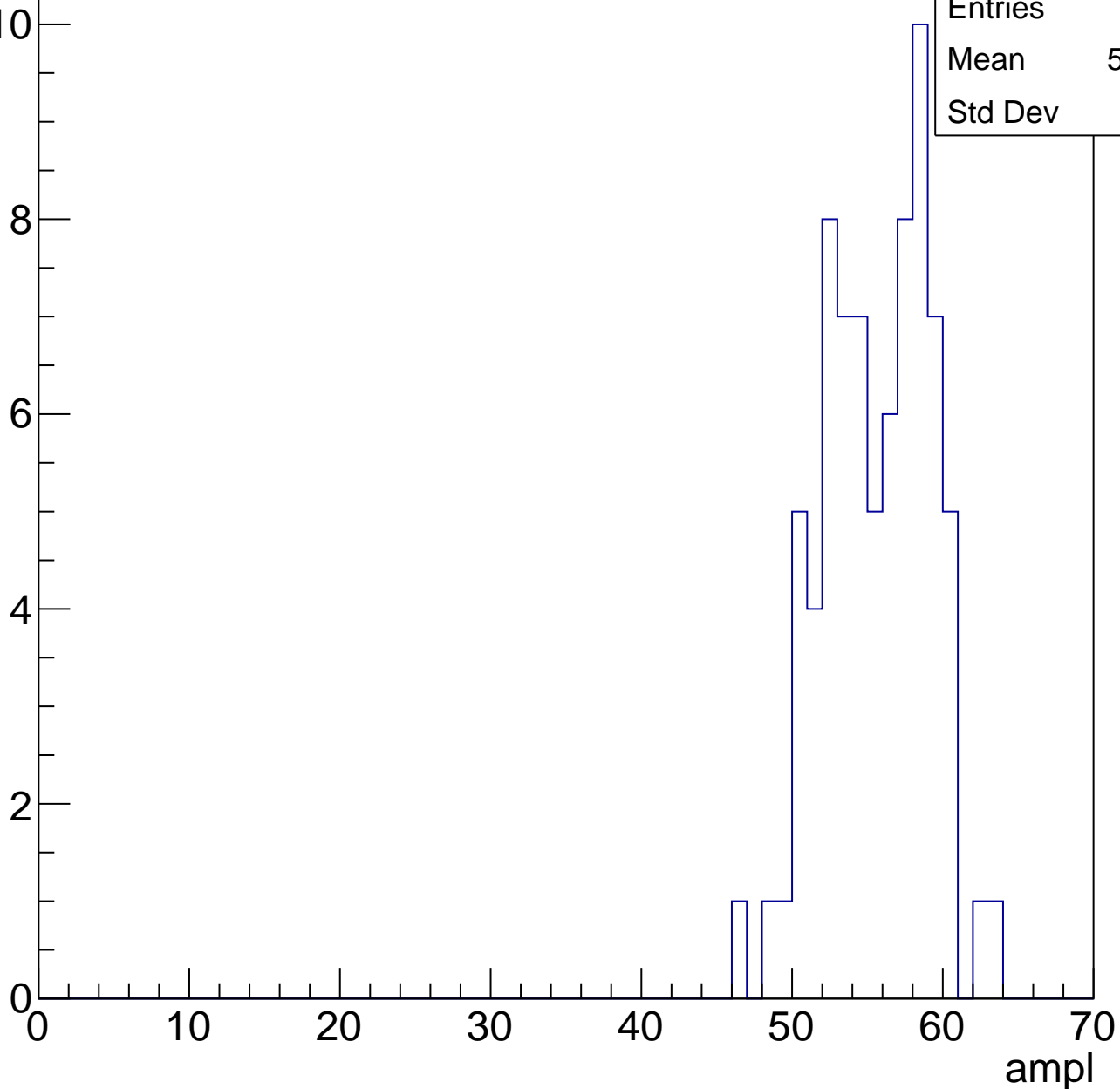


# B1L101S, U3-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

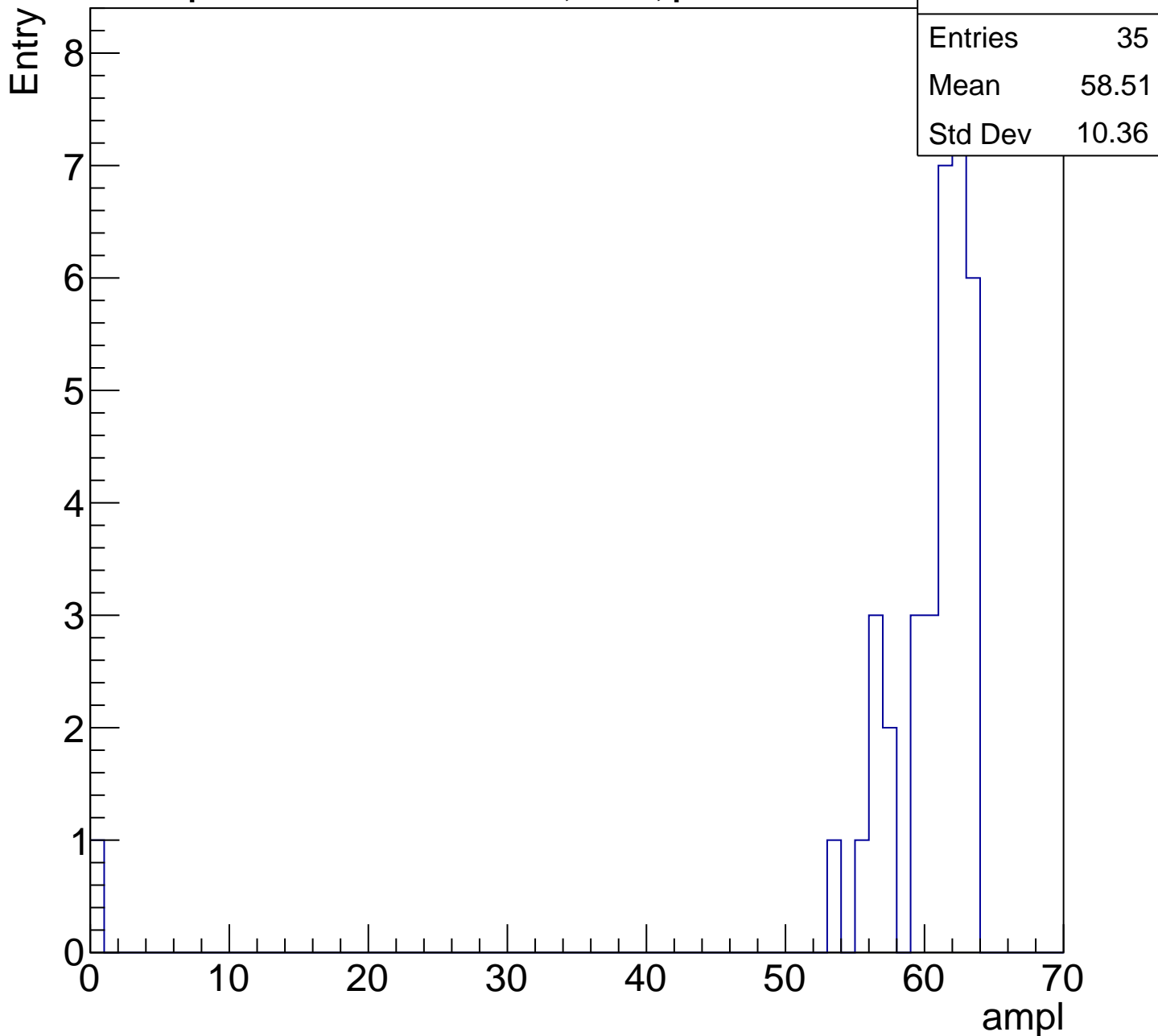
Entry

Entries	77
Mean	55.16
Std Dev	3.49



# B1L101S, U3-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch47, adc6

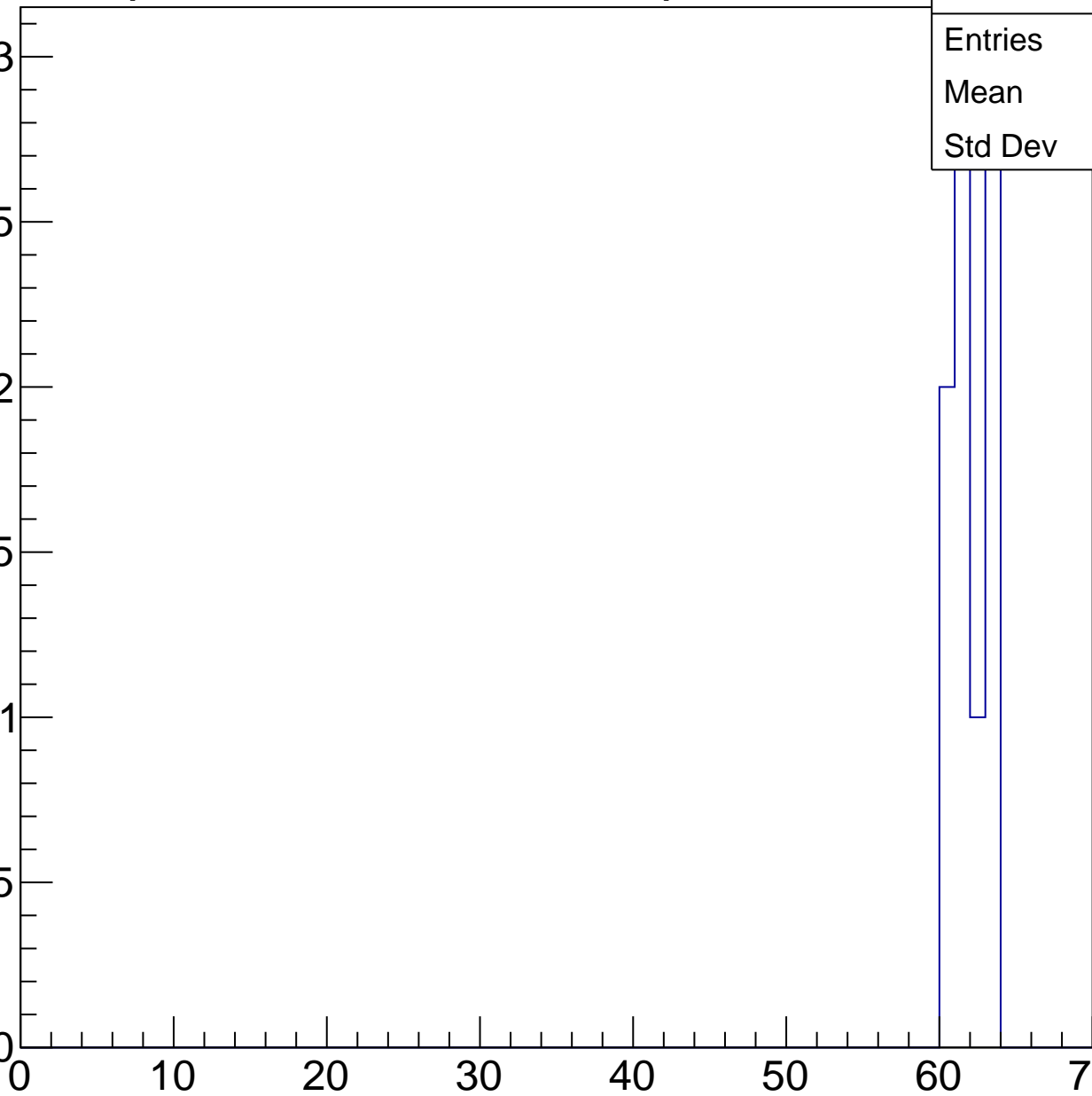
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	9
Mean	61.56
Std Dev	1.165

ampl





# B1L101S, U3-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch48, adc0

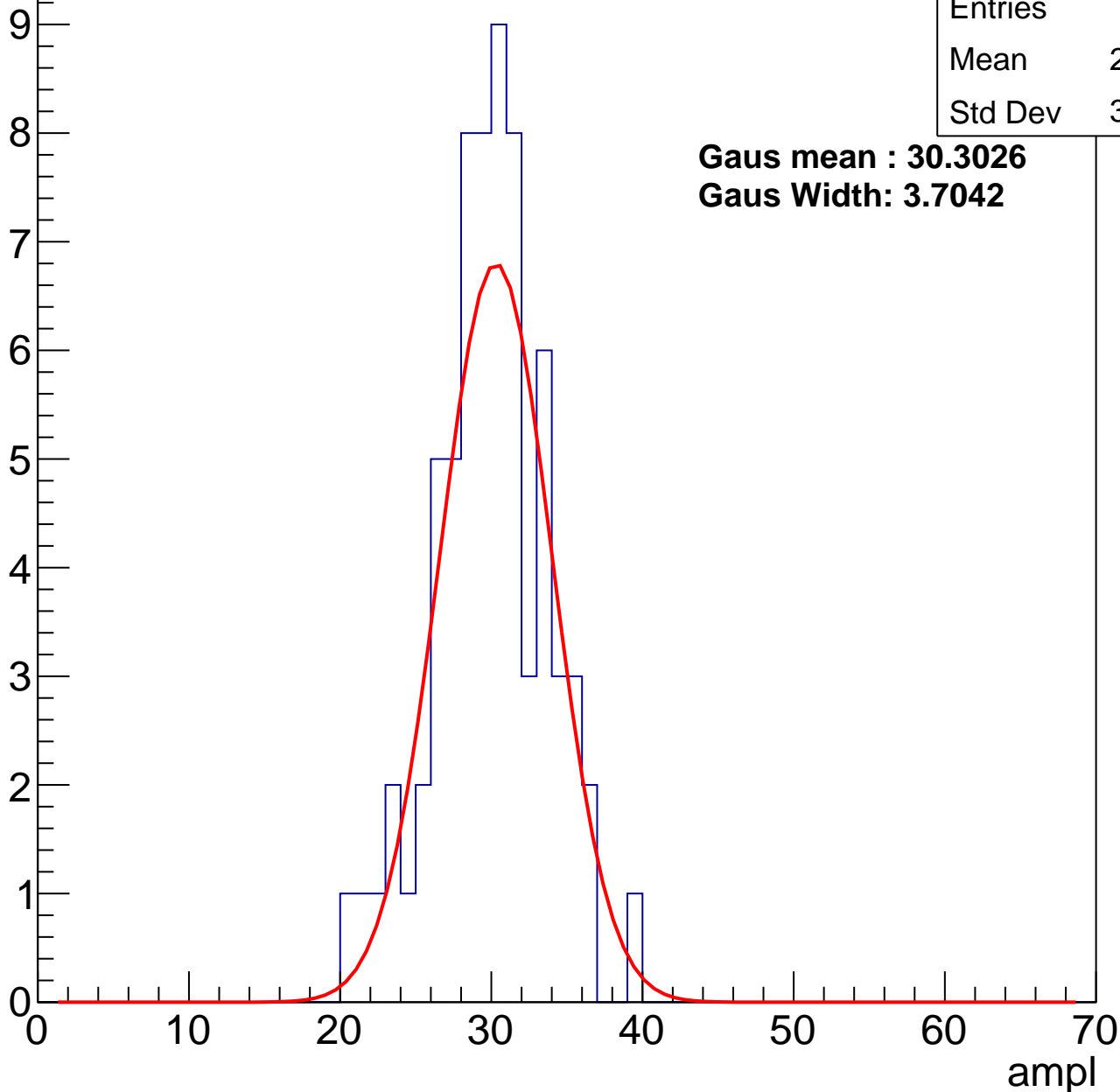
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	29.48
Std Dev	3.662

**Gaus mean : 30.3026**

**Gaus Width: 3.7042**



# B1L101S, U3-ch48, adc1

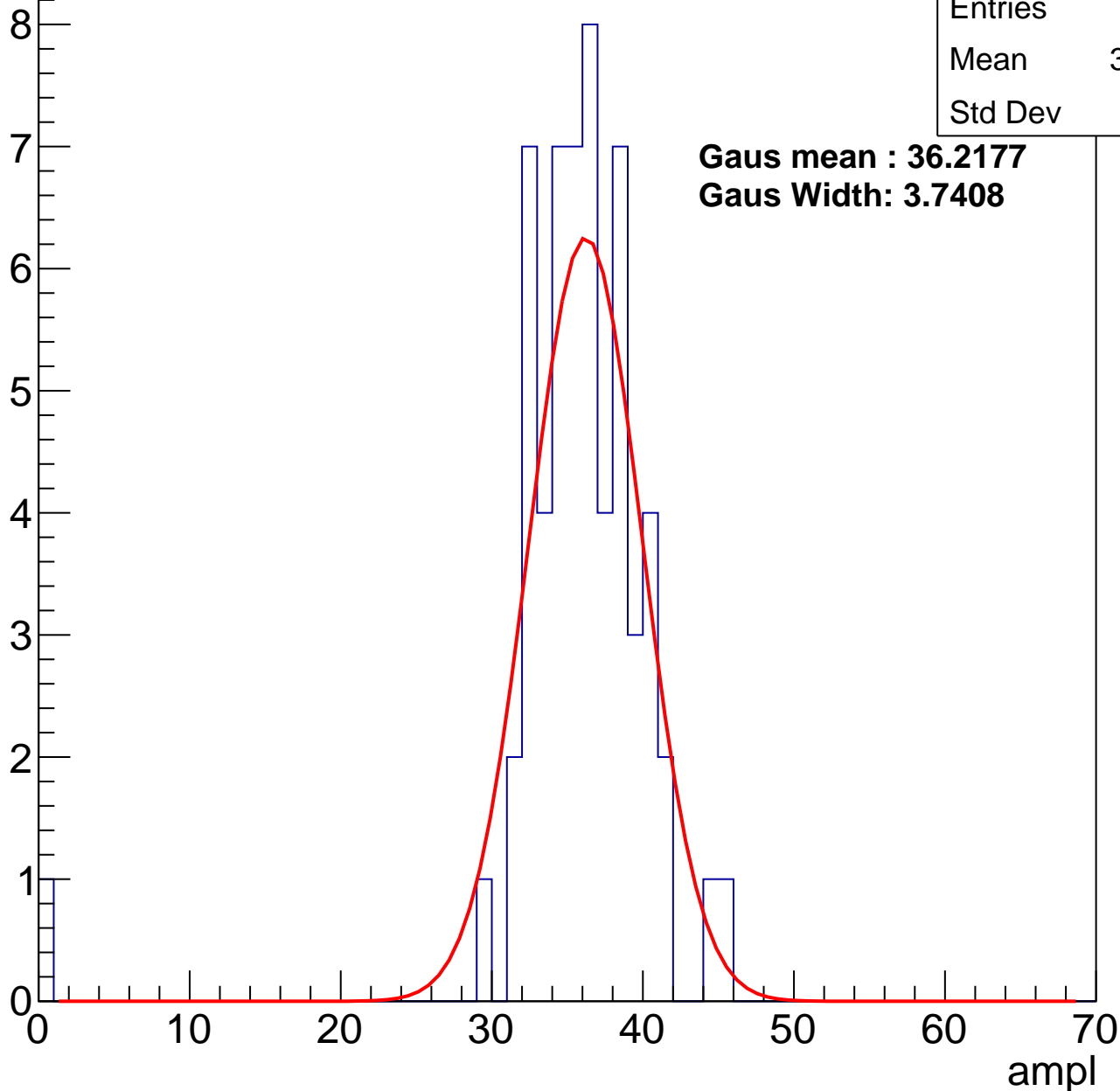
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	35.25
Std Dev	5.62

**Gaus mean : 36.2177**

**Gaus Width: 3.7408**



# B1L101S, U3-ch48, adc2

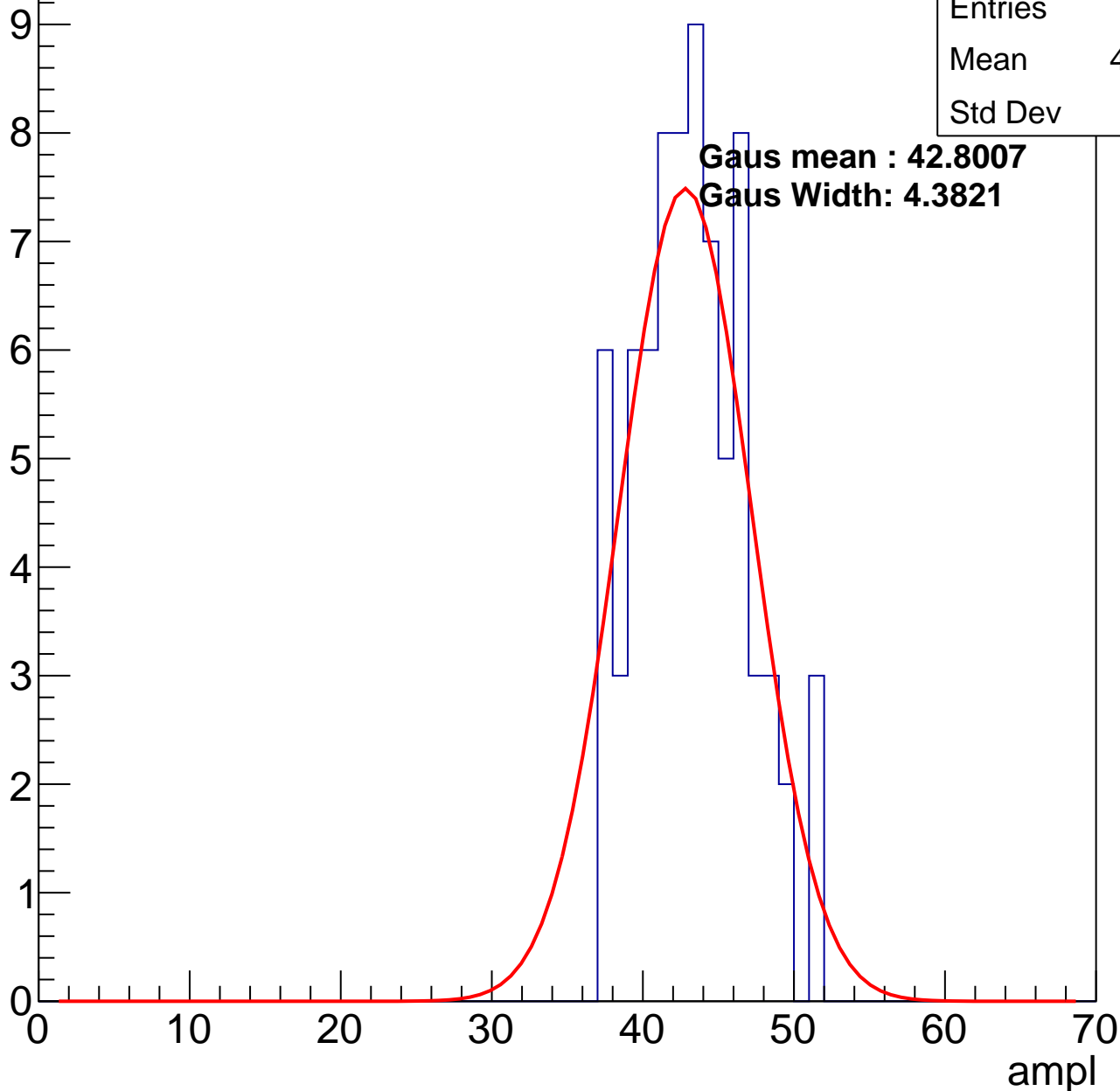
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	42.83
Std Dev	3.54

**Gaus mean : 42.8007**

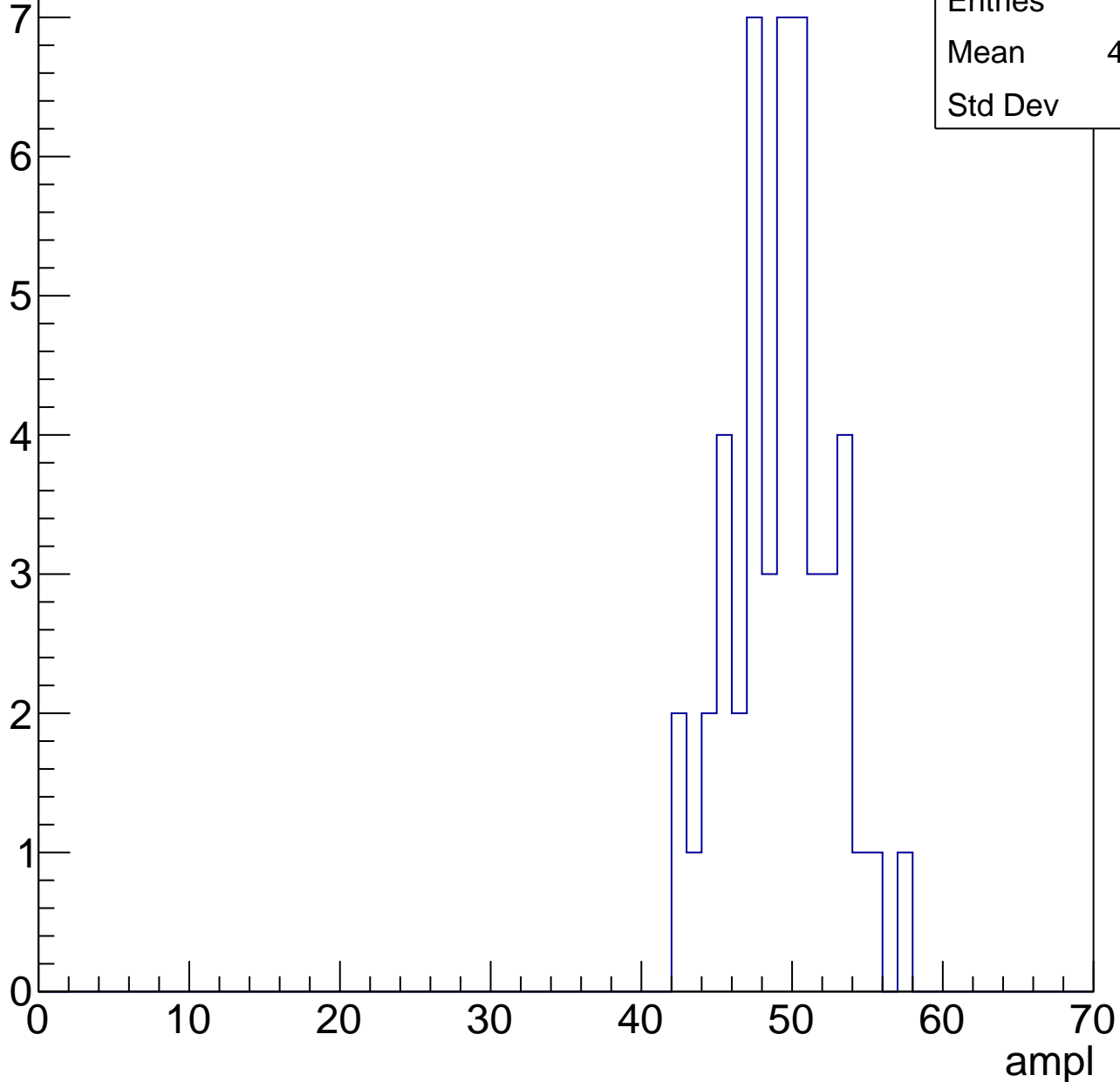
**Gaus Width: 4.3821**



# B1L101S, U3-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

Entries 46

Mean 53.57

Std Dev 2.968

ampl

0

10

20

30

40

50

60

70

0

10

20

30

40

50

60

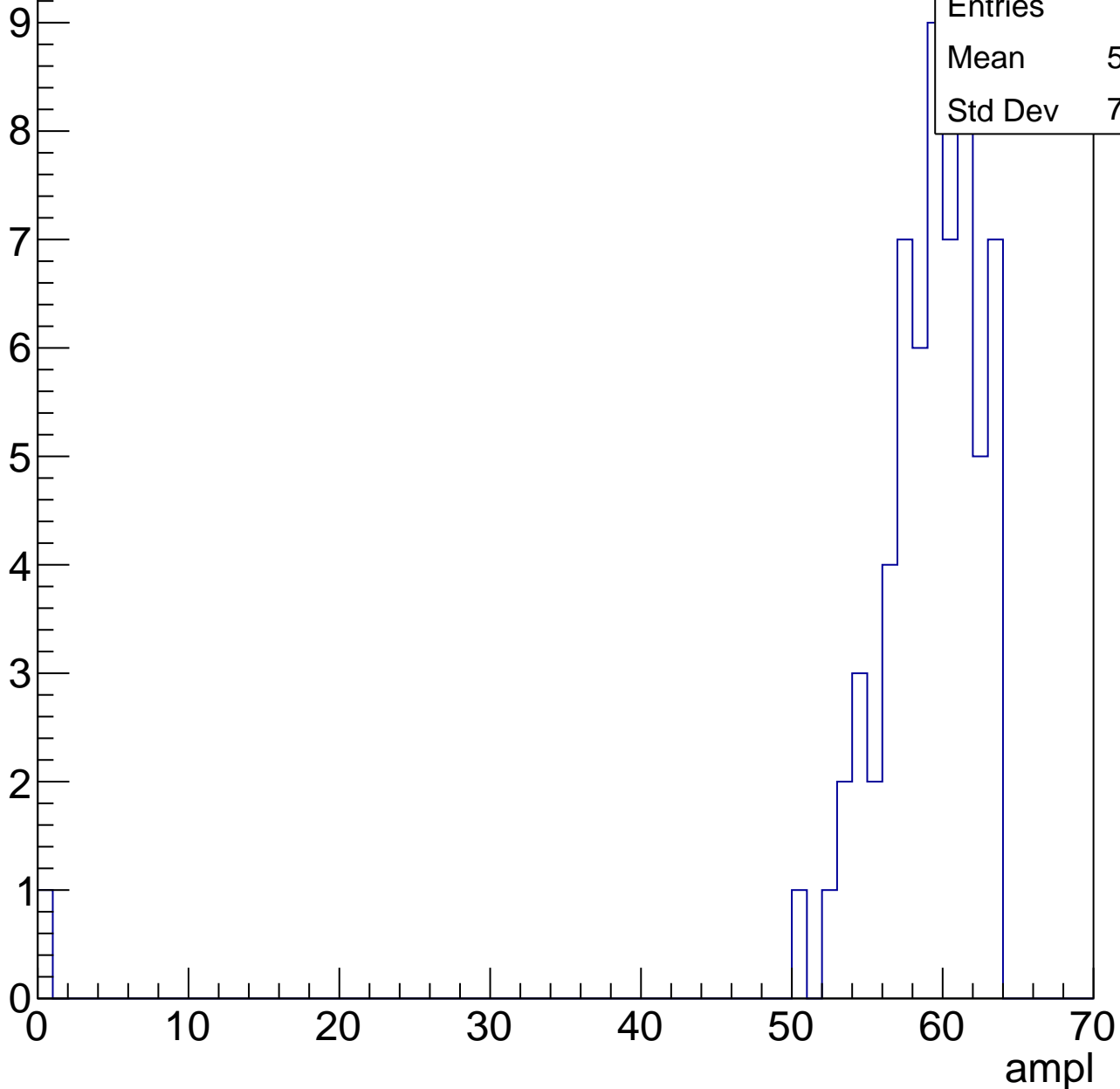
70

# B1L101S, U3-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	57.79
Std Dev	7.933

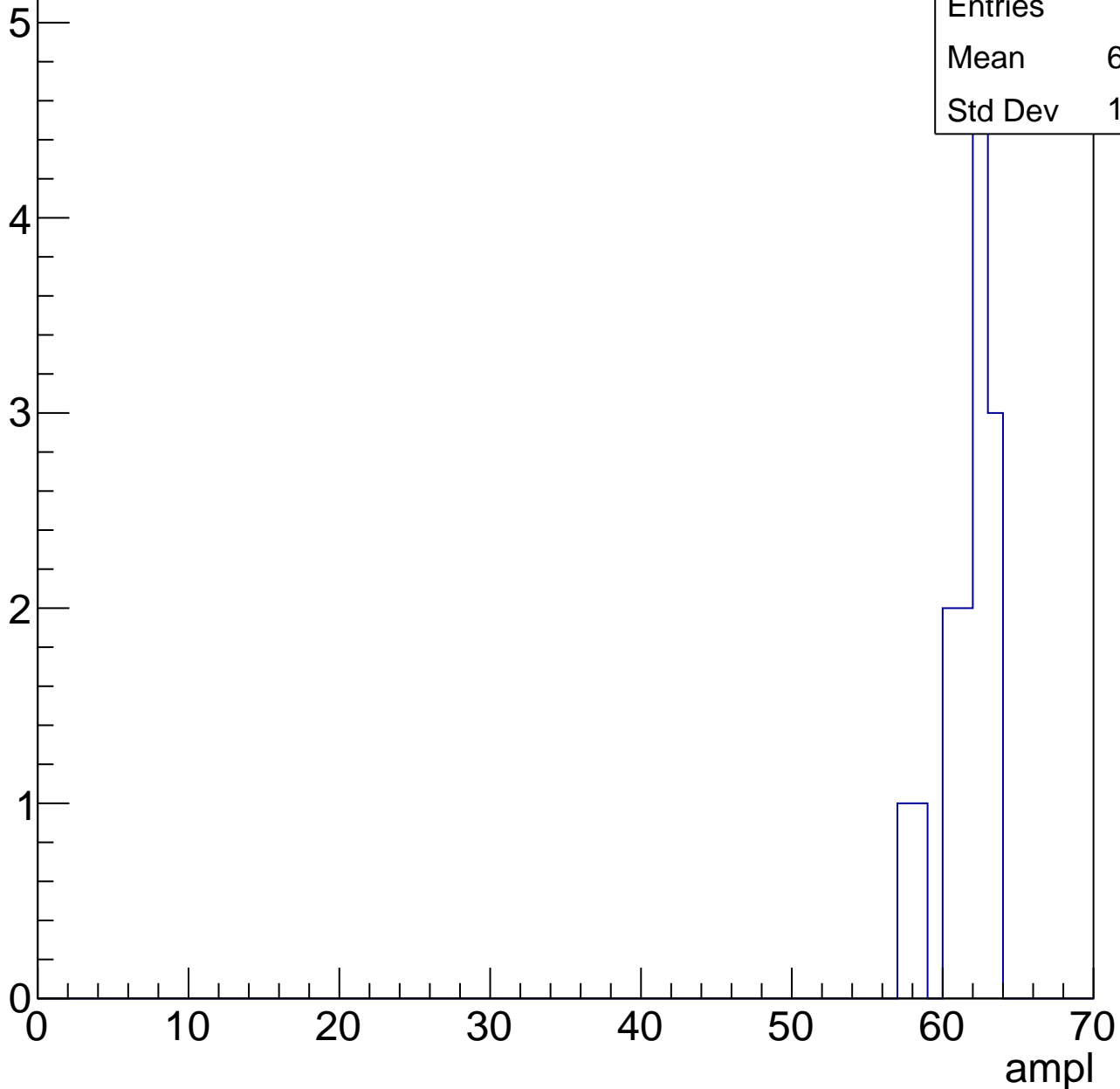


# B1L101S, U3-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	14
Mean	61.14
Std Dev	1.767





# B1L101S, U3-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch49, adc0

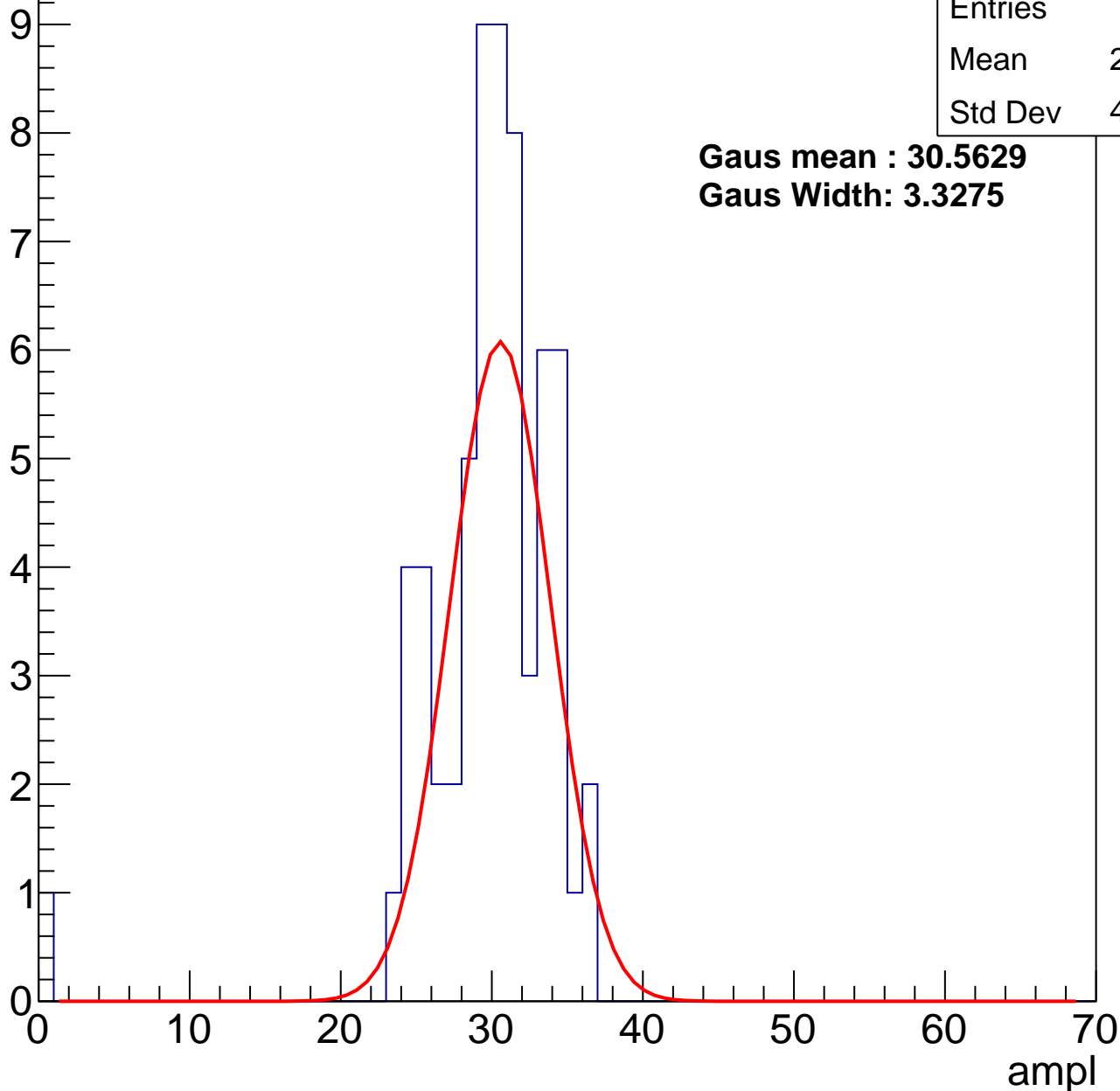
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	29.35
Std Dev	4.899

**Gaus mean : 30.5629**

**Gaus Width: 3.3275**



# B1L101S, U3-ch49, adc1

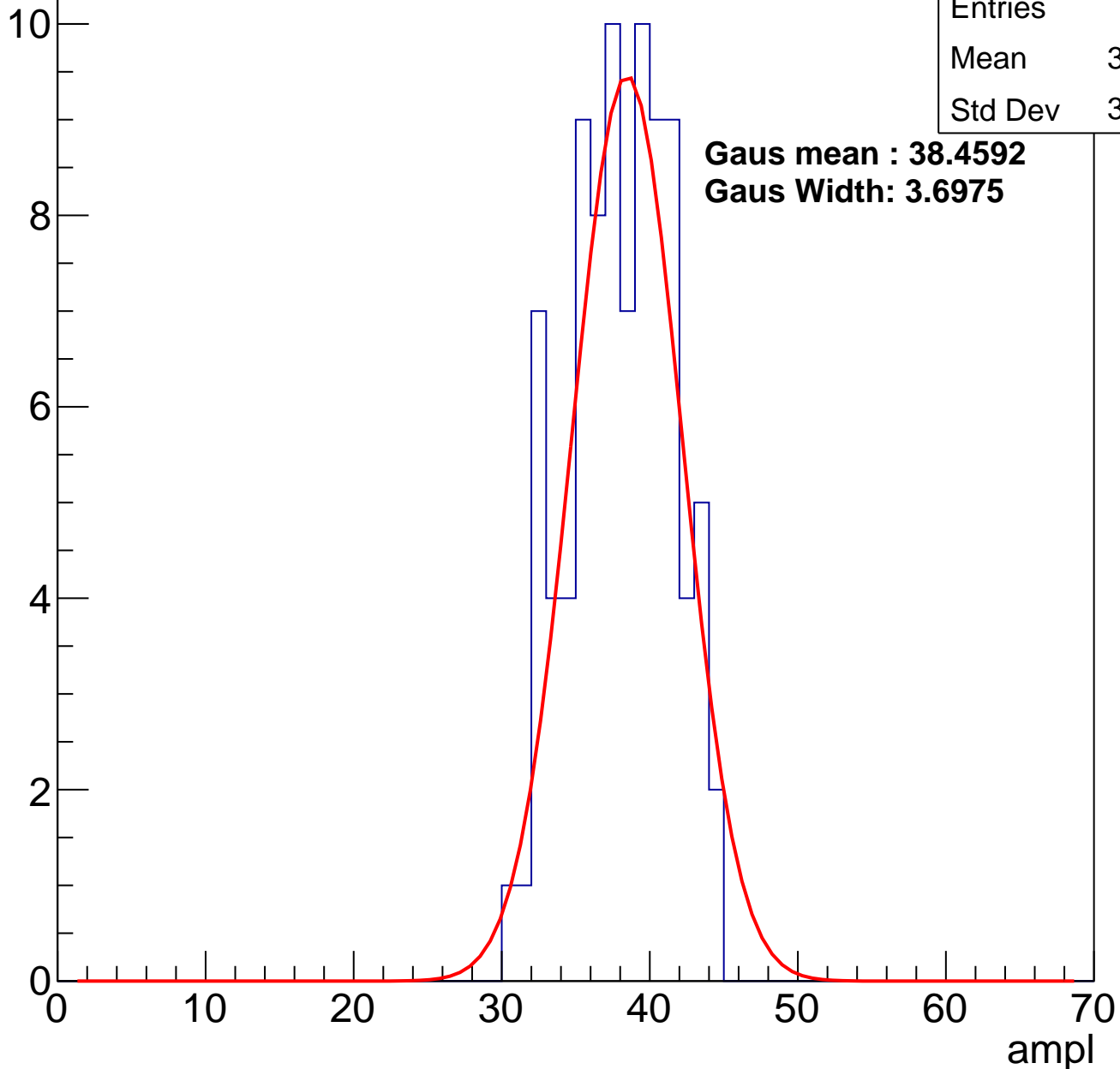
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	90
Mean	37.58
Std Dev	3.373

**Gaus mean : 38.4592**

**Gaus Width: 3.6975**

Entry



# B1L101S, U3-ch49, adc2

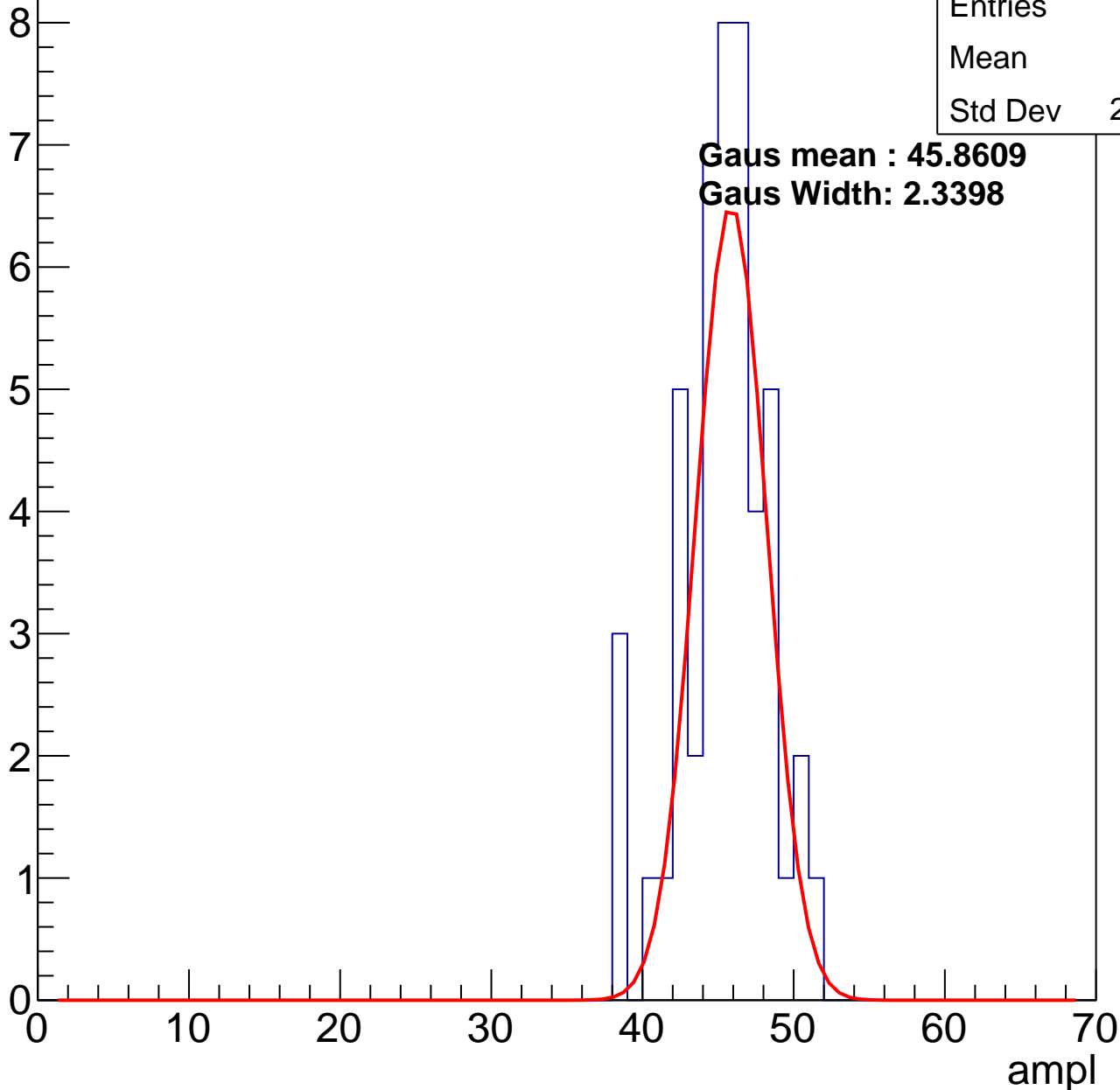
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	44.9
Std Dev	2.953

**Gaus mean : 45.8609**

**Gaus Width: 2.3398**

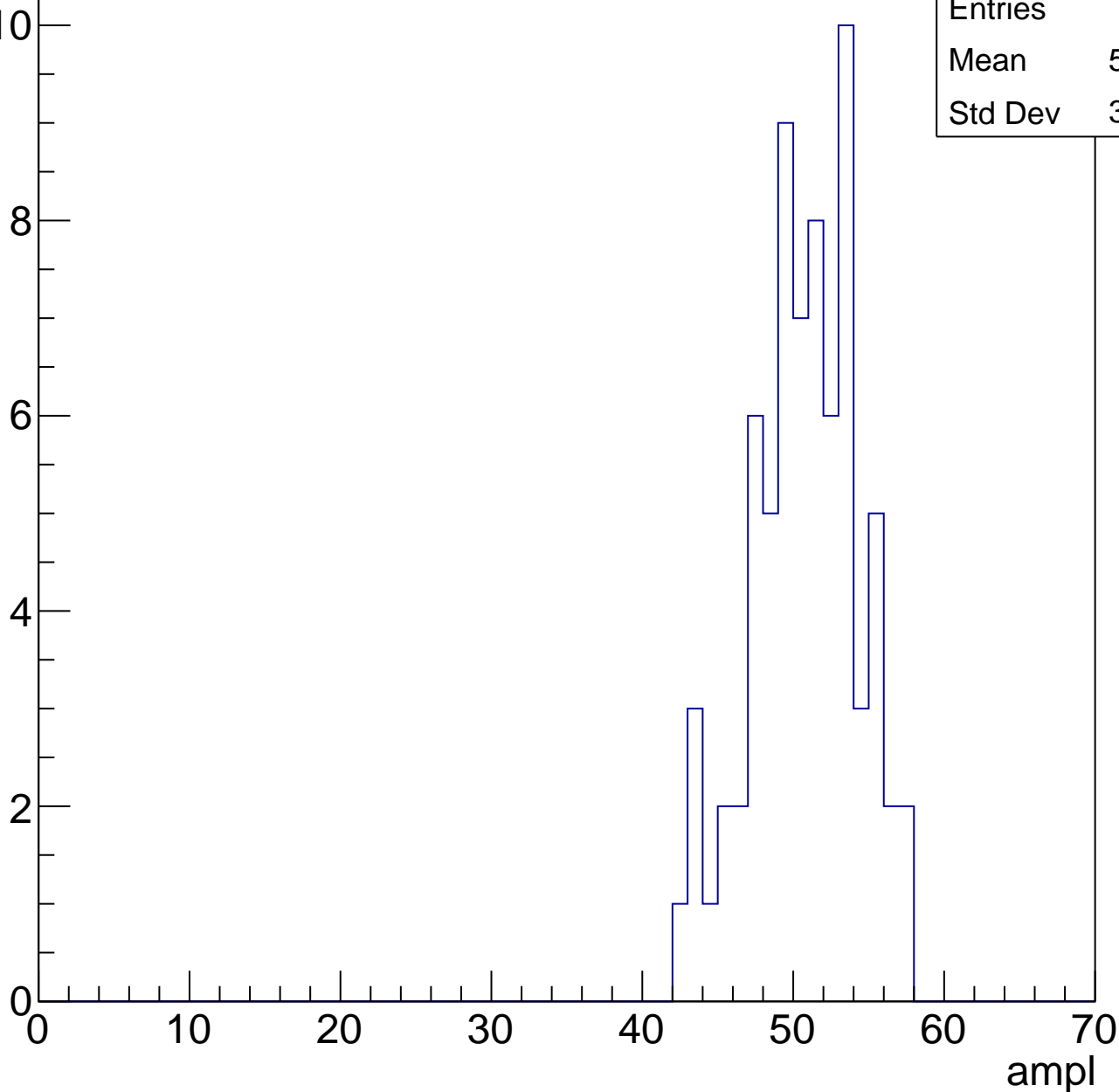


# B1L101S, U3-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	50.32
Std Dev	3.475

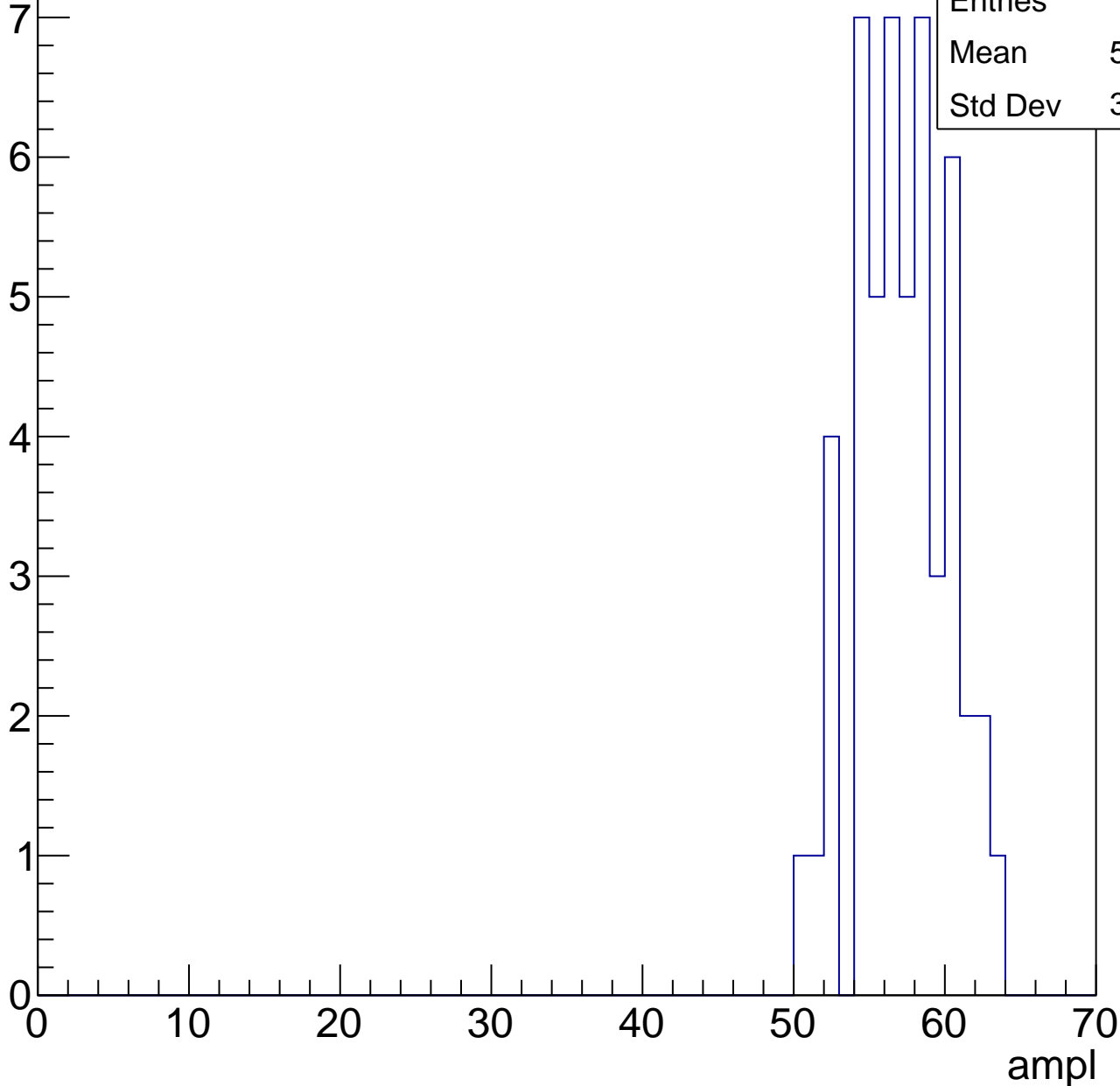


# B1L101S, U3-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	56.69
Std Dev	3.006

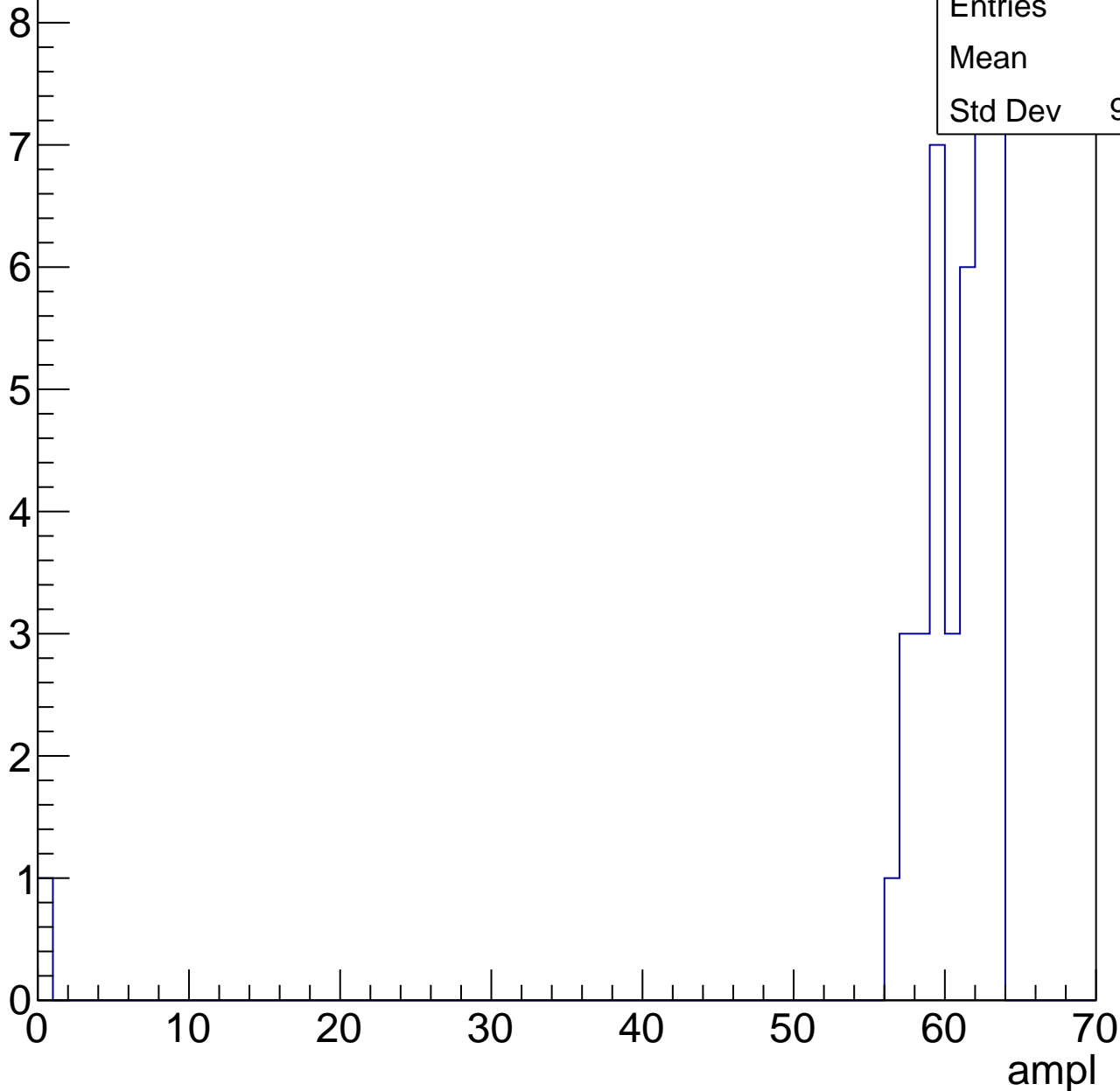


# B1L101S, U3-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

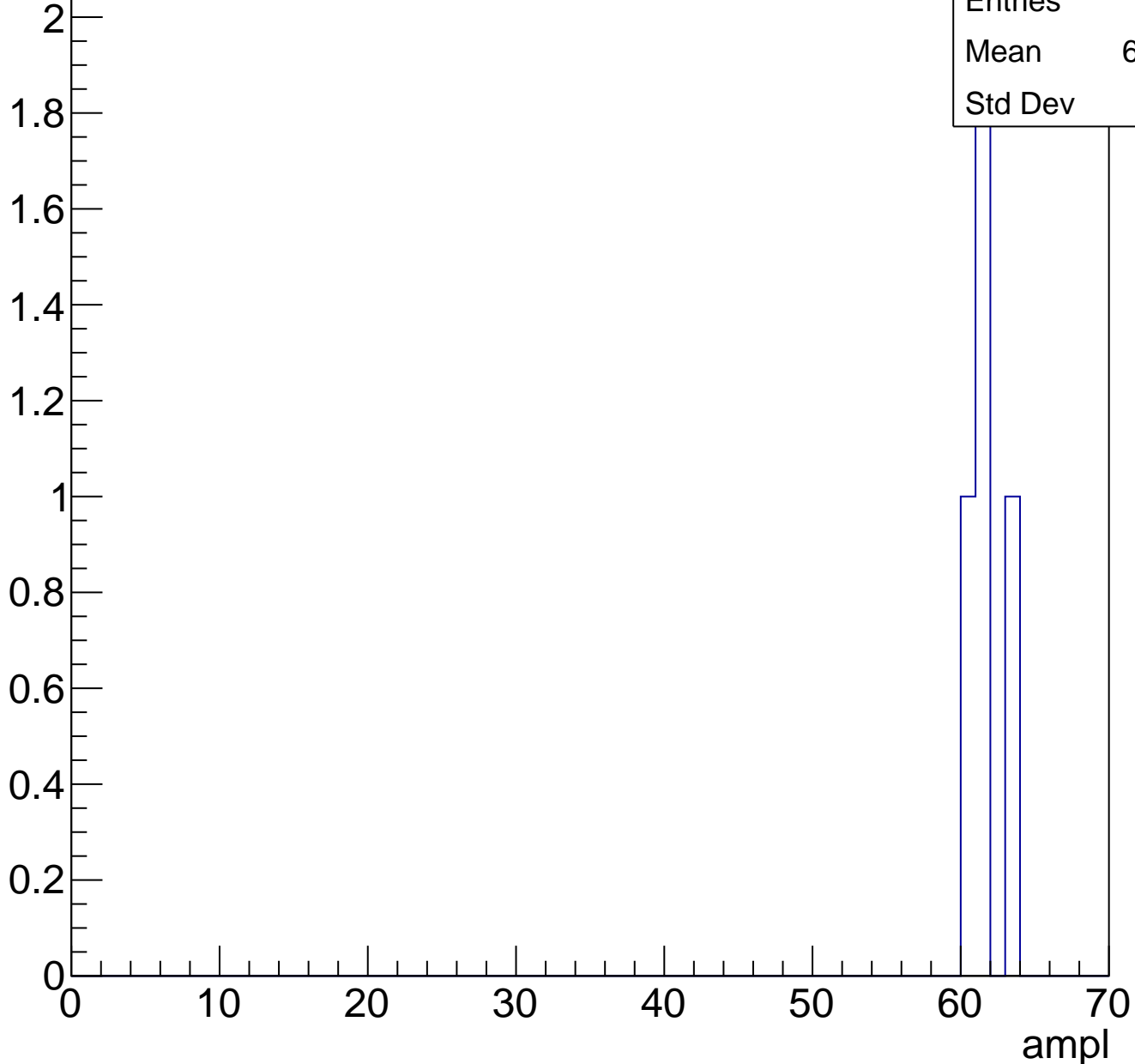
Entries	40
Mean	59
Std Dev	9.659



# B1L101S, U3-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch49, adc7

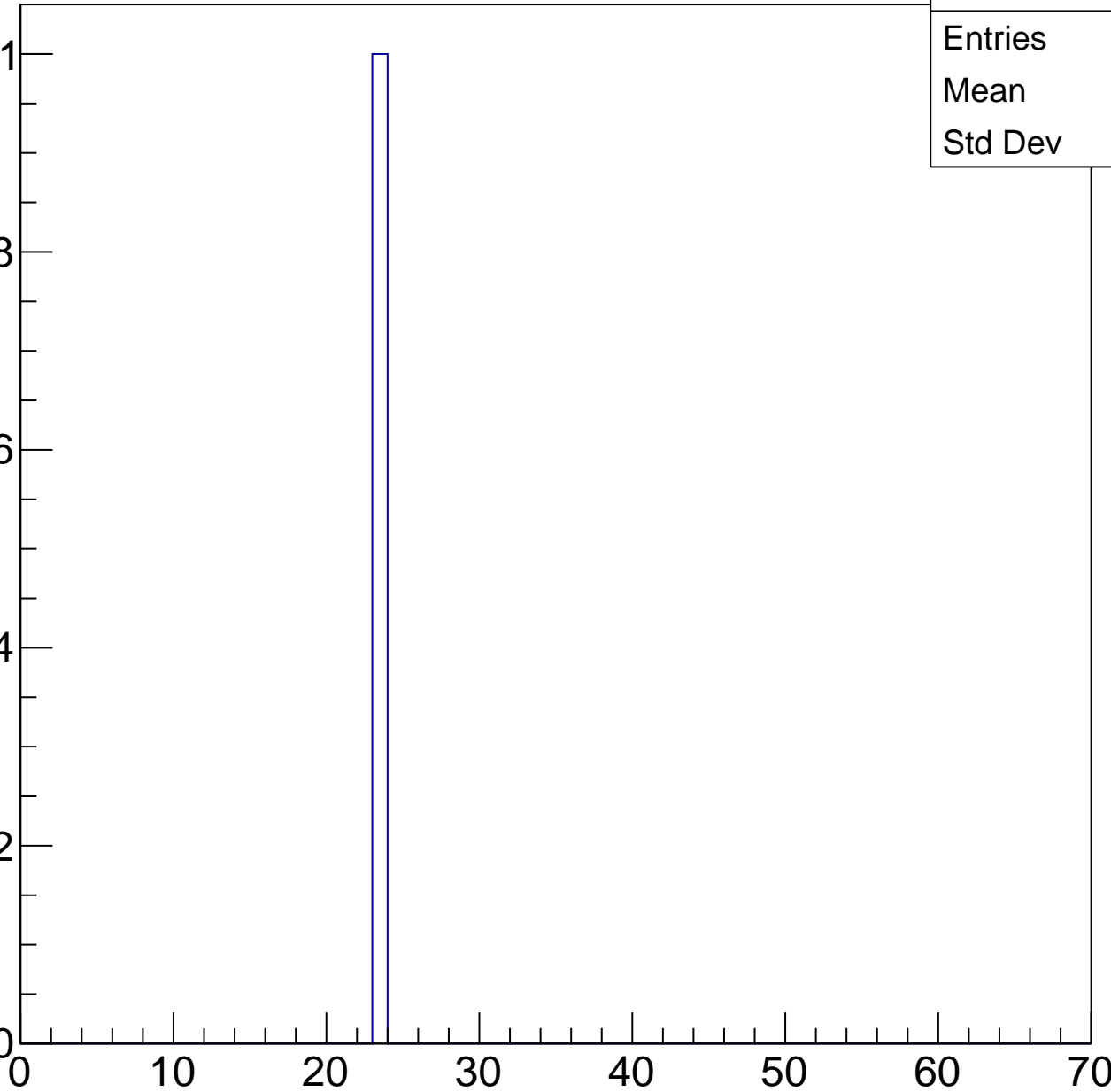
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	23
Std Dev	0

ampl



# B1L101S, U3-ch50, adc0

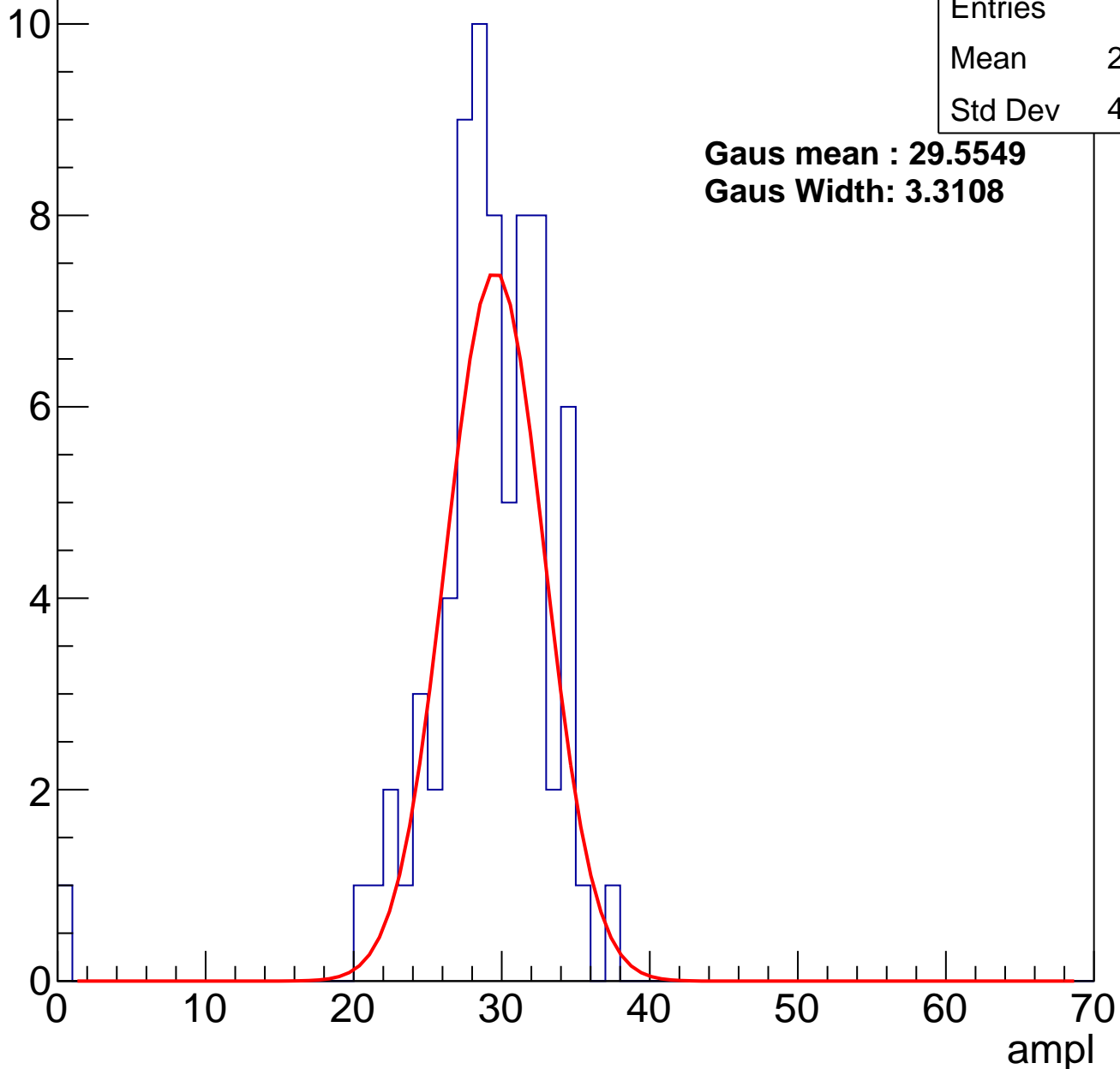
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	73
Mean	28.56
Std Dev	4.806

**Gaus mean : 29.5549**

**Gaus Width: 3.3108**

Entry



# B1L101S, U3-ch50, adc1

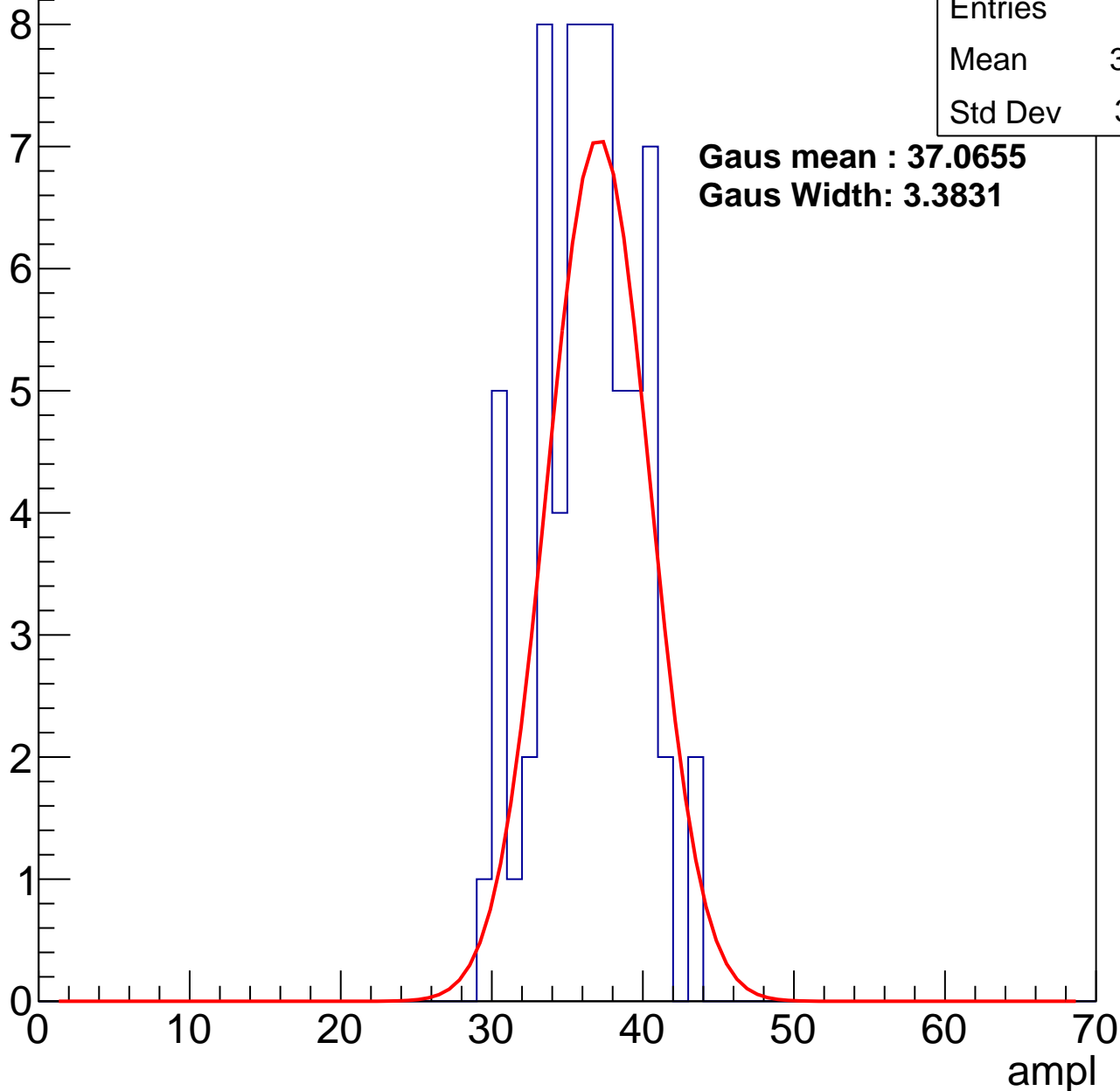
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	35.92
Std Dev	3.291

**Gaus mean : 37.0655**

**Gaus Width: 3.3831**



# B1L101S, U3-ch50, adc2

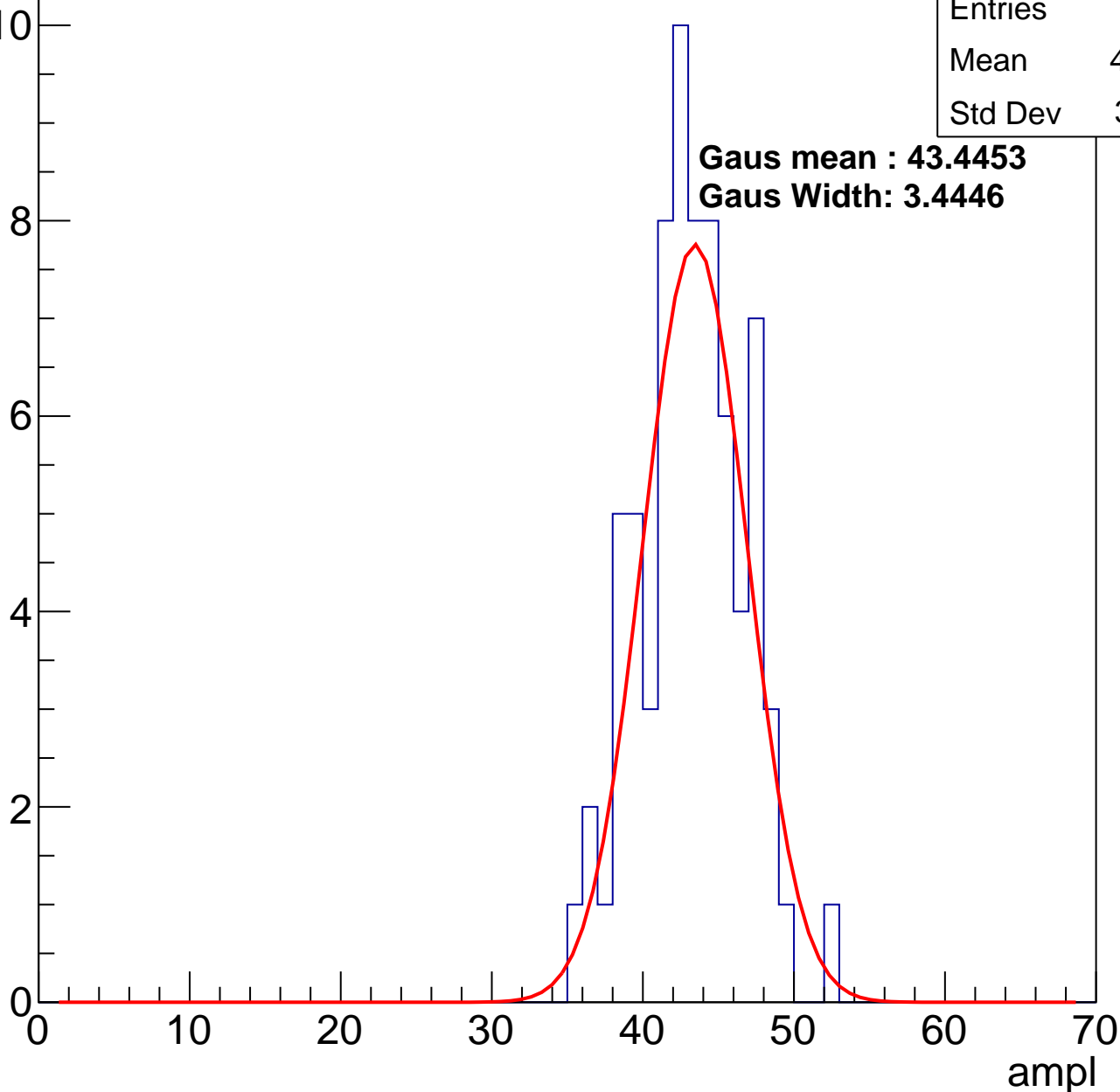
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	42.75
Std Dev	3.391

**Gaus mean : 43.4453**

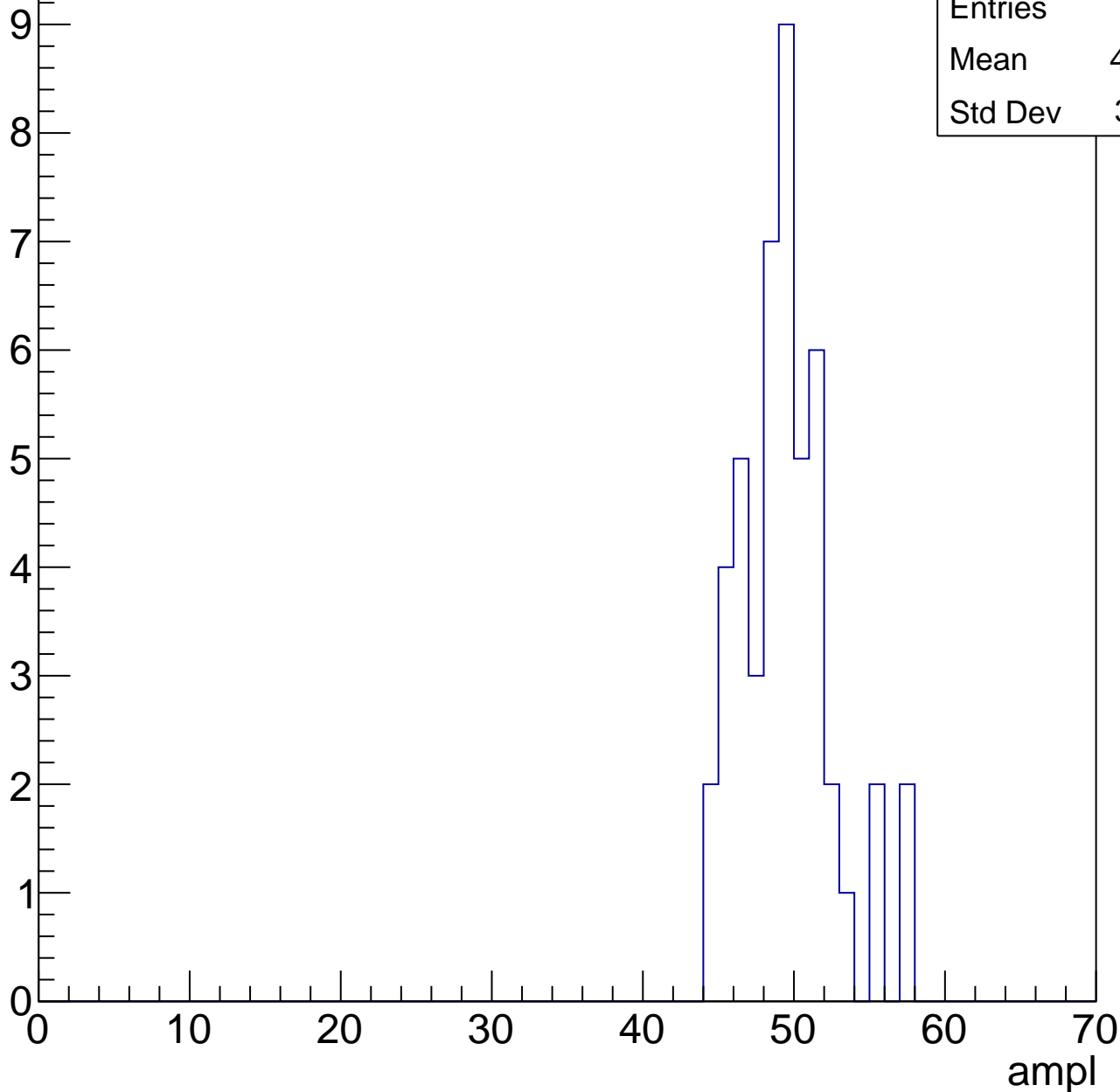
**Gaus Width: 3.4446**



# B1L101S, U3-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

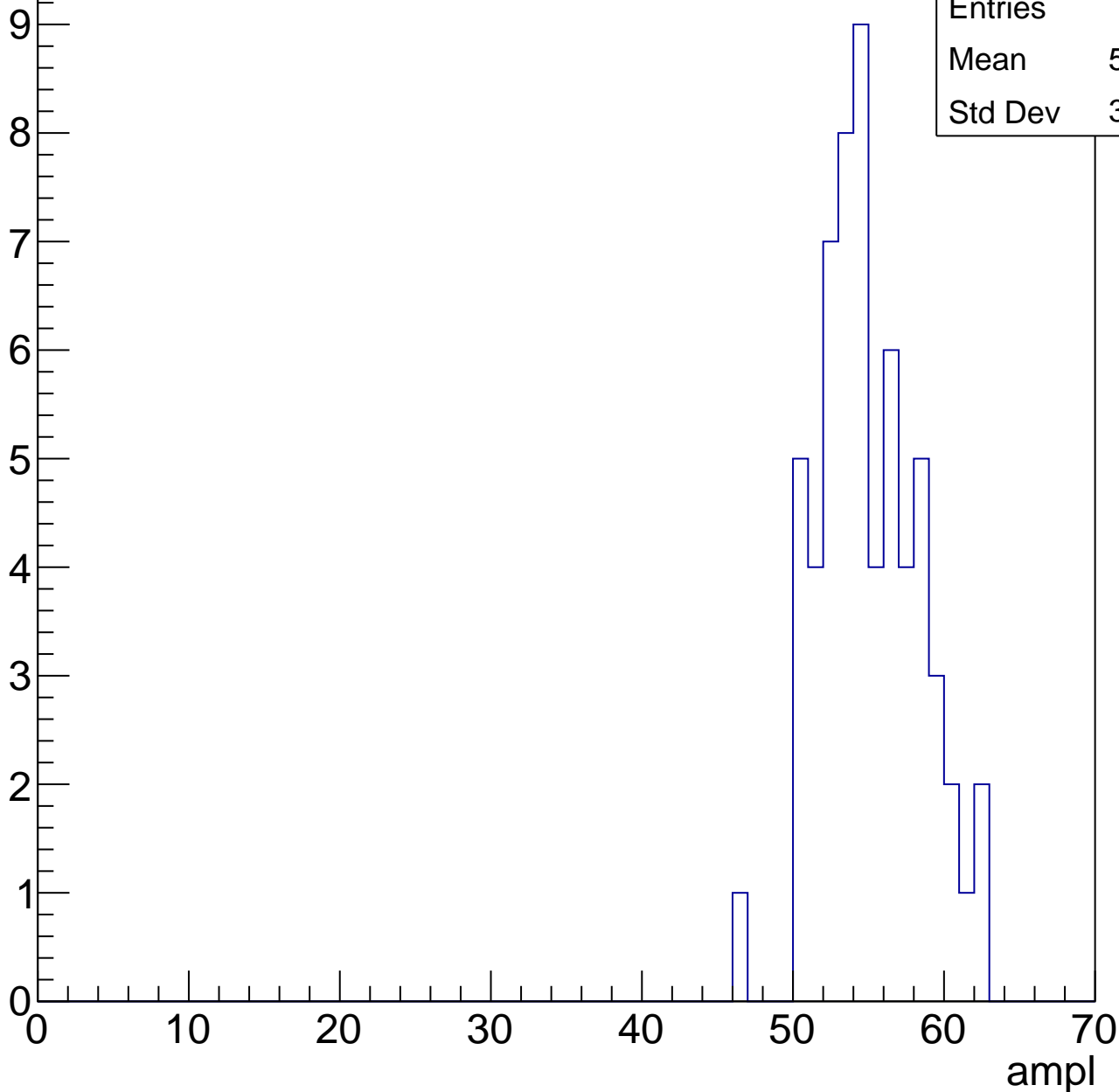


# B1L101S, U3-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	54.59
Std Dev	3.296



# B1L101S, U3-ch50, adc5

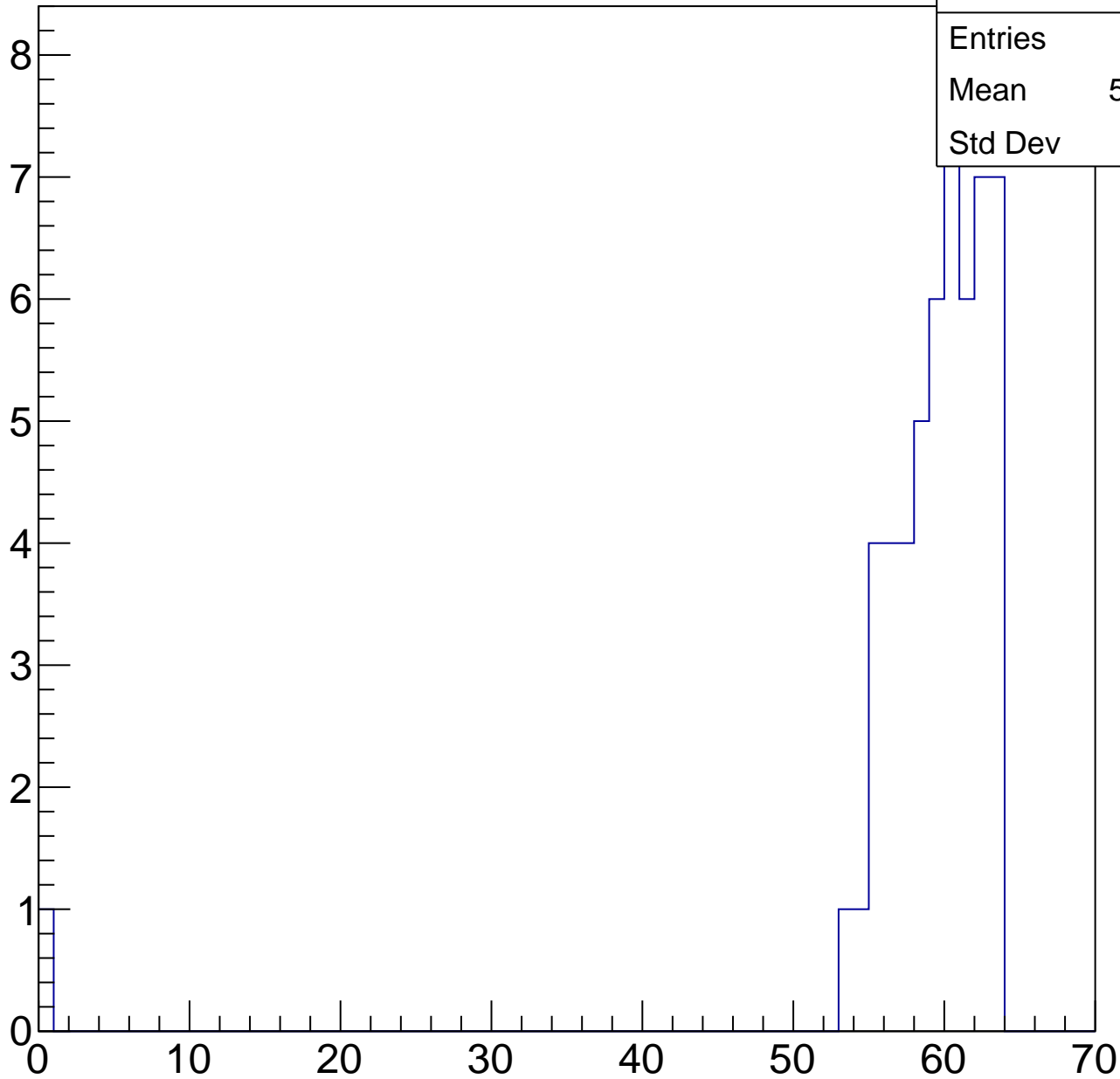
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	54
Mean	58.22
Std Dev	8.43

ampl



# B1L101S, U3-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	7
Mean	61.57
Std Dev	1.4

ampl

0 10 20 30 40 50 60 70



# B1L101S, U3-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch51, adc0

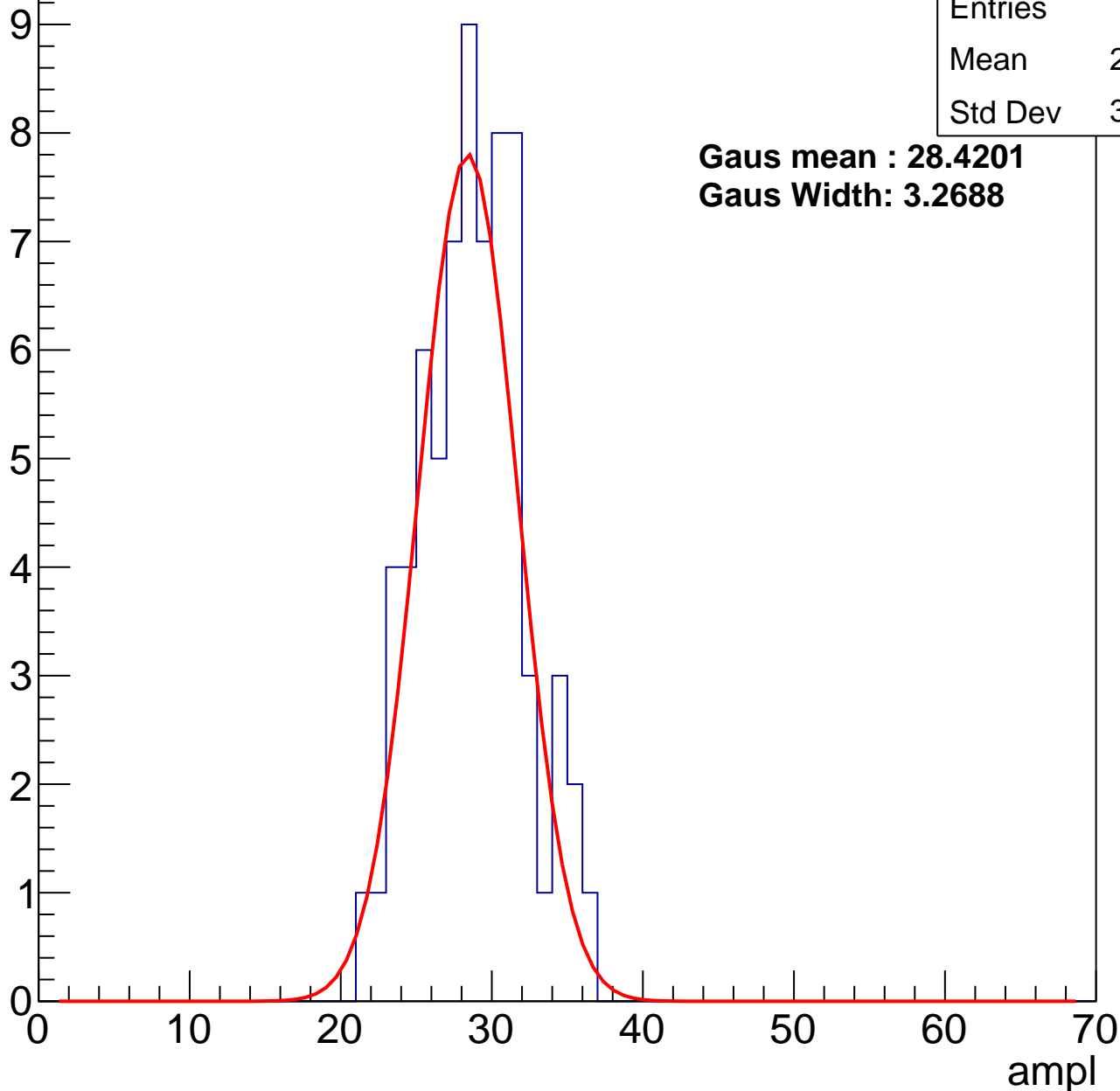
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	28.29
Std Dev	3.334

**Gaus mean : 28.4201**

**Gaus Width: 3.2688**



# B1L101S, U3-ch51, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

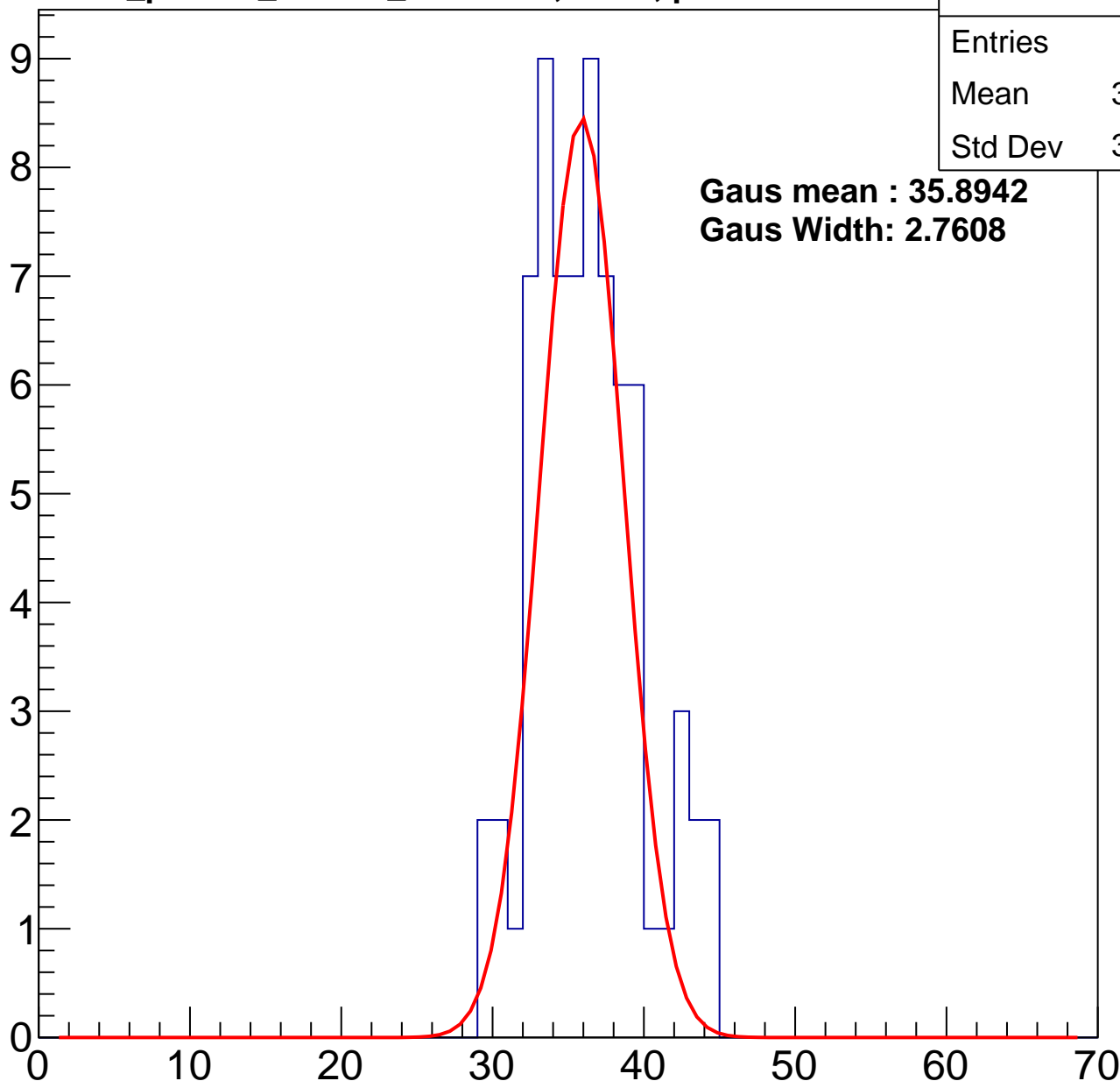
9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	72
Mean	35.82
Std Dev	3.497

**Gaus mean : 35.8942**

**Gaus Width: 2.7608**

ampl



# B1L101S, U3-ch51, adc2

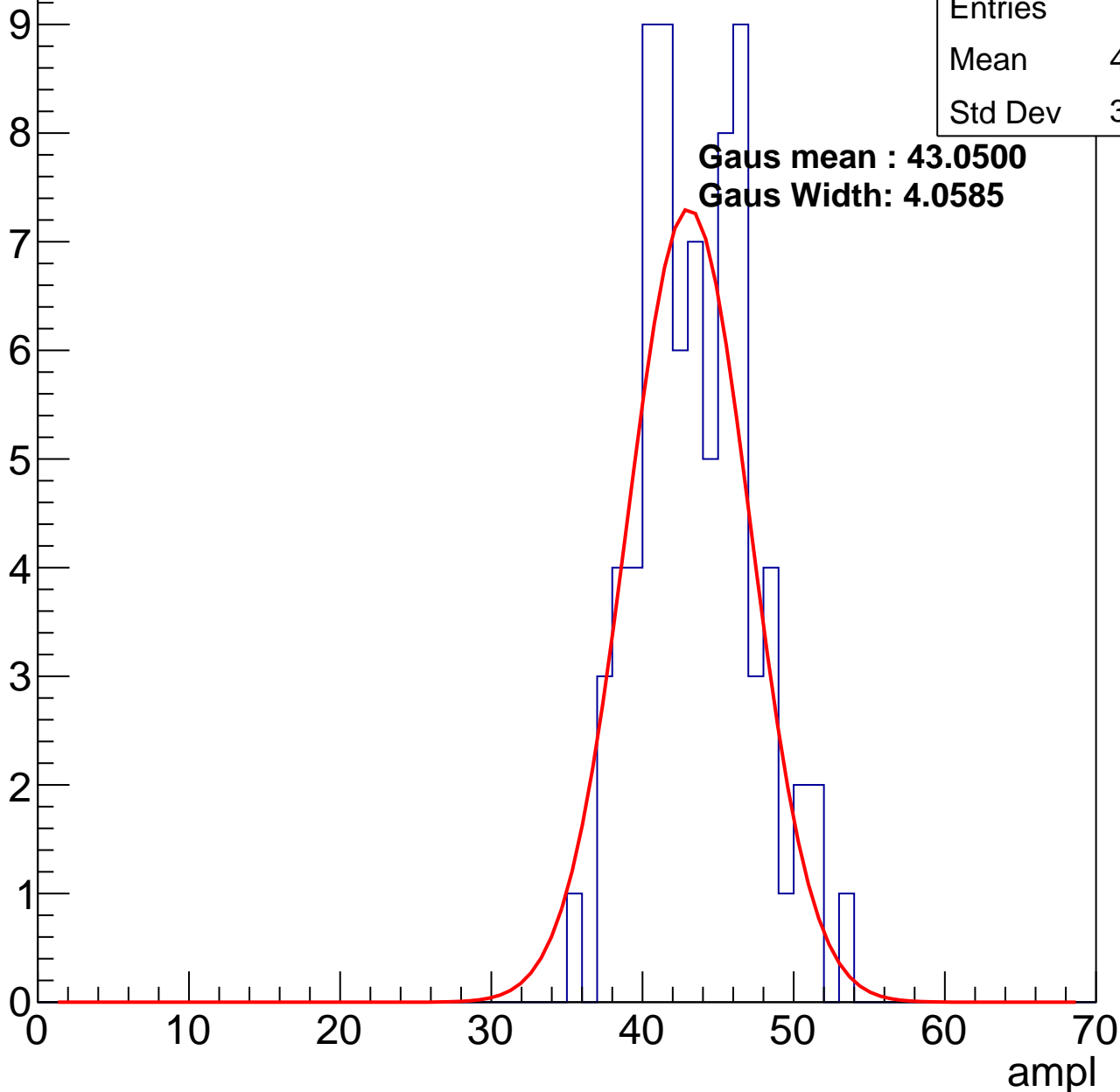
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	43.17
Std Dev	3.729

**Gaus mean : 43.0500**

**Gaus Width: 4.0585**

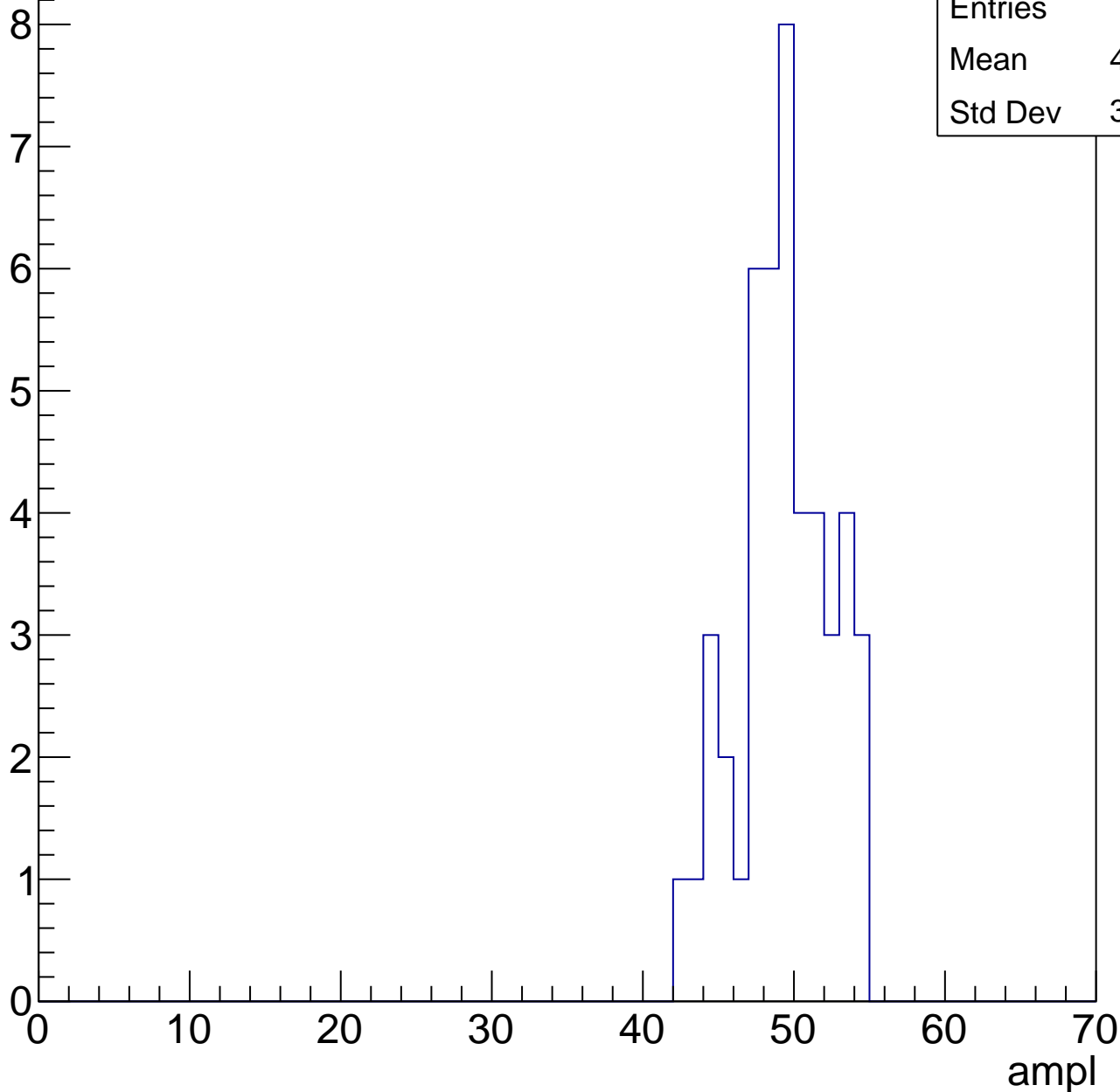


# B1L101S, U3-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

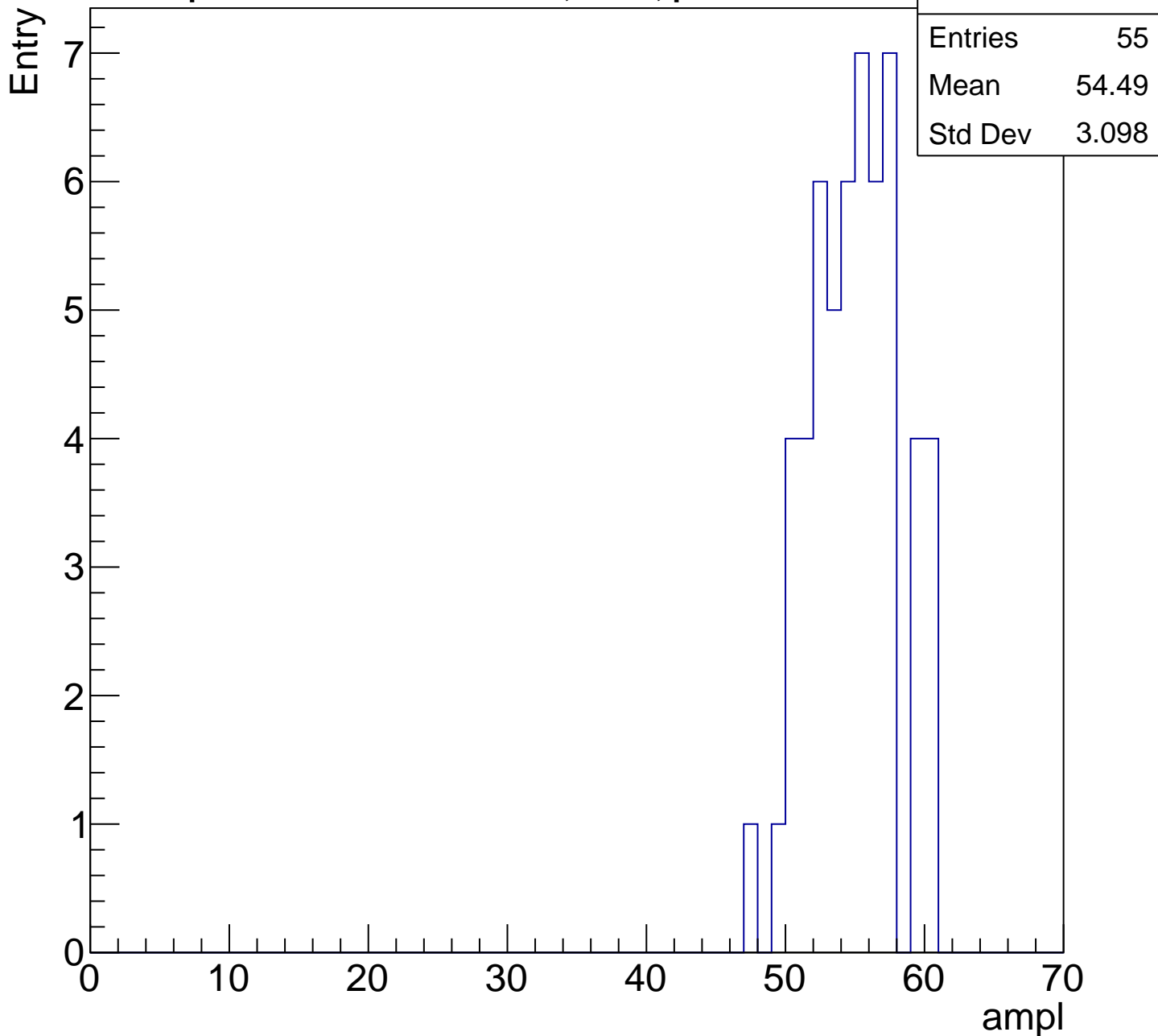
Entry

Entries	46
Mean	48.89
Std Dev	3.009



# B1L101S, U3-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

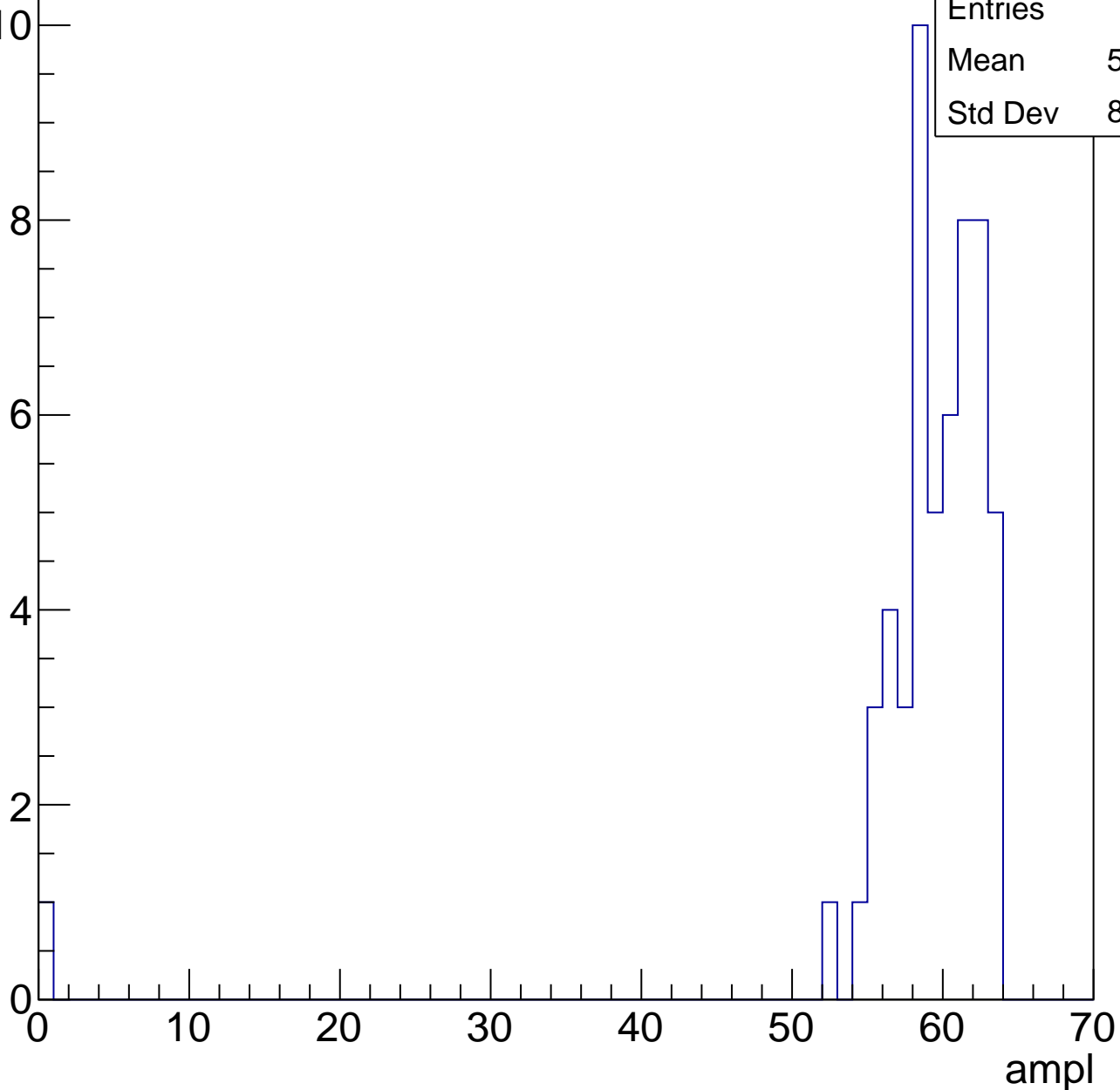


# B1L101S, U3-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	58.18
Std Dev	8.328

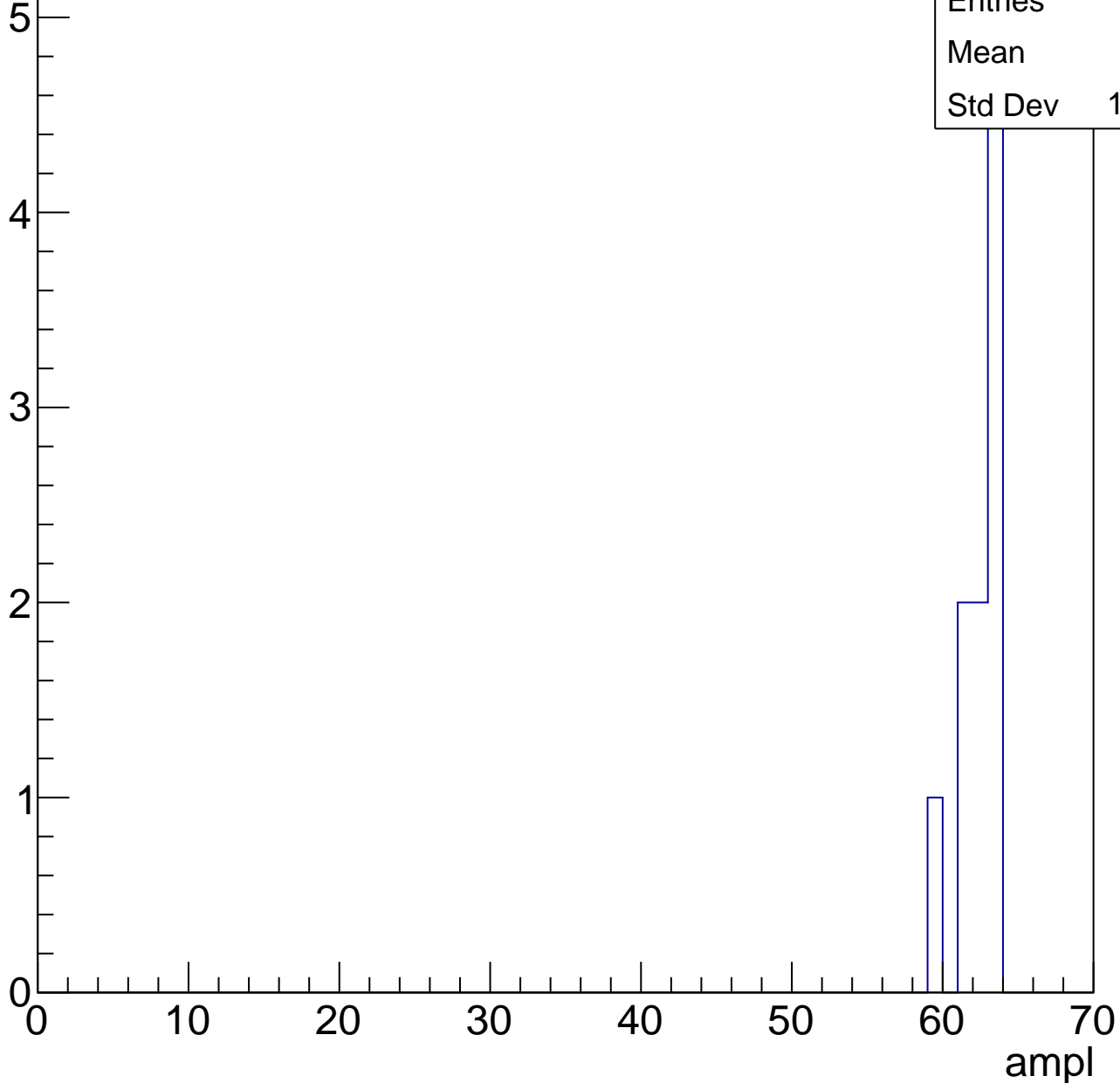


# B1L101S, U3-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	10
Mean	62
Std Dev	1.265





# B1L101S, U3-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U3-ch52, adc0

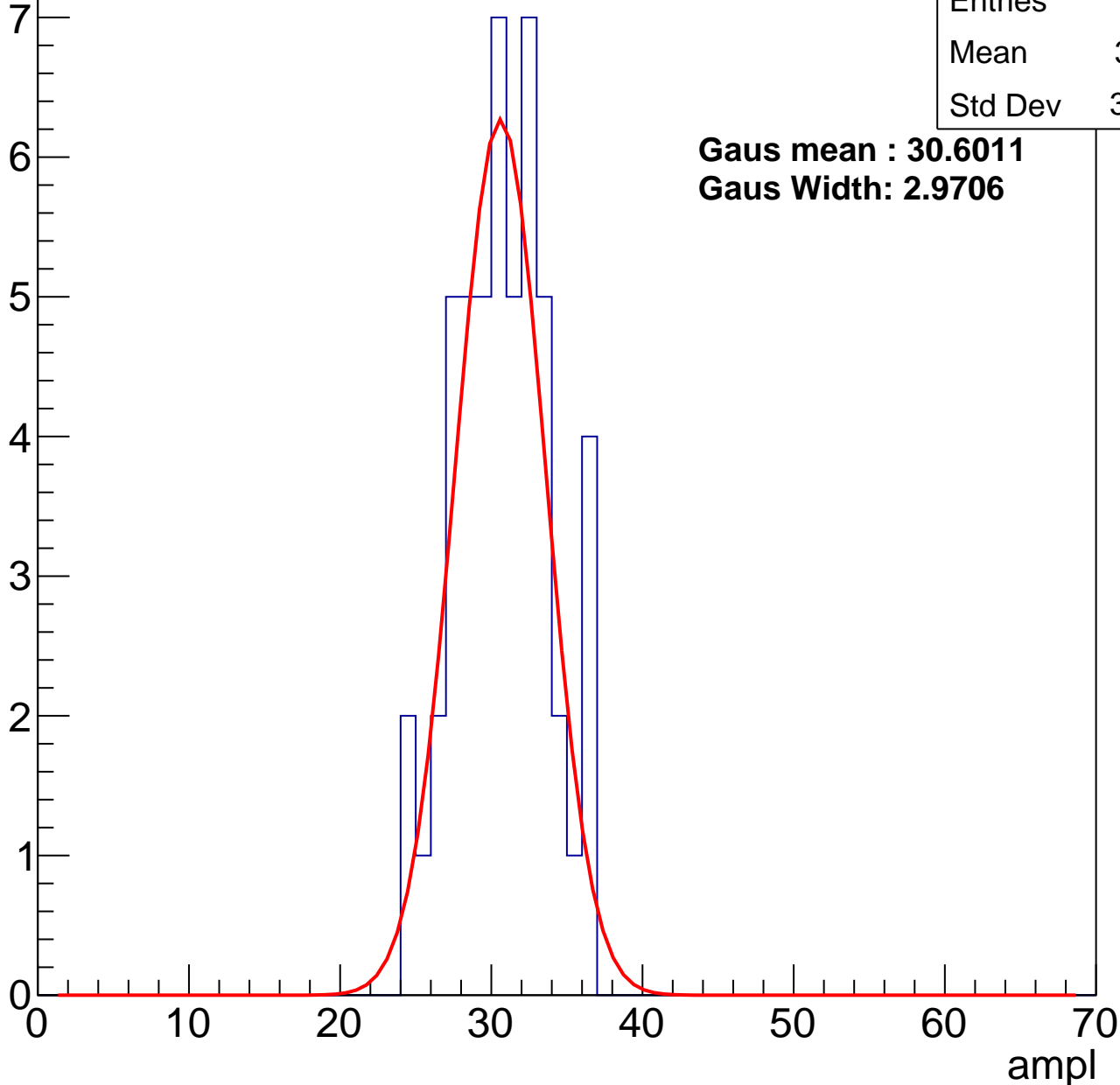
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	30.31
Std Dev	3.045

**Gaus mean : 30.6011**

**Gaus Width: 2.9706**



# B1L101S, U3-ch52, adc1

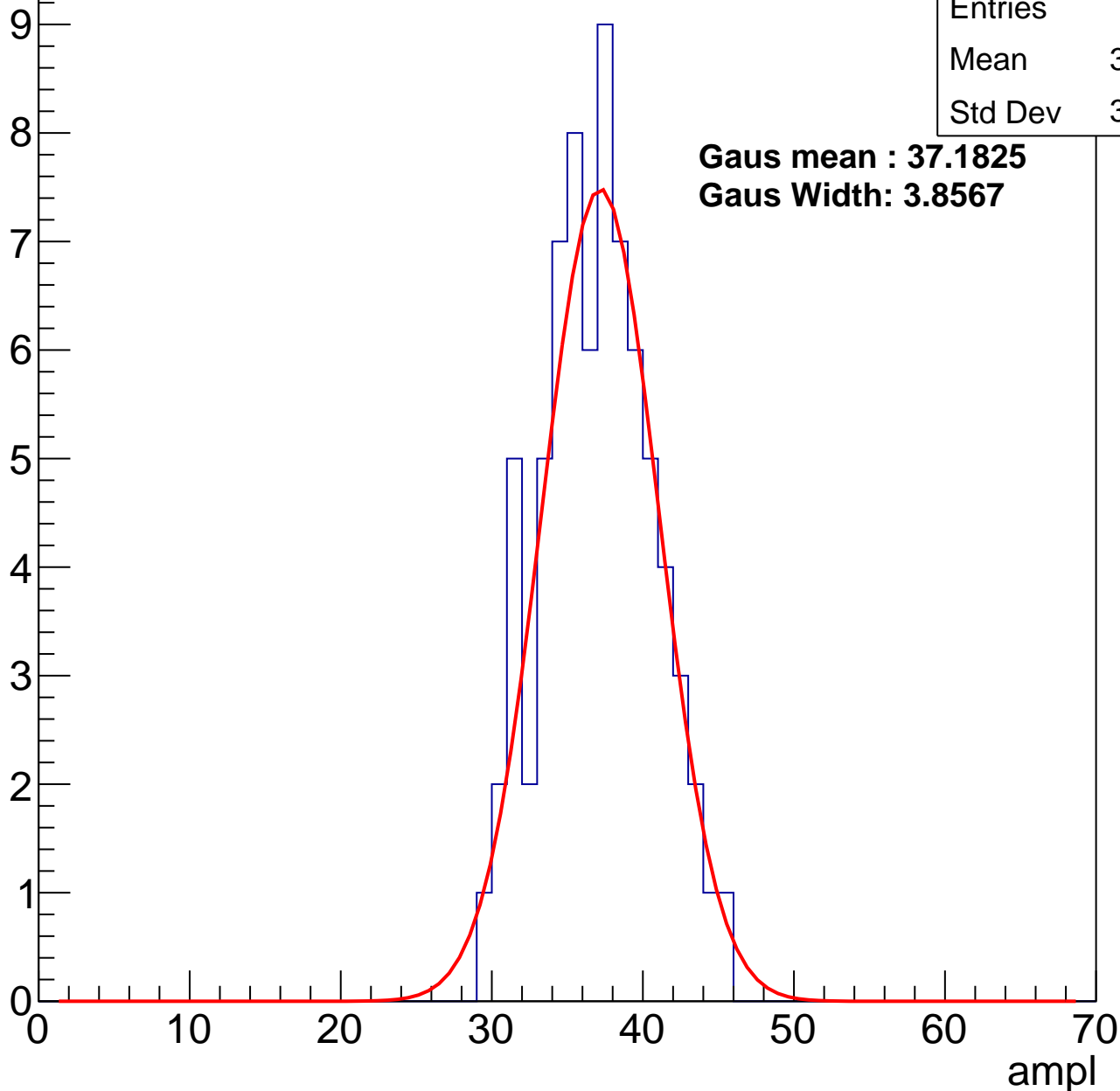
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	36.55
Std Dev	3.599

**Gaus mean : 37.1825**

**Gaus Width: 3.8567**



# B1L101S, U3-ch52, adc2

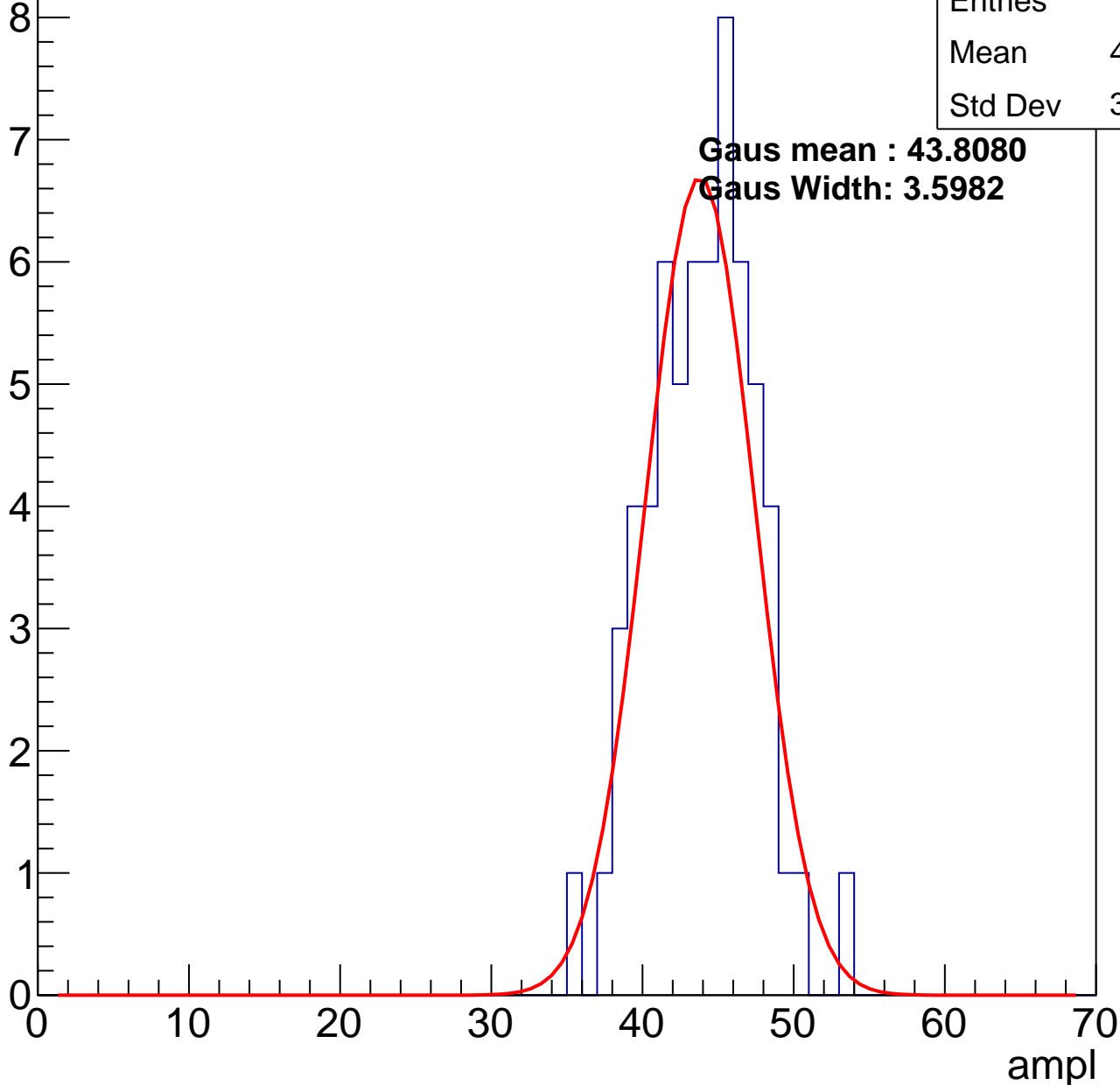
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	43.47
Std Dev	3.472

**Gaus mean : 43.8080**

**Gaus Width: 3.5982**

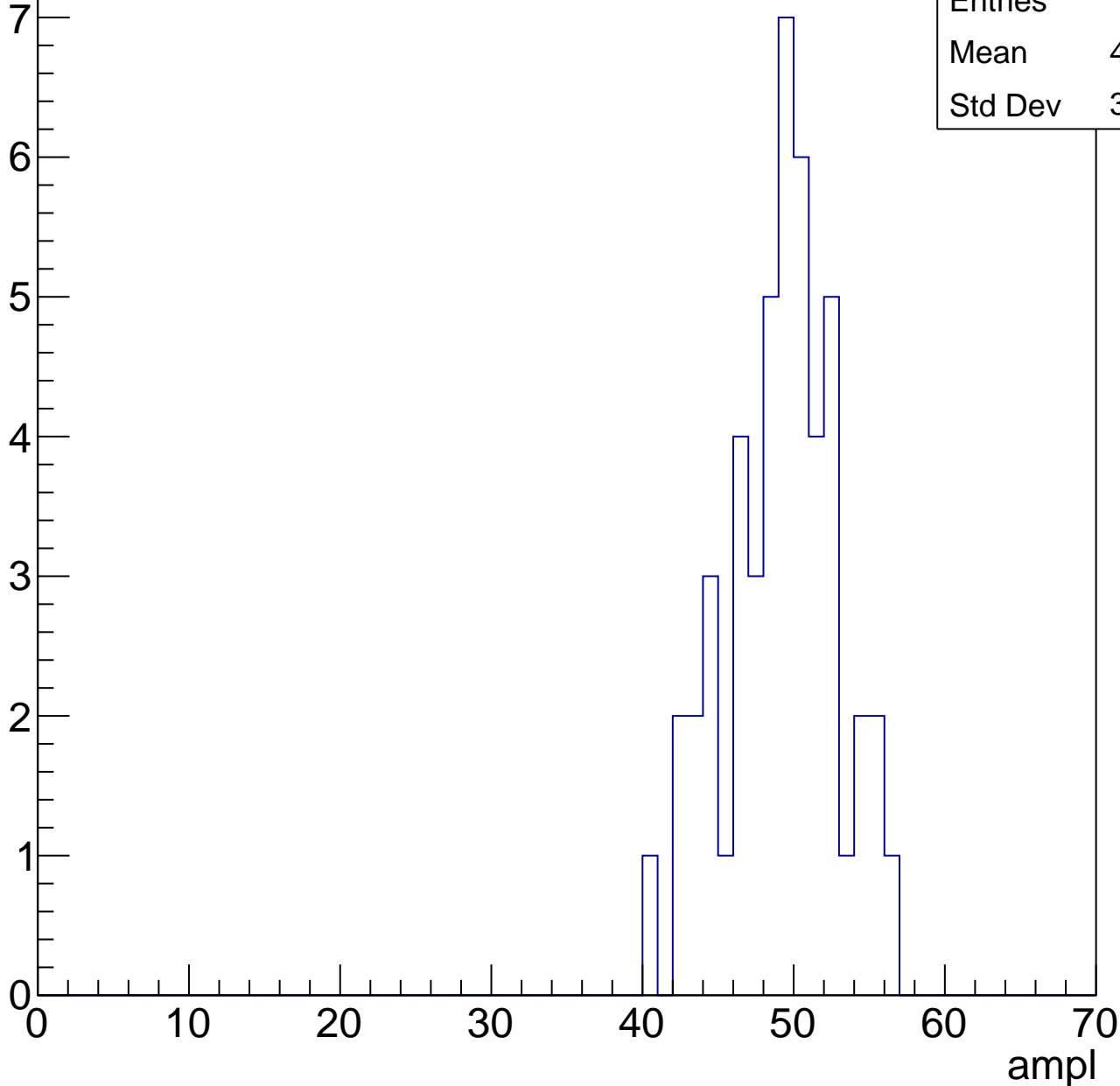


# B1L101S, U3-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	48.69
Std Dev	3.626

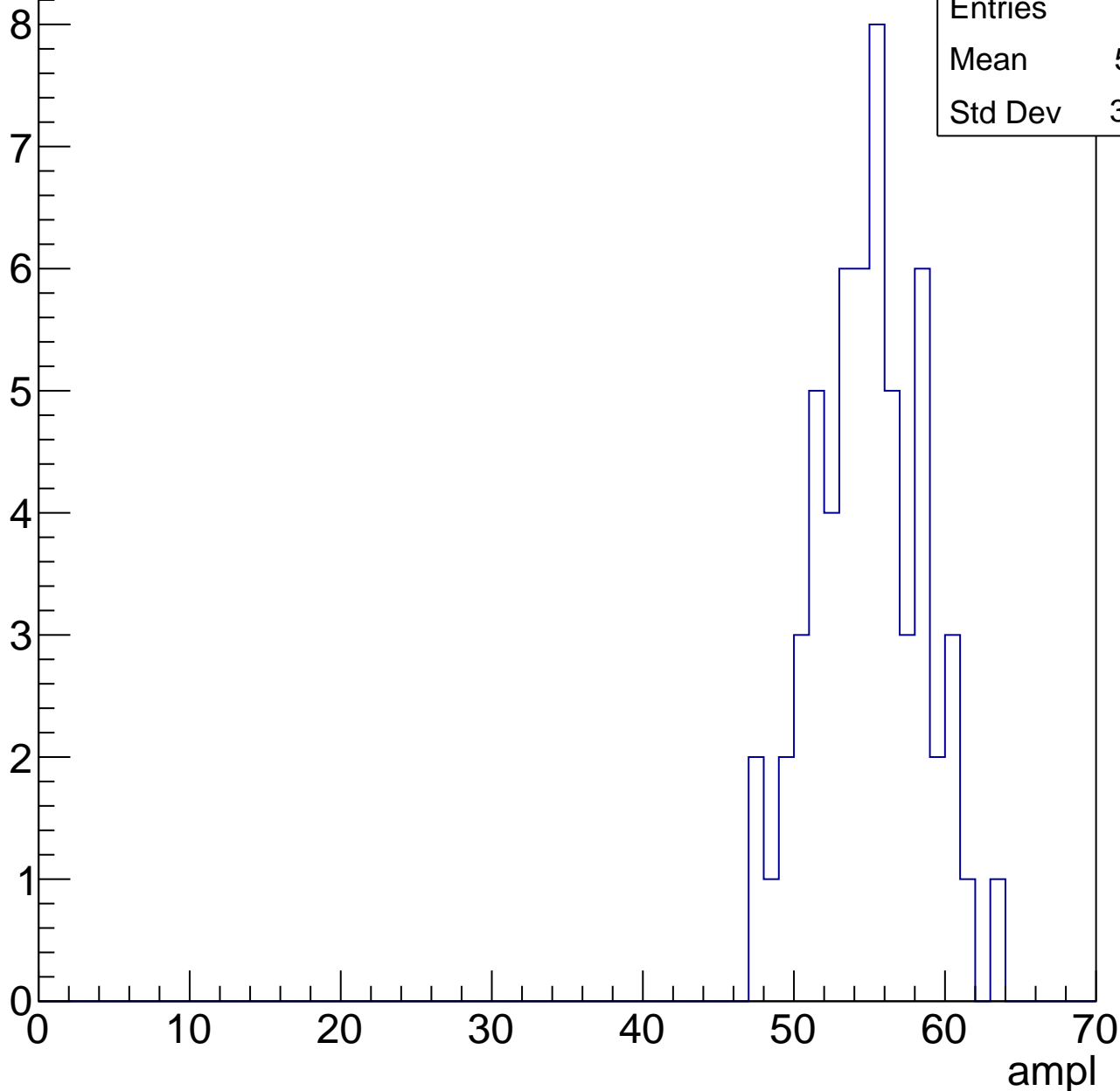


# B1L101S, U3-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

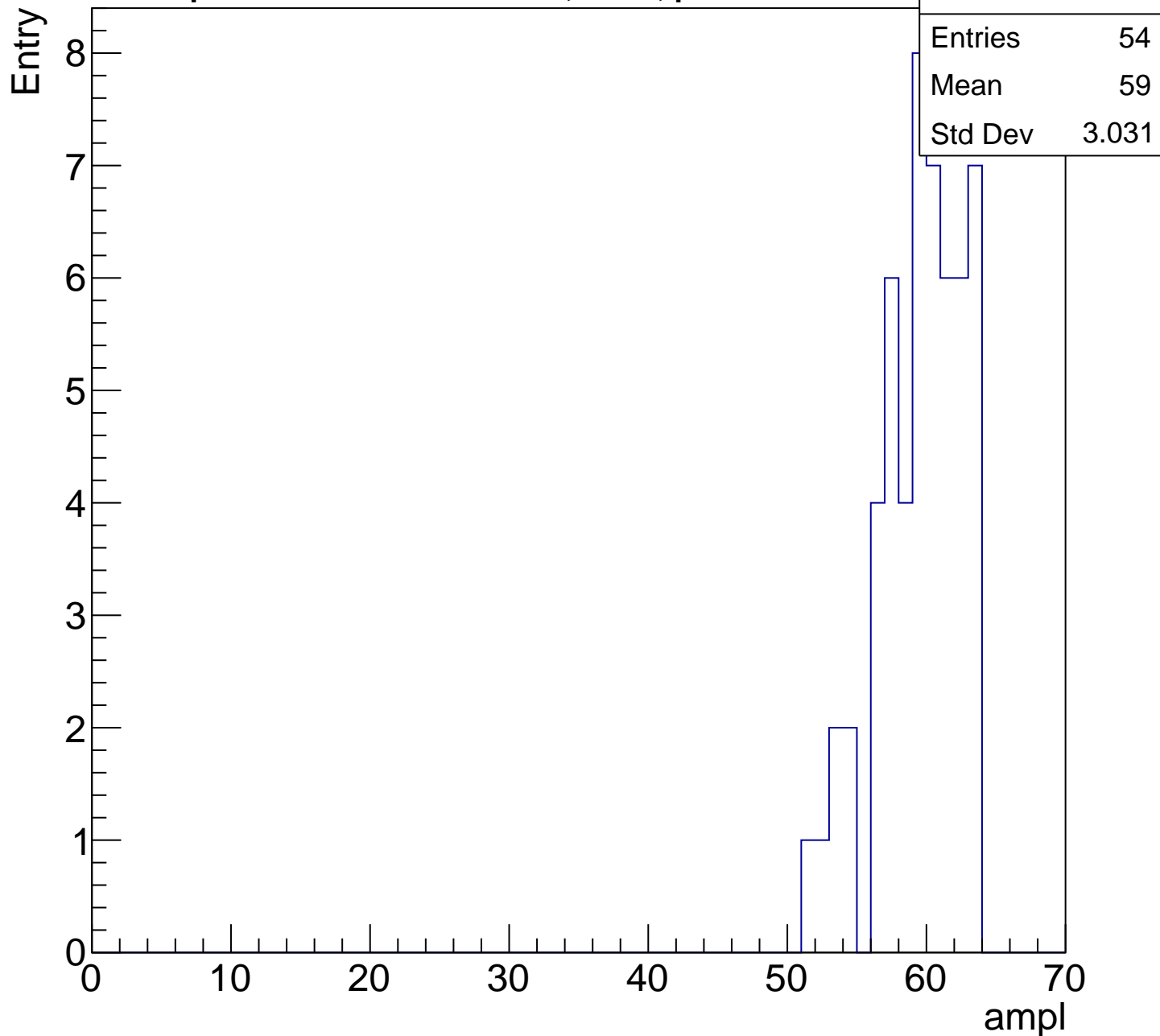
Entry

Entries	58
Mean	54.41
Std Dev	3.543



# B1L101S, U3-ch52, adc5

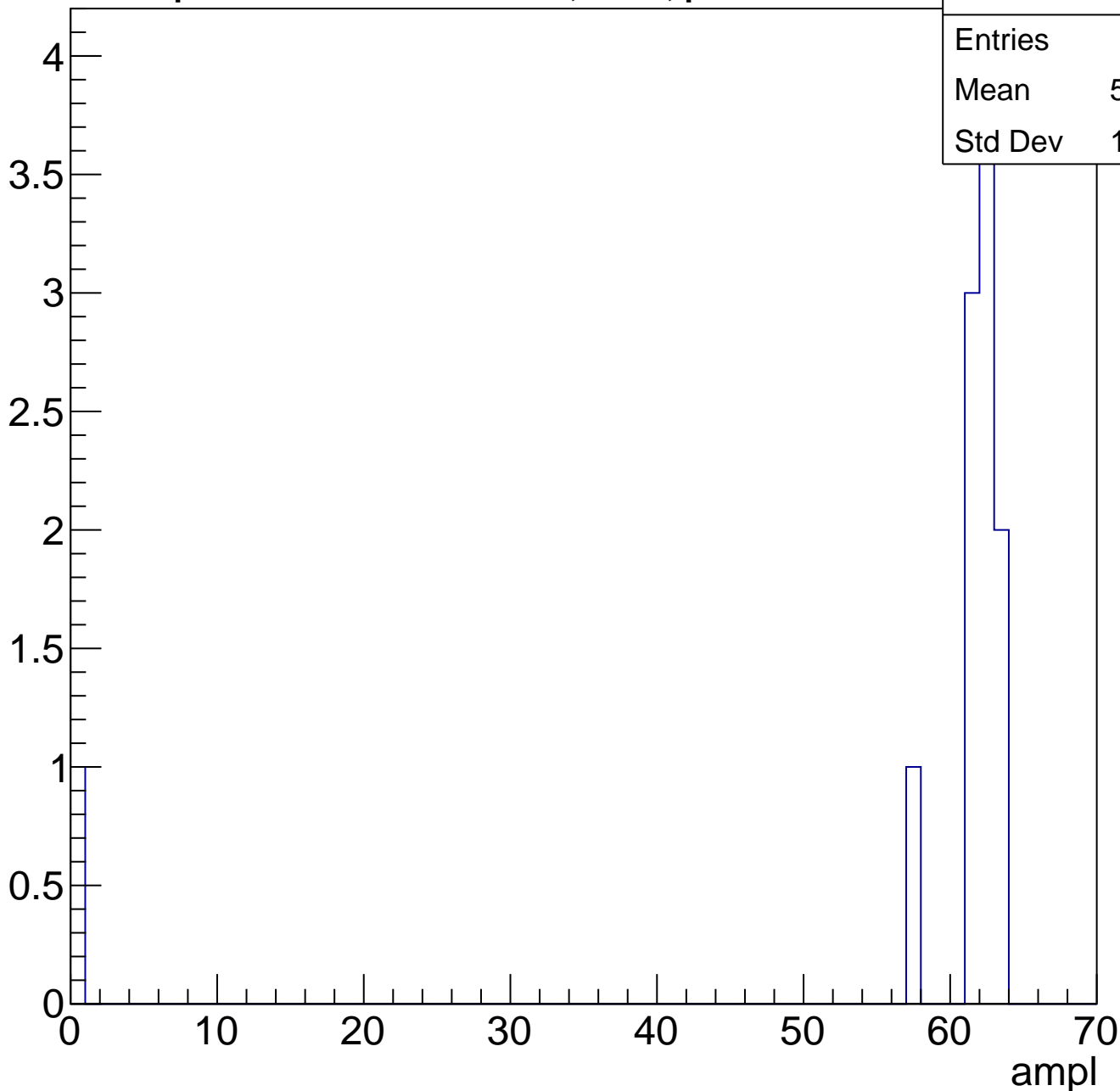
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	11
Mean	55.82
Std Dev	17.72



# B1L101S, U3-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	23
Std Dev	0

ampl

# B1L101S, U3-ch53, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	89
Mean	28.97
Std Dev	5.074

**Gaus mean : 30.5688**

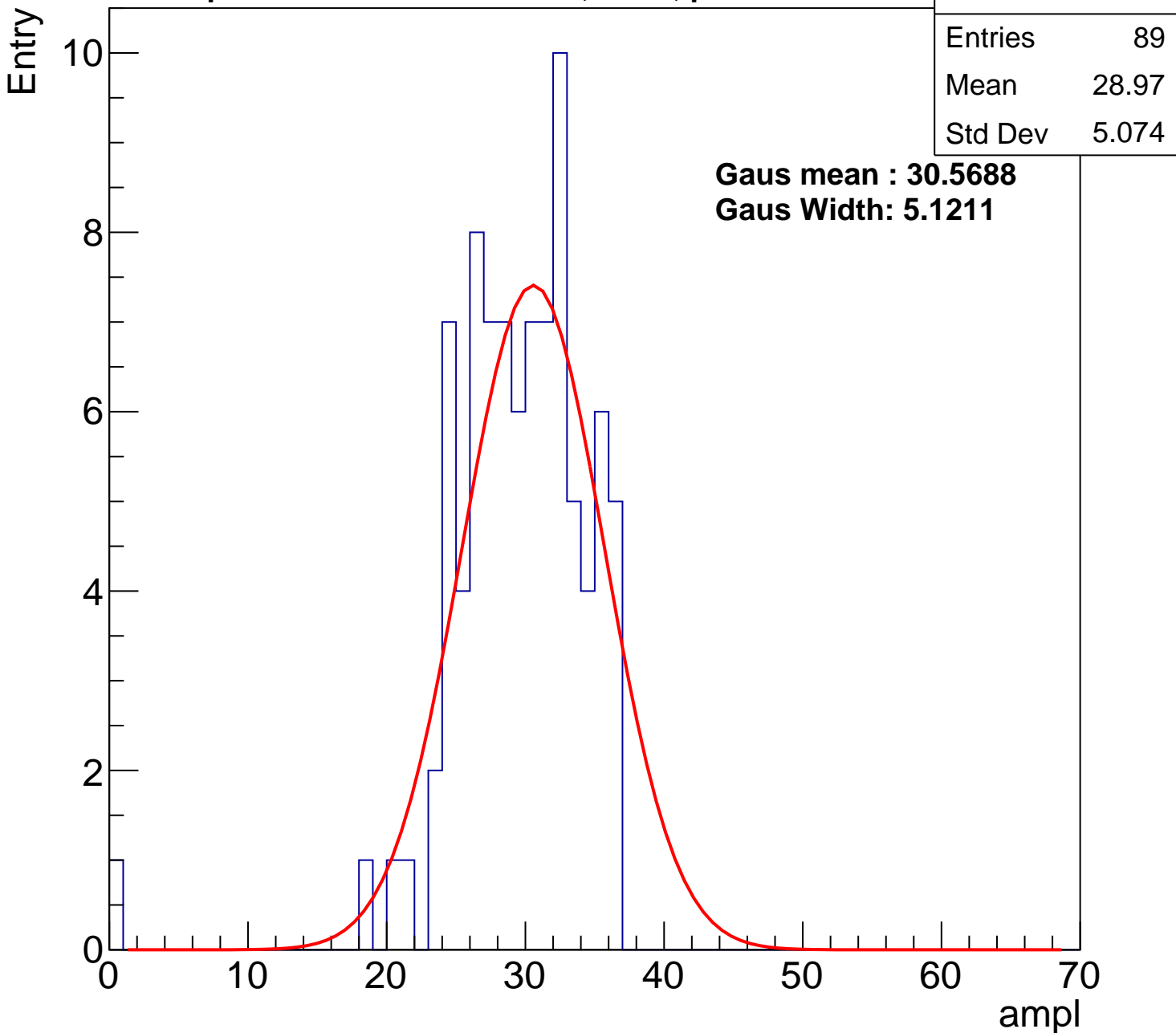
**Gaus Width: 5.1211**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U3-ch53, adc1

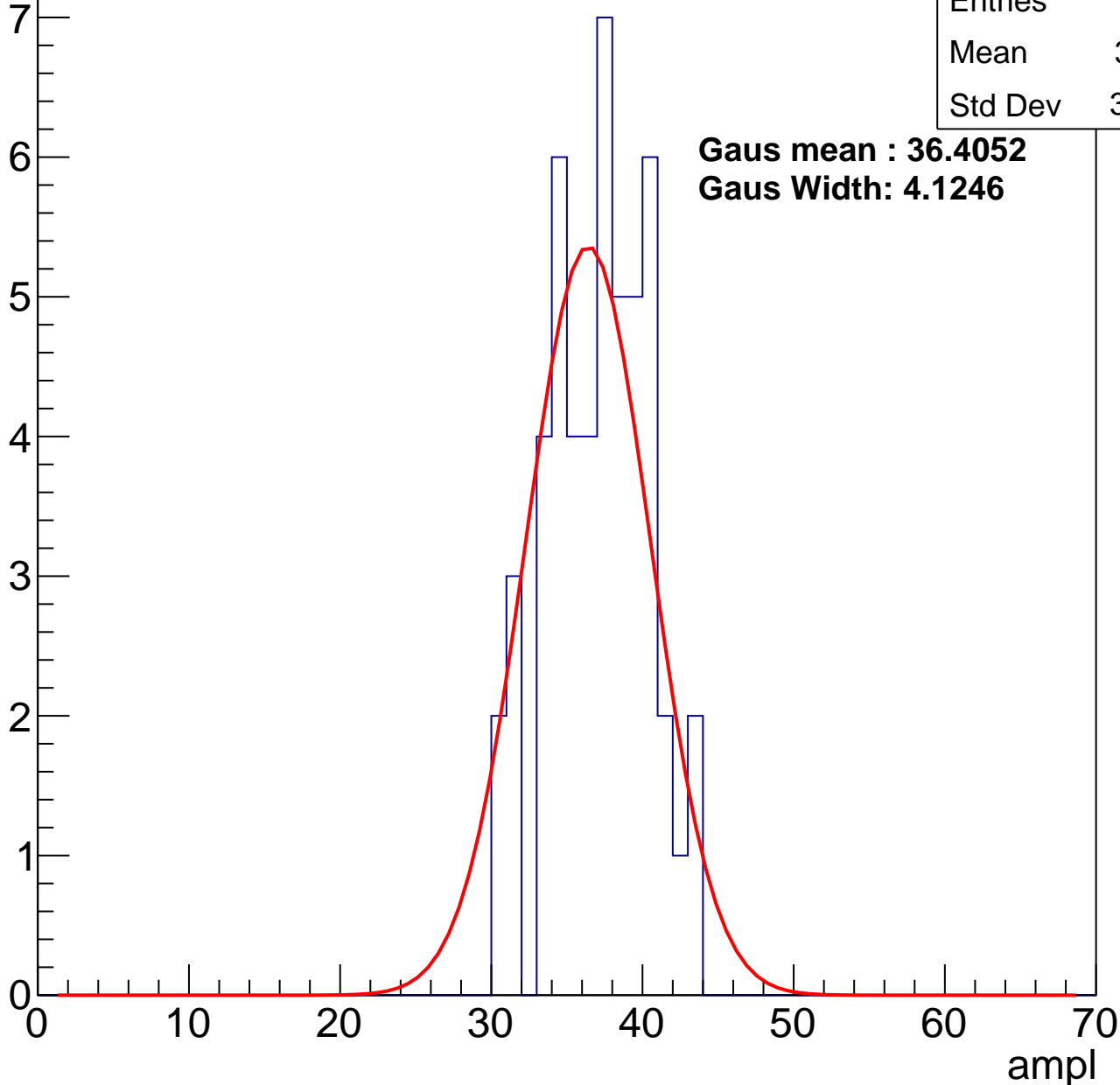
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	36.61
Std Dev	3.266

**Gaus mean : 36.4052**

**Gaus Width: 4.1246**



# B1L101S, U3-ch53, adc2

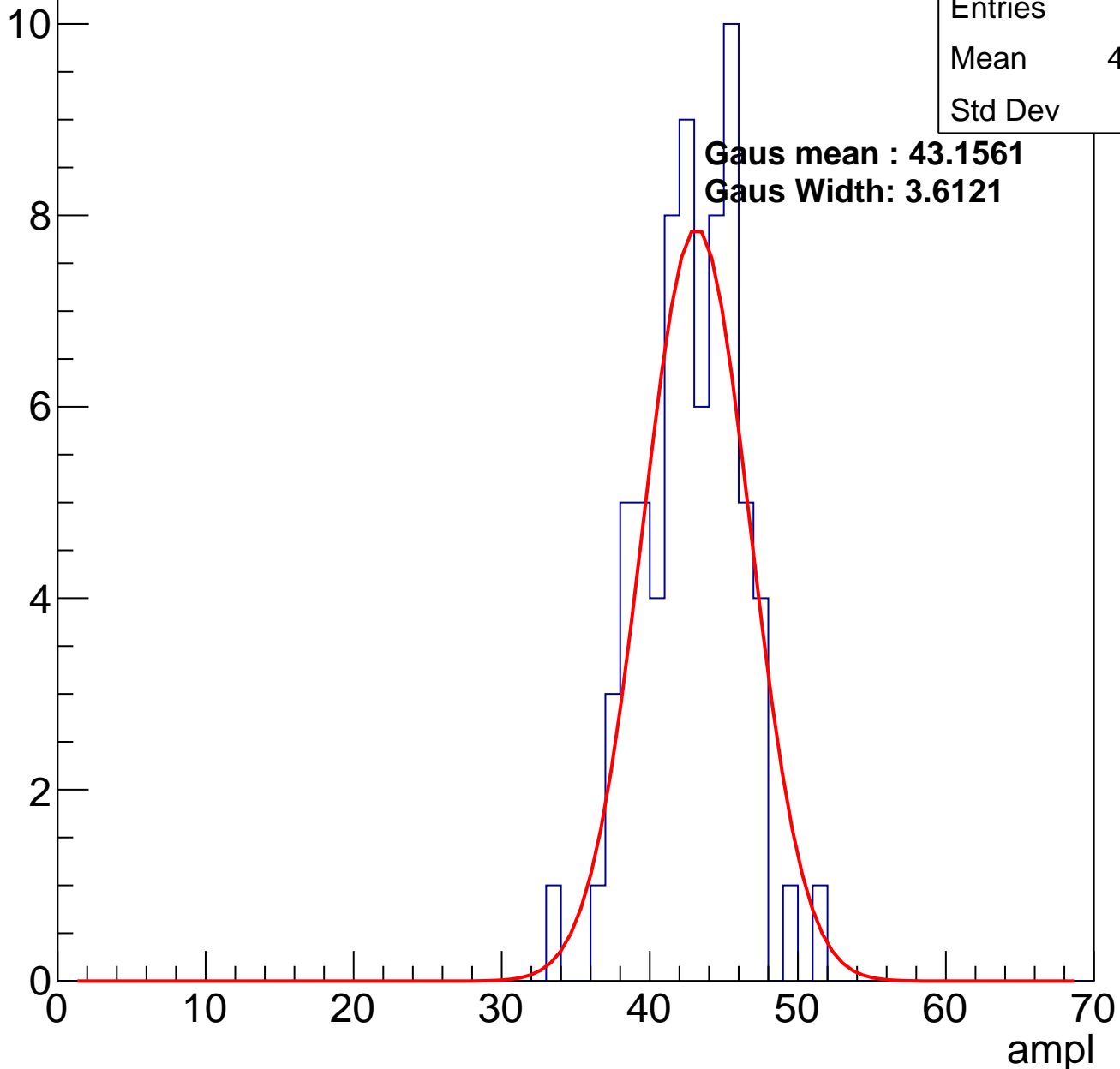
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	71
Mean	42.38
Std Dev	3.29

**Gaus mean : 43.1561**

**Gaus Width: 3.6121**

Entry

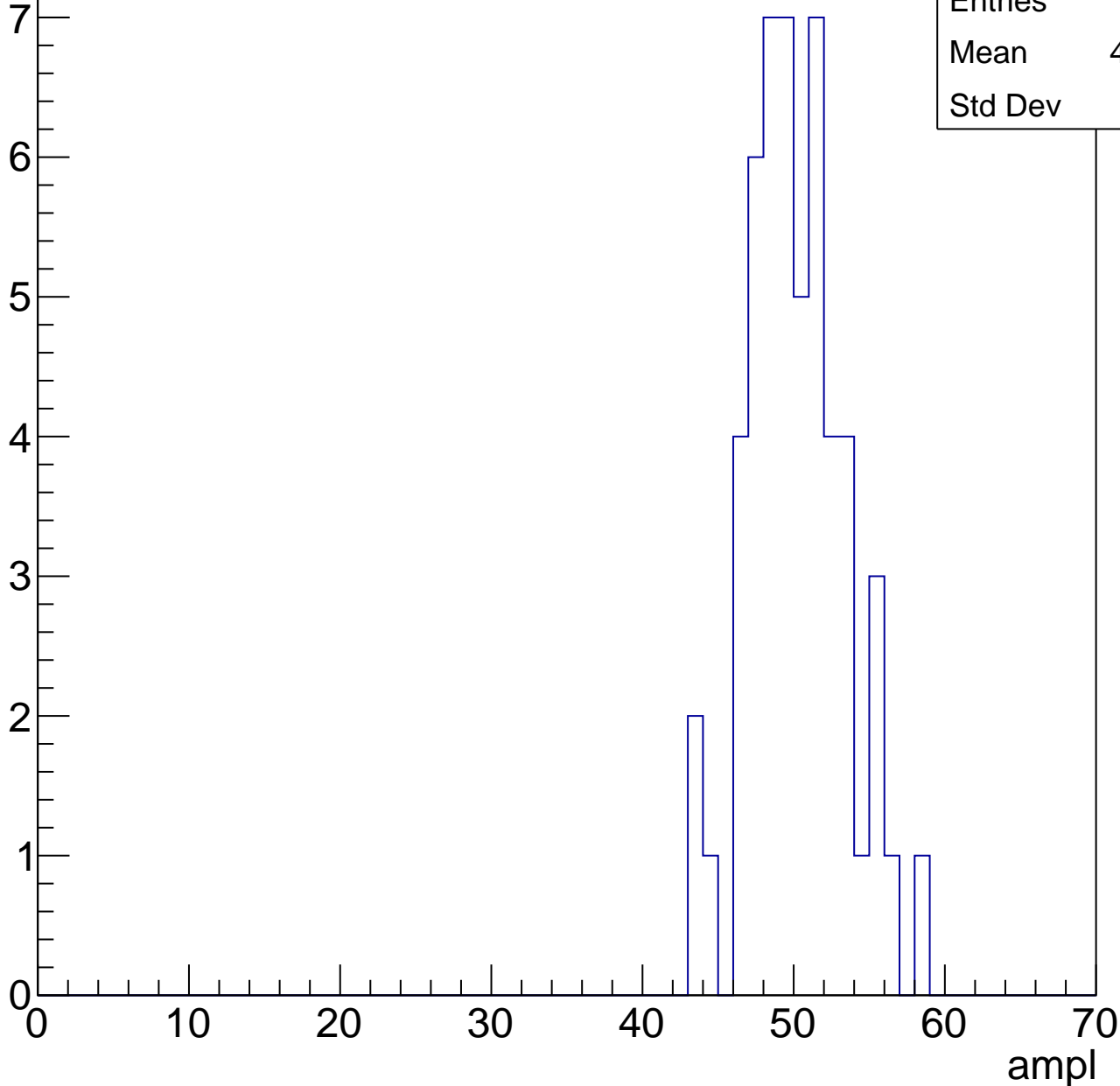


# B1L101S, U3-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	49.72
Std Dev	3.17

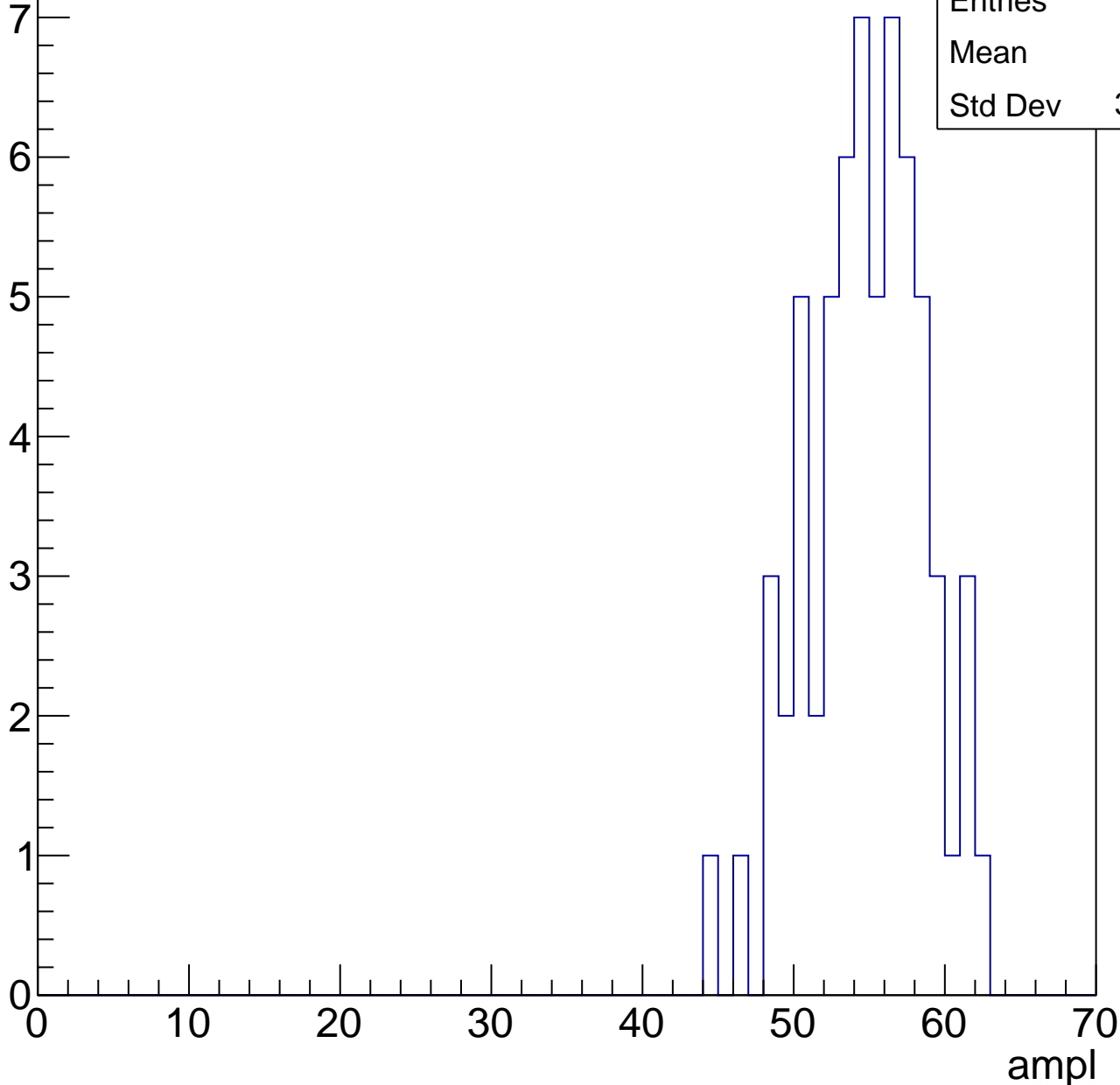


# B1L101S, U3-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	54.3
Std Dev	3.841

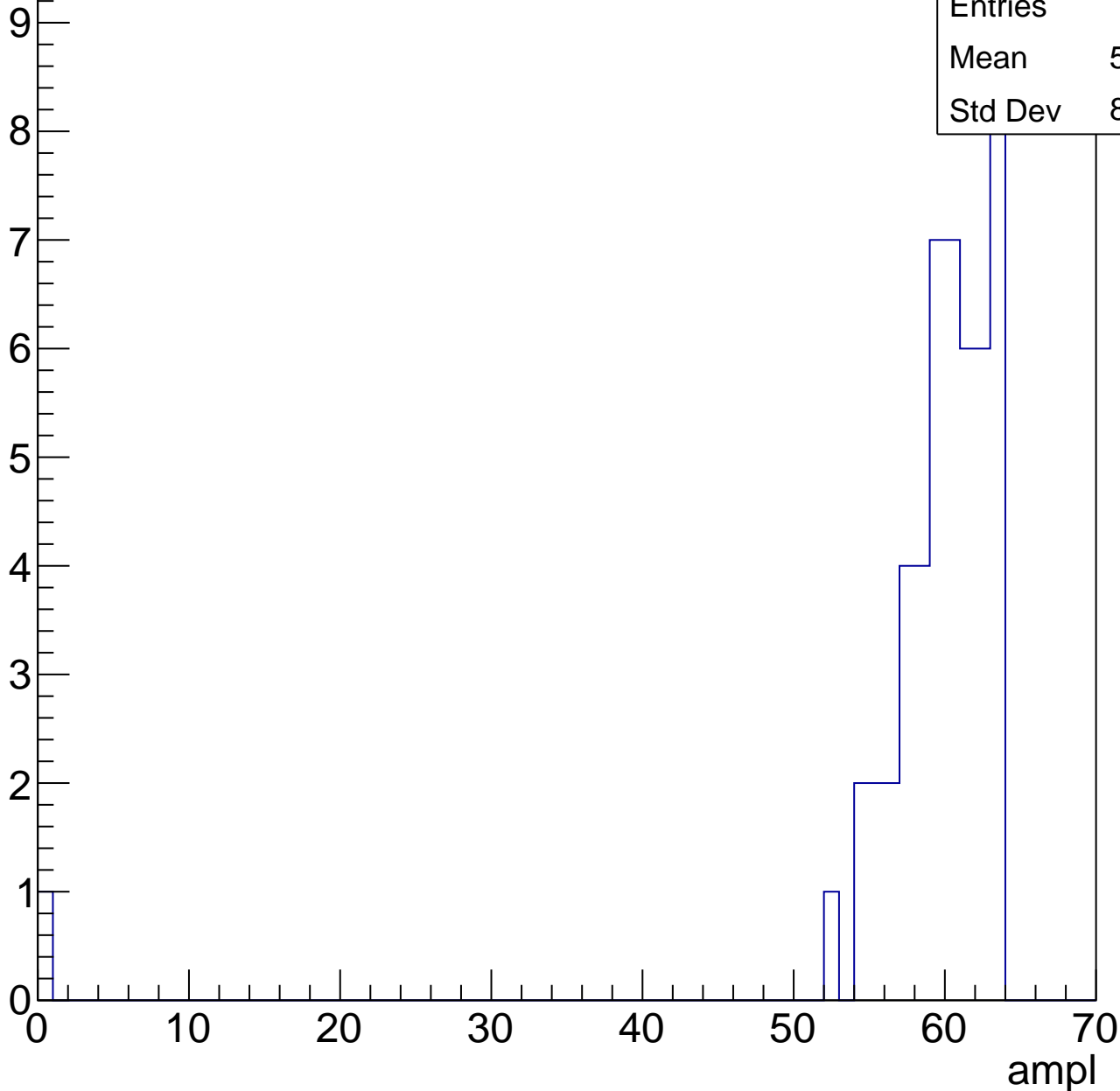


# B1L101S, U3-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

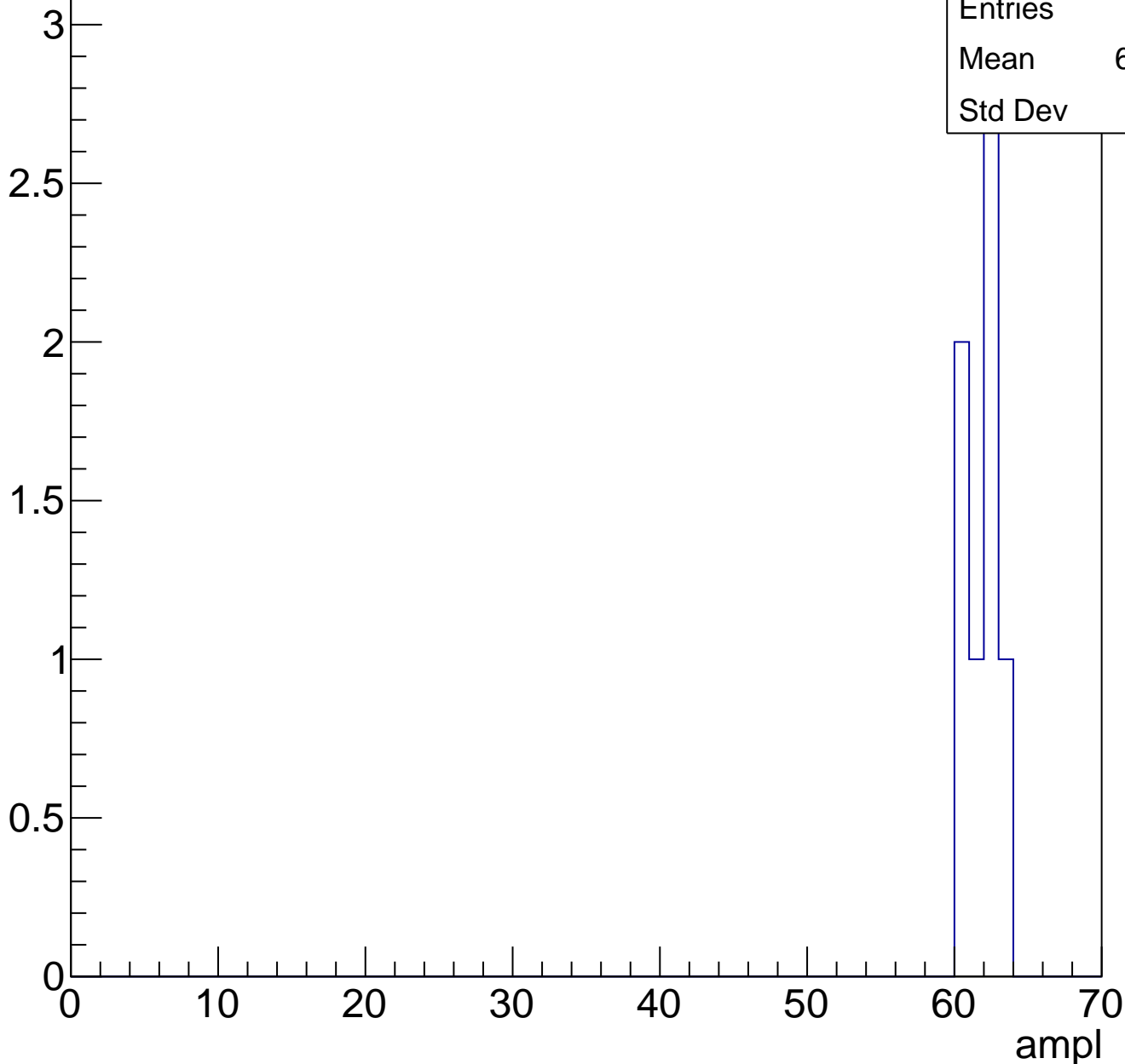
Entries	51
Mean	58.43
Std Dev	8.703



# B1L101S, U3-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U3-ch54, adc0

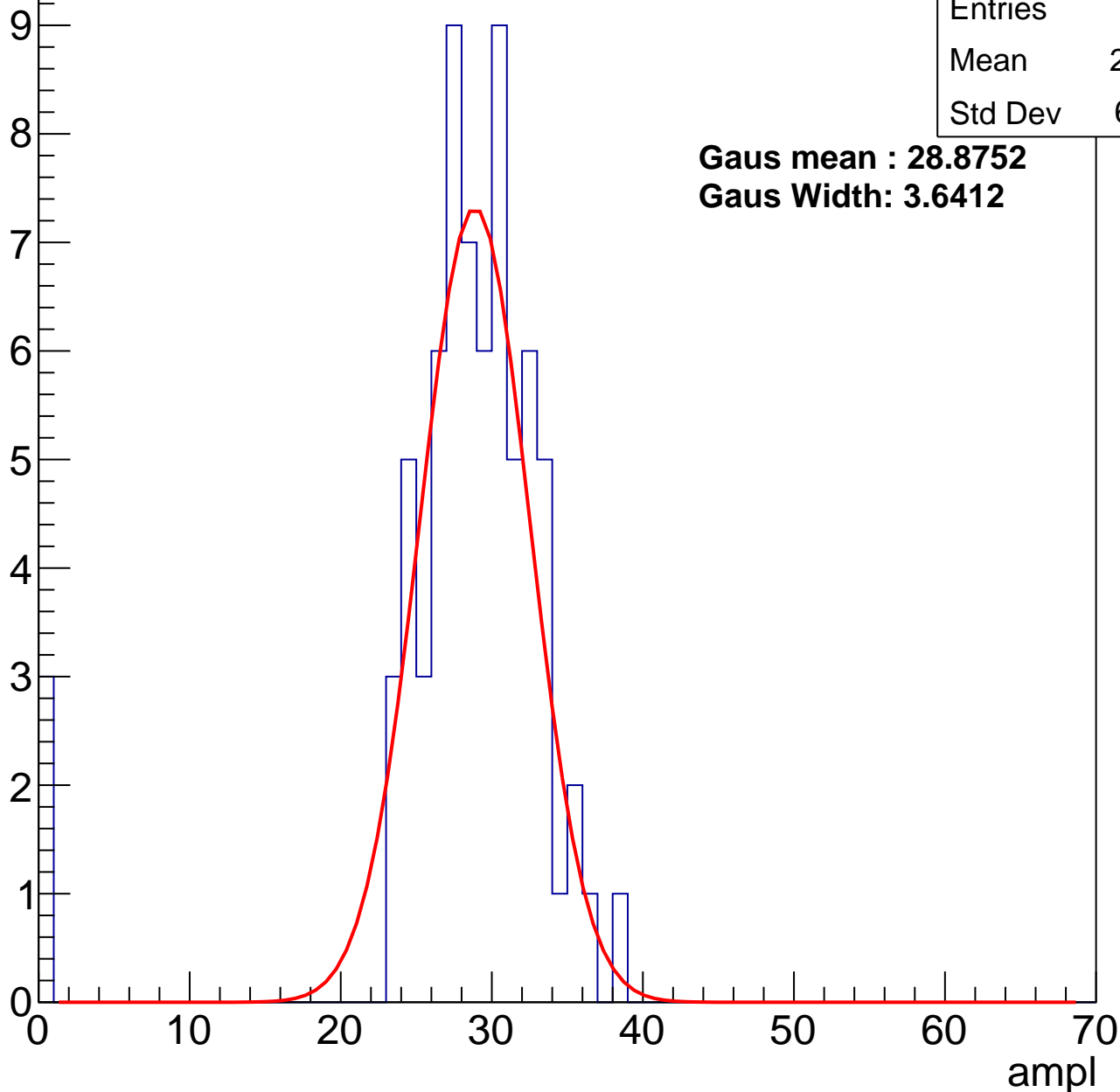
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	27.68
Std Dev	6.631

**Gaus mean : 28.8752**

**Gaus Width: 3.6412**



# B1L101S, U3-ch54, adc1

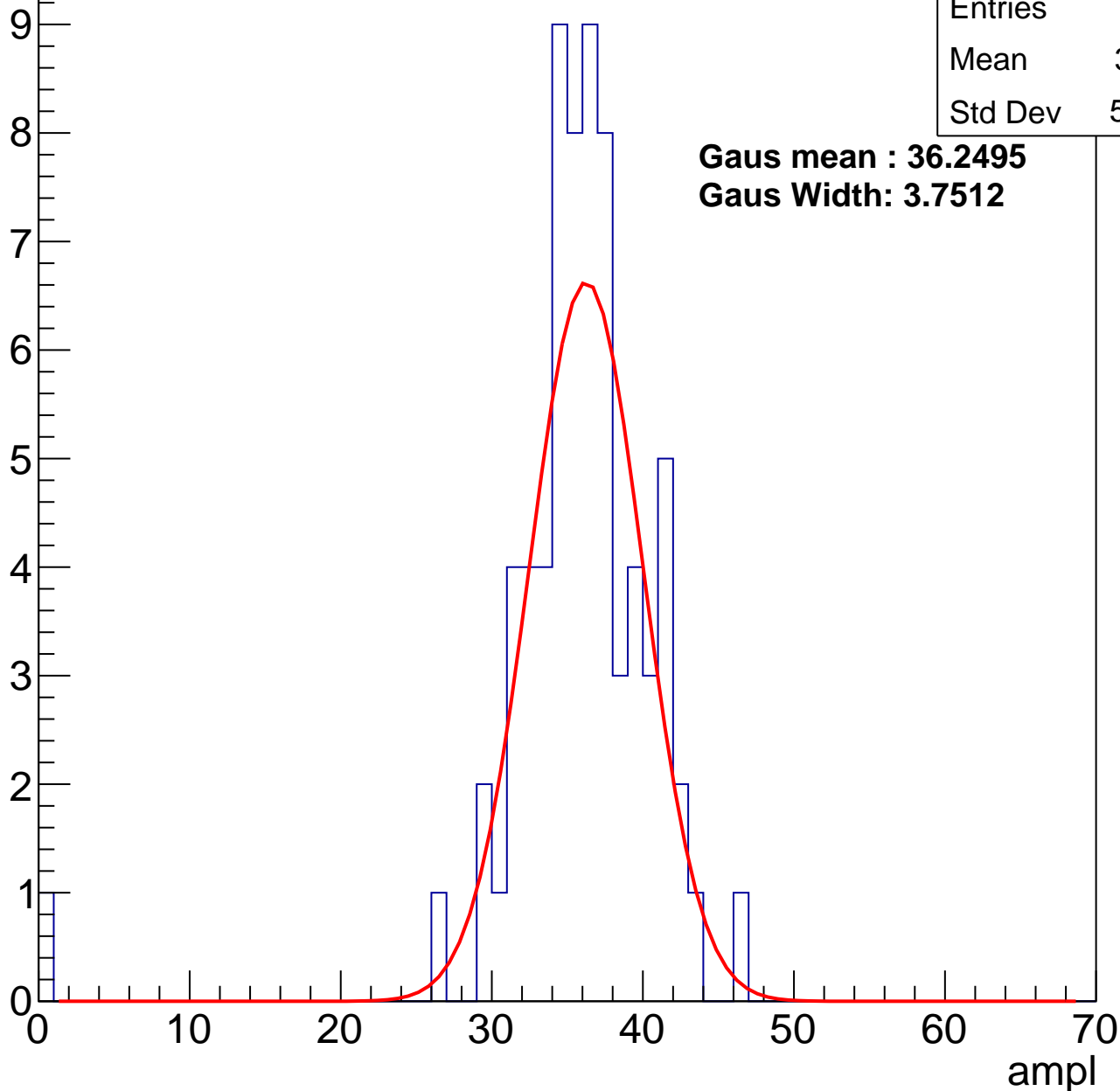
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	35.31
Std Dev	5.595

**Gaus mean : 36.2495**

**Gaus Width: 3.7512**



# B1L101S, U3-ch54, adc2

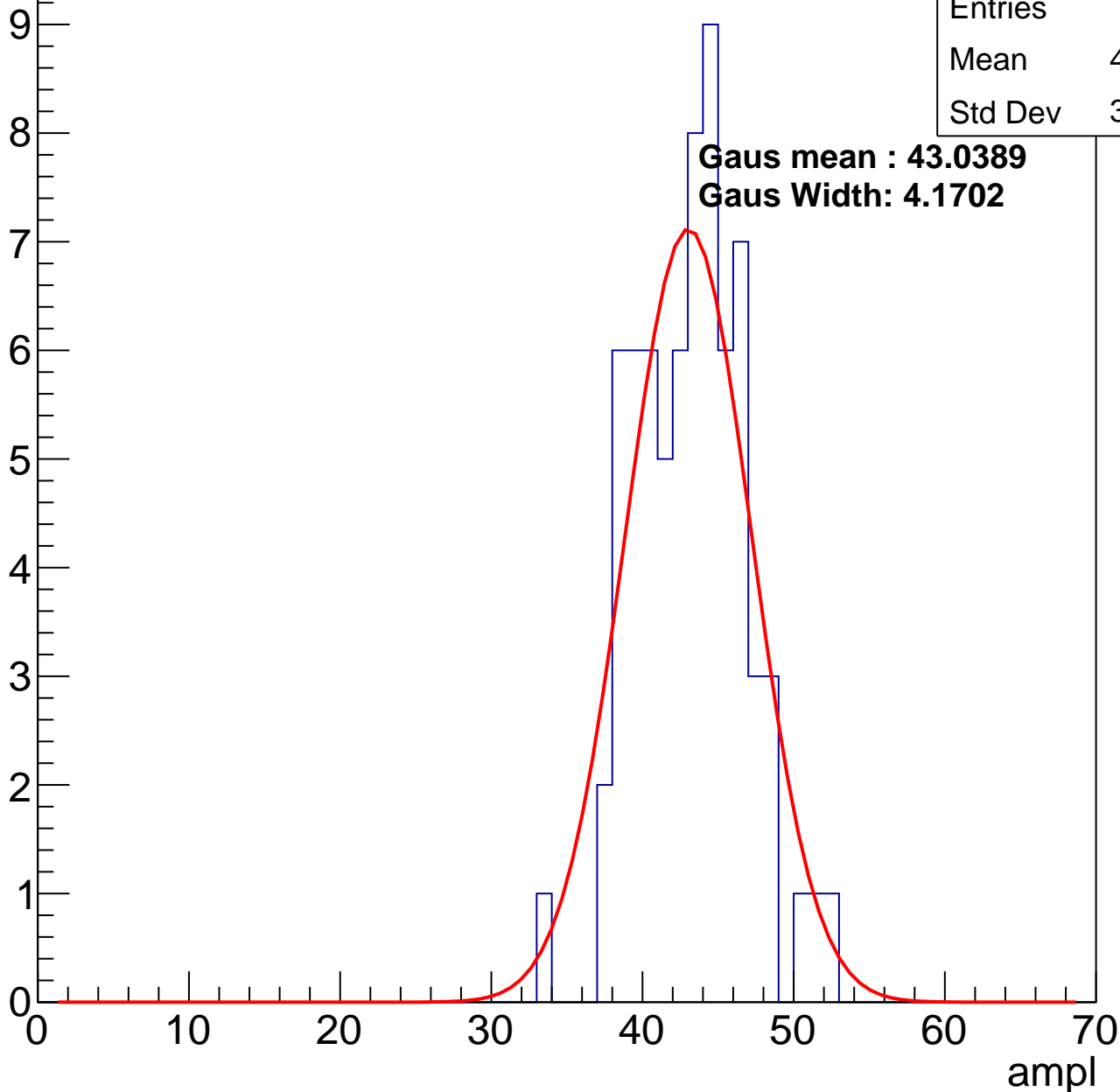
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	42.76
Std Dev	3.574

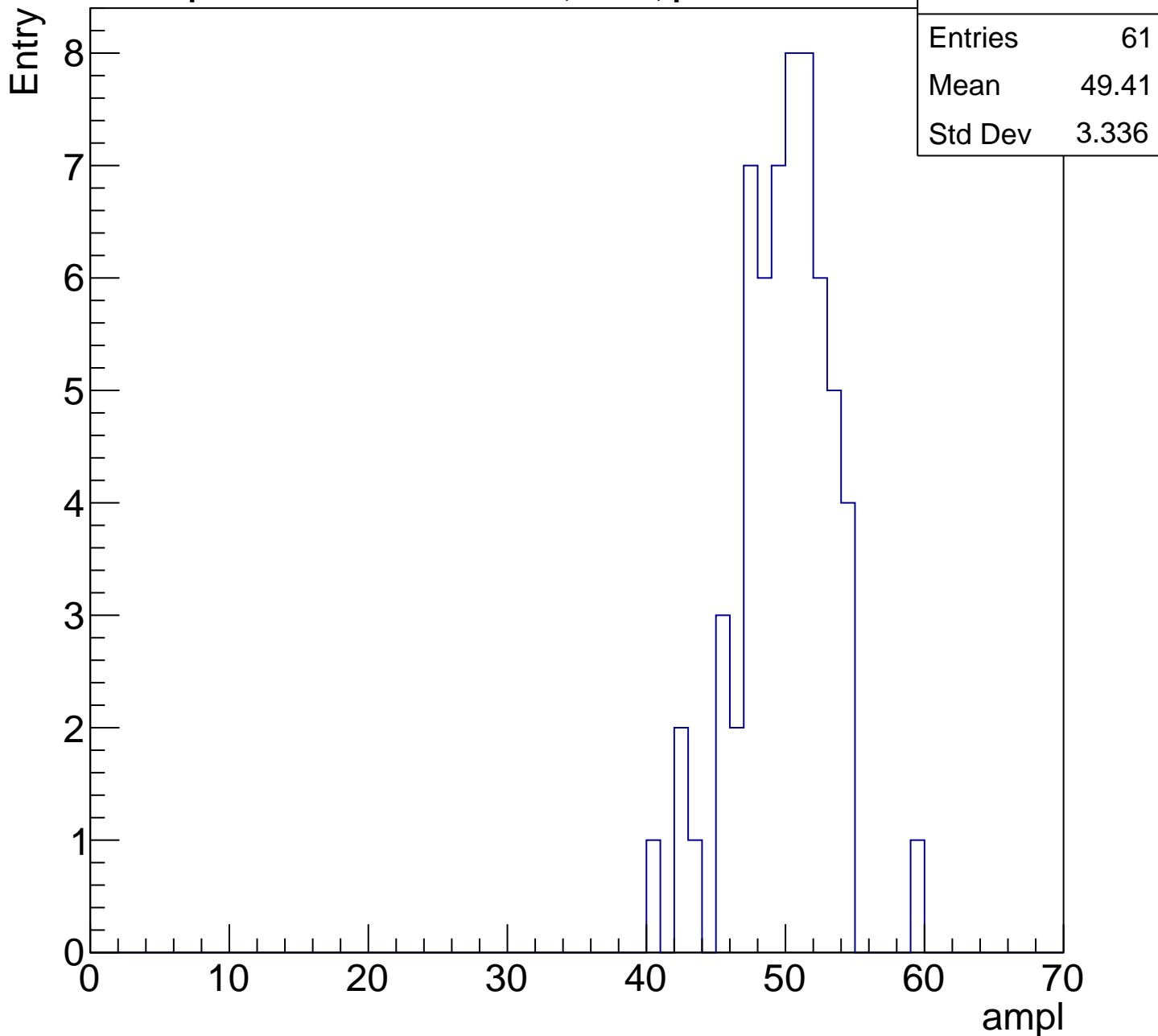
**Gaus mean : 43.0389**

**Gaus Width: 4.1702**



# B1L101S, U3-ch54, adc3

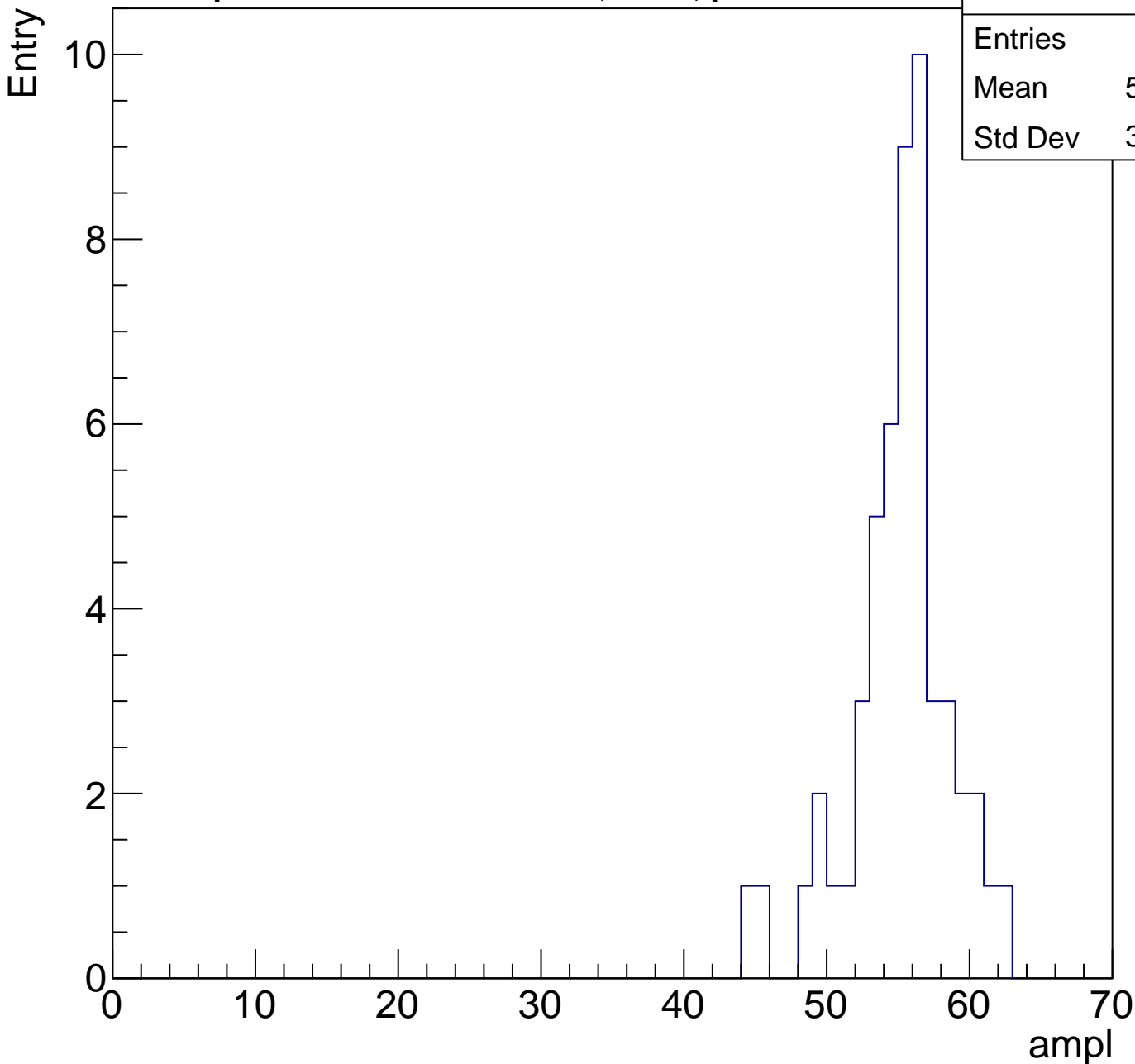
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	52
Mean	54.65
Std Dev	3.524

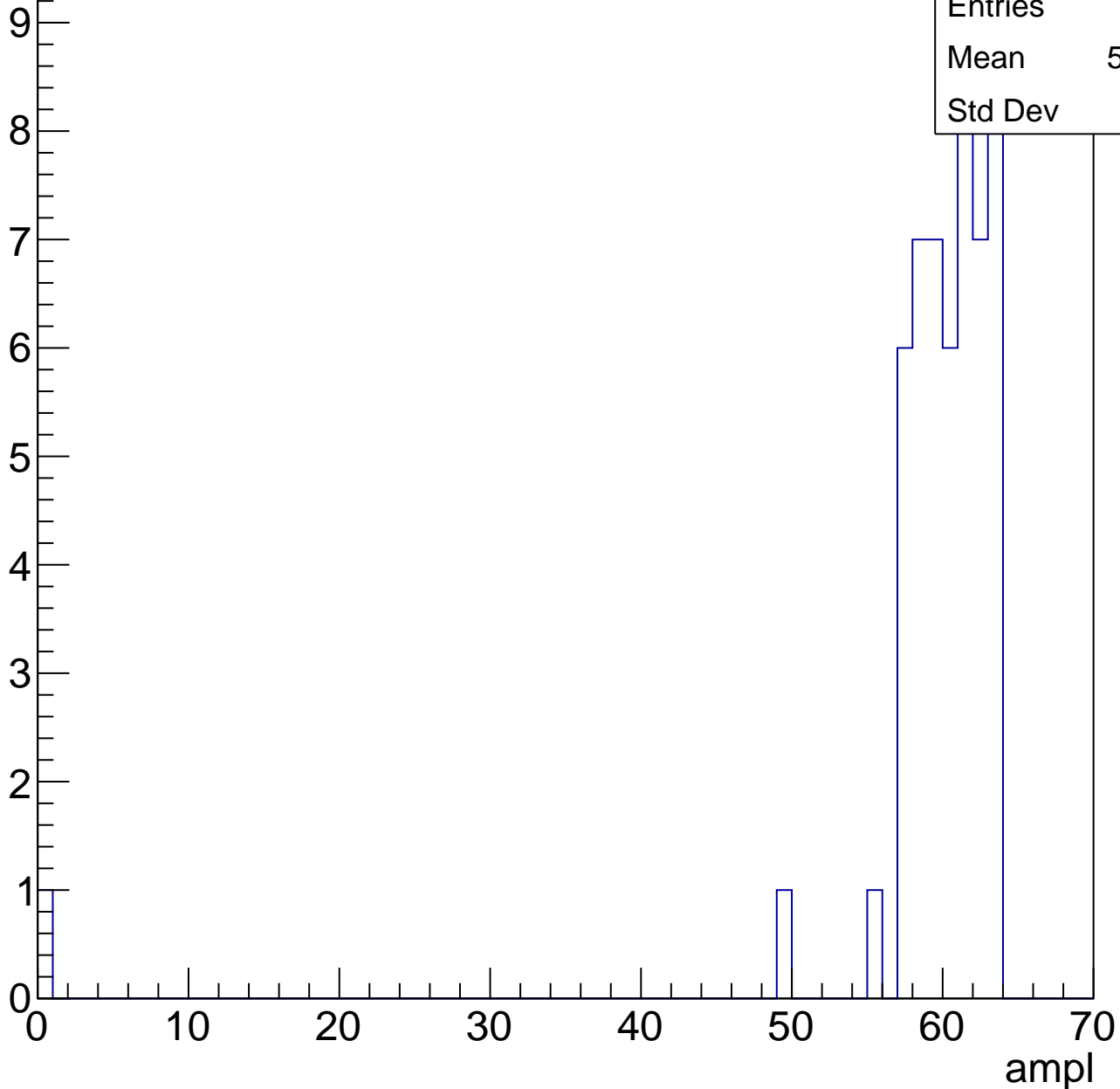


# B1L101S, U3-ch54, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	58.72
Std Dev	8.53



# B1L101S, U3-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

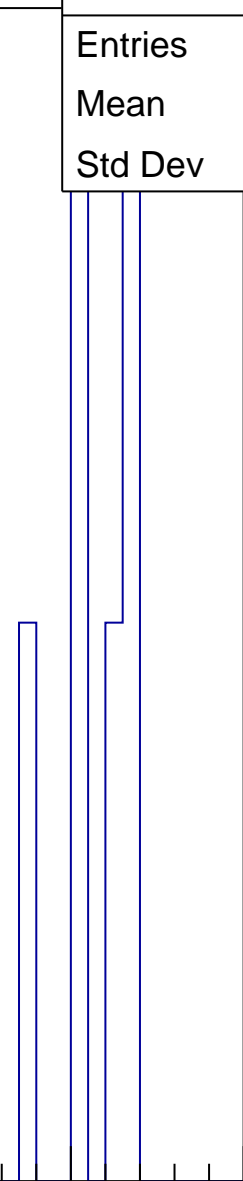
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	60.83
Std Dev	2.115

0 10 20 30 40 50 60 70

ampl





# B1L101S, U3-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch55, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	82
Mean	29.62
Std Dev	4.82

**Gaus mean : 30.1249**

**Gaus Width: 3.9835**

Entry

10  
8  
6  
4  
2  
0

ampl

0

10

20

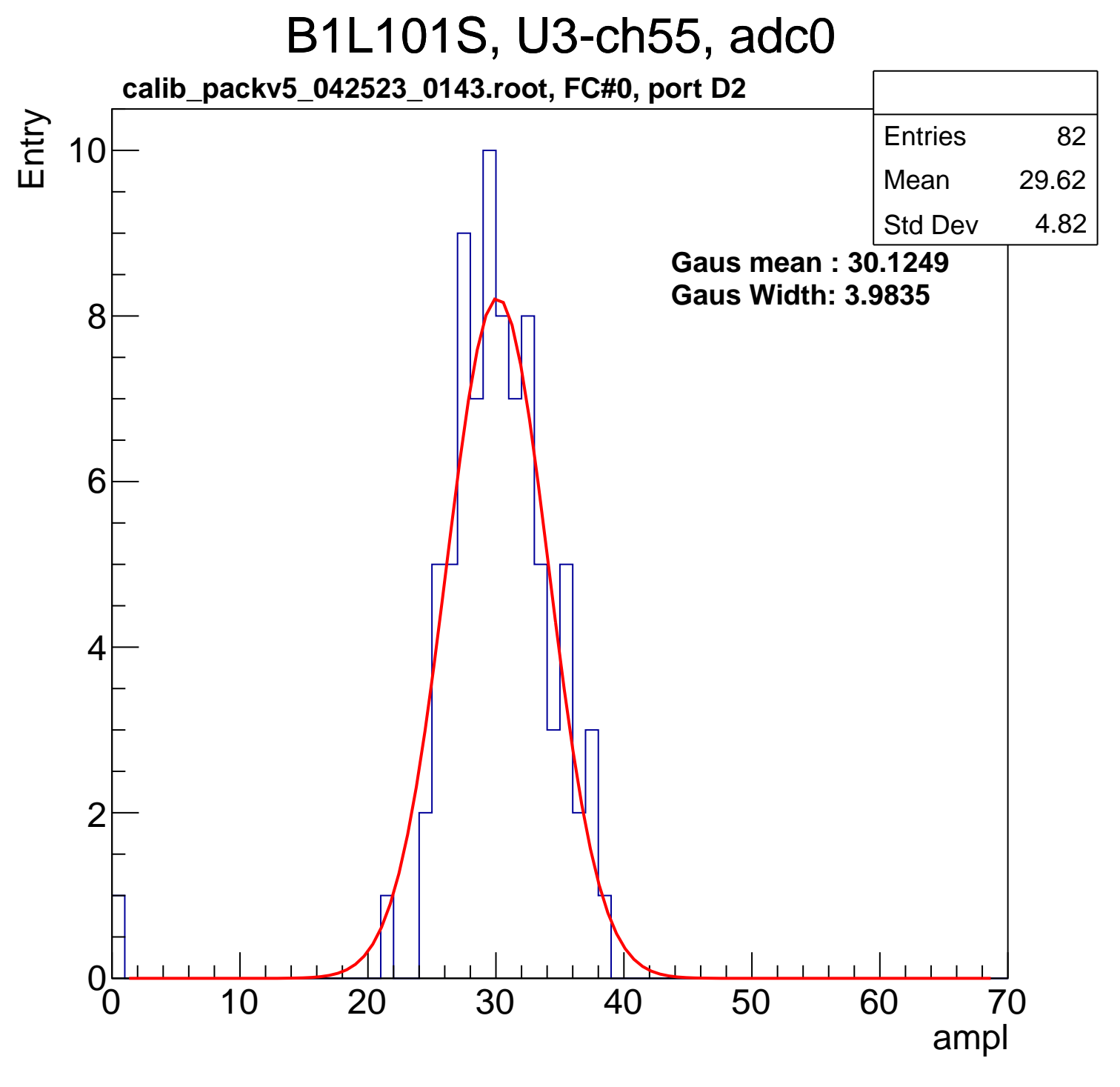
30

40

50

60

70



# B1L101S, U3-ch55, adc1

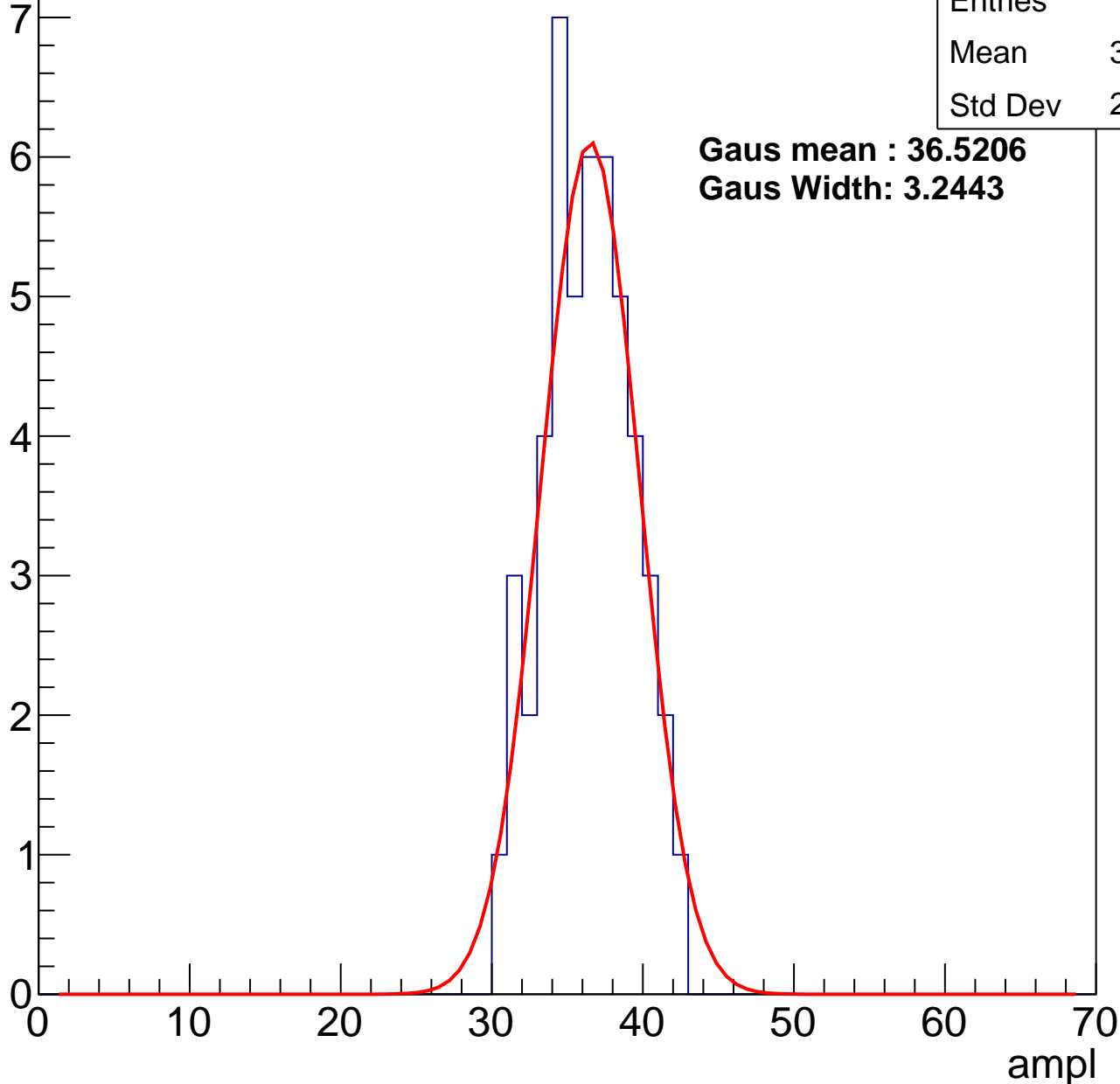
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	35.92
Std Dev	2.884

**Gaus mean : 36.5206**

**Gaus Width: 3.2443**



# B1L101S, U3-ch55, adc2

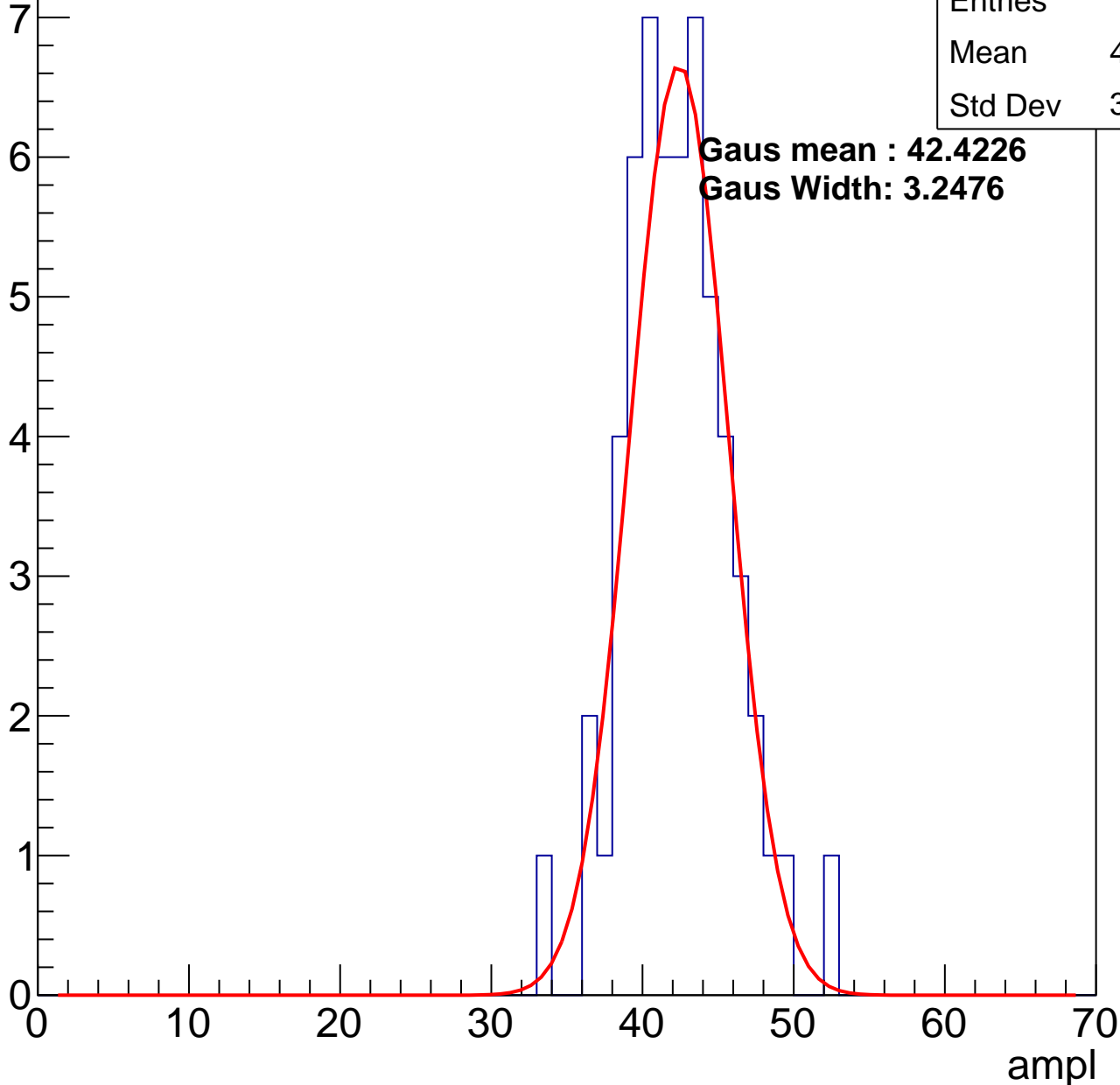
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	41.89
Std Dev	3.442

**Gaus mean : 42.4226**

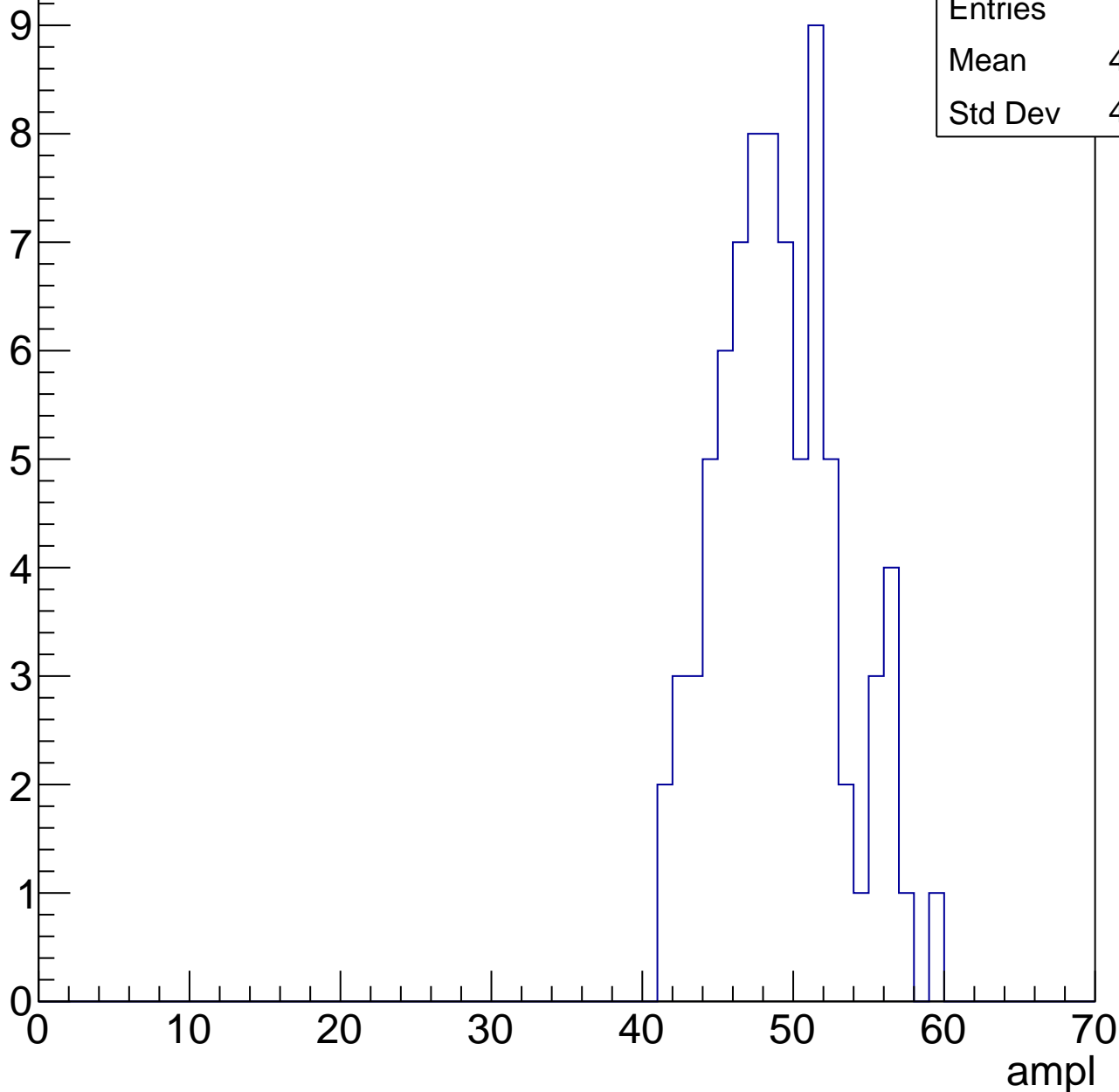
**Gaus Width: 3.2476**



# B1L101S, U3-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



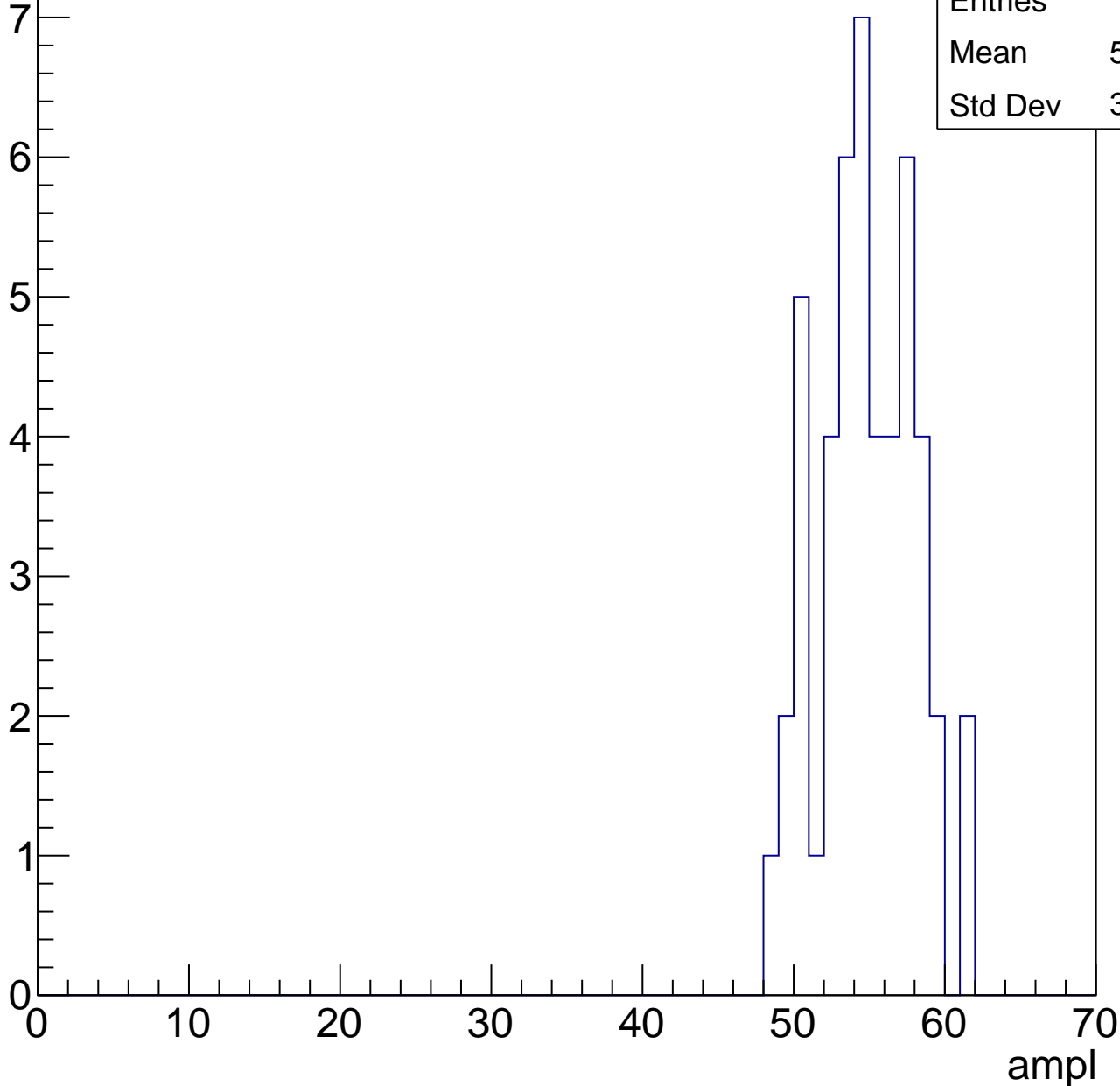
Entries	80
Mean	48.58
Std Dev	4.037

# B1L101S, U3-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	54.35
Std Dev	3.152



# B1L101S, U3-ch55, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

Entries 50

Mean 59.38

Std Dev 2.856

ampl

0

10

20

30

40

50

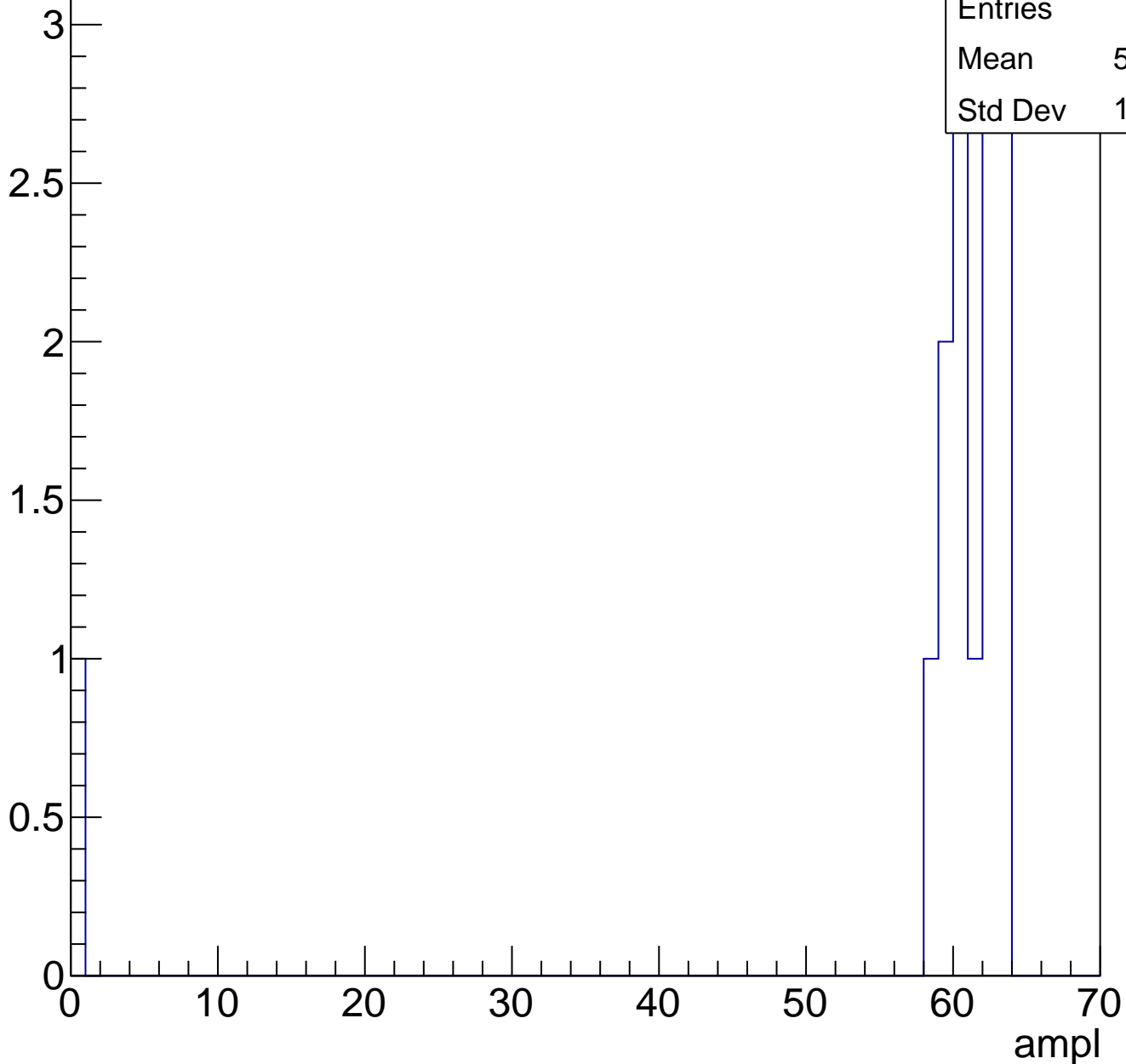
60

70

# B1L101S, U3-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch56, adc0

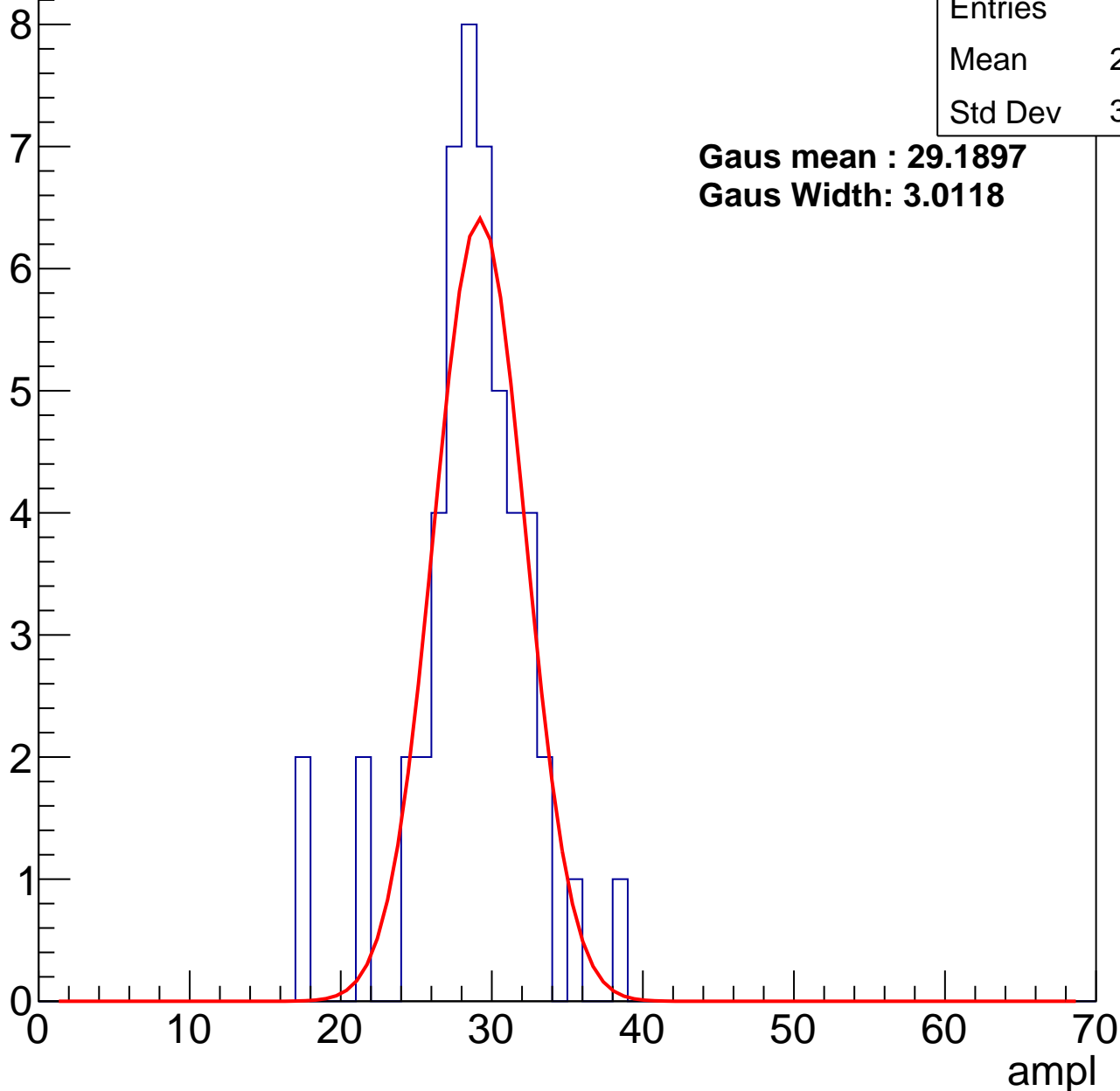
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	28.14
Std Dev	3.804

**Gaus mean : 29.1897**

**Gaus Width: 3.0118**



# B1L101S, U3-ch56, adc1

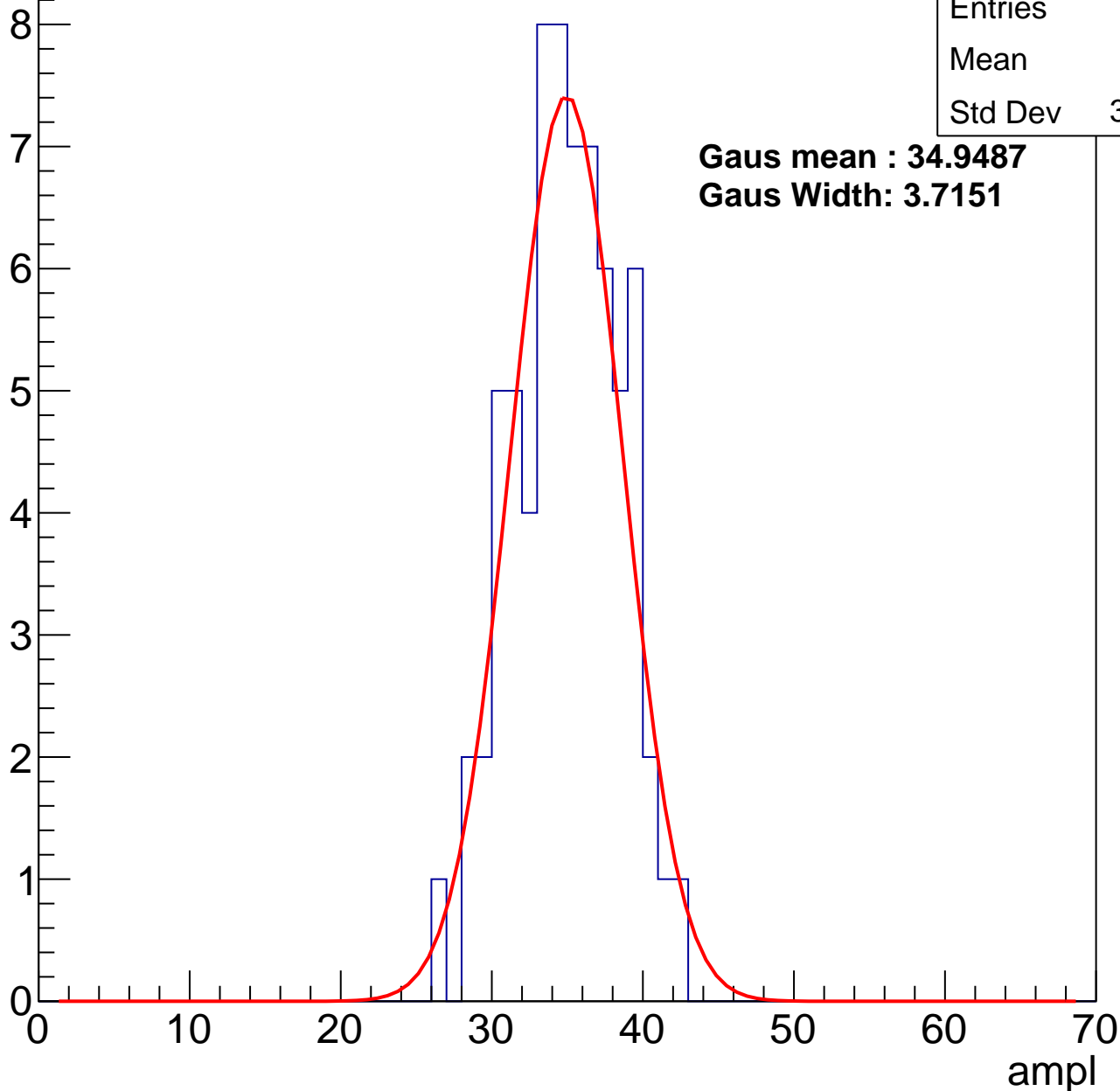
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	34.5
Std Dev	3.426

**Gaus mean : 34.9487**

**Gaus Width: 3.7151**



# B1L101S, U3-ch56, adc2

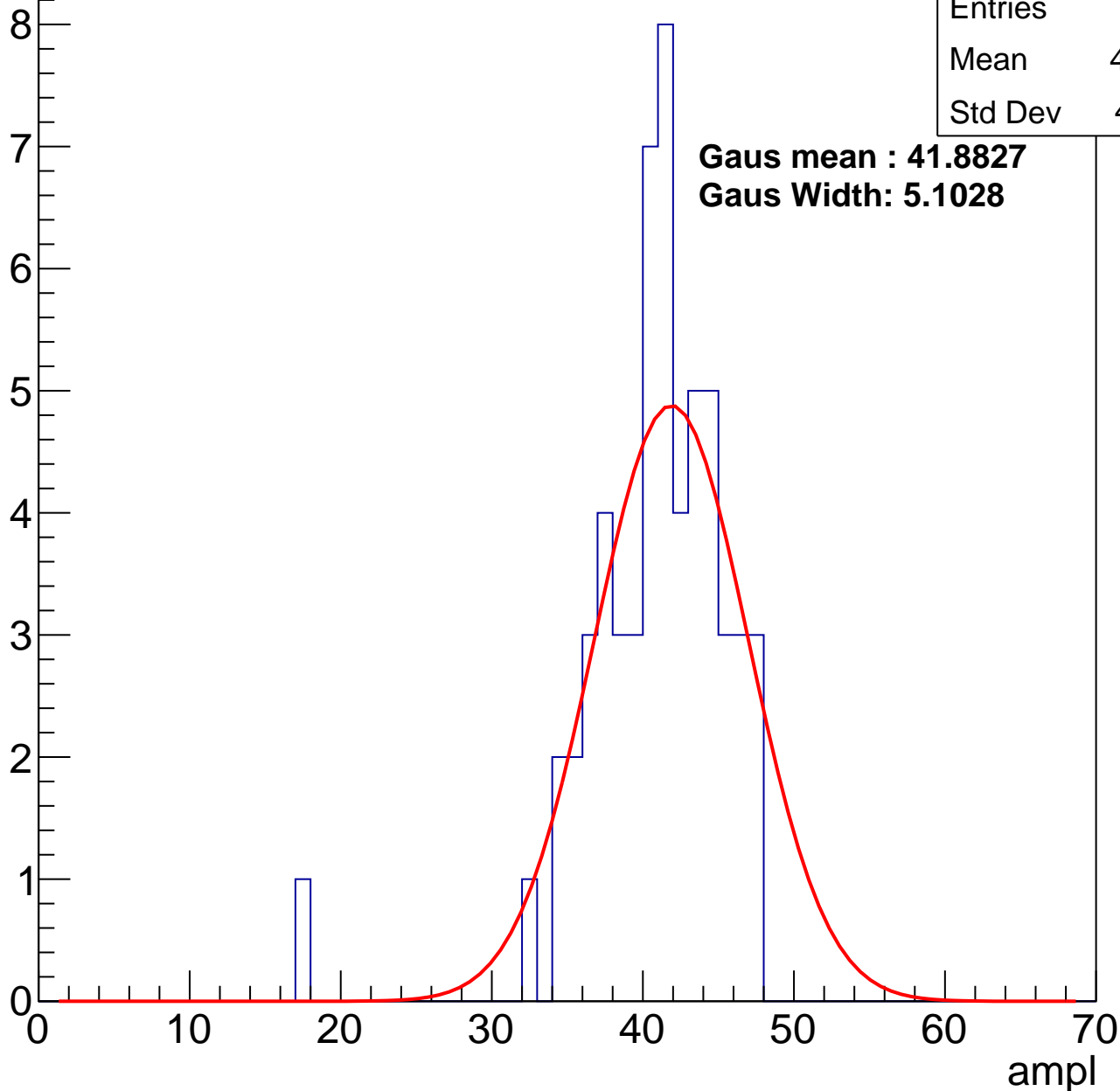
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	40.33
Std Dev	4.751

**Gaus mean : 41.8827**

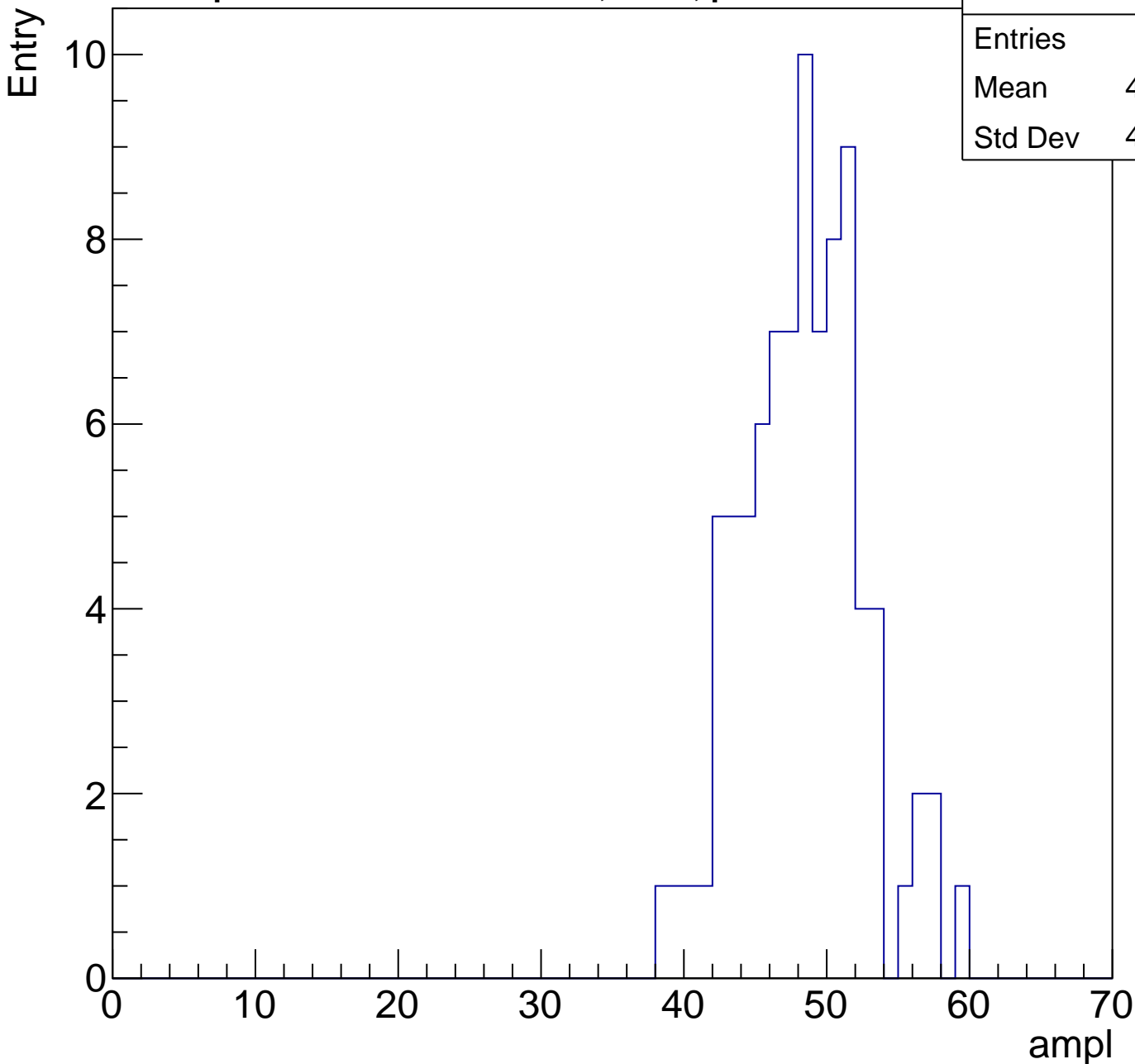
**Gaus Width: 5.1028**



# B1L101S, U3-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	87
Mean	47.89
Std Dev	4.167

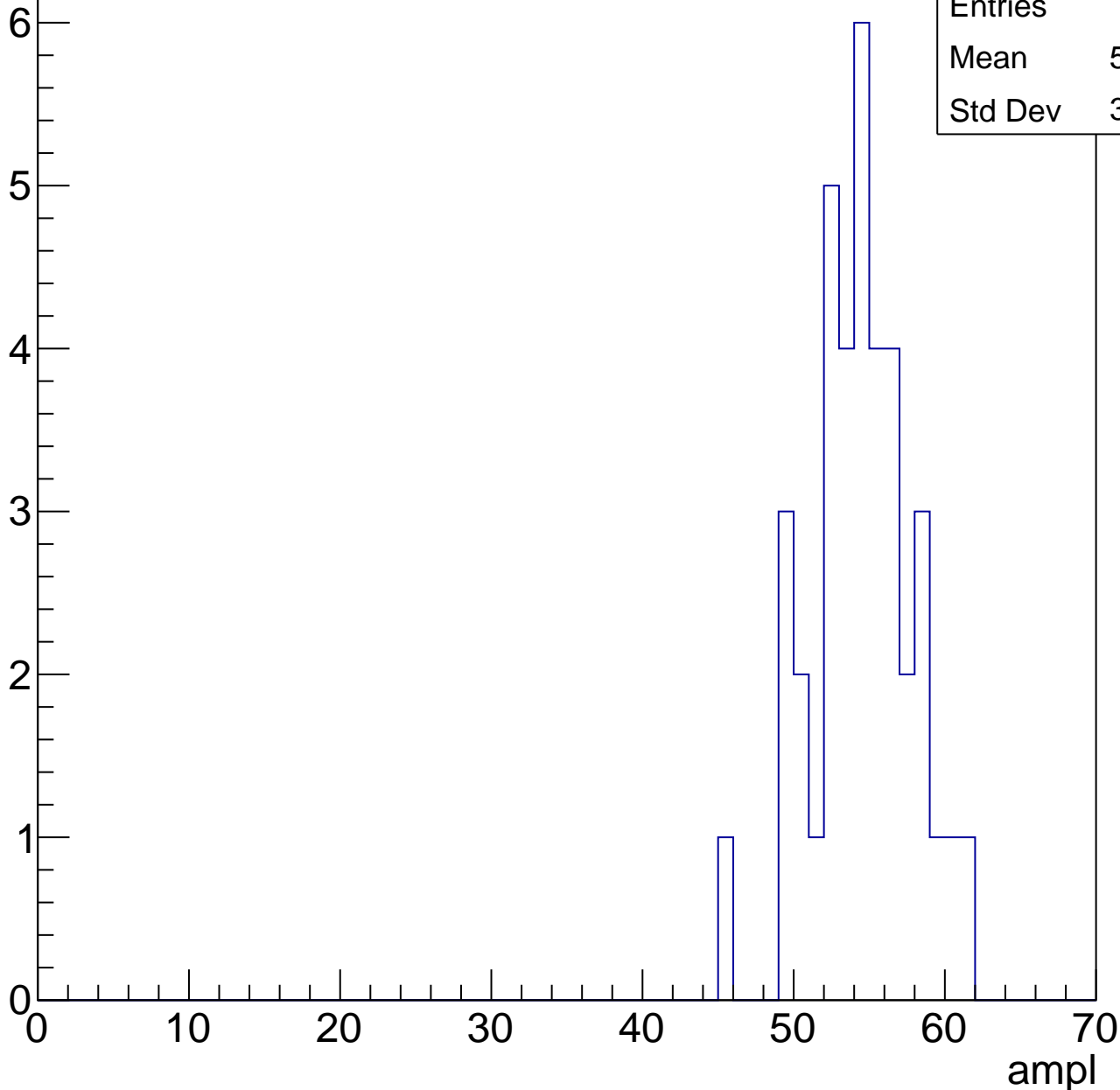


# B1L101S, U3-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

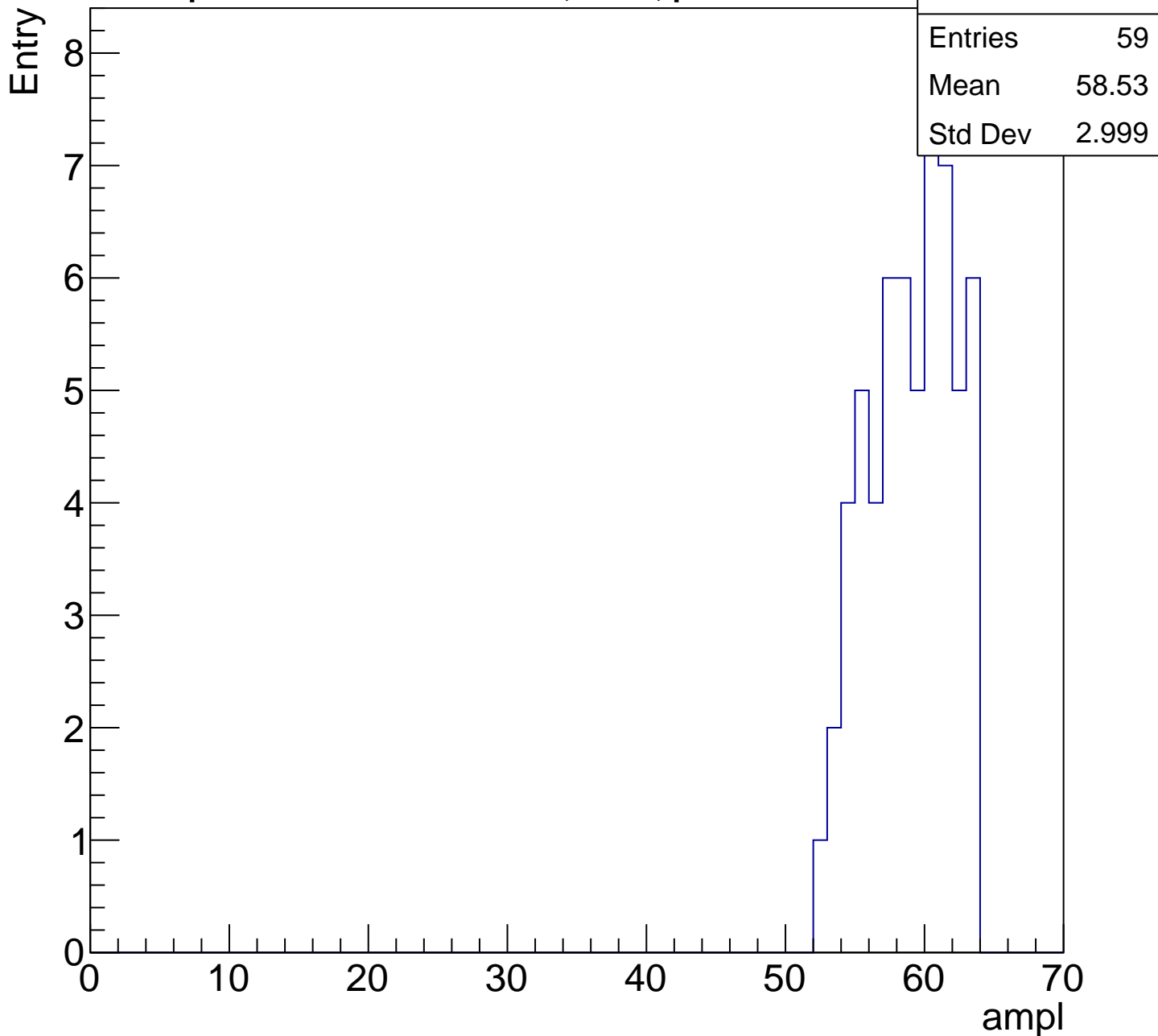
Entry

Entries	38
Mean	53.97
Std Dev	3.313



# B1L101S, U3-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

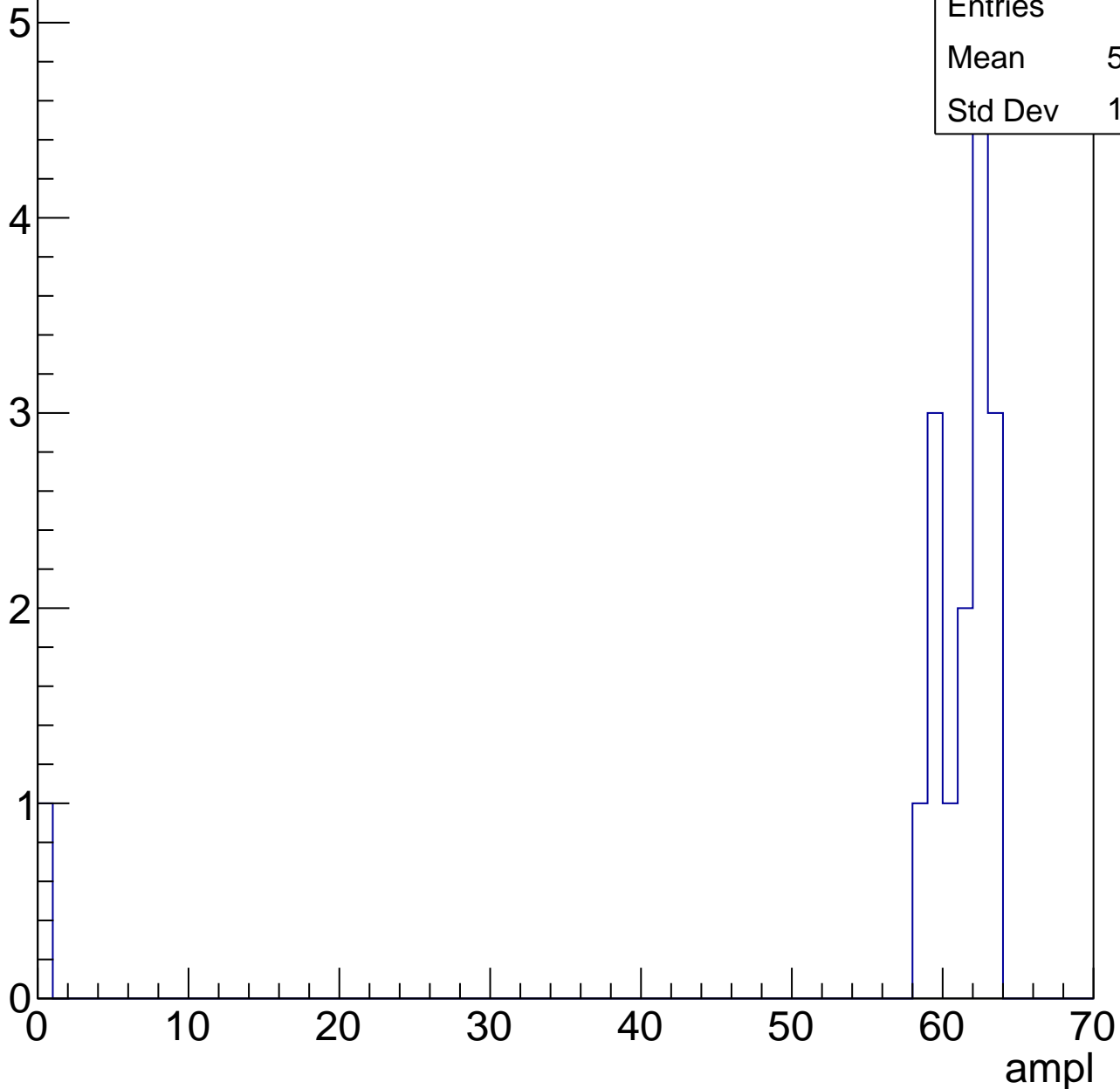


# B1L101S, U3-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	16
Mean	57.25
Std Dev	14.86

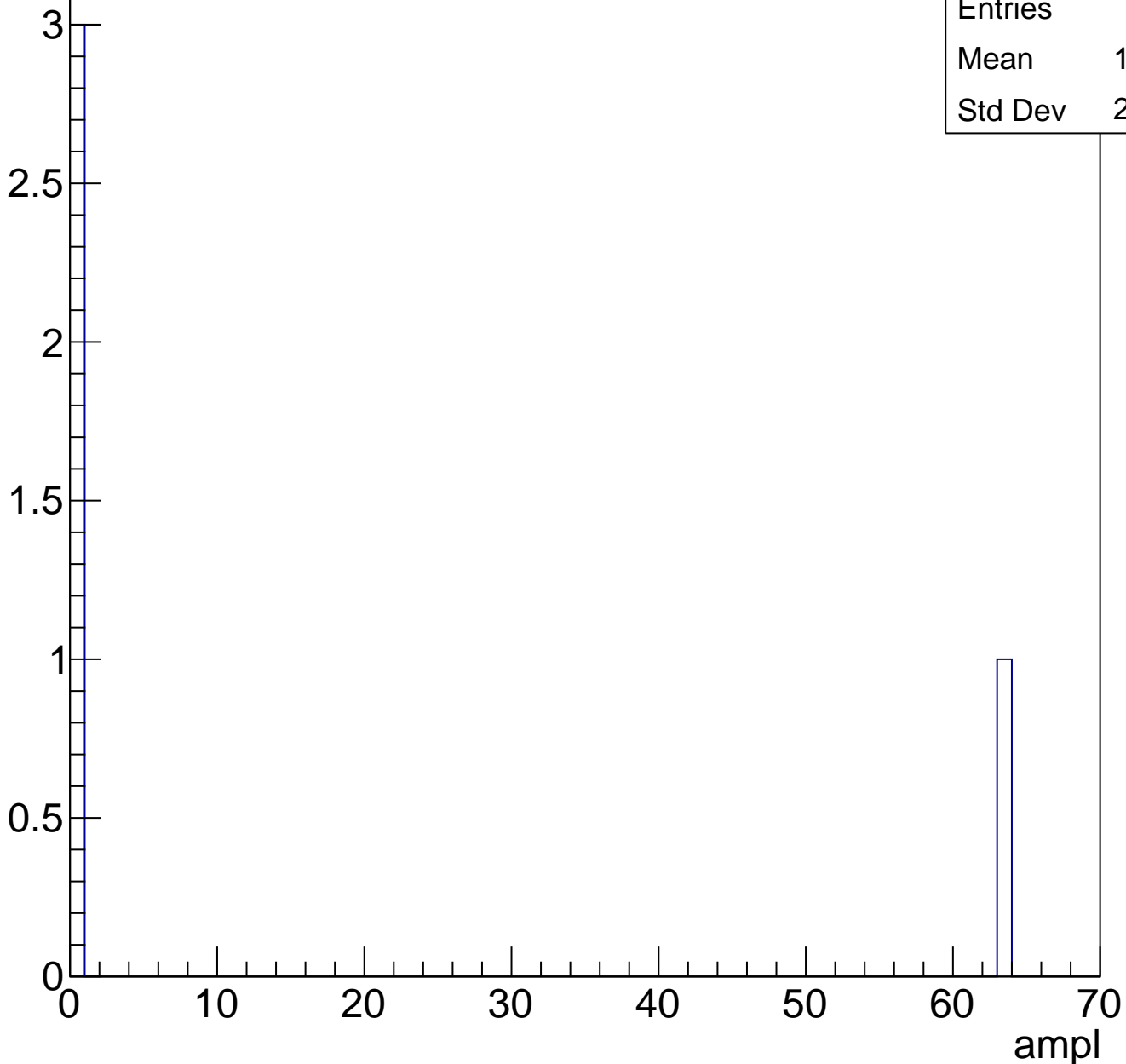




# B1L101S, U3-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch57, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	82
Mean	29.16
Std Dev	5.103

**Gaus mean : 29.6010**

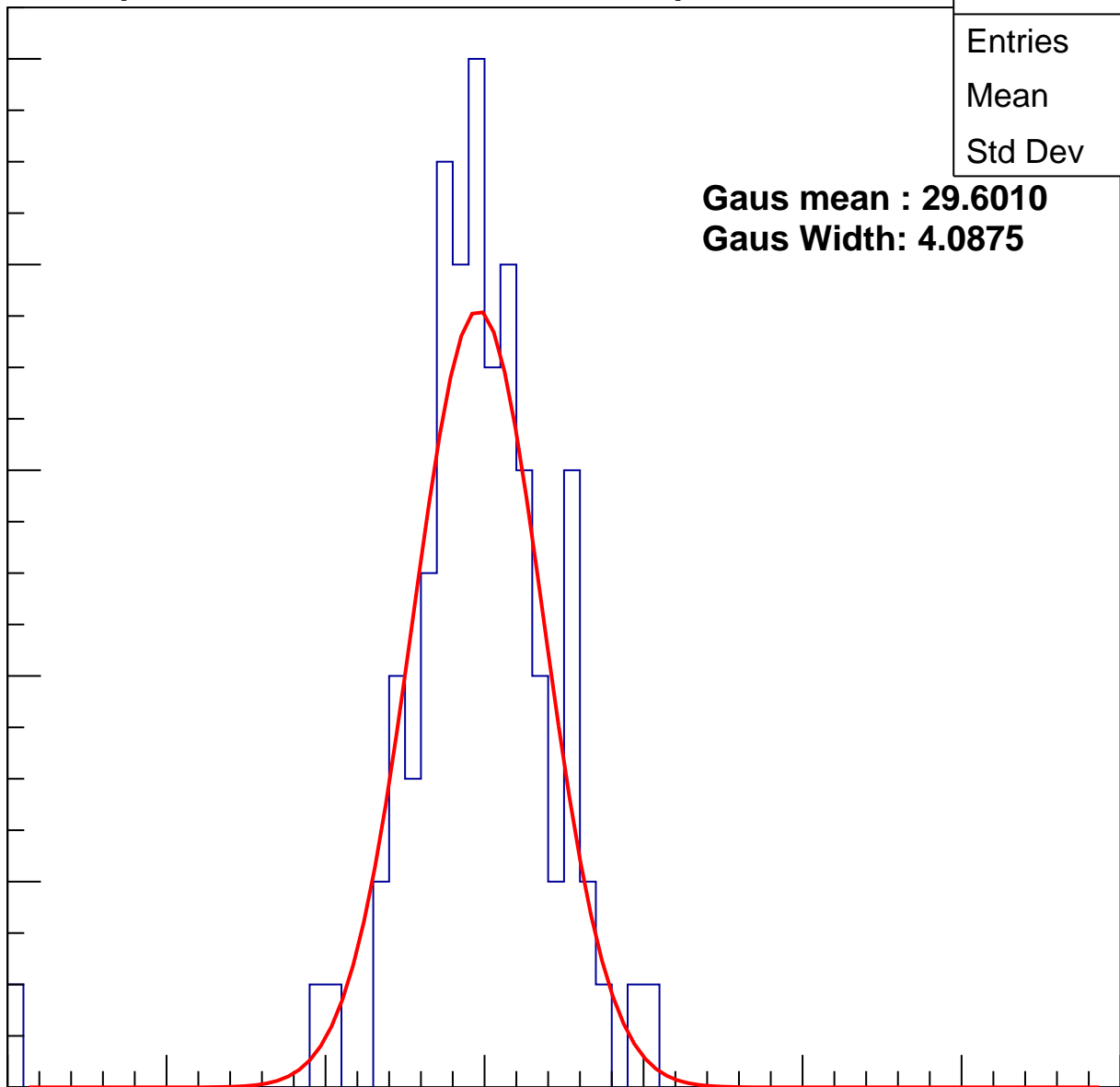
**Gaus Width: 4.0875**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U3-ch57, adc1

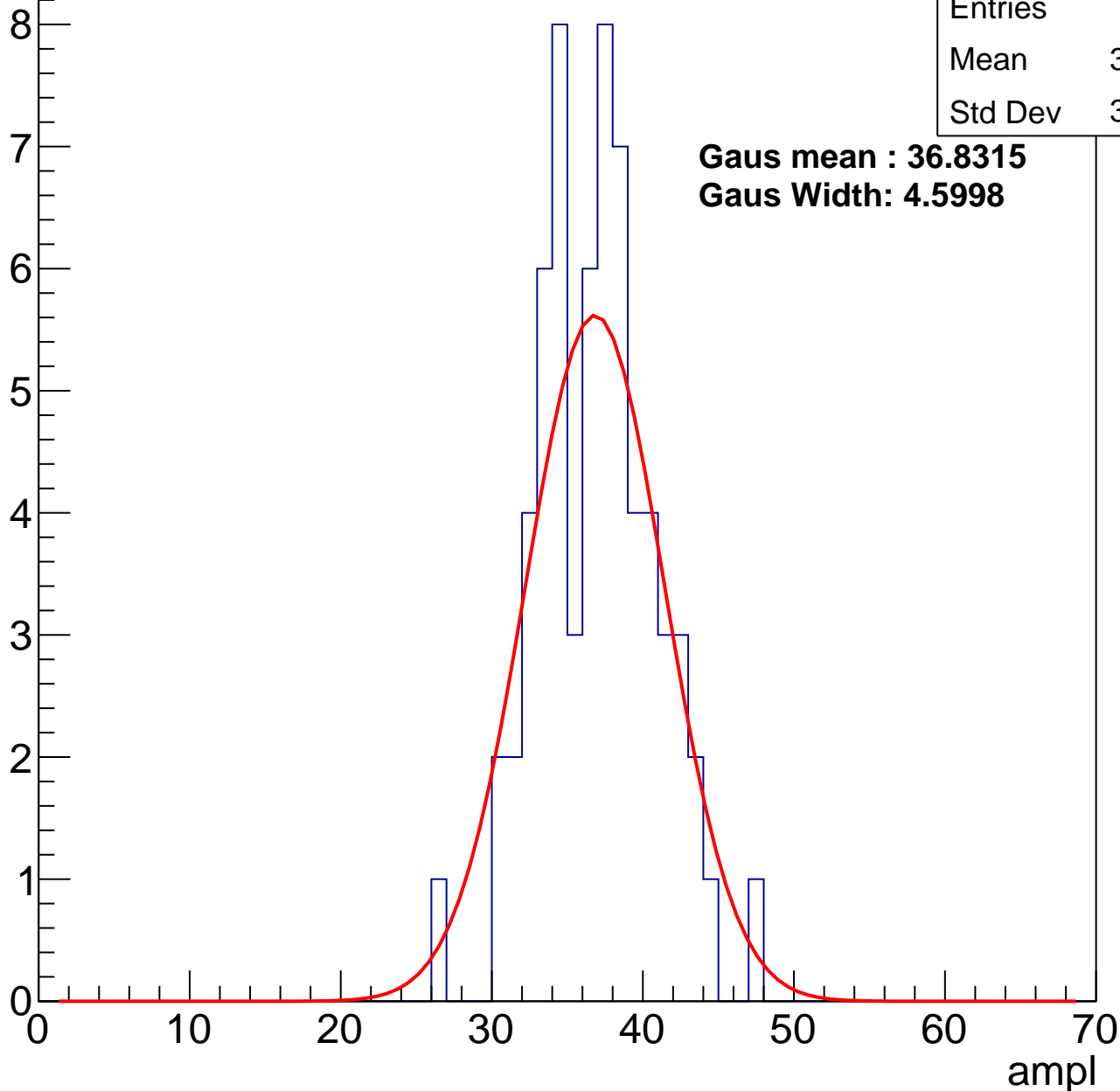
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	36.48
Std Dev	3.848

**Gaus mean : 36.8315**

**Gaus Width: 4.5998**



# B1L101S, U3-ch57, adc2

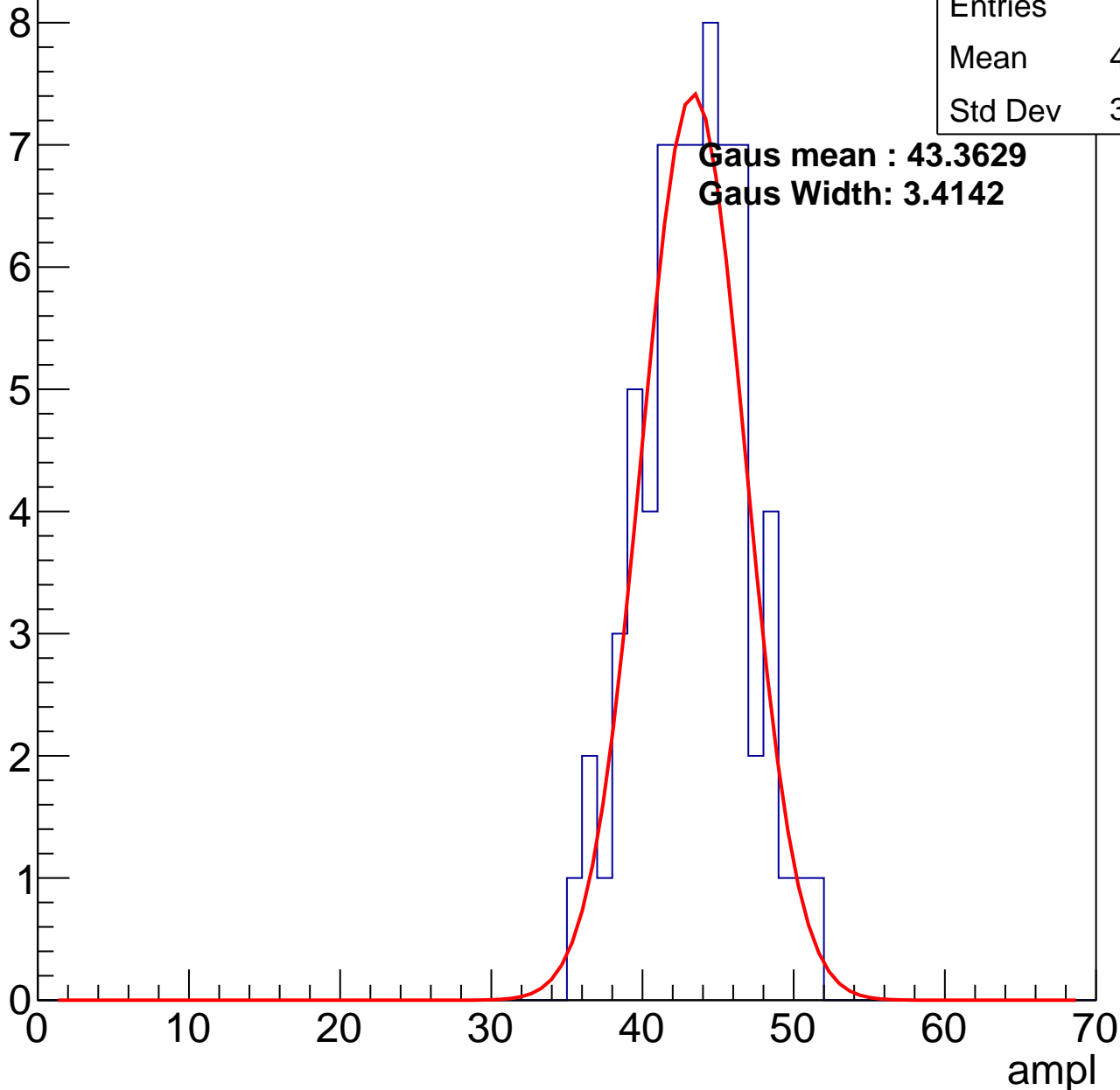
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	42.94
Std Dev	3.438

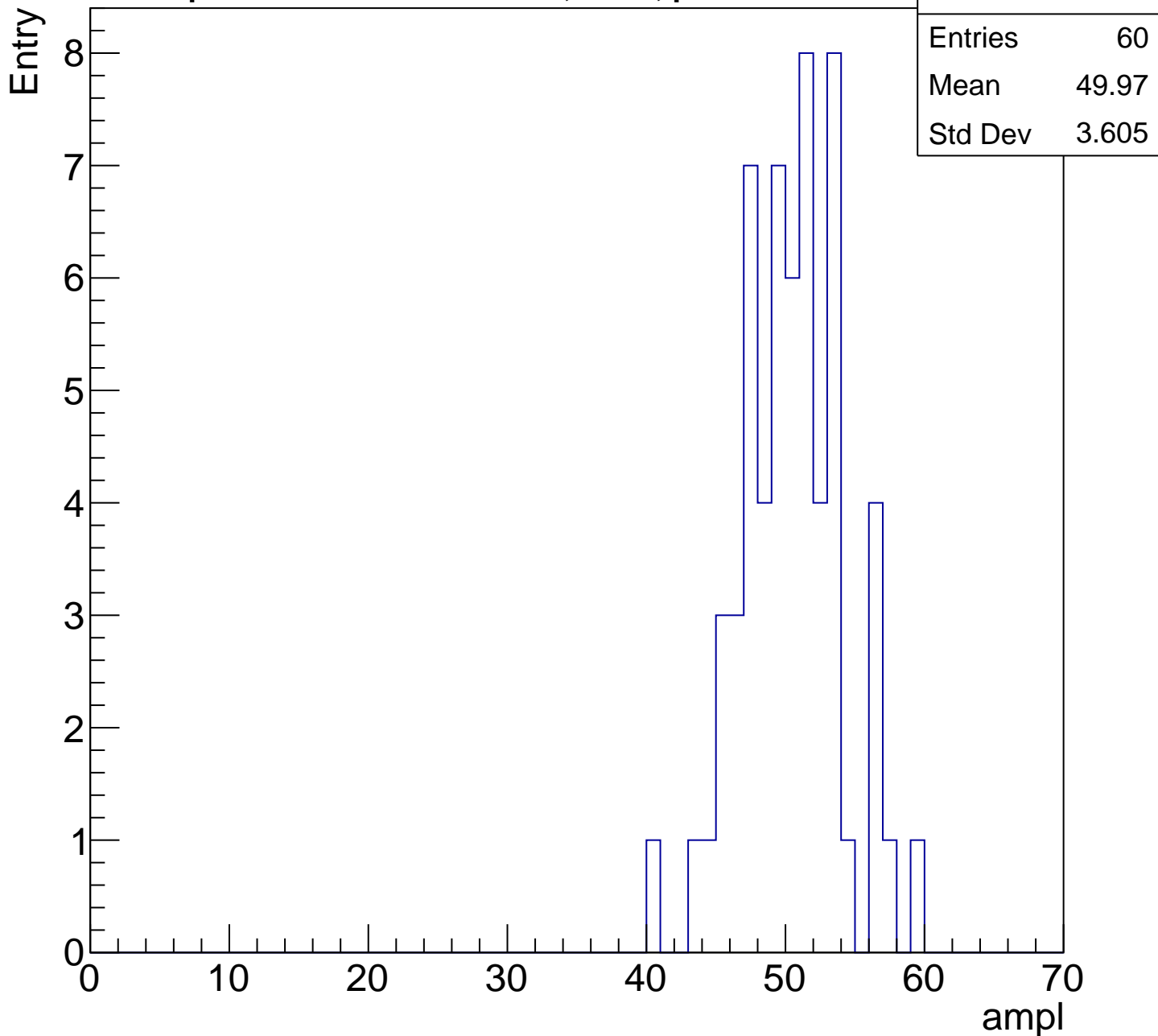
**Gaus mean : 43.3629**

**Gaus Width: 3.4142**



# B1L101S, U3-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

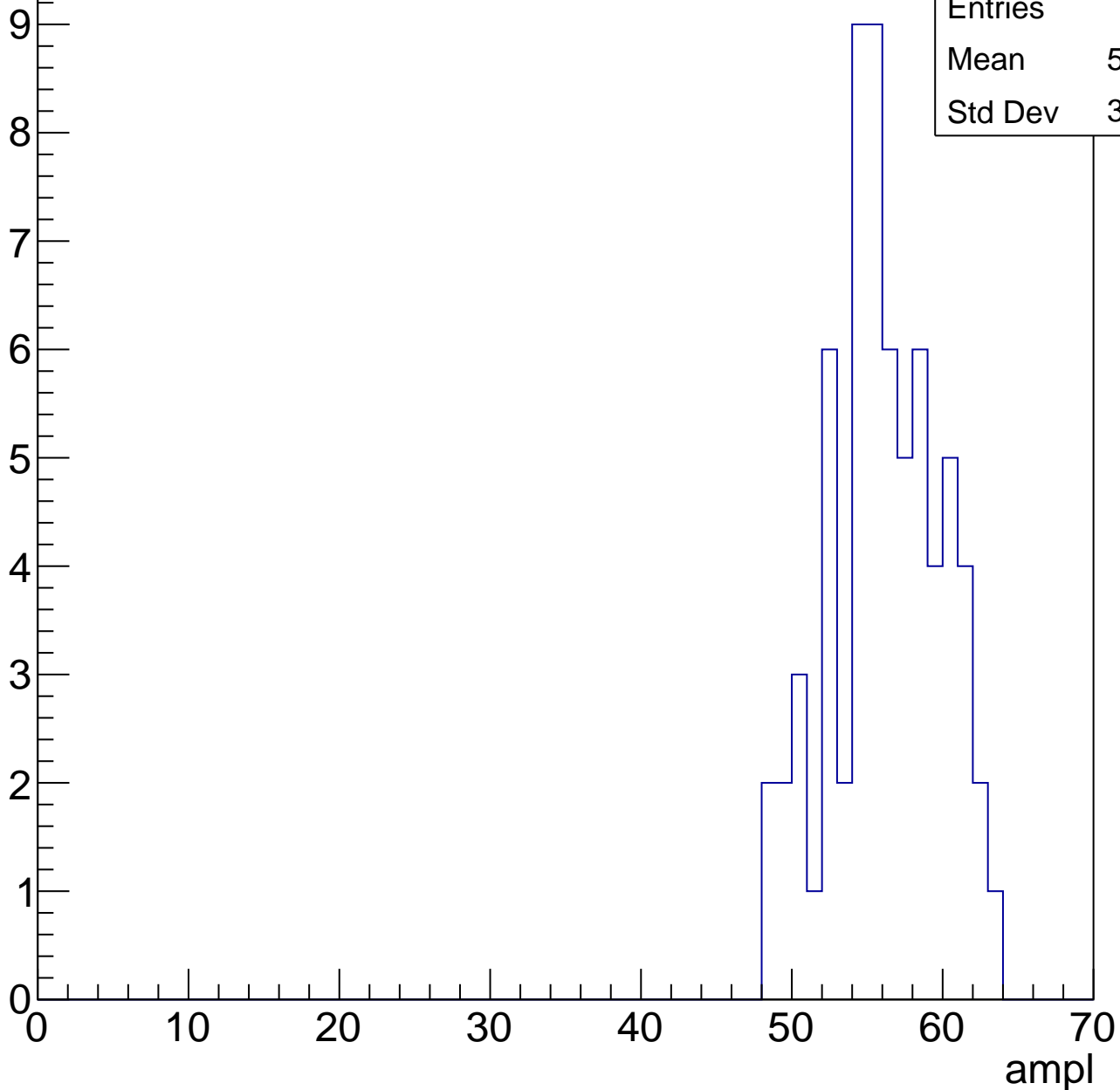


# B1L101S, U3-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	55.67
Std Dev	3.617

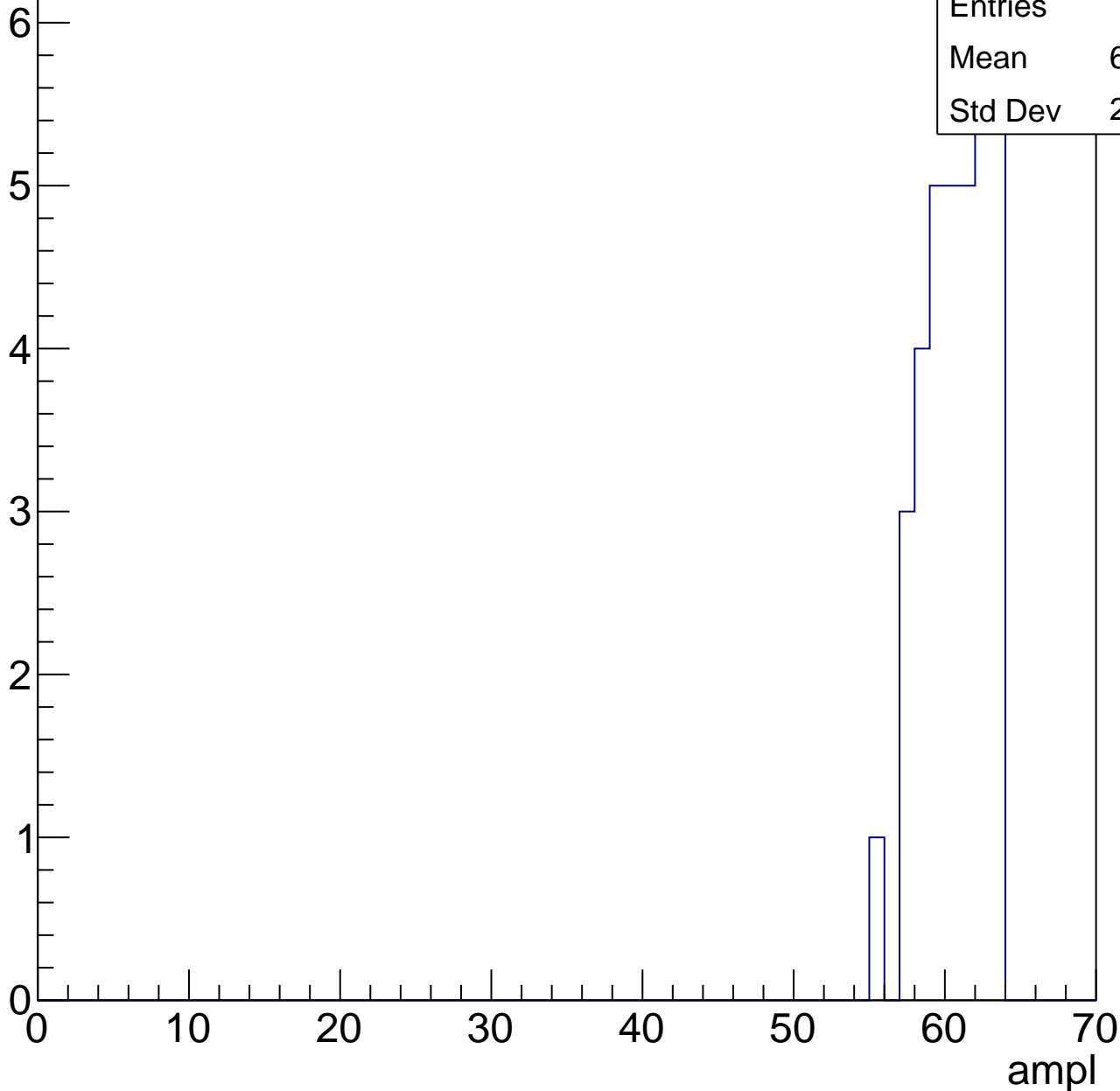


# B1L101S, U3-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

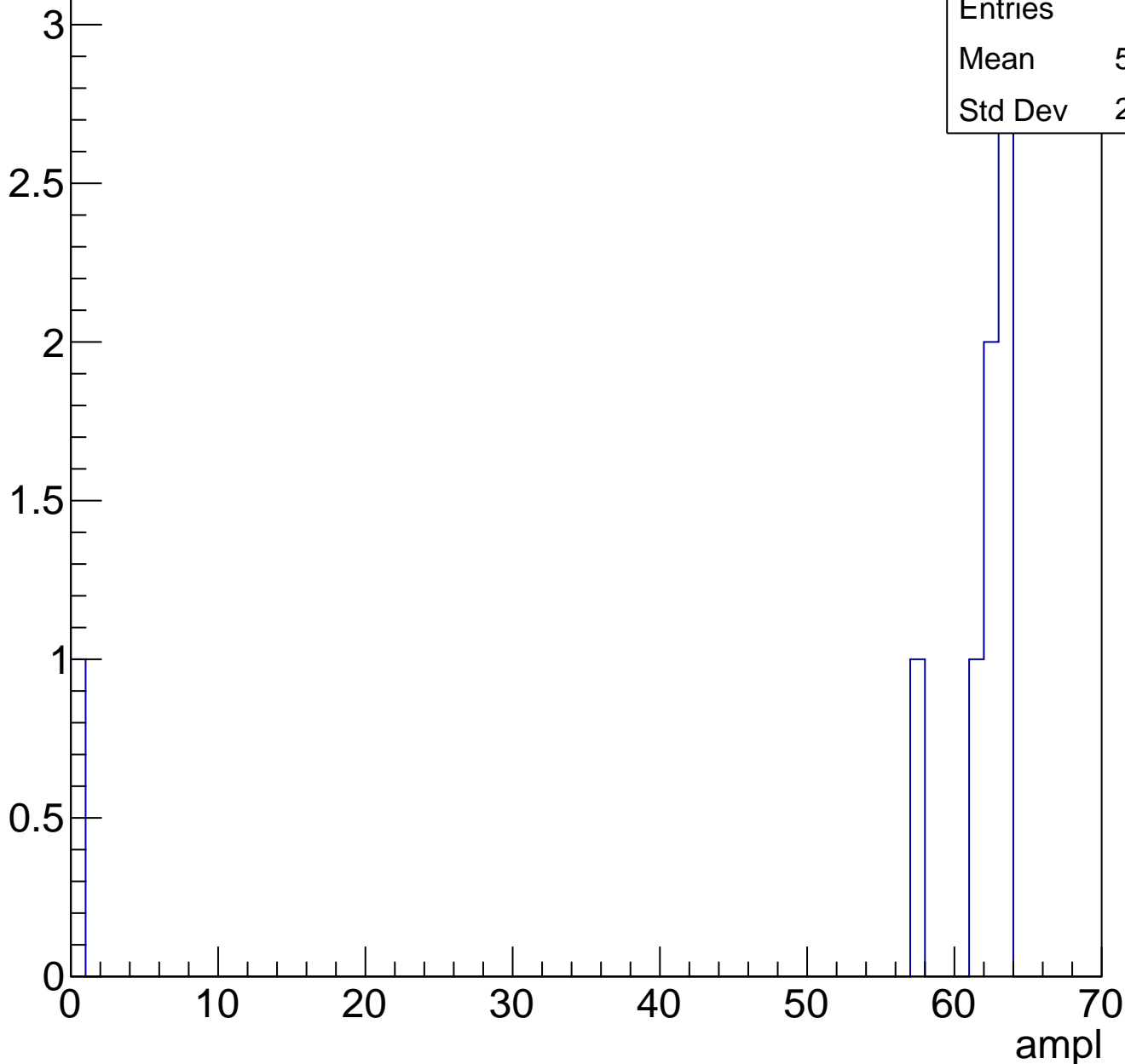
Entries	35
Mean	60.23
Std Dev	2.099



# B1L101S, U3-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch58, adc0

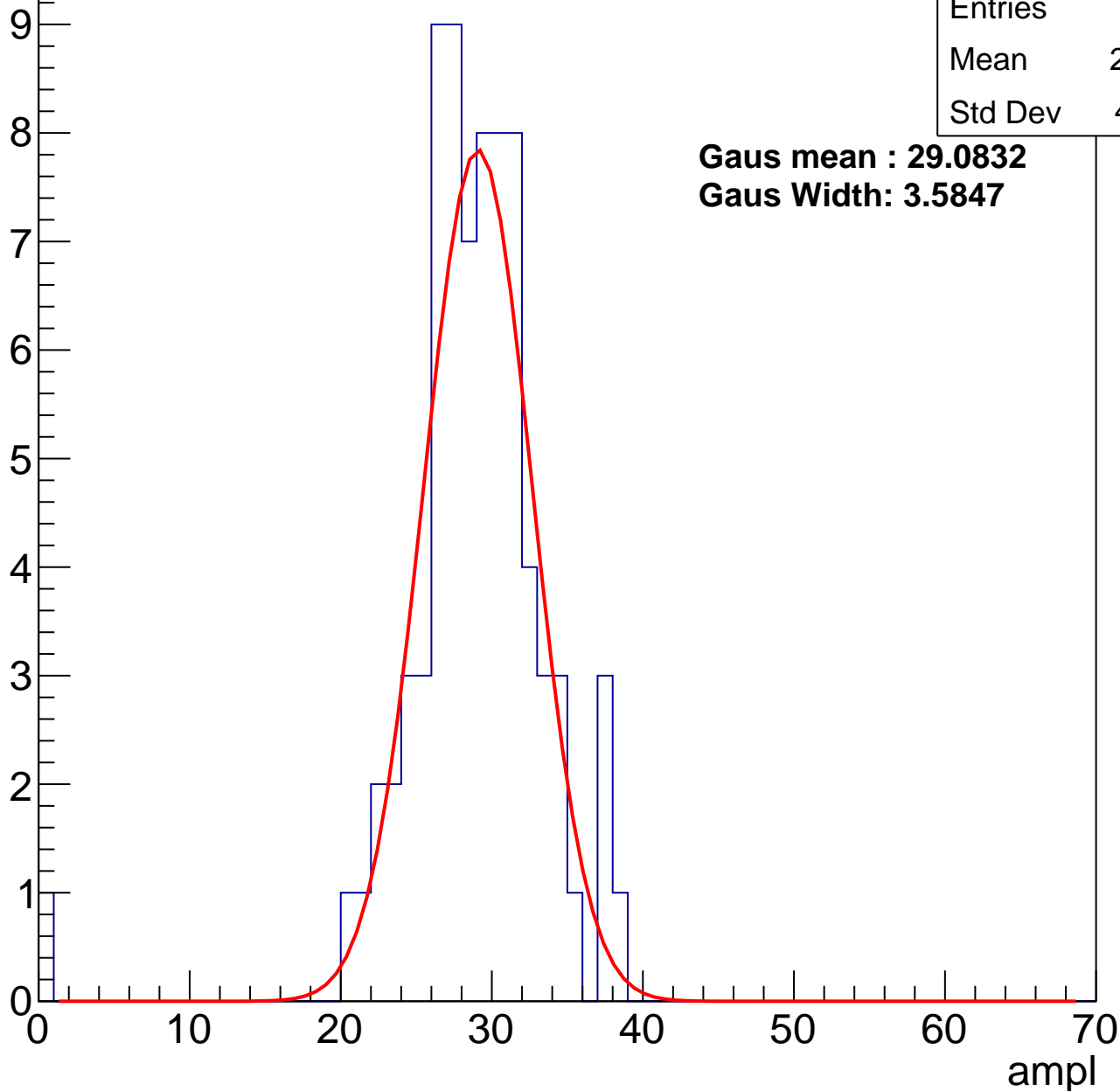
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	28.36
Std Dev	4.941

**Gaus mean : 29.0832**

**Gaus Width: 3.5847**



# B1L101S, U3-ch58, adc1

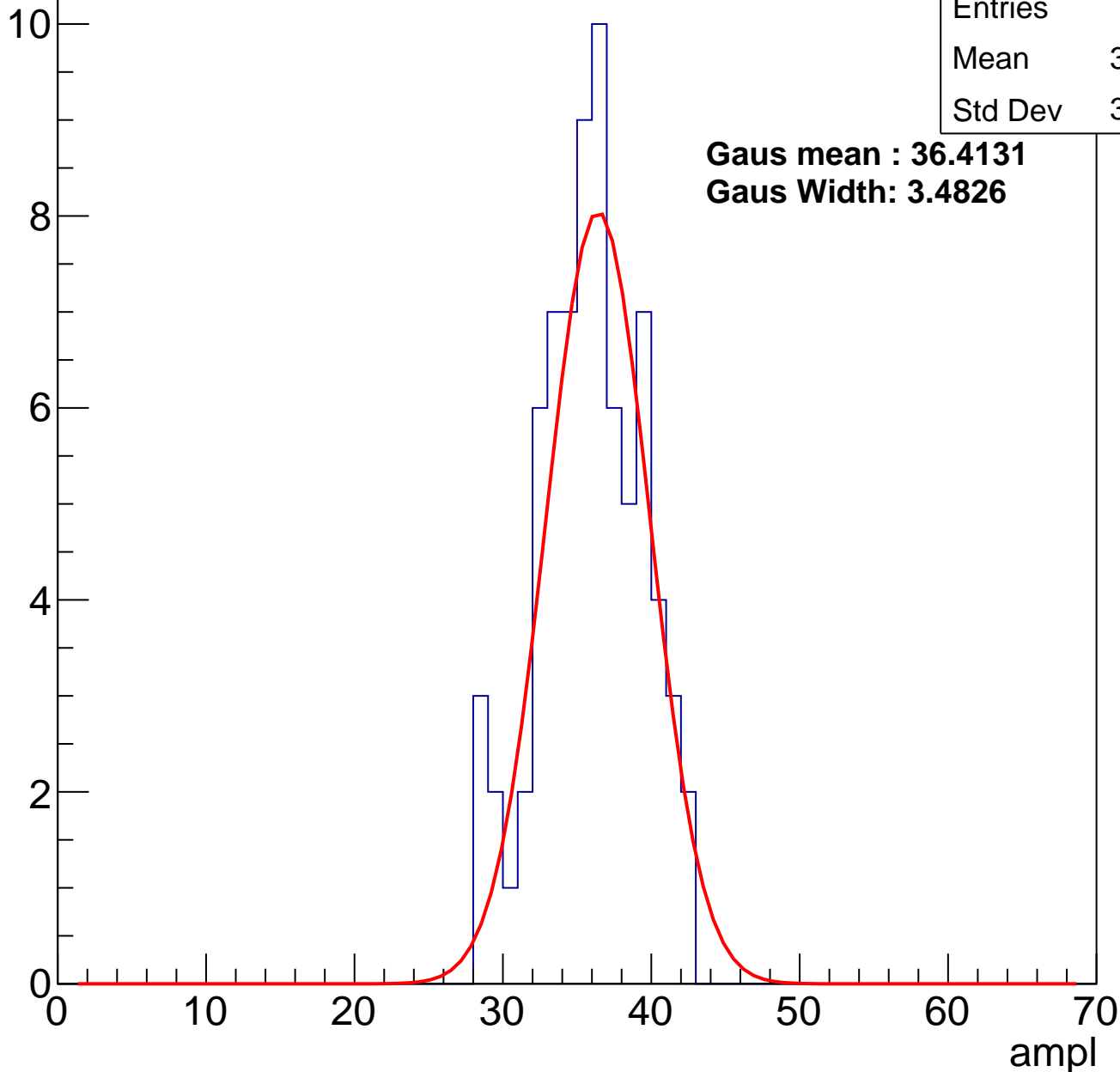
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	74
Mean	35.43
Std Dev	3.386

**Gaus mean : 36.4131**

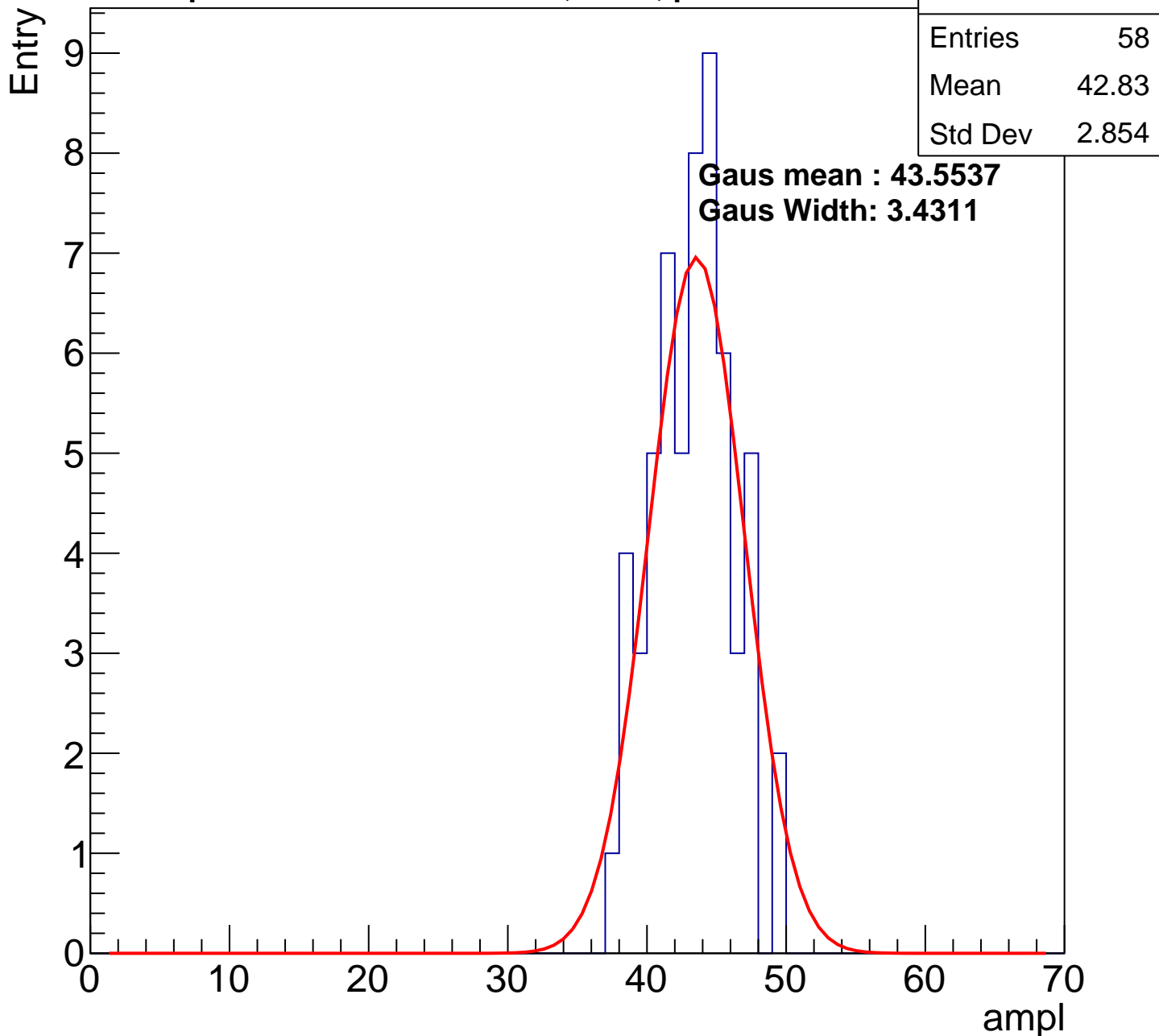
**Gaus Width: 3.4826**

Entry



# B1L101S, U3-ch58, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

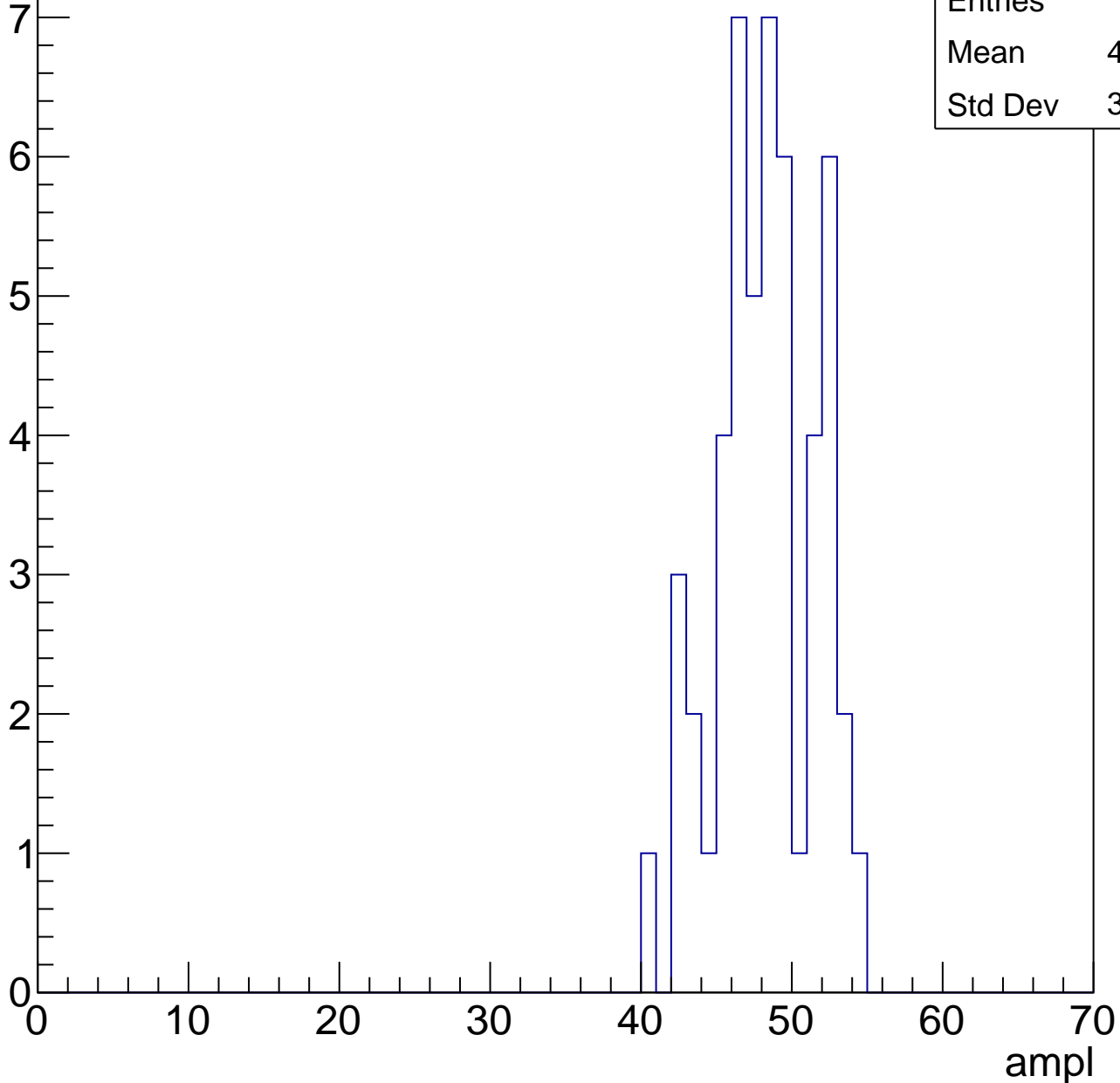


# B1L101S, U3-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	47.78
Std Dev	3.264

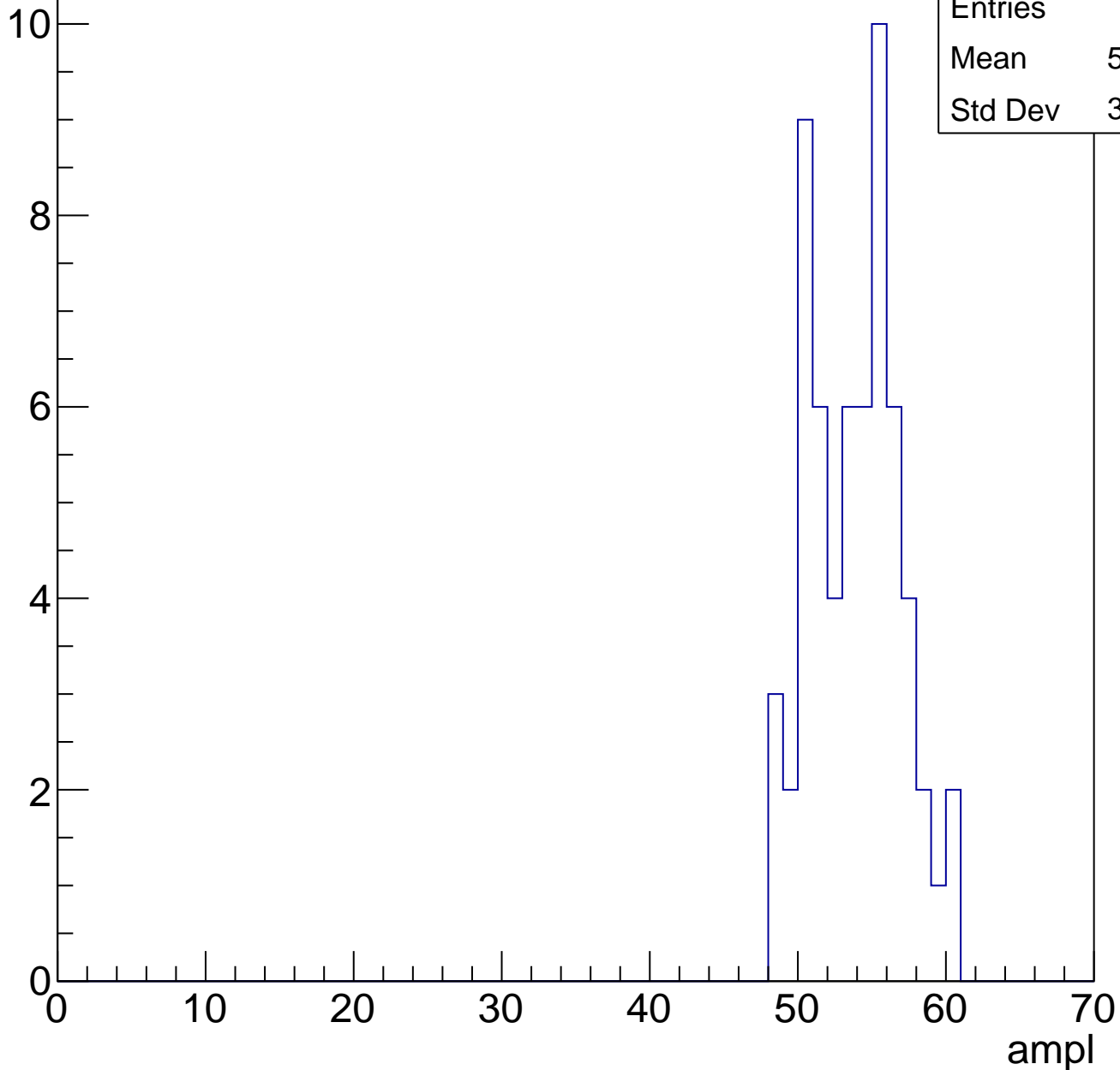


# B1L101S, U3-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	61
Mean	53.39
Std Dev	3.015

Entry

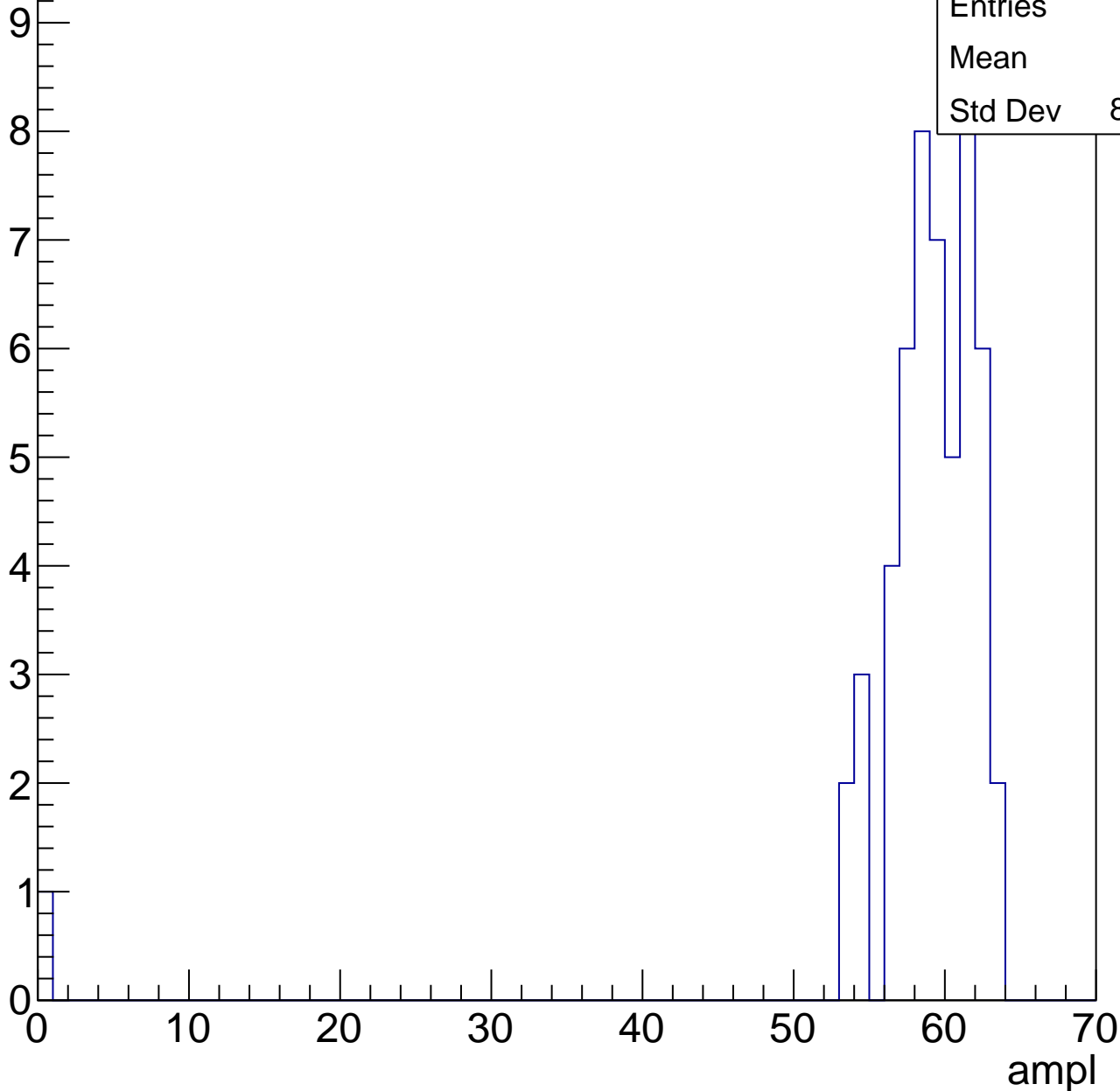


# B1L101S, U3-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

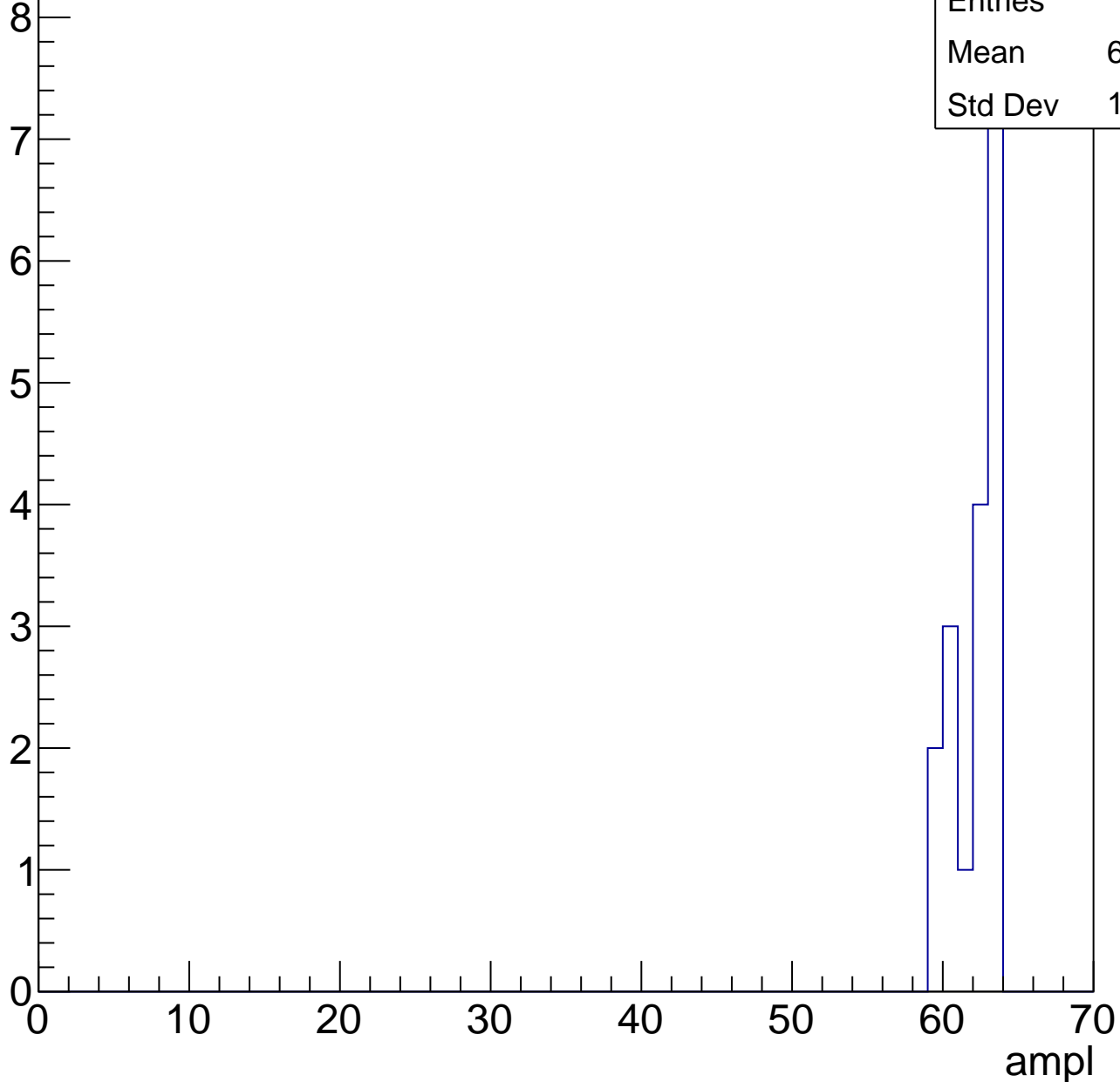
Entries	53
Mean	57.7
Std Dev	8.393



# B1L101S, U3-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch59, adc0

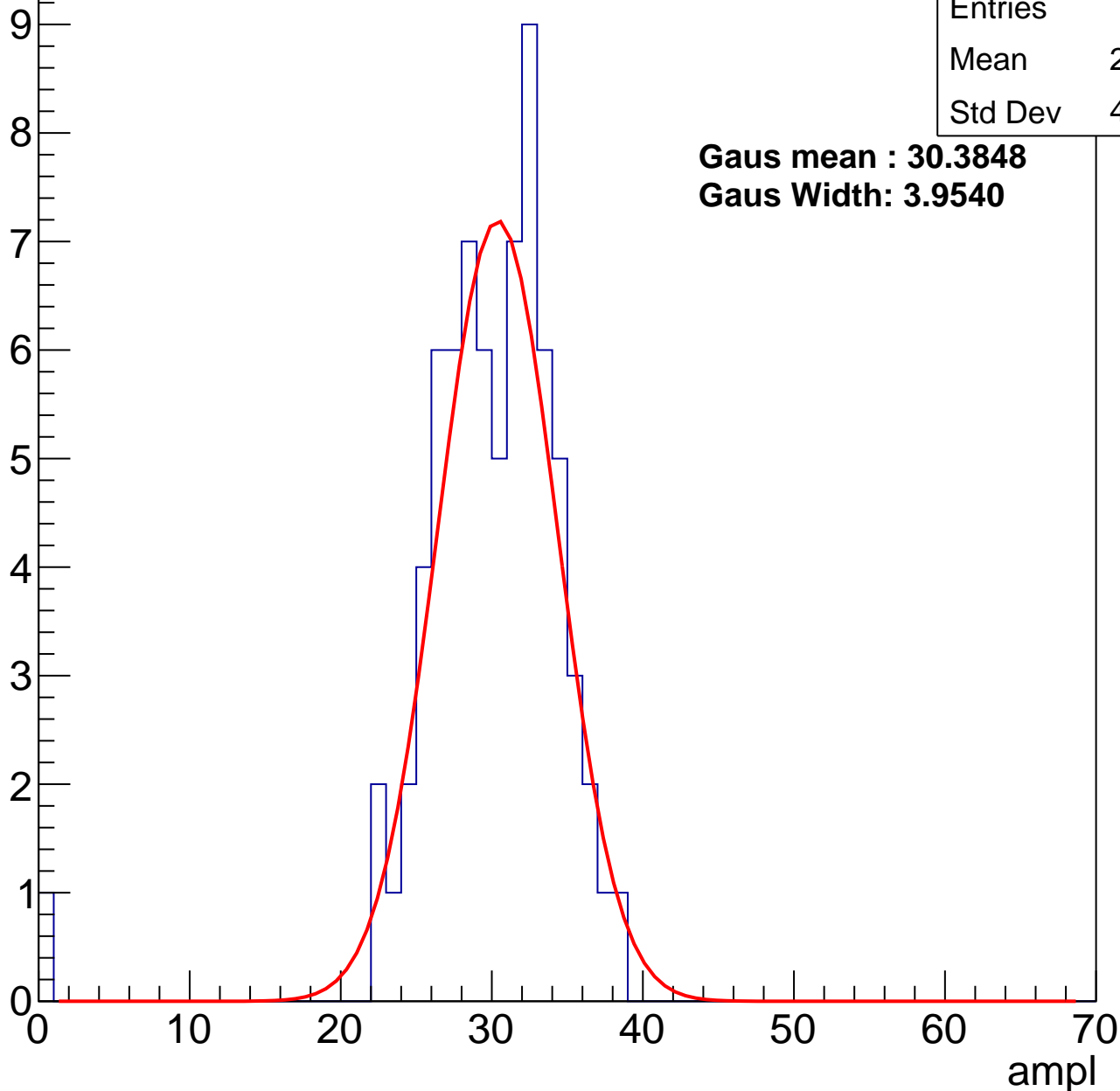
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	29.43
Std Dev	4.995

**Gaus mean : 30.3848**

**Gaus Width: 3.9540**



# B1L101S, U3-ch59, adc1

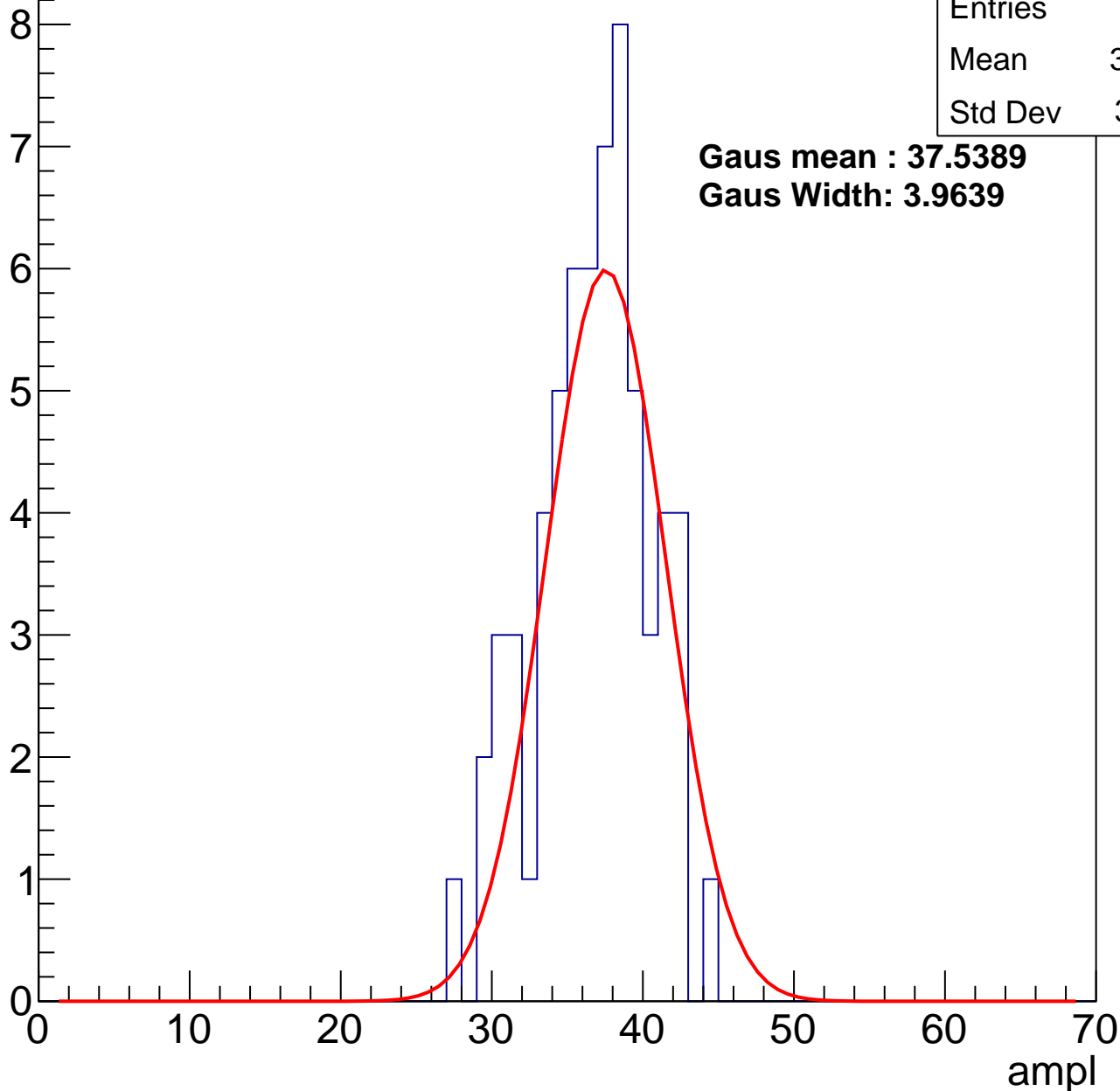
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	36.22
Std Dev	3.731

**Gaus mean : 37.5389**

**Gaus Width: 3.9639**



# B1L101S, U3-ch59, adc2

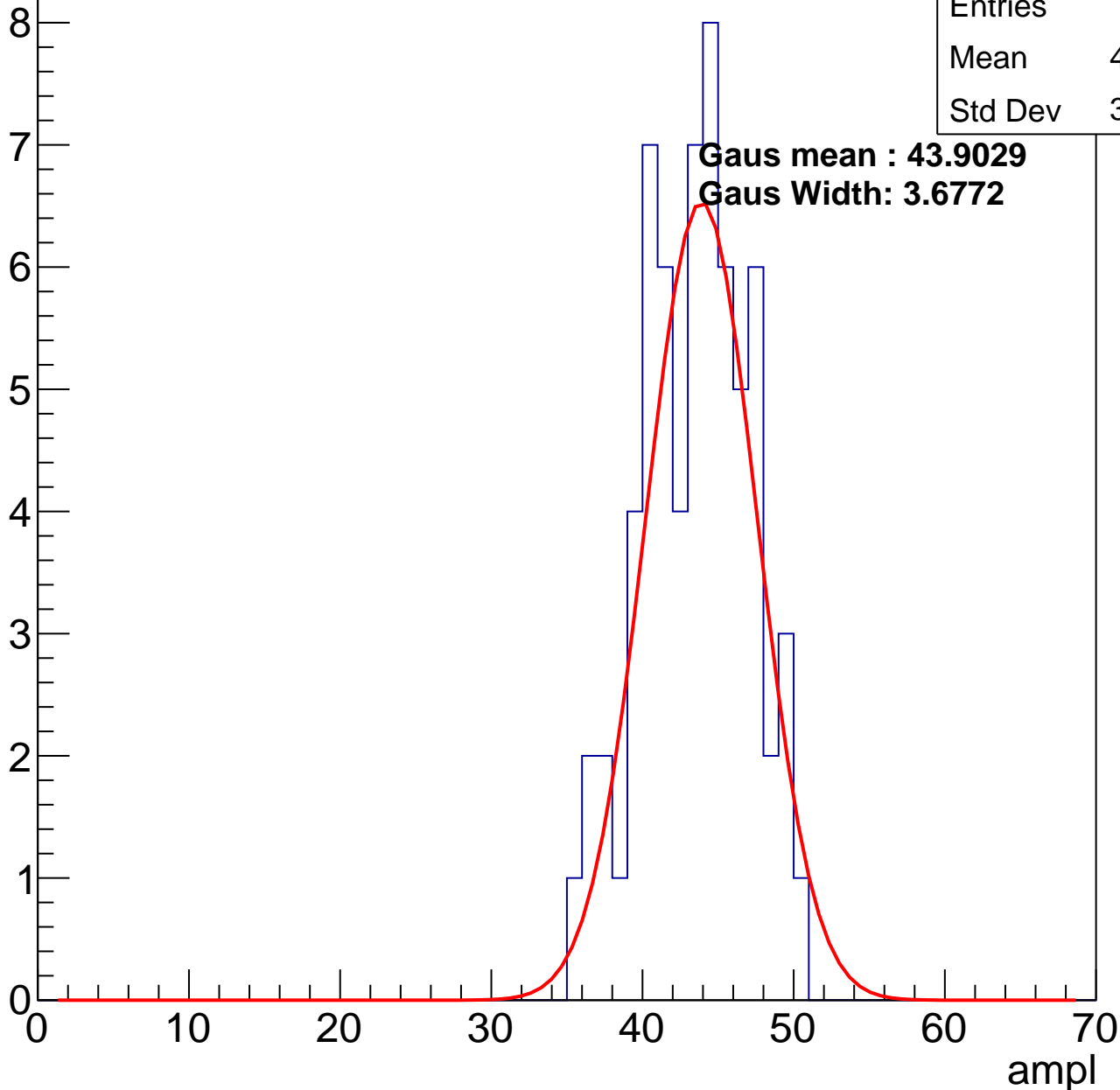
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	43.03
Std Dev	3.495

**Gaus mean : 43.9029**

**Gaus Width: 3.6772**

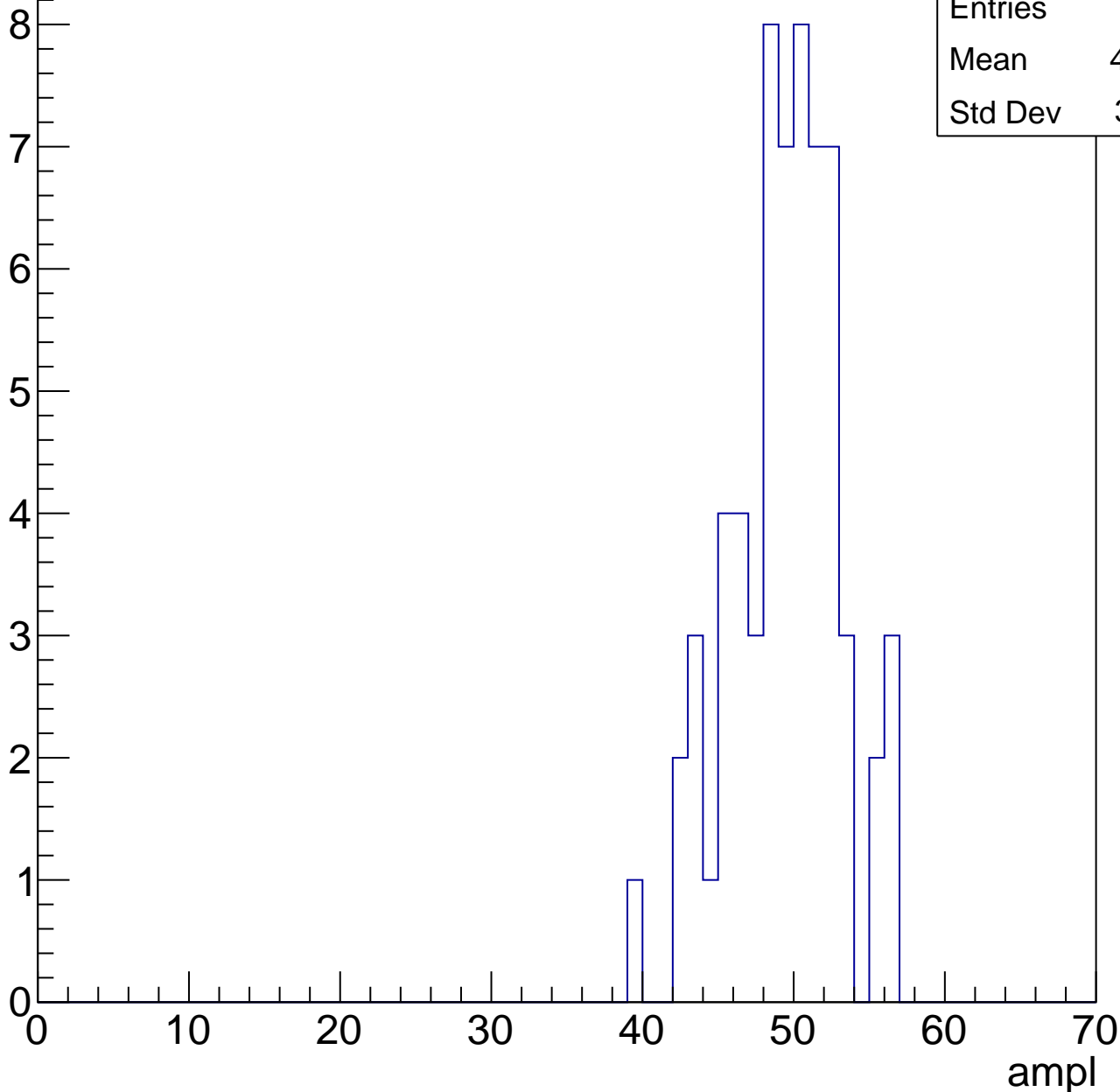


# B1L101S, U3-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

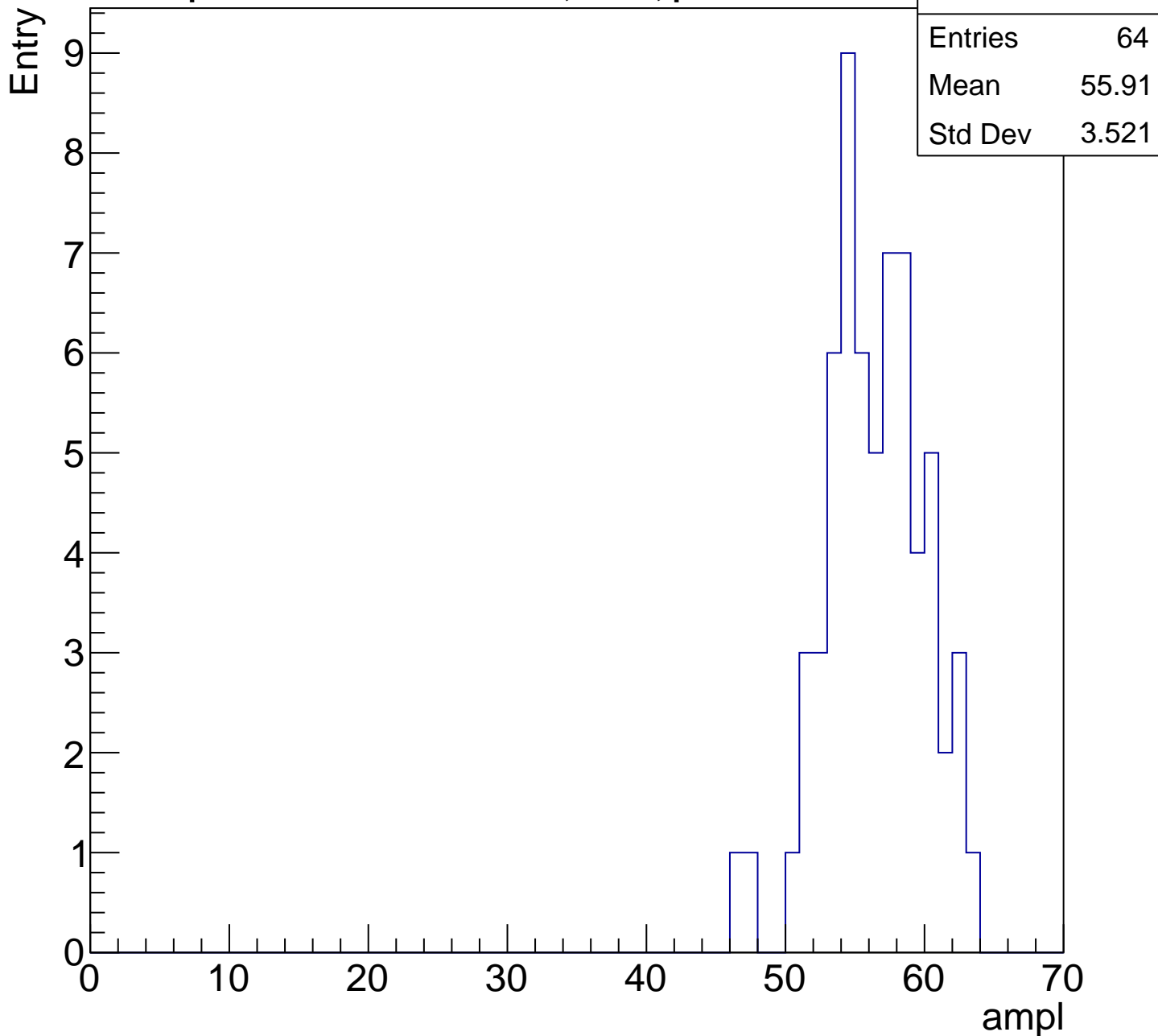
Entry

Entries	63
Mean	48.98
Std Dev	3.601



# B1L101S, U3-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	47
Mean	58.62
Std Dev	9.033

ampl

0

10

20

30

40

50

60

70

# B1L101S, U3-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0



# B1L101S, U3-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	62
Std Dev	0

ampl

# B1L101S, U3-ch60, adc0

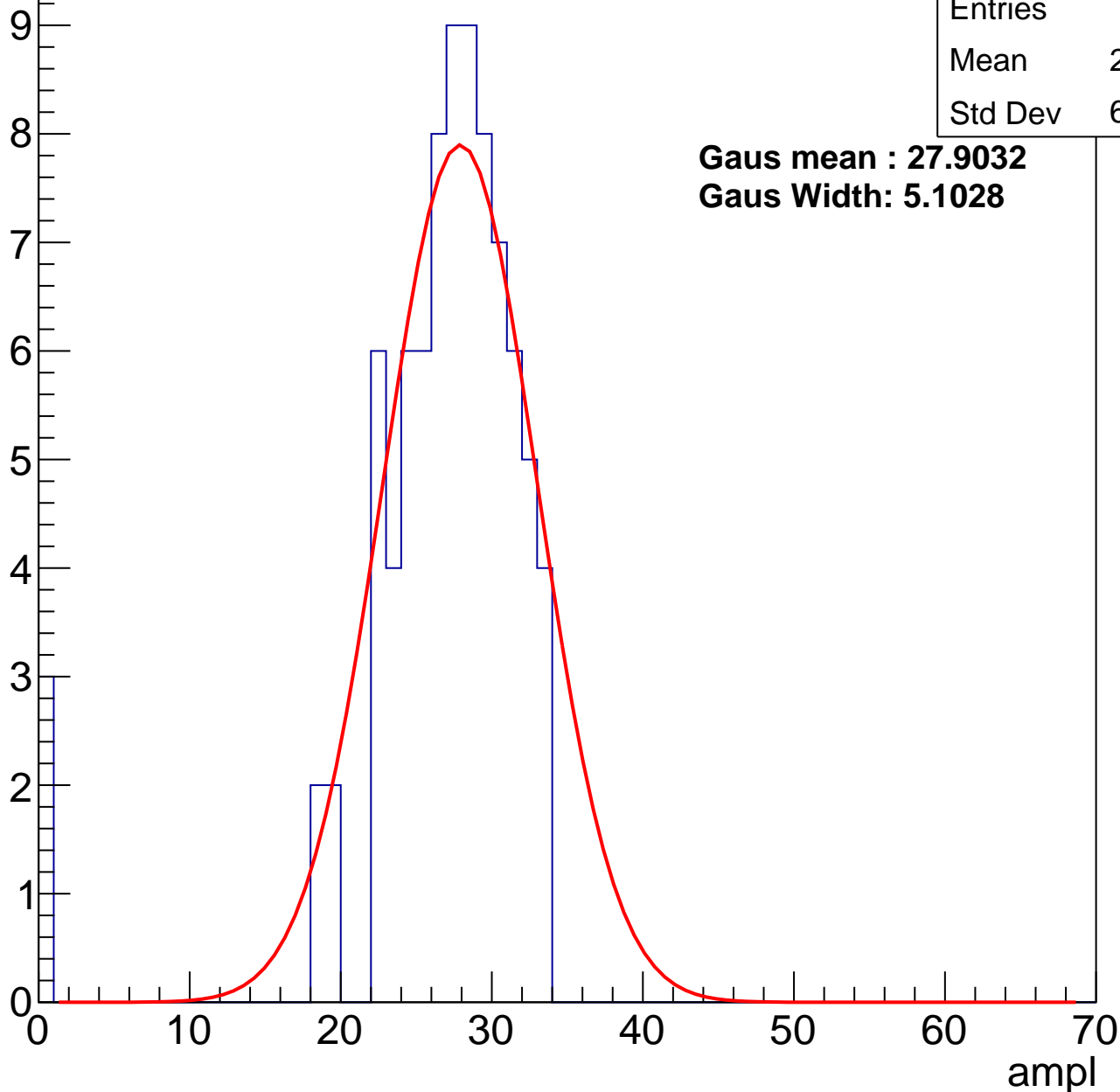
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	85
Mean	26.06
Std Dev	6.108

**Gaus mean : 27.9032**

**Gaus Width: 5.1028**



# B1L101S, U3-ch60, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	67
Mean	34.91
Std Dev	3.309

**Gaus mean : 34.8374**

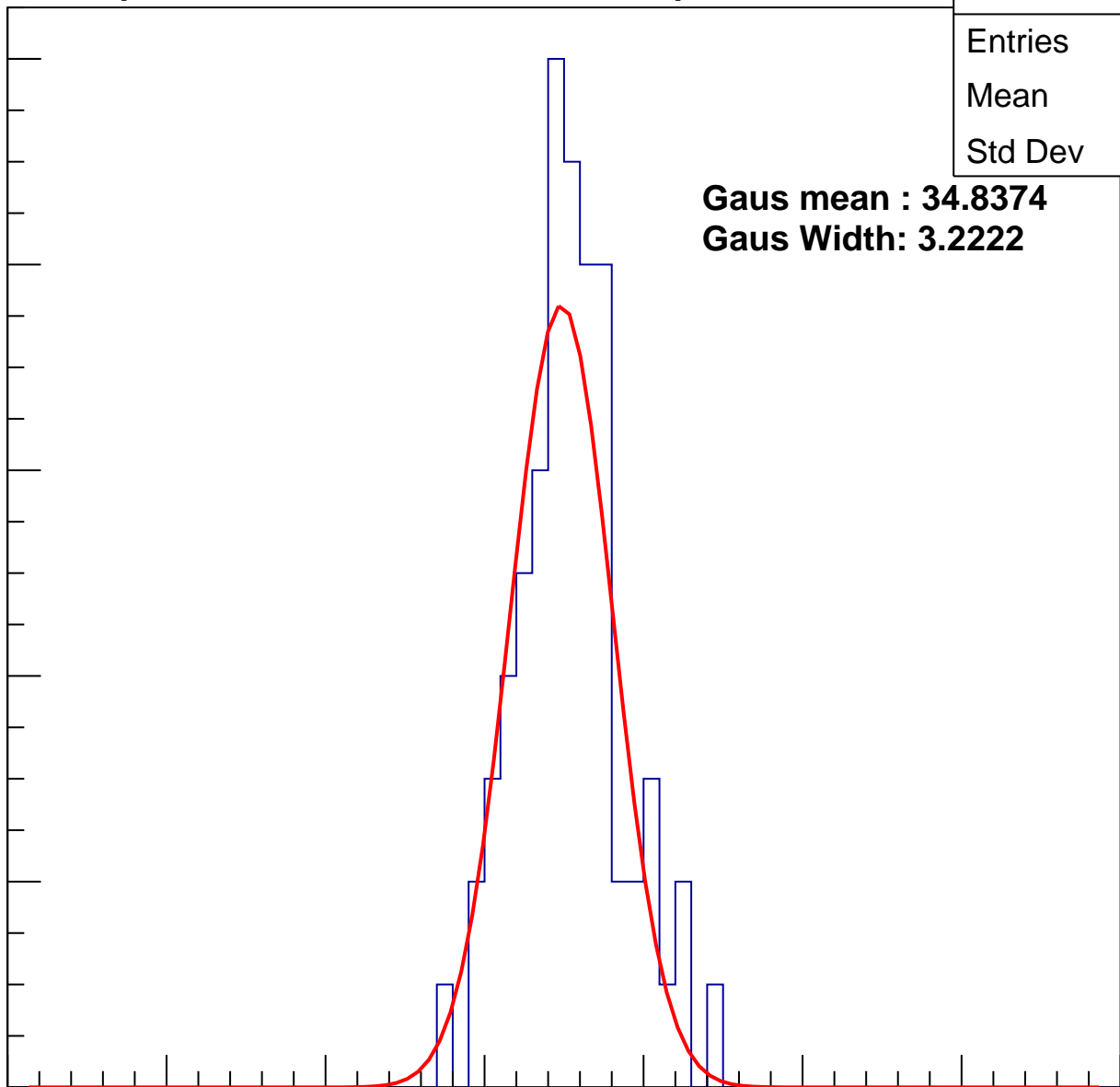
**Gaus Width: 3.2222**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U3-ch60, adc2

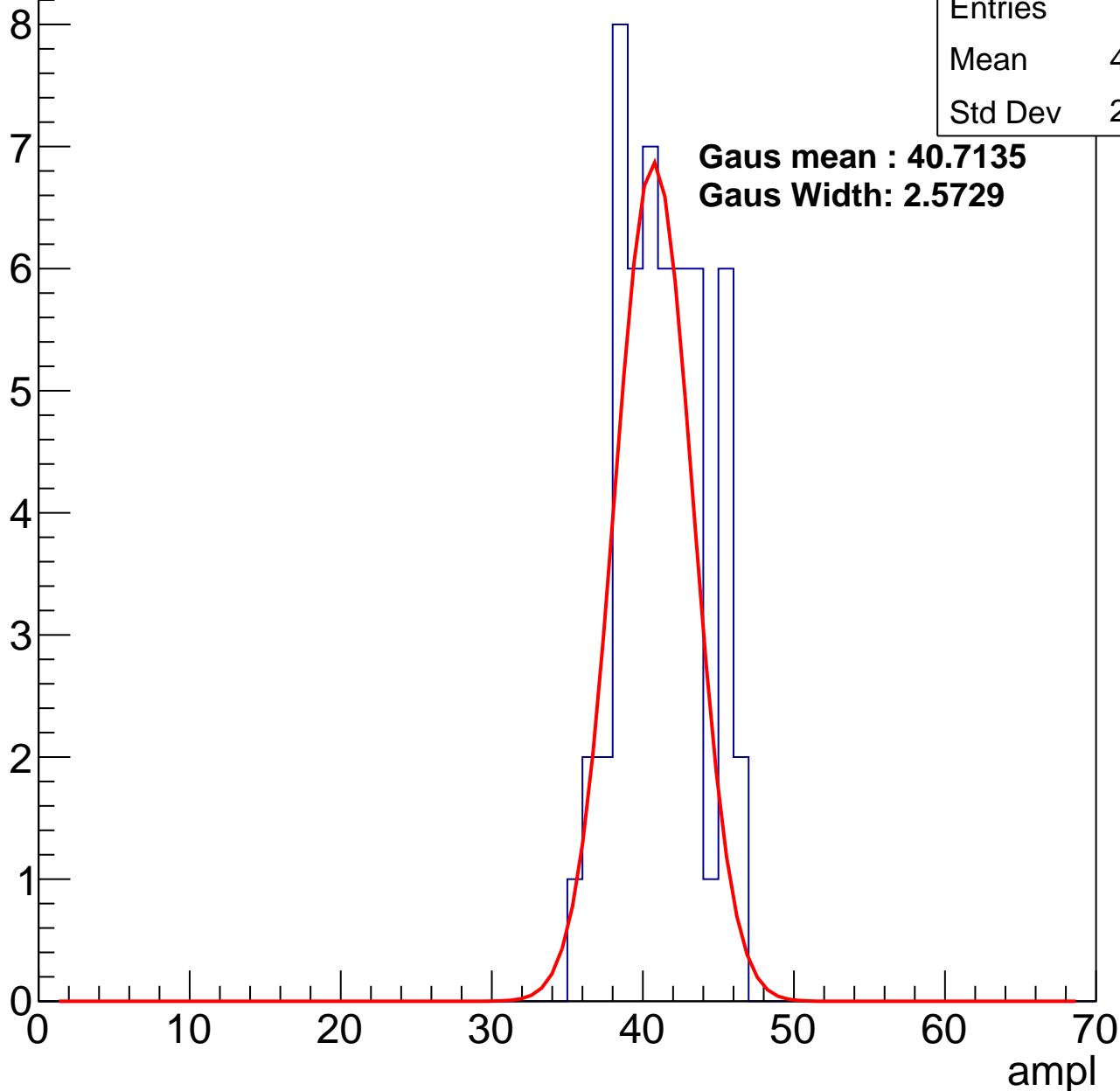
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	40.77
Std Dev	2.758

**Gaus mean : 40.7135**

**Gaus Width: 2.5729**



# B1L101S, U3-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

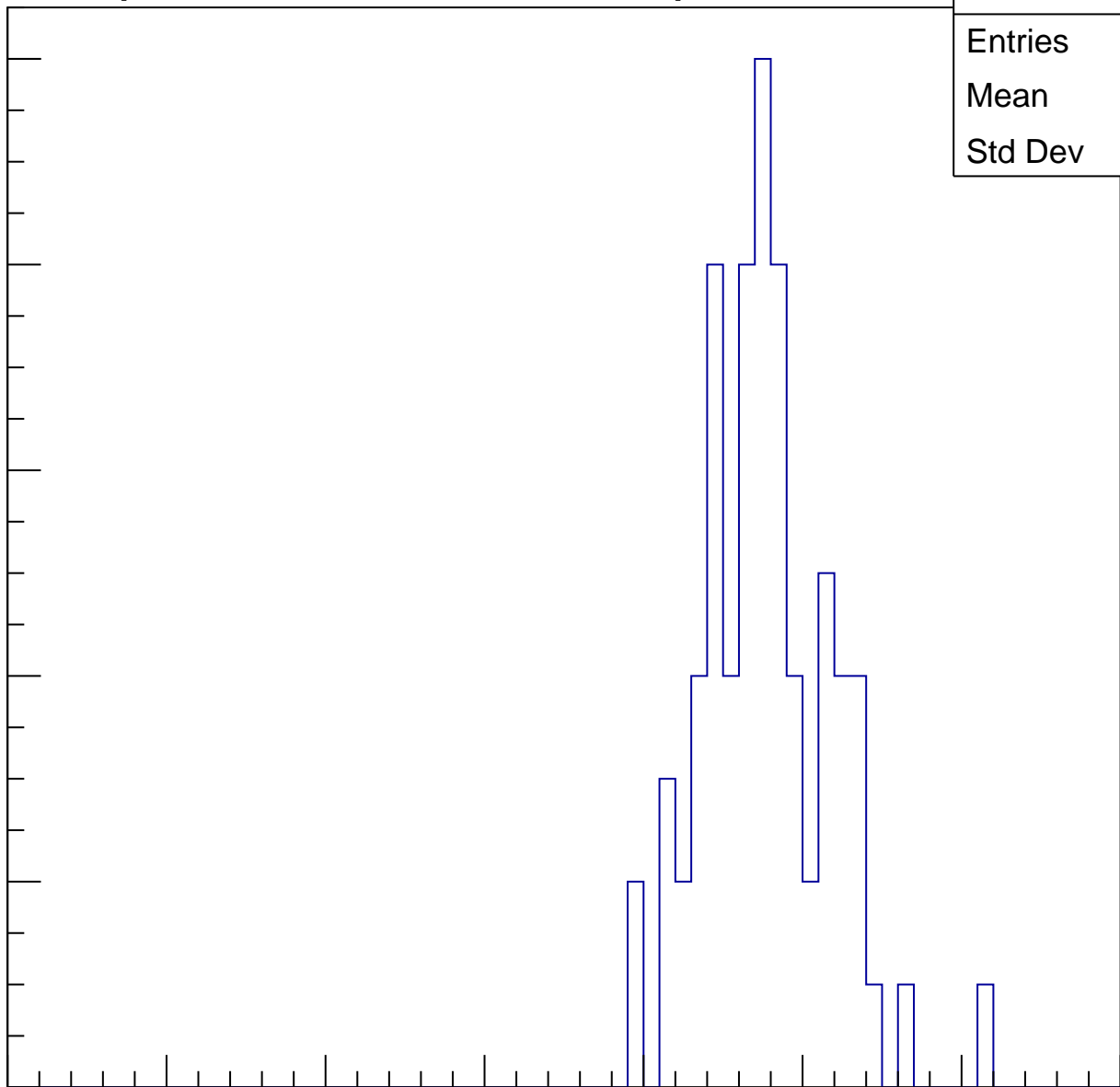
Entries	71
Mean	47.23
Std Dev	3.997

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

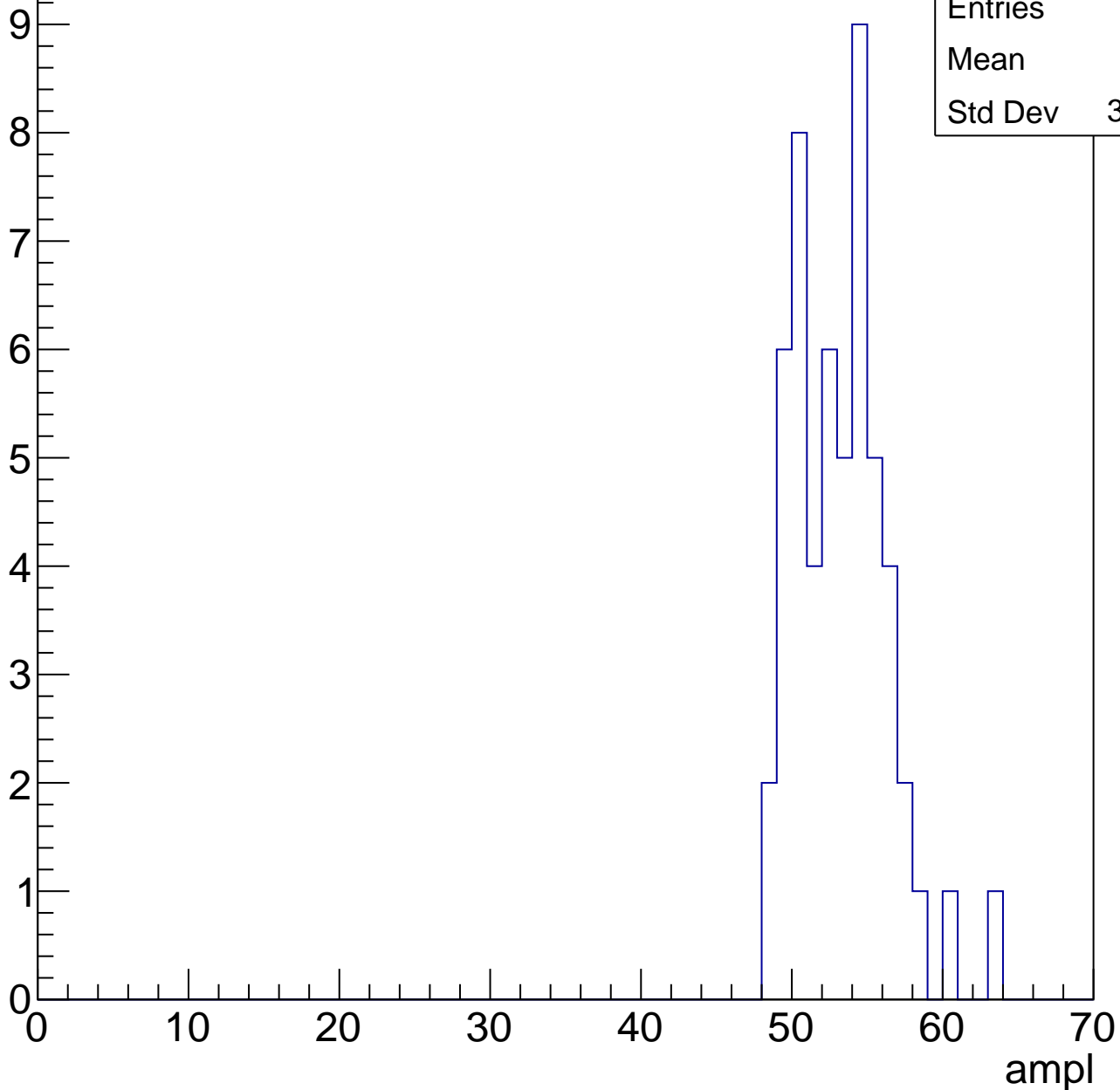


# B1L101S, U3-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

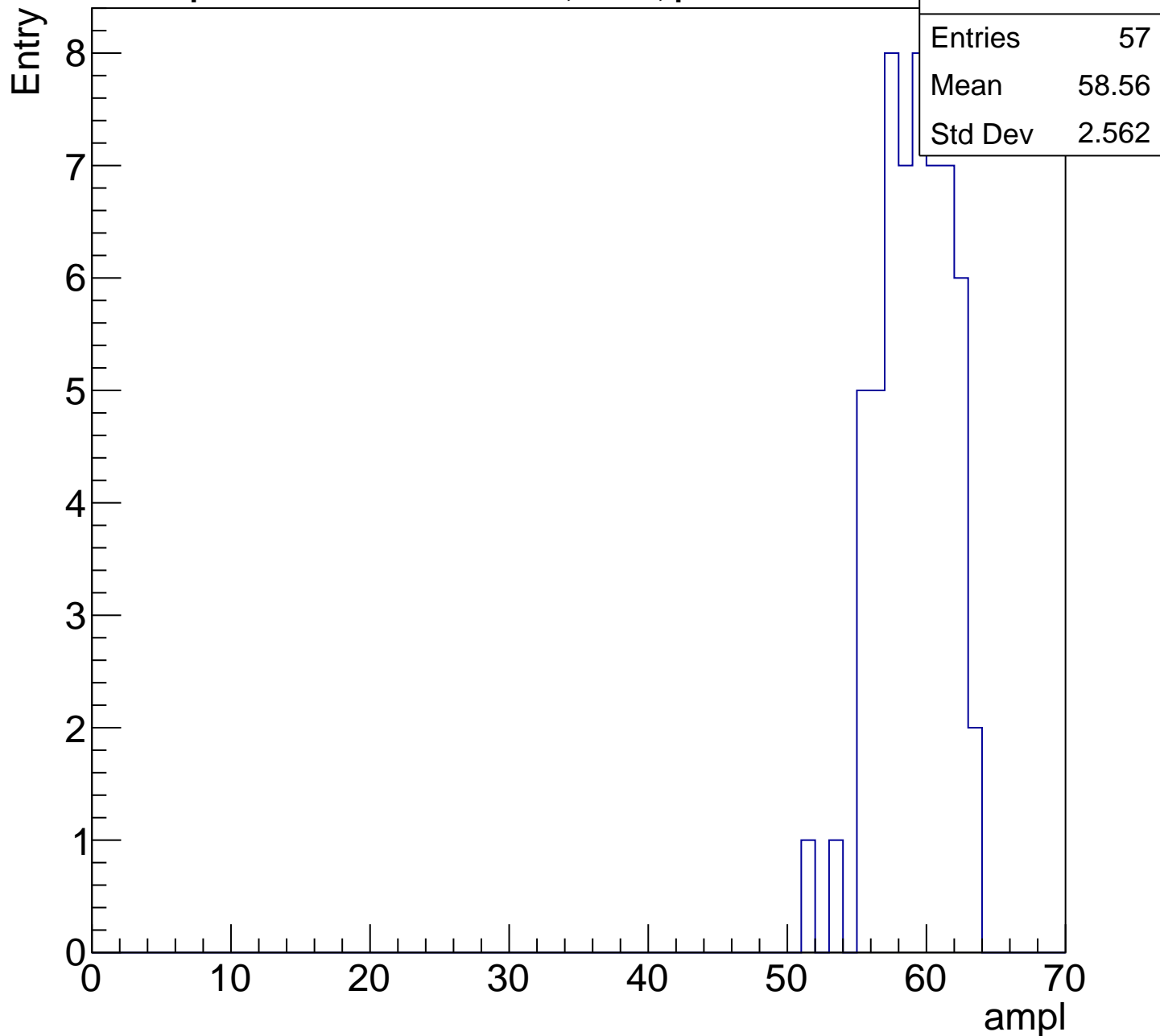
Entry

Entries	54
Mean	52.8
Std Dev	3.069



# B1L101S, U3-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

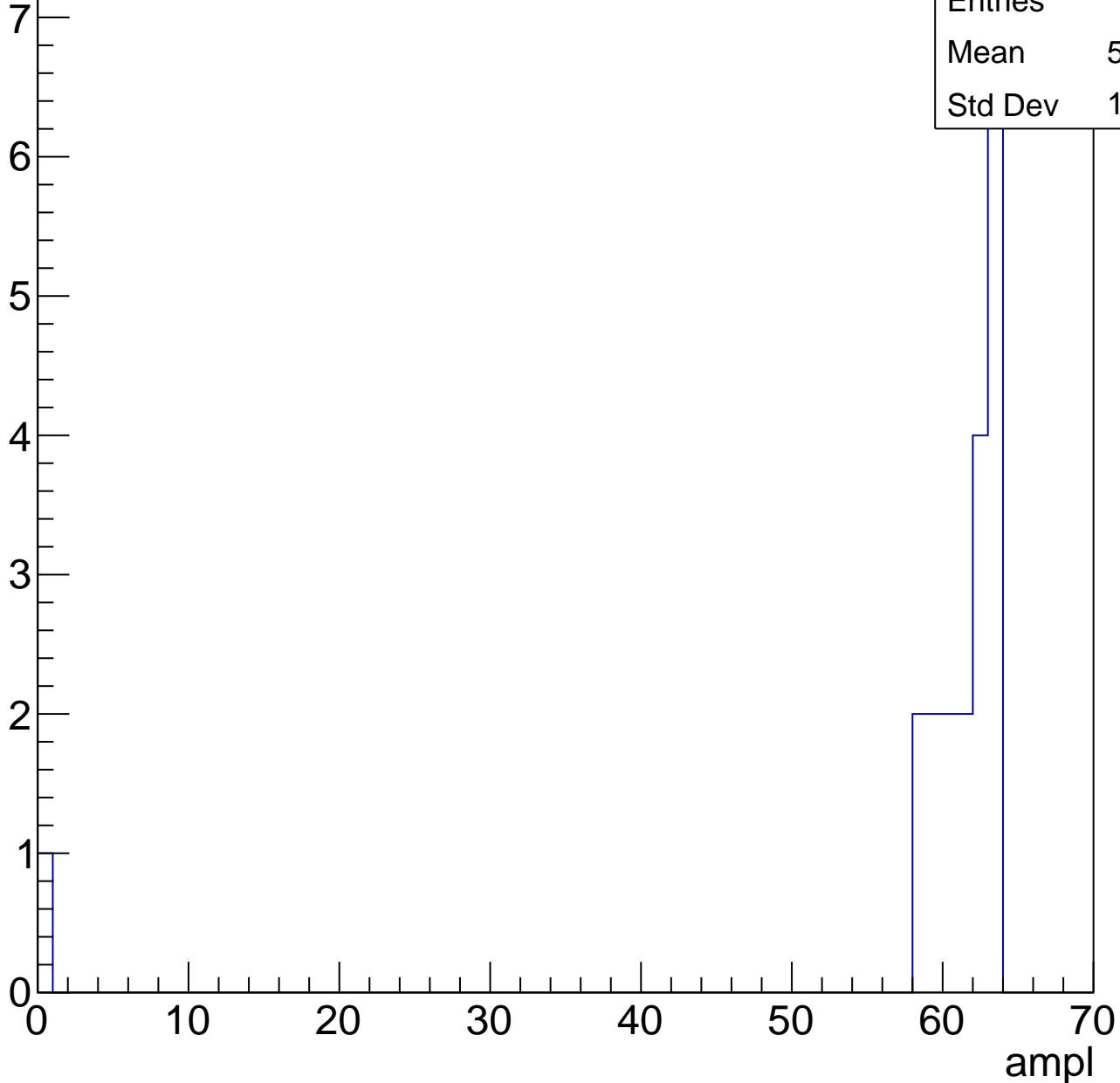


# B1L101S, U3-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	20
Mean	58.25
Std Dev	13.47





# B1L101S, U3-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch61, adc0

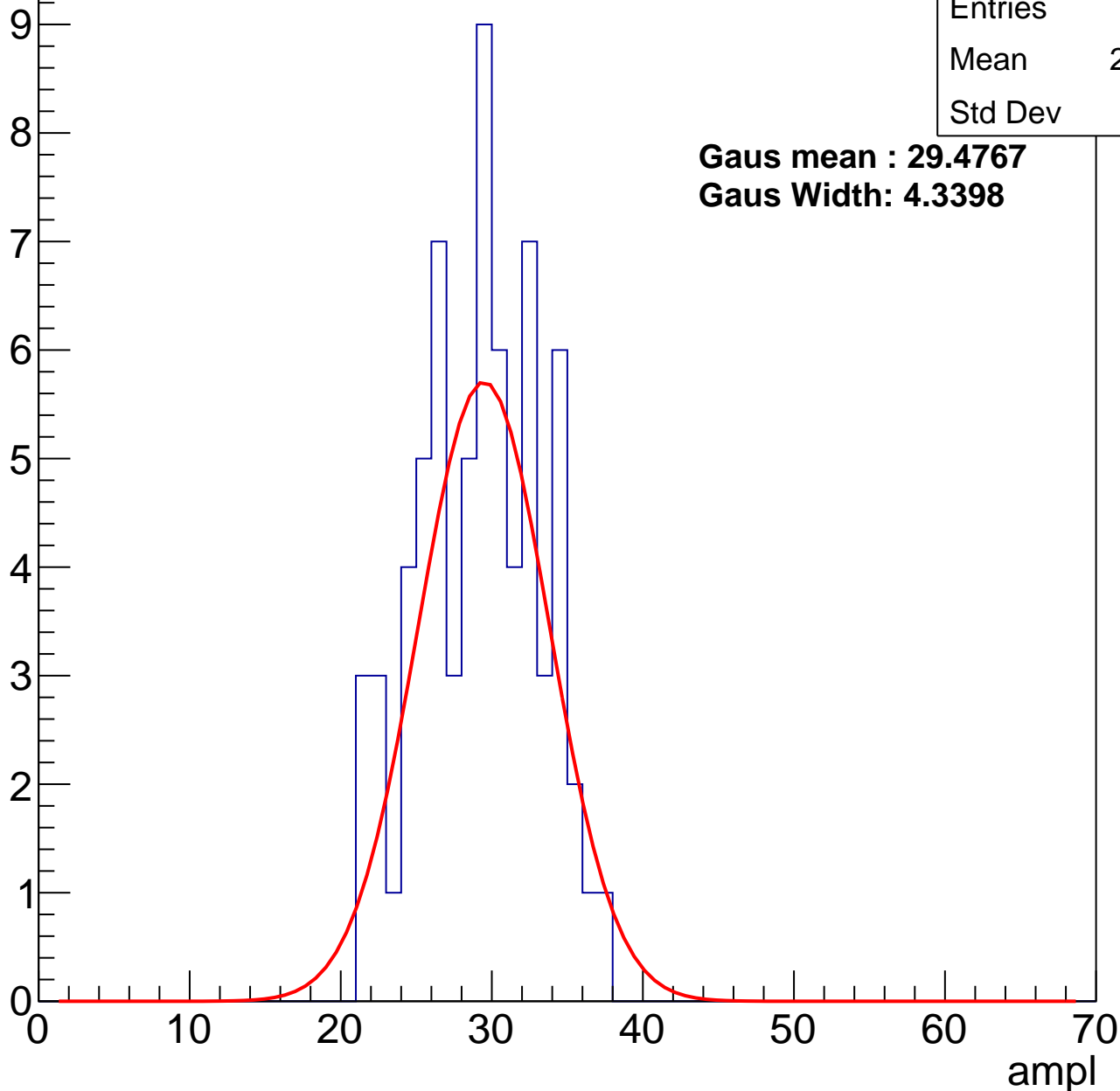
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	28.73
Std Dev	3.96

**Gaus mean : 29.4767**

**Gaus Width: 4.3398**



# B1L101S, U3-ch61, adc1

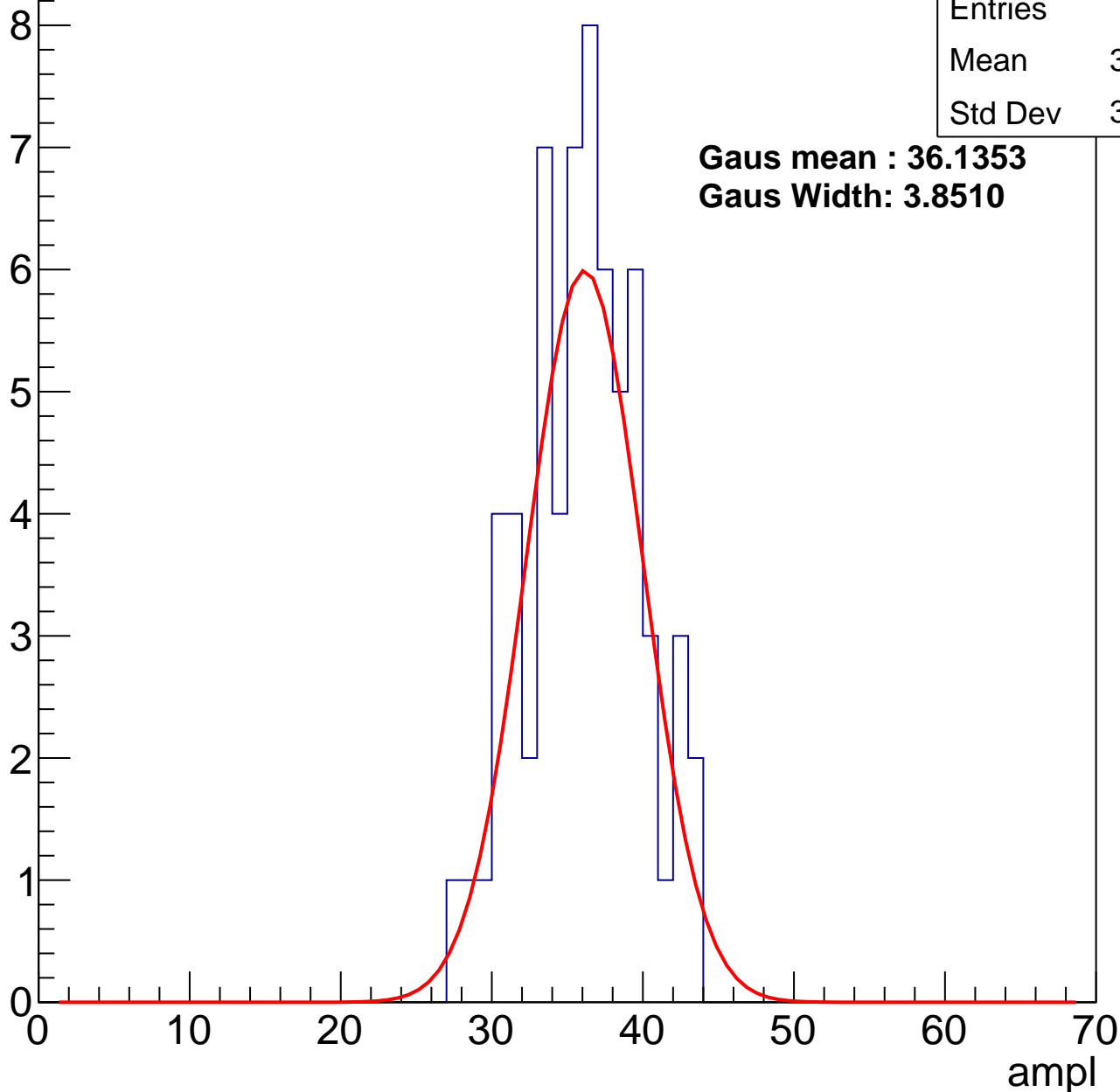
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	35.55
Std Dev	3.725

**Gaus mean : 36.1353**

**Gaus Width: 3.8510**



# B1L101S, U3-ch61, adc2

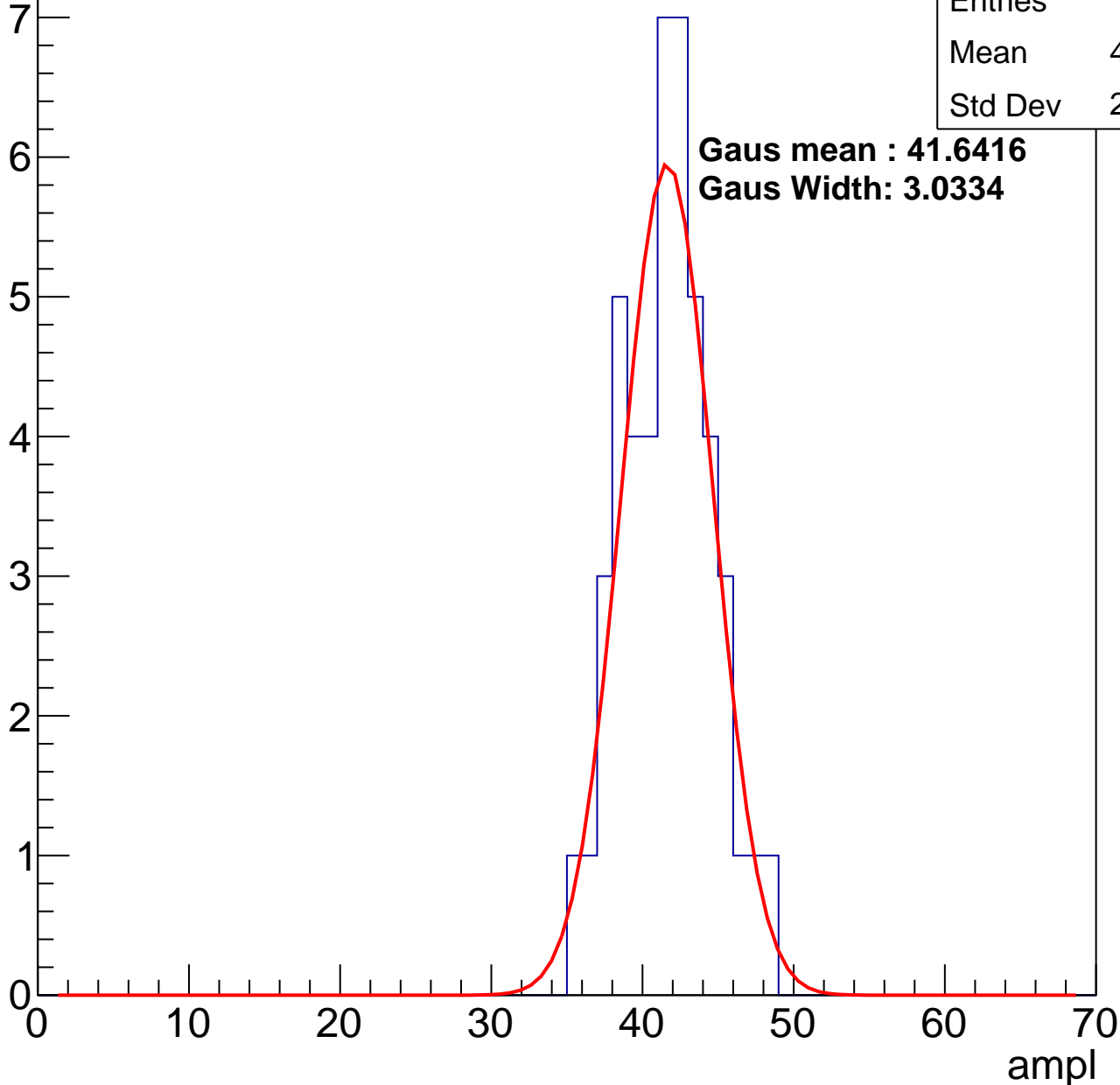
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	41.19
Std Dev	2.893

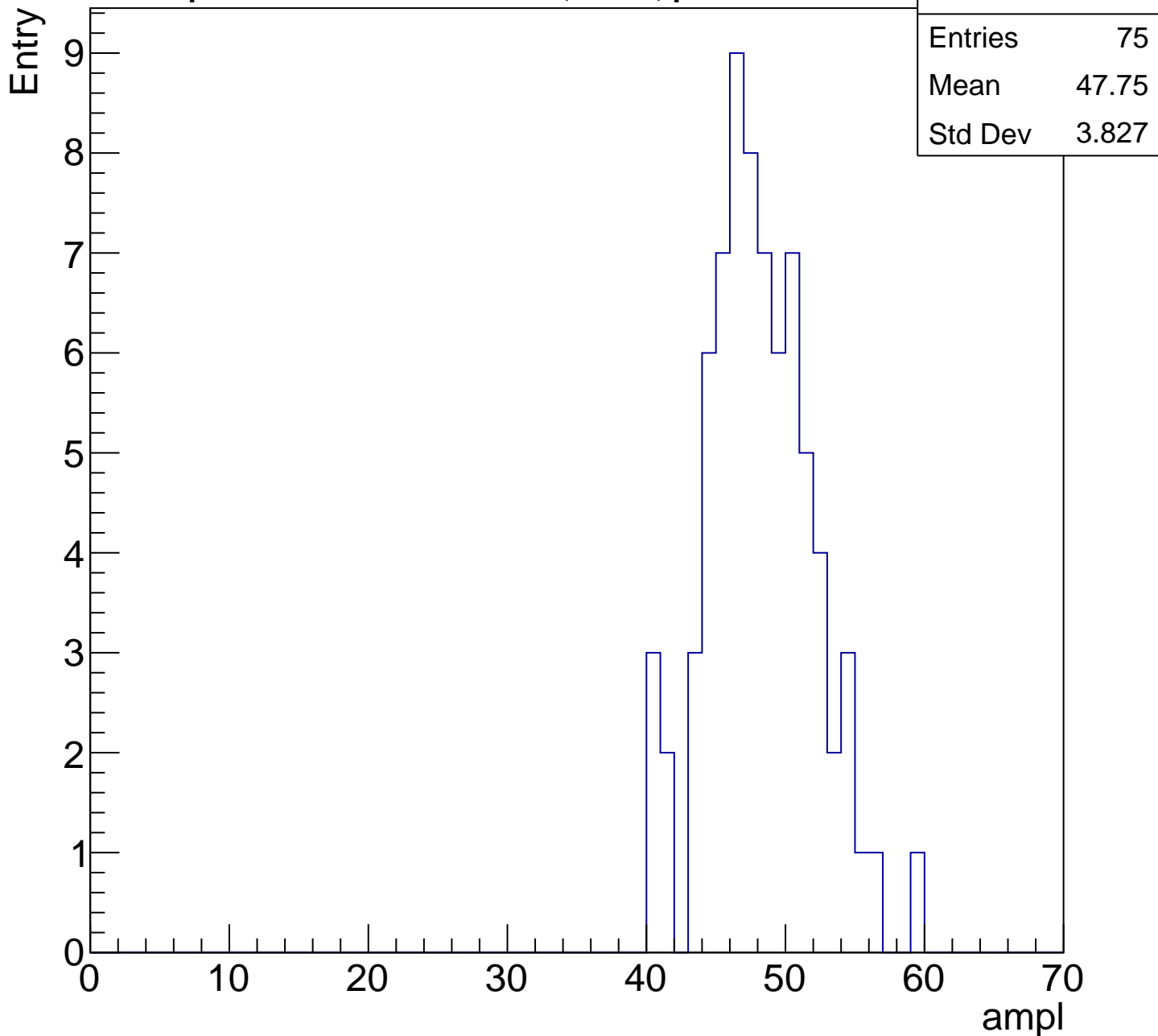
**Gaus mean : 41.6416**

**Gaus Width: 3.0334**



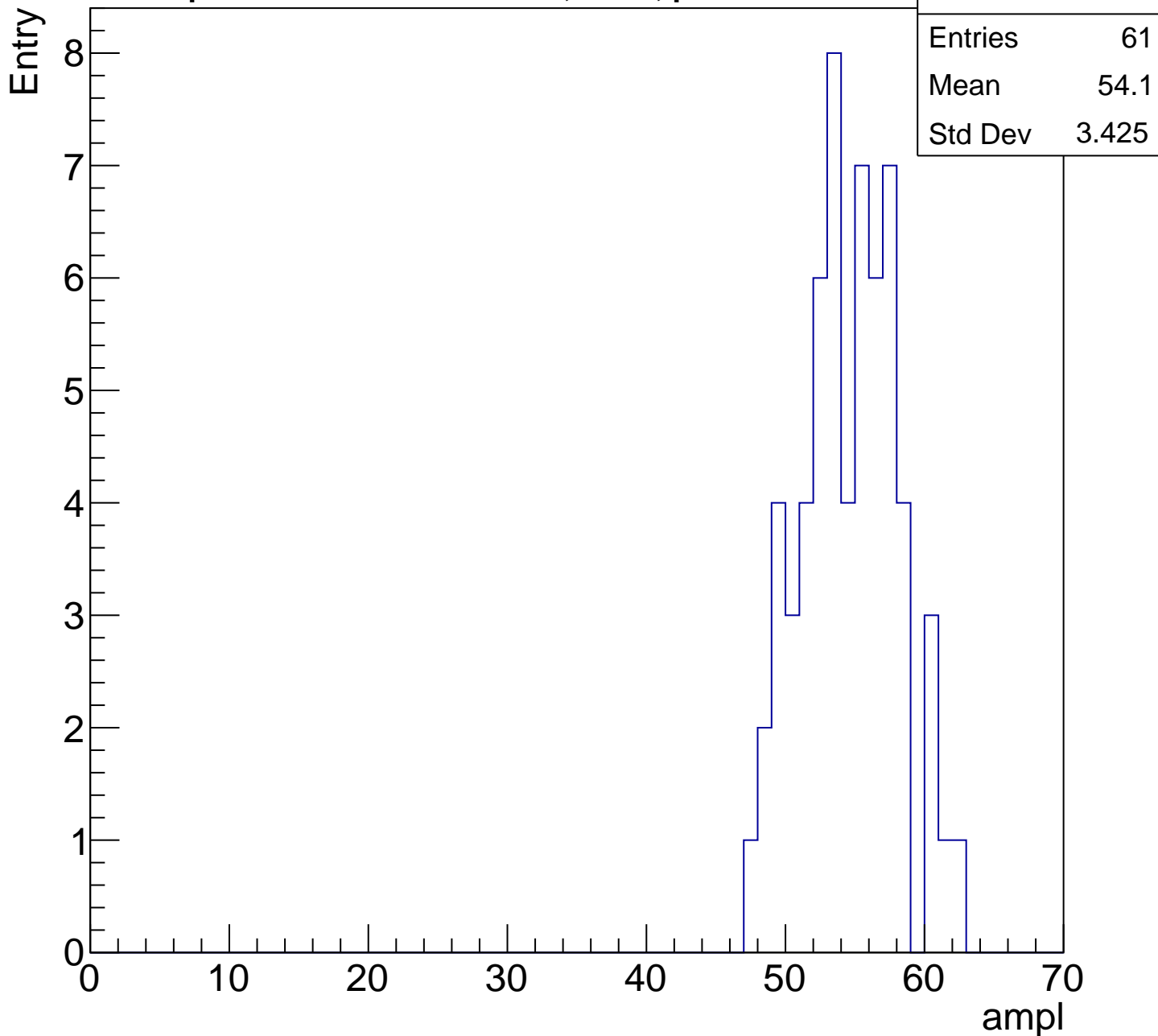
# B1L101S, U3-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

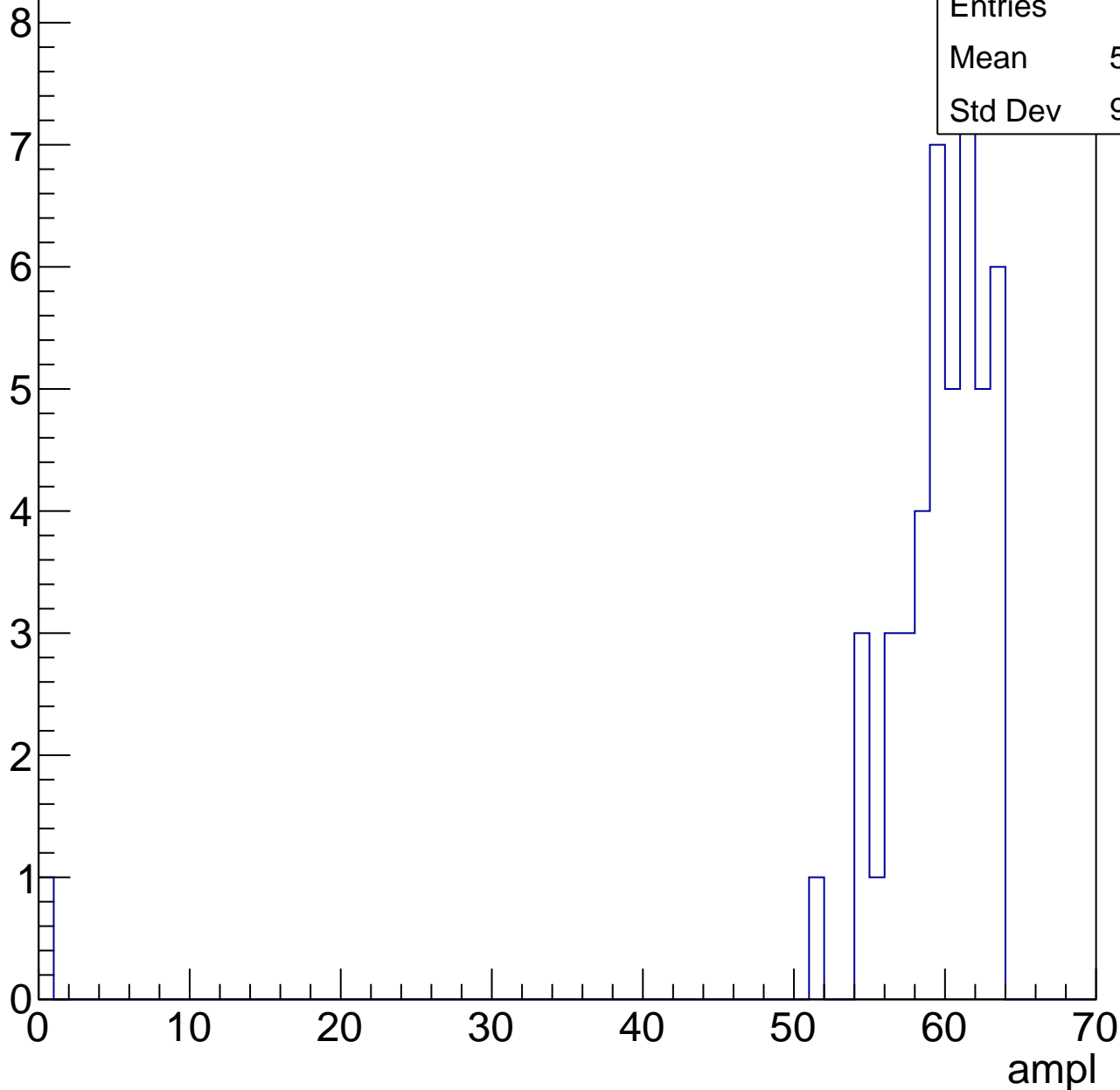


# B1L101S, U3-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

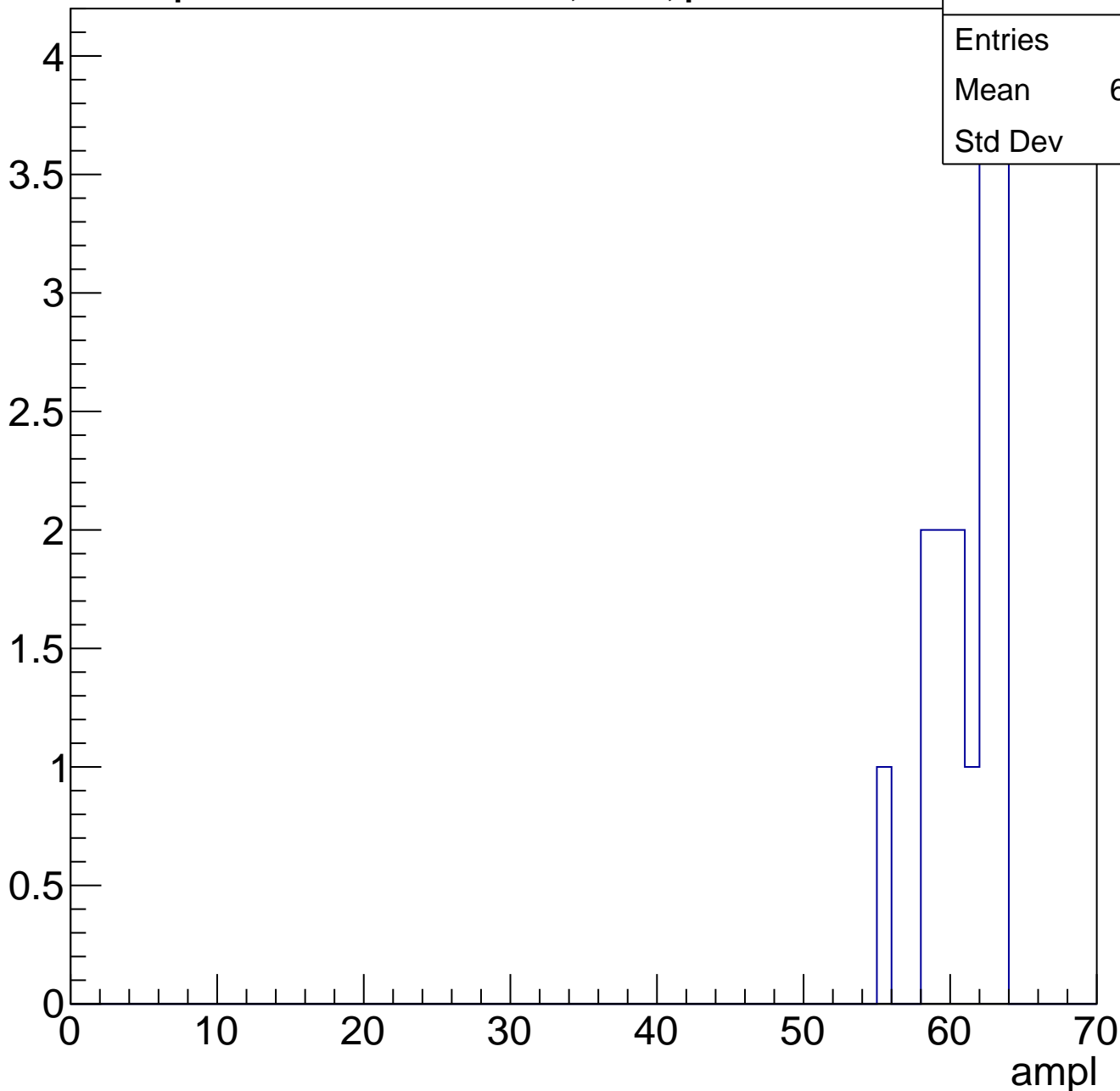
Entries	47
Mean	58.04
Std Dev	9.008



# B1L101S, U3-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch62, adc0

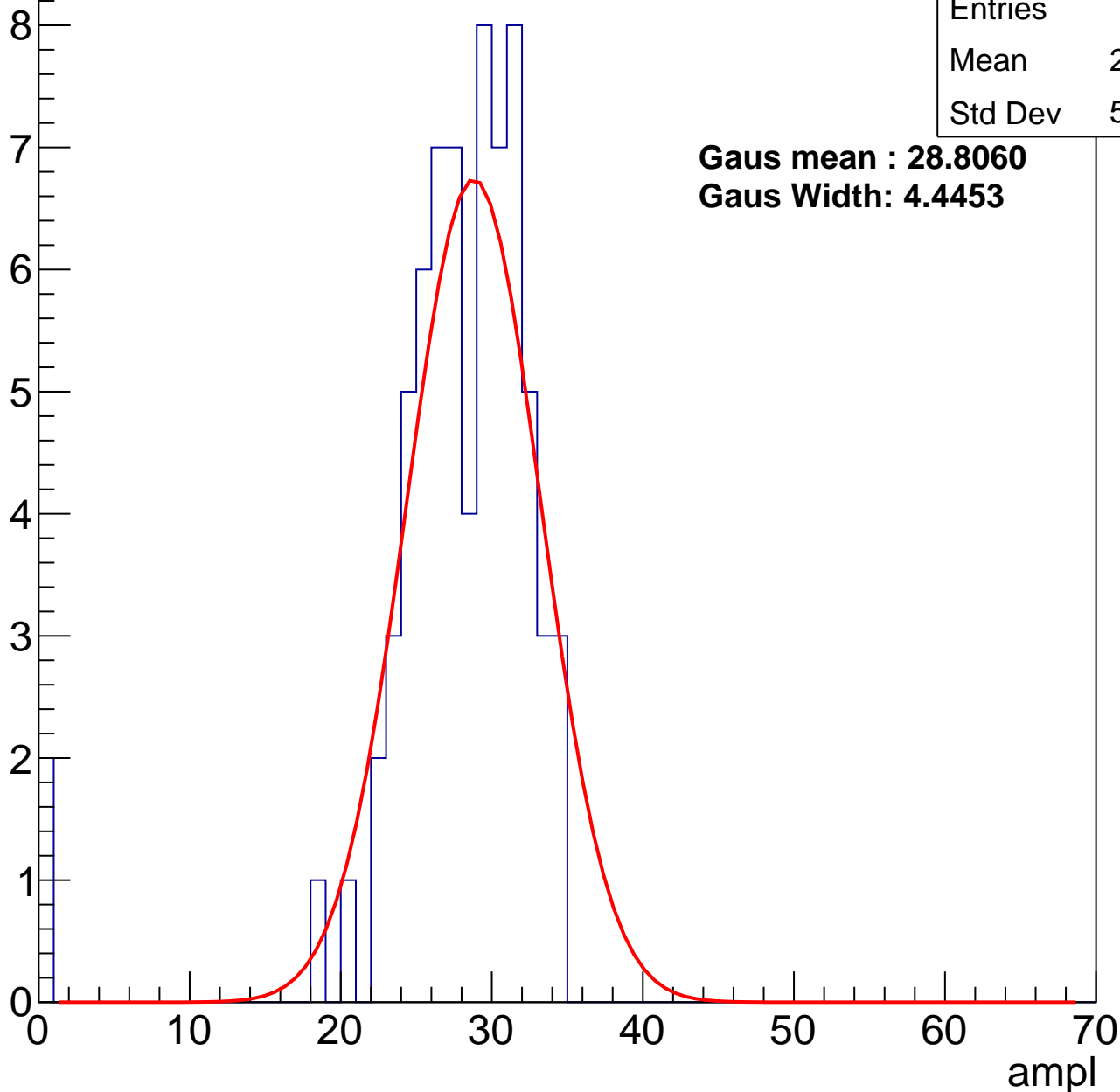
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	27.15
Std Dev	5.734

**Gaus mean : 28.8060**

**Gaus Width: 4.4453**



# B1L101S, U3-ch62, adc1

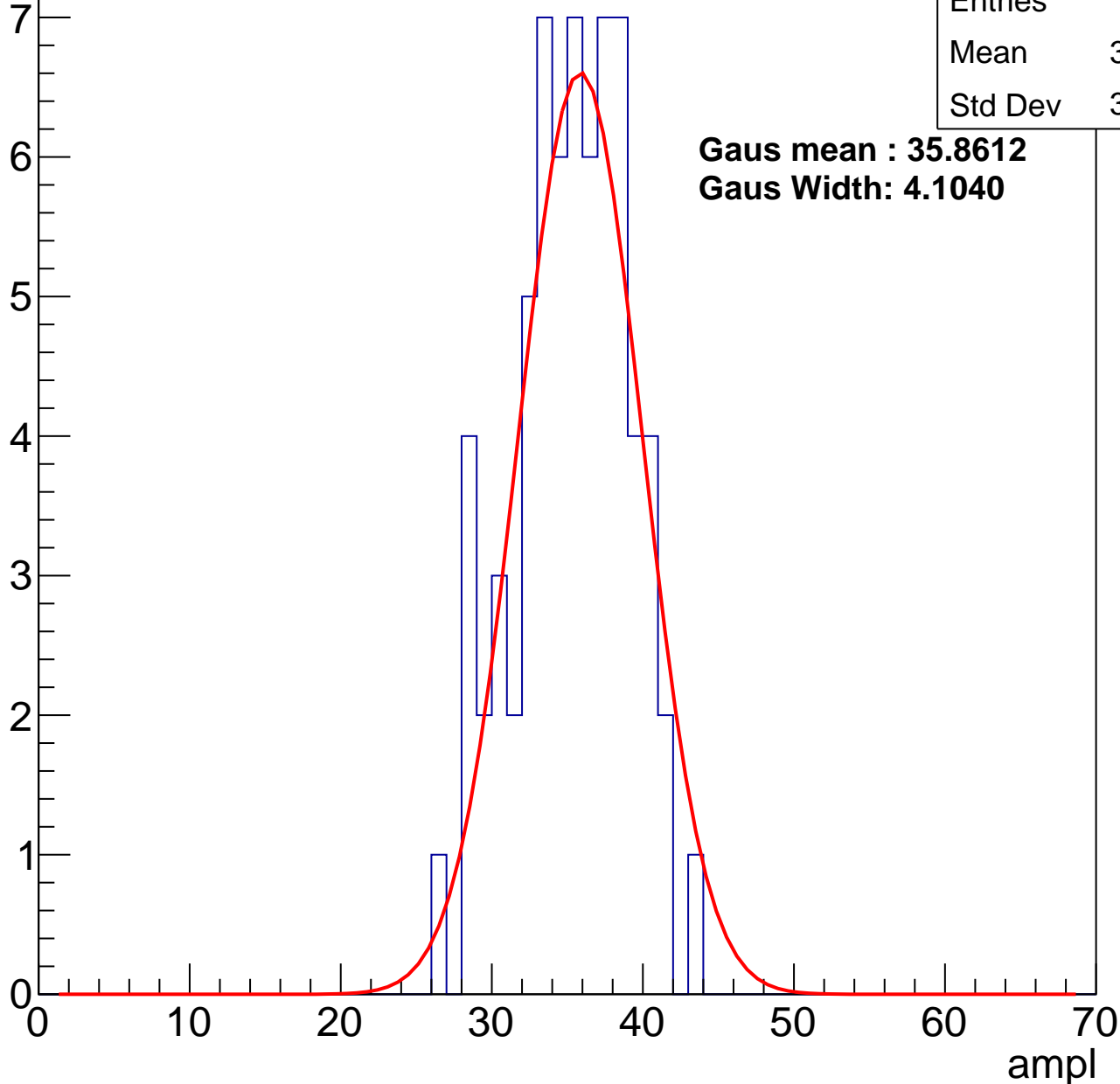
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	34.85
Std Dev	3.699

**Gaus mean : 35.8612**

**Gaus Width: 4.1040**



# B1L101S, U3-ch62, adc2

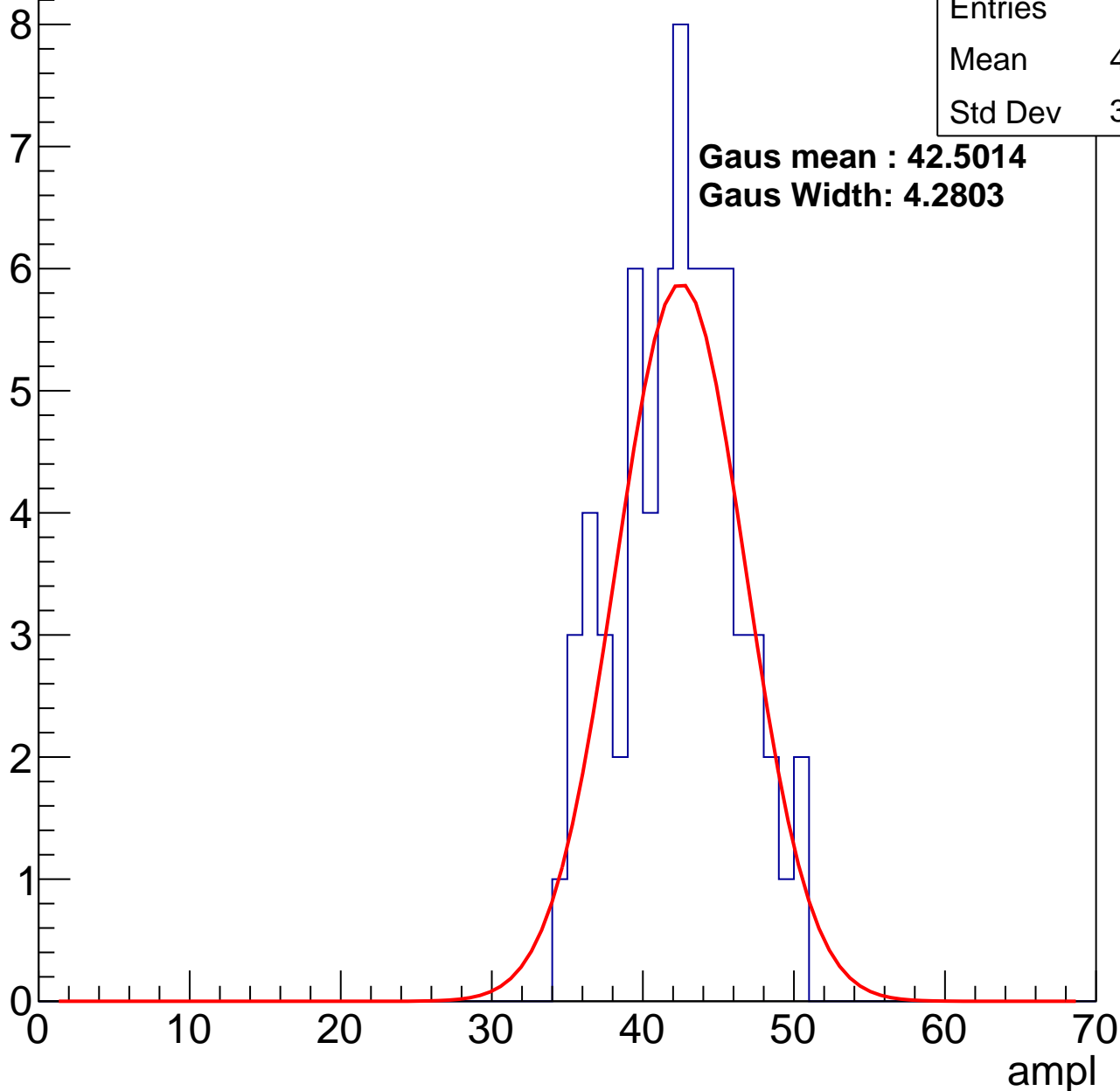
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	41.85
Std Dev	3.878

**Gaus mean : 42.5014**

**Gaus Width: 4.2803**

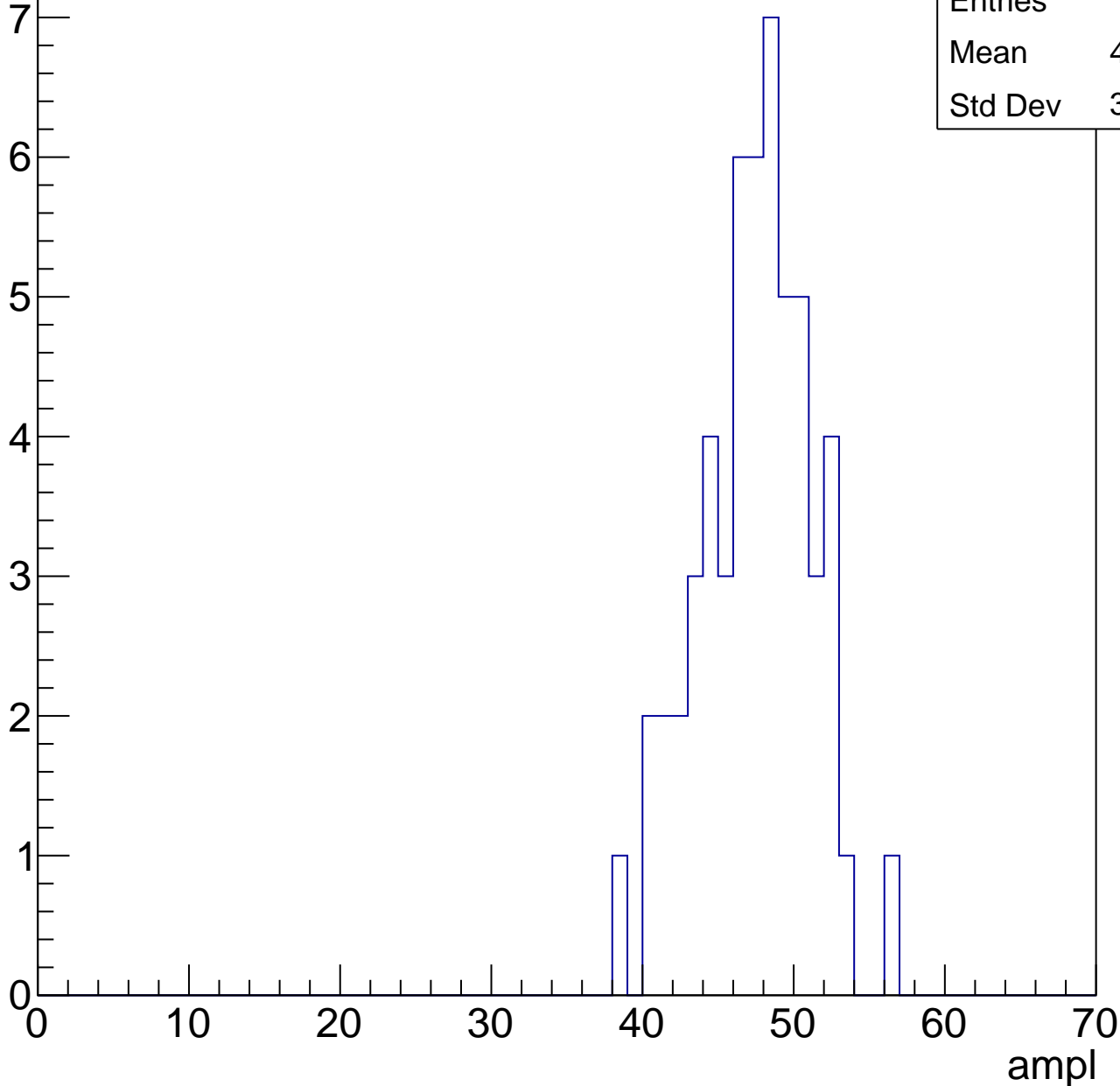


# B1L101S, U3-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

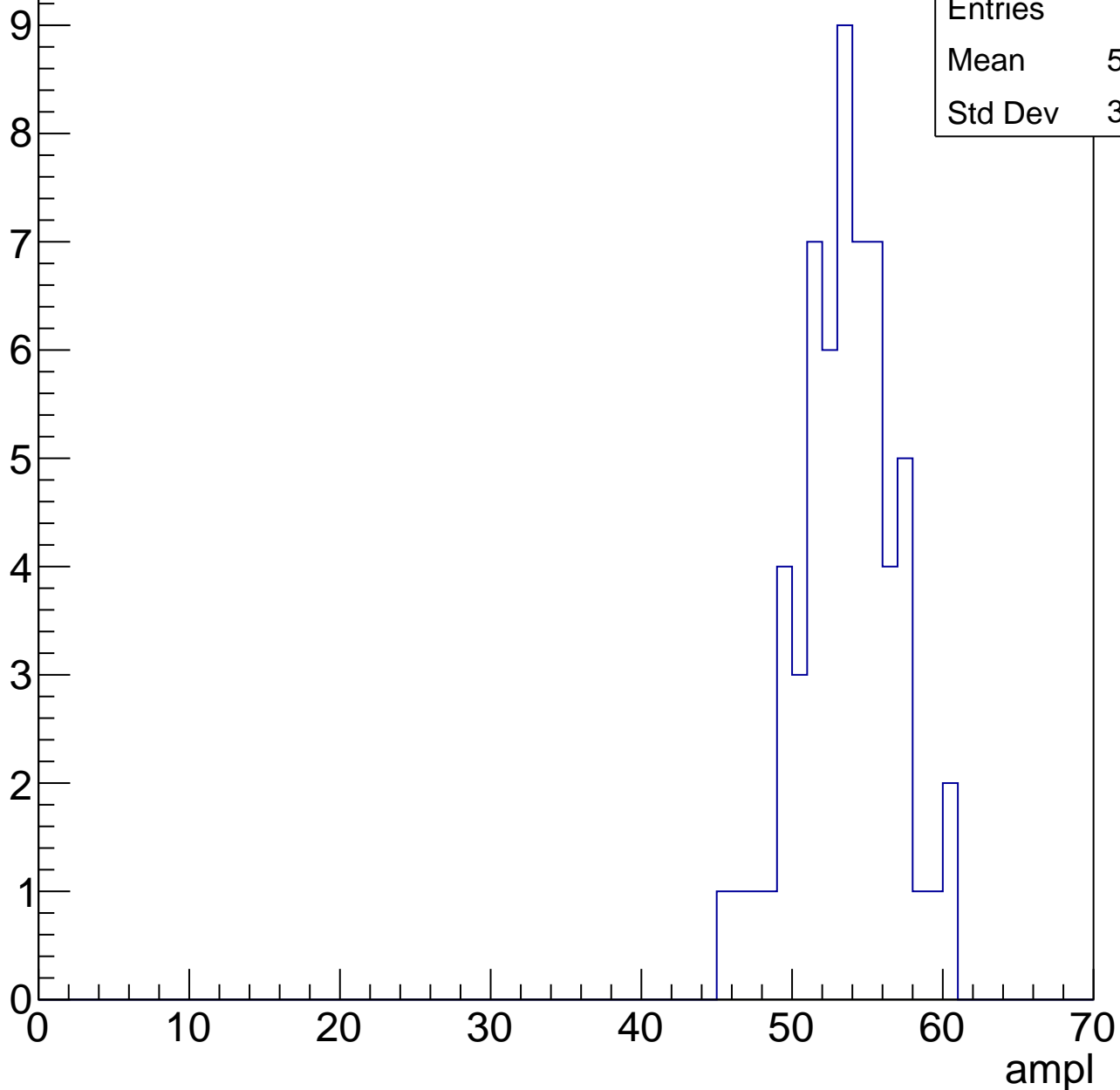
Entries	55
Mean	46.96
Std Dev	3.668



# B1L101S, U3-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

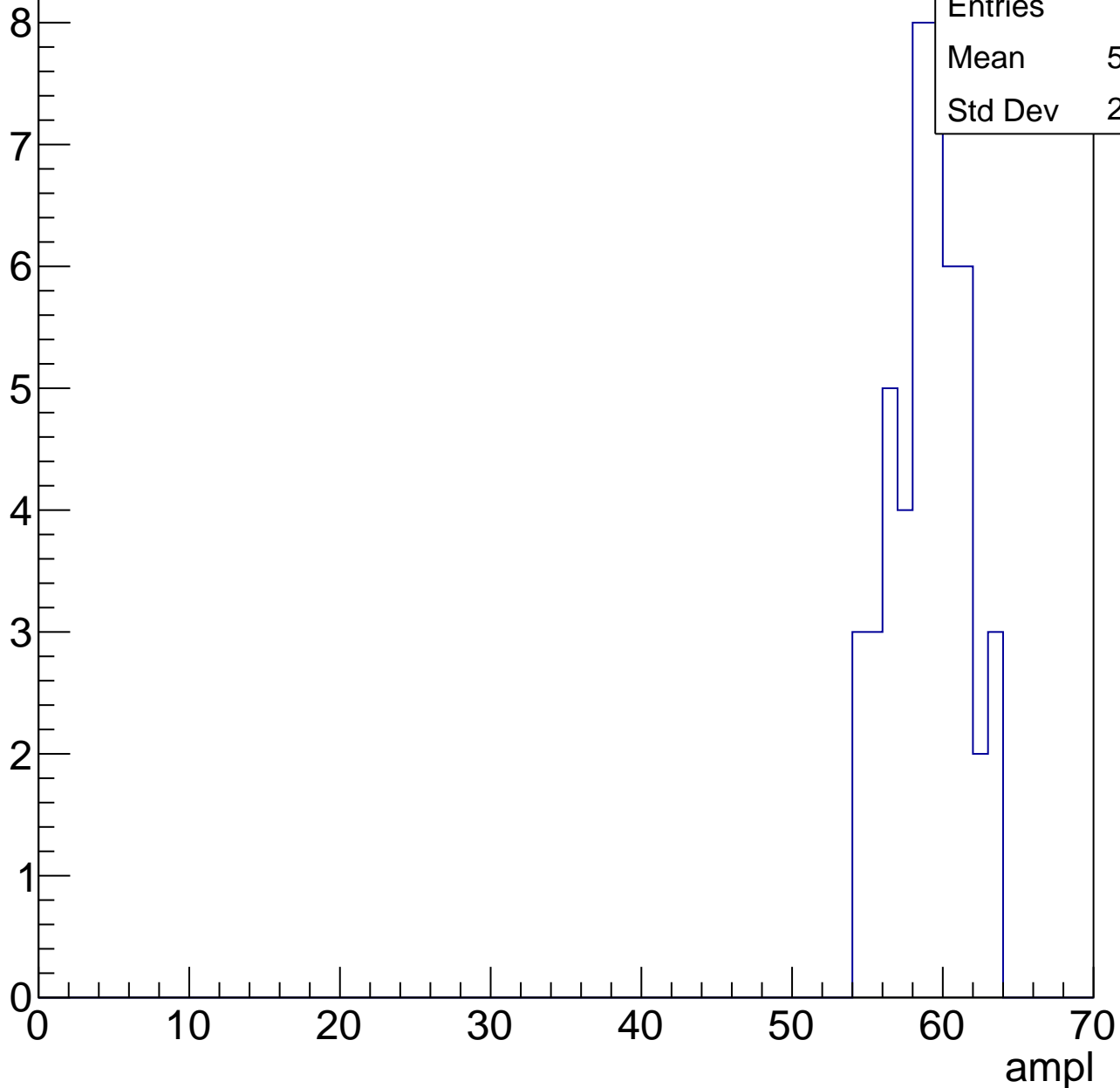
Entry



# B1L101S, U3-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

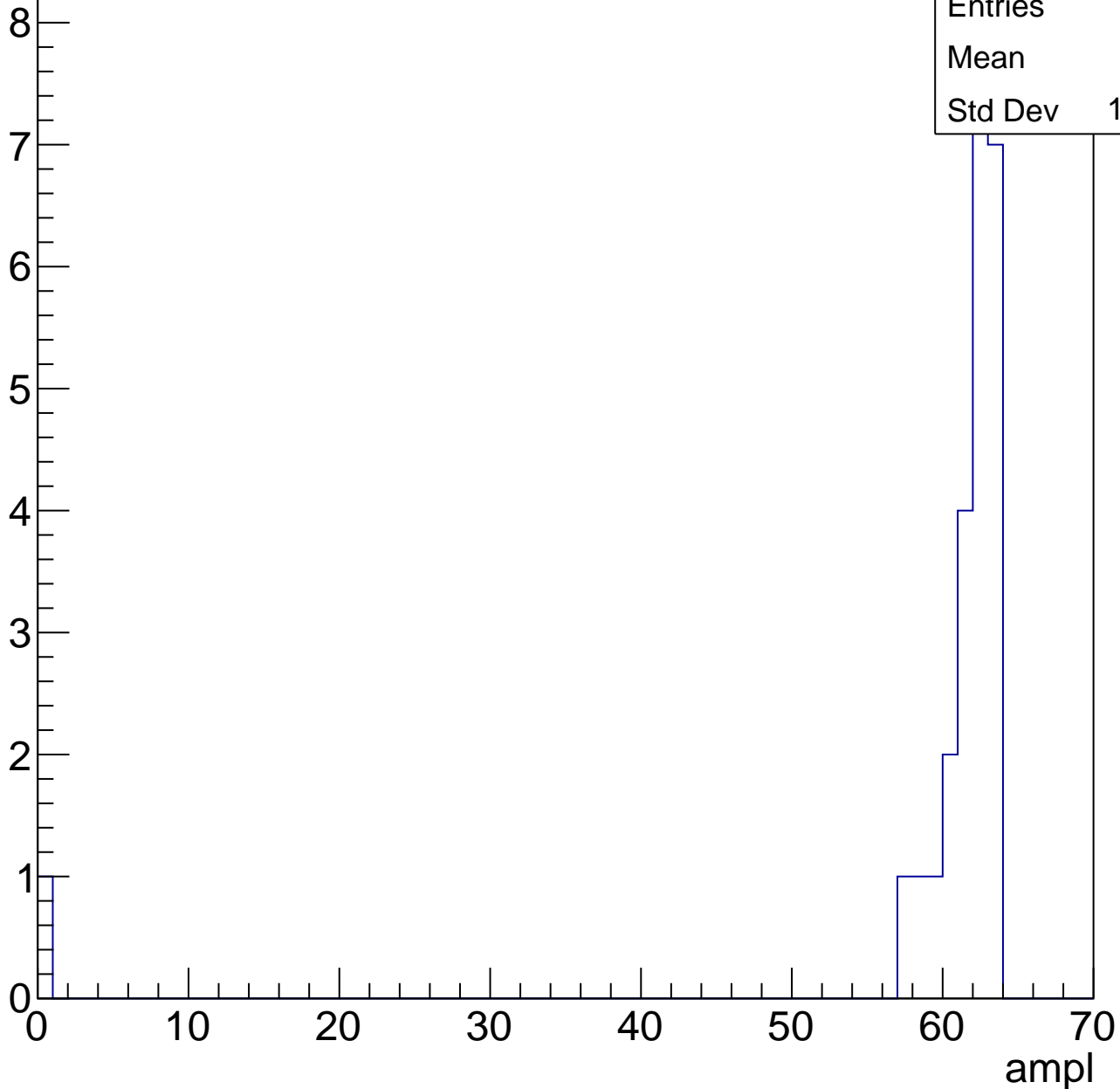


# B1L101S, U3-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	25
Mean	59
Std Dev	12.15





# B1L101S, U3-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U3-ch63, adc0

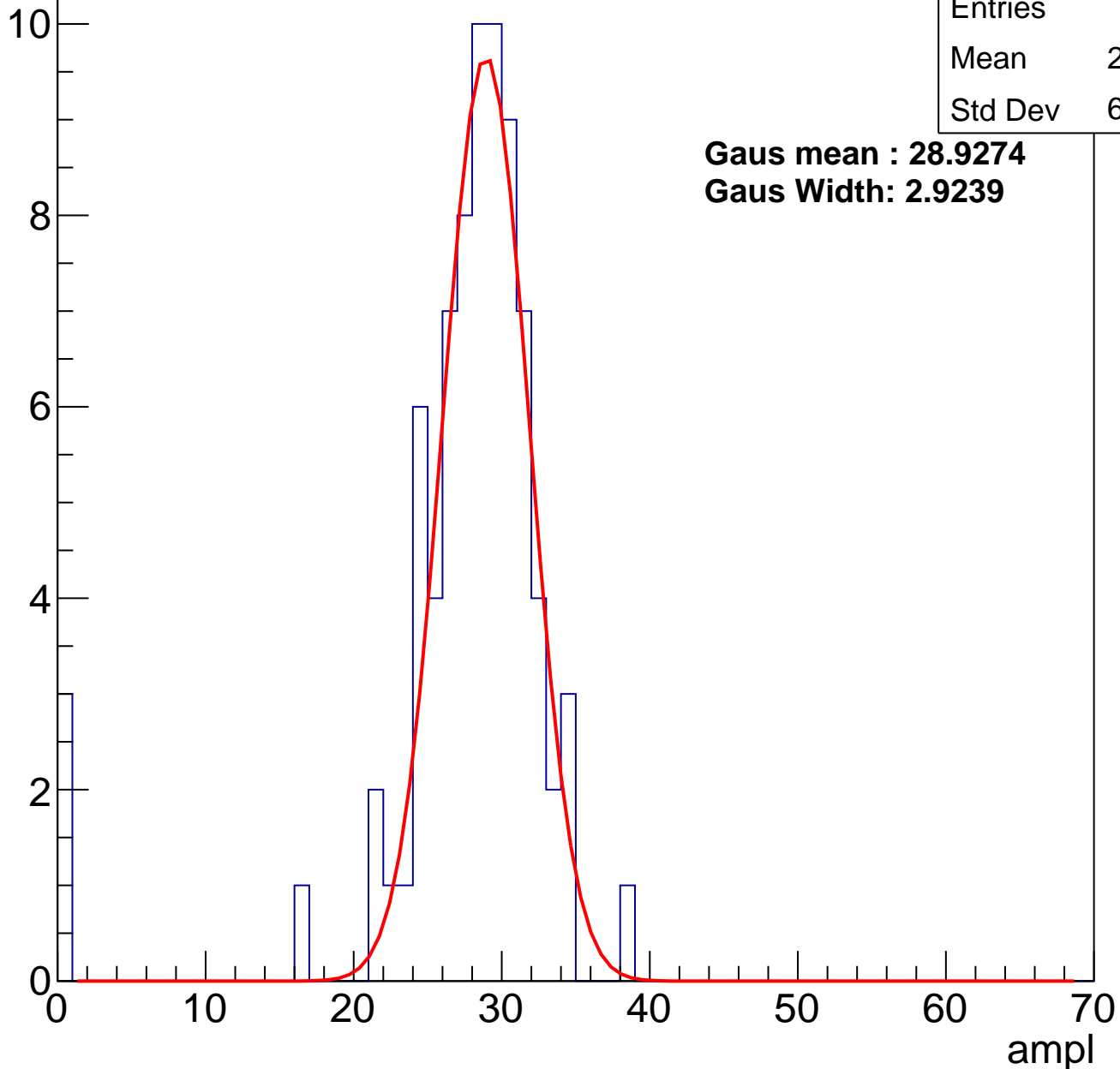
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	79
Mean	27.04
Std Dev	6.345

**Gaus mean : 28.9274**

**Gaus Width: 2.9239**

Entry



# B1L101S, U3-ch63, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	70
Mean	35.19
Std Dev	5.383

**Gaus mean : 35.8363**

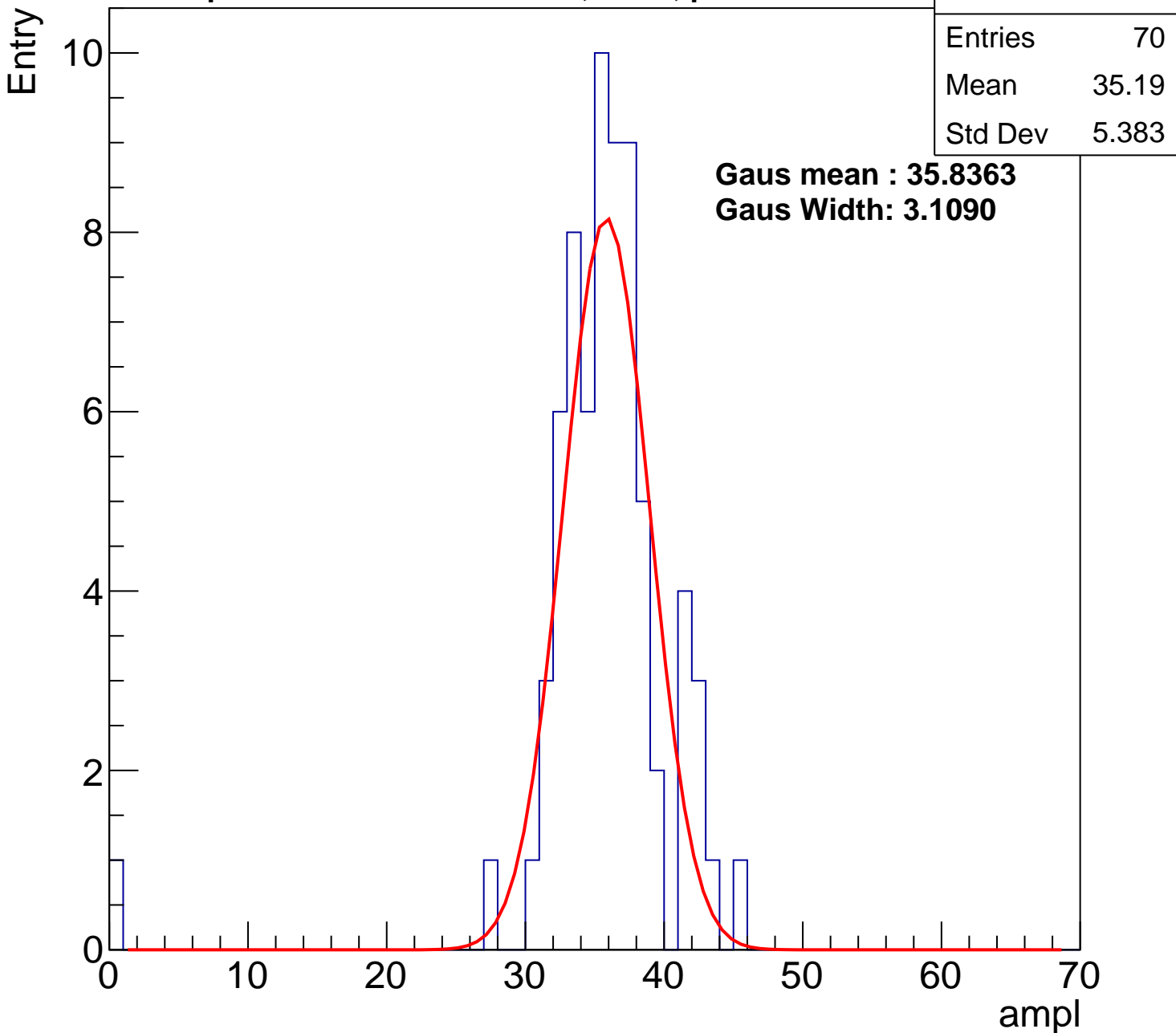
**Gaus Width: 3.1090**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U3-ch63, adc2

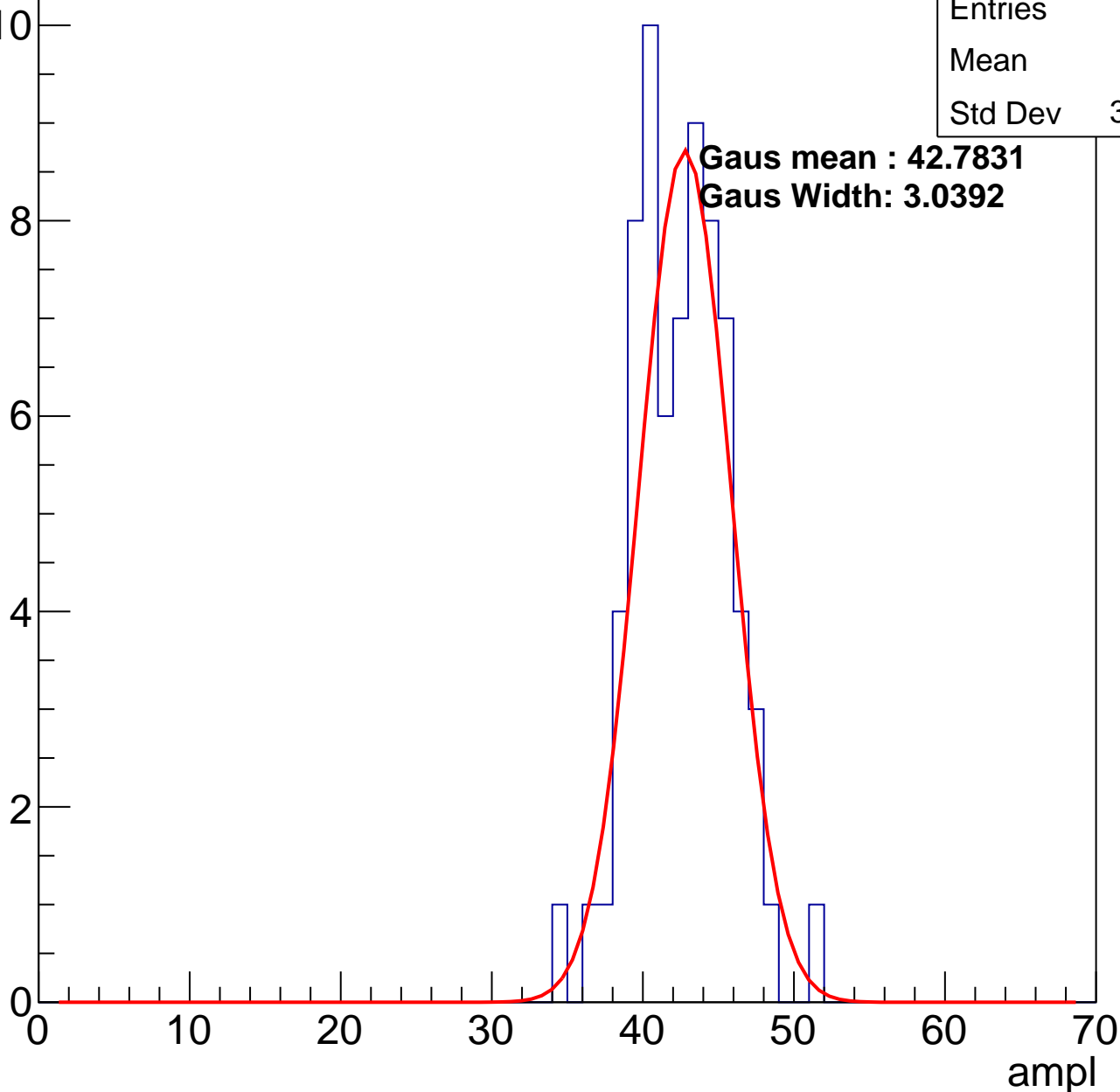
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	42.1
Std Dev	3.063

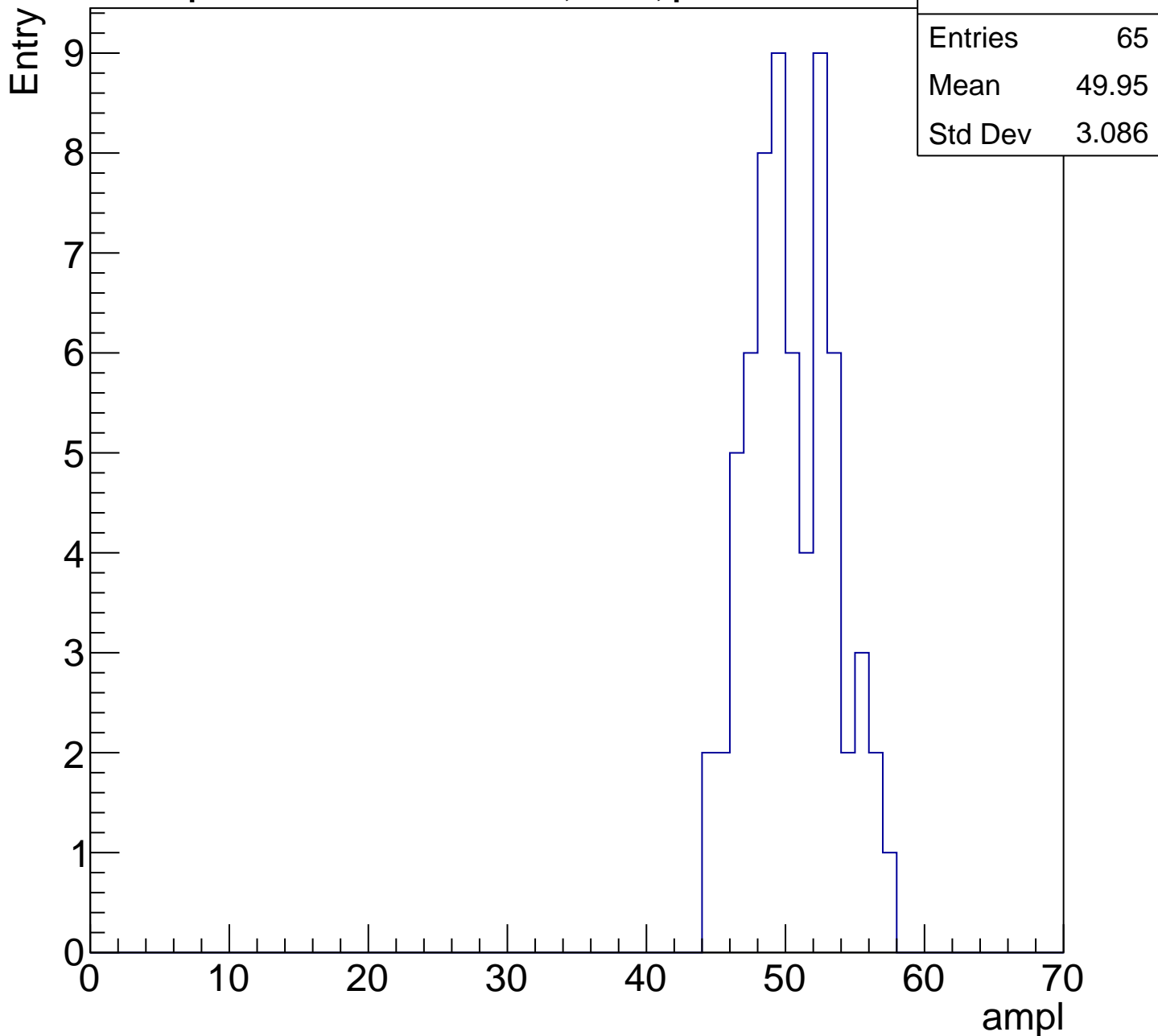
**Gaus mean : 42.7831**

**Gaus Width: 3.0392**



# B1L101S, U3-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

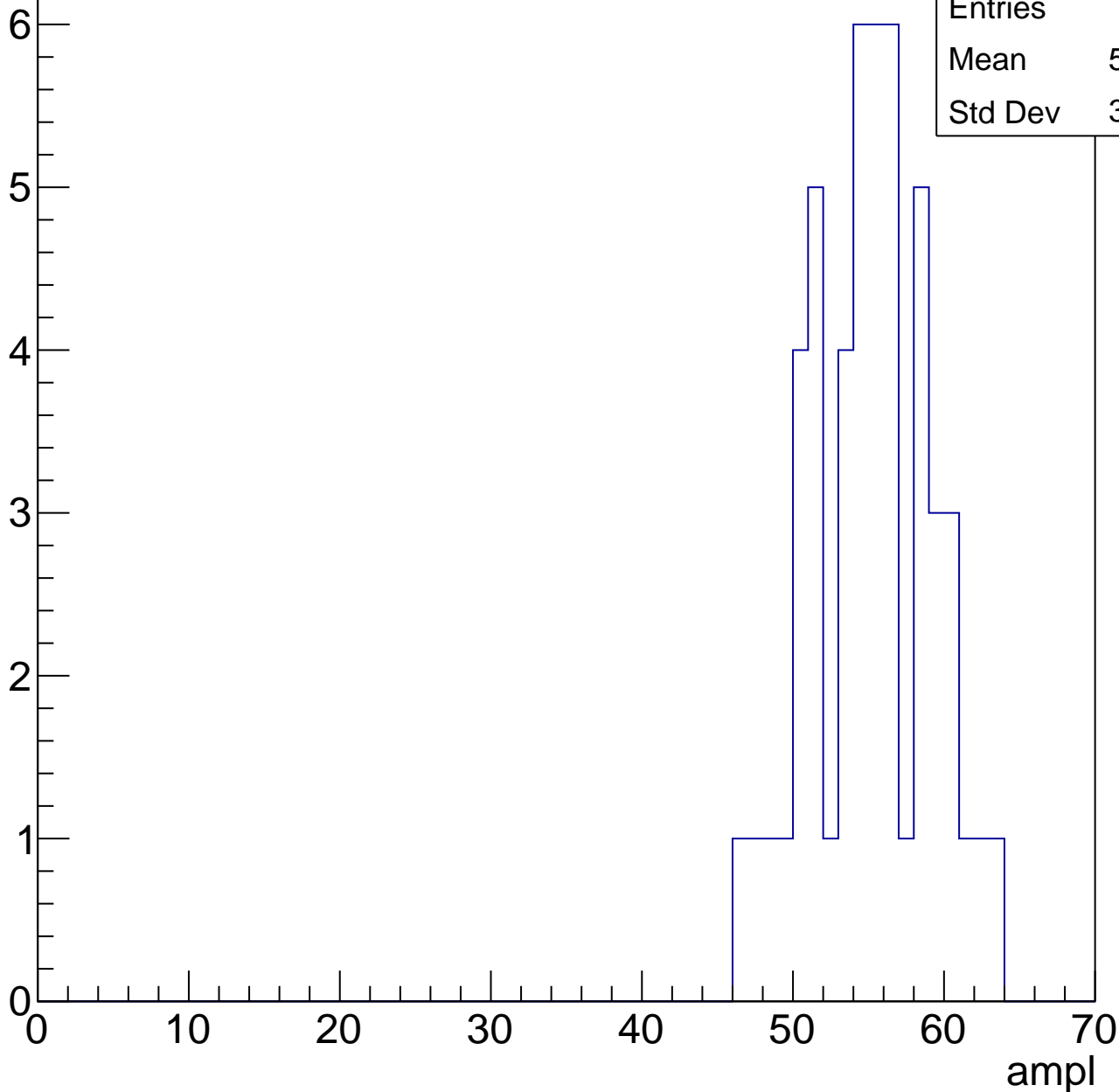


# B1L101S, U3-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

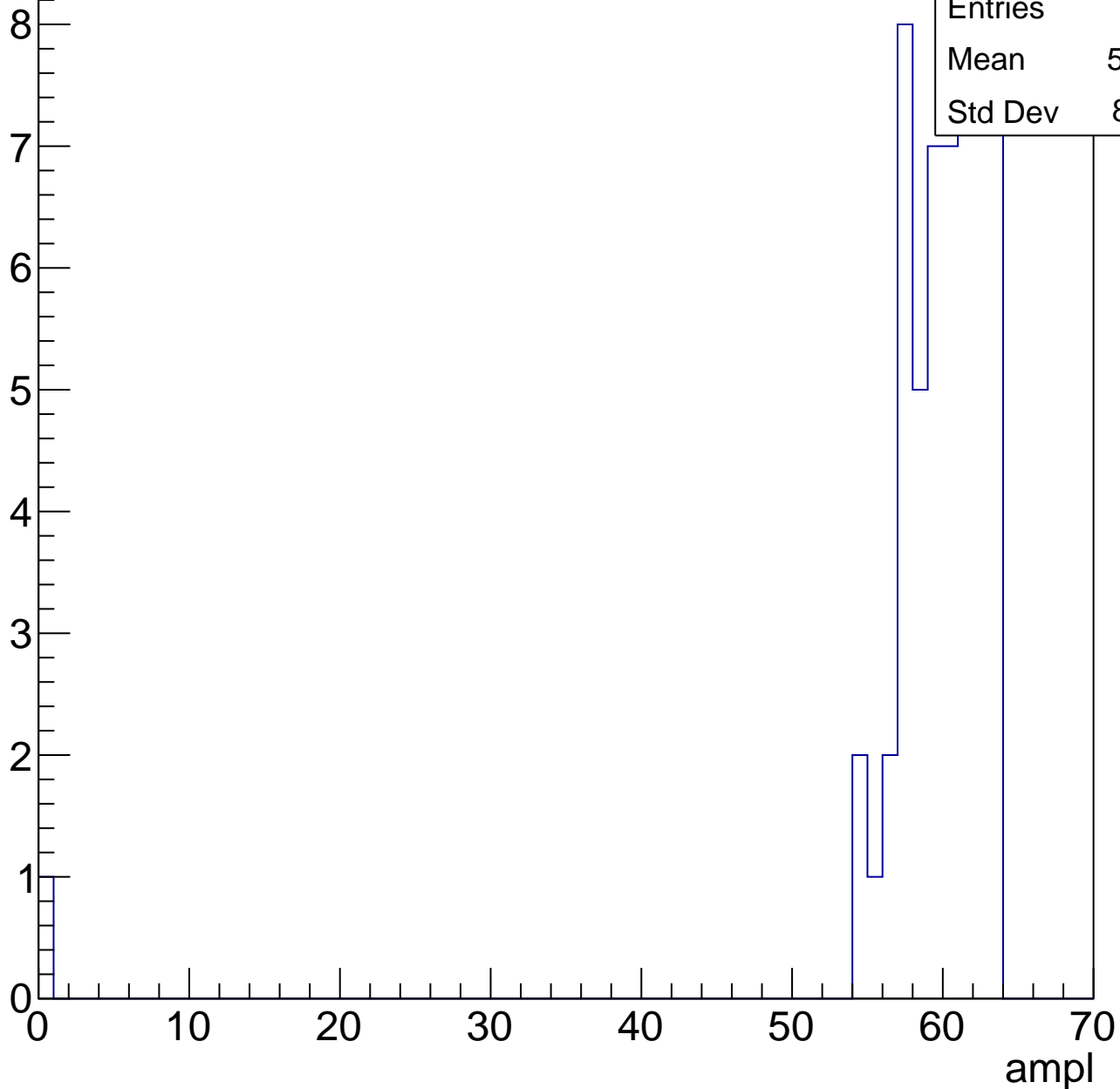
Entries	51
Mean	54.69
Std Dev	3.868



# B1L101S, U3-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

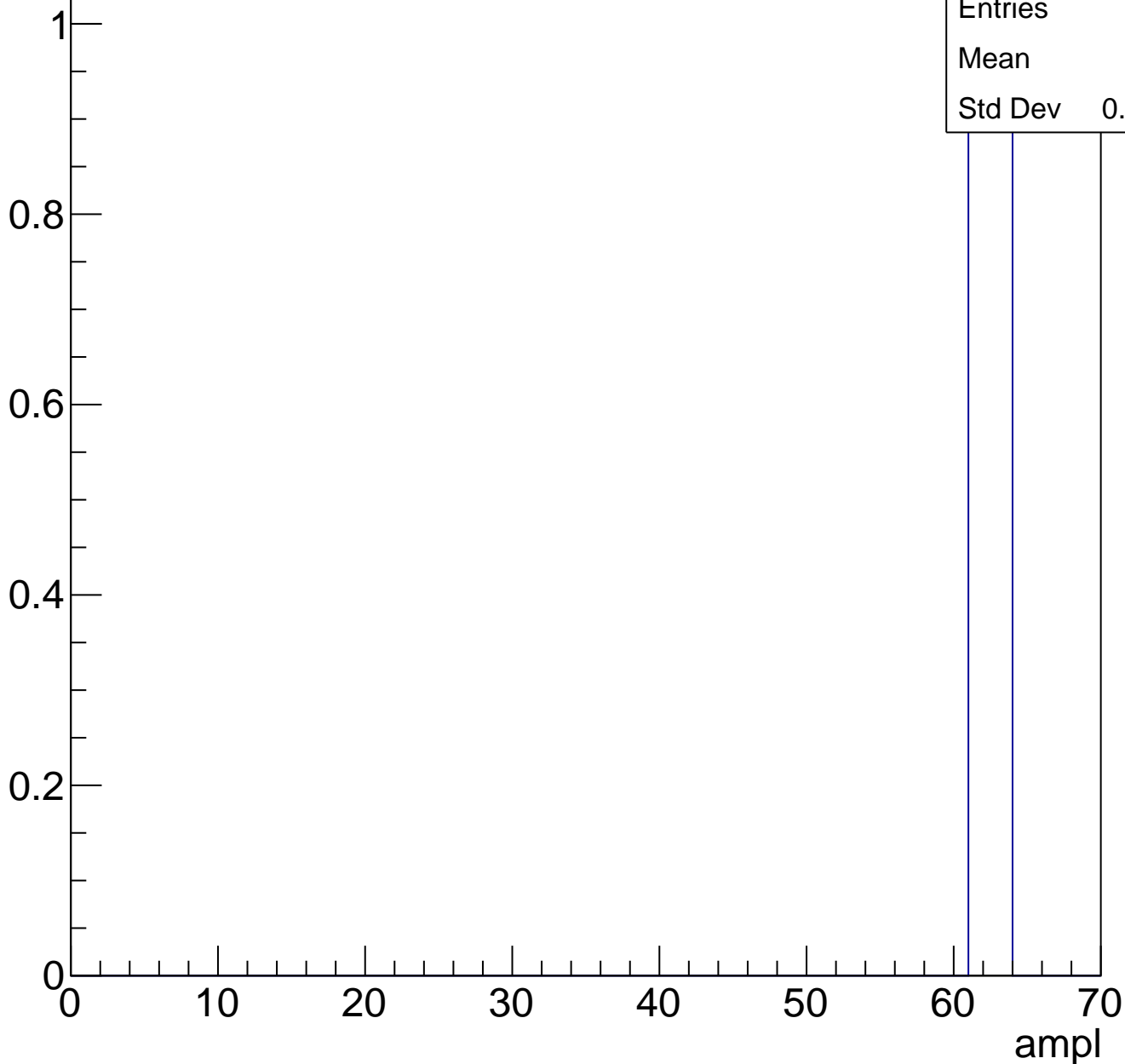
Entry



# B1L101S, U3-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch64, adc0

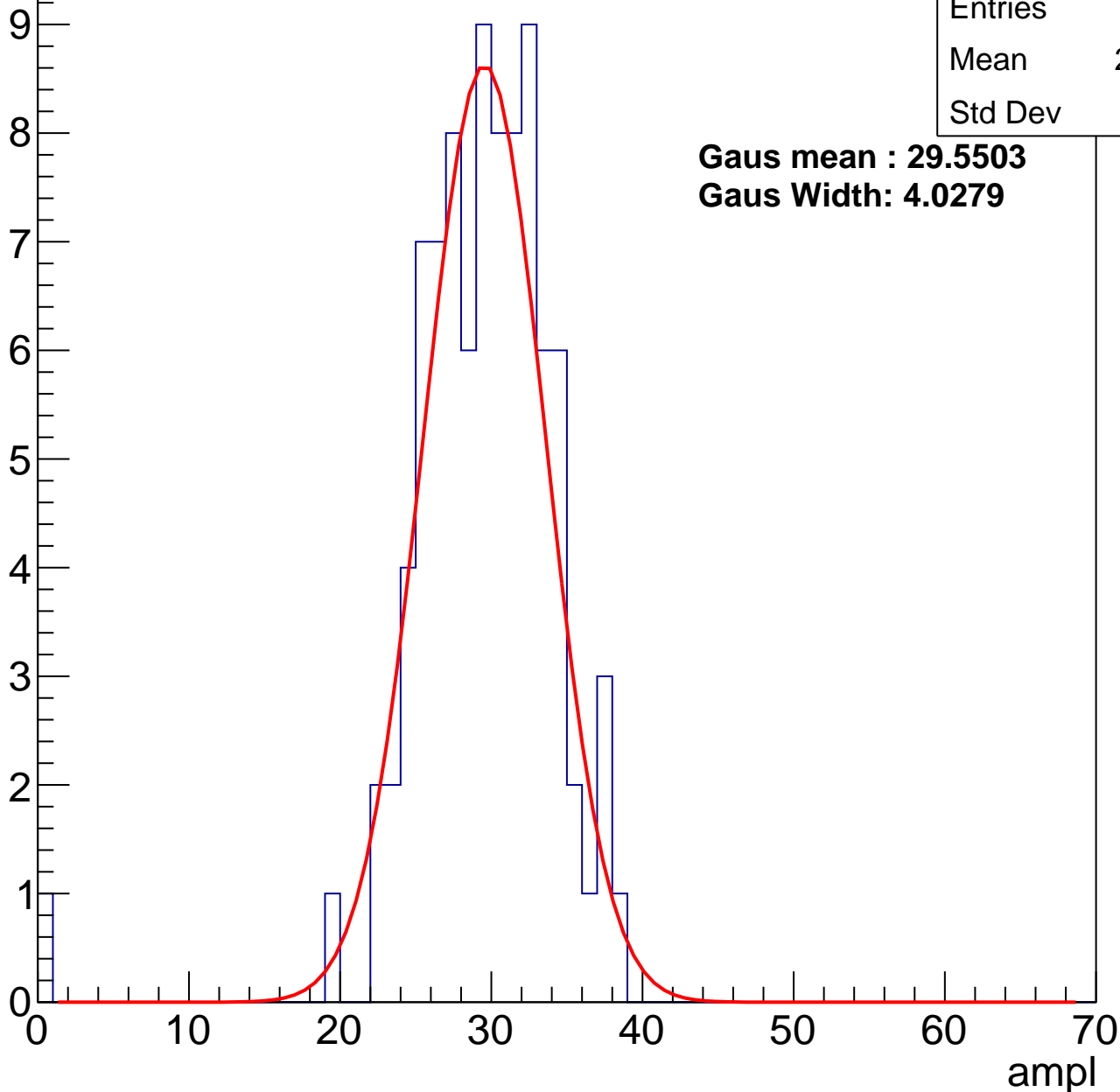
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	91
Mean	29.01
Std Dev	4.9

**Gaus mean : 29.5503**

**Gaus Width: 4.0279**



# B1L101S, U3-ch64, adc1

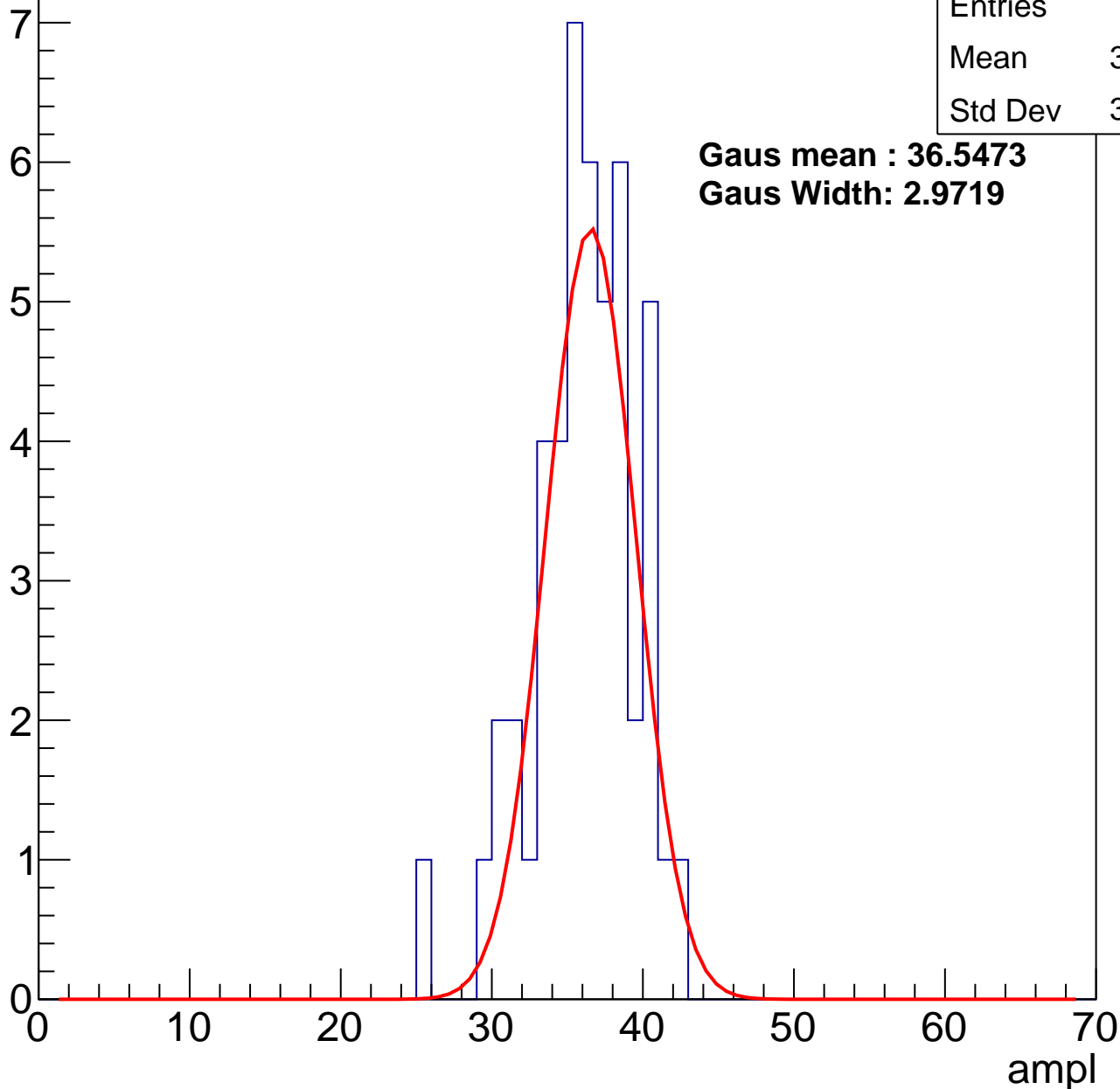
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	35.65
Std Dev	3.382

**Gaus mean : 36.5473**

**Gaus Width: 2.9719**



# B1L101S, U3-ch64, adc2

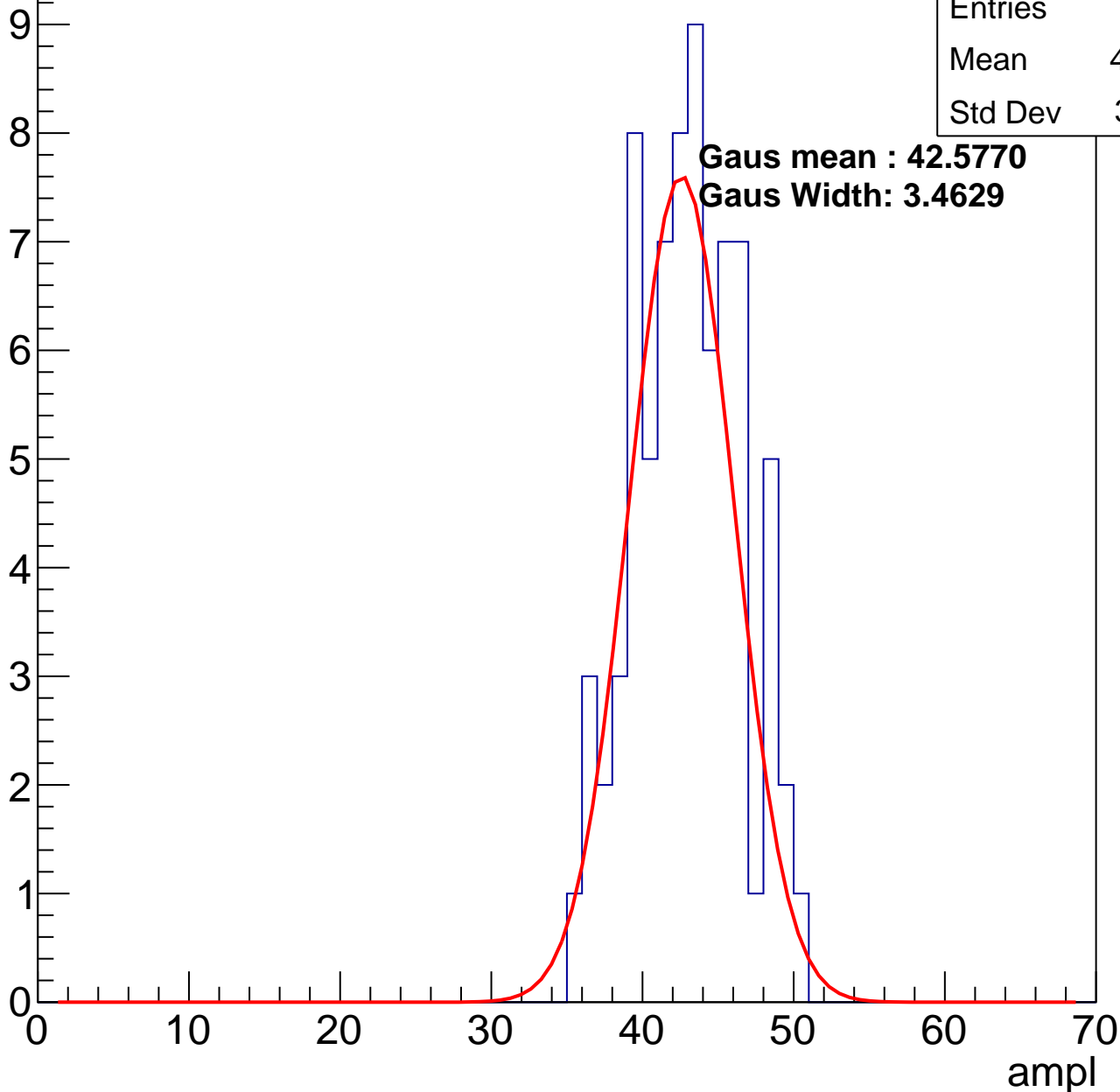
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	42.52
Std Dev	3.481

**Gaus mean : 42.5770**

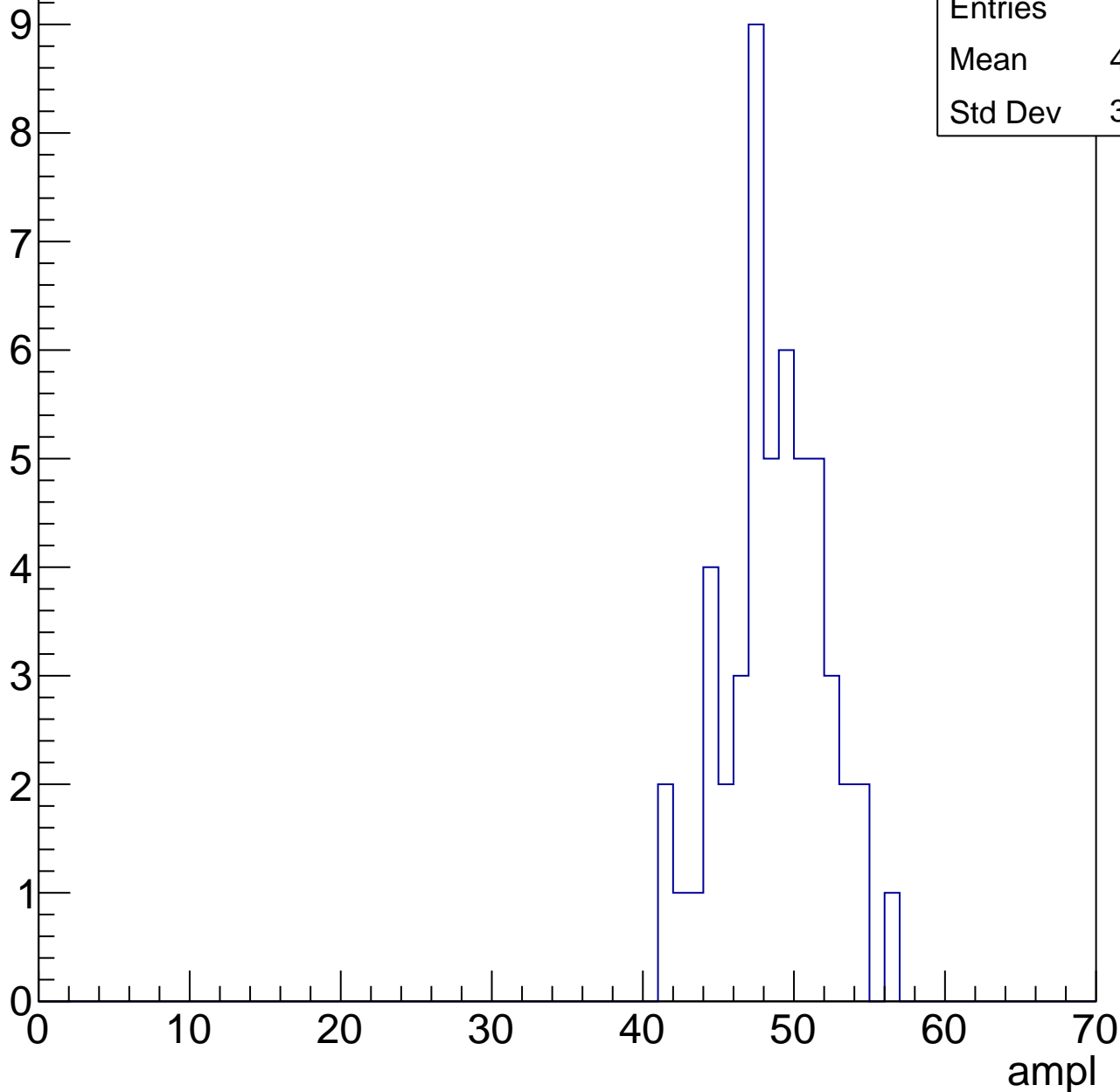
**Gaus Width: 3.4629**



# B1L101S, U3-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

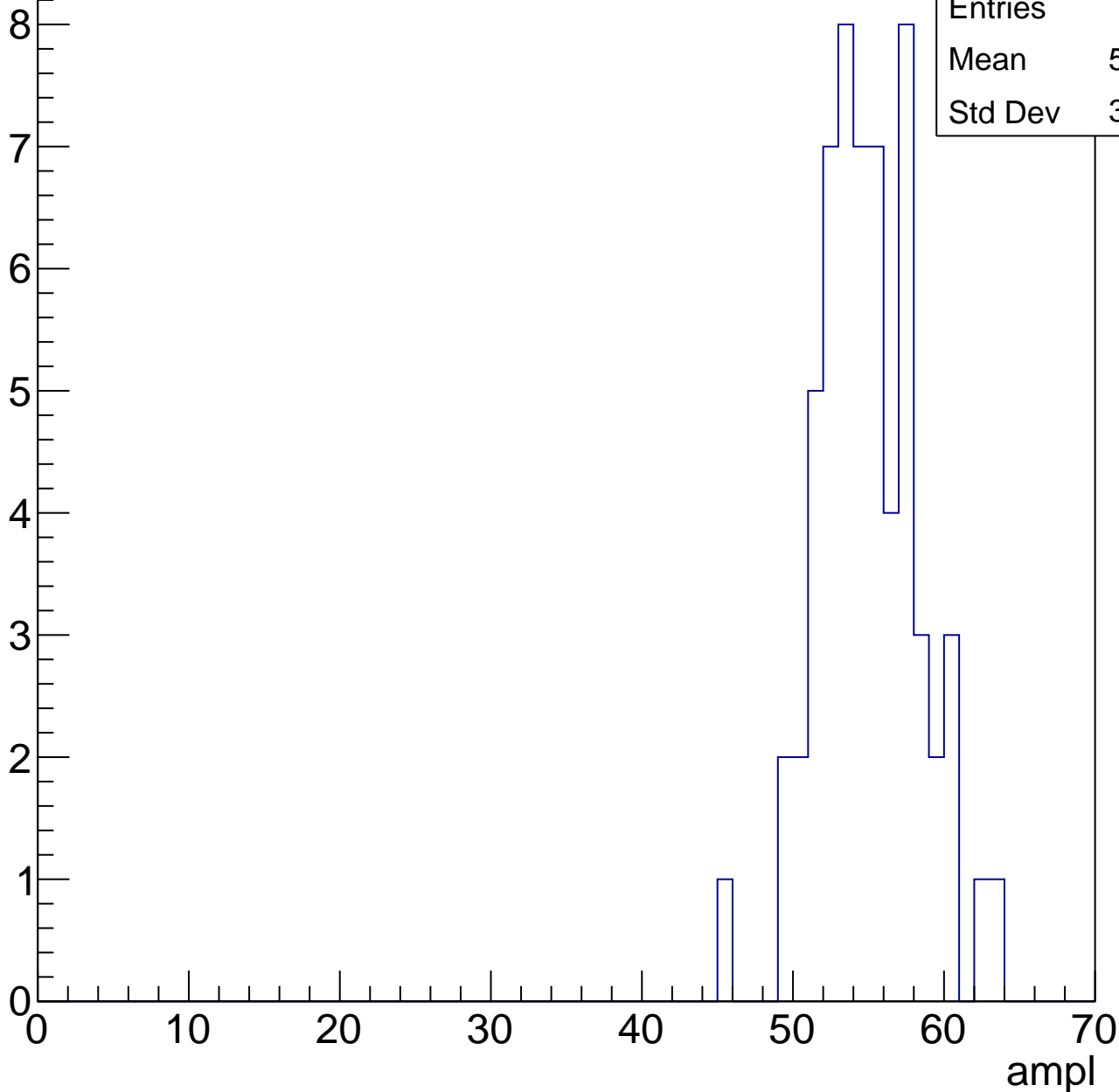


# B1L101S, U3-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	54.52
Std Dev	3.322

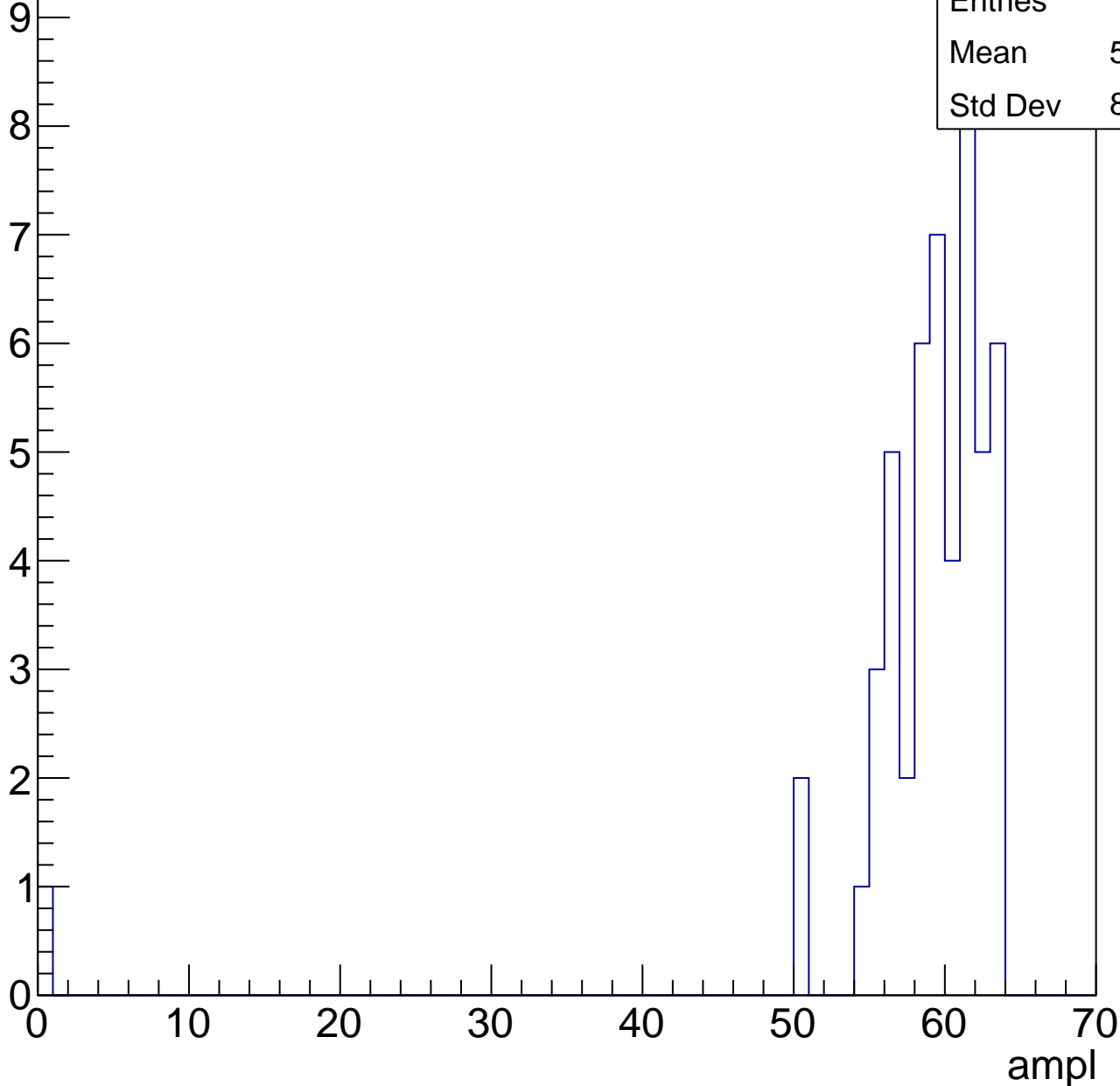


# B1L101S, U3-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

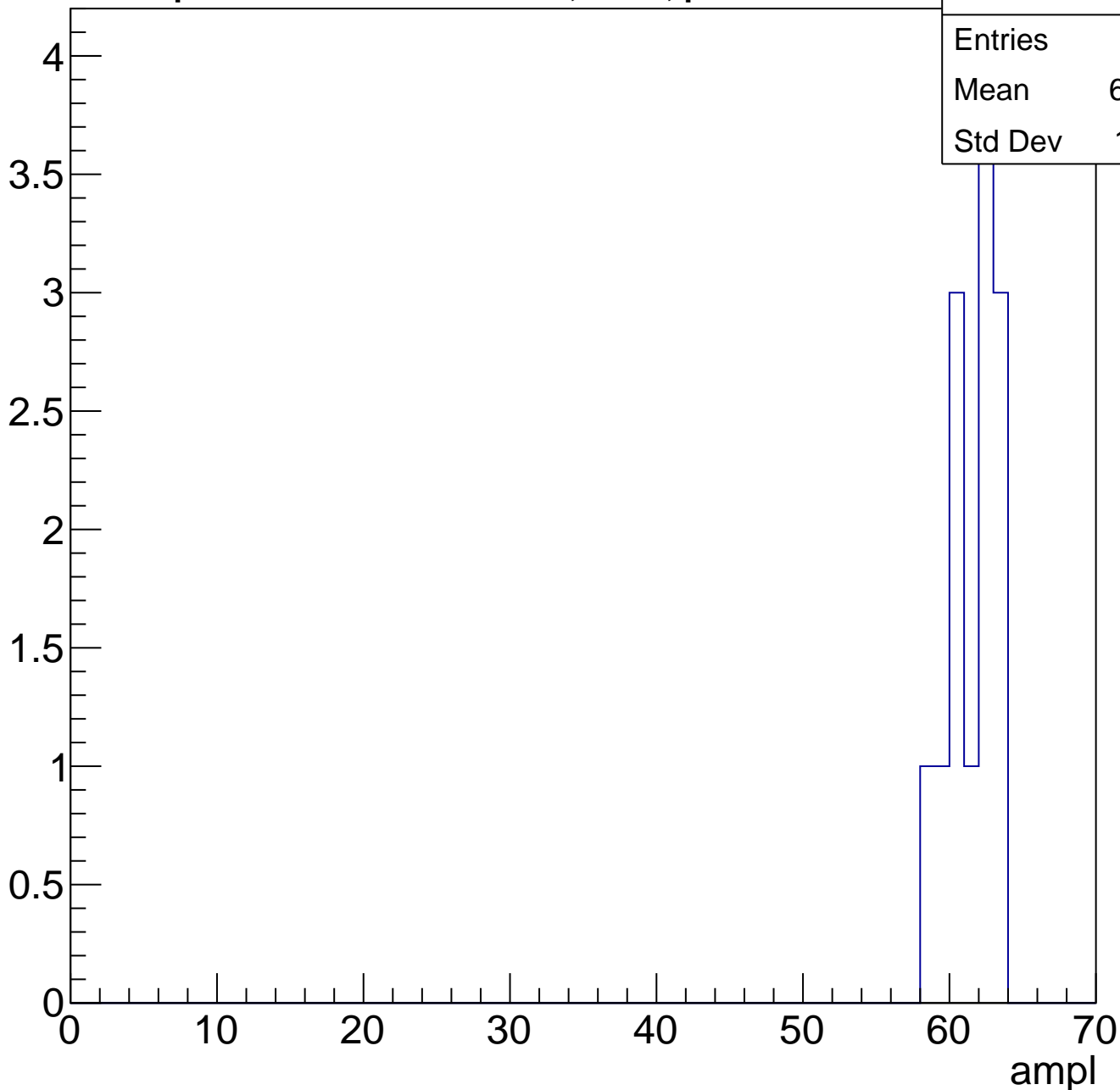
Entries	51
Mean	57.86
Std Dev	8.734



# B1L101S, U3-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U3-ch65, adc0

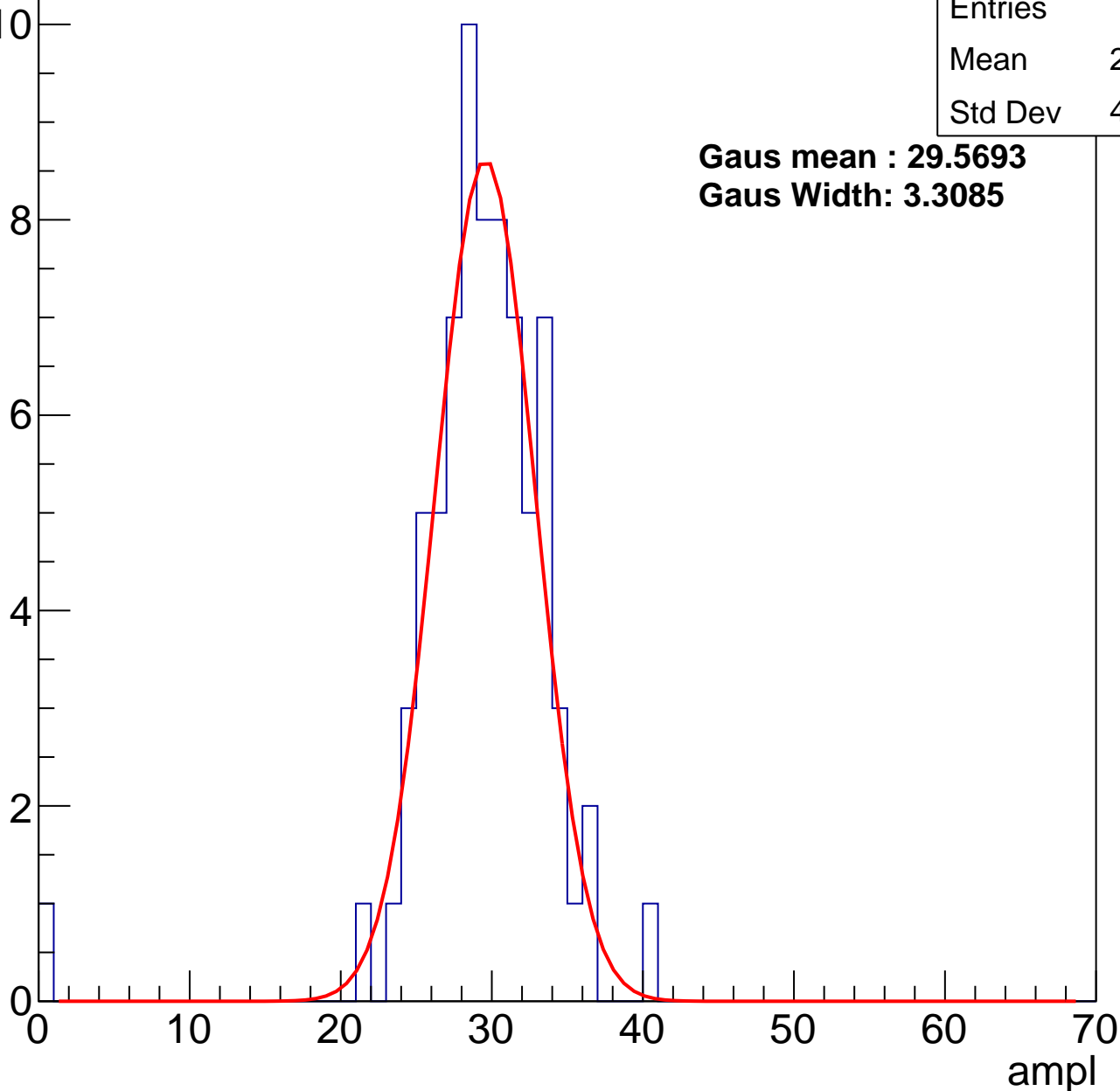
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	28.92
Std Dev	4.763

**Gaus mean : 29.5693**

**Gaus Width: 3.3085**



# B1L101S, U3-ch65, adc1

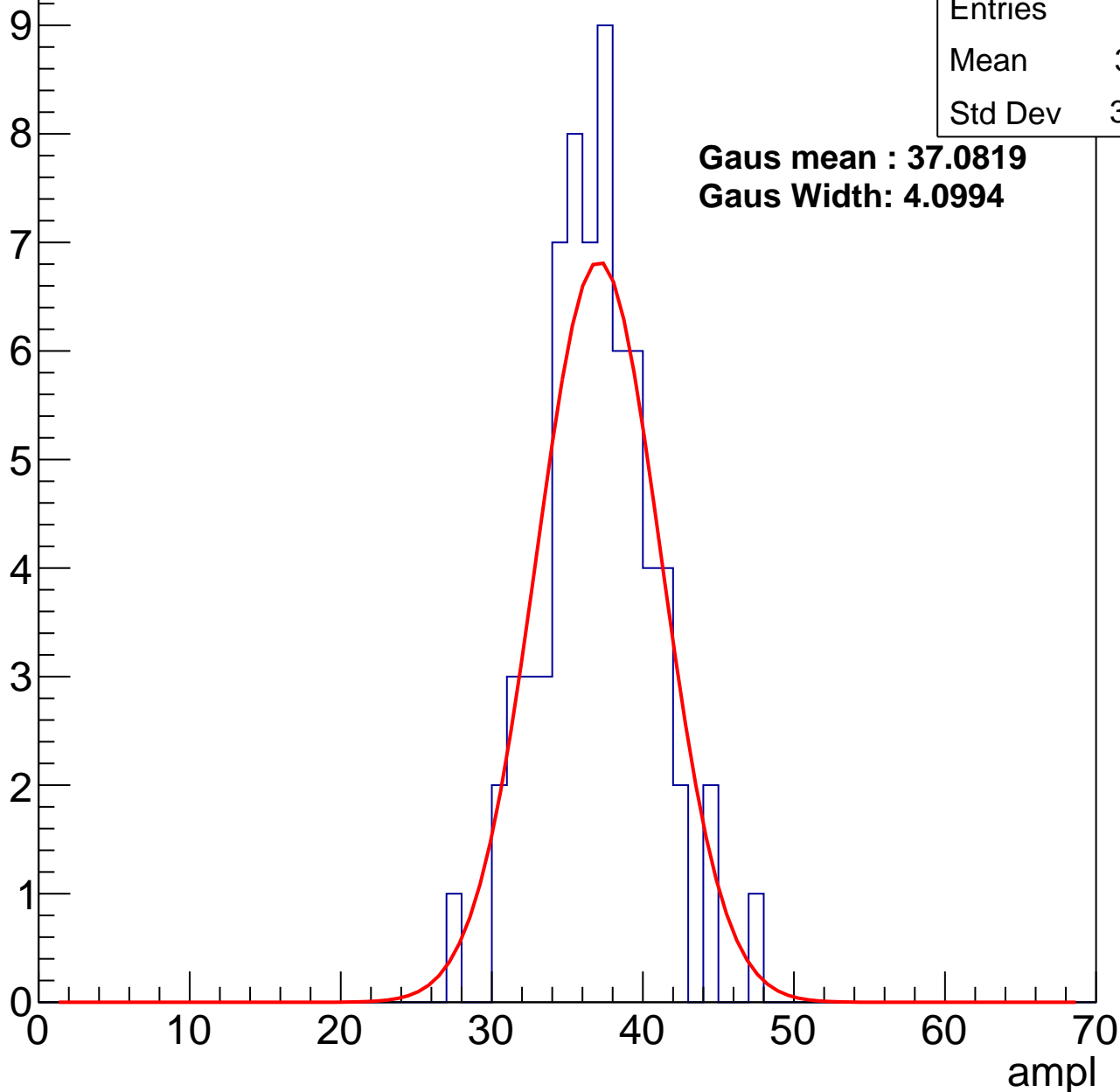
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	36.51
Std Dev	3.624

**Gaus mean : 37.0819**

**Gaus Width: 4.0994**



# B1L101S, U3-ch65, adc2

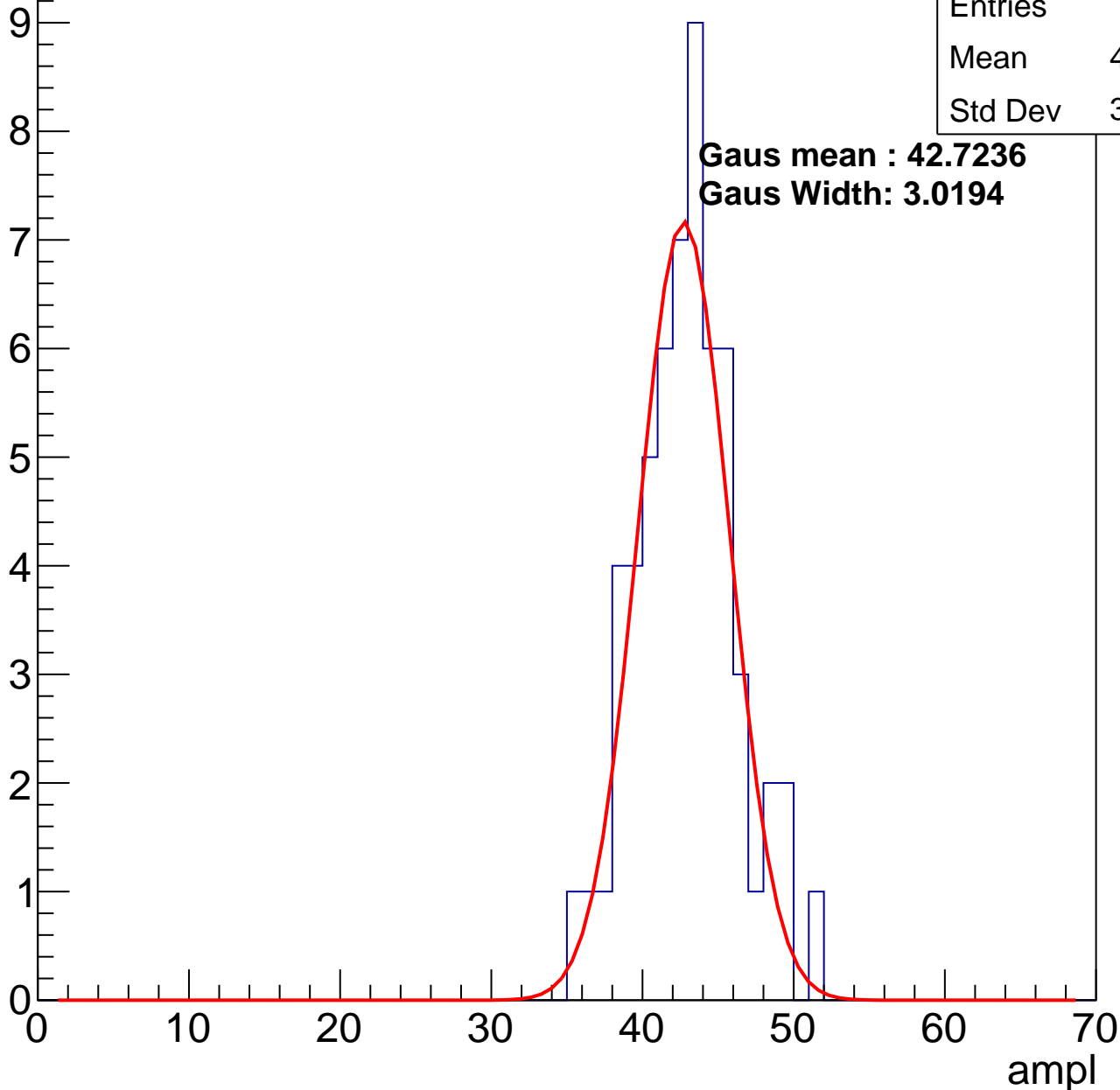
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	42.49
Std Dev	3.275

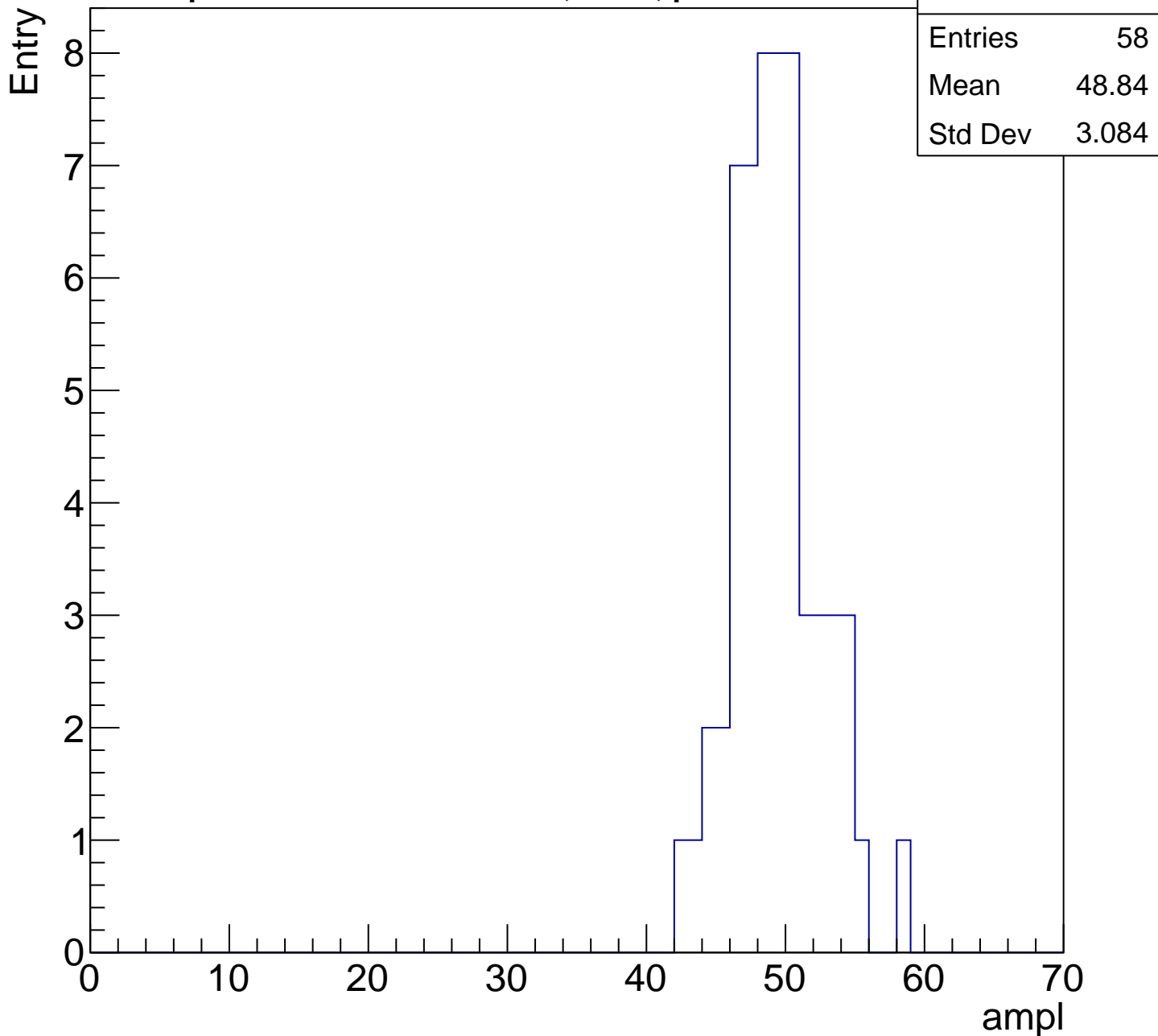
**Gaus mean : 42.7236**

**Gaus Width: 3.0194**



# B1L101S, U3-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

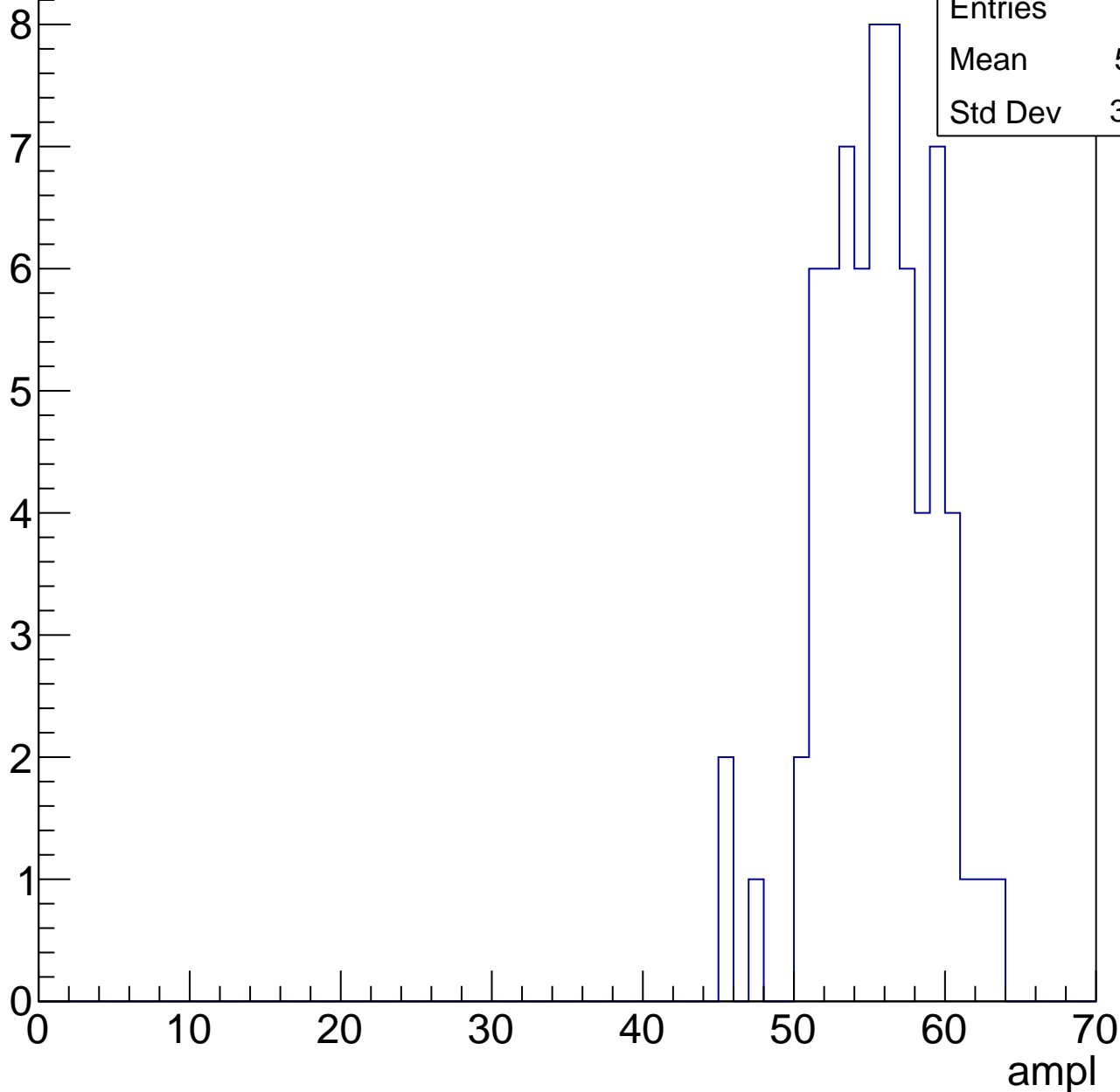


# B1L101S, U3-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	55.01
Std Dev	3.639

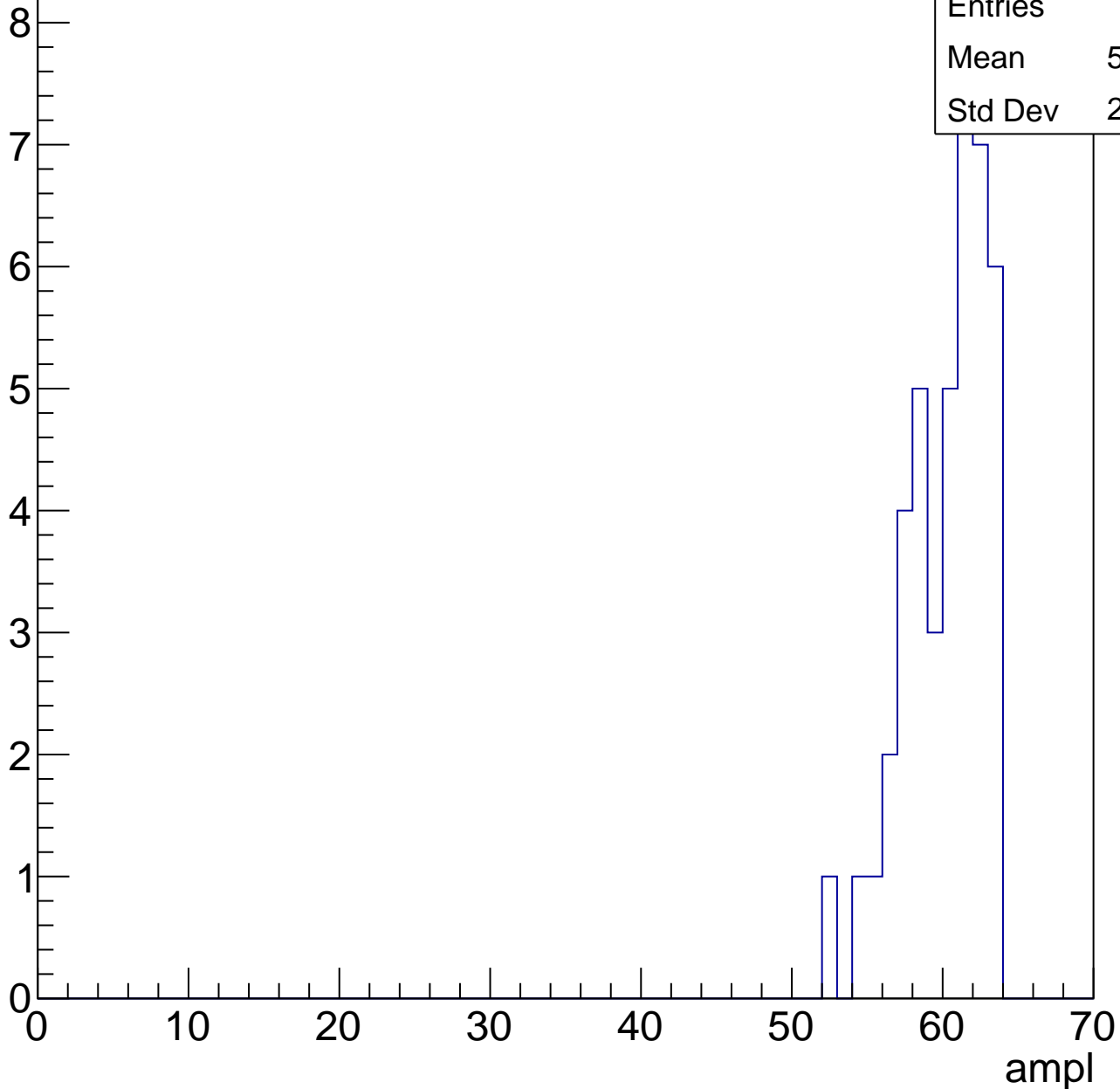


# B1L101S, U3-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

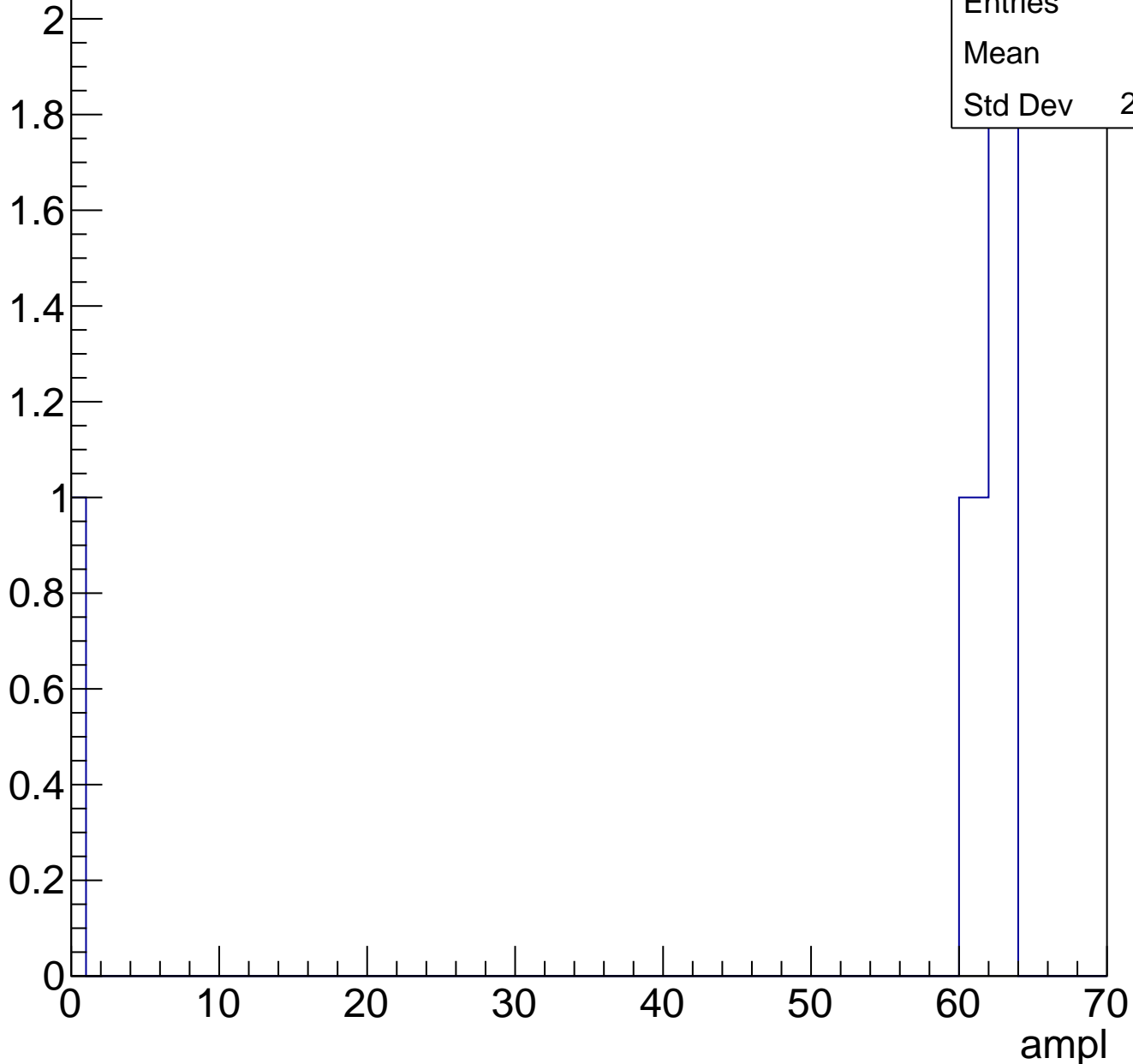
Entries	43
Mean	59.72
Std Dev	2.653



# B1L101S, U3-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

1

Mean

63

Std Dev

0

# B1L101S, U3-ch66, adc0

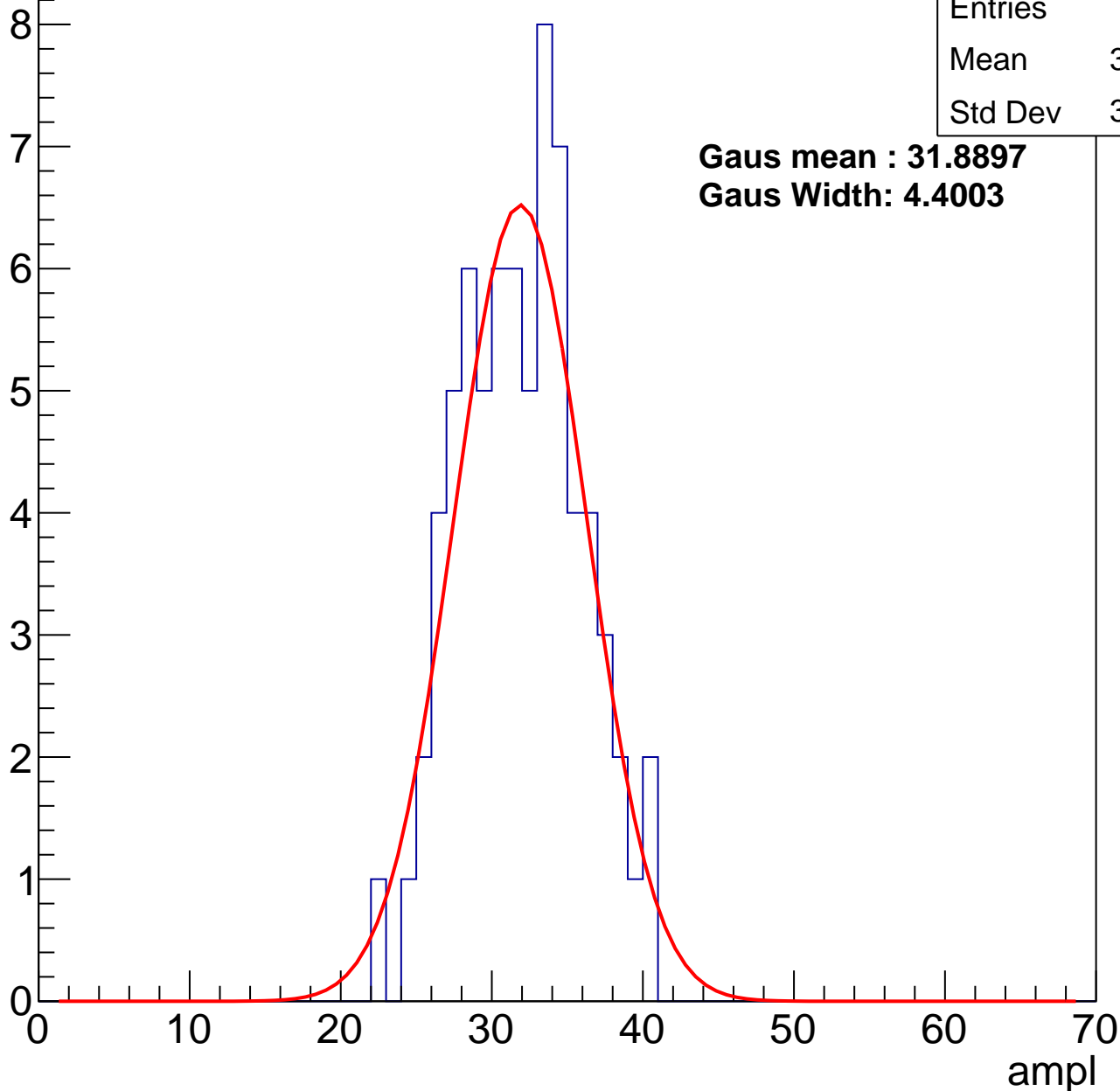
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	31.47
Std Dev	3.983

**Gaus mean : 31.8897**

**Gaus Width: 4.4003**



# B1L101S, U3-ch66, adc1

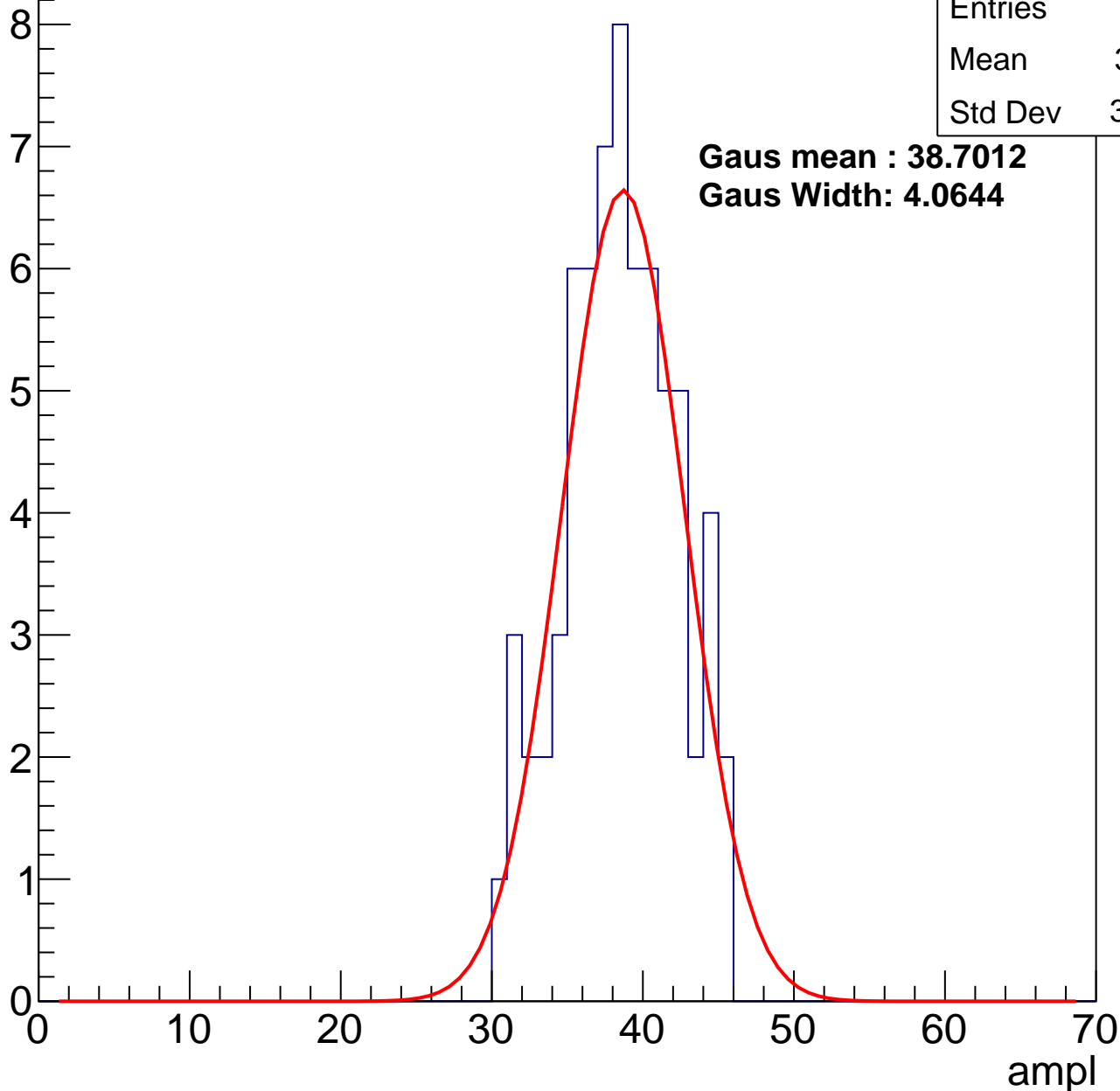
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	38.01
Std Dev	3.664

**Gaus mean : 38.7012**

**Gaus Width: 4.0644**



# B1L101S, U3-ch66, adc2

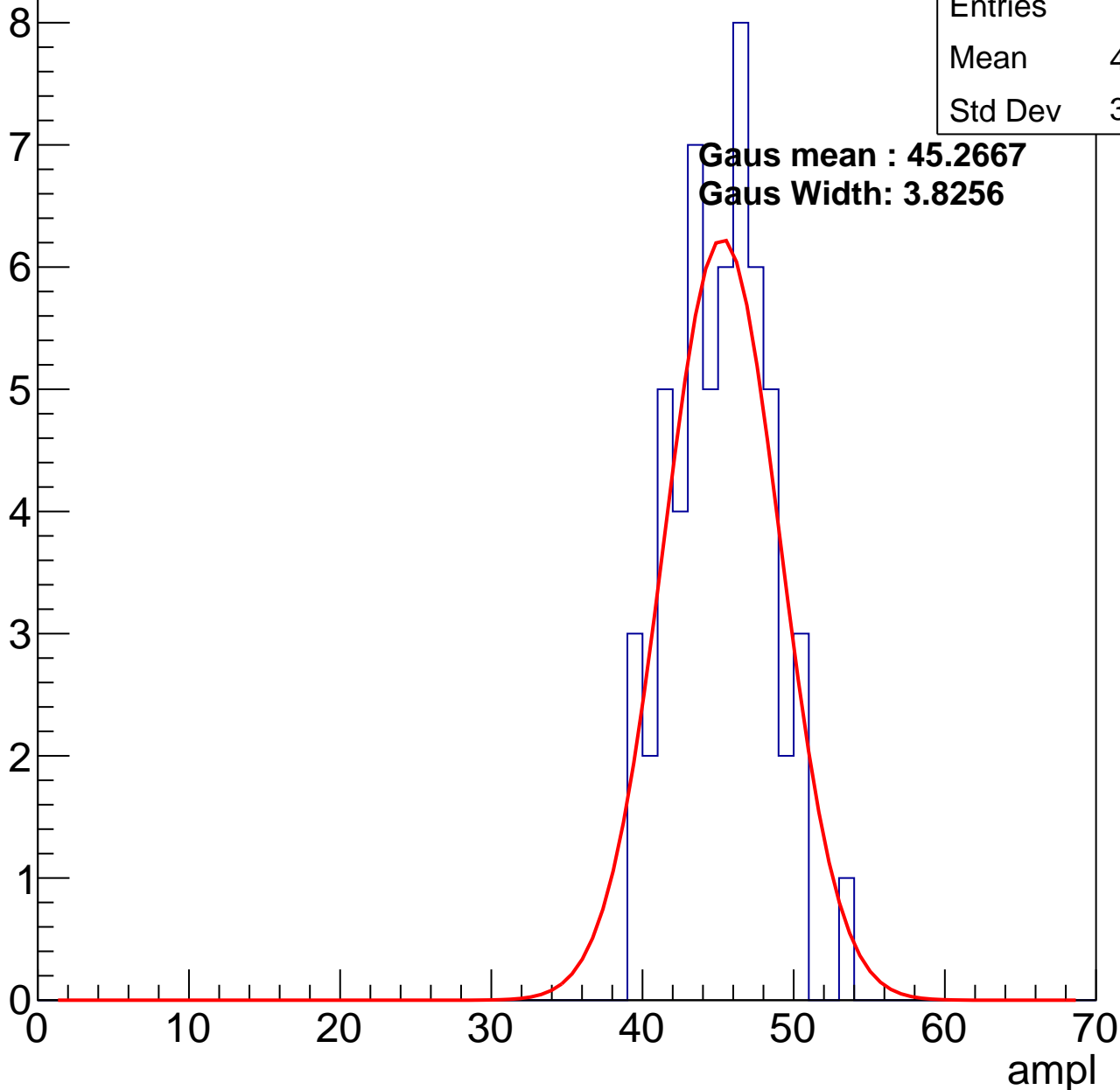
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	44.77
Std Dev	3.112

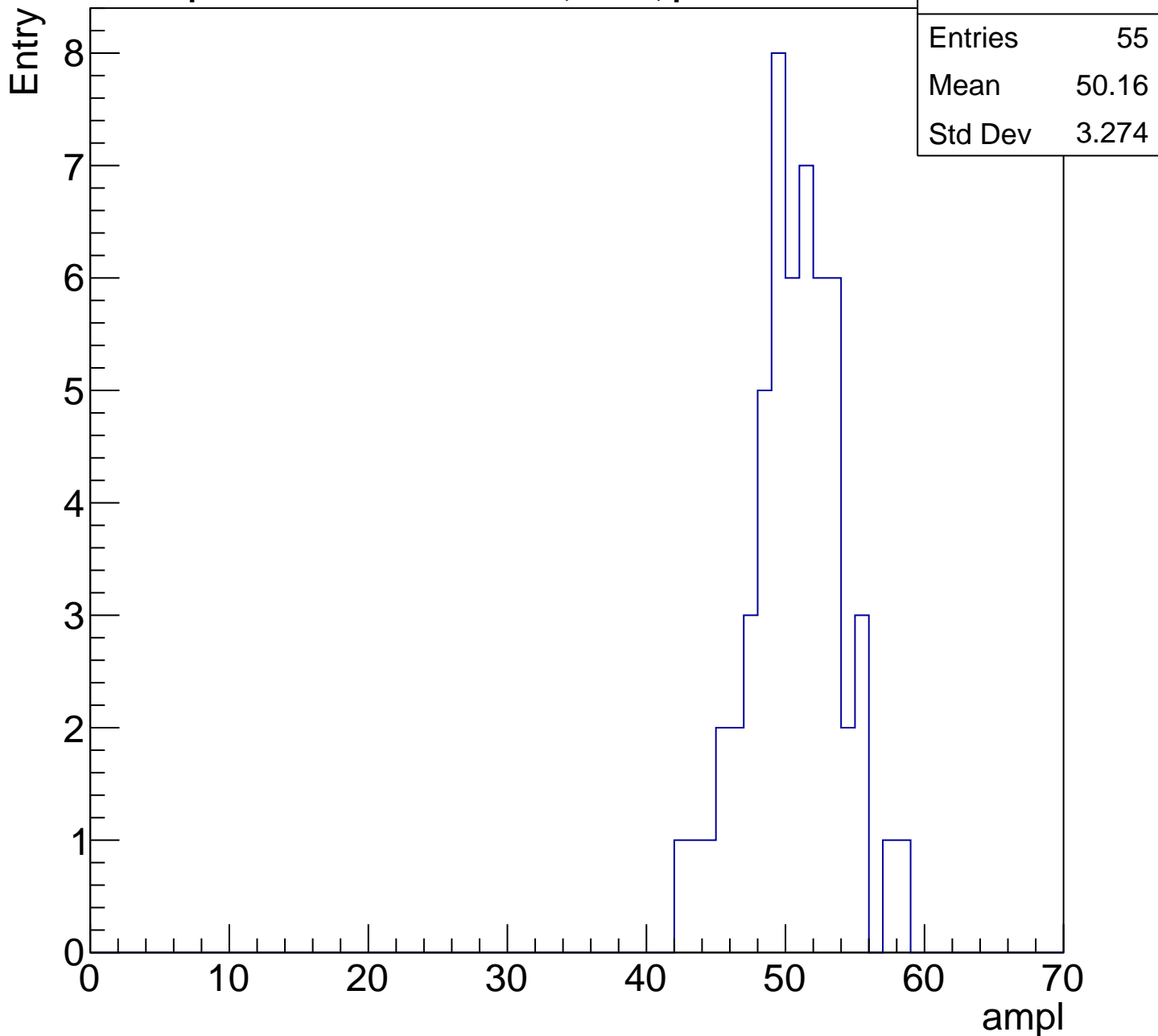
**Gaus mean : 45.2667**

**Gaus Width: 3.8256**



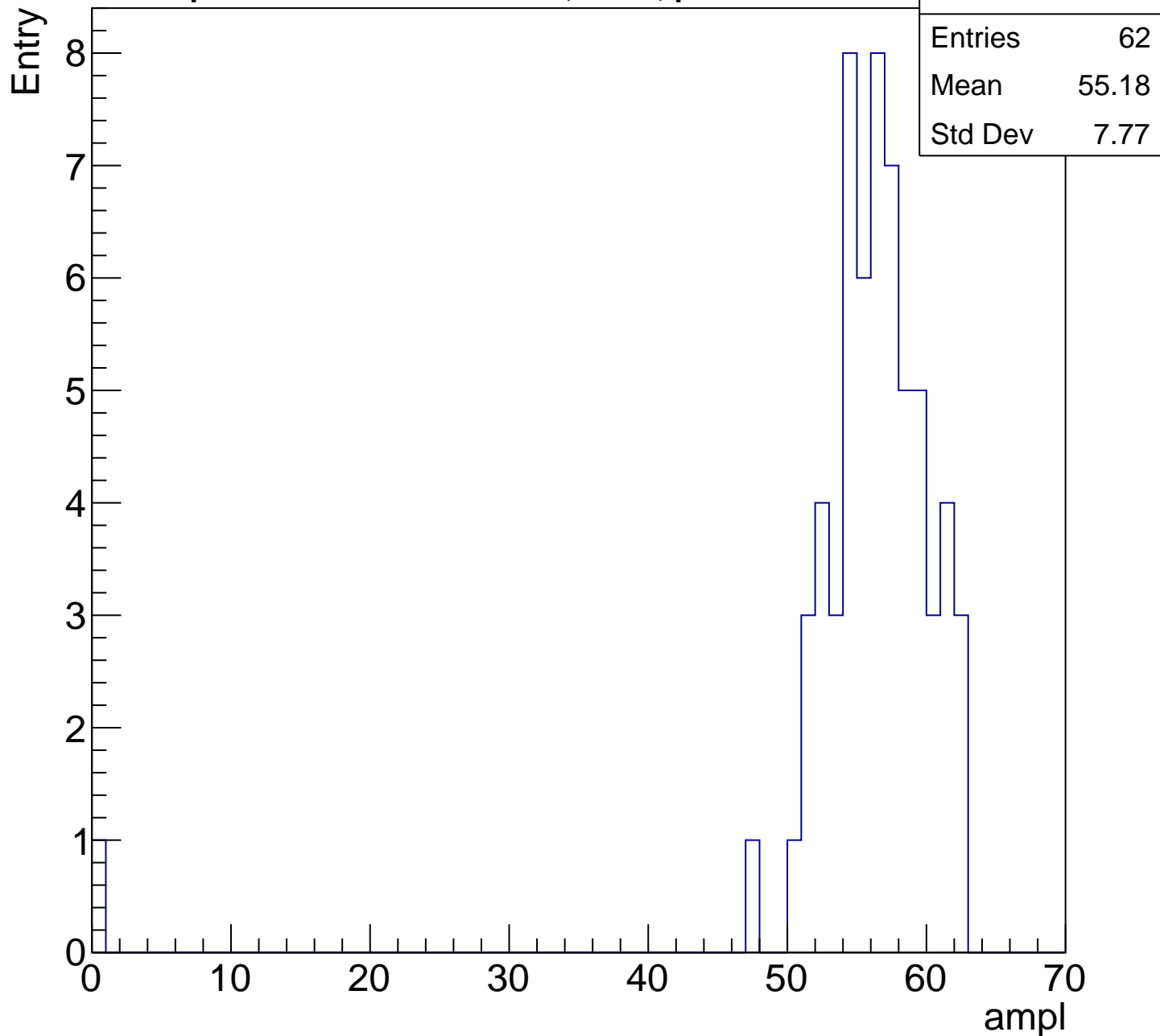
# B1L101S, U3-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

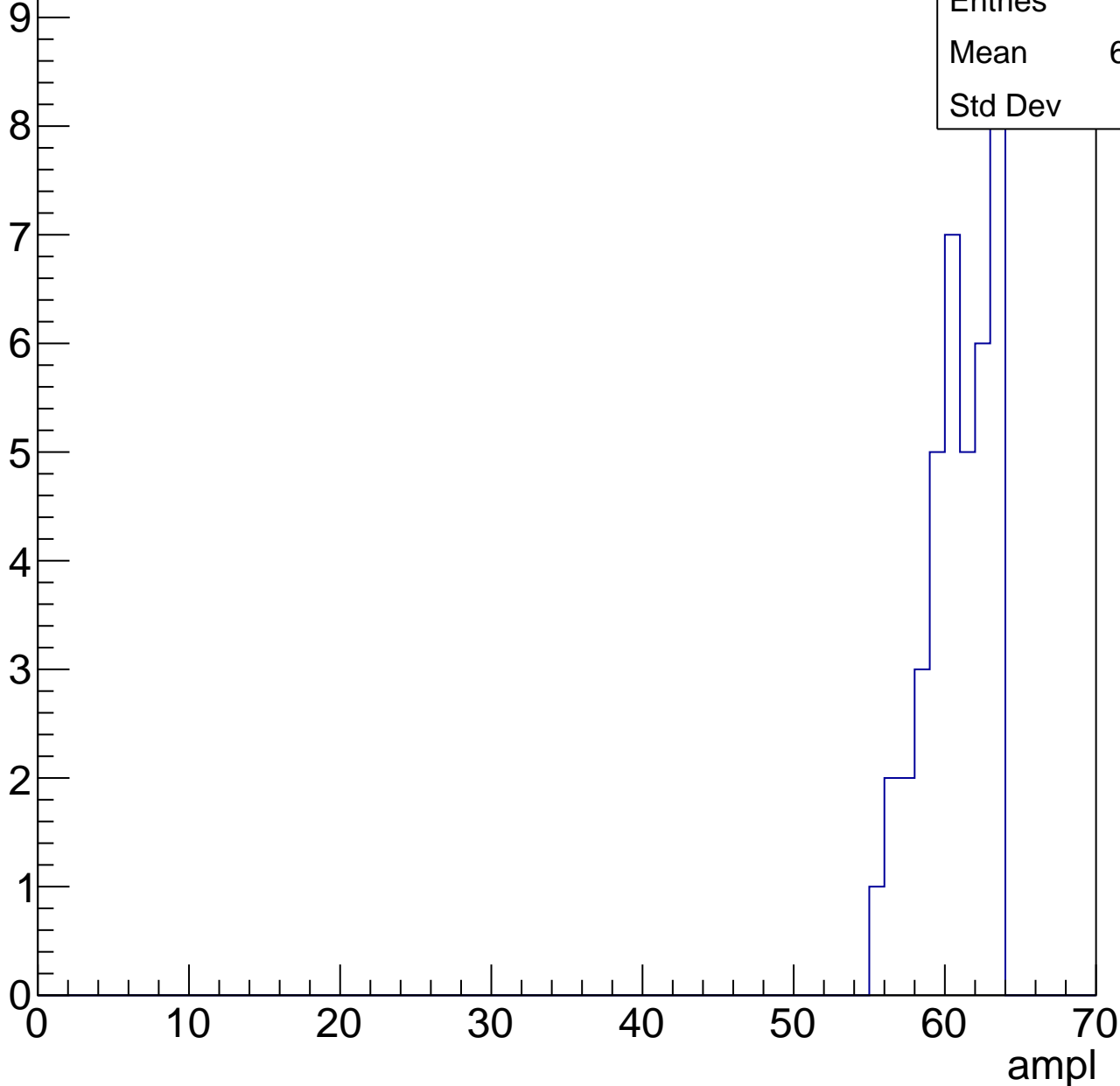


# B1L101S, U3-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

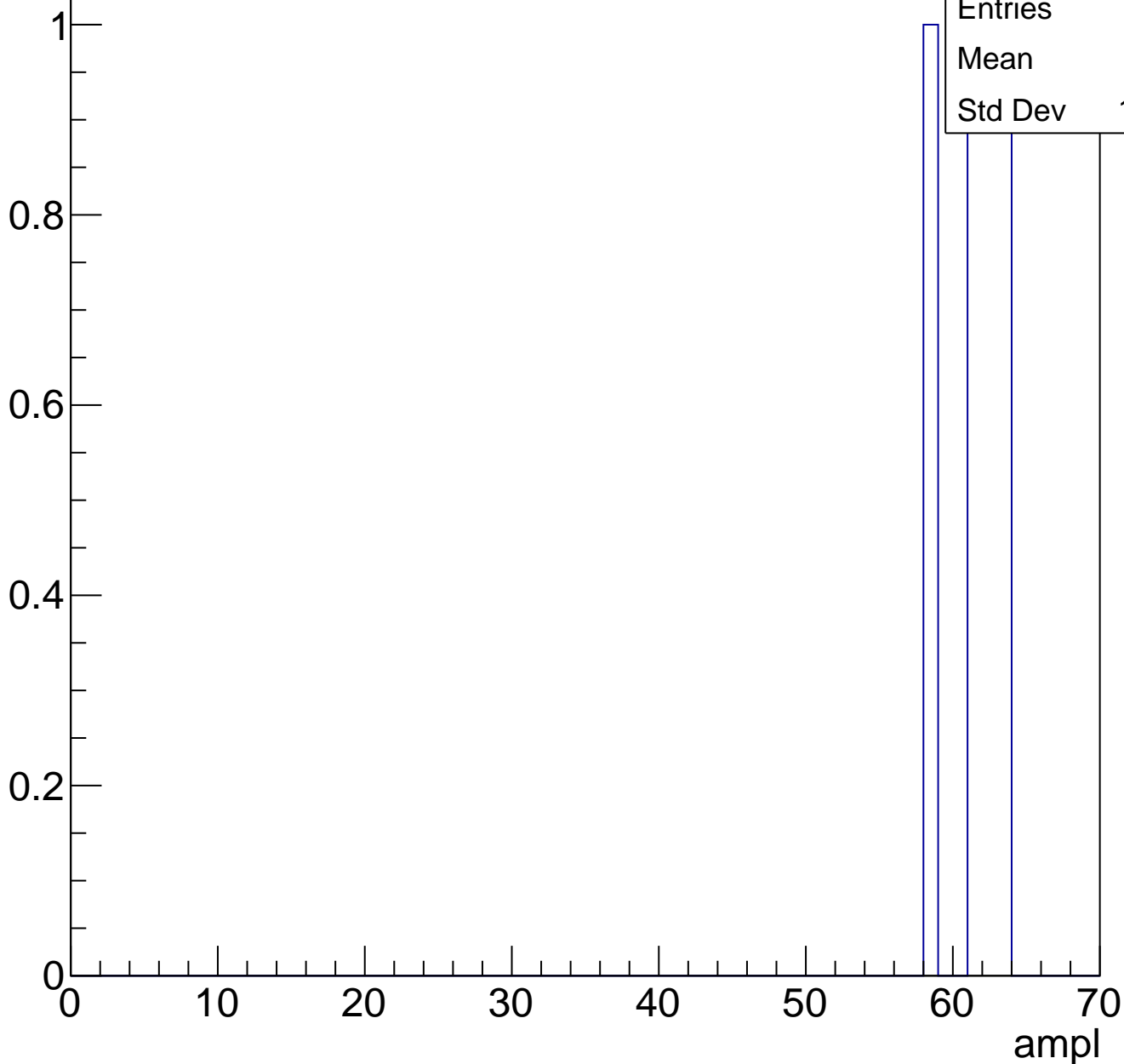
Entries	40
Mean	60.35
Std Dev	2.22



# B1L101S, U3-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch67, adc0

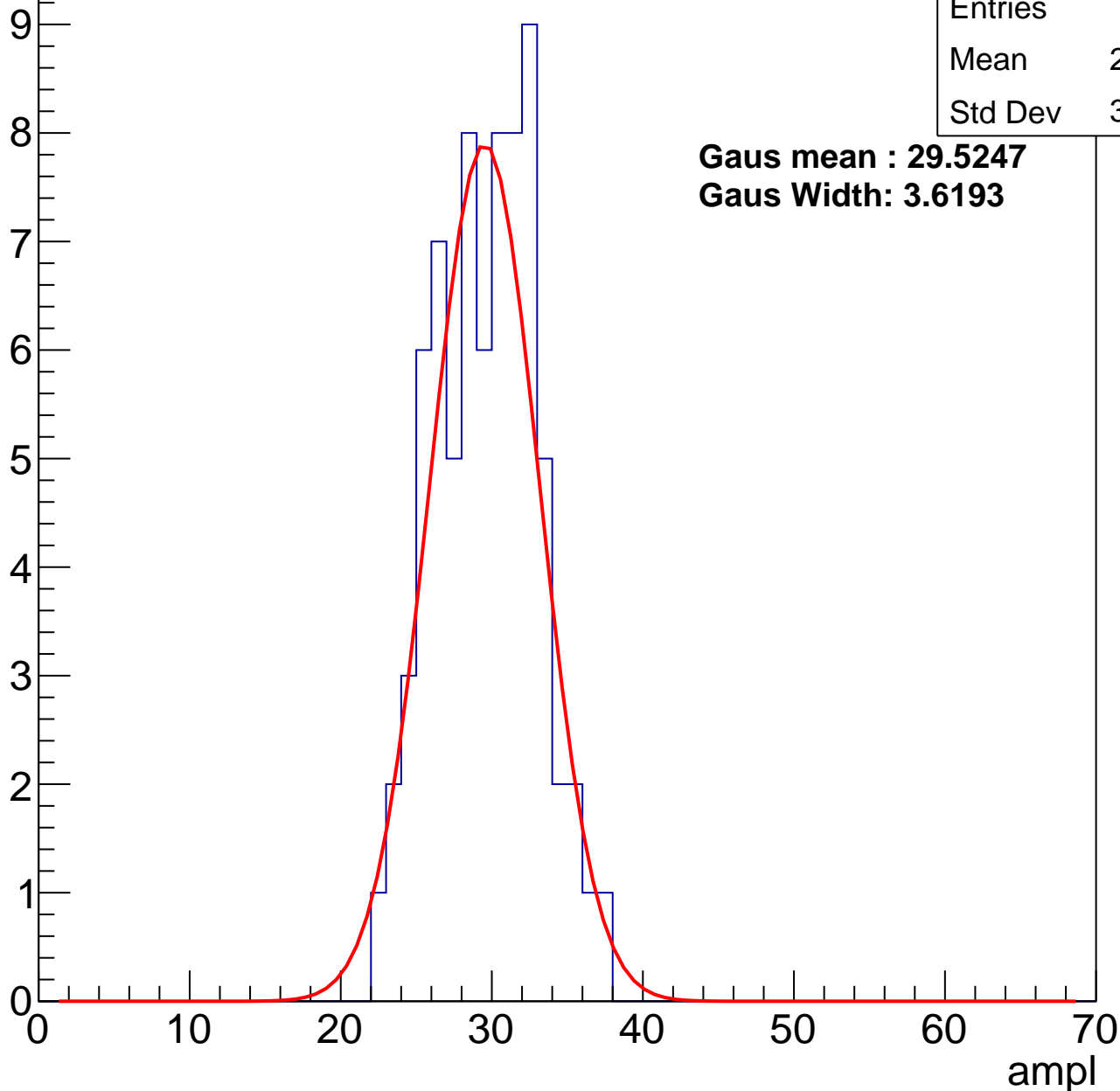
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	29.15
Std Dev	3.323

**Gaus mean : 29.5247**

**Gaus Width: 3.6193**



# B1L101S, U3-ch67, adc1

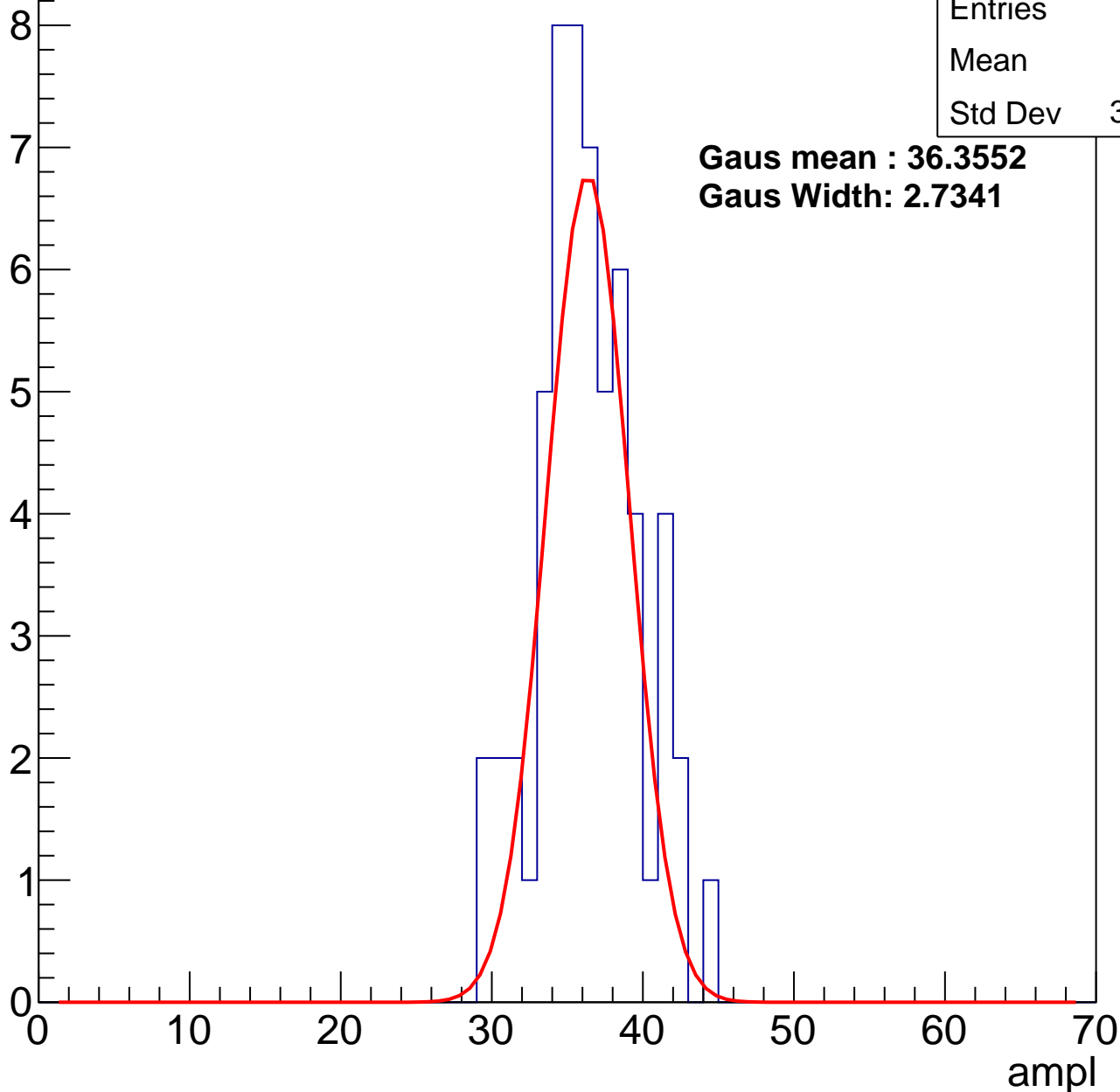
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	35.9
Std Dev	3.315

**Gaus mean : 36.3552**

**Gaus Width: 2.7341**



# B1L101S, U3-ch67, adc2

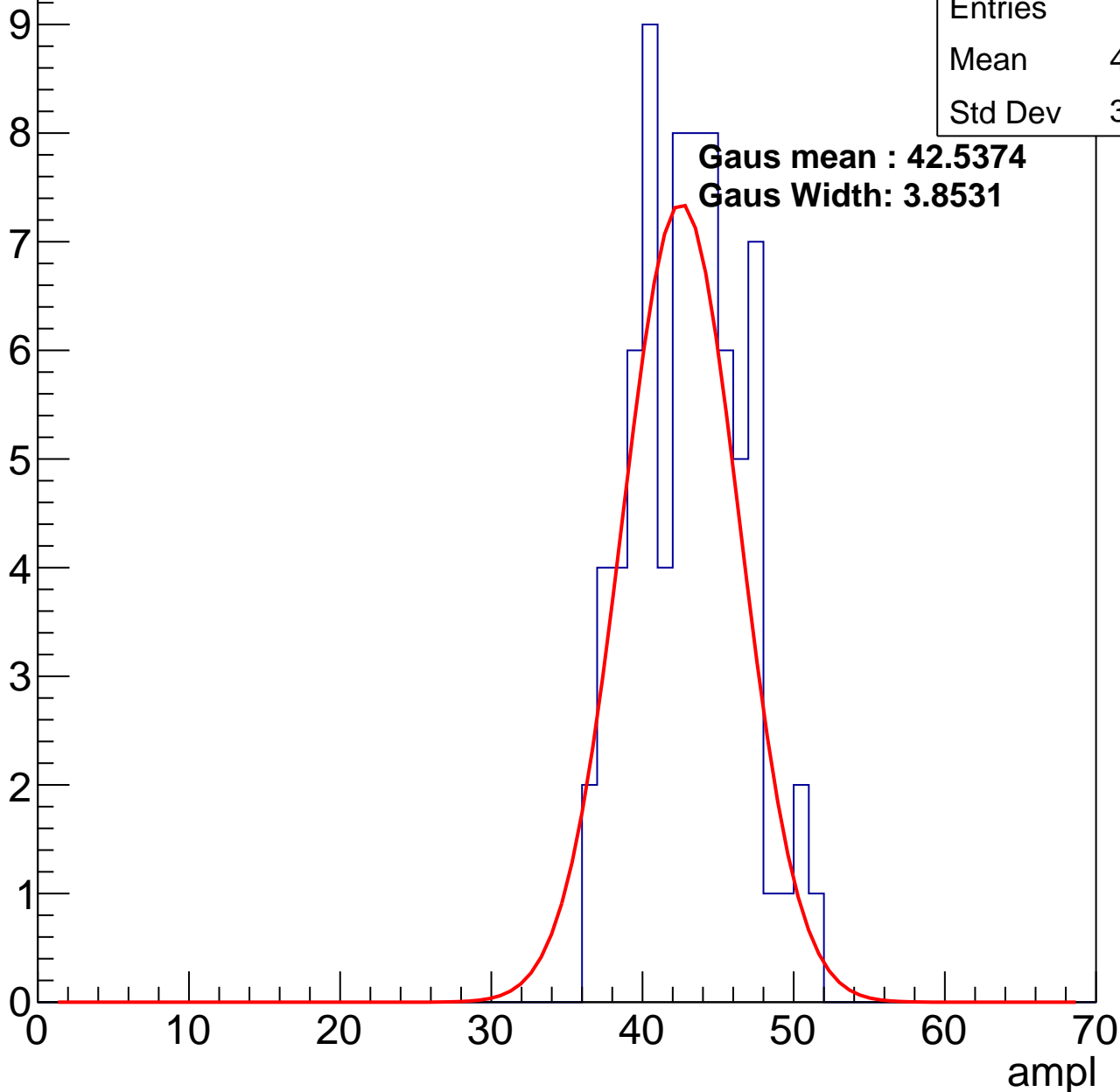
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	42.62
Std Dev	3.524

**Gaus mean : 42.5374**

**Gaus Width: 3.8531**

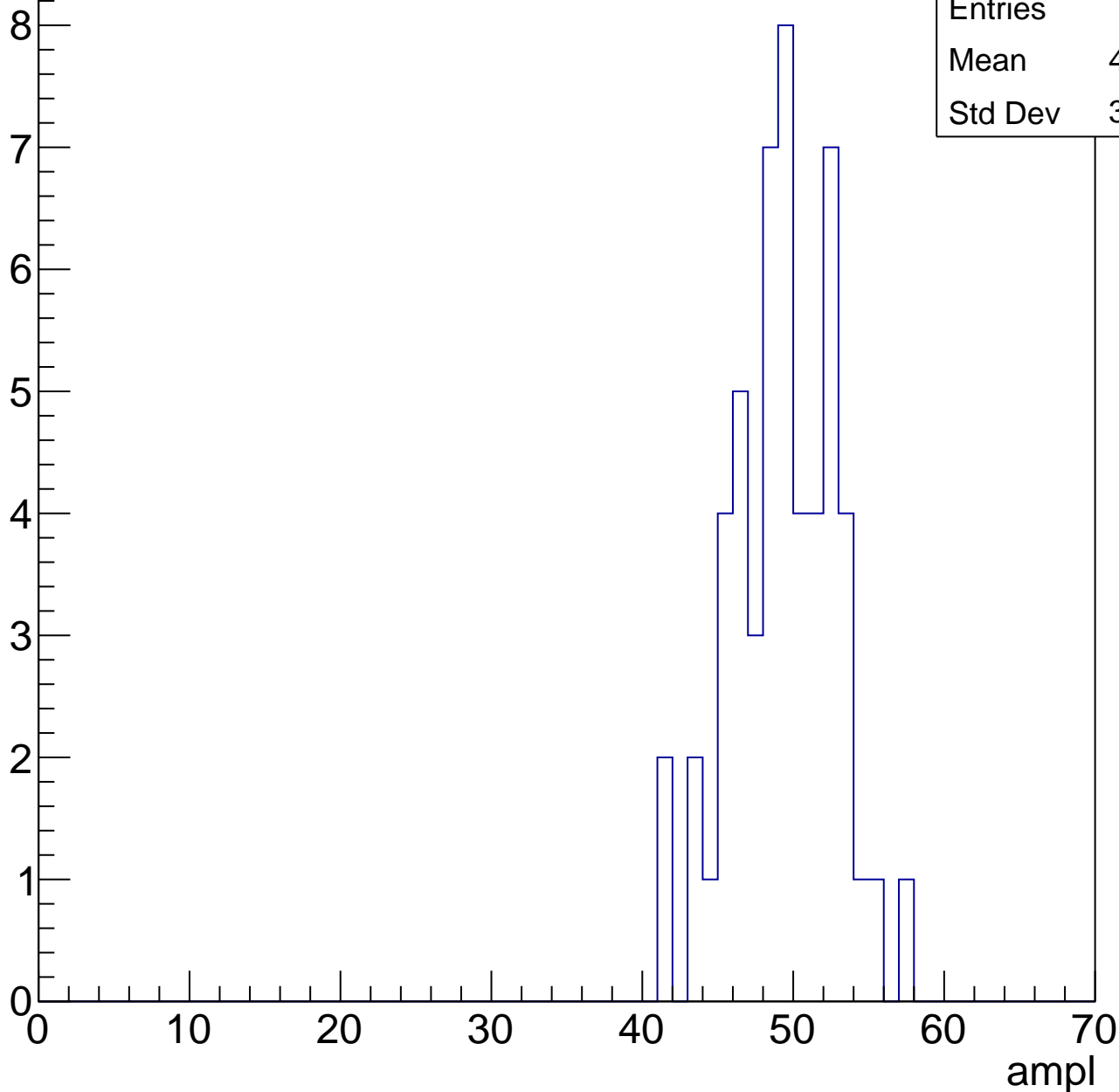


# B1L101S, U3-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	48.83
Std Dev	3.398

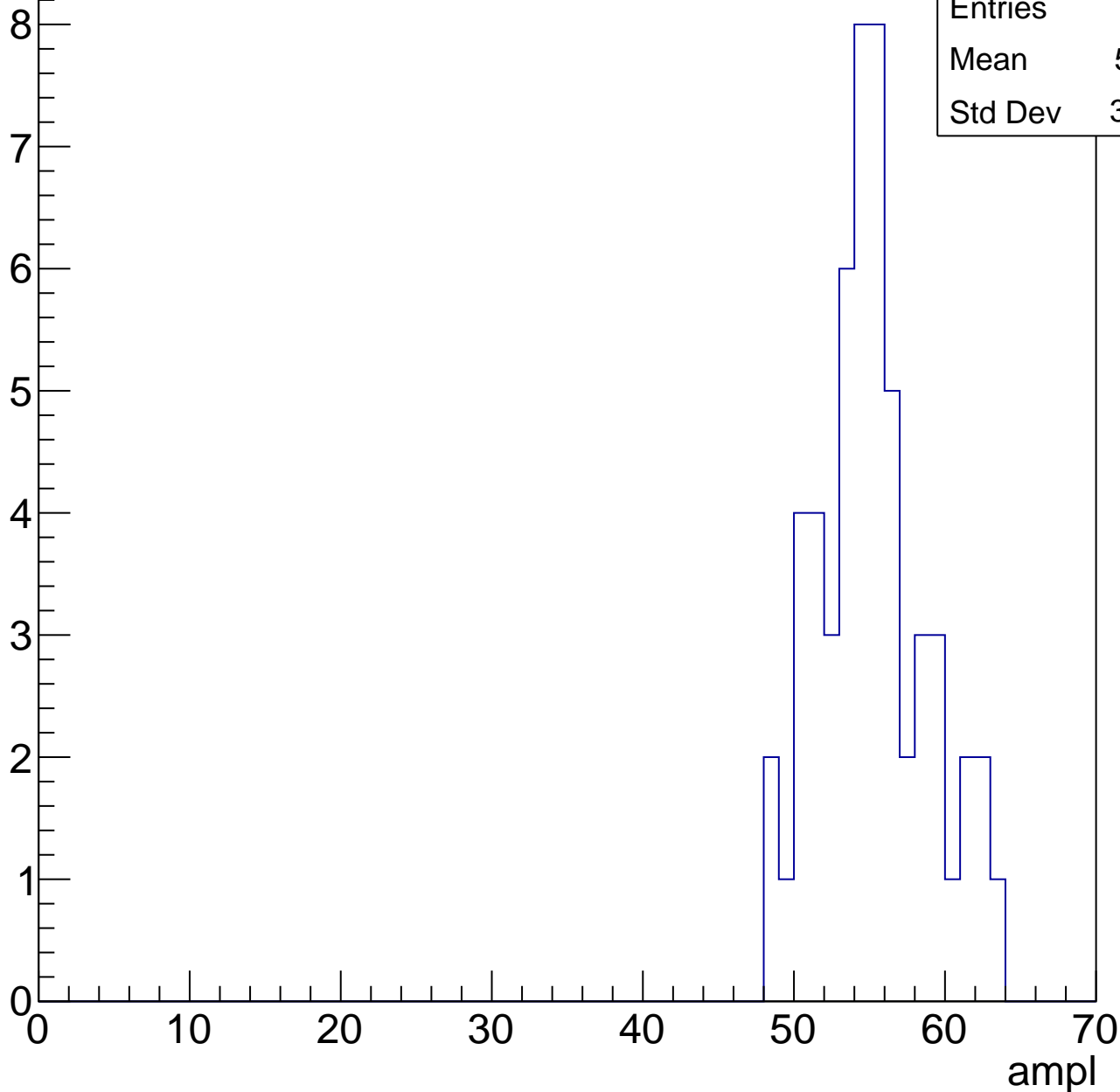


# B1L101S, U3-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	54.71
Std Dev	3.566



# B1L101S, U3-ch67, adc5

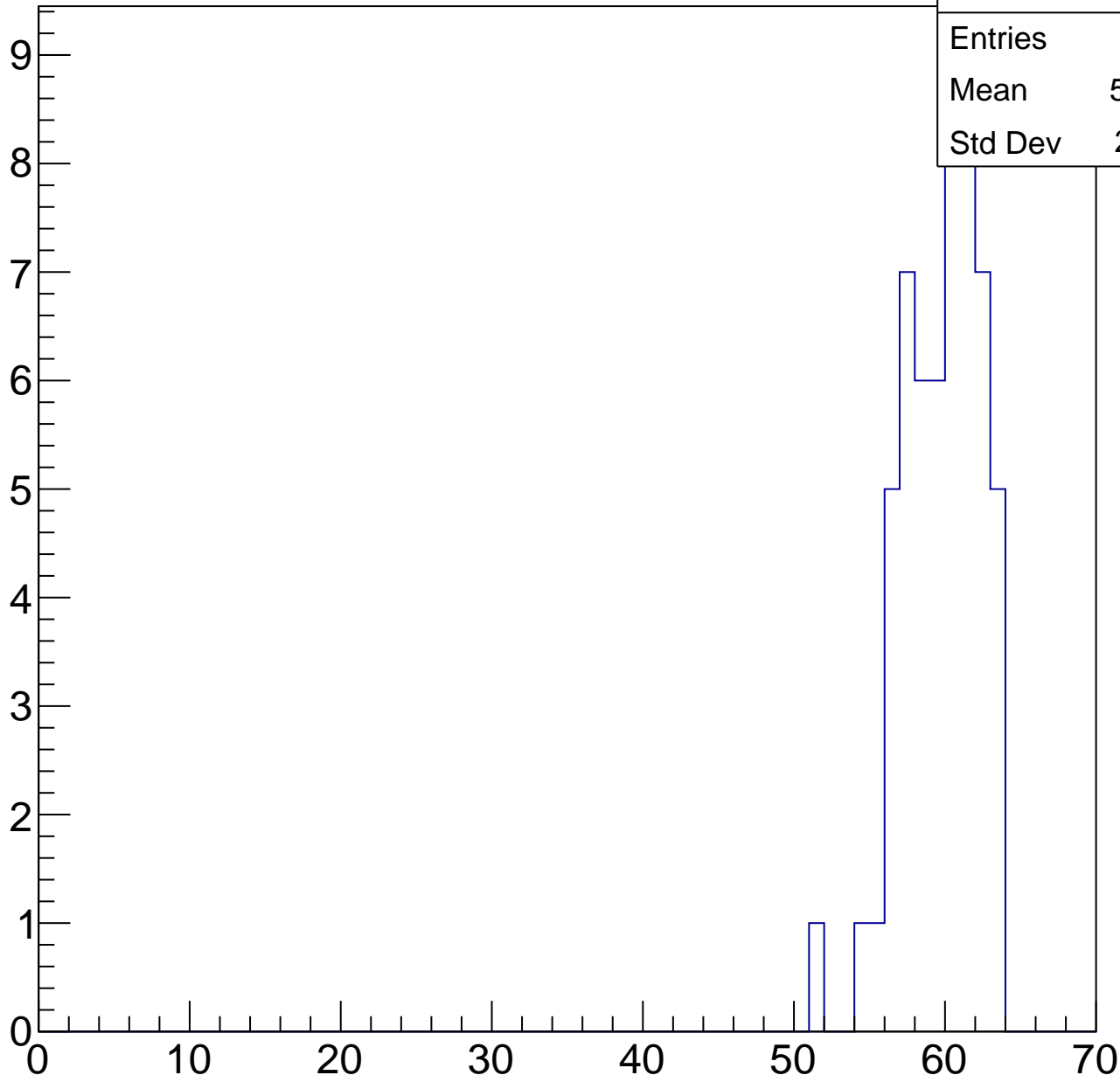
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	56
Mean	59.25
Std Dev	2.551

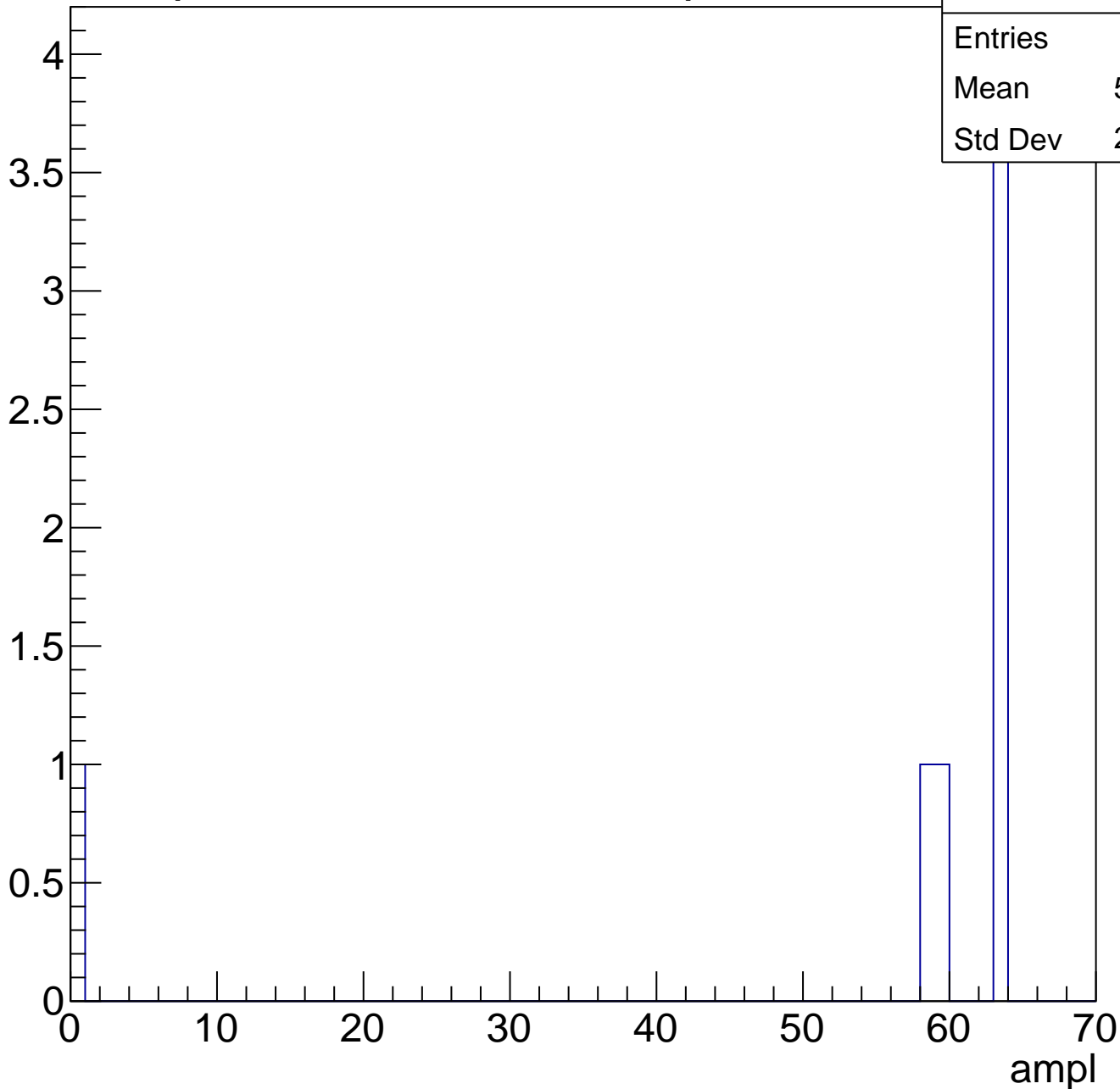
ampl



# B1L101S, U3-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

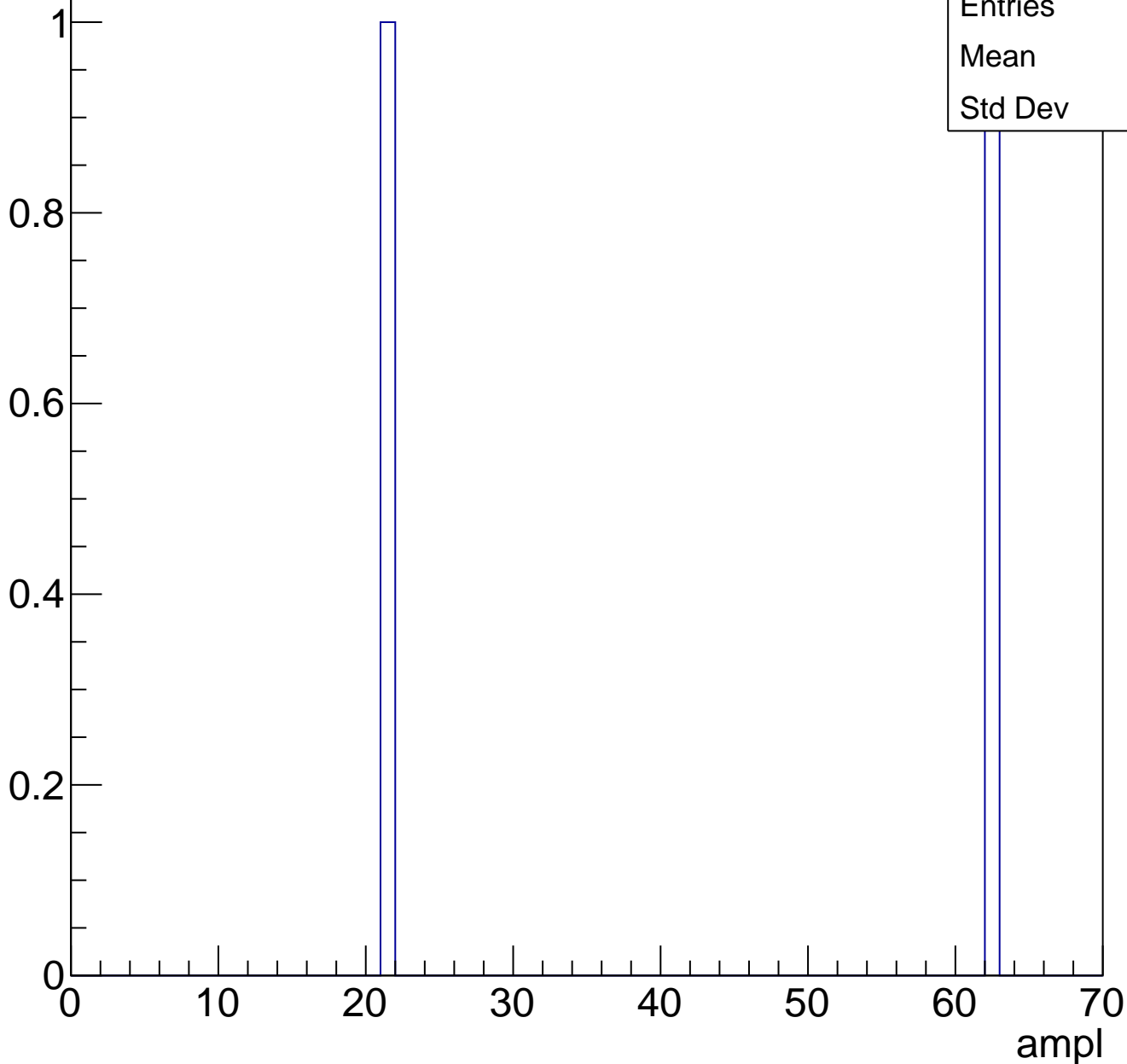




# B1L101S, U3-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch68, adc0

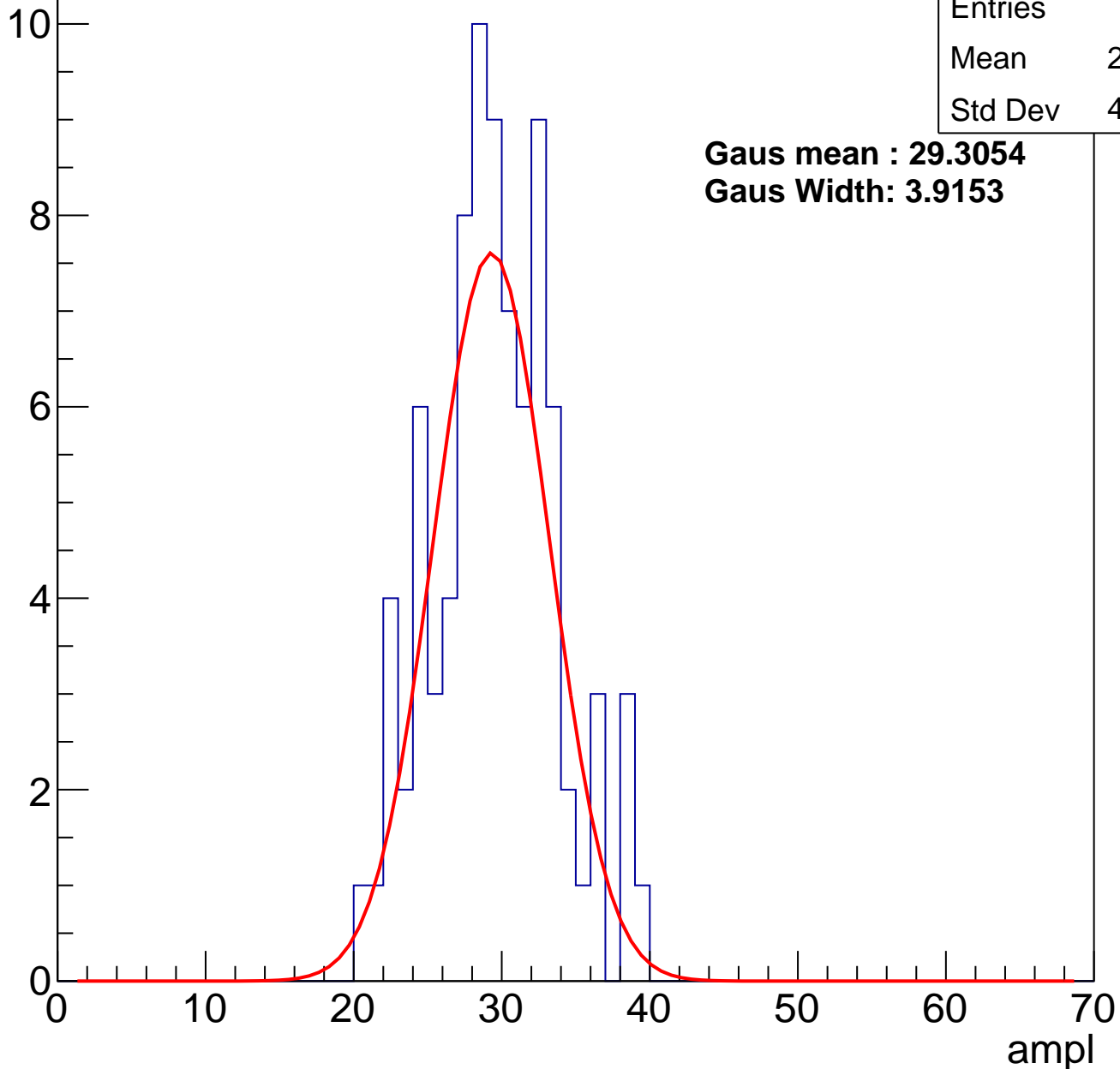
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	86
Mean	29.08
Std Dev	4.138

**Gaus mean : 29.3054**

**Gaus Width: 3.9153**

Entry



# B1L101S, U3-ch68, adc1

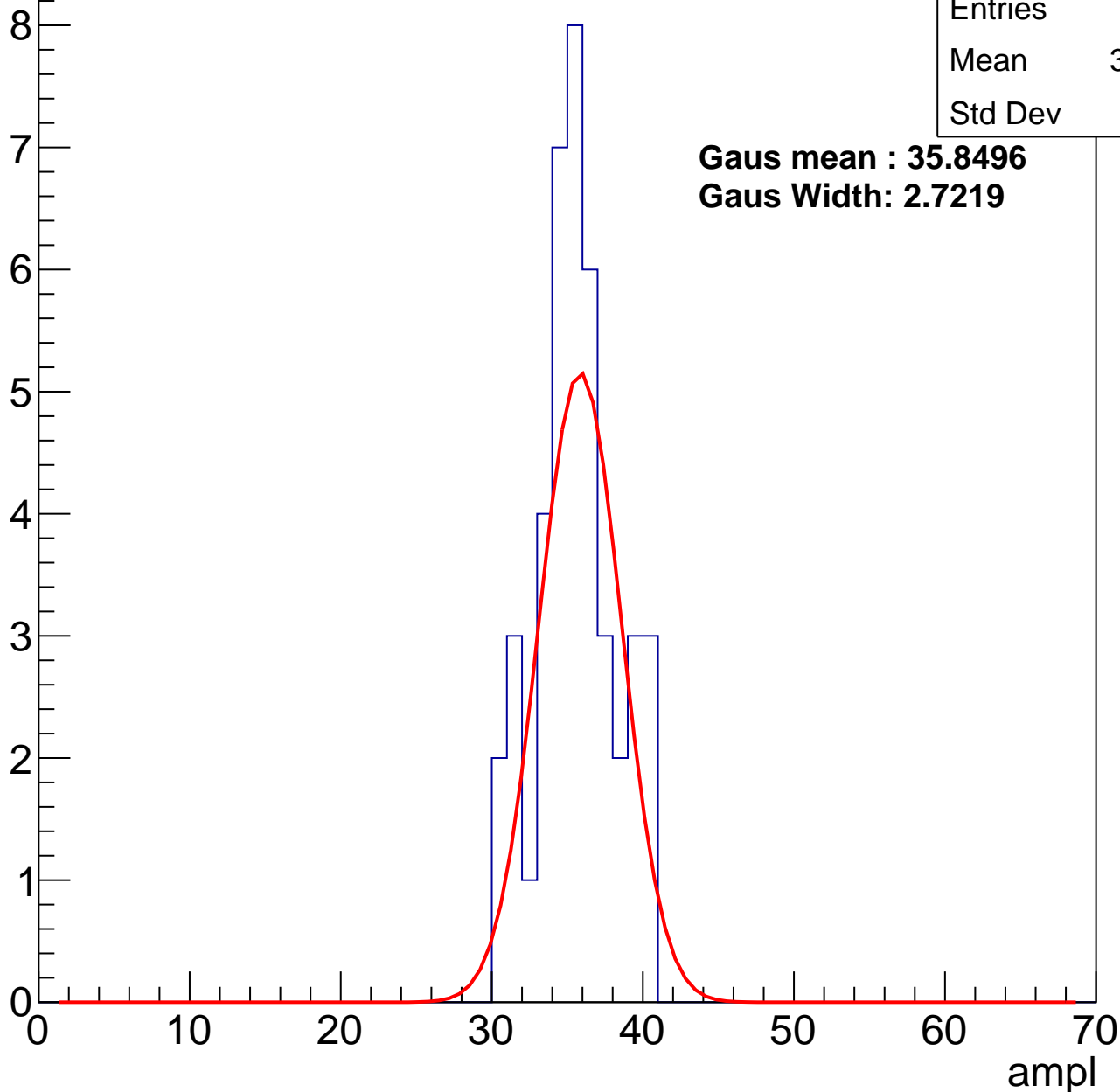
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	35.12
Std Dev	2.62

**Gaus mean : 35.8496**

**Gaus Width: 2.7219**



# B1L101S, U3-ch68, adc2

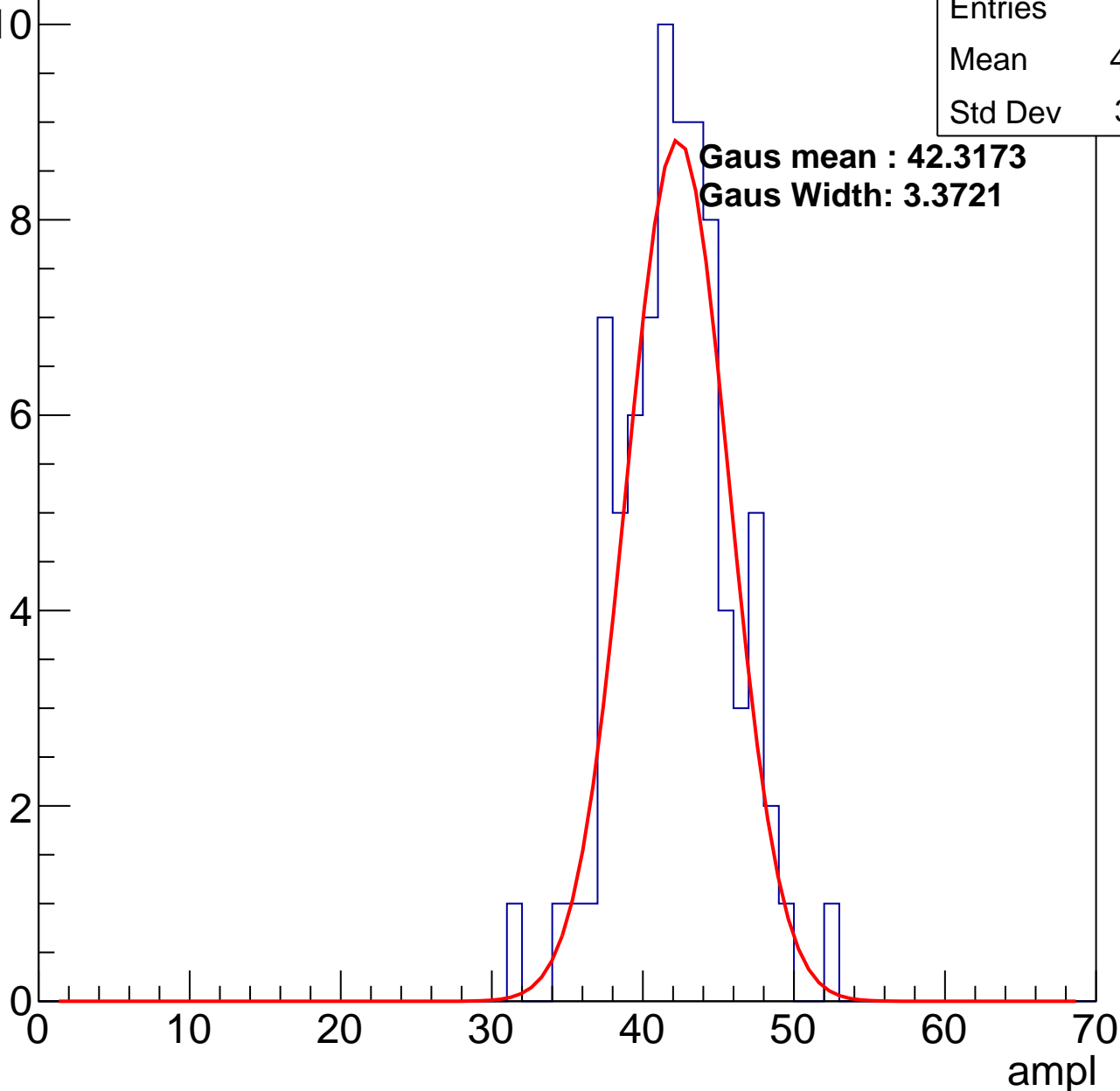
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	41.68
Std Dev	3.651

**Gaus mean : 42.3173**

**Gaus Width: 3.3721**

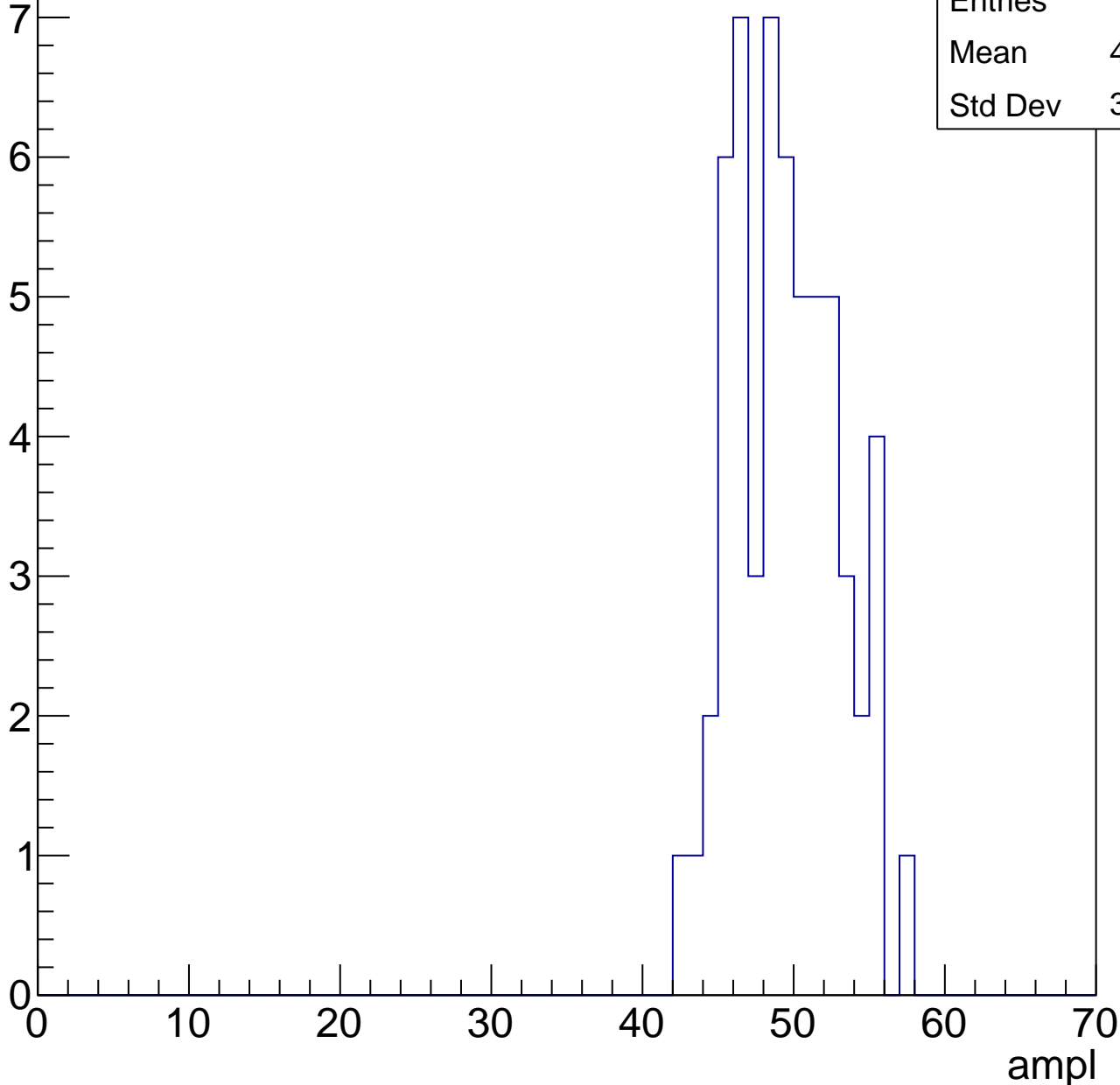


# B1L101S, U3-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	49.05
Std Dev	3.446

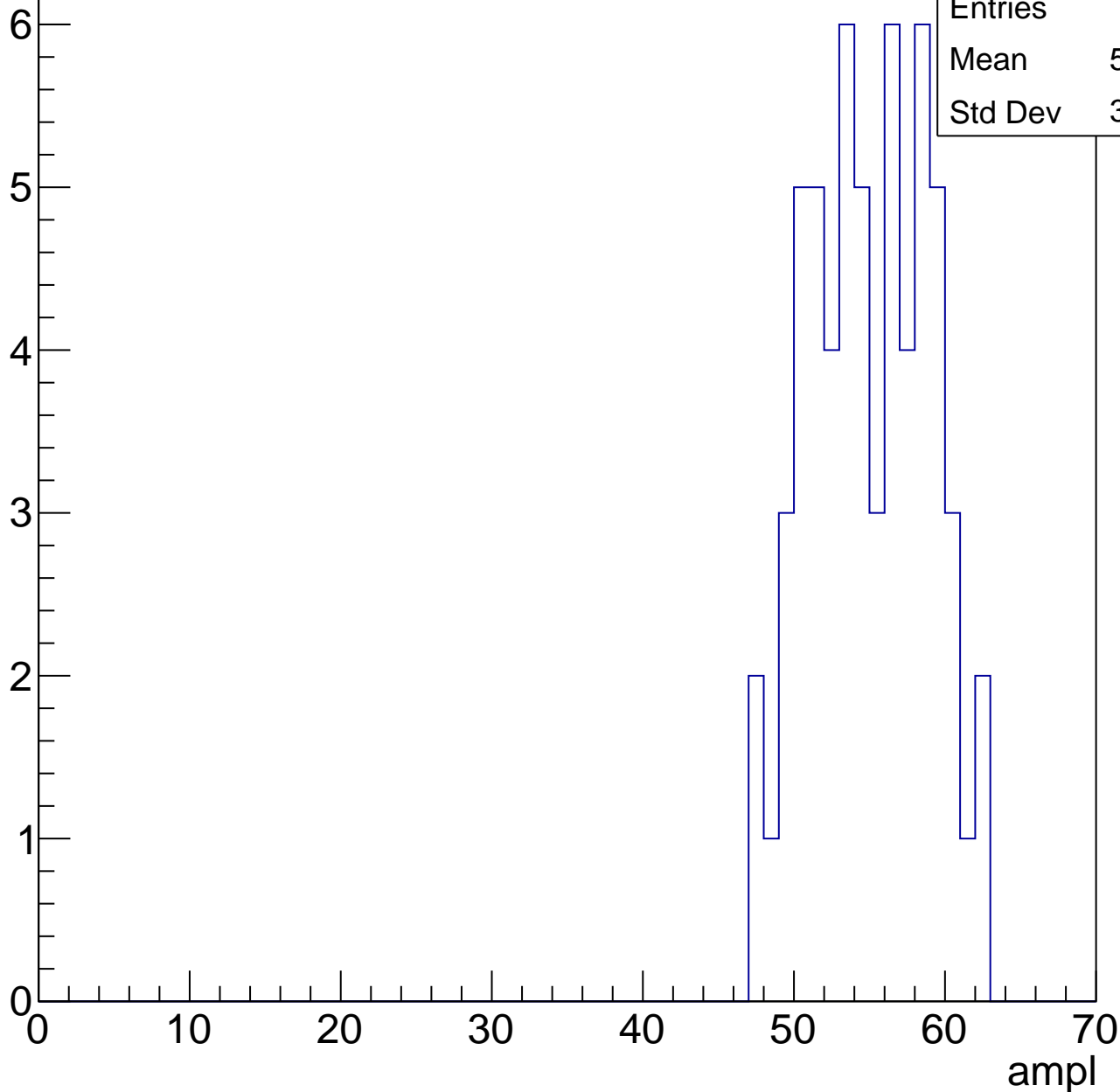


# B1L101S, U3-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	54.54
Std Dev	3.856

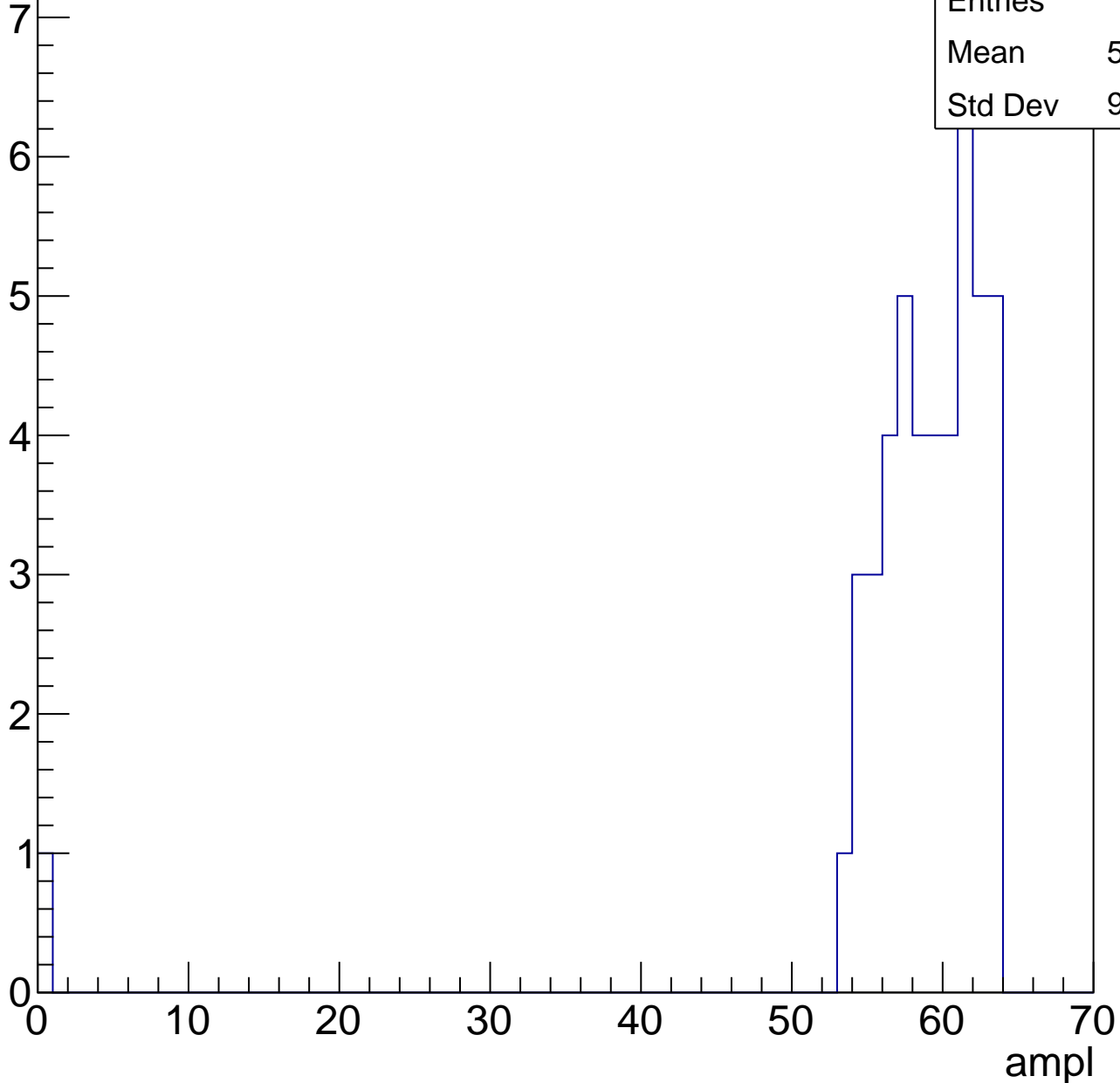


# B1L101S, U3-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	57.59
Std Dev	9.047

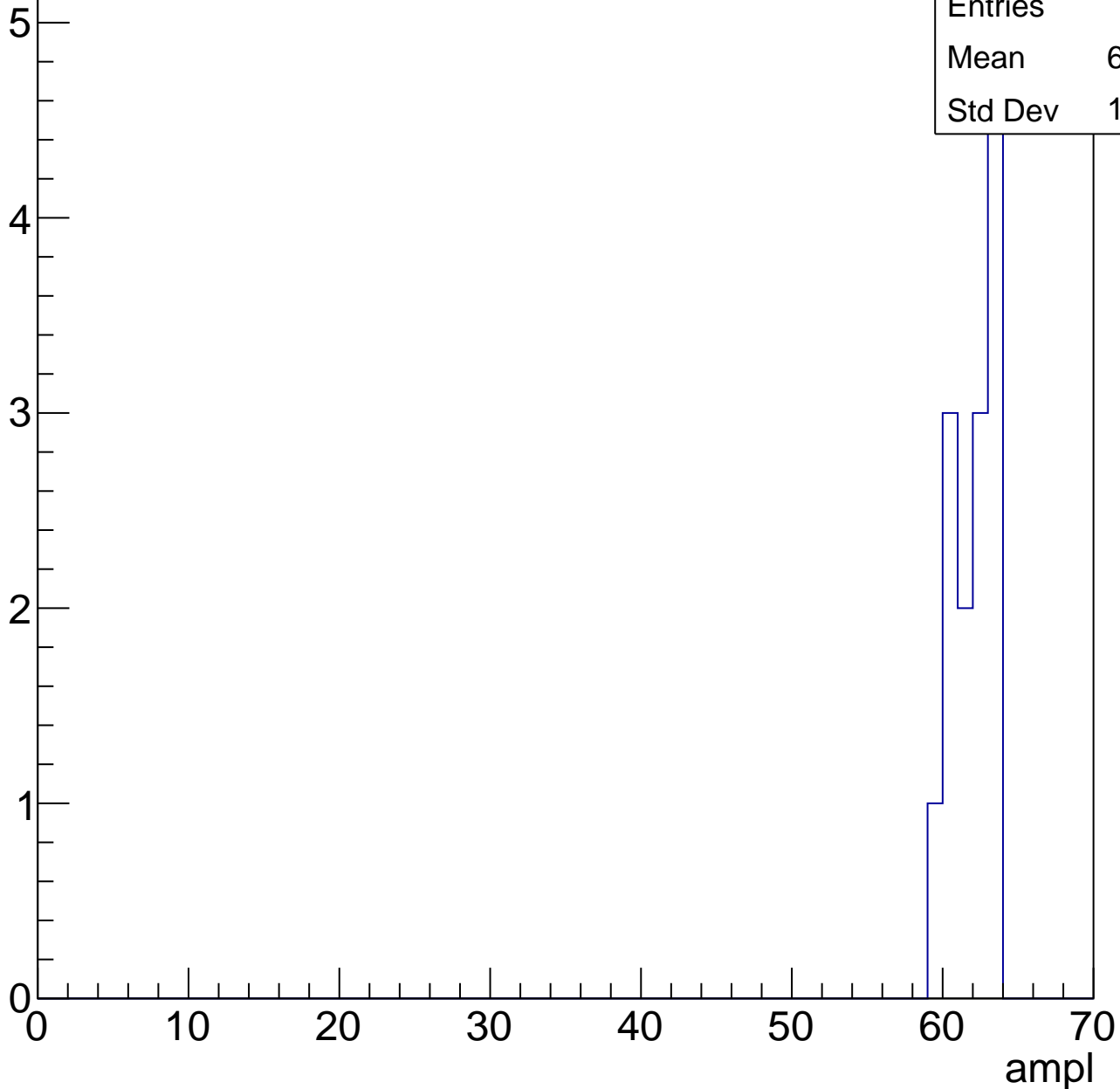


# B1L101S, U3-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	14
Mean	61.57
Std Dev	1.348





# B1L101S, U3-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch69, adc0

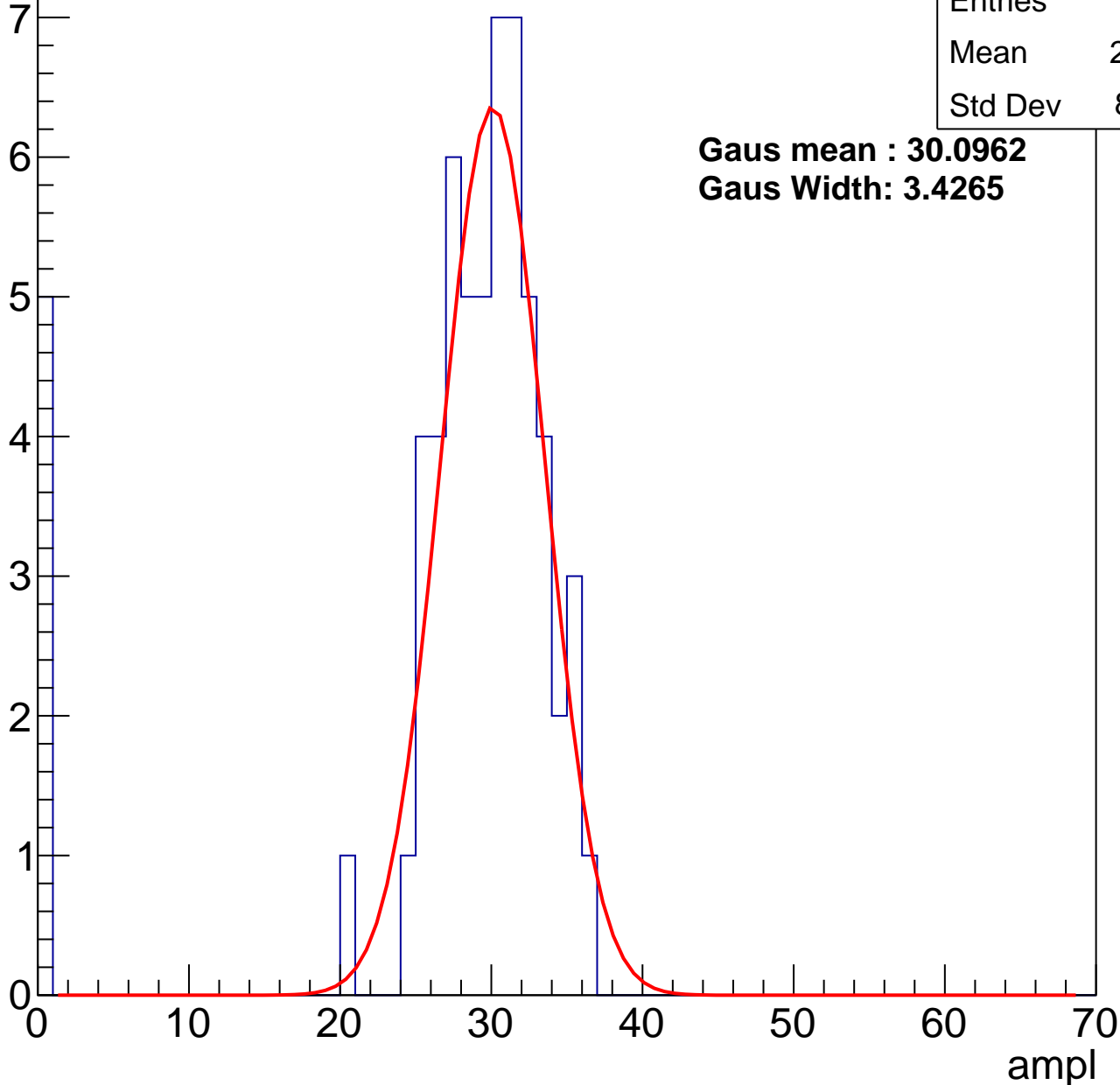
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	27.05
Std Dev	8.721

**Gaus mean : 30.0962**

**Gaus Width: 3.4265**



# B1L101S, U3-ch69, adc1

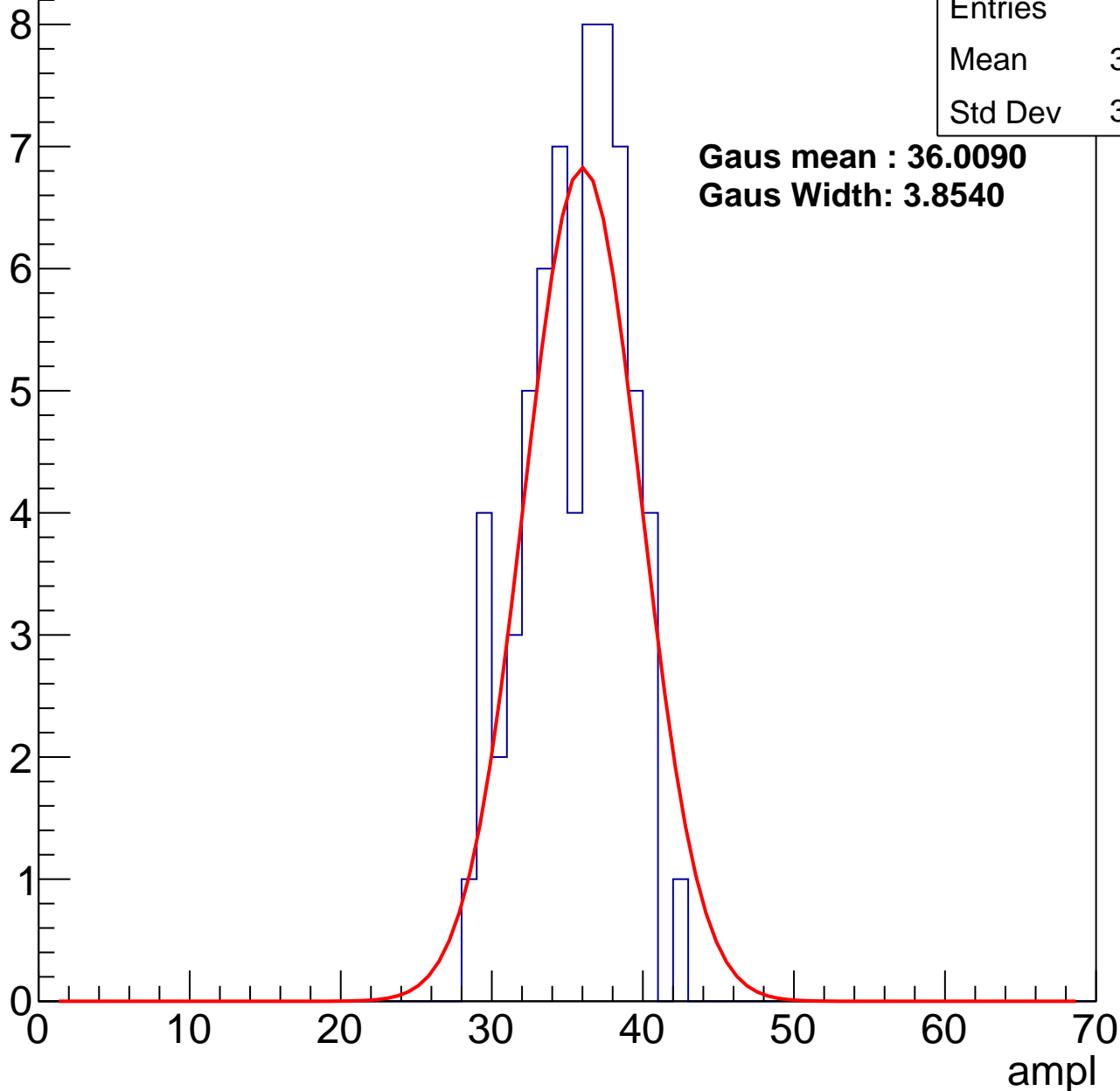
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	35.08
Std Dev	3.278

**Gaus mean : 36.0090**

**Gaus Width: 3.8540**



# B1L101S, U3-ch69, adc2

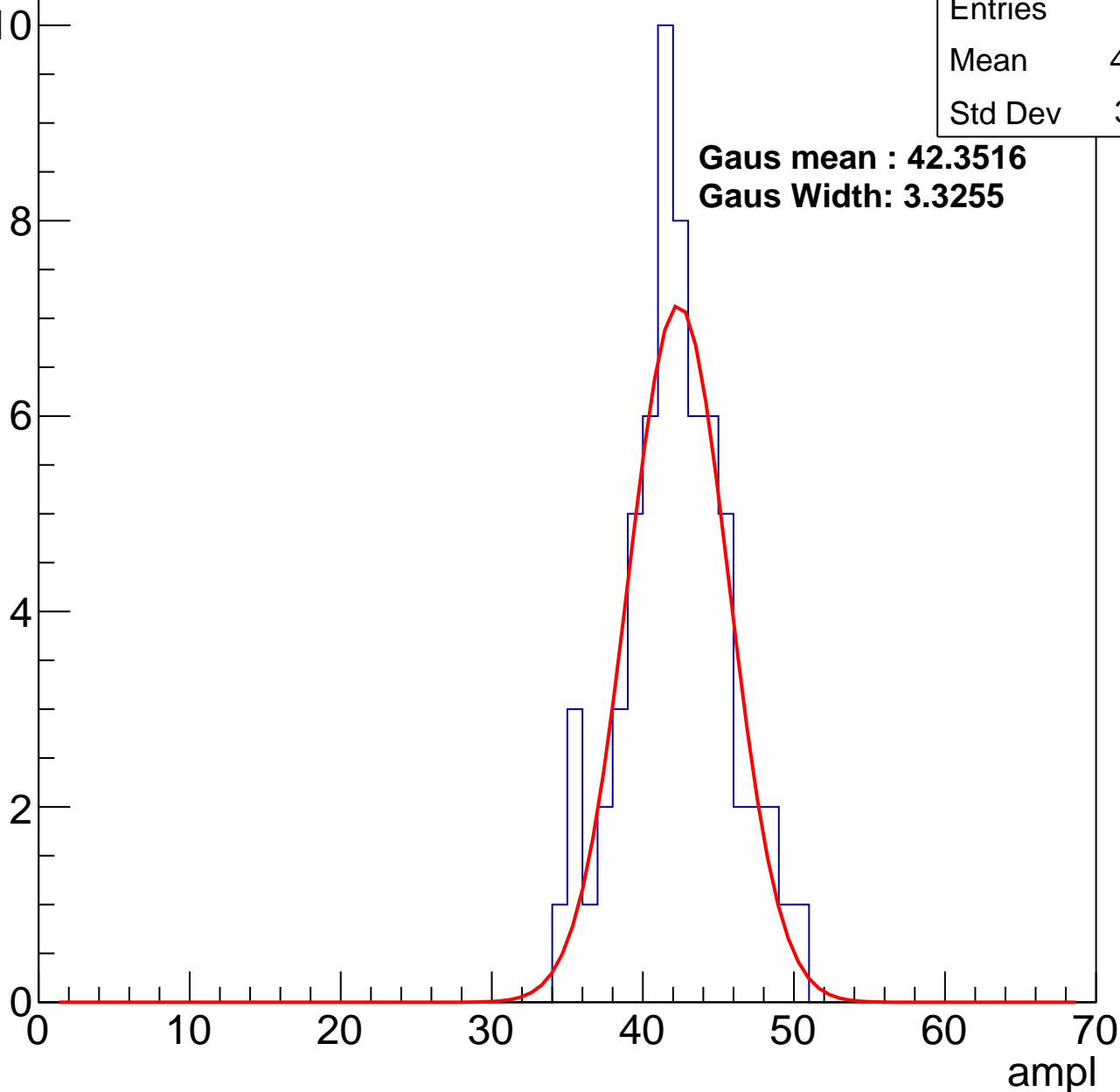
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	41.75
Std Dev	3.451

**Gaus mean : 42.3516**

**Gaus Width: 3.3255**

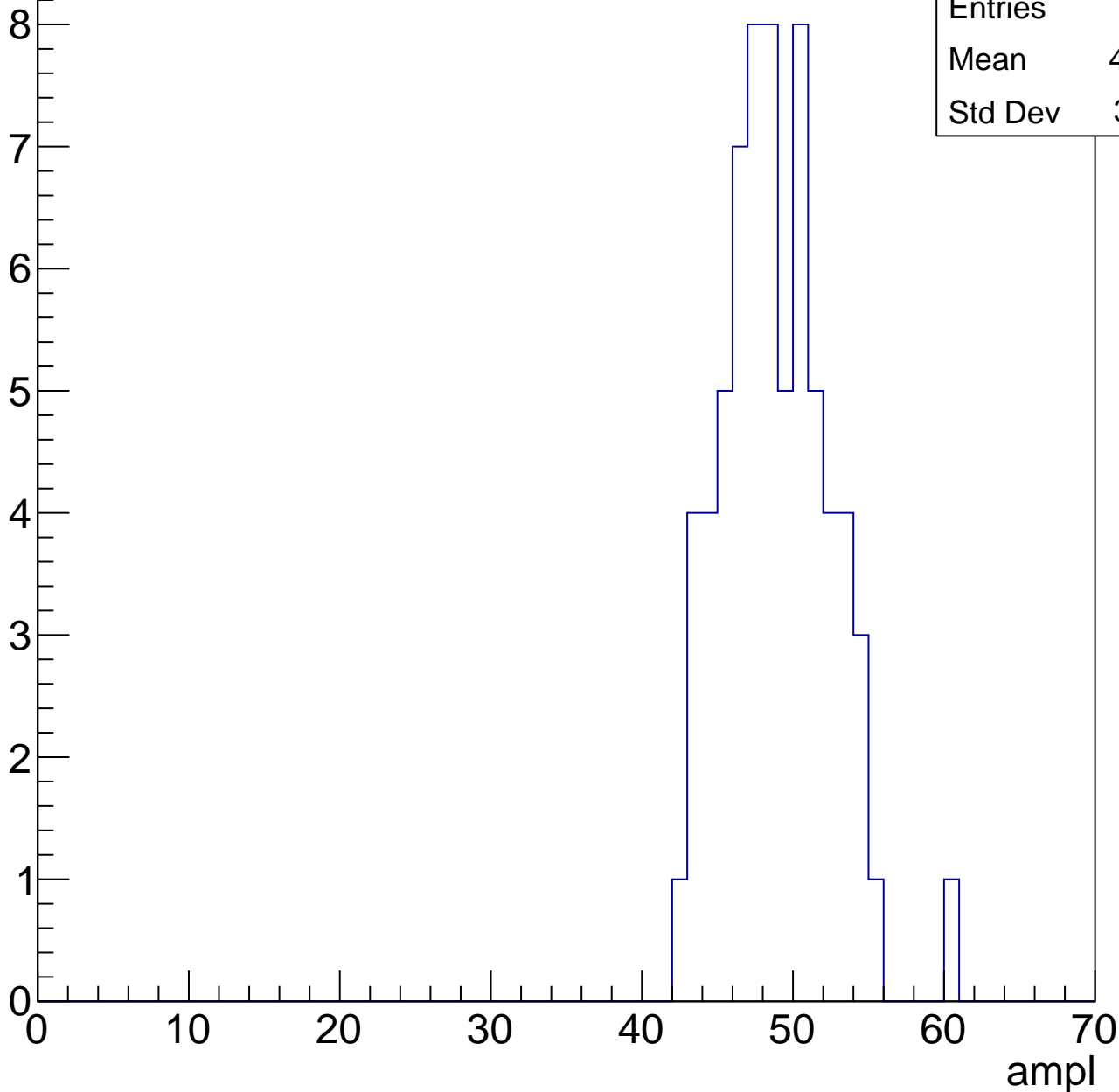


# B1L101S, U3-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	48.44
Std Dev	3.461

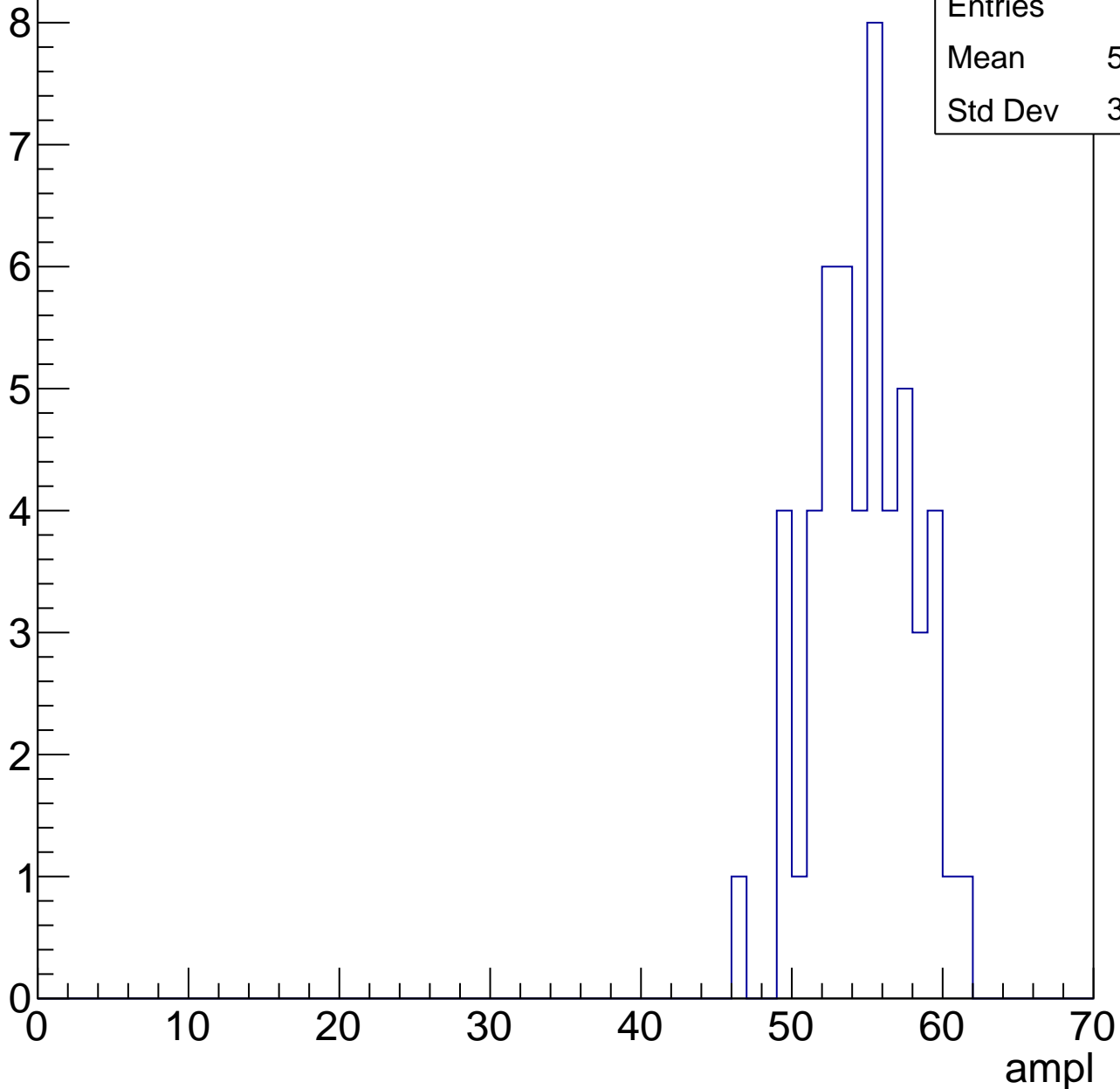


# B1L101S, U3-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	54.27
Std Dev	3.235



# B1L101S, U3-ch69, adc5

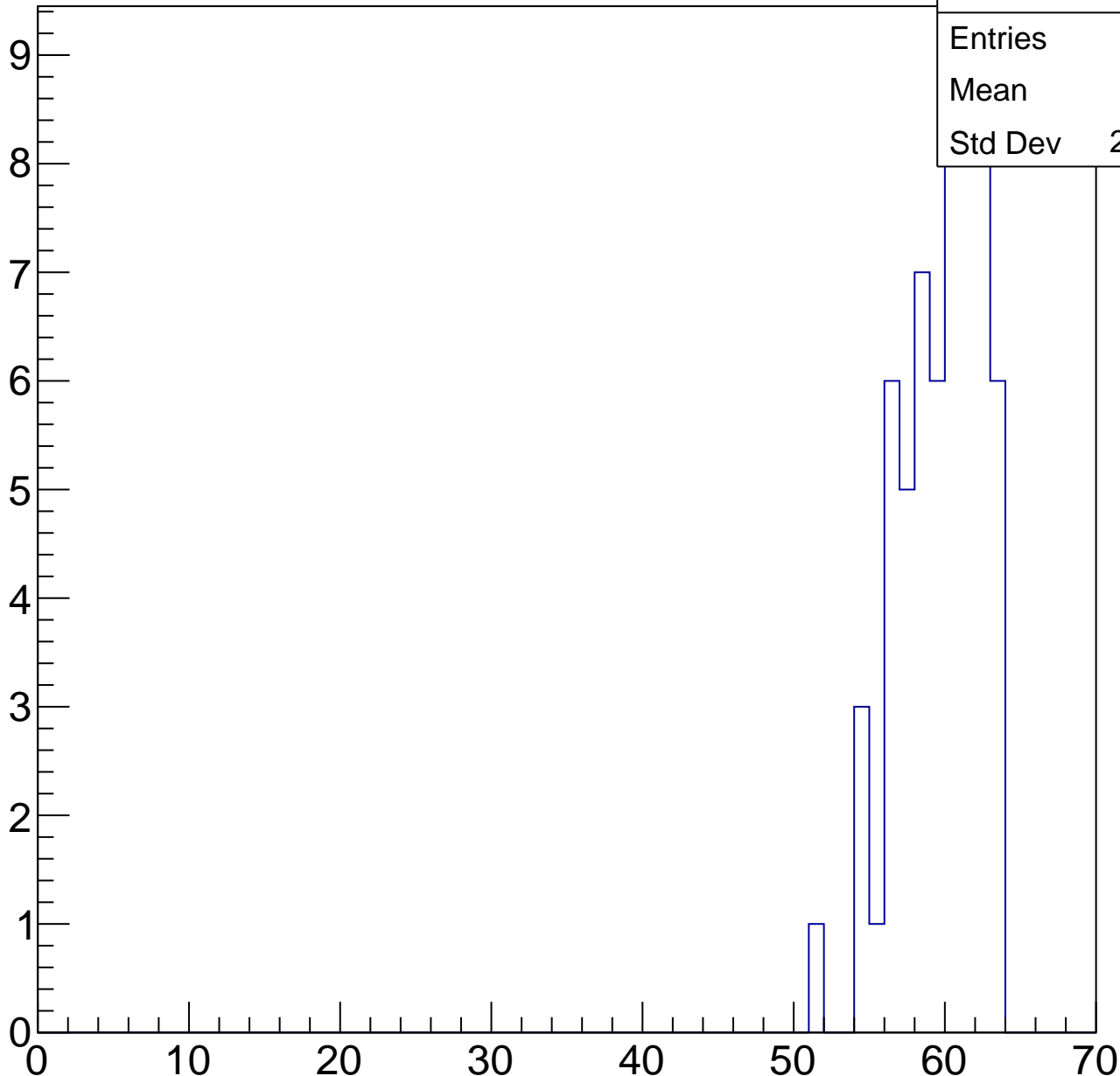
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	60
Mean	59.2
Std Dev	2.725

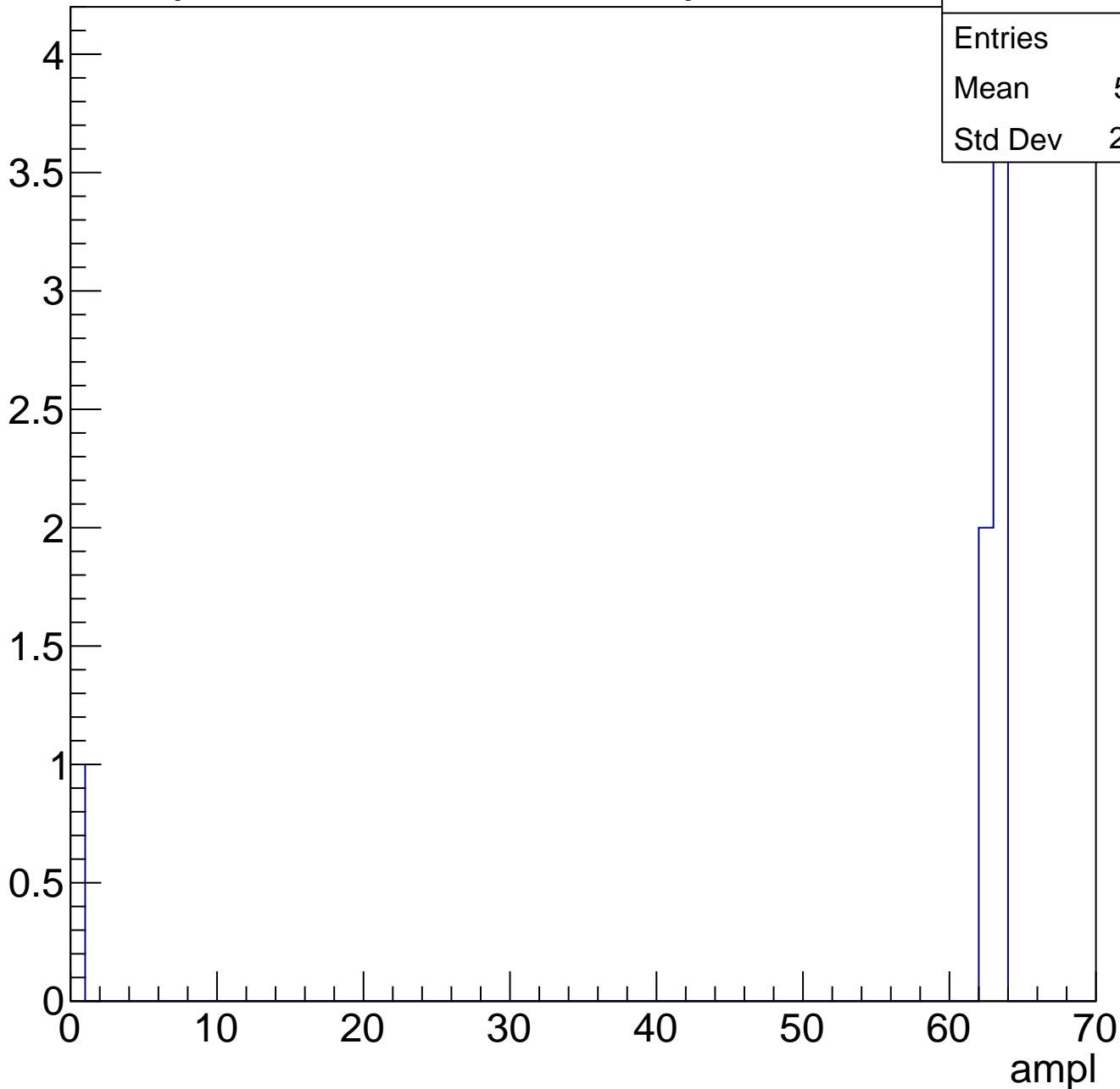
ampl



# B1L101S, U3-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U3-ch70, adc0

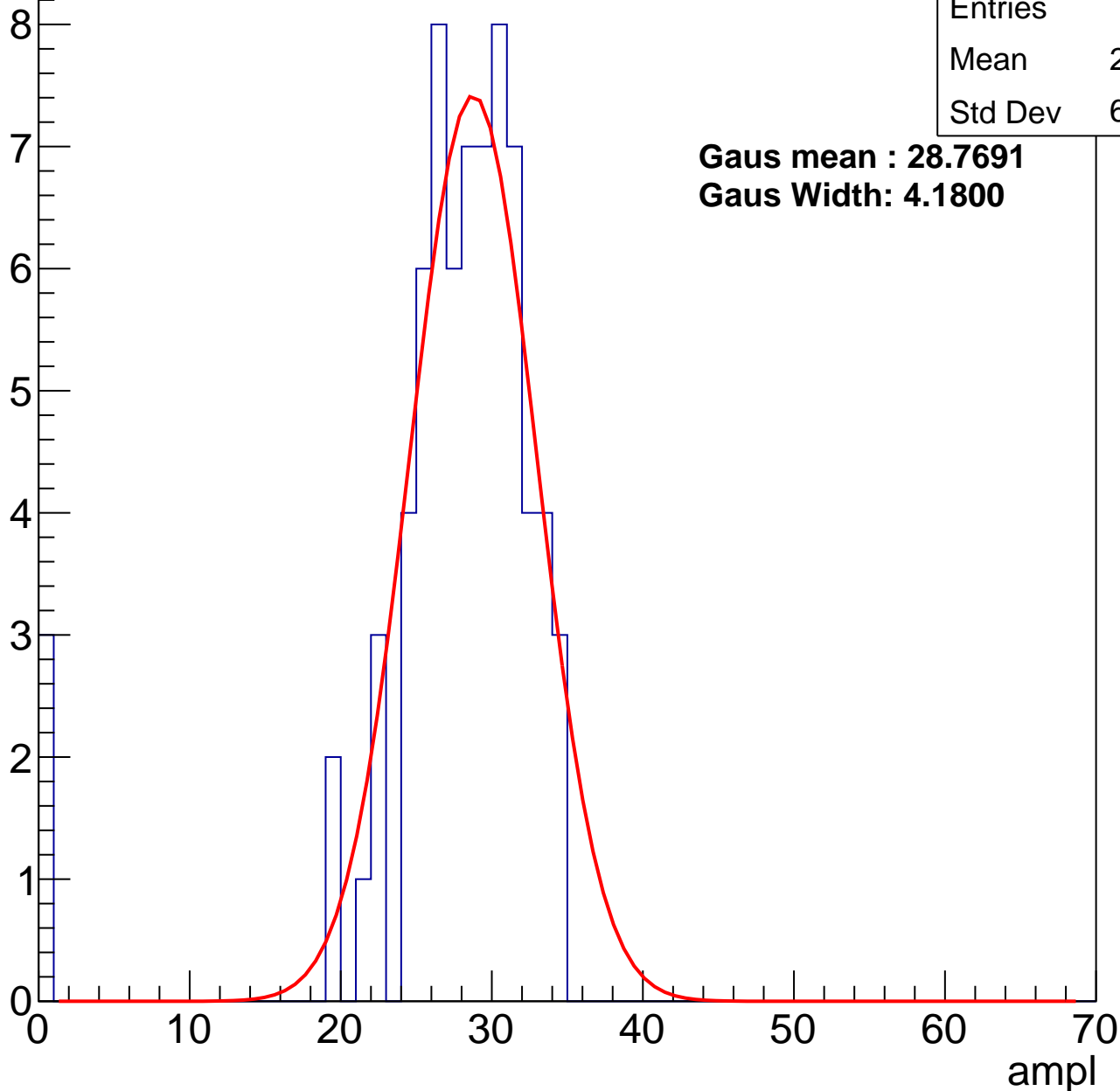
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	26.84
Std Dev	6.519

**Gaus mean : 28.7691**

**Gaus Width: 4.1800**



# B1L101S, U3-ch70, adc1

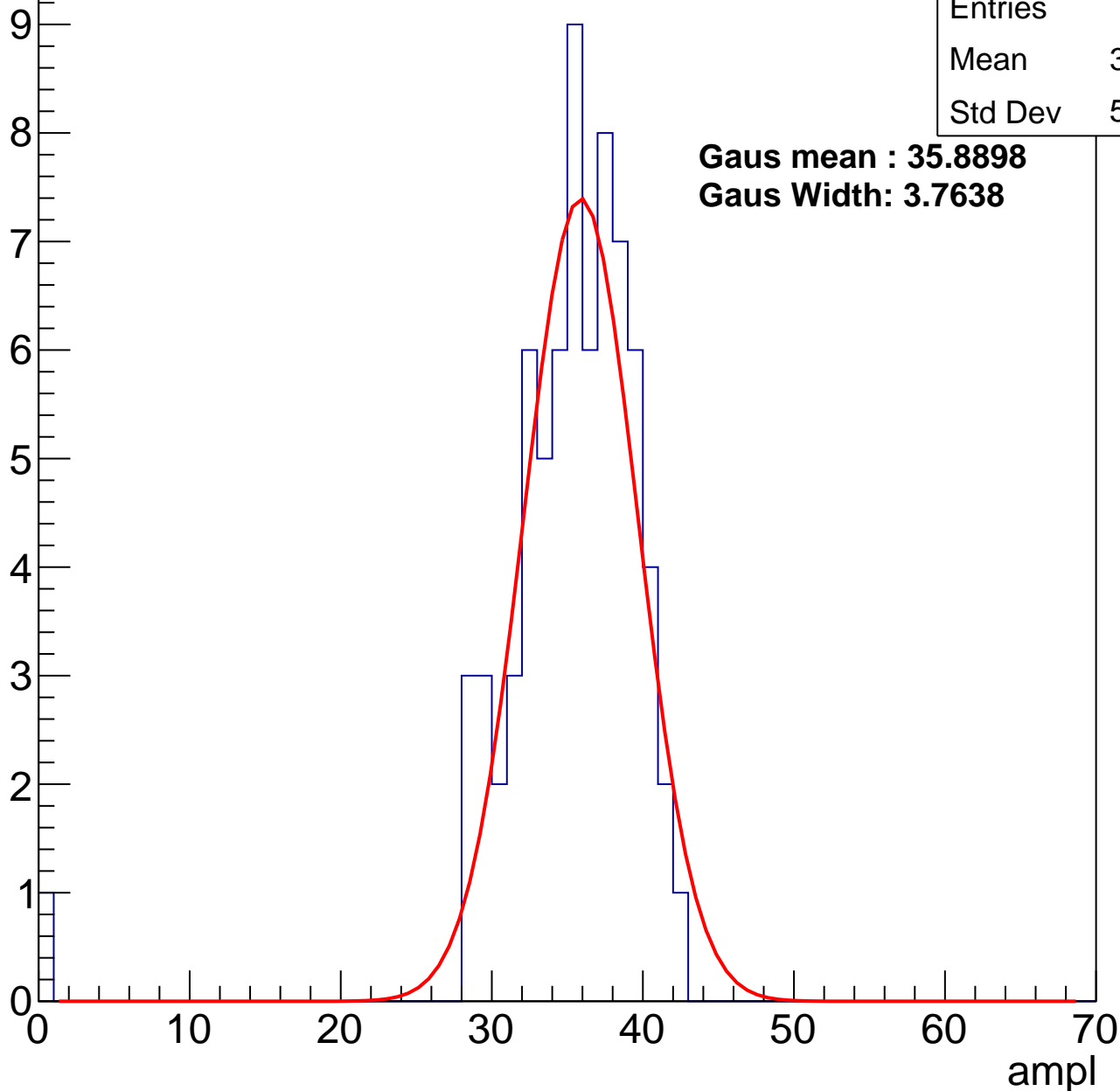
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	34.67
Std Dev	5.359

**Gaus mean : 35.8898**

**Gaus Width: 3.7638**



# B1L101S, U3-ch70, adc2

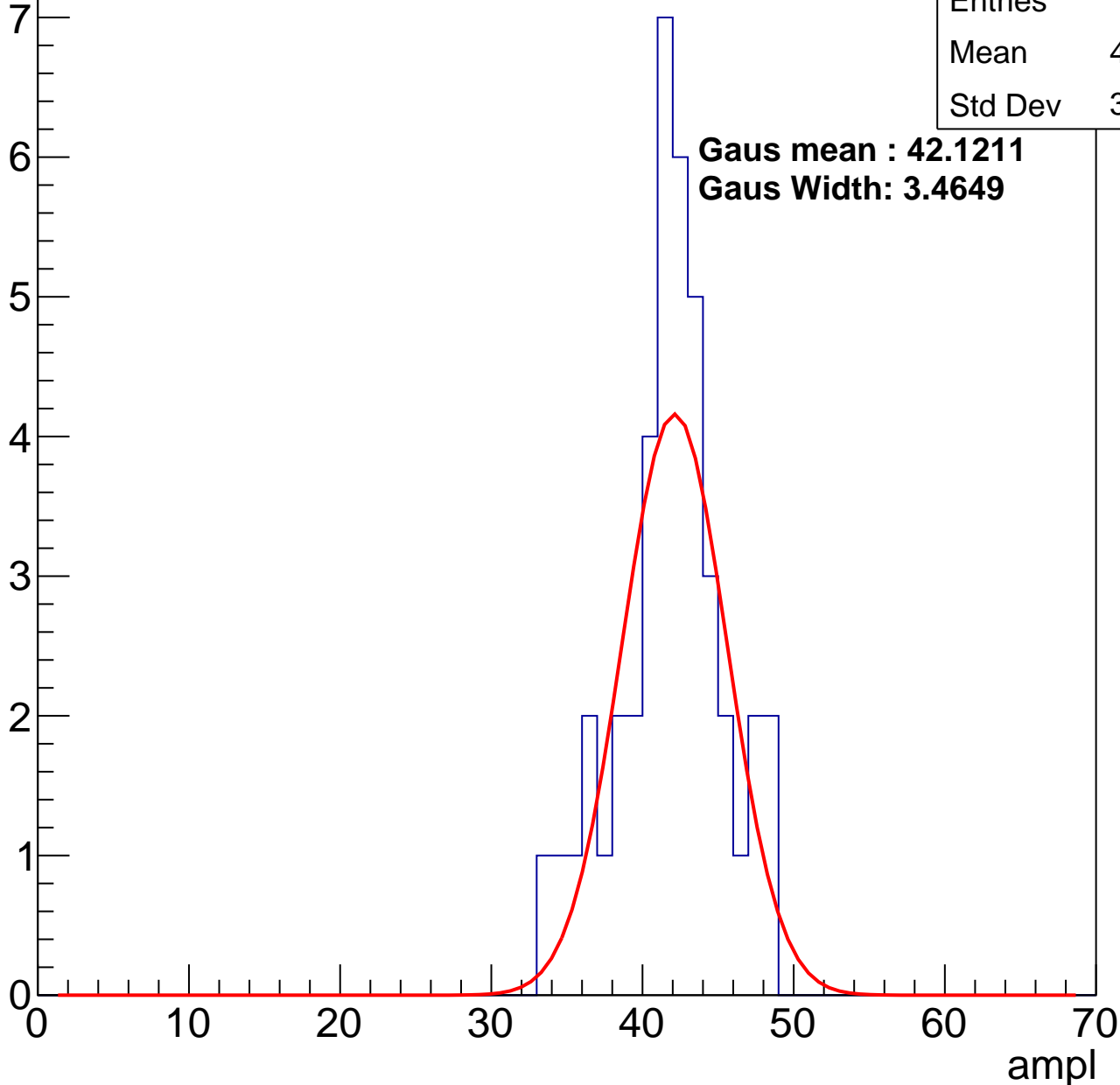
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	41.36
Std Dev	3.517

**Gaus mean : 42.1211**

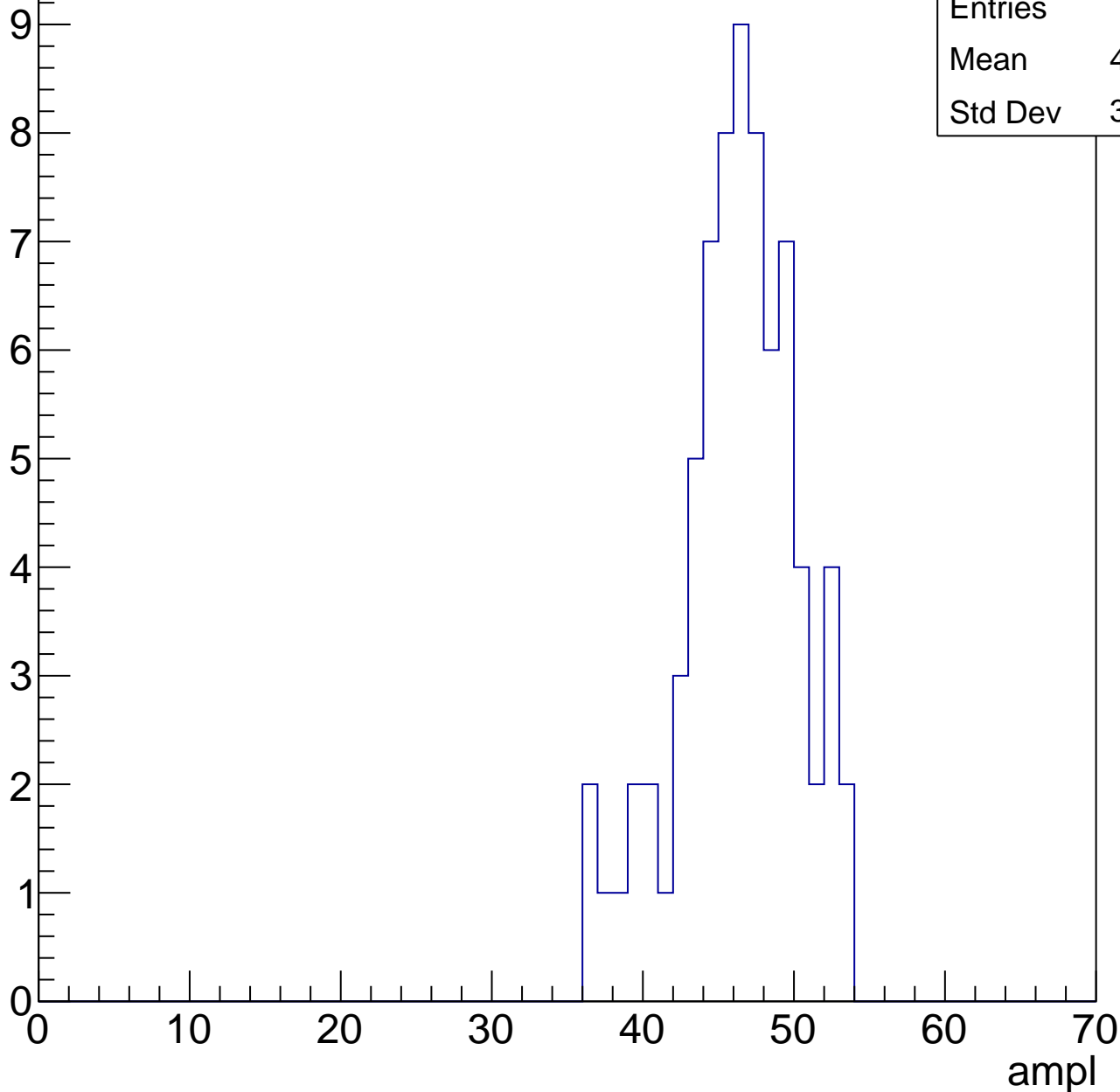
**Gaus Width: 3.4649**



# B1L101S, U3-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

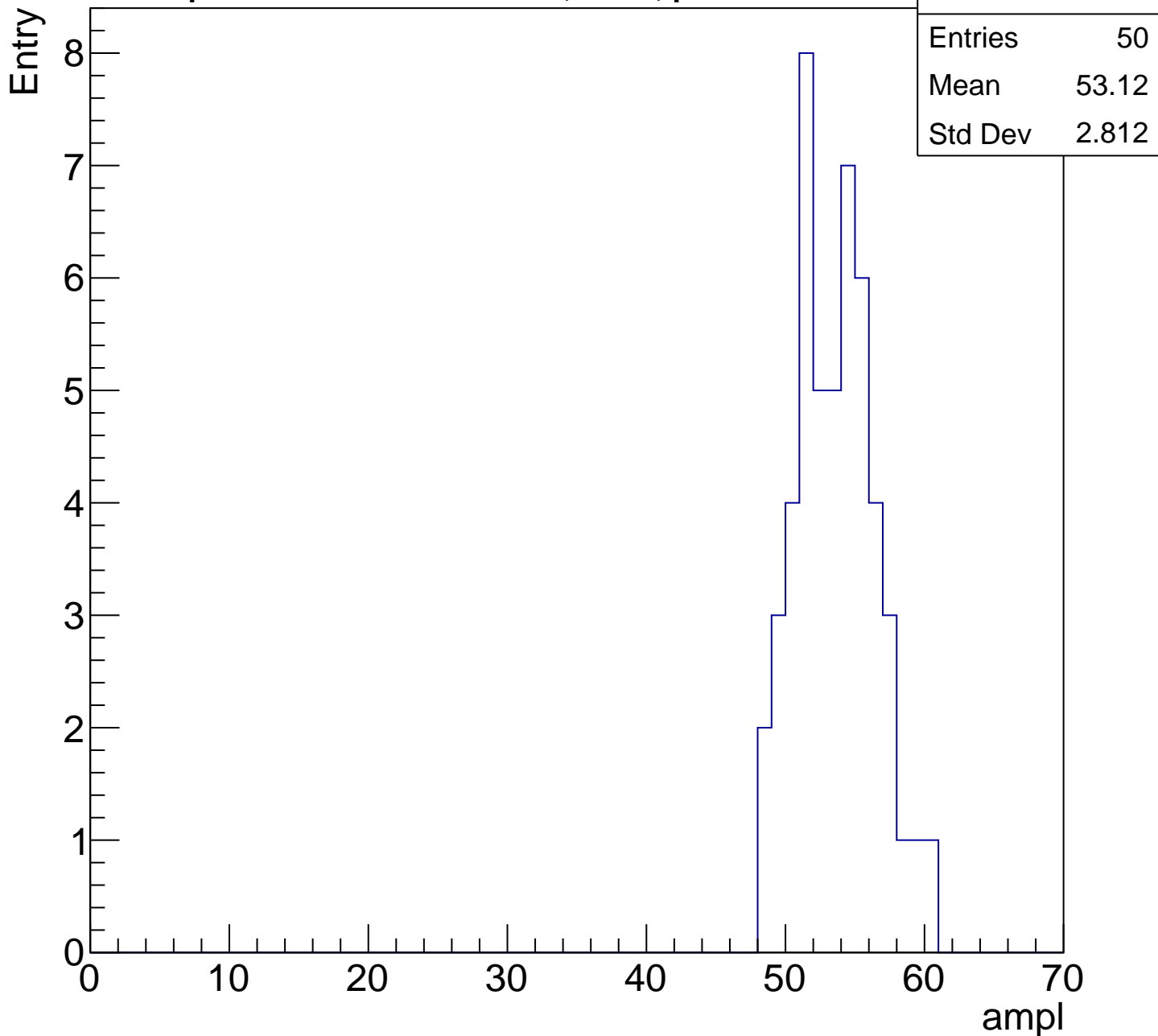
Entry



Entries	74
Mean	45.84
Std Dev	3.887

# B1L101S, U3-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

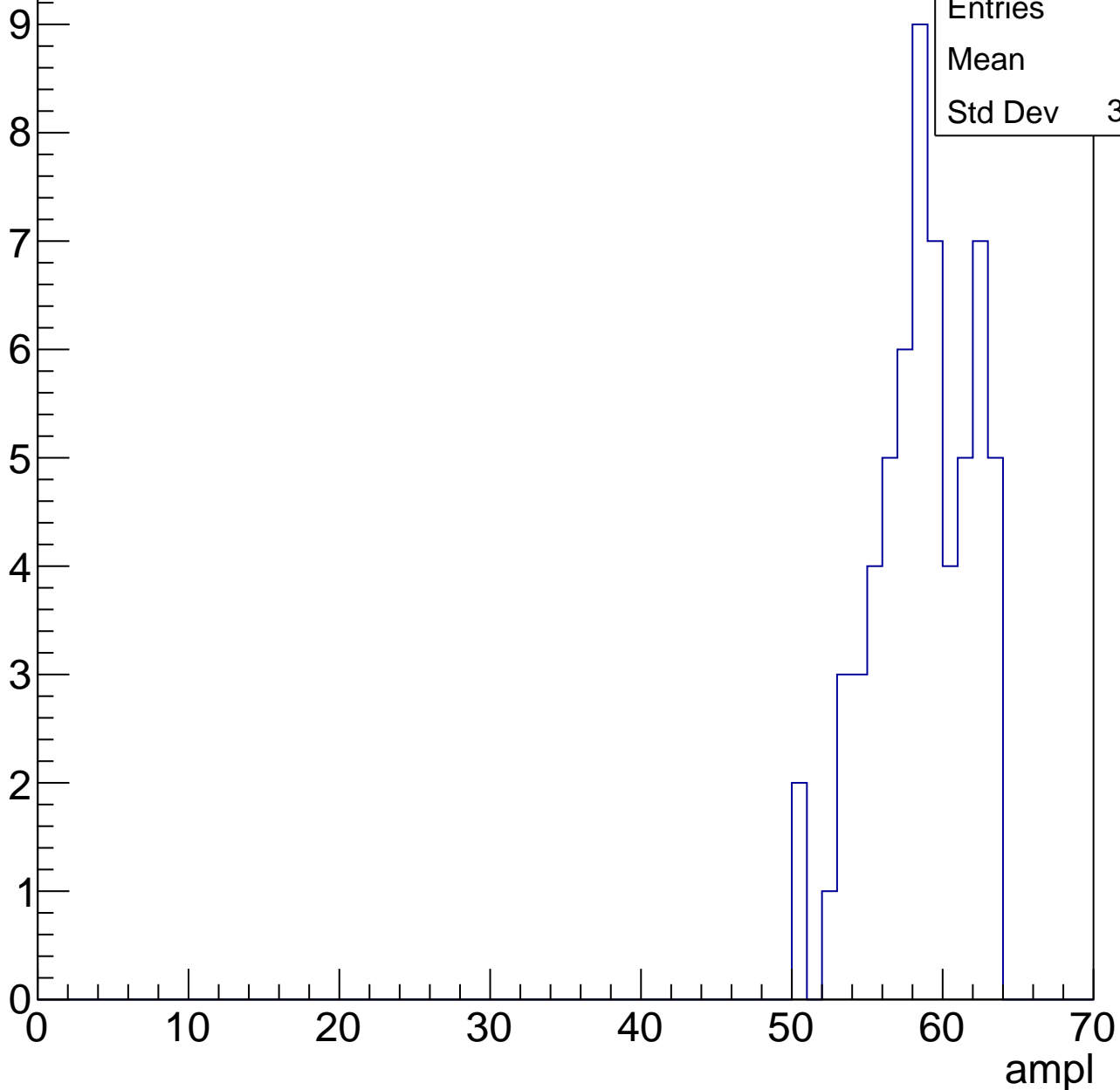


# B1L101S, U3-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

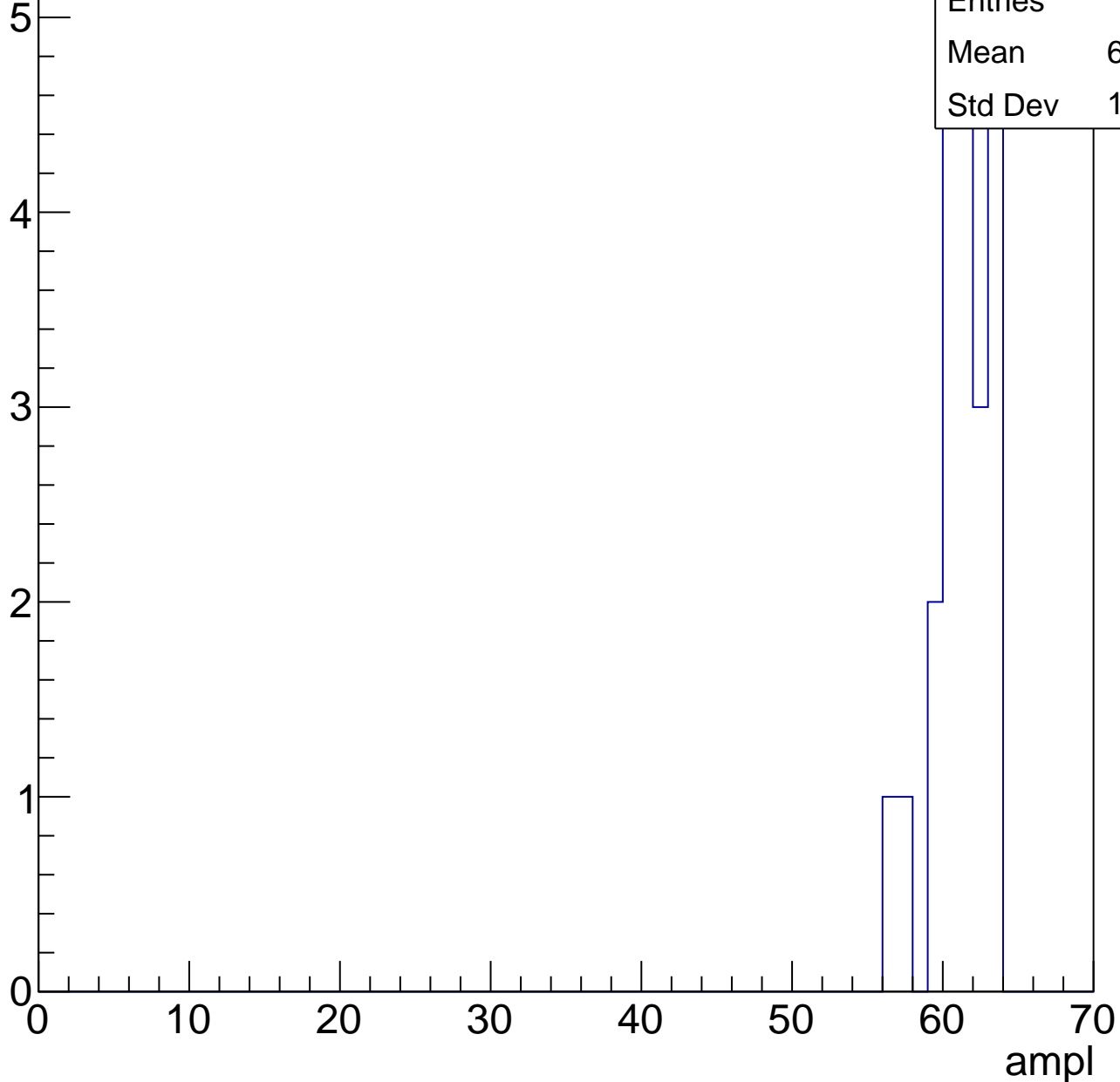
Entries	61
Mean	58.1
Std Dev	3.273



# B1L101S, U3-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U3-ch71, adc0

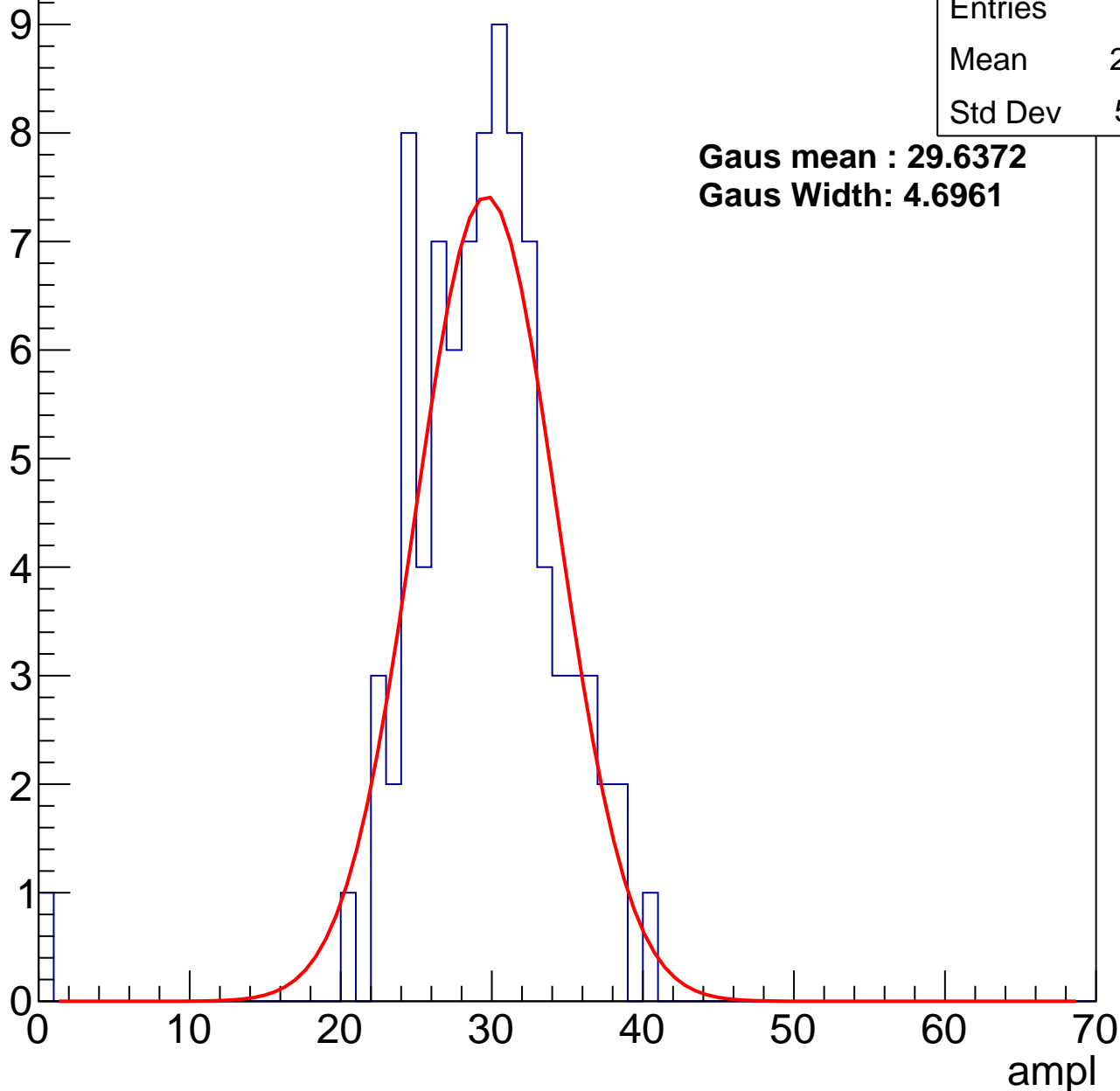
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	89
Mean	28.93
Std Dev	5.201

**Gaus mean : 29.6372**

**Gaus Width: 4.6961**



# B1L101S, U3-ch71, adc1

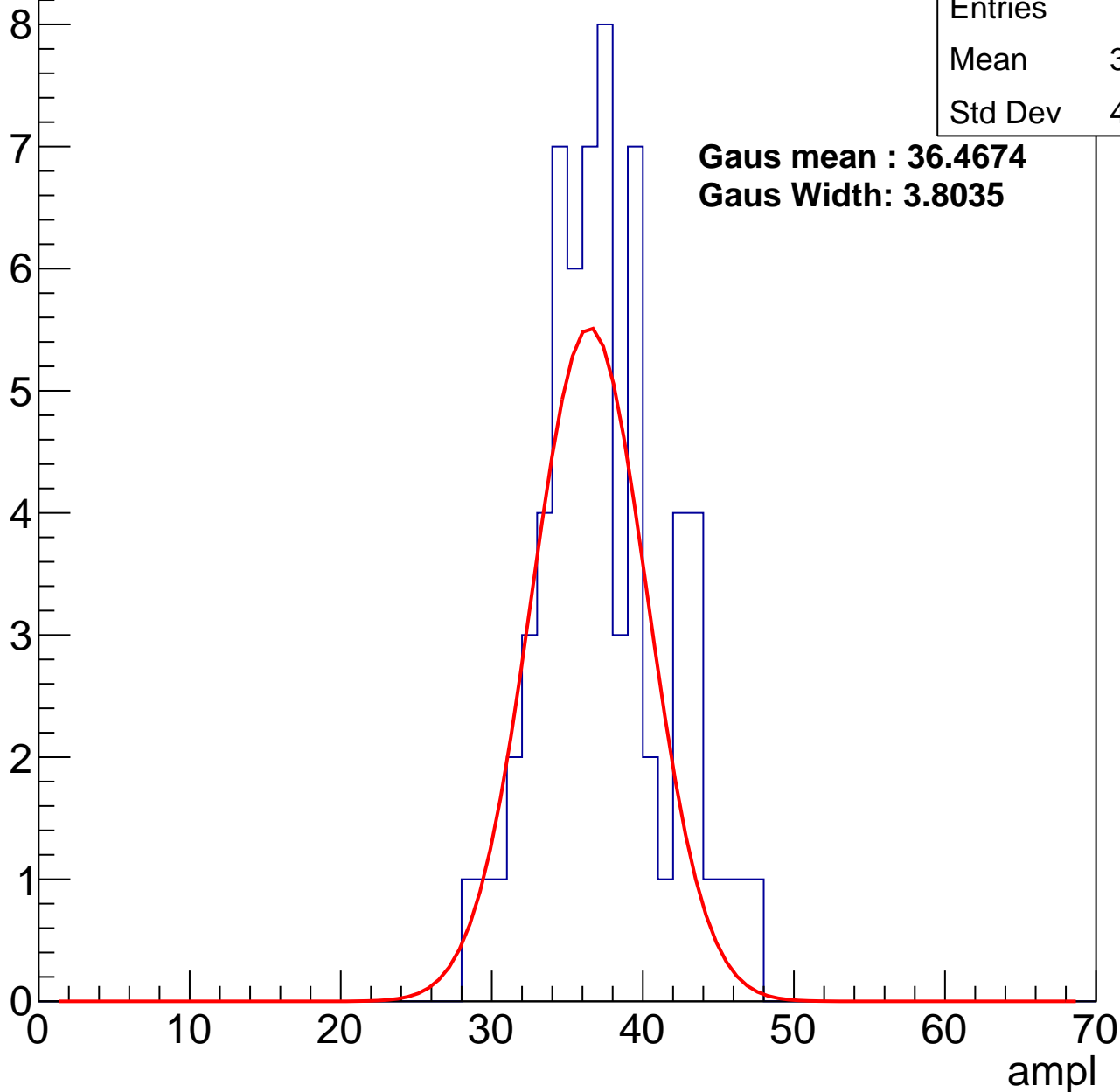
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	36.97
Std Dev	4.117

**Gaus mean : 36.4674**

**Gaus Width: 3.8035**



# B1L101S, U3-ch71, adc2

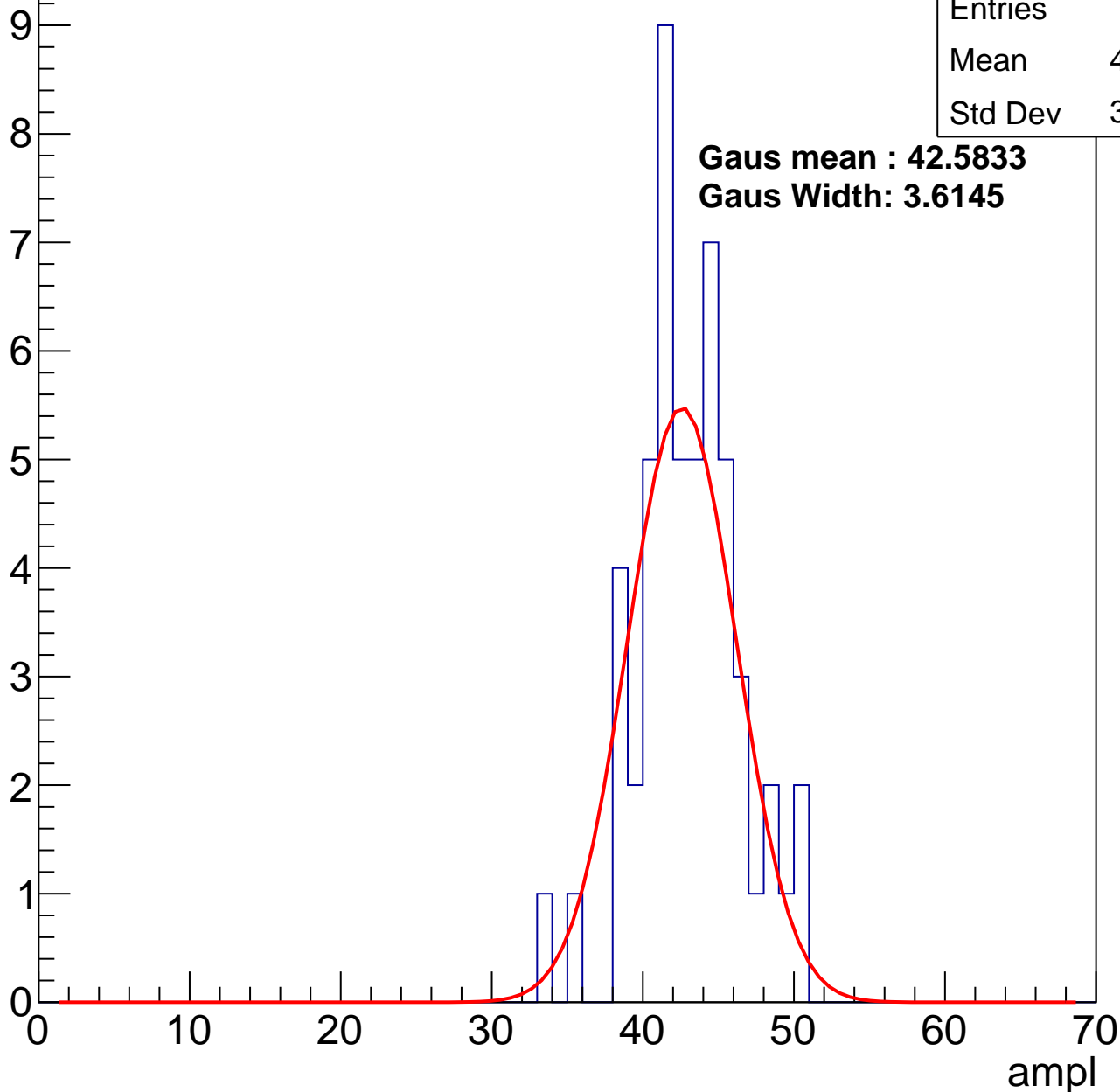
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	42.55
Std Dev	3.434

**Gaus mean : 42.5833**

**Gaus Width: 3.6145**

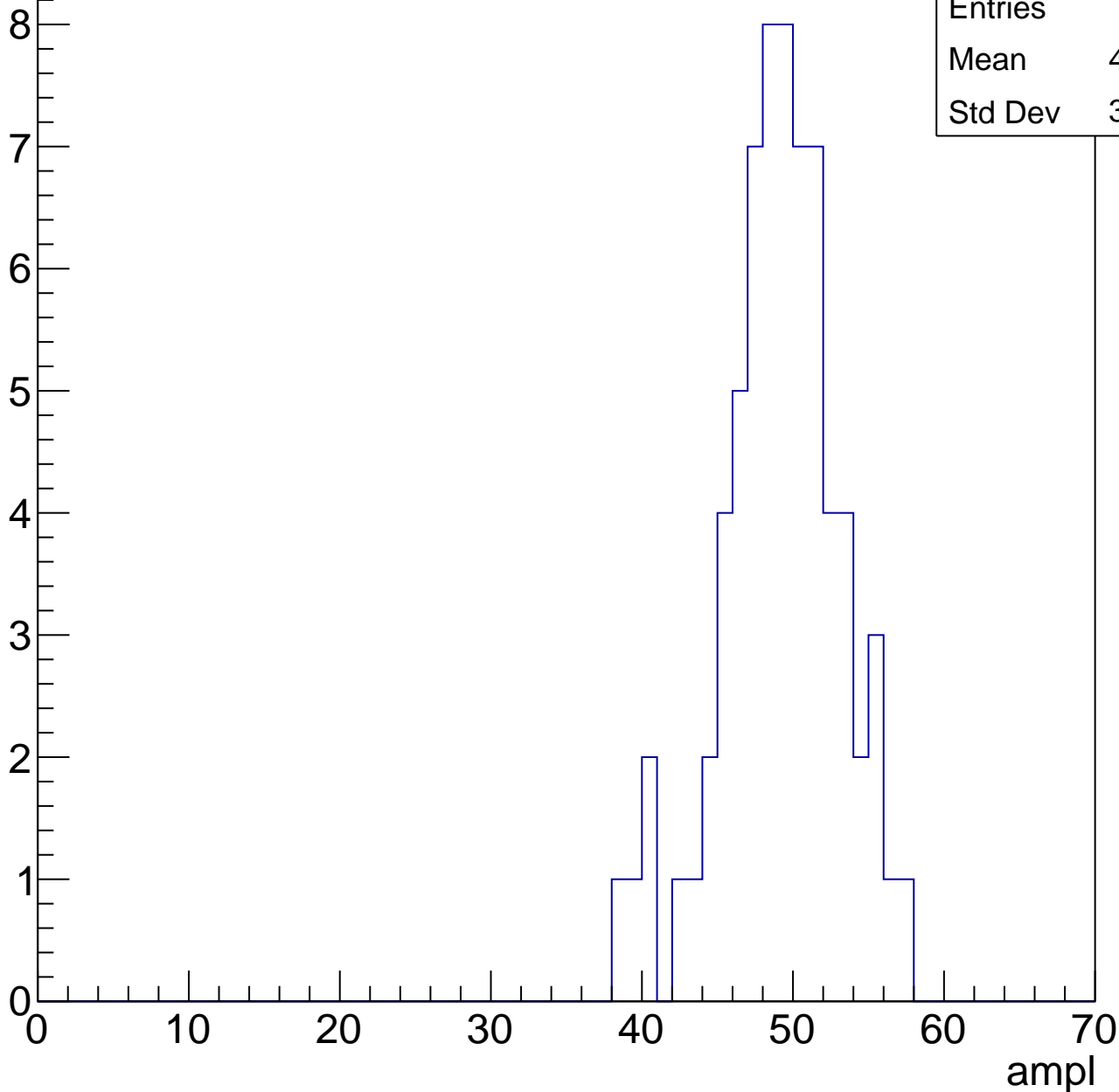


# B1L101S, U3-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

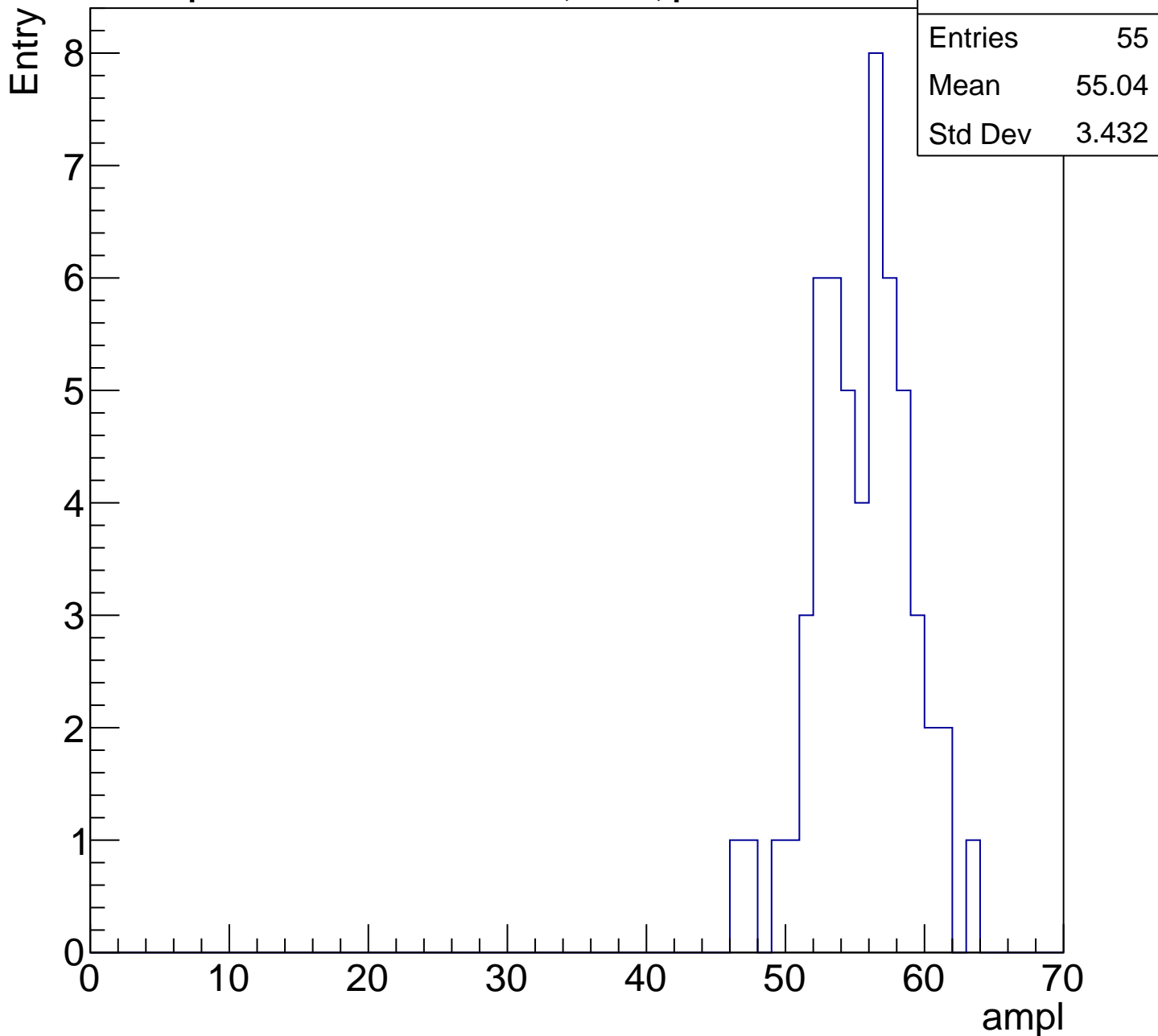
Entry

Entries	69
Mean	48.67
Std Dev	3.922



# B1L101S, U3-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

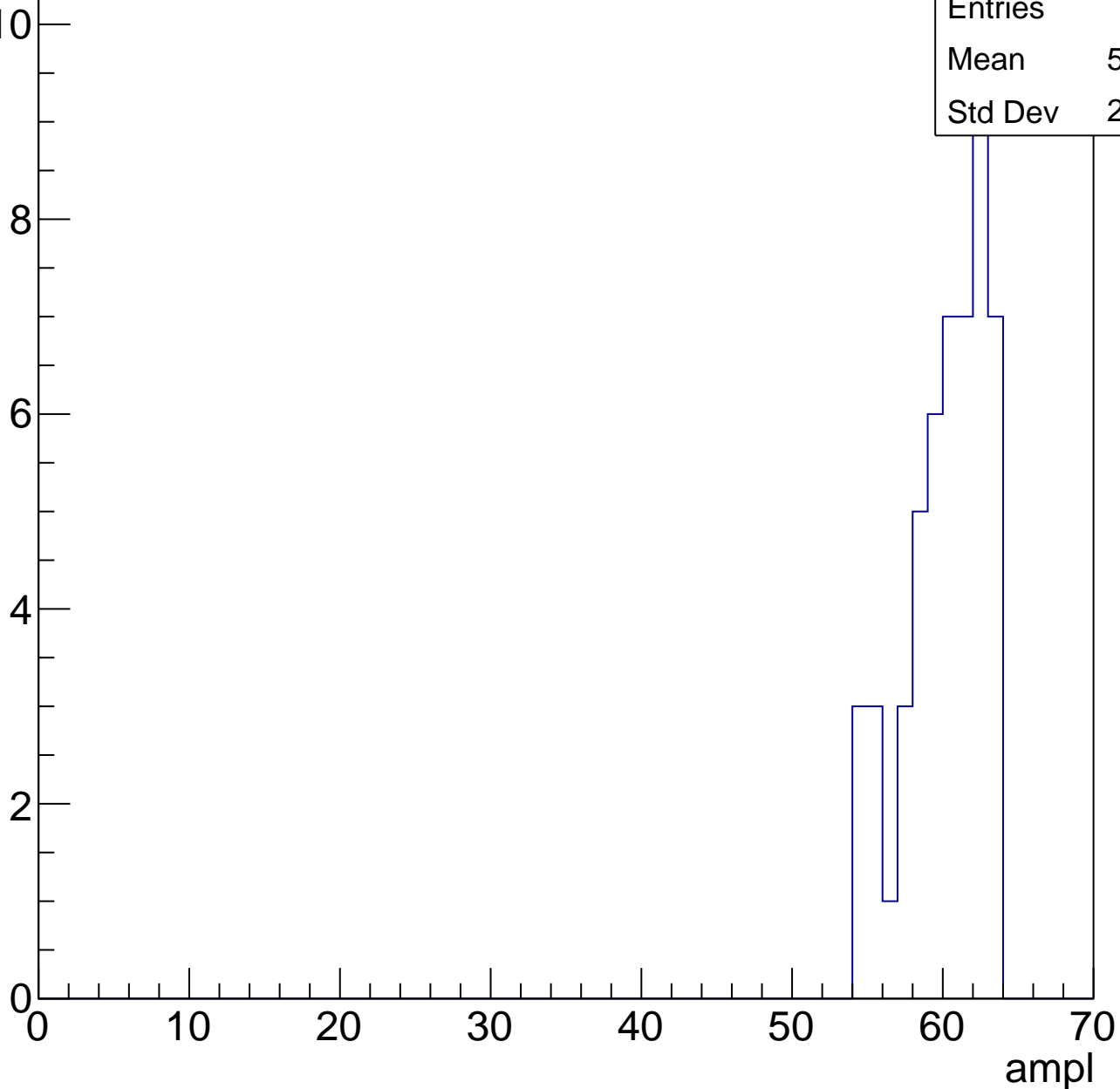


# B1L101S, U3-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

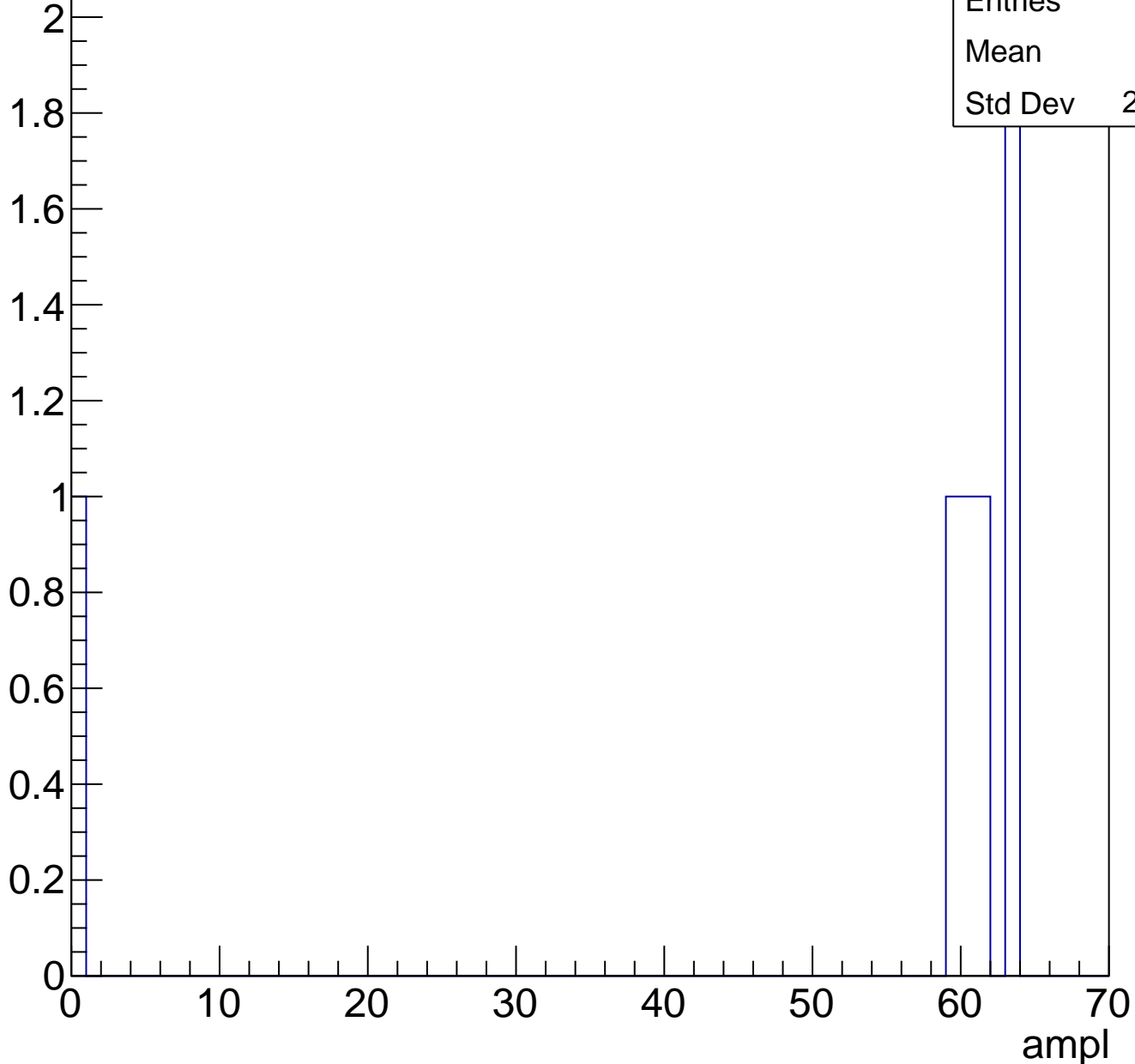
Entries	52
Mean	59.73
Std Dev	2.625



# B1L101S, U3-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U3-ch72, adc0

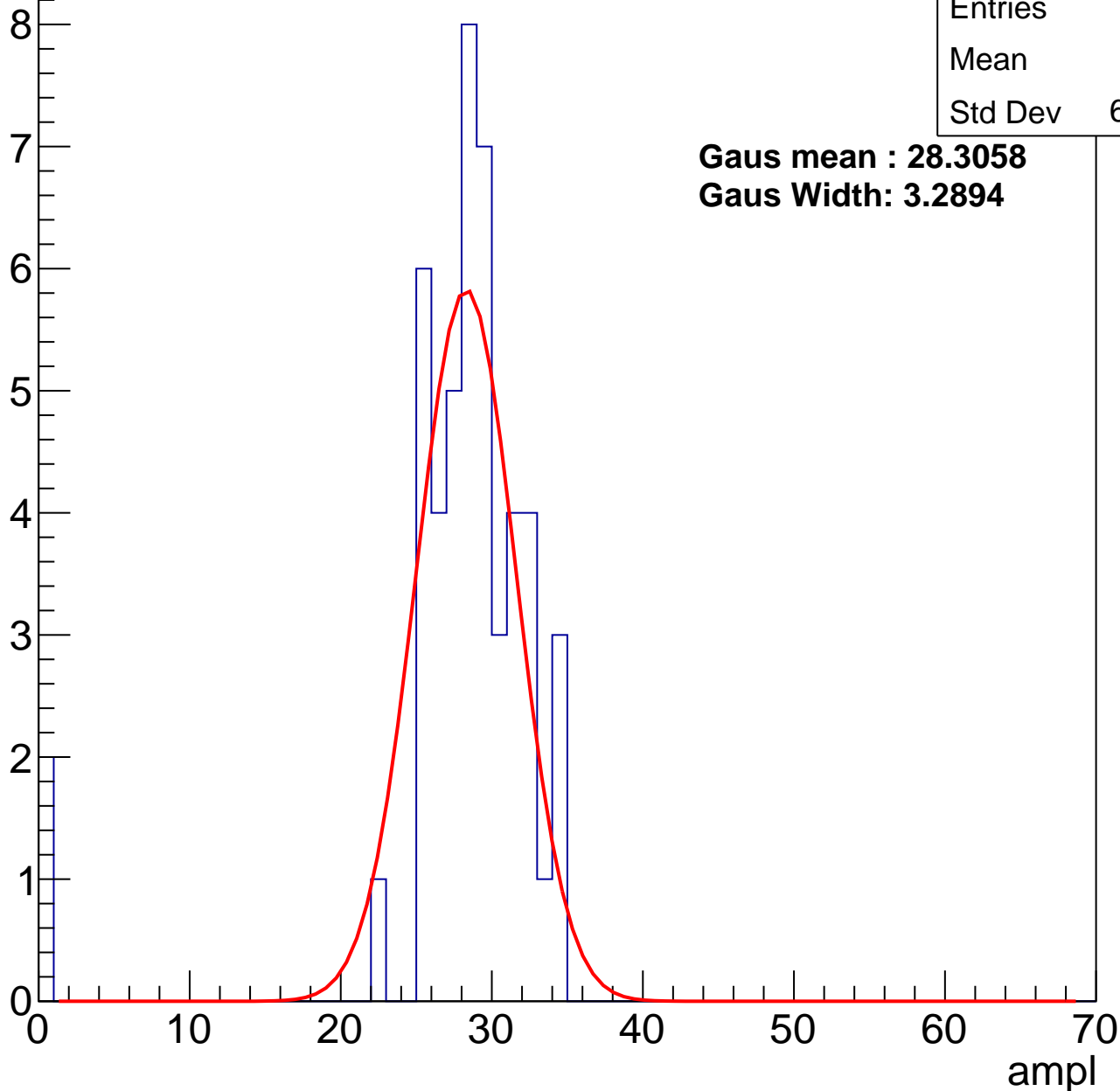
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	27.4
Std Dev	6.314

**Gaus mean : 28.3058**

**Gaus Width: 3.2894**



# B1L101S, U3-ch72, adc1

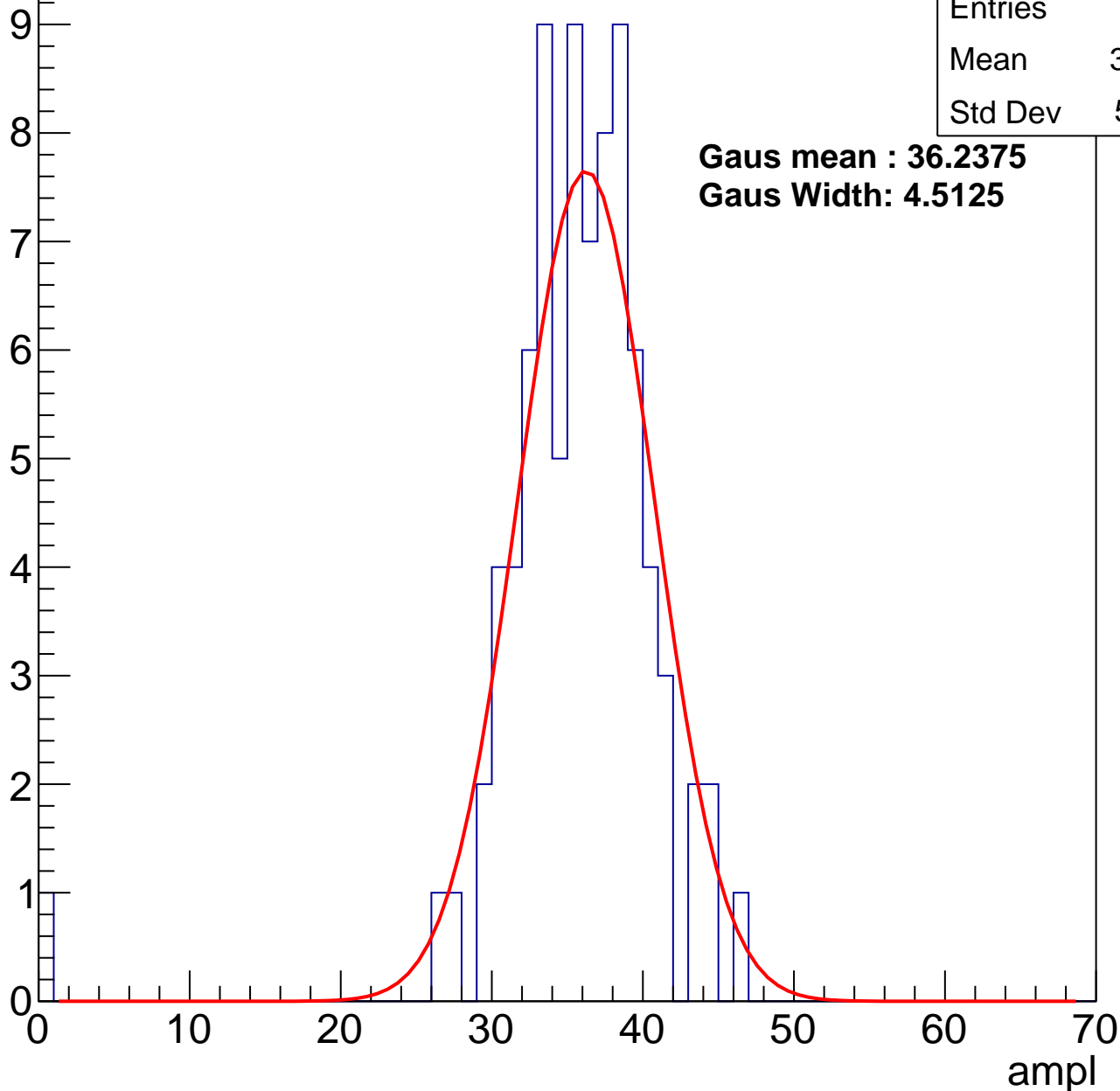
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	84
Mean	35.19
Std Dev	5.491

**Gaus mean : 36.2375**

**Gaus Width: 4.5125**



# B1L101S, U3-ch72, adc2

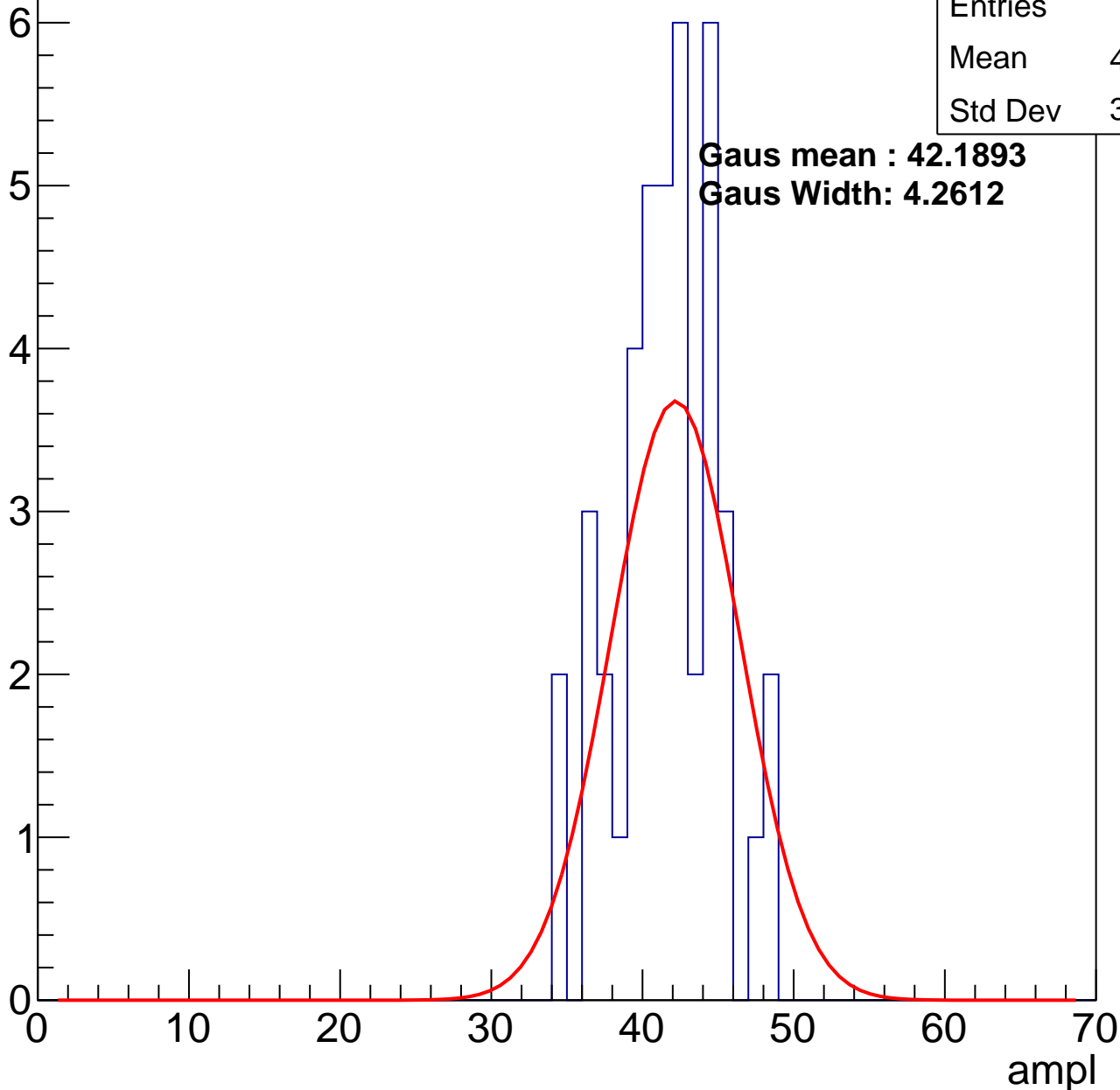
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	41.17
Std Dev	3.394

**Gaus mean : 42.1893**

**Gaus Width: 4.2612**

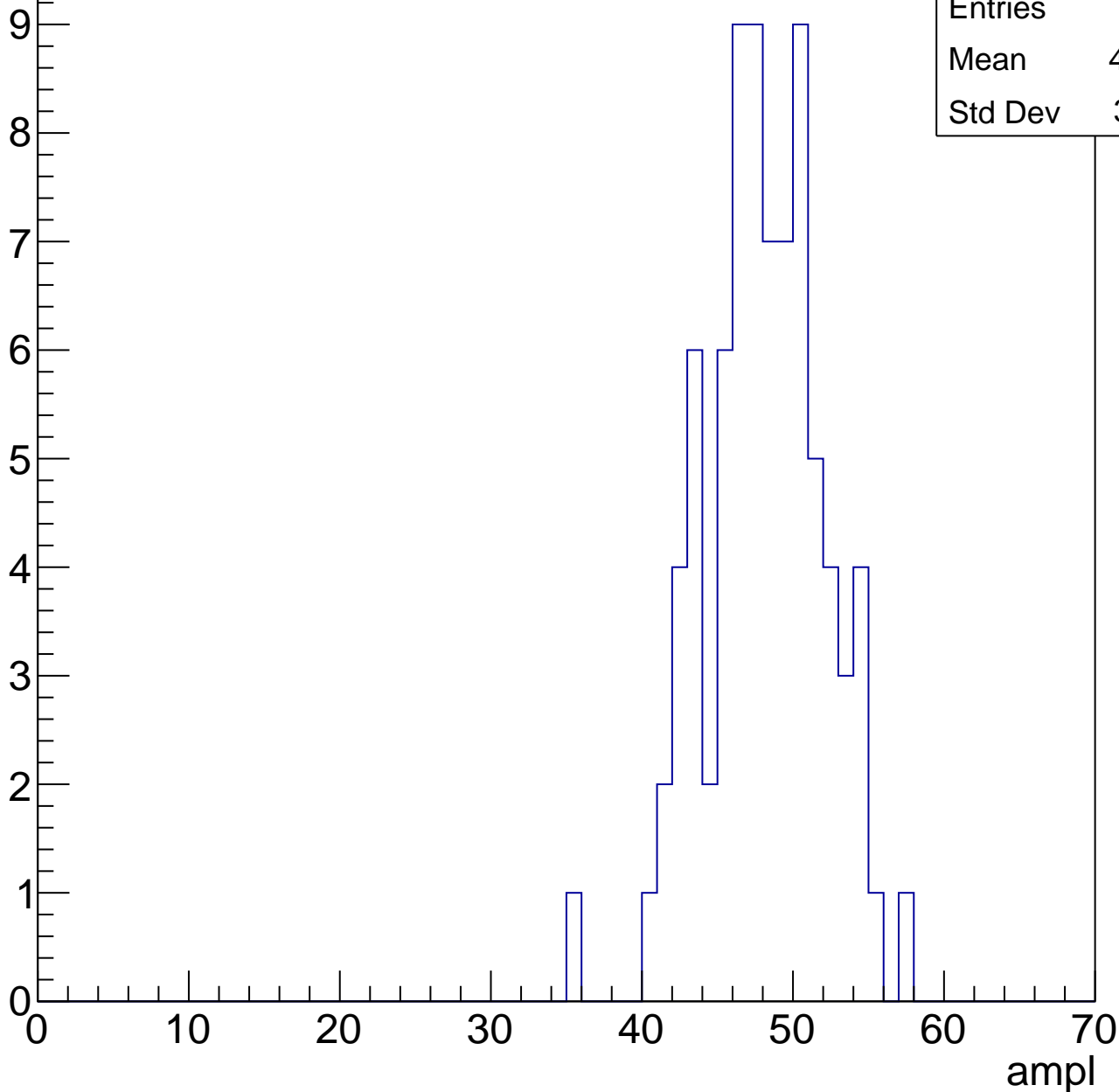


# B1L101S, U3-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

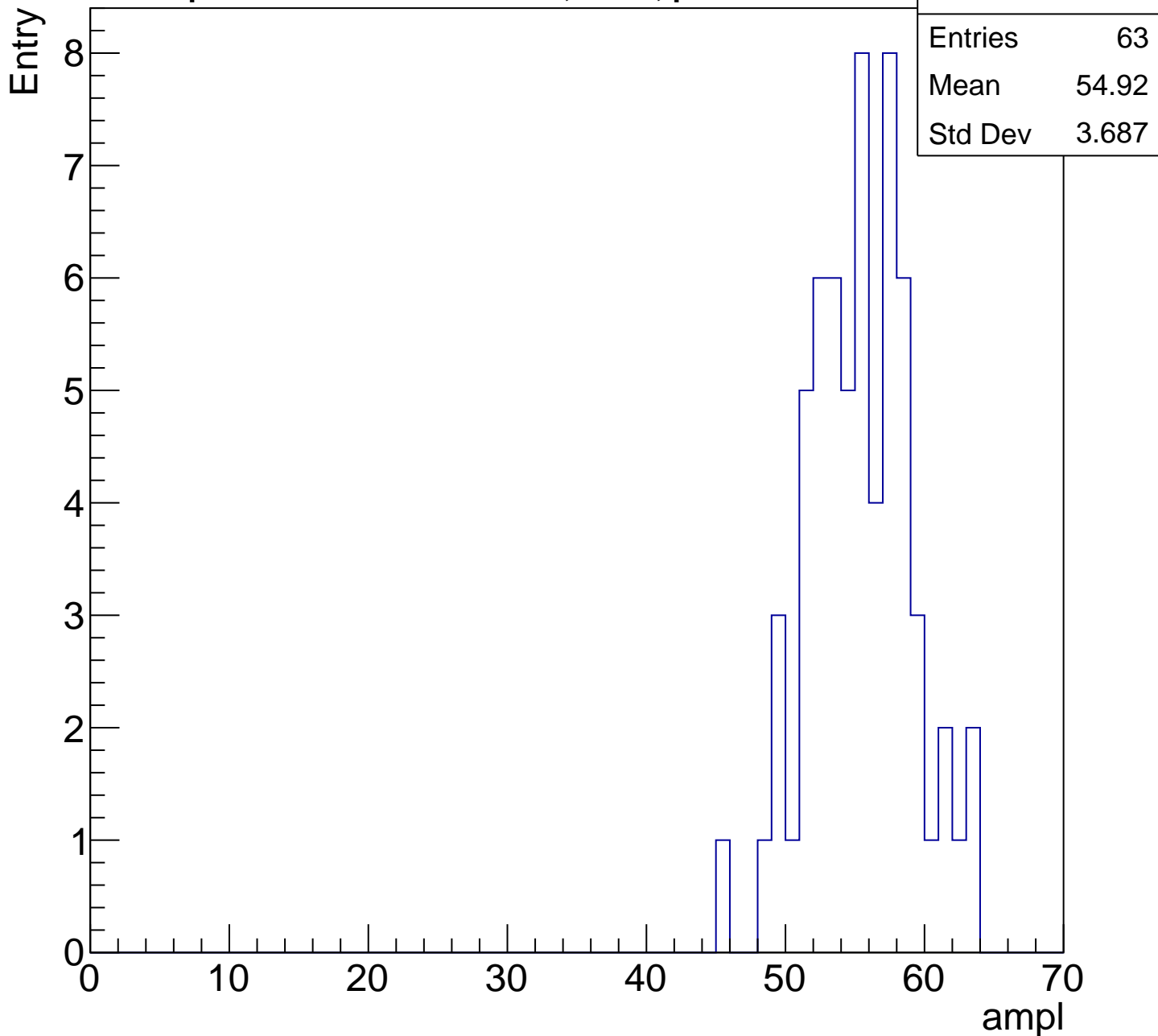
Entry

Entries	81
Mean	47.62
Std Dev	3.921



# B1L101S, U3-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

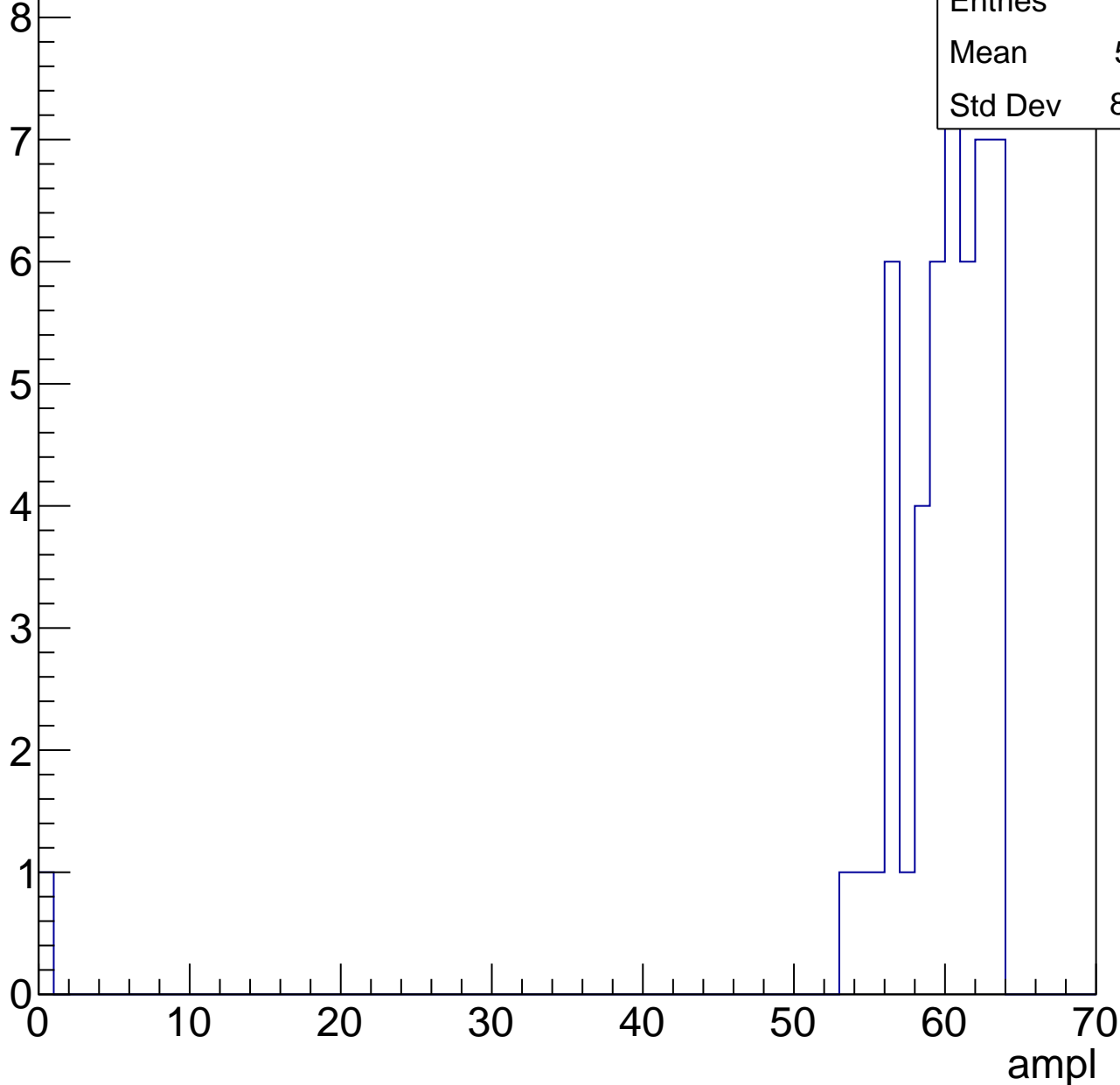


# B1L101S, U3-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	58.41
Std Dev	8.818



# B1L101S, U3-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

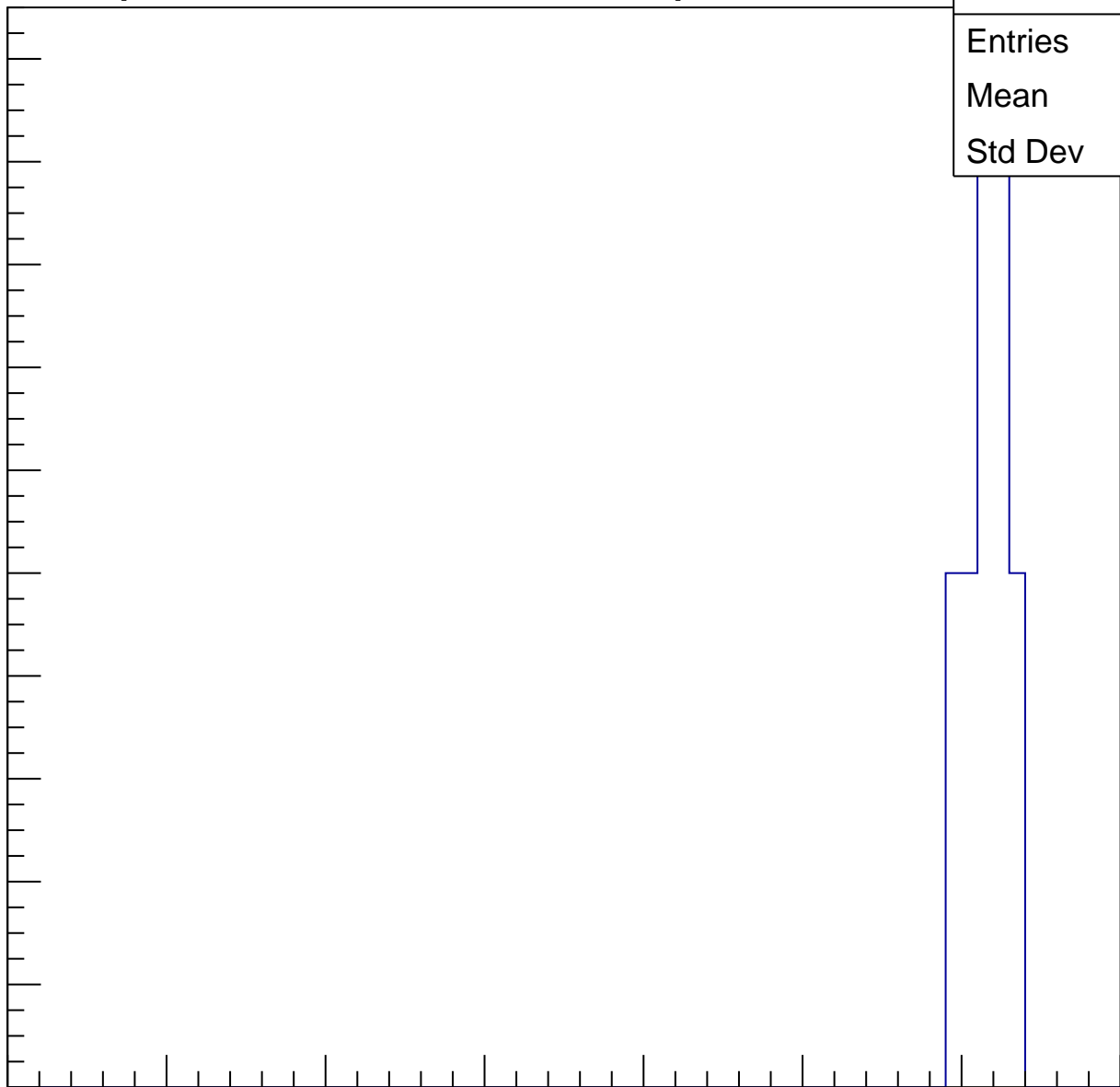
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	7
Mean	61.14
Std Dev	1.245

0 10 20 30 40 50 60 70

ampl





# B1L101S, U3-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U3-ch73, adc0

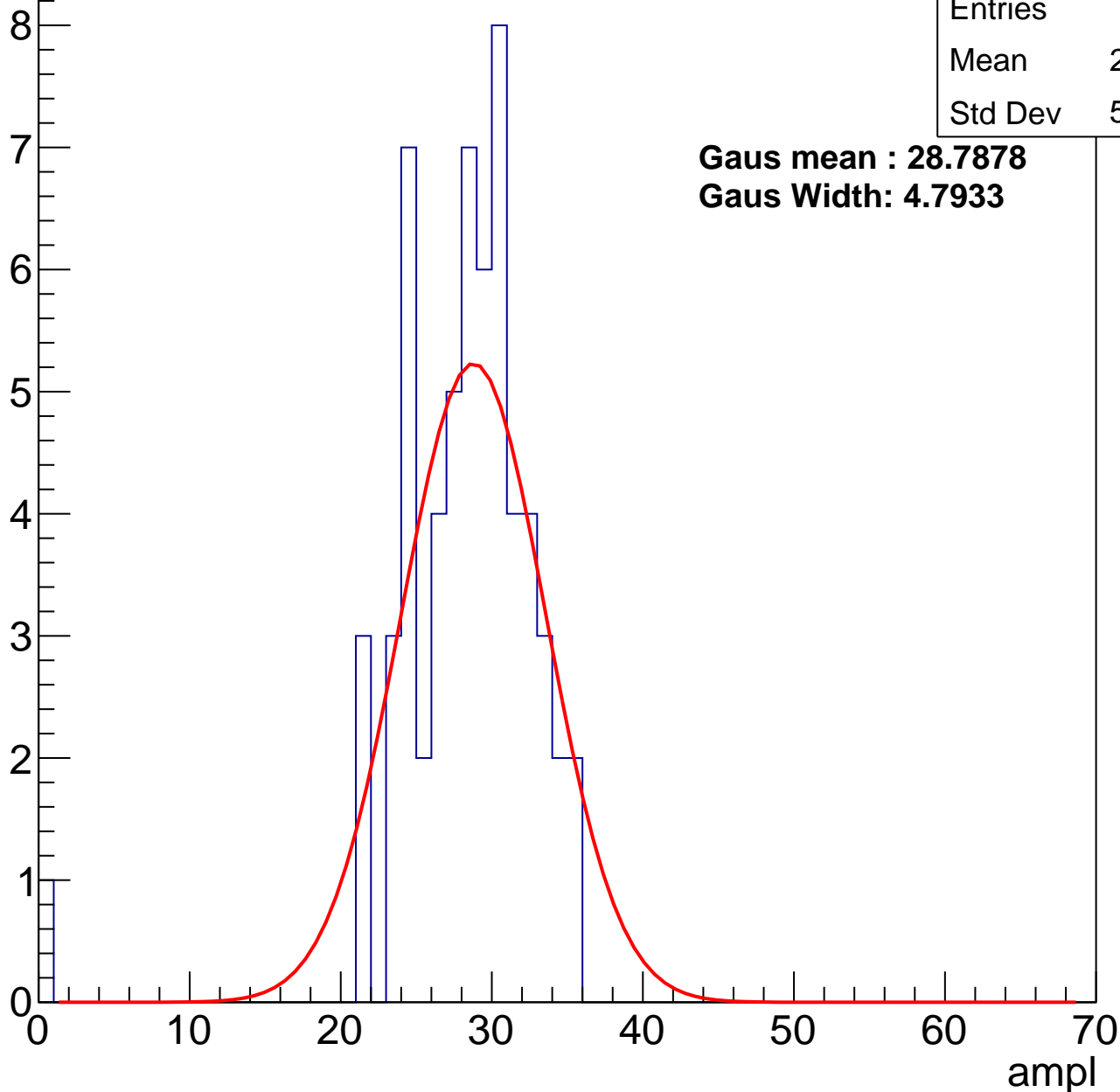
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	27.67
Std Dev	5.014

**Gaus mean : 28.7878**

**Gaus Width: 4.7933**



# B1L101S, U3-ch73, adc1

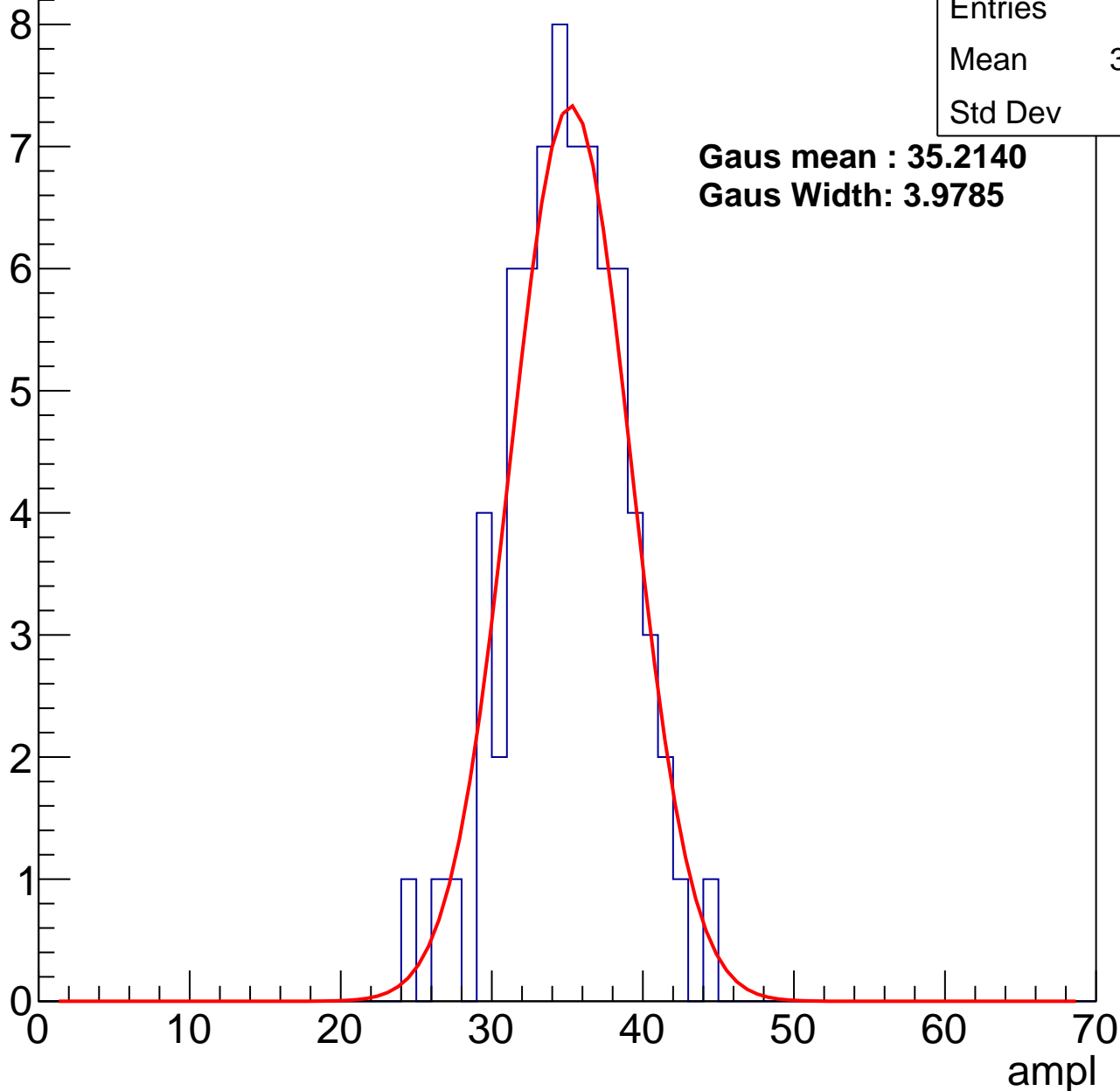
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	34.59
Std Dev	3.81

**Gaus mean : 35.2140**

**Gaus Width: 3.9785**



# B1L101S, U3-ch73, adc2

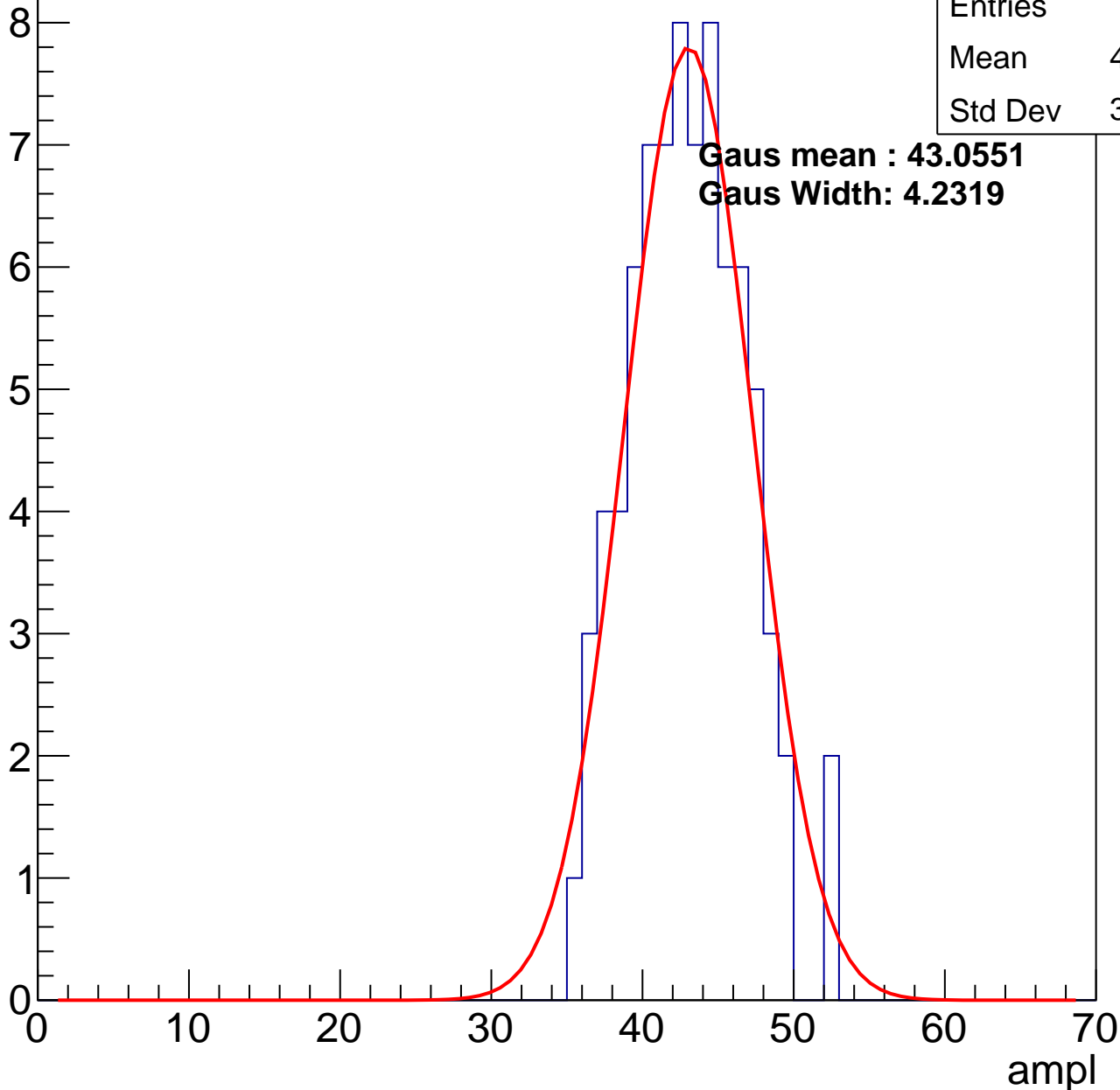
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	42.53
Std Dev	3.744

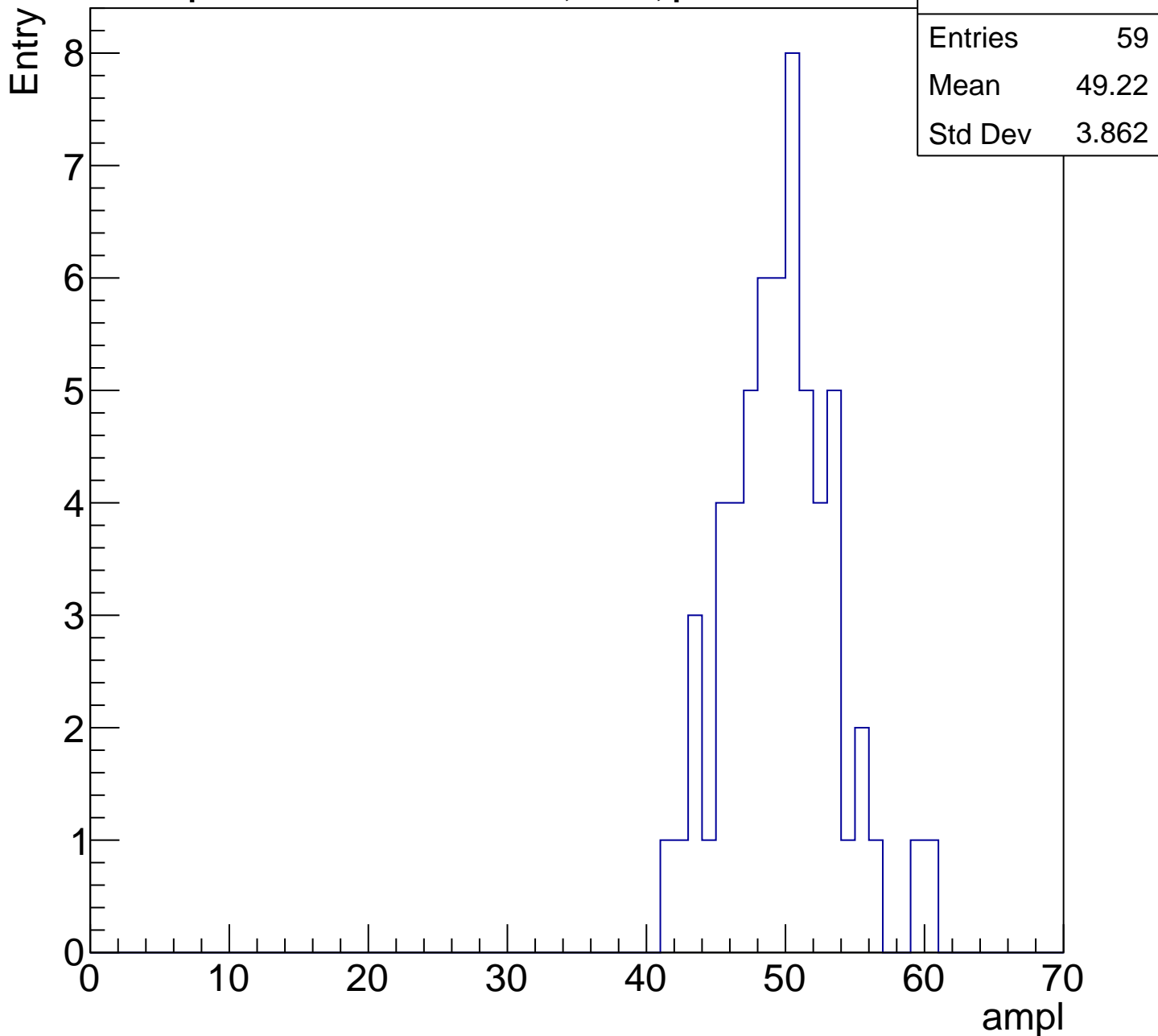
**Gaus mean : 43.0551**

**Gaus Width: 4.2319**



# B1L101S, U3-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

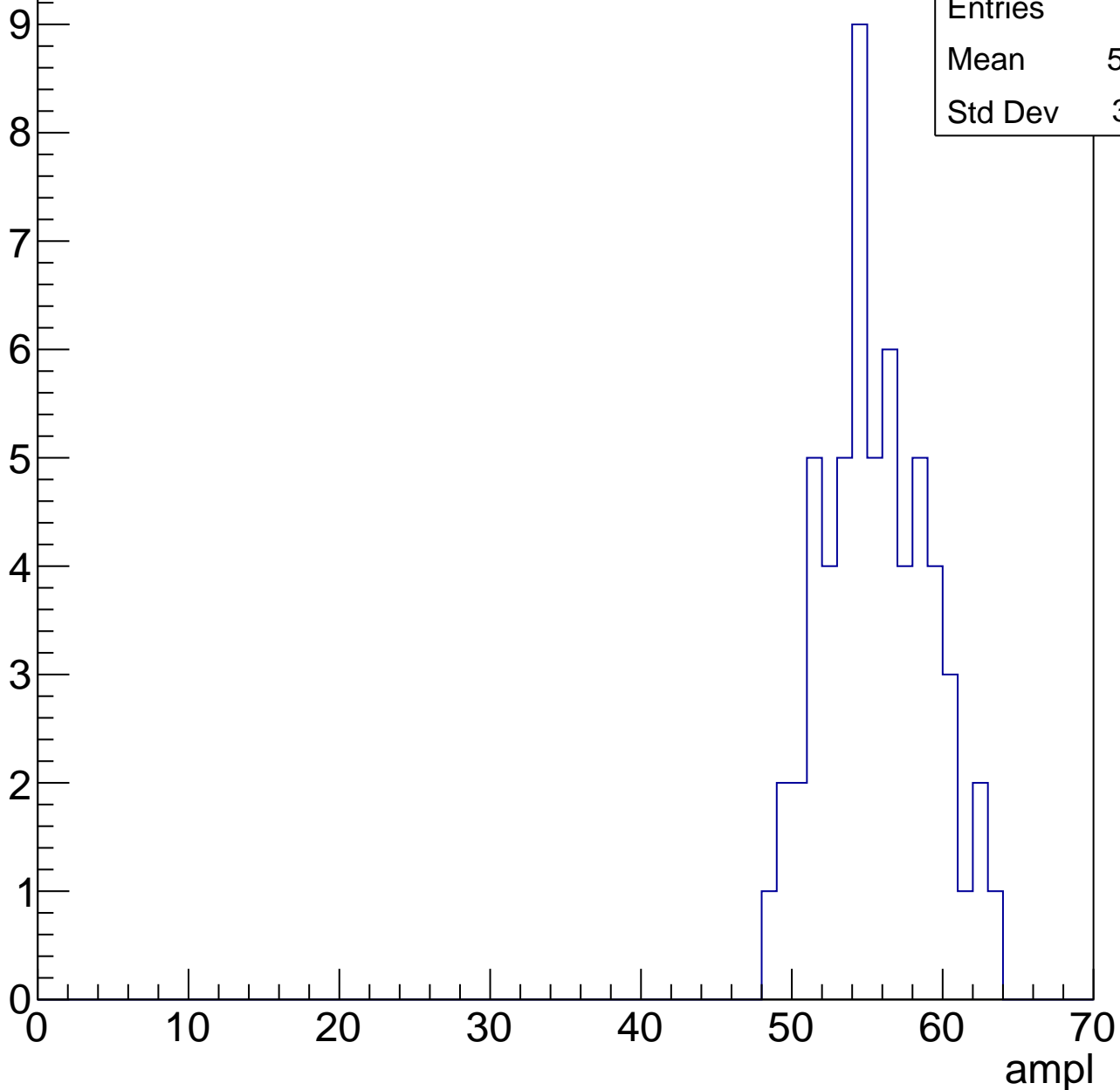


# B1L101S, U3-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	55.14
Std Dev	3.491

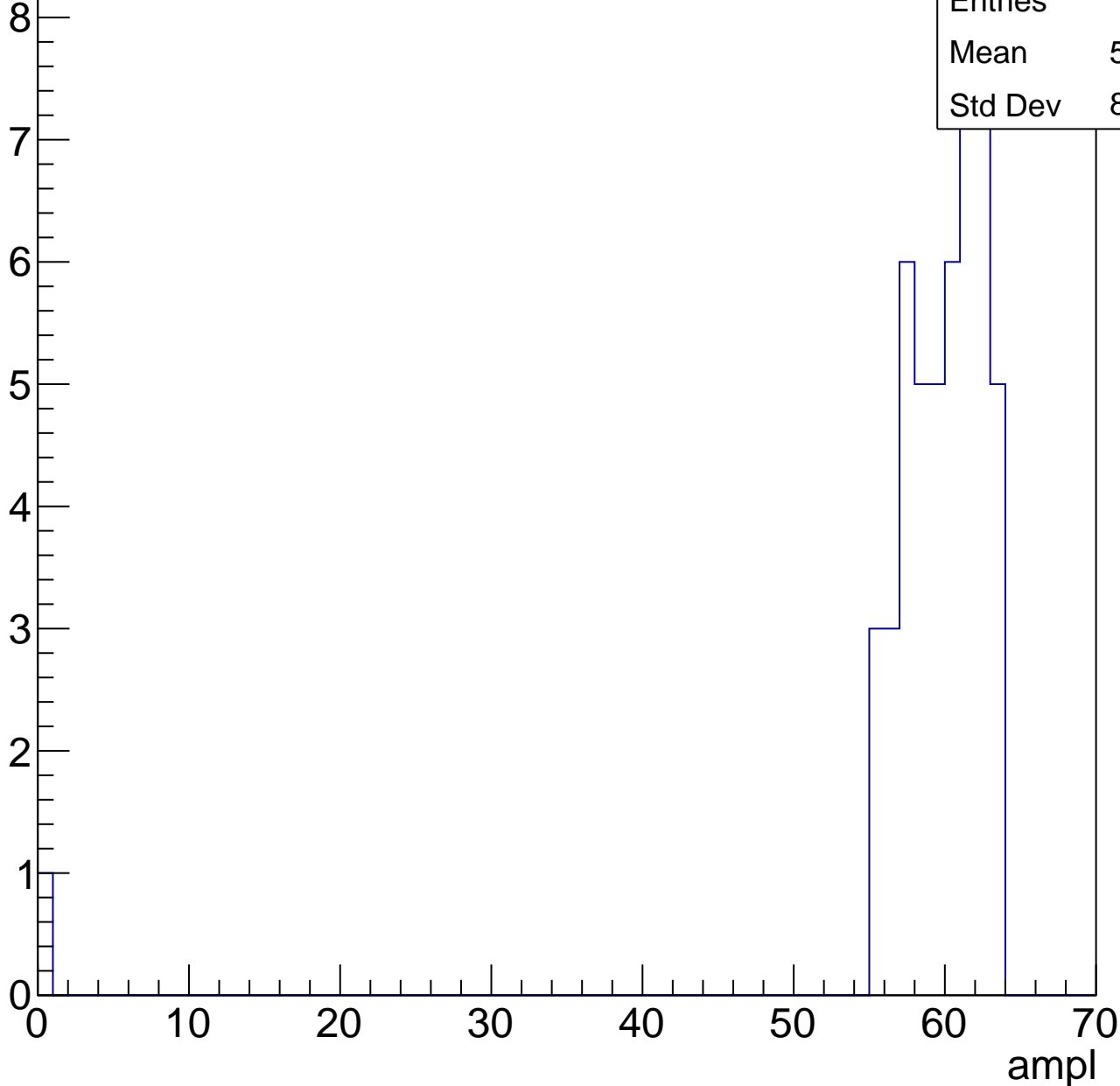


# B1L101S, U3-ch73, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

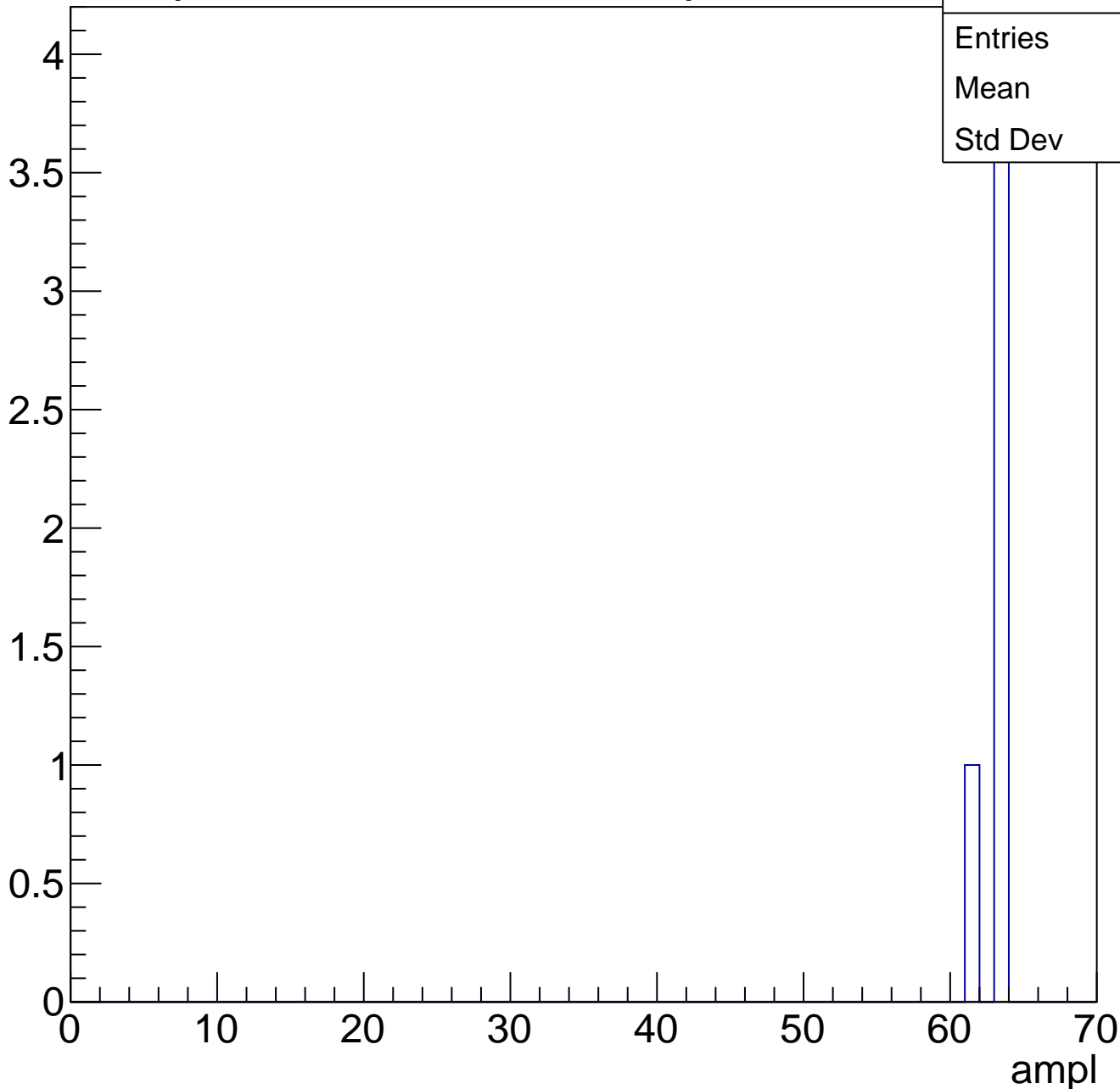
Entries	50
Mean	58.38
Std Dev	8.667



# B1L101S, U3-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U3-ch74, adc0

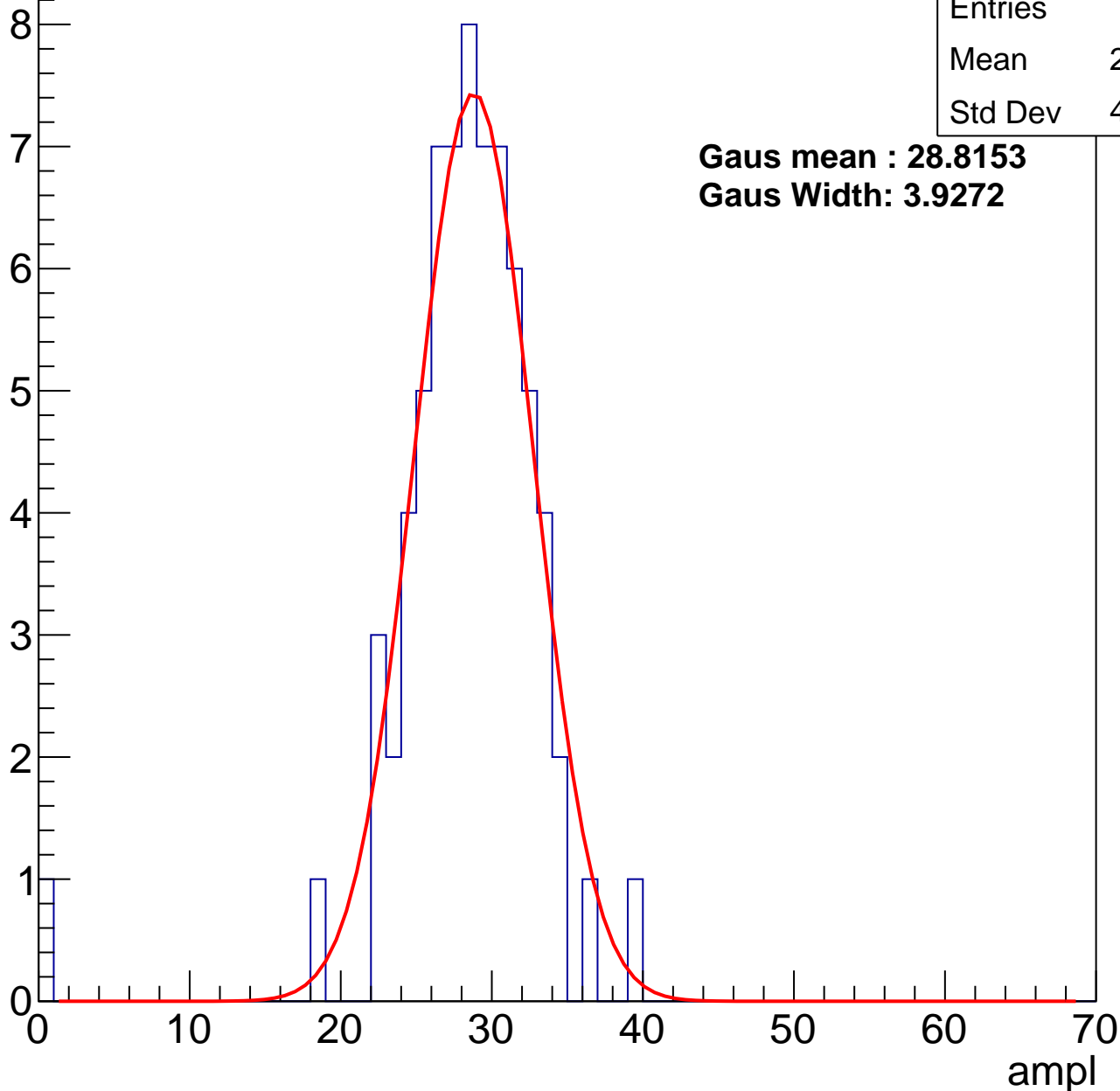
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	27.89
Std Dev	4.909

**Gaus mean : 28.8153**

**Gaus Width: 3.9272**



# B1L101S, U3-ch74, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	71
Mean	35.2
Std Dev	5.45

**Gaus mean : 35.9402**

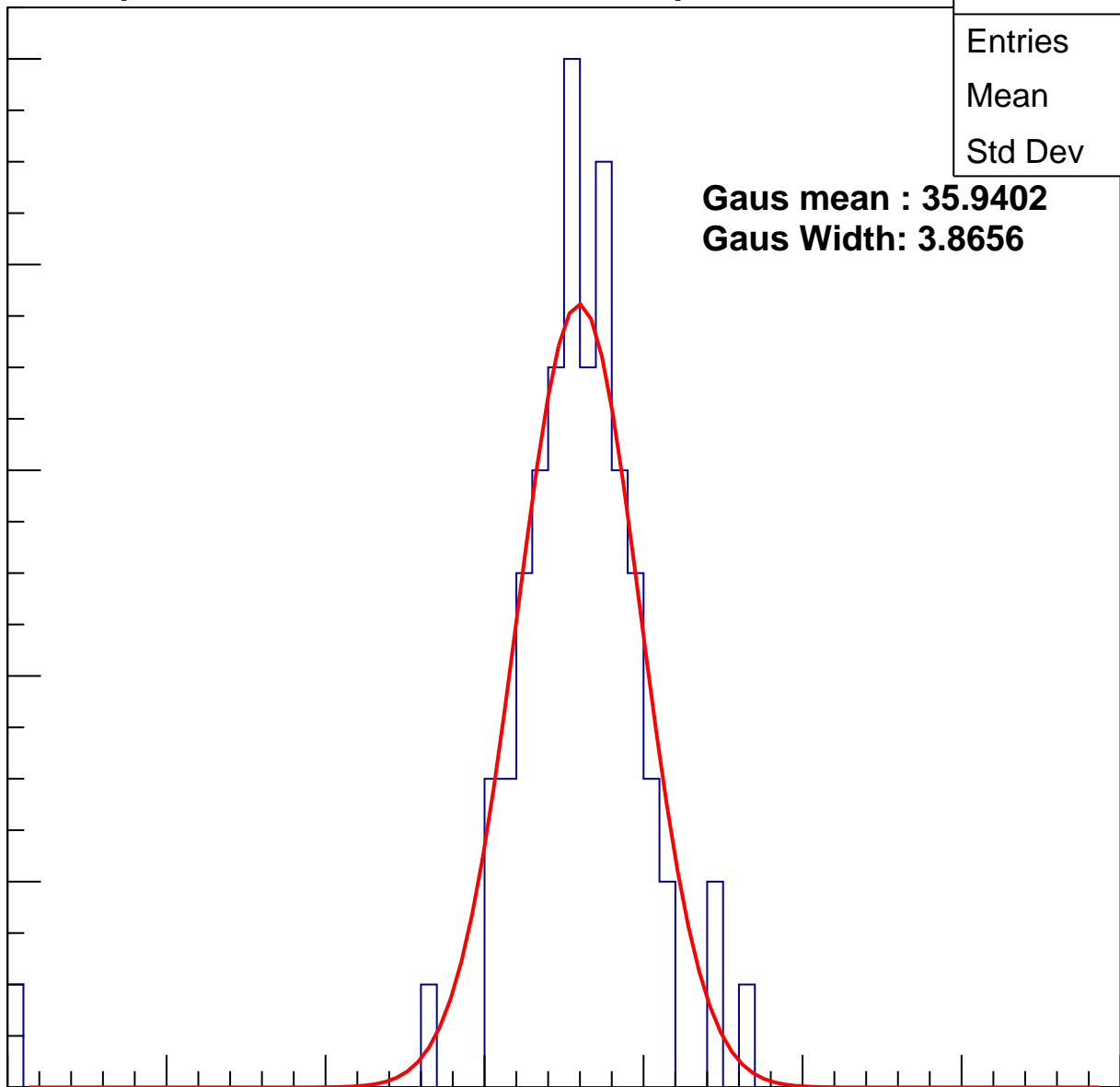
**Gaus Width: 3.8656**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U3-ch74, adc2

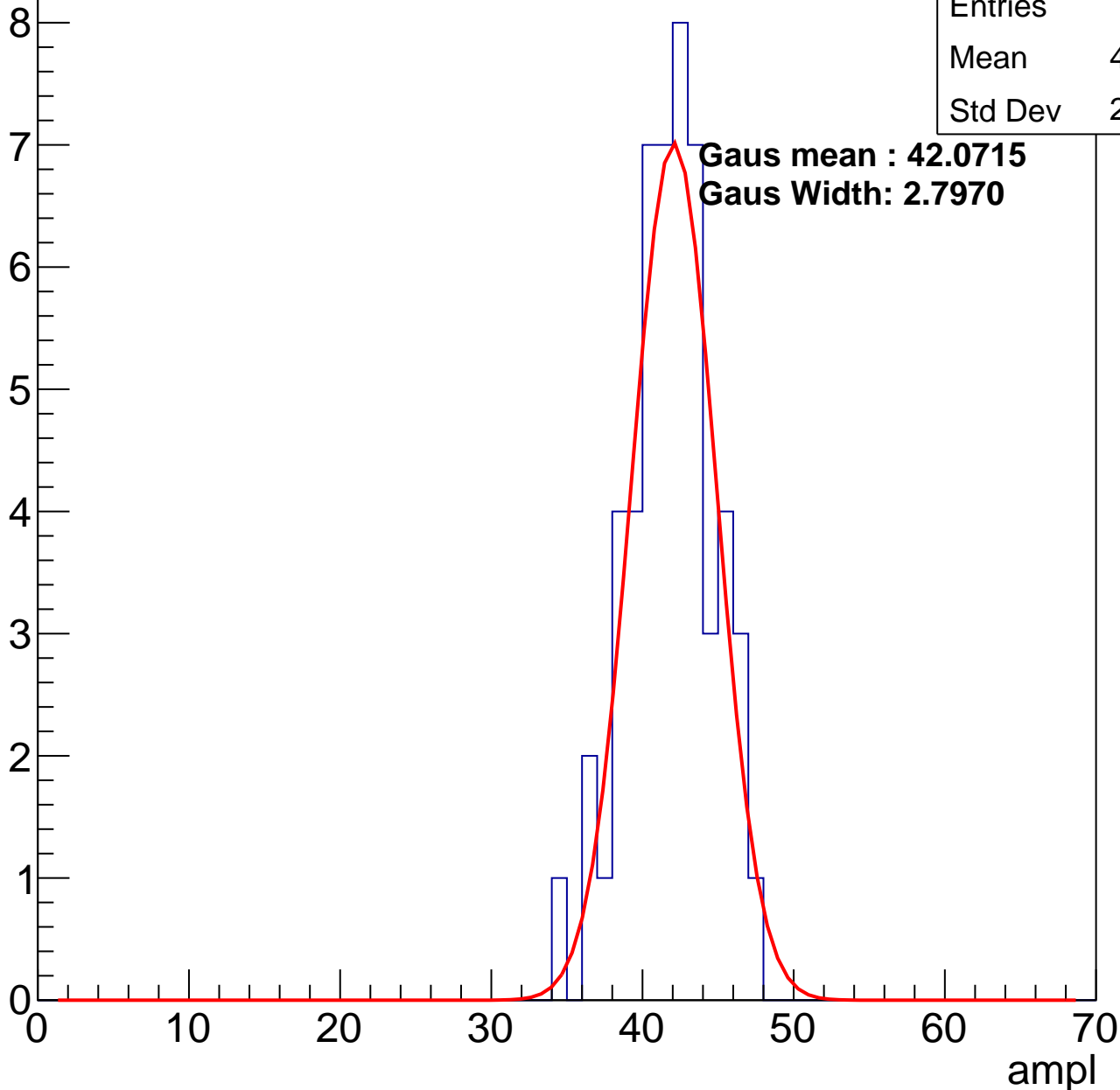
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	41.38
Std Dev	2.788

**Gaus mean : 42.0715**

**Gaus Width: 2.7970**

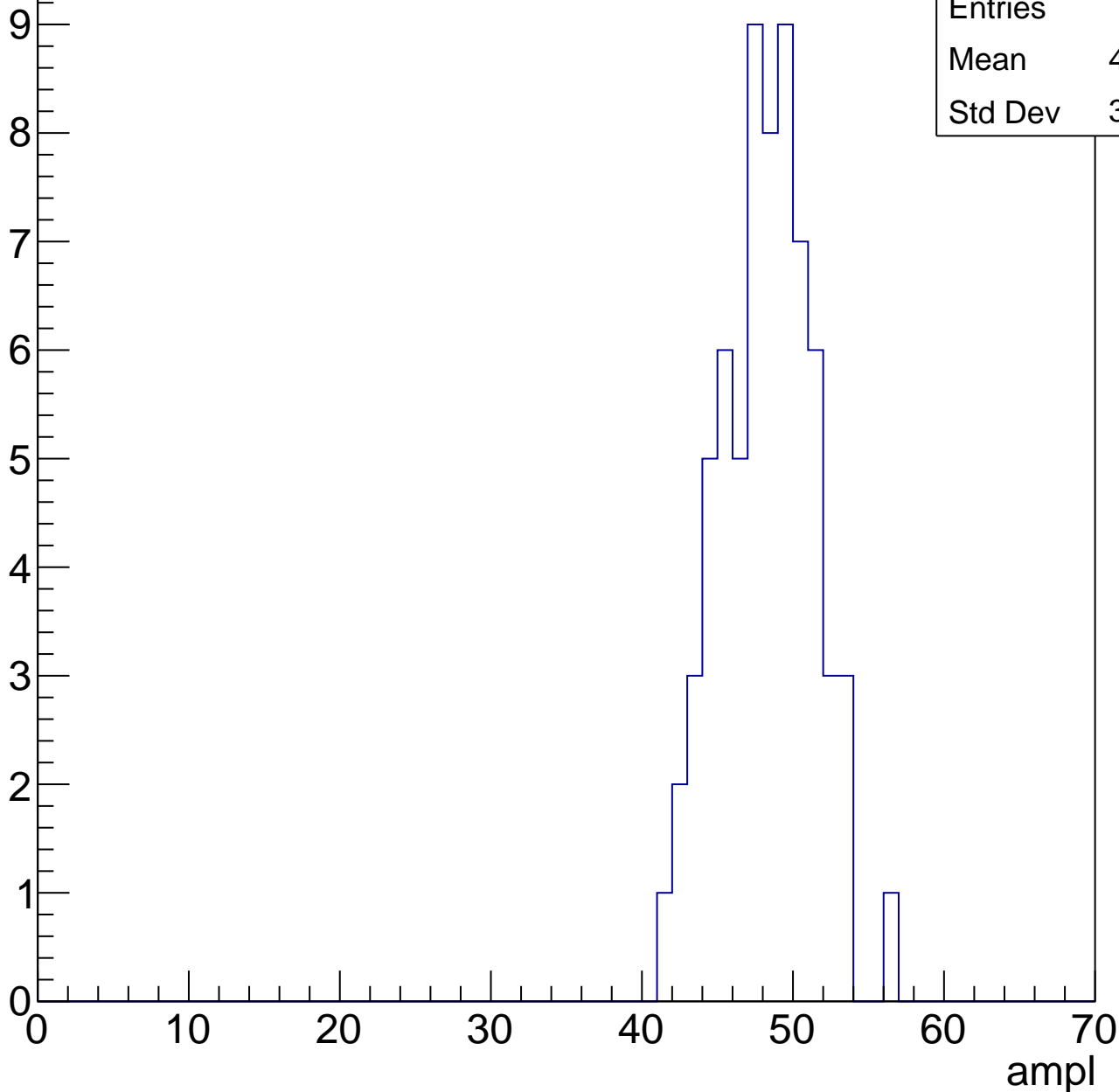


# B1L101S, U3-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	47.78
Std Dev	3.053

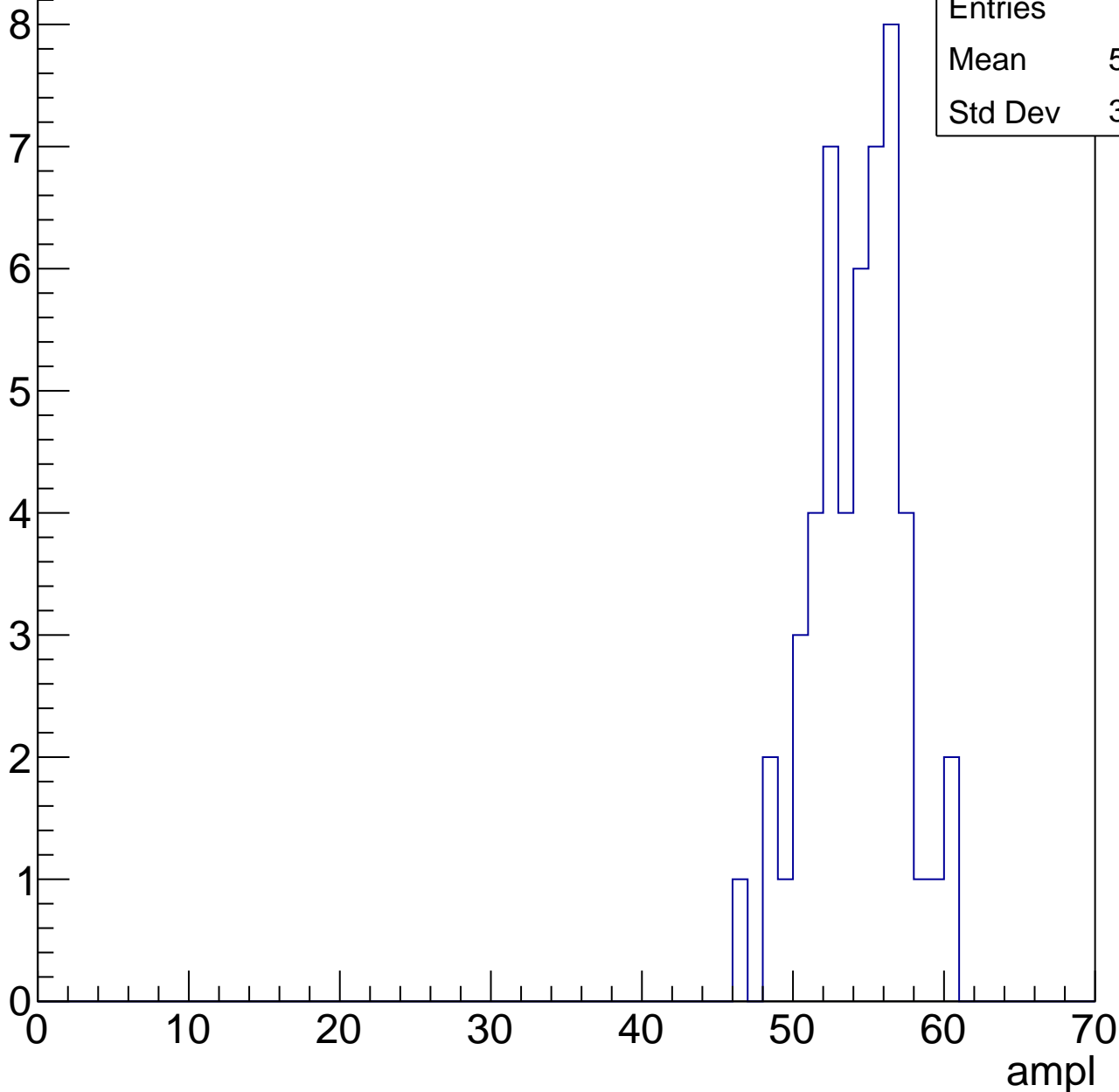


# B1L101S, U3-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	53.78
Std Dev	3.012

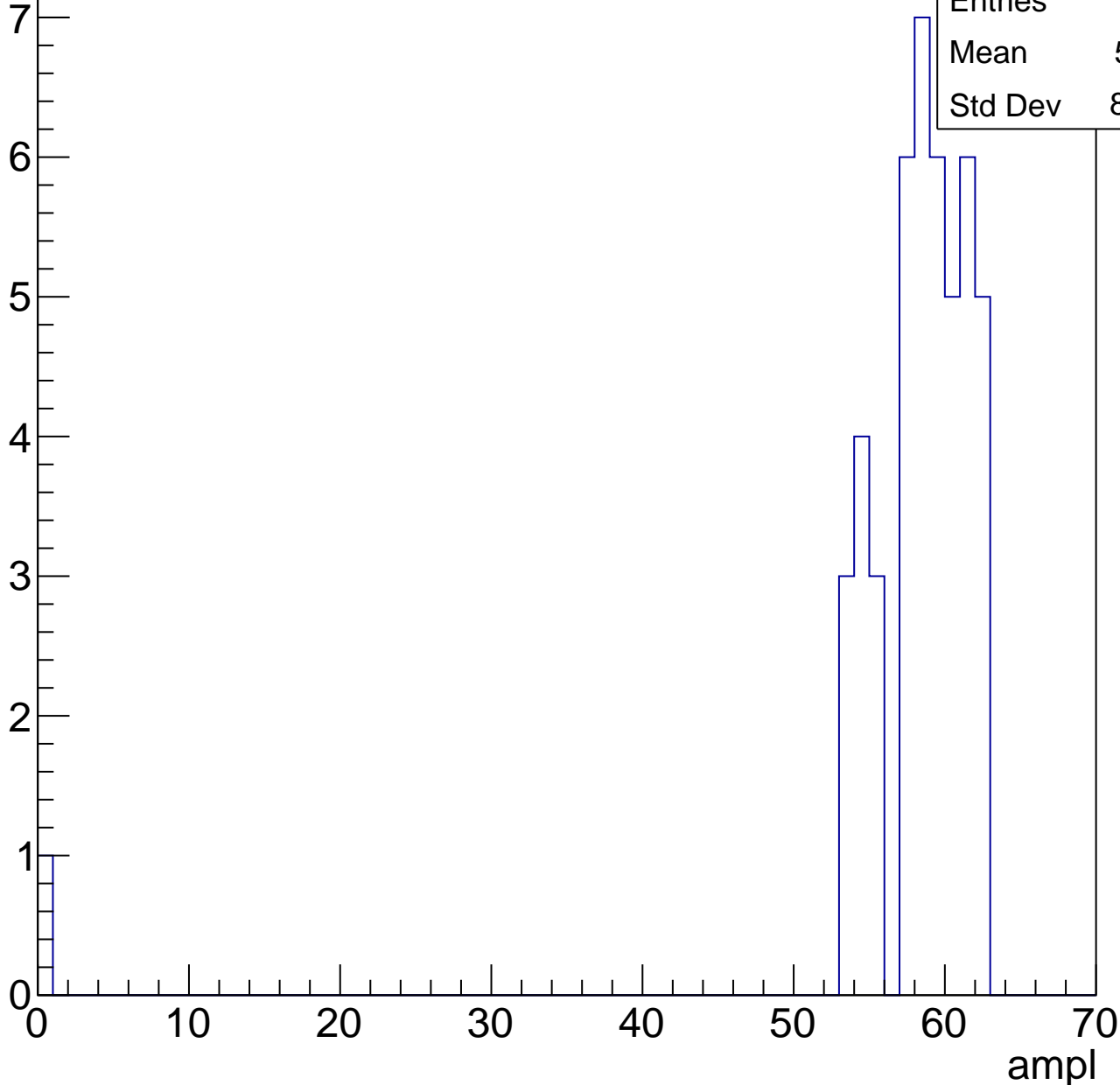


# B1L101S, U3-ch74, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	56.91
Std Dev	8.898

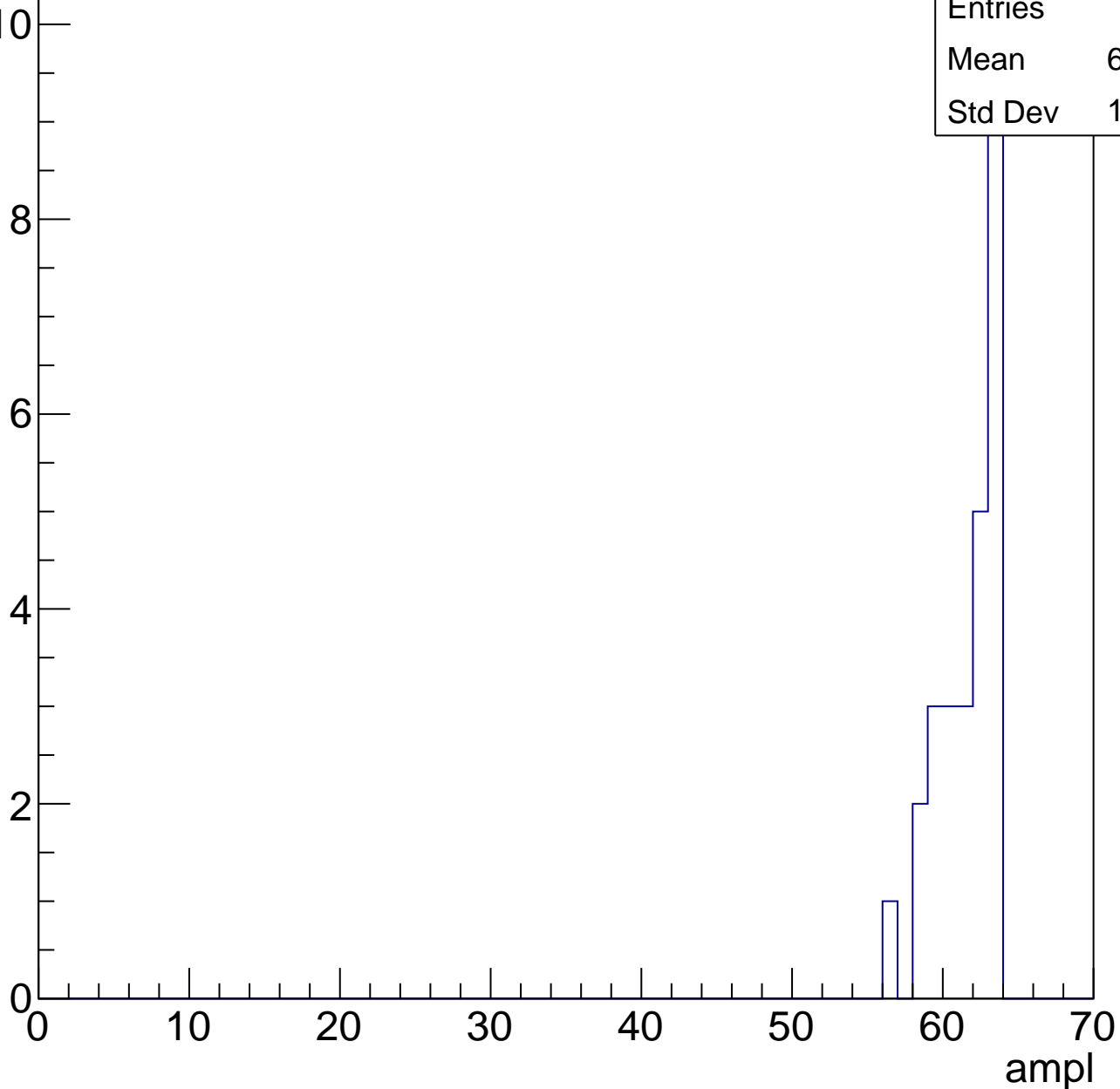


# B1L101S, U3-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	27
Mean	61.19
Std Dev	1.944

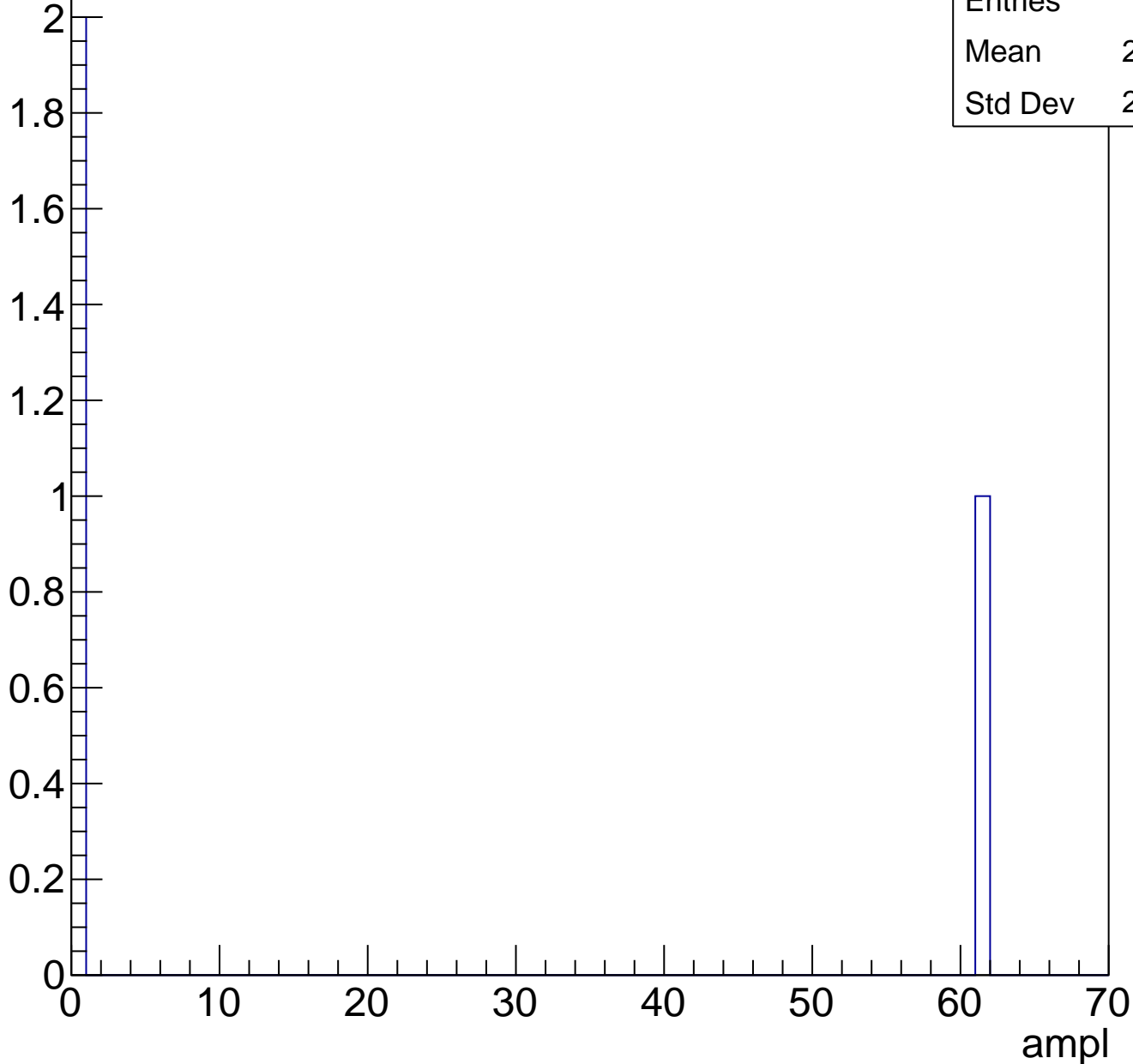




# B1L101S, U3-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch75, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	76
Mean	25.71
Std Dev	4.585

**Gaus mean : 26.8941**

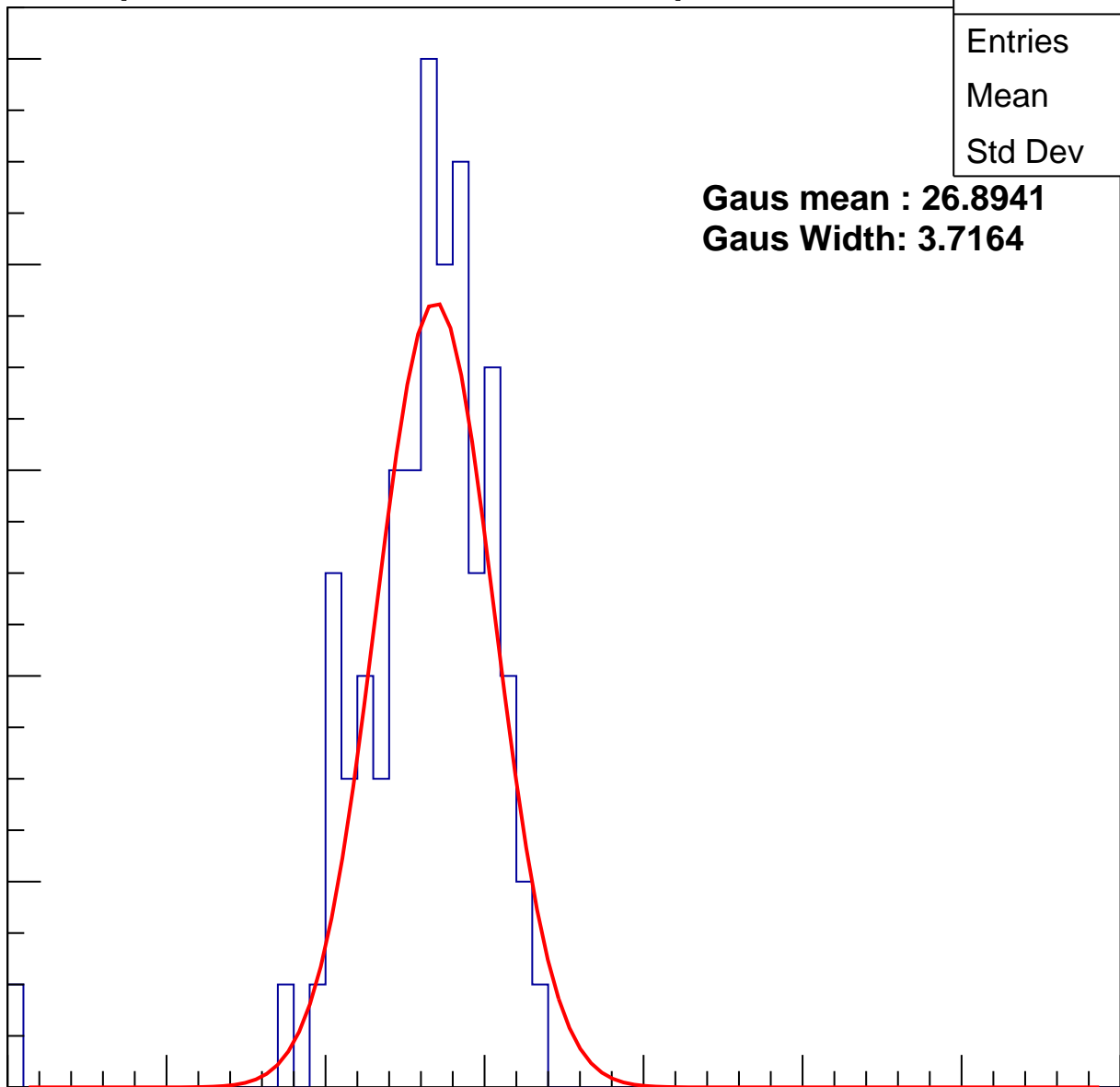
**Gaus Width: 3.7164**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U3-ch75, adc1

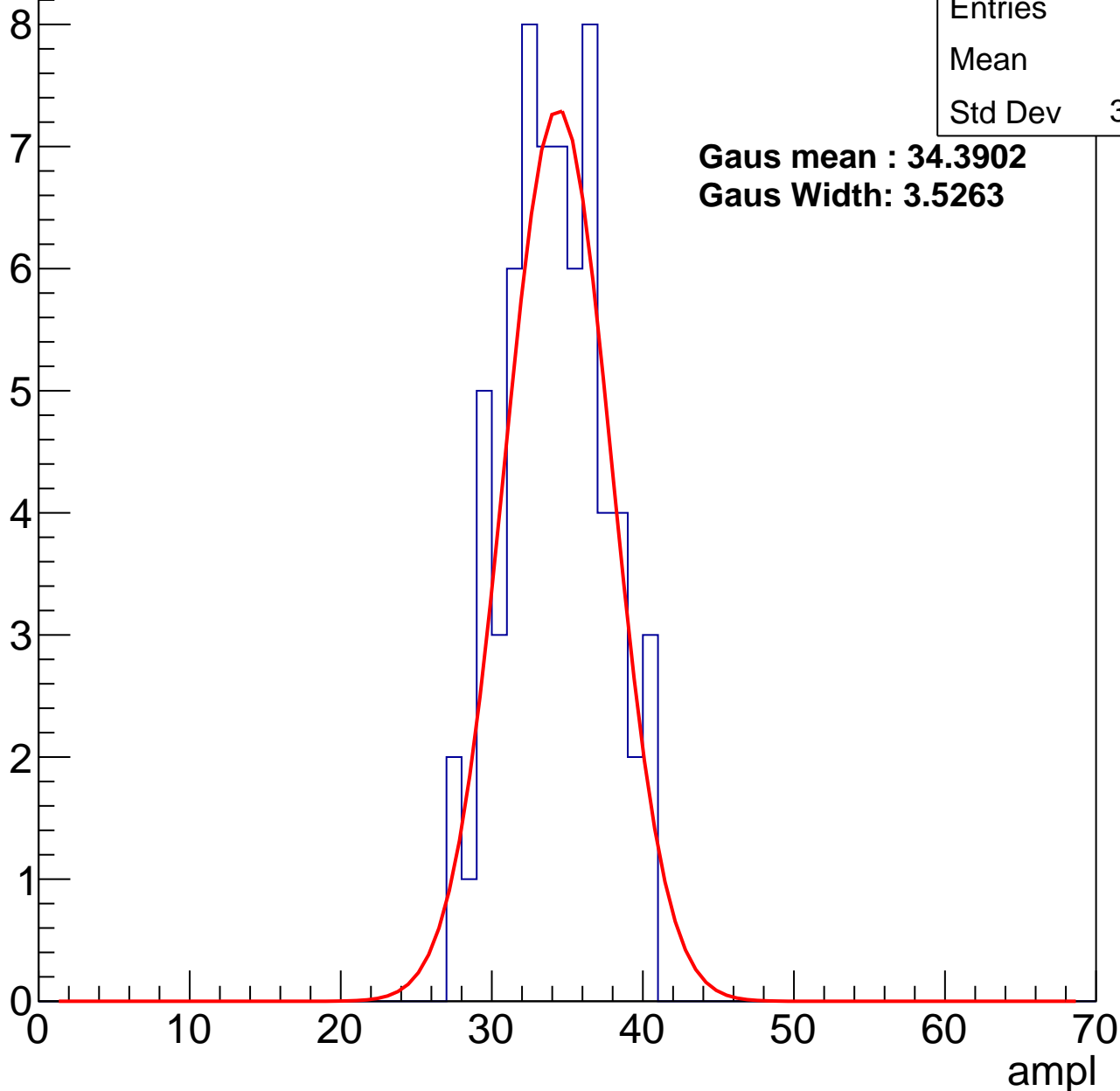
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	33.7
Std Dev	3.233

**Gaus mean : 34.3902**

**Gaus Width: 3.5263**



# B1L101S, U3-ch75, adc2

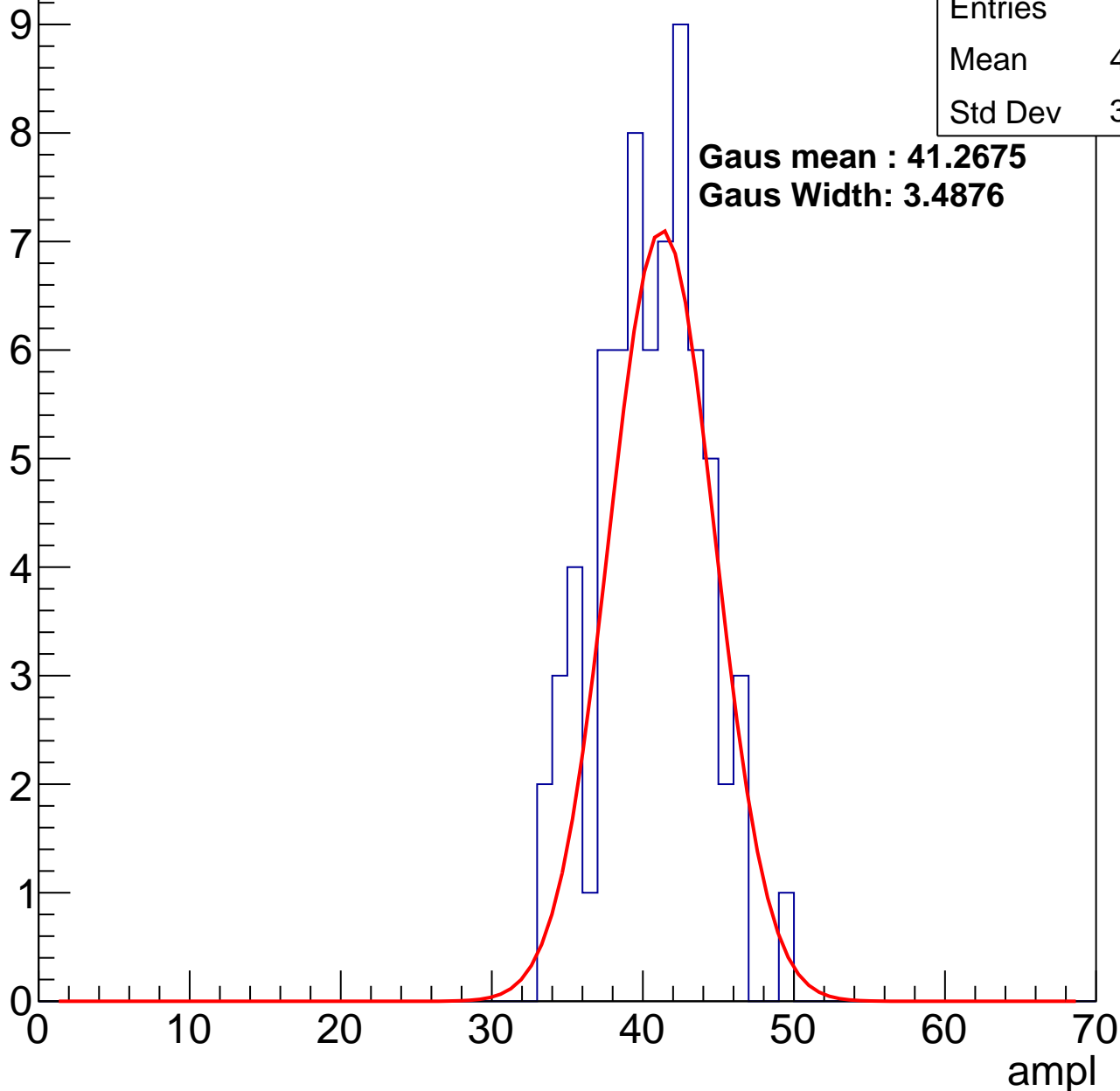
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	40.09
Std Dev	3.455

**Gaus mean : 41.2675**

**Gaus Width: 3.4876**

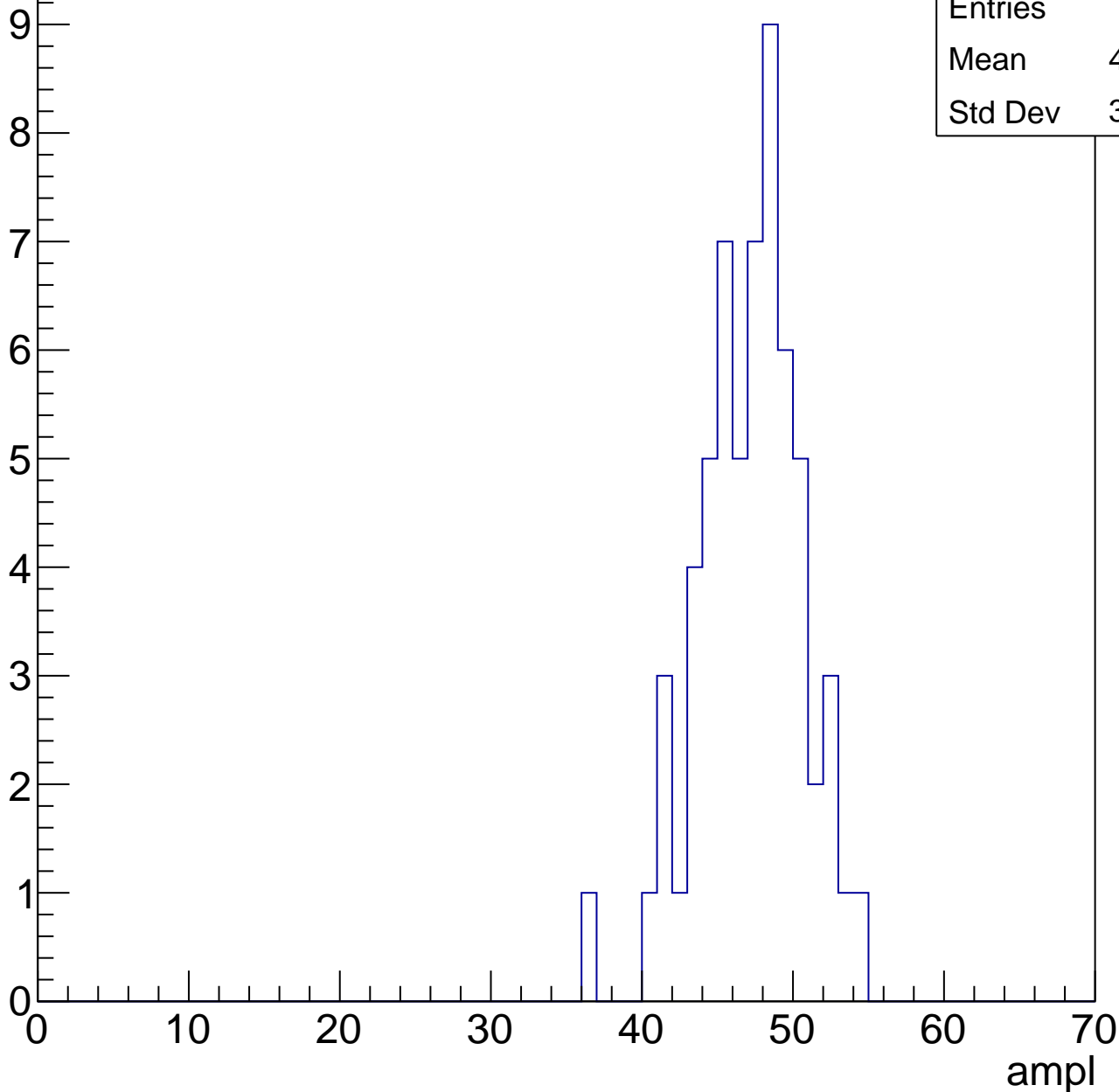


# B1L101S, U3-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	46.69
Std Dev	3.409

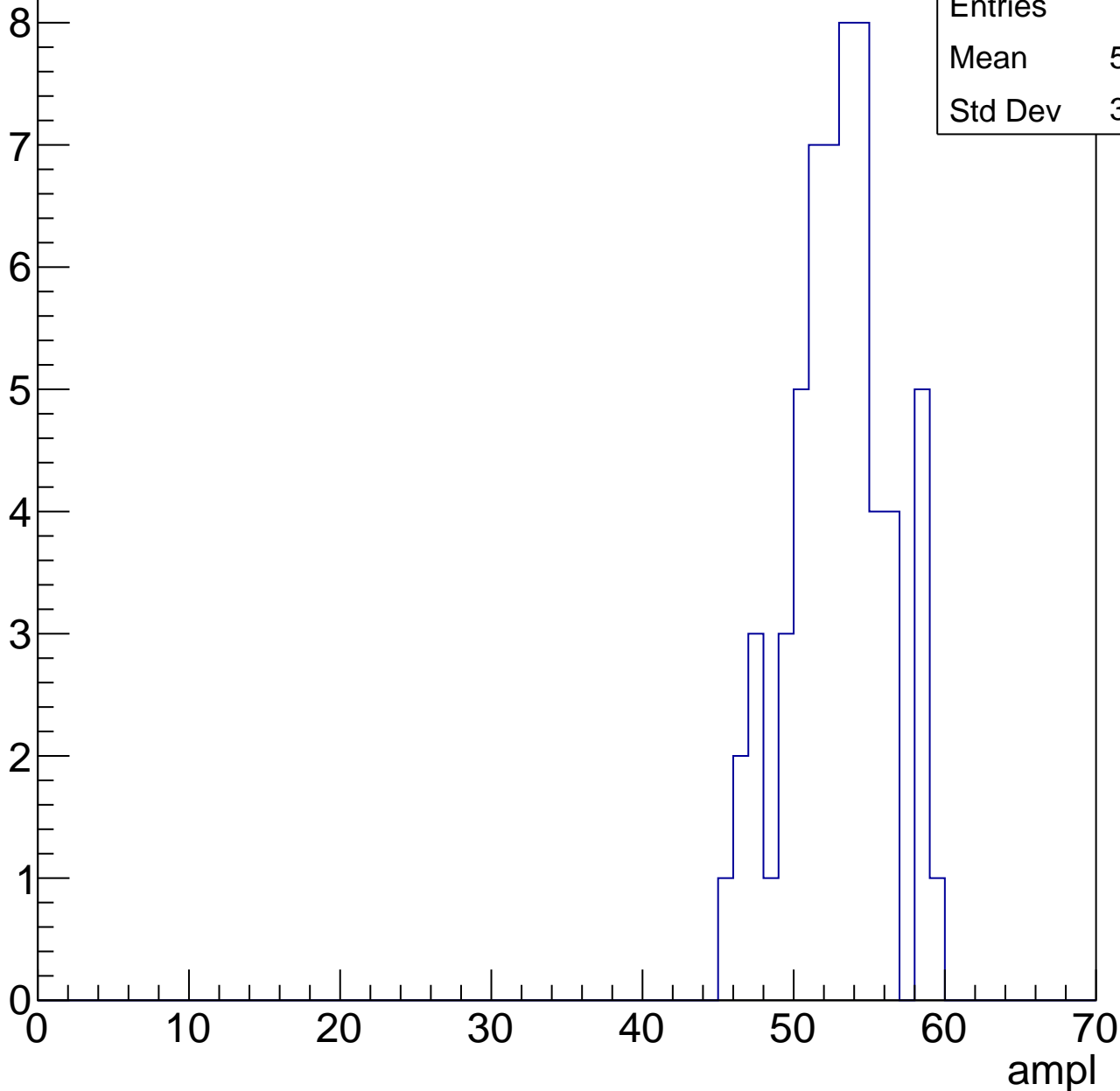


# B1L101S, U3-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

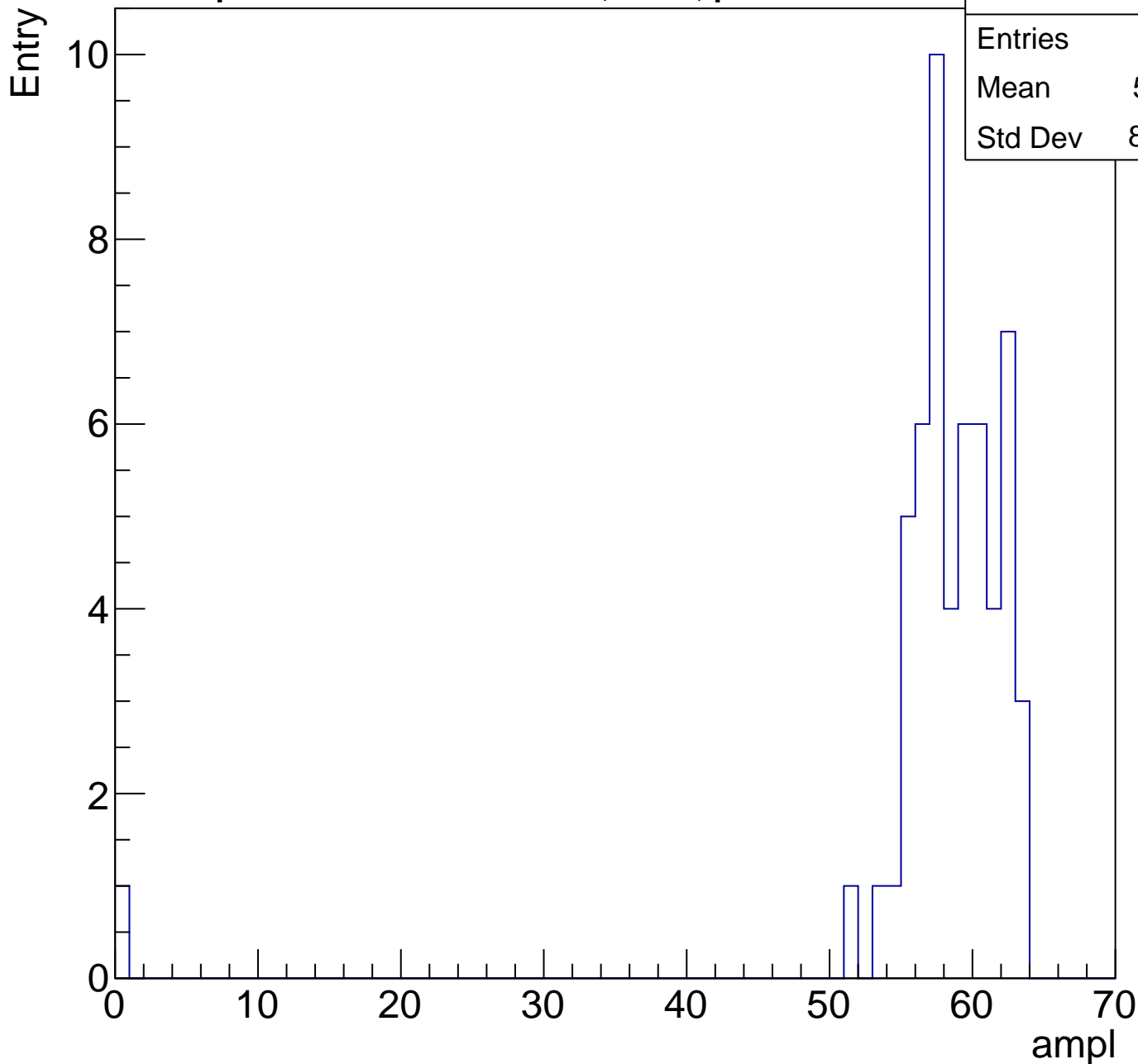
Entries	59
Mean	52.42
Std Dev	3.253



# B1L101S, U3-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	55
Mean	57.31
Std Dev	8.268

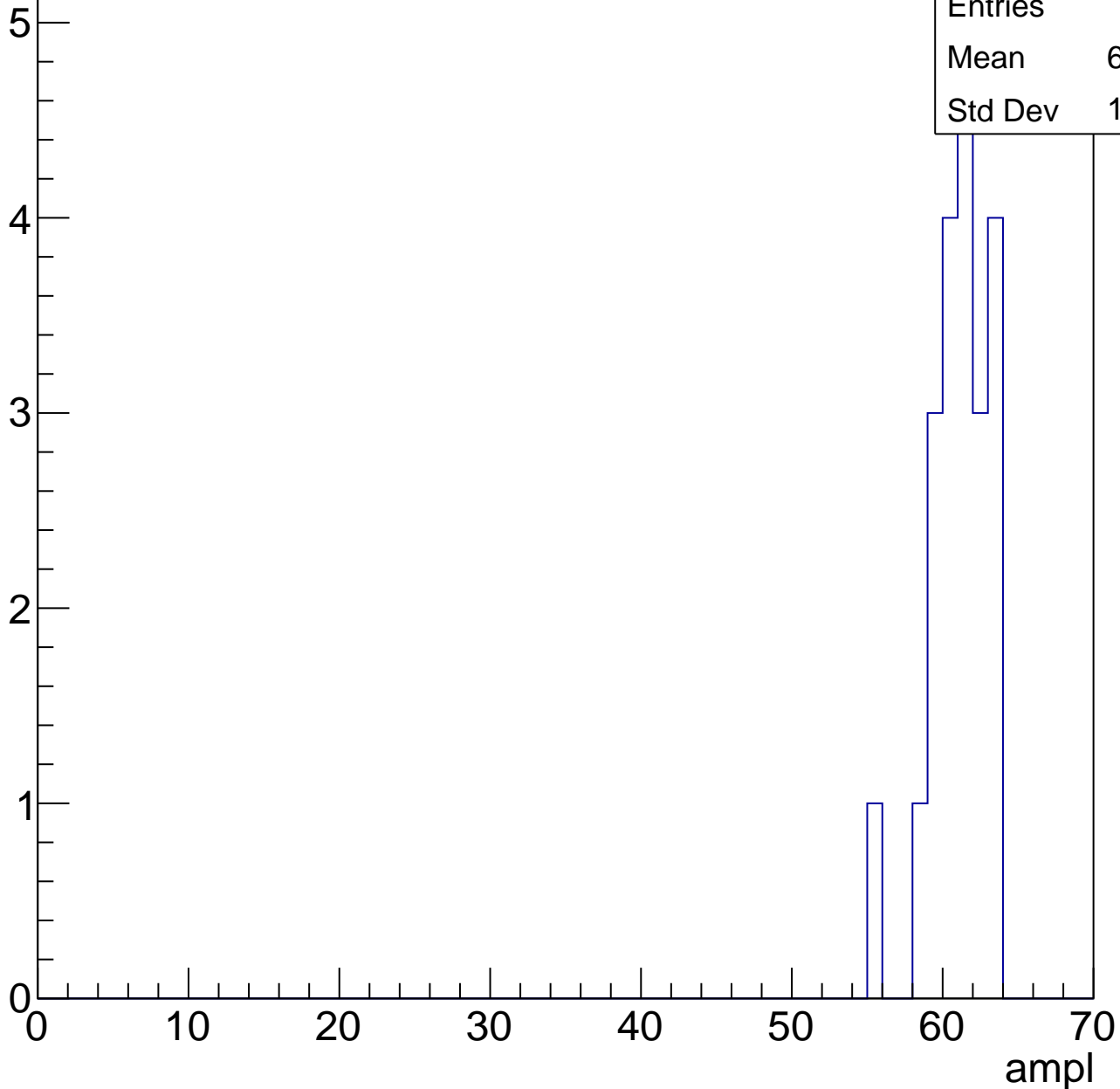


# B1L101S, U3-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	21
Mean	60.62
Std Dev	1.914

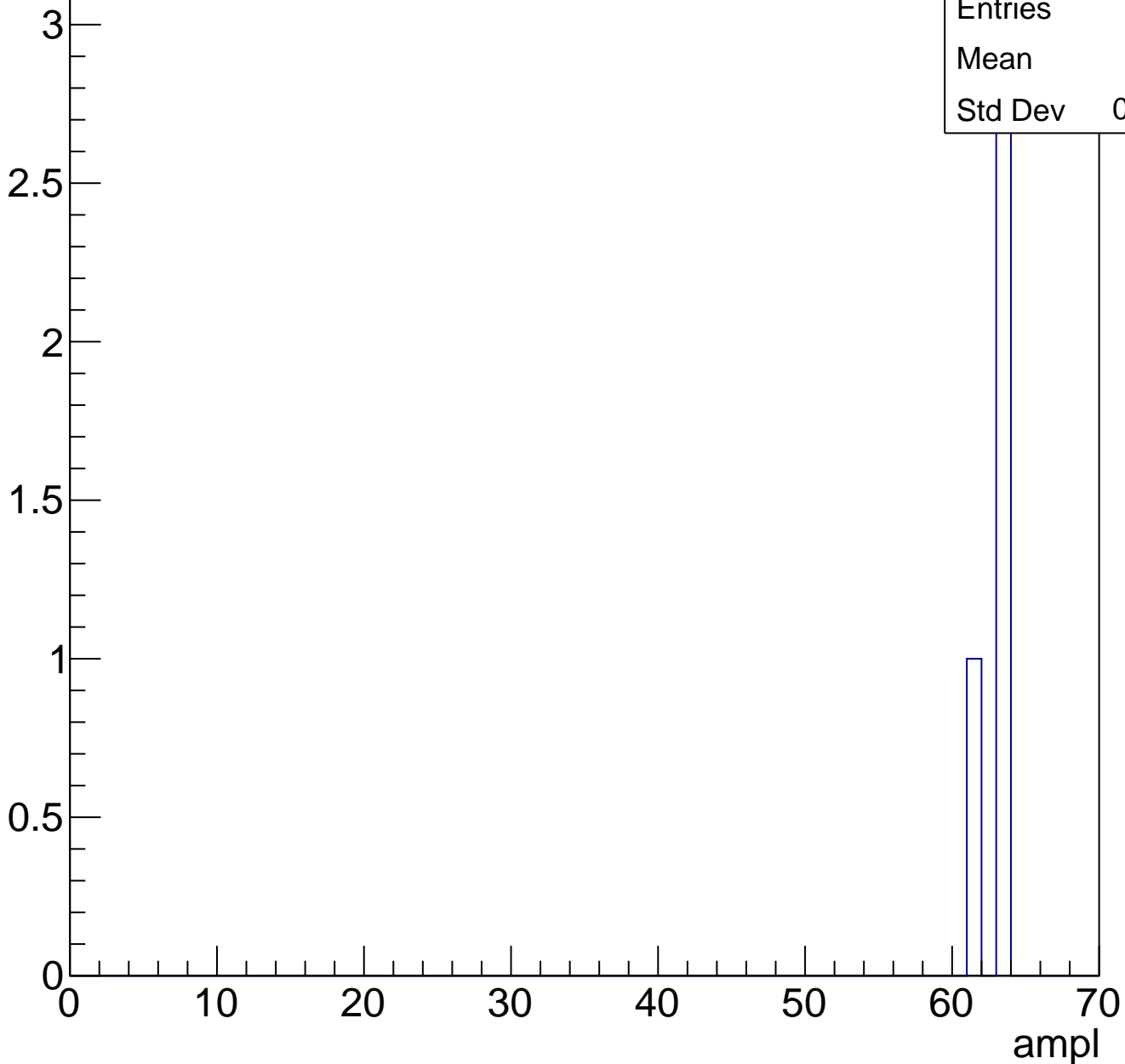




# B1L101S, U3-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



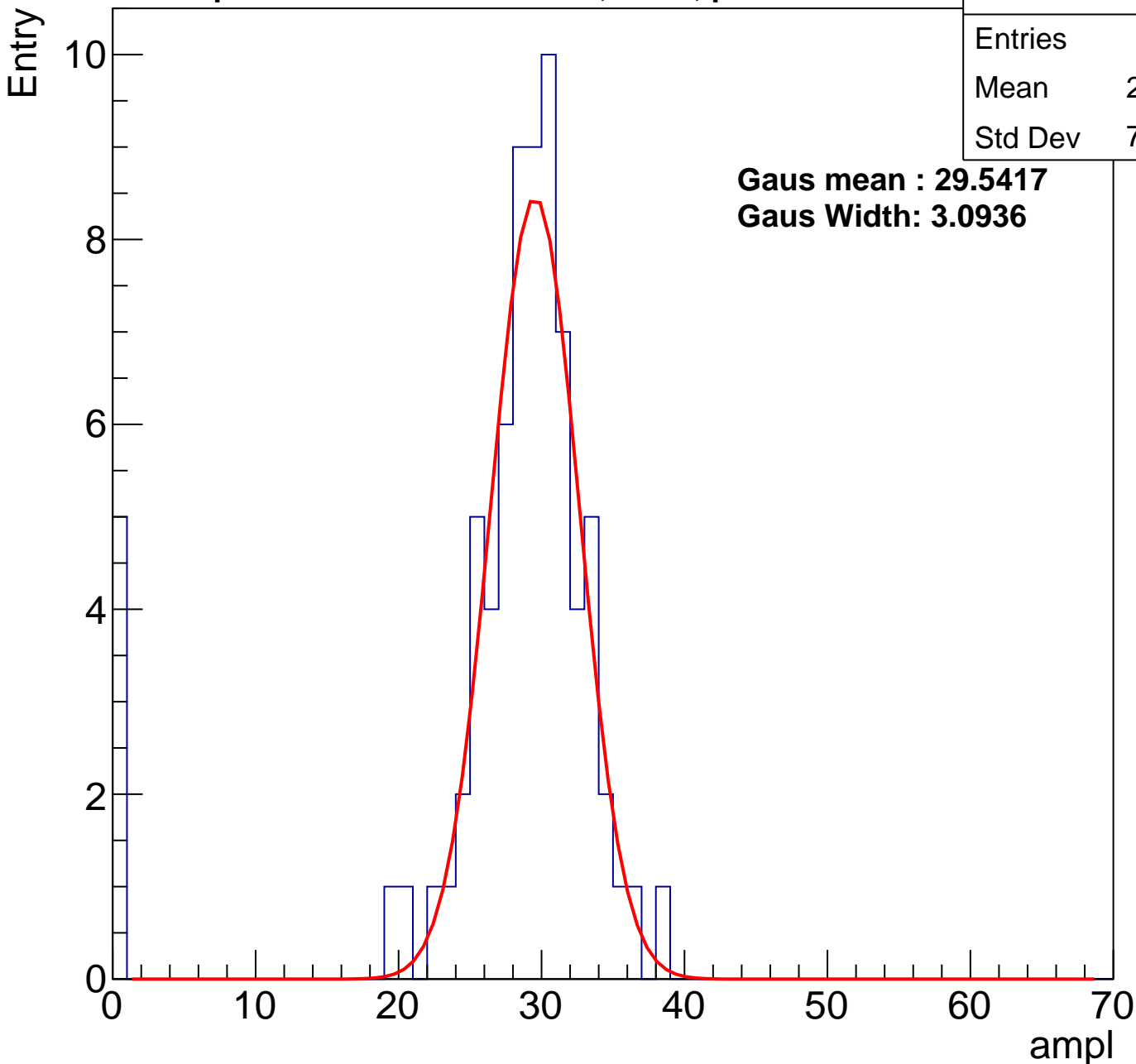
# B1L101S, U3-ch76, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	75
Mean	26.97
Std Dev	7.943

**Gaus mean : 29.5417**

**Gaus Width: 3.0936**



# B1L101S, U3-ch76, adc1

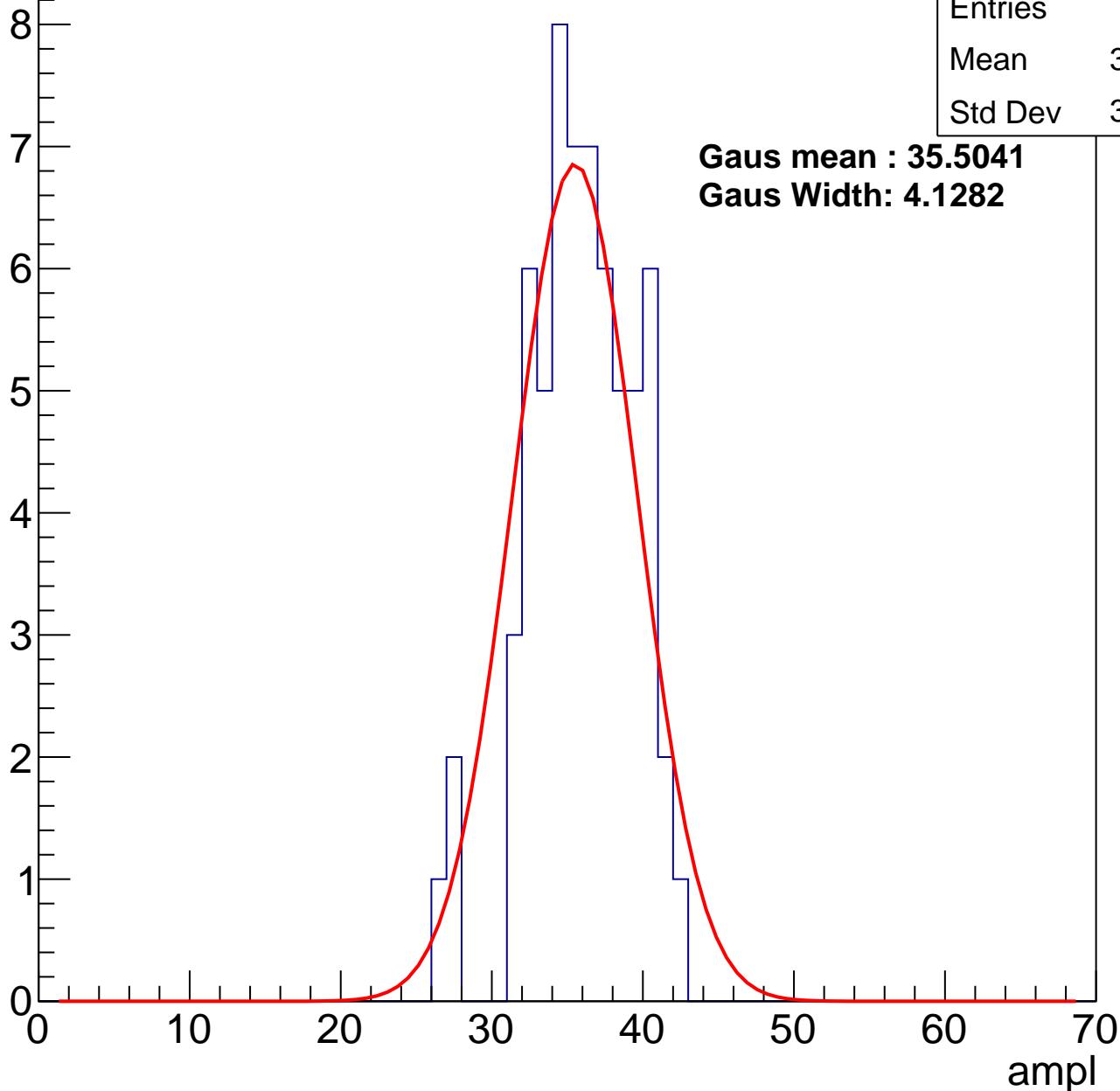
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	35.47
Std Dev	3.428

**Gaus mean : 35.5041**

**Gaus Width: 4.1282**



# B1L101S, U3-ch76, adc2

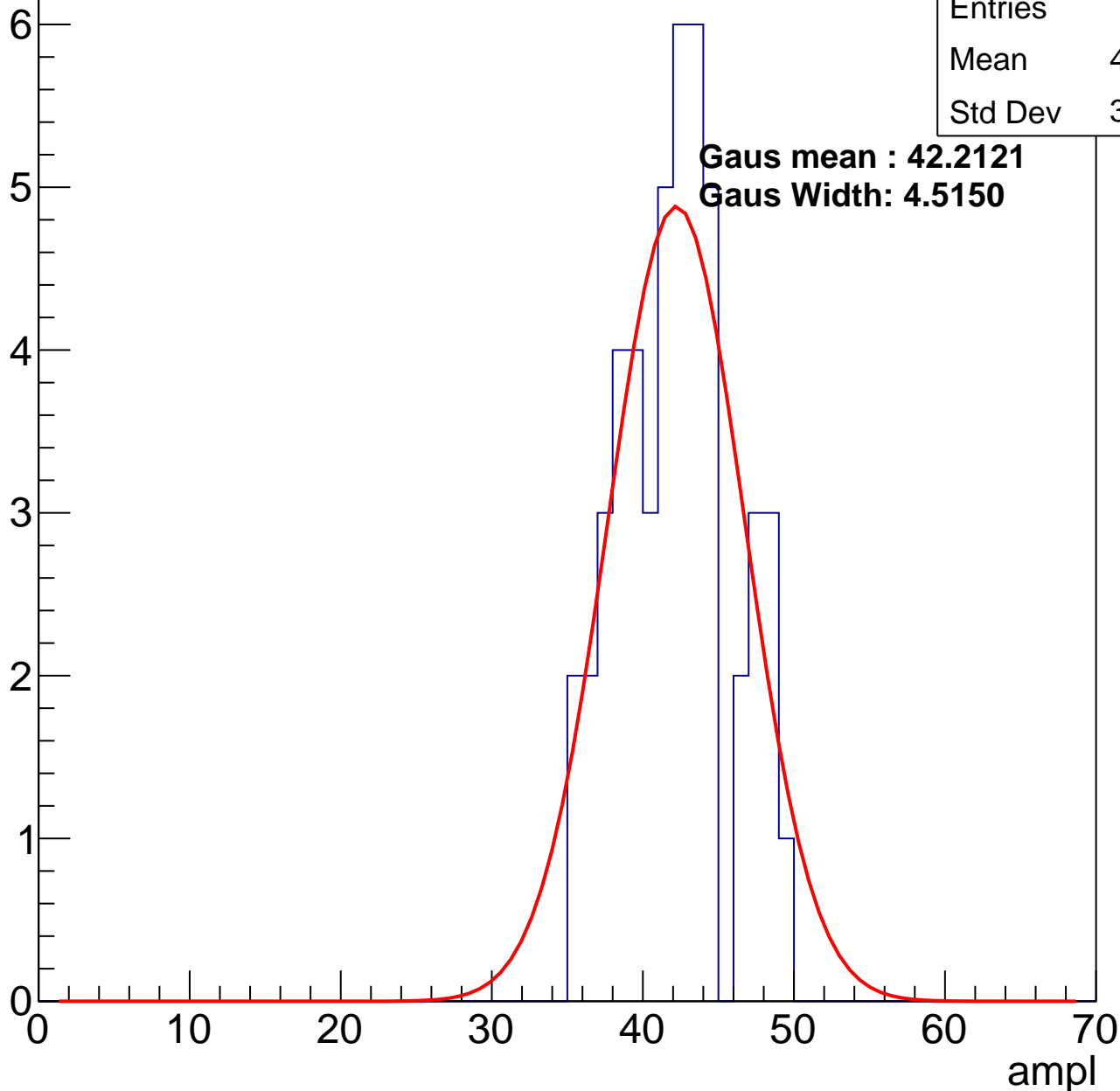
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	41.67
Std Dev	3.633

**Gaus mean : 42.2121**

**Gaus Width: 4.5150**

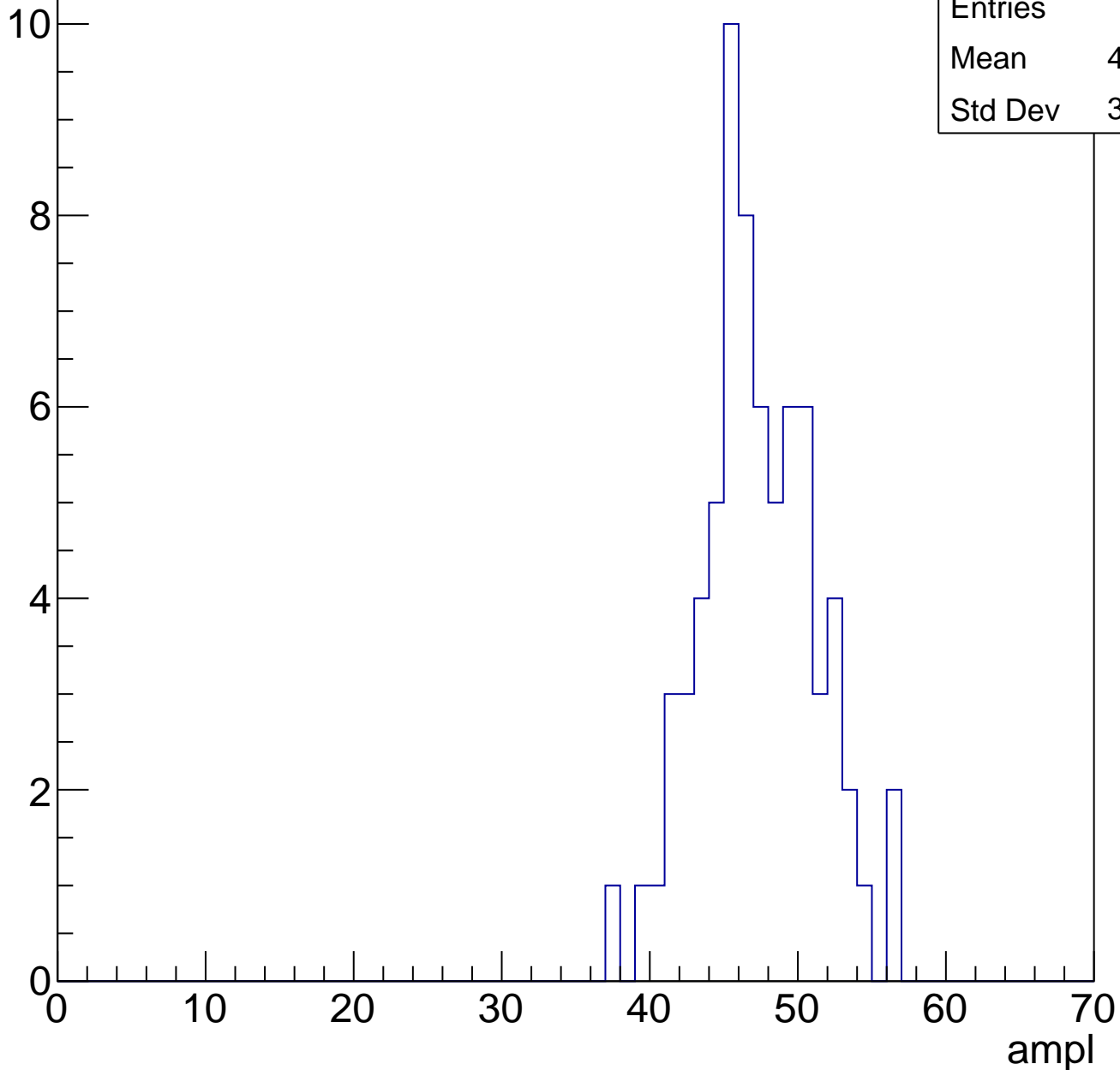


# B1L101S, U3-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

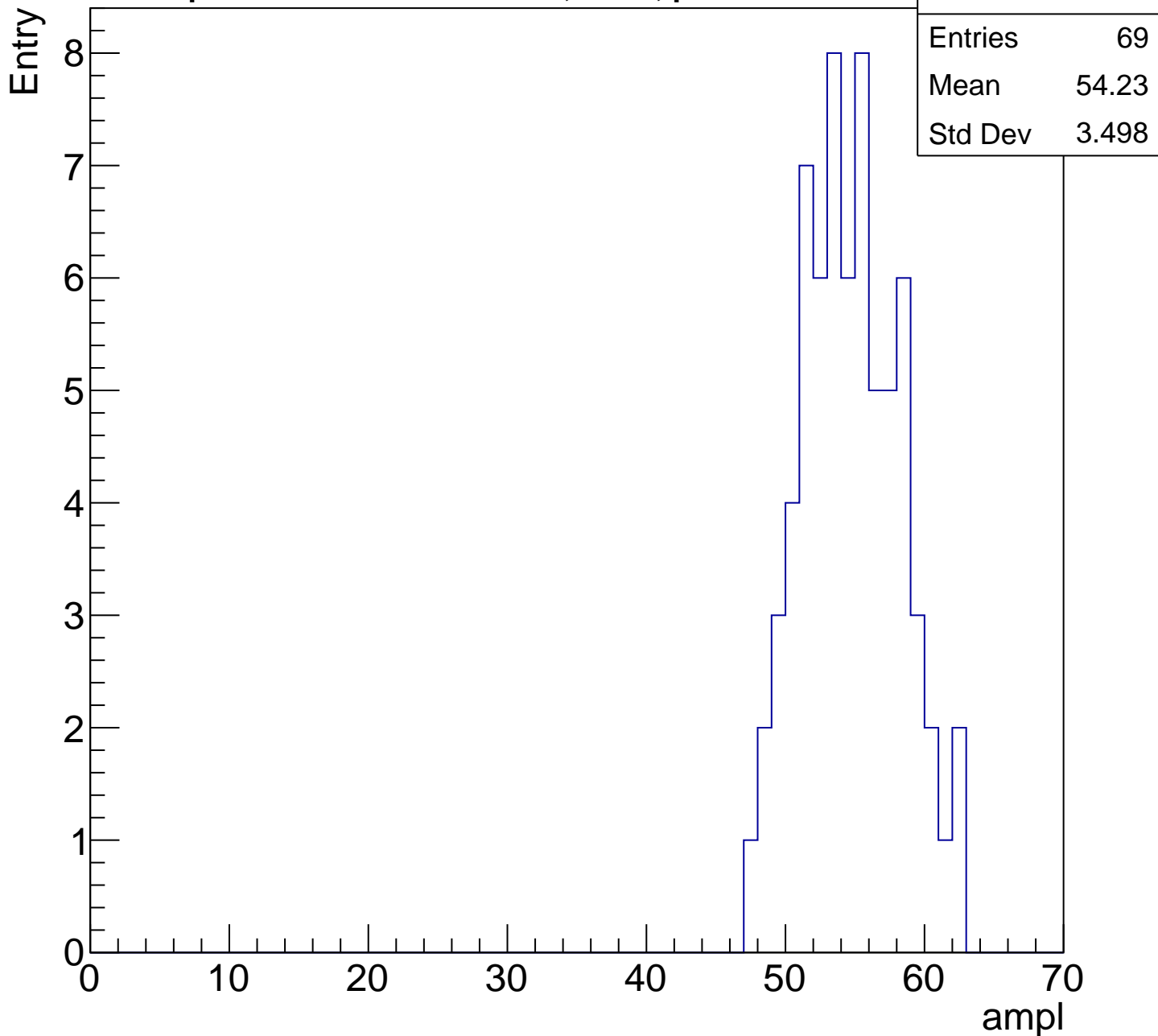
Entries	71
Mean	46.82
Std Dev	3.872

Entry



# B1L101S, U3-ch76, adc4

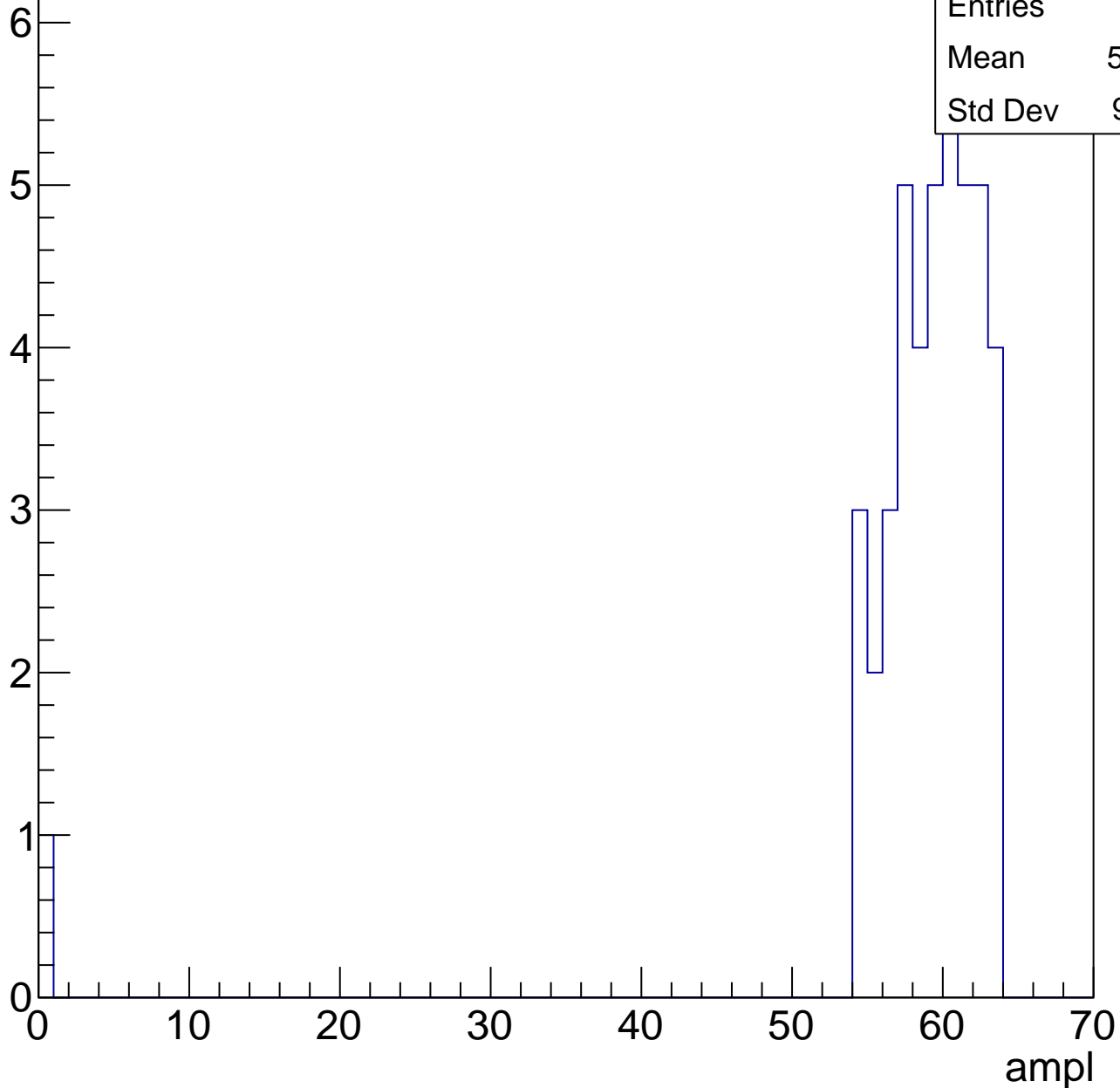
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

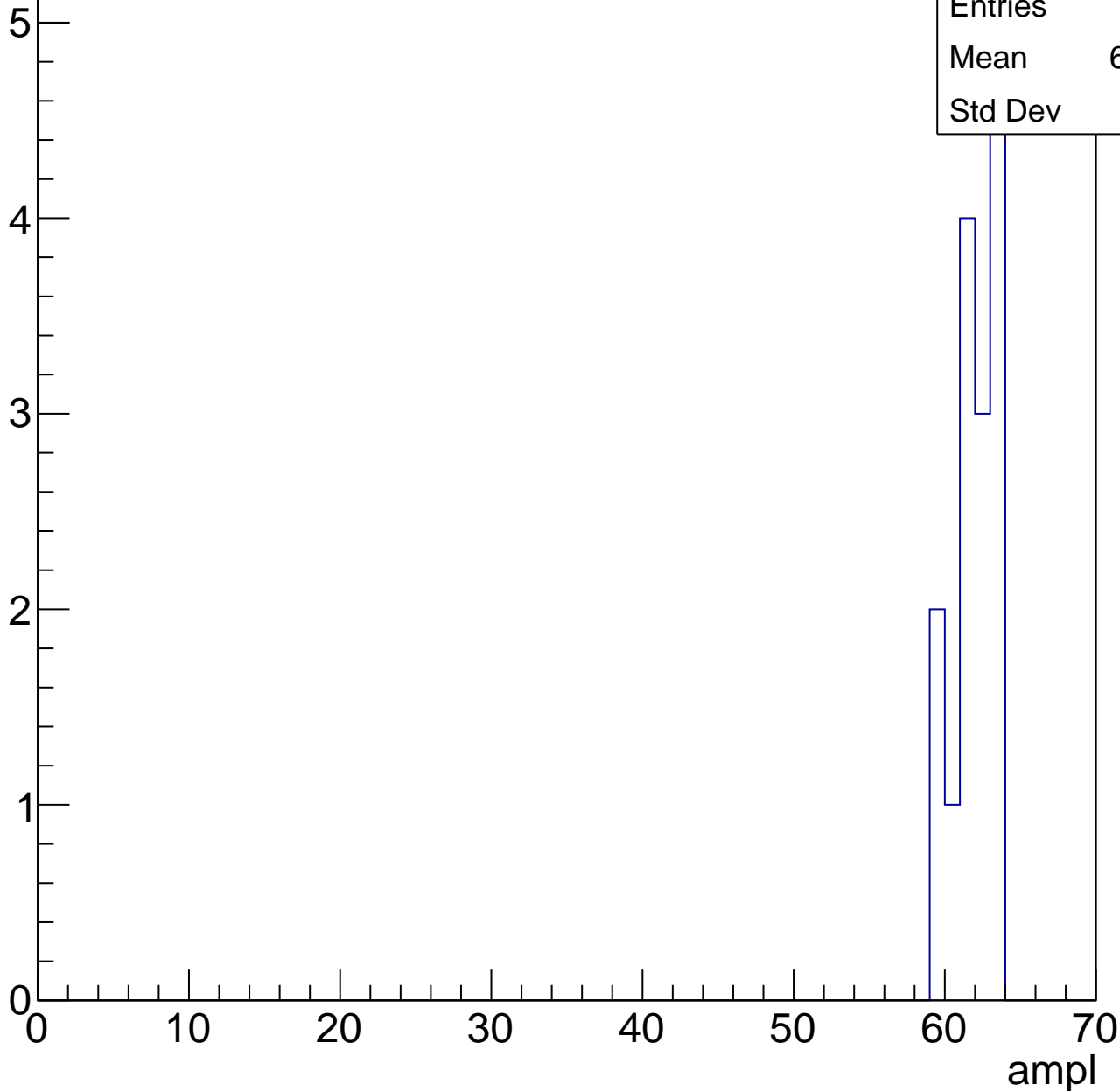


# B1L101S, U3-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	15
Mean	61.53
Std Dev	1.36

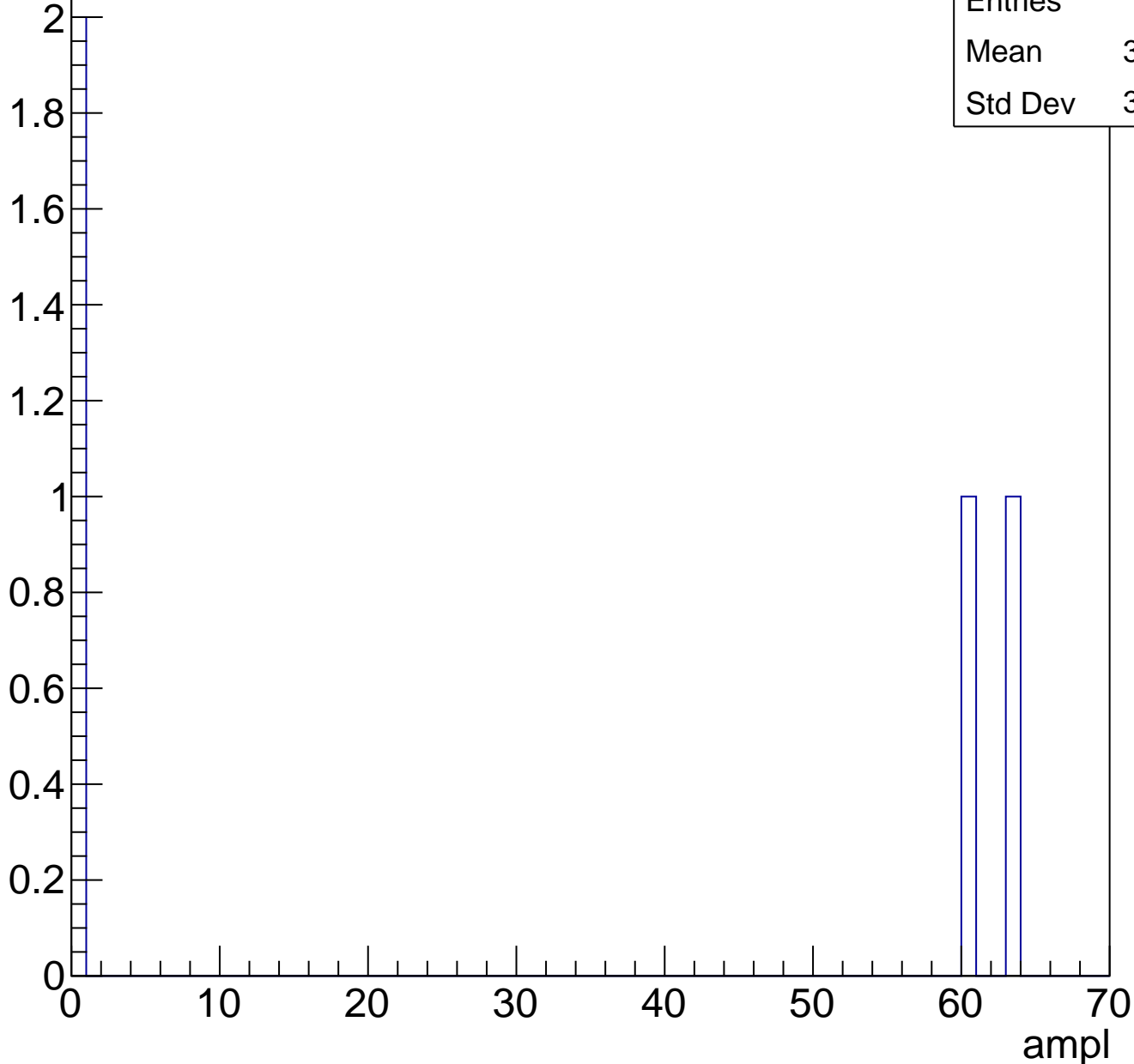




# B1L101S, U3-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	4
Mean	30.75
Std Dev	30.77

# B1L101S, U3-ch77, adc0

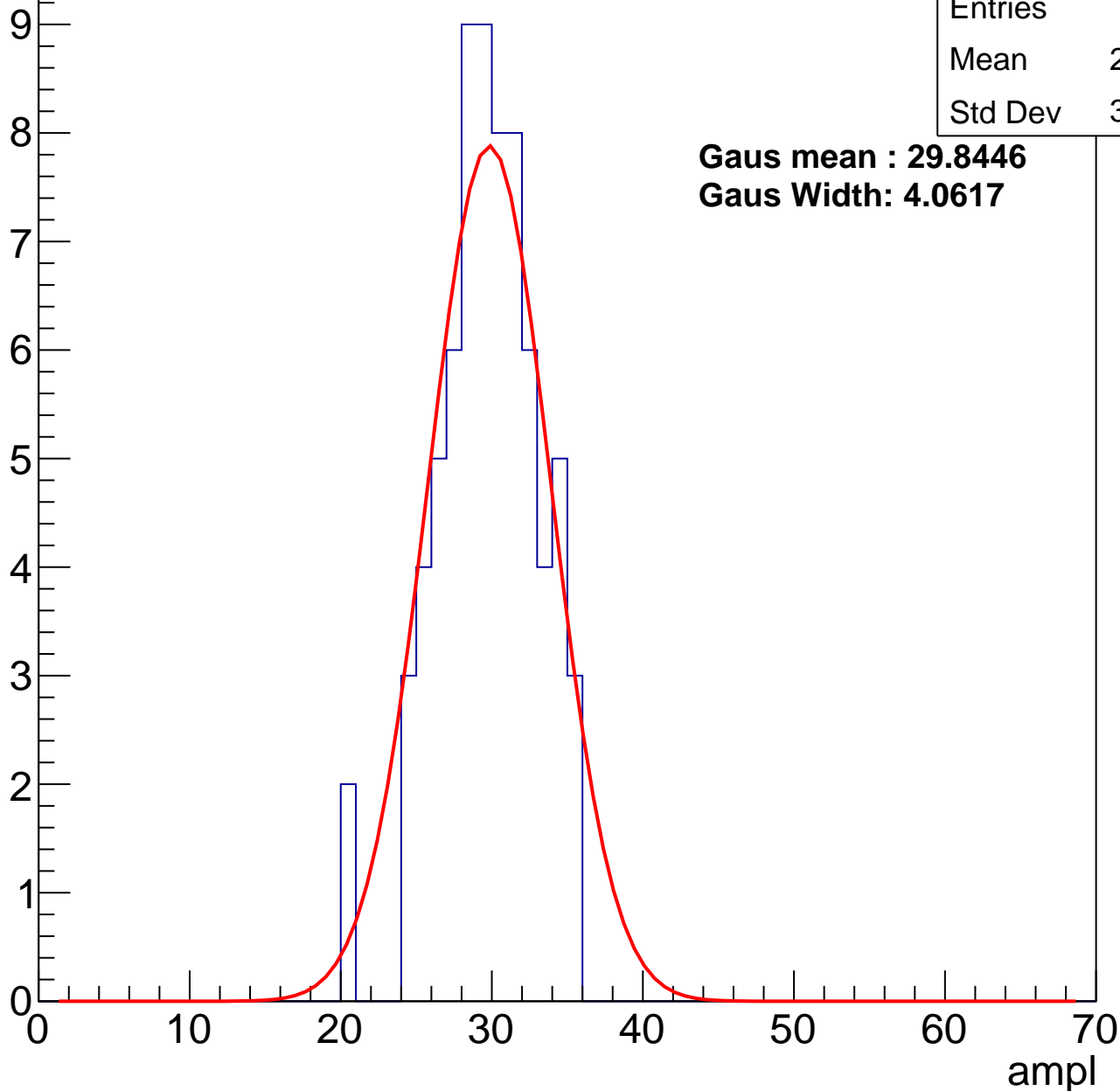
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	29.22
Std Dev	3.263

**Gaus mean : 29.8446**

**Gaus Width: 4.0617**



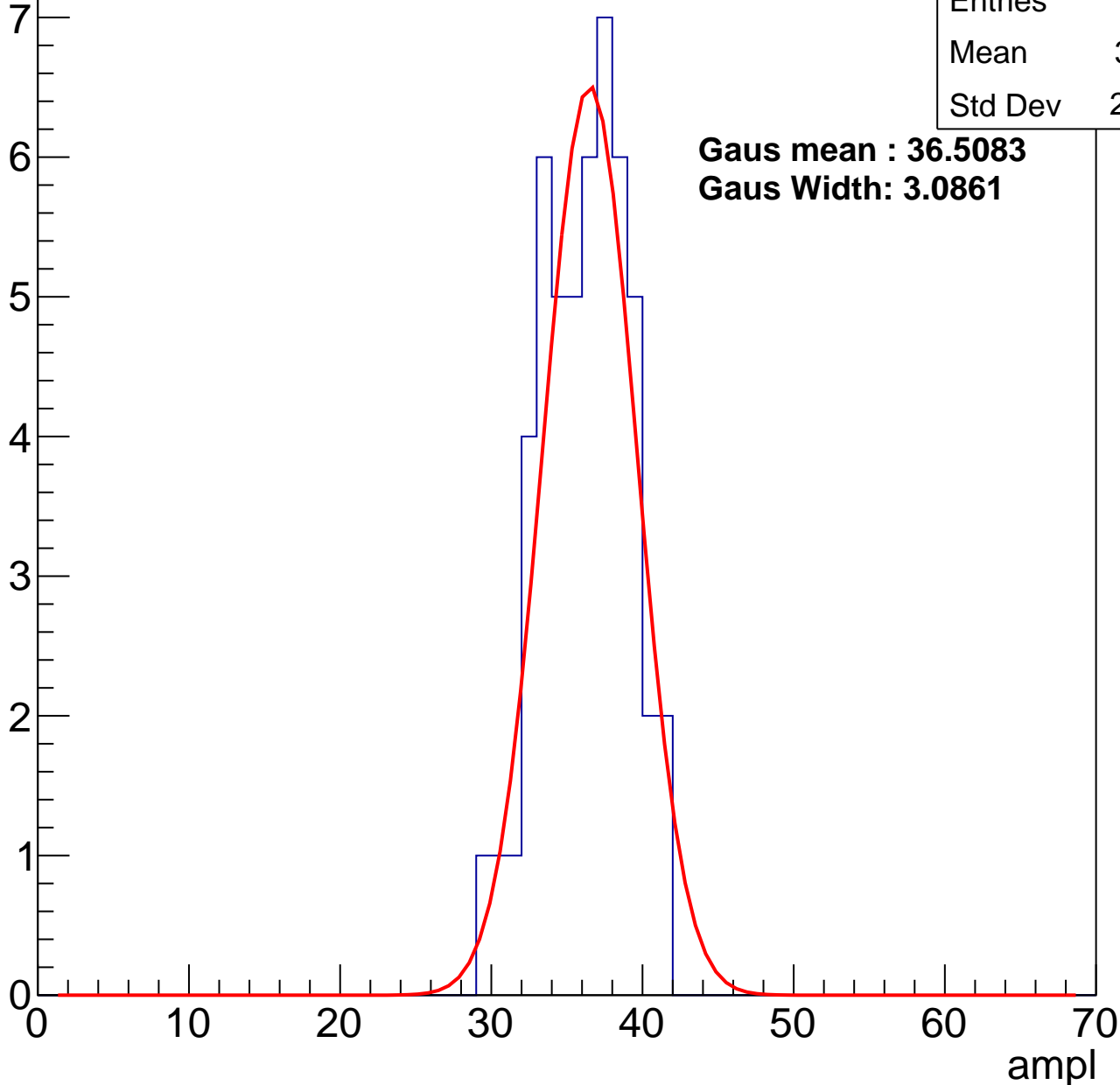
# B1L101S, U3-ch77, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	35.71
Std Dev	2.824

**Gaus mean : 36.5083**  
**Gaus Width: 3.0861**



# B1L101S, U3-ch77, adc2

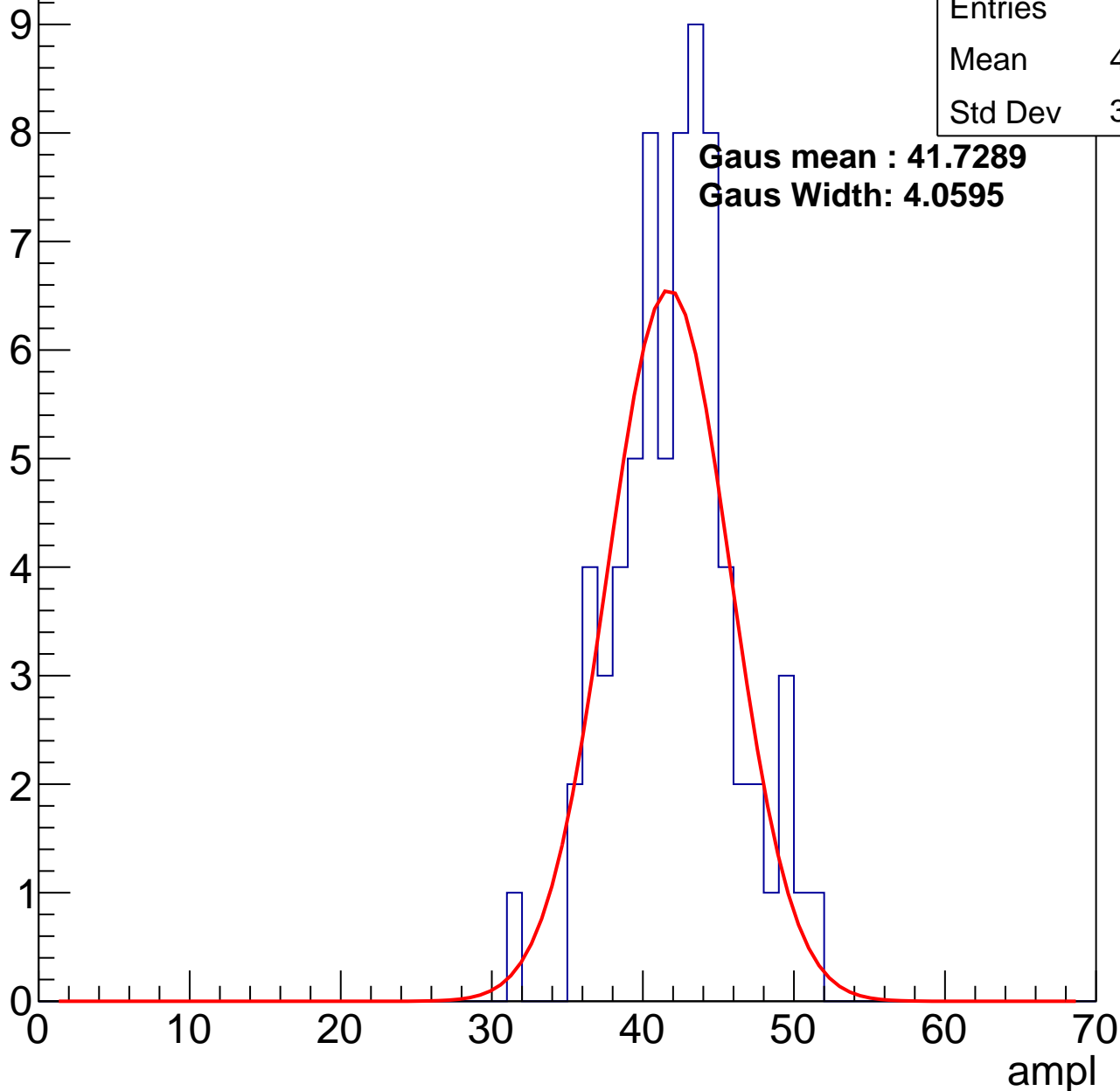
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	41.76
Std Dev	3.876

**Gaus mean : 41.7289**

**Gaus Width: 4.0595**

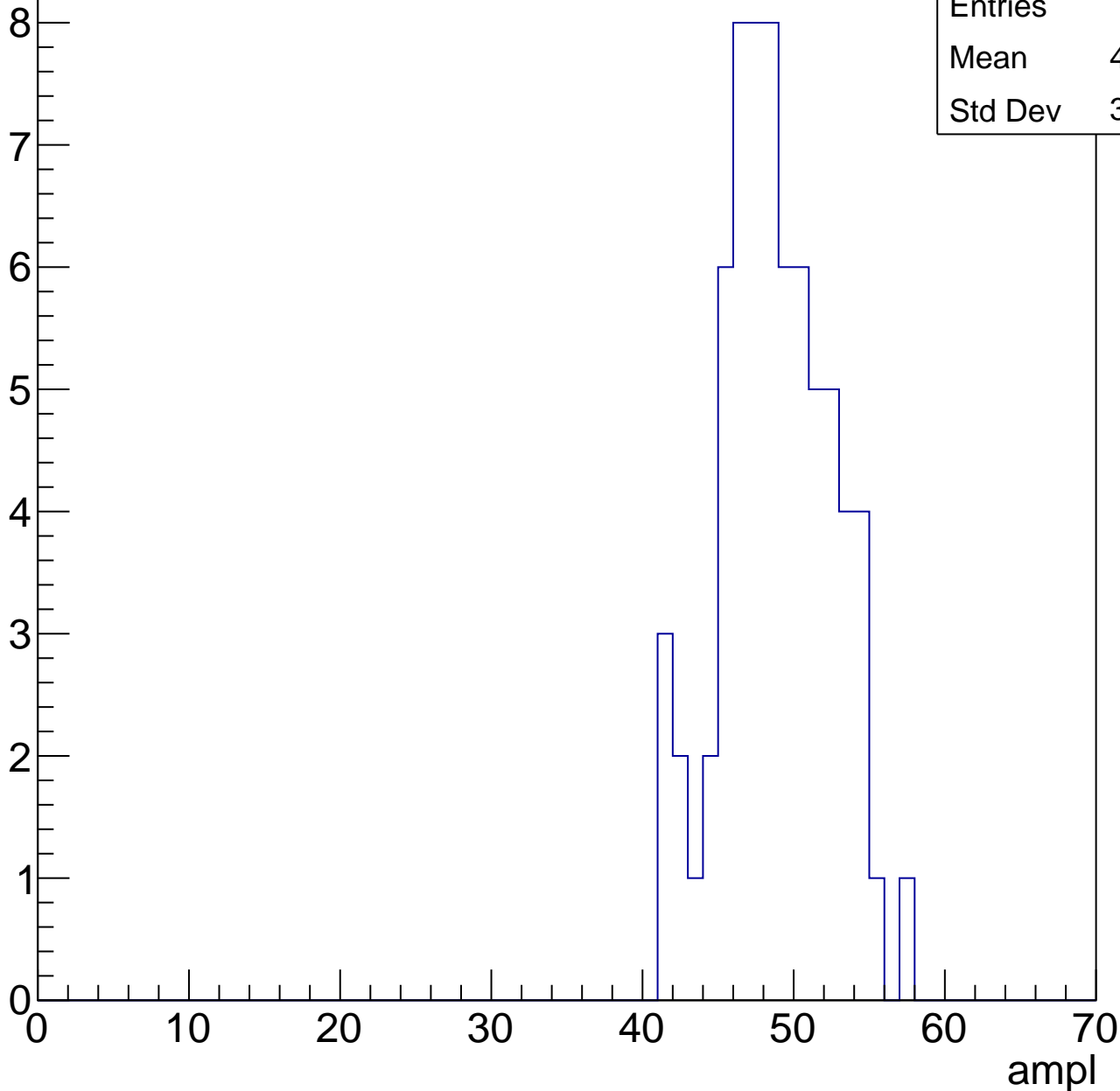


# B1L101S, U3-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

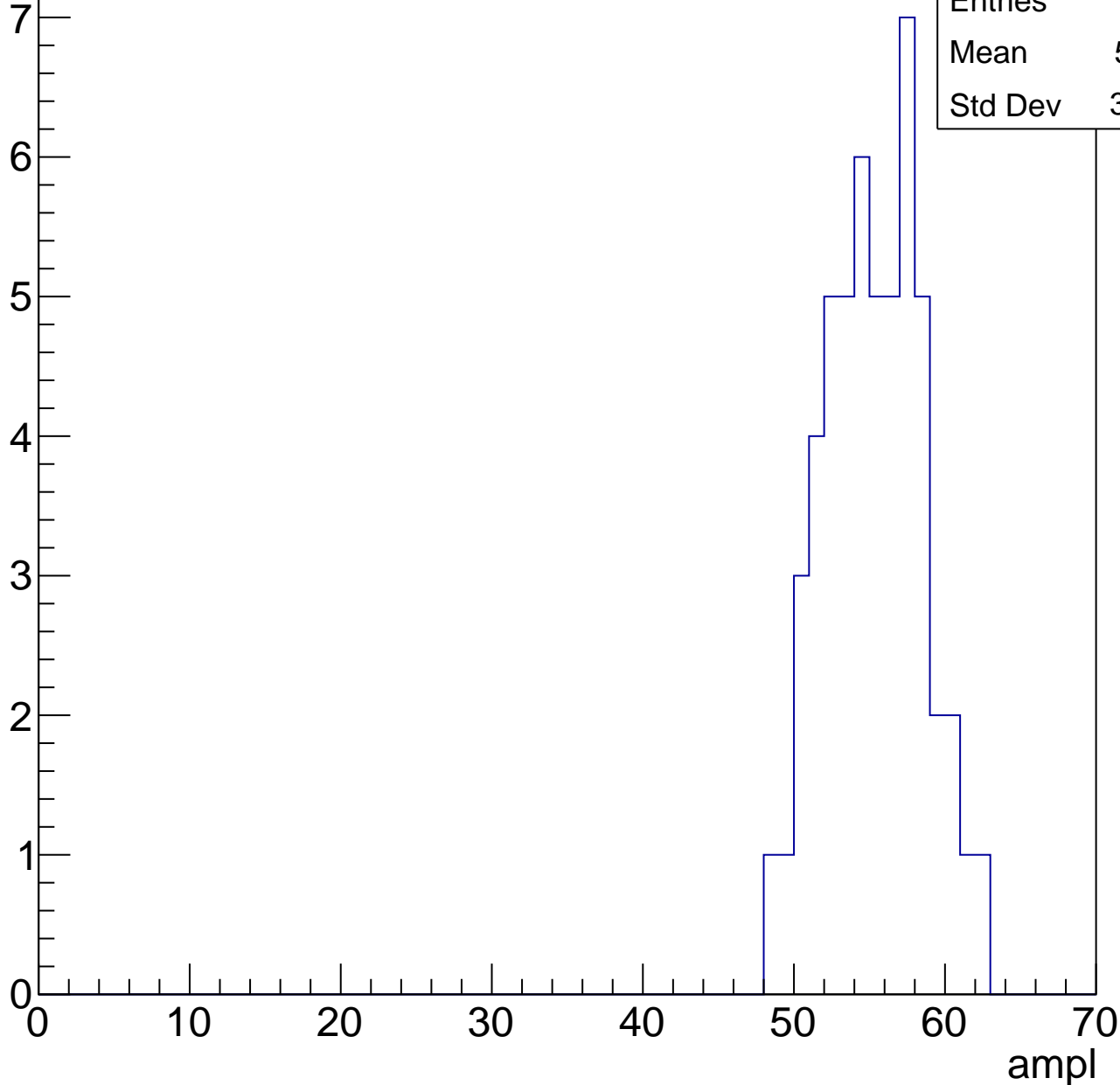
Entries	70
Mean	48.36
Std Dev	3.566



# B1L101S, U3-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

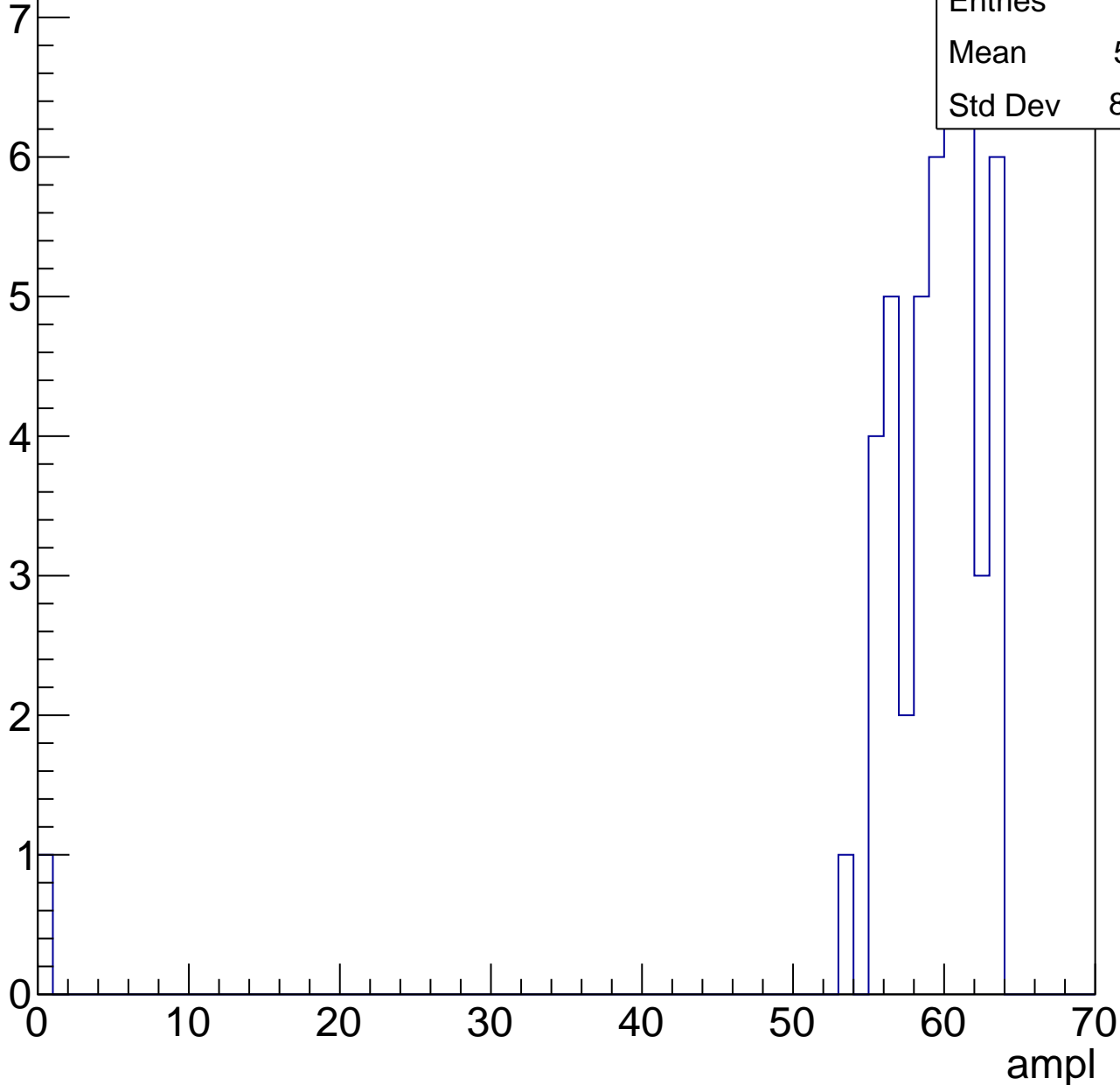


# B1L101S, U3-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	57.91
Std Dev	8.922

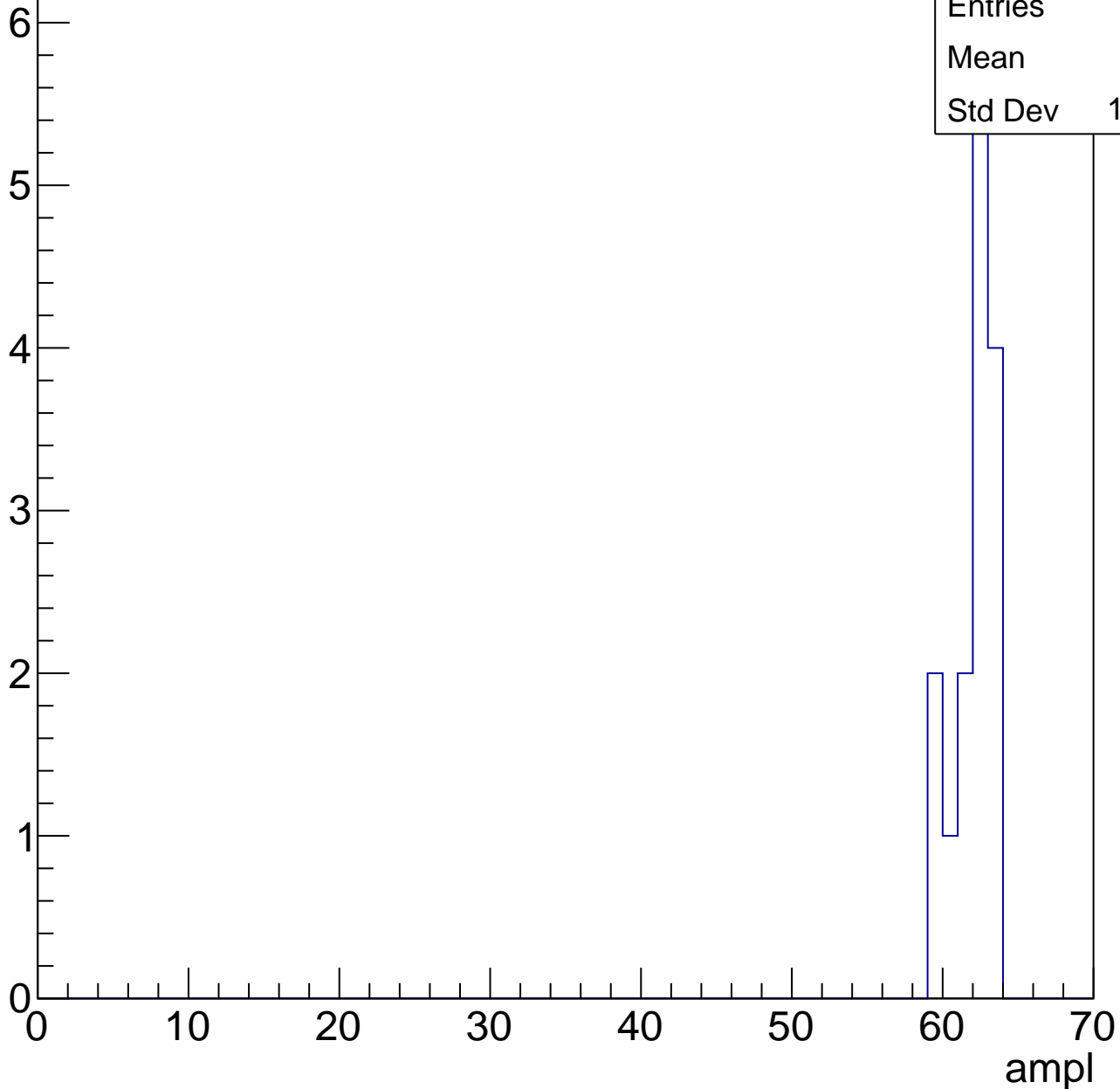


# B1L101S, U3-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	15
Mean	61.6
Std Dev	1.306





# B1L101S, U3-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U3-ch78, adc0

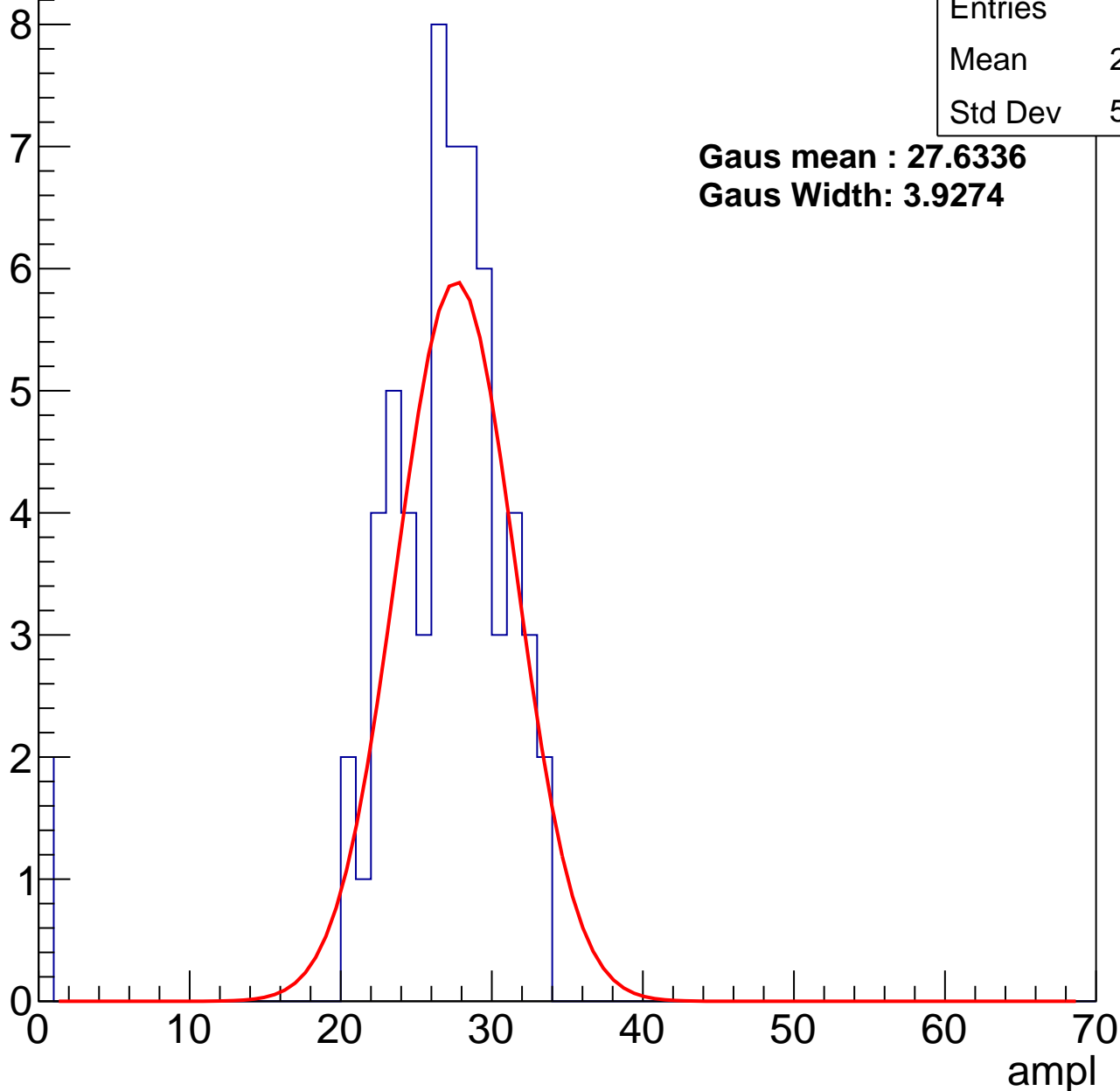
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	25.87
Std Dev	5.753

**Gaus mean : 27.6336**

**Gaus Width: 3.9274**



# B1L101S, U3-ch78, adc1

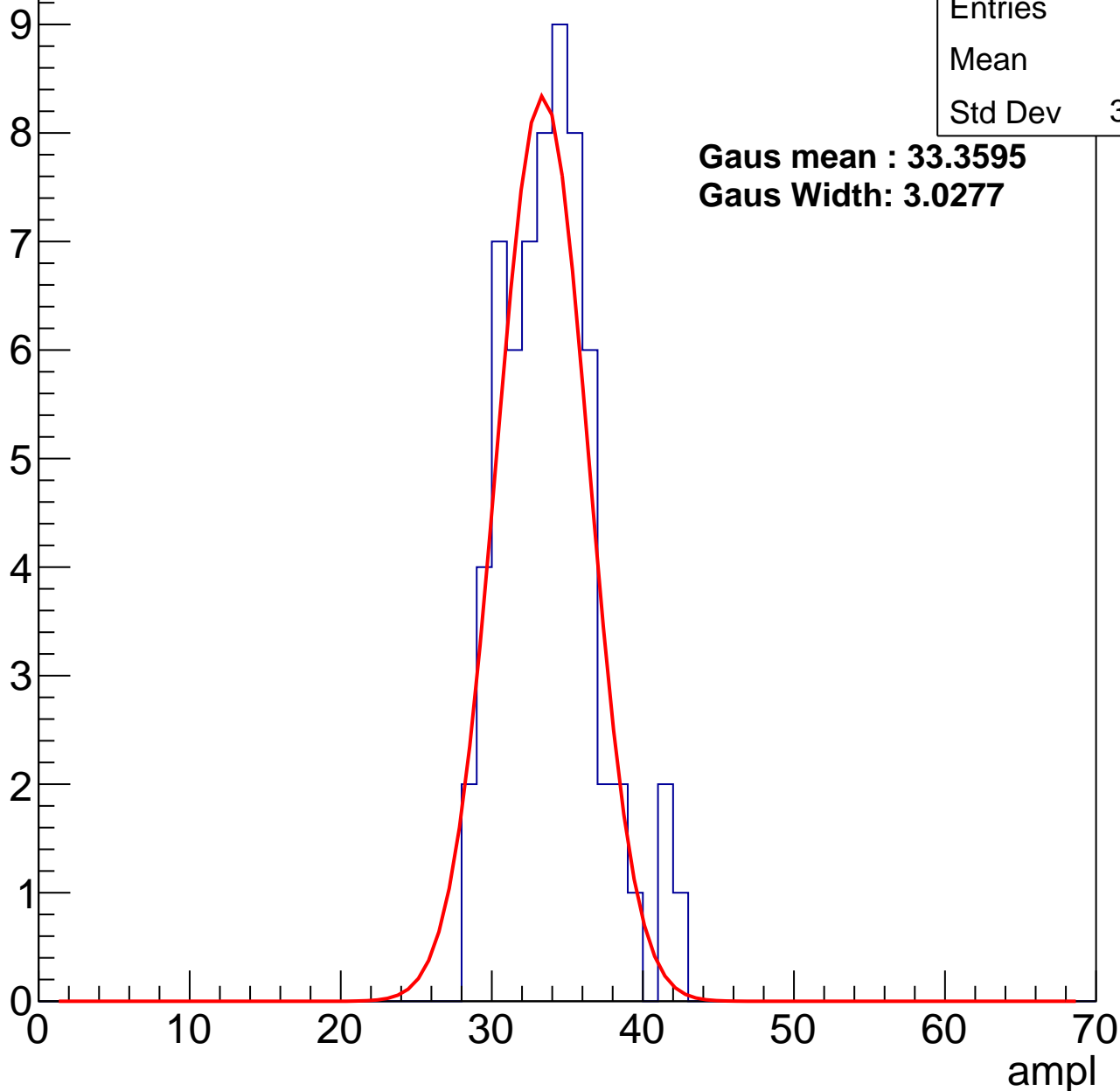
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	33.4
Std Dev	3.087

**Gaus mean : 33.3595**

**Gaus Width: 3.0277**



# B1L101S, U3-ch78, adc2

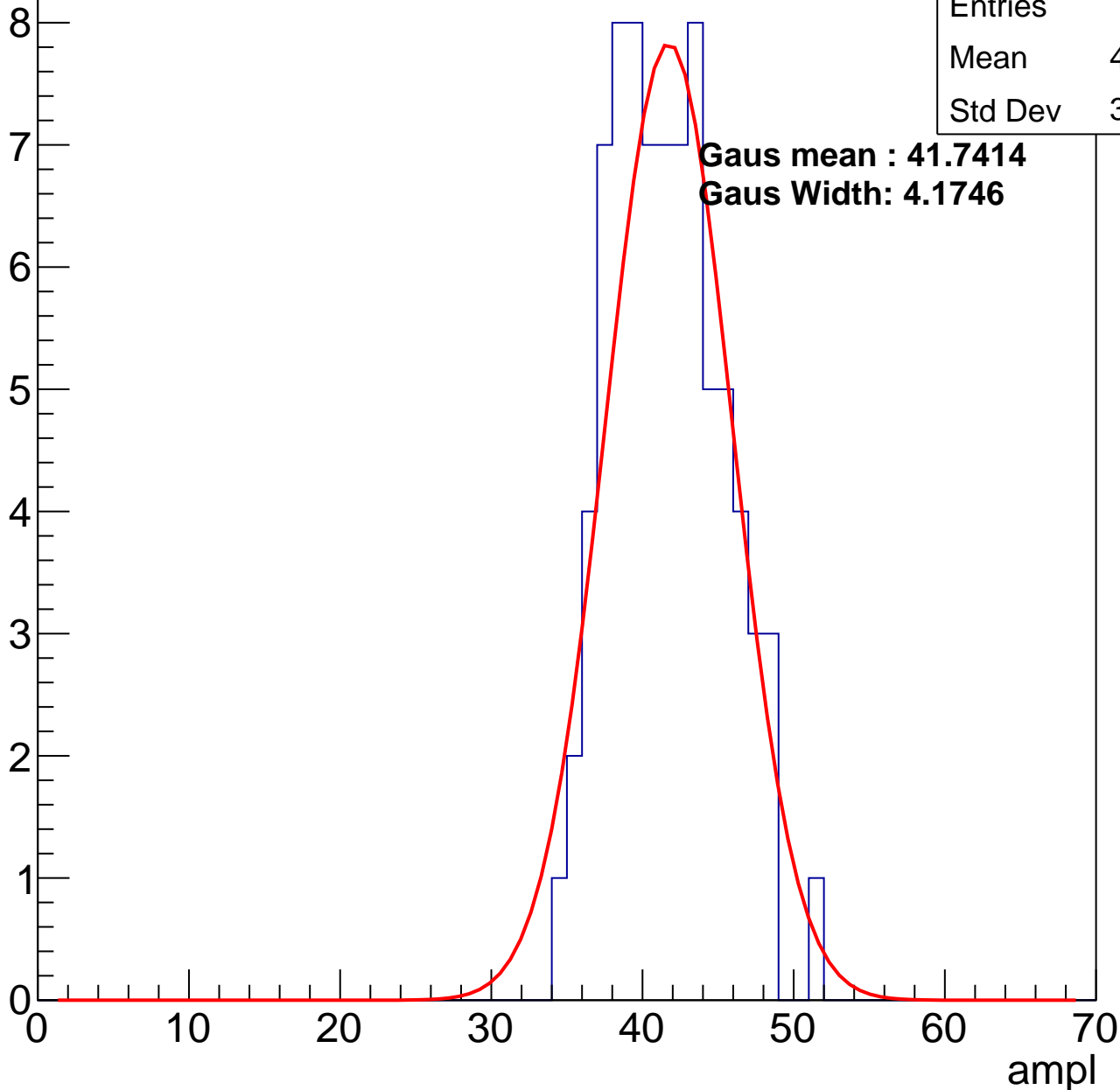
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	41.16
Std Dev	3.642

**Gaus mean : 41.7414**

**Gaus Width: 4.1746**

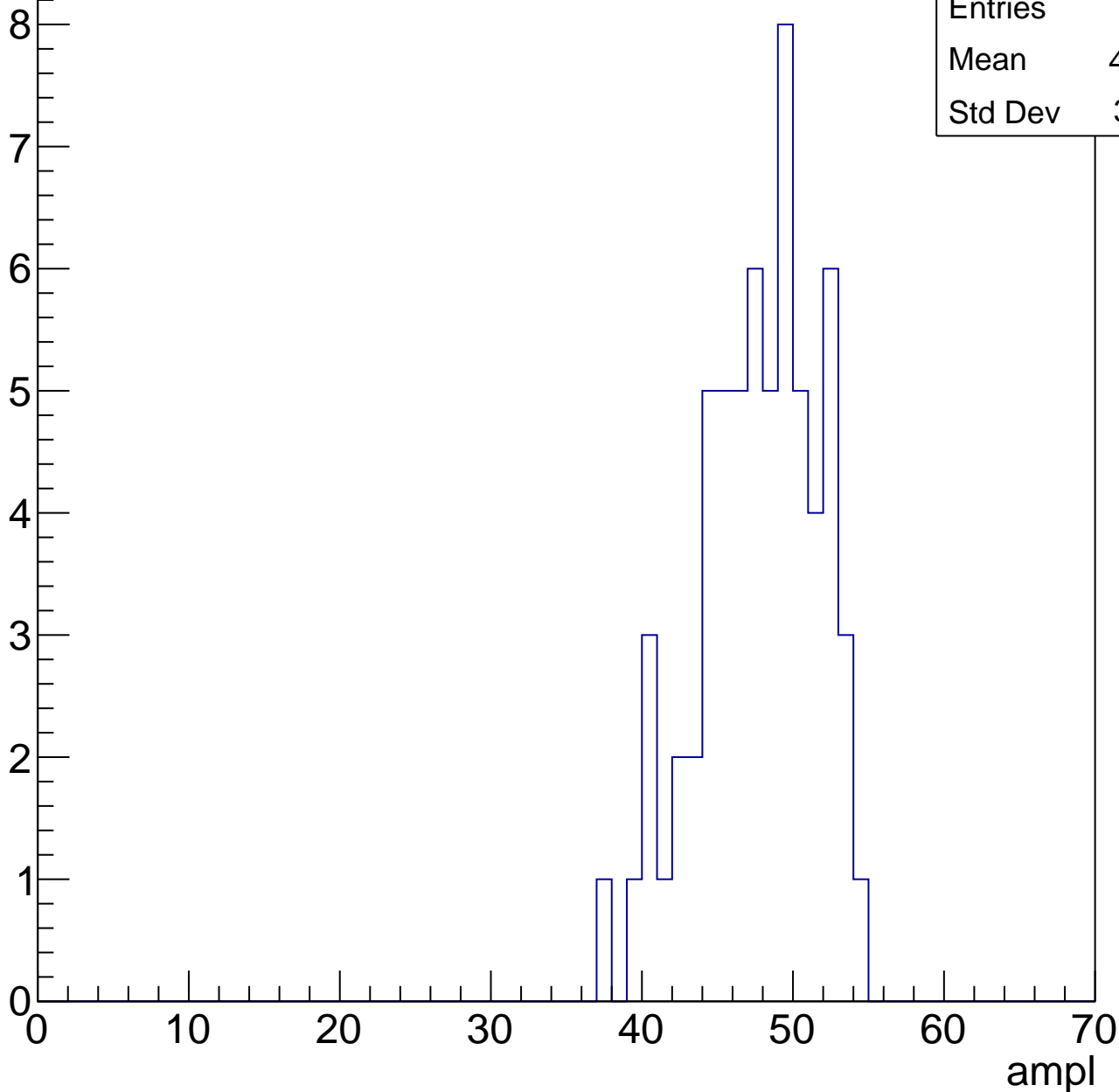


# B1L101S, U3-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

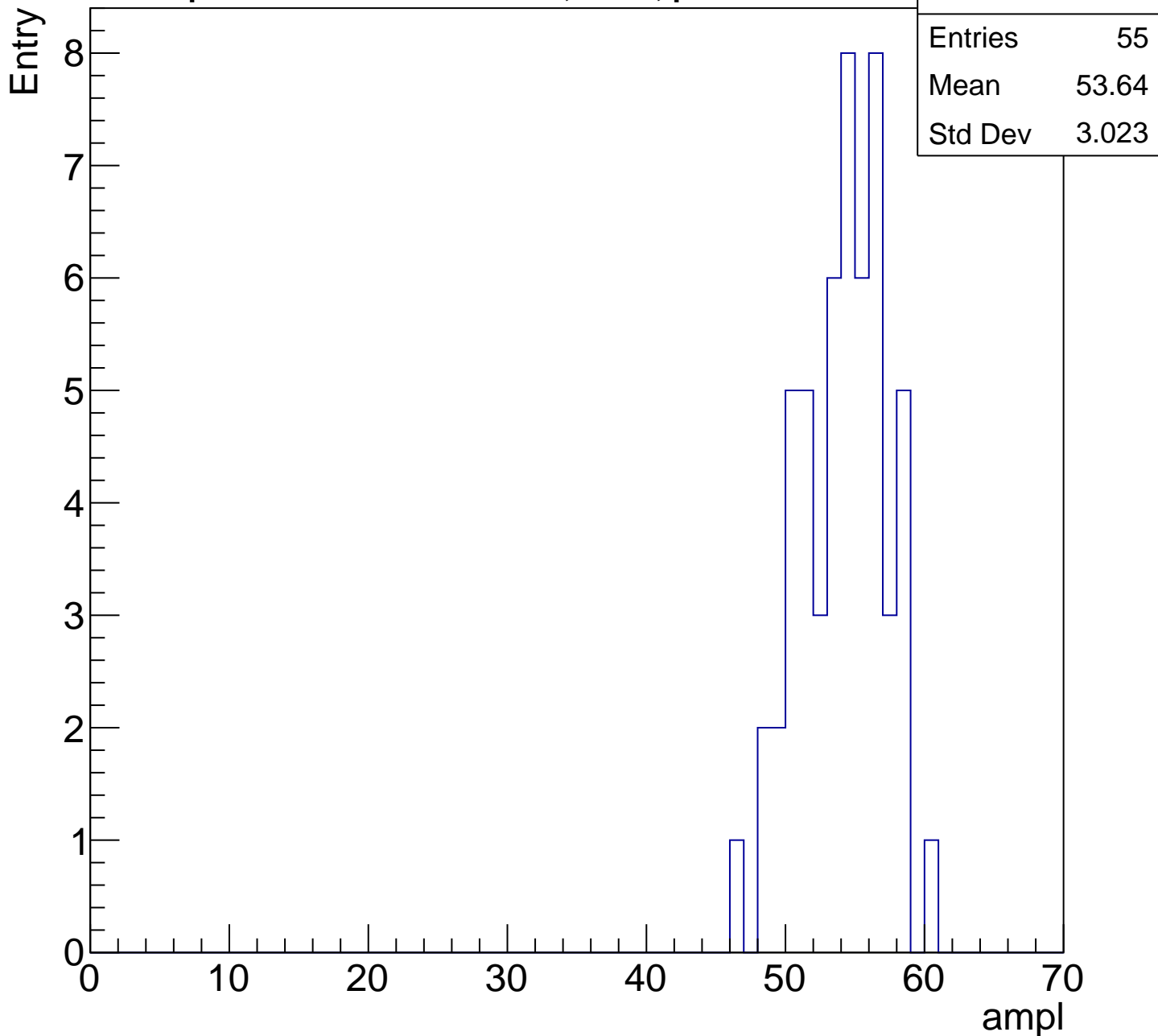
Entry

Entries	63
Mean	47.22
Std Dev	3.881



# B1L101S, U3-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

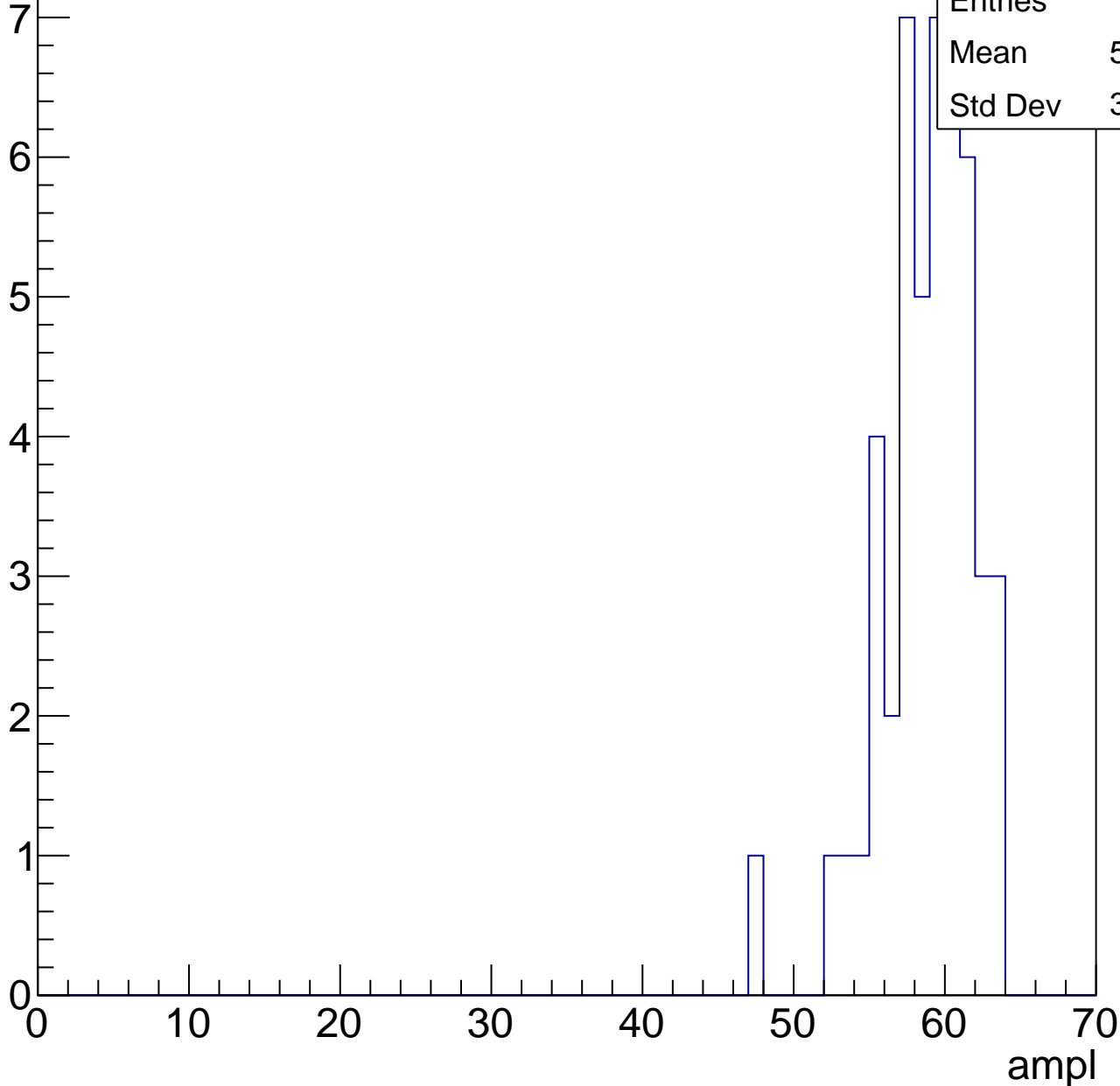


# B1L101S, U3-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	58.35
Std Dev	3.079

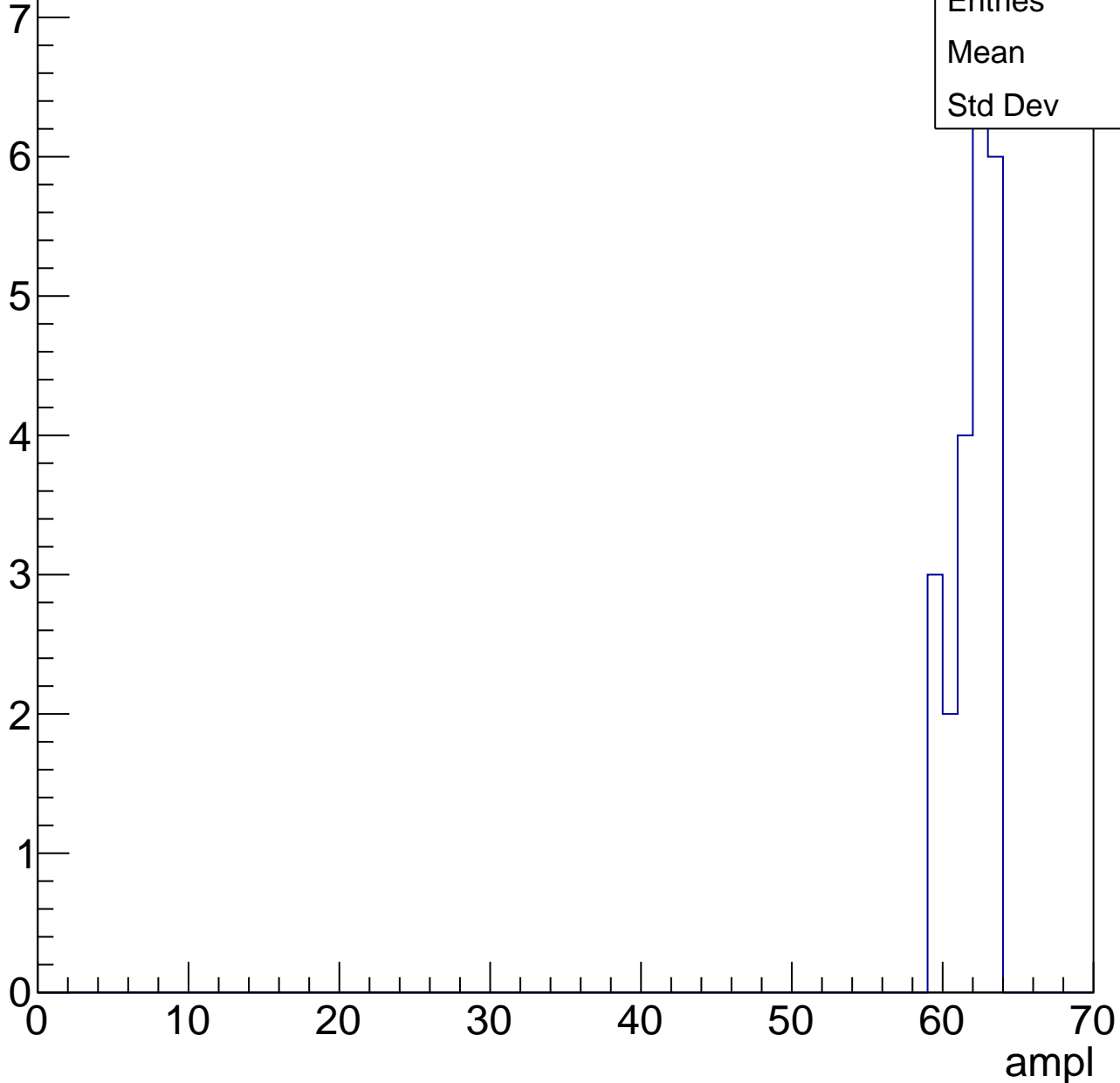


# B1L101S, U3-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	22
Mean	61.5
Std Dev	1.34

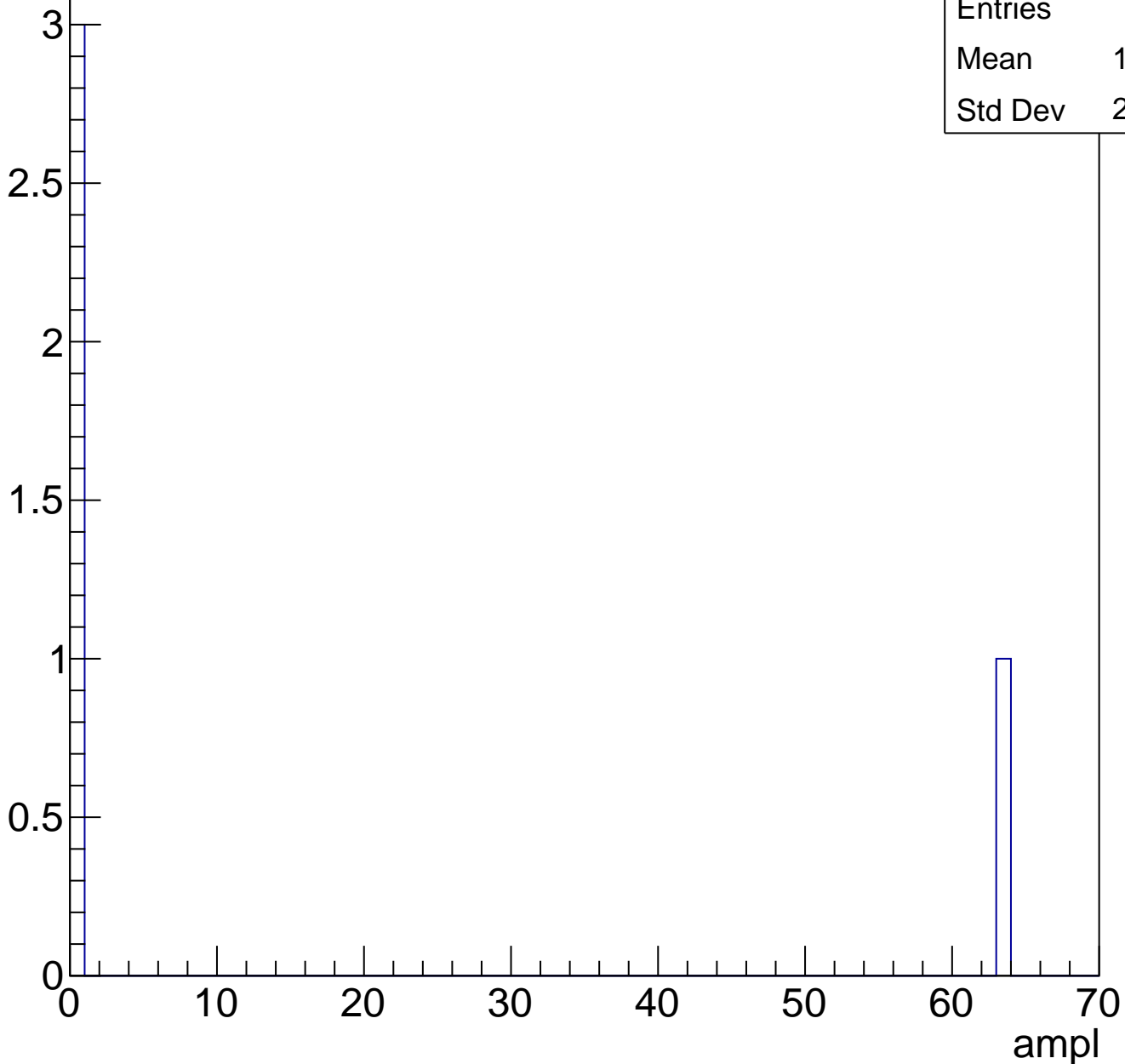




# B1L101S, U3-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch79, adc0

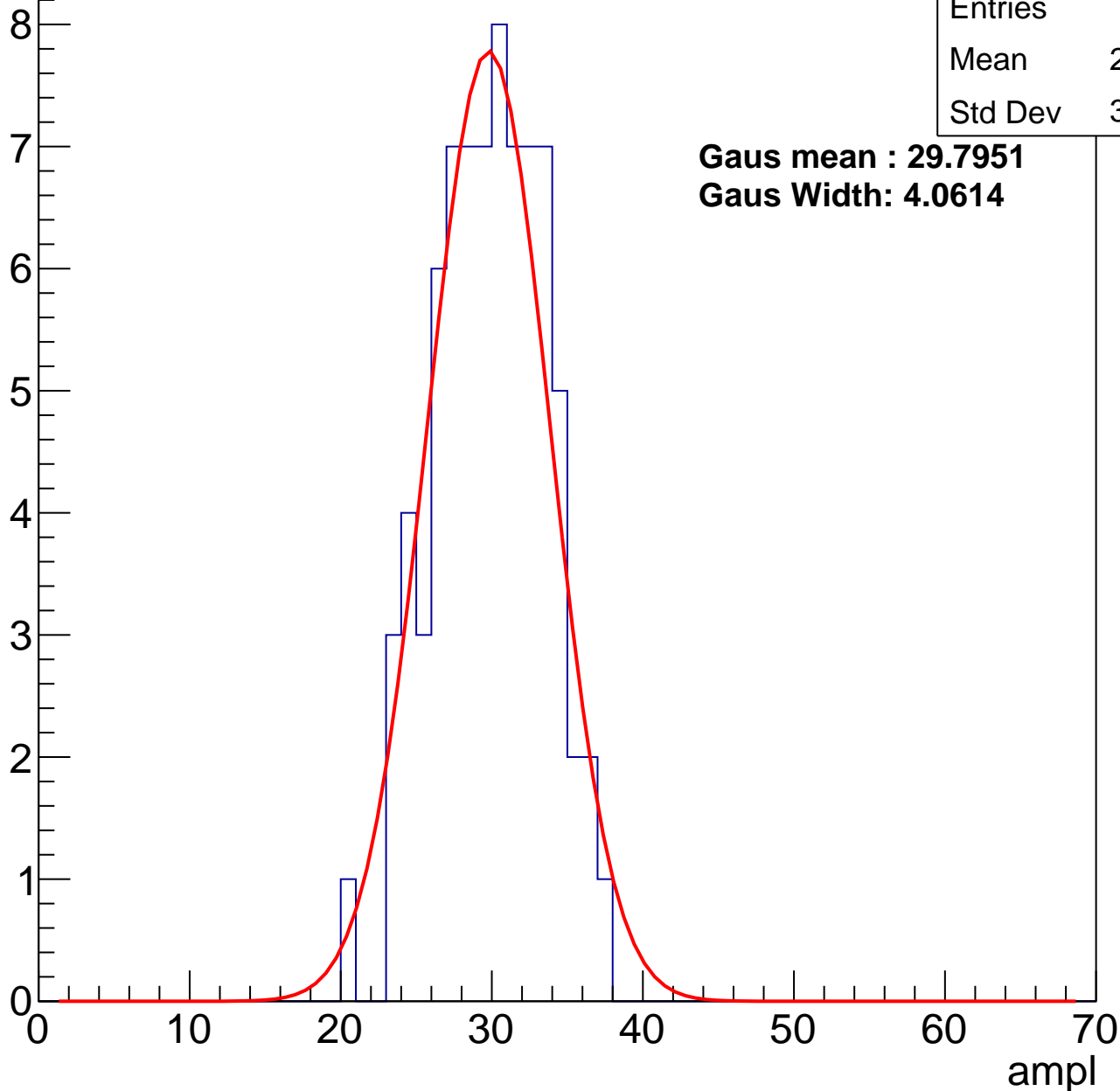
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	29.42
Std Dev	3.572

**Gaus mean : 29.7951**

**Gaus Width: 4.0614**



# B1L101S, U3-ch79, adc1

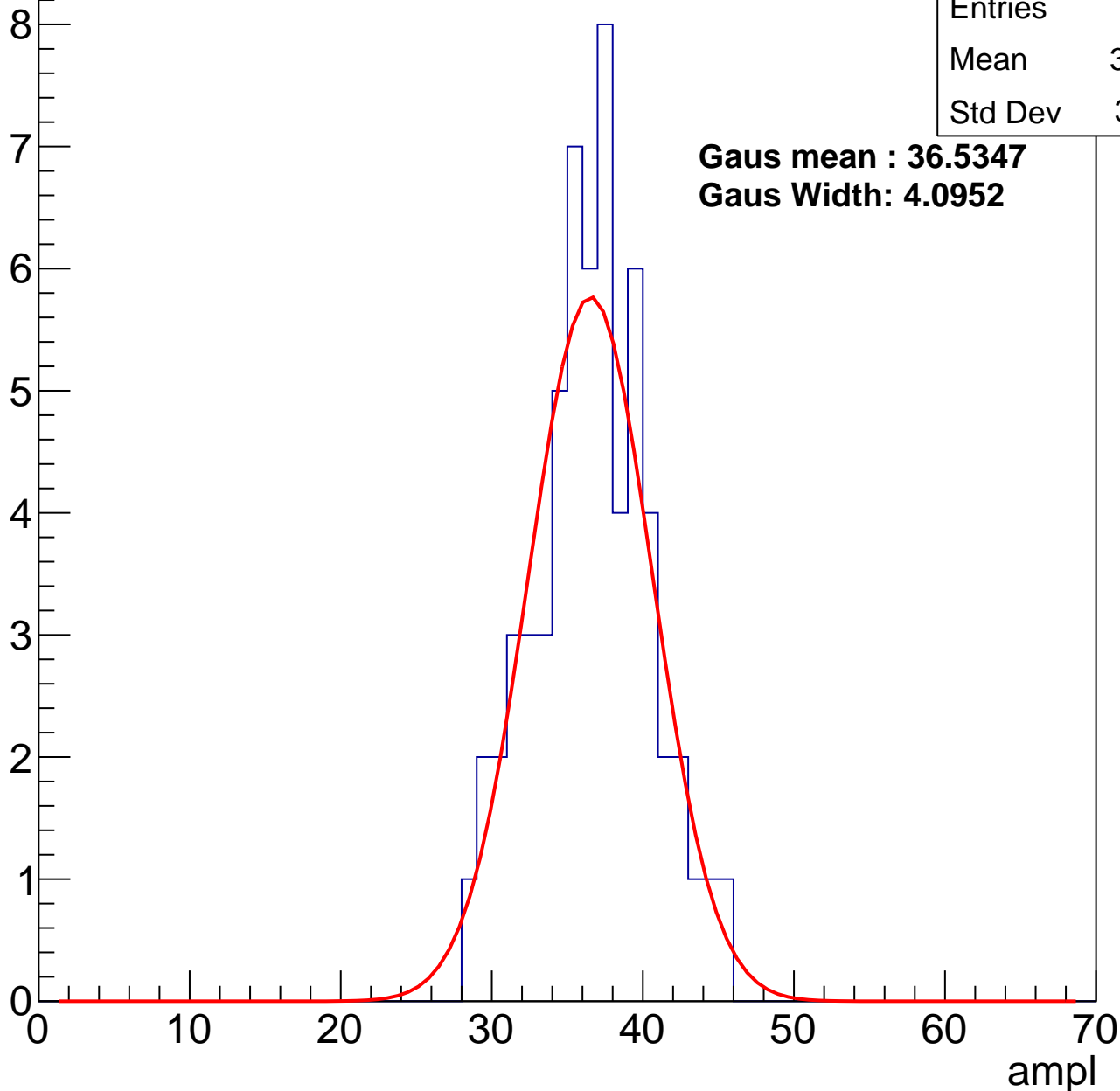
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	36.15
Std Dev	3.771

**Gaus mean : 36.5347**

**Gaus Width: 4.0952**



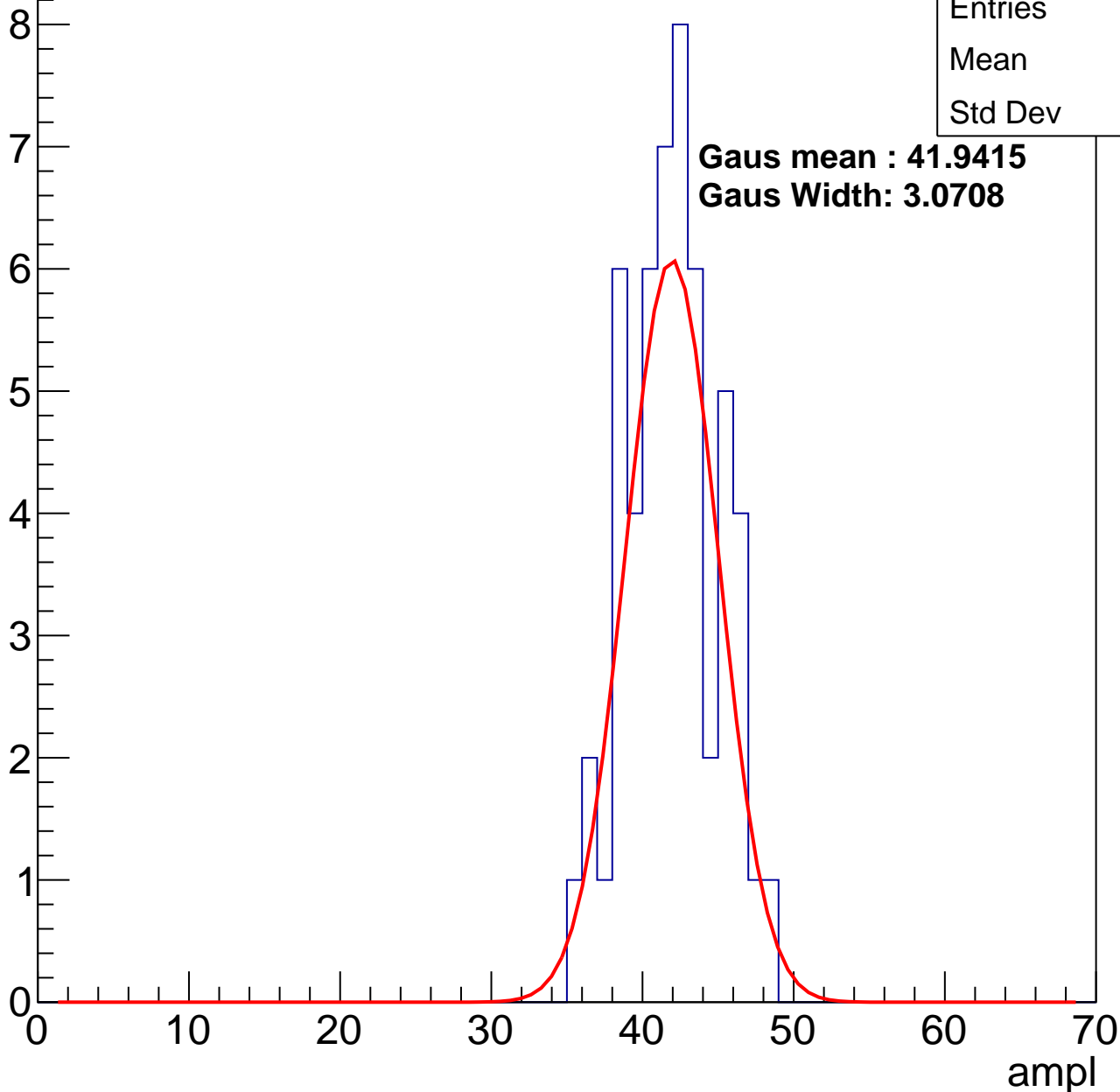
# B1L101S, U3-ch79, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	41.5
Std Dev	2.98

**Gaus mean : 41.9415**  
**Gaus Width: 3.0708**

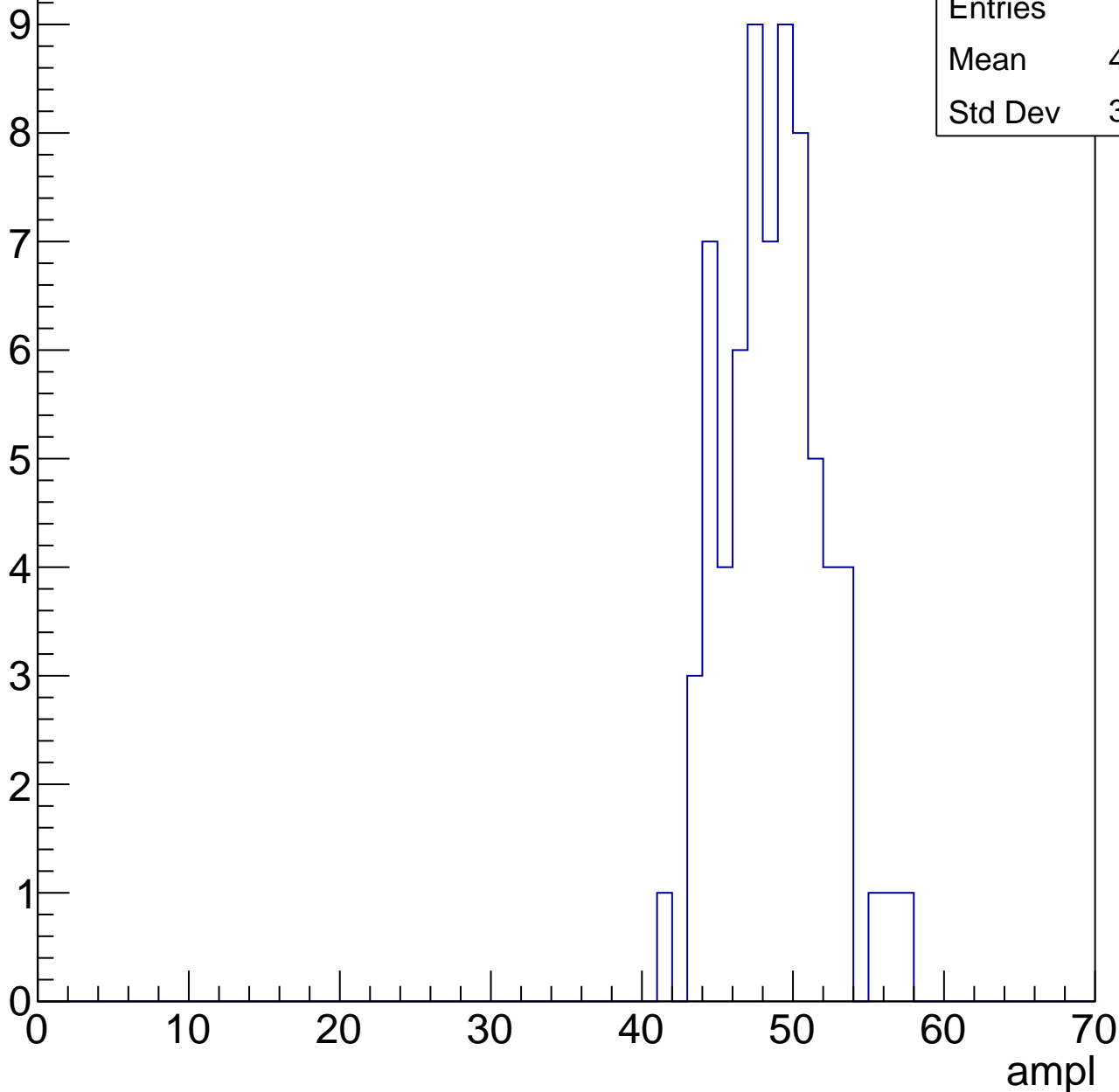


# B1L101S, U3-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

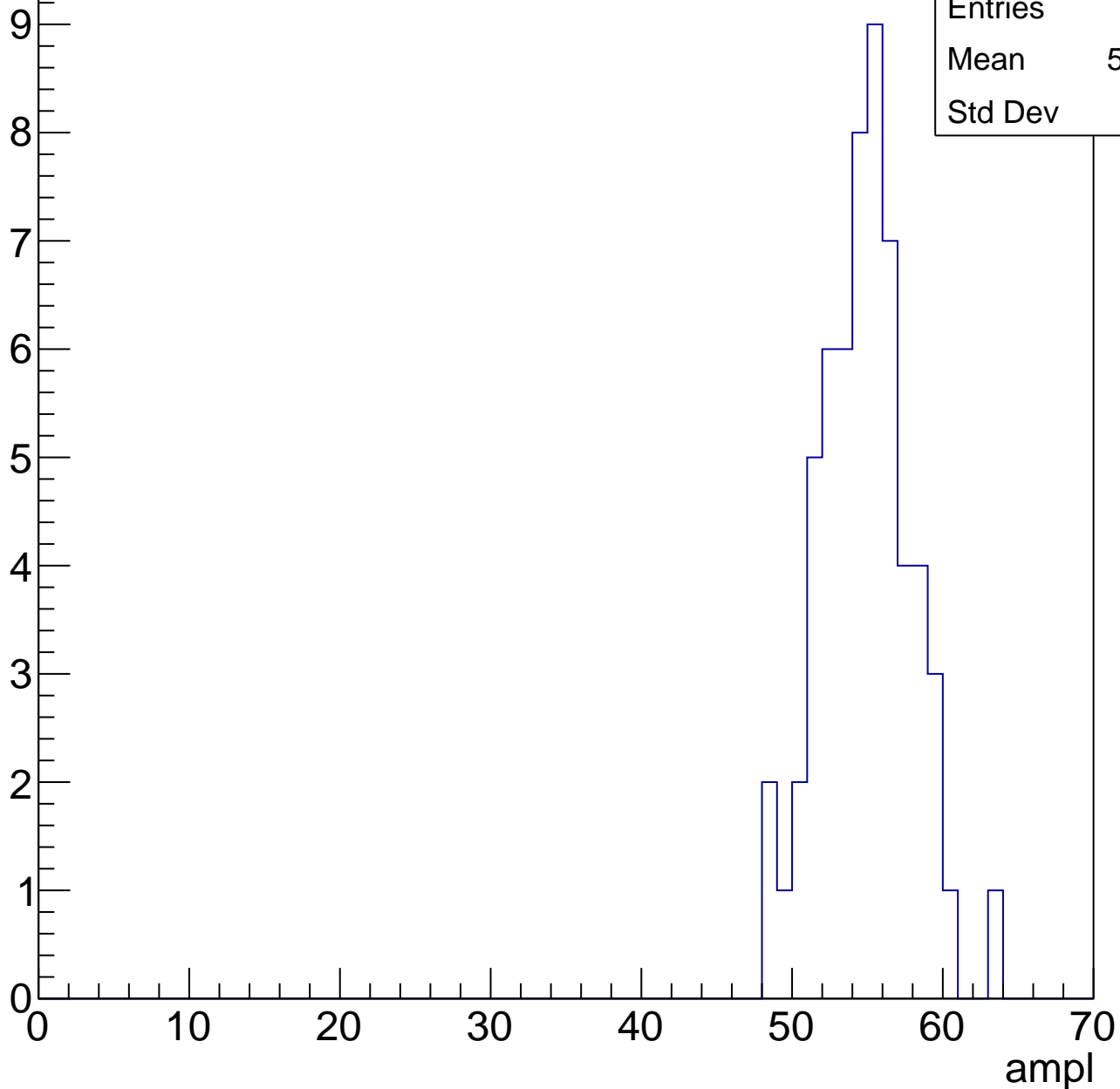
Entries	70
Mean	48.24
Std Dev	3.262



# B1L101S, U3-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

10

Entries 57

Mean 58.93

Std Dev 8.197

8

6

4

2

0

0

10

20

30

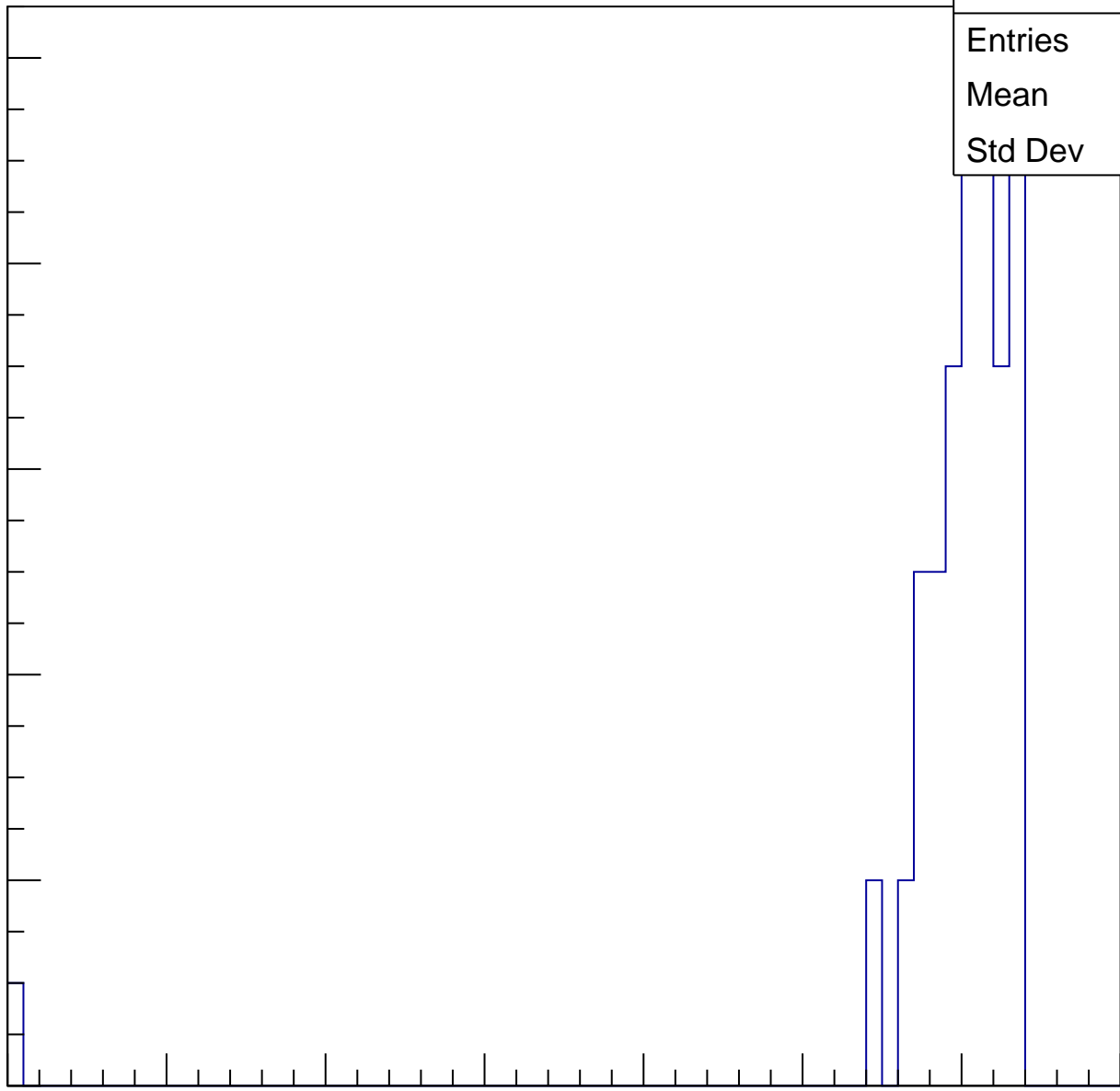
40

50

60

70

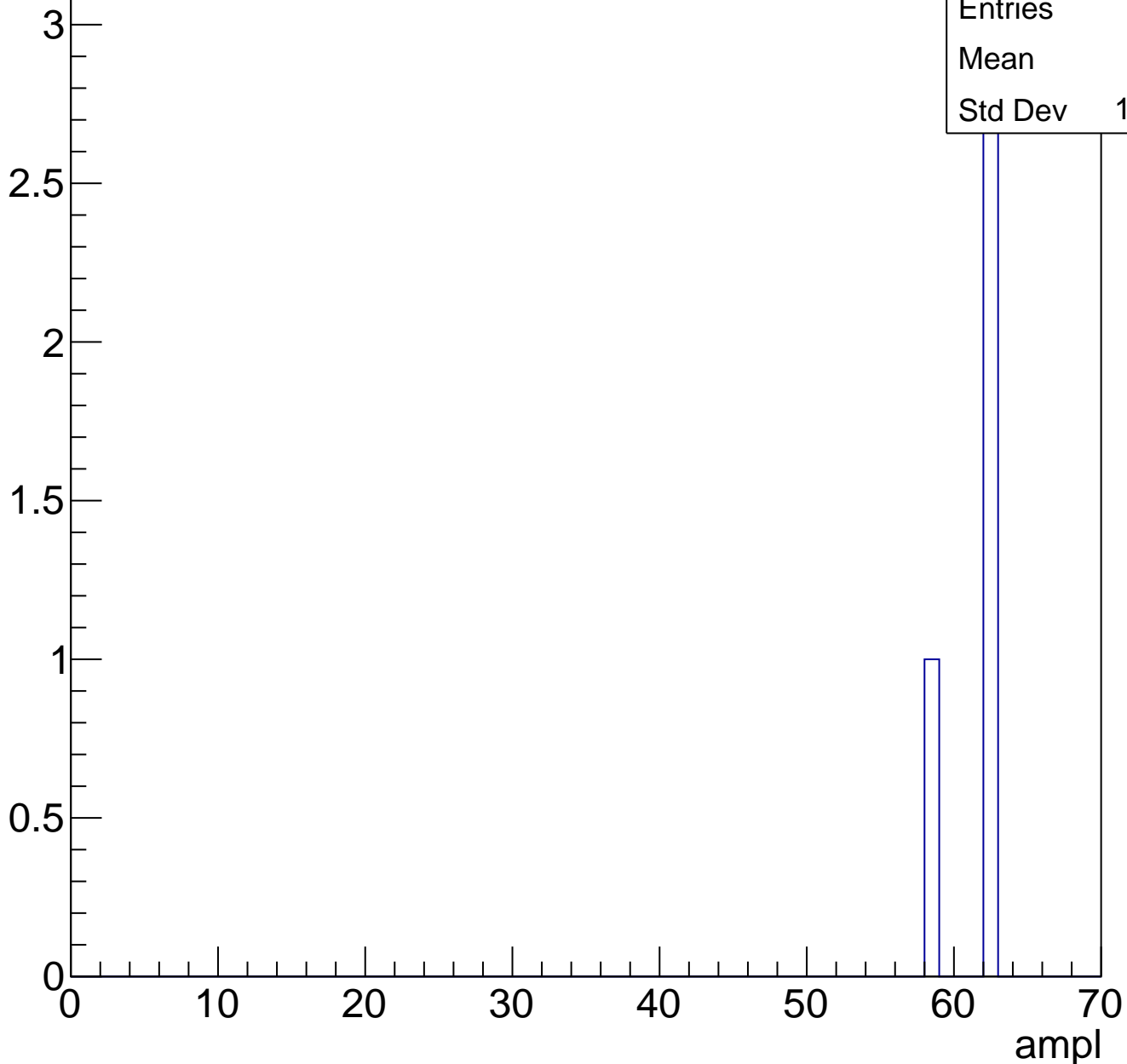
ampl



# B1L101S, U3-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

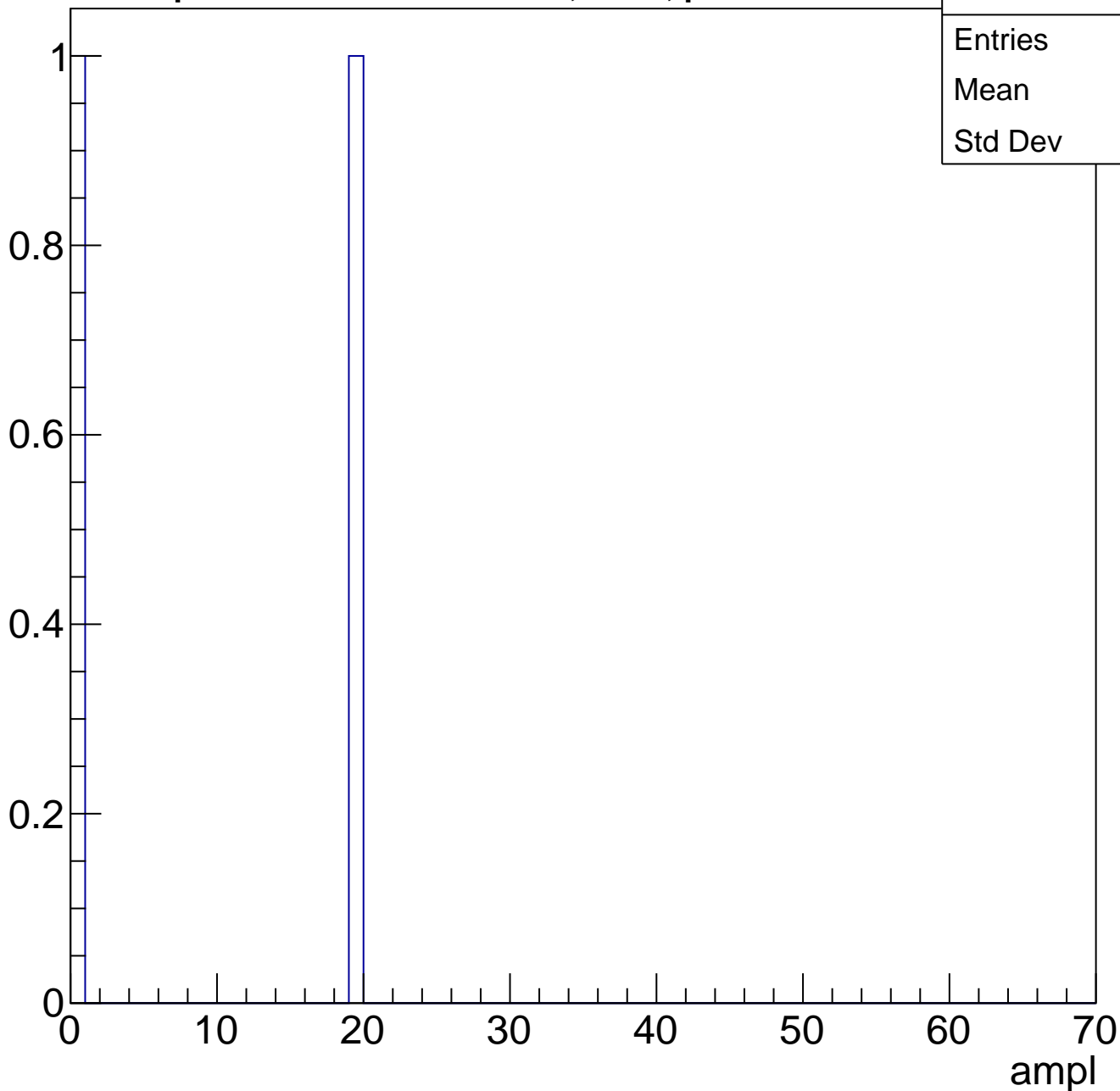




# B1L101S, U3-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch80, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	85
Mean	27.11
Std Dev	4.88

**Gaus mean : 28.3094**

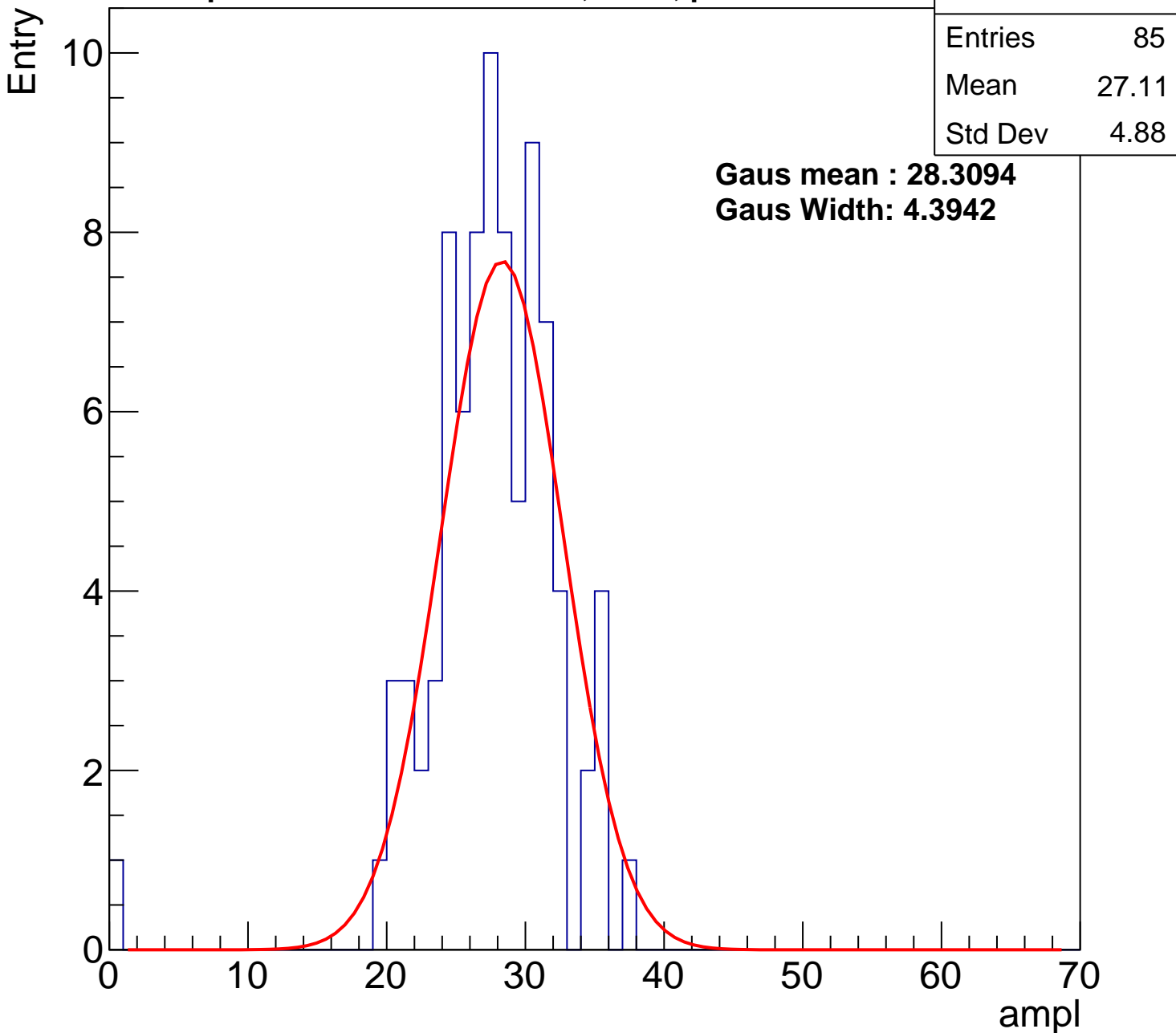
**Gaus Width: 4.3942**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U3-ch80, adc1

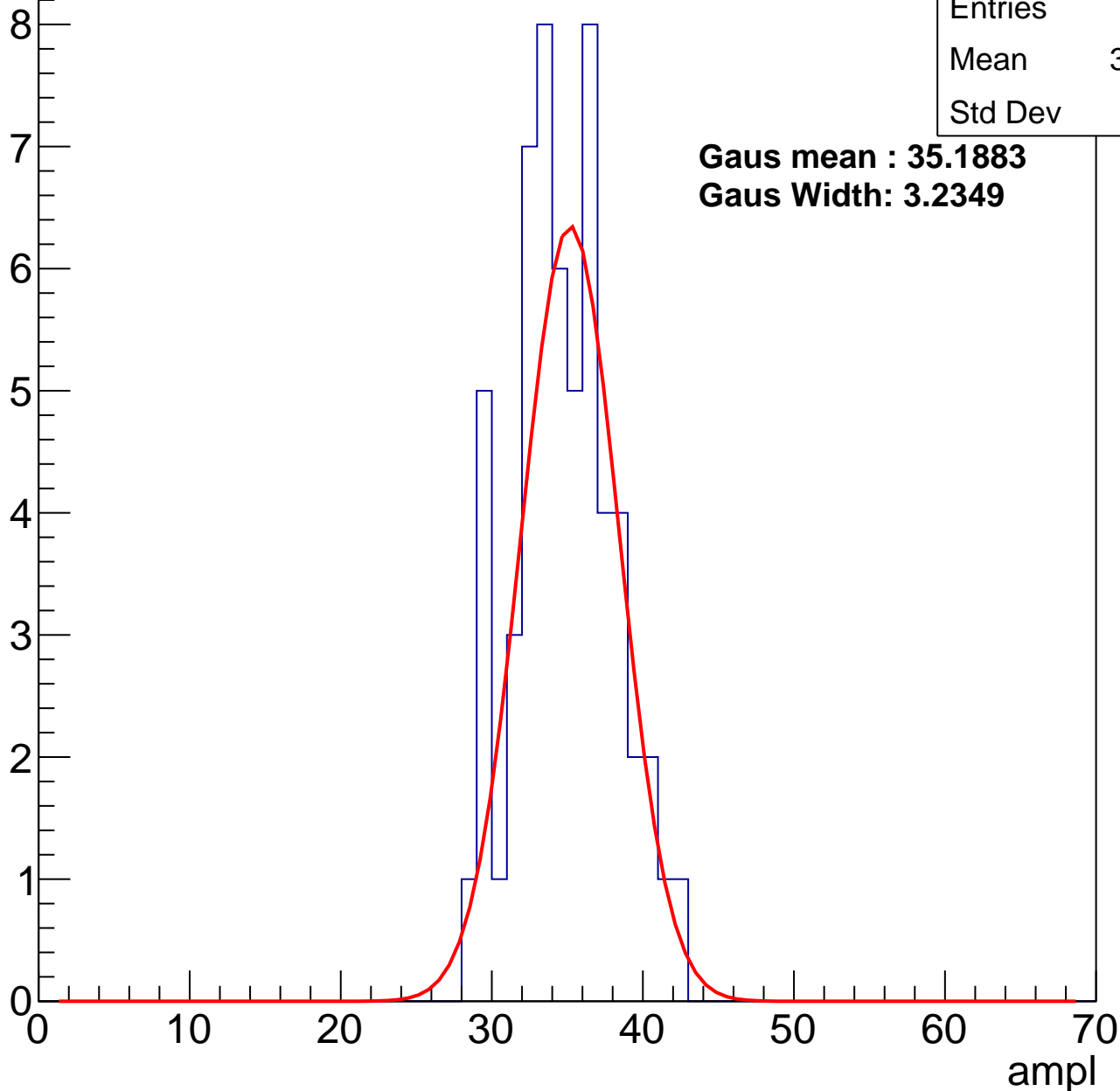
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	34.34
Std Dev	3.23

**Gaus mean : 35.1883**

**Gaus Width: 3.2349**



# B1L101S, U3-ch80, adc2

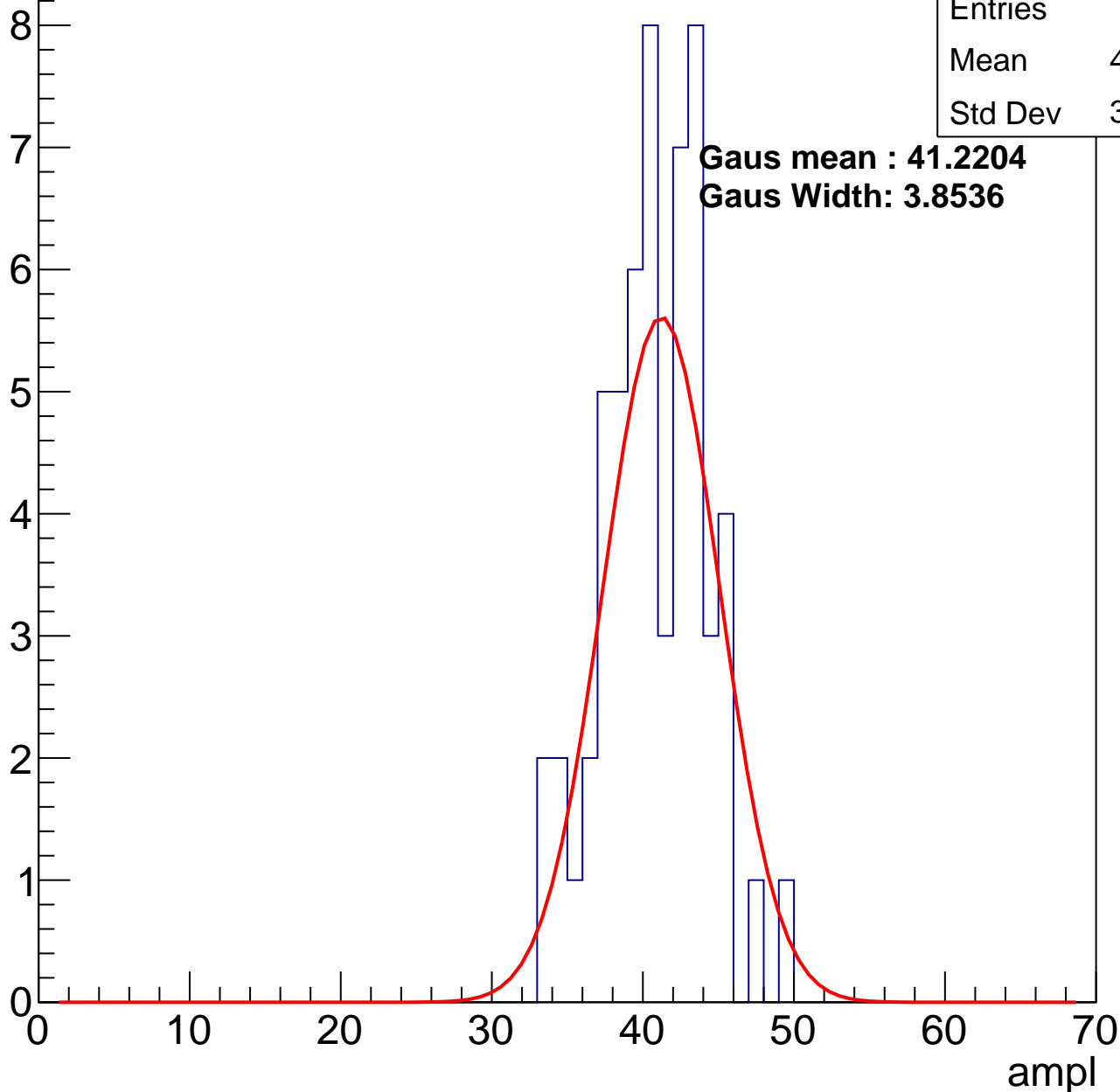
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	40.33
Std Dev	3.406

**Gaus mean : 41.2204**

**Gaus Width: 3.8536**

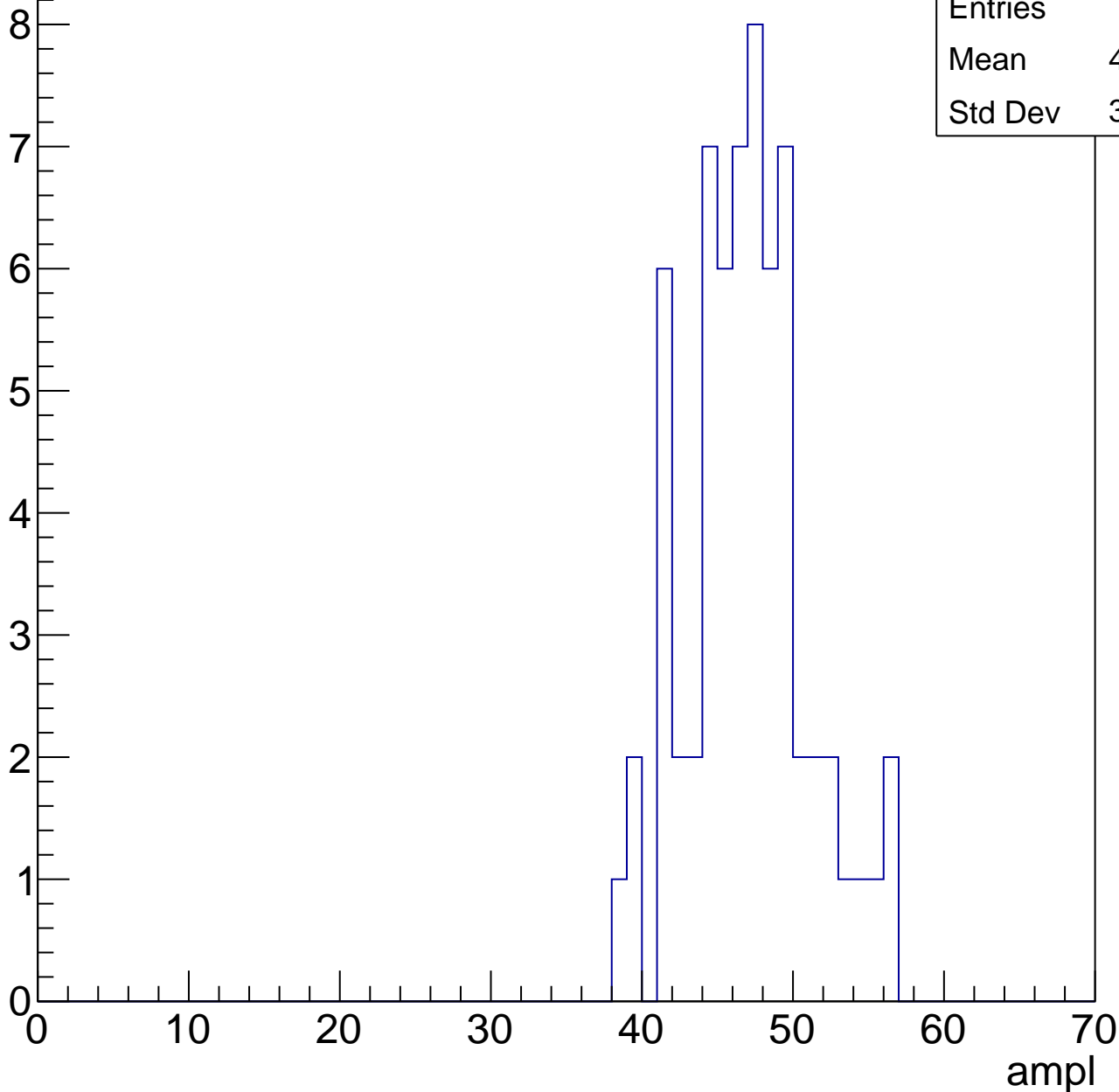


# B1L101S, U3-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

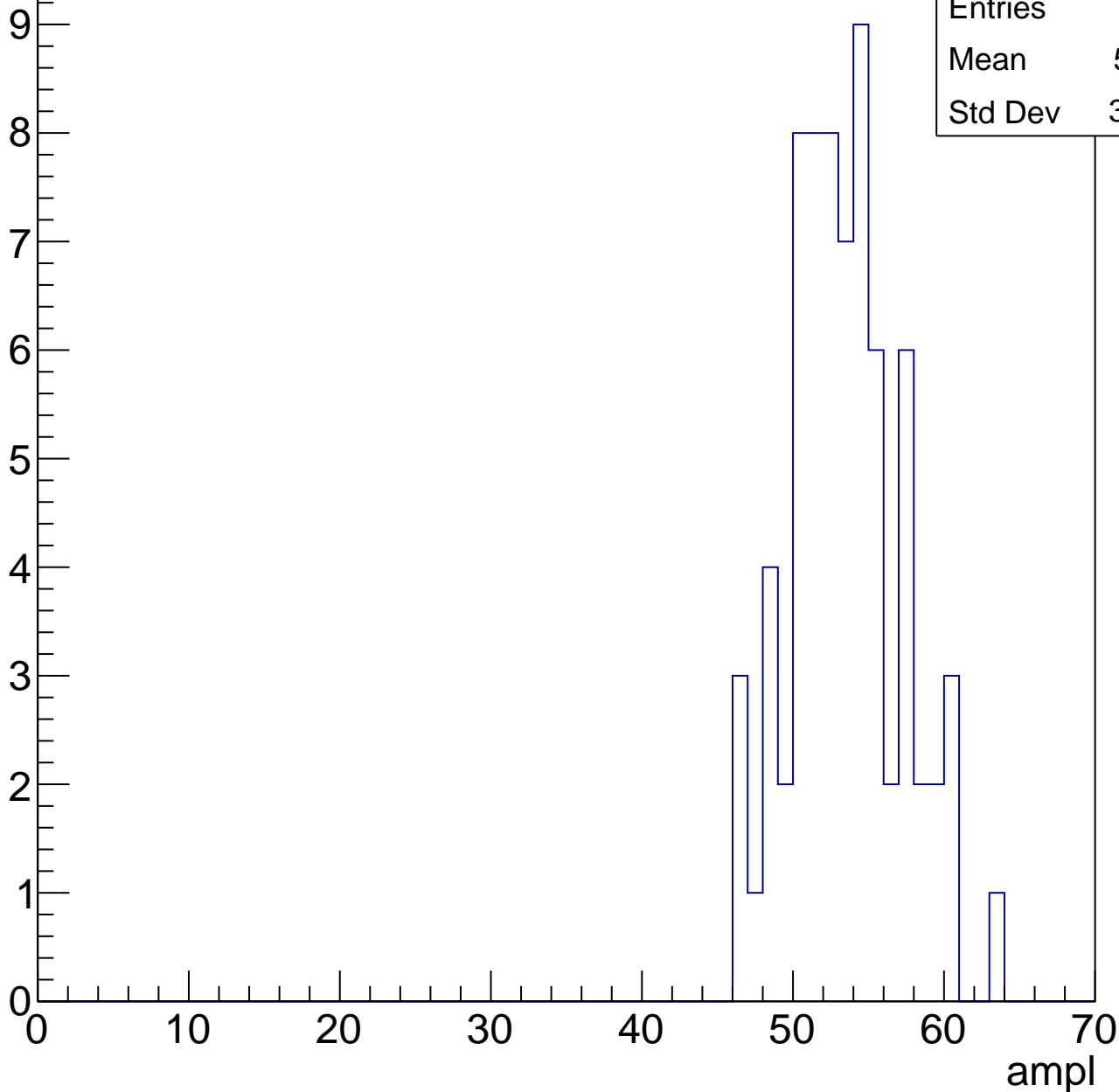
Entries	65
Mean	46.45
Std Dev	3.973



# B1L101S, U3-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

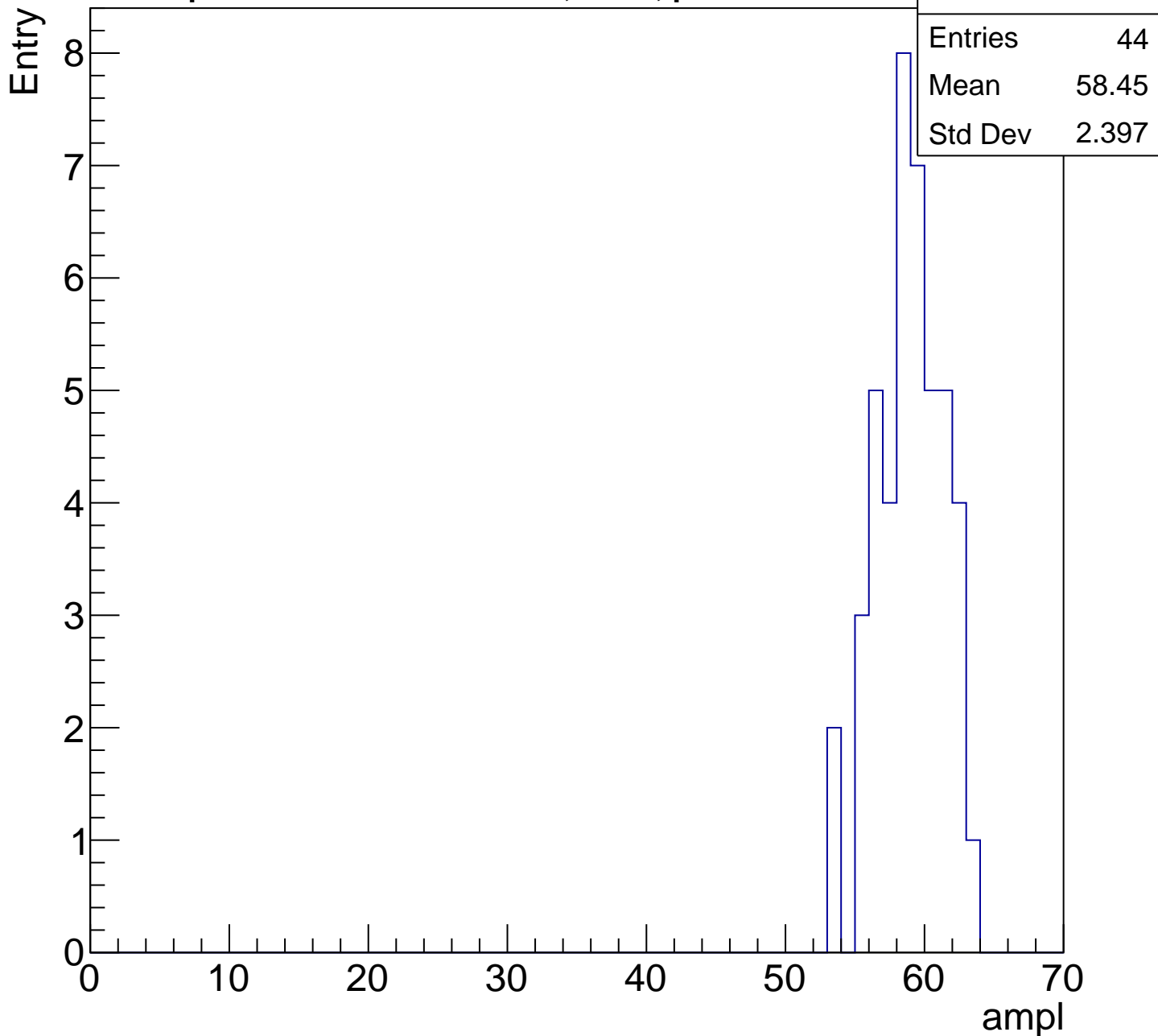
Entry



Entries	72
Mean	53.01
Std Dev	3.619

# B1L101S, U3-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

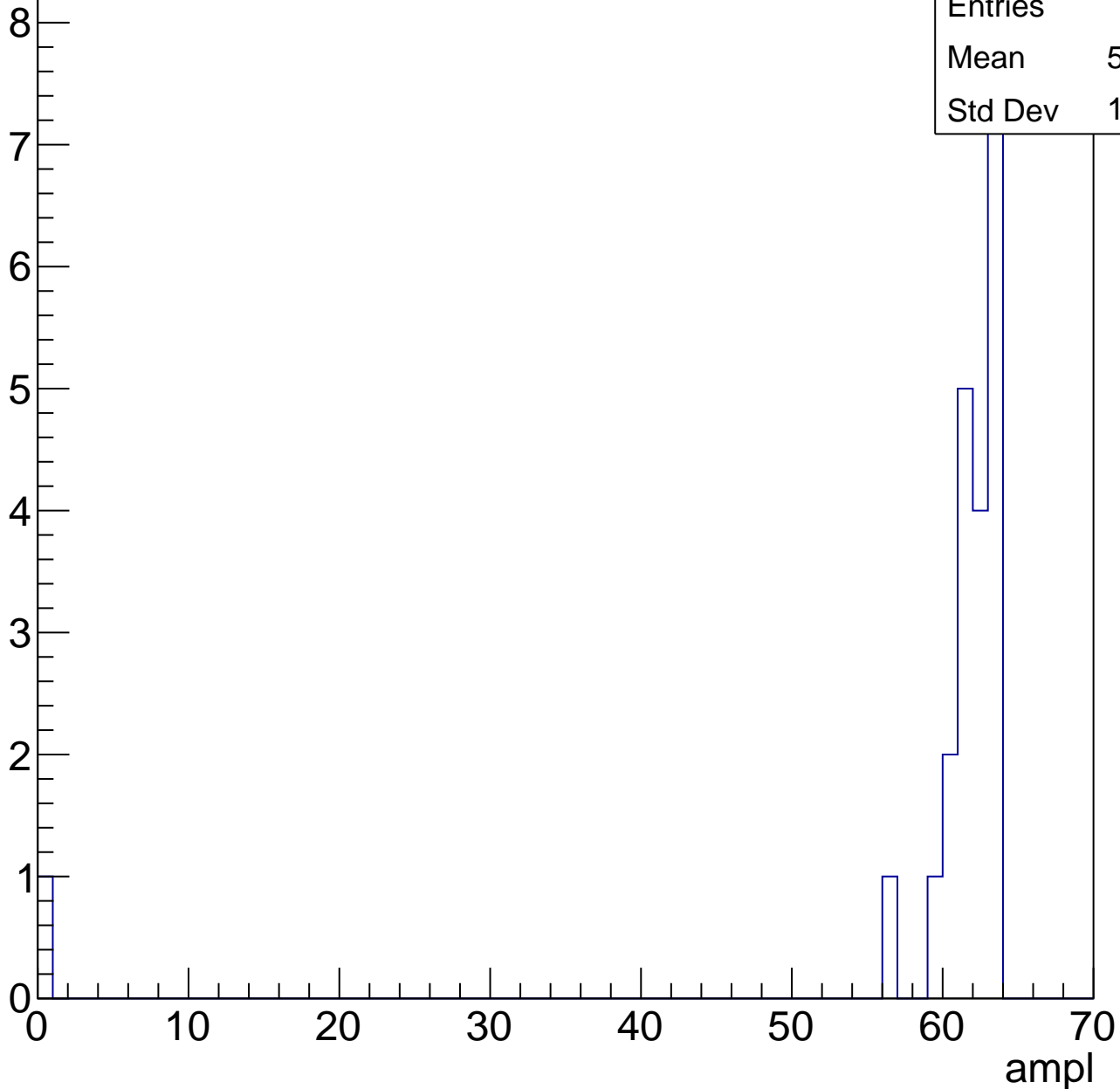


# B1L101S, U3-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	22
Mean	58.73
Std Dev	12.92





# B1L101S, U3-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch81, adc0

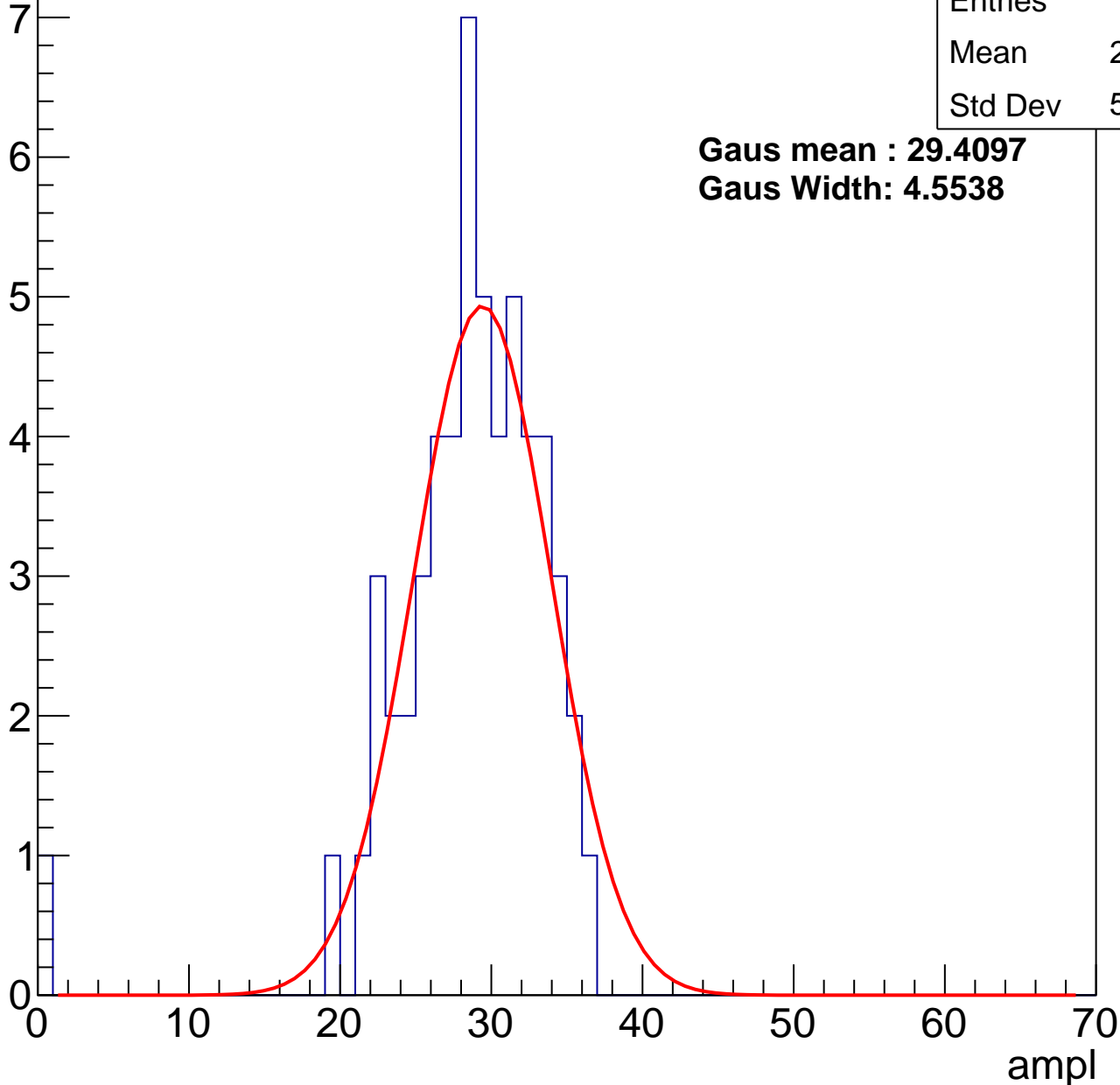
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	28.05
Std Dev	5.429

**Gaus mean : 29.4097**

**Gaus Width: 4.5538**



# B1L101S, U3-ch81, adc1

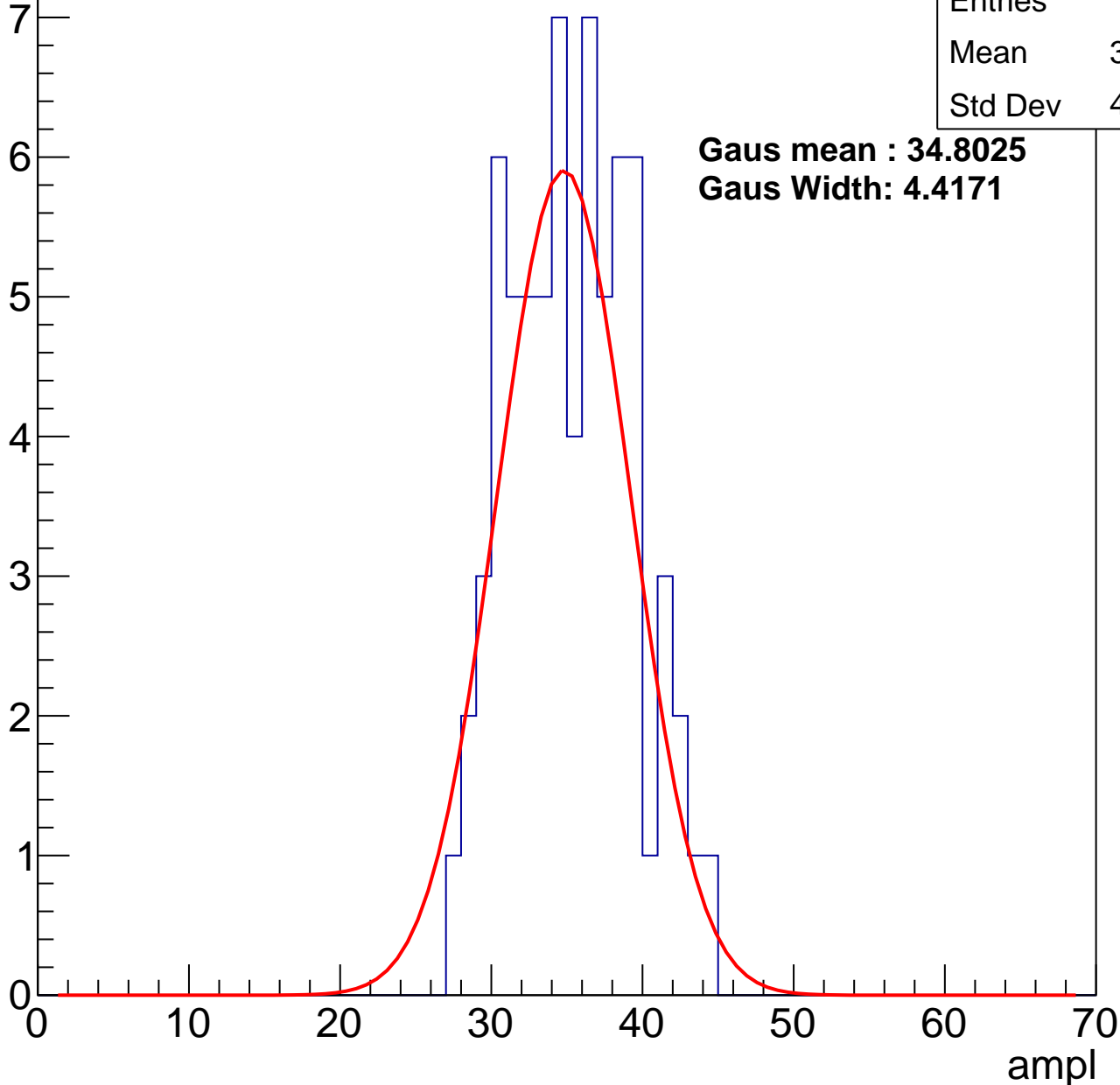
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	34.87
Std Dev	4.007

**Gaus mean : 34.8025**

**Gaus Width: 4.4171**



# B1L101S, U3-ch81, adc2

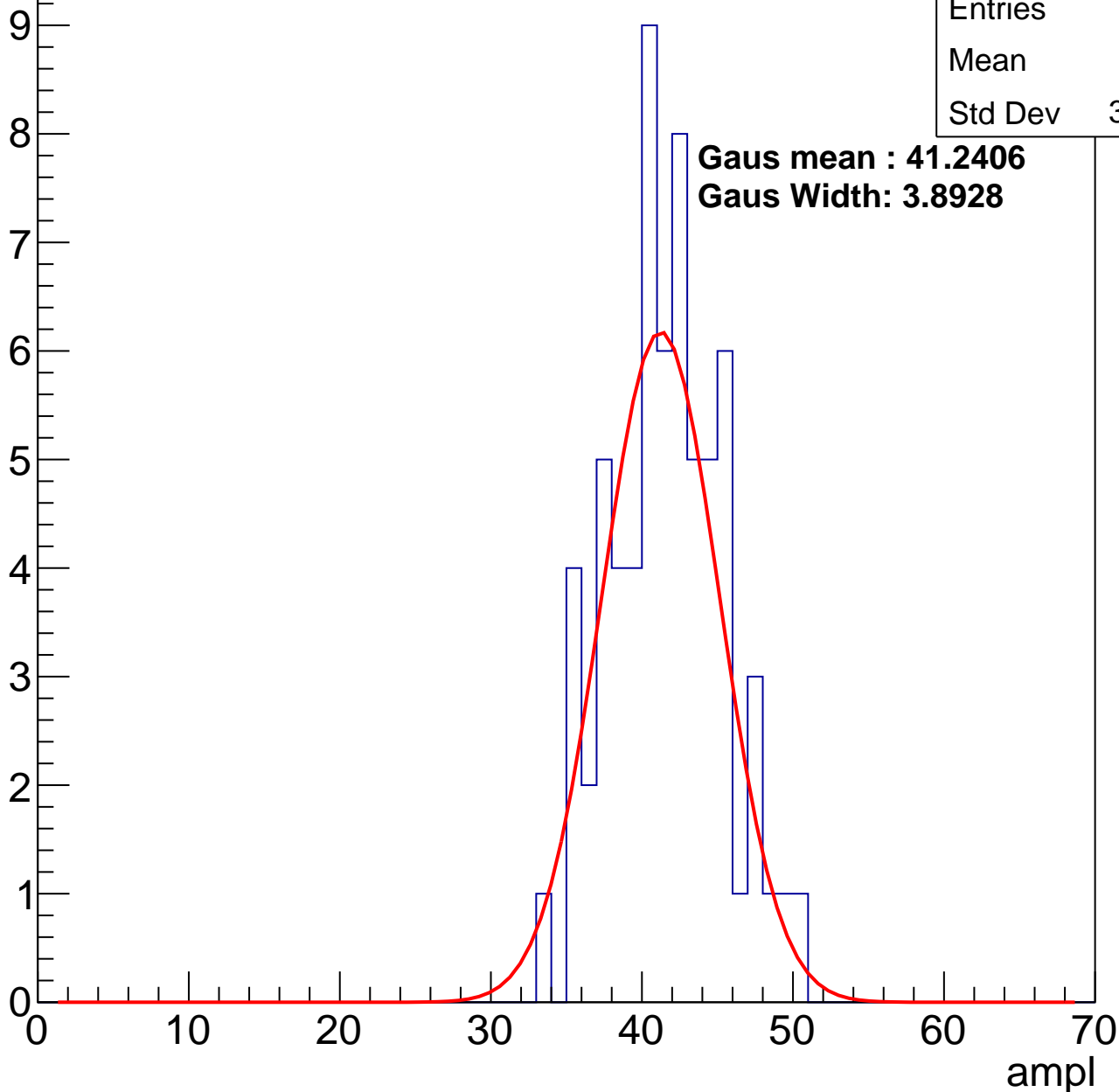
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	41.2
Std Dev	3.677

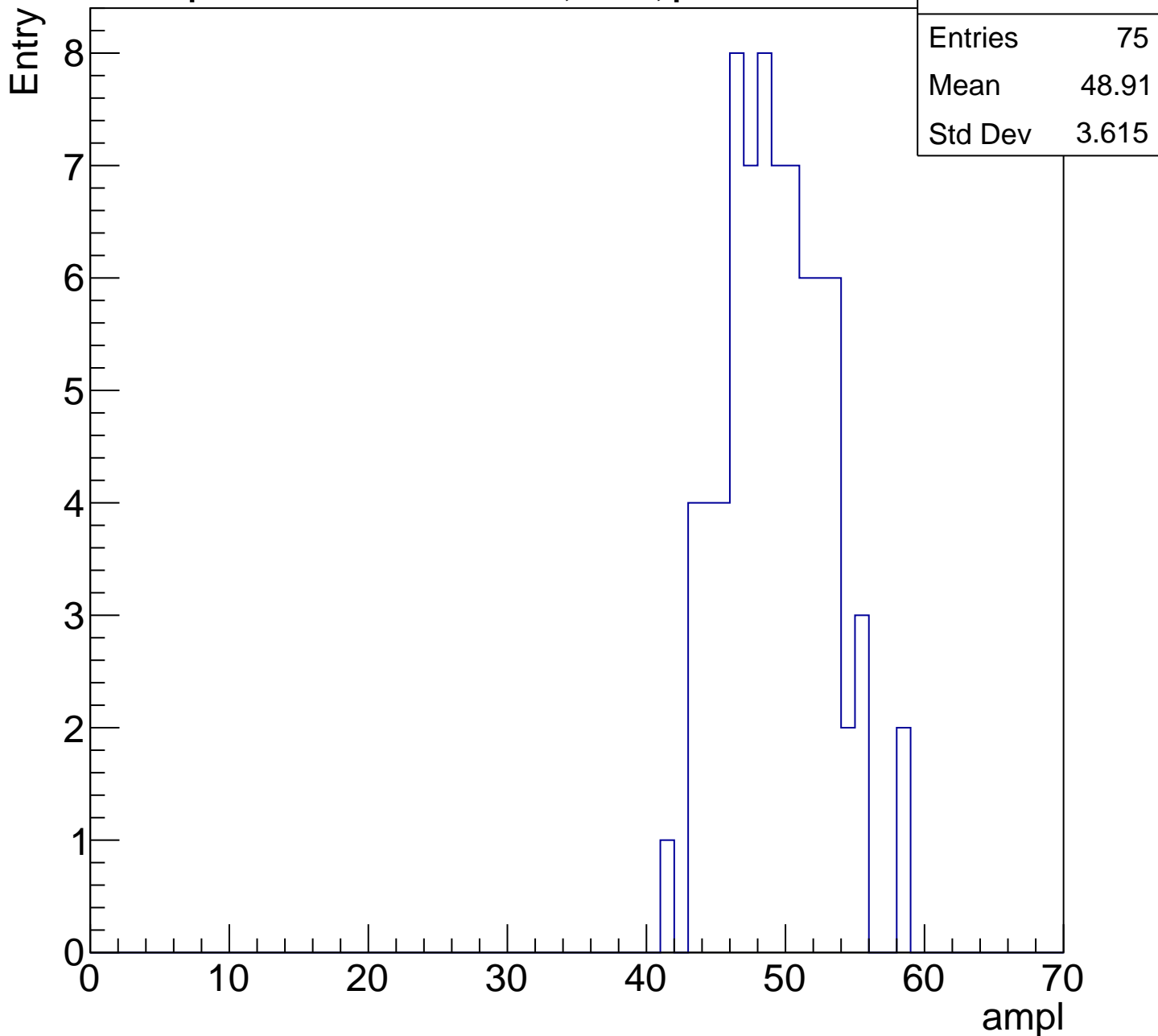
**Gaus mean : 41.2406**

**Gaus Width: 3.8928**



# B1L101S, U3-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

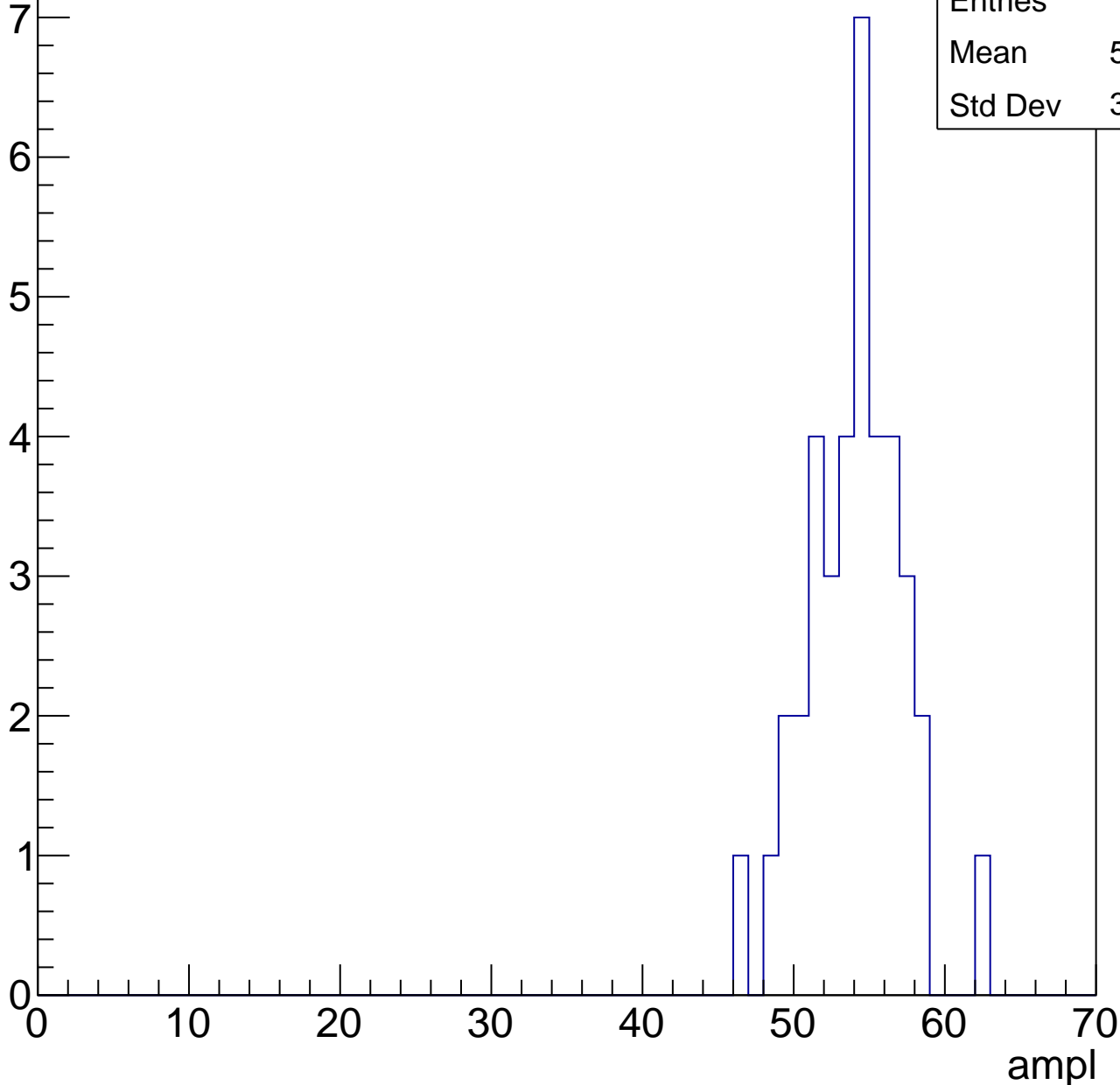


# B1L101S, U3-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

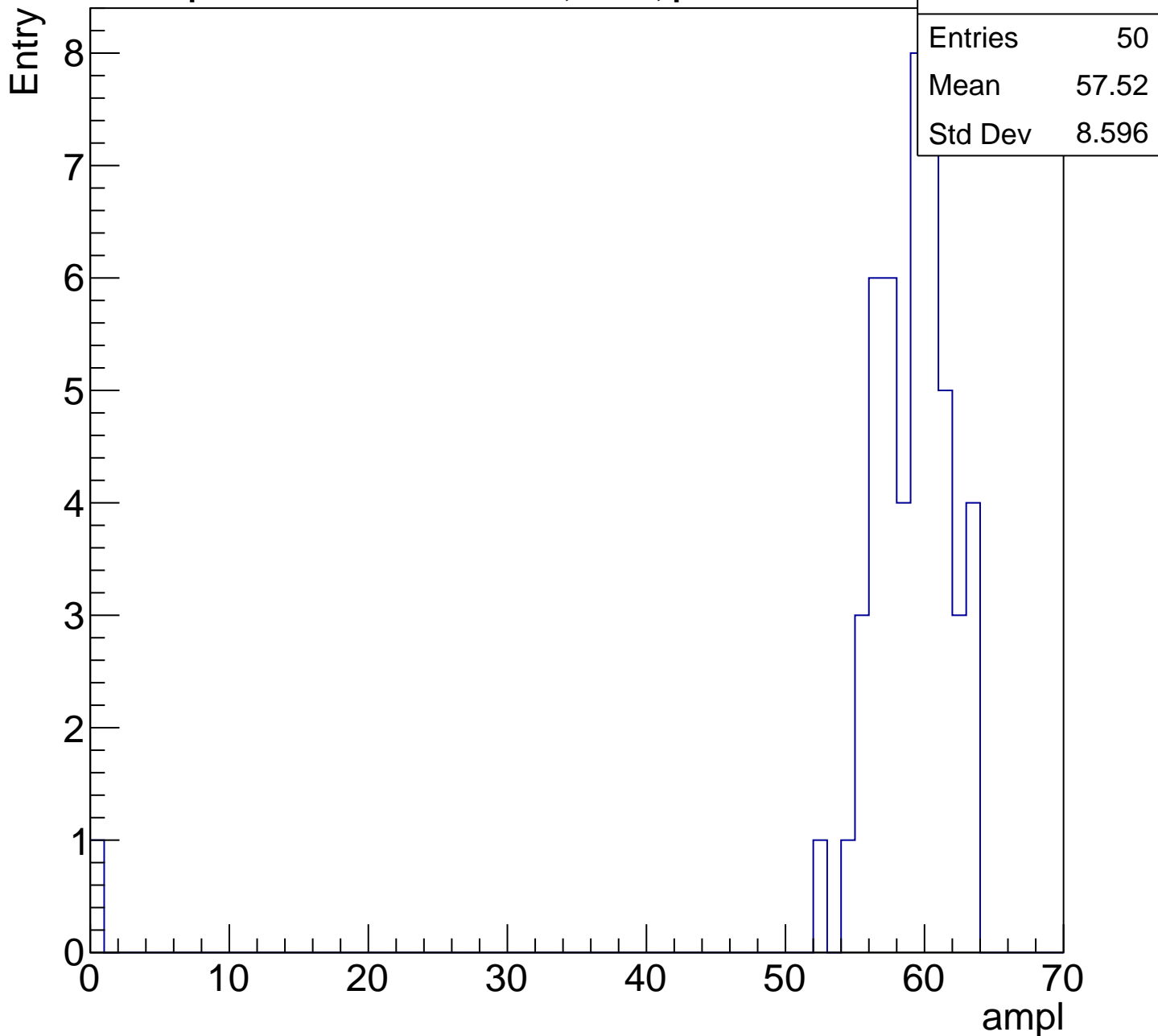
Entry

Entries	38
Mean	53.55
Std Dev	3.118



# B1L101S, U3-ch81, adc5

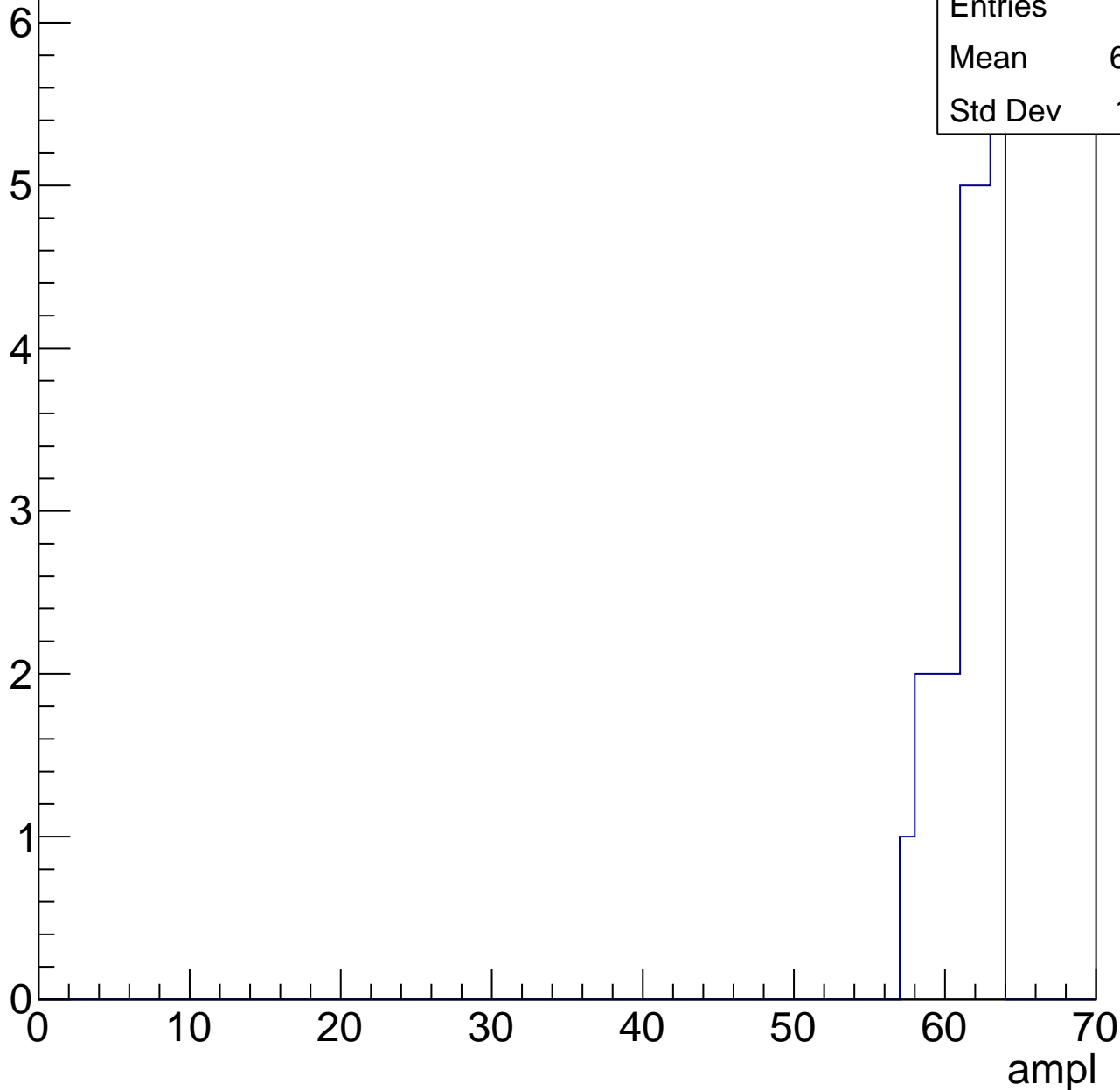
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

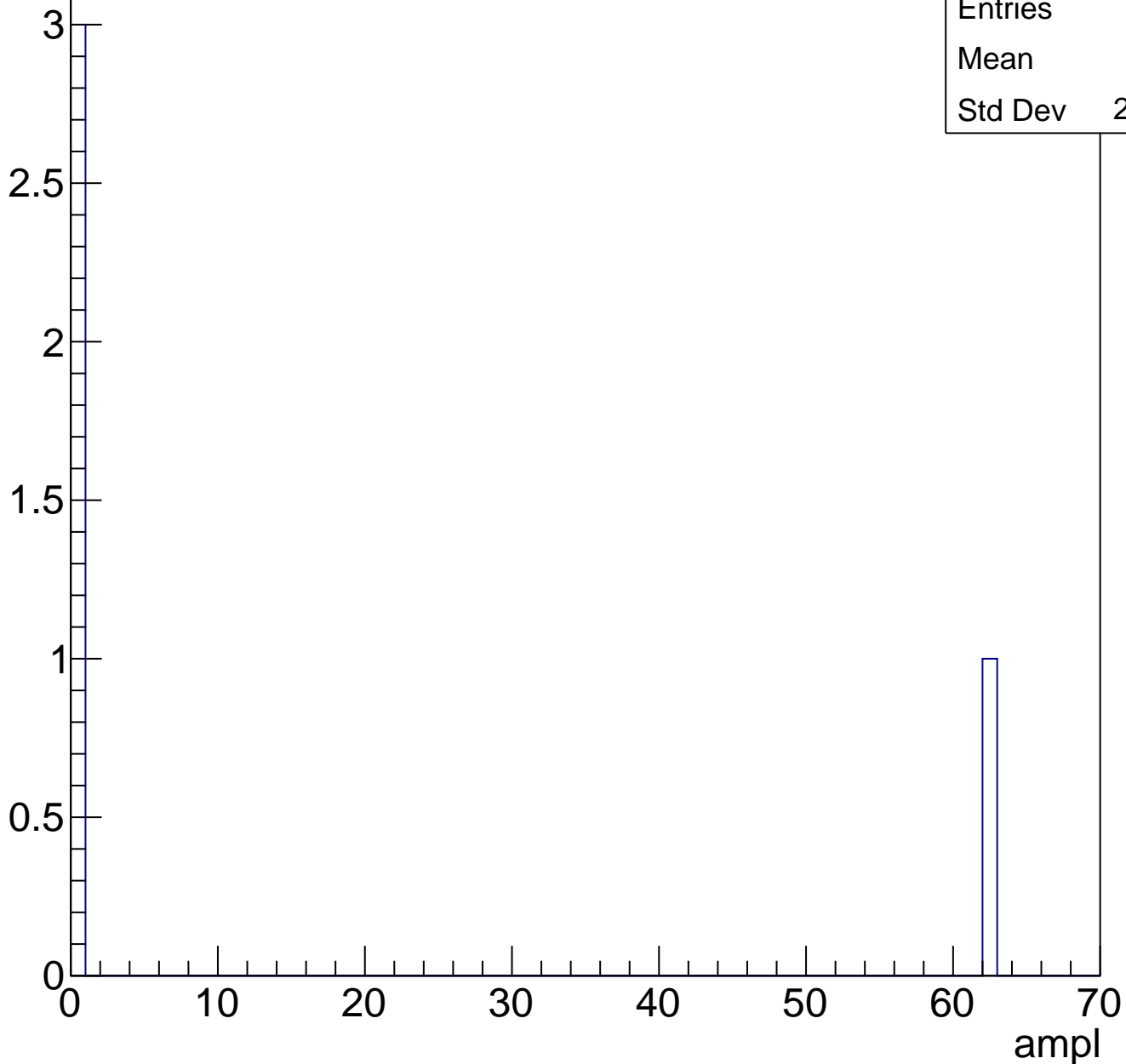




# B1L101S, U3-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch82, adc0

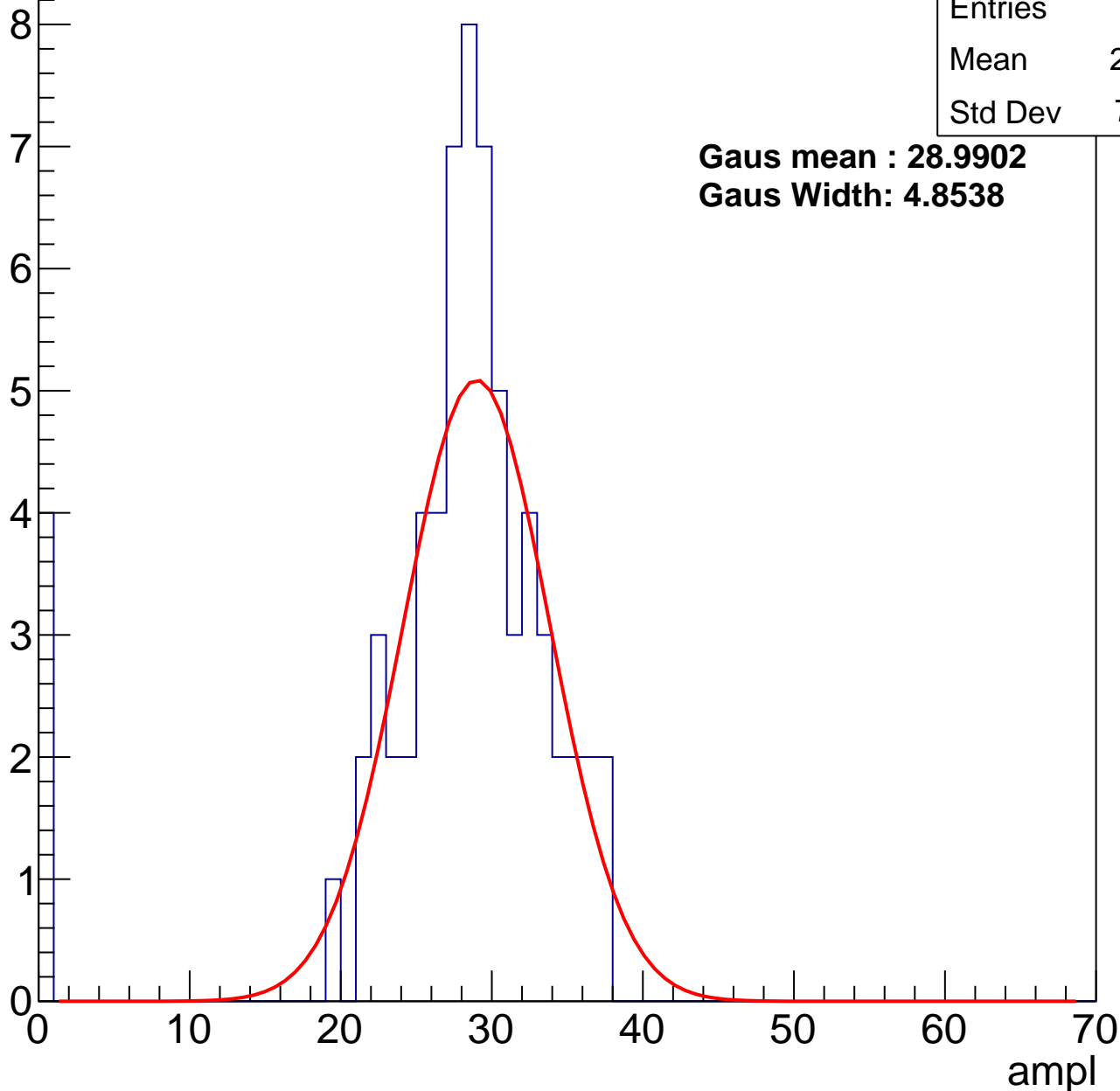
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	26.79
Std Dev	7.841

**Gaus mean : 28.9902**

**Gaus Width: 4.8538**



# B1L101S, U3-ch82, adc1

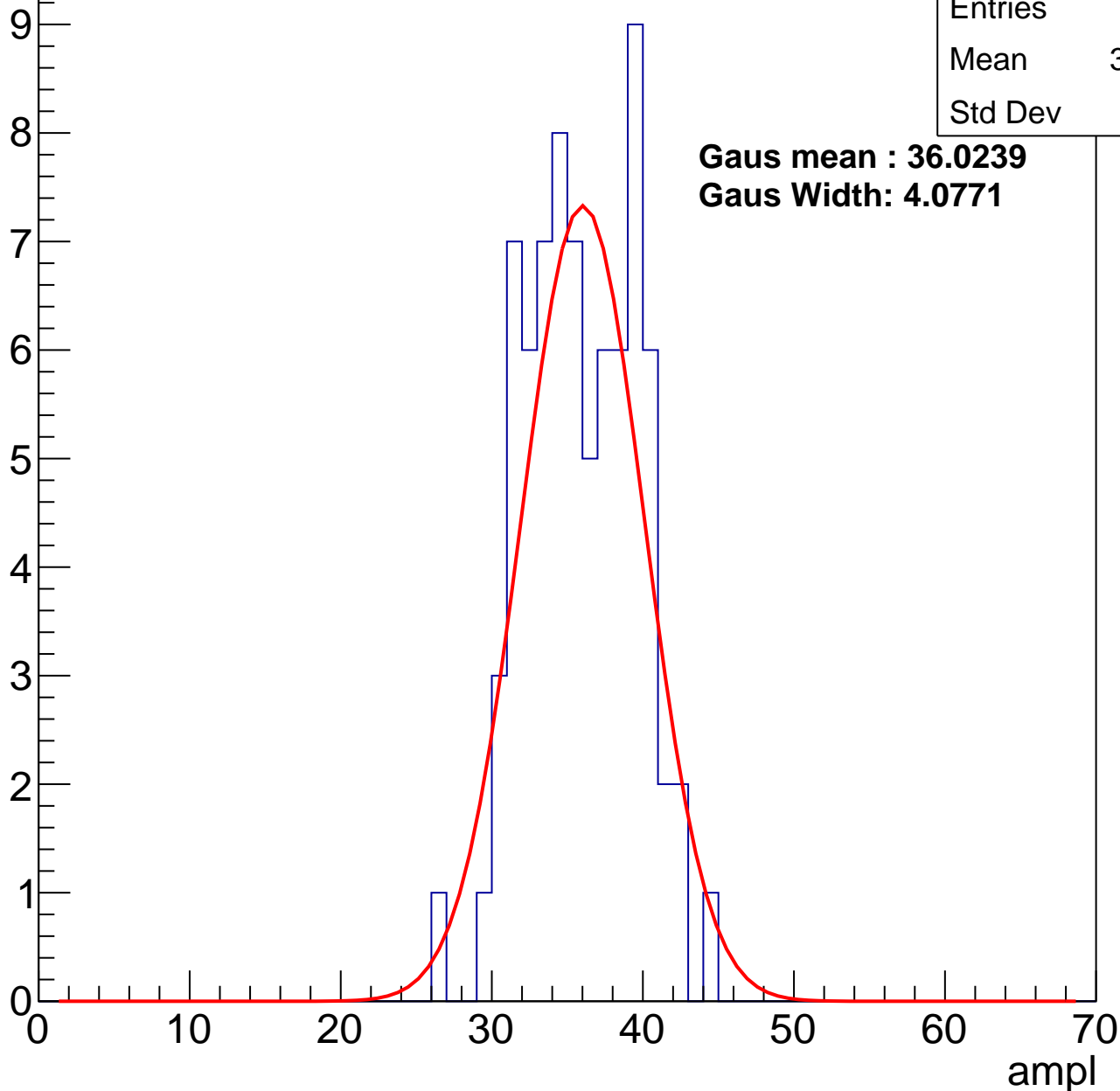
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	35.49
Std Dev	3.61

**Gaus mean : 36.0239**

**Gaus Width: 4.0771**



# B1L101S, U3-ch82, adc2

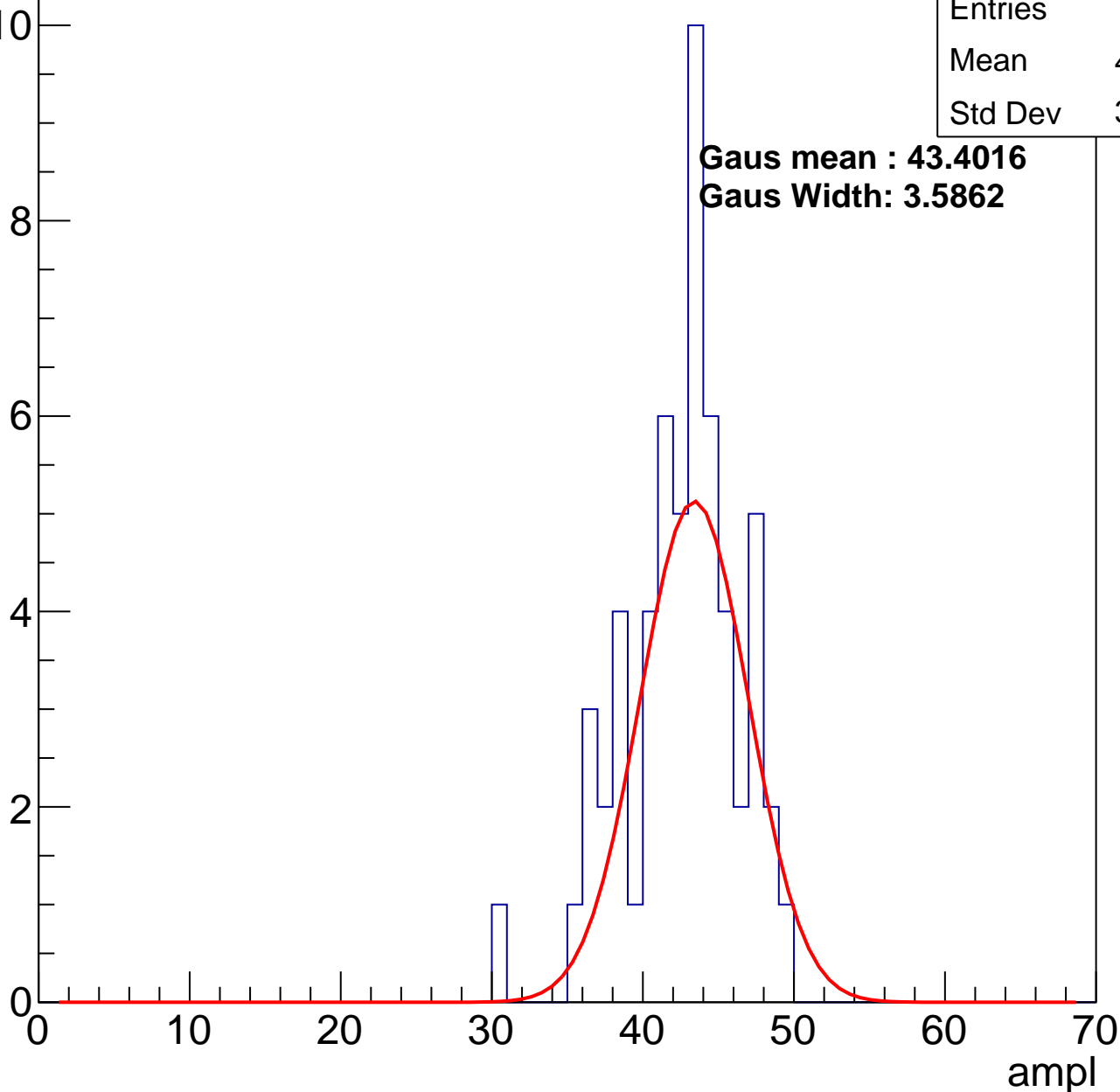
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	42.11
Std Dev	3.731

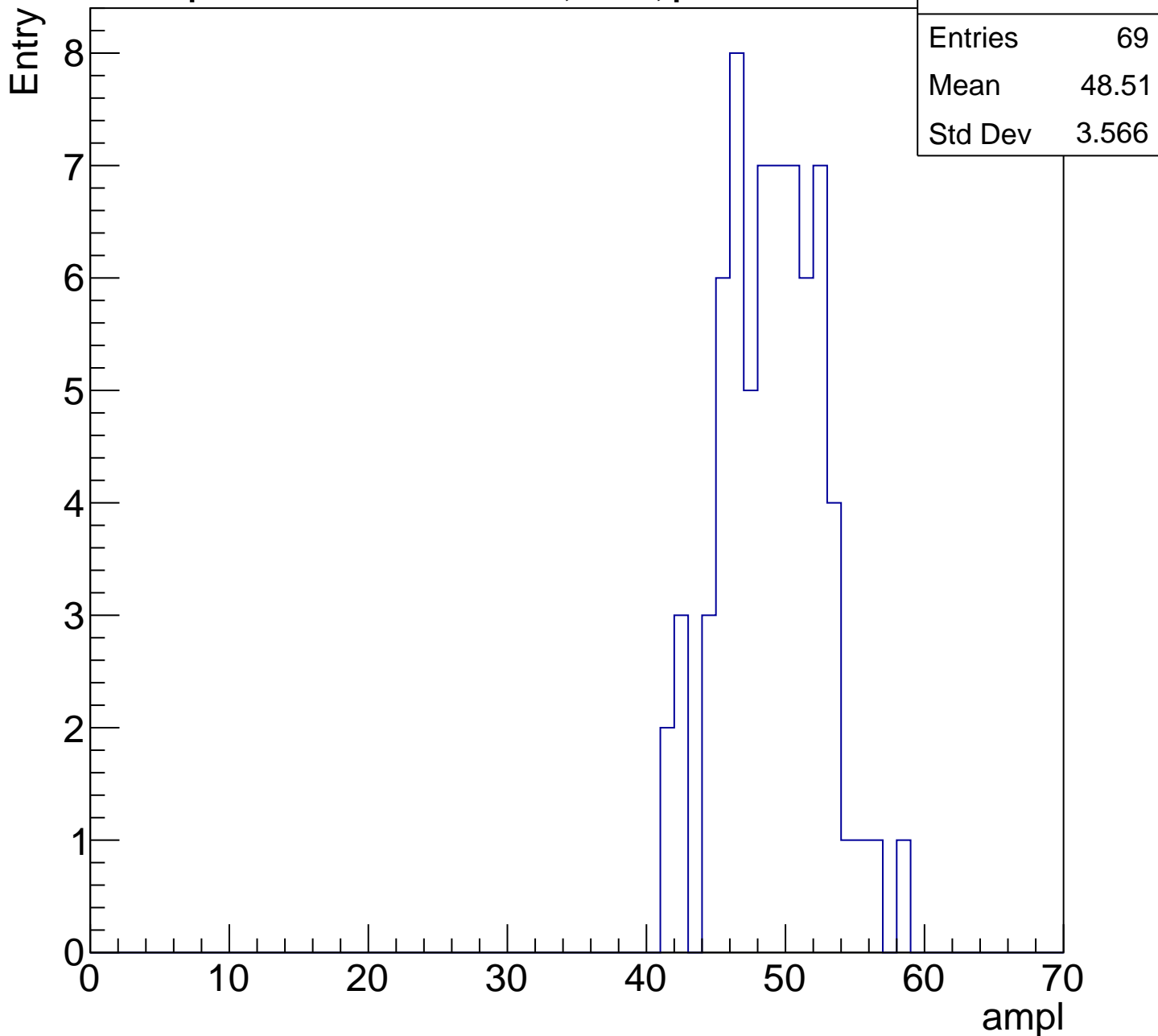
**Gaus mean : 43.4016**

**Gaus Width: 3.5862**



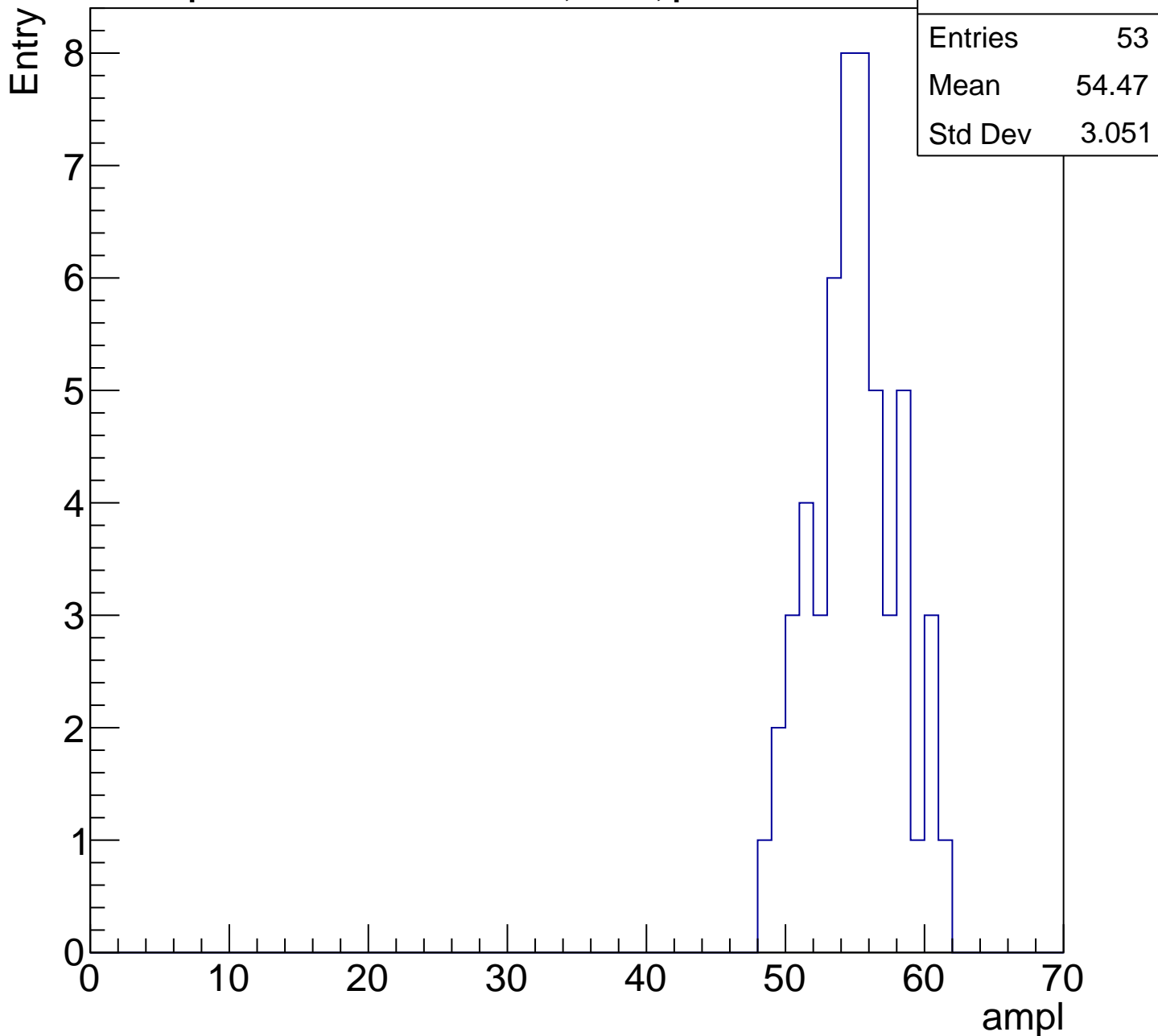
# B1L101S, U3-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2



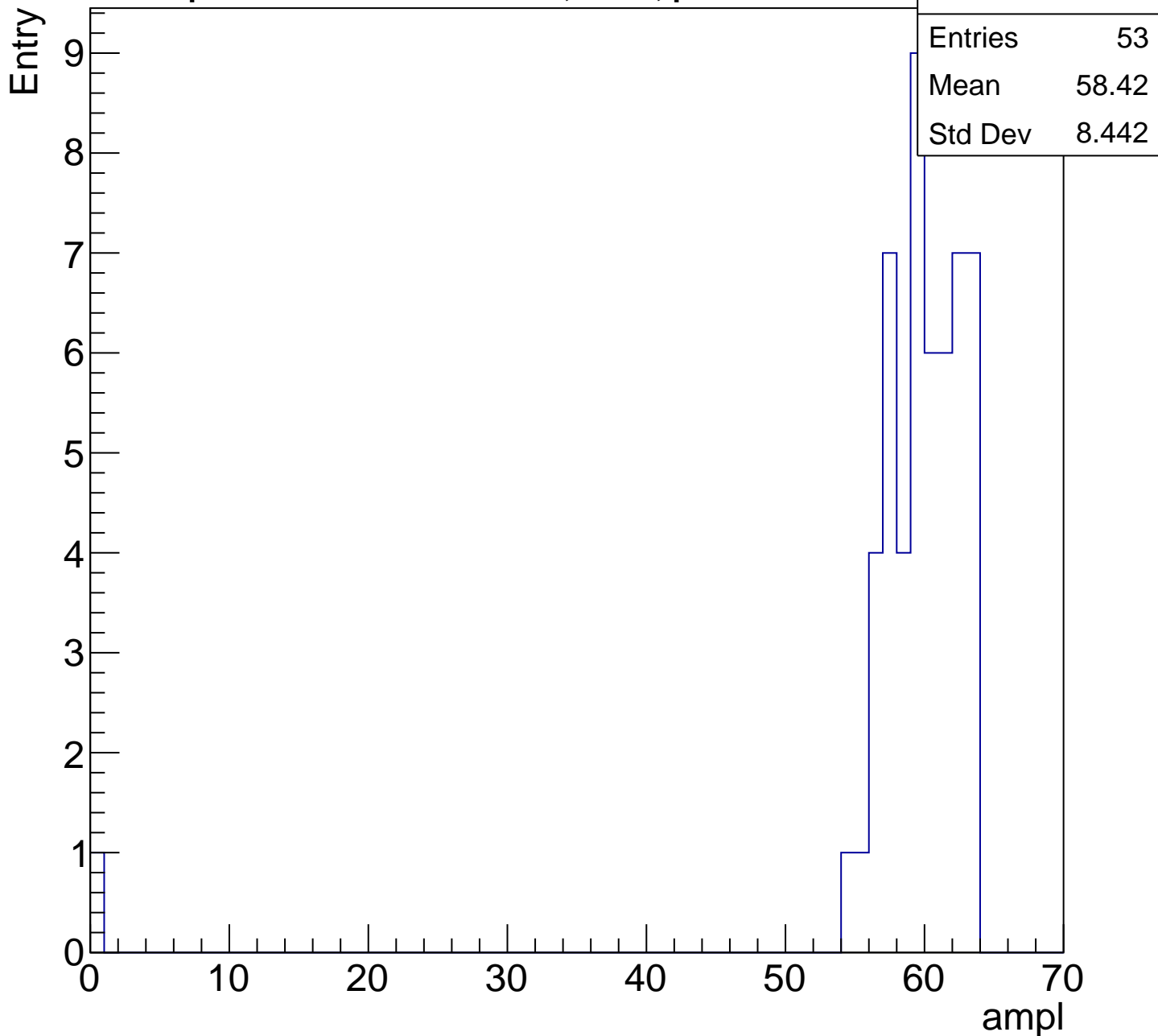
# B1L101S, U3-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch82, adc5

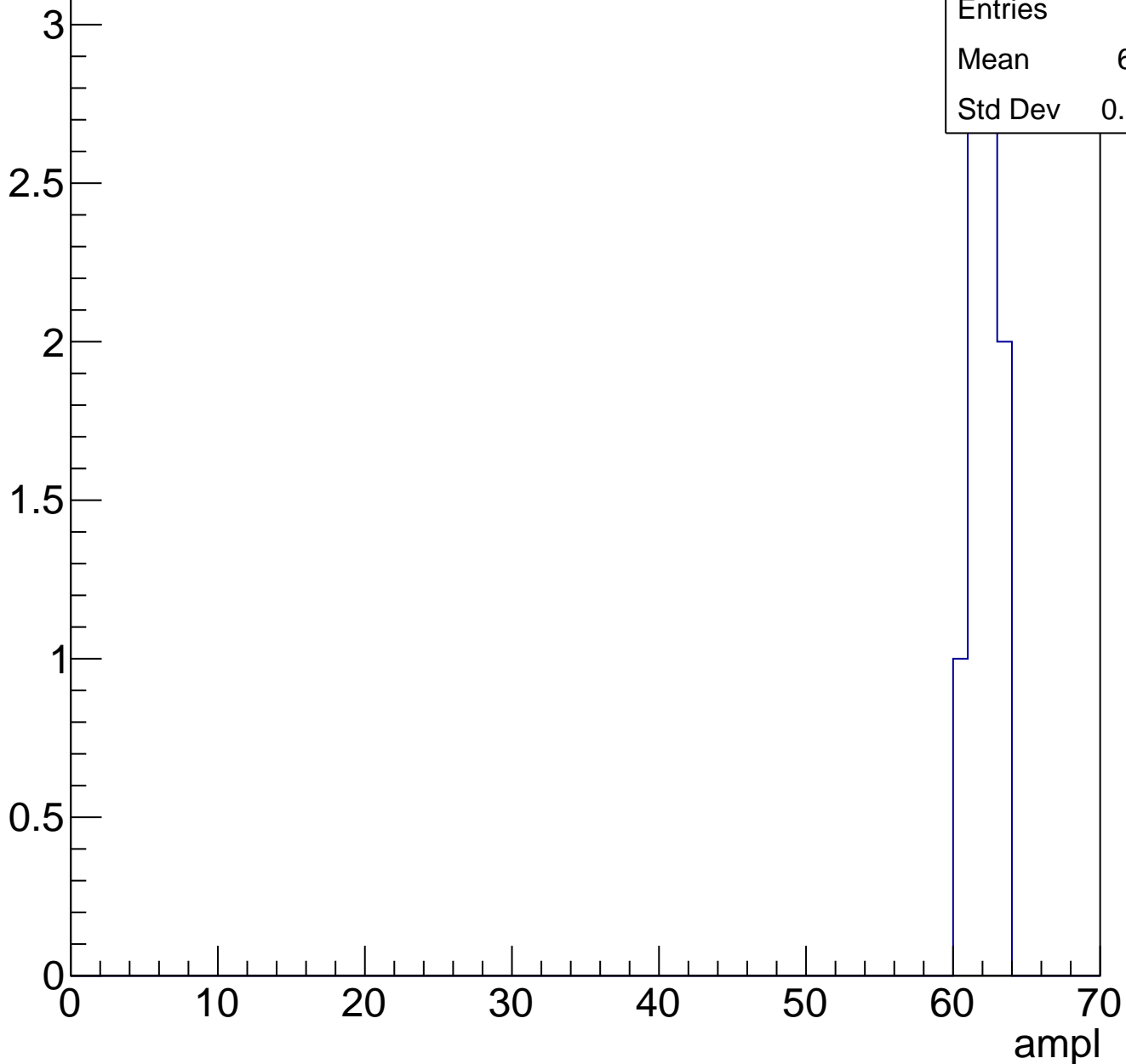
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L101S, U3-ch83, adc0

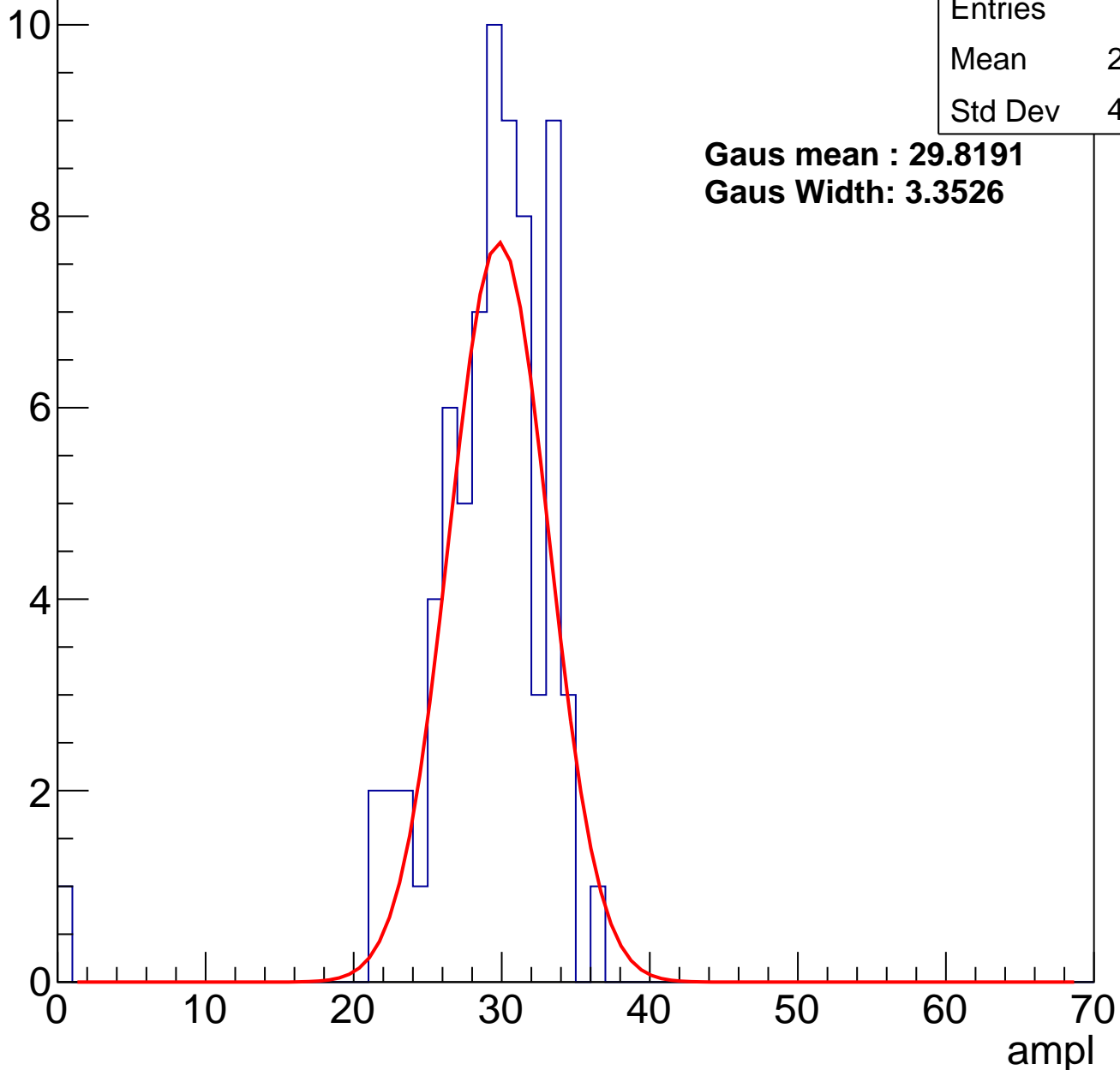
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	73
Mean	28.52
Std Dev	4.723

**Gaus mean : 29.8191**

**Gaus Width: 3.3526**

Entry



# B1L101S, U3-ch83, adc1

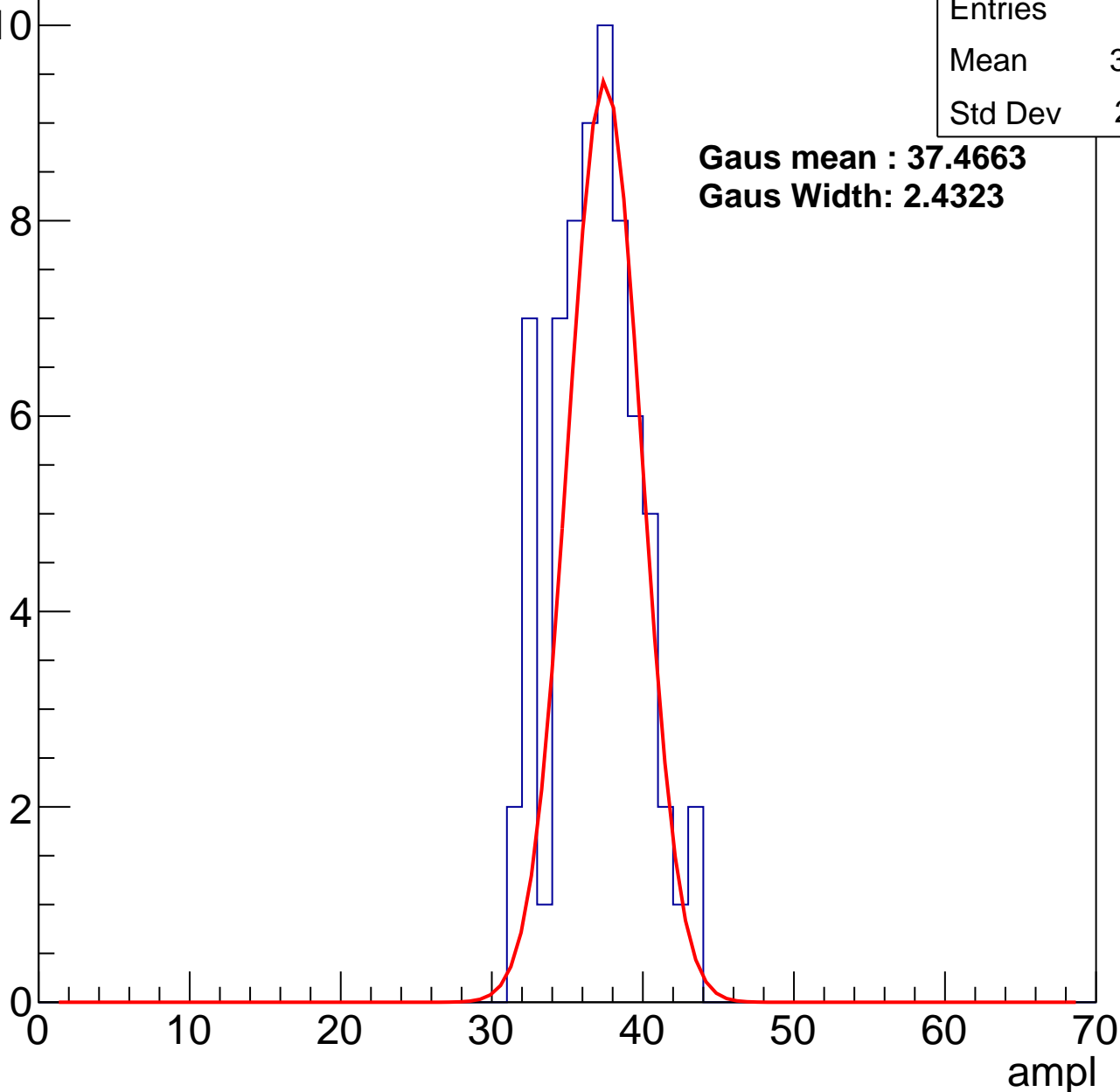
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	36.46
Std Dev	2.851

**Gaus mean : 37.4663**

**Gaus Width: 2.4323**



# B1L101S, U3-ch83, adc2

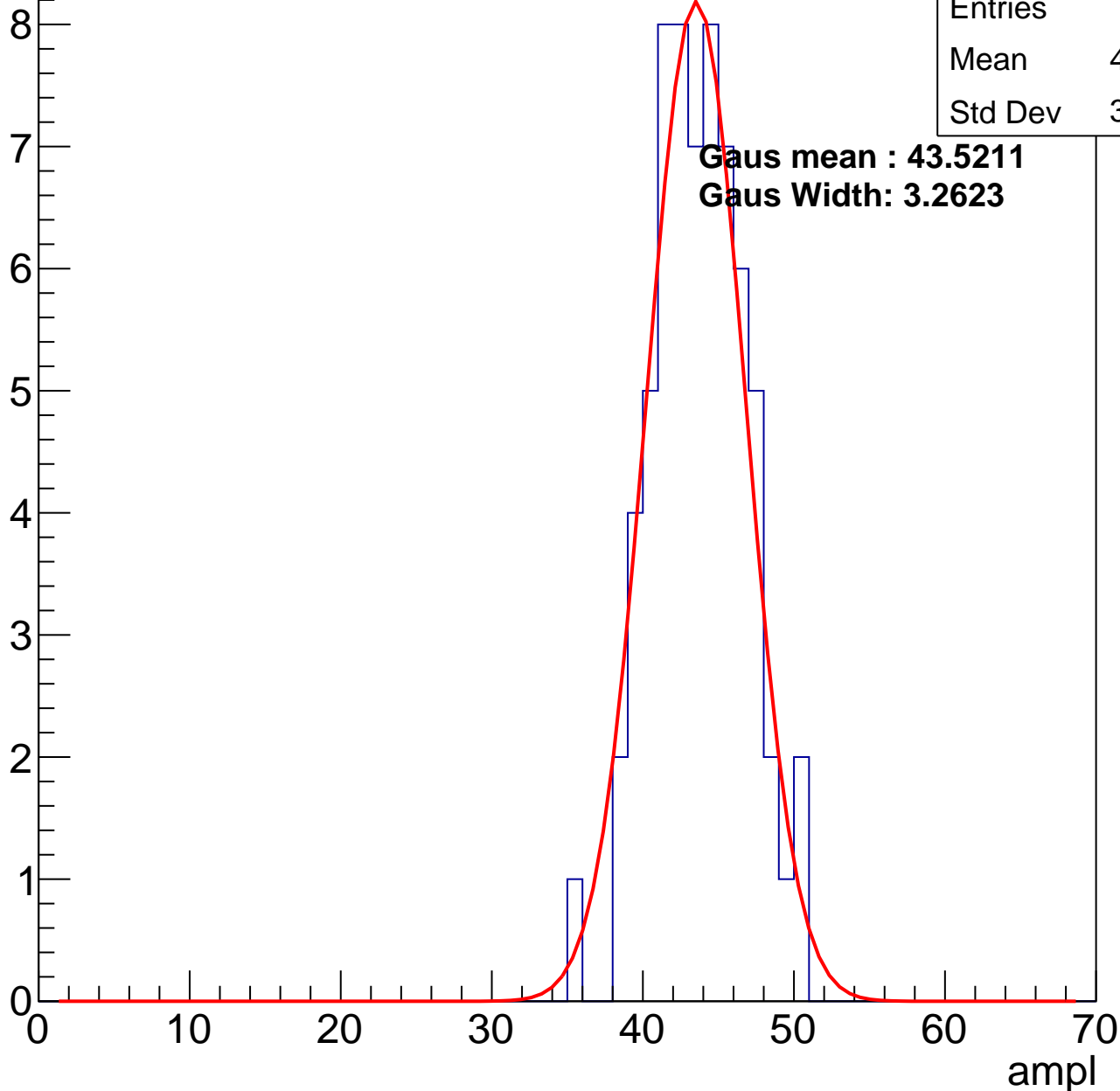
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	43.26
Std Dev	3.047

**Gaus mean : 43.5211**

**Gaus Width: 3.2623**

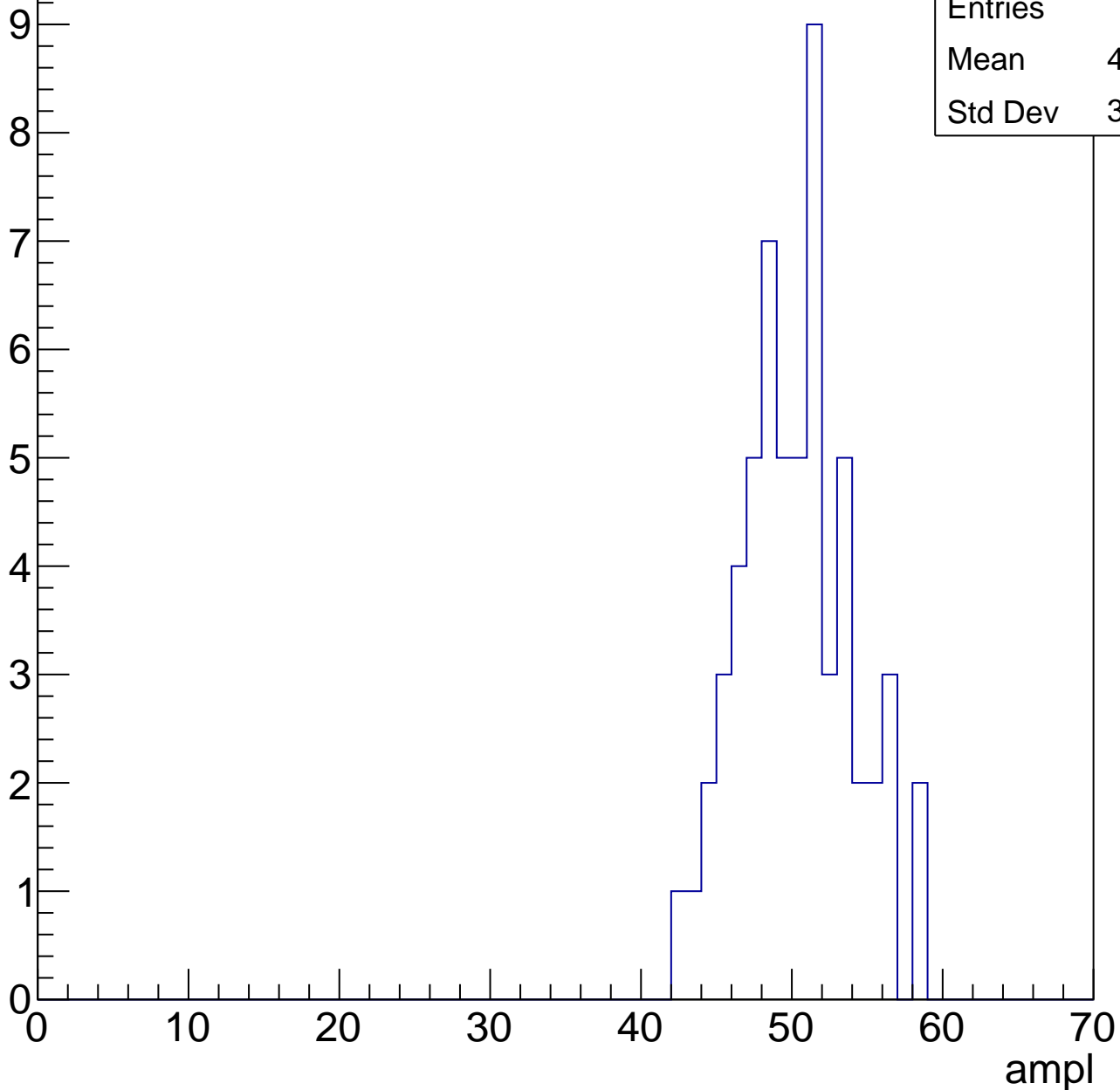


# B1L101S, U3-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	49.83
Std Dev	3.646

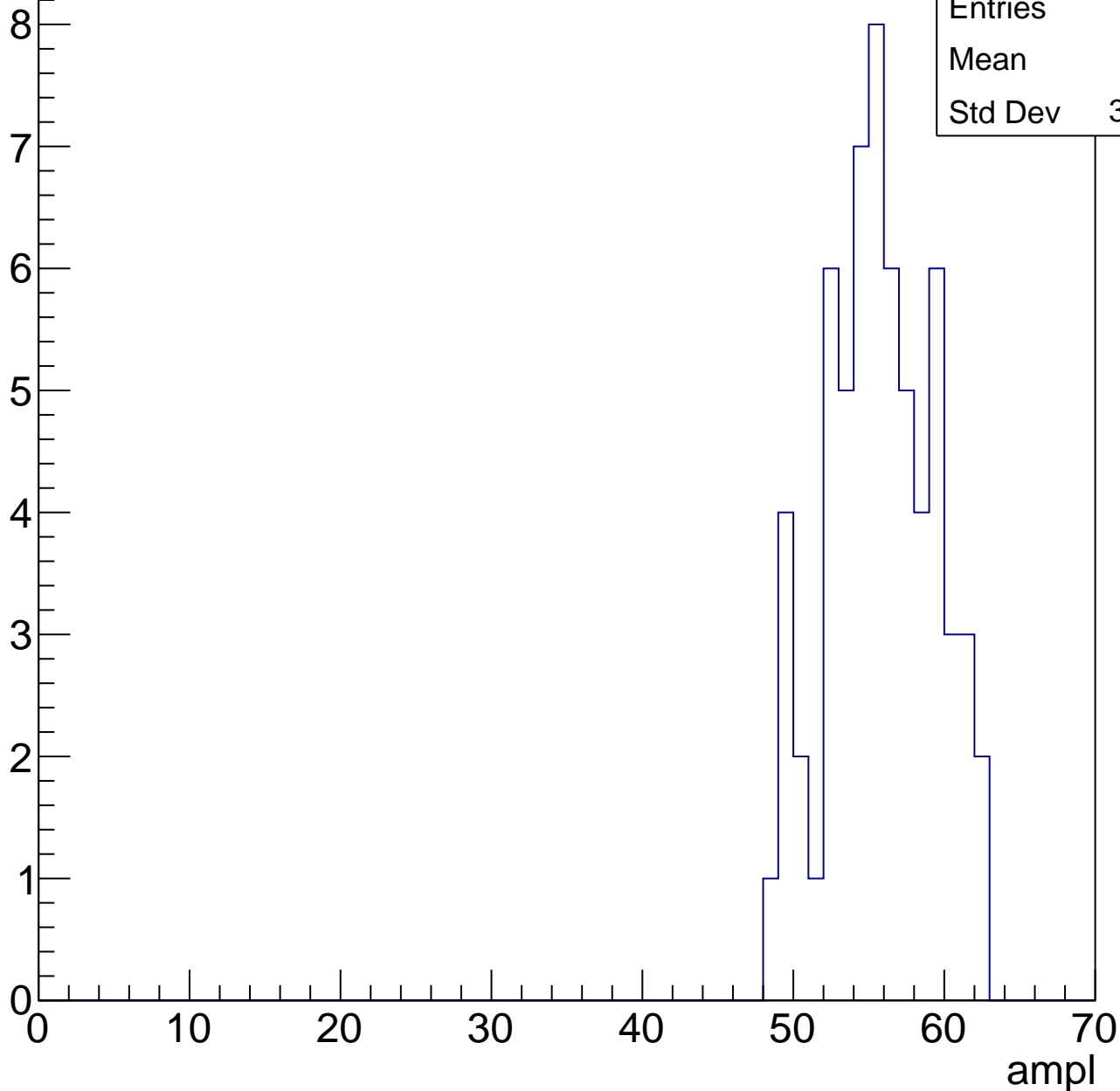


# B1L101S, U3-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

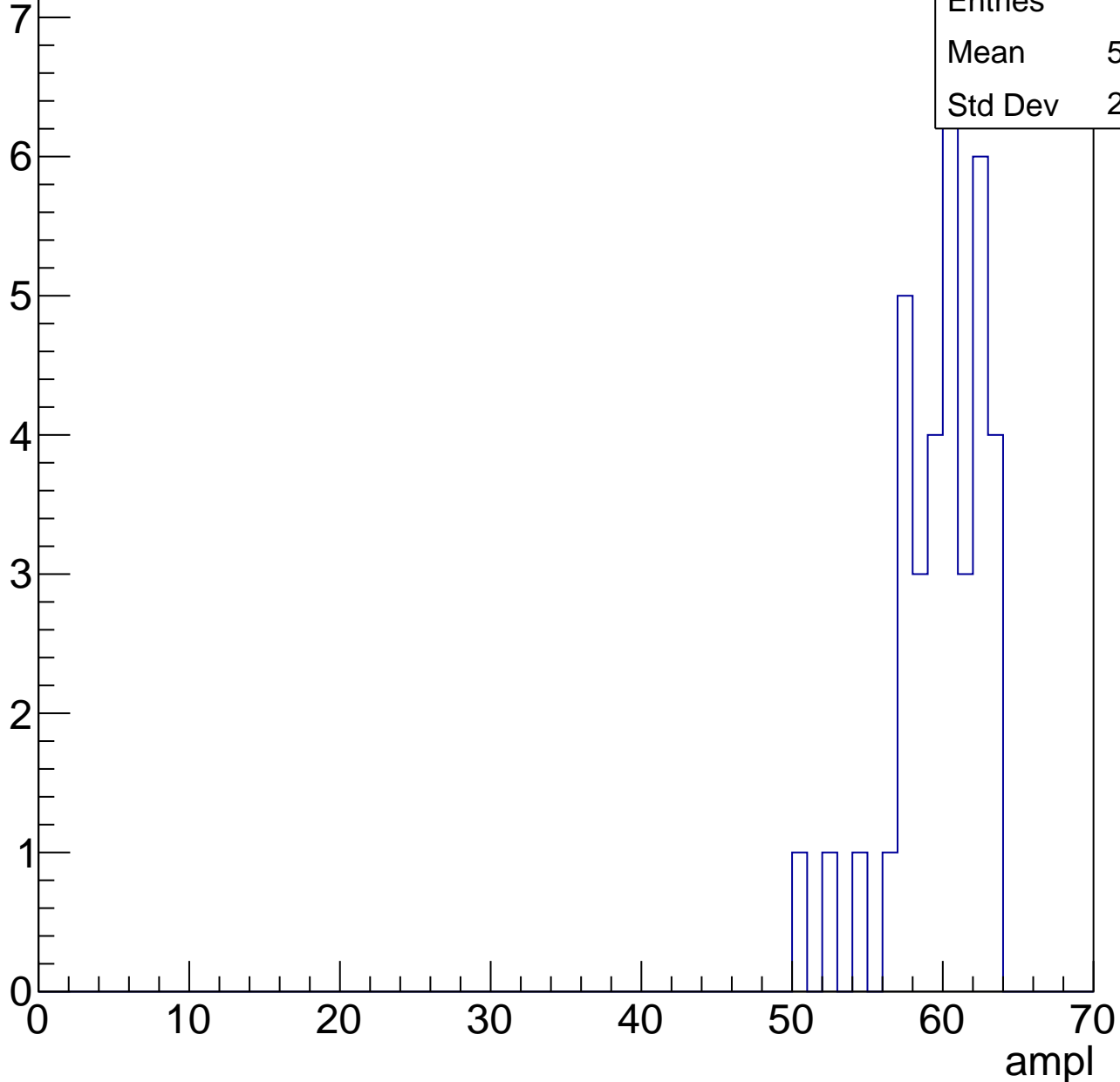
Entries	63
Mean	55.3
Std Dev	3.503



# B1L101S, U3-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

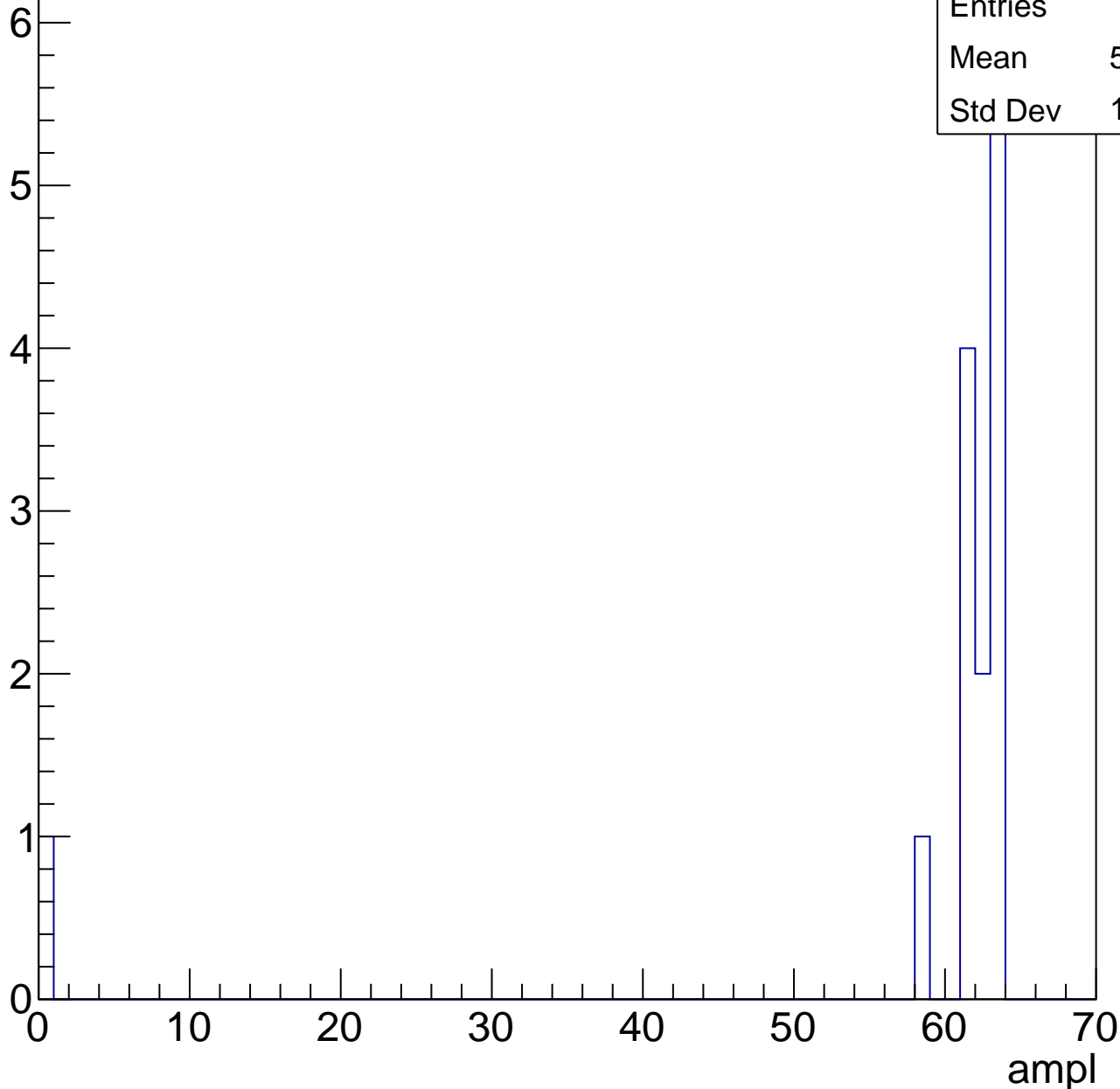


# B1L101S, U3-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	14
Mean	57.43
Std Dev	15.99





# B1L101S, U3-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch84, adc0

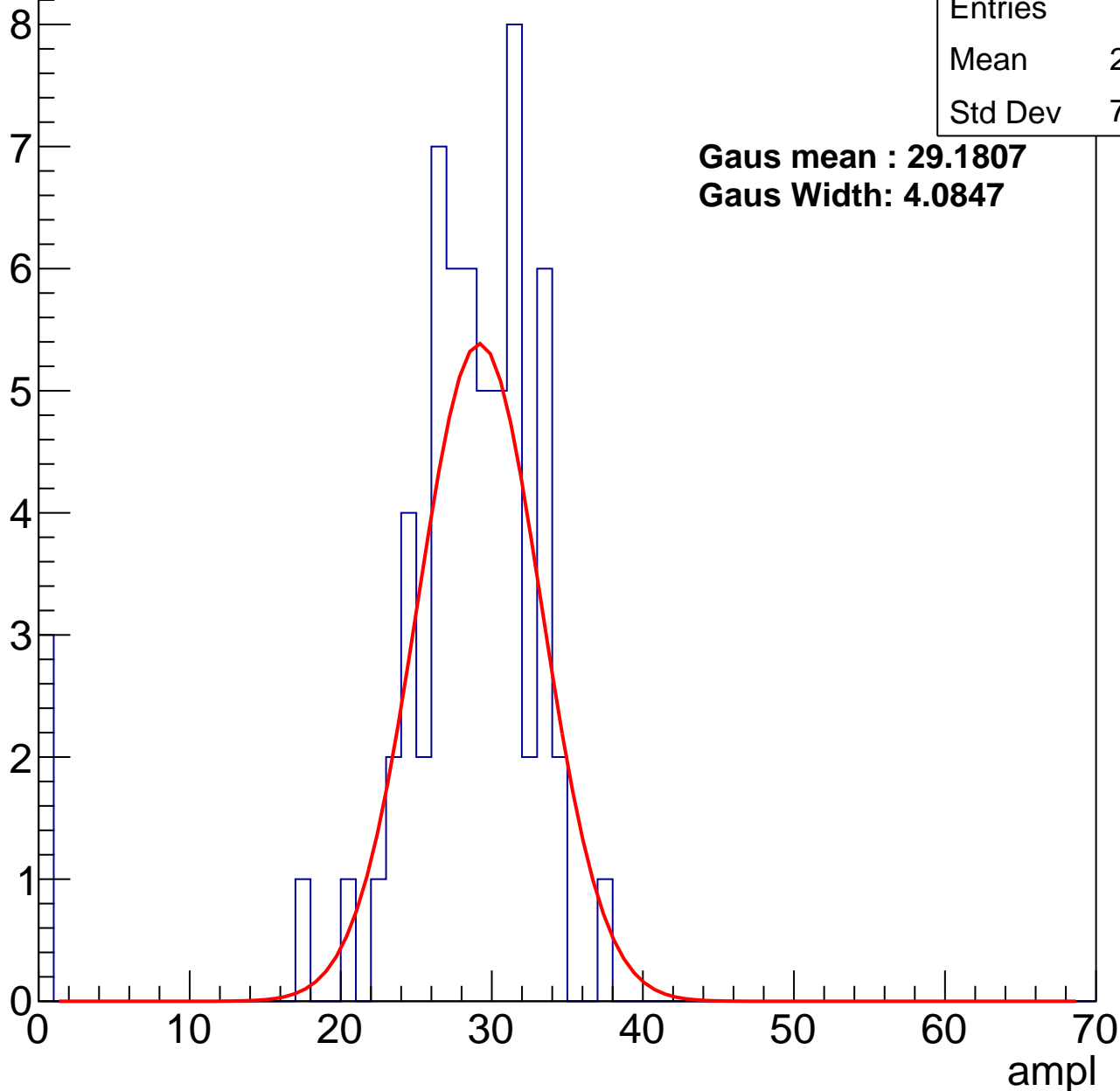
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	26.98
Std Dev	7.079

**Gaus mean : 29.1807**

**Gaus Width: 4.0847**



# B1L101S, U3-ch84, adc1

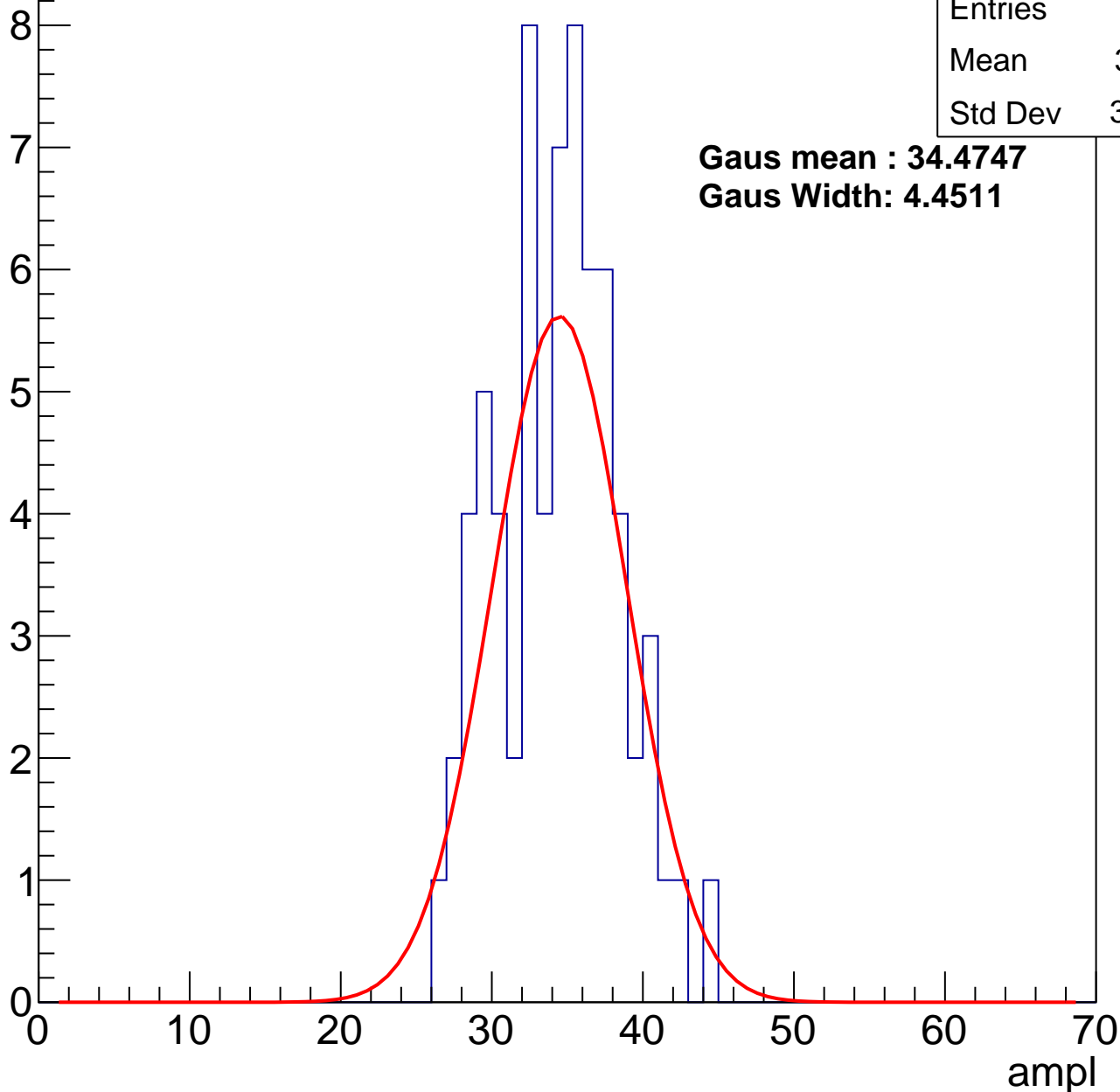
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	33.91
Std Dev	3.937

**Gaus mean : 34.4747**

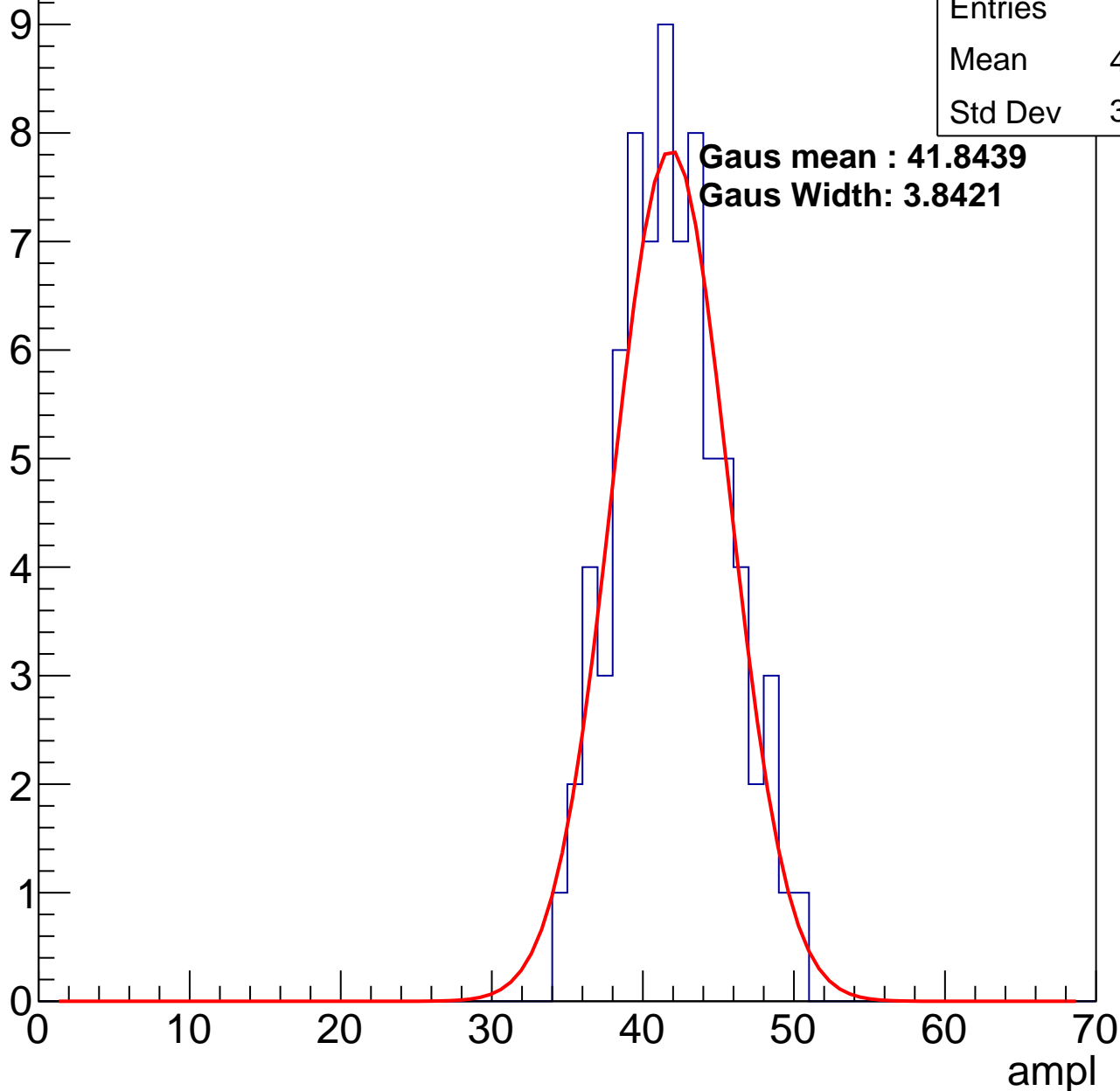
**Gaus Width: 4.4511**



# B1L101S, U3-ch84, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

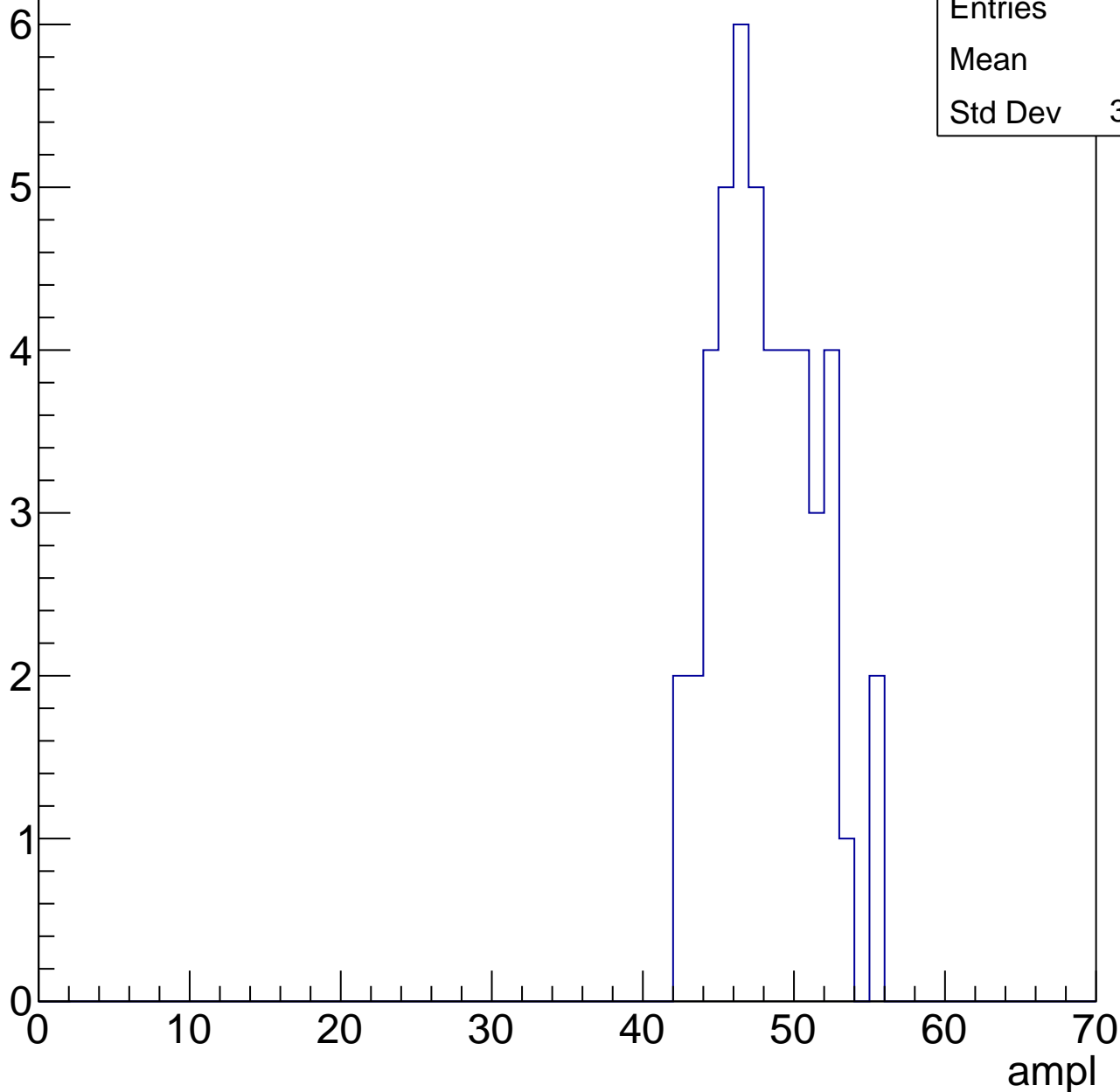


# B1L101S, U3-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	47.7
Std Dev	3.263

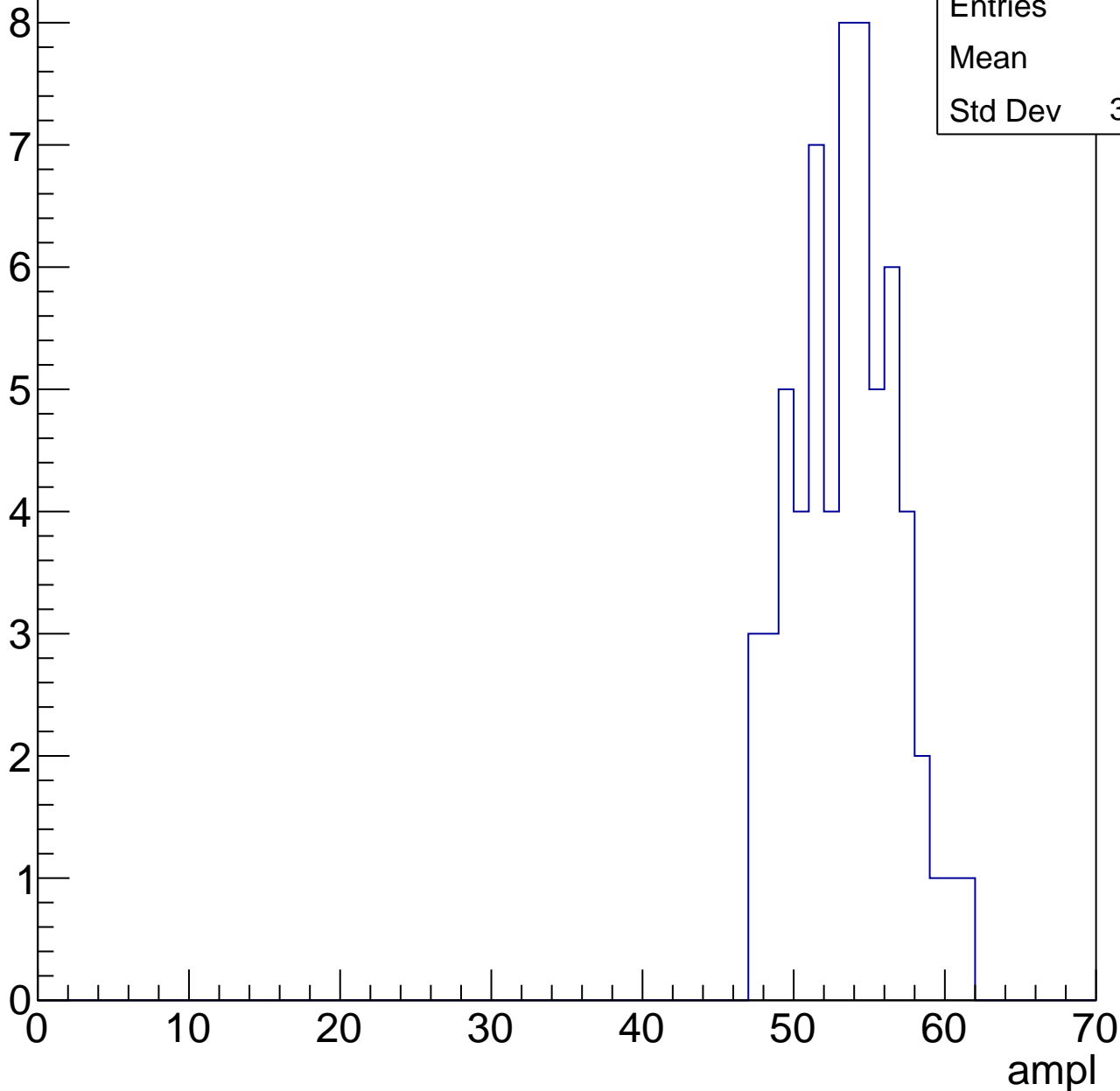


# B1L101S, U3-ch84, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

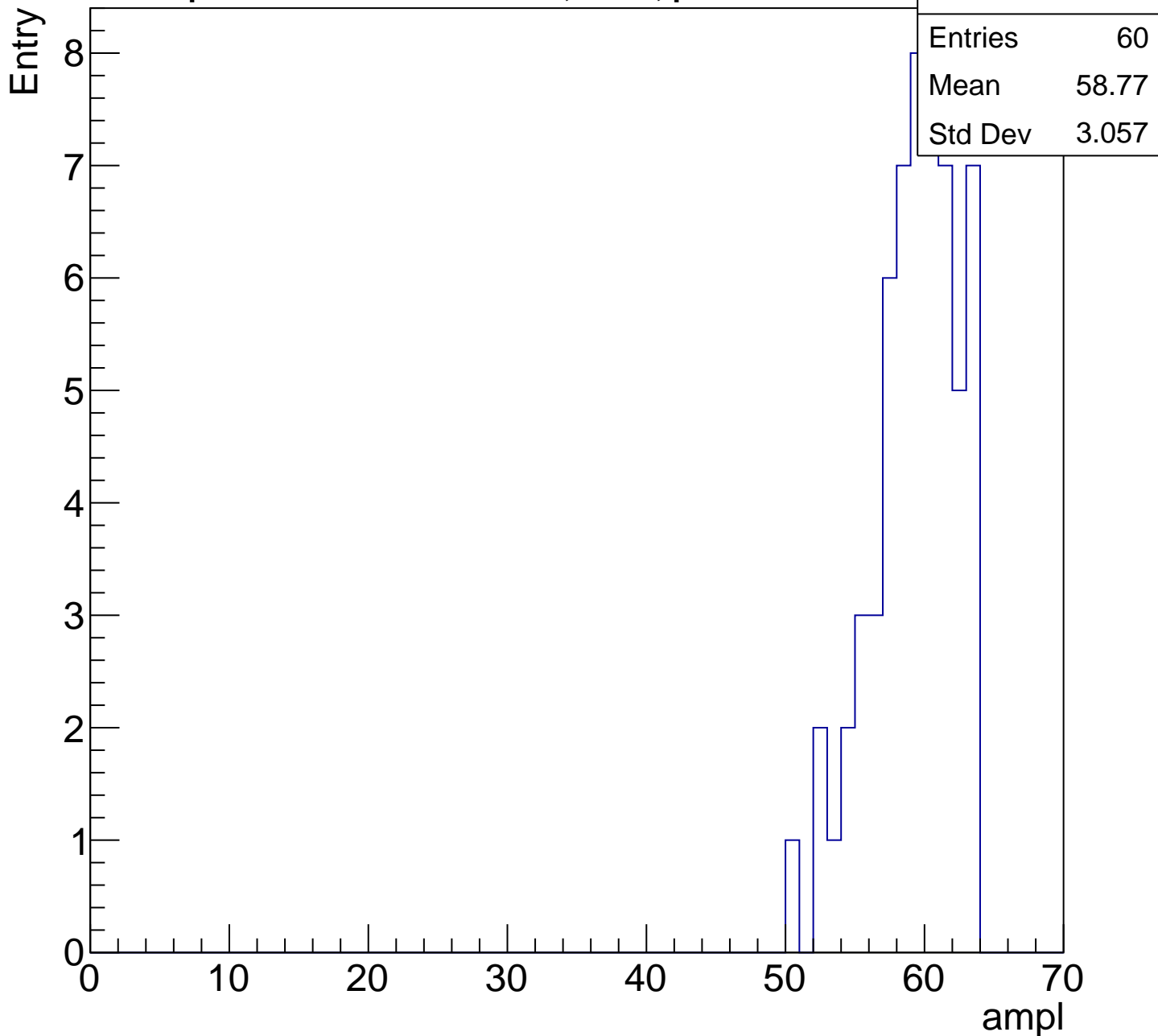
Entry

Entries	62
Mean	53
Std Dev	3.302



# B1L101S, U3-ch84, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

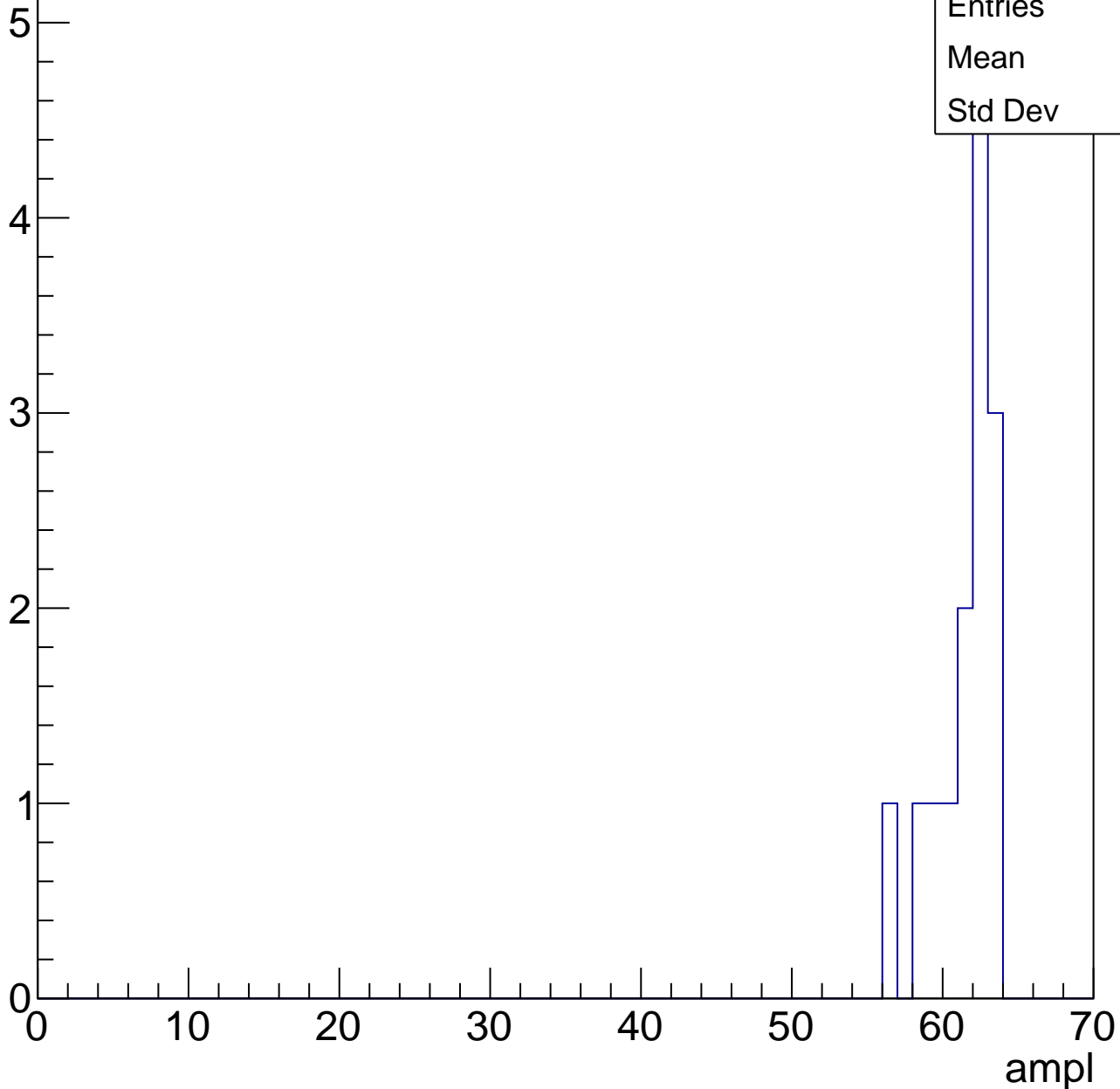


# B1L101S, U3-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	14
Mean	61
Std Dev	2





# B1L101S, U3-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L101S, U3-ch85, adc0

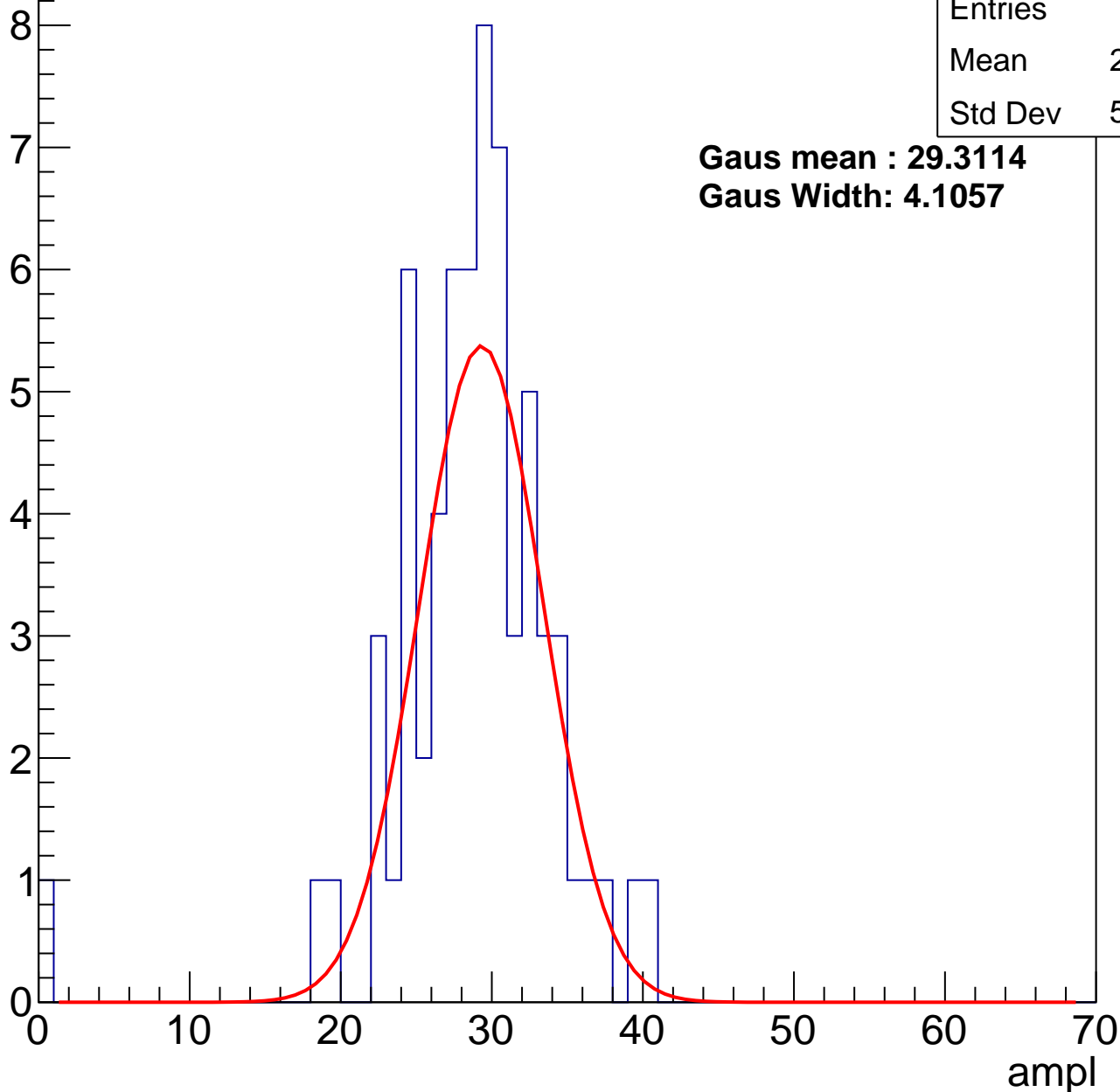
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	28.26
Std Dev	5.567

**Gaus mean : 29.3114**

**Gaus Width: 4.1057**



# B1L101S, U3-ch85, adc1

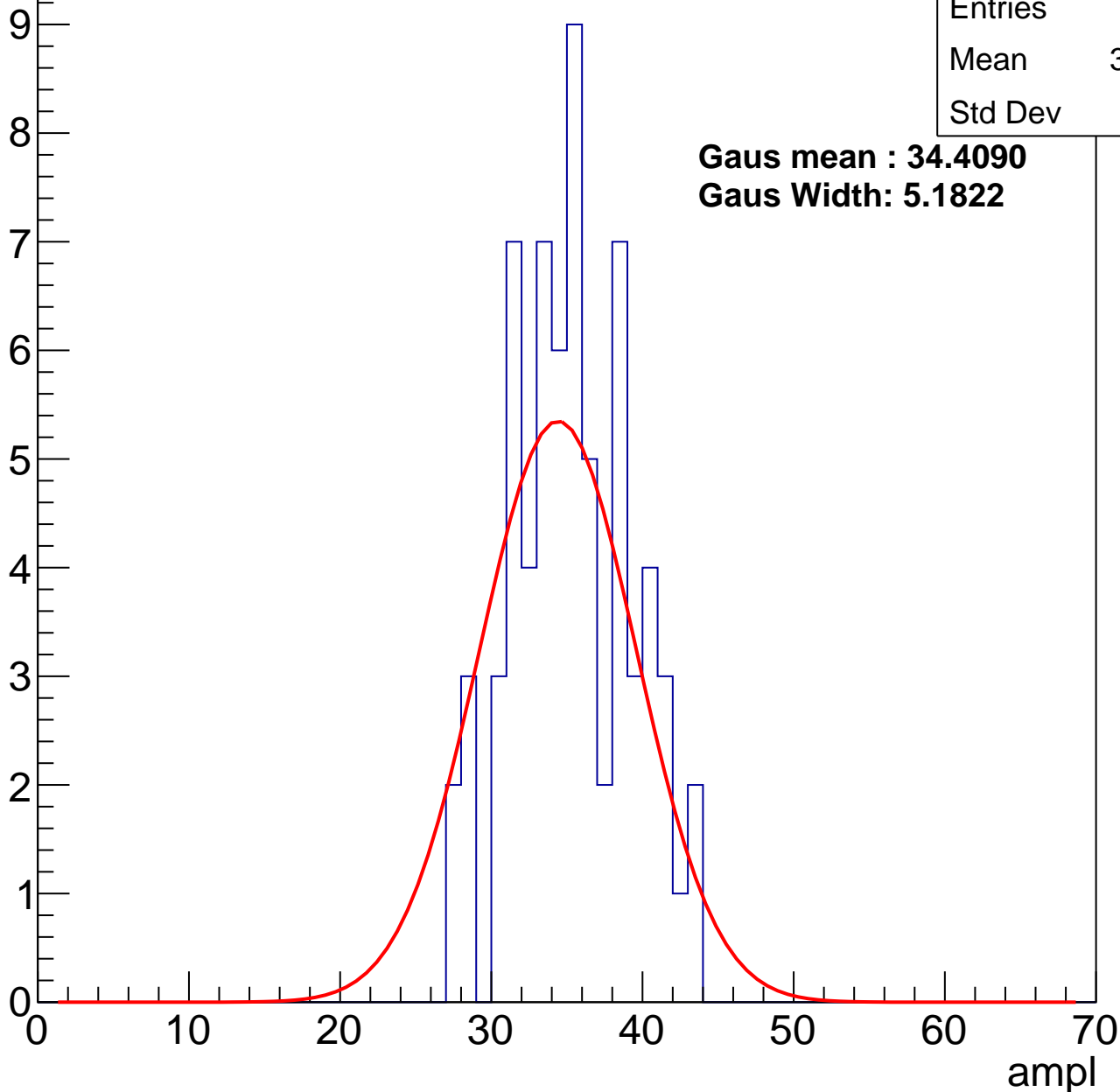
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	34.87
Std Dev	3.91

**Gaus mean : 34.4090**

**Gaus Width: 5.1822**

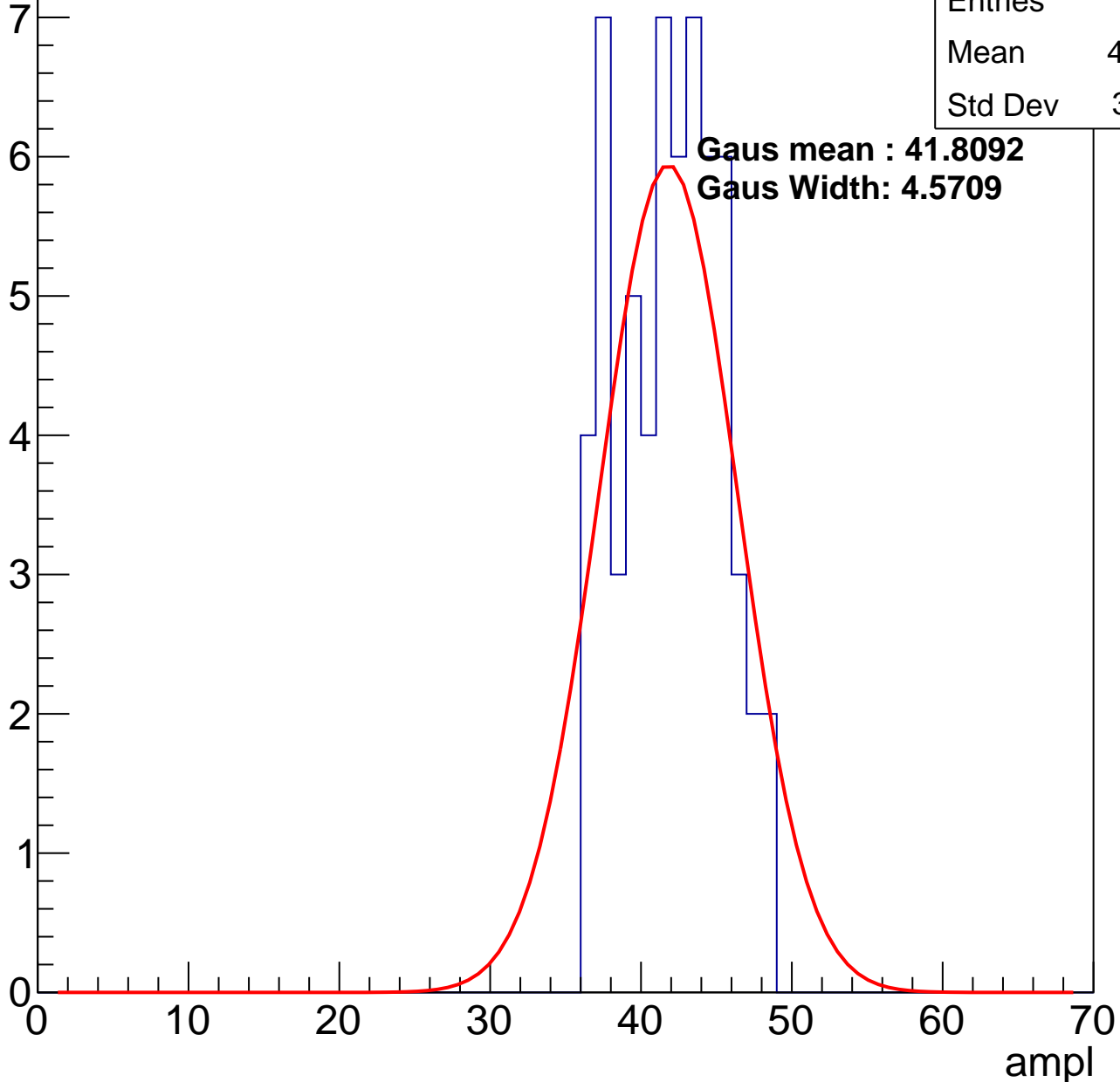


# B1L101S, U3-ch85, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	41.52
Std Dev	3.301

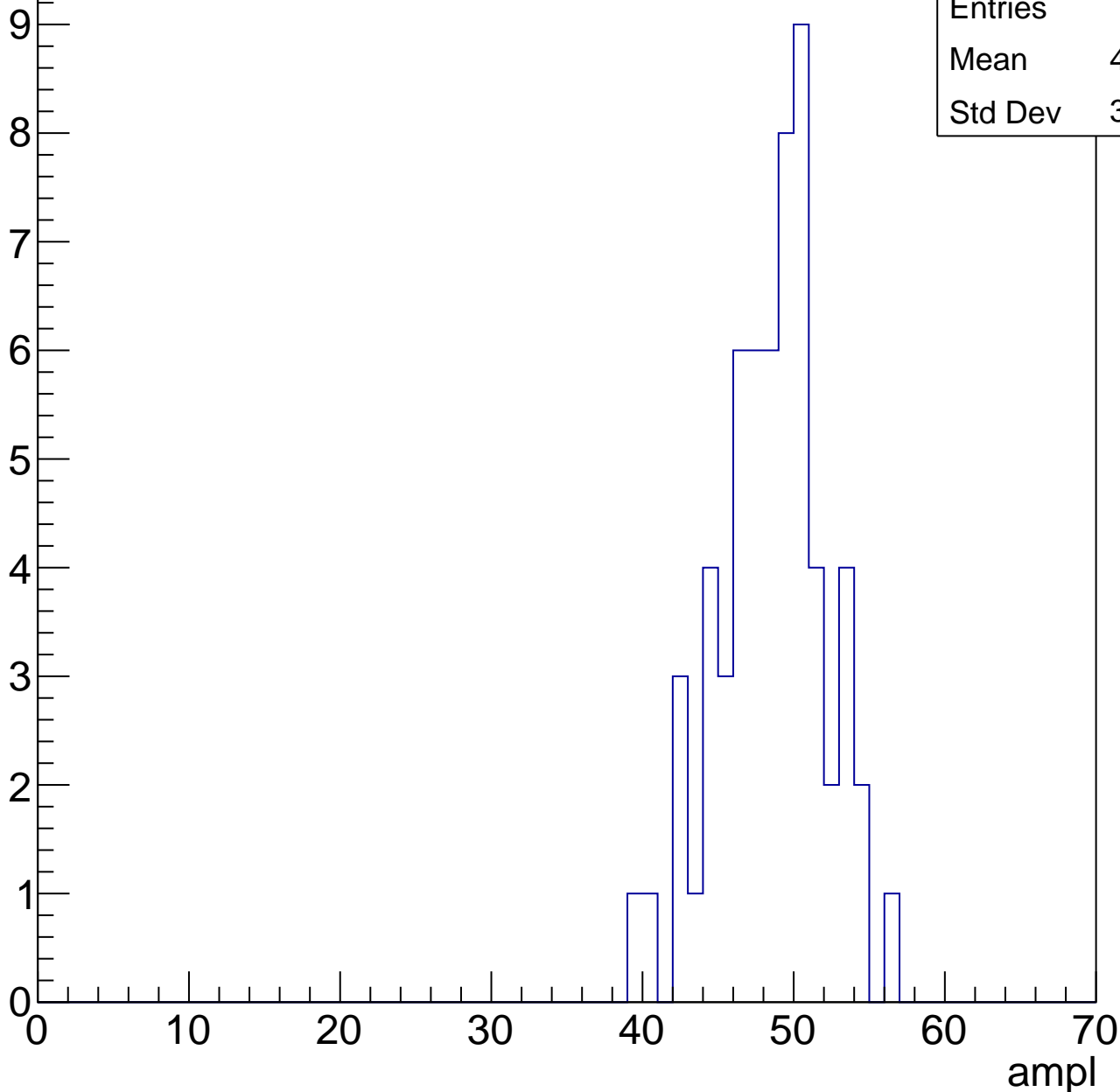


# B1L101S, U3-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	48.05
Std Dev	3.499

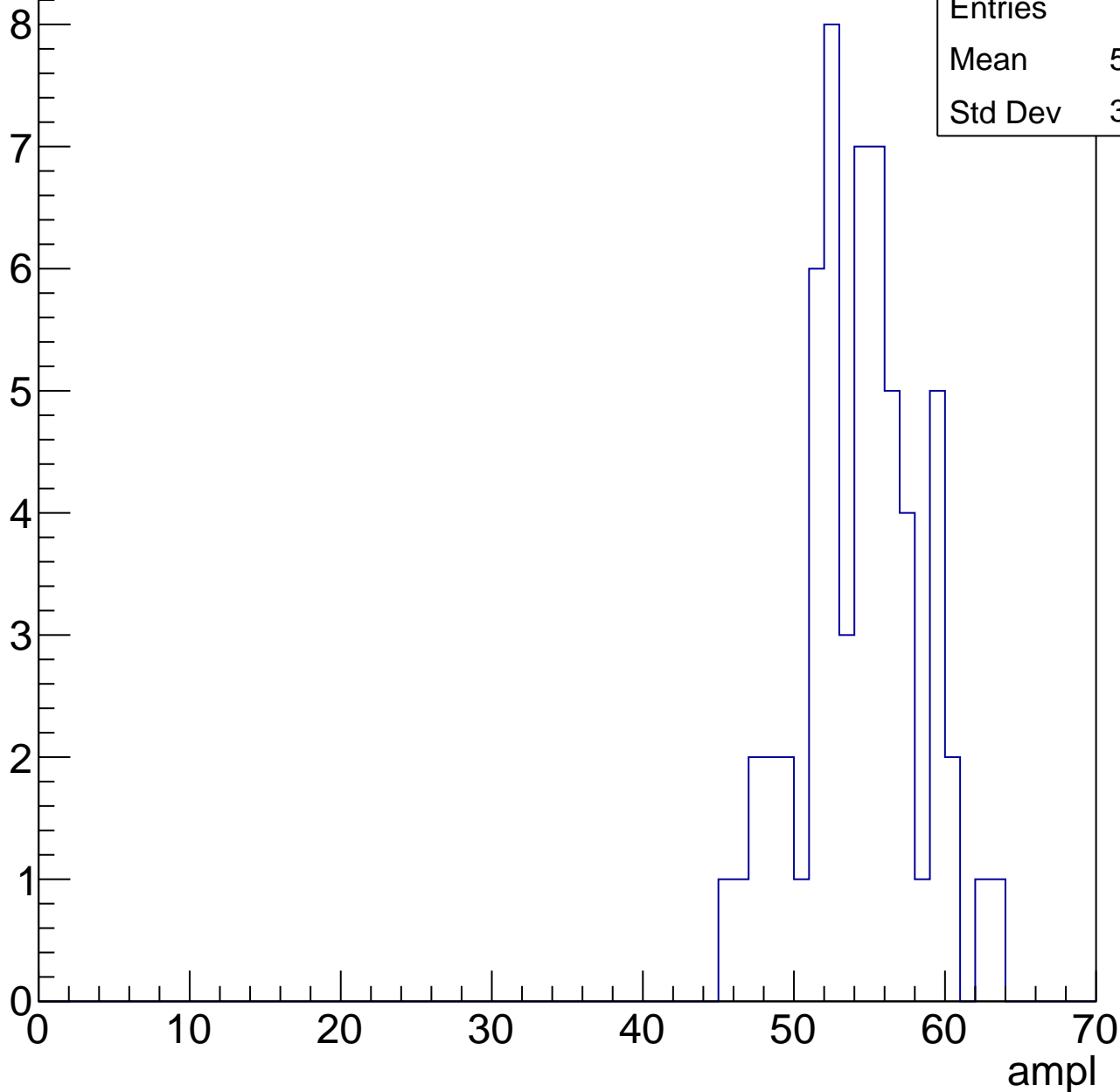


# B1L101S, U3-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	53.88
Std Dev	3.884

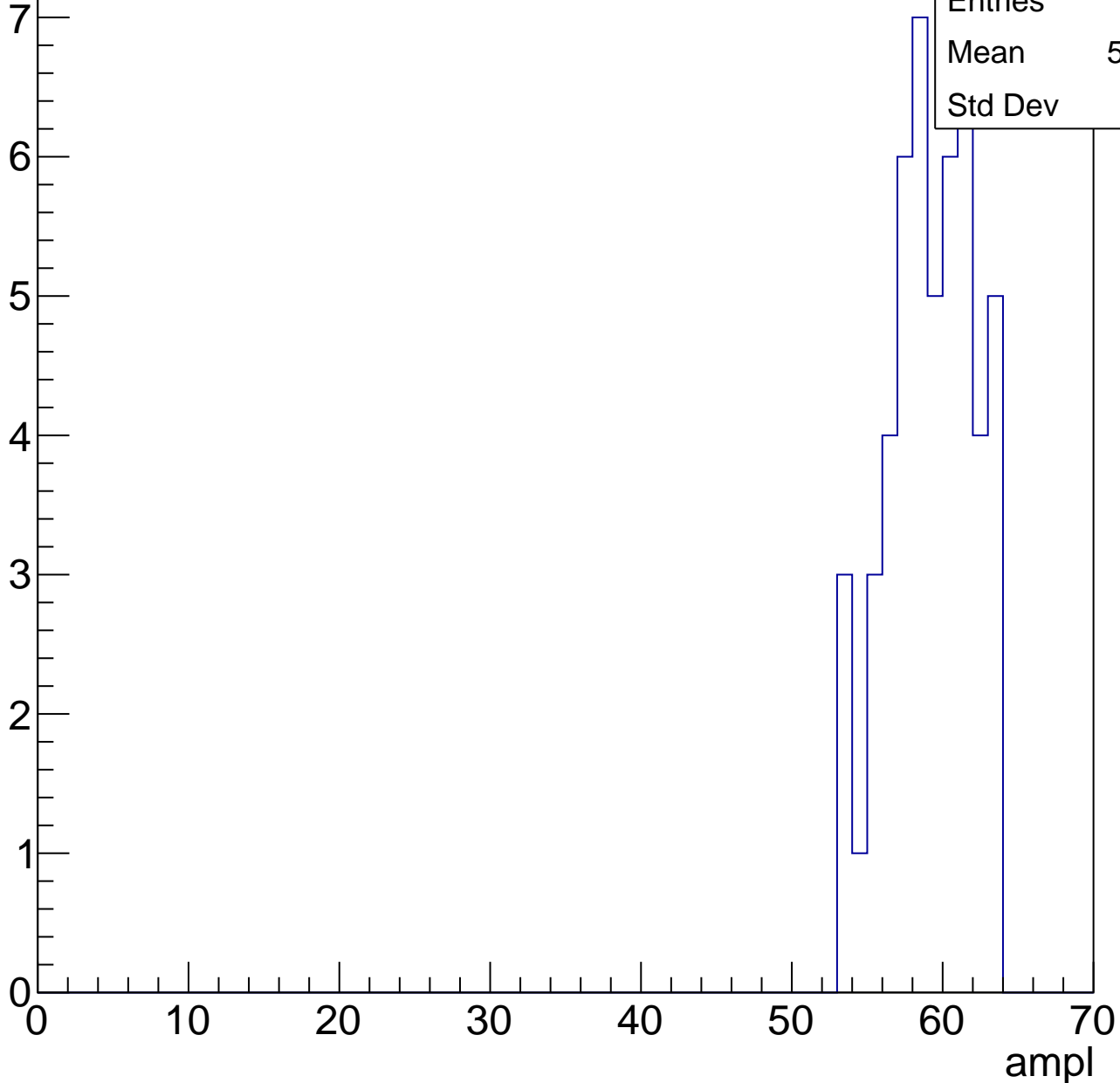


# B1L101S, U3-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	58.73
Std Dev	2.78

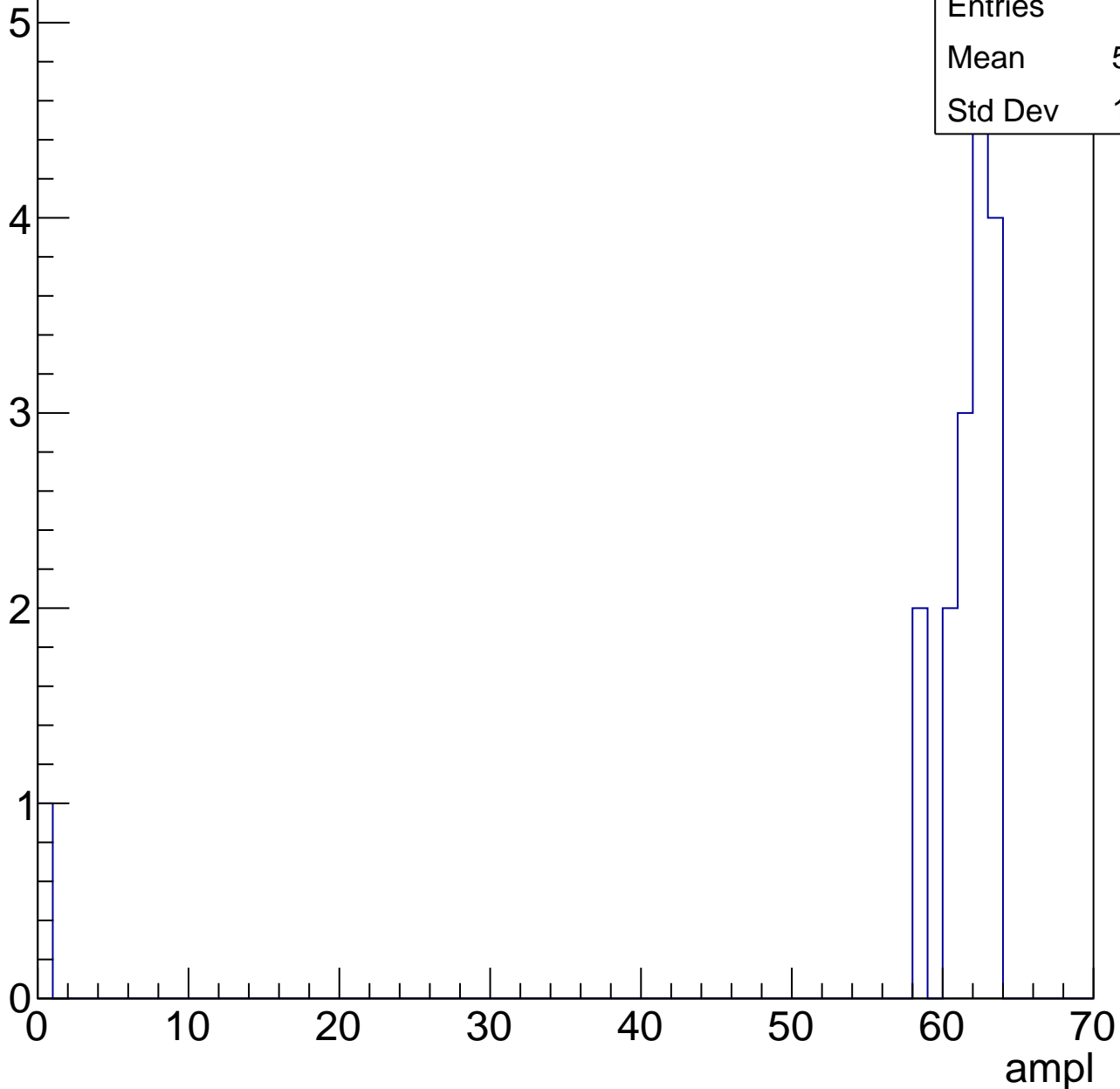


# B1L101S, U3-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	17
Mean	57.71
Std Dev	14.51





# B1L101S, U3-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U3-ch86, adc0

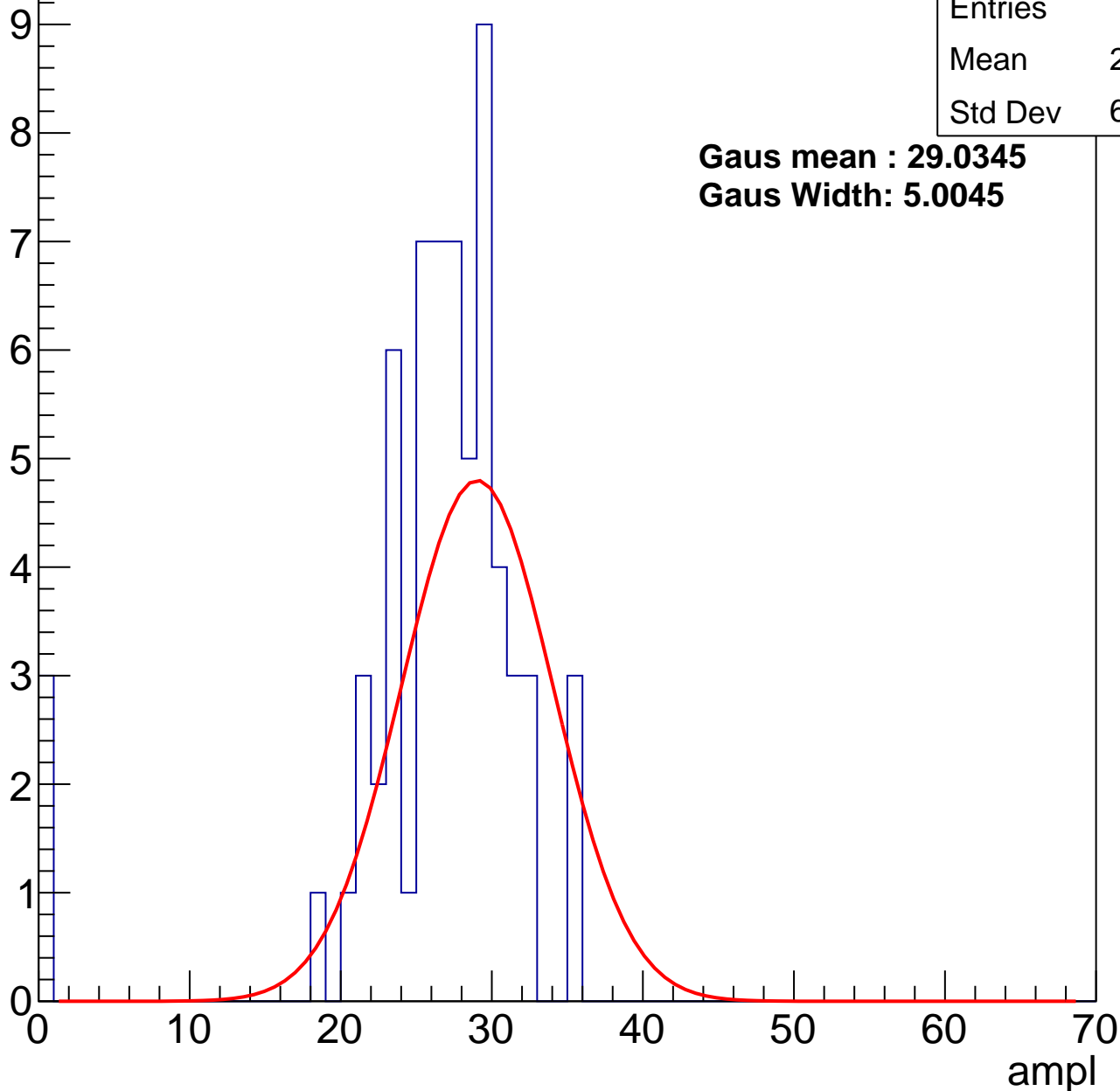
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	25.66
Std Dev	6.669

**Gaus mean : 29.0345**

**Gaus Width: 5.0045**



# B1L101S, U3-ch86, adc1

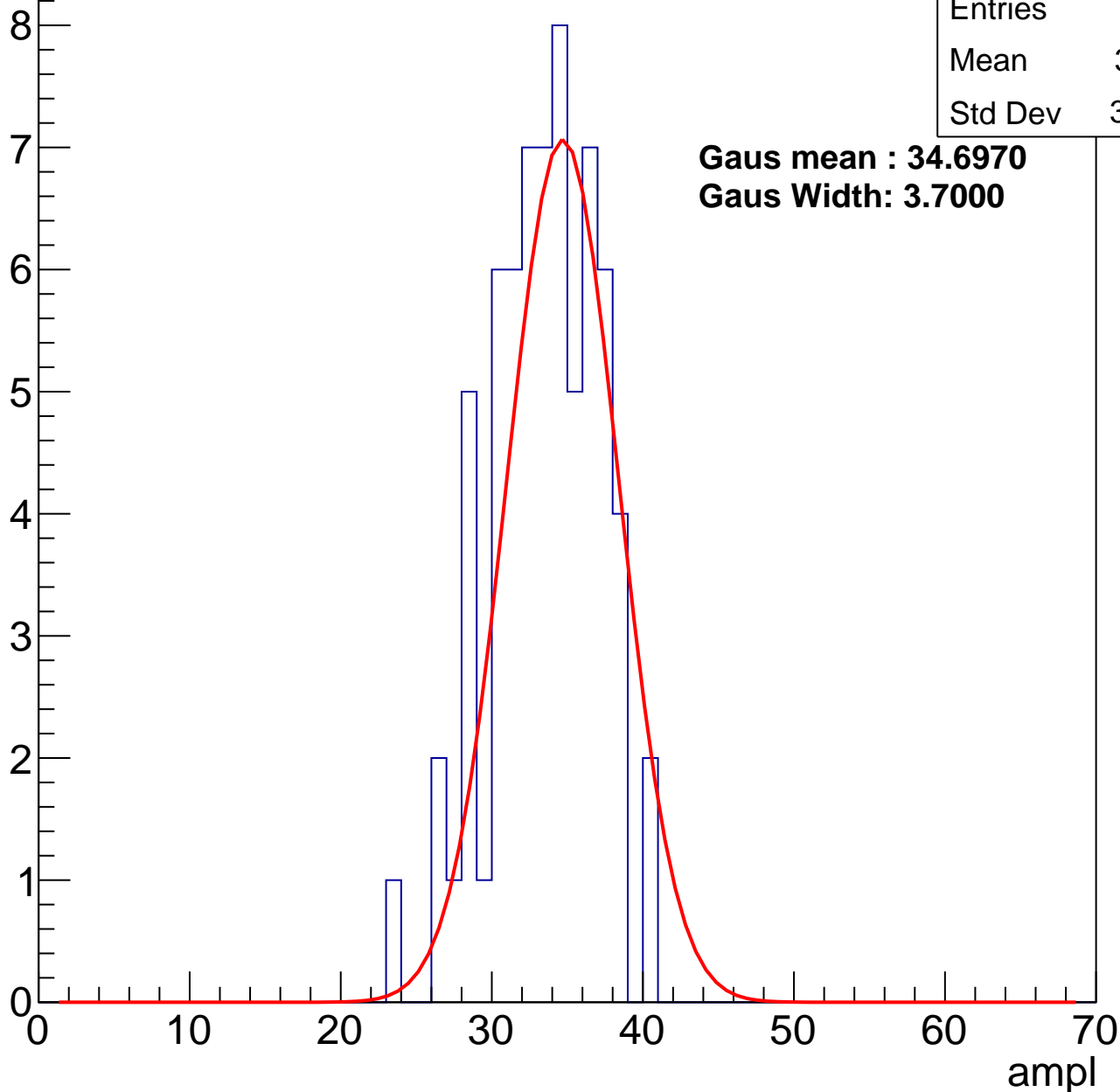
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	33.01
Std Dev	3.525

**Gaus mean : 34.6970**

**Gaus Width: 3.7000**



# B1L101S, U3-ch86, adc2

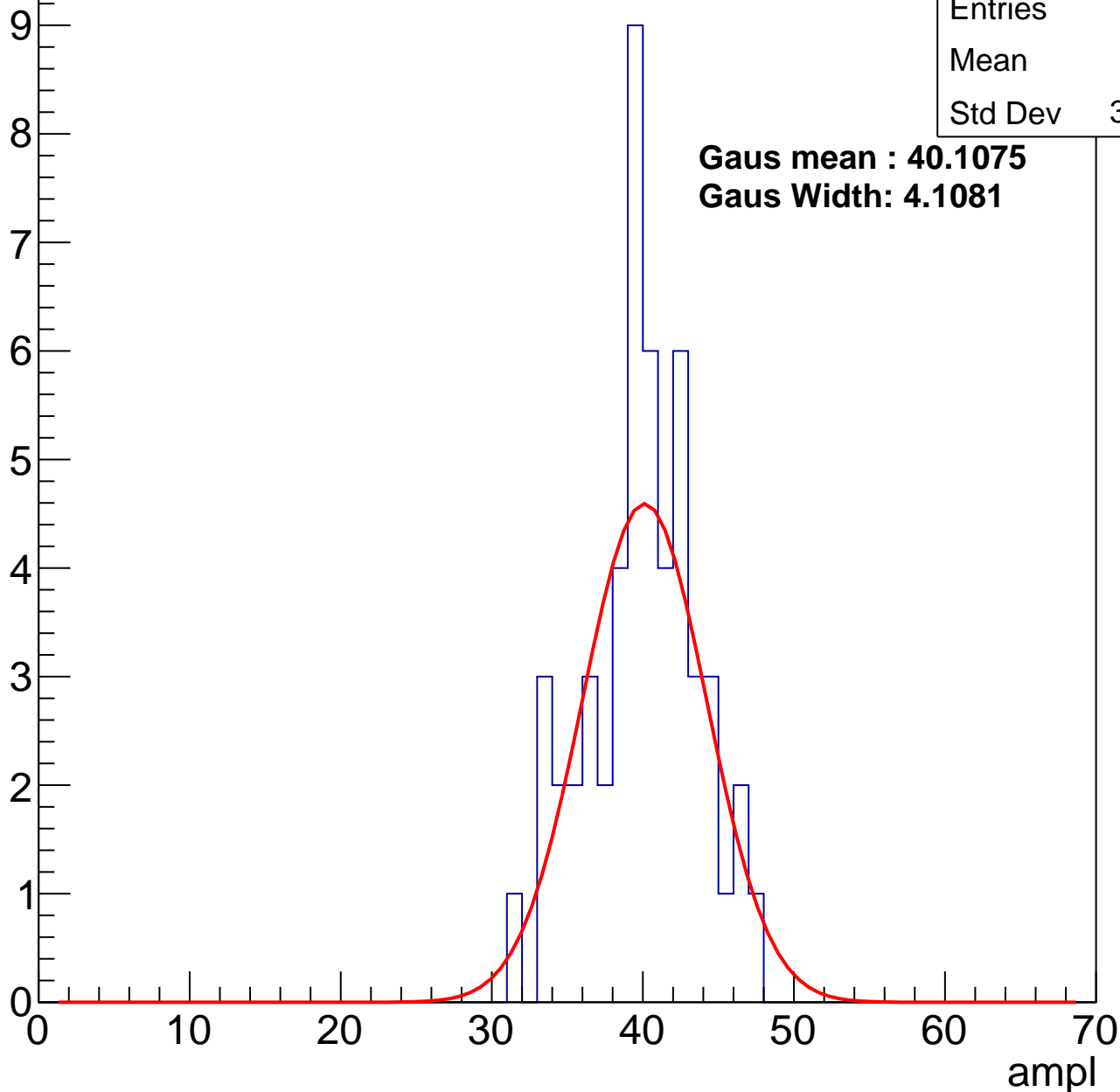
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	39.5
Std Dev	3.608

**Gaus mean : 40.1075**

**Gaus Width: 4.1081**

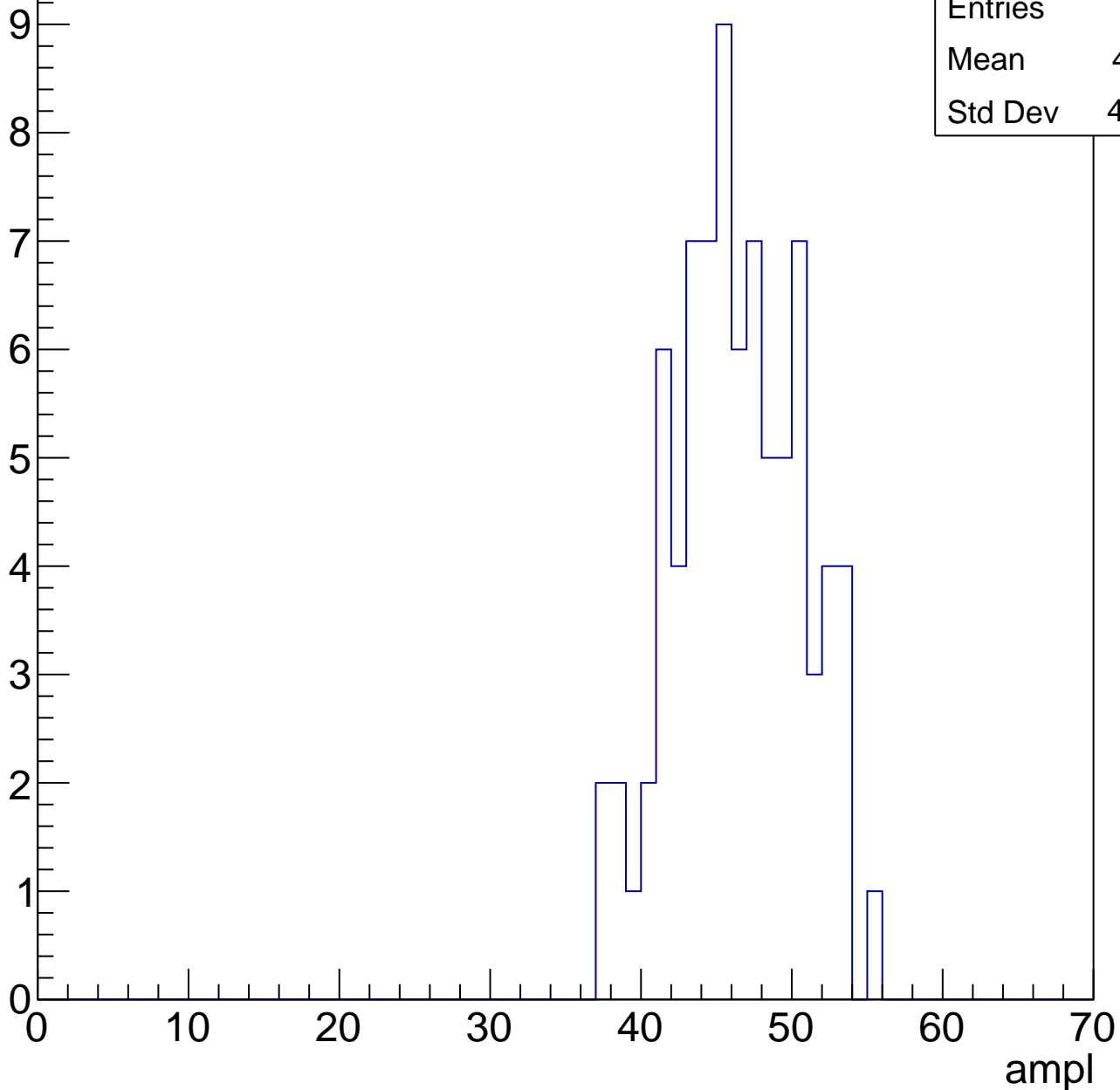


# B1L101S, U3-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	45.91
Std Dev	4.138

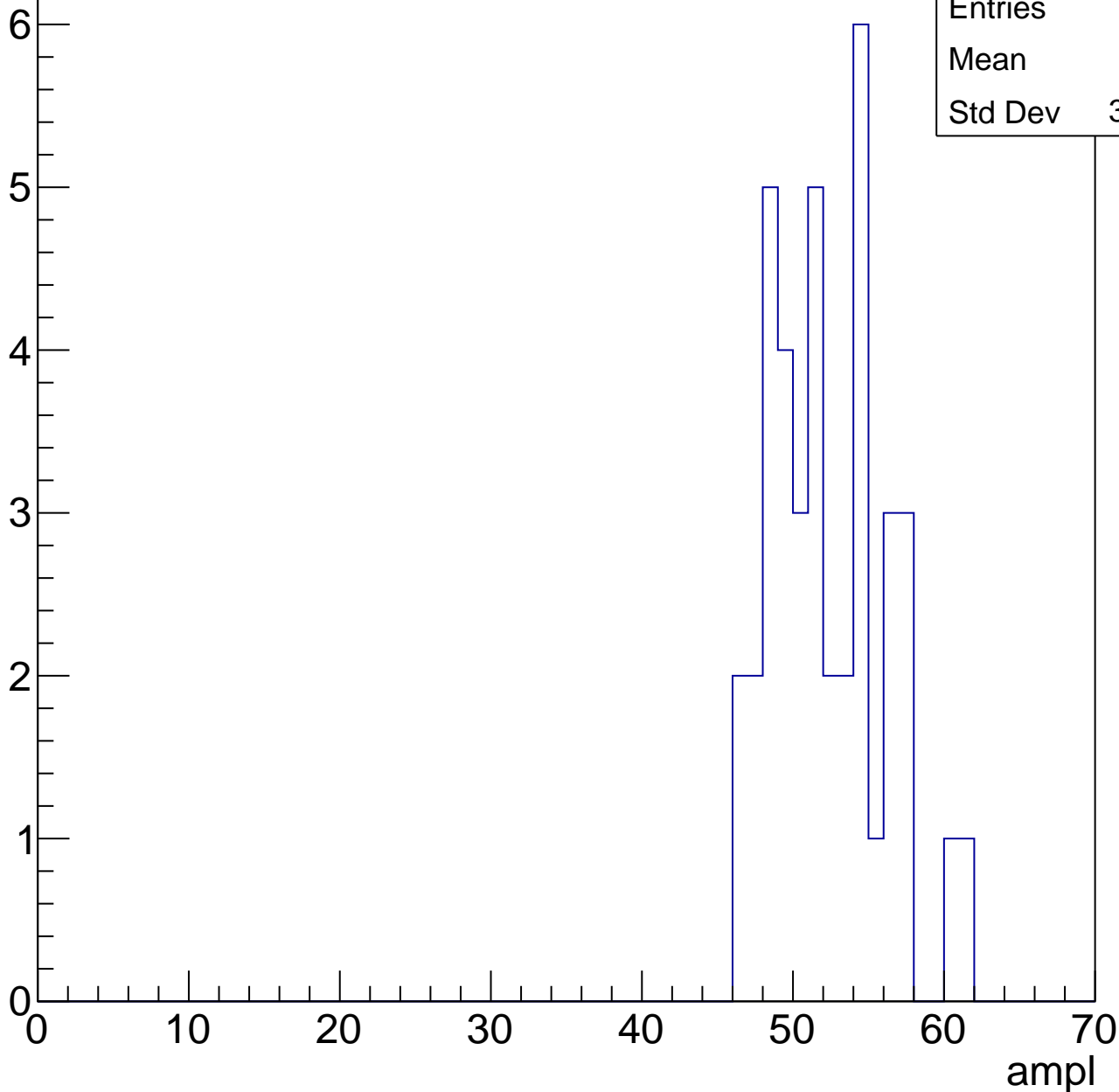


# B1L101S, U3-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

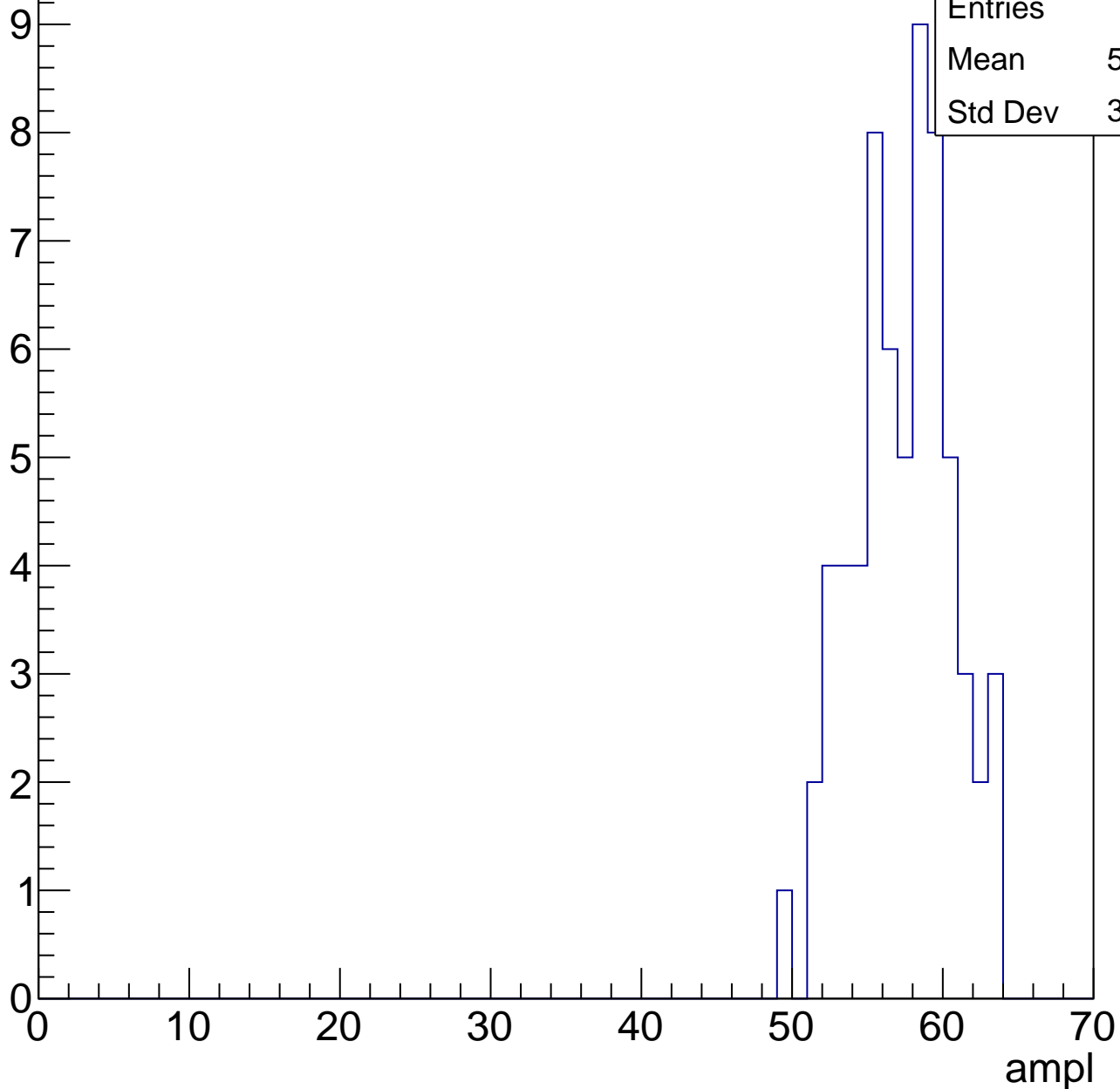
Entries	40
Mean	51.9
Std Dev	3.734



# B1L101S, U3-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



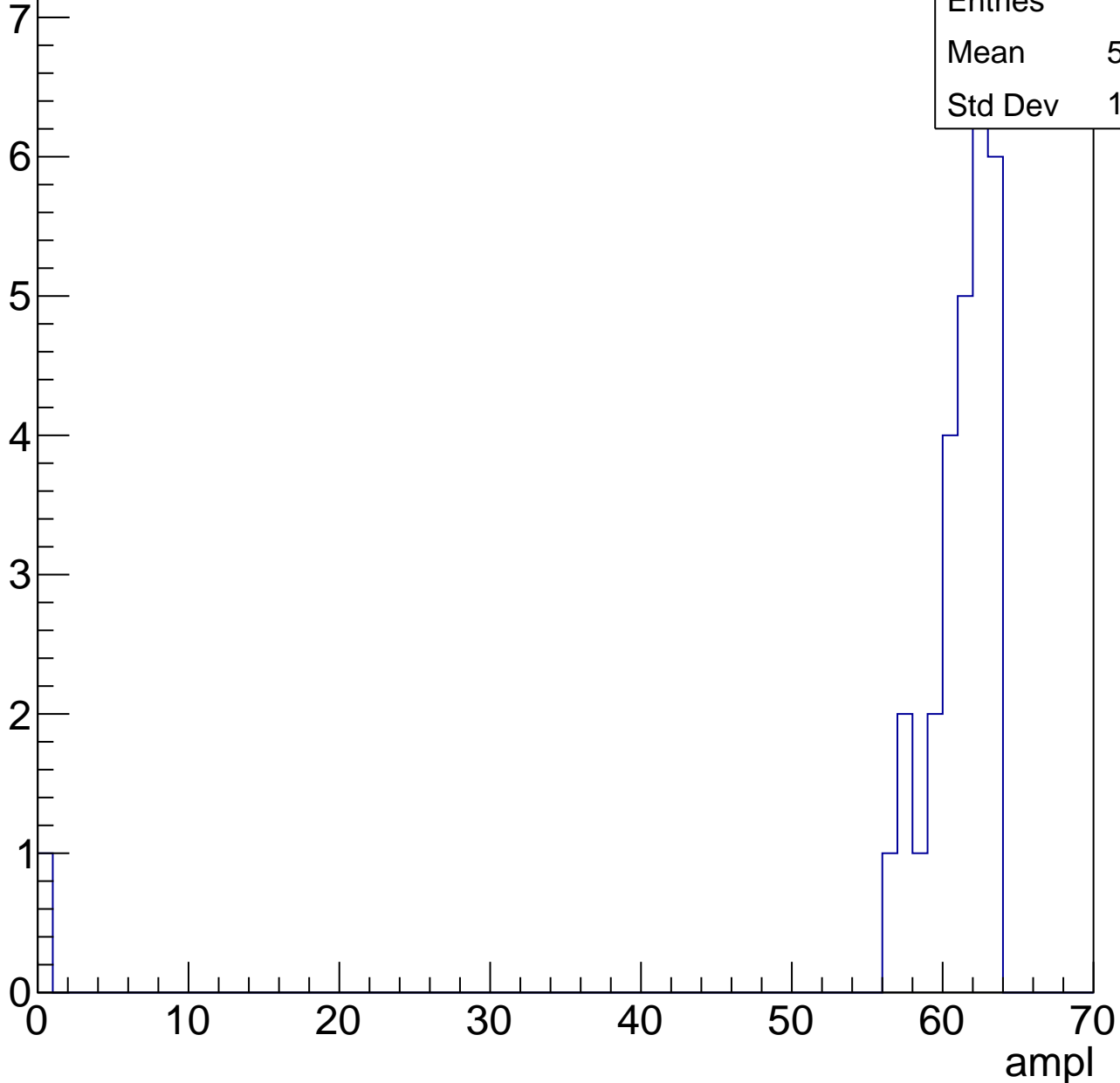
Entries	64
Mean	56.84
Std Dev	3.222

# B1L101S, U3-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	29
Mean	58.72
Std Dev	11.26

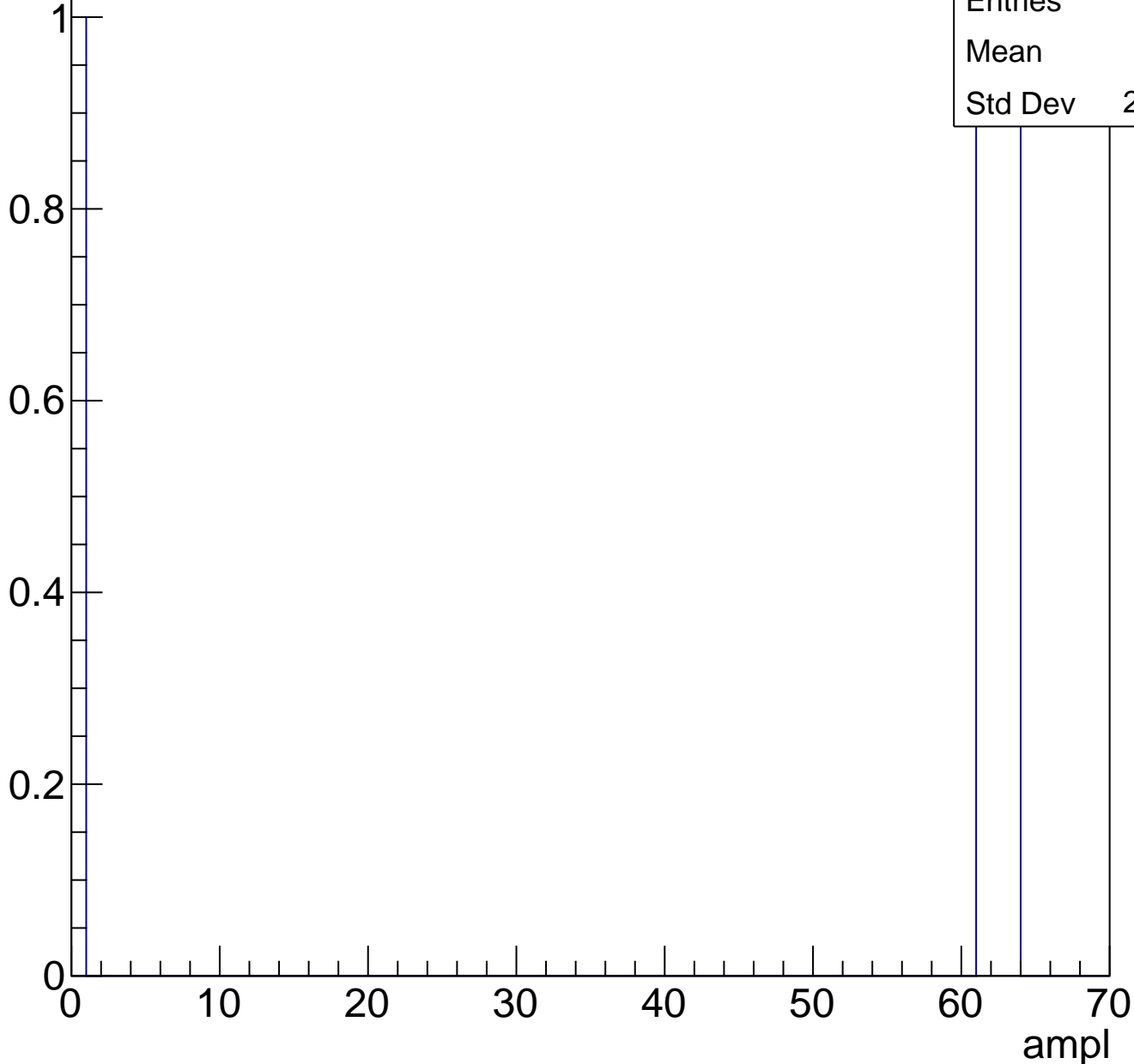




# B1L101S, U3-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch87, adc0

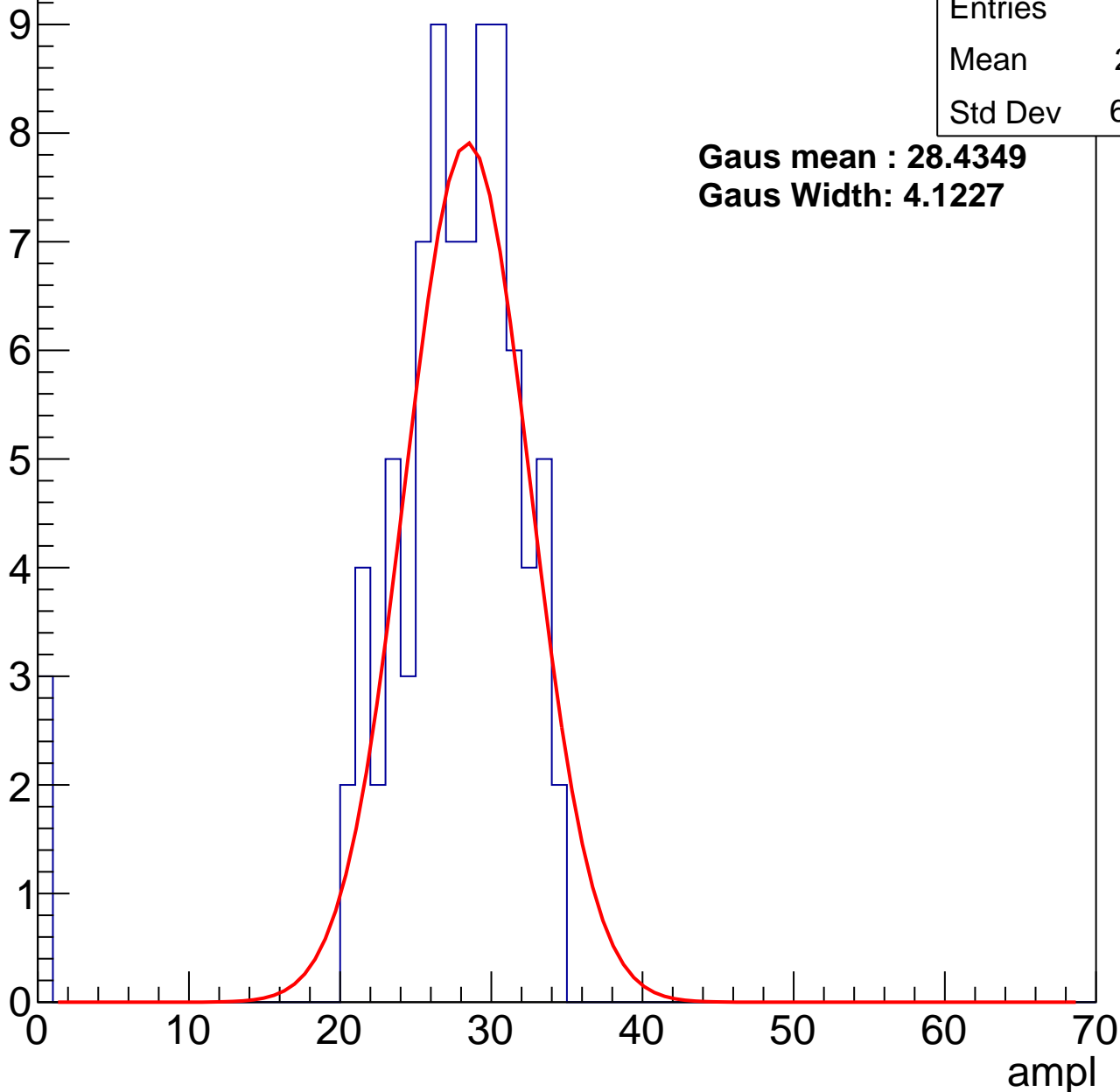
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	84
Mean	26.51
Std Dev	6.173

**Gaus mean : 28.4349**

**Gaus Width: 4.1227**



# B1L101S, U3-ch87, adc1

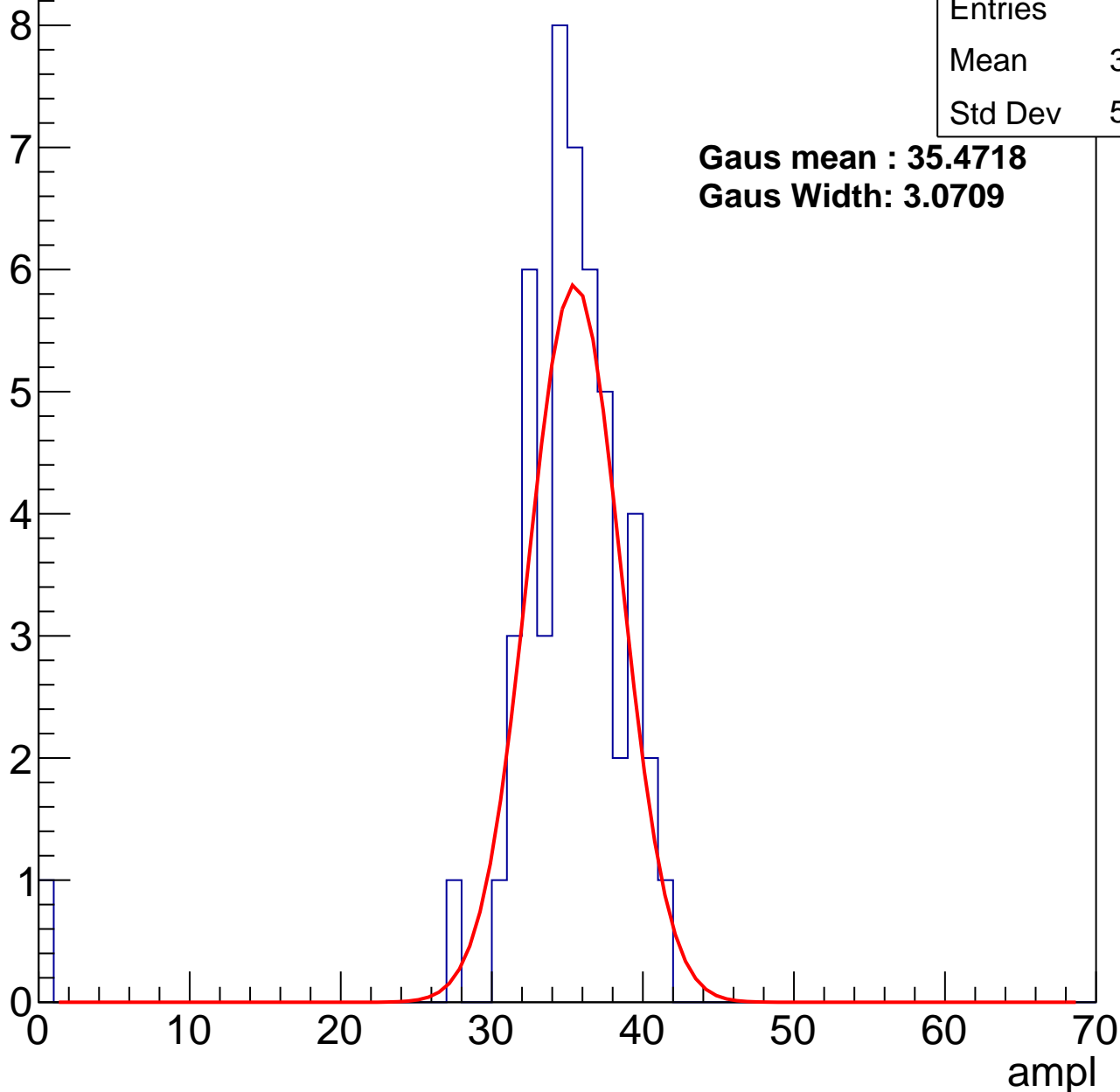
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	34.24
Std Dev	5.659

**Gaus mean : 35.4718**

**Gaus Width: 3.0709**



# B1L101S, U3-ch87, adc2

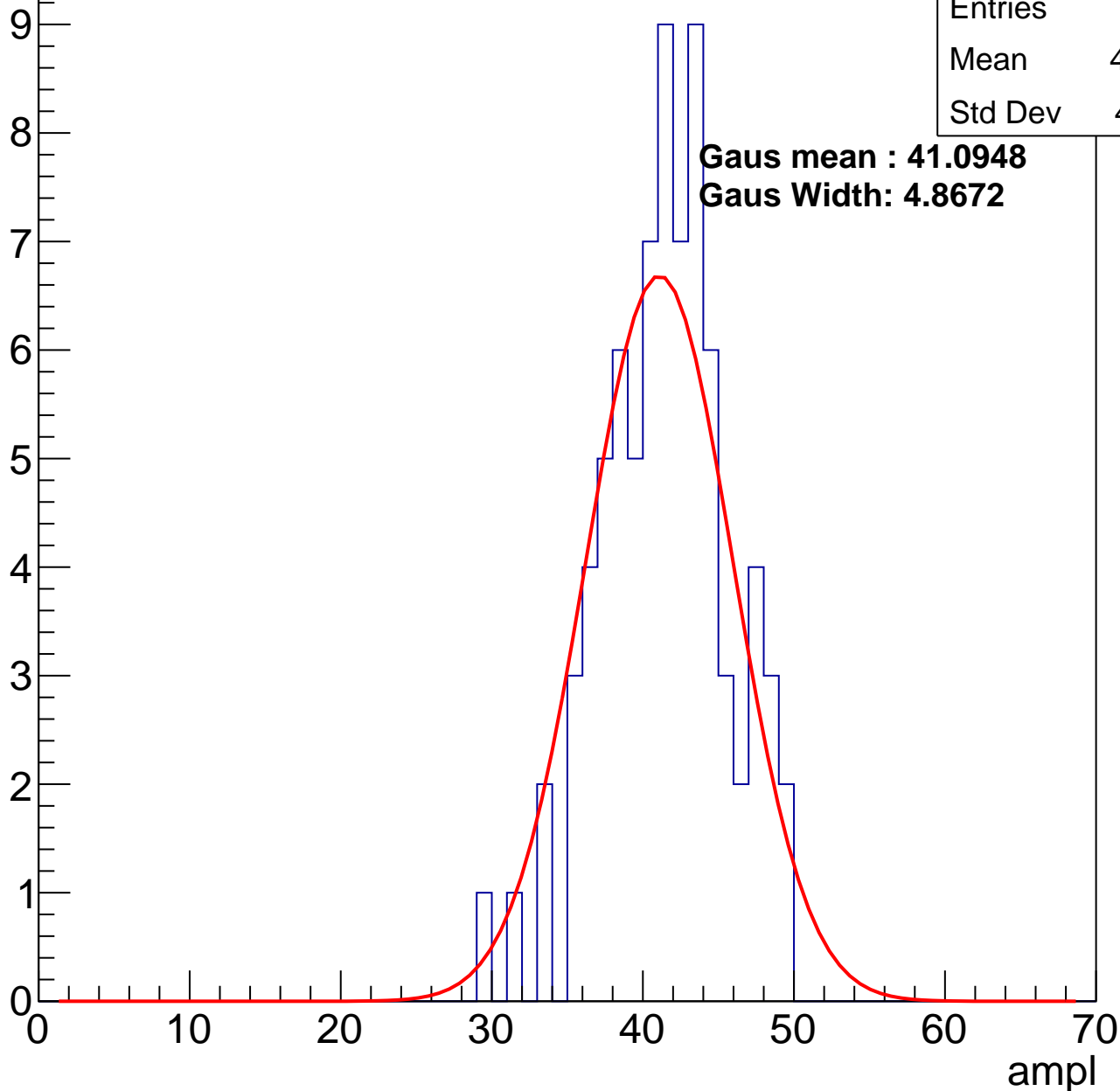
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	40.94
Std Dev	4.141

**Gaus mean : 41.0948**

**Gaus Width: 4.8672**

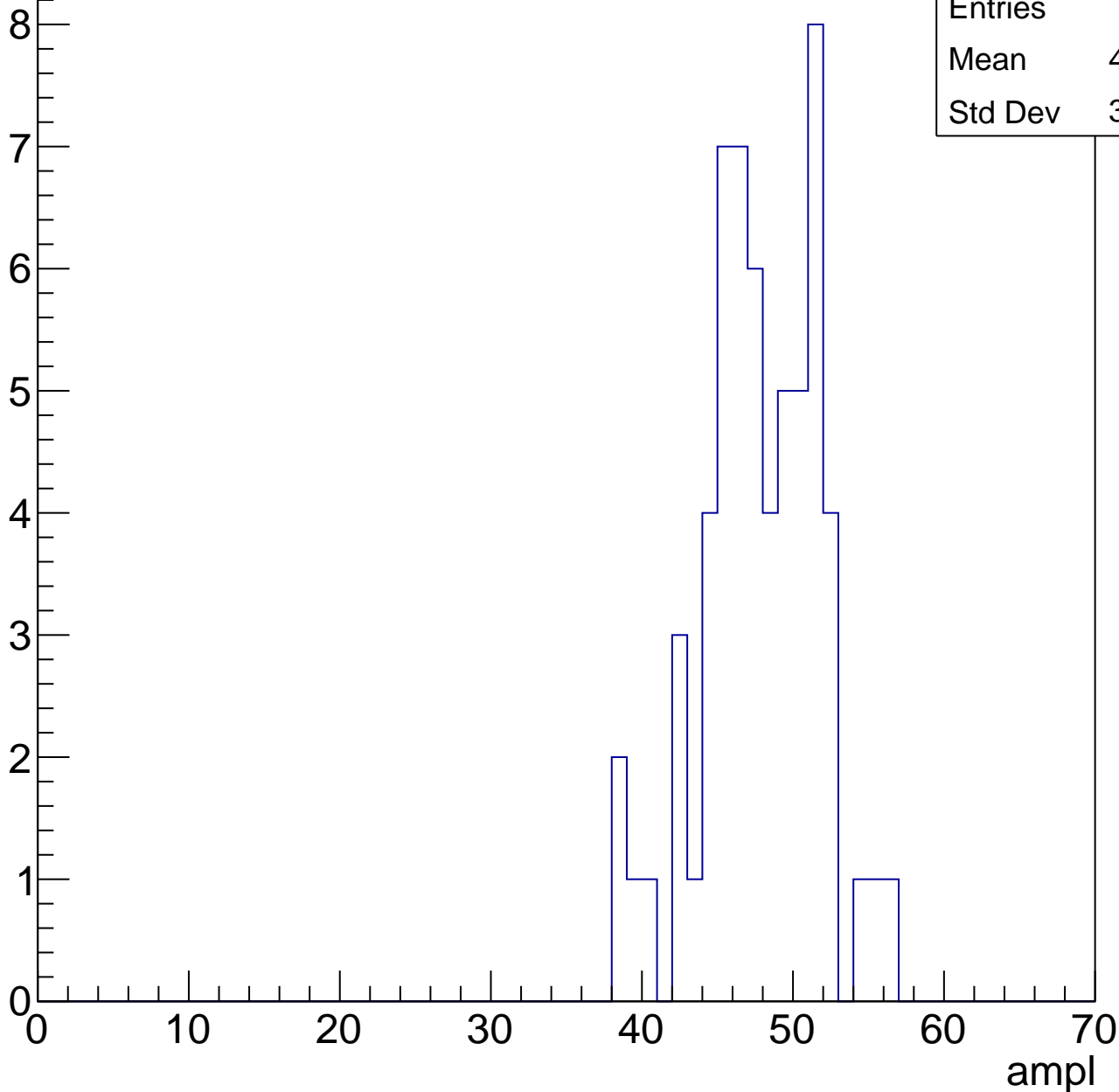


# B1L101S, U3-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	47.33
Std Dev	3.887

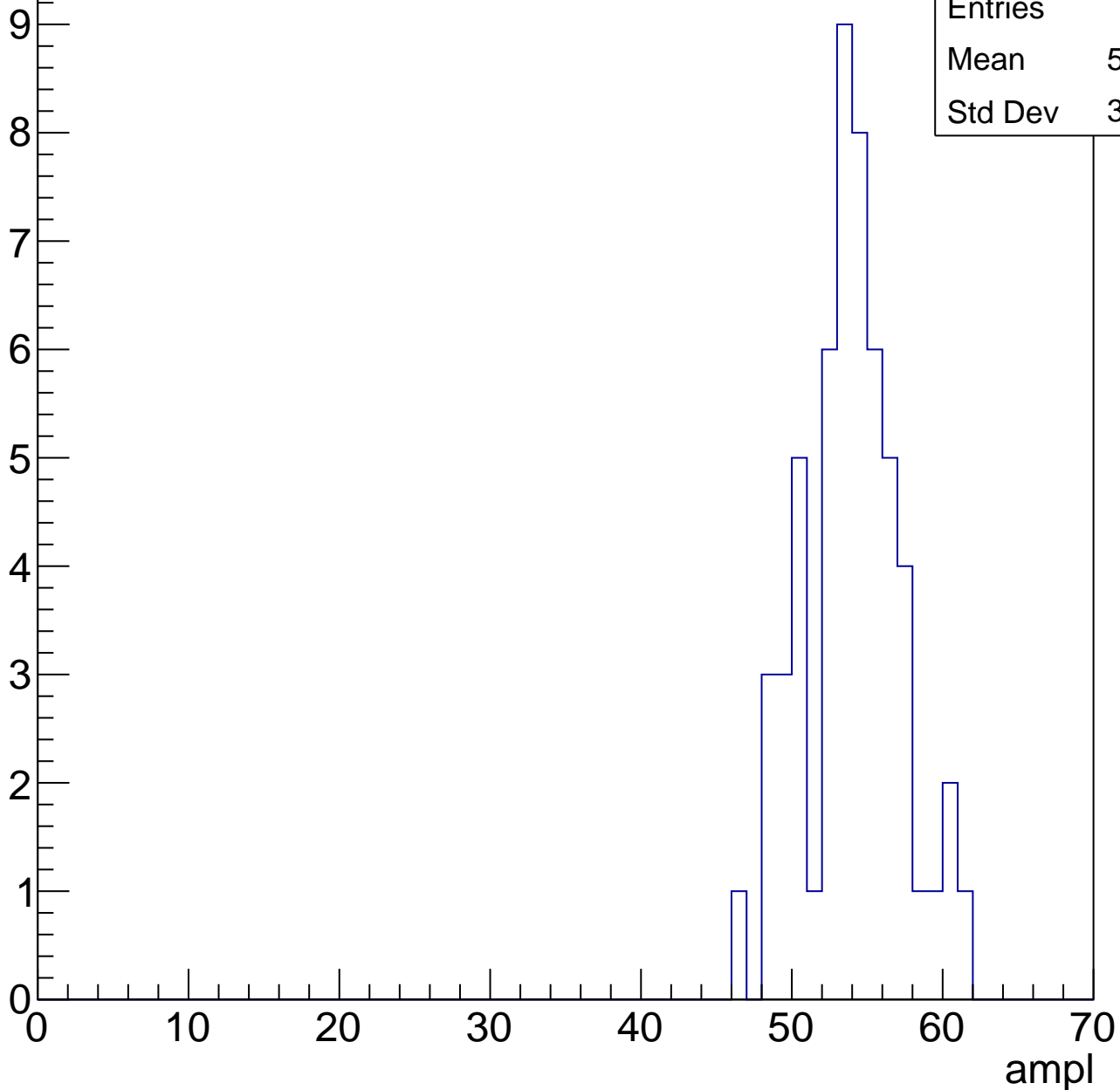


# B1L101S, U3-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

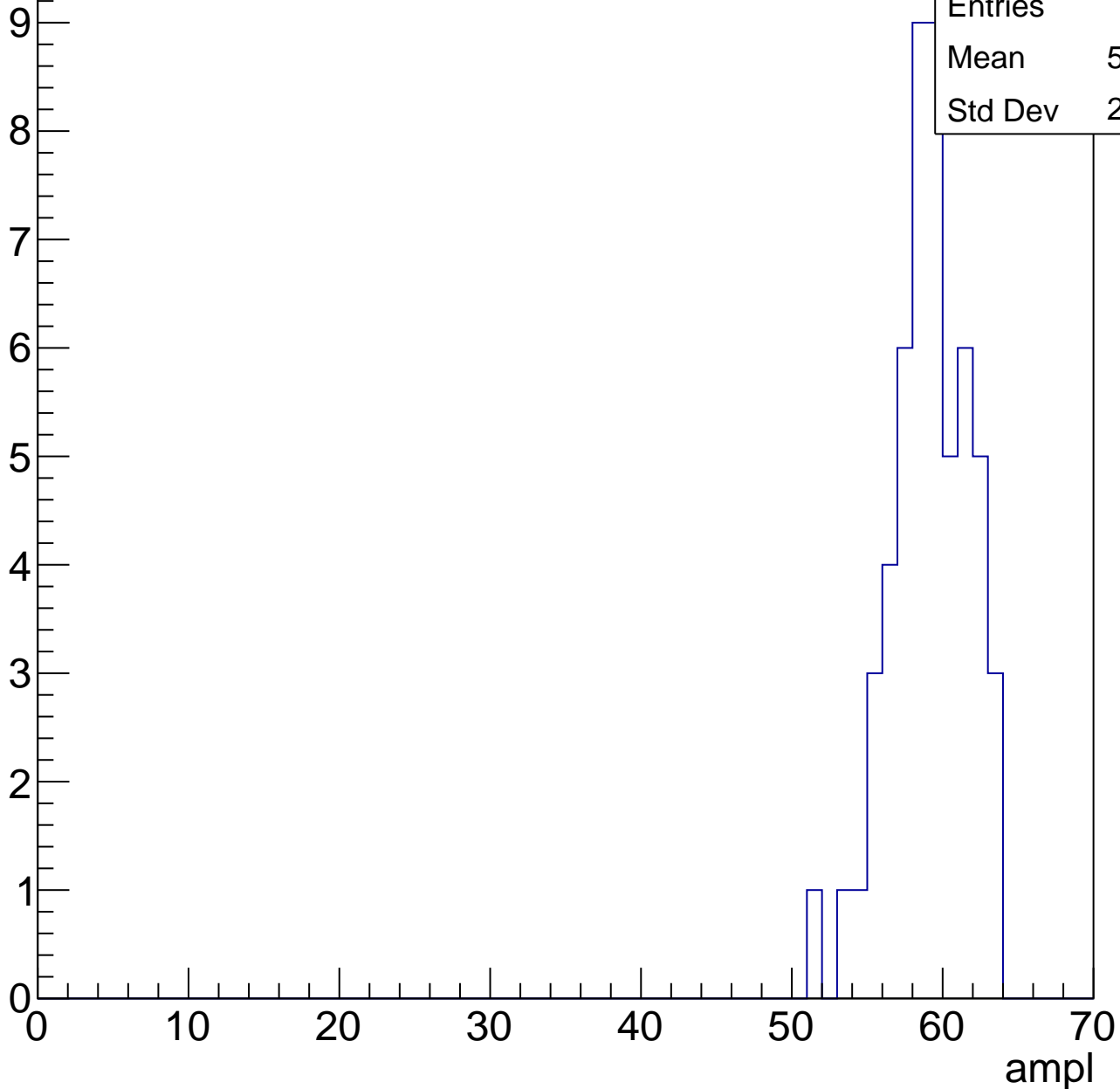
Entries	56
Mean	53.48
Std Dev	3.213



# B1L101S, U3-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

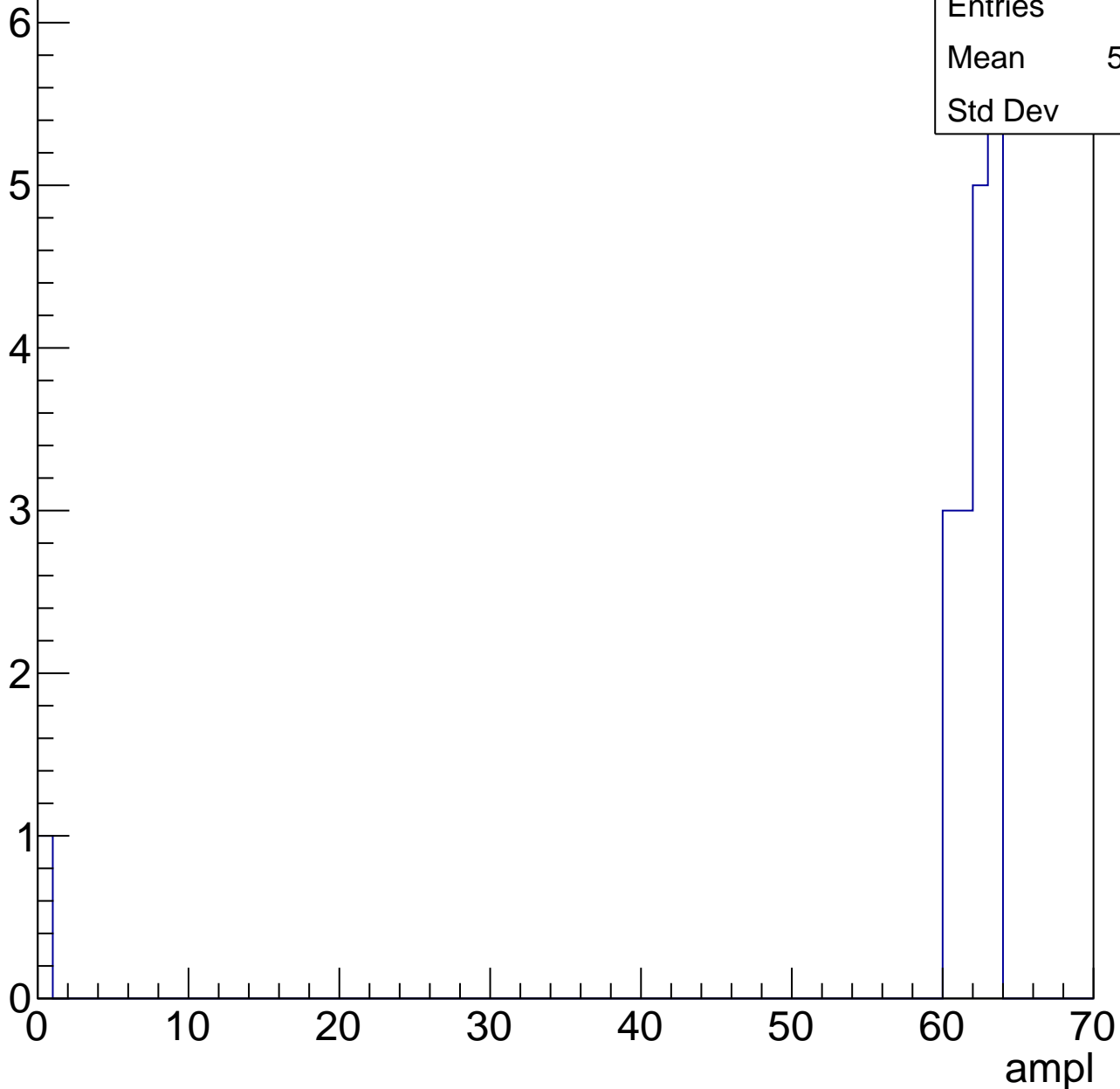


# B1L101S, U3-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	18
Mean	58.39
Std Dev	14.2





# B1L101S, U3-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch88, adc0

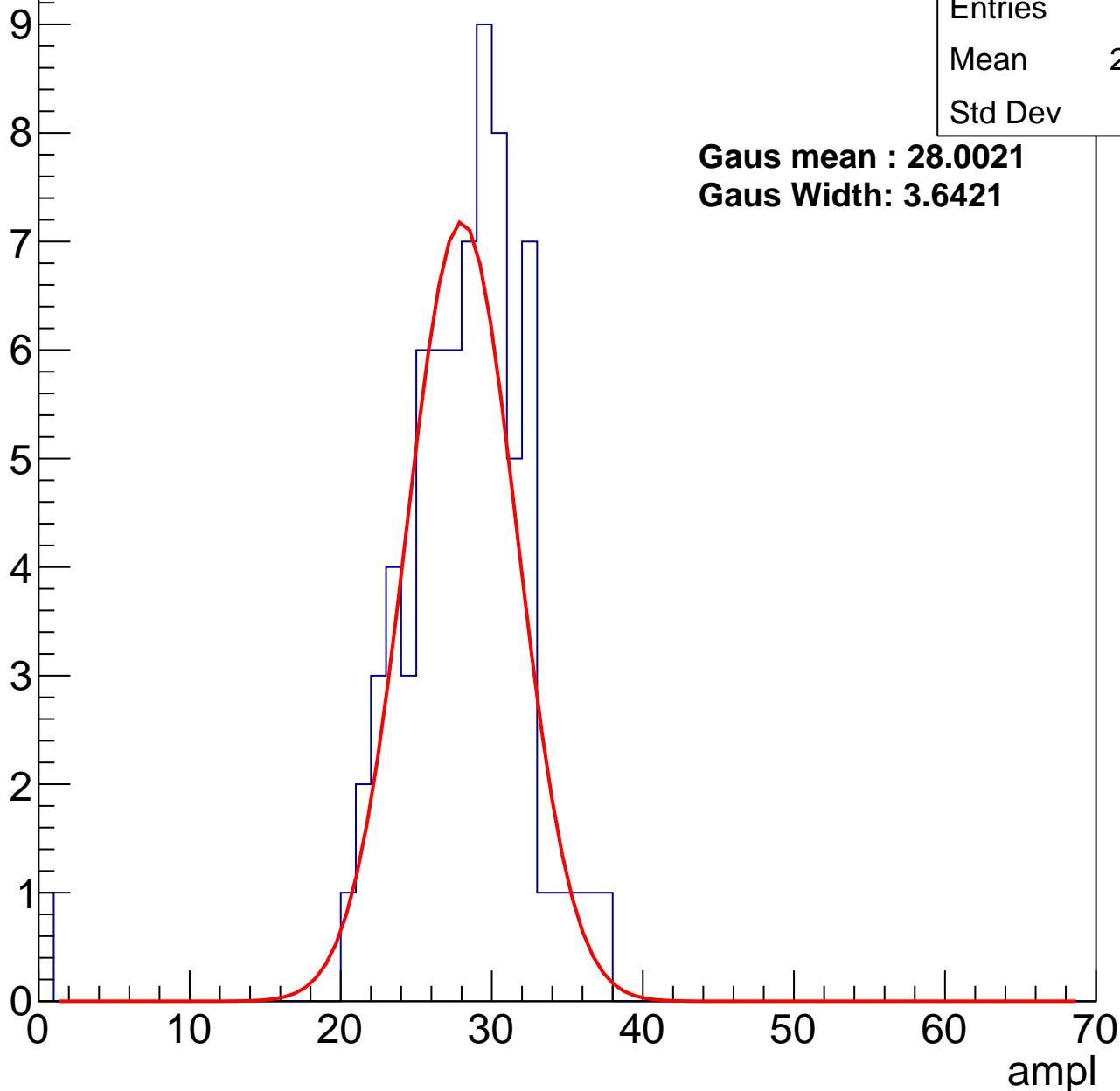
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	27.55
Std Dev	4.86

**Gaus mean : 28.0021**

**Gaus Width: 3.6421**



# B1L101S, U3-ch88, adc1

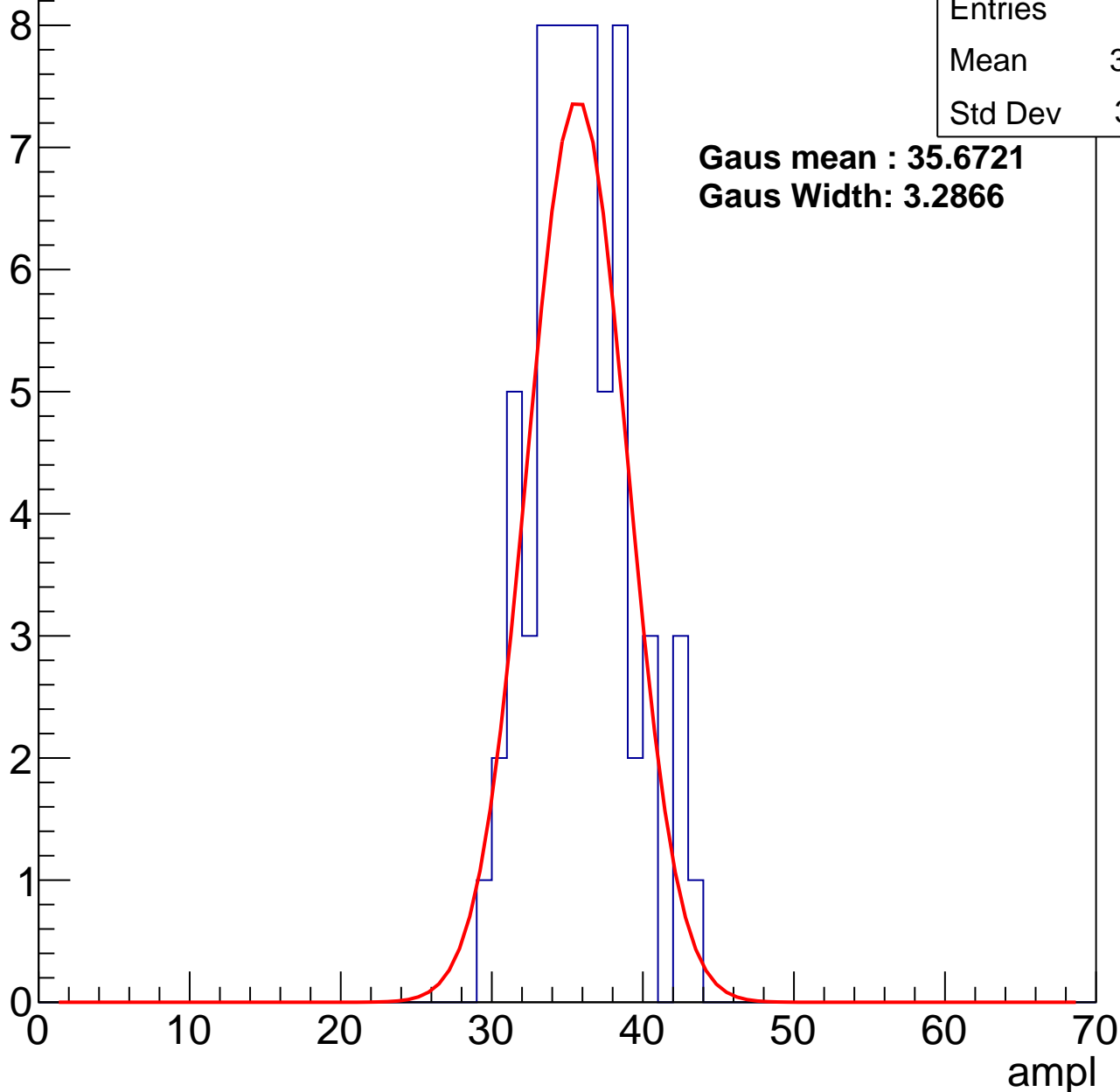
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	35.38
Std Dev	3.141

**Gaus mean : 35.6721**

**Gaus Width: 3.2866**



# B1L101S, U3-ch88, adc2

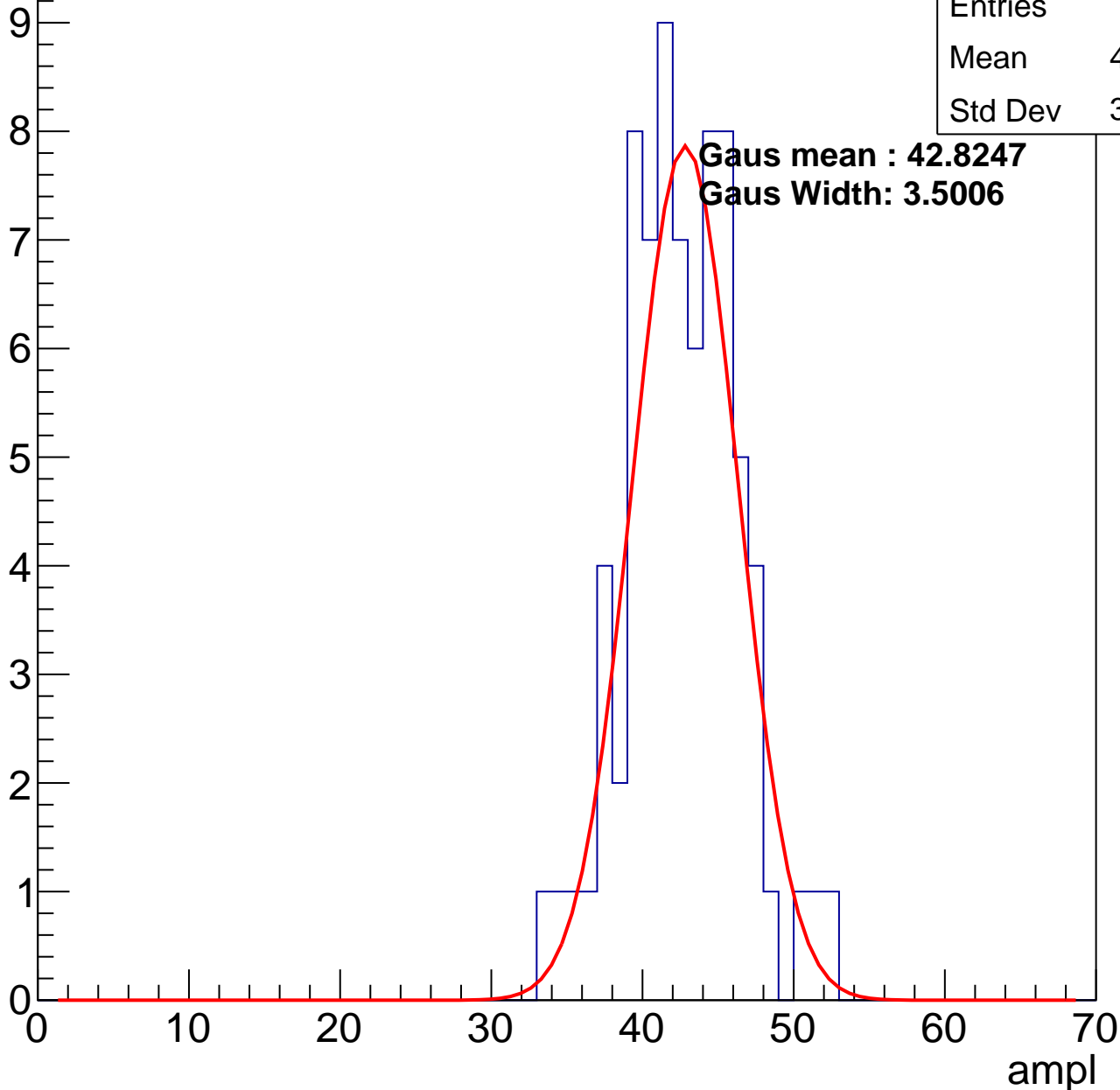
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	42.18
Std Dev	3.698

**Gaus mean : 42.8247**

**Gaus Width: 3.5006**

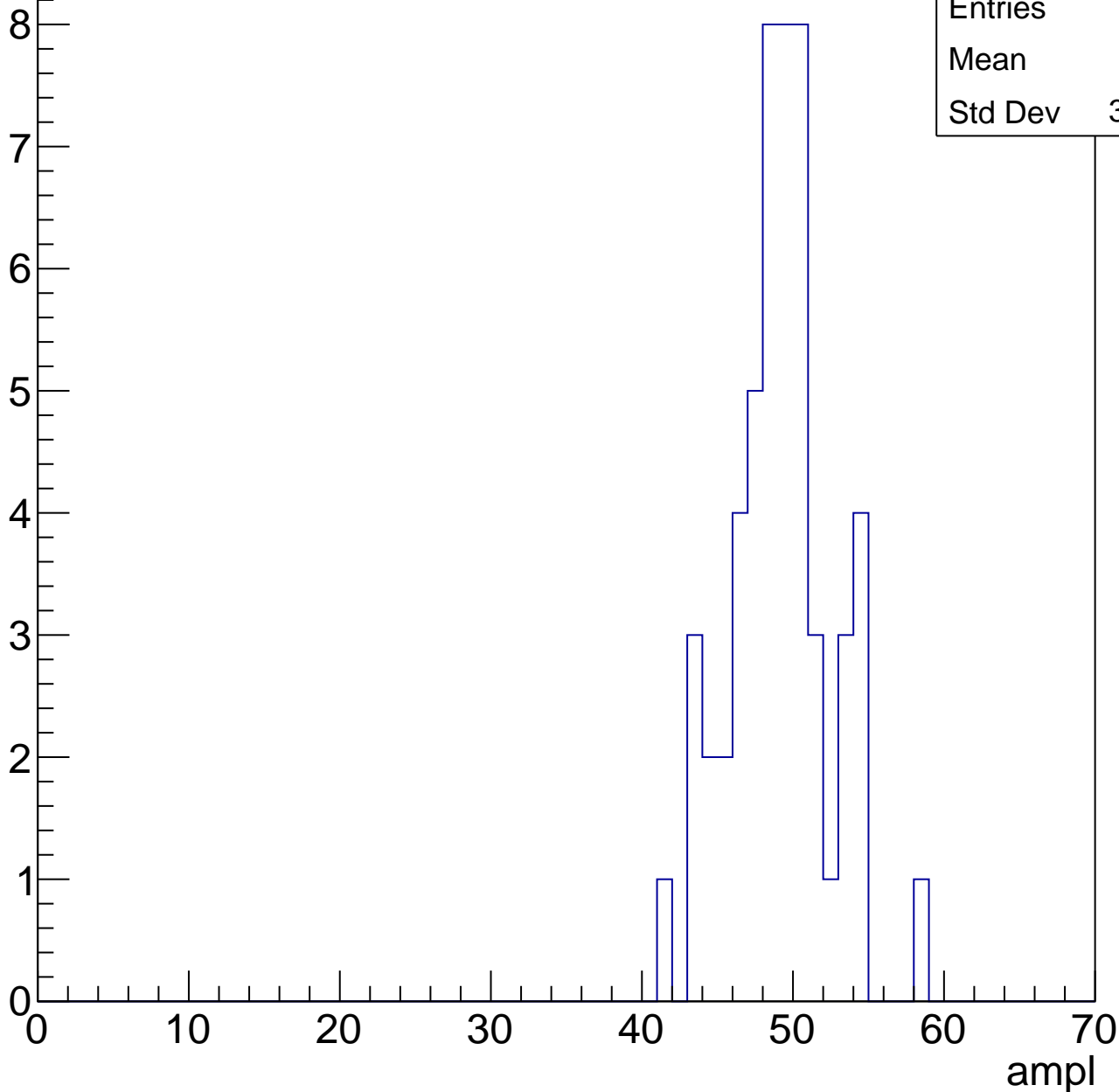


# B1L101S, U3-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	48.7
Std Dev	3.283

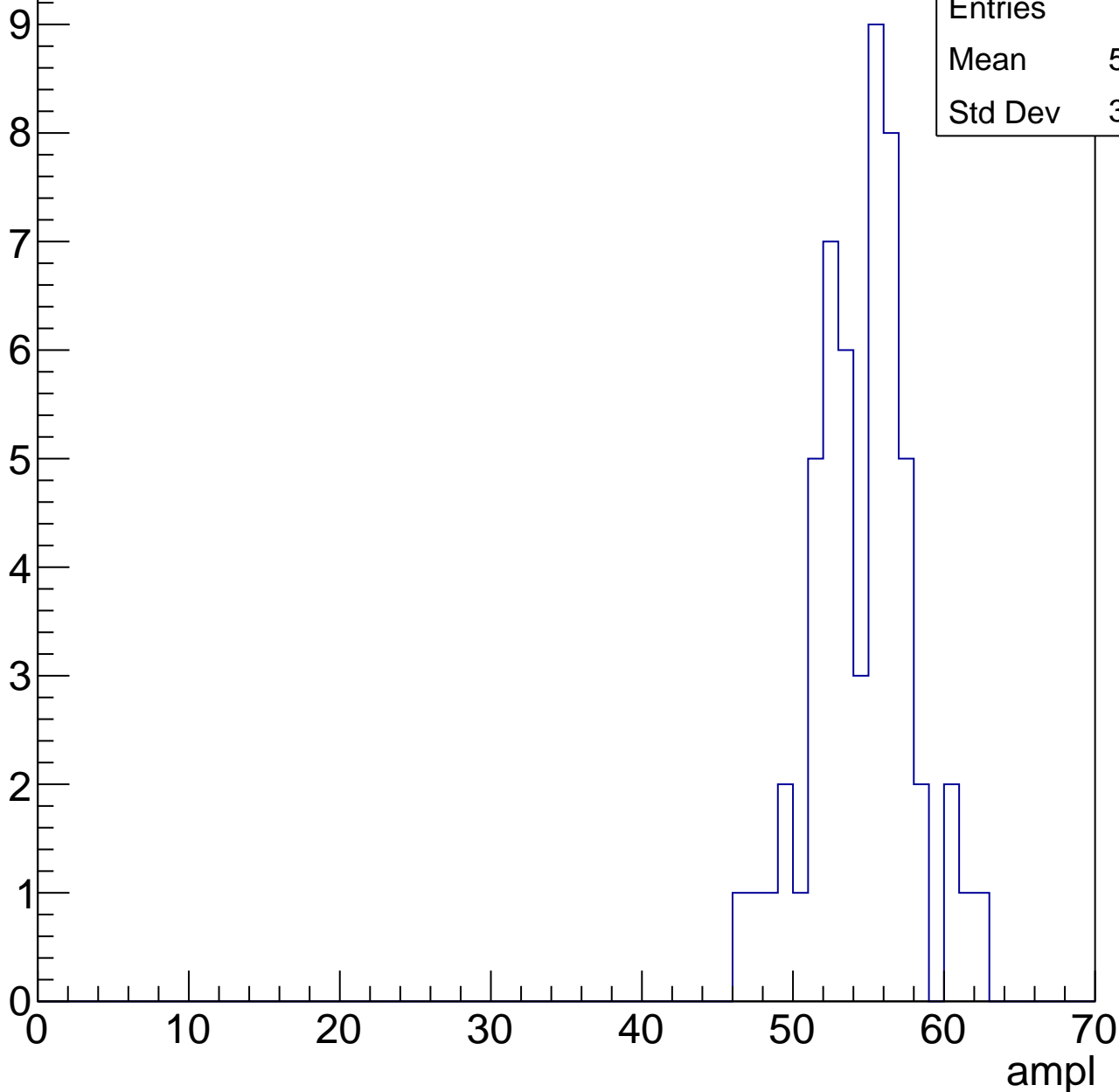


# B1L101S, U3-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	54.09
Std Dev	3.293

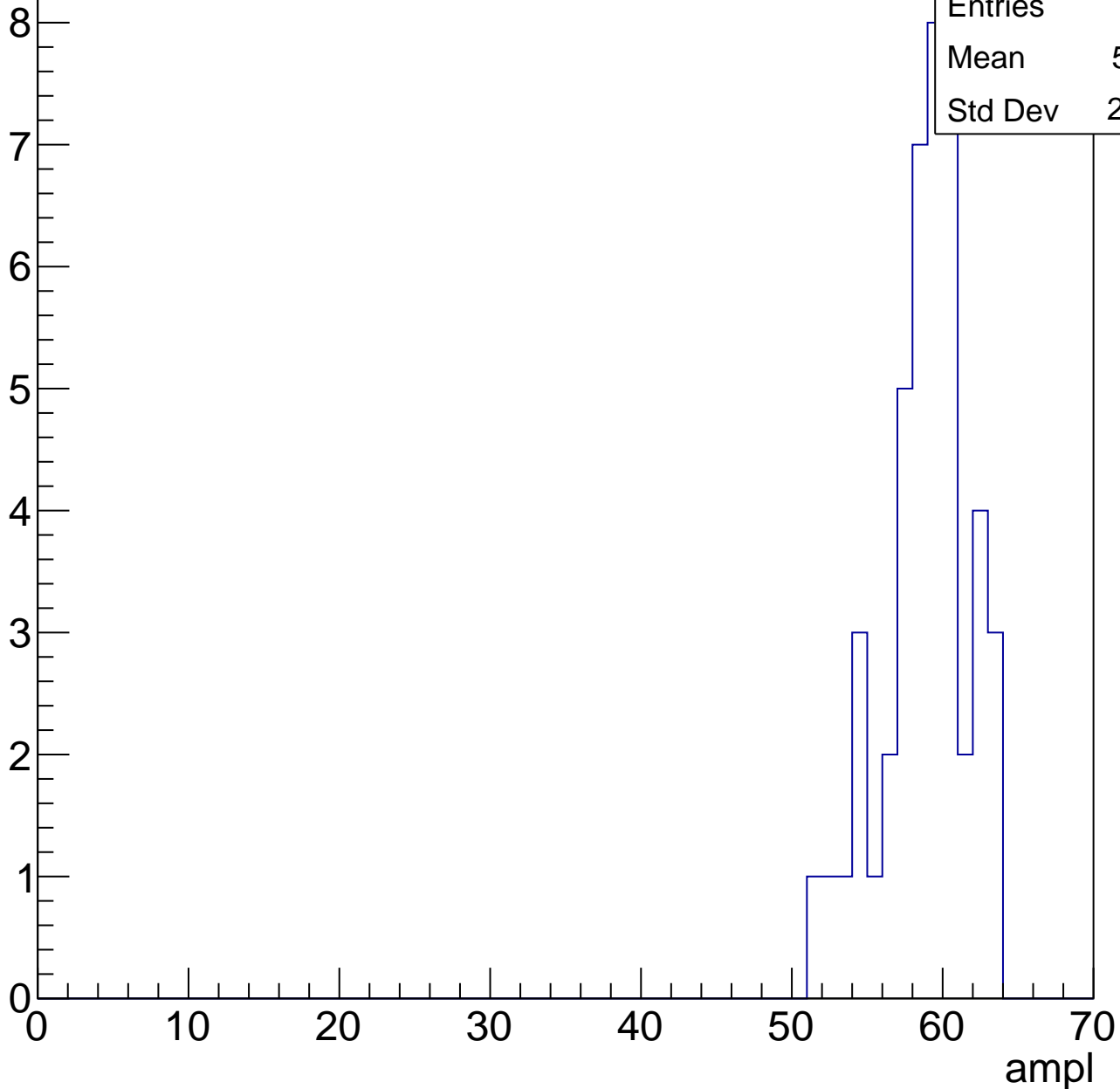


# B1L101S, U3-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	58.41
Std Dev	2.833

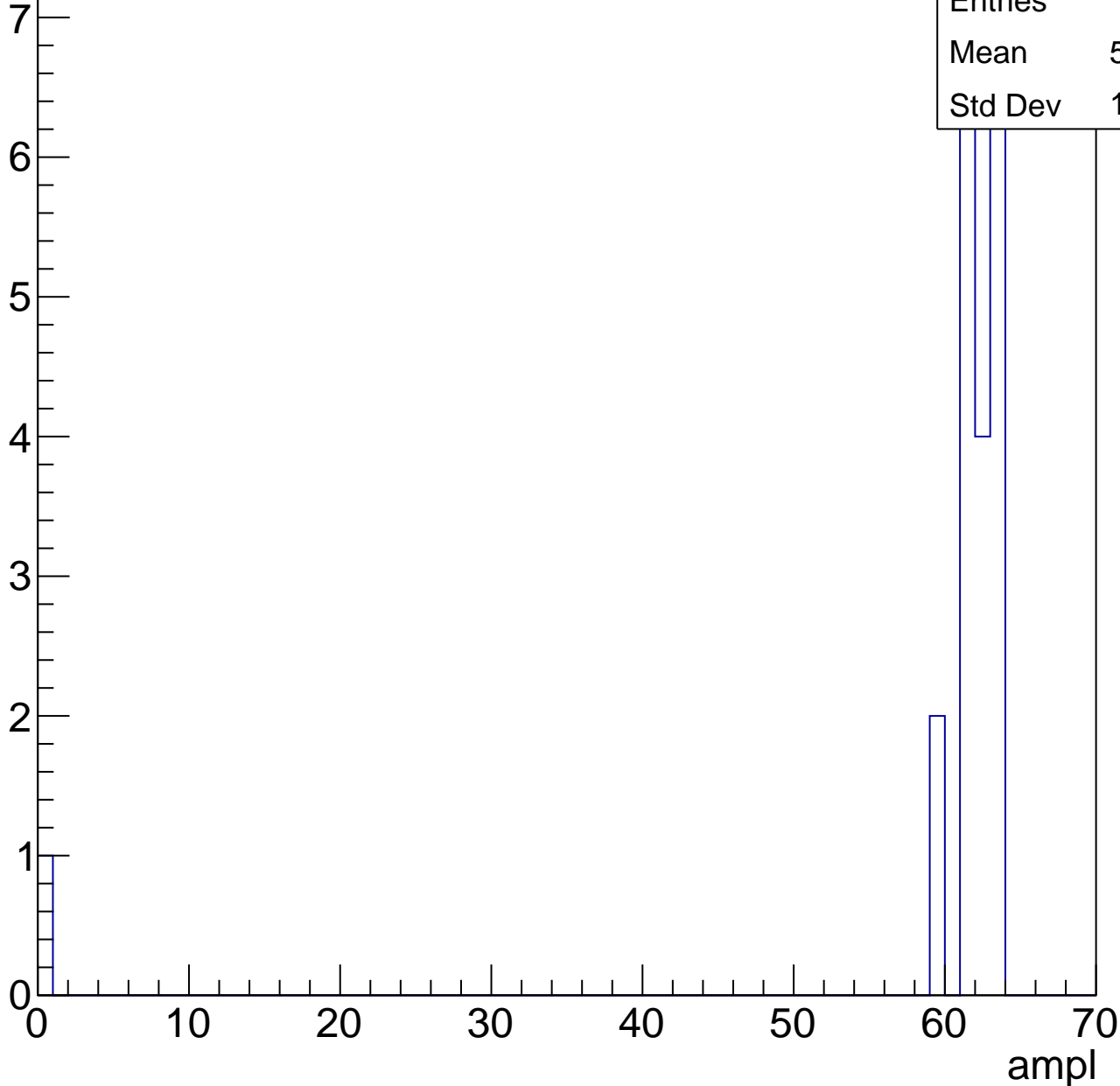


# B1L101S, U3-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	21
Mean	58.76
Std Dev	13.19

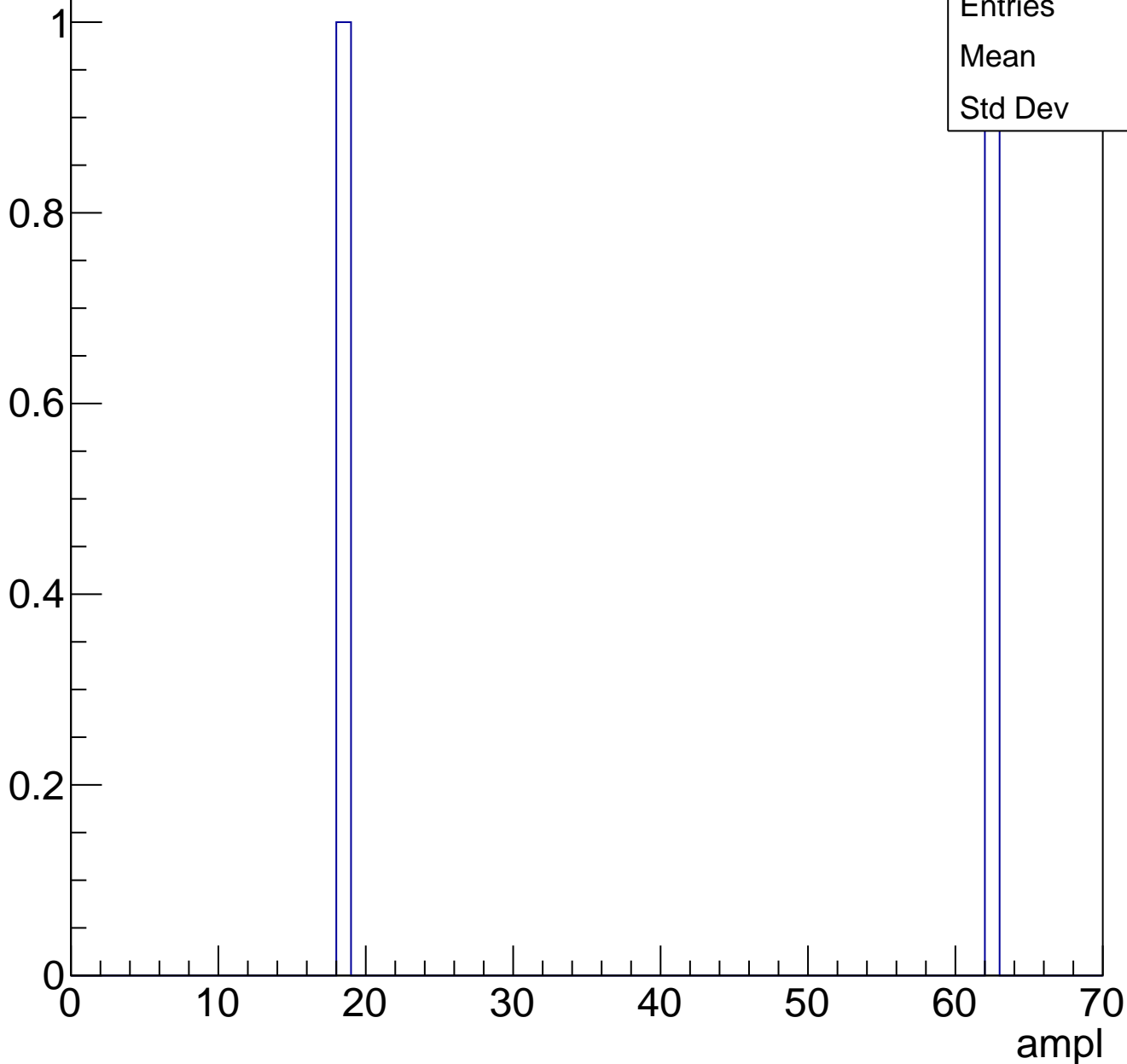




# B1L101S, U3-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch89, adc0

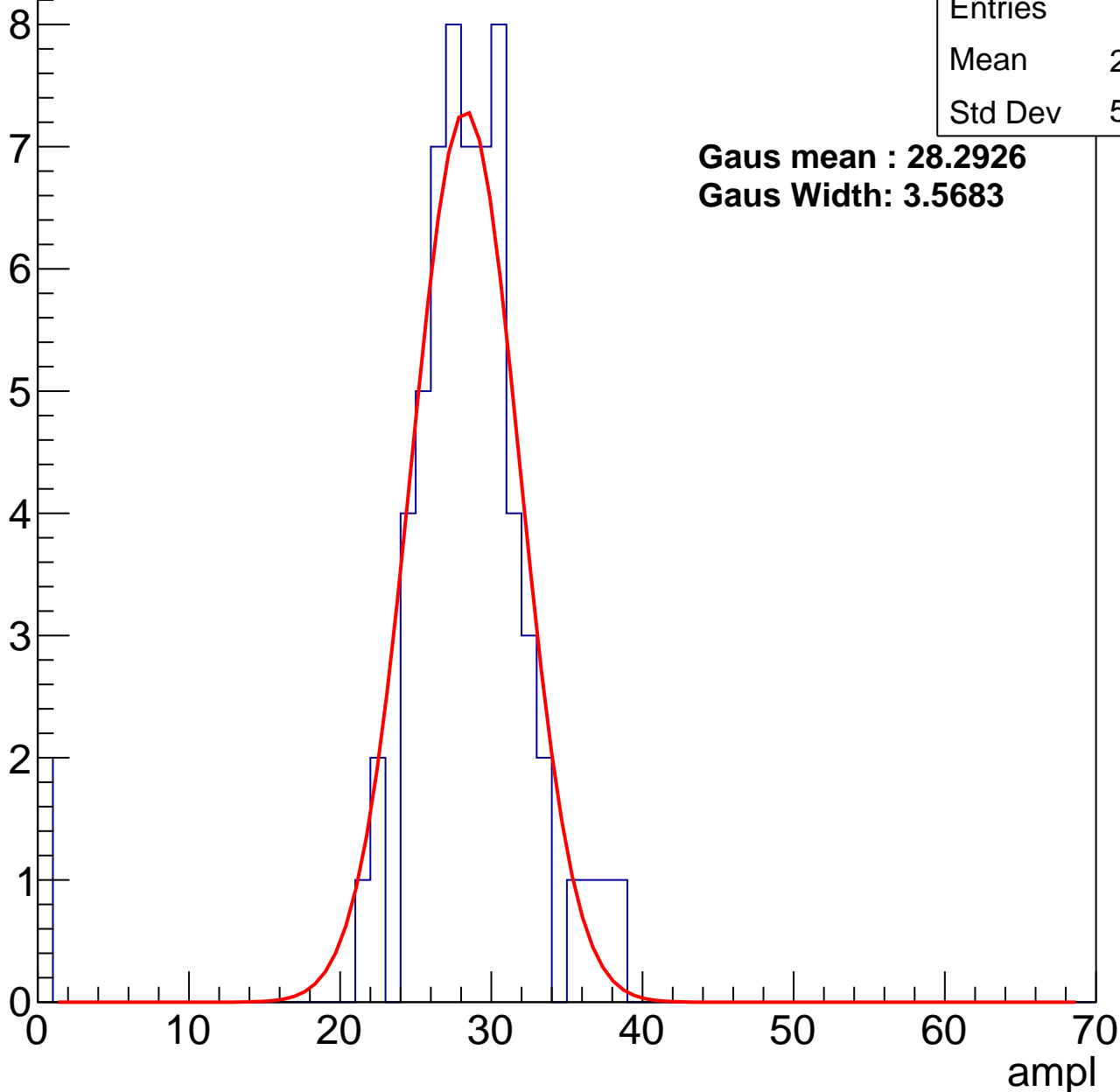
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	27.42
Std Dev	5.968

**Gaus mean : 28.2926**

**Gaus Width: 3.5683**



# B1L101S, U3-ch89, adc1

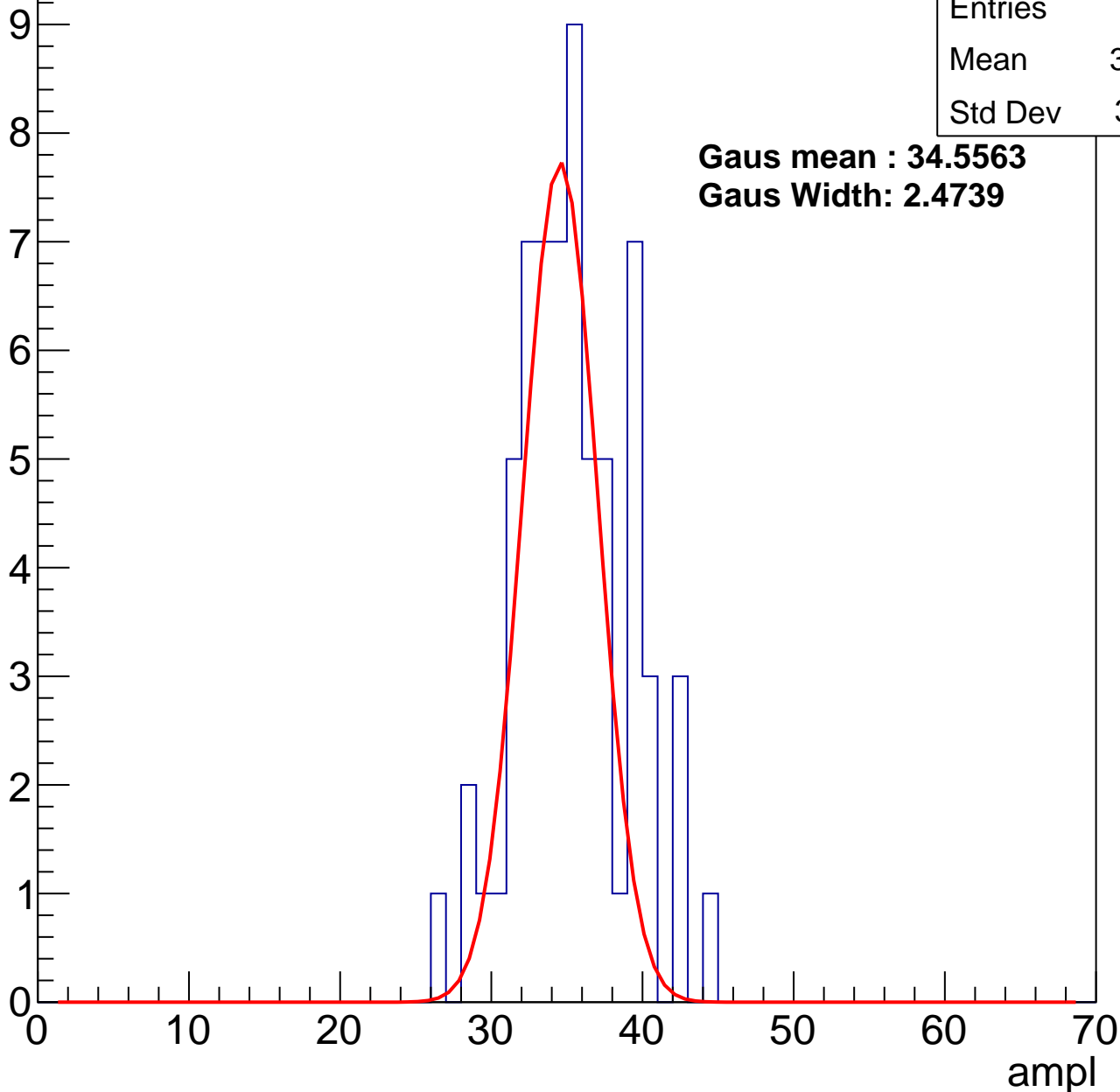
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	34.92
Std Dev	3.651

**Gaus mean : 34.5563**

**Gaus Width: 2.4739**



# B1L101S, U3-ch89, adc2

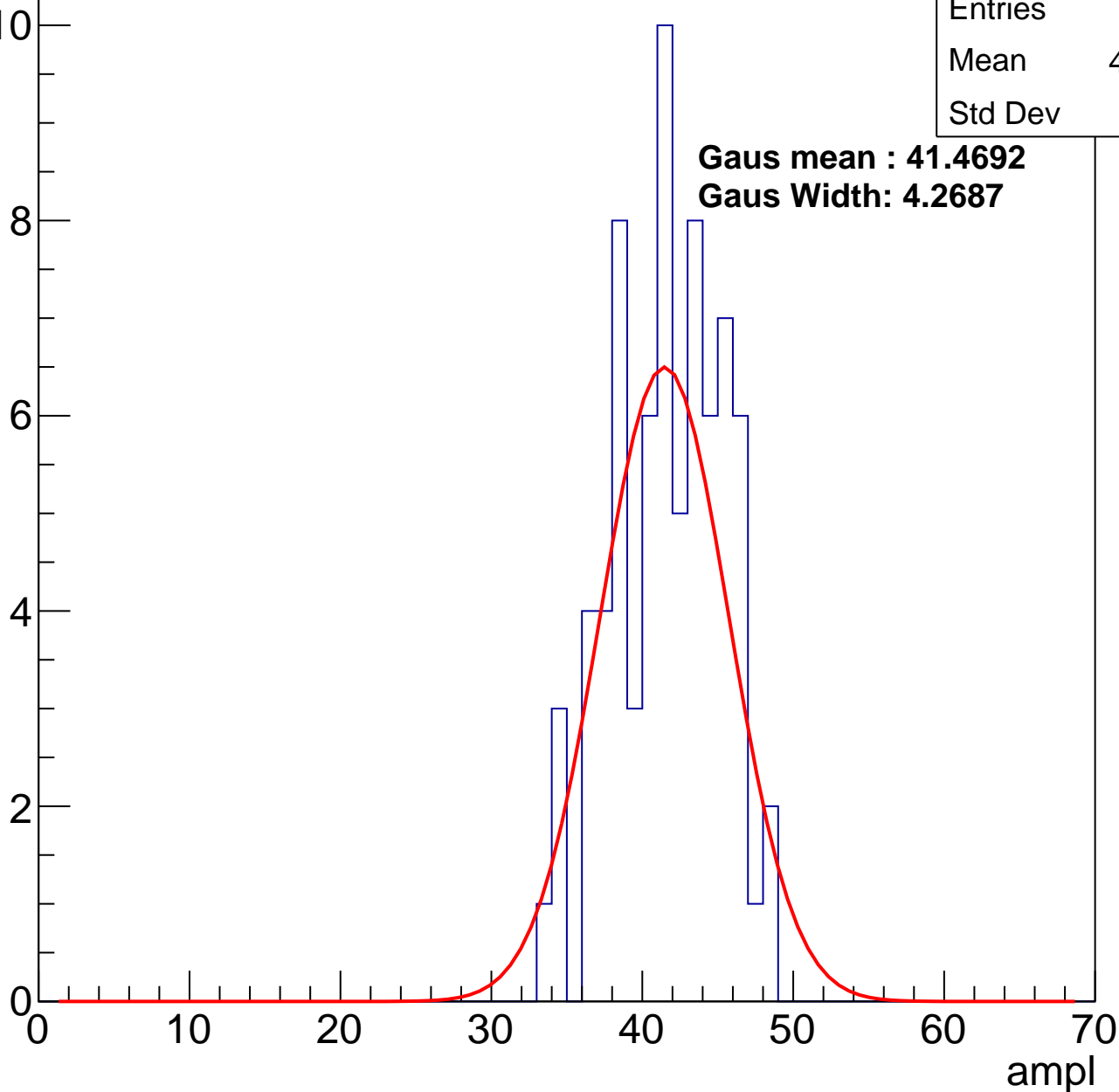
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	41.22
Std Dev	3.58

**Gaus mean : 41.4692**

**Gaus Width: 4.2687**

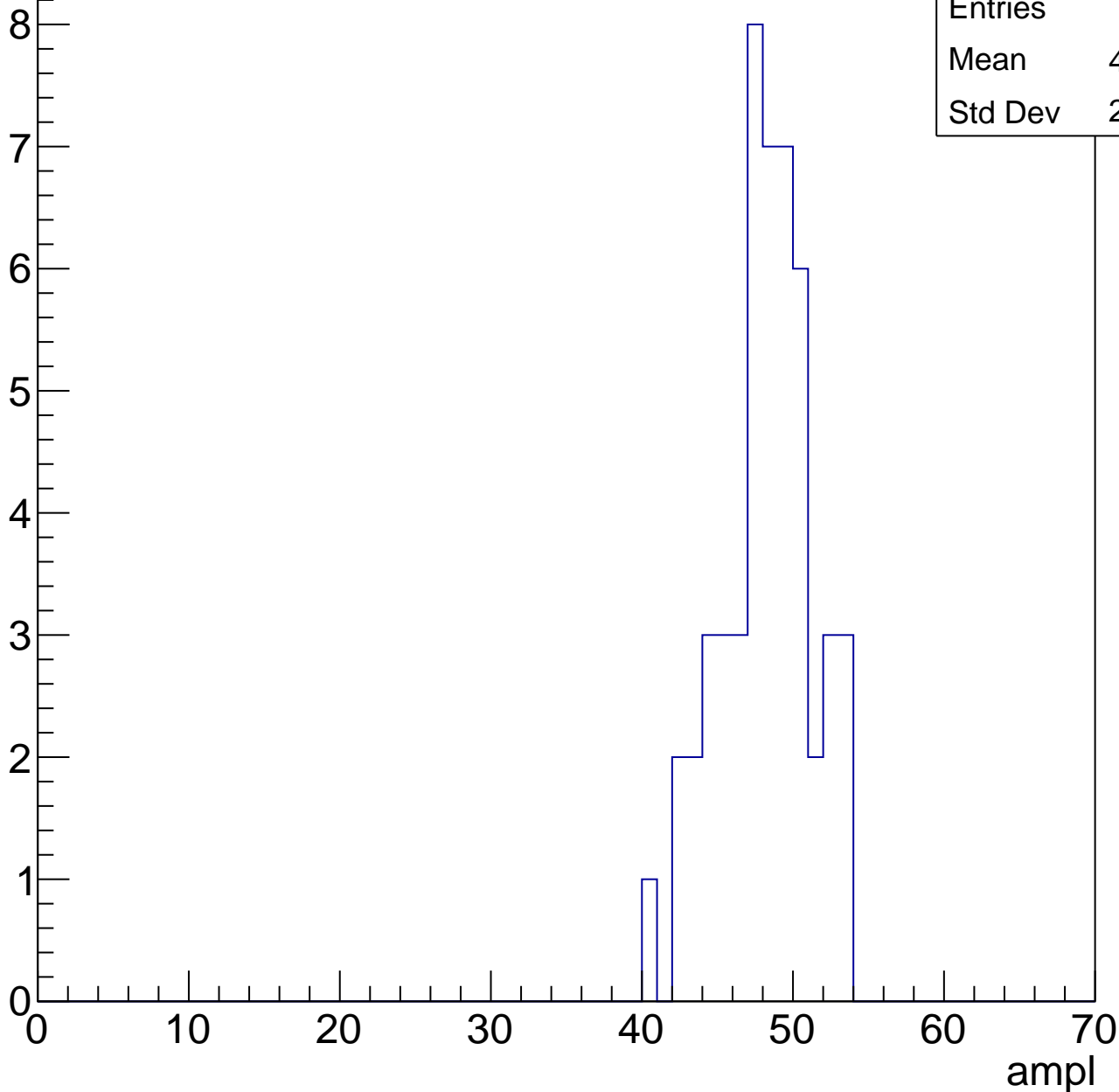


# B1L101S, U3-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	47.74
Std Dev	2.999

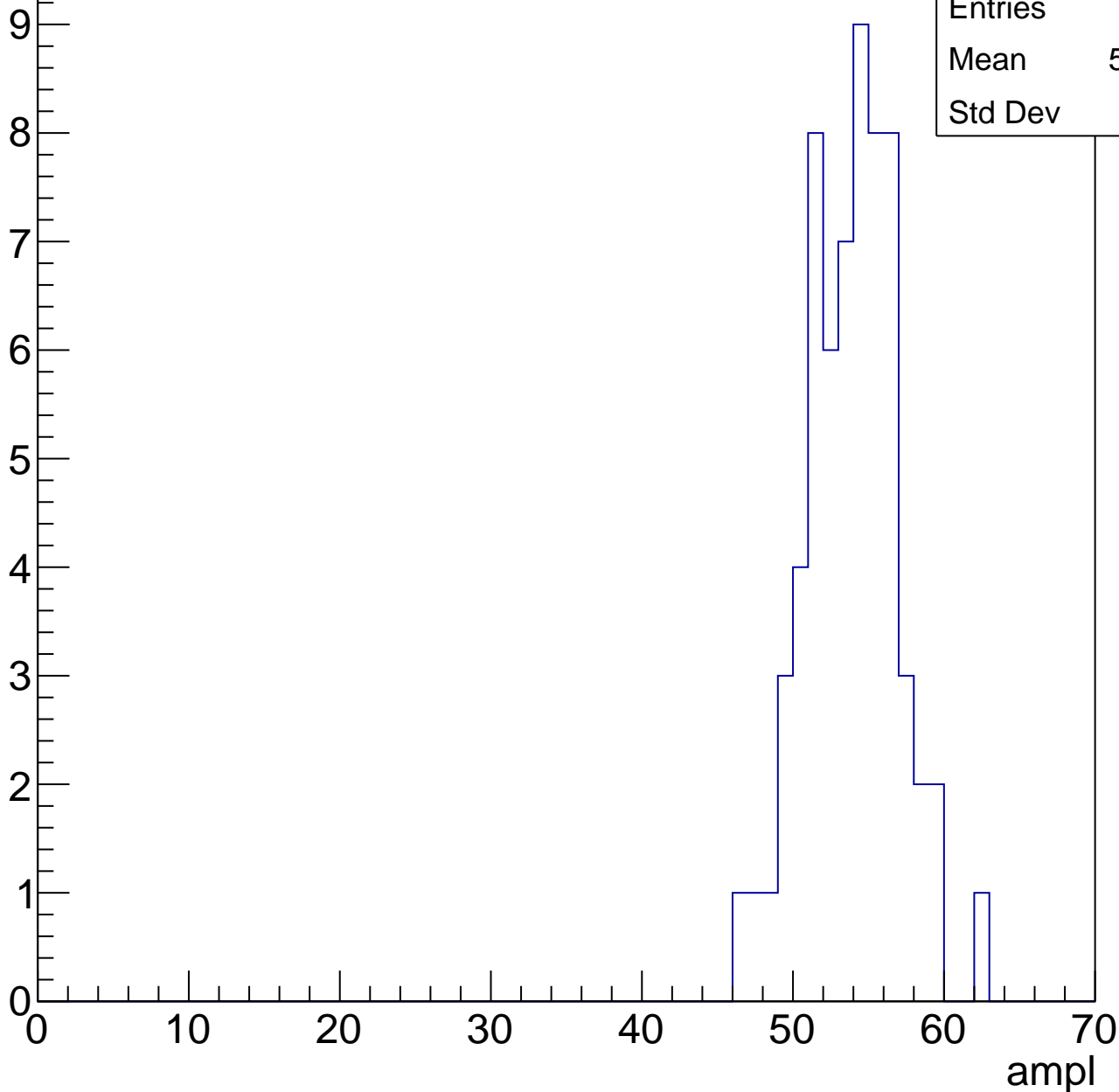


# B1L101S, U3-ch89, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	53.44
Std Dev	3.02



# B1L101S, U3-ch89, adc5

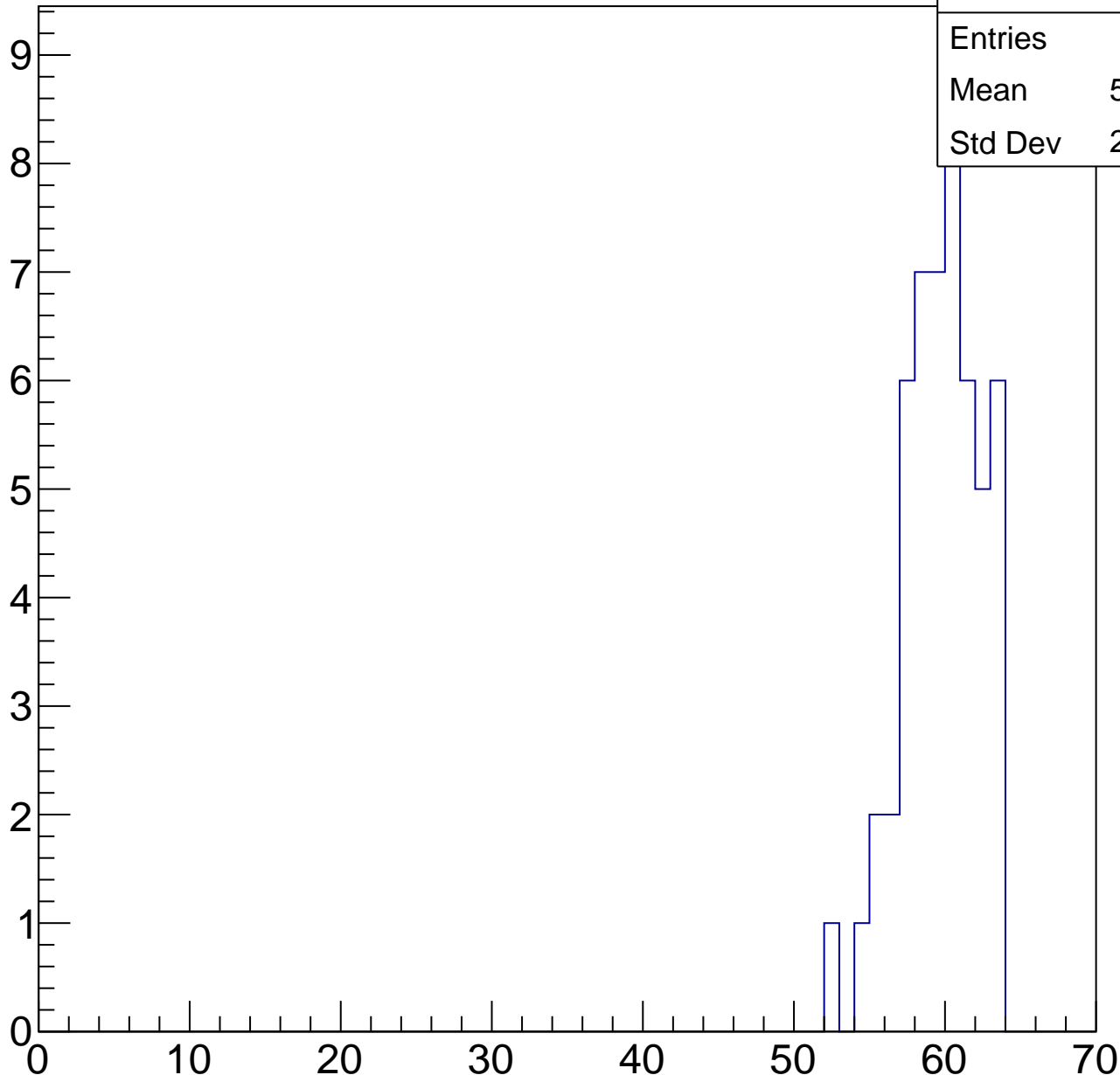
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	52
Mean	59.29
Std Dev	2.499

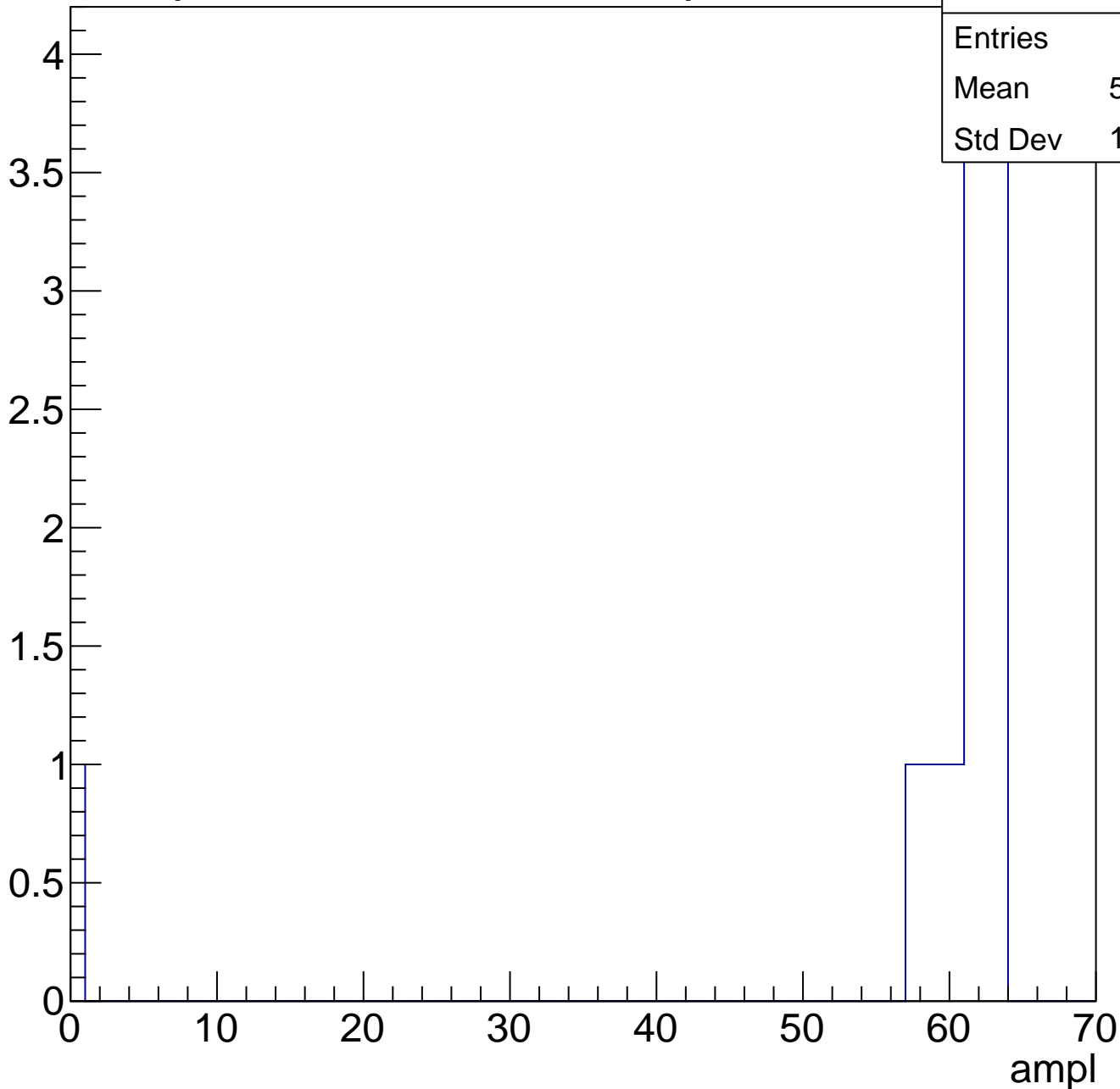
ampl



# B1L101S, U3-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U3-ch90, adc0

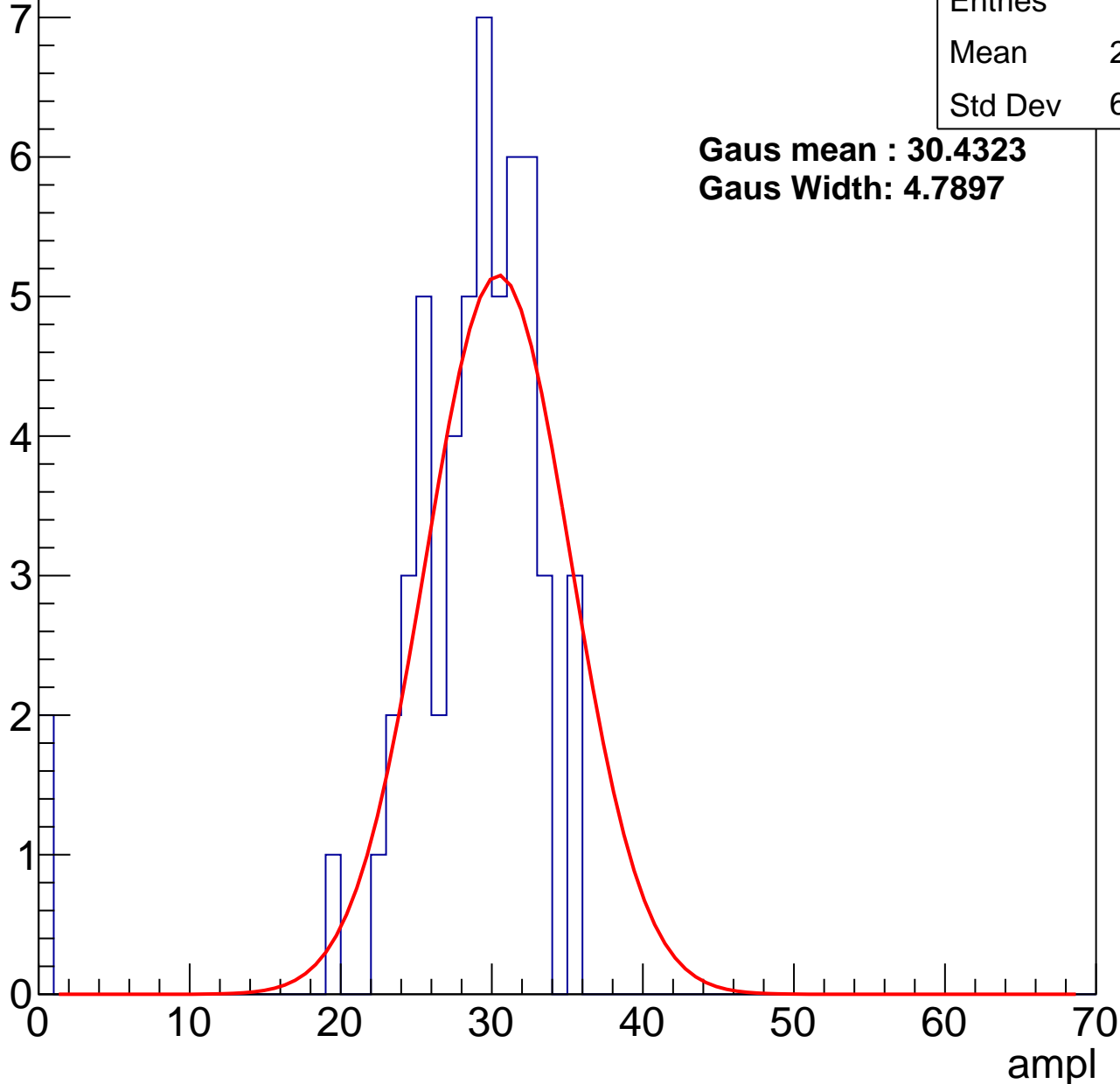
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	27.62
Std Dev	6.369

**Gaus mean : 30.4323**

**Gaus Width: 4.7897**



# B1L101S, U3-ch90, adc1

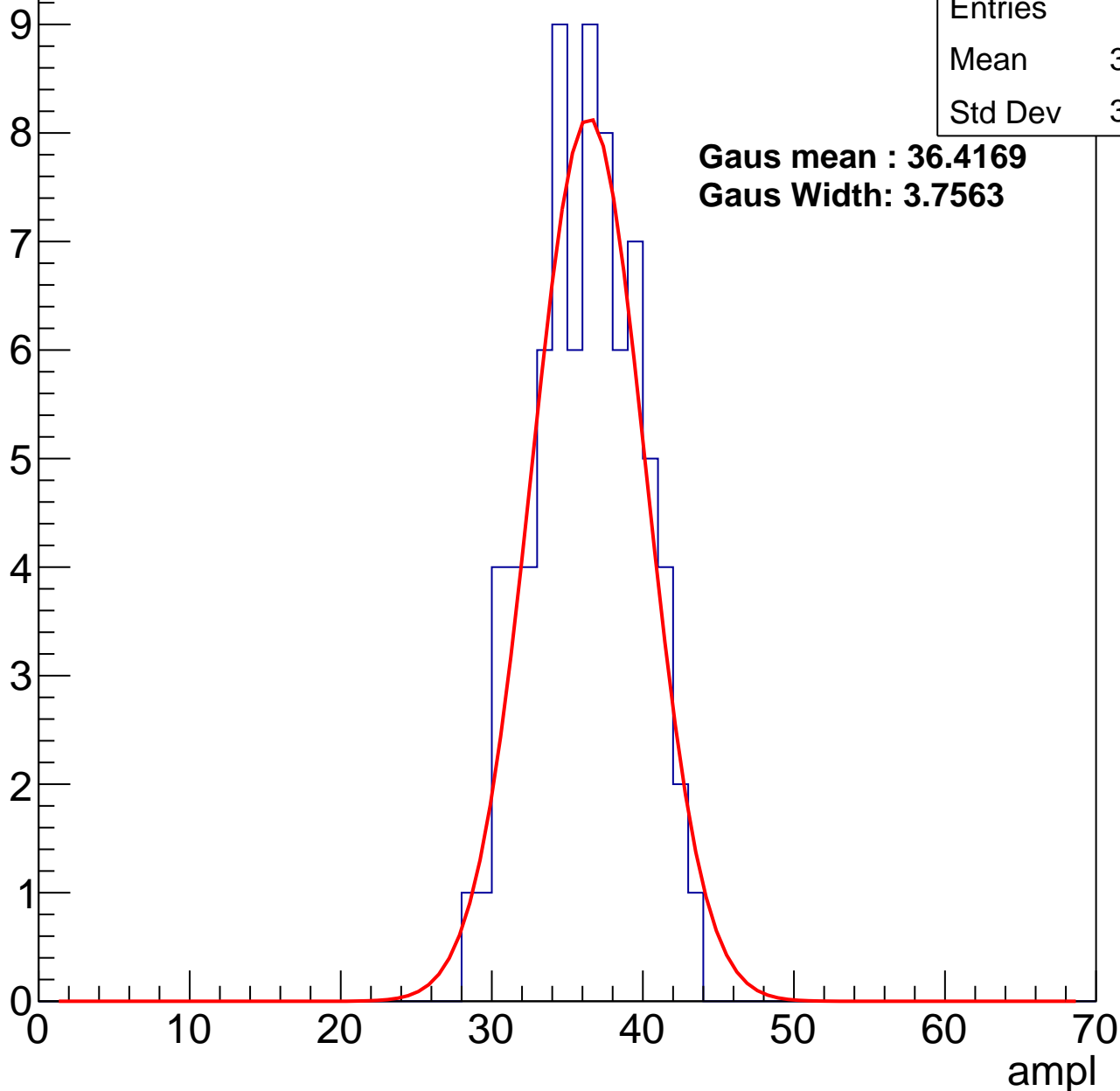
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	35.78
Std Dev	3.436

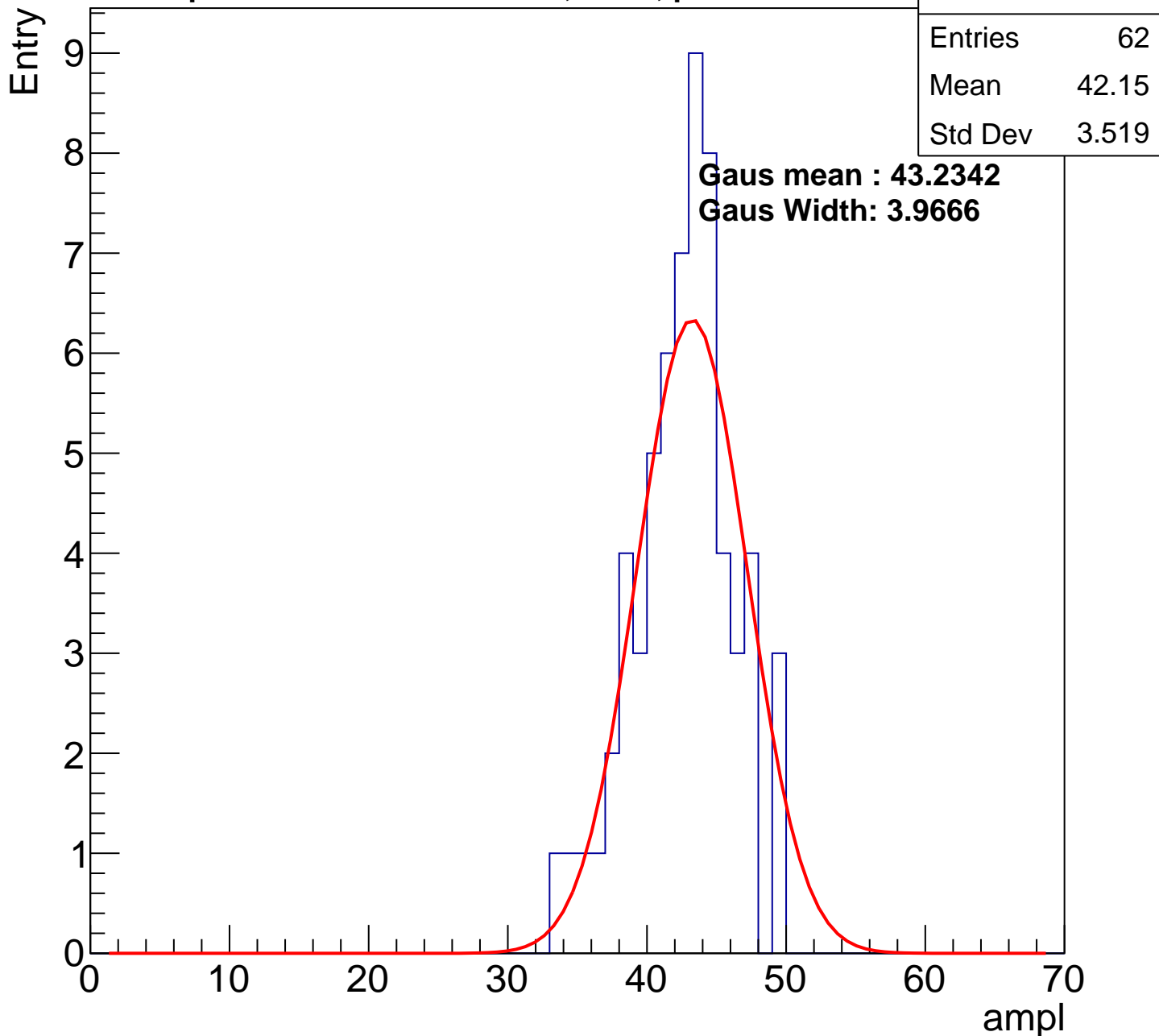
**Gaus mean : 36.4169**

**Gaus Width: 3.7563**



# B1L101S, U3-ch90, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

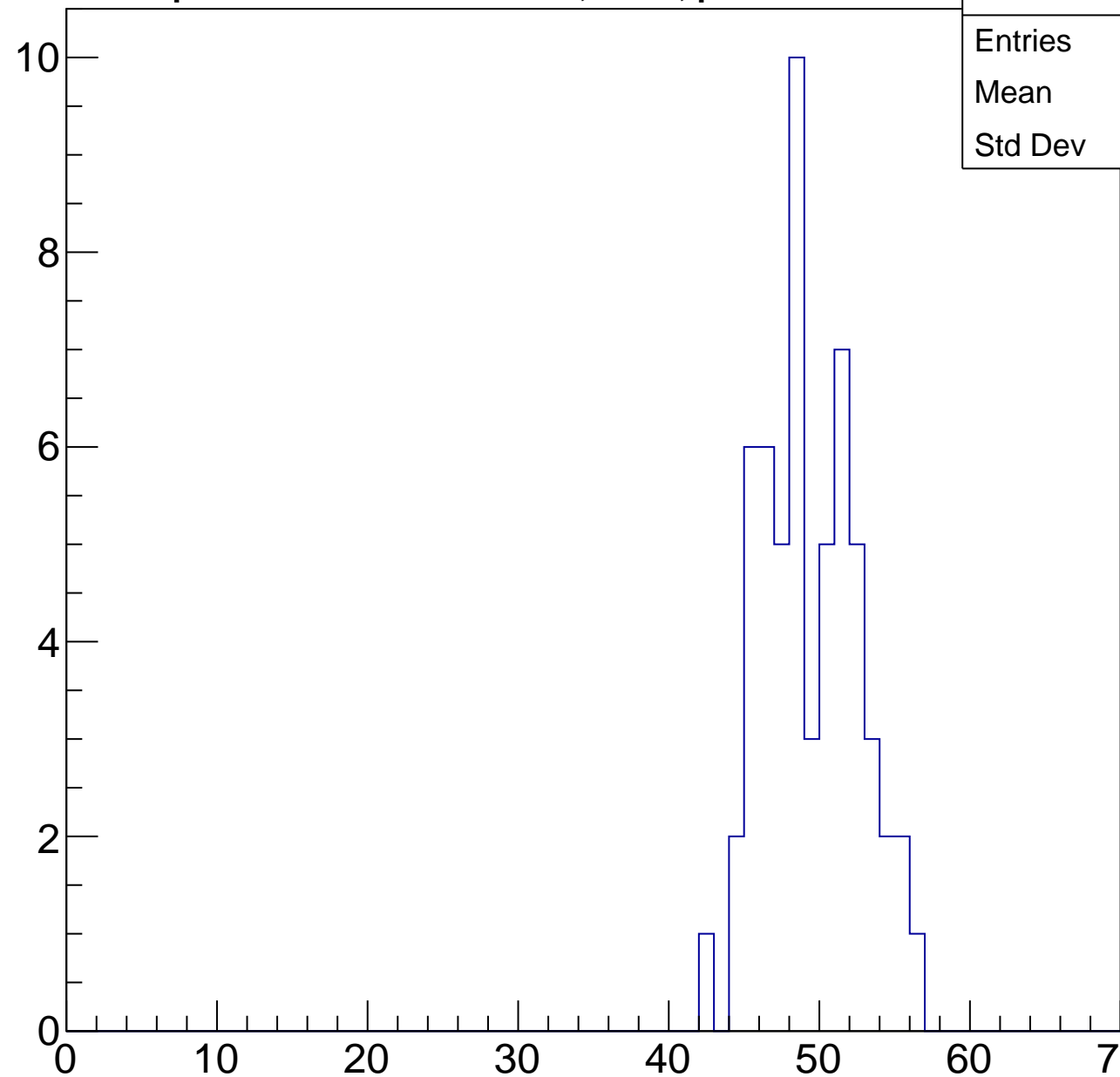
Entries	58
Mean	48.93
Std Dev	3.151

Entry

10  
8  
6  
4  
2  
0

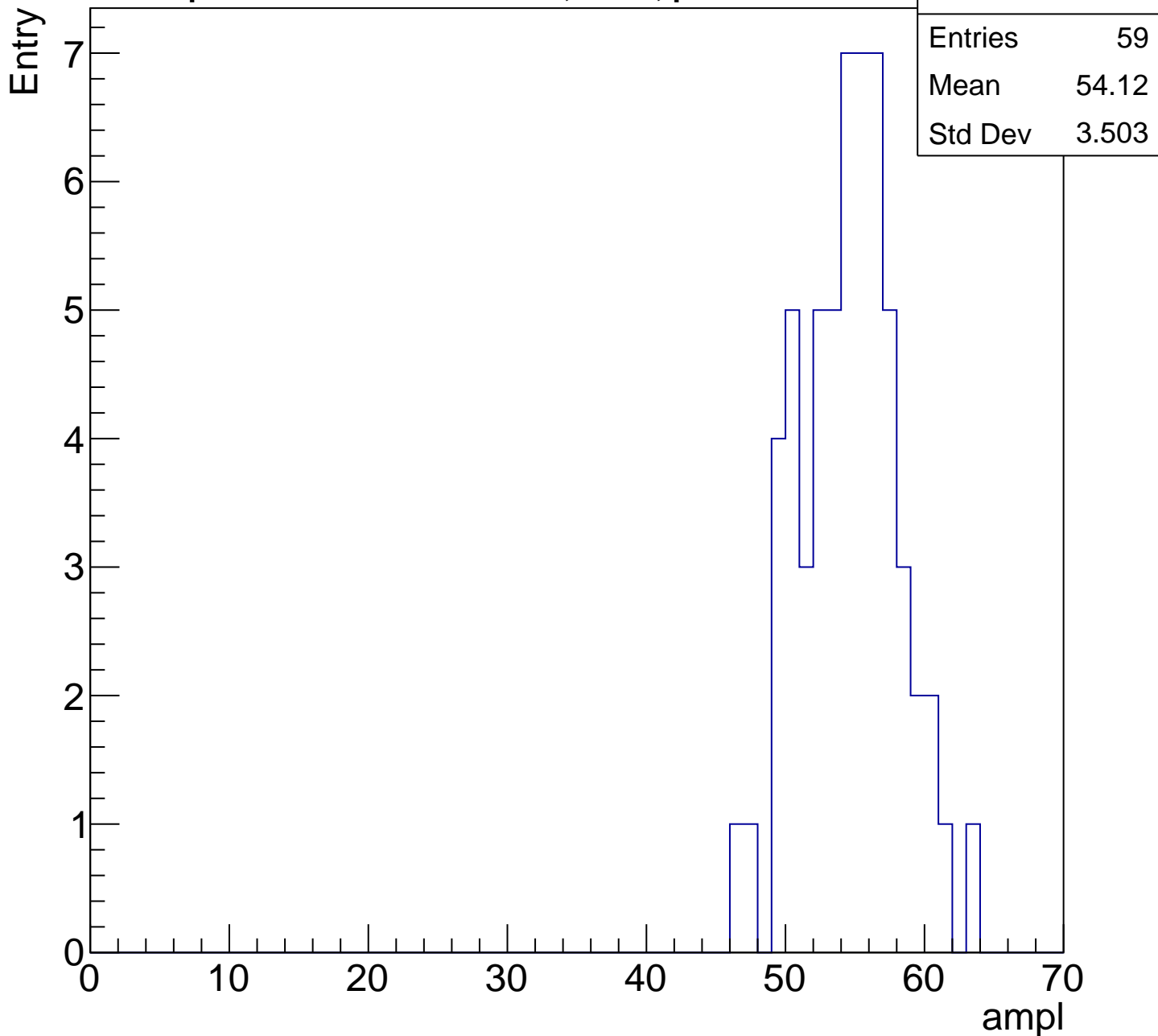
0 10 20 30 40 50 60 70

ampl



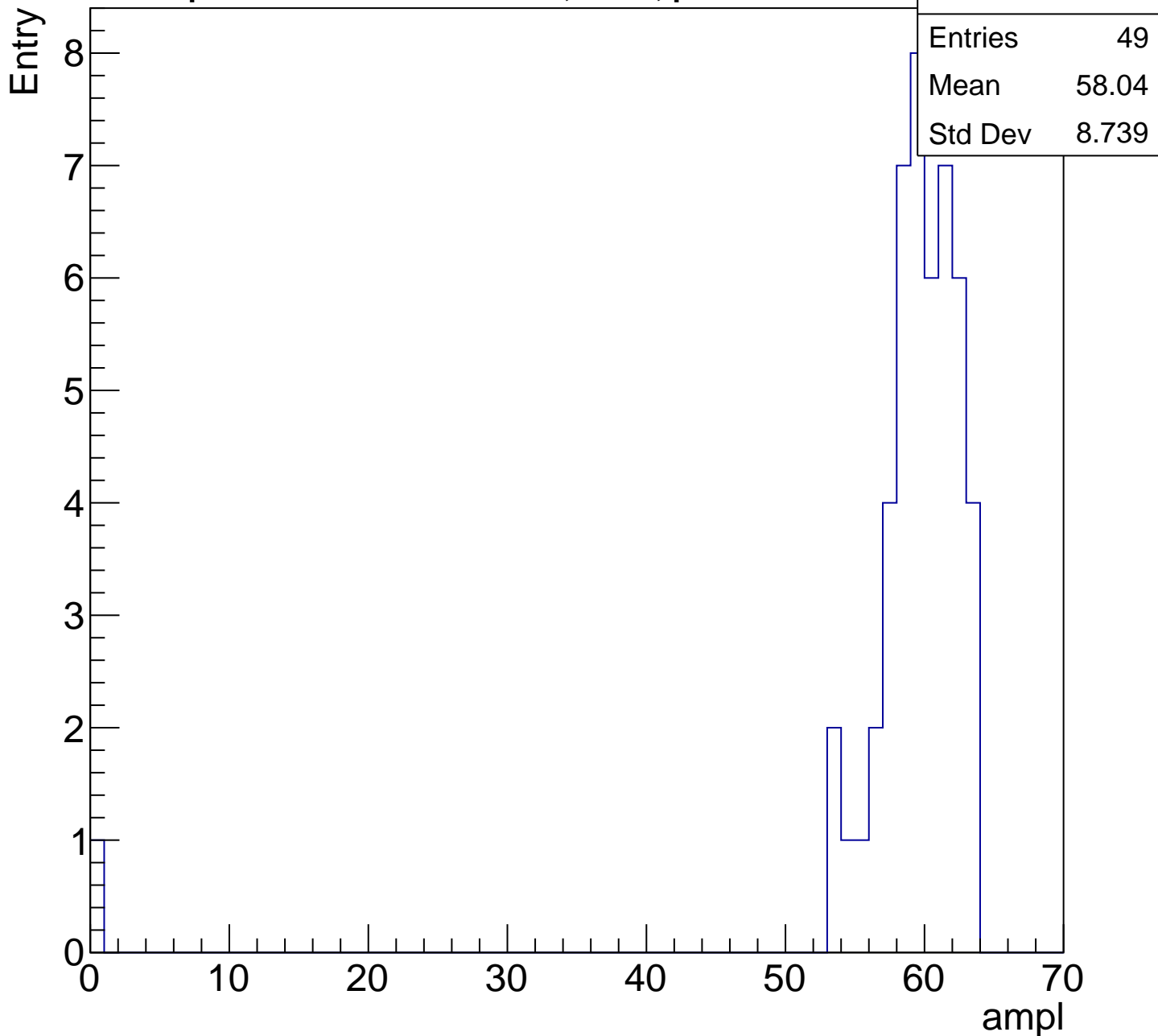
# B1L101S, U3-ch90, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch90, adc5

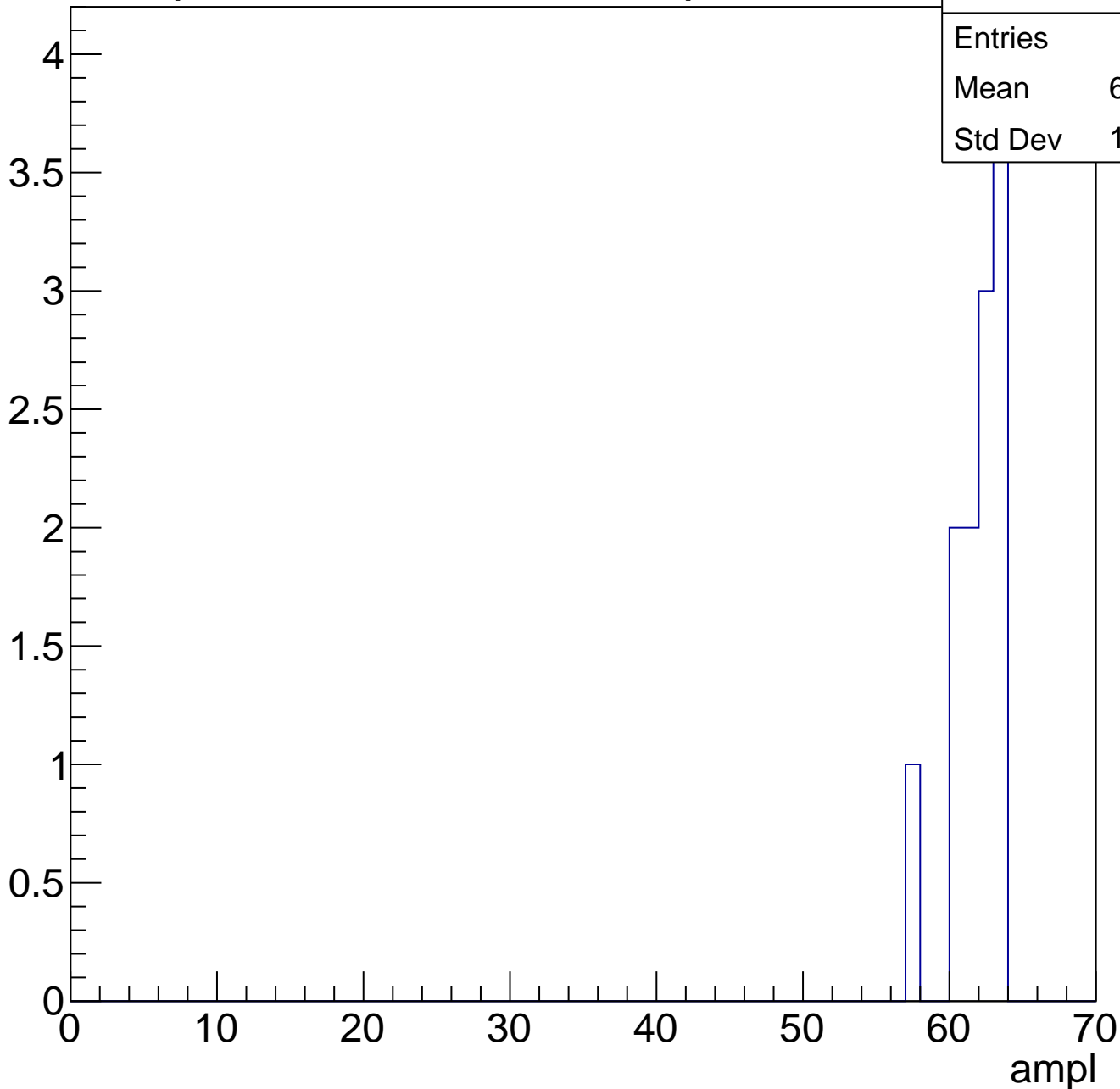
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch91, adc0

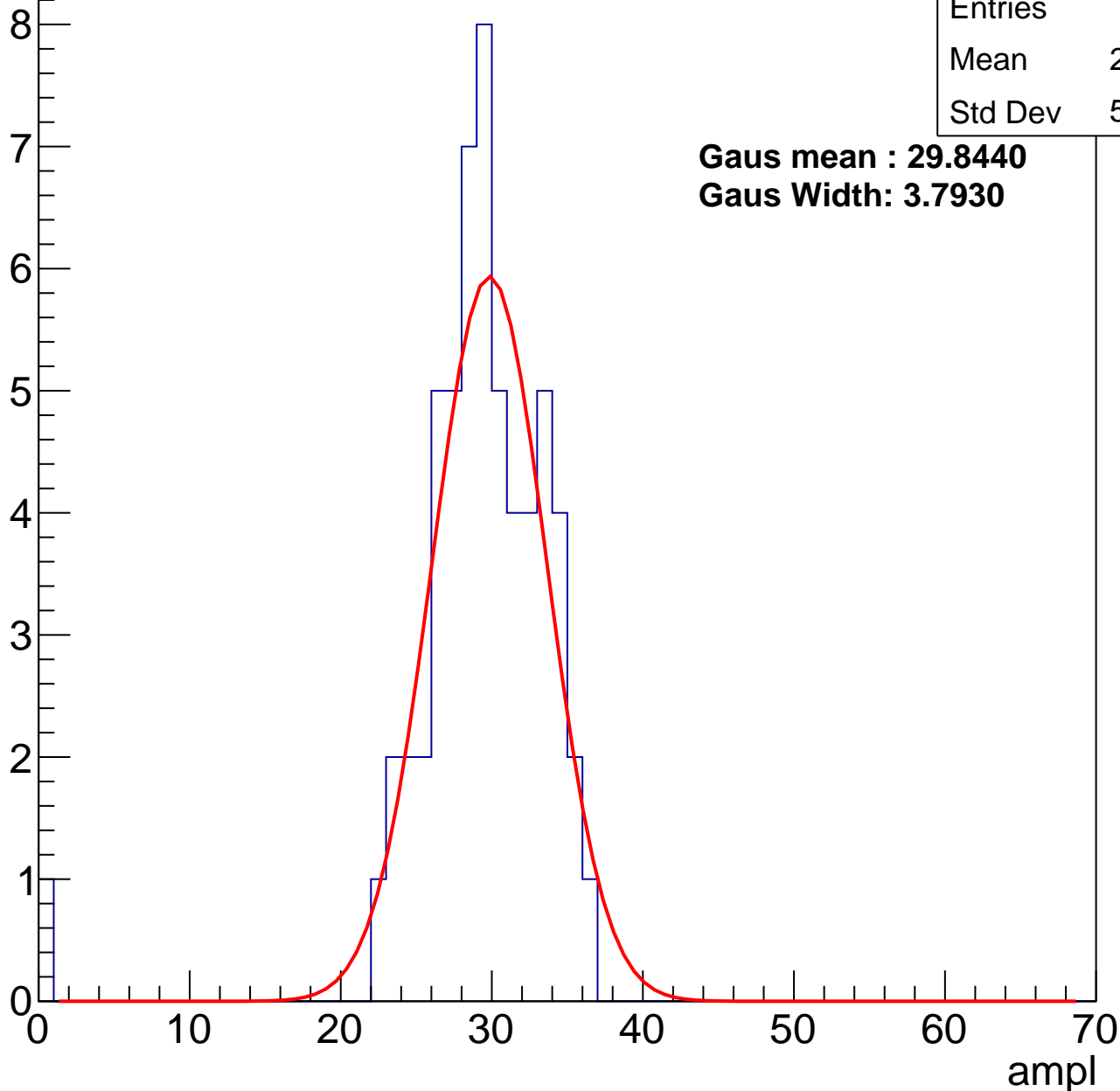
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	28.76
Std Dev	5.035

**Gaus mean : 29.8440**

**Gaus Width: 3.7930**



# B1L101S, U3-ch91, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

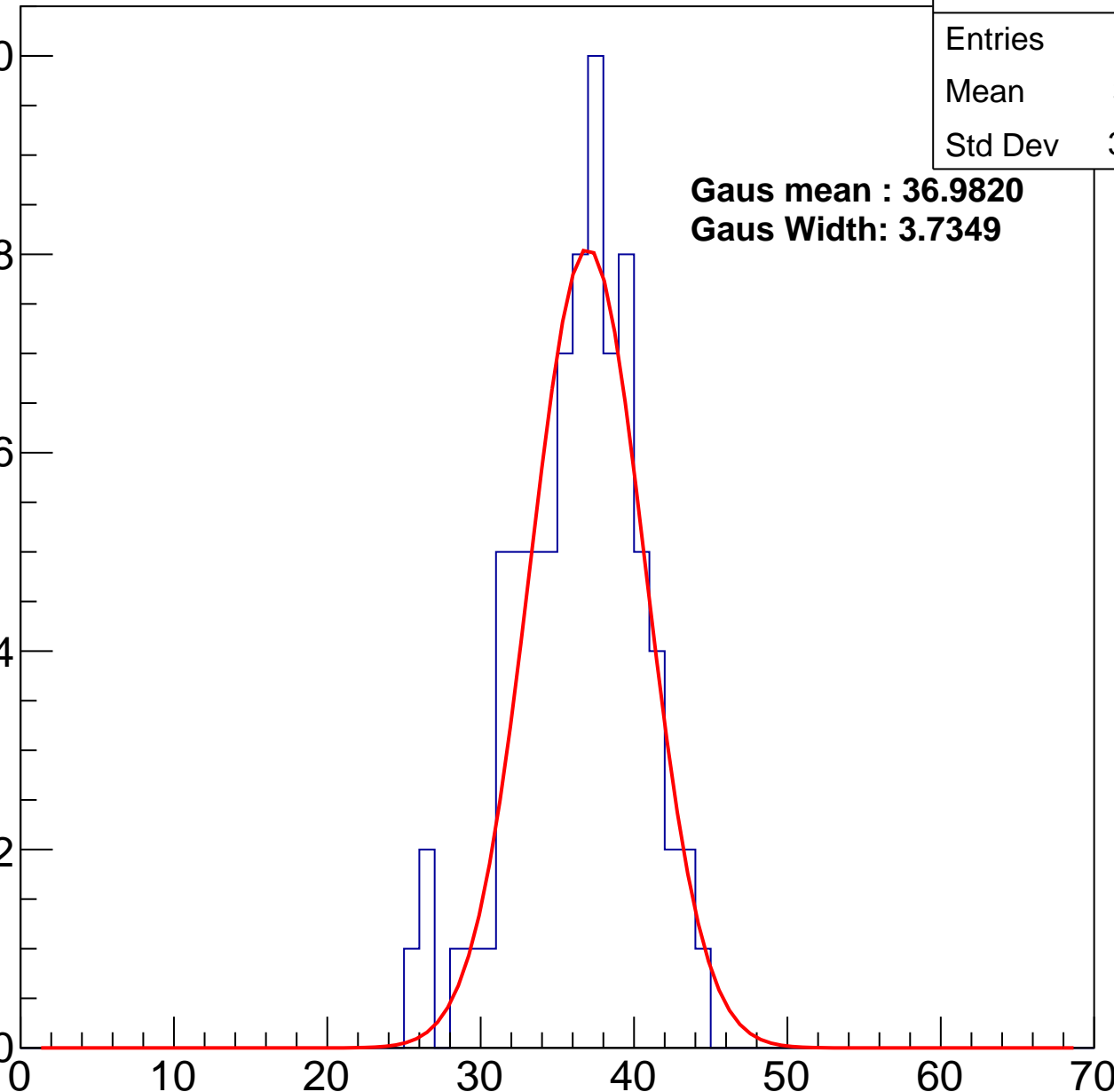
Entries	80
Mean	35.91
Std Dev	3.985

**Gaus mean : 36.9820**

**Gaus Width: 3.7349**

10  
8  
6  
4  
2  
0

ampl



# B1L101S, U3-ch91, adc2

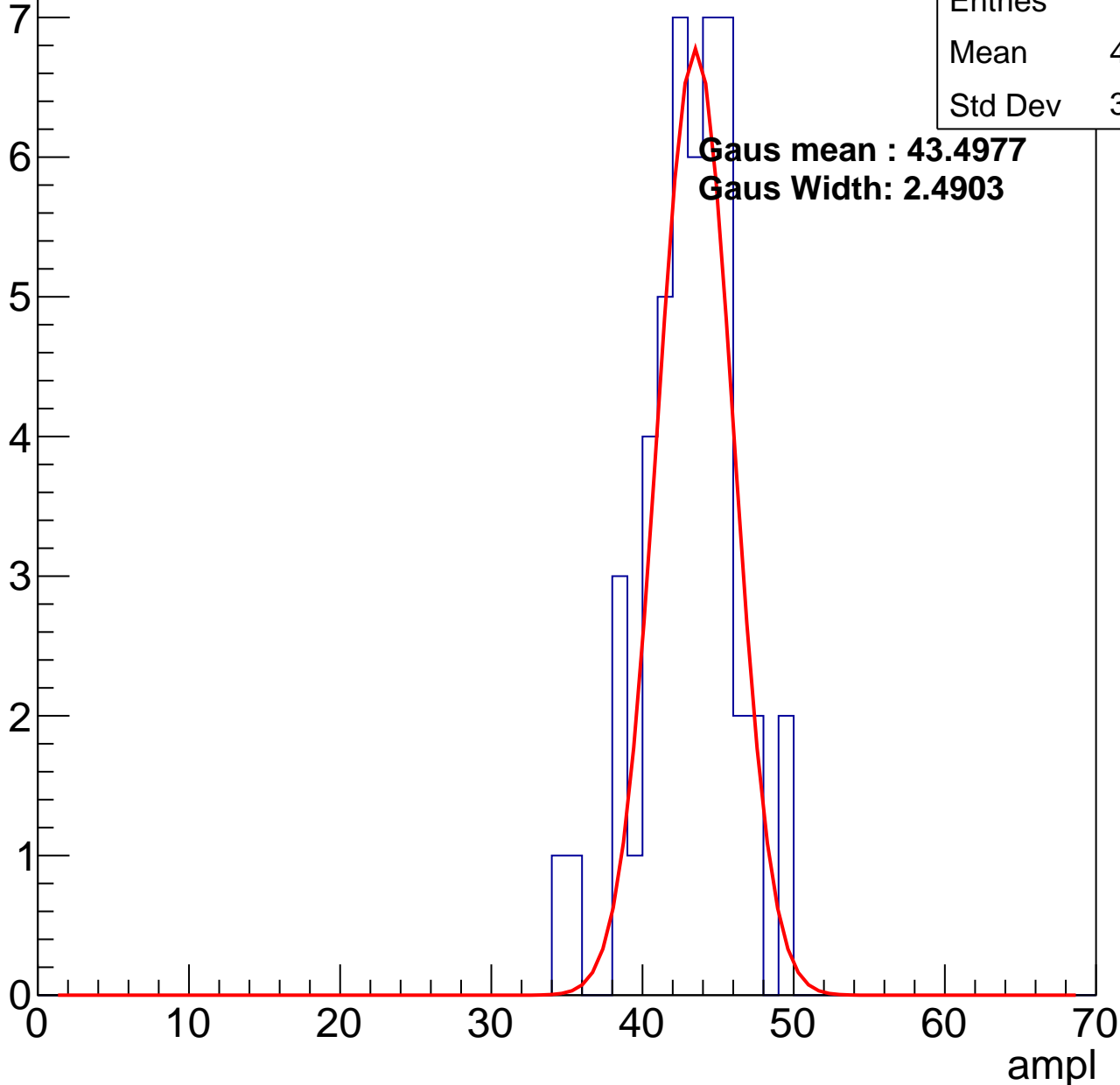
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	42.62
Std Dev	3.059

**Gaus mean : 43.4977**

**Gaus Width: 2.4903**

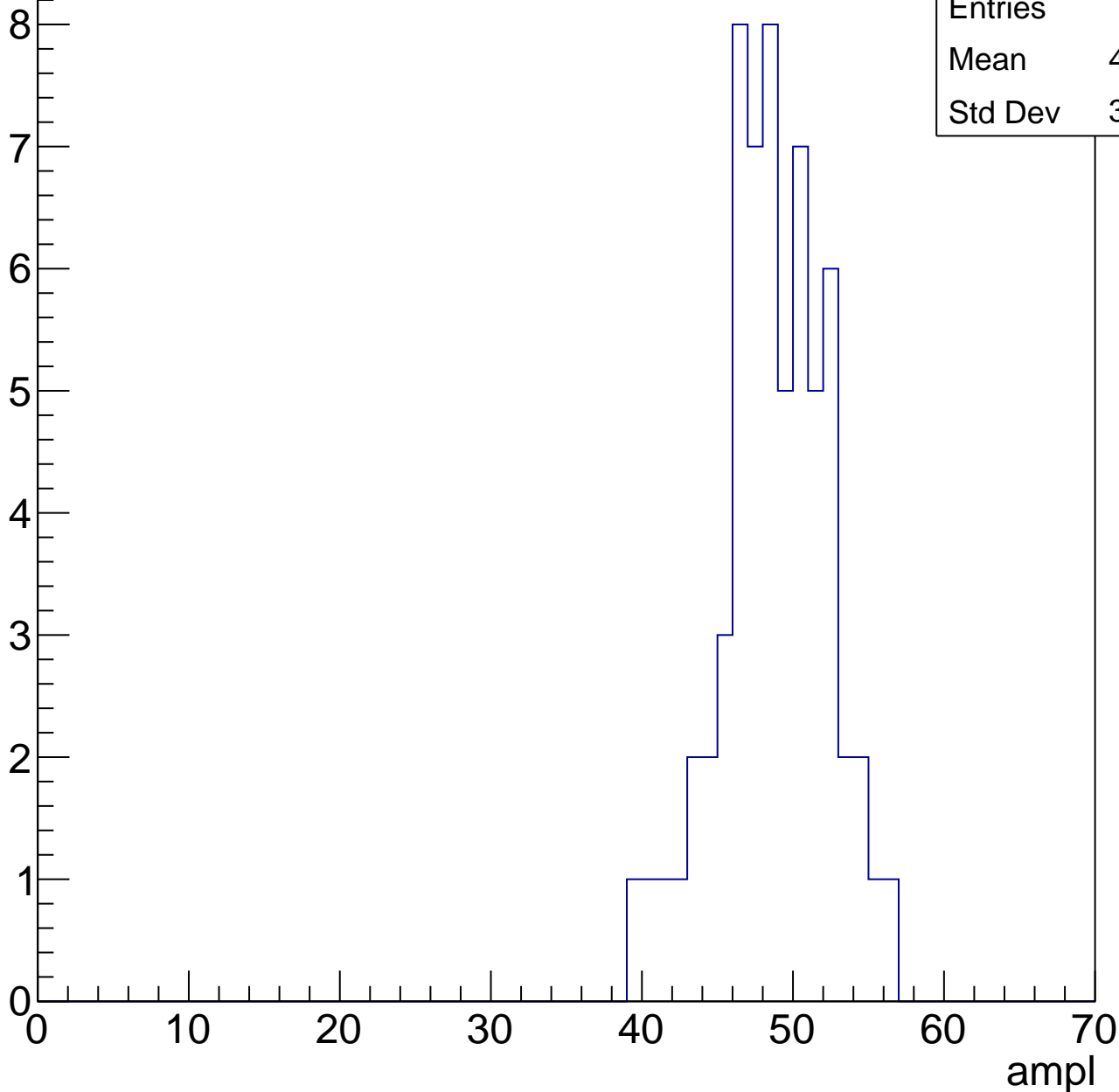


# B1L101S, U3-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

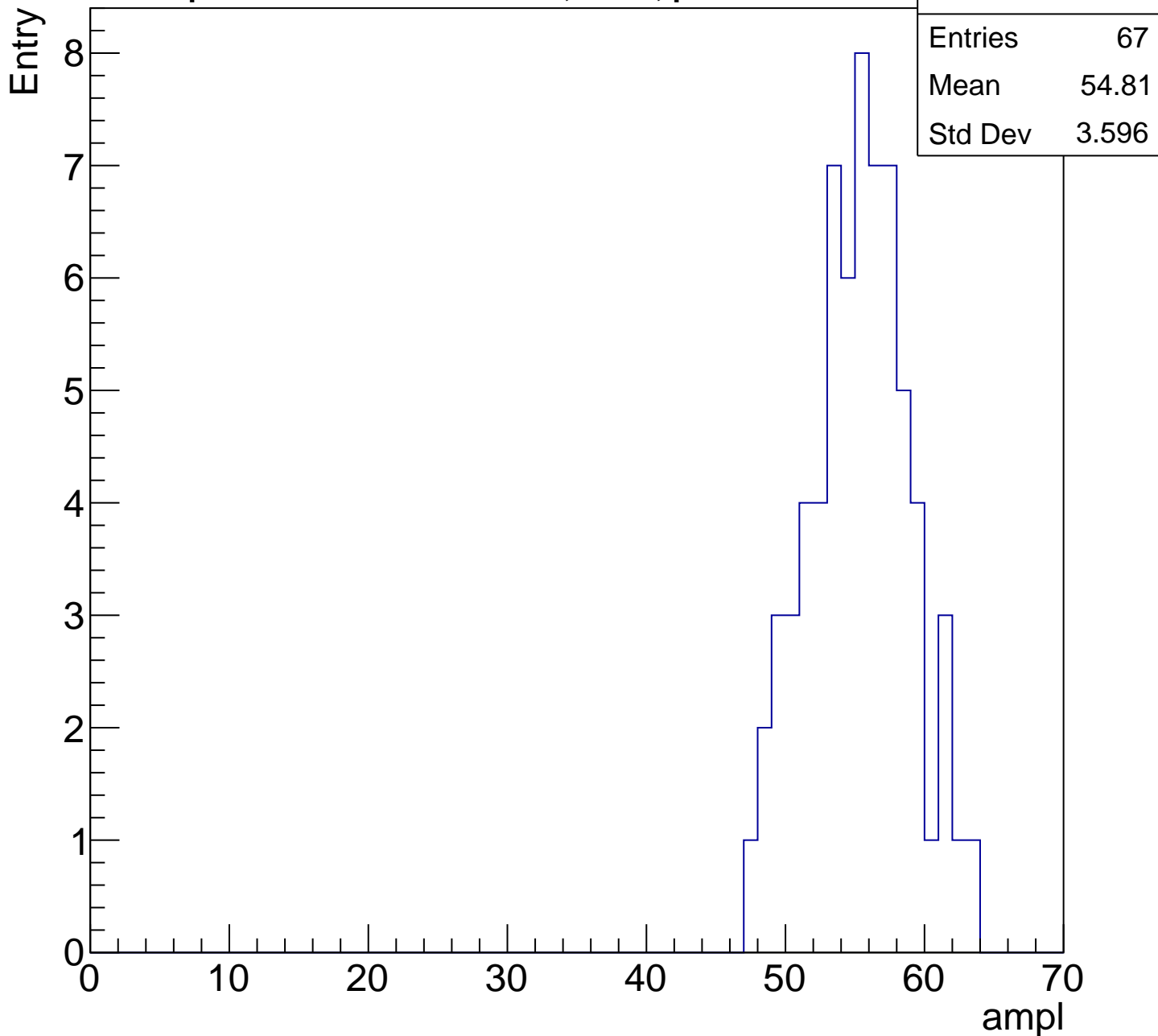
Entry

Entries	63
Mean	48.24
Std Dev	3.526



# B1L101S, U3-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch91, adc5

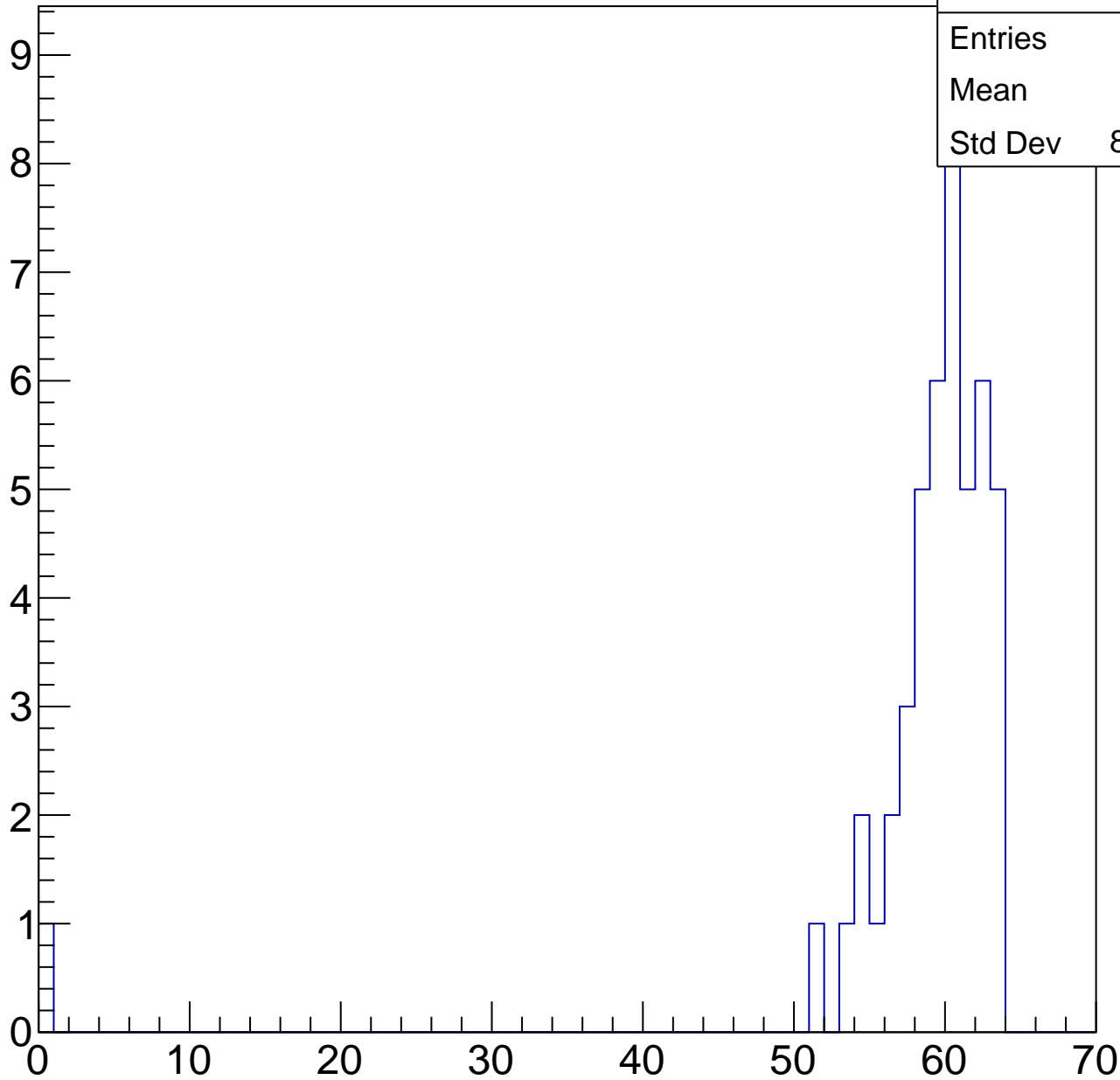
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	47
Mean	58
Std Dev	8.989

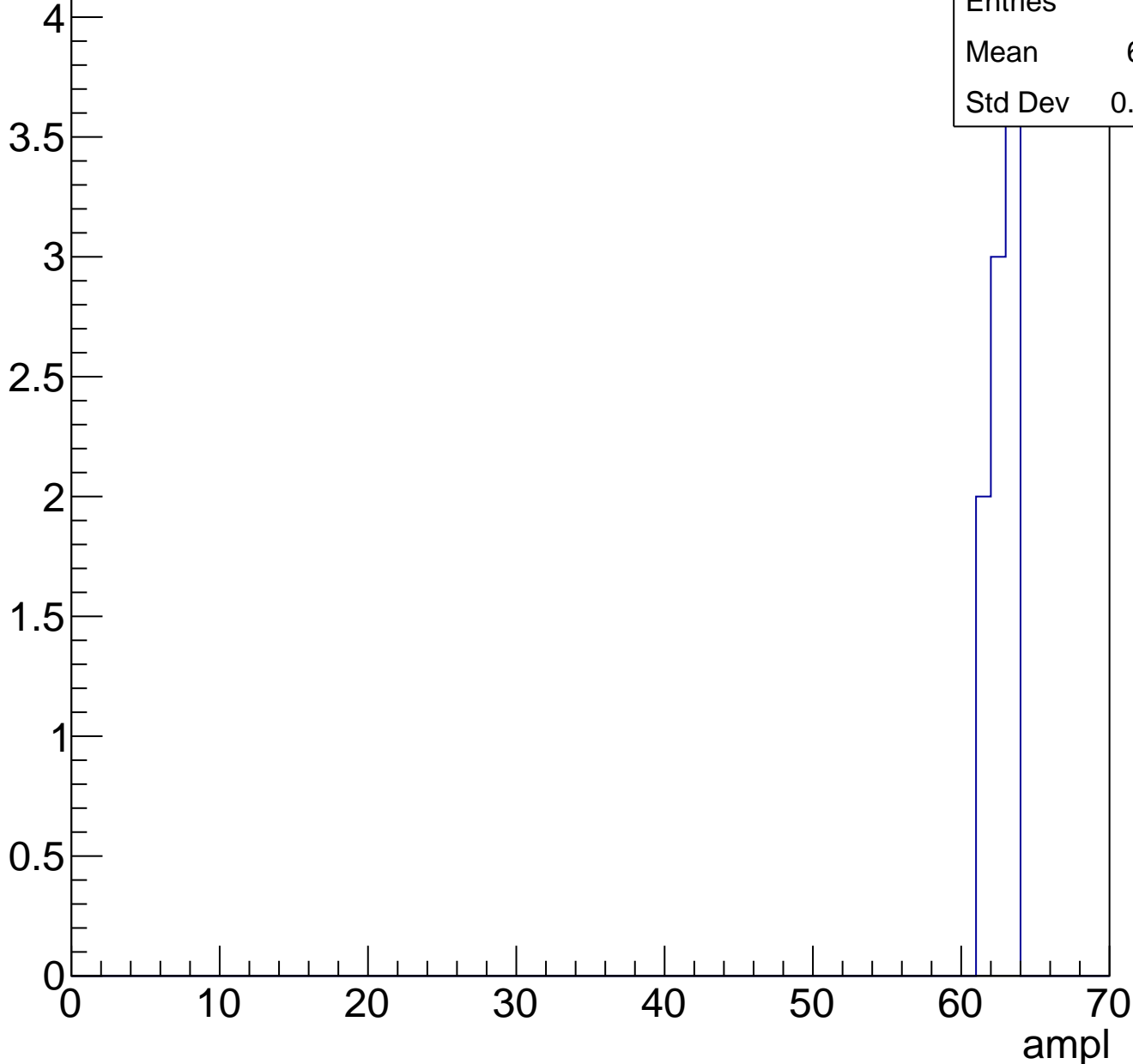
ampl



# B1L101S, U3-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch92, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	76
Mean	28.34
Std Dev	6.622

**Gaus mean : 29.8217**

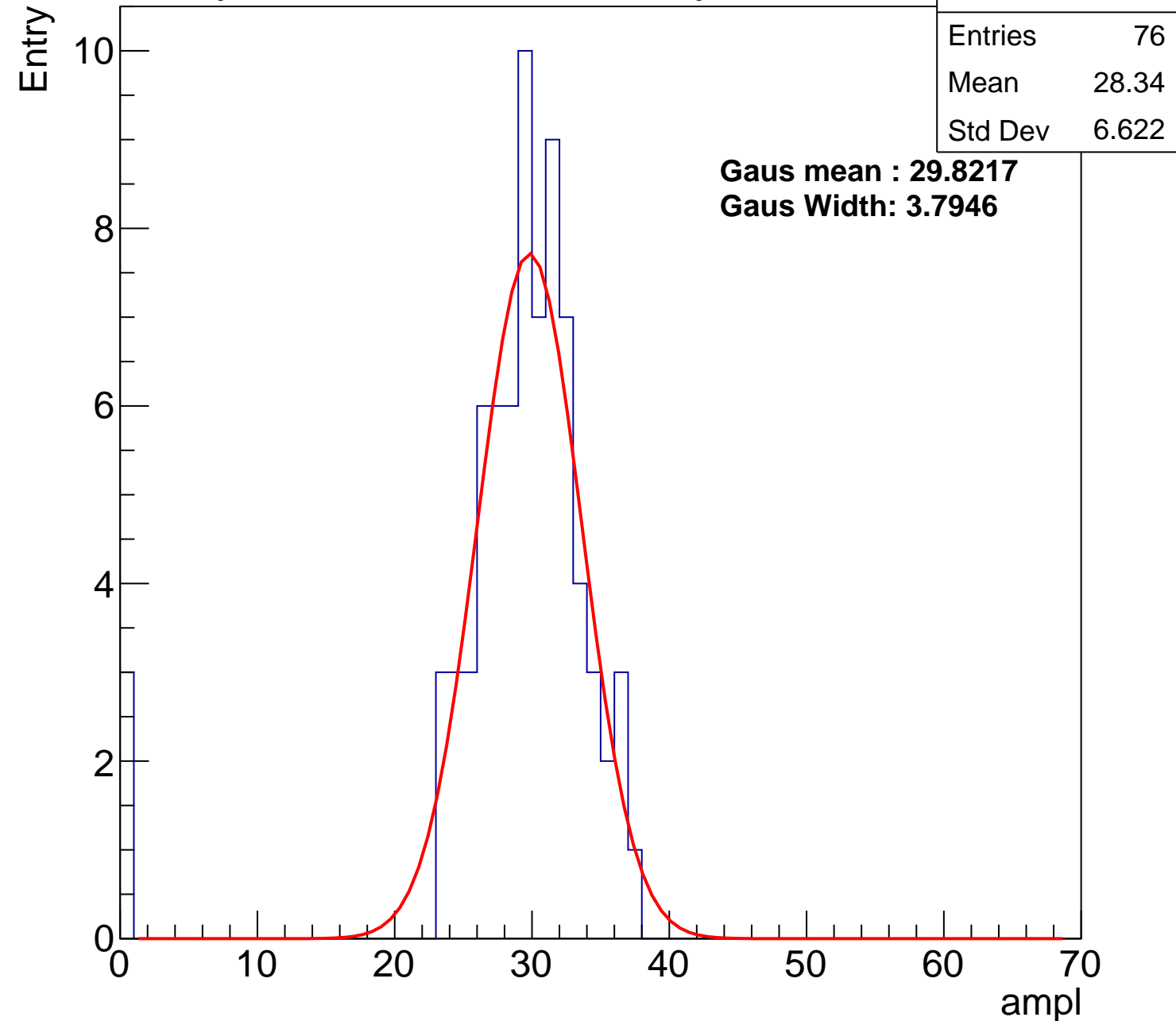
**Gaus Width: 3.7946**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U3-ch92, adc1

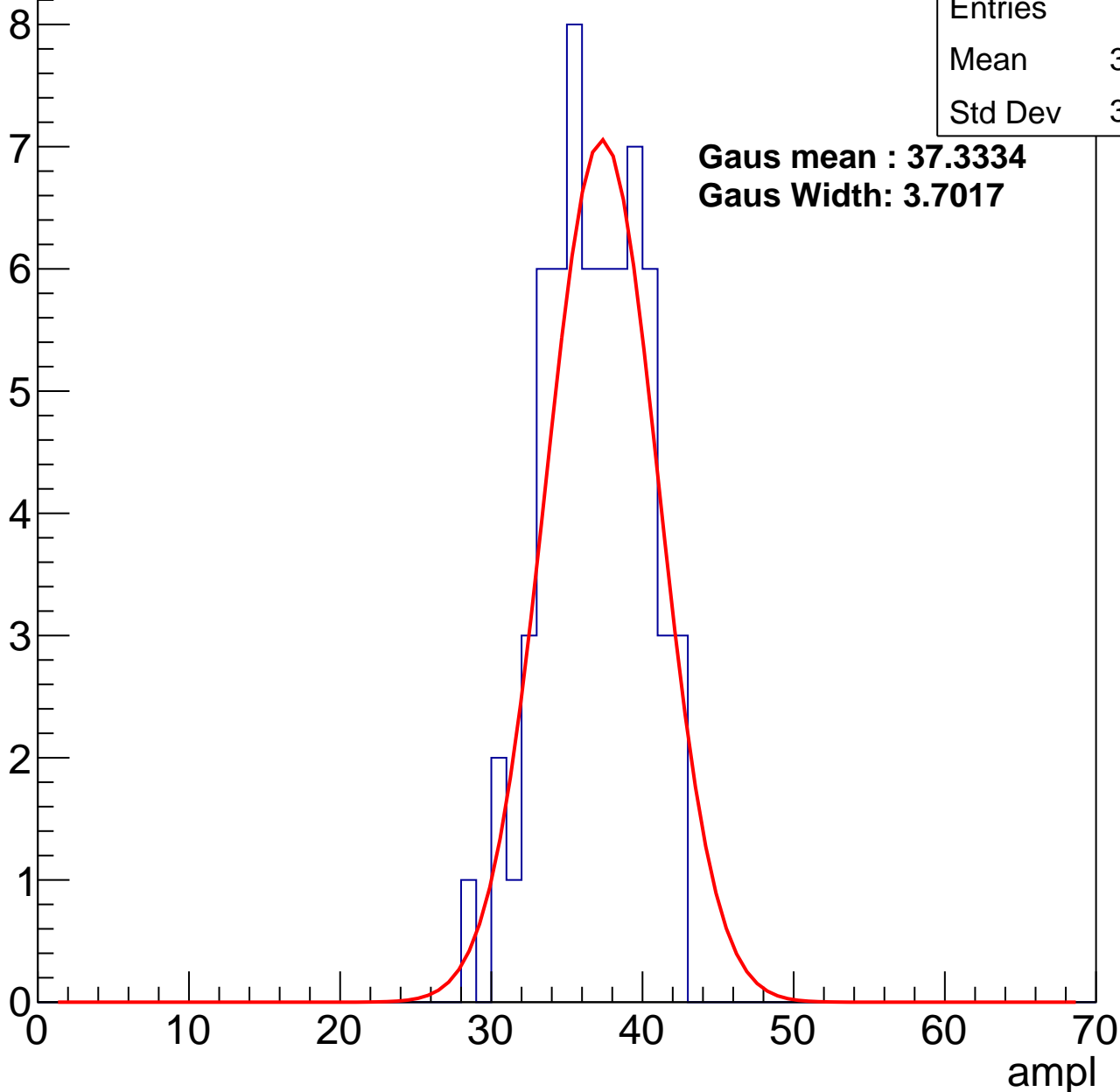
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	36.33
Std Dev	3.212

**Gaus mean : 37.3334**

**Gaus Width: 3.7017**



# B1L101S, U3-ch92, adc2

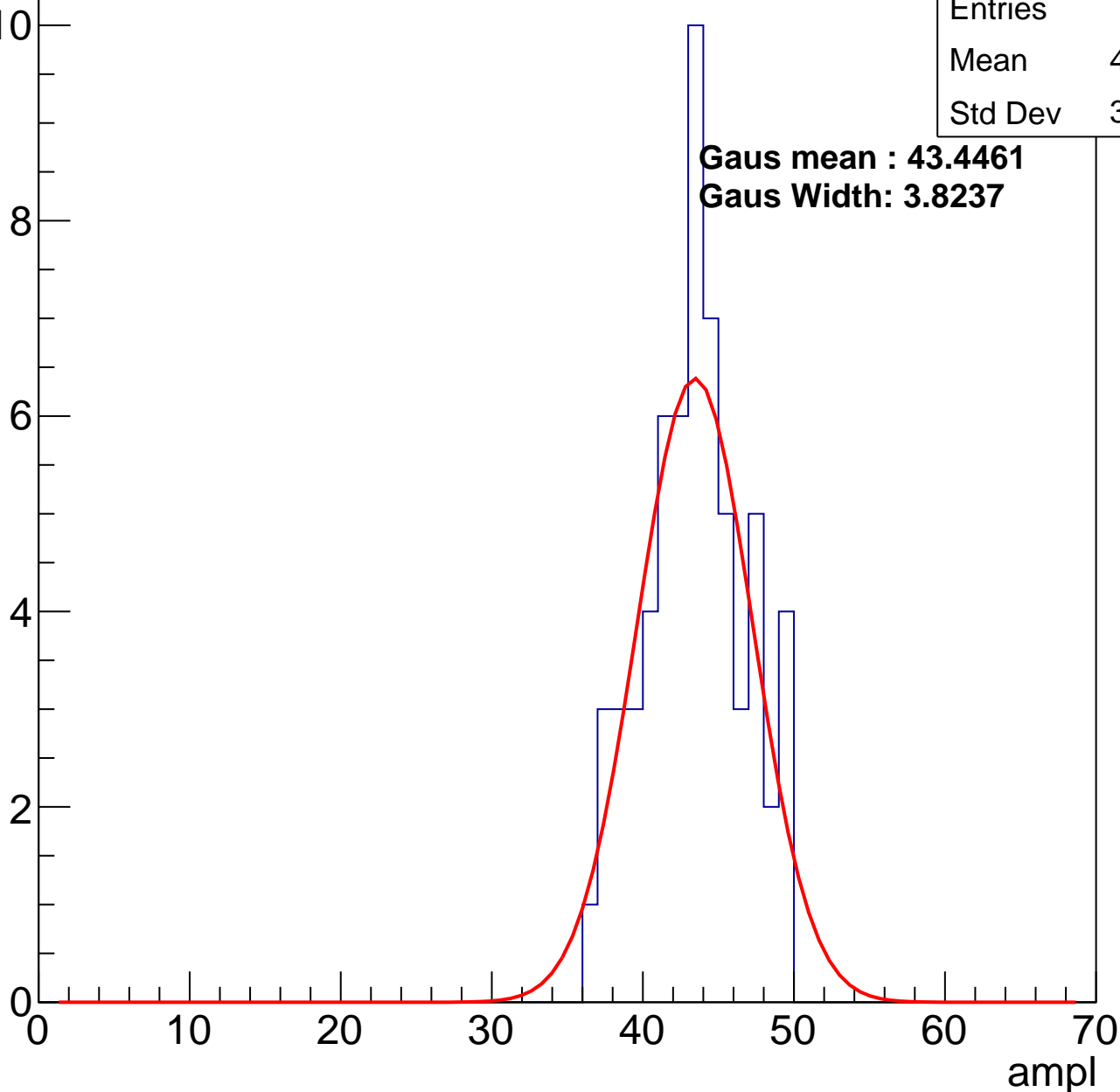
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	42.97
Std Dev	3.297

**Gaus mean : 43.4461**

**Gaus Width: 3.8237**

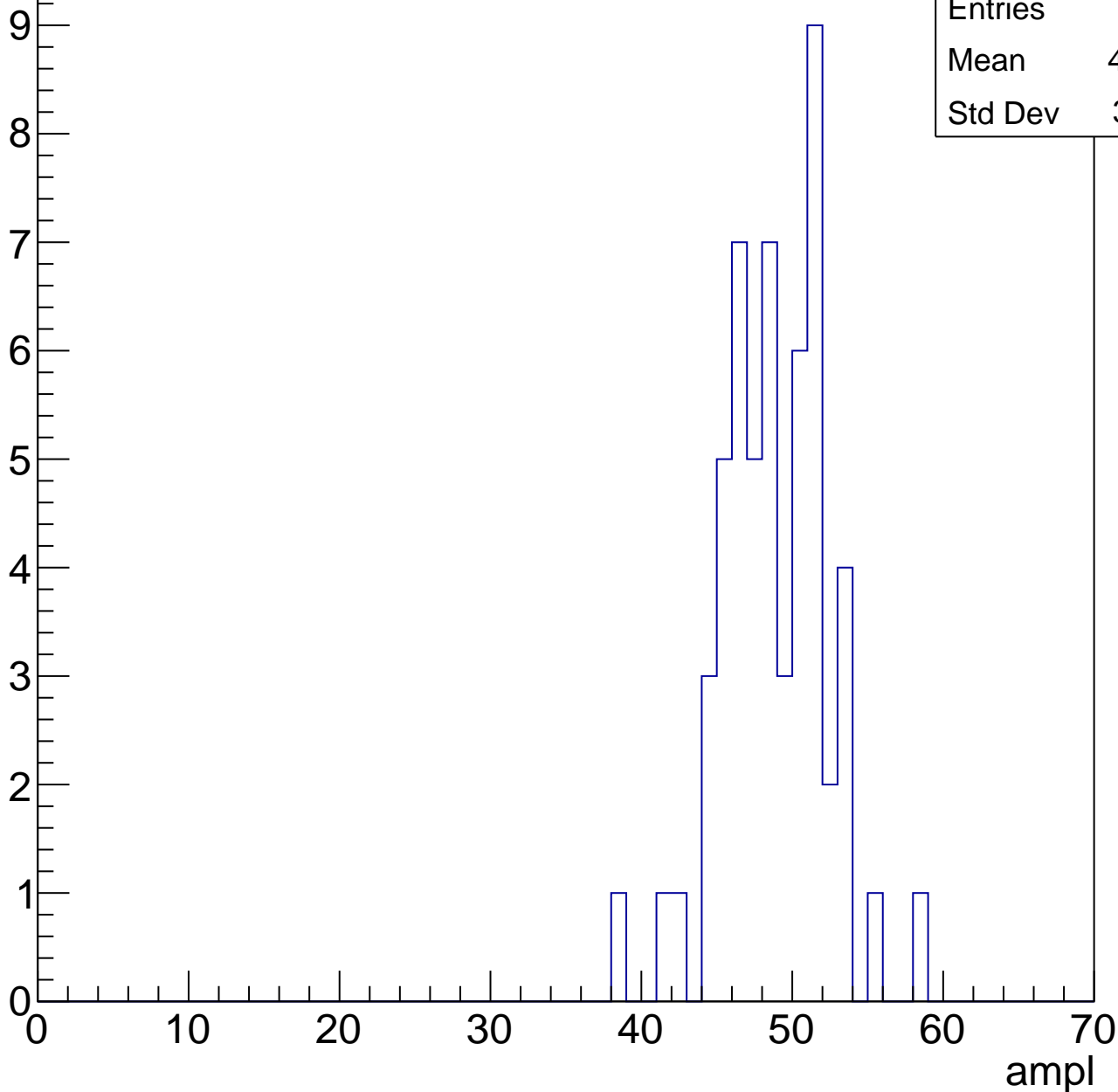


# B1L101S, U3-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	48.32
Std Dev	3.521

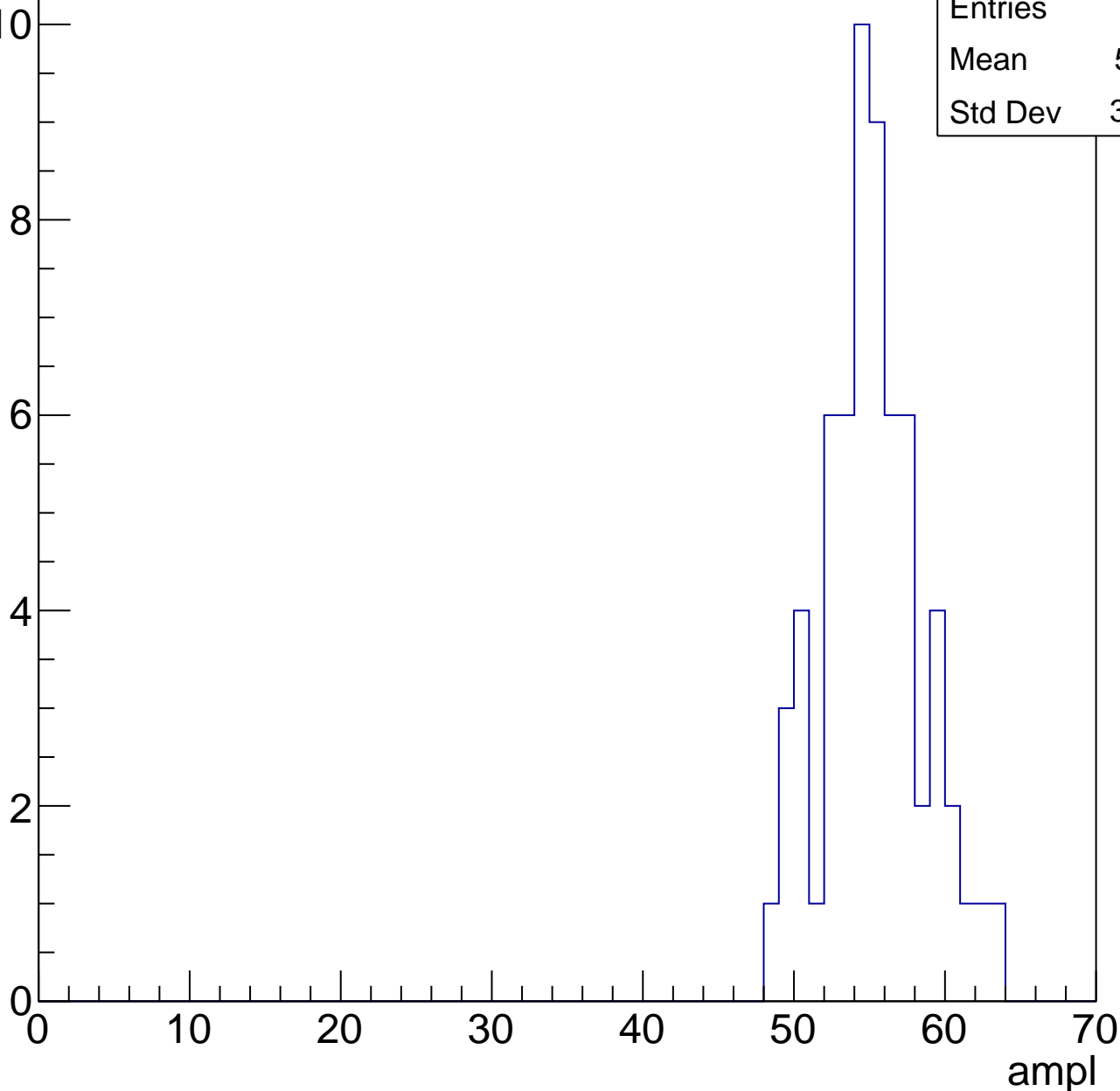


# B1L101S, U3-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	54.71
Std Dev	3.253



# B1L101S, U3-ch92, adc5

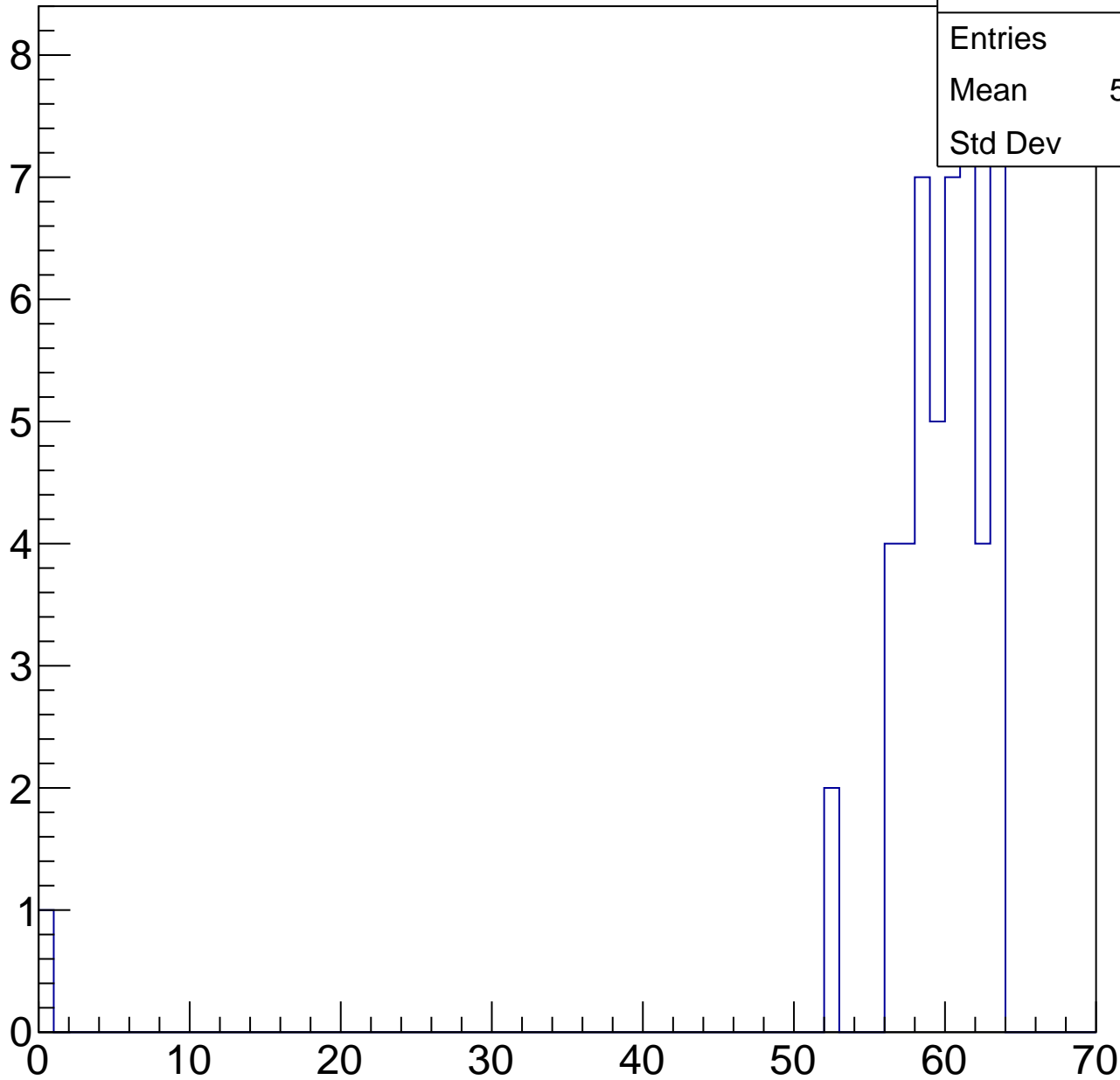
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	50
Mean	58.34
Std Dev	8.74

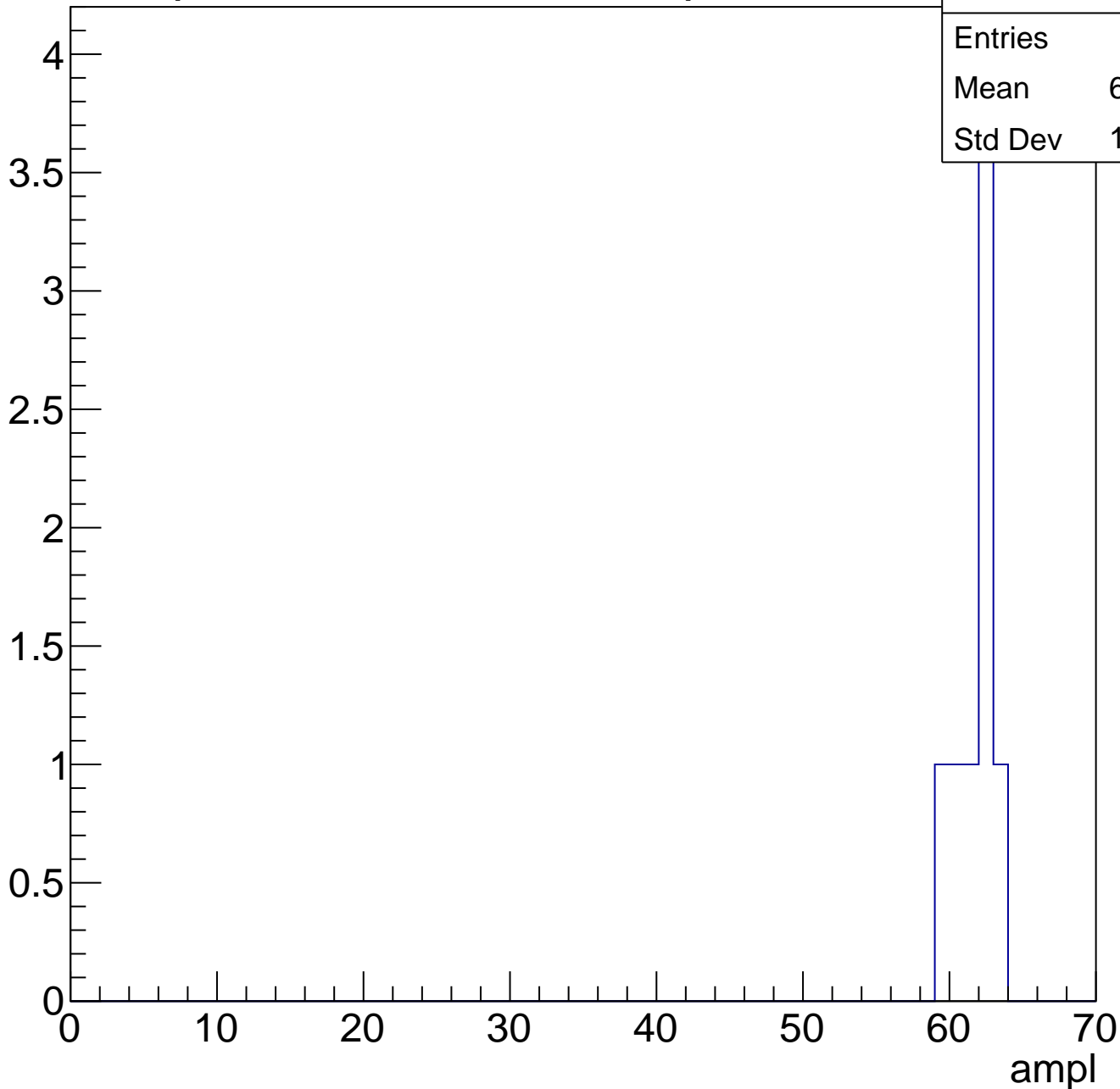
ampl



# B1L101S, U3-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch93, adc0

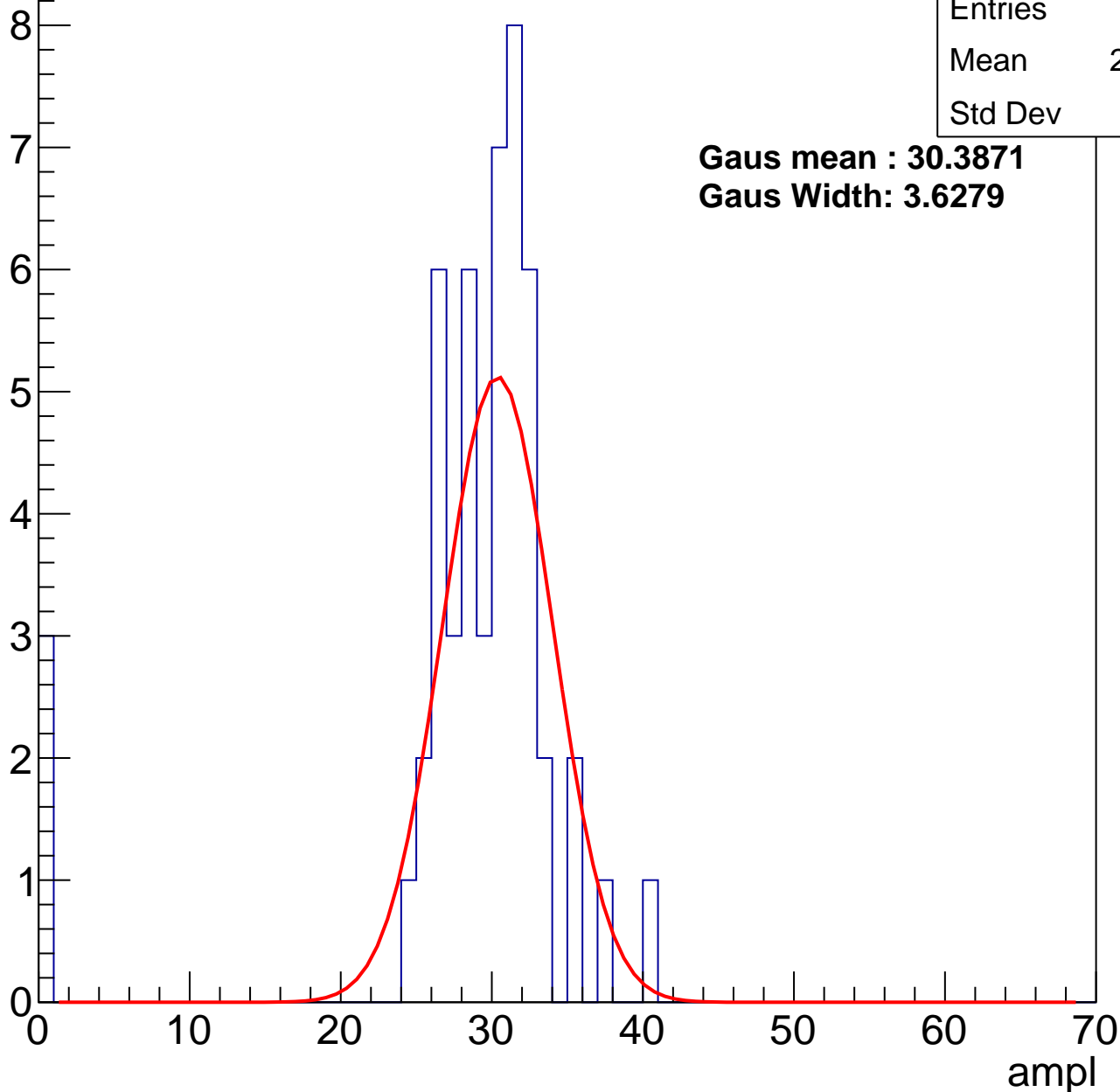
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	28.02
Std Dev	7.65

**Gaus mean : 30.3871**

**Gaus Width: 3.6279**



# B1L101S, U3-ch93, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	59
Mean	34.51
Std Dev	3.347

**Gaus mean : 35.7275**

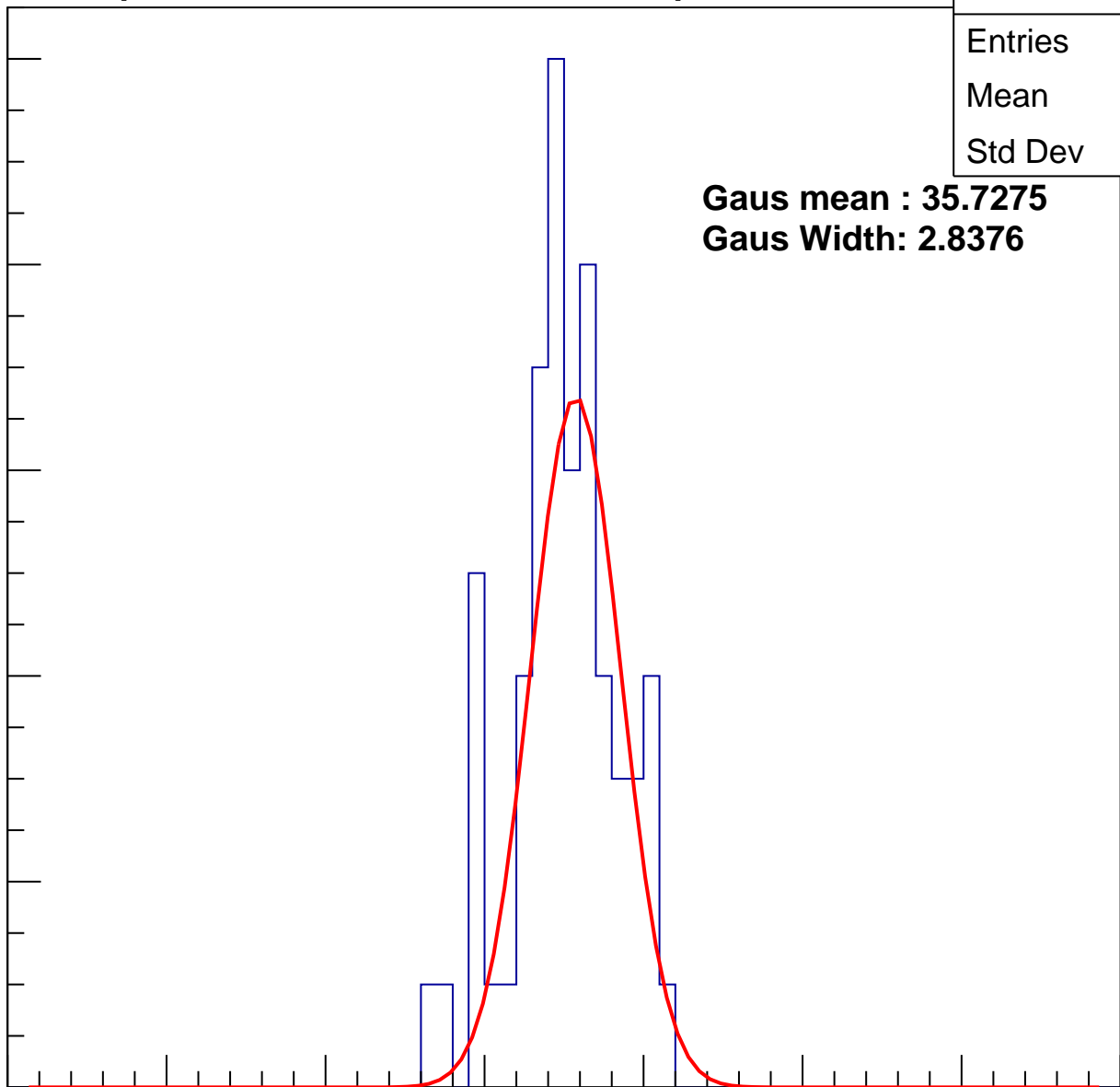
**Gaus Width: 2.8376**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U3-ch93, adc2

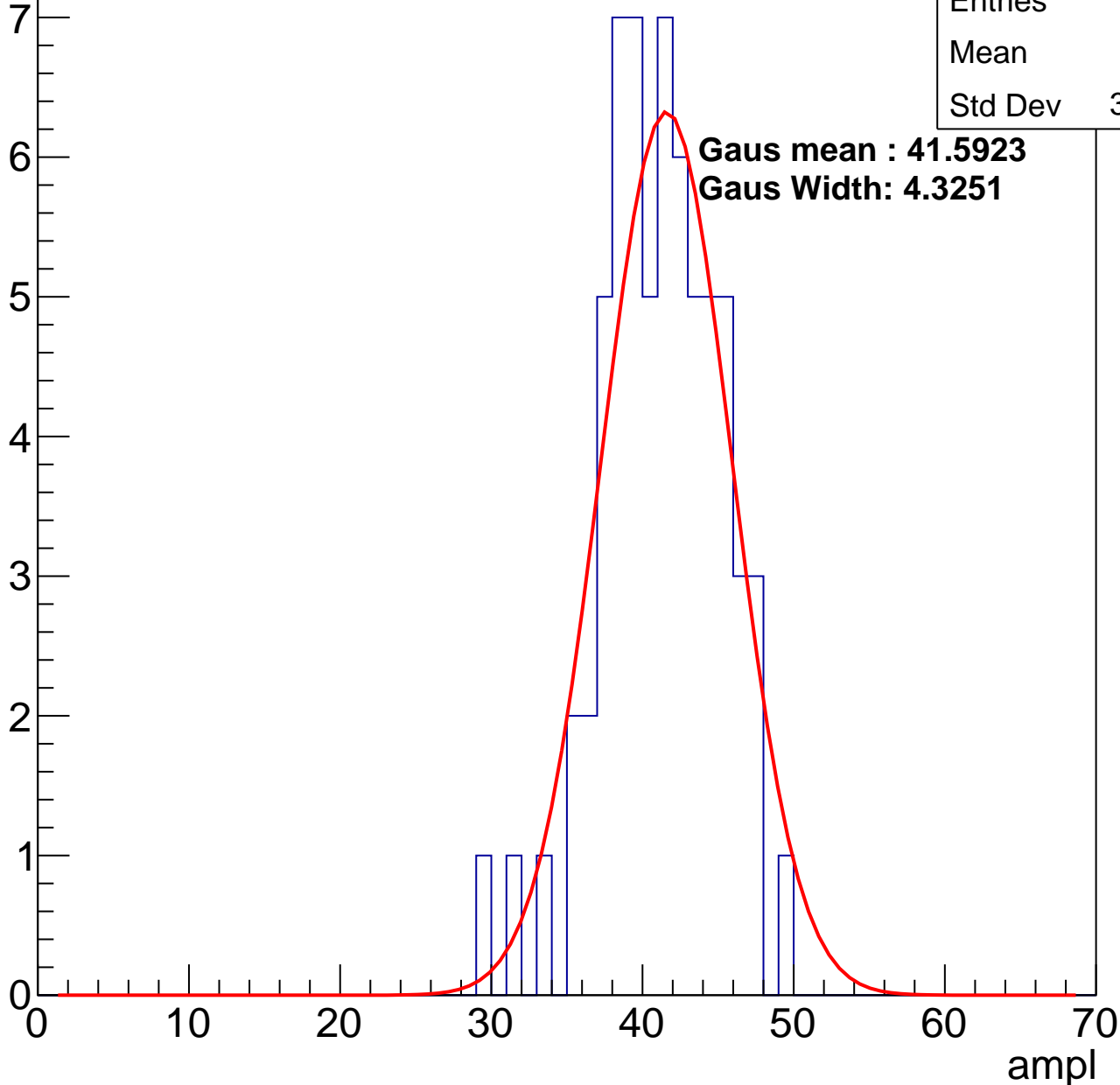
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	40.7
Std Dev	3.888

**Gaus mean : 41.5923**

**Gaus Width: 4.3251**

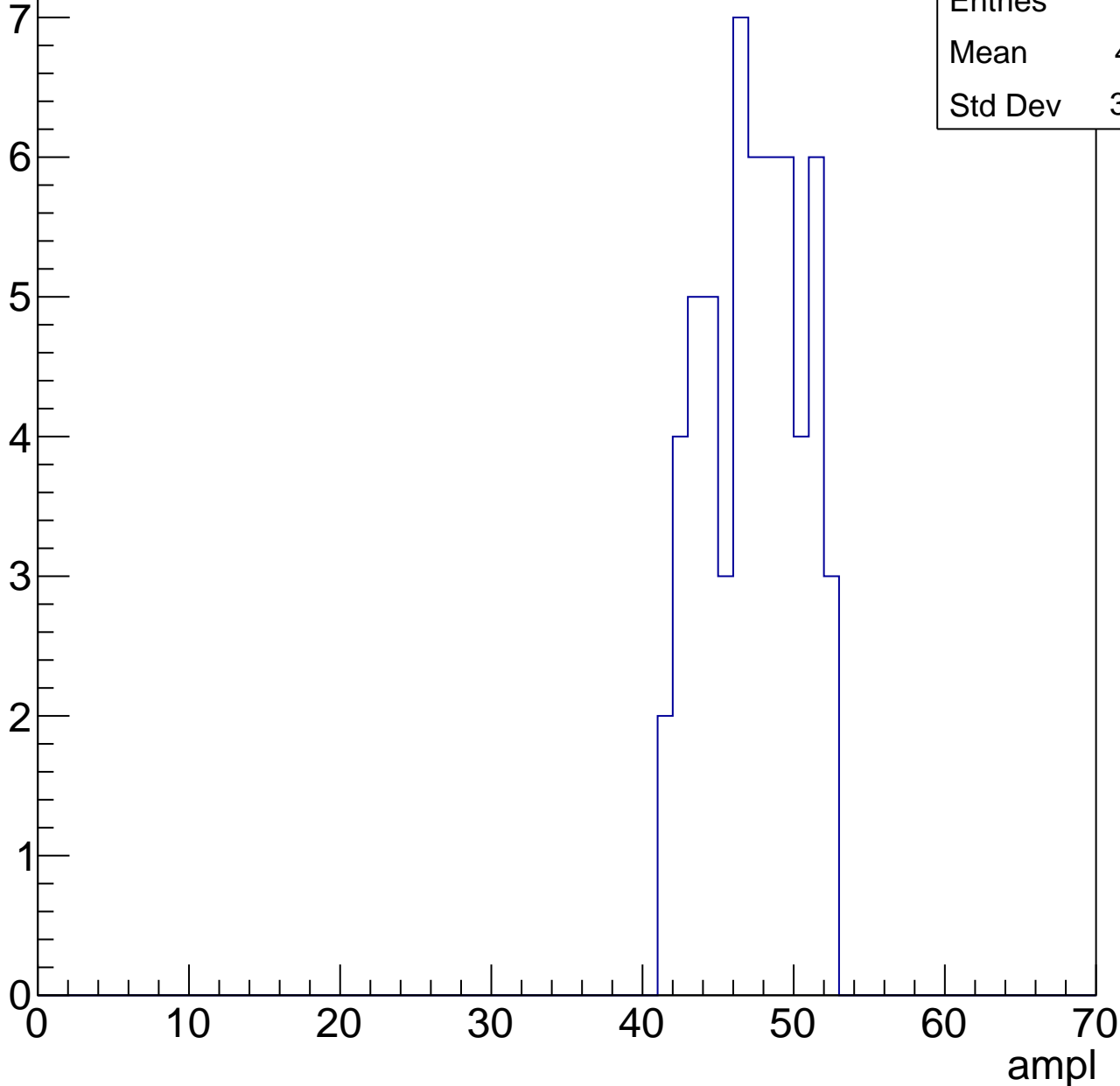


# B1L101S, U3-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	46.81
Std Dev	3.109

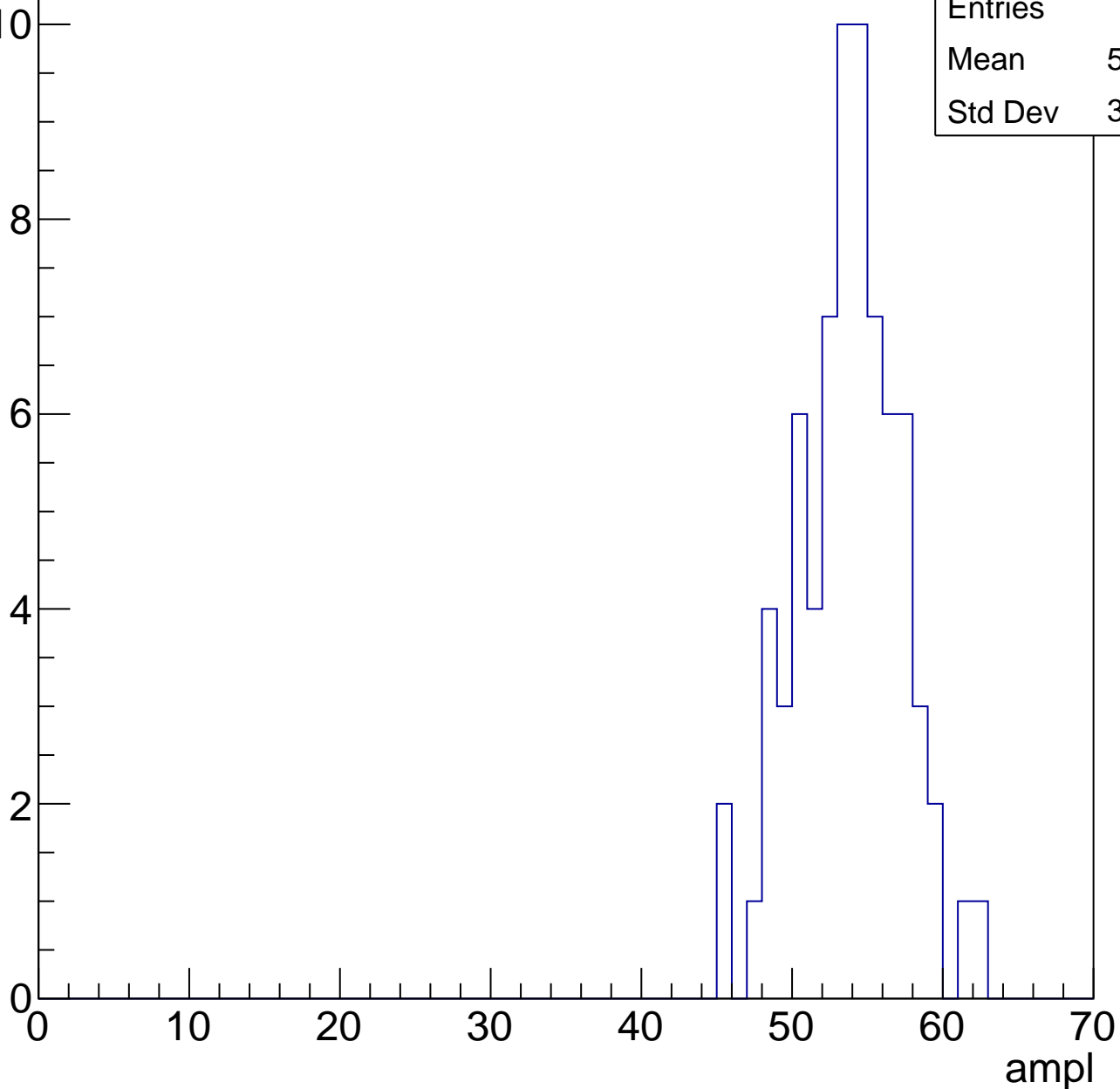


# B1L101S, U3-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	53.32
Std Dev	3.436

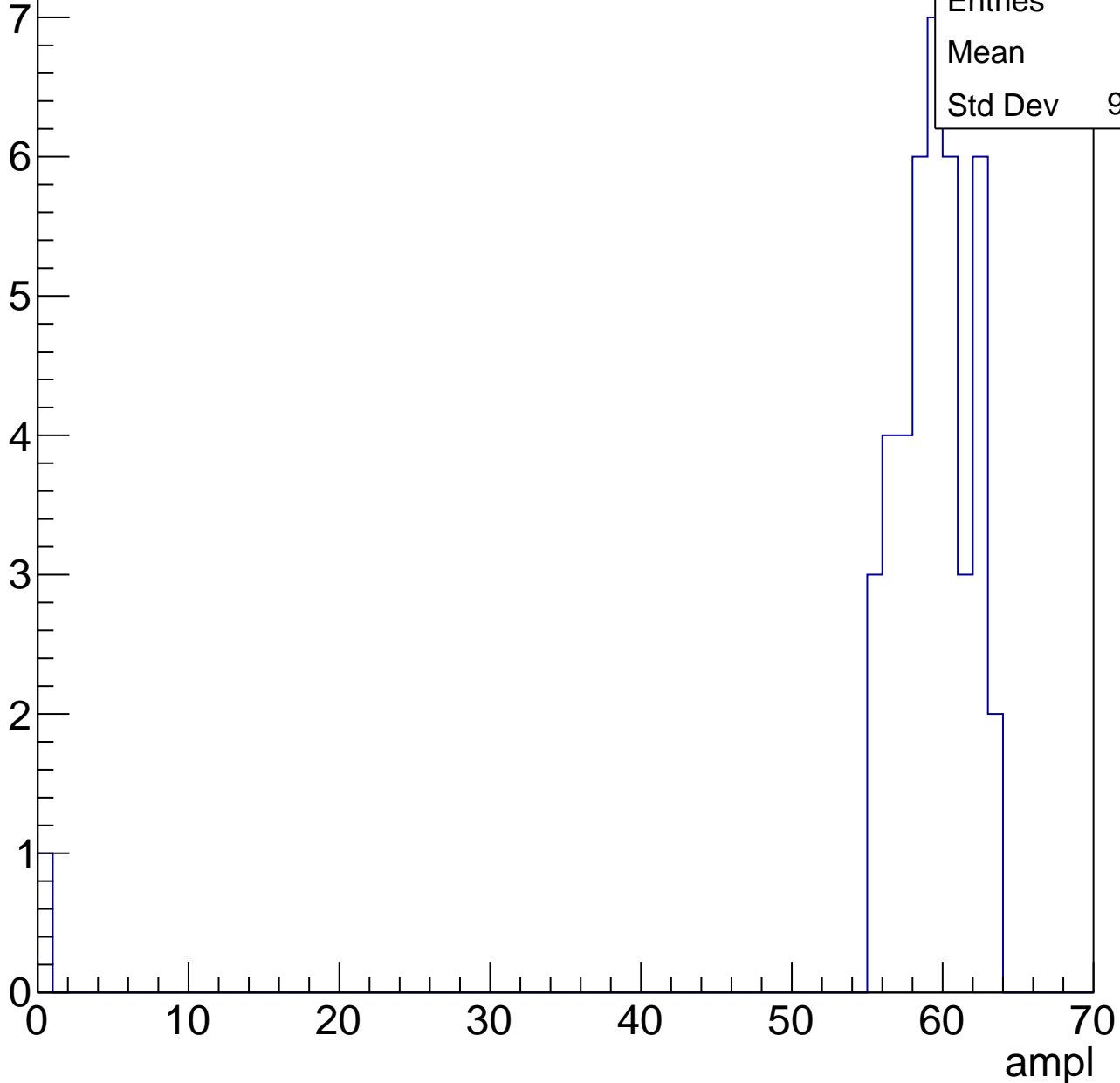


# B1L101S, U3-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	57.6
Std Dev	9.269

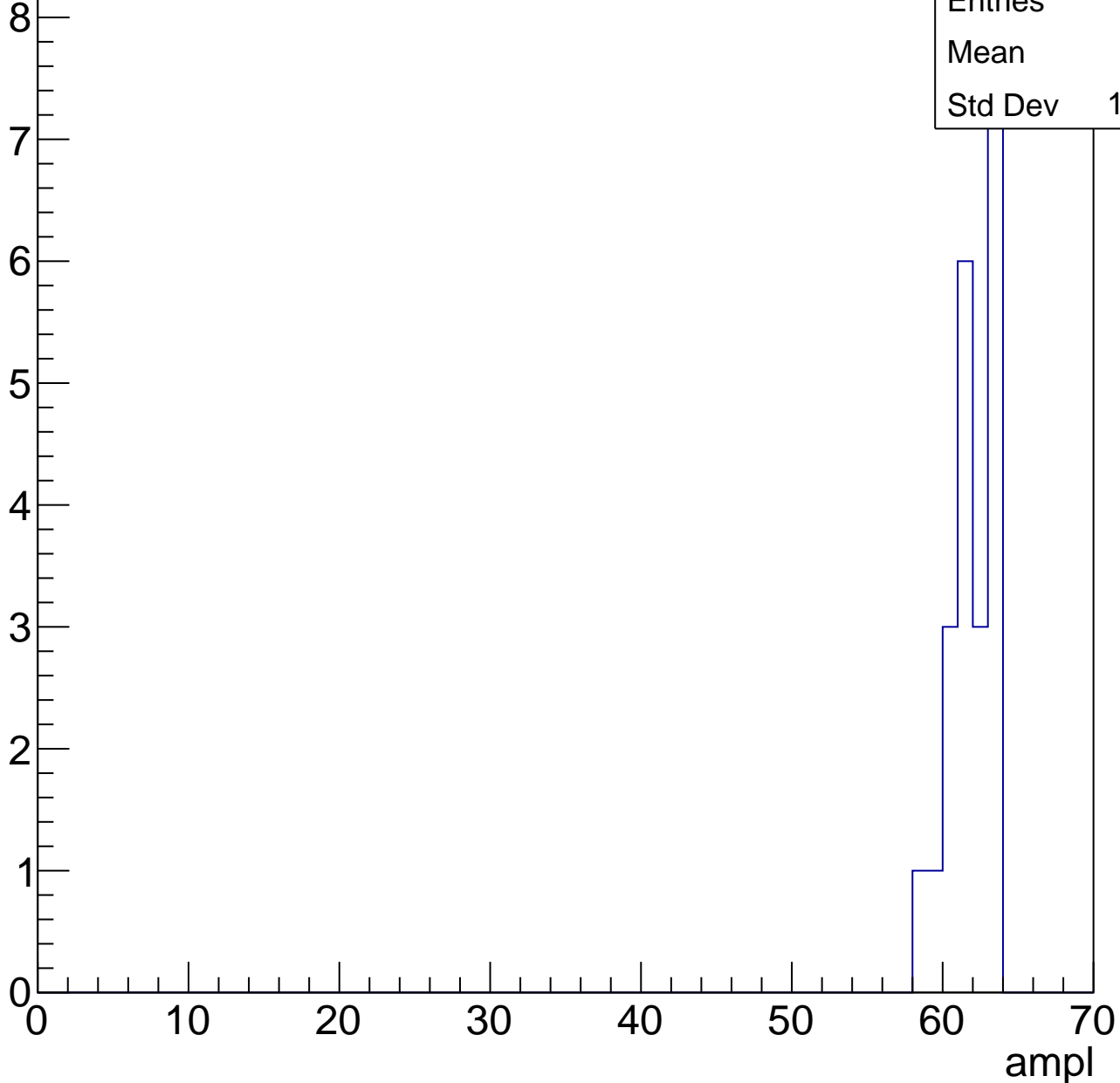


# B1L101S, U3-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	22
Mean	61.5
Std Dev	1.438

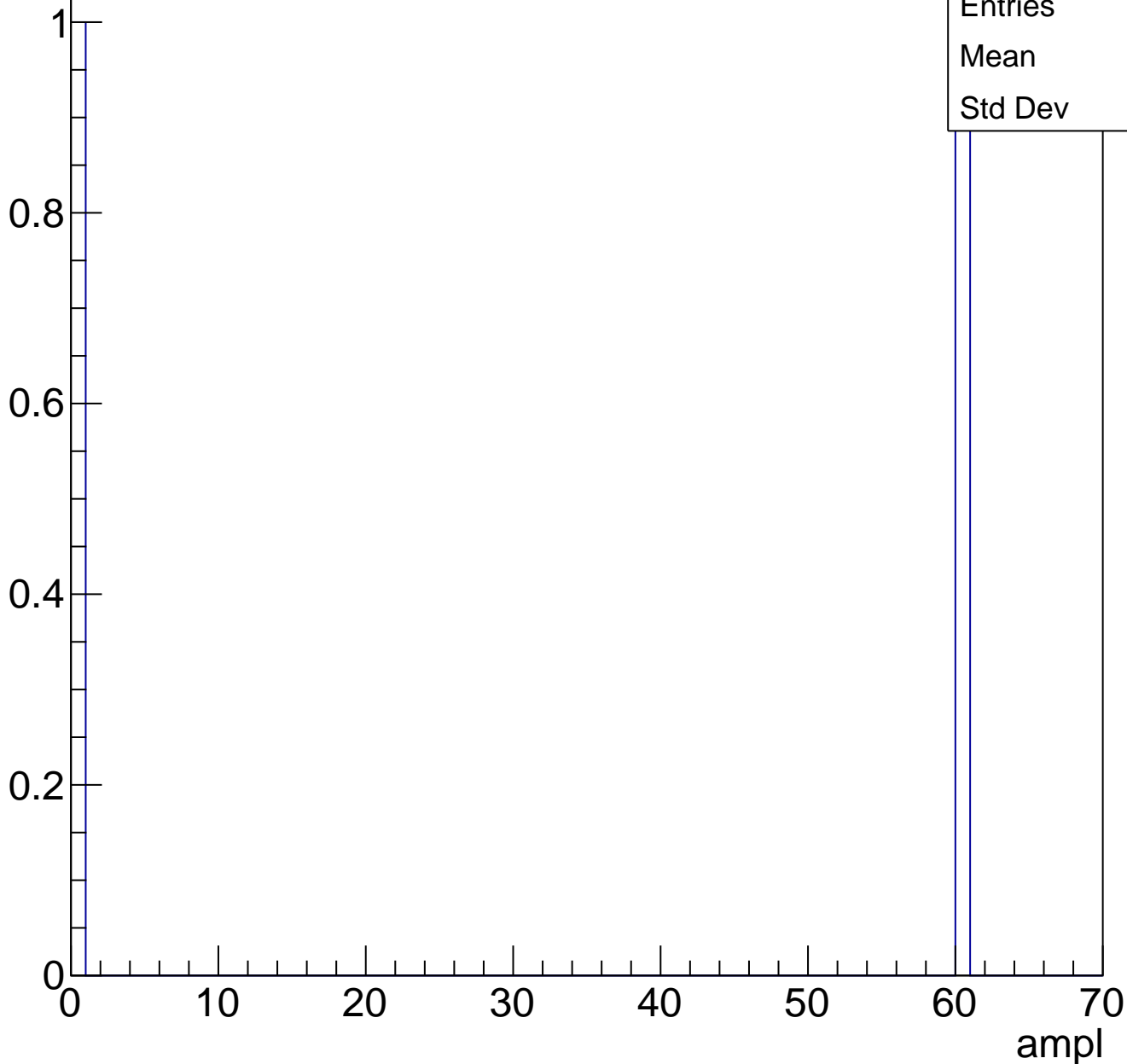




# B1L101S, U3-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch94, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	85
Mean	27.82
Std Dev	6.739

**Gaus mean : 29.2043**

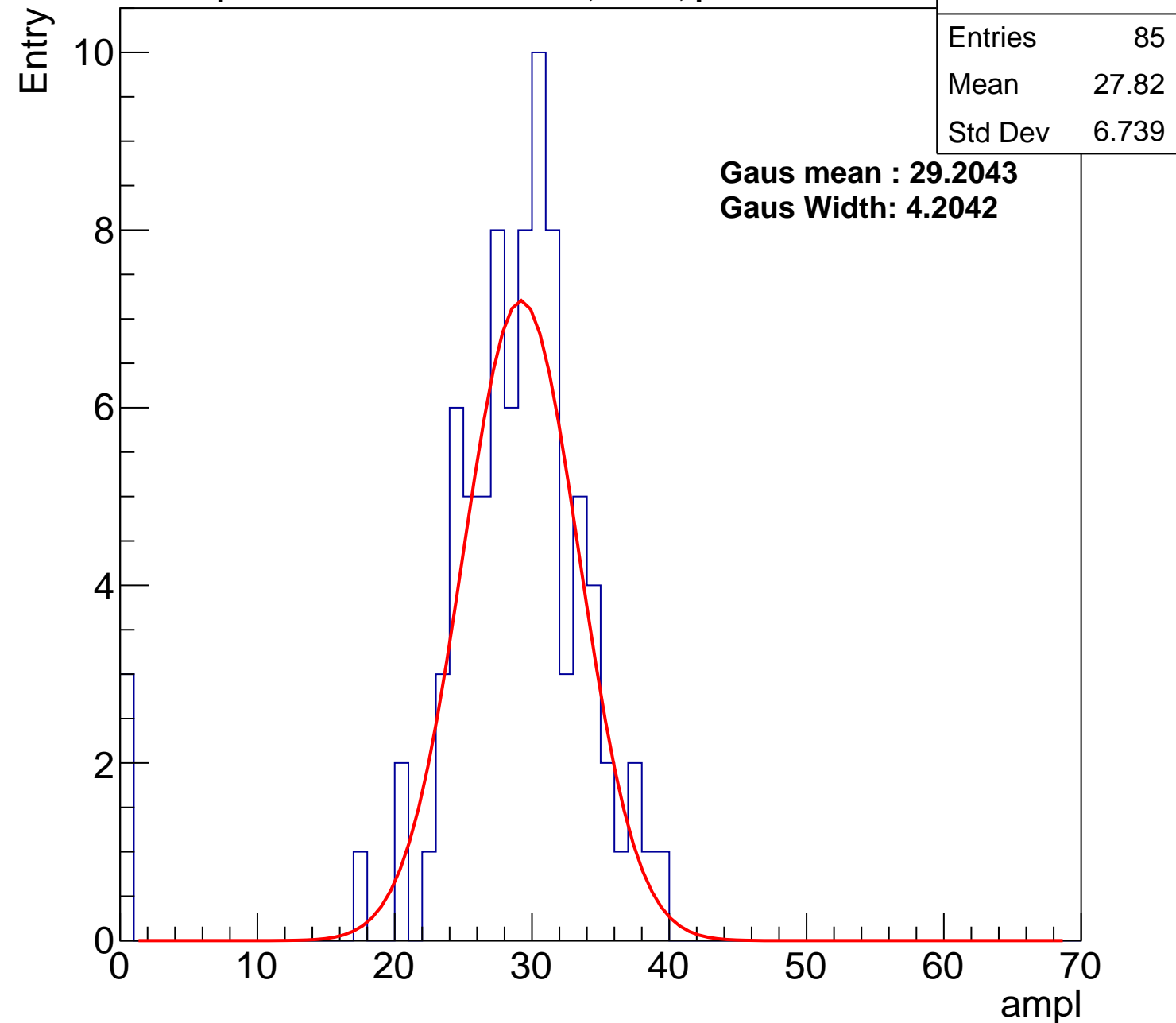
**Gaus Width: 4.2042**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U3-ch94, adc1

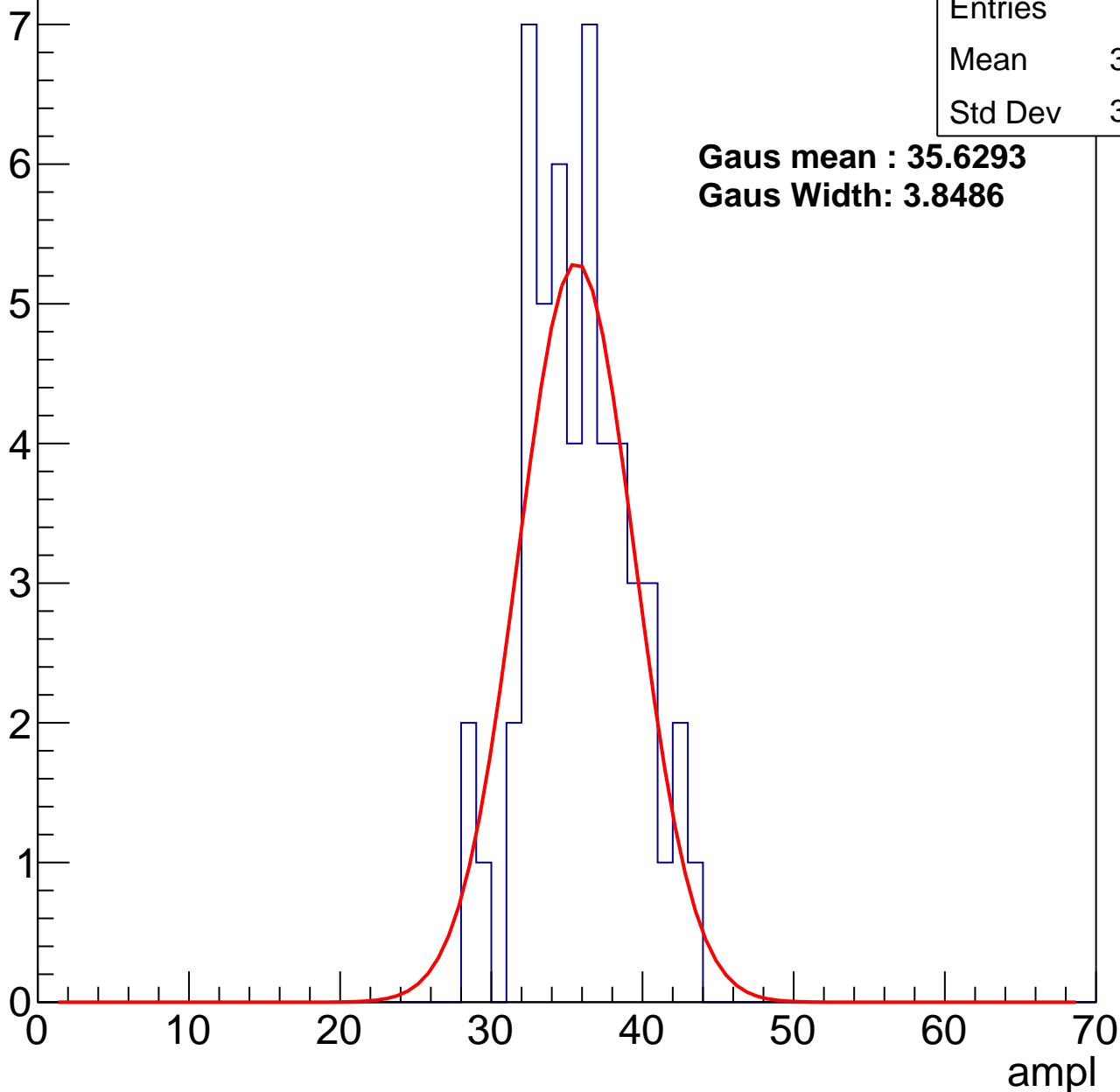
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	35.33
Std Dev	3.479

**Gaus mean : 35.6293**

**Gaus Width: 3.8486**



# B1L101S, U3-ch94, adc2

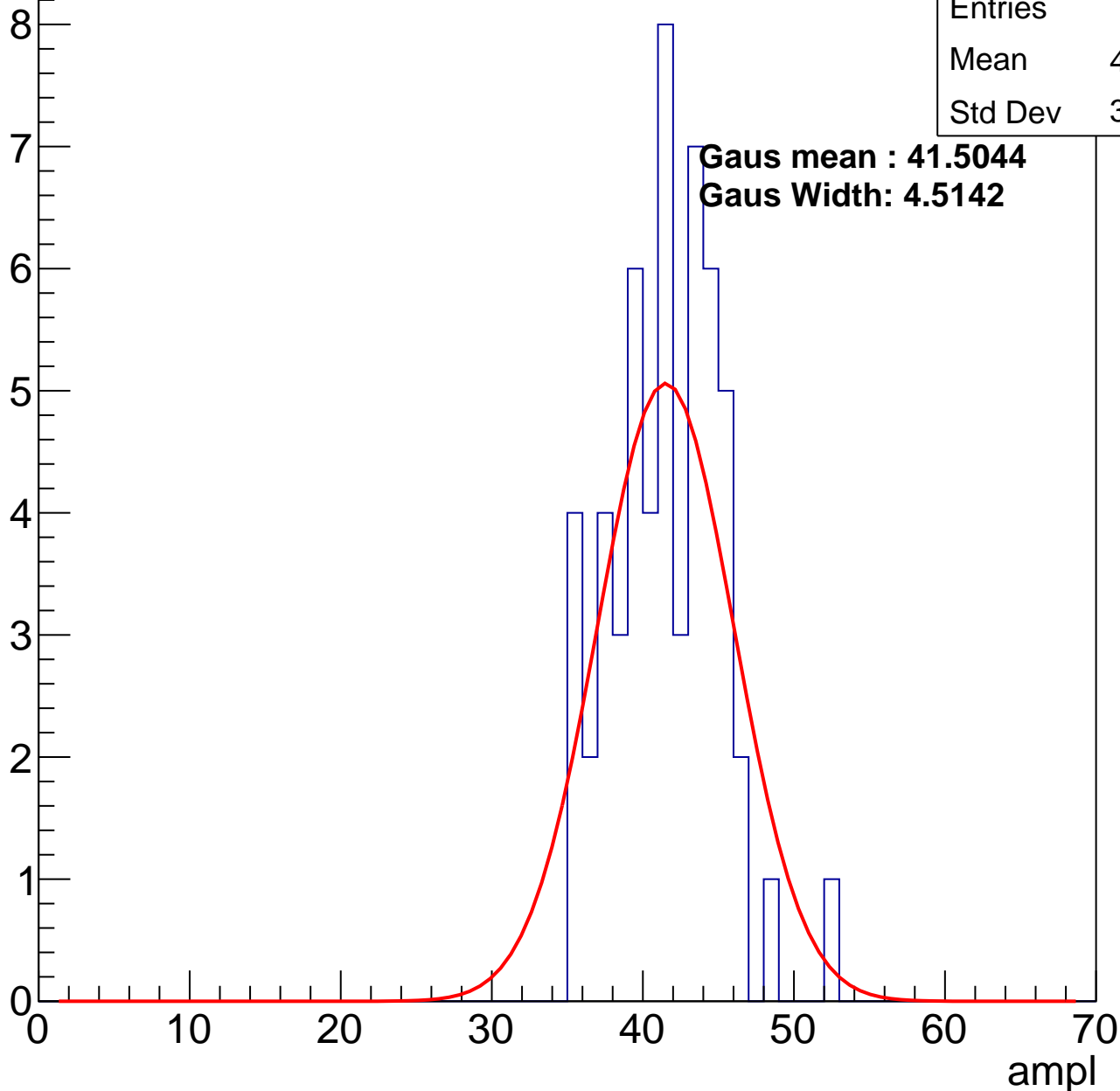
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	41.14
Std Dev	3.528

**Gaus mean : 41.5044**

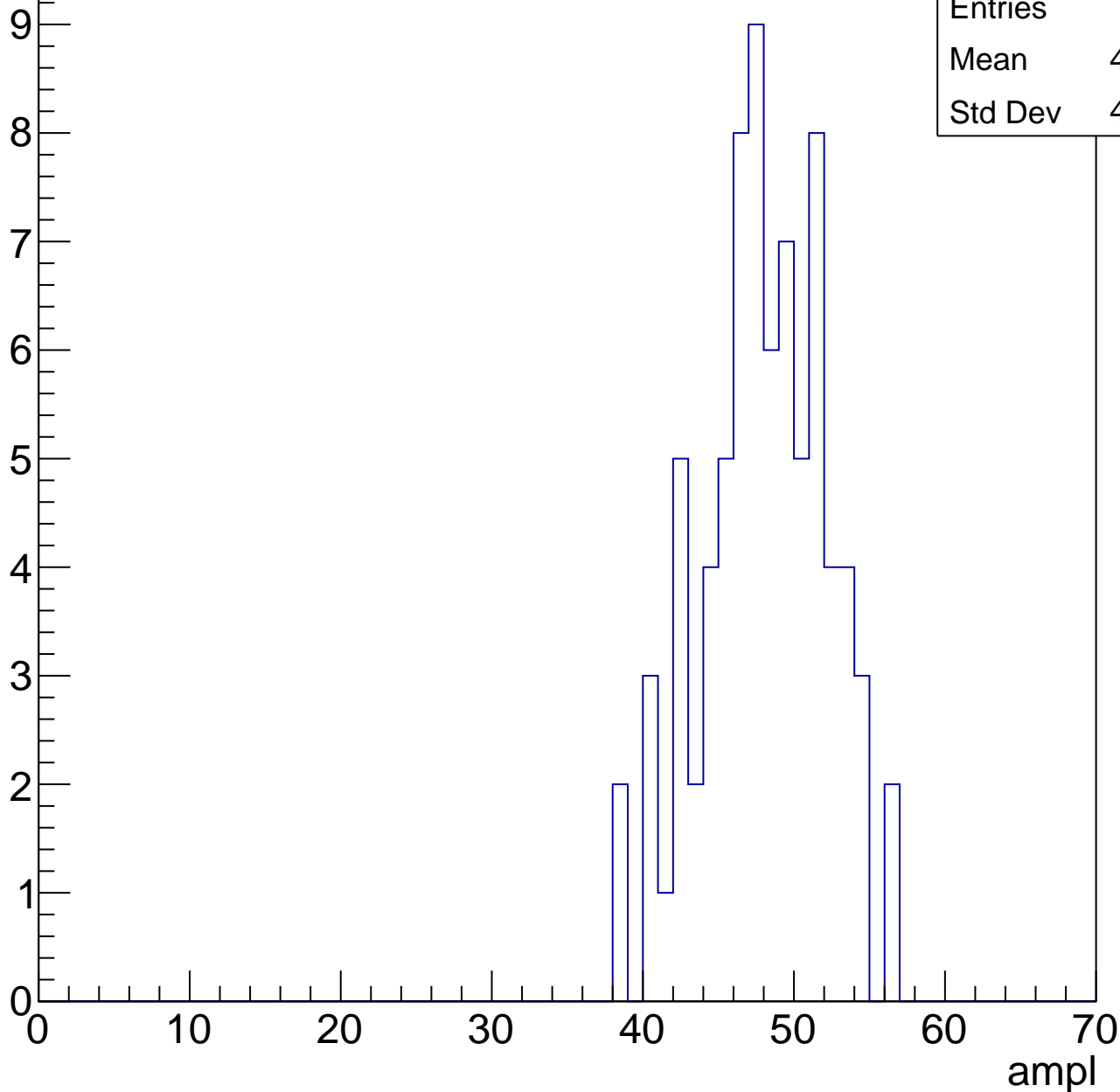
**Gaus Width: 4.5142**



# B1L101S, U3-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

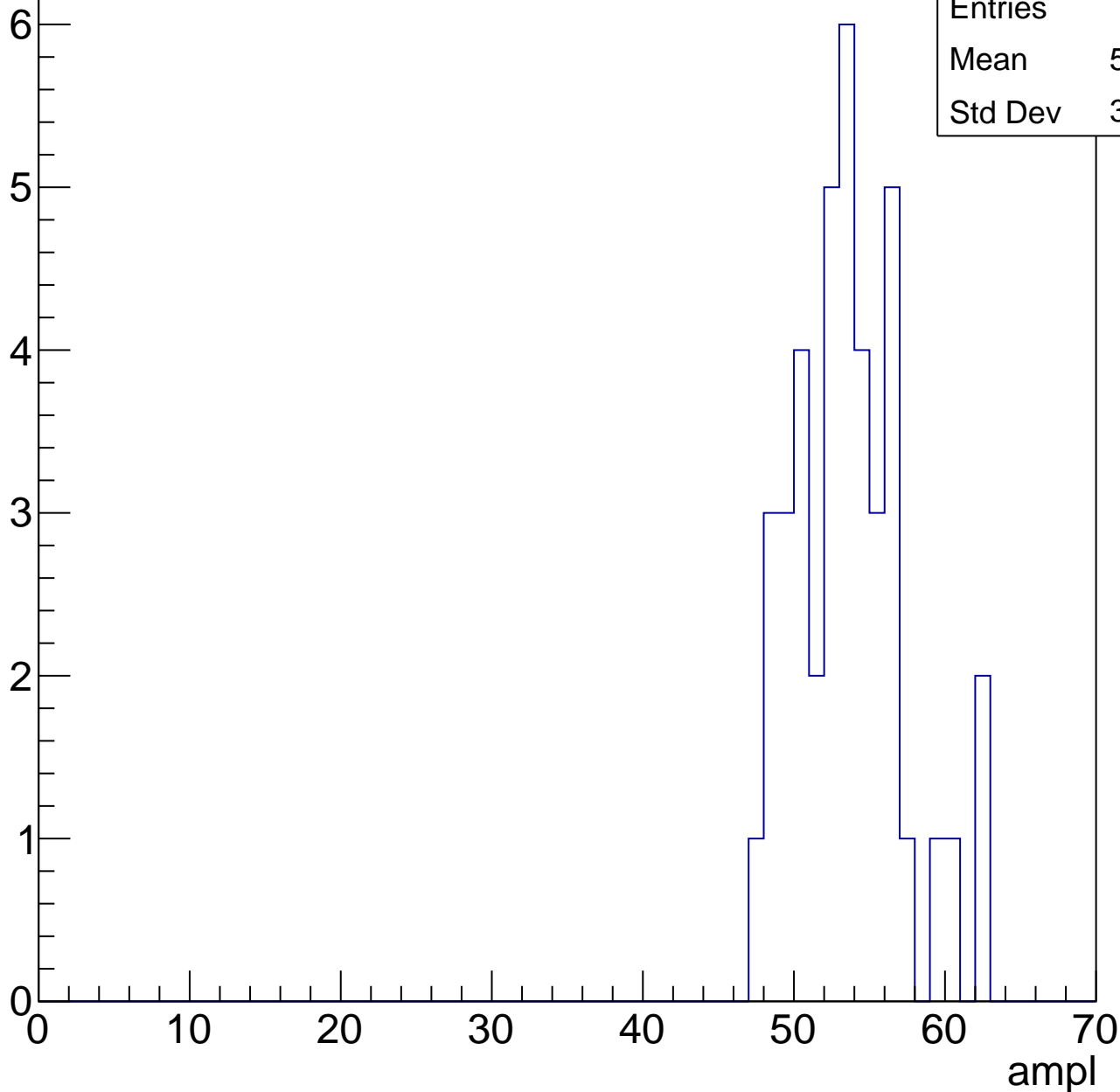


# B1L101S, U3-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

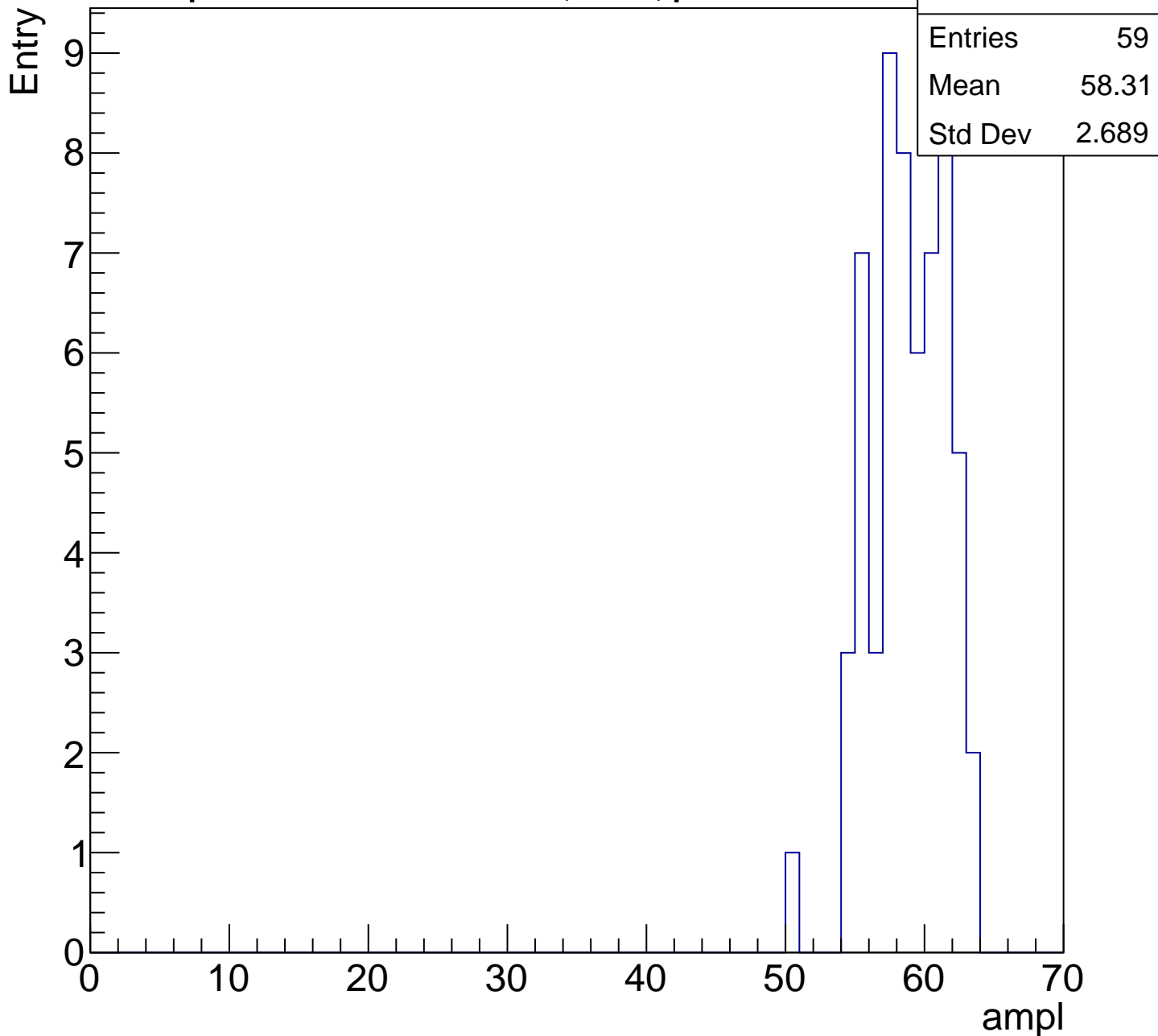
Entry

Entries	41
Mean	53.15
Std Dev	3.599



# B1L101S, U3-ch94, adc5

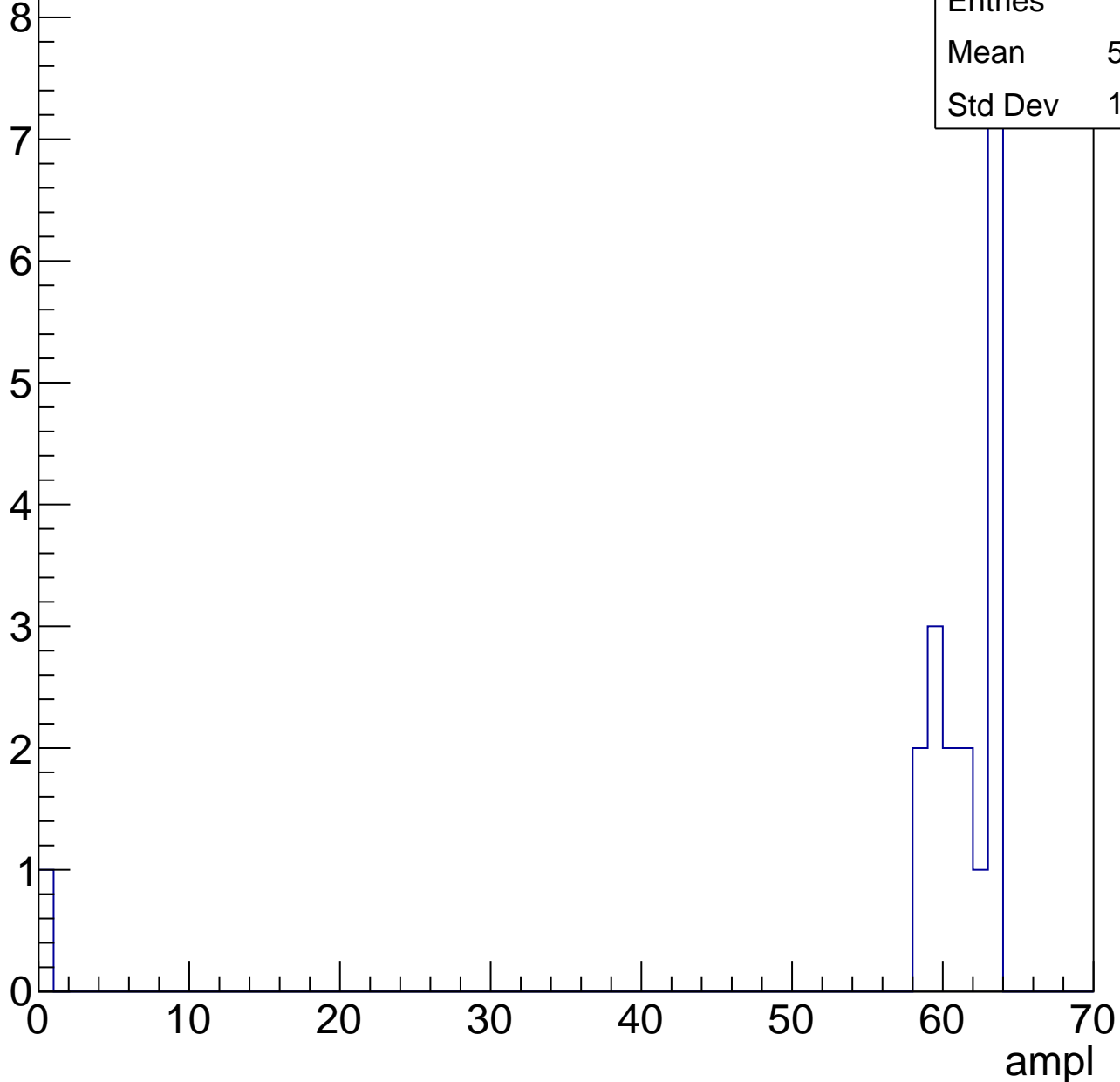
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

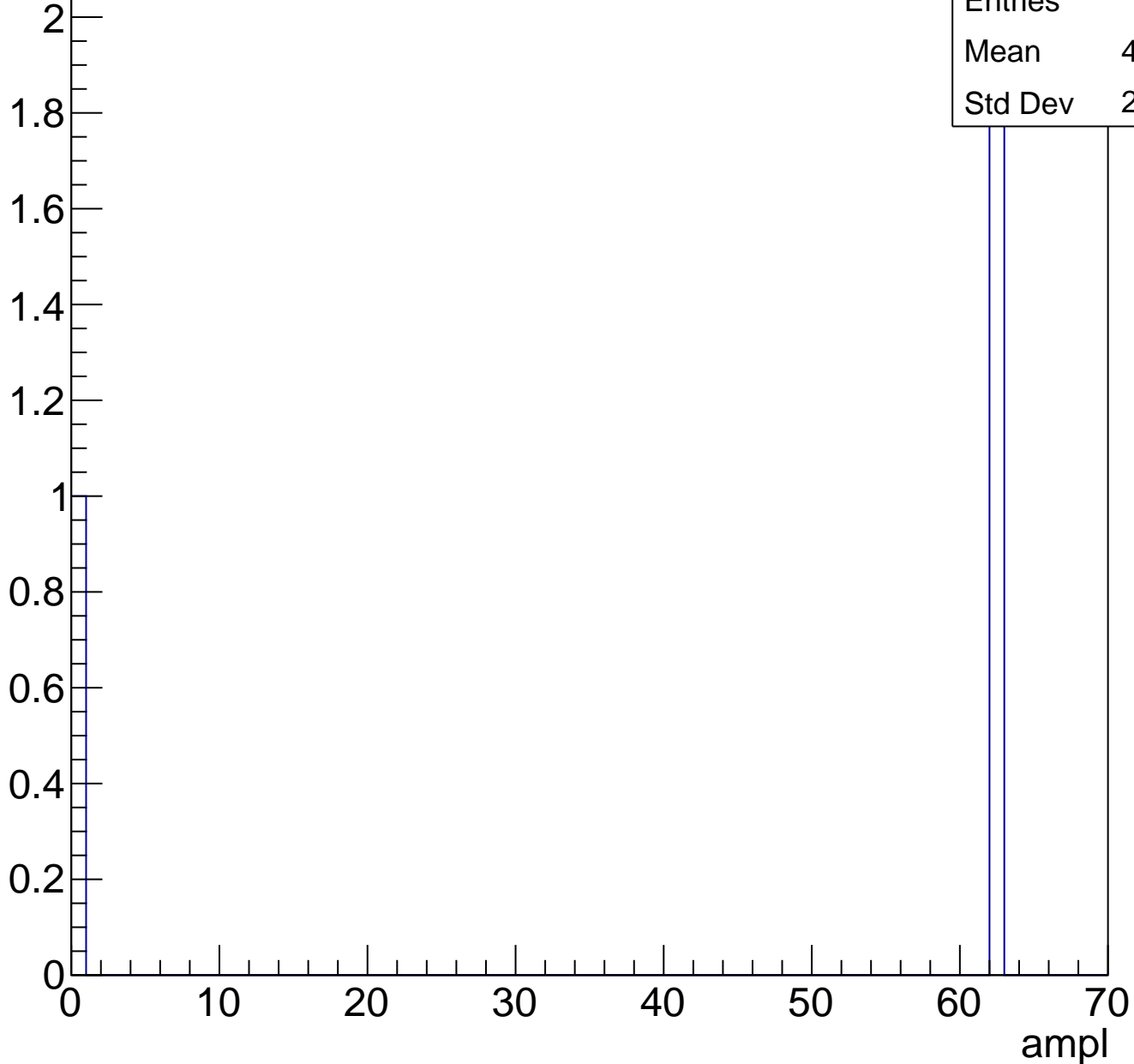




# B1L101S, U3-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch95, adc0

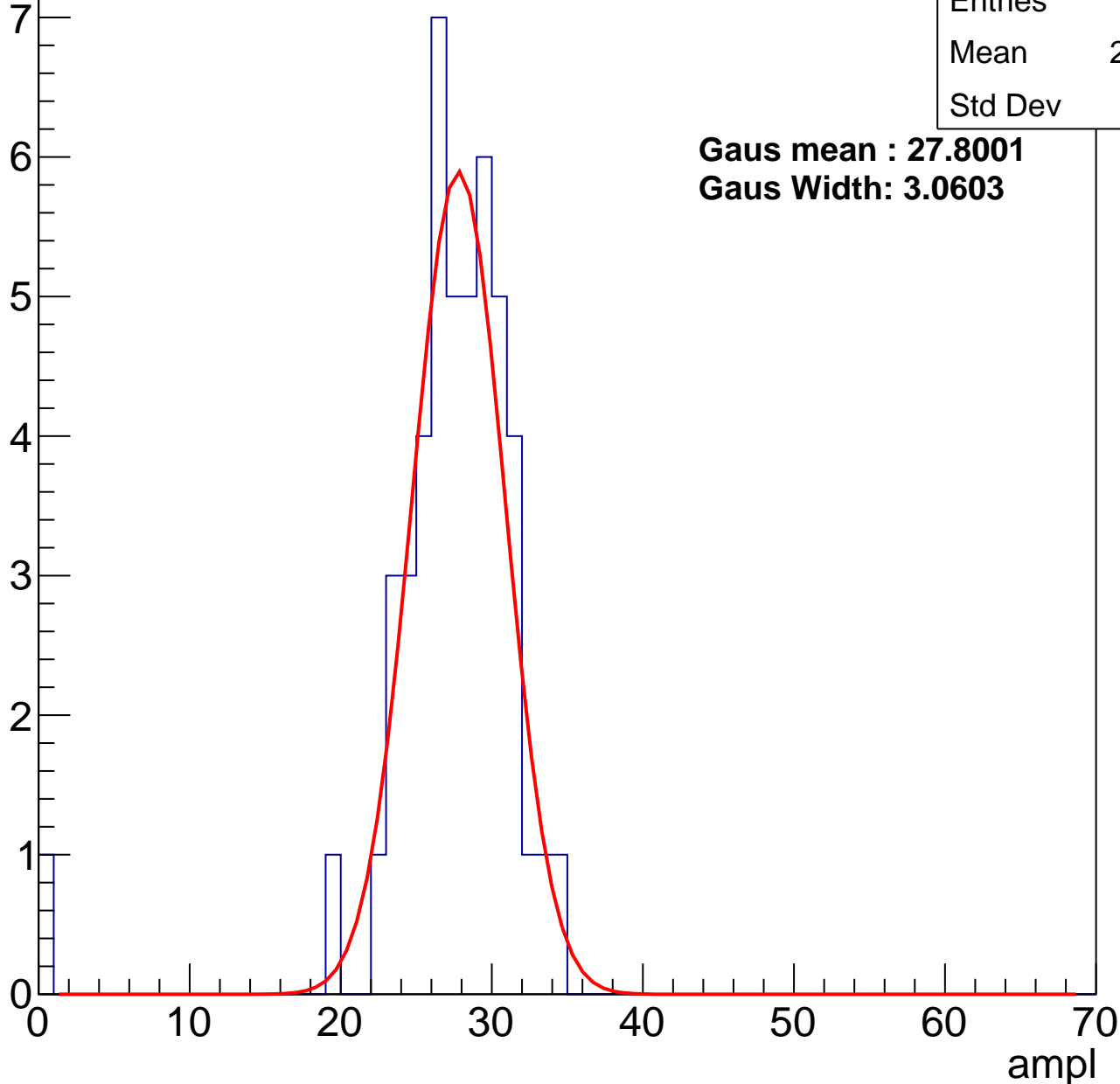
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	26.79
Std Dev	4.92

**Gaus mean : 27.8001**

**Gaus Width: 3.0603**



# B1L101S, U3-ch95, adc1

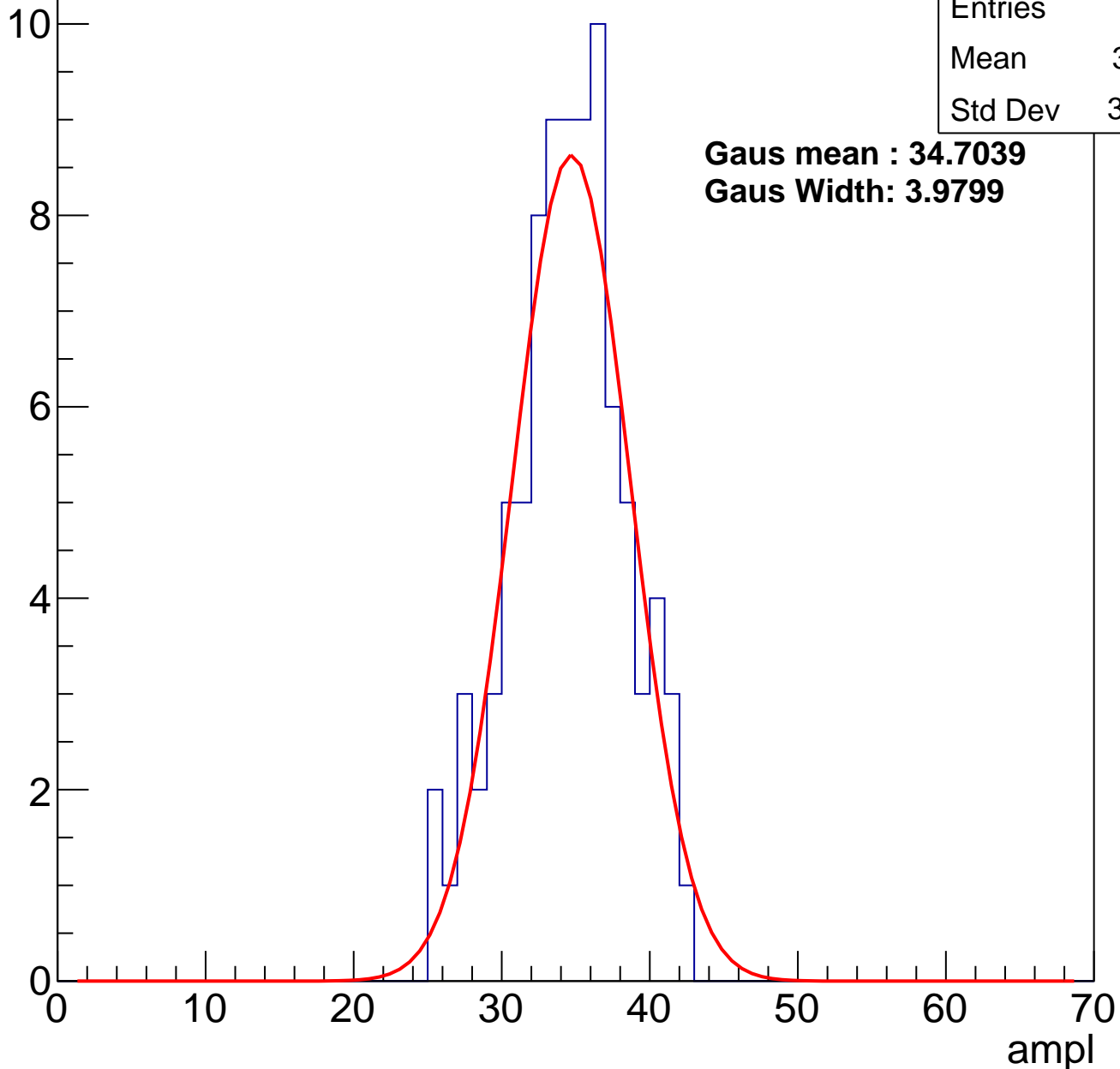
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	88
Mean	34.01
Std Dev	3.842

**Gaus mean : 34.7039**

**Gaus Width: 3.9799**

Entry



# B1L101S, U3-ch95, adc2

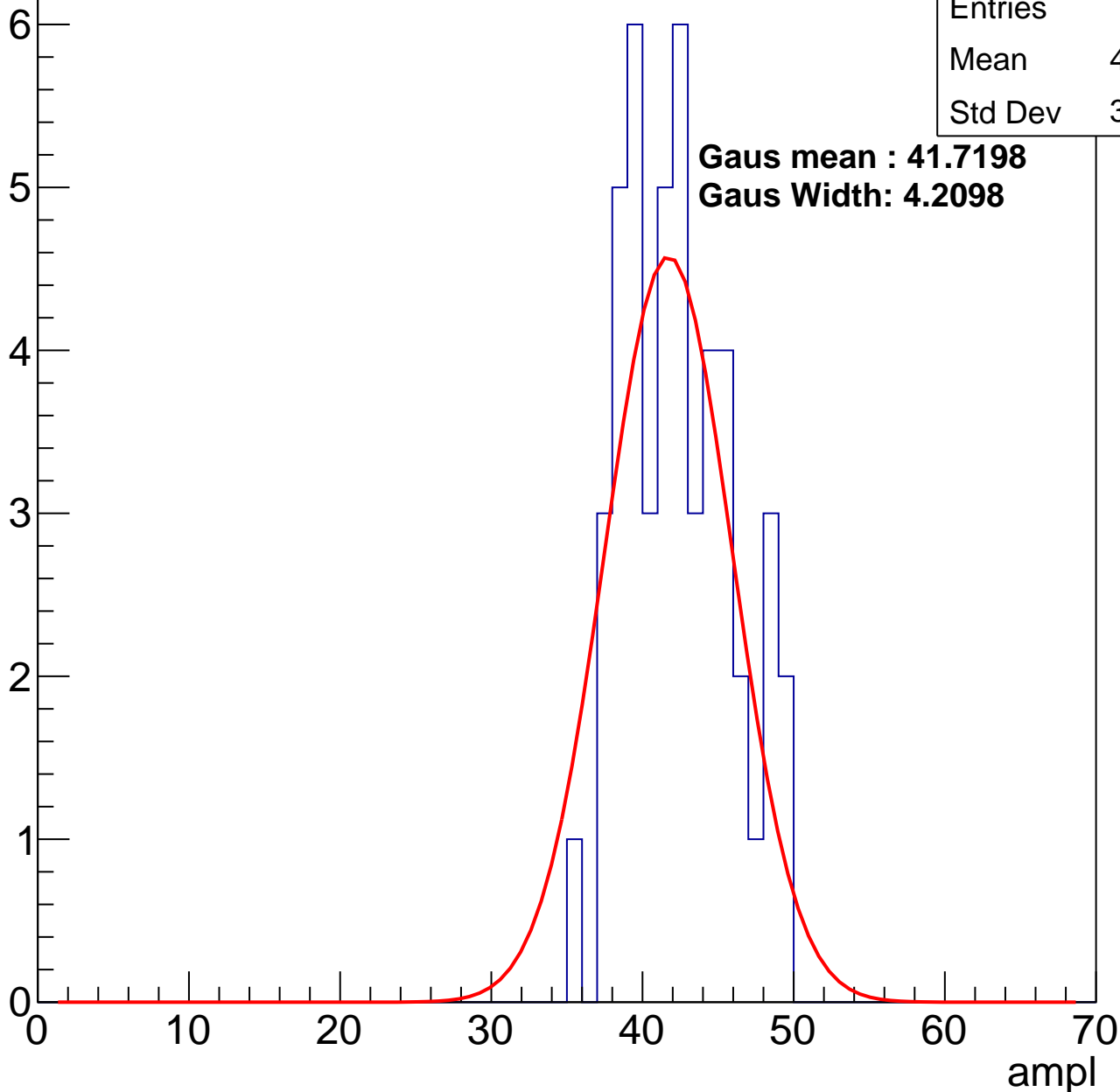
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	41.94
Std Dev	3.514

**Gaus mean : 41.7198**

**Gaus Width: 4.2098**

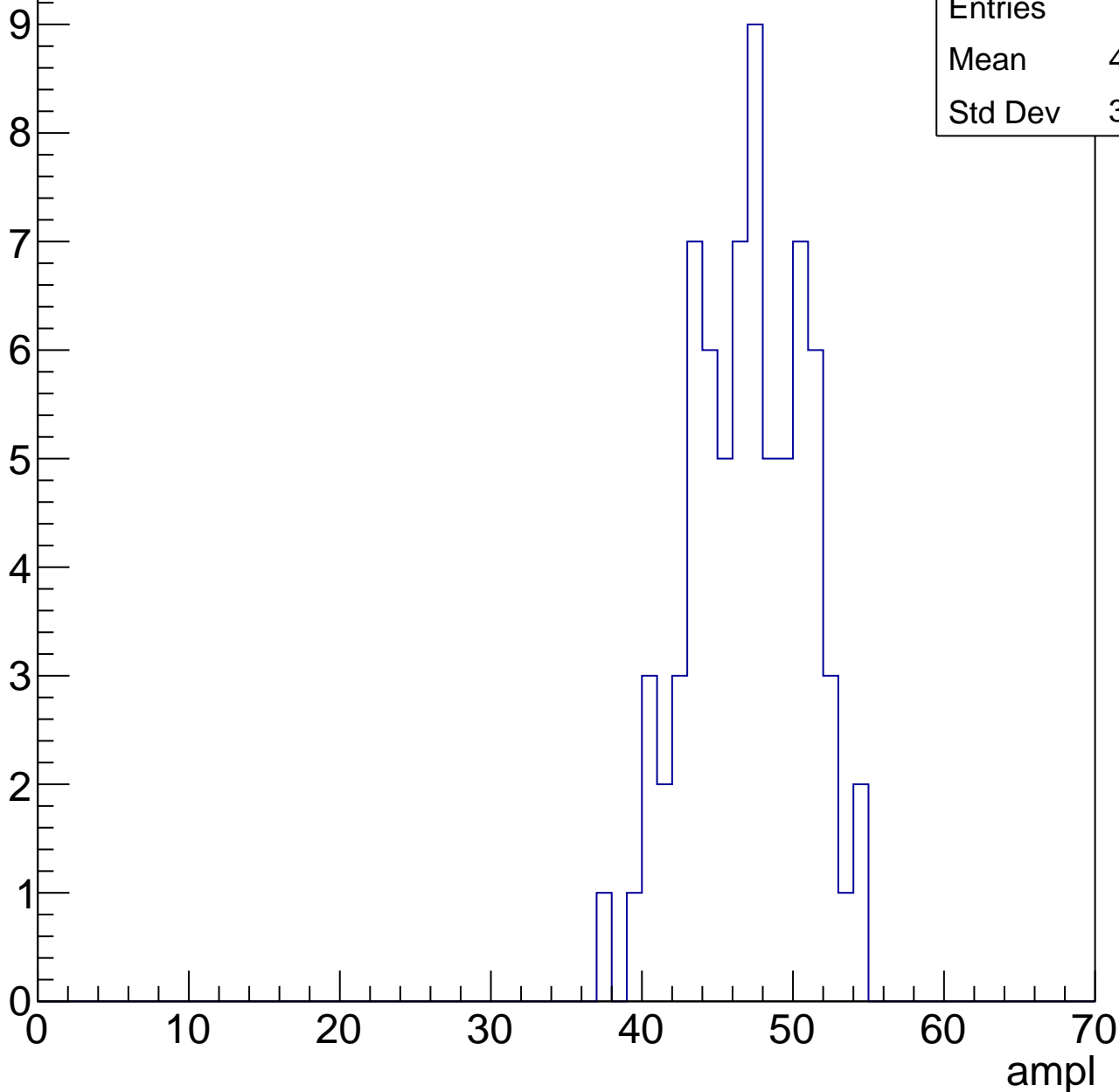


# B1L101S, U3-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

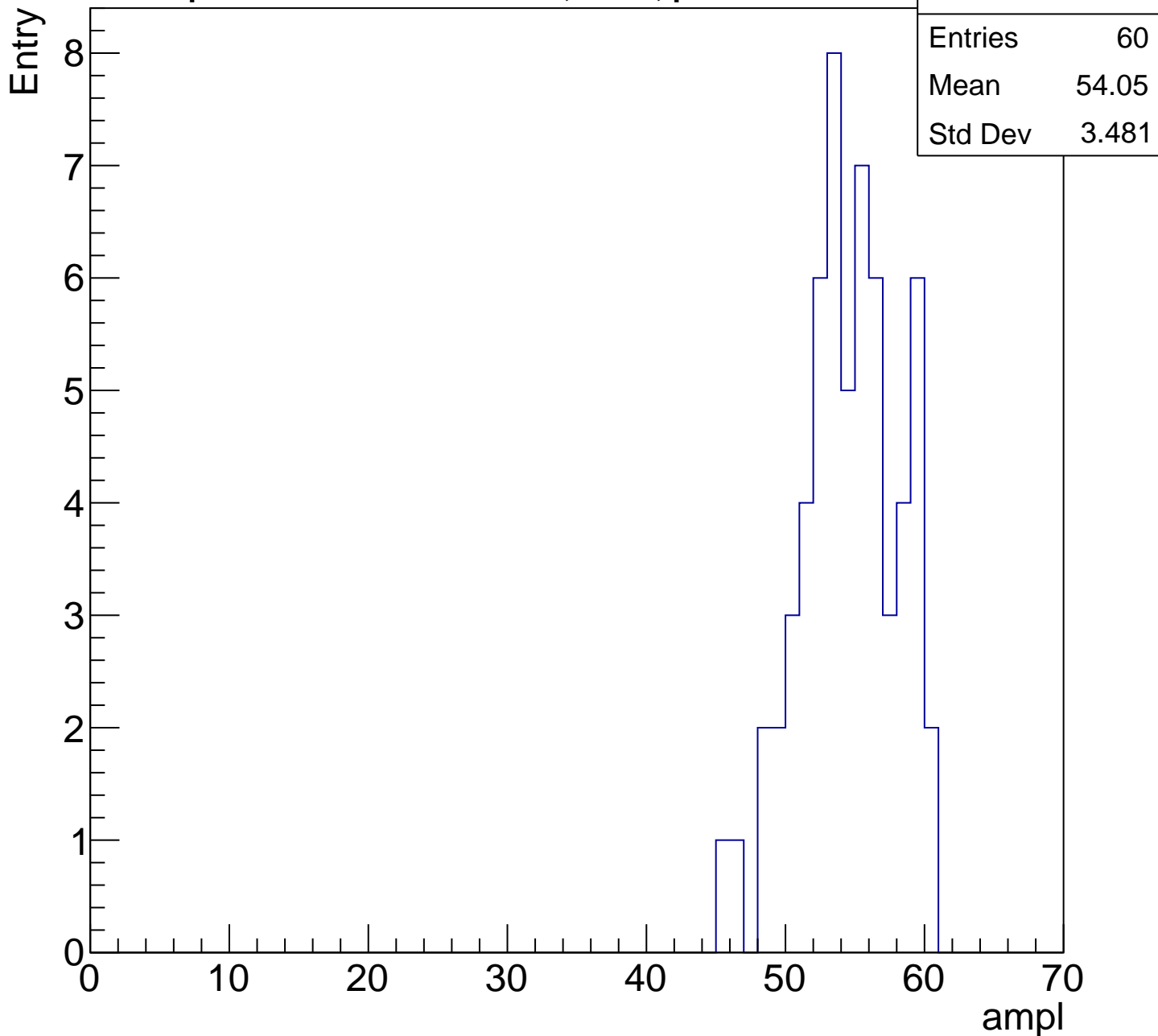
Entry

Entries	73
Mean	46.53
Std Dev	3.753



# B1L101S, U3-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

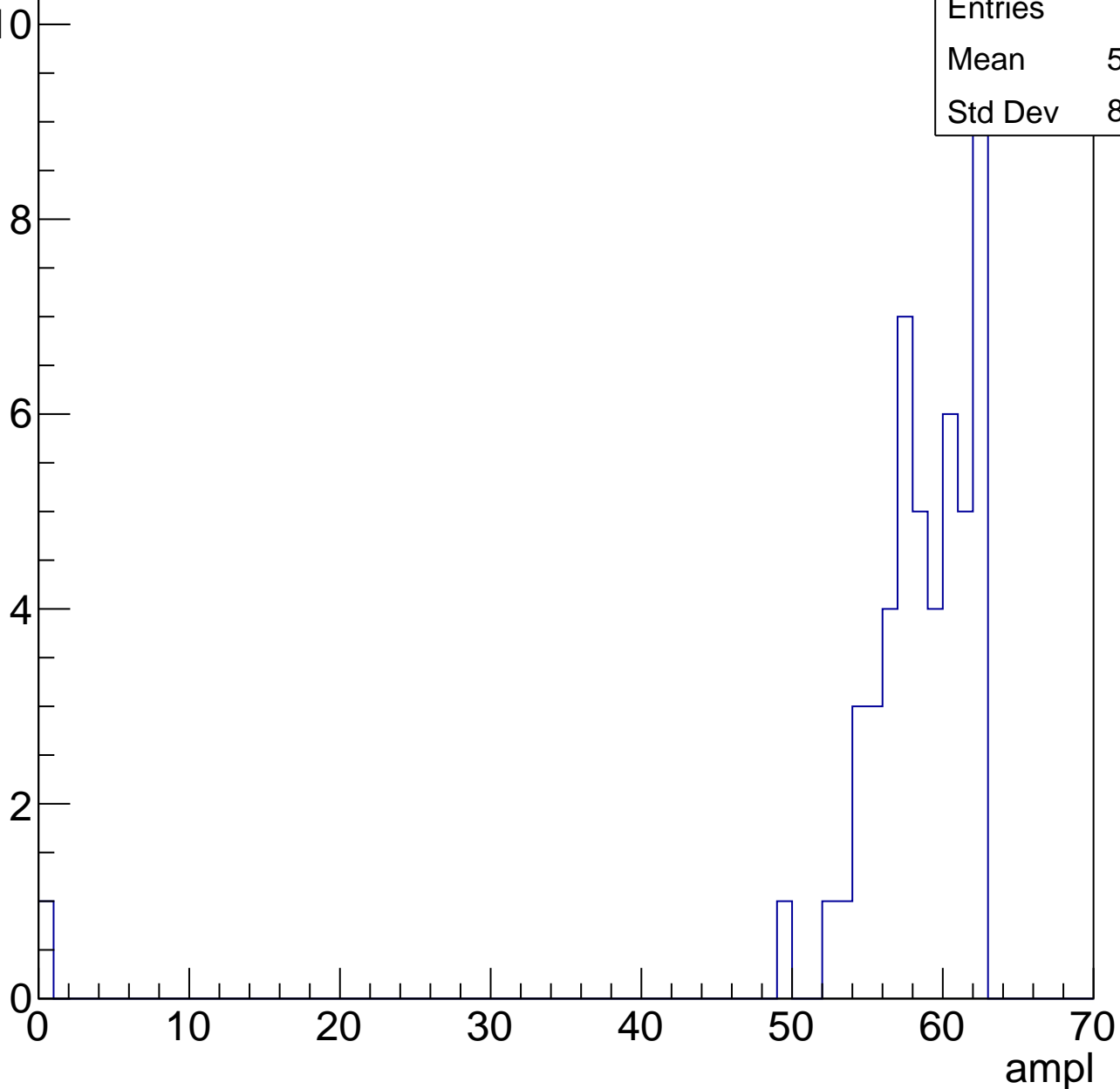


# B1L101S, U3-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	57.16
Std Dev	8.633



# B1L101S, U3-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	17
Mean	61.88
Std Dev	1.49

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

0

2

4

6

8

10



# B1L101S, U3-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch96, adc0

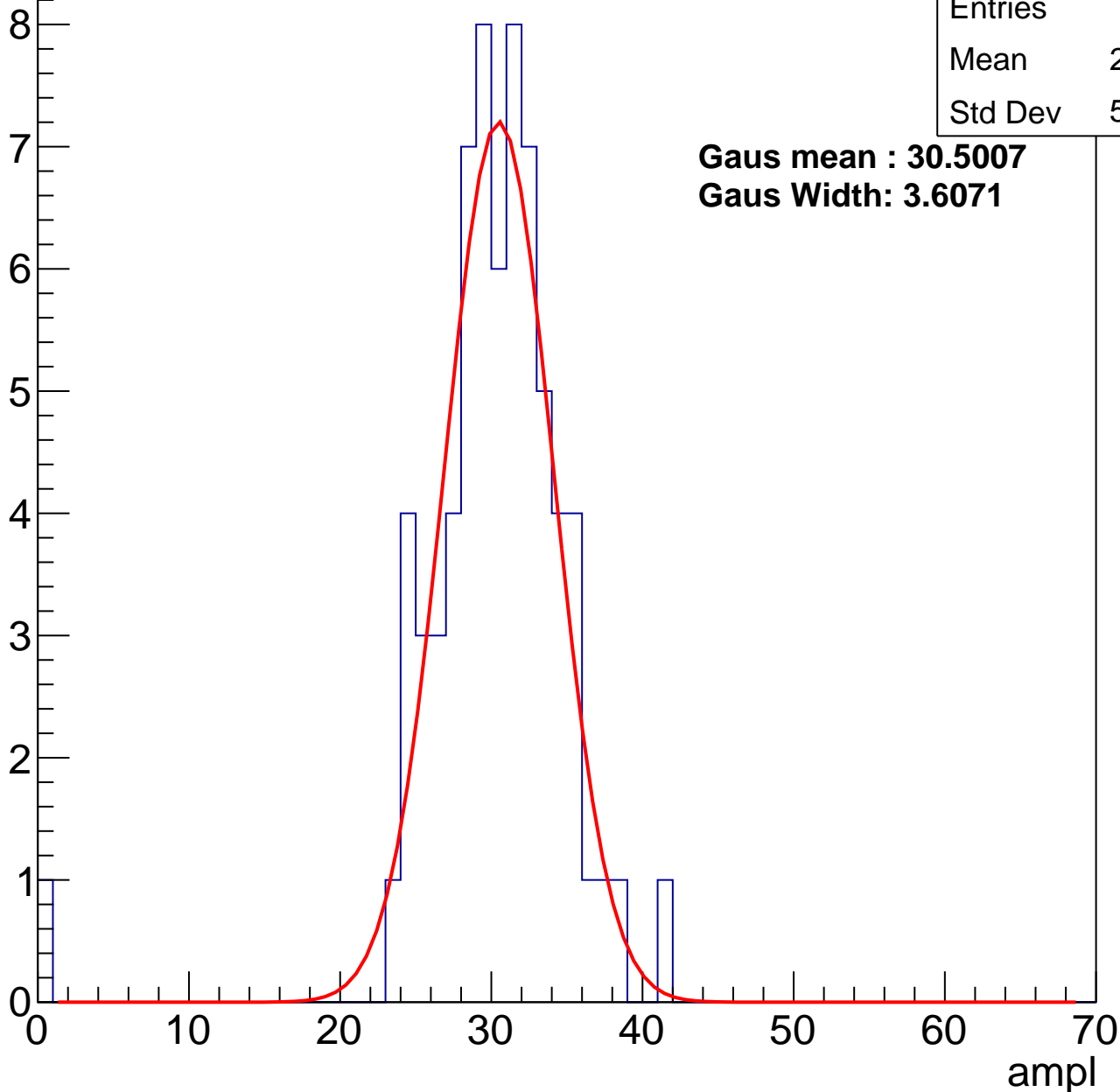
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	29.75
Std Dev	5.106

**Gaus mean : 30.5007**

**Gaus Width: 3.6071**



# B1L101S, U3-ch96, adc1

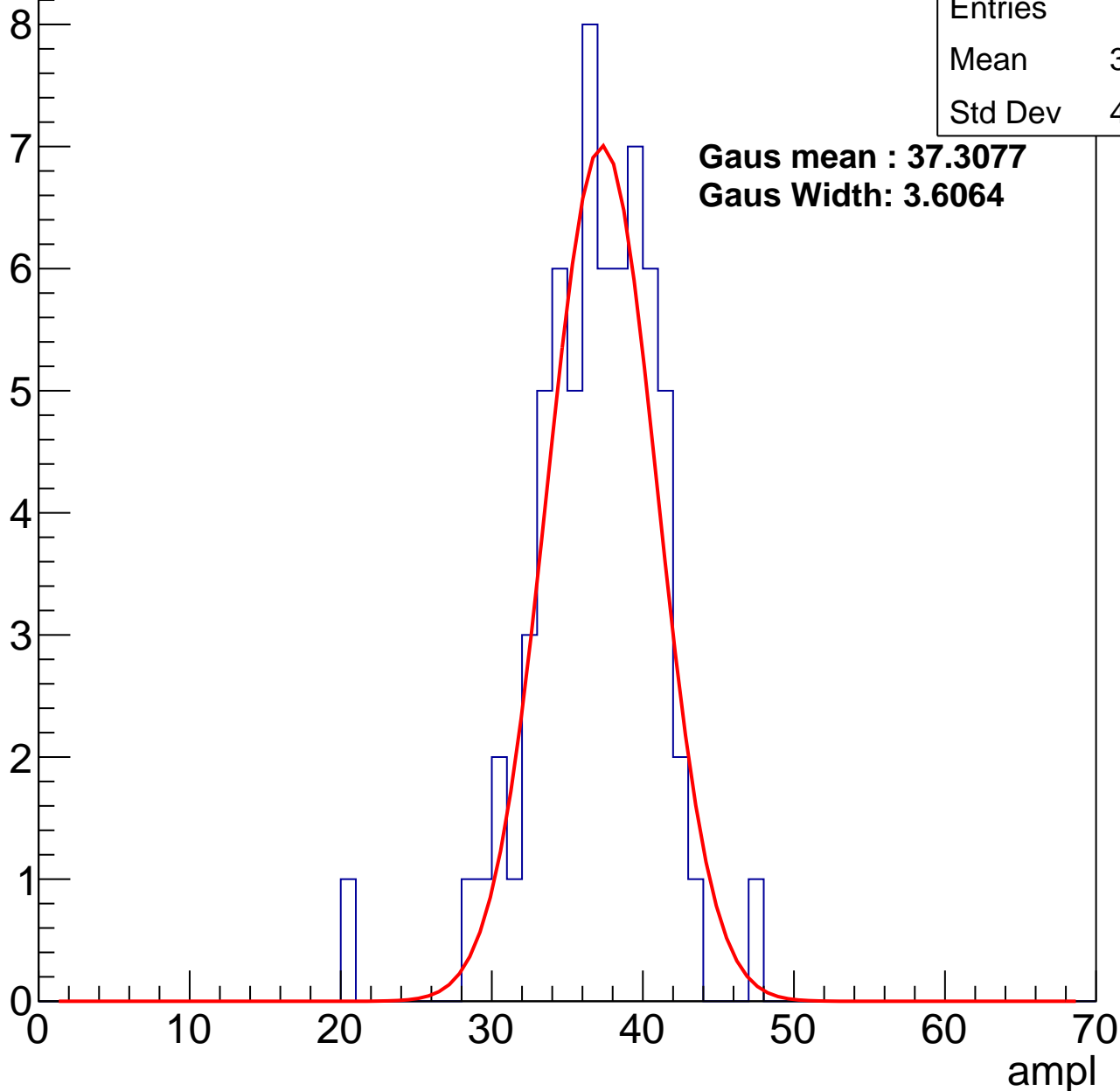
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	36.39
Std Dev	4.114

**Gaus mean : 37.3077**

**Gaus Width: 3.6064**



# B1L101S, U3-ch96, adc2

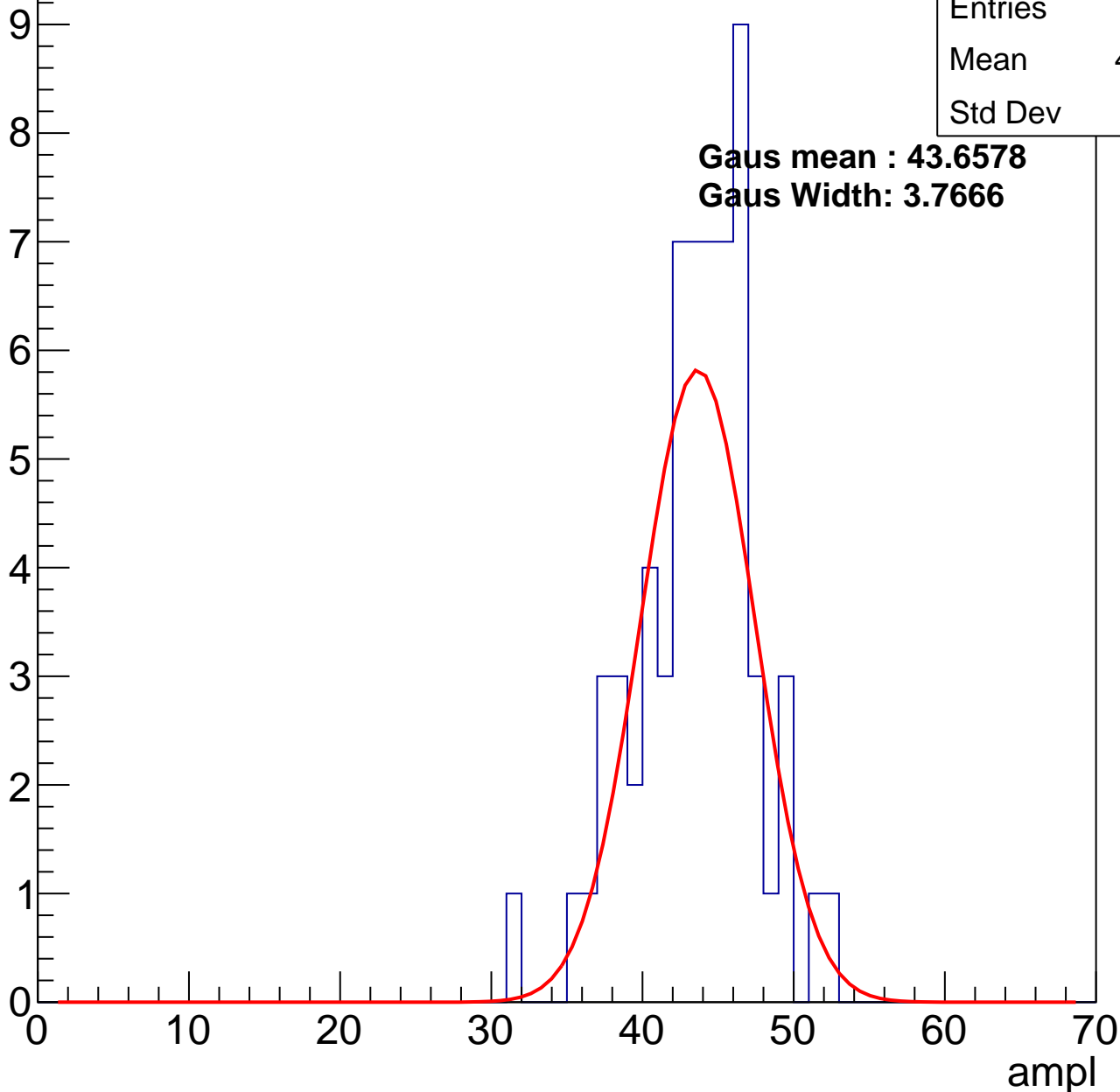
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	43.11
Std Dev	3.89

**Gaus mean : 43.6578**

**Gaus Width: 3.7666**

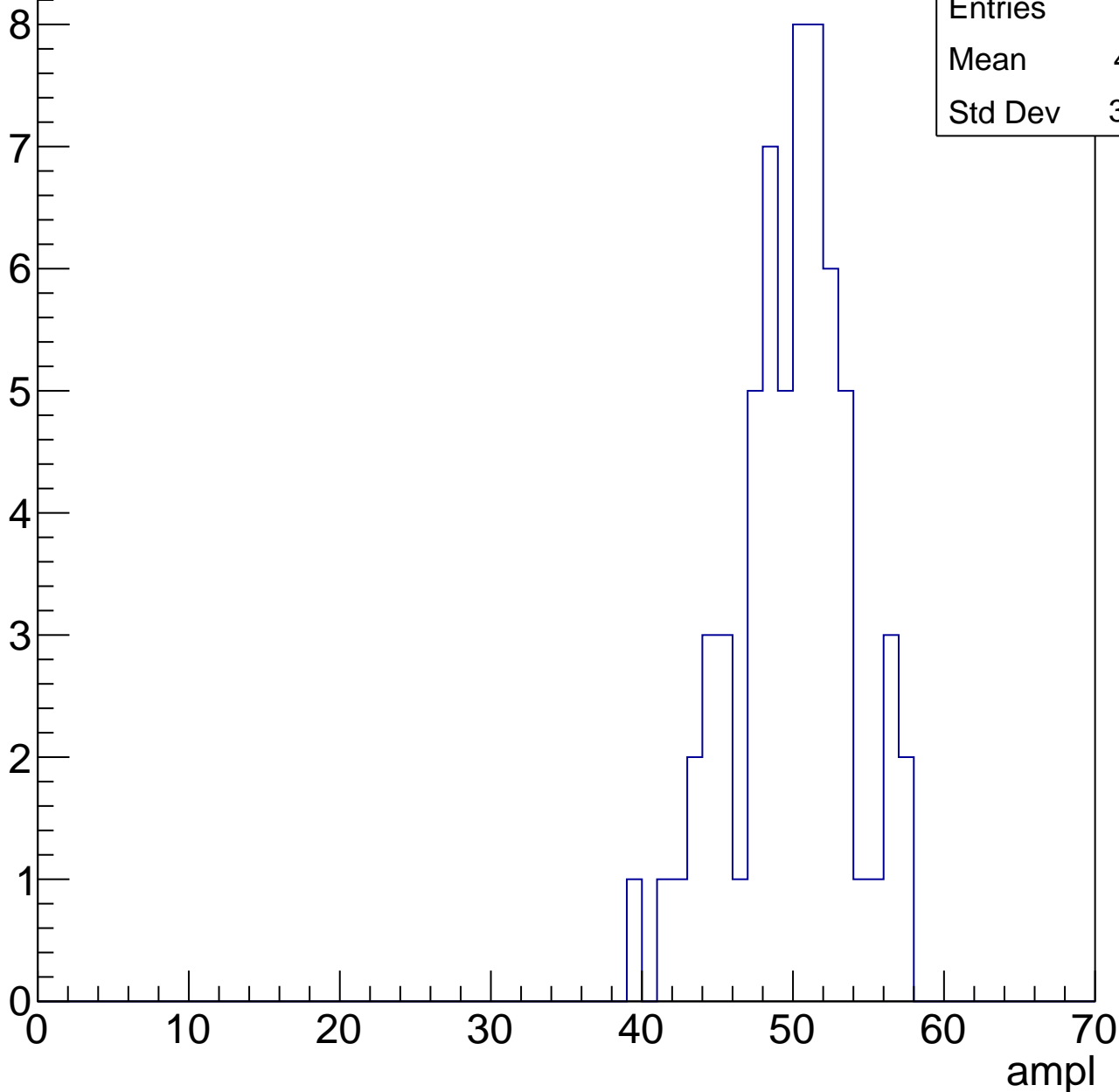


# B1L101S, U3-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	49.41
Std Dev	3.869

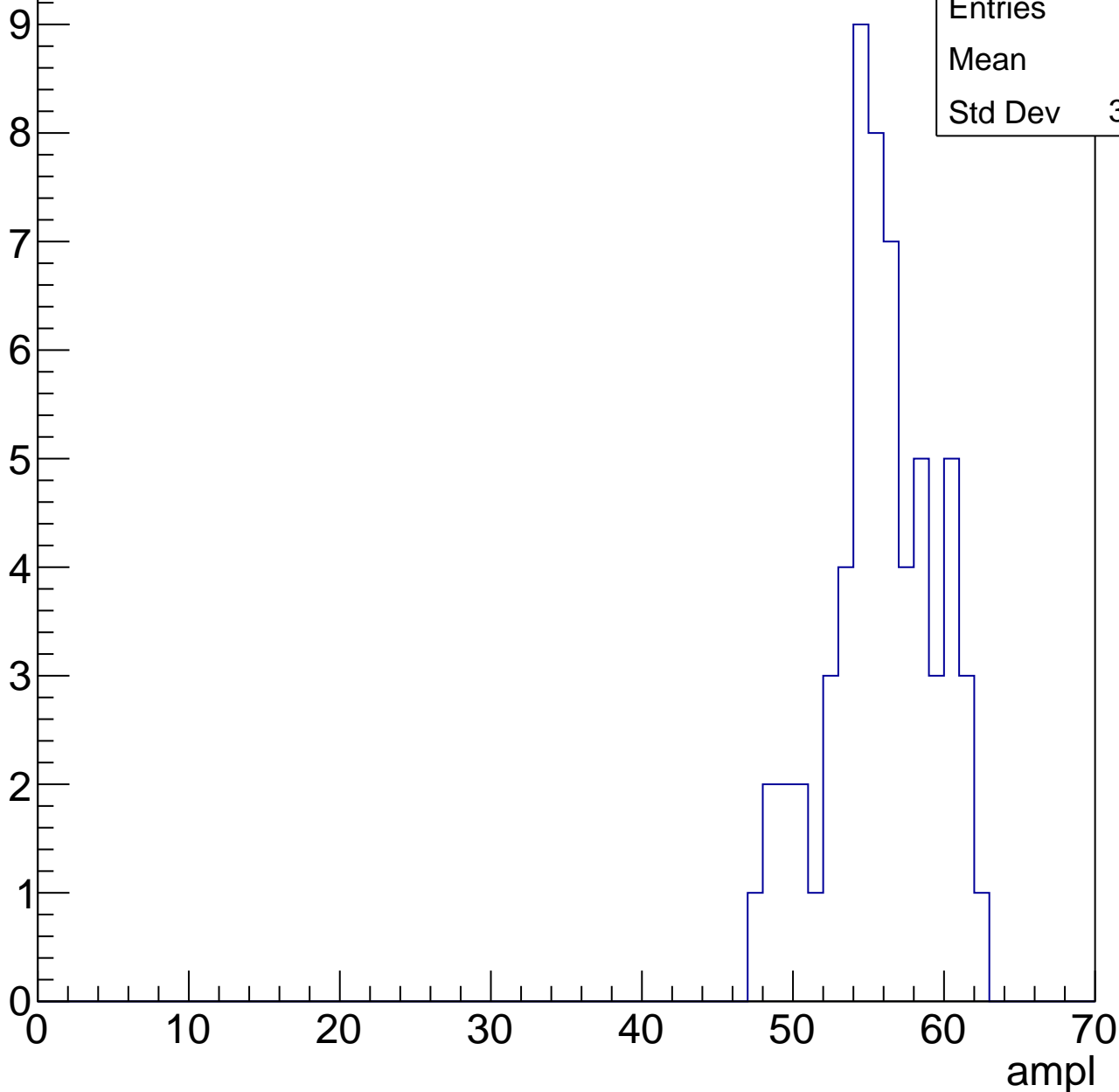


# B1L101S, U3-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	55.3
Std Dev	3.523

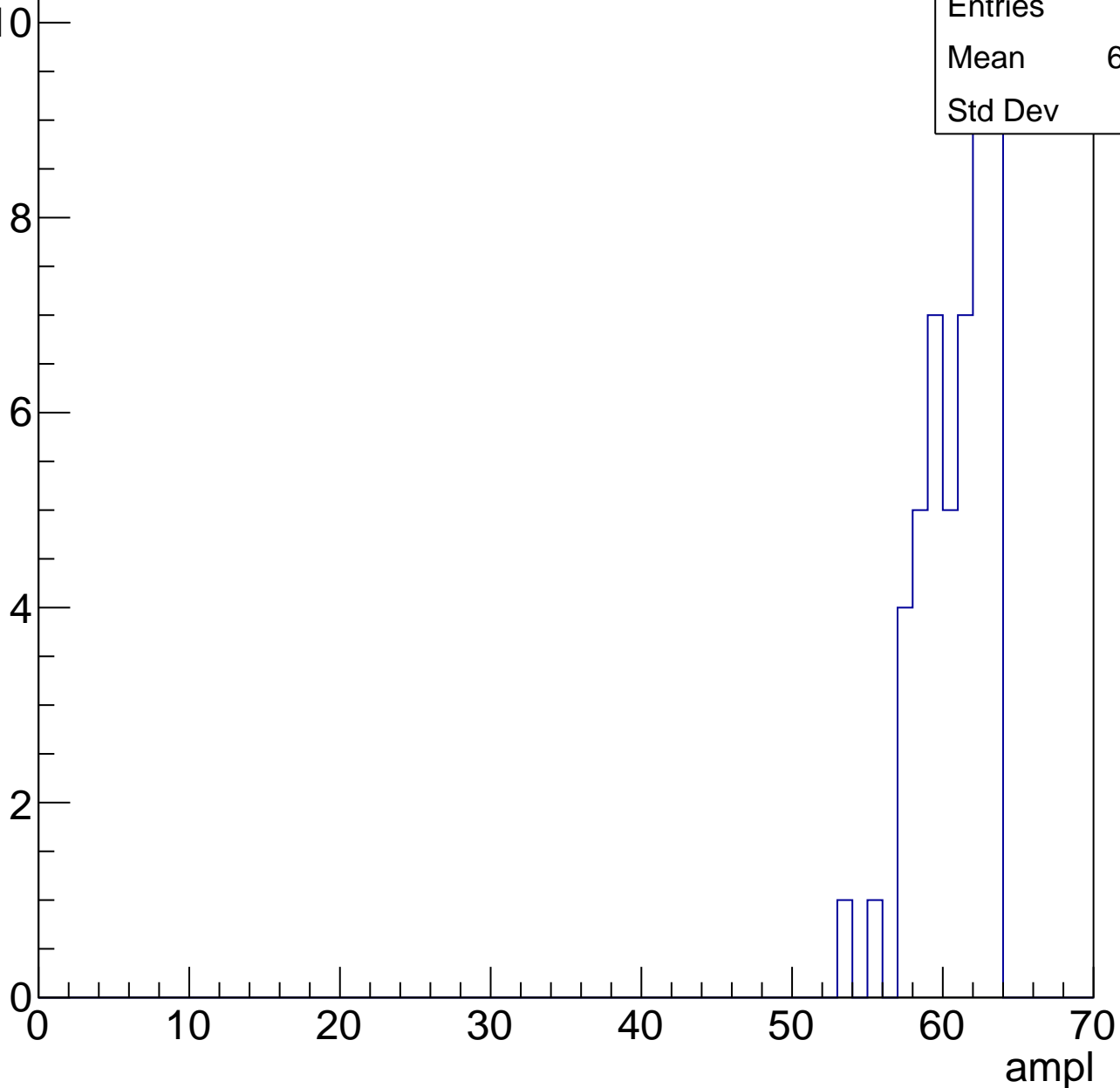


# B1L101S, U3-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	49
Mean	60.29
Std Dev	2.33



# B1L101S, U3-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0



# B1L101S, U3-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch97, adc0

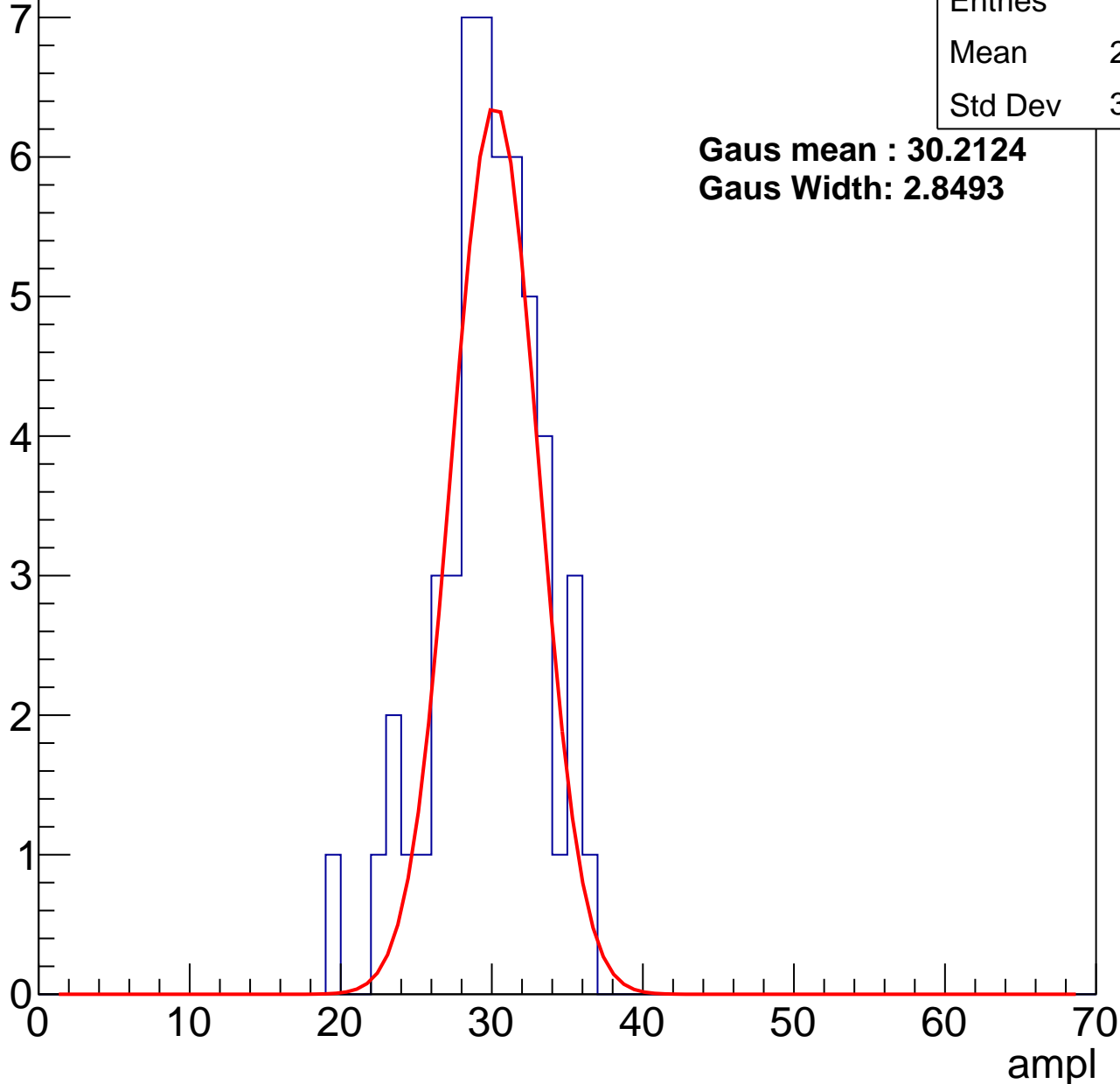
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	29.37
Std Dev	3.459

**Gaus mean : 30.2124**

**Gaus Width: 2.8493**



# B1L101S, U3-ch97, adc1

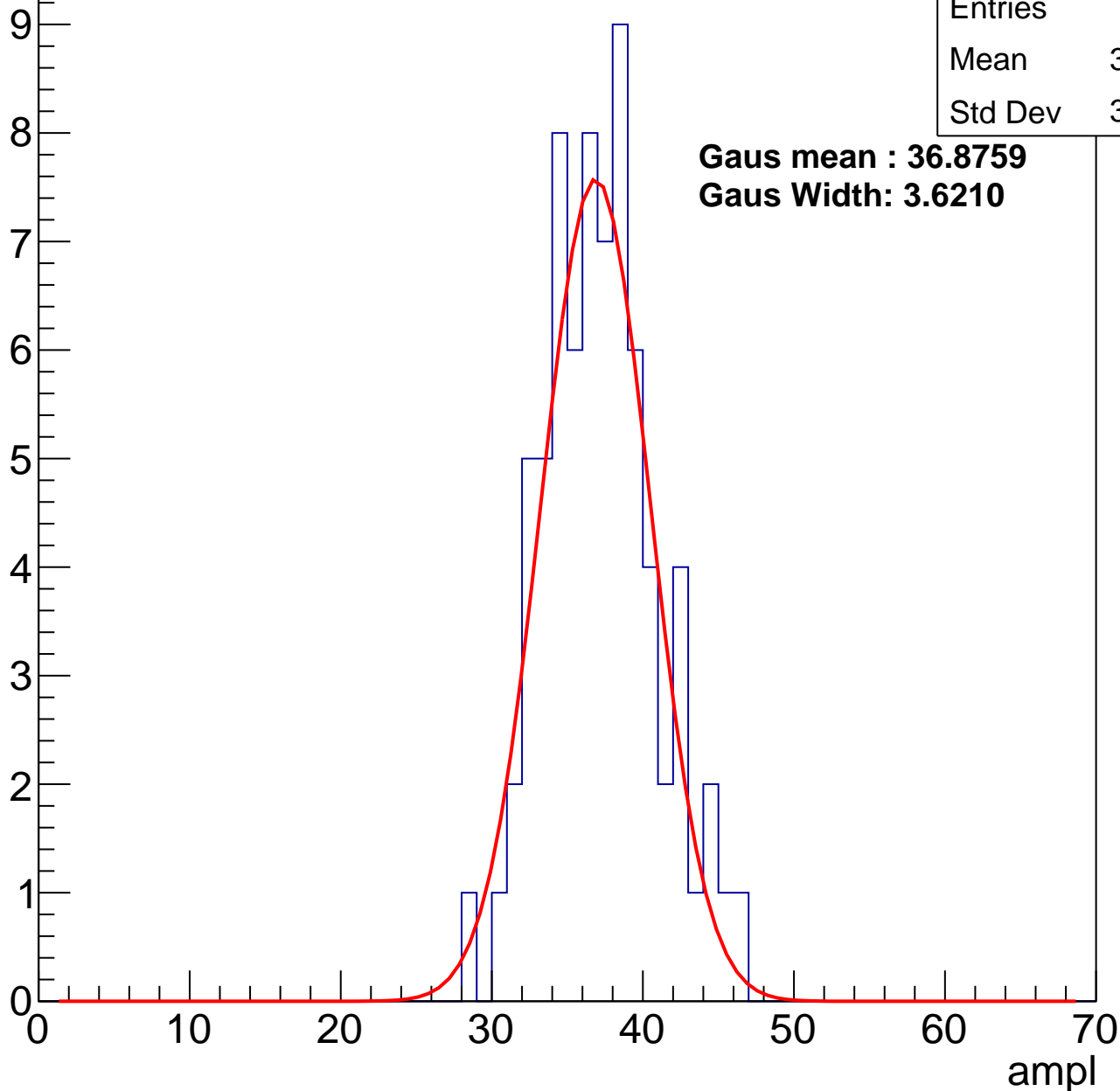
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	73
Mean	36.74
Std Dev	3.675

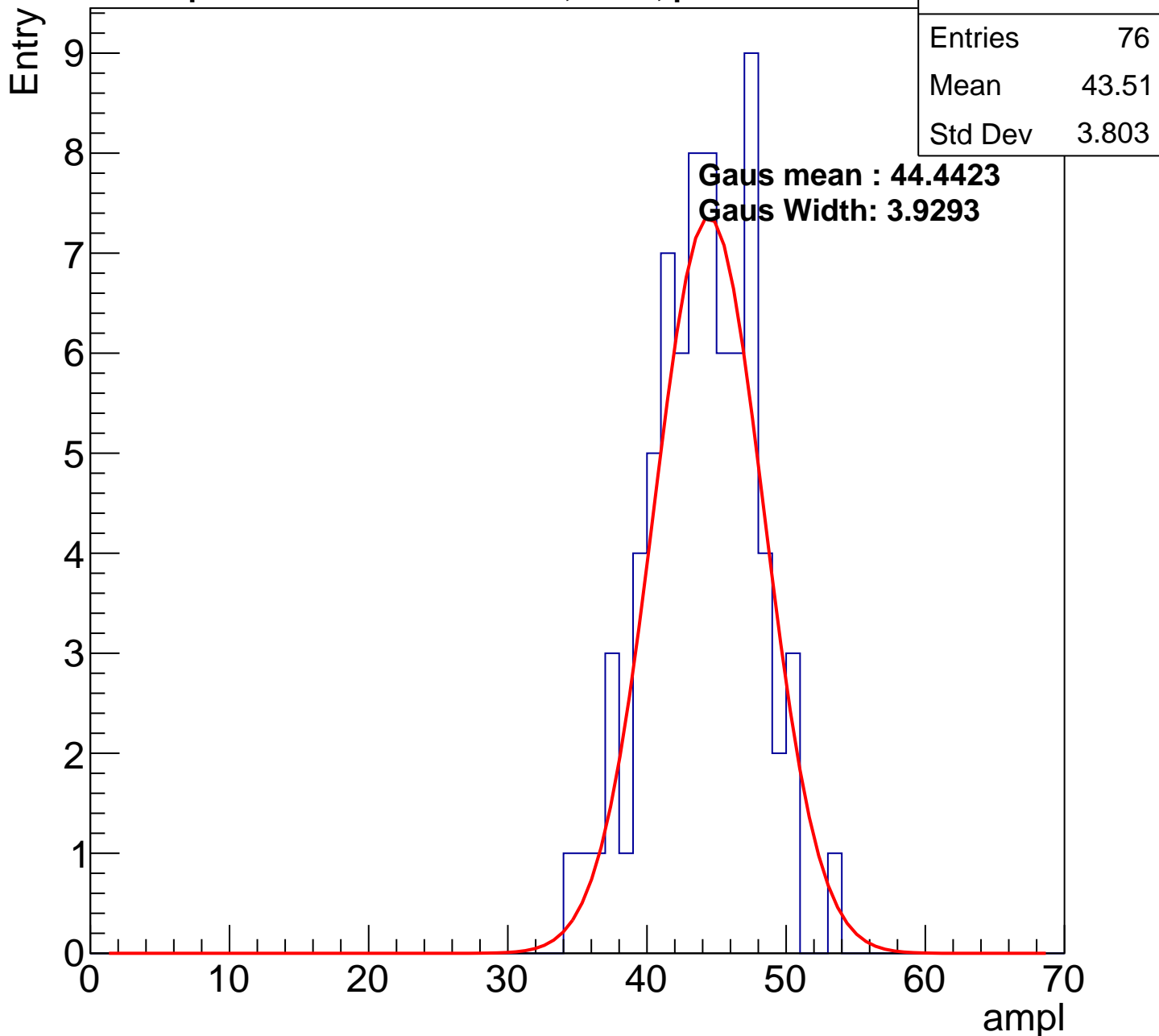
**Gaus mean : 36.8759**

**Gaus Width: 3.6210**



# B1L101S, U3-ch97, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

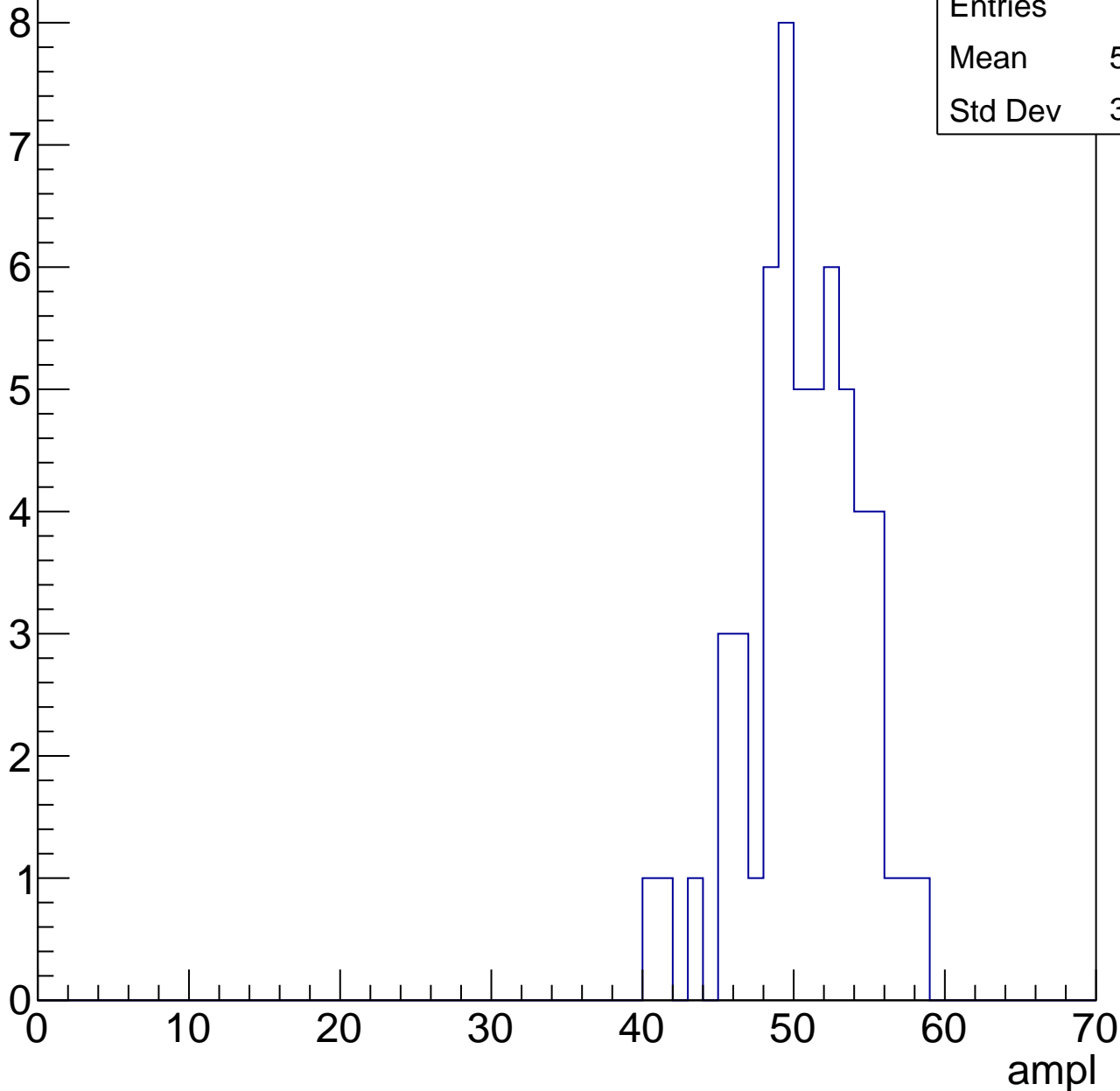


# B1L101S, U3-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	50.23
Std Dev	3.727

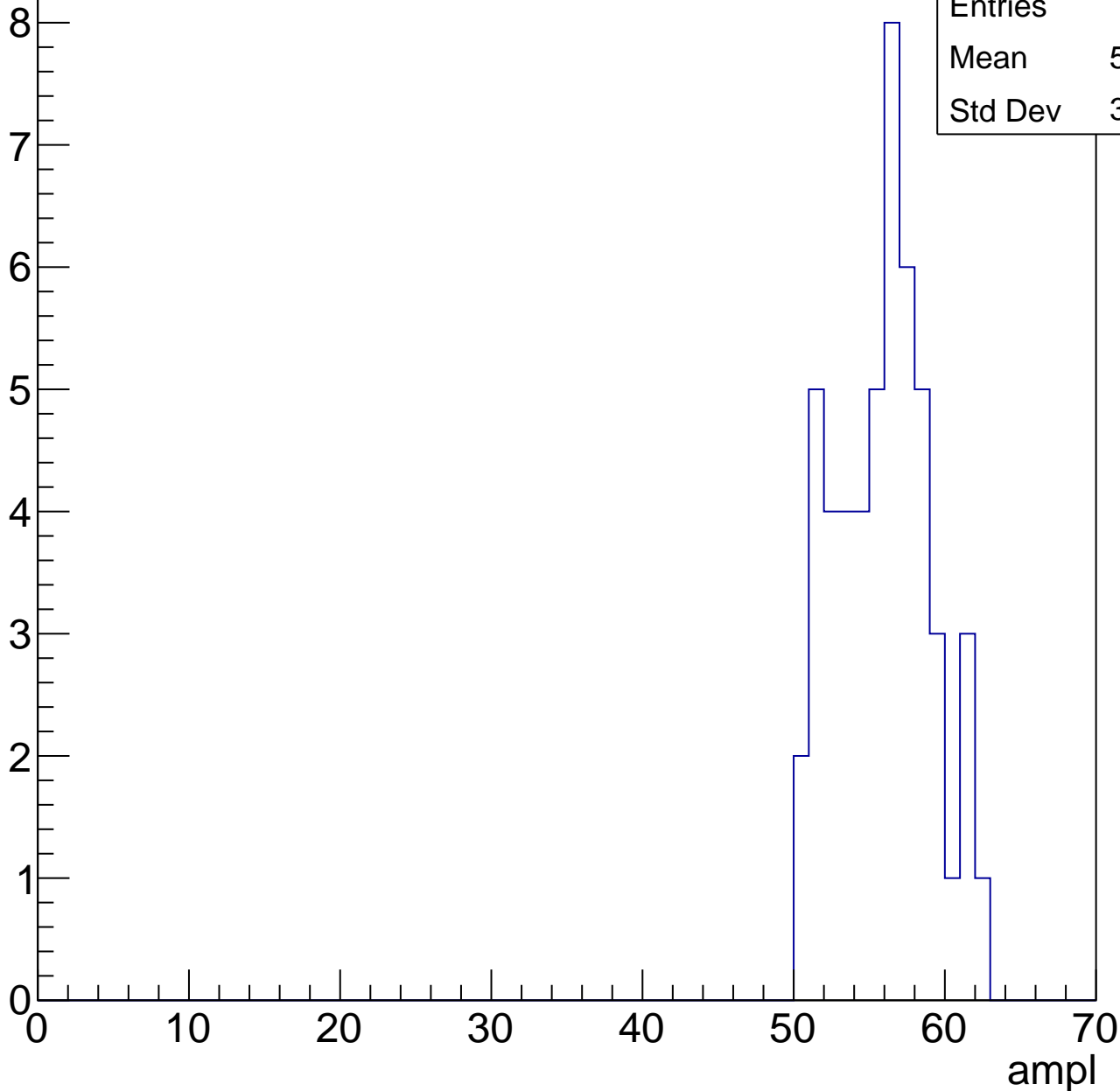


# B1L101S, U3-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	55.45
Std Dev	3.076



# B1L101S, U3-ch97, adc5

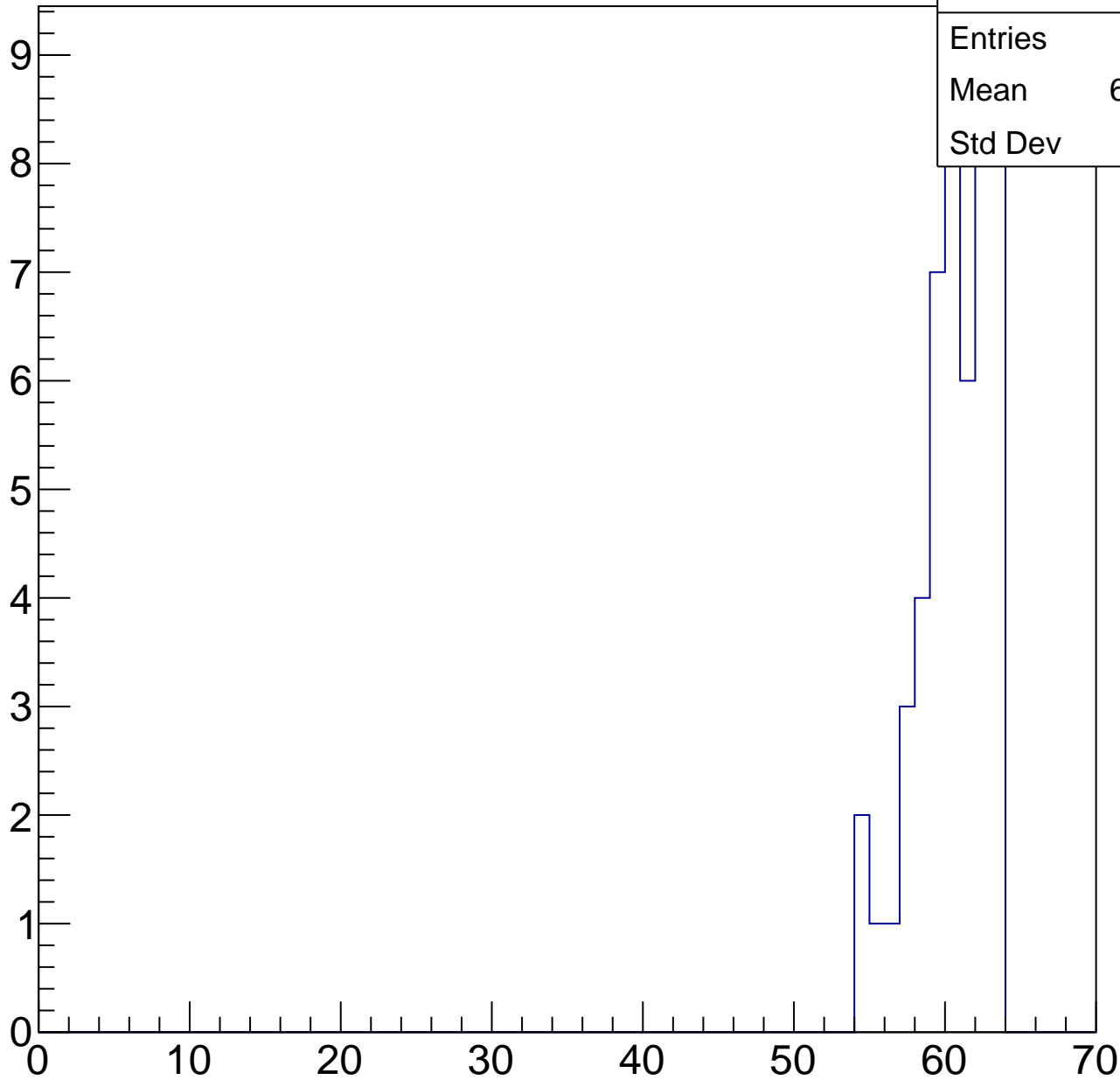
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	60.02
Std Dev	2.36

ampl



# B1L101S, U3-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U3-ch98, adc0

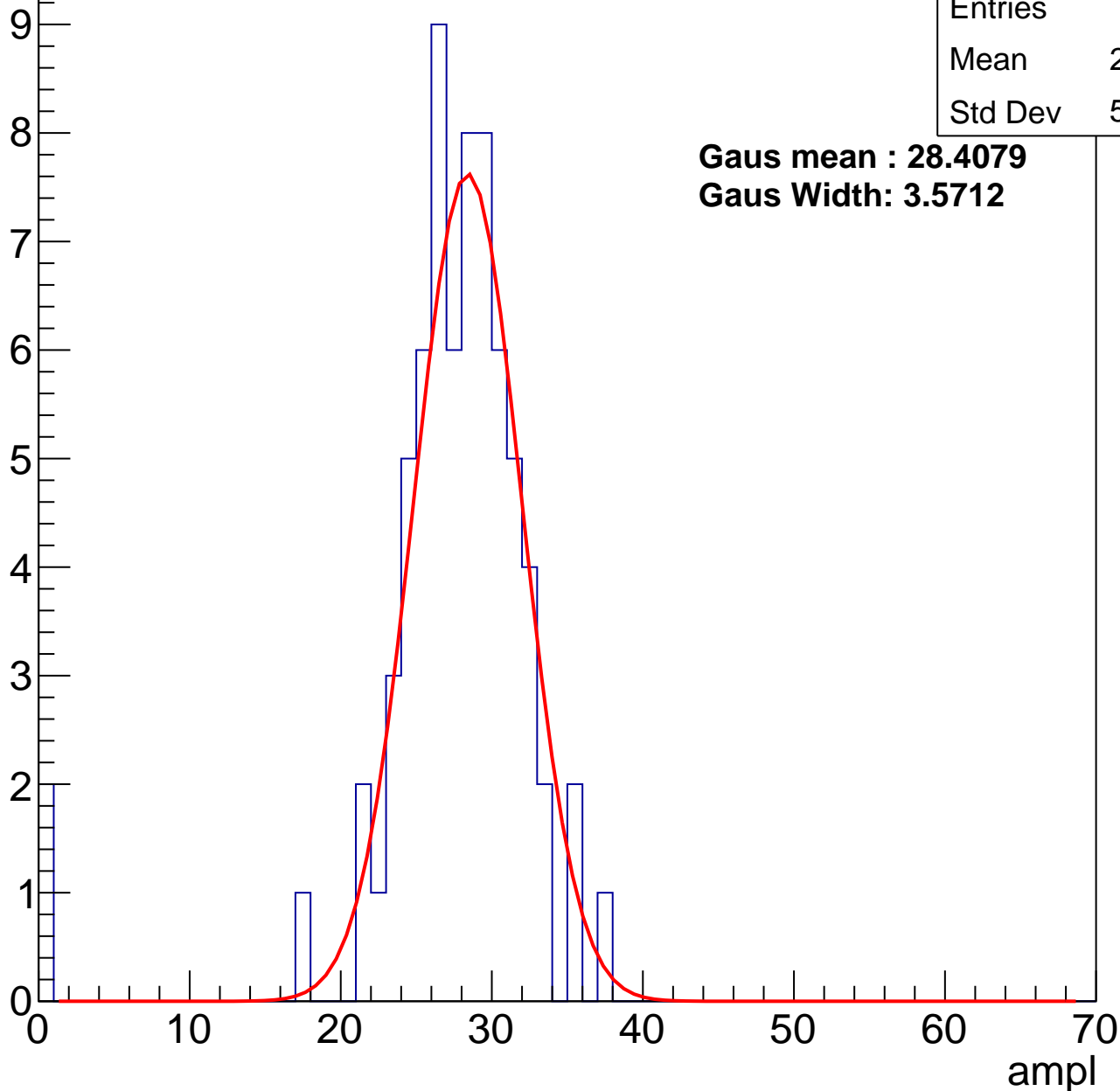
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	71
Mean	26.87
Std Dev	5.758

**Gaus mean : 28.4079**

**Gaus Width: 3.5712**



# B1L101S, U3-ch98, adc1

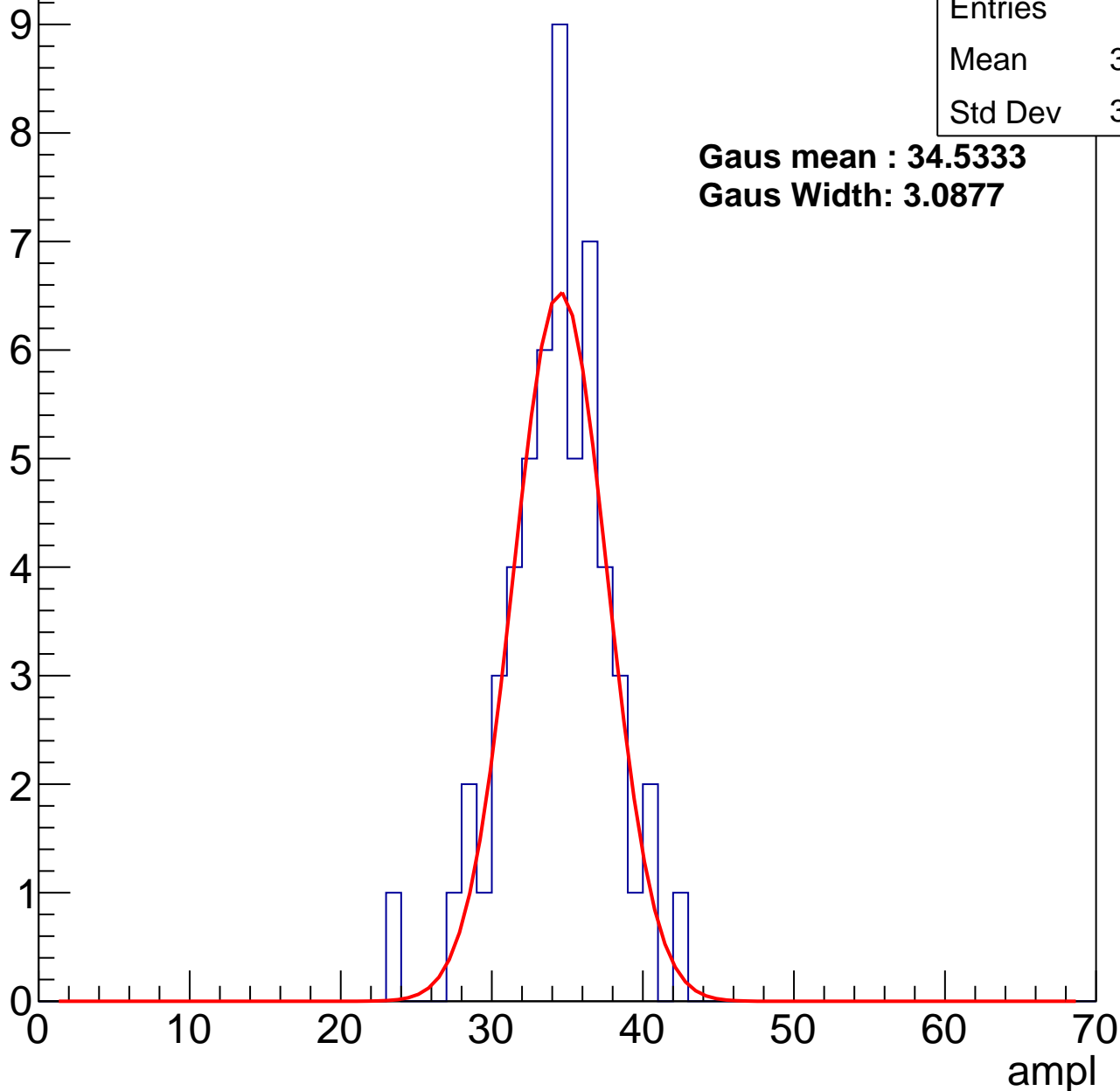
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	33.87
Std Dev	3.449

**Gaus mean : 34.5333**

**Gaus Width: 3.0877**



# B1L101S, U3-ch98, adc2

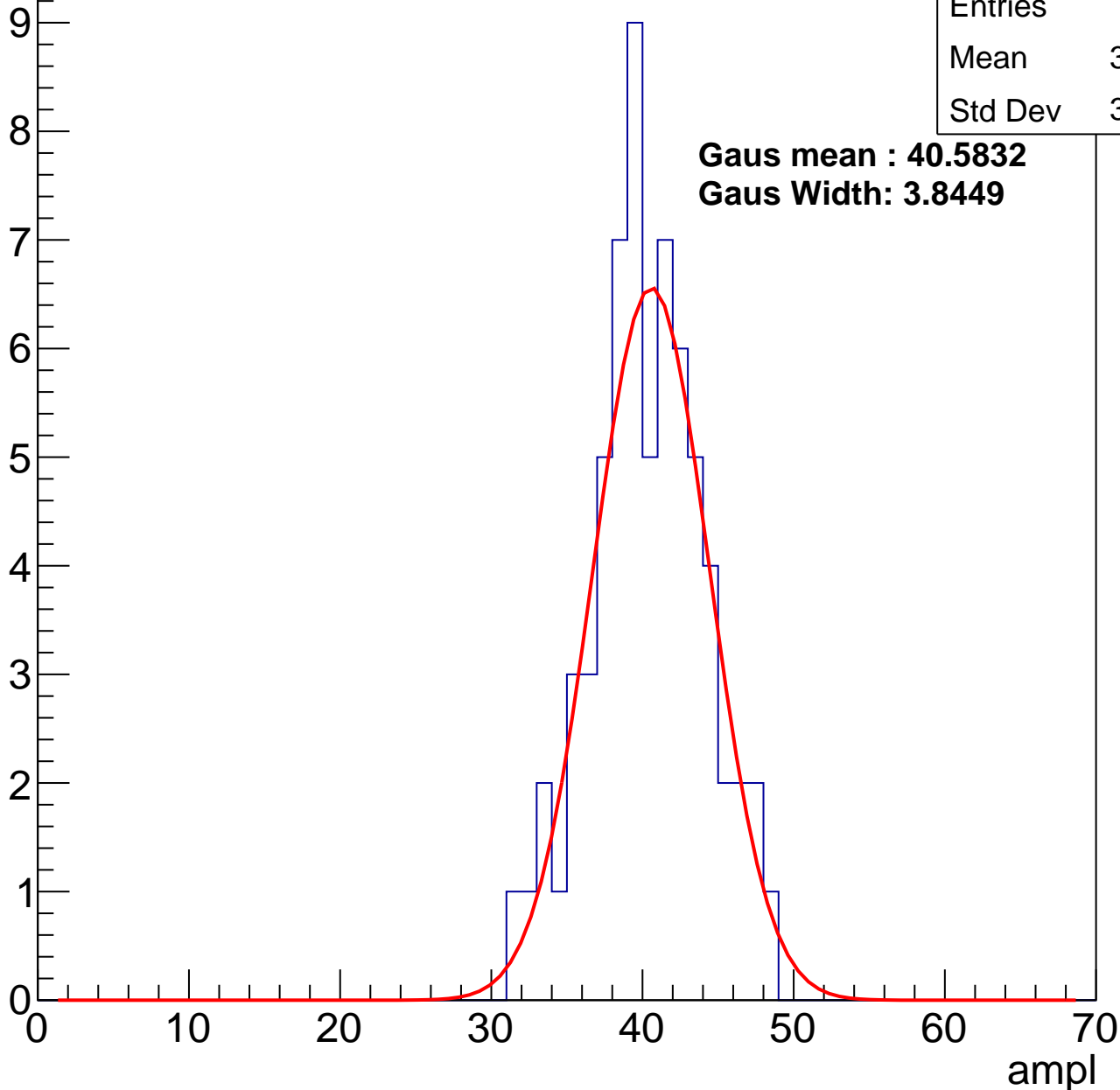
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	39.88
Std Dev	3.707

**Gaus mean : 40.5832**

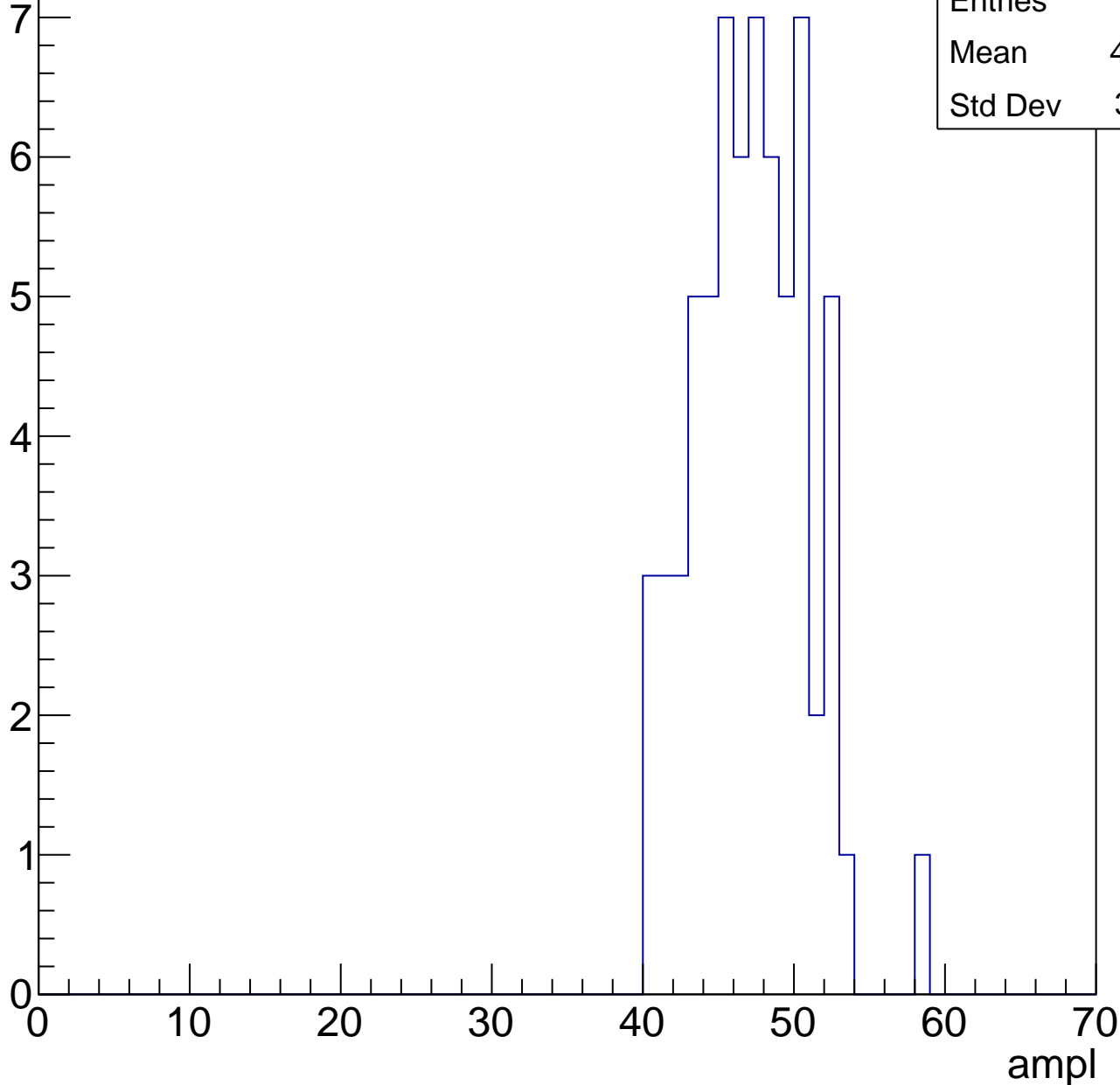
**Gaus Width: 3.8449**



# B1L101S, U3-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

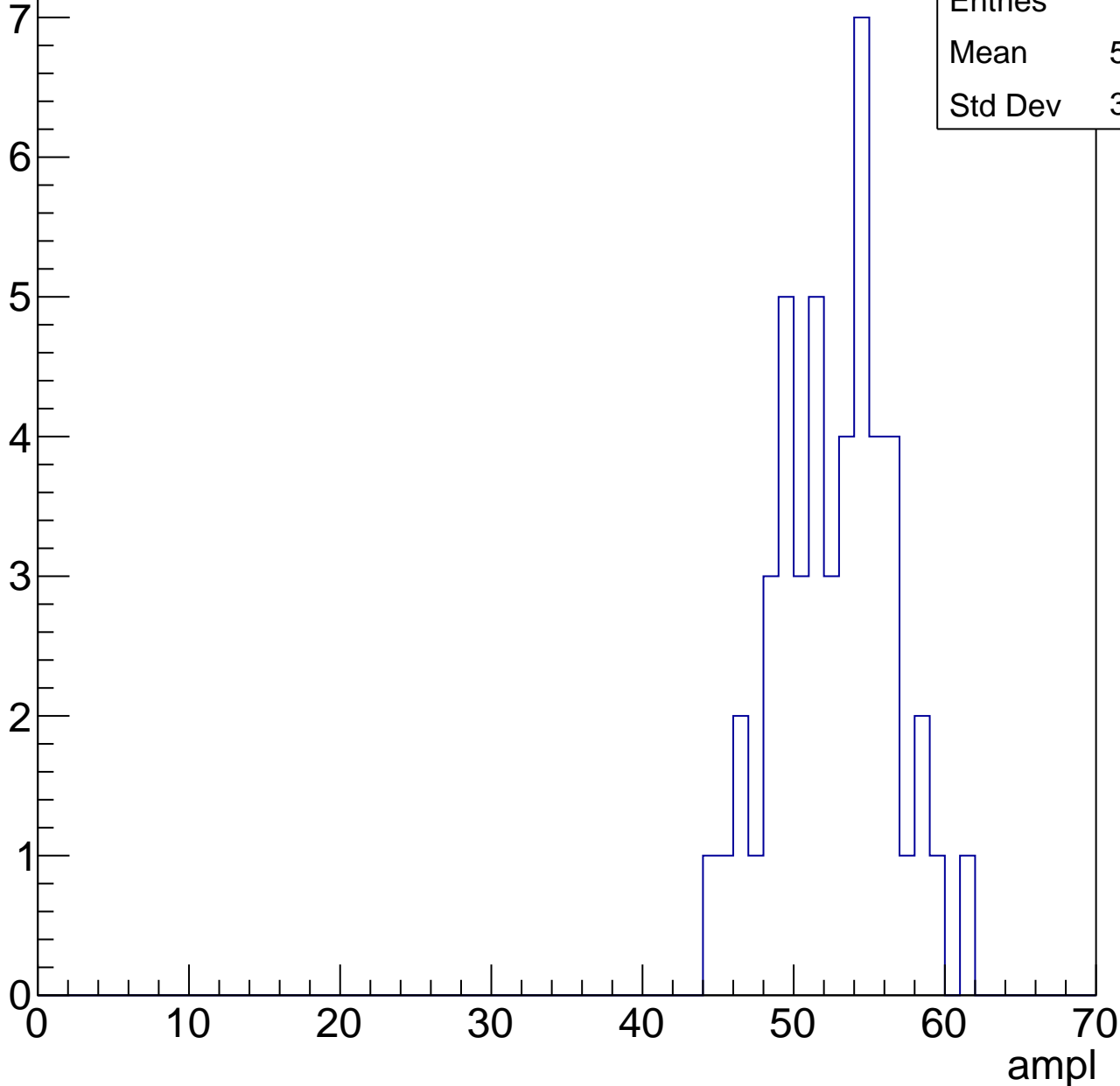


# B1L101S, U3-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

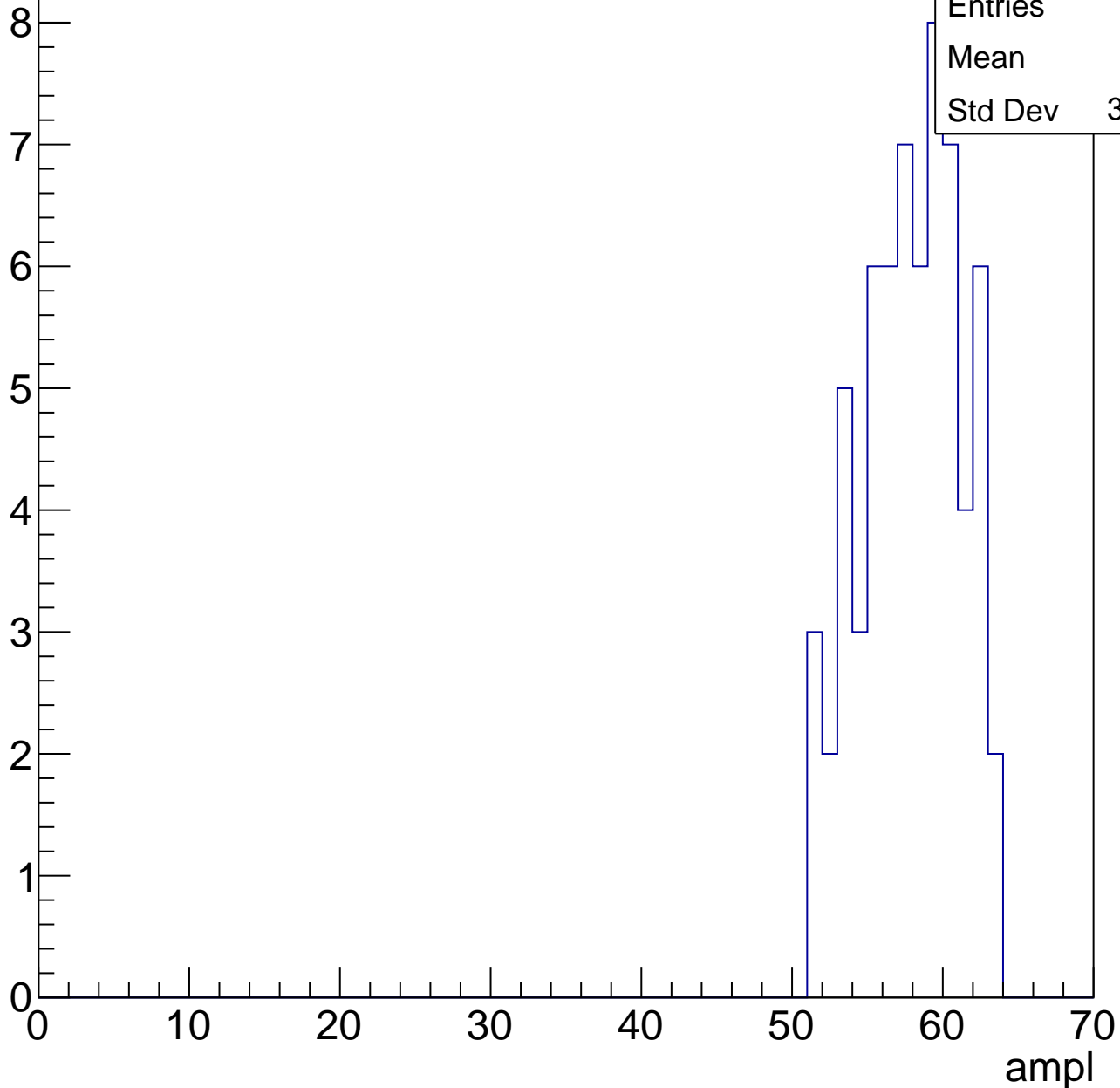
Entries	48
Mean	52.19
Std Dev	3.756



# B1L101S, U3-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

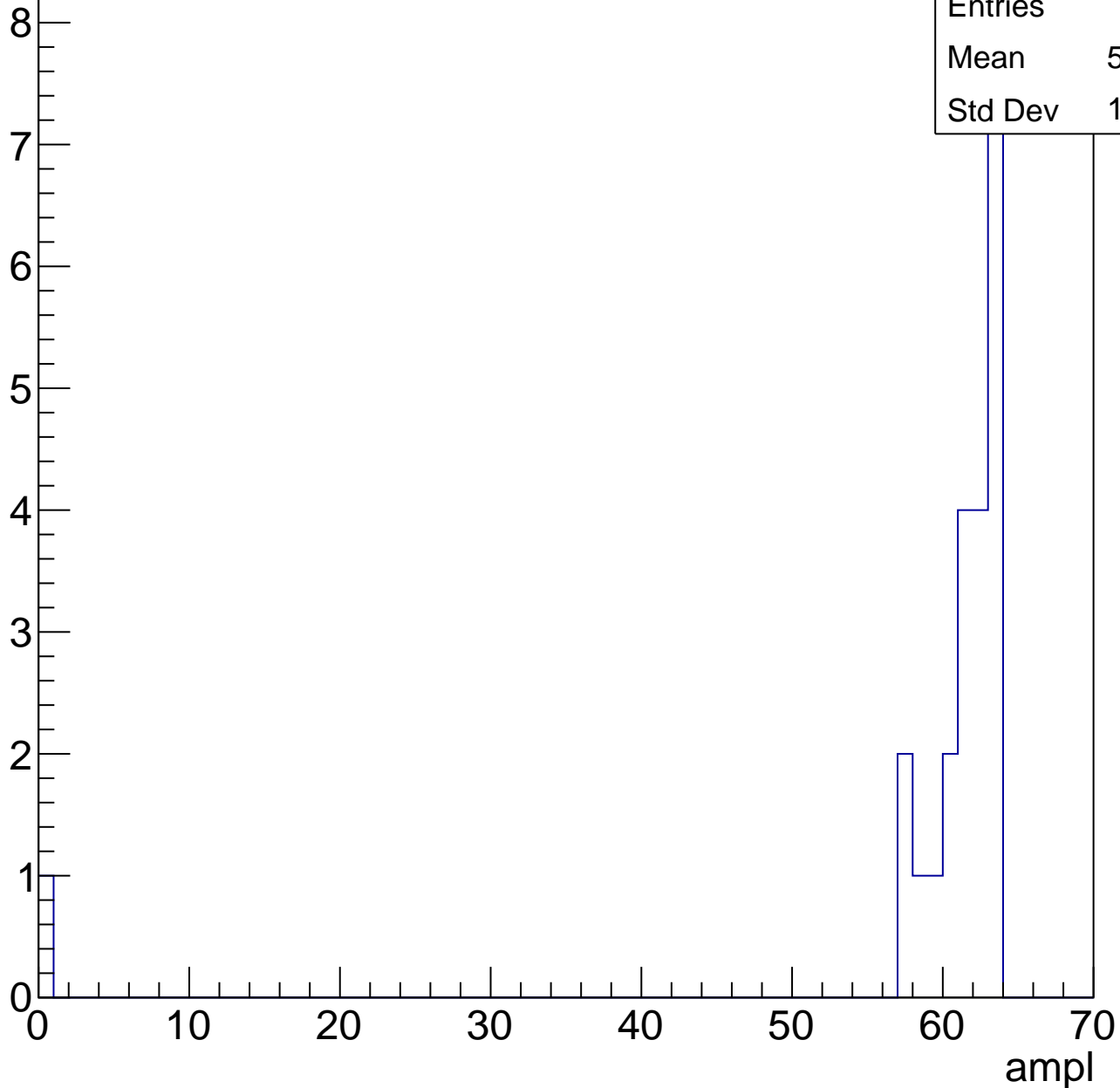


# B1L101S, U3-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	23
Mean	58.57
Std Dev	12.63

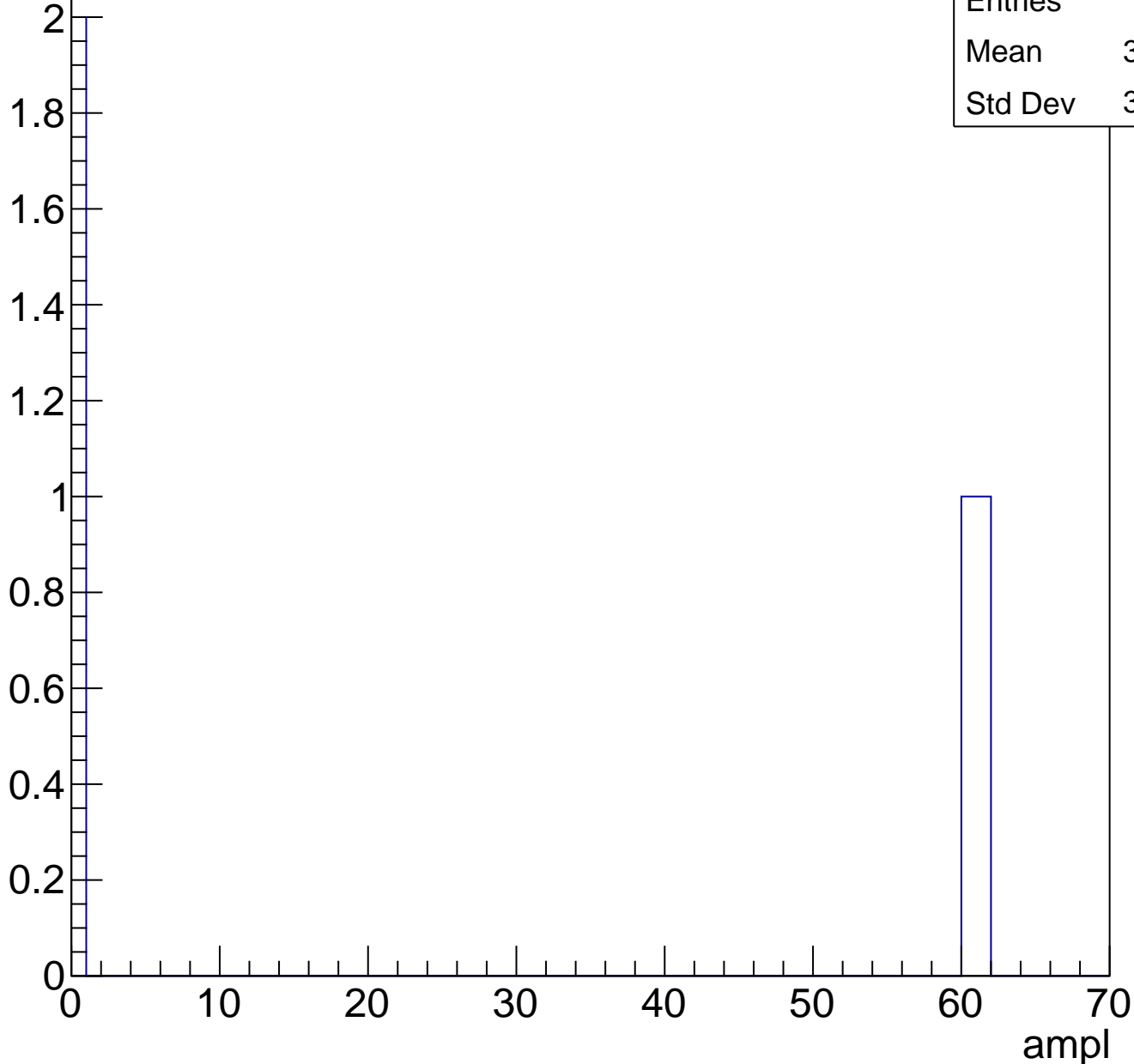




# B1L101S, U3-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch99, adc0

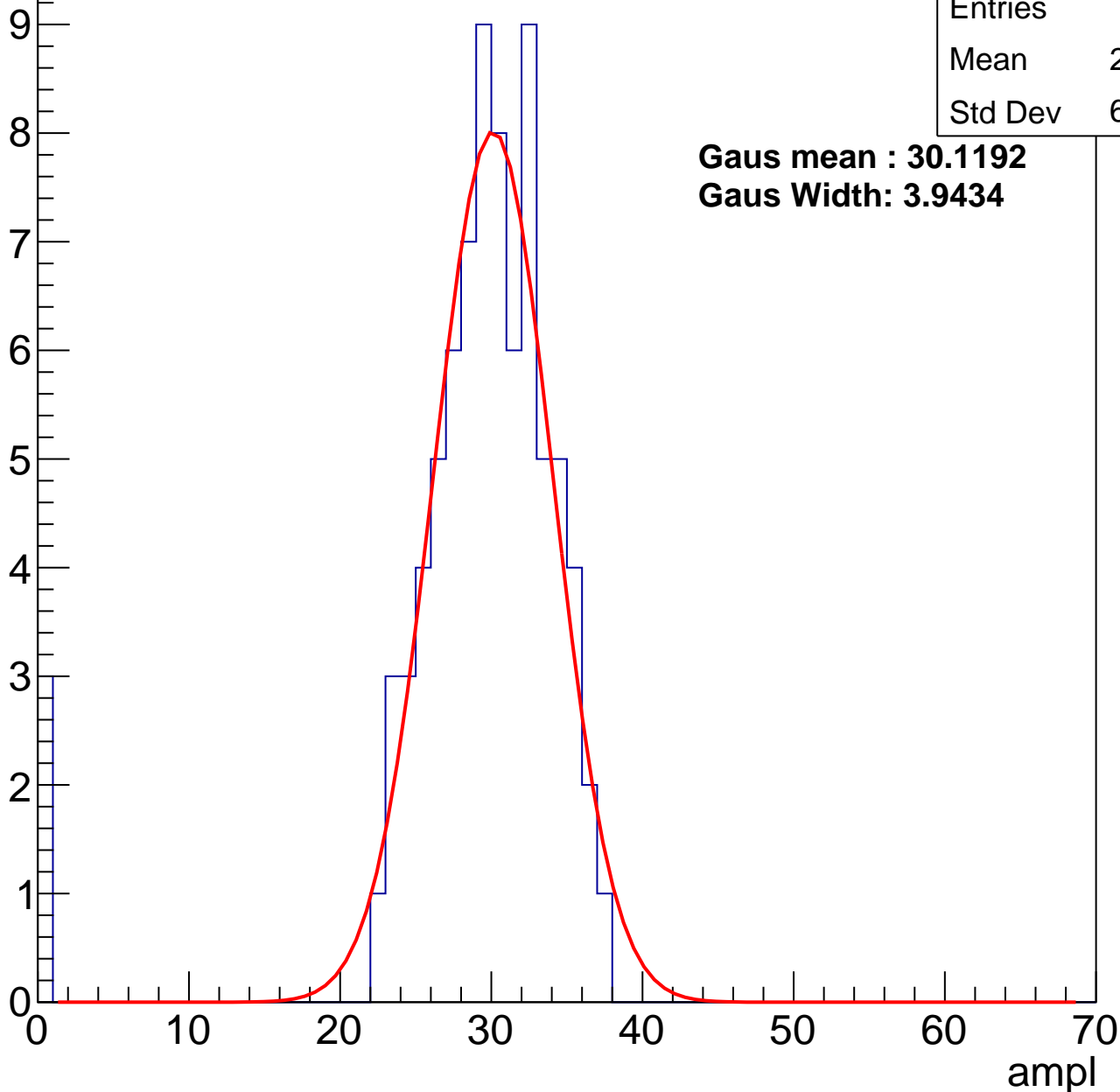
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	81
Mean	28.52
Std Dev	6.574

**Gaus mean : 30.1192**

**Gaus Width: 3.9434**



# B1L101S, U3-ch99, adc1

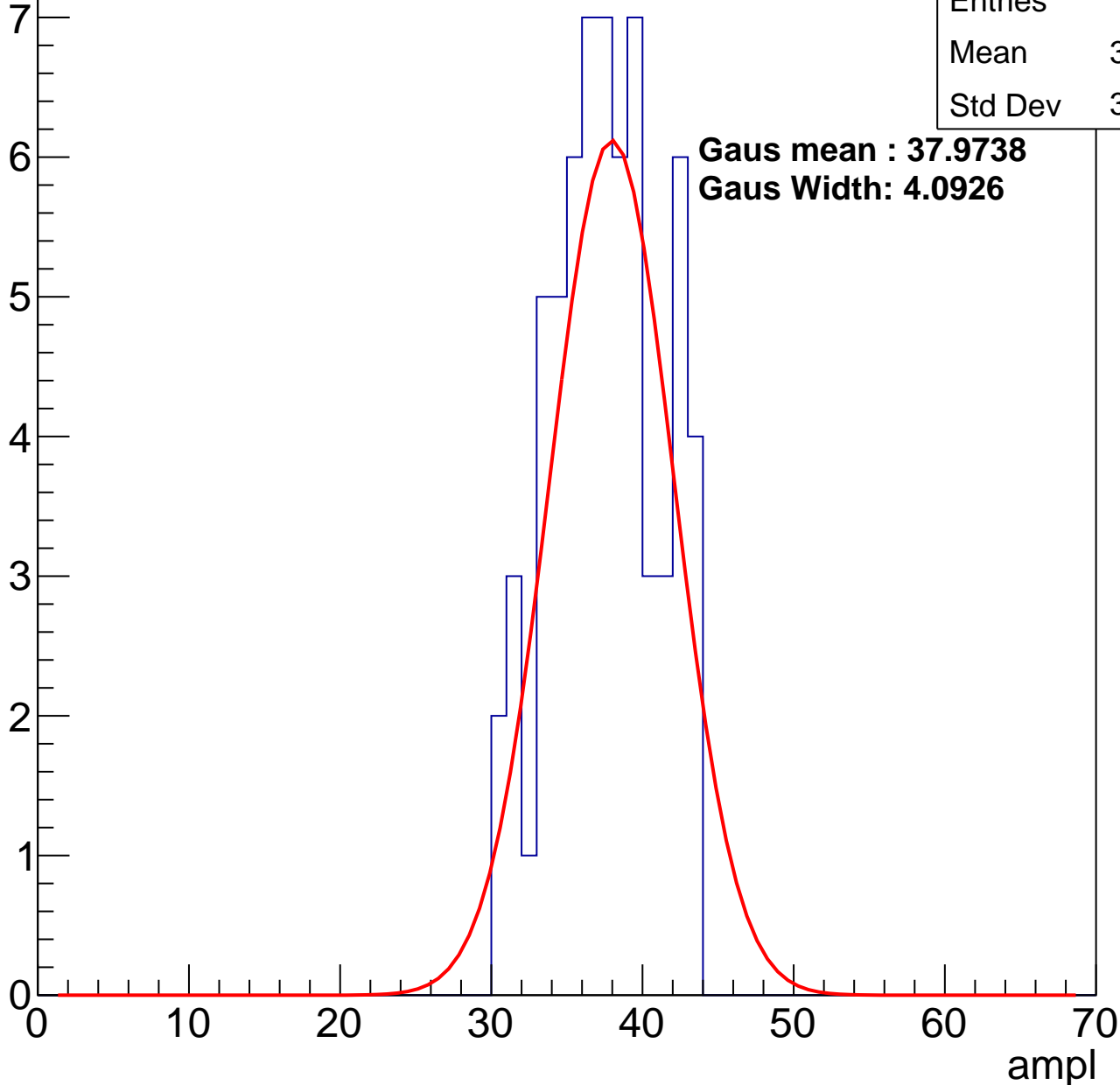
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	37.06
Std Dev	3.486

**Gaus mean : 37.9738**

**Gaus Width: 4.0926**



# B1L101S, U3-ch99, adc2

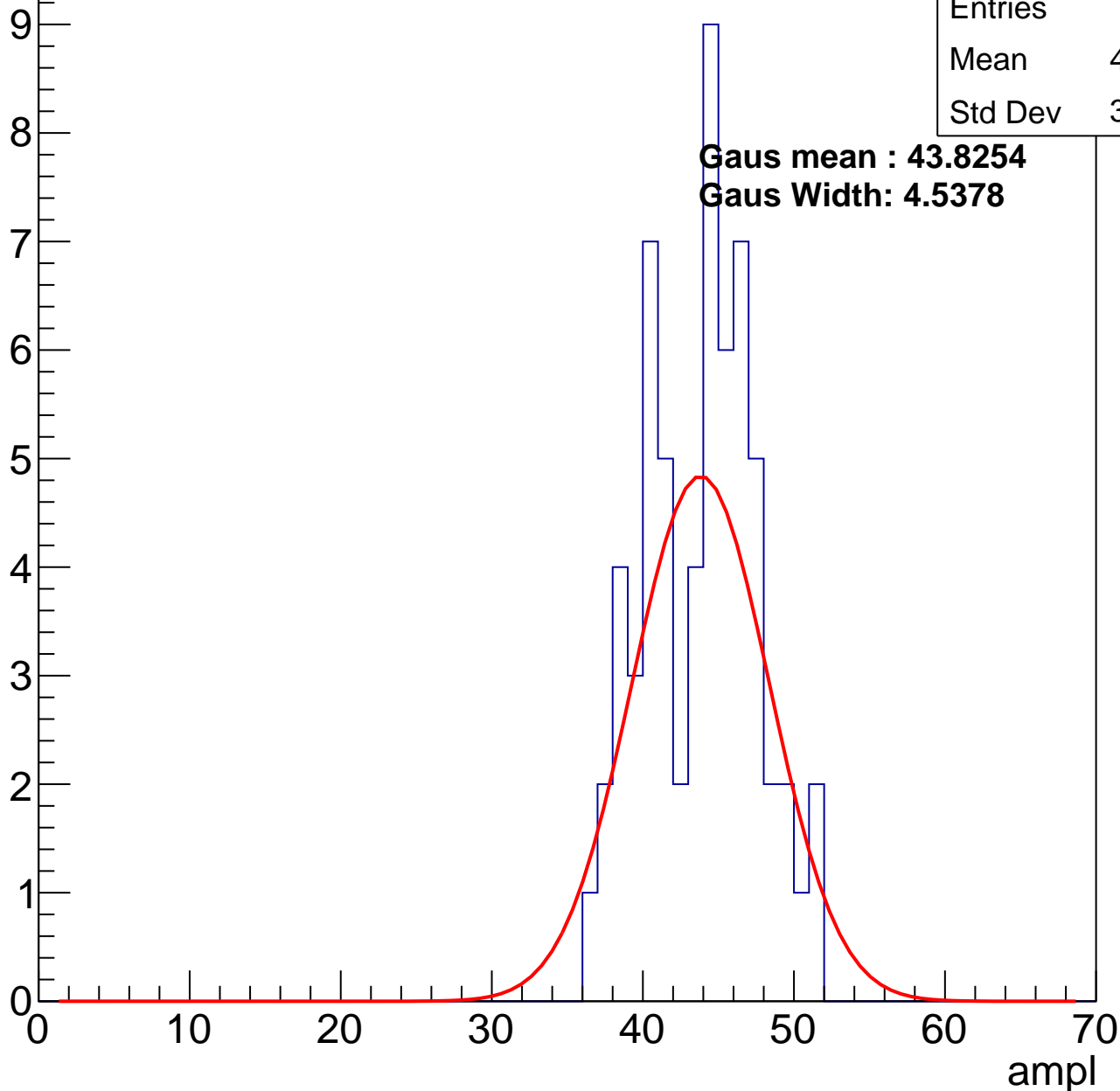
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	43.37
Std Dev	3.638

**Gaus mean : 43.8254**

**Gaus Width: 4.5378**

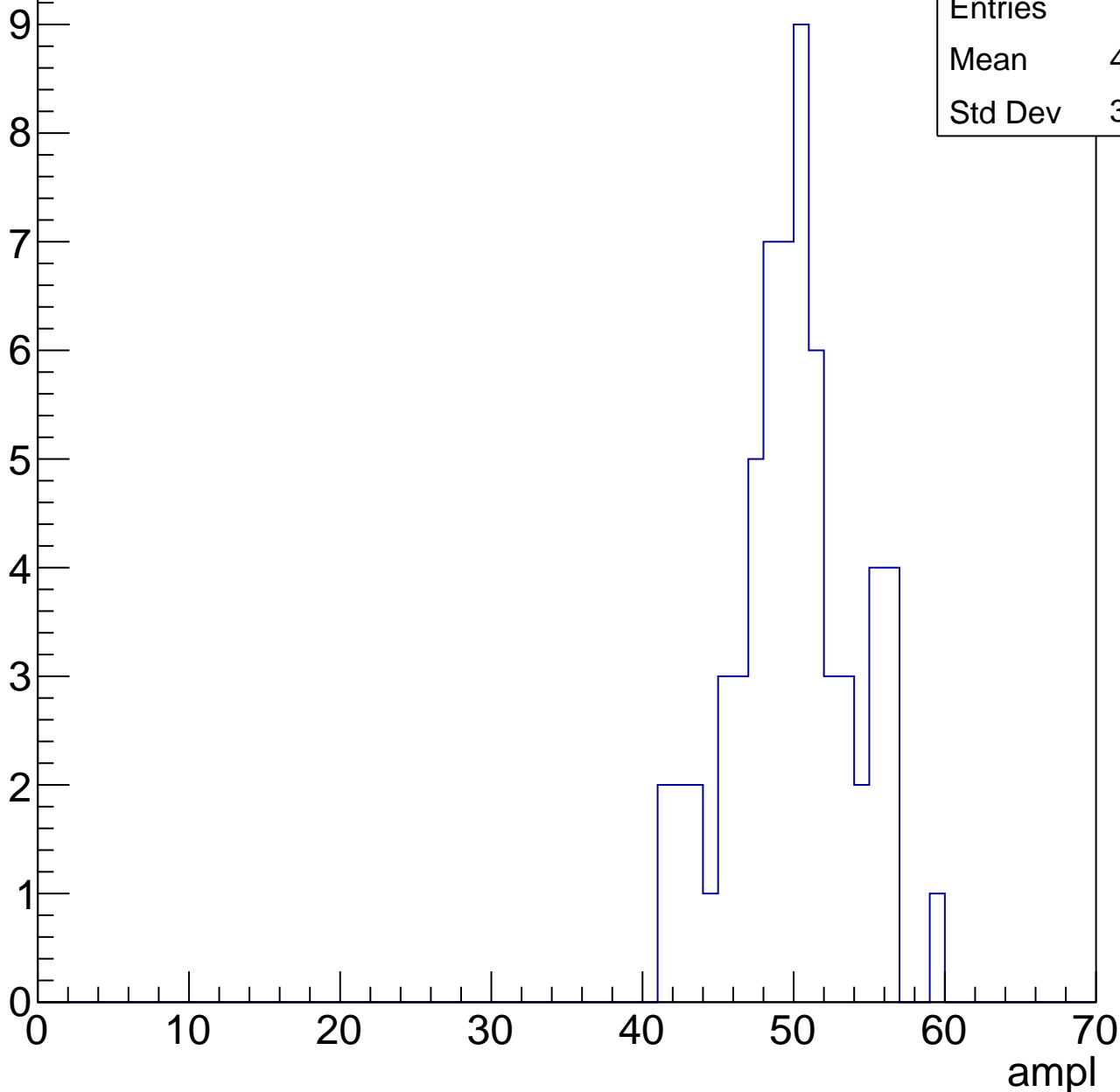


# B1L101S, U3-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	49.45
Std Dev	3.972

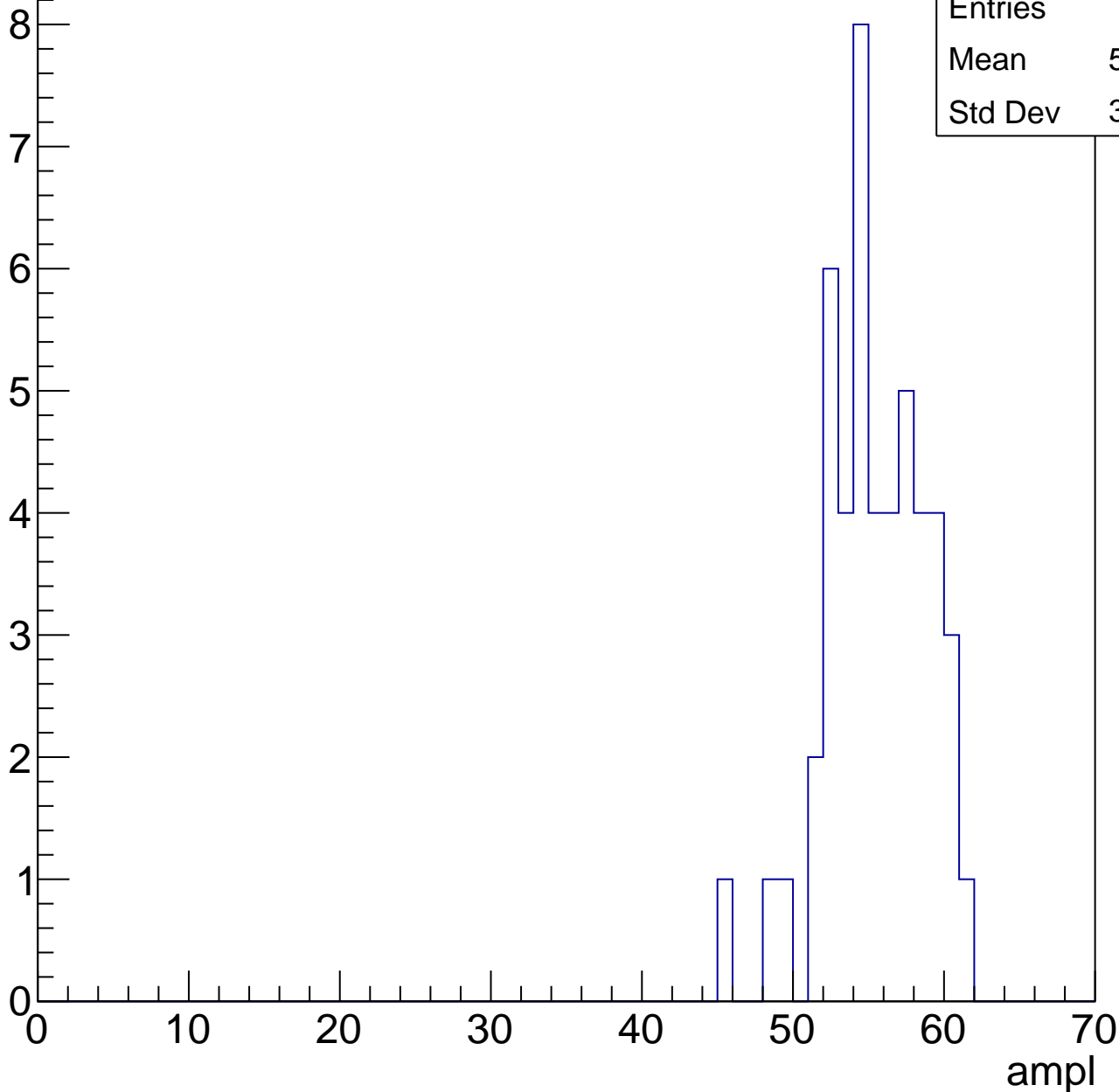


# B1L101S, U3-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	48
Mean	54.96
Std Dev	3.323

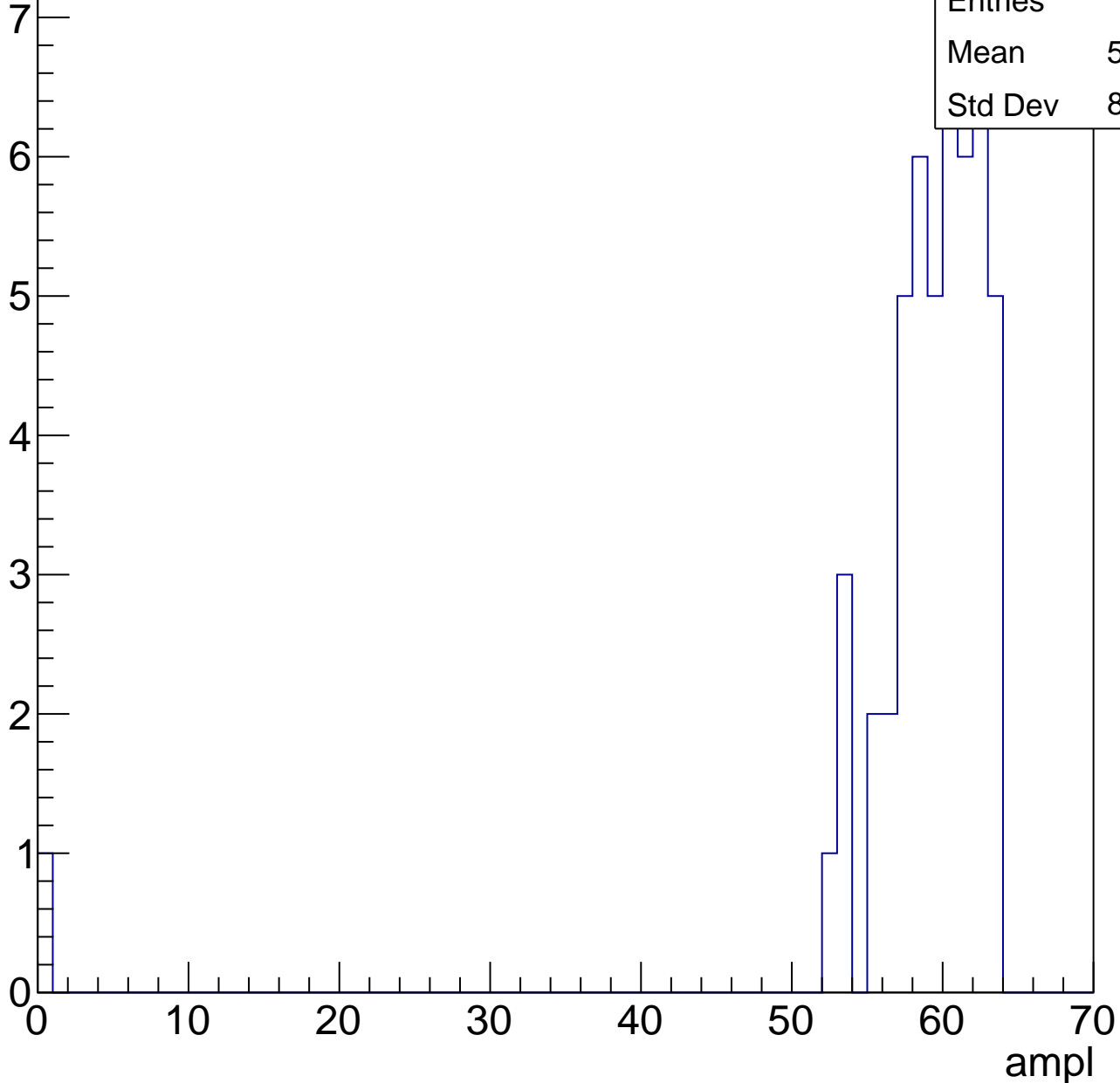


# B1L101S, U3-ch99, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	57.92
Std Dev	8.752

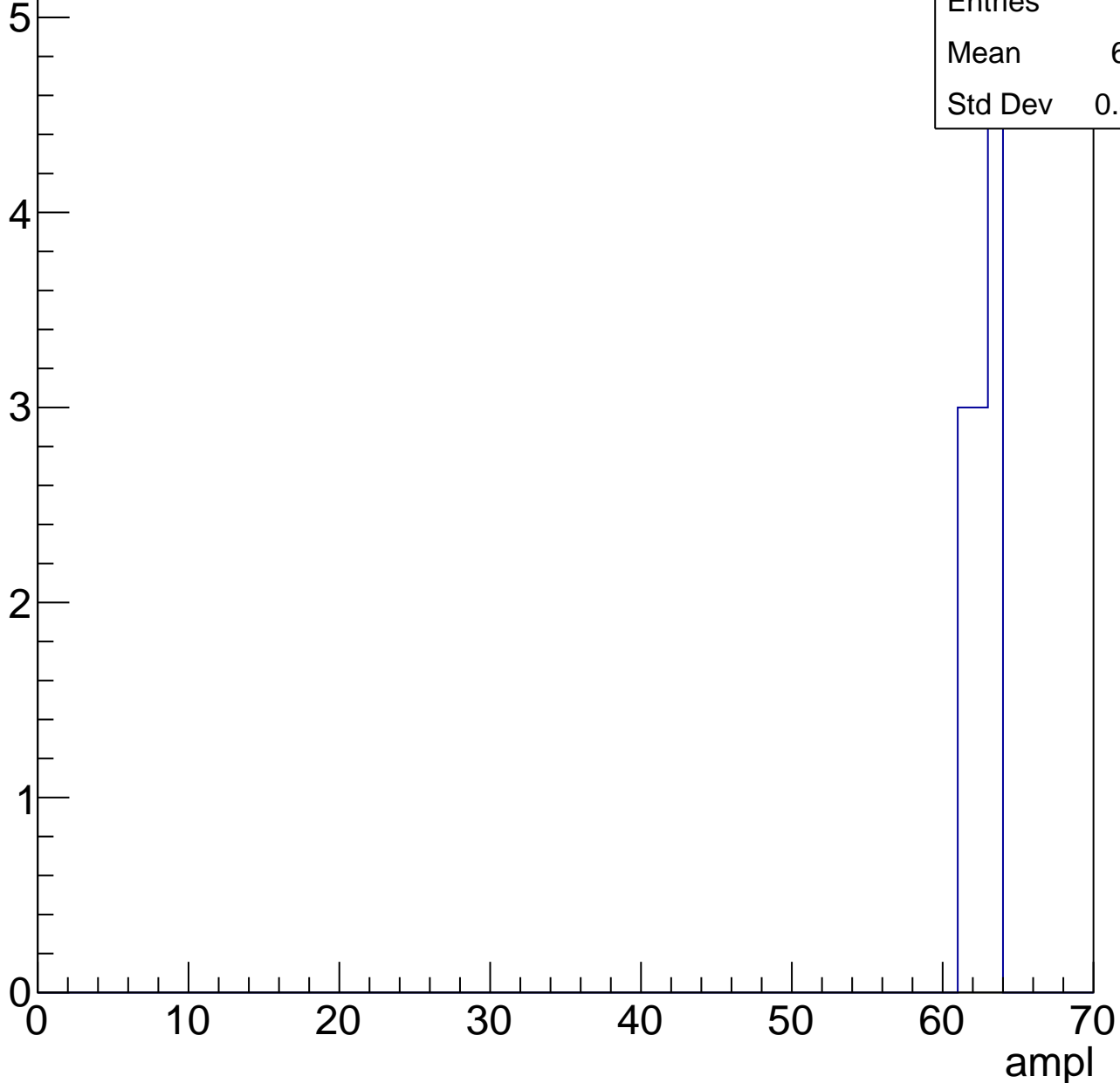


# B1L101S, U3-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	11
Mean	62.18
Std Dev	0.8332





# B1L101S, U3-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch100, adc0

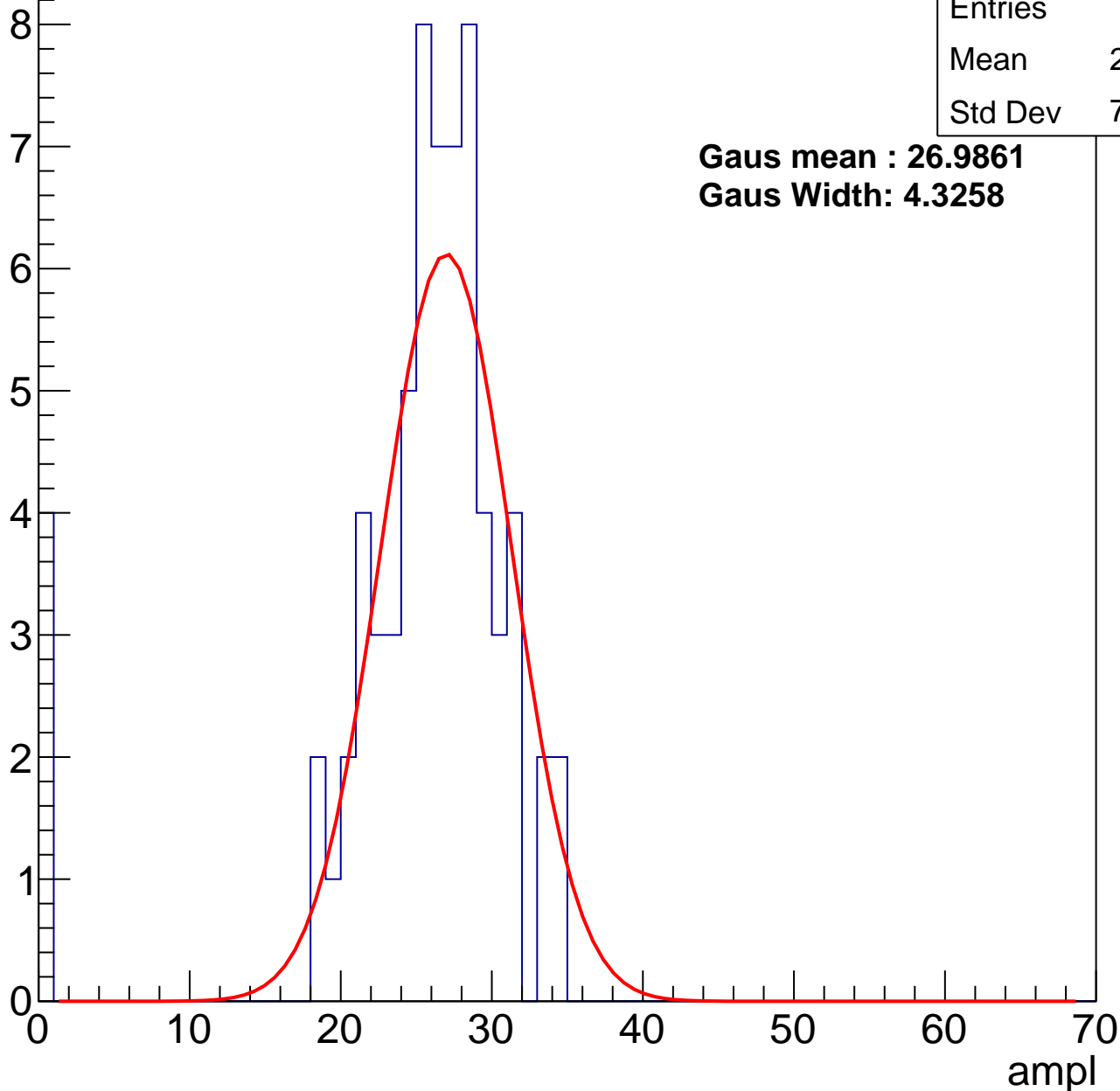
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	24.54
Std Dev	7.078

**Gaus mean : 26.9861**

**Gaus Width: 4.3258**



# B1L101S, U3-ch100, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	66
Mean	32.48
Std Dev	3.434

**Gaus mean : 32.6234**

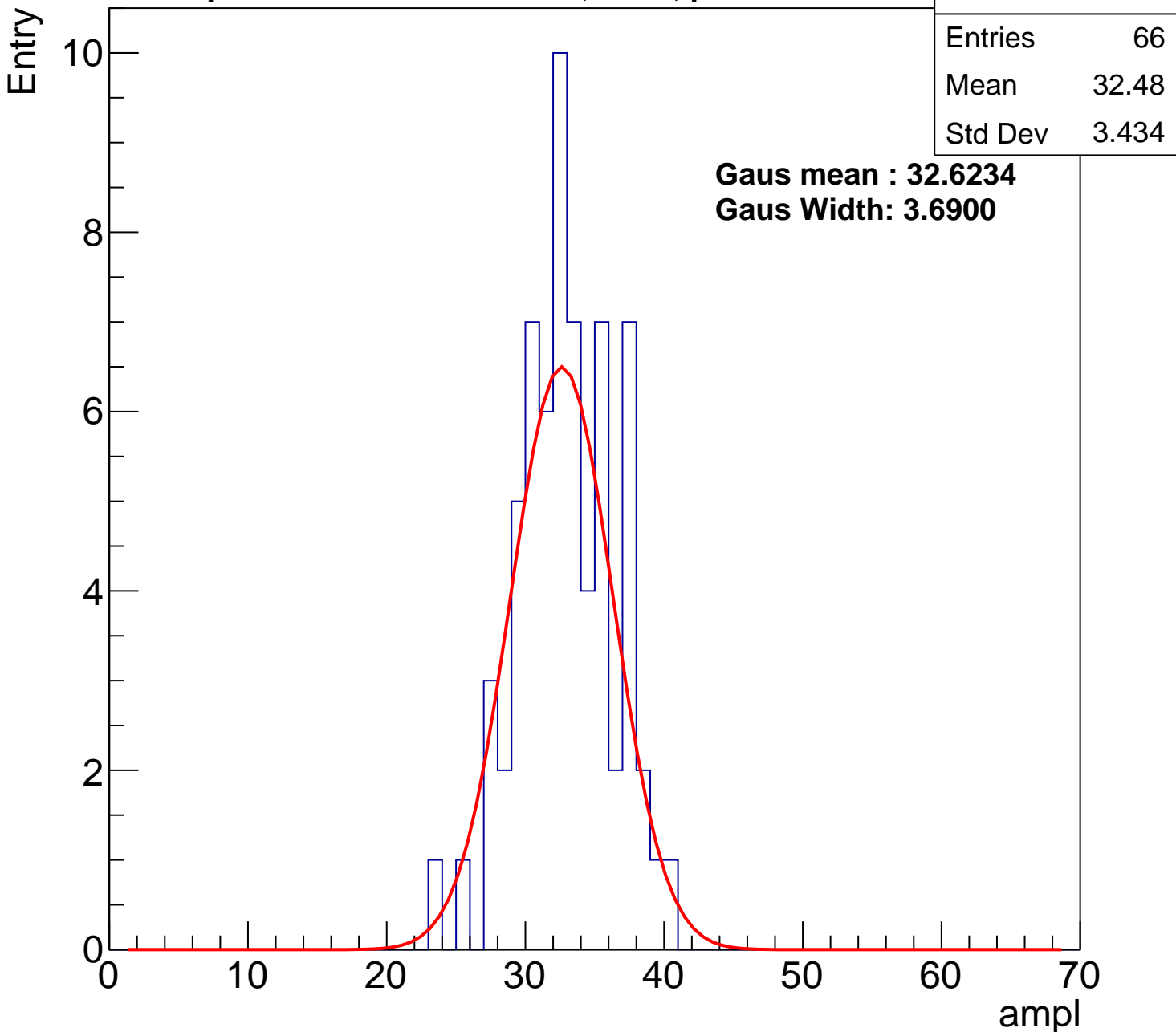
**Gaus Width: 3.6900**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U3-ch100, adc2

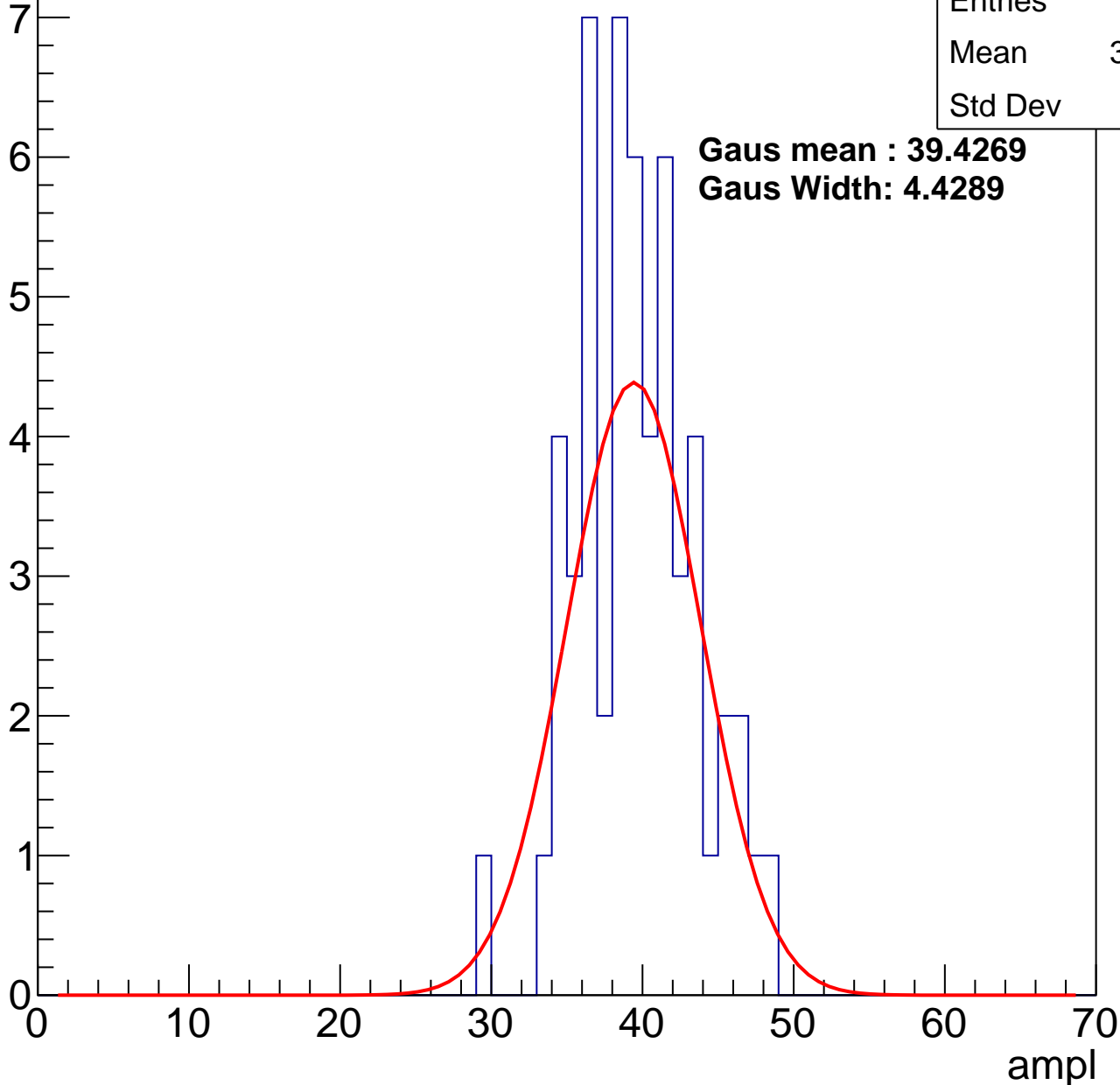
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	39.16
Std Dev	3.86

**Gaus mean : 39.4269**

**Gaus Width: 4.4289**

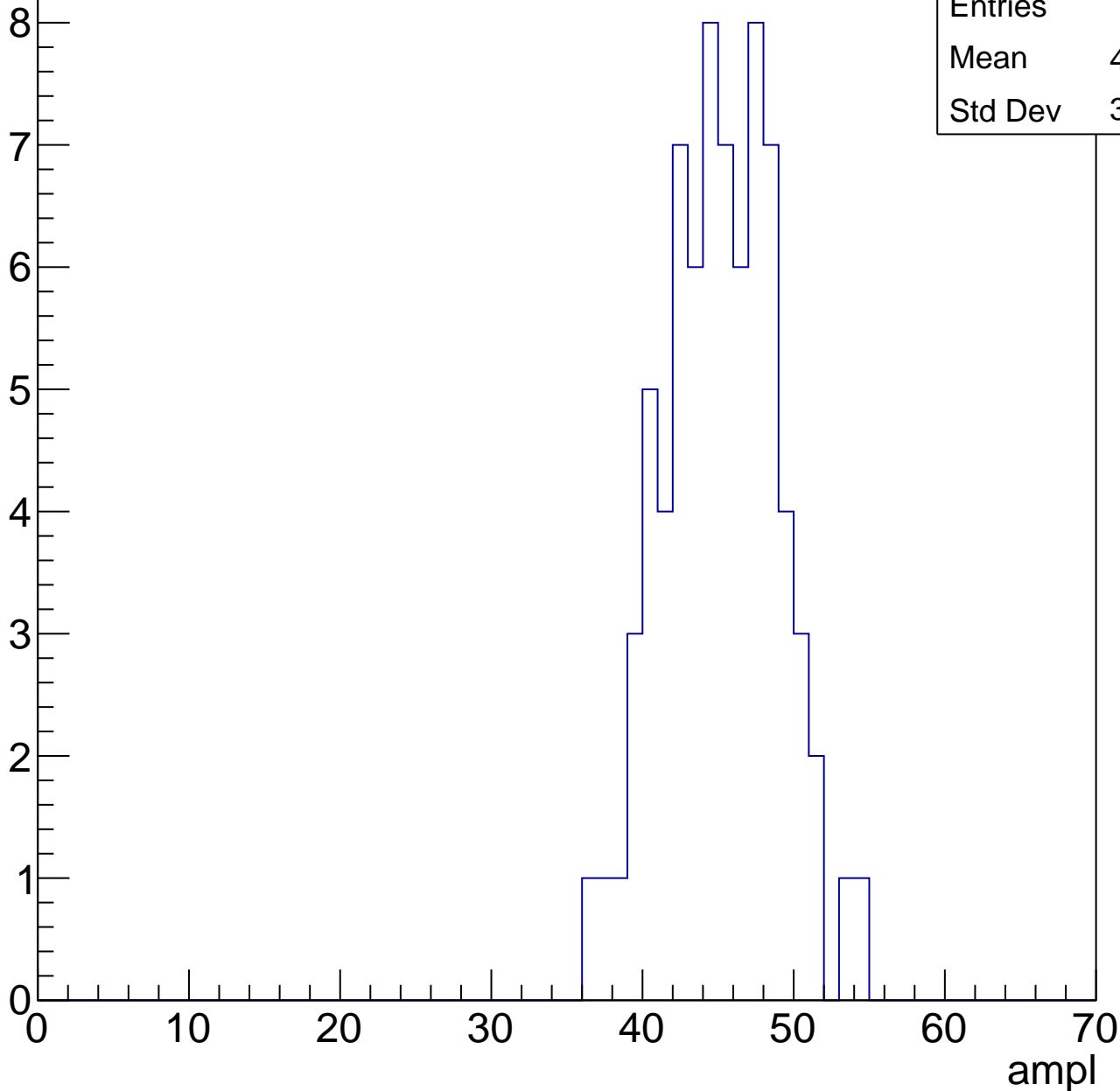


# B1L101S, U3-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	44.72
Std Dev	3.719

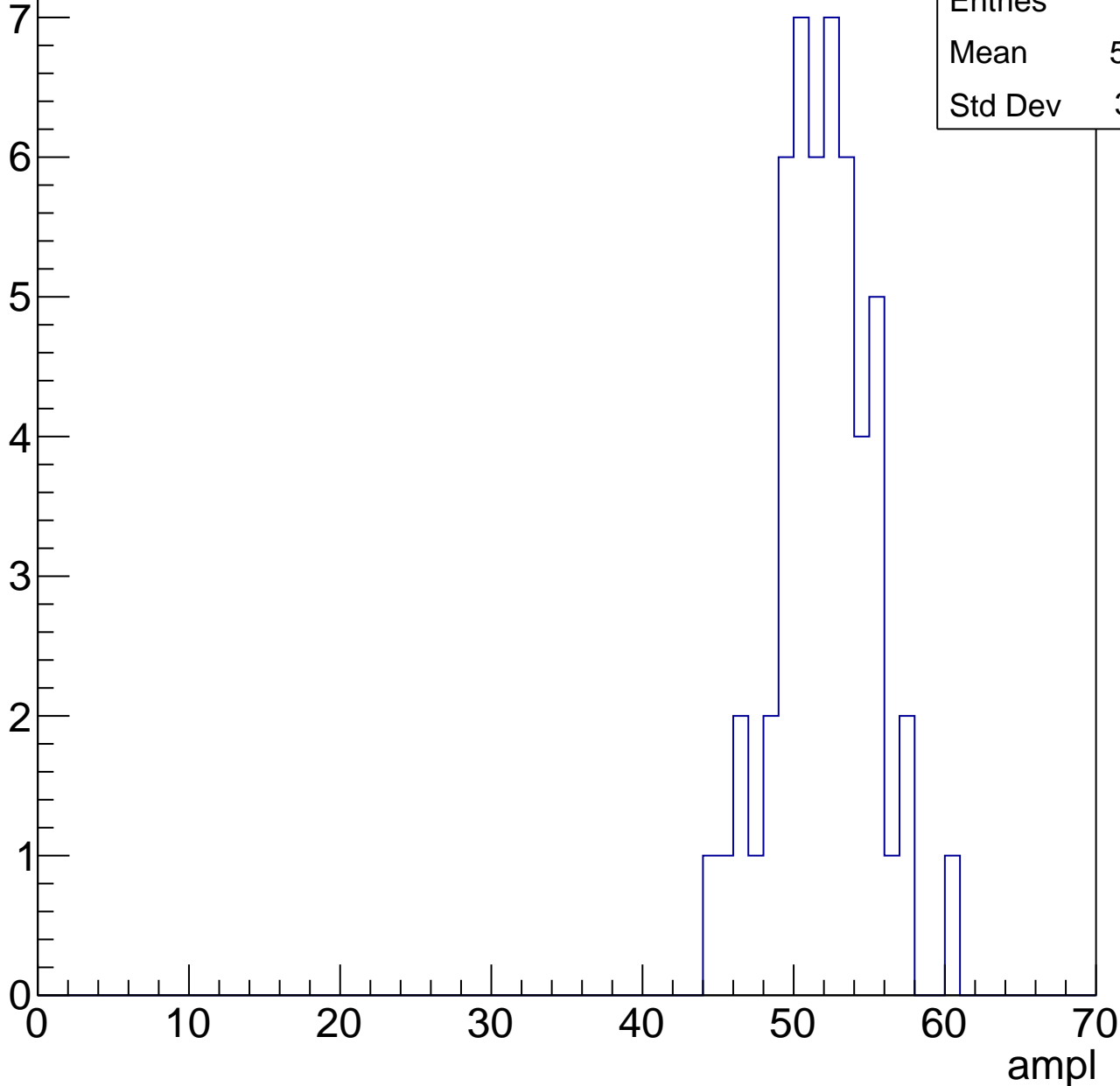


# B1L101S, U3-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

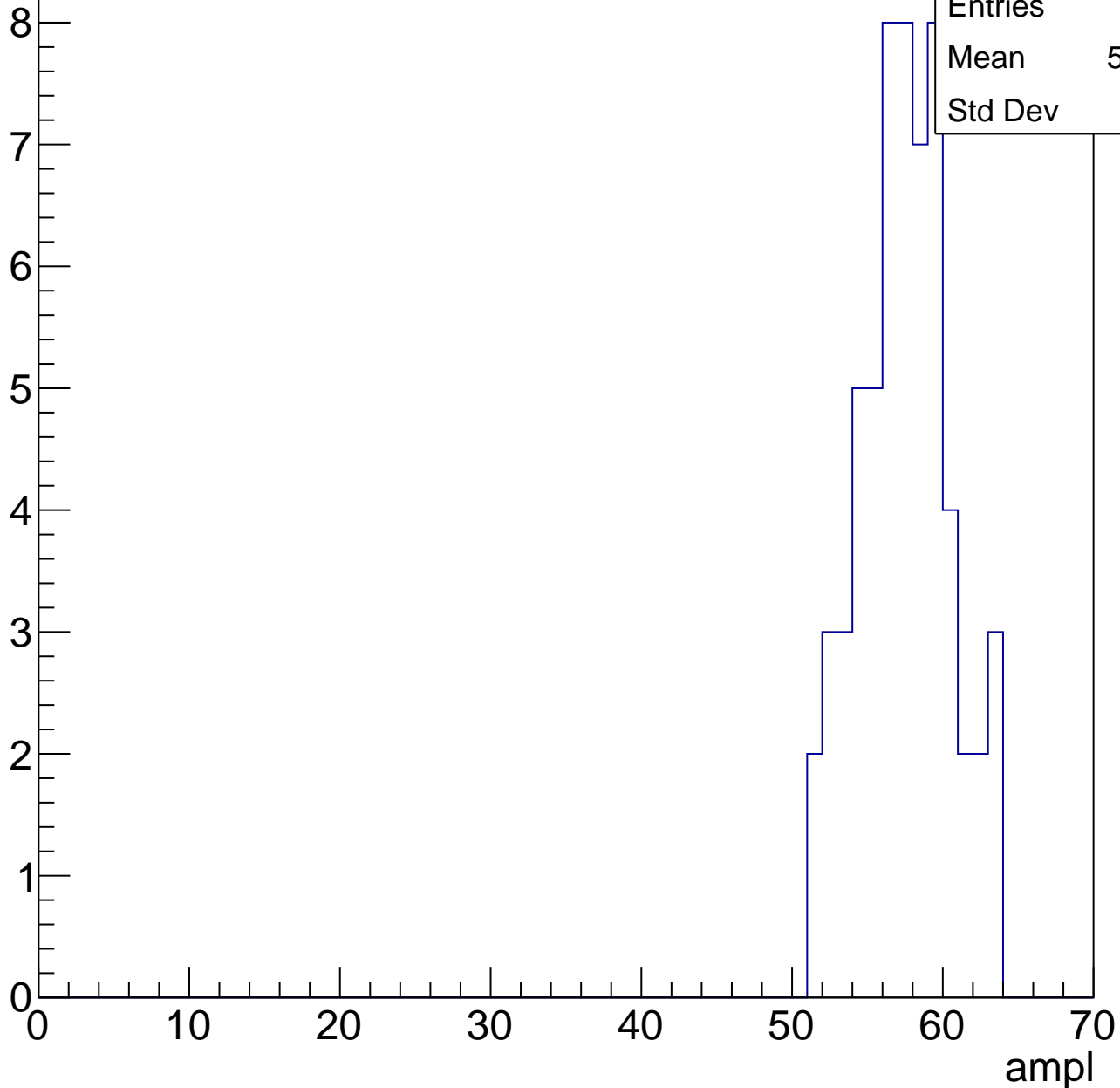
Entries	52
Mean	51.48
Std Dev	3.141



# B1L101S, U3-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

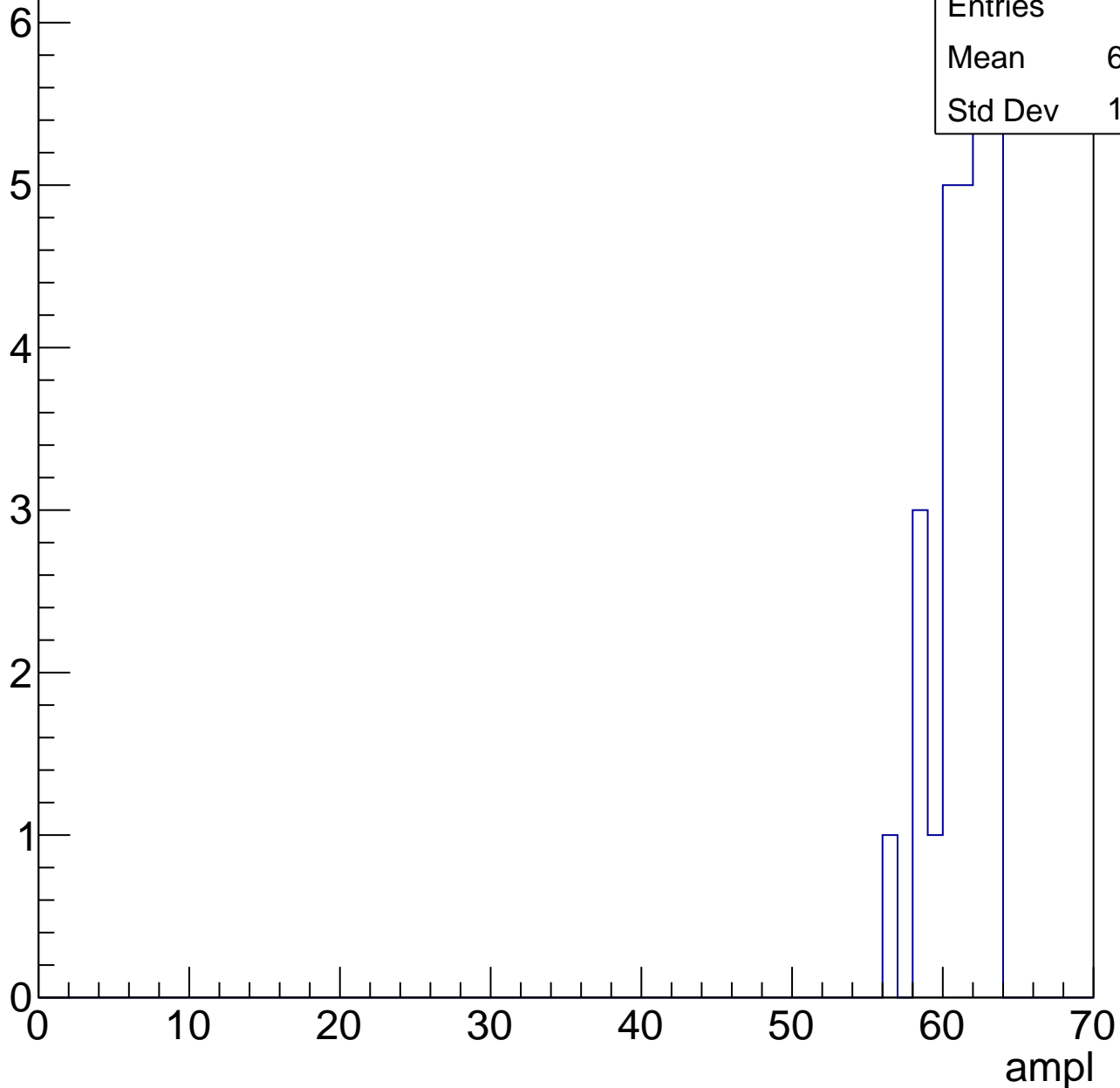
Entry



# B1L101S, U3-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



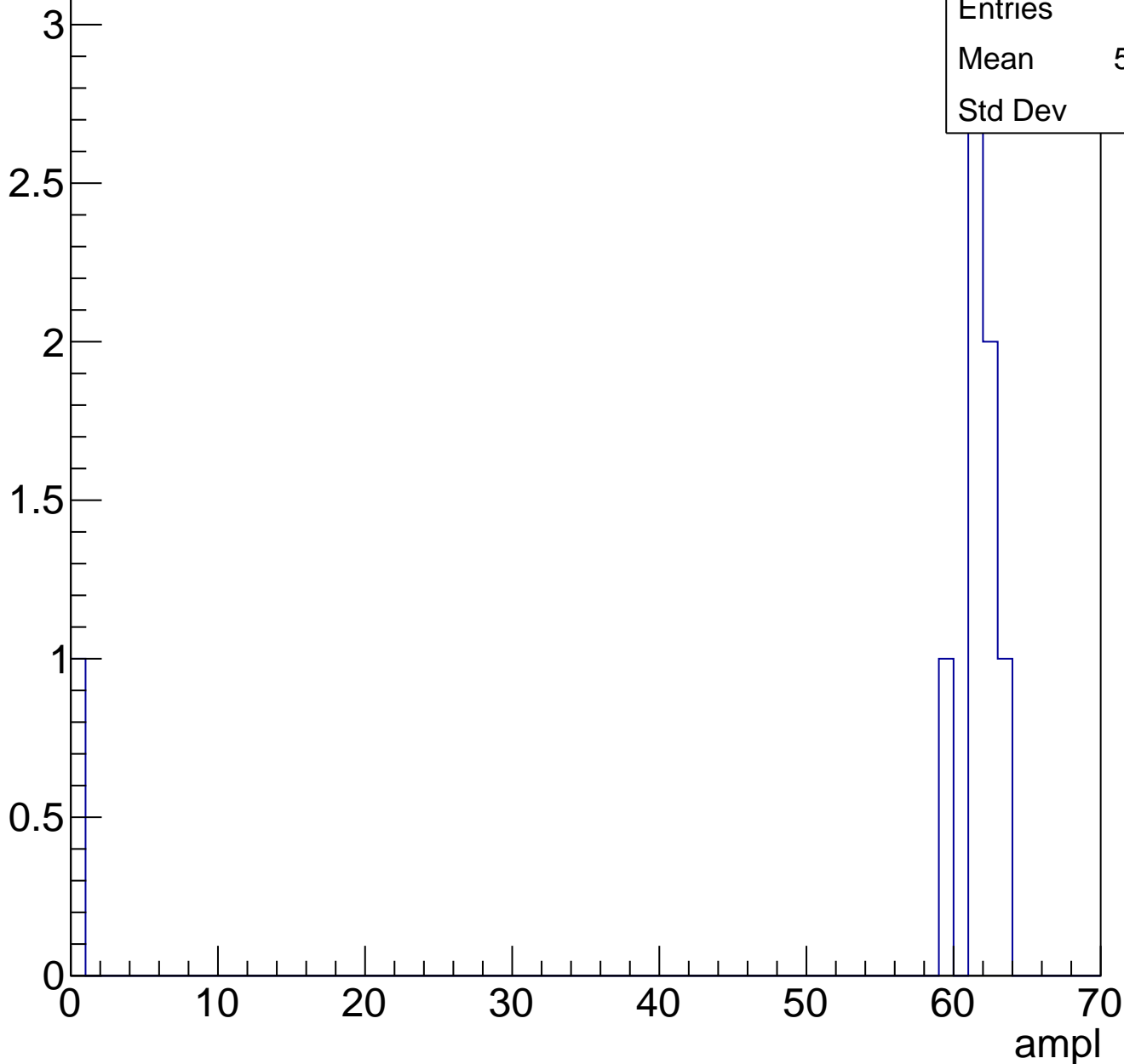
Entries	27
Mean	60.89
Std Dev	1.832



# B1L101S, U3-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch101, adc0

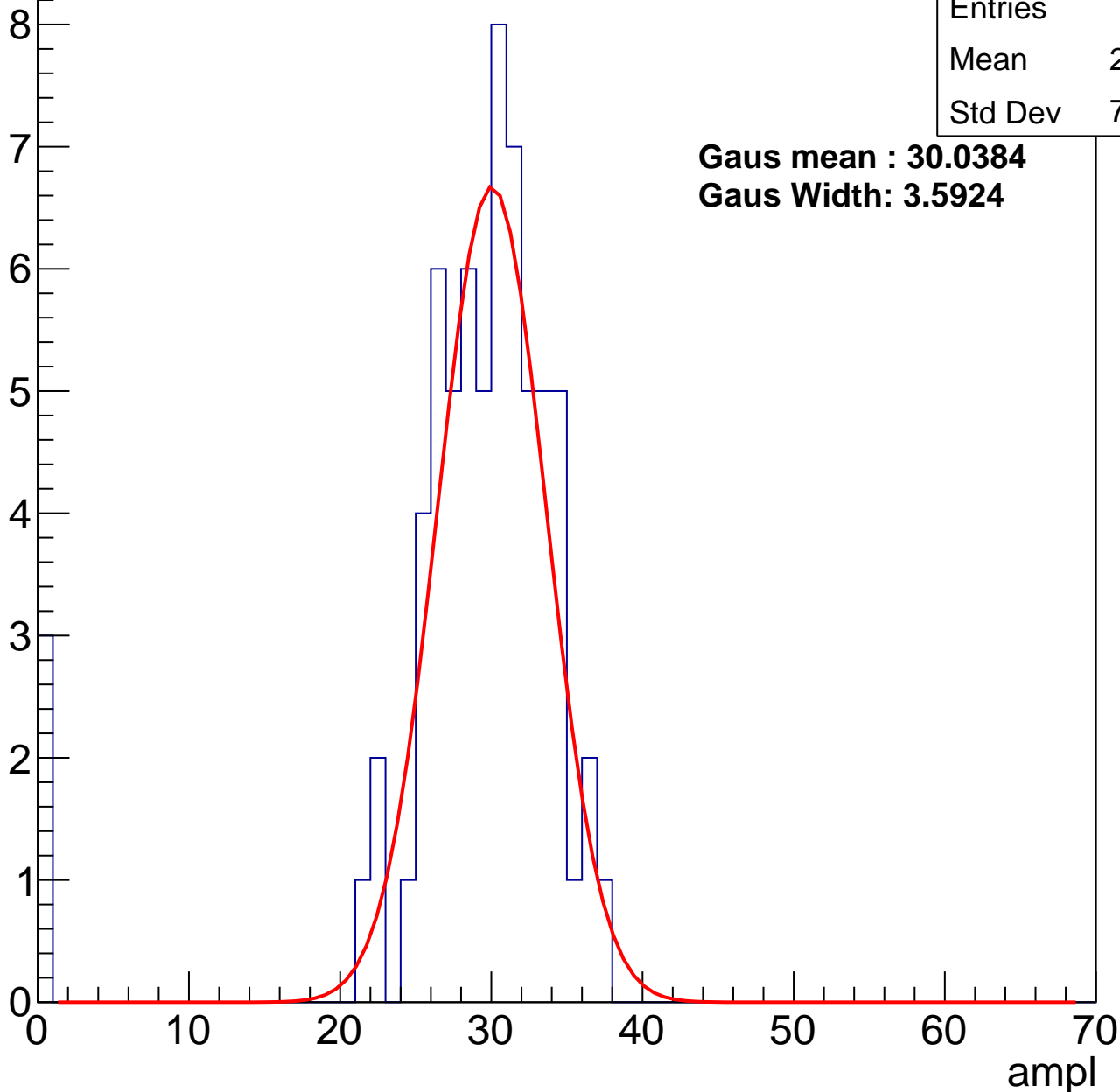
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	28.19
Std Dev	7.012

**Gaus mean : 30.0384**

**Gaus Width: 3.5924**



# B1L101S, U3-ch101, adc1

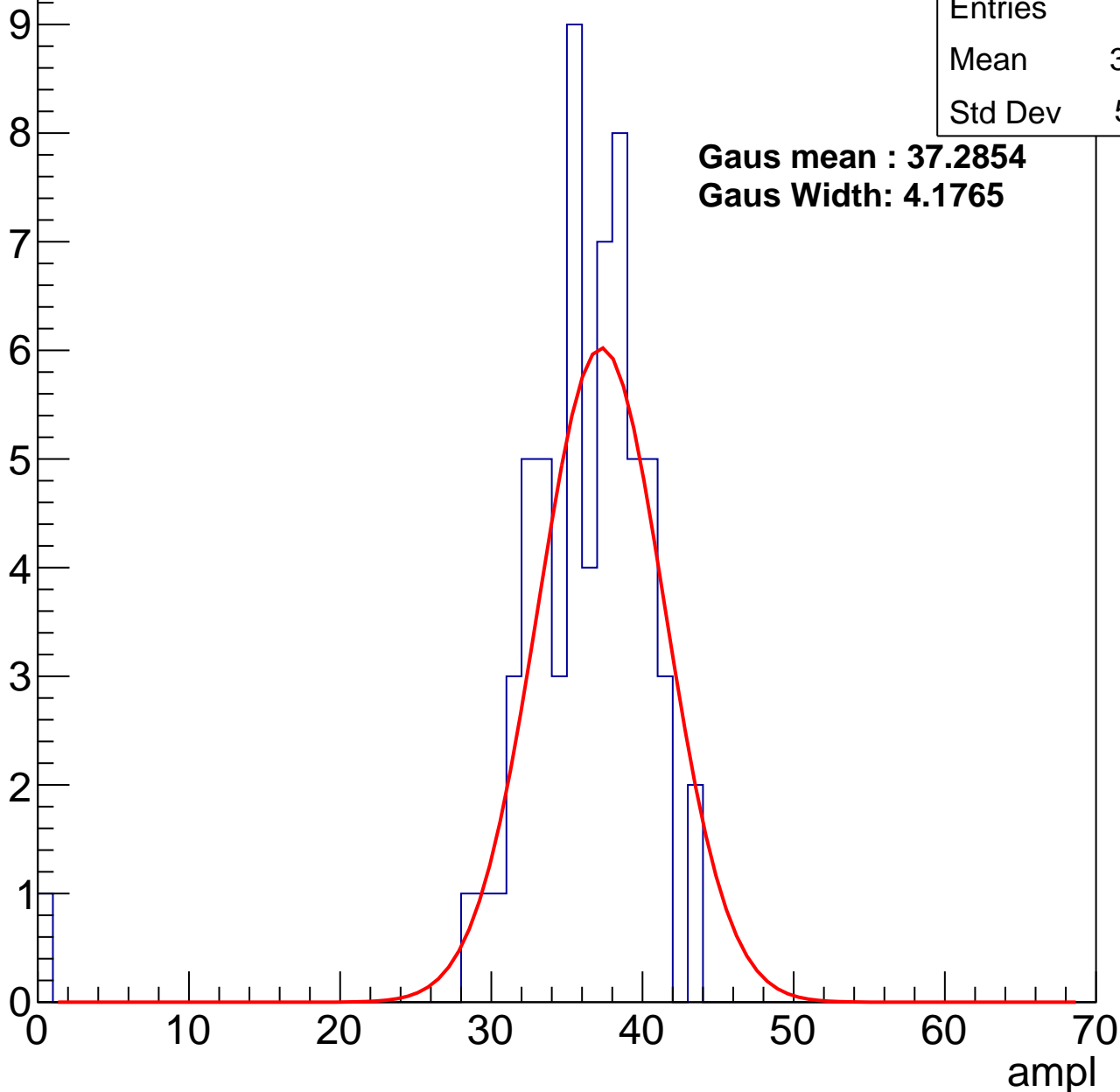
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	35.44
Std Dev	5.611

**Gaus mean : 37.2854**

**Gaus Width: 4.1765**



# B1L101S, U3-ch101, adc2

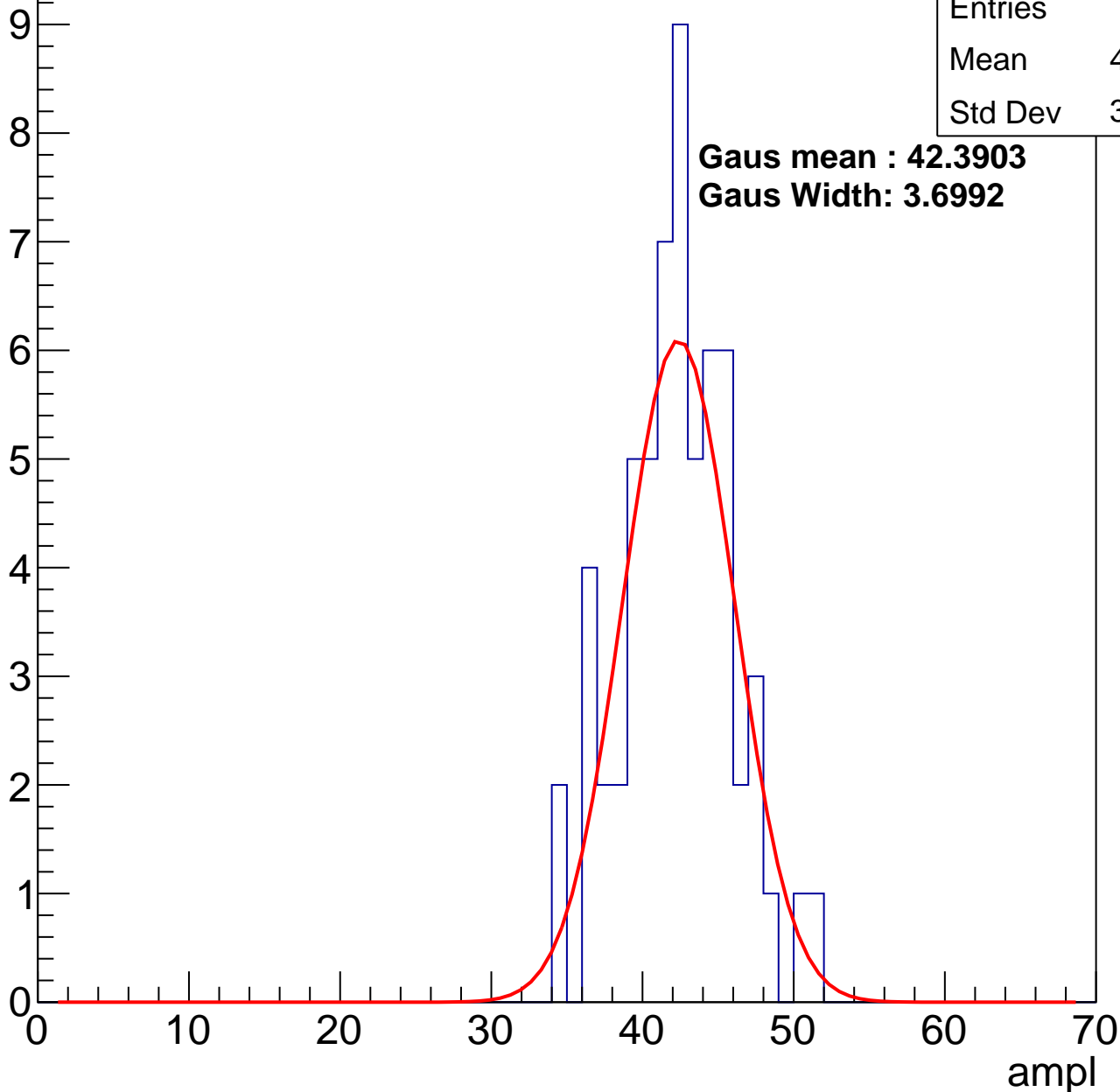
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	41.85
Std Dev	3.612

**Gaus mean : 42.3903**

**Gaus Width: 3.6992**

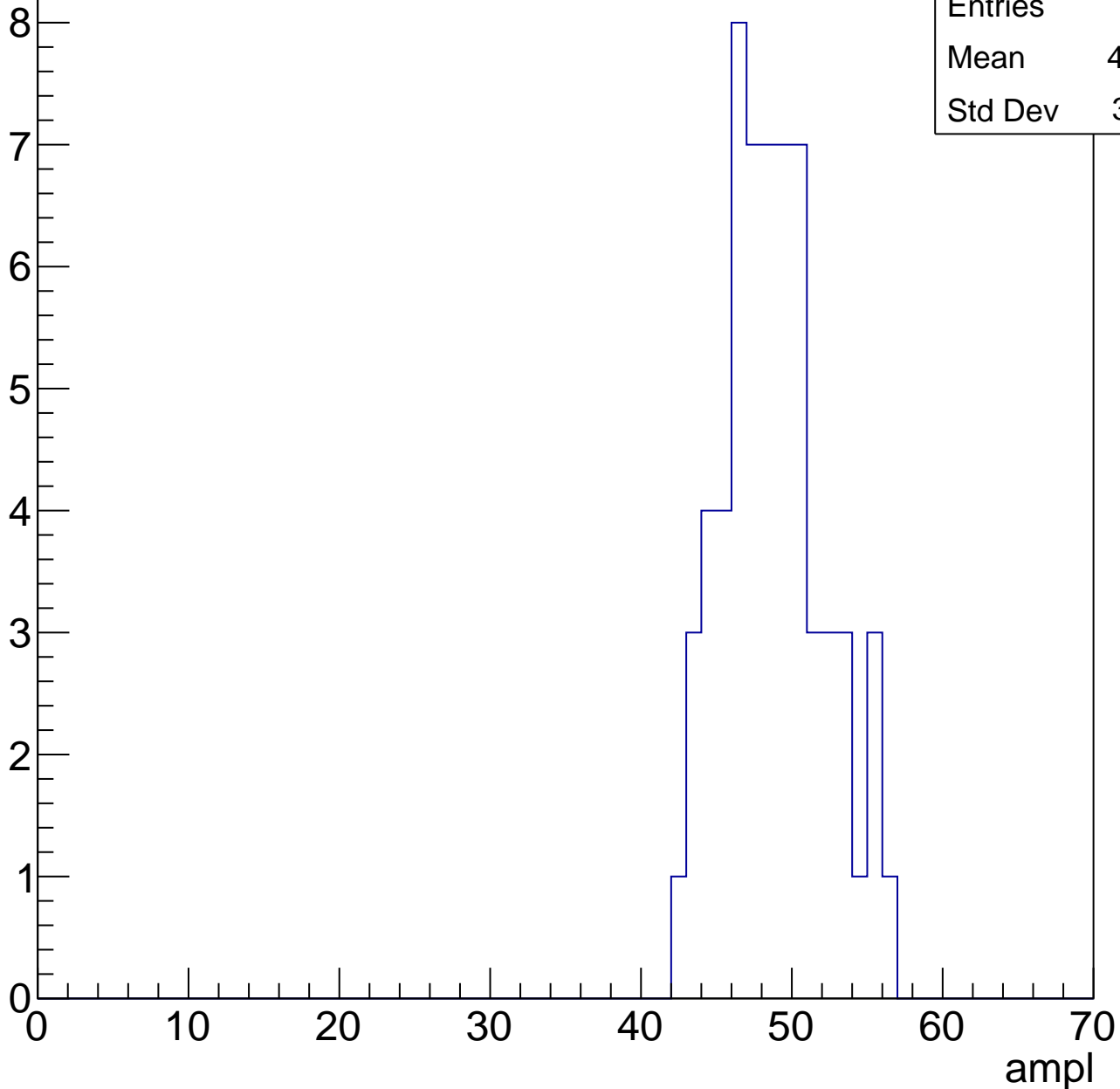


# B1L101S, U3-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	48.32
Std Dev	3.301

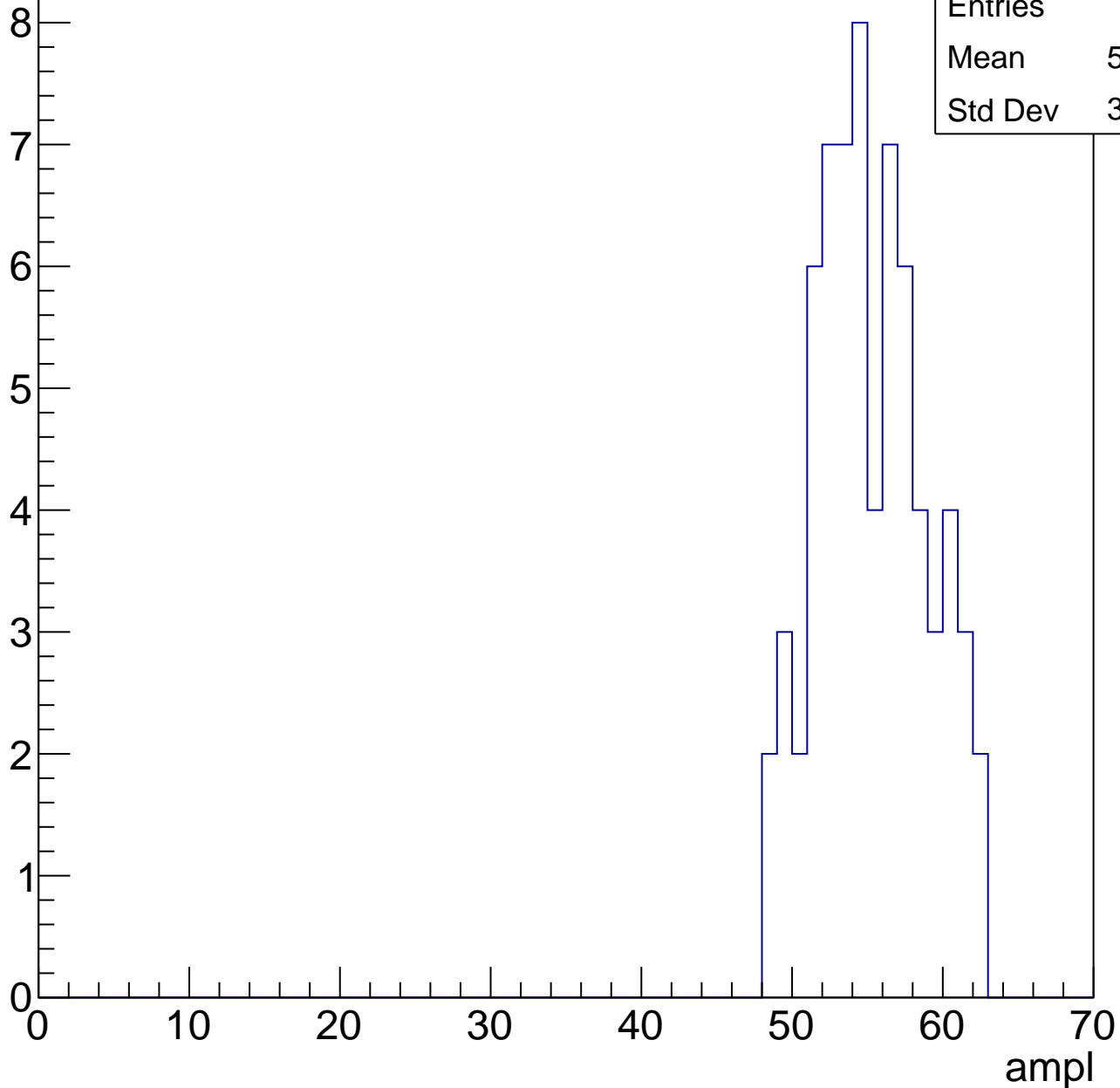


# B1L101S, U3-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	54.79
Std Dev	3.575

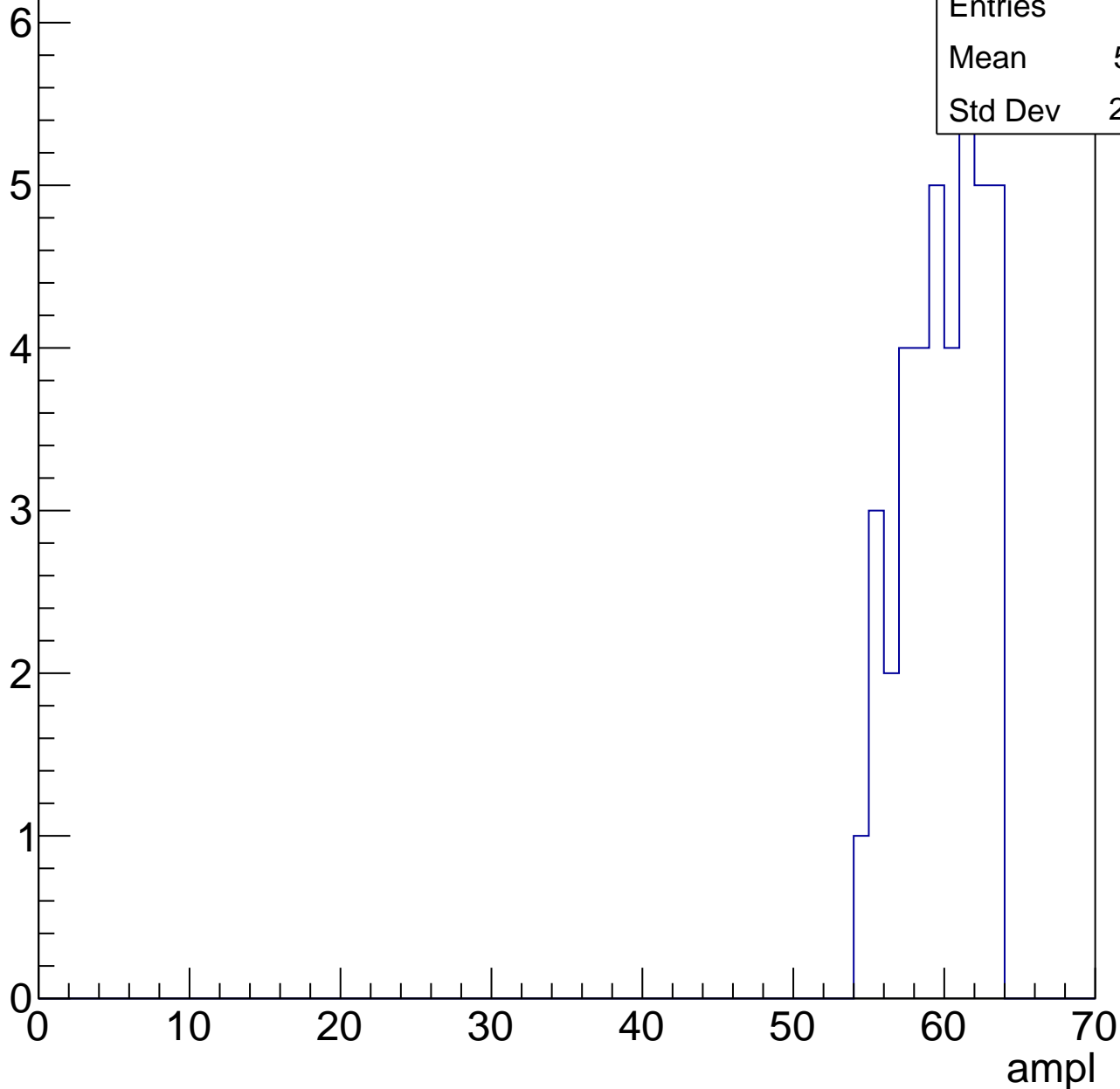


# B1L101S, U3-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	39
Mean	59.41
Std Dev	2.569

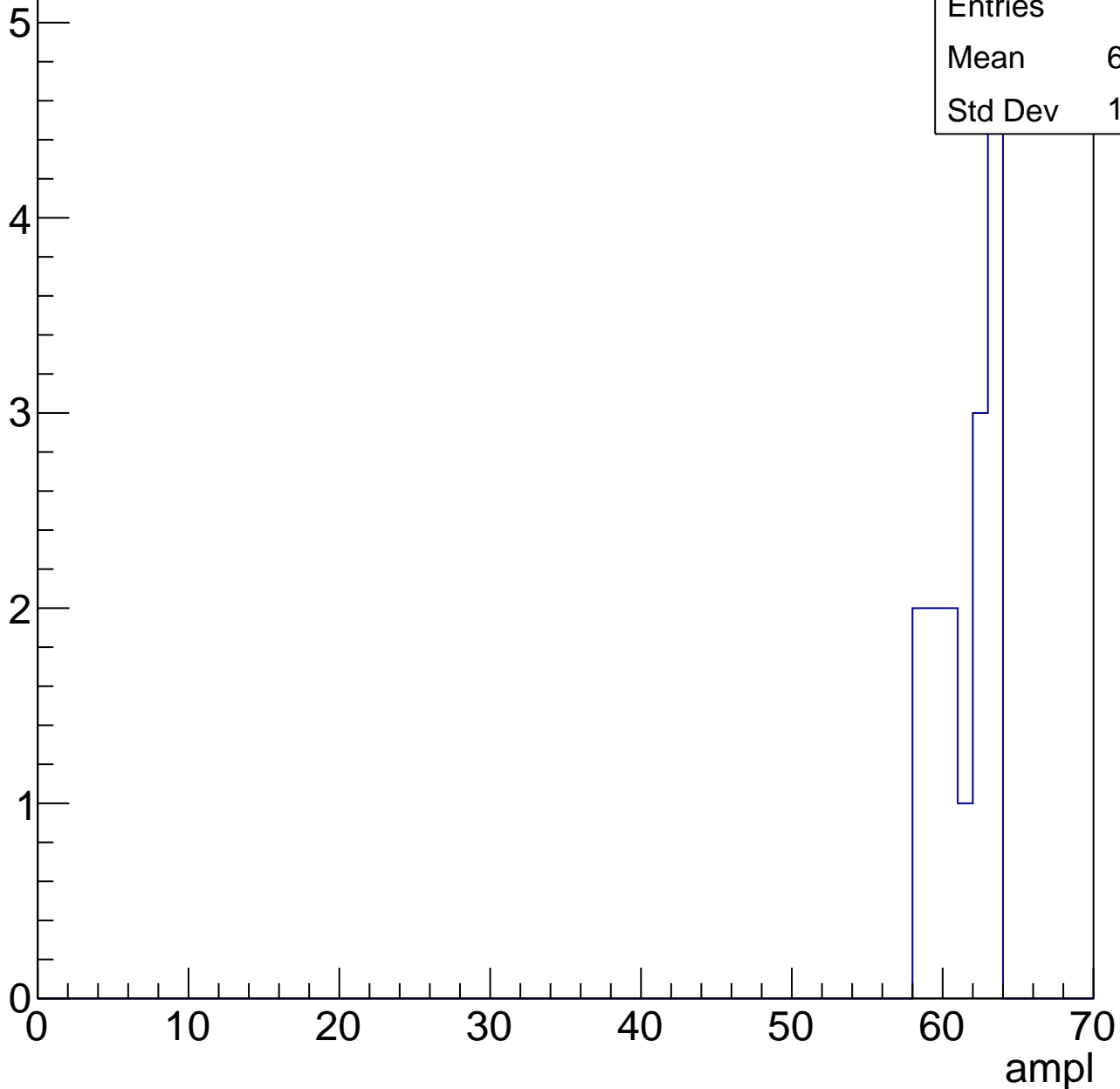


# B1L101S, U3-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	15
Mean	61.07
Std Dev	1.843





# B1L101S, U3-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U3-ch102, adc0

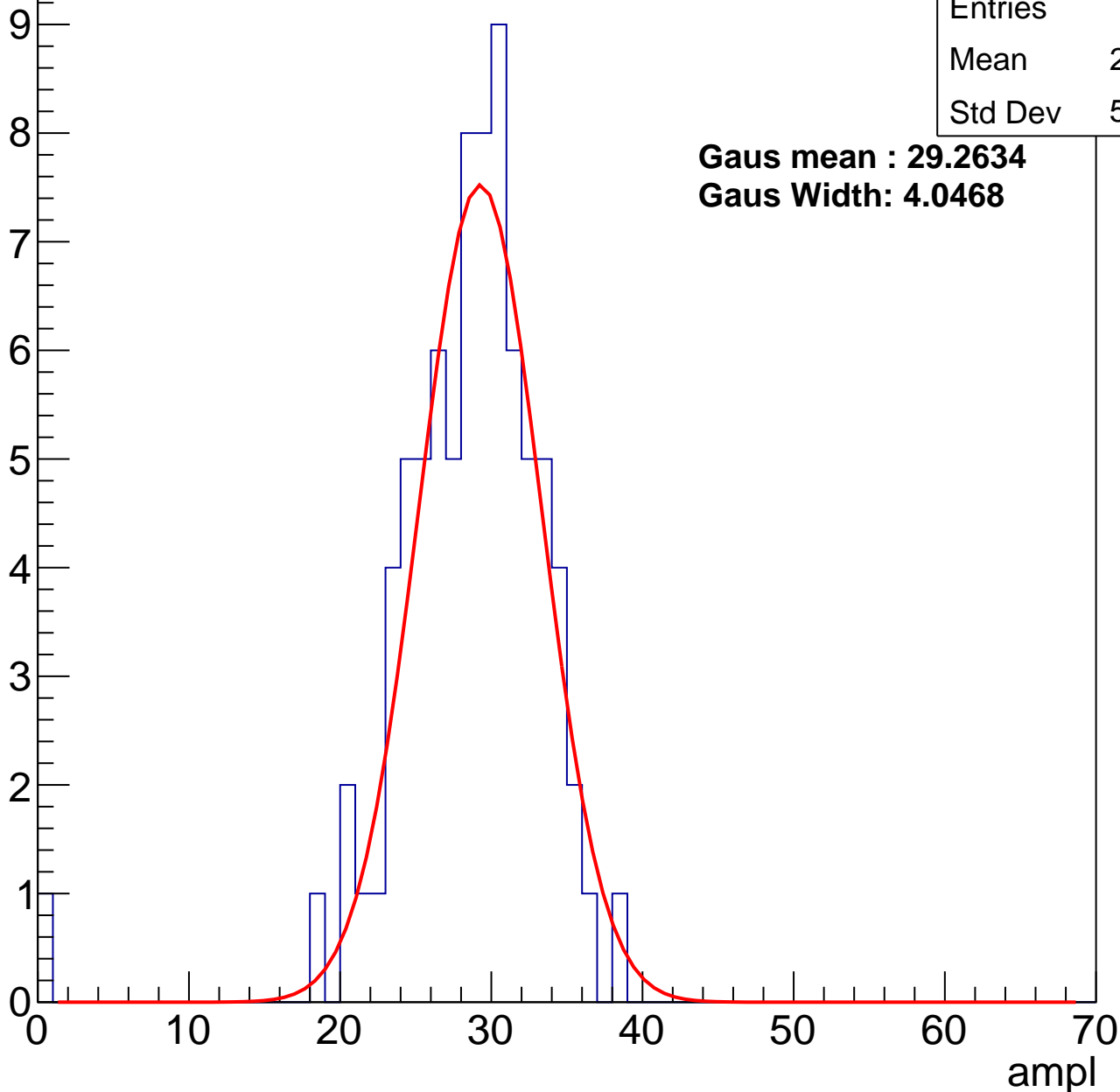
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	28.07
Std Dev	5.074

**Gaus mean : 29.2634**

**Gaus Width: 4.0468**



# B1L101S, U3-ch102, adc1

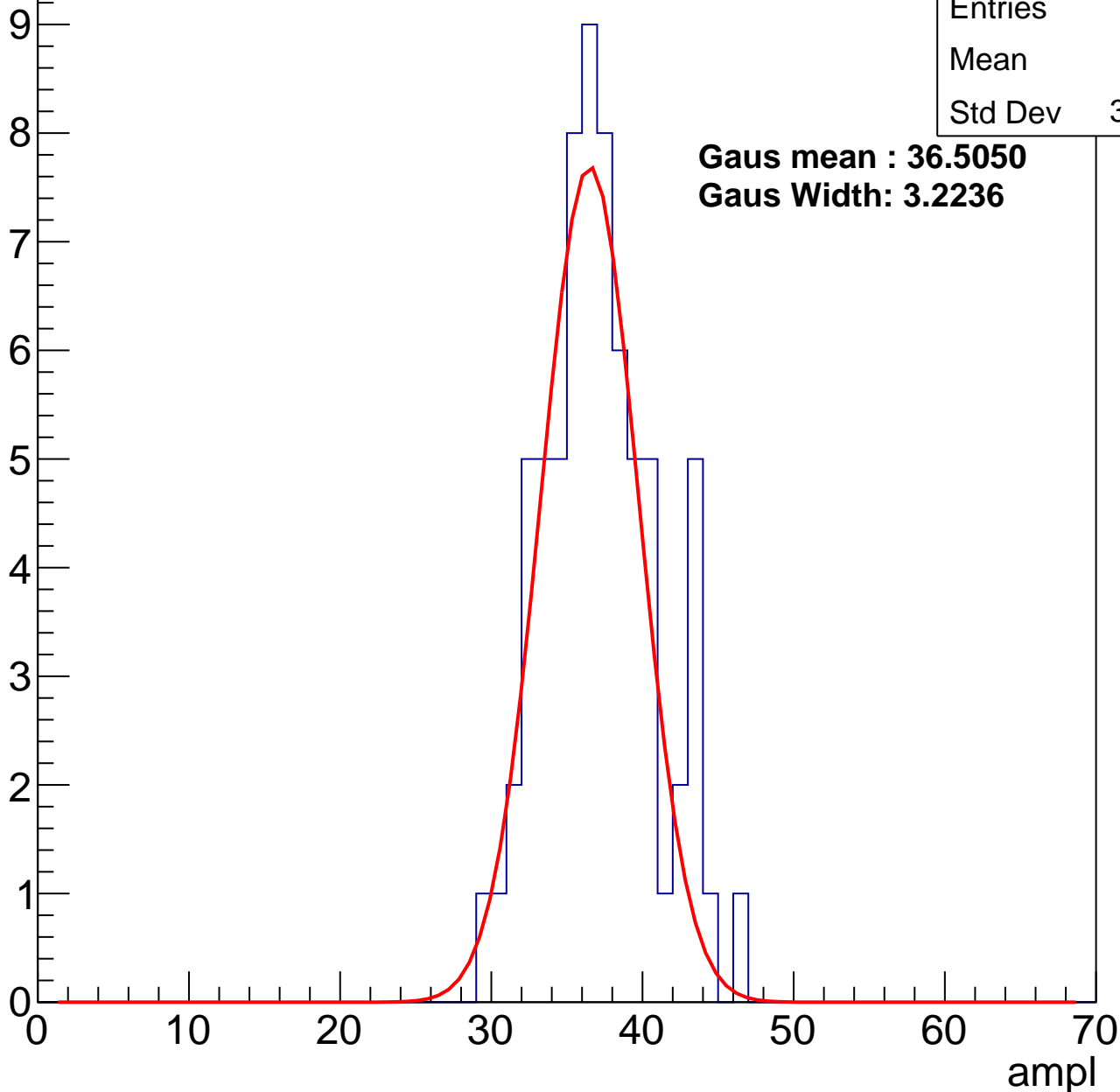
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	36.7
Std Dev	3.619

**Gaus mean : 36.5050**

**Gaus Width: 3.2236**



# B1L101S, U3-ch102, adc2

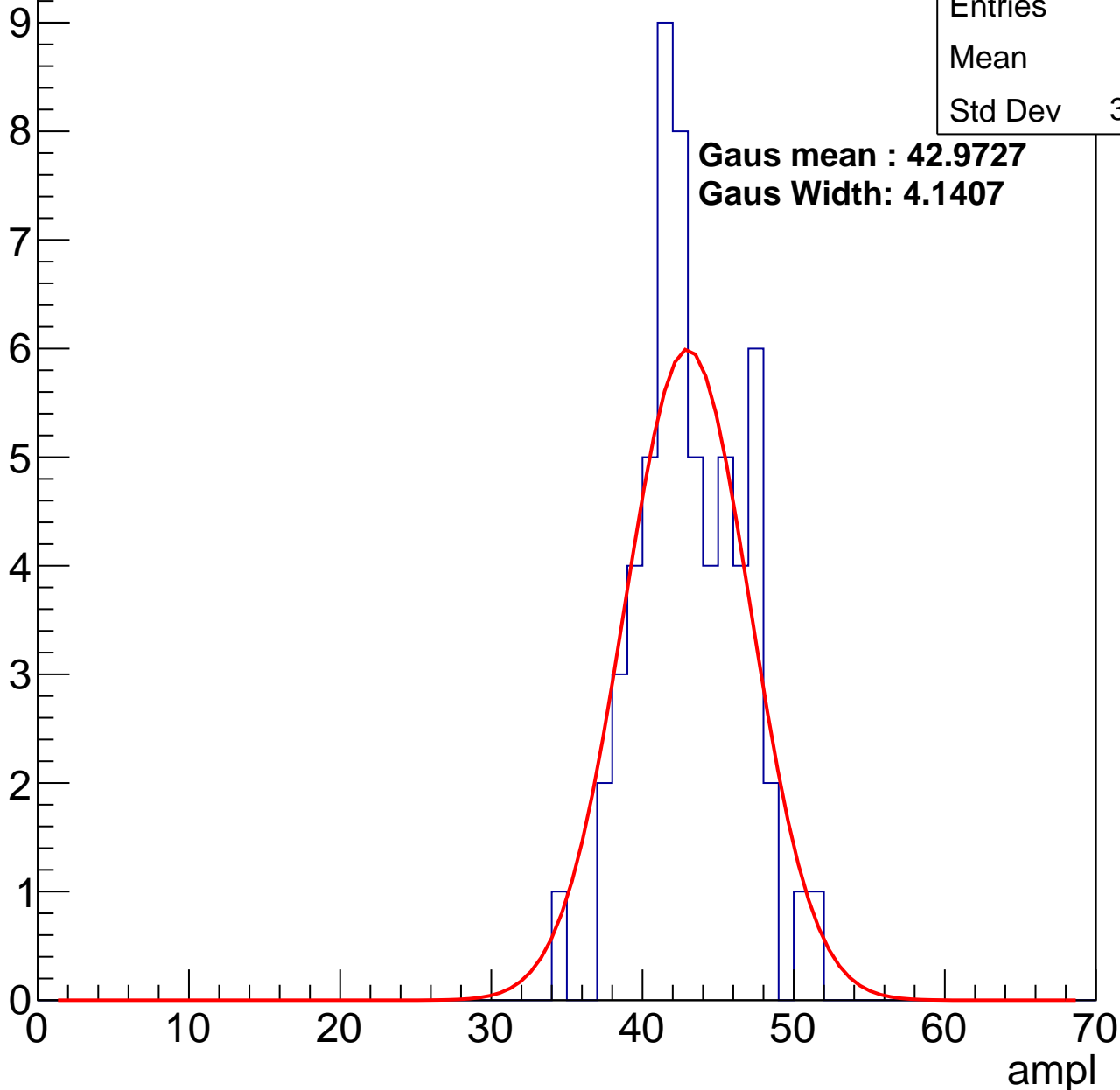
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	42.7
Std Dev	3.402

**Gaus mean : 42.9727**

**Gaus Width: 4.1407**

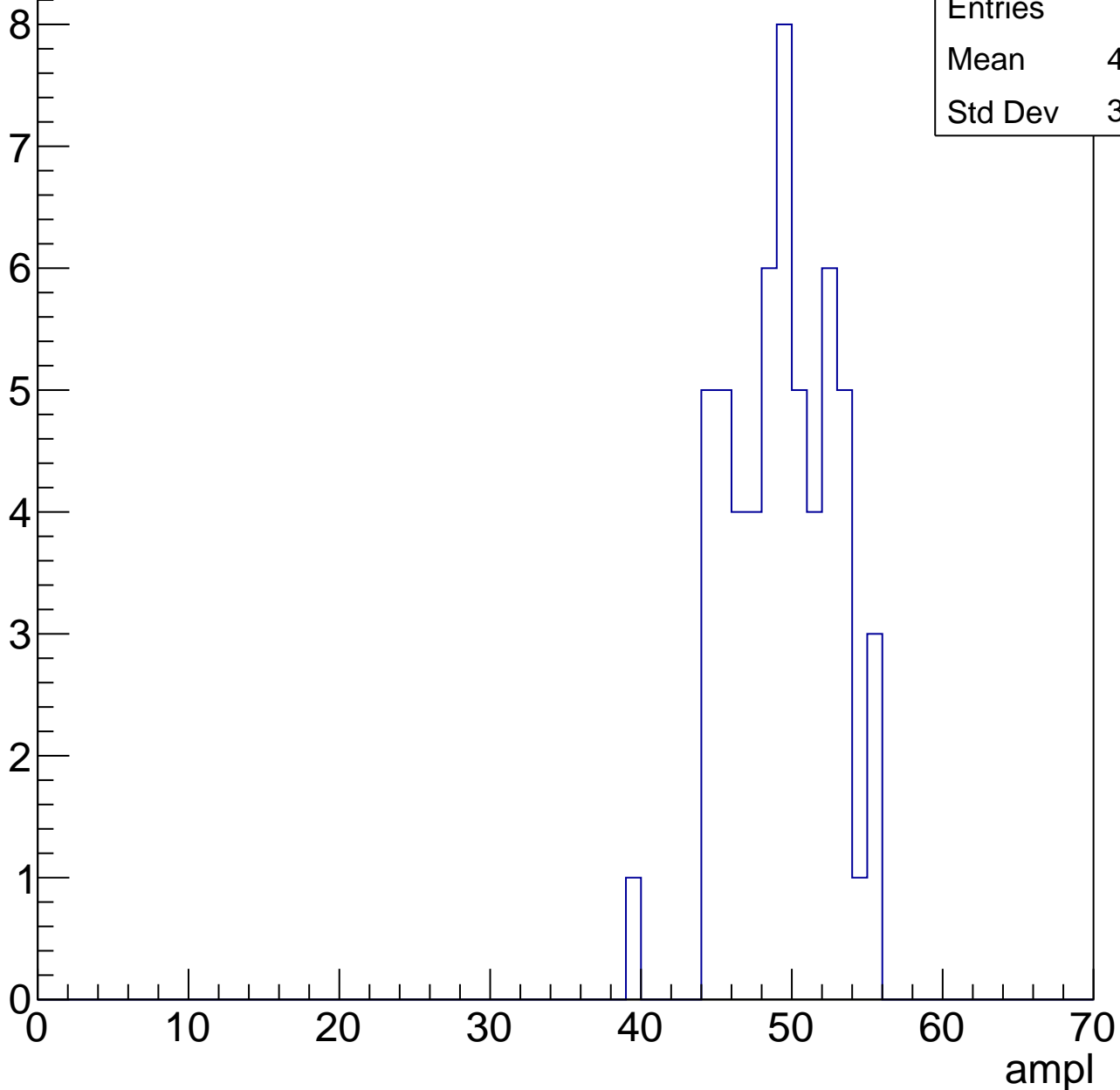


# B1L101S, U3-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	48.88
Std Dev	3.377

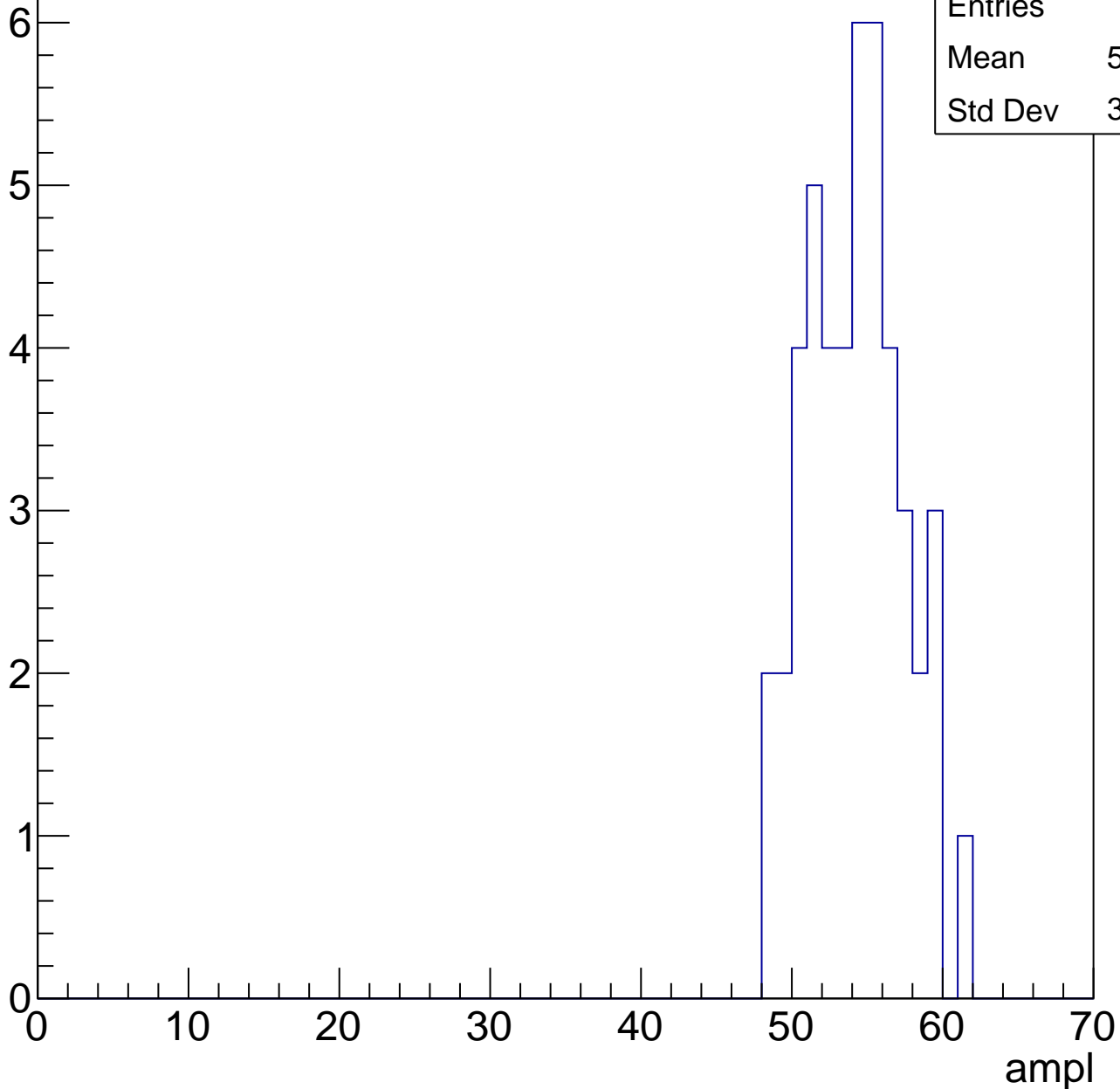


# B1L101S, U3-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	46
Mean	53.74
Std Dev	3.138

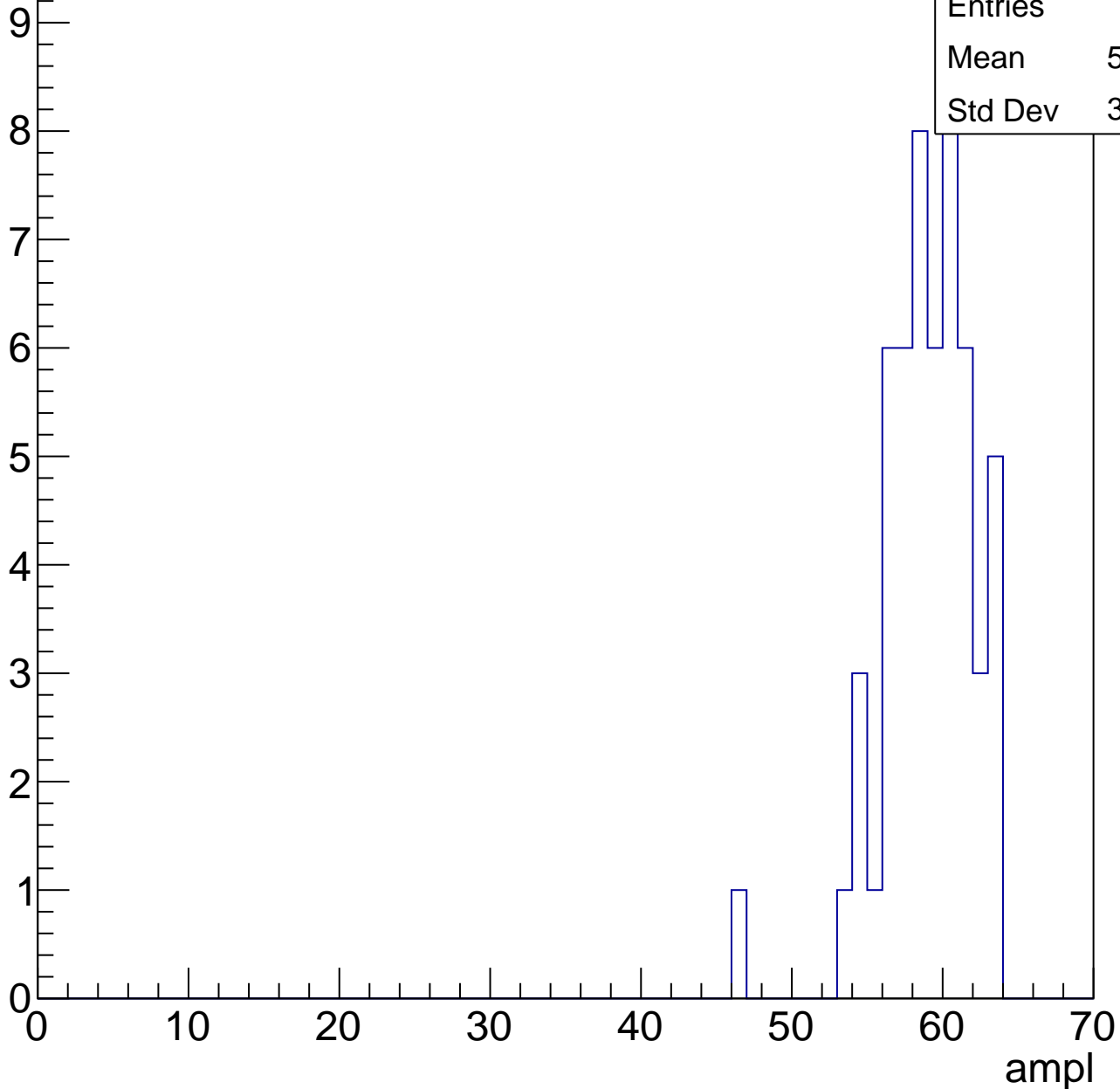


# B1L101S, U3-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	58.53
Std Dev	3.044

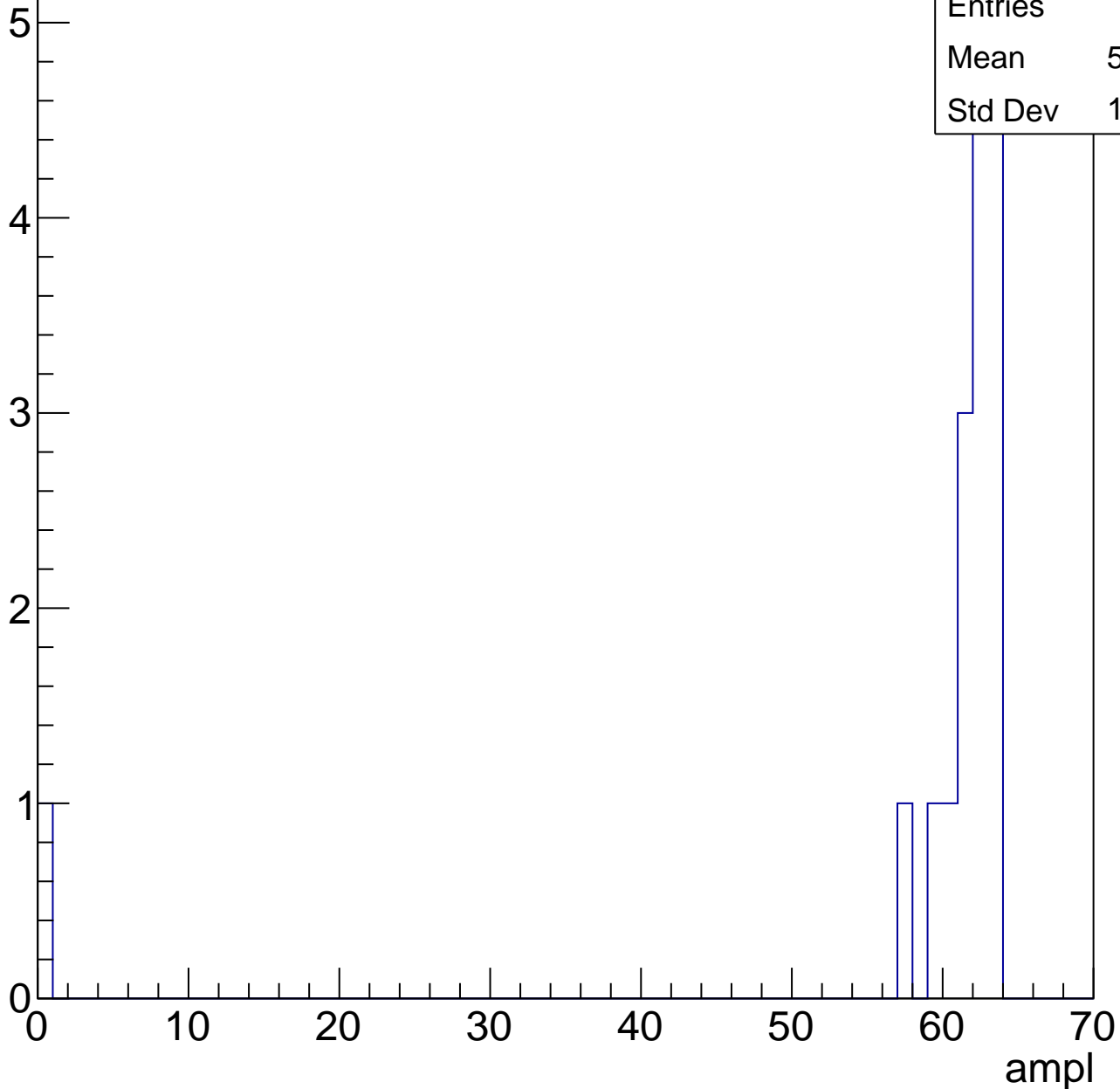


# B1L101S, U3-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	17
Mean	57.88
Std Dev	14.56

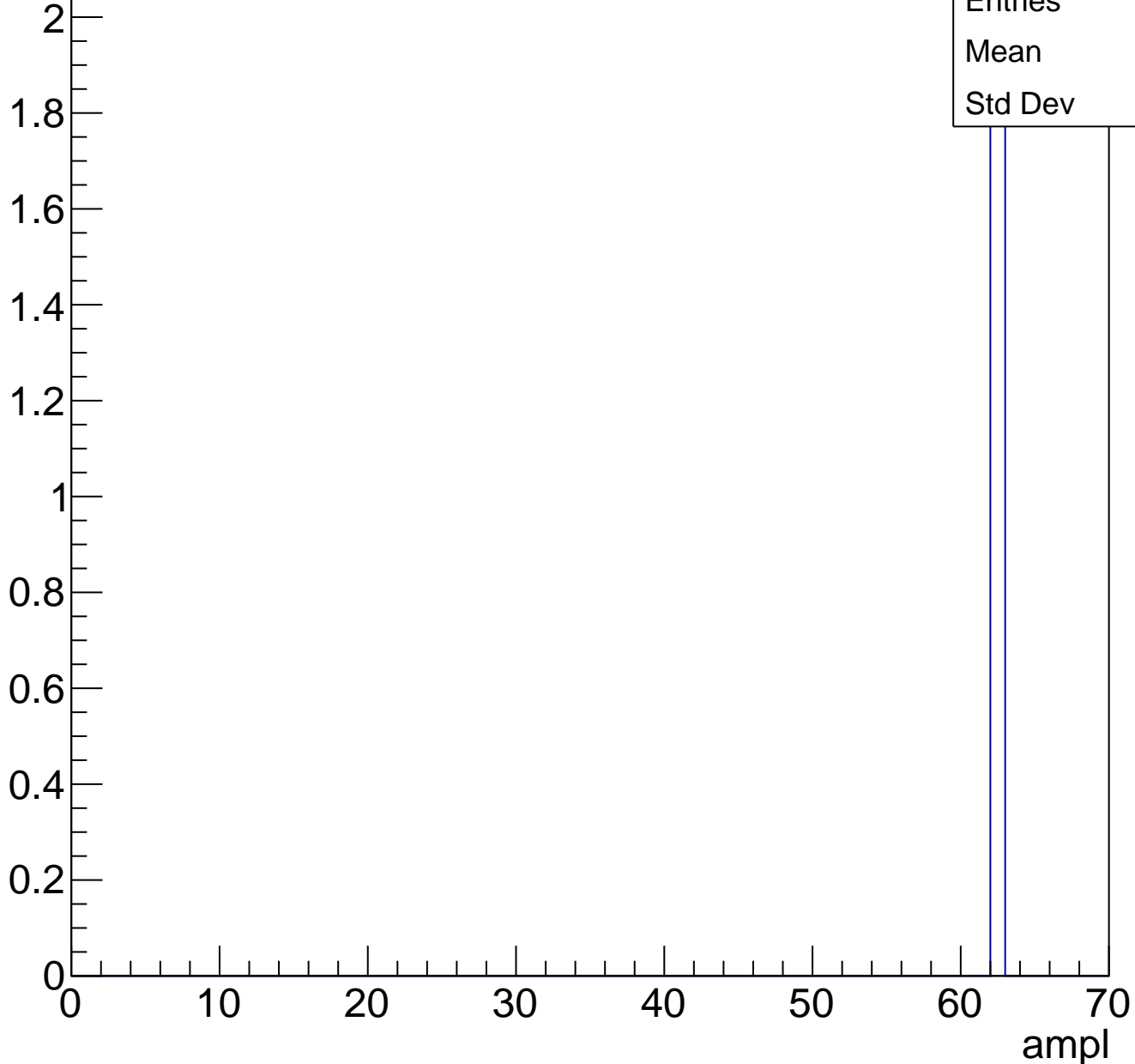




# B1L101S, U3-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch103, adc0

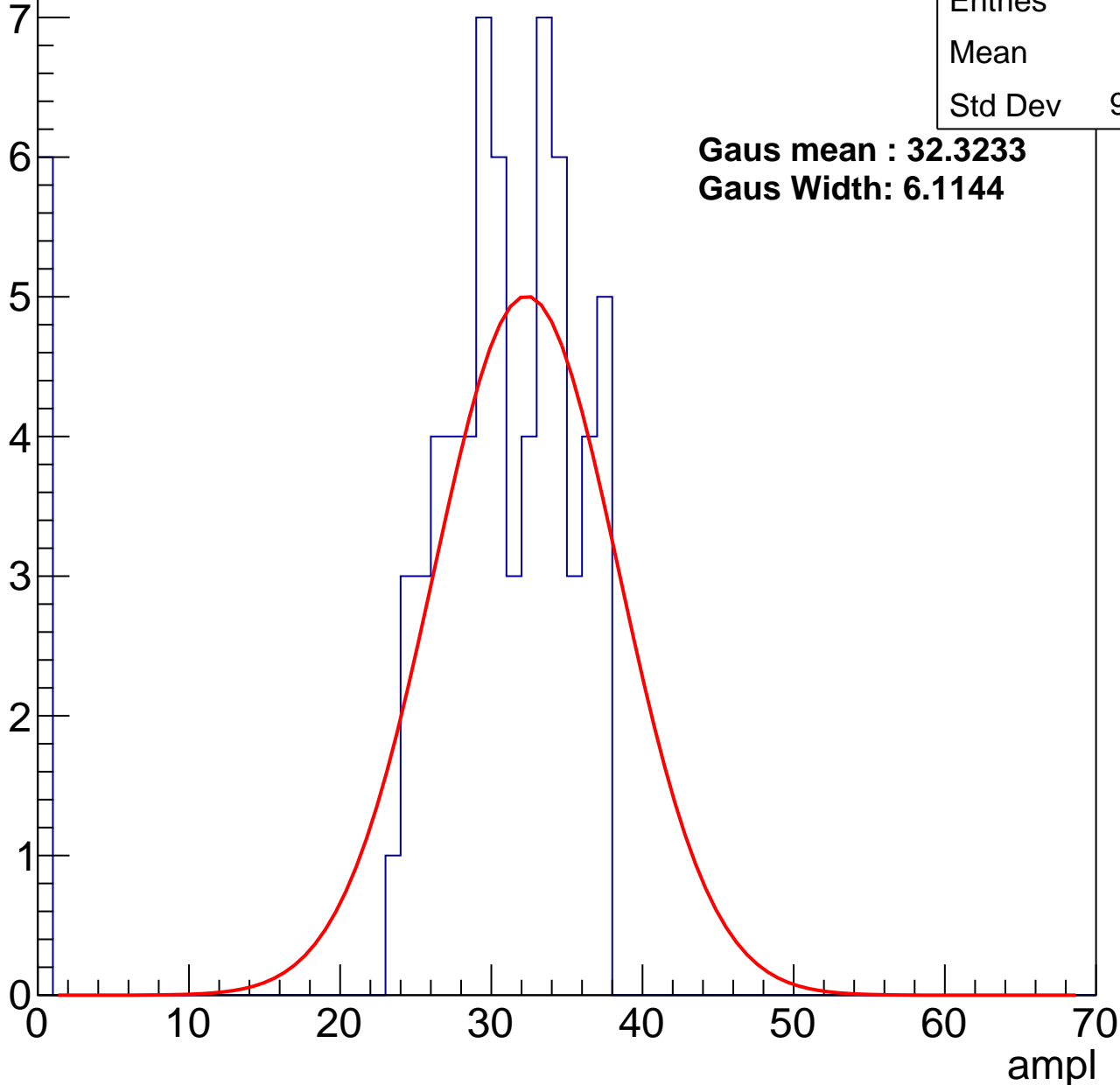
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	28.1
Std Dev	9.369

**Gaus mean : 32.3233**

**Gaus Width: 6.1144**



# B1L101S, U3-ch103, adc1

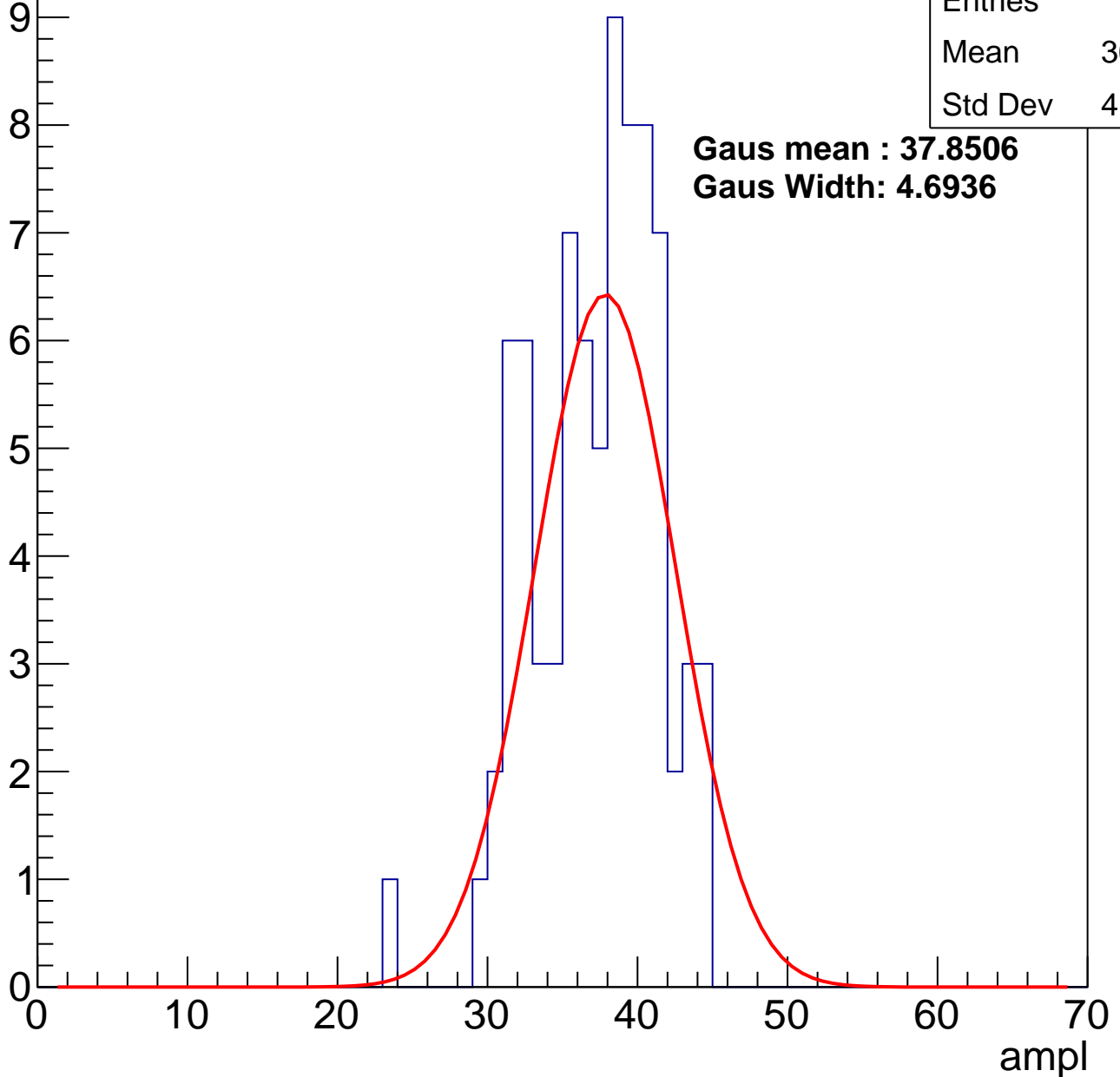
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	36.79
Std Dev	4.122

**Gaus mean : 37.8506**

**Gaus Width: 4.6936**



# B1L101S, U3-ch103, adc2

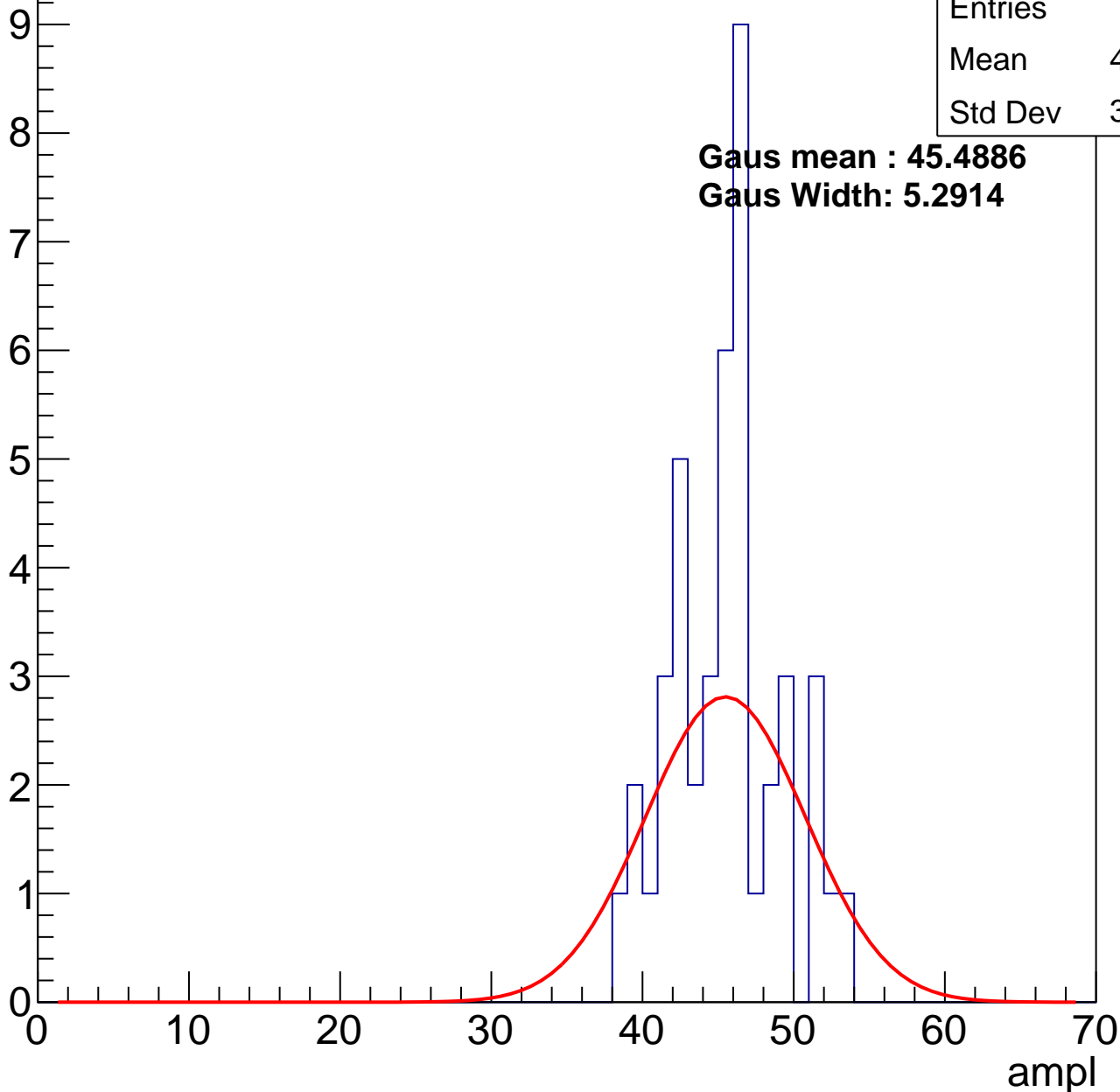
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	45.09
Std Dev	3.575

**Gaus mean : 45.4886**

**Gaus Width: 5.2914**



# B1L101S, U3-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

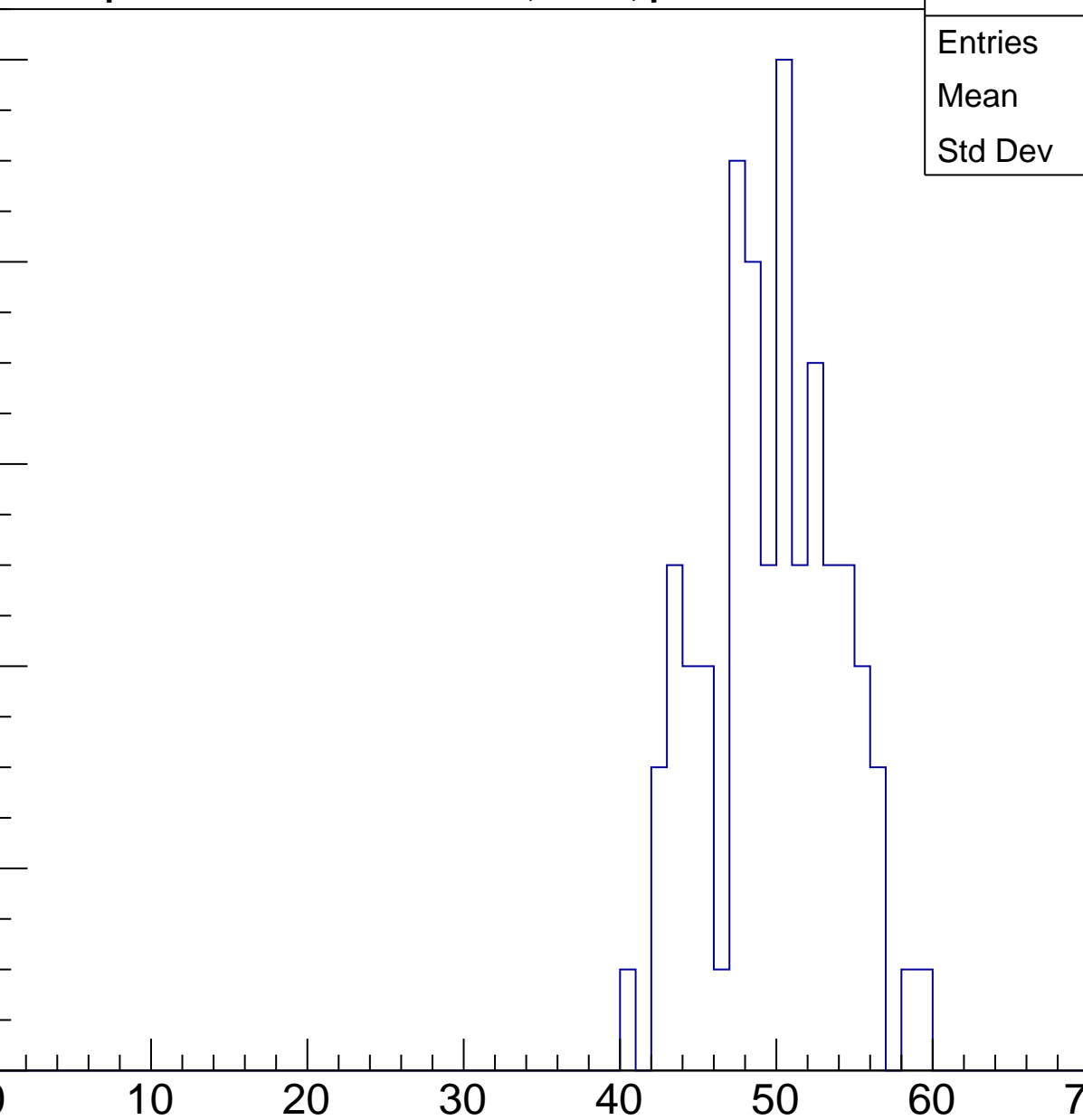
Entries	81
Mean	49.31
Std Dev	4.138

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

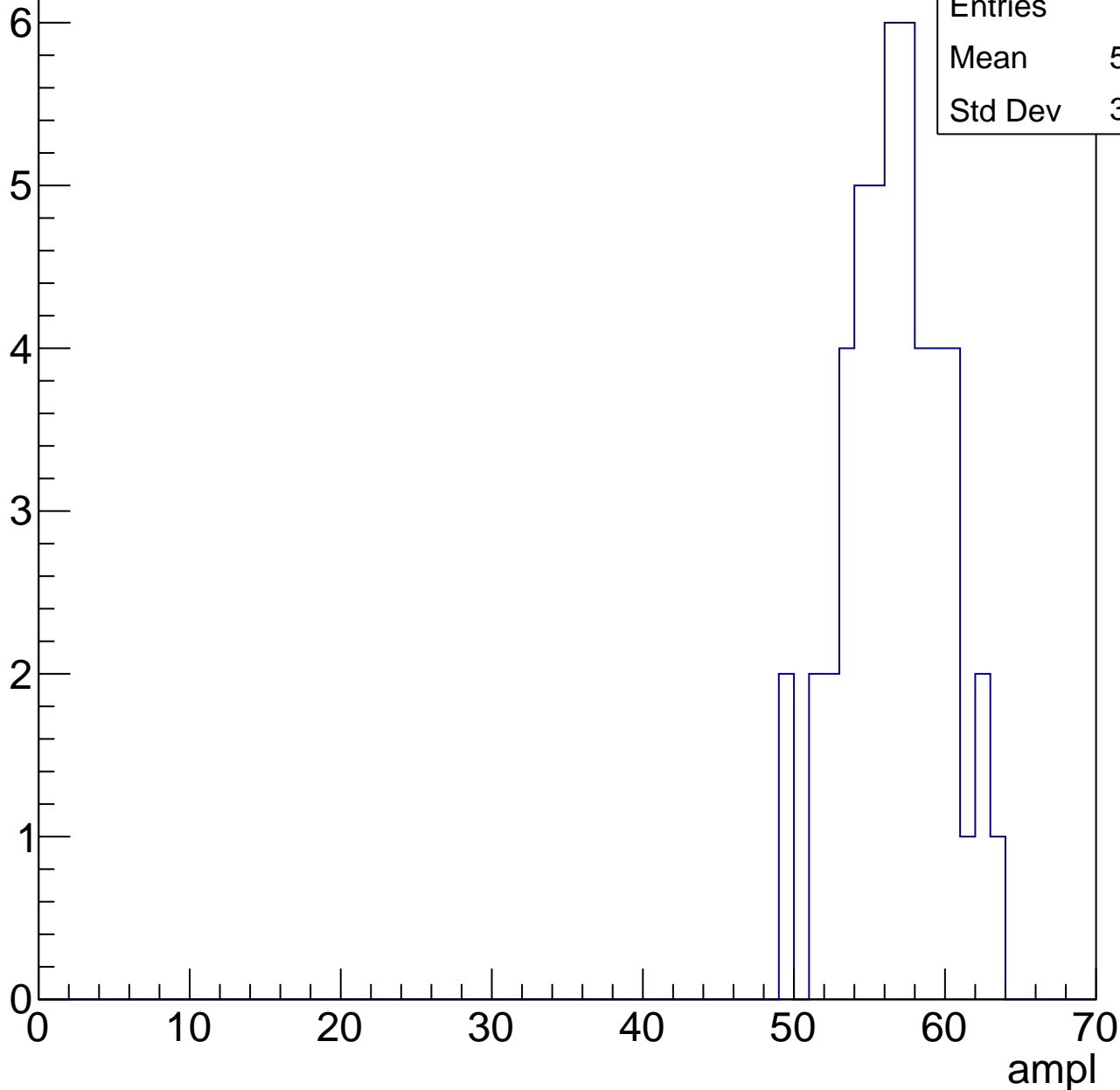


# B1L101S, U3-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

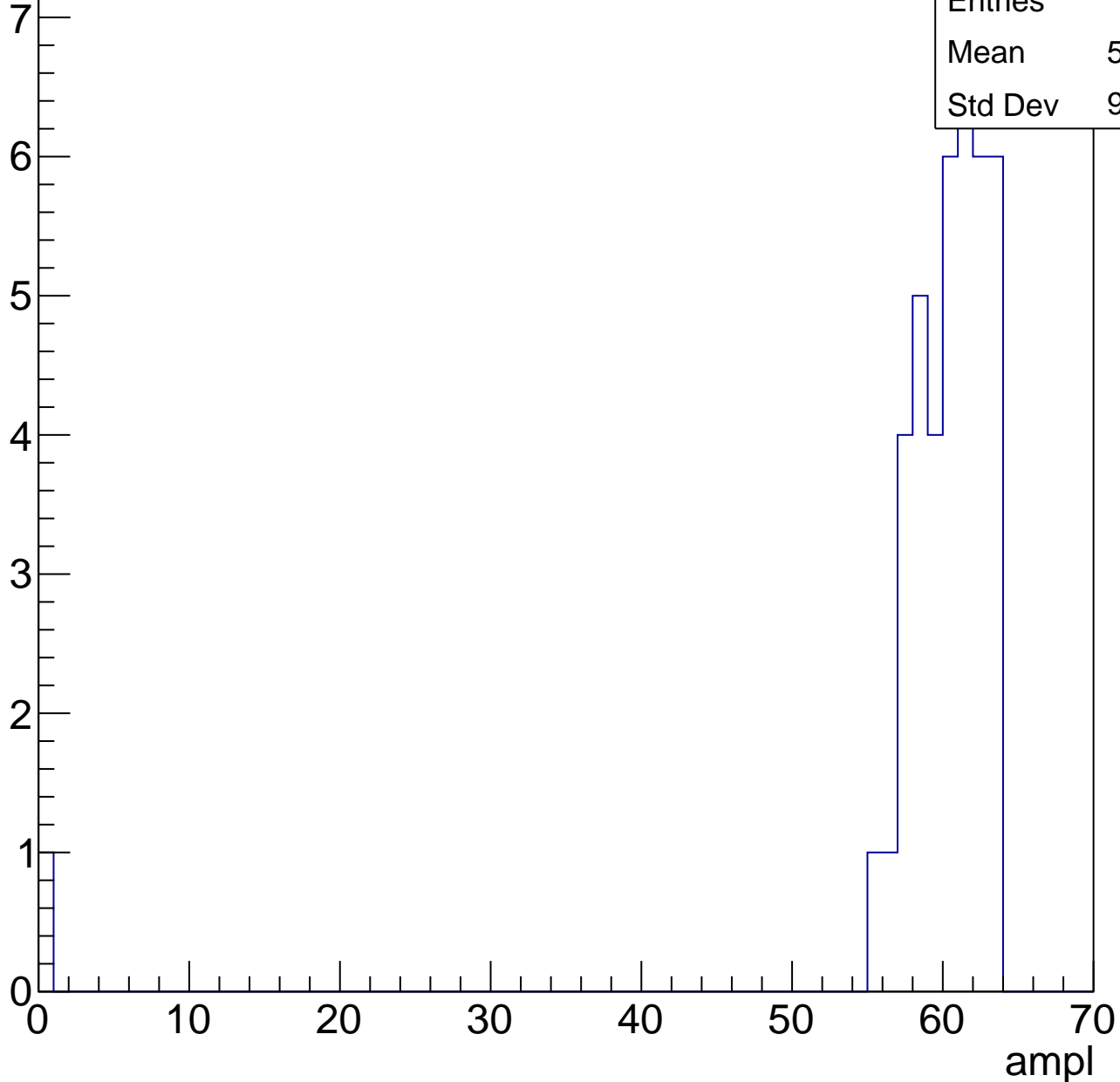
Entries	48
Mean	56.15
Std Dev	3.253



# B1L101S, U3-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

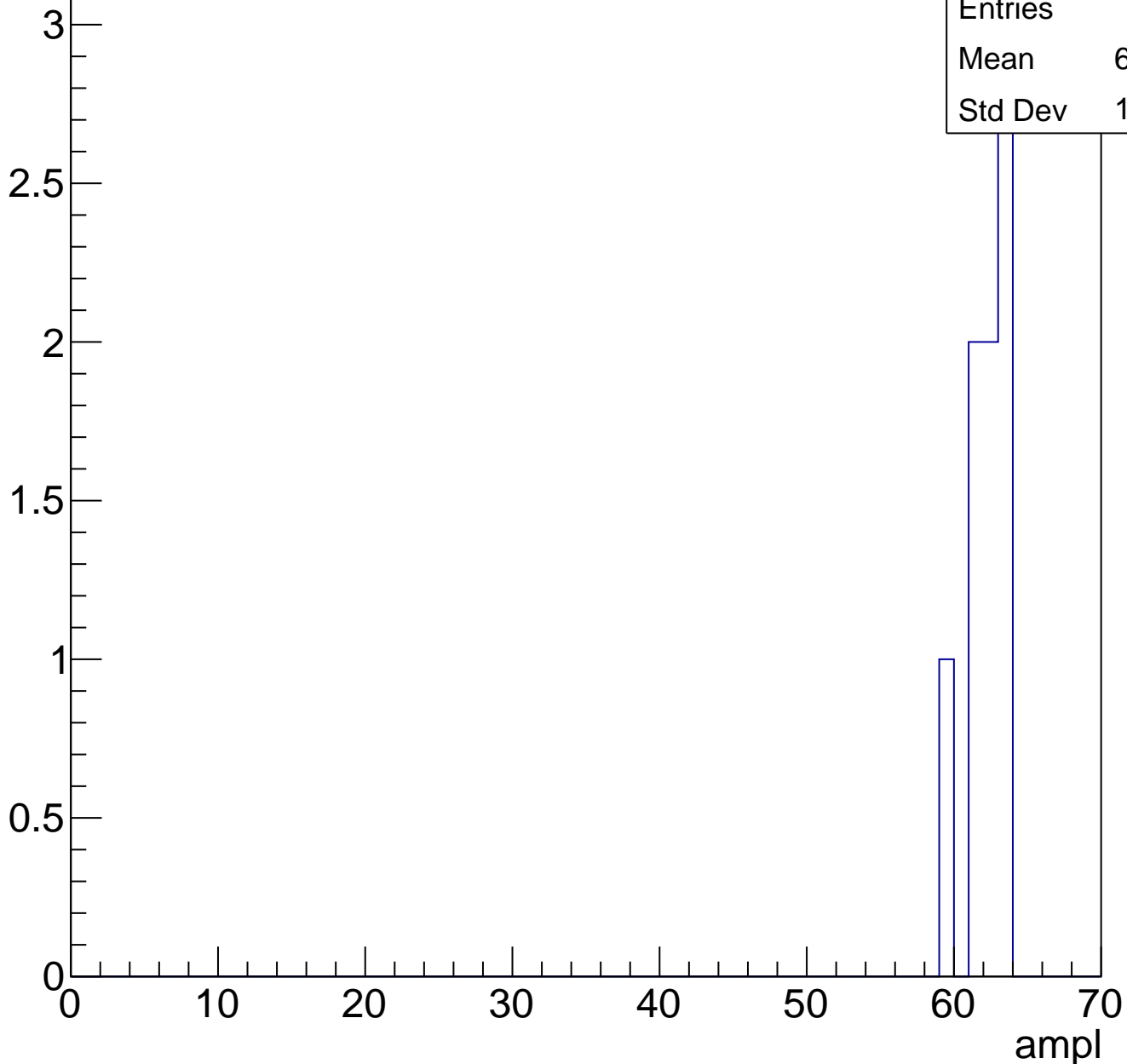
Entry



# B1L101S, U3-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U3-ch104, adc0

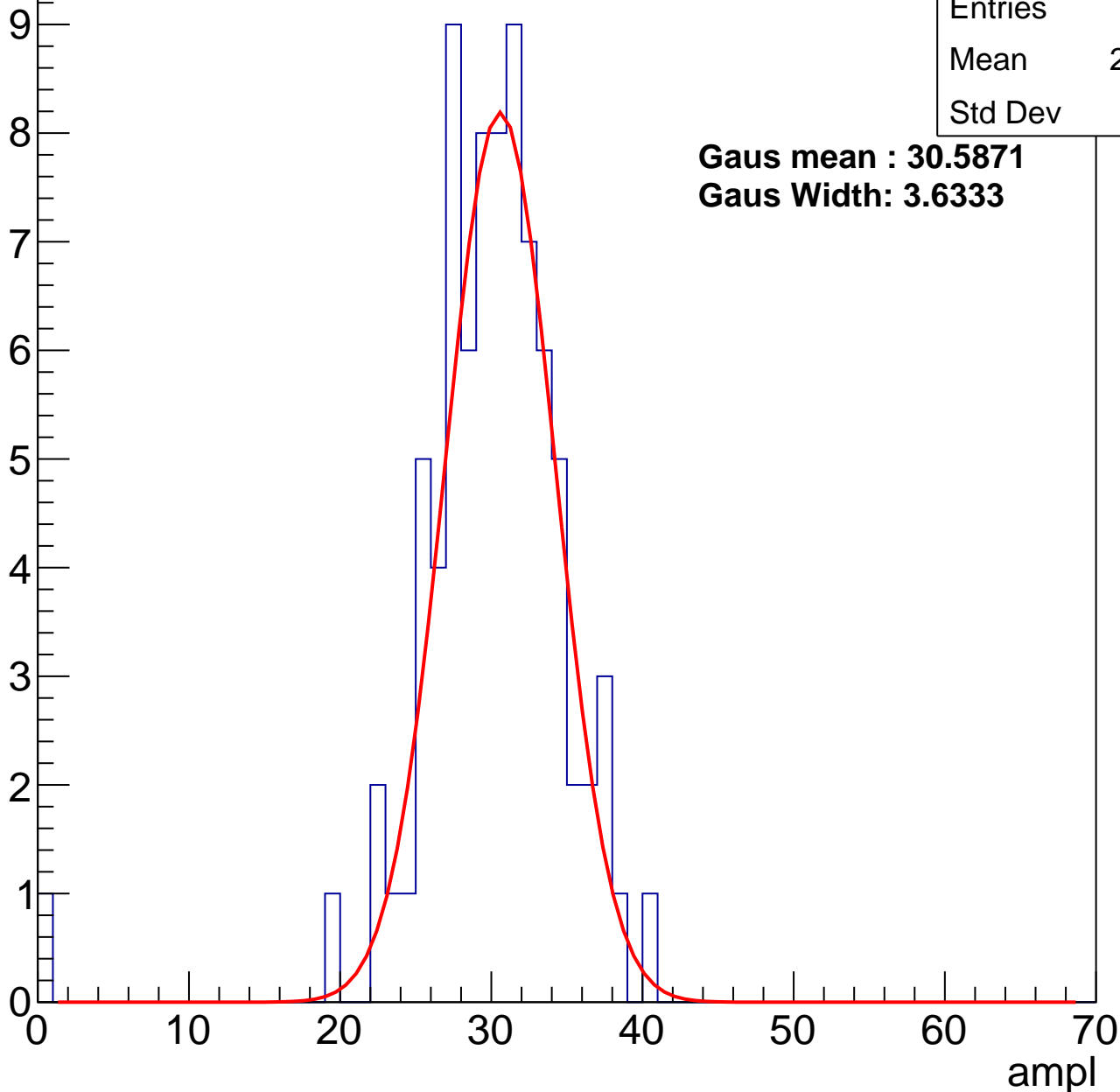
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	29.56
Std Dev	5.09

**Gaus mean : 30.5871**

**Gaus Width: 3.6333**



# B1L101S, U3-ch104, adc1

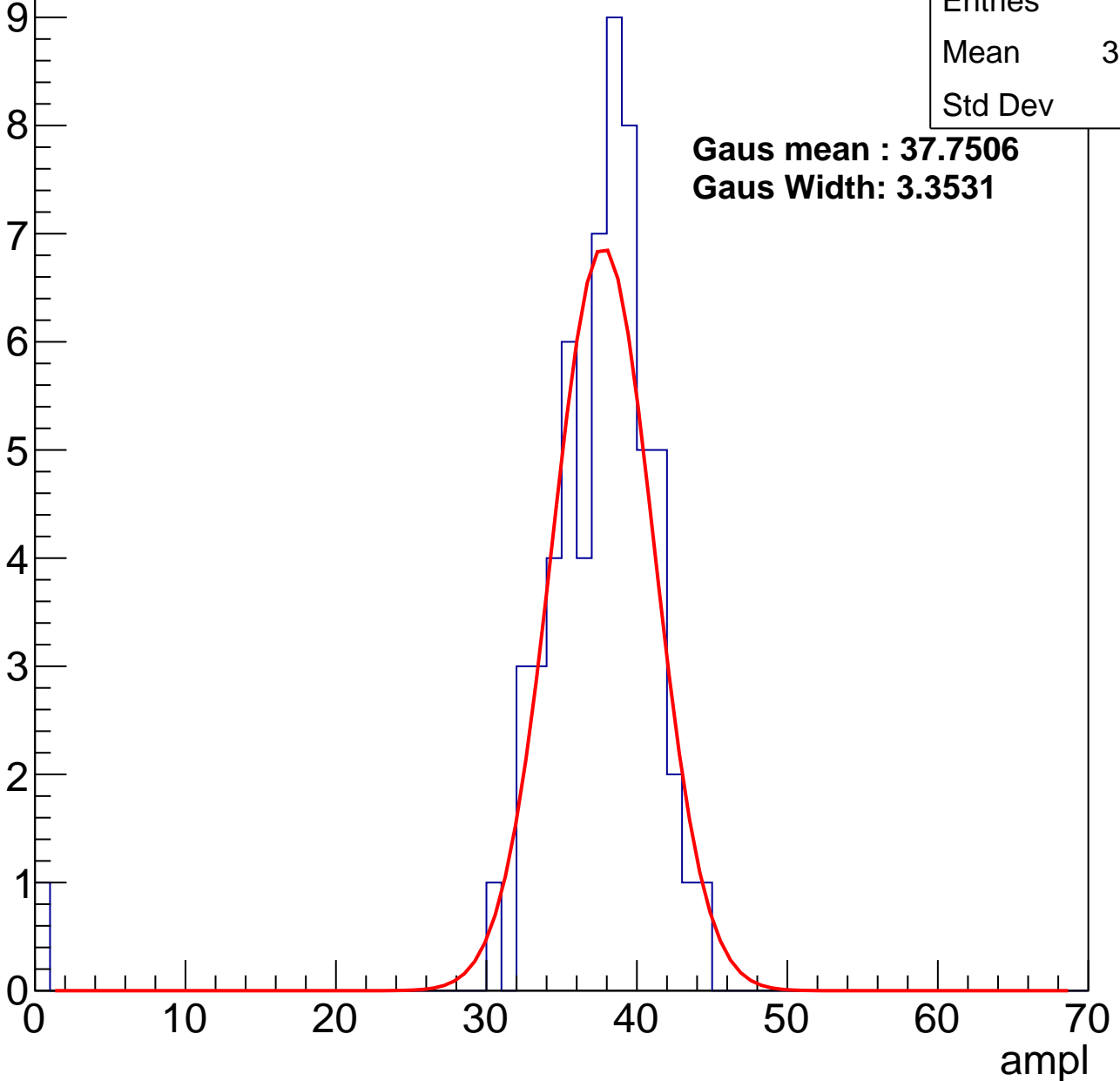
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	36.73
Std Dev	5.63

**Gaus mean : 37.7506**

**Gaus Width: 3.3531**



# B1L101S, U3-ch104, adc2

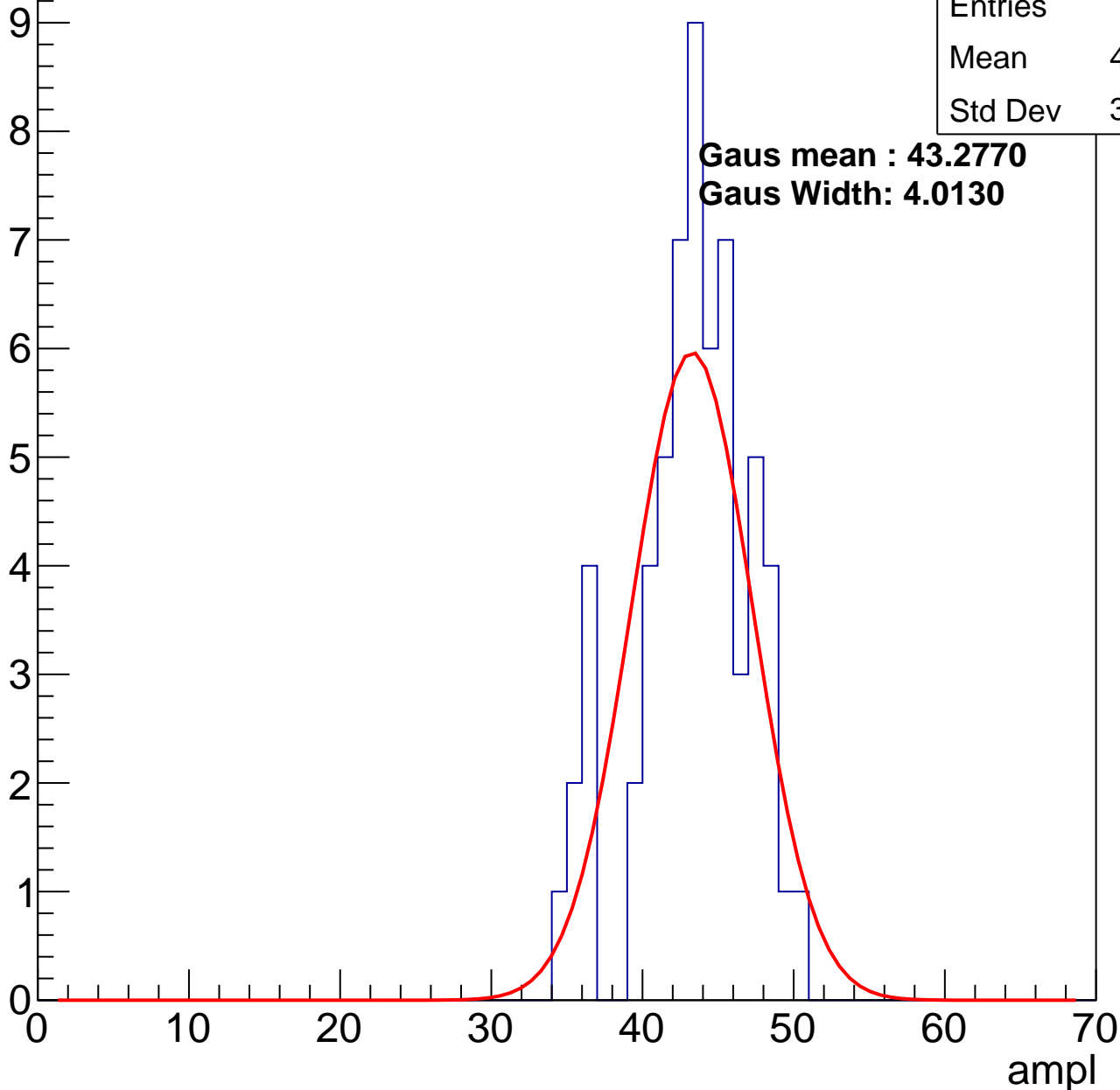
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	42.87
Std Dev	3.677

**Gaus mean : 43.2770**

**Gaus Width: 4.0130**

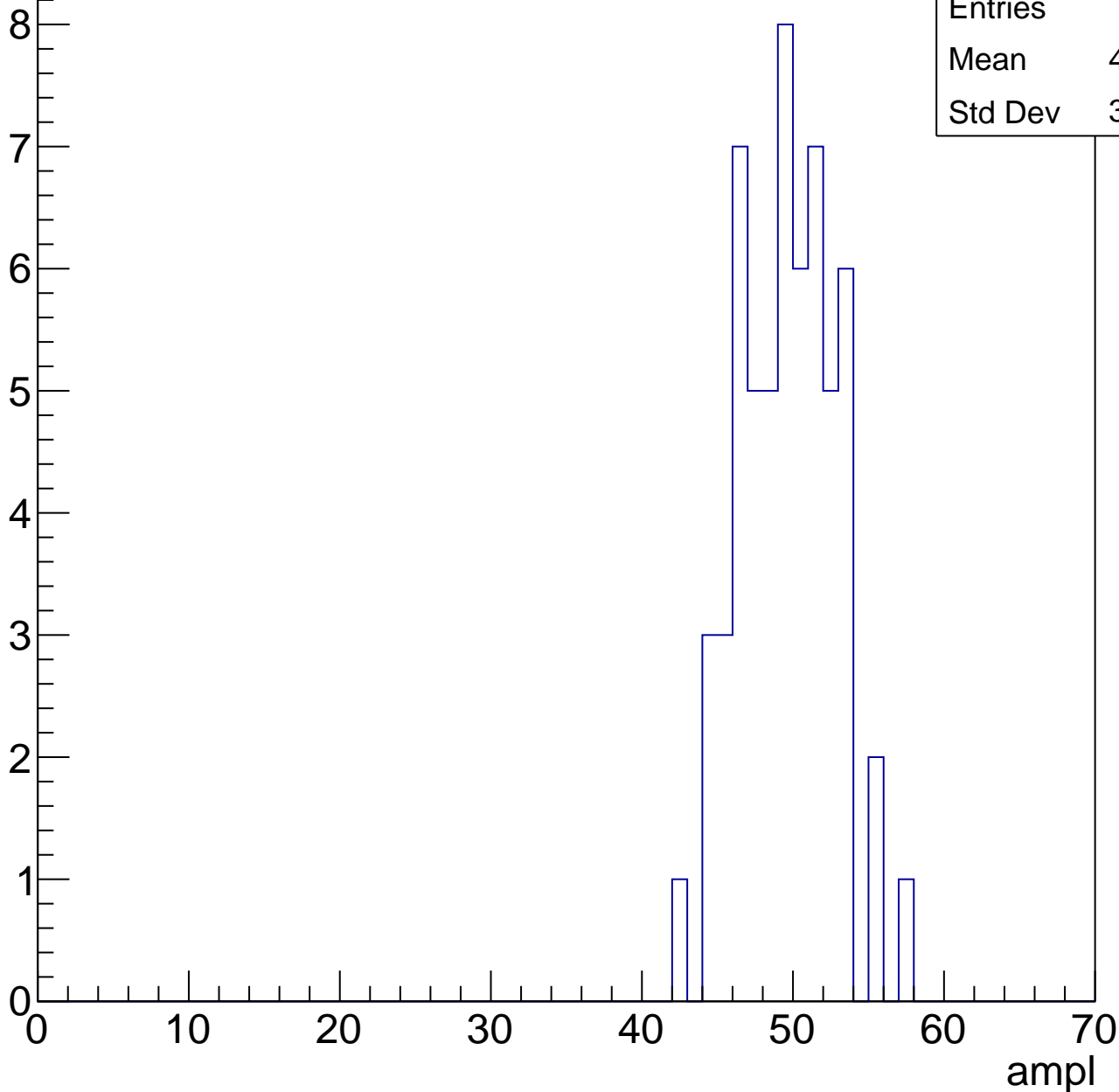


# B1L101S, U3-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

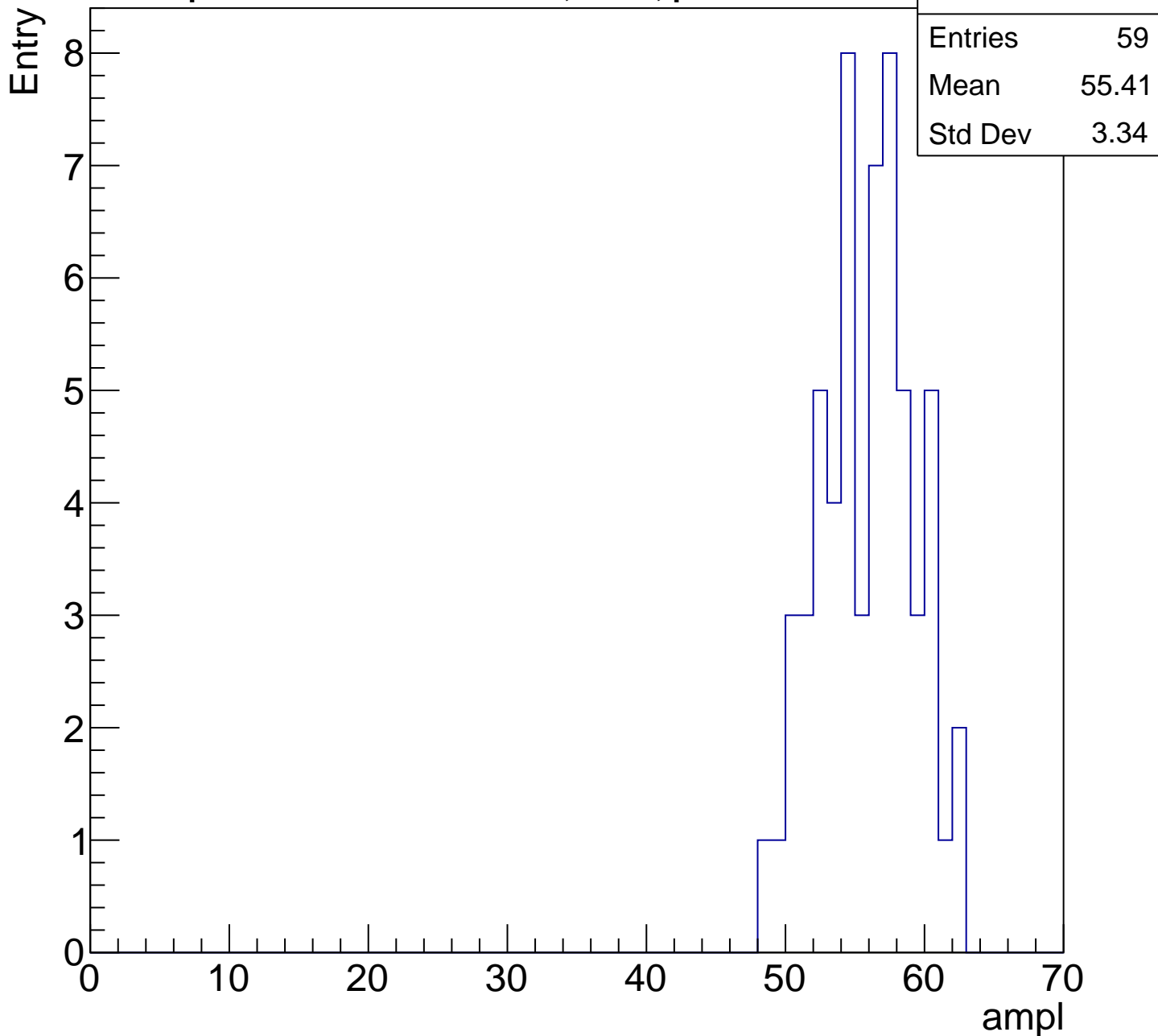
Entry

Entries	59
Mean	49.15
Std Dev	3.107



# B1L101S, U3-ch104, adc4

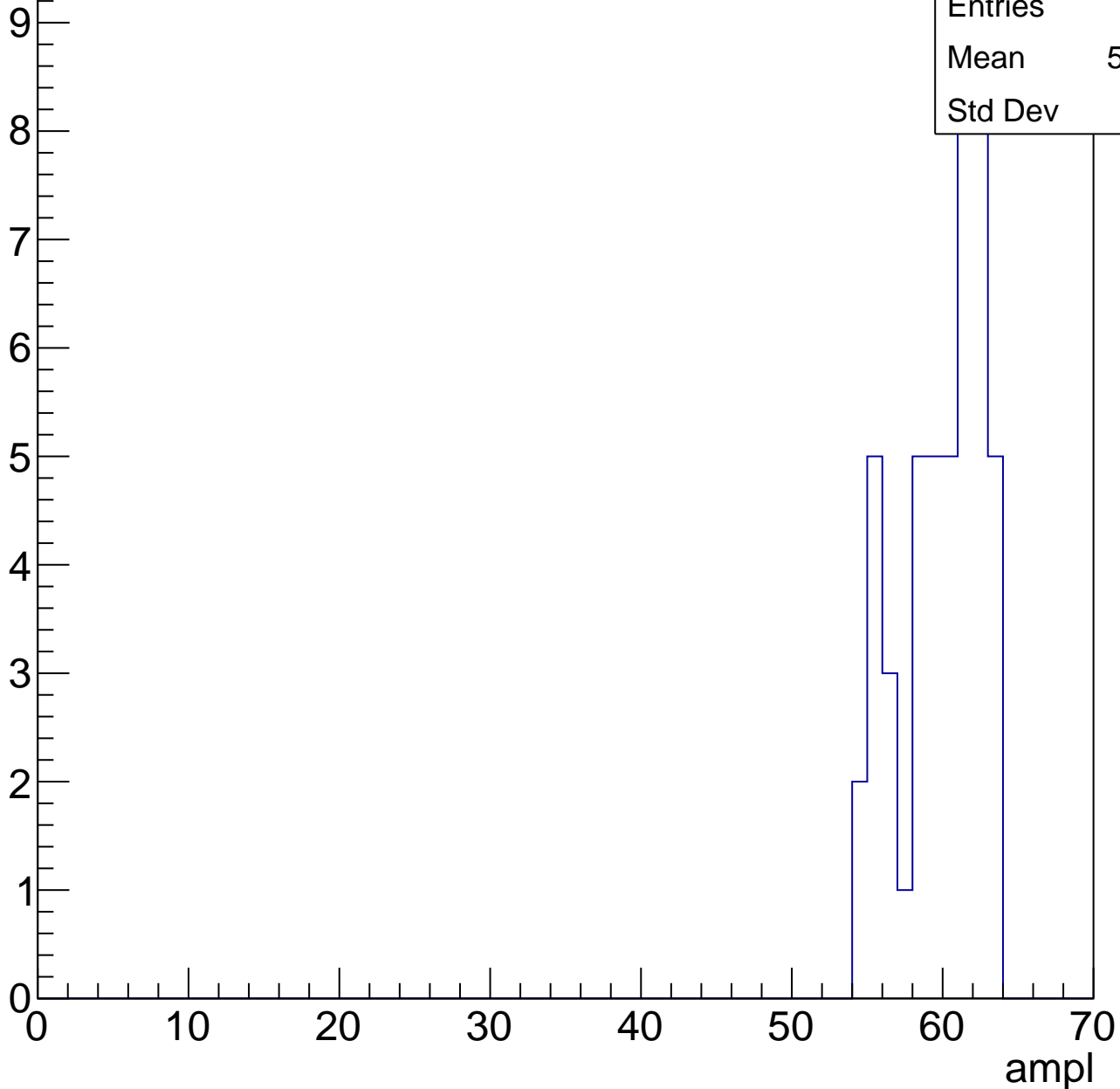
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

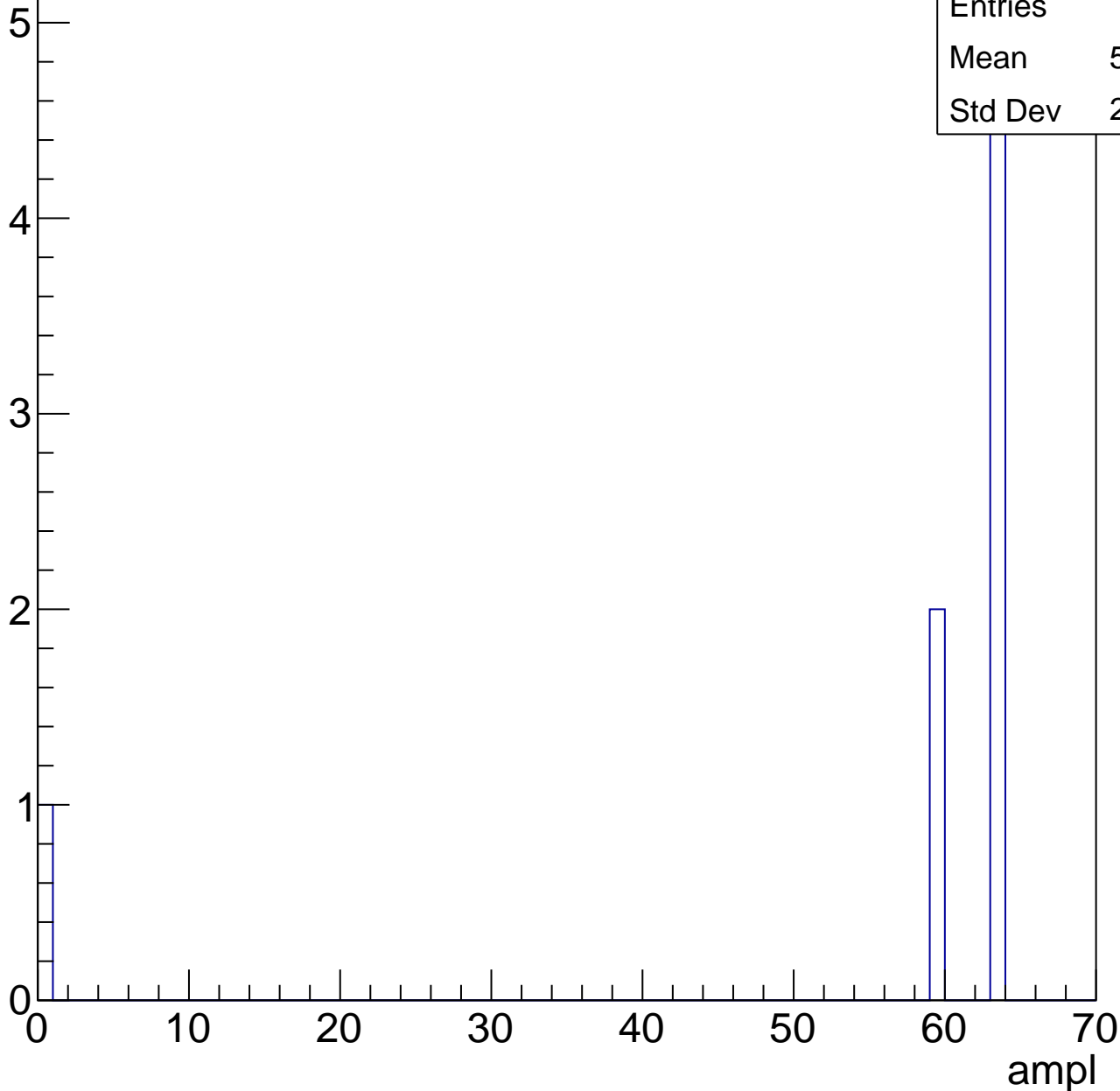


# B1L101S, U3-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	8
Mean	54.12
Std Dev	20.53





# B1L101S, U3-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L101S, U3-ch105, adc0

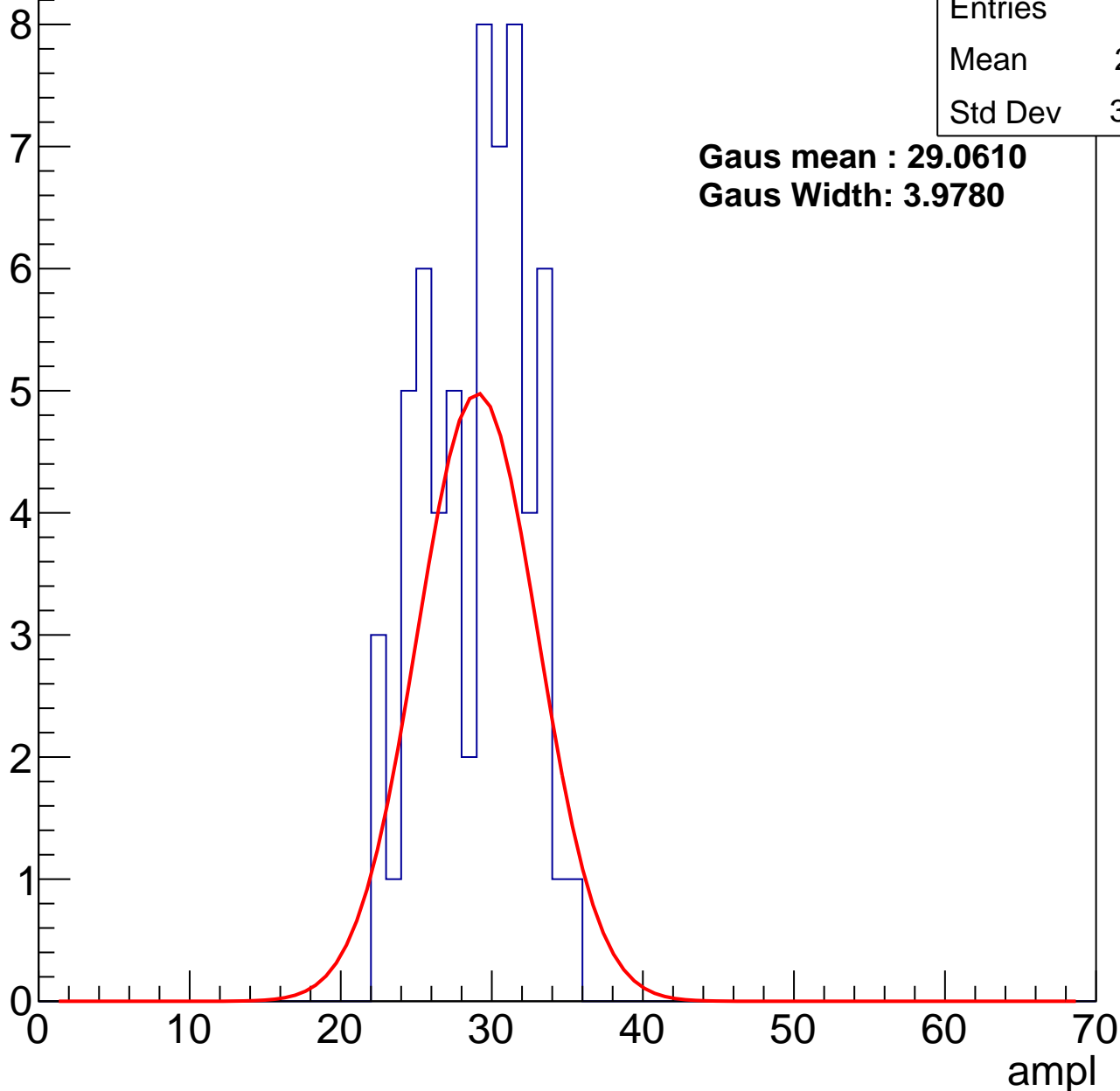
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	28.51
Std Dev	3.337

**Gaus mean : 29.0610**

**Gaus Width: 3.9780**



# B1L101S, U3-ch105, adc1

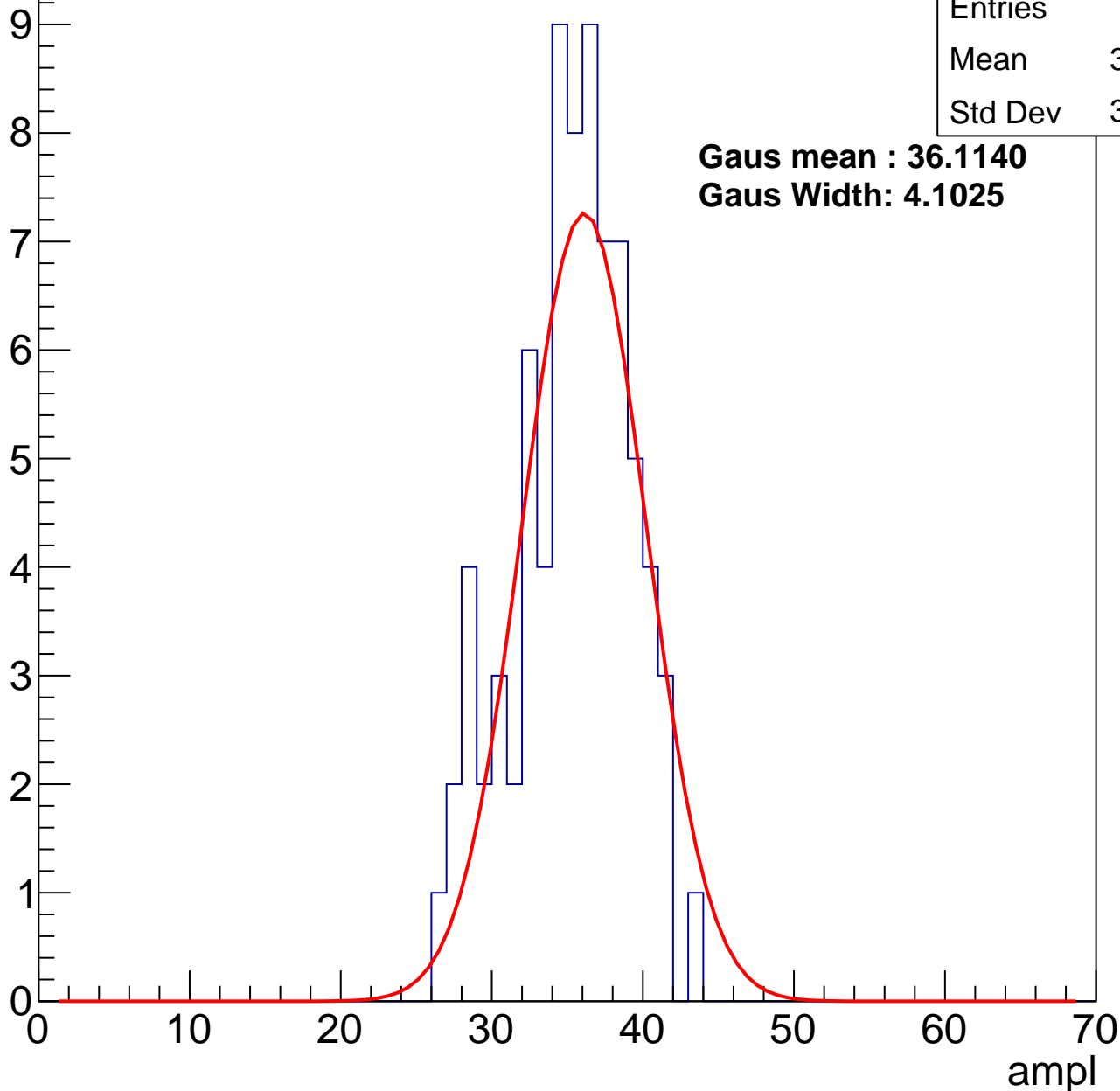
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	34.83
Std Dev	3.802

**Gaus mean : 36.1140**

**Gaus Width: 4.1025**



# B1L101S, U3-ch105, adc2

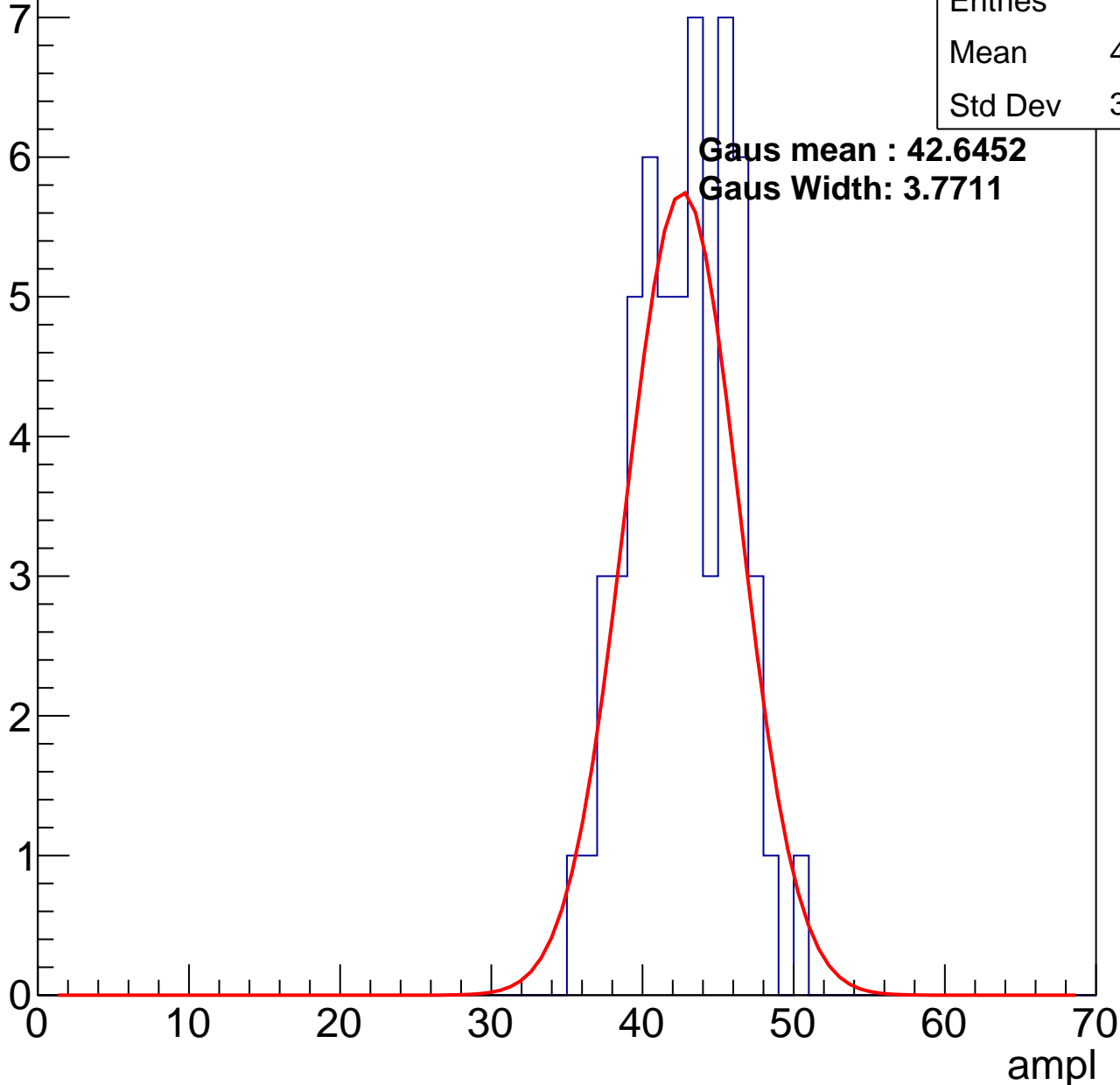
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	42.26
Std Dev	3.327

**Gaus mean : 42.6452**

**Gaus Width: 3.7711**

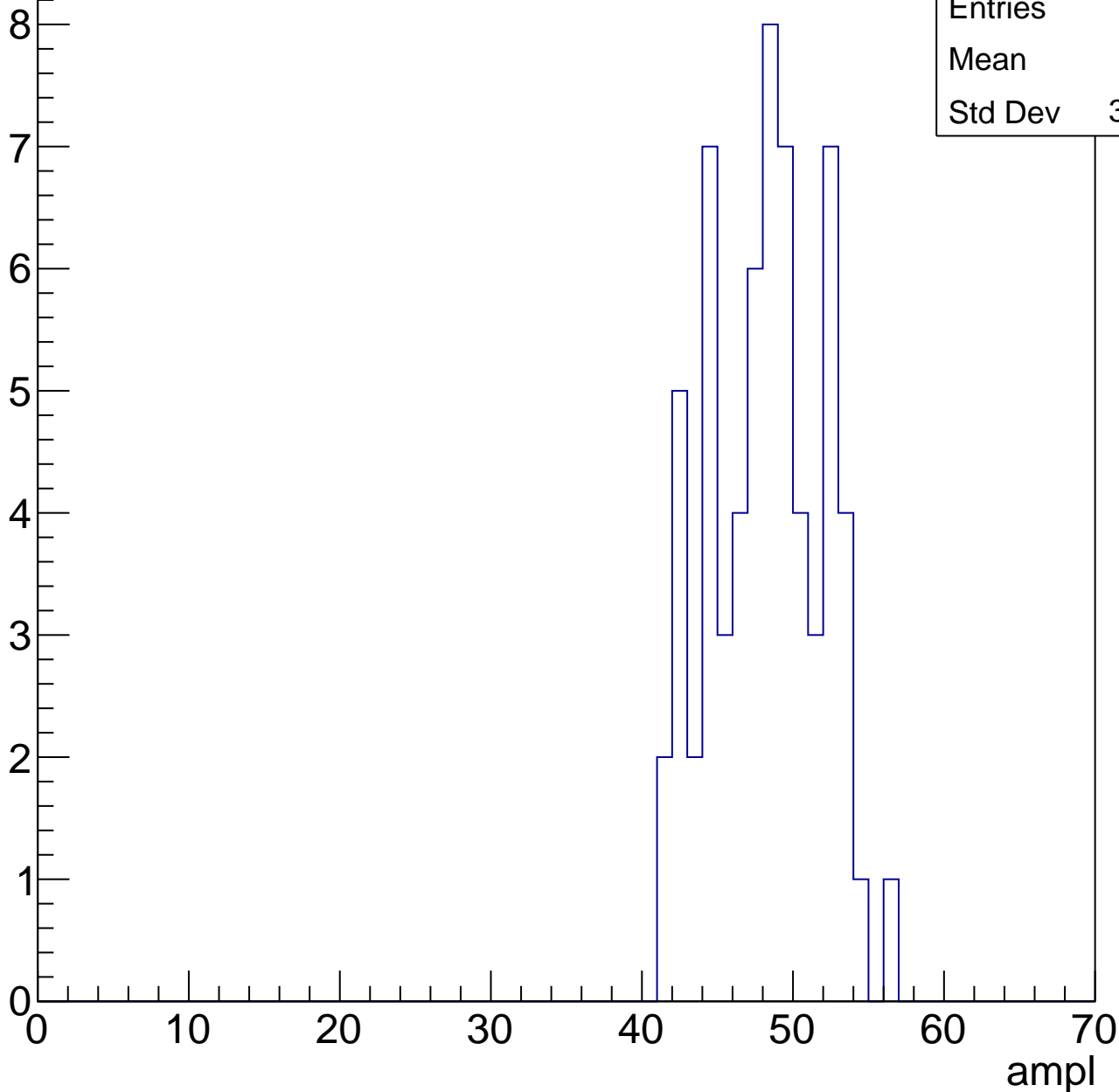


# B1L101S, U3-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

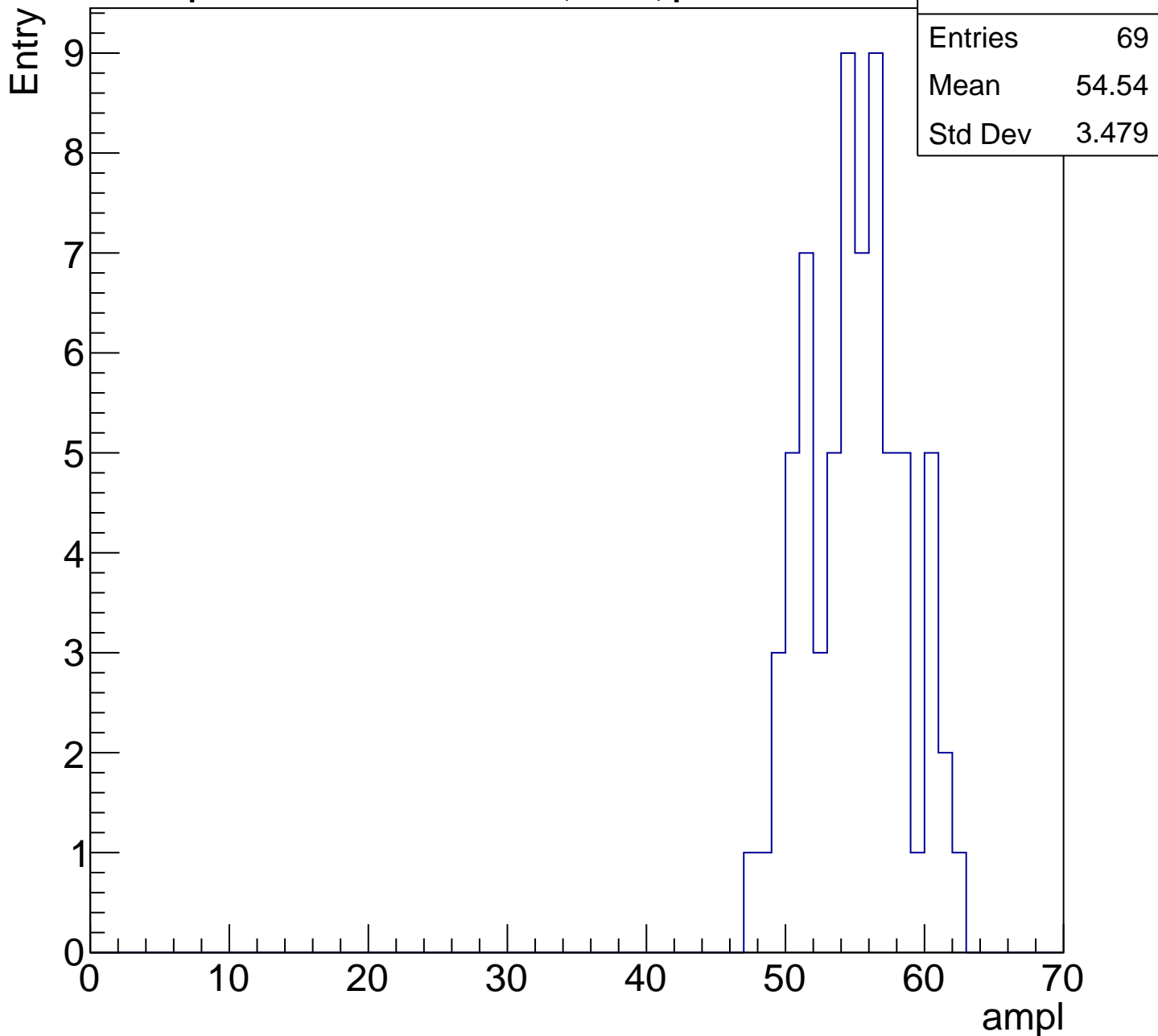
Entry

Entries	64
Mean	47.7
Std Dev	3.634



# B1L101S, U3-ch105, adc4

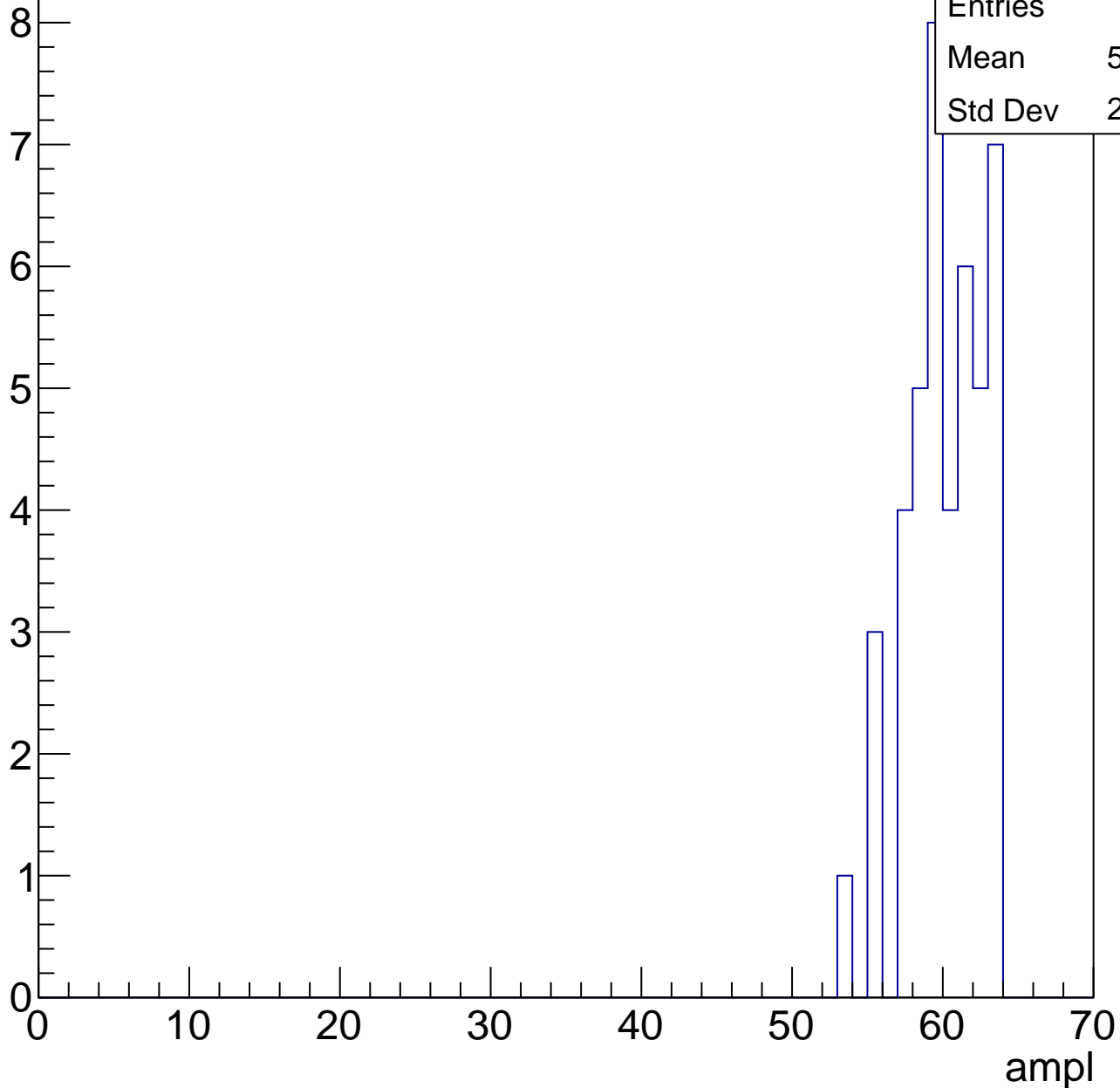
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

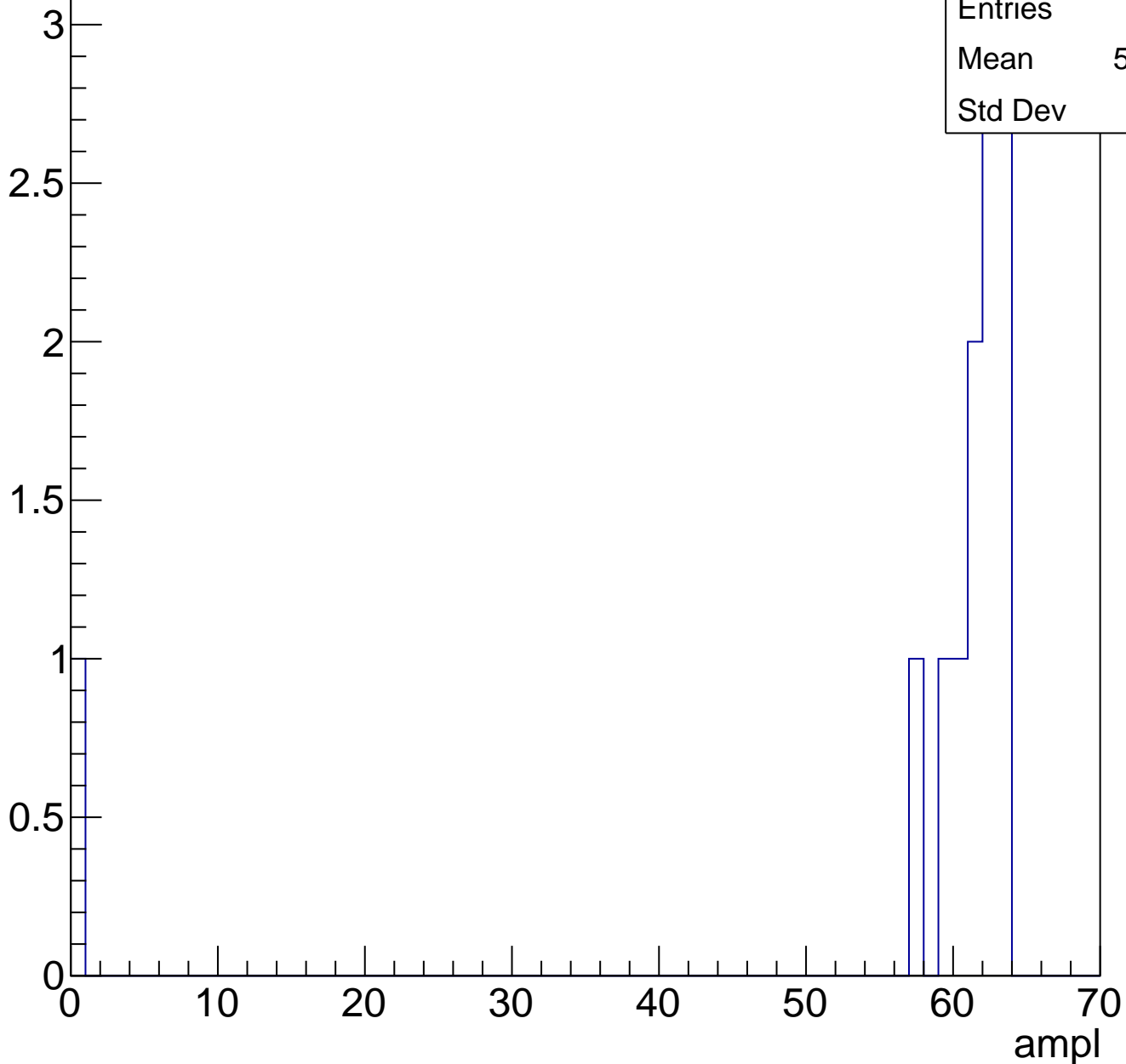
Entry



# B1L101S, U3-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

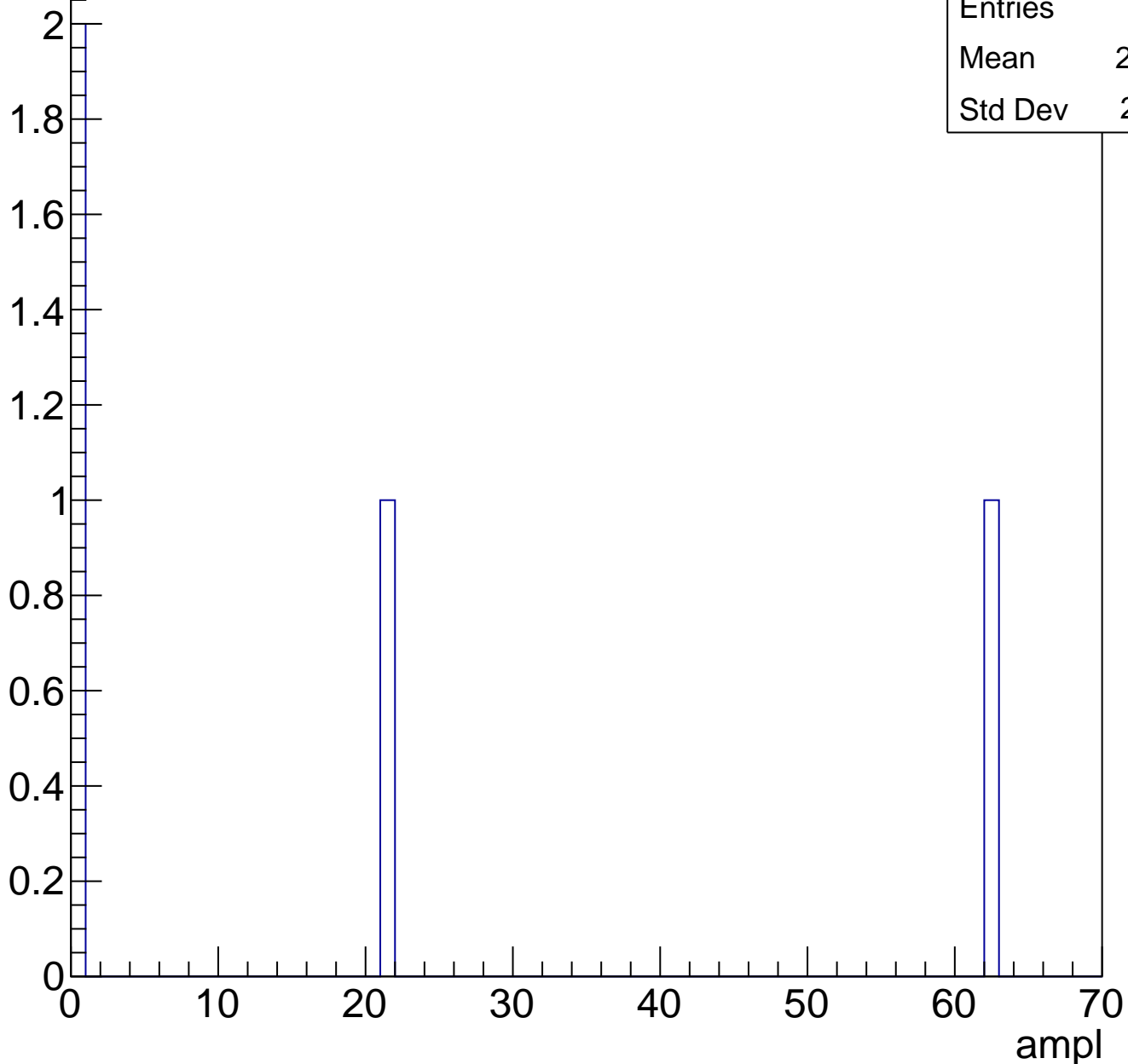




# B1L101S, U3-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	4
Mean	20.75
Std Dev	25.31

# B1L101S, U3-ch106, adc0

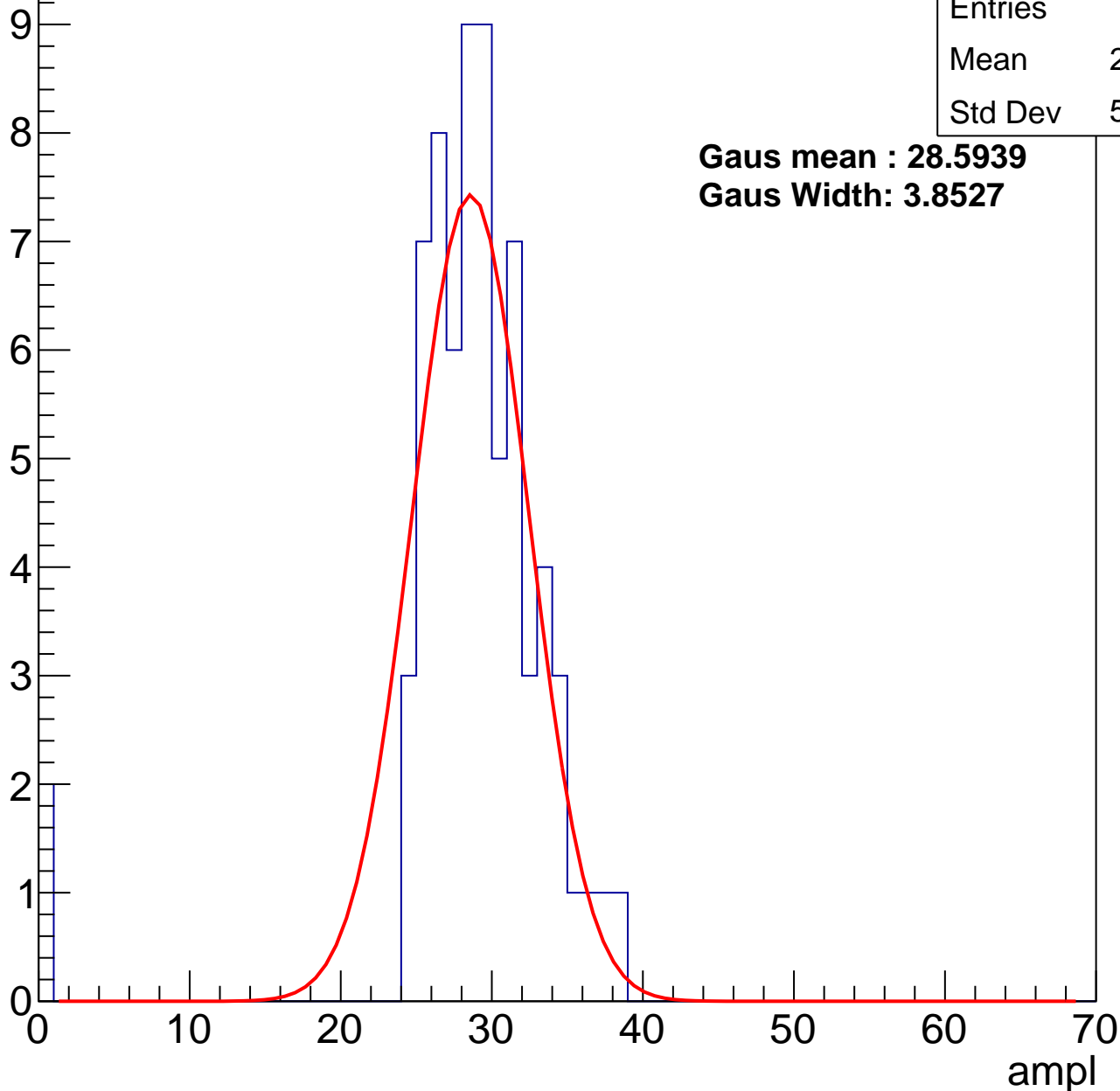
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	28.19
Std Dev	5.802

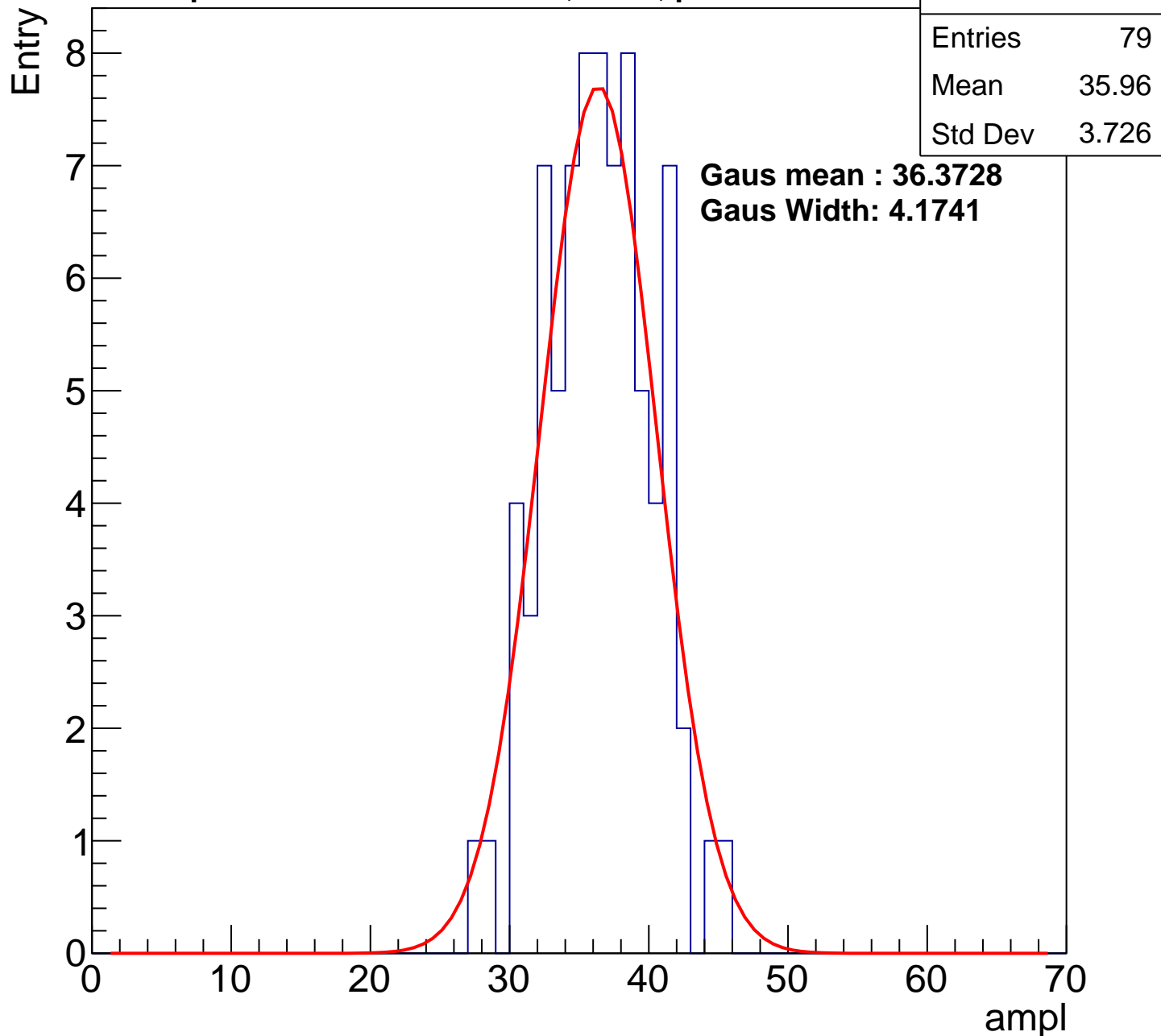
**Gaus mean : 28.5939**

**Gaus Width: 3.8527**



# B1L101S, U3-ch106, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch106, adc2

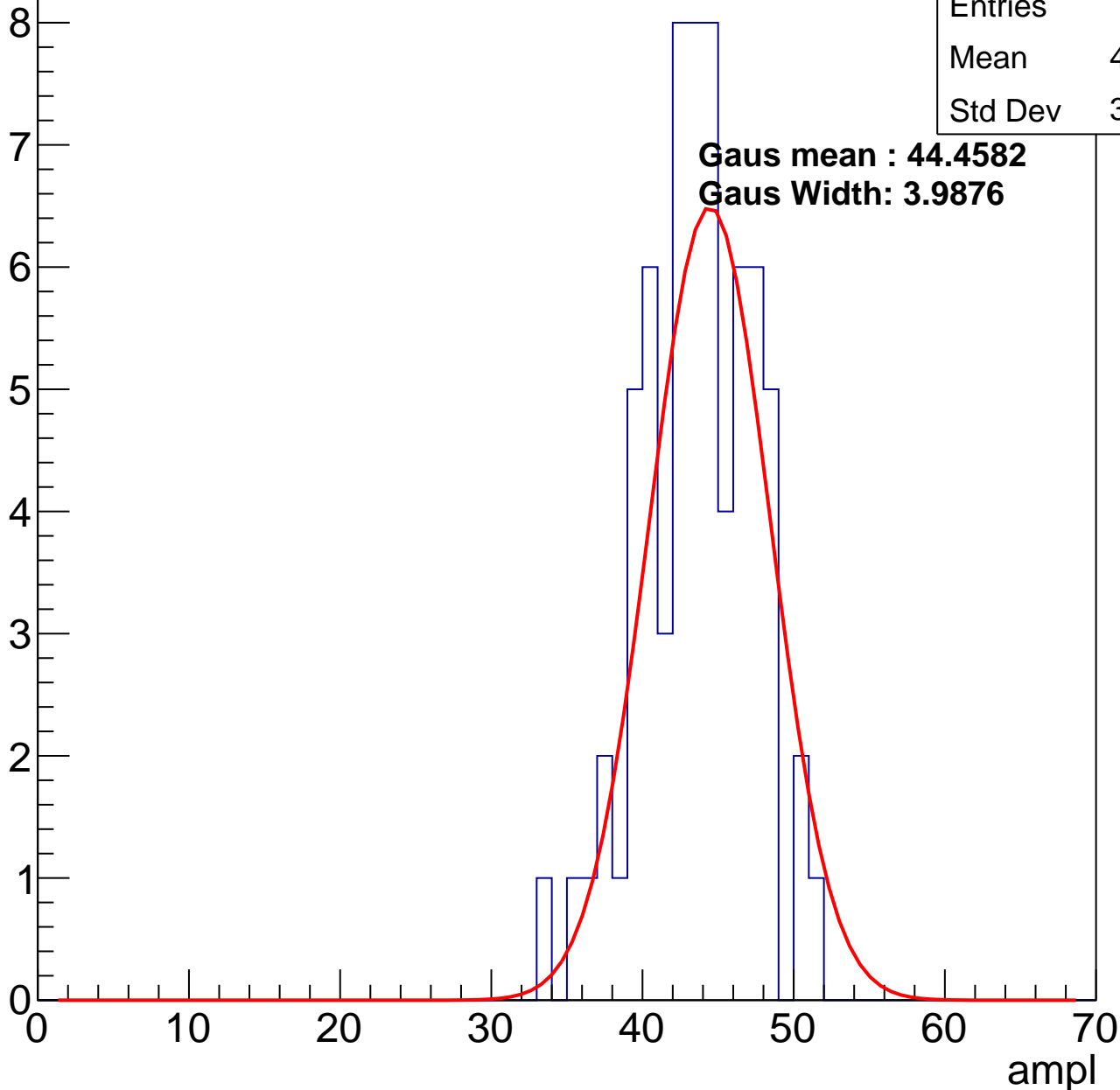
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	43.16
Std Dev	3.685

**Gaus mean : 44.4582**

**Gaus Width: 3.9876**

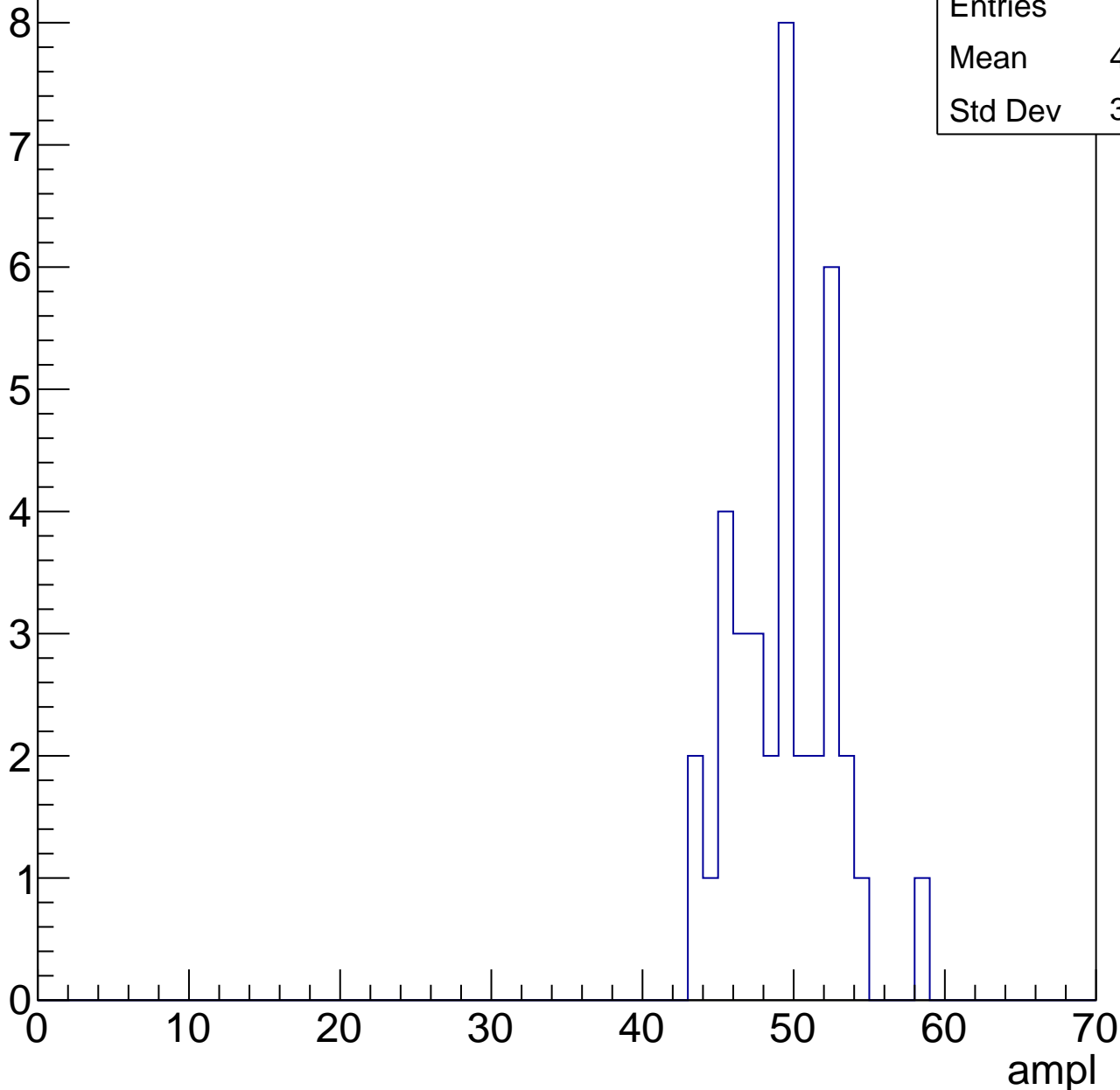


# B1L101S, U3-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

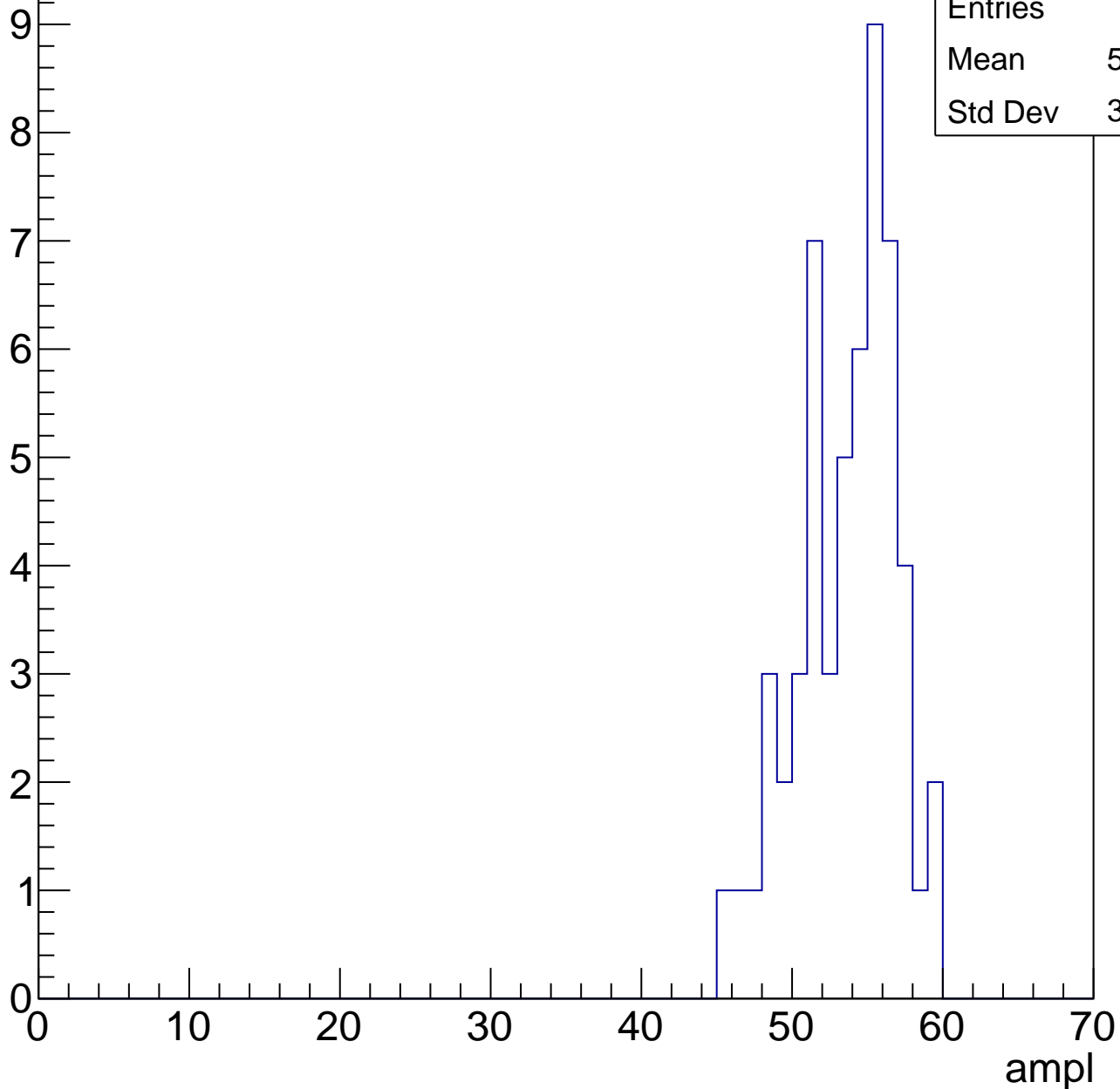
Entries	37
Mean	48.89
Std Dev	3.303



# B1L101S, U3-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

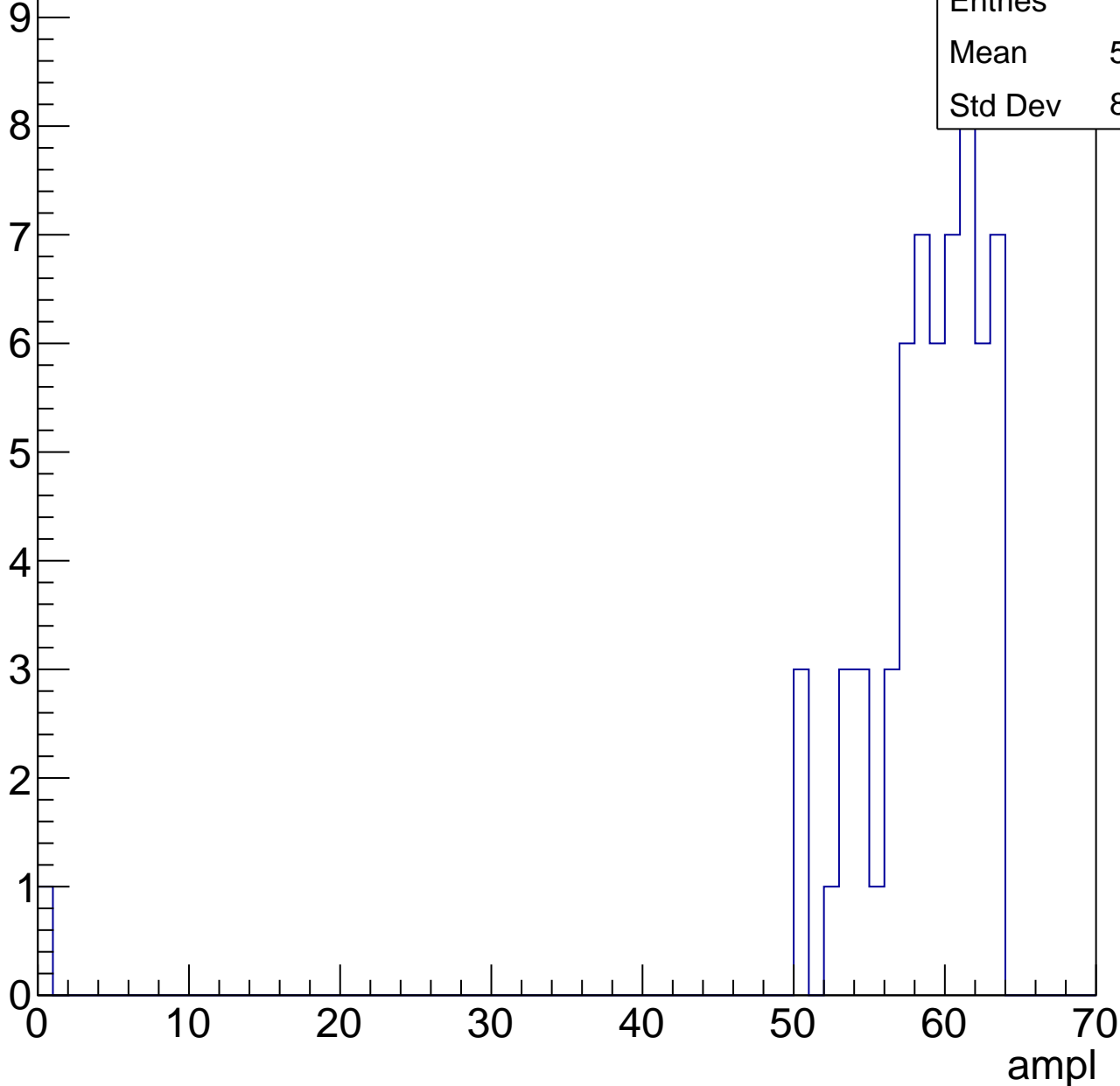


# B1L101S, U3-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

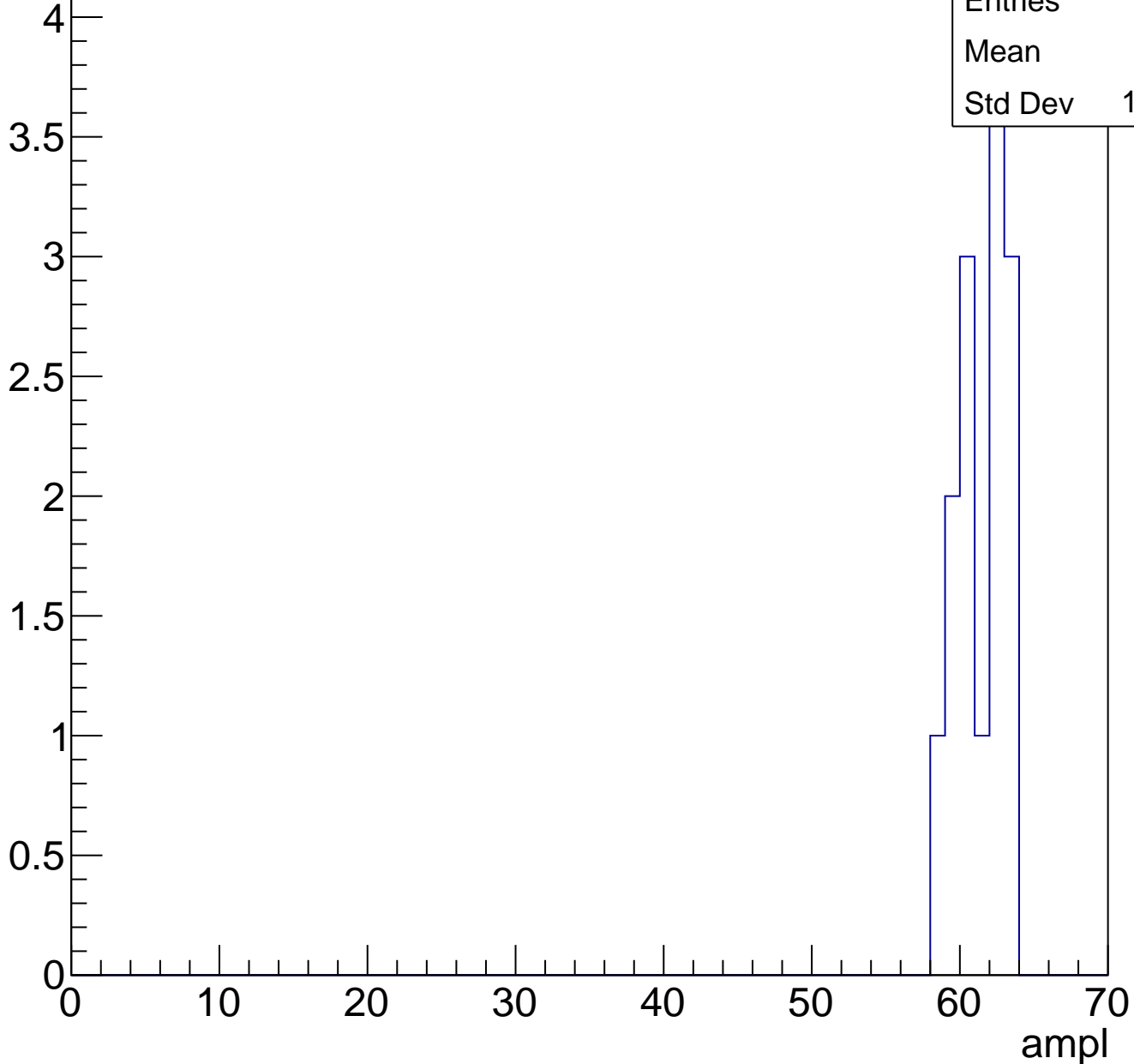
Entries	63
Mean	57.62
Std Dev	8.086



# B1L101S, U3-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U3-ch107, adc0

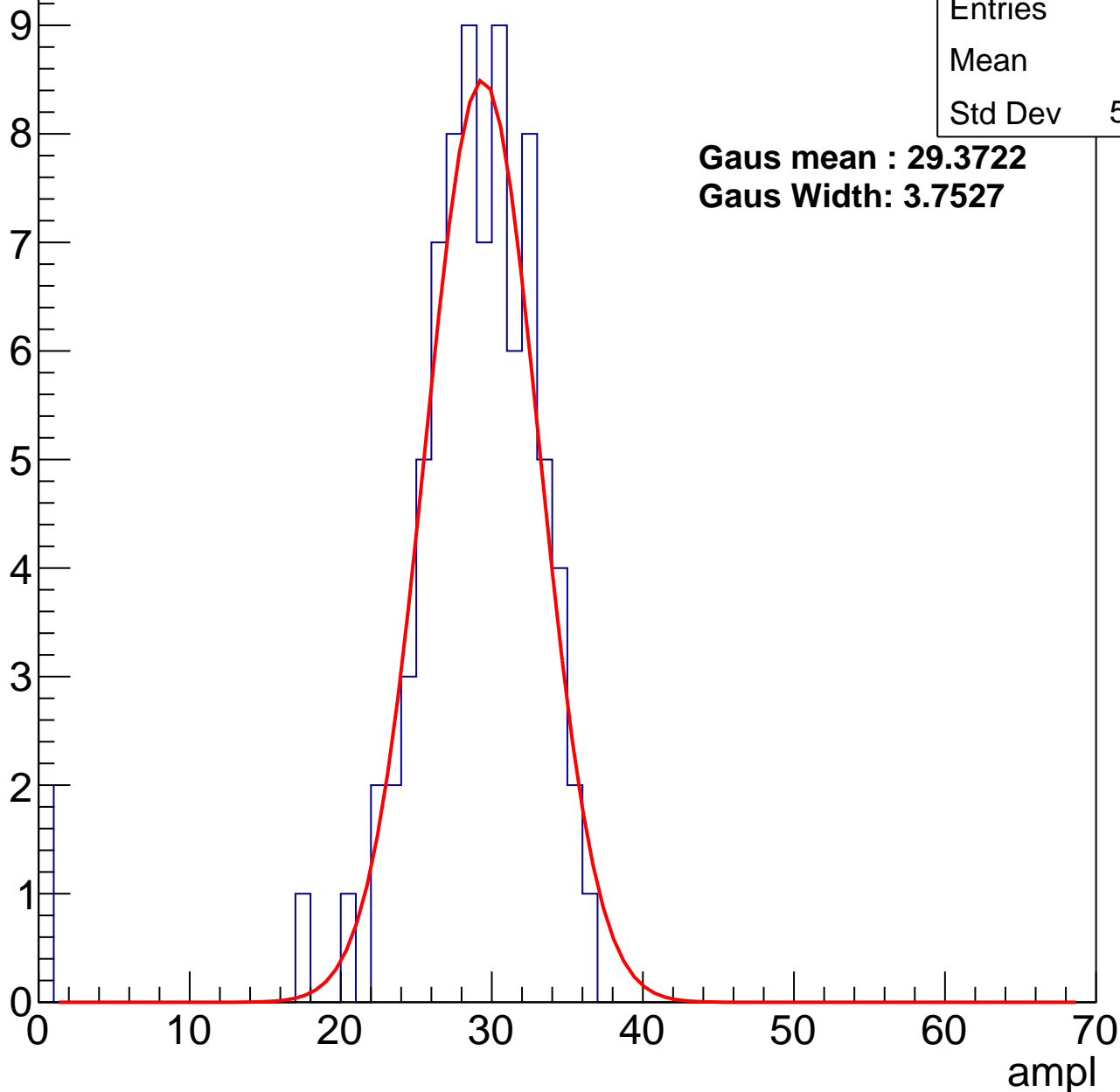
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	82
Mean	28
Std Dev	5.696

**Gaus mean : 29.3722**

**Gaus Width: 3.7527**



# B1L101S, U3-ch107, adc1

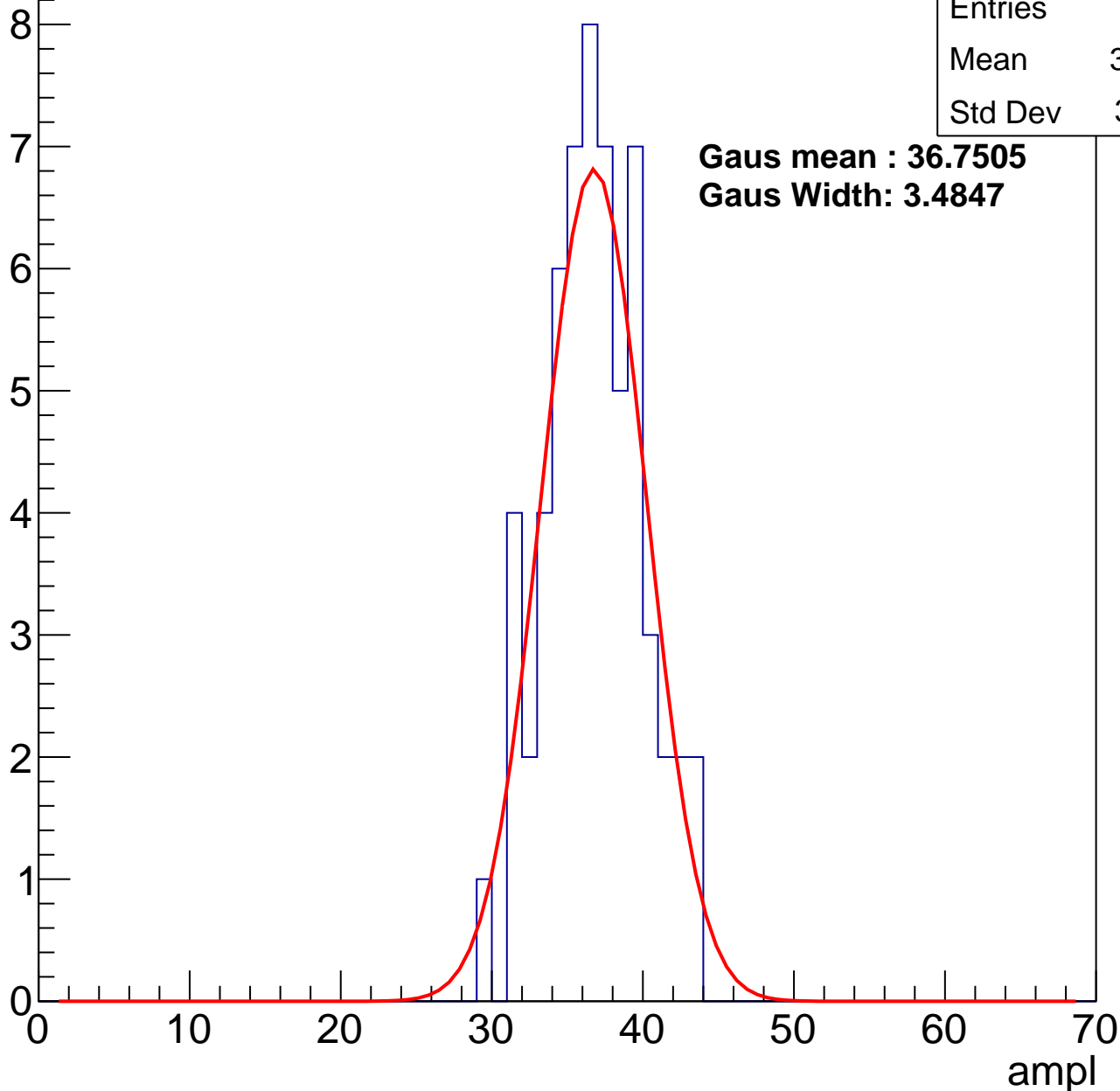
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	36.33
Std Dev	3.161

**Gaus mean : 36.7505**

**Gaus Width: 3.4847**



# B1L101S, U3-ch107, adc2

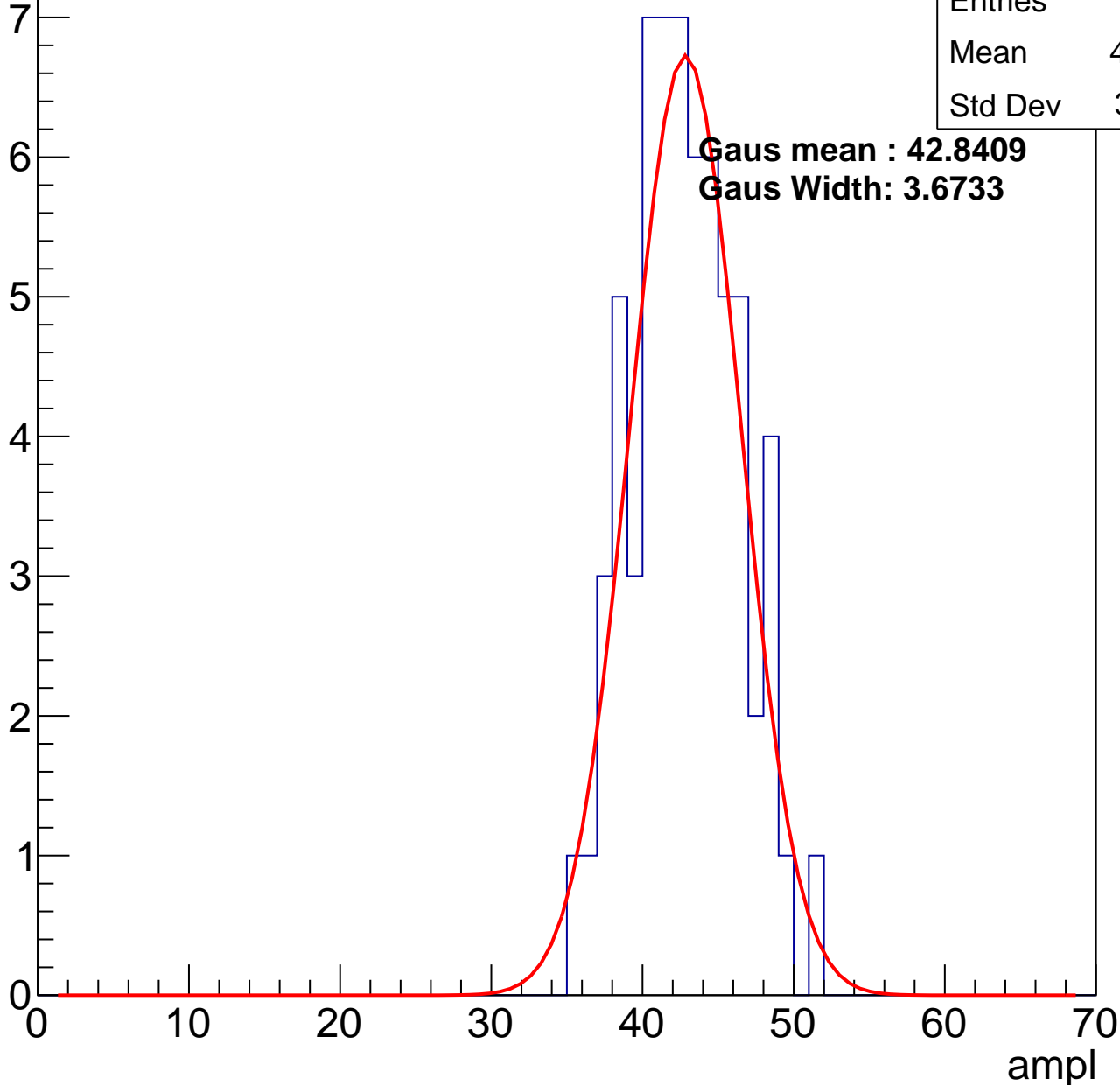
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	64
Mean	42.39
Std Dev	3.471

**Gaus mean : 42.8409**

**Gaus Width: 3.6733**

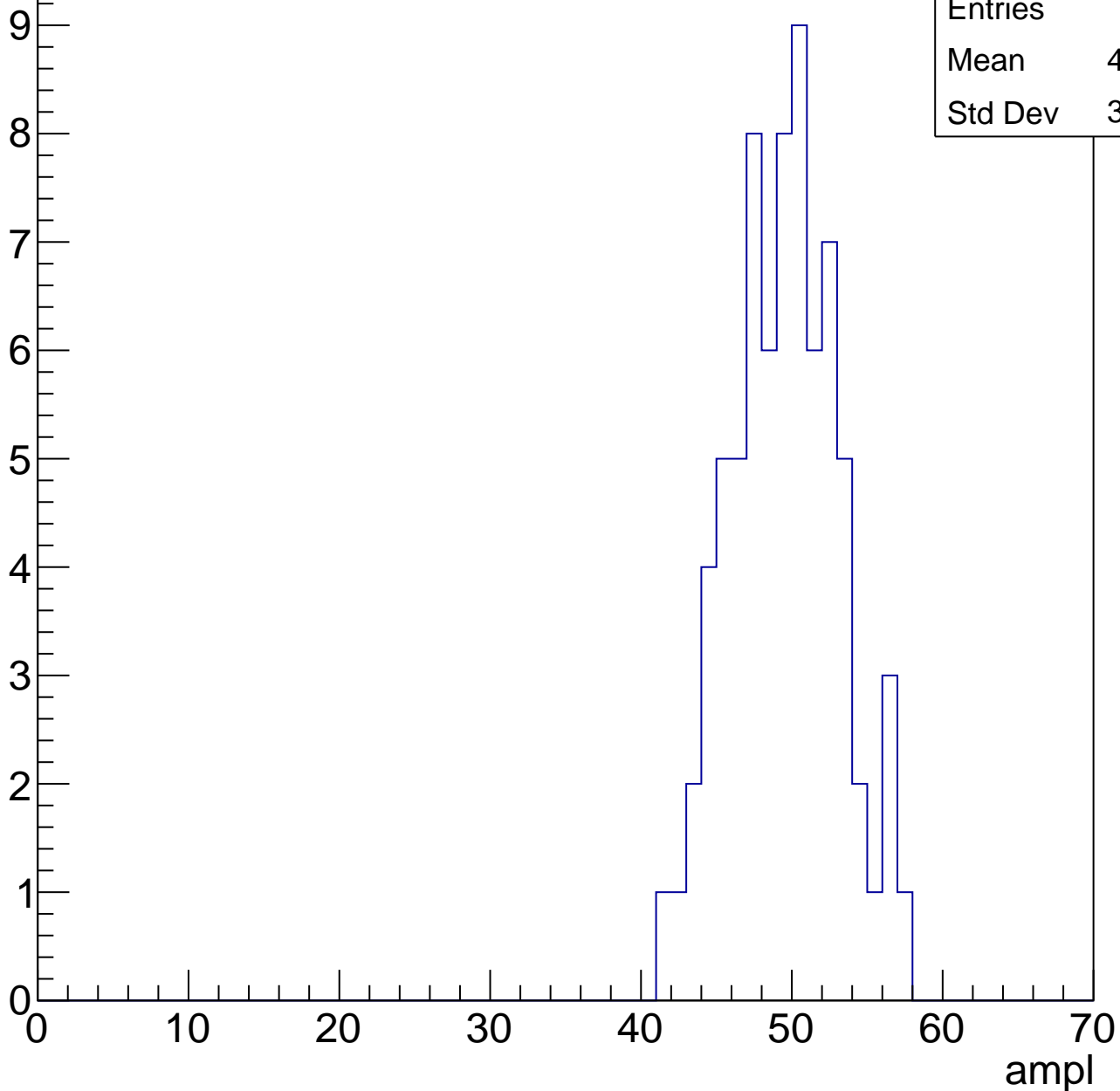


# B1L101S, U3-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

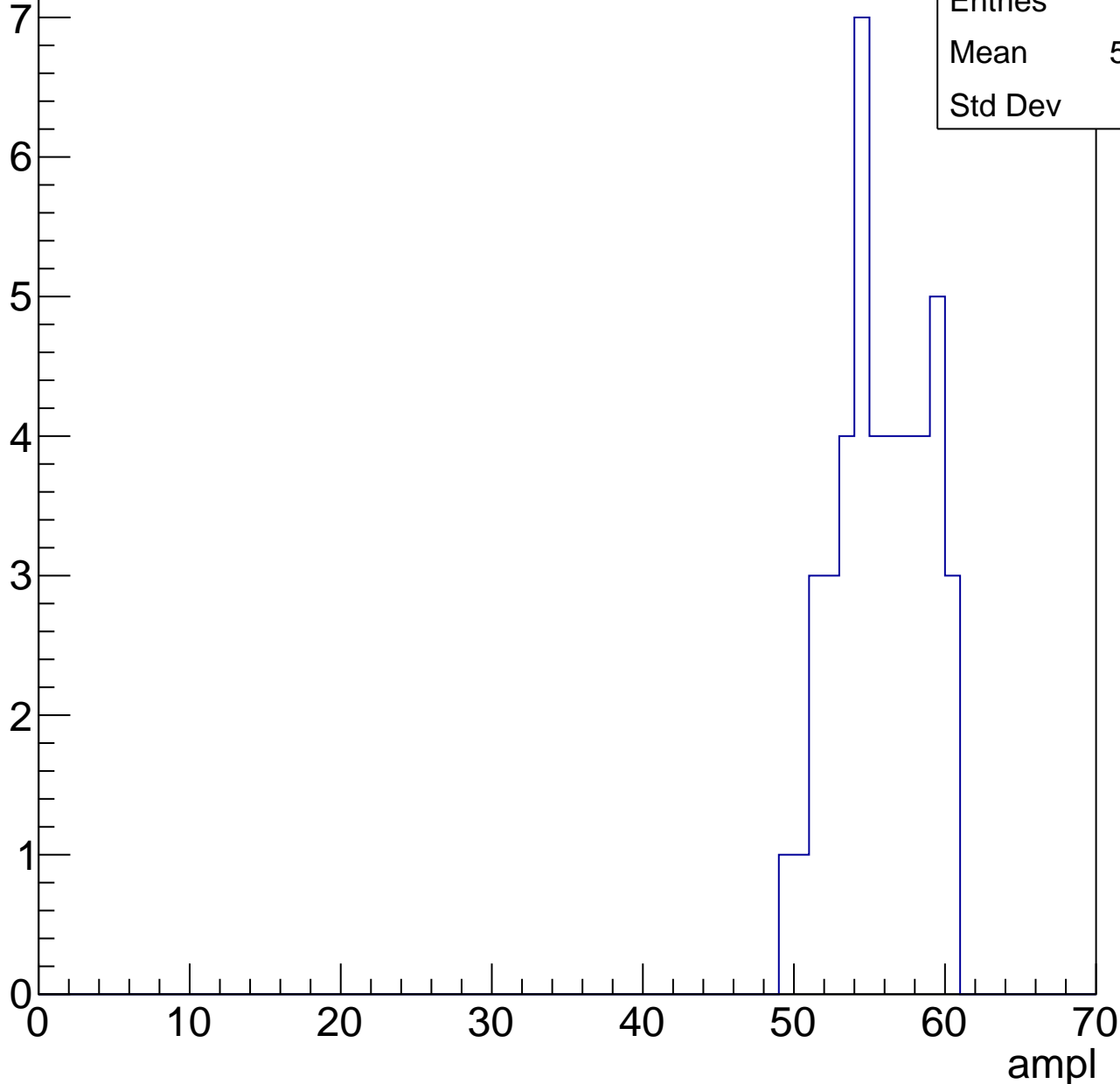
Entries	74
Mean	49.04
Std Dev	3.528



# B1L101S, U3-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



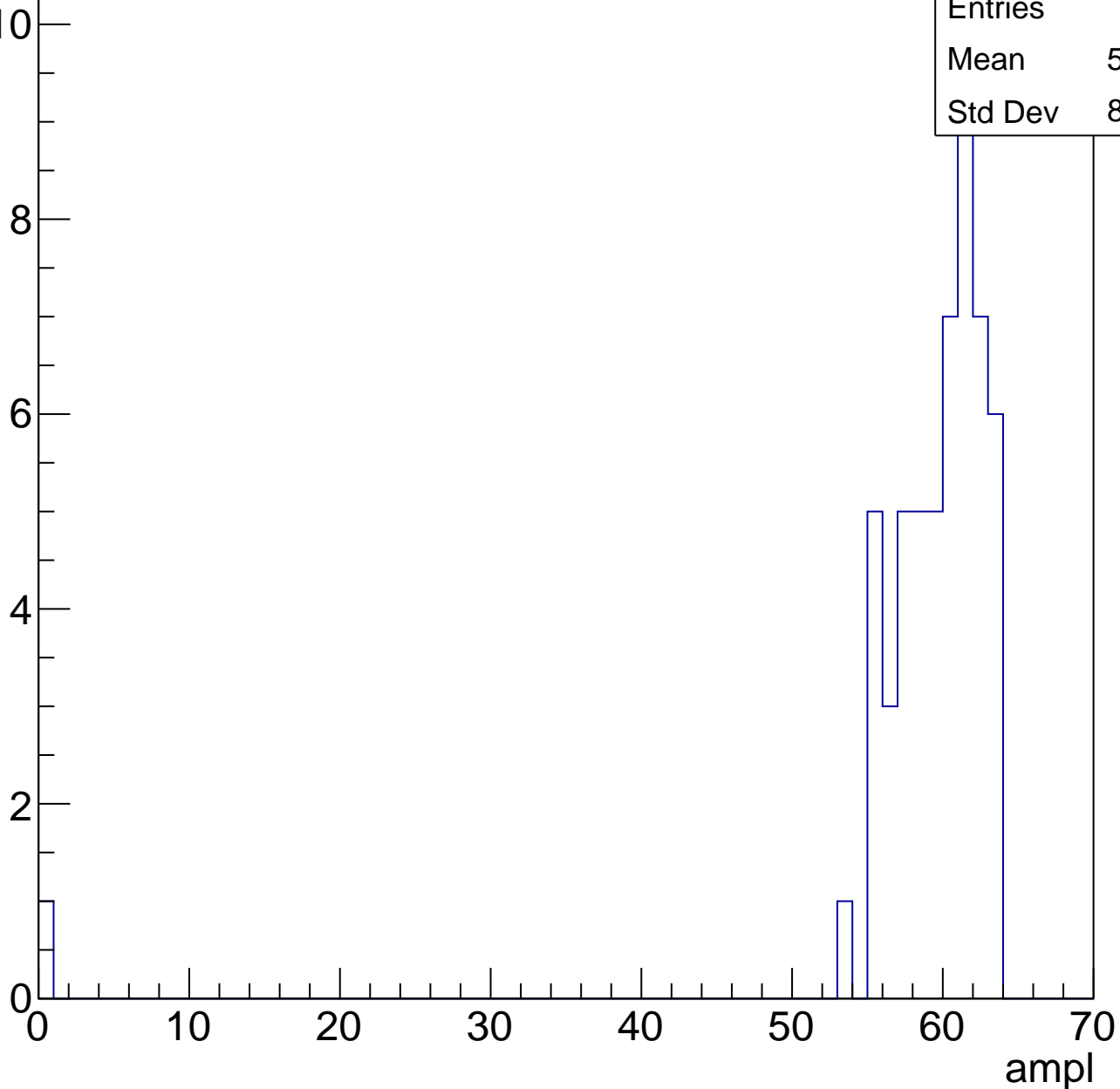
Entries	43
Mean	55.28
Std Dev	2.92

# B1L101S, U3-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

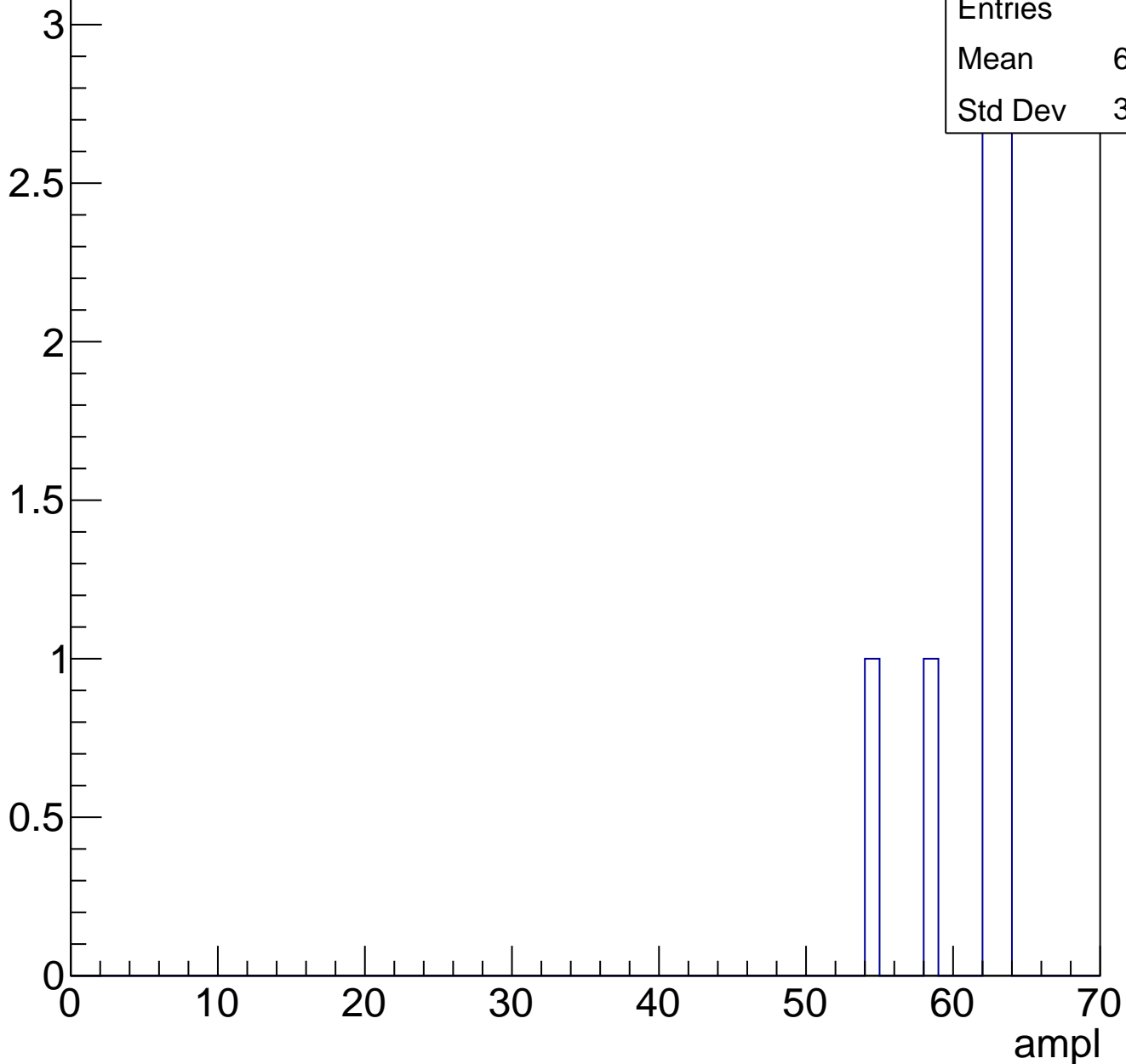
Entries	55
Mean	58.33
Std Dev	8.345



# B1L101S, U3-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L101S, U3-ch108, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	77
Mean	25.87
Std Dev	5.56

**Gaus mean : 26.9017**

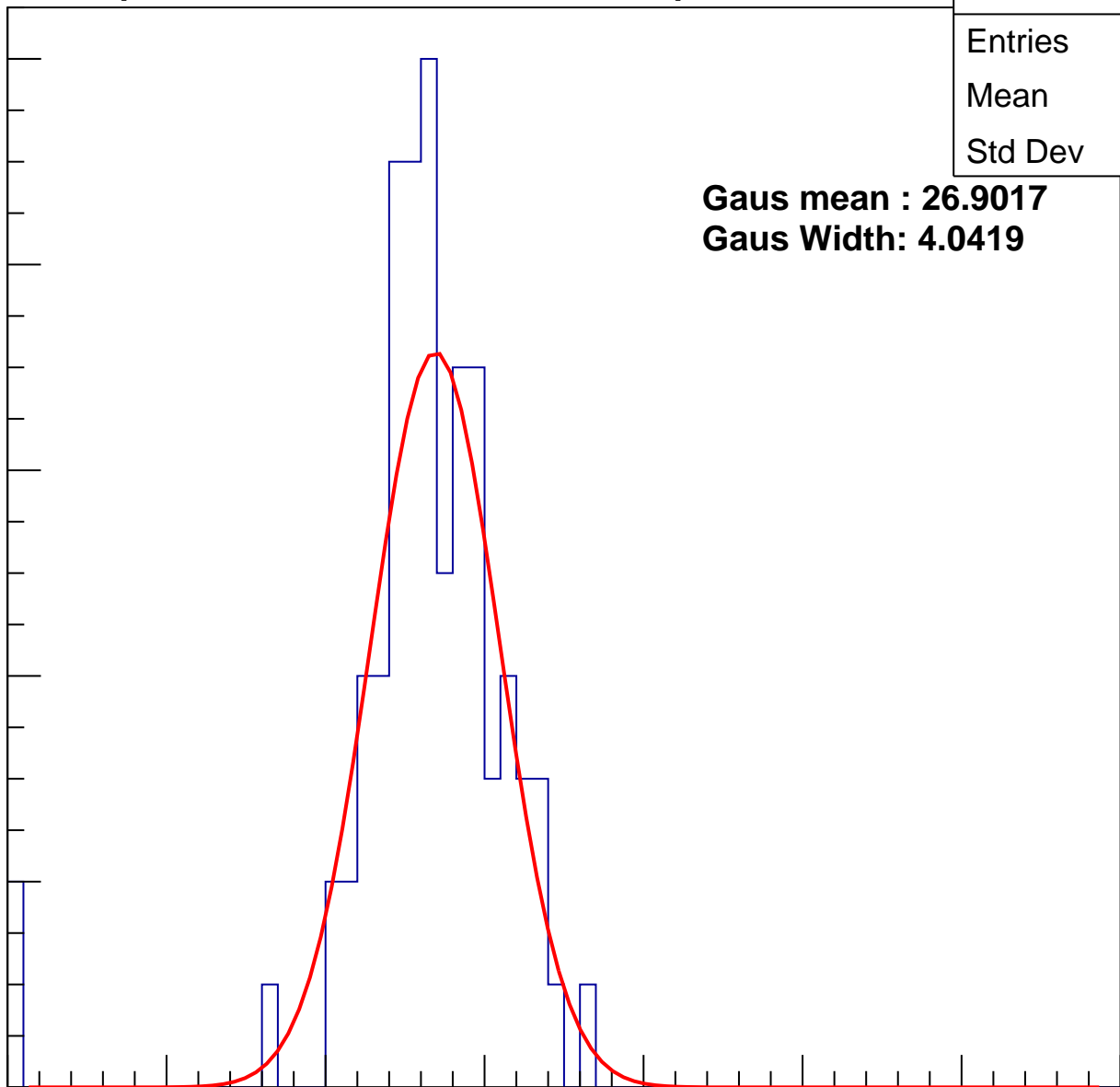
**Gaus Width: 4.0419**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U3-ch108, adc1

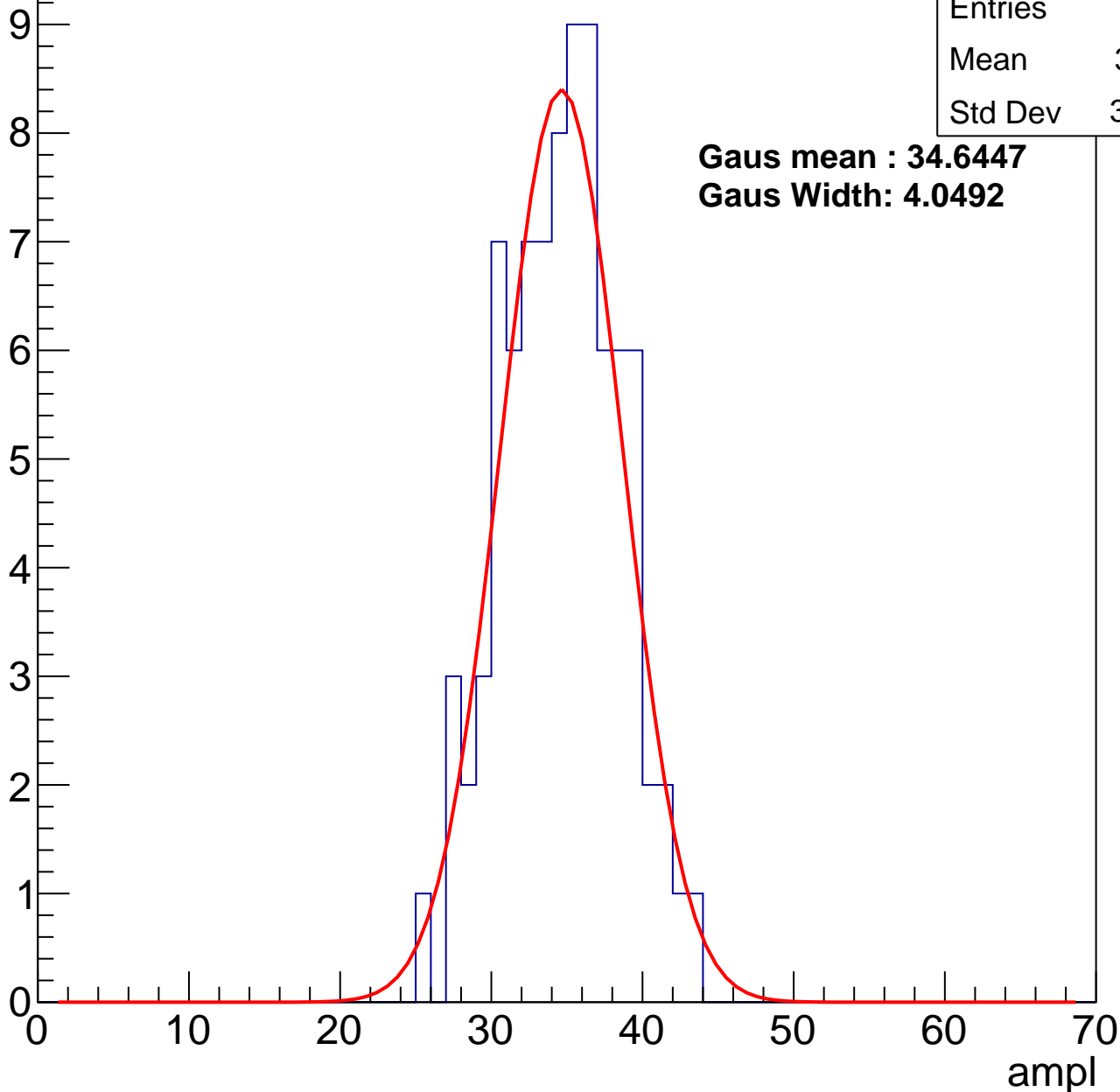
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	86
Mean	34.21
Std Dev	3.785

**Gaus mean : 34.6447**

**Gaus Width: 4.0492**



# B1L101S, U3-ch108, adc2

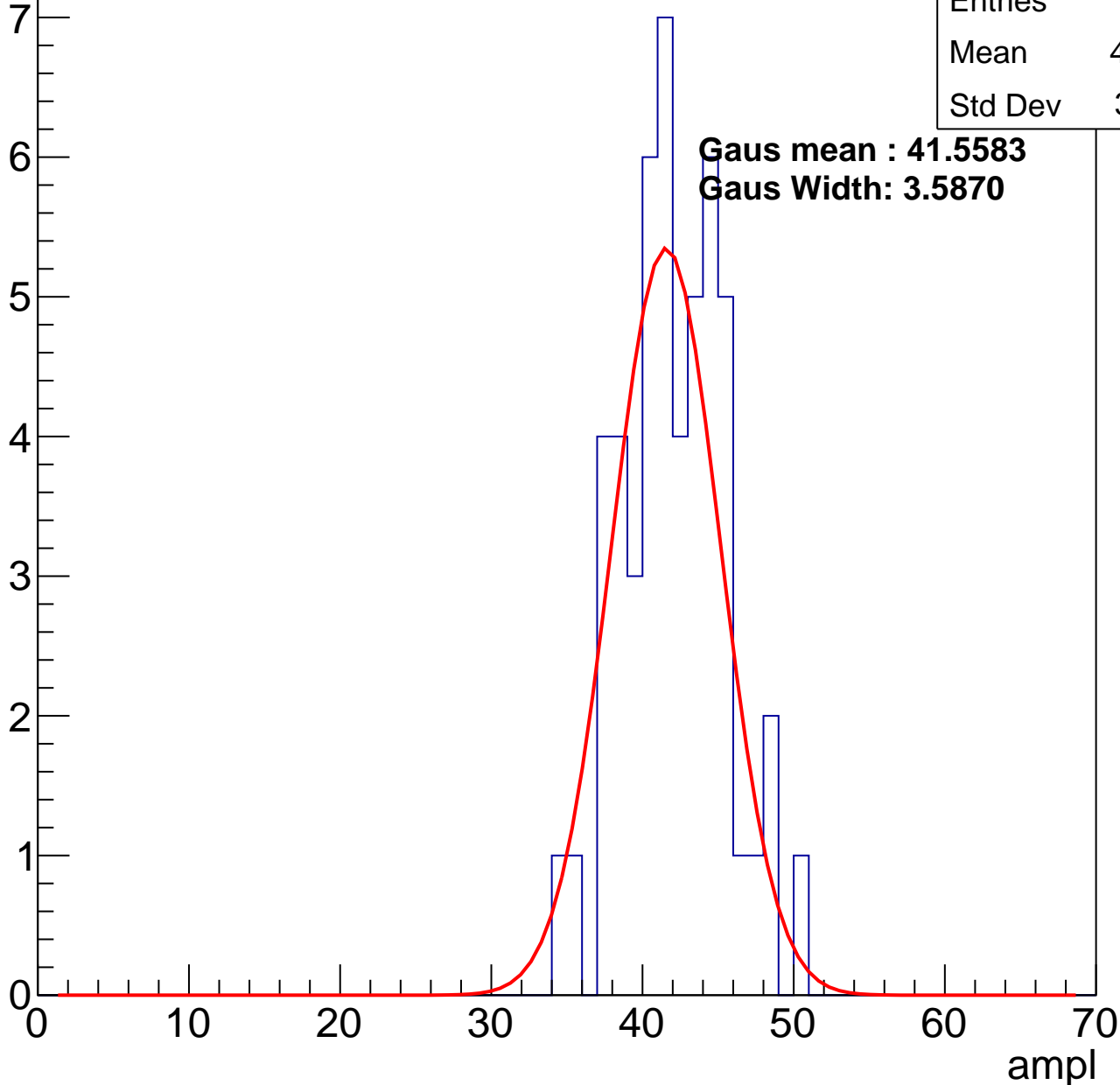
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	41.65
Std Dev	3.371

**Gaus mean : 41.5583**

**Gaus Width: 3.5870**

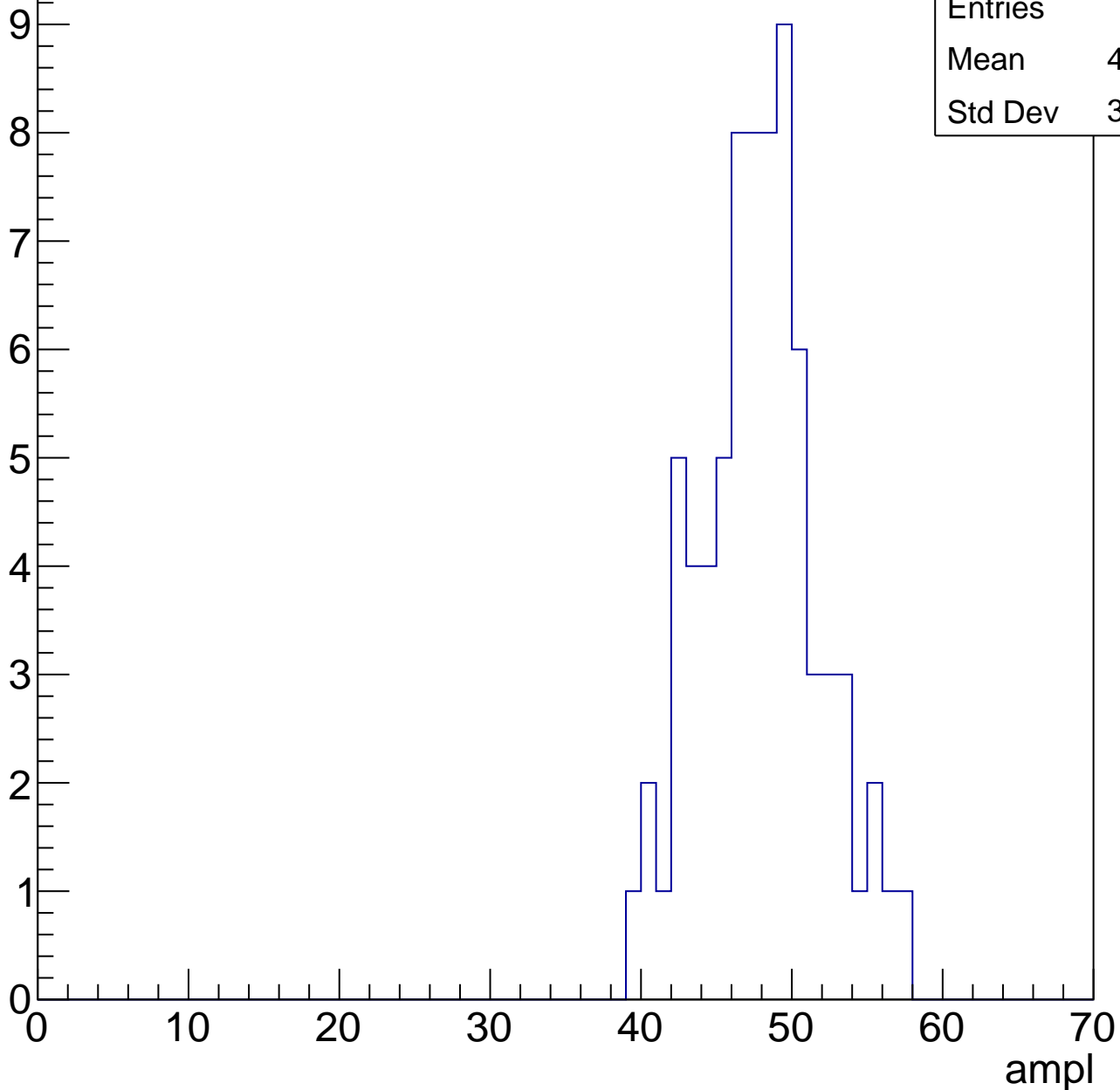


# B1L101S, U3-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	47.43
Std Dev	3.872

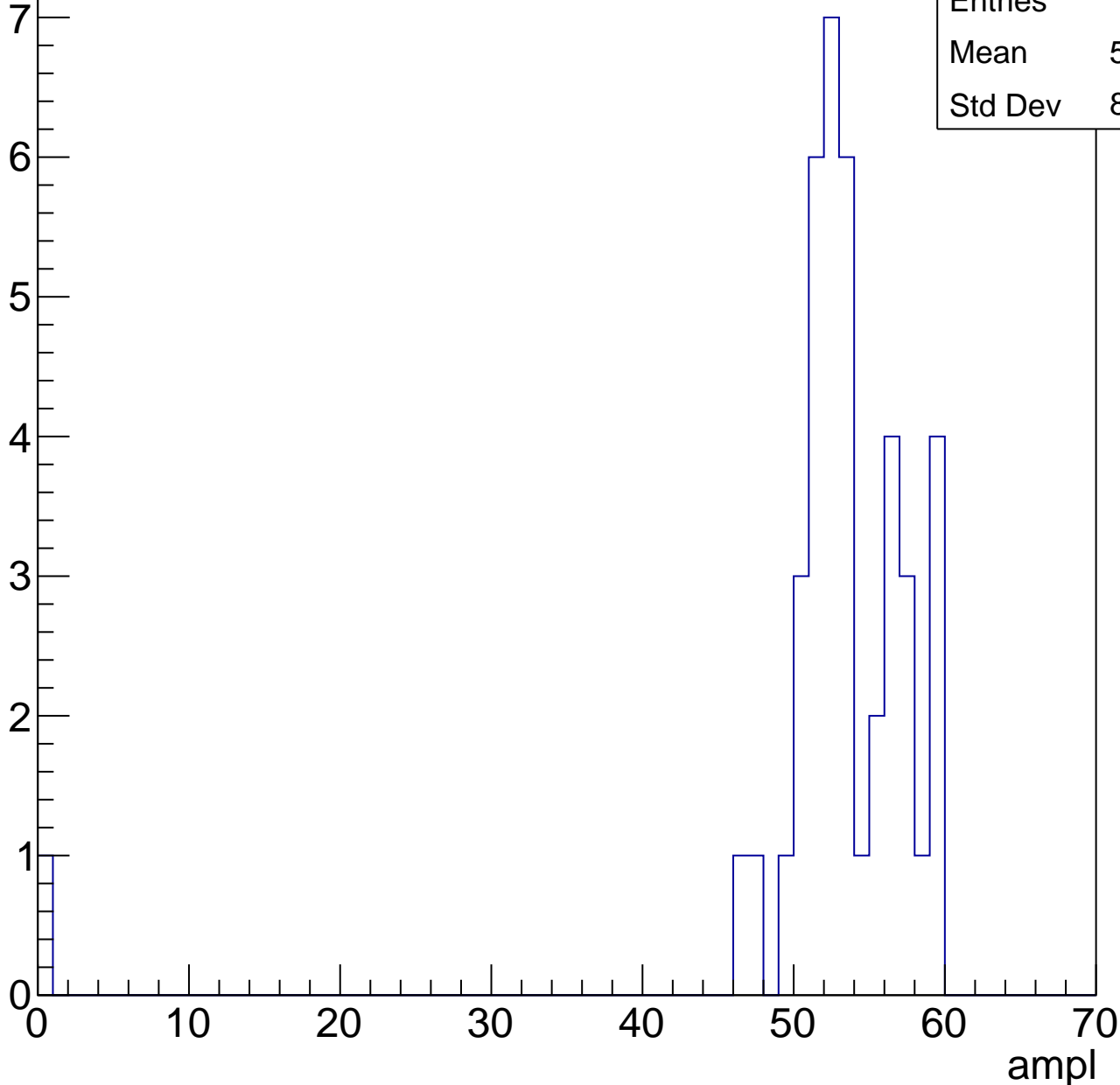


# B1L101S, U3-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	41
Mean	52.02
Std Dev	8.822



# B1L101S, U3-ch108, adc5

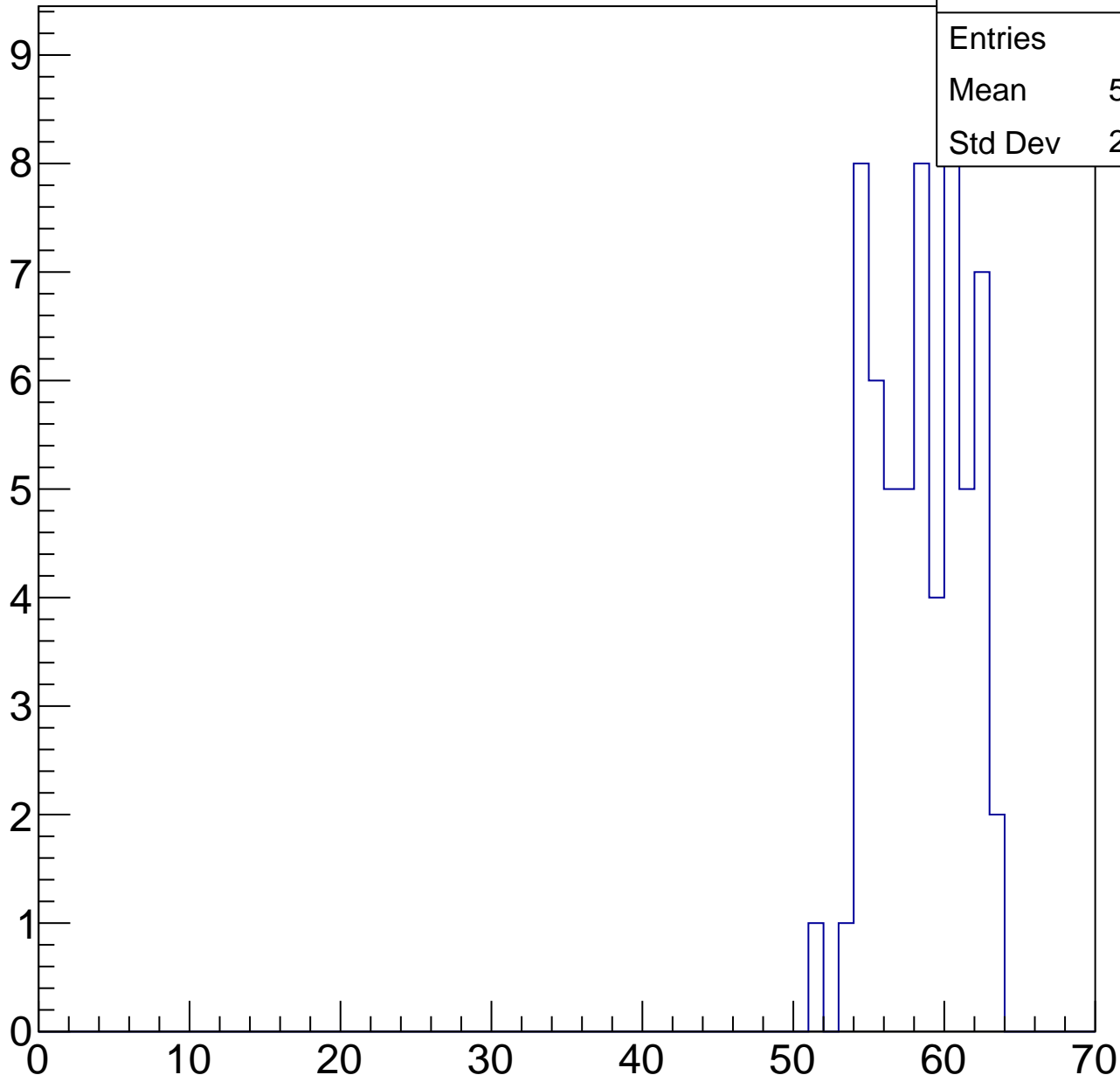
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	61
Mean	57.97
Std Dev	2.942

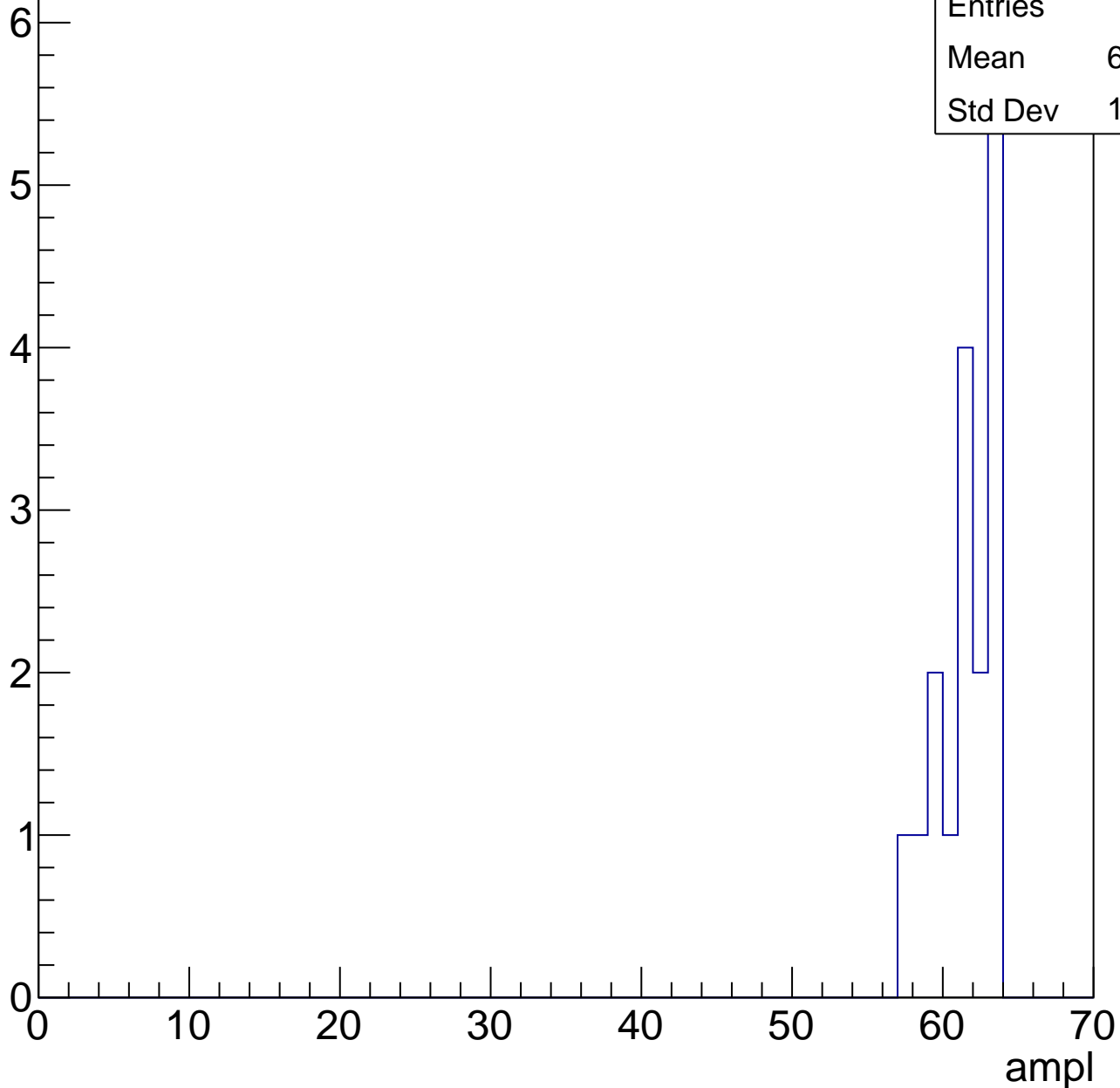
ampl



# B1L101S, U3-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

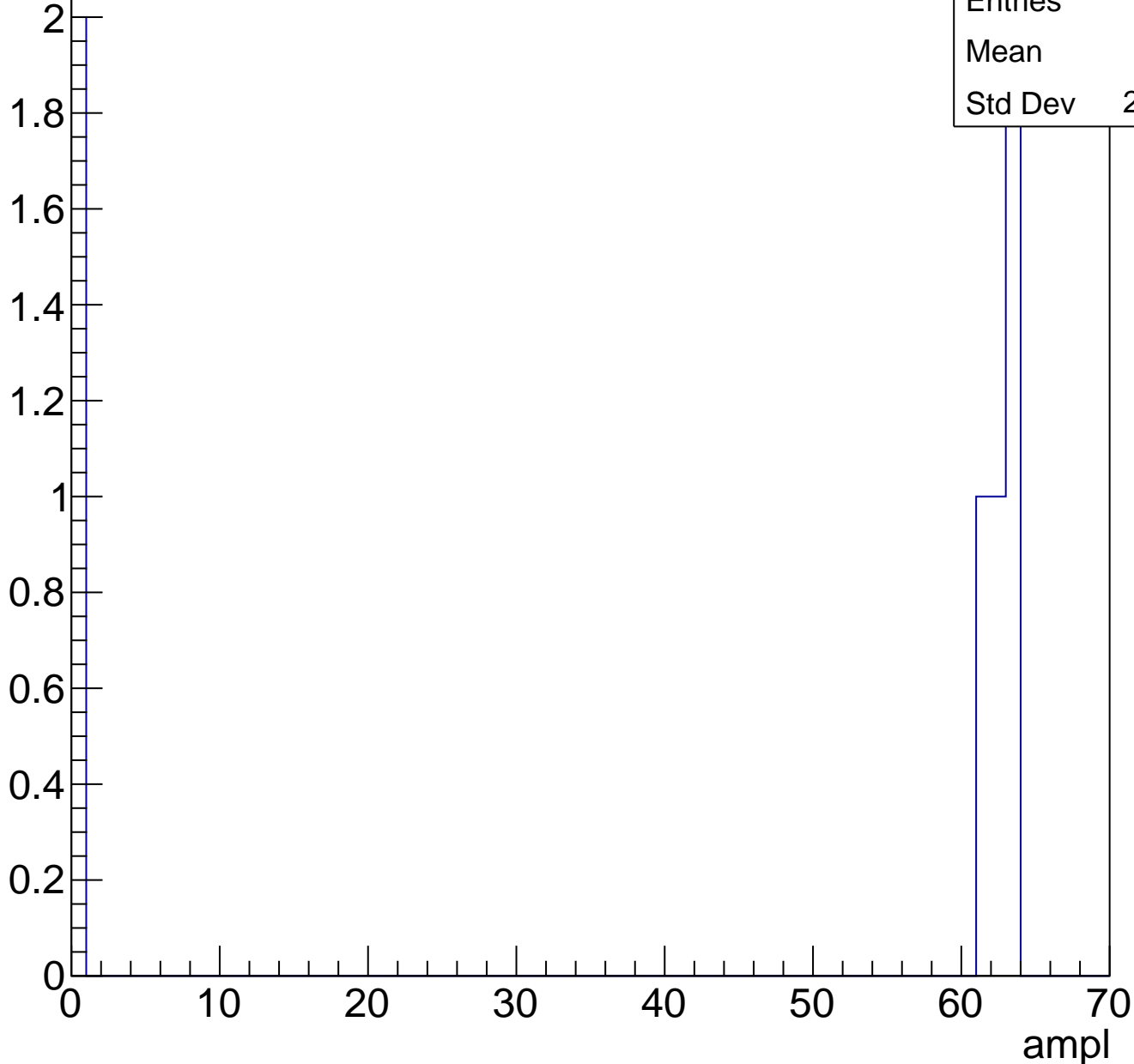




# B1L101S, U3-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch109, adc0

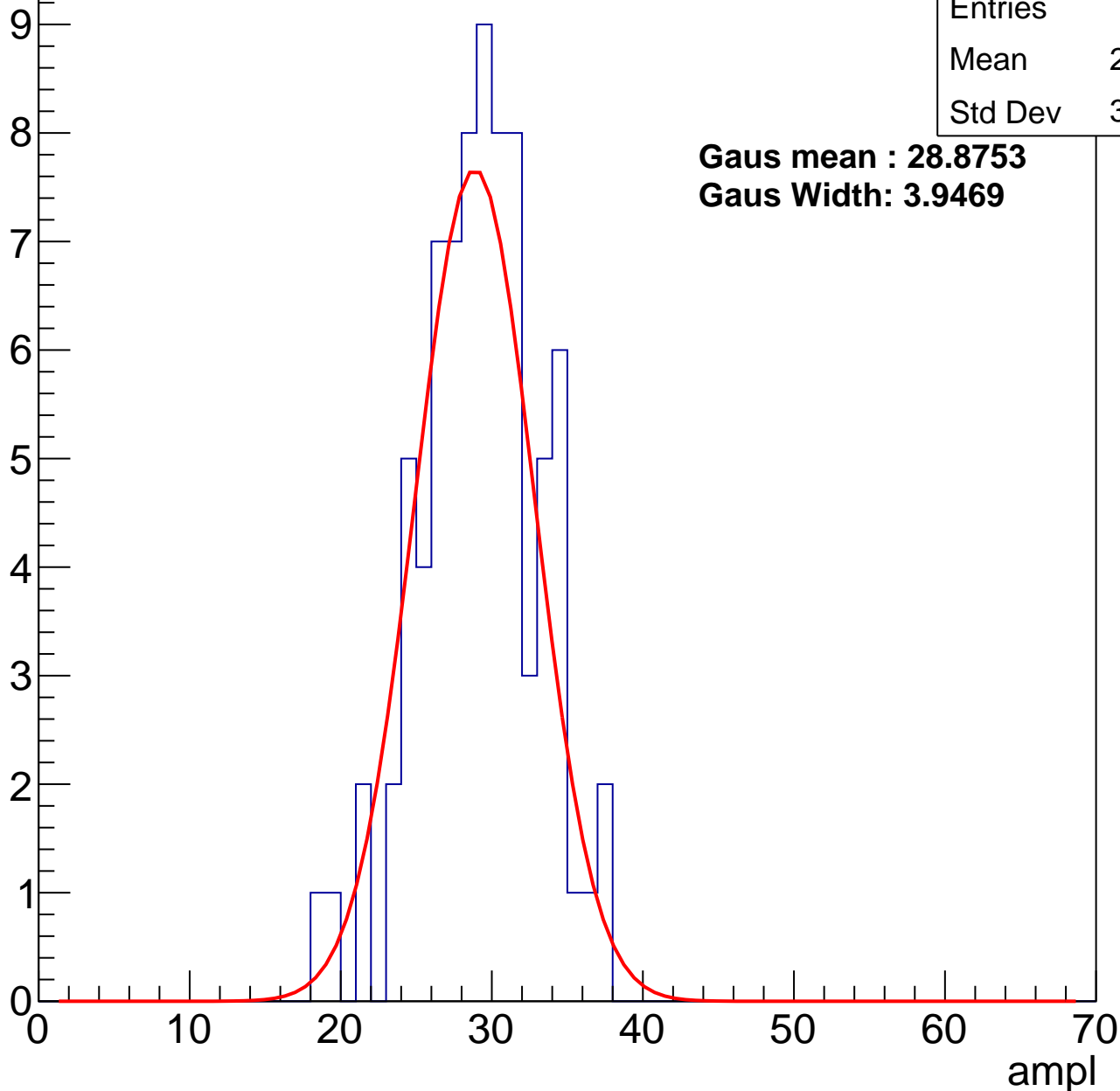
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	28.74
Std Dev	3.895

**Gaus mean : 28.8753**

**Gaus Width: 3.9469**



# B1L101S, U3-ch109, adc1

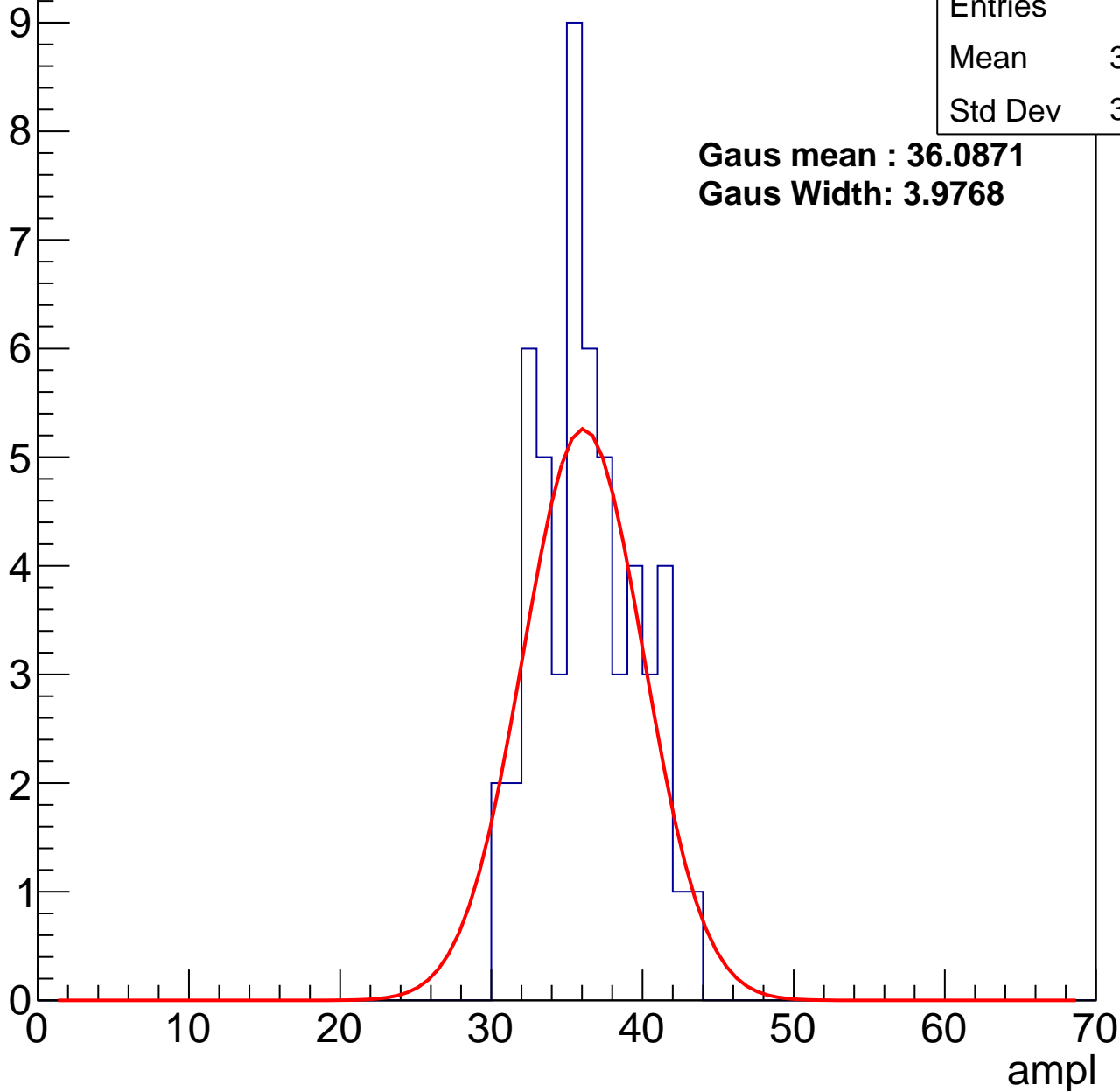
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	35.85
Std Dev	3.246

**Gaus mean : 36.0871**

**Gaus Width: 3.9768**



# B1L101S, U3-ch109, adc2

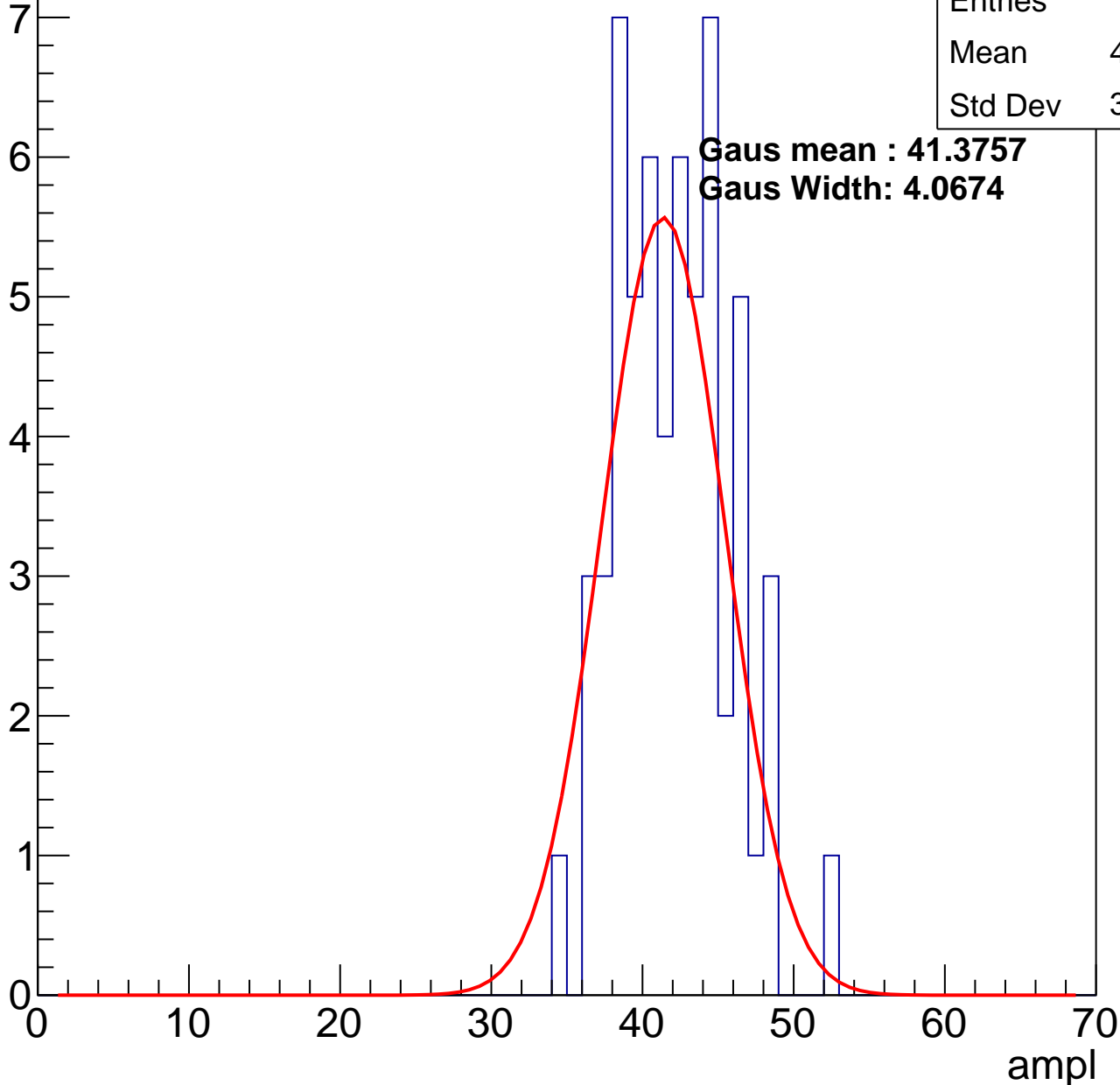
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	41.63
Std Dev	3.654

**Gaus mean : 41.3757**

**Gaus Width: 4.0674**

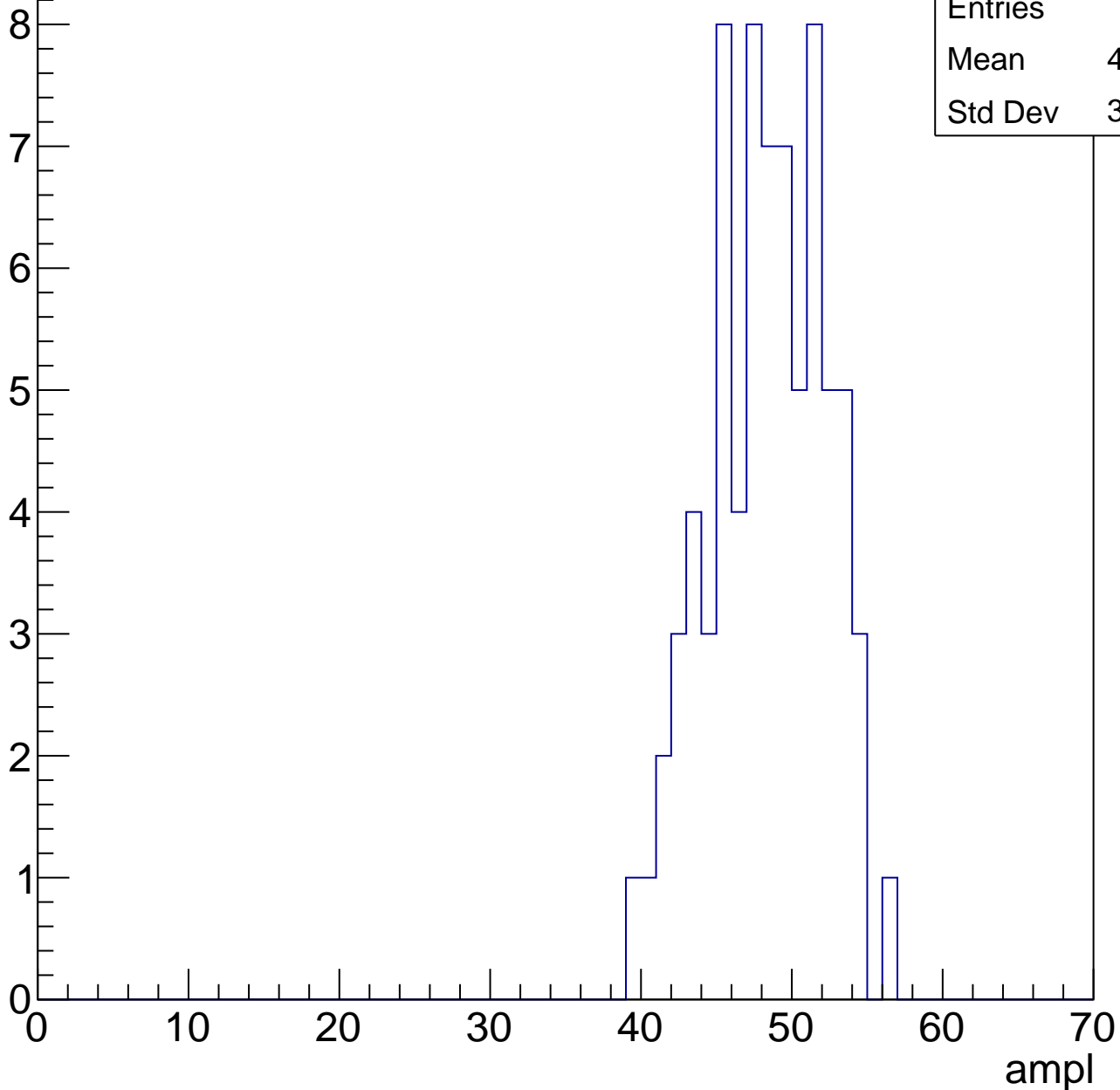


# B1L101S, U3-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	47.88
Std Dev	3.777

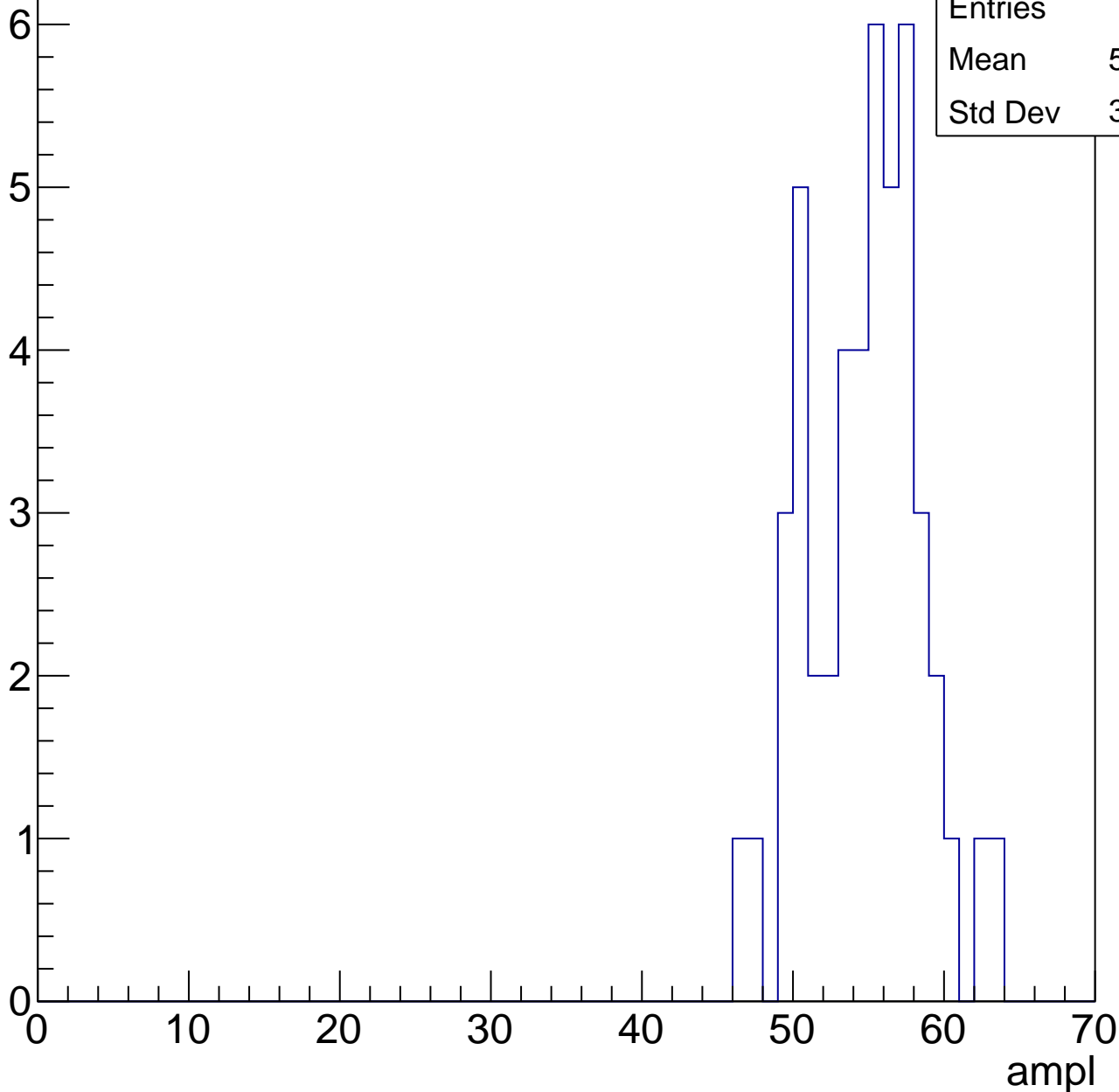


# B1L101S, U3-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	54.32
Std Dev	3.725



# B1L101S, U3-ch109, adc5

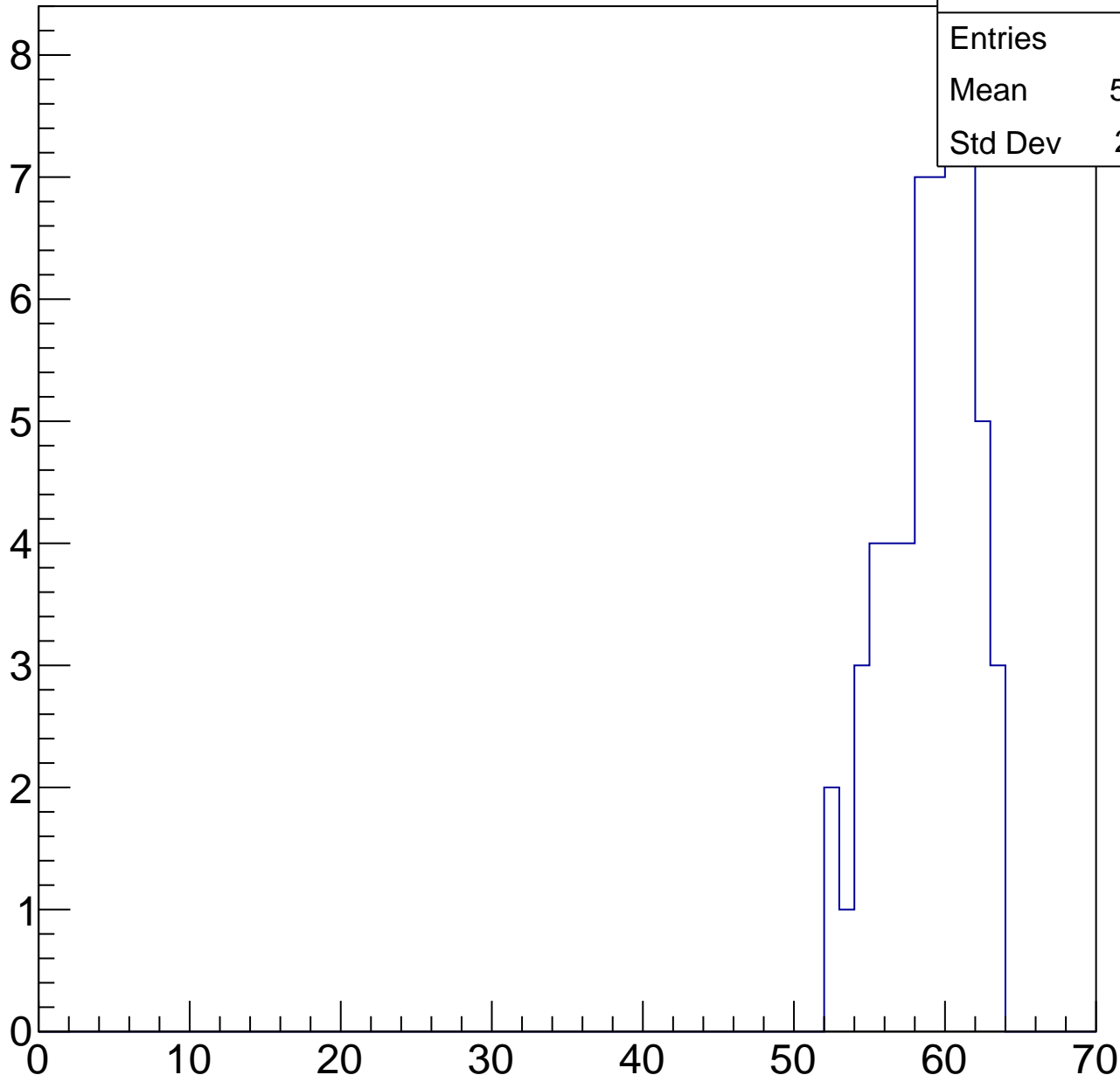
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	56
Mean	58.52
Std Dev	2.841

ampl

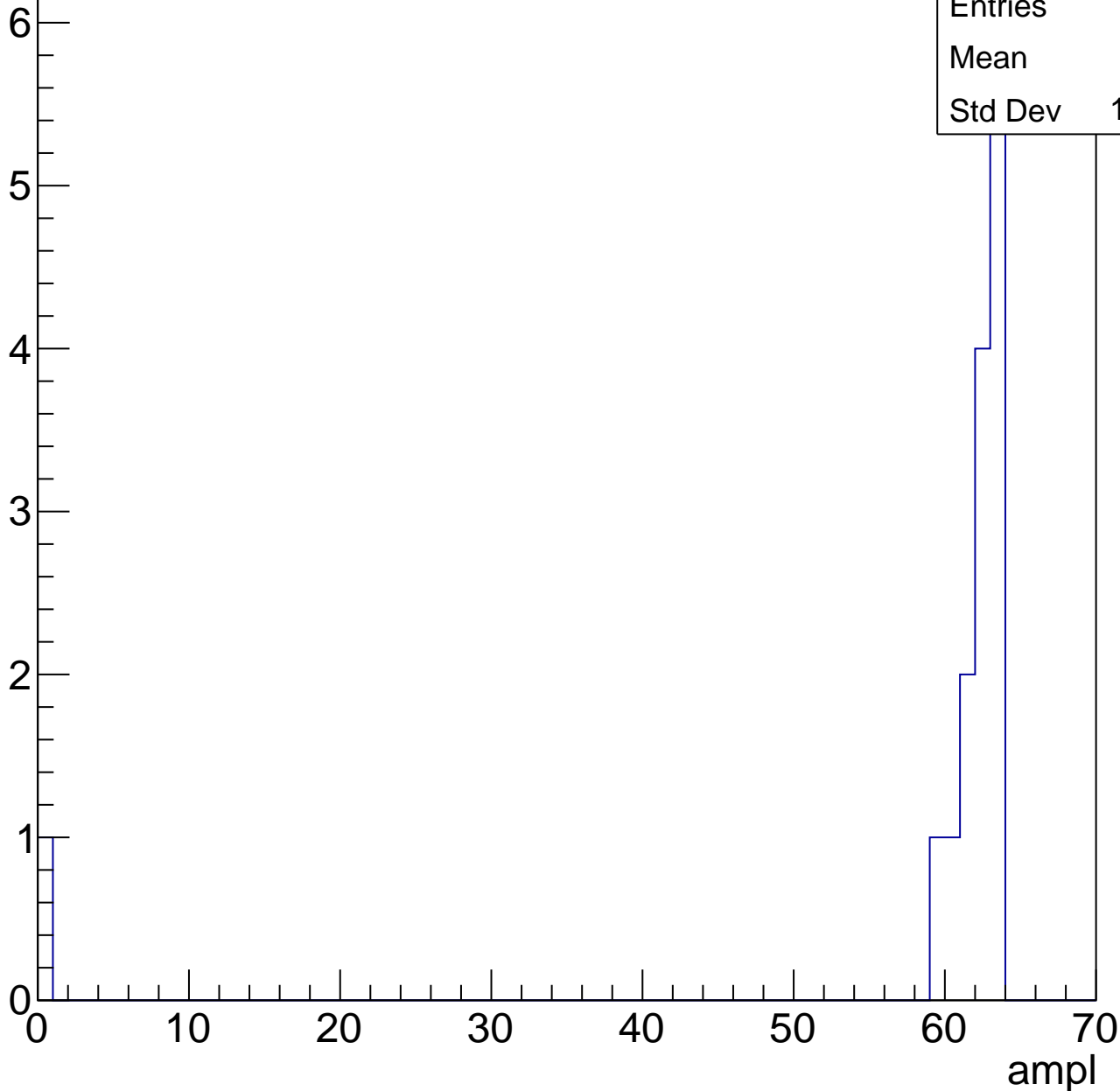


# B1L101S, U3-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	15
Mean	57.8
Std Dev	15.49





# B1L101S, U3-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U3-ch110, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	72
Mean	26.15
Std Dev	5.499

**Gaus mean : 27.2920**

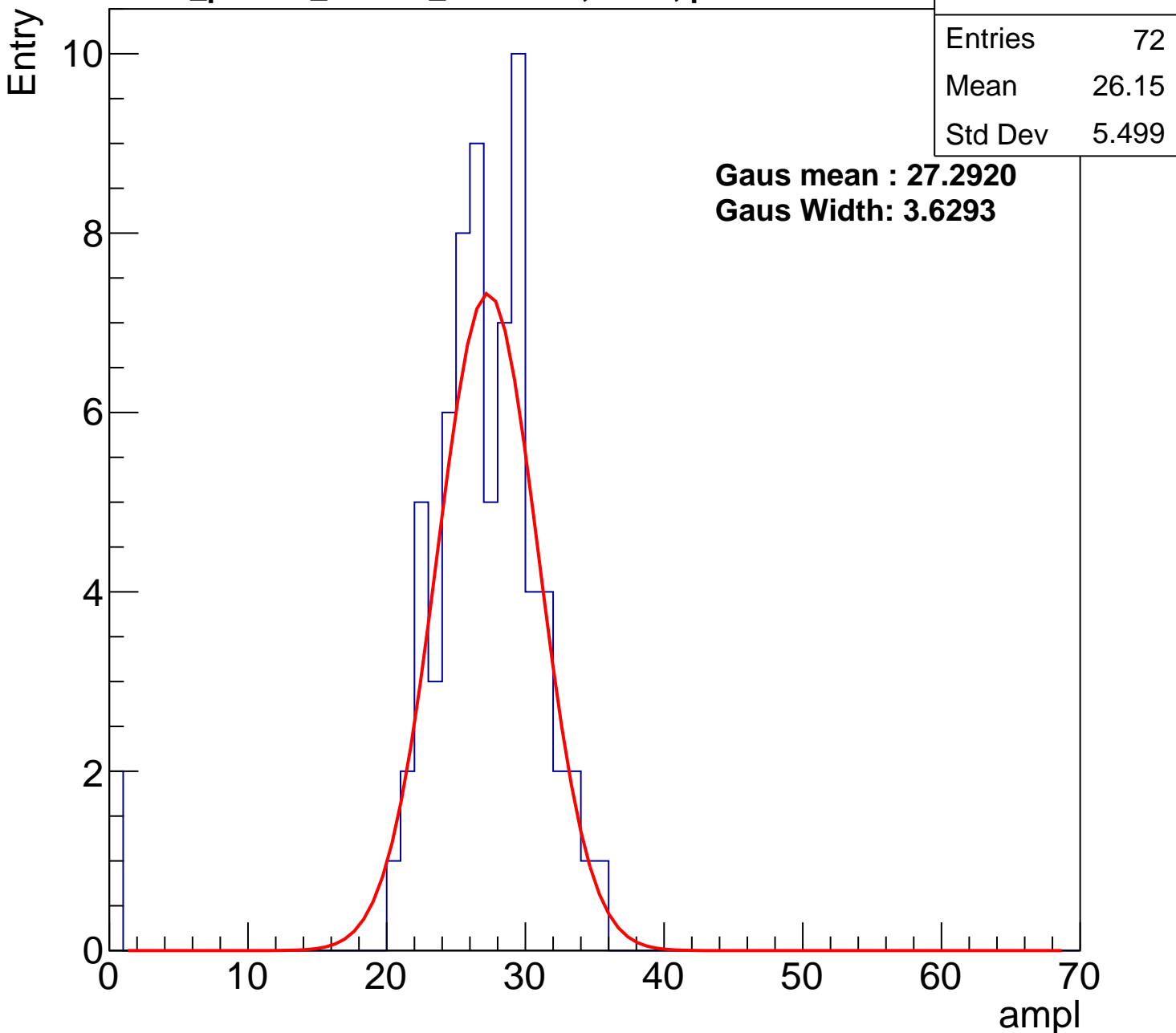
**Gaus Width: 3.6293**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U3-ch110, adc1

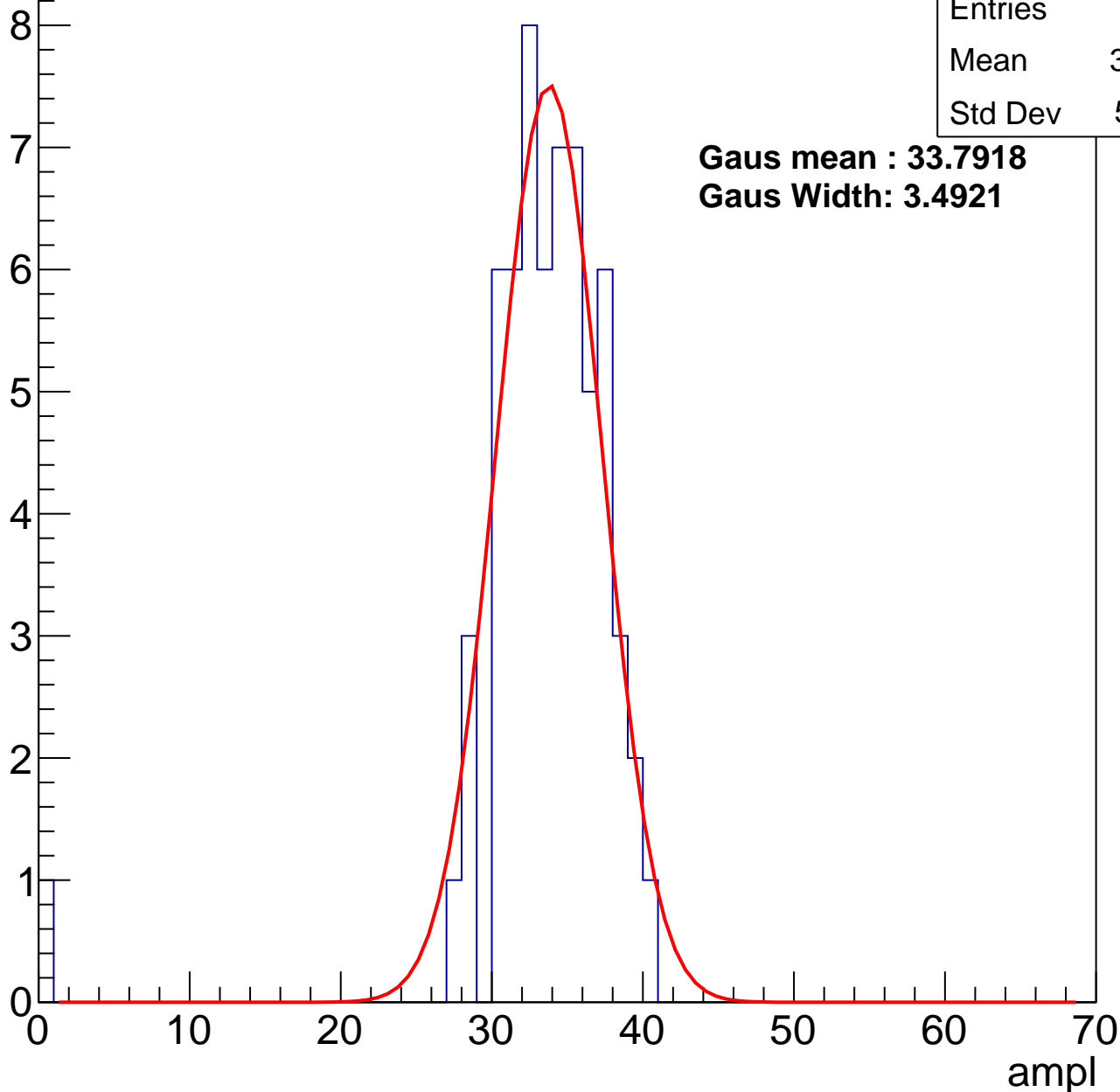
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	33.03
Std Dev	5.171

**Gaus mean : 33.7918**

**Gaus Width: 3.4921**



# B1L101S, U3-ch110, adc2

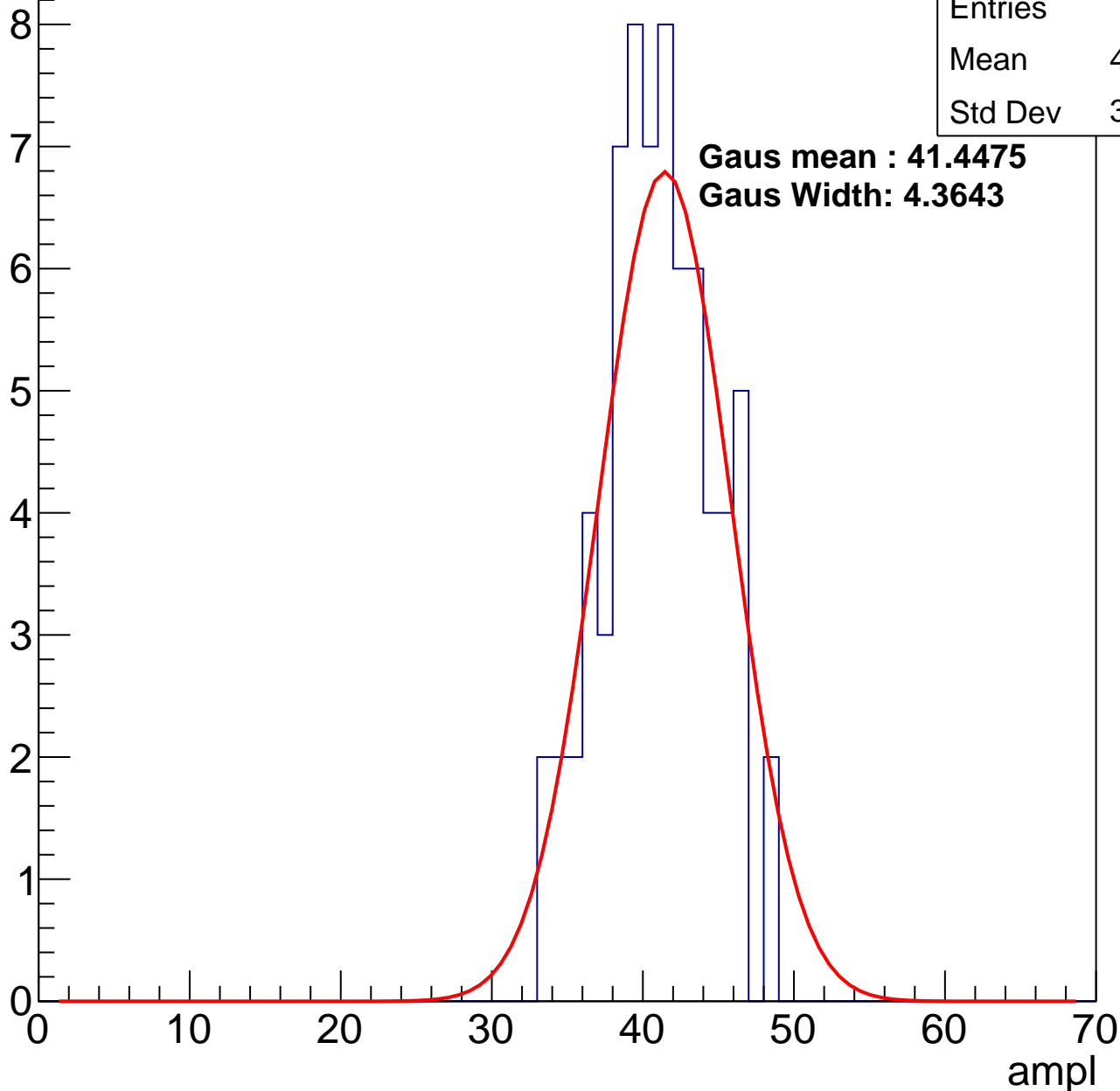
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	40.53
Std Dev	3.557

**Gaus mean : 41.4475**

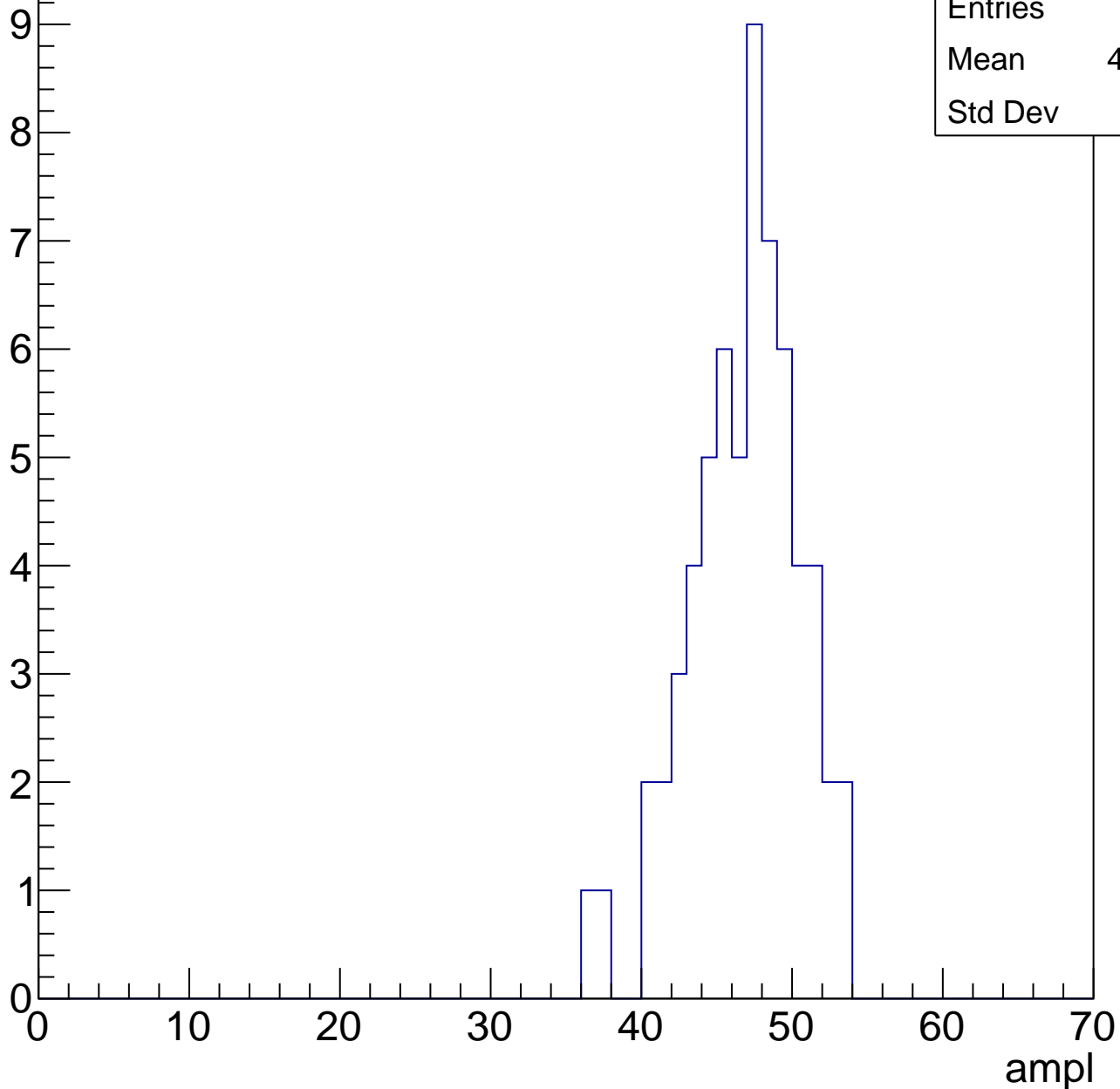
**Gaus Width: 4.3643**



# B1L101S, U3-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

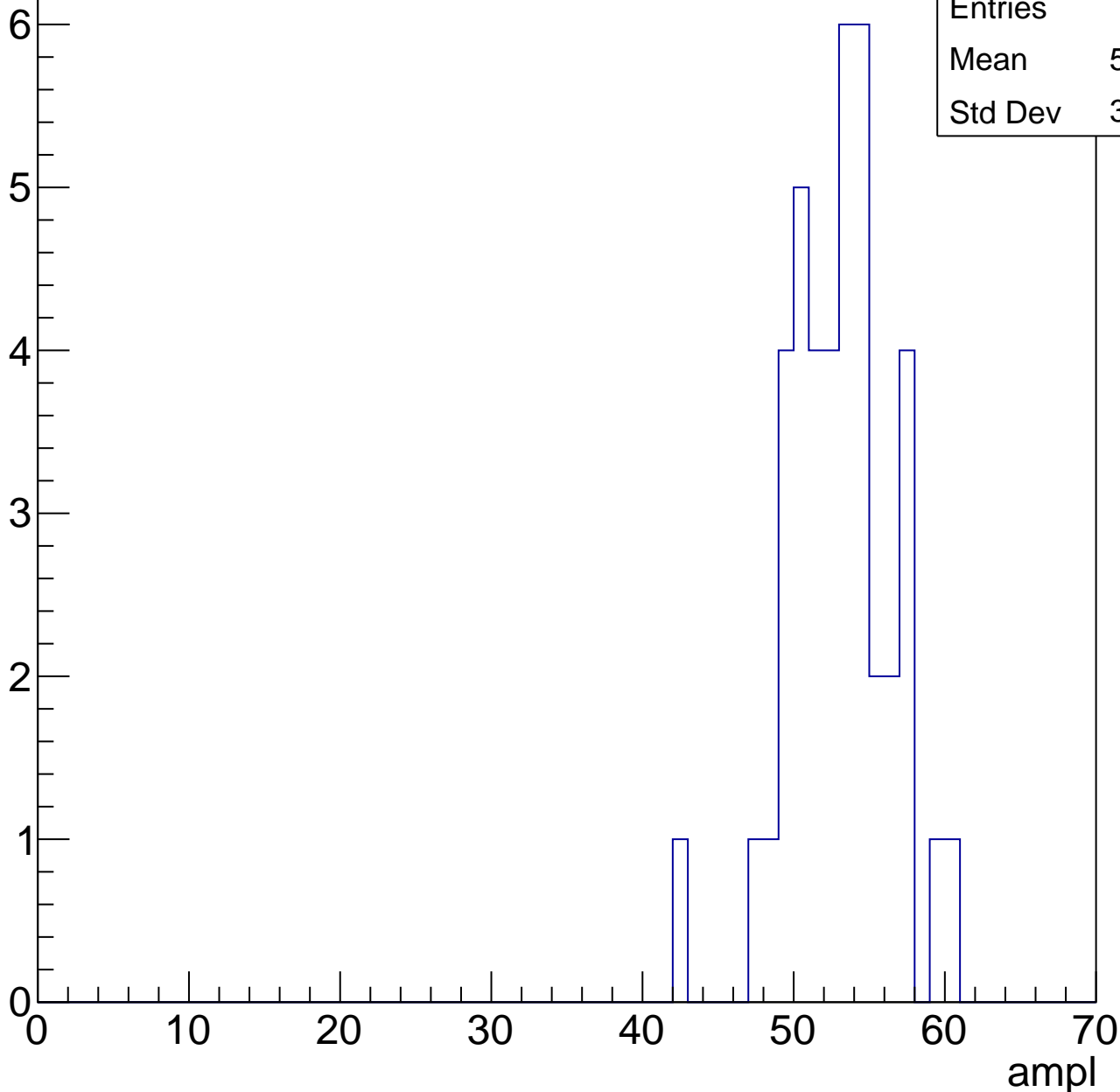


# B1L101S, U3-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	52.52
Std Dev	3.389

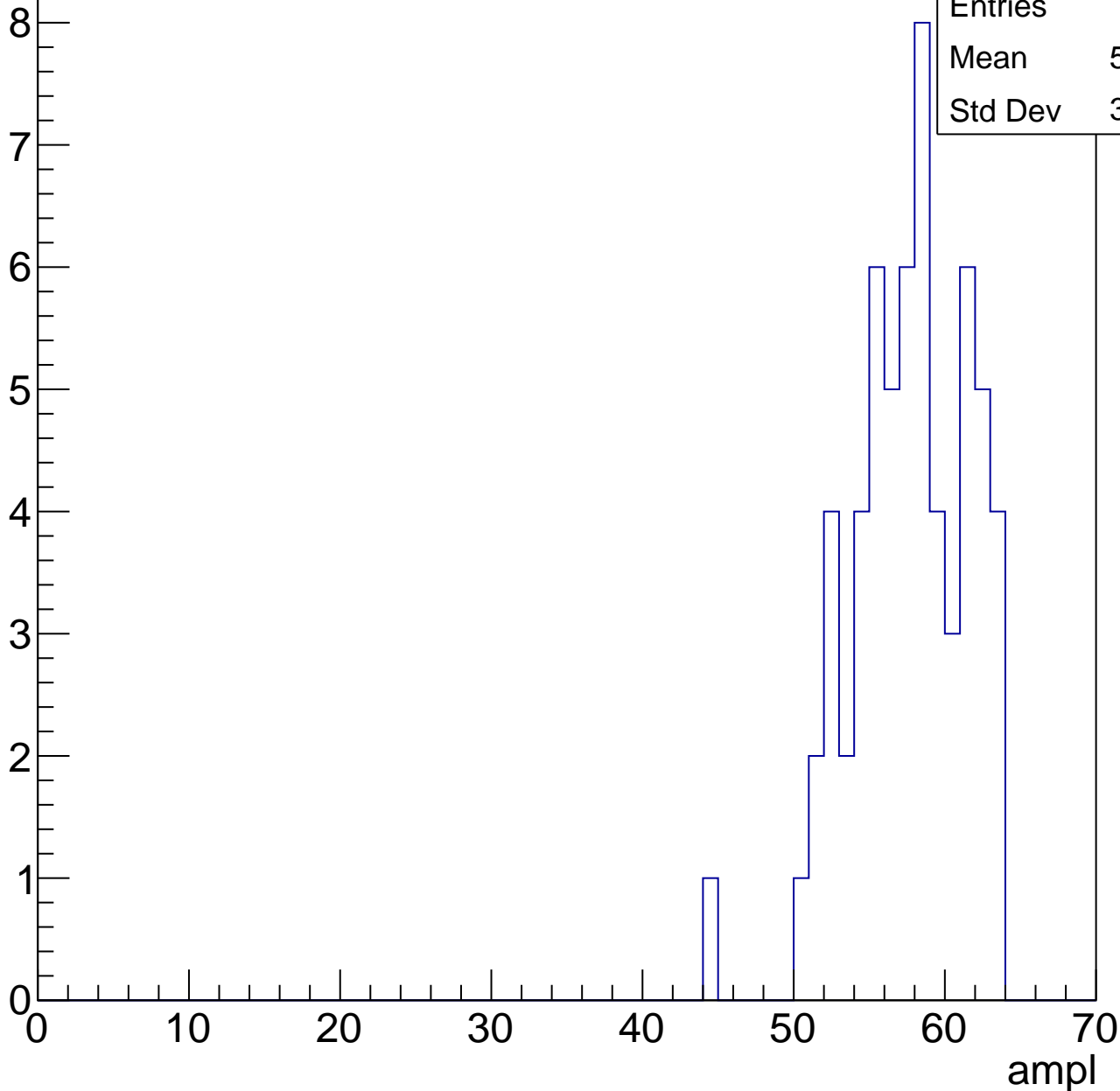


# B1L101S, U3-ch110, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	57.15
Std Dev	3.845



# B1L101S, U3-ch110, adc6

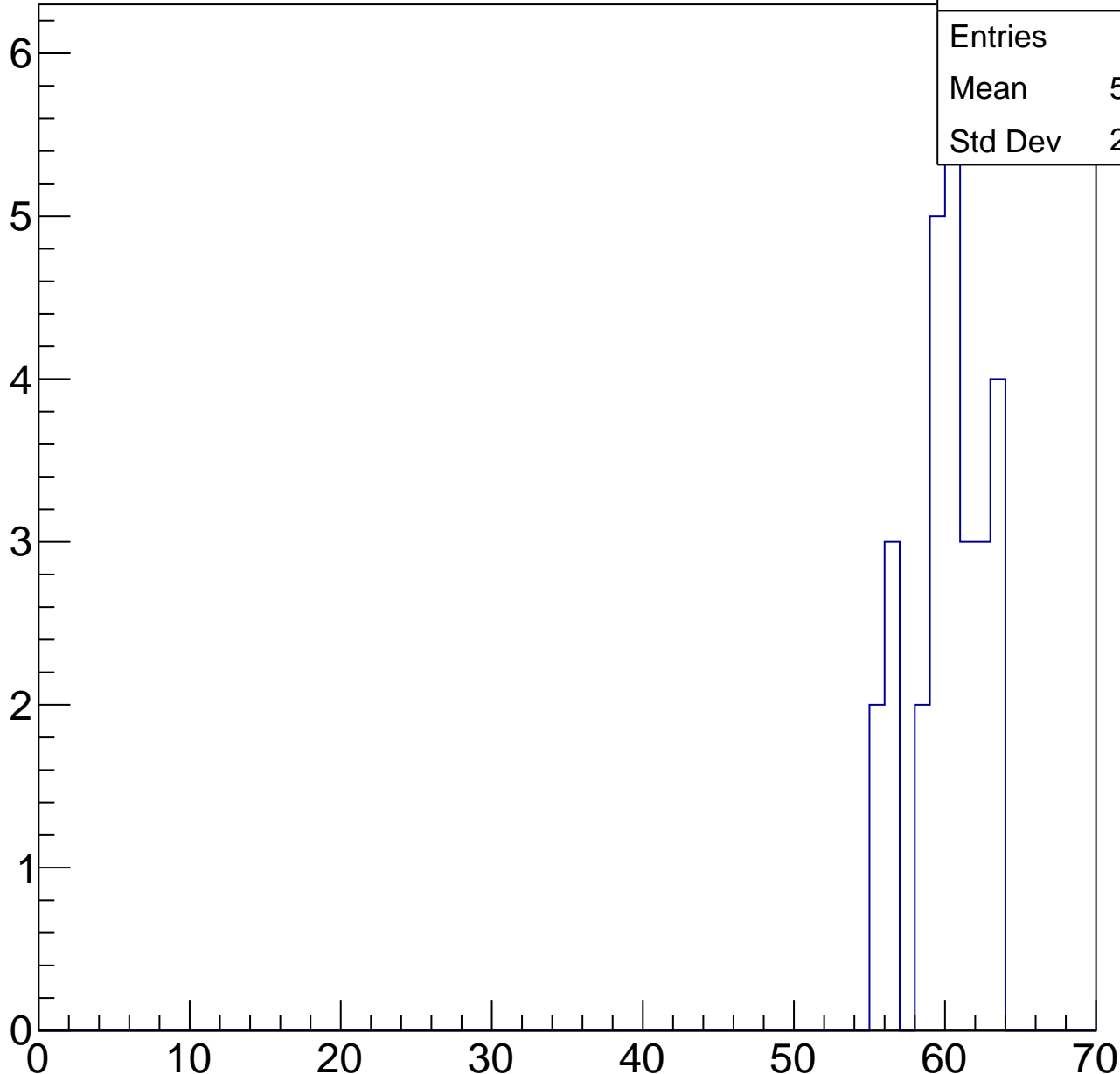
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

6  
5  
4  
3  
2  
1  
0

Entries	28
Mean	59.64
Std Dev	2.379

ampl

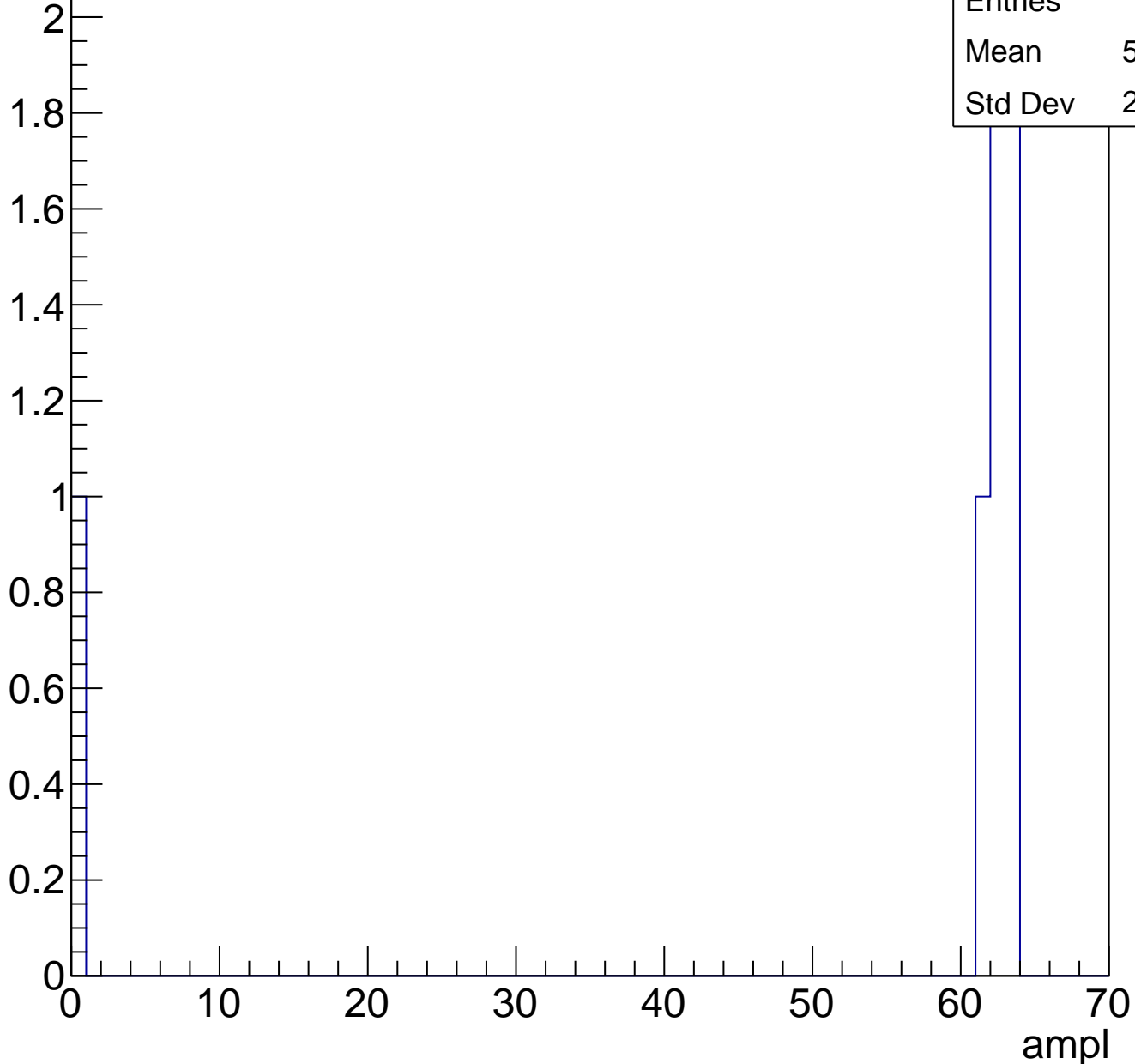




# B1L101S, U3-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch111, adc0

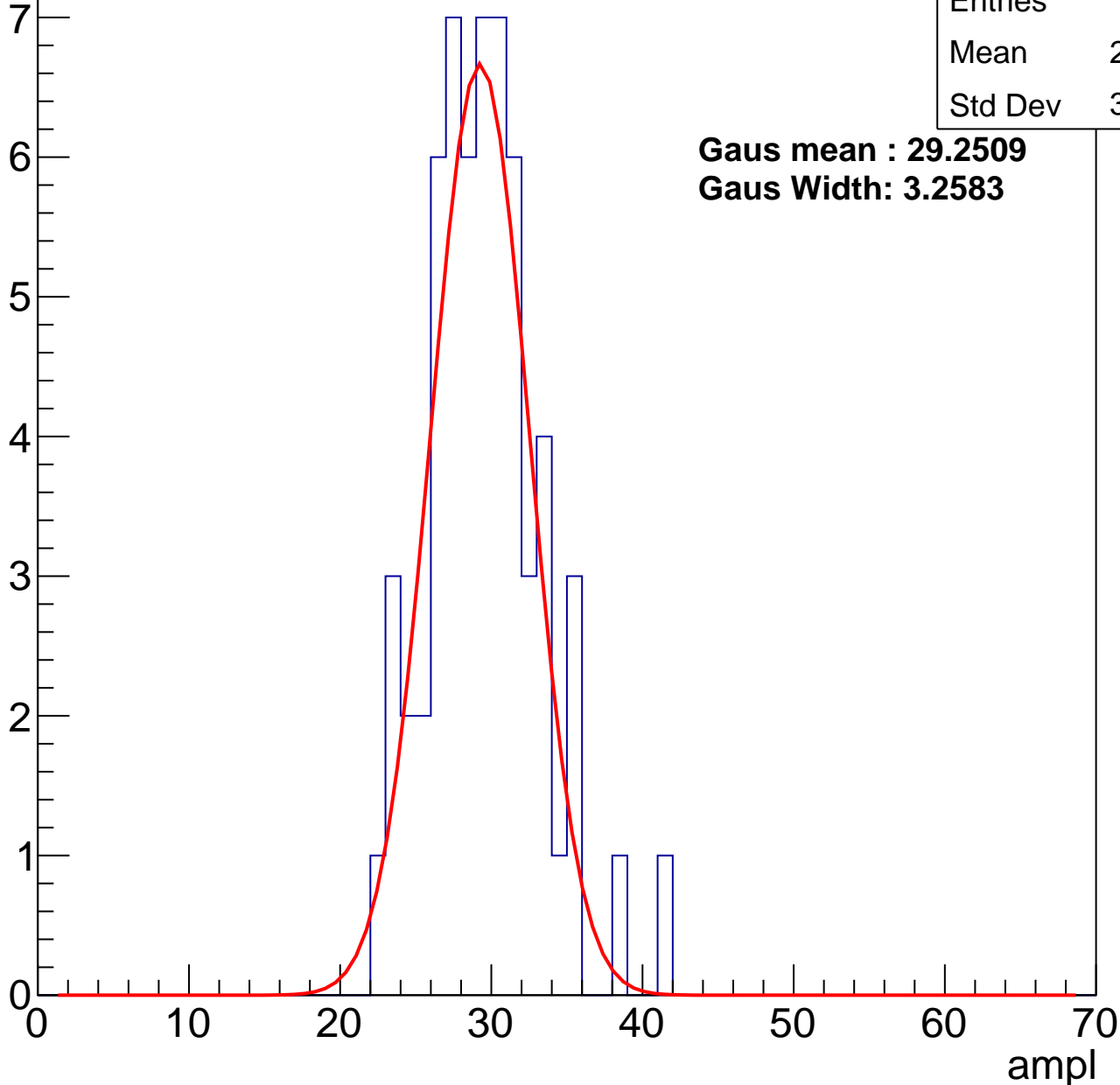
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	29.12
Std Dev	3.666

**Gaus mean : 29.2509**

**Gaus Width: 3.2583**



# B1L101S, U3-ch111, adc1

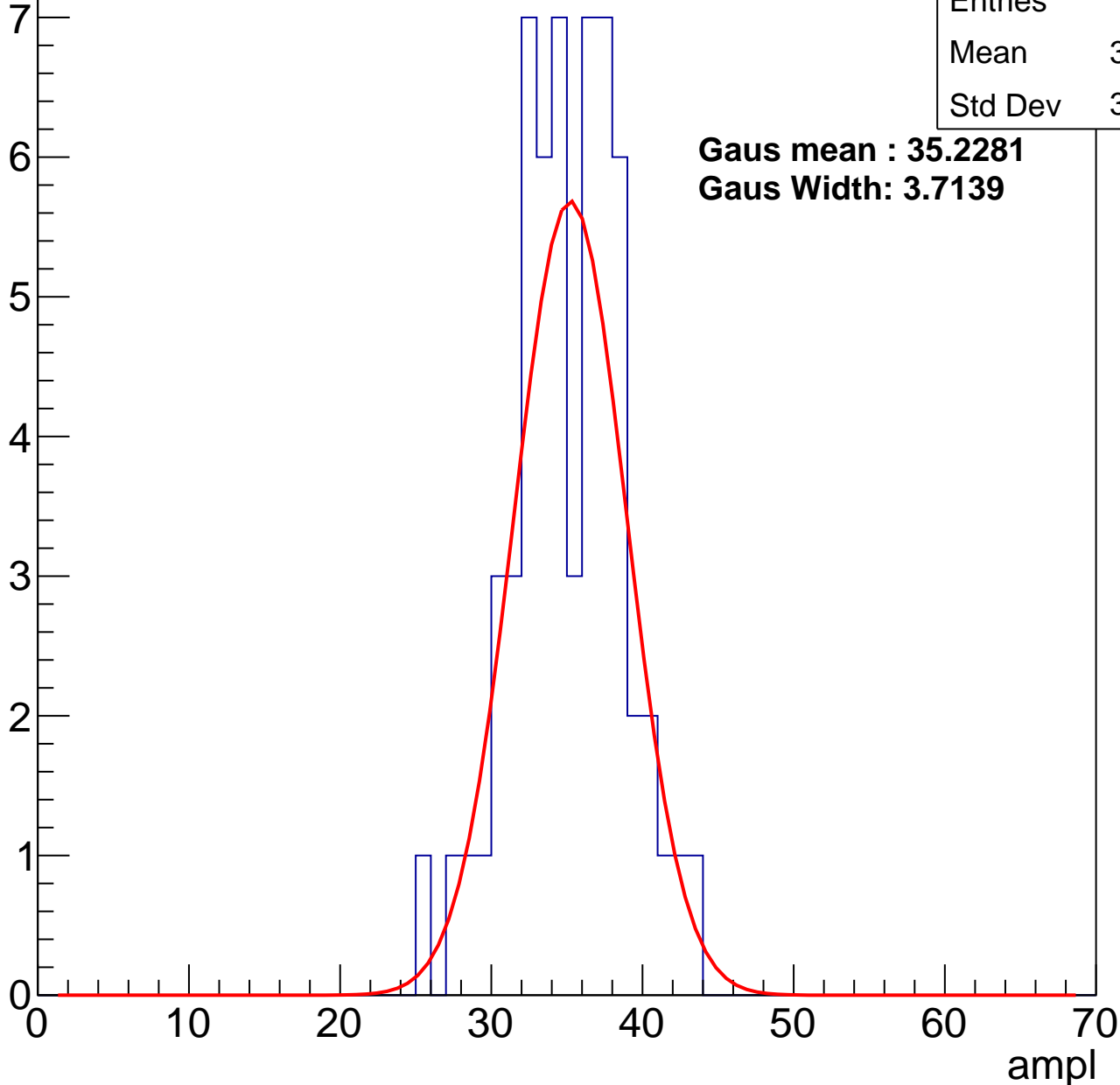
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	60
Mean	34.67
Std Dev	3.604

**Gaus mean : 35.2281**

**Gaus Width: 3.7139**



# B1L101S, U3-ch111, adc2

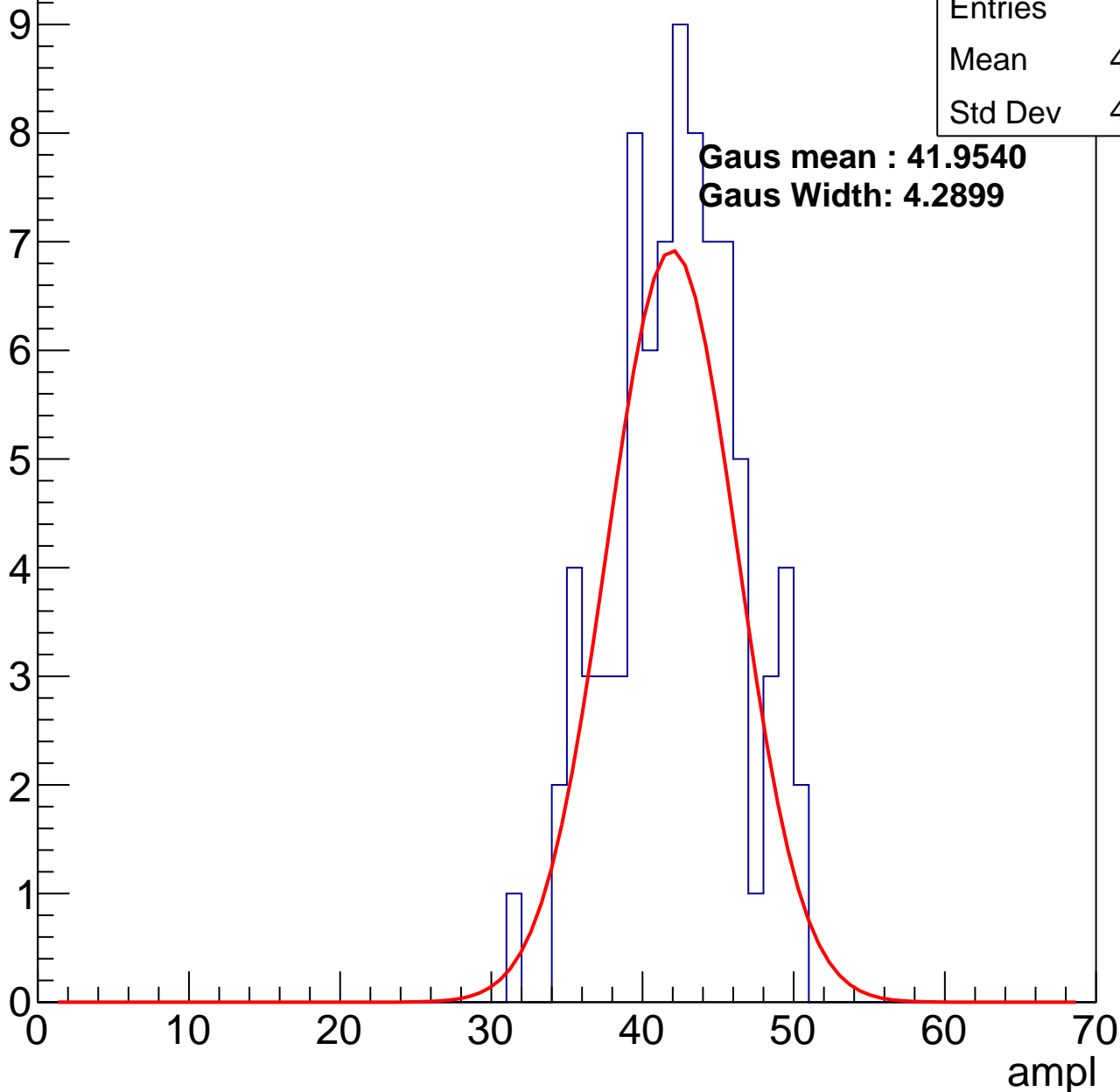
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	83
Mean	41.84
Std Dev	4.126

**Gaus mean : 41.9540**

**Gaus Width: 4.2899**

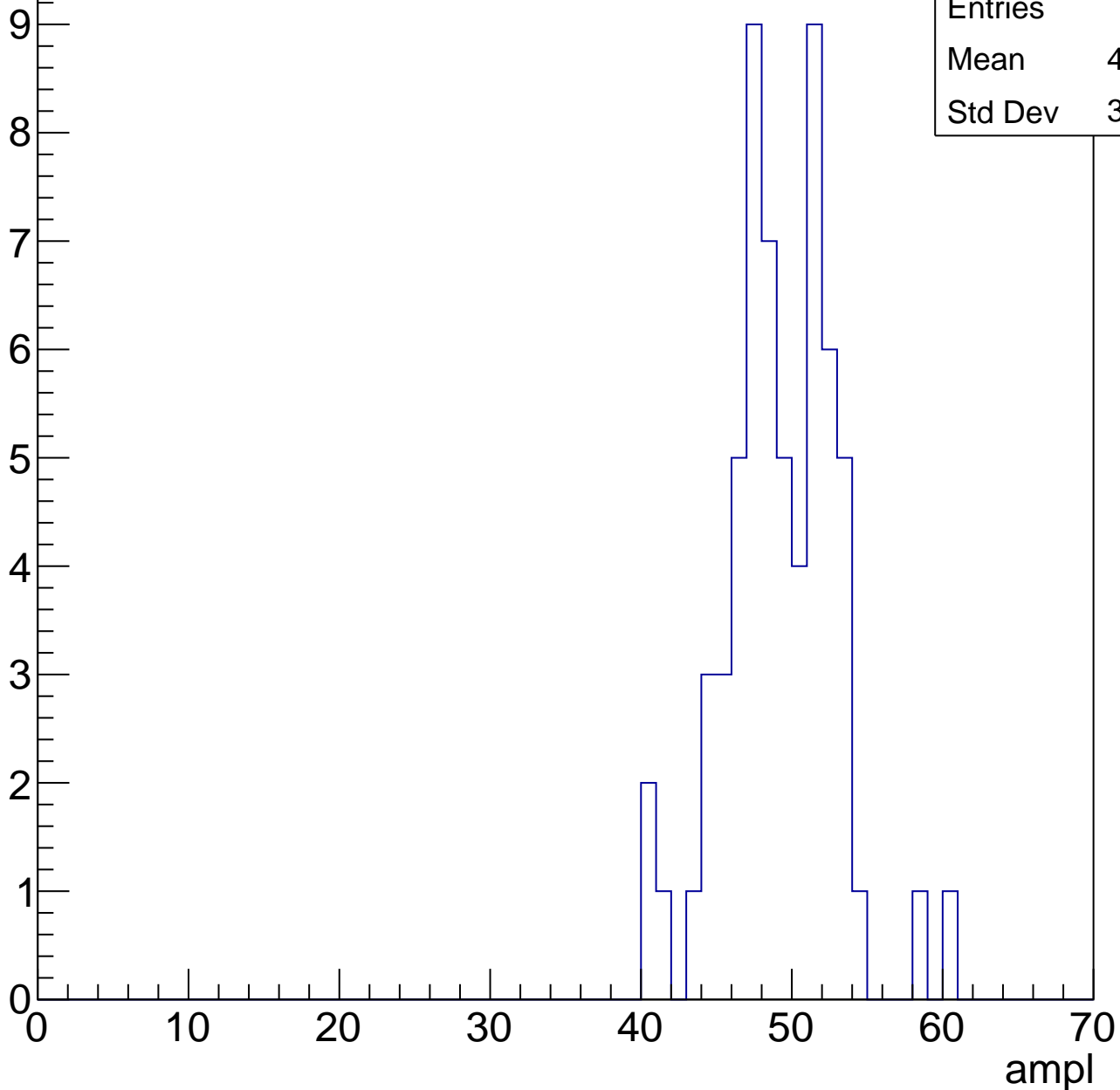


# B1L101S, U3-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	48.78
Std Dev	3.718

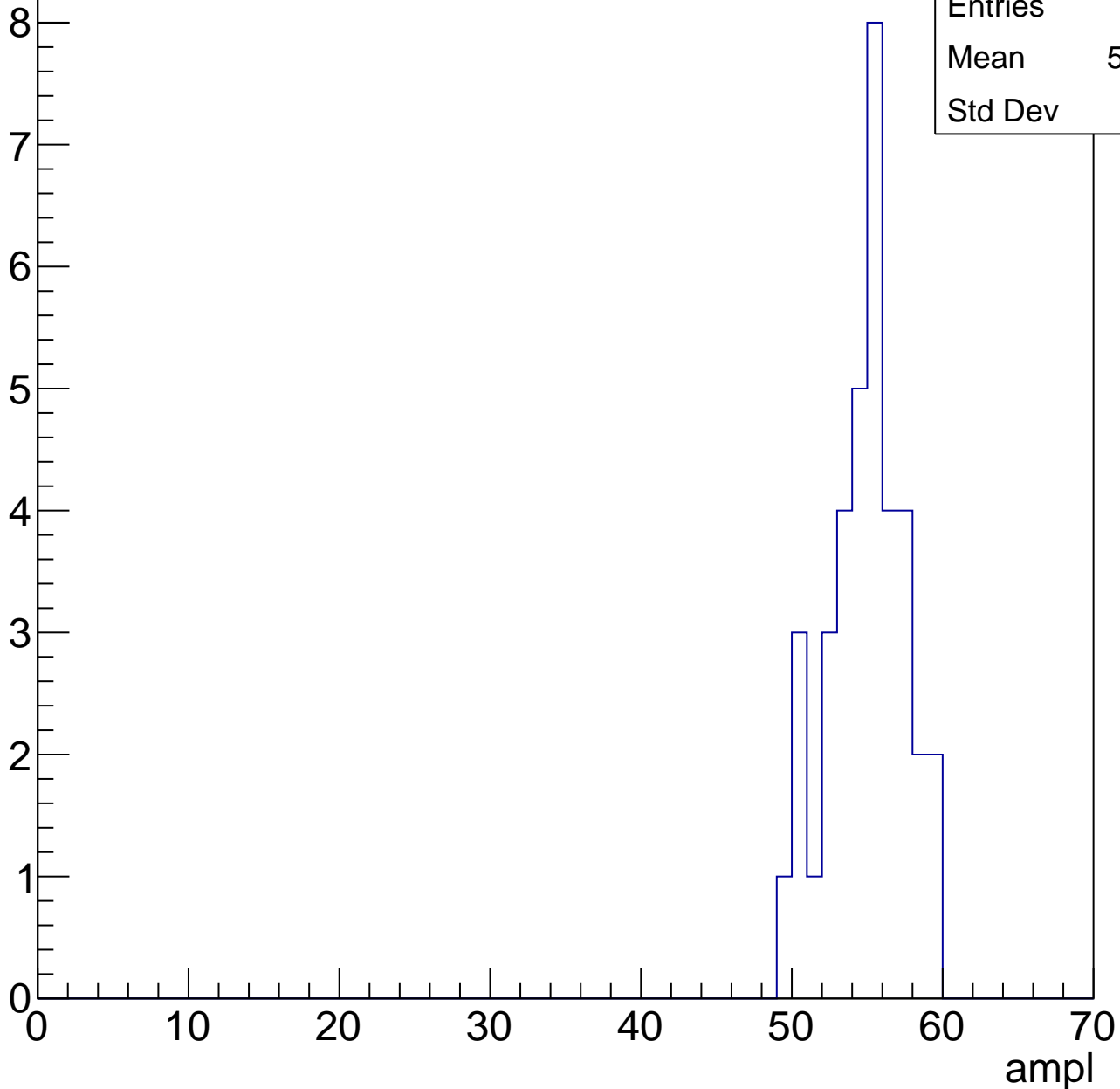


# B1L101S, U3-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	37
Mean	54.43
Std Dev	2.51



# B1L101S, U3-ch111, adc5

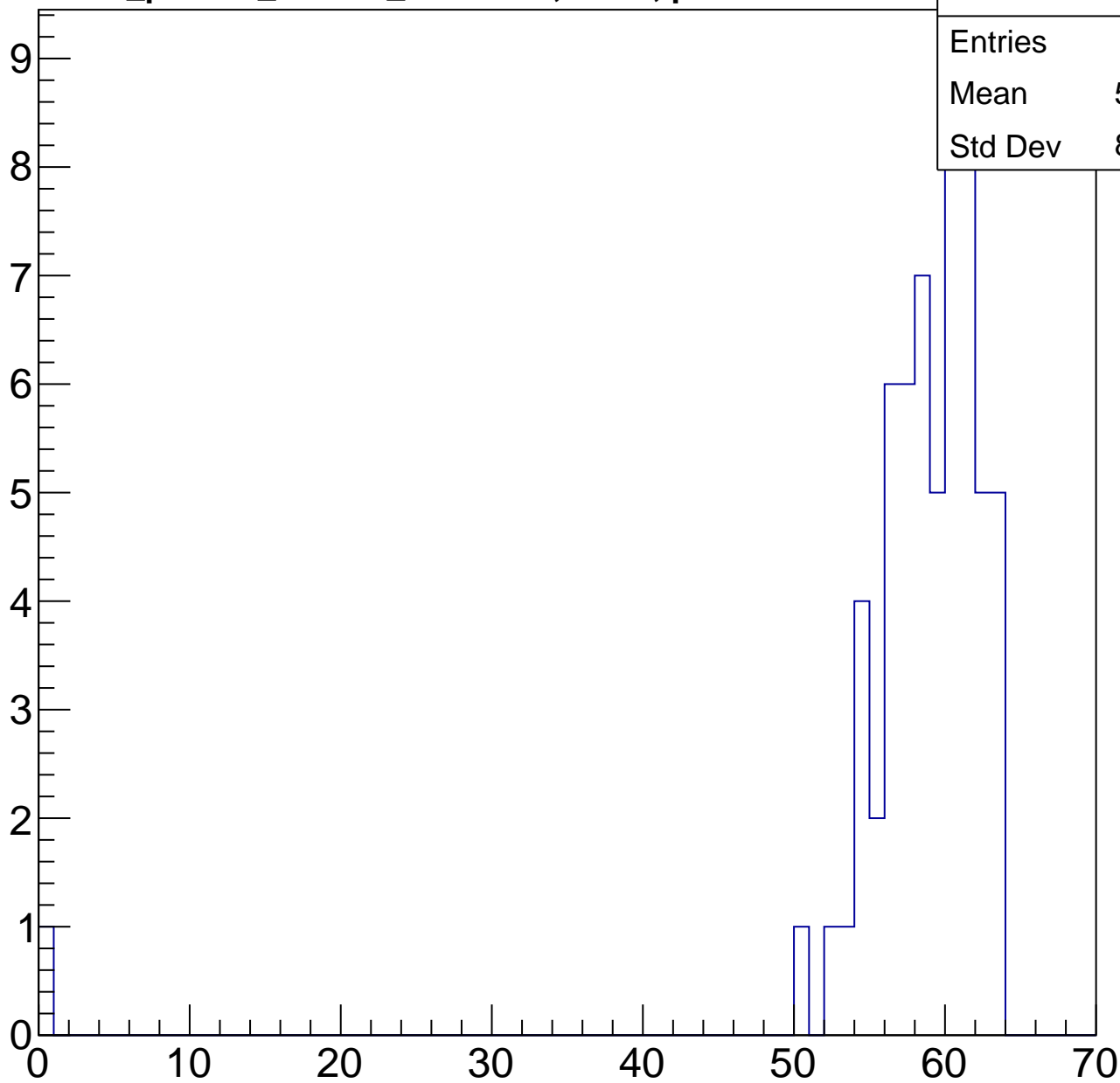
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	61
Mean	57.61
Std Dev	8.011

ampl

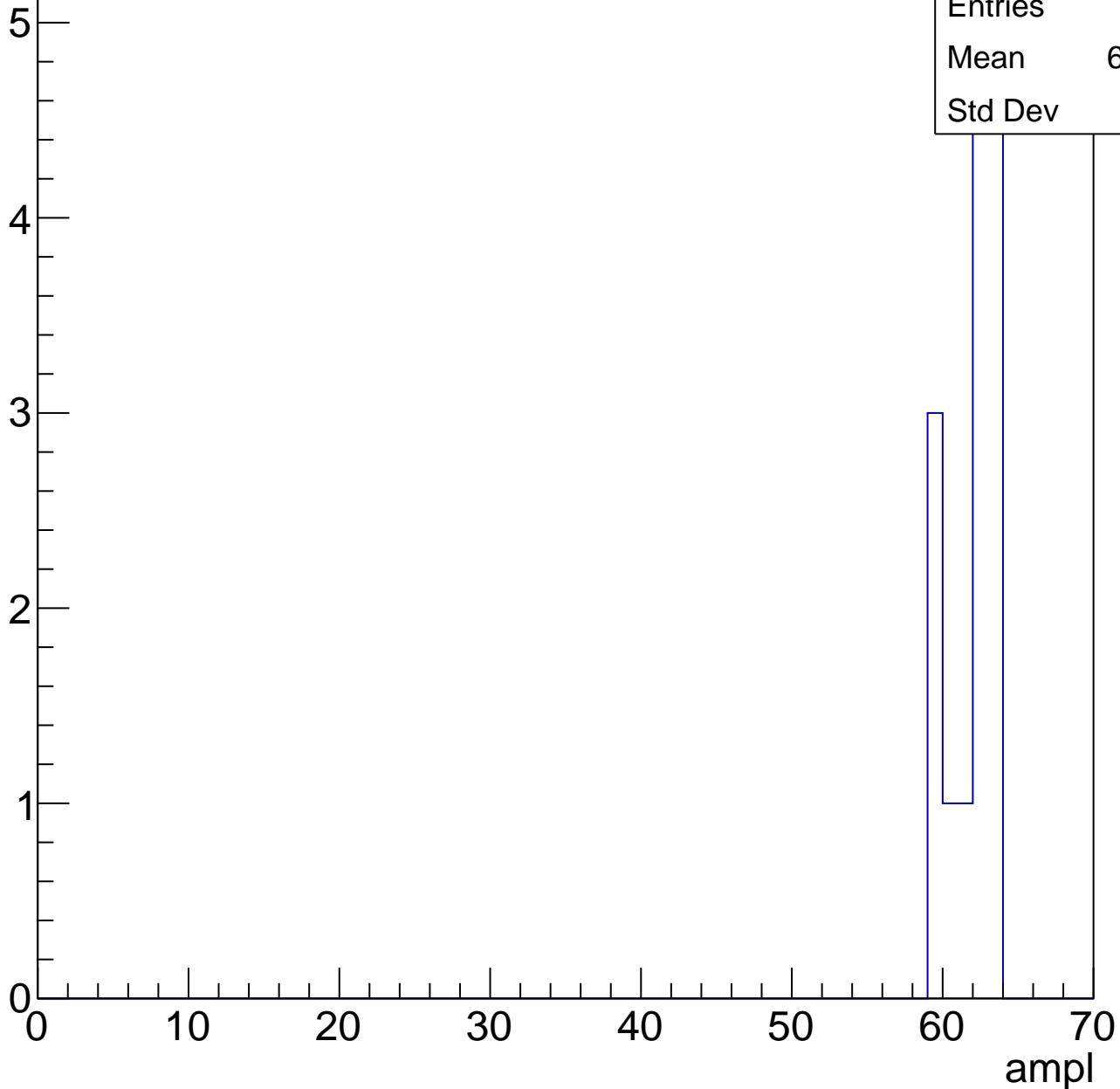


# B1L101S, U3-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	15
Mean	61.53
Std Dev	1.5





# B1L101S, U3-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch112, adc0

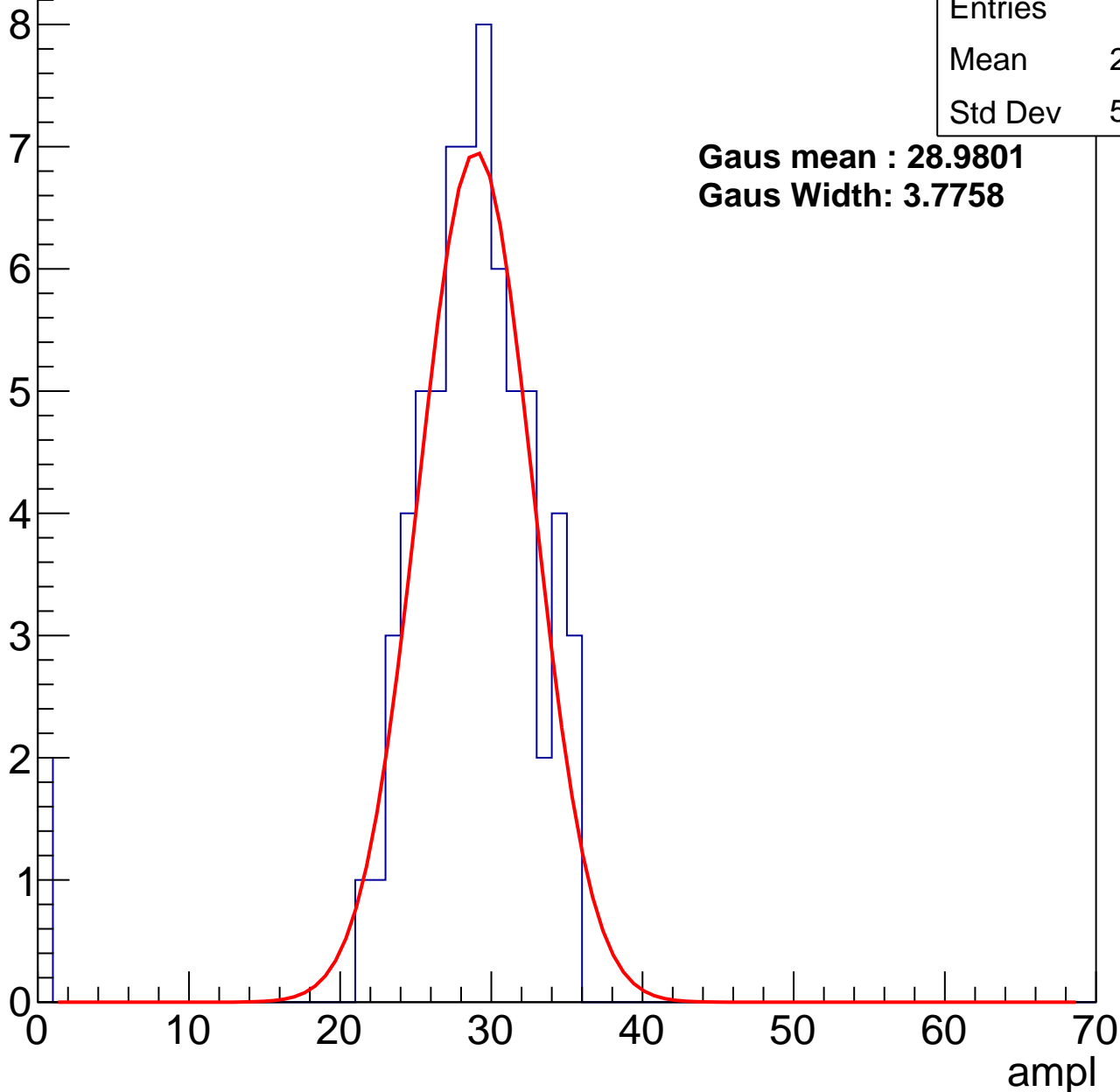
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	27.68
Std Dev	5.885

**Gaus mean : 28.9801**

**Gaus Width: 3.7758**



# B1L101S, U3-ch112, adc1

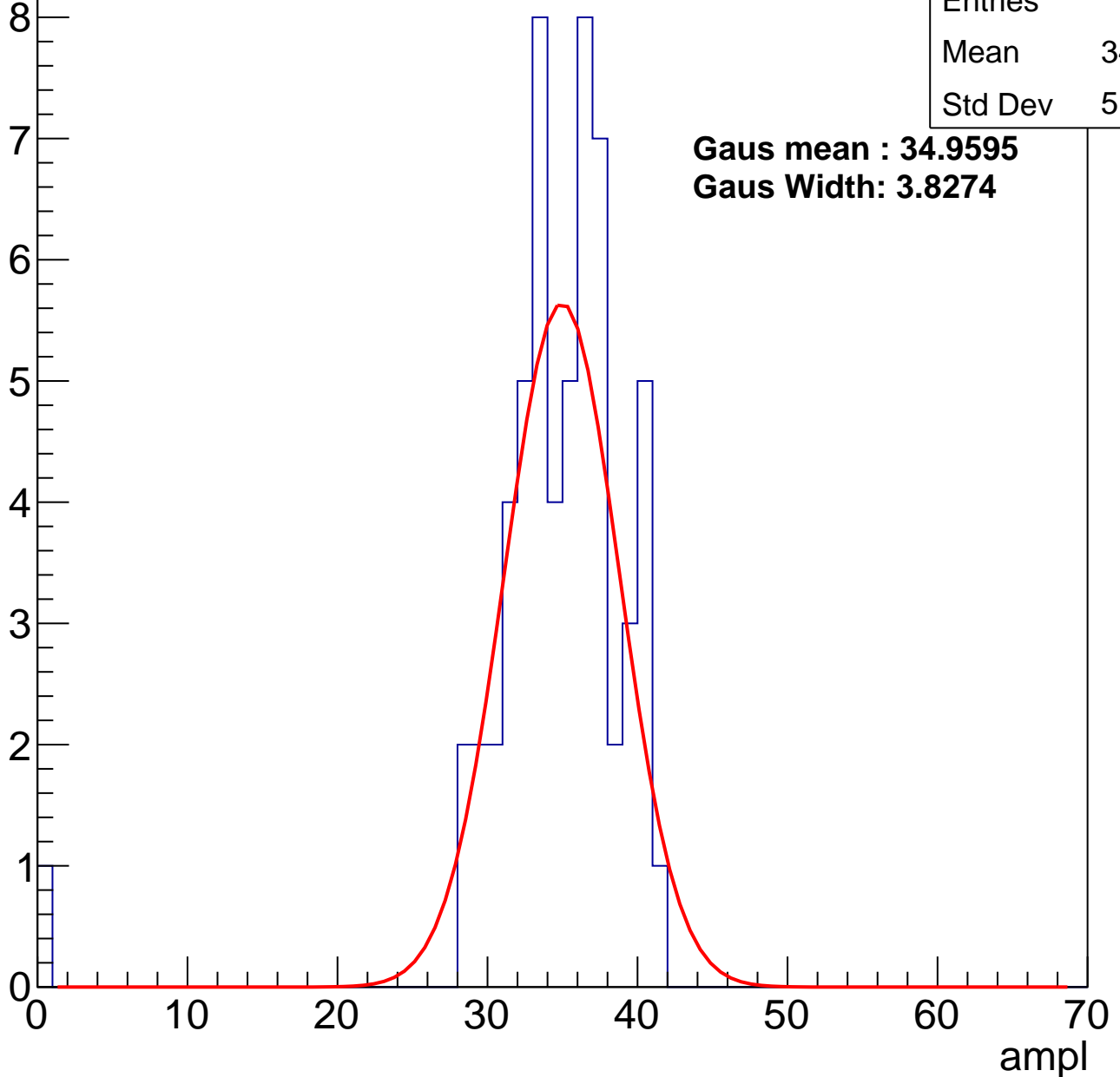
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	34.14
Std Dev	5.537

**Gaus mean : 34.9595**

**Gaus Width: 3.8274**



# B1L101S, U3-ch112, adc2

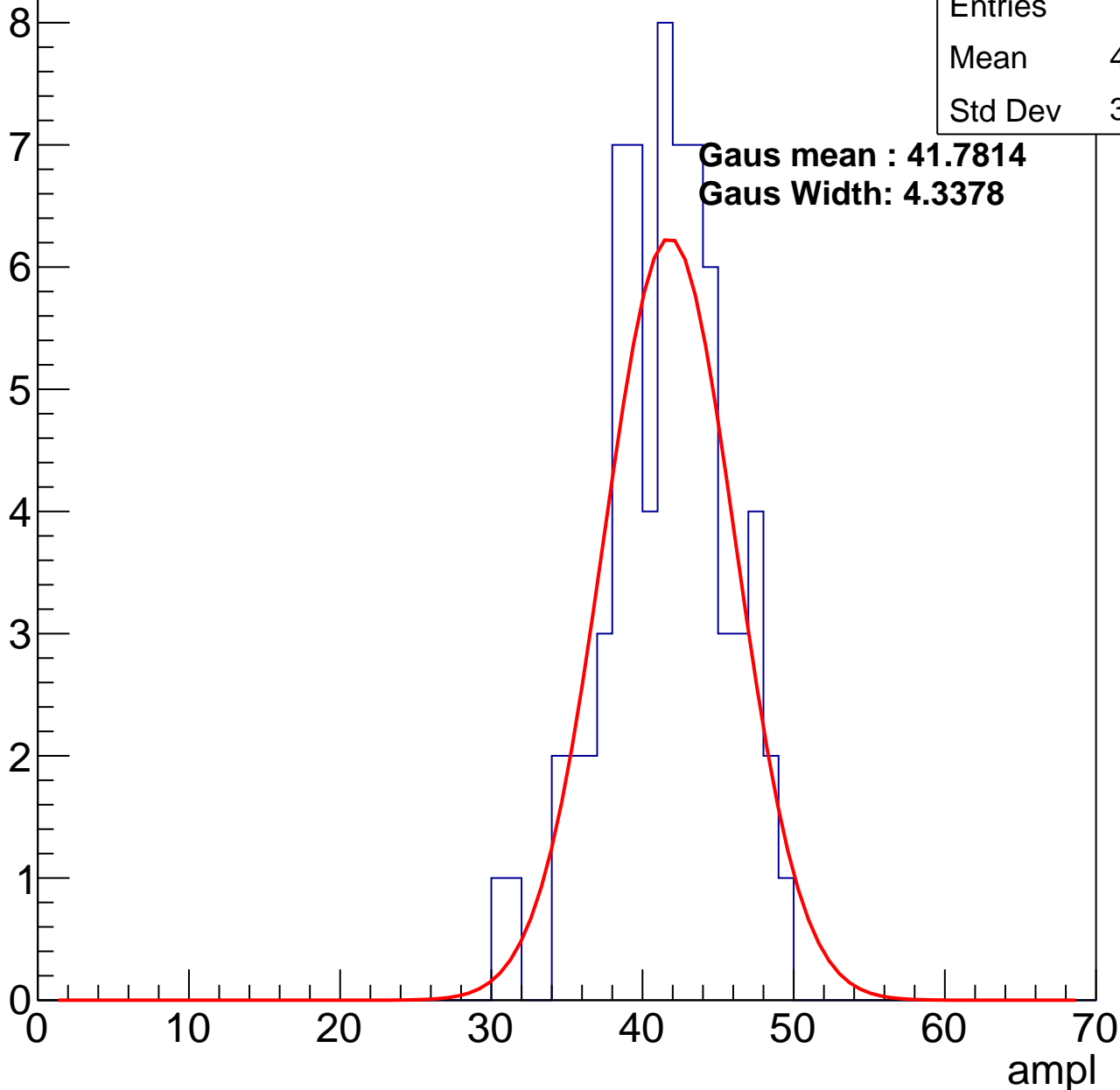
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	41.06
Std Dev	3.967

**Gaus mean : 41.7814**

**Gaus Width: 4.3378**

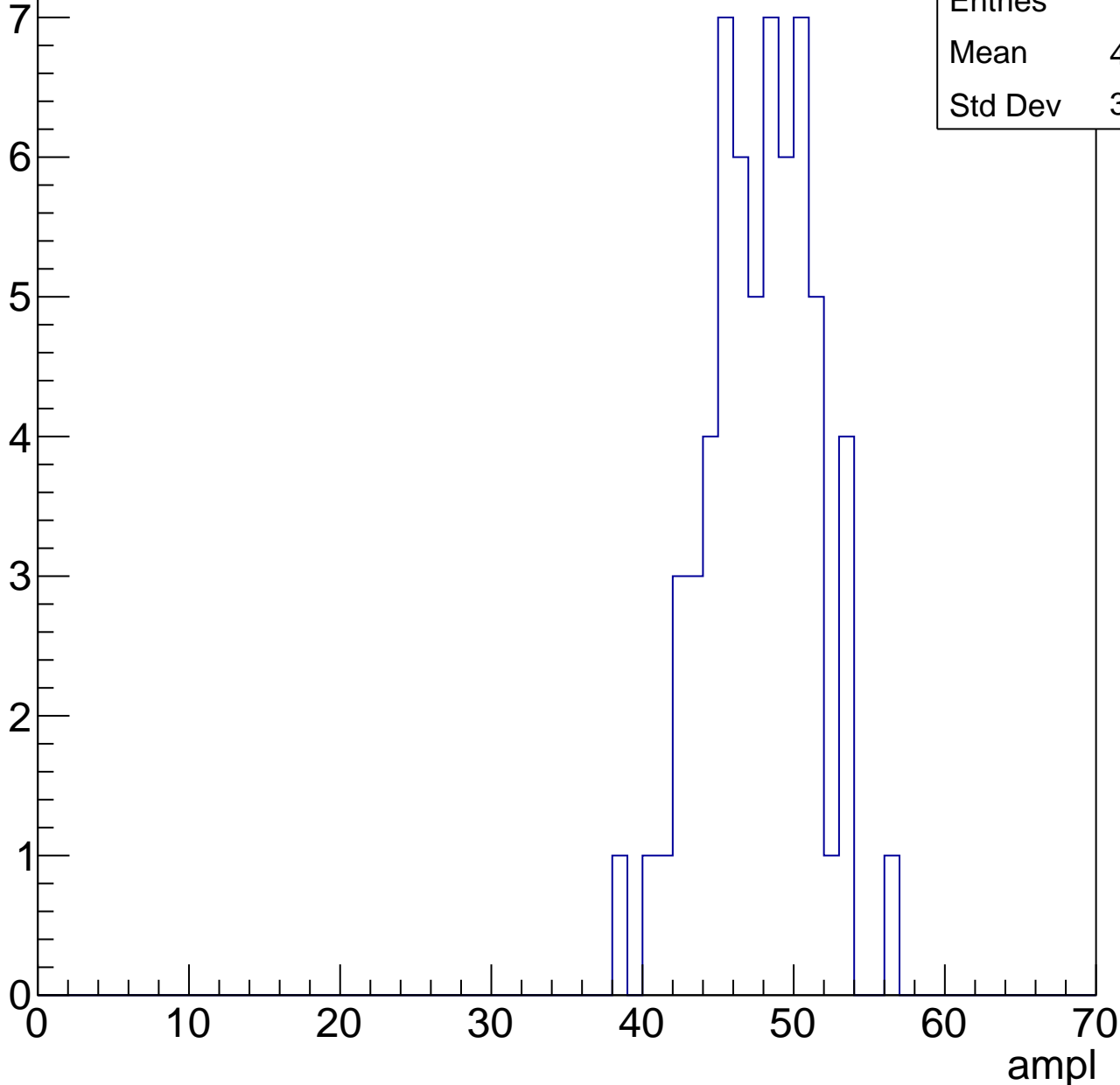


# B1L101S, U3-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	47.27
Std Dev	3.543

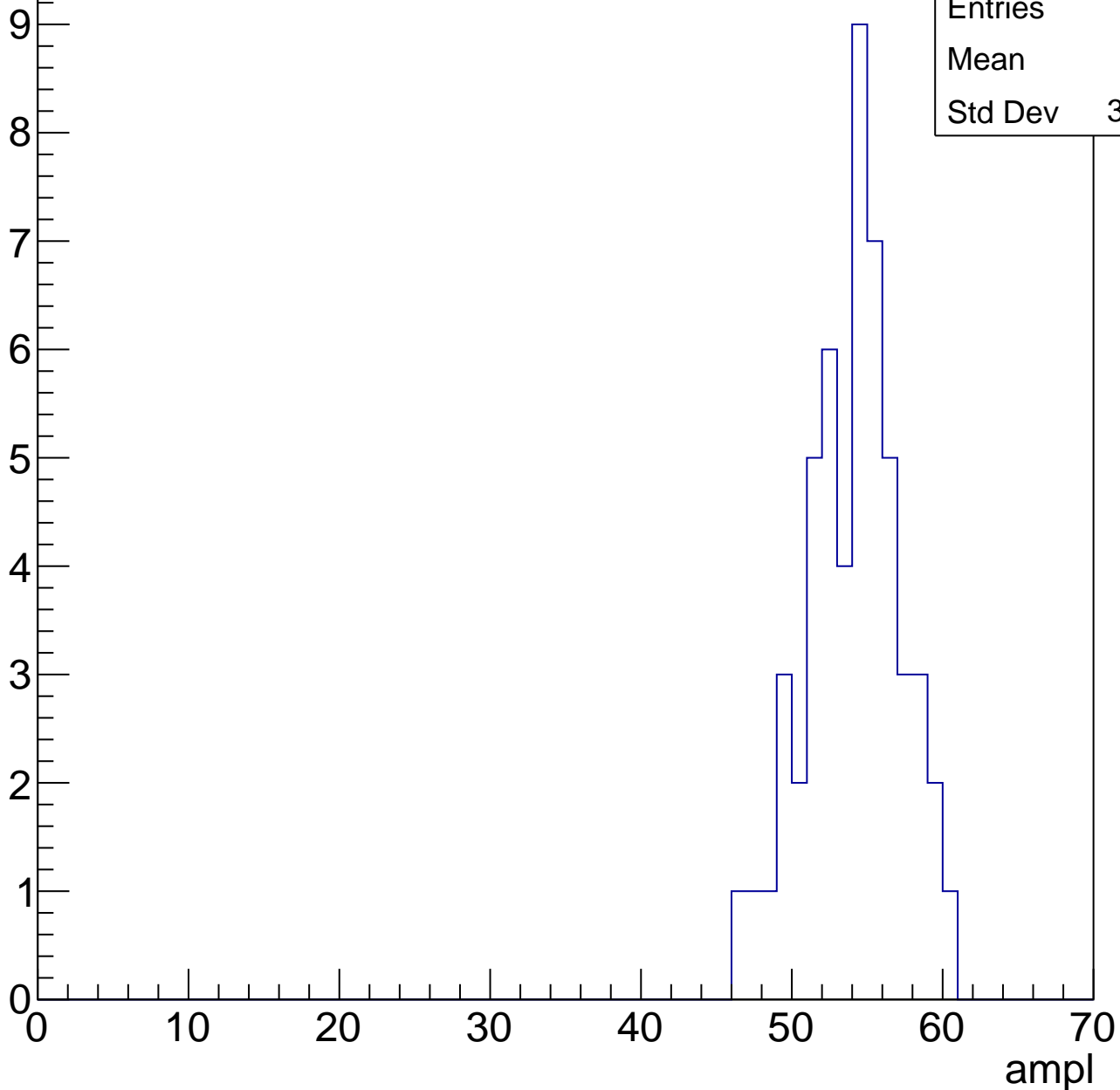


# B1L101S, U3-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	53
Mean	53.6
Std Dev	3.098

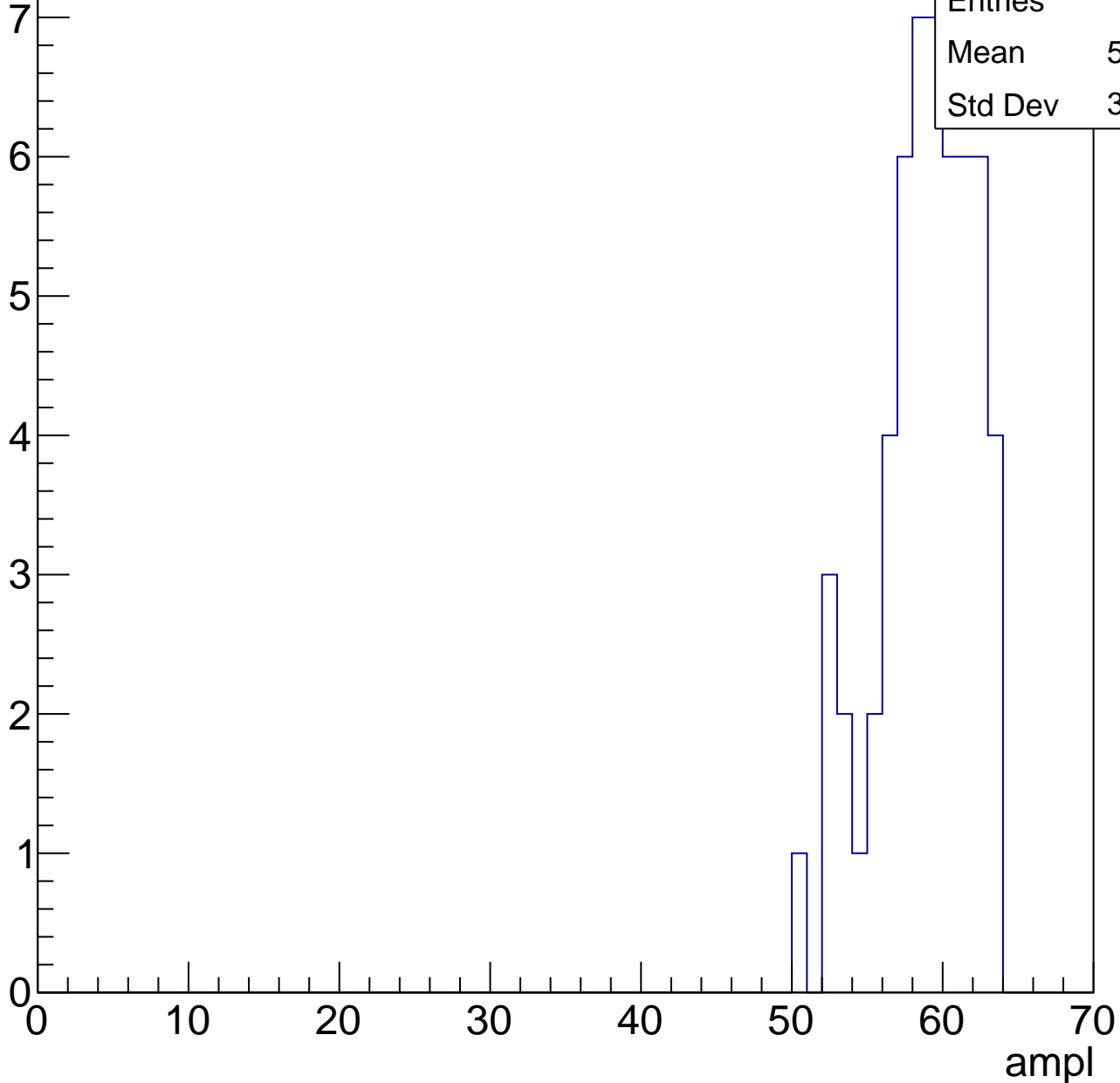


# B1L101S, U3-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

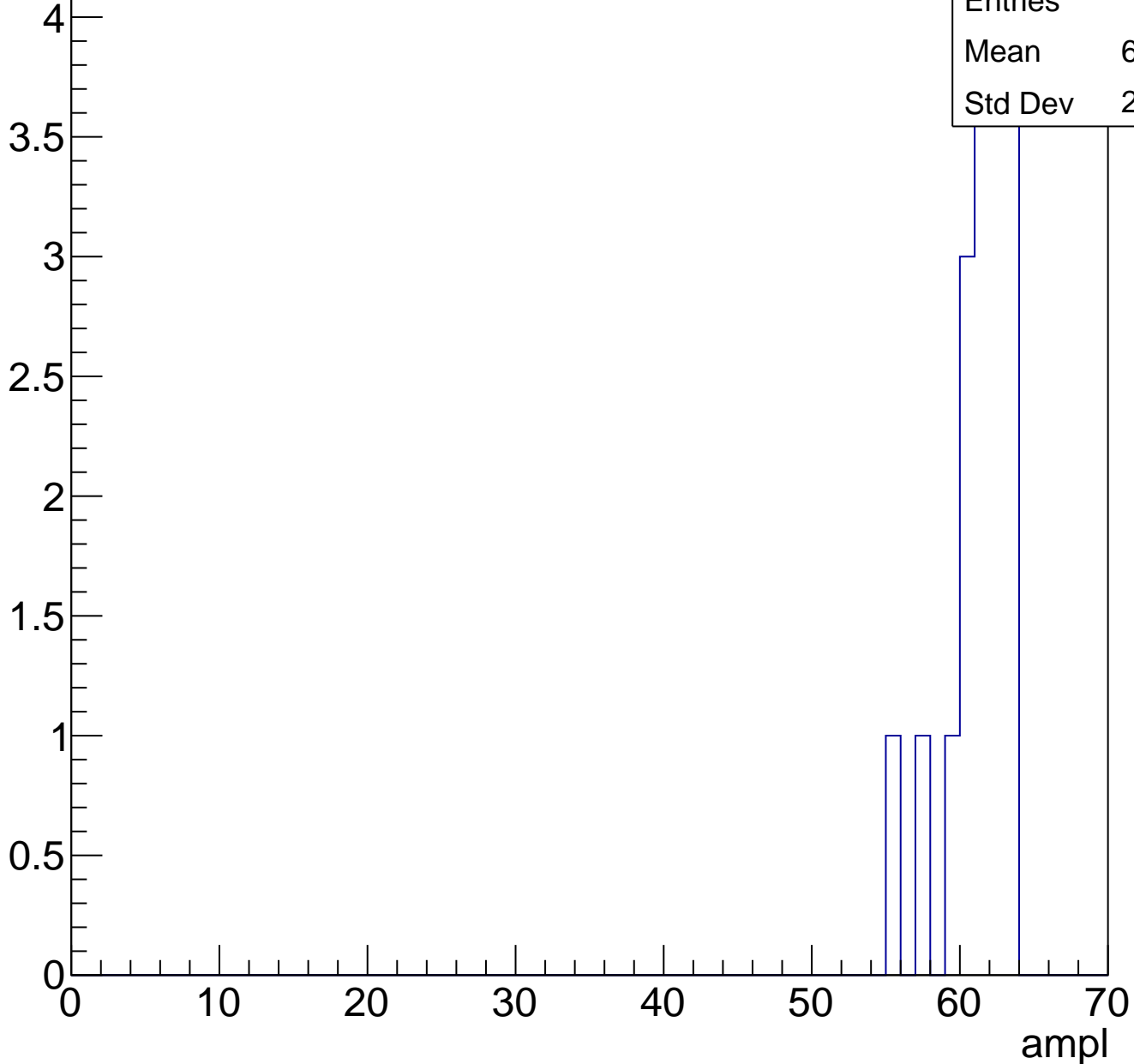
Entries	55
Mean	58.38
Std Dev	3.165



# B1L101S, U3-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	18
Mean	60.83
Std Dev	2.088



# B1L101S, U3-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch113, adc0

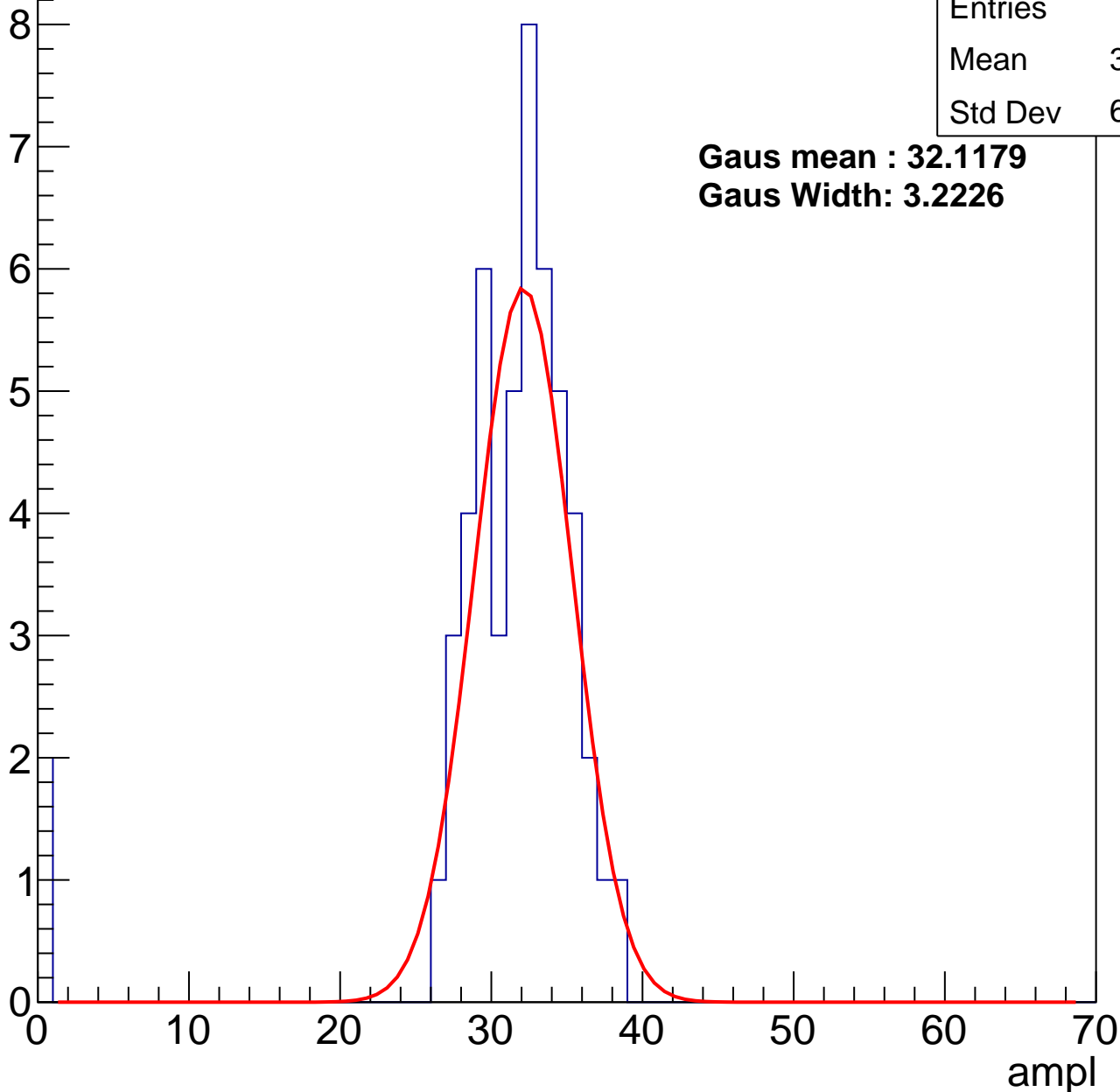
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	30.37
Std Dev	6.736

**Gaus mean : 32.1179**

**Gaus Width: 3.2226**



# B1L101S, U3-ch113, adc1

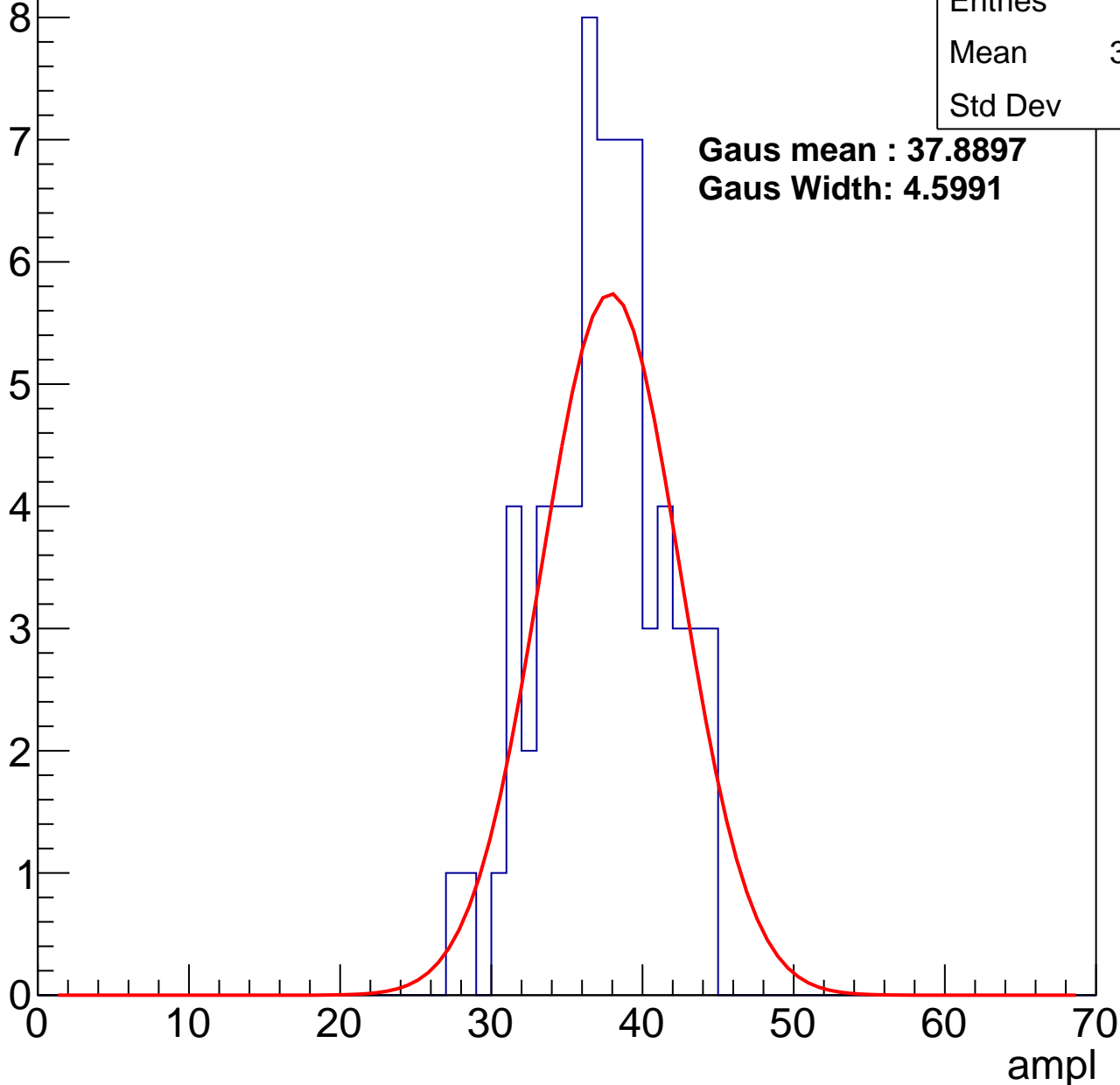
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	66
Mean	36.94
Std Dev	3.9

**Gaus mean : 37.8897**

**Gaus Width: 4.5991**



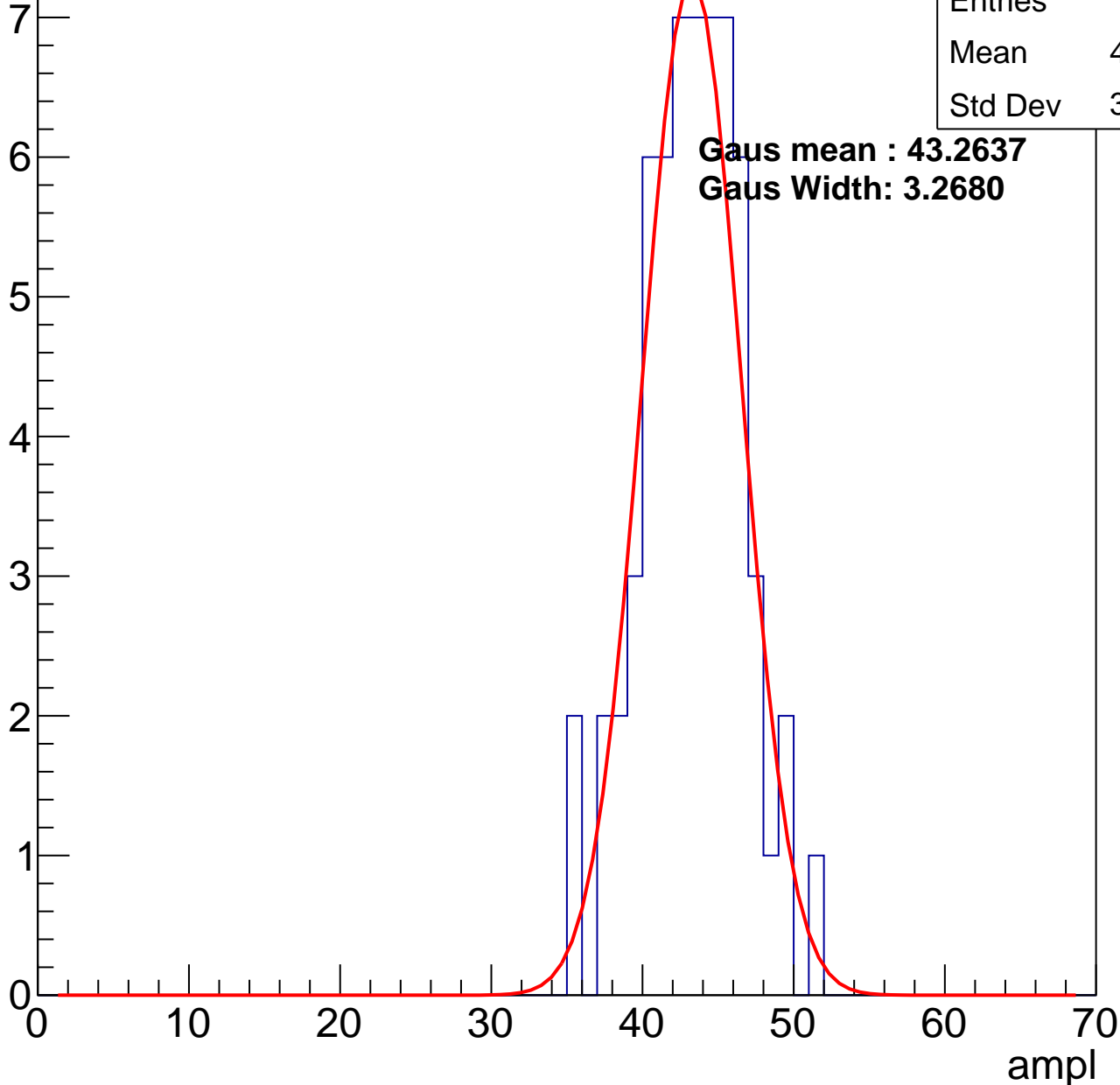
# B1L101S, U3-ch113, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	42.82
Std Dev	3.309

**Gaus mean : 43.2637**  
**Gaus Width: 3.2680**

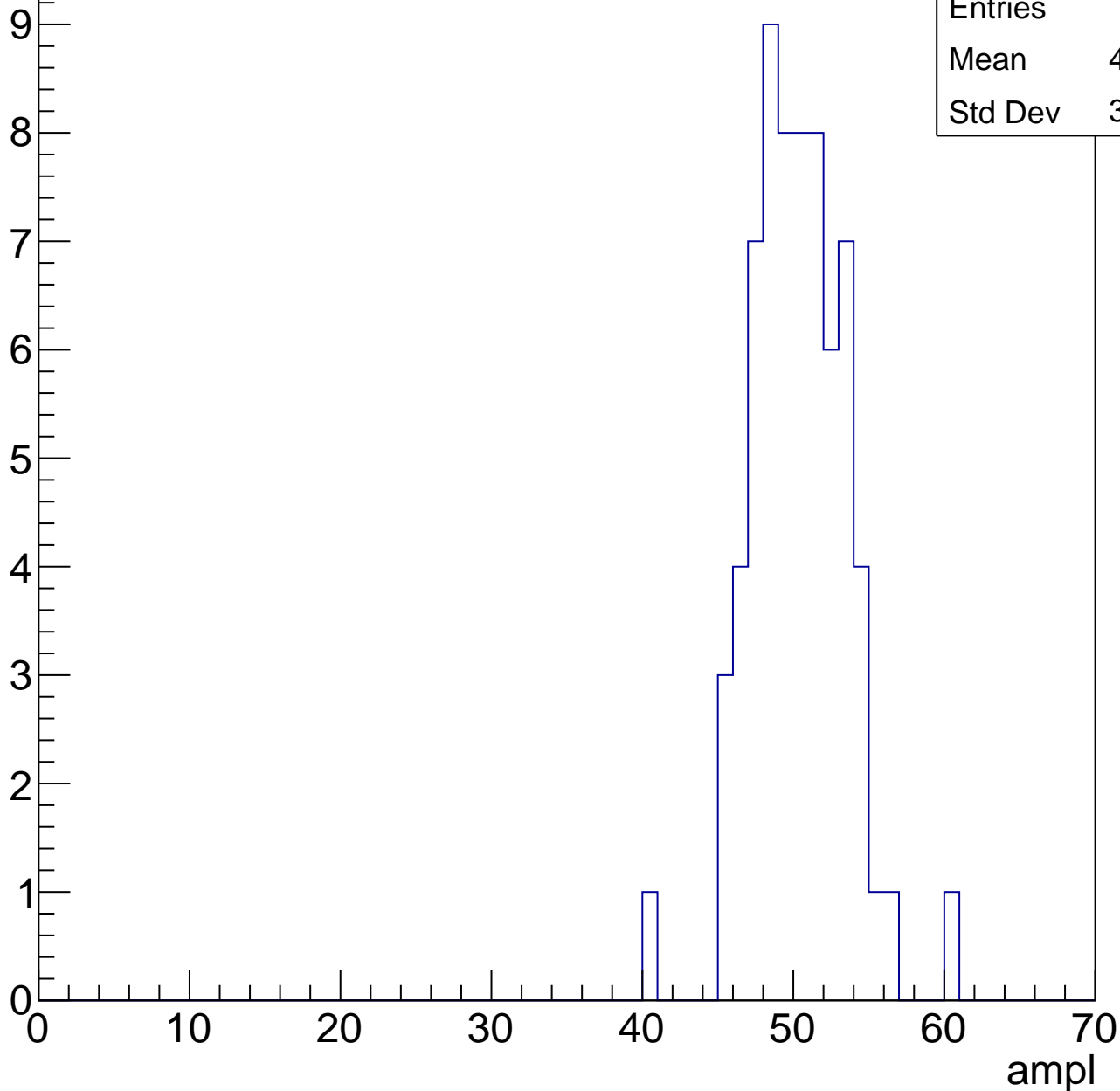


# B1L101S, U3-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

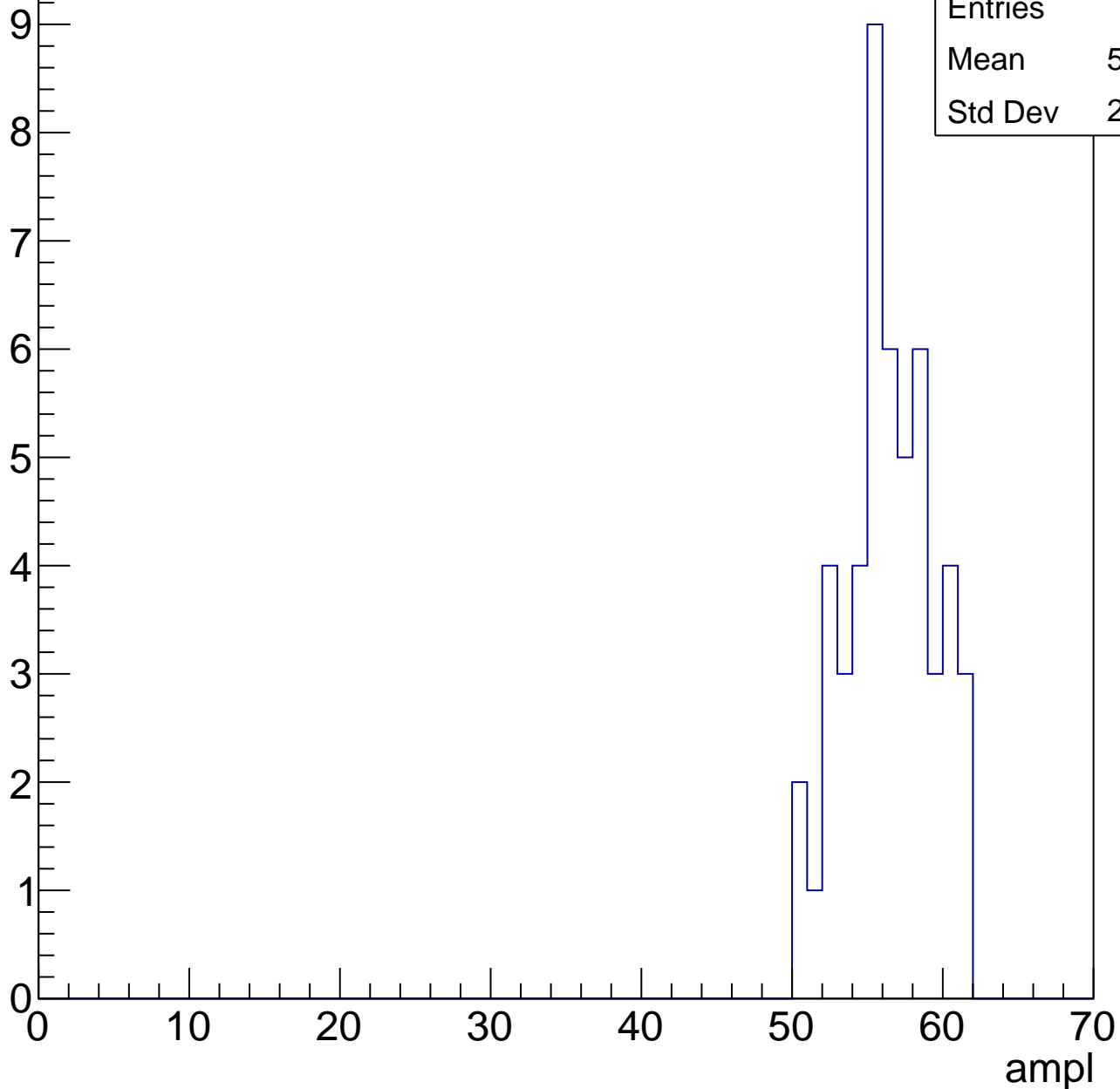
Entries	68
Mean	49.85
Std Dev	3.126



# B1L101S, U3-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



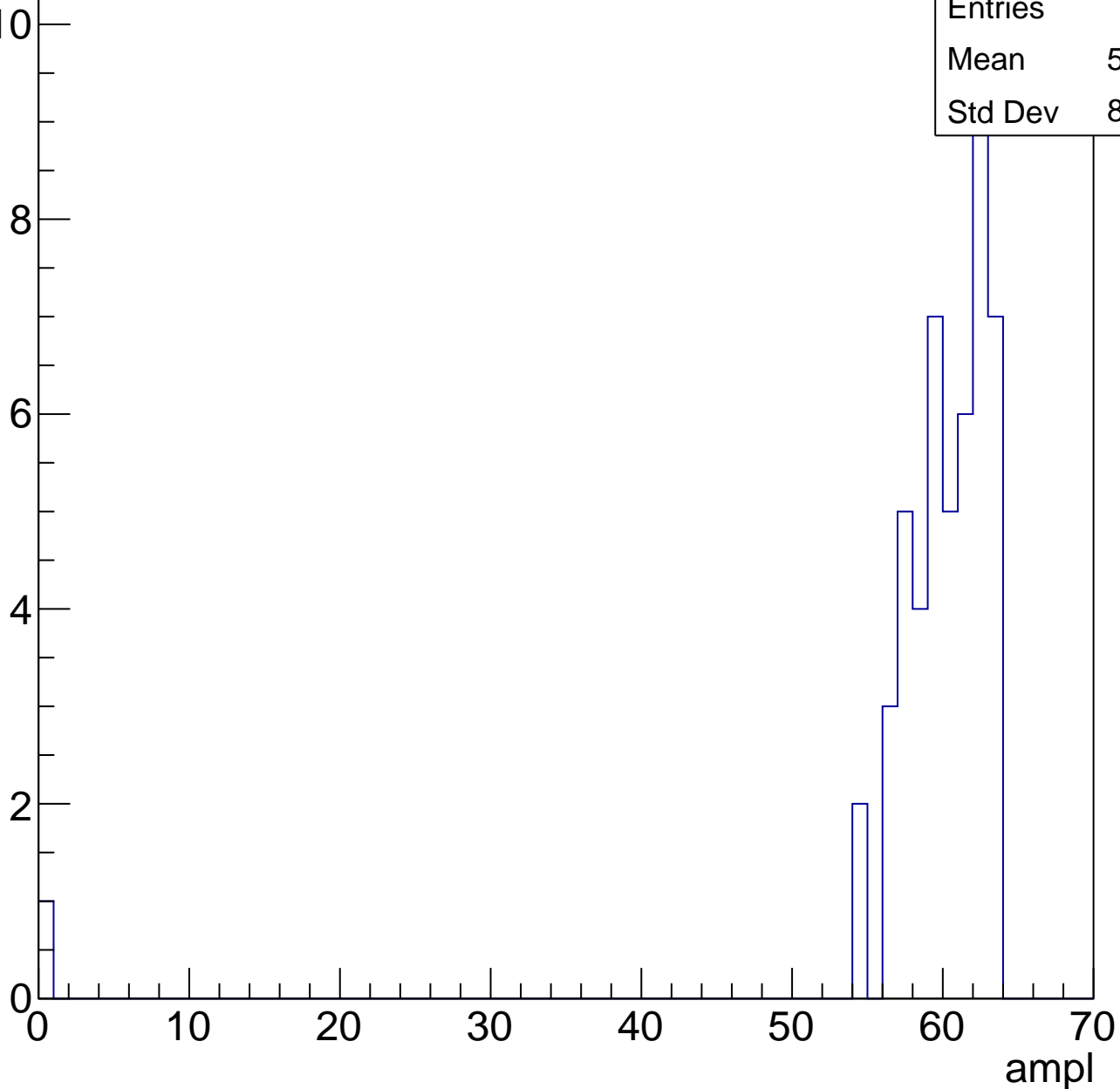
Entries	50
Mean	55.96
Std Dev	2.856

# B1L101S, U3-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	58.66
Std Dev	8.726



# B1L101S, U3-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U3-ch114, adc0

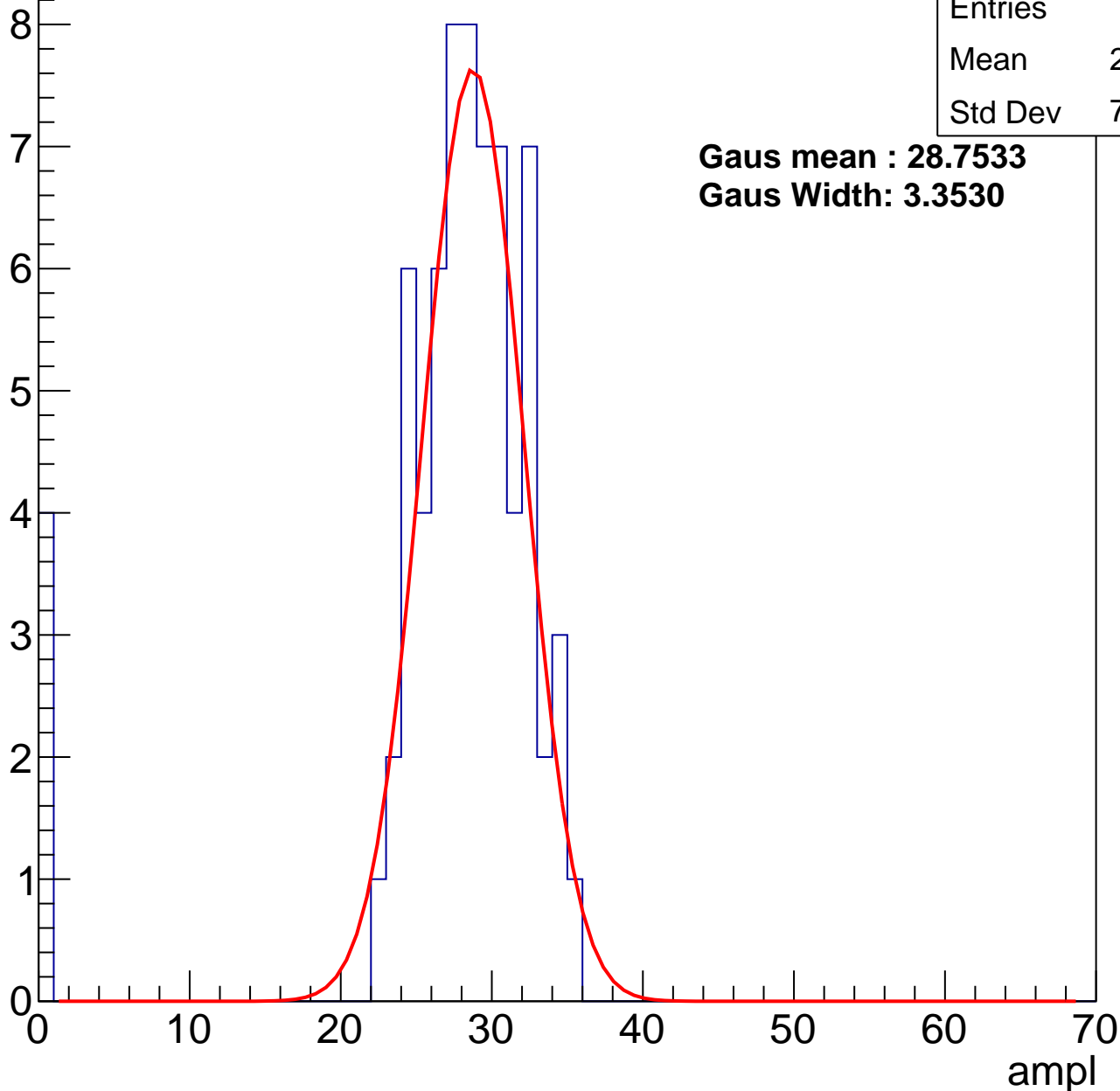
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	70
Mean	26.74
Std Dev	7.236

**Gaus mean : 28.7533**

**Gaus Width: 3.3530**



# B1L101S, U3-ch114, adc1

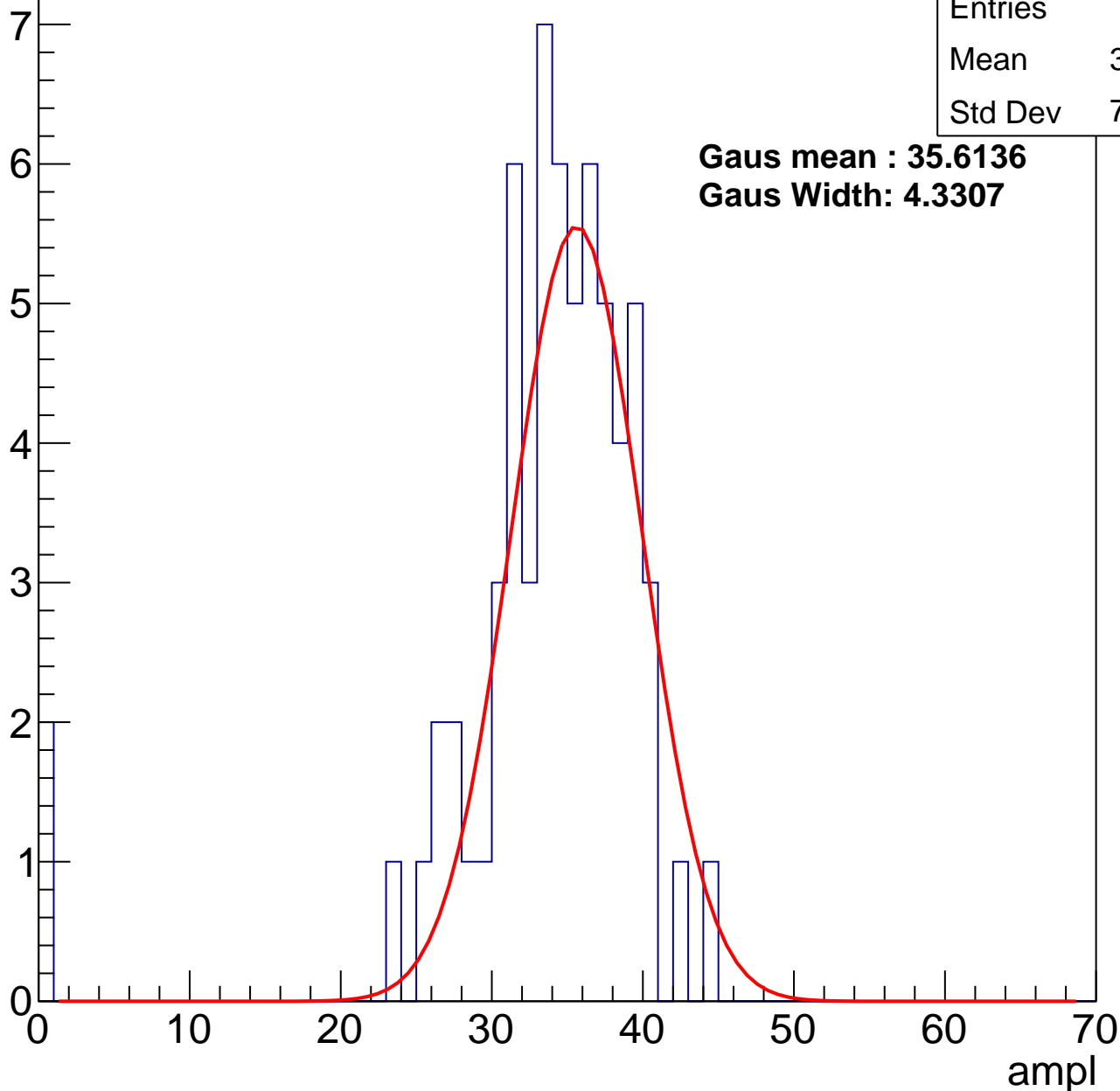
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	33.03
Std Dev	7.228

**Gaus mean : 35.6136**

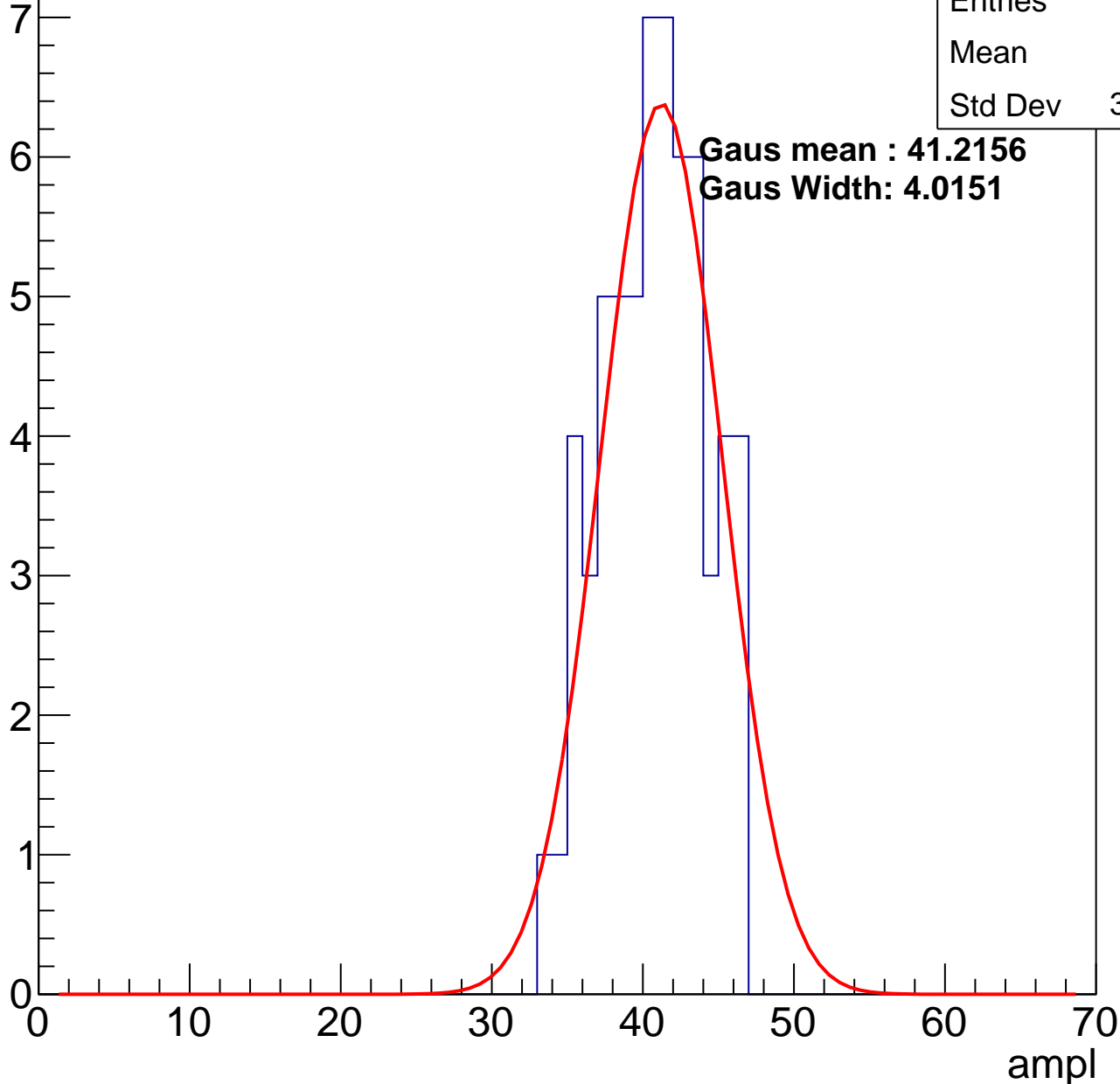
**Gaus Width: 4.3307**



# B1L101S, U3-ch114, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	61
Mean	40.3
Std Dev	3.326

# B1L101S, U3-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	73
Mean	47.14
Std Dev	3.83

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

0

2

4

6

8

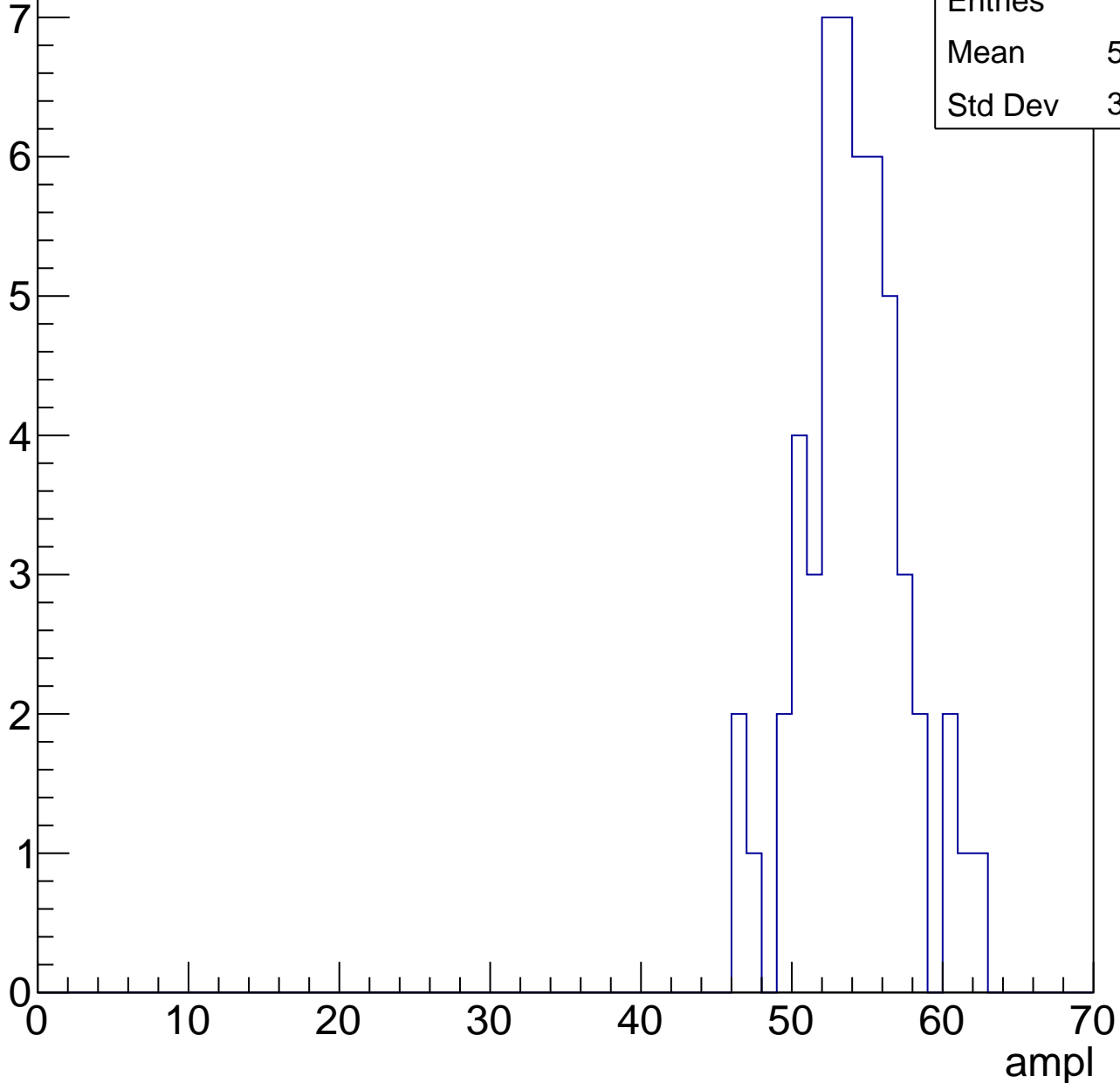
10

# B1L101S, U3-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	53.63
Std Dev	3.442

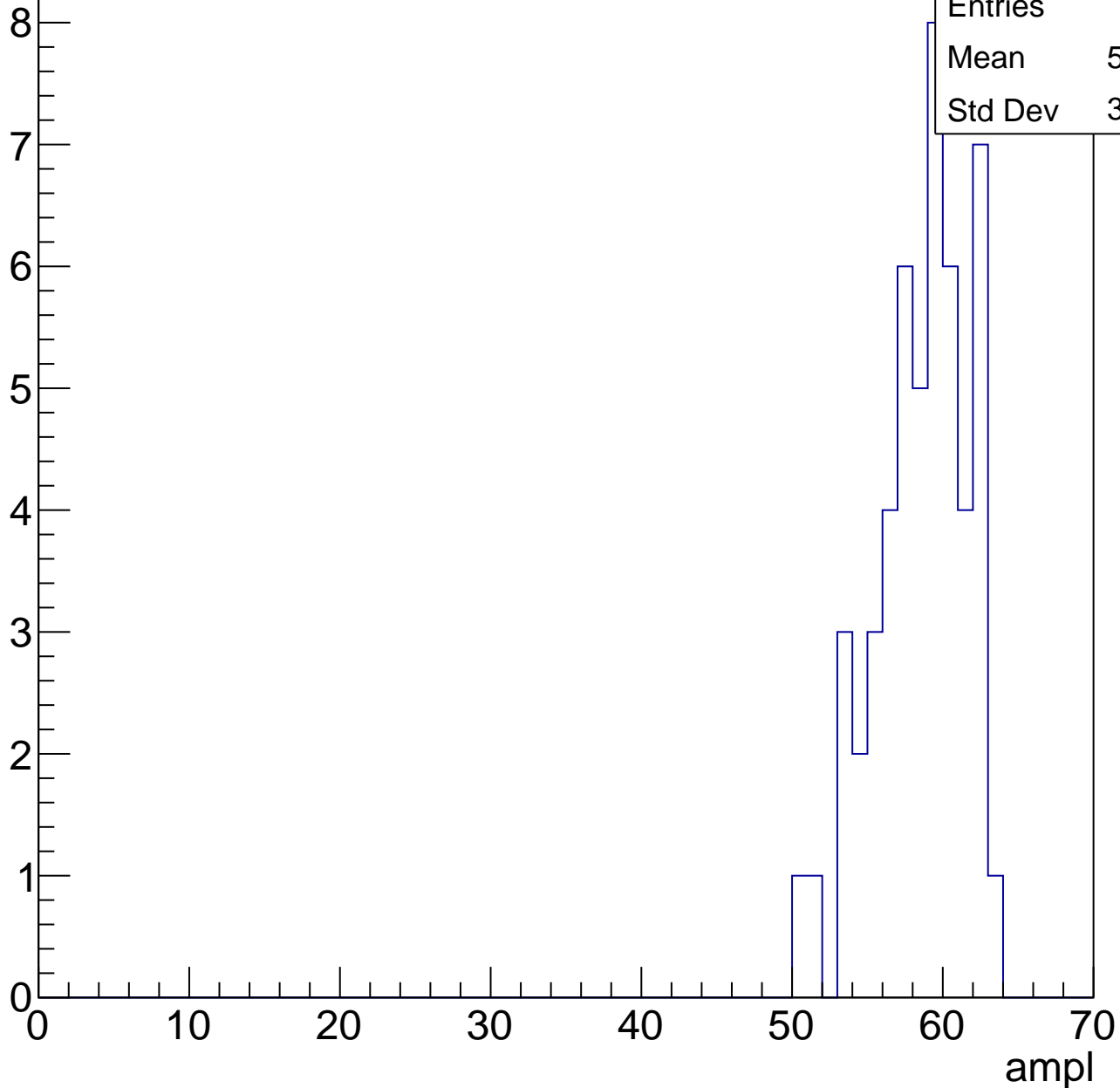


# B1L101S, U3-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	58.08
Std Dev	3.048

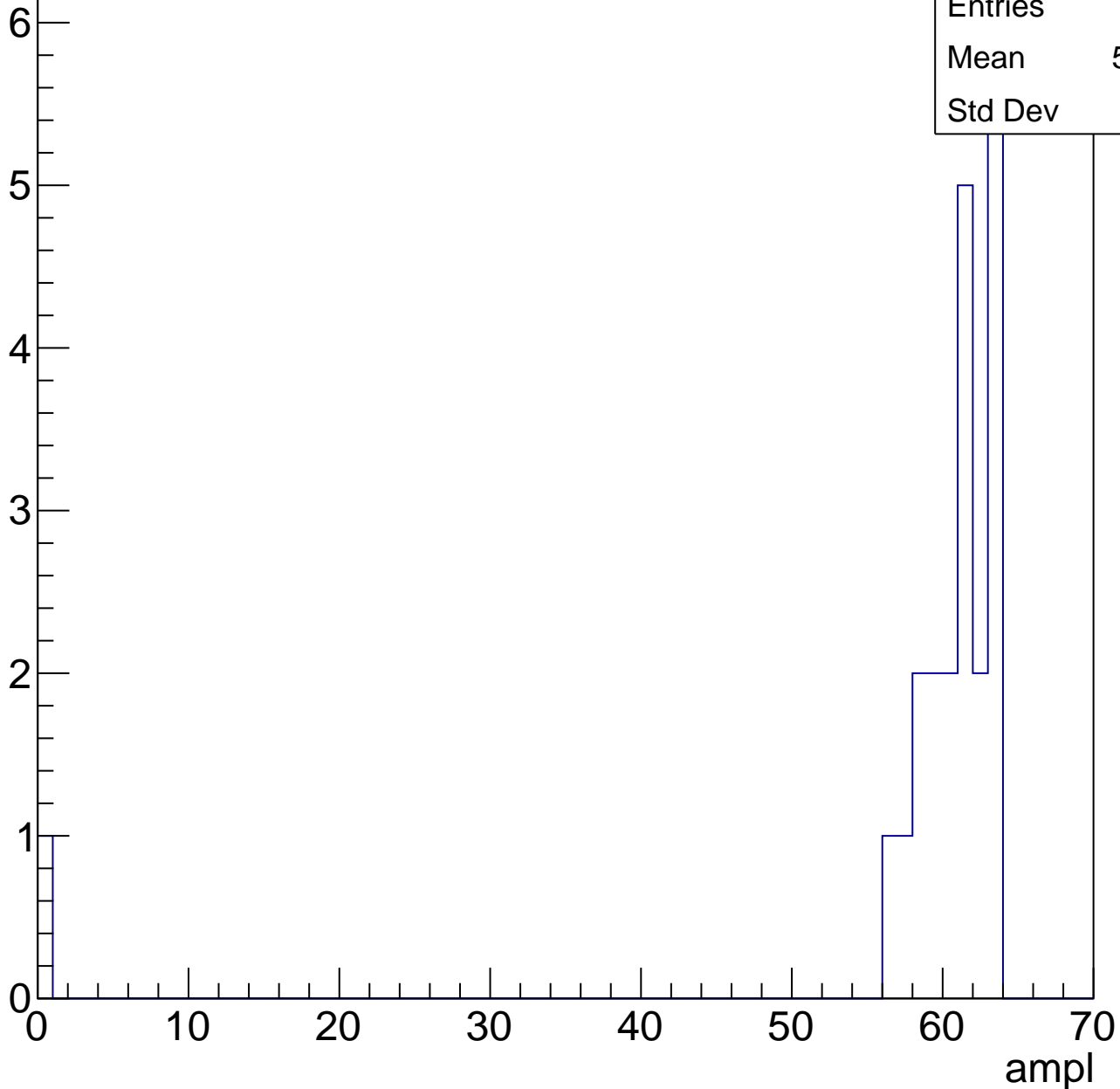


# B1L101S, U3-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	22
Mean	57.91
Std Dev	12.8

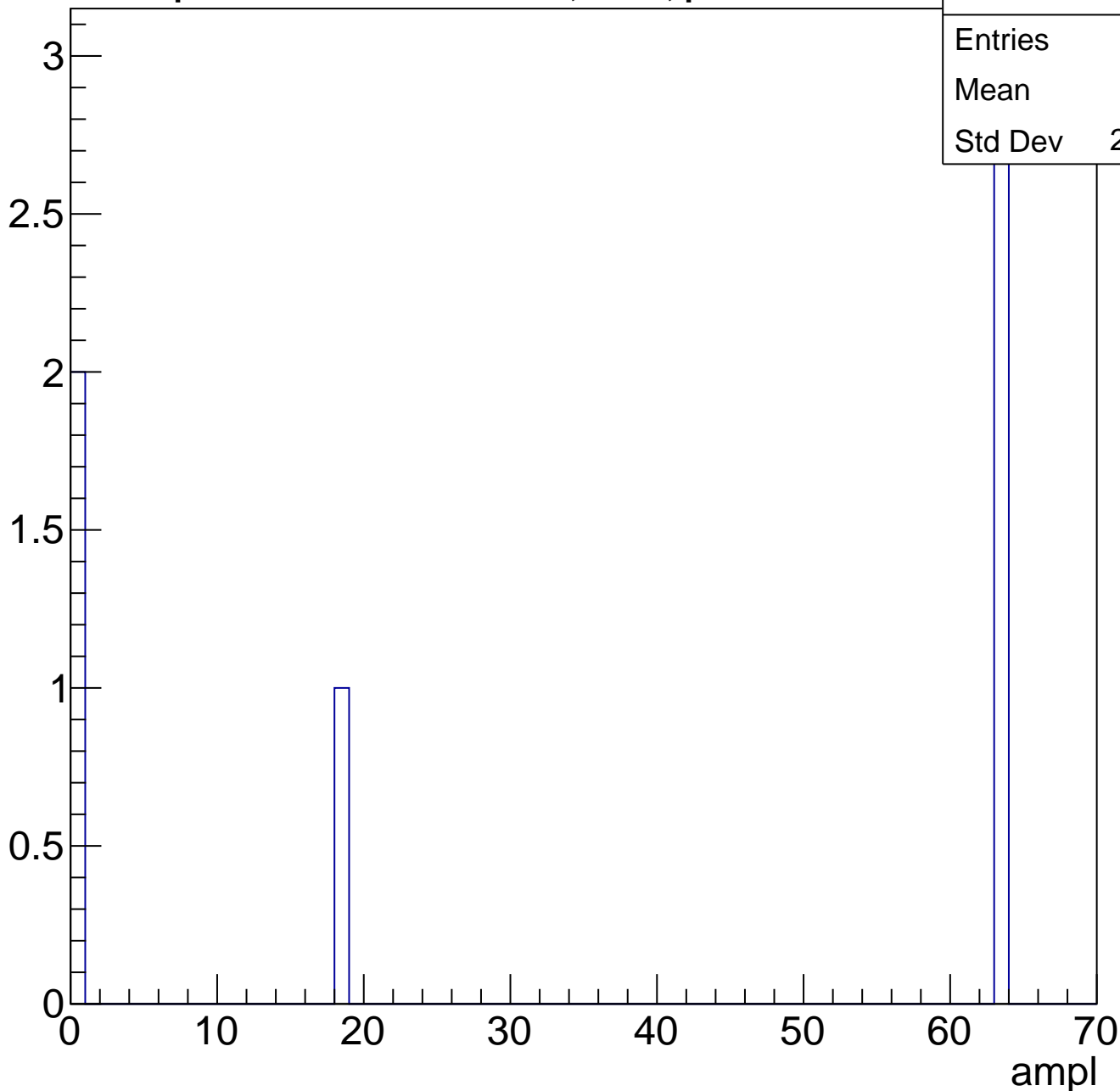




# B1L101S, U3-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch115, adc0

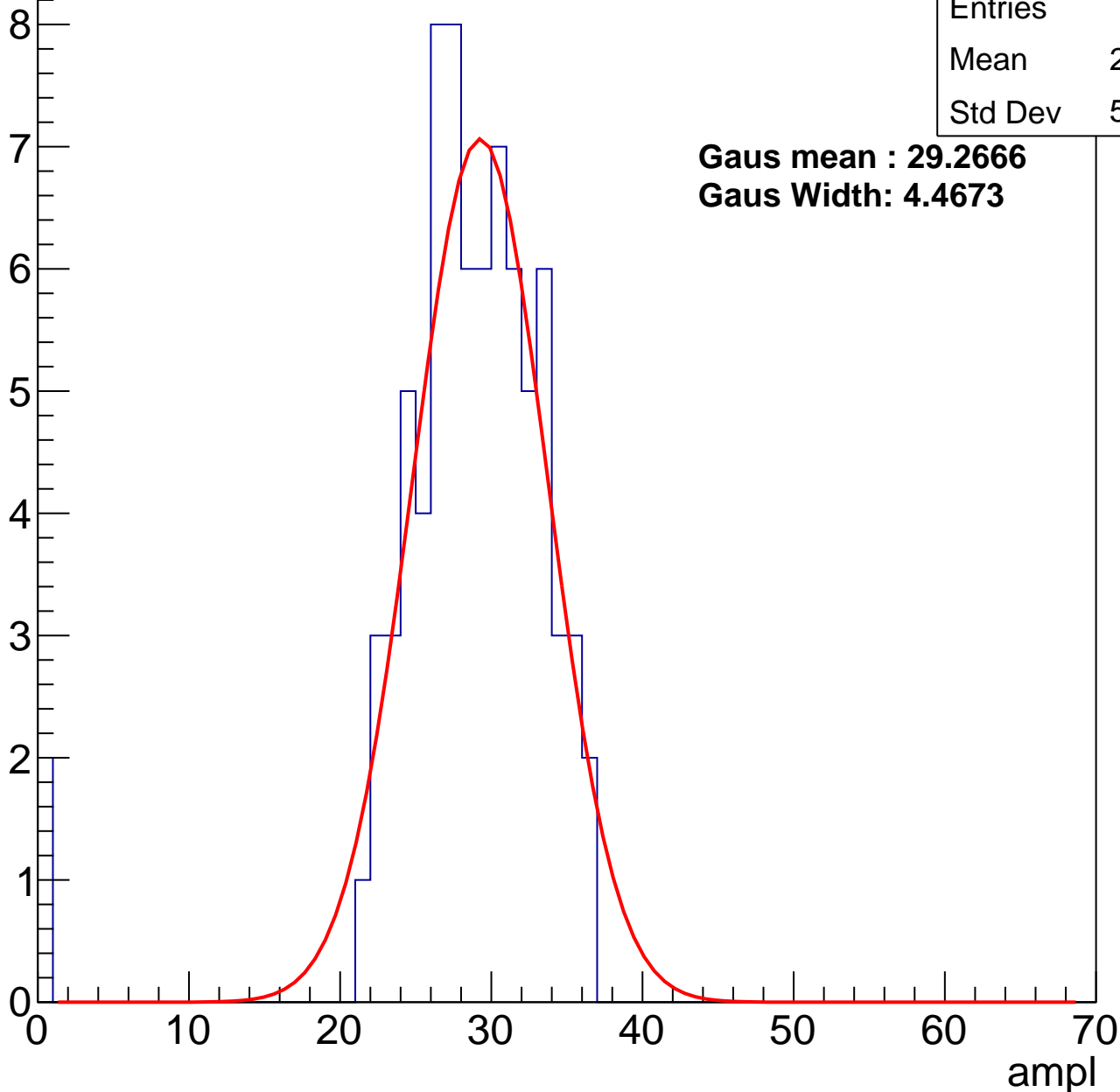
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	78
Mean	27.88
Std Dev	5.835

**Gaus mean : 29.2666**

**Gaus Width: 4.4673**



# B1L101S, U3-ch115, adc1

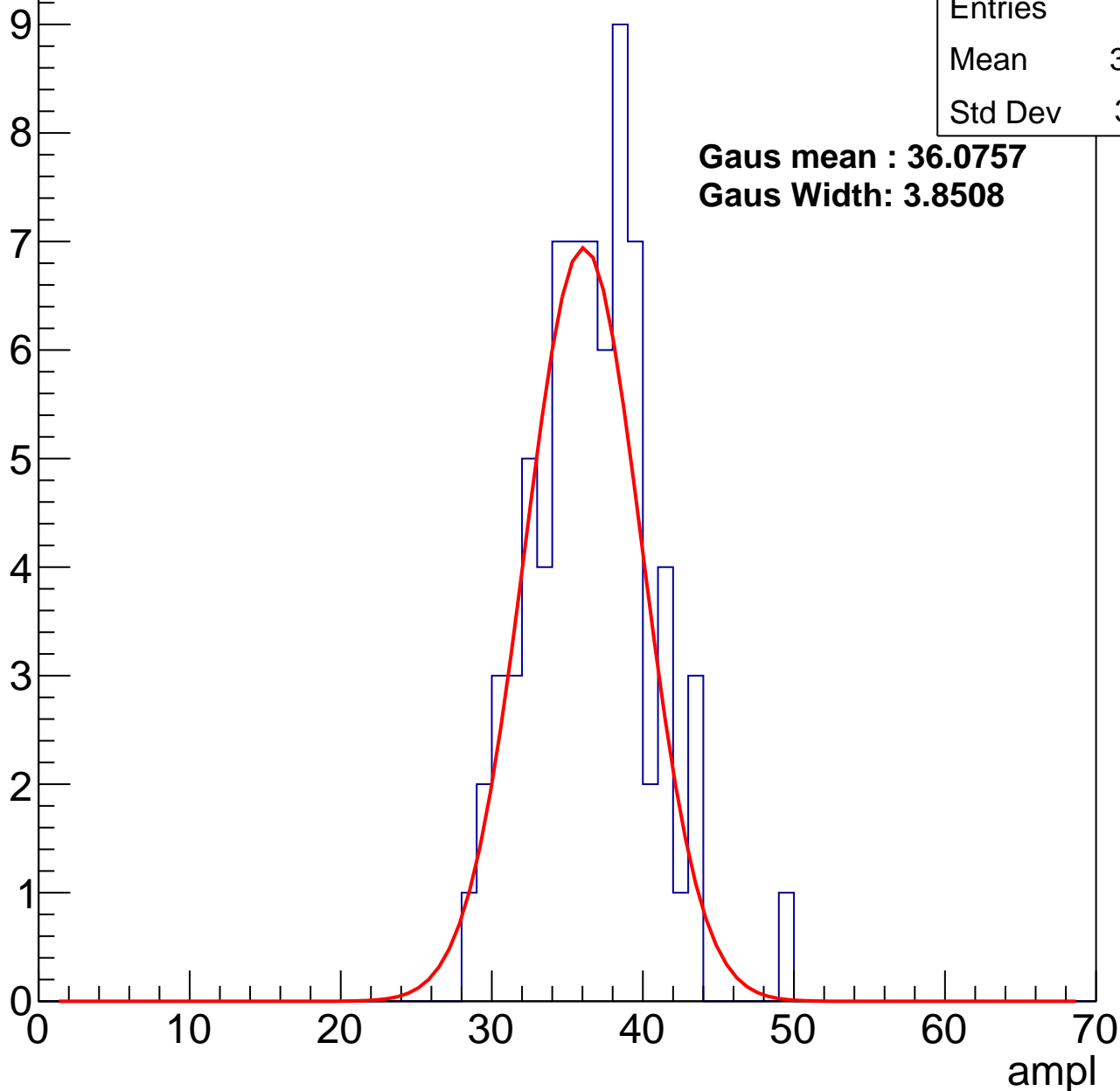
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	36.07
Std Dev	3.881

**Gaus mean : 36.0757**

**Gaus Width: 3.8508**



# B1L101S, U3-ch115, adc2

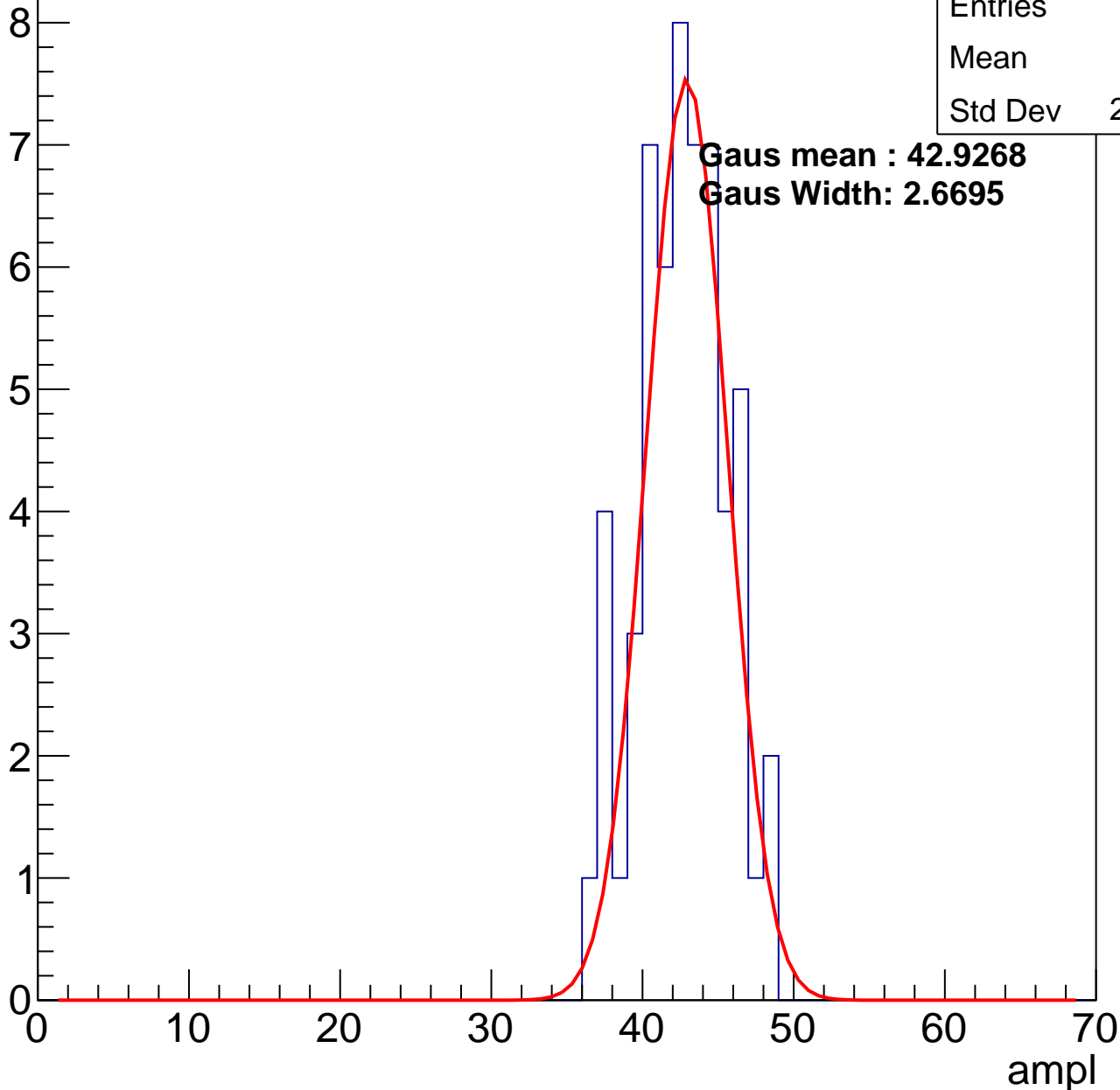
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	42.2
Std Dev	2.862

**Gaus mean : 42.9268**

**Gaus Width: 2.6695**

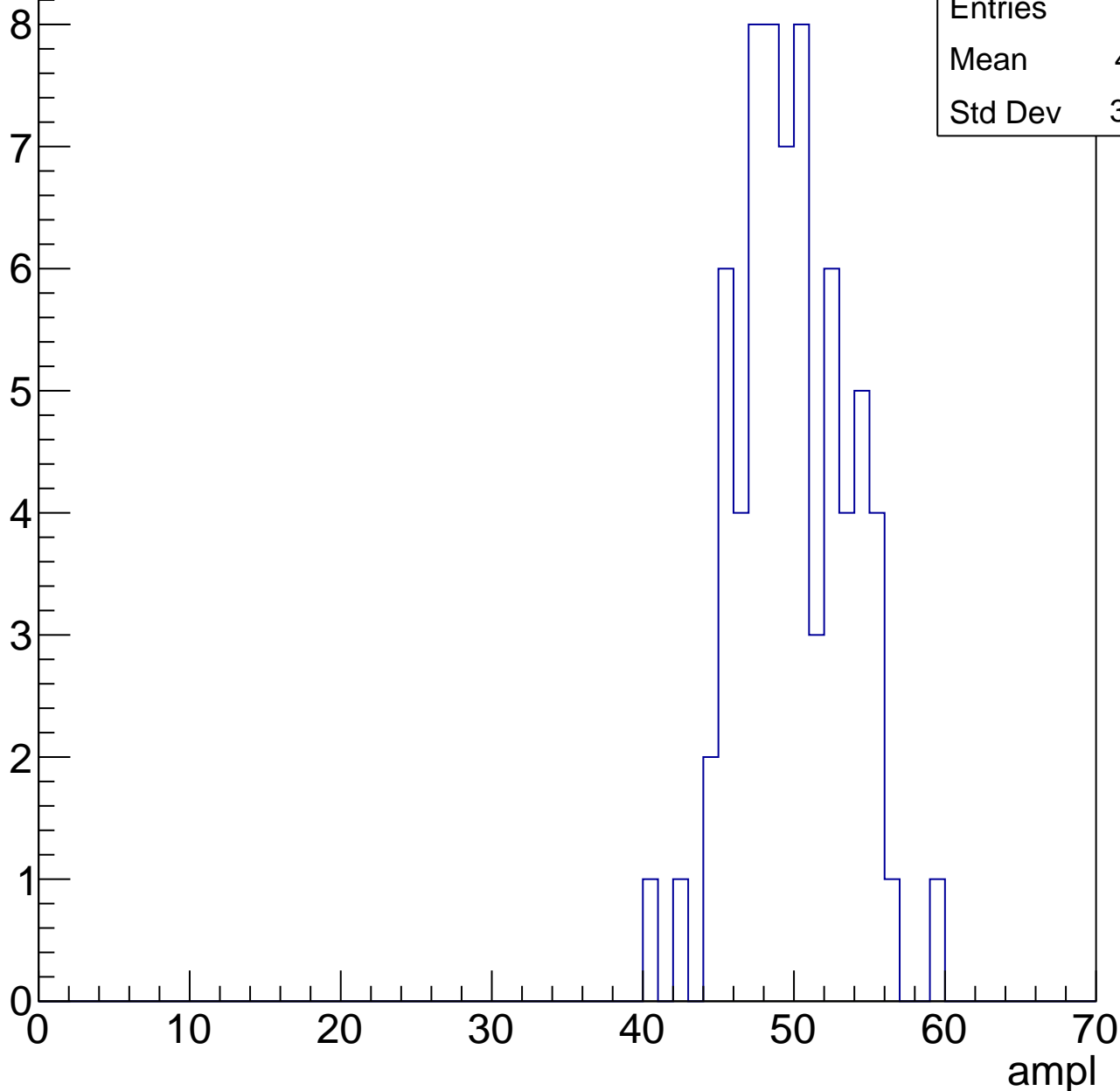


# B1L101S, U3-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	49.41
Std Dev	3.605

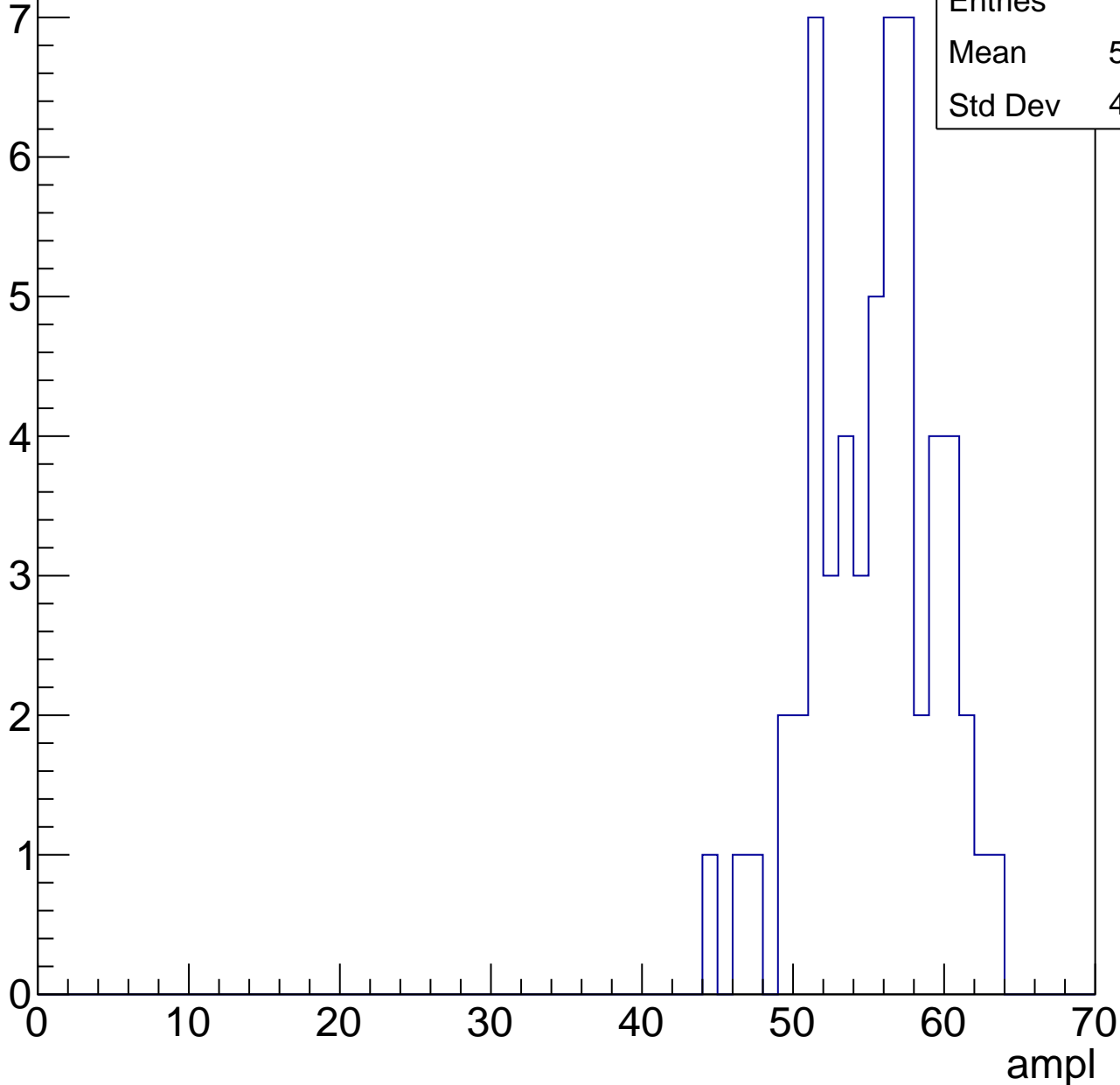


# B1L101S, U3-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

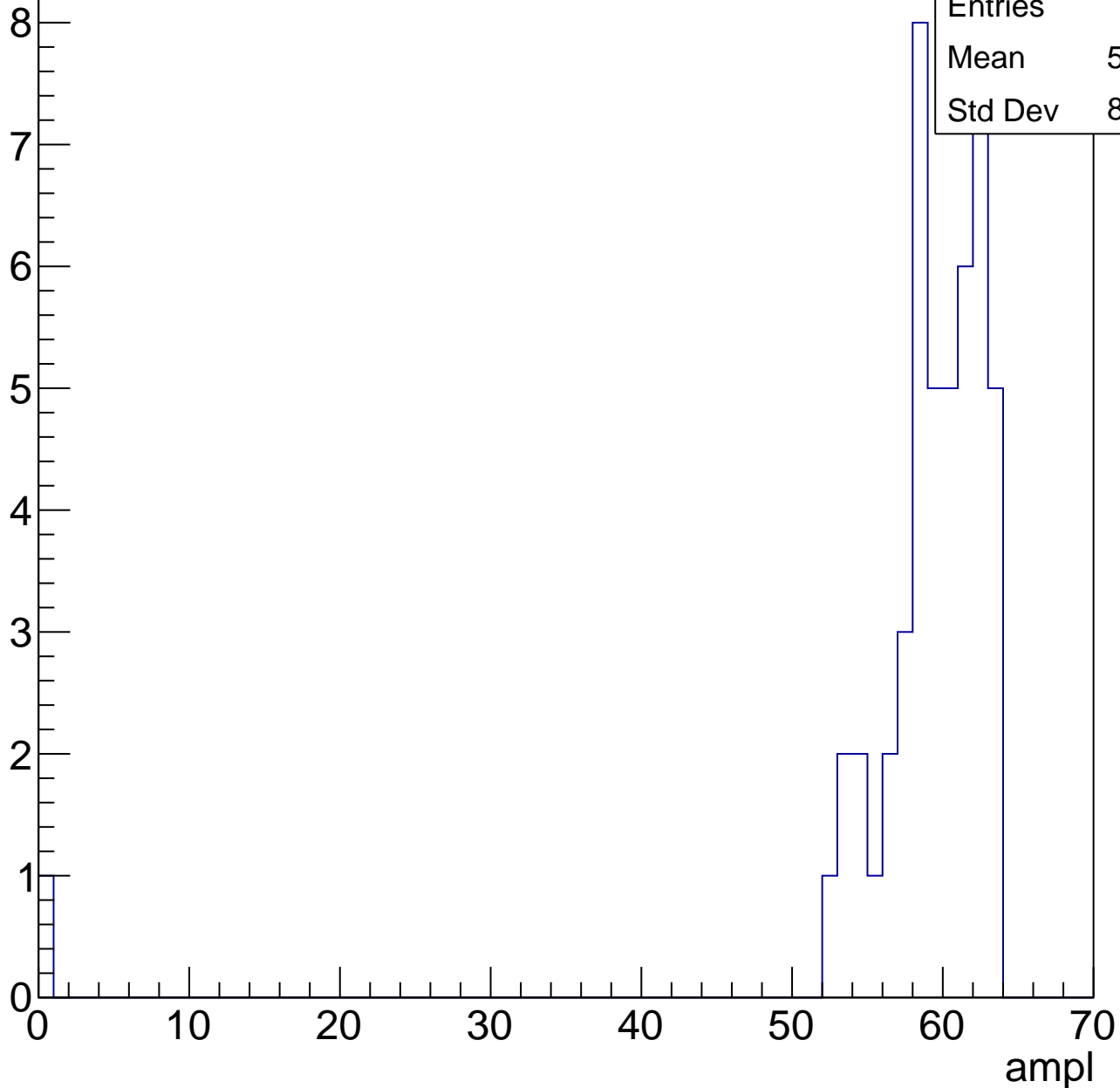
Entries	57
Mean	54.86
Std Dev	4.076



# B1L101S, U3-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

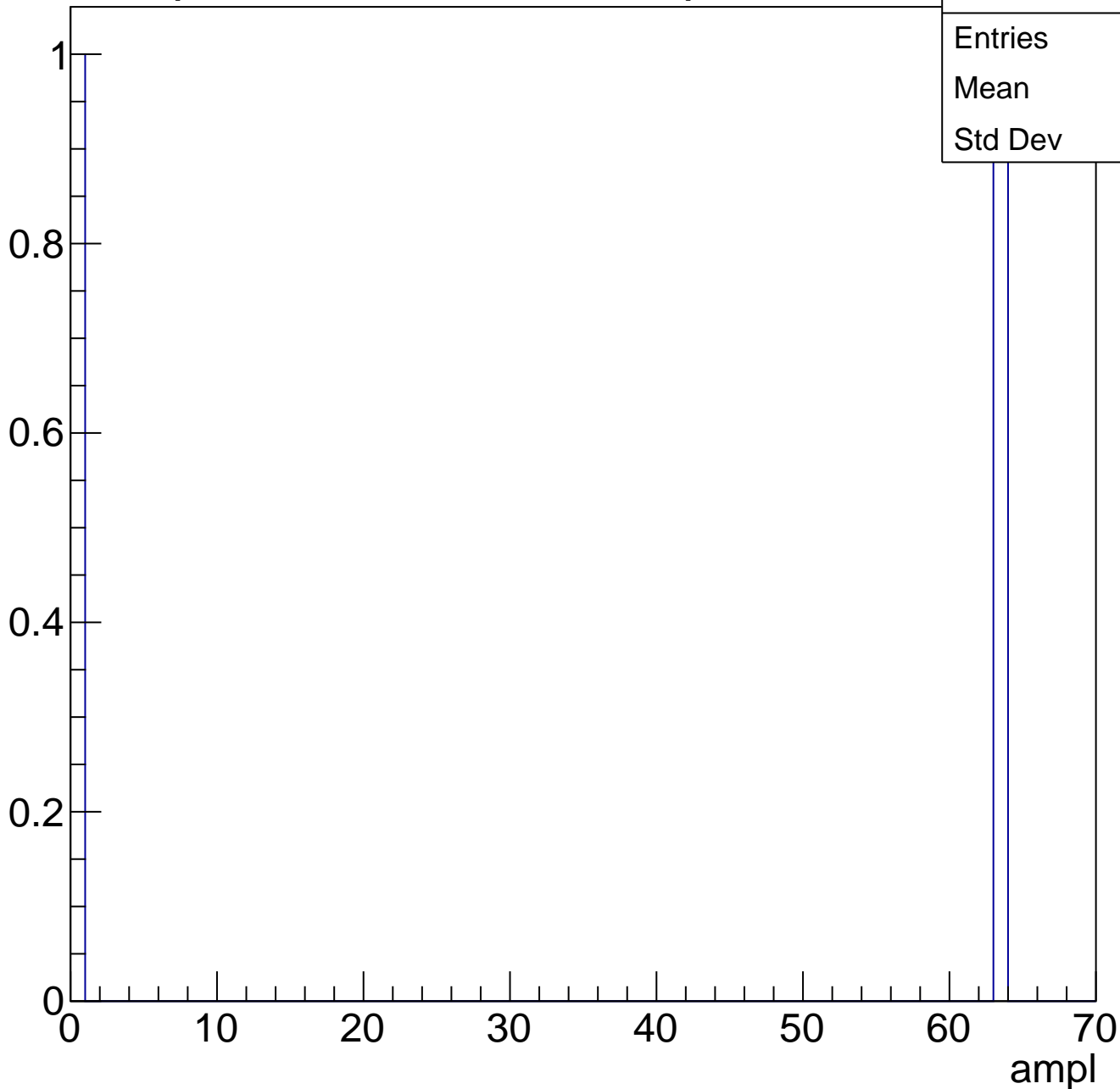




# B1L101S, U3-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch116, adc0

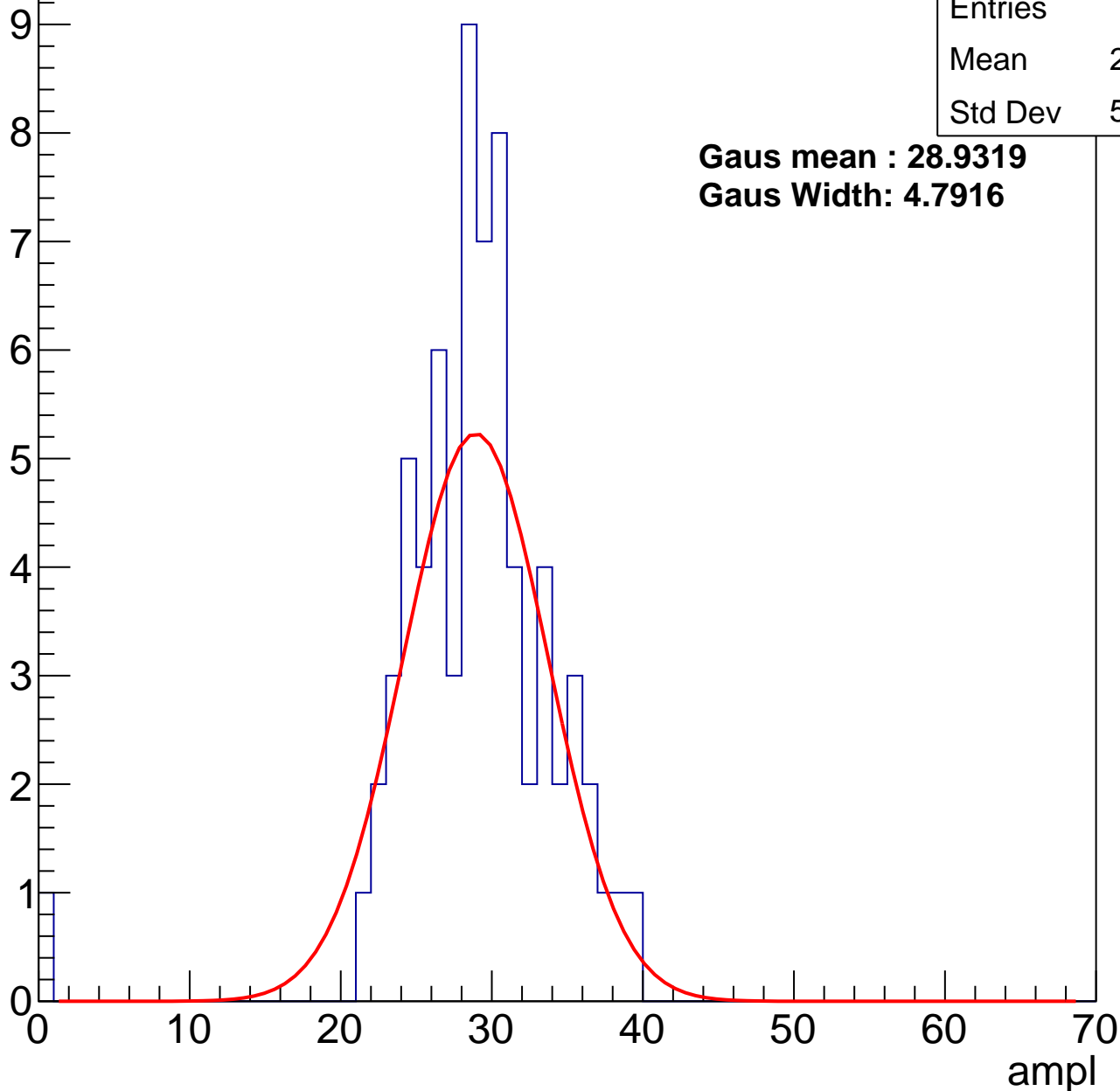
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	28.48
Std Dev	5.334

**Gaus mean : 28.9319**

**Gaus Width: 4.7916**



# B1L101S, U3-ch116, adc1

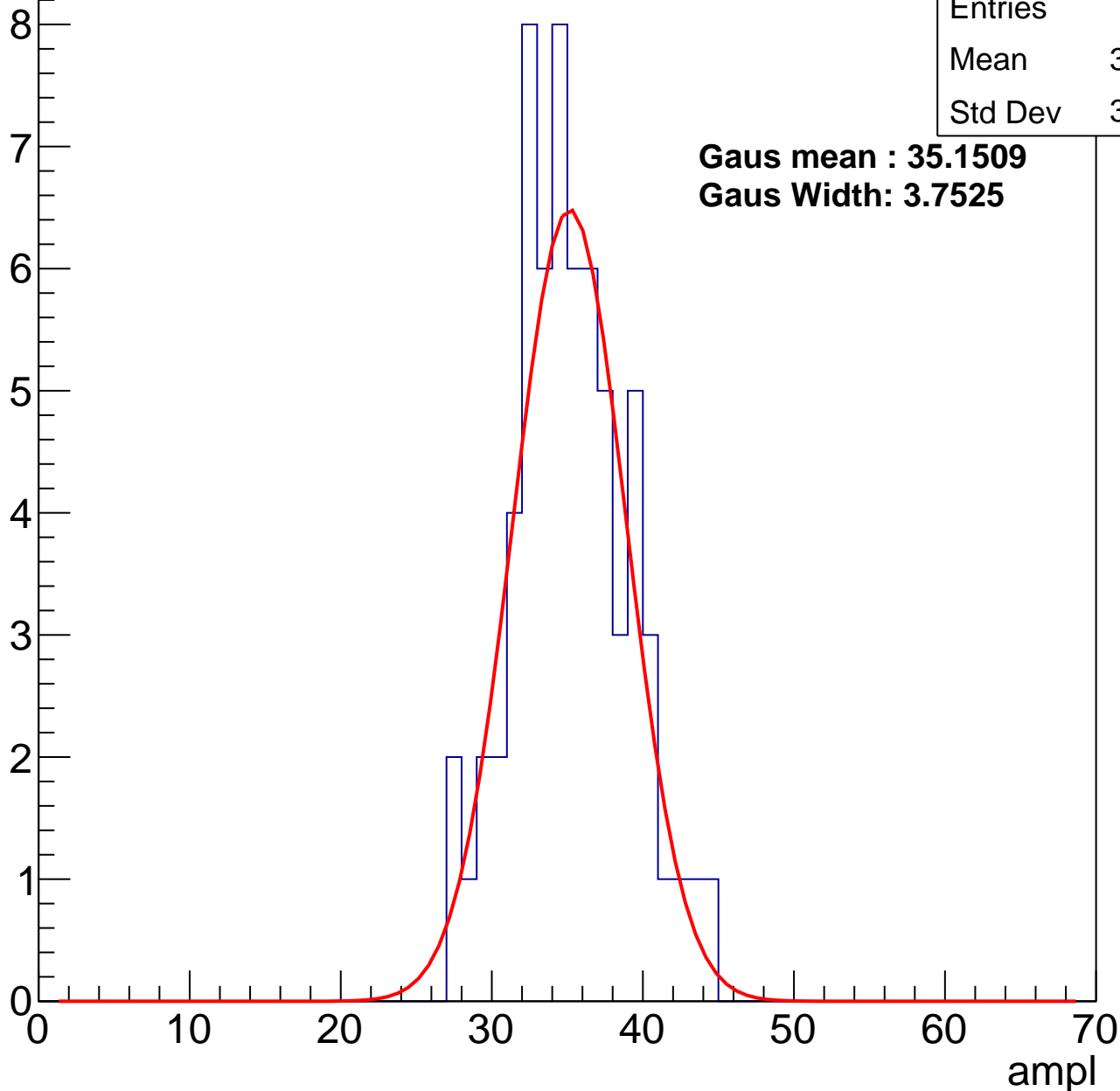
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	34.77
Std Dev	3.724

**Gaus mean : 35.1509**

**Gaus Width: 3.7525**



# B1L101S, U3-ch116, adc2

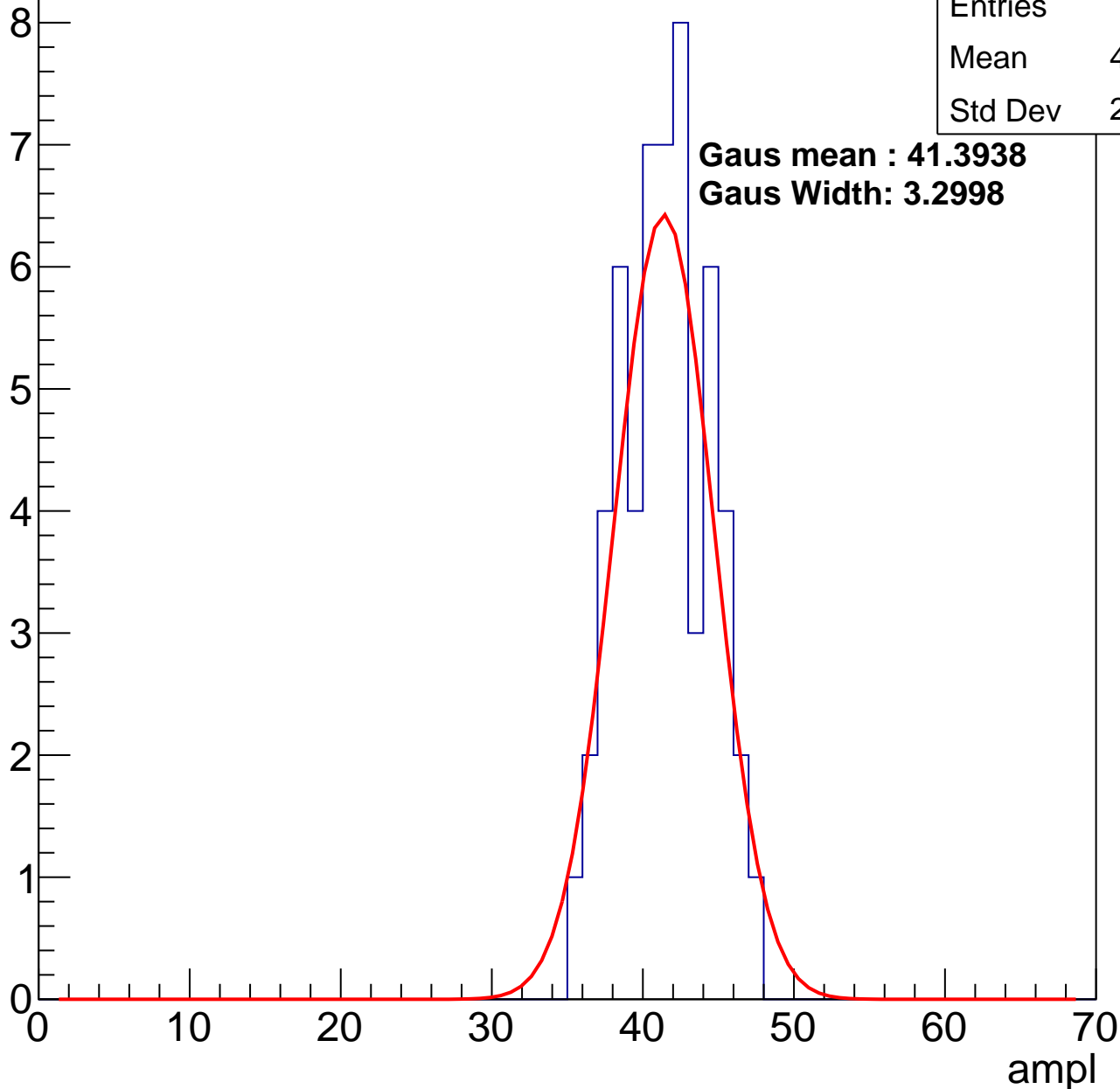
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	40.98
Std Dev	2.864

**Gaus mean : 41.3938**

**Gaus Width: 3.2998**



# B1L101S, U3-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	75
Mean	48.25
Std Dev	3.994

Entry

10

8

6

4

2

0

0

10

20

30

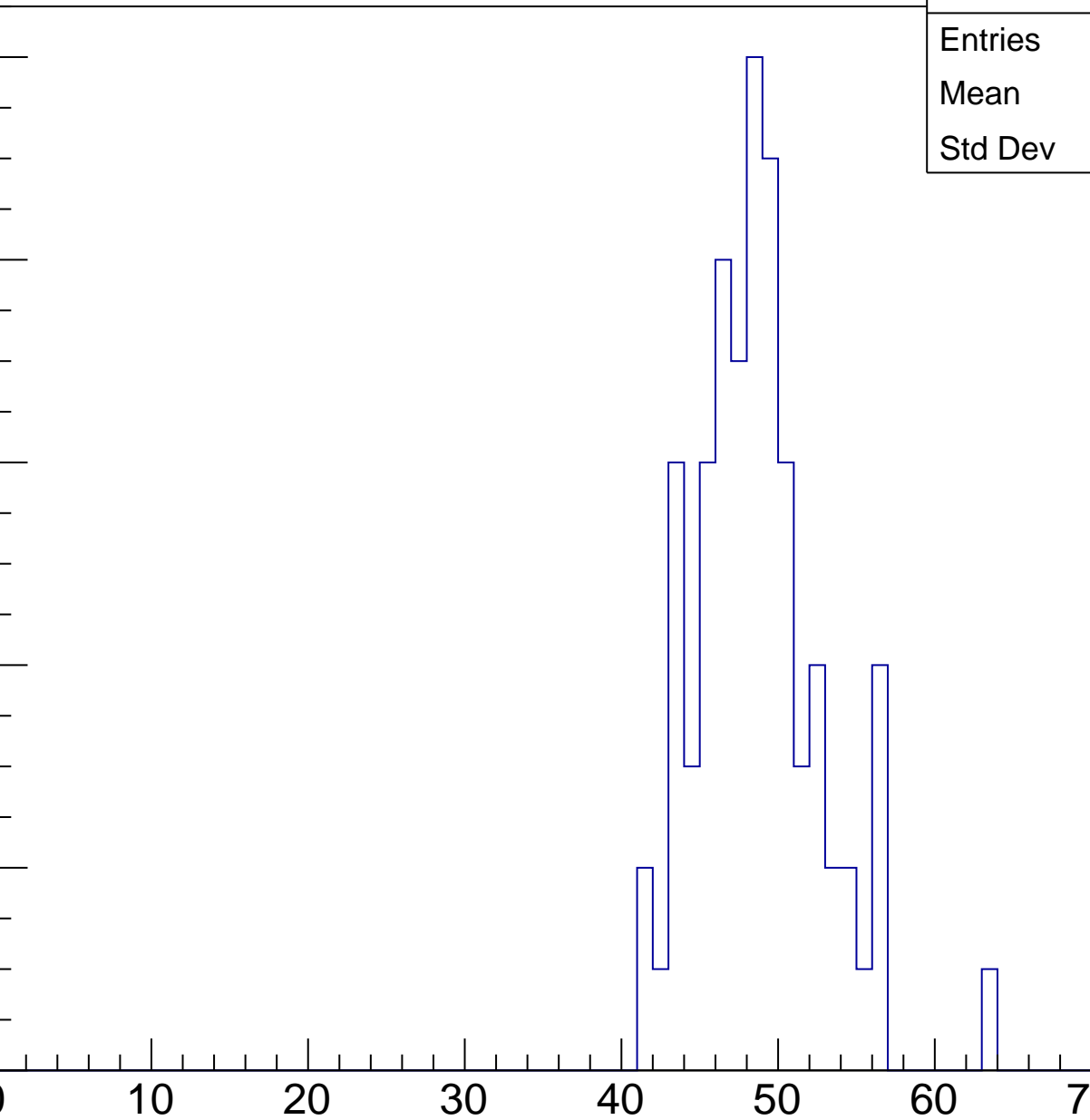
40

50

60

ampl

70

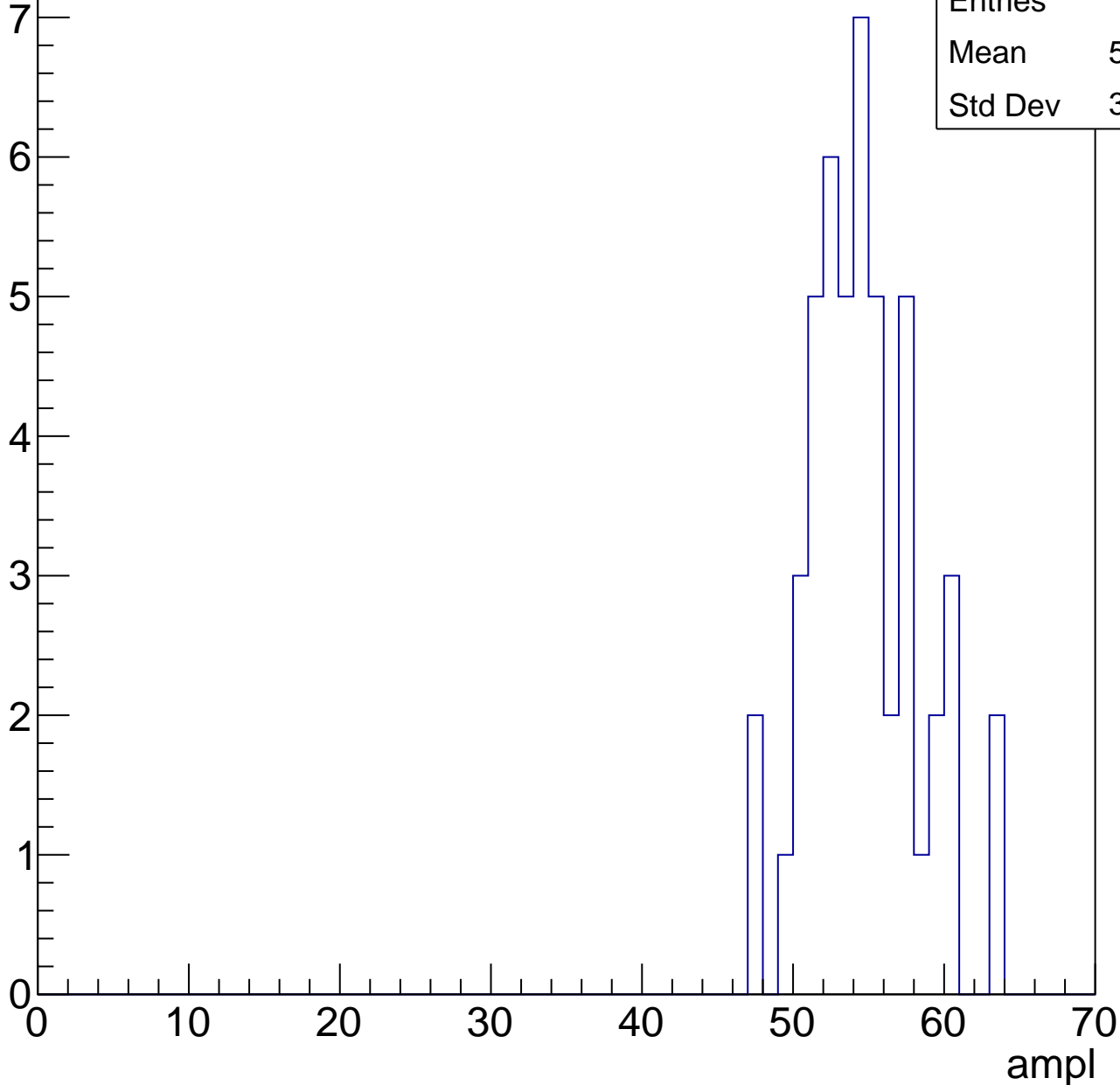


# B1L101S, U3-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

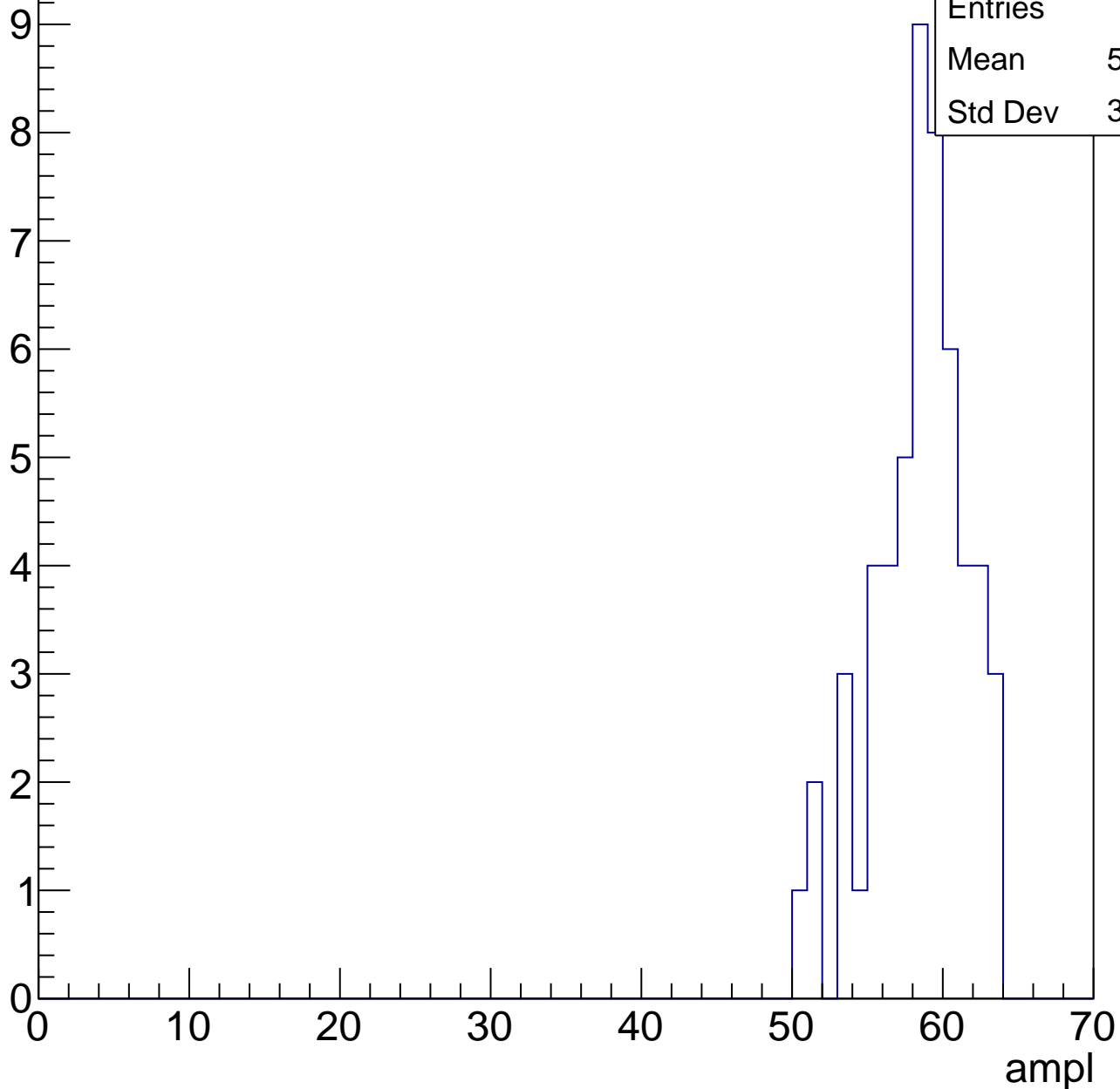
Entries	49
Mean	54.22
Std Dev	3.604



# B1L101S, U3-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

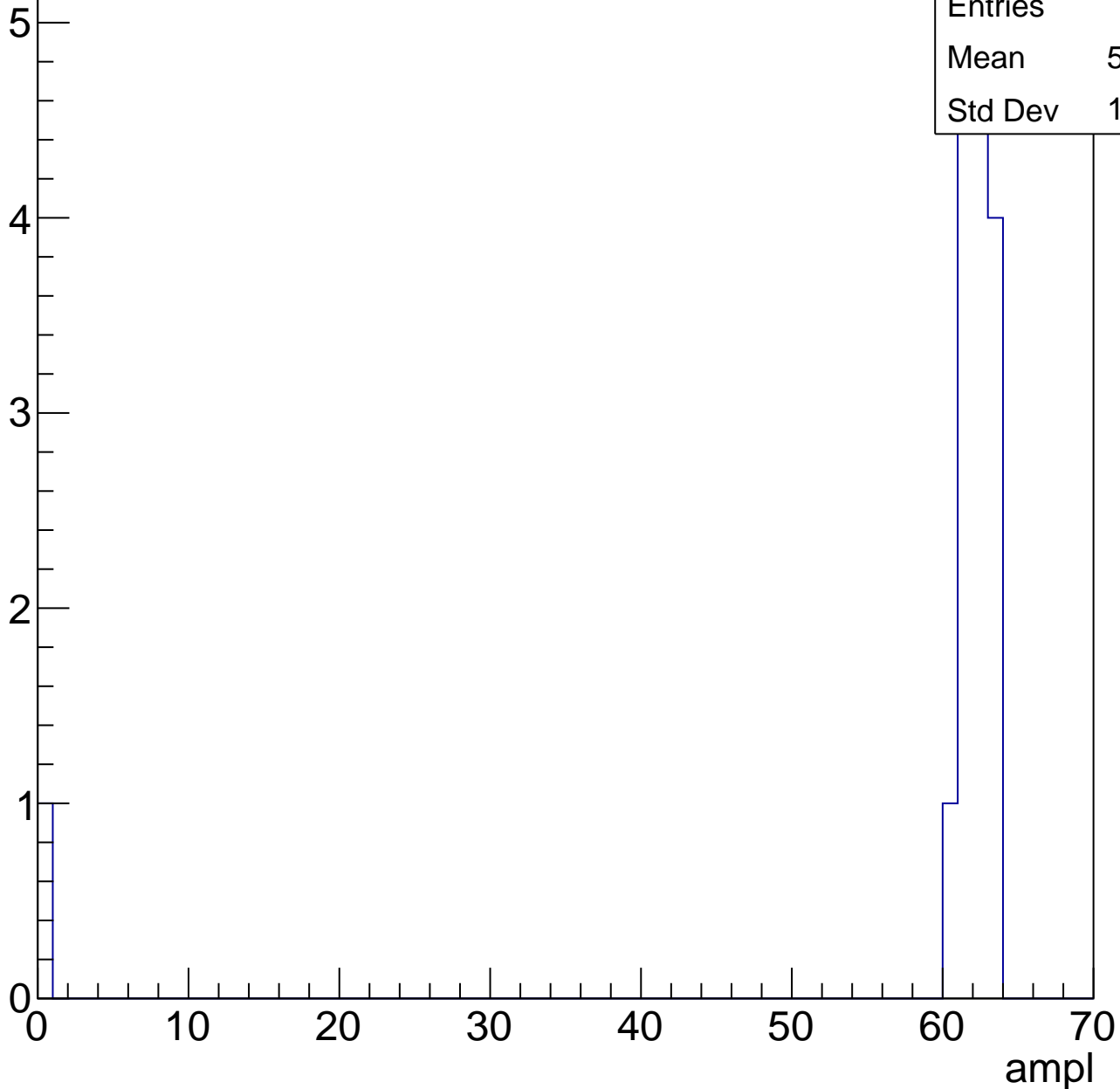


# B1L101S, U3-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	16
Mean	57.94
Std Dev	14.99

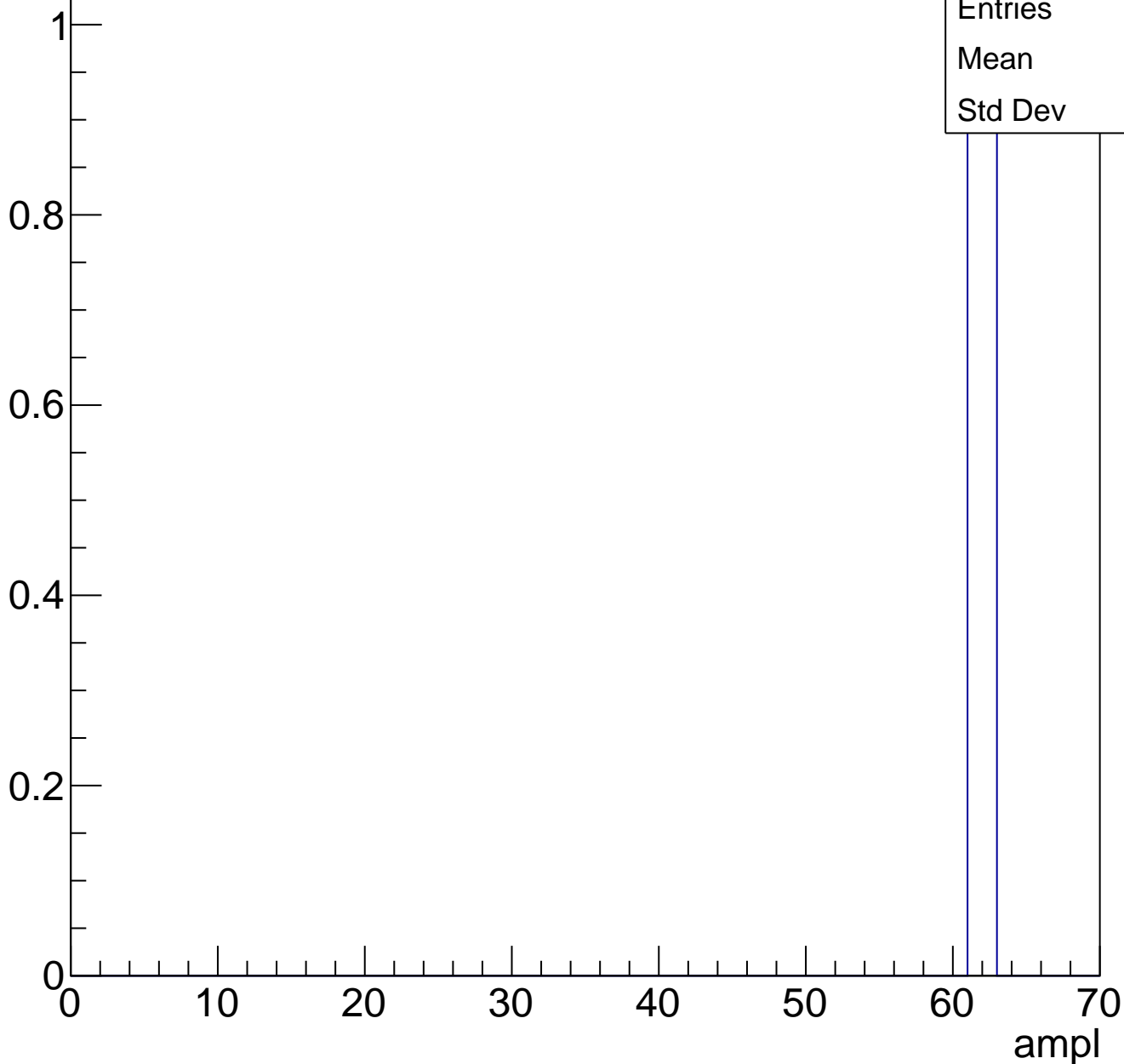




# B1L101S, U3-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch117, adc0

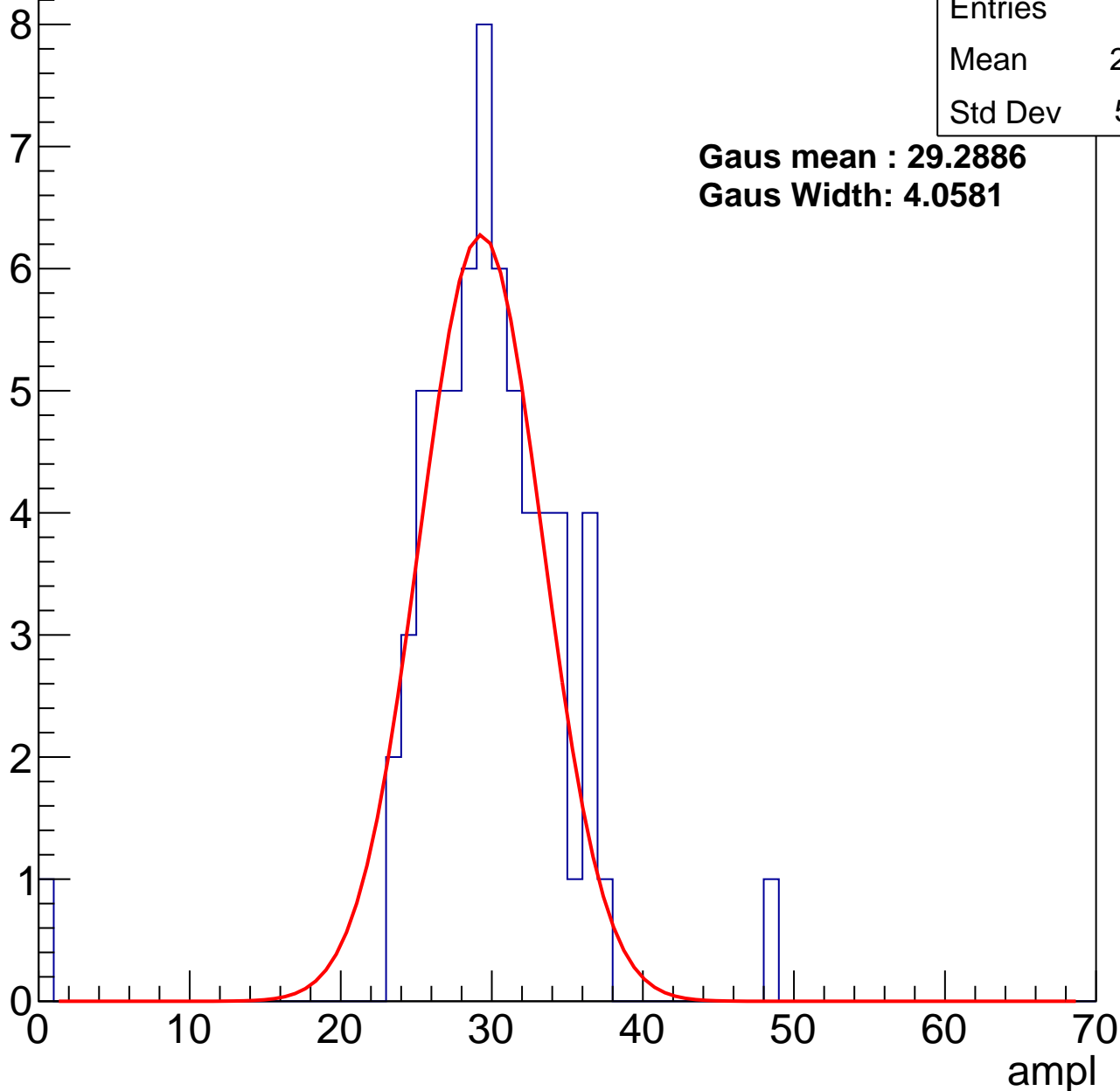
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	29.28
Std Dev	5.571

**Gaus mean : 29.2886**

**Gaus Width: 4.0581**



# B1L101S, U3-ch117, adc1

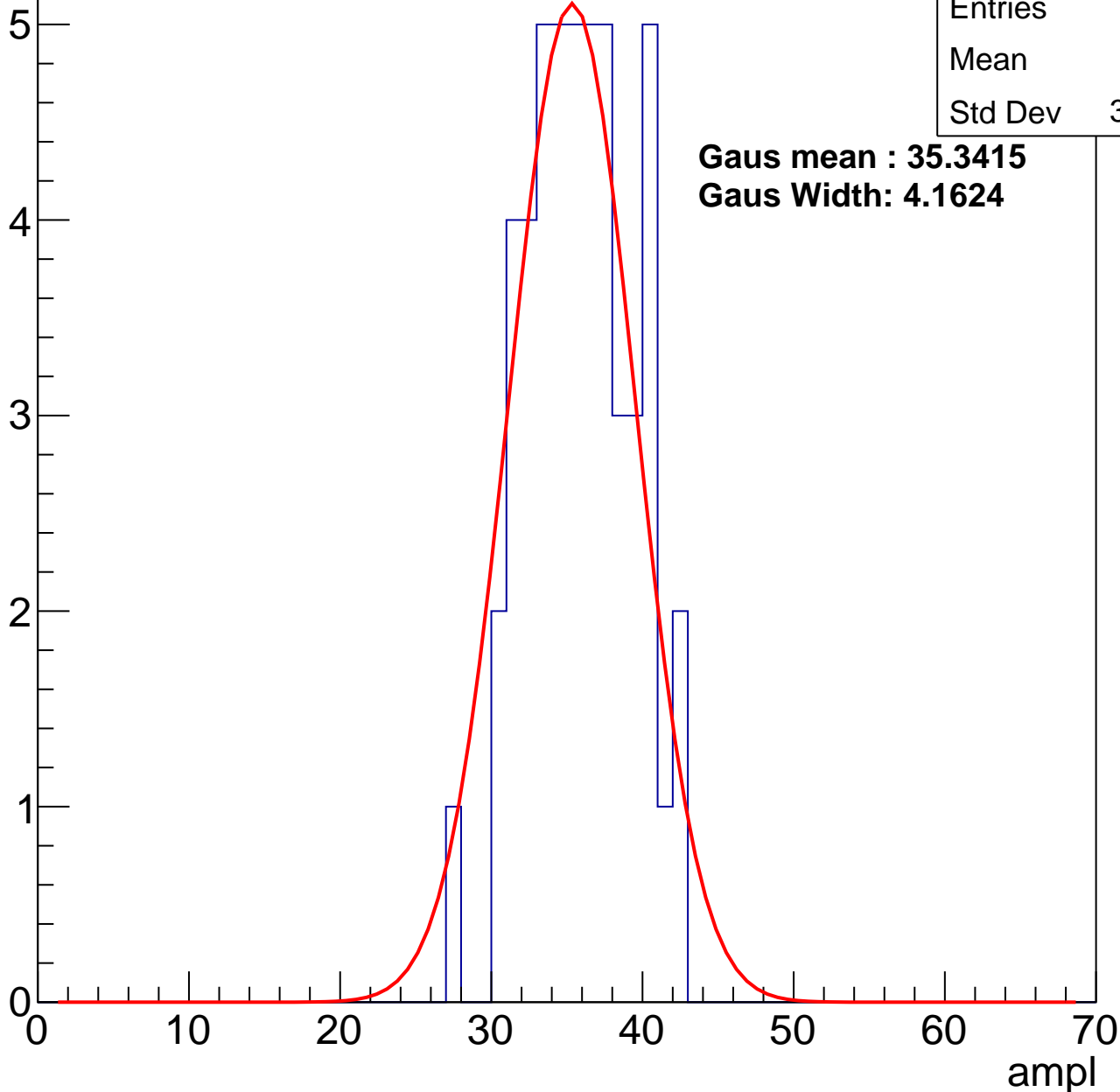
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	35.4
Std Dev	3.435

**Gaus mean : 35.3415**

**Gaus Width: 4.1624**



# B1L101S, U3-ch117, adc2

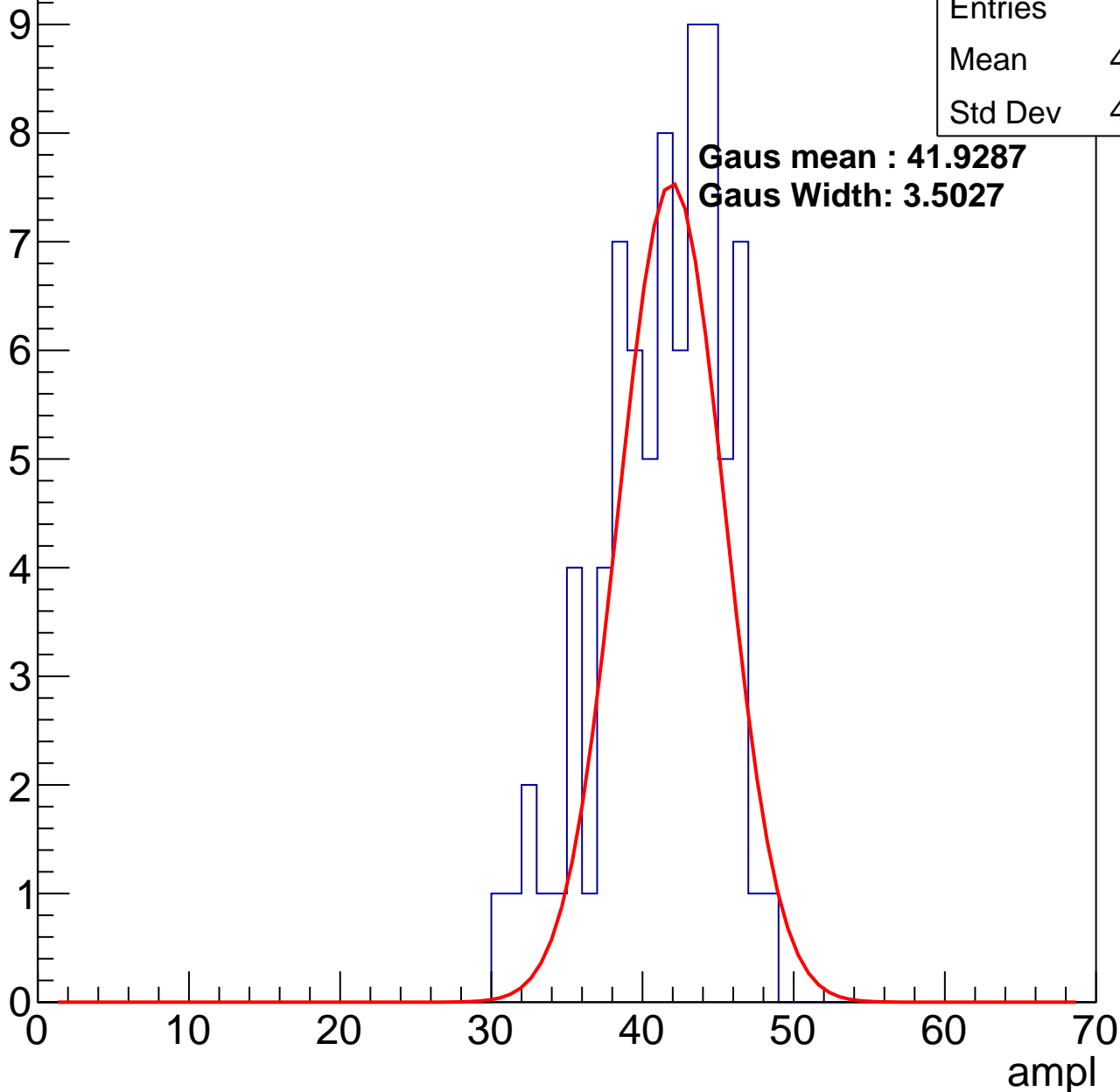
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	40.77
Std Dev	4.025

**Gaus mean : 41.9287**

**Gaus Width: 3.5027**

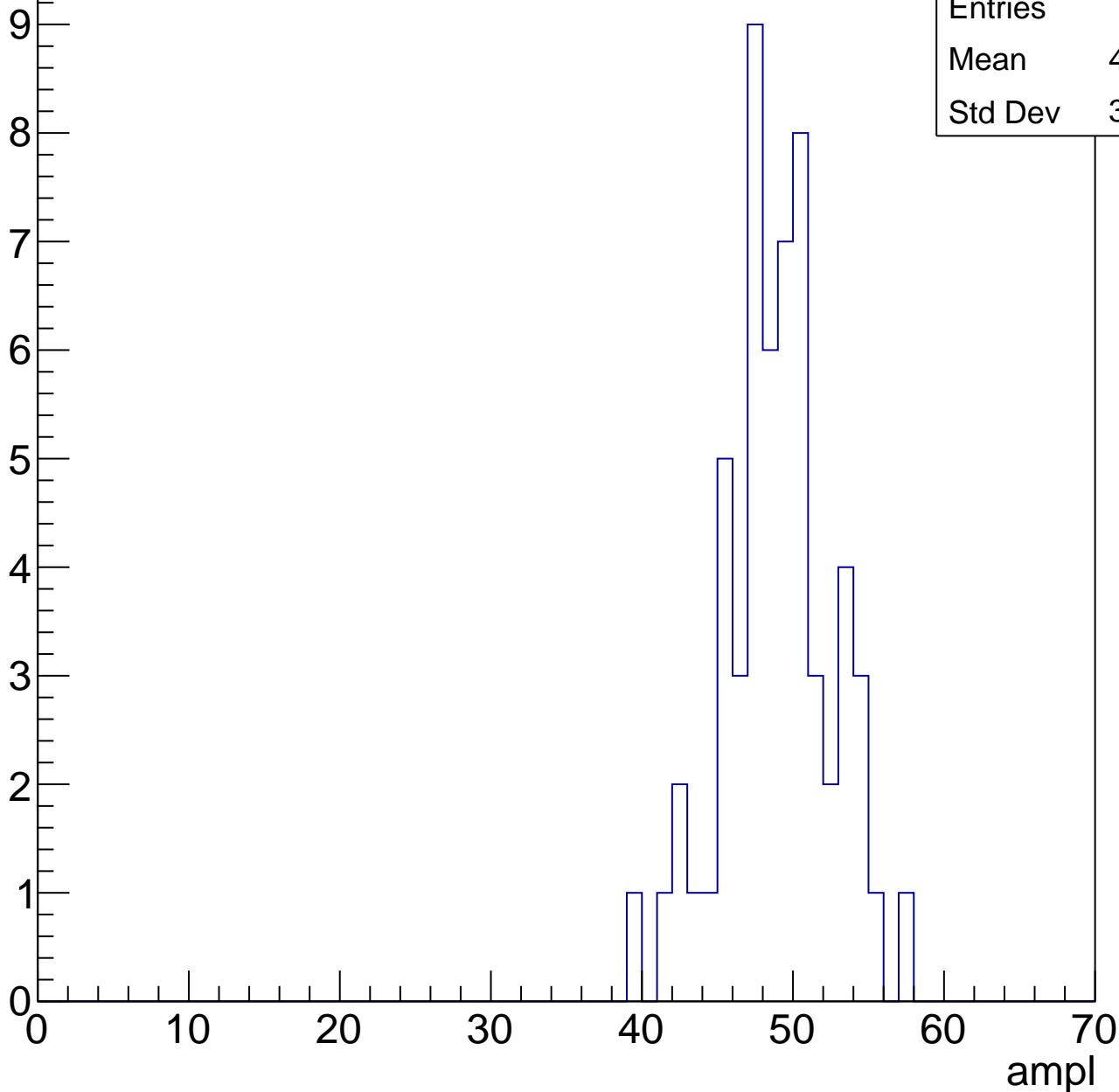


# B1L101S, U3-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

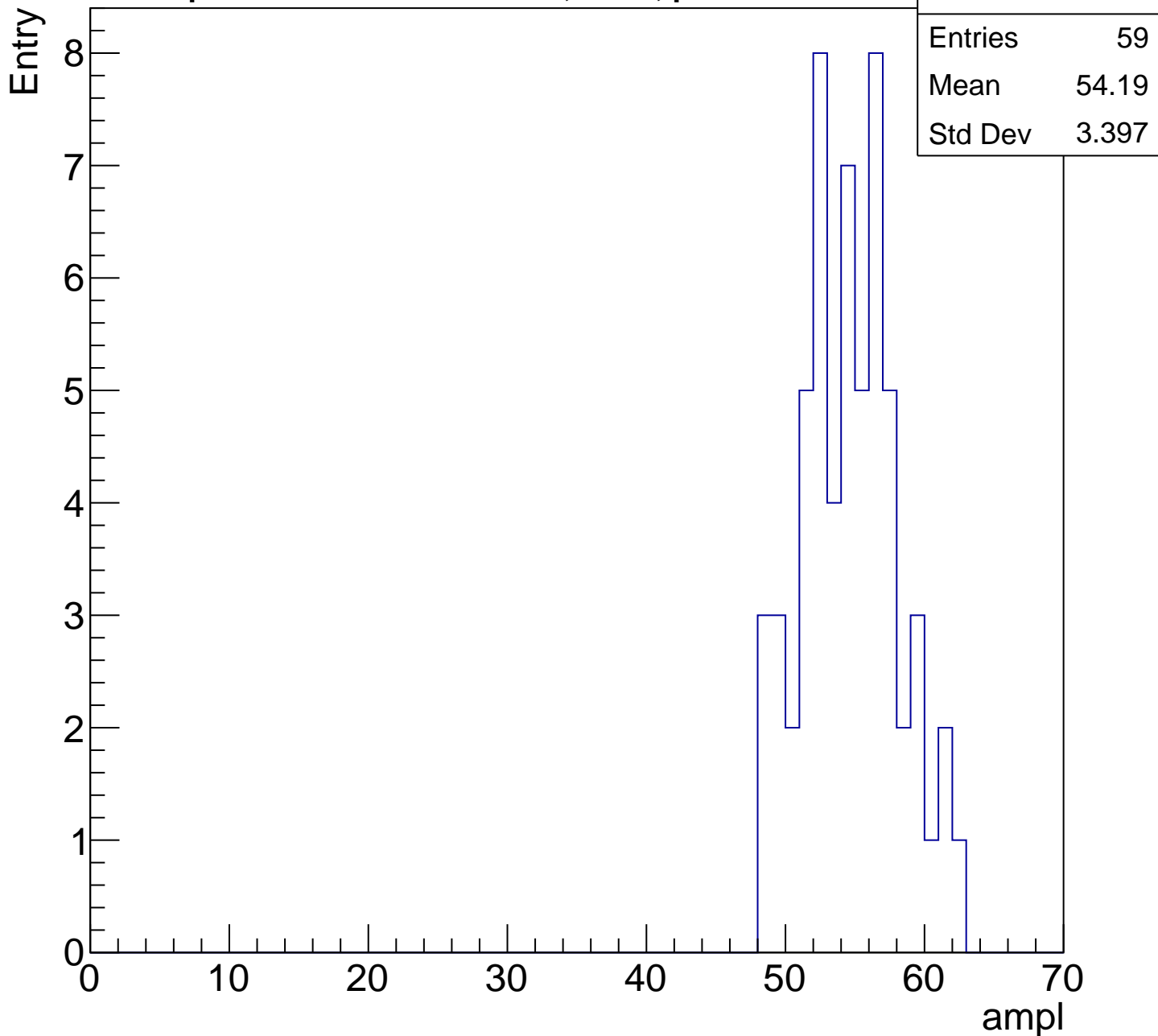
Entry

Entries	58
Mean	48.47
Std Dev	3.554



# B1L101S, U3-ch117, adc4

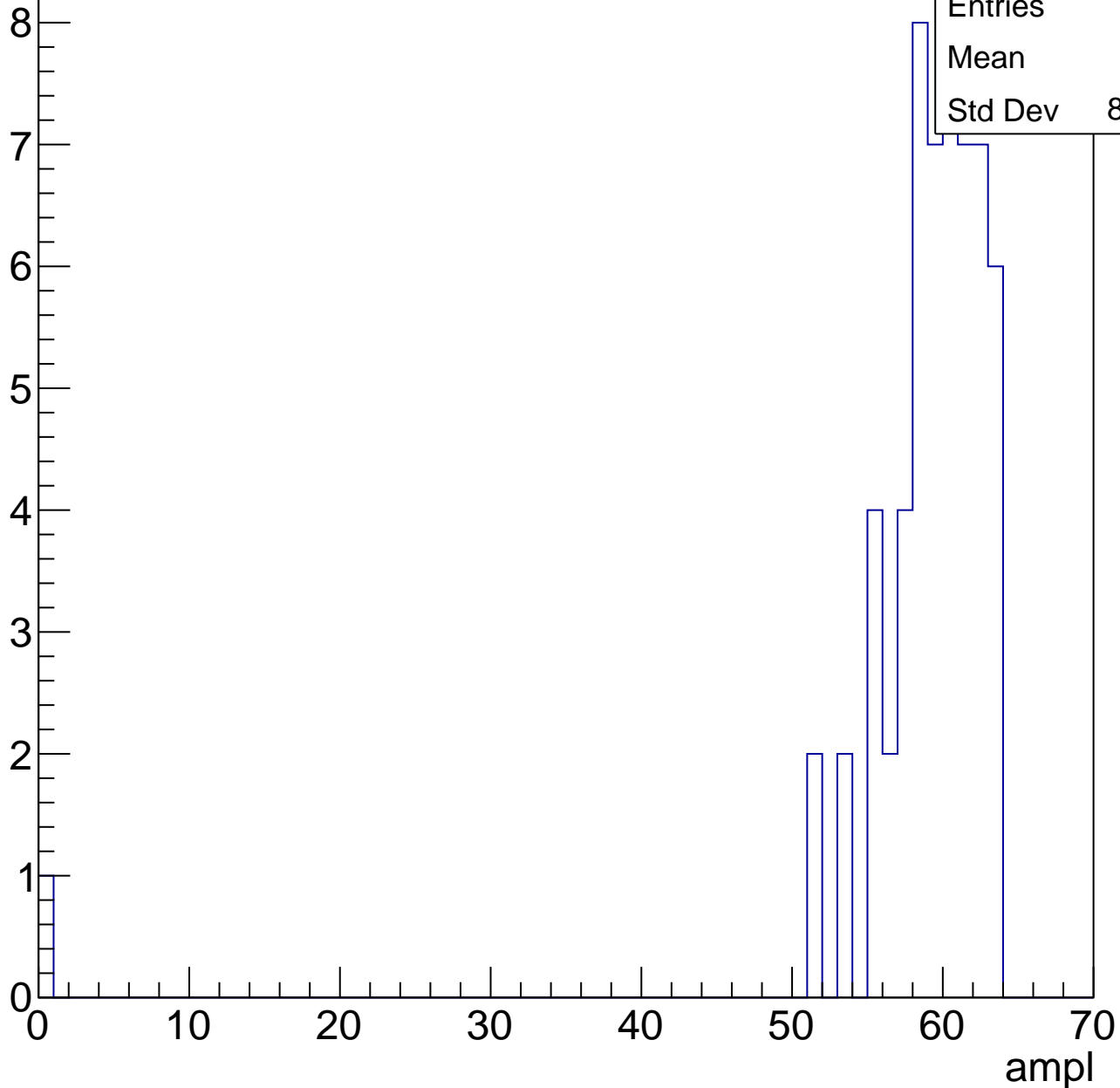
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch118, adc0

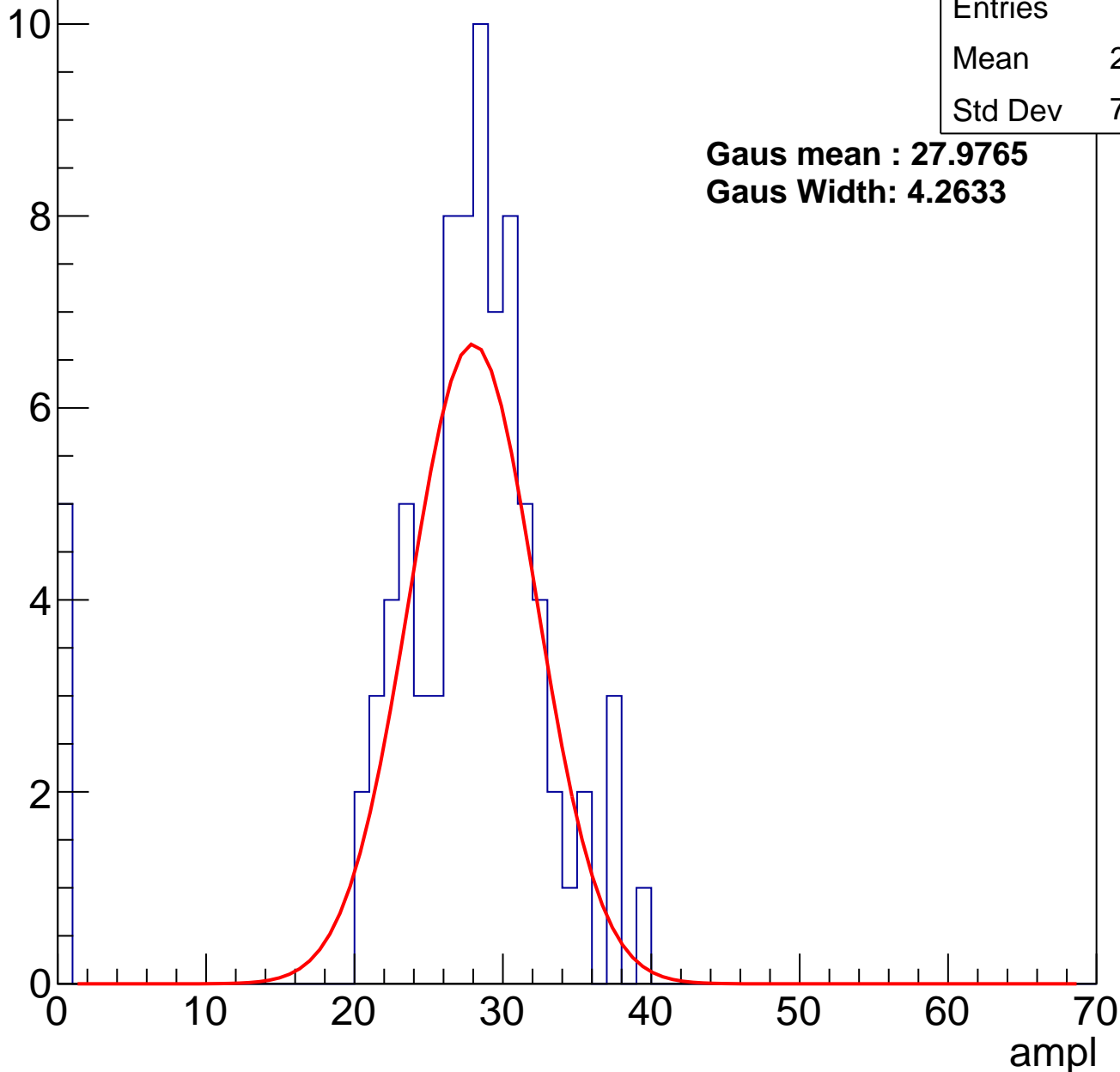
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	84
Mean	26.23
Std Dev	7.723

**Gaus mean : 27.9765**

**Gaus Width: 4.2633**

Entry



# B1L101S, U3-ch118, adc1

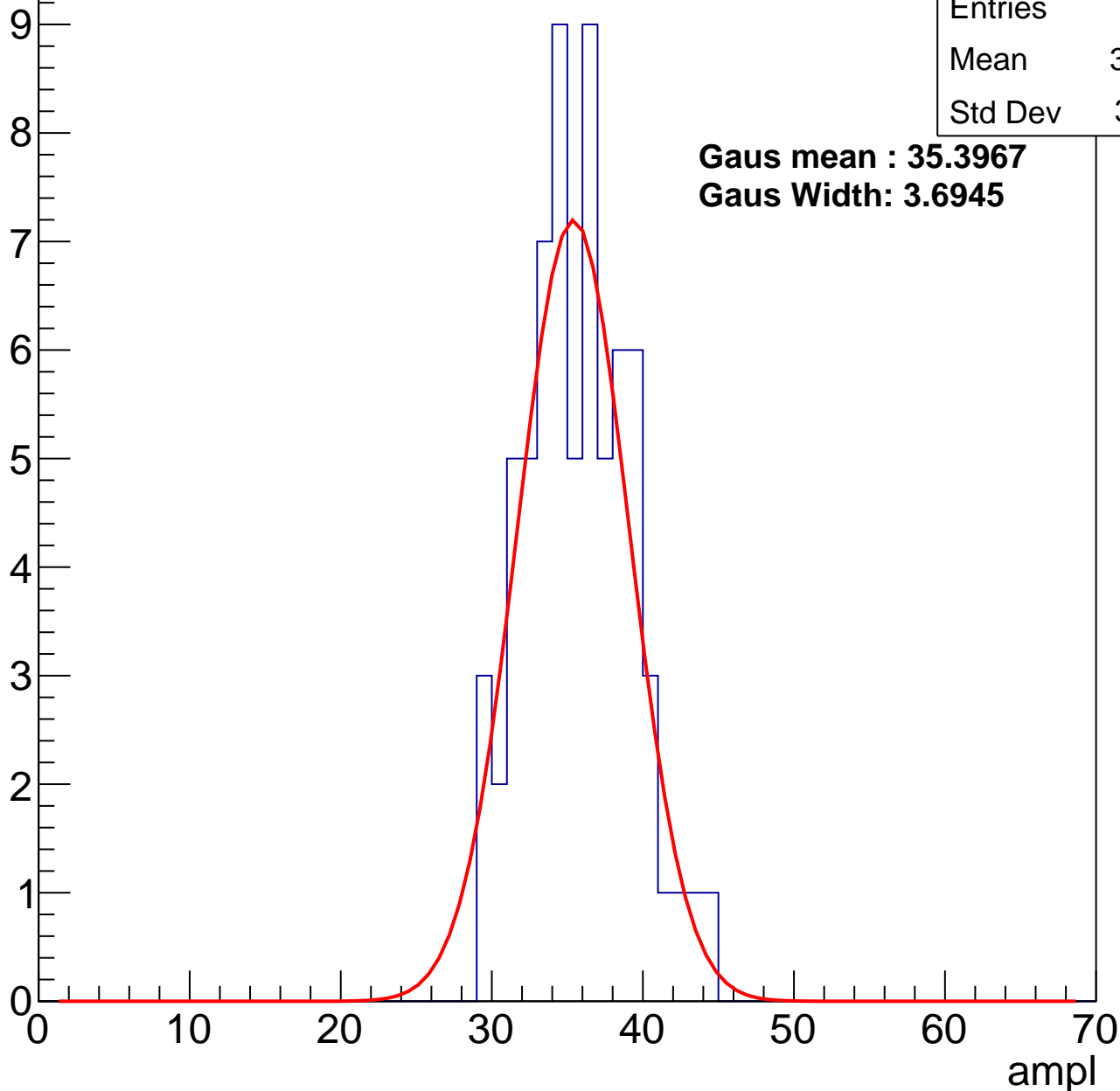
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	69
Mean	35.29
Std Dev	3.401

**Gaus mean : 35.3967**

**Gaus Width: 3.6945**



# B1L101S, U3-ch118, adc2

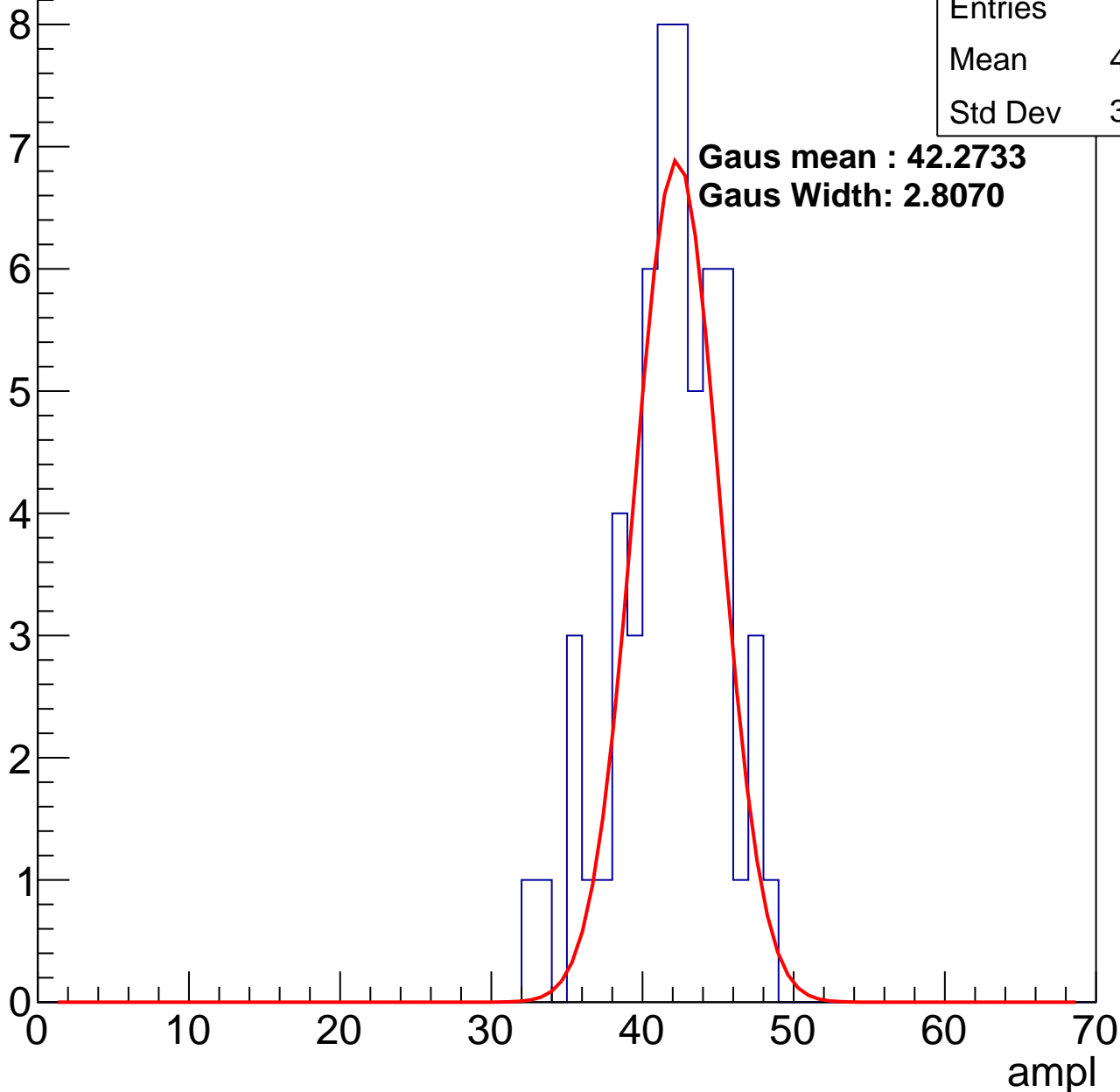
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	41.38
Std Dev	3.473

**Gaus mean : 42.2733**

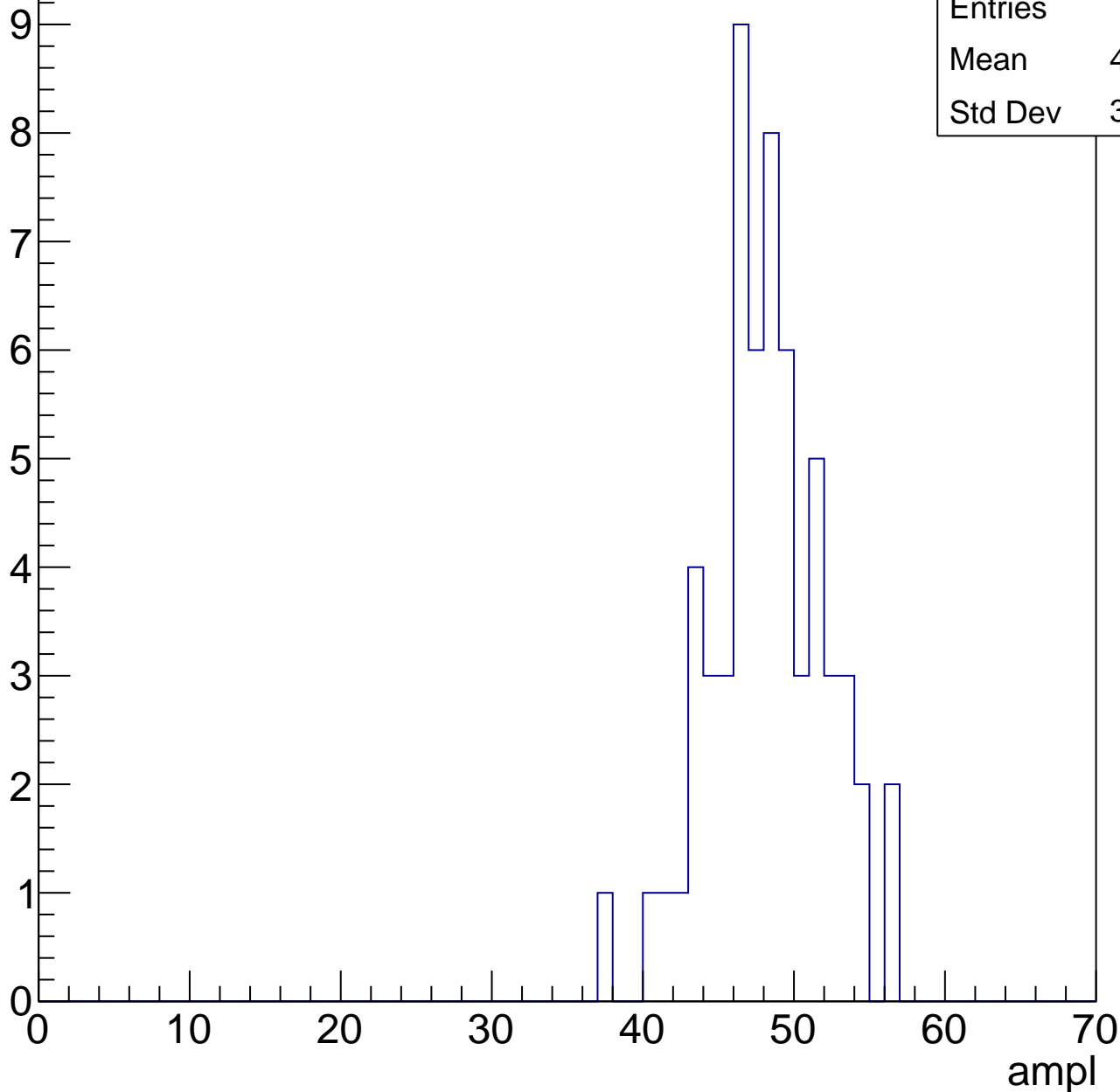
**Gaus Width: 2.8070**



# B1L101S, U3-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



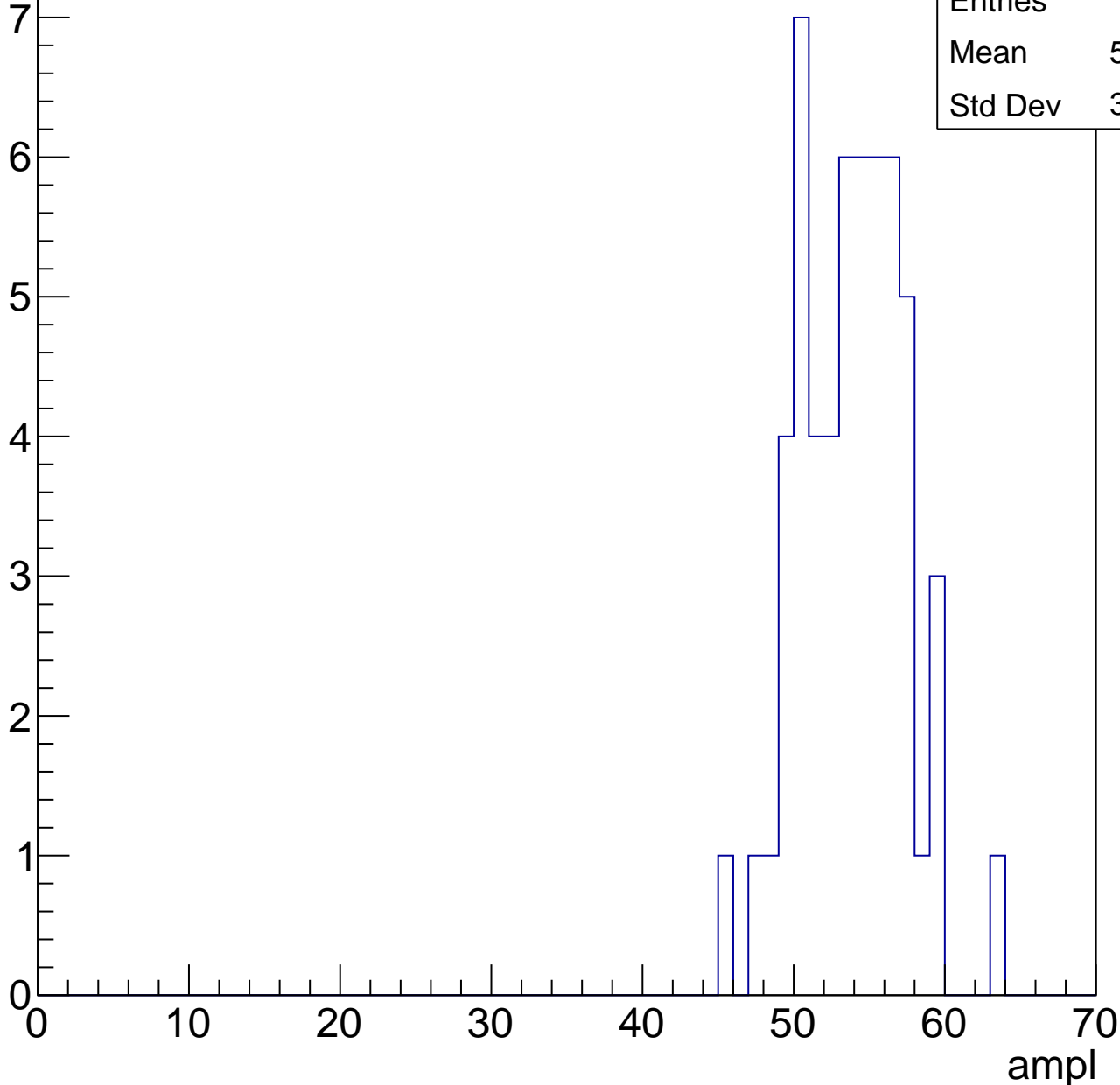
Entries	61
Mean	47.75
Std Dev	3.775

# B1L101S, U3-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	56
Mean	53.38
Std Dev	3.436

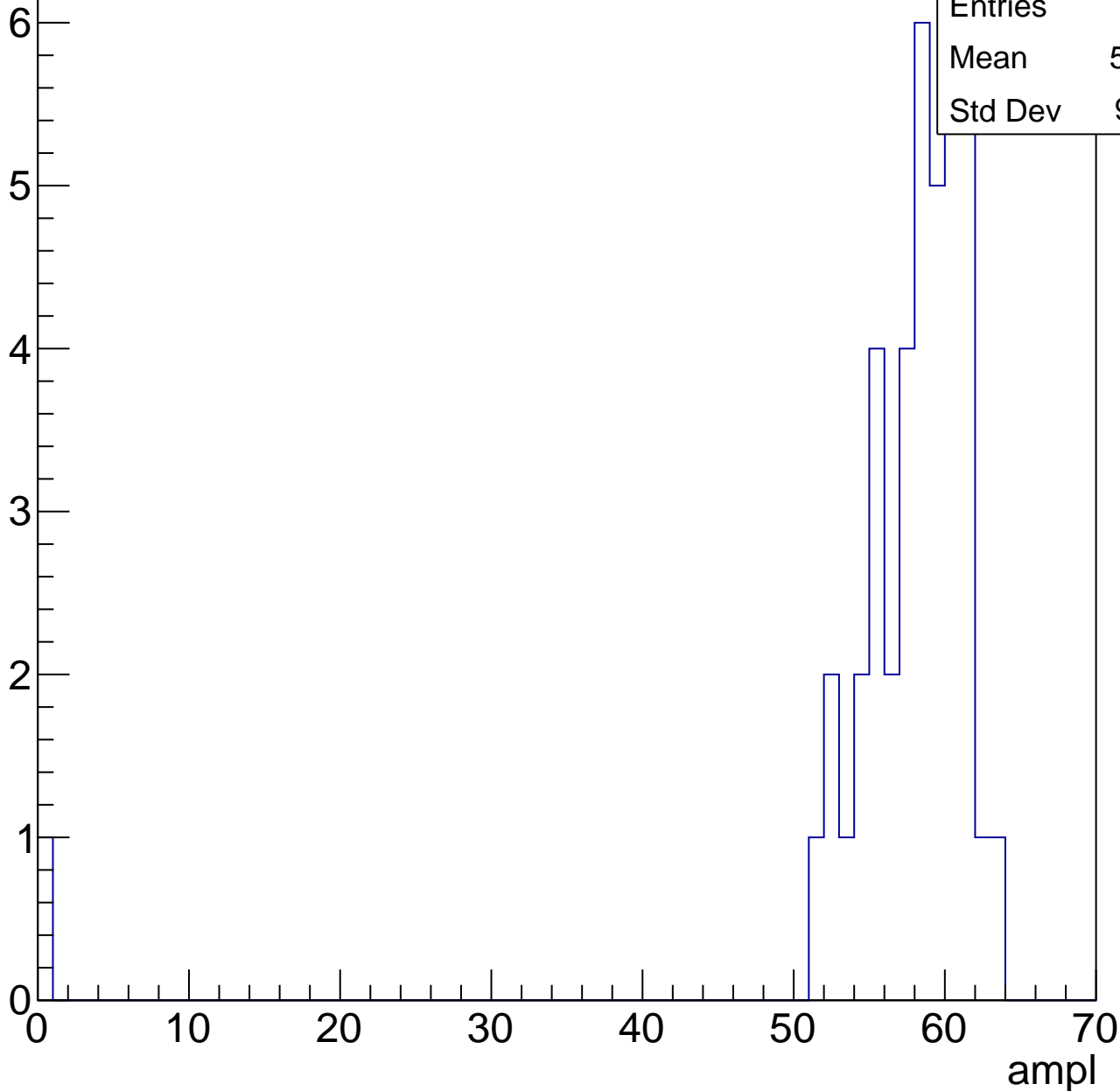


# B1L101S, U3-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	42
Mean	56.43
Std Dev	9.271

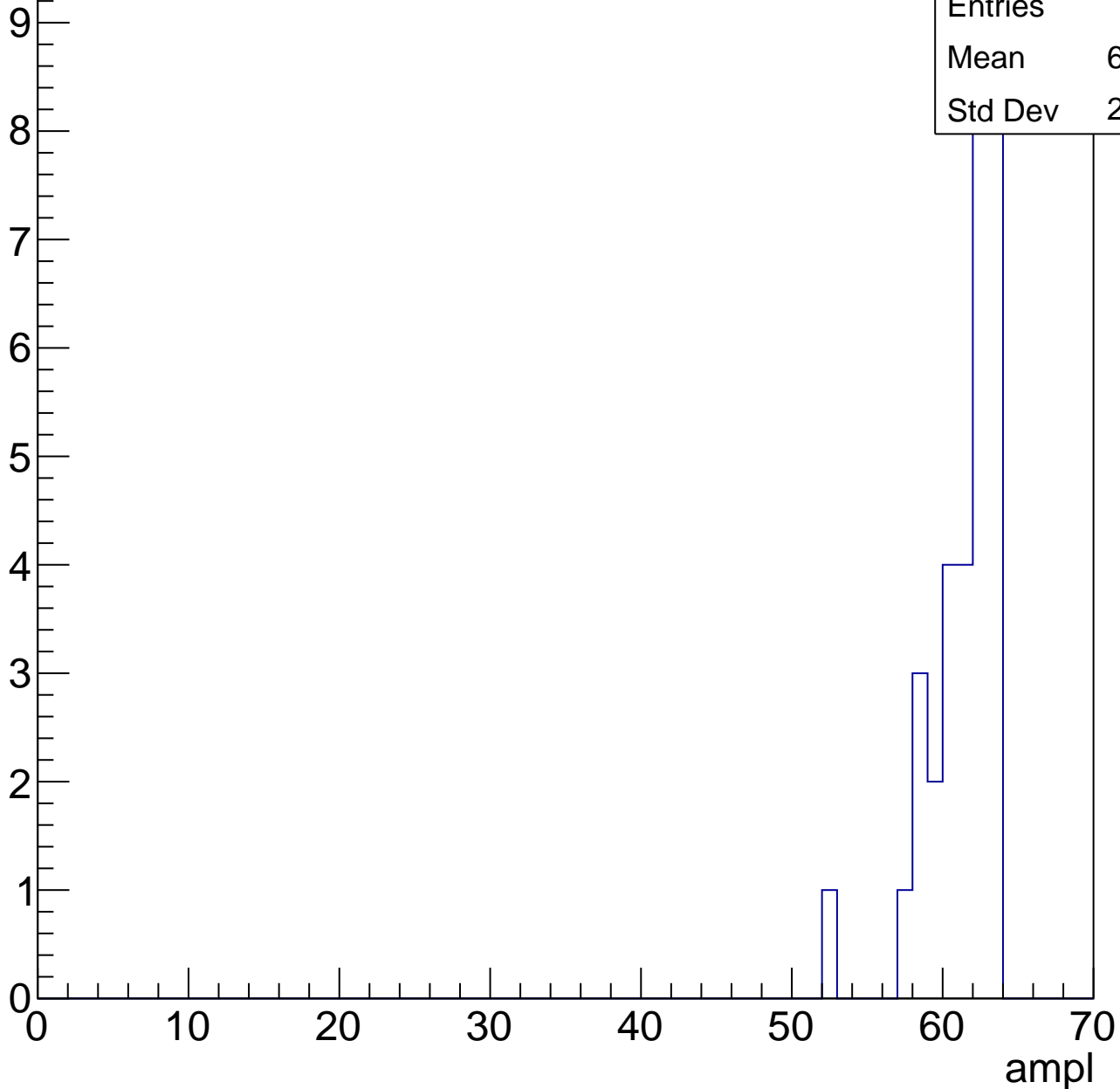


# B1L101S, U3-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	32
Mean	60.84
Std Dev	2.347





# B1L101S, U3-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U3-ch119, adc0

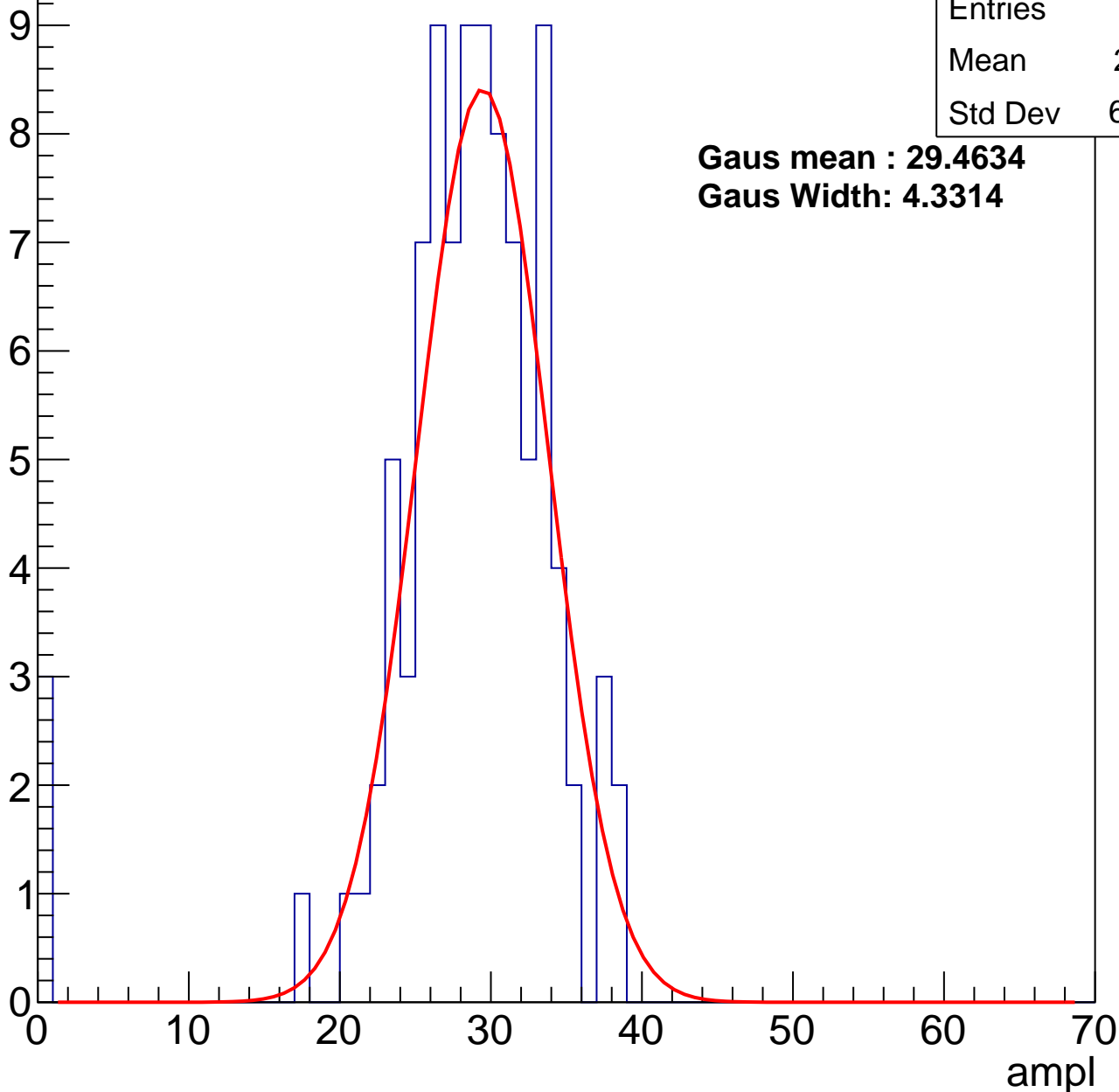
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	97
Mean	27.91
Std Dev	6.446

**Gaus mean : 29.4634**

**Gaus Width: 4.3314**



# B1L101S, U3-ch119, adc1

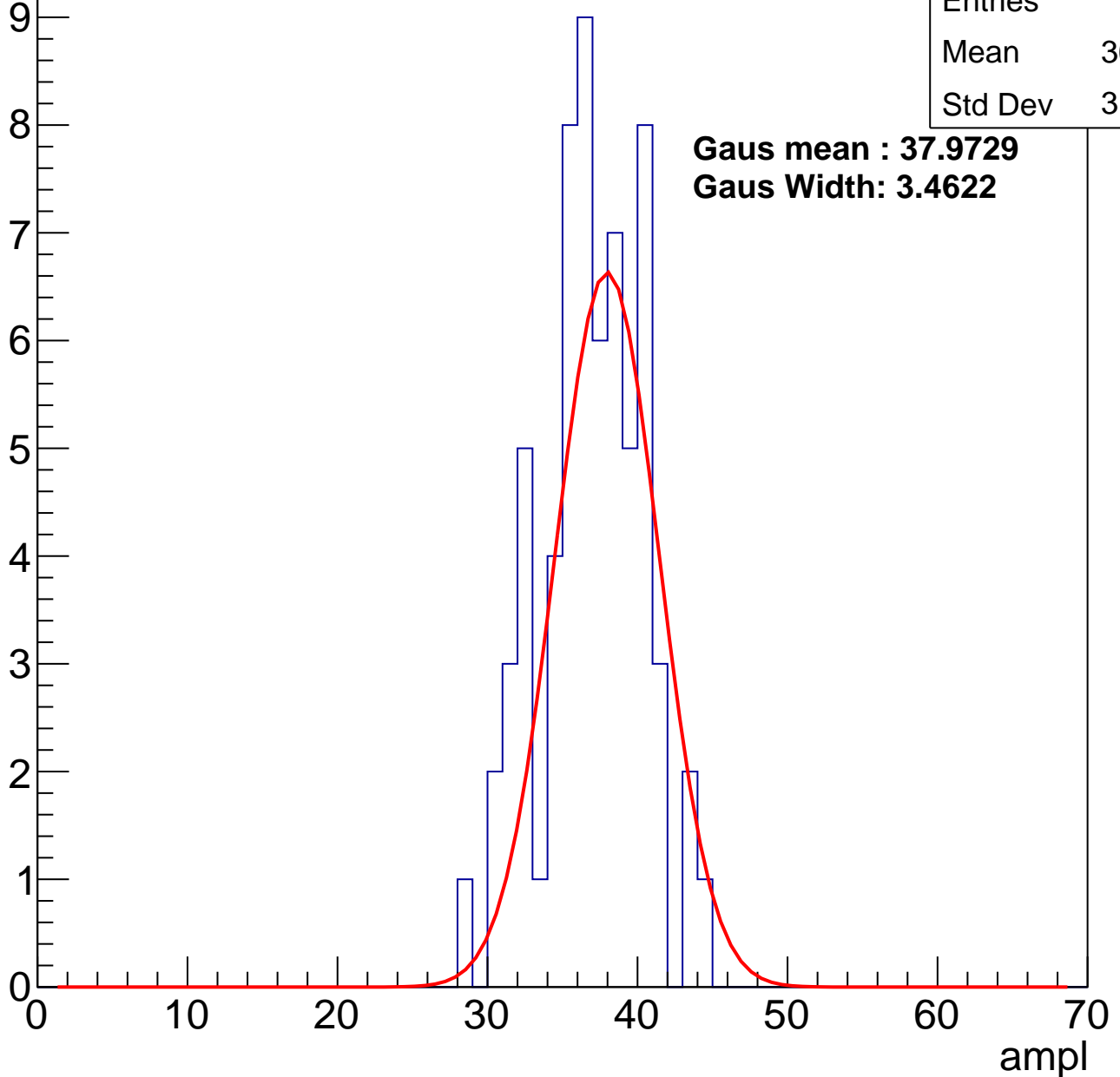
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	36.46
Std Dev	3.406

**Gaus mean : 37.9729**

**Gaus Width: 3.4622**



# B1L101S, U3-ch119, adc2

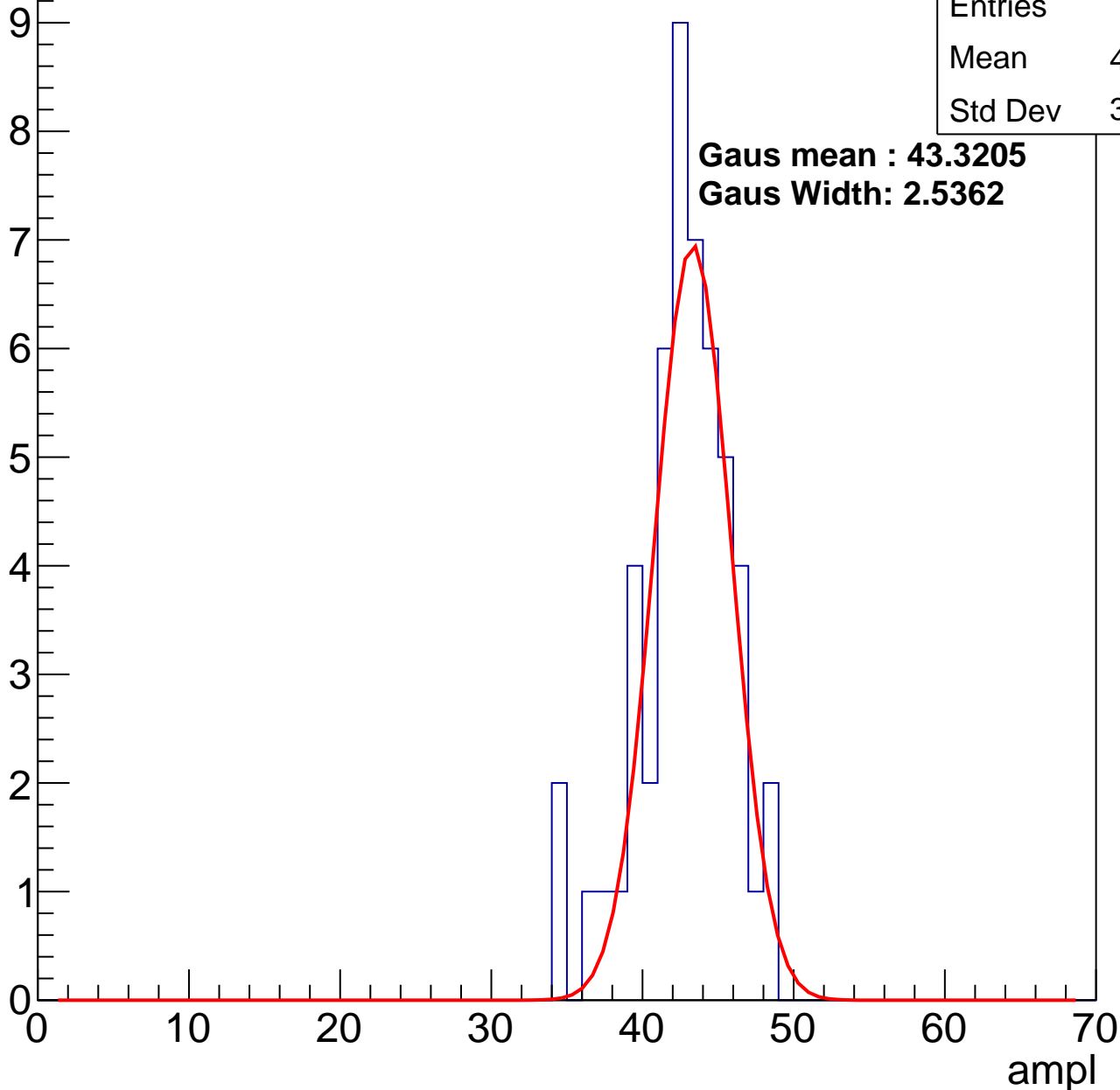
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	42.27
Std Dev	3.094

**Gaus mean : 43.3205**

**Gaus Width: 2.5362**

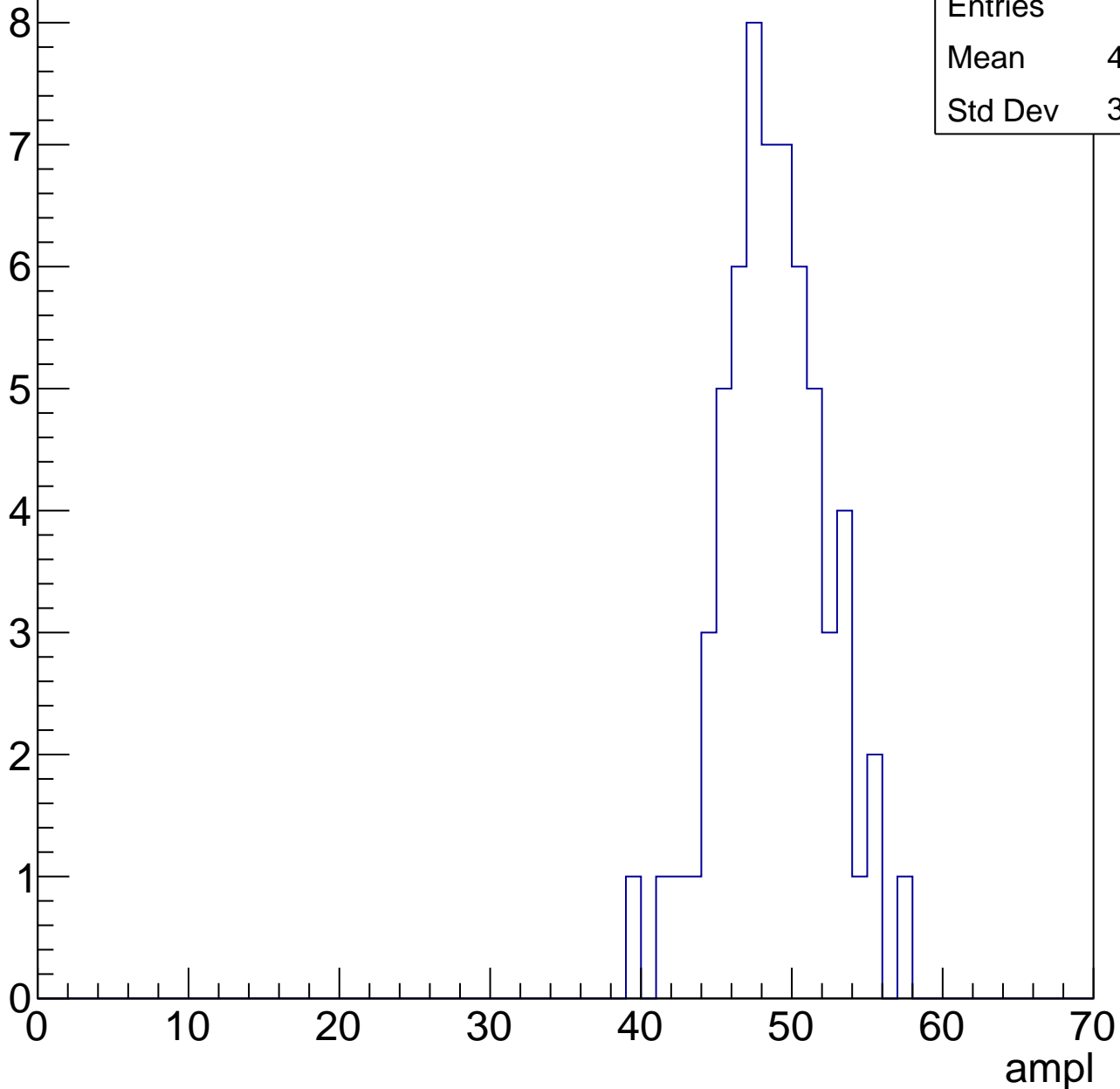


# B1L101S, U3-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	48.34
Std Dev	3.473

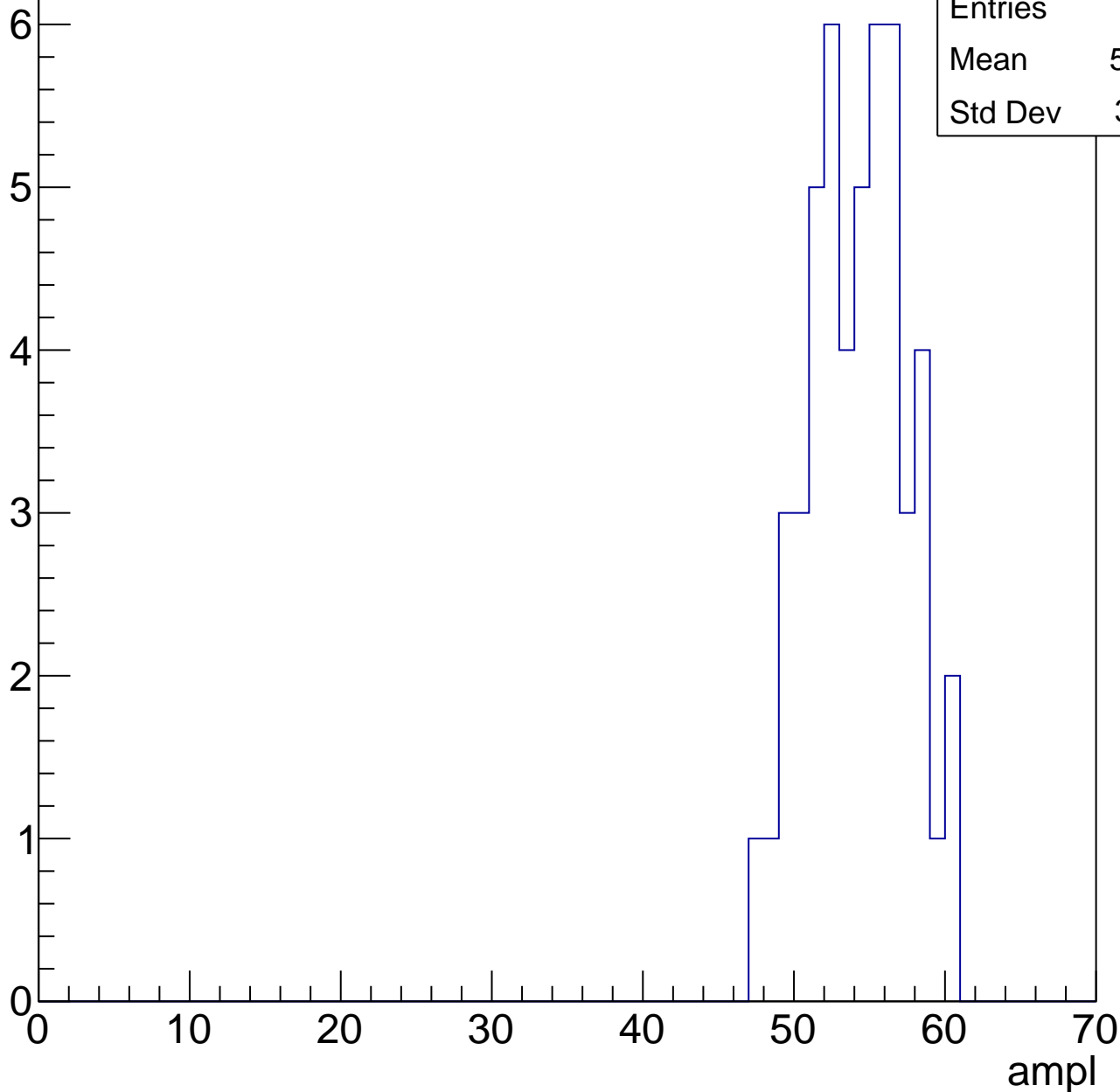


# B1L101S, U3-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	53.78
Std Dev	3.151

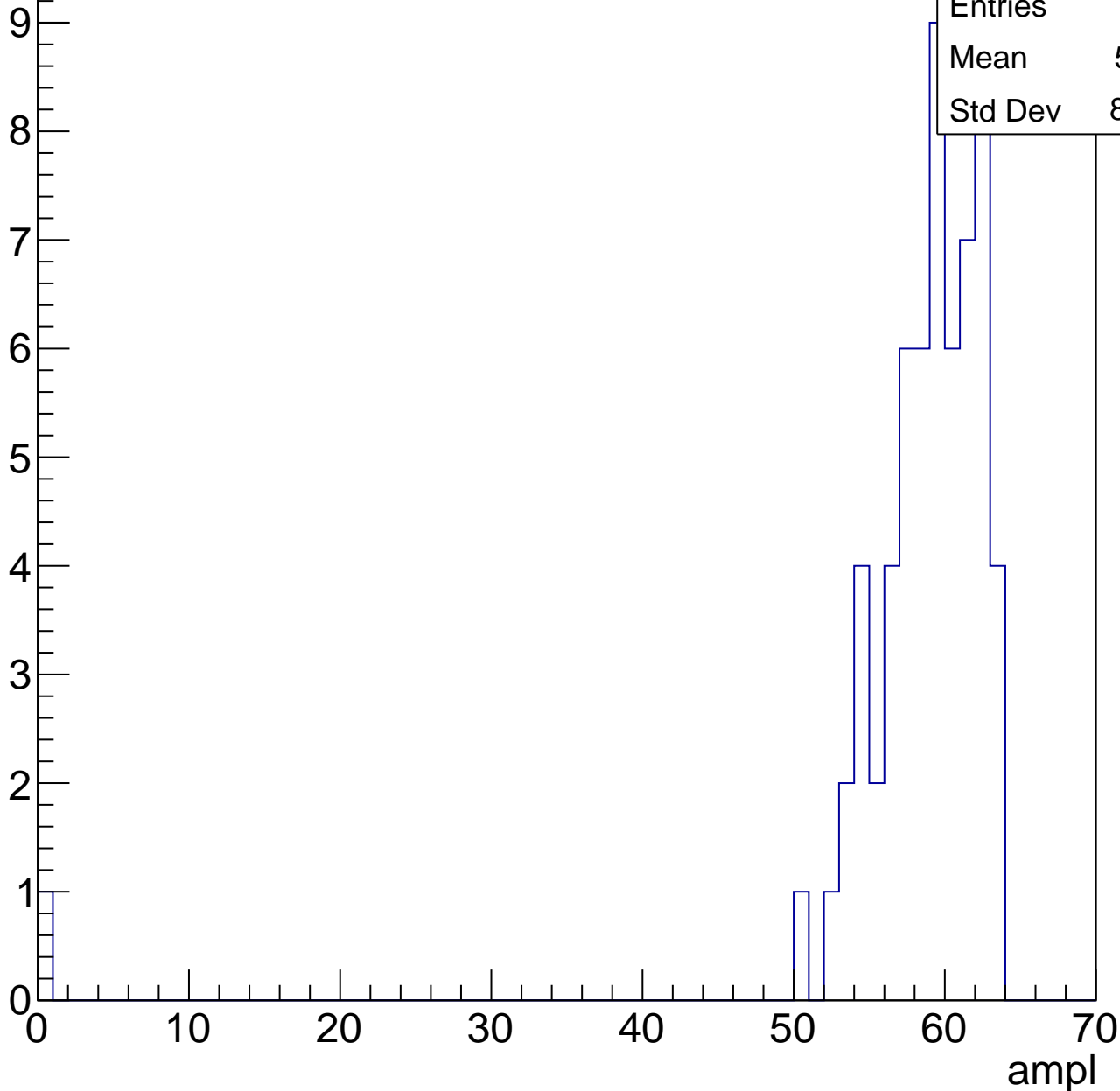


# B1L101S, U3-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	61
Mean	57.61
Std Dev	8.029

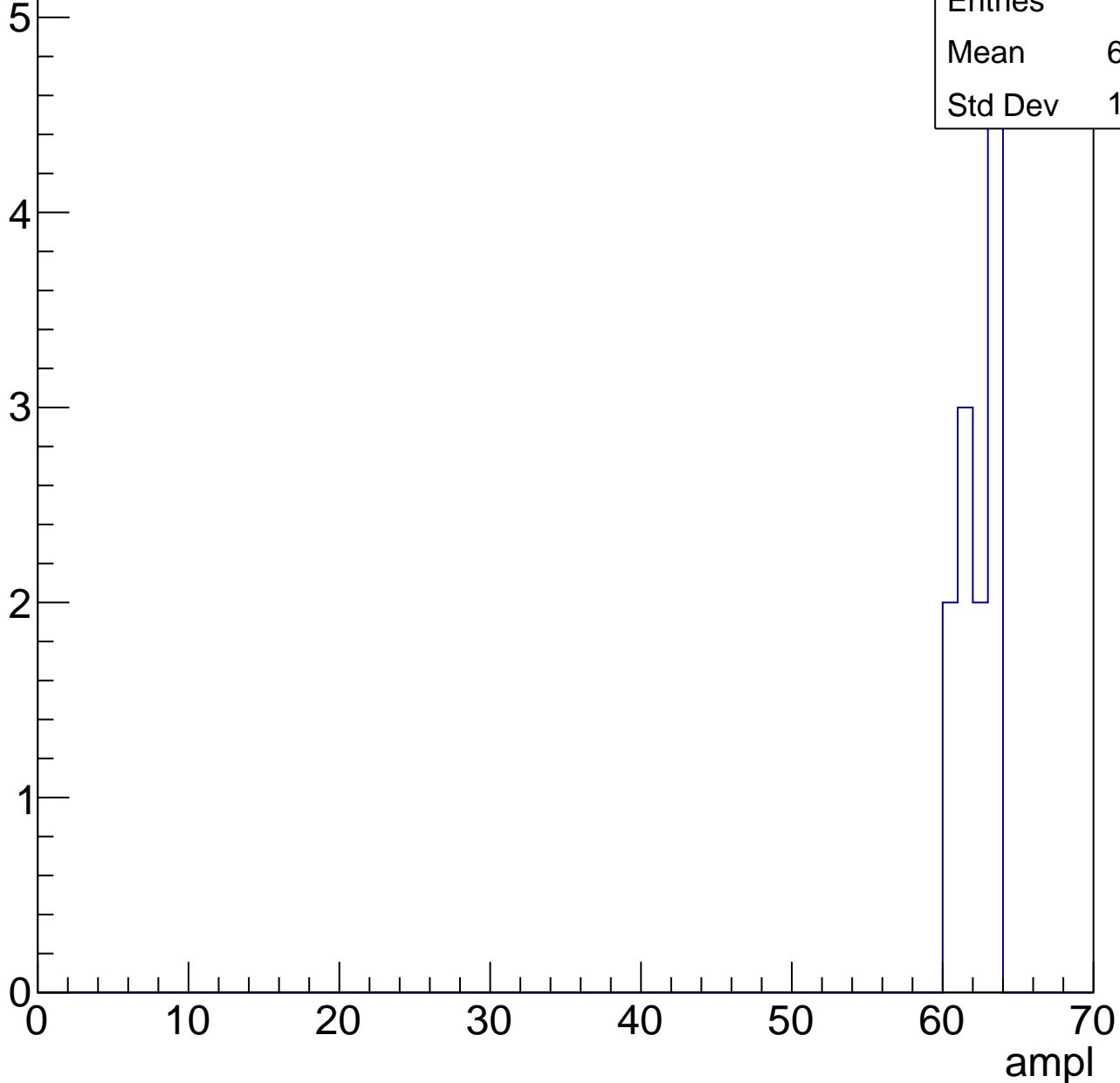


# B1L101S, U3-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	12
Mean	61.83
Std Dev	1.143

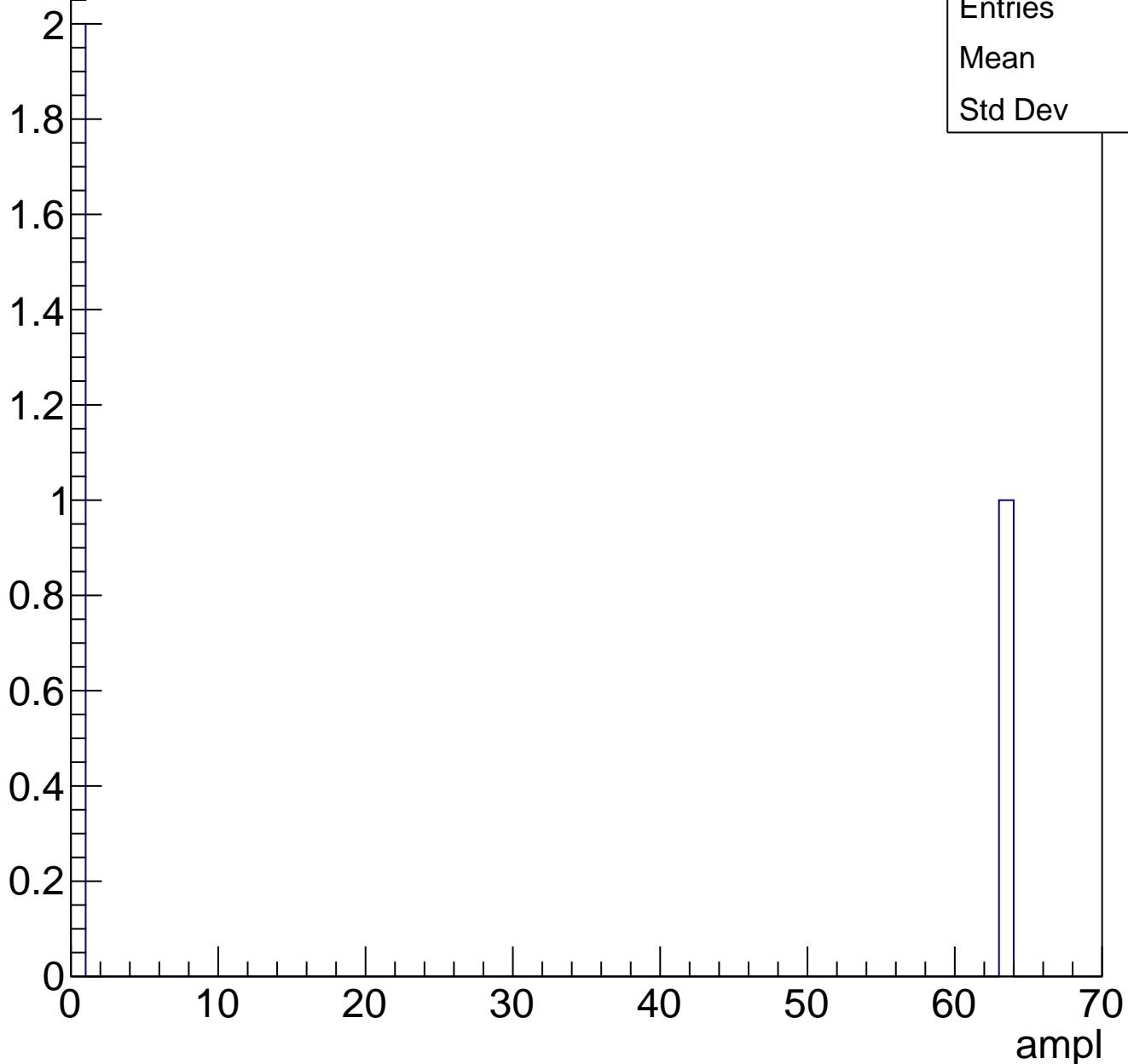




# B1L101S, U3-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L101S, U3-ch120, adc0

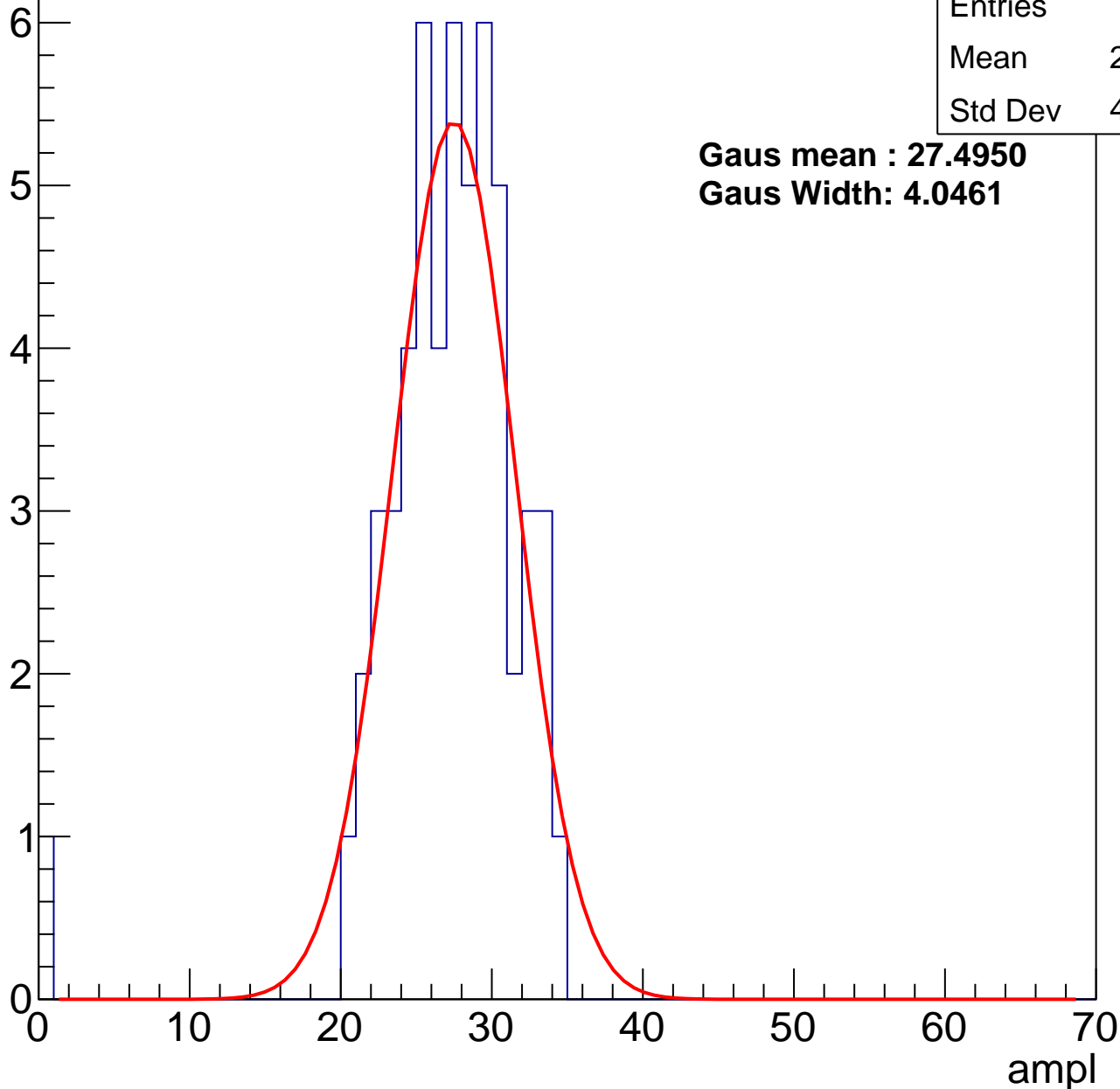
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	26.62
Std Dev	4.985

**Gaus mean : 27.4950**

**Gaus Width: 4.0461**



# B1L101S, U3-ch120, adc1

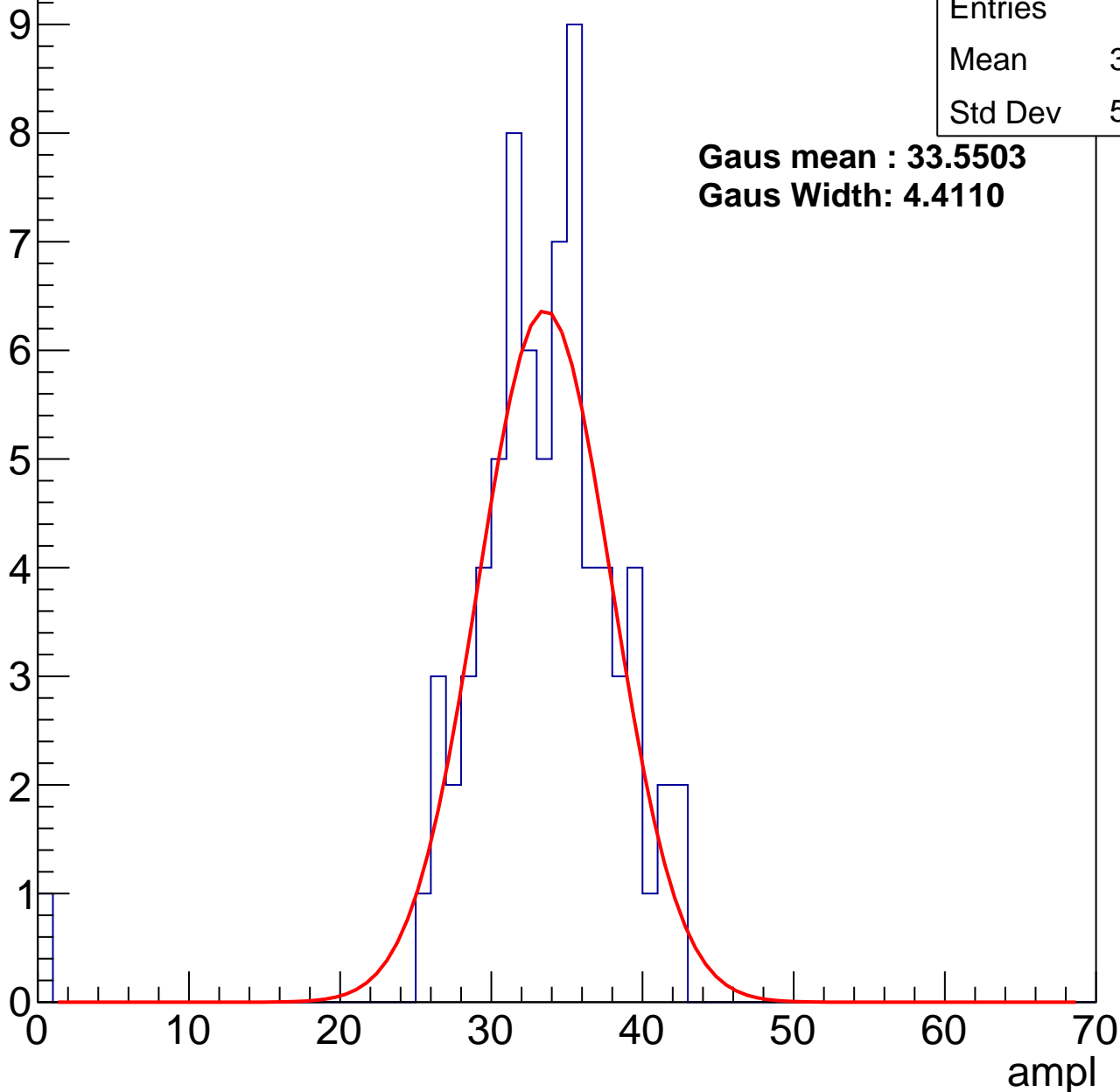
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	74
Mean	32.88
Std Dev	5.568

**Gaus mean : 33.5503**

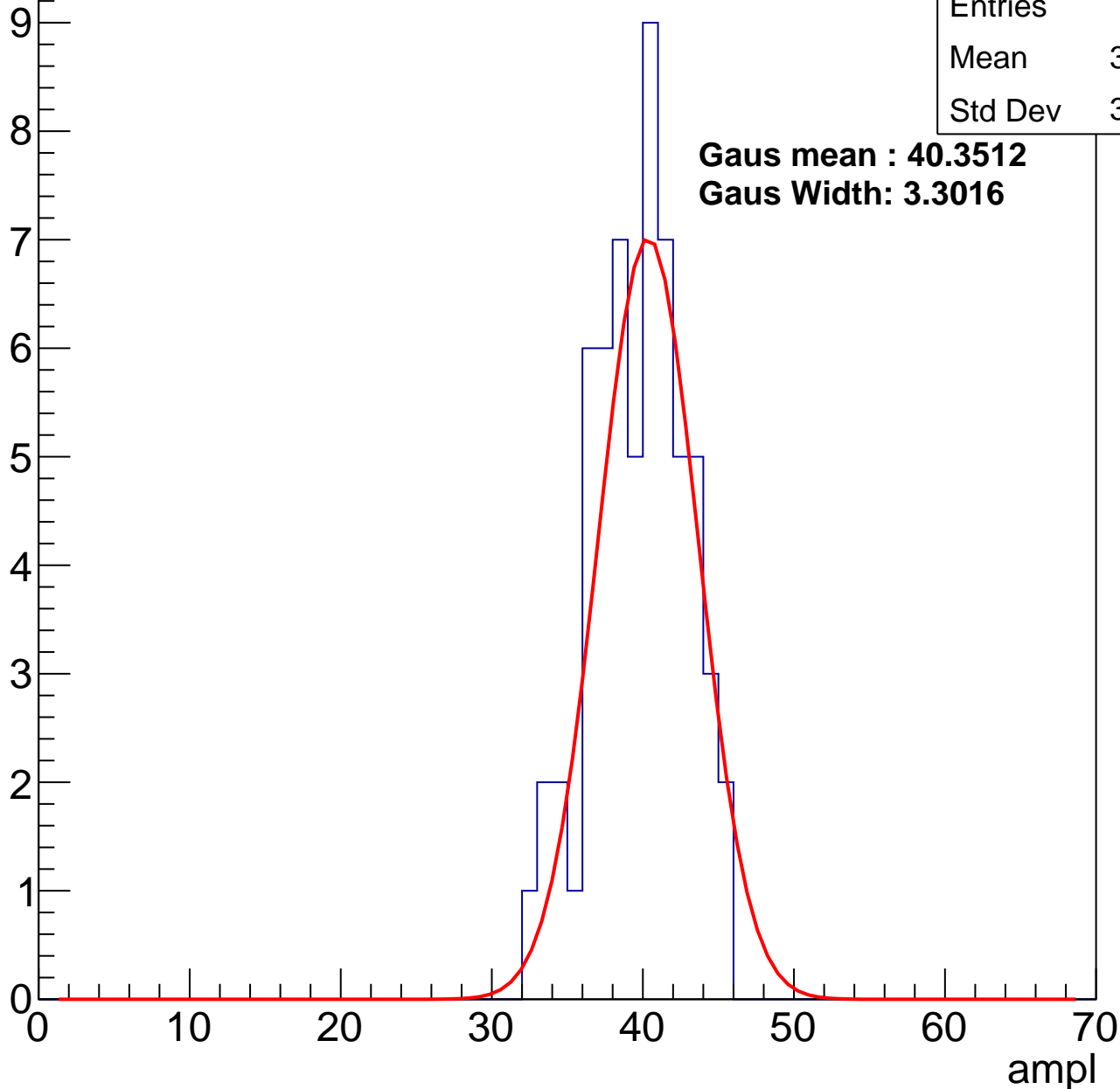
**Gaus Width: 4.4110**



# B1L101S, U3-ch120, adc2

calib\_packv5\_042523\_0143.root, FC#0, port D2

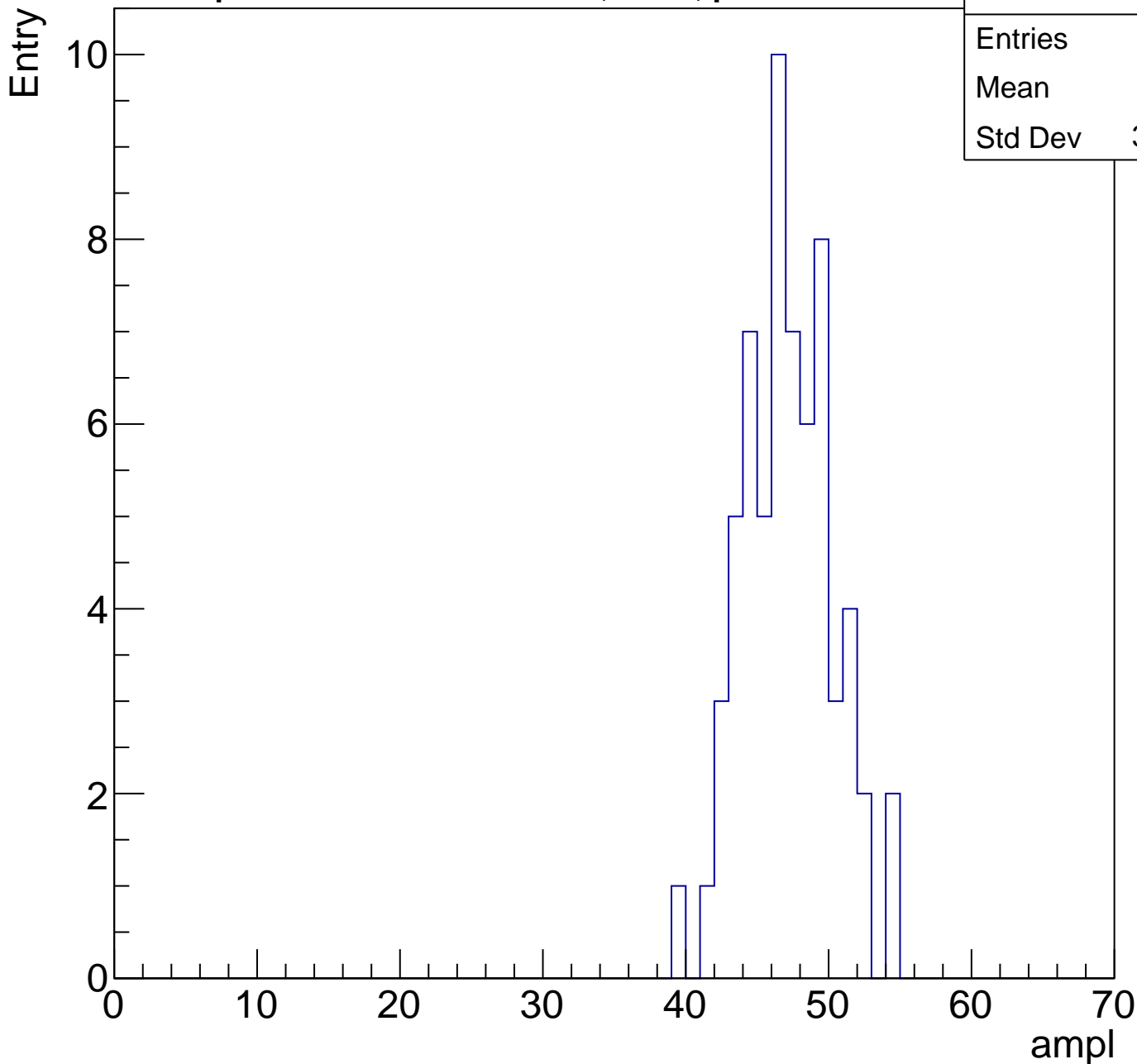
Entry



# B1L101S, U3-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	64
Mean	46.7
Std Dev	3.111

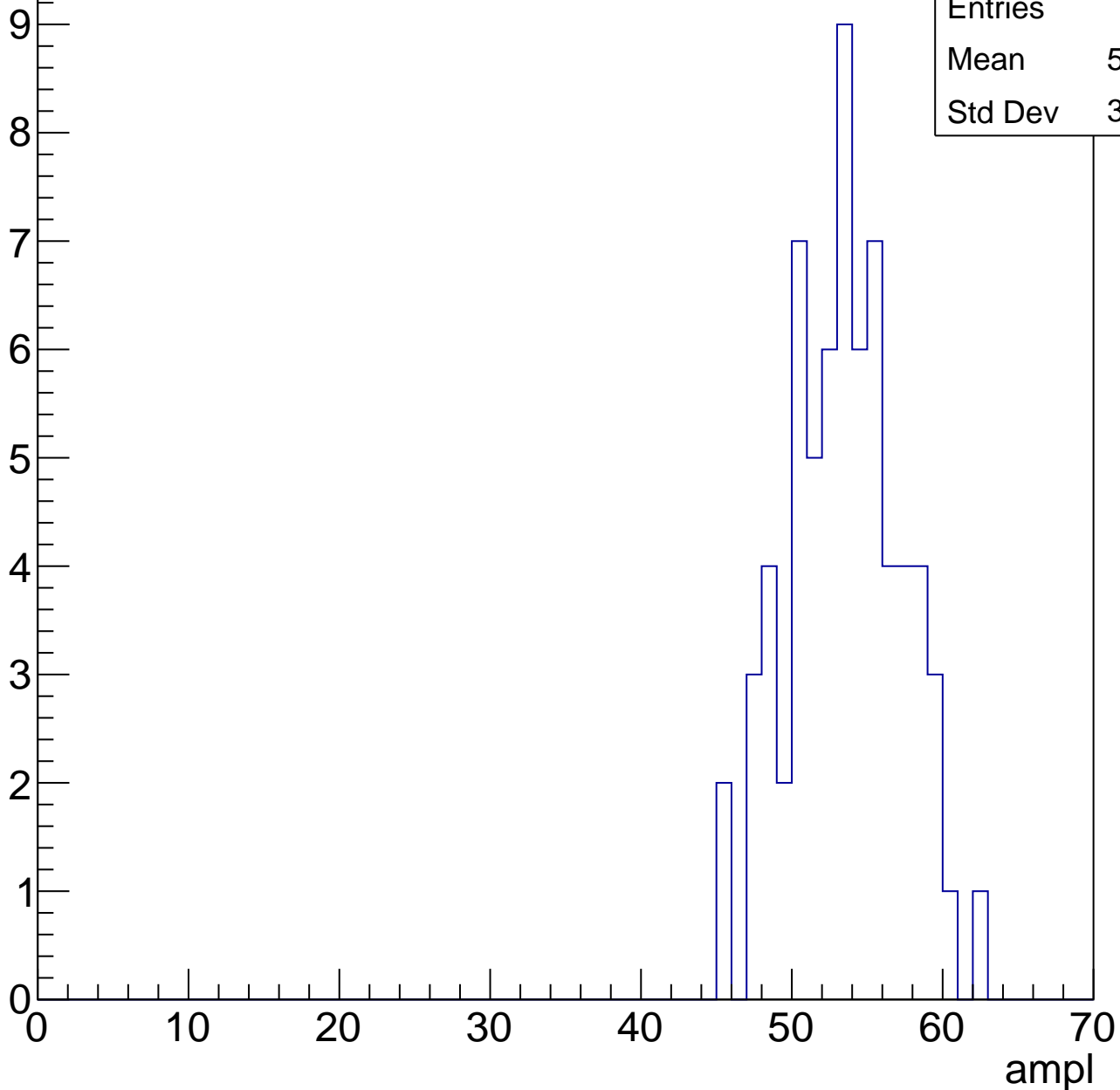


# B1L101S, U3-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	53.04
Std Dev	3.696

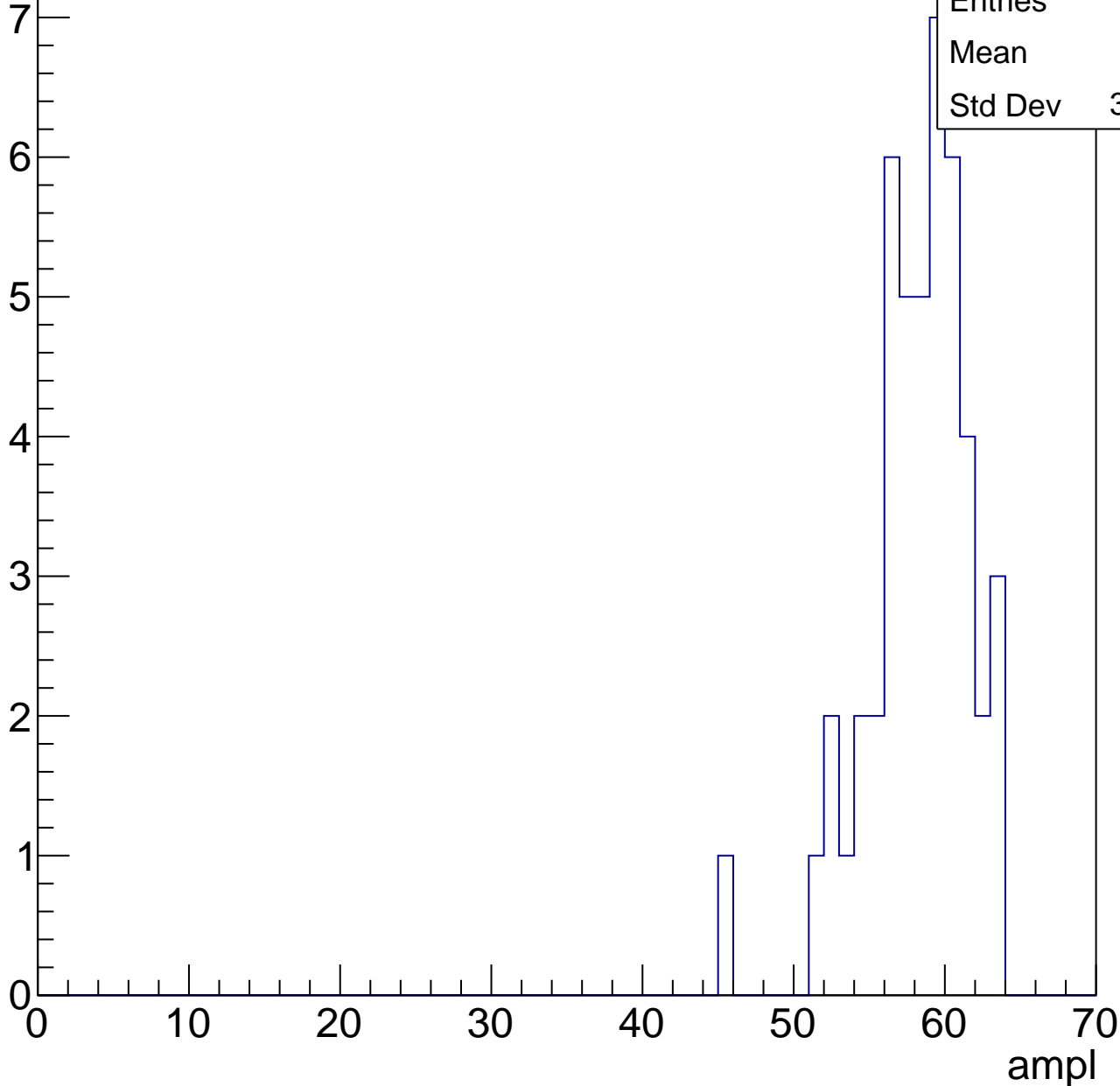


# B1L101S, U3-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	57.7
Std Dev	3.464

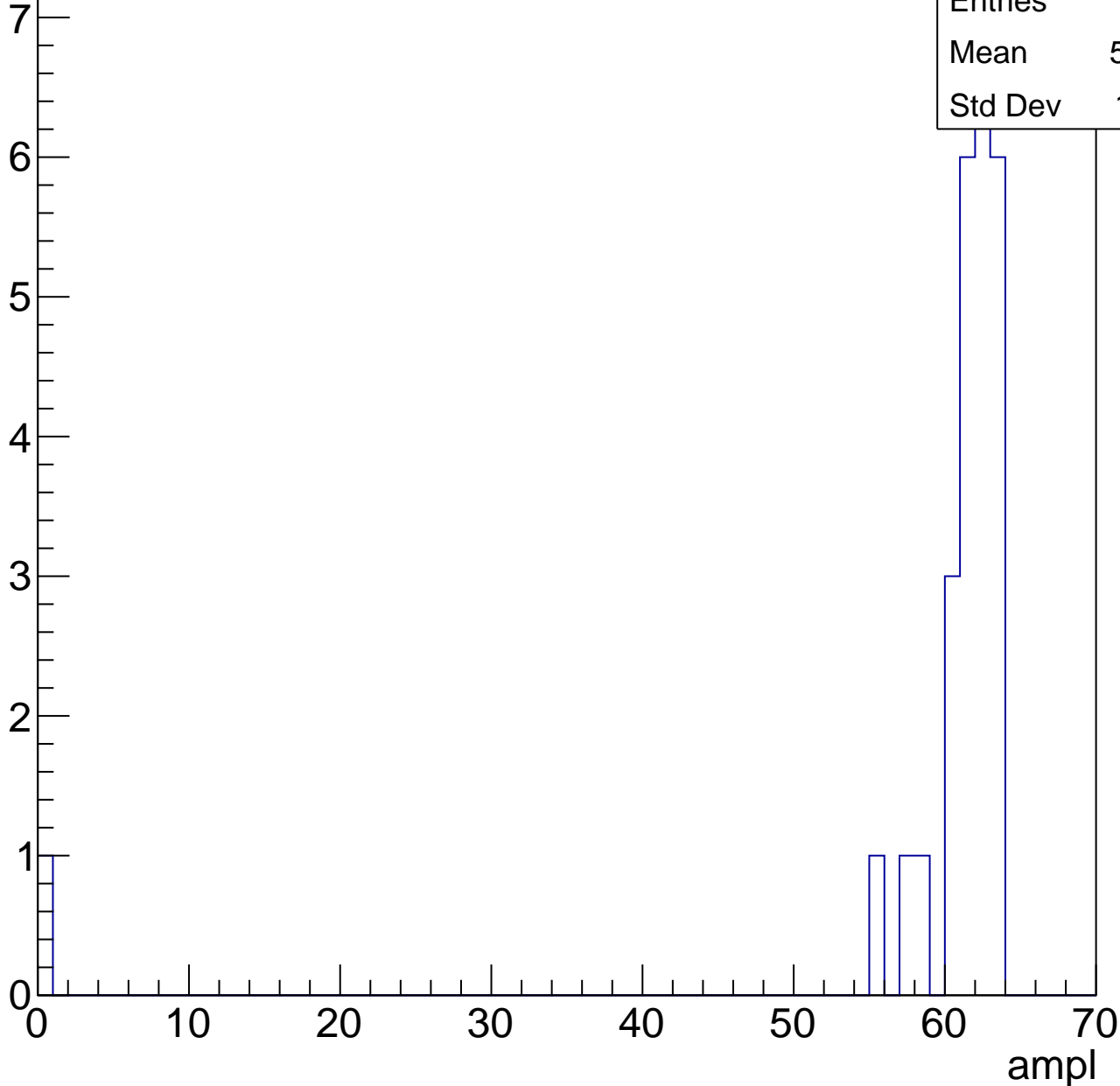


# B1L101S, U3-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	26
Mean	58.77
Std Dev	11.91





# B1L101S, U3-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	1
Mean	63
Std Dev	0

# B1L101S, U3-ch121, adc0

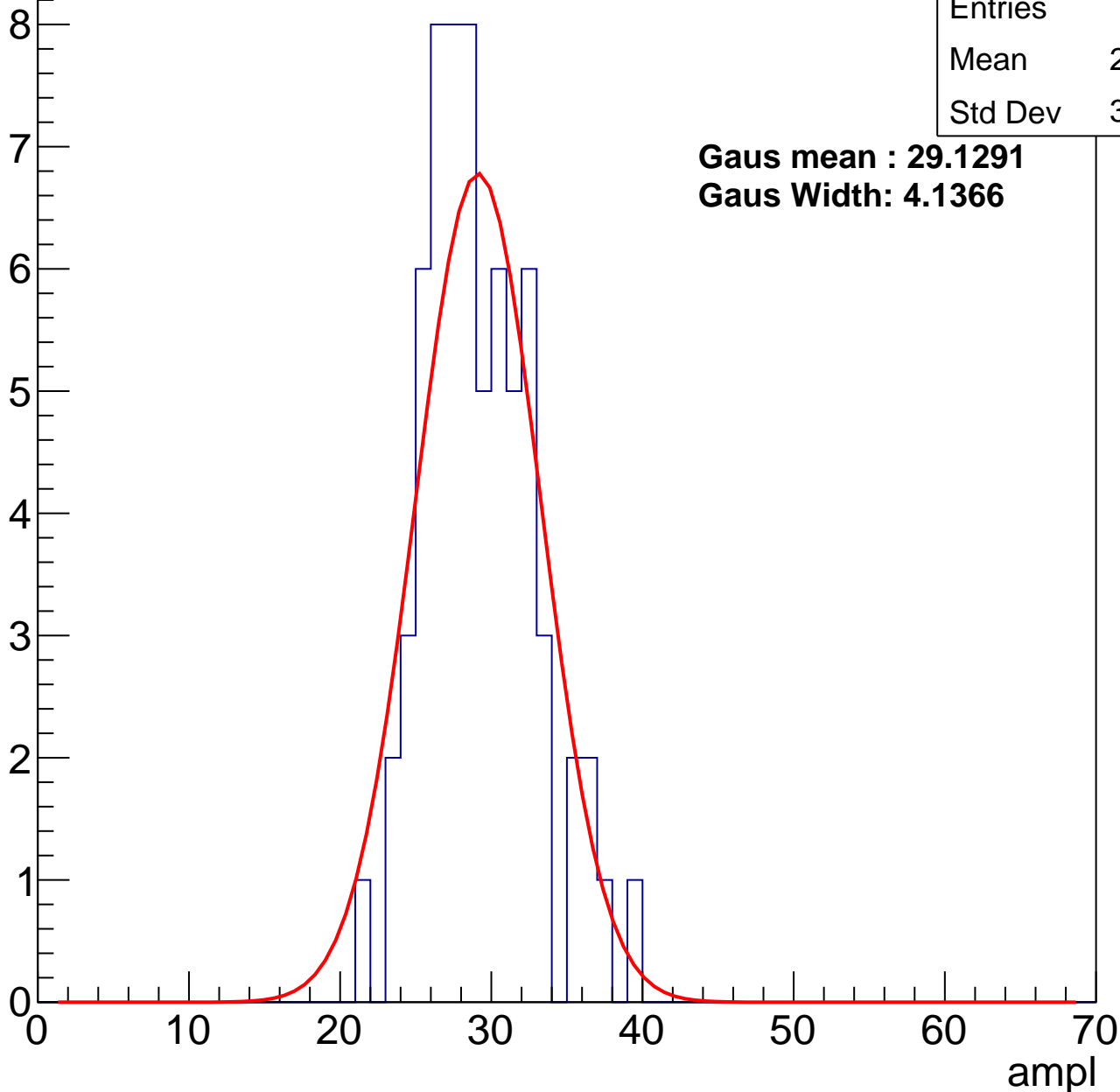
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	28.75
Std Dev	3.617

**Gaus mean : 29.1291**

**Gaus Width: 4.1366**



# B1L101S, U3-ch121, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	76
Mean	34.96
Std Dev	3.726

**Gaus mean : 34.8535**

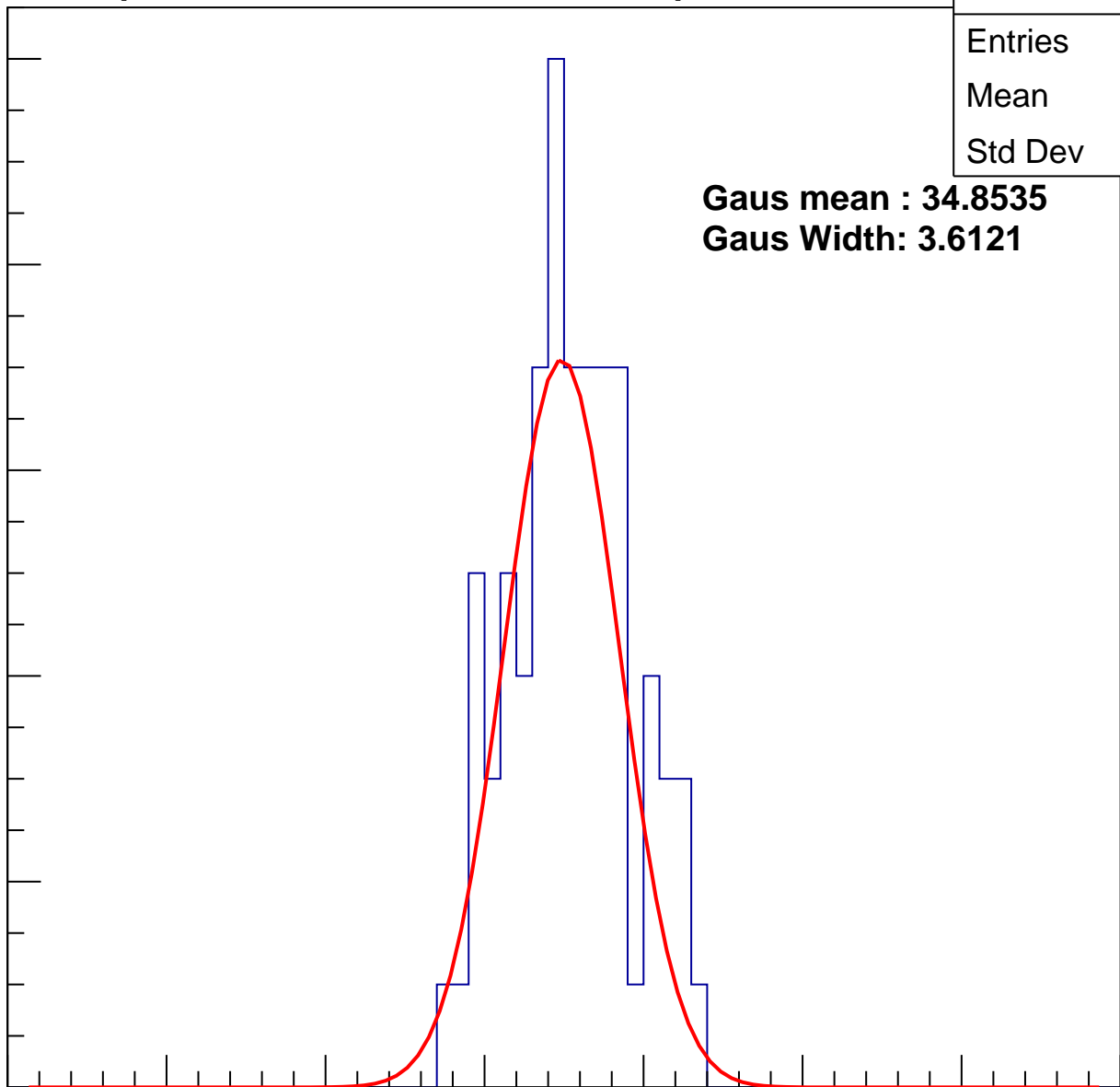
**Gaus Width: 3.6121**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U3-ch121, adc2

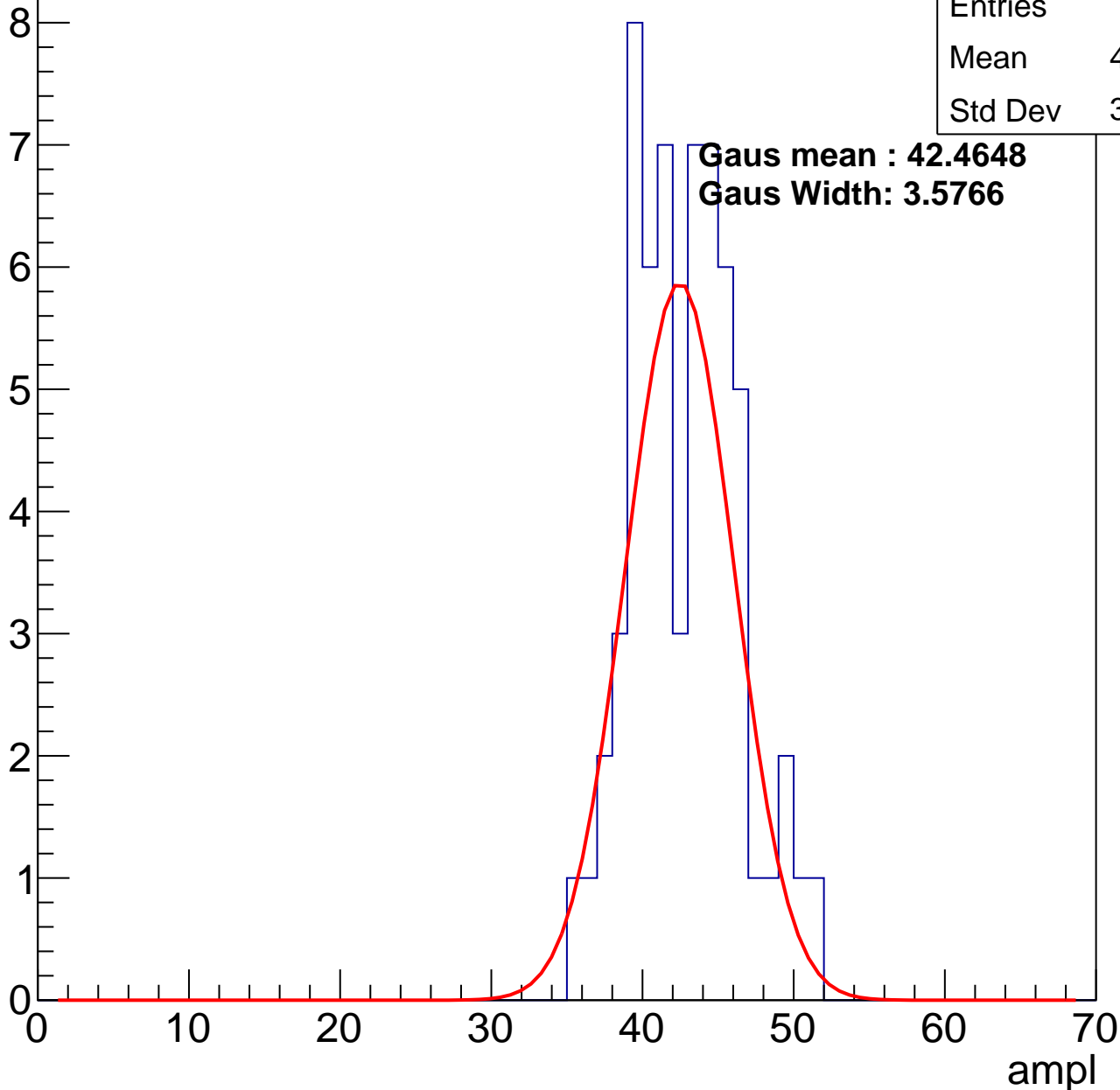
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	62
Mean	42.37
Std Dev	3.479

**Gaus mean : 42.4648**

**Gaus Width: 3.5766**

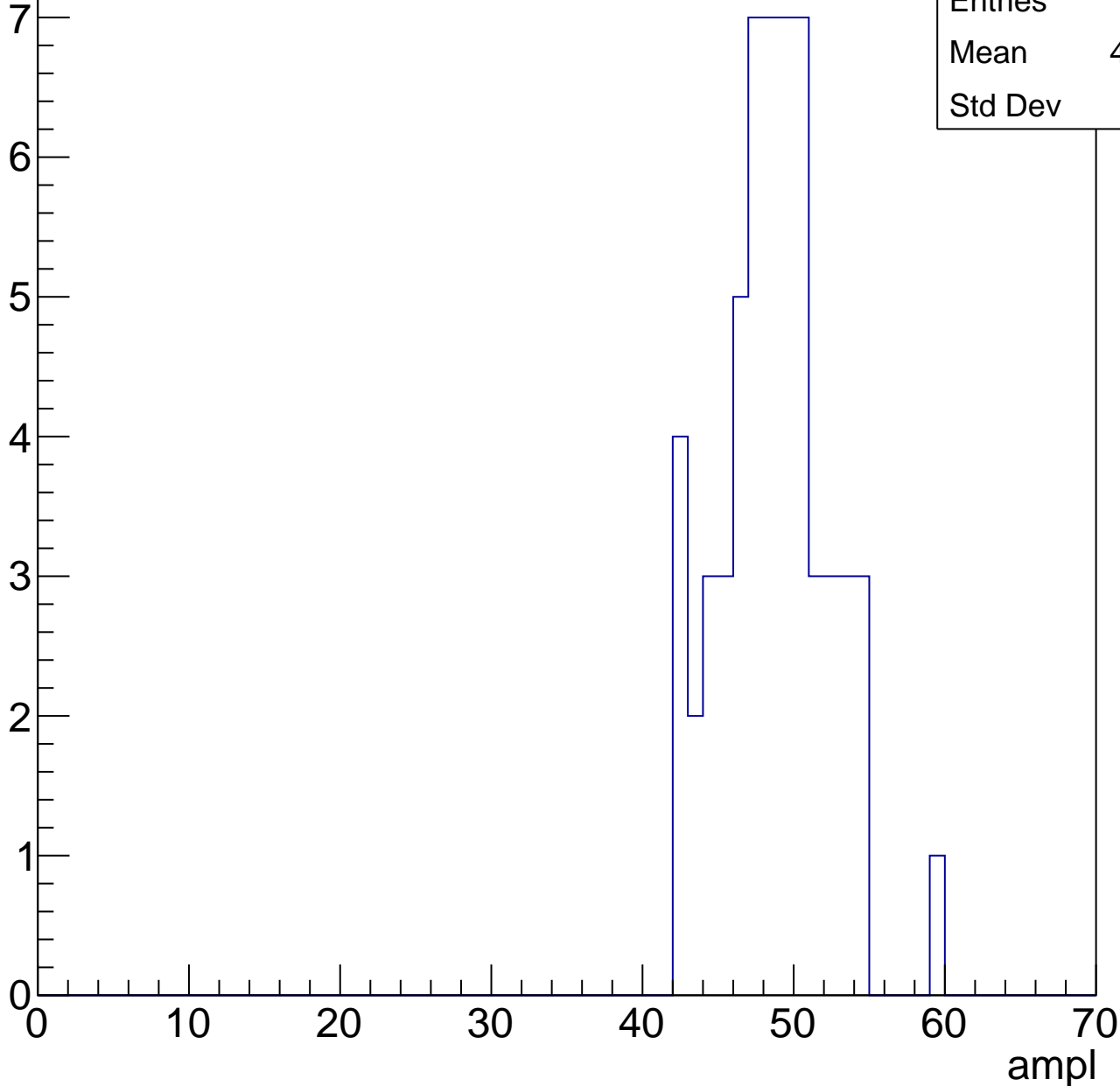


# B1L101S, U3-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	48.24
Std Dev	3.49

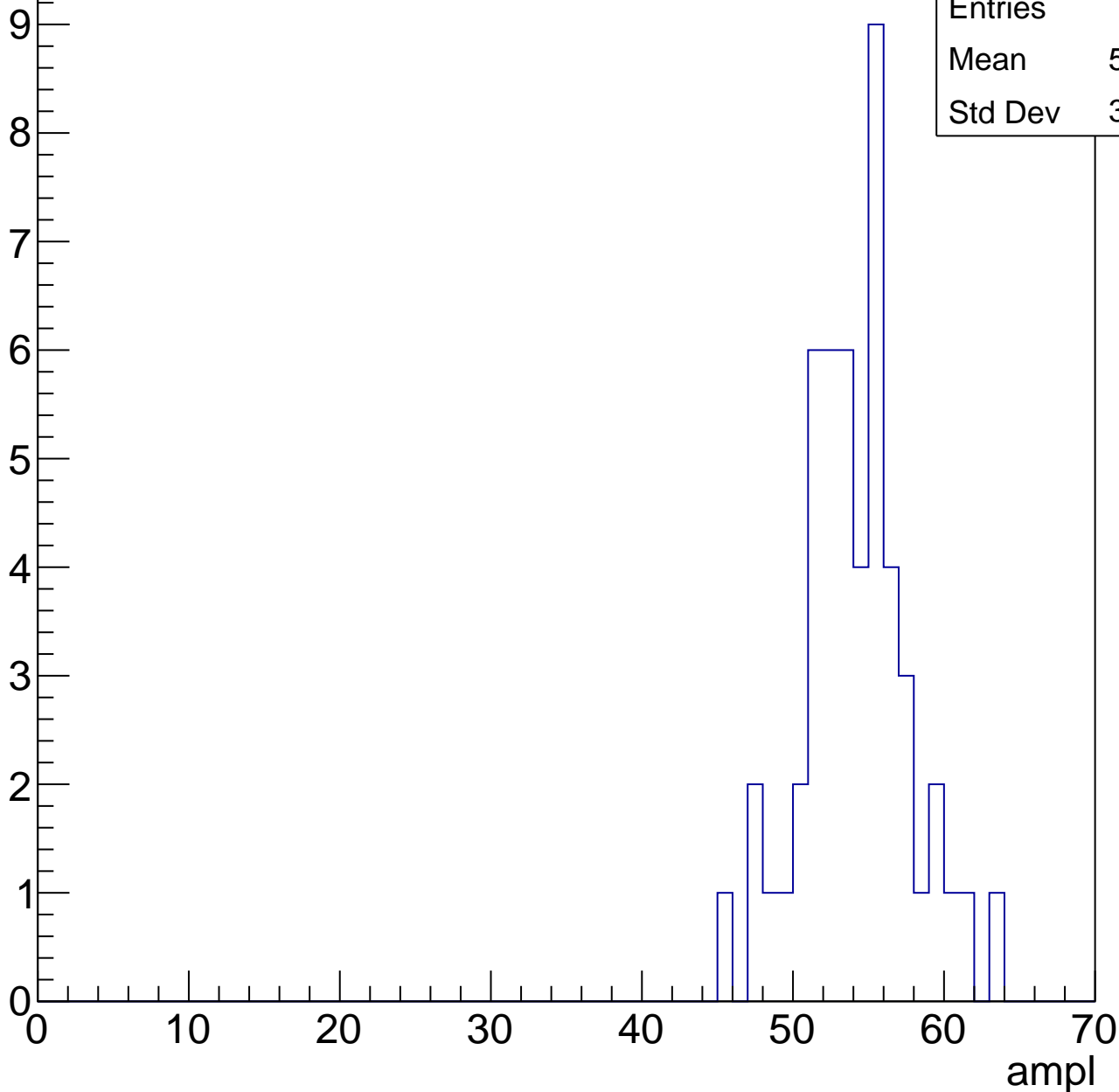


# B1L101S, U3-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	51
Mean	53.69
Std Dev	3.529

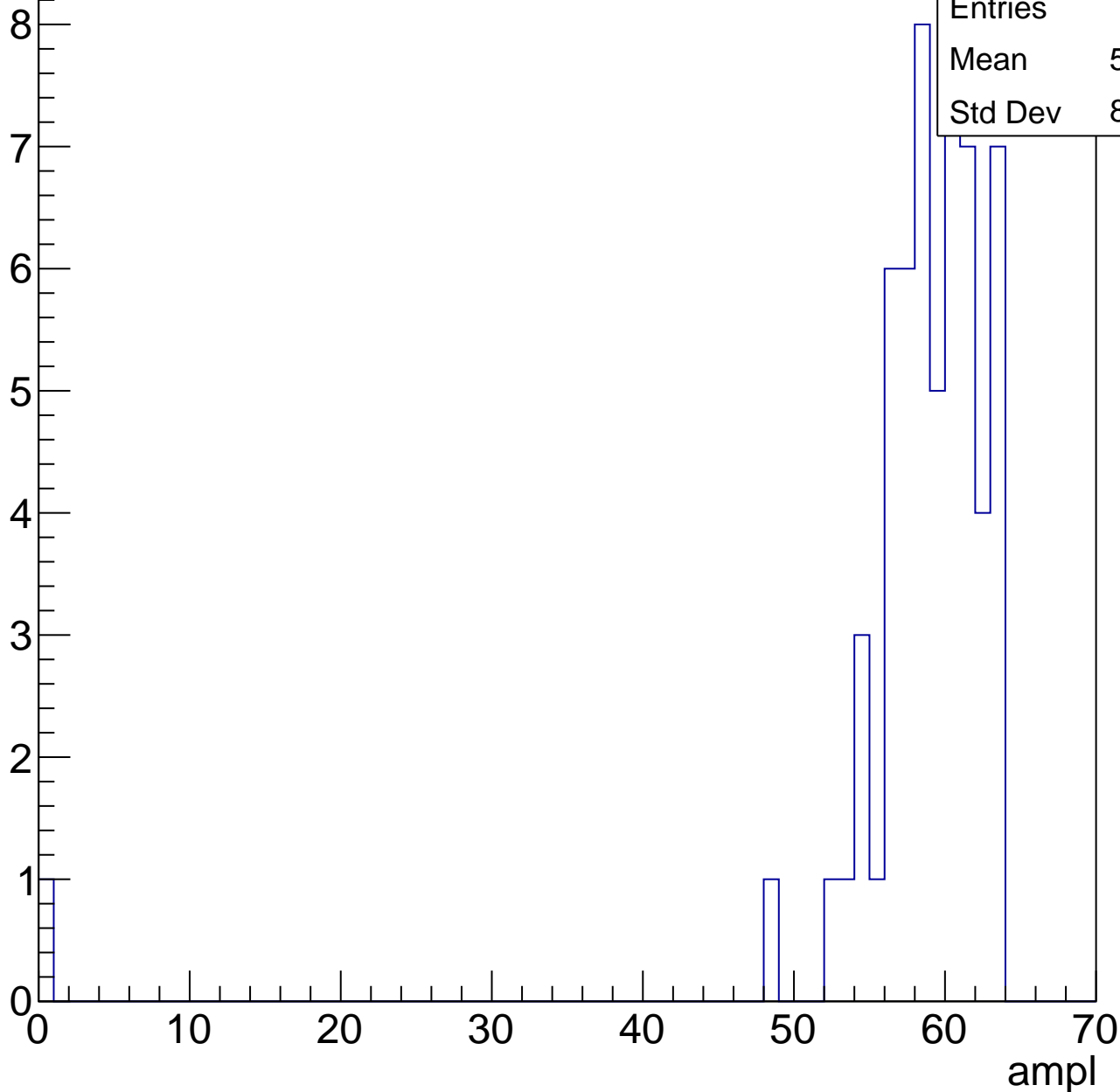


# B1L101S, U3-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	57.68
Std Dev	8.177

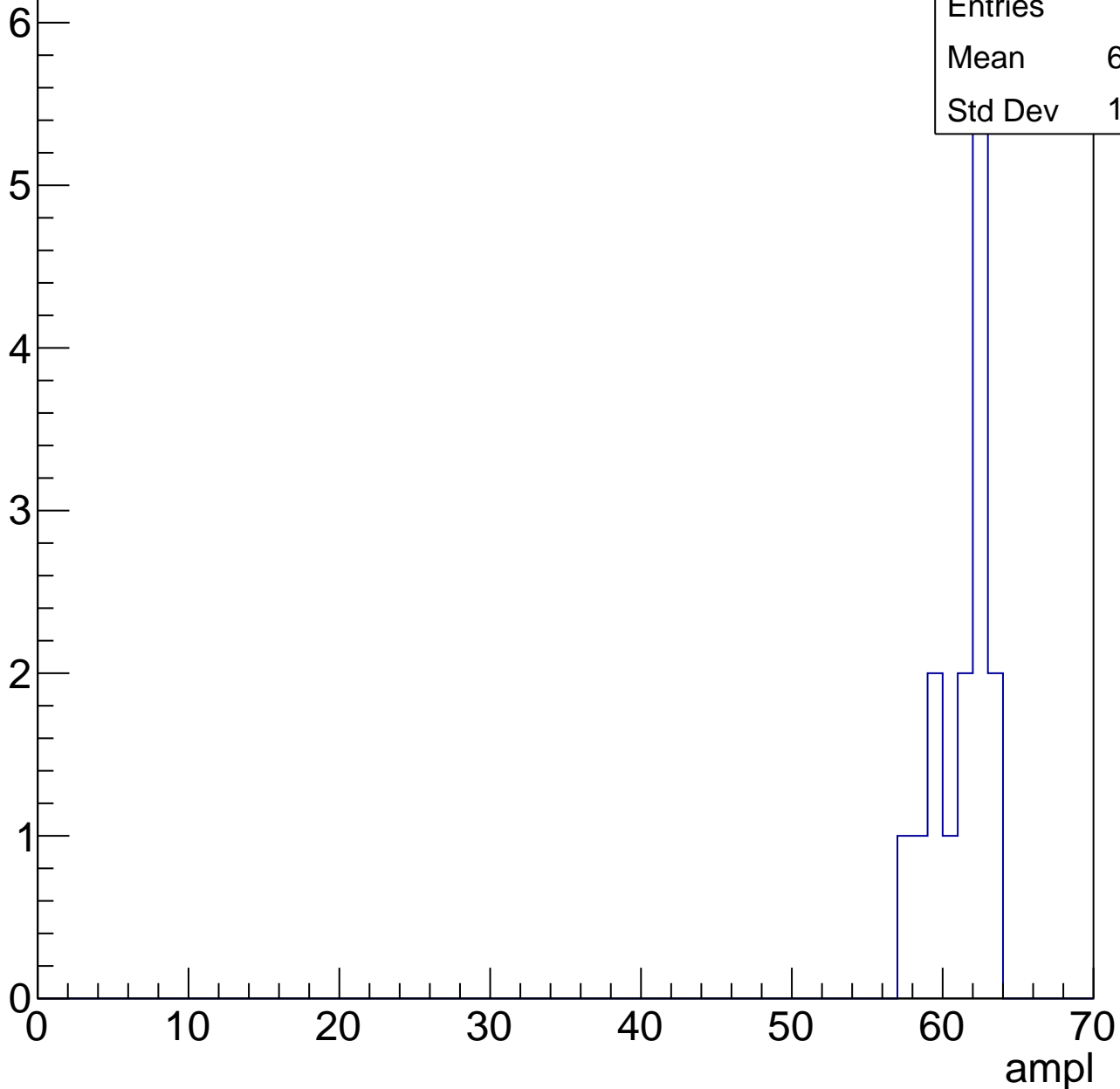


# B1L101S, U3-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	15
Mean	60.87
Std Dev	1.784





# B1L101S, U3-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U3-ch122, adc0

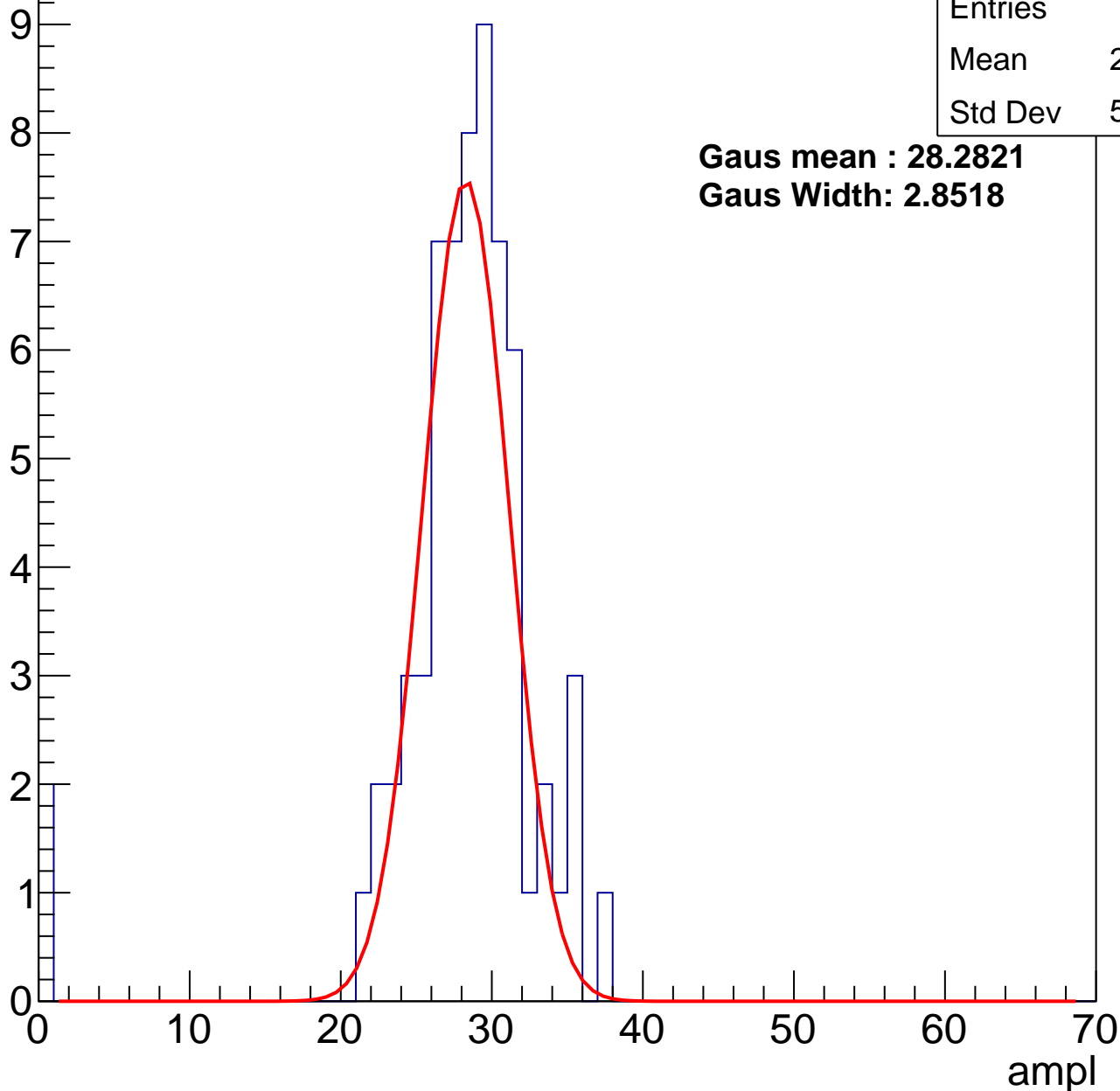
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	27.45
Std Dev	5.884

**Gaus mean : 28.2821**

**Gaus Width: 2.8518**



# B1L101S, U3-ch122, adc1

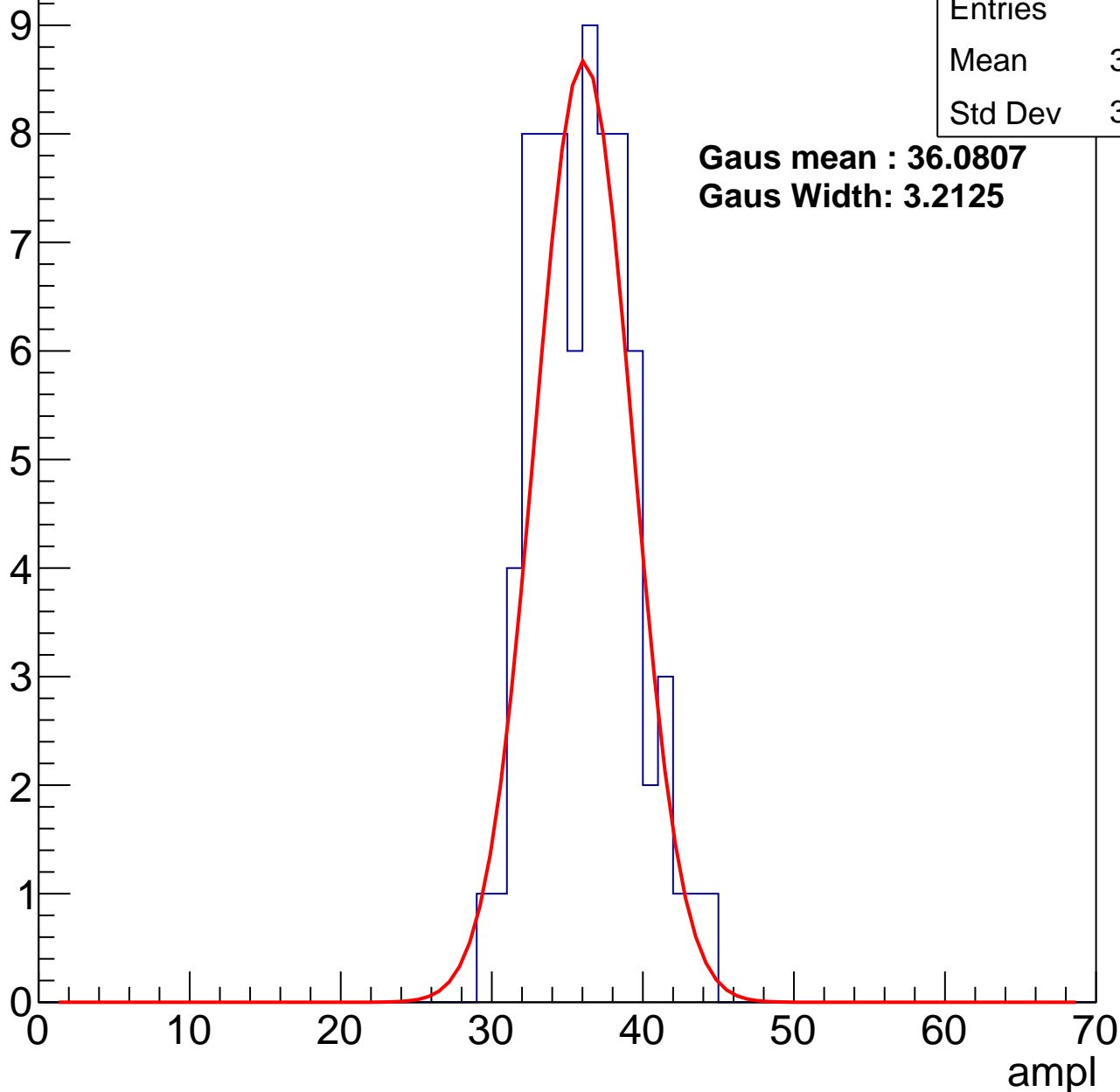
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	75
Mean	35.67
Std Dev	3.193

**Gaus mean : 36.0807**

**Gaus Width: 3.2125**



# B1L101S, U3-ch122, adc2

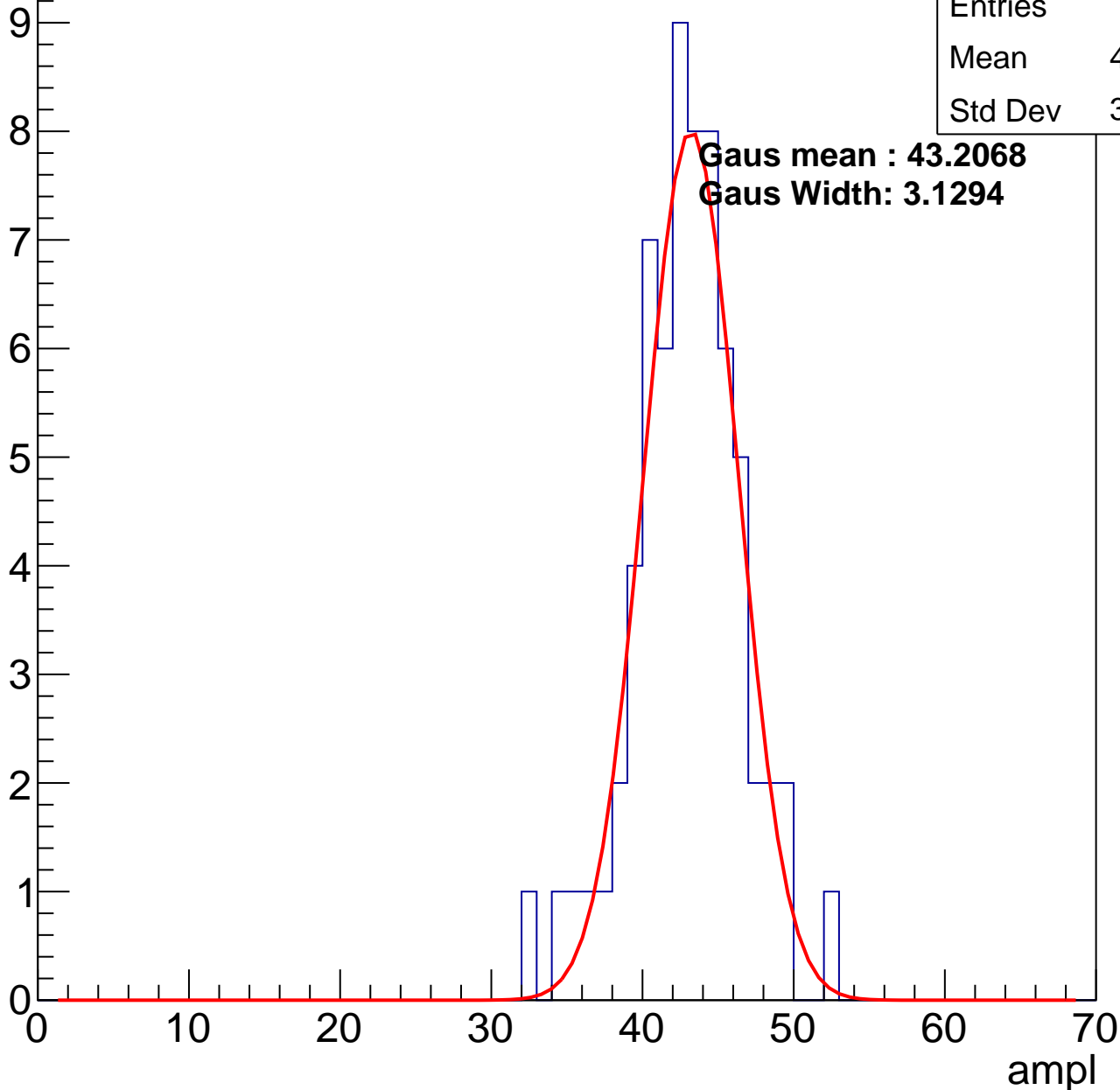
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	42.48
Std Dev	3.572

**Gaus mean : 43.2068**

**Gaus Width: 3.1294**

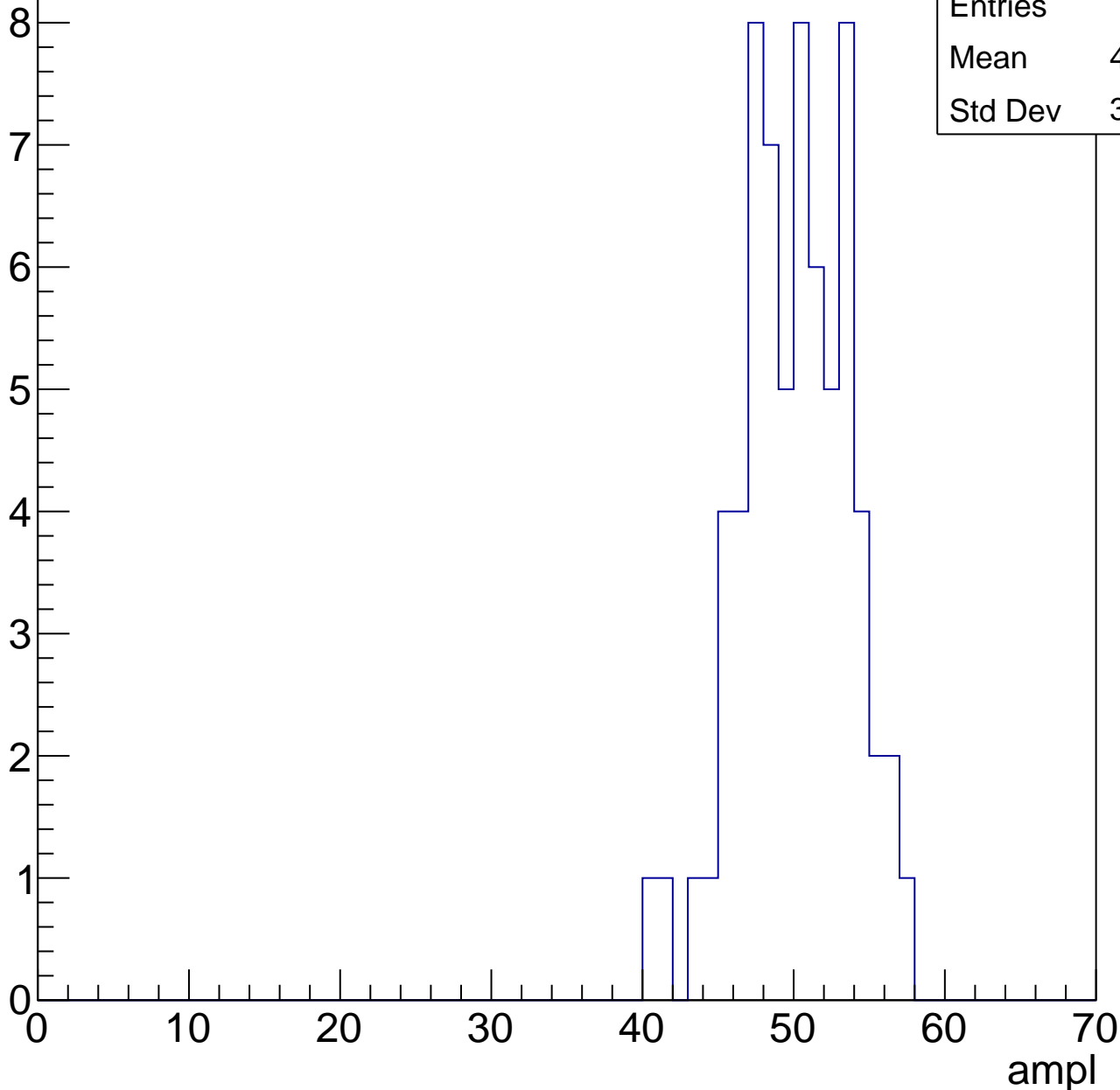


# B1L101S, U3-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	68
Mean	49.62
Std Dev	3.552

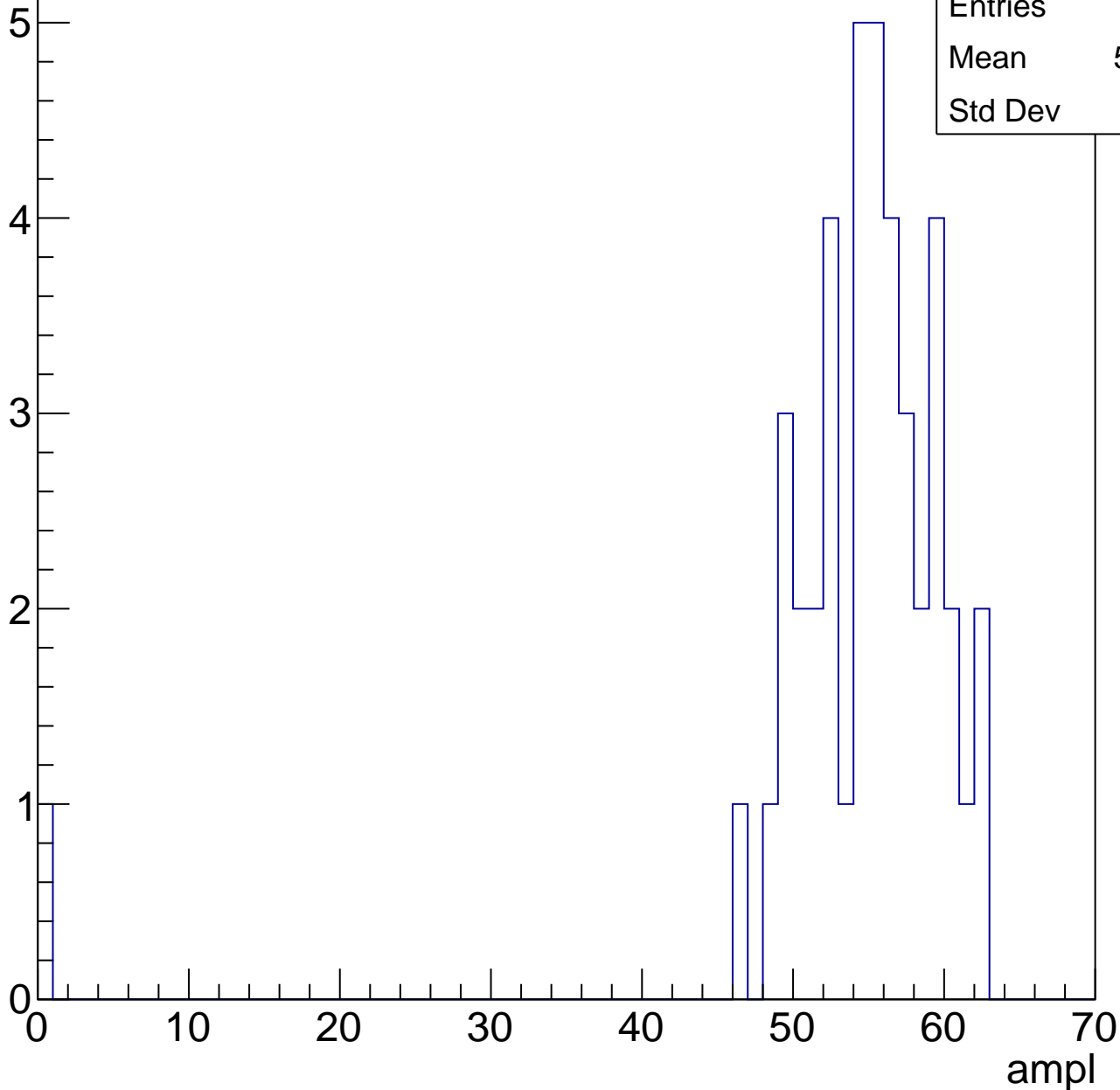


# B1L101S, U3-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	43
Mean	53.51
Std Dev	9.12

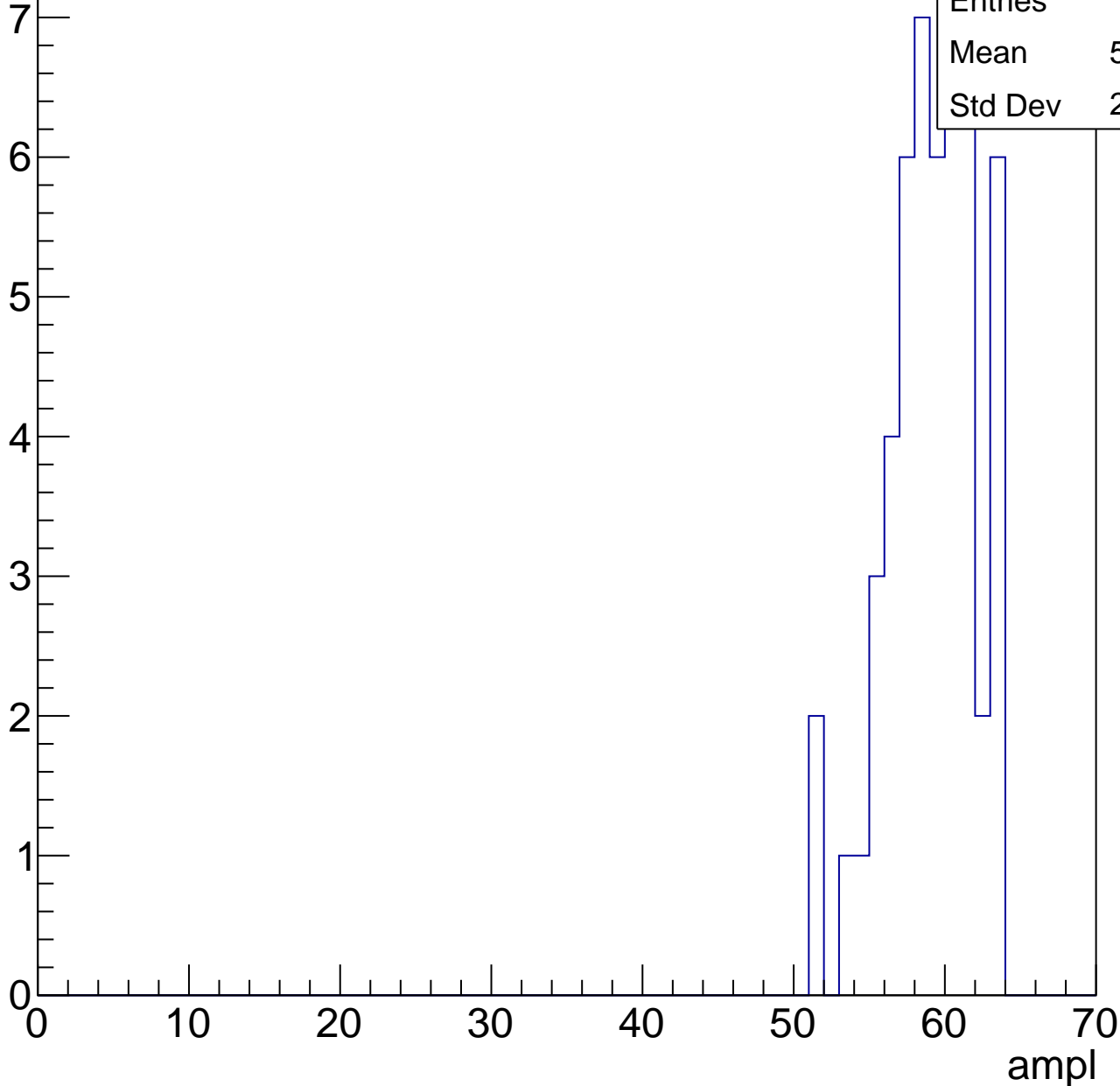


# B1L101S, U3-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	52
Mean	58.63
Std Dev	2.929

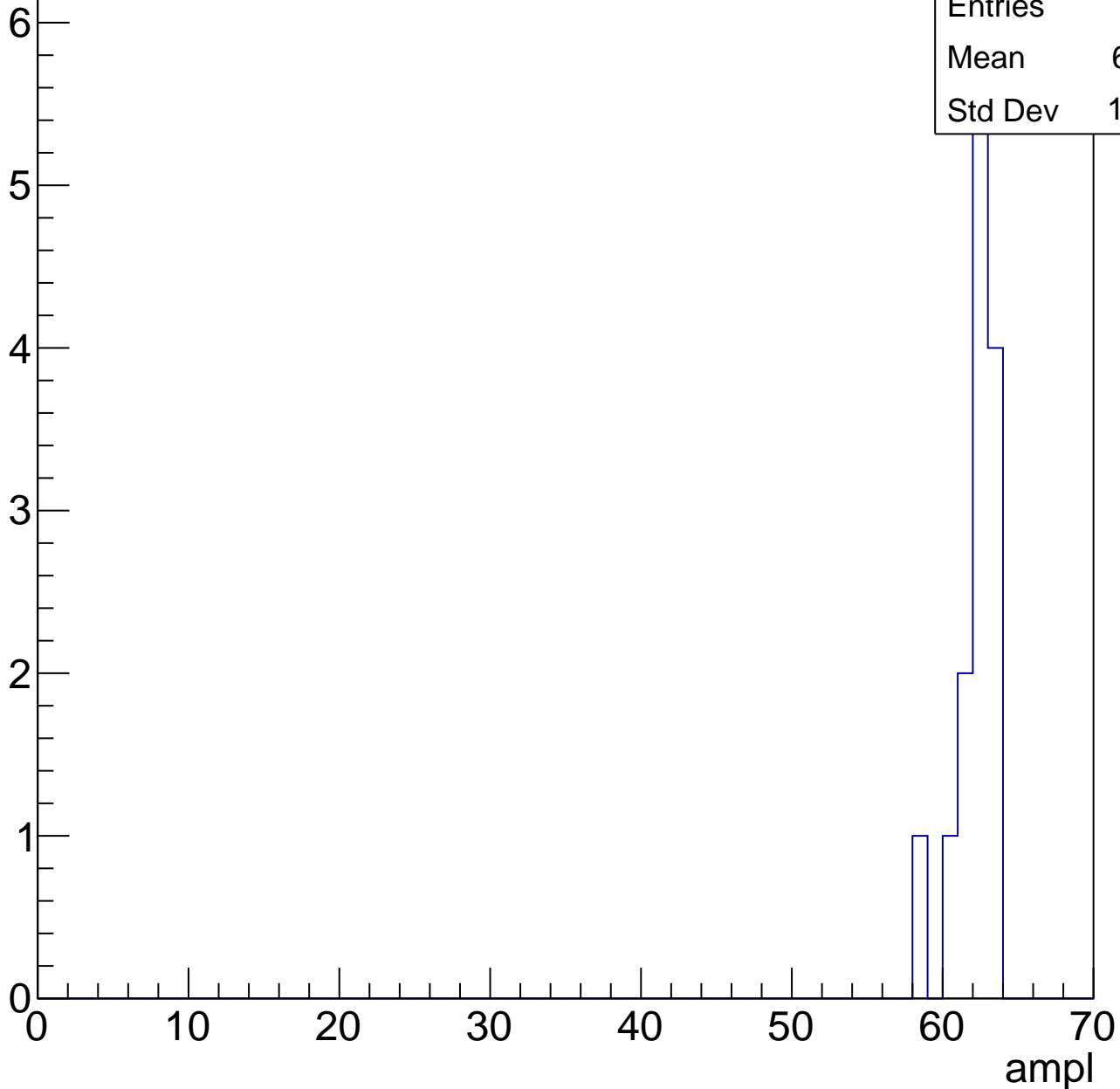


# B1L101S, U3-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	14
Mean	61.71
Std Dev	1.332





# B1L101S, U3-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L101S, U3-ch123, adc0

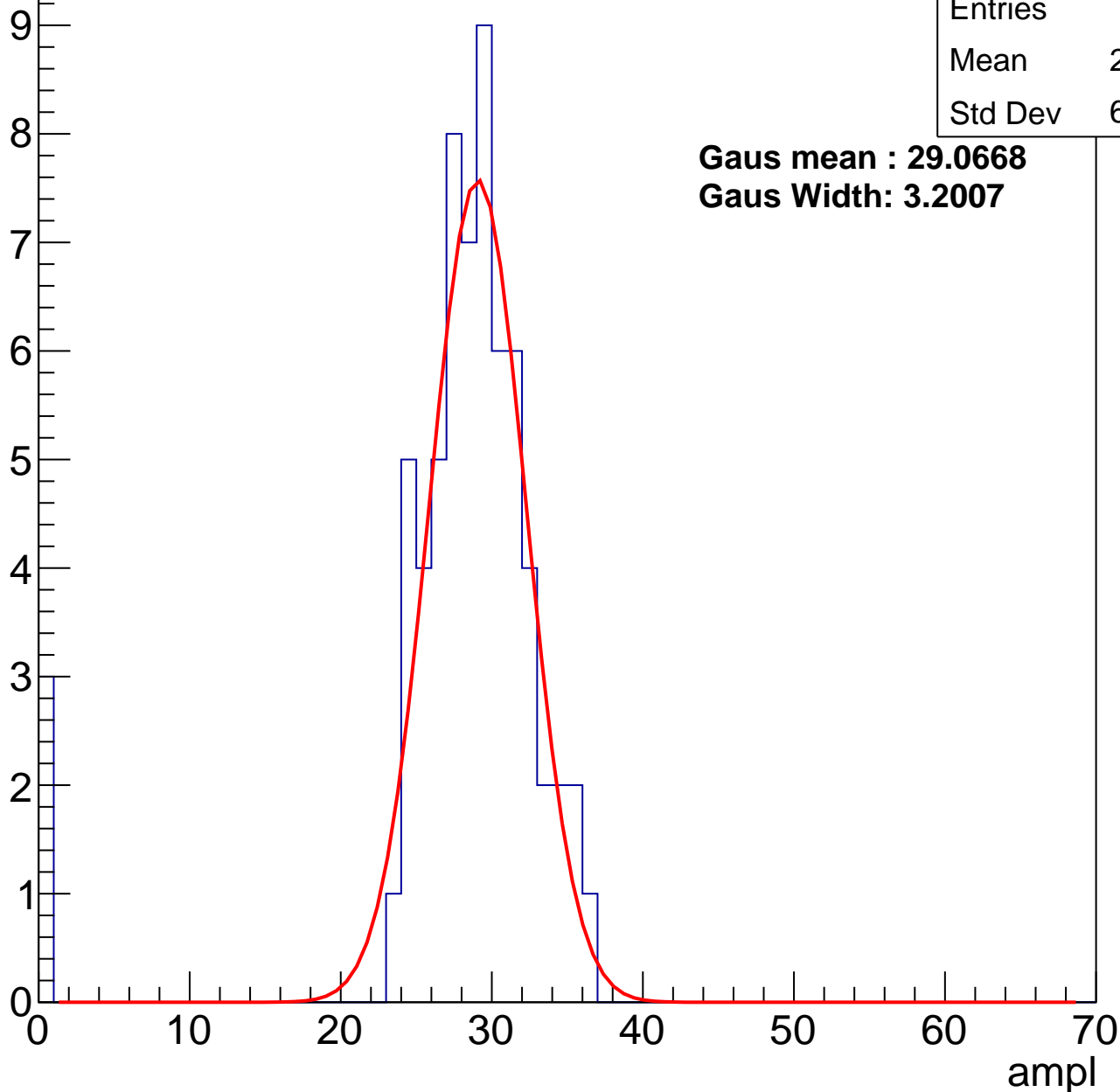
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	65
Mean	27.38
Std Dev	6.716

**Gaus mean : 29.0668**

**Gaus Width: 3.2007**



# B1L101S, U3-ch123, adc1

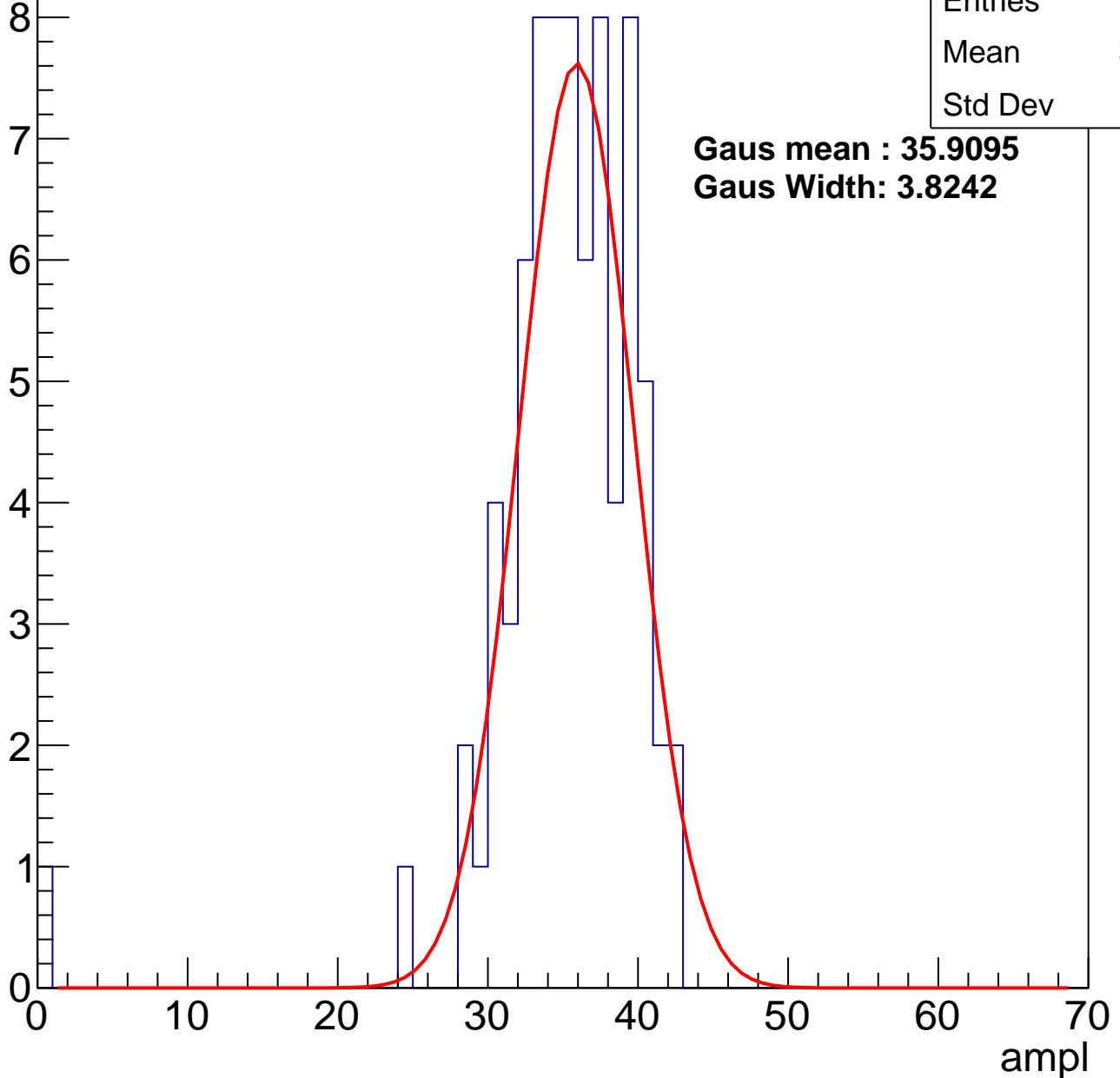
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	34.7
Std Dev	5.36

**Gaus mean : 35.9095**

**Gaus Width: 3.8242**



# B1L101S, U3-ch123, adc2

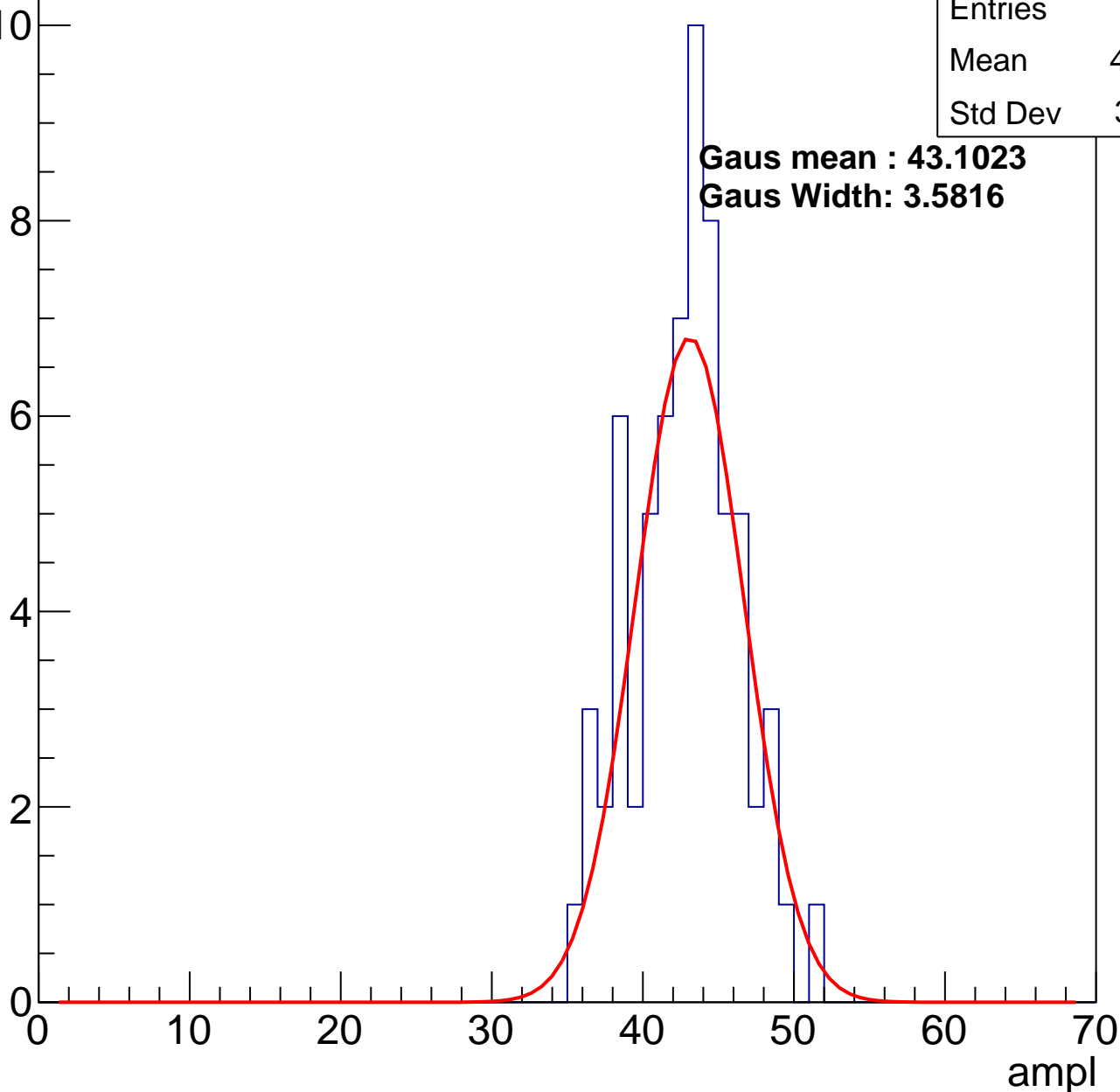
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	67
Mean	42.36
Std Dev	3.441

**Gaus mean : 43.1023**

**Gaus Width: 3.5816**

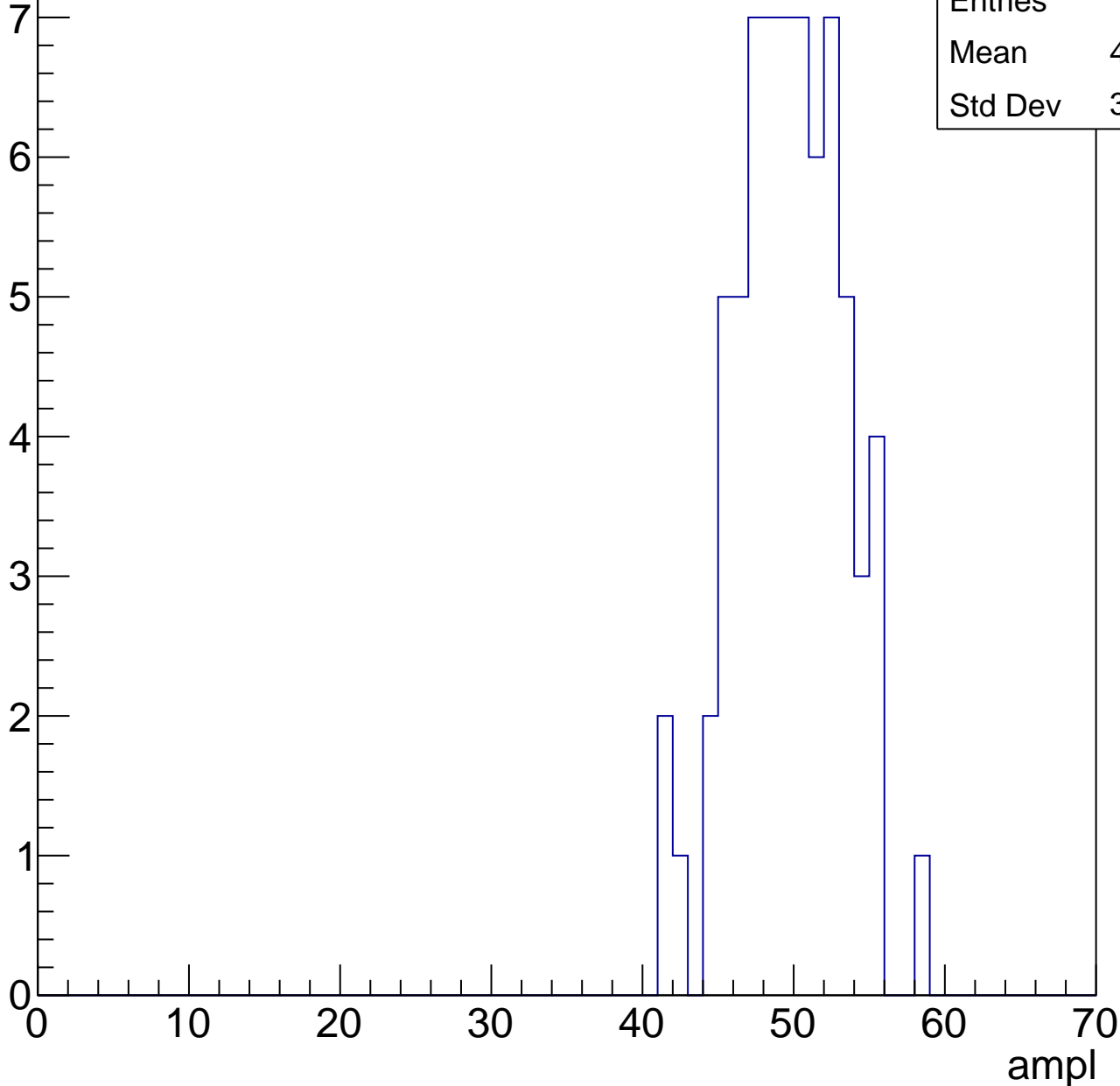


# B1L101S, U3-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

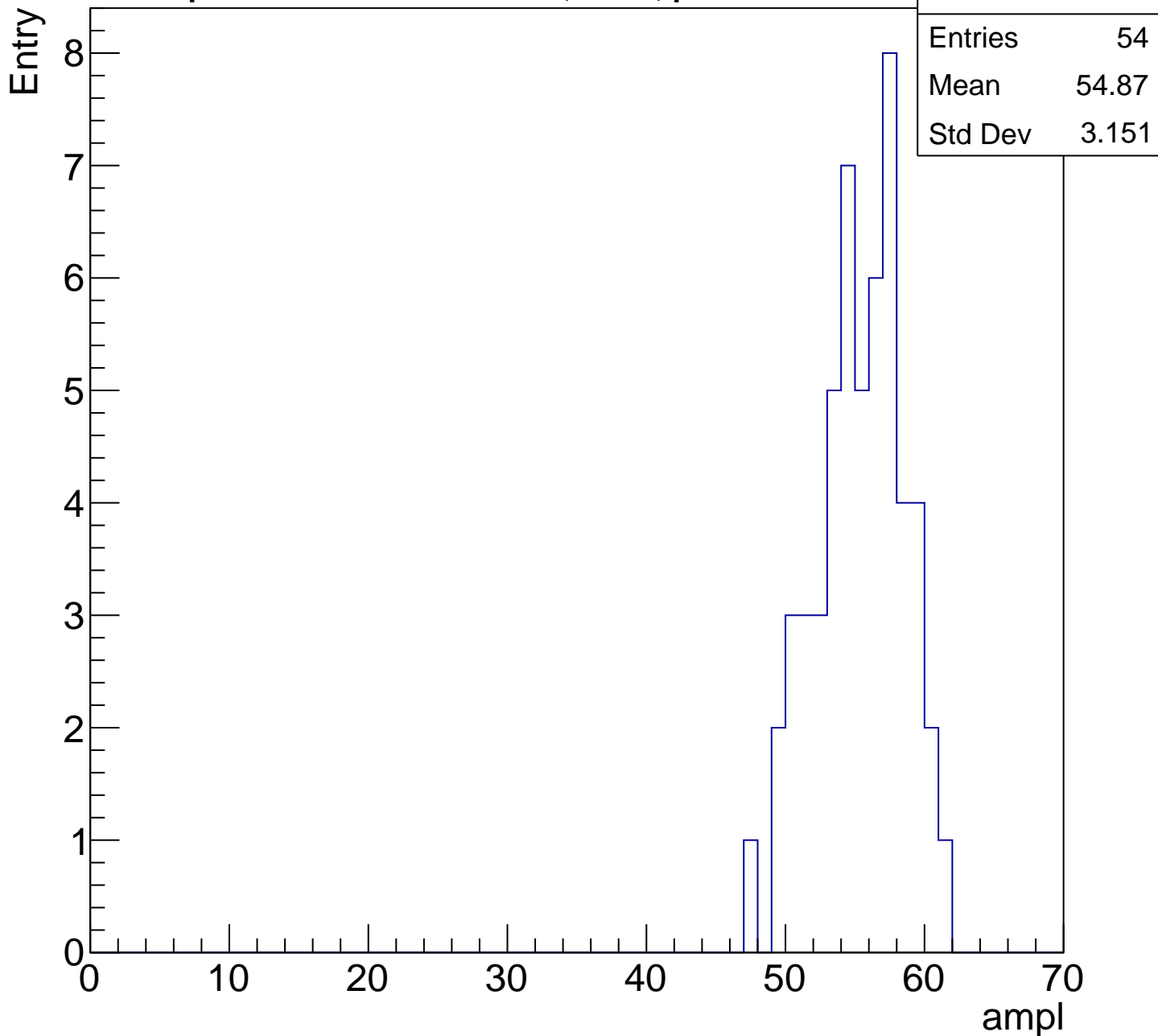
Entry

Entries	69
Mean	49.28
Std Dev	3.522



# B1L101S, U3-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

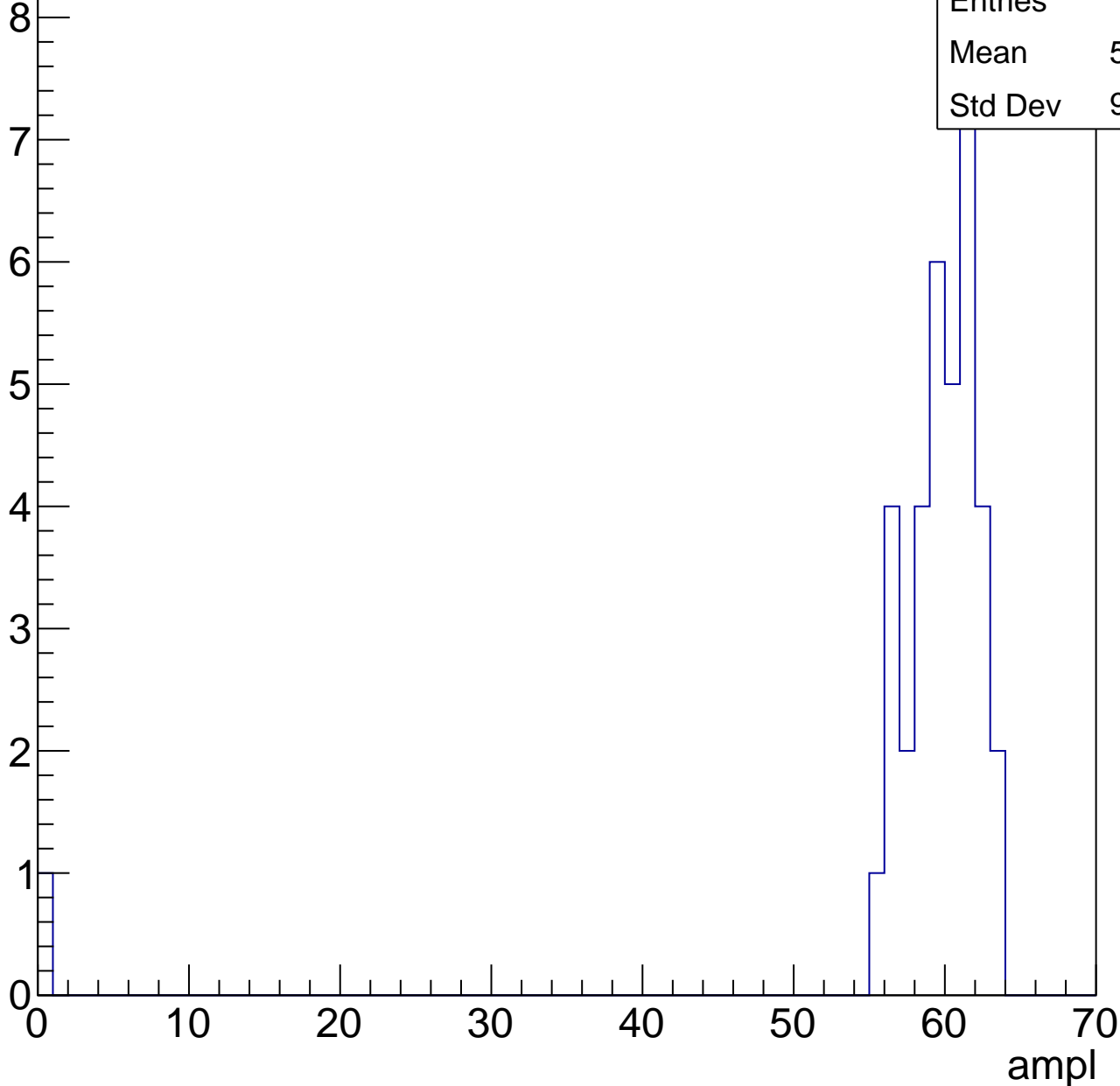


# B1L101S, U3-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	37
Mean	57.86
Std Dev	9.867

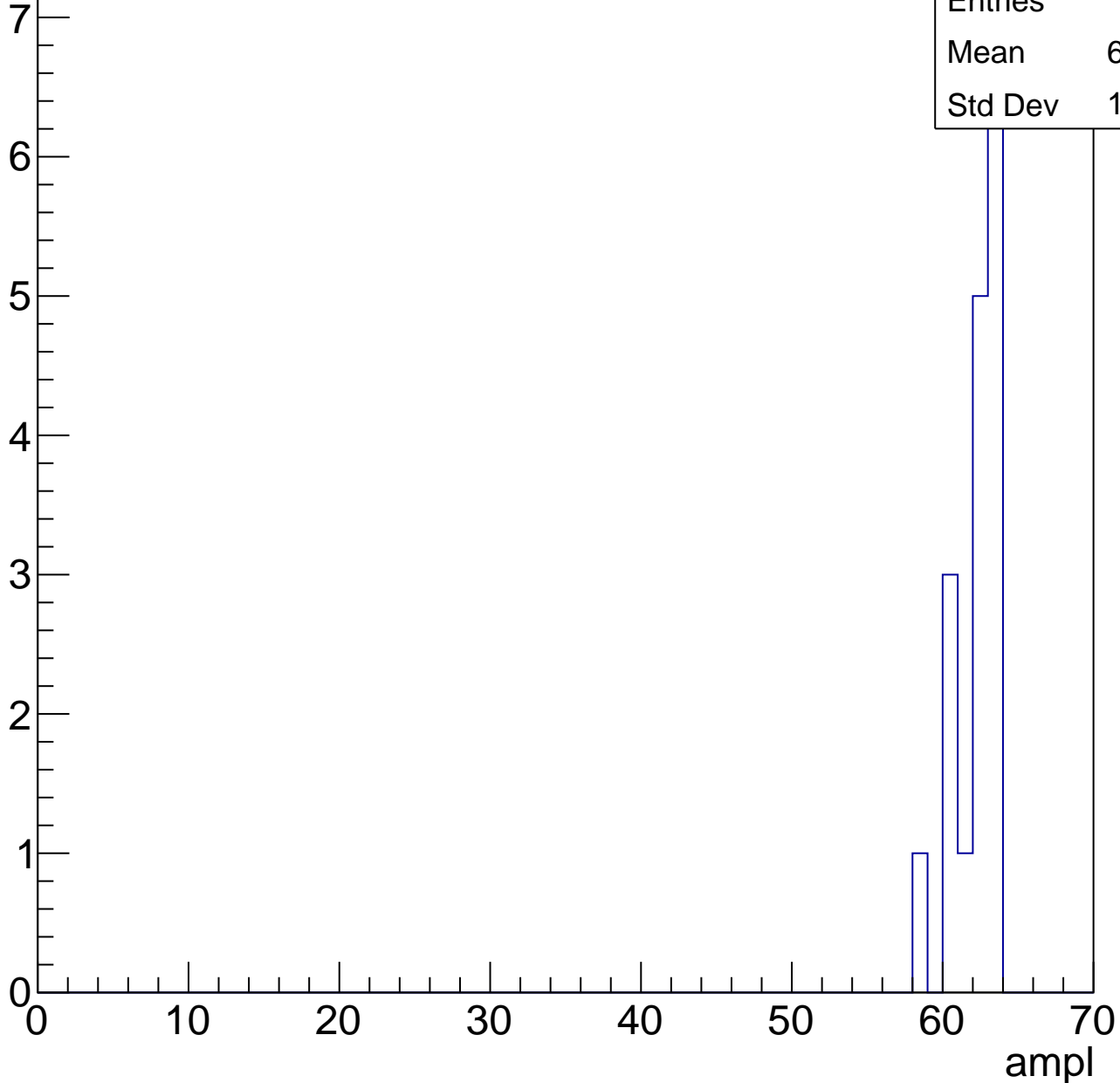


# B1L101S, U3-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	17
Mean	61.76
Std Dev	1.436

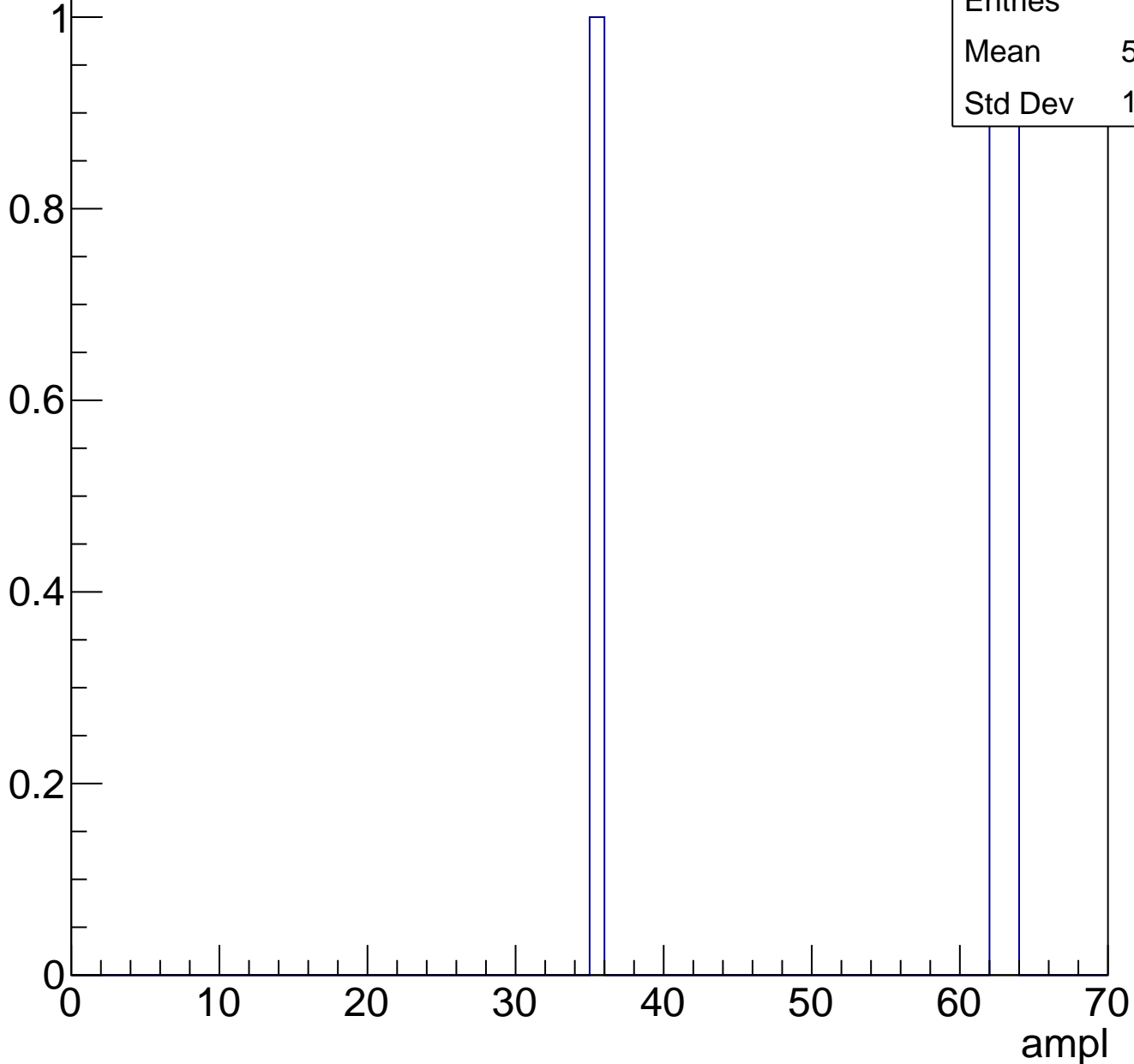




# B1L101S, U3-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch124, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	88
Mean	27.23
Std Dev	4.764

**Gaus mean : 27.9516**

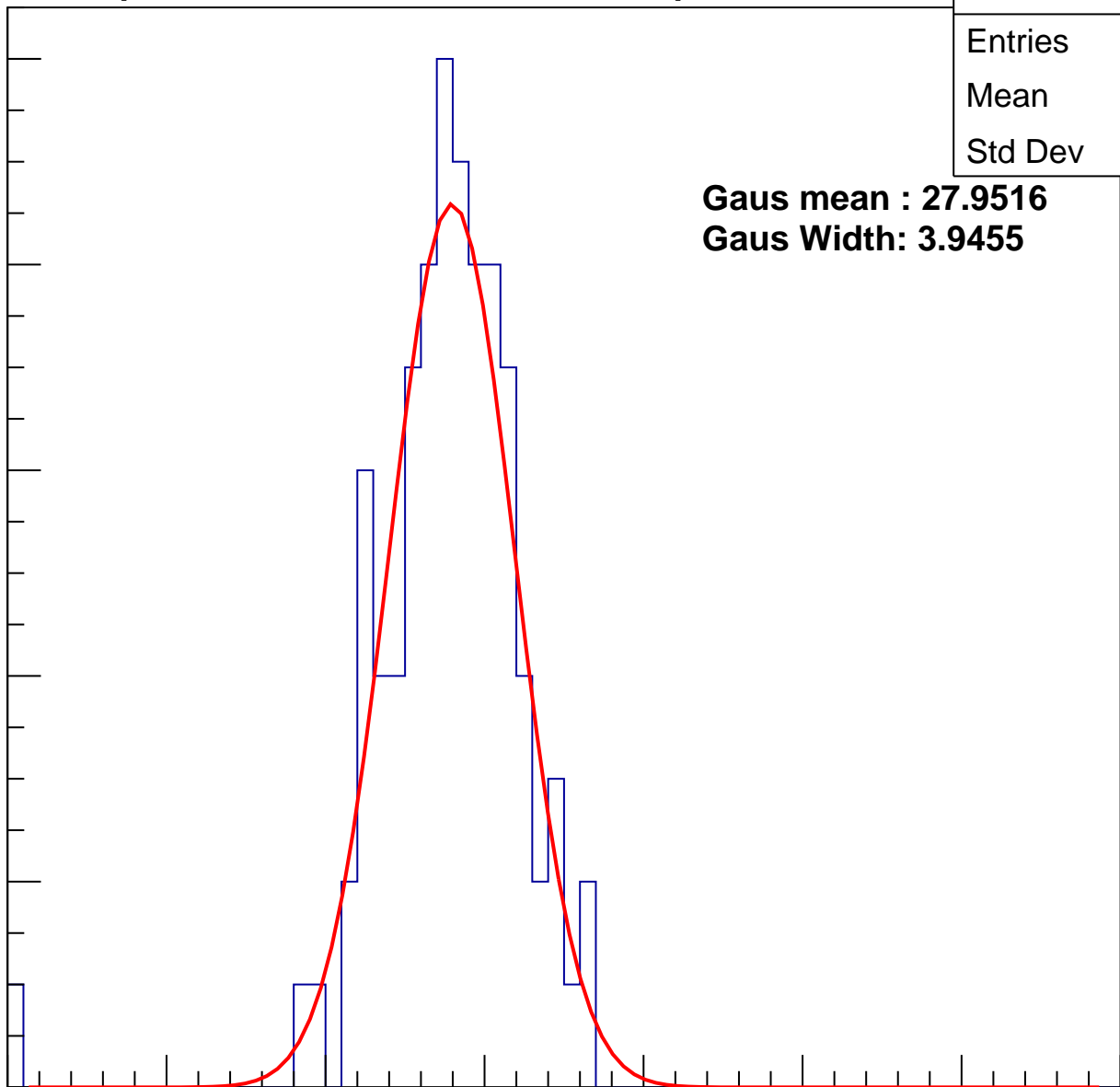
**Gaus Width: 3.9455**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U3-ch124, adc1

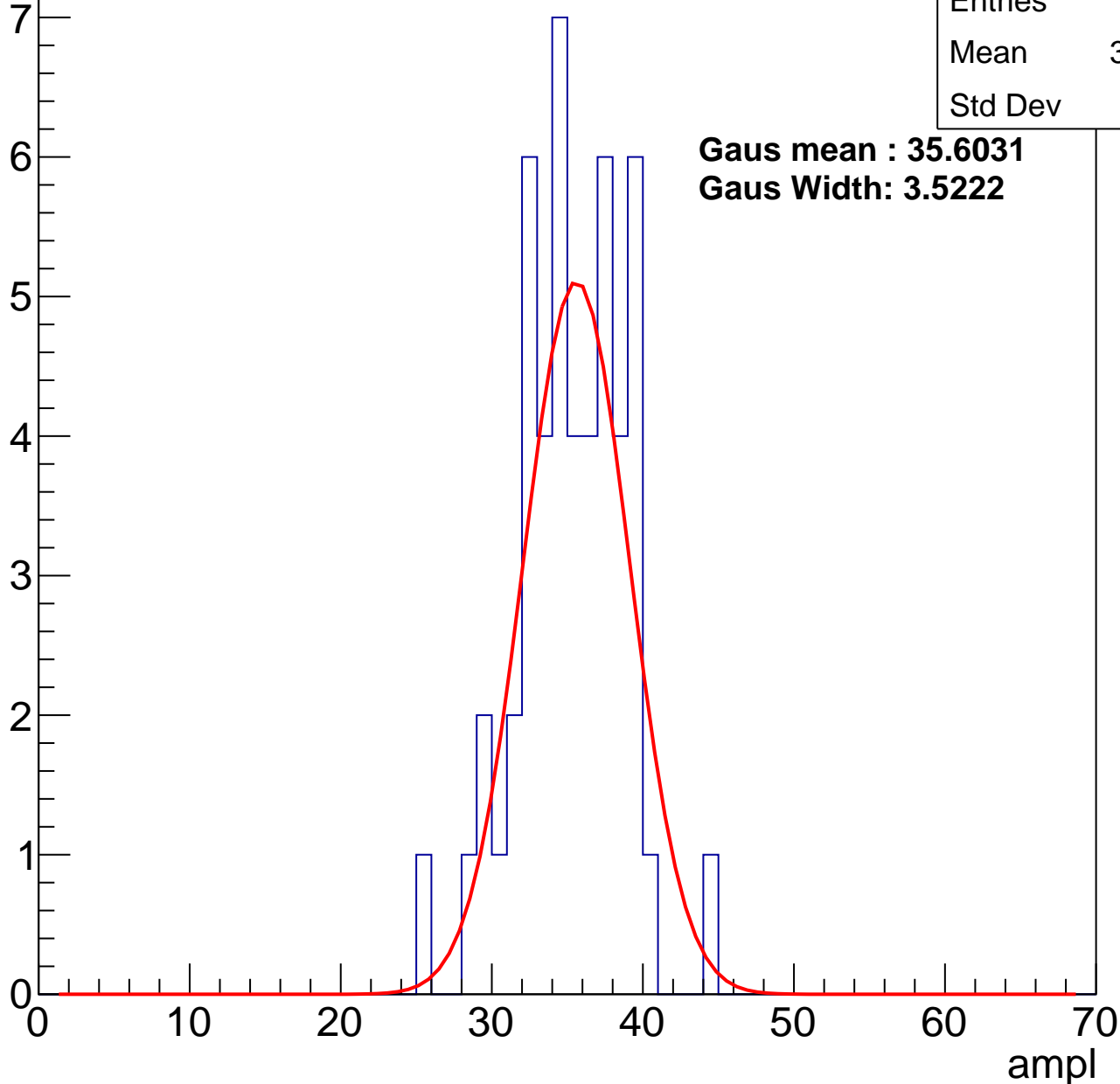
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	50
Mean	34.82
Std Dev	3.52

**Gaus mean : 35.6031**

**Gaus Width: 3.5222**



# B1L101S, U3-ch124, adc2

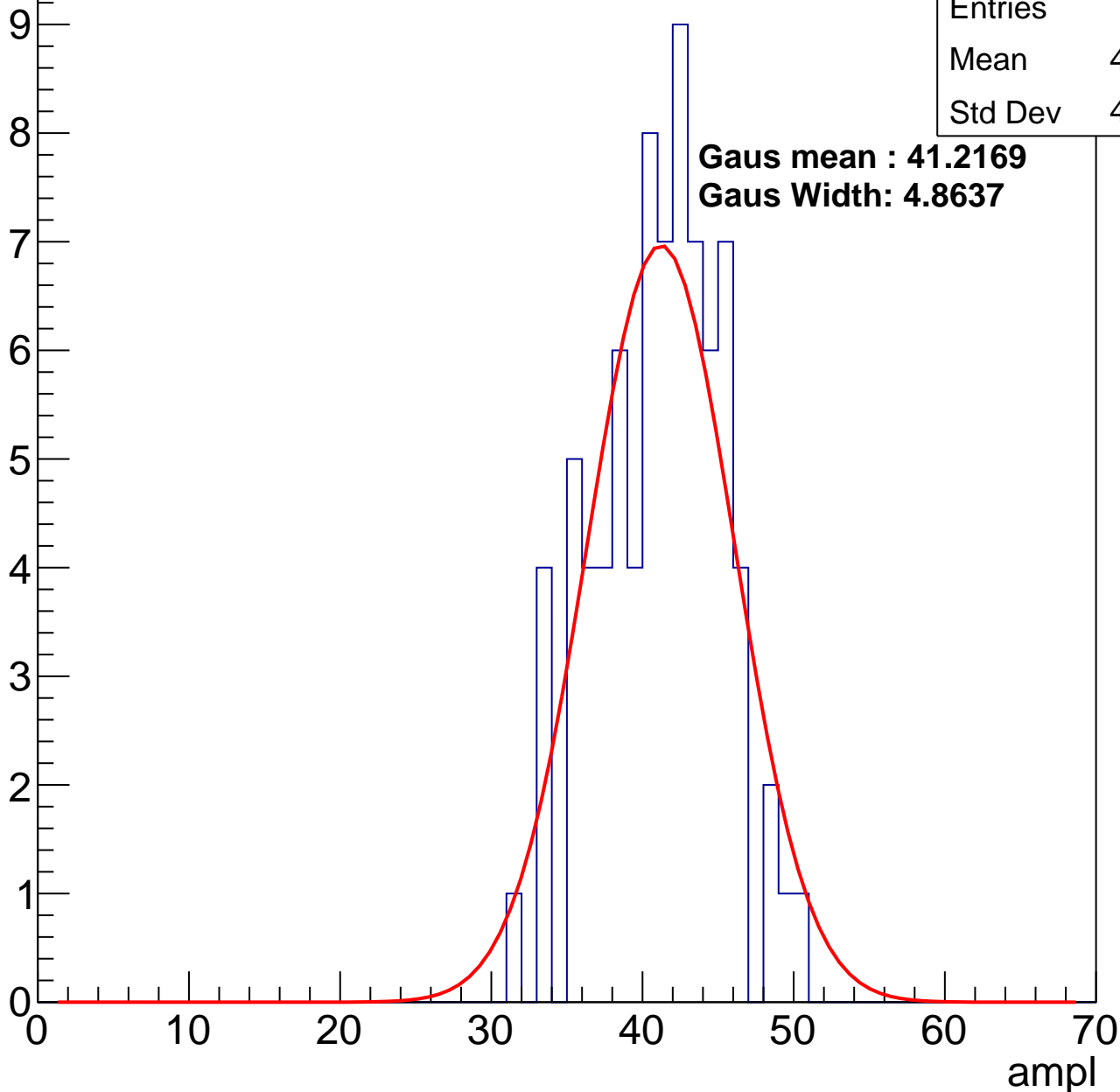
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	80
Mean	40.73
Std Dev	4.059

**Gaus mean : 41.2169**

**Gaus Width: 4.8637**

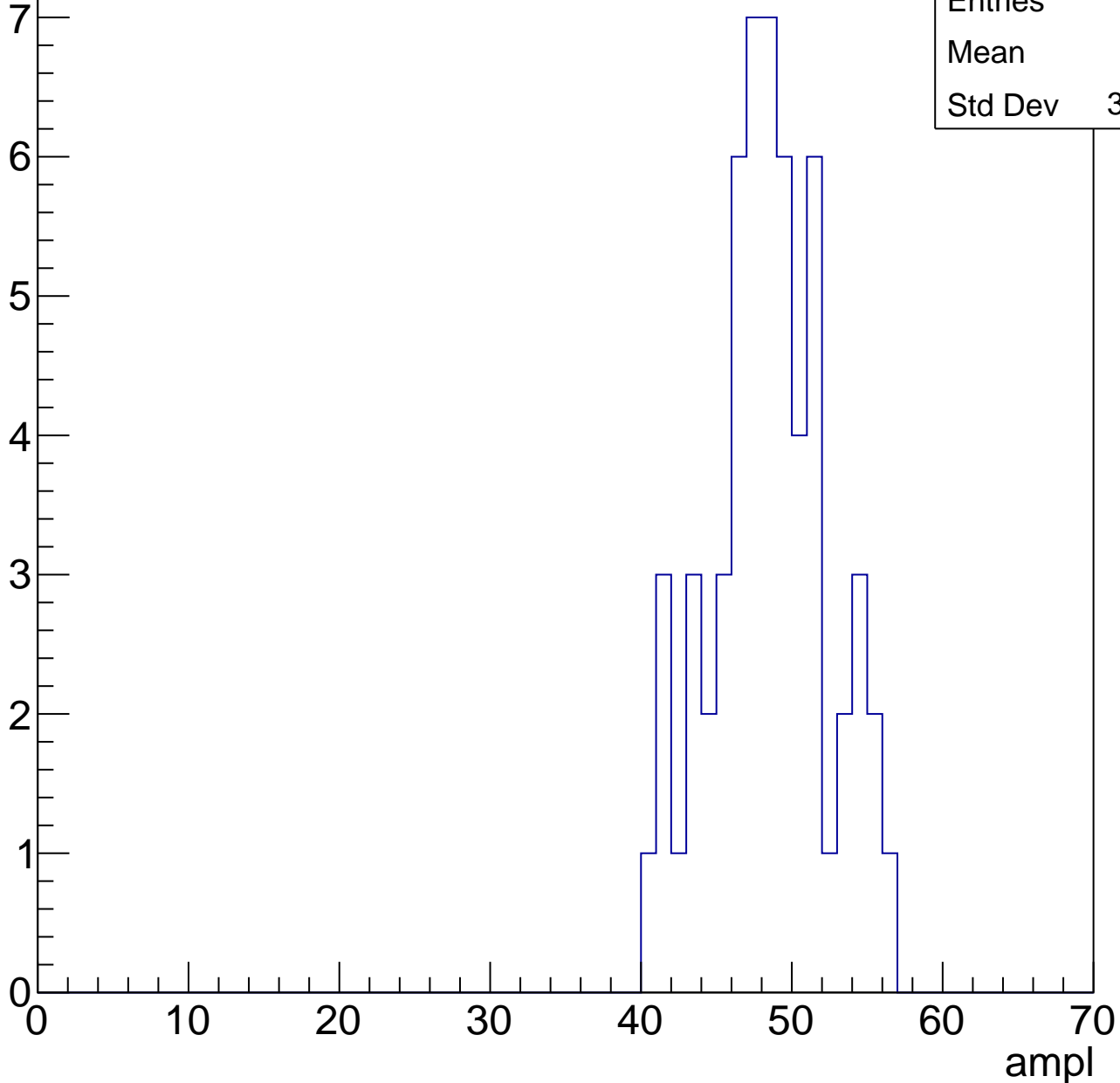


# B1L101S, U3-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	58
Mean	48
Std Dev	3.769

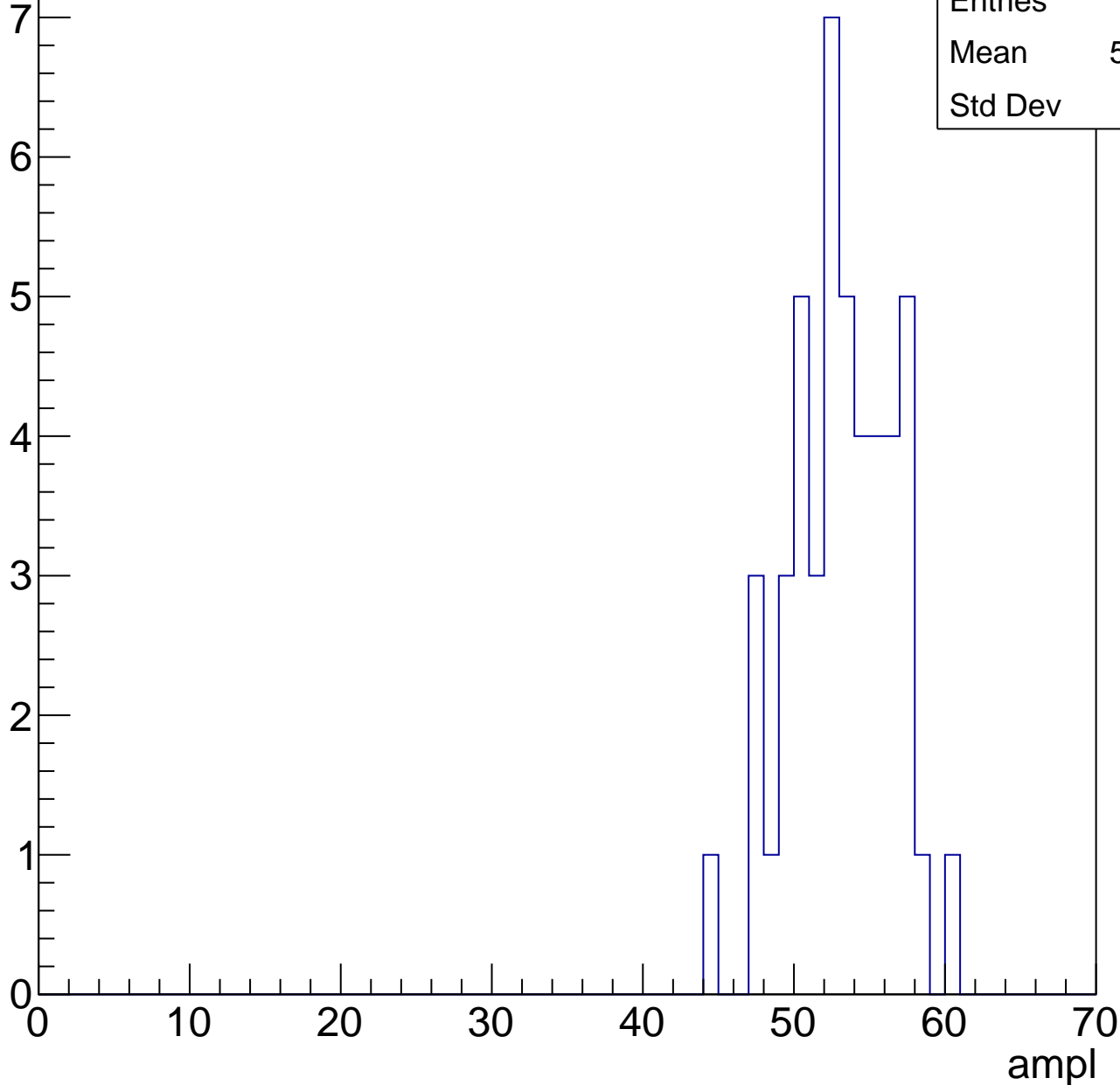


# B1L101S, U3-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	47
Mean	52.66
Std Dev	3.36



# B1L101S, U3-ch124, adc5

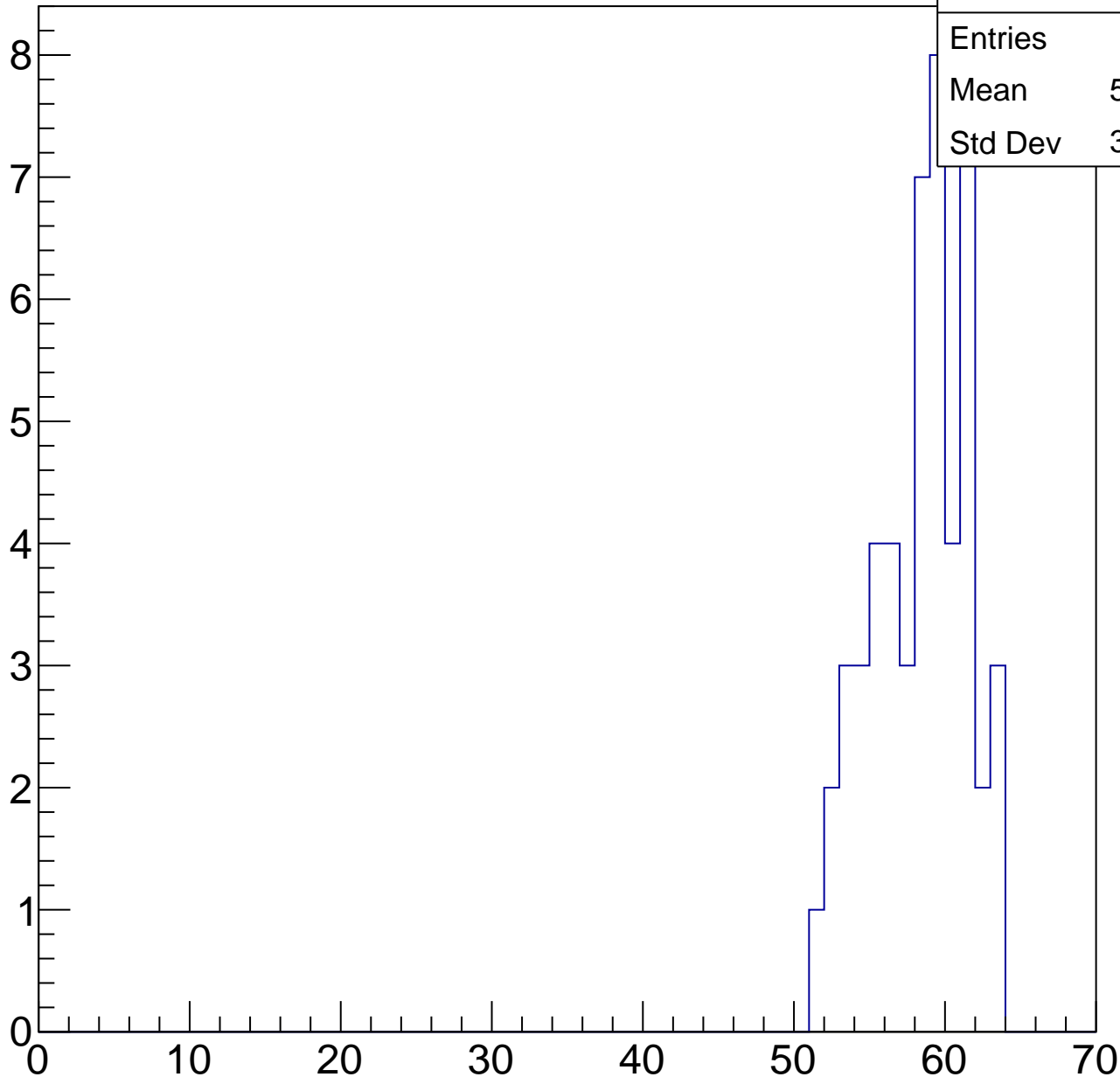
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	52
Mean	57.88
Std Dev	3.105

ampl



# B1L101S, U3-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

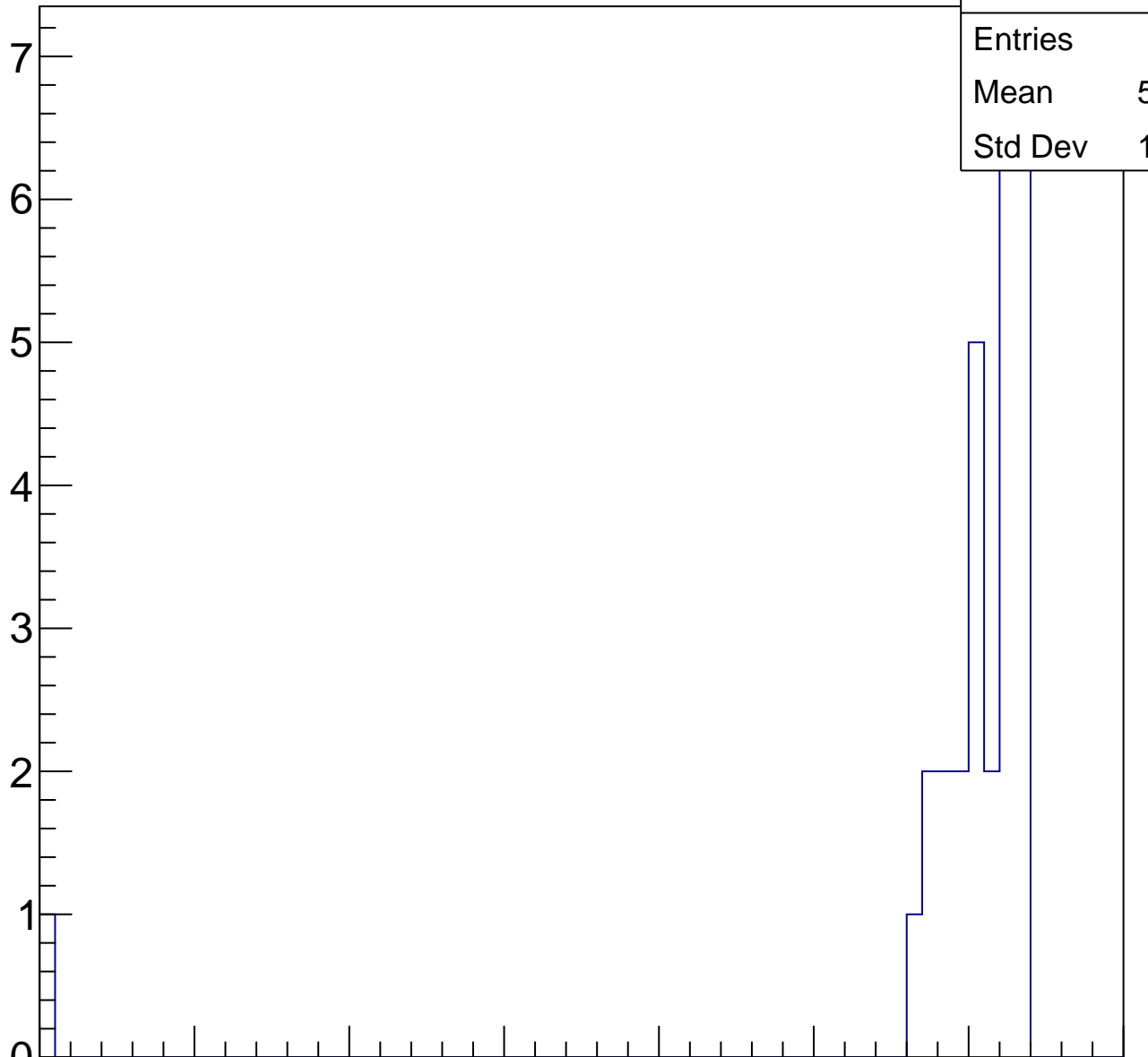
Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	29
Mean	58.66
Std Dev	11.27

ampl

0 10 20 30 40 50 60 70





# B1L101S, U3-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch125, adc0

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	80
Mean	27.23
Std Dev	6.423

**Gaus mean : 28.7518**

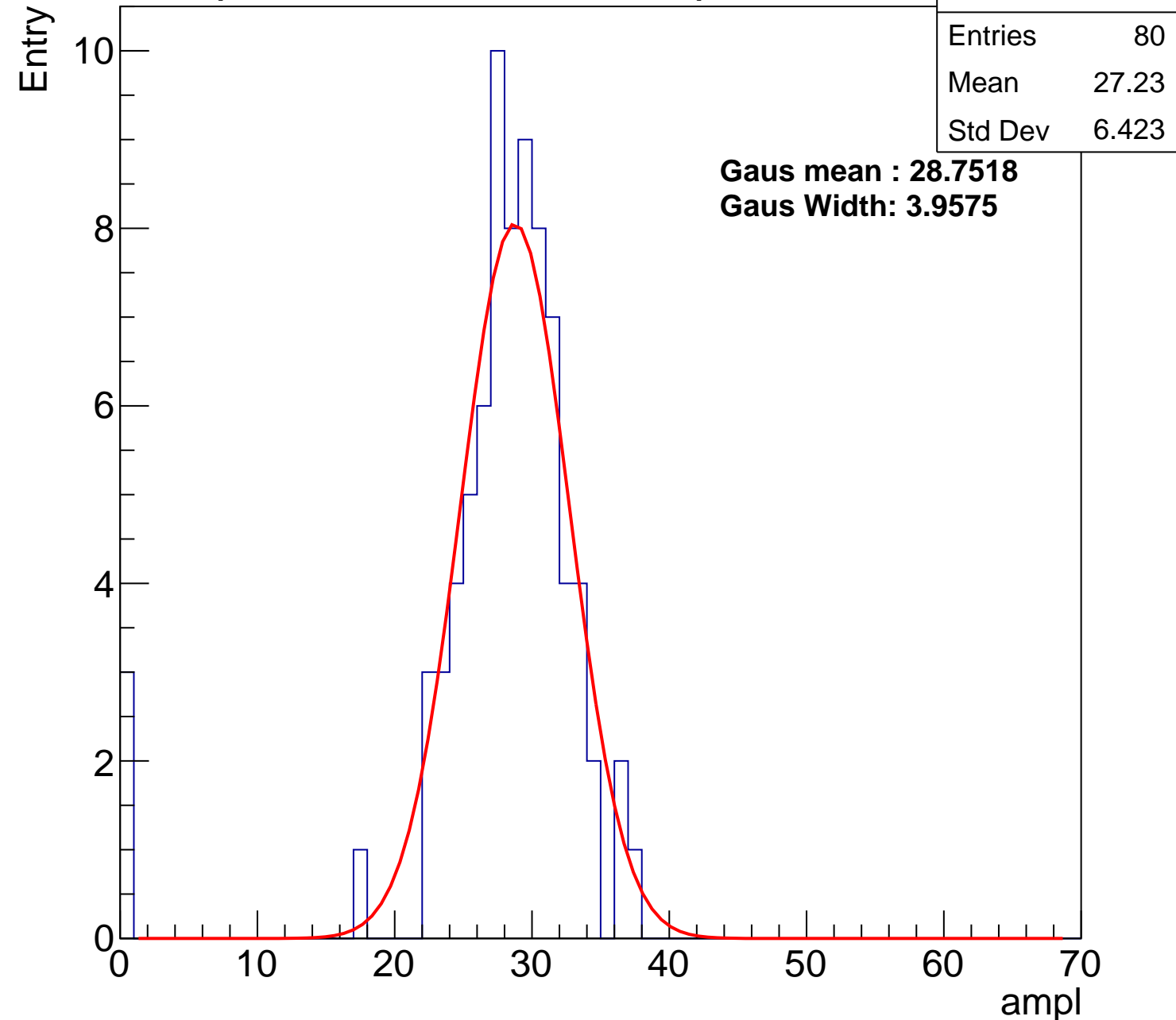
**Gaus Width: 3.9575**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L101S, U3-ch125, adc1

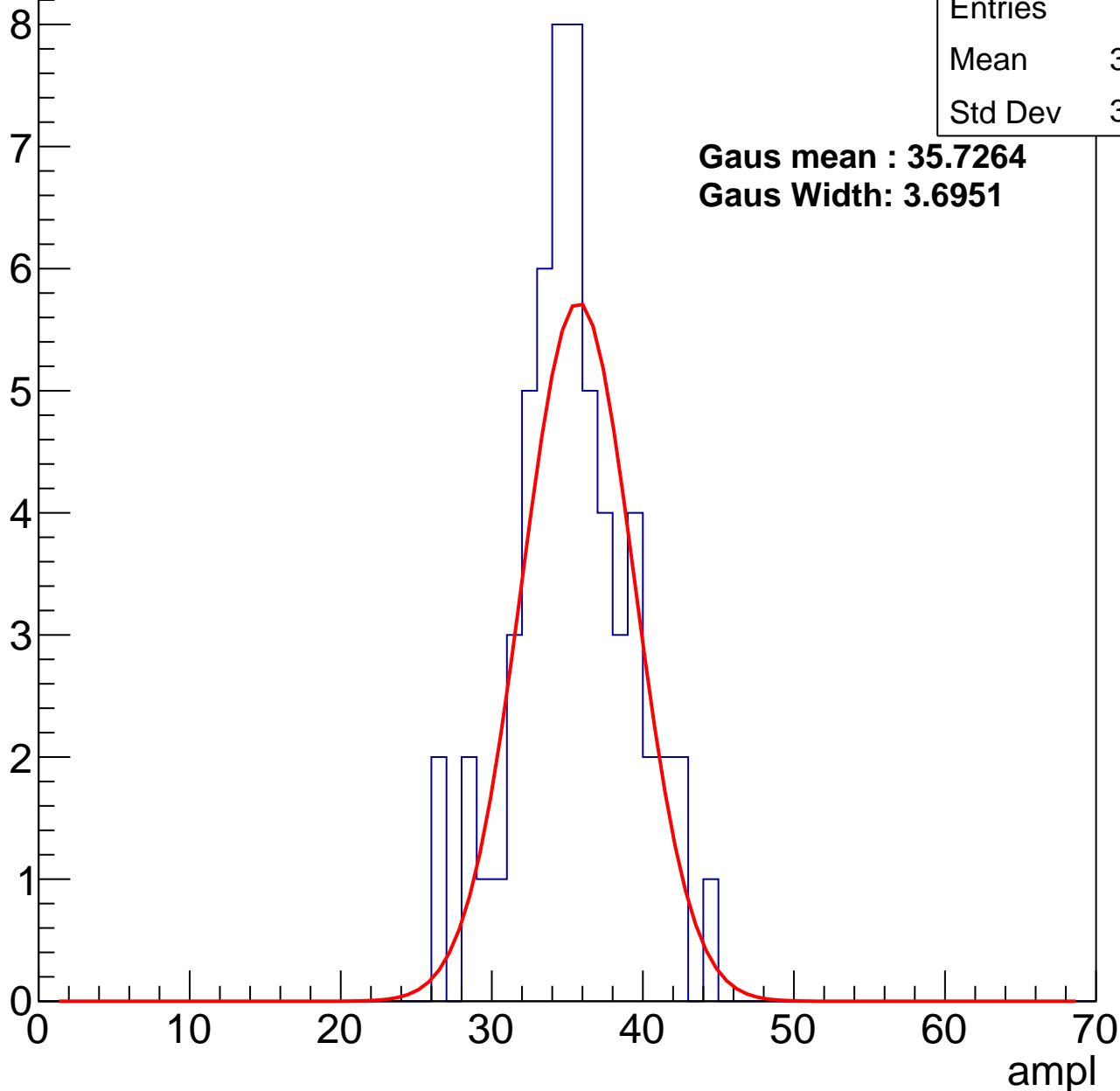
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	59
Mean	34.88
Std Dev	3.814

**Gaus mean : 35.7264**

**Gaus Width: 3.6951**



# B1L101S, U3-ch125, adc2

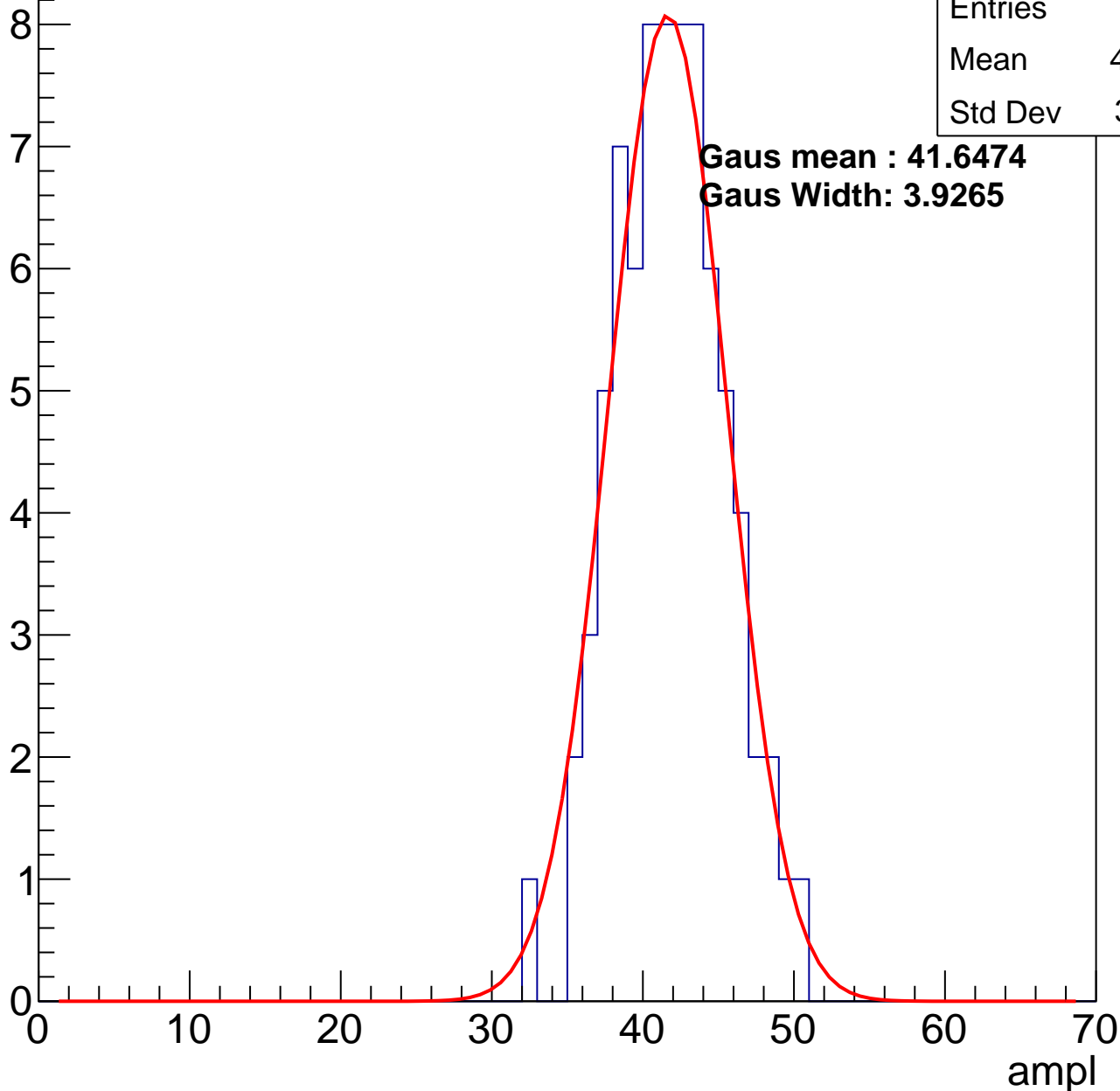
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	77
Mean	41.36
Std Dev	3.571

**Gaus mean : 41.6474**

**Gaus Width: 3.9265**

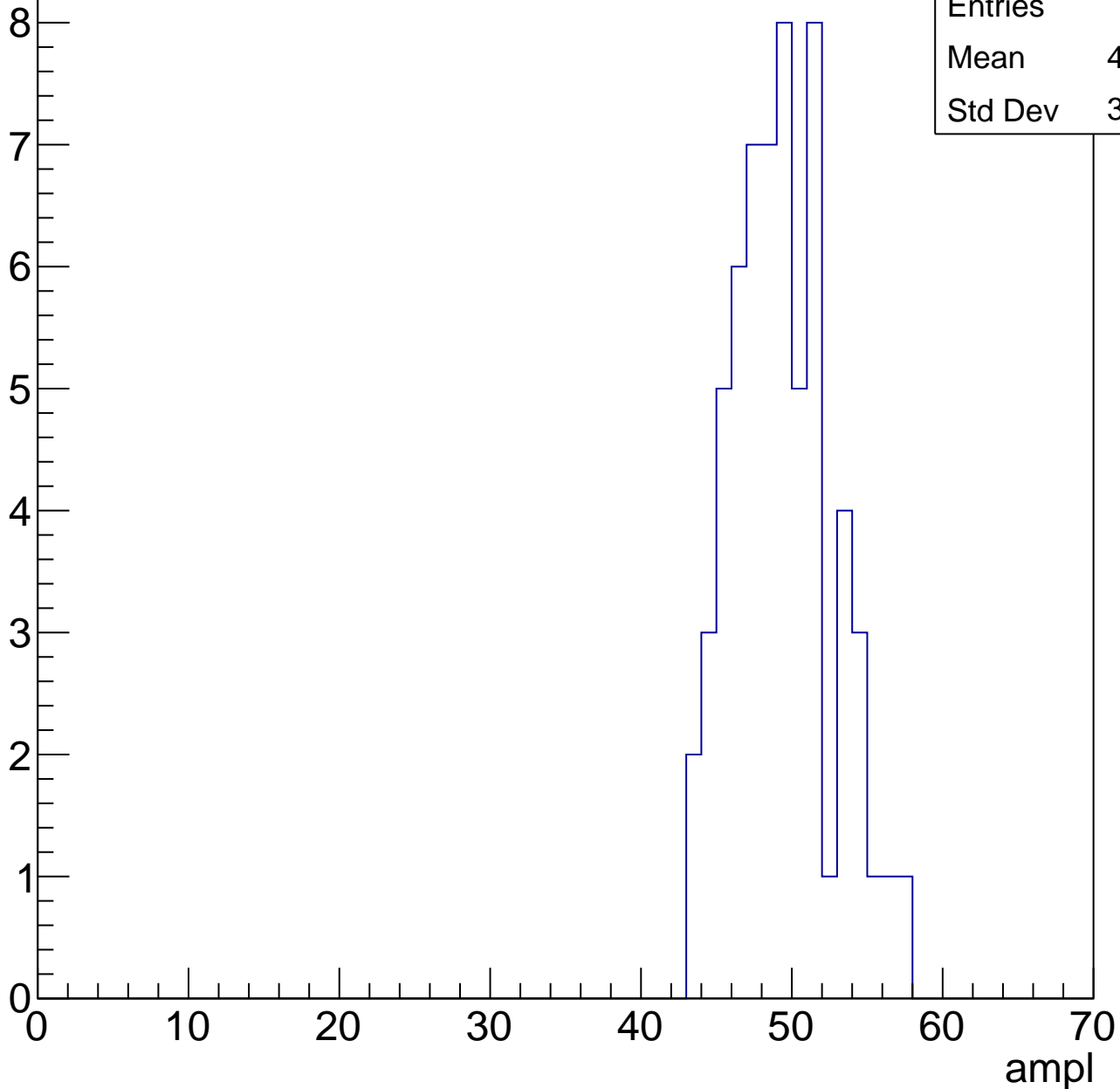


# B1L101S, U3-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

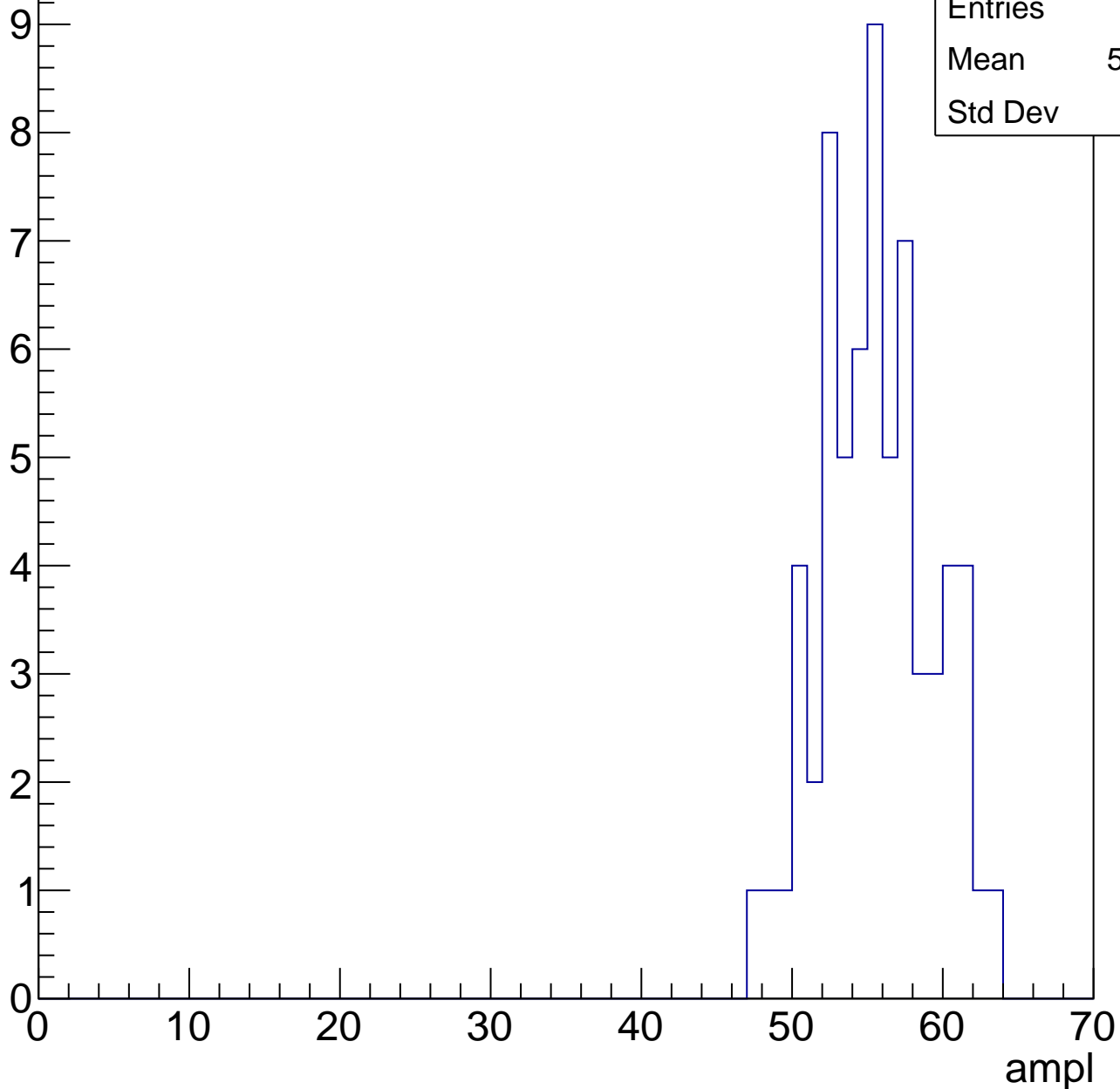
Entries	62
Mean	48.84
Std Dev	3.234



# B1L101S, U3-ch125, adc4

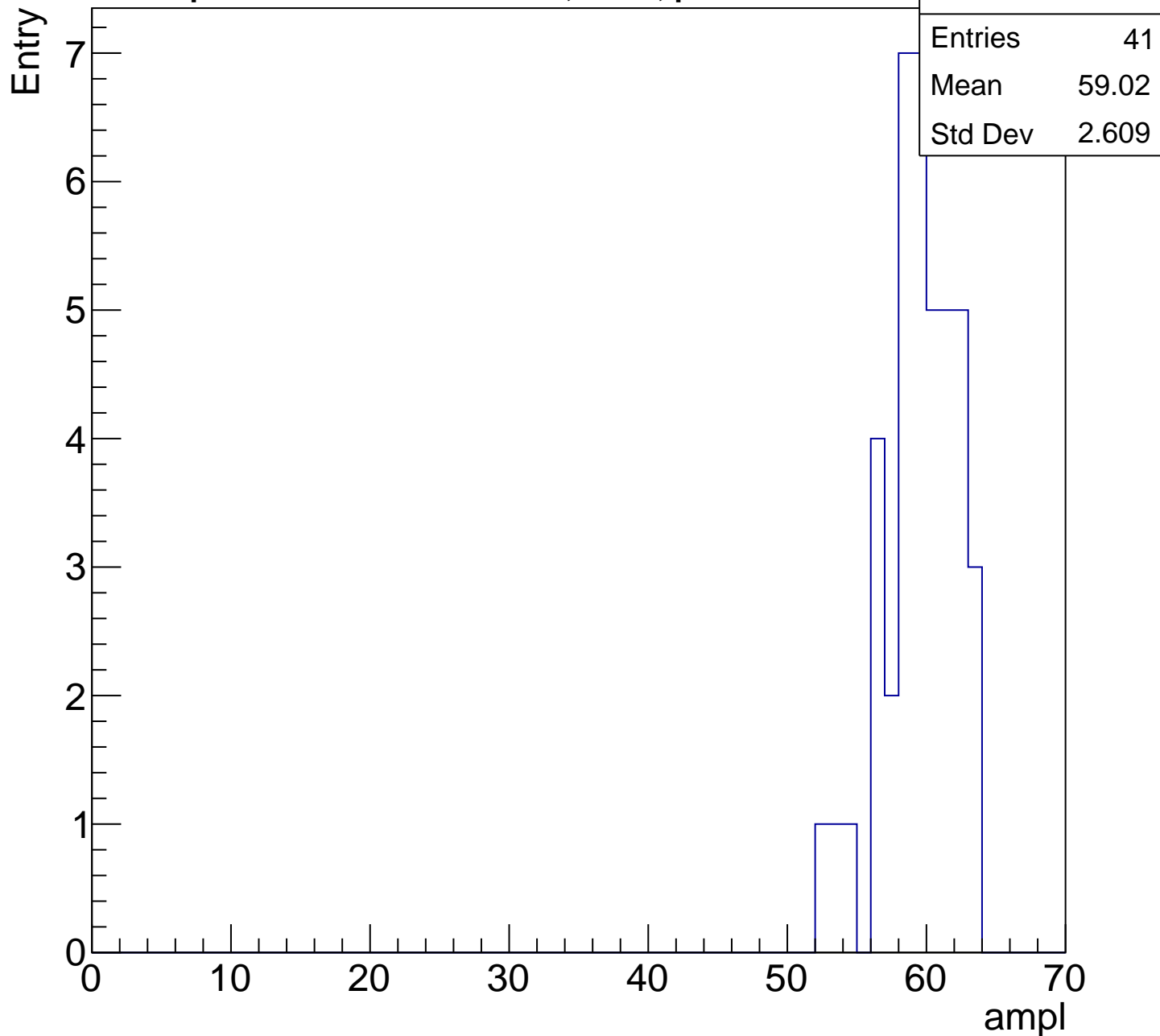
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch125, adc5

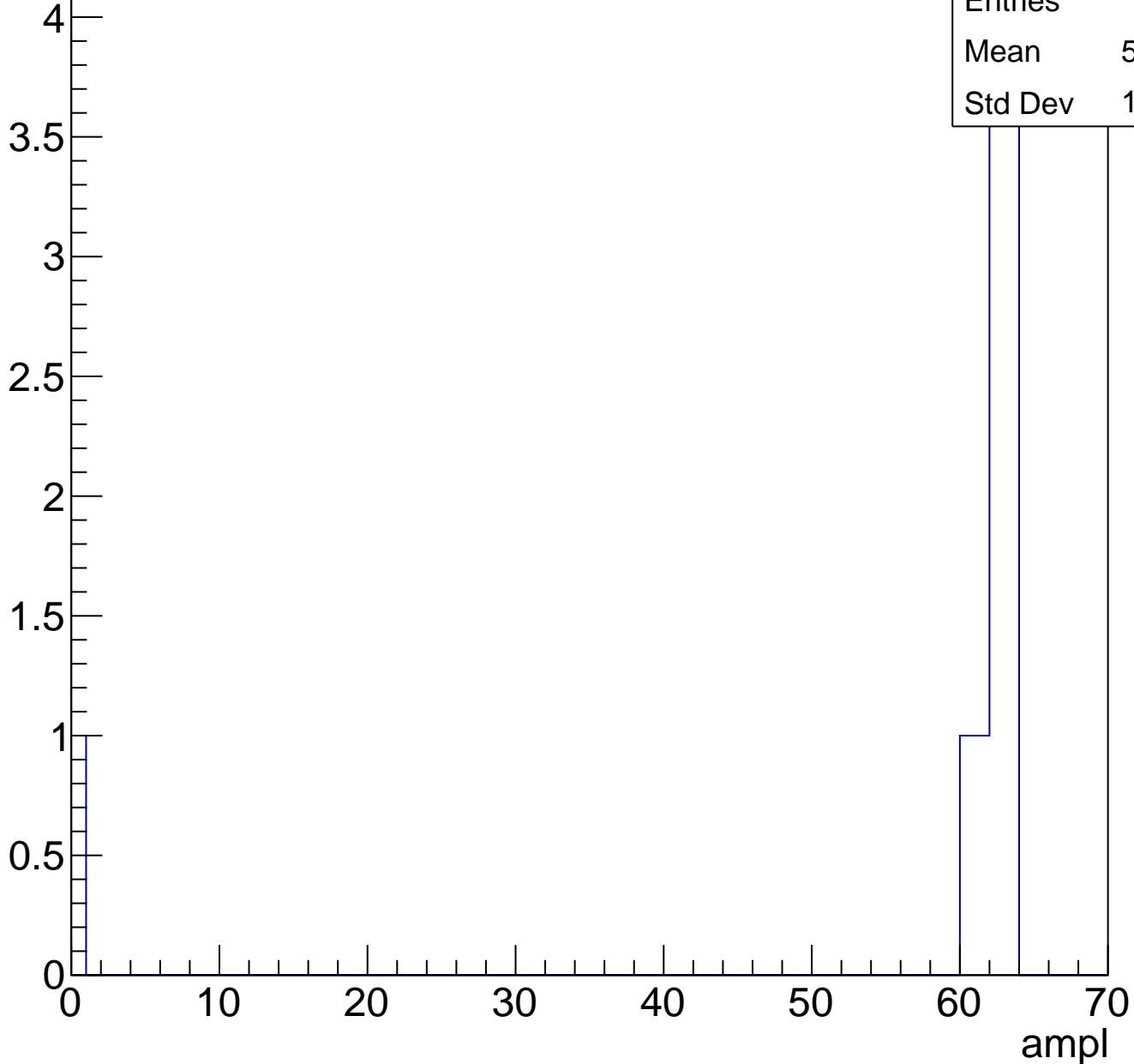
calib\_packv5\_042523\_0143.root, FC#0, port D2



# B1L101S, U3-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



# B1L101S, U3-ch126, adc0

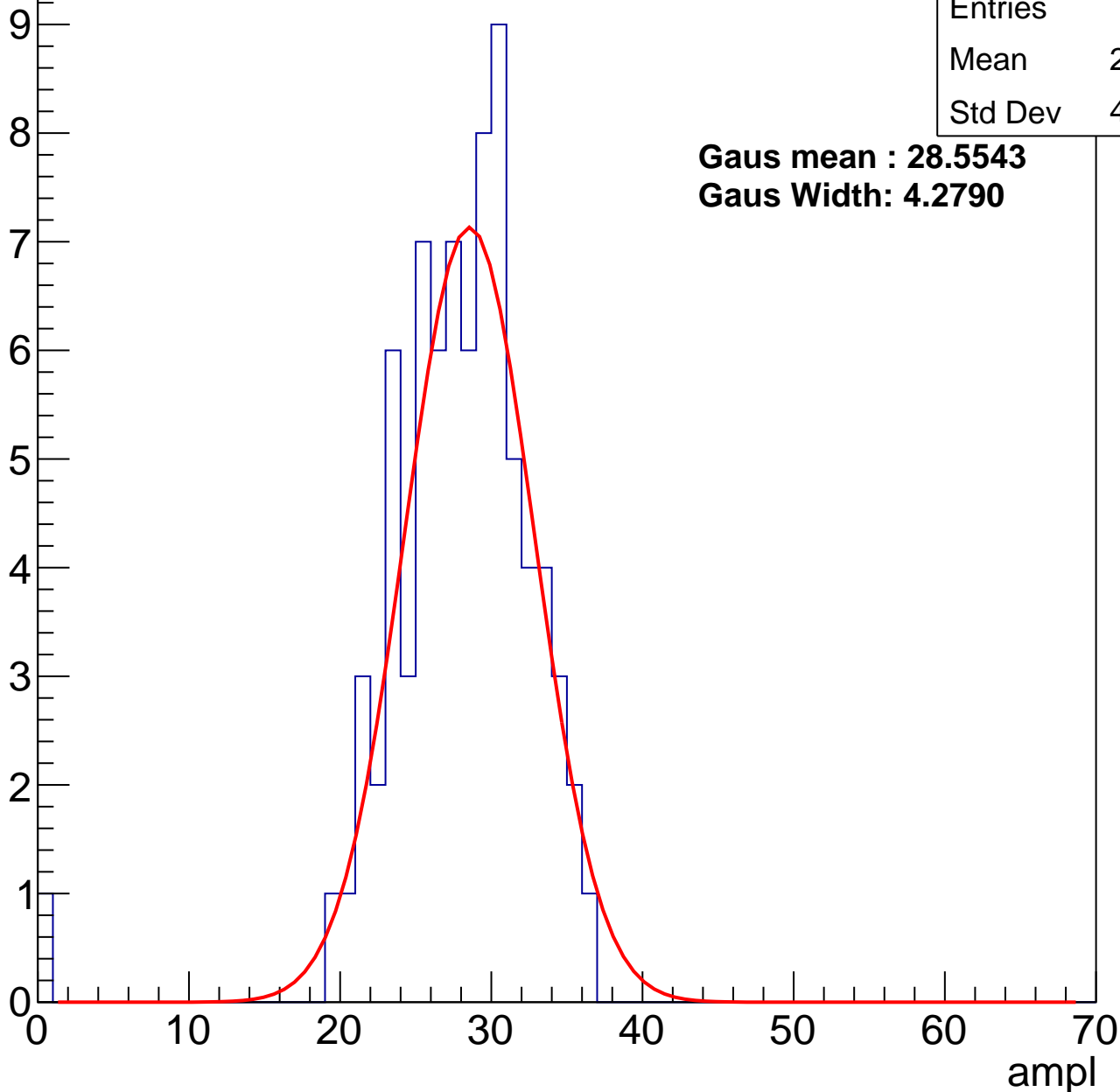
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	79
Mean	27.46
Std Dev	4.955

**Gaus mean : 28.5543**

**Gaus Width: 4.2790**



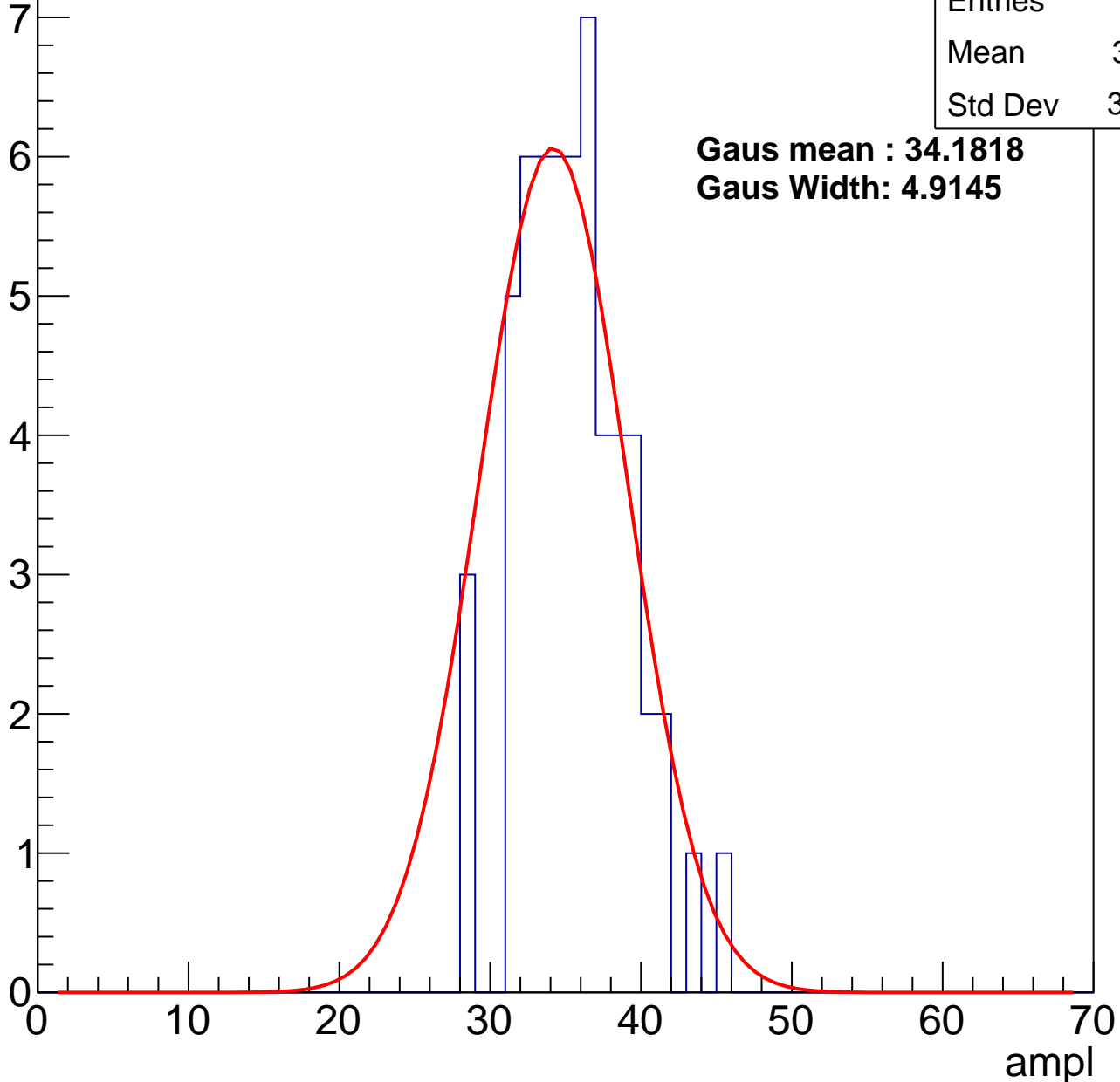
# B1L101S, U3-ch126, adc1

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	57
Mean	35.11
Std Dev	3.553

**Gaus mean : 34.1818**  
**Gaus Width: 4.9145**



# B1L101S, U3-ch126, adc2

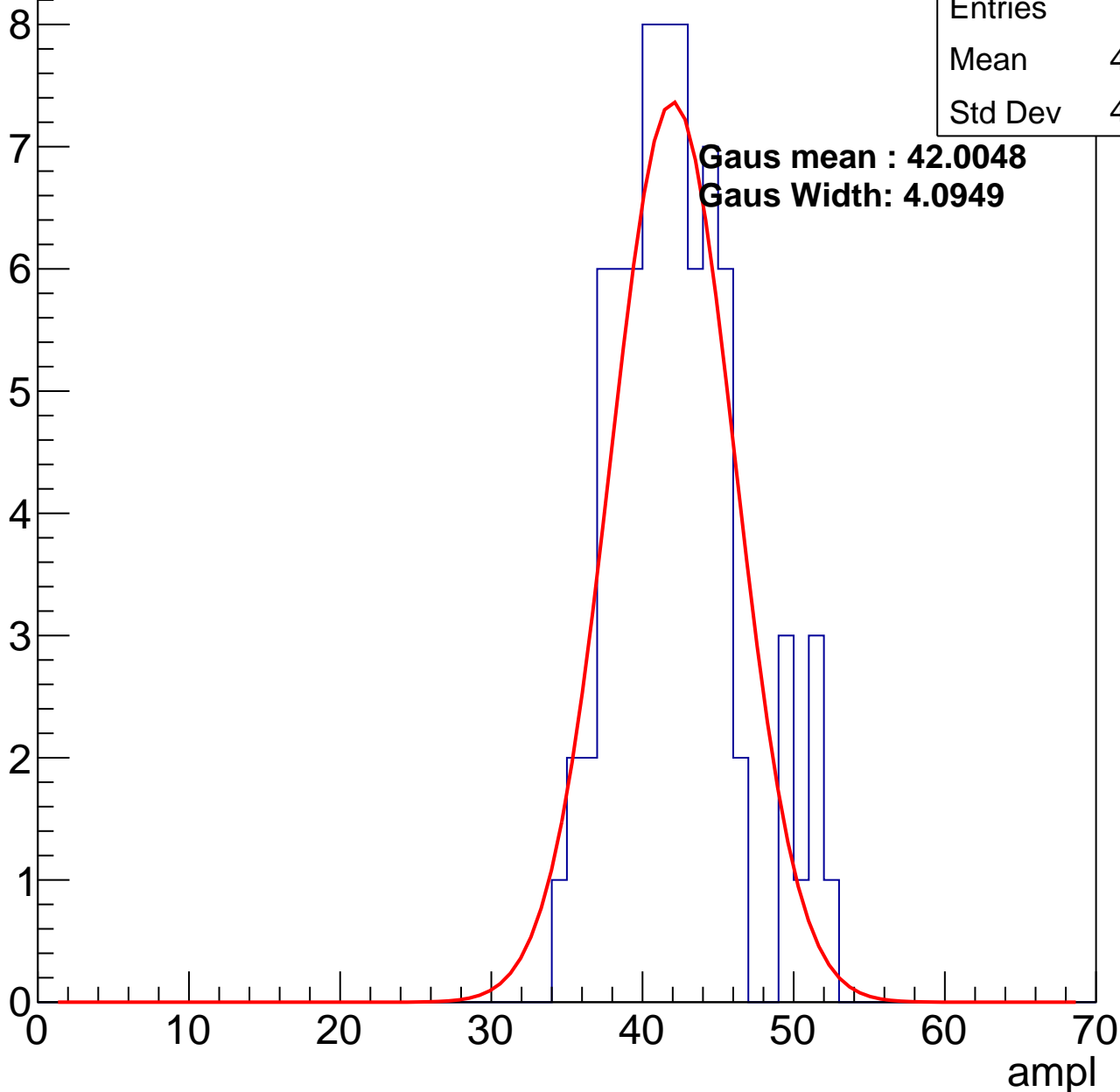
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	76
Mean	41.76
Std Dev	4.045

**Gaus mean : 42.0048**

**Gaus Width: 4.0949**

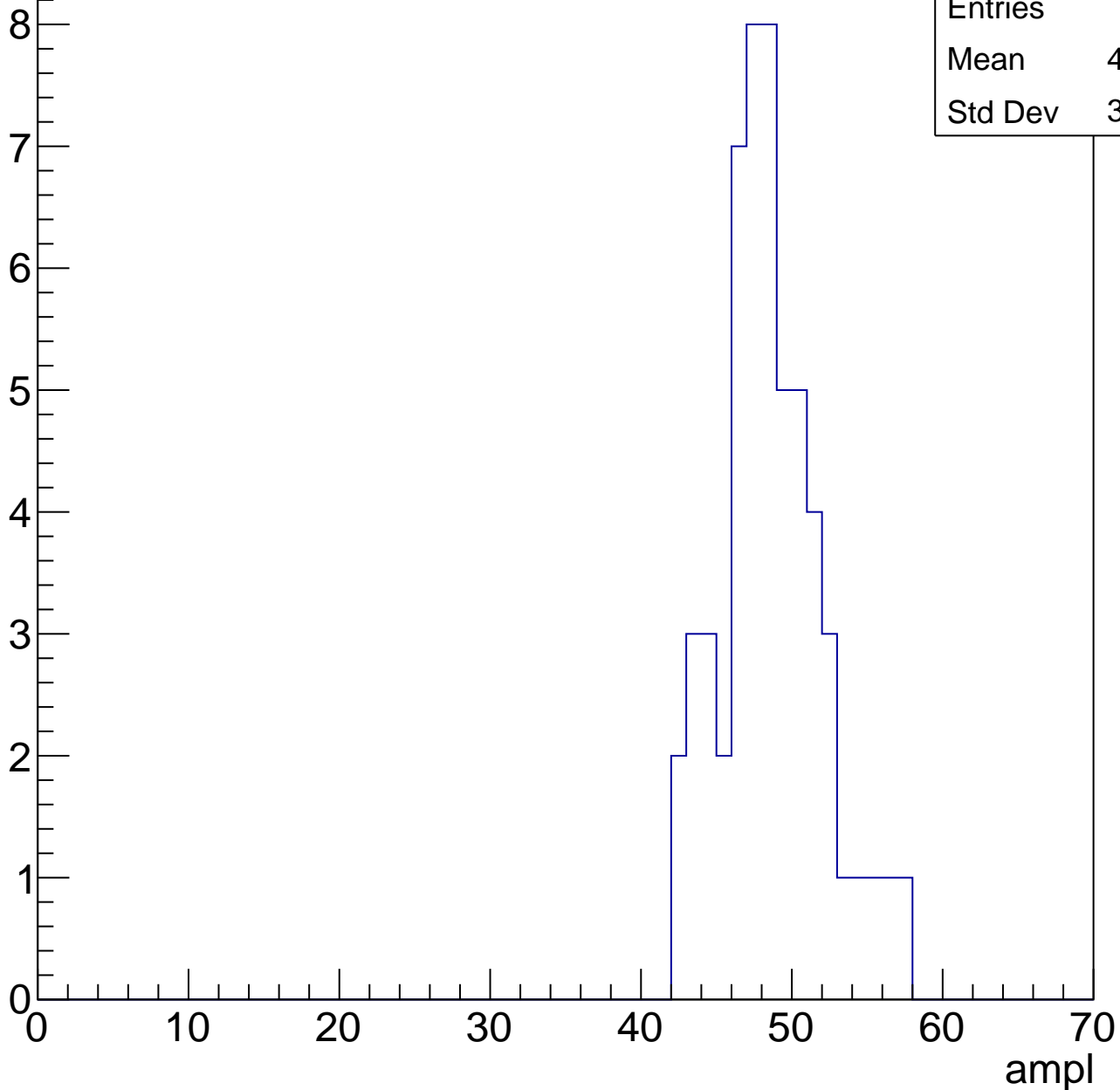


# B1L101S, U3-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	55
Mean	48.13
Std Dev	3.336

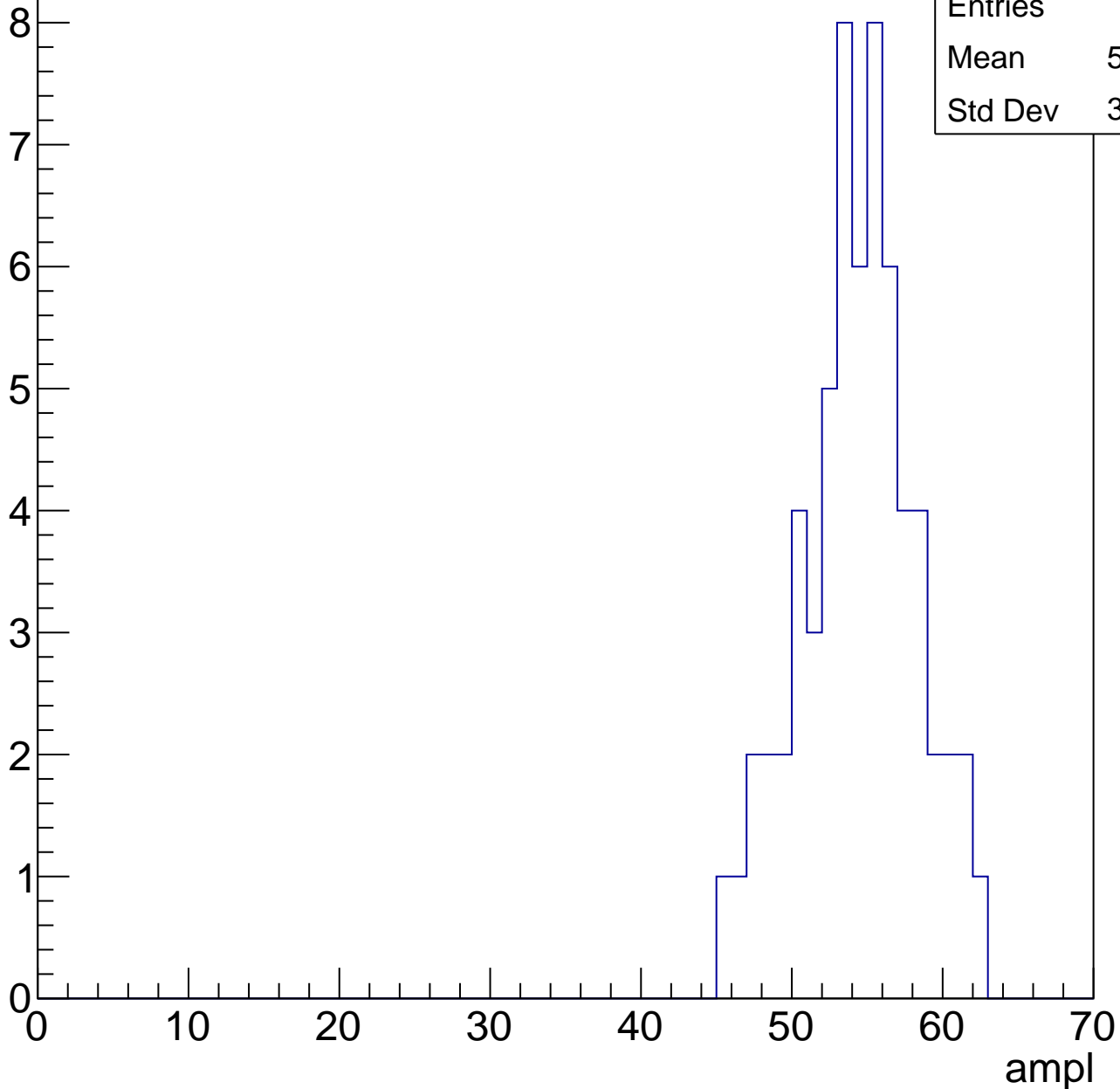


# B1L101S, U3-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	63
Mean	53.94
Std Dev	3.779



# B1L101S, U3-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

7

6

5

4

3

2

1

0

Entries 51

Mean 59.27

Std Dev 2.87

ampl

0

10

20

30

40

50

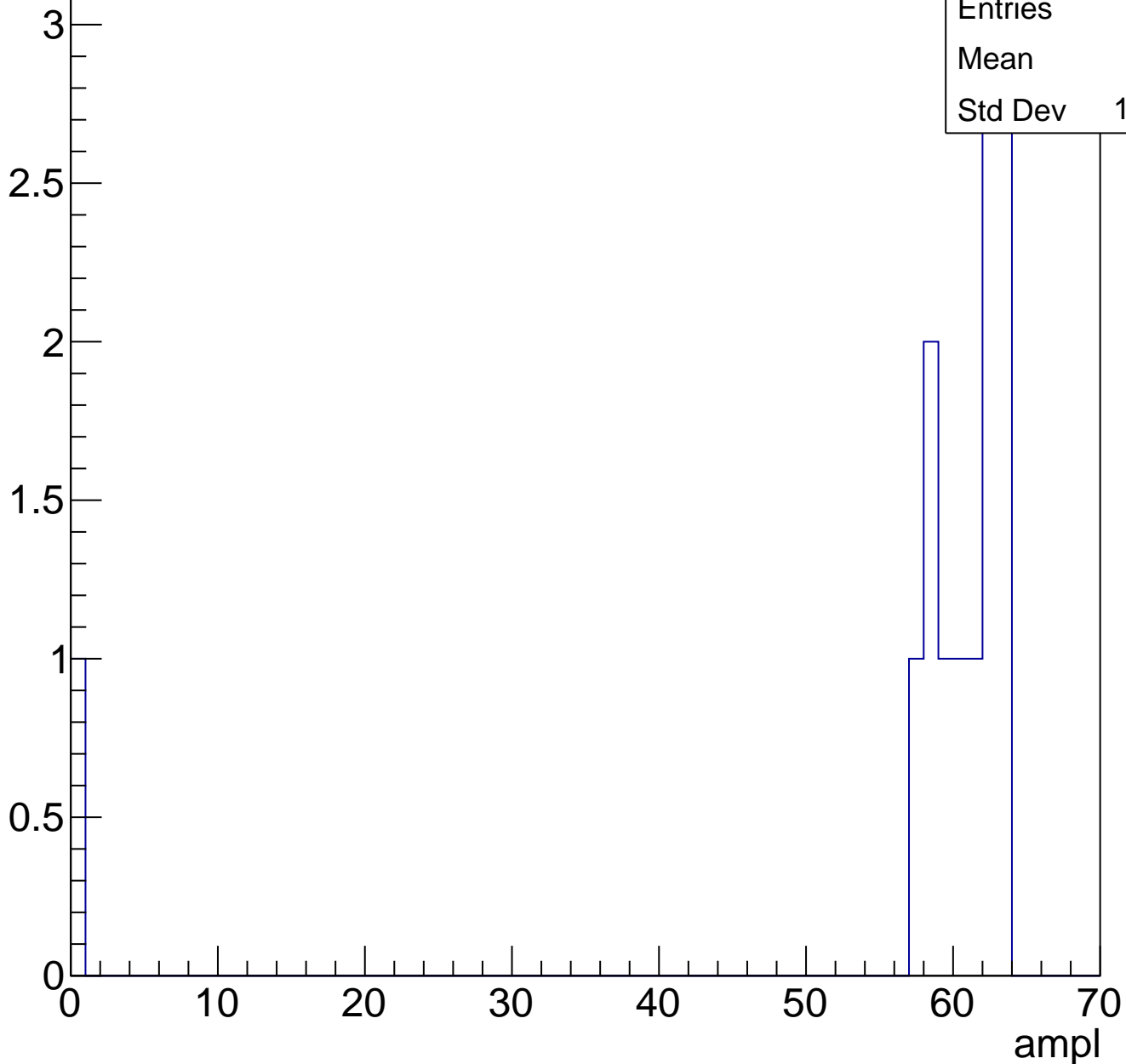
60

70

# B1L101S, U3-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry





# B1L101S, U3-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L101S, U3-ch127, adc0

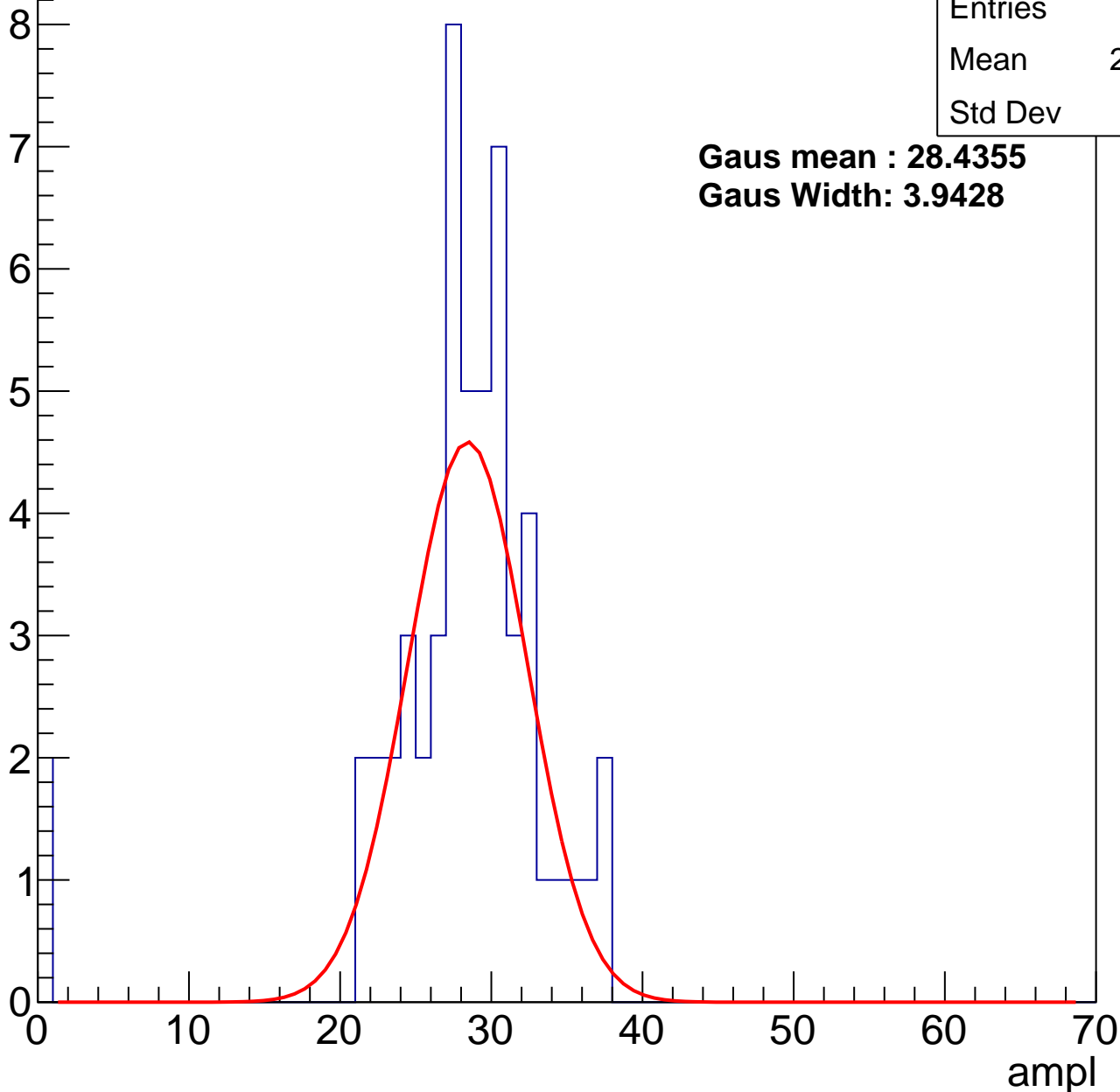
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	27.33
Std Dev	6.54

**Gaus mean : 28.4355**

**Gaus Width: 3.9428**



# B1L101S, U3-ch127, adc1

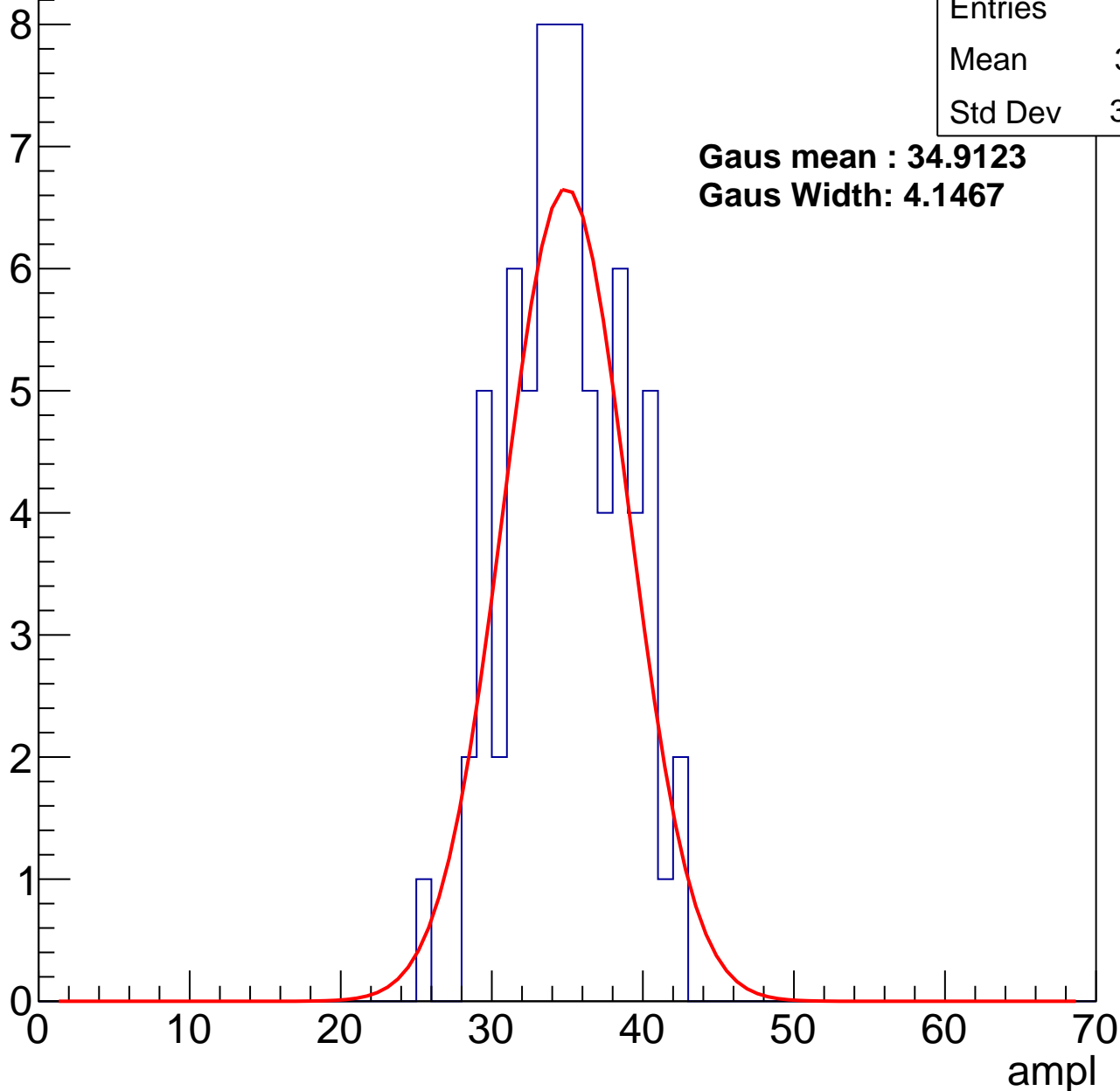
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	34.51
Std Dev	3.708

**Gaus mean : 34.9123**

**Gaus Width: 4.1467**



# B1L101S, U3-ch127, adc2

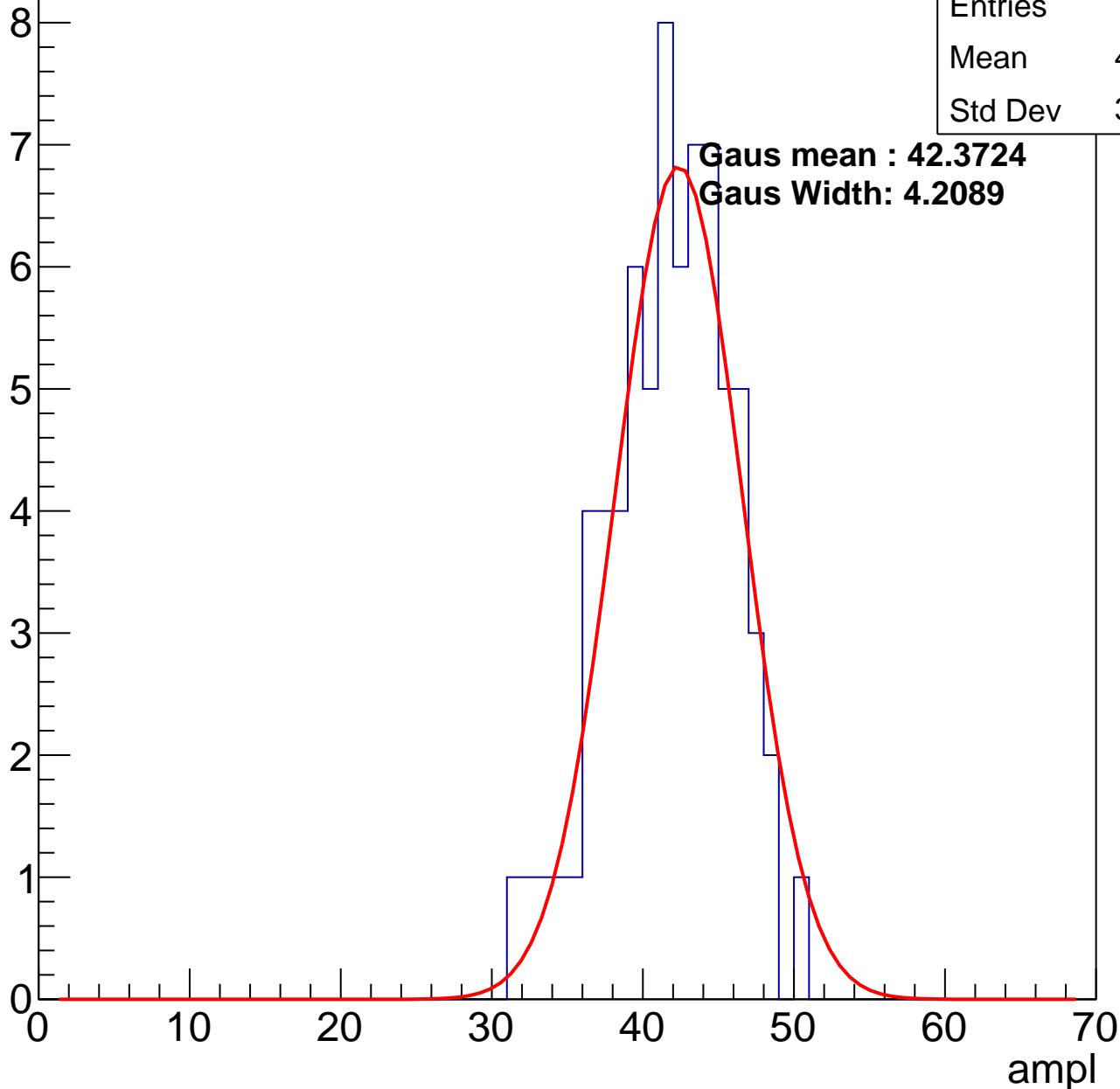
calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	72
Mean	41.31
Std Dev	3.981

**Gaus mean : 42.3724**

**Gaus Width: 4.2089**

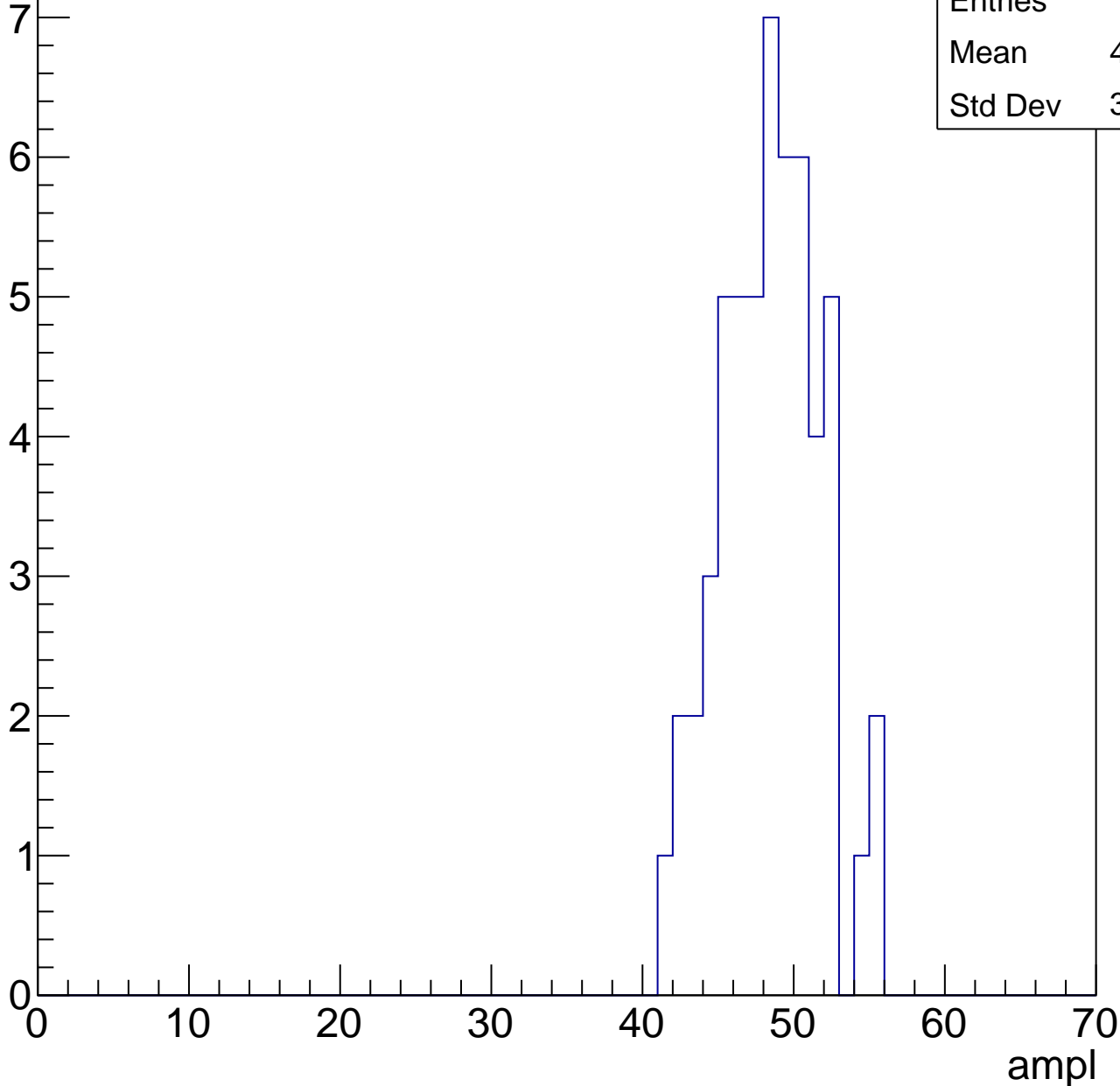


# B1L101S, U3-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	54
Mean	47.98
Std Dev	3.246



# B1L101S, U3-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entries	64
Mean	53.83
Std Dev	3.719

Entry

10

8

6

4

2

0

0

10

20

30

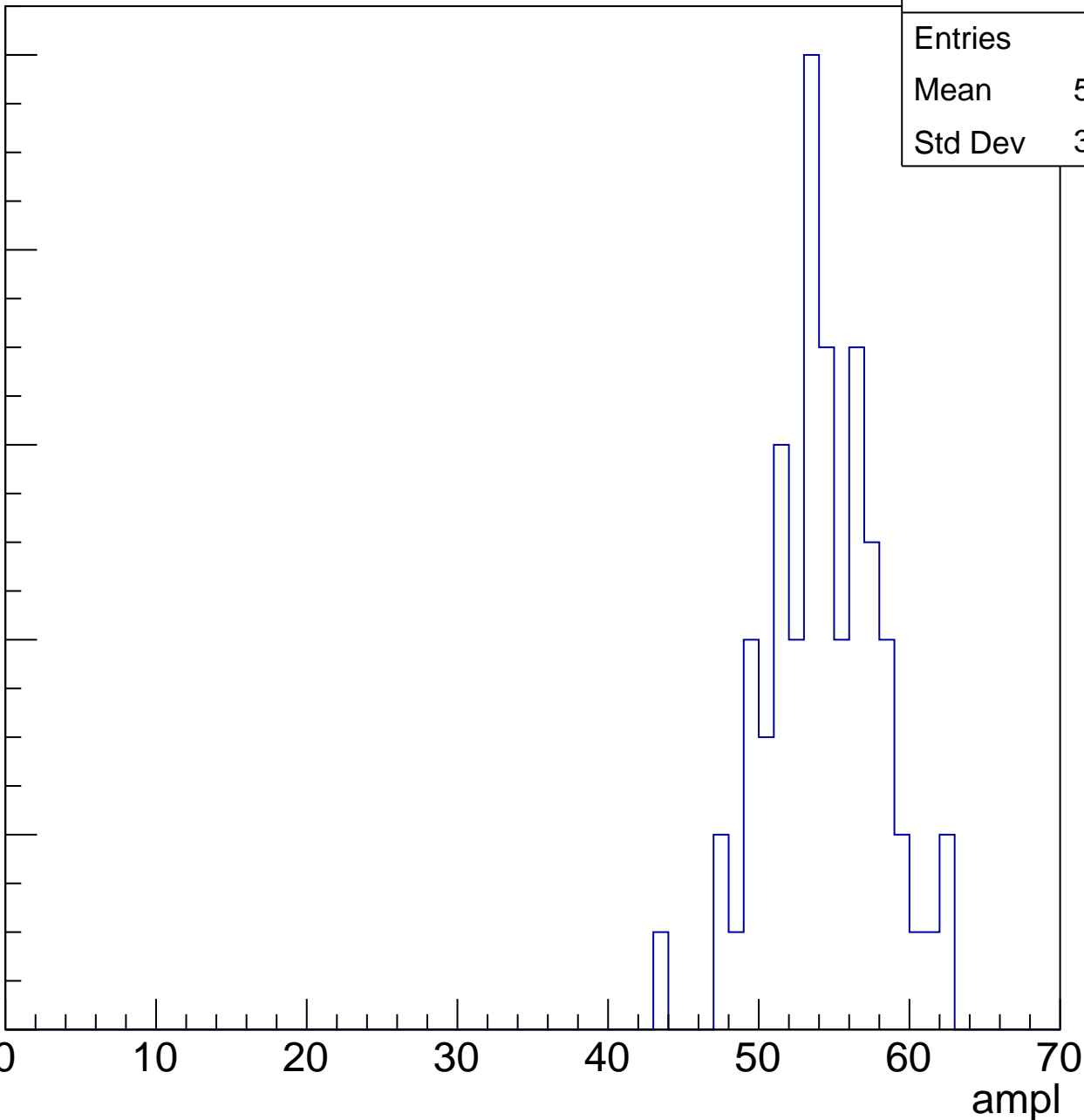
40

50

60

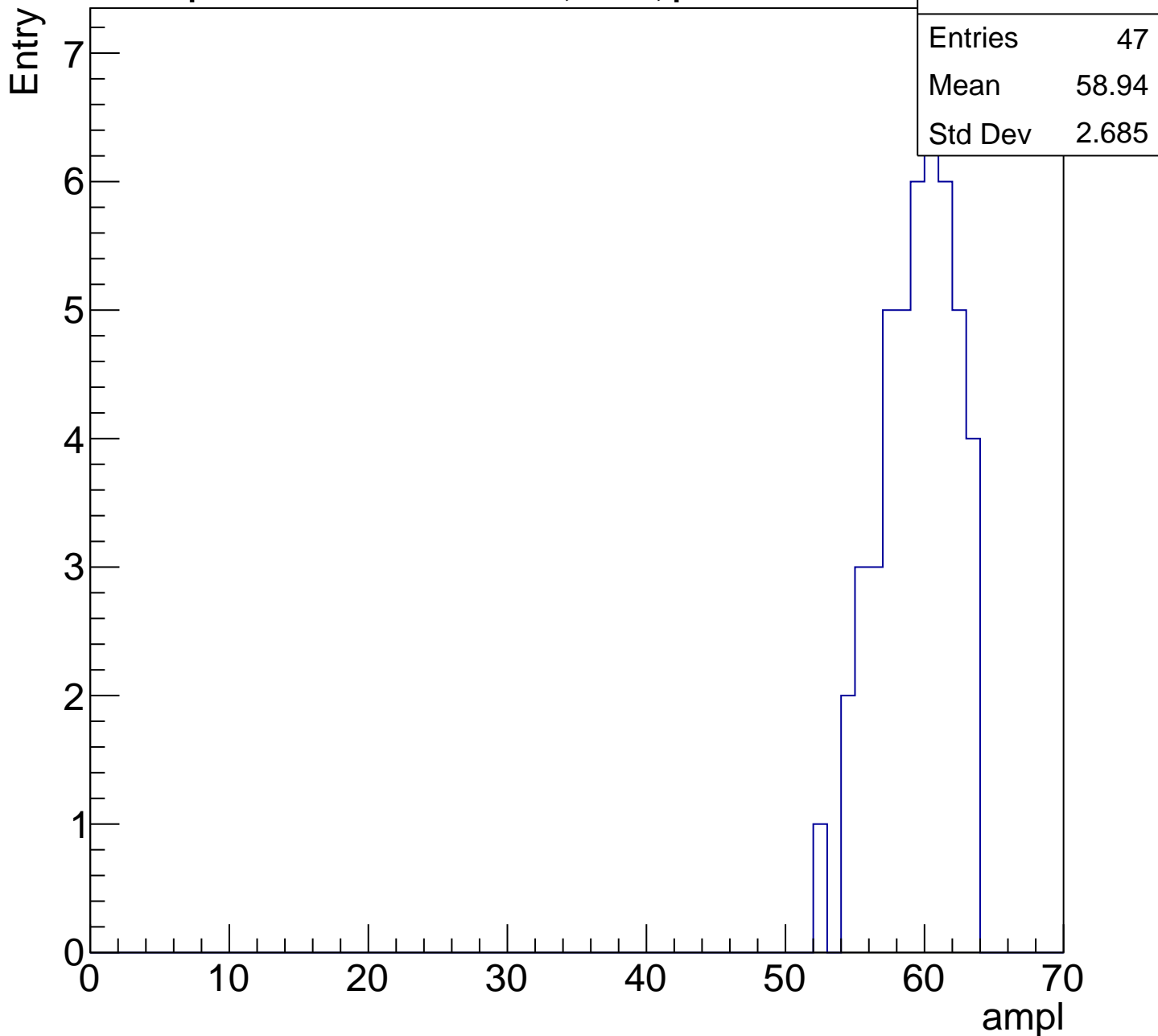
70

ampl



# B1L101S, U3-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#0, port D2

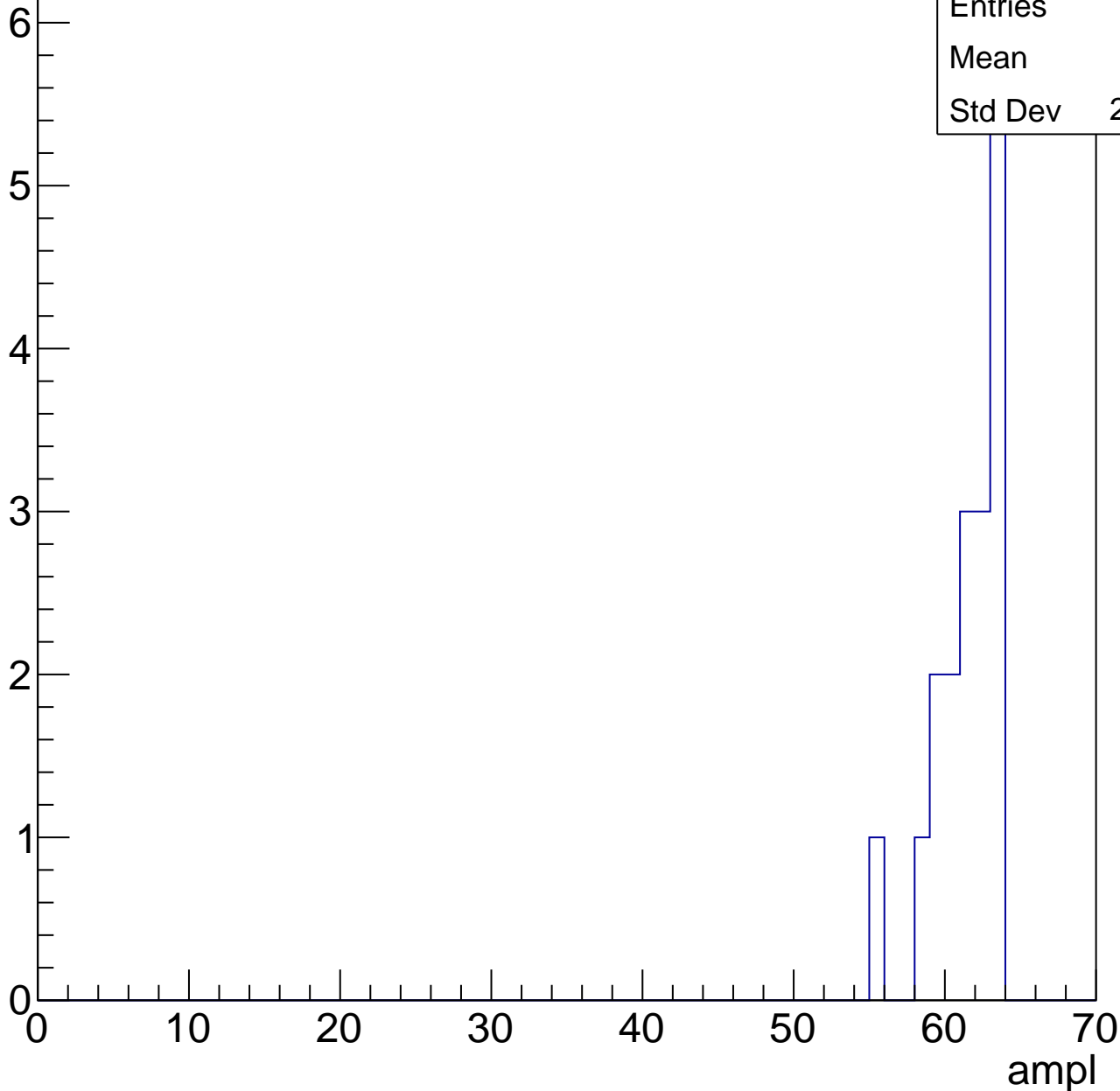


# B1L101S, U3-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

Entries	18
Mean	61
Std Dev	2.134





# B1L101S, U3-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry

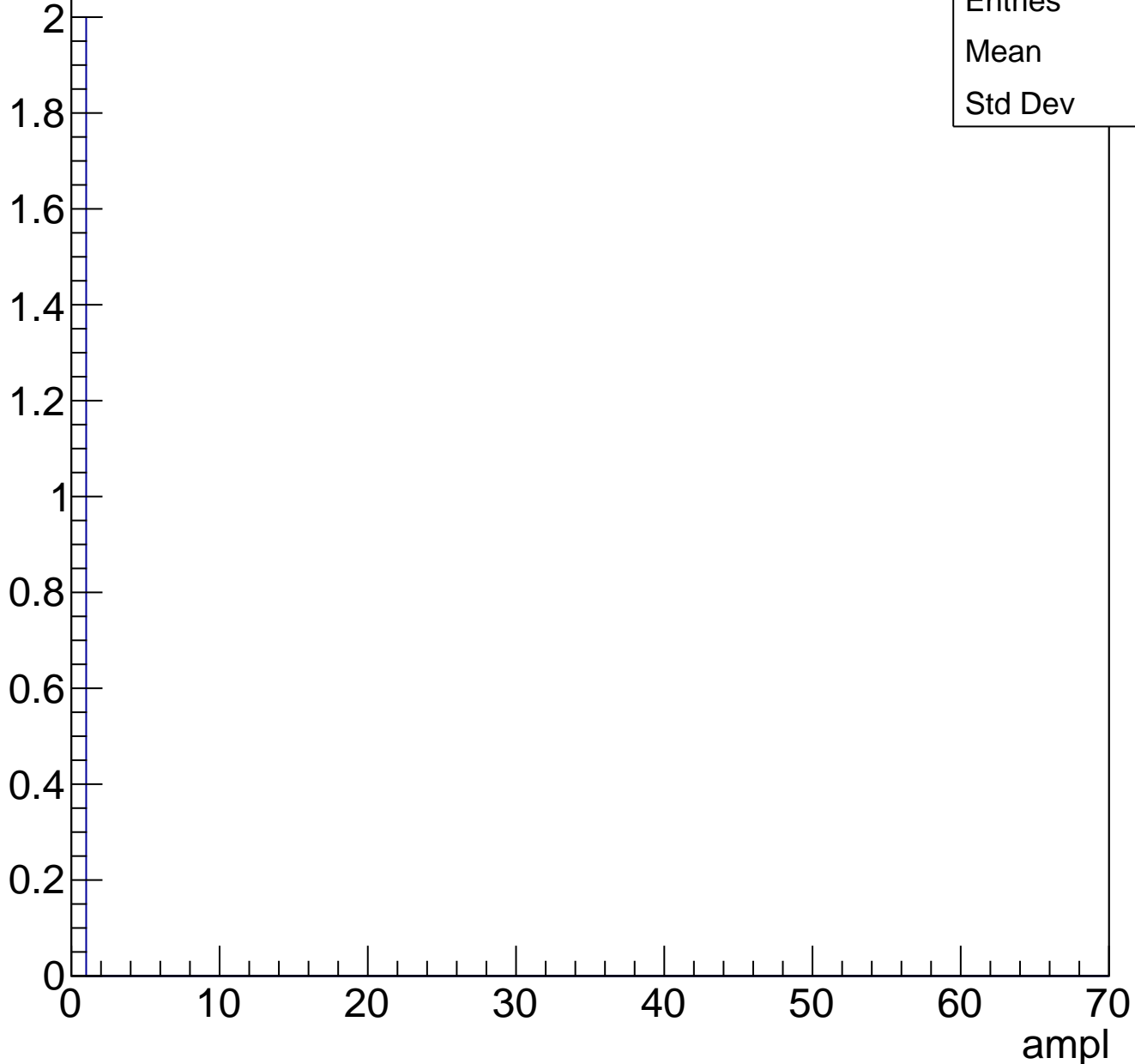


Entries	2
Mean	0
Std Dev	0

# B1L101S, U3-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#0, port D2

Entry



Entries	2
Mean	0
Std Dev	0