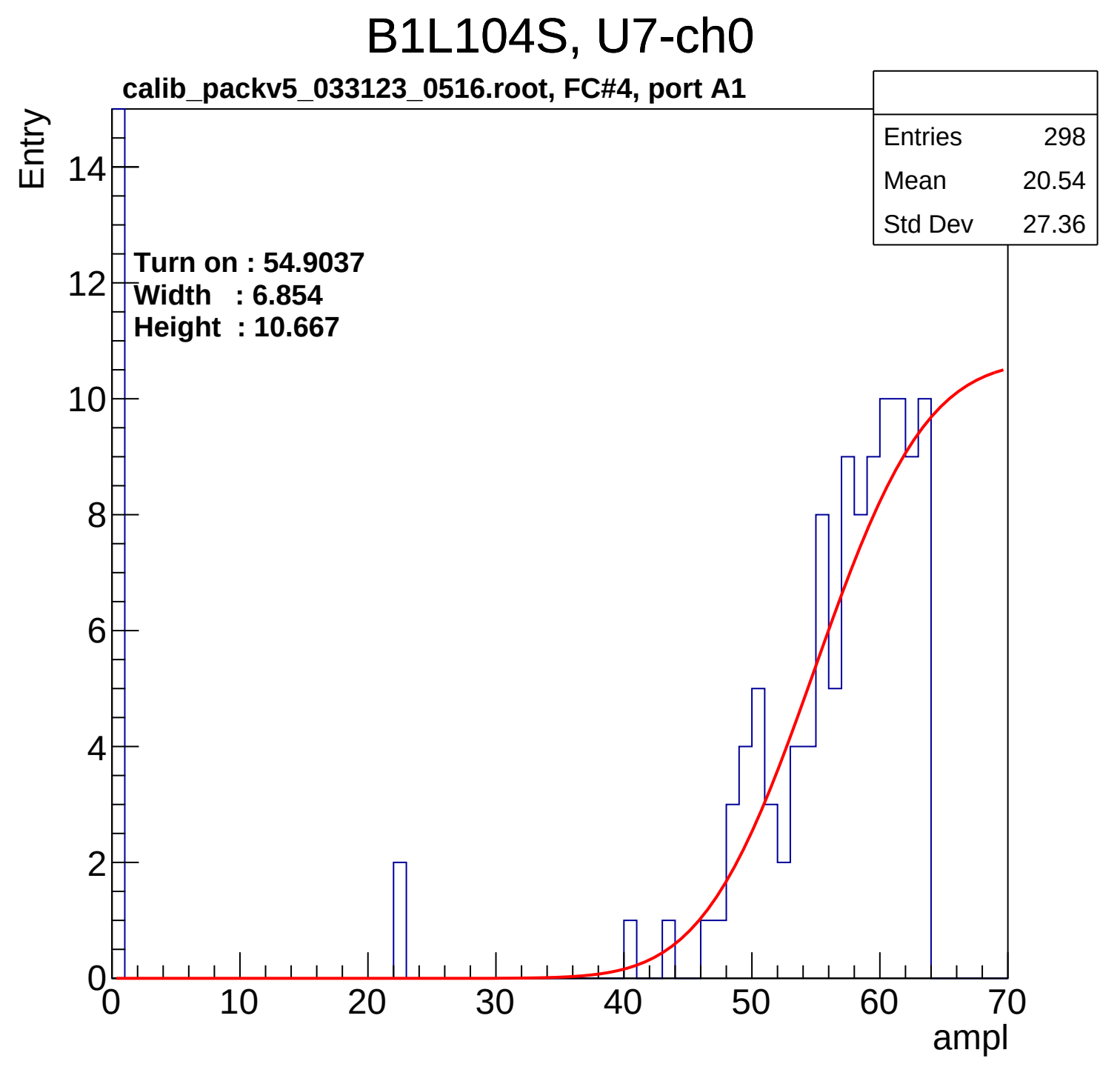
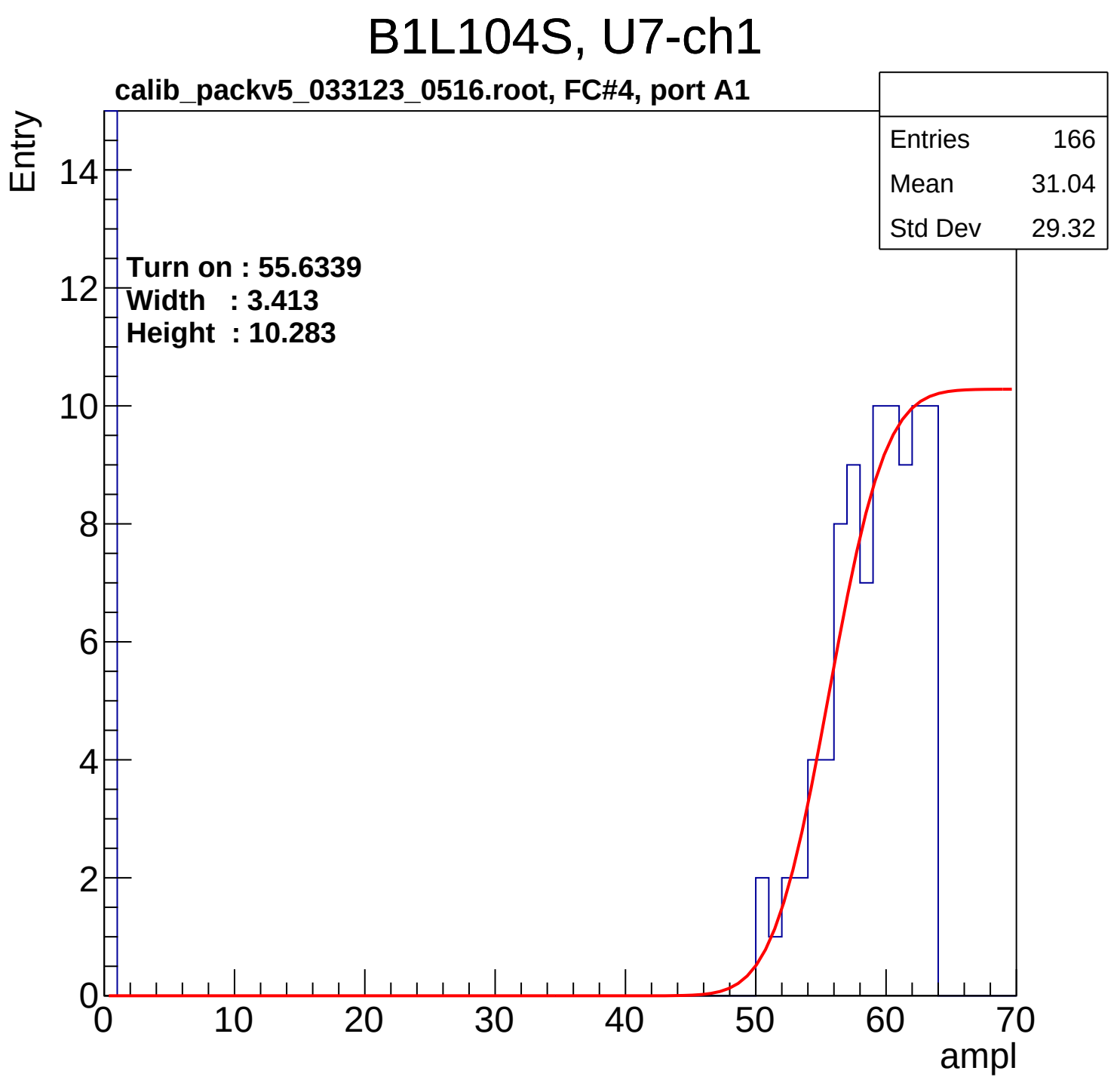
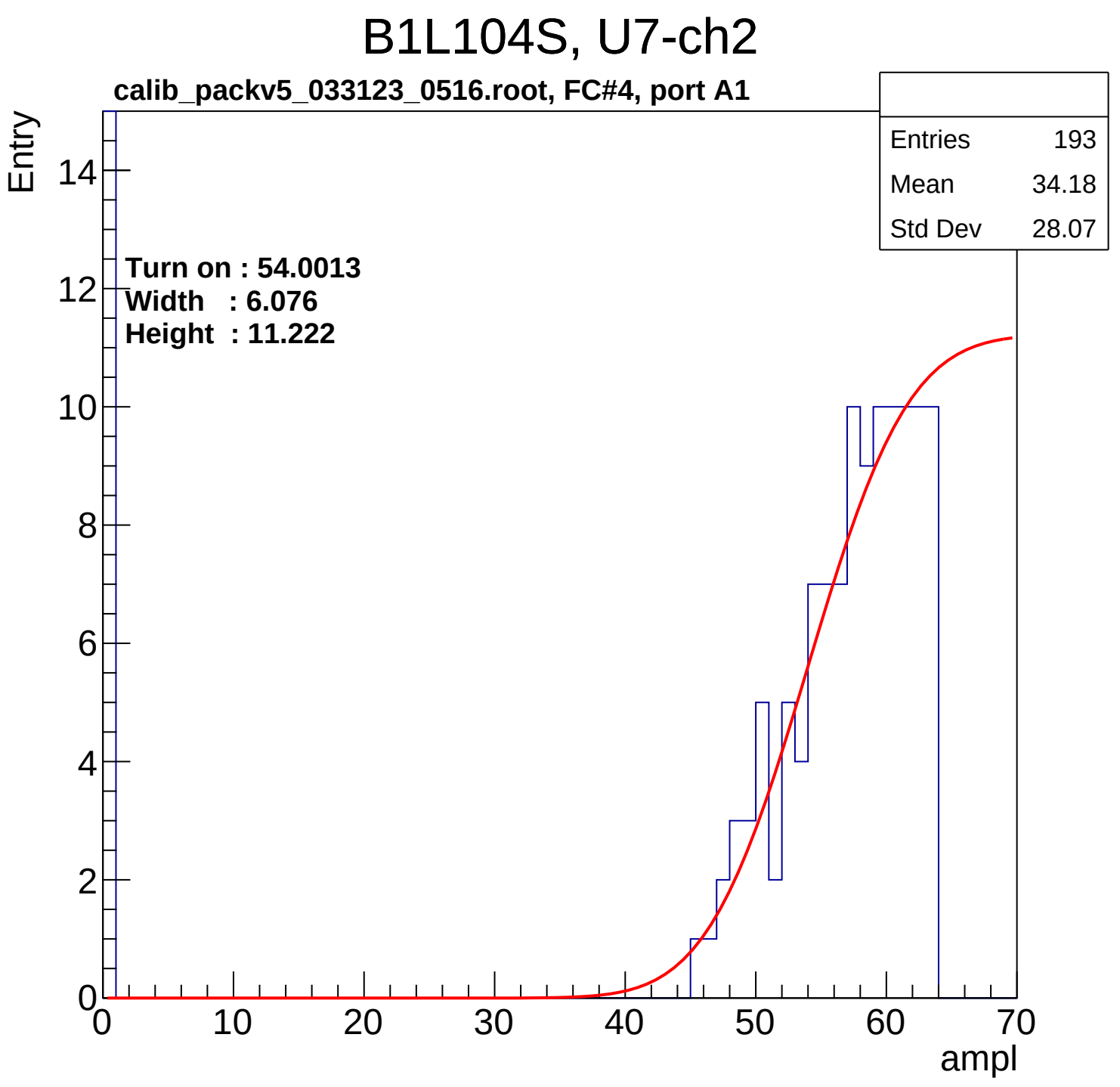
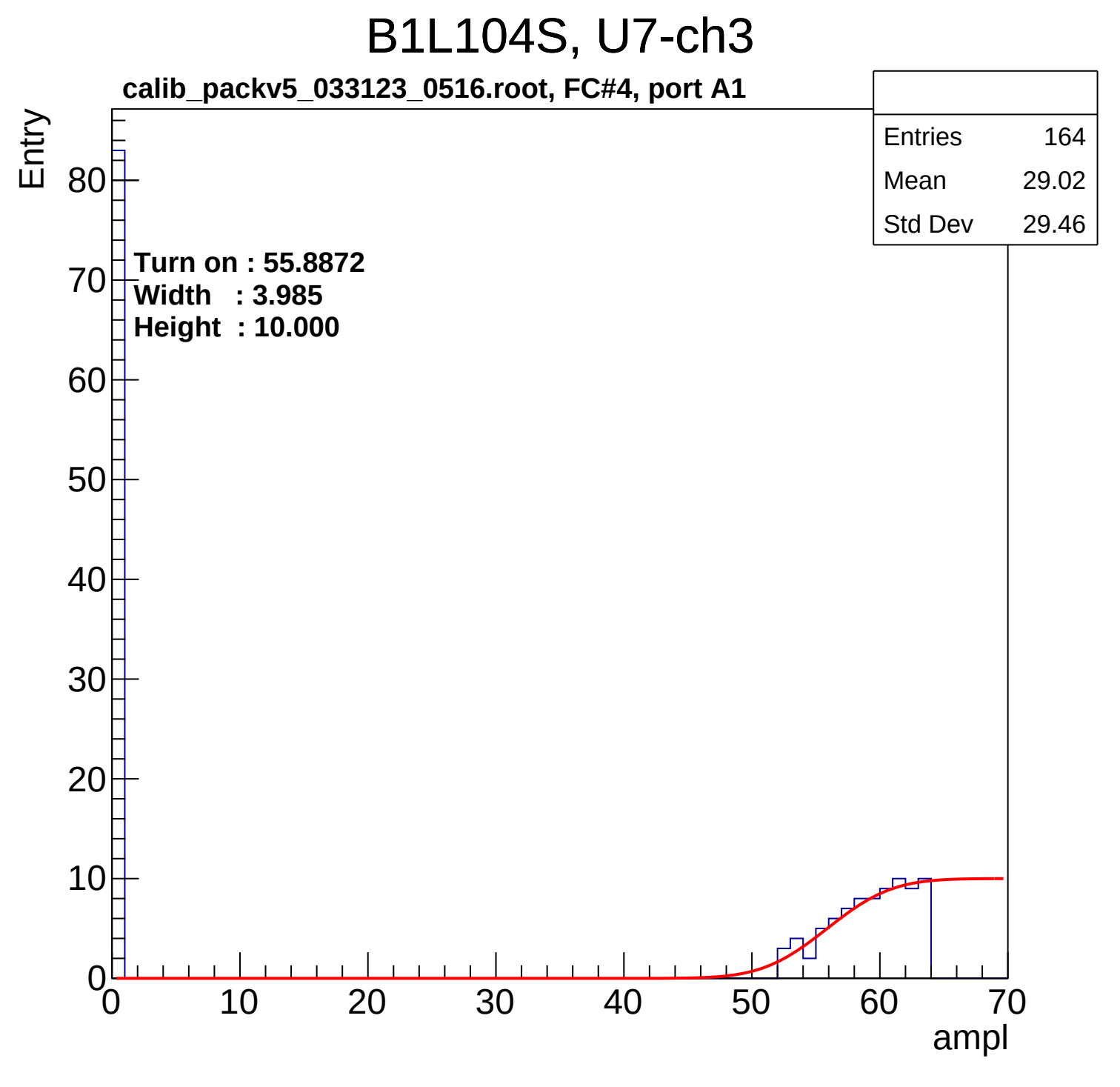
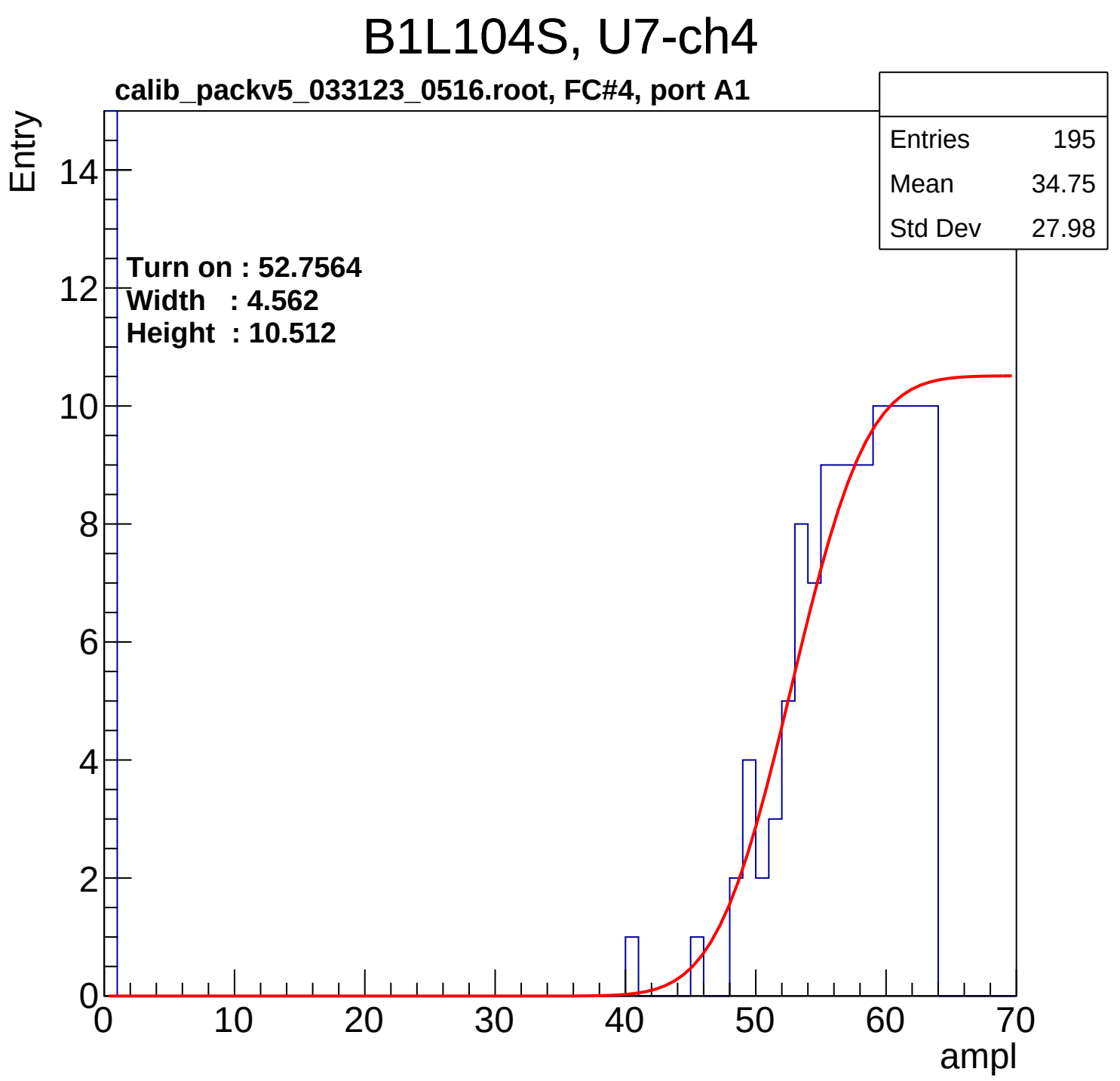
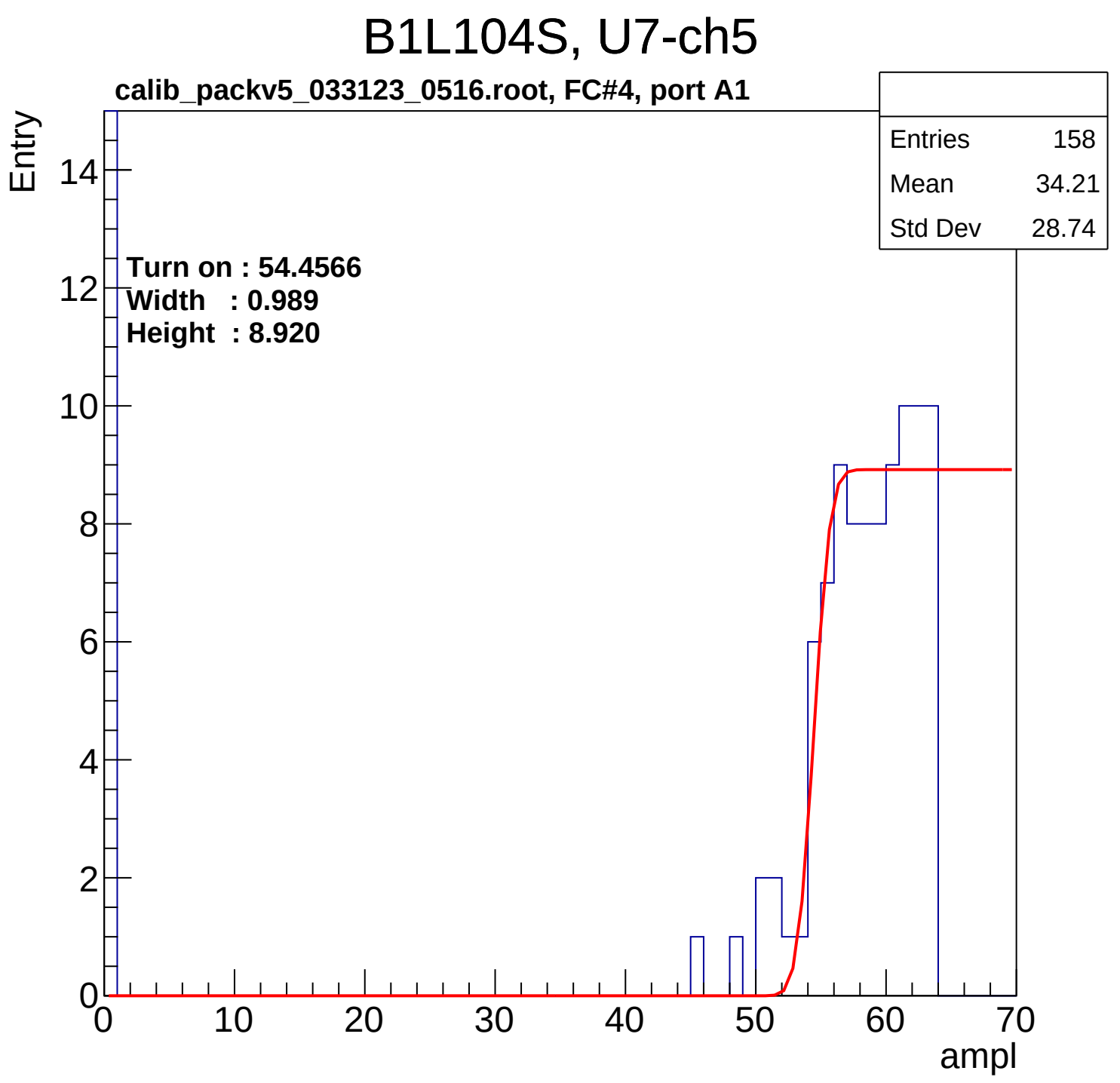

B1L104S, U7-ch0
calib_packv5_033123_0516.root, FC#4, port A1
Entries 298
Mean 20.54
Std Dev 27.36
Turn on : 54.9037
Width : 6.854
Height : 10.667
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

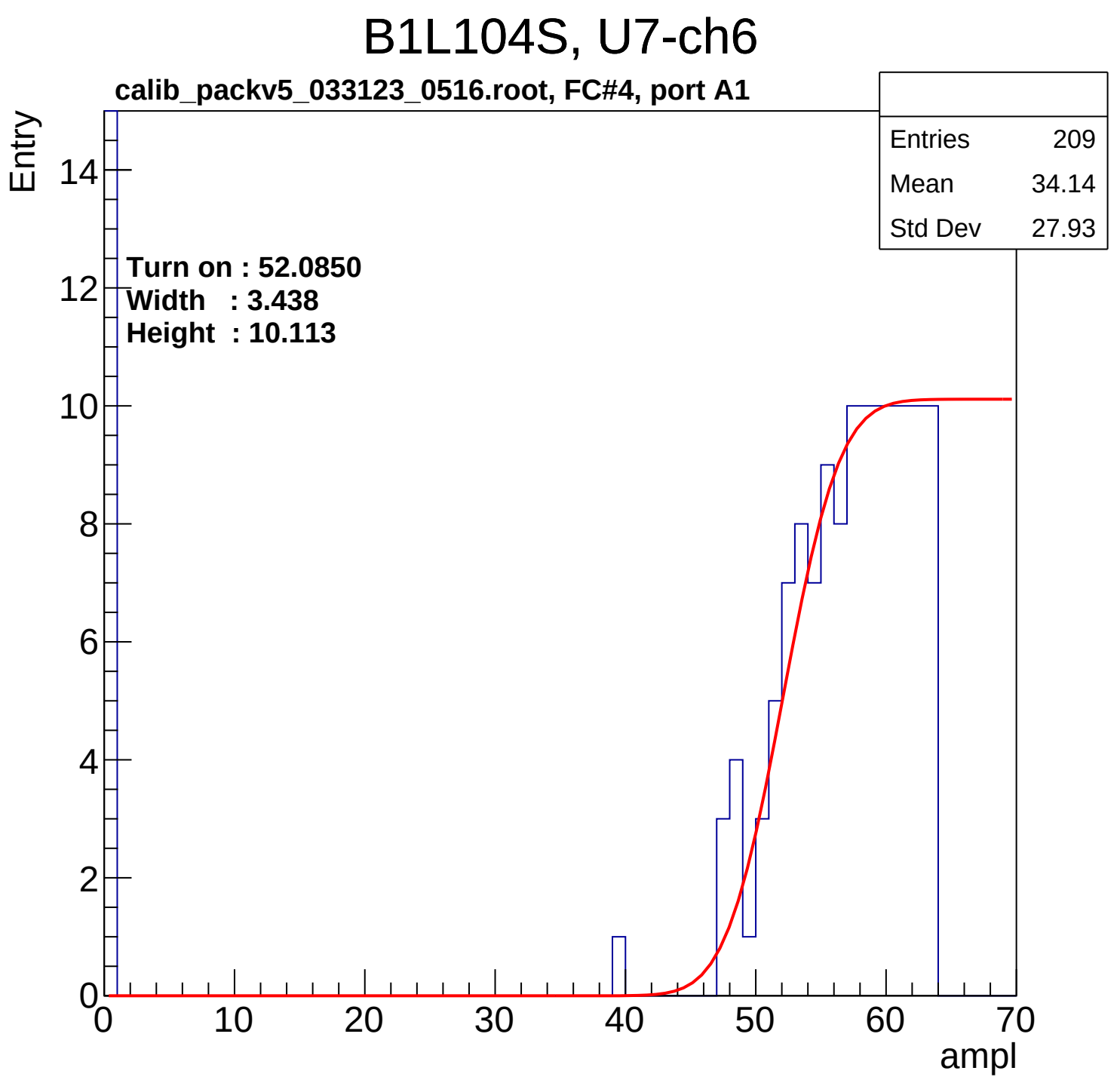

B1L104S, U7-ch1
calib_packv5_033123_0516.root, FC#4, port A1
Entries 166
Mean 31.04
Std Dev 29.32
Turn on : 55.6339
Width : 3.413
Height : 10.283
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

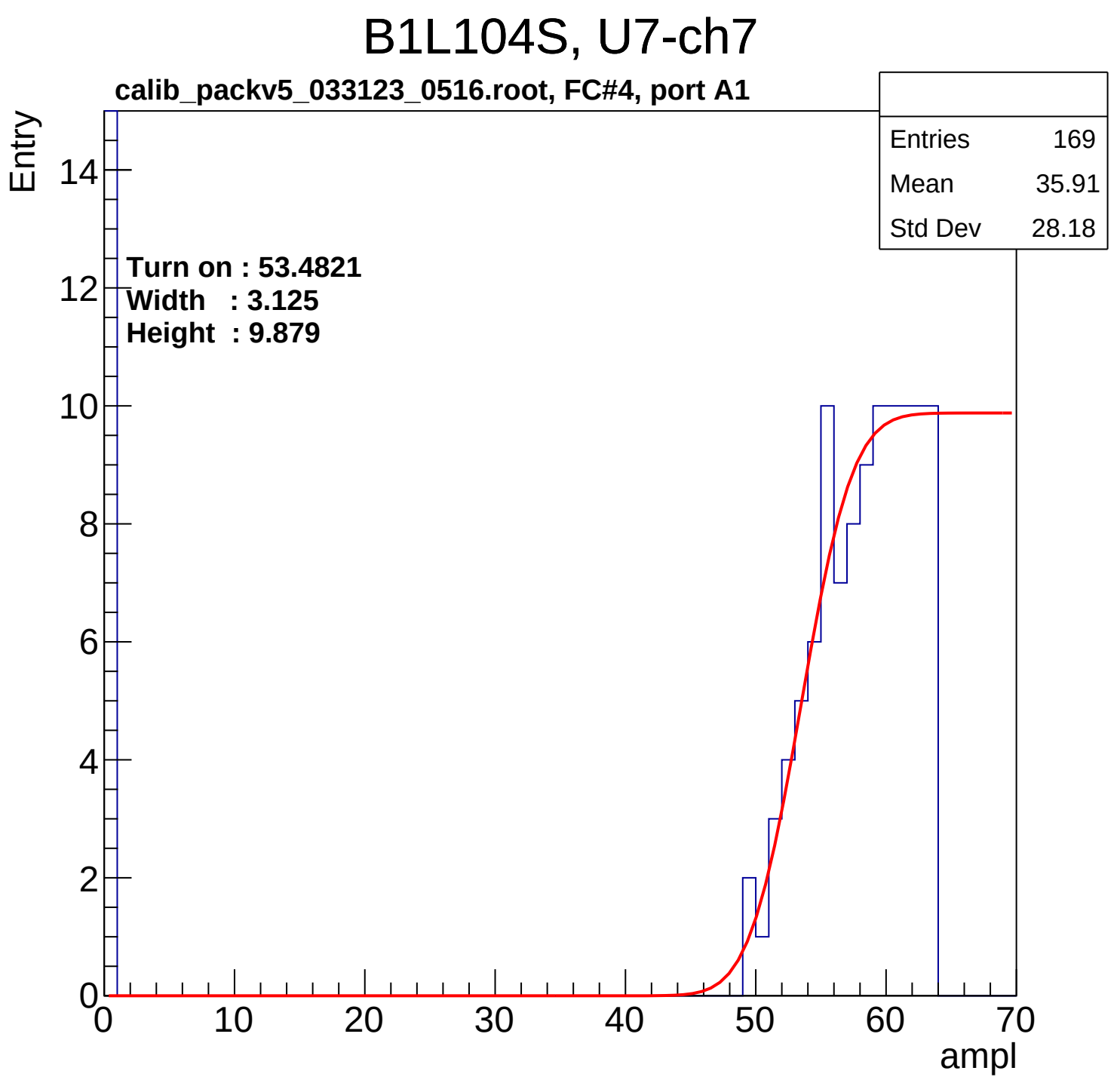

B1L104S, U7-ch2
calib_packv5_033123_0516.root, FC#4, port A1
Entries 193
Mean 34.18
Std Dev 28.07
Turn on : 54.0013
Width : 6.076
Height : 11.222
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

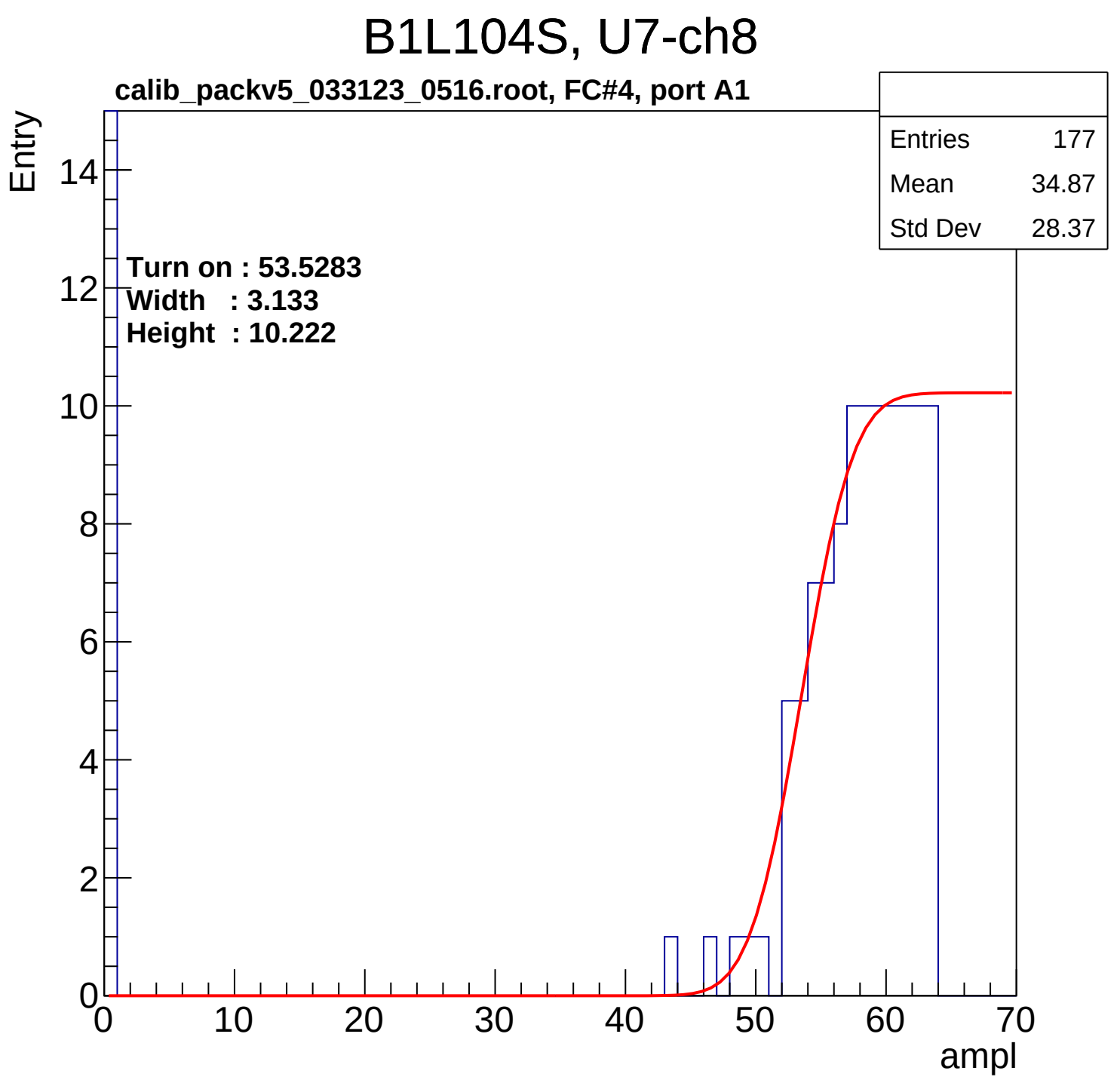

B1L104S, U7-ch3
calib_packv5_033123_0516.root, FC#4, port A1
Entries 164
Mean 29.02
Std Dev 29.46
Turn on : 55.8872
Width : 3.985
Height : 10.000
Entry
ampl
0
10
20
30
40
50
60
70
80

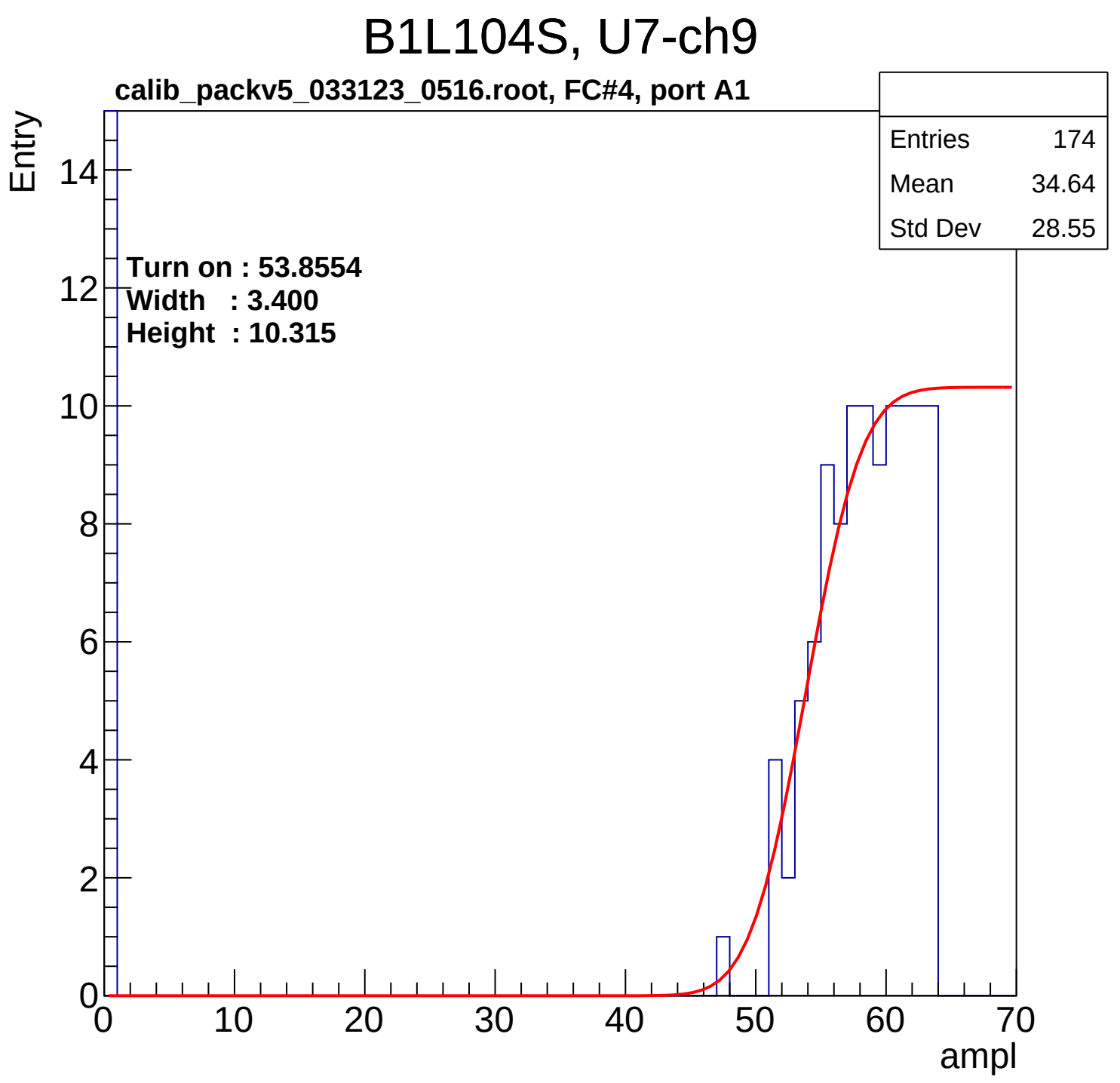

B1L104S, U7-ch4
calib_packv5_033123_0516.root, FC#4, port A1
Entries 195
Mean 34.75
Std Dev 27.98
Turn on : 52.7564
Width : 4.562
Height : 10.512
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

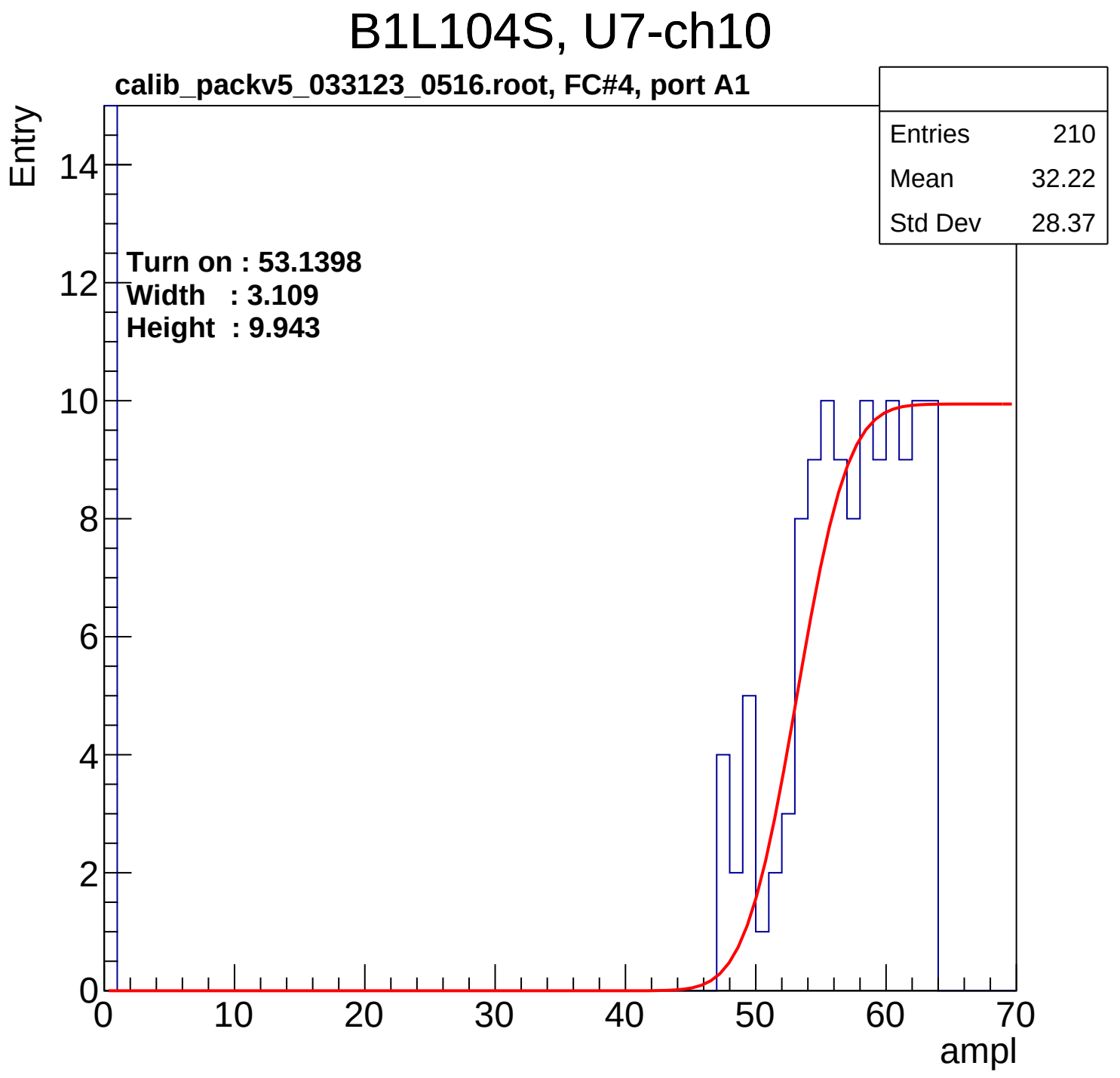

B1L104S, U7-ch5
calib_packv5_033123_0516.root, FC#4, port A1
Entries 158
Mean 34.21
Std Dev 28.74
Turn on : 54.4566
Width : 0.989
Height : 8.920
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

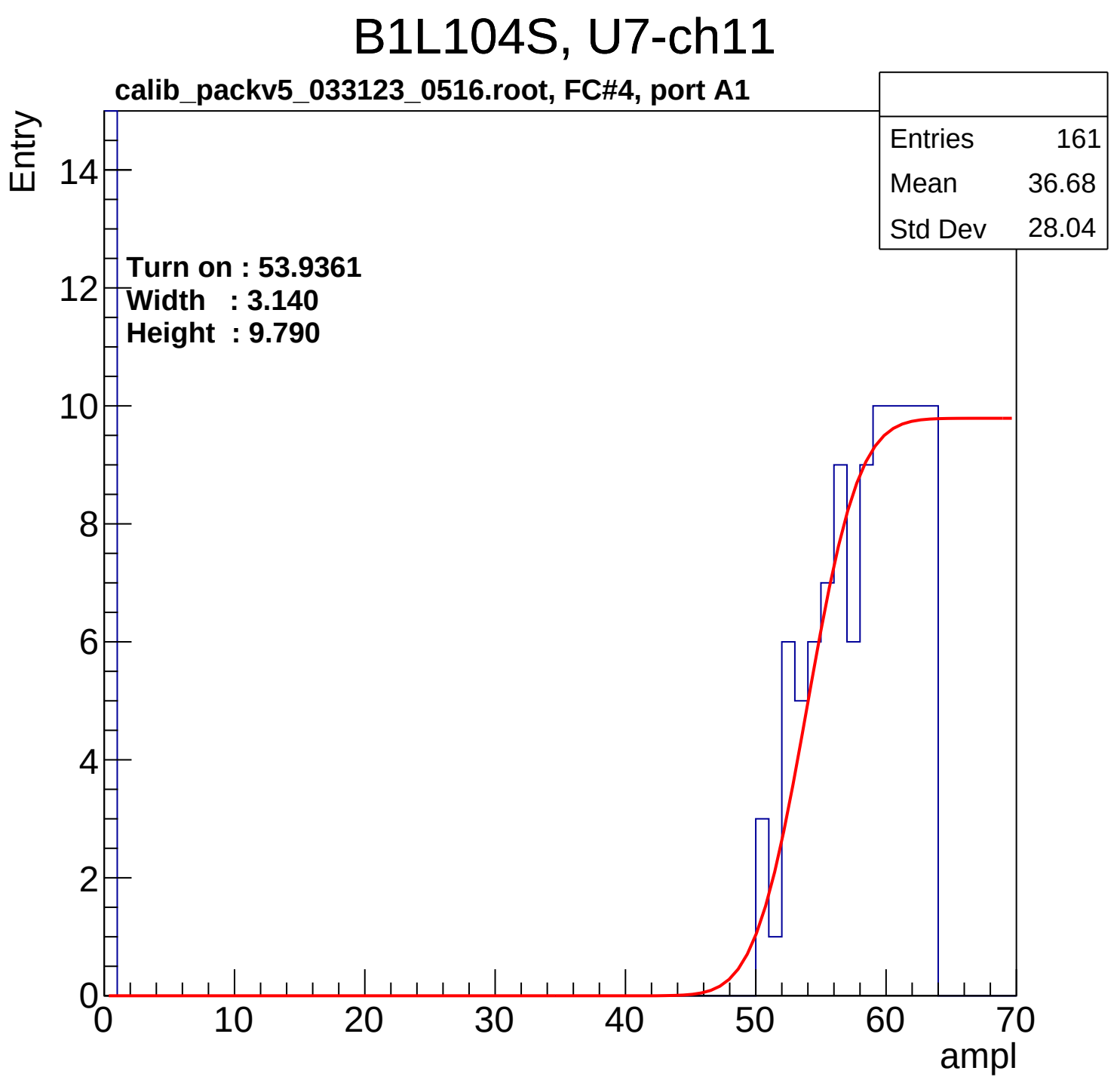

B1L104S, U7-ch6
calib_packv5_033123_0516.root, FC#4, port A1
Entries 209
Mean 34.14
Std Dev 27.93
Turn on : 52.0850
Width : 3.438
Height : 10.113
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

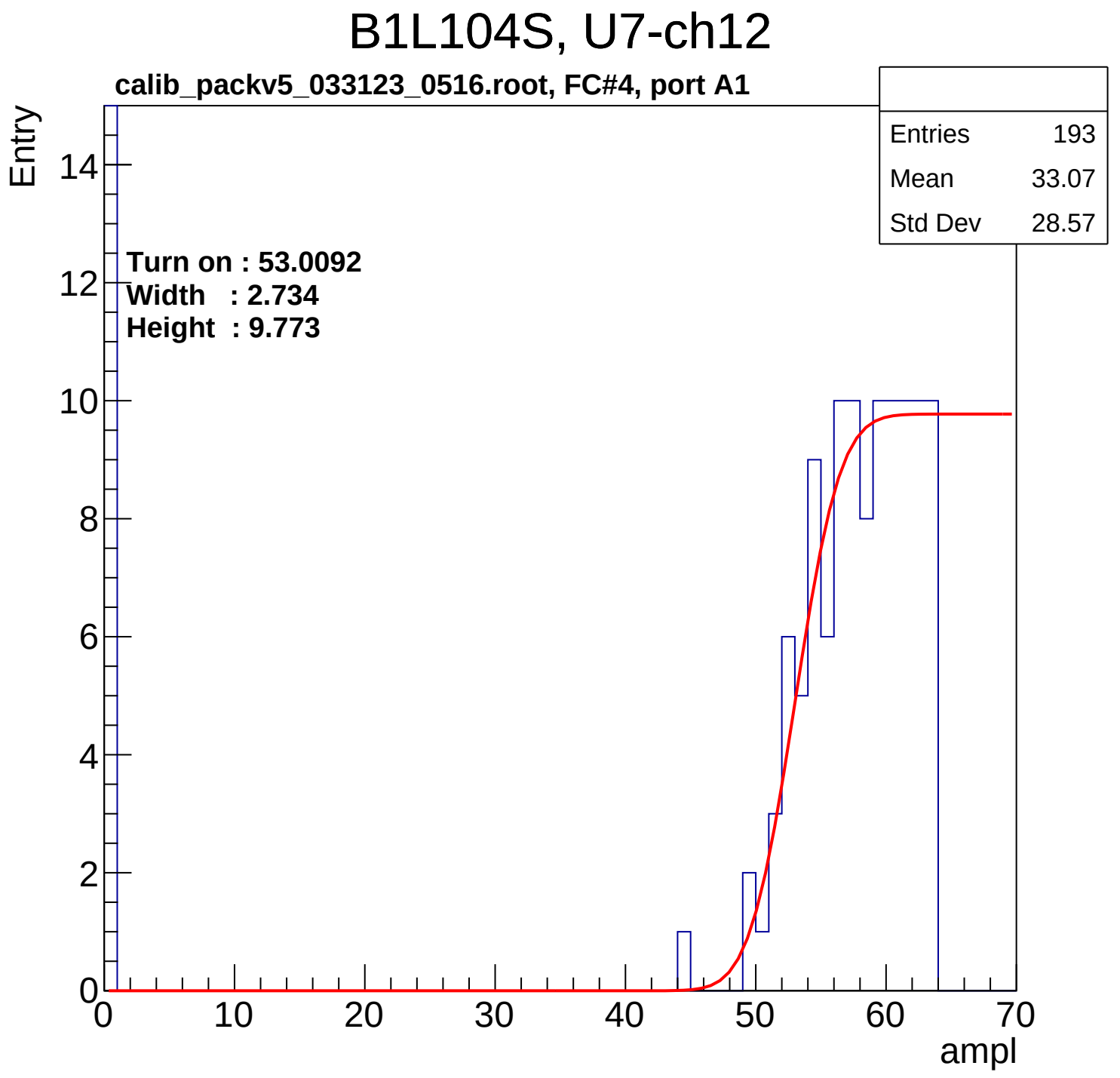

B1L104S, U7-ch7
calib_packv5_033123_0516.root, FC#4, port A1
Entries 169
Mean 35.91
Std Dev 28.18
Turn on : 53.4821
Width : 3.125
Height : 9.879
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

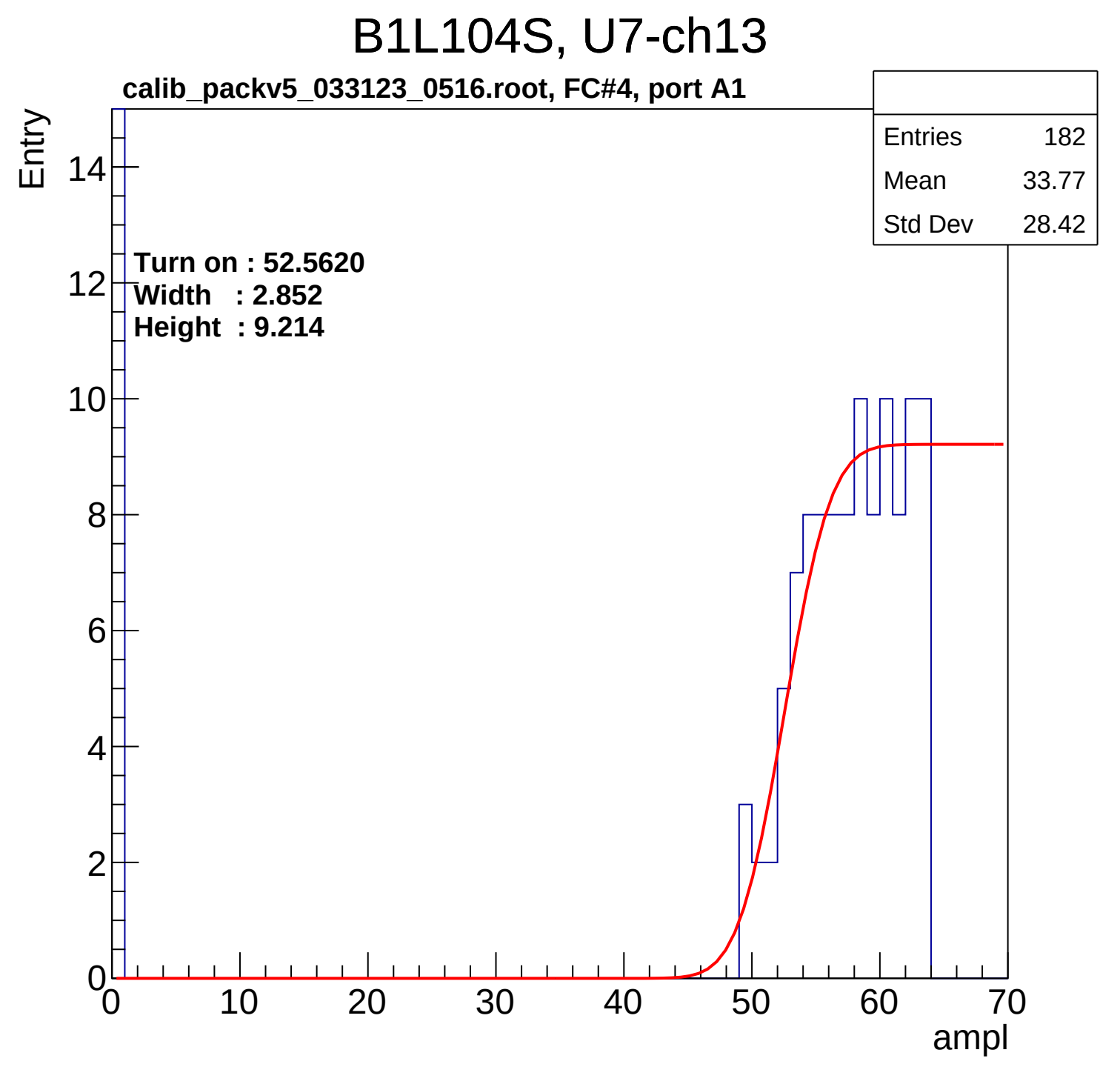

B1L104S, U7-ch8
calib_packv5_033123_0516.root, FC#4, port A1
Entries 177
Mean 34.87
Std Dev 28.37
Turn on : 53.5283
Width : 3.133
Height : 10.222
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

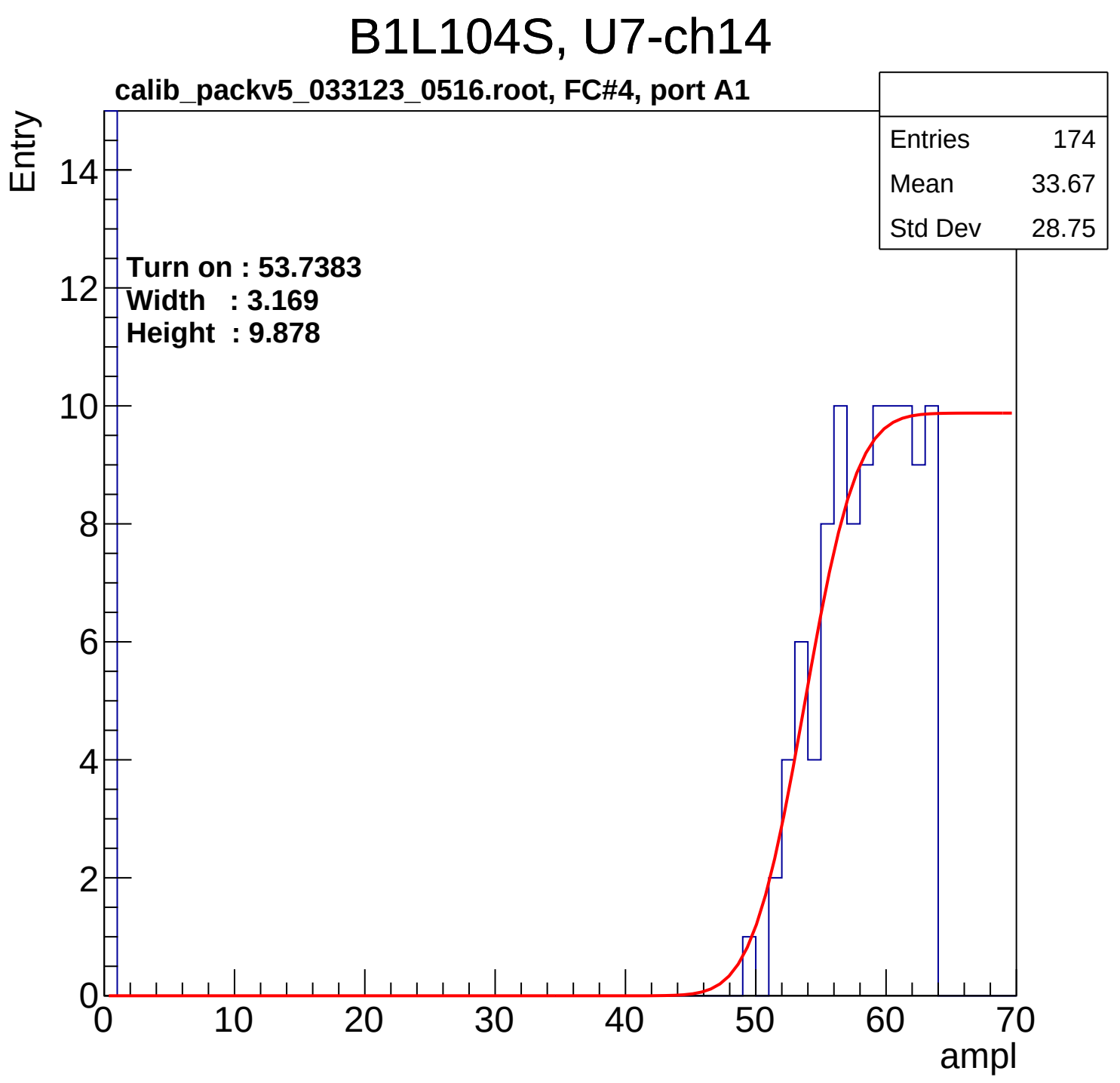

B1L104S, U7-ch9
calib_packv5_033123_0516.root, FC#4, port A1
Entries 174
Mean 34.64
Std Dev 28.55
Turn on : 53.8554
Width : 3.400
Height : 10.315
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

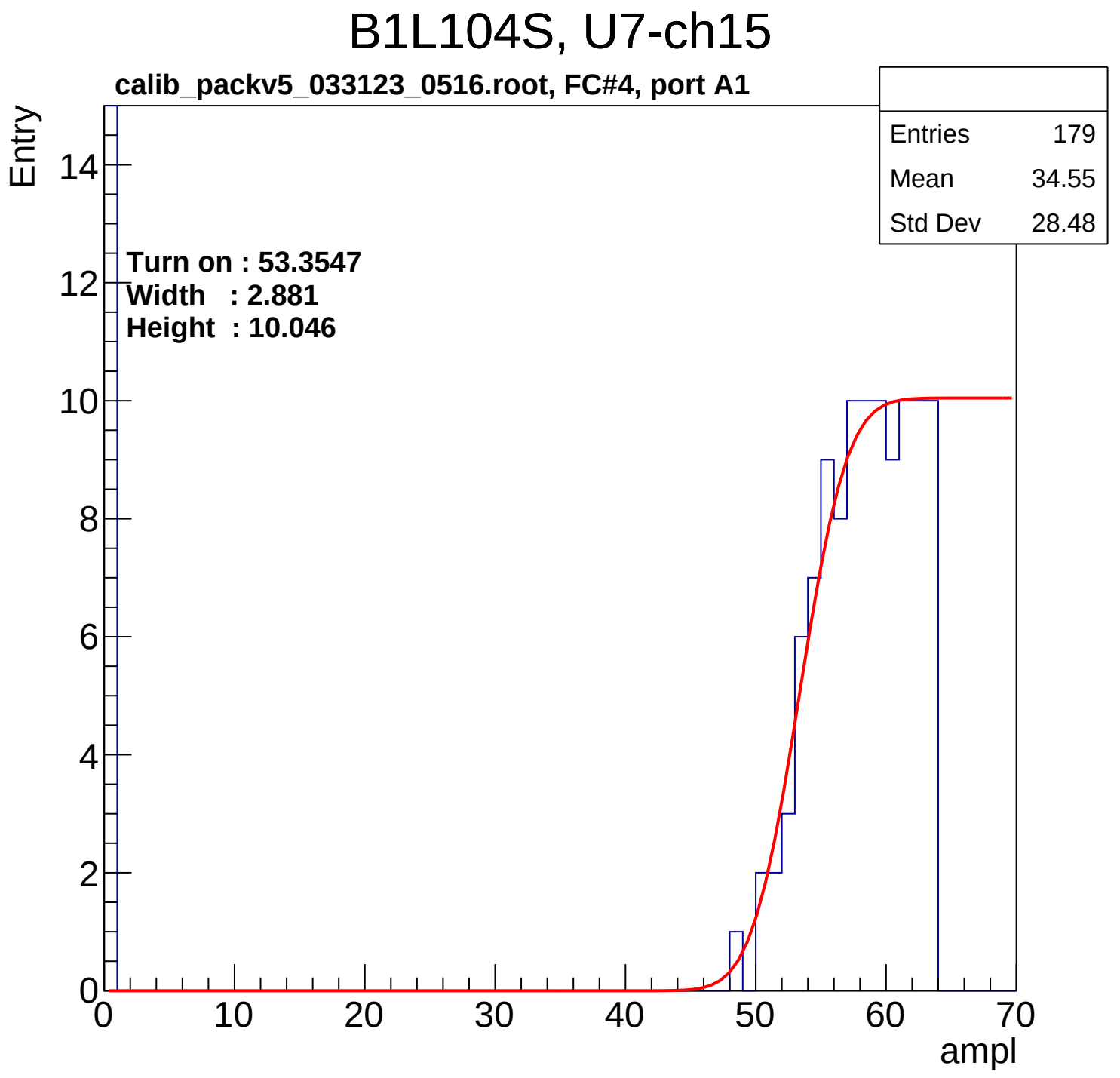

B1L104S, U7-ch10
calib_packv5_033123_0516.root, FC#4, port A1
Entries 210
Mean 32.22
Std Dev 28.37
Turn on : 53.1398
Width : 3.109
Height : 9.943
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

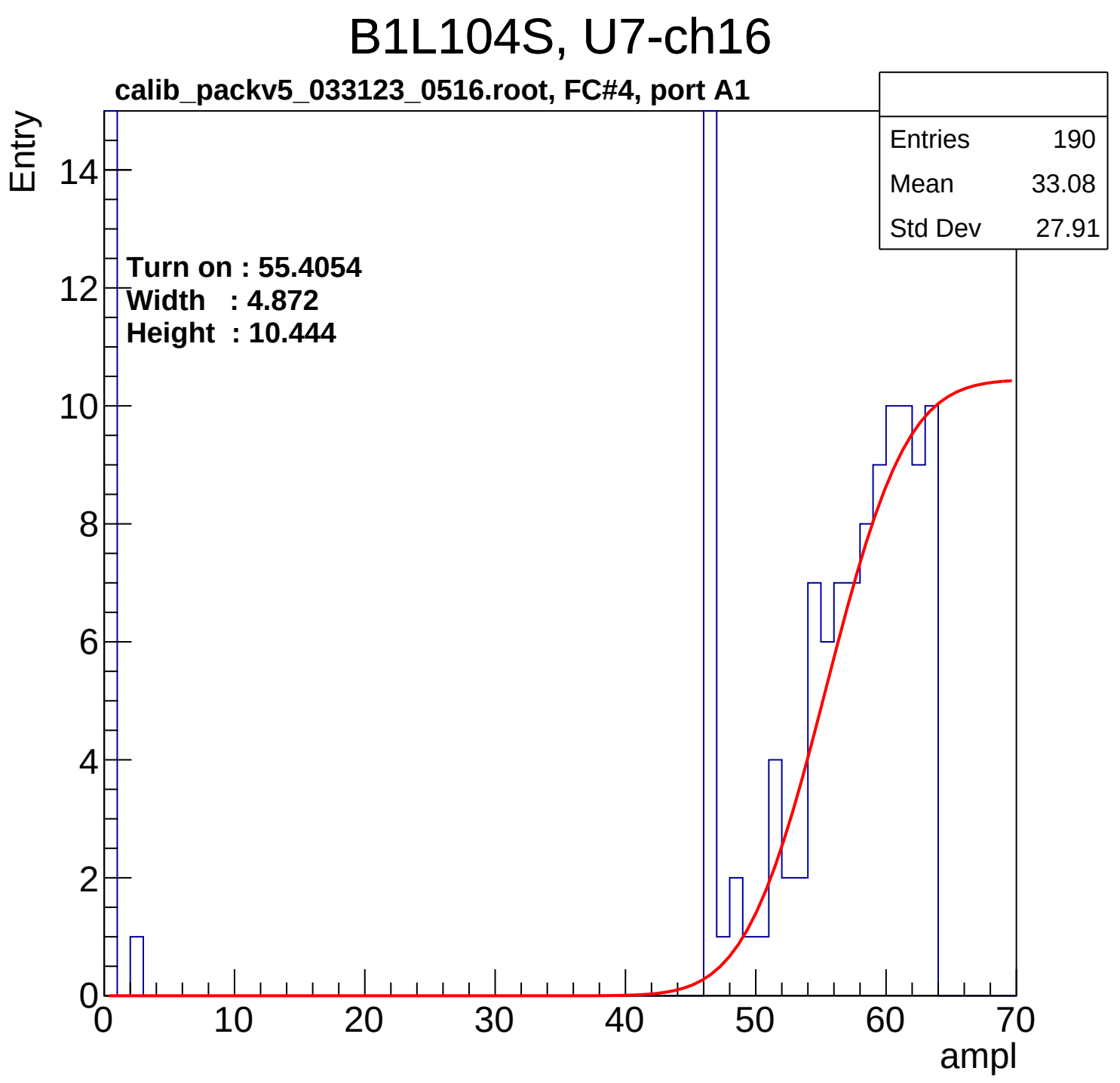

B1L104S, U7-ch11
calib_packv5_033123_0516.root, FC#4, port A1
Entries 161
Mean 36.68
Std Dev 28.04
Turn on : 53.9361
Width : 3.140
Height : 9.790
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

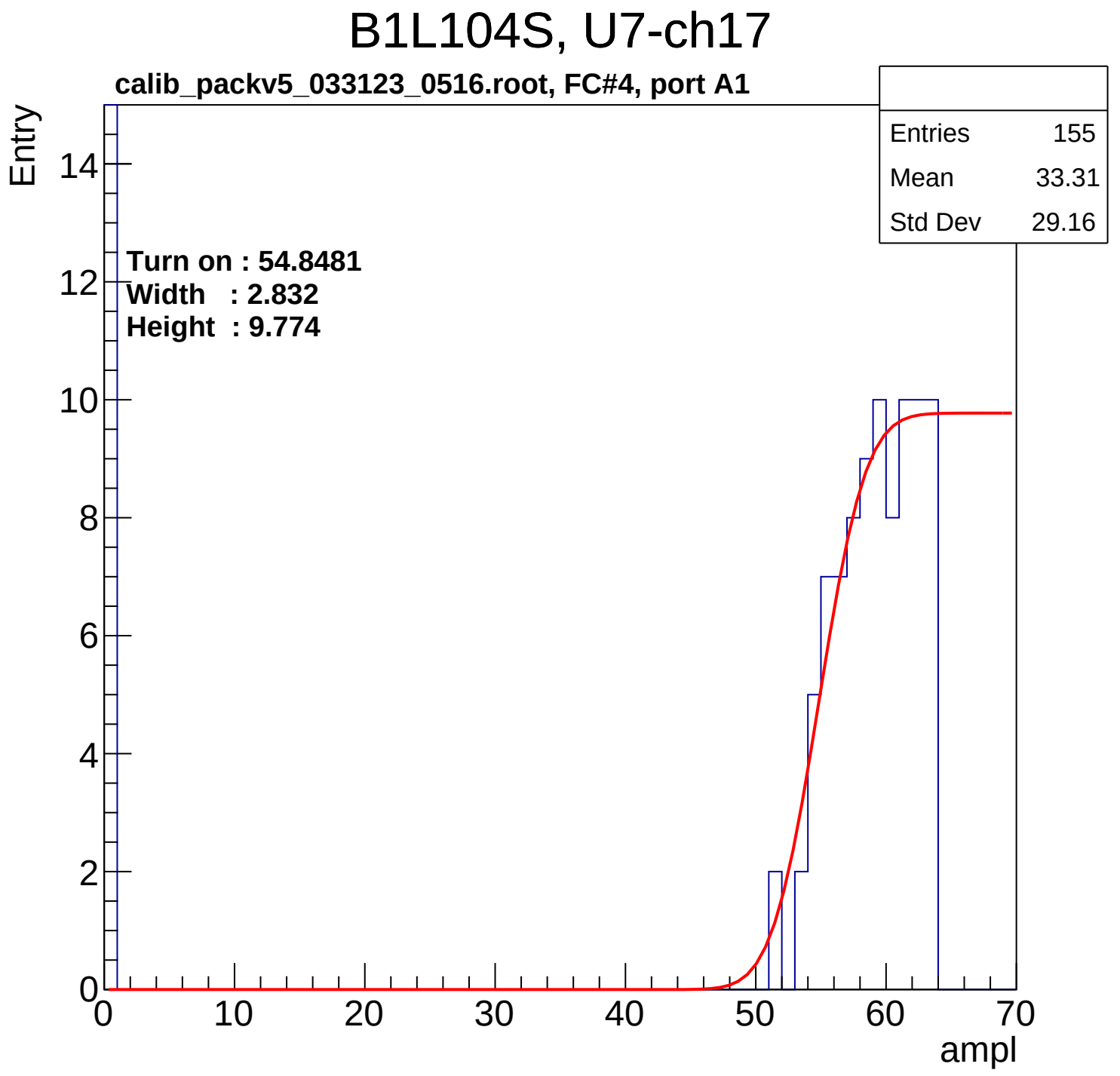

B1L104S, U7-ch12
calib_packv5_033123_0516.root, FC#4, port A1
Entries 193
Mean 33.07
Std Dev 28.57
Turn on : 53.0092
Width : 2.734
Height : 9.773
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

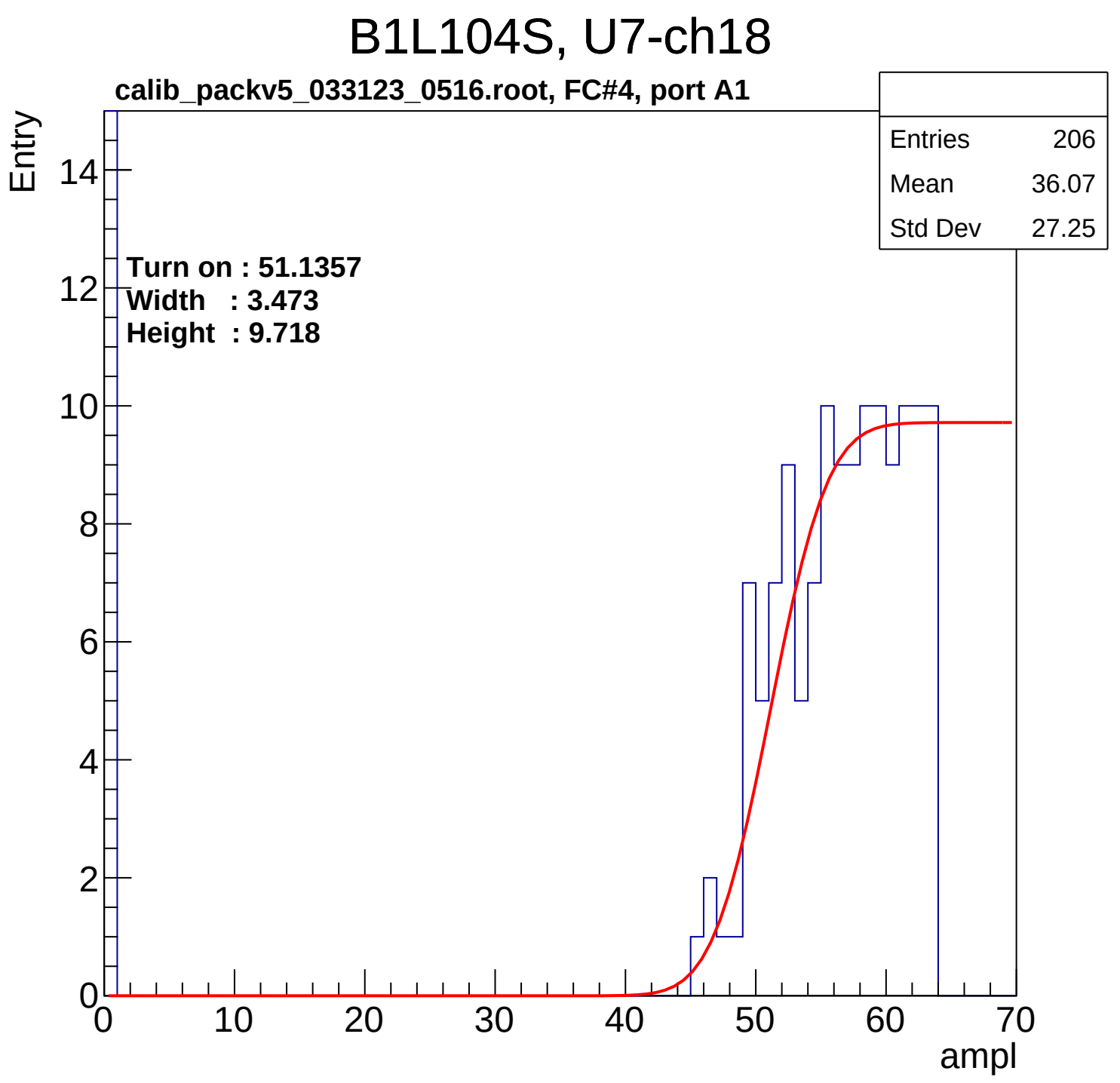

B1L104S, U7-ch13
calib_packv5_033123_0516.root, FC#4, port A1
Entries 182
Mean 33.77
Std Dev 28.42
Turn on : 52.5620
Width : 2.852
Height : 9.214
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

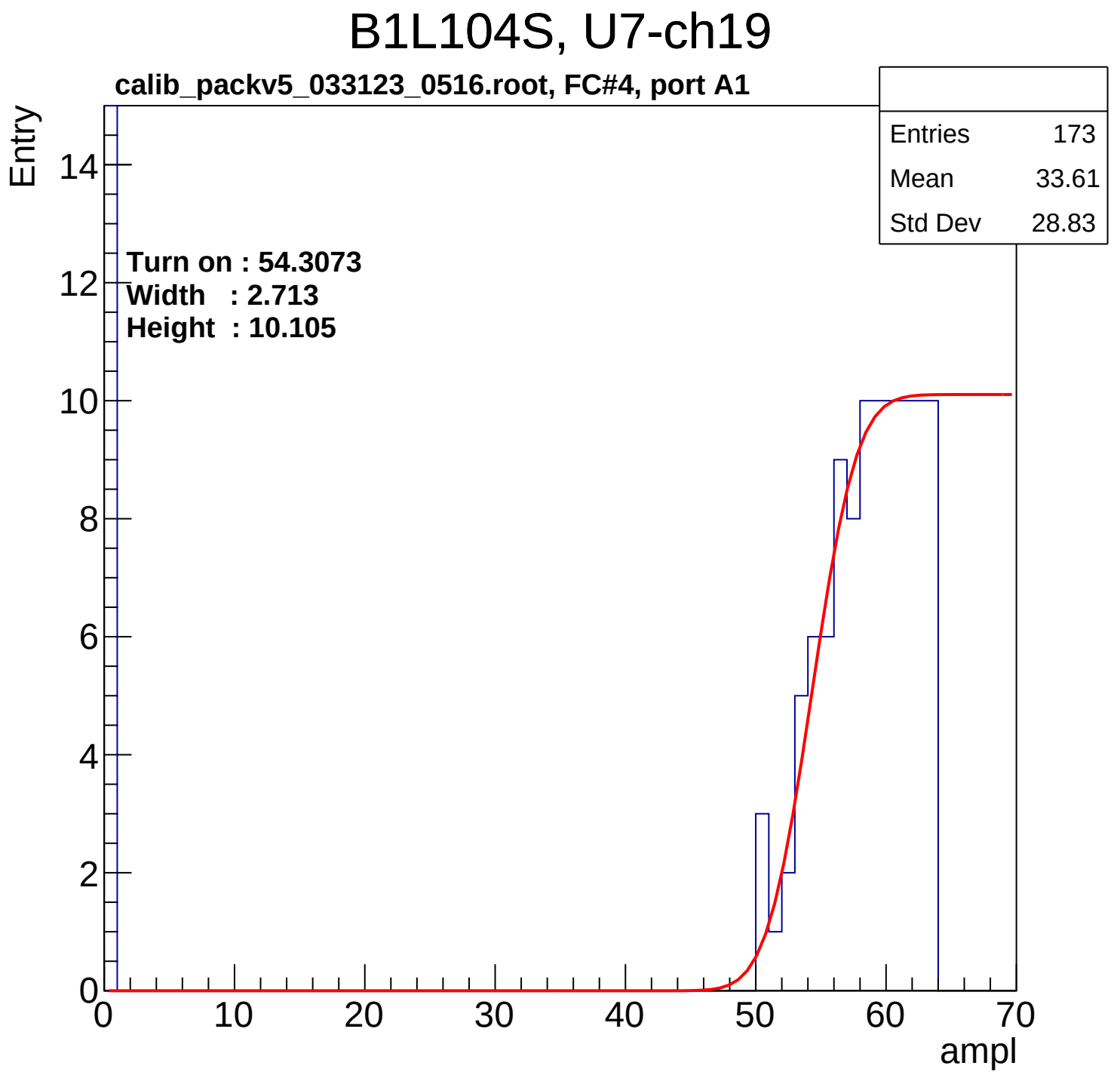

B1L104S, U7-ch14
calib_packv5_033123_0516.root, FC#4, port A1
Entries 174
Mean 33.67
Std Dev 28.75
Turn on : 53.7383
Width : 3.169
Height : 9.878
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

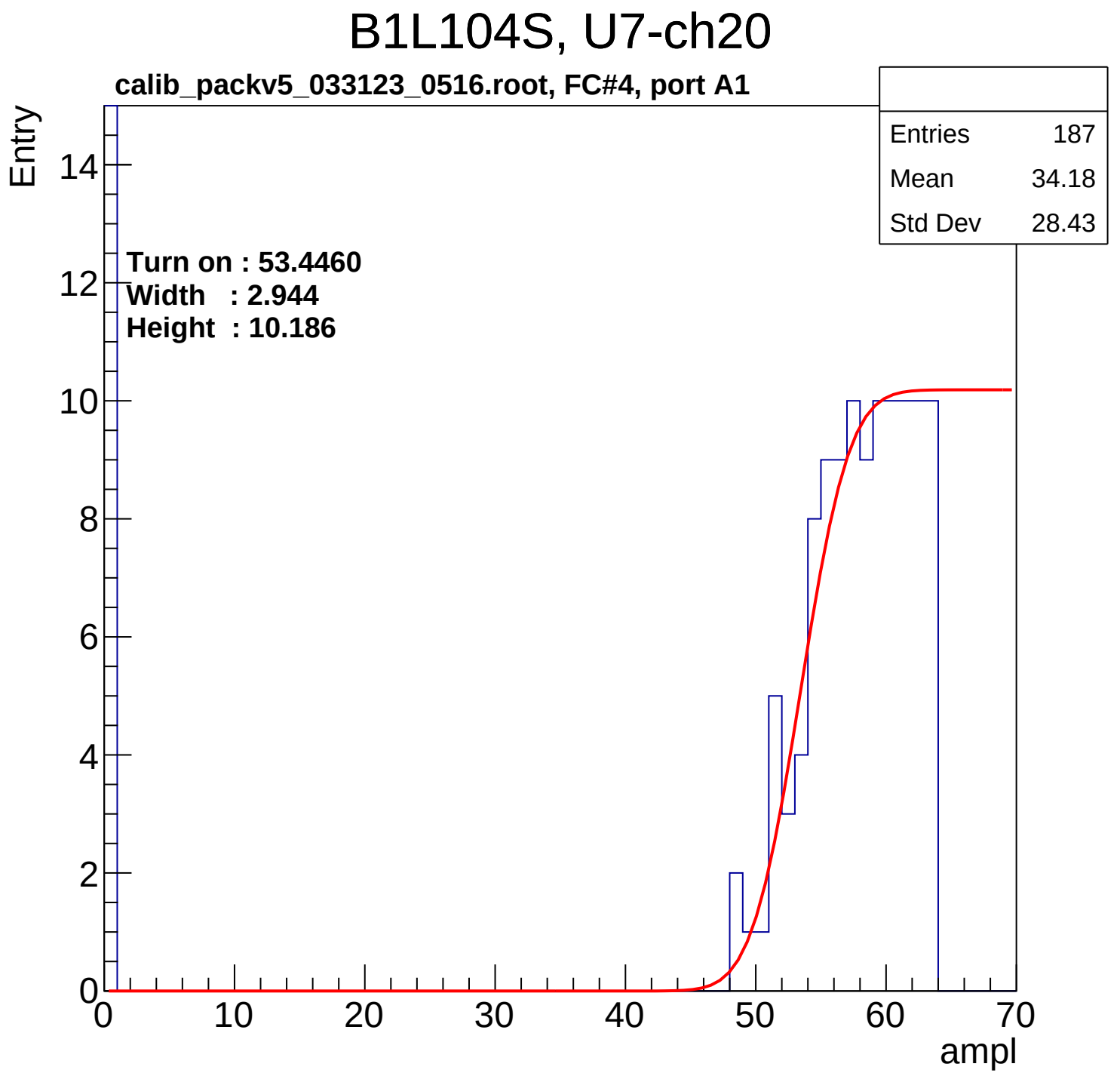

B1L104S, U7-ch15
calib_packv5_033123_0516.root, FC#4, port A1
Entries 179
Mean 34.55
Std Dev 28.48
Turn on : 53.3547
Width : 2.881
Height : 10.046
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

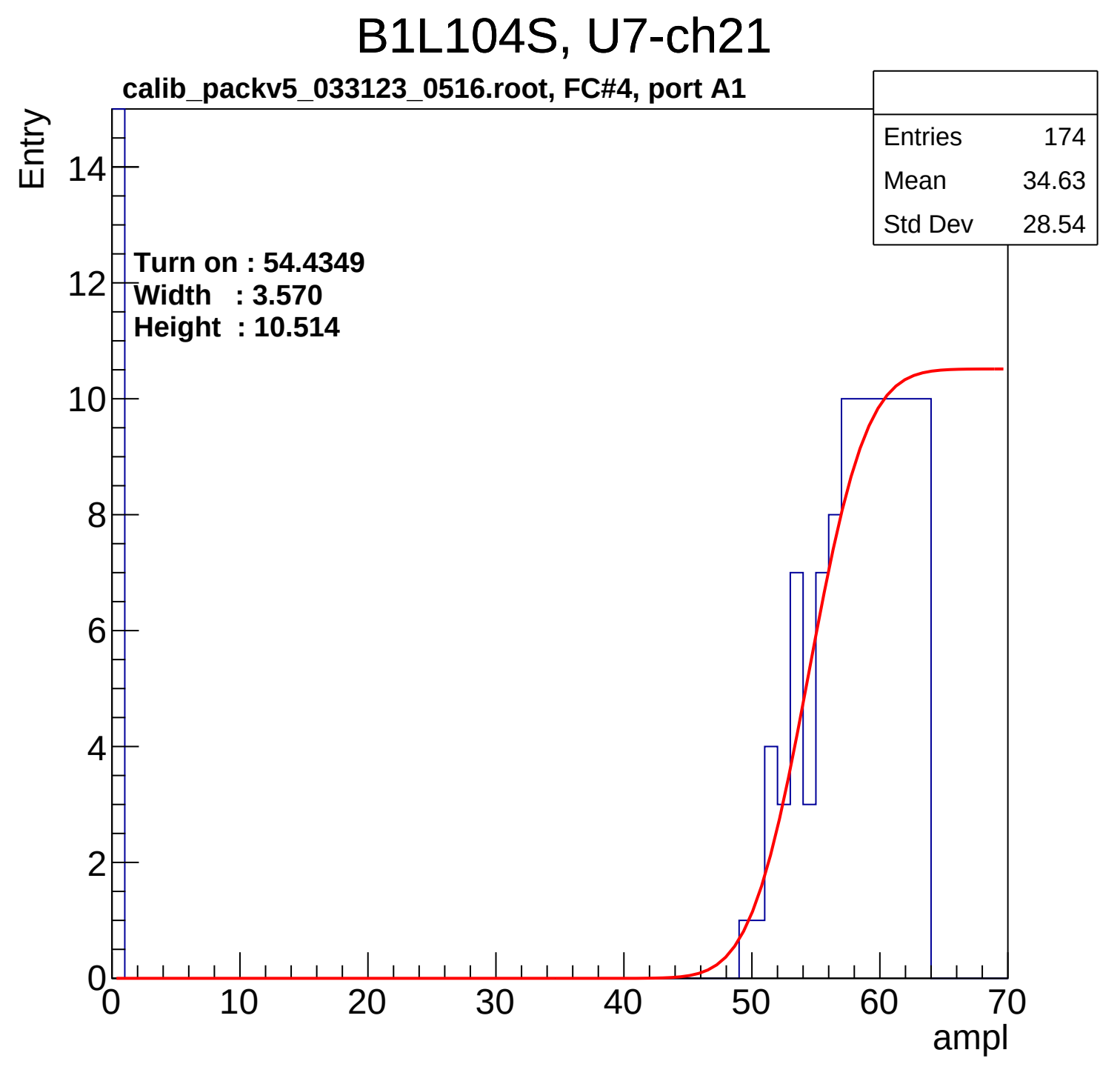

B1L104S, U7-ch16
calib_packv5_033123_0516.root, FC#4, port A1
Entries 190
Mean 33.08
Std Dev 27.91
Turn on : 55.4054
Width : 4.872
Height : 10.444
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

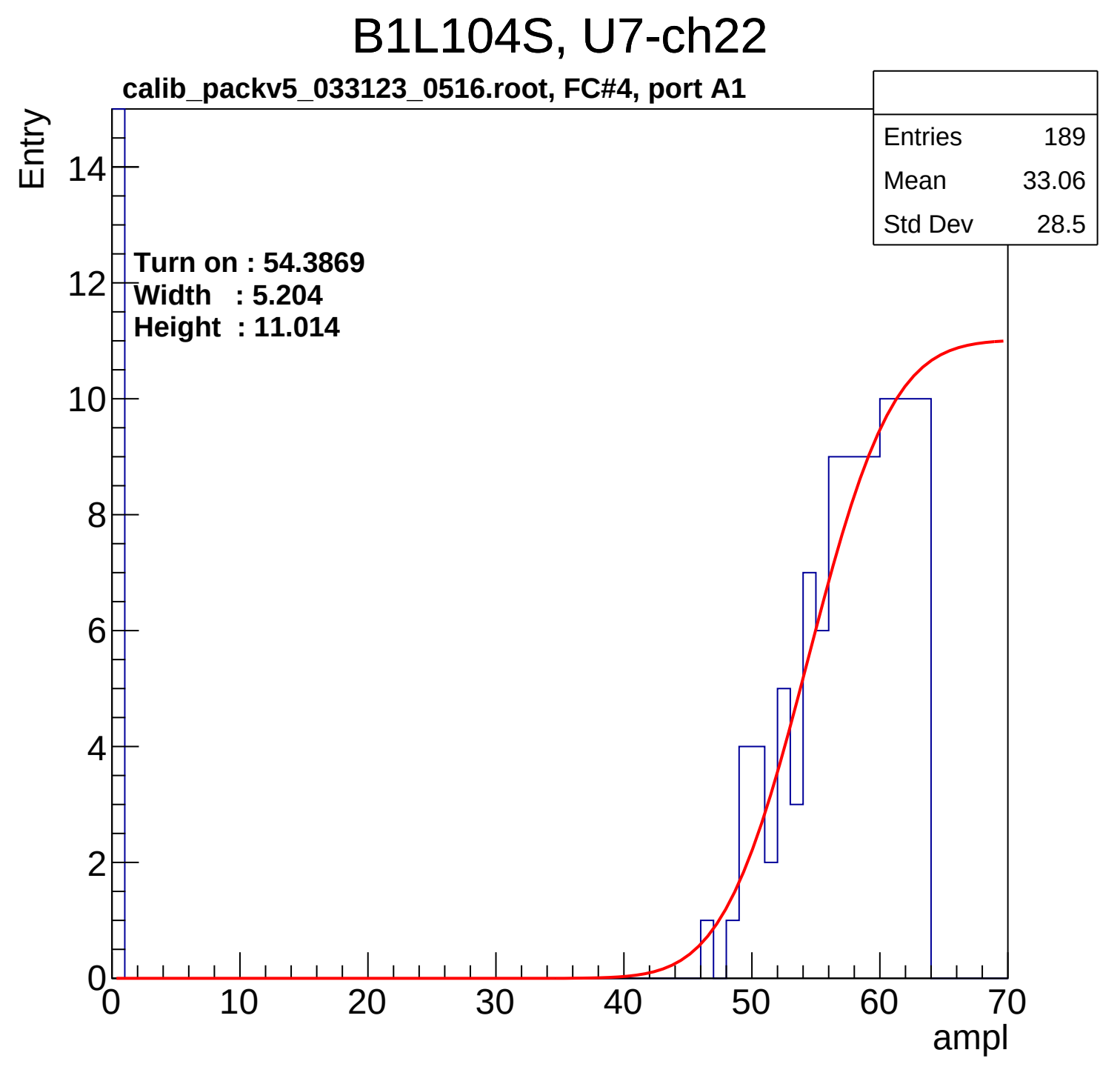

B1L104S, U7-ch17
calib_packv5_033123_0516.root, FC#4, port A1
Entries 155
Mean 33.31
Std Dev 29.16
Turn on : 54.8481
Width : 2.832
Height : 9.774
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

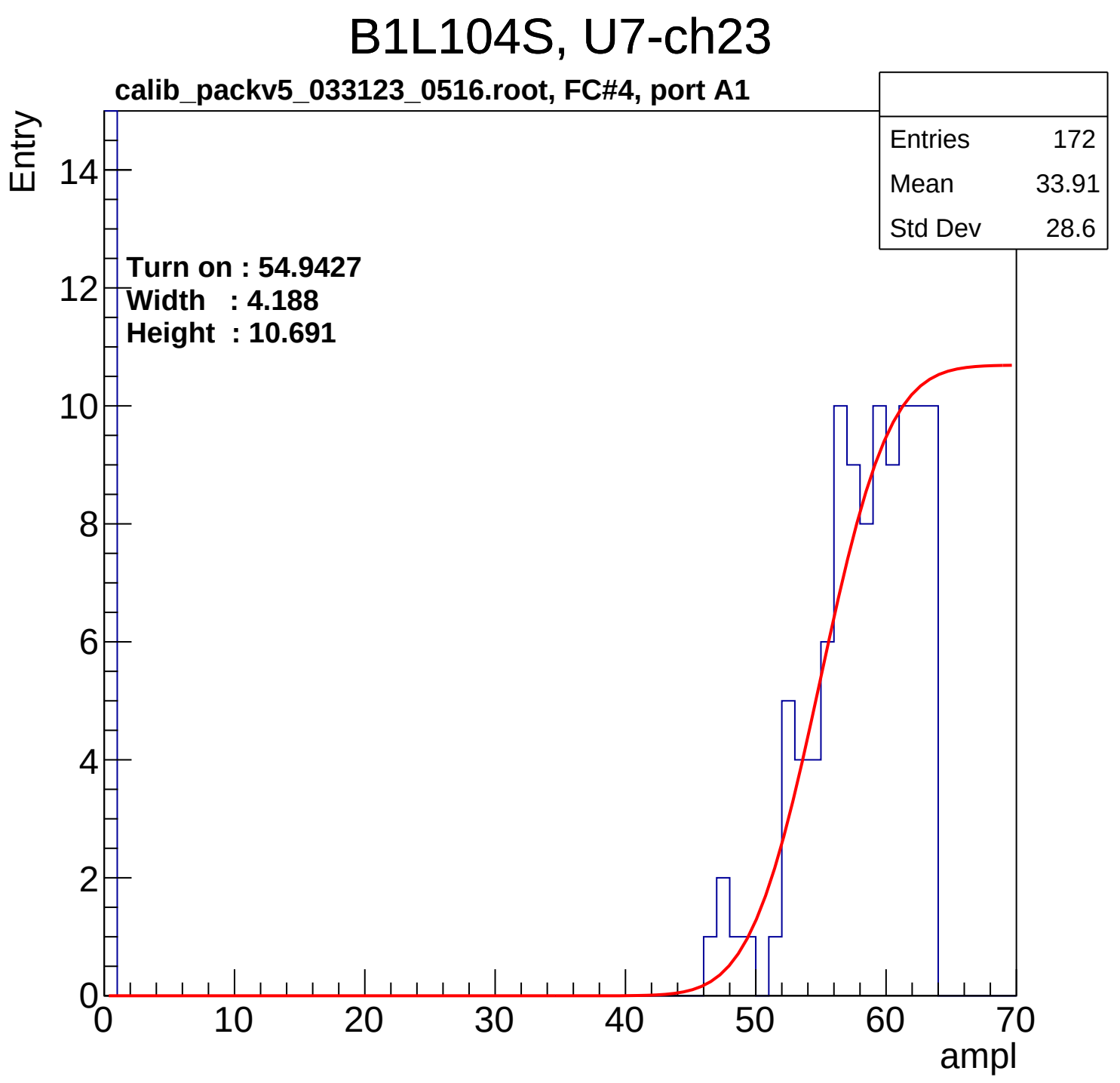

B1L104S, U7-ch18
calib_packv5_033123_0516.root, FC#4, port A1
Entries 206
Mean 36.07
Std Dev 27.25
Turn on : 51.1357
Width : 3.473
Height : 9.718
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

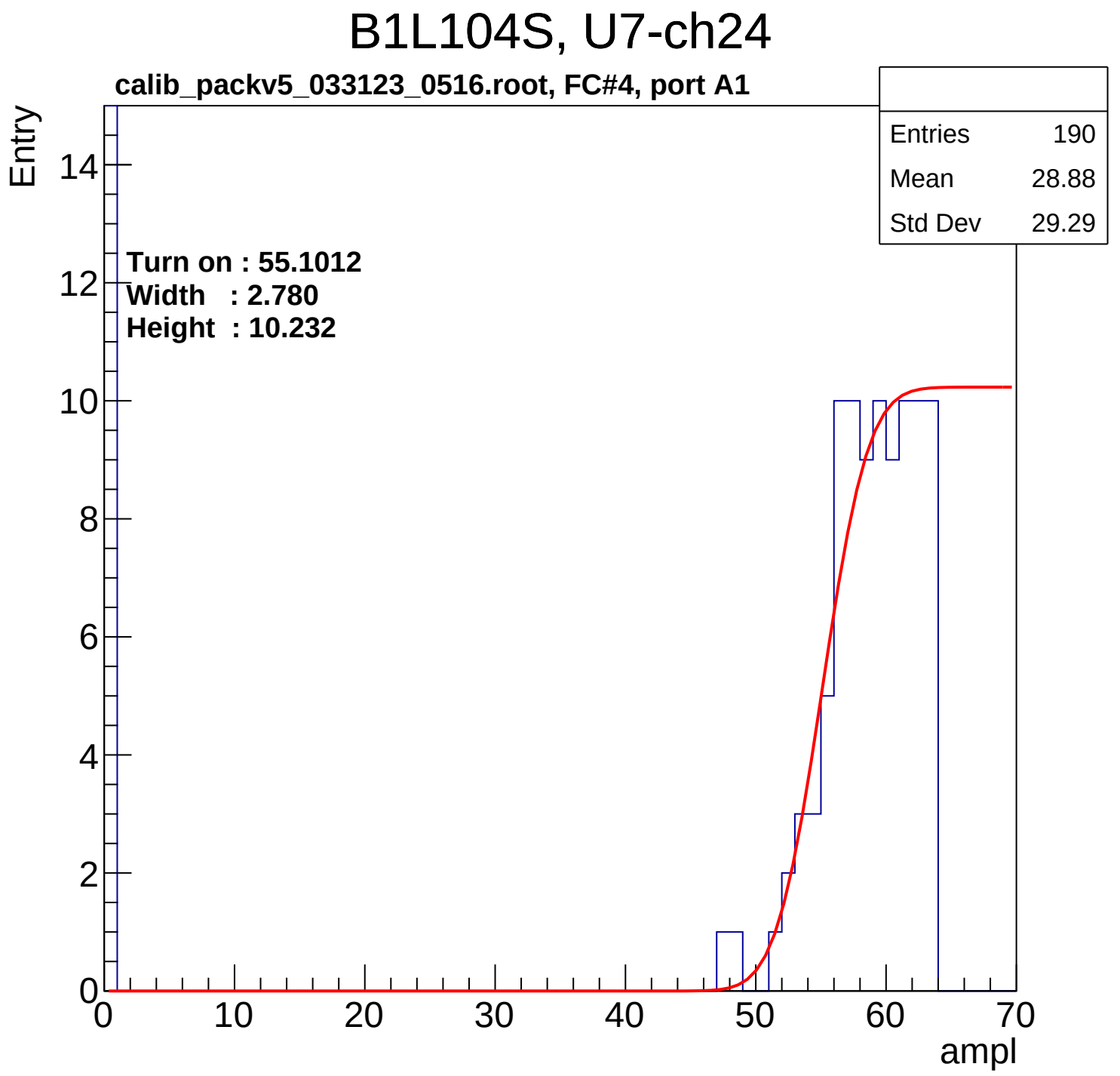

B1L104S, U7-ch19
calib_packv5_033123_0516.root, FC#4, port A1
Entries 173
Mean 33.61
Std Dev 28.83
Turn on : 54.3073
Width : 2.713
Height : 10.105
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

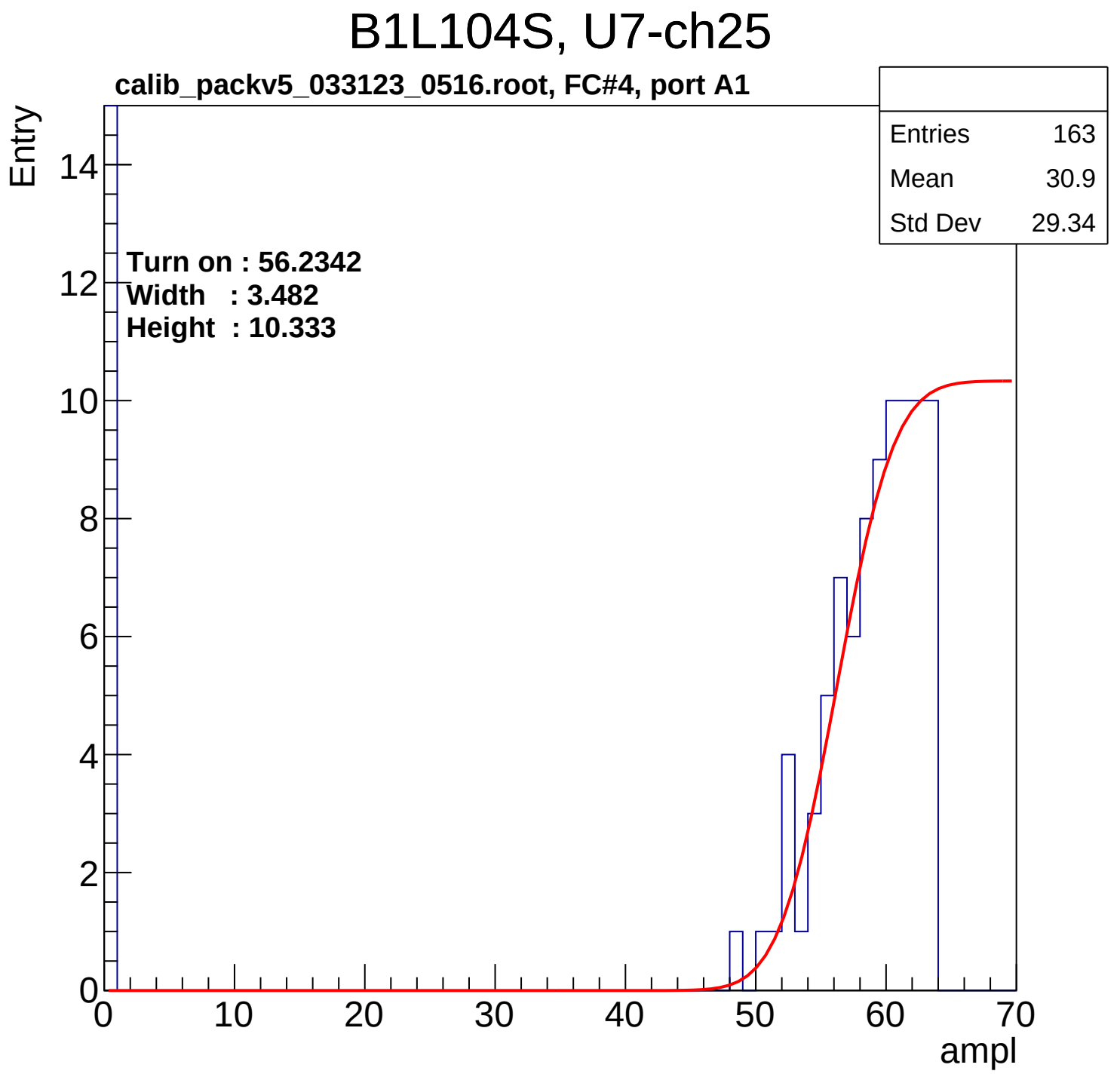

B1L104S, U7-ch20
calib_packv5_033123_0516.root, FC#4, port A1
Entries 187
Mean 34.18
Std Dev 28.43
Turn on : 53.4460
Width : 2.944
Height : 10.186
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

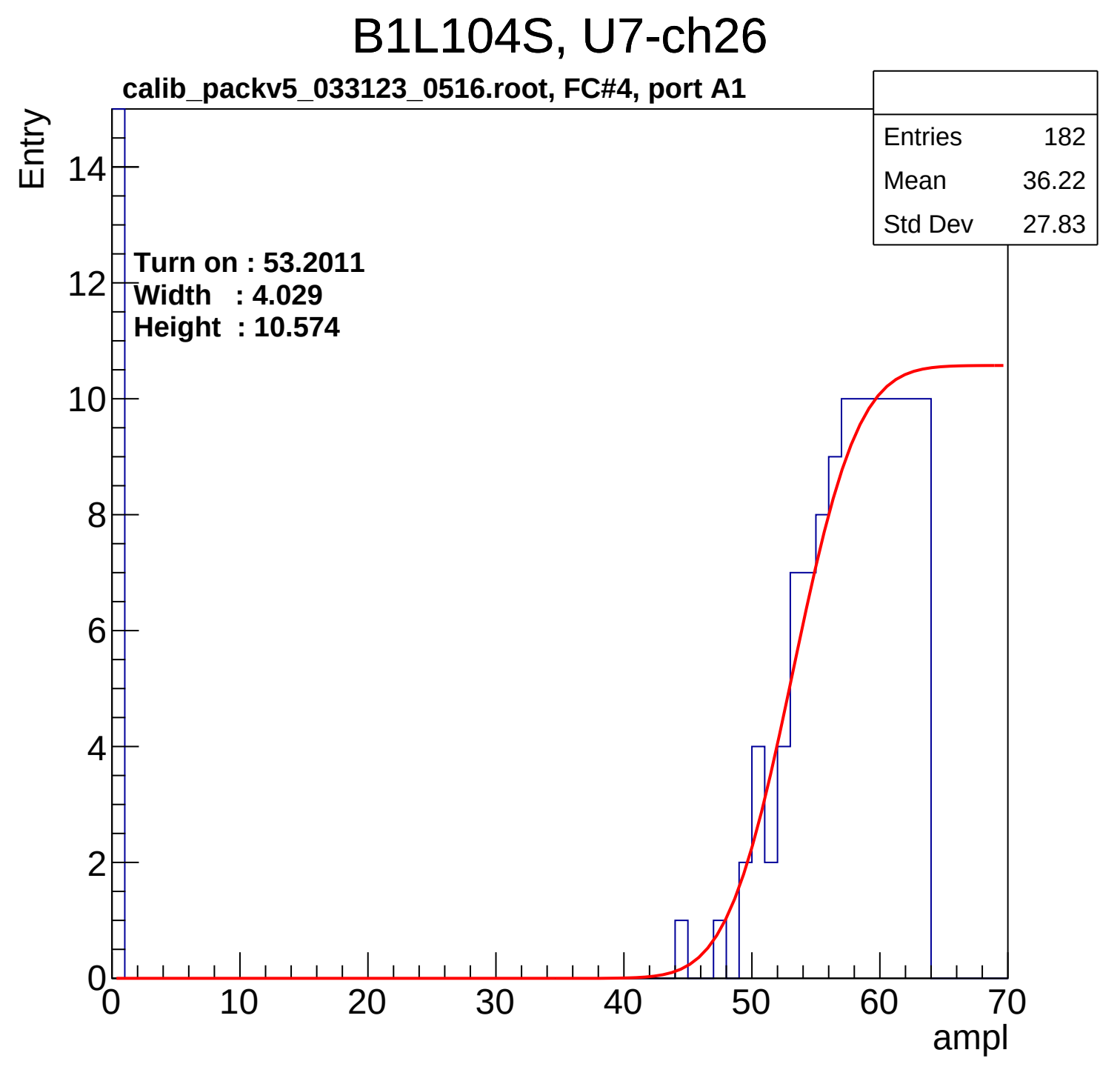

B1L104S, U7-ch21
calib_packv5_033123_0516.root, FC#4, port A1
Entries 174
Mean 34.63
Std Dev 28.54
Turn on : 54.4349
Width : 3.570
Height : 10.514
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

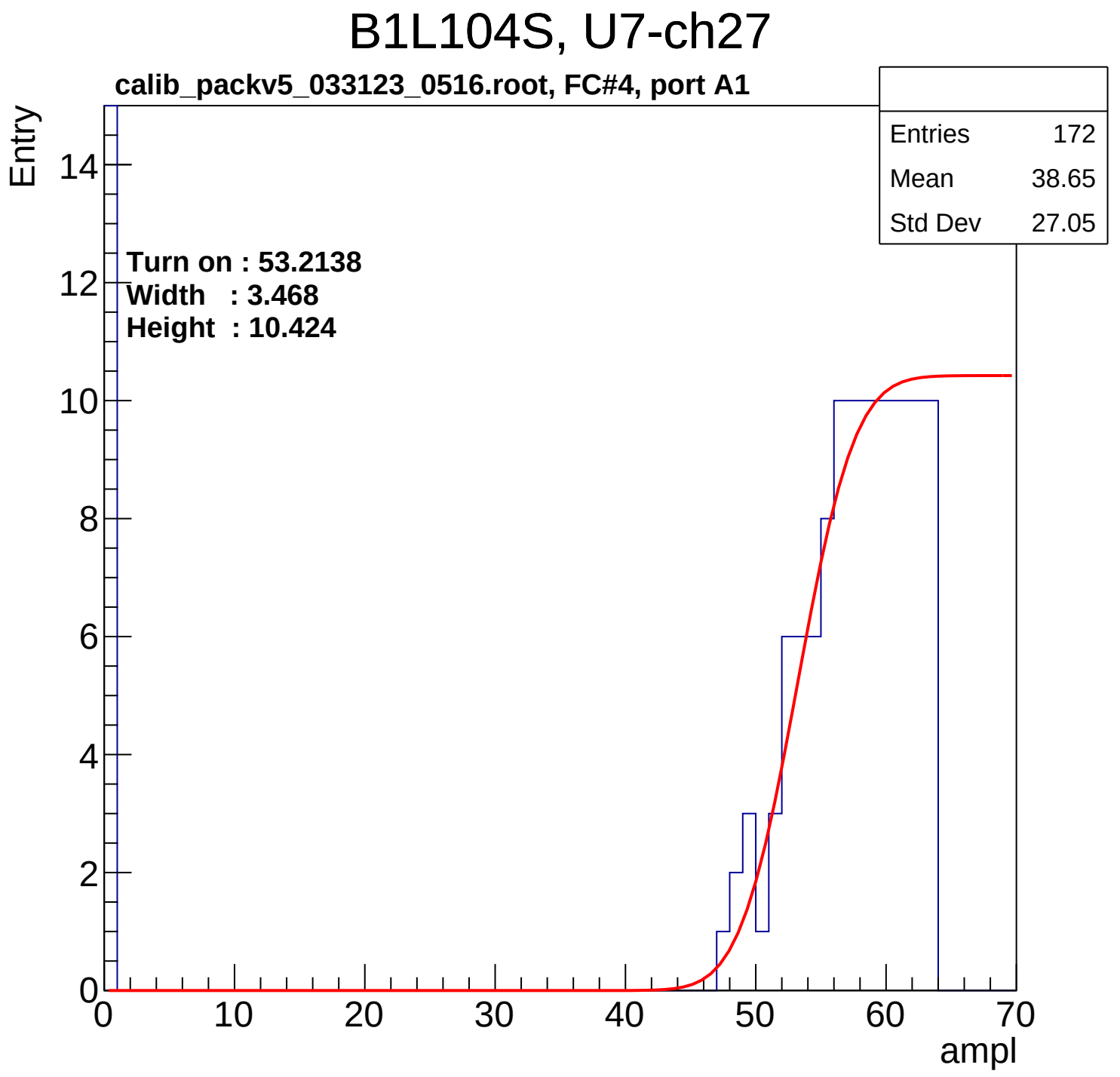

B1L104S, U7-ch22
calib_packv5_033123_0516.root, FC#4, port A1
Entries 189
Mean 33.06
Std Dev 28.5
Turn on : 54.3869
Width : 5.204
Height : 11.014
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

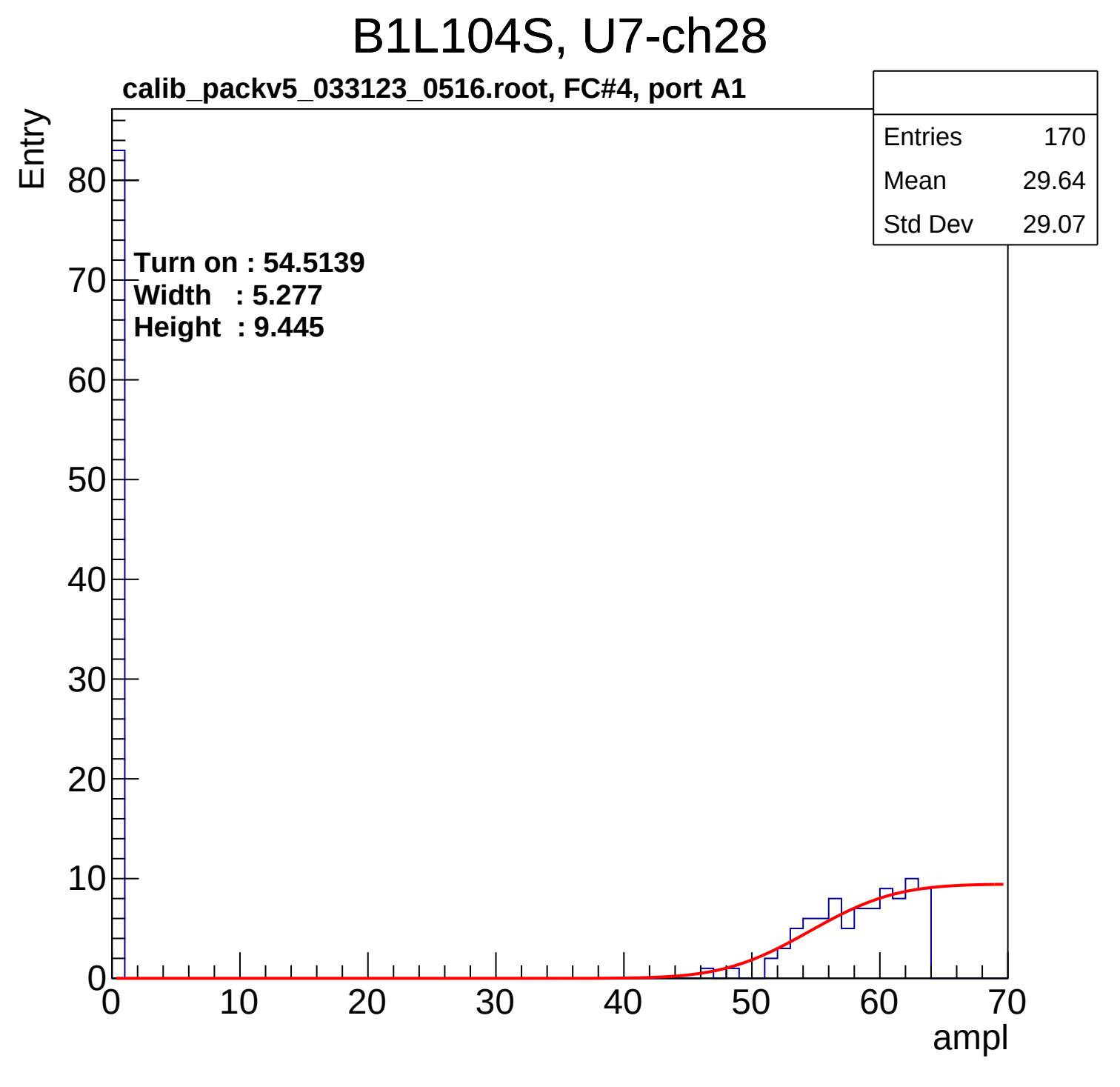

B1L104S, U7-ch23
calib_packv5_033123_0516.root, FC#4, port A1
Entries 172
Mean 33.91
Std Dev 28.6
Turn on : 54.9427
Width : 4.188
Height : 10.691
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

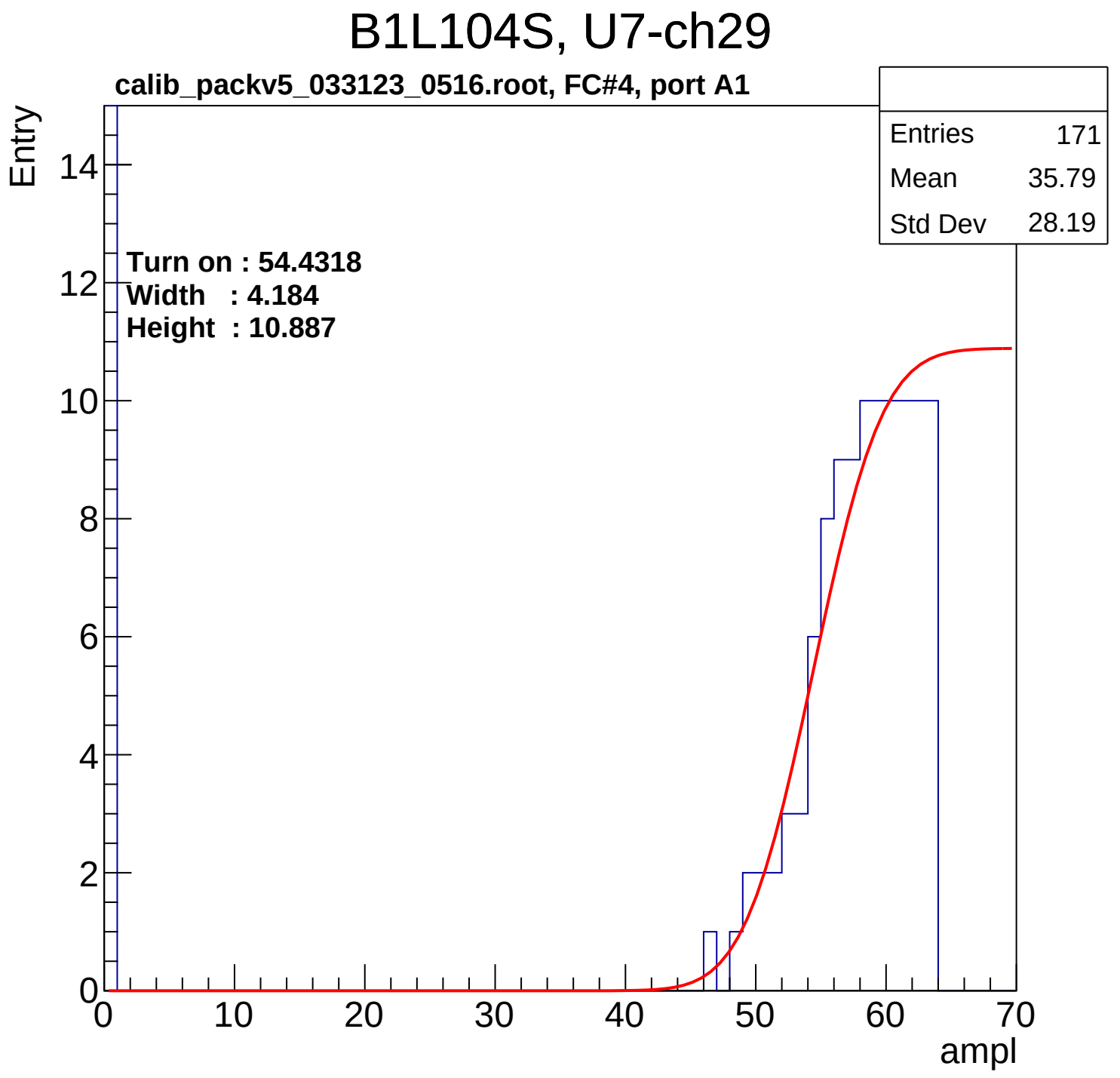

B1L104S, U7-ch24
calib_packv5_033123_0516.root, FC#4, port A1
Entries 190
Mean 28.88
Std Dev 29.29
Turn on : 55.1012
Width : 2.780
Height : 10.232
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

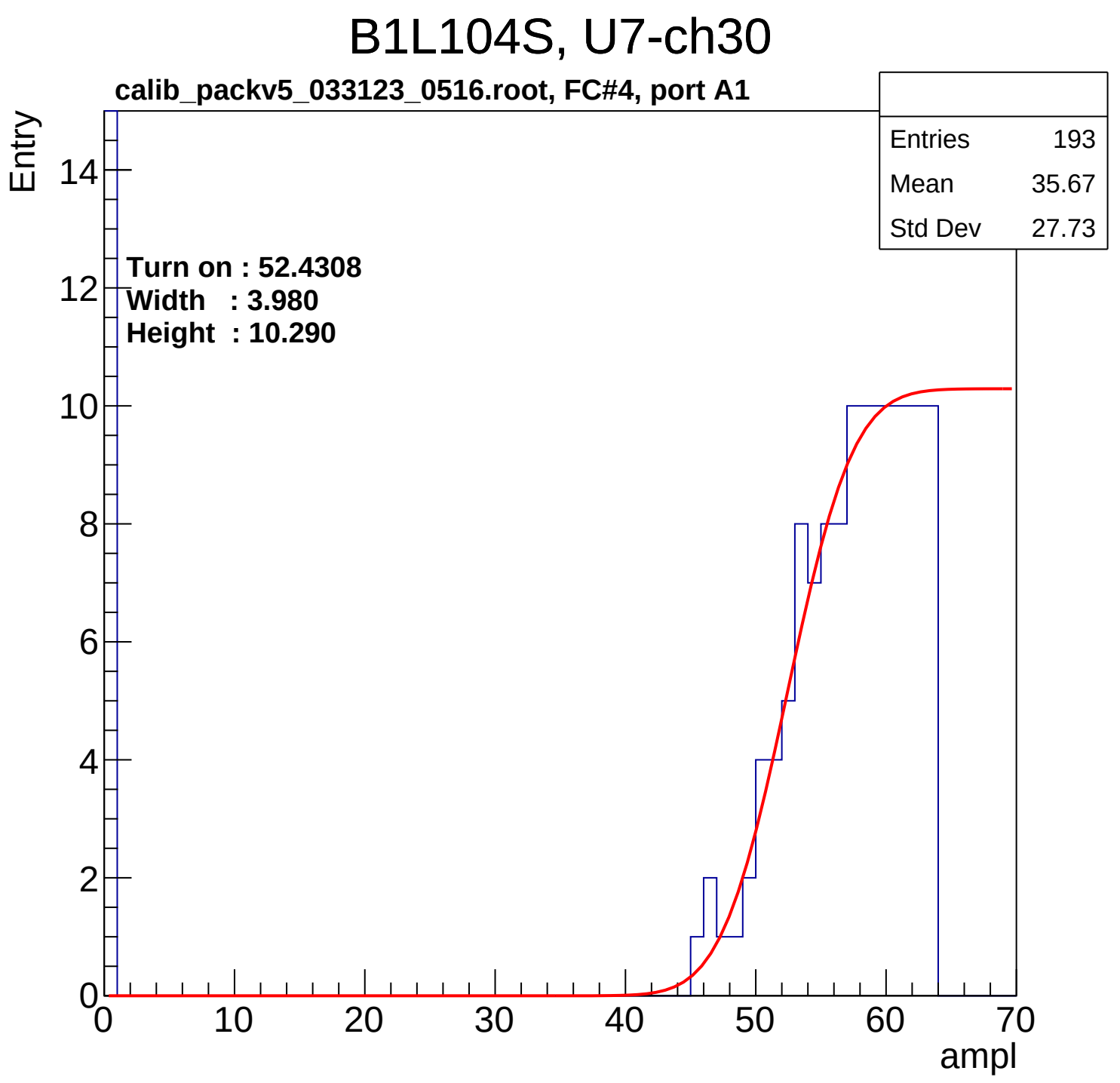

B1L104S, U7-ch25
calib_packv5_033123_0516.root, FC#4, port A1
Entries 163
Mean 30.9
Std Dev 29.34
Turn on : 56.2342
Width : 3.482
Height : 10.333
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

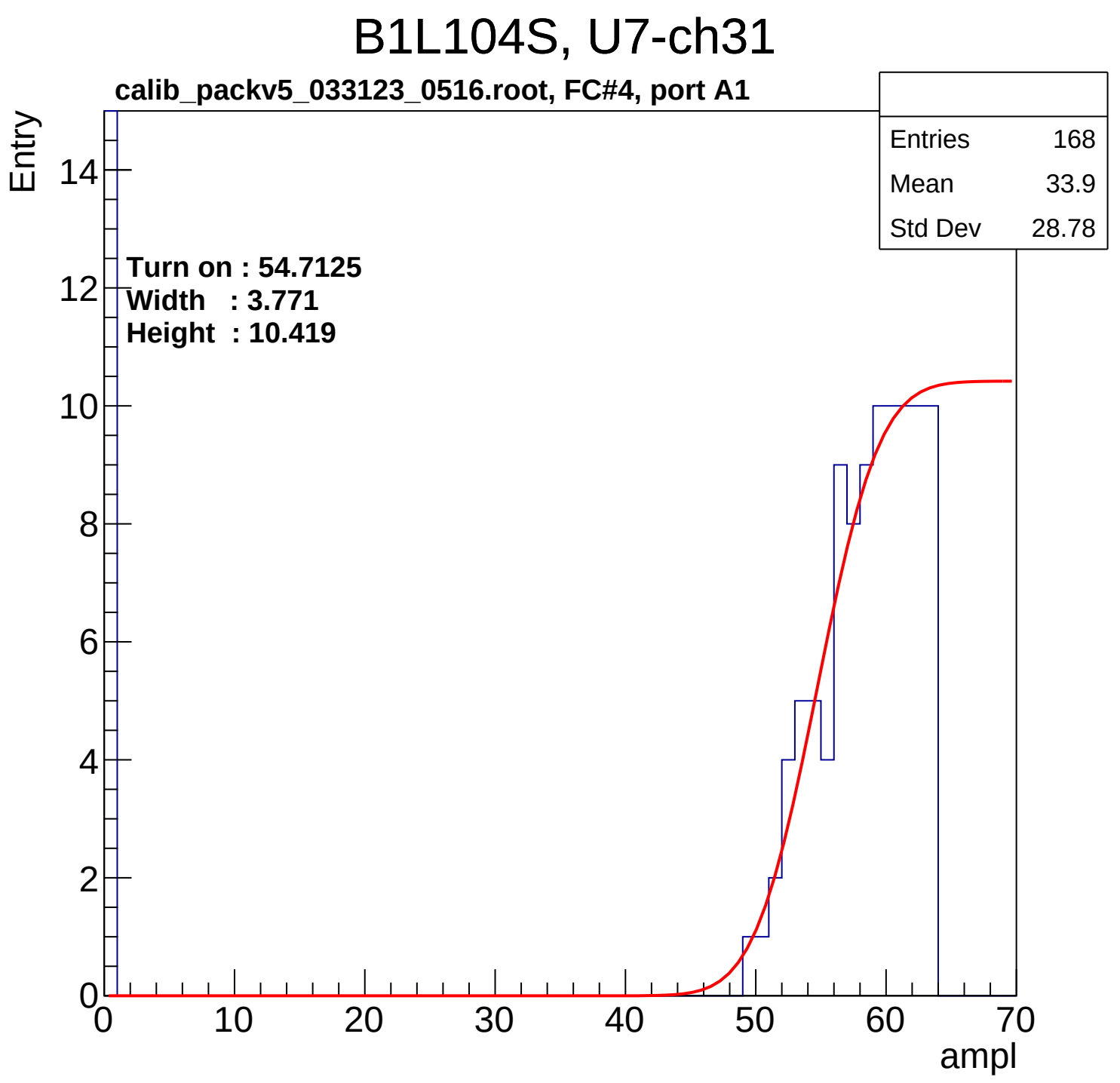

B1L104S, U7-ch26
calib_packv5_033123_0516.root, FC#4, port A1
Entries 182
Mean 36.22
Std Dev 27.83
Turn on : 53.2011
Width : 4.029
Height : 10.574
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

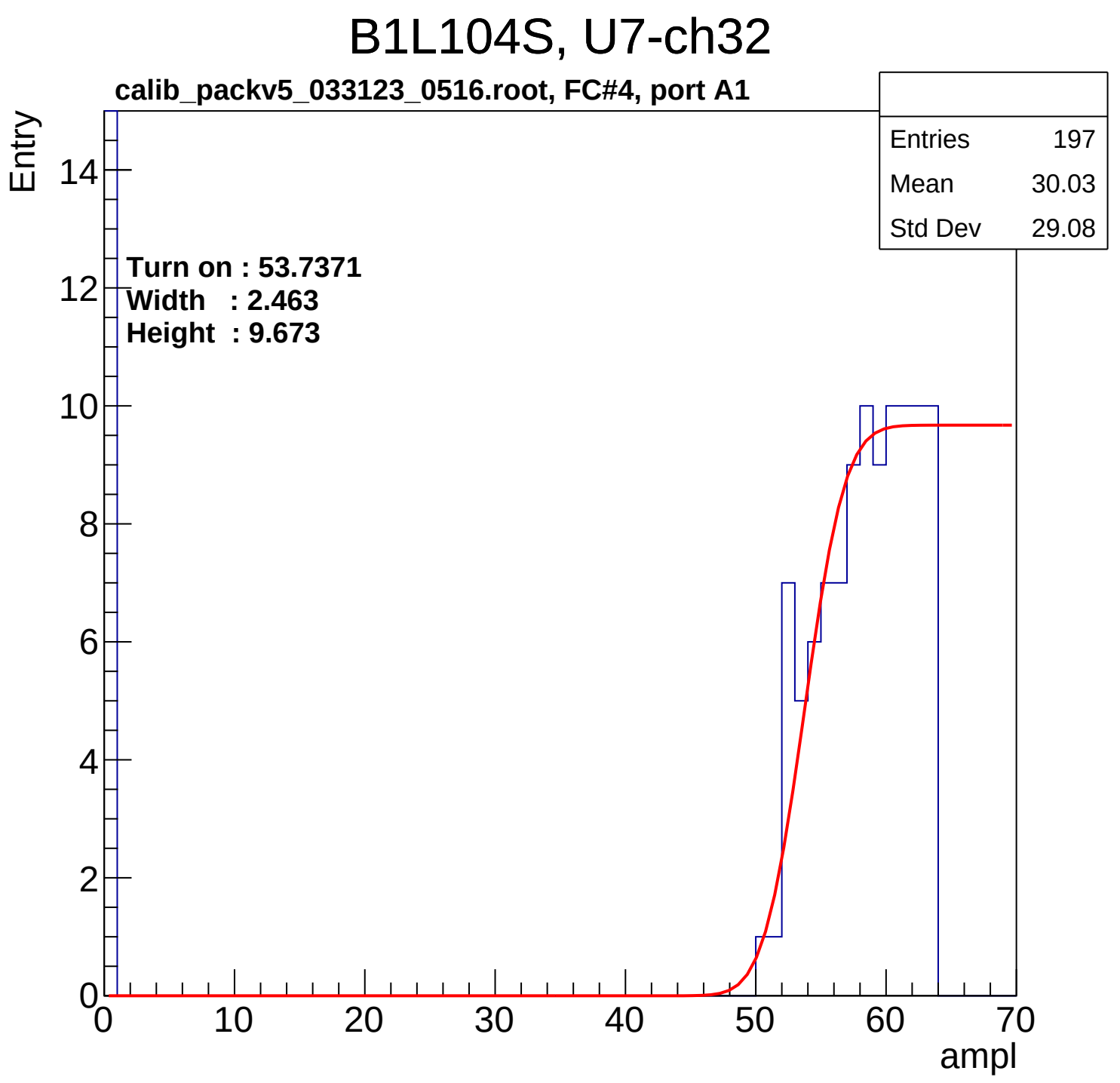

B1L104S, U7-ch27
calib_packv5_033123_0516.root, FC#4, port A1
Entries 172
Mean 38.65
Std Dev 27.05
Turn on : 53.2138
Width : 3.468
Height : 10.424
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

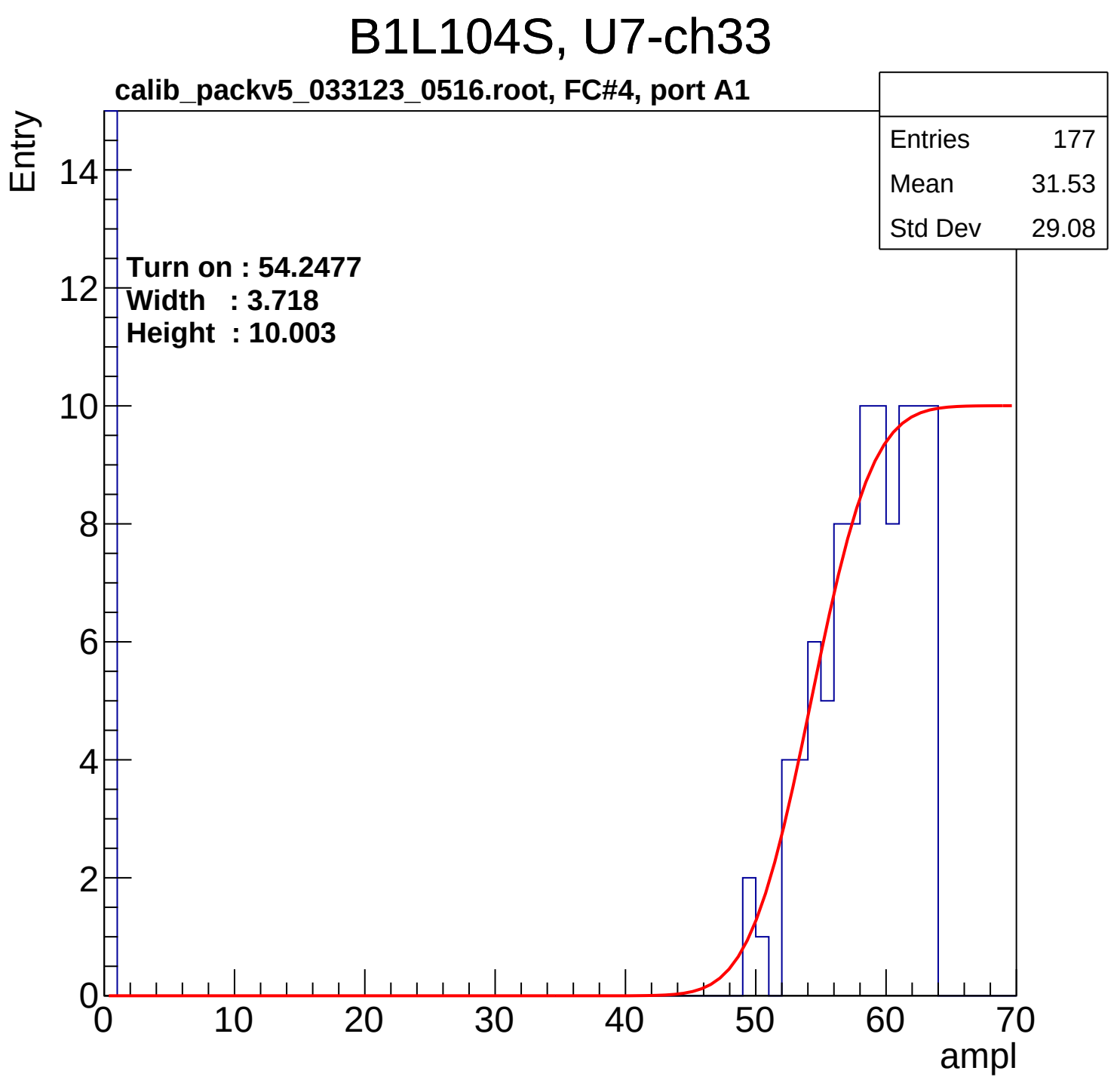

B1L104S, U7-ch28
calib_packv5_033123_0516.root, FC#4, port A1
Entries 170
Mean 29.64
Std Dev 29.07
Turn on : 54.5139
Width : 5.277
Height : 9.445
Entry
ampl
0
10
20
30
40
50
60
70
80

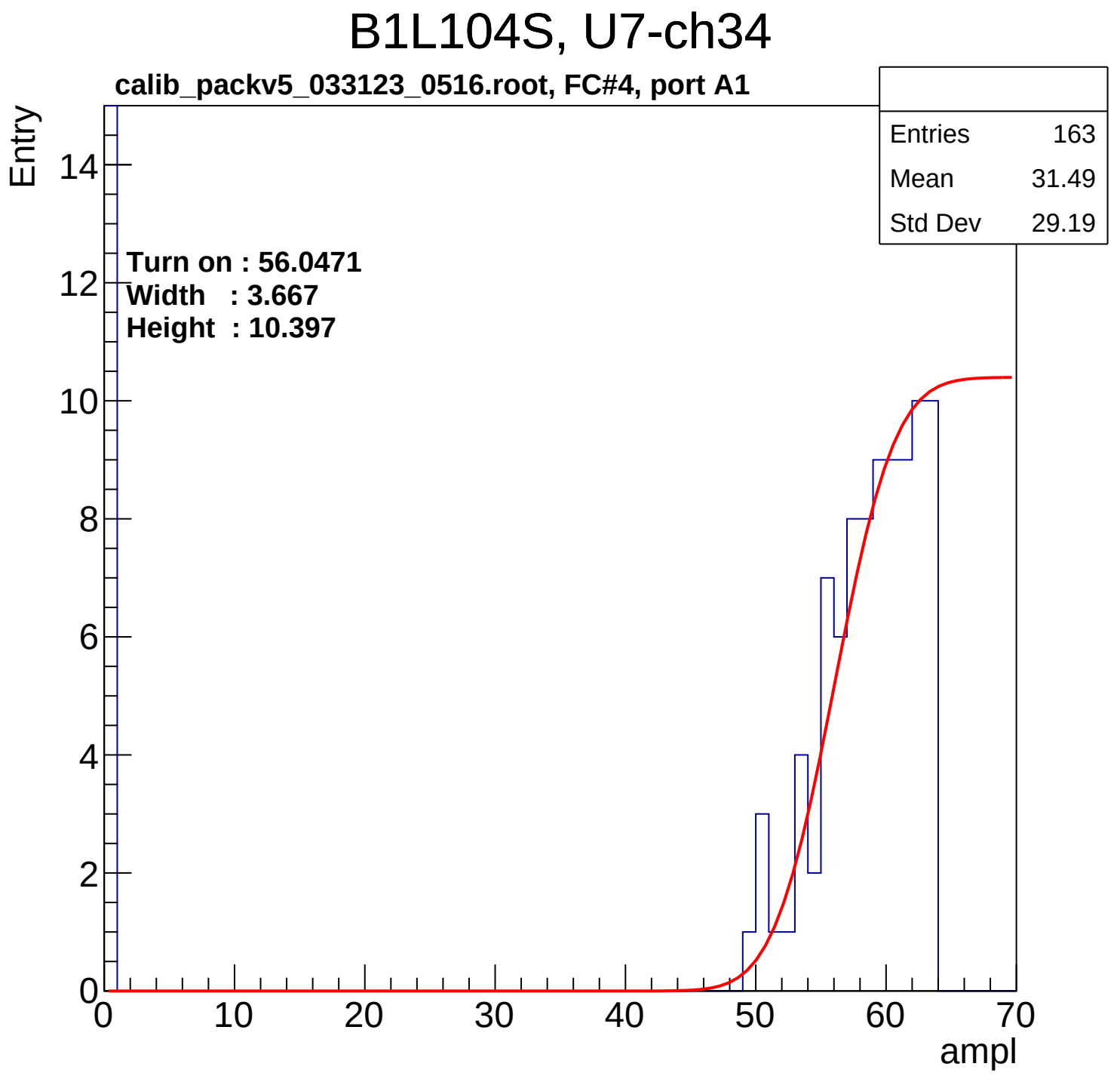

B1L104S, U7-ch29
calib_packv5_033123_0516.root, FC#4, port A1
Entries 171
Mean 35.79
Std Dev 28.19
Turn on : 54.4318
Width : 4.184
Height : 10.887
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

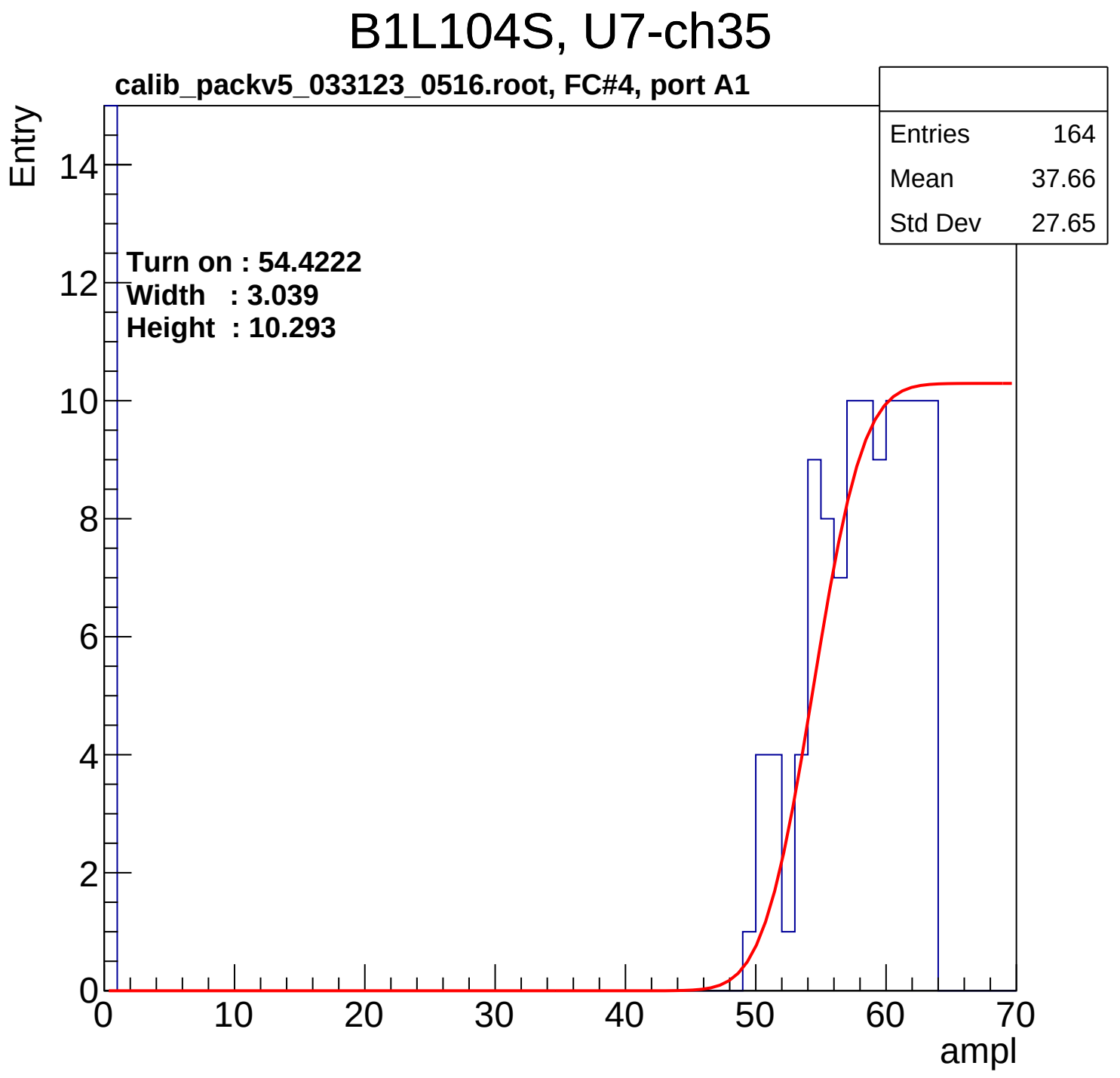

B1L104S, U7-ch30
calib_packv5_033123_0516.root, FC#4, port A1
Entries 193
Mean 35.67
Std Dev 27.73
Turn on : 52.4308
Width : 3.980
Height : 10.290
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

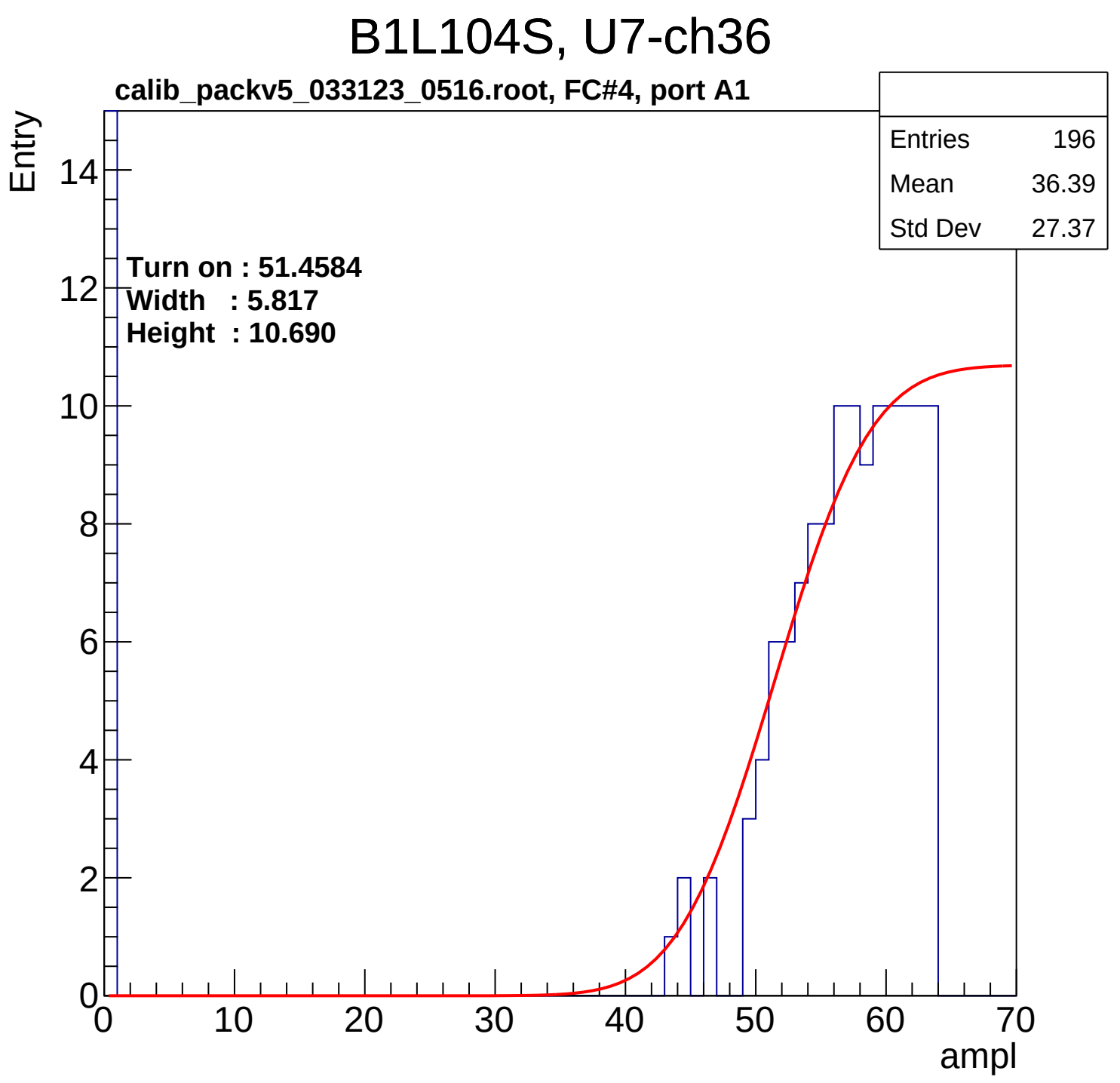

B1L104S, U7-ch31
calib_packv5_033123_0516.root, FC#4, port A1
Entries 168
Mean 33.9
Std Dev 28.78
Turn on : 54.7125
Width : 3.771
Height : 10.419
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

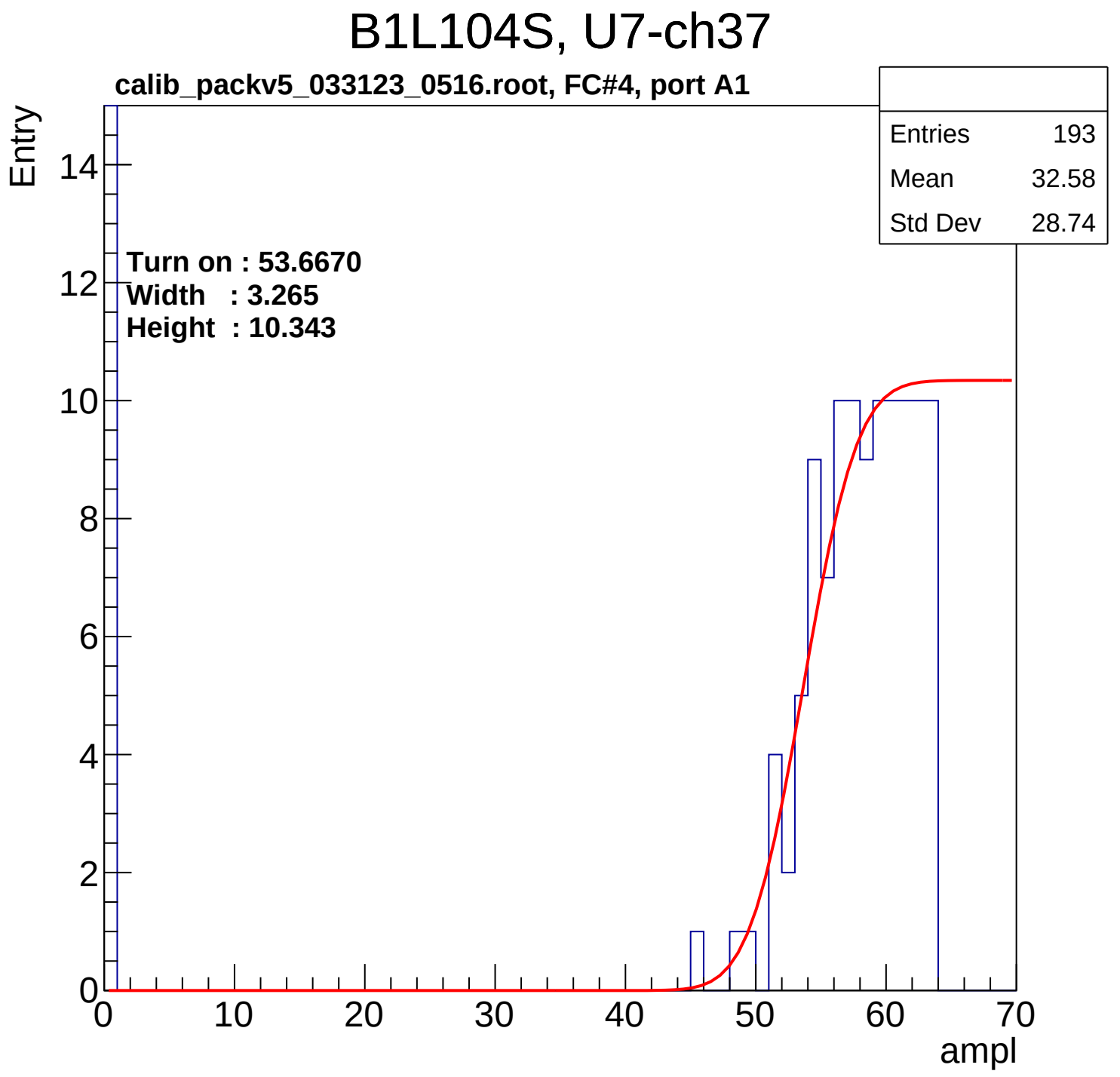

B1L104S, U7-ch32
calib_packv5_033123_0516.root, FC#4, port A1
Entries 197
Mean 30.03
Std Dev 29.08
Turn on : 53.7371
Width : 2.463
Height : 9.673
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

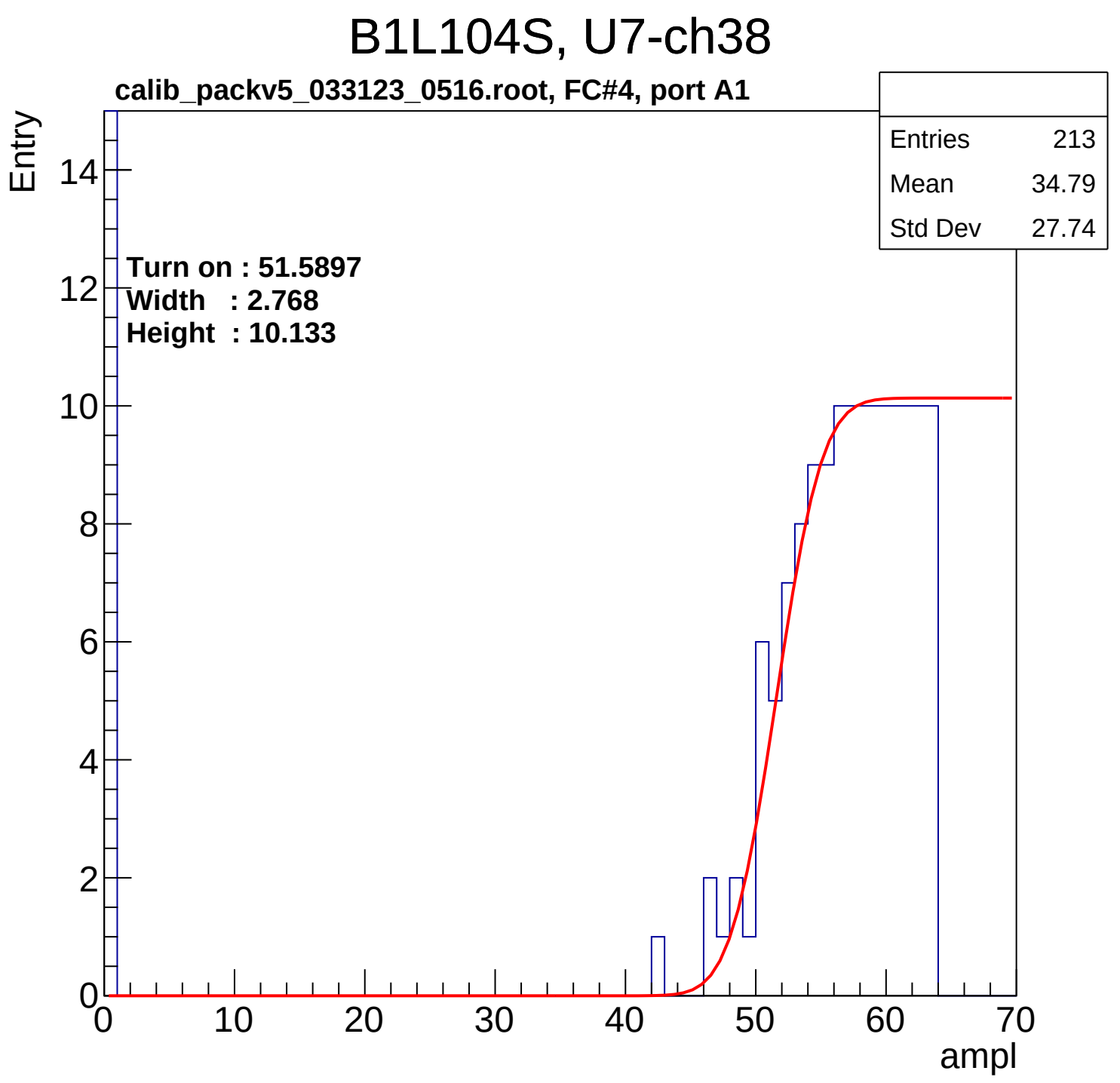

B1L104S, U7-ch33
calib_packv5_033123_0516.root, FC#4, port A1
Entries 177
Mean 31.53
Std Dev 29.08
Turn on : 54.2477
Width : 3.718
Height : 10.003
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

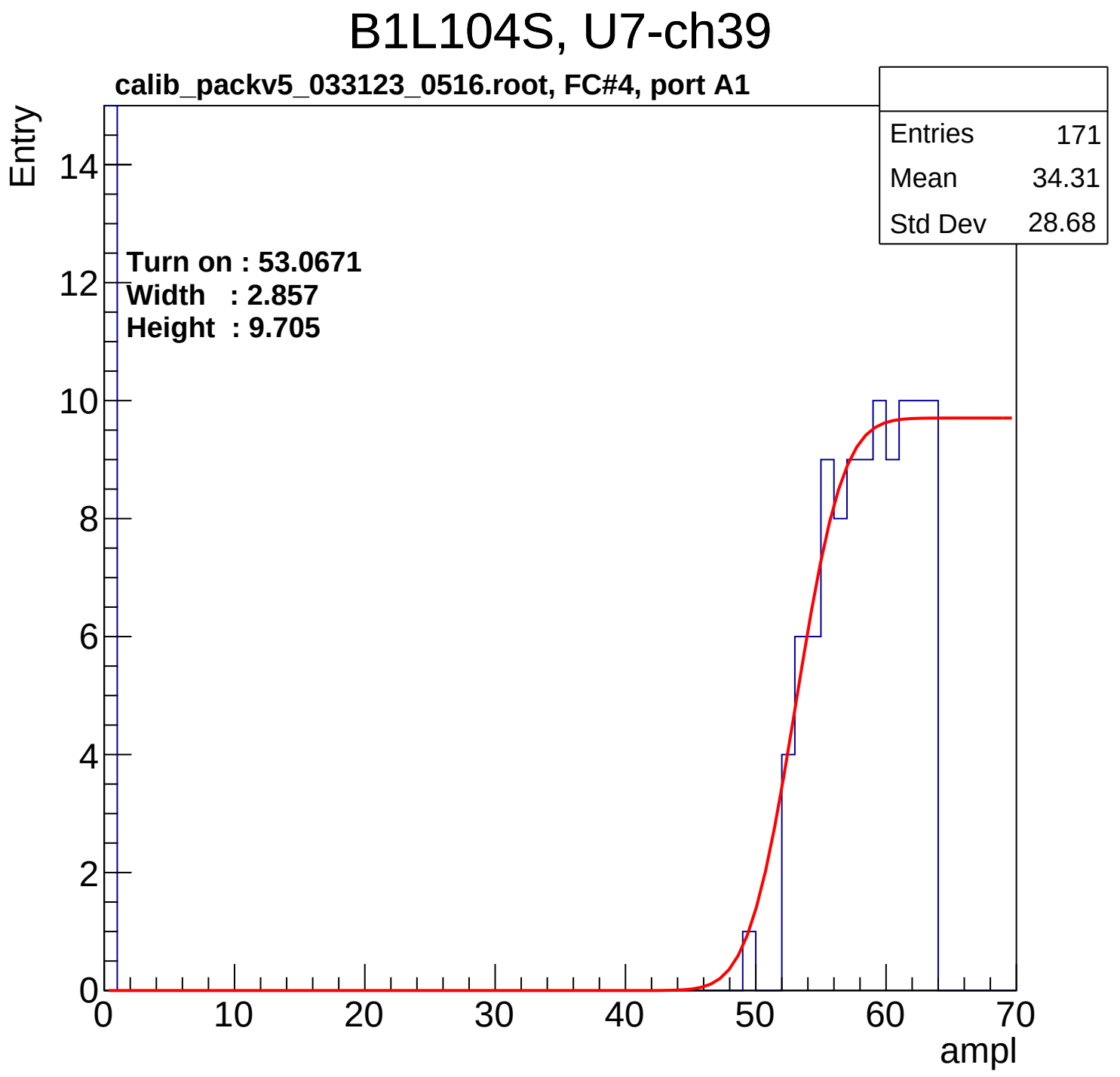

B1L104S, U7-ch34
calib_packv5_033123_0516.root, FC#4, port A1
Entries 163
Mean 31.49
Std Dev 29.19
Turn on : 56.0471
Width : 3.667
Height : 10.397
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

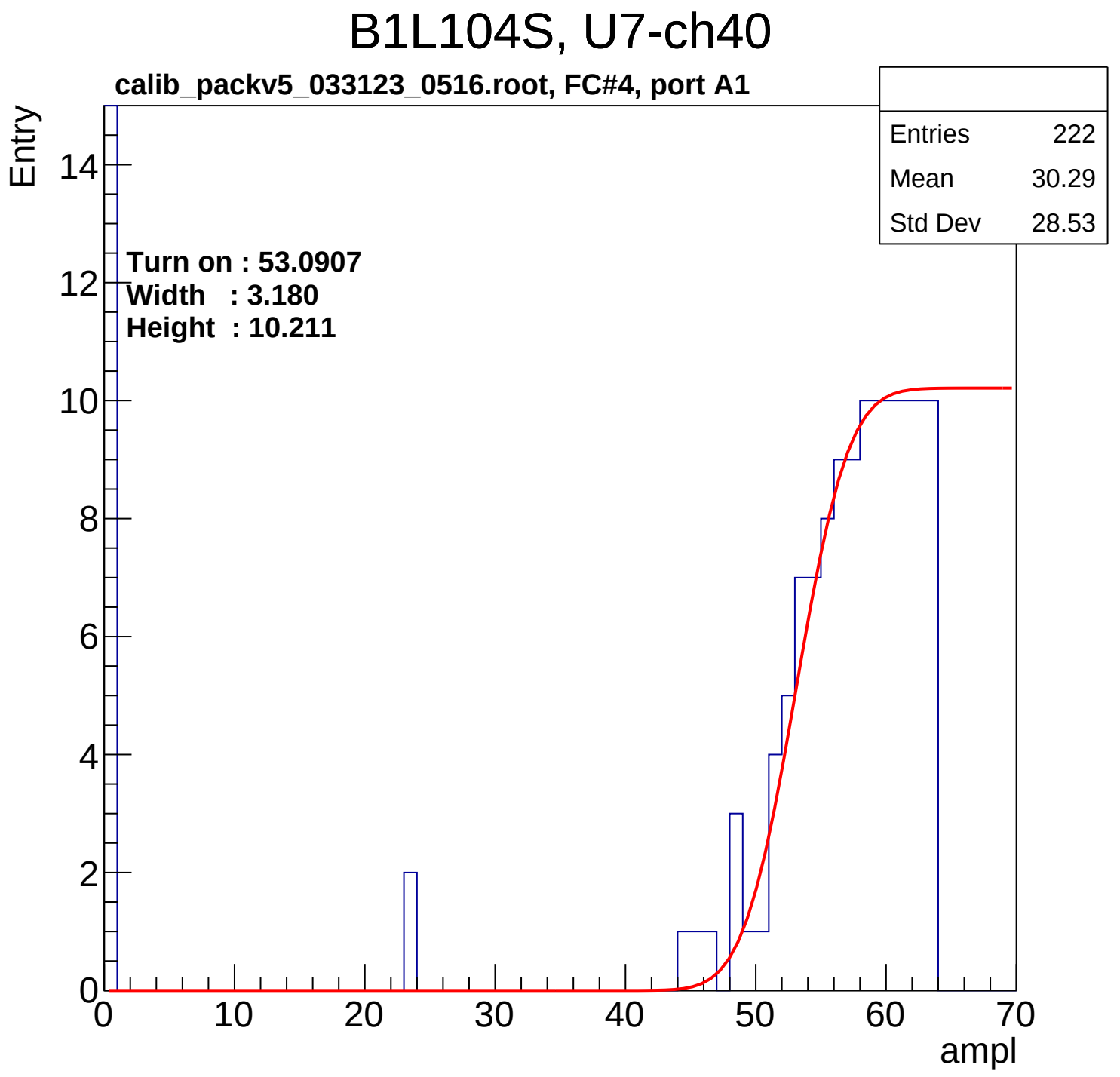

B1L104S, U7-ch35
calib_packv5_033123_0516.root, FC#4, port A1
Entries 164
Mean 37.66
Std Dev 27.65
Turn on : 54.4222
Width : 3.039
Height : 10.293
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

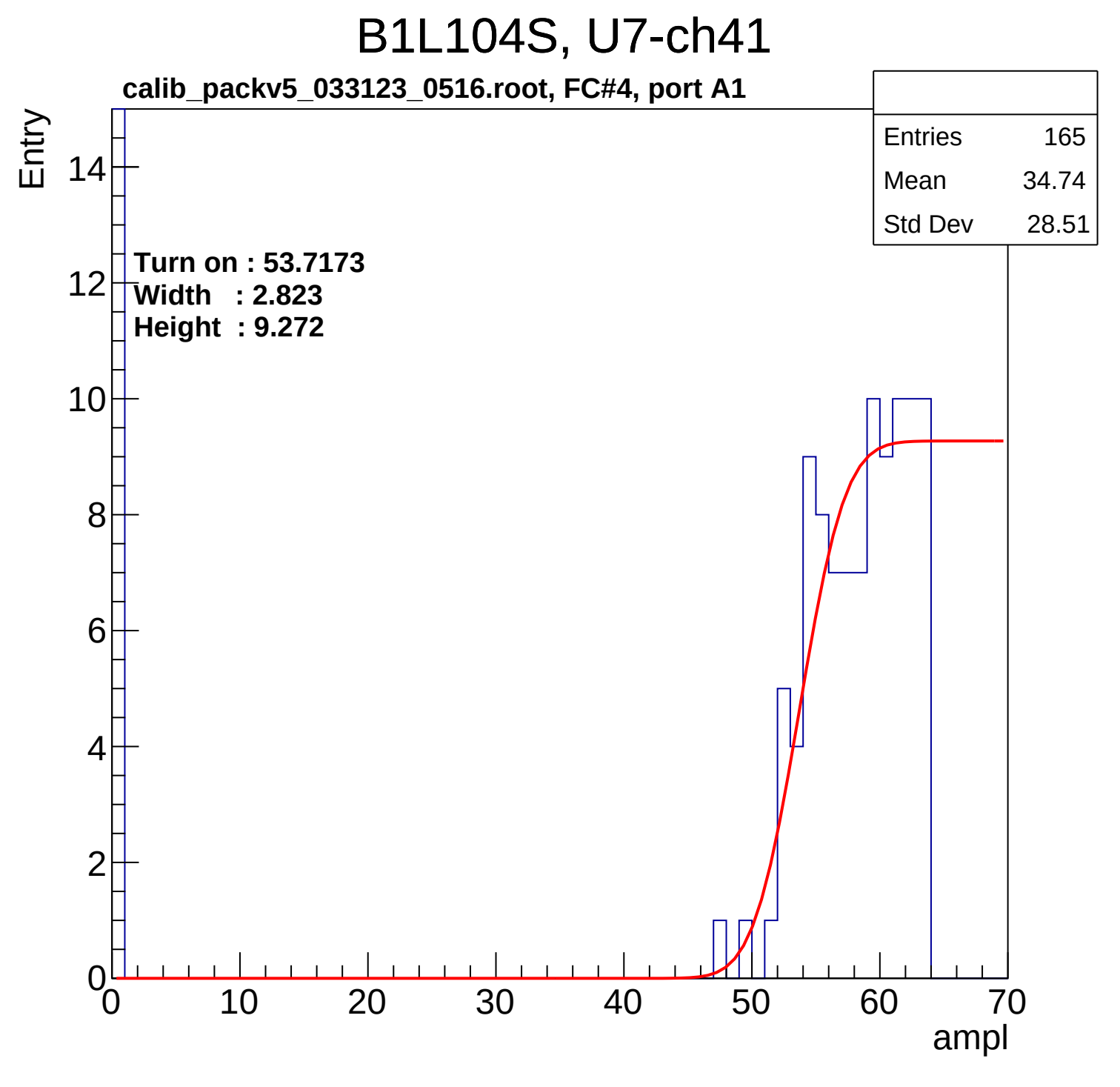

B1L104S, U7-ch36
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 36.39
Std Dev 27.37
Turn on : 51.4584
Width : 5.817
Height : 10.690
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

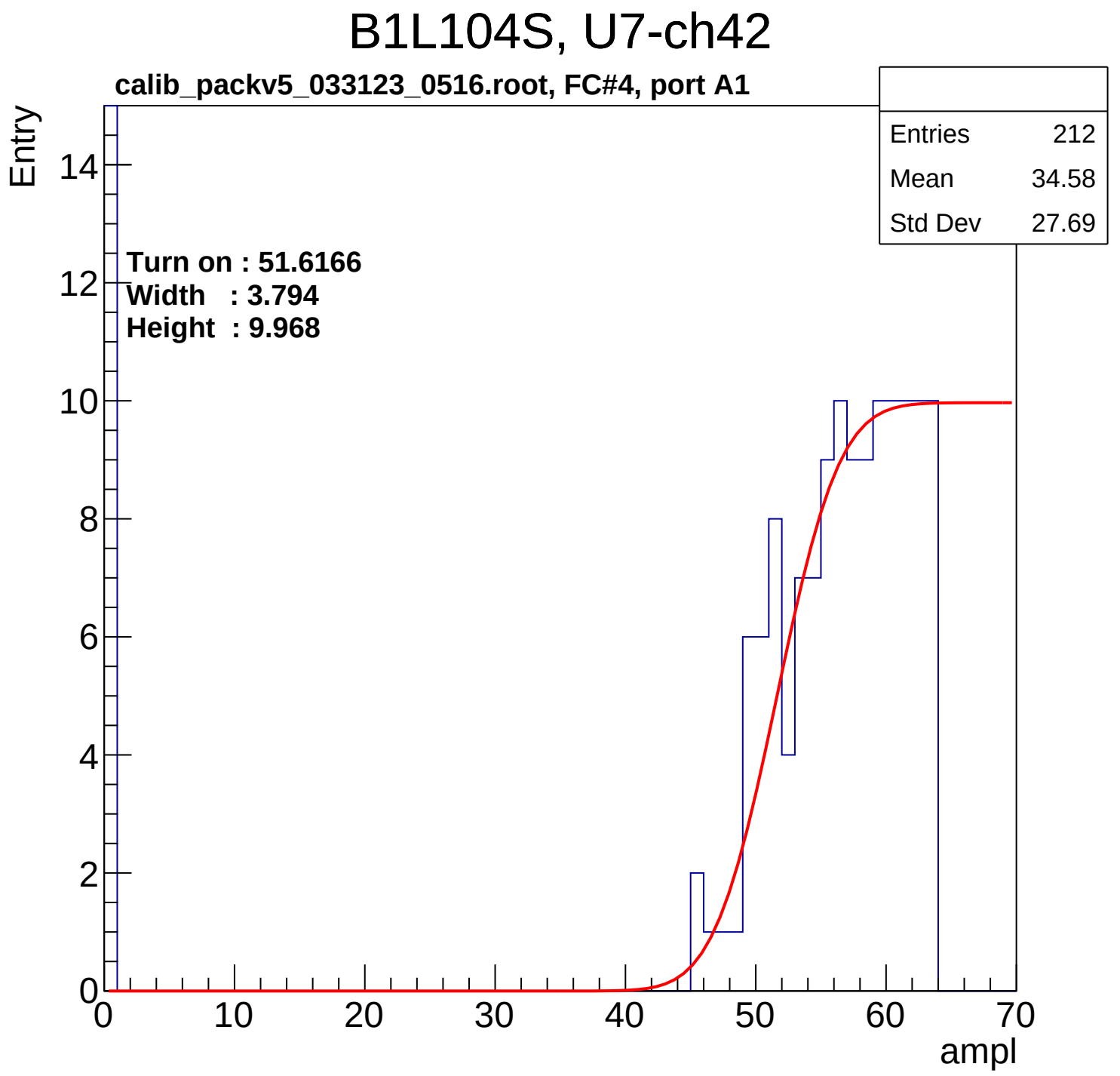

B1L104S, U7-ch37
calib_packv5_033123_0516.root, FC#4, port A1
Entries 193
Mean 32.58
Std Dev 28.74
Turn on : 53.6670
Width : 3.265
Height : 10.343
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

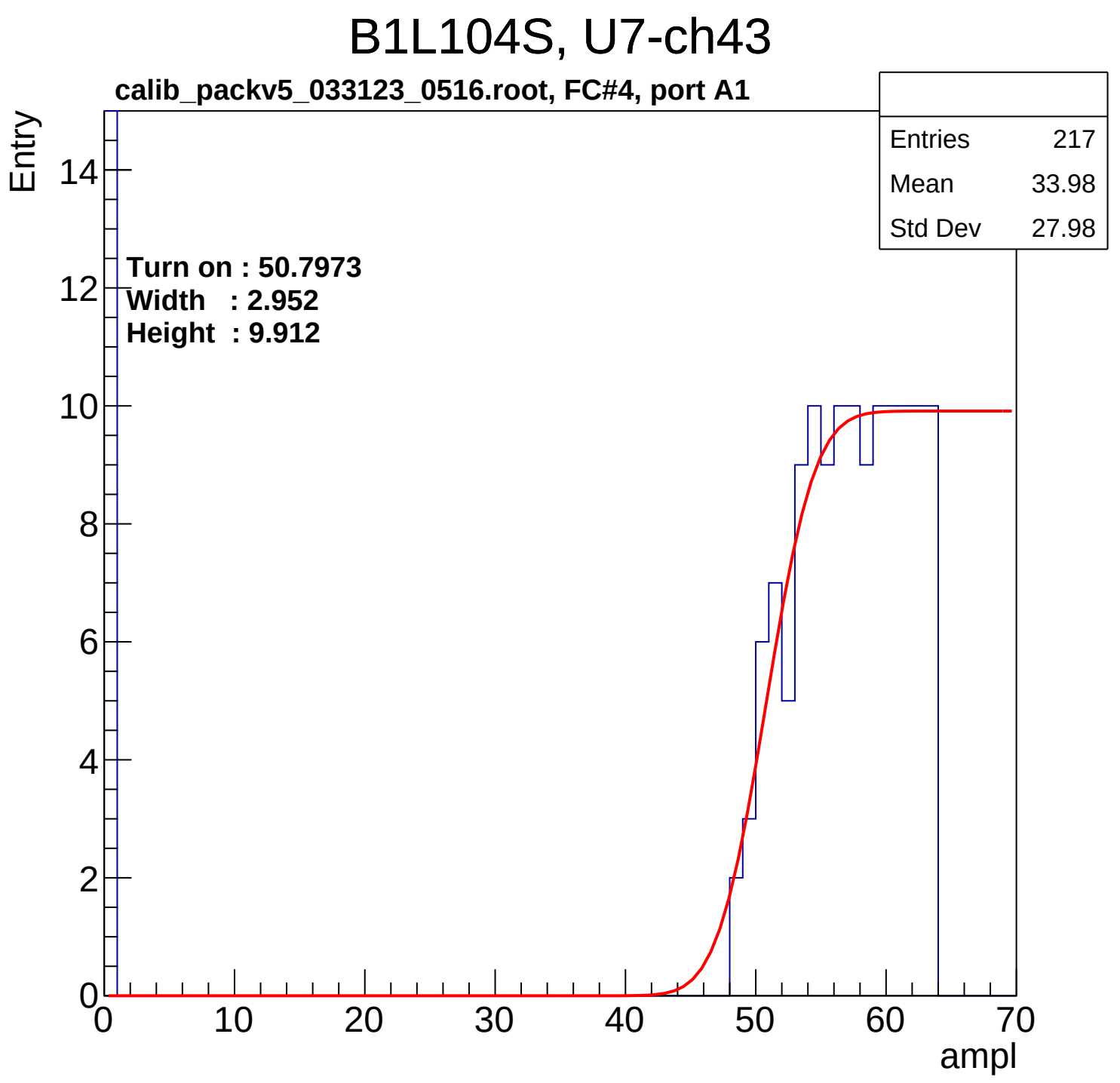

B1L104S, U7-ch38
calib_packv5_033123_0516.root, FC#4, port A1
Entries 213
Mean 34.79
Std Dev 27.74
Turn on : 51.5897
Width : 2.768
Height : 10.133
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

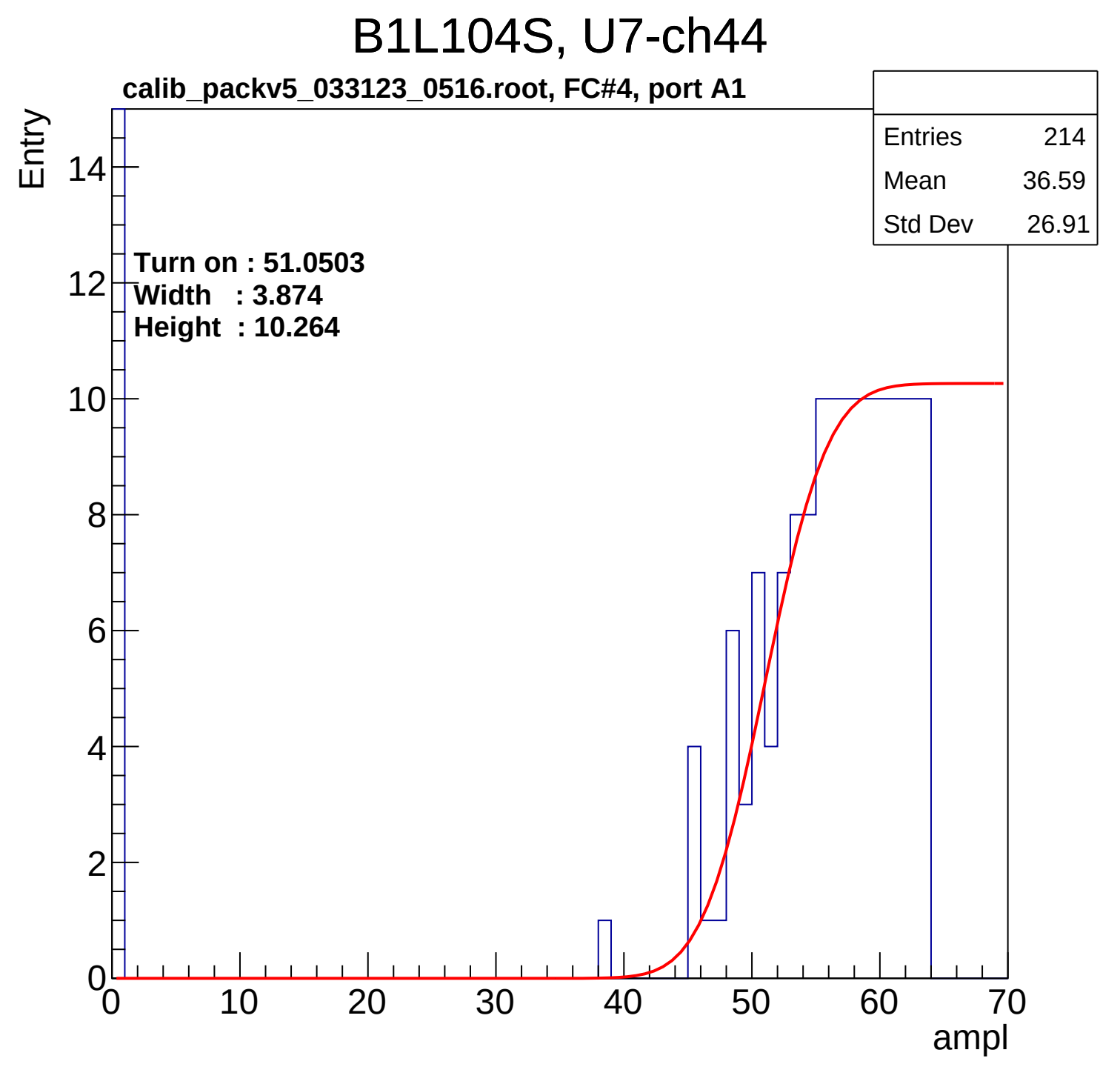

B1L104S, U7-ch39
calib_packv5_033123_0516.root, FC#4, port A1
Entries 171
Mean 34.31
Std Dev 28.68
Turn on : 53.0671
Width : 2.857
Height : 9.705
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

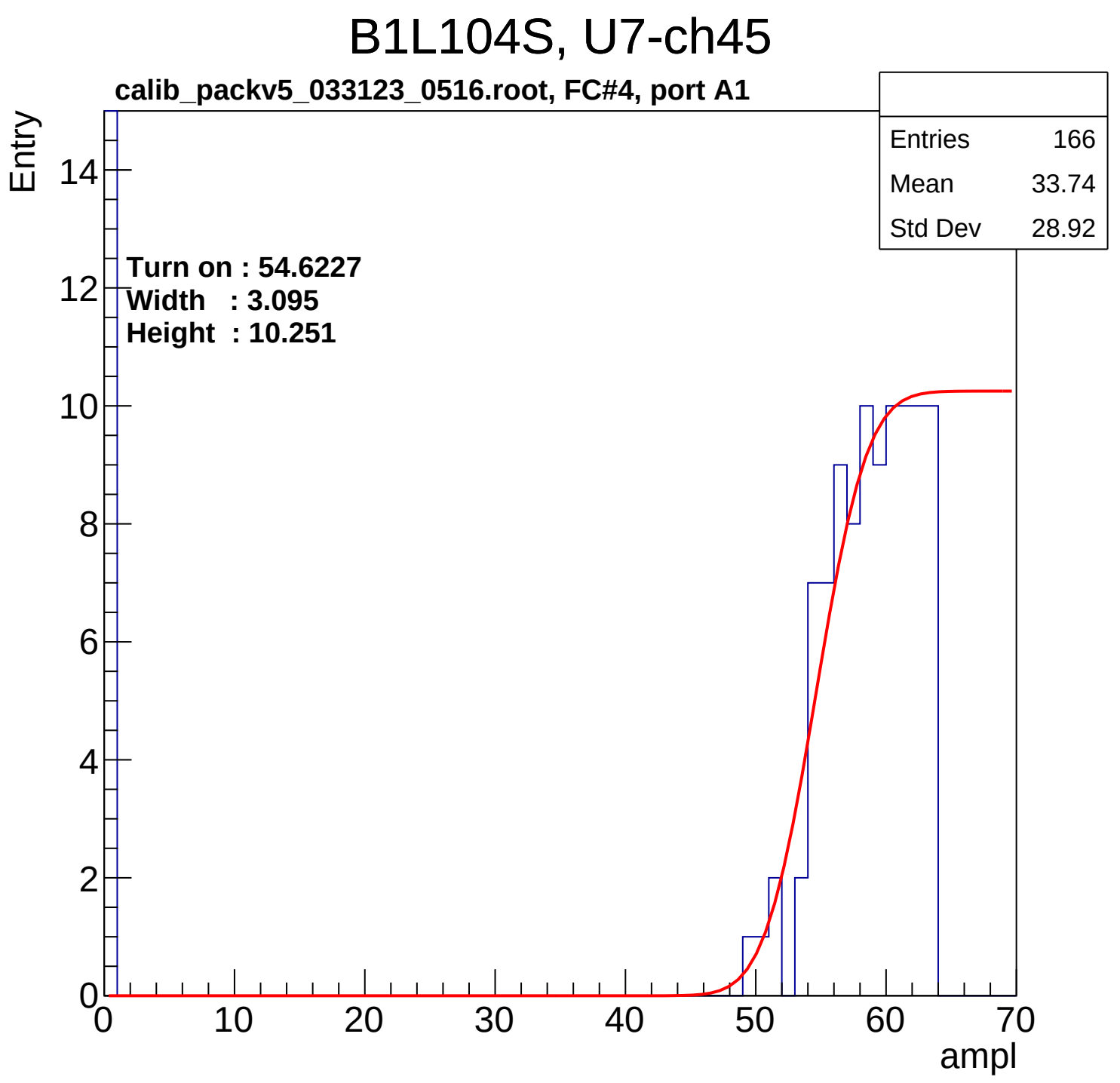

B1L104S, U7-ch40
calib_packv5_033123_0516.root, FC#4, port A1
Entries 222
Mean 30.29
Std Dev 28.53
Turn on : 53.0907
Width : 3.180
Height : 10.211
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

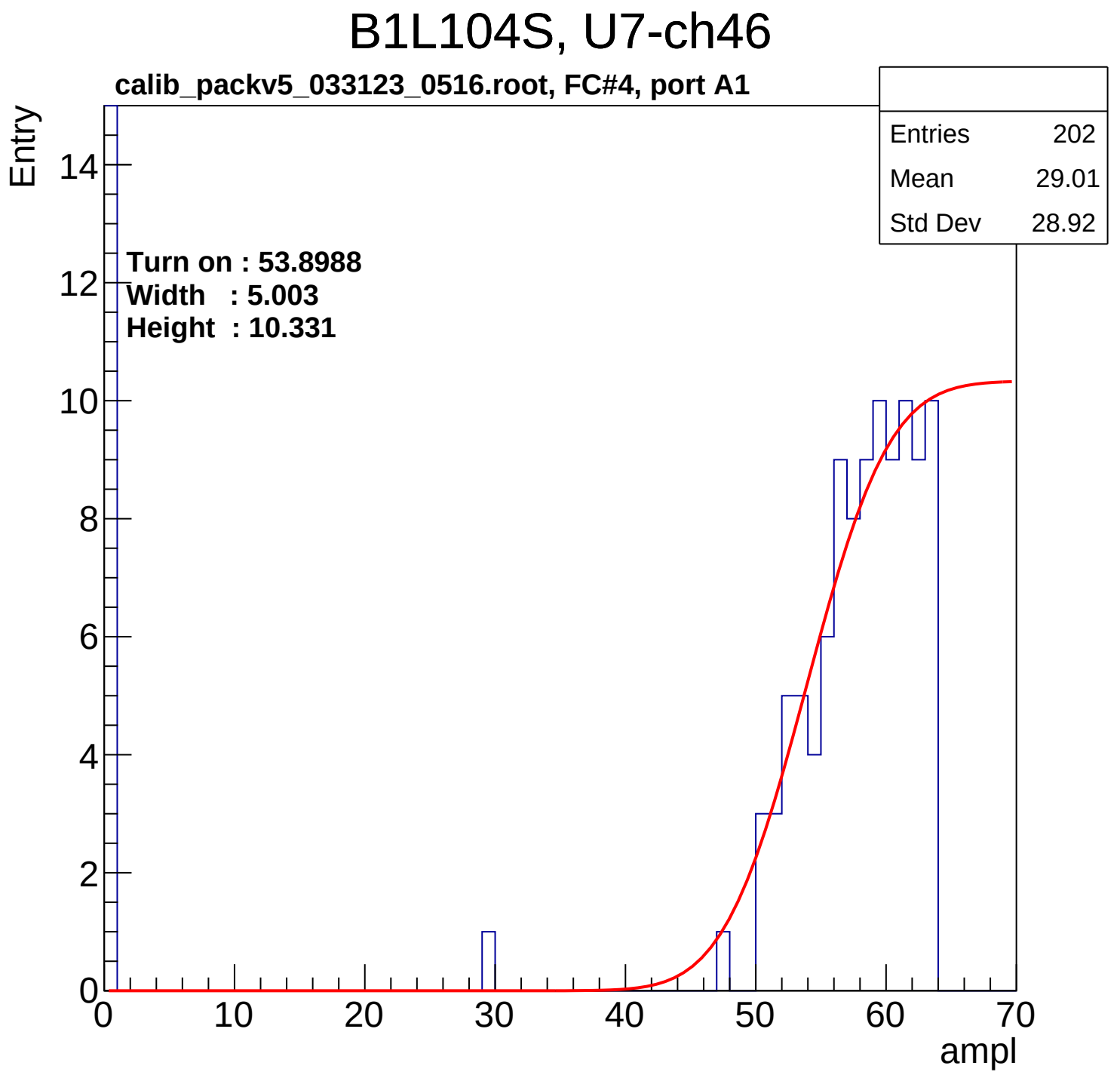

B1L104S, U7-ch41
calib_packv5_033123_0516.root, FC#4, port A1
Entries 165
Mean 34.74
Std Dev 28.51
Turn on : 53.7173
Width : 2.823
Height : 9.272
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

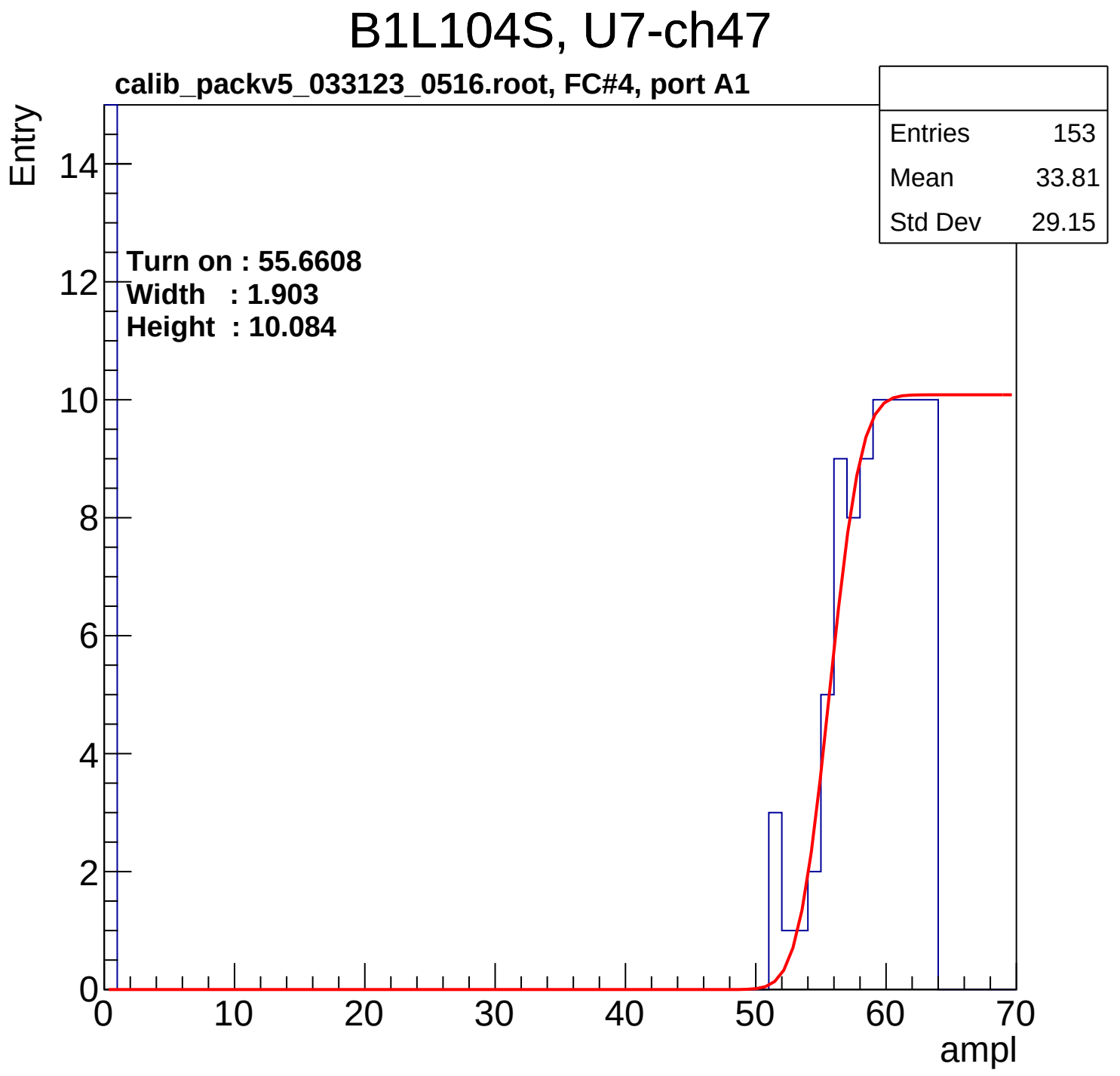

B1L104S, U7-ch42
calib_packv5_033123_0516.root, FC#4, port A1
Entries 212
Mean 34.58
Std Dev 27.69
Turn on : 51.6166
Width : 3.794
Height : 9.968
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

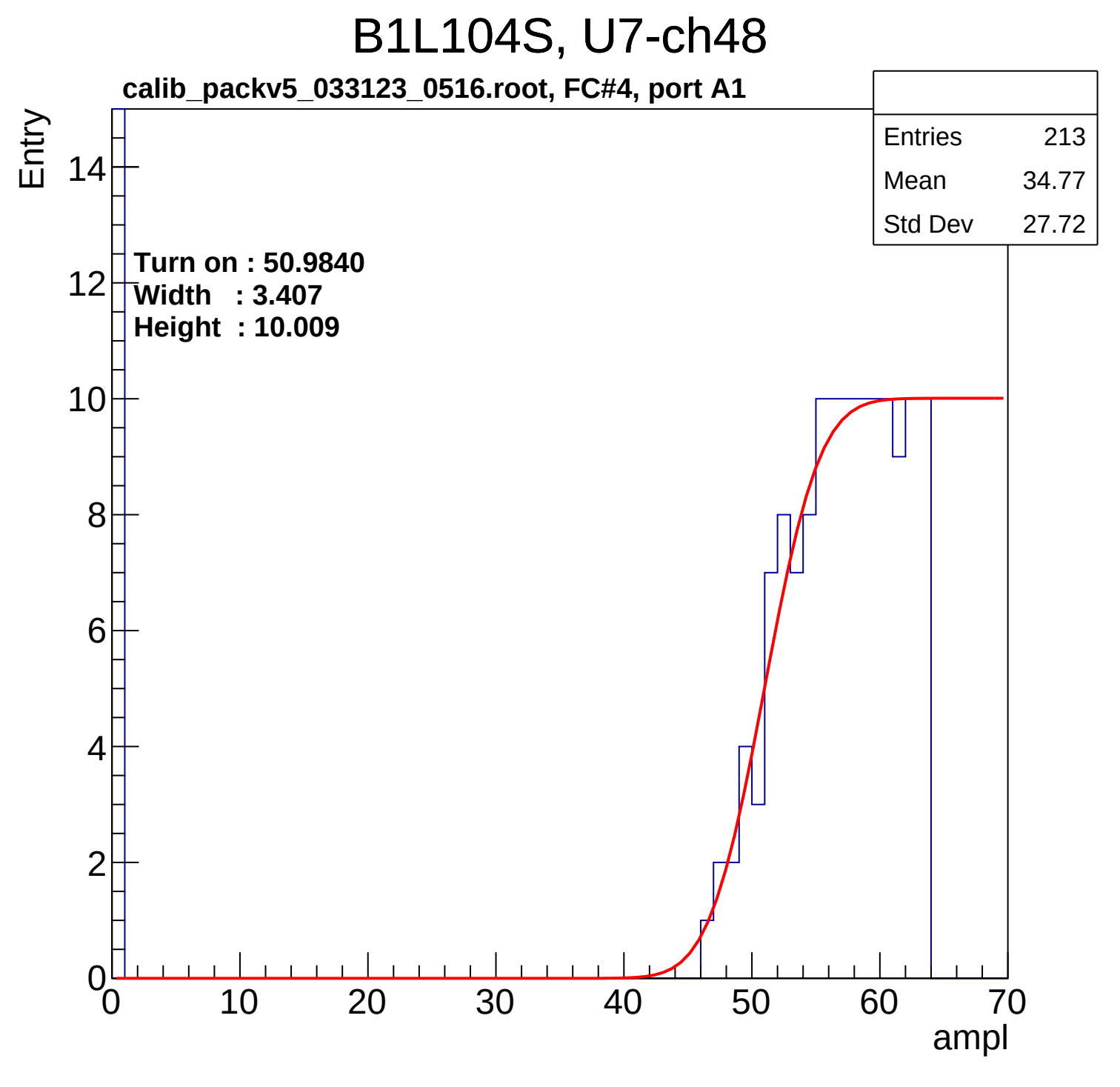

B1L104S, U7-ch43
calib_packv5_033123_0516.root, FC#4, port A1
Entries 217
Mean 33.98
Std Dev 27.98
Turn on : 50.7973
Width : 2.952
Height : 9.912
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

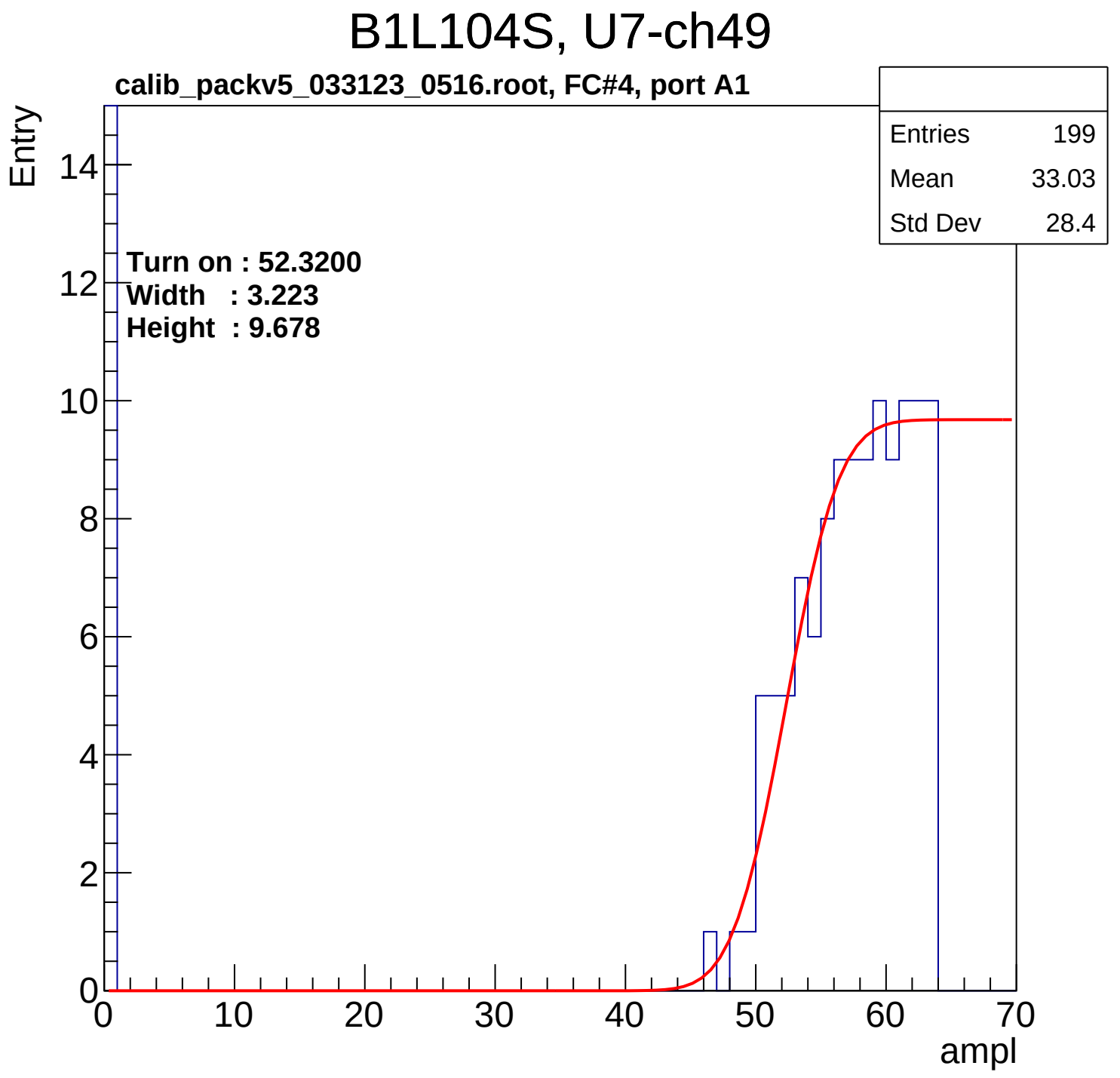

B1L104S, U7-ch44
calib_packv5_033123_0516.root, FC#4, port A1
Entries 214
Mean 36.59
Std Dev 26.91
Turn on : 51.0503
Width : 3.874
Height : 10.264
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

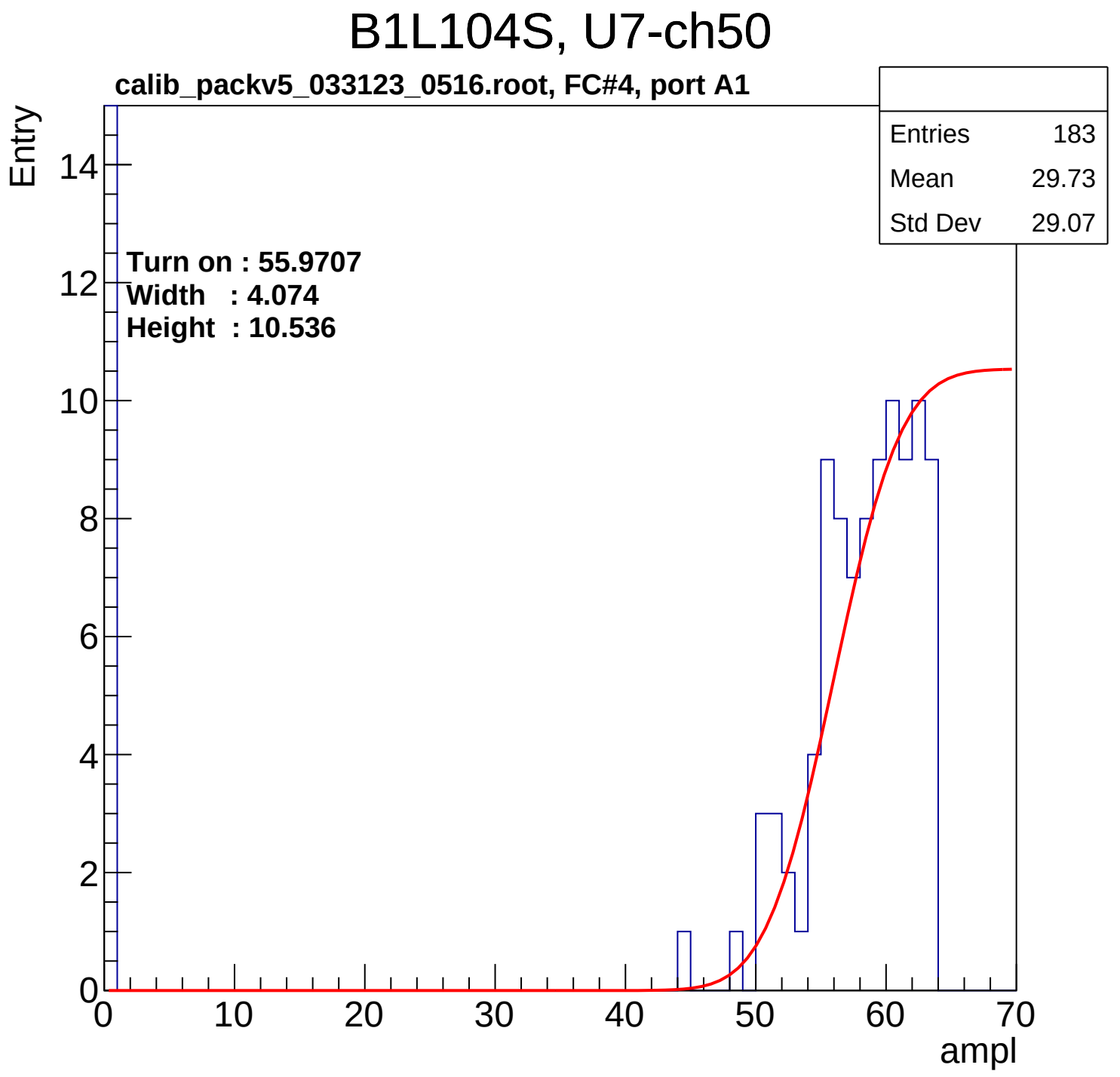

B1L104S, U7-ch45
calib_packv5_033123_0516.root, FC#4, port A1
Entries 166
Mean 33.74
Std Dev 28.92
Turn on : 54.6227
Width : 3.095
Height : 10.251
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

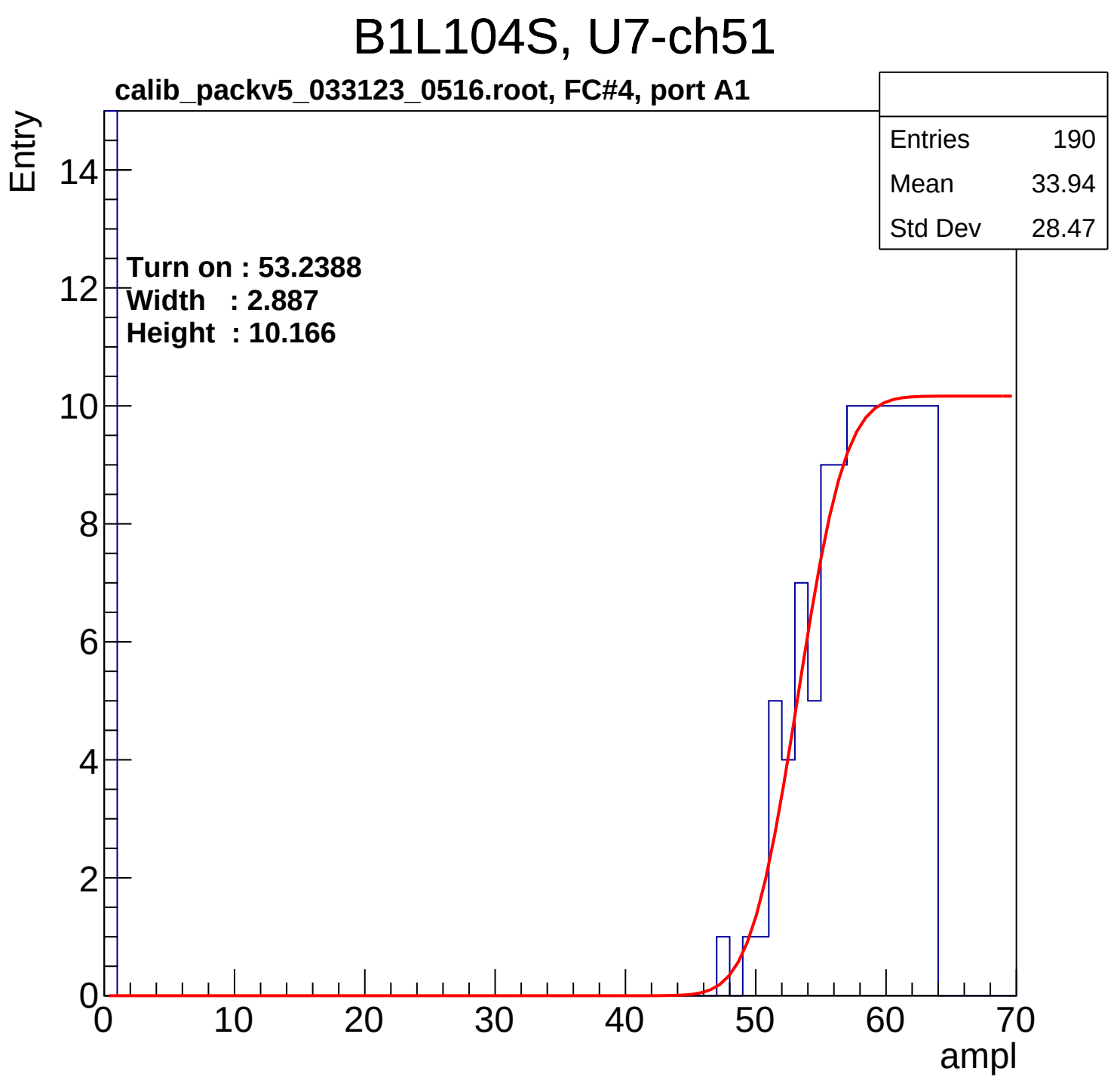

B1L104S, U7-ch46
calib_packv5_033123_0516.root, FC#4, port A1
Entries 202
Mean 29.01
Std Dev 28.92
Turn on : 53.8988
Width : 5.003
Height : 10.331
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

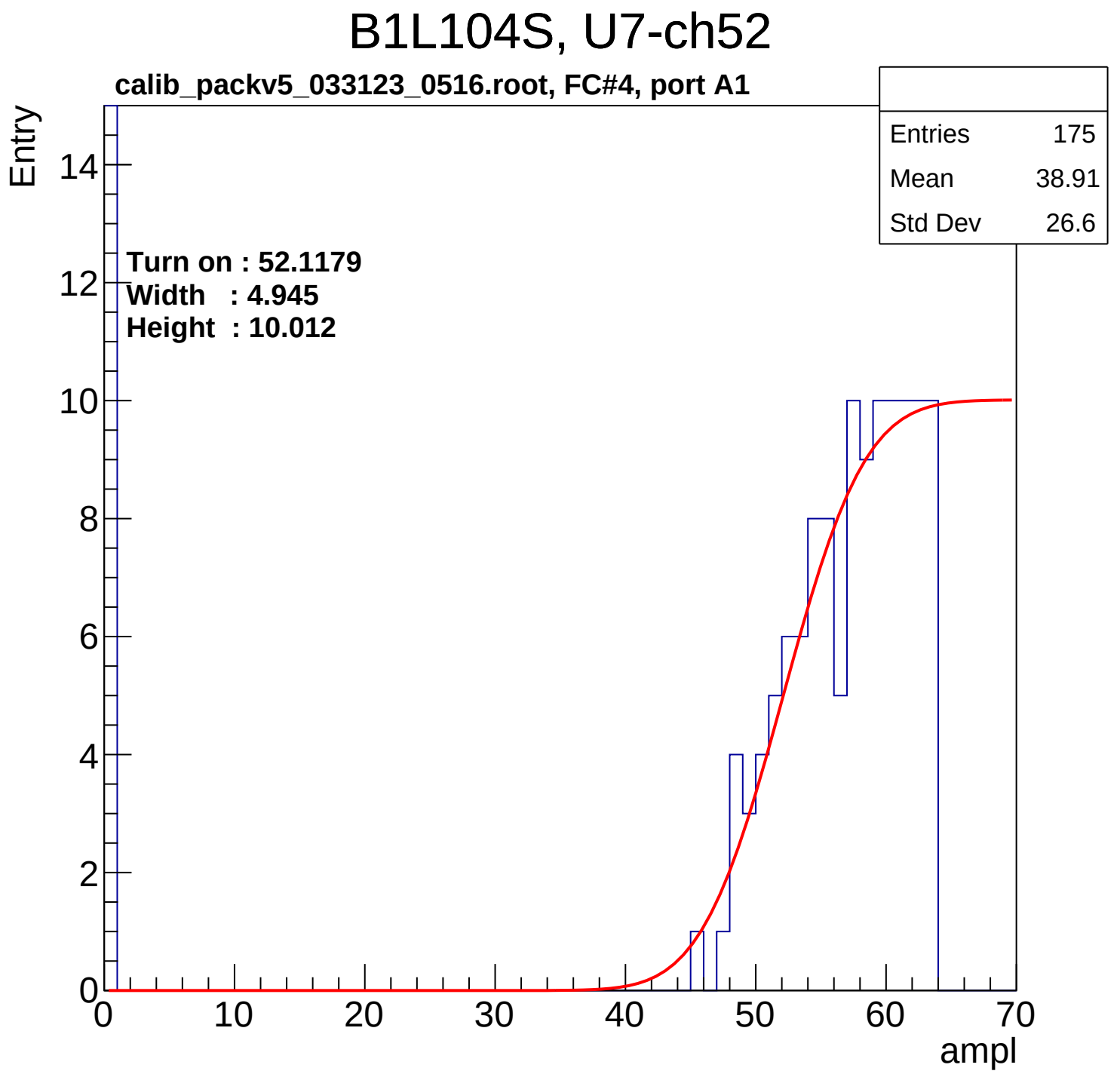

B1L104S, U7-ch47
calib_packv5_033123_0516.root, FC#4, port A1
Entries 153
Mean 33.81
Std Dev 29.15
Turn on : 55.6608
Width : 1.903
Height : 10.084
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

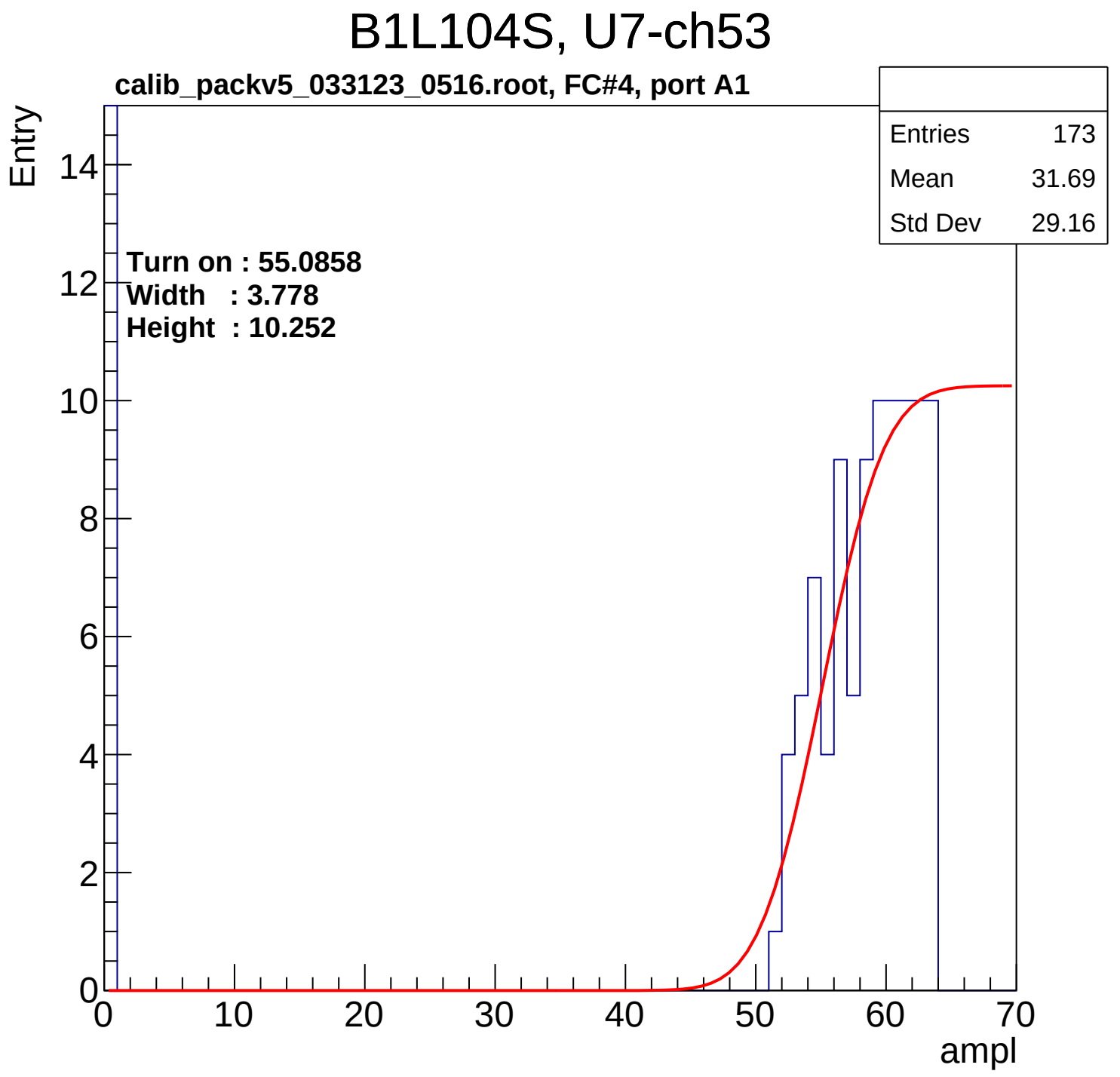

B1L104S, U7-ch48
calib_packv5_033123_0516.root, FC#4, port A1
Entries 213
Mean 34.77
Std Dev 27.72
Turn on : 50.9840
Width : 3.407
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

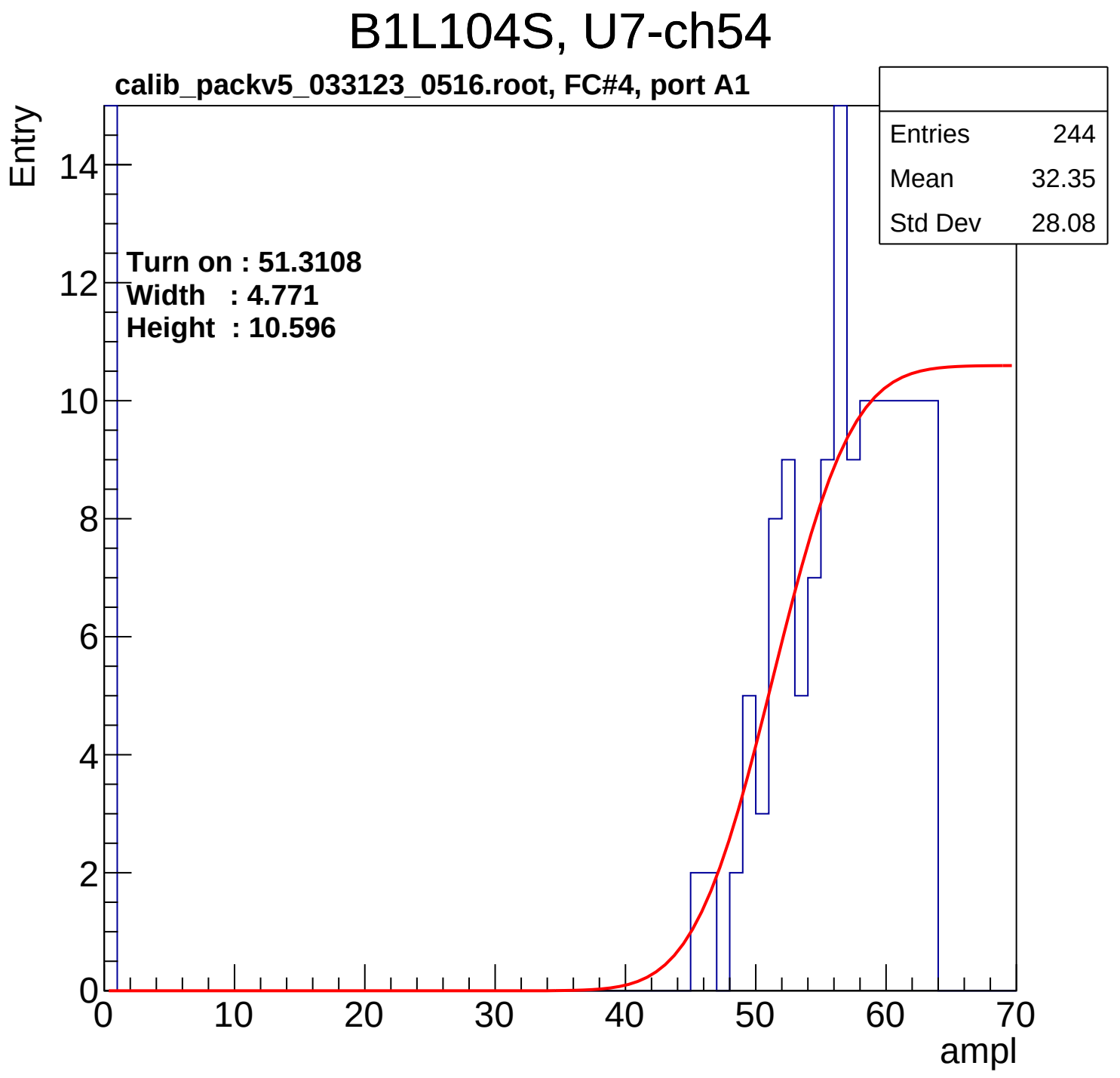

B1L104S, U7-ch49
calib_packv5_033123_0516.root, FC#4, port A1
Entries 199
Mean 33.03
Std Dev 28.4
Turn on : 52.3200
Width : 3.223
Height : 9.678
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

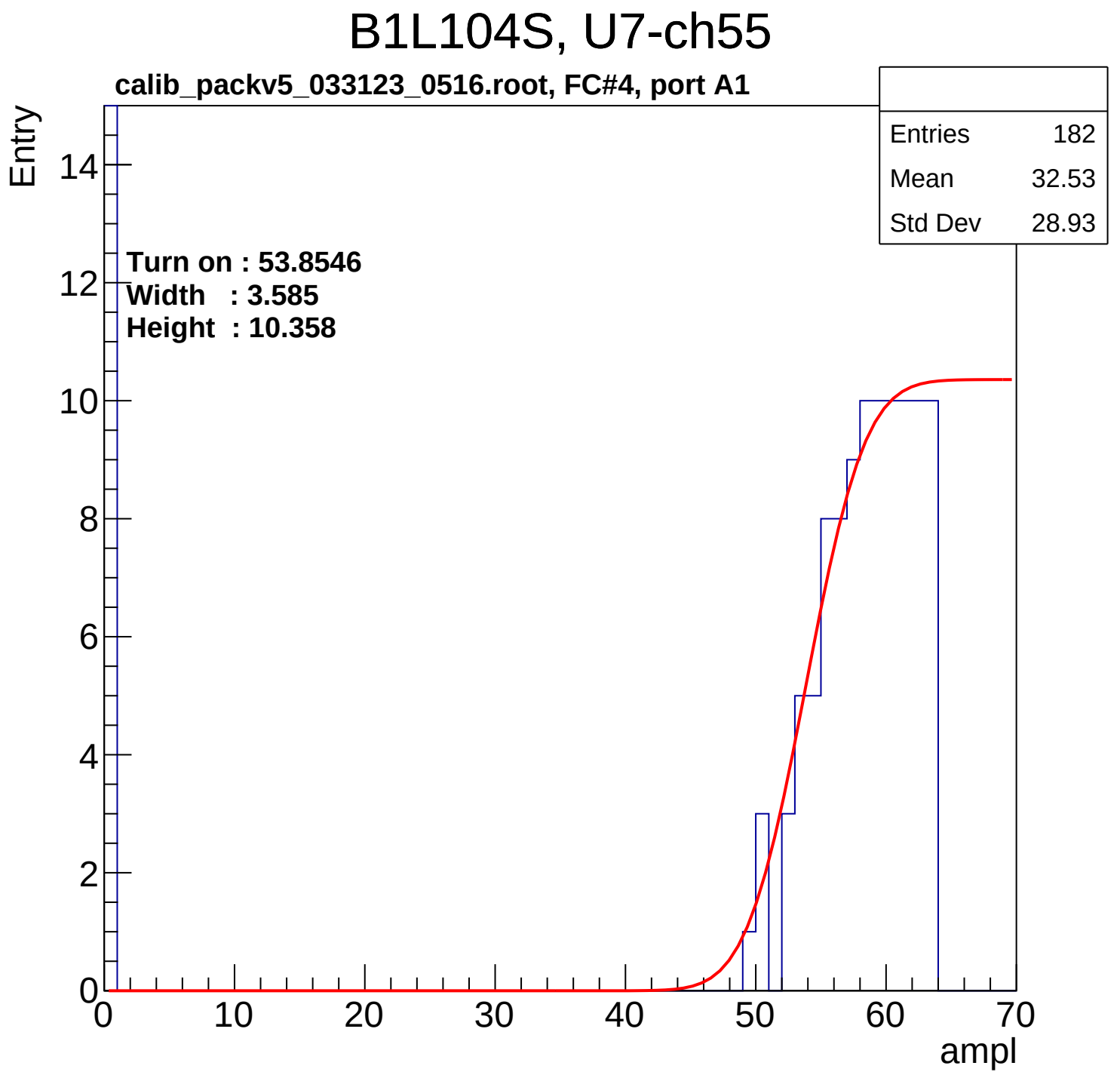

B1L104S, U7-ch50
calib_packv5_033123_0516.root, FC#4, port A1
Entries 183
Mean 29.73
Std Dev 29.07
Turn on : 55.9707
Width : 4.074
Height : 10.536
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

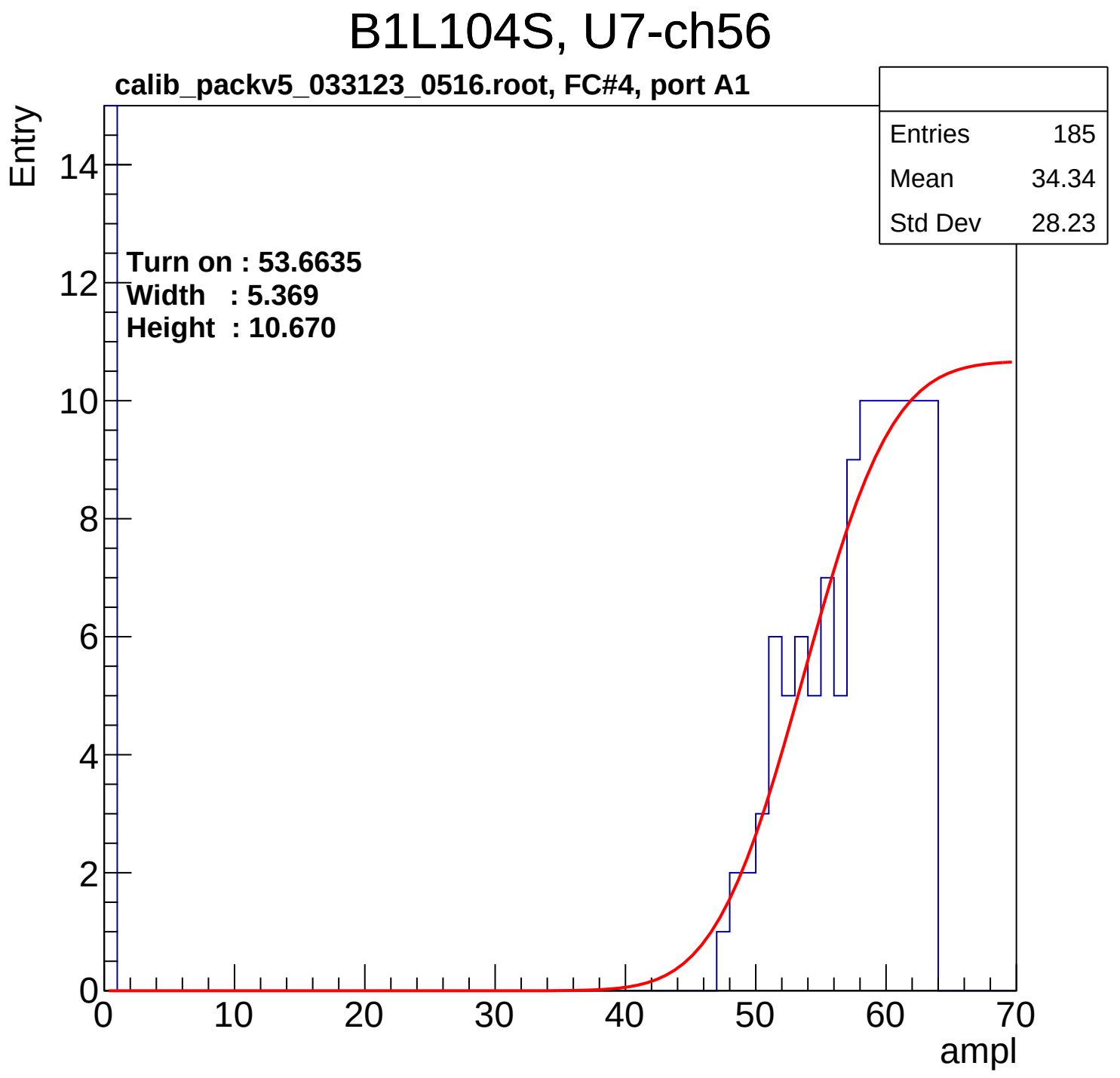

B1L104S, U7-ch51
calib_packv5_033123_0516.root, FC#4, port A1
Entries 190
Mean 33.94
Std Dev 28.47
Turn on : 53.2388
Width : 2.887
Height : 10.166
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

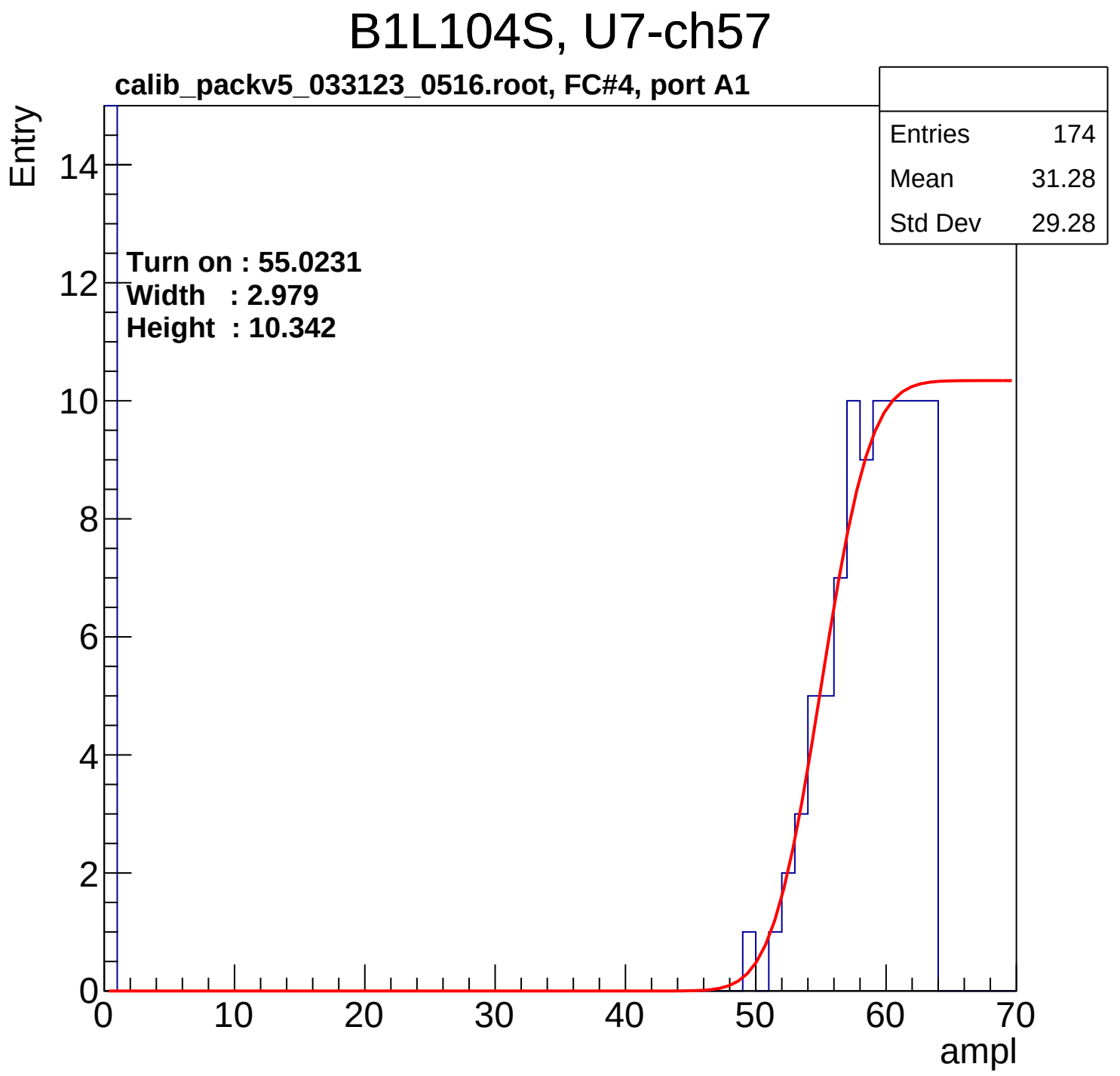

B1L104S, U7-ch52
calib_packv5_033123_0516.root, FC#4, port A1
Entries 175
Mean 38.91
Std Dev 26.6
Turn on : 52.1179
Width : 4.945
Height : 10.012
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

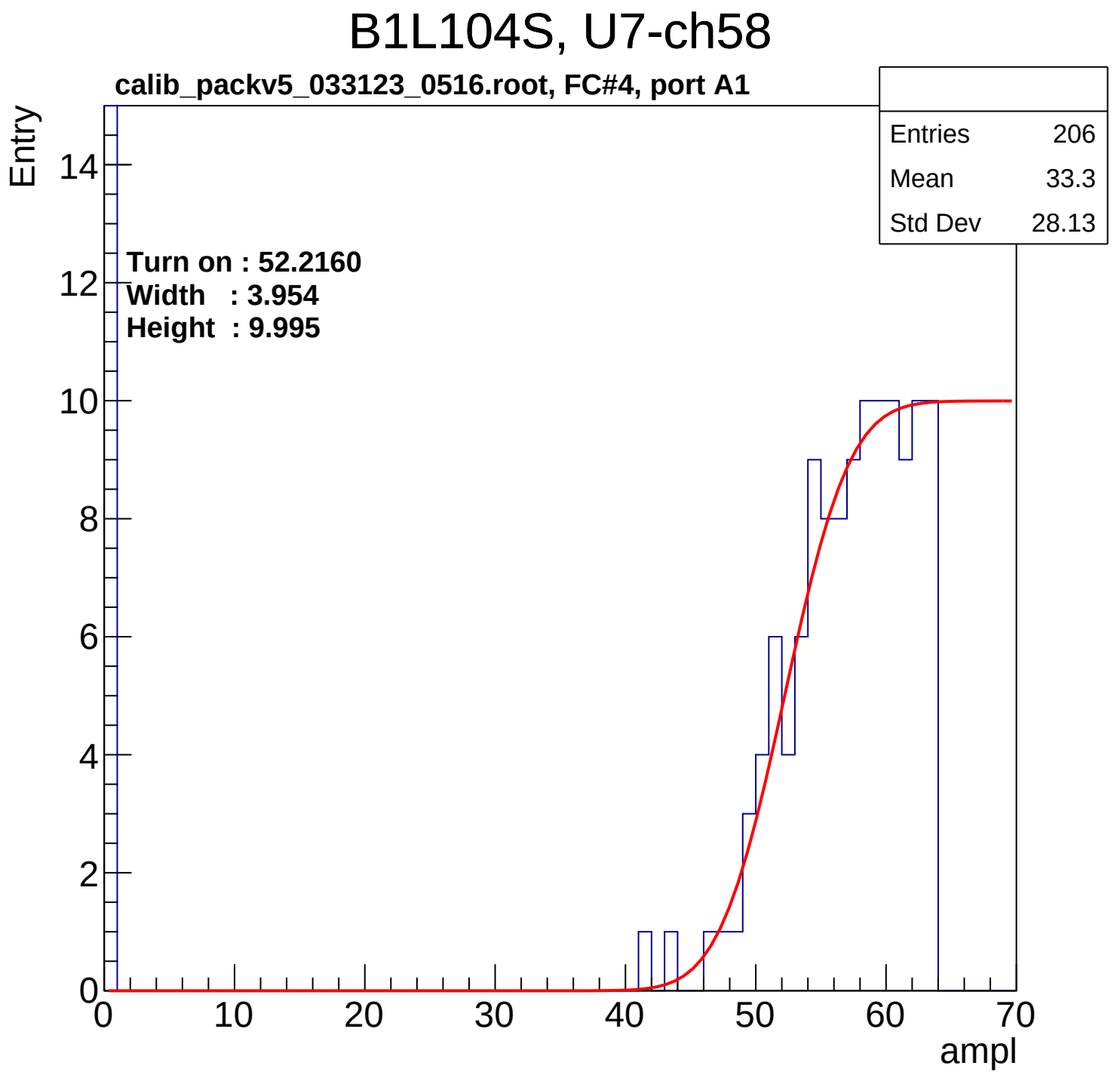

B1L104S, U7-ch53
calib_packv5_033123_0516.root, FC#4, port A1
Entries 173
Mean 31.69
Std Dev 29.16
Turn on : 55.0858
Width : 3.778
Height : 10.252
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

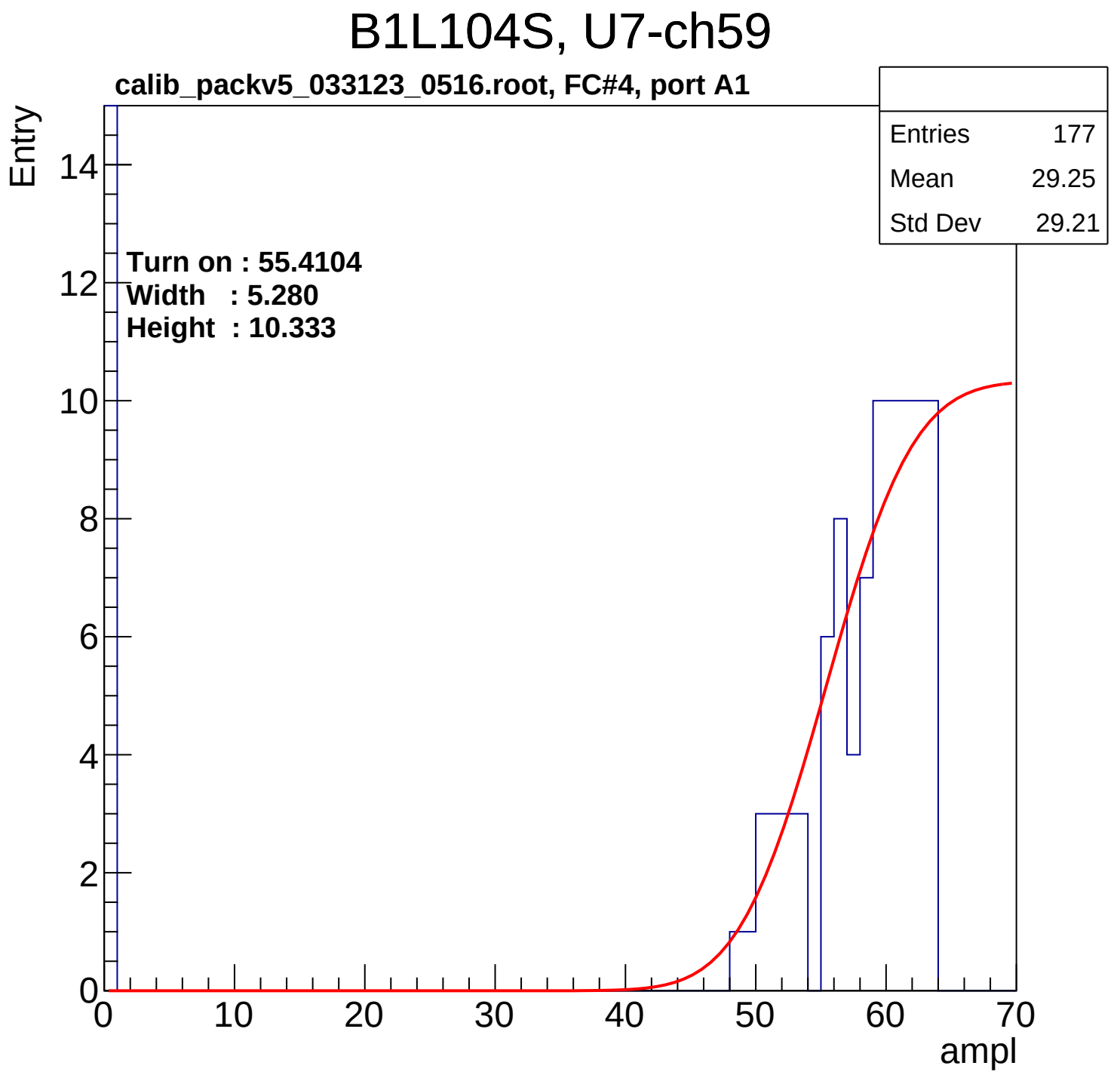

B1L104S, U7-ch54
calib_packv5_033123_0516.root, FC#4, port A1
Entries 244
Mean 32.35
Std Dev 28.08
Turn on : 51.3108
Width : 4.771
Height : 10.596
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

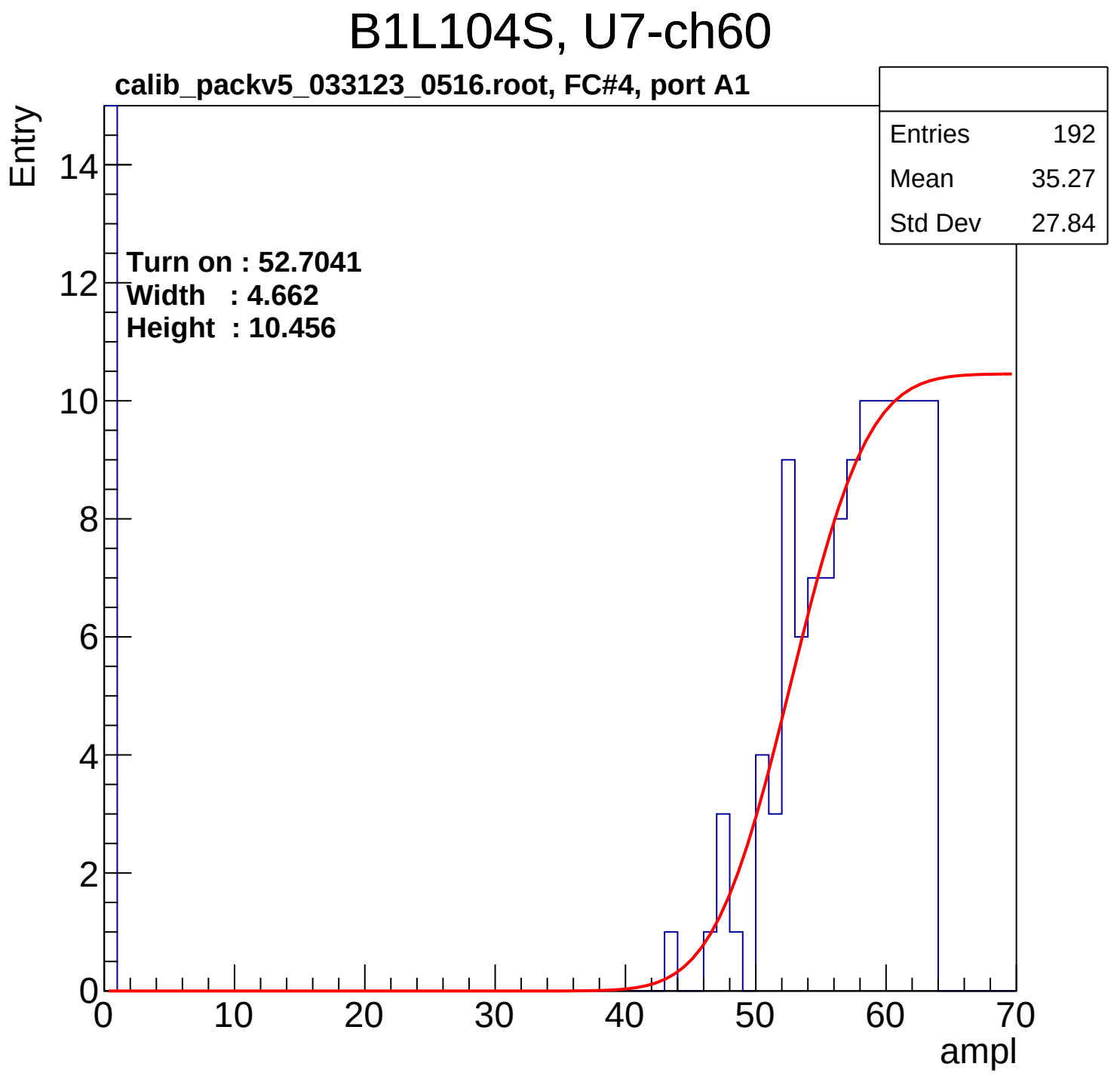

B1L104S, U7-ch55
calib_packv5_033123_0516.root, FC#4, port A1
Entries 182
Mean 32.53
Std Dev 28.93
Turn on : 53.8546
Width : 3.585
Height : 10.358
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

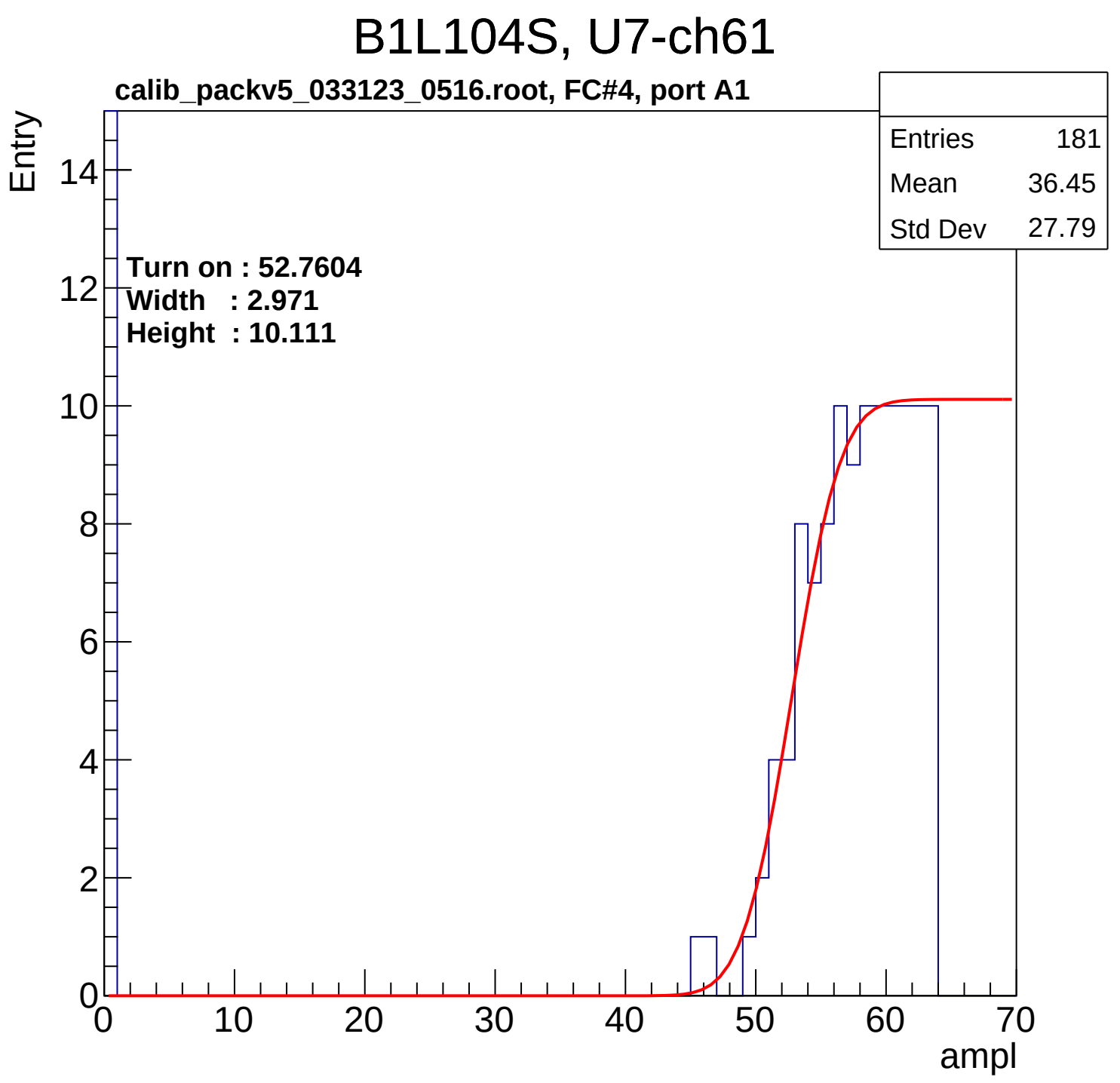

B1L104S, U7-ch56
calib_packv5_033123_0516.root, FC#4, port A1
Entries 185
Mean 34.34
Std Dev 28.23
Turn on : 53.6635
Width : 5.369
Height : 10.670
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

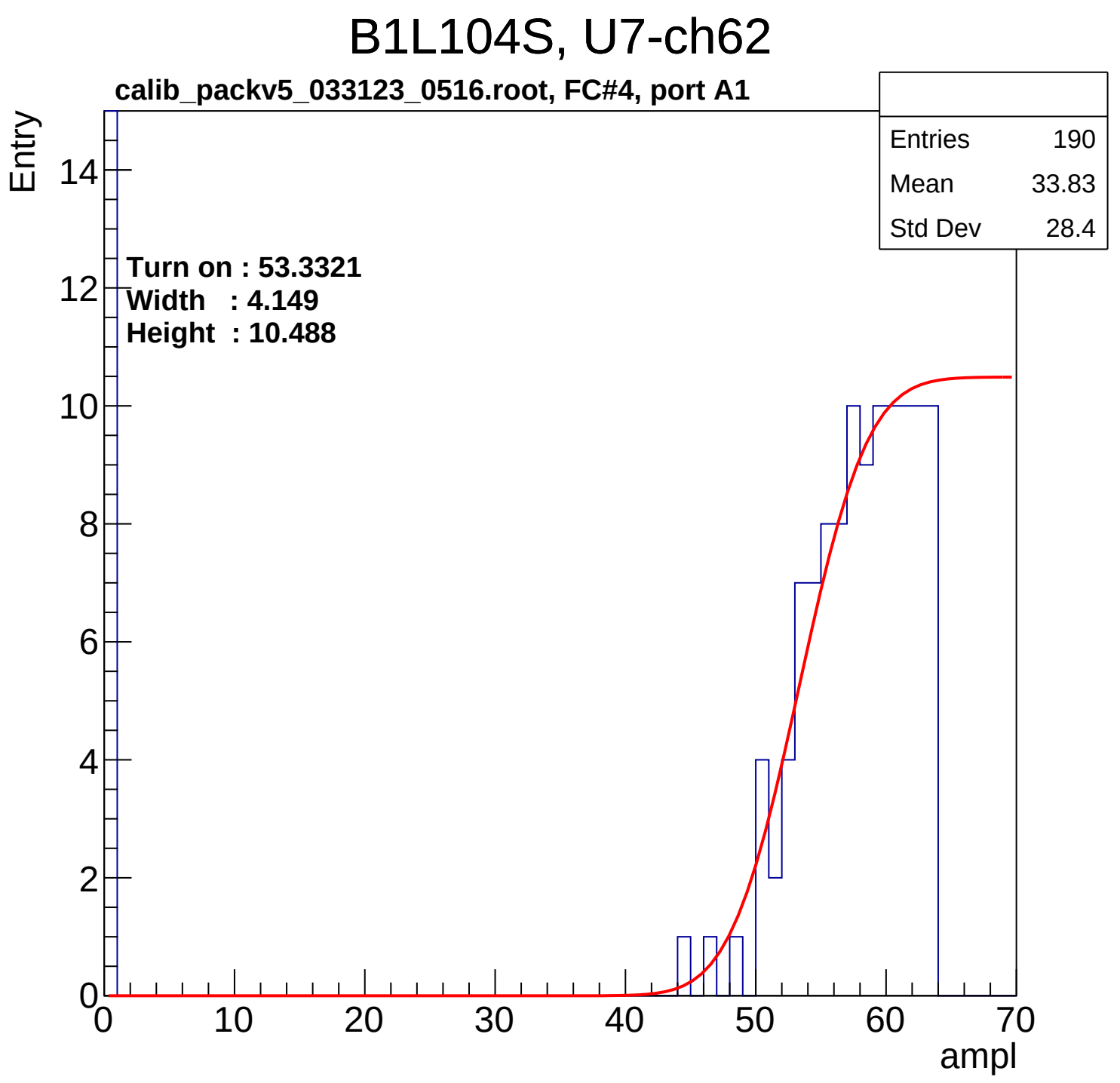

B1L104S, U7-ch57
calib_packv5_033123_0516.root, FC#4, port A1
Entries 174
Mean 31.28
Std Dev 29.28
Turn on : 55.0231
Width : 2.979
Height : 10.342
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

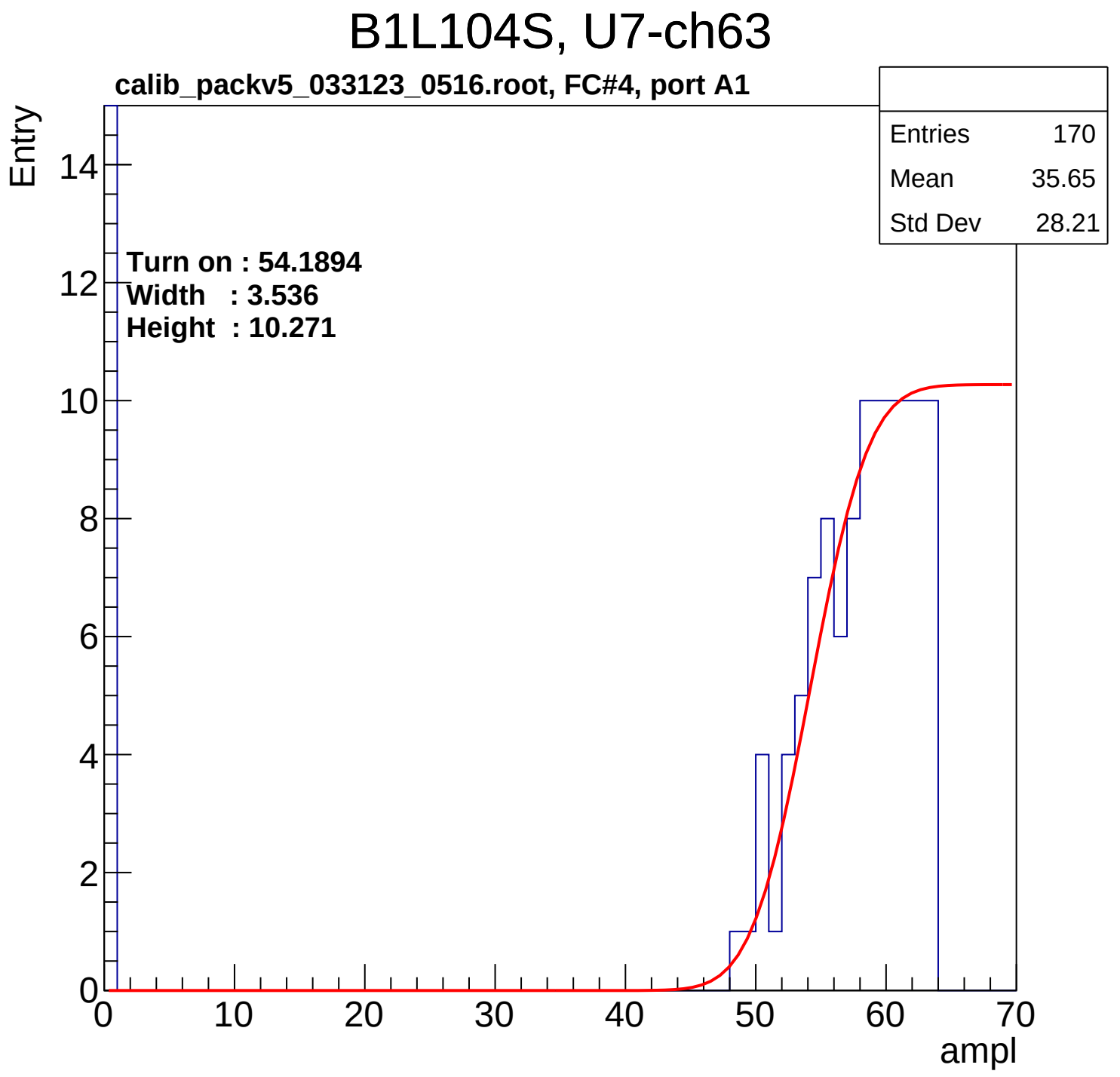

B1L104S, U7-ch58
calib_packv5_033123_0516.root, FC#4, port A1
Entries 206
Mean 33.3
Std Dev 28.13
Turn on : 52.2160
Width : 3.954
Height : 9.995
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

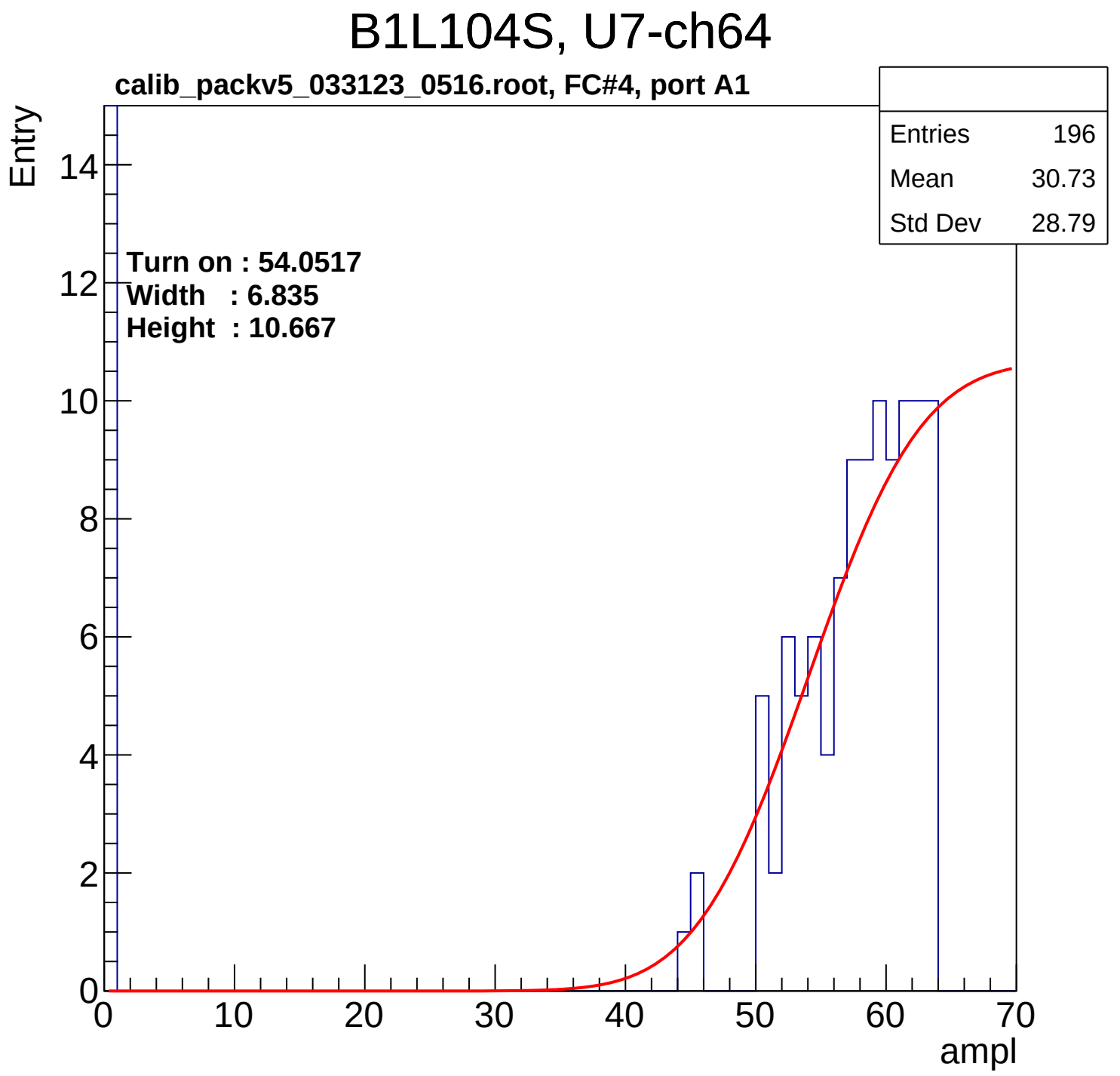

B1L104S, U7-ch59
calib_packv5_033123_0516.root, FC#4, port A1
Entries 177
Mean 29.25
Std Dev 29.21
Turn on : 55.4104
Width : 5.280
Height : 10.333
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

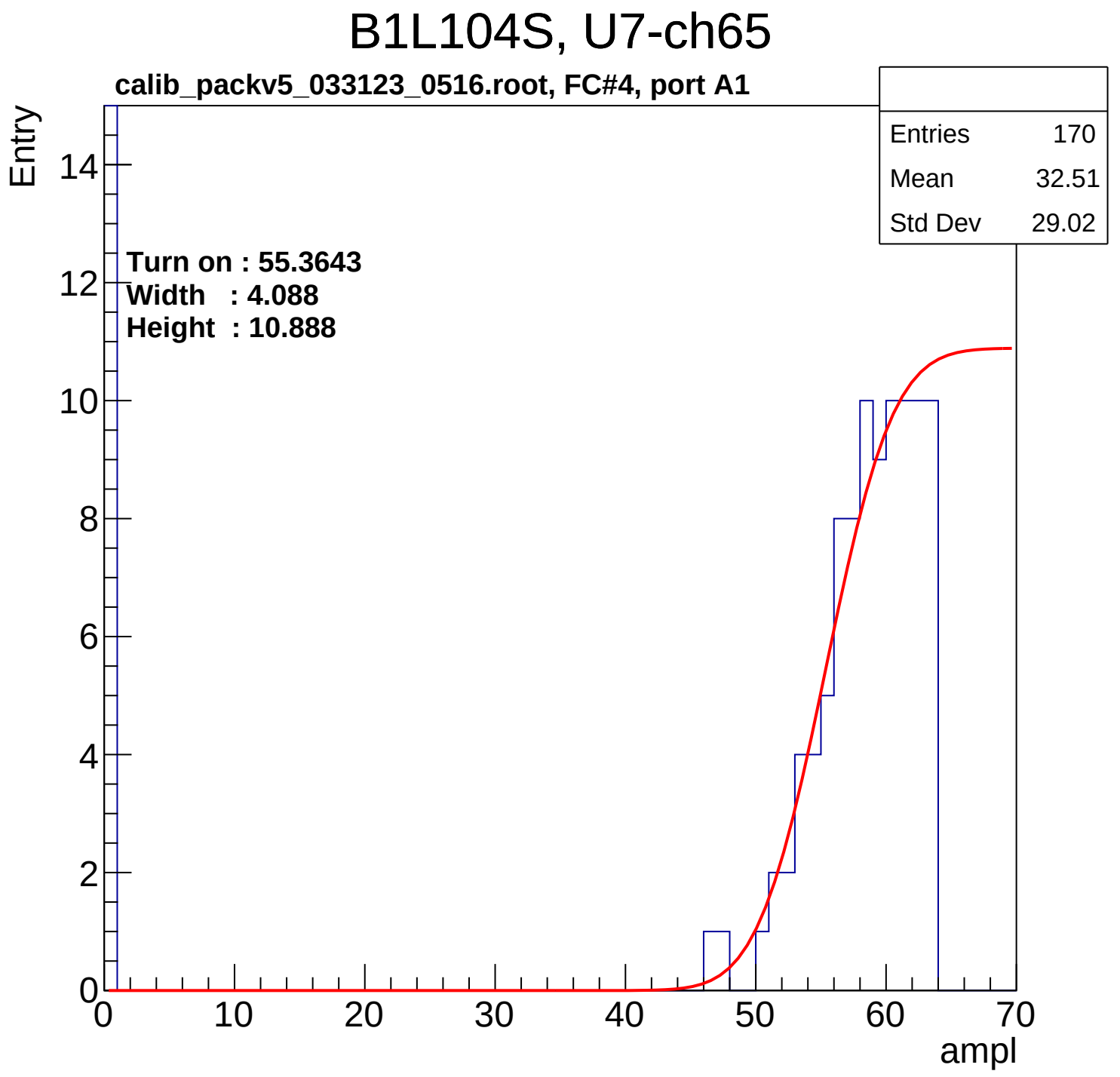

B1L104S, U7-ch60
calib_packv5_033123_0516.root, FC#4, port A1
Entries 192
Mean 35.27
Std Dev 27.84
Turn on : 52.7041
Width : 4.662
Height : 10.456
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

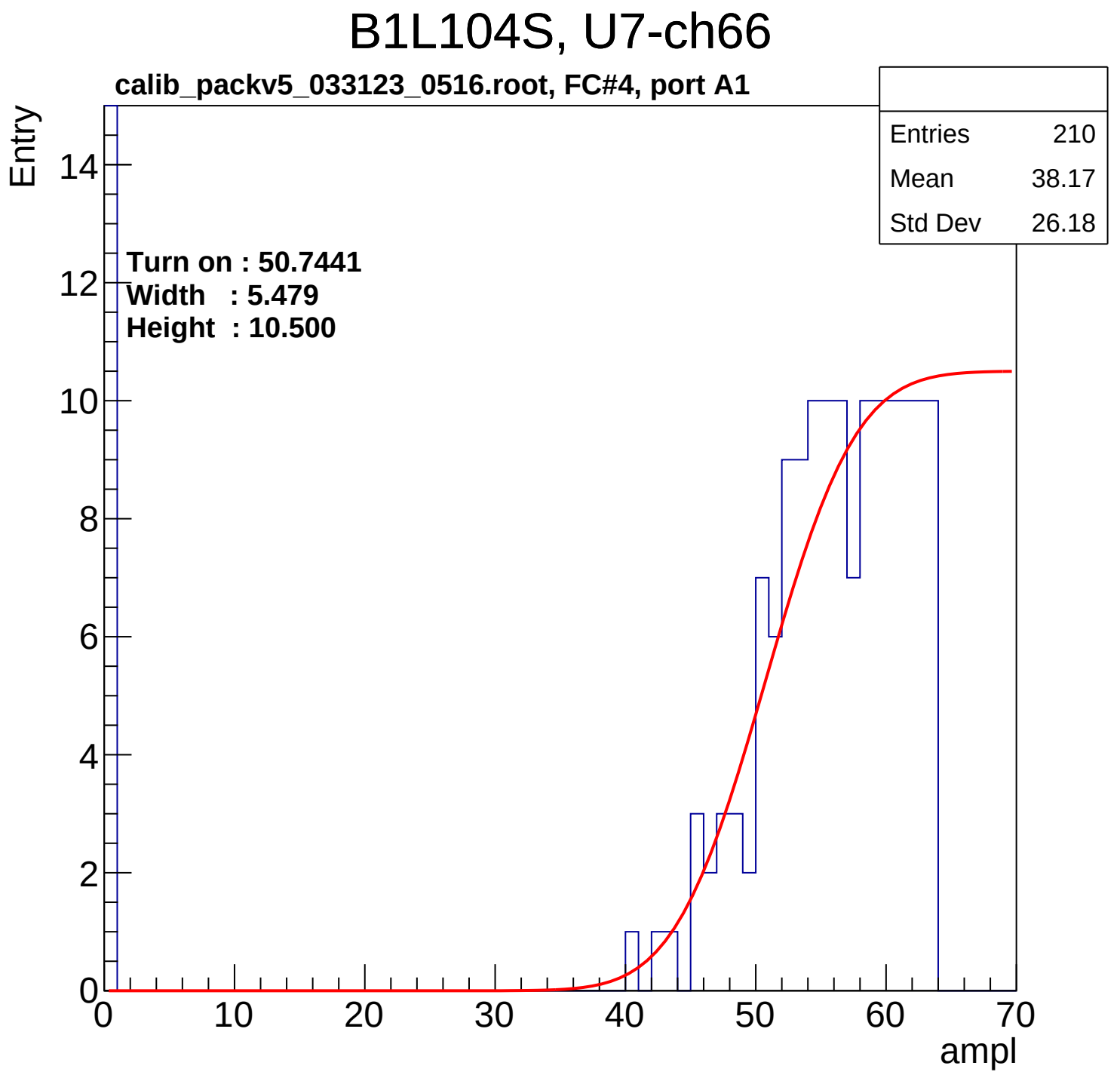

B1L104S, U7-ch61
calib_packv5_033123_0516.root, FC#4, port A1
Entries 181
Mean 36.45
Std Dev 27.79
Turn on : 52.7604
Width : 2.971
Height : 10.111
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

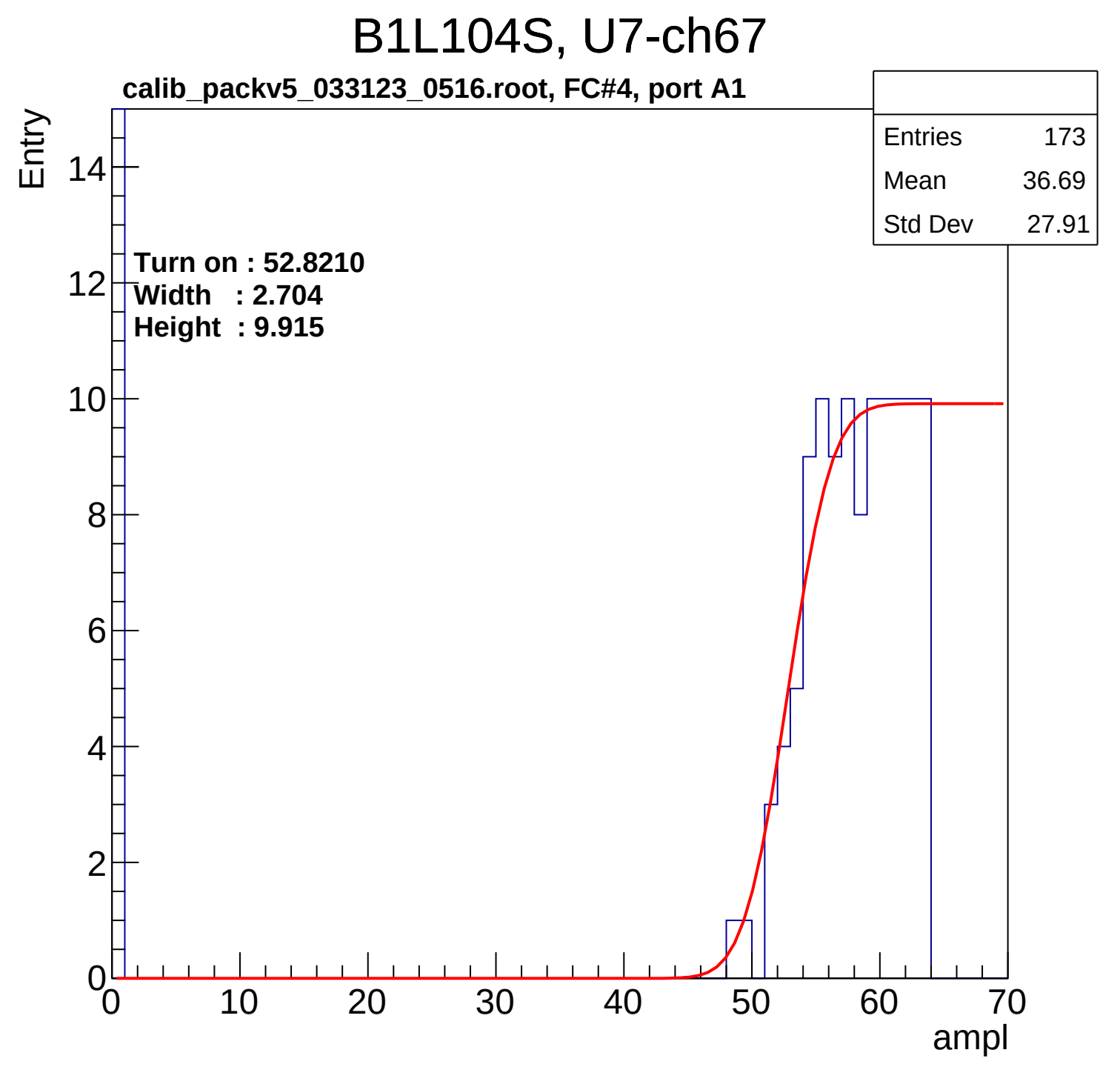

B1L104S, U7-ch62
calib_packv5_033123_0516.root, FC#4, port A1
Entries 190
Mean 33.83
Std Dev 28.4
Turn on : 53.3321
Width : 4.149
Height : 10.488
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

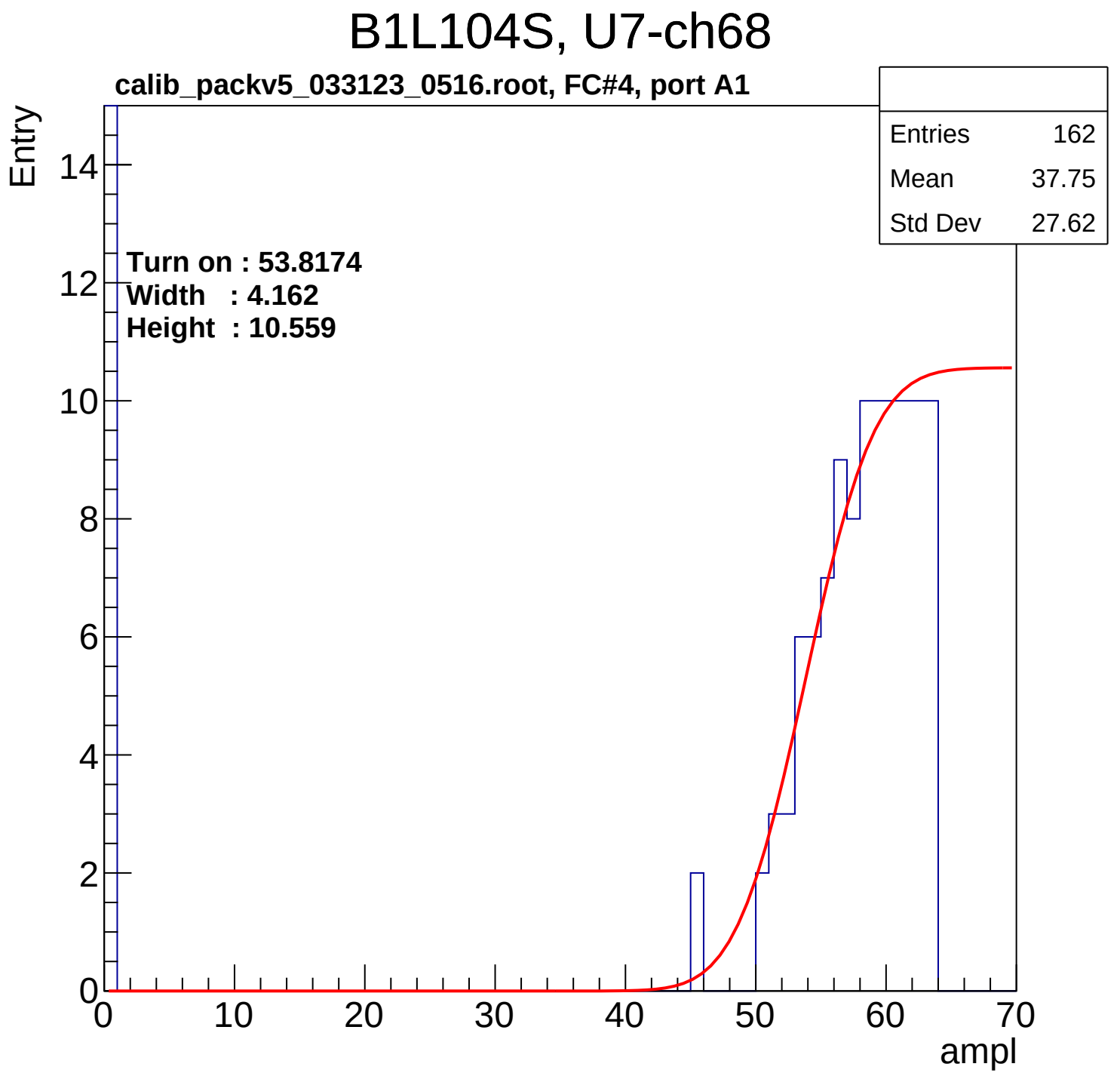

B1L104S, U7-ch63
calib_packv5_033123_0516.root, FC#4, port A1
Entries 170
Mean 35.65
Std Dev 28.21
Turn on : 54.1894
Width : 3.536
Height : 10.271
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

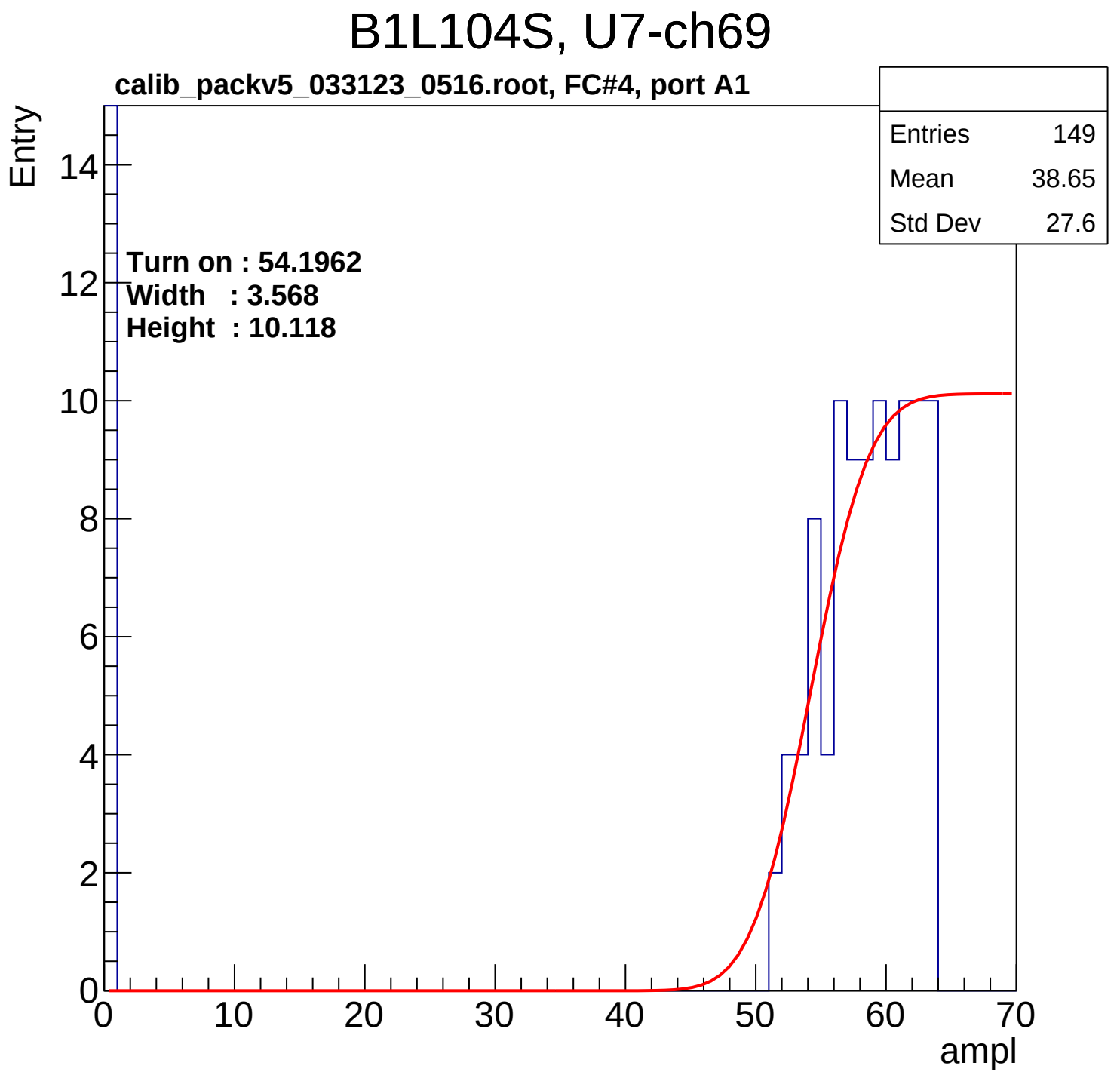

B1L104S, U7-ch64
calib_packv5_033123_0516.root, FC#4, port A1
Entries 196
Mean 30.73
Std Dev 28.79
Turn on : 54.0517
Width : 6.835
Height : 10.667
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

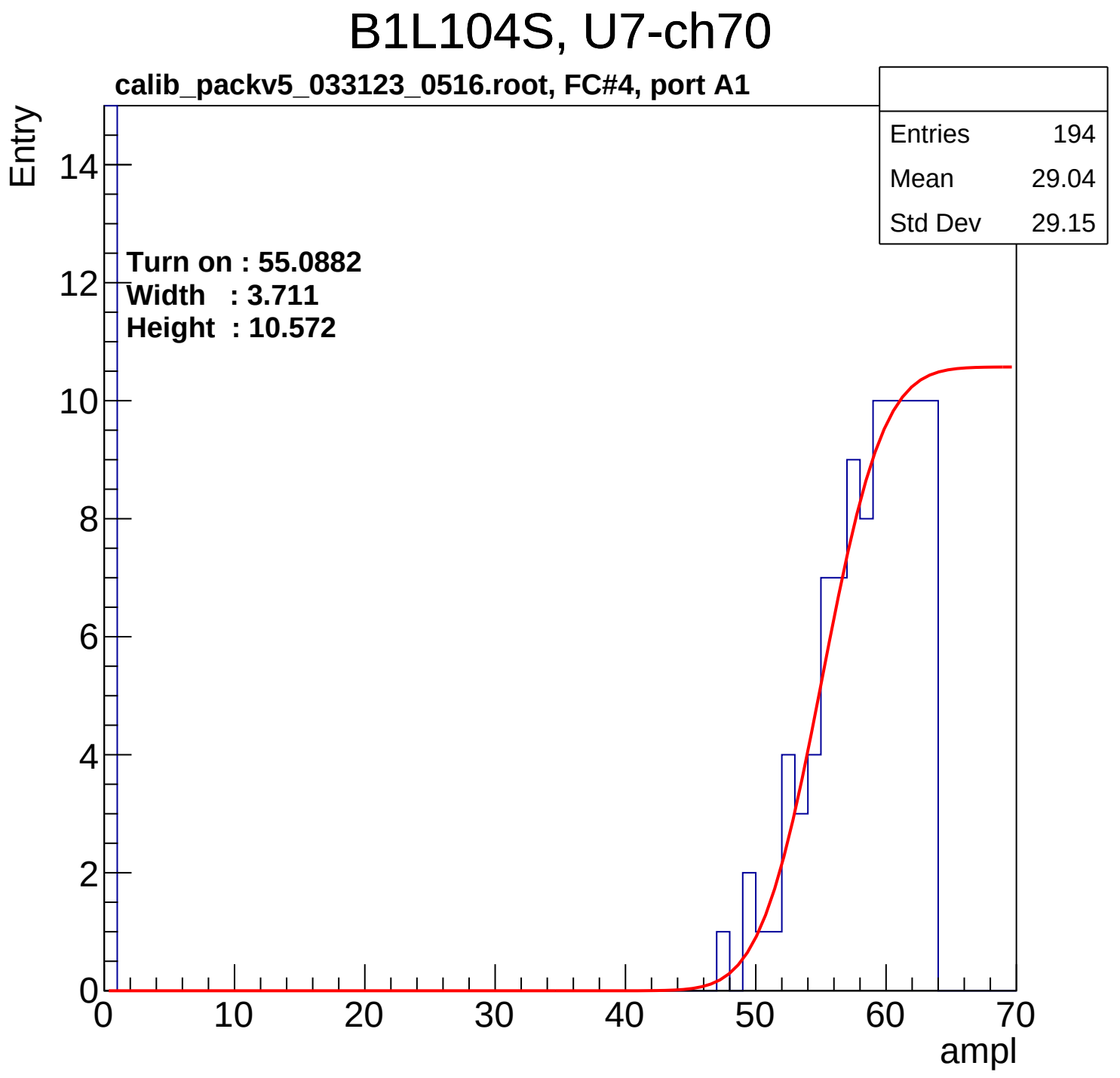

B1L104S, U7-ch65
calib_packv5_033123_0516.root, FC#4, port A1
Entries 170
Mean 32.51
Std Dev 29.02
Turn on : 55.3643
Width : 4.088
Height : 10.888
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

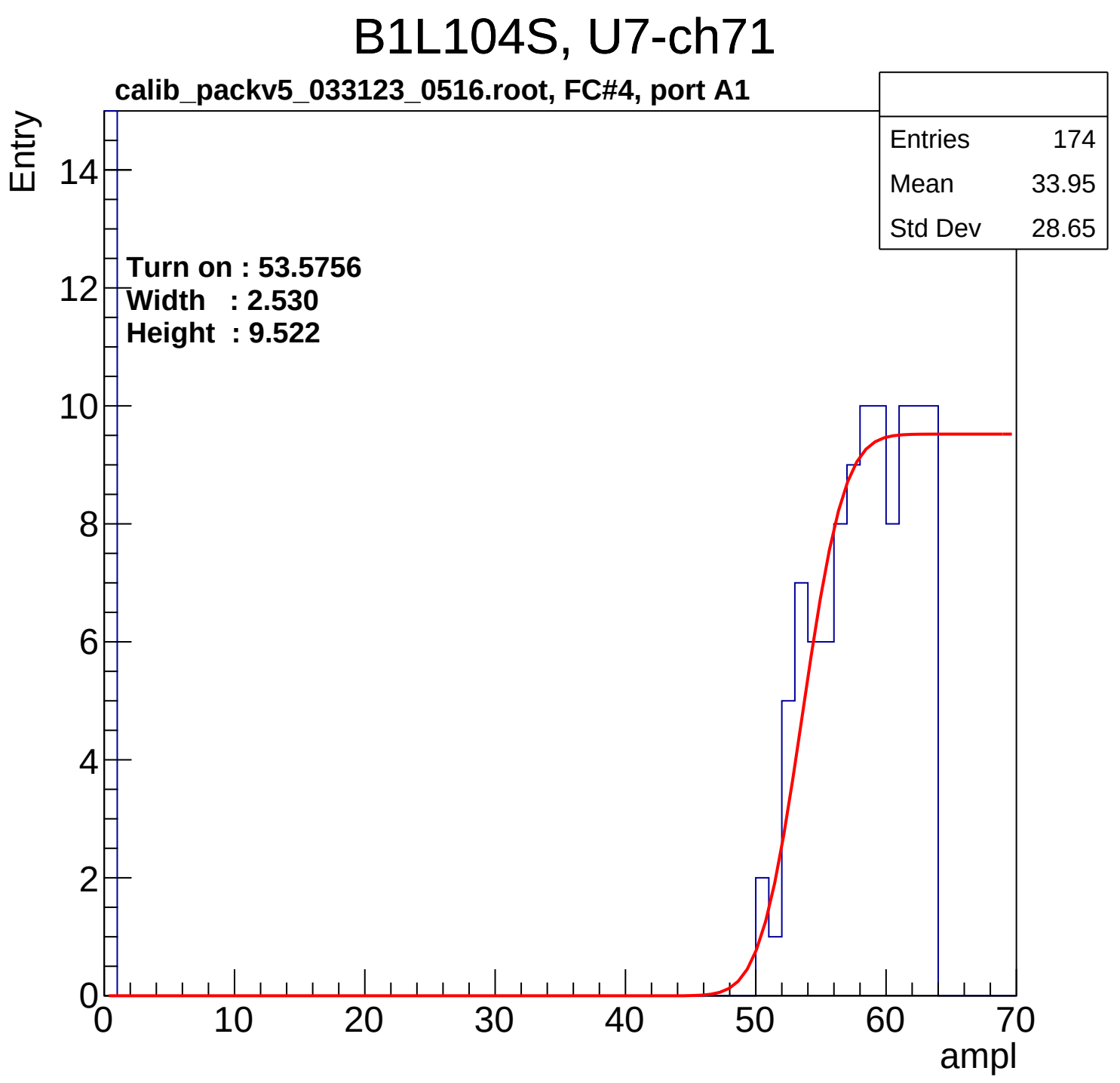

B1L104S, U7-ch66
calib_packv5_033123_0516.root, FC#4, port A1
Entries 210
Mean 38.17
Std Dev 26.18
Turn on : 50.7441
Width : 5.479
Height : 10.500
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

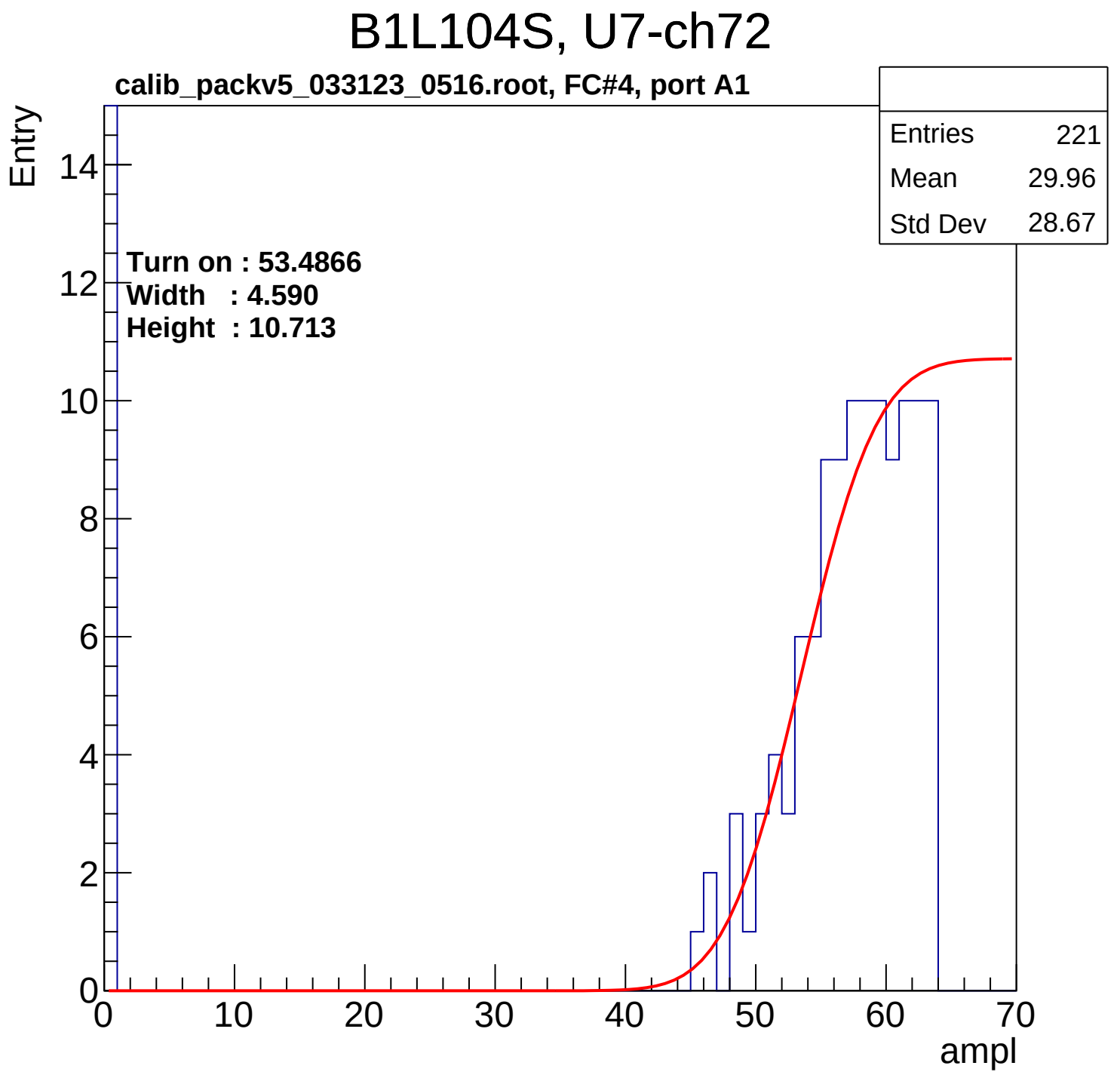

B1L104S, U7-ch67
calib_packv5_033123_0516.root, FC#4, port A1
Entries 173
Mean 36.69
Std Dev 27.91
Turn on : 52.8210
Width : 2.704
Height : 9.915
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

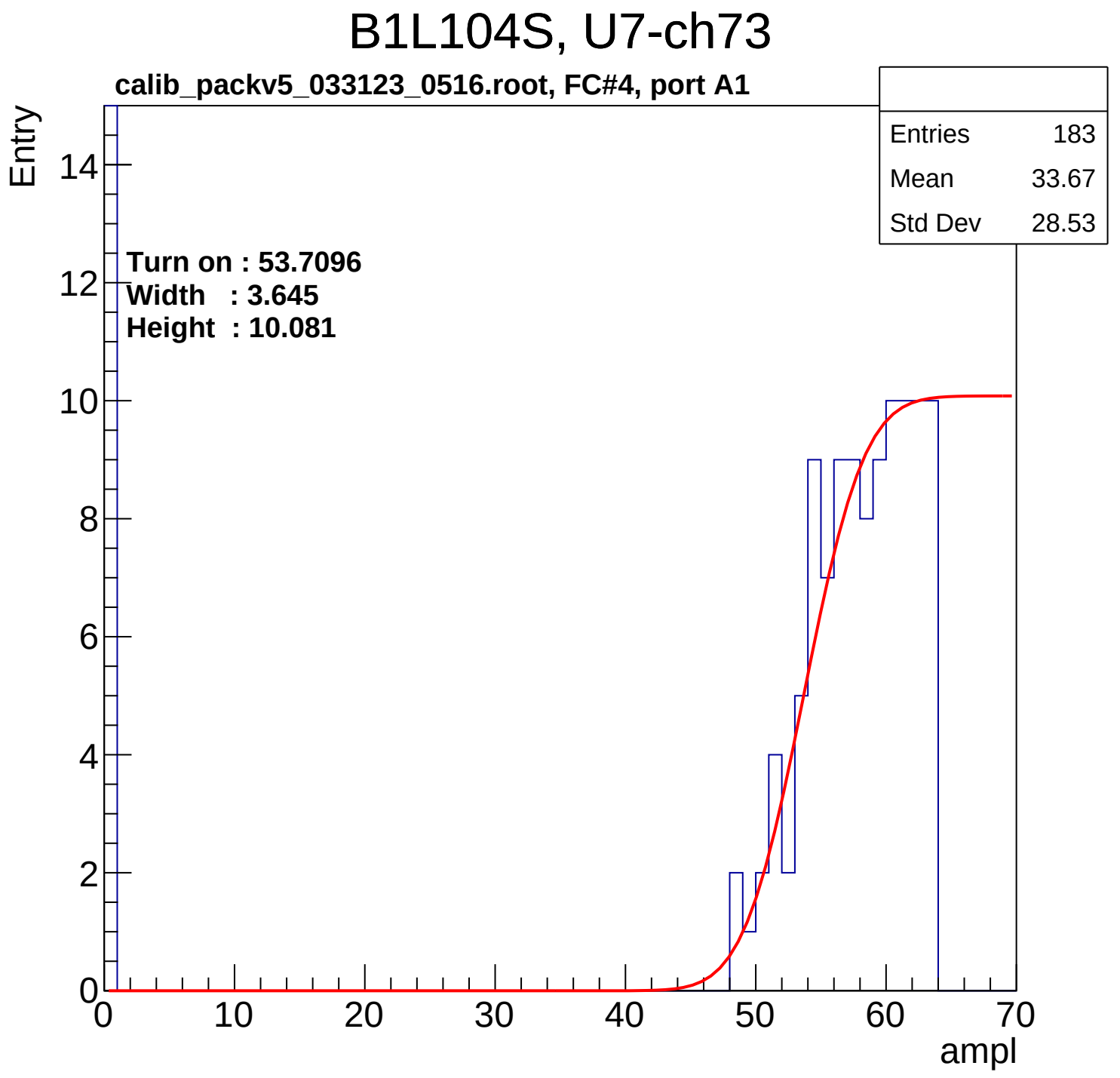

B1L104S, U7-ch68
calib_packv5_033123_0516.root, FC#4, port A1
Entries 162
Mean 37.75
Std Dev 27.62
Turn on : 53.8174
Width : 4.162
Height : 10.559
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

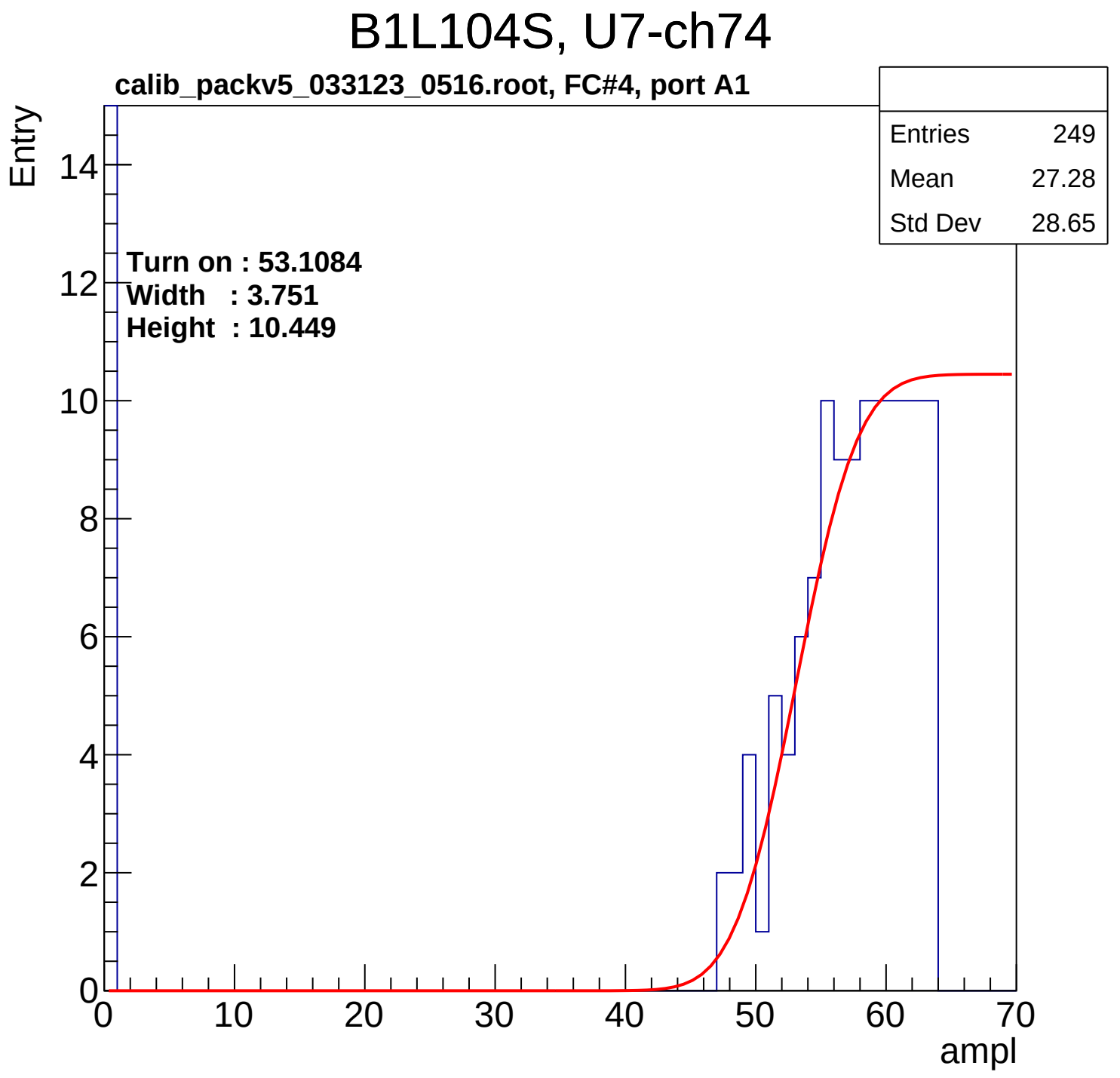

B1L104S, U7-ch69
calib_packv5_033123_0516.root, FC#4, port A1
Entries 149
Mean 38.65
Std Dev 27.6
Turn on : 54.1962
Width : 3.568
Height : 10.118
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

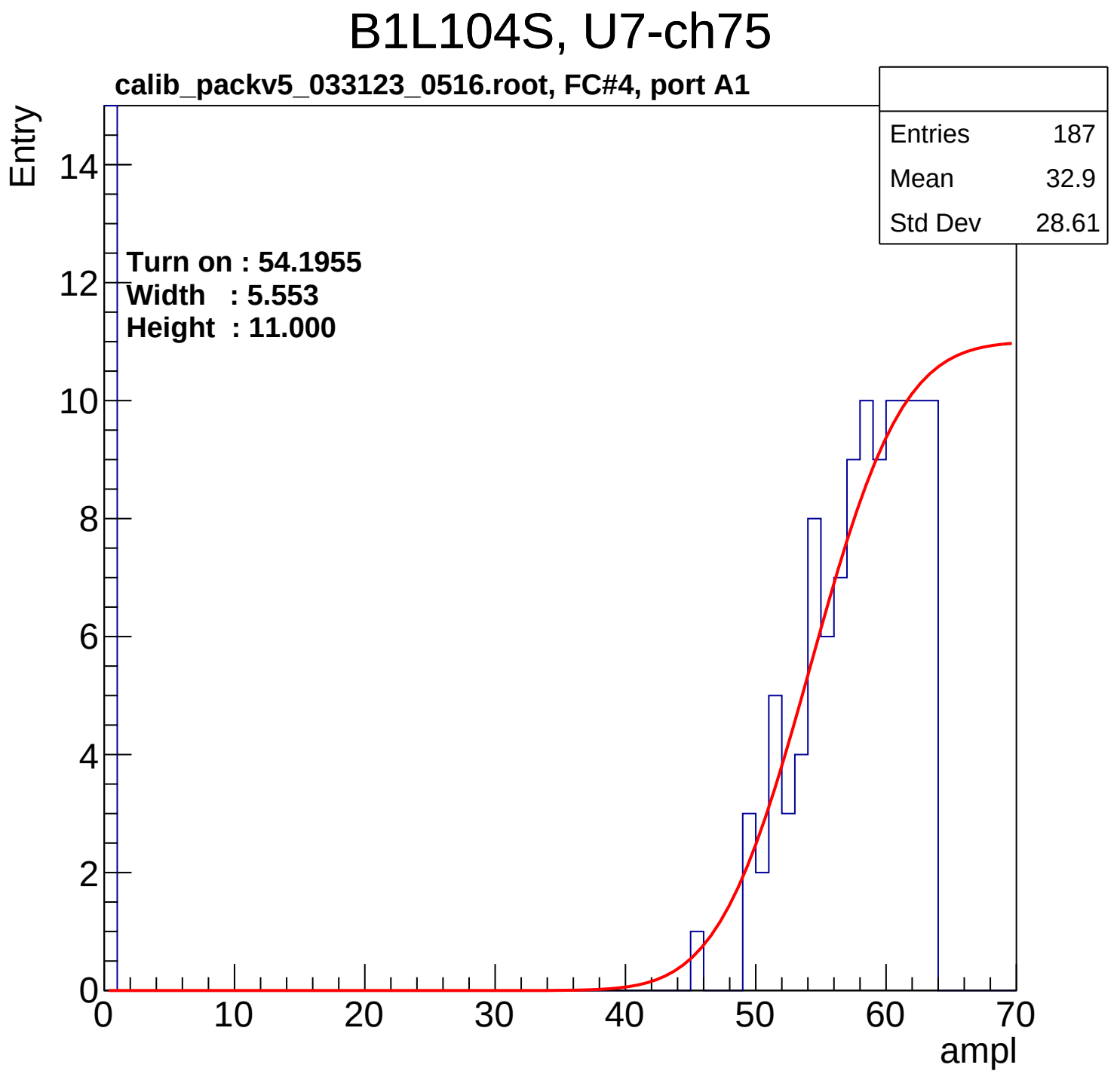

B1L104S, U7-ch70
calib_packv5_033123_0516.root, FC#4, port A1
Entries 194
Mean 29.04
Std Dev 29.15
Turn on : 55.0882
Width : 3.711
Height : 10.572
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

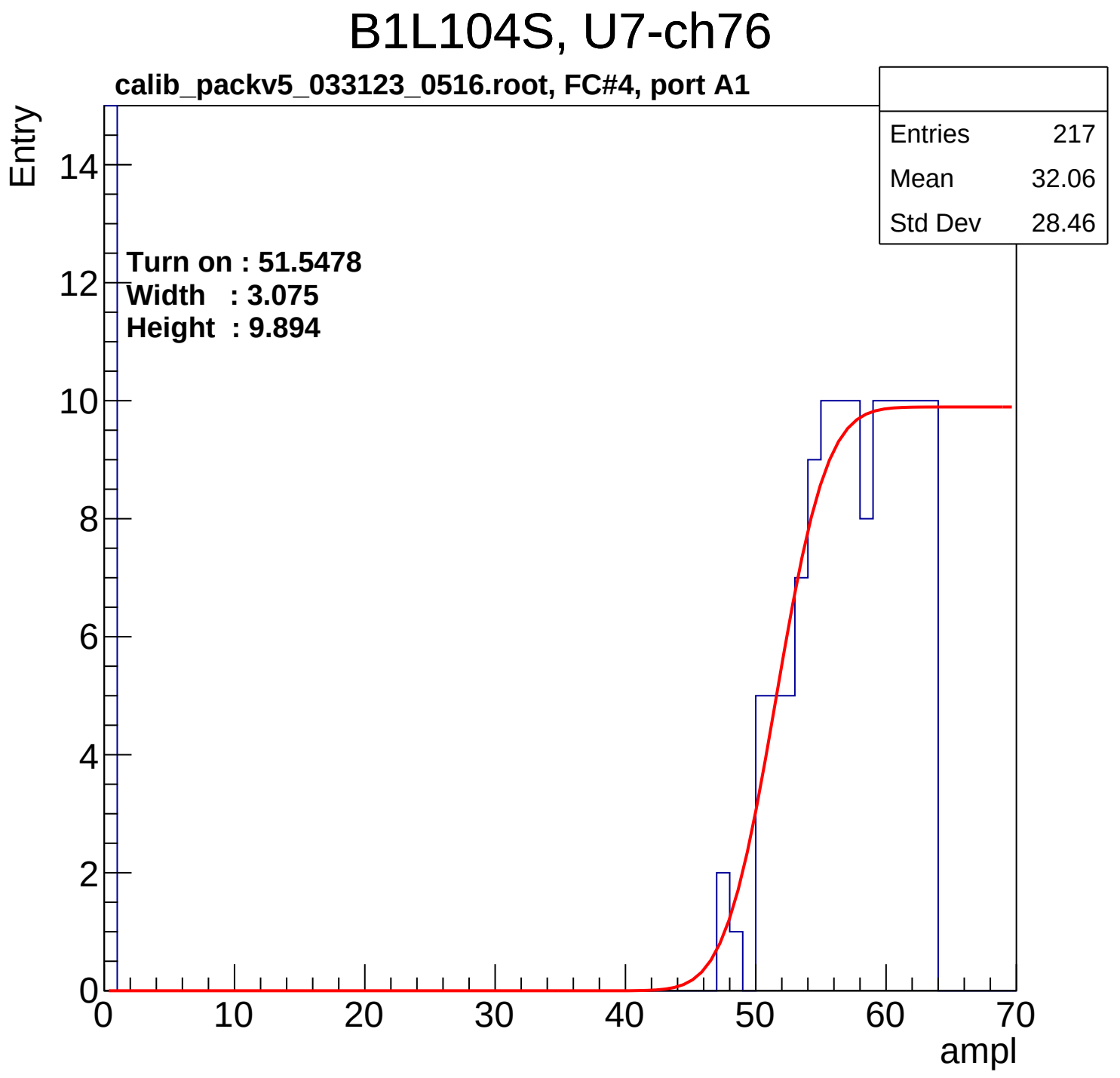

B1L104S, U7-ch71
calib_packv5_033123_0516.root, FC#4, port A1
Entries 174
Mean 33.95
Std Dev 28.65
Turn on : 53.5756
Width : 2.530
Height : 9.522
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

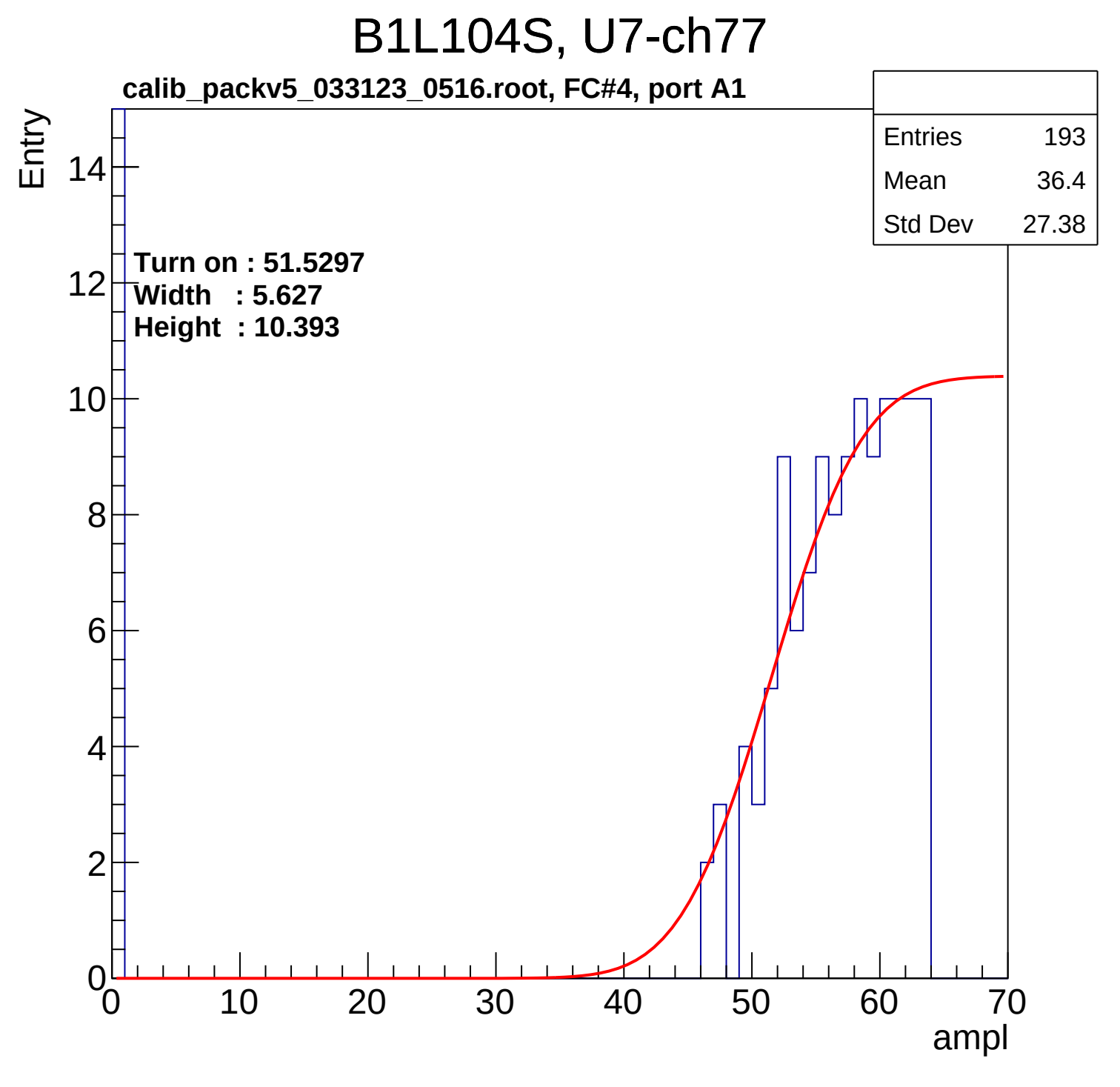

B1L104S, U7-ch72
calib_packv5_033123_0516.root, FC#4, port A1
Entries 221
Mean 29.96
Std Dev 28.67
Turn on : 53.4866
Width : 4.590
Height : 10.713
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

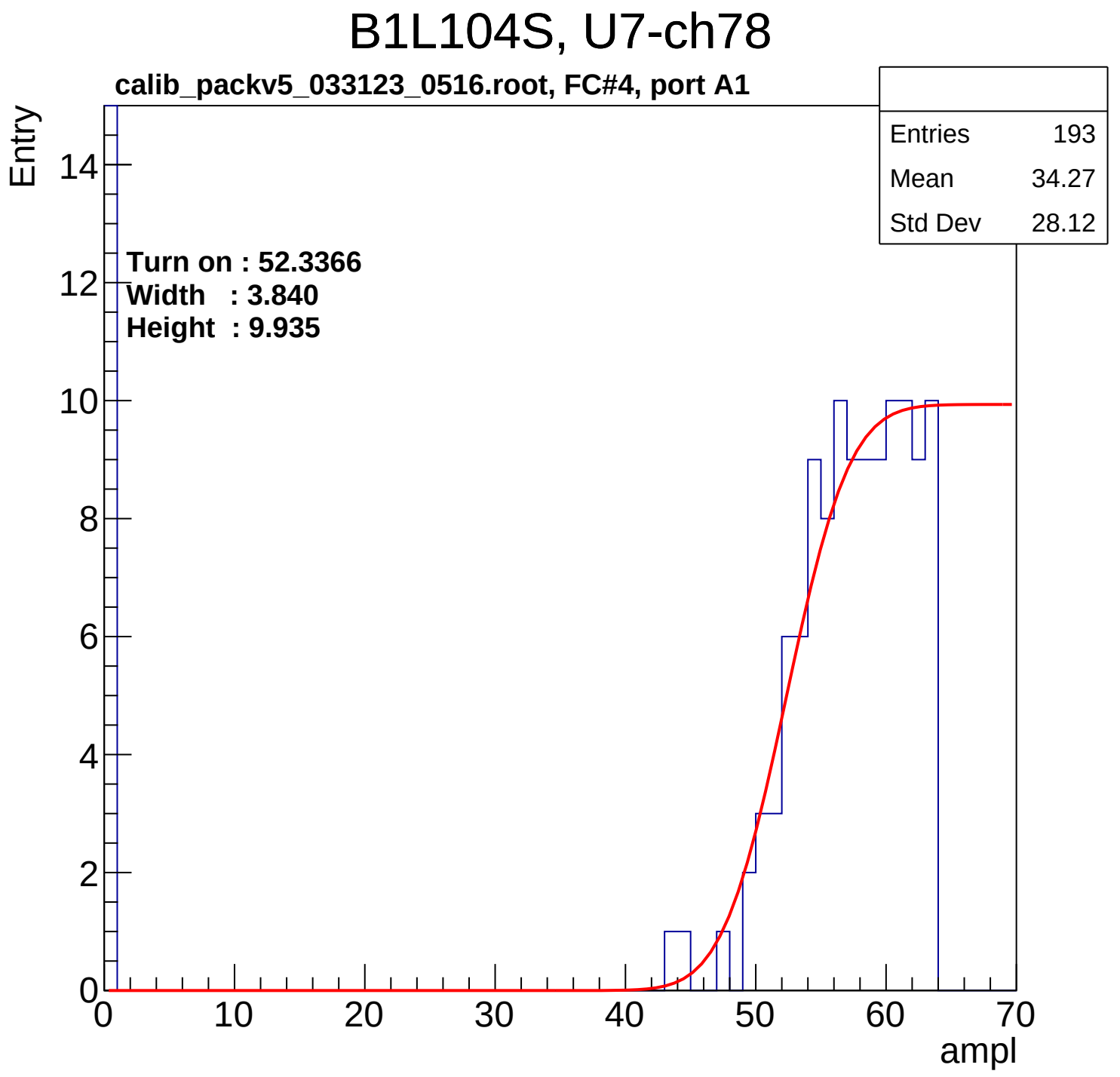

B1L104S, U7-ch73
calib_packv5_033123_0516.root, FC#4, port A1
Entries 183
Mean 33.67
Std Dev 28.53
Turn on : 53.7096
Width : 3.645
Height : 10.081
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

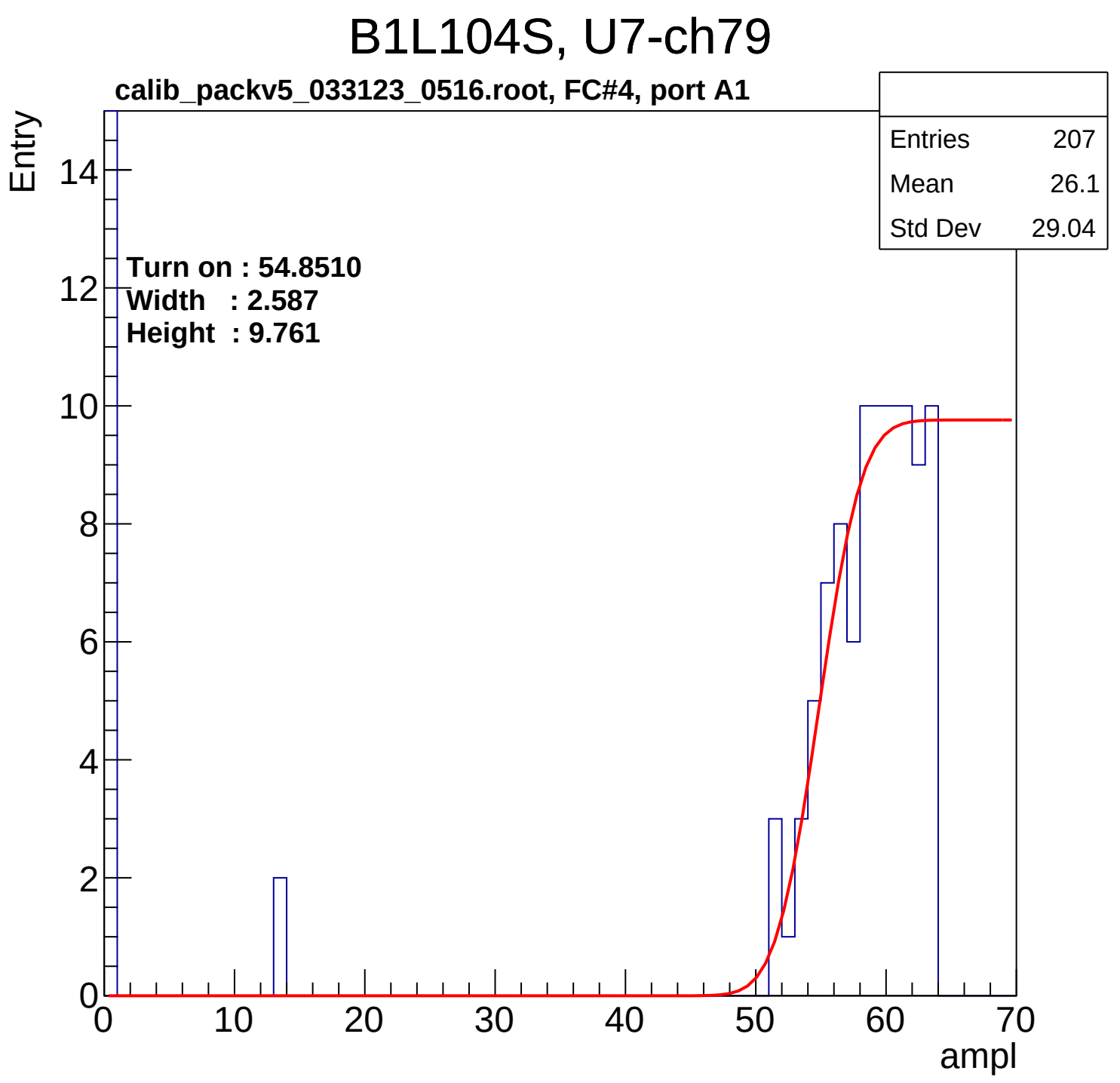

B1L104S, U7-ch74
calib_packv5_033123_0516.root, FC#4, port A1
Entries 249
Mean 27.28
Std Dev 28.65
Turn on : 53.1084
Width : 3.751
Height : 10.449
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

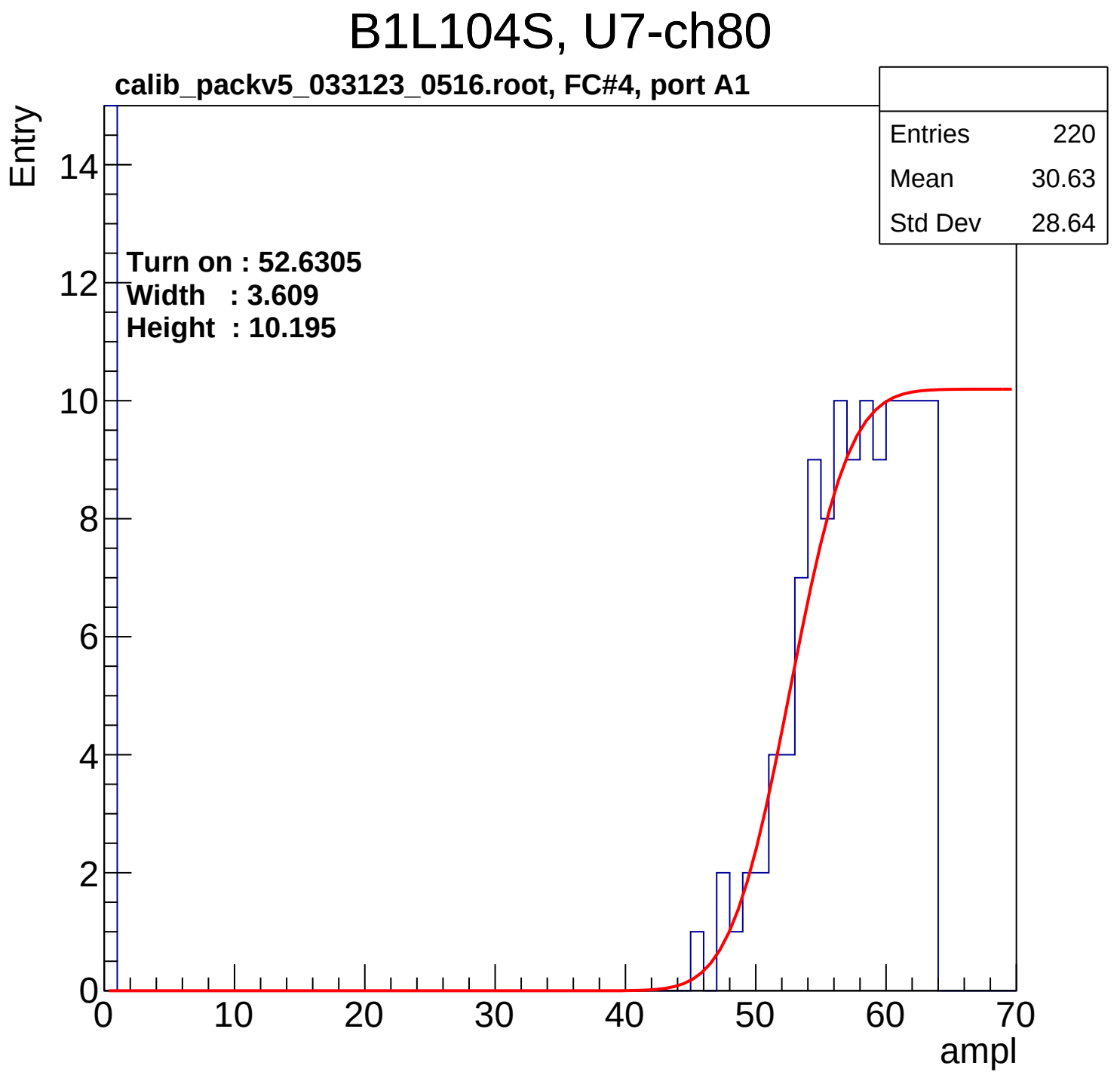

B1L104S, U7-ch75
calib_packv5_033123_0516.root, FC#4, port A1
Entries 187
Mean 32.9
Std Dev 28.61
Turn on : 54.1955
Width : 5.553
Height : 11.000
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

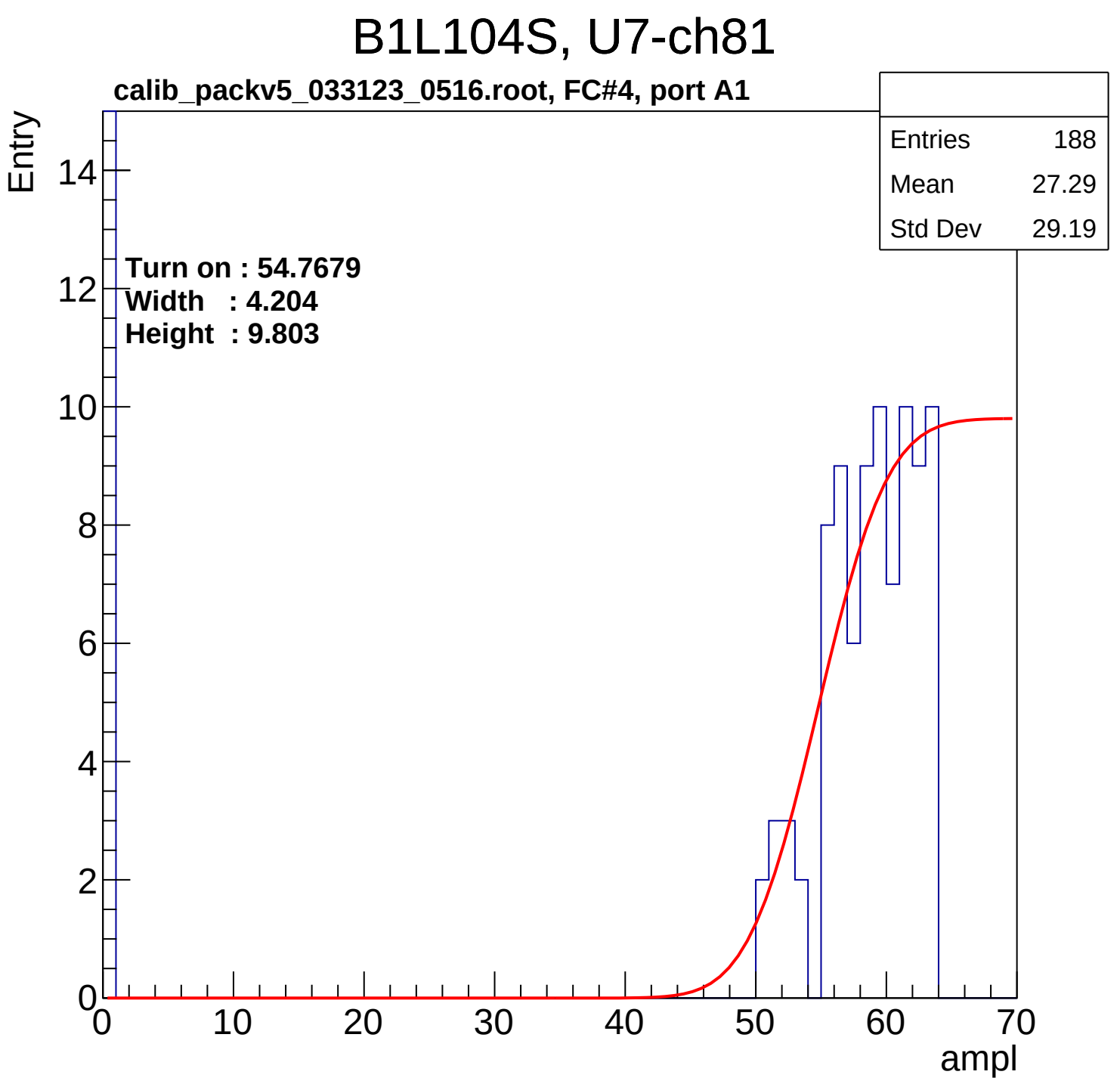

B1L104S, U7-ch76
calib_packv5_033123_0516.root, FC#4, port A1
Entries 217
Mean 32.06
Std Dev 28.46
Turn on : 51.5478
Width : 3.075
Height : 9.894
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

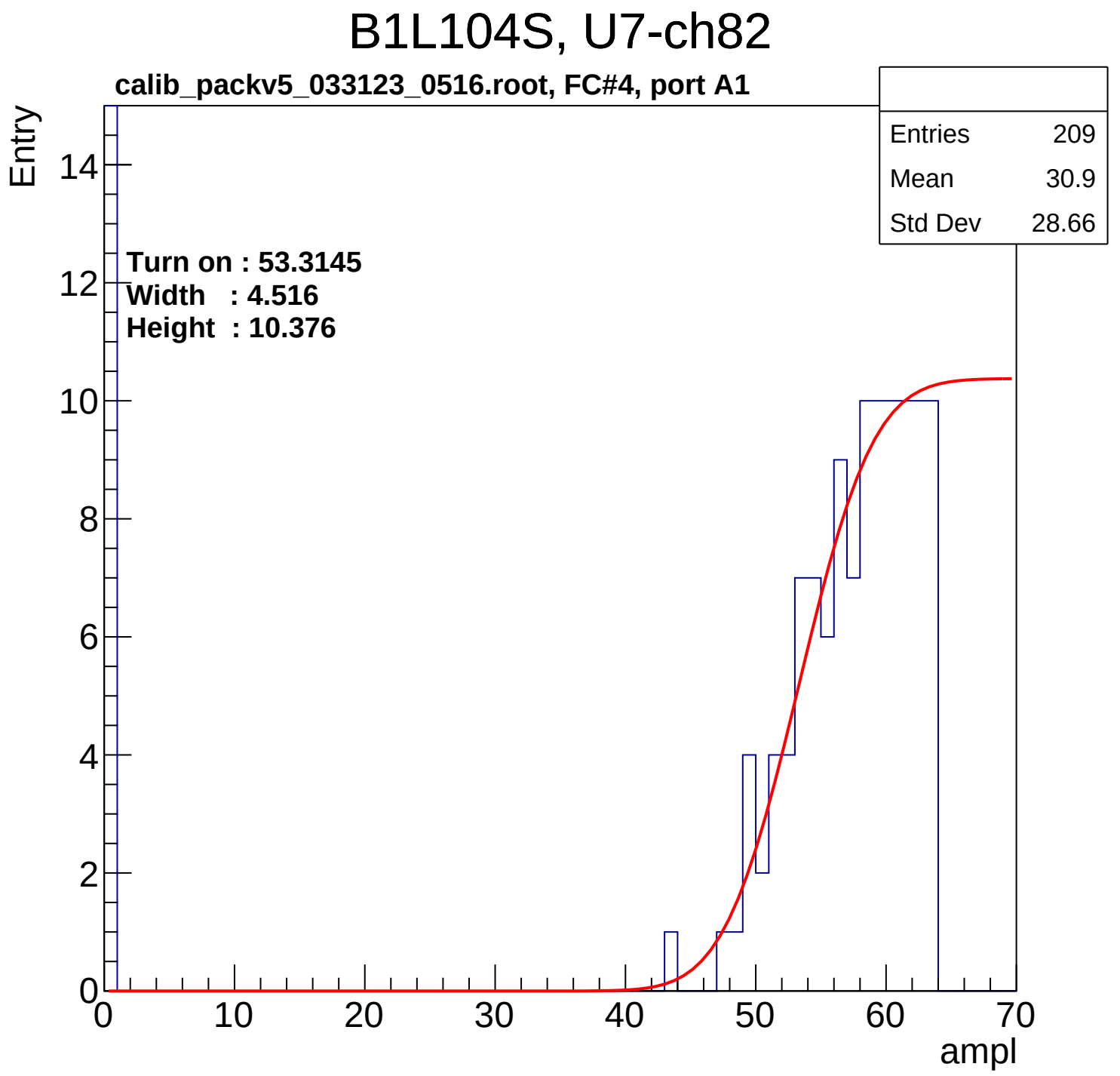

B1L104S, U7-ch77
calib_packv5_033123_0516.root, FC#4, port A1
Entries 193
Mean 36.4
Std Dev 27.38
Turn on : 51.5297
Width : 5.627
Height : 10.393
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

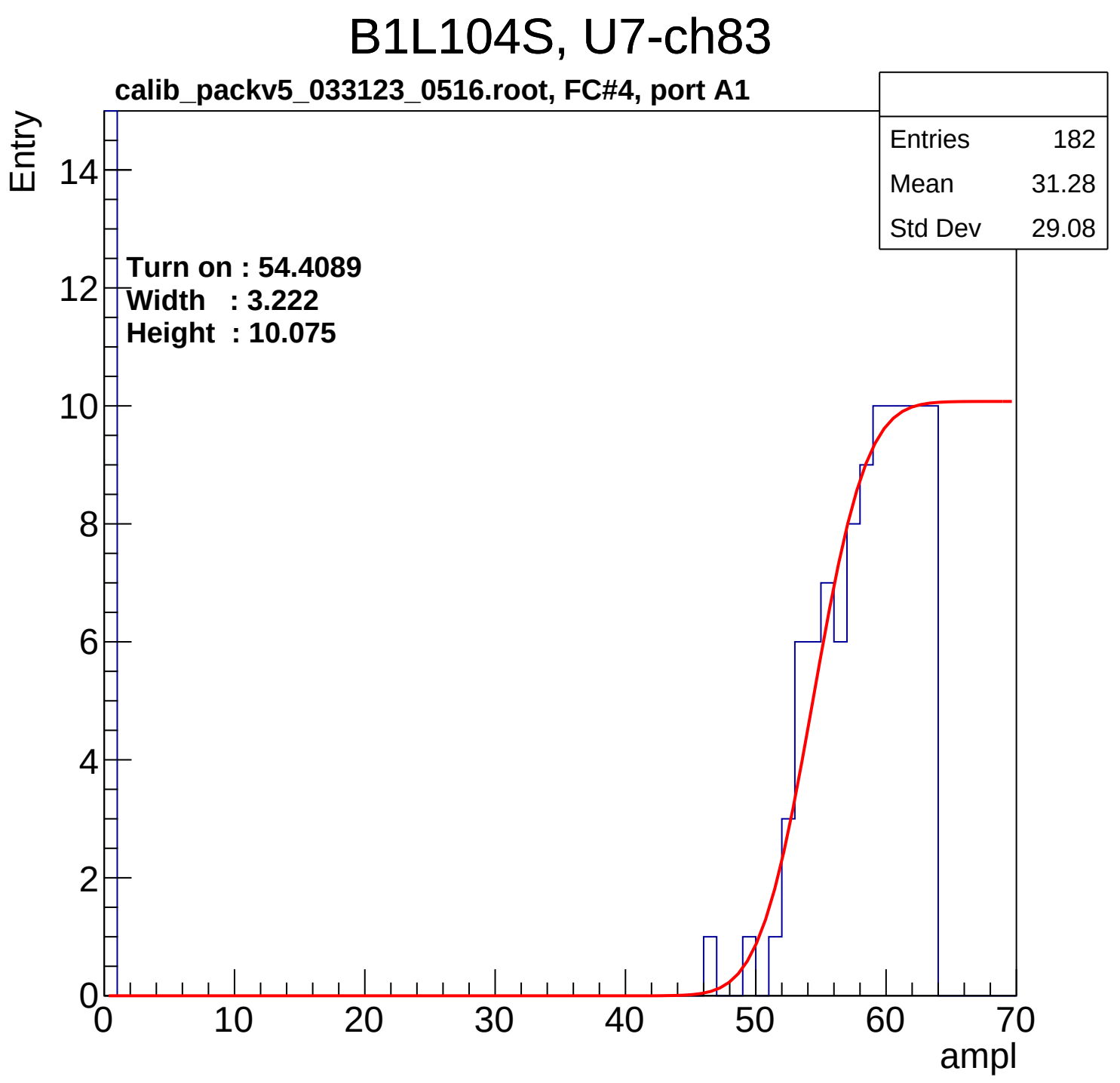

B1L104S, U7-ch78
calib_packv5_033123_0516.root, FC#4, port A1
Entries 193
Mean 34.27
Std Dev 28.12
Turn on : 52.3366
Width : 3.840
Height : 9.935
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

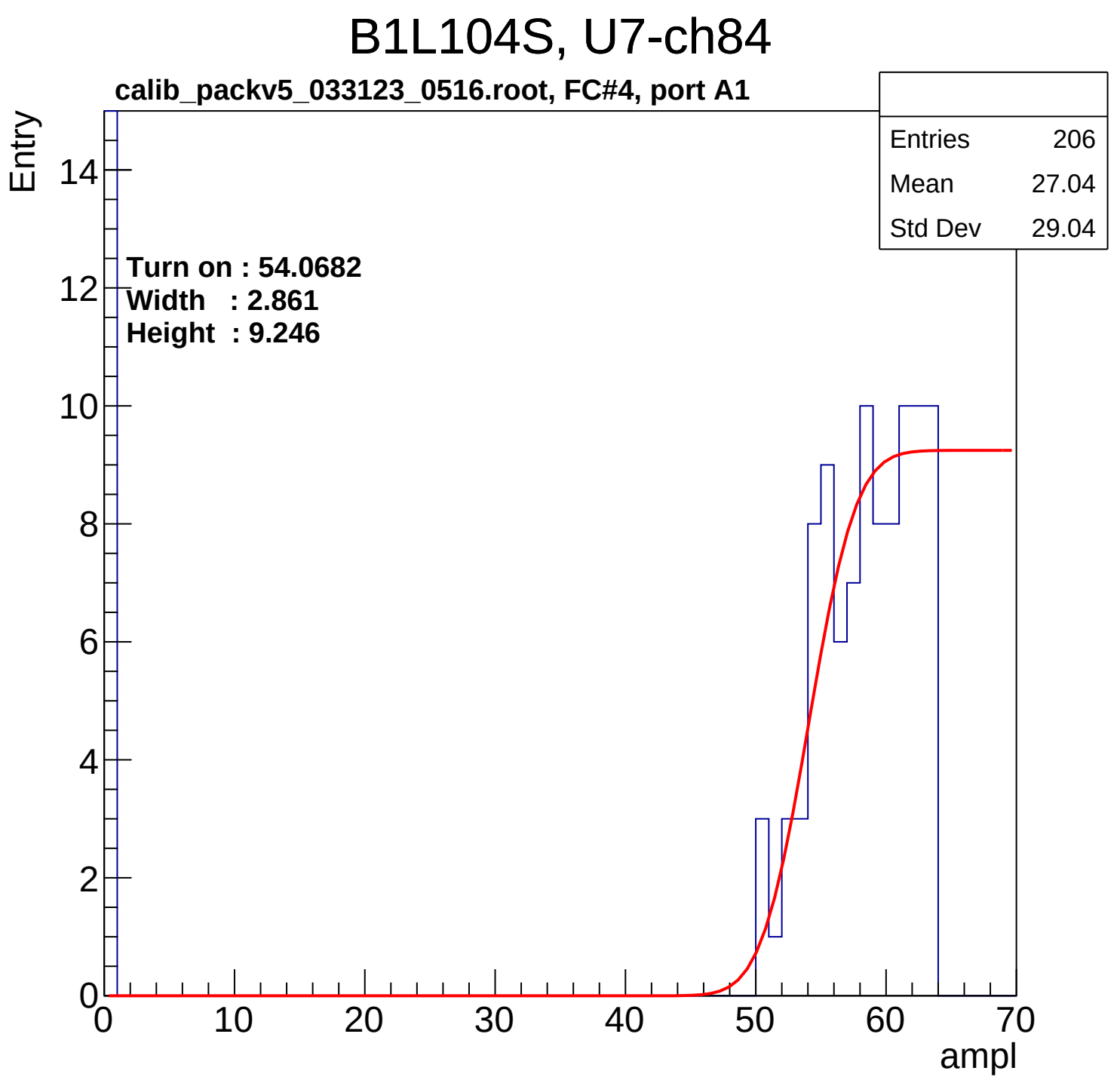

B1L104S, U7-ch79
calib_packv5_033123_0516.root, FC#4, port A1
Entries 207
Mean 26.1
Std Dev 29.04
Turn on : 54.8510
Width : 2.587
Height : 9.761
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

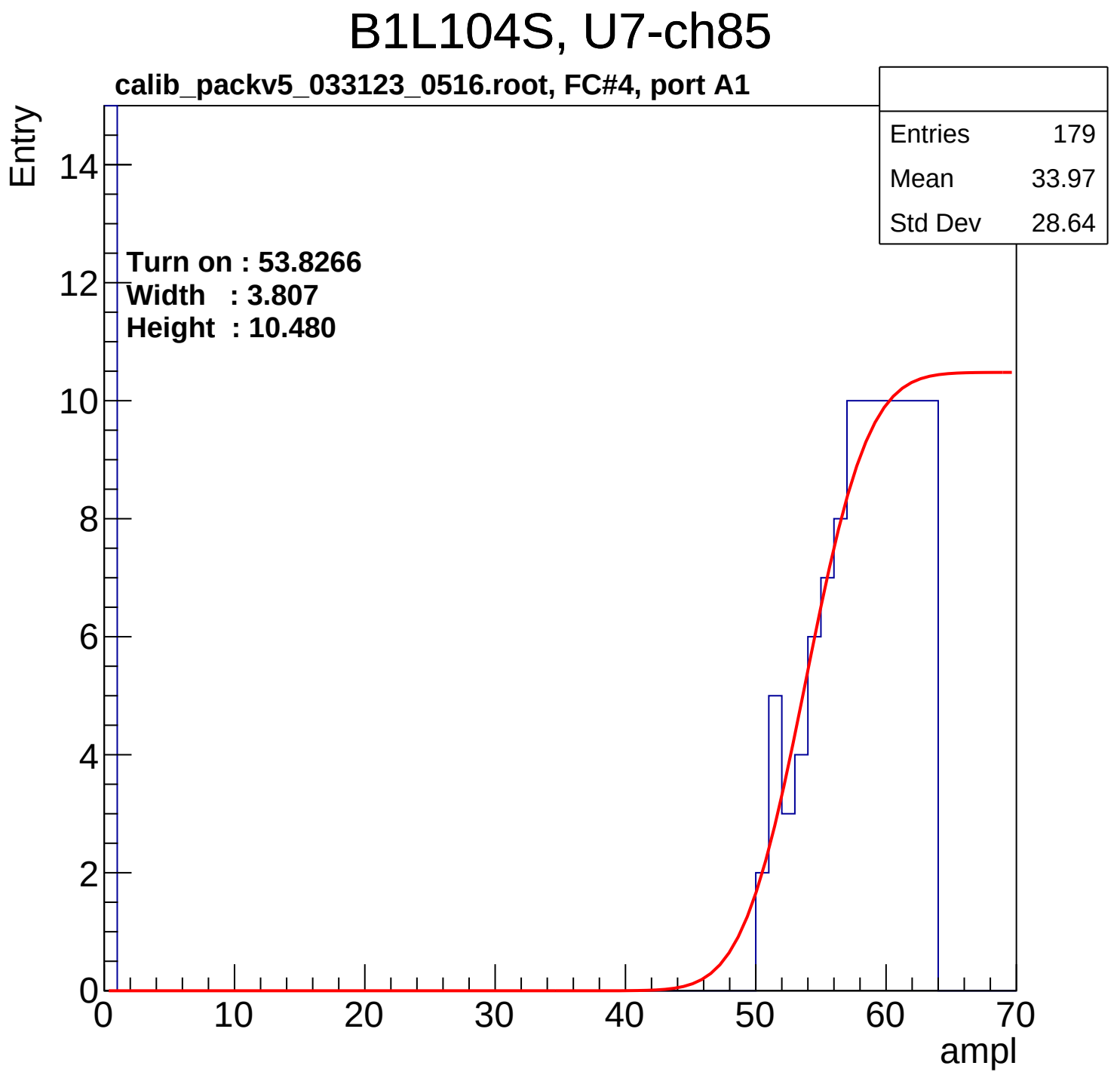

B1L104S, U7-ch80
calib_packv5_033123_0516.root, FC#4, port A1
Entries 220
Mean 30.63
Std Dev 28.64
Turn on : 52.6305
Width : 3.609
Height : 10.195
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

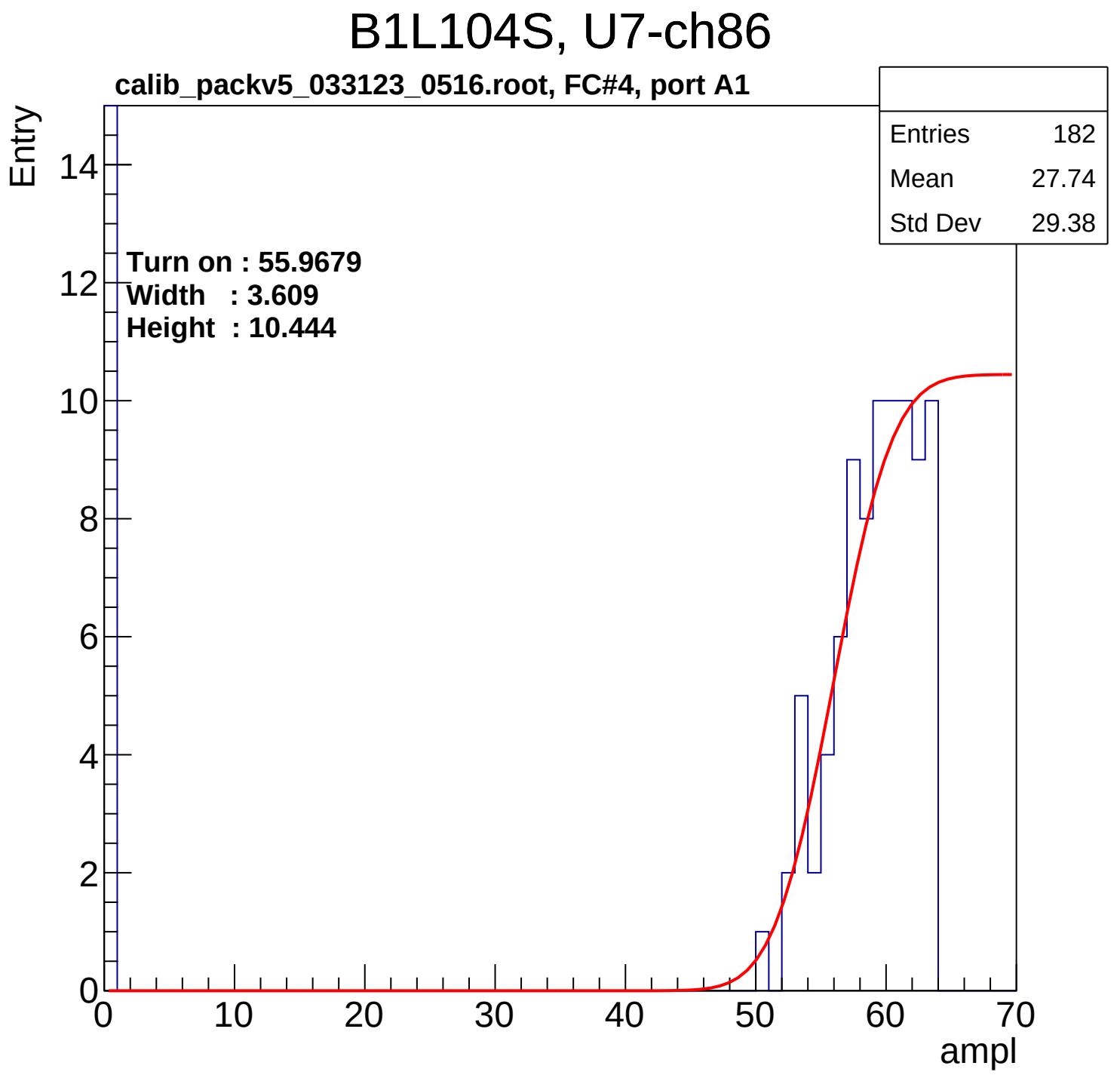

B1L104S, U7-ch81
calib_packv5_033123_0516.root, FC#4, port A1
Entries 188
Mean 27.29
Std Dev 29.19
Turn on : 54.7679
Width : 4.204
Height : 9.803
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

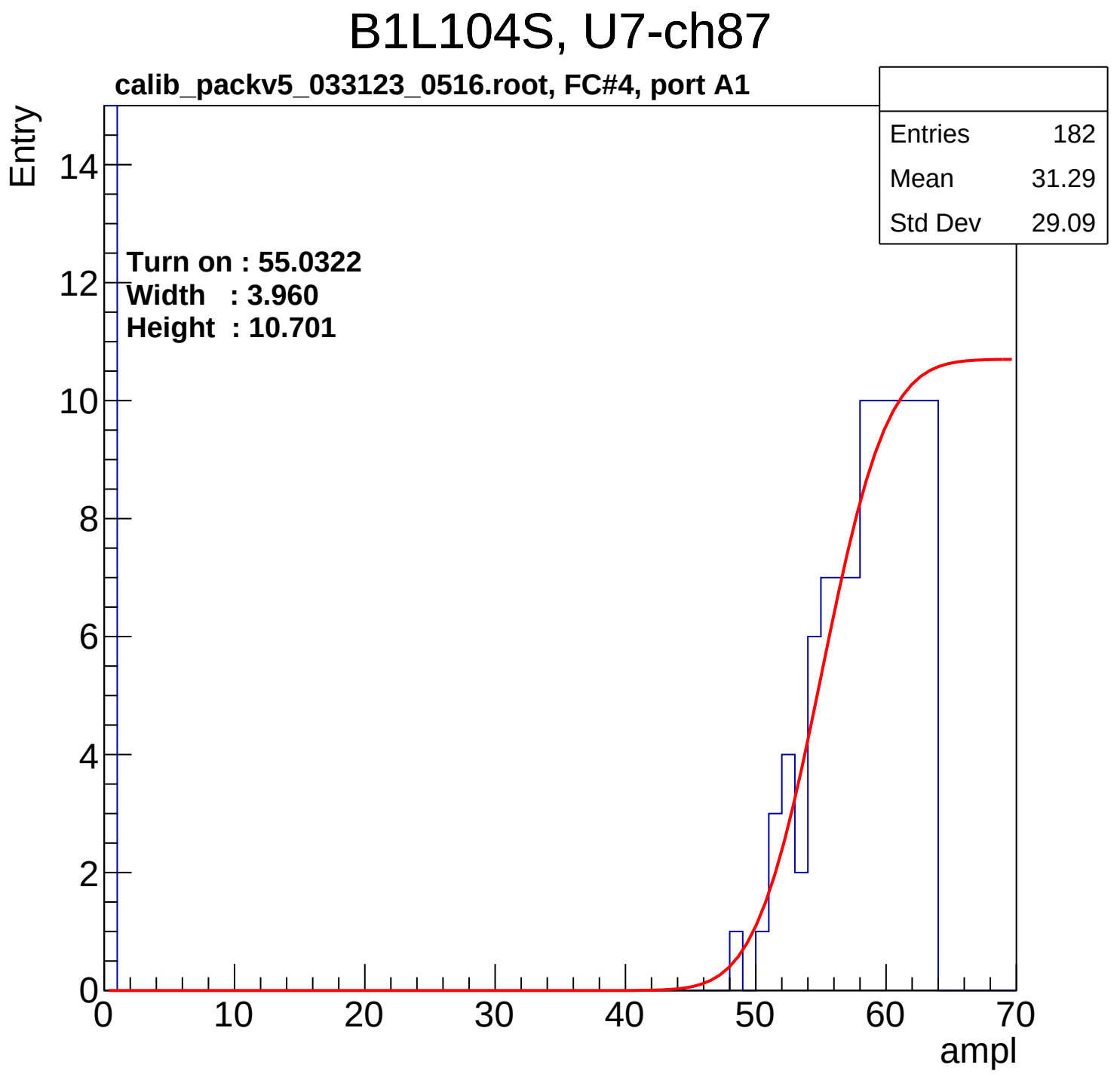

B1L104S, U7-ch82
calib_packv5_033123_0516.root, FC#4, port A1
Entries 209
Mean 30.9
Std Dev 28.66
Turn on : 53.3145
Width : 4.516
Height : 10.376
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

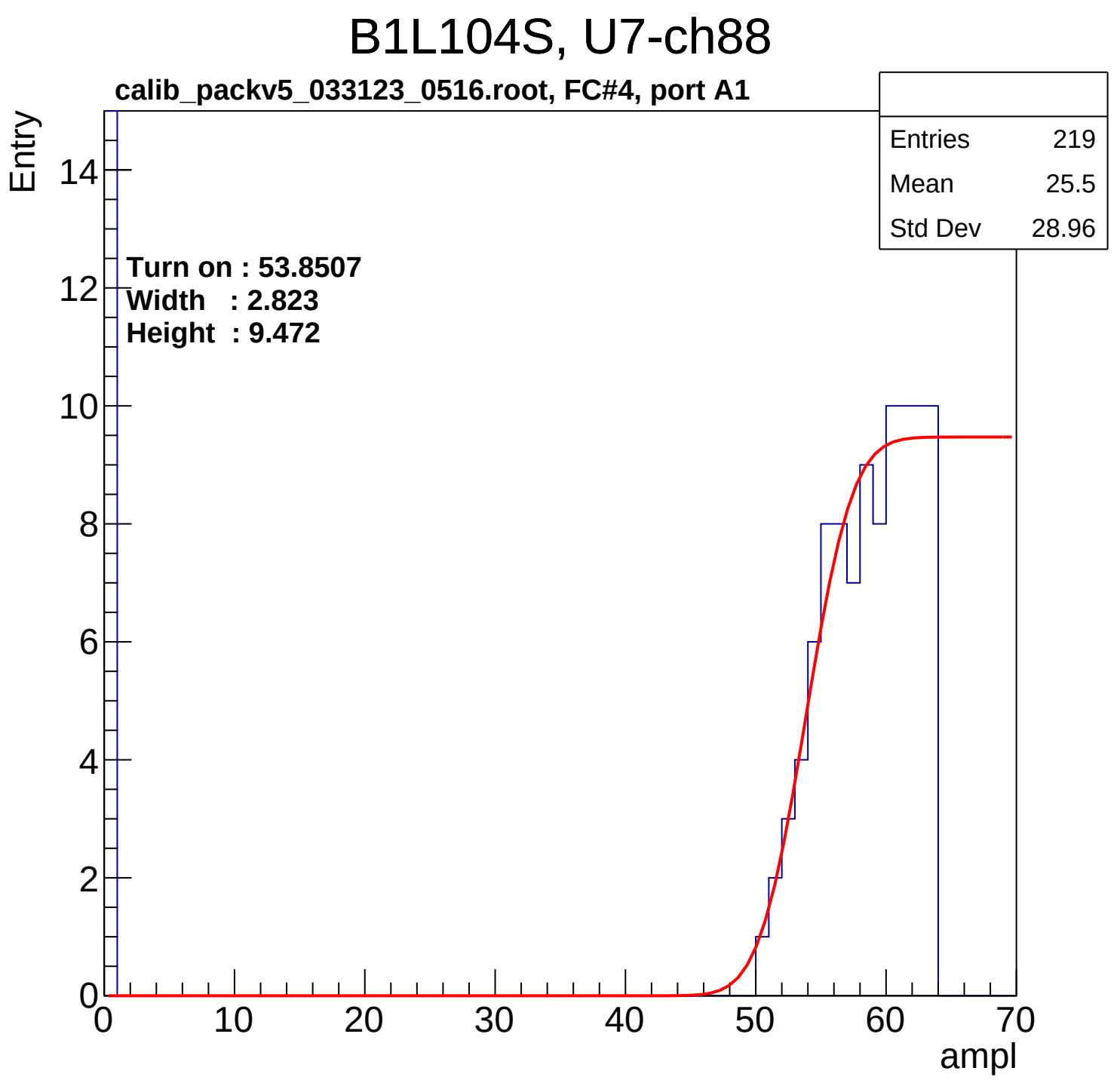

B1L104S, U7-ch83
calib_packv5_033123_0516.root, FC#4, port A1
Entries 182
Mean 31.28
Std Dev 29.08
Turn on : 54.4089
Width : 3.222
Height : 10.075
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

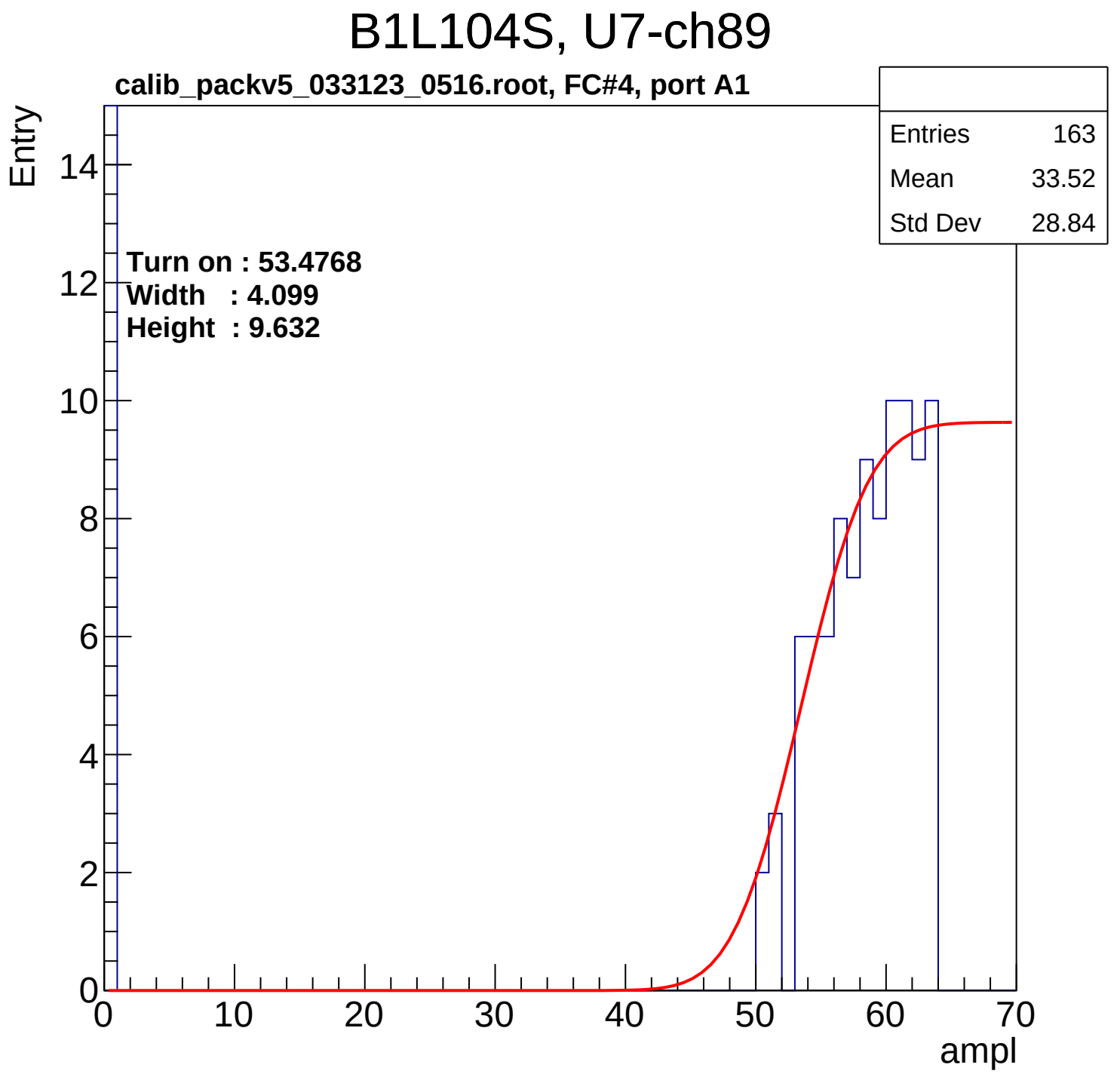

B1L104S, U7-ch84
calib_packv5_033123_0516.root, FC#4, port A1
Entries 206
Mean 27.04
Std Dev 29.04
Turn on : 54.0682
Width : 2.861
Height : 9.246
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

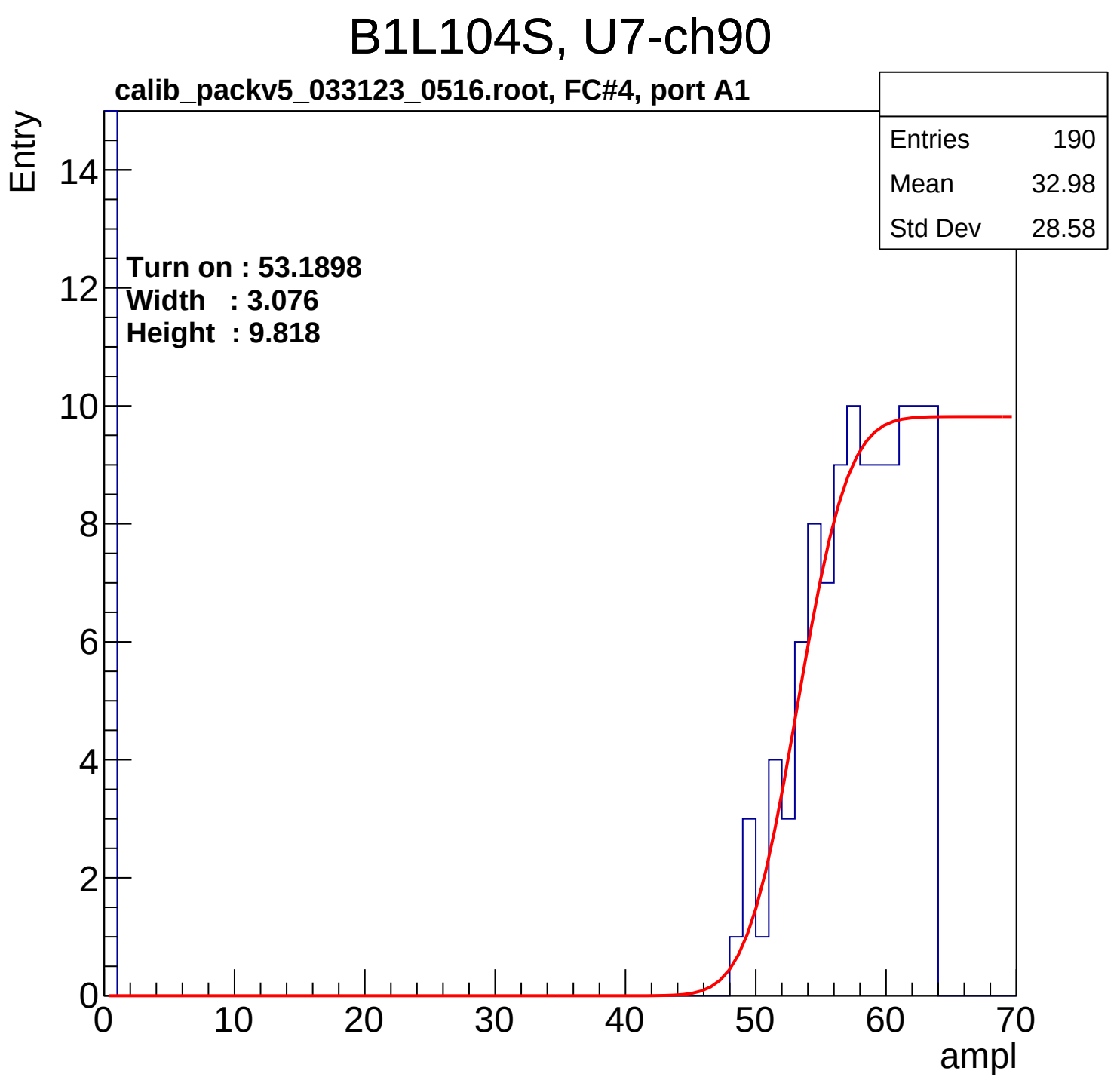

B1L104S, U7-ch85
calib_packv5_033123_0516.root, FC#4, port A1
Entries 179
Mean 33.97
Std Dev 28.64
Turn on : 53.8266
Width : 3.807
Height : 10.480
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

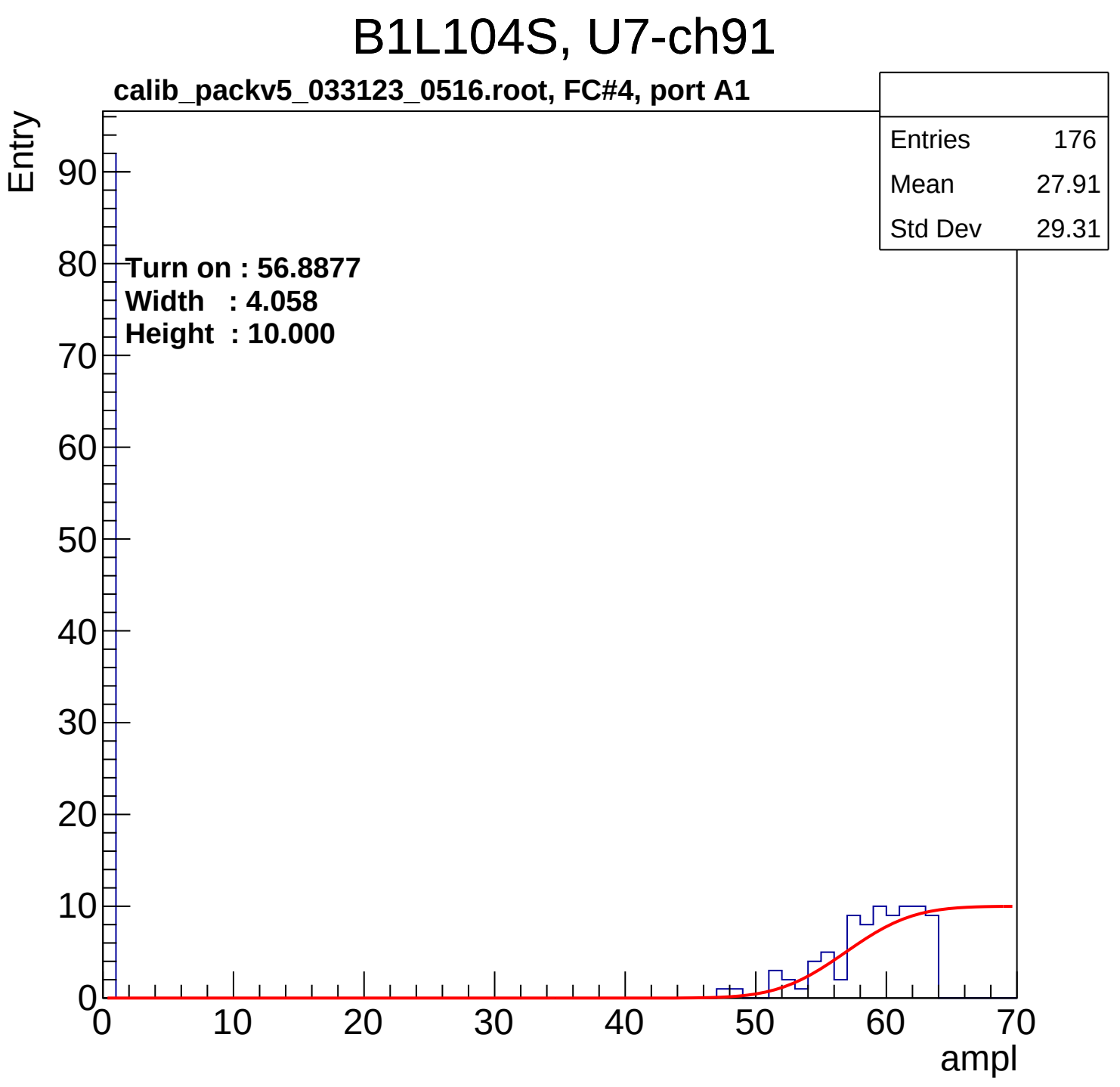

B1L104S, U7-ch86
calib_packv5_033123_0516.root, FC#4, port A1
Entries 182
Mean 27.74
Std Dev 29.38
Turn on : 55.9679
Width : 3.609
Height : 10.444
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

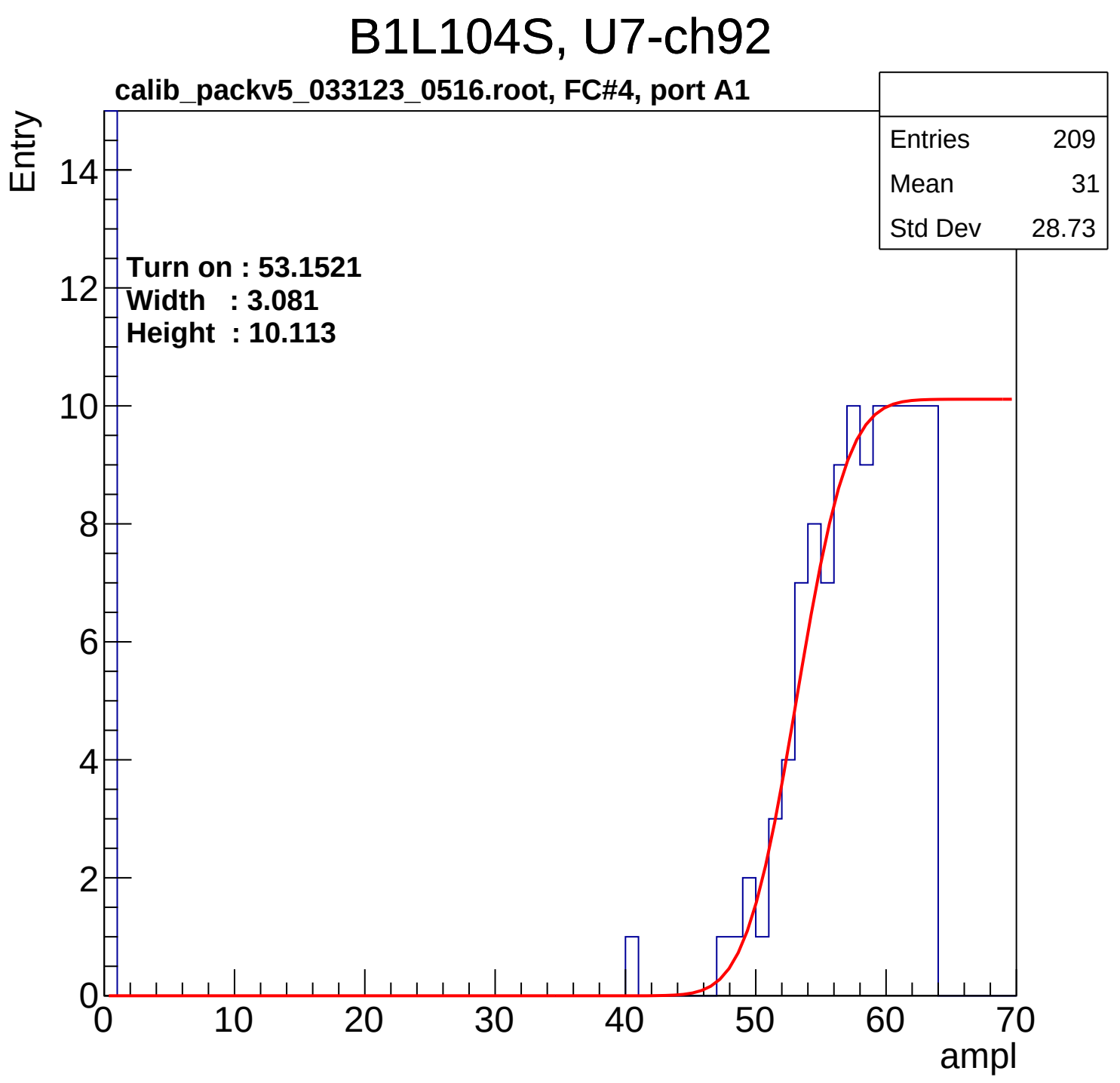

B1L104S, U7-ch87
calib_packv5_033123_0516.root, FC#4, port A1
Entries 182
Mean 31.29
Std Dev 29.09
Turn on : 55.0322
Width : 3.960
Height : 10.701
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

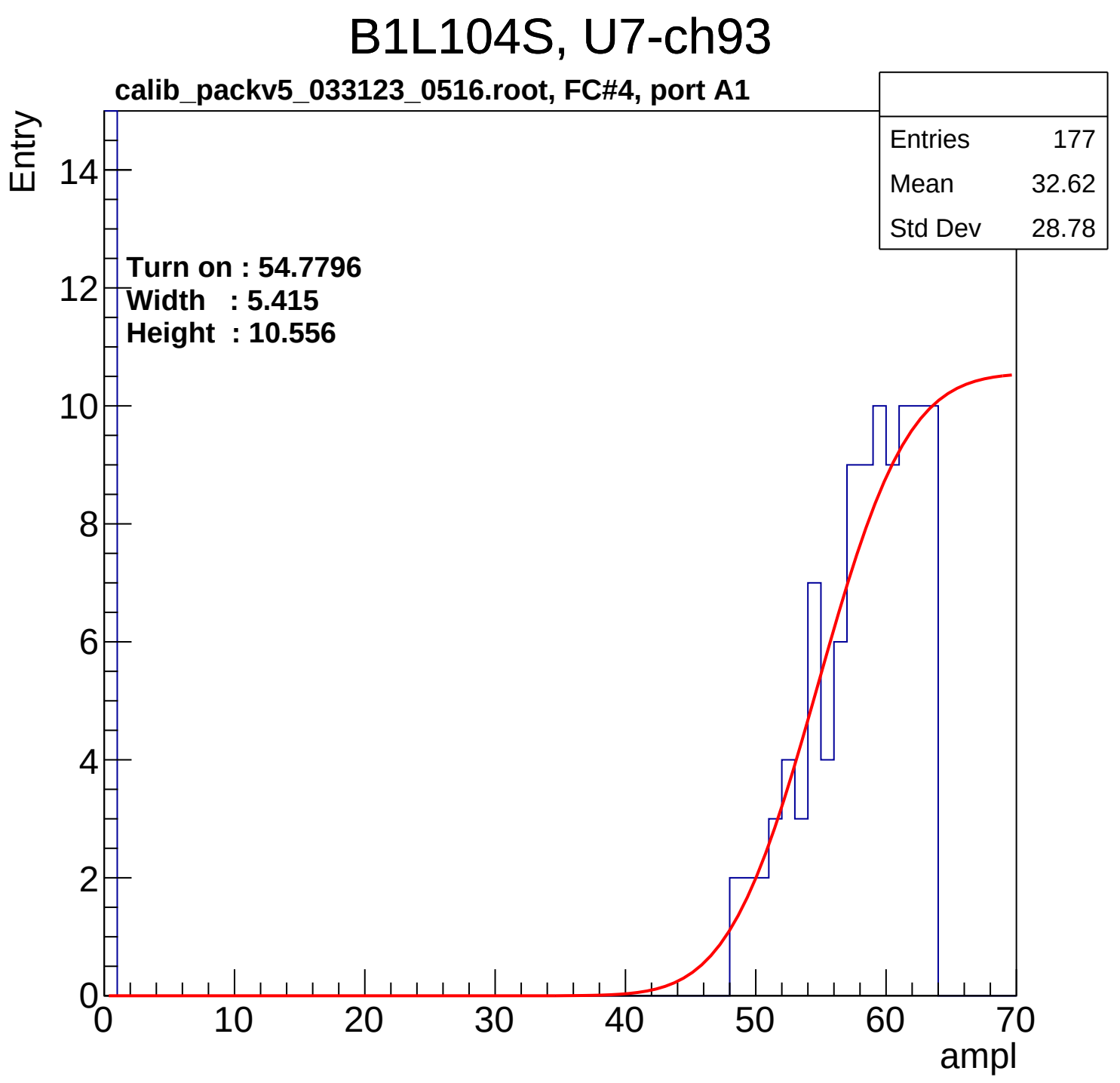

B1L104S, U7-ch88
calib_packv5_033123_0516.root, FC#4, port A1
Entries 219
Mean 25.5
Std Dev 28.96
Turn on : 53.8507
Width : 2.823
Height : 9.472
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

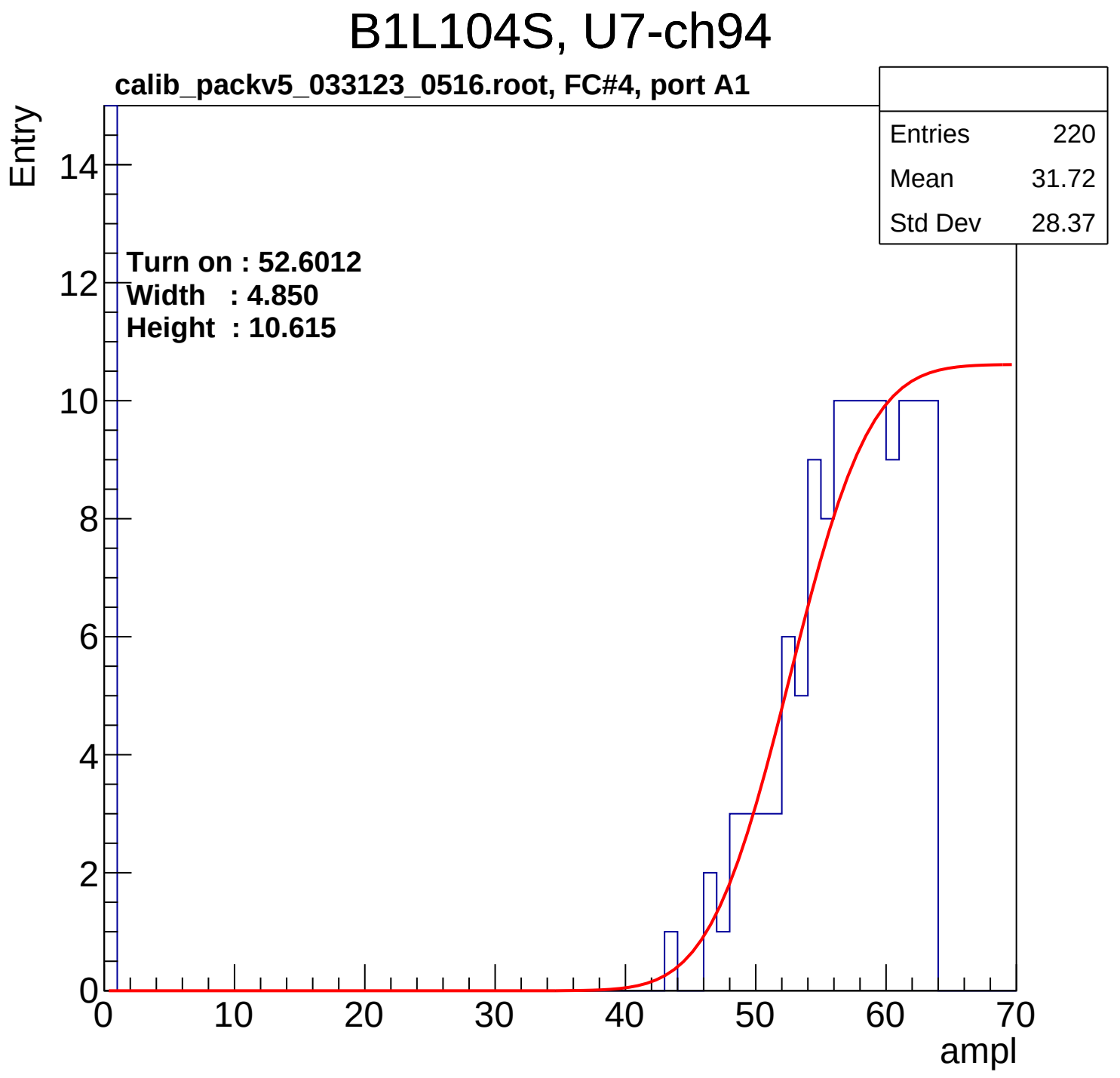

B1L104S, U7-ch89
calib_packv5_033123_0516.root, FC#4, port A1
Entries 163
Mean 33.52
Std Dev 28.84
Turn on : 53.4768
Width : 4.099
Height : 9.632
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

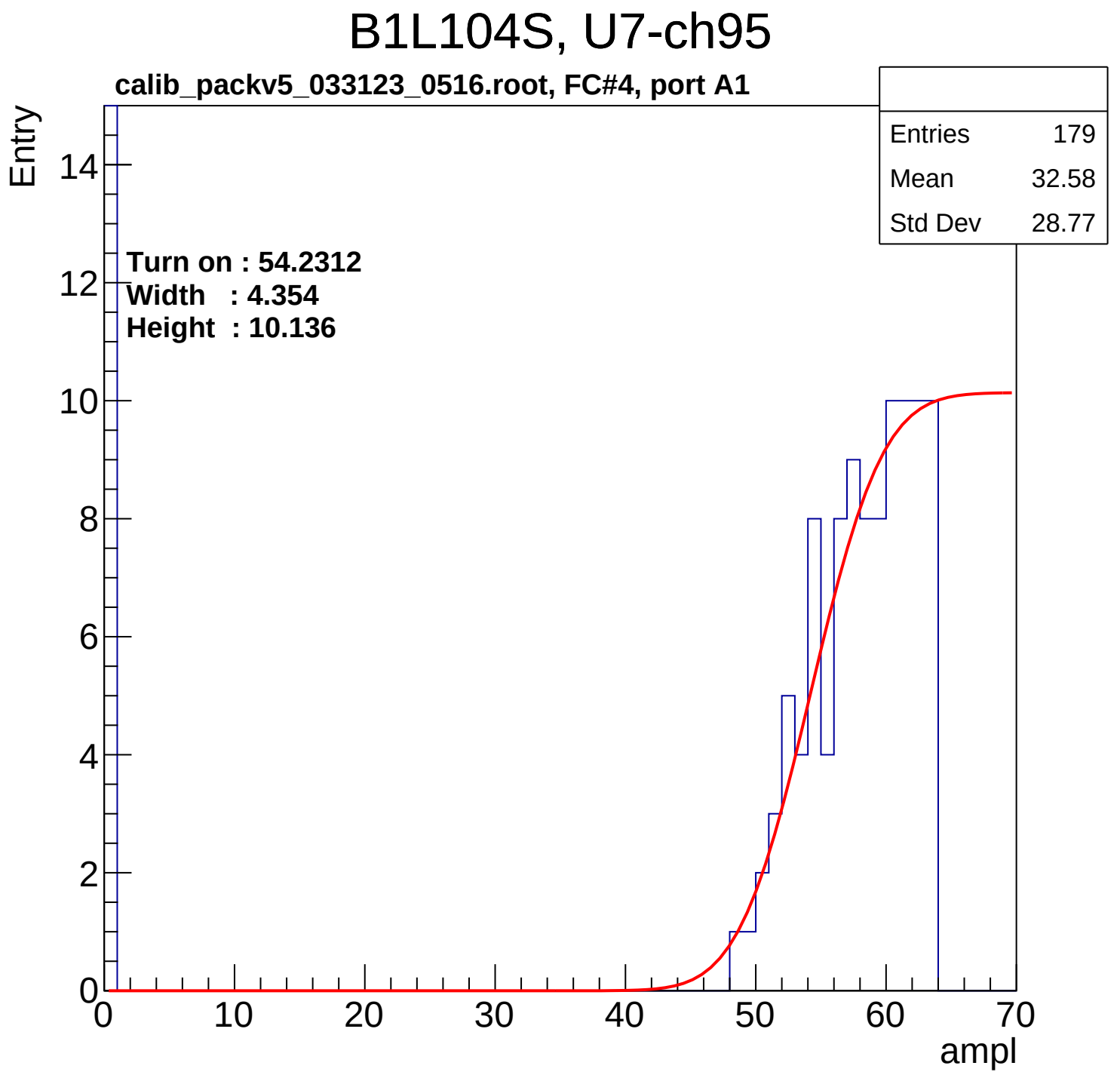

B1L104S, U7-ch90
calib_packv5_033123_0516.root, FC#4, port A1
Entries 190
Mean 32.98
Std Dev 28.58
Turn on : 53.1898
Width : 3.076
Height : 9.818
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

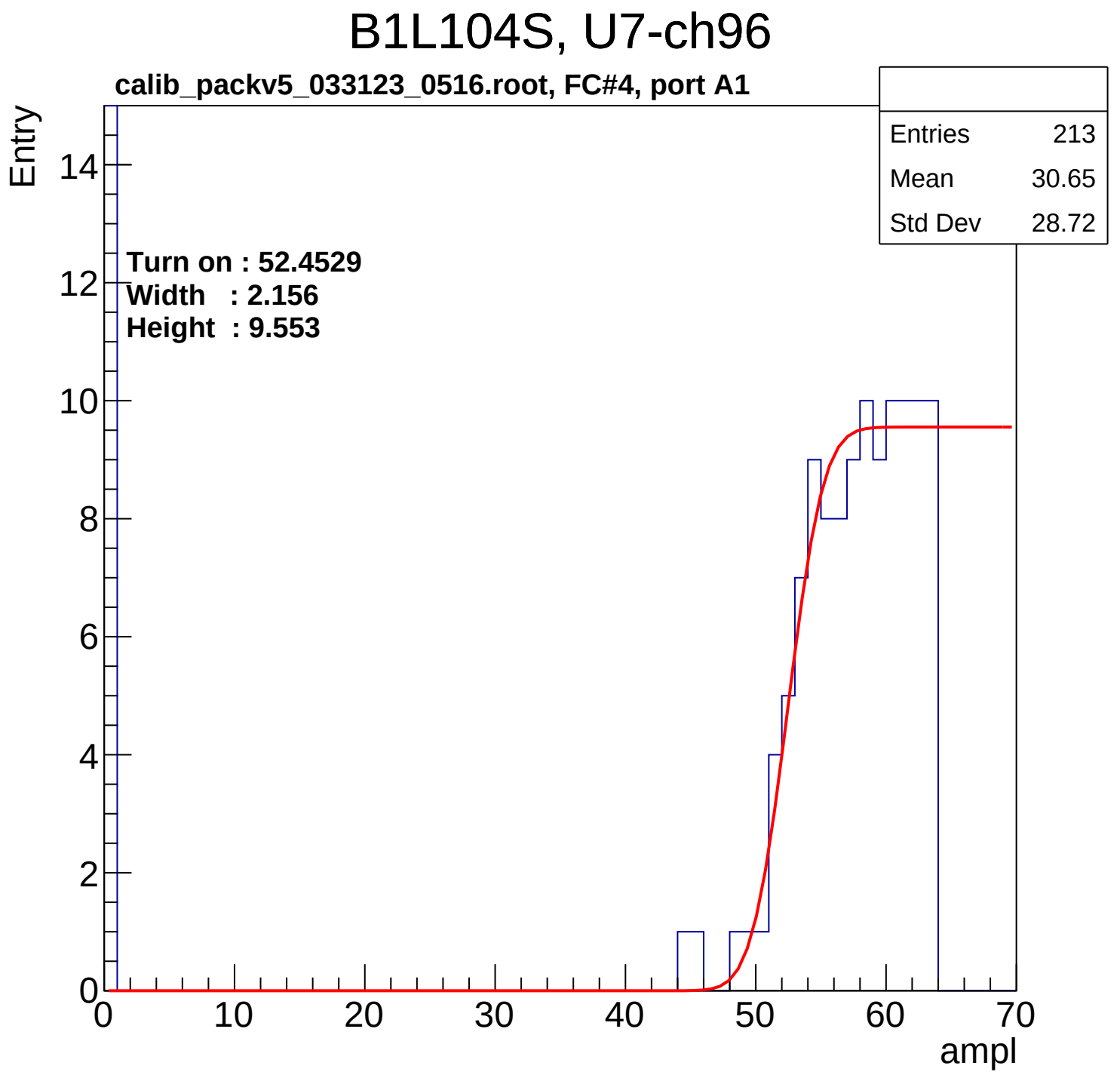

B1L104S, U7-ch91
calib_packv5_033123_0516.root, FC#4, port A1
Entries 176
Mean 27.91
Std Dev 29.31
Turn on : 56.8877
Width : 4.058
Height : 10.000
Entry
ampl
0
10
20
30
40
50
60
70
80
90

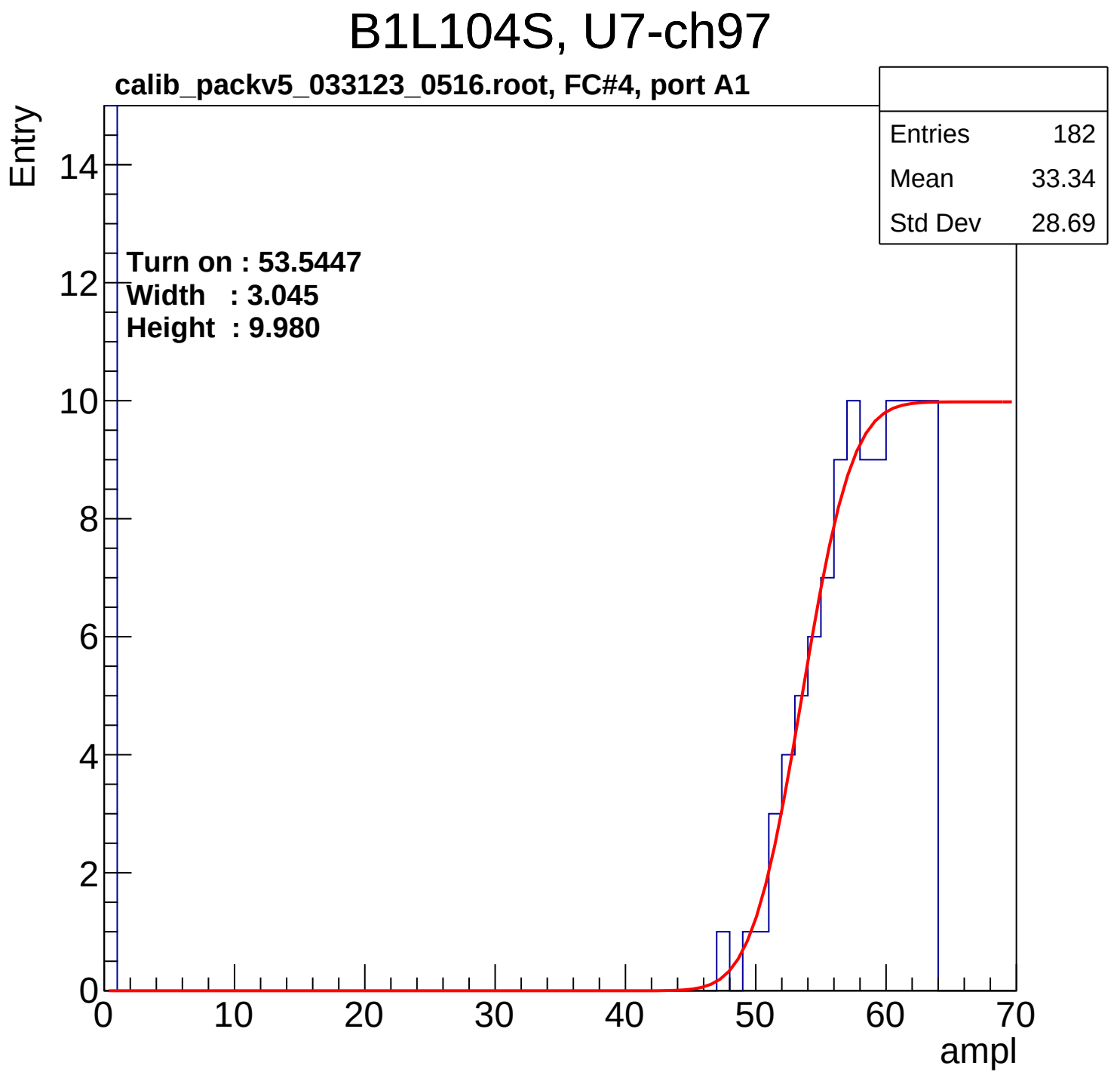

B1L104S, U7-ch92
calib_packv5_033123_0516.root, FC#4, port A1
Entries 209
Mean 31
Std Dev 28.73
Turn on : 53.1521
Width : 3.081
Height : 10.113
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

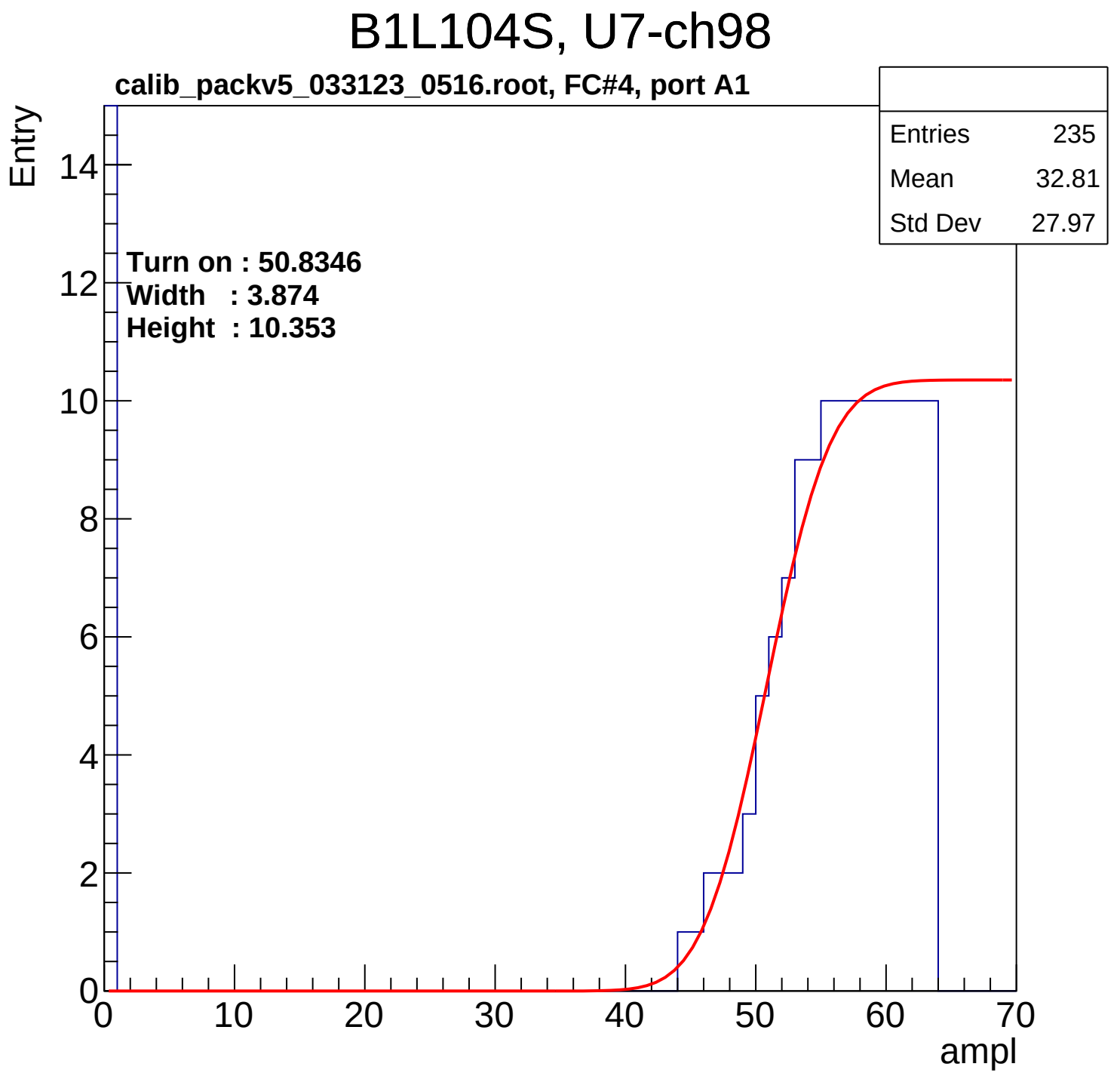

B1L104S, U7-ch93
calib_packv5_033123_0516.root, FC#4, port A1
Entries 177
Mean 32.62
Std Dev 28.78
Turn on : 54.7796
Width : 5.415
Height : 10.556
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

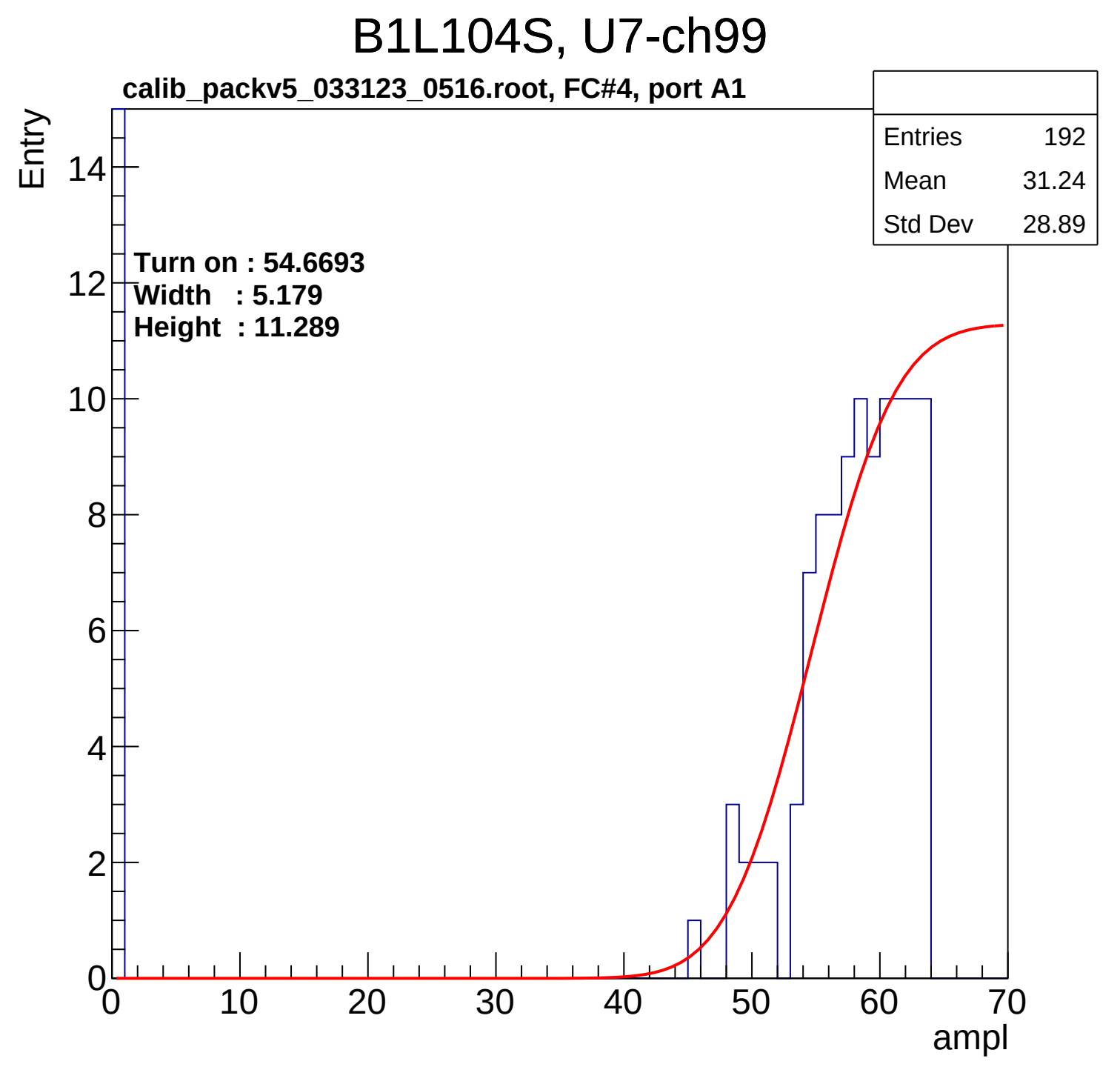

B1L104S, U7-ch94
calib_packv5_033123_0516.root, FC#4, port A1
Entries 220
Mean 31.72
Std Dev 28.37
Turn on : 52.6012
Width : 4.850
Height : 10.615
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

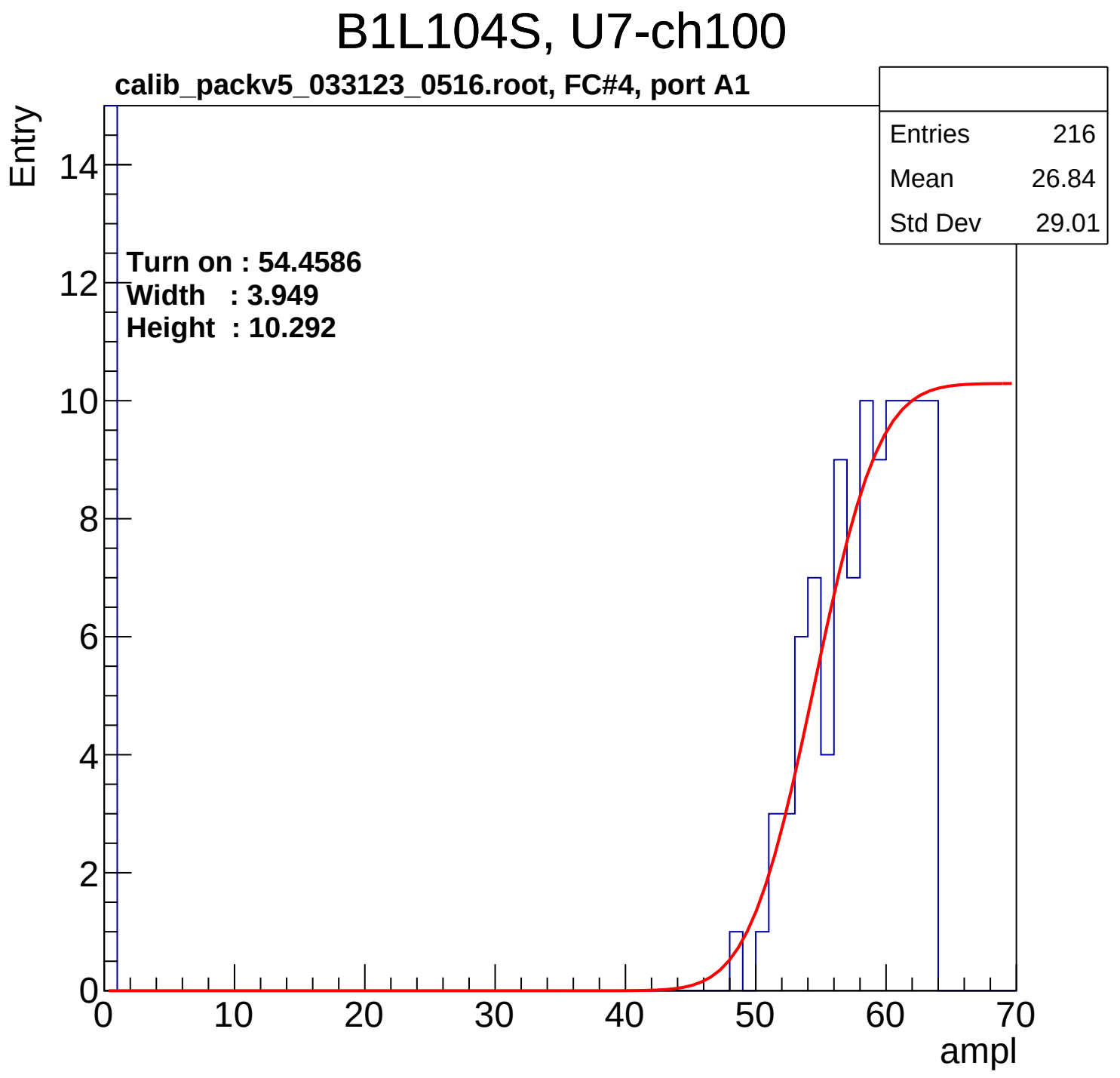

B1L104S, U7-ch95
calib_packv5_033123_0516.root, FC#4, port A1
Entries 179
Mean 32.58
Std Dev 28.77
Turn on : 54.2312
Width : 4.354
Height : 10.136
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

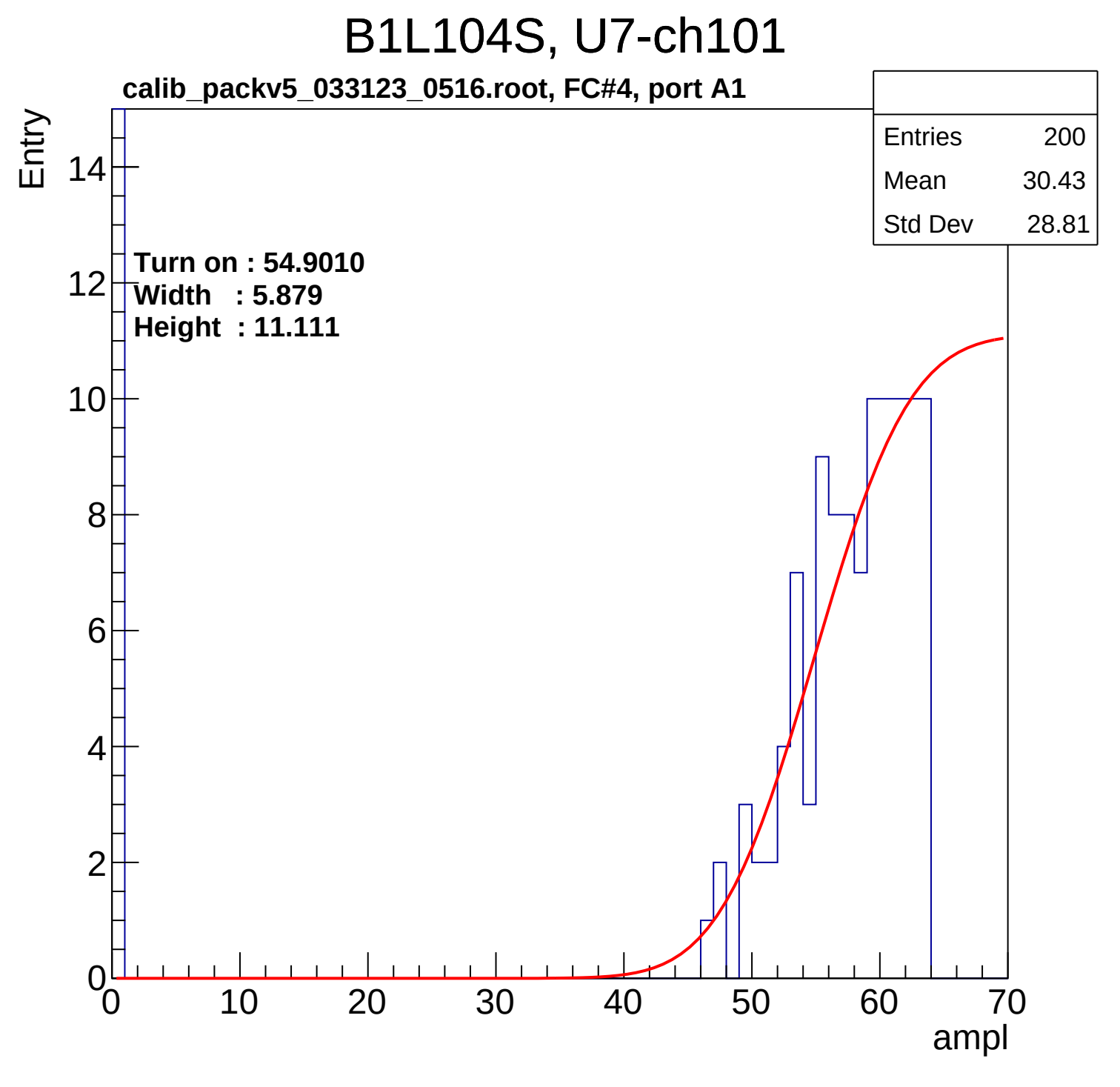

B1L104S, U7-ch96
calib_packv5_033123_0516.root, FC#4, port A1
Entries 213
Mean 30.65
Std Dev 28.72
Turn on : 52.4529
Width : 2.156
Height : 9.553
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

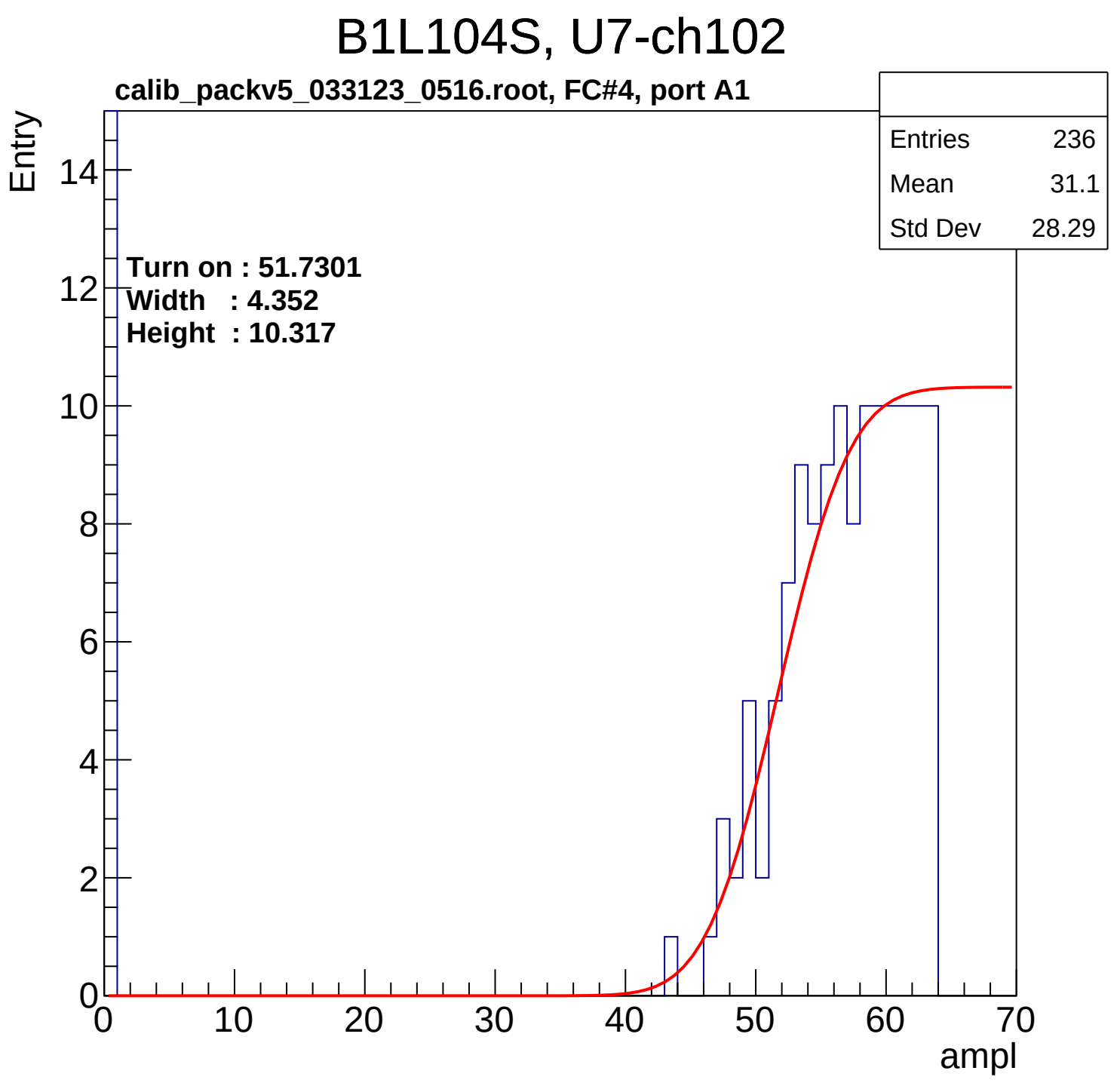

B1L104S, U7-ch97
calib_packv5_033123_0516.root, FC#4, port A1
Entries 182
Mean 33.34
Std Dev 28.69
Turn on : 53.5447
Width : 3.045
Height : 9.980
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

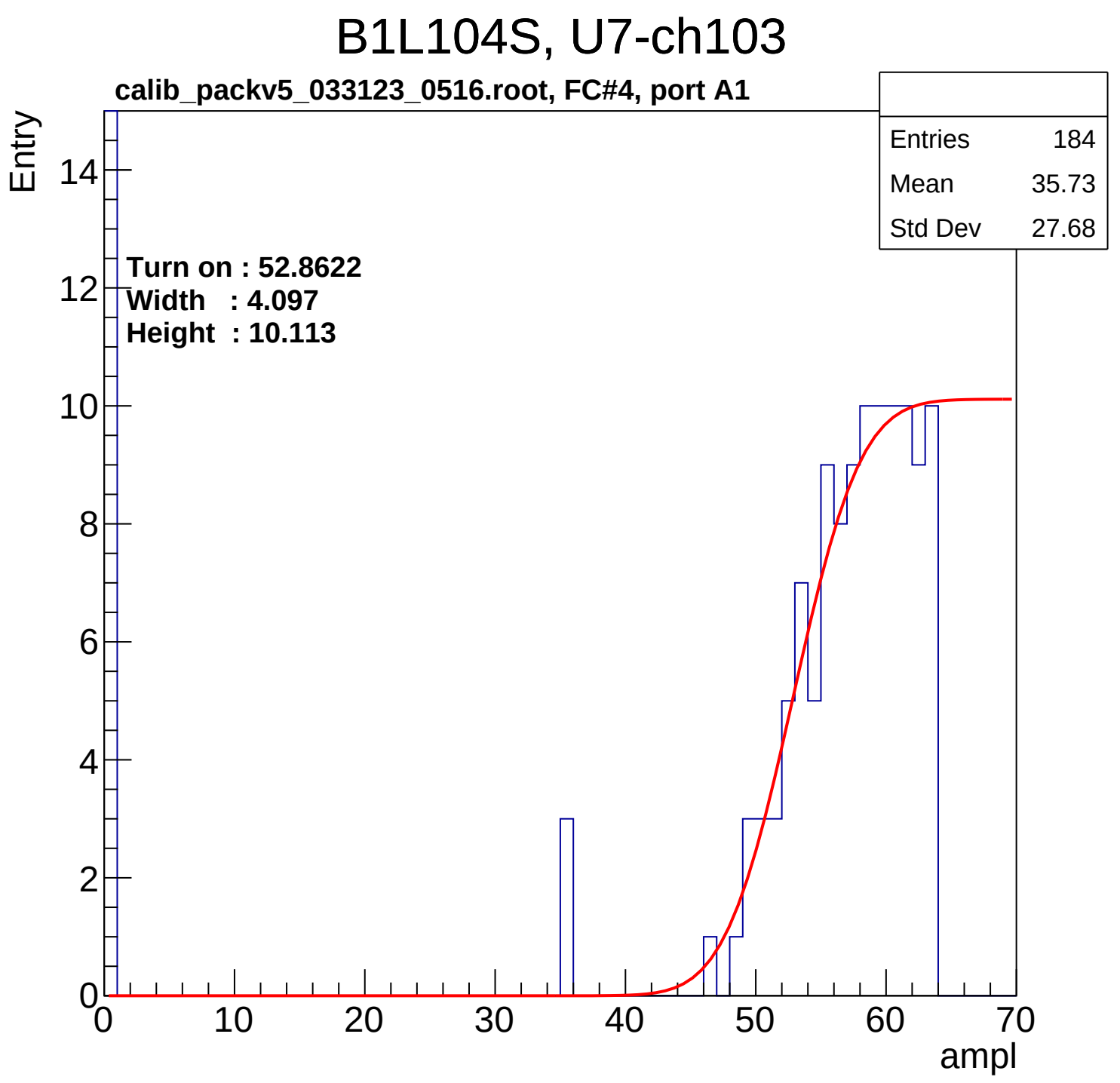

B1L104S, U7-ch98
calib_packv5_033123_0516.root, FC#4, port A1
Entries 235
Mean 32.81
Std Dev 27.97
Turn on : 50.8346
Width : 3.874
Height : 10.353
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

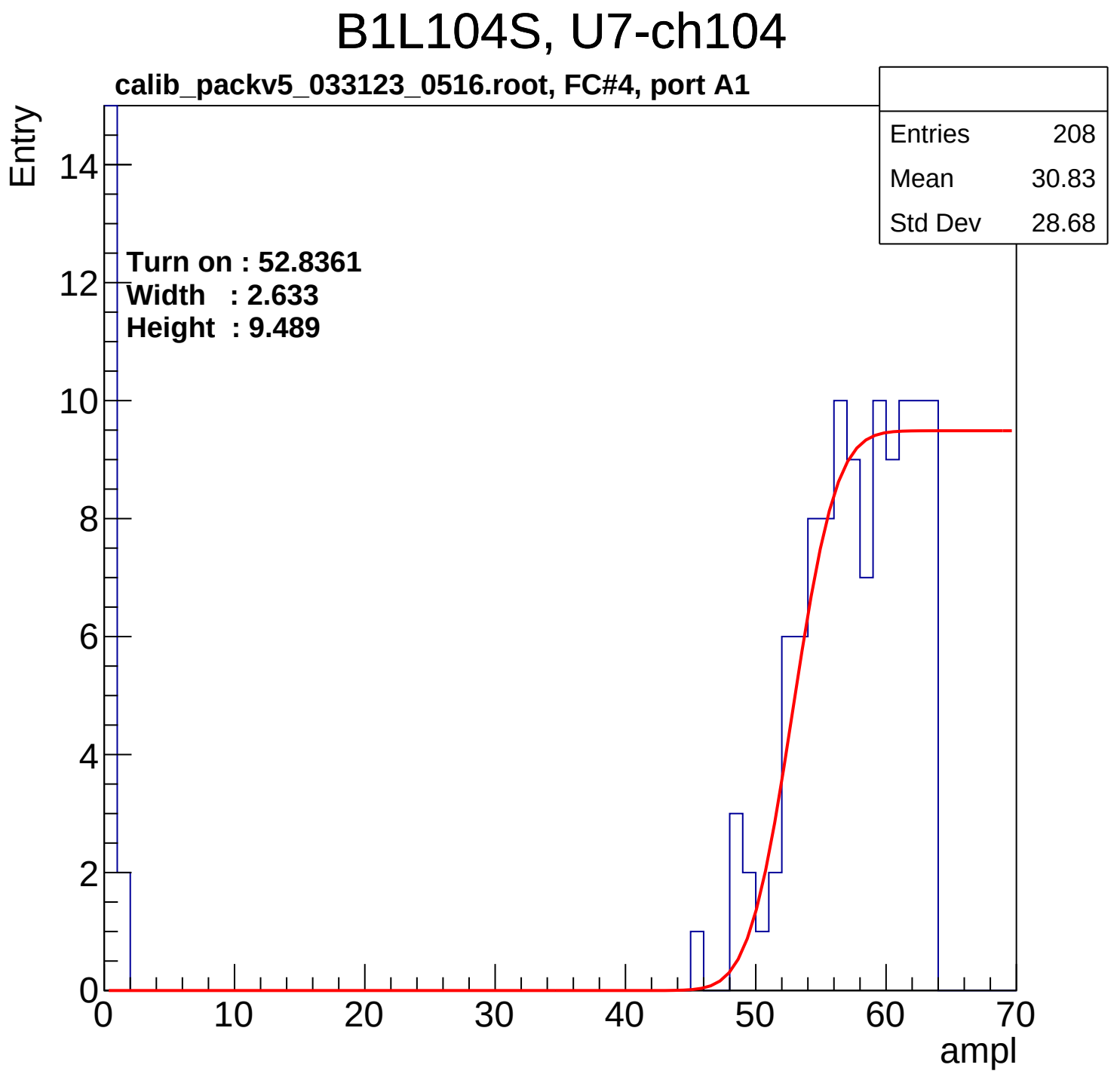

B1L104S, U7-ch99
calib_packv5_033123_0516.root, FC#4, port A1
Entries 192
Mean 31.24
Std Dev 28.89
Turn on : 54.6693
Width : 5.179
Height : 11.289
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

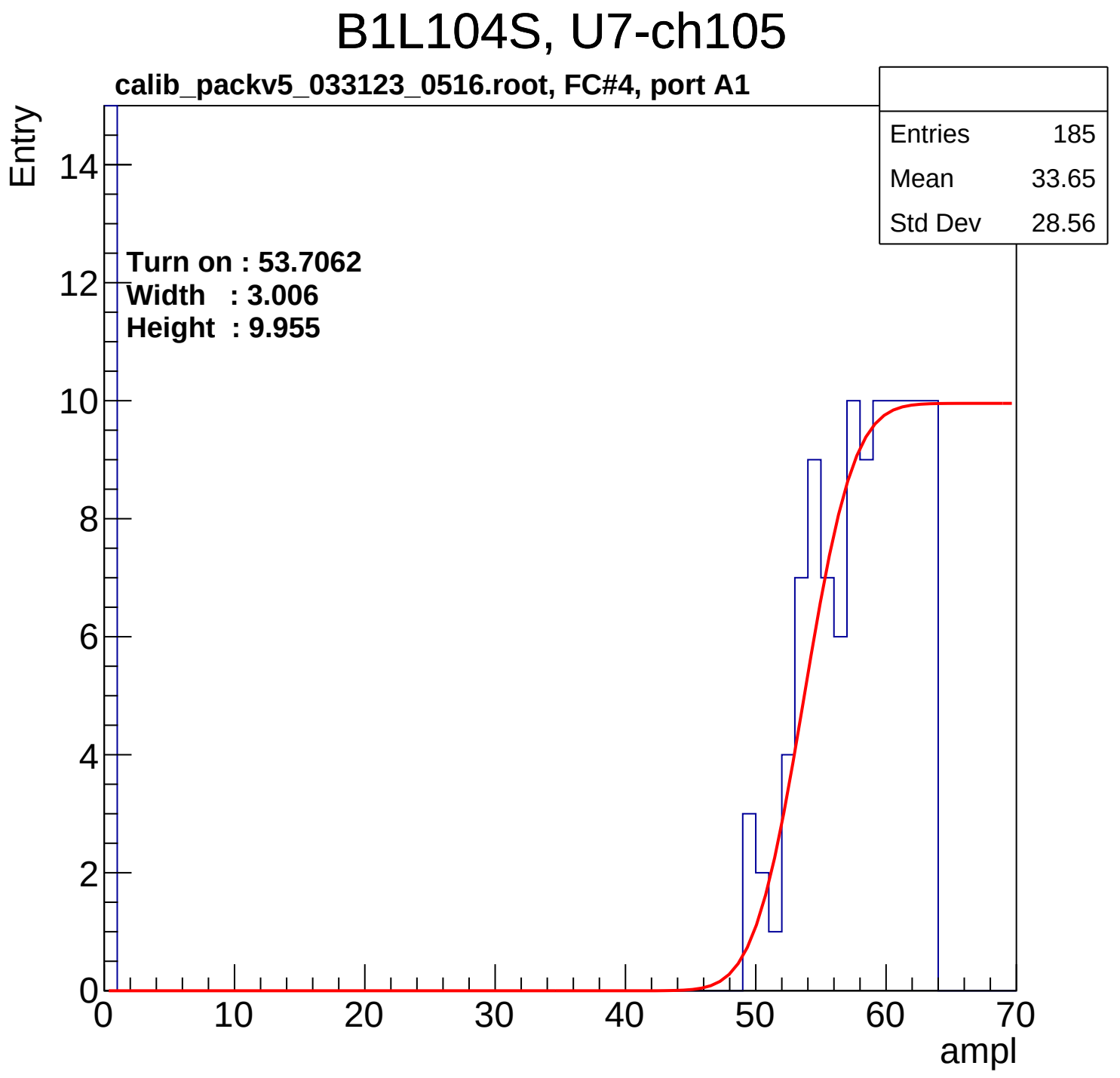

B1L104S, U7-ch100
calib_packv5_033123_0516.root, FC#4, port A1
Entries 216
Mean 26.84
Std Dev 29.01
Turn on : 54.4586
Width : 3.949
Height : 10.292
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

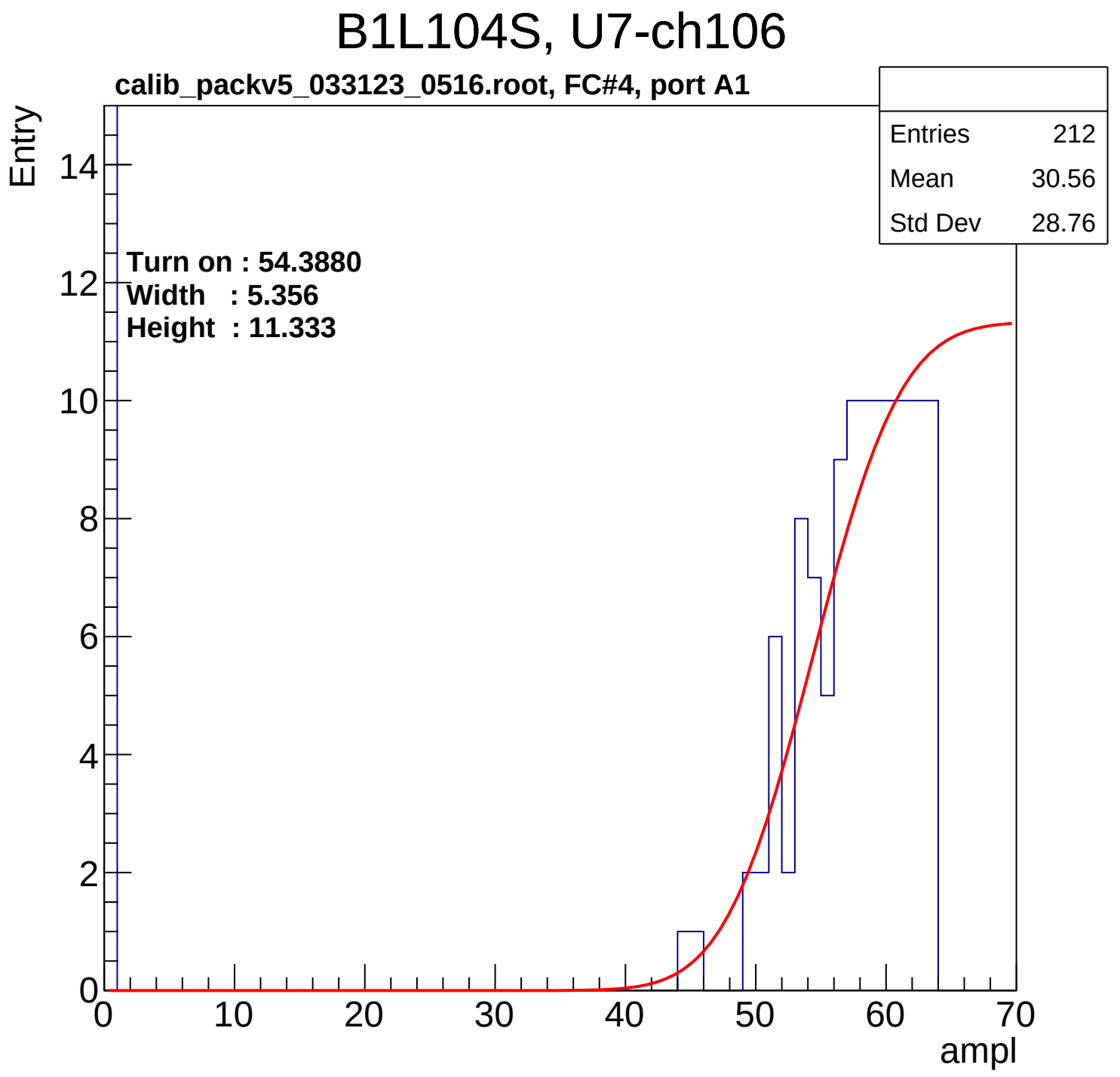

B1L104S, U7-ch101
calib_packv5_033123_0516.root, FC#4, port A1
Entries 200
Mean 30.43
Std Dev 28.81
Turn on : 54.9010
Width : 5.879
Height : 11.111
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

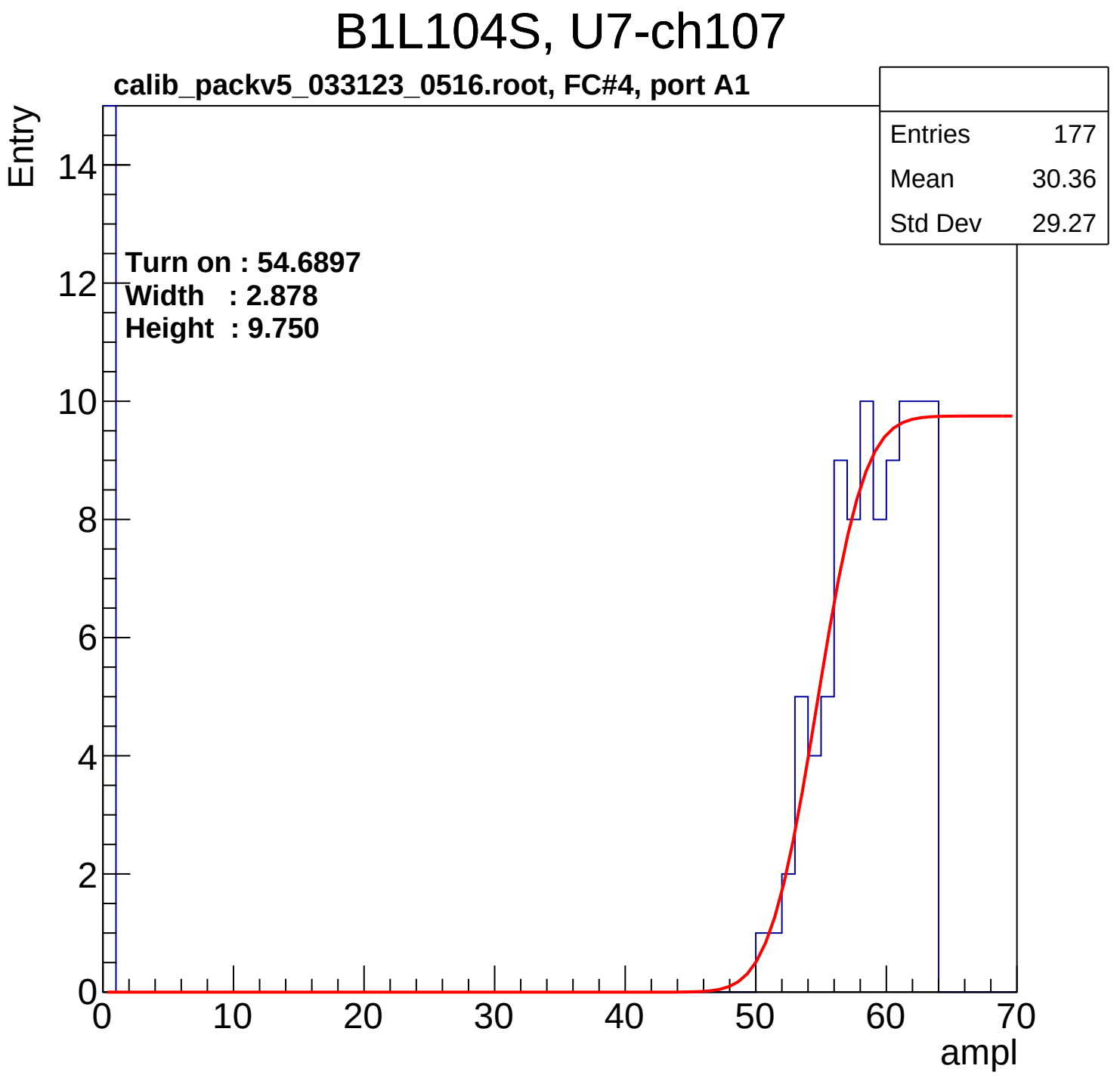

B1L104S, U7-ch102
calib_packv5_033123_0516.root, FC#4, port A1
Entries 236
Mean 31.1
Std Dev 28.29
Turn on : 51.7301
Width : 4.352
Height : 10.317
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

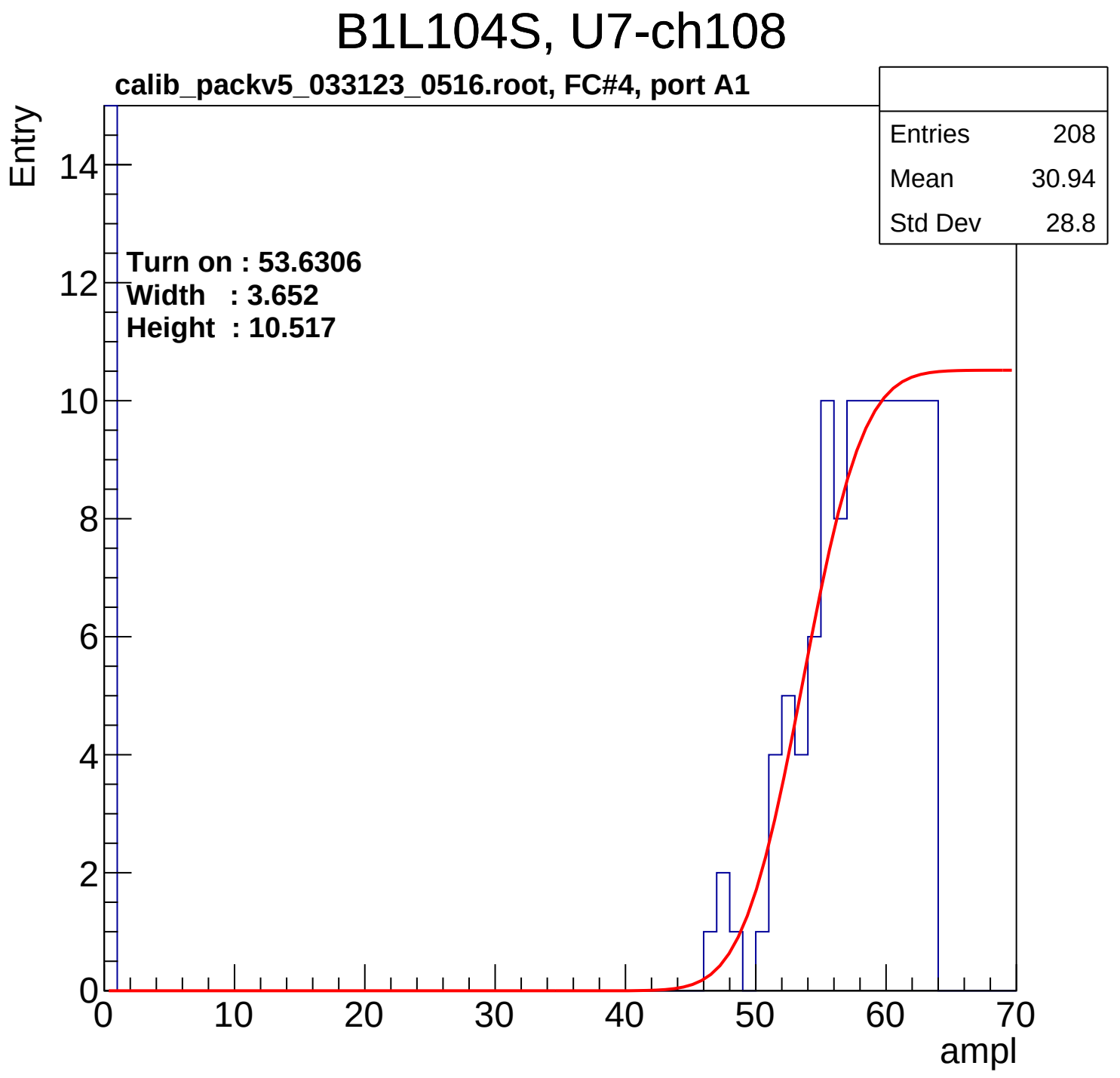

B1L104S, U7-ch103
calib_packv5_033123_0516.root, FC#4, port A1
Entries 184
Mean 35.73
Std Dev 27.68
Turn on : 52.8622
Width : 4.097
Height : 10.113
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

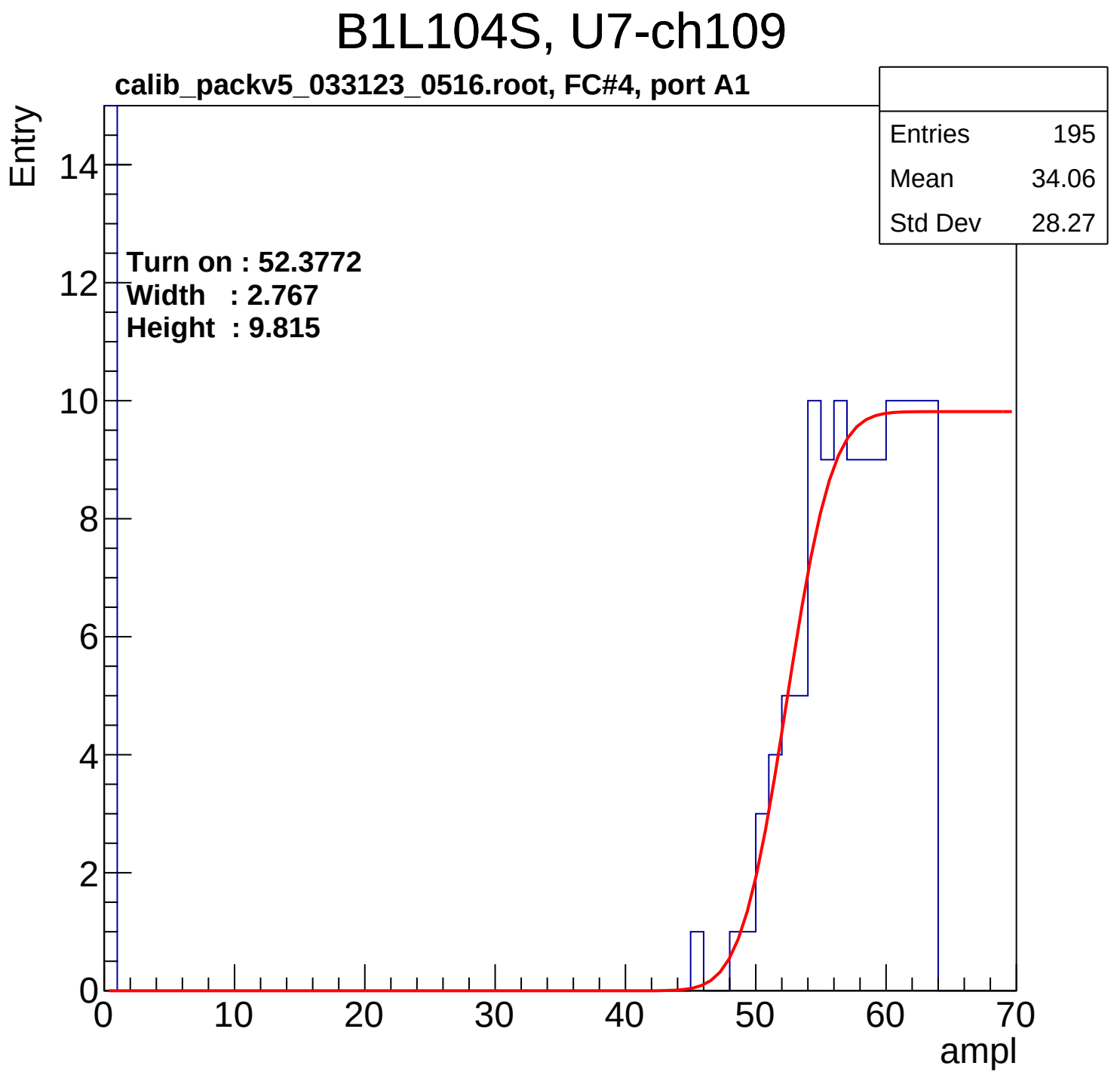

B1L104S, U7-ch104
calib_packv5_033123_0516.root, FC#4, port A1
Entries 208
Mean 30.83
Std Dev 28.68
Turn on : 52.8361
Width : 2.633
Height : 9.489
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

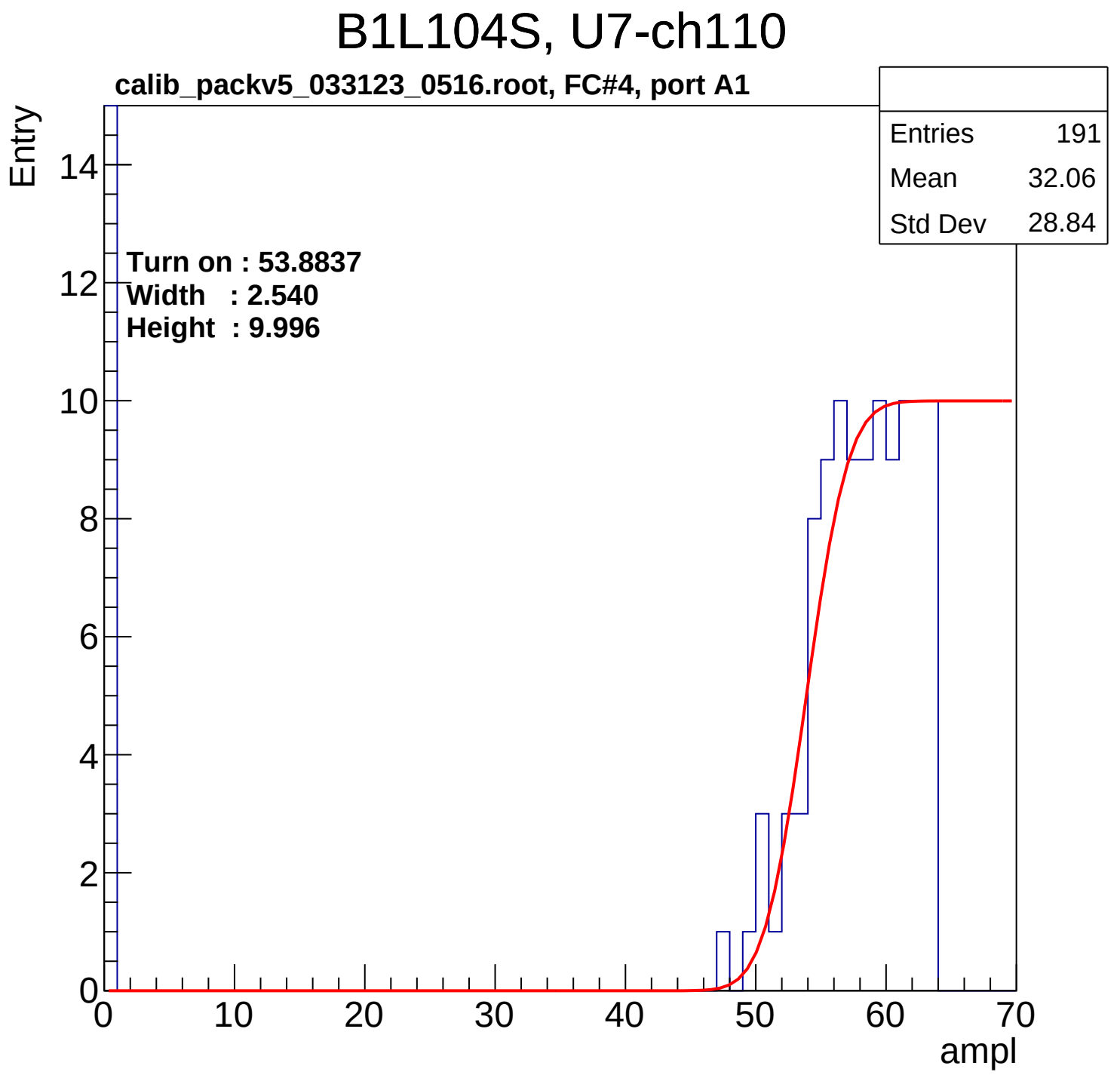

B1L104S, U7-ch105
calib_packv5_033123_0516.root, FC#4, port A1
Entries 185
Mean 33.65
Std Dev 28.56
Turn on : 53.7062
Width : 3.006
Height : 9.955
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

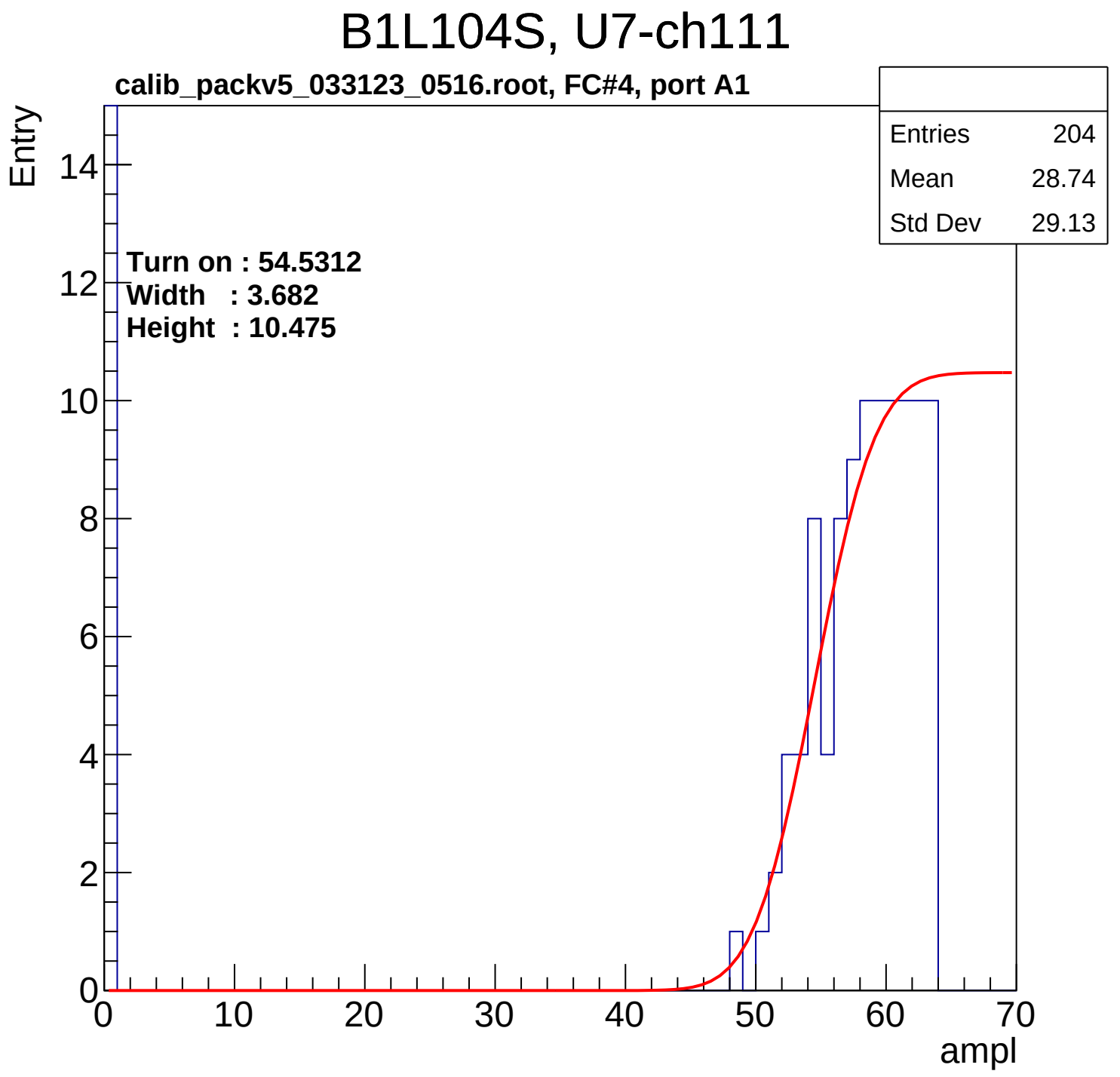

B1L104S, U7-ch106
calib_packv5_033123_0516.root, FC#4, port A1
Entries 212
Mean 30.56
Std Dev 28.76
Turn on : 54.3880
Width : 5.356
Height : 11.333
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

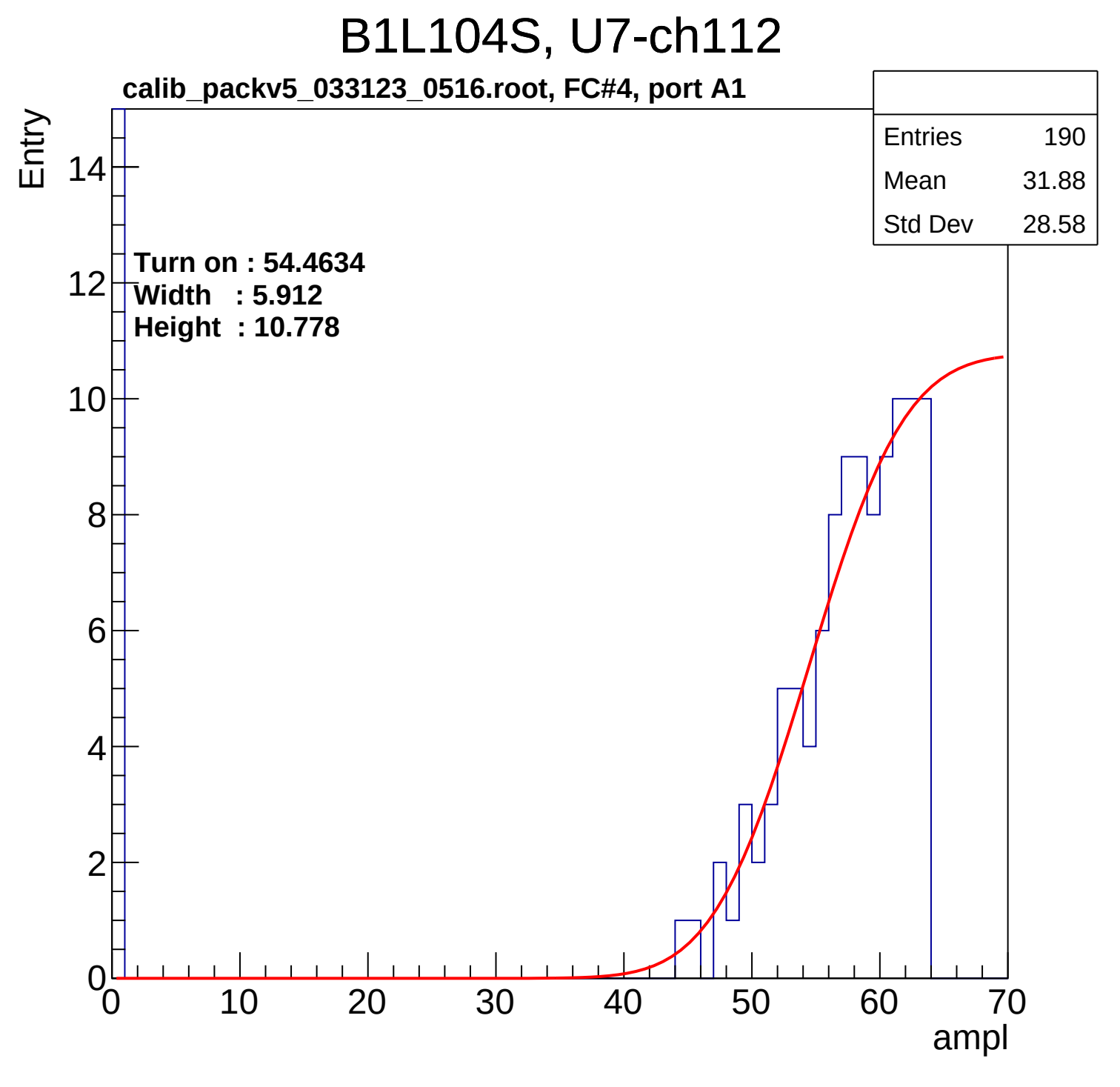

B1L104S, U7-ch107
calib_packv5_033123_0516.root, FC#4, port A1
Entries 177
Mean 30.36
Std Dev 29.27
Turn on : 54.6897
Width : 2.878
Height : 9.750
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

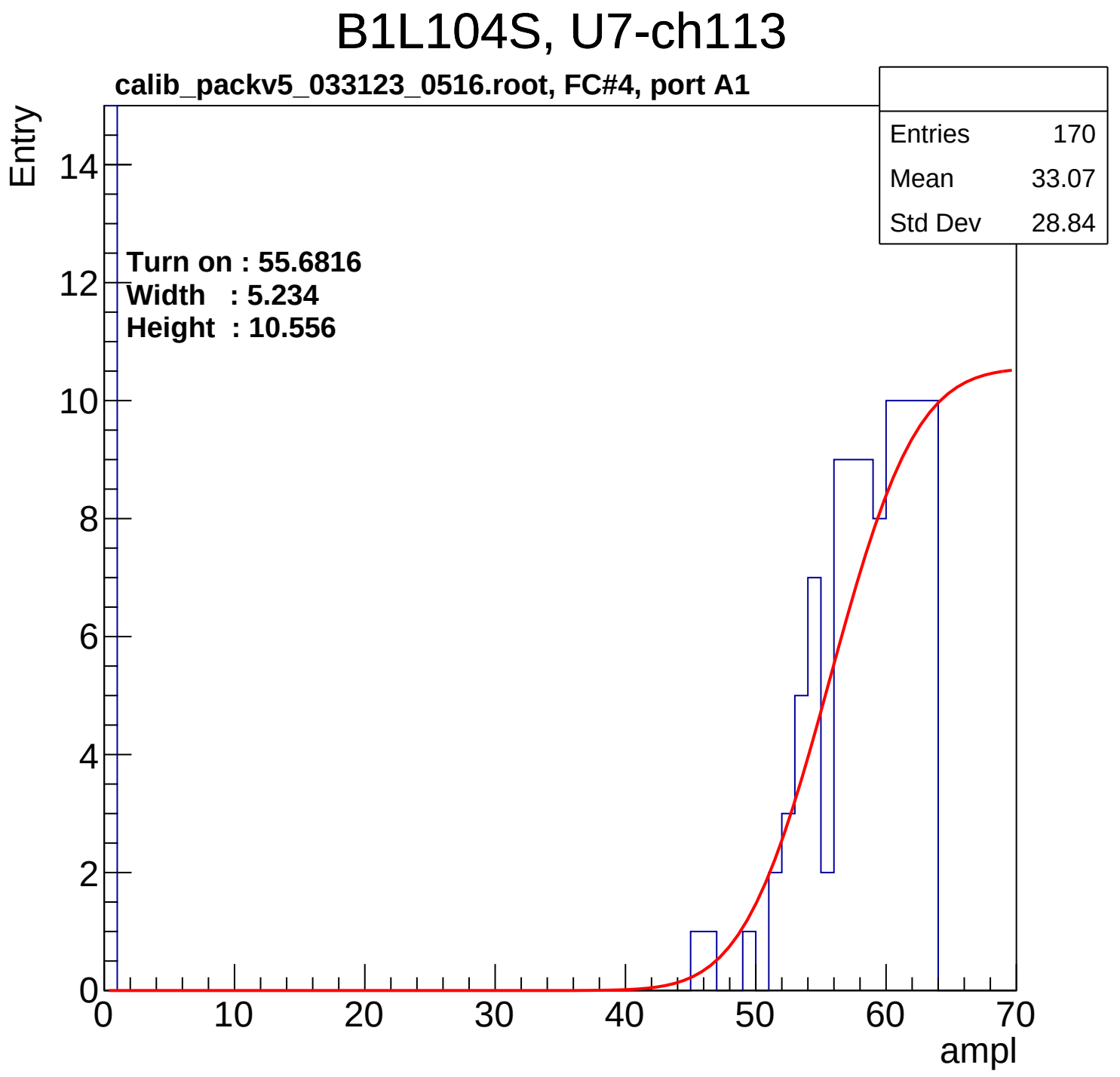

B1L104S, U7-ch108
calib_packv5_033123_0516.root, FC#4, port A1
Entries 208
Mean 30.94
Std Dev 28.8
Turn on : 53.6306
Width : 3.652
Height : 10.517
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

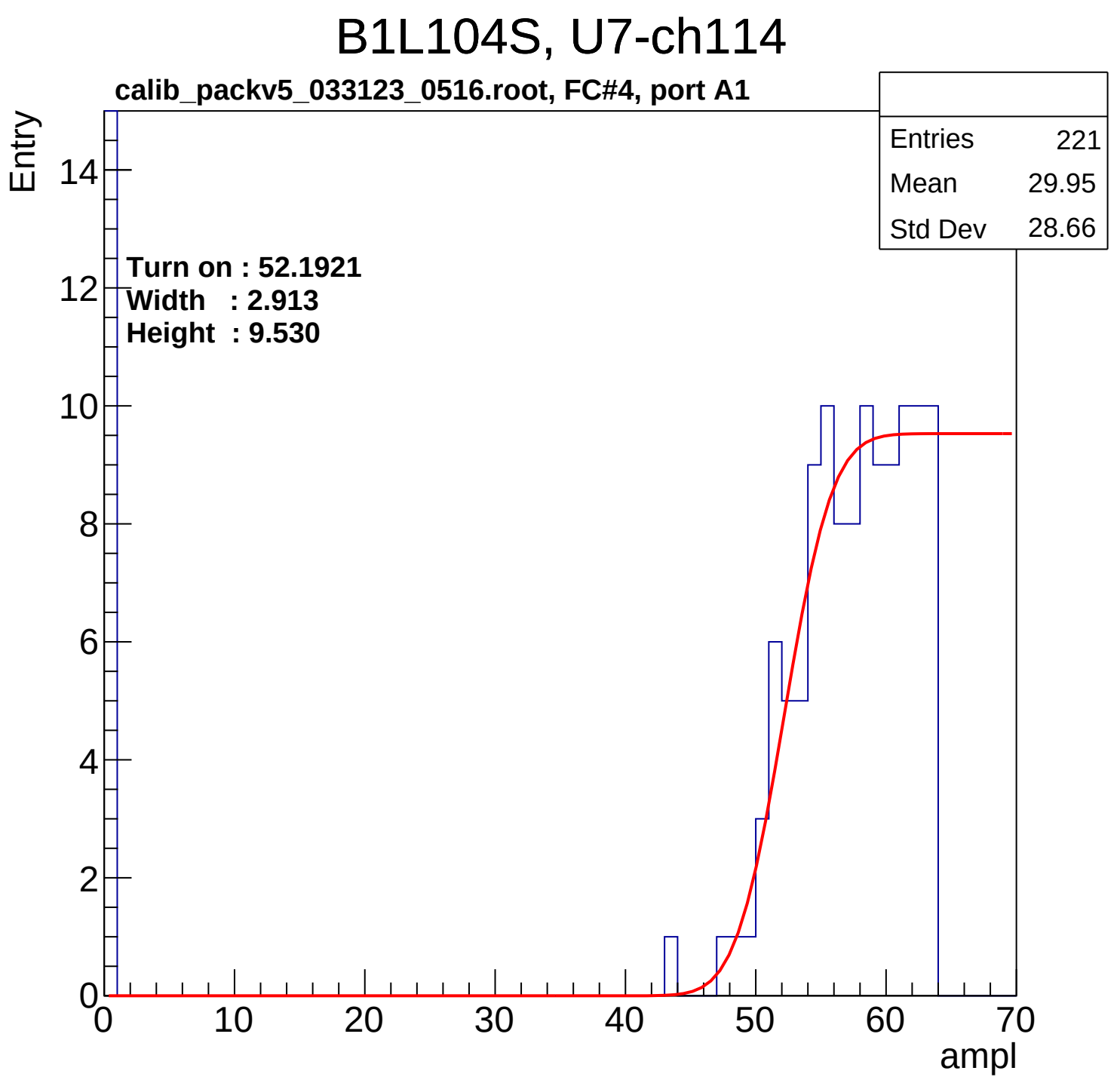

B1L104S, U7-ch109
calib_packv5_033123_0516.root, FC#4, port A1
Entries 195
Mean 34.06
Std Dev 28.27
Turn on : 52.3772
Width : 2.767
Height : 9.815
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

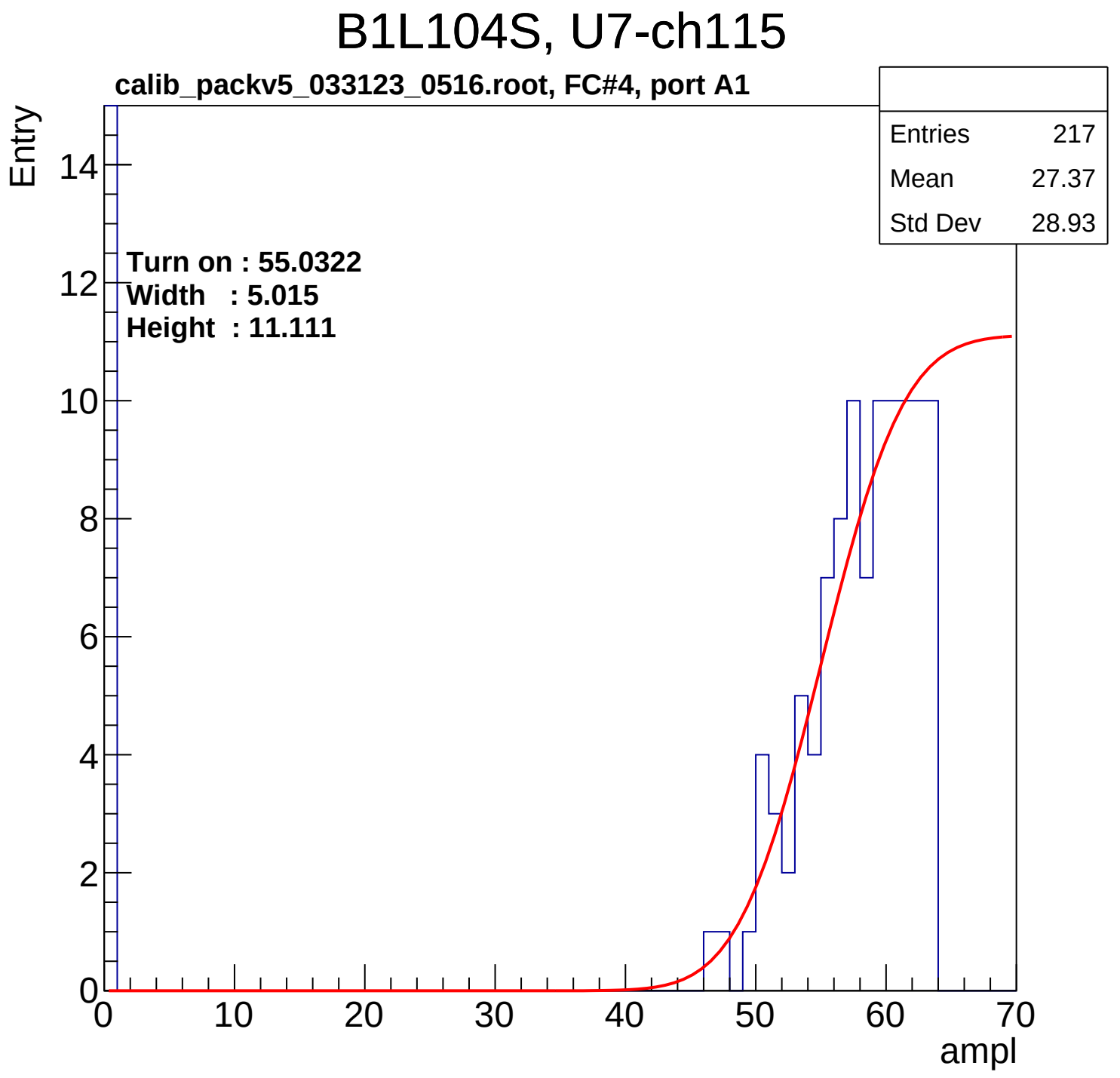

B1L104S, U7-ch110
calib_packv5_033123_0516.root, FC#4, port A1
Entries 191
Mean 32.06
Std Dev 28.84
Turn on : 53.8837
Width : 2.540
Height : 9.996
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

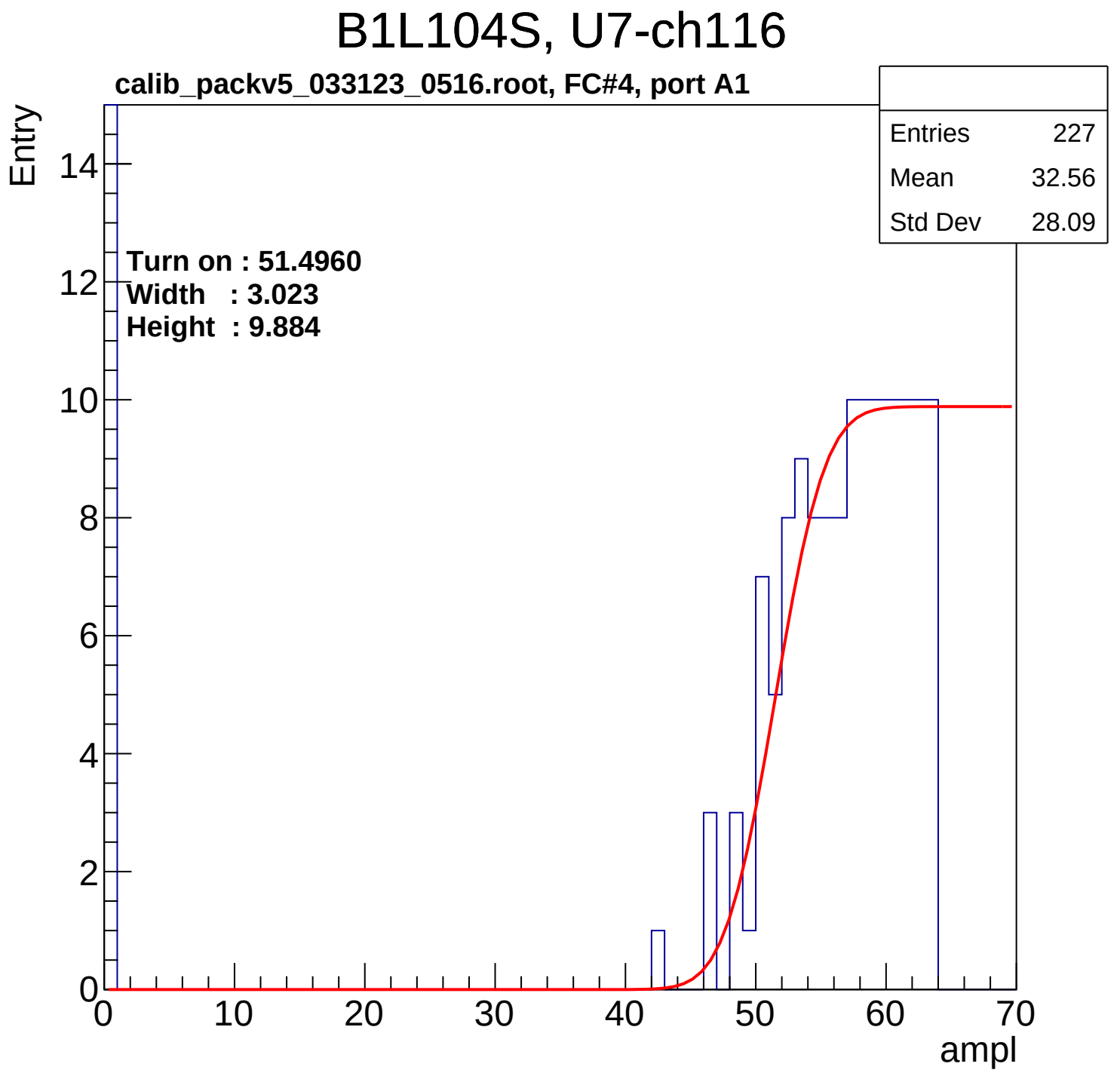

B1L104S, U7-ch111
calib_packv5_033123_0516.root, FC#4, port A1
Entries 204
Mean 28.74
Std Dev 29.13
Turn on : 54.5312
Width : 3.682
Height : 10.475
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

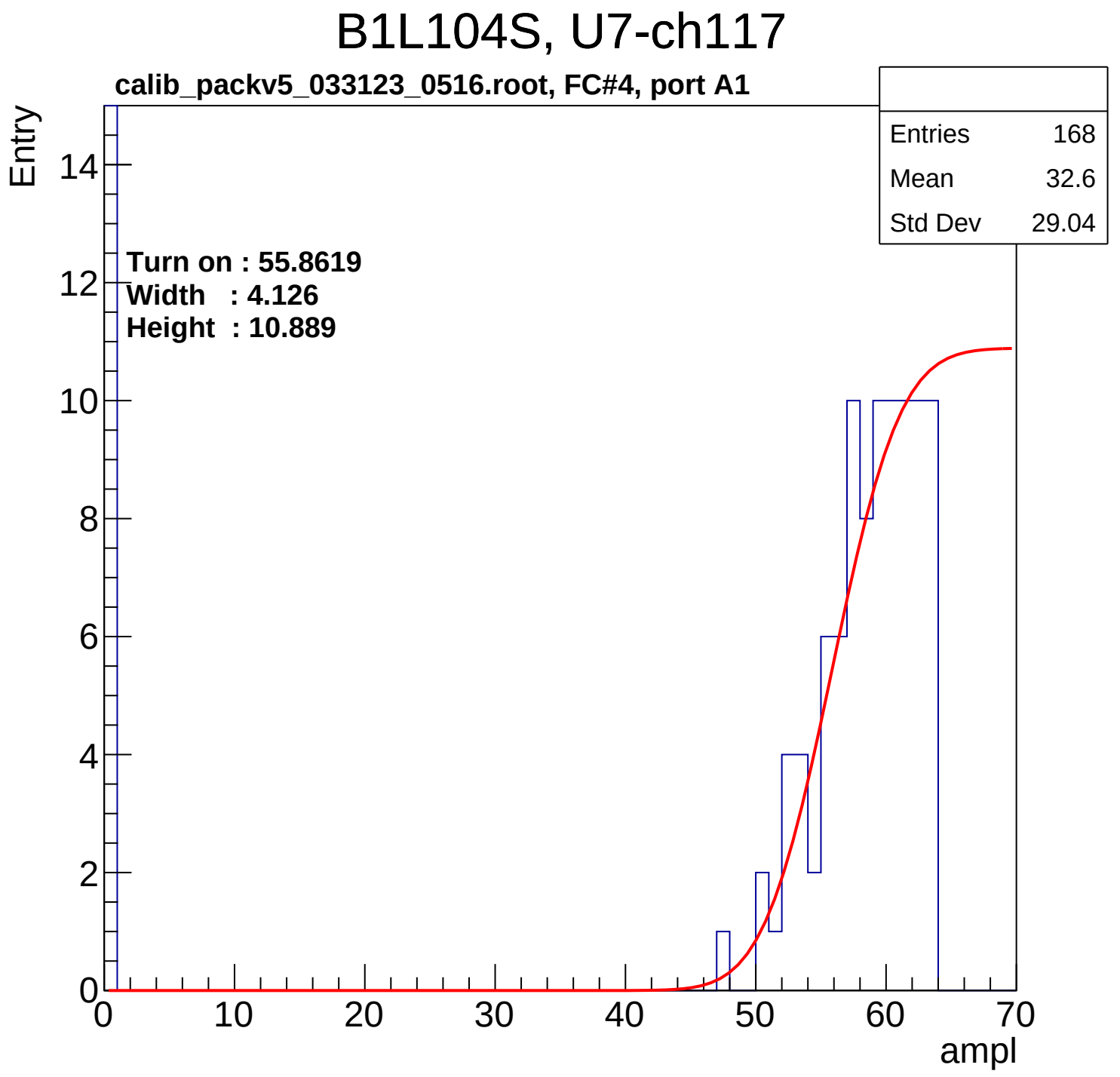

B1L104S, U7-ch112
calib_packv5_033123_0516.root, FC#4, port A1
Entries 190
Mean 31.88
Std Dev 28.58
Turn on : 54.4634
Width : 5.912
Height : 10.778
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

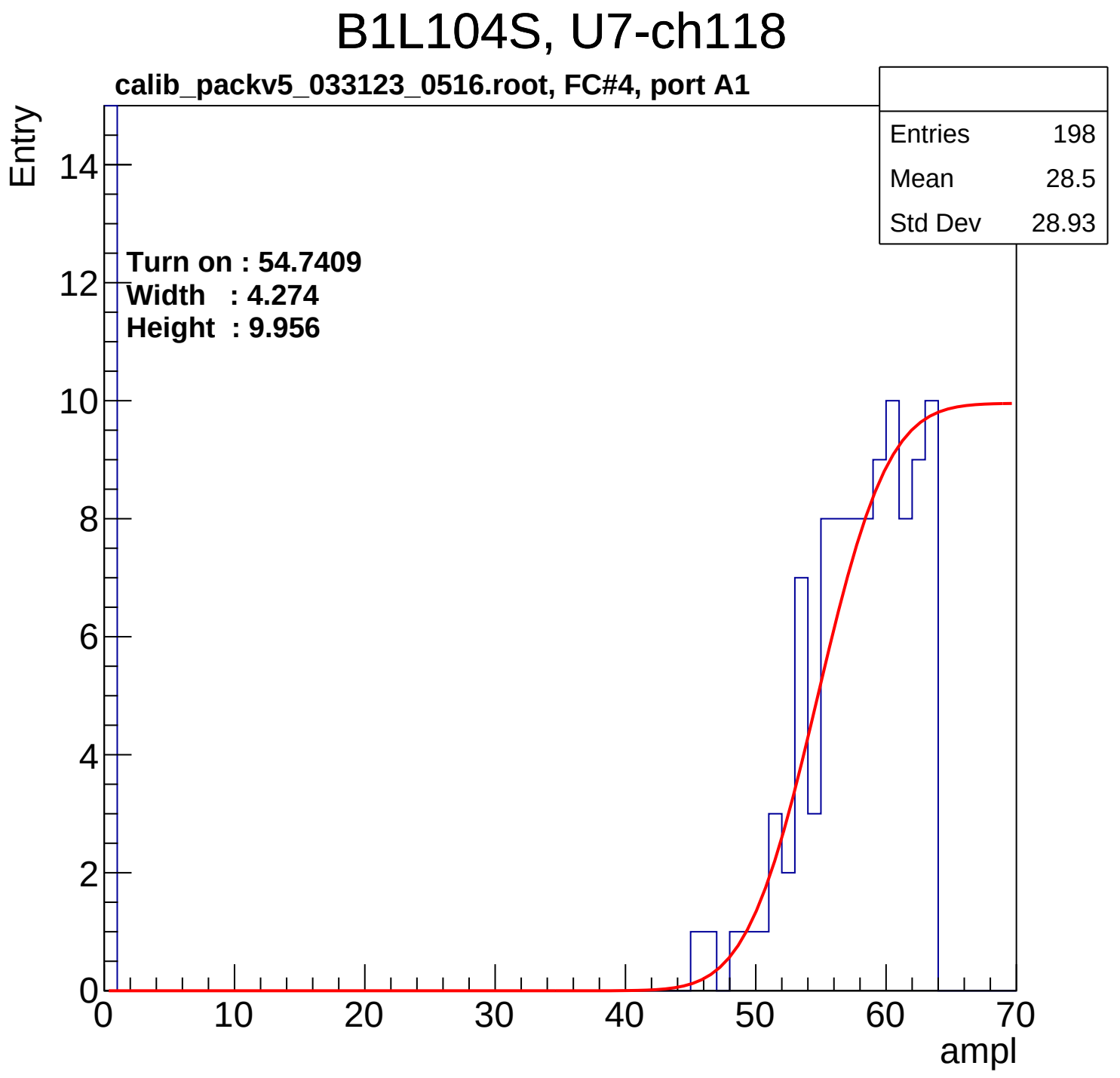

B1L104S, U7-ch113
calib_packv5_033123_0516.root, FC#4, port A1
Entries 170
Mean 33.07
Std Dev 28.84
Turn on : 55.6816
Width : 5.234
Height : 10.556
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

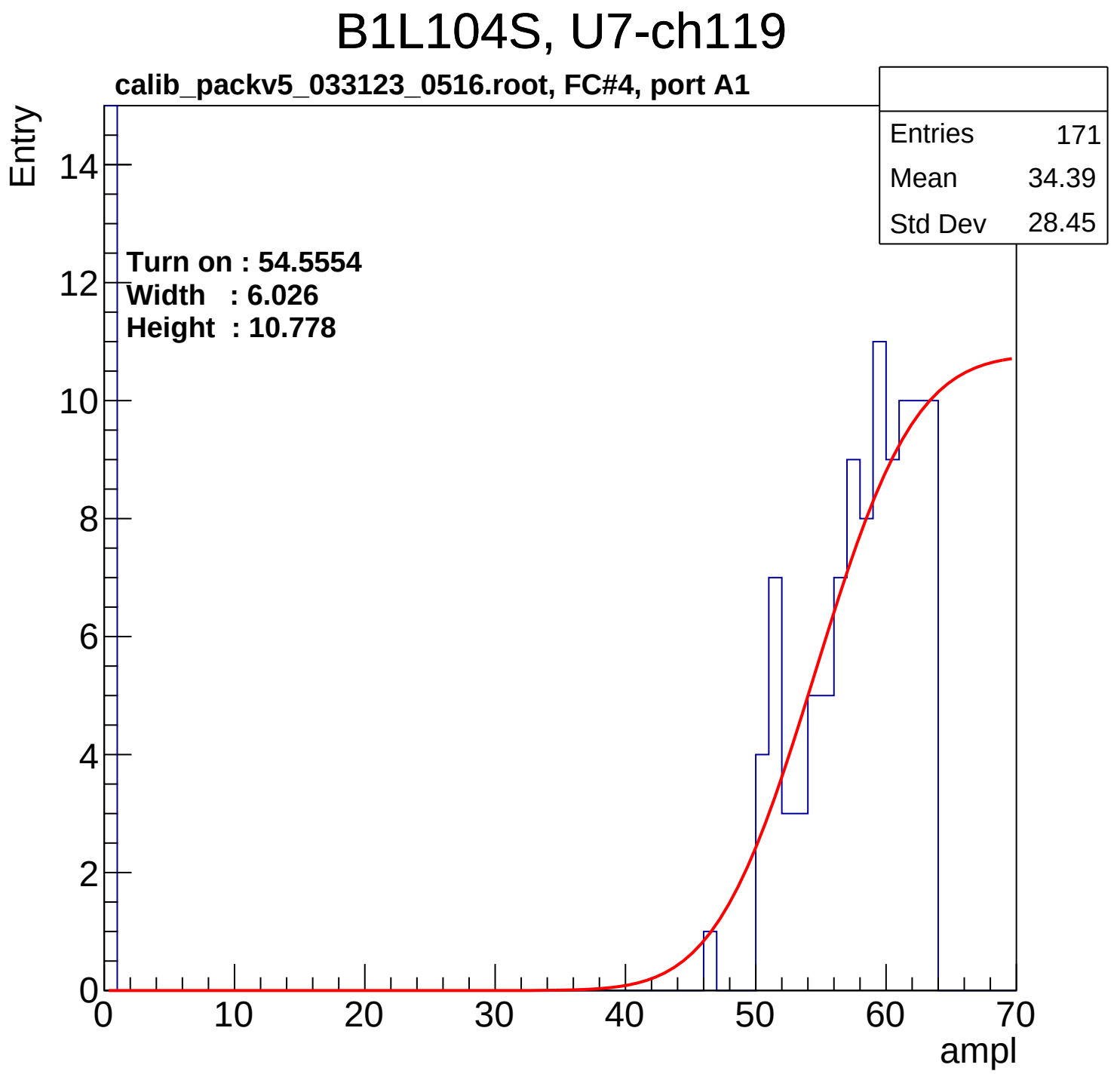

B1L104S, U7-ch114
calib_packv5_033123_0516.root, FC#4, port A1
Entries 221
Mean 29.95
Std Dev 28.66
Turn on : 52.1921
Width : 2.913
Height : 9.530
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

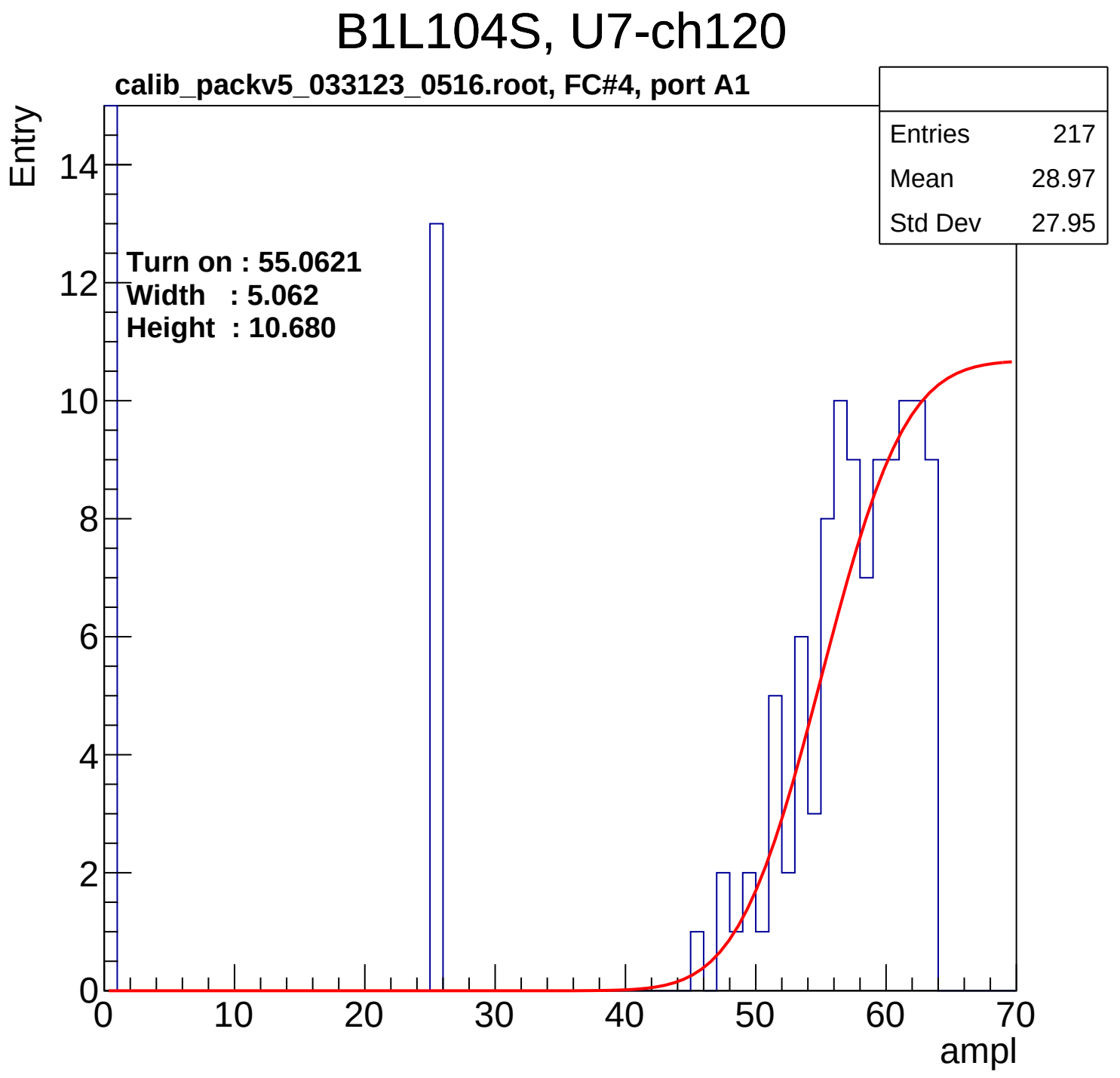

B1L104S, U7-ch115
calib_packv5_033123_0516.root, FC#4, port A1
Entries 217
Mean 27.37
Std Dev 28.93
Turn on : 55.0322
Width : 5.015
Height : 11.111
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

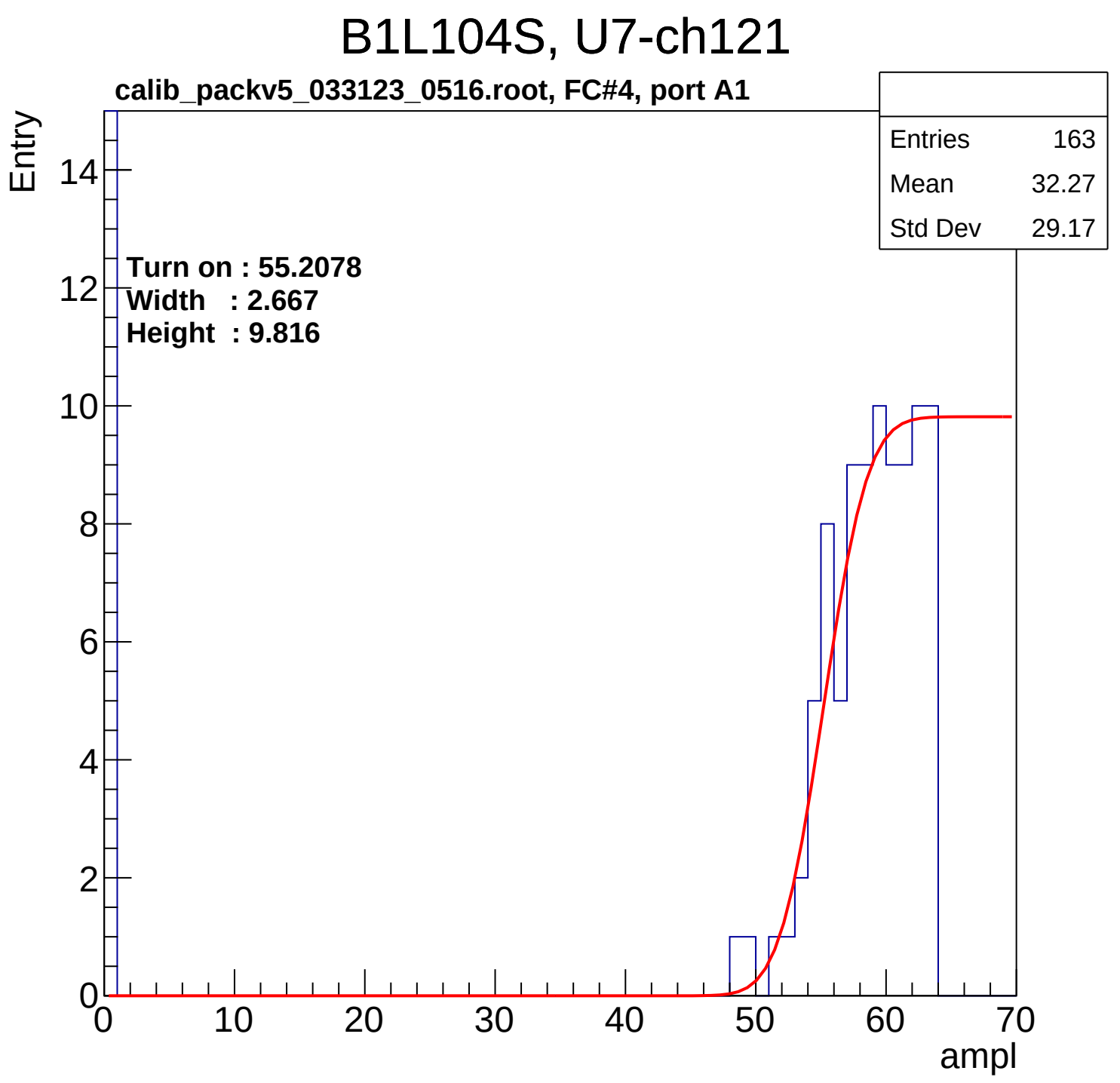

B1L104S, U7-ch116
calib_packv5_033123_0516.root, FC#4, port A1
Entries 227
Mean 32.56
Std Dev 28.09
Turn on : 51.4960
Width : 3.023
Height : 9.884
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

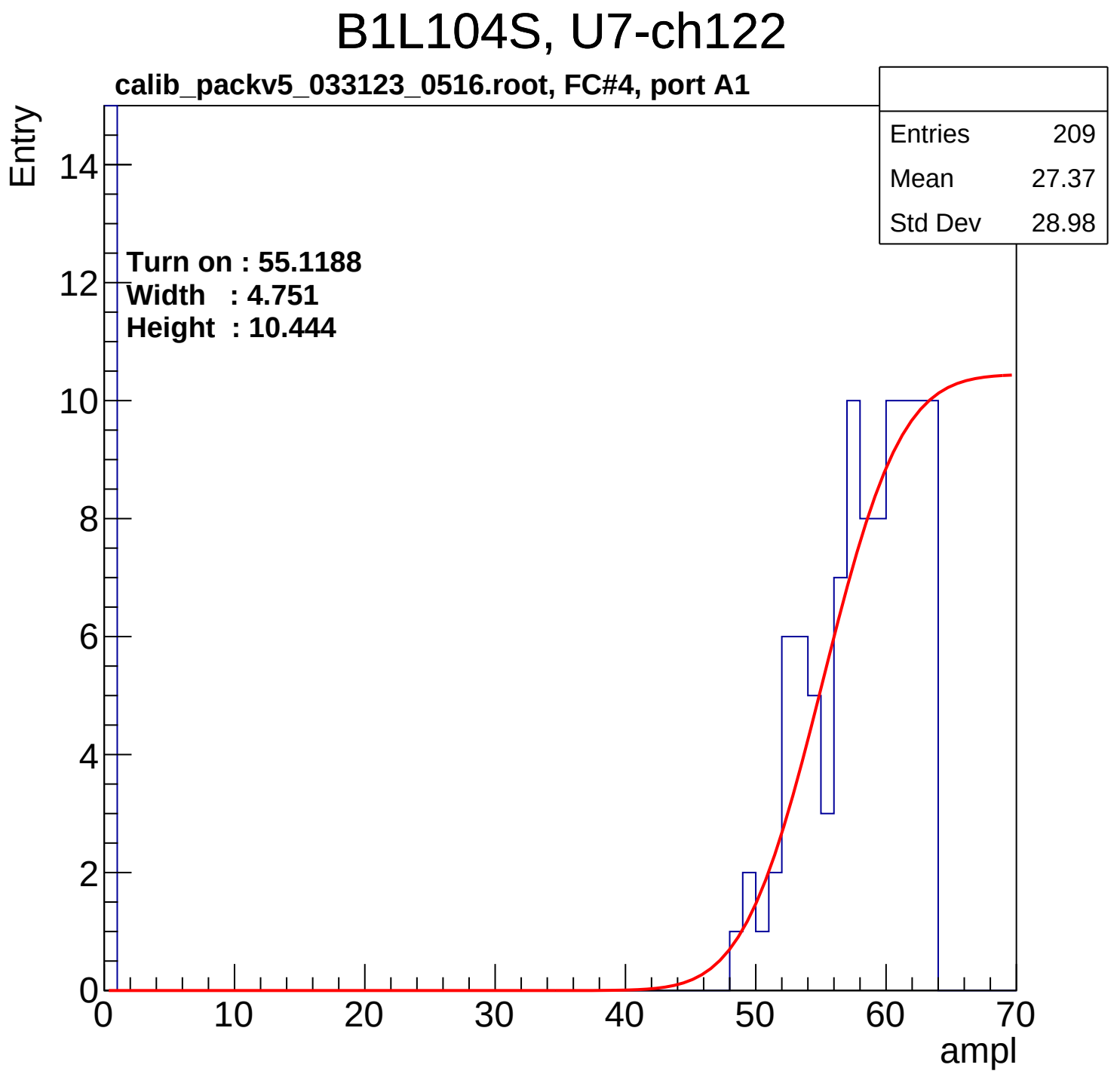

B1L104S, U7-ch117
calib_packv5_033123_0516.root, FC#4, port A1
Entries 168
Mean 32.6
Std Dev 29.04
Turn on : 55.8619
Width : 4.126
Height : 10.889
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

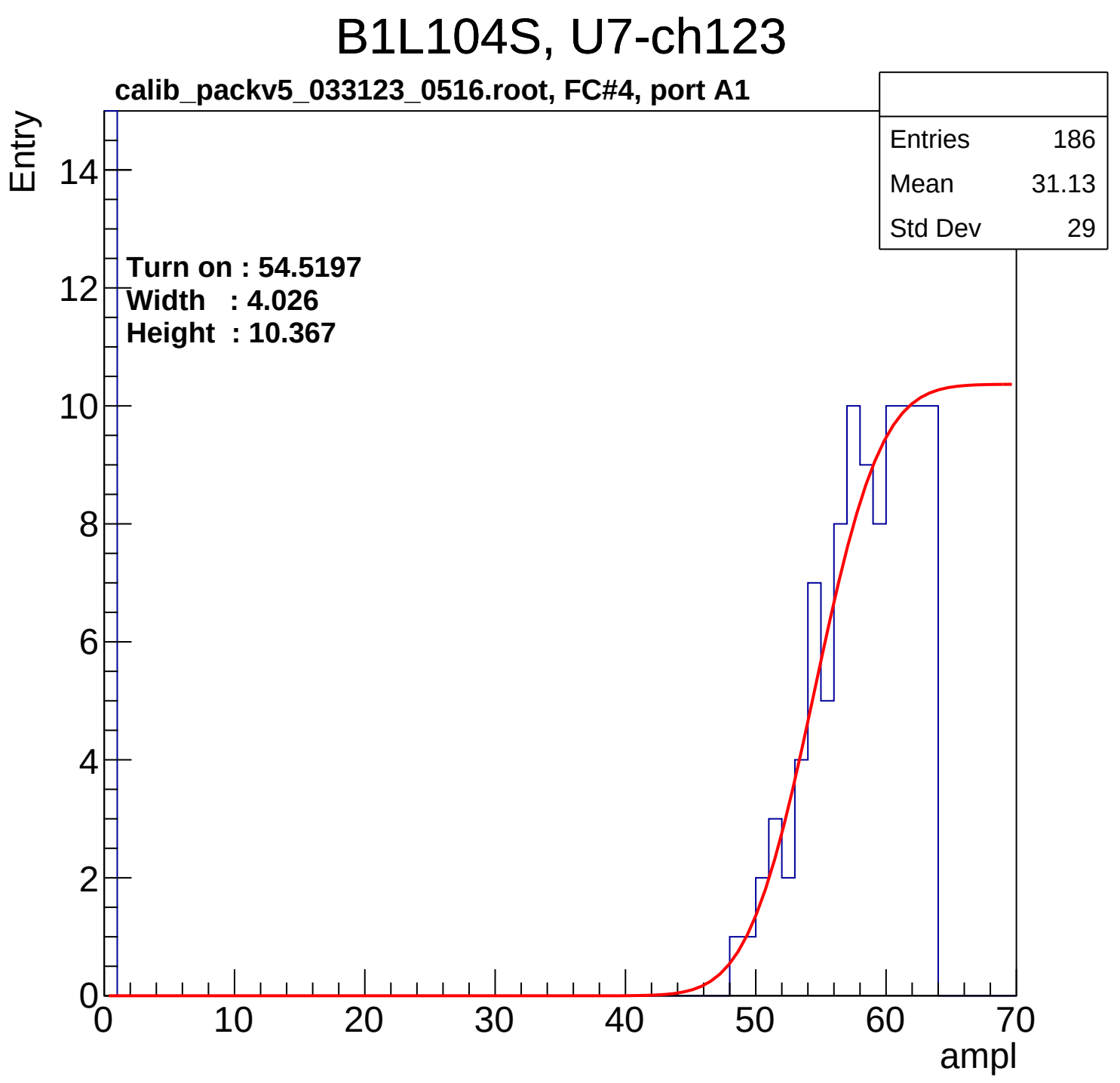

B1L104S, U7-ch118
calib_packv5_033123_0516.root, FC#4, port A1
Entries 198
Mean 28.5
Std Dev 28.93
Turn on : 54.7409
Width : 4.274
Height : 9.956
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

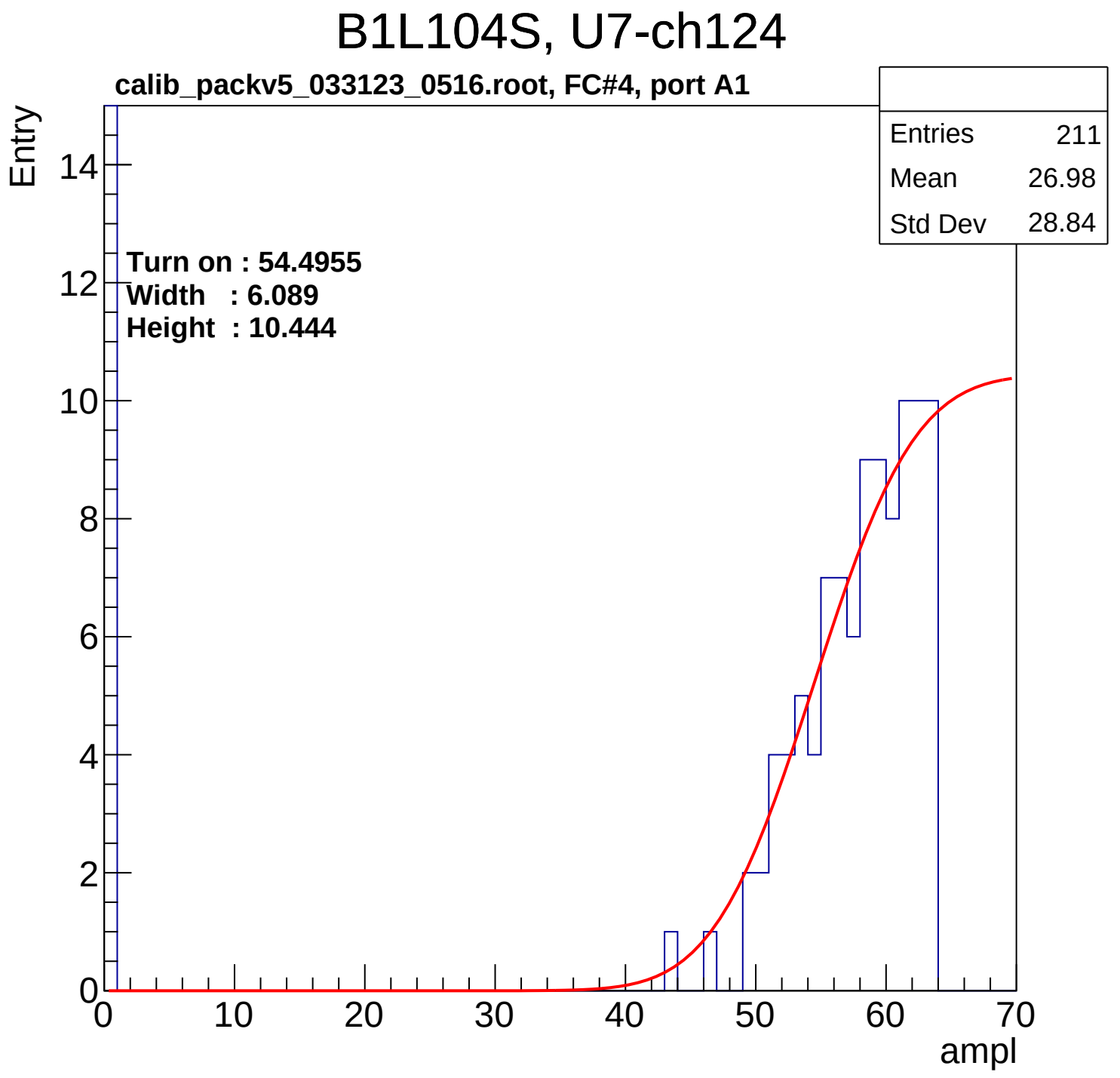

B1L104S, U7-ch119
calib_packv5_033123_0516.root, FC#4, port A1
Entries 171
Mean 34.39
Std Dev 28.45
Turn on : 54.5554
Width : 6.026
Height : 10.778
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

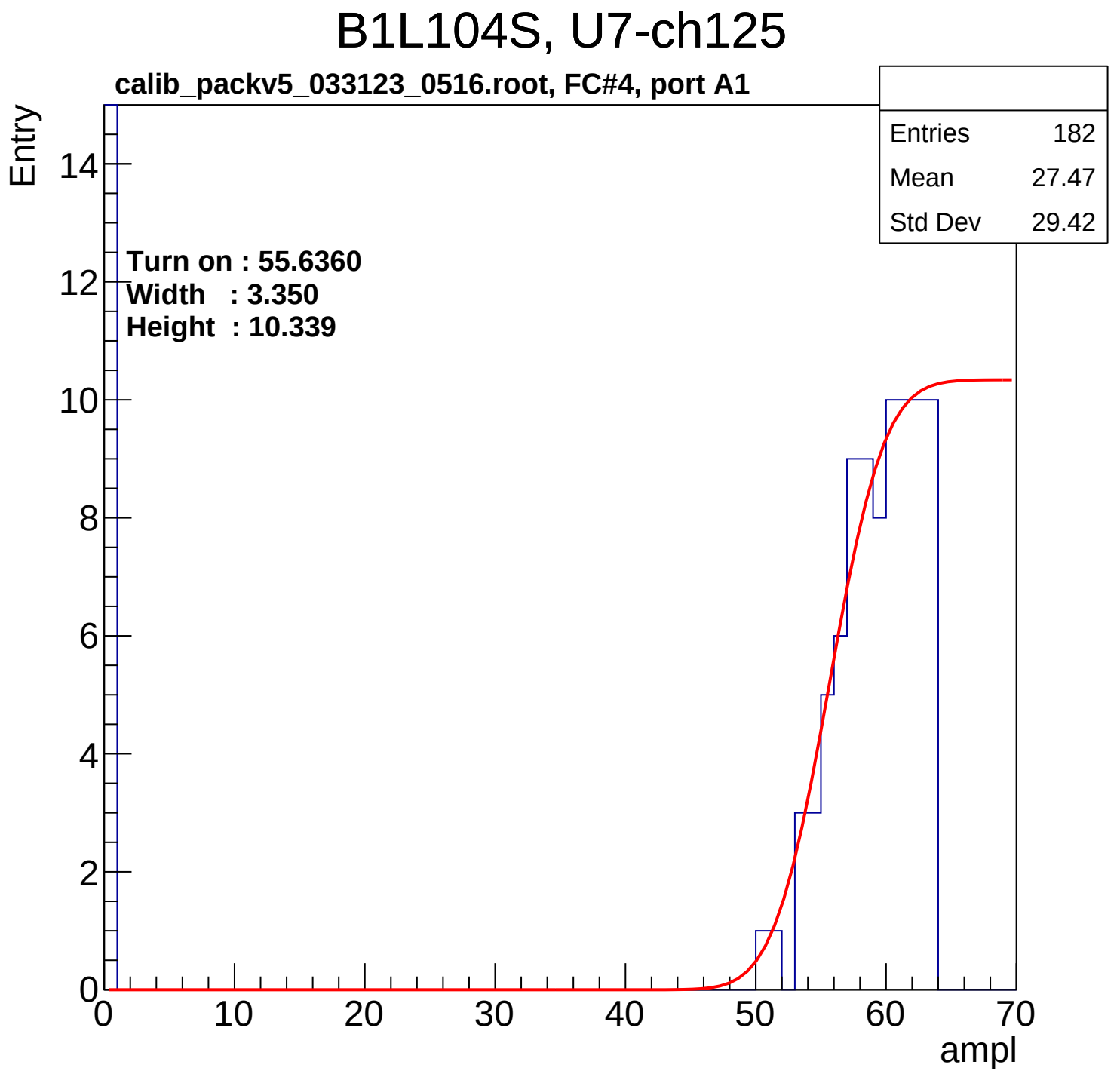

B1L104S, U7-ch120
calib_packv5_033123_0516.root, FC#4, port A1
Entries 217
Mean 28.97
Std Dev 27.95
Turn on : 55.0621
Width : 5.062
Height : 10.680
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

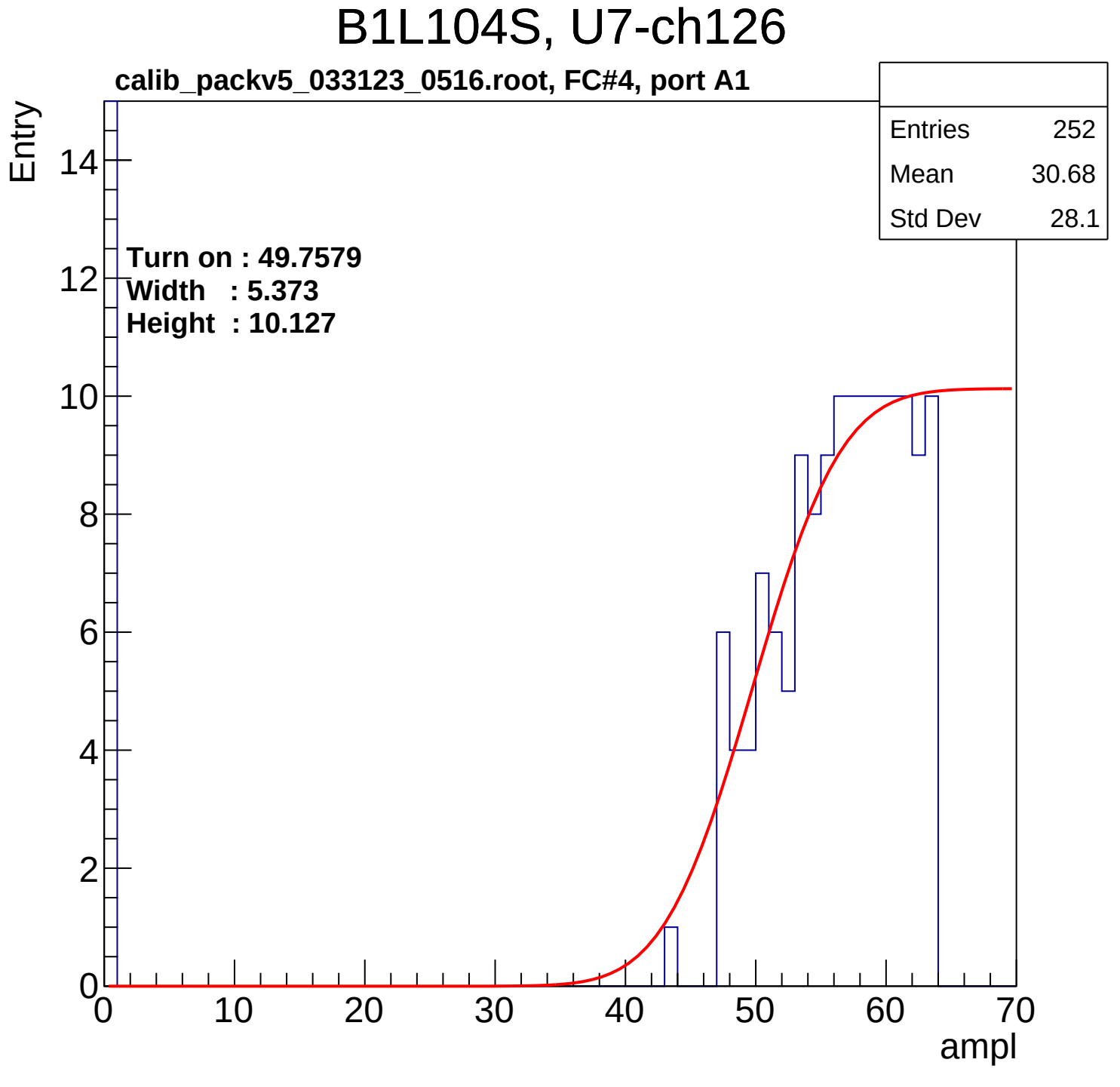

B1L104S, U7-ch121
calib_packv5_033123_0516.root, FC#4, port A1
Entries 163
Mean 32.27
Std Dev 29.17
Turn on : 55.2078
Width : 2.667
Height : 9.816
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

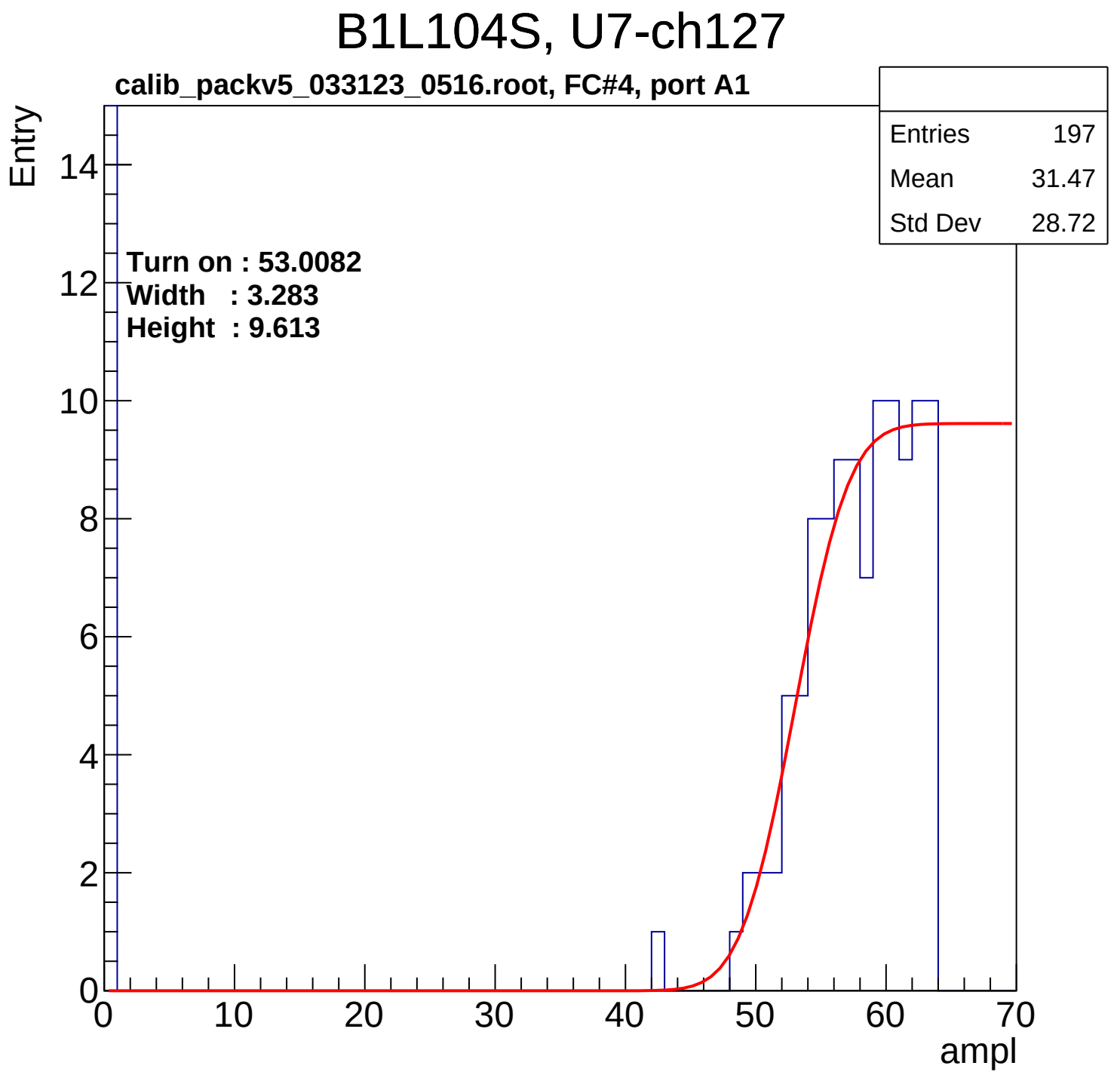

B1L104S, U7-ch122
calib_packv5_033123_0516.root, FC#4, port A1
Entries 209
Mean 27.37
Std Dev 28.98
Turn on : 55.1188
Width : 4.751
Height : 10.444
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

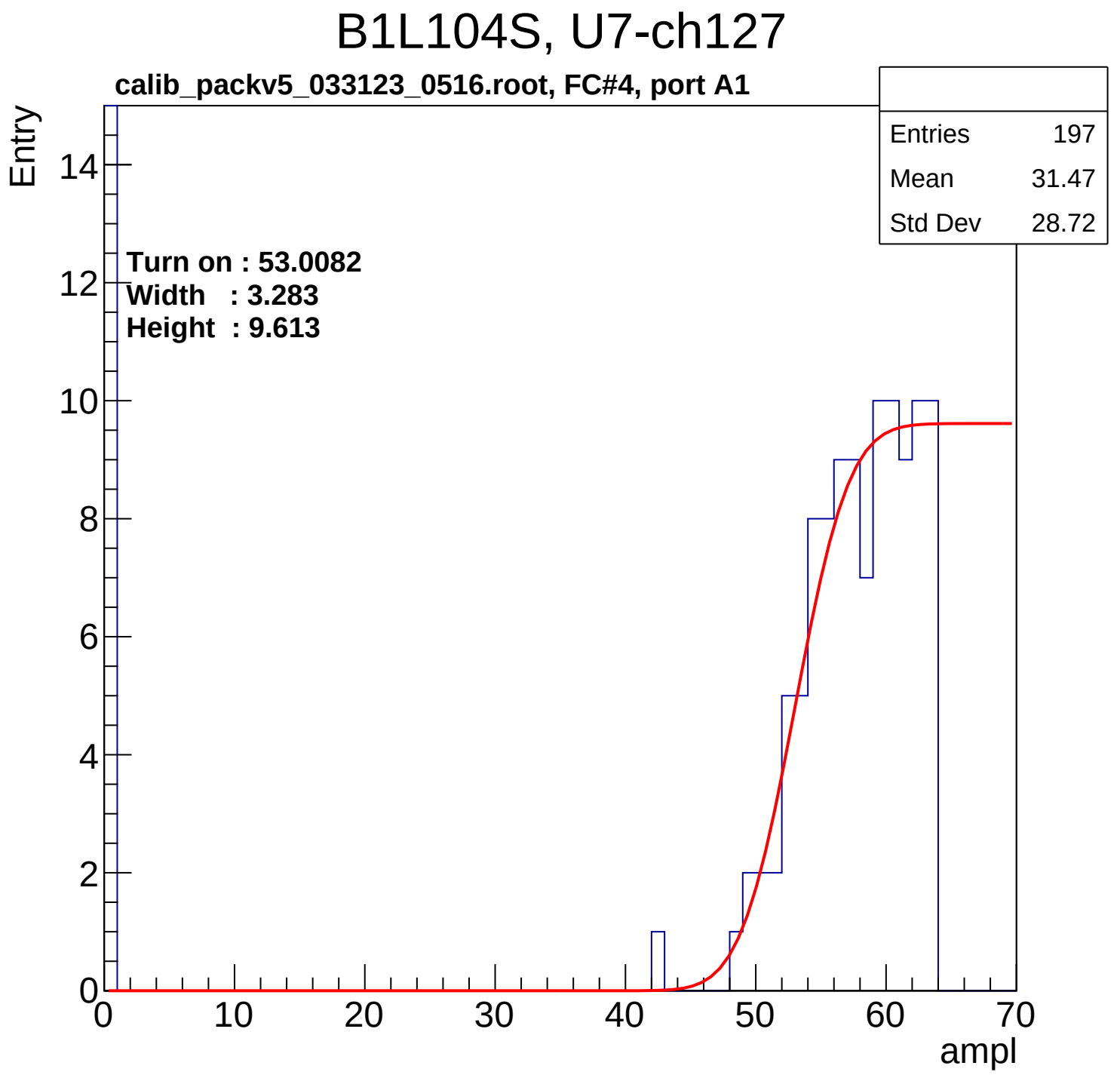

B1L104S, U7-ch123
calib_packv5_033123_0516.root, FC#4, port A1
Entries 186
Mean 31.13
Std Dev 29
Turn on : 54.5197
Width : 4.026
Height : 10.367
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U7-ch124
calib_packv5_033123_0516.root, FC#4, port A1
Entries 211
Mean 26.98
Std Dev 28.84
Turn on : 54.4955
Width : 6.089
Height : 10.444
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U7-ch125
calib_packv5_033123_0516.root, FC#4, port A1
Entries 182
Mean 27.47
Std Dev 29.42
Turn on : 55.6360
Width : 3.350
Height : 10.339
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U7-ch126
calib_packv5_033123_0516.root, FC#4, port A1
Entries 252
Mean 30.68
Std Dev 28.1
Turn on : 49.7579
Width : 5.373
Height : 10.127
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U7-ch127
calib_packv5_033123_0516.root, FC#4, port A1
Entries 197
Mean 31.47
Std Dev 28.72
Turn on : 53.0082
Width : 3.283
Height : 9.613
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L104S, U7-ch127
calib_packv5_033123_0516.root, FC#4, port A1
Entries 197
Mean 31.47
Std Dev 28.72
Turn on : 53.0082
Width : 3.283
Height : 9.613
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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