



# B1L102S, U16-ch0, adc0

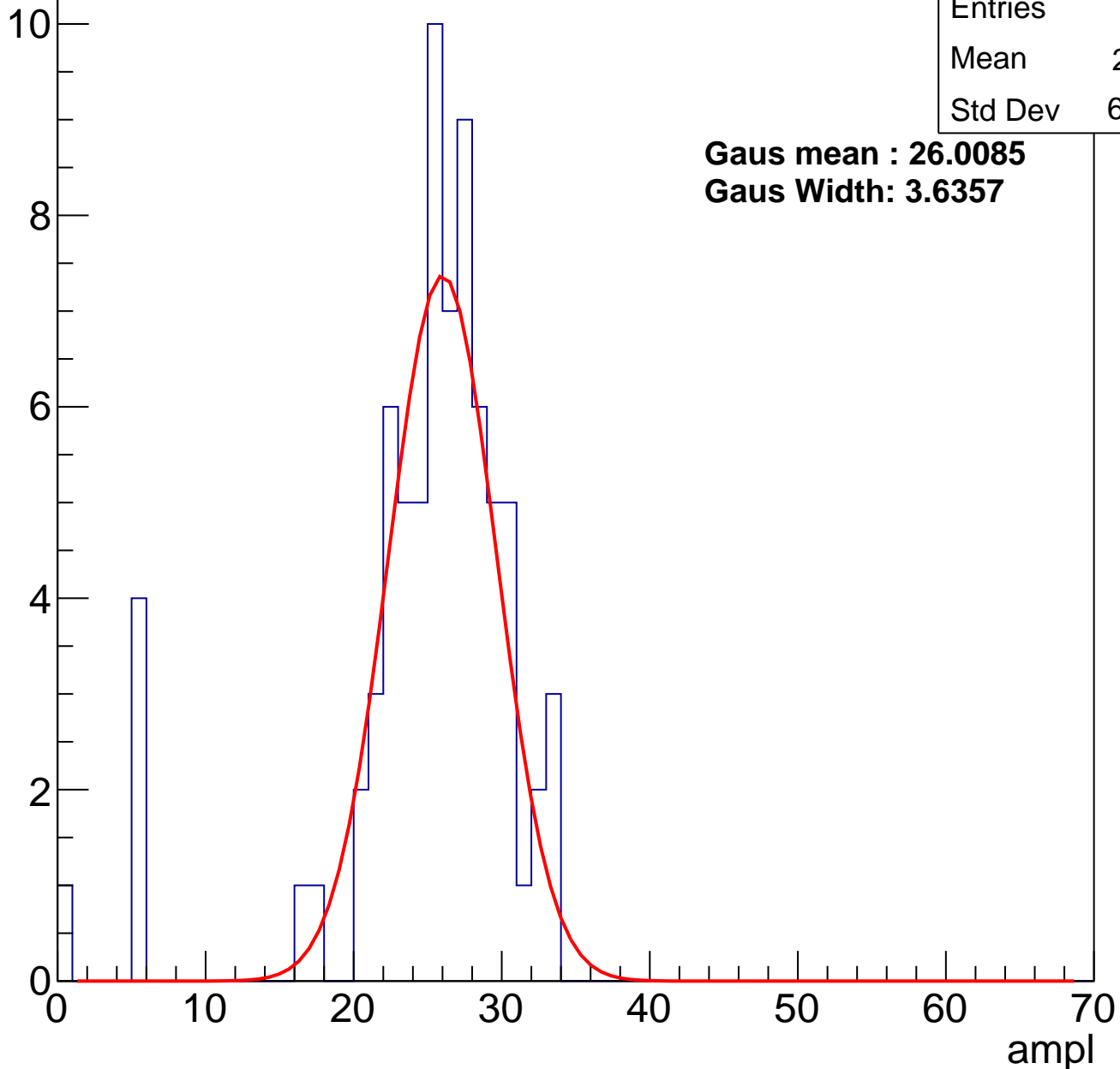
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	76
Mean	24.41
Std Dev	6.436

**Gaus mean : 26.0085**

**Gaus Width: 3.6357**

Entry



# B1L102S, U16-ch0, adc1

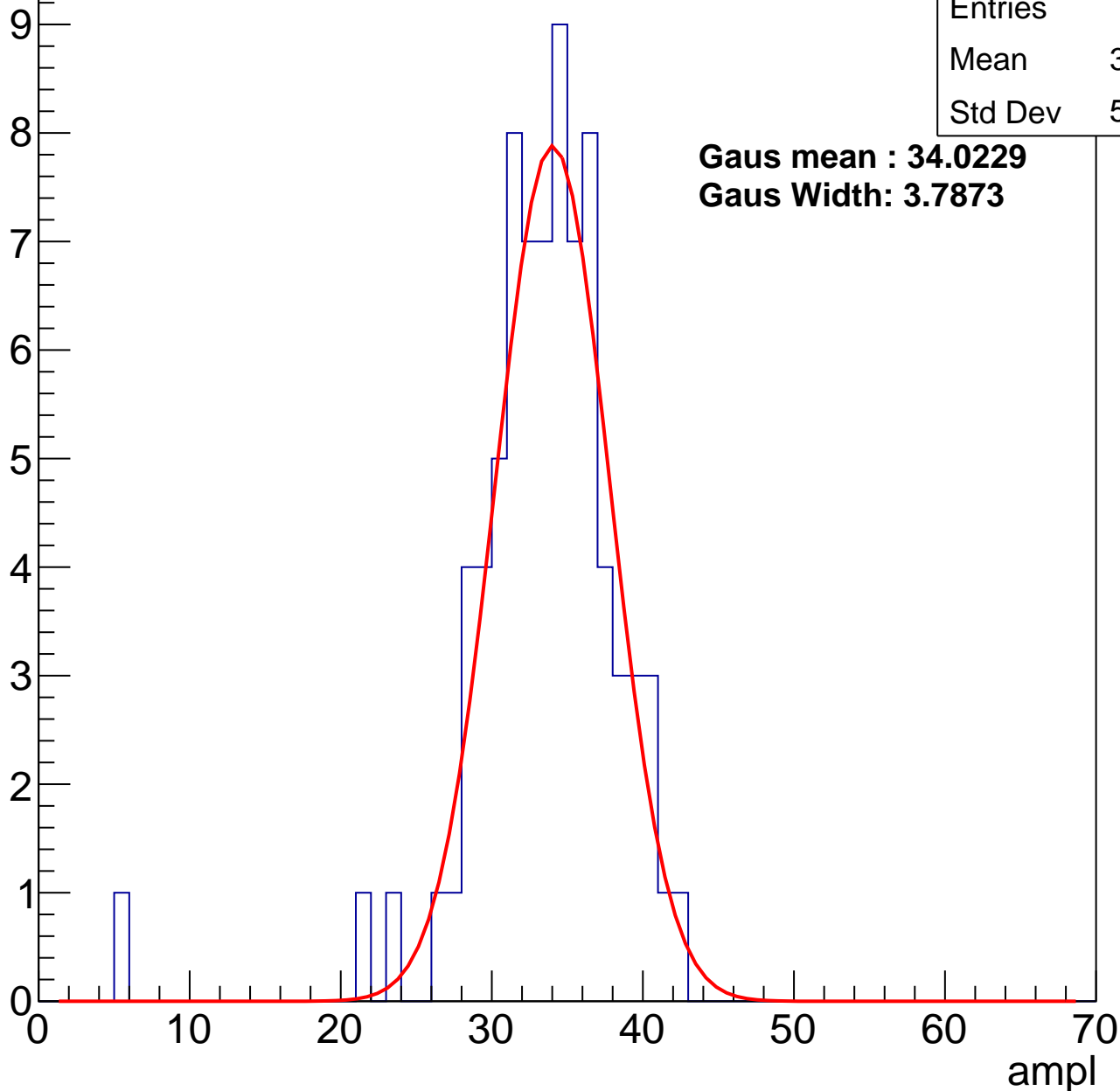
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	32.96
Std Dev	5.043

**Gaus mean : 34.0229**

**Gaus Width: 3.7873**



# B1L102S, U16-ch0, adc2

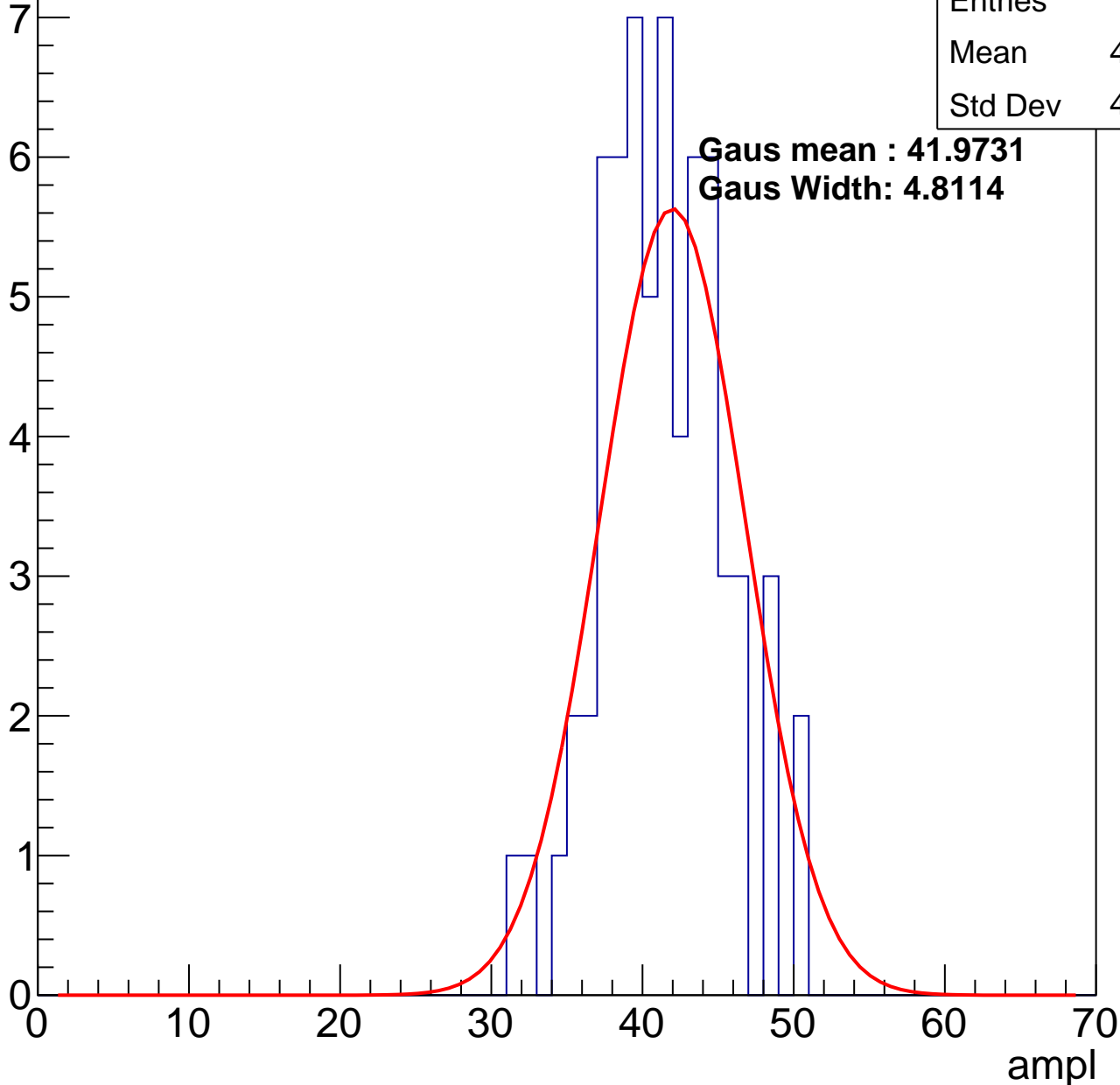
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	40.86
Std Dev	4.015

**Gaus mean : 41.9731**

**Gaus Width: 4.8114**

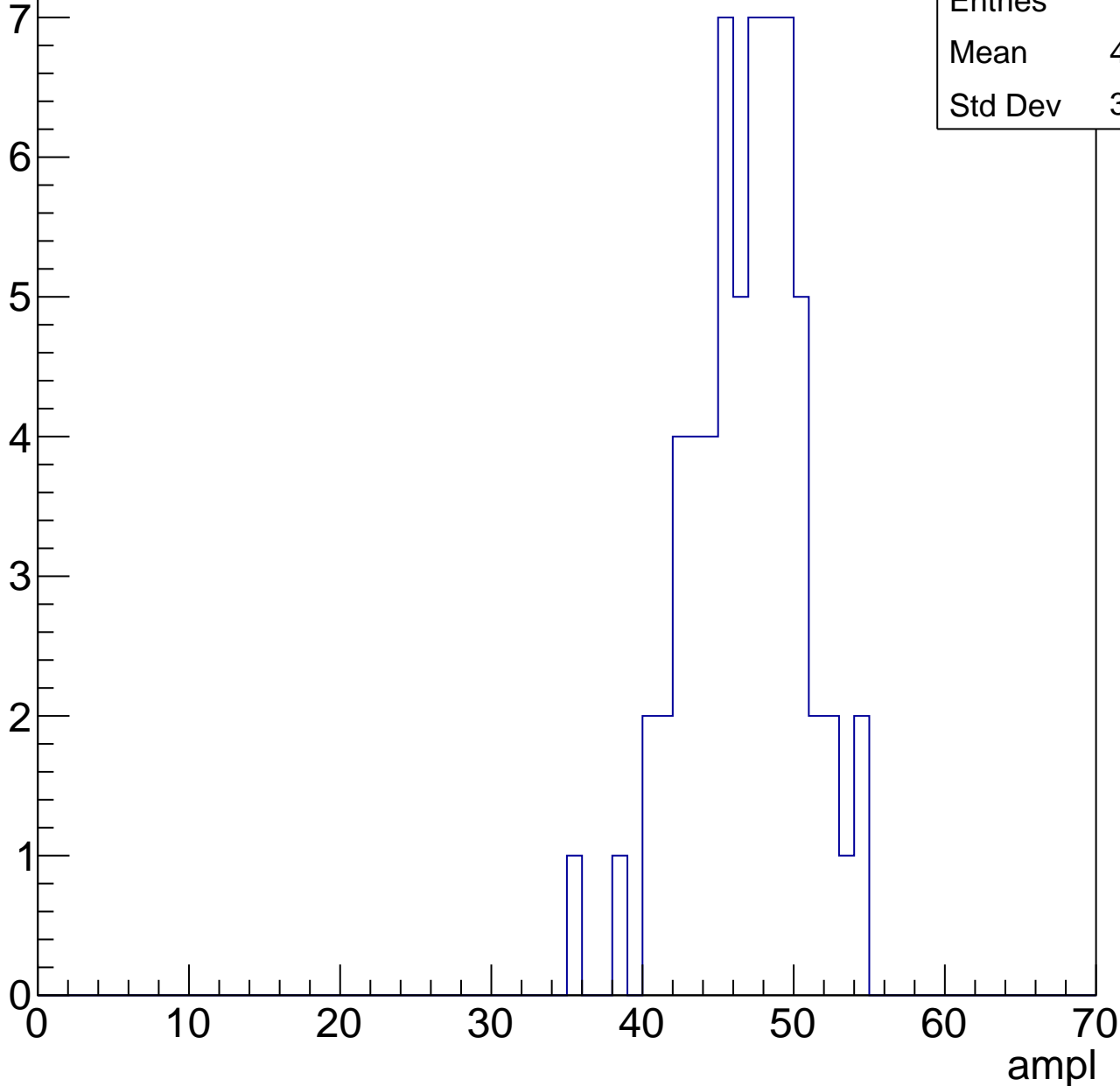


# B1L102S, U16-ch0, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	46.37
Std Dev	3.777

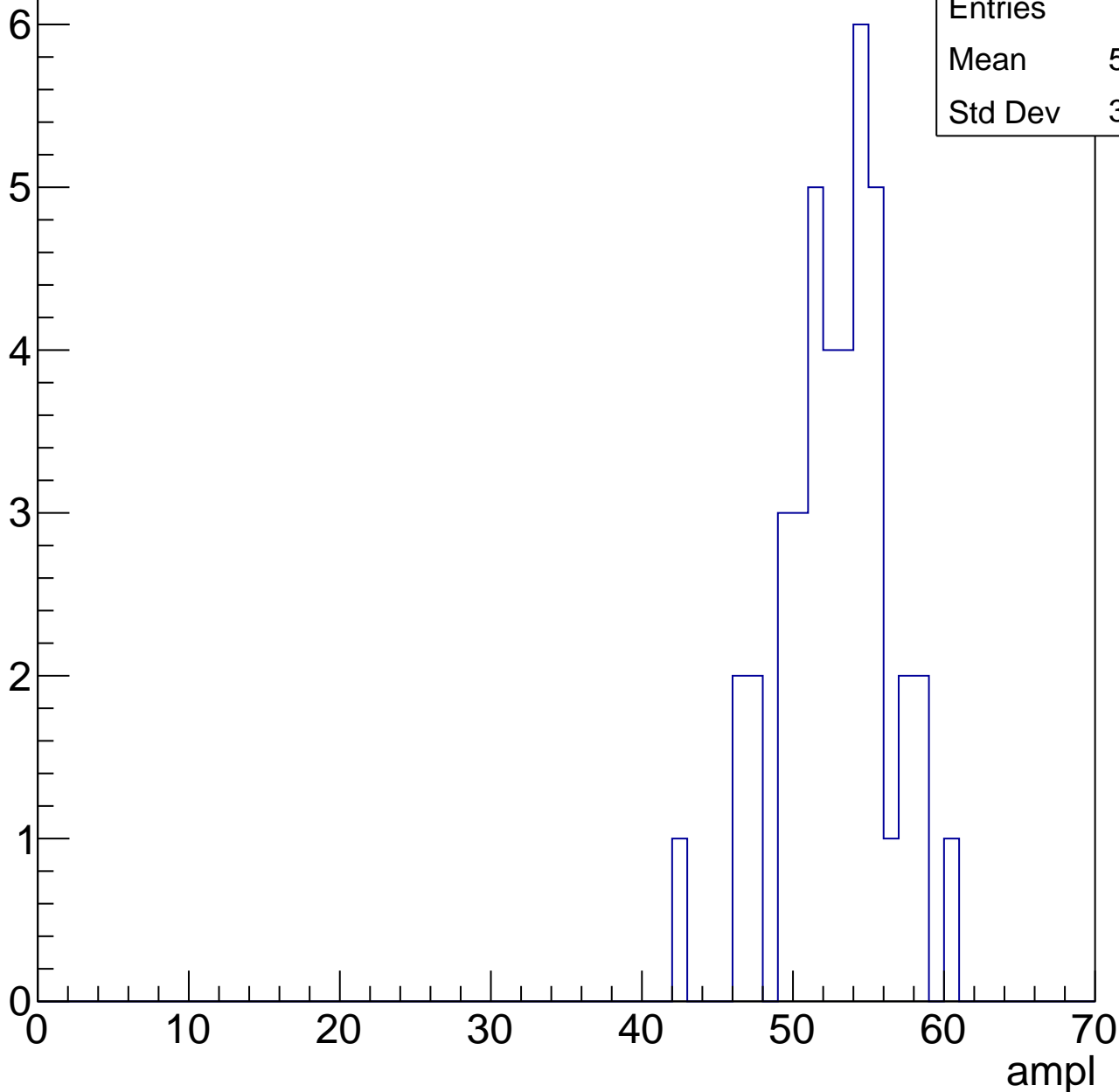


# B1L102S, U16-ch0, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

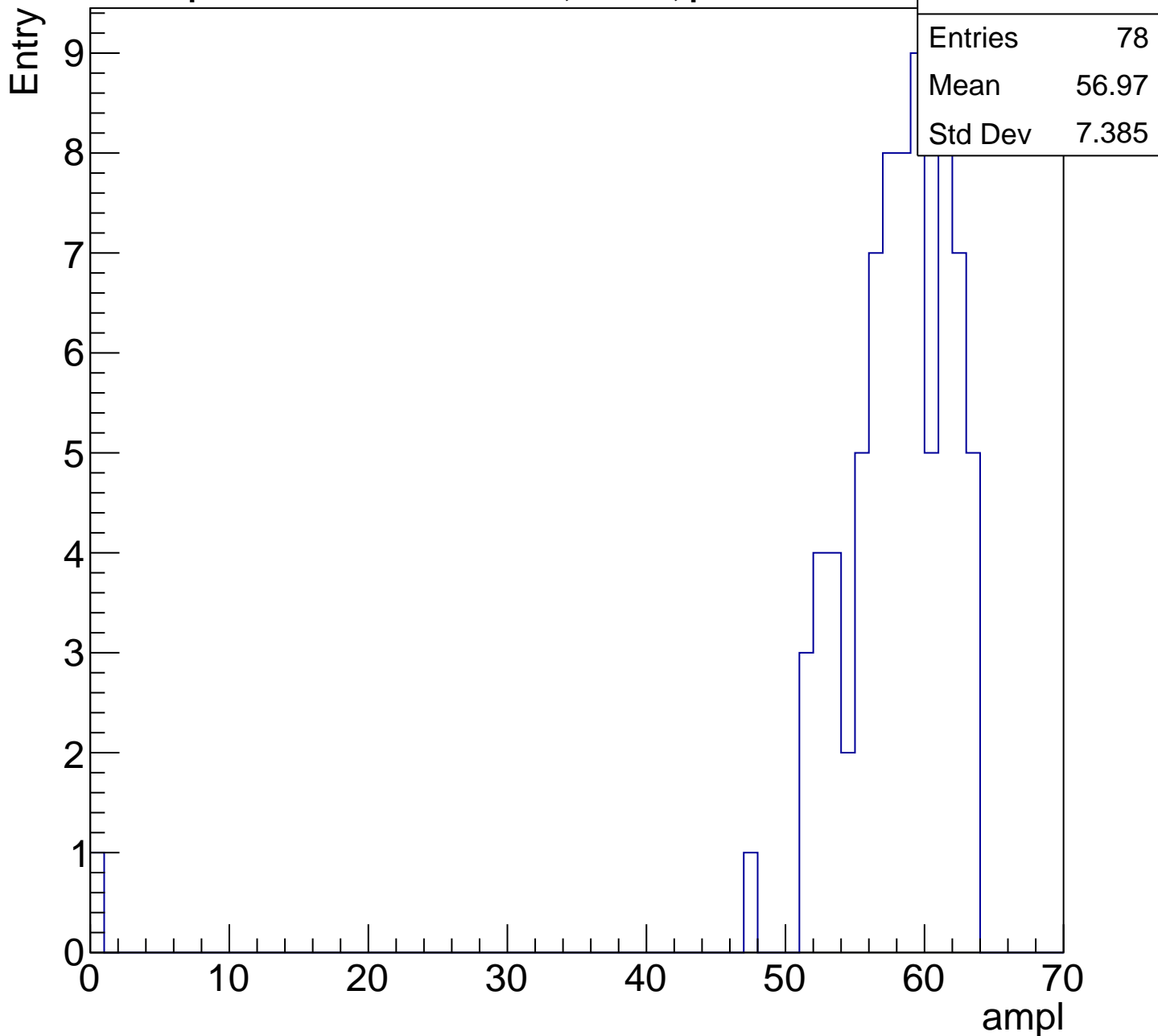
Entry

Entries	41
Mean	52.32
Std Dev	3.619



# B1L102S, U16-ch0, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

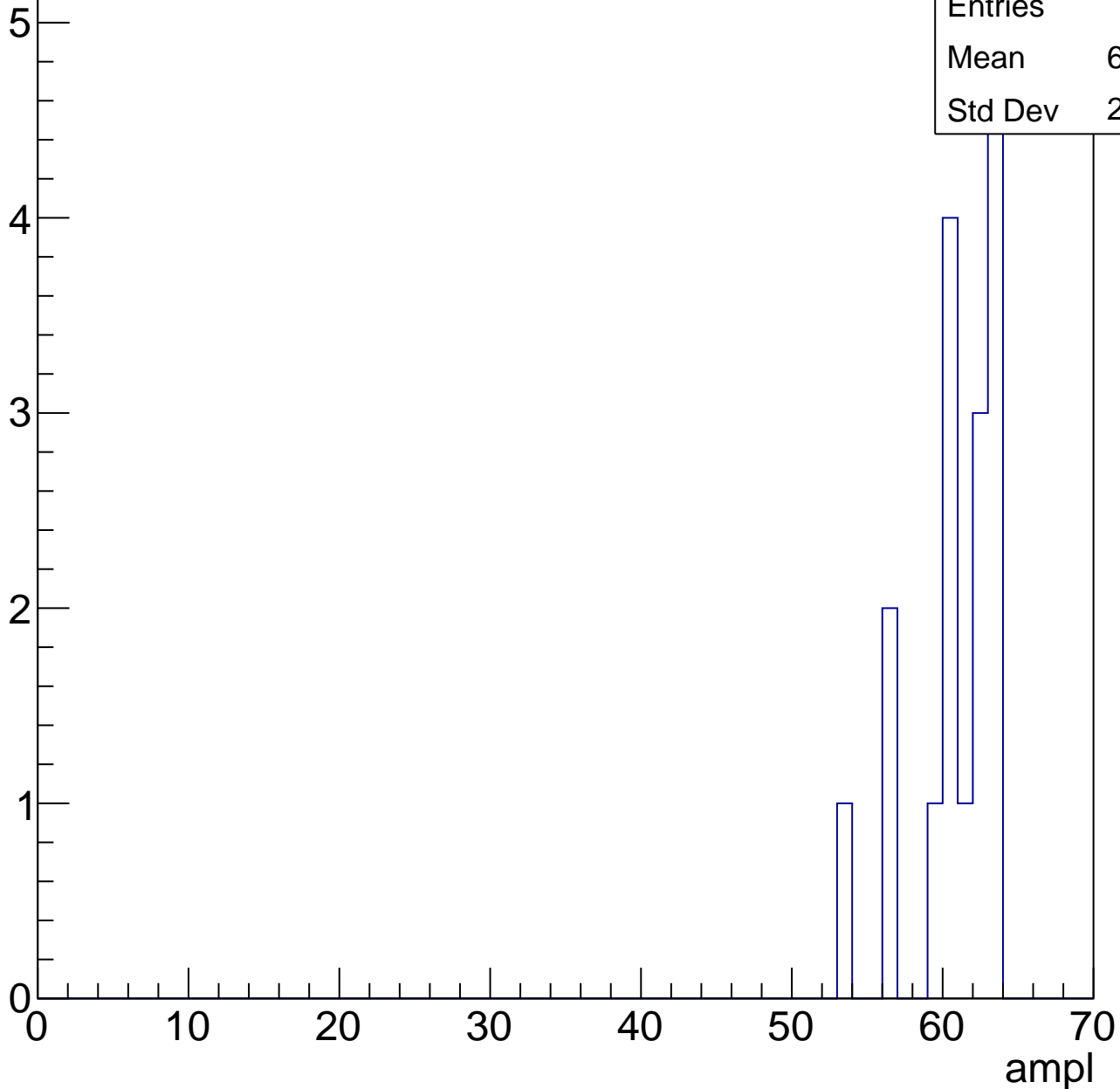


# B1L102S, U16-ch0, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	17
Mean	60.35
Std Dev	2.848





# B1L102S, U16-ch0, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U16-ch1, adc0

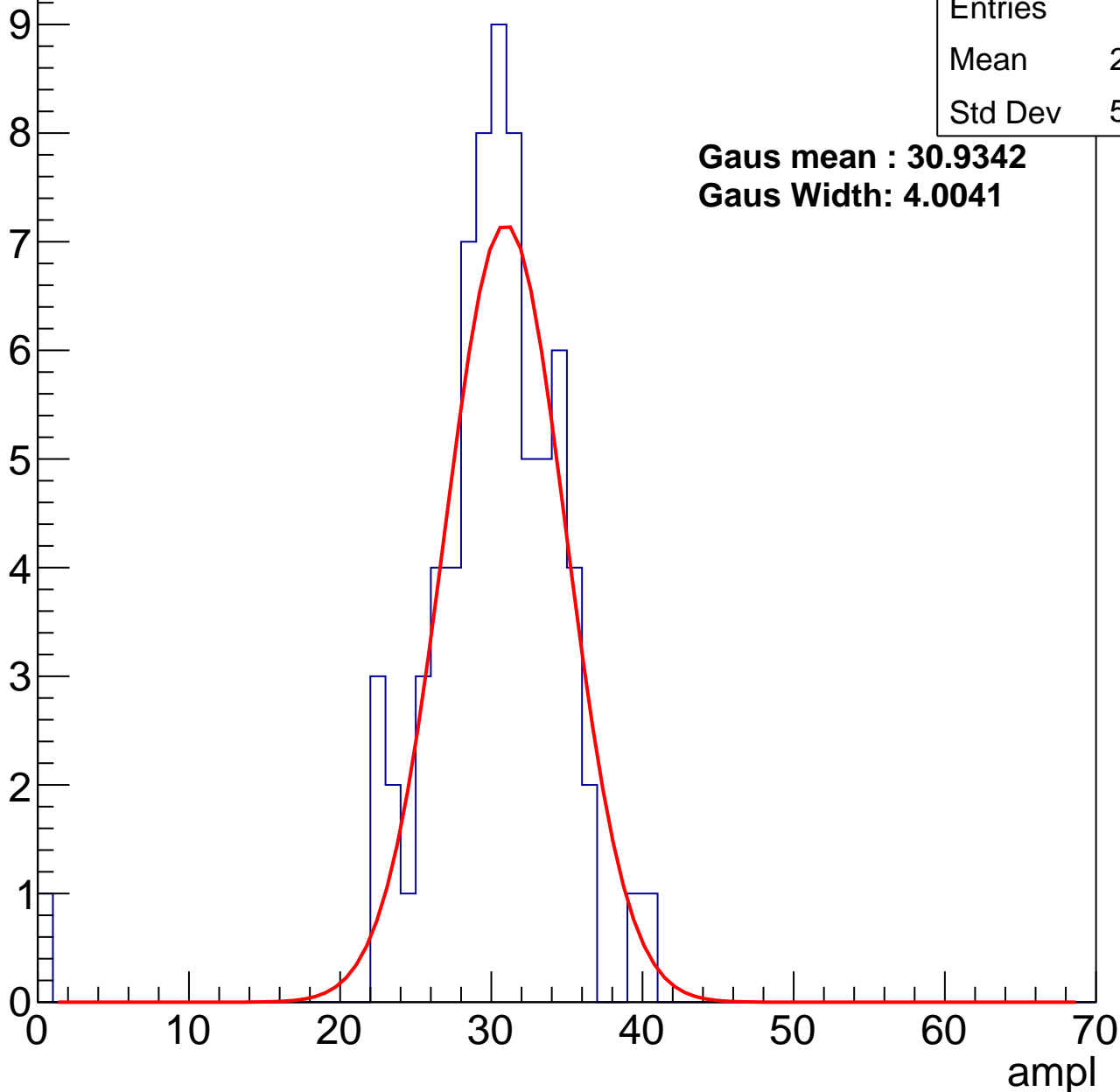
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	29.58
Std Dev	5.128

**Gaus mean : 30.9342**

**Gaus Width: 4.0041**



# B1L102S, U16-ch1, adc1

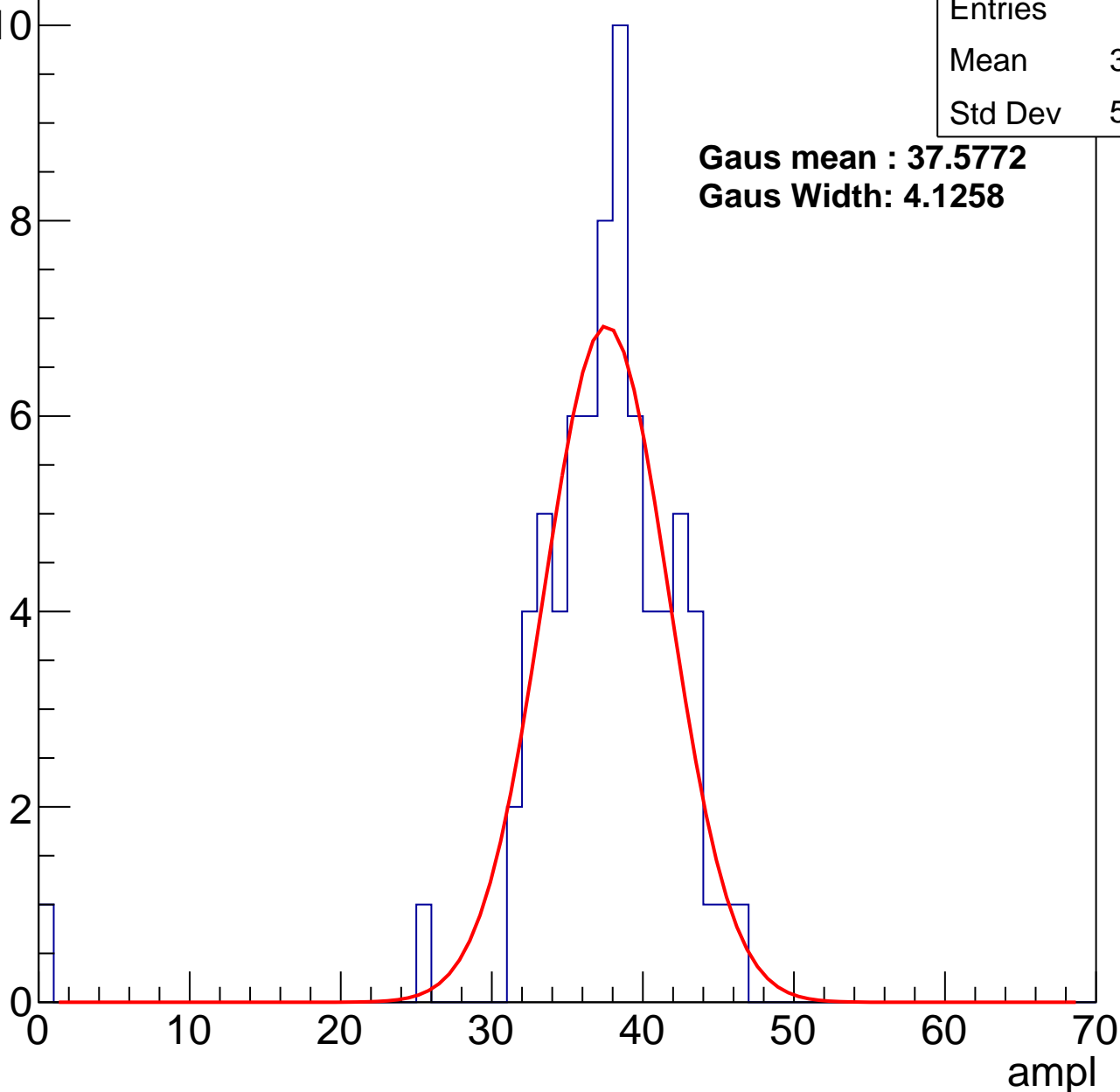
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	36.89
Std Dev	5.766

**Gaus mean : 37.5772**

**Gaus Width: 4.1258**



# B1L102S, U16-ch1, adc2

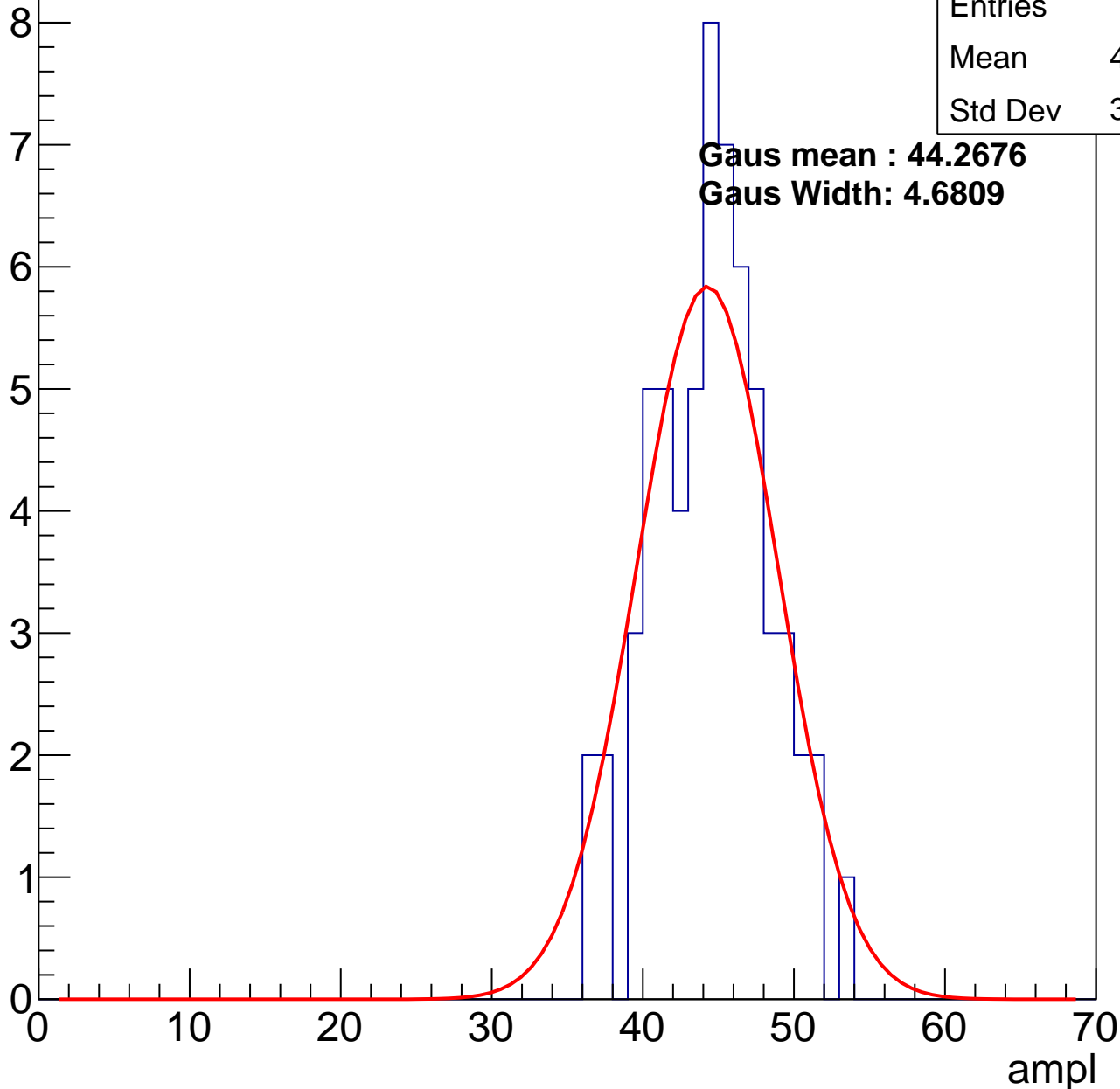
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	44.05
Std Dev	3.773

**Gaus mean : 44.2676**

**Gaus Width: 4.6809**

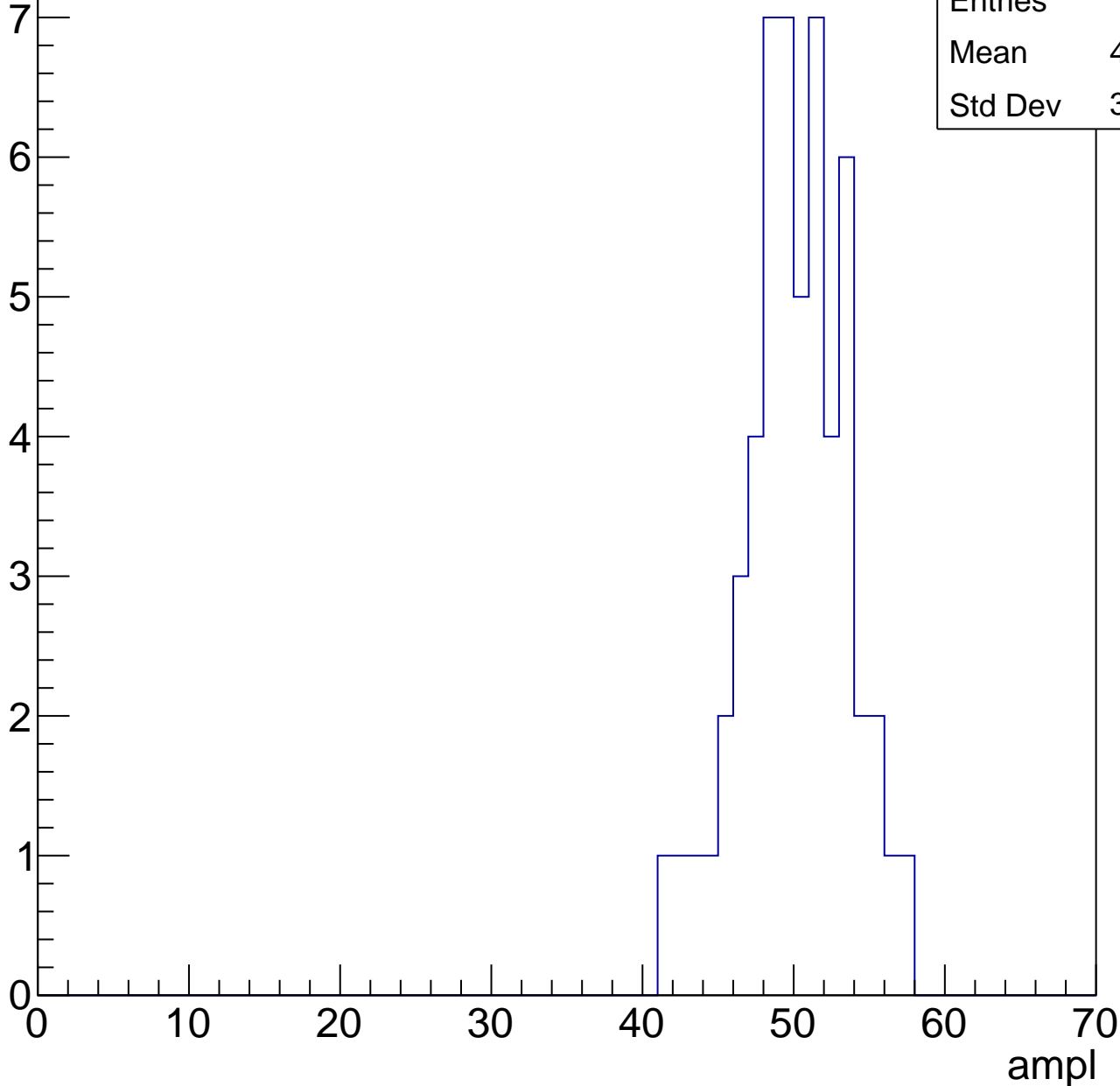


# B1L102S, U16-ch1, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	49.62
Std Dev	3.398

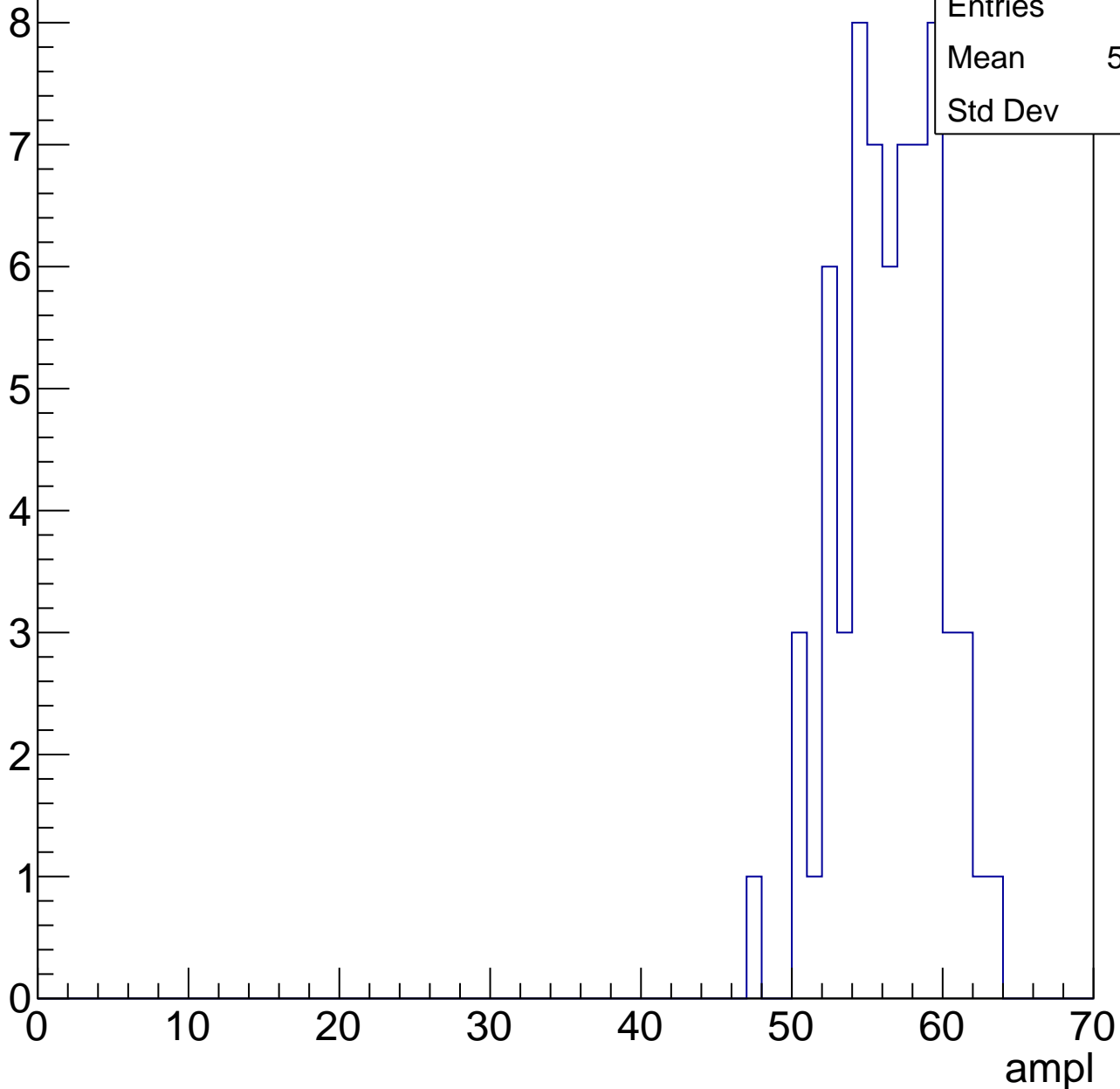


# B1L102S, U16-ch1, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	55.95
Std Dev	3.26

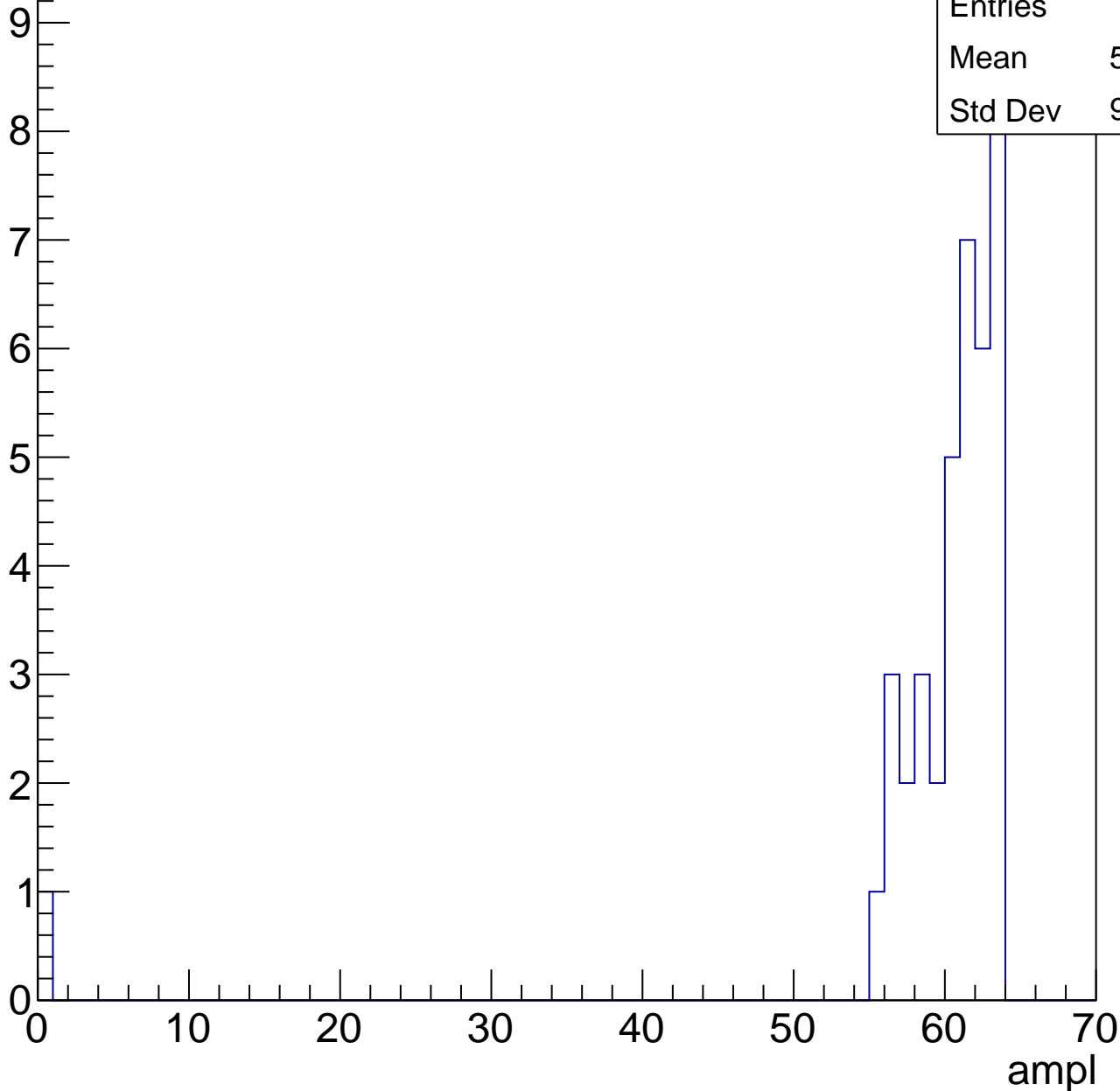


# B1L102S, U16-ch1, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

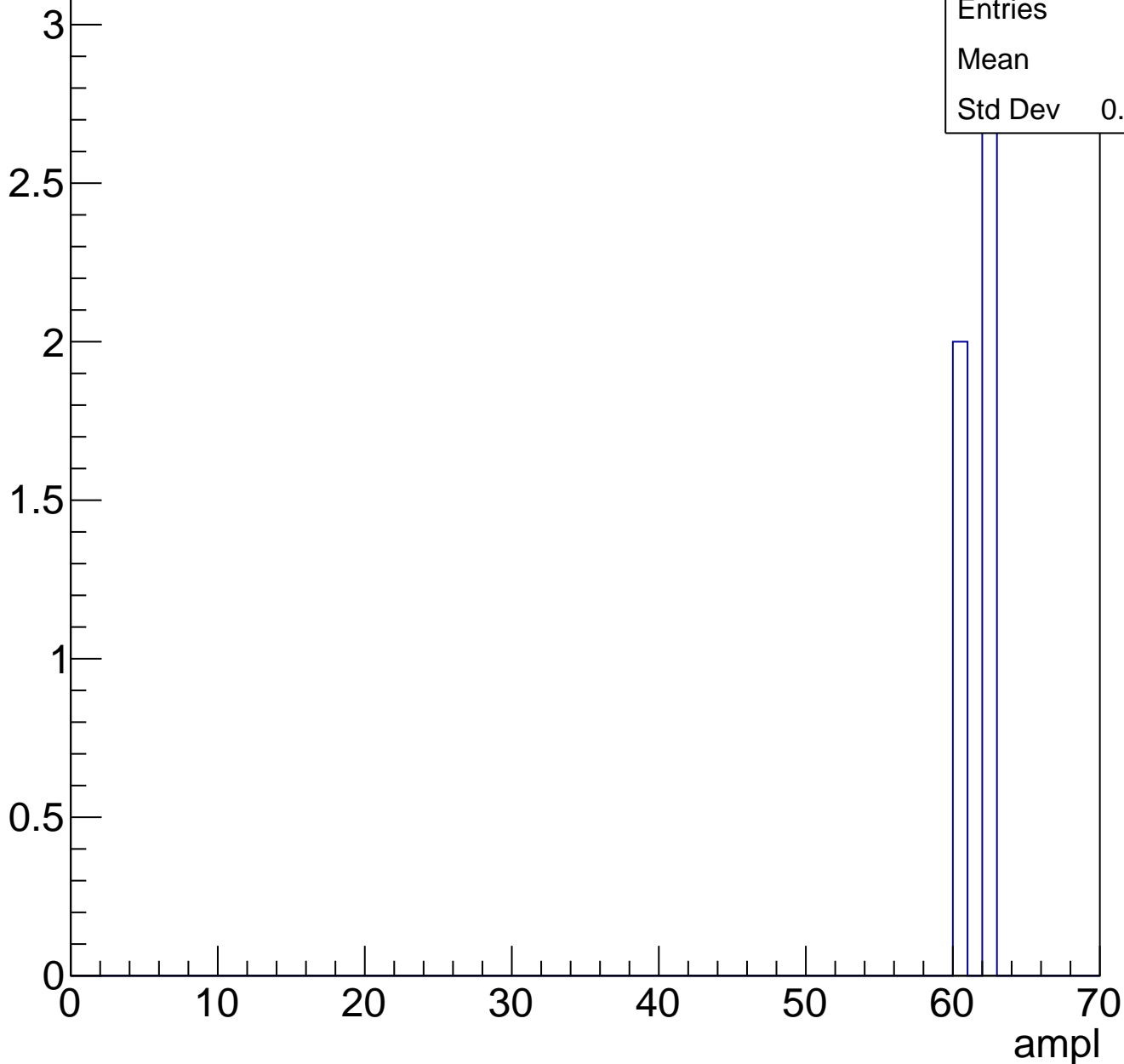
Entries	39
Mean	58.85
Std Dev	9.825



# B1L102S, U16-ch1, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch1, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch2, adc0

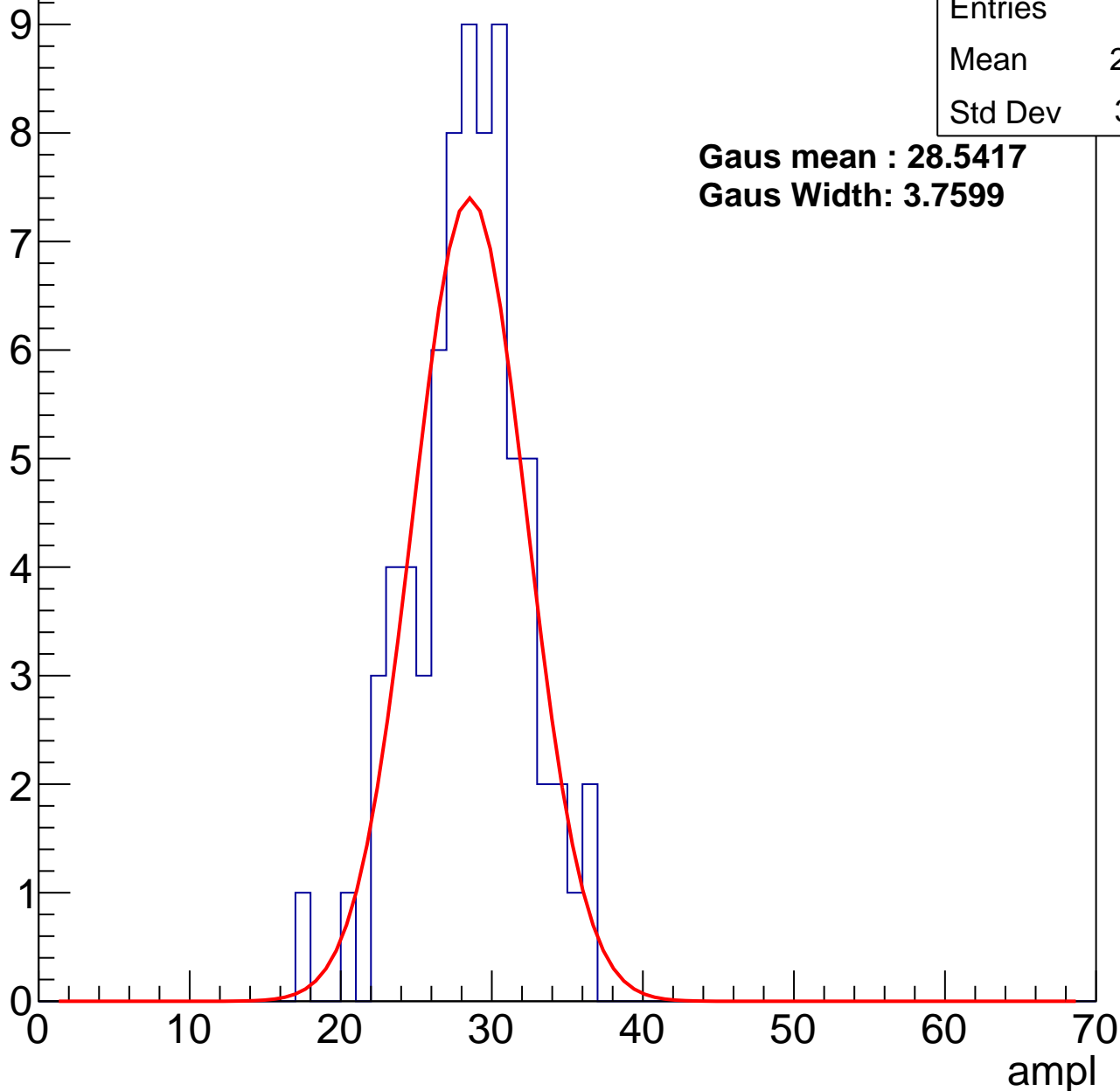
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	28.05
Std Dev	3.671

**Gaus mean : 28.5417**

**Gaus Width: 3.7599**



# B1L102S, U16-ch2, adc1

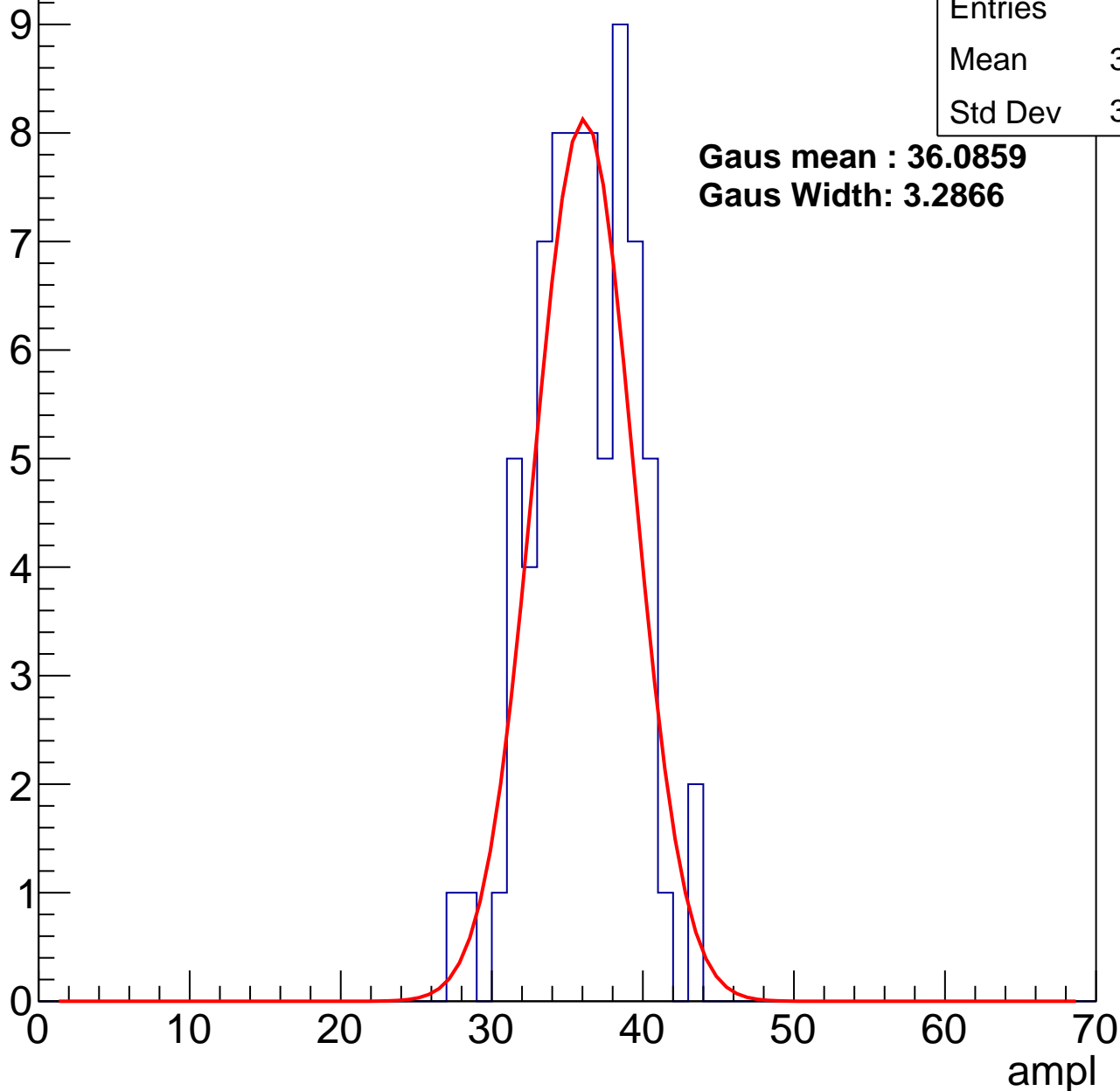
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	35.64
Std Dev	3.272

**Gaus mean : 36.0859**

**Gaus Width: 3.2866**



# B1L102S, U16-ch2, adc2

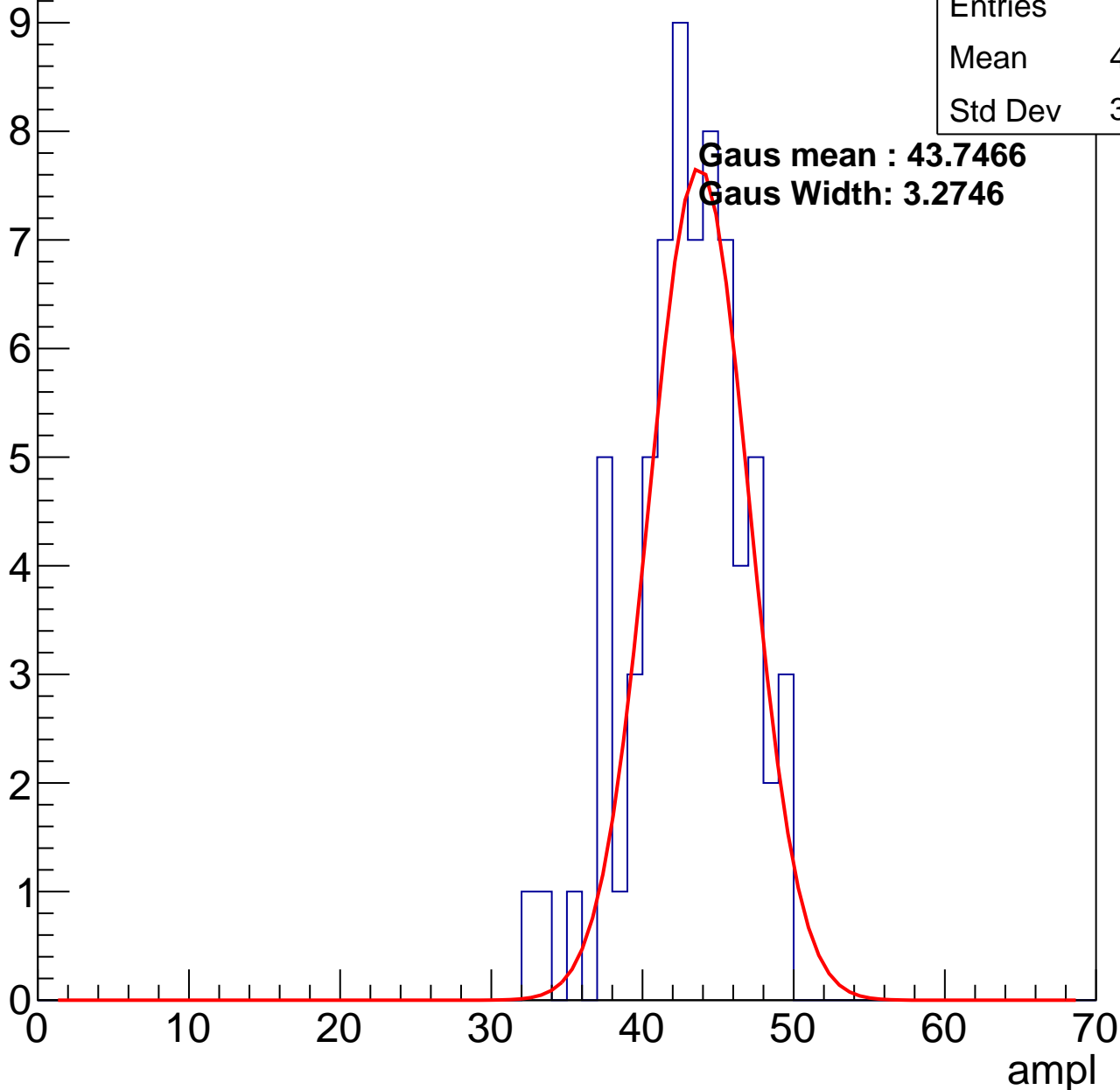
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	42.54
Std Dev	3.642

**Gaus mean : 43.7466**

**Gaus Width: 3.2746**

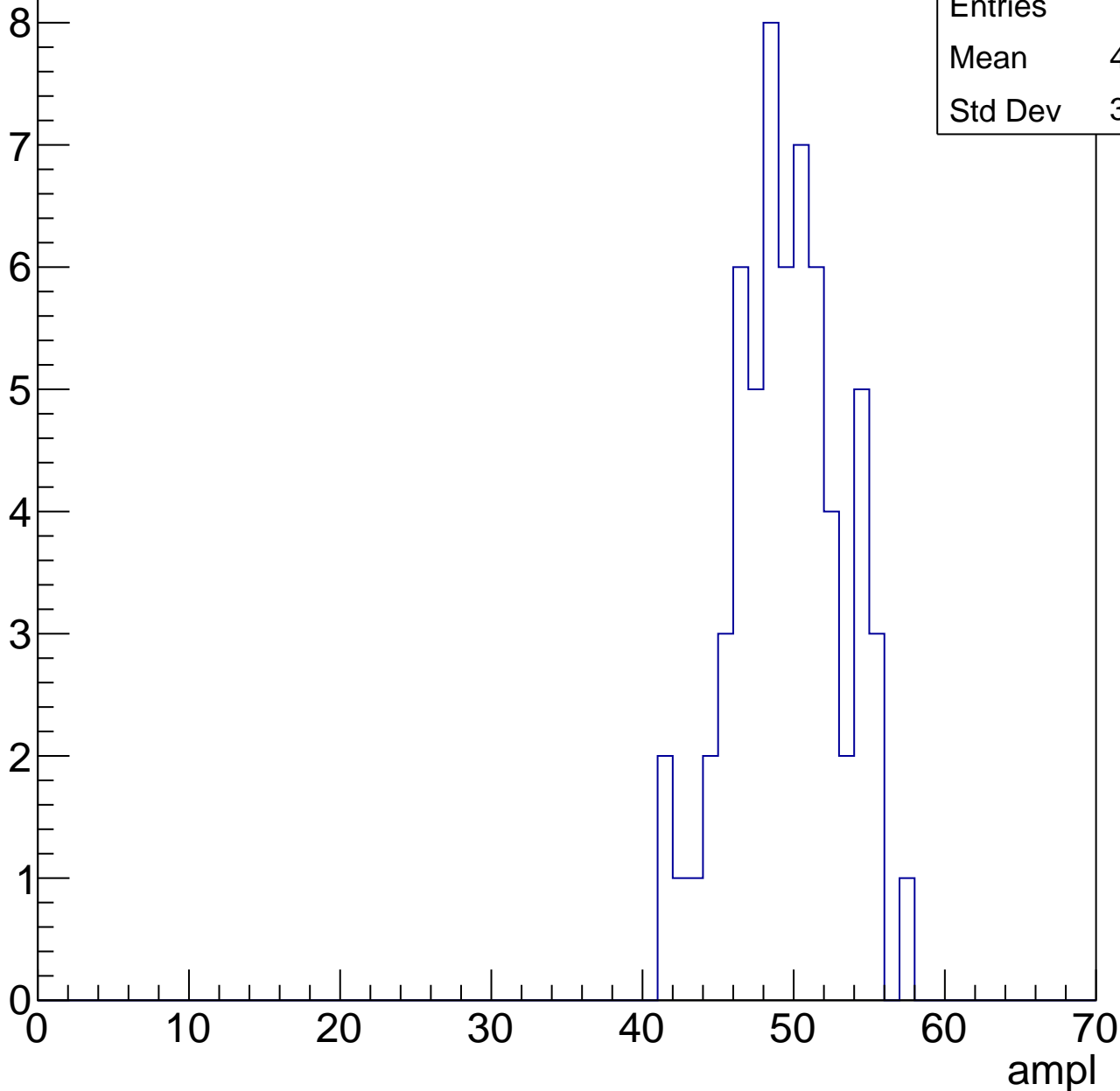


# B1L102S, U16-ch2, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

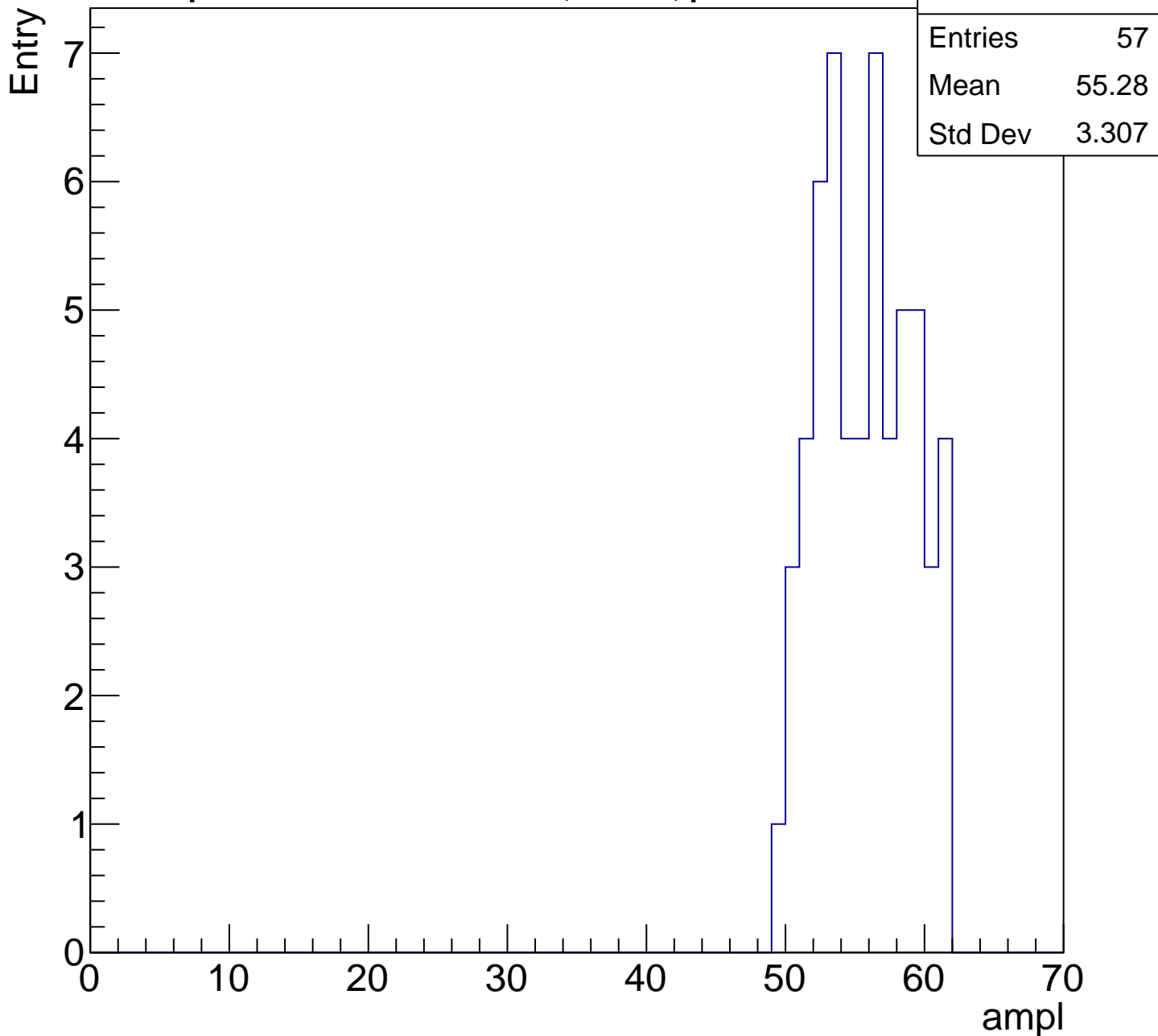
Entry

Entries	62
Mean	49.05
Std Dev	3.567



# B1L102S, U16-ch2, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

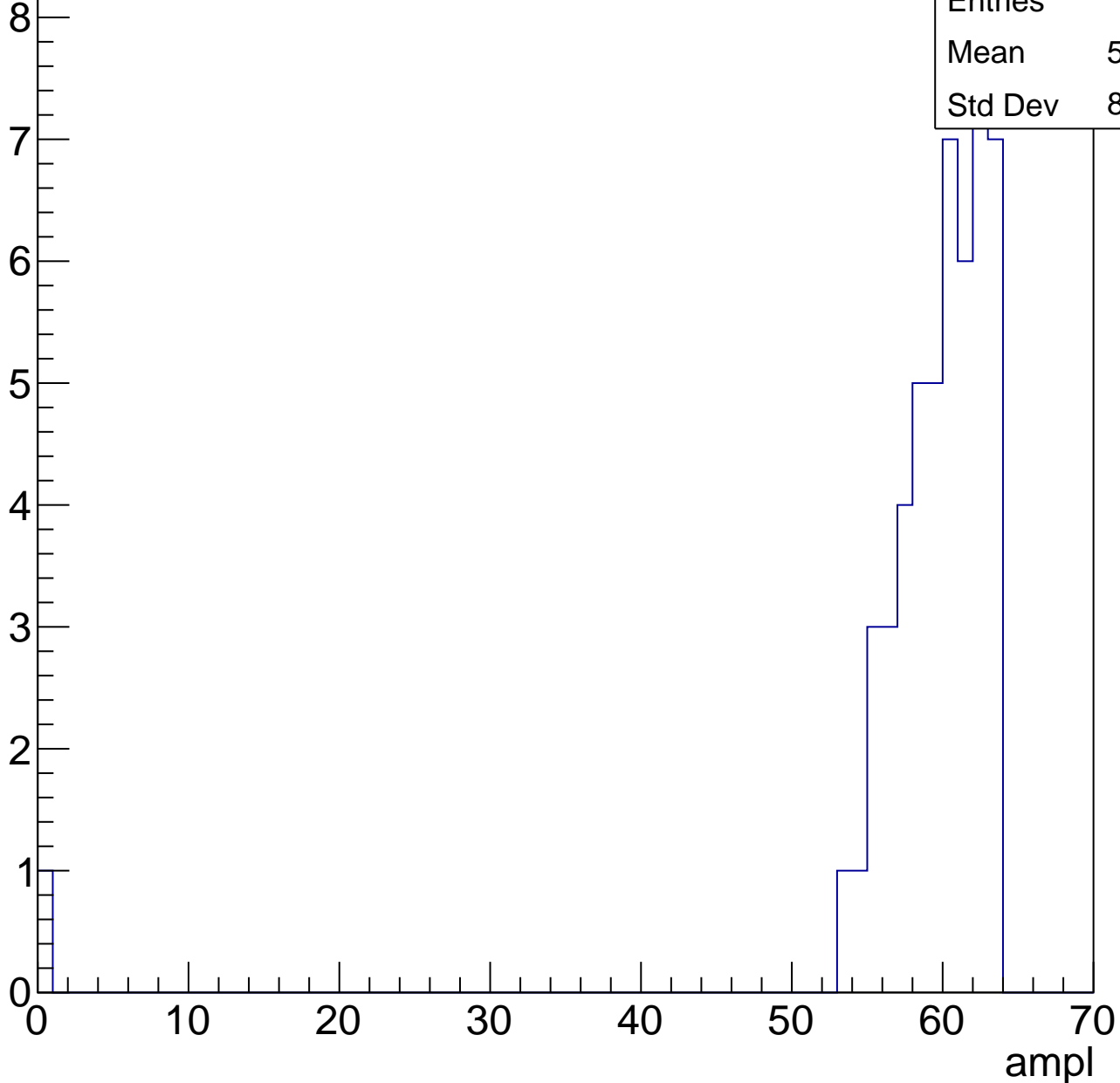


# B1L102S, U16-ch2, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

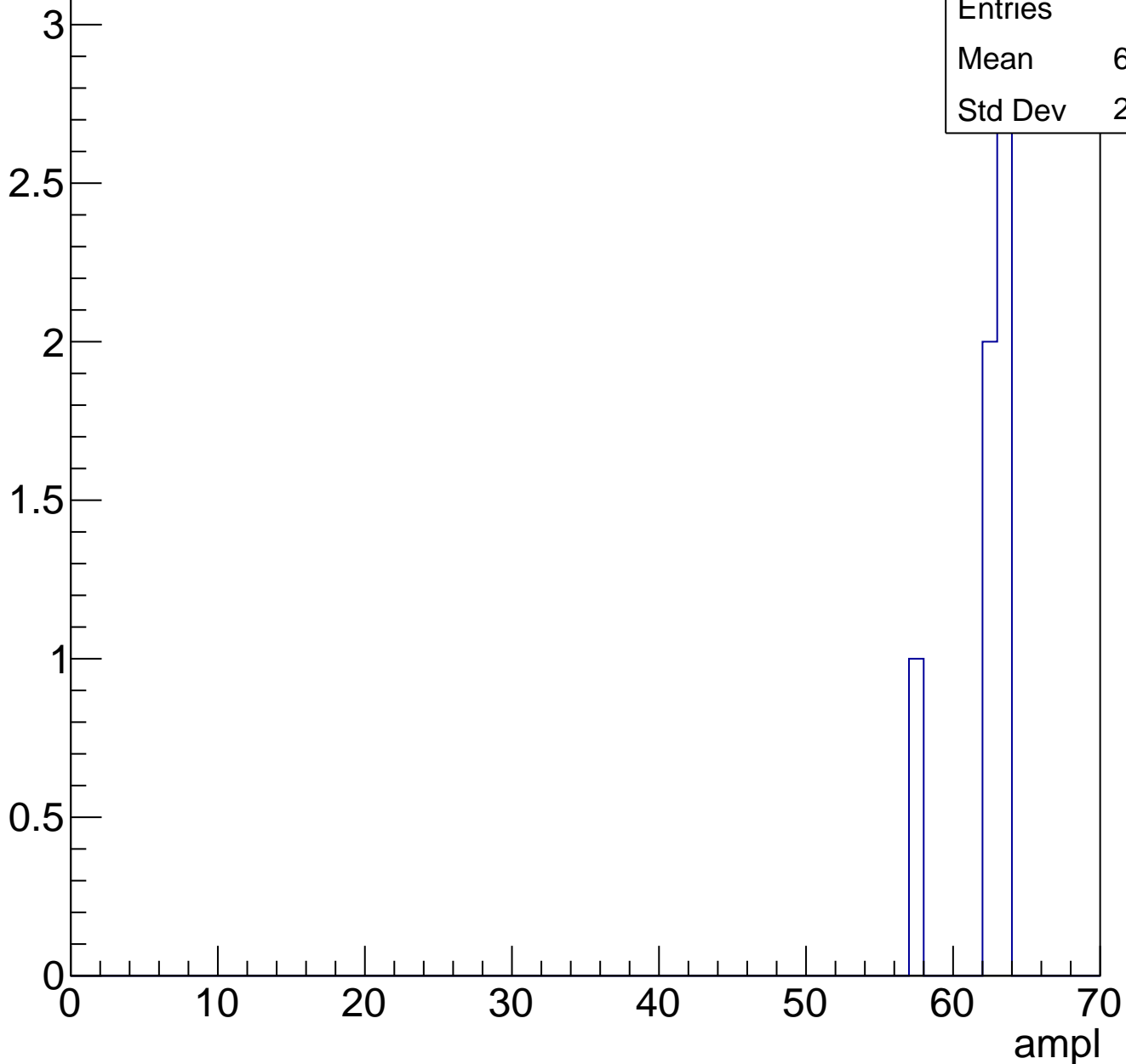
Entries	51
Mean	58.35
Std Dev	8.668



# B1L102S, U16-ch2, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch2, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch3, adc0

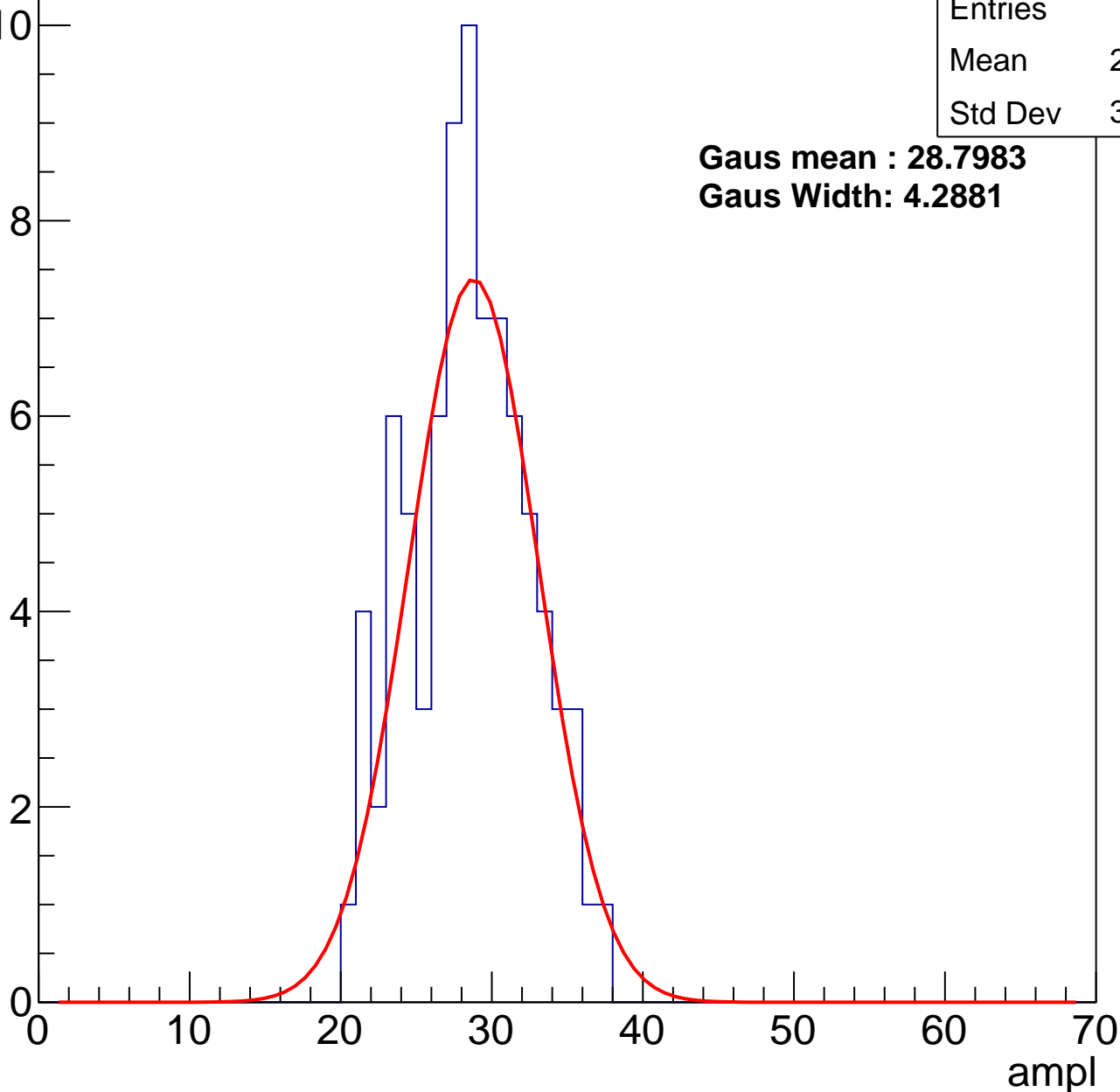
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	83
Mean	28.08
Std Dev	3.943

**Gaus mean : 28.7983**

**Gaus Width: 4.2881**



# B1L102S, U16-ch3, adc1

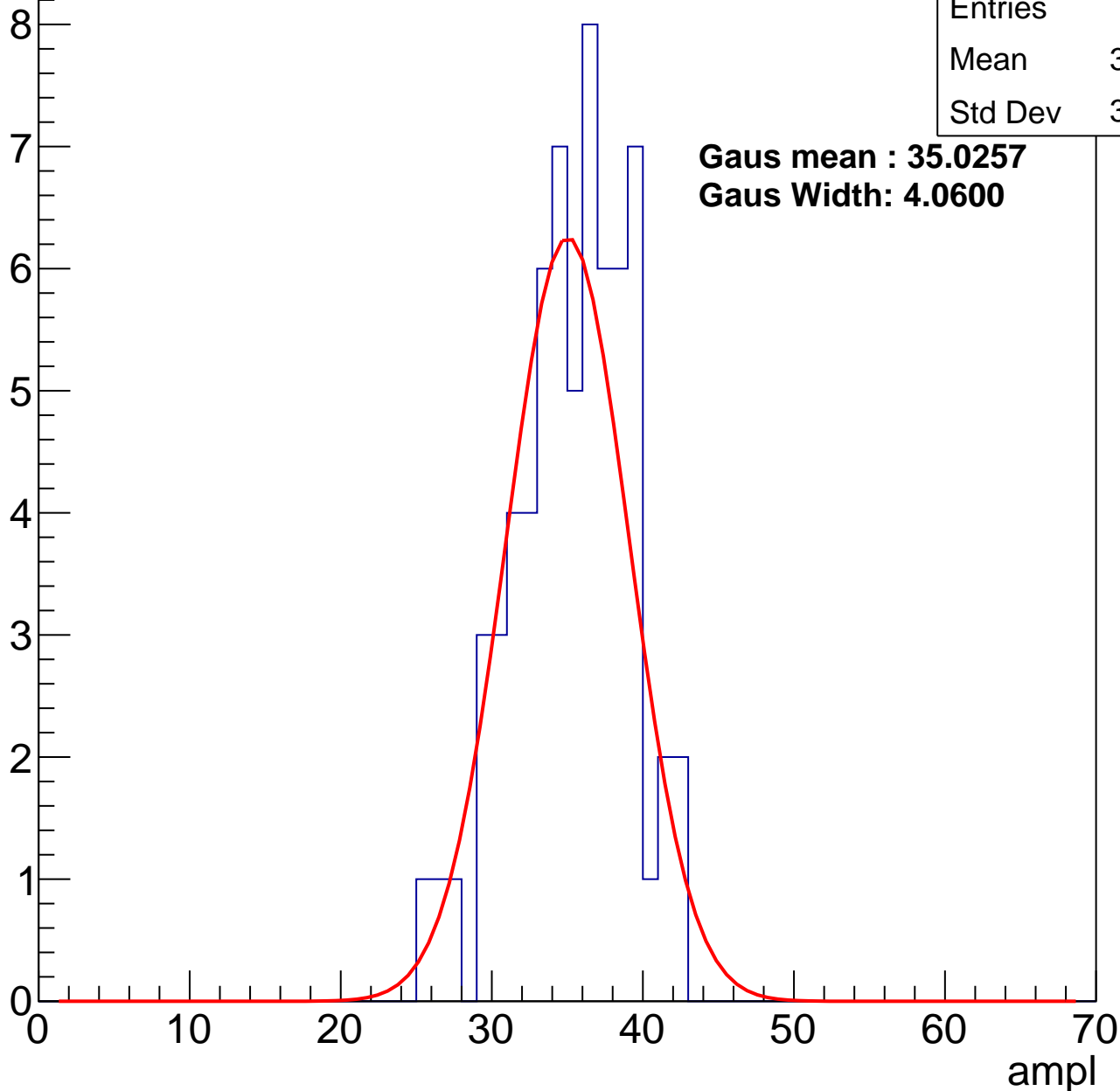
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	34.85
Std Dev	3.767

**Gaus mean : 35.0257**

**Gaus Width: 4.0600**



# B1L102S, U16-ch3, adc2

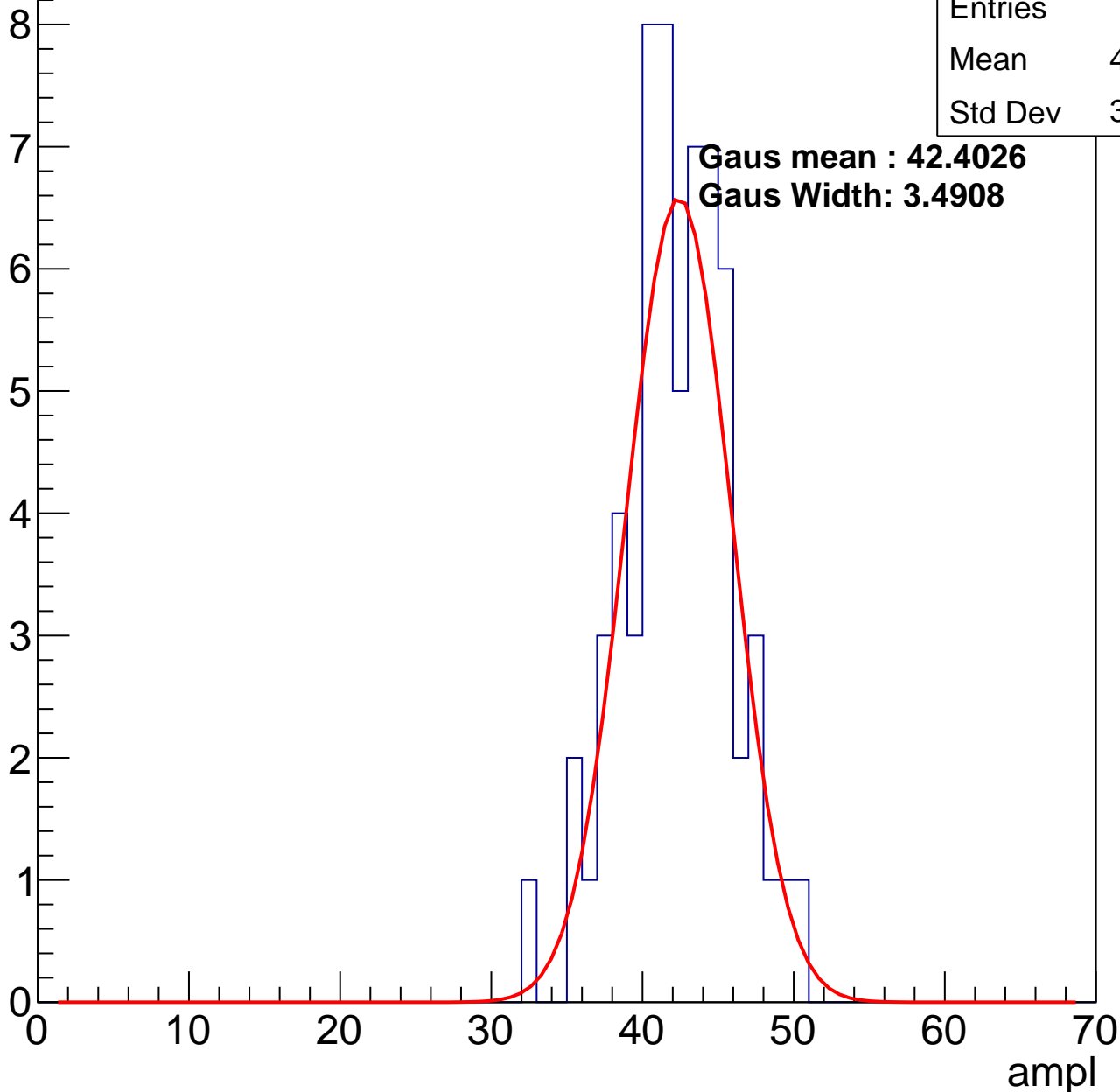
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	41.83
Std Dev	3.526

**Gaus mean : 42.4026**

**Gaus Width: 3.4908**

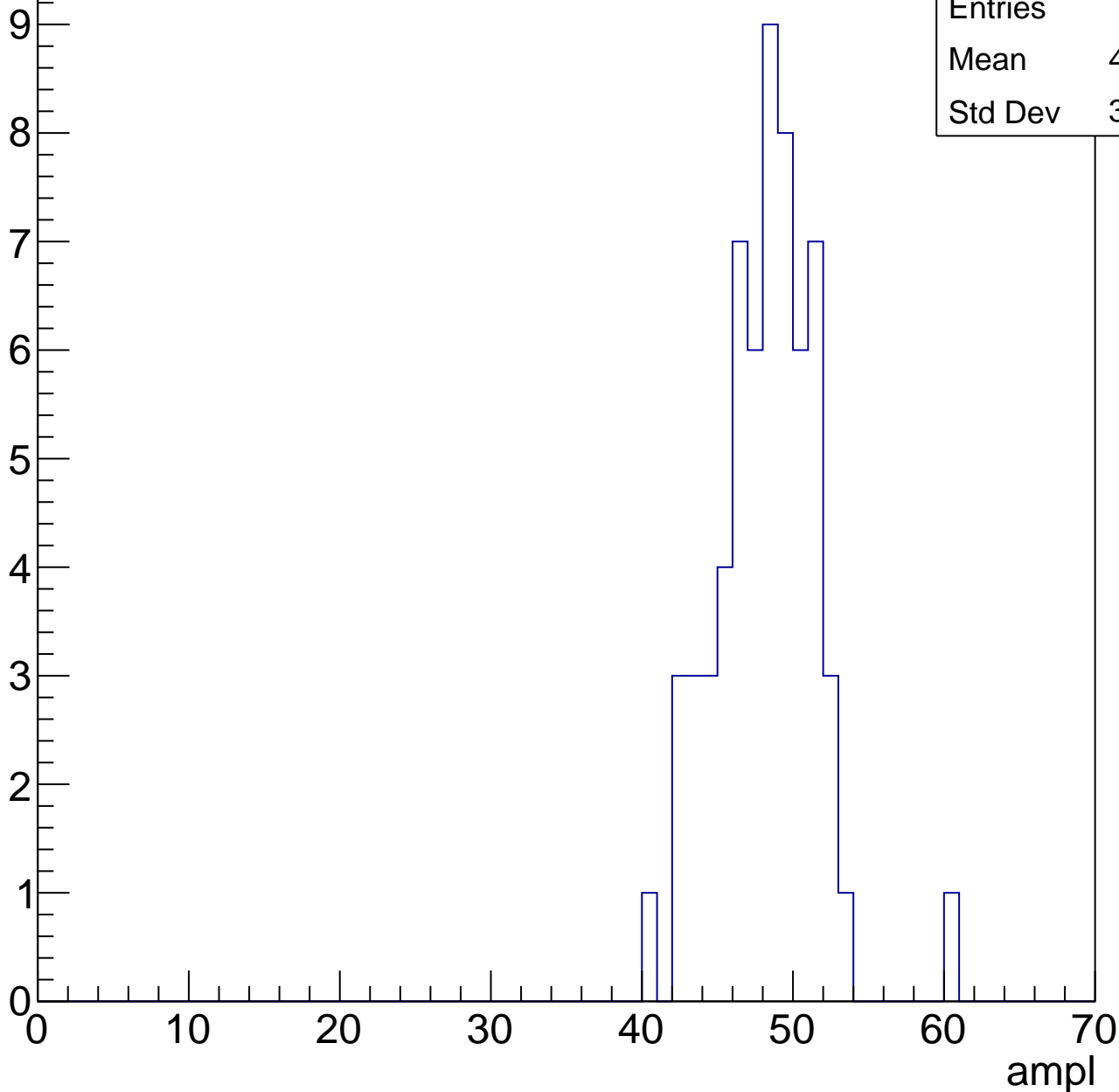


# B1L102S, U16-ch3, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

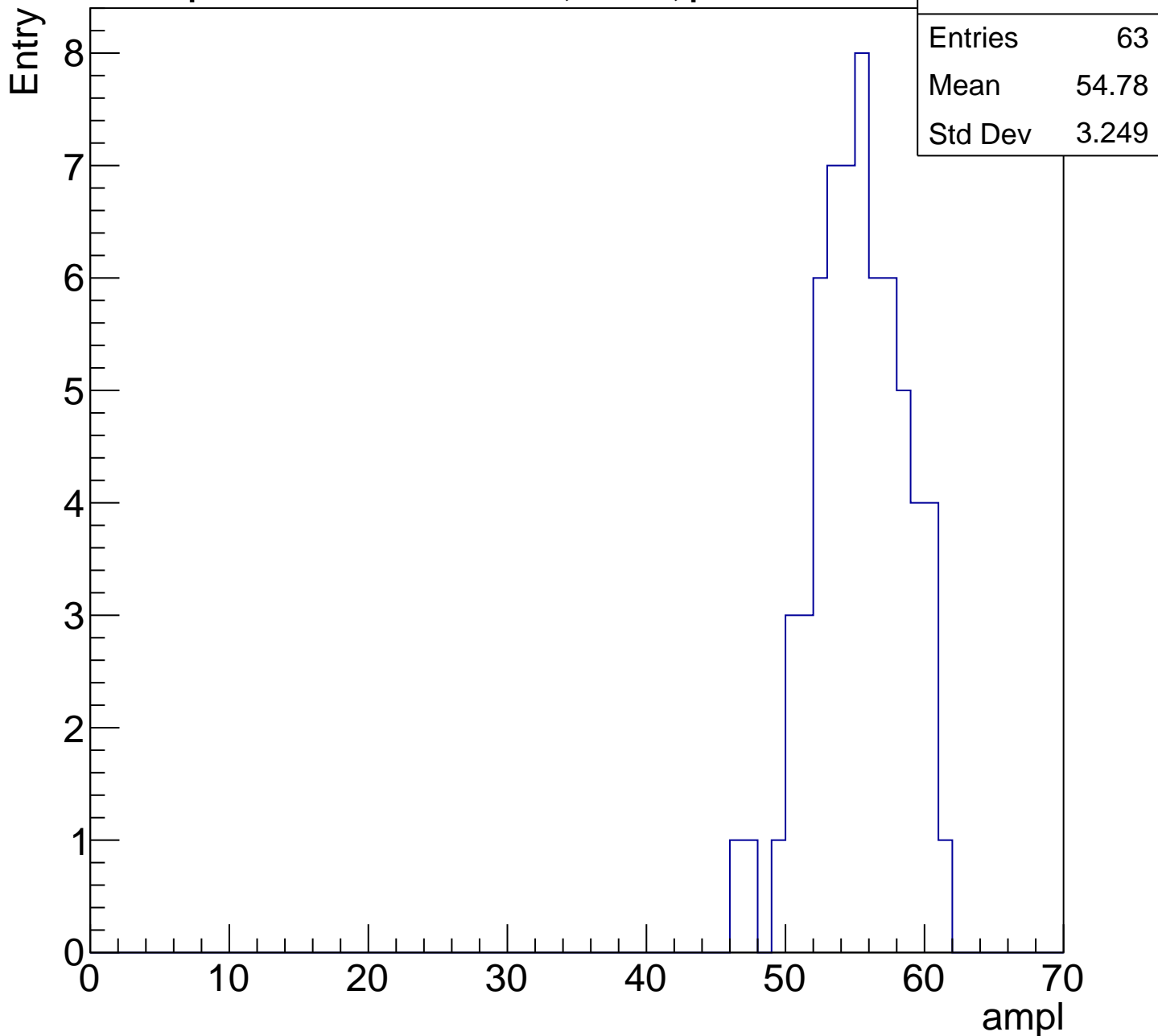
Entry

Entries	62
Mean	47.76
Std Dev	3.296



# B1L102S, U16-ch3, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

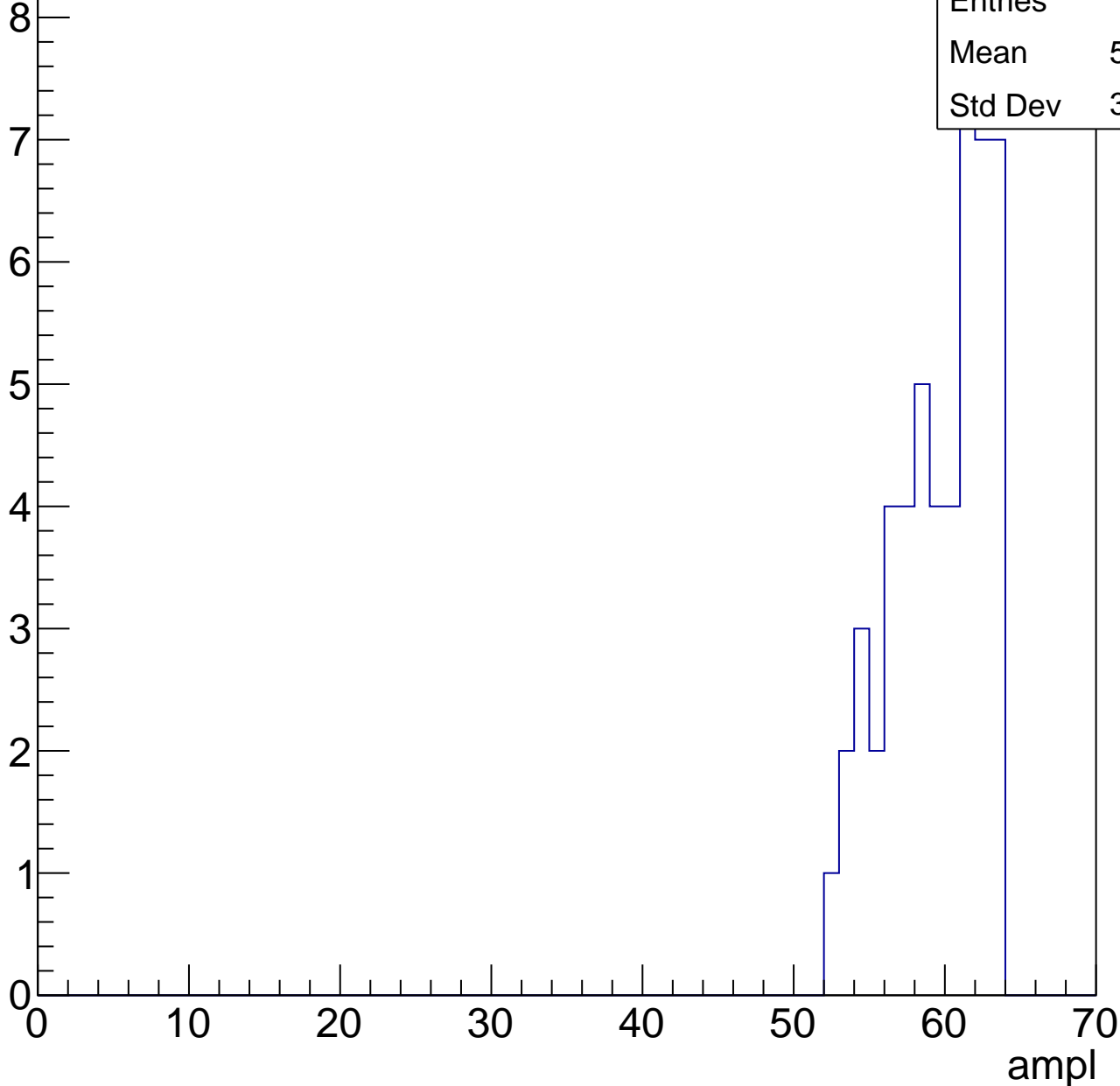


# B1L102S, U16-ch3, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	59.04
Std Dev	3.118



# B1L102S, U16-ch3, adc6

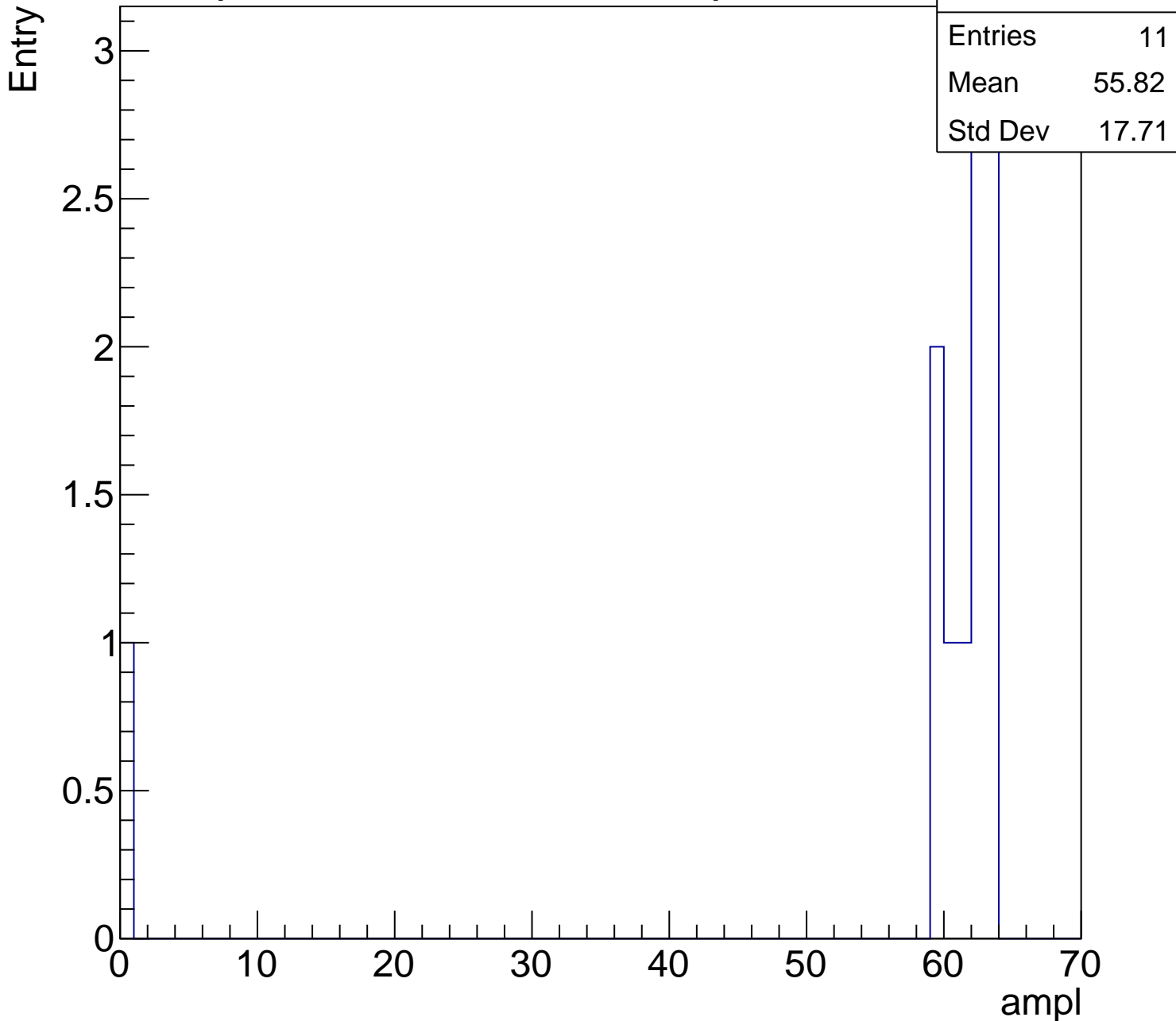
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	11
Mean	55.82
Std Dev	17.71

ampl





# B1L102S, U16-ch3, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch4, adc0

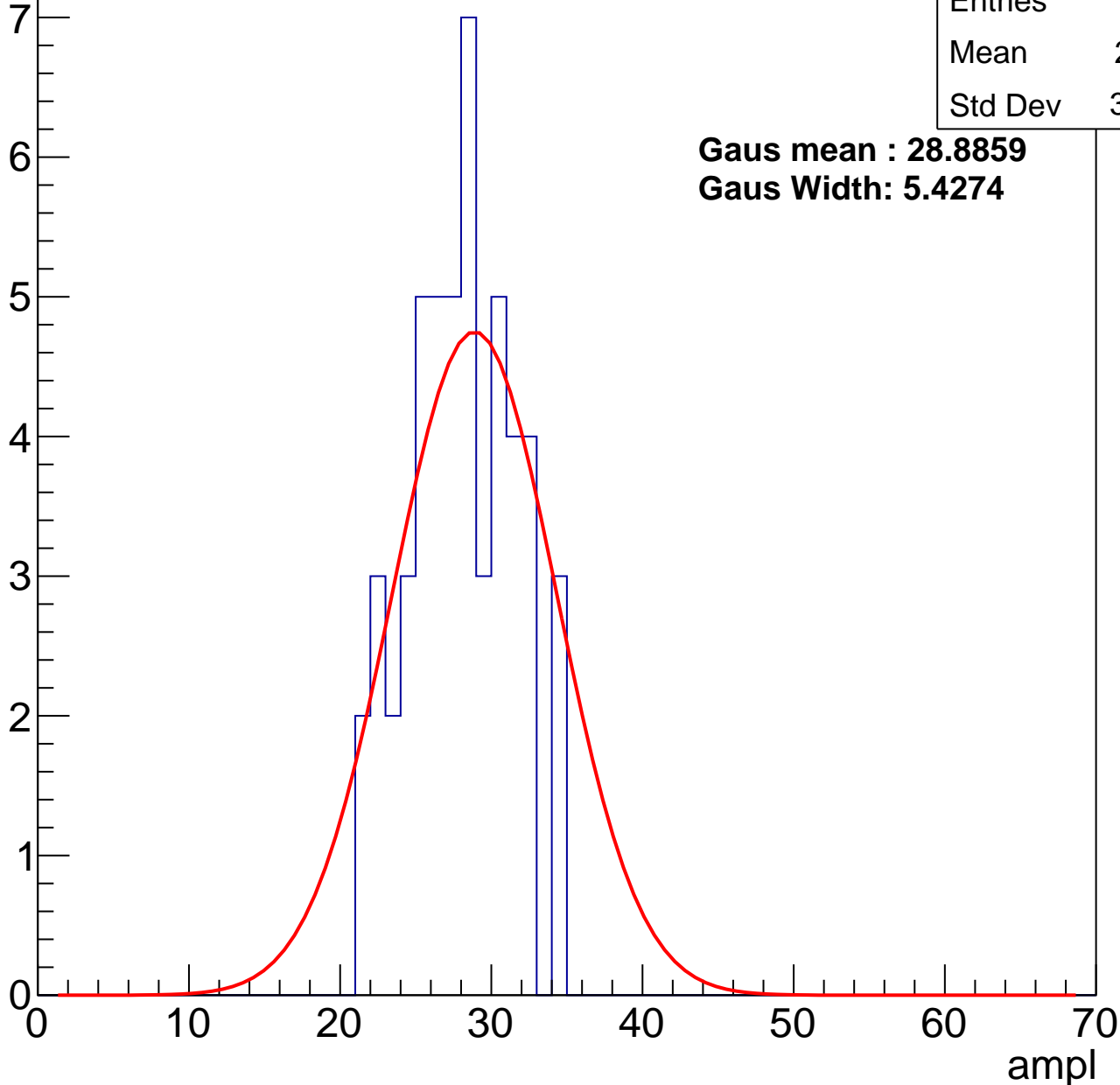
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	27.51
Std Dev	3.409

**Gaus mean : 28.8859**

**Gaus Width: 5.4274**



# B1L102S, U16-ch4, adc1

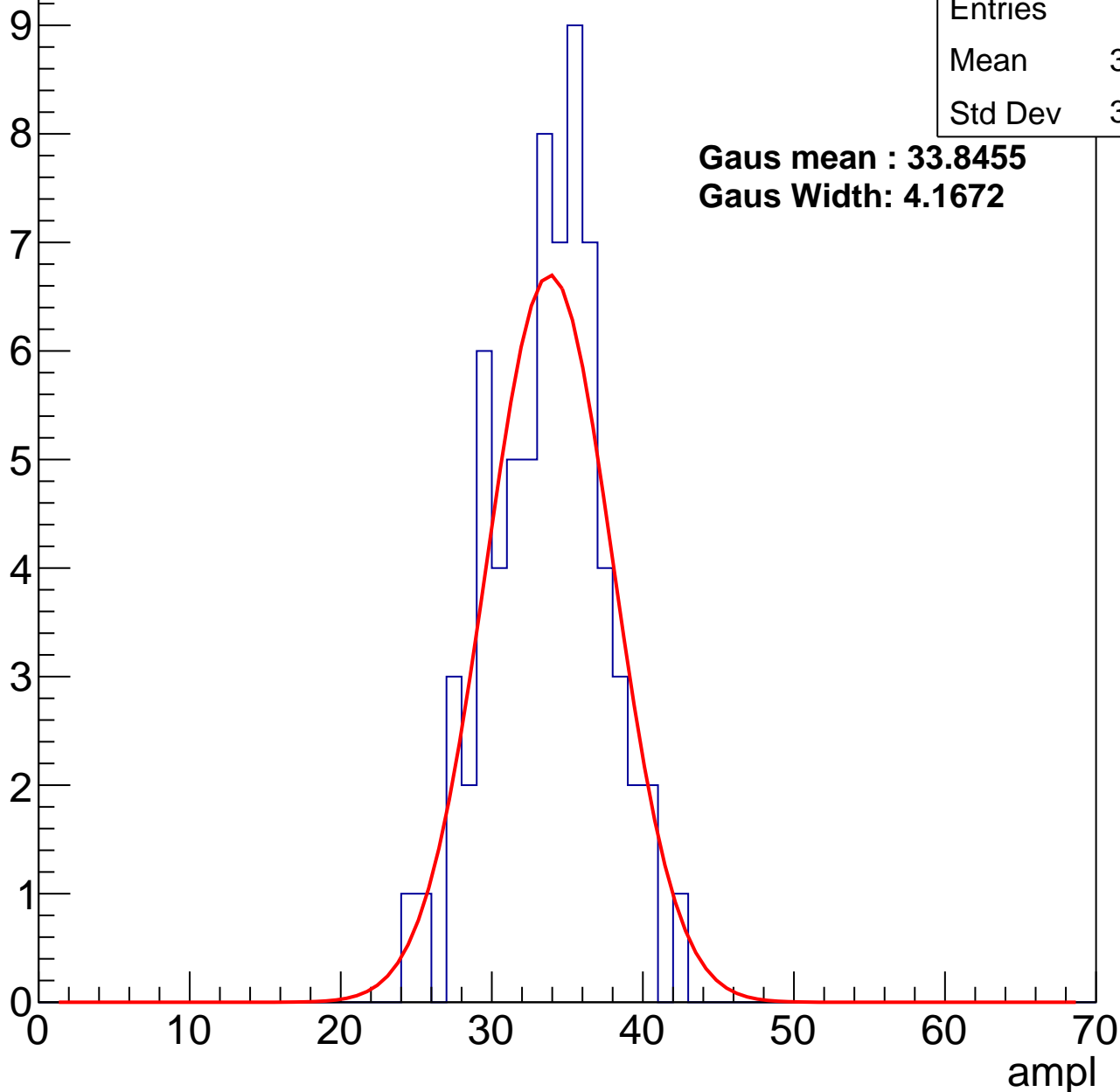
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	33.23
Std Dev	3.688

**Gaus mean : 33.8455**

**Gaus Width: 4.1672**



# B1L102S, U16-ch4, adc2

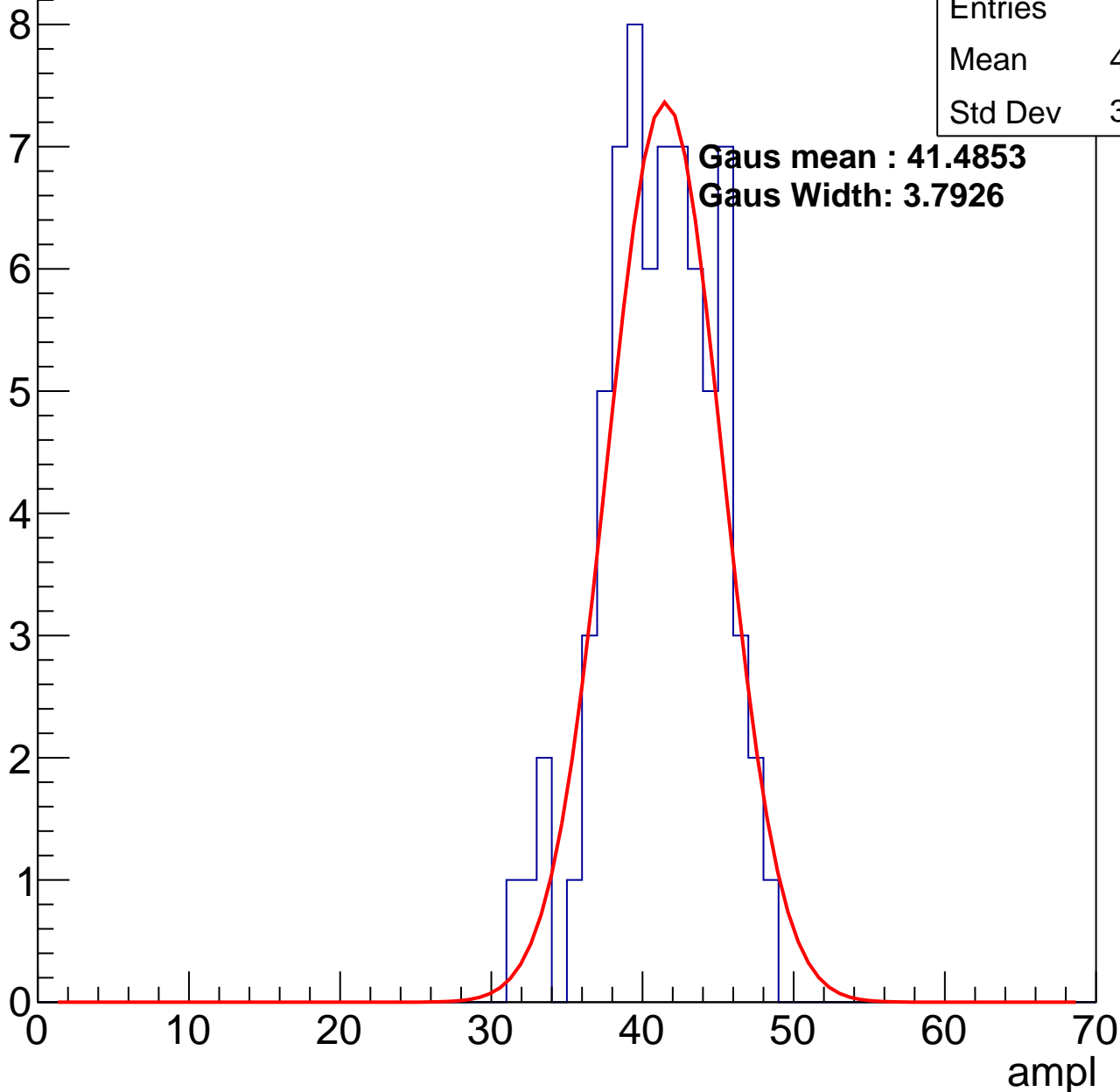
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	40.68
Std Dev	3.685

**Gaus mean : 41.4853**

**Gaus Width: 3.7926**

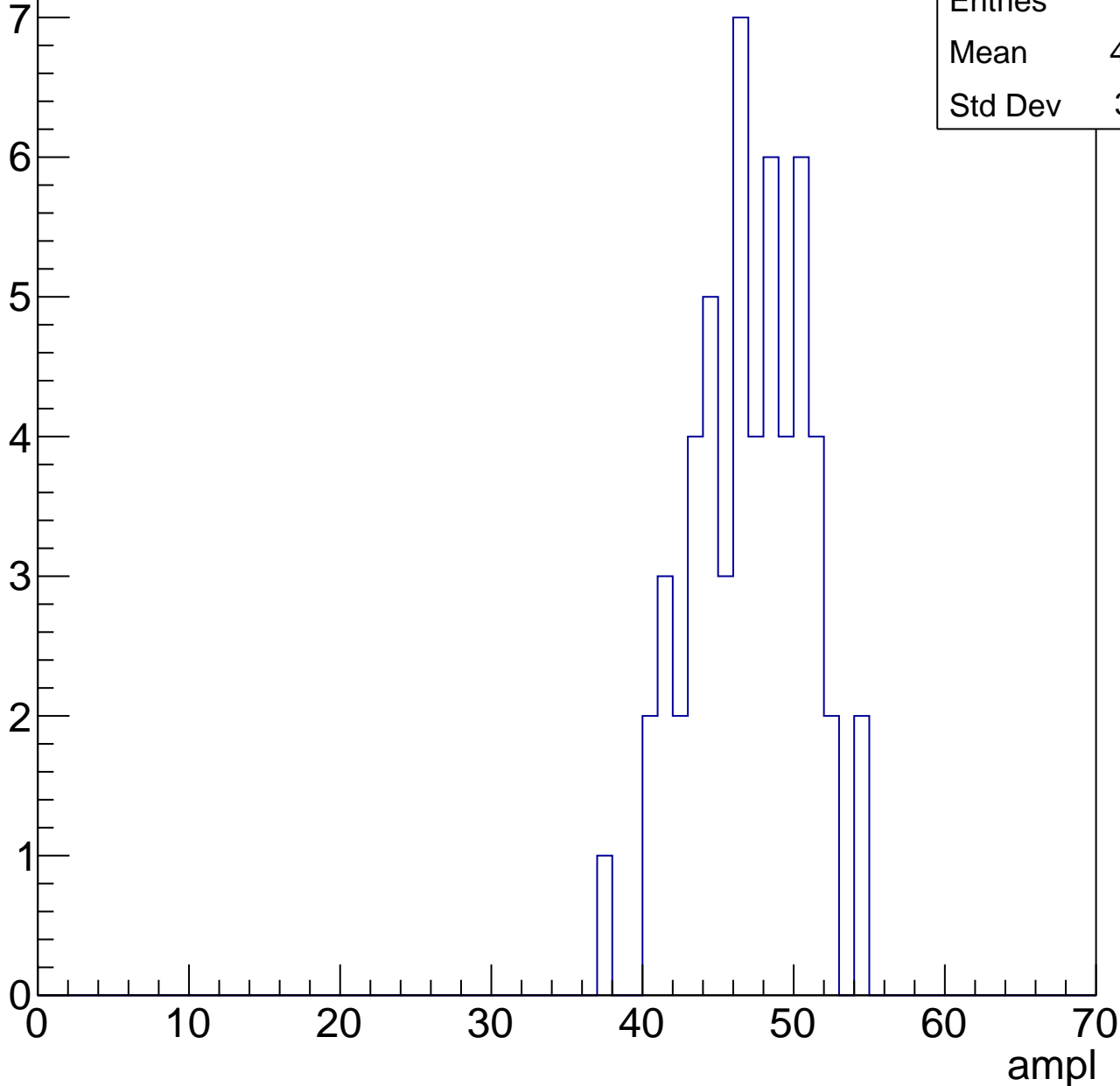


# B1L102S, U16-ch4, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	46.56
Std Dev	3.721

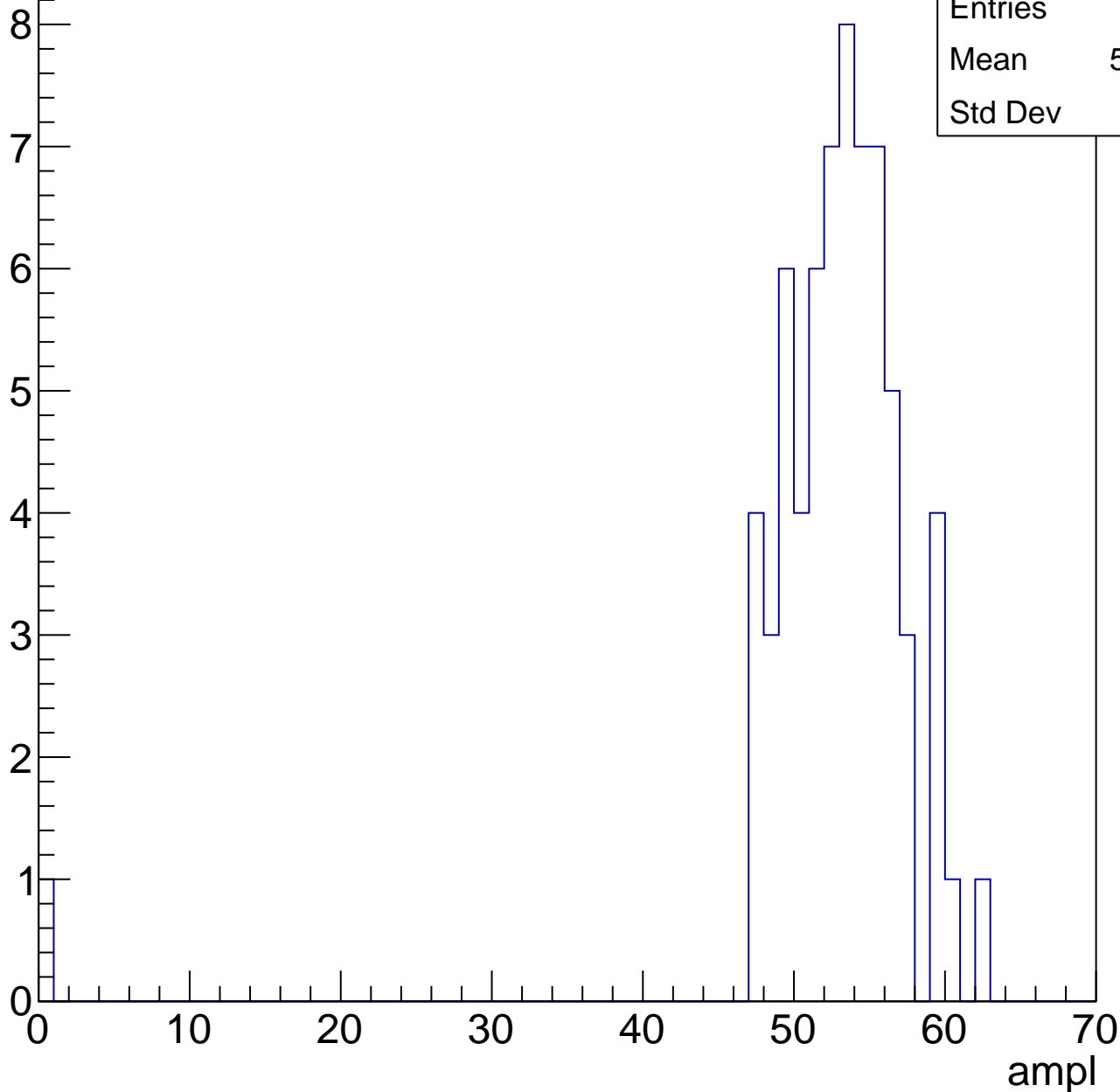


# B1L102S, U16-ch4, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	52.12
Std Dev	7.27

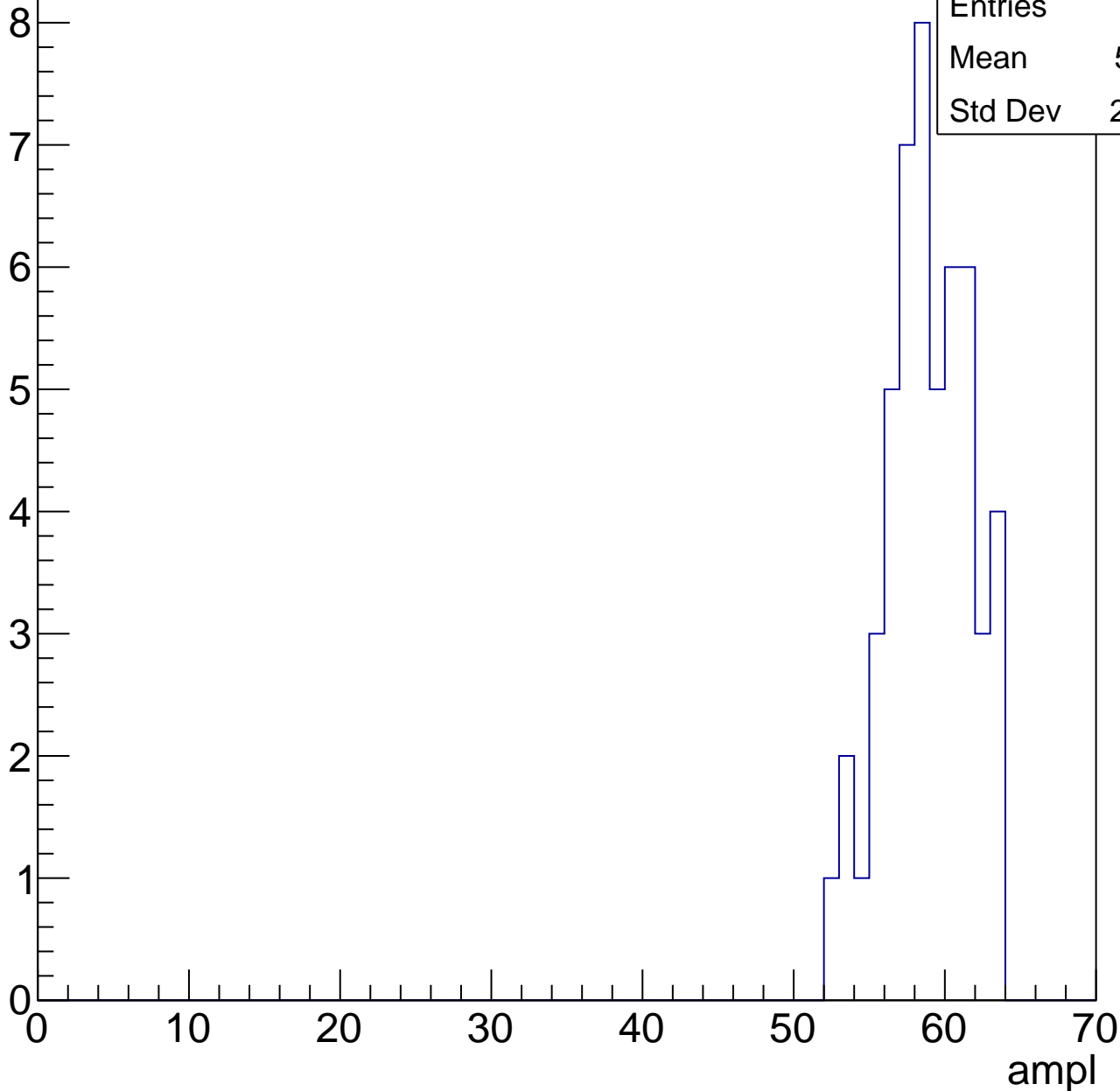


# B1L102S, U16-ch4, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	58.41
Std Dev	2.724

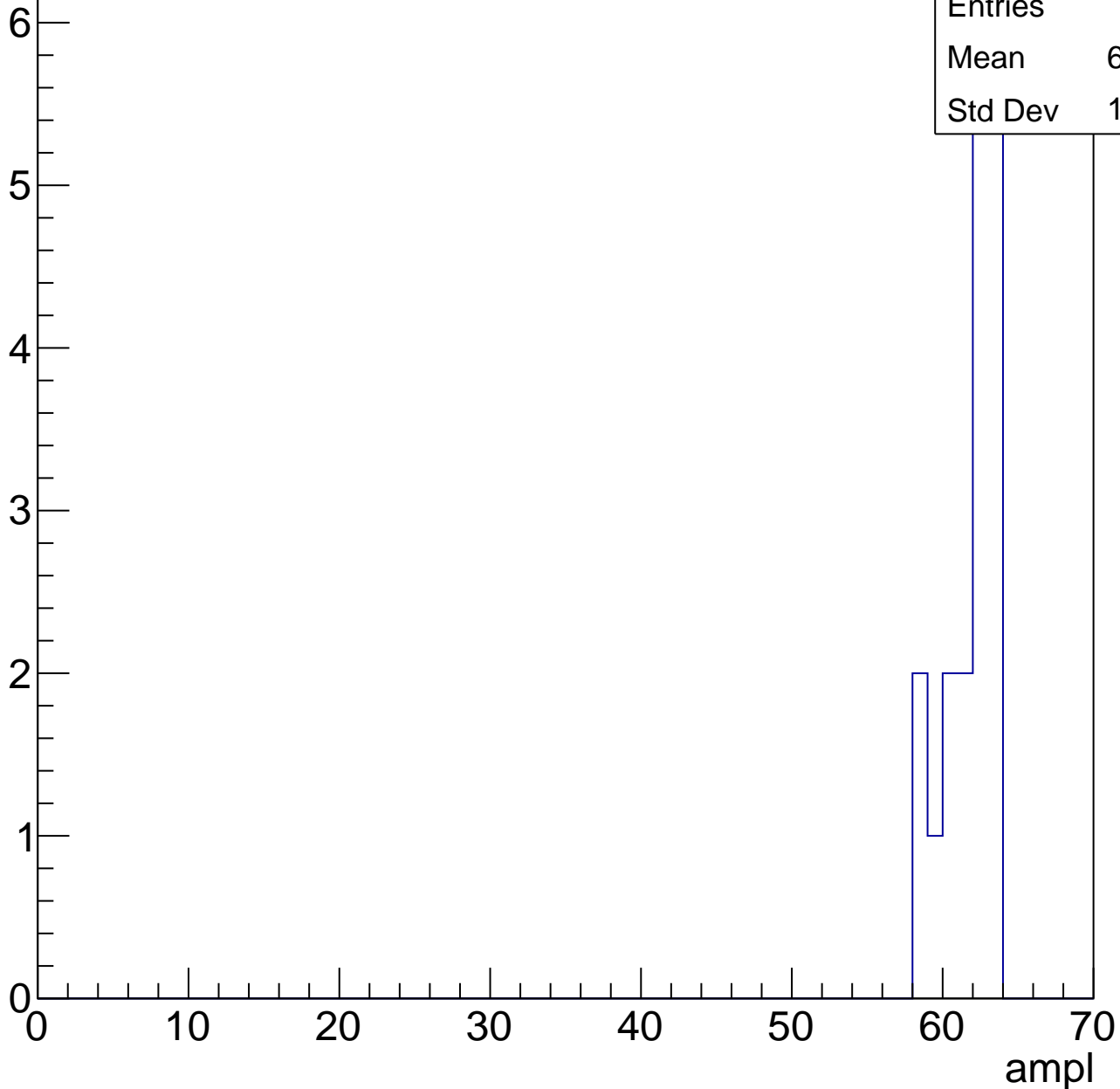


# B1L102S, U16-ch4, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	19
Mean	61.42
Std Dev	1.632





# B1L102S, U16-ch4, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	60.67
Std Dev	0.4714

ampl

0 10 20 30 40 50 60 70

# B1L102S, U16-ch5, adc0

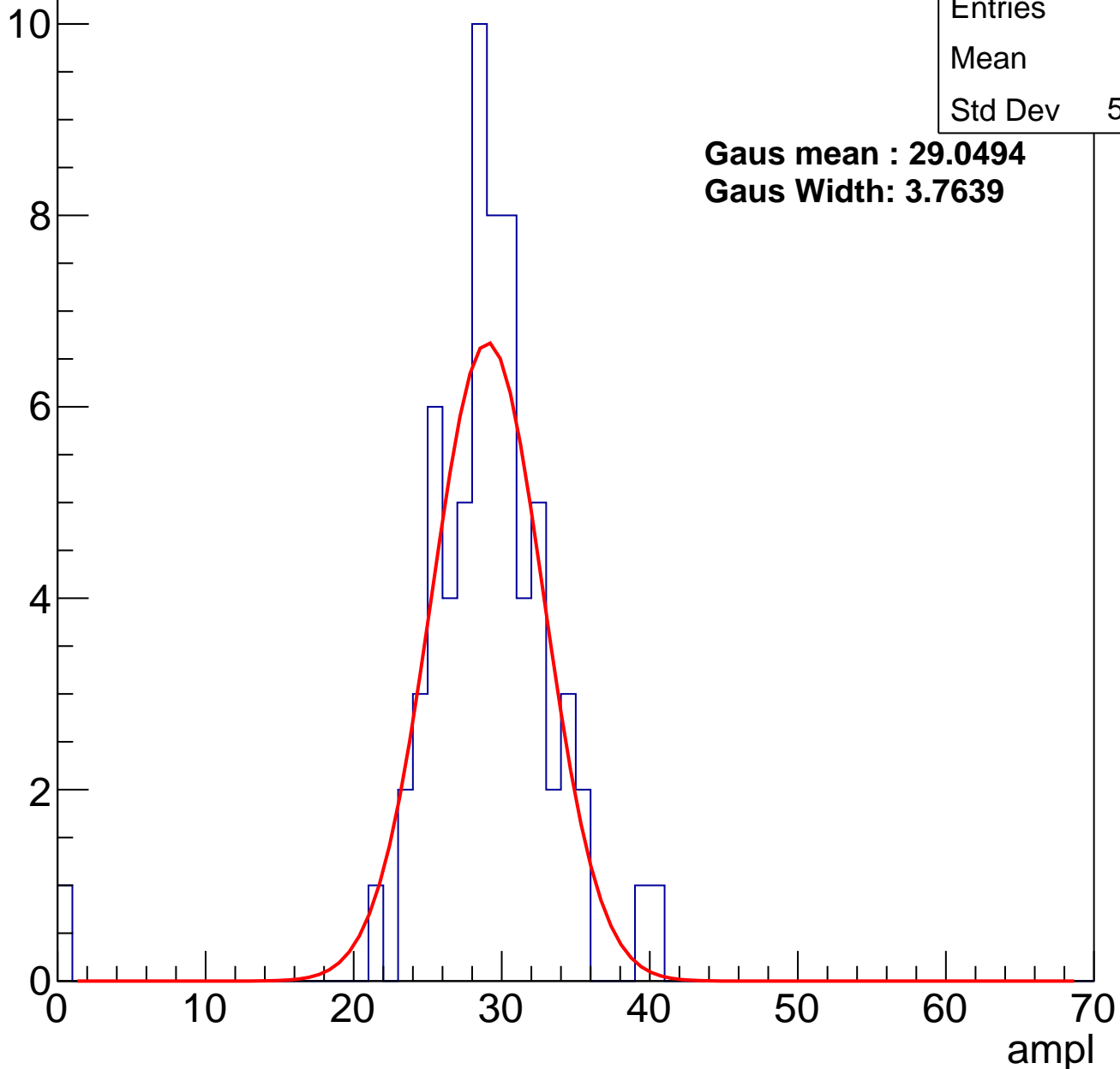
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	66
Mean	28.5
Std Dev	5.025

**Gaus mean : 29.0494**

**Gaus Width: 3.7639**

Entry



# B1L102S, U16-ch5, adc1

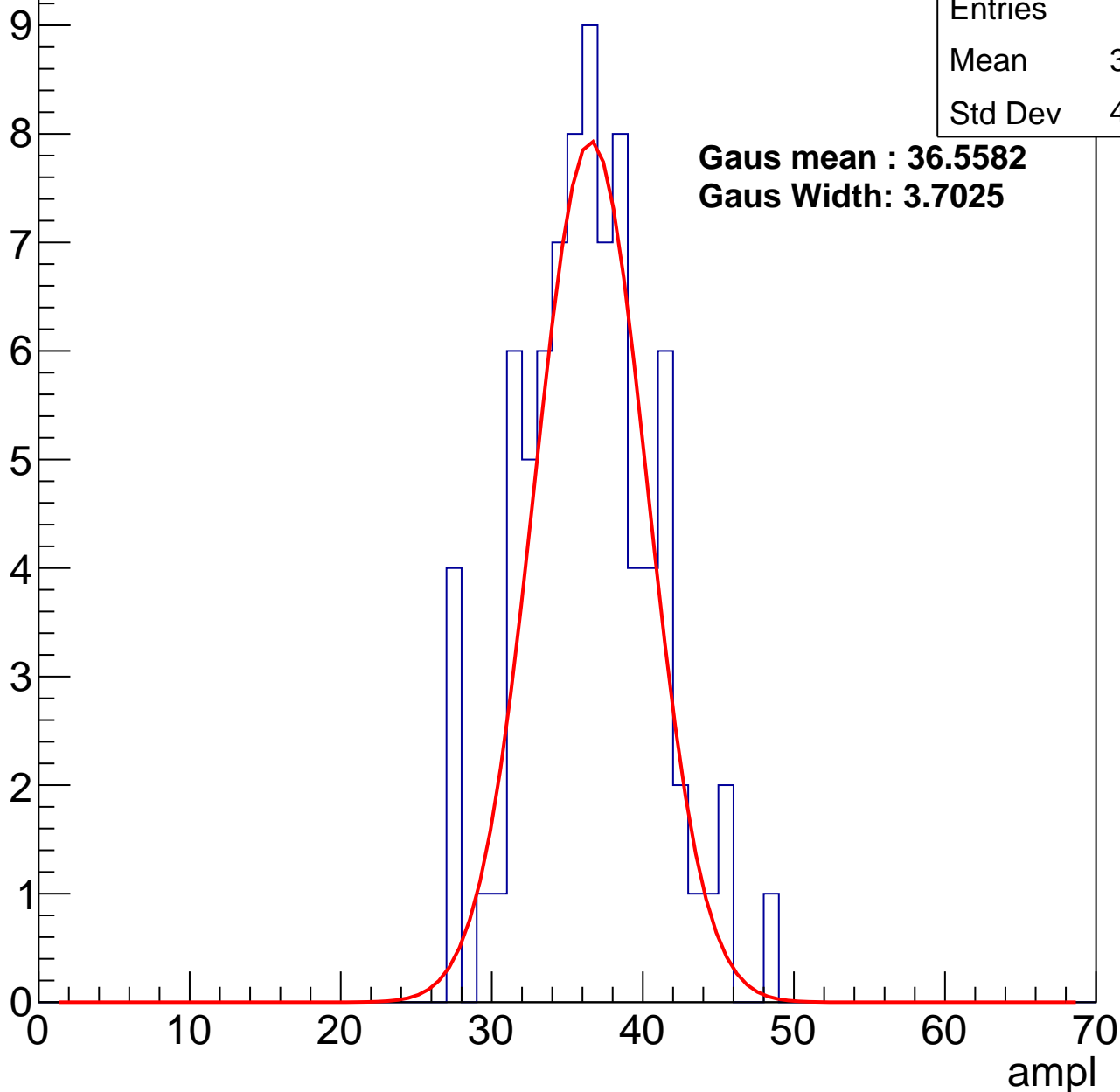
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	83
Mean	35.99
Std Dev	4.264

**Gaus mean : 36.5582**

**Gaus Width: 3.7025**



# B1L102S, U16-ch5, adc2

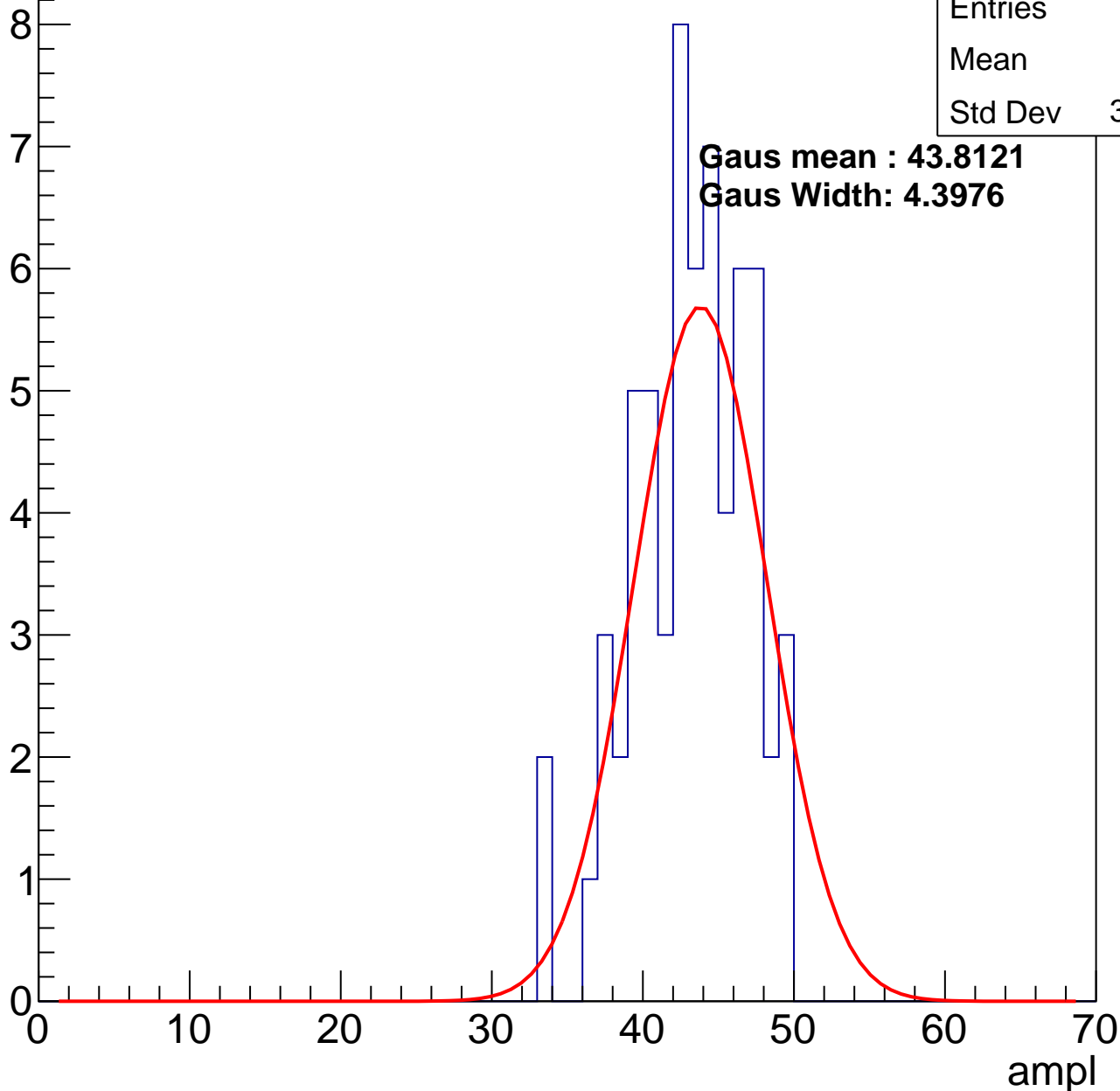
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	42.7
Std Dev	3.732

**Gaus mean : 43.8121**

**Gaus Width: 4.3976**

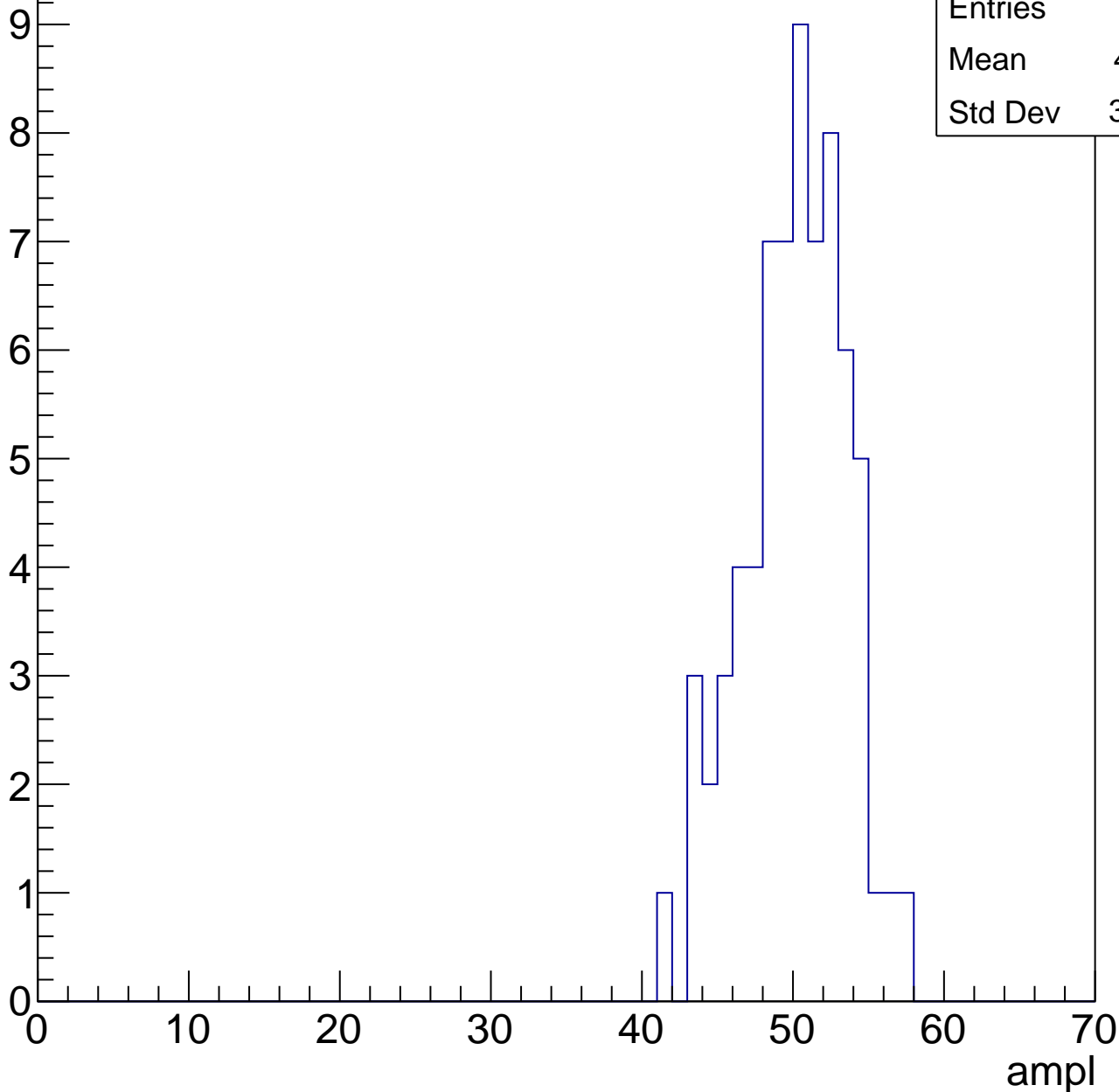


# B1L102S, U16-ch5, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	49.61
Std Dev	3.367

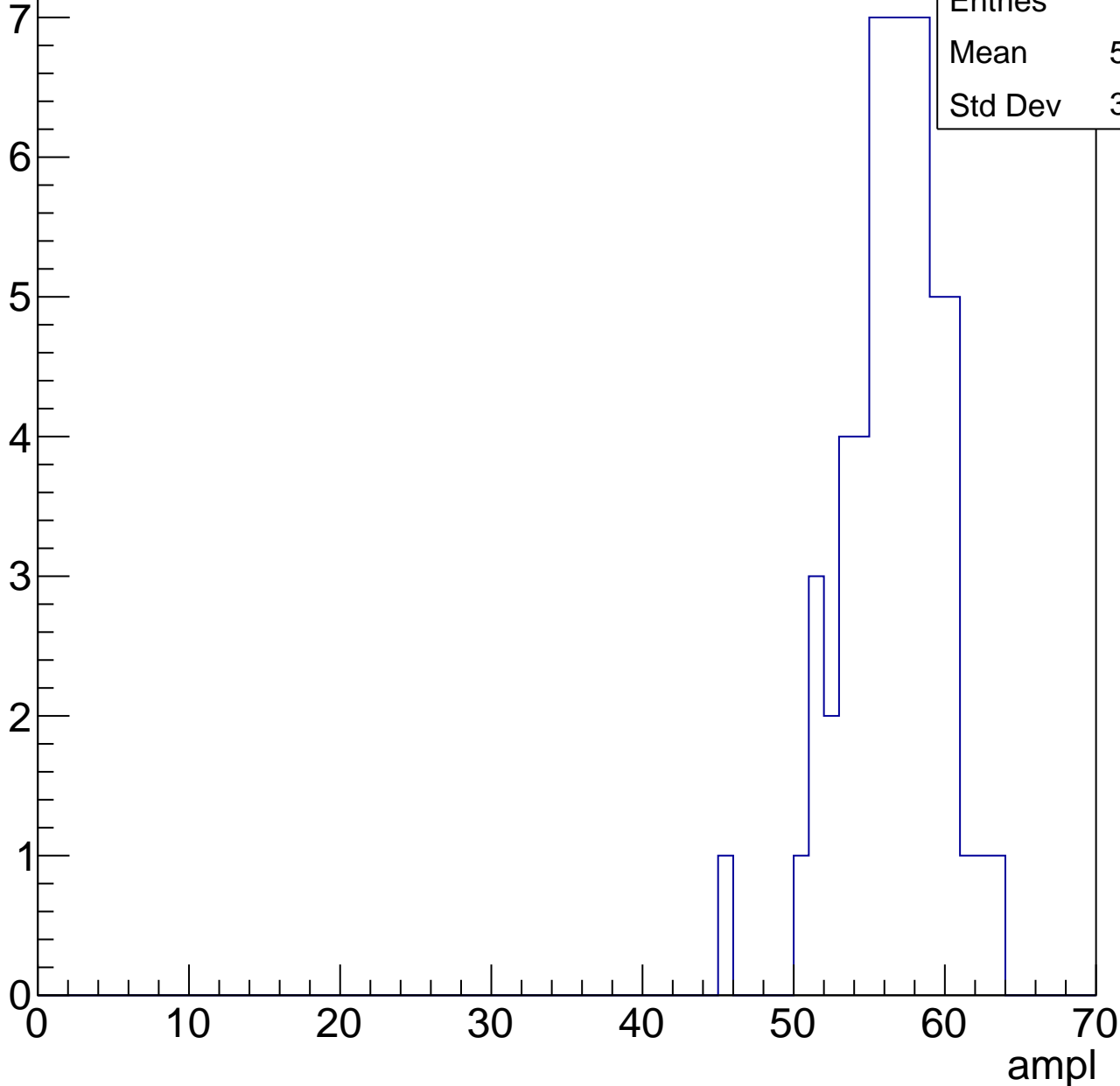


# B1L102S, U16-ch5, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	56.12
Std Dev	3.252

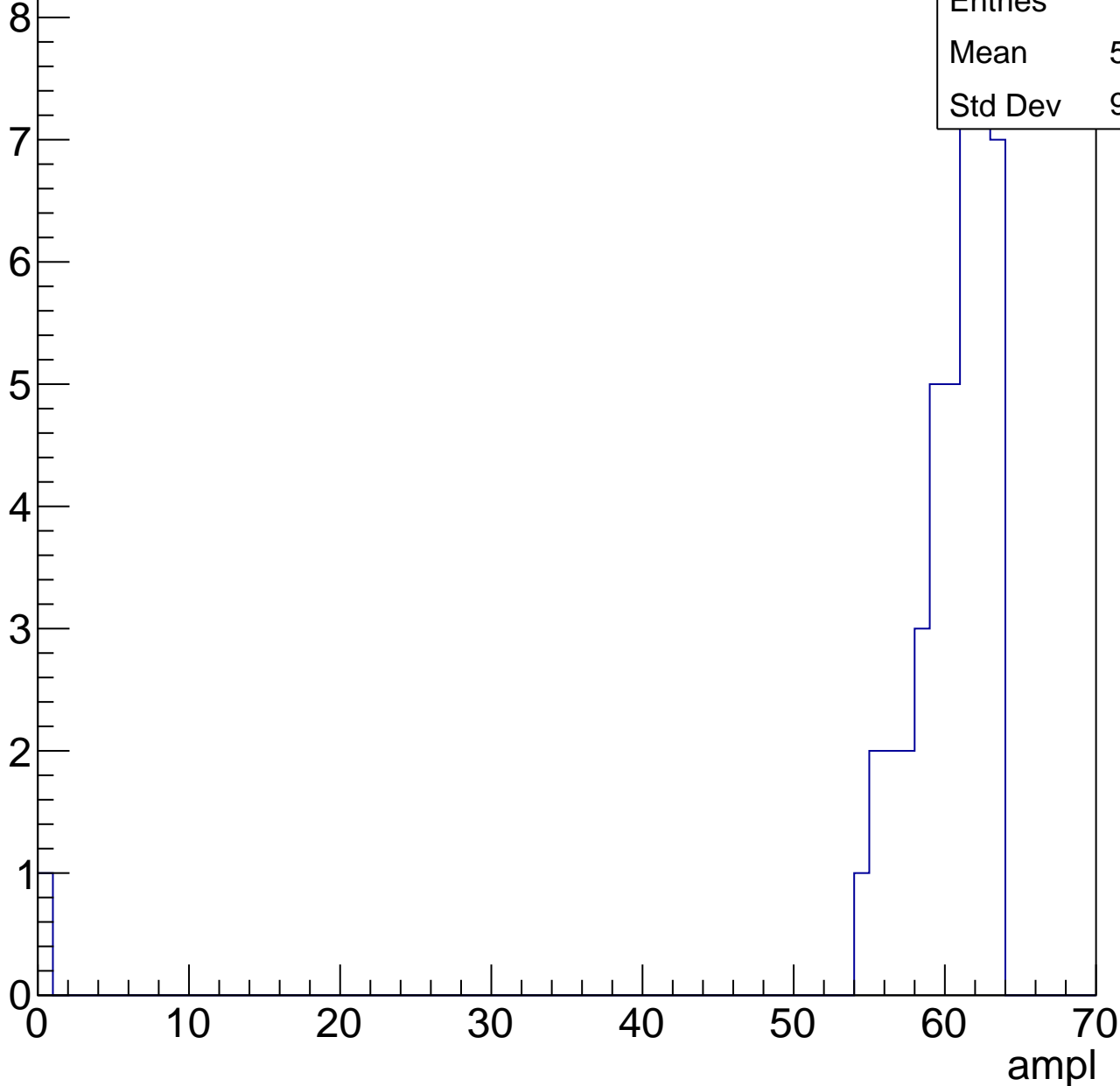


# B1L102S, U16-ch5, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

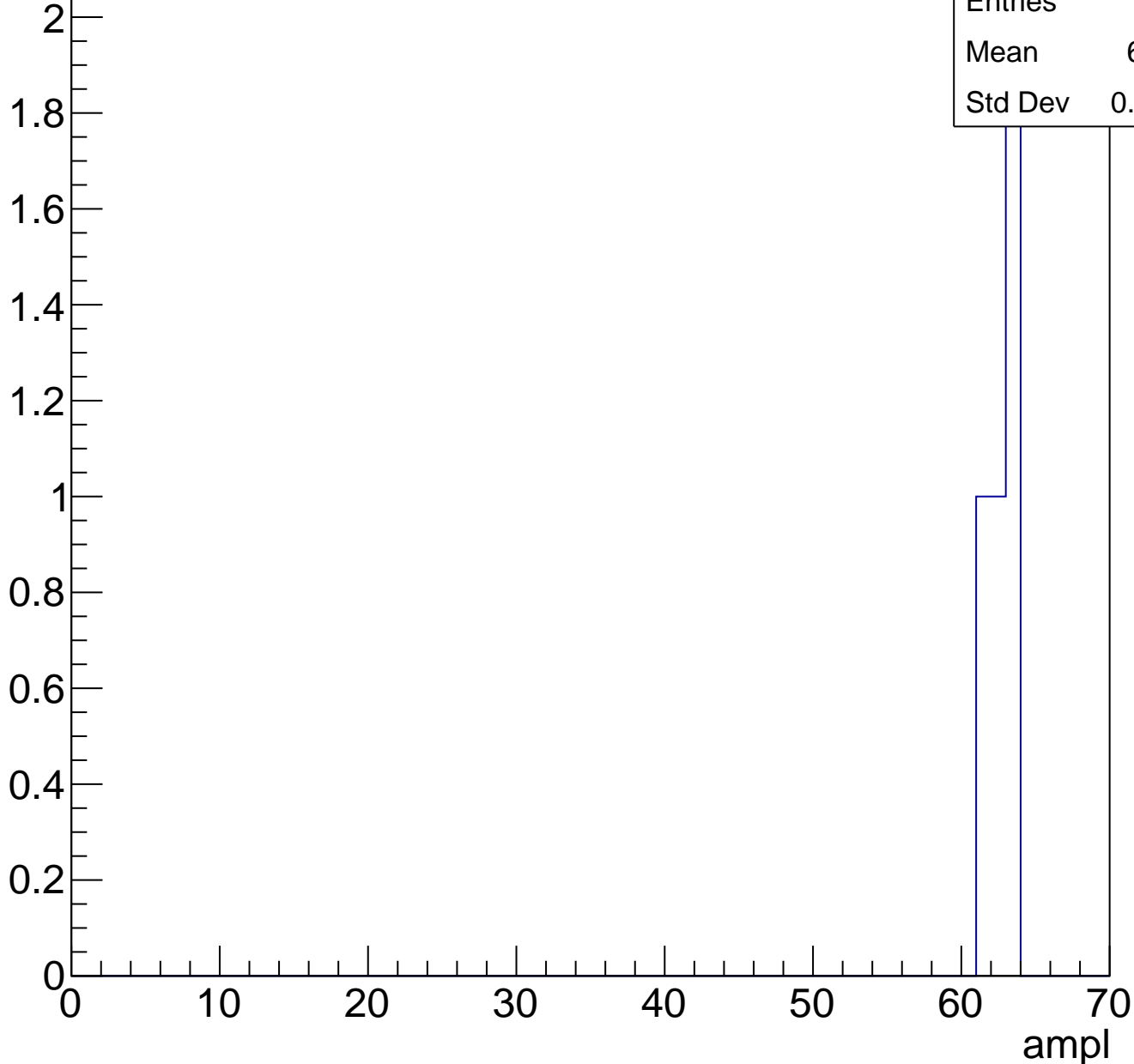
Entries	44
Mean	58.73
Std Dev	9.275



# B1L102S, U16-ch5, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch5, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U16-ch6, adc0

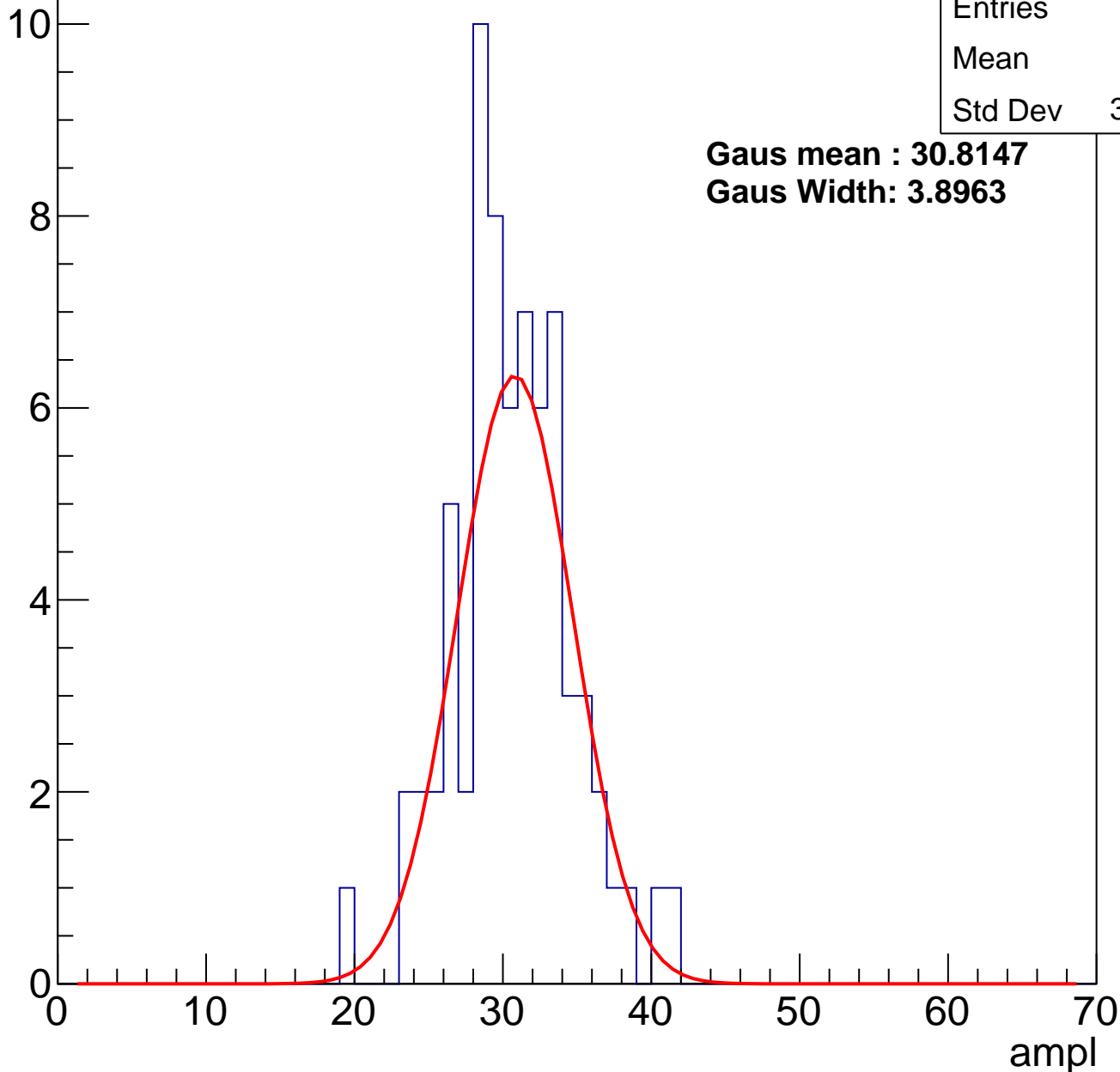
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	70
Mean	30.2
Std Dev	3.977

**Gaus mean : 30.8147**

**Gaus Width: 3.8963**

Entry



# B1L102S, U16-ch6, adc1

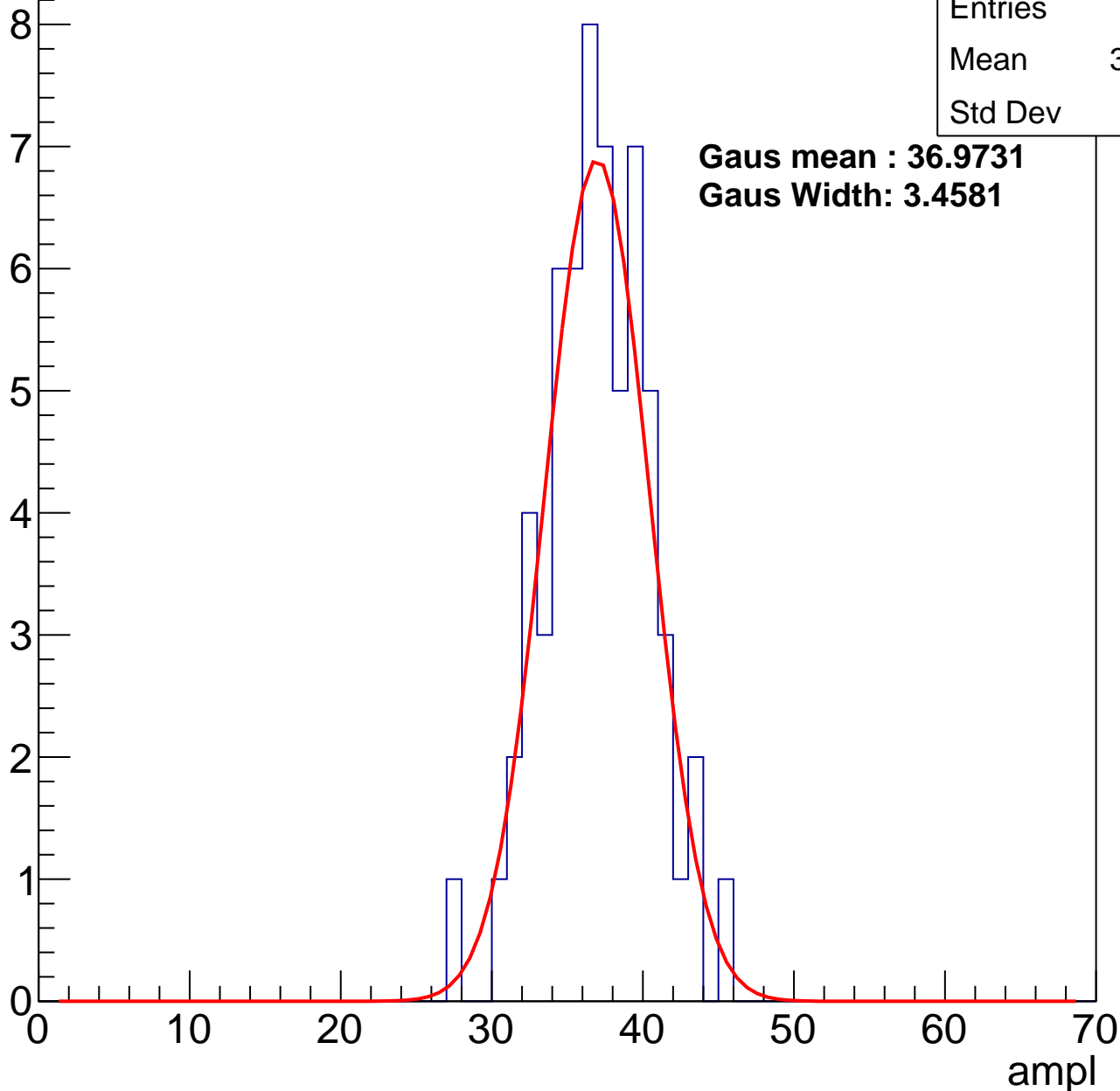
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	36.55
Std Dev	3.43

**Gaus mean : 36.9731**

**Gaus Width: 3.4581**



# B1L102S, U16-ch6, adc2

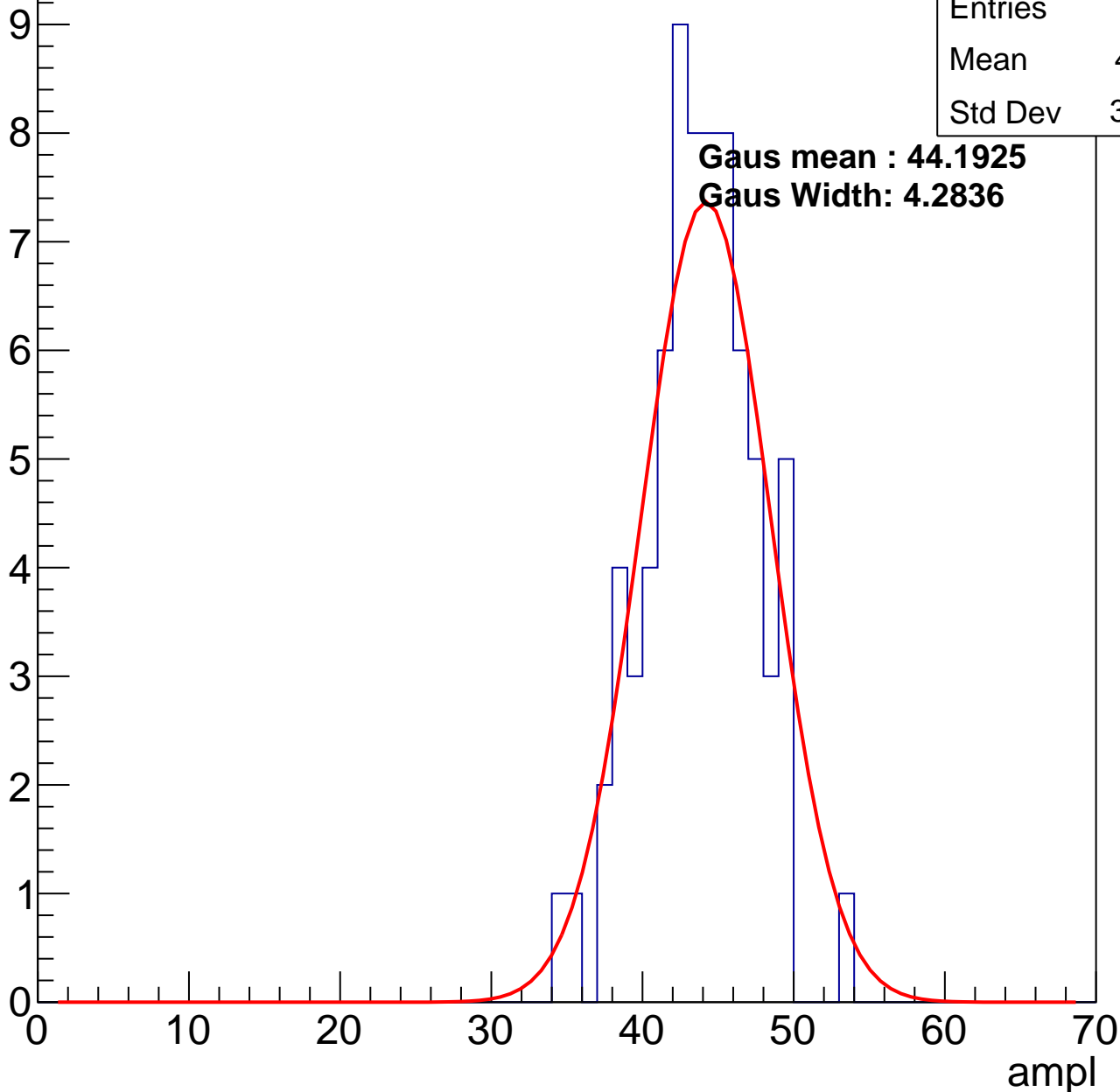
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	43.31
Std Dev	3.594

**Gaus mean : 44.1925**

**Gaus Width: 4.2836**



# B1L102S, U16-ch6, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

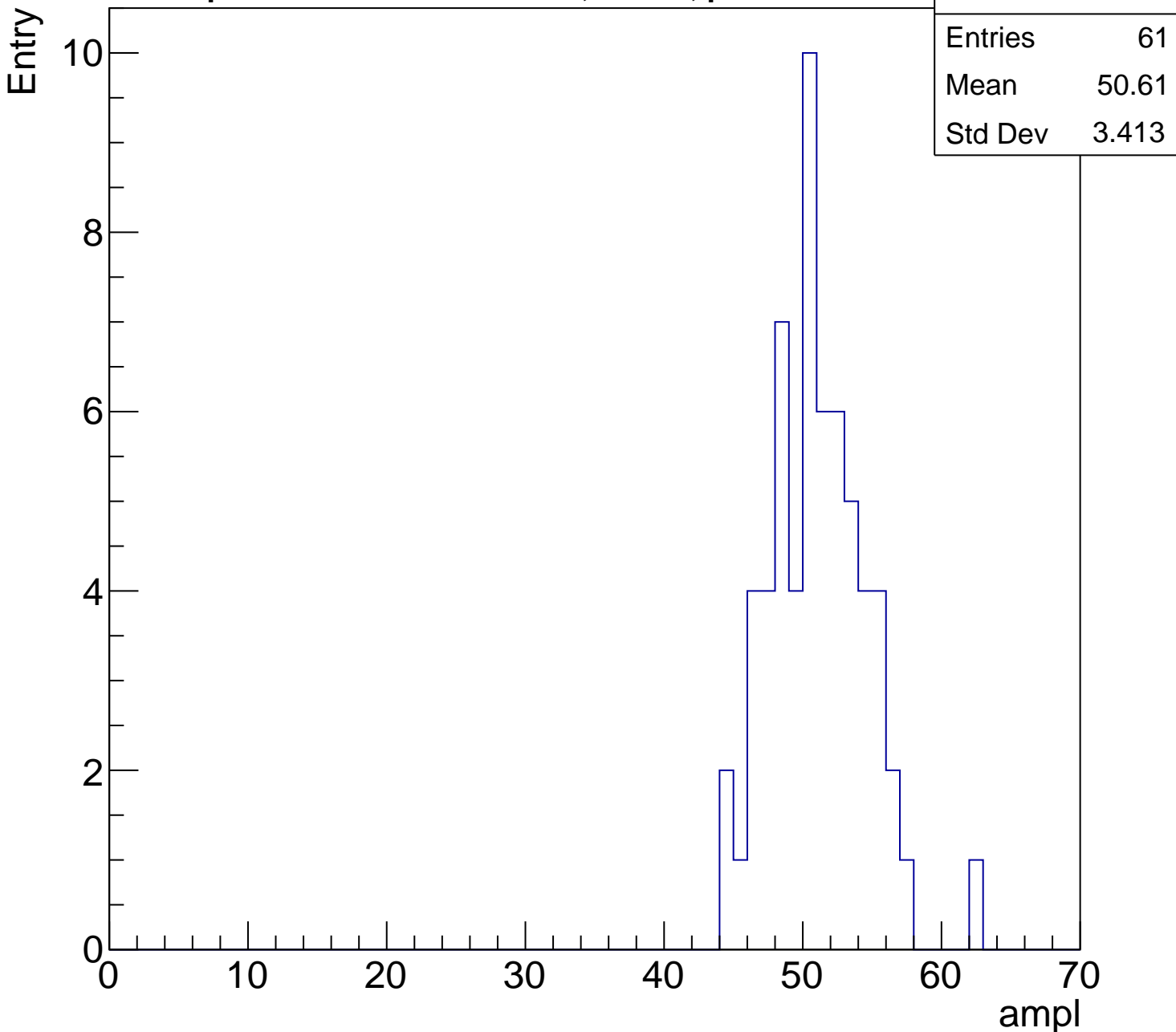
Entries	61
Mean	50.61
Std Dev	3.413

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

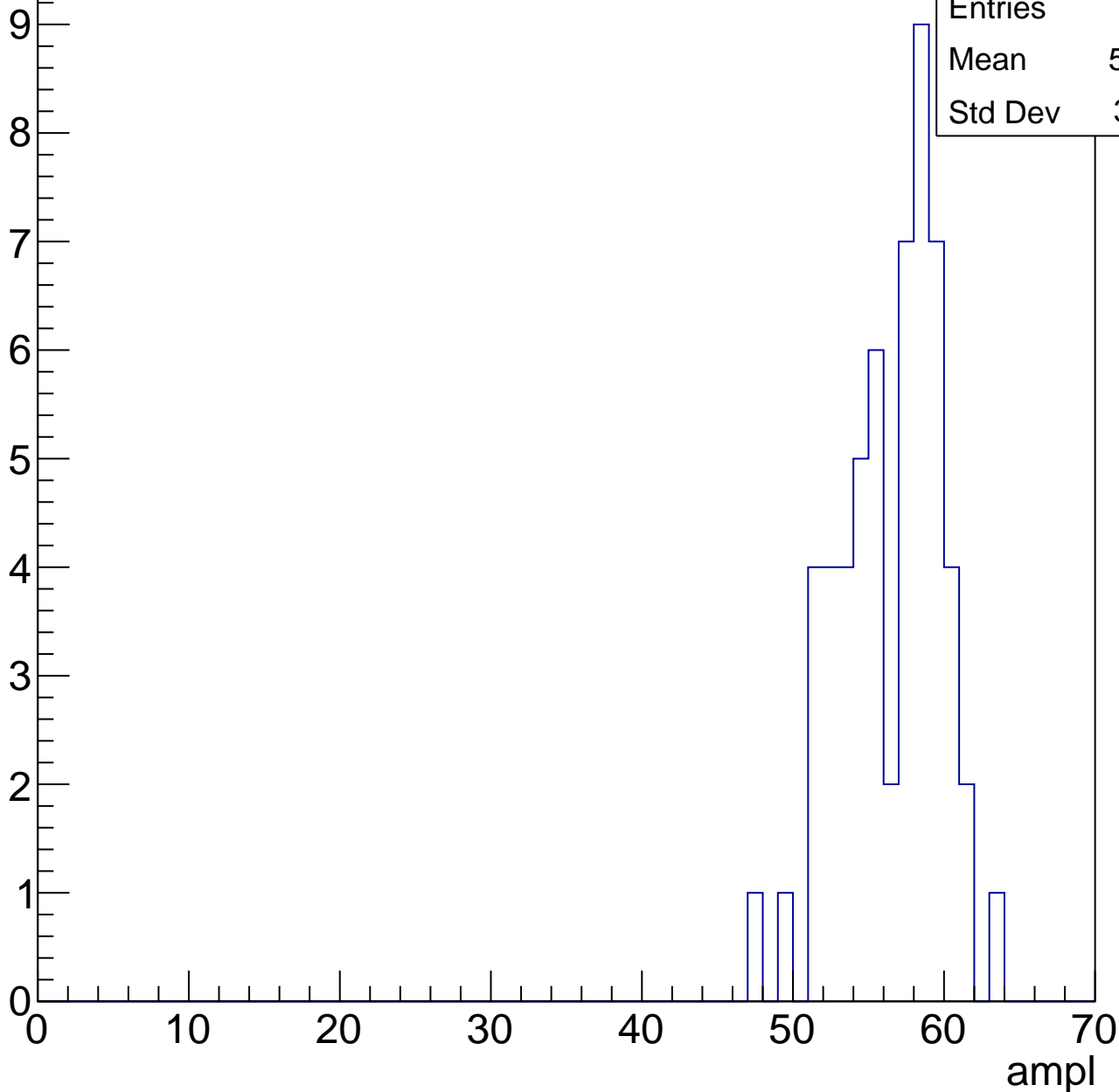


# B1L102S, U16-ch6, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	55.98
Std Dev	3.311

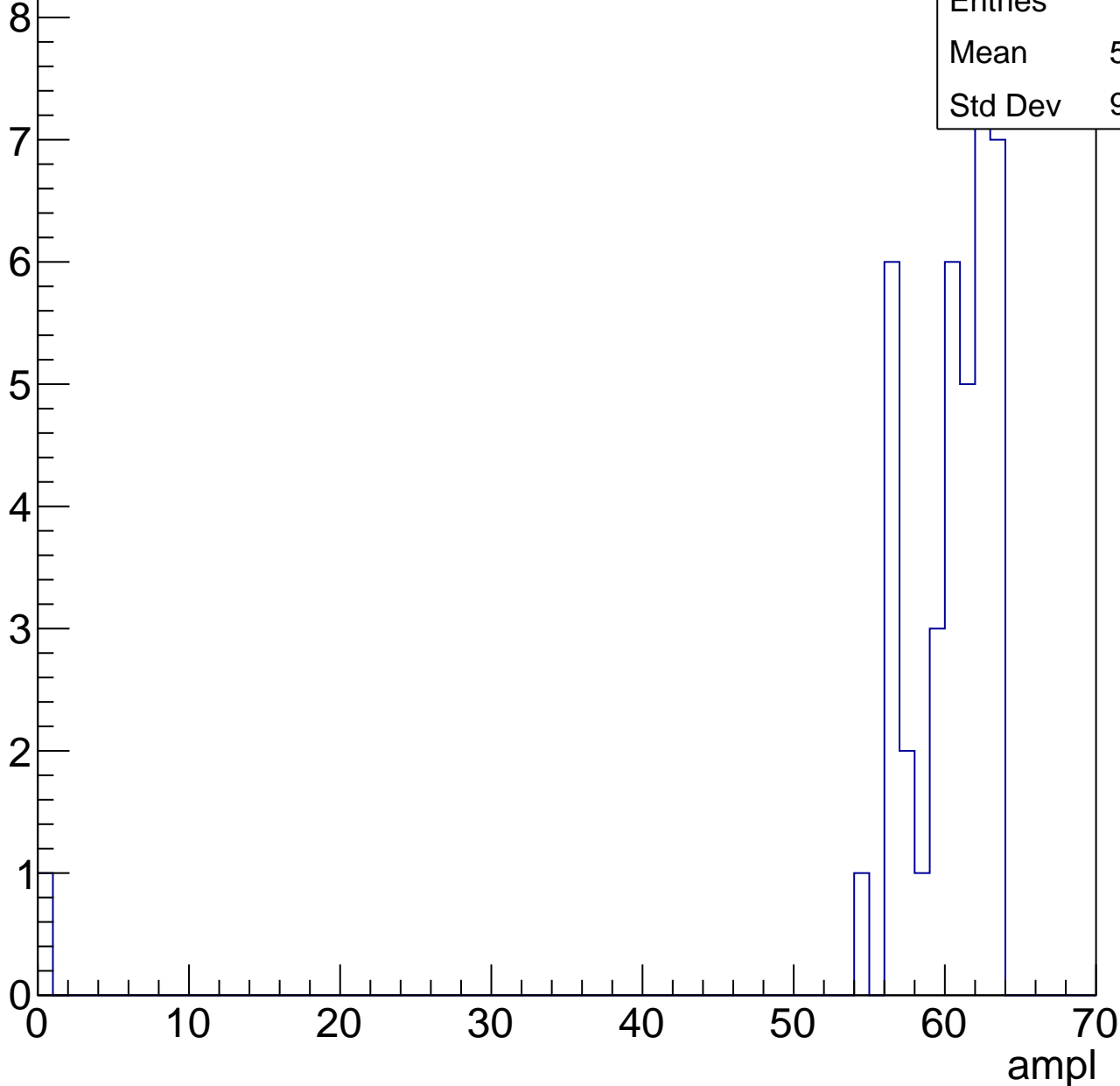


# B1L102S, U16-ch6, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	58.52
Std Dev	9.708



# B1L102S, U16-ch6, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

ampl

Entries

6

Mean

61.83

Std Dev

0.8975



# B1L102S, U16-ch6, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch7, adc0

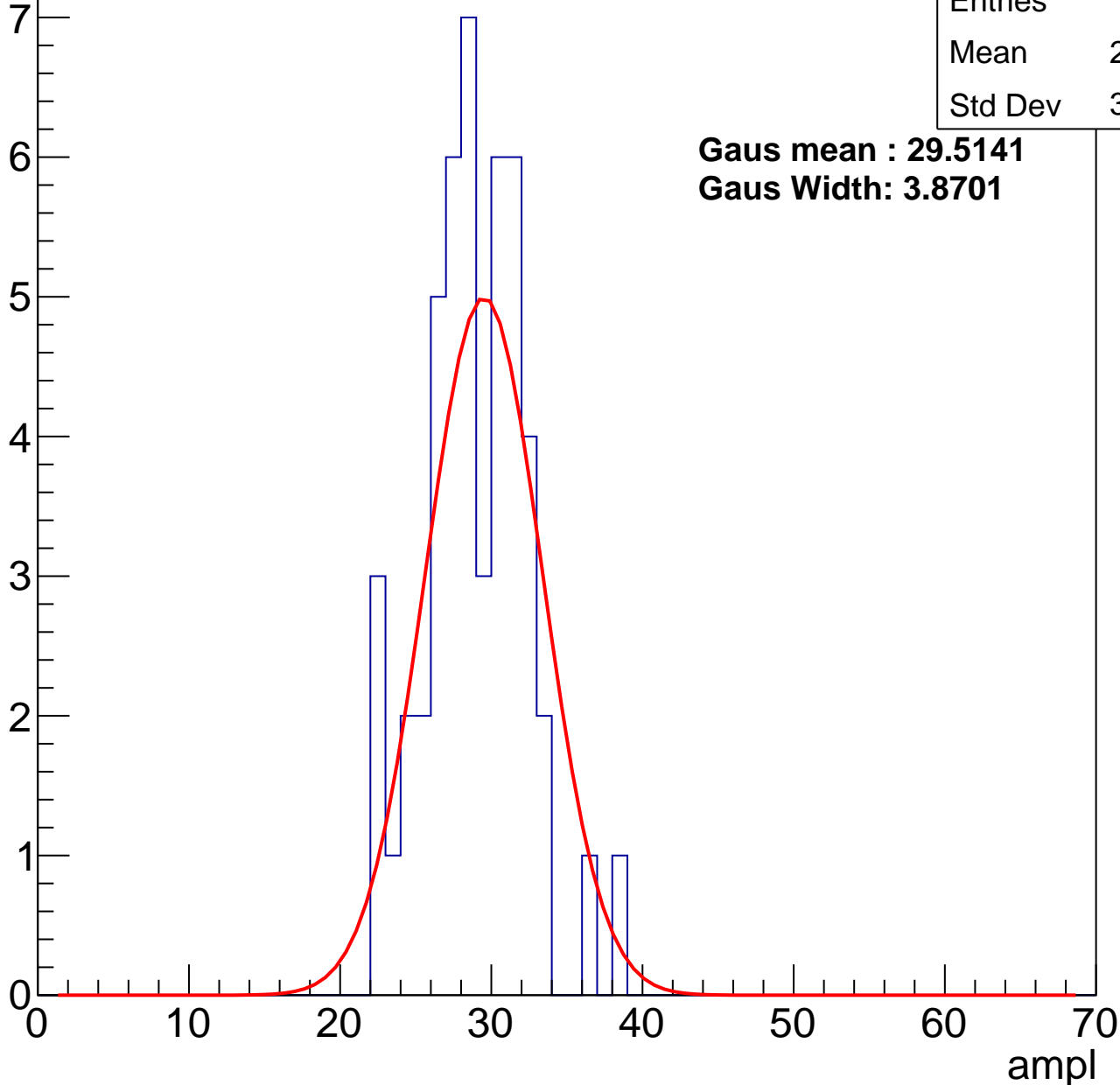
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	28.49
Std Dev	3.369

**Gaus mean : 29.5141**

**Gaus Width: 3.8701**



# B1L102S, U16-ch7, adc1

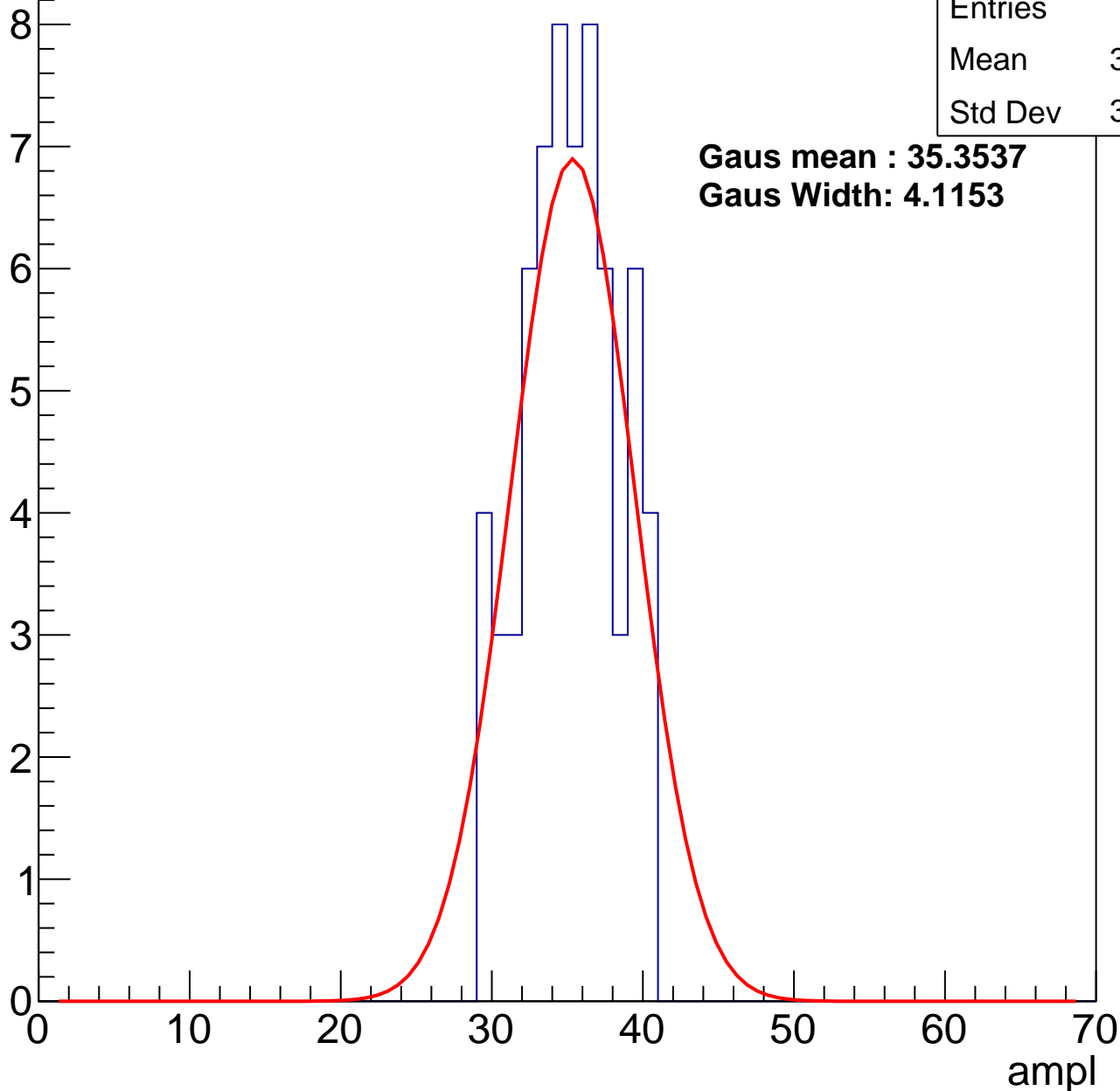
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	34.72
Std Dev	3.056

**Gaus mean : 35.3537**

**Gaus Width: 4.1153**



# B1L102S, U16-ch7, adc2

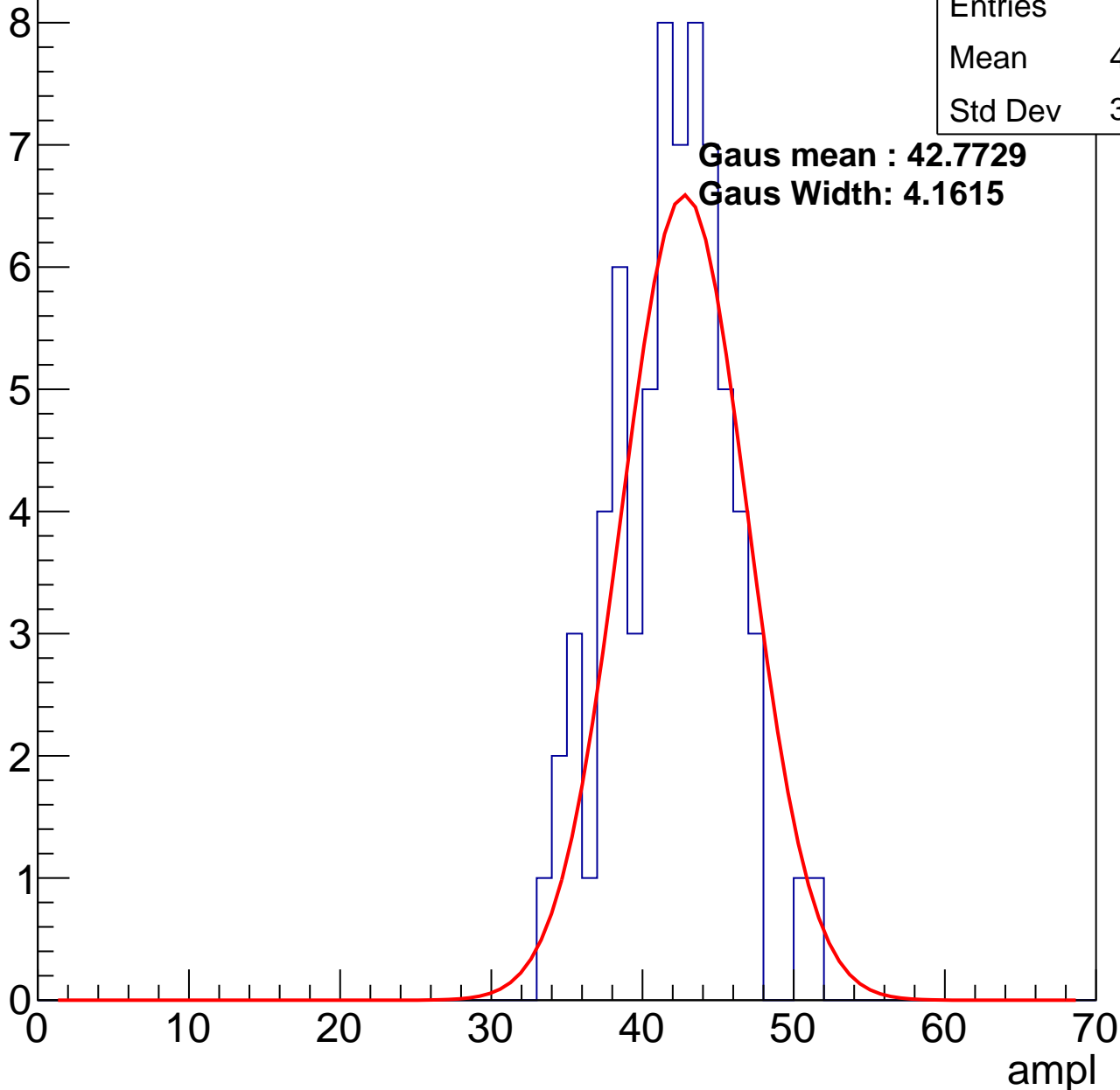
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	41.45
Std Dev	3.782

**Gaus mean : 42.7729**

**Gaus Width: 4.1615**

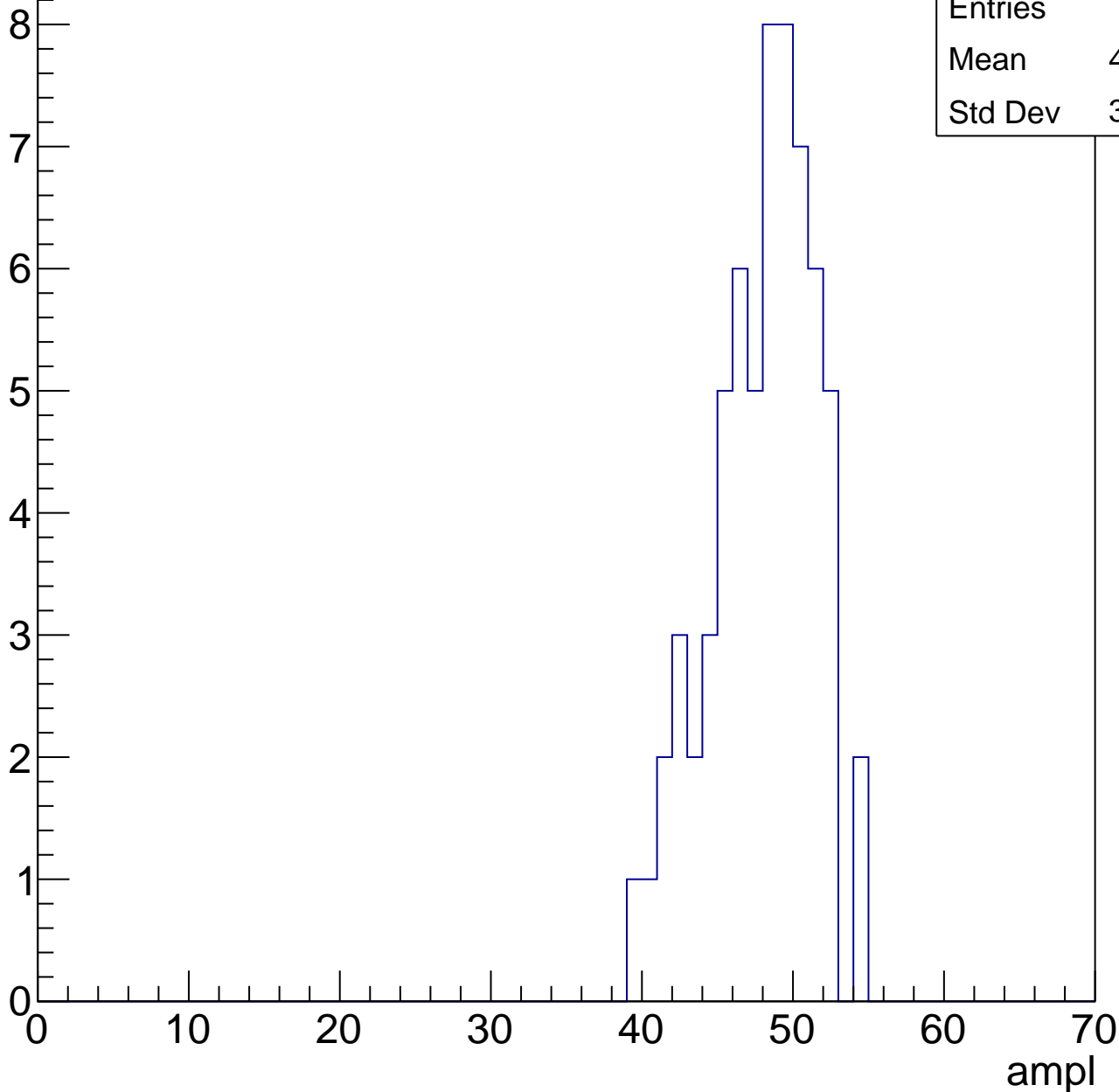


# B1L102S, U16-ch7, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

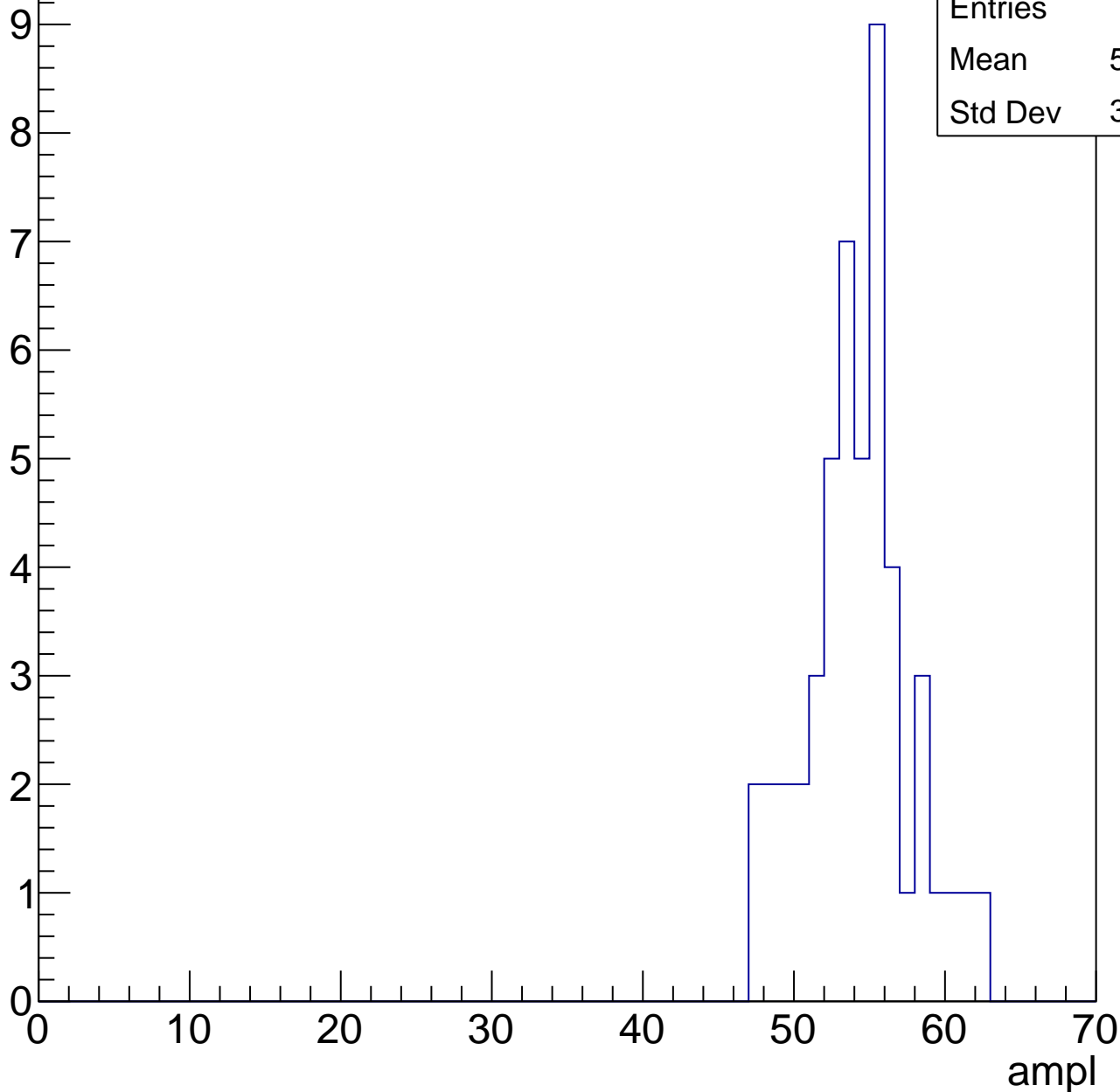
Entries	64
Mean	47.52
Std Dev	3.423



# B1L102S, U16-ch7, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

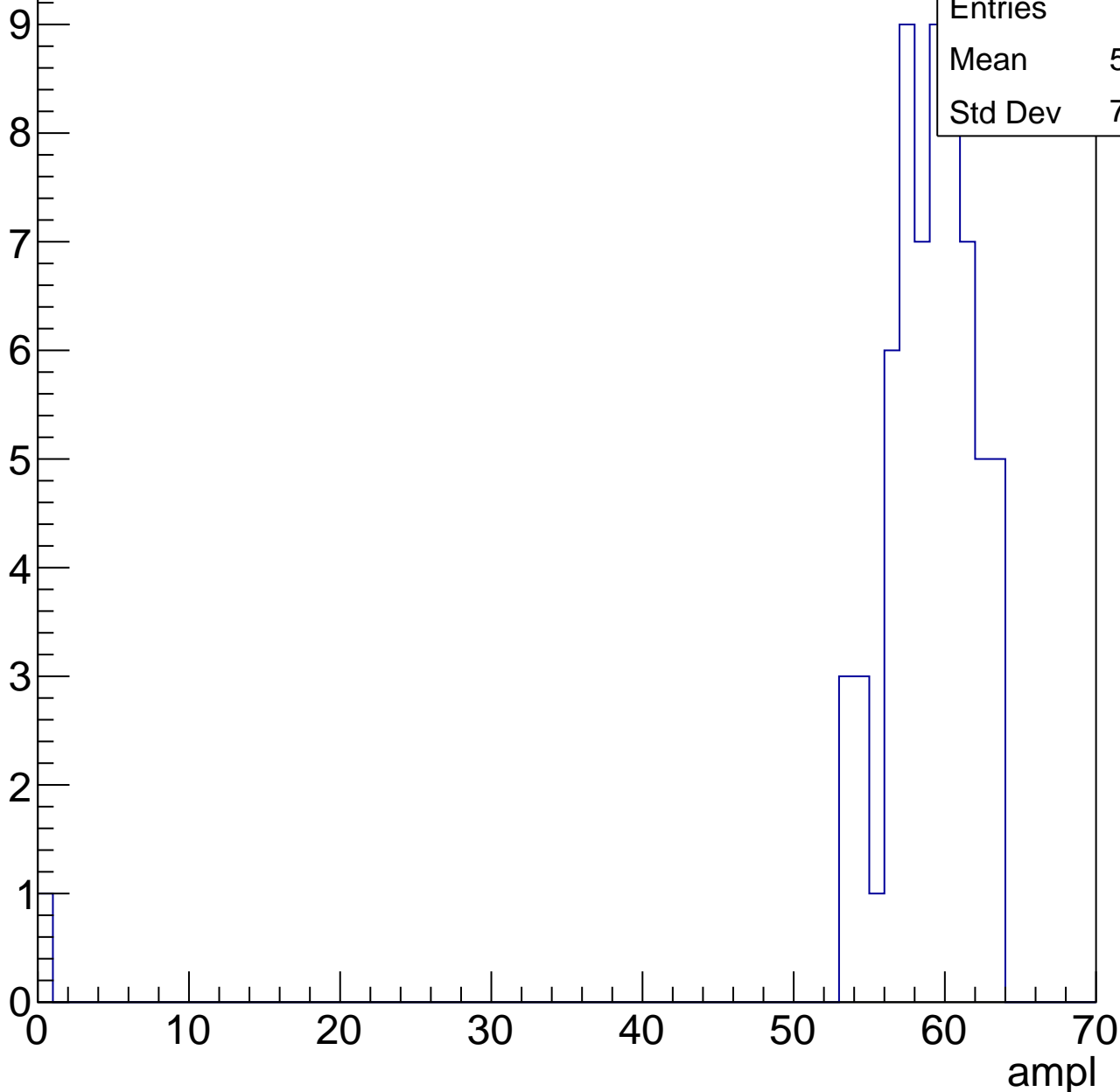


# B1L102S, U16-ch7, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	57.75
Std Dev	7.684

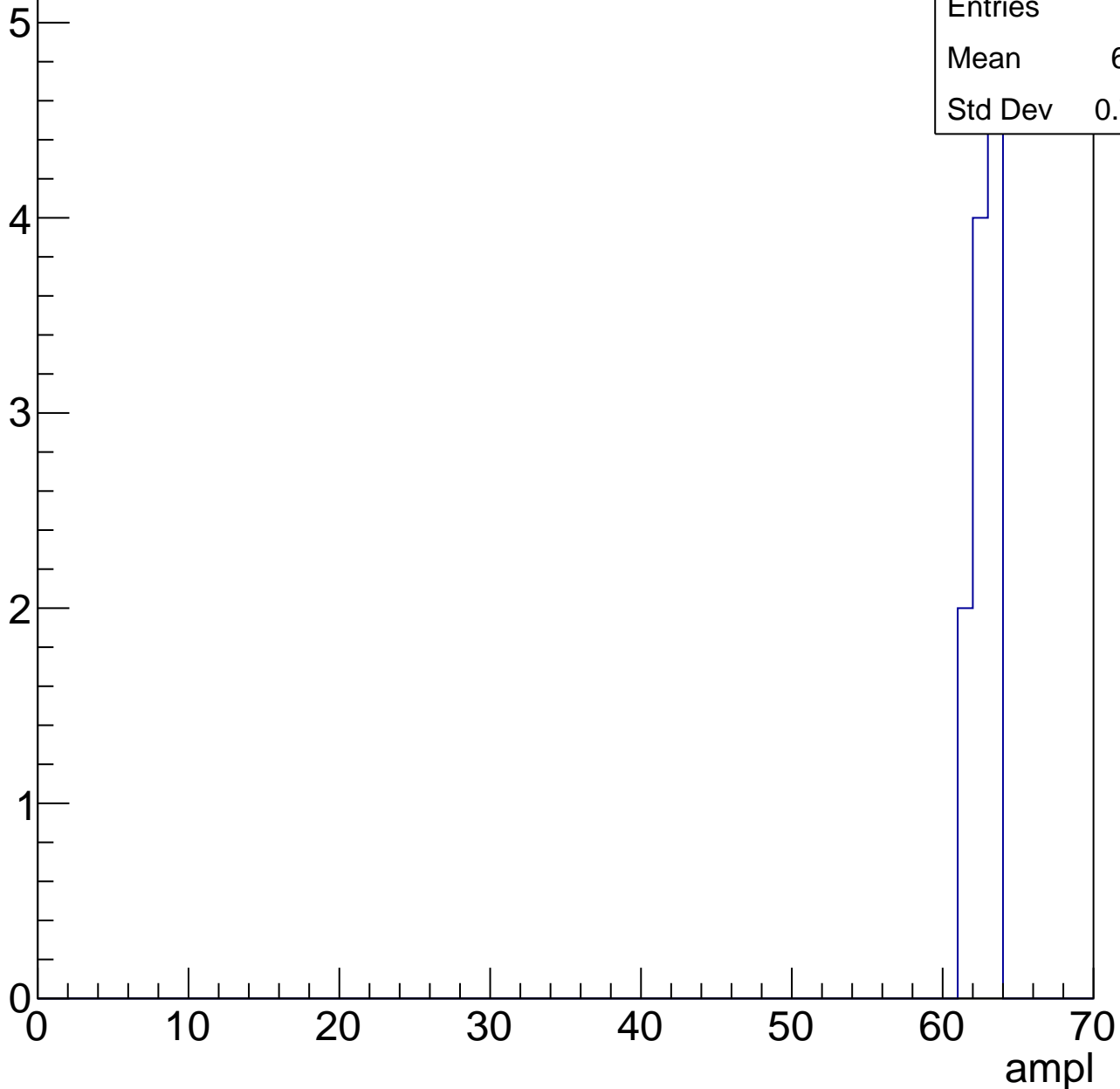


# B1L102S, U16-ch7, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	11
Mean	62.27
Std Dev	0.7497





# B1L102S, U16-ch7, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch8, adc0

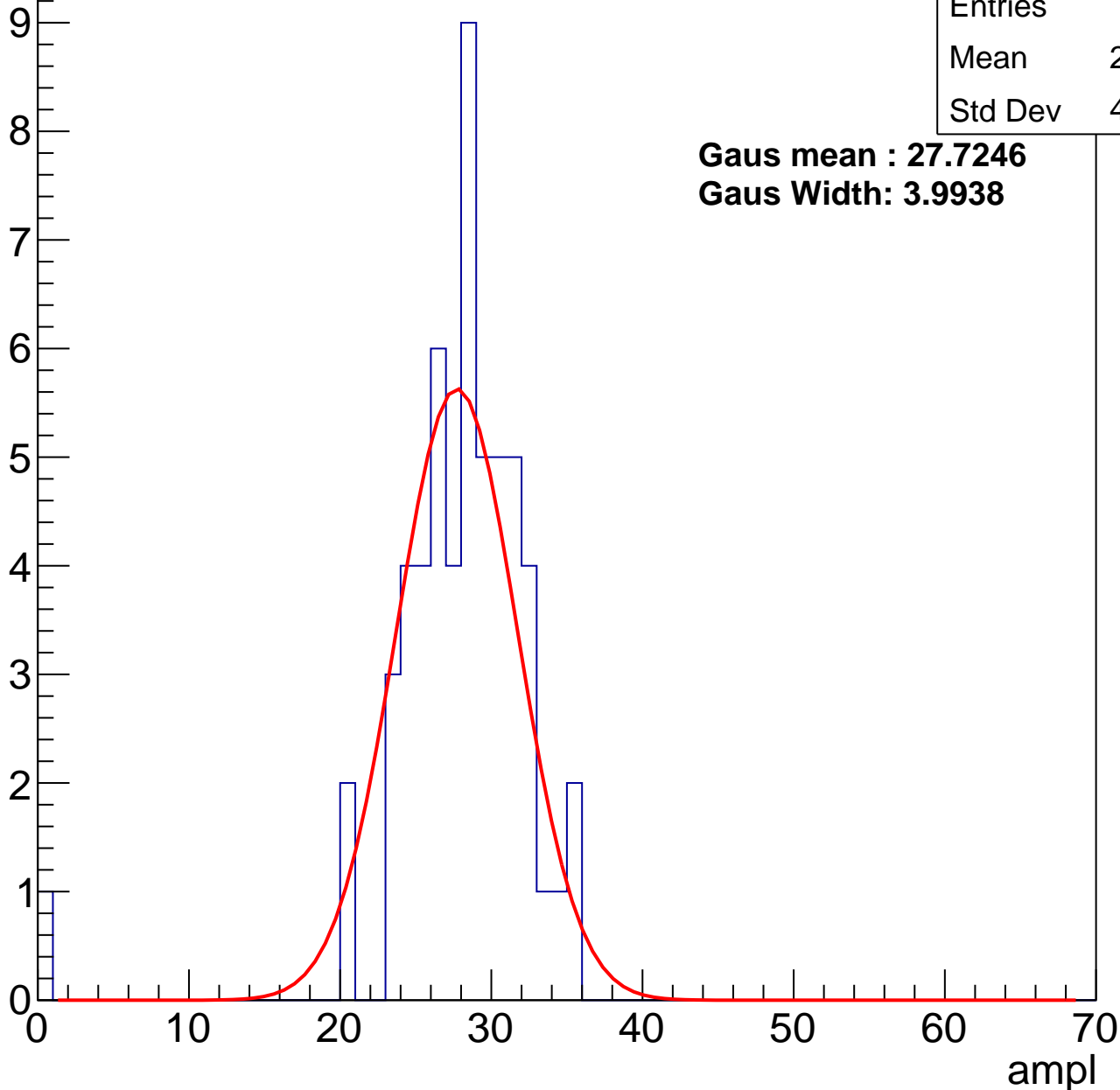
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	27.43
Std Dev	4.982

**Gaus mean : 27.7246**

**Gaus Width: 3.9938**



# B1L102S, U16-ch8, adc1

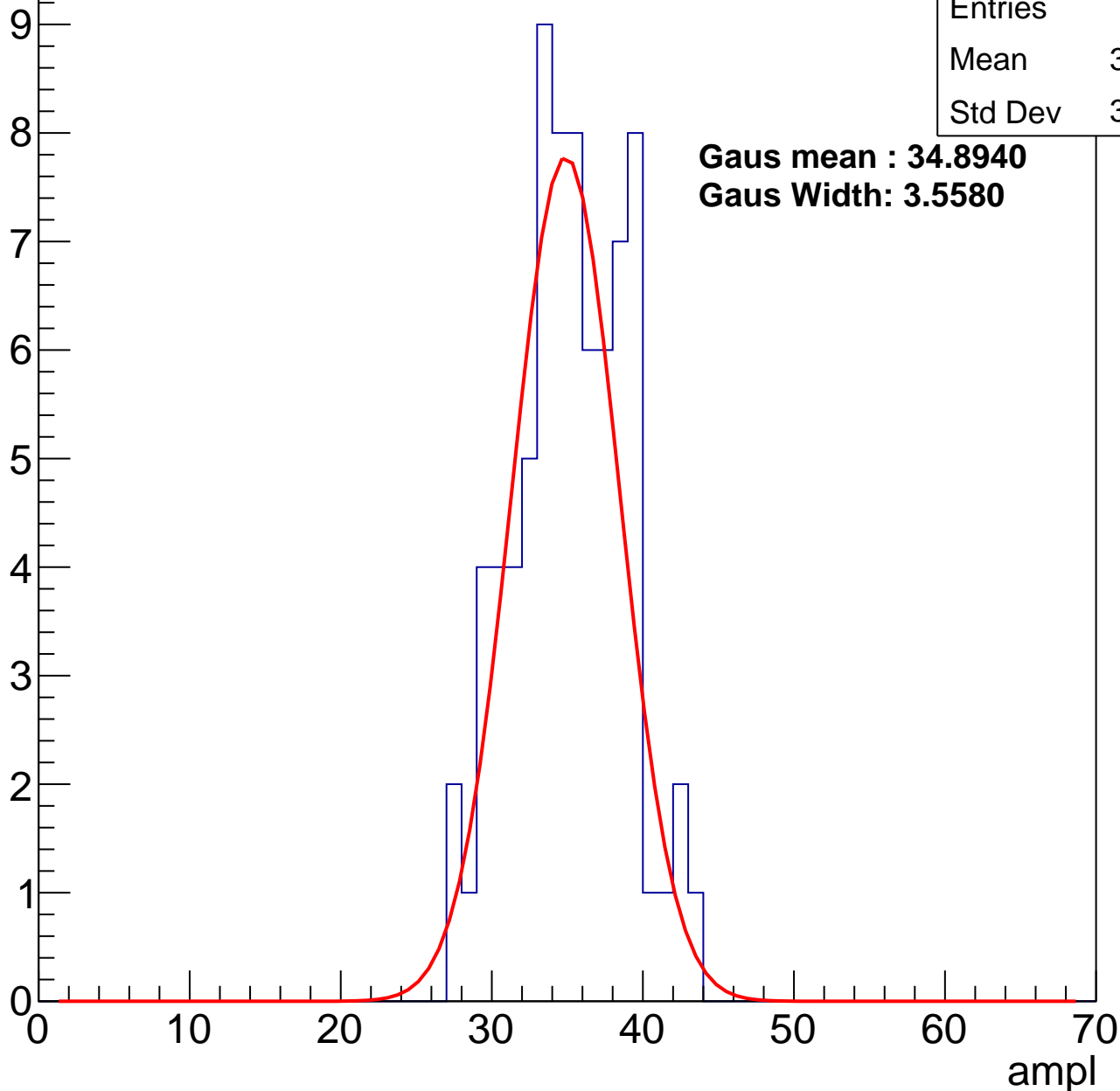
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	34.74
Std Dev	3.627

**Gaus mean : 34.8940**

**Gaus Width: 3.5580**



# B1L102S, U16-ch8, adc2

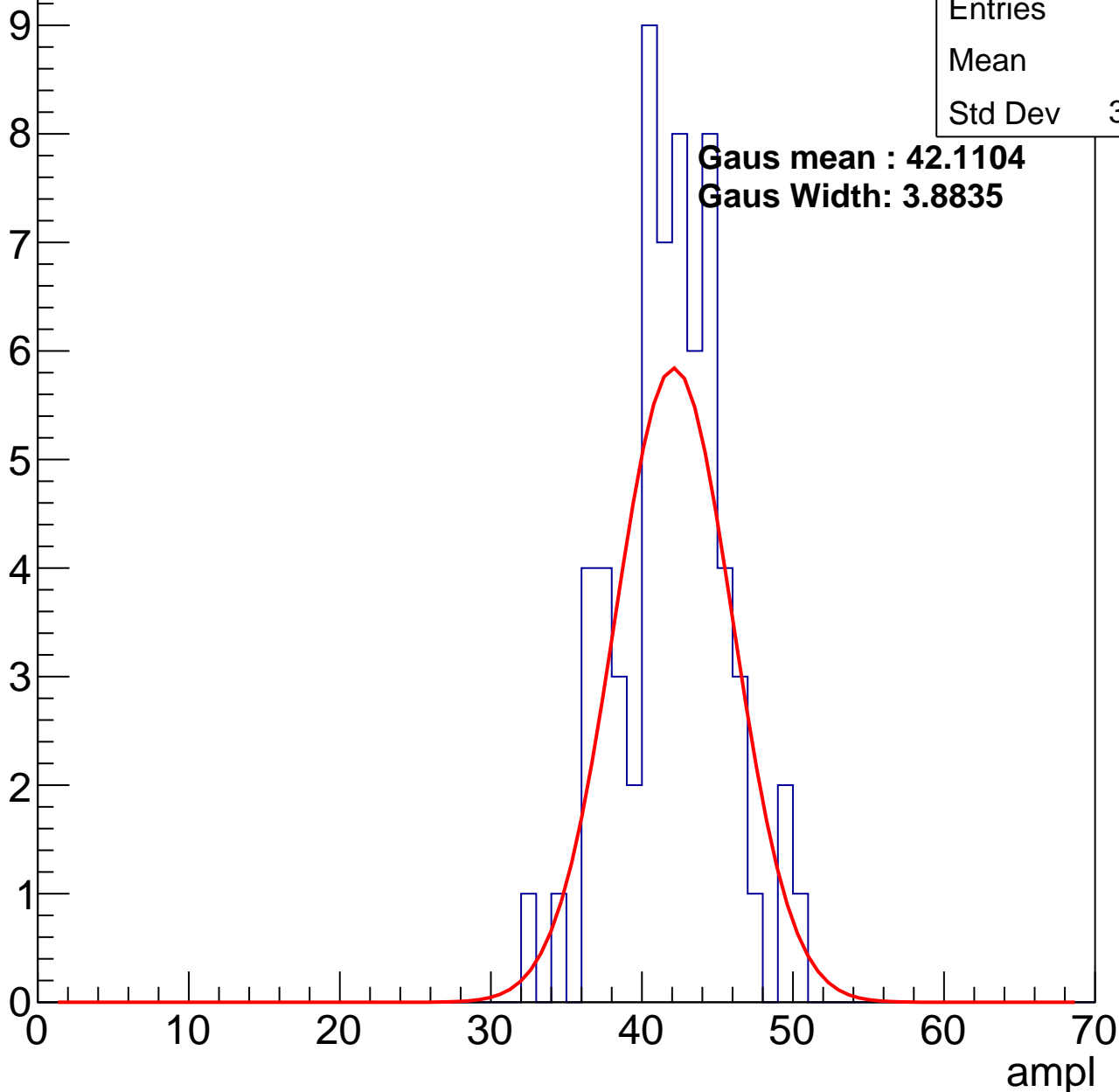
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	41.5
Std Dev	3.558

**Gaus mean : 42.1104**

**Gaus Width: 3.8835**

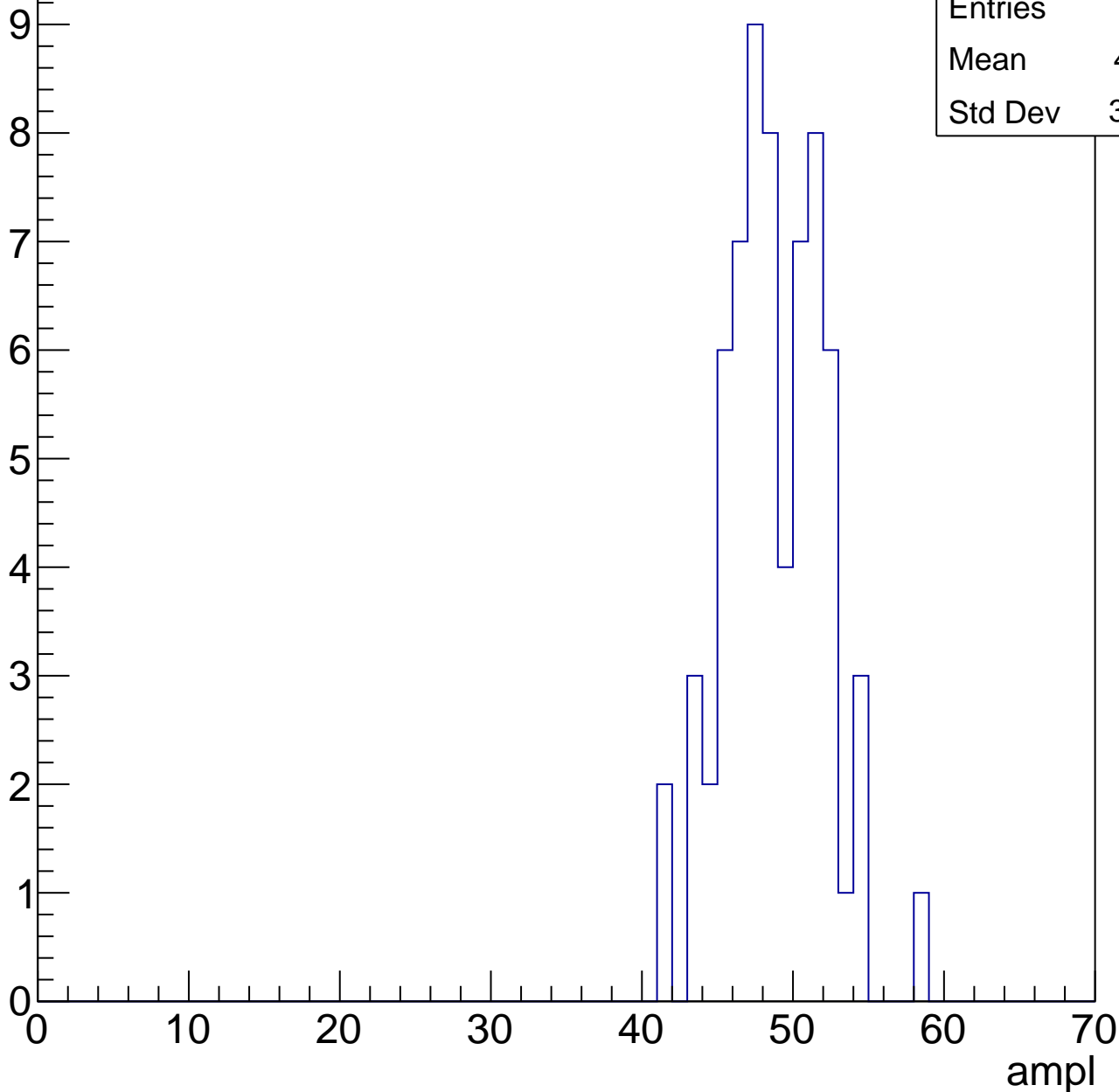


# B1L102S, U16-ch8, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

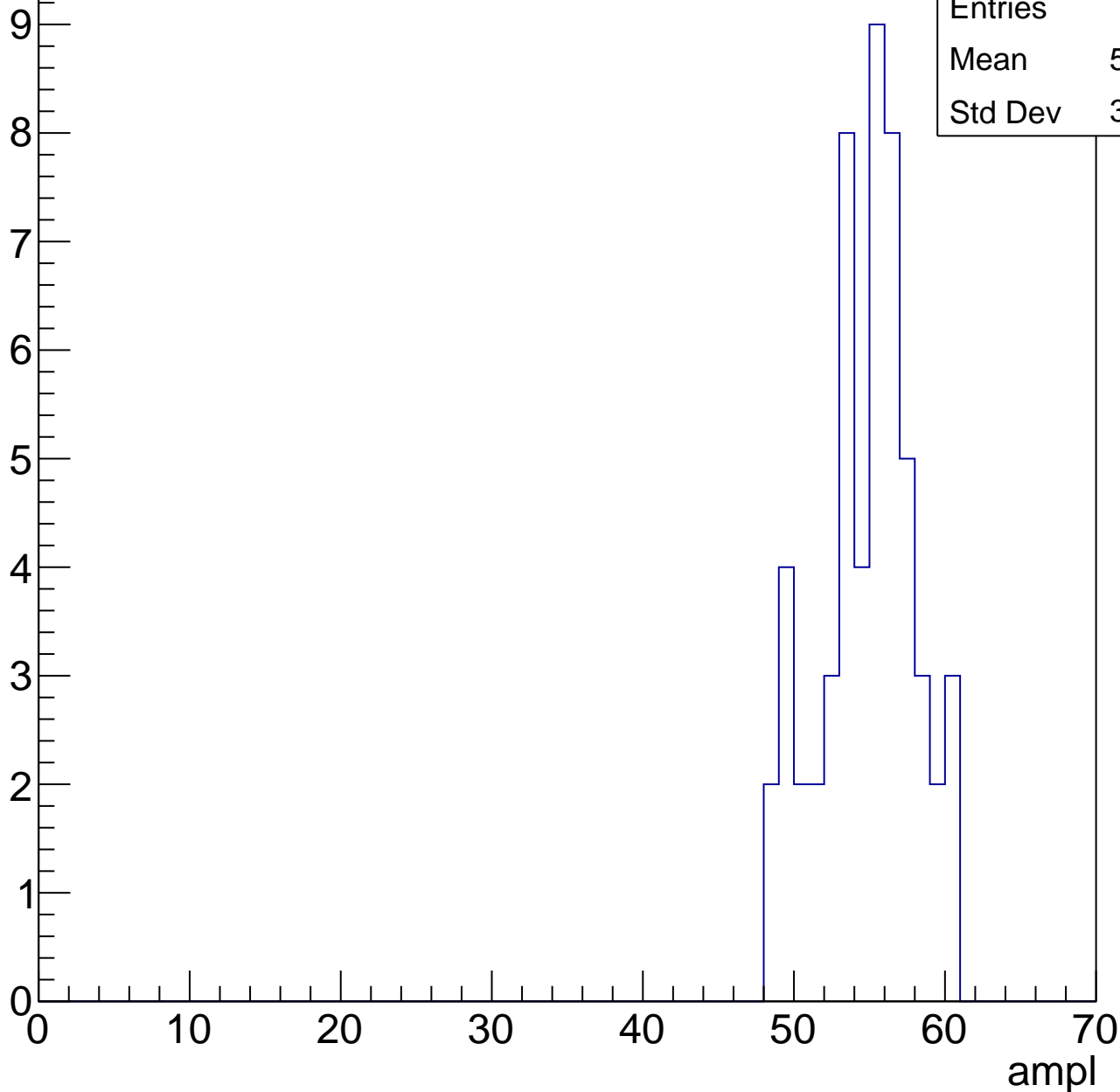
Entries	67
Mean	48.31
Std Dev	3.284



# B1L102S, U16-ch8, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

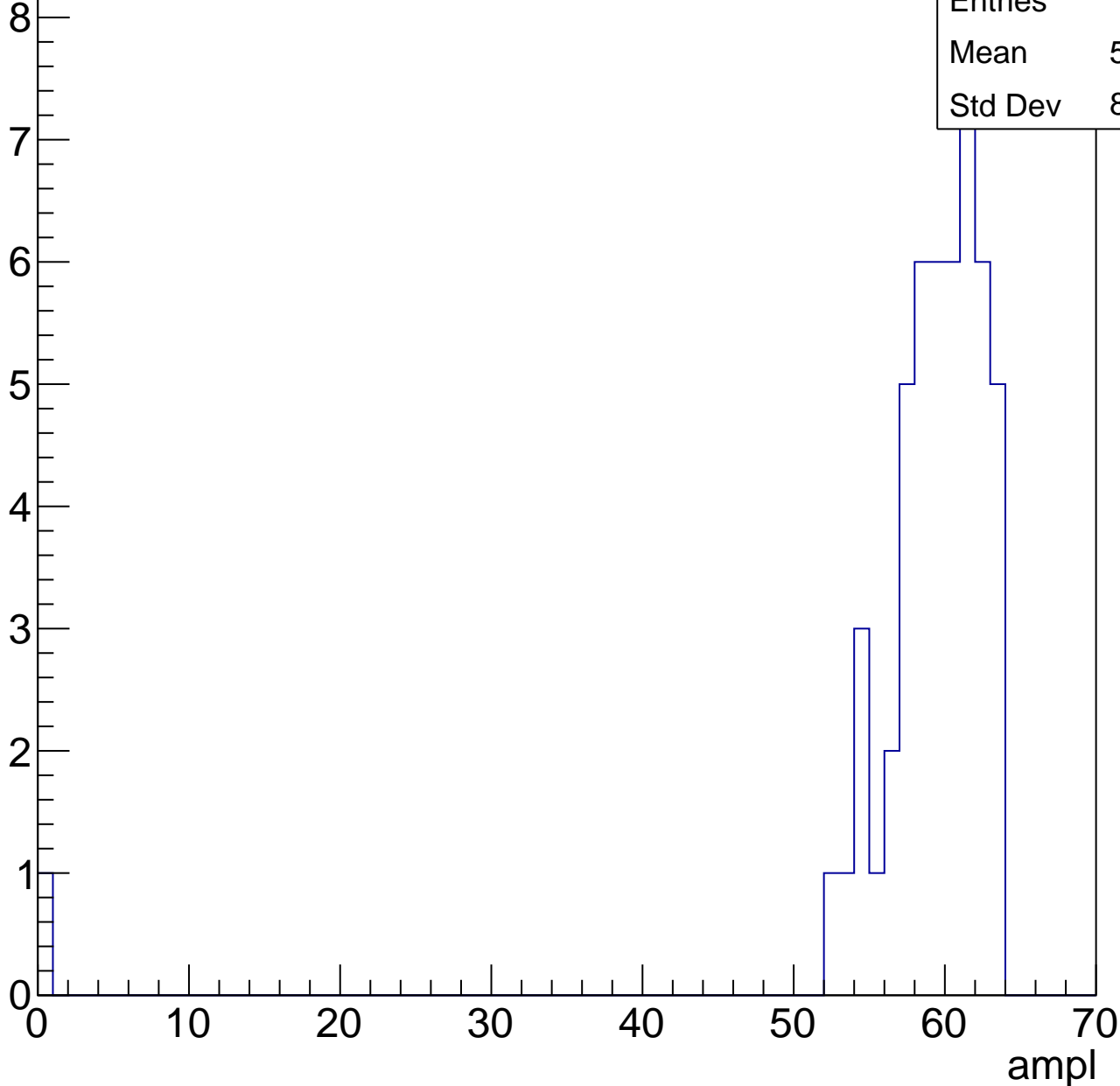


# B1L102S, U16-ch8, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

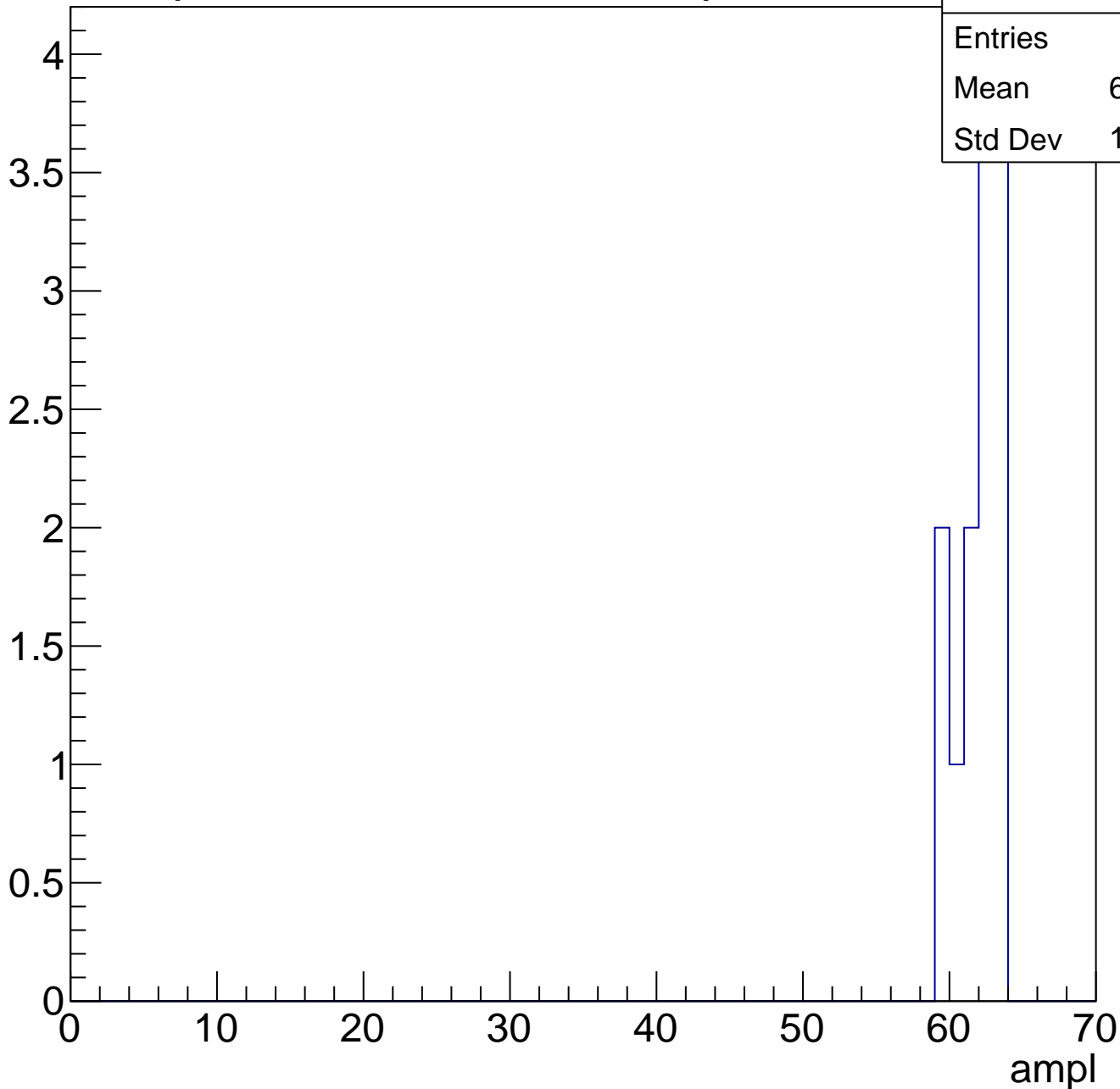
Entries	51
Mean	57.96
Std Dev	8.652



# B1L102S, U16-ch8, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

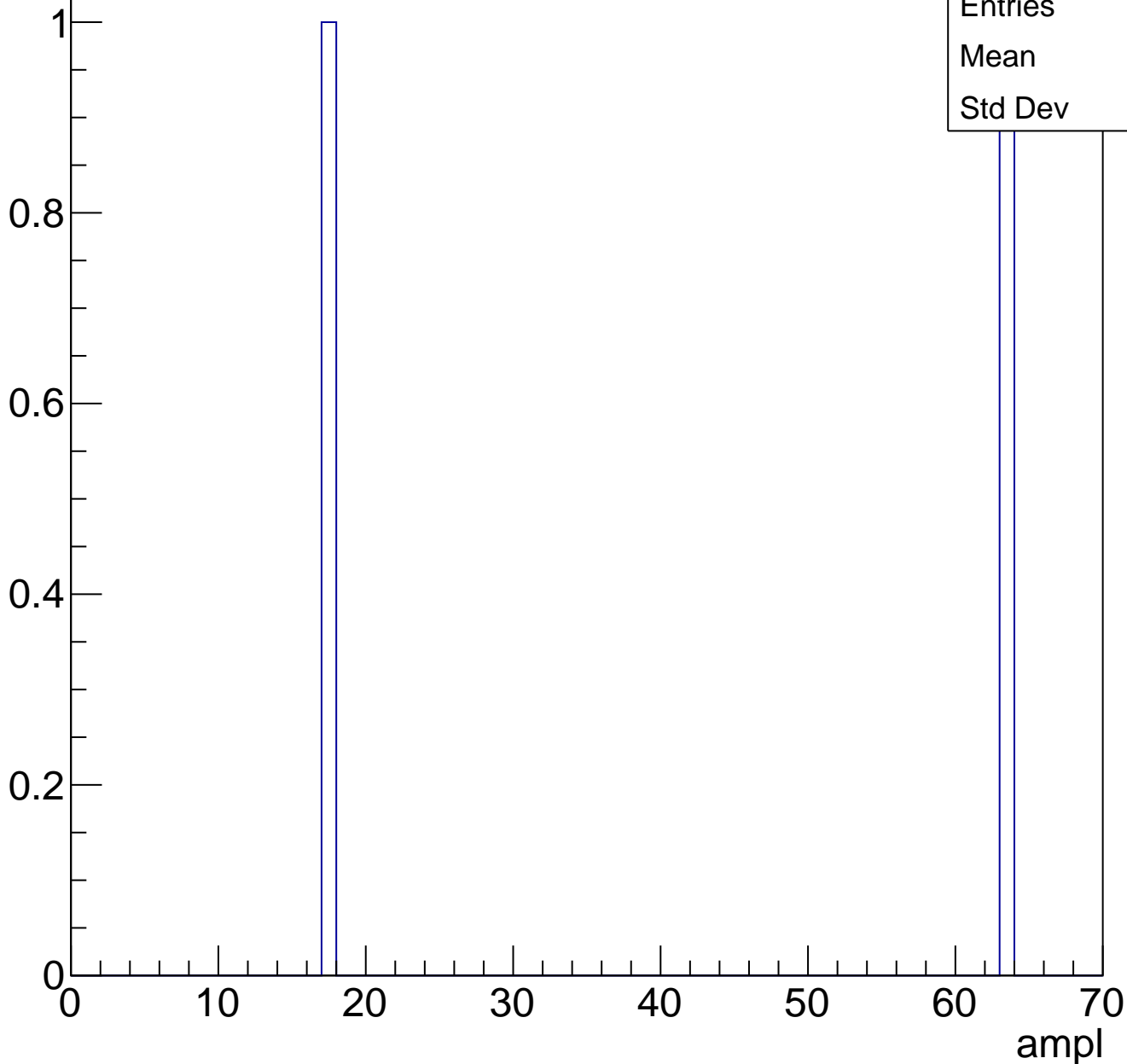




# B1L102S, U16-ch8, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch9, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	75
Mean	29.11
Std Dev	4.914

**Gaus mean : 30.2681**

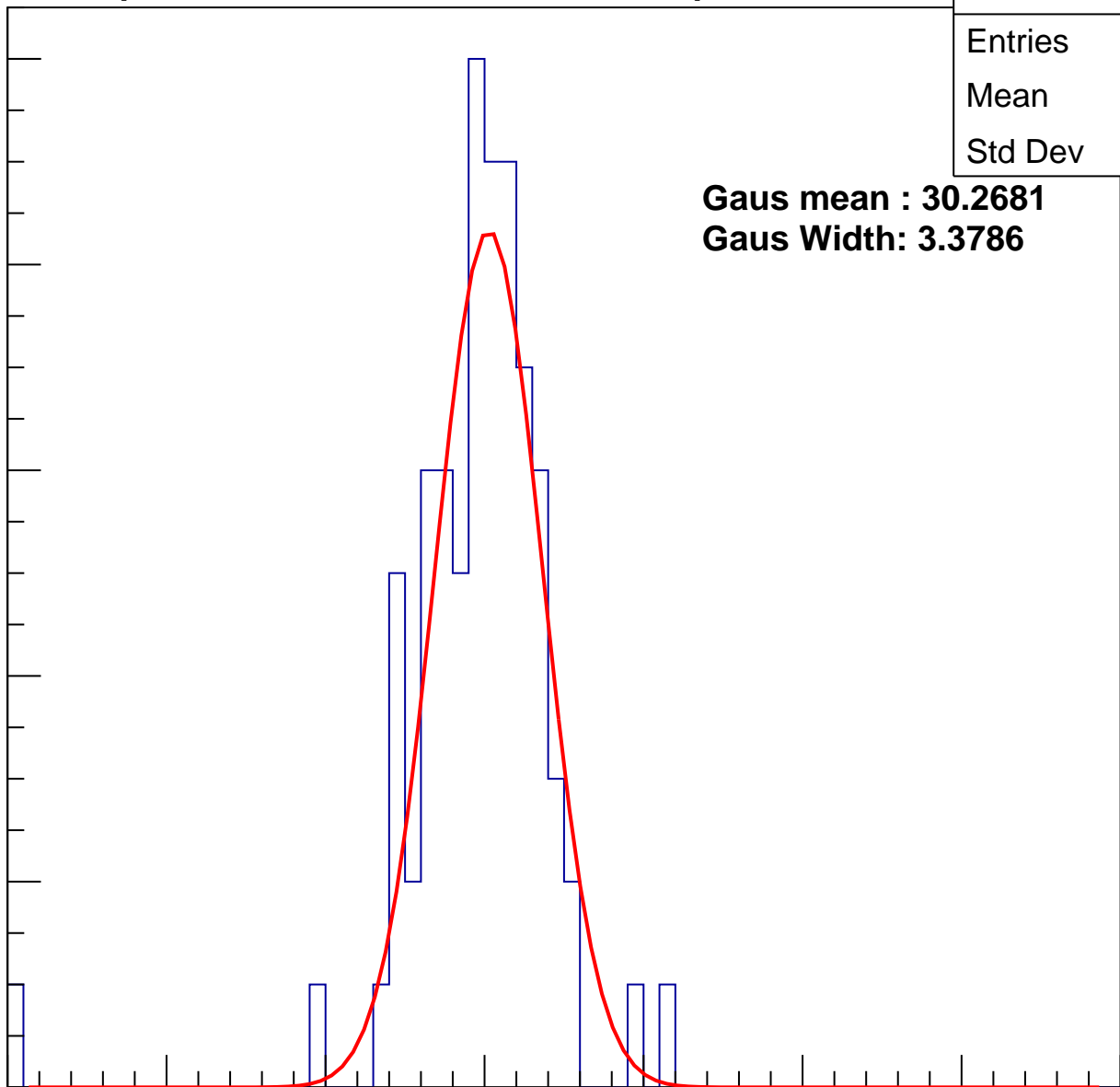
**Gaus Width: 3.3786**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U16-ch9, adc1

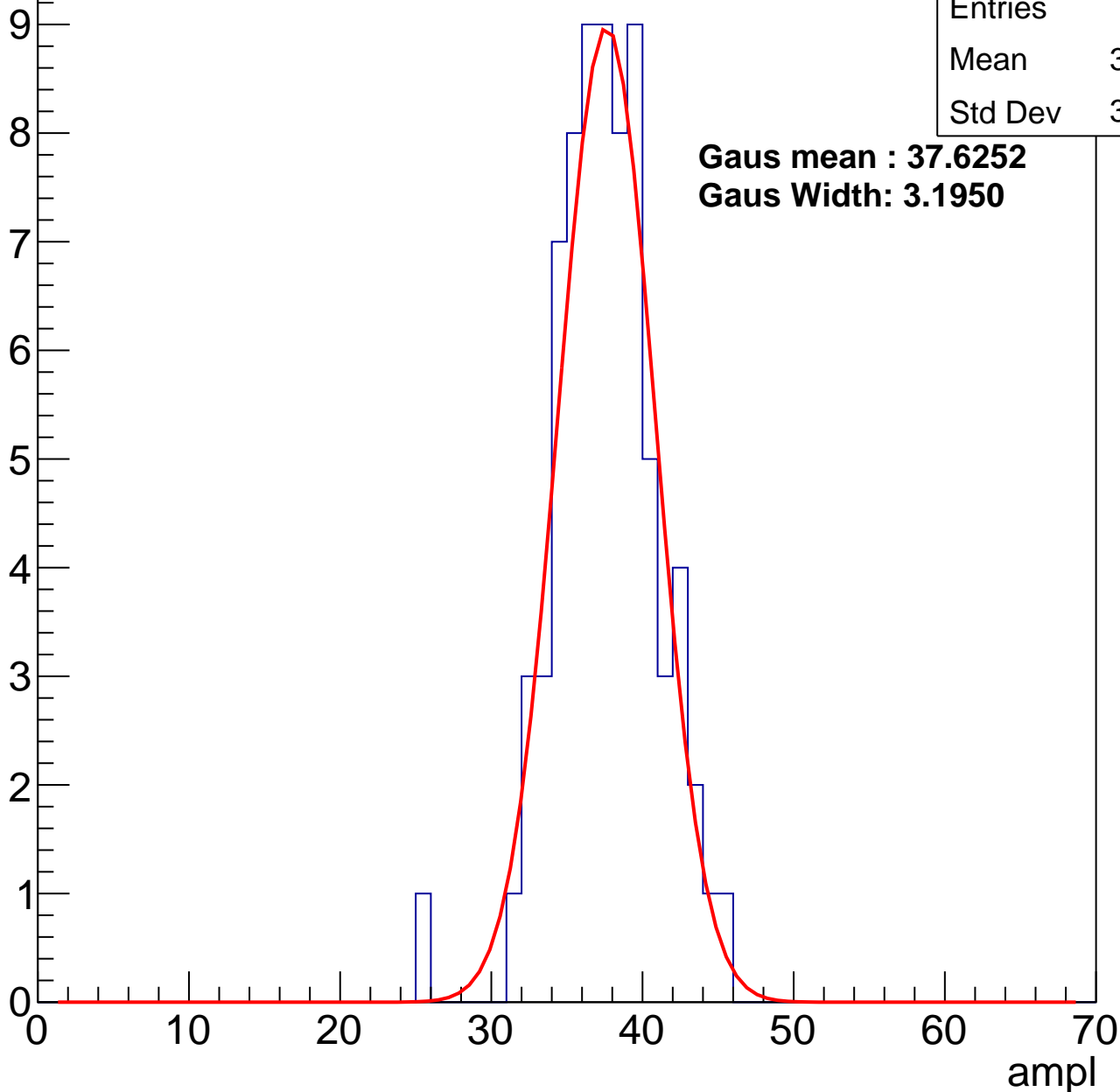
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	37.12
Std Dev	3.345

**Gaus mean : 37.6252**

**Gaus Width: 3.1950**



# B1L102S, U16-ch9, adc2

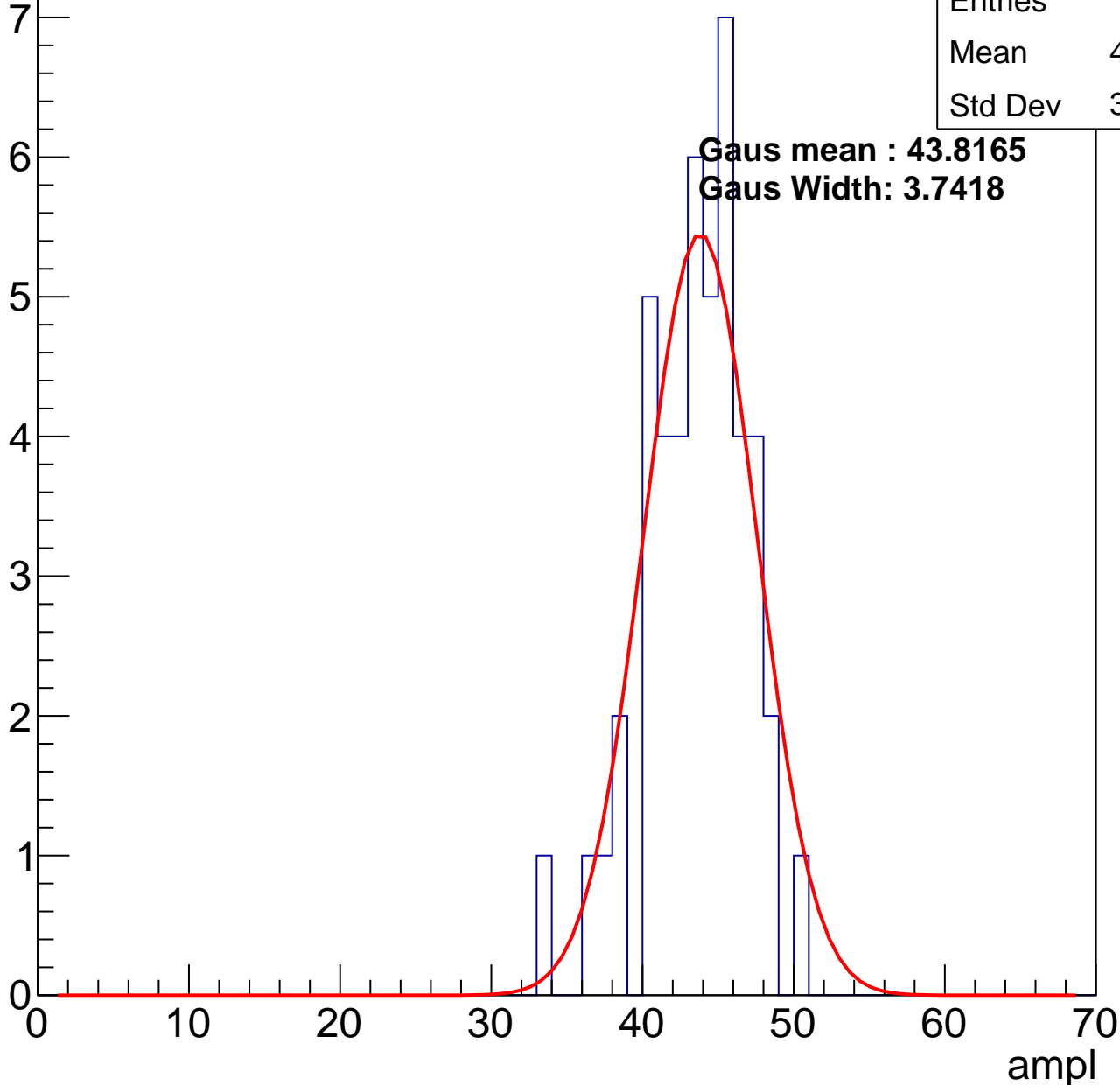
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	43.09
Std Dev	3.363

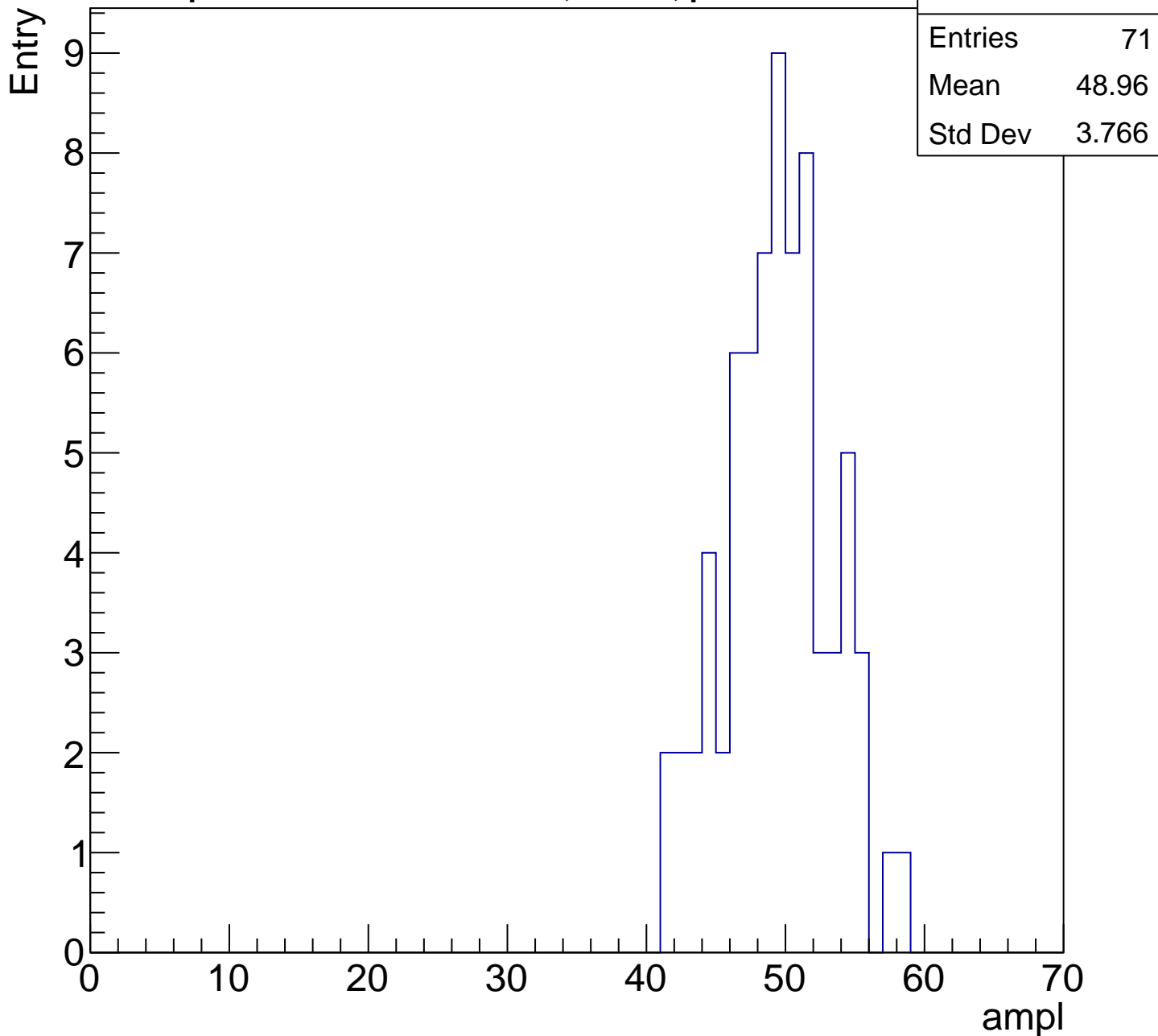
**Gaus mean : 43.8165**

**Gaus Width: 3.7418**



# B1L102S, U16-ch9, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

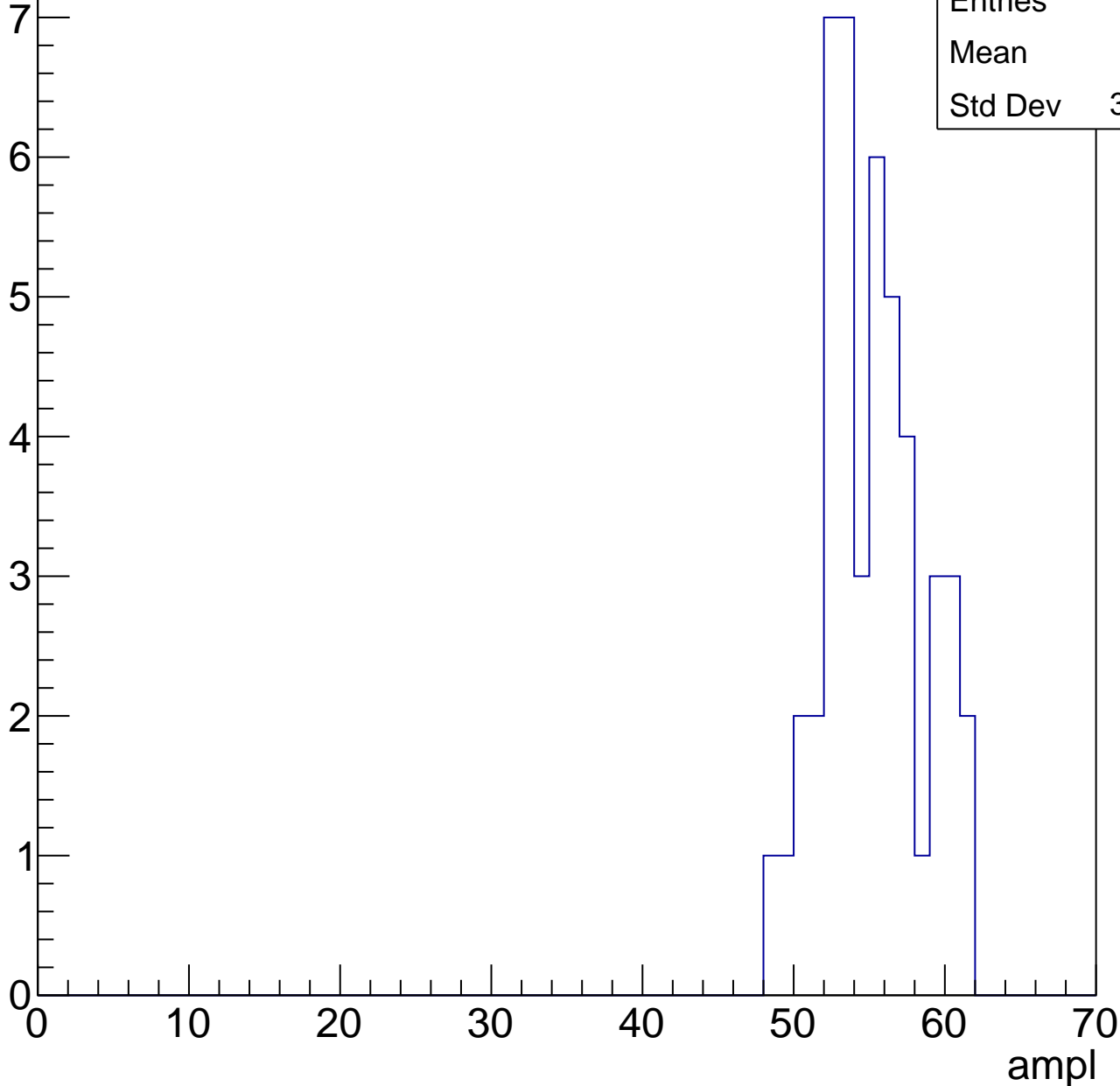


# B1L102S, U16-ch9, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	54.7
Std Dev	3.202

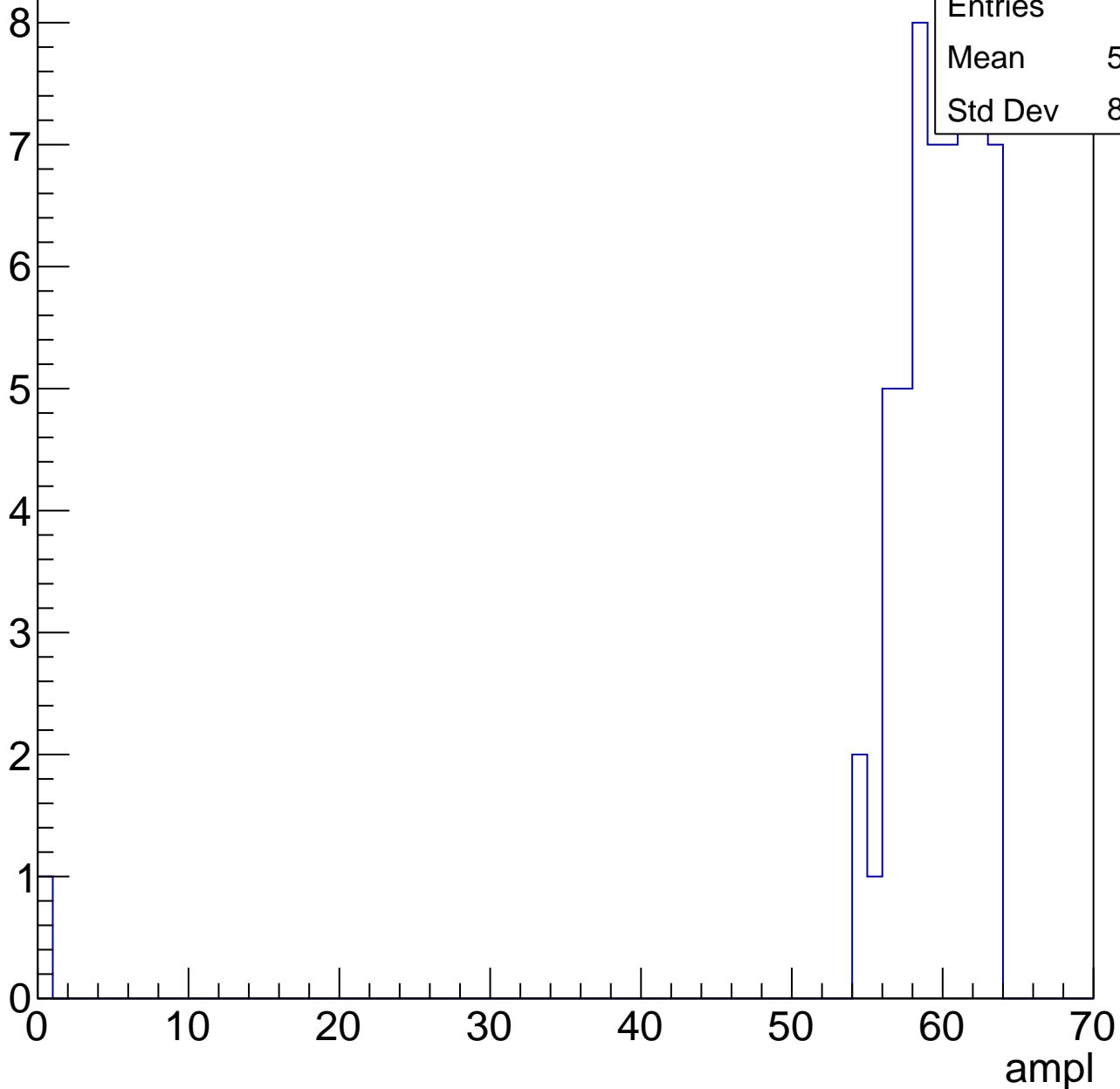


# B1L102S, U16-ch9, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	58.47
Std Dev	8.054



# B1L102S, U16-ch9, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch9, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U16-ch10, adc0

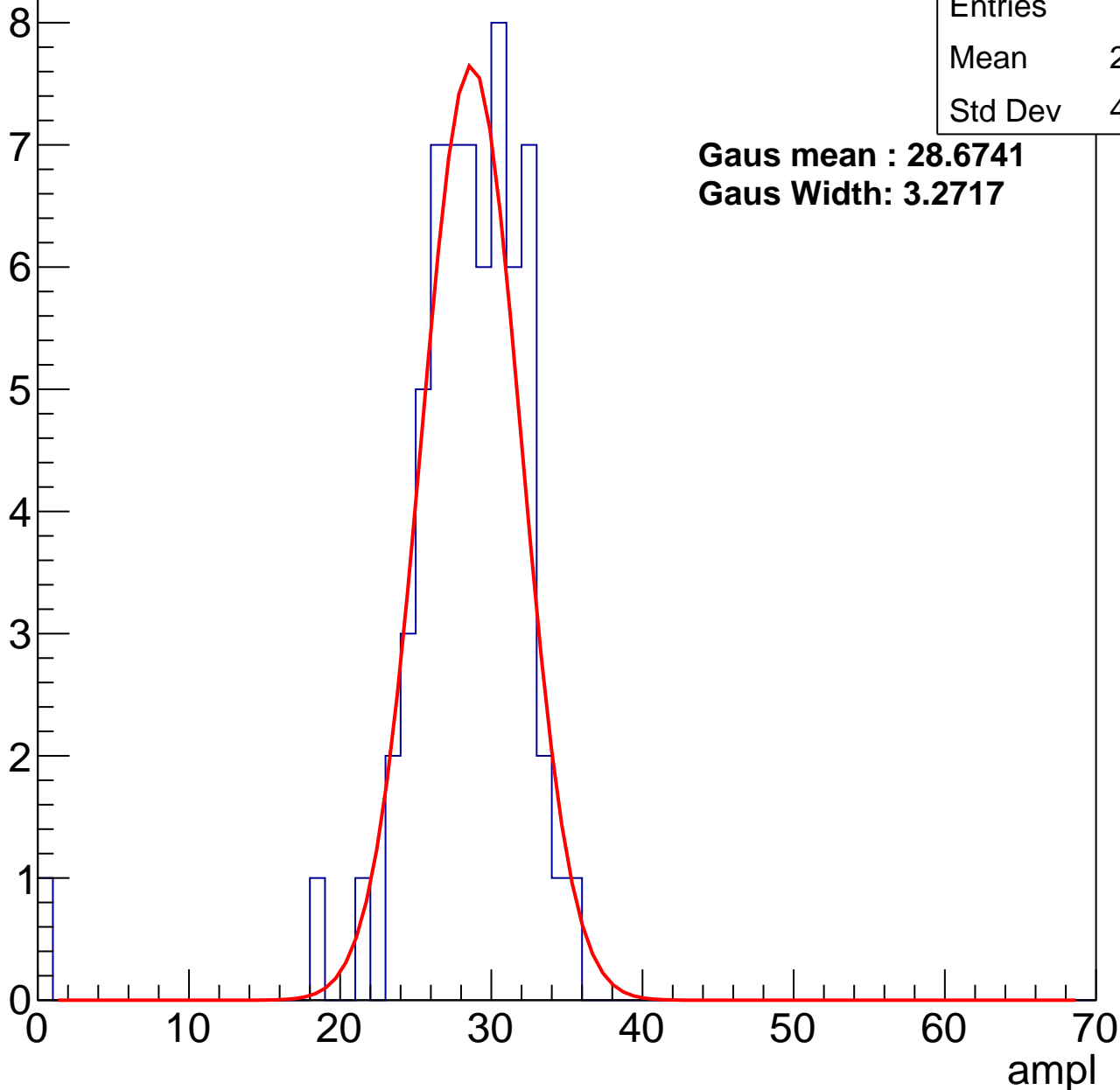
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	27.82
Std Dev	4.719

**Gaus mean : 28.6741**

**Gaus Width: 3.2717**



# B1L102S, U16-ch10, adc1

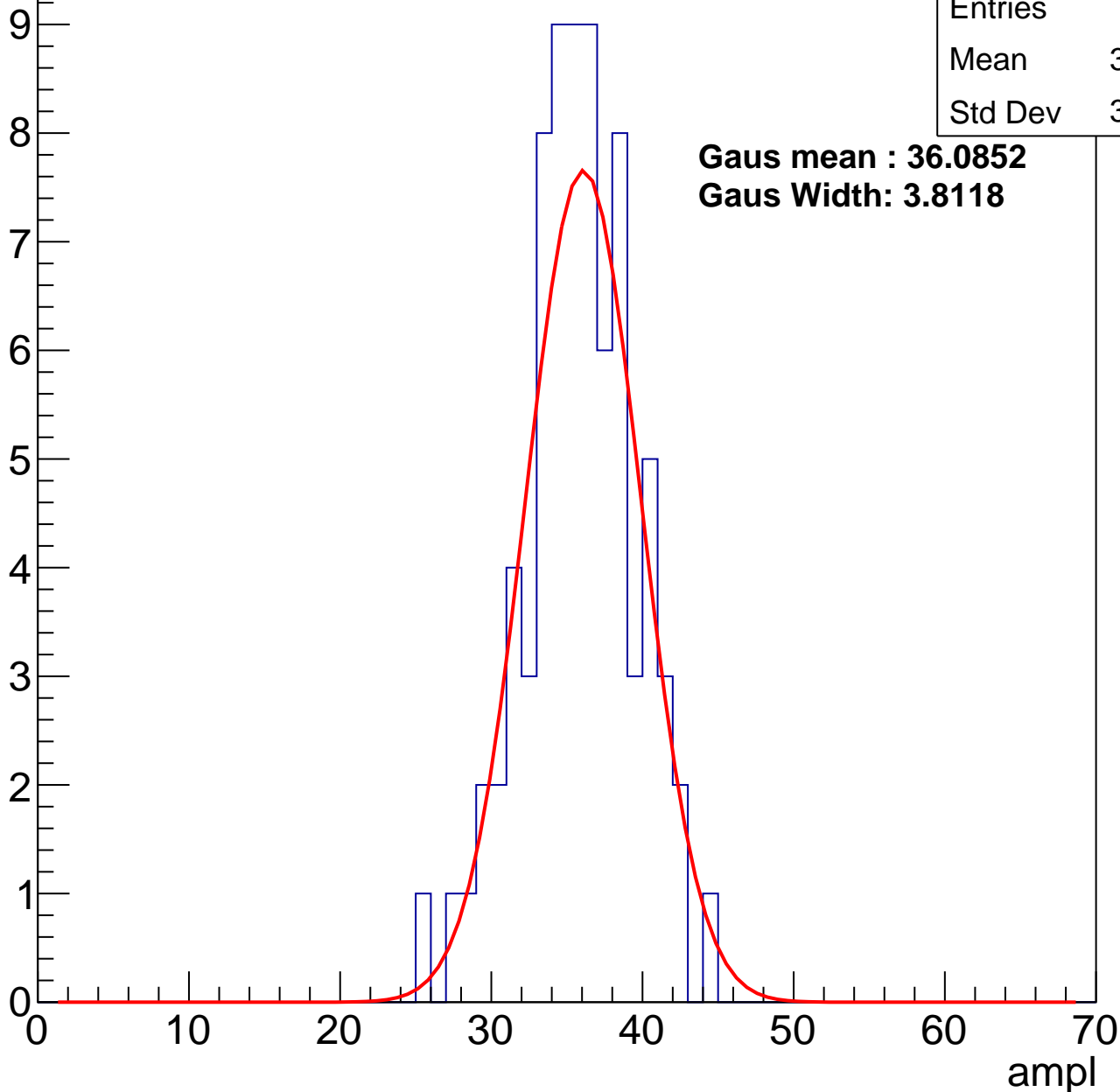
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	35.34
Std Dev	3.645

**Gaus mean : 36.0852**

**Gaus Width: 3.8118**



# B1L102S, U16-ch10, adc2

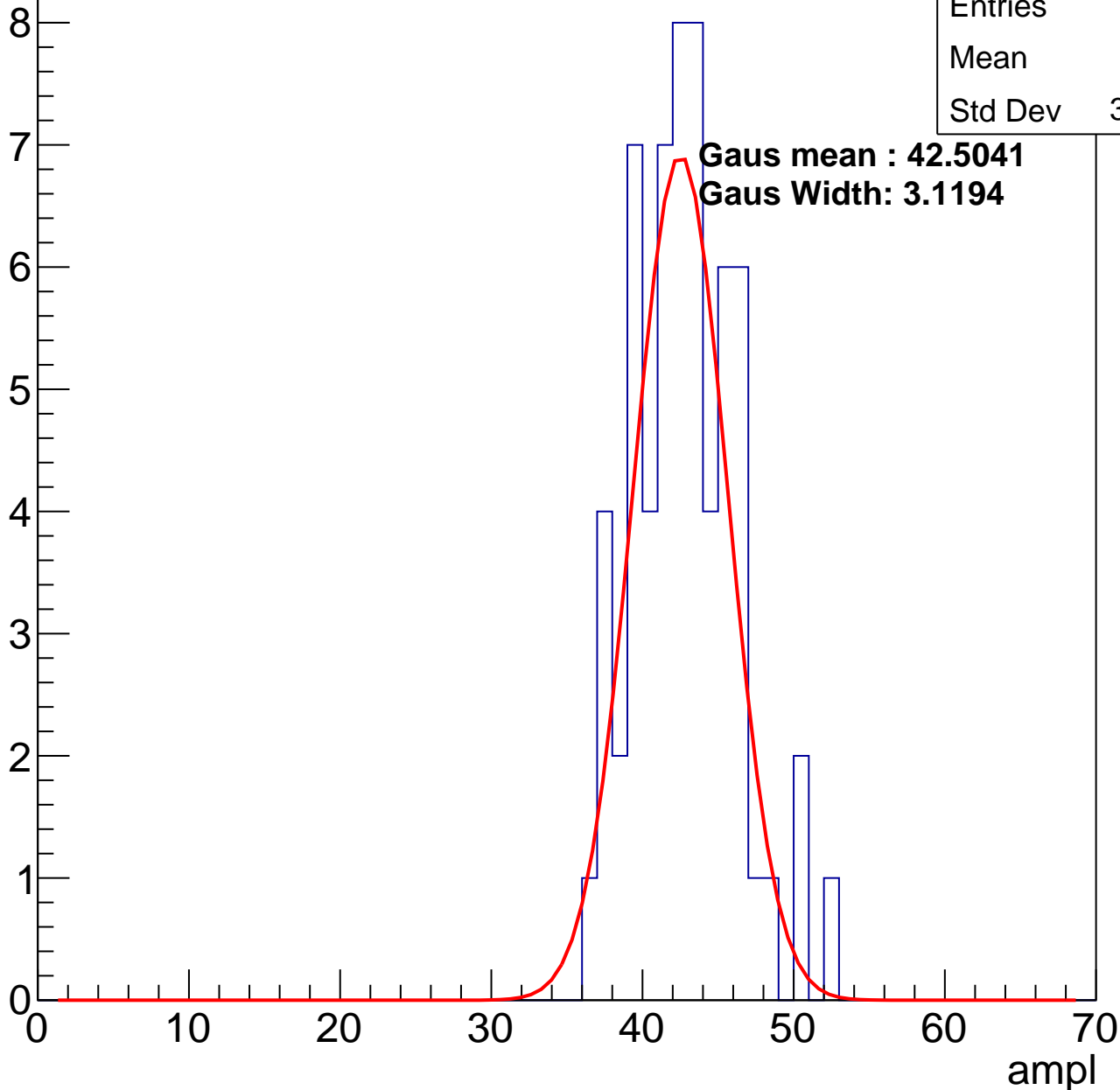
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	42.4
Std Dev	3.377

**Gaus mean : 42.5041**

**Gaus Width: 3.1194**

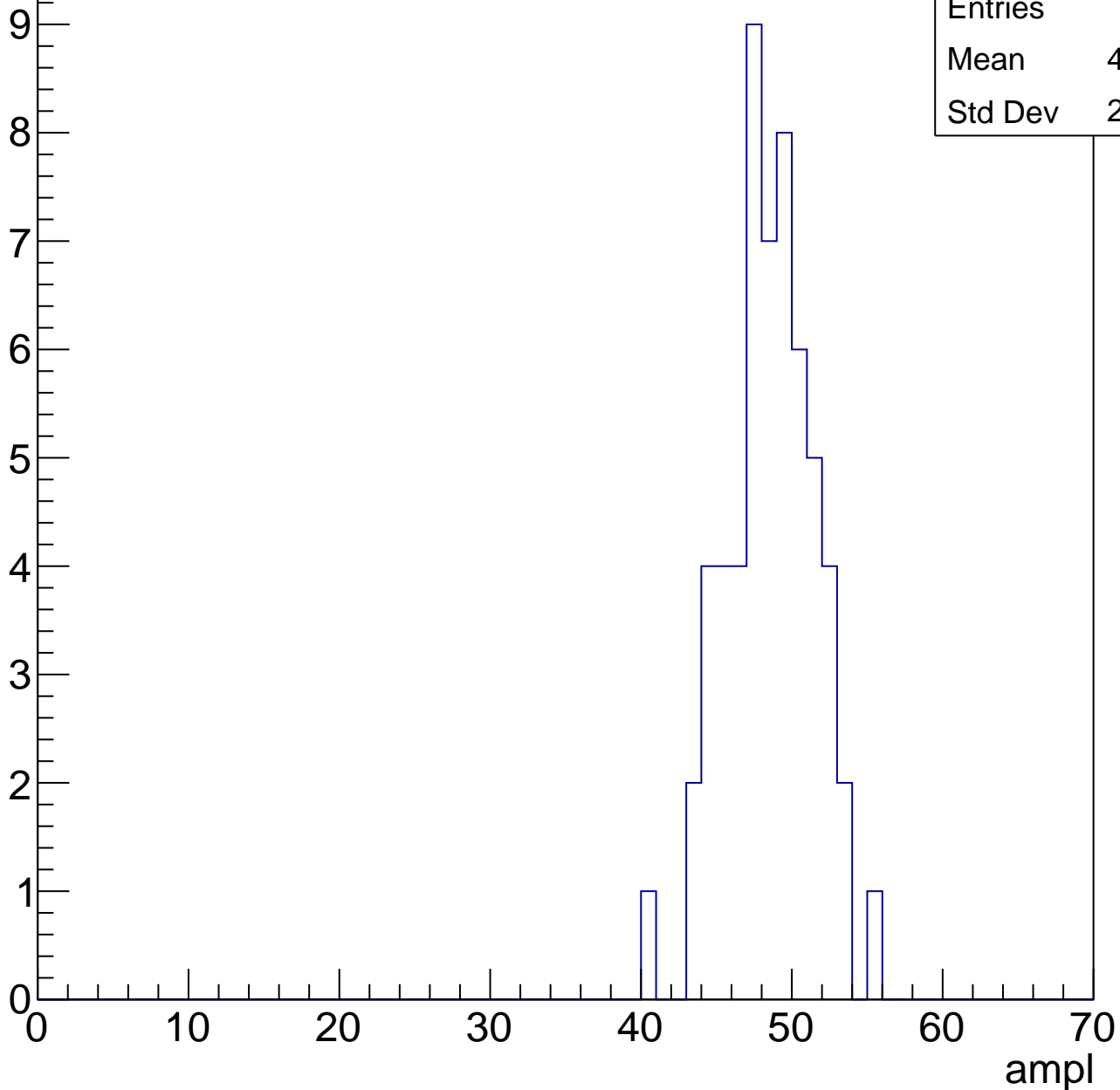


# B1L102S, U16-ch10, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	48.09
Std Dev	2.898

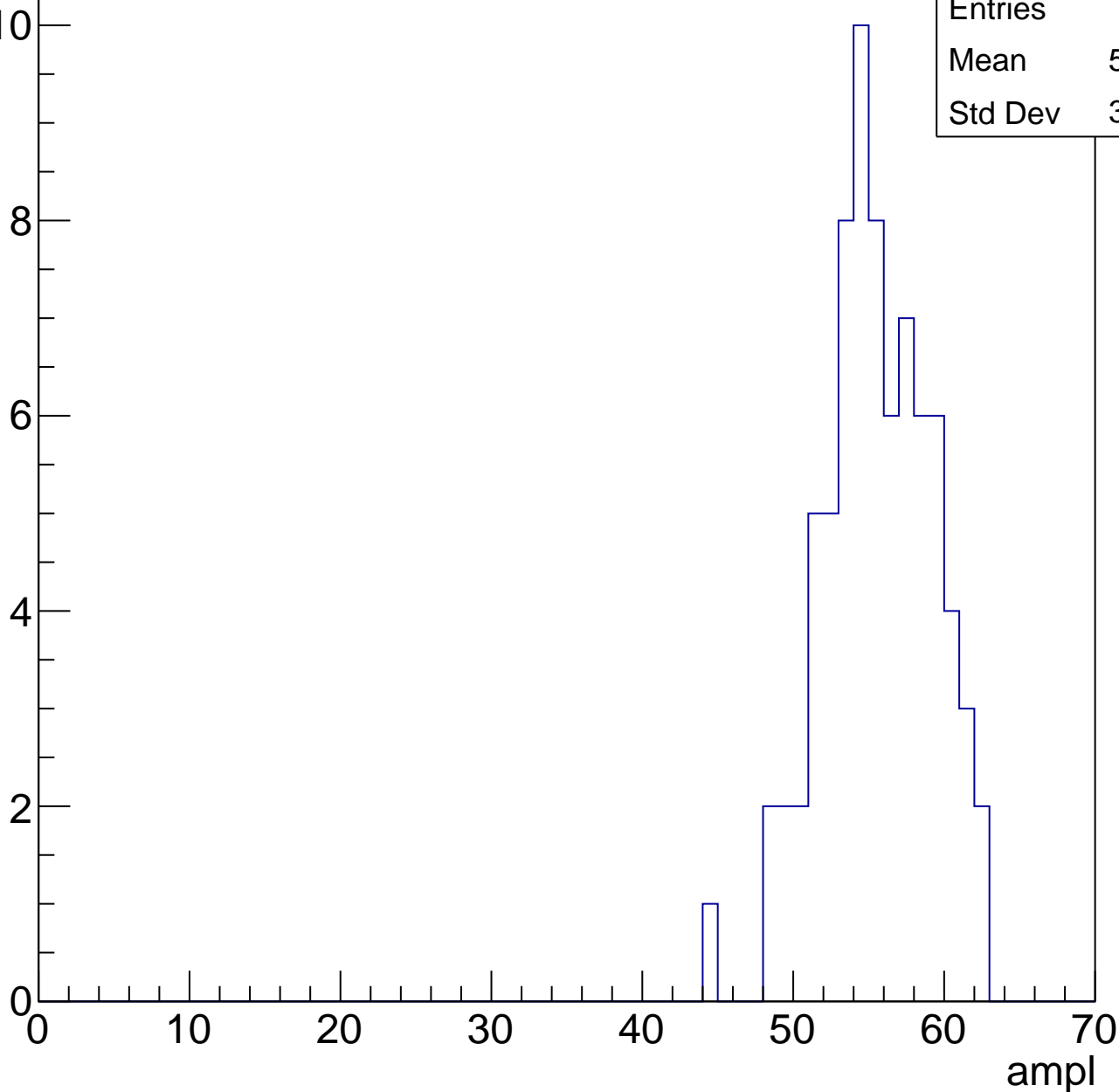


# B1L102S, U16-ch10, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	55.08
Std Dev	3.599

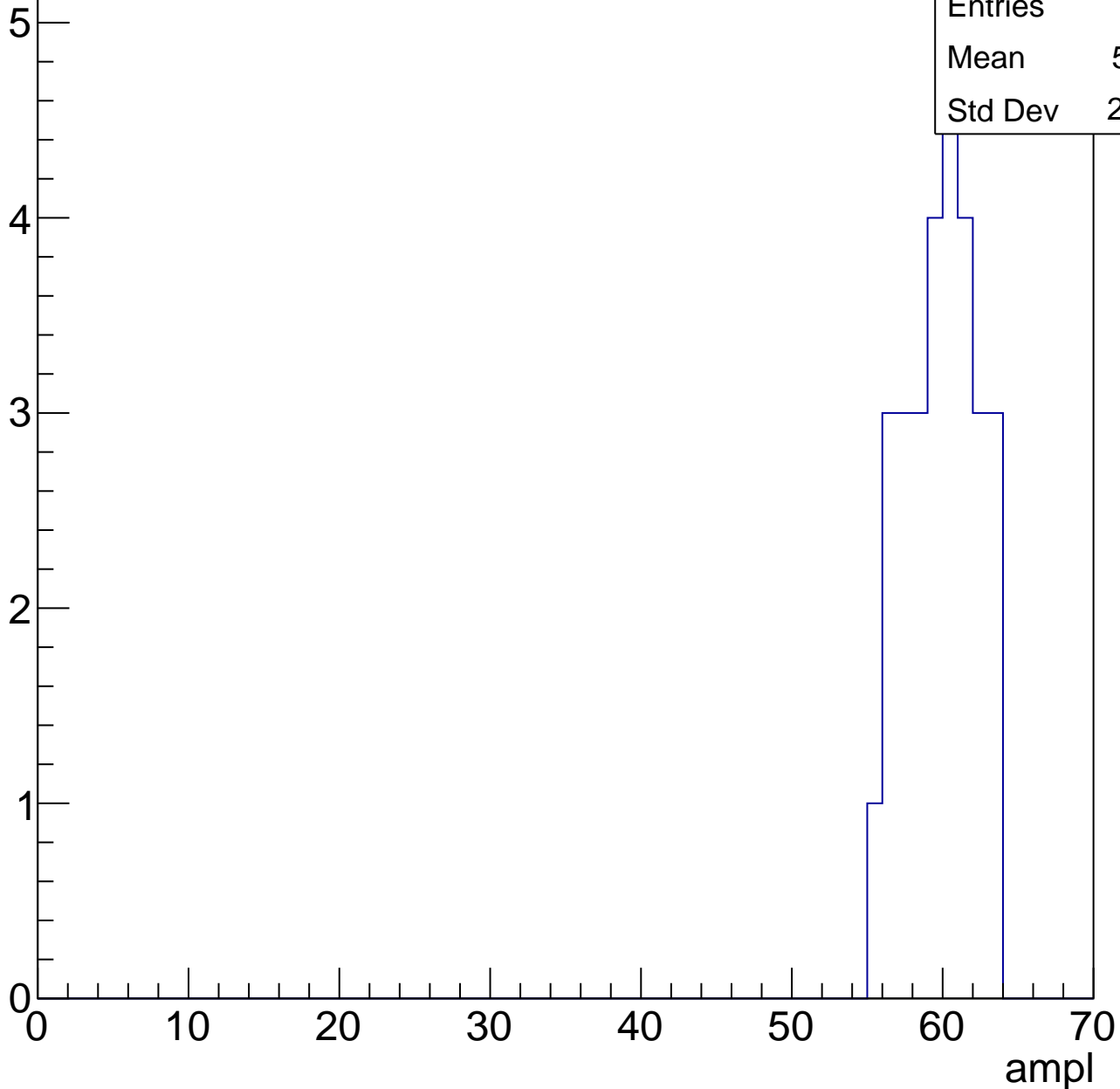


# B1L102S, U16-ch10, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	29
Mean	59.41
Std Dev	2.267

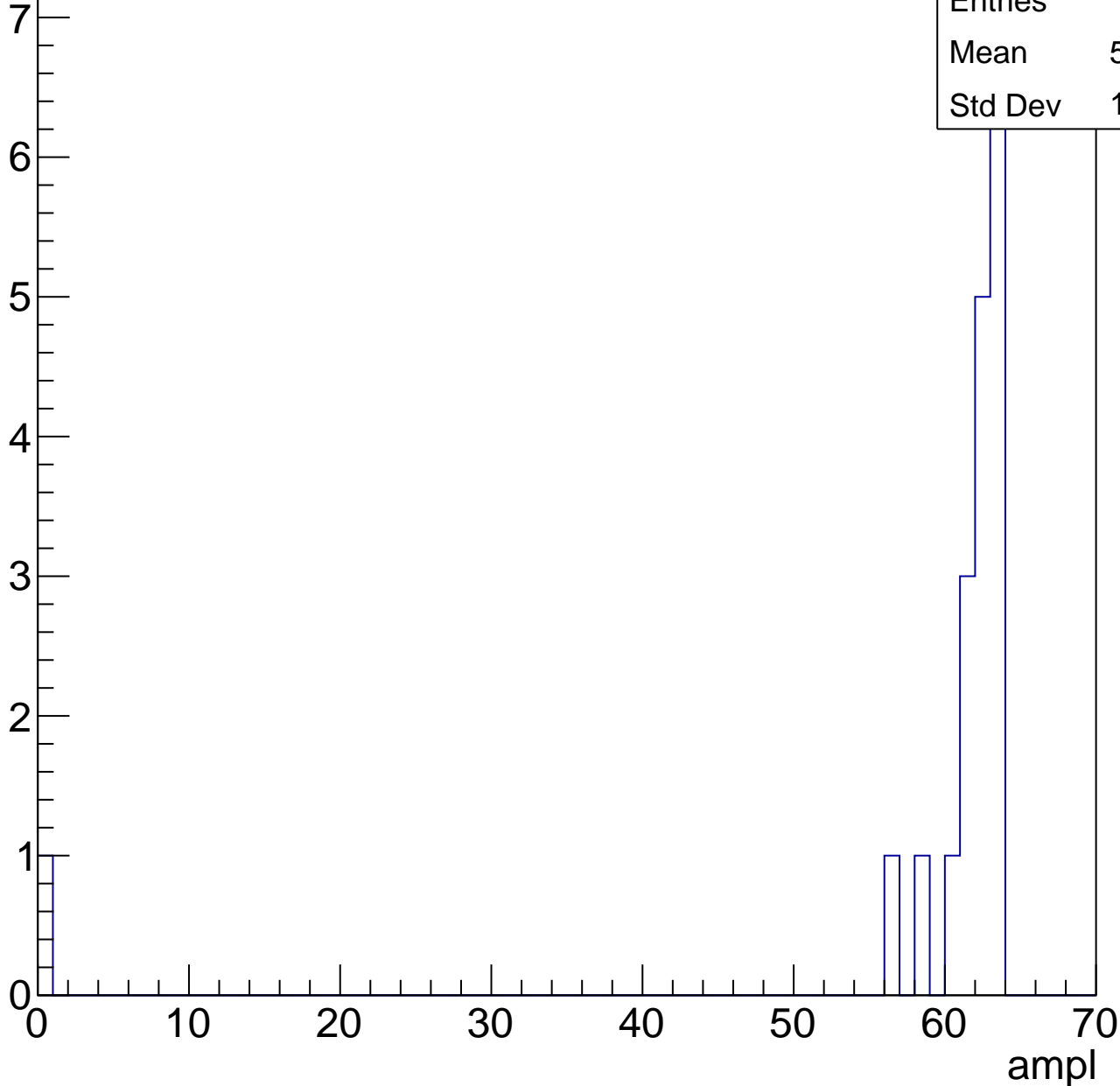


# B1L102S, U16-ch10, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	19
Mean	58.32
Std Dev	13.86





# B1L102S, U16-ch10, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	6
Std Dev	8.485

# B1L102S, U16-ch11, adc0

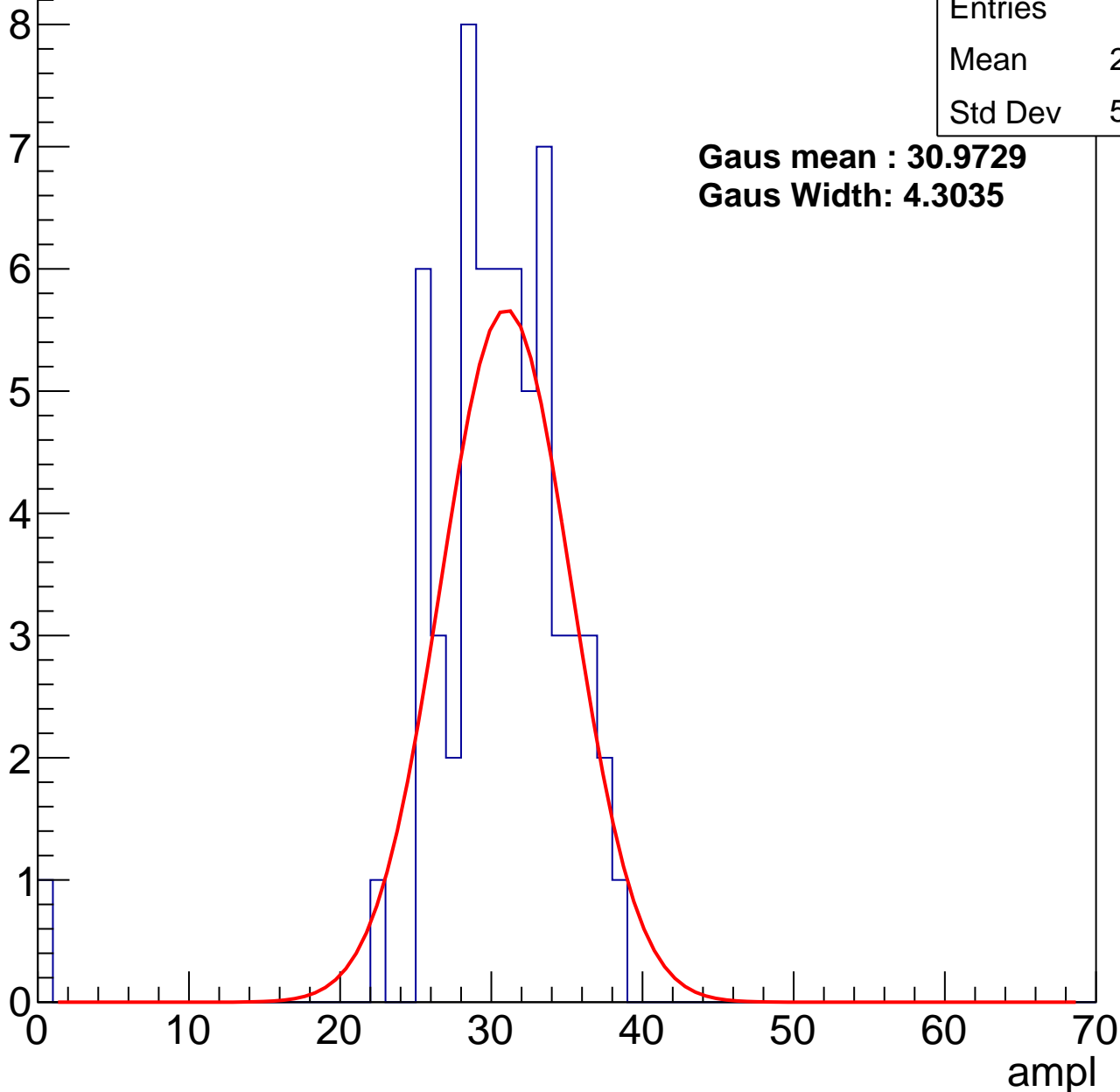
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	29.94
Std Dev	5.194

**Gaus mean : 30.9729**

**Gaus Width: 4.3035**



# B1L102S, U16-ch11, adc1

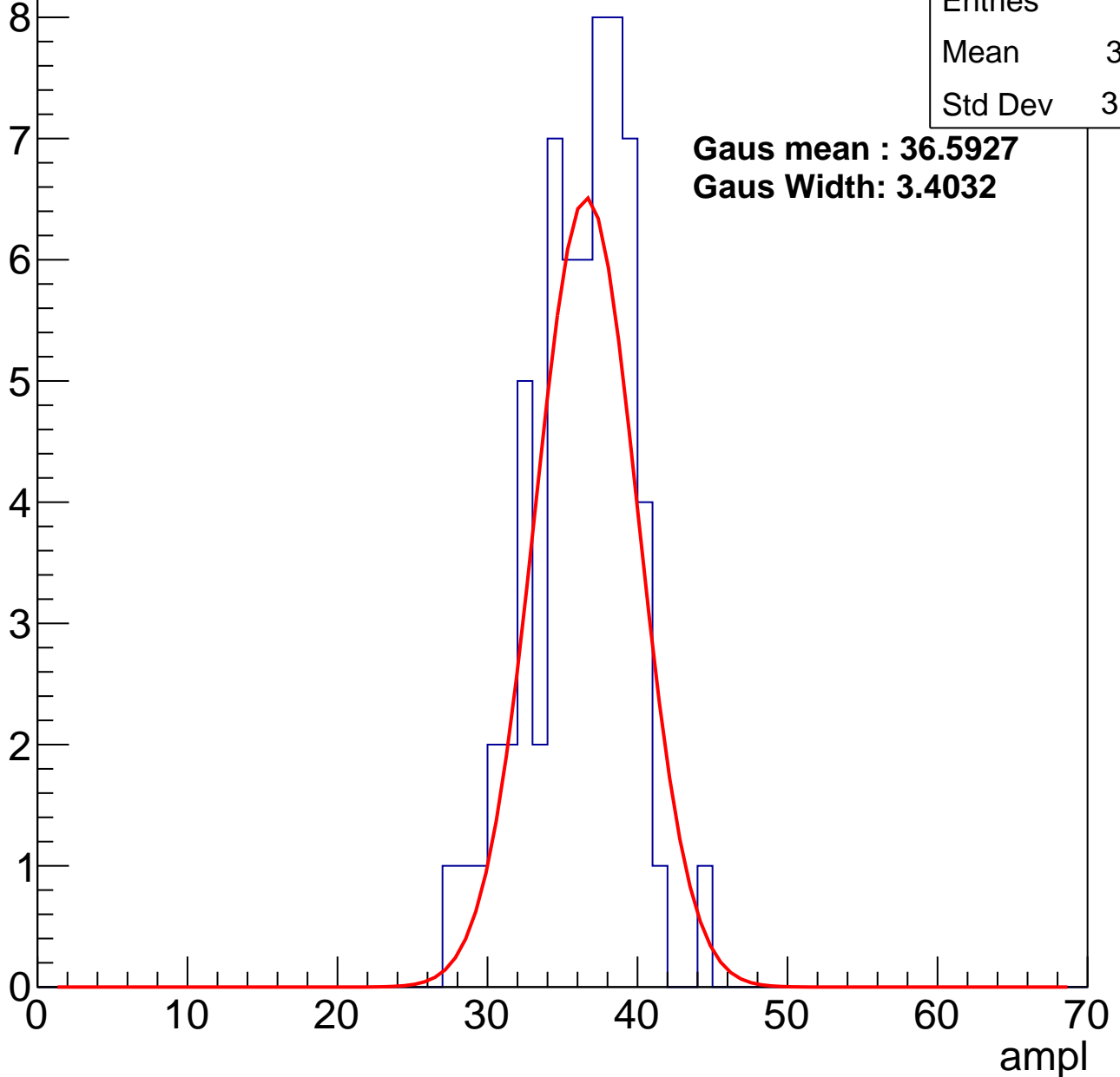
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	35.71
Std Dev	3.357

**Gaus mean : 36.5927**

**Gaus Width: 3.4032**



# B1L102S, U16-ch11, adc2

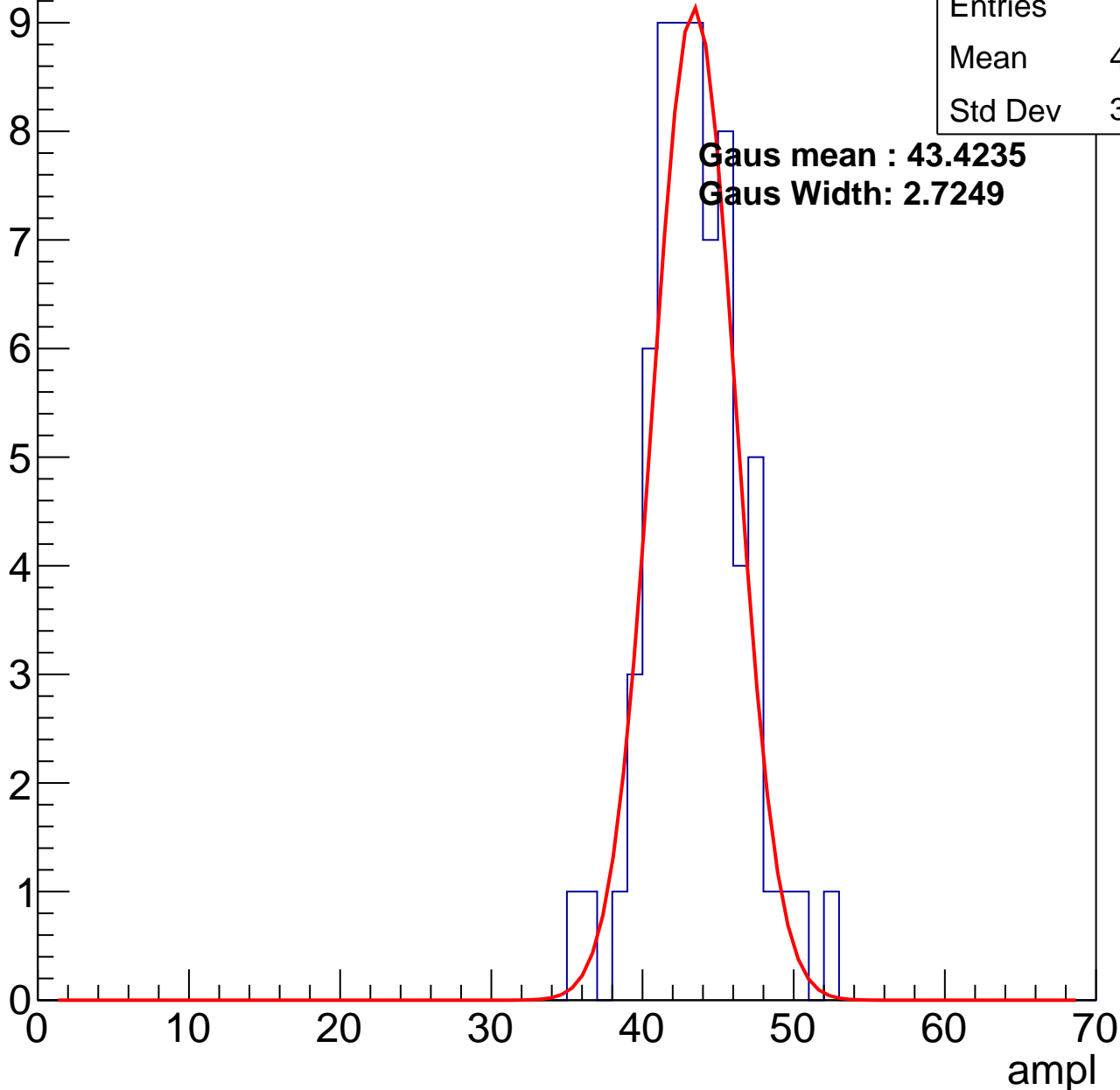
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	43.07
Std Dev	3.068

**Gaus mean : 43.4235**

**Gaus Width: 2.7249**

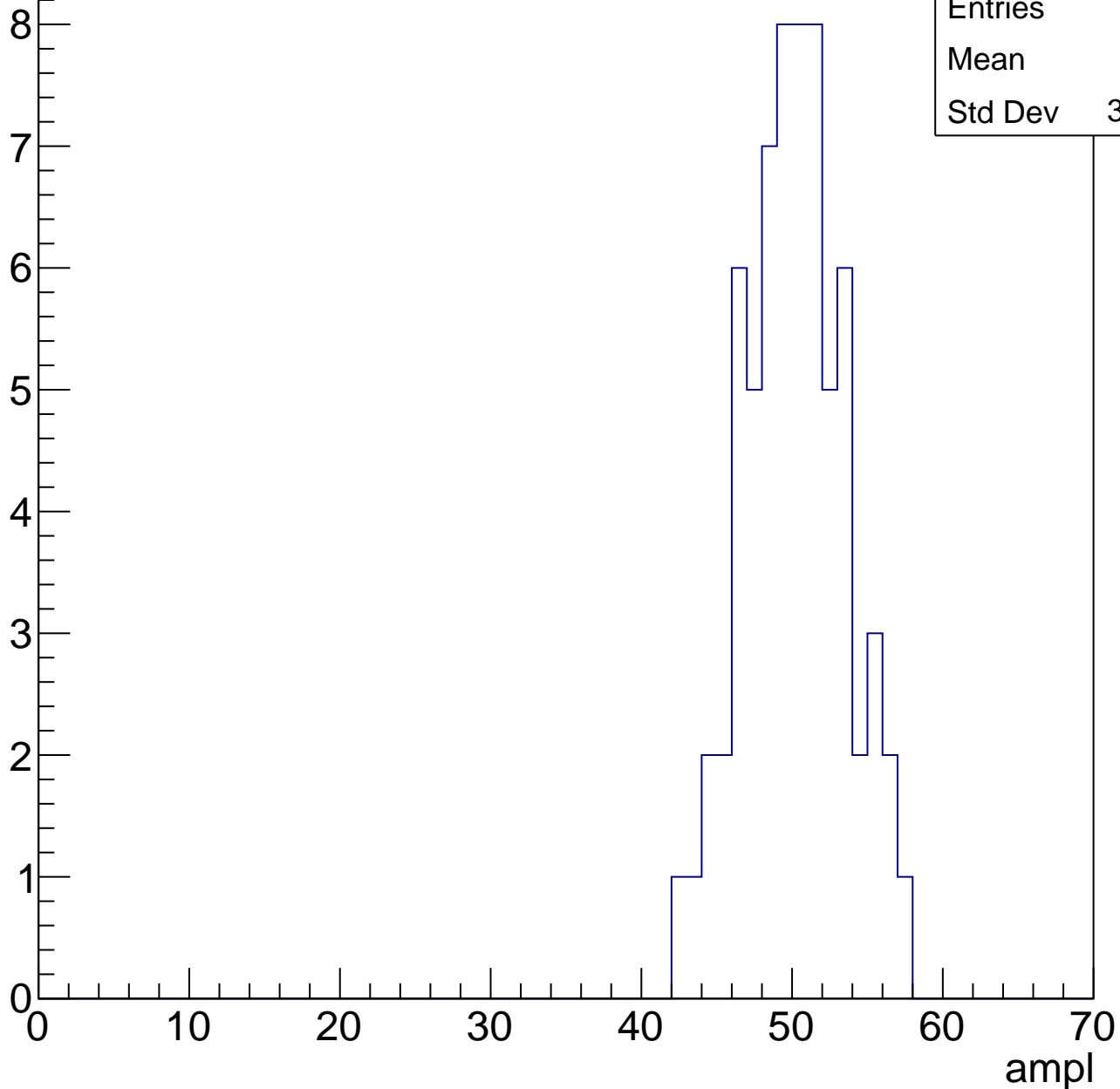


# B1L102S, U16-ch11, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

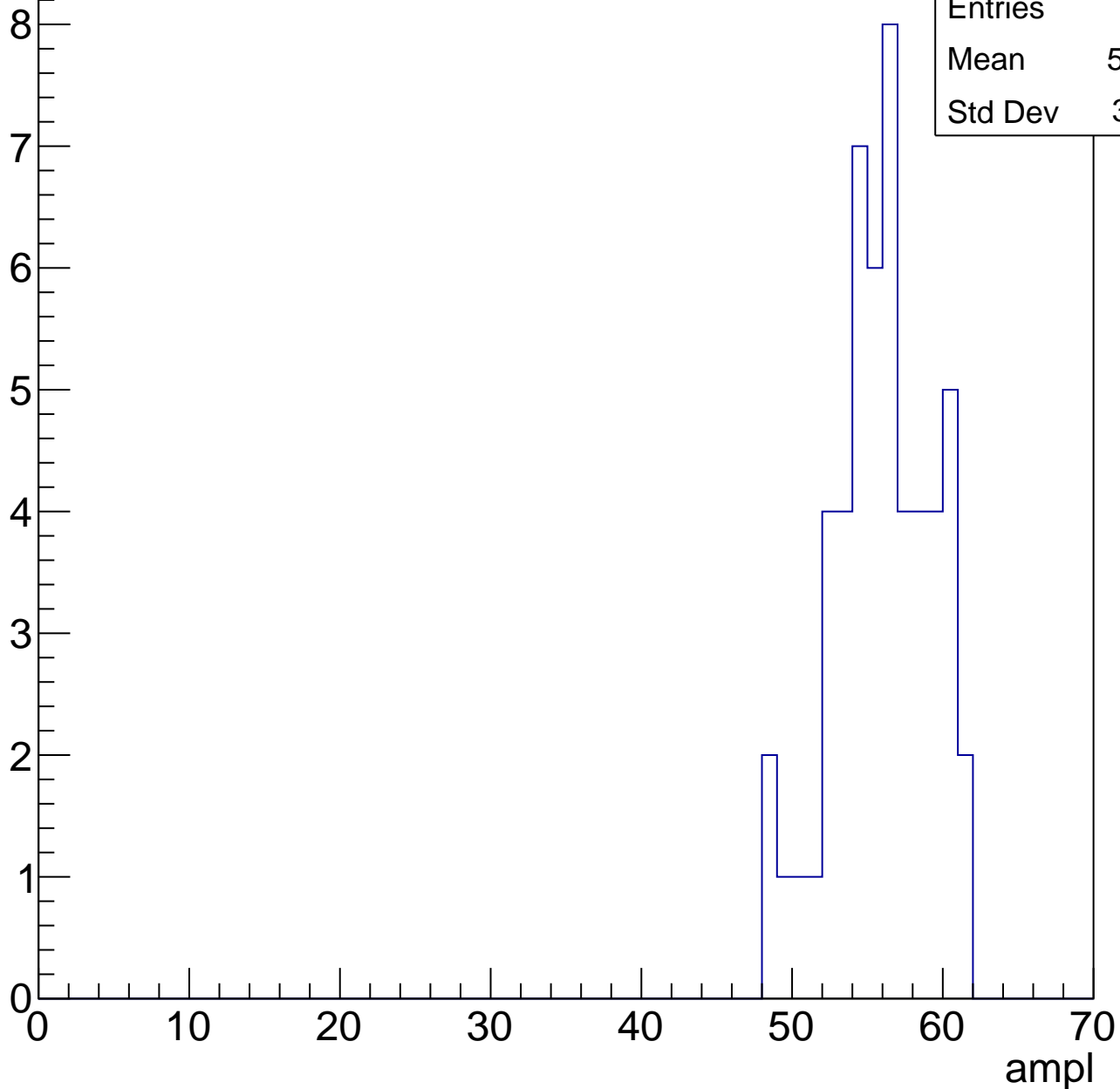
Entries	67
Mean	49.7
Std Dev	3.269



# B1L102S, U16-ch11, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



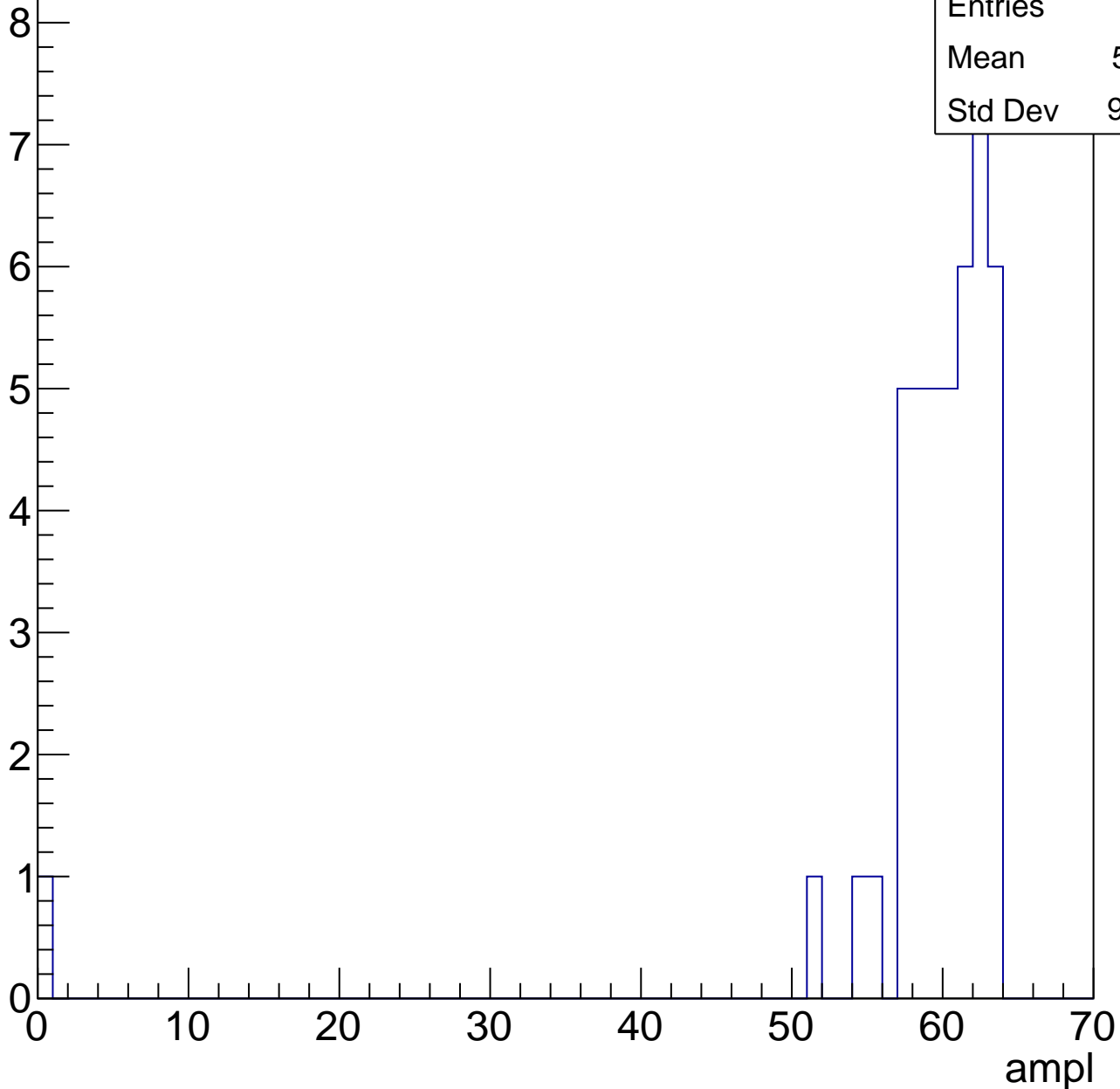
Entries	53
Mean	55.47
Std Dev	3.201

# B1L102S, U16-ch11, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

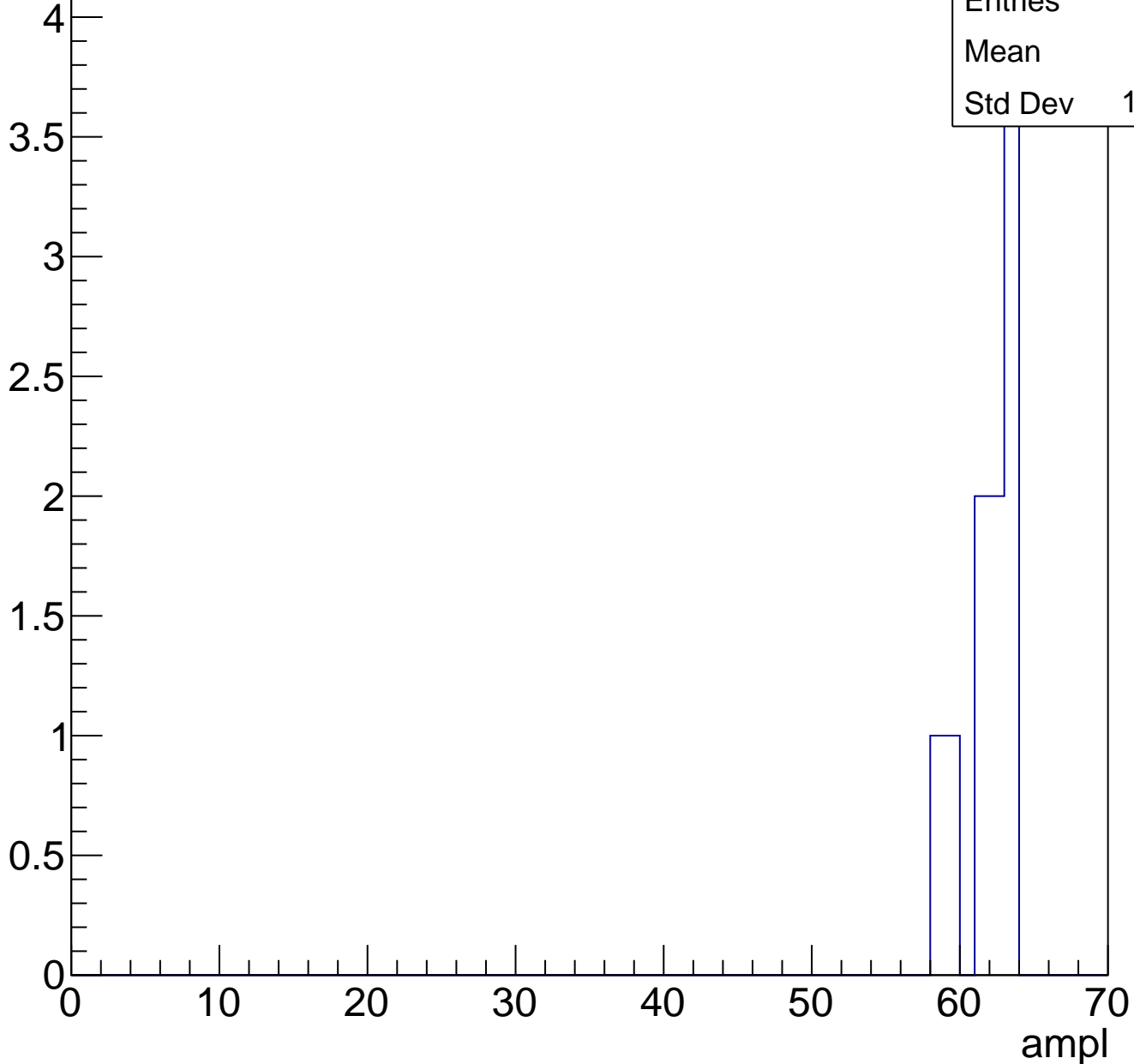
Entries	44
Mean	58.41
Std Dev	9.284



# B1L102S, U16-ch11, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

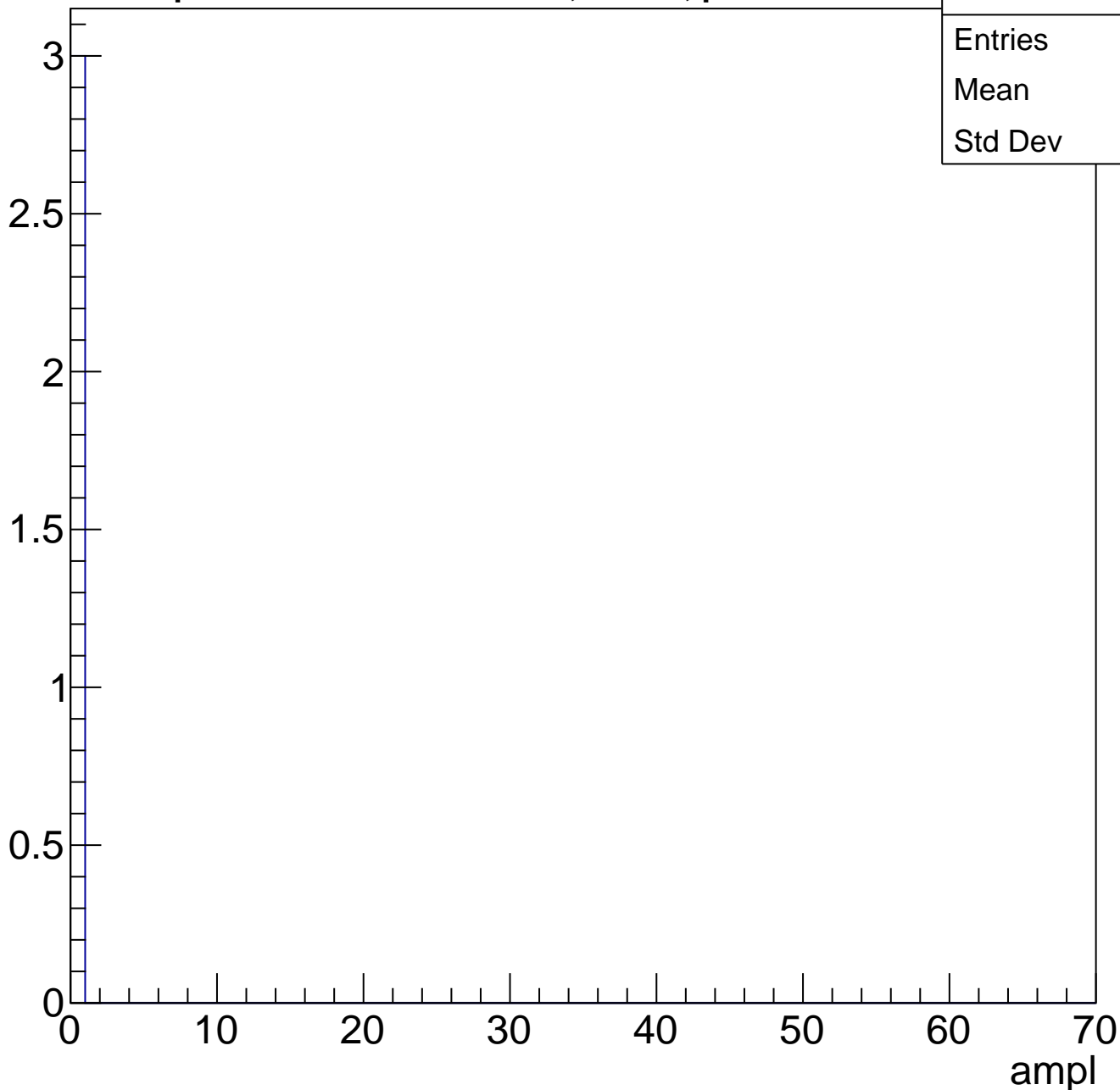




# B1L102S, U16-ch11, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L102S, U16-ch12, adc0

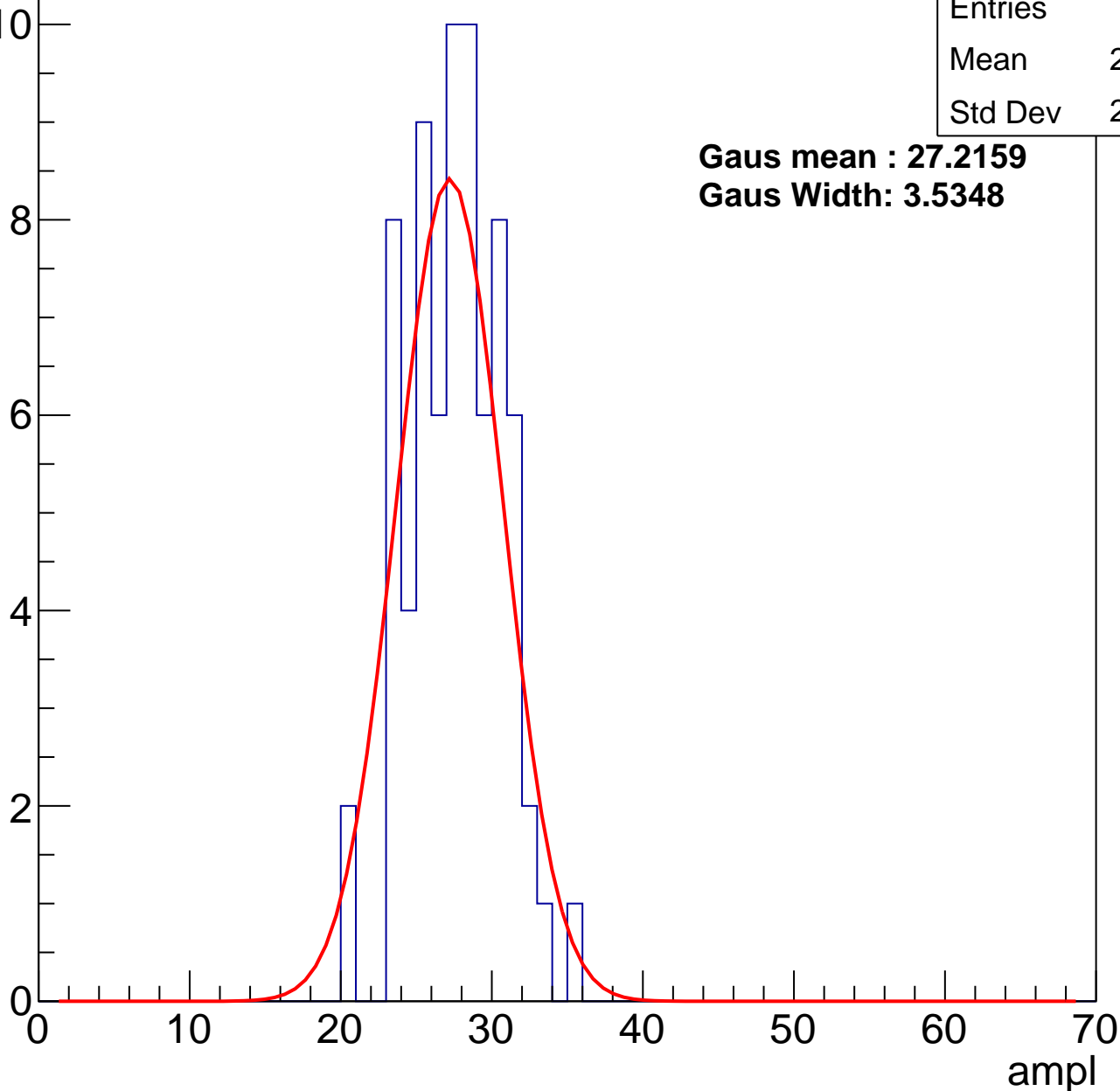
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	27.16
Std Dev	2.993

**Gaus mean : 27.2159**

**Gaus Width: 3.5348**



# B1L102S, U16-ch12, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	75
Mean	34.97
Std Dev	3.402

**Gaus mean : 35.3707**

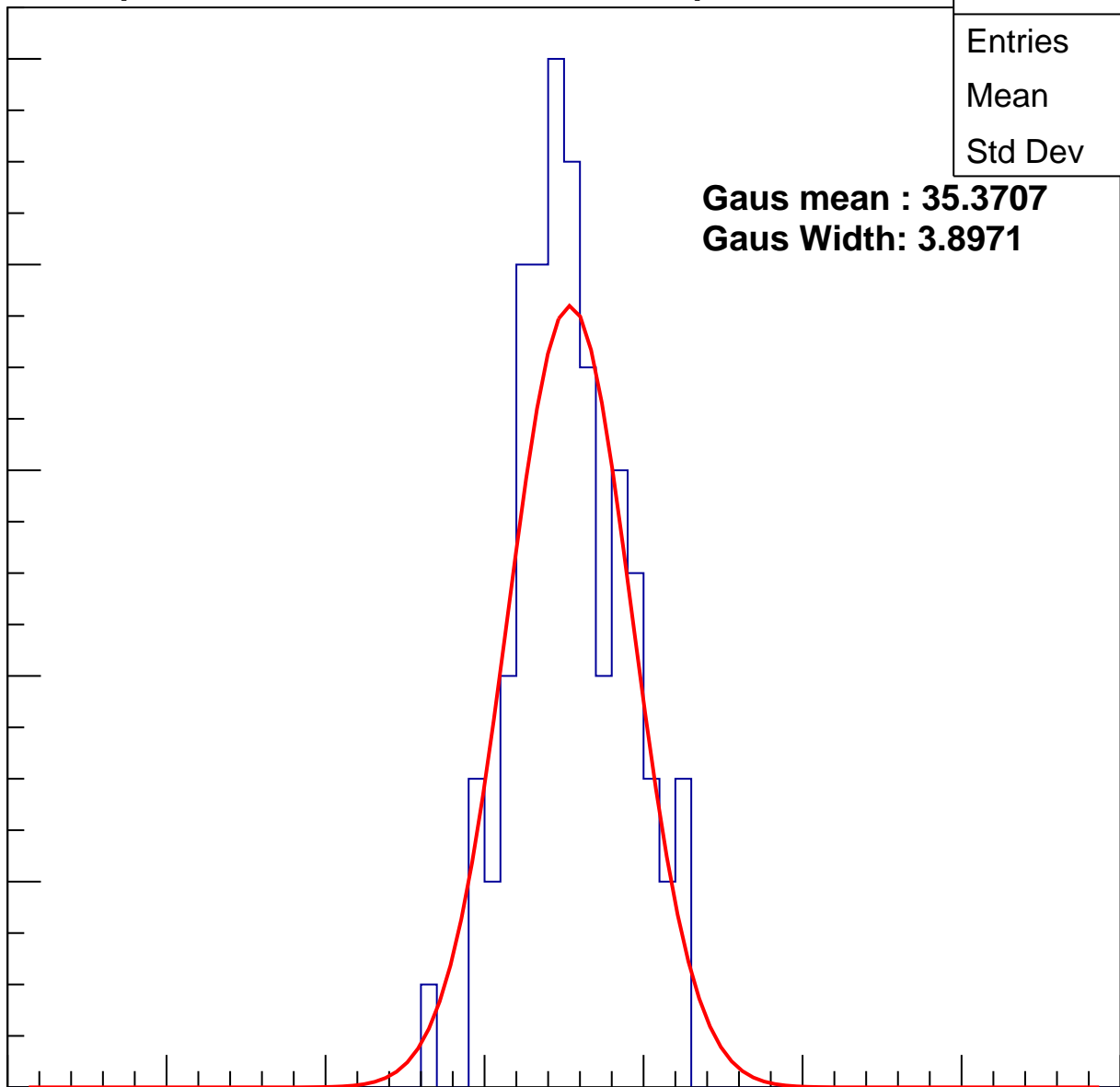
**Gaus Width: 3.8971**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U16-ch12, adc2

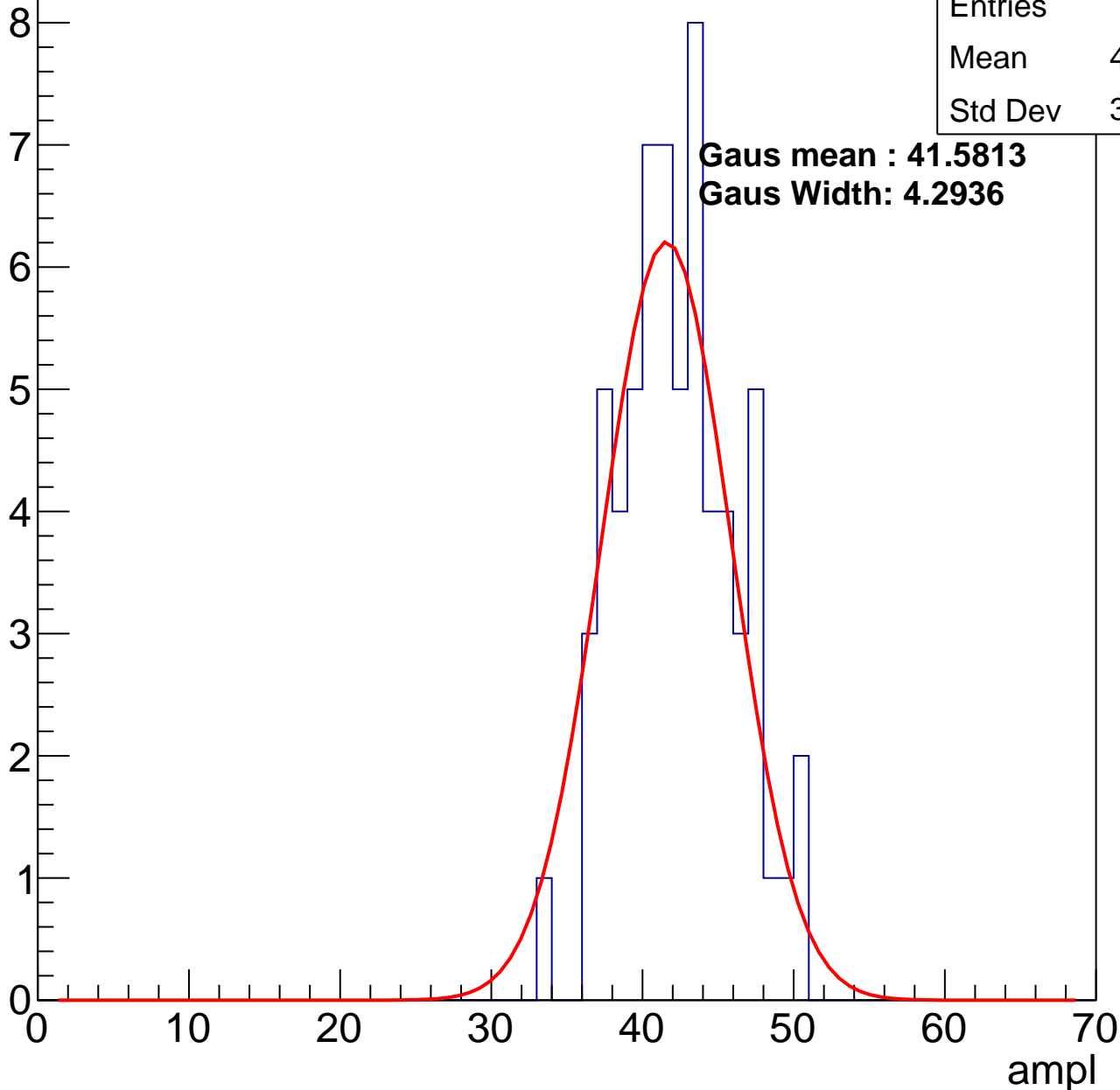
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	41.85
Std Dev	3.726

**Gaus mean : 41.5813**

**Gaus Width: 4.2936**

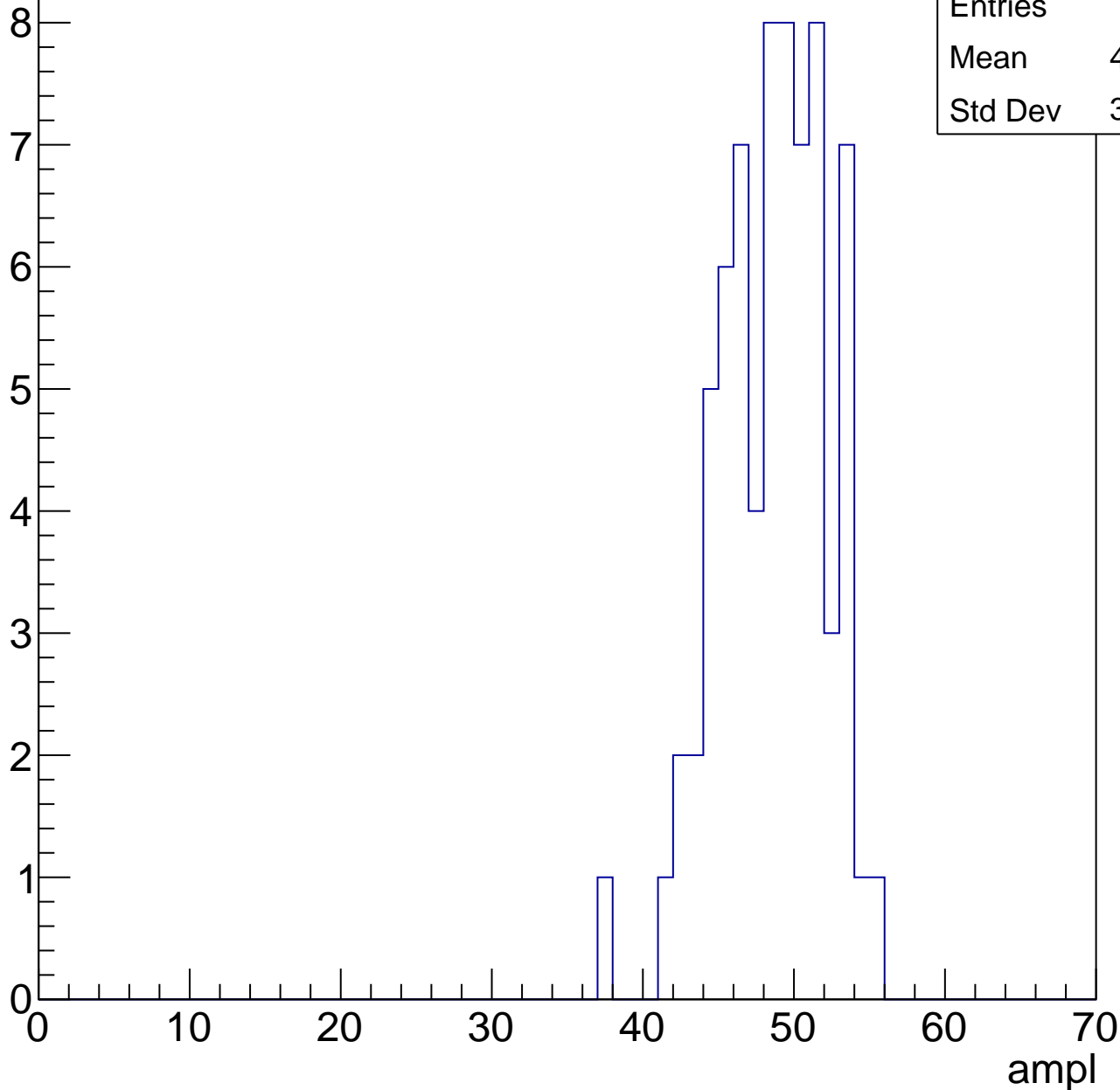


# B1L102S, U16-ch12, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	48.14
Std Dev	3.506

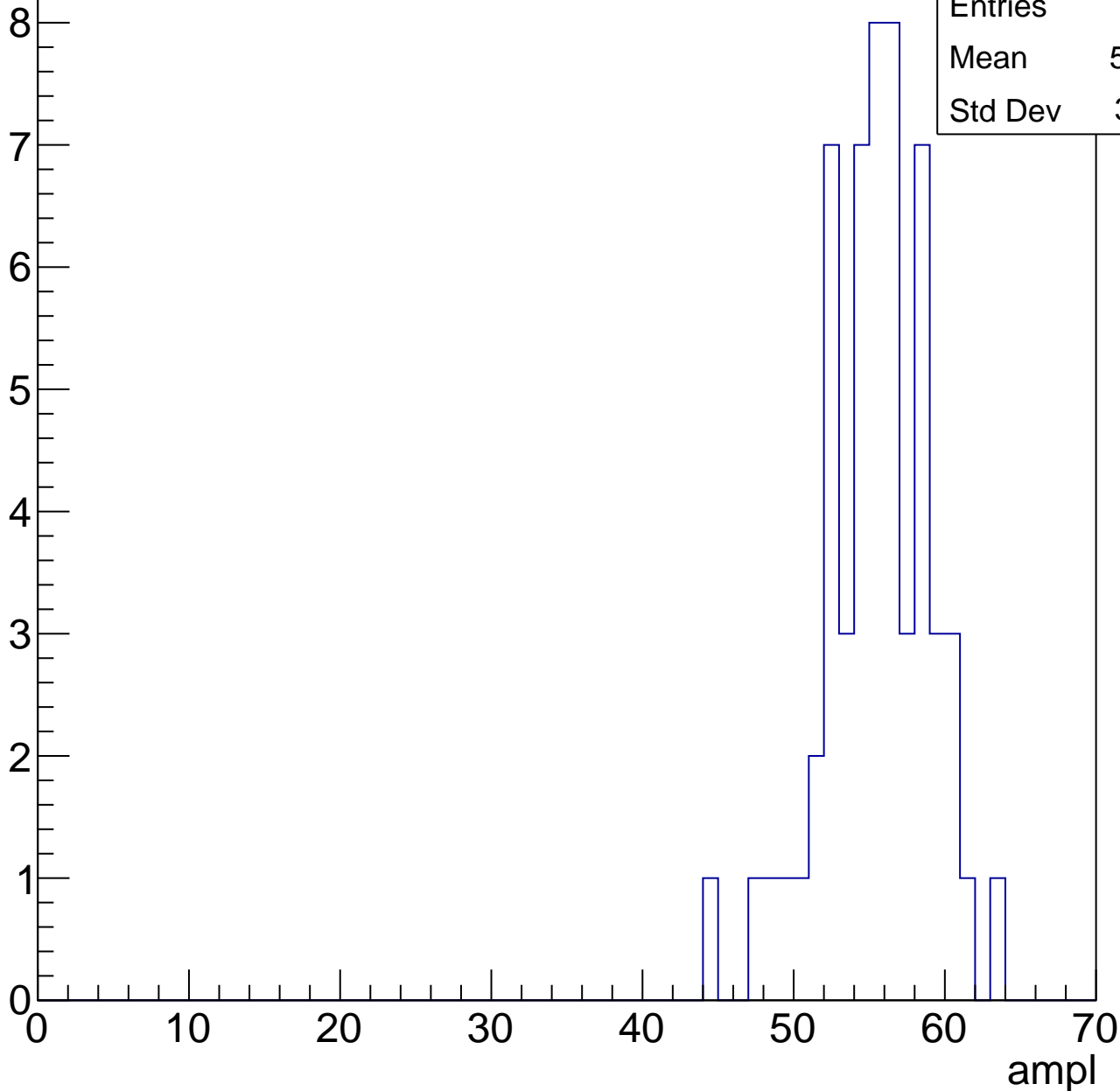


# B1L102S, U16-ch12, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	54.95
Std Dev	3.511

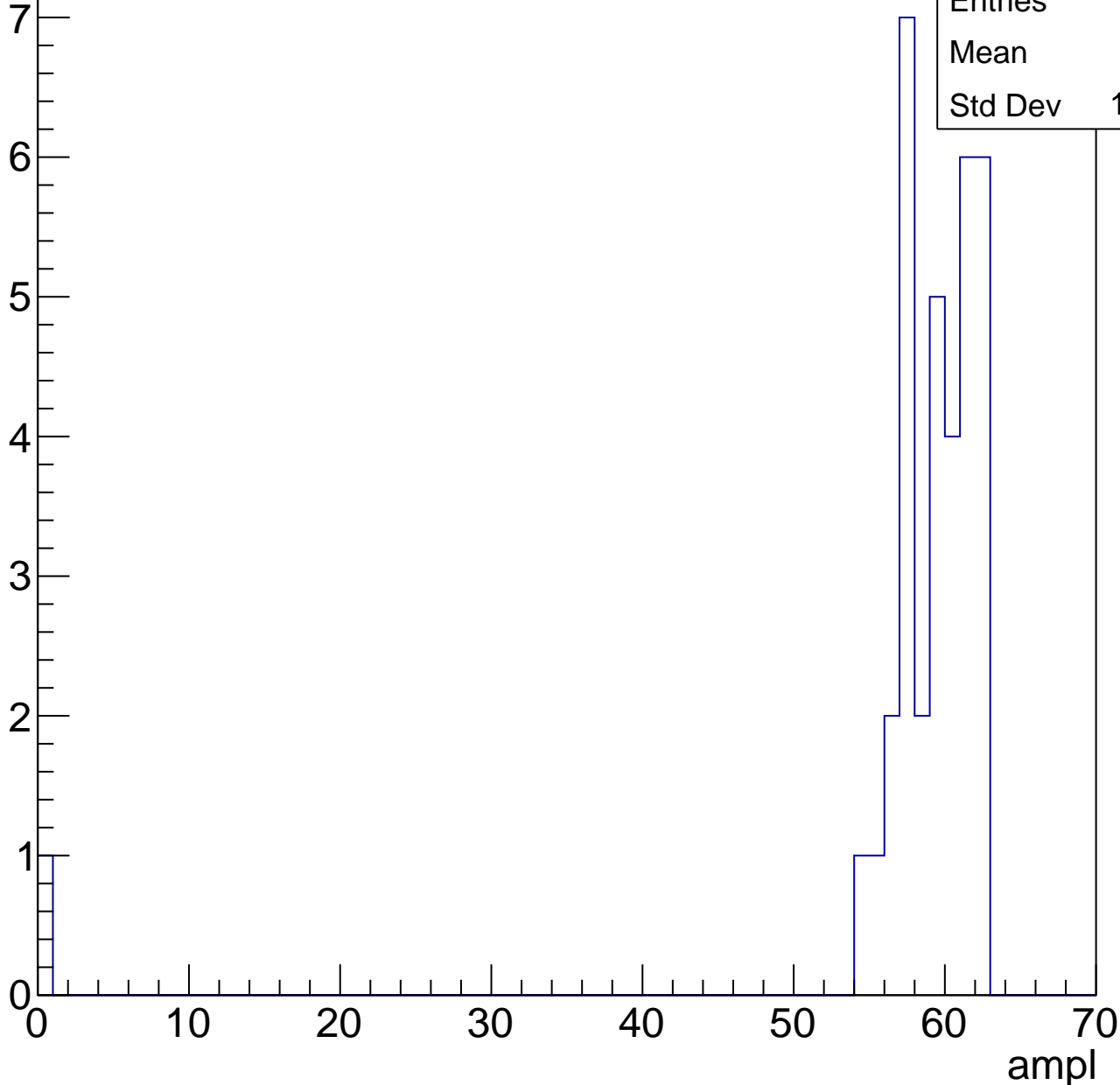


# B1L102S, U16-ch12, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	35
Mean	57.4
Std Dev	10.09

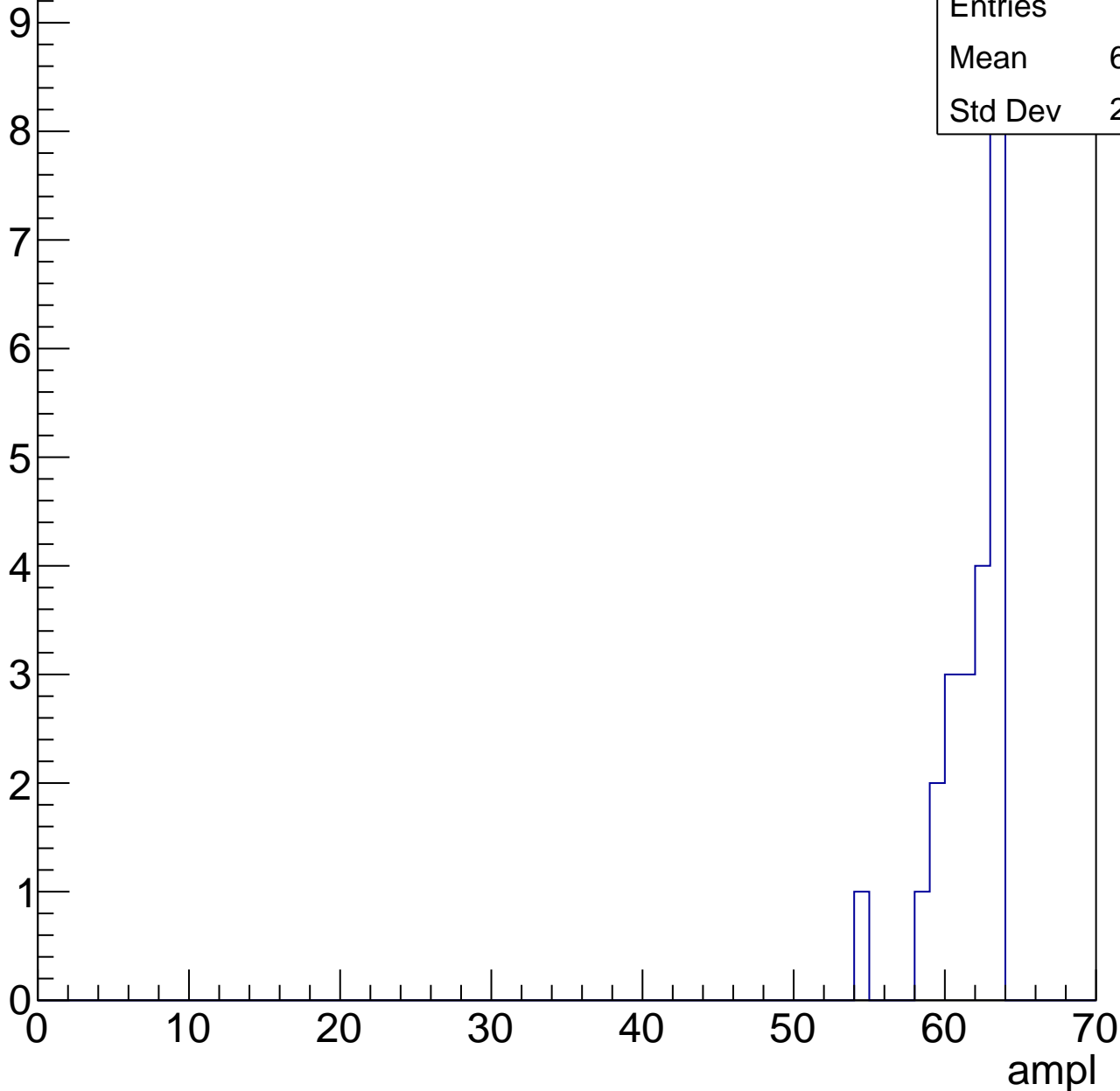


# B1L102S, U16-ch12, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	23
Mean	61.22
Std Dev	2.166





# B1L102S, U16-ch12, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch13, adc0

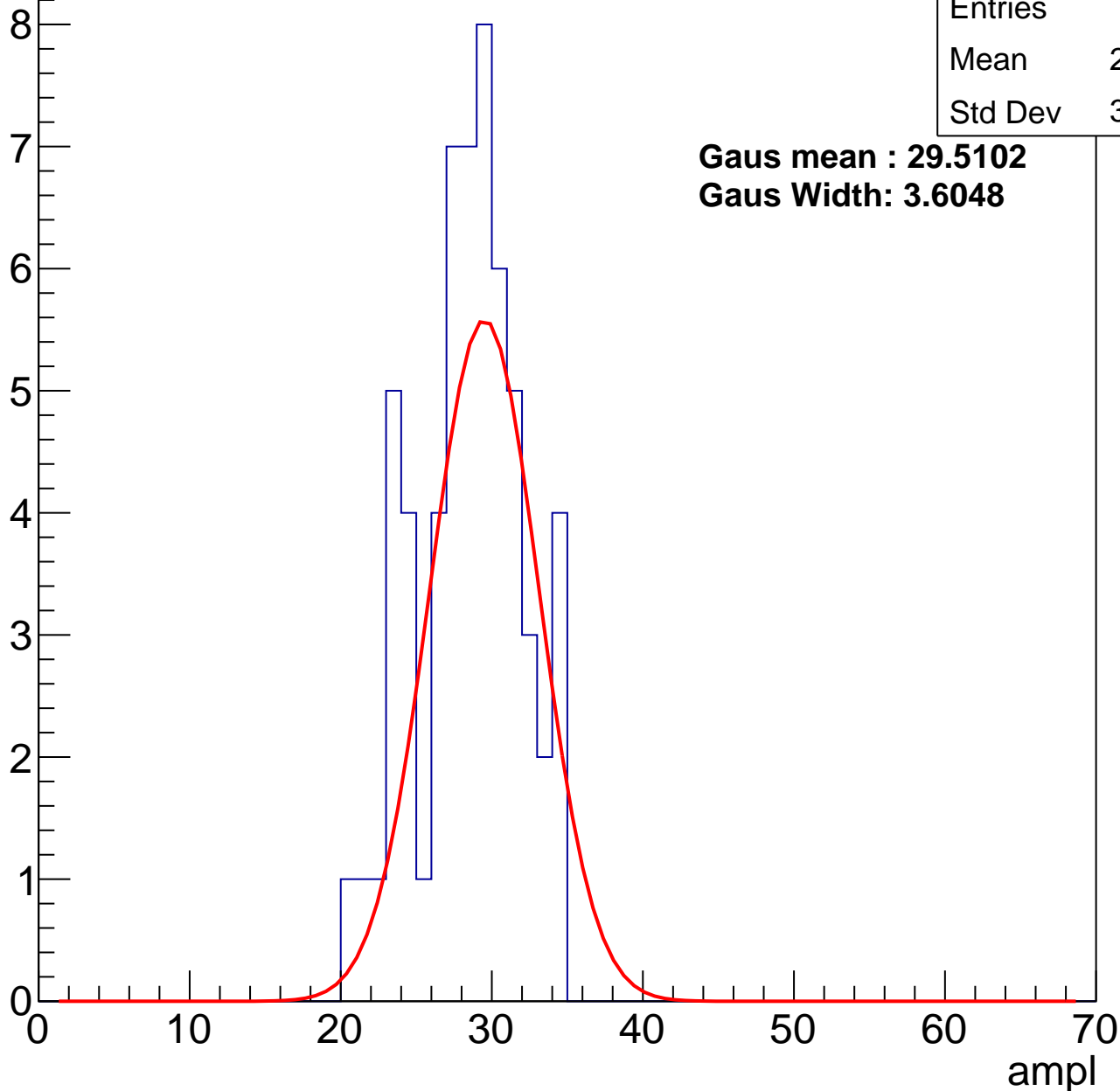
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	28.02
Std Dev	3.417

**Gaus mean : 29.5102**

**Gaus Width: 3.6048**



# B1L102S, U16-ch13, adc1

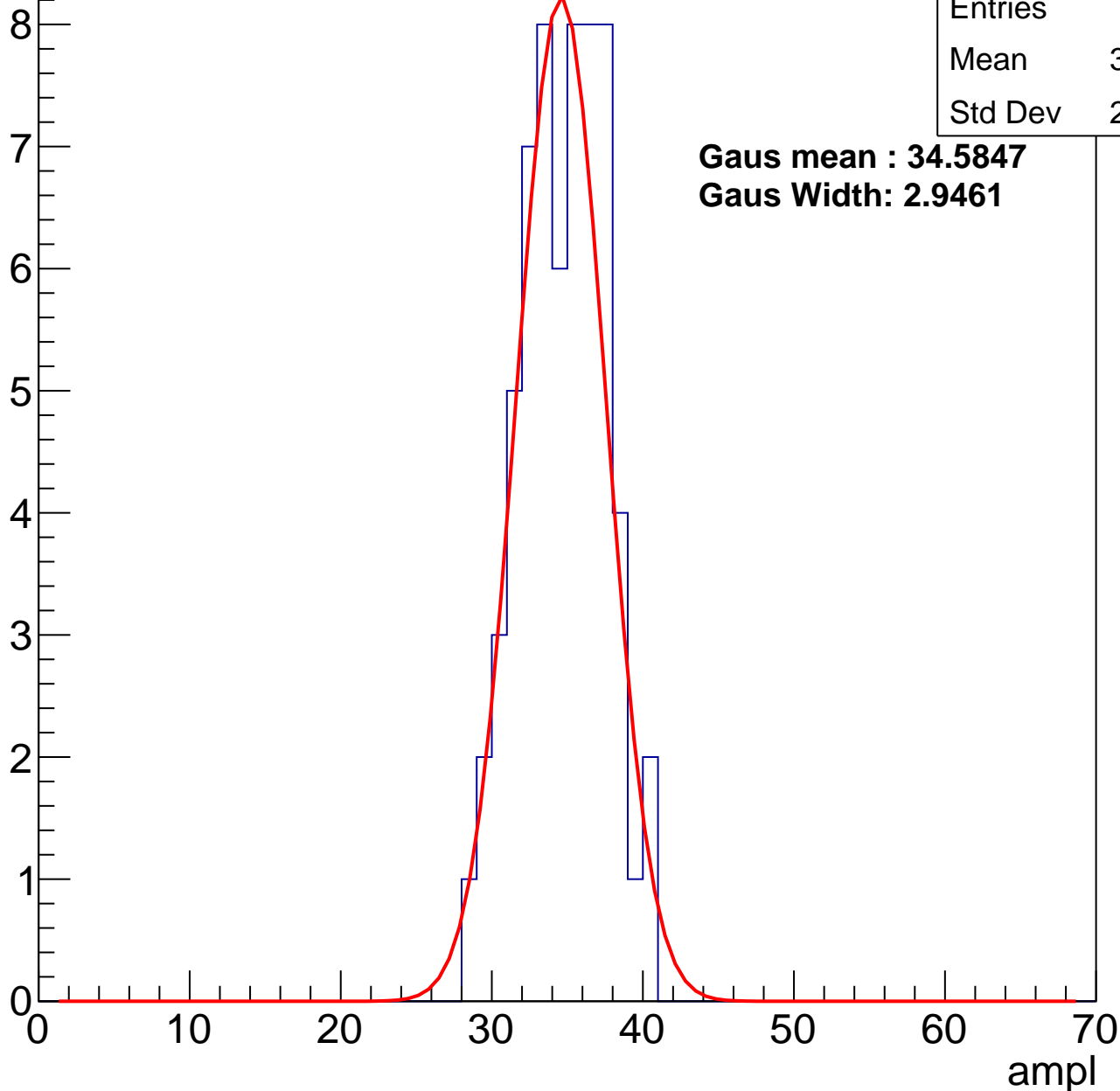
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	34.25
Std Dev	2.772

**Gaus mean : 34.5847**

**Gaus Width: 2.9461**



# B1L102S, U16-ch13, adc2

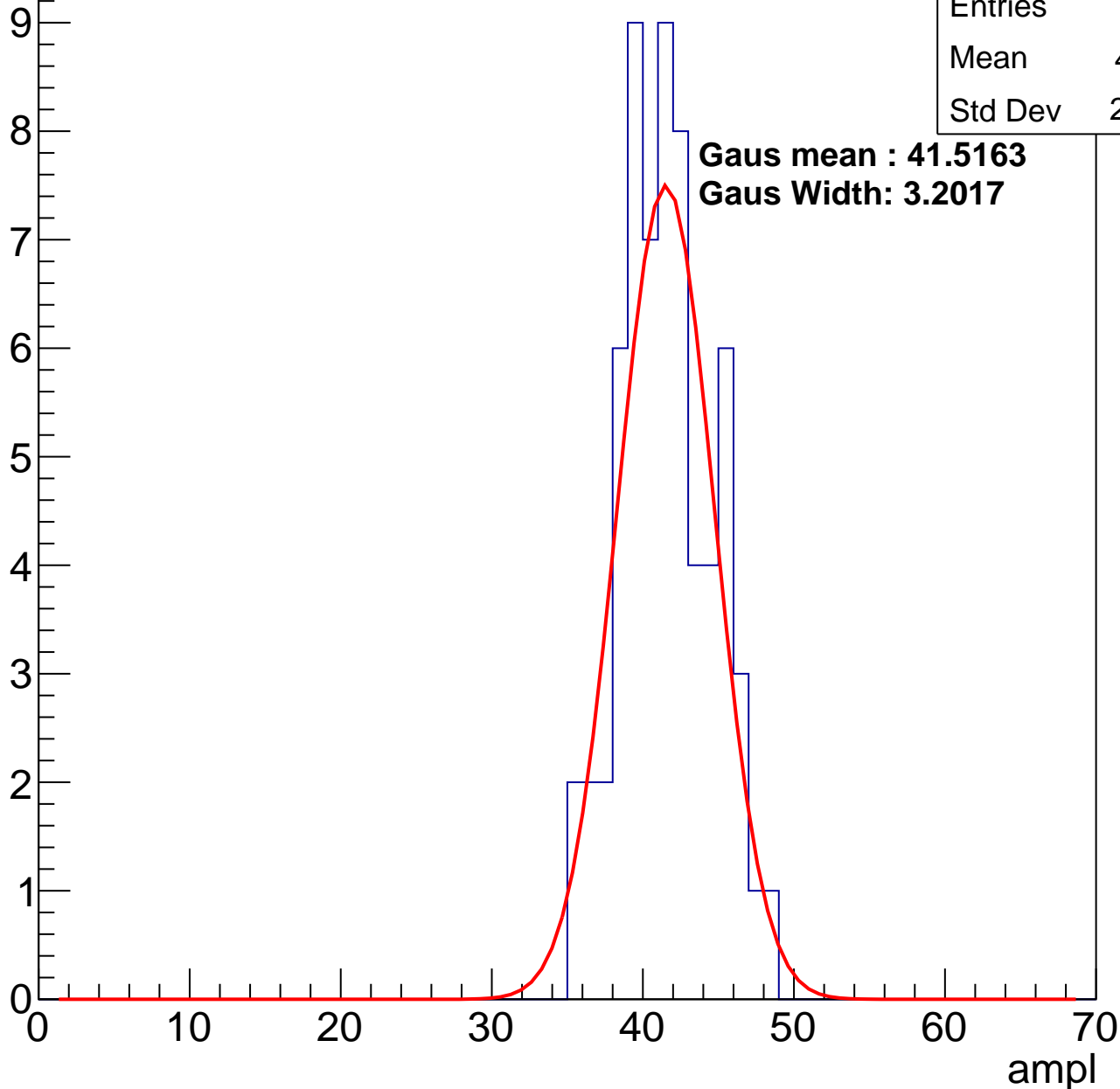
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	41.11
Std Dev	2.974

**Gaus mean : 41.5163**

**Gaus Width: 3.2017**



# B1L102S, U16-ch13, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

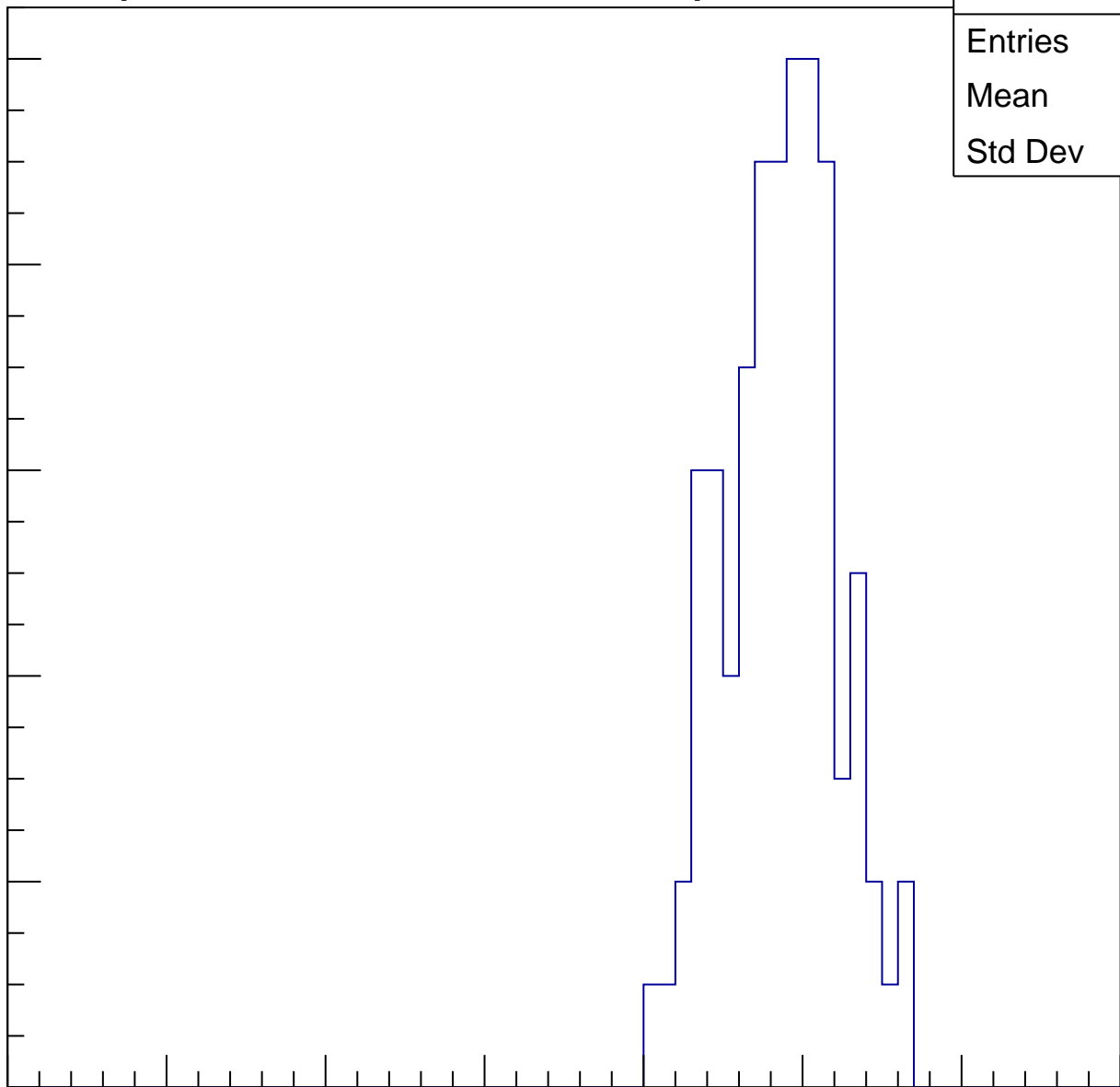
Entries	87
Mean	48.15
Std Dev	3.482

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

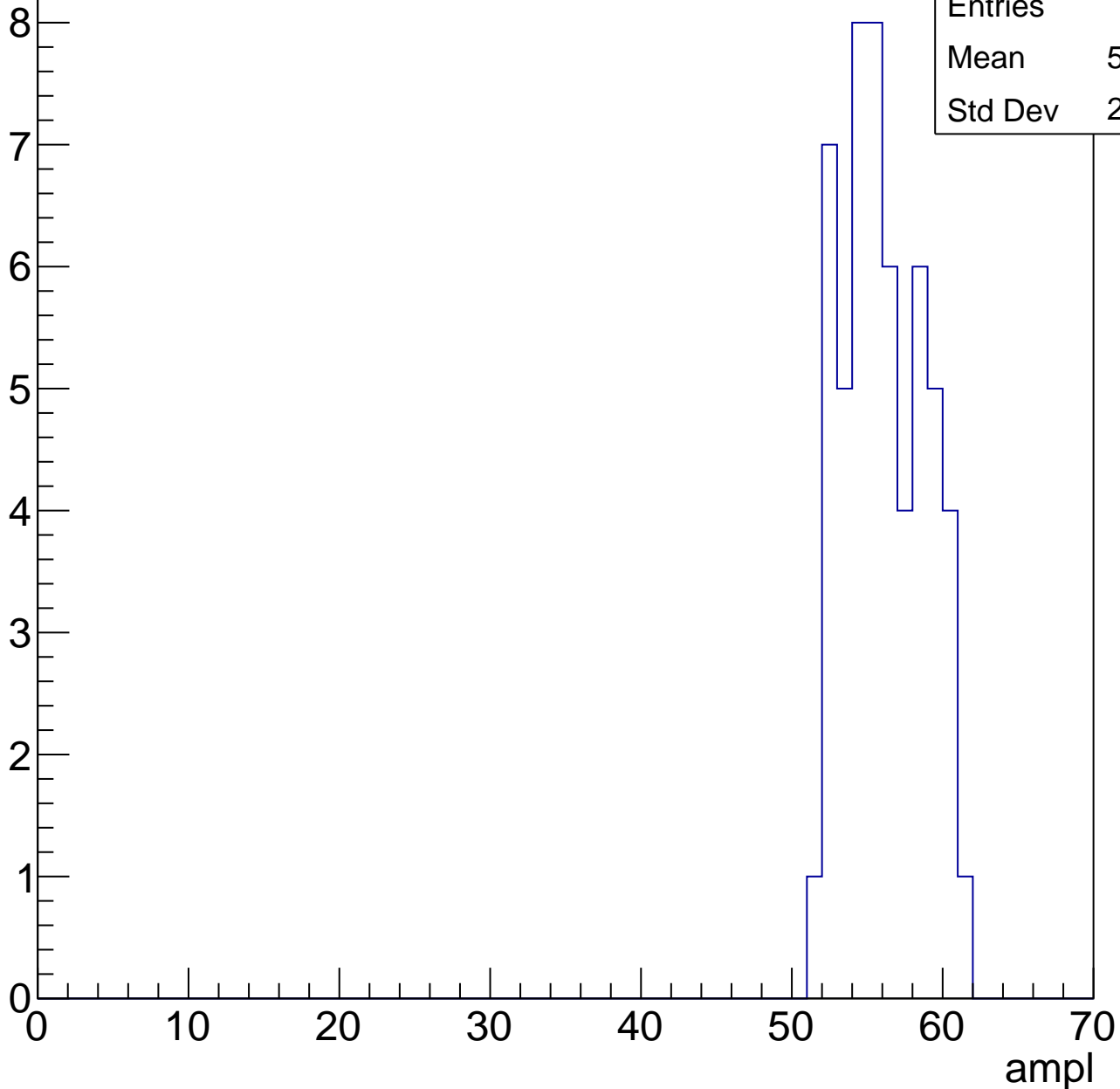


# B1L102S, U16-ch13, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	55.64
Std Dev	2.617

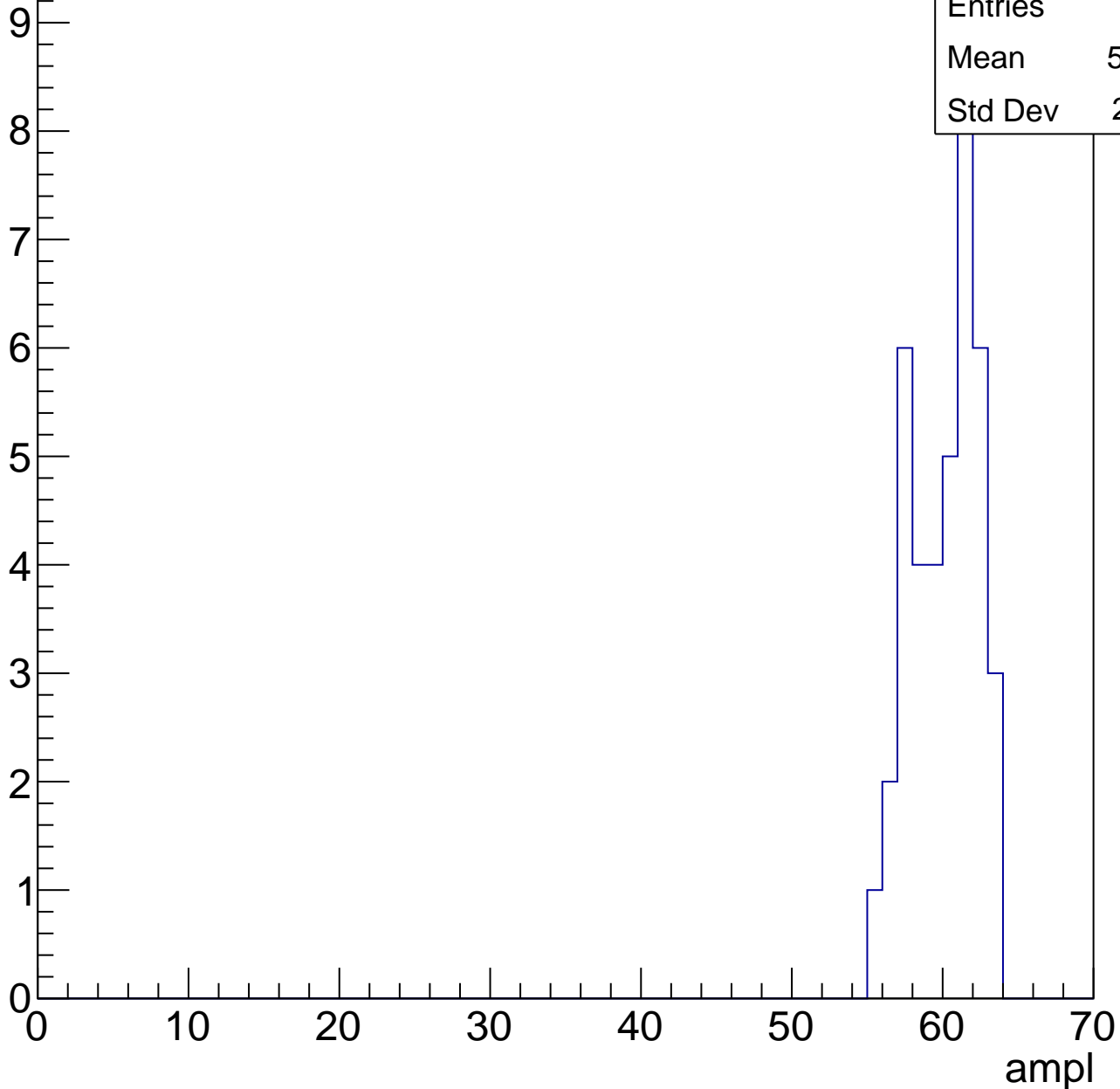


# B1L102S, U16-ch13, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	59.67
Std Dev	2.161

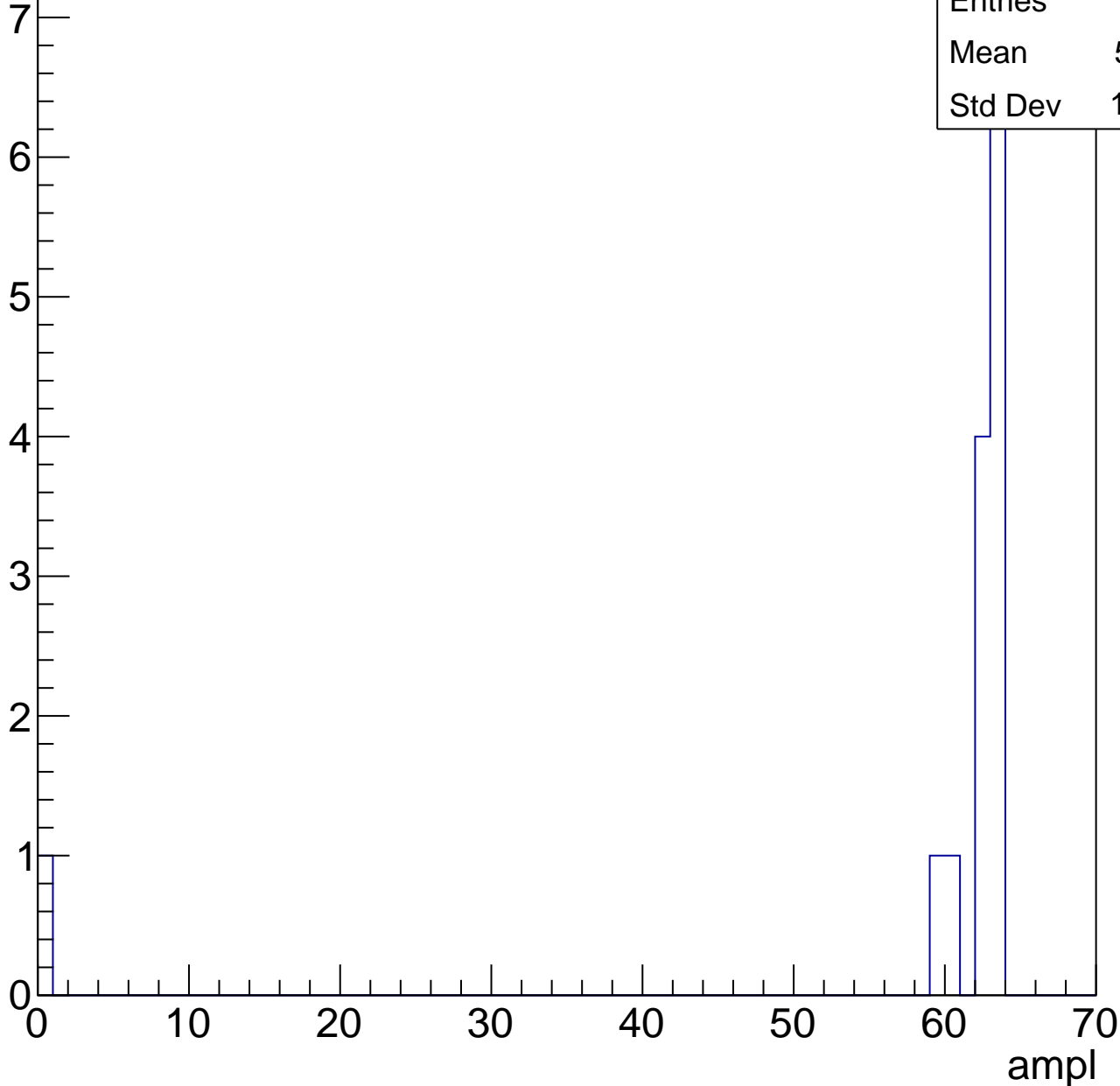


# B1L102S, U16-ch13, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	14
Mean	57.71
Std Dev	16.05





# B1L102S, U16-ch13, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch14, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	84
Mean	27.17
Std Dev	6.38

**Gaus mean : 28.7817**

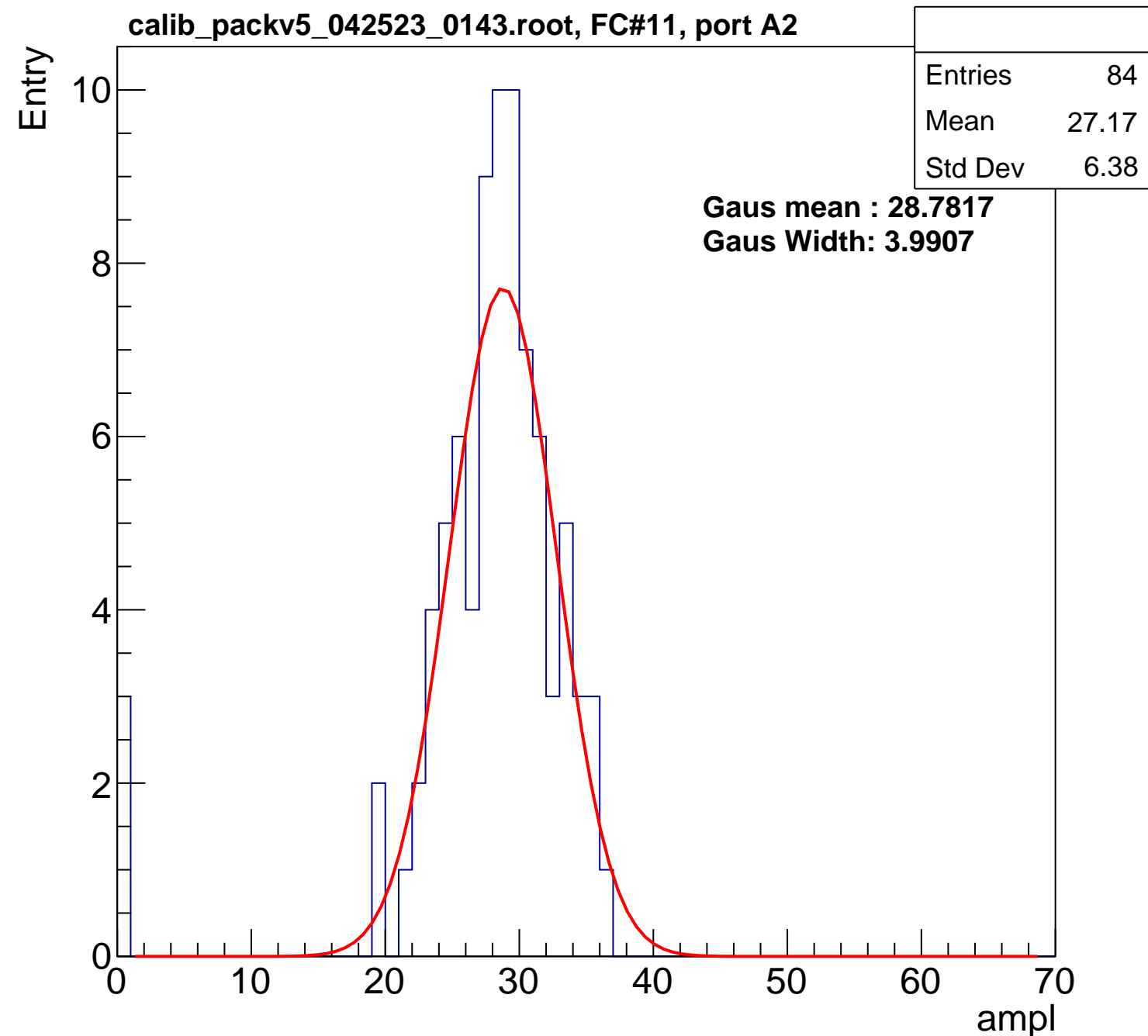
**Gaus Width: 3.9907**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



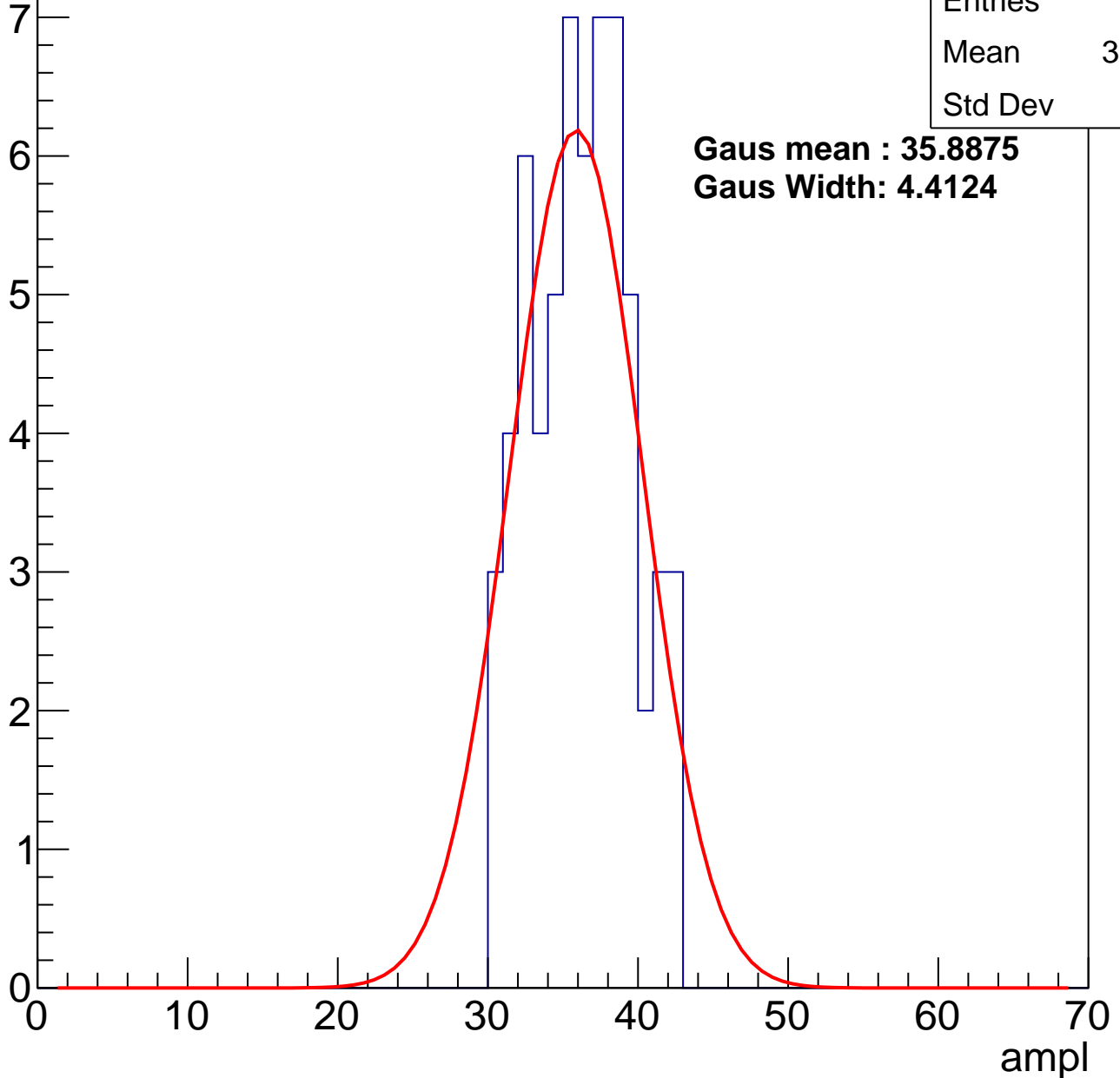
# B1L102S, U16-ch14, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	35.77
Std Dev	3.26

**Gaus mean : 35.8875**  
**Gaus Width: 4.4124**



# B1L102S, U16-ch14, adc2

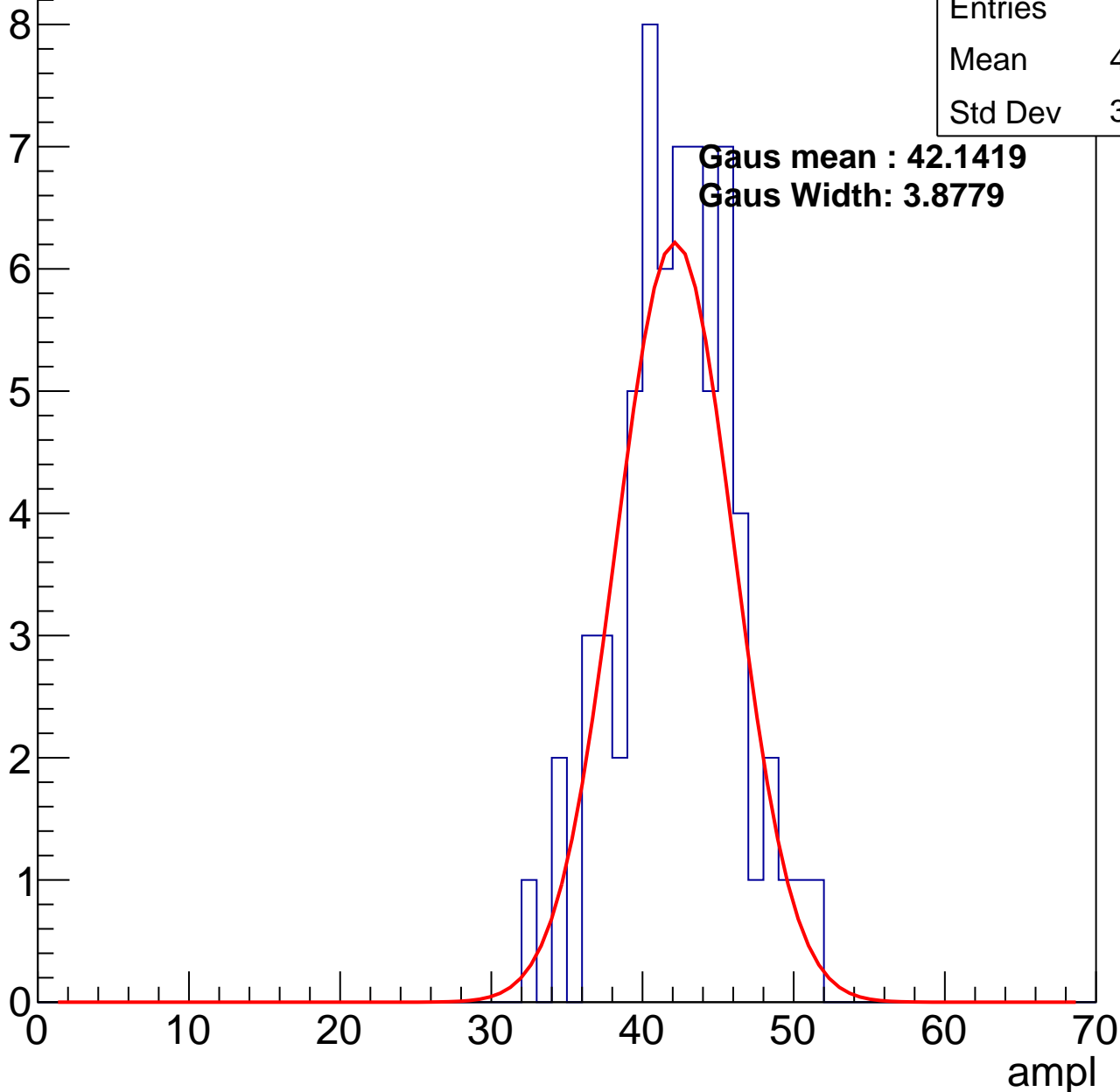
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	41.86
Std Dev	3.833

**Gaus mean : 42.1419**

**Gaus Width: 3.8779**

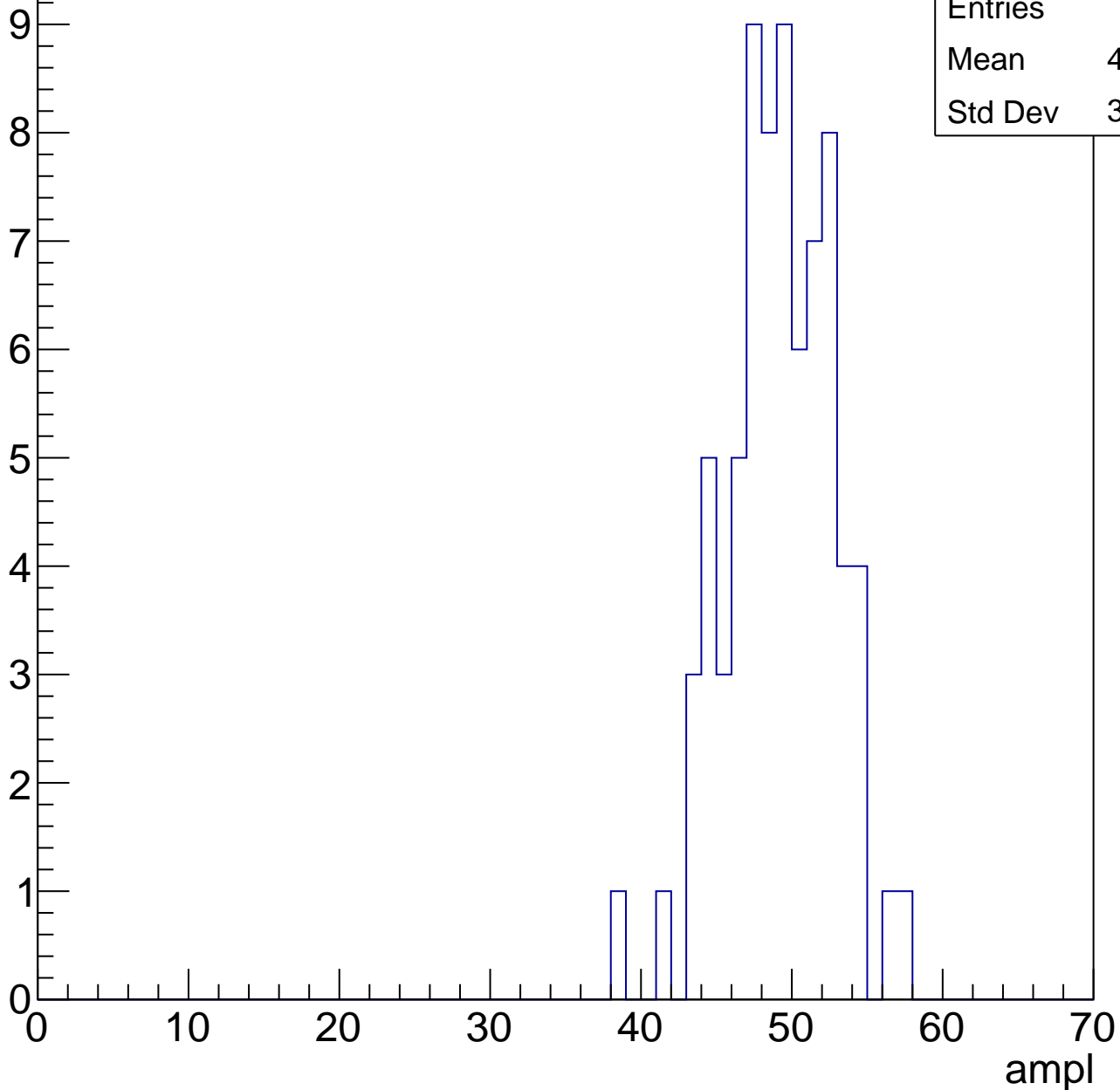


# B1L102S, U16-ch14, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	48.73
Std Dev	3.526

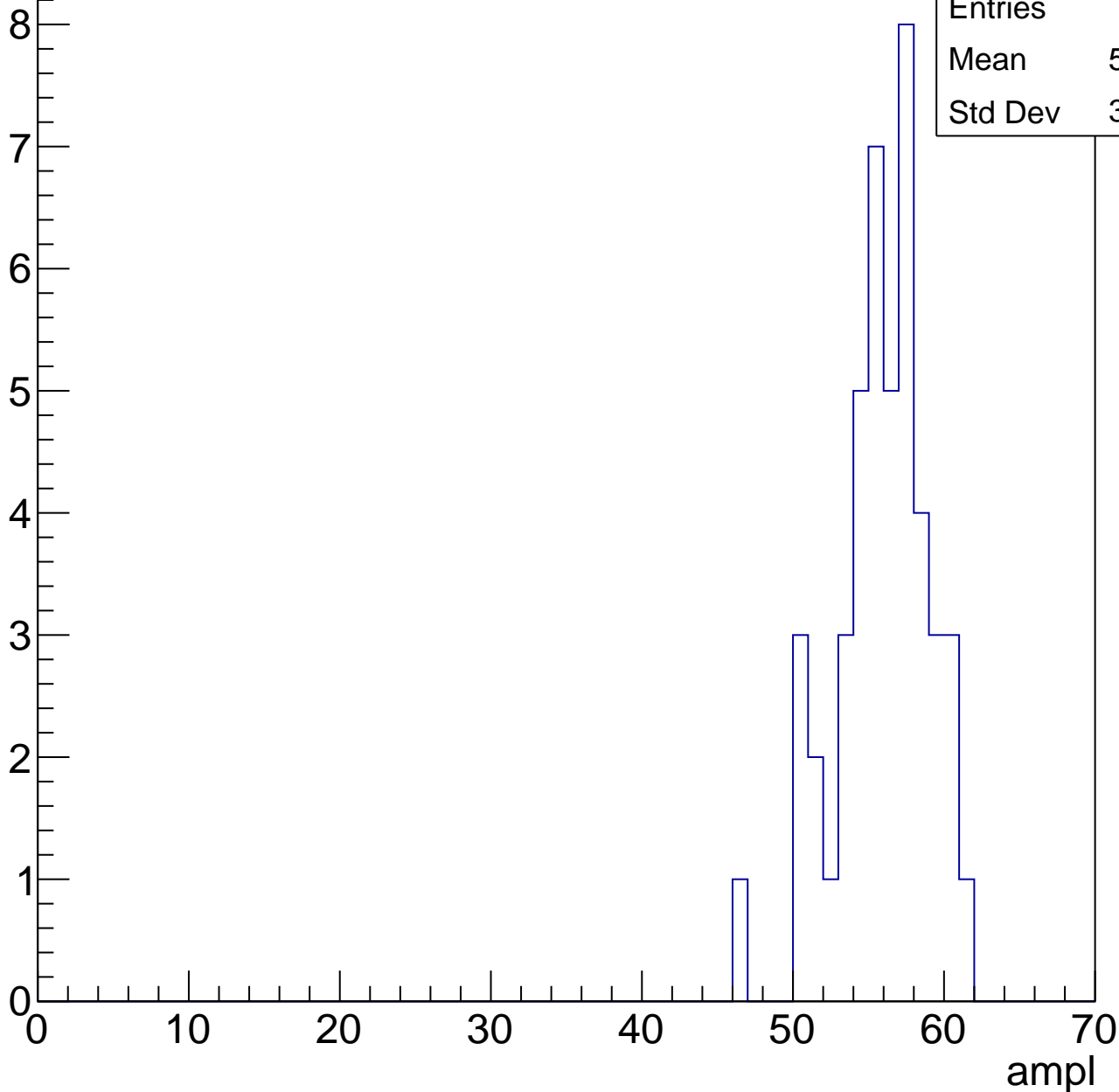


# B1L102S, U16-ch14, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	55.43
Std Dev	3.083

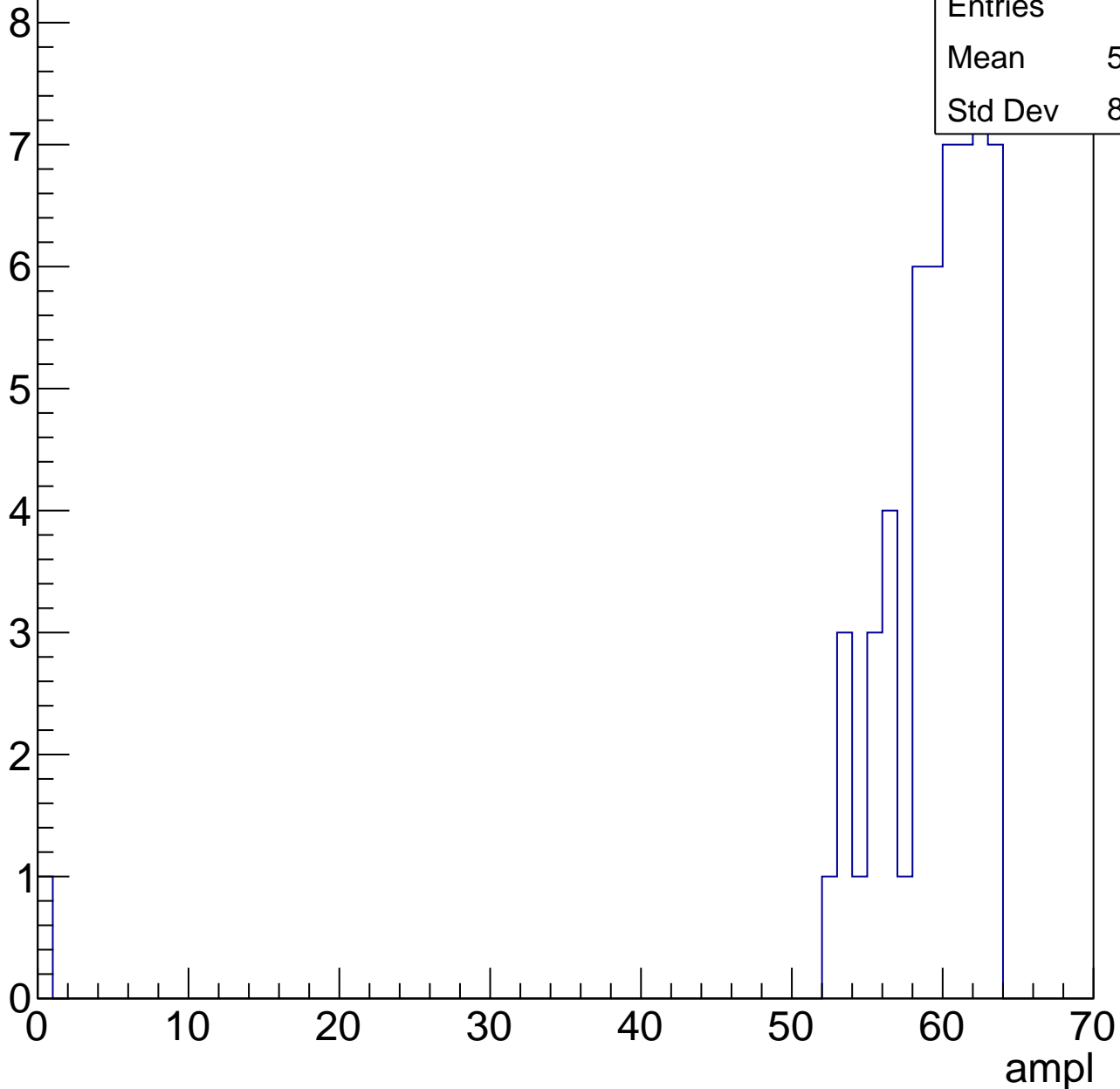


# B1L102S, U16-ch14, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

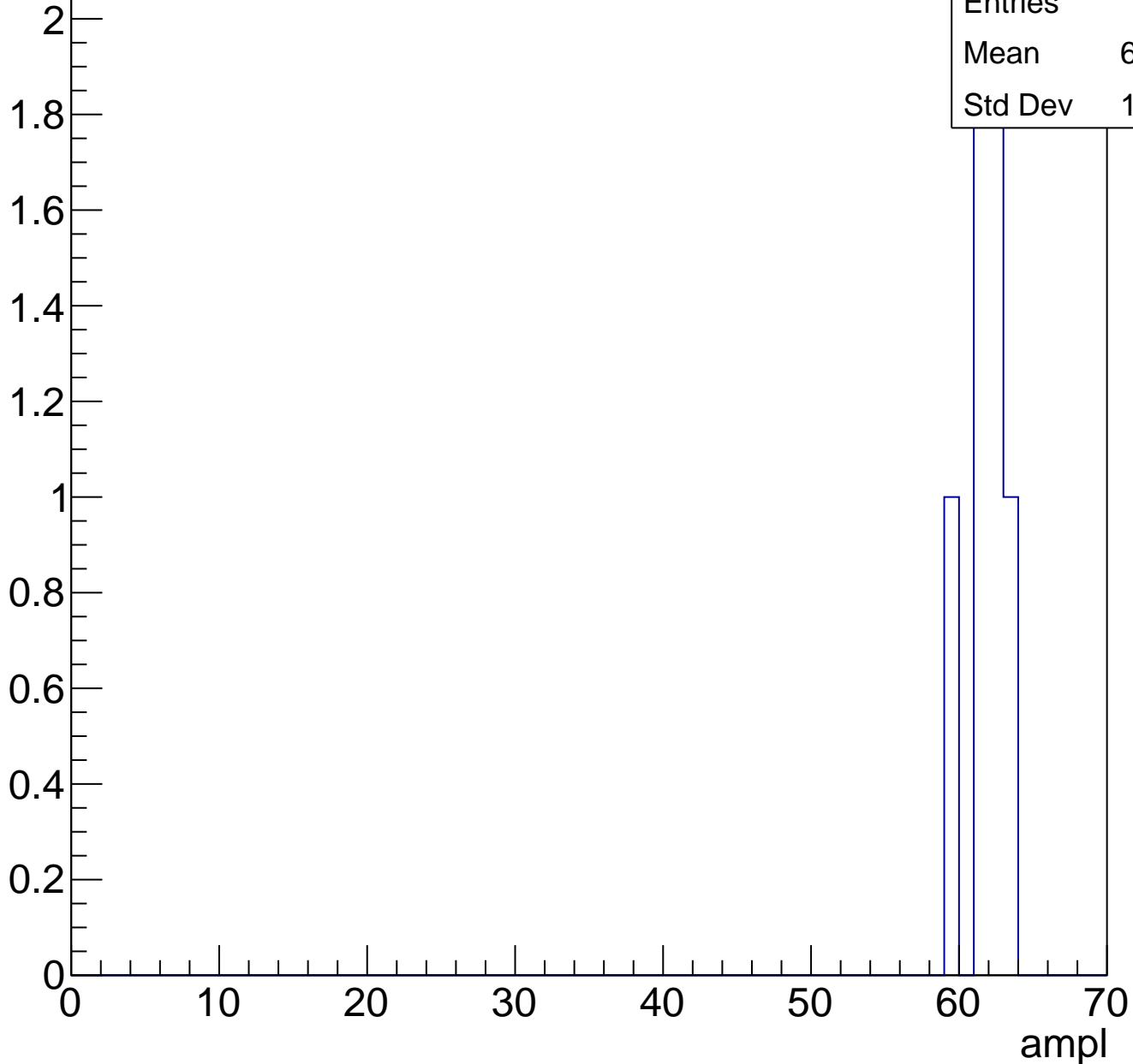
Entries	55
Mean	58.13
Std Dev	8.457



# B1L102S, U16-ch14, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch14, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch15, adc0

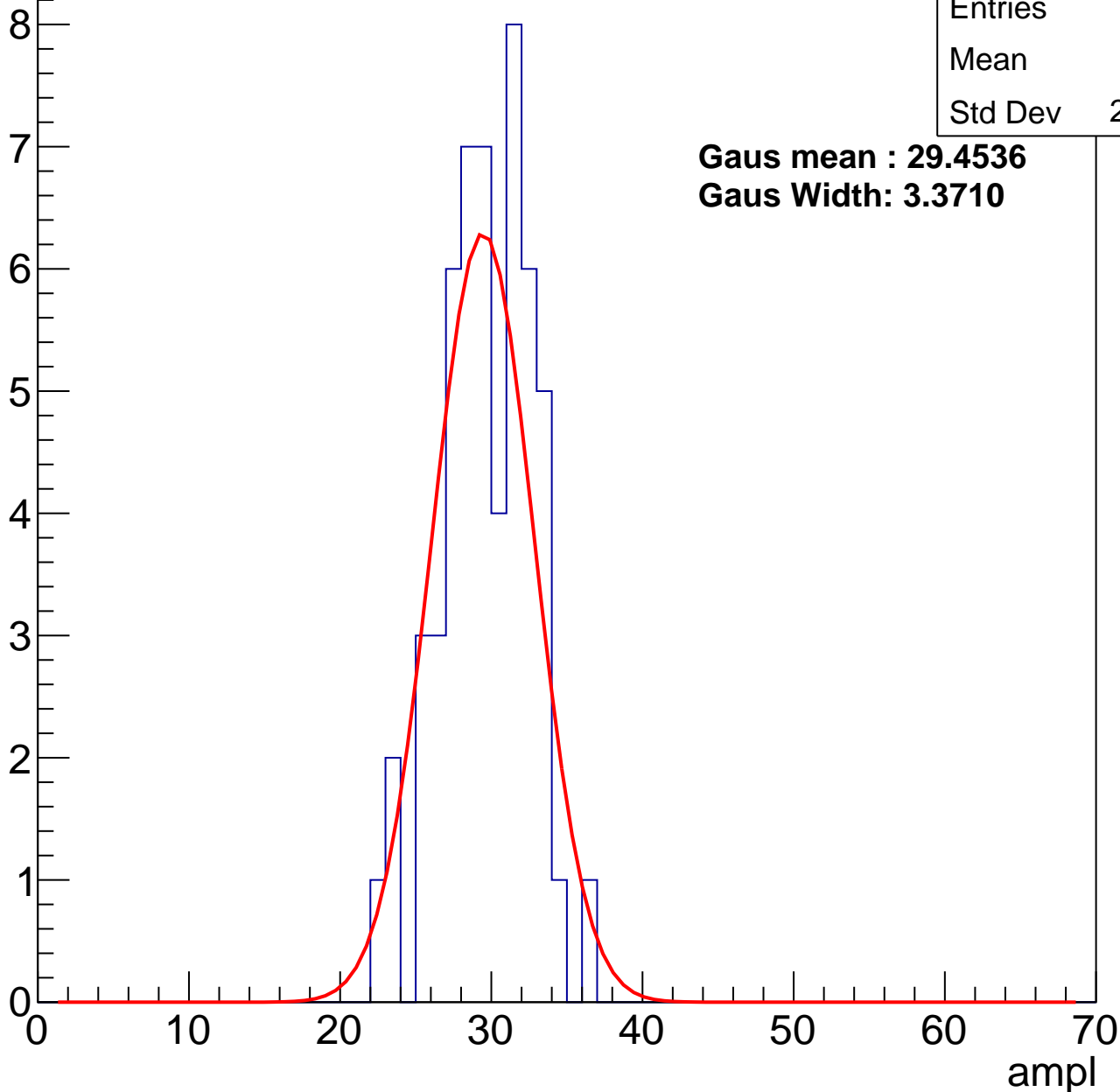
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	29.2
Std Dev	2.946

**Gaus mean : 29.4536**

**Gaus Width: 3.3710**



# B1L102S, U16-ch15, adc1

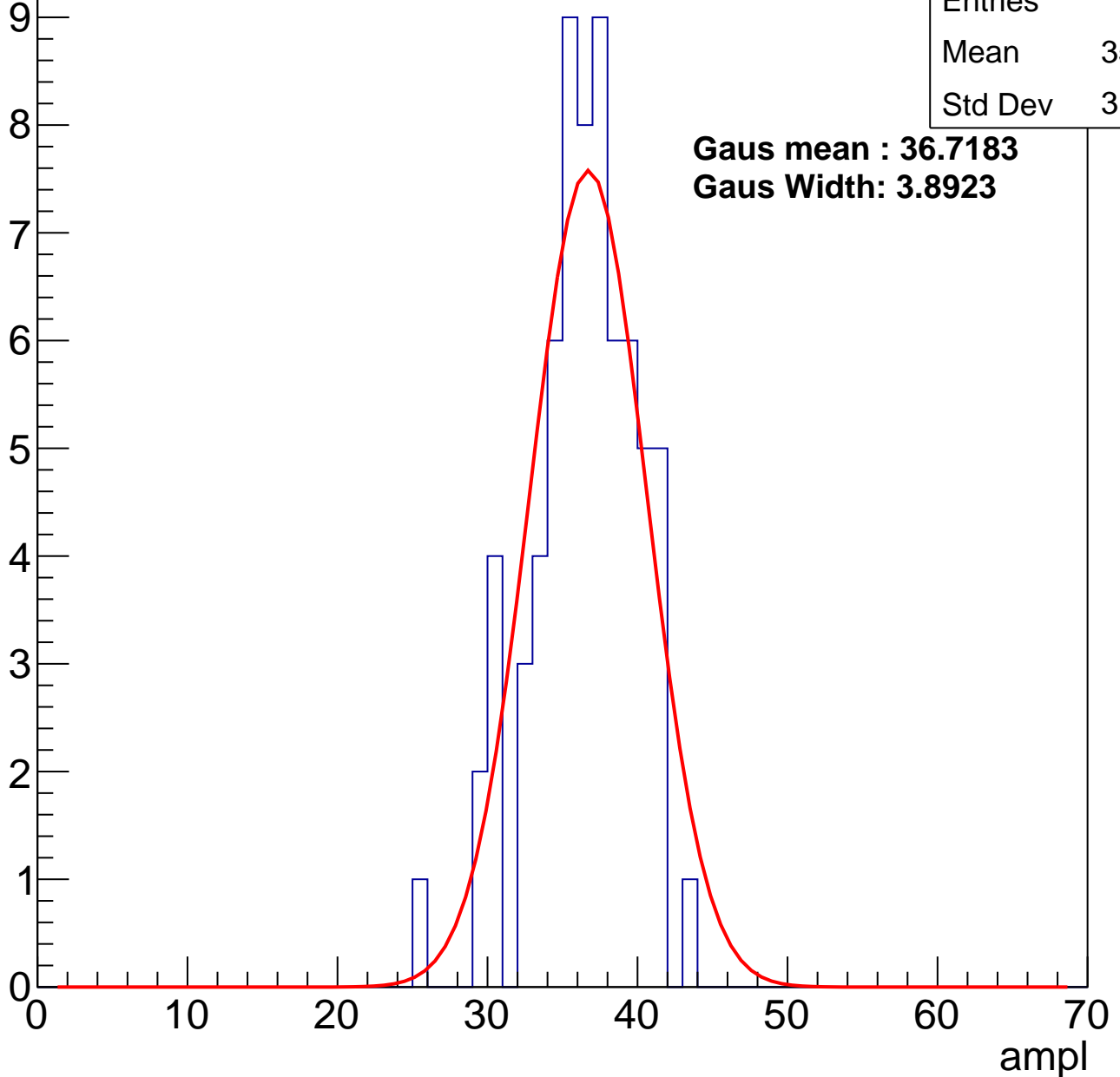
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	35.96
Std Dev	3.449

**Gaus mean : 36.7183**

**Gaus Width: 3.8923**



# B1L102S, U16-ch15, adc2

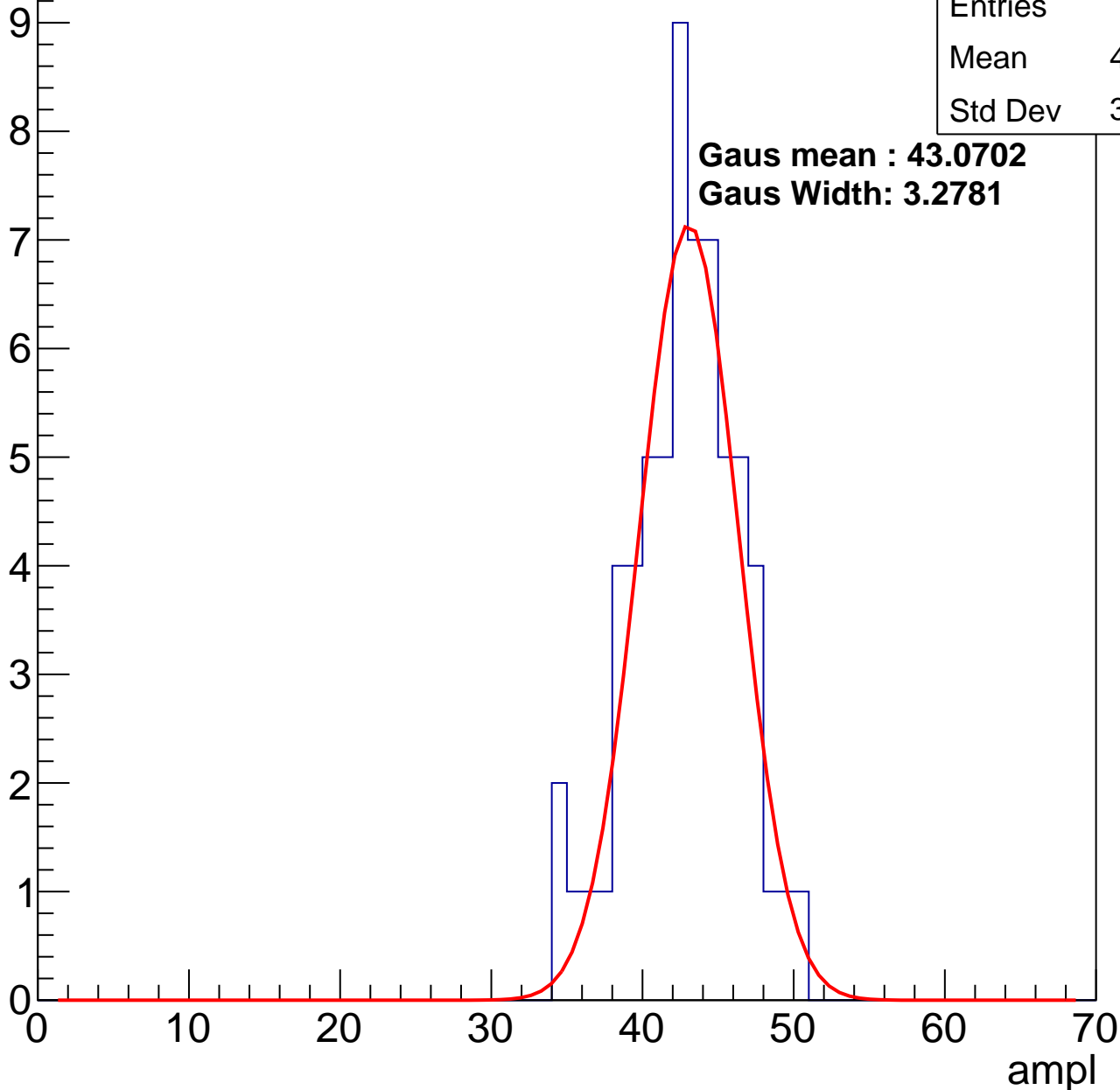
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	42.32
Std Dev	3.486

**Gaus mean : 43.0702**

**Gaus Width: 3.2781**

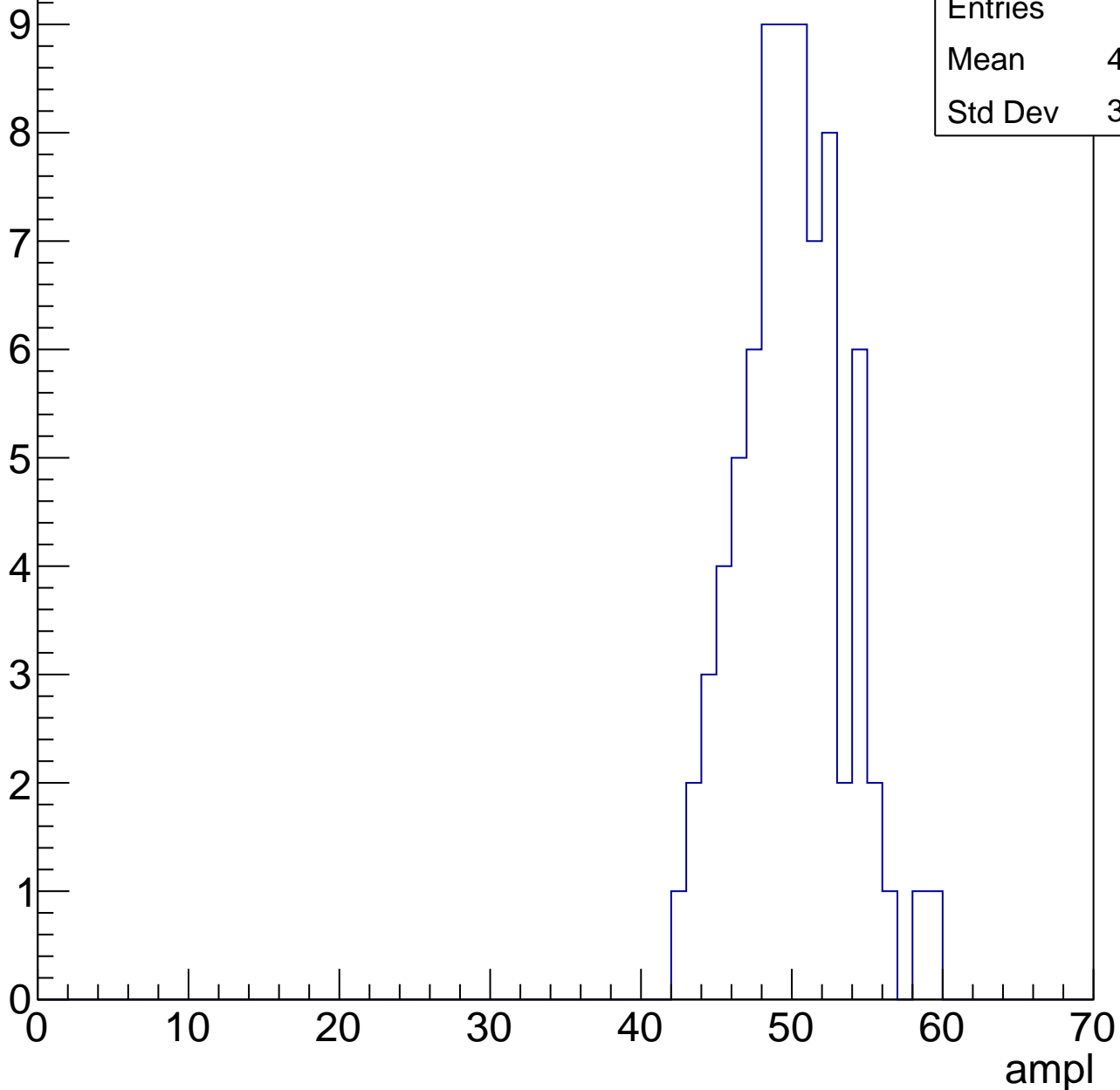


# B1L102S, U16-ch15, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	49.49
Std Dev	3.466

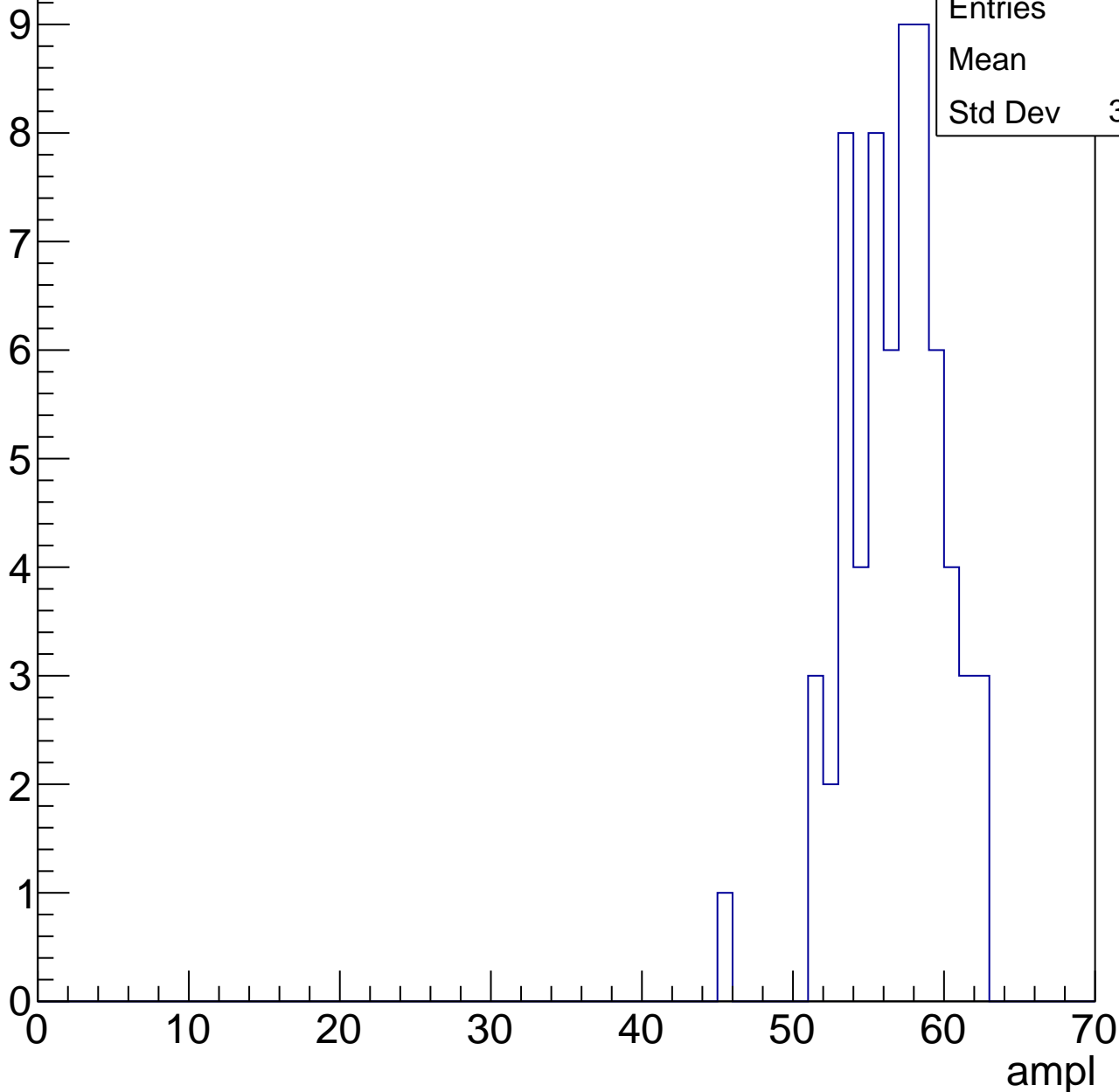


# B1L102S, U16-ch15, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	56.3
Std Dev	3.172

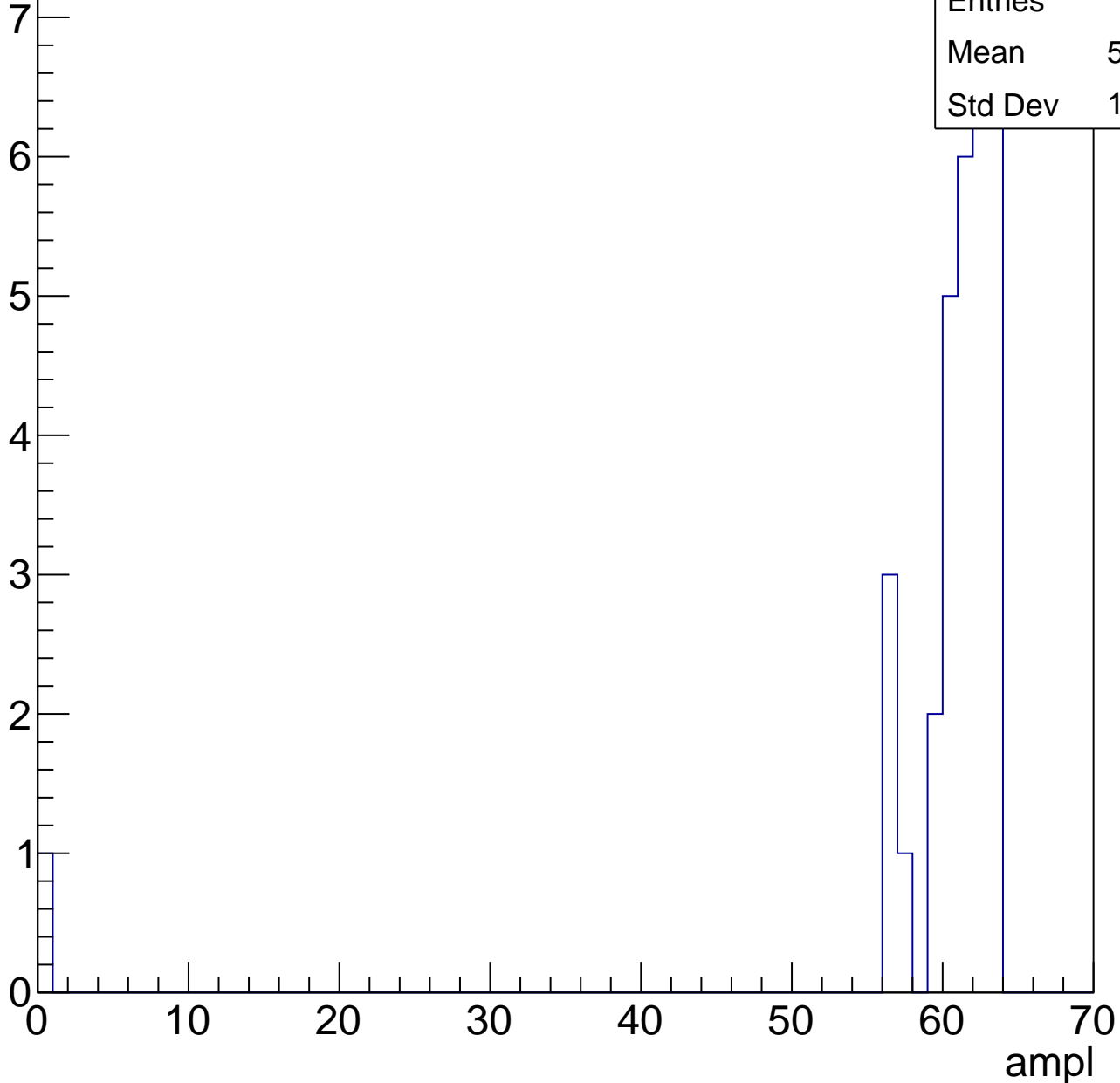


# B1L102S, U16-ch15, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

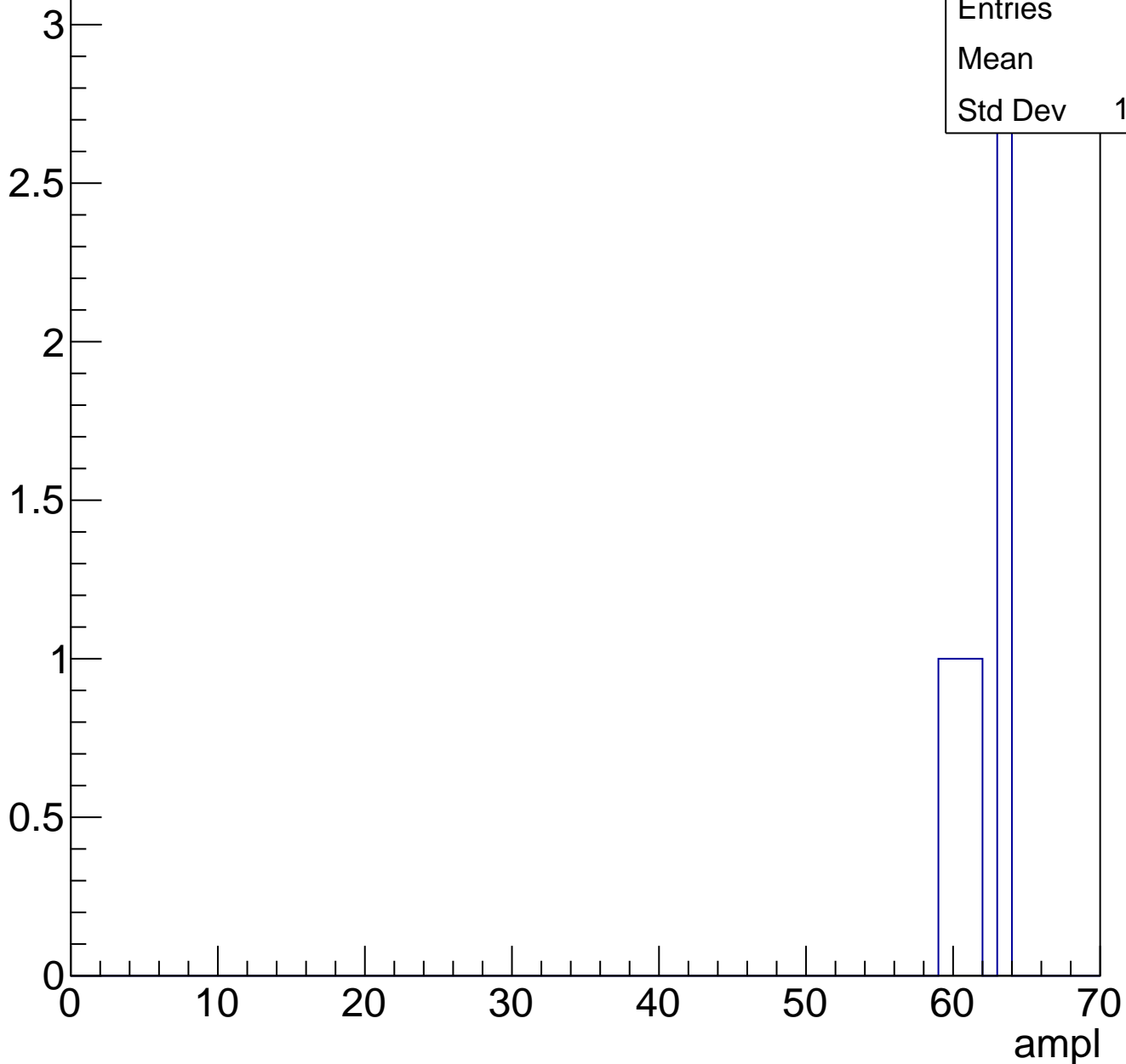
Entries	32
Mean	58.88
Std Dev	10.78



# B1L102S, U16-ch15, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch15, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U16-ch16, adc0

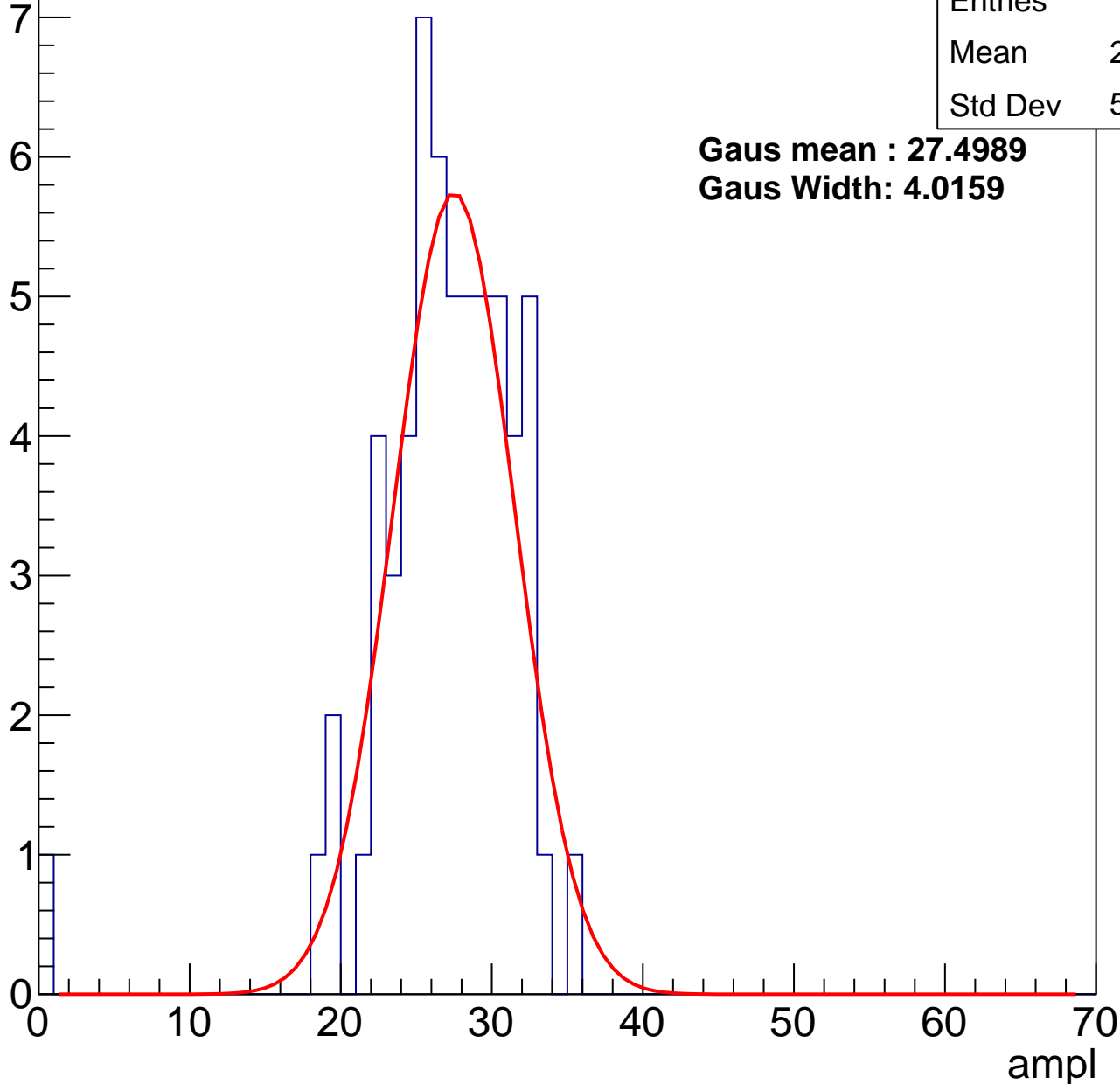
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	26.38
Std Dev	5.047

**Gaus mean : 27.4989**

**Gaus Width: 4.0159**



# B1L102S, U16-ch16, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	84
Mean	34
Std Dev	3.7

**Gaus mean : 34.3070**

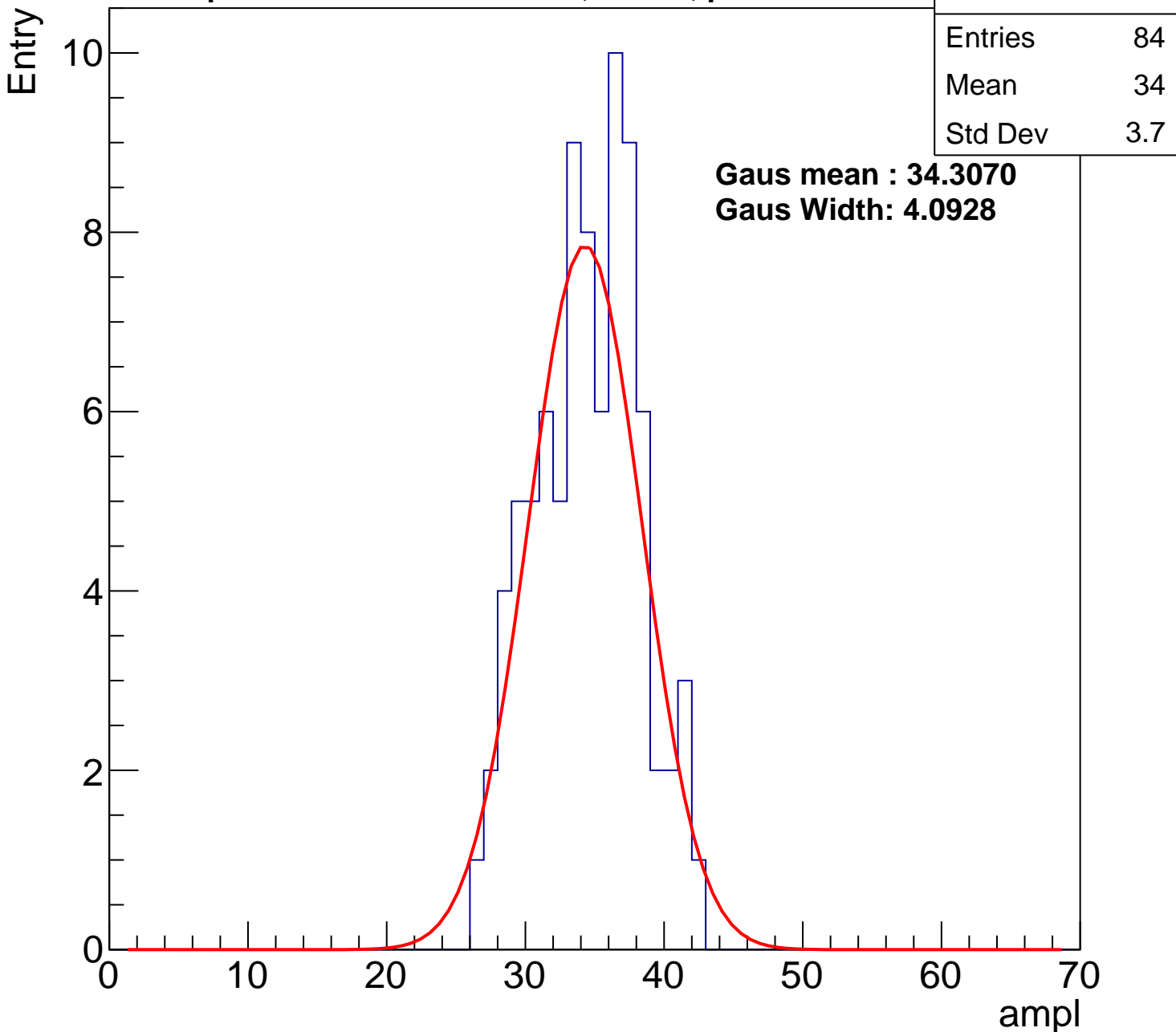
**Gaus Width: 4.0928**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U16-ch16, adc2

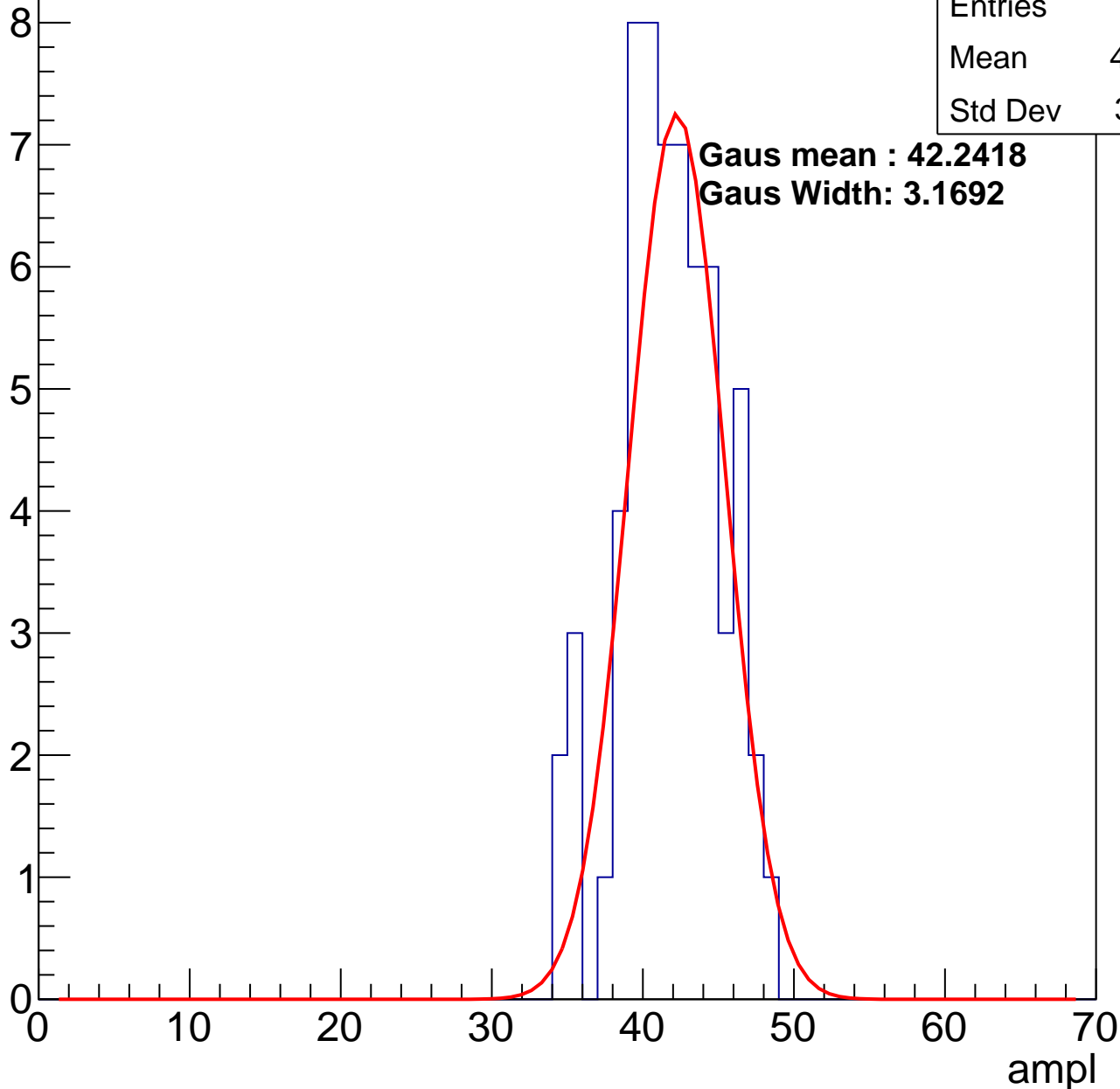
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	41.33
Std Dev	3.261

**Gaus mean : 42.2418**

**Gaus Width: 3.1692**

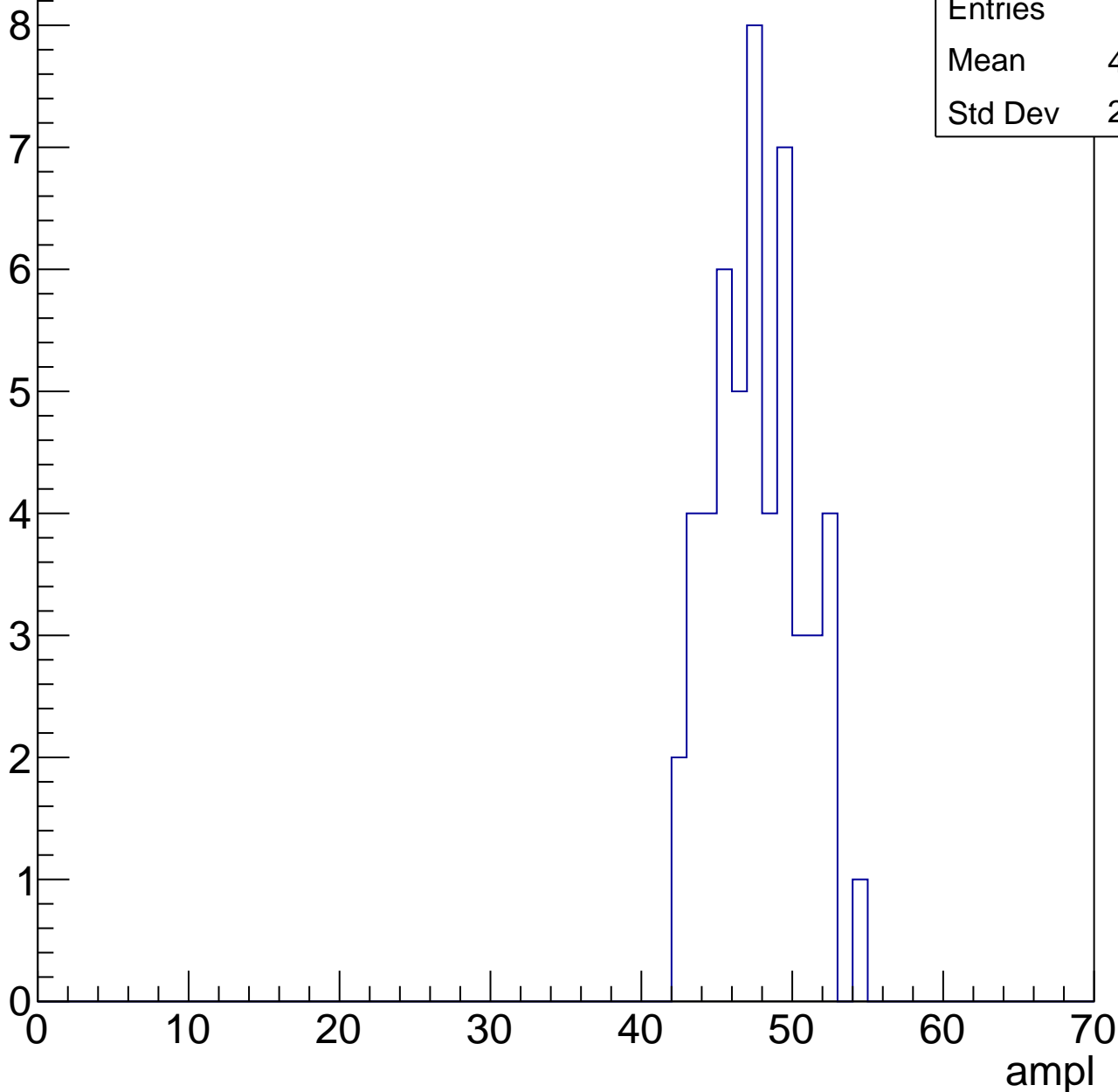


# B1L102S, U16-ch16, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	47.22
Std Dev	2.913

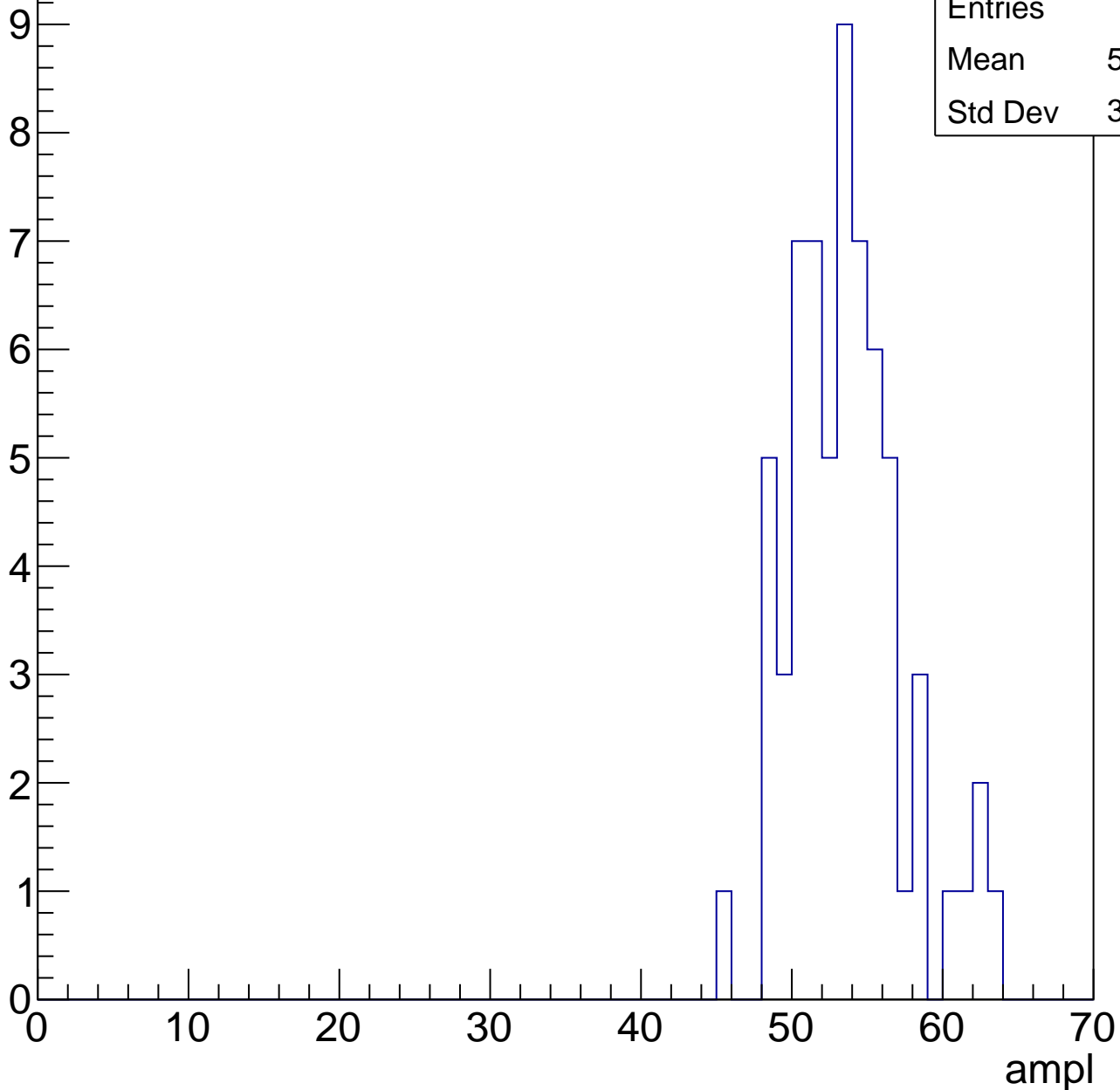


# B1L102S, U16-ch16, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	53.17
Std Dev	3.694

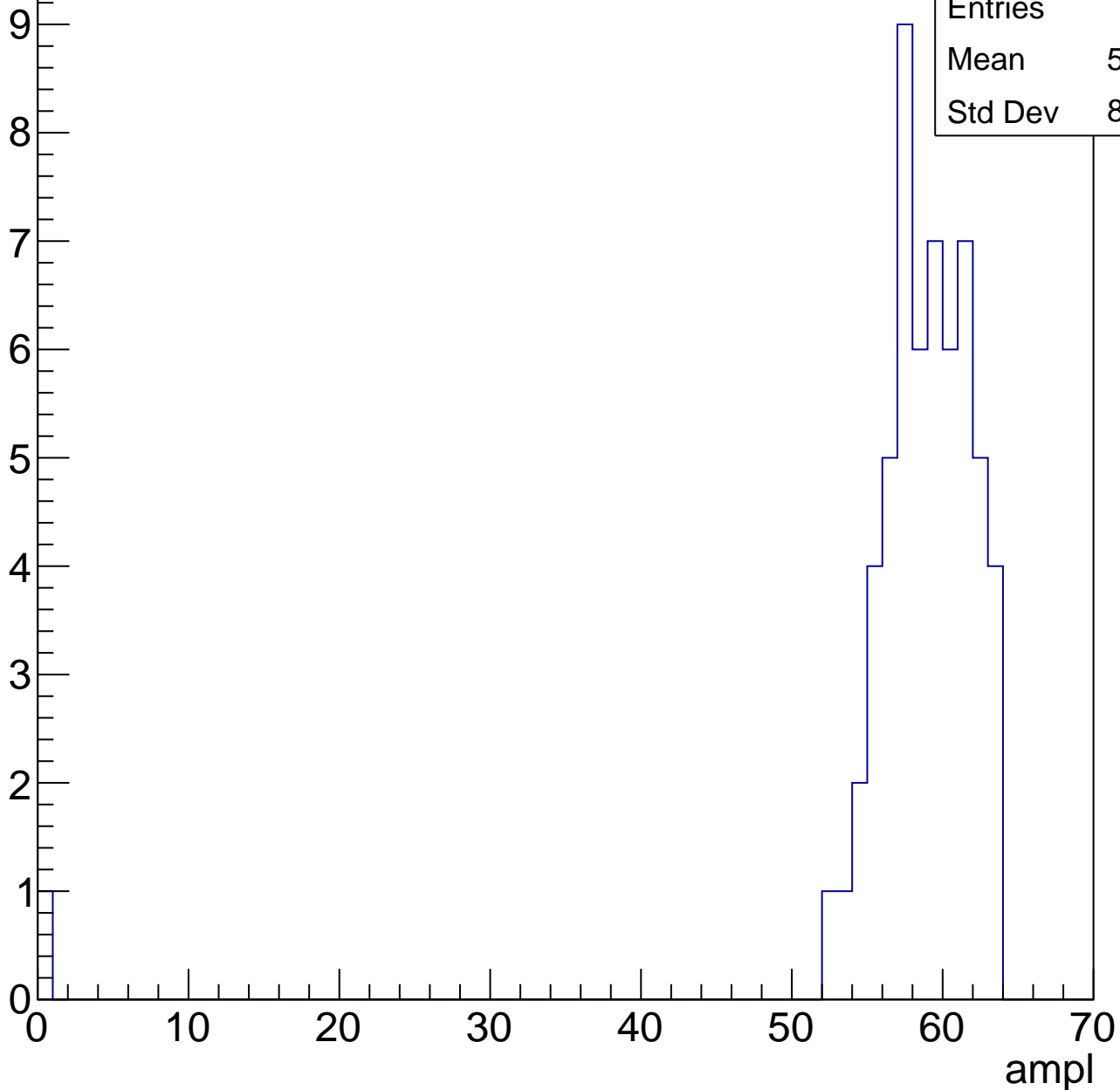


# B1L102S, U16-ch16, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	57.52
Std Dev	8.076



# B1L102S, U16-ch16, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries	15
Mean	60.8
Std Dev	1.6



# B1L102S, U16-ch16, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch17, adc0

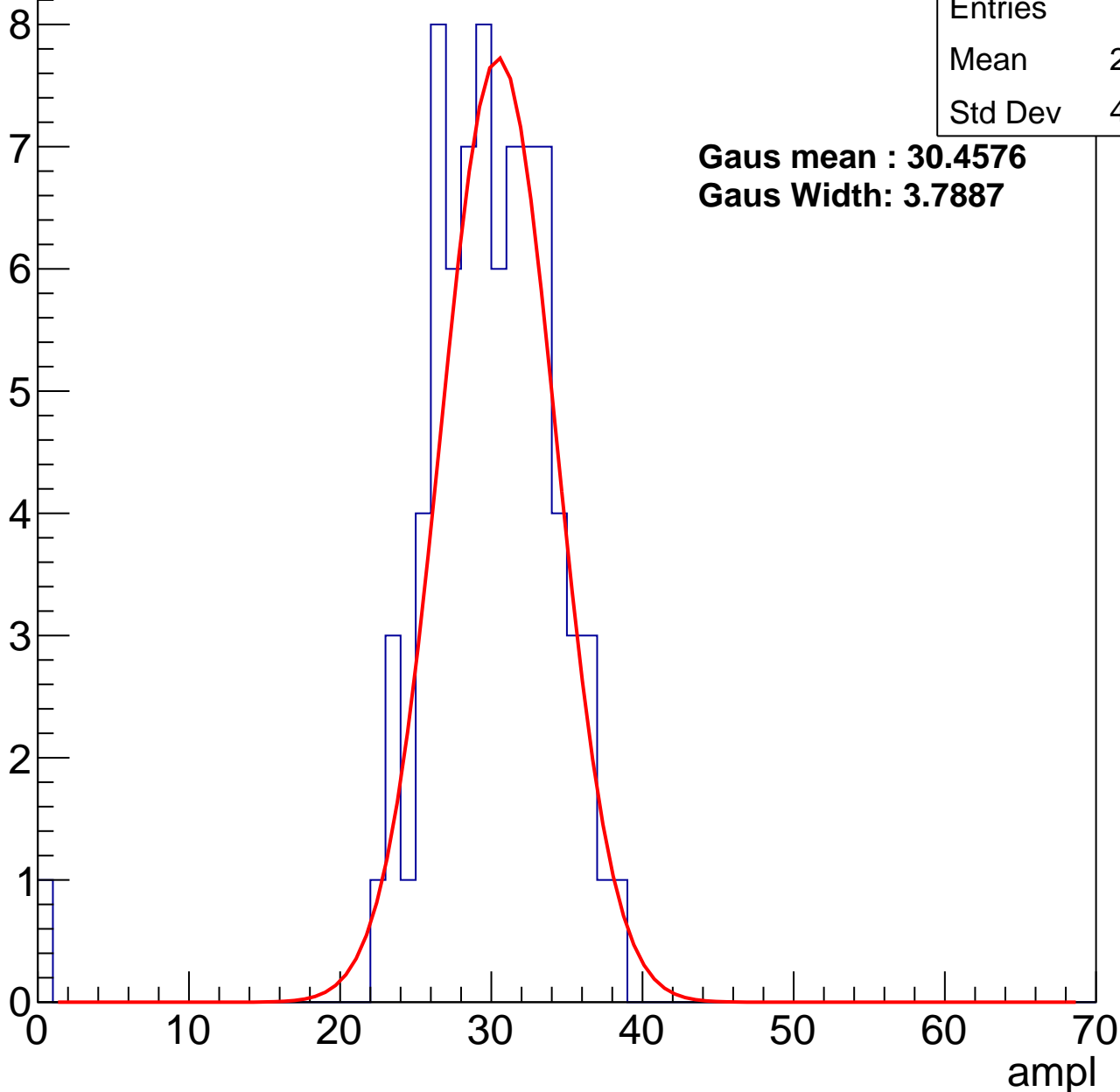
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	29.35
Std Dev	4.922

**Gaus mean : 30.4576**

**Gaus Width: 3.7887**



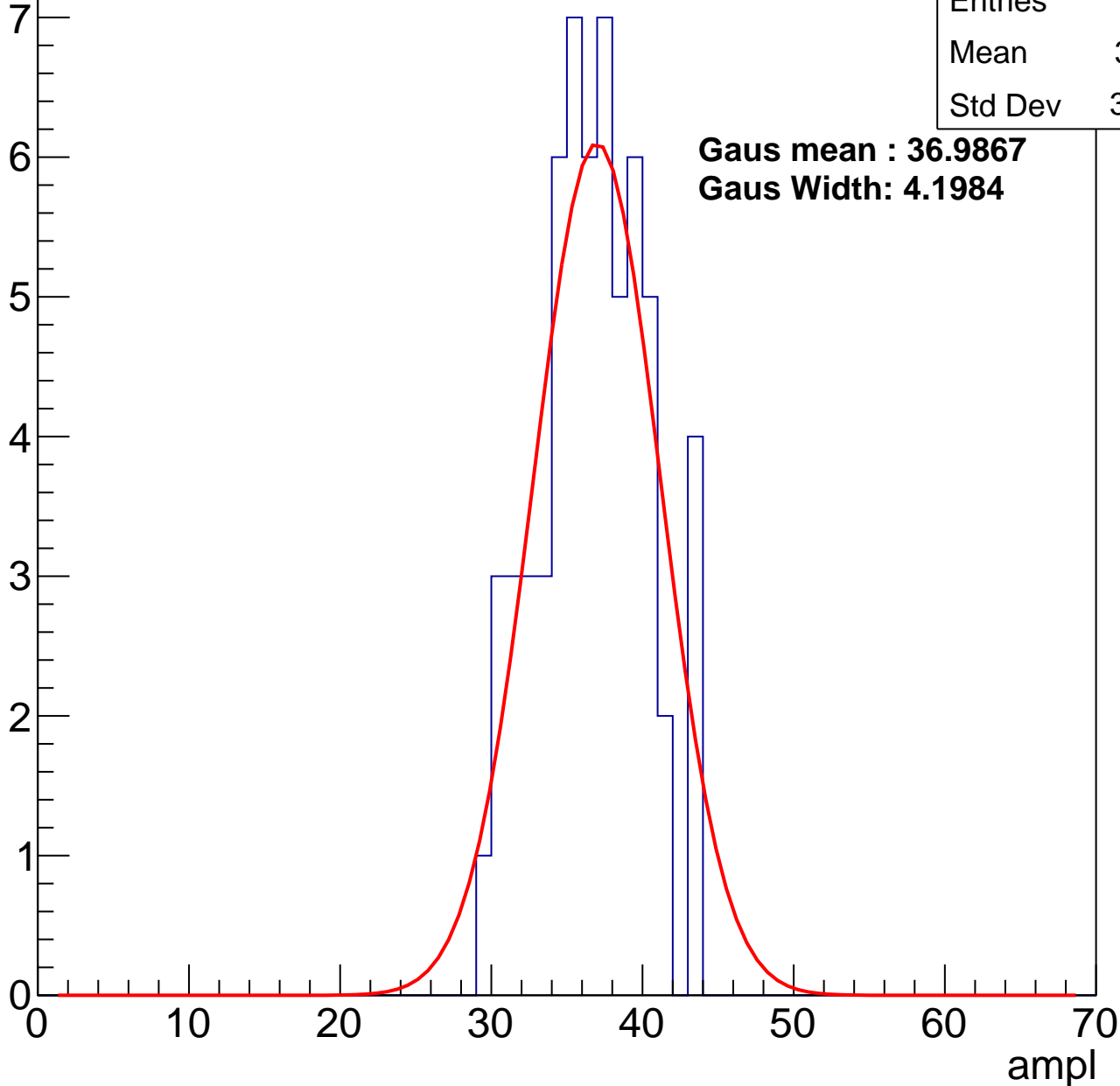
# B1L102S, U16-ch17, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	36.21
Std Dev	3.488

**Gaus mean : 36.9867**  
**Gaus Width: 4.1984**



# B1L102S, U16-ch17, adc2

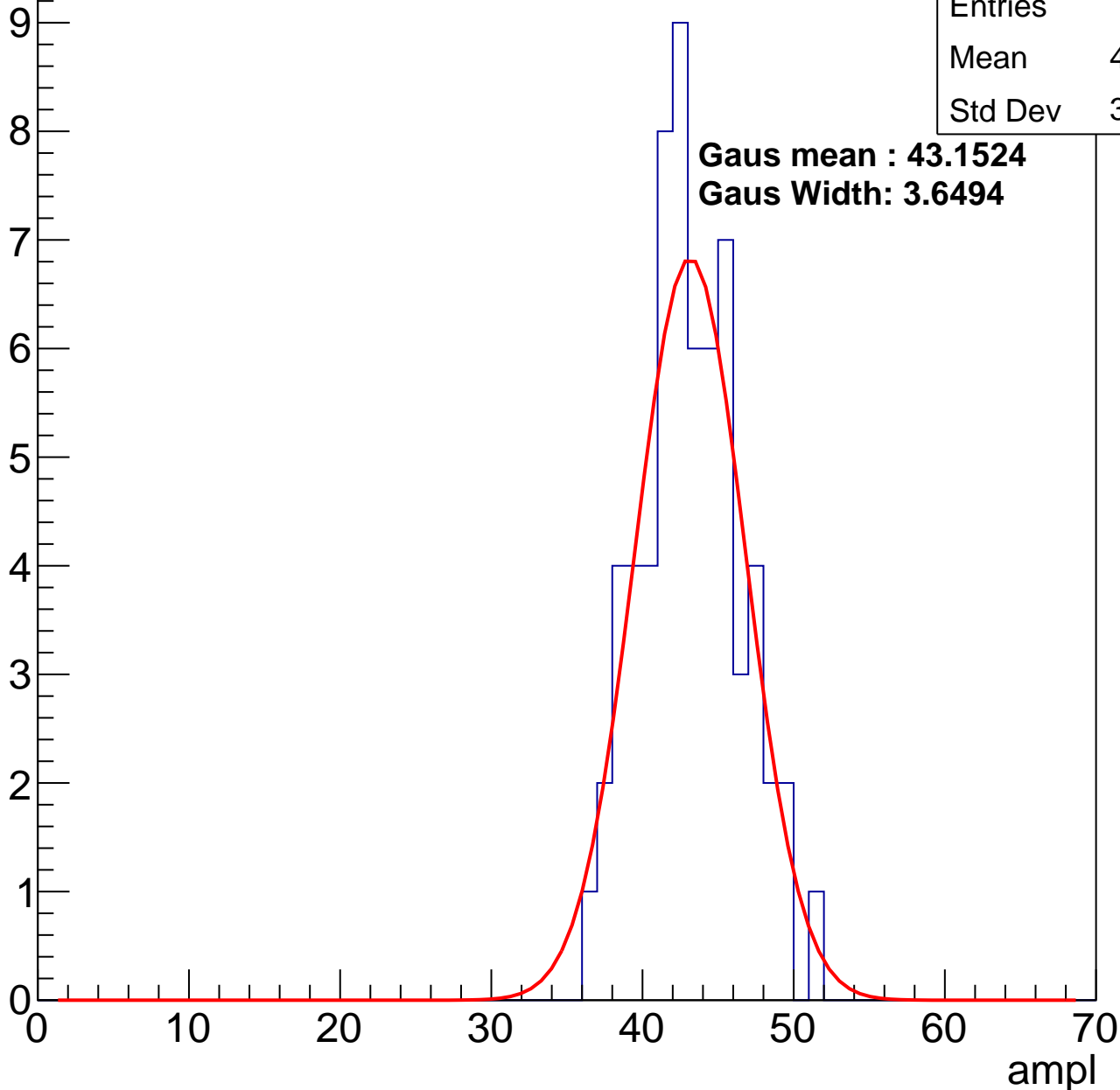
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	42.73
Std Dev	3.257

**Gaus mean : 43.1524**

**Gaus Width: 3.6494**

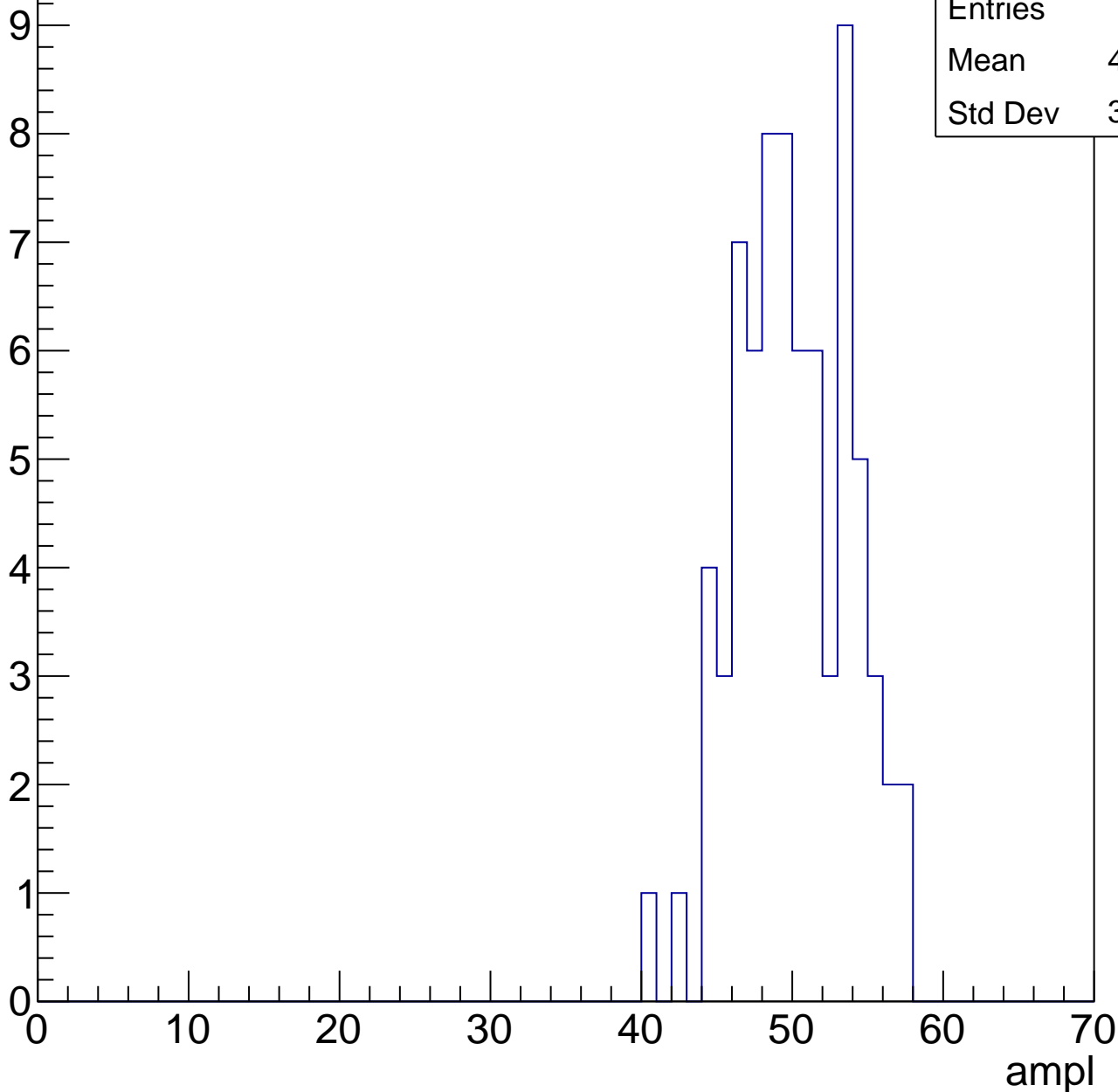


# B1L102S, U16-ch17, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	49.64
Std Dev	3.682

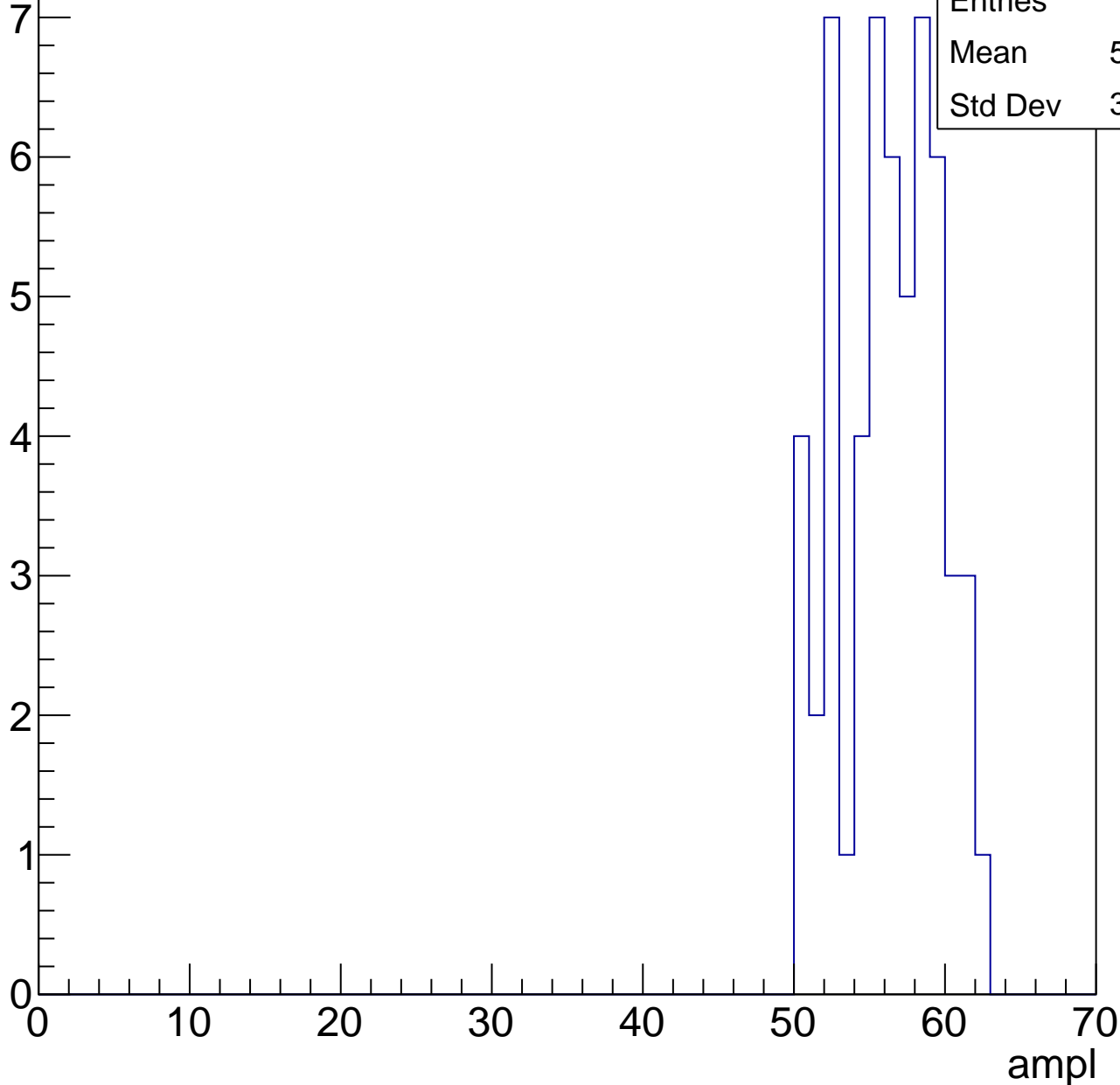


# B1L102S, U16-ch17, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	55.82
Std Dev	3.224

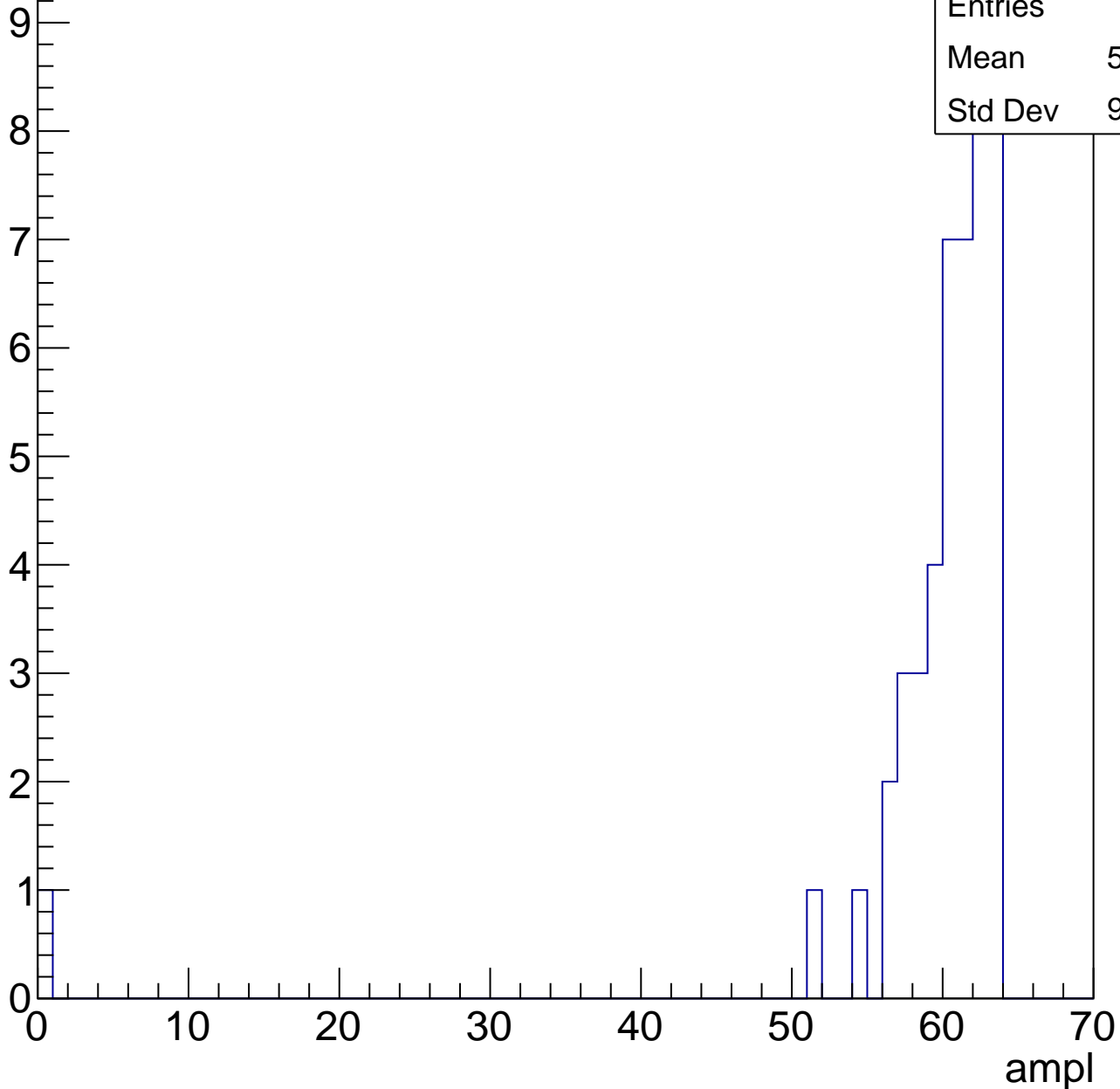


# B1L102S, U16-ch17, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	58.85
Std Dev	9.144



# B1L102S, U16-ch17, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

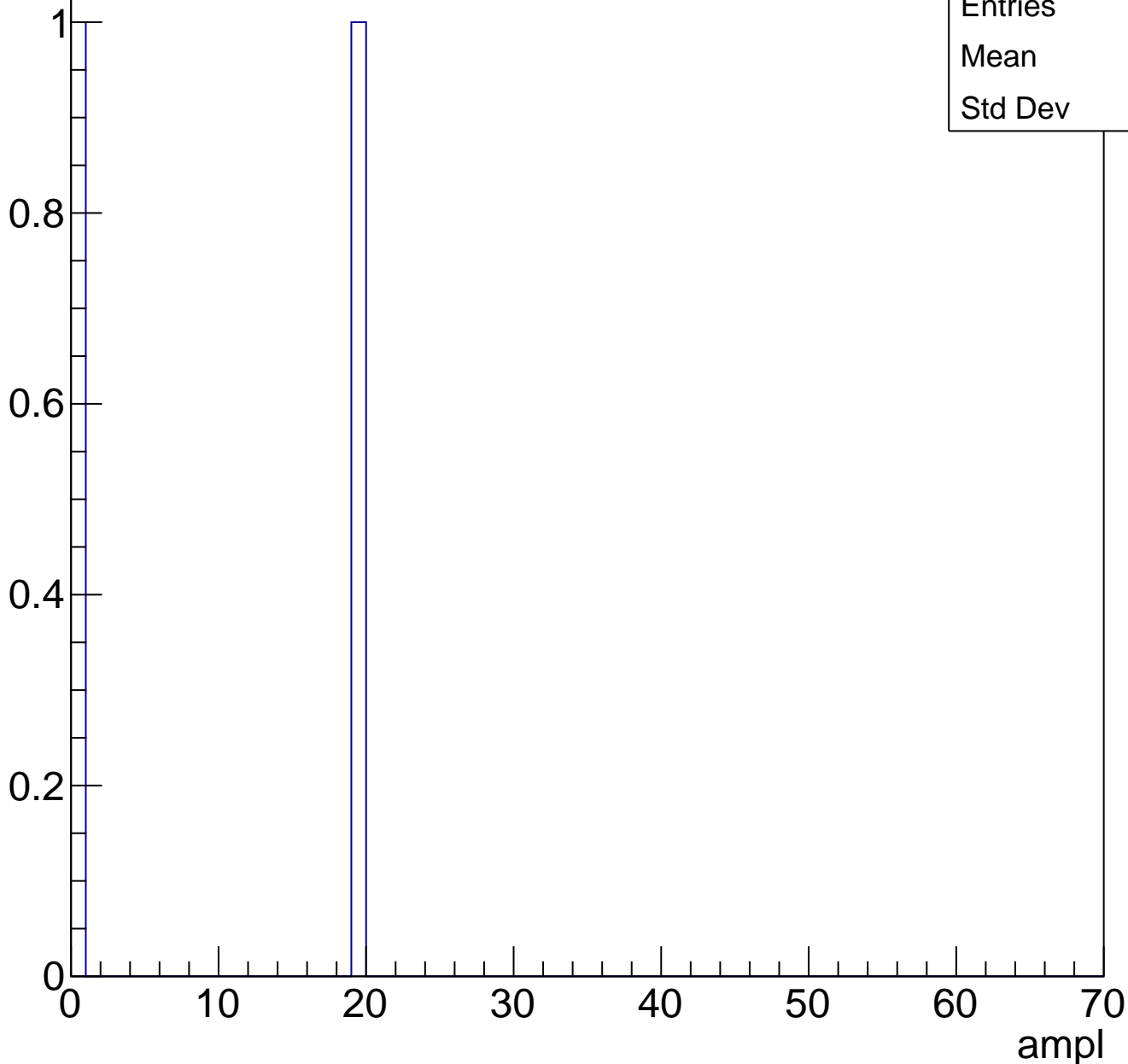




# B1L102S, U16-ch17, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	9.5
Std Dev	9.5

# B1L102S, U16-ch18, adc0

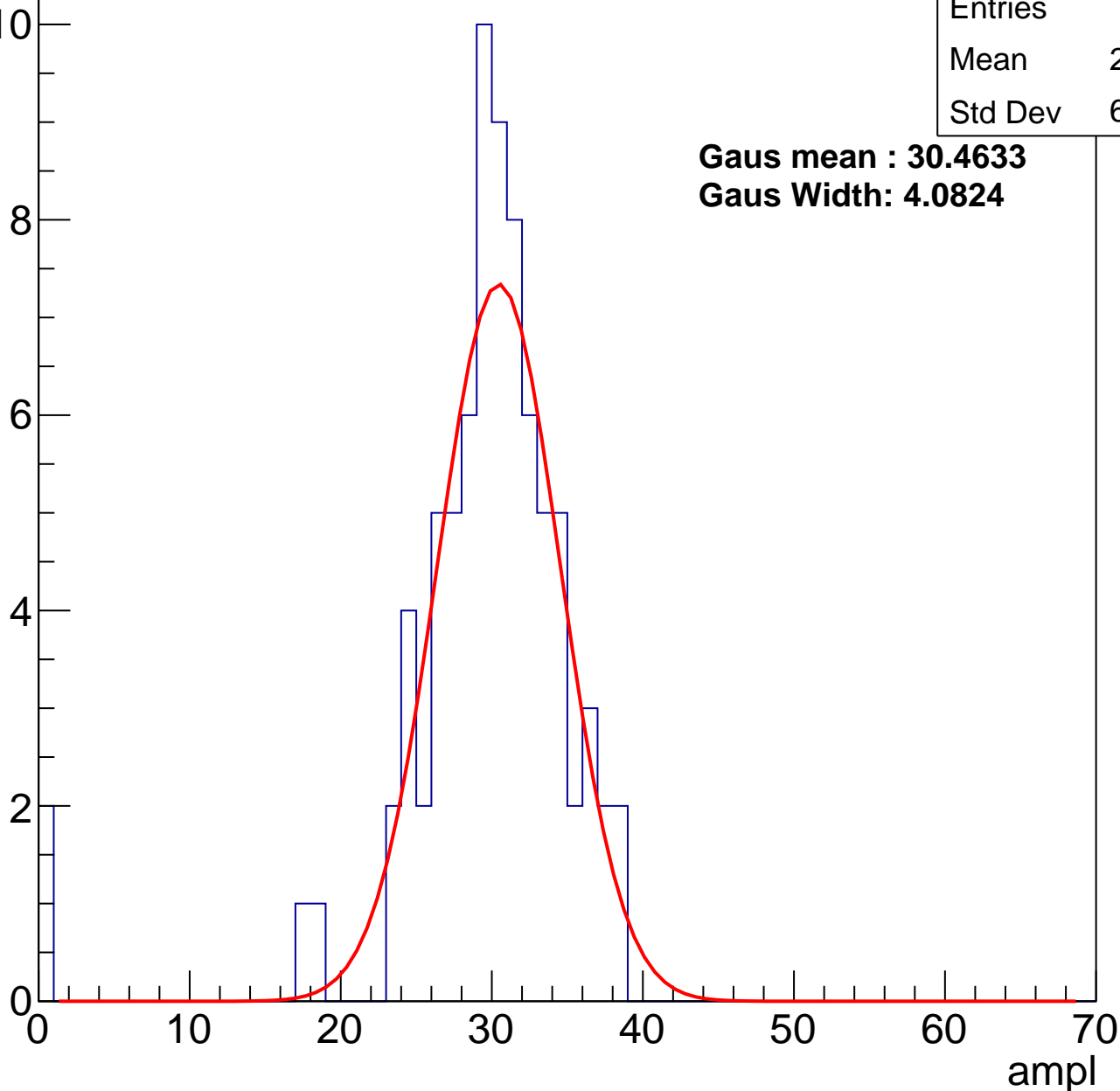
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	29.04
Std Dev	6.155

**Gaus mean : 30.4633**

**Gaus Width: 4.0824**



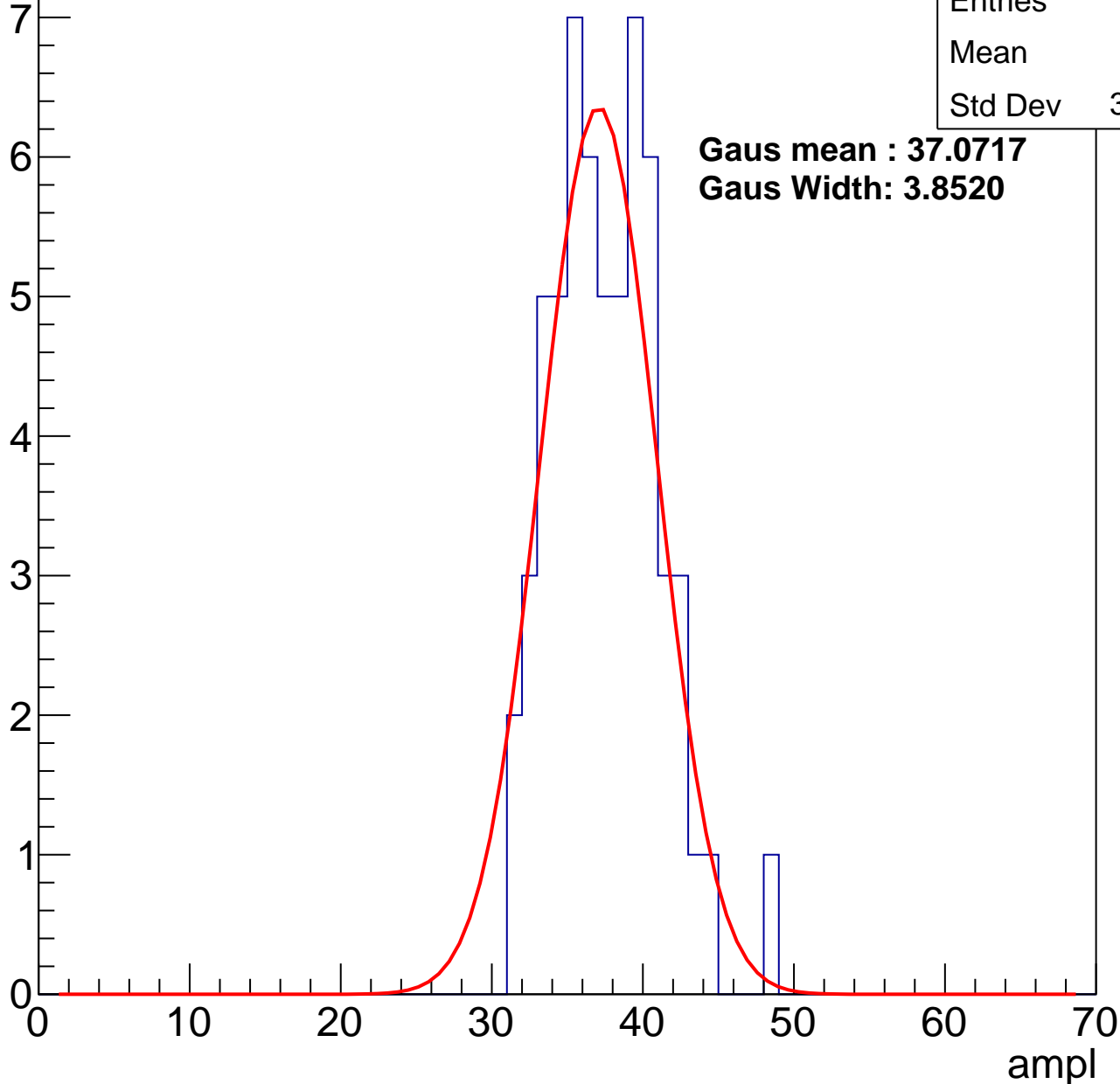
# B1L102S, U16-ch18, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	37.1
Std Dev	3.467

**Gaus mean : 37.0717**  
**Gaus Width: 3.8520**



# B1L102S, U16-ch18, adc2

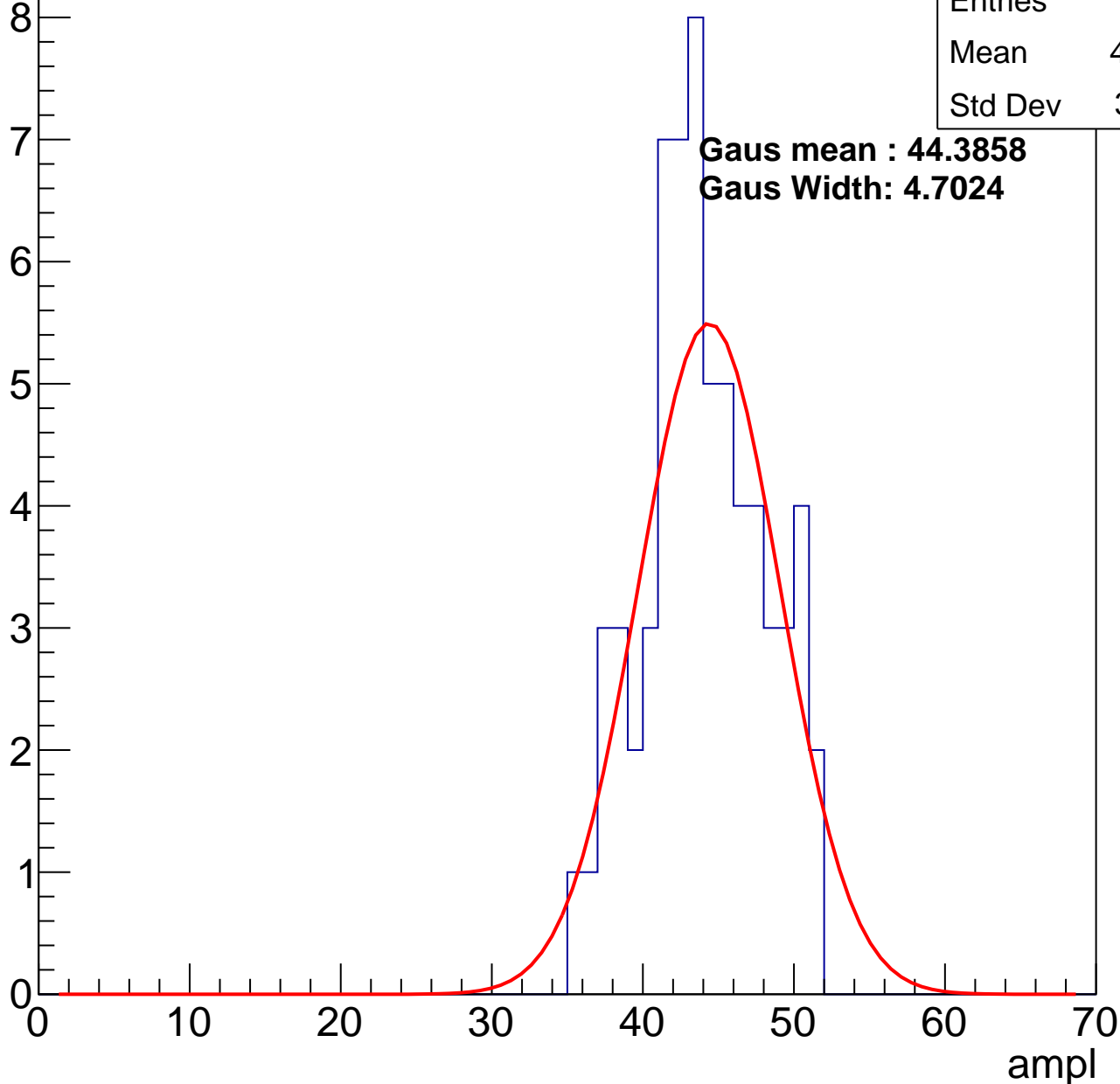
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	43.52
Std Dev	3.931

**Gaus mean : 44.3858**

**Gaus Width: 4.7024**

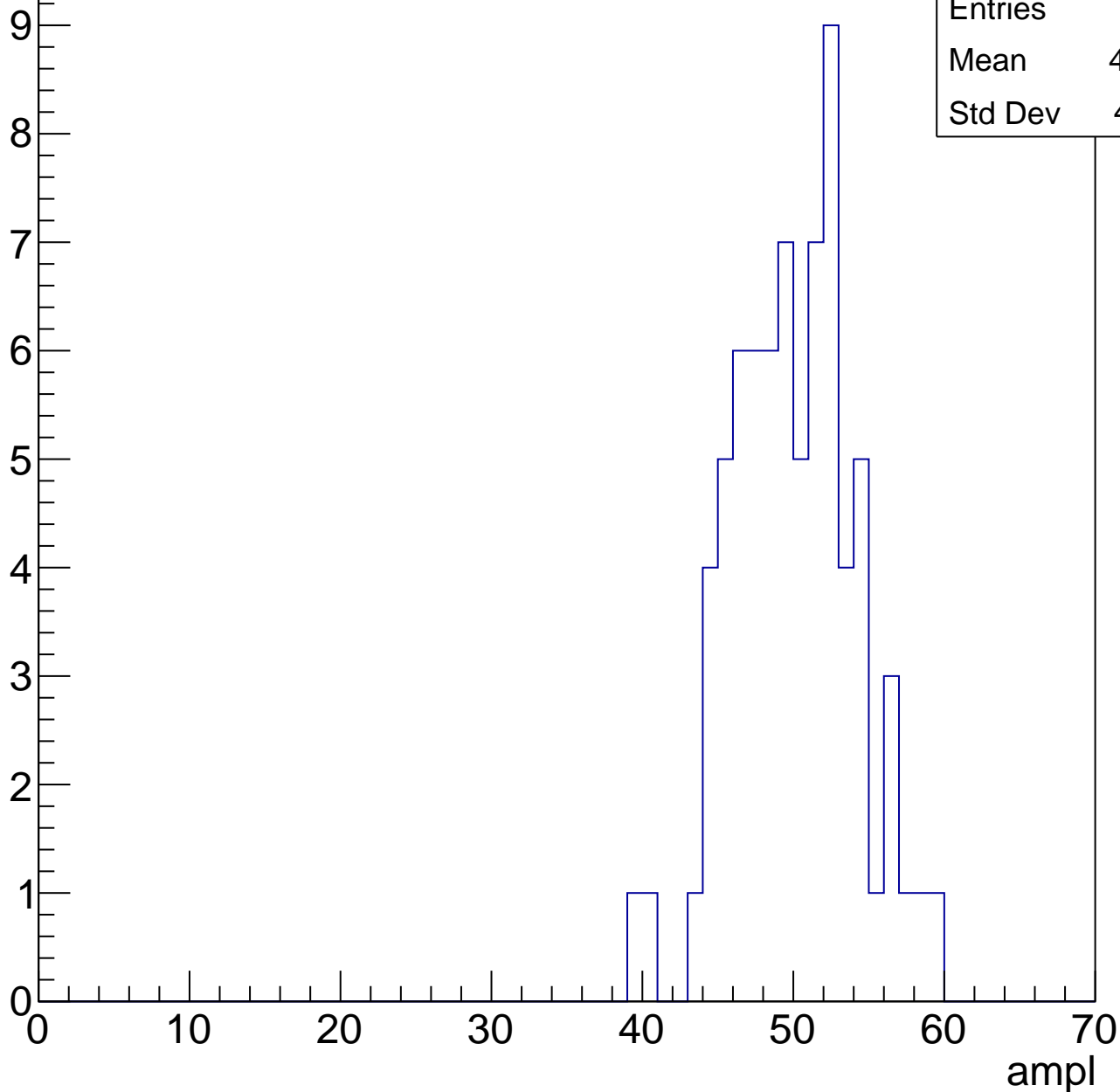


# B1L102S, U16-ch18, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	49.54
Std Dev	4.011

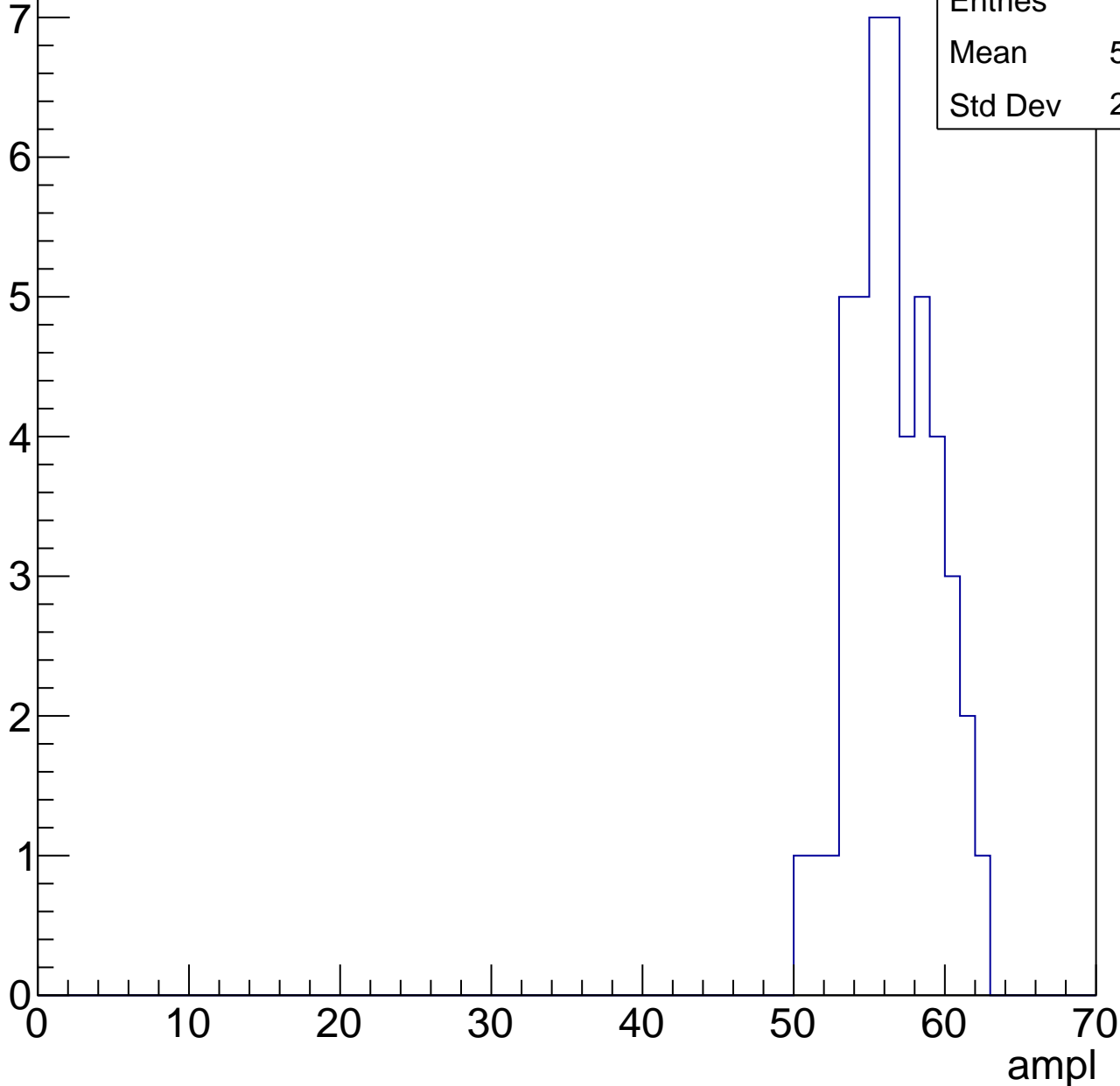


# B1L102S, U16-ch18, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	46
Mean	56.15
Std Dev	2.726

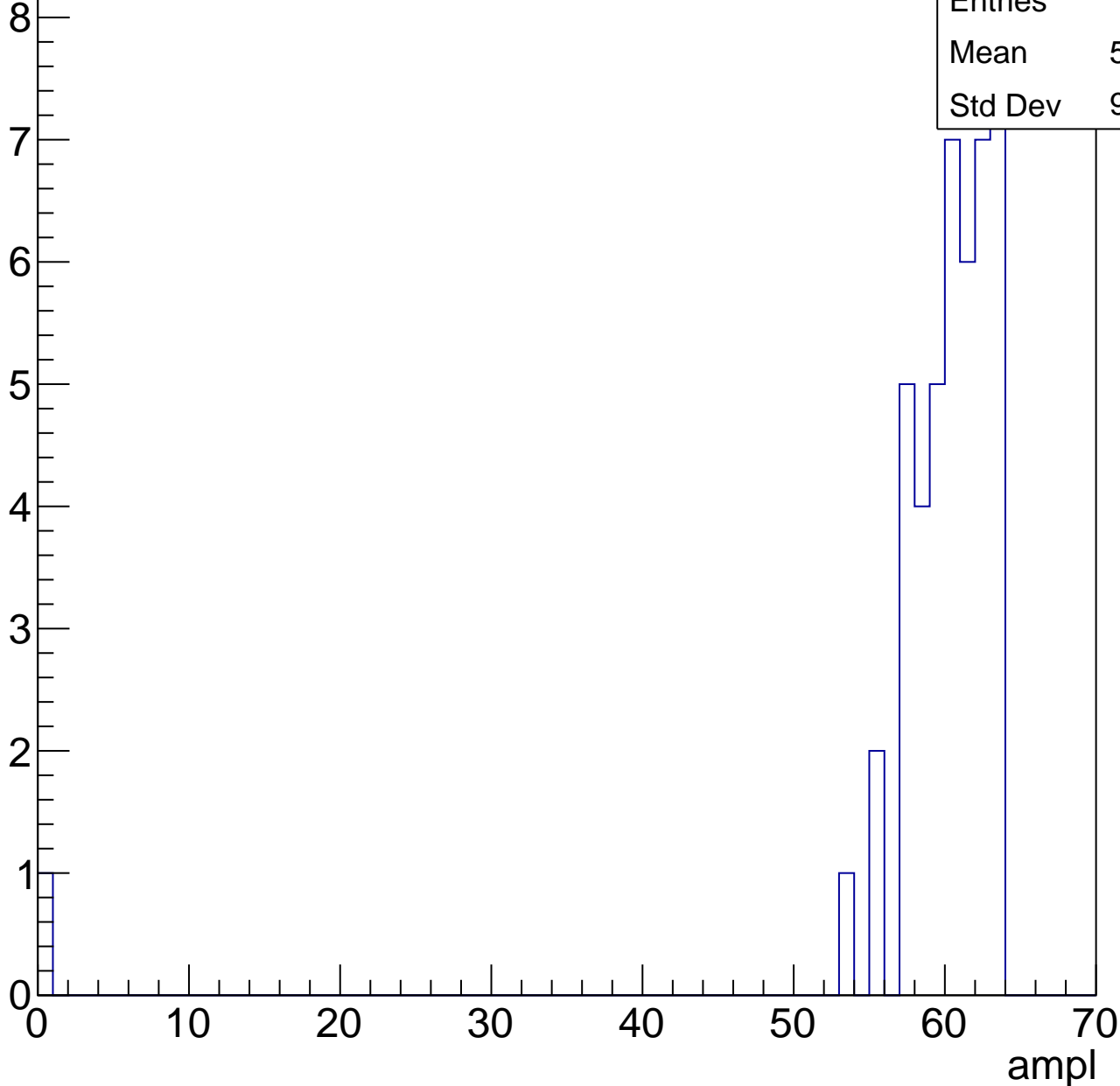


# B1L102S, U16-ch18, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

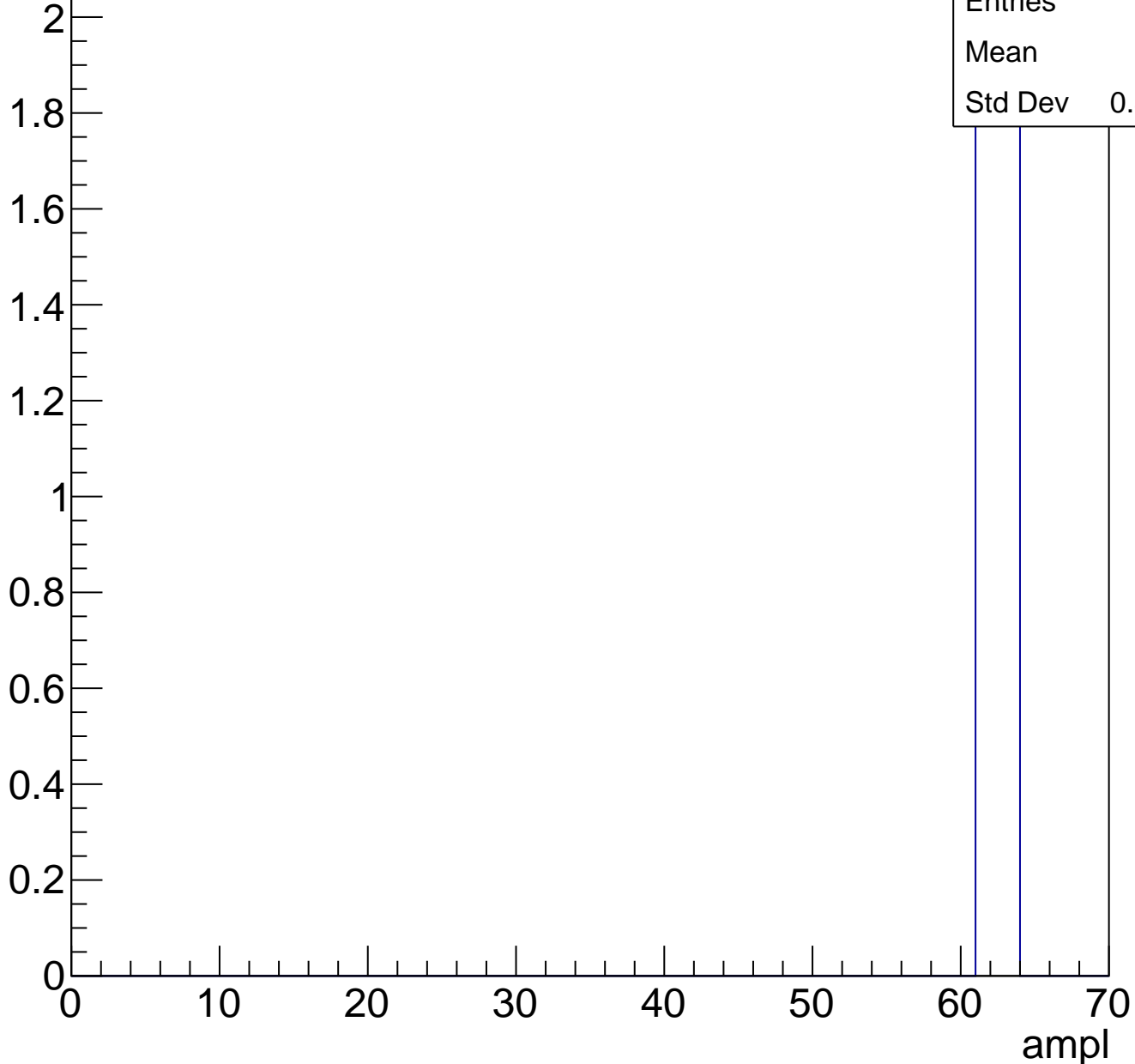
Entries	46
Mean	58.67
Std Dev	9.077



# B1L102S, U16-ch18, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

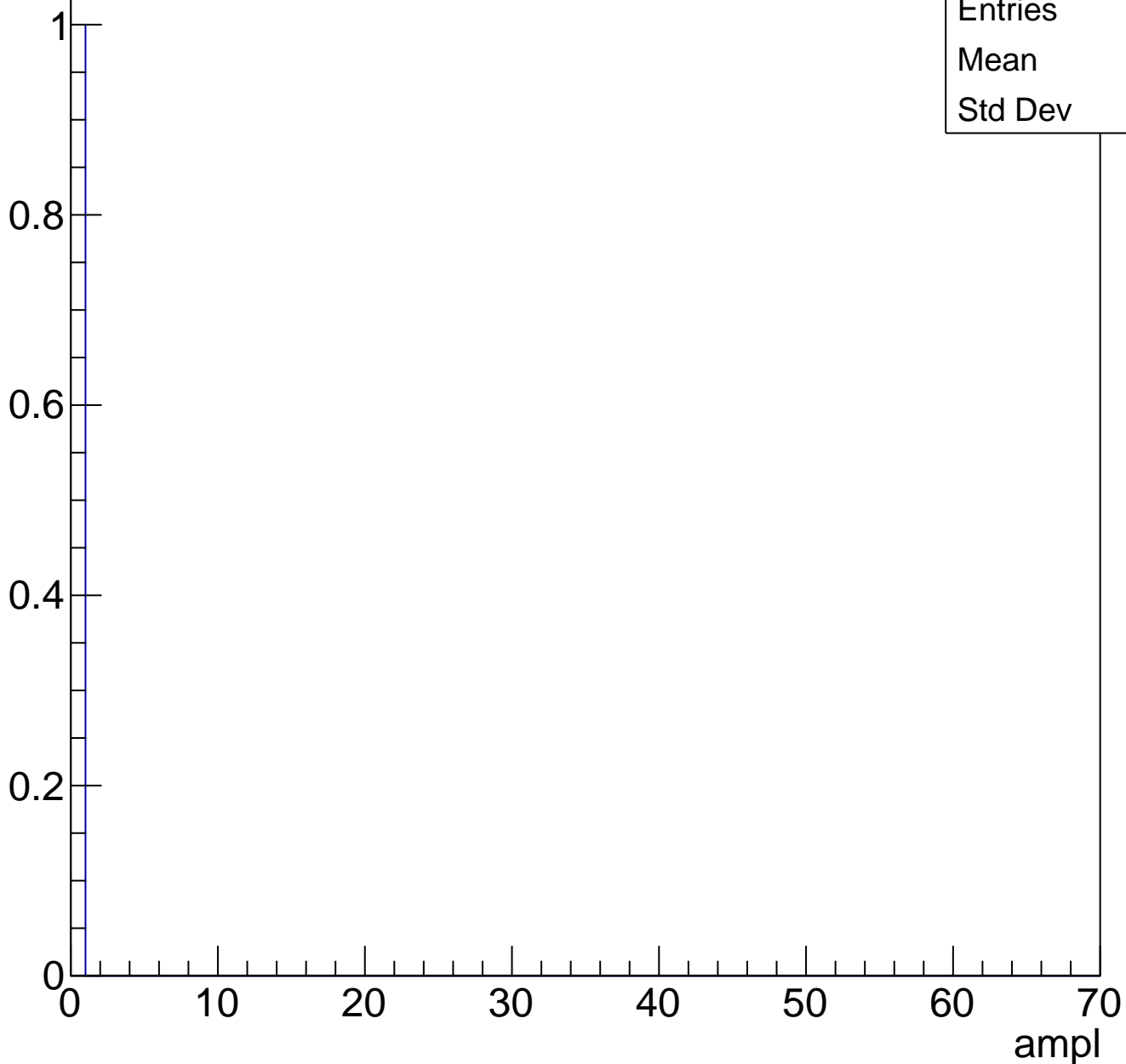




# B1L102S, U16-ch18, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch19, adc0

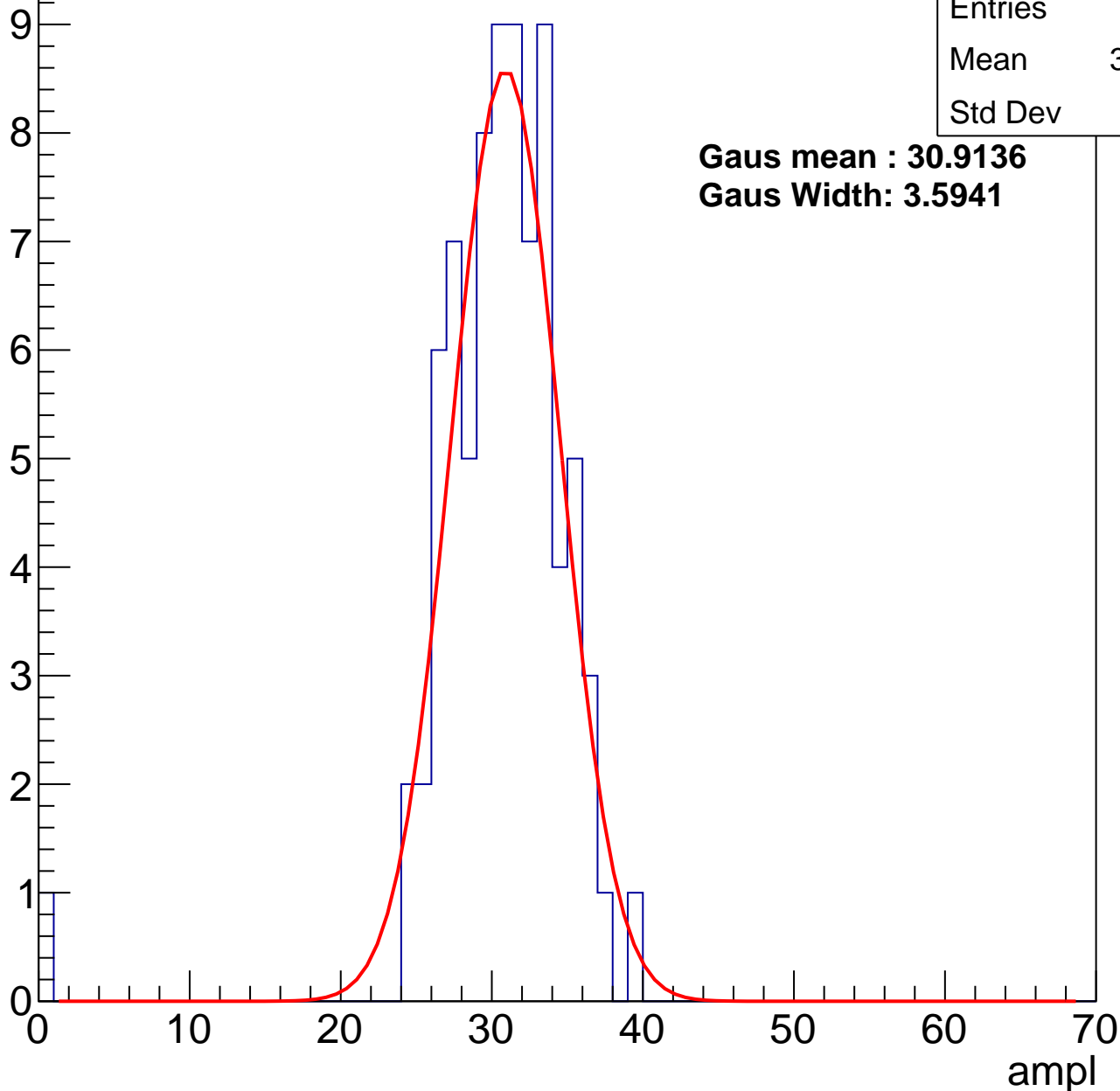
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	30.13
Std Dev	4.71

**Gaus mean : 30.9136**

**Gaus Width: 3.5941**



# B1L102S, U16-ch19, adc1

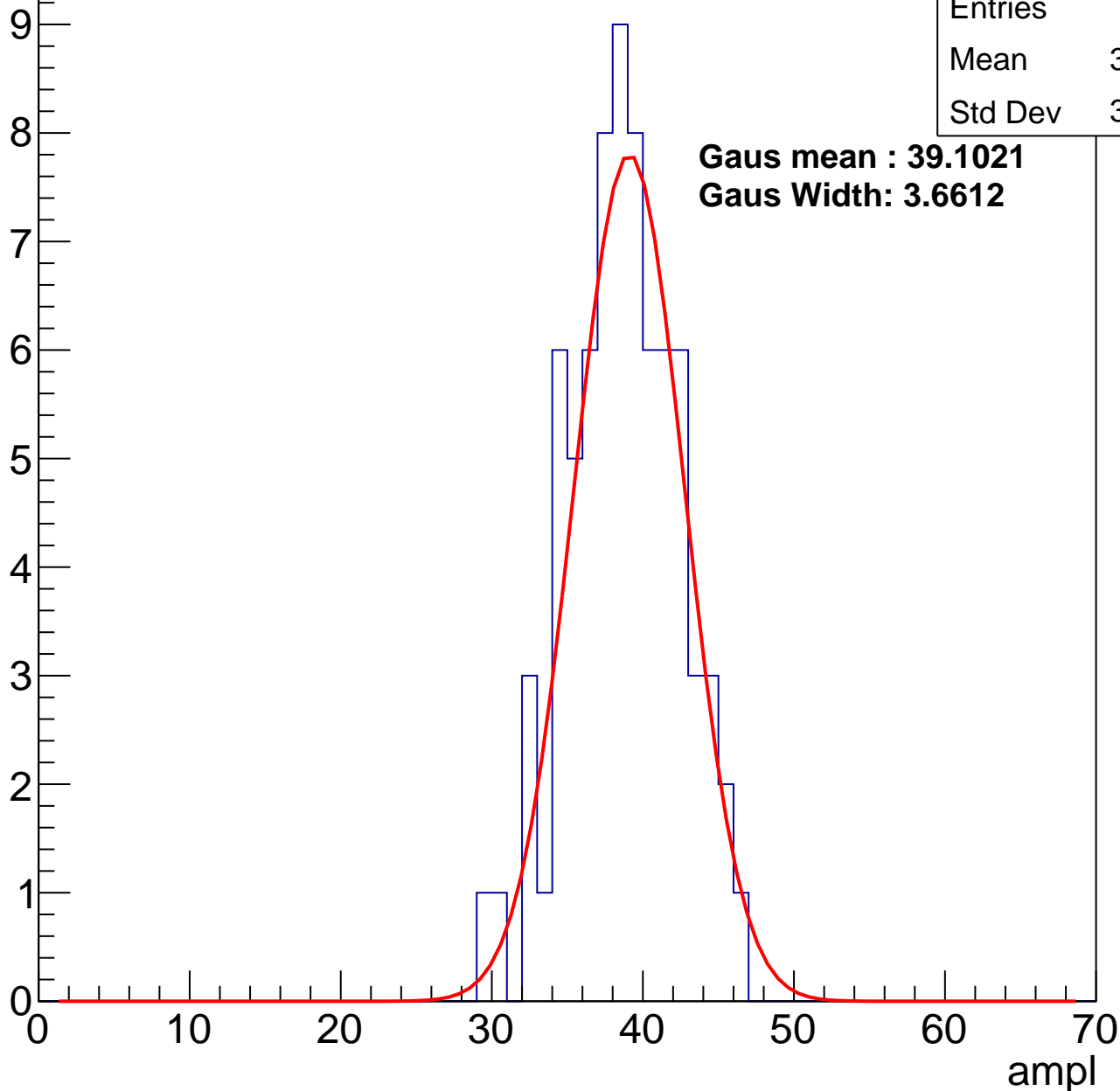
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	38.24
Std Dev	3.603

**Gaus mean : 39.1021**

**Gaus Width: 3.6612**



# B1L102S, U16-ch19, adc2

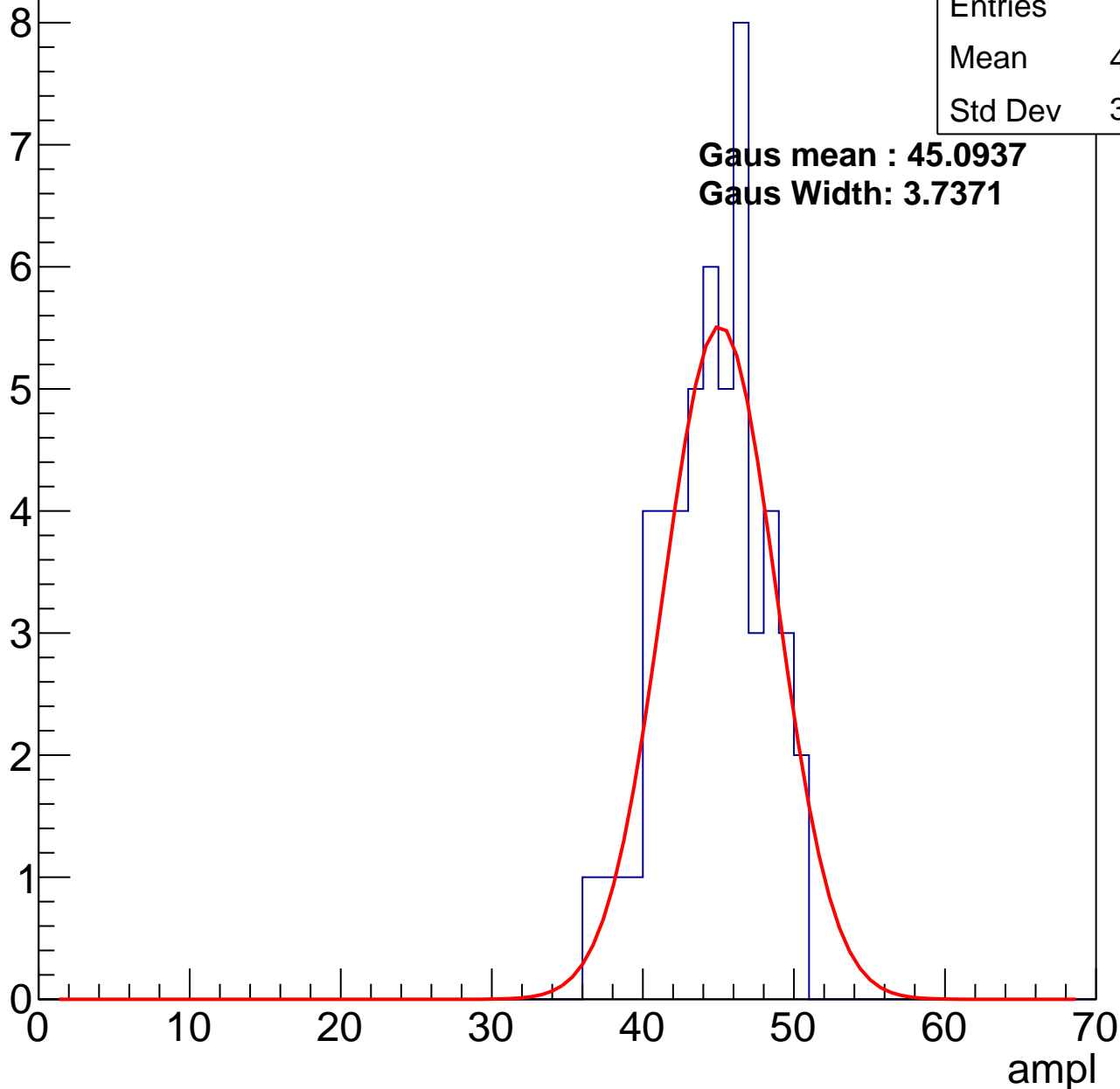
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	44.12
Std Dev	3.309

**Gaus mean : 45.0937**

**Gaus Width: 3.7371**

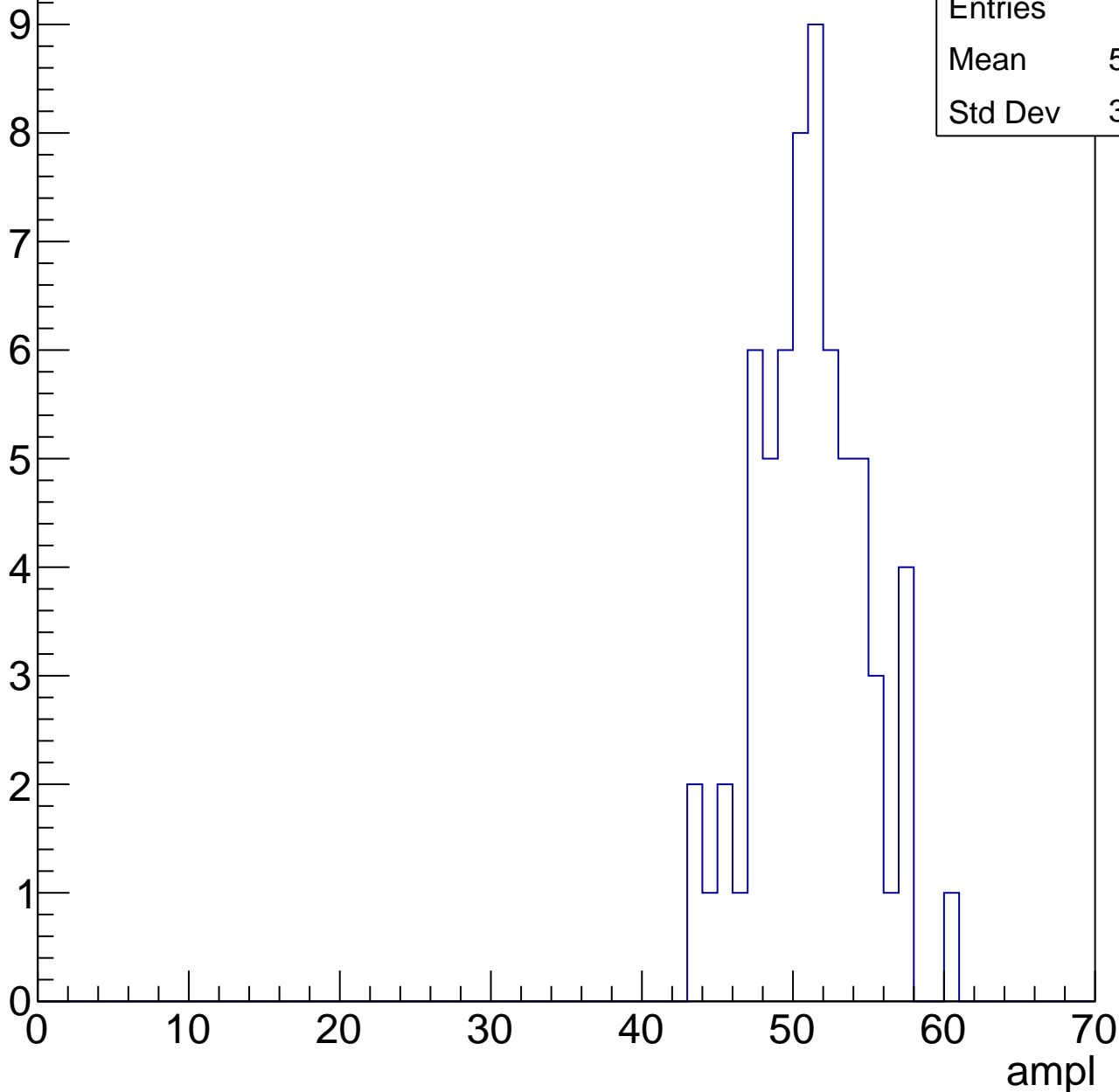


# B1L102S, U16-ch19, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	50.72
Std Dev	3.532

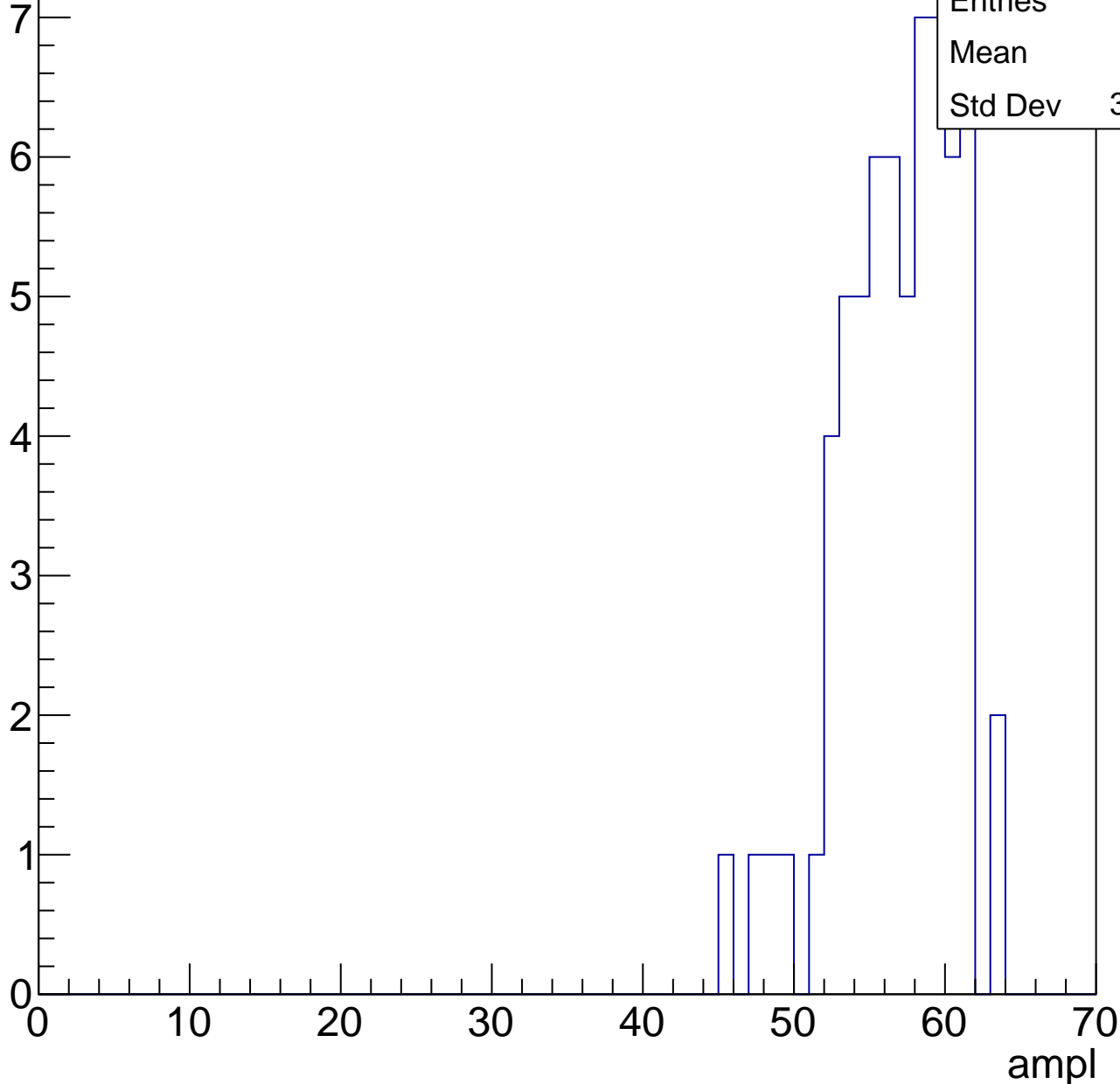


# B1L102S, U16-ch19, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	56.4
Std Dev	3.782

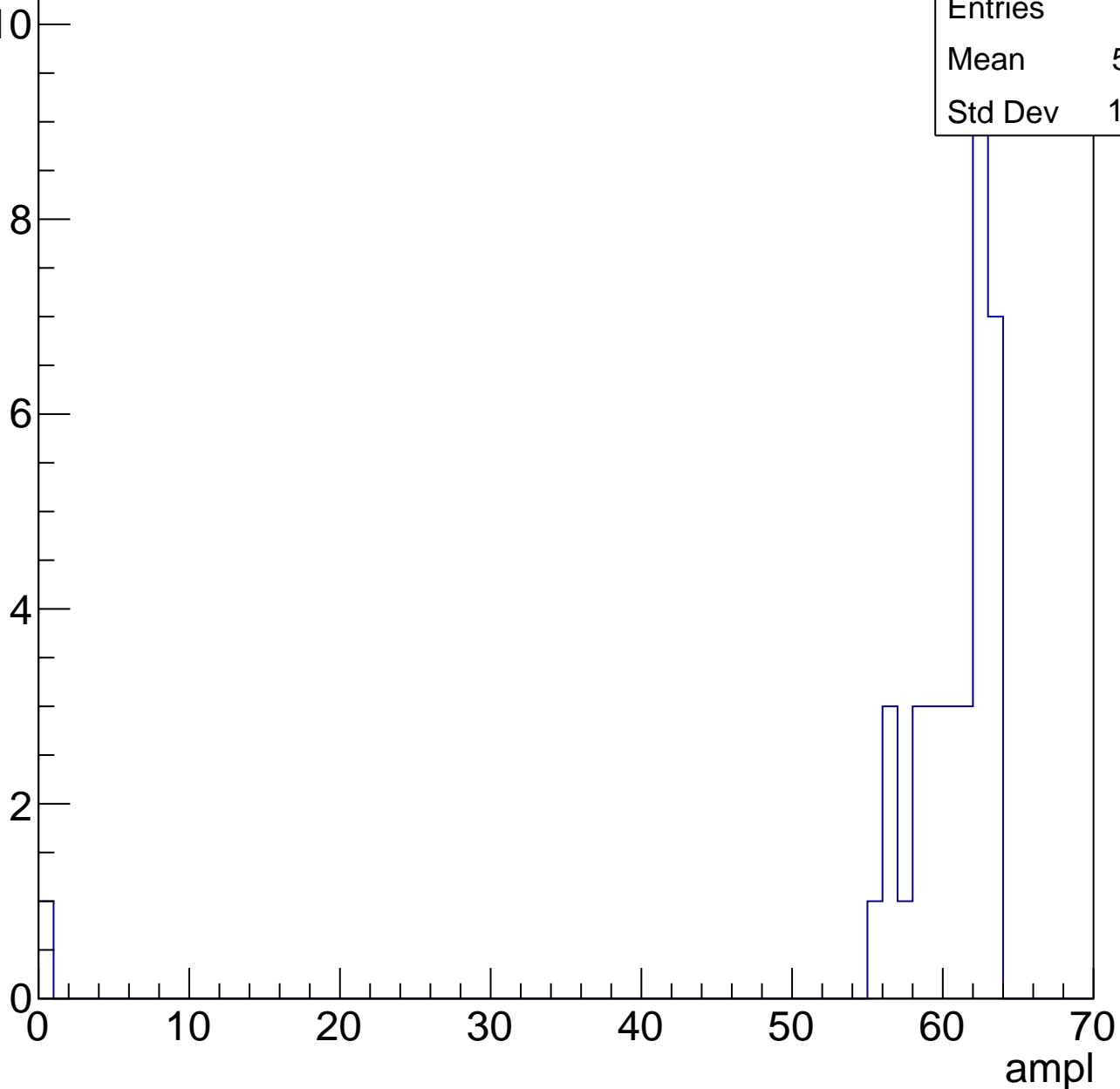


# B1L102S, U16-ch19, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	35
Mean	58.71
Std Dev	10.34



# B1L102S, U16-ch19, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	63
Std Dev	0



# B1L102S, U16-ch19, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U16-ch20, adc0

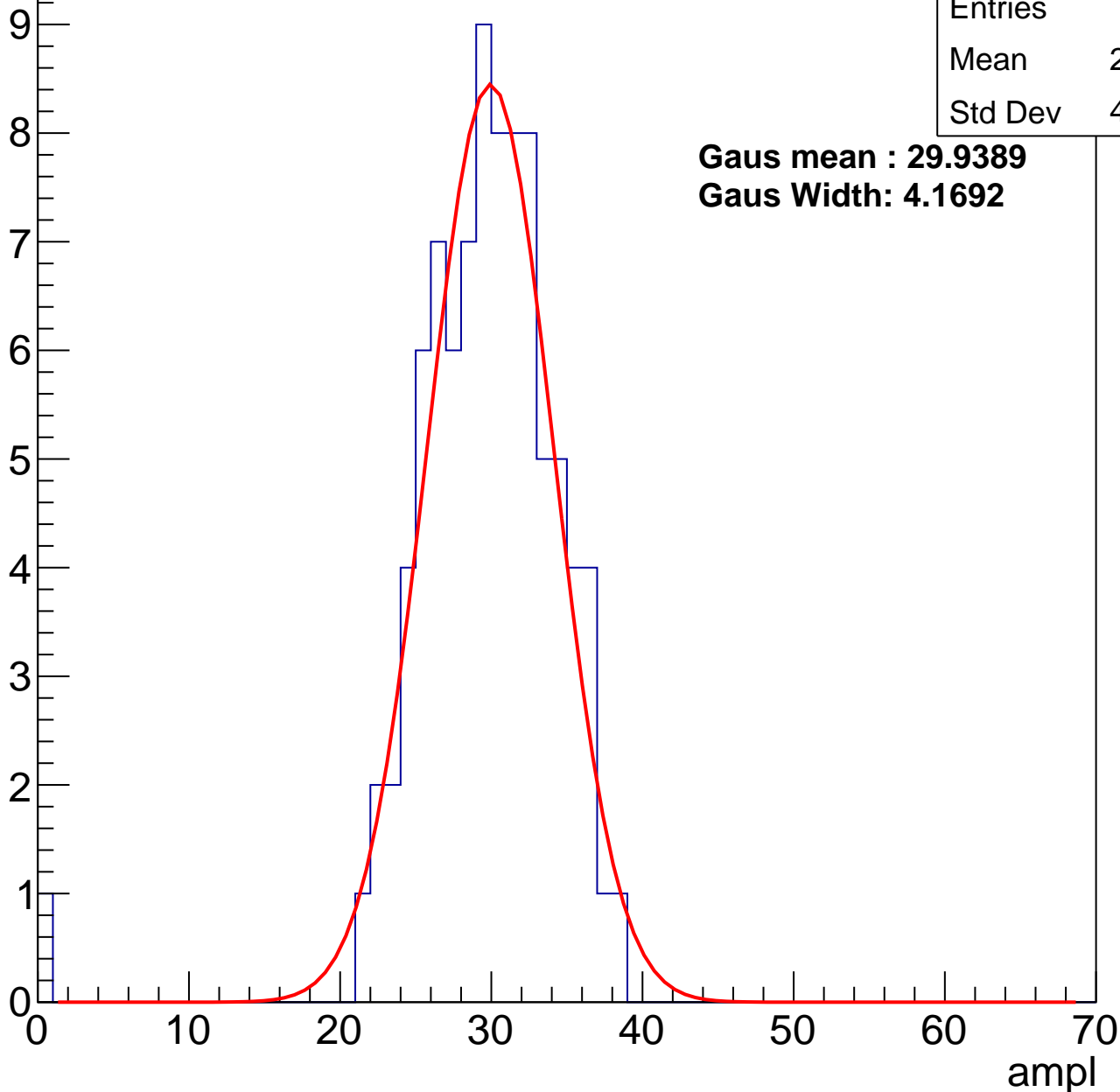
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	89
Mean	29.17
Std Dev	4.932

**Gaus mean : 29.9389**

**Gaus Width: 4.1692**



# B1L102S, U16-ch20, adc1

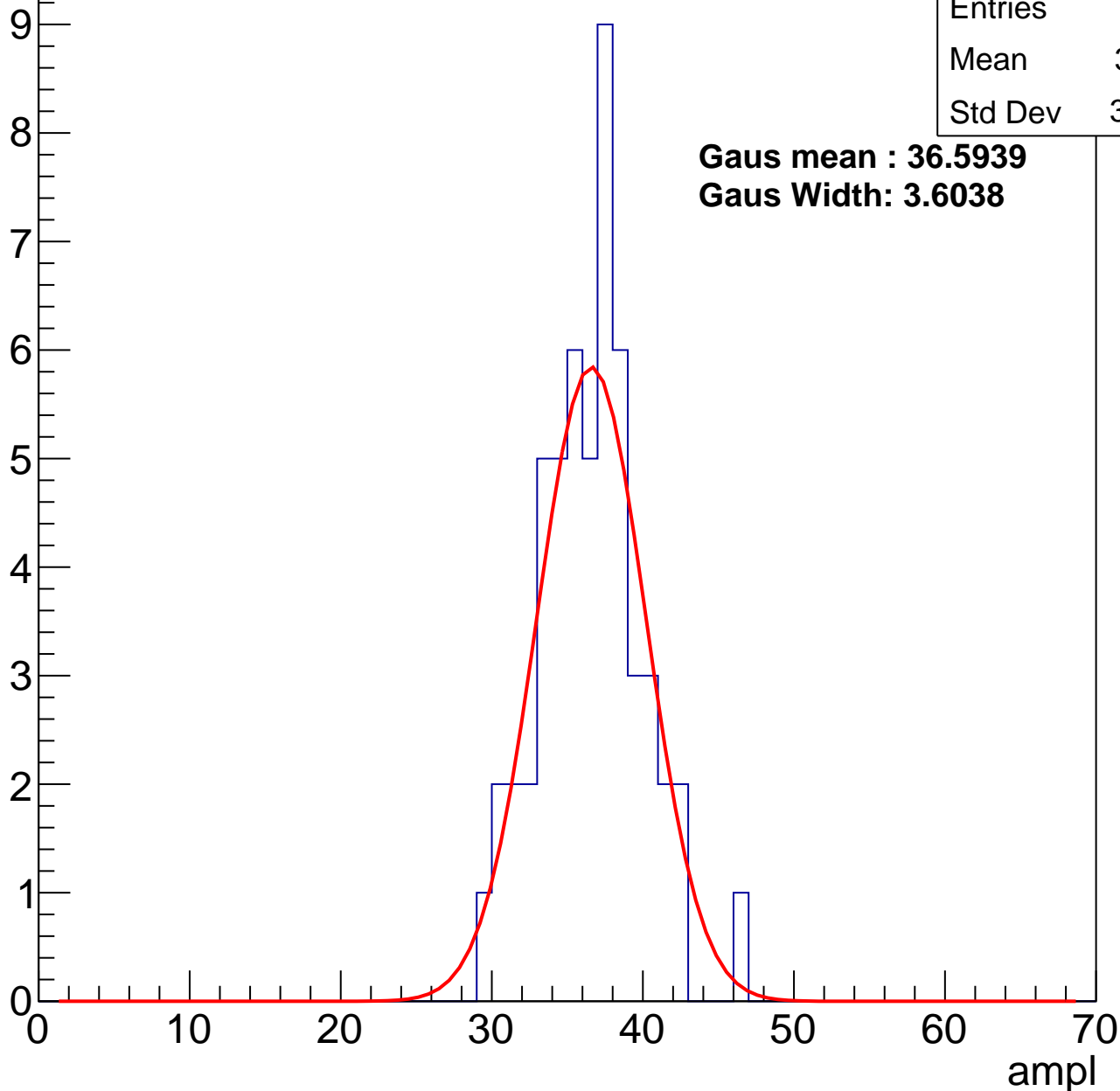
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	36.11
Std Dev	3.343

**Gaus mean : 36.5939**

**Gaus Width: 3.6038**



# B1L102S, U16-ch20, adc2

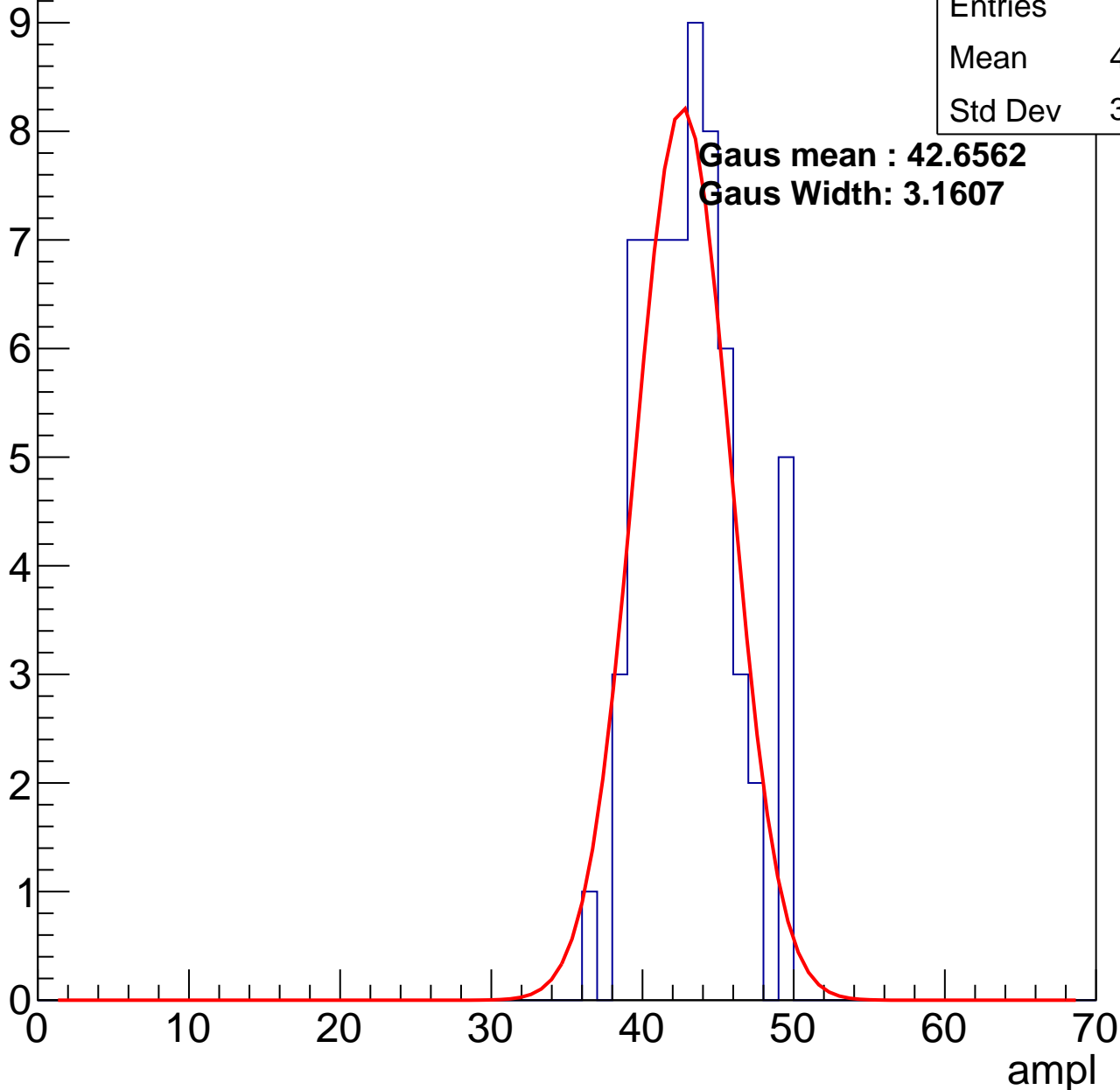
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	42.62
Std Dev	3.027

**Gaus mean : 42.6562**

**Gaus Width: 3.1607**



# B1L102S, U16-ch20, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

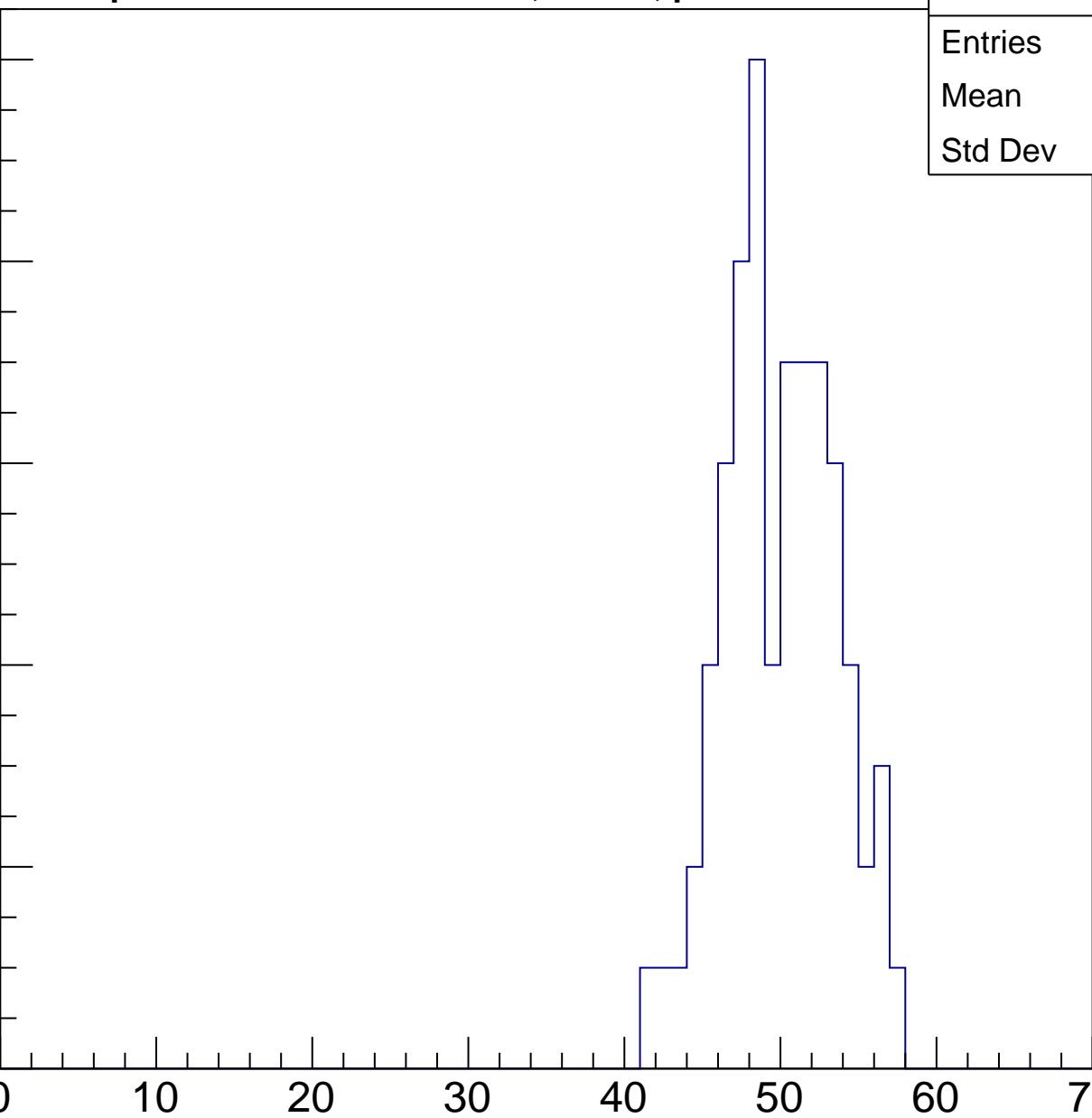
Entries	74
Mean	49.49
Std Dev	3.523

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

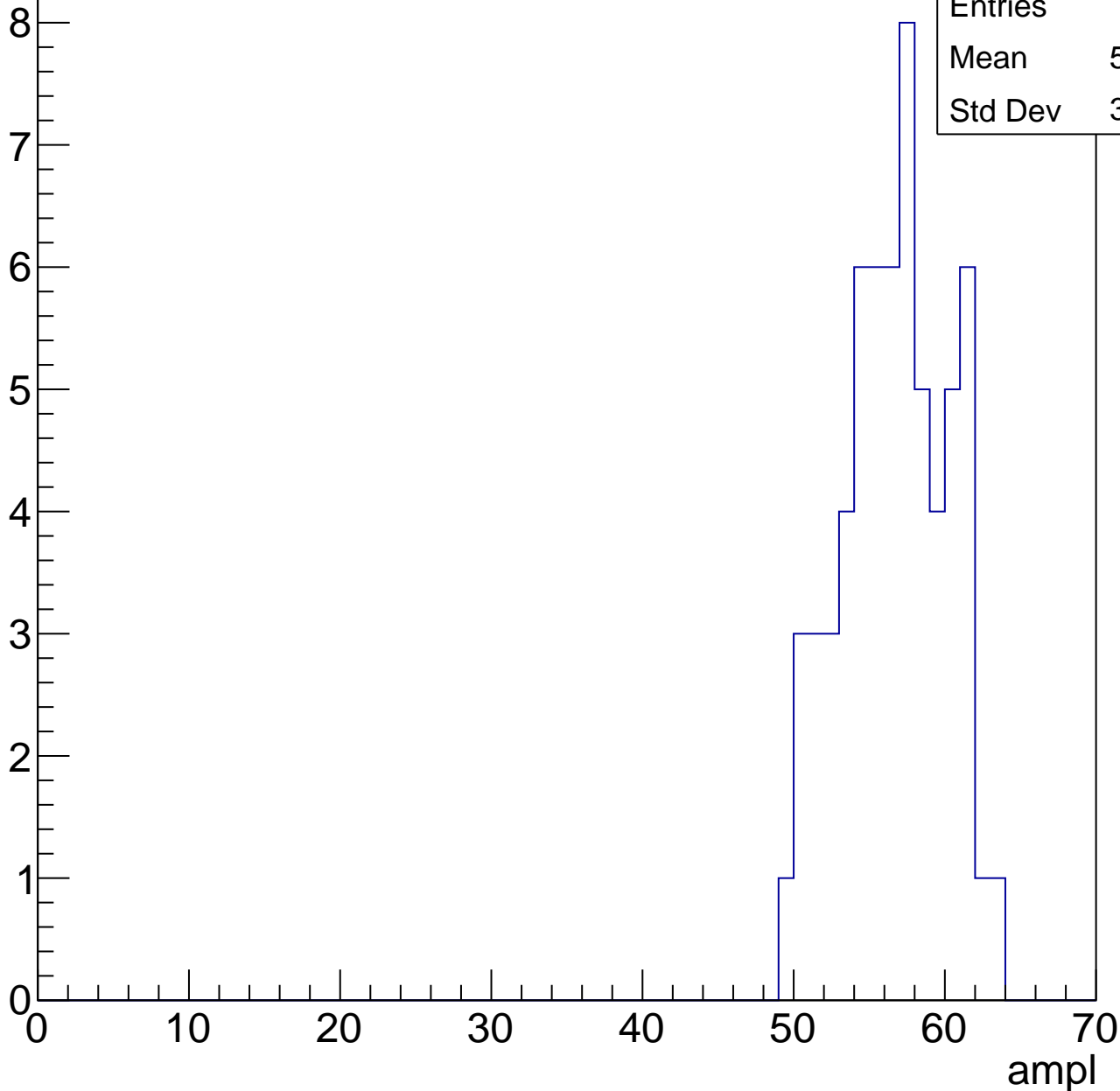


# B1L102S, U16-ch20, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	56.18
Std Dev	3.415

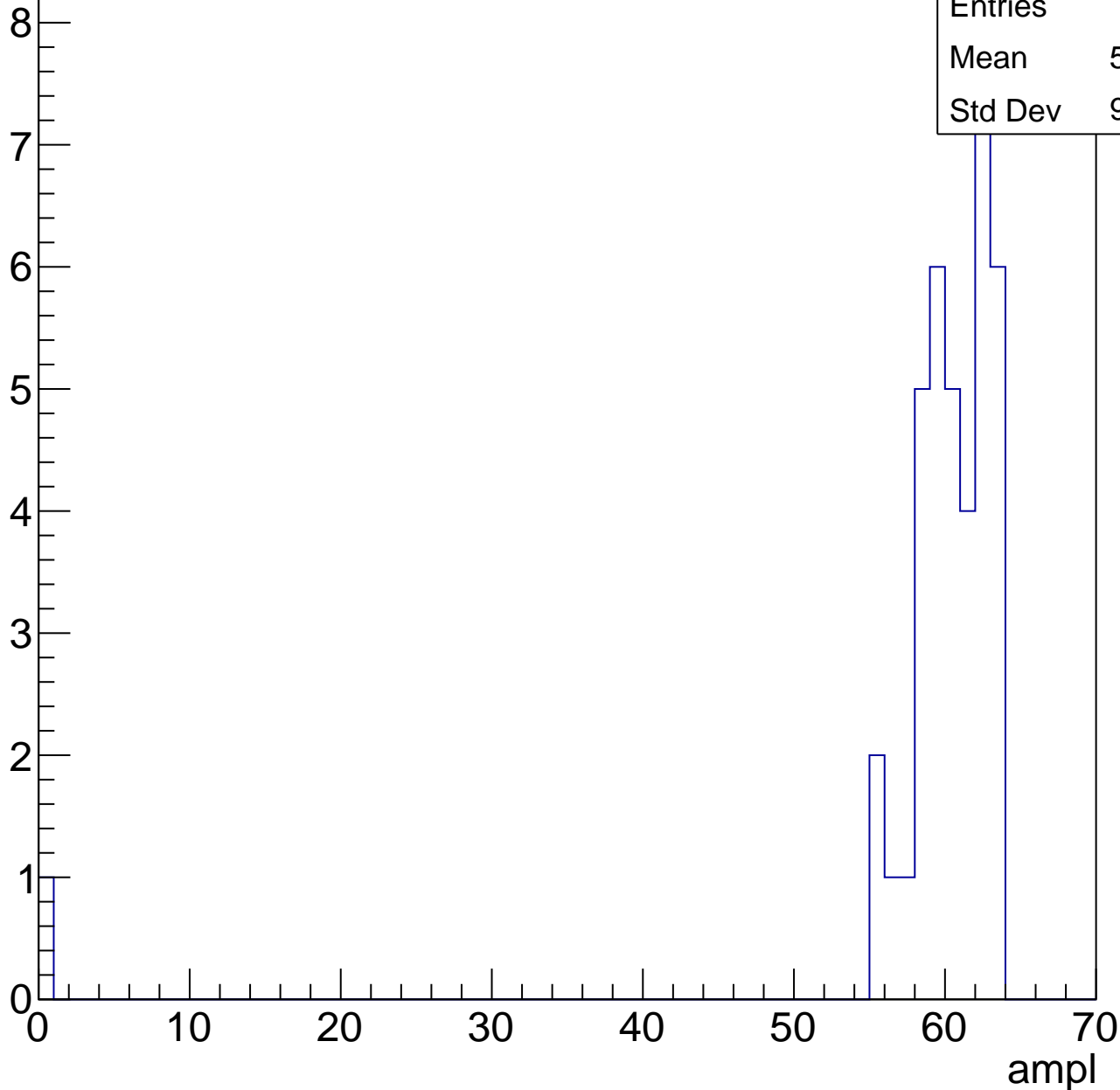


# B1L102S, U16-ch20, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	39
Mean	58.59
Std Dev	9.758



# B1L102S, U16-ch20, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch20, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U16-ch21, adc0

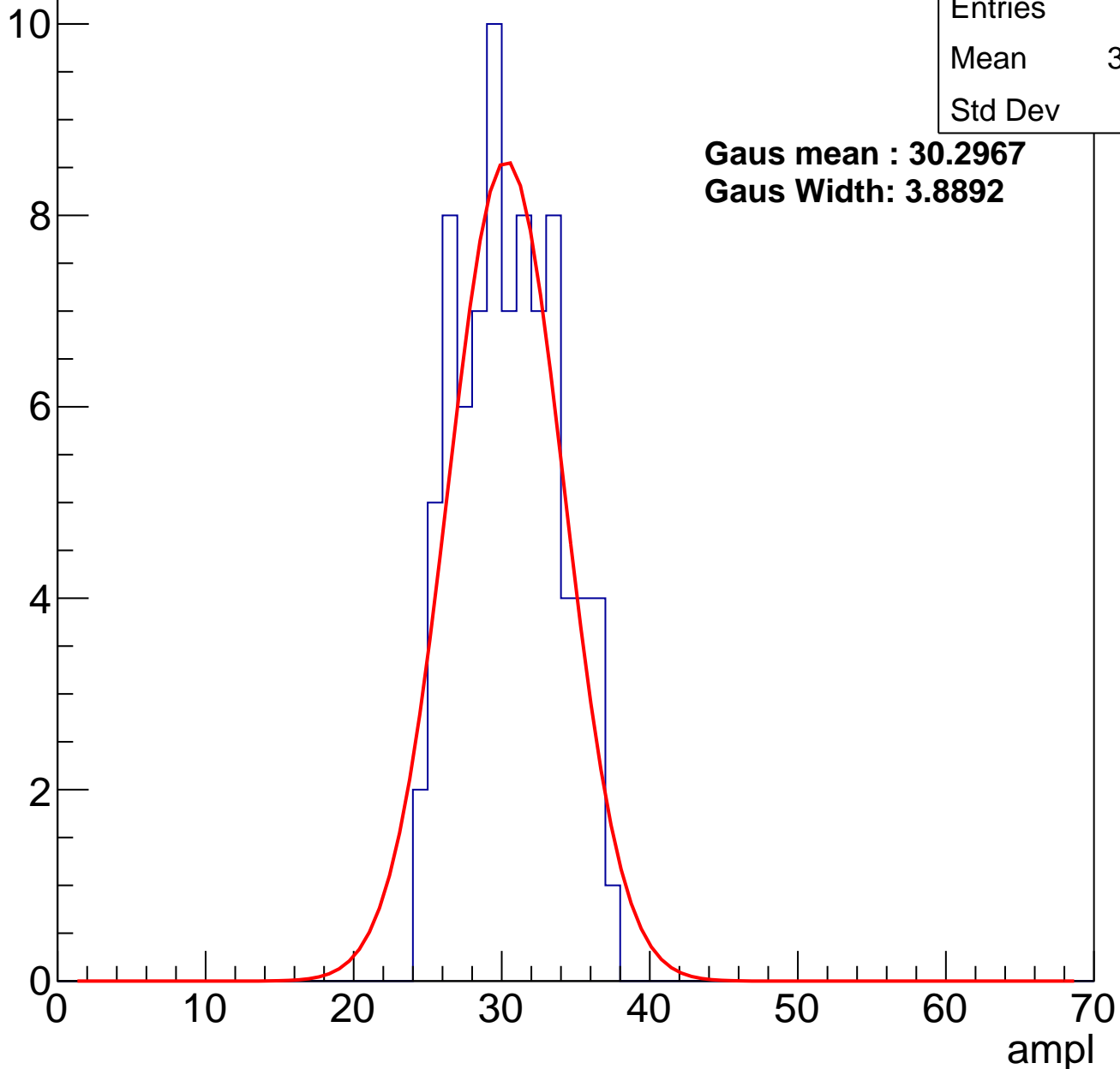
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	81
Mean	30.02
Std Dev	3.3

**Gaus mean : 30.2967**

**Gaus Width: 3.8892**

Entry



# B1L102S, U16-ch21, adc1

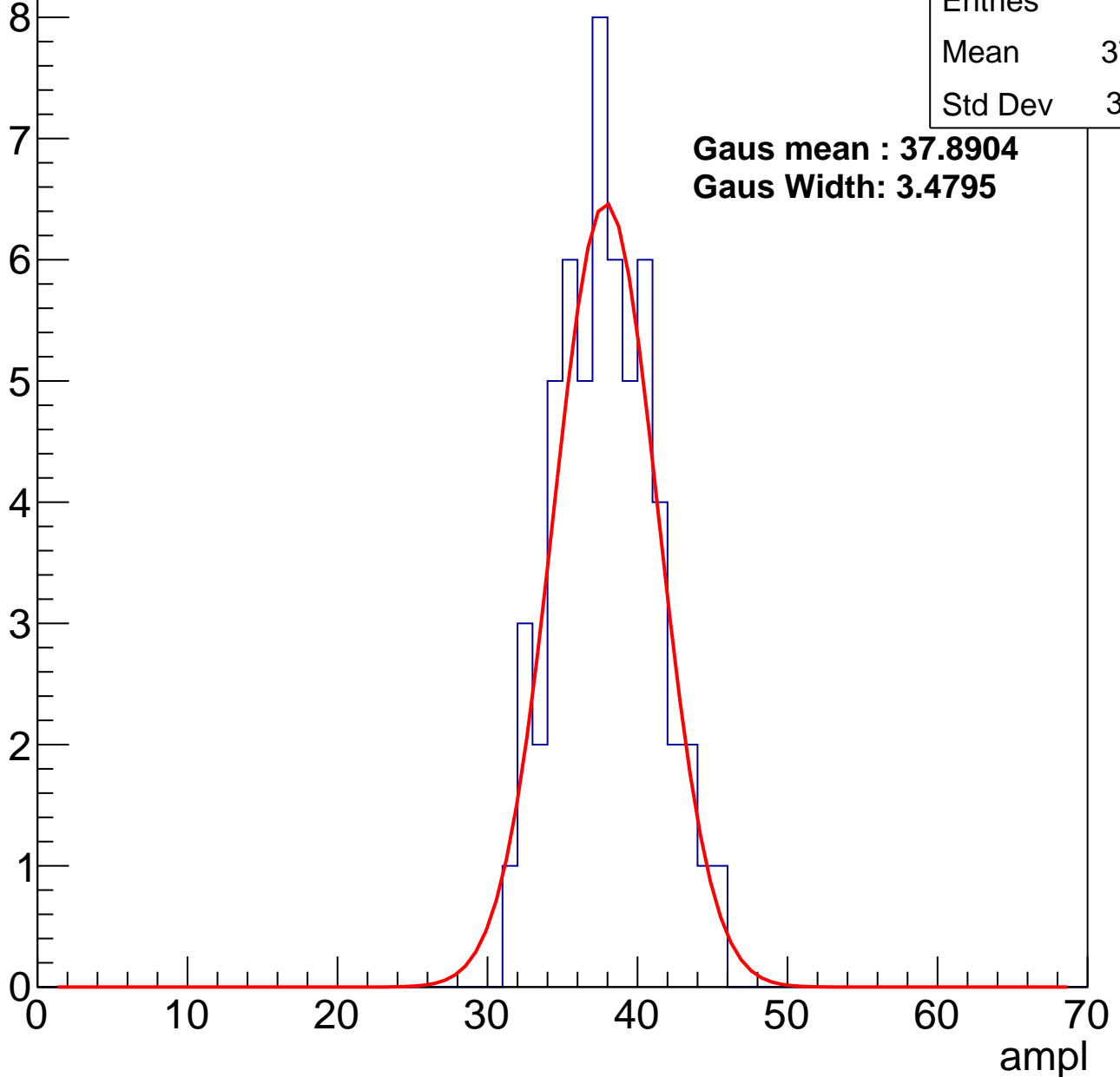
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	37.46
Std Dev	3.201

**Gaus mean : 37.8904**

**Gaus Width: 3.4795**



# B1L102S, U16-ch21, adc2

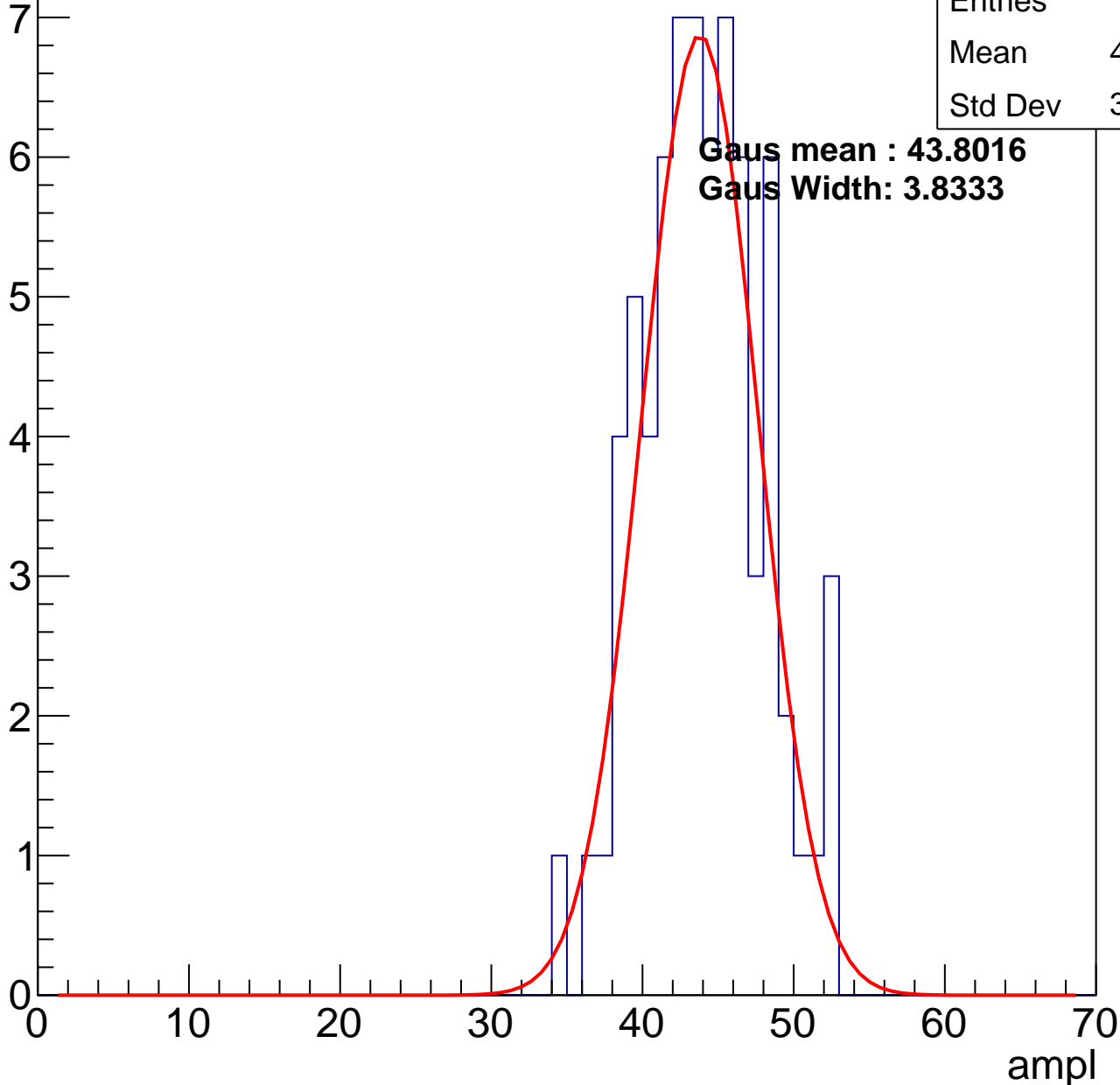
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	43.58
Std Dev	3.942

**Gaus mean : 43.8016**

**Gaus Width: 3.8333**

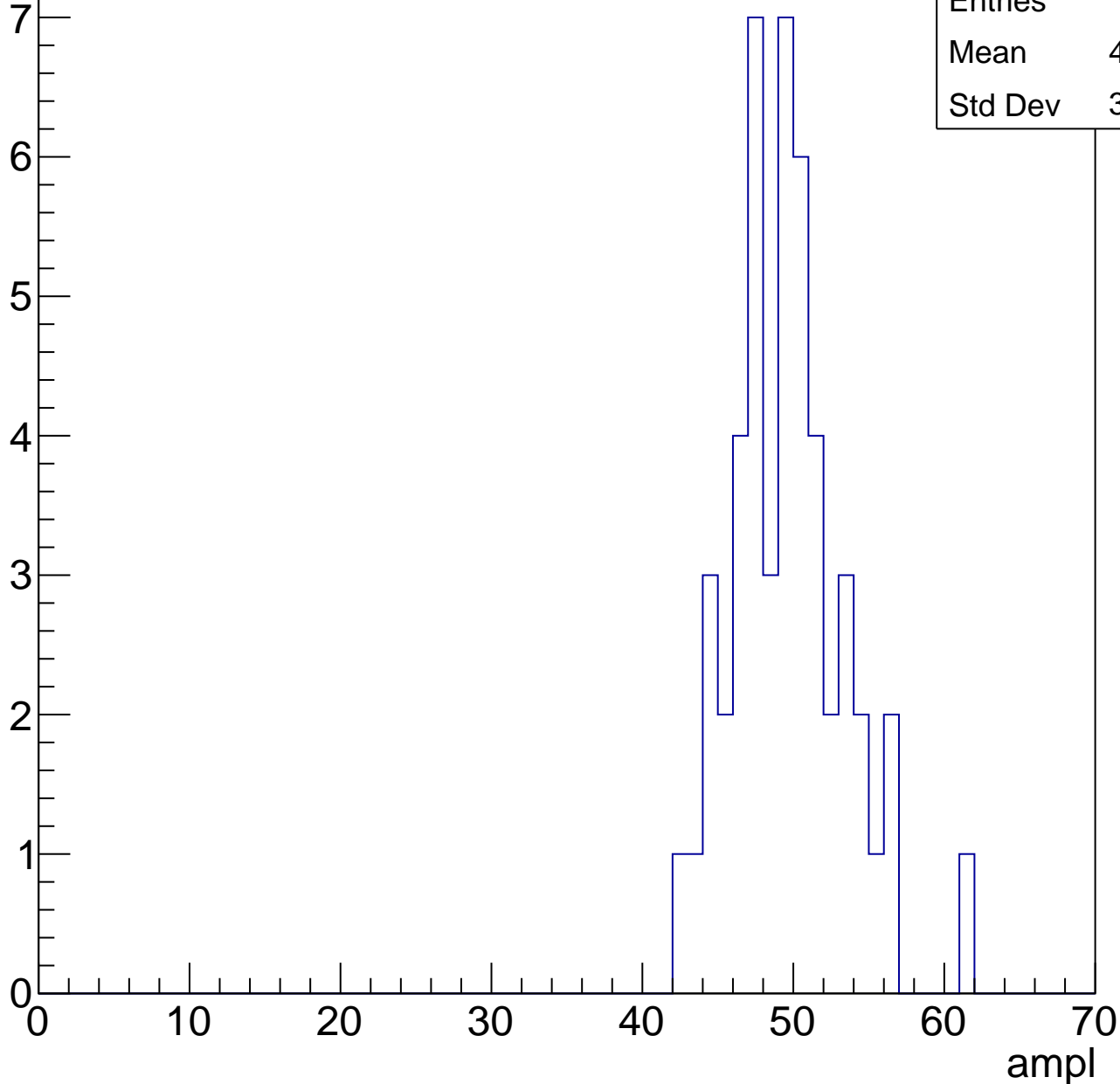


# B1L102S, U16-ch21, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	49.18
Std Dev	3.707

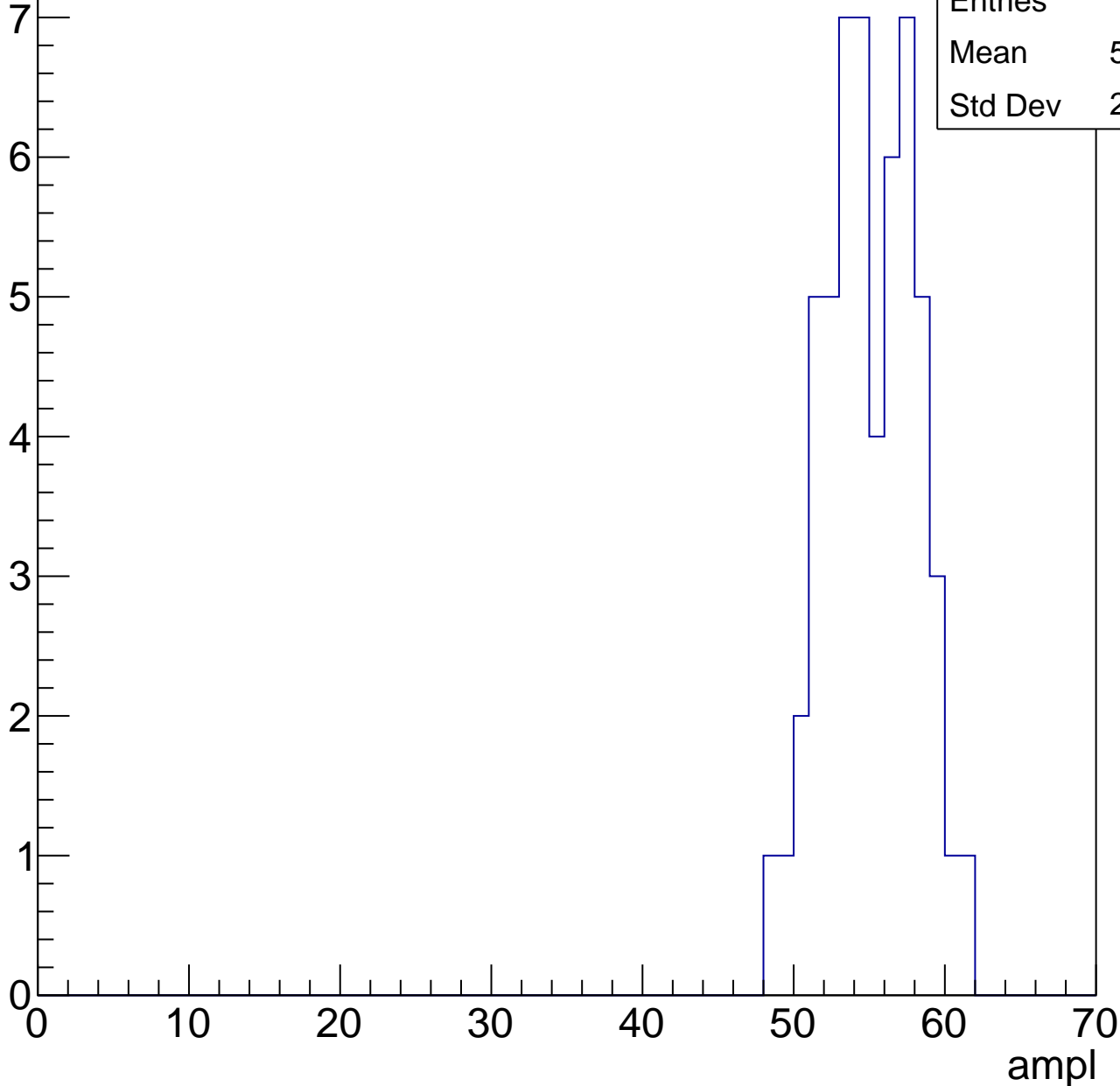


# B1L102S, U16-ch21, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	54.62
Std Dev	2.939

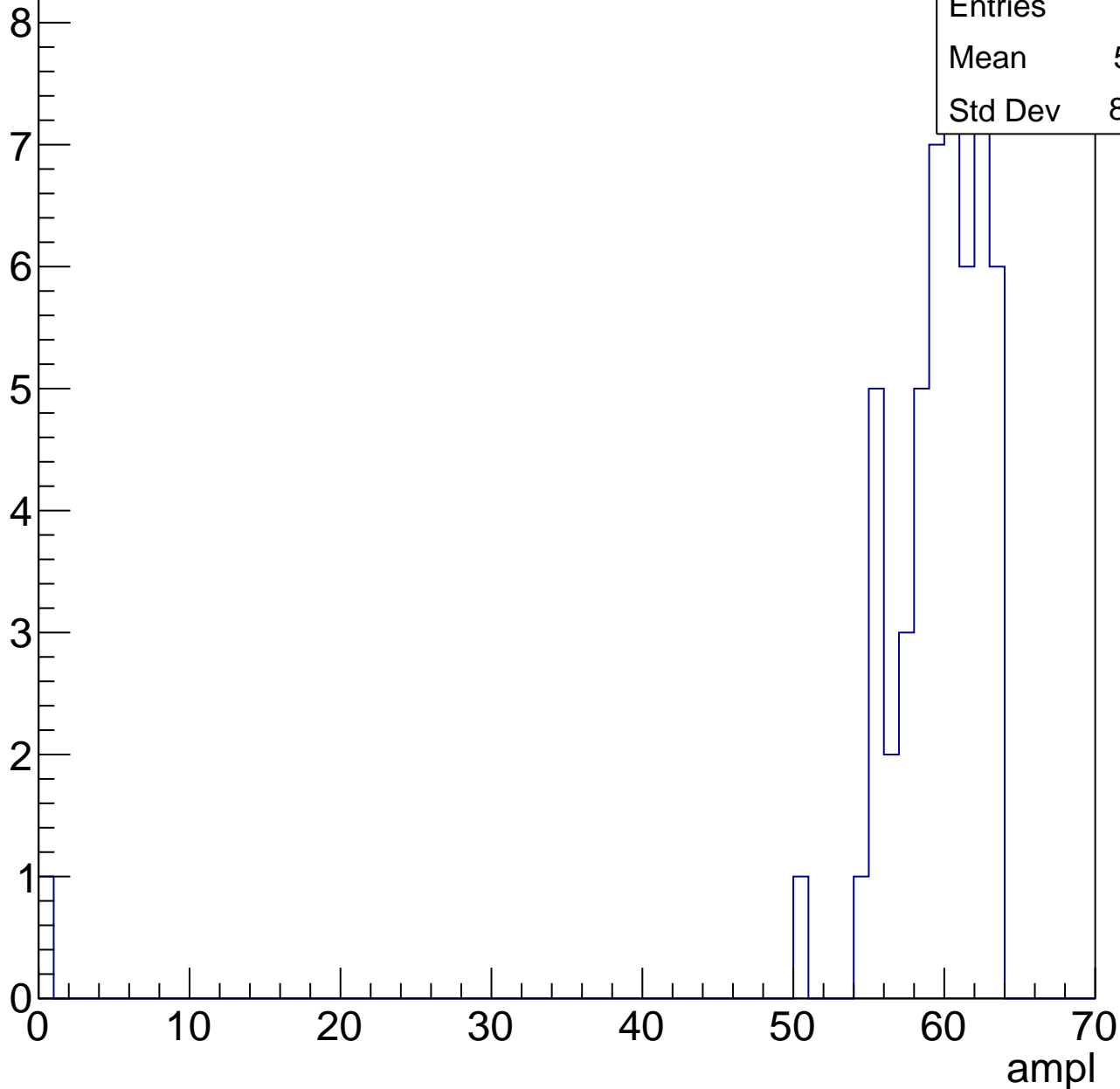


# B1L102S, U16-ch21, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

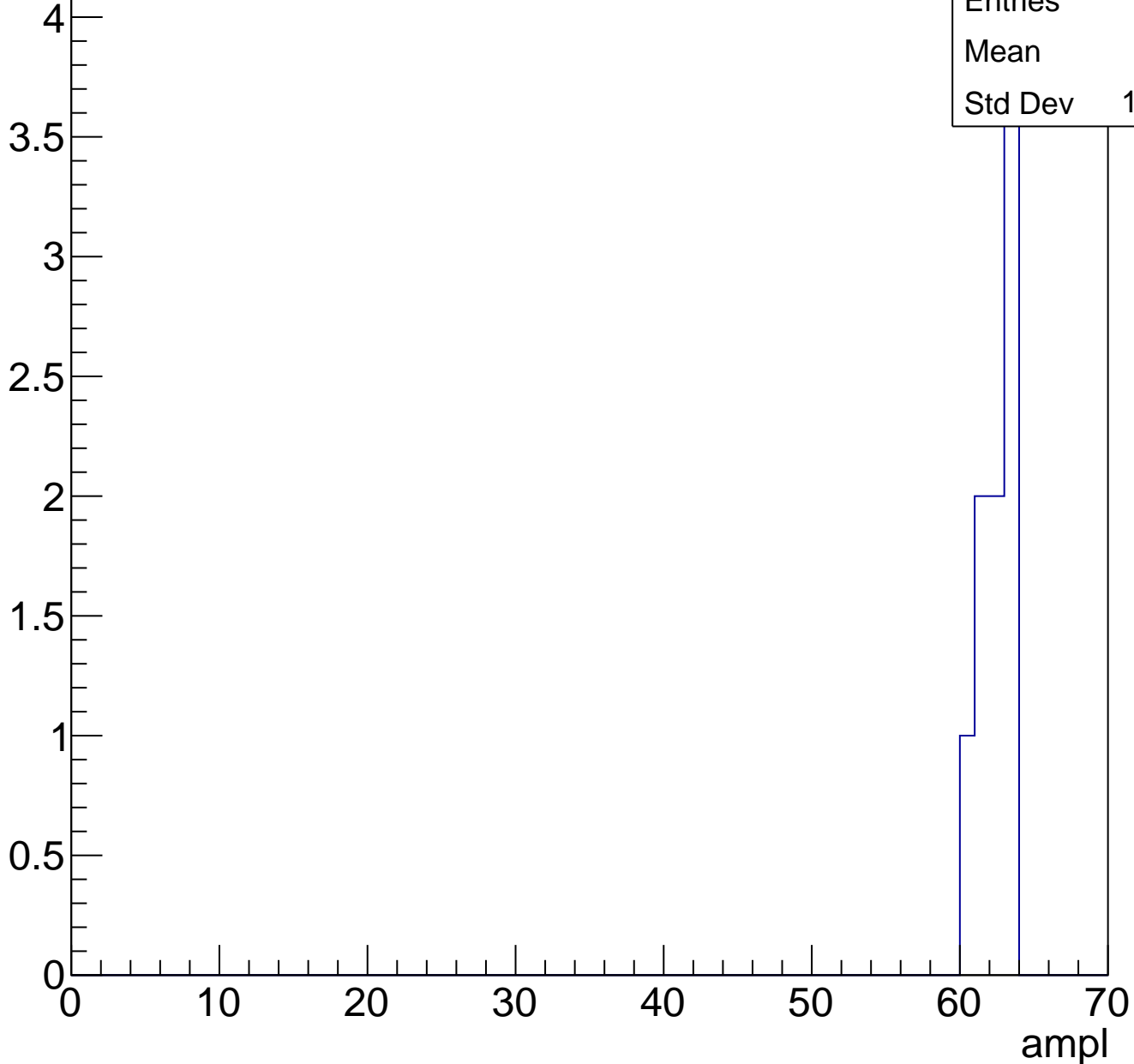
Entries	53
Mean	58.21
Std Dev	8.544



# B1L102S, U16-ch21, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch21, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch22, adc0

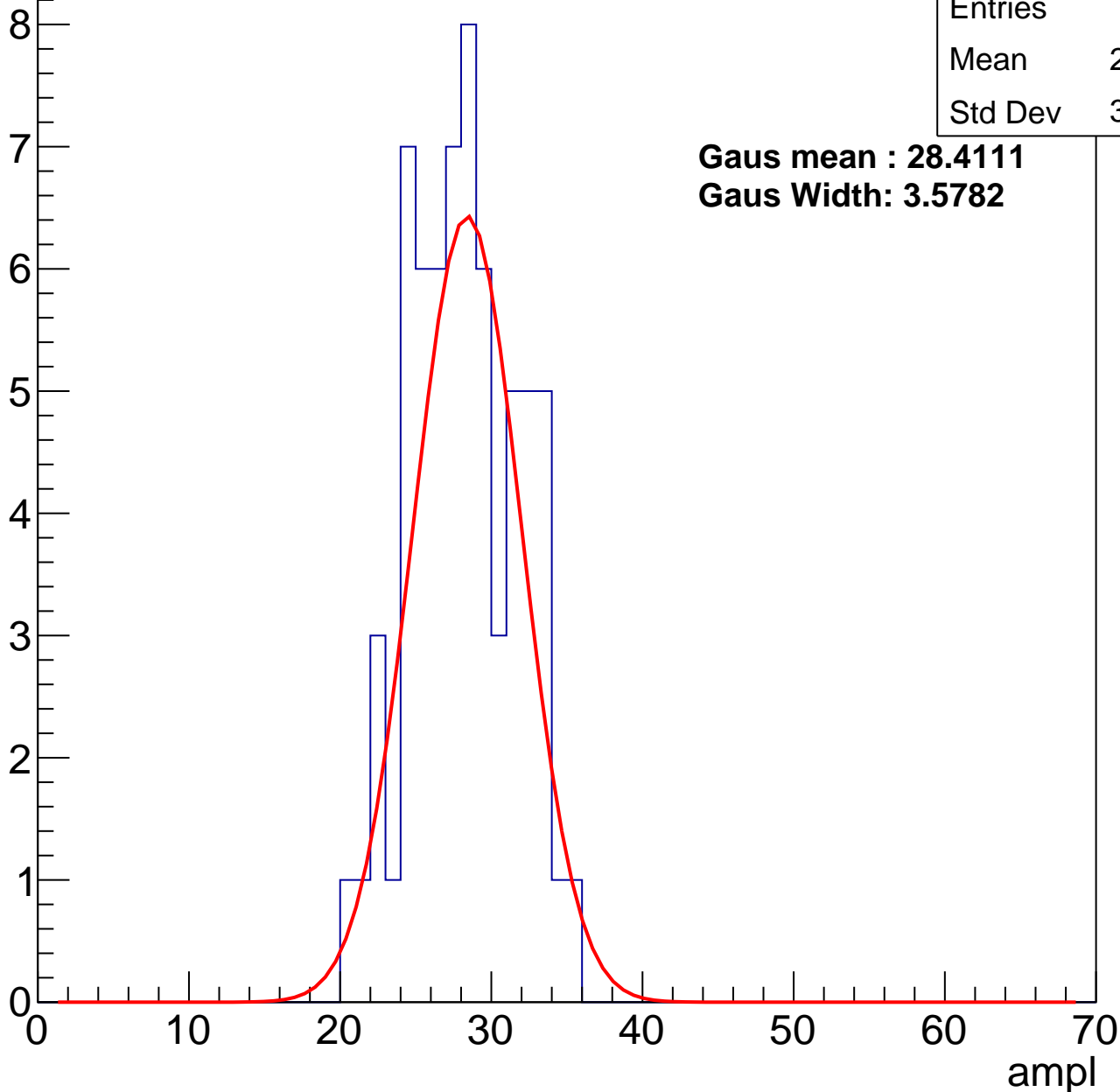
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	27.73
Std Dev	3.462

**Gaus mean : 28.4111**

**Gaus Width: 3.5782**



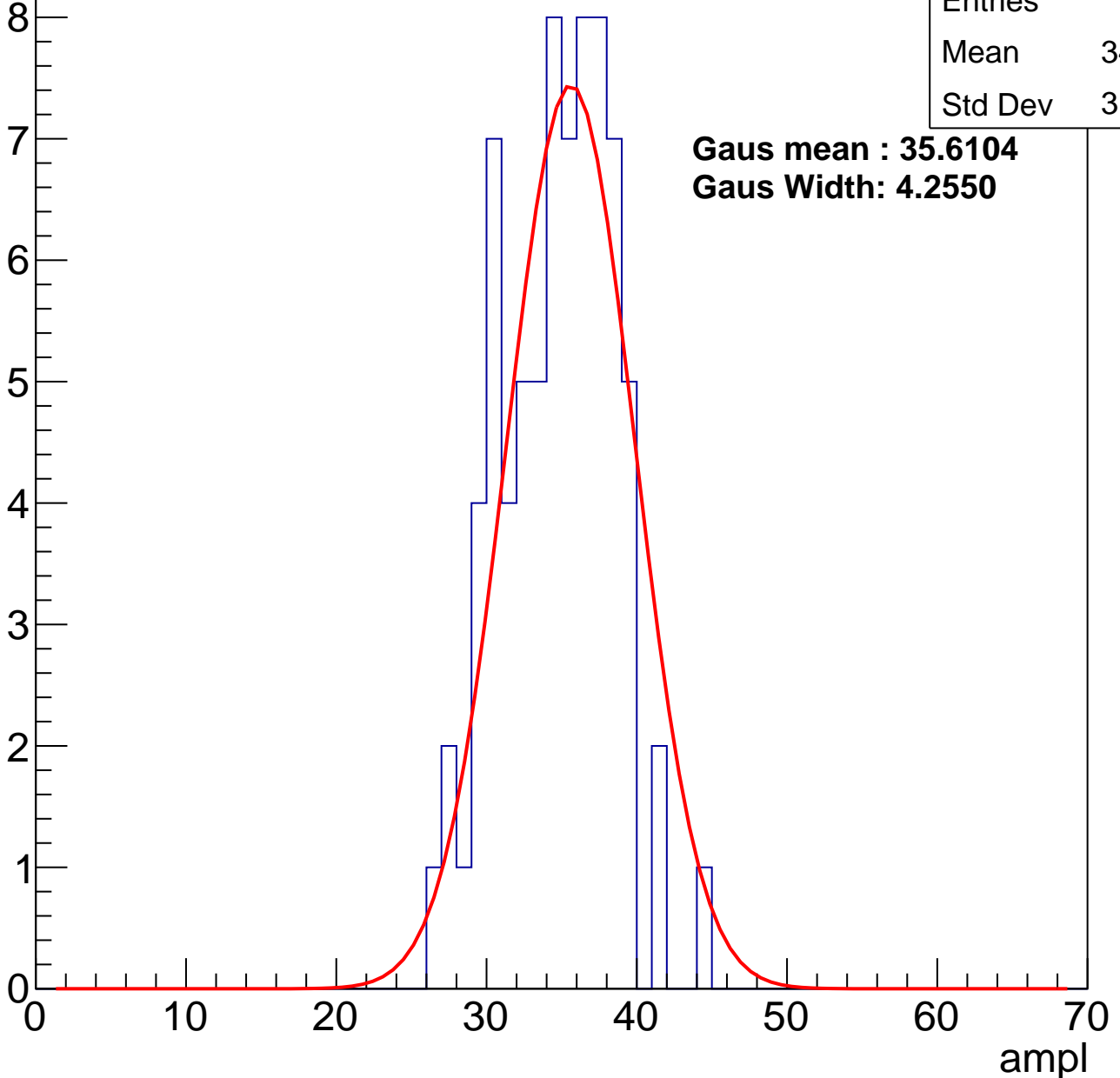
# B1L102S, U16-ch22, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	34.28
Std Dev	3.672

**Gaus mean : 35.6104**  
**Gaus Width: 4.2550**



# B1L102S, U16-ch22, adc2

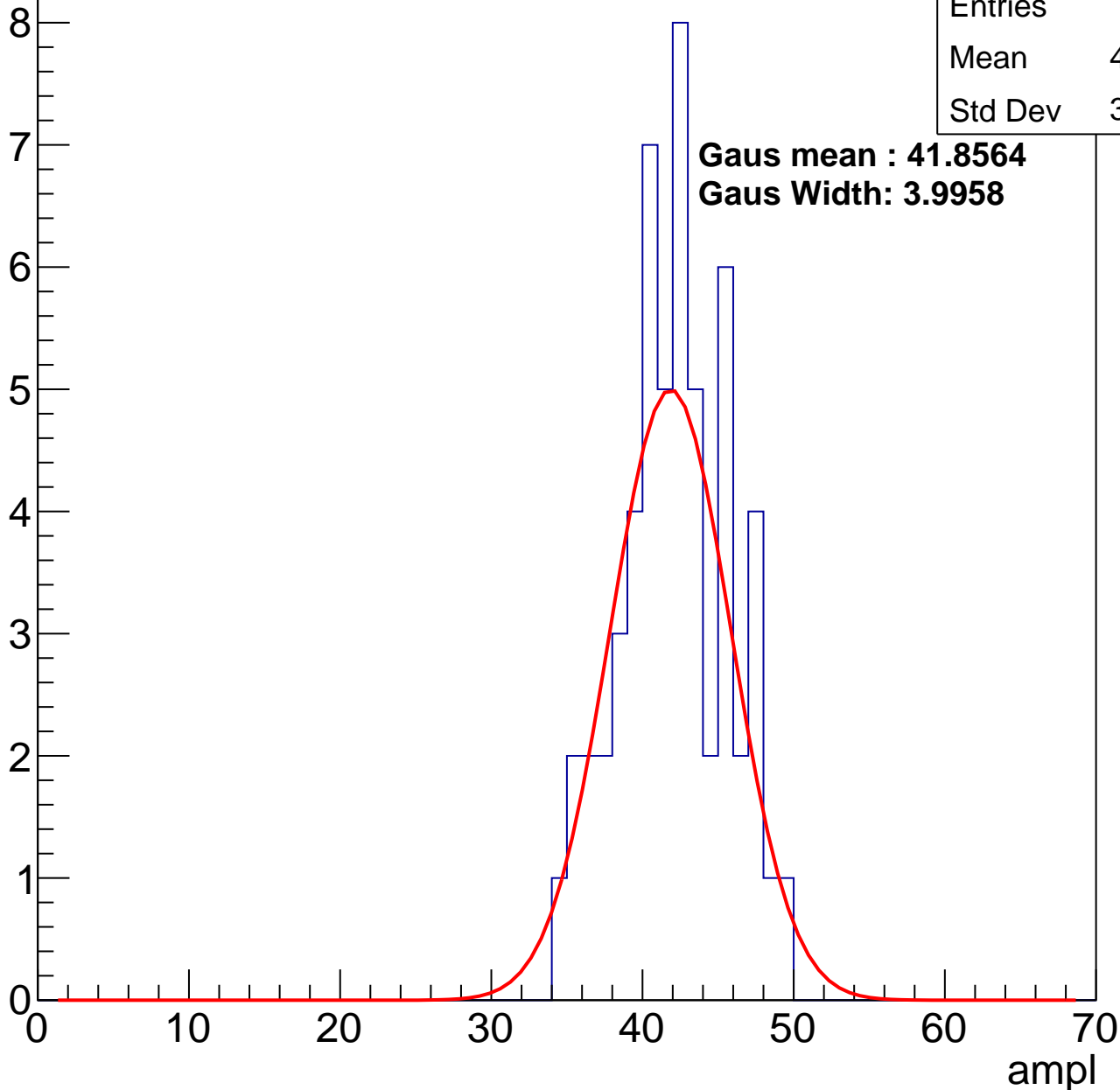
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	41.65
Std Dev	3.512

**Gaus mean : 41.8564**

**Gaus Width: 3.9958**

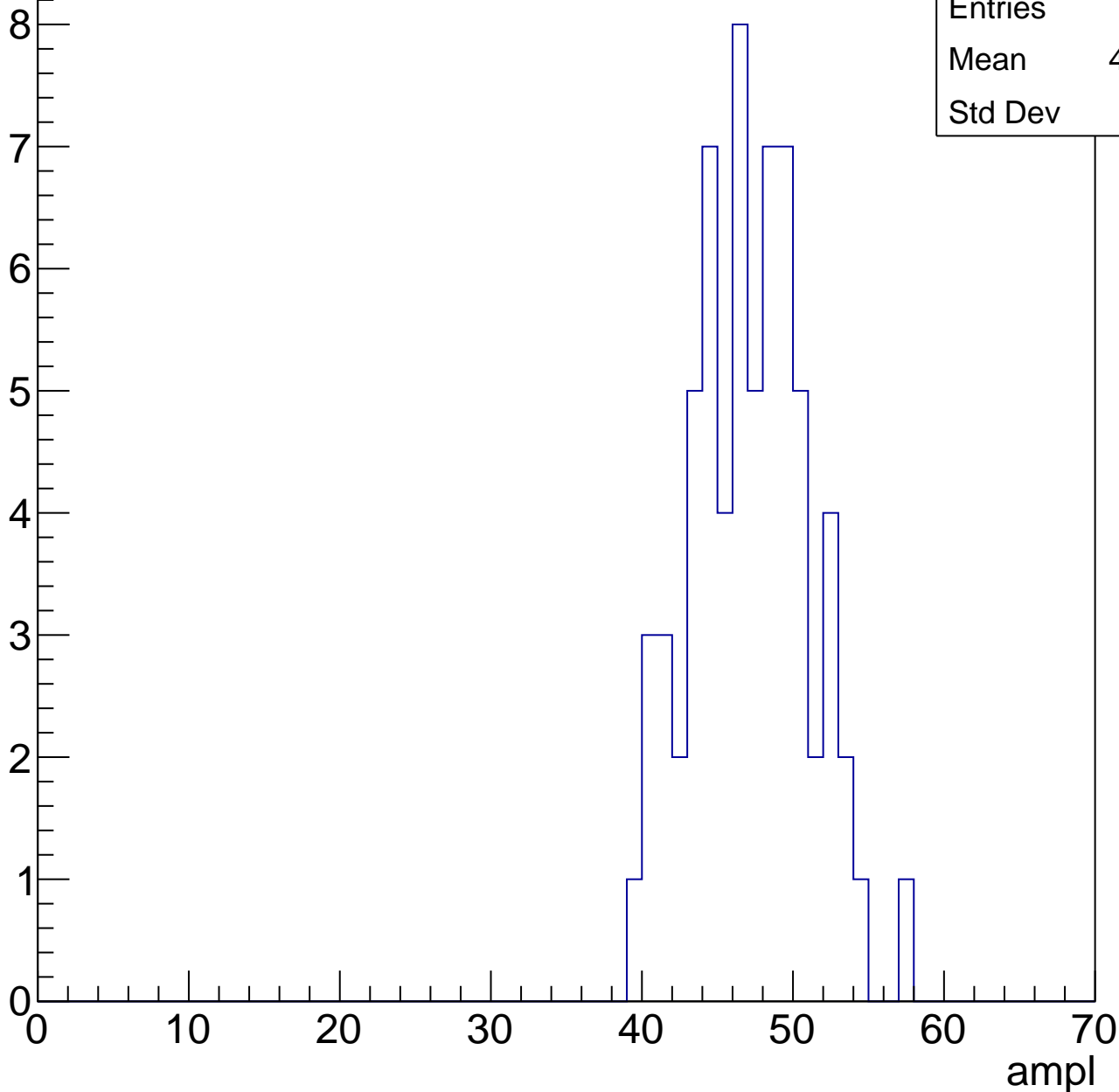


# B1L102S, U16-ch22, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	46.69
Std Dev	3.79

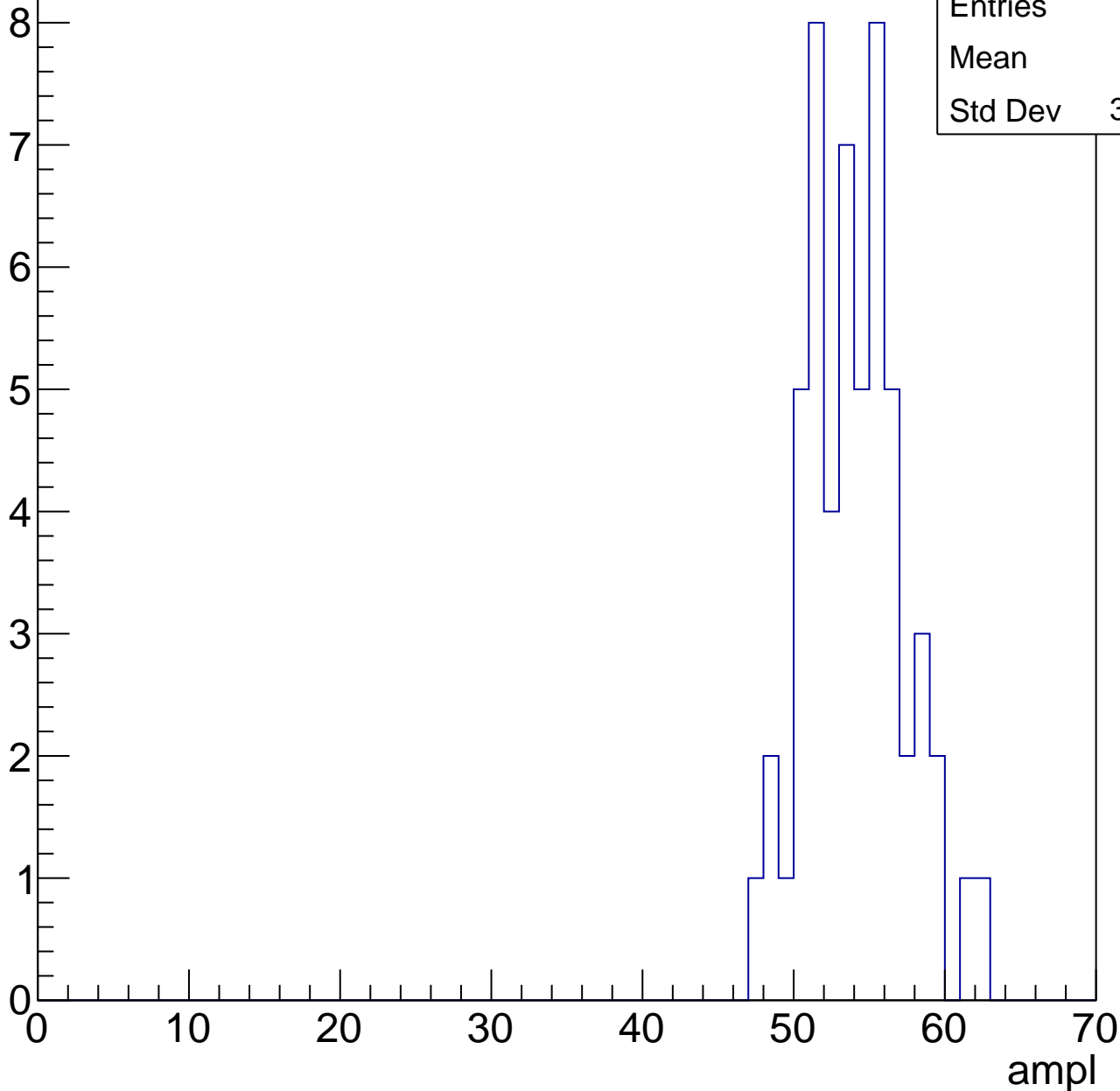


# B1L102S, U16-ch22, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

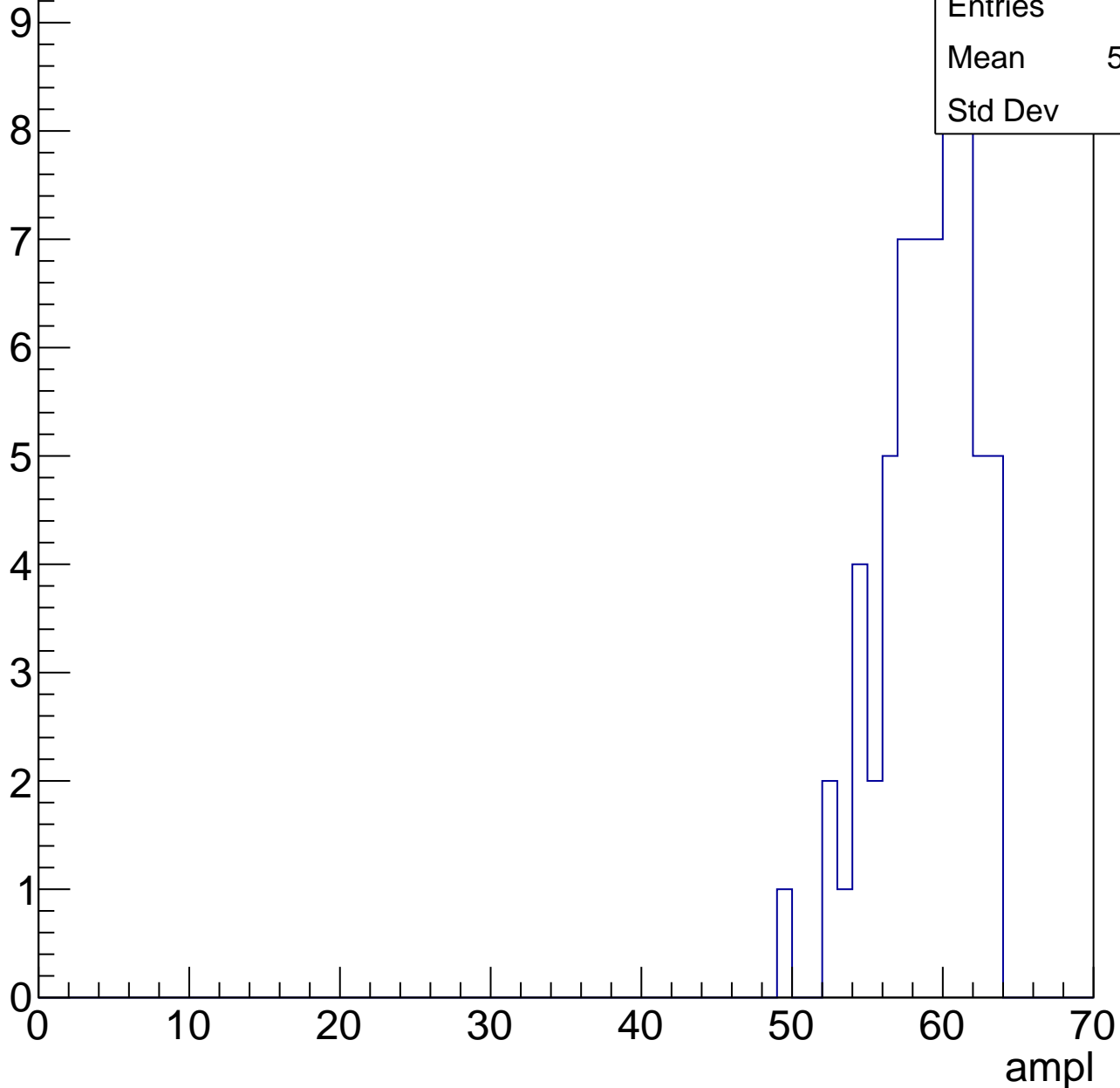
Entries	55
Mean	53.6
Std Dev	3.217



# B1L102S, U16-ch22, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

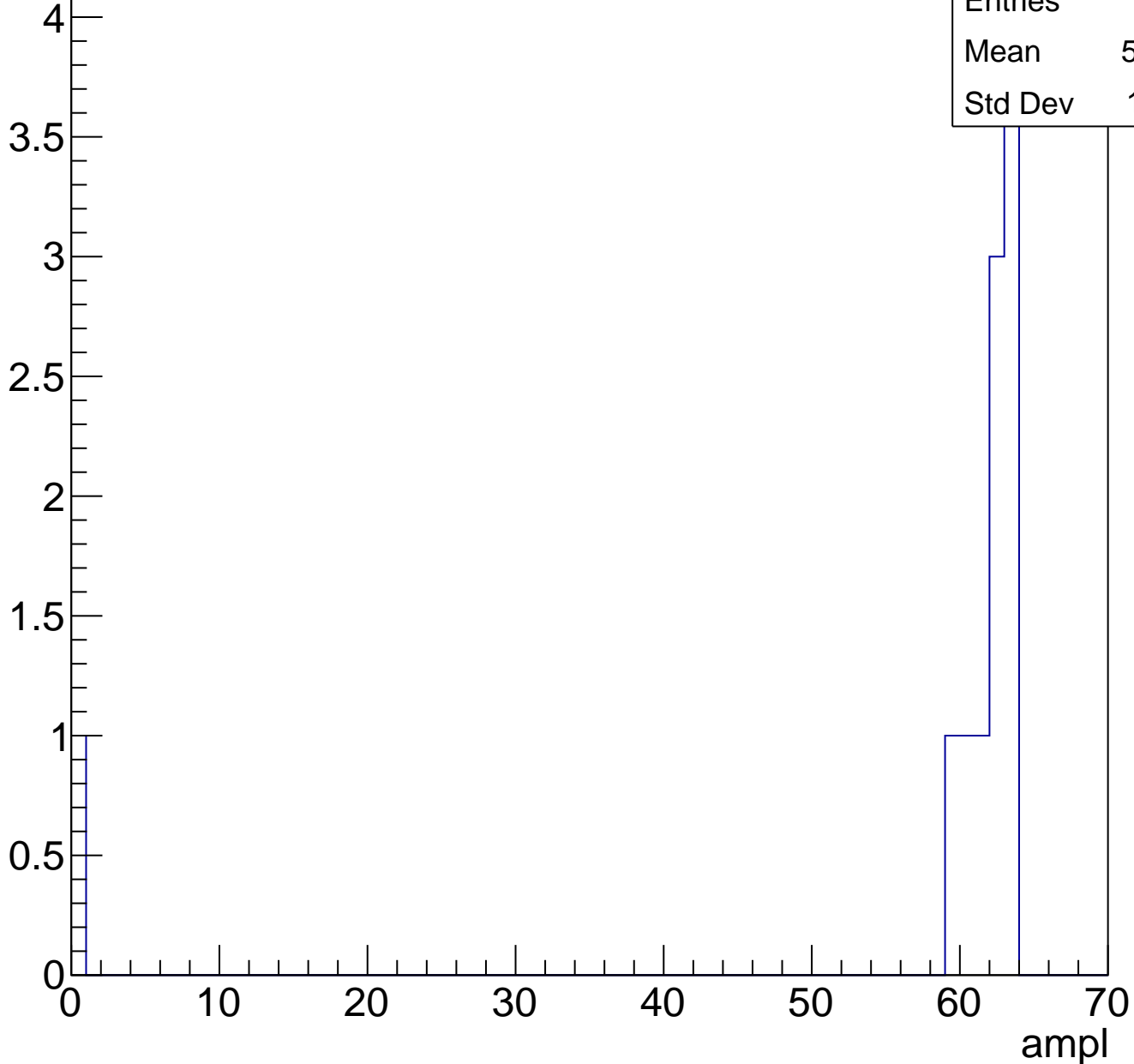
Entry



# B1L102S, U16-ch22, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch22, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	4
Mean	31.25
Std Dev	31.25

# B1L102S, U16-ch23, adc0

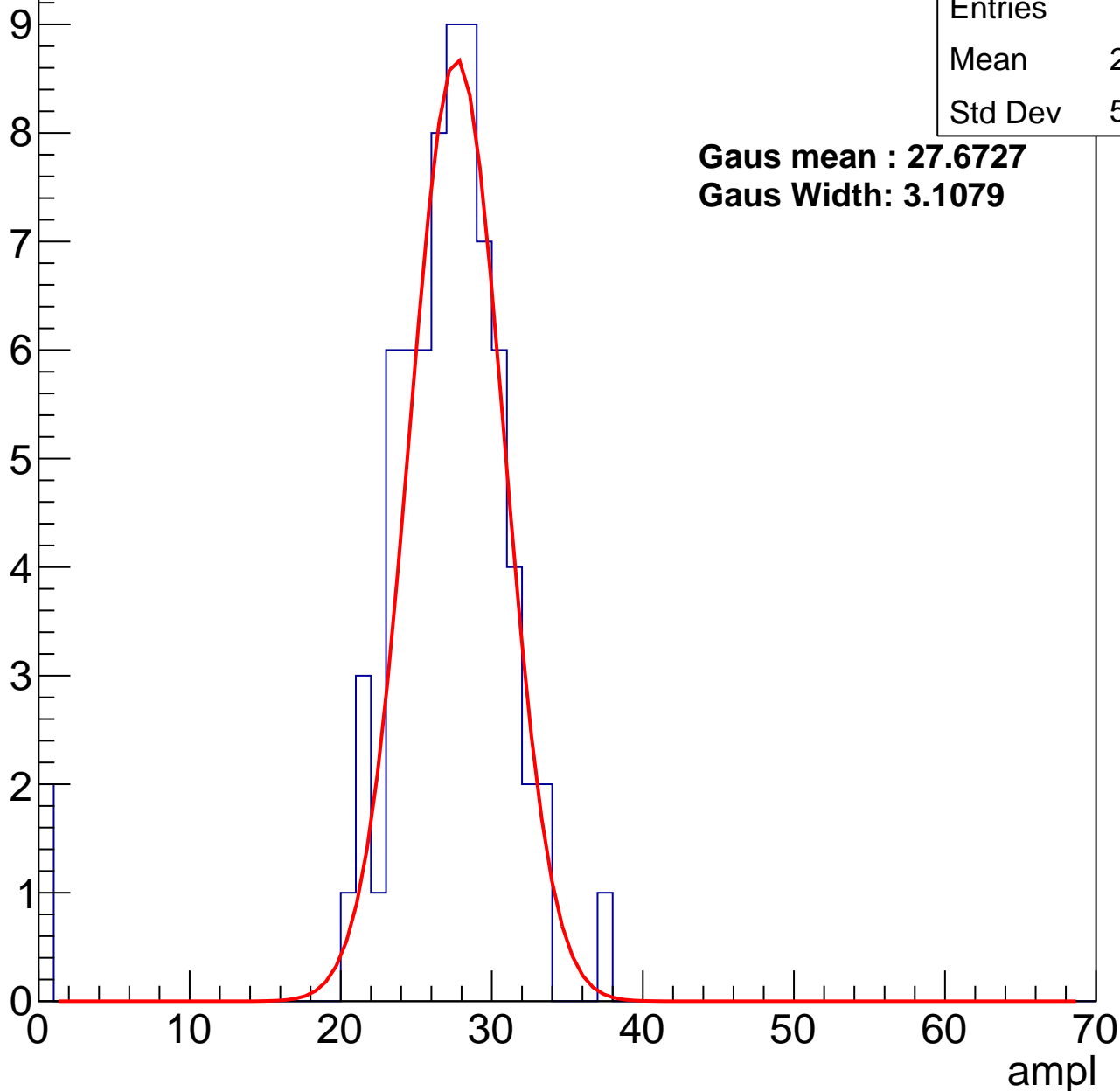
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	26.22
Std Dev	5.433

**Gaus mean : 27.6727**

**Gaus Width: 3.1079**



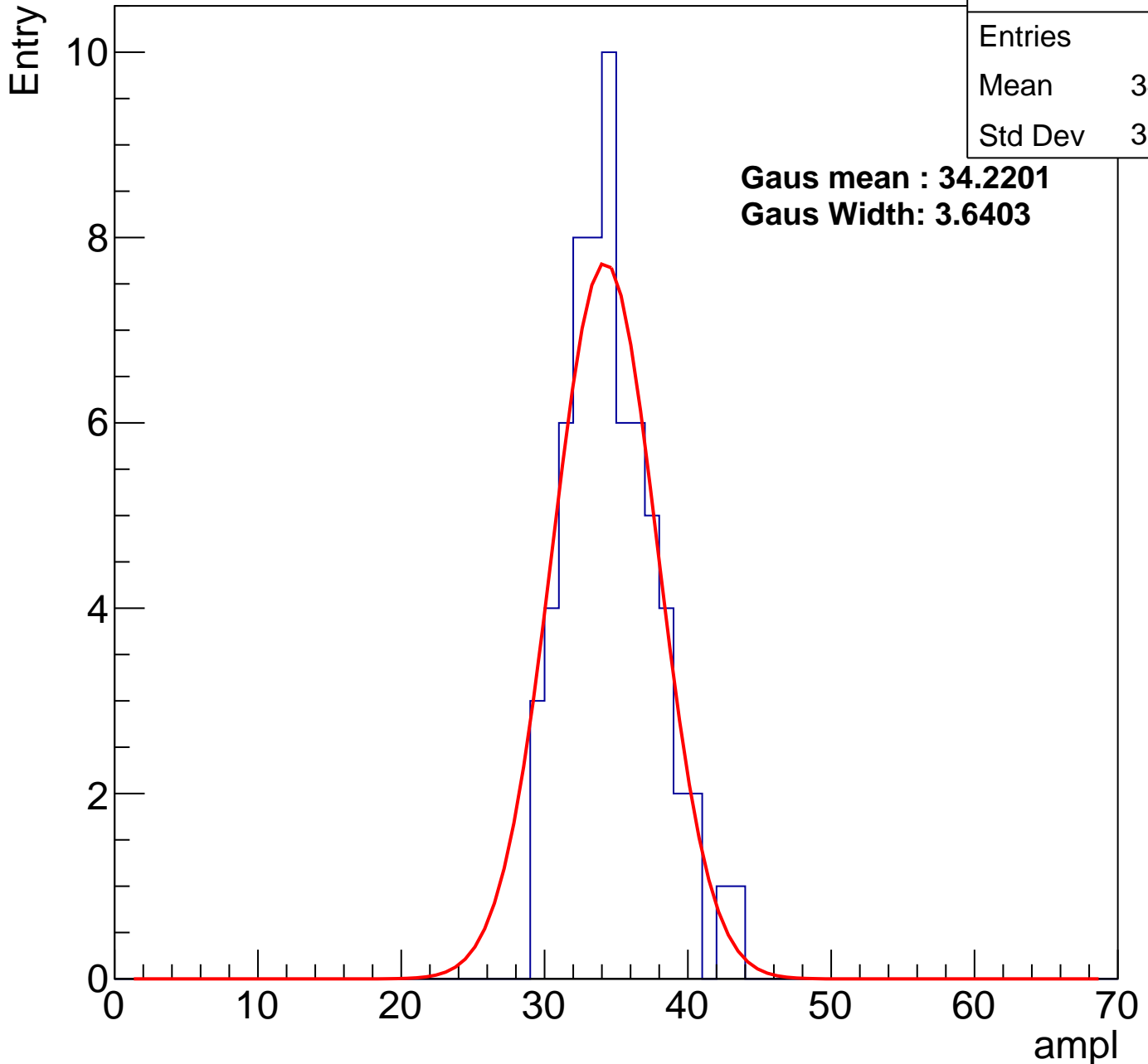
# B1L102S, U16-ch23, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	66
Mean	34.23
Std Dev	3.103

**Gaus mean : 34.2201**

**Gaus Width: 3.6403**



# B1L102S, U16-ch23, adc2

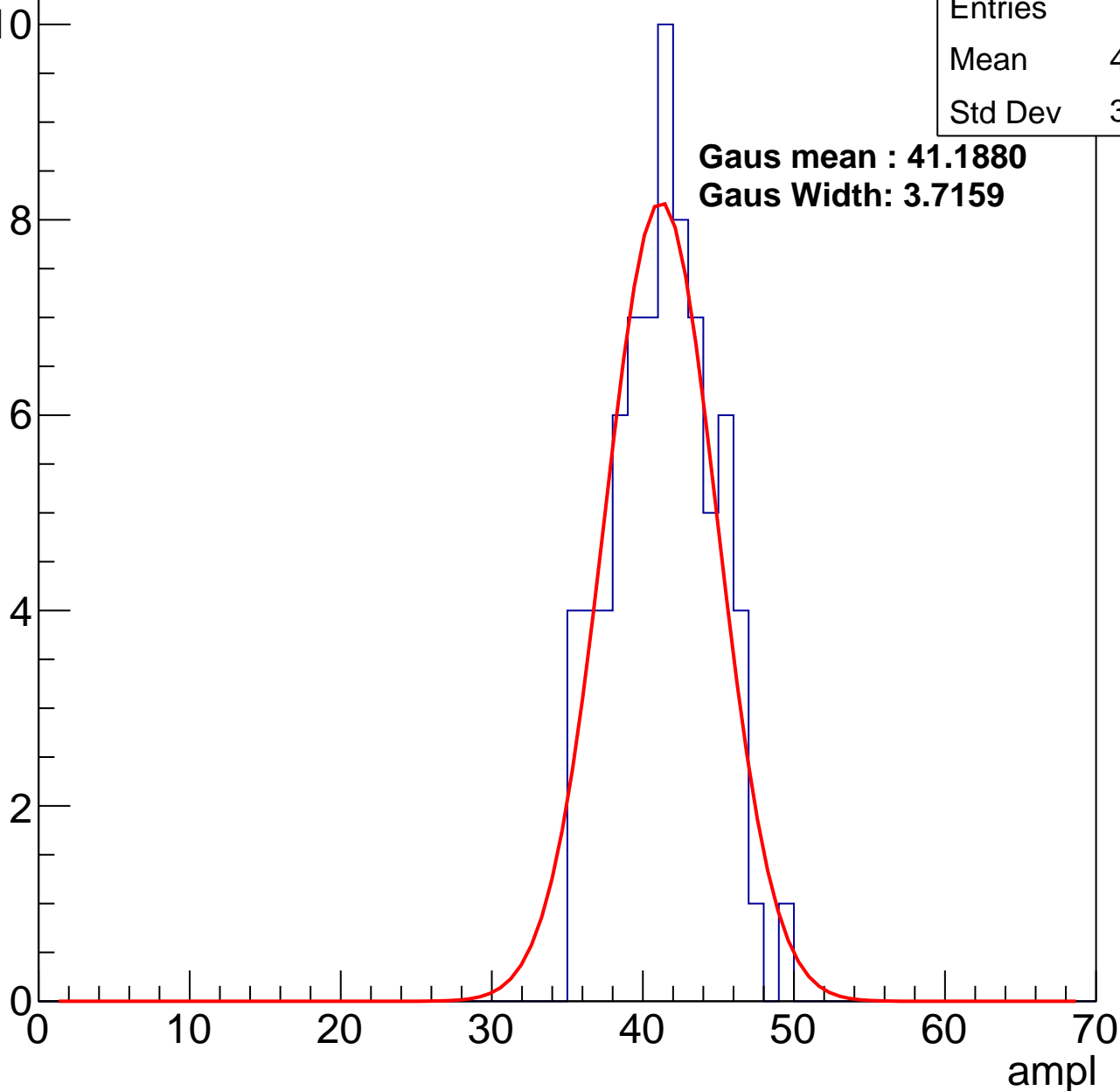
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	40.95
Std Dev	3.234

**Gaus mean : 41.1880**

**Gaus Width: 3.7159**



# B1L102S, U16-ch23, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

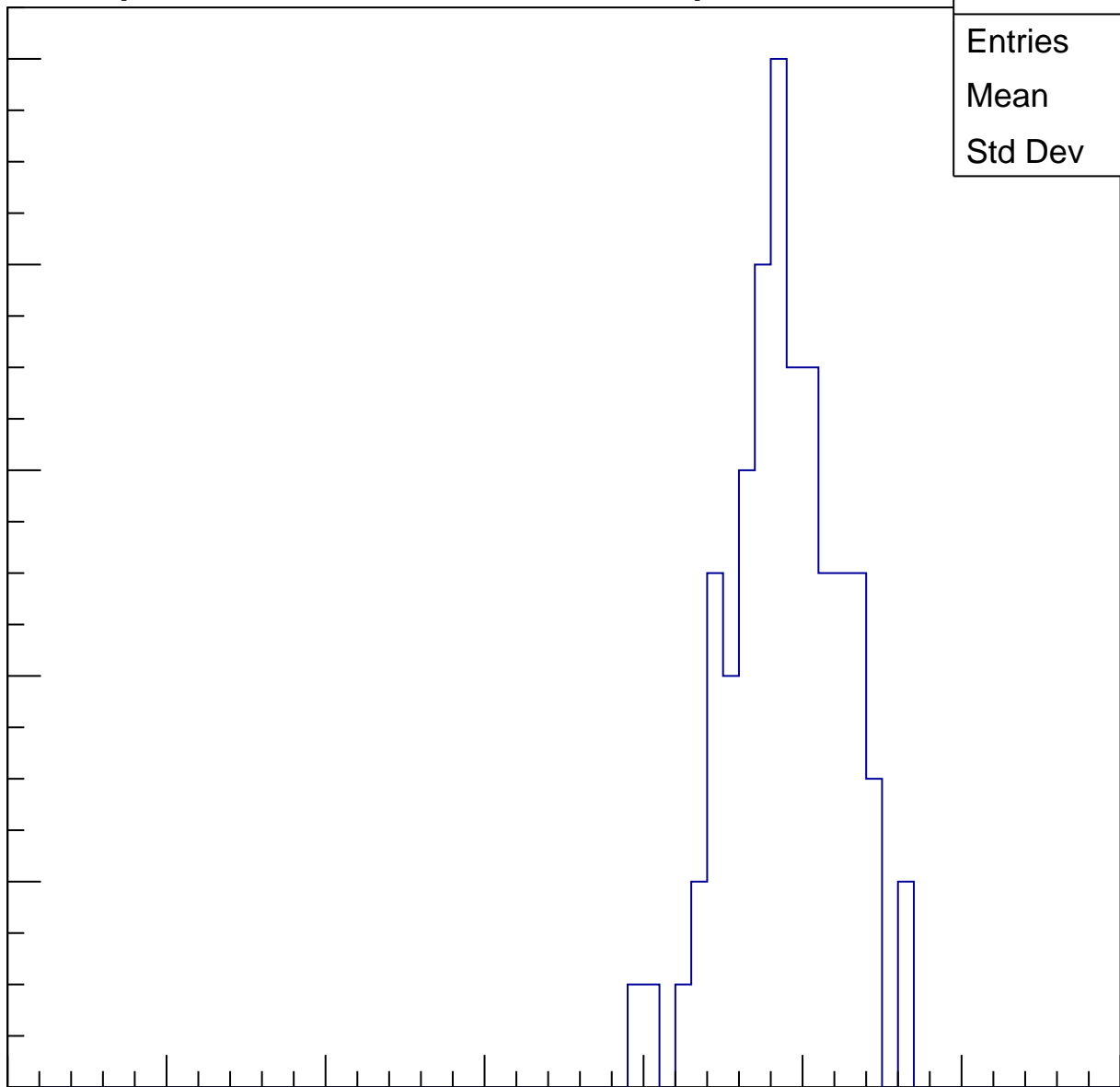
Entries	72
Mean	48.42
Std Dev	3.511

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

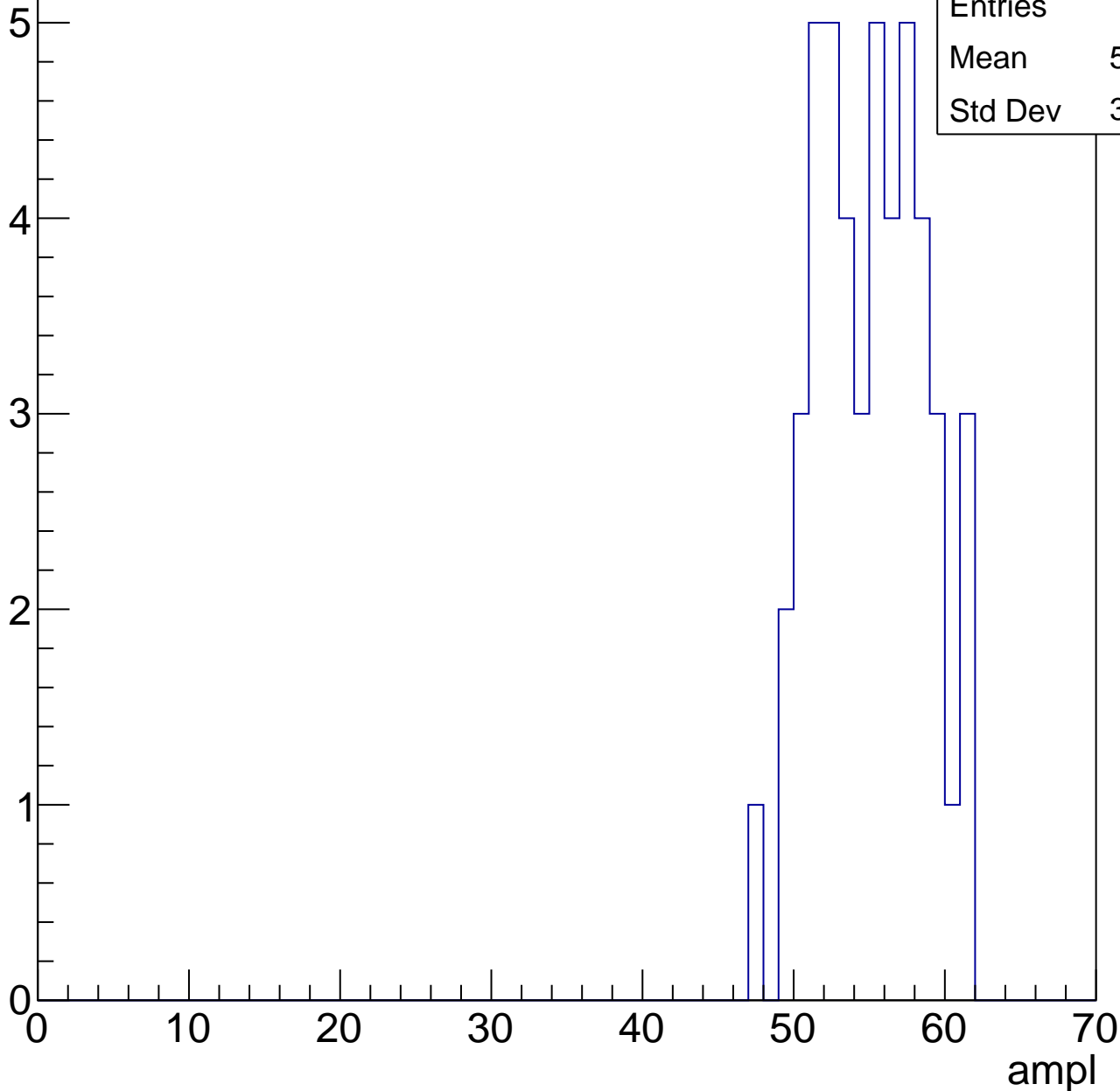


# B1L102S, U16-ch23, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	54.58
Std Dev	3.499



# B1L102S, U16-ch23, adc5

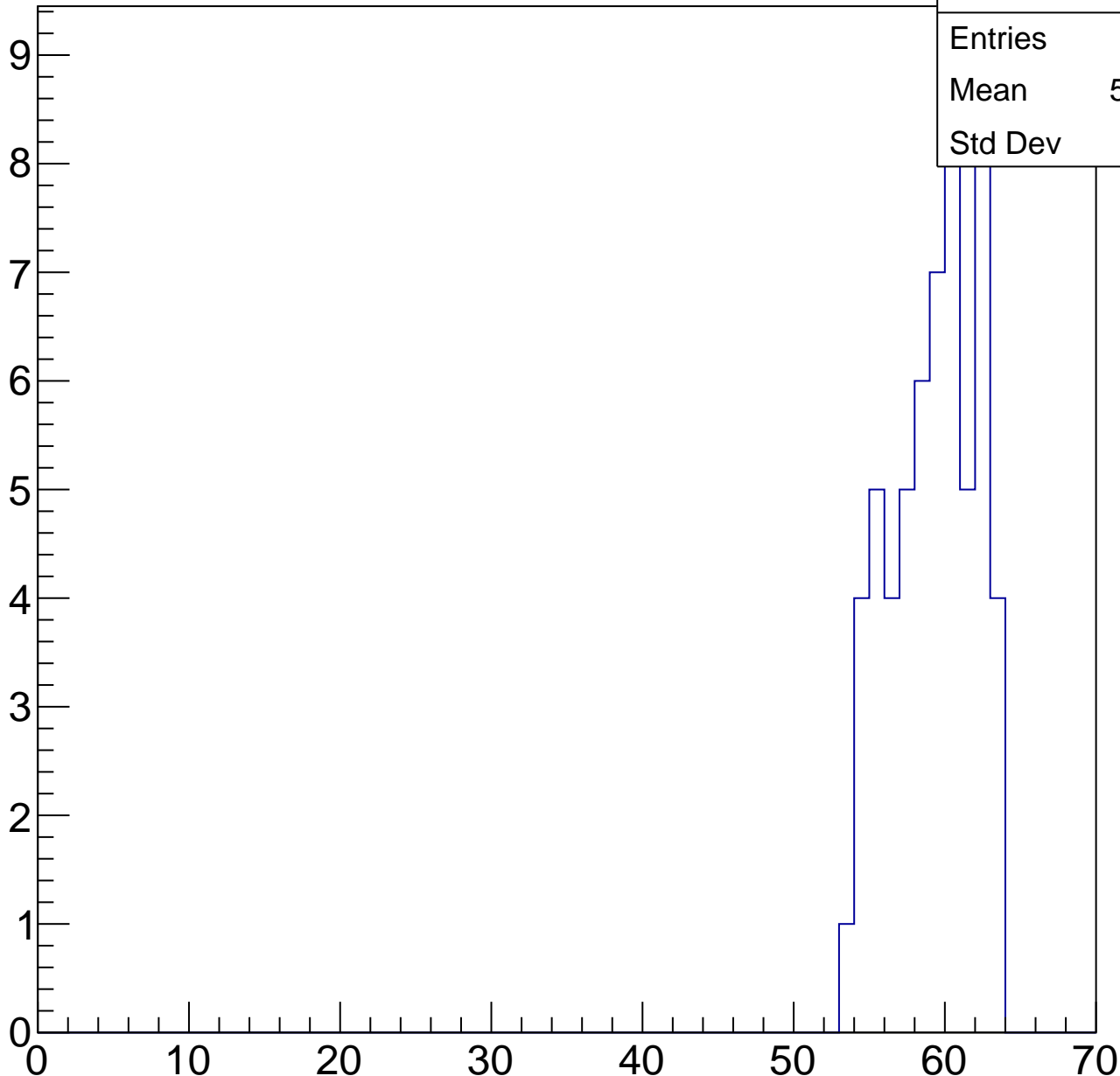
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	58
Mean	58.78
Std Dev	2.78

ampl

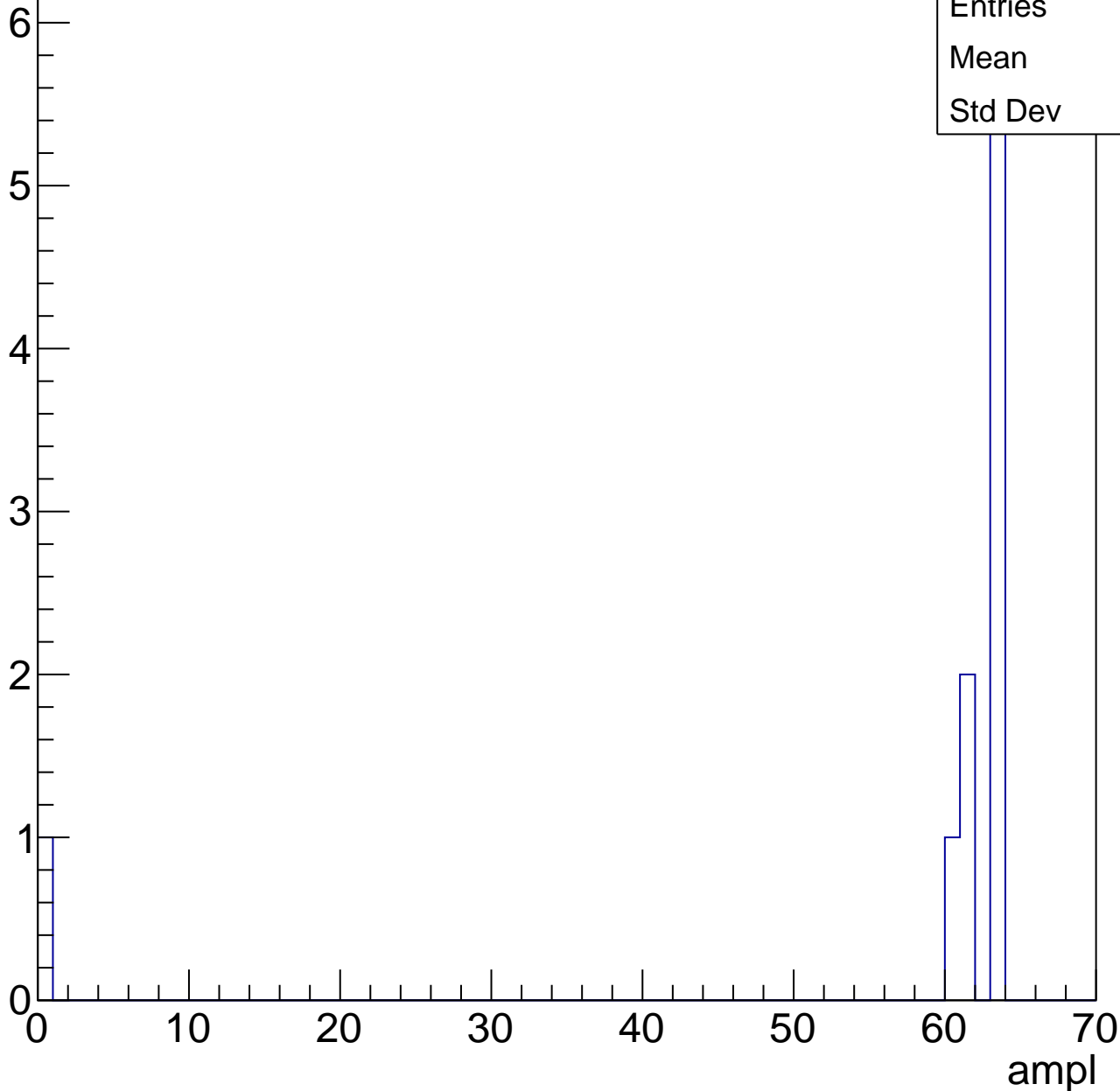


# B1L102S, U16-ch23, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	10
Mean	56
Std Dev	18.7





# B1L102S, U16-ch23, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch24, adc0

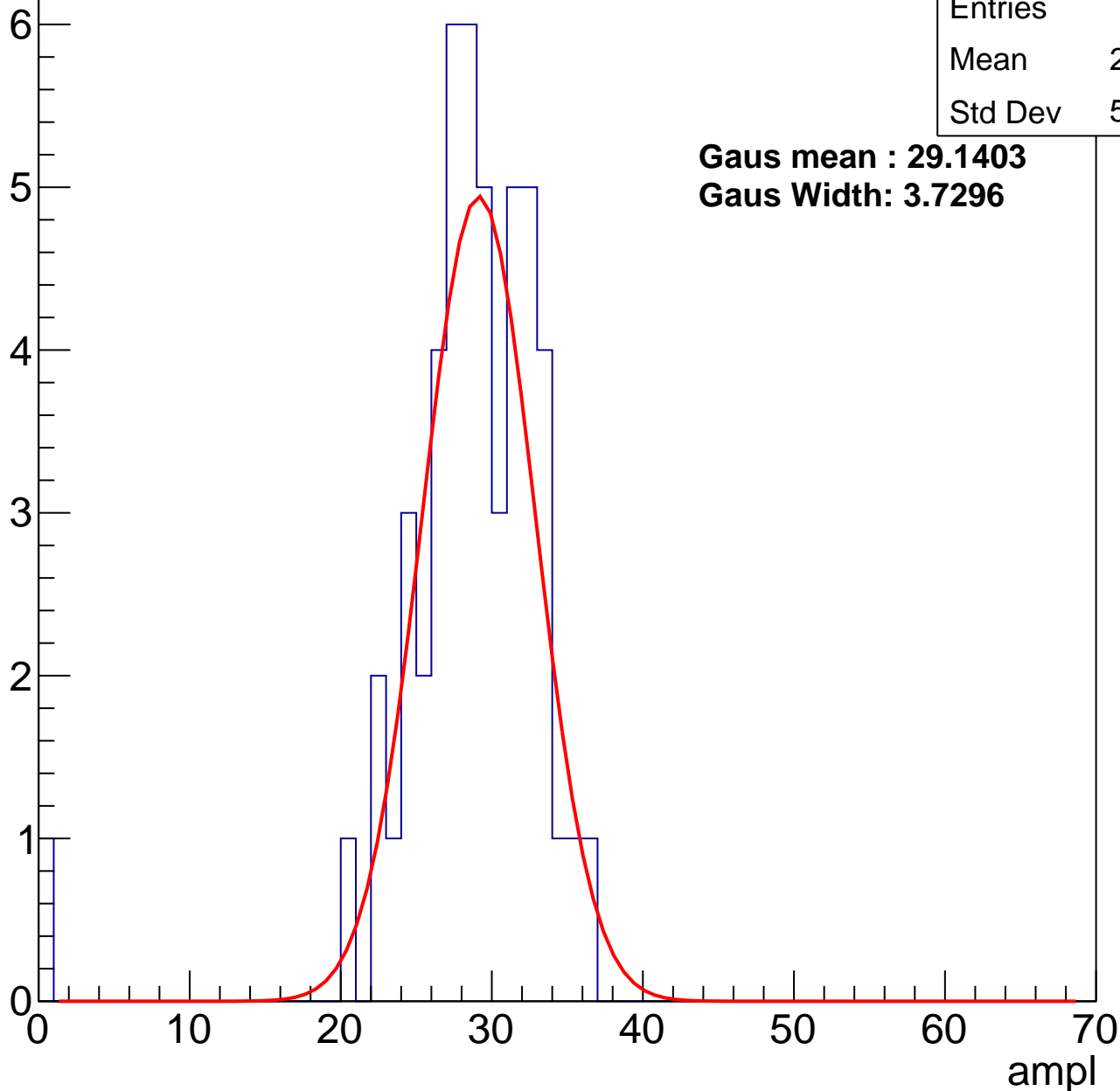
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	28.04
Std Dev	5.284

**Gaus mean : 29.1403**

**Gaus Width: 3.7296**



# B1L102S, U16-ch24, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	94
Mean	34.81
Std Dev	5.608

**Gaus mean : 35.3198**

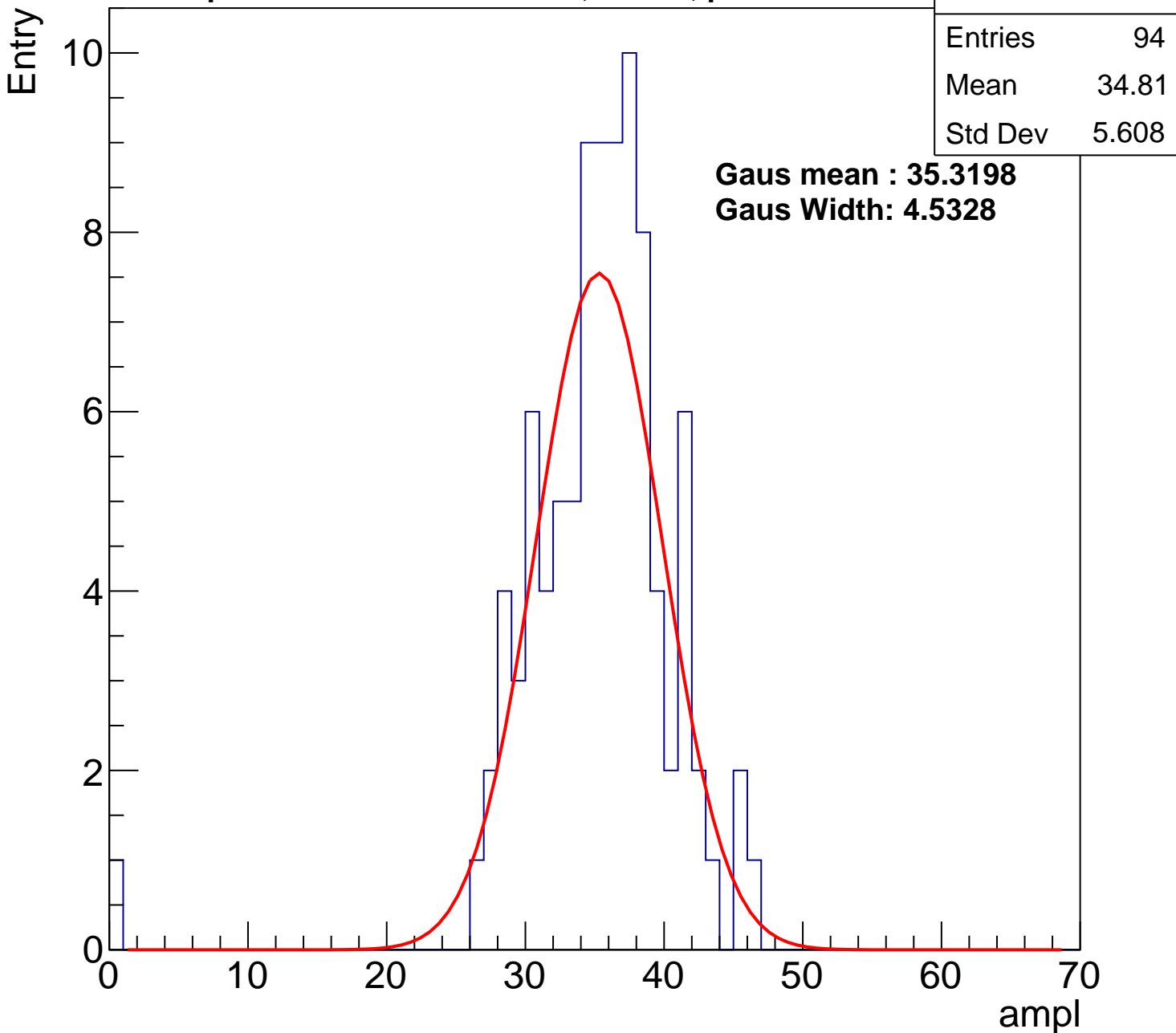
**Gaus Width: 4.5328**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U16-ch24, adc2

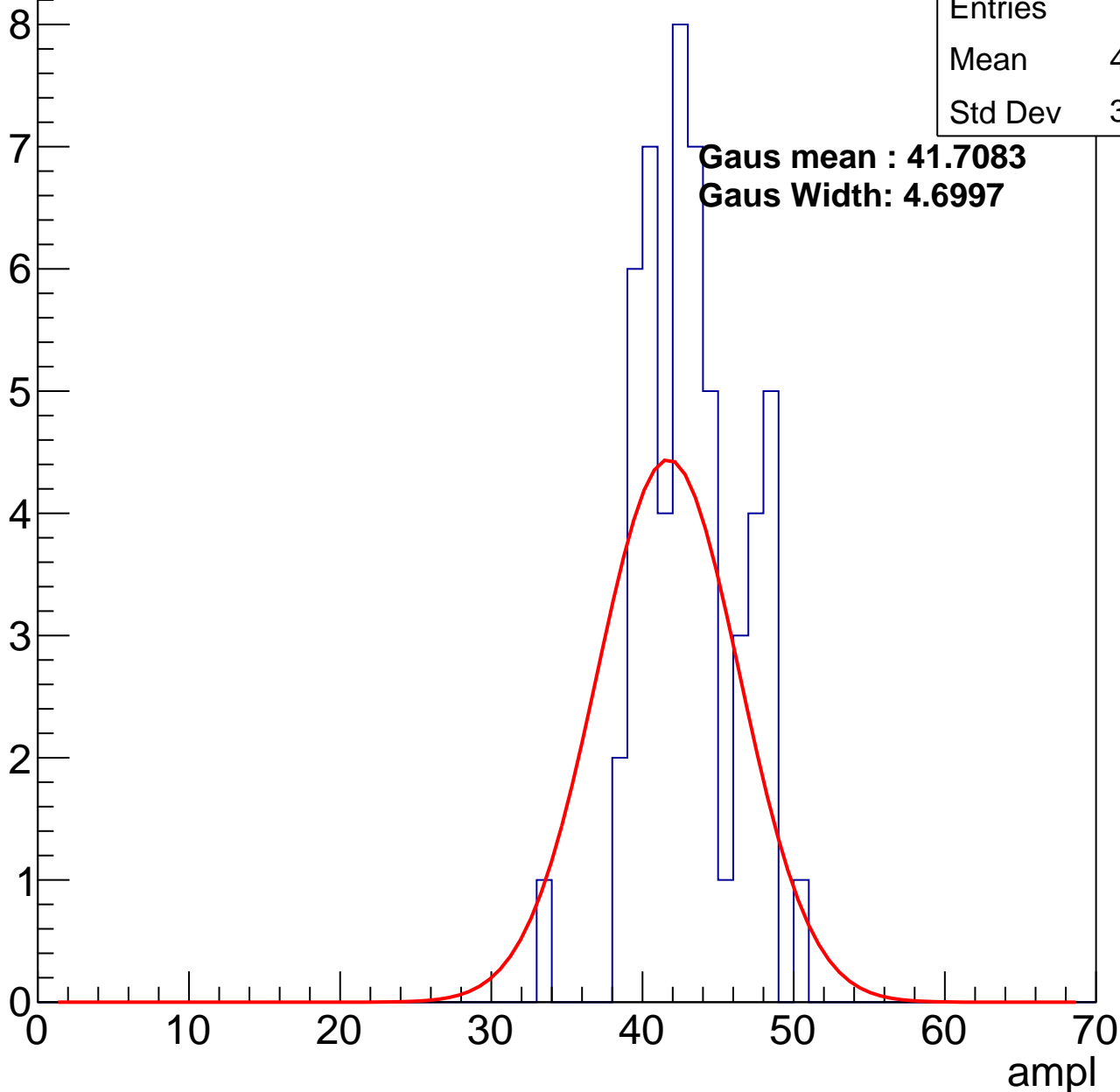
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	42.69
Std Dev	3.338

**Gaus mean : 41.7083**

**Gaus Width: 4.6997**



# B1L102S, U16-ch24, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	80
Mean	49.26
Std Dev	3.587

Entry

10

8

6

4

2

0

0

10

20

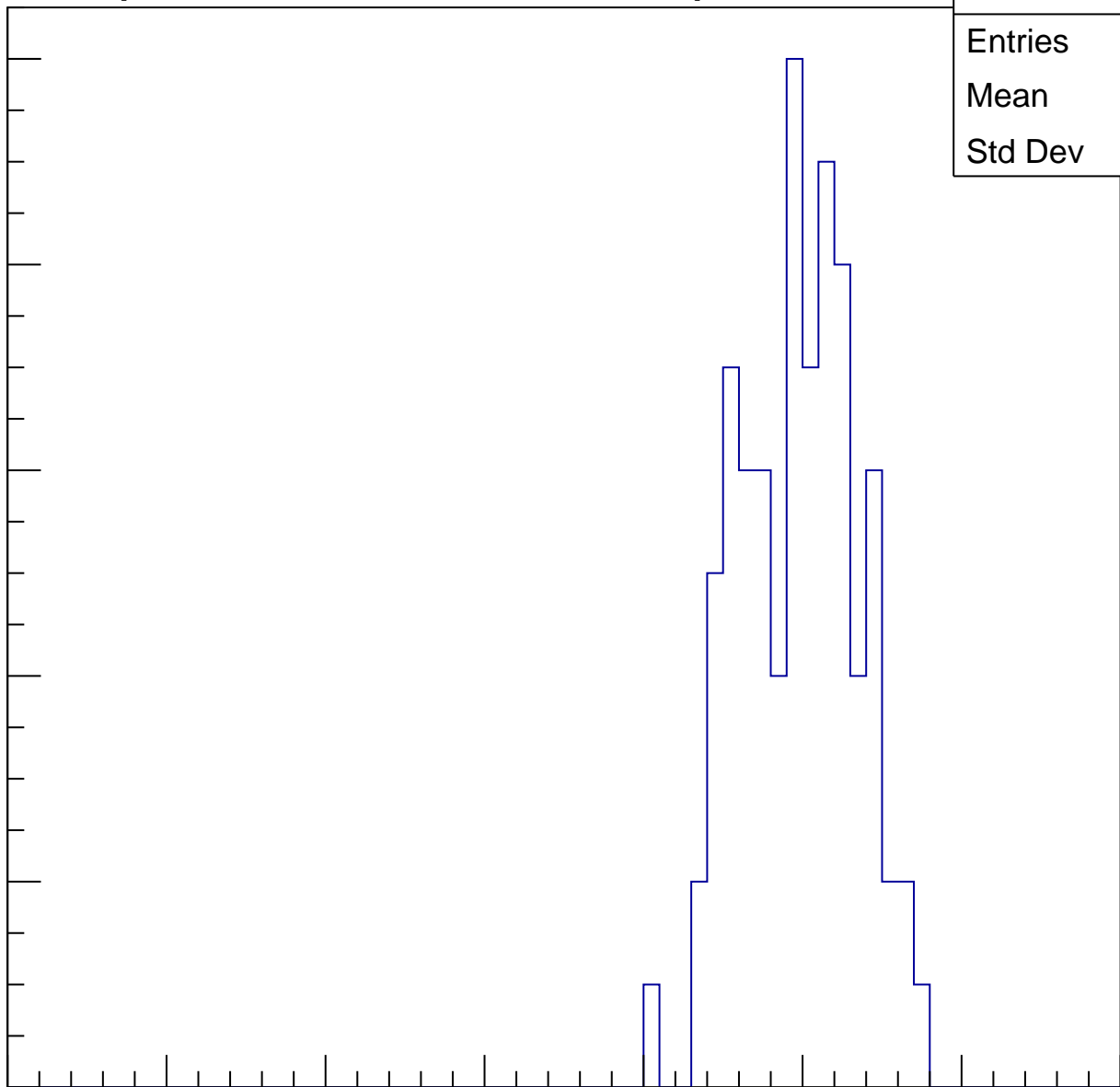
30

40

50

60

ampl

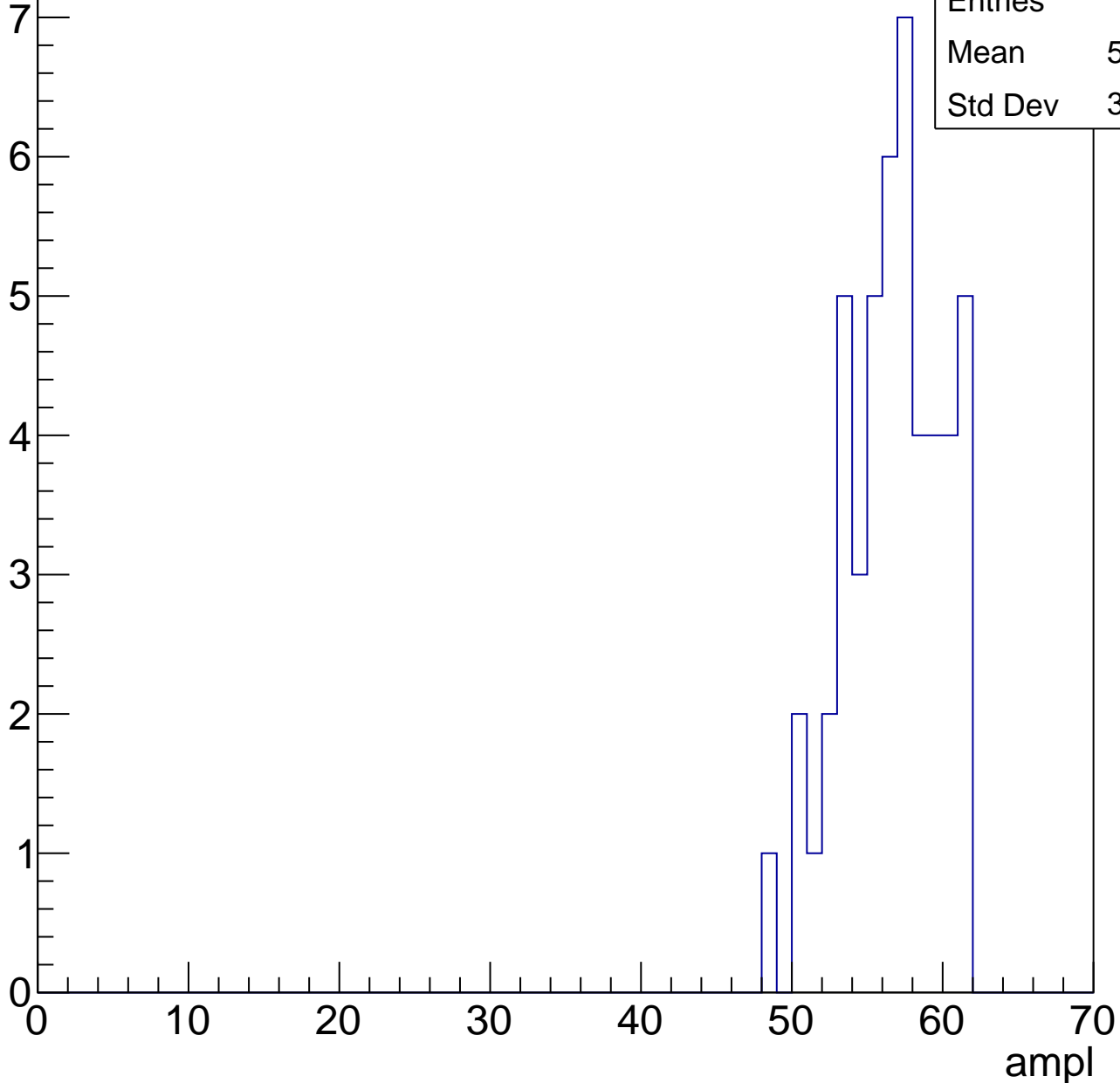


# B1L102S, U16-ch24, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	56.18
Std Dev	3.199

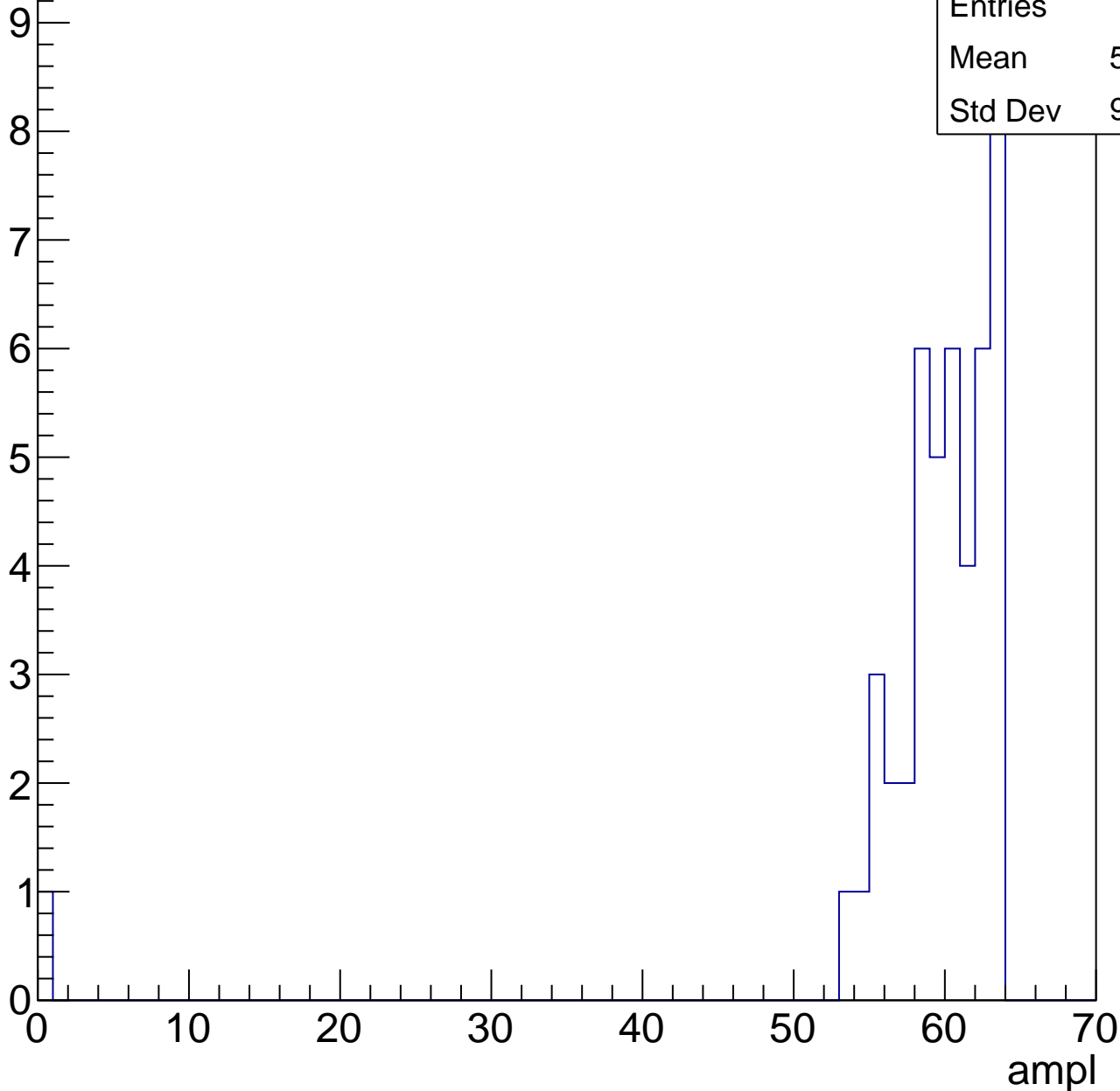


# B1L102S, U16-ch24, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

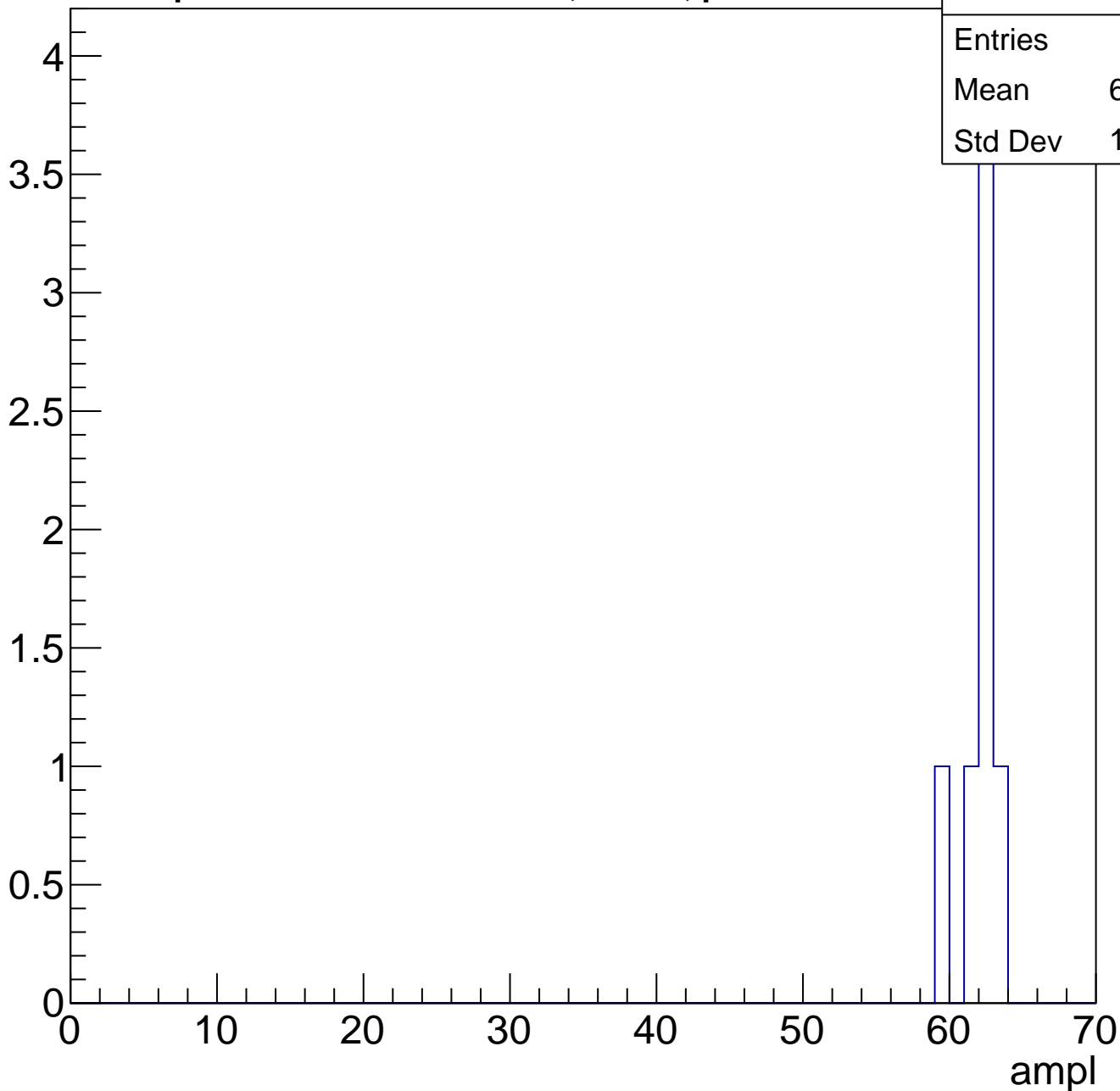
Entries	46
Mean	58.35
Std Dev	9.116



# B1L102S, U16-ch24, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch24, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U16-ch25, adc0

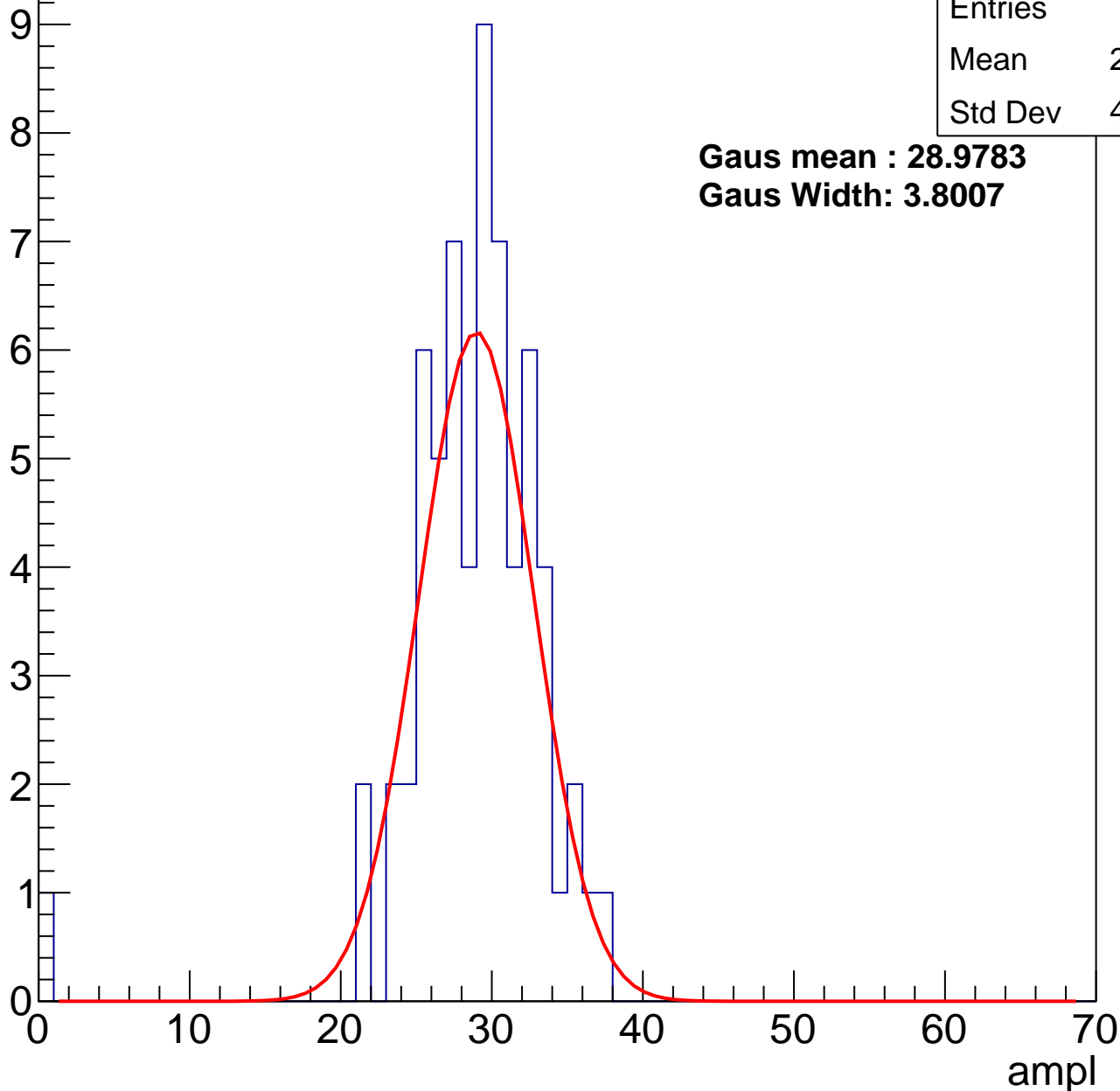
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	28.33
Std Dev	4.978

**Gaus mean : 28.9783**

**Gaus Width: 3.8007**



# B1L102S, U16-ch25, adc1

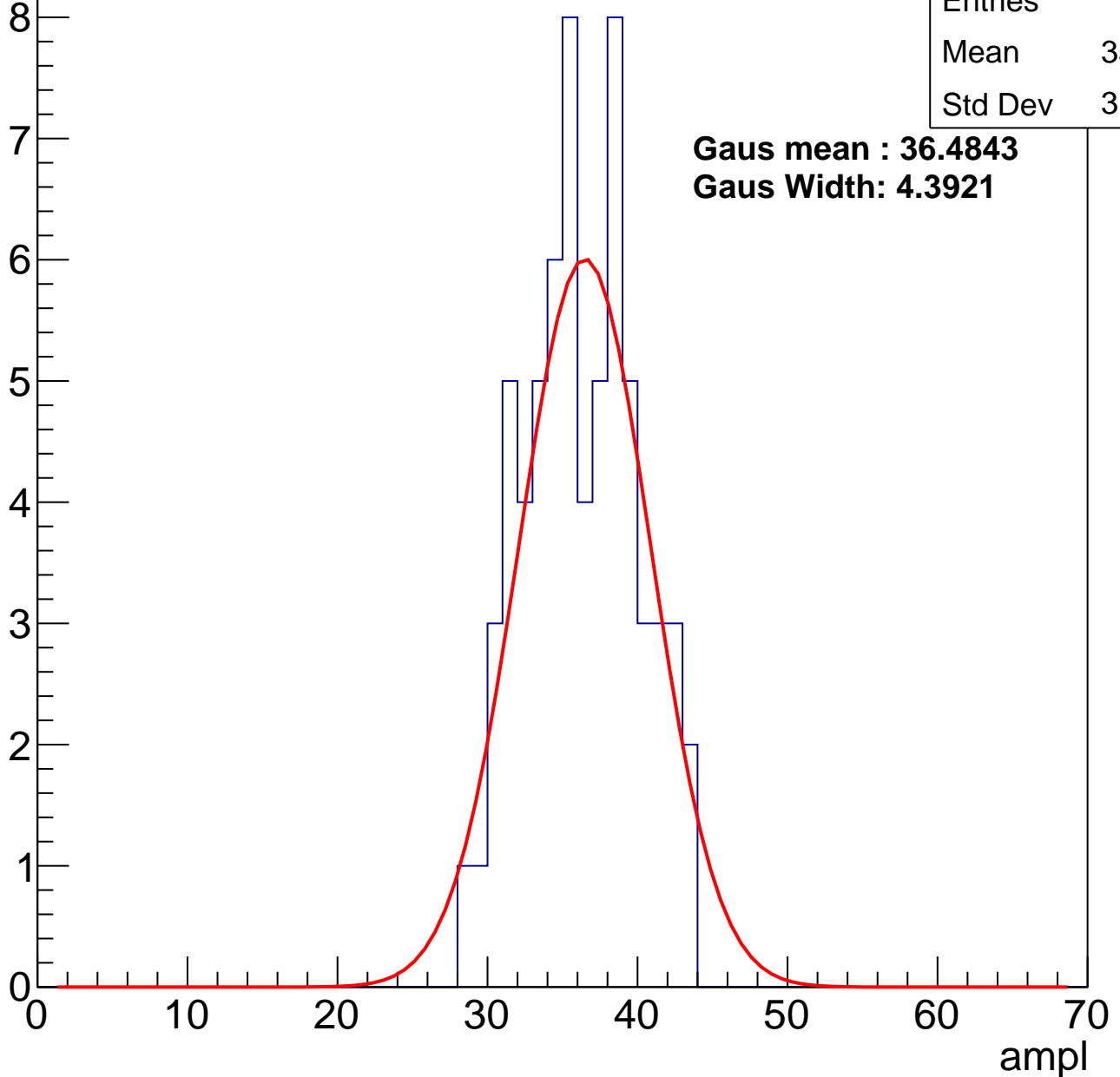
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	35.79
Std Dev	3.683

**Gaus mean : 36.4843**

**Gaus Width: 4.3921**



# B1L102S, U16-ch25, adc2

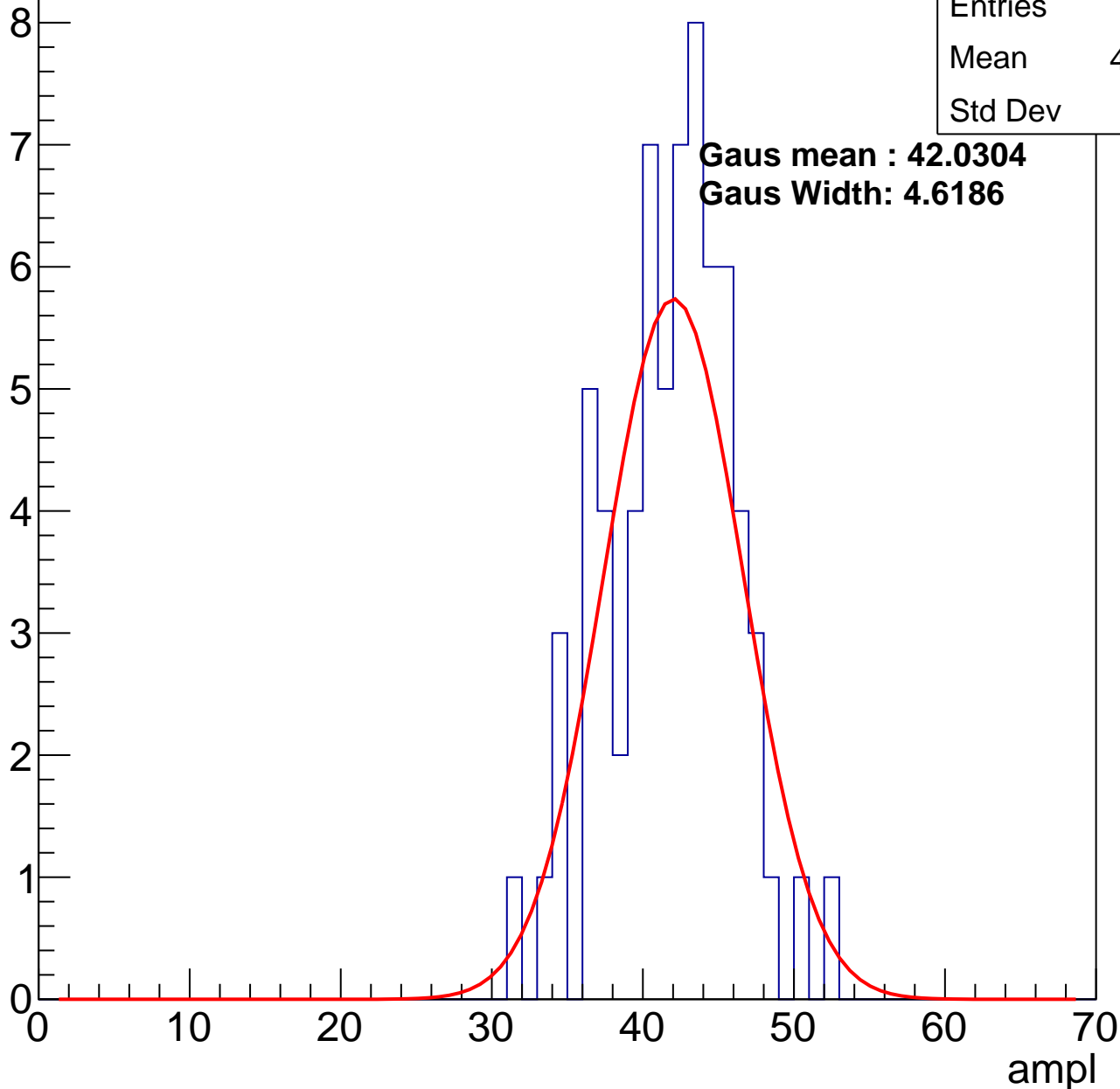
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	41.42
Std Dev	4.13

**Gaus mean : 42.0304**

**Gaus Width: 4.6186**

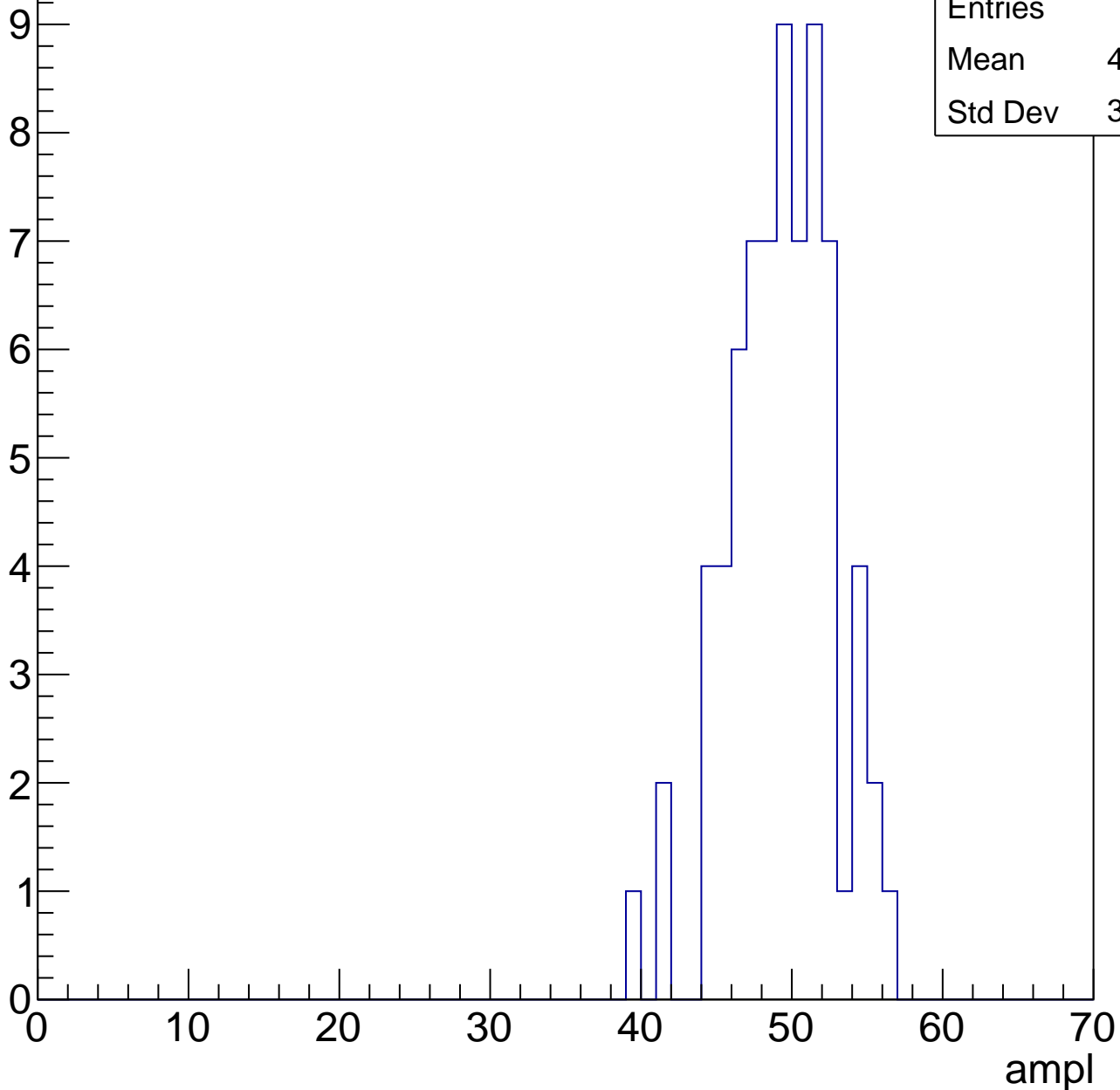


# B1L102S, U16-ch25, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

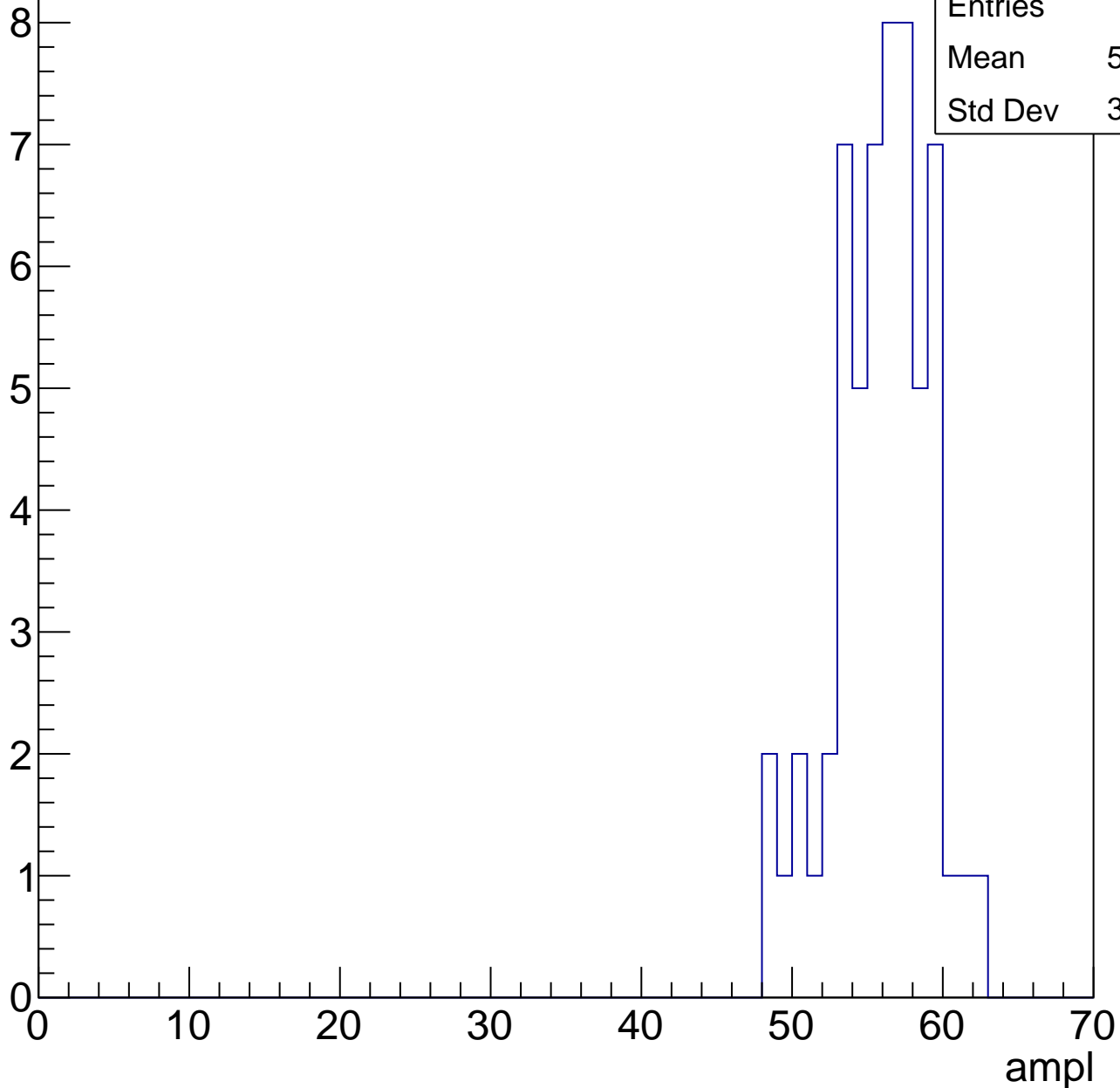
Entries	71
Mean	48.83
Std Dev	3.403



# B1L102S, U16-ch25, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

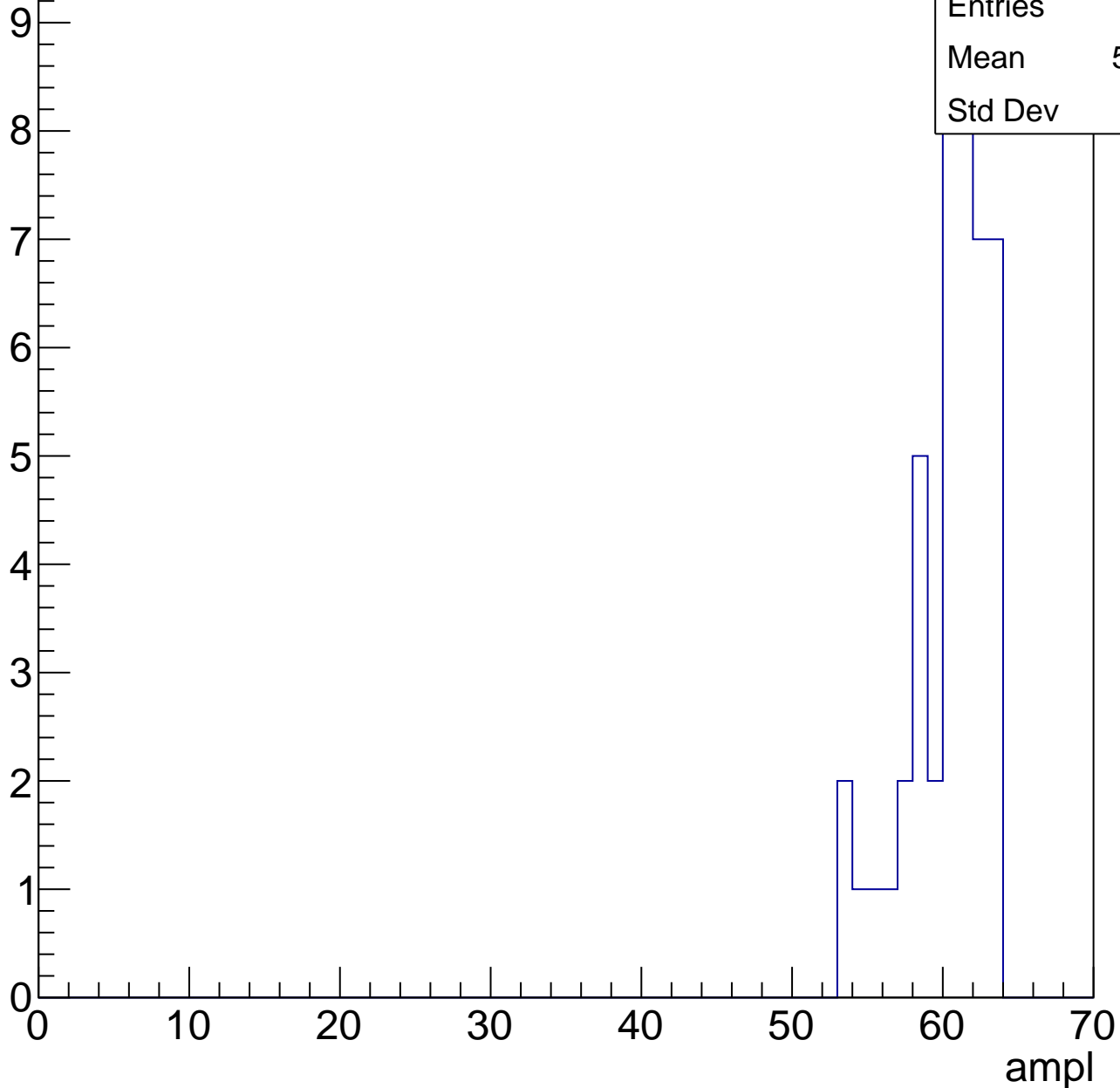


Entries	58
Mean	55.45
Std Dev	3.069

# B1L102S, U16-ch25, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch25, adc6

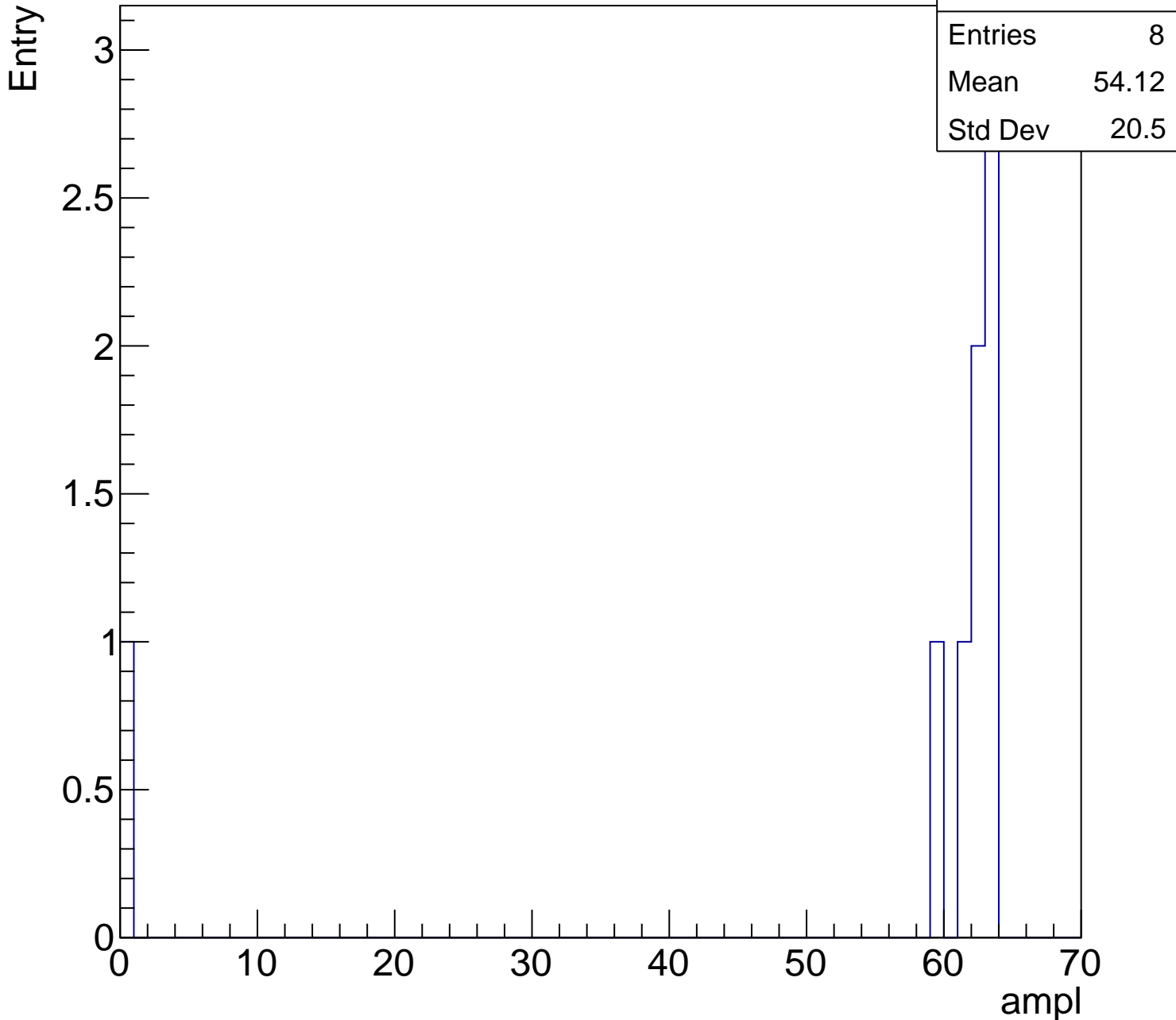
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3  
2.5  
2  
1.5  
1  
0.5  
0

Entries	8
Mean	54.12
Std Dev	20.5

ampl





# B1L102S, U16-ch25, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch26, adc0

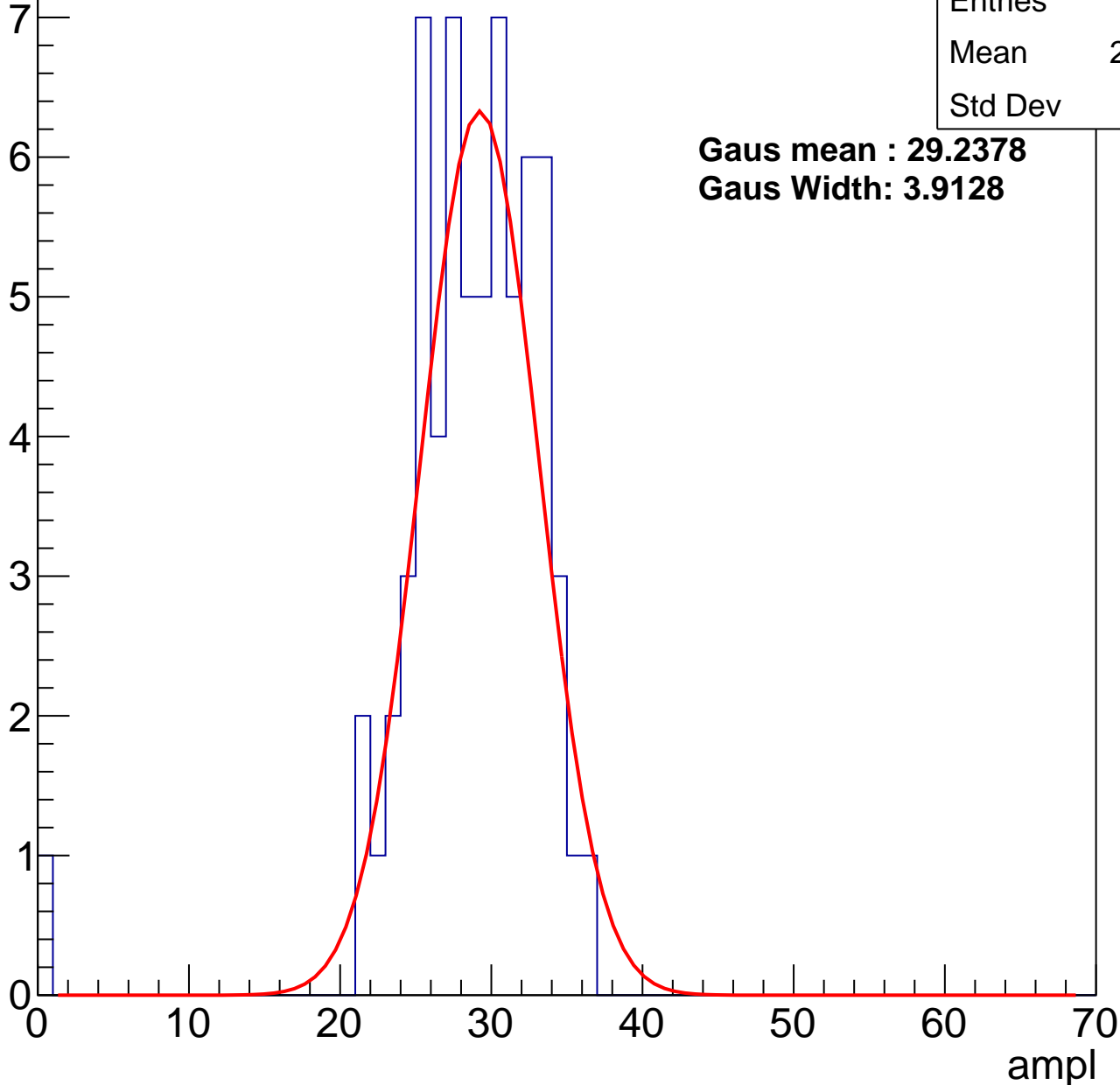
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	28.23
Std Dev	4.99

**Gaus mean : 29.2378**

**Gaus Width: 3.9128**



# B1L102S, U16-ch26, adc1

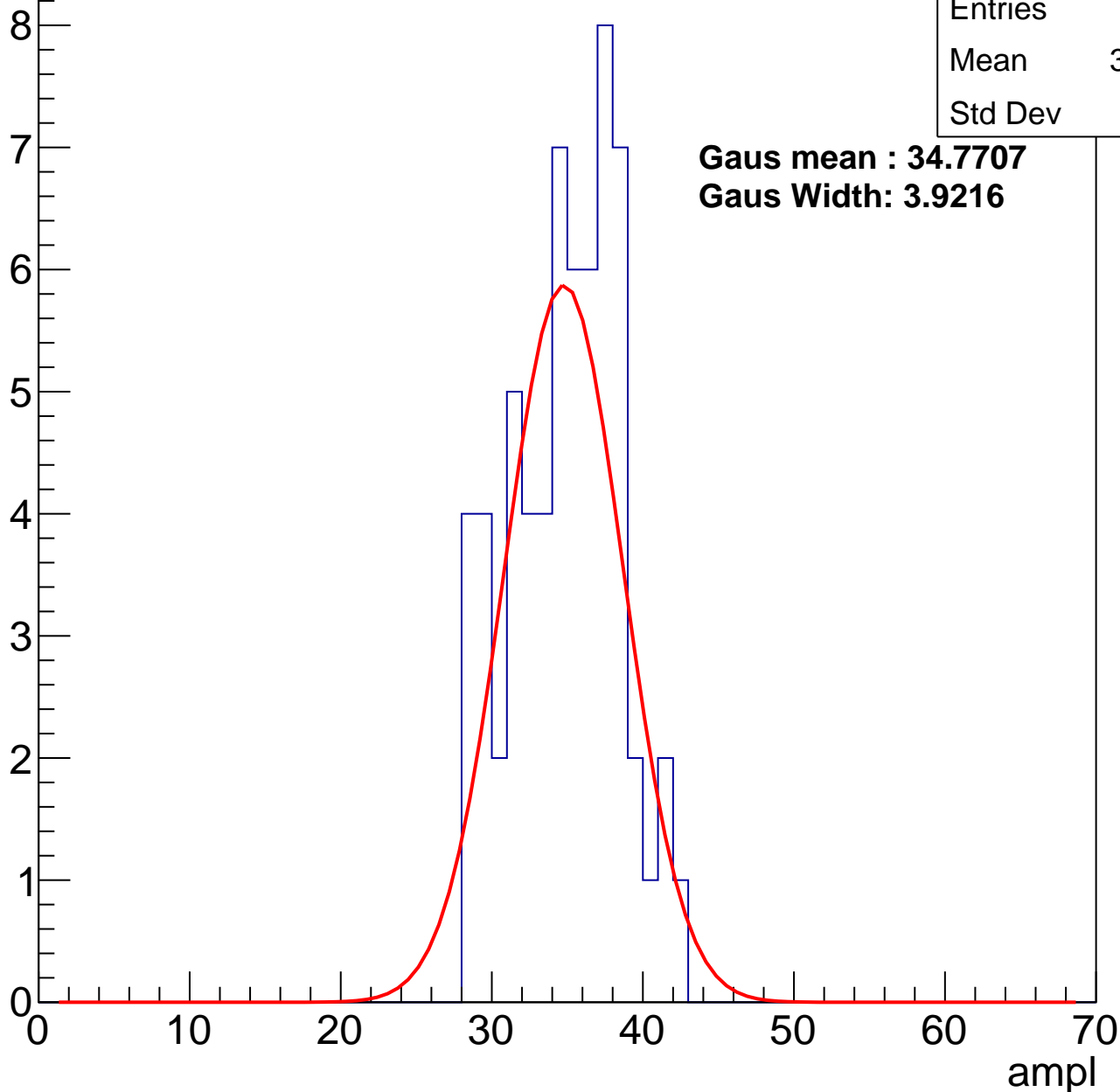
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	34.46
Std Dev	3.54

**Gaus mean : 34.7707**

**Gaus Width: 3.9216**



# B1L102S, U16-ch26, adc2

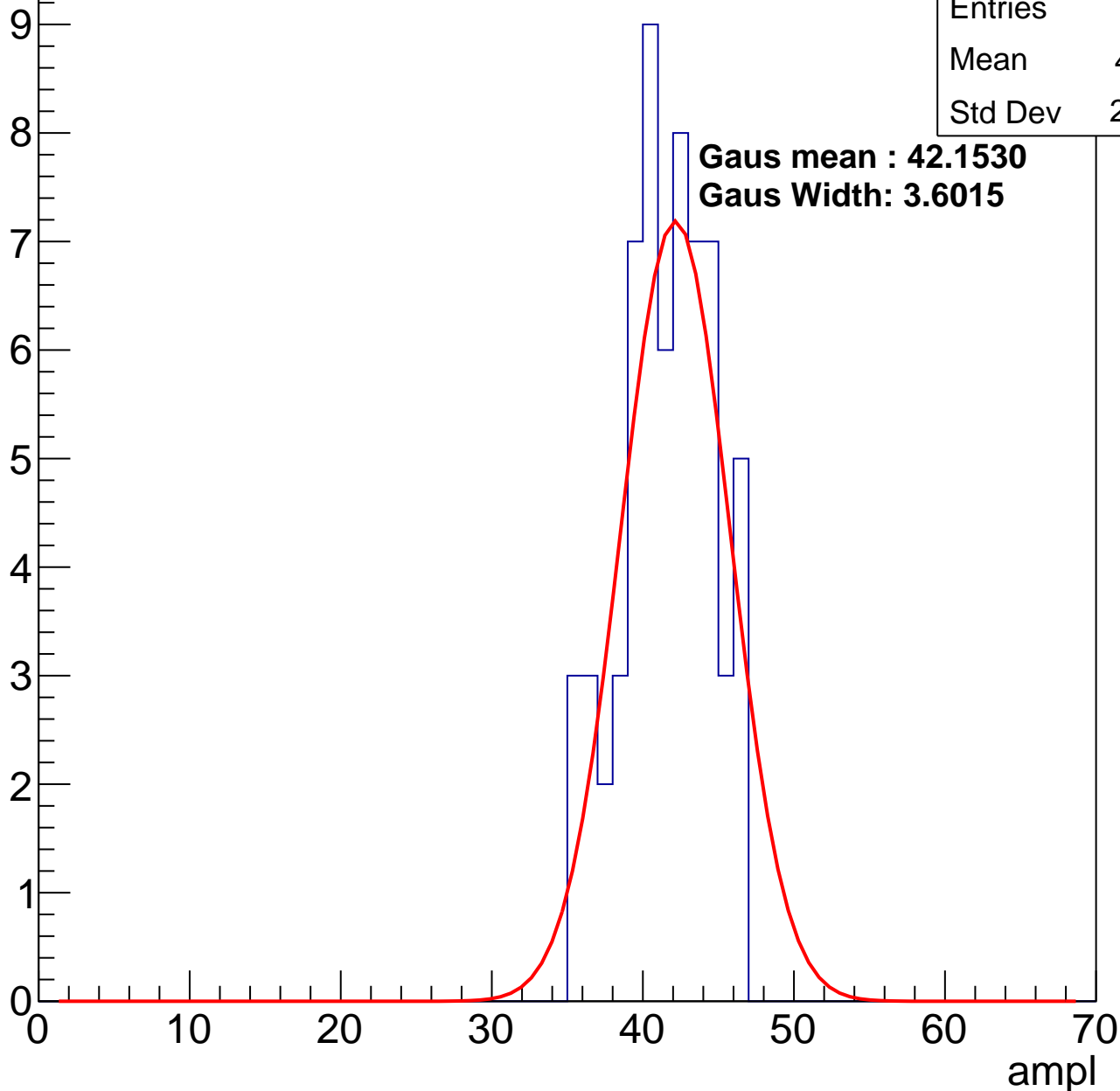
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	41.11
Std Dev	2.955

**Gaus mean : 42.1530**

**Gaus Width: 3.6015**

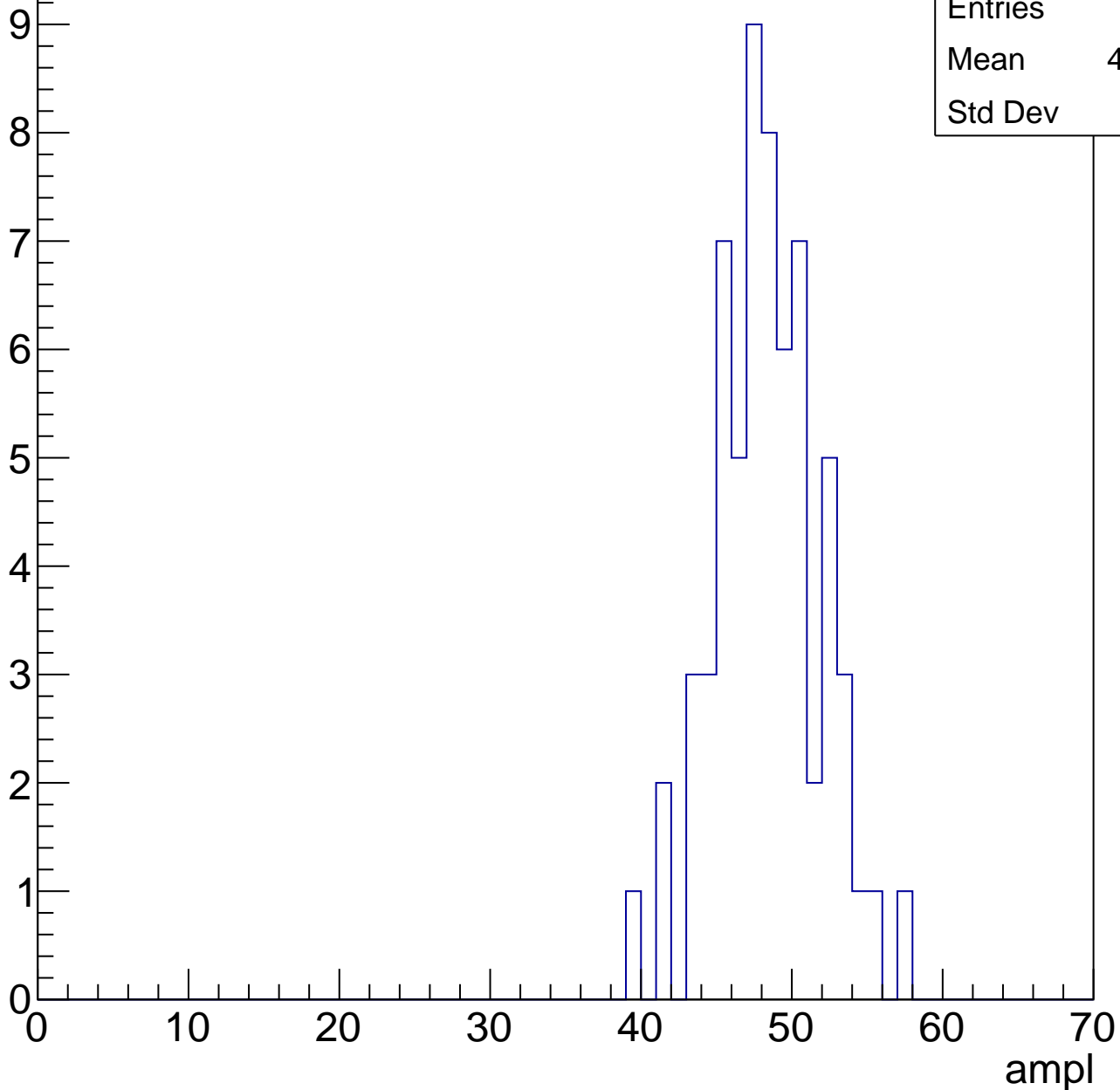


# B1L102S, U16-ch26, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	47.89
Std Dev	3.46

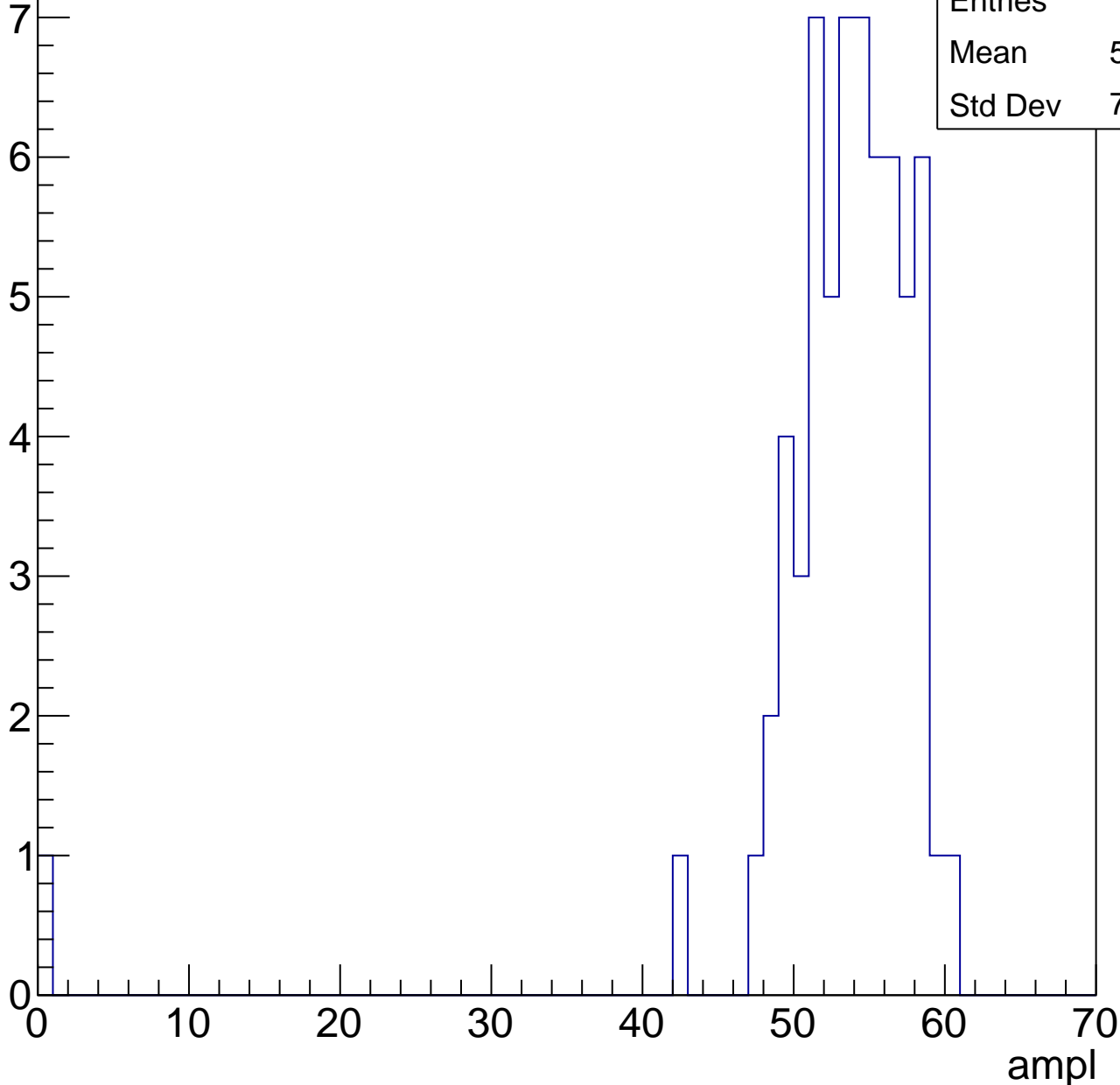


# B1L102S, U16-ch26, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	52.62
Std Dev	7.486



# B1L102S, U16-ch26, adc5

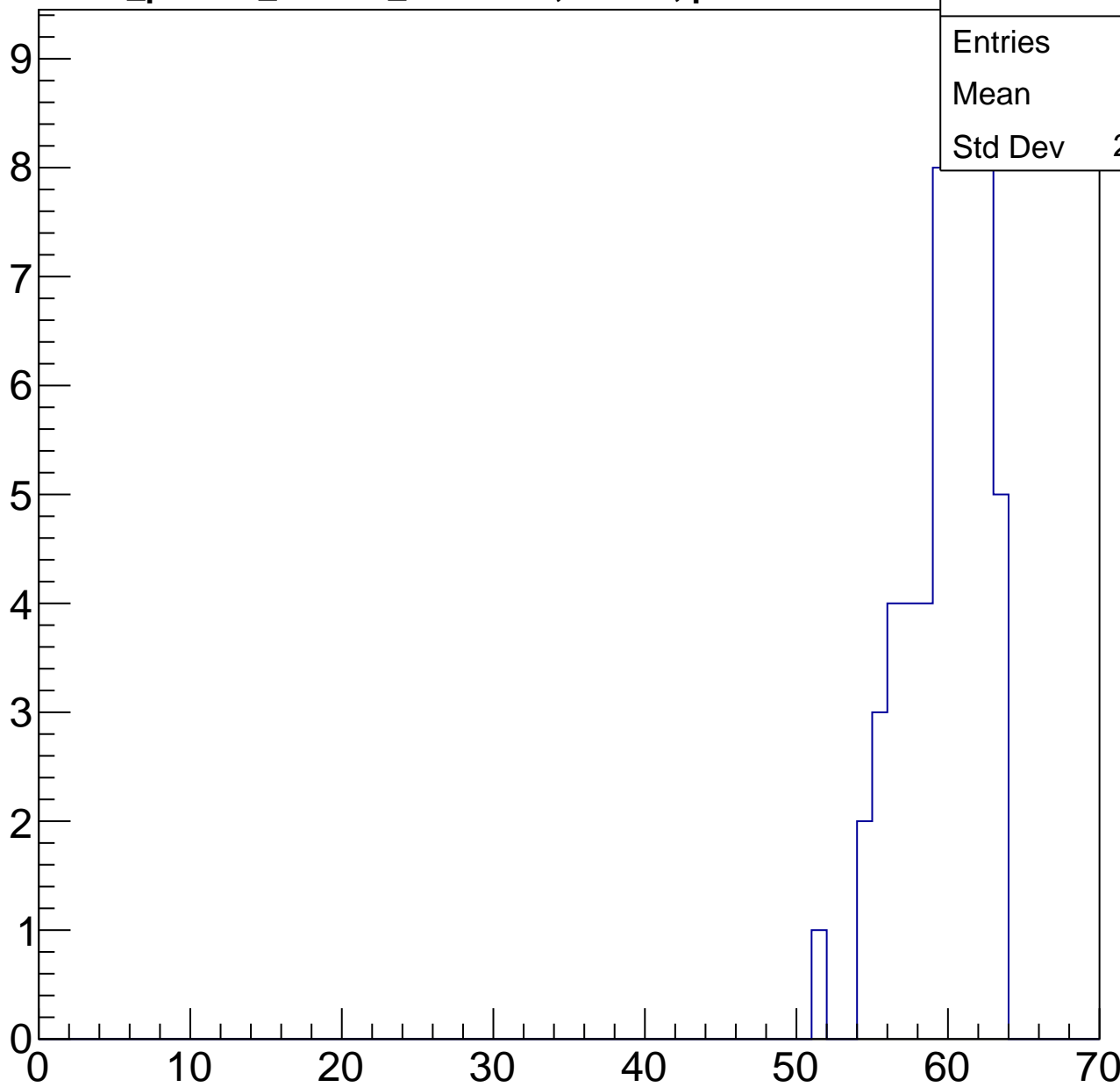
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	56
Mean	59.3
Std Dev	2.718

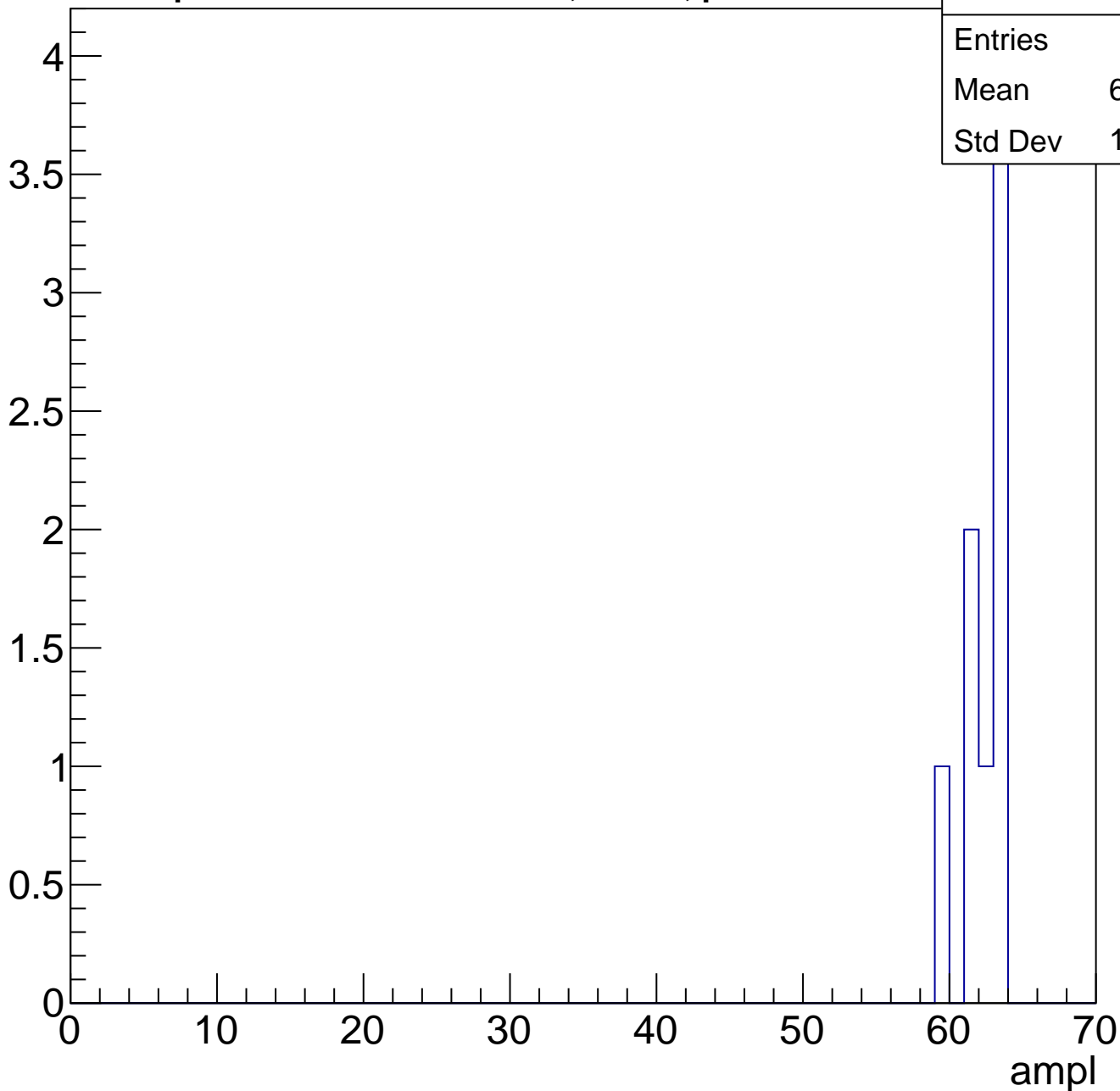
ampl



# B1L102S, U16-ch26, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

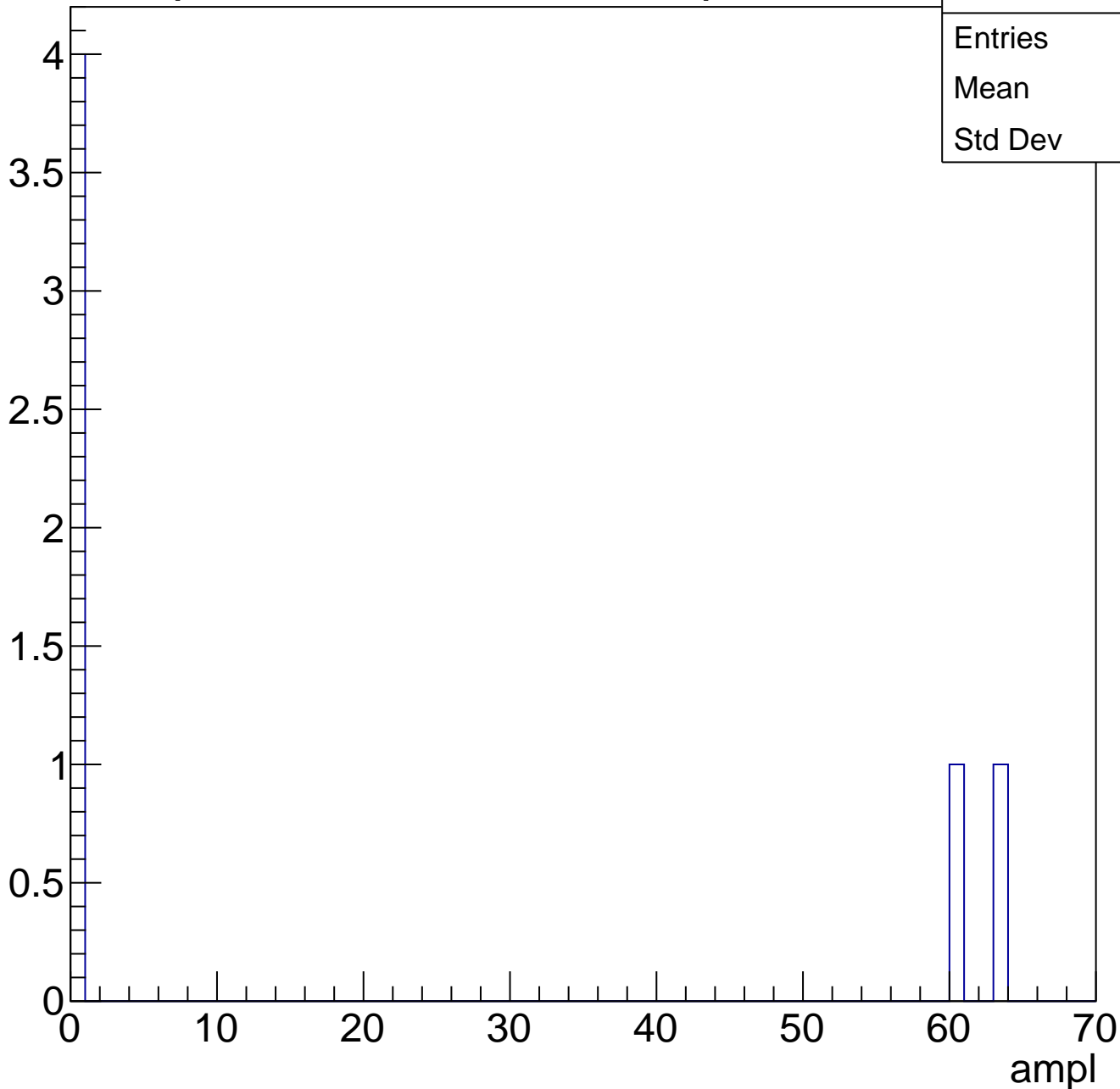




# B1L102S, U16-ch26, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	6
Mean	20.5
Std Dev	29

# B1L102S, U16-ch27, adc0

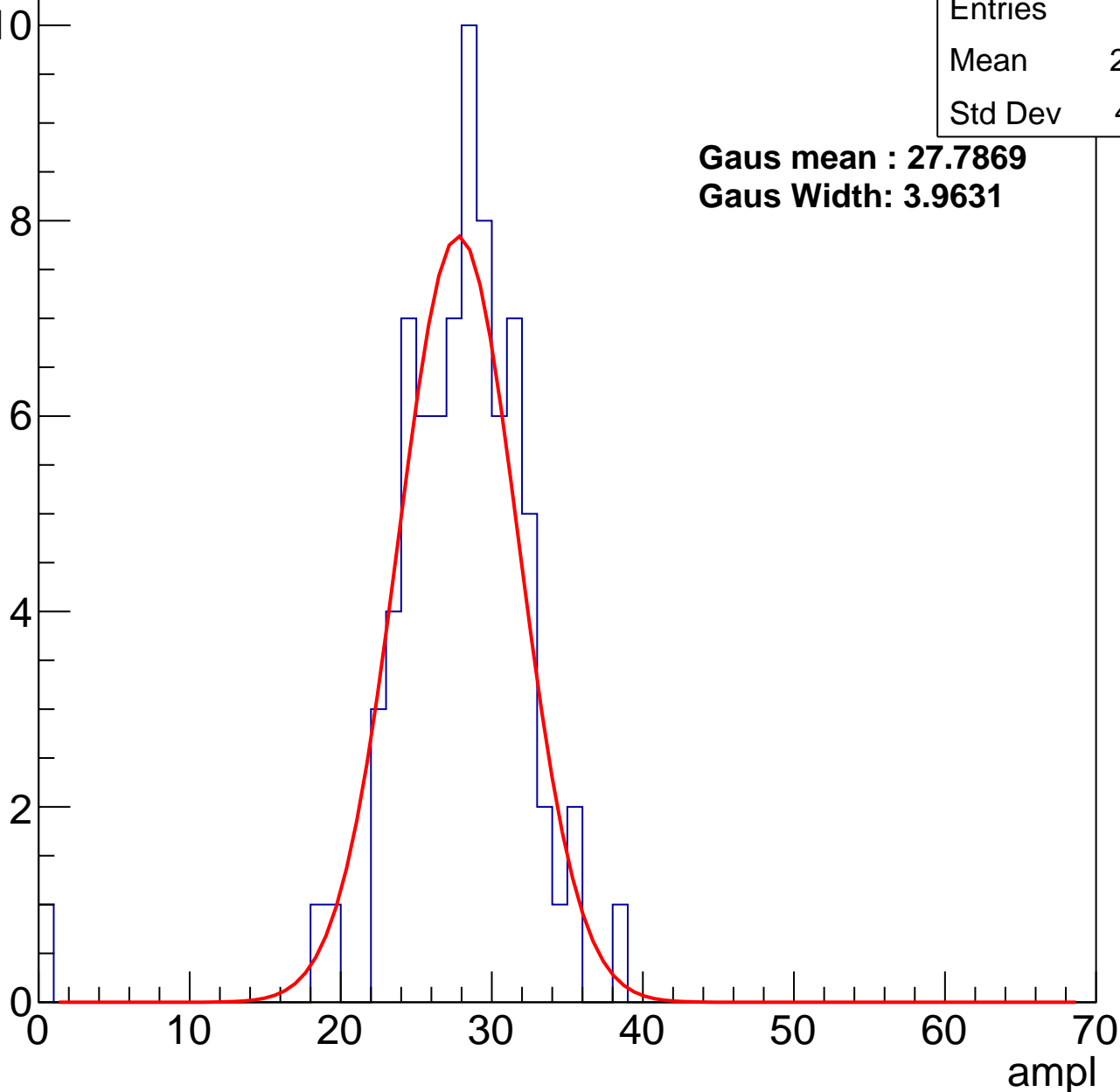
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	27.37
Std Dev	4.801

**Gaus mean : 27.7869**

**Gaus Width: 3.9631**



# B1L102S, U16-ch27, adc1

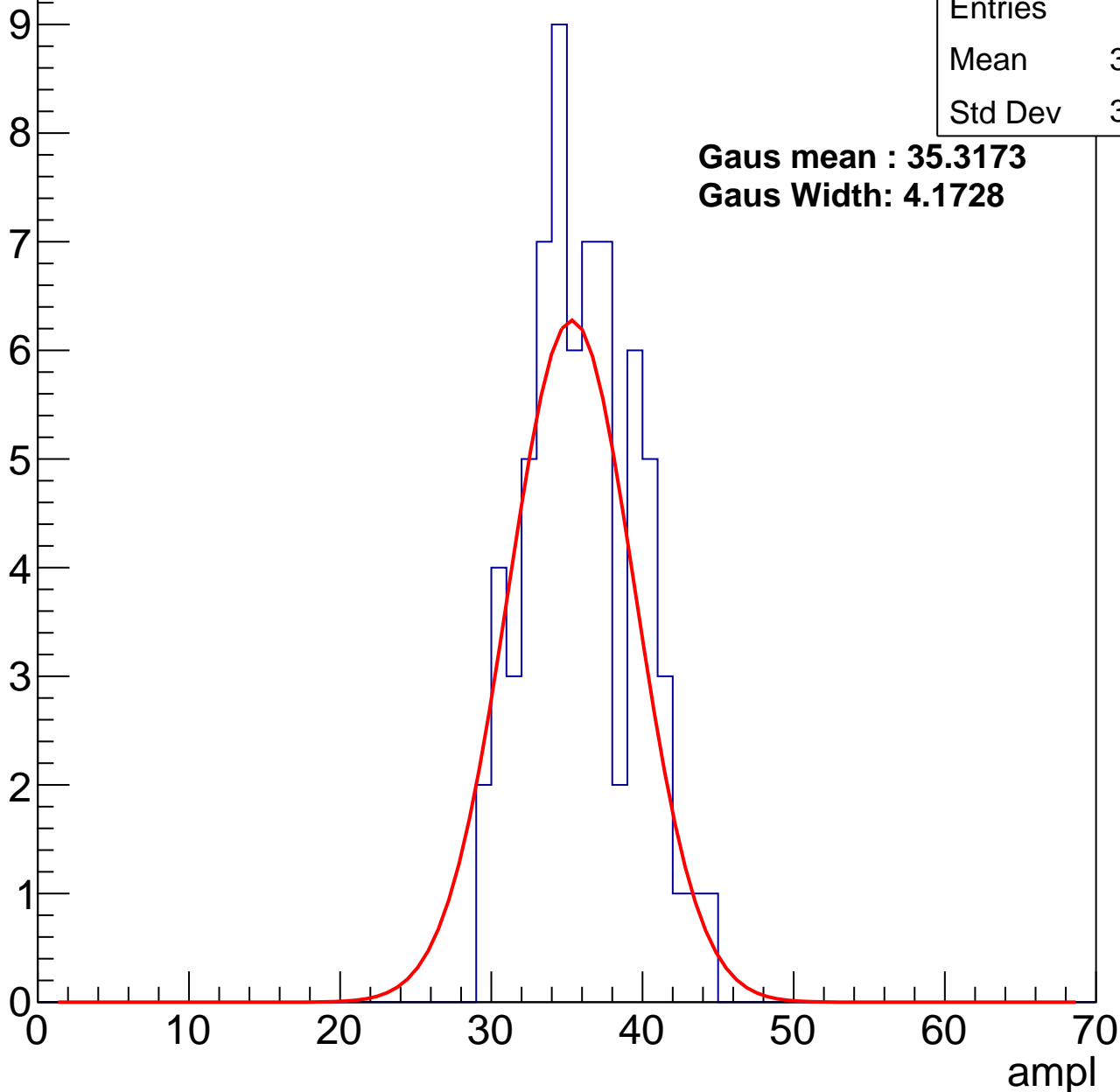
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	35.52
Std Dev	3.529

**Gaus mean : 35.3173**

**Gaus Width: 4.1728**



# B1L102S, U16-ch27, adc2

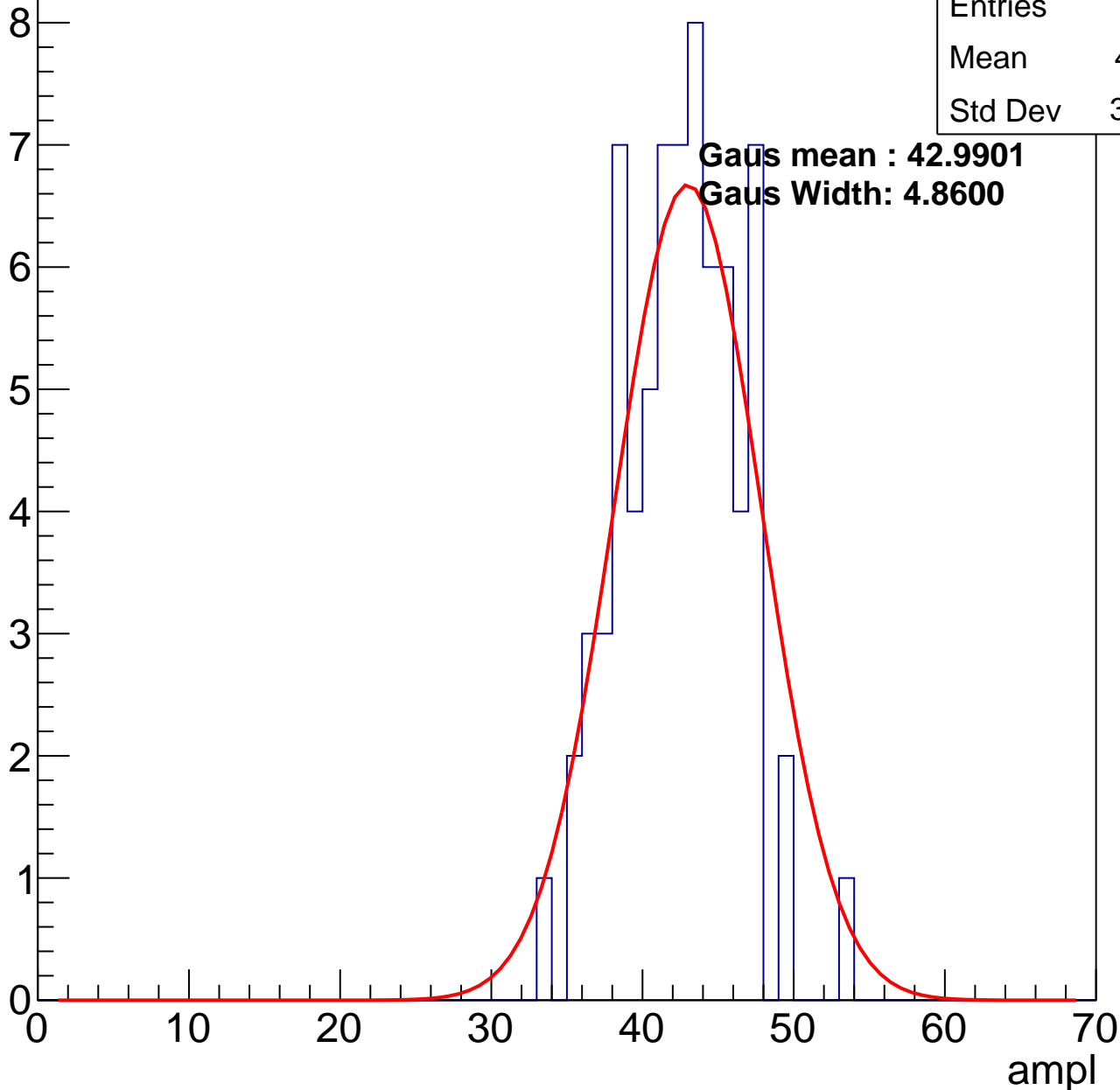
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	42.01
Std Dev	3.848

**Gaus mean : 42.9901**

**Gaus Width: 4.8600**

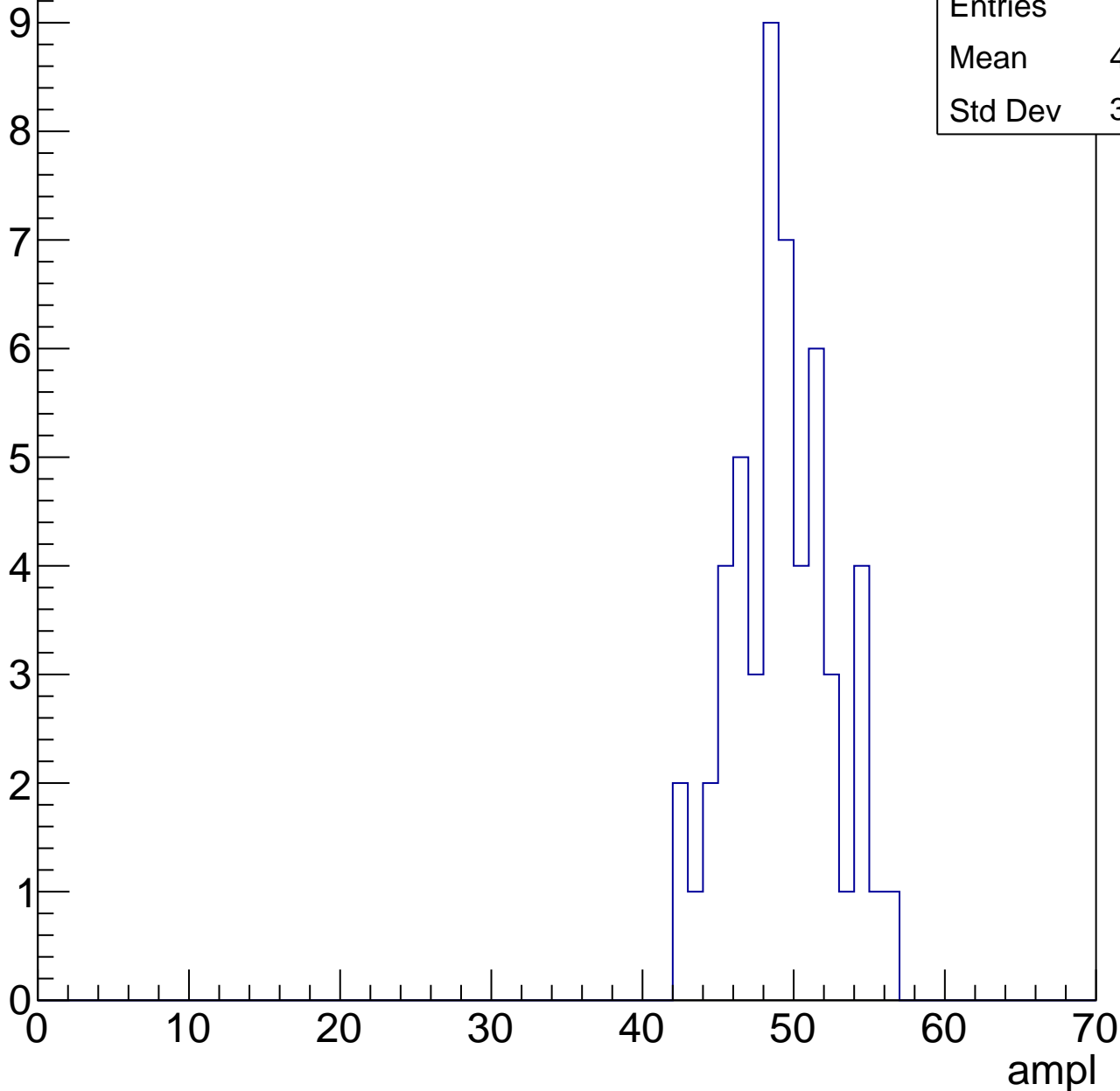


# B1L102S, U16-ch27, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	48.74
Std Dev	3.269

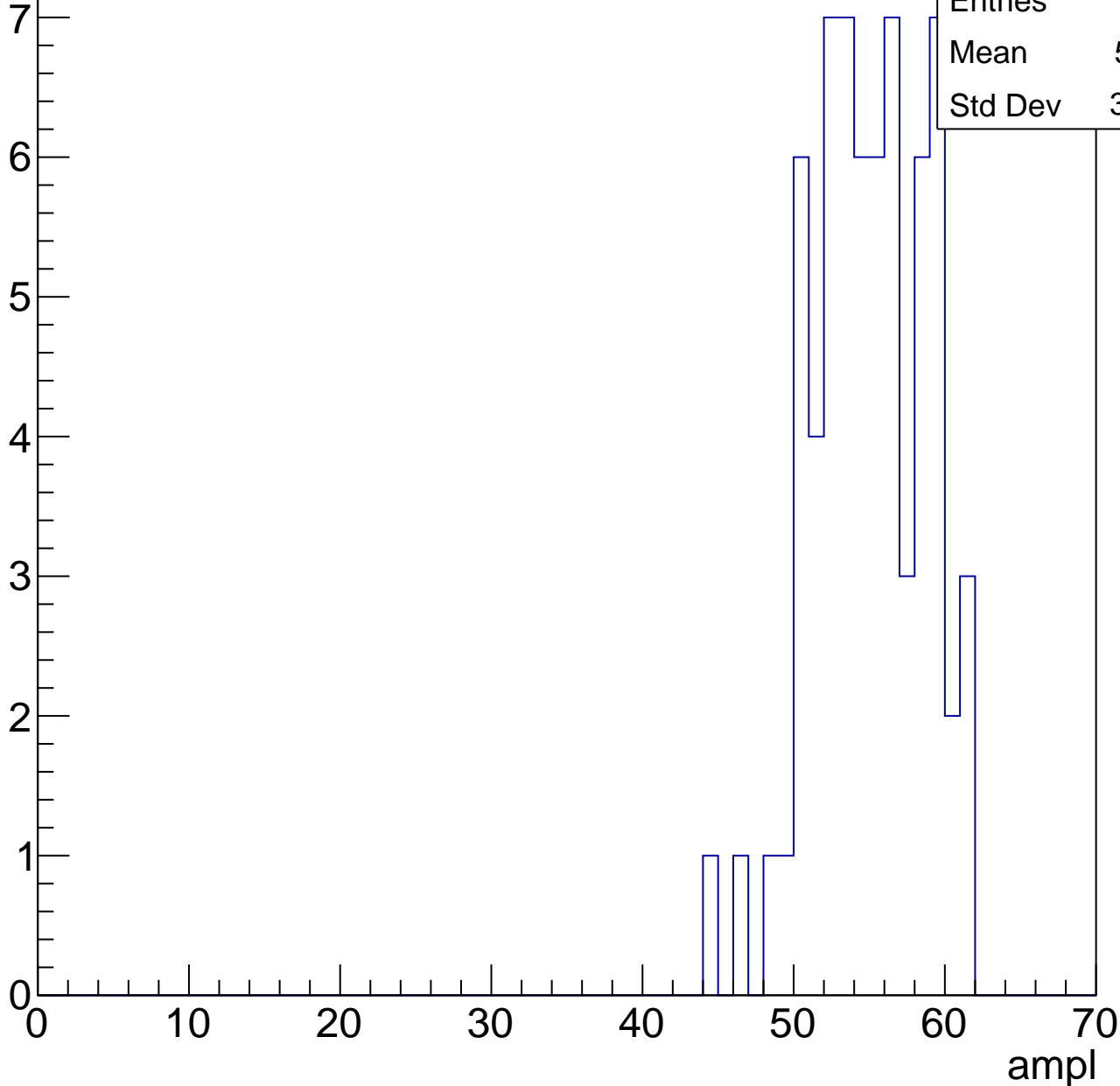


# B1L102S, U16-ch27, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	54.51
Std Dev	3.688

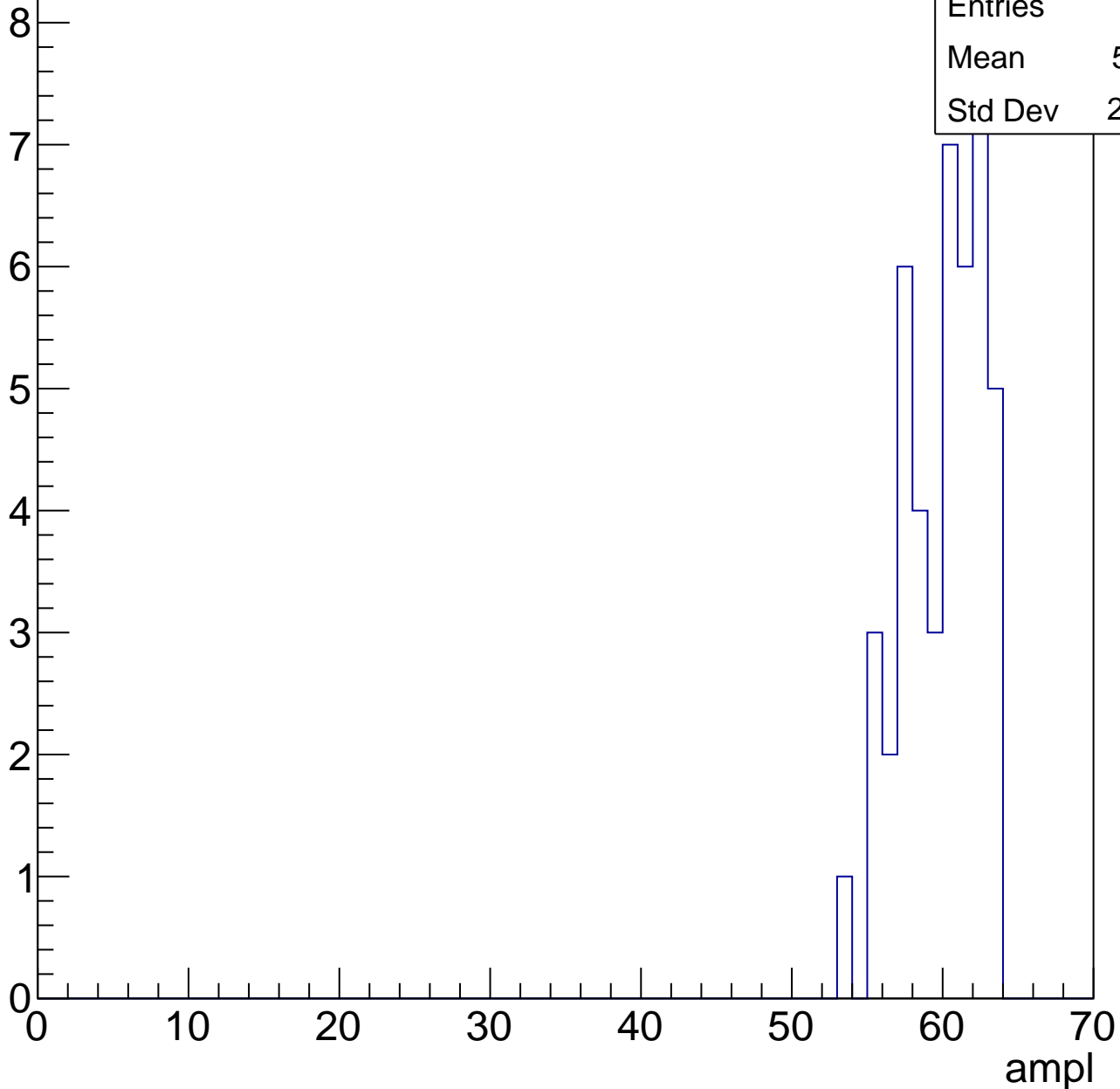


# B1L102S, U16-ch27, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	59.51
Std Dev	2.587

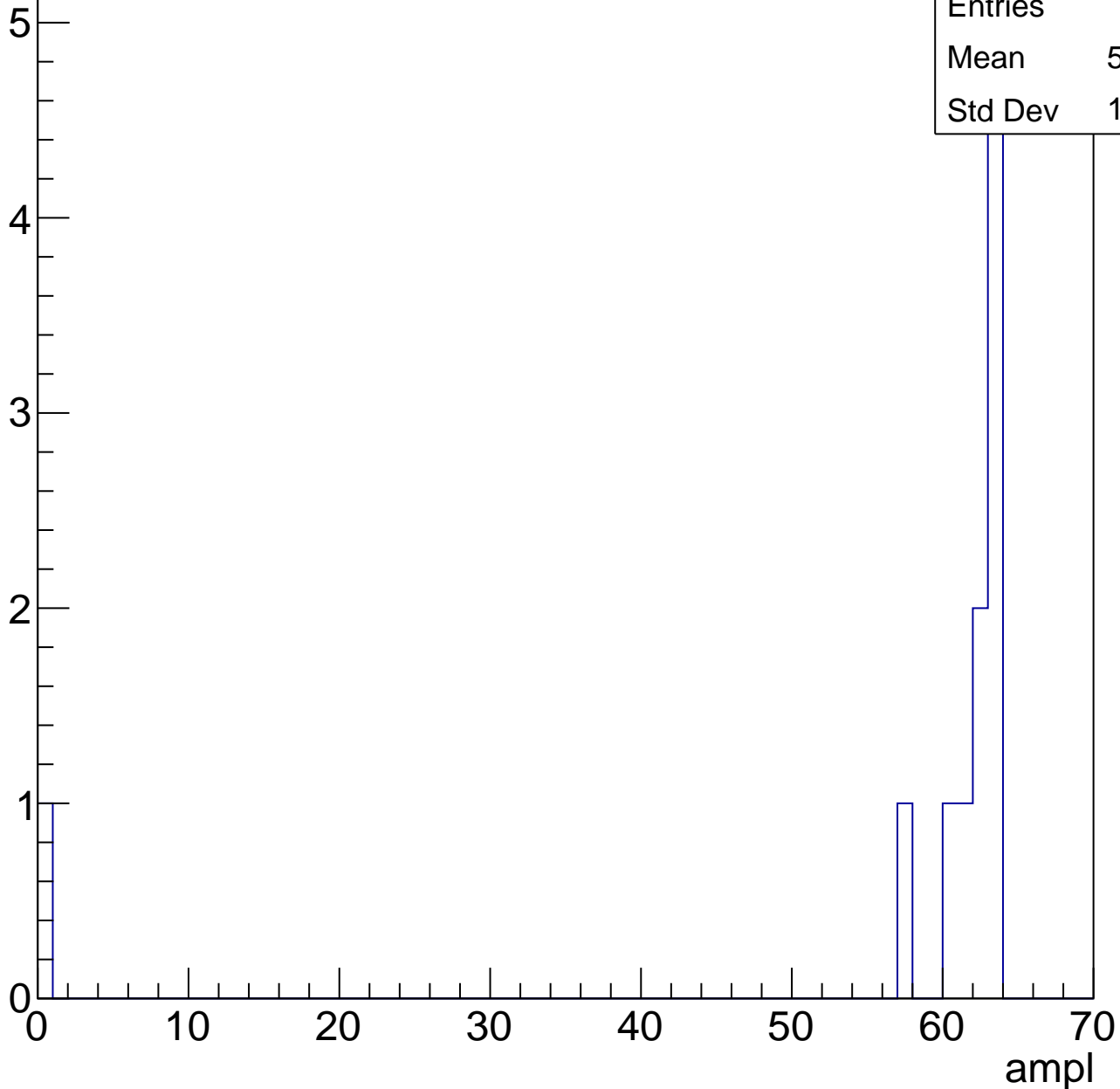


# B1L102S, U16-ch27, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	11
Mean	56.09
Std Dev	17.82





# B1L102S, U16-ch27, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch28, adc0

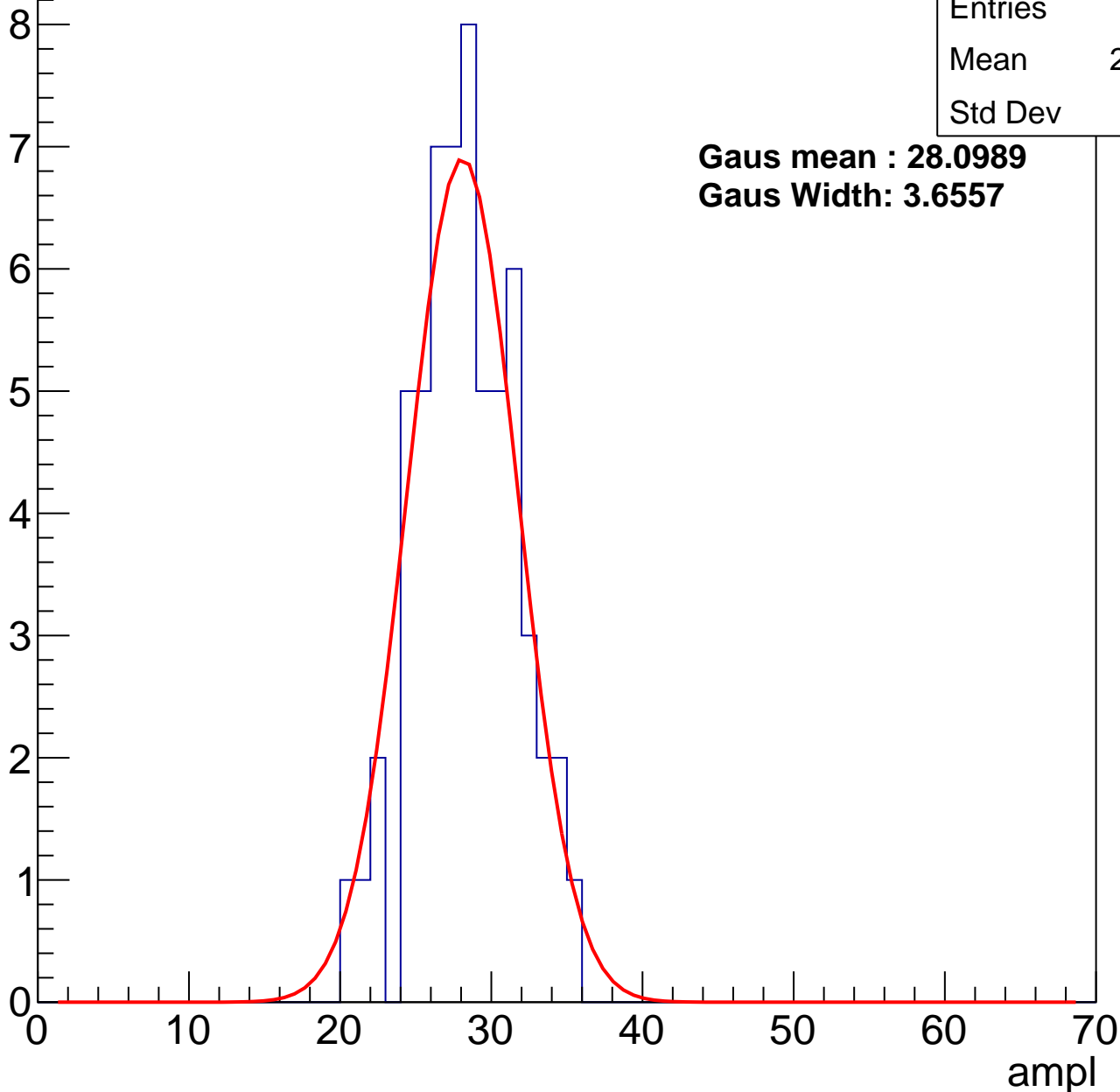
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	27.85
Std Dev	3.27

**Gaus mean : 28.0989**

**Gaus Width: 3.6557**



# B1L102S, U16-ch28, adc1

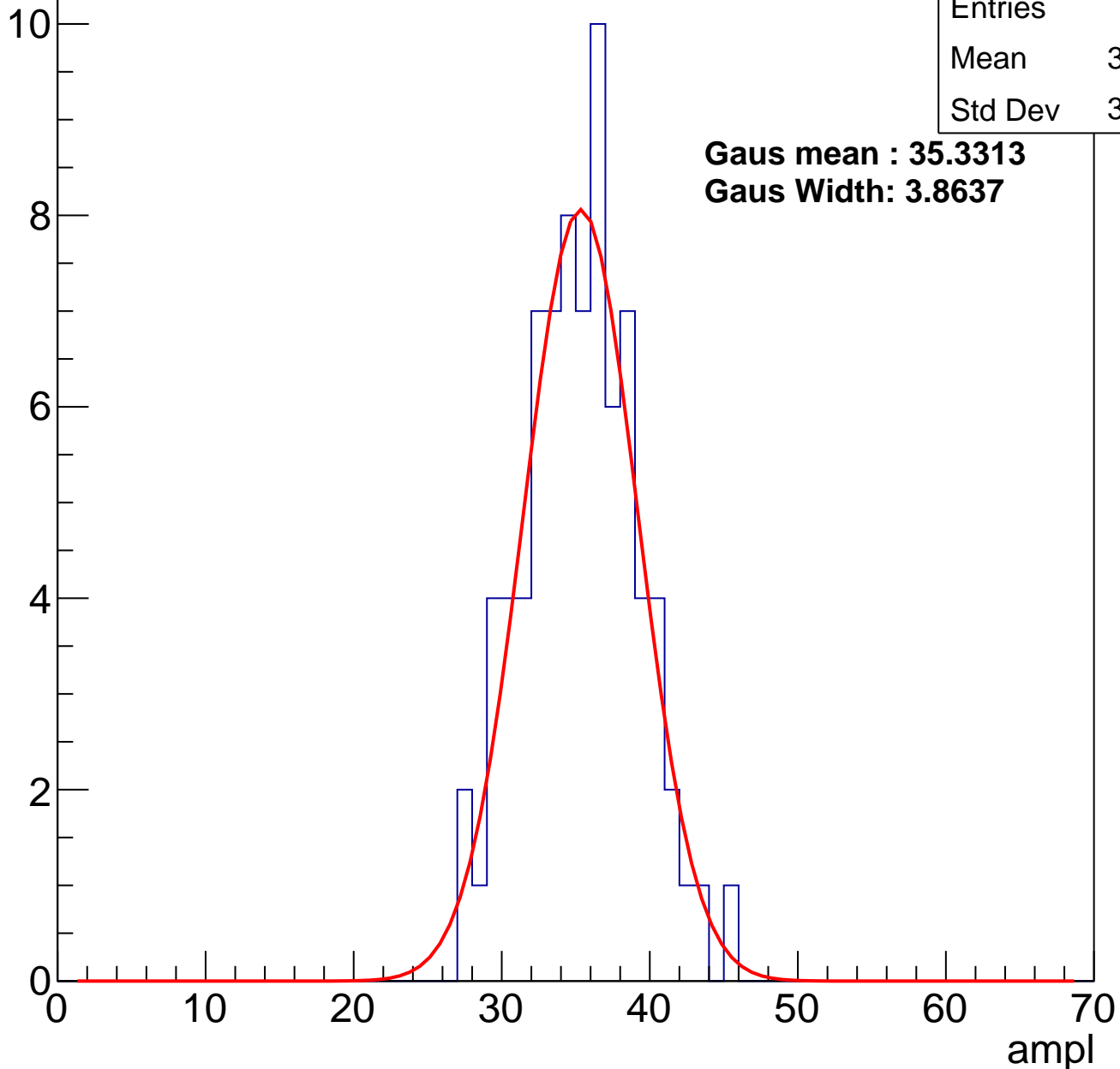
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	80
Mean	34.88
Std Dev	3.756

**Gaus mean : 35.3313**

**Gaus Width: 3.8637**

Entry



# B1L102S, U16-ch28, adc2

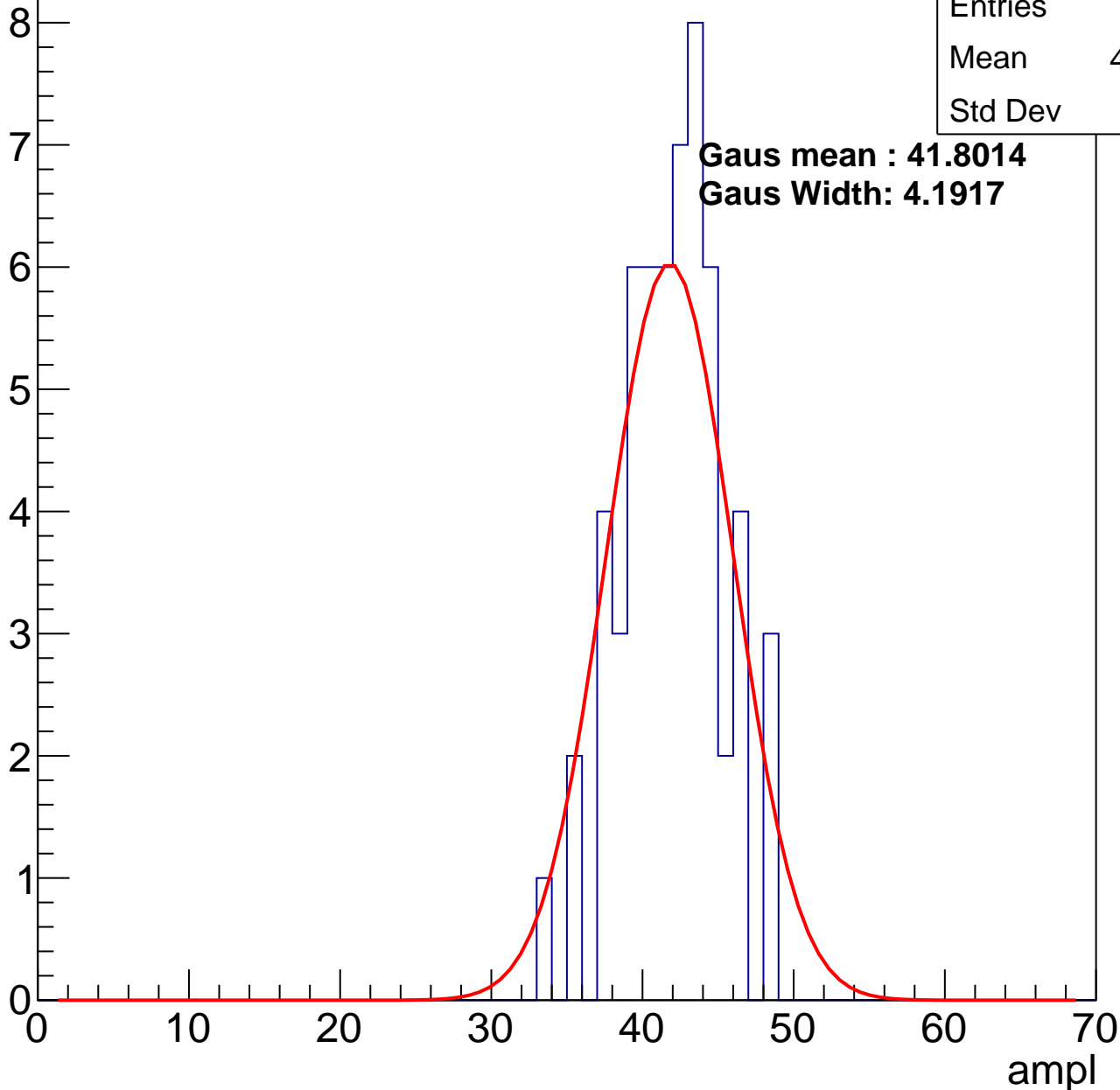
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	41.47
Std Dev	3.26

**Gaus mean : 41.8014**

**Gaus Width: 4.1917**

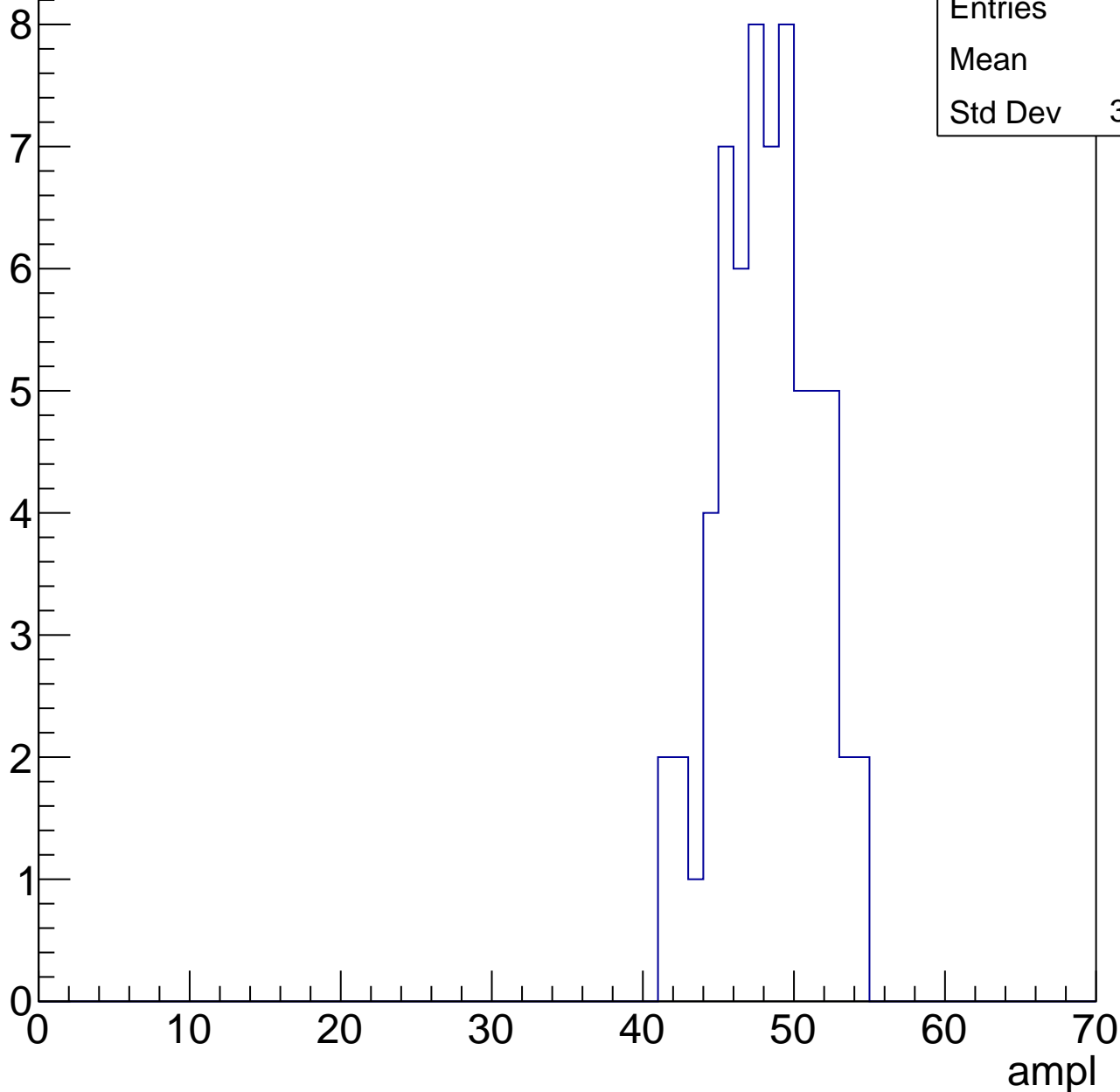


# B1L102S, U16-ch28, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	47.8
Std Dev	3.128

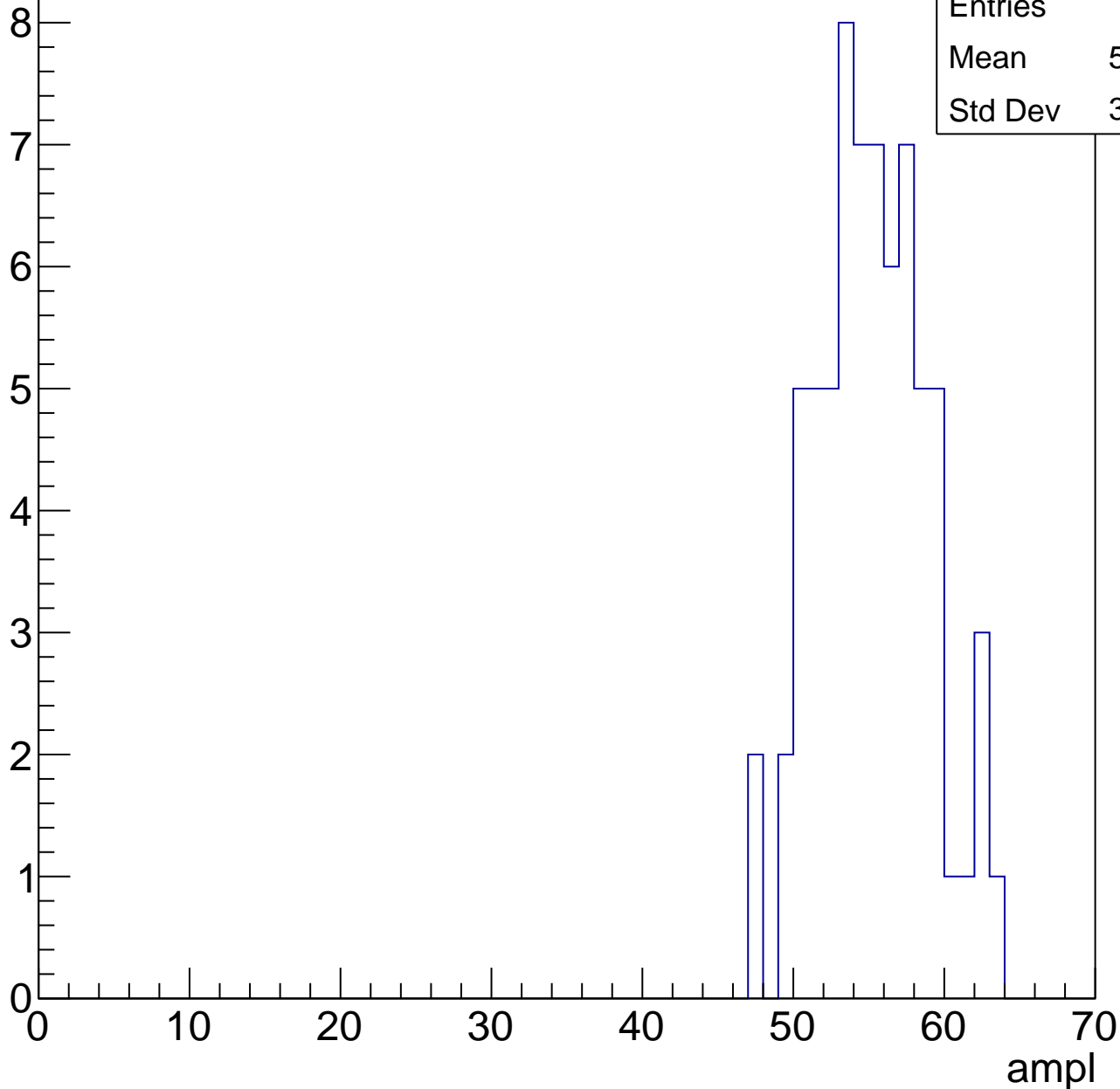


# B1L102S, U16-ch28, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	54.77
Std Dev	3.618

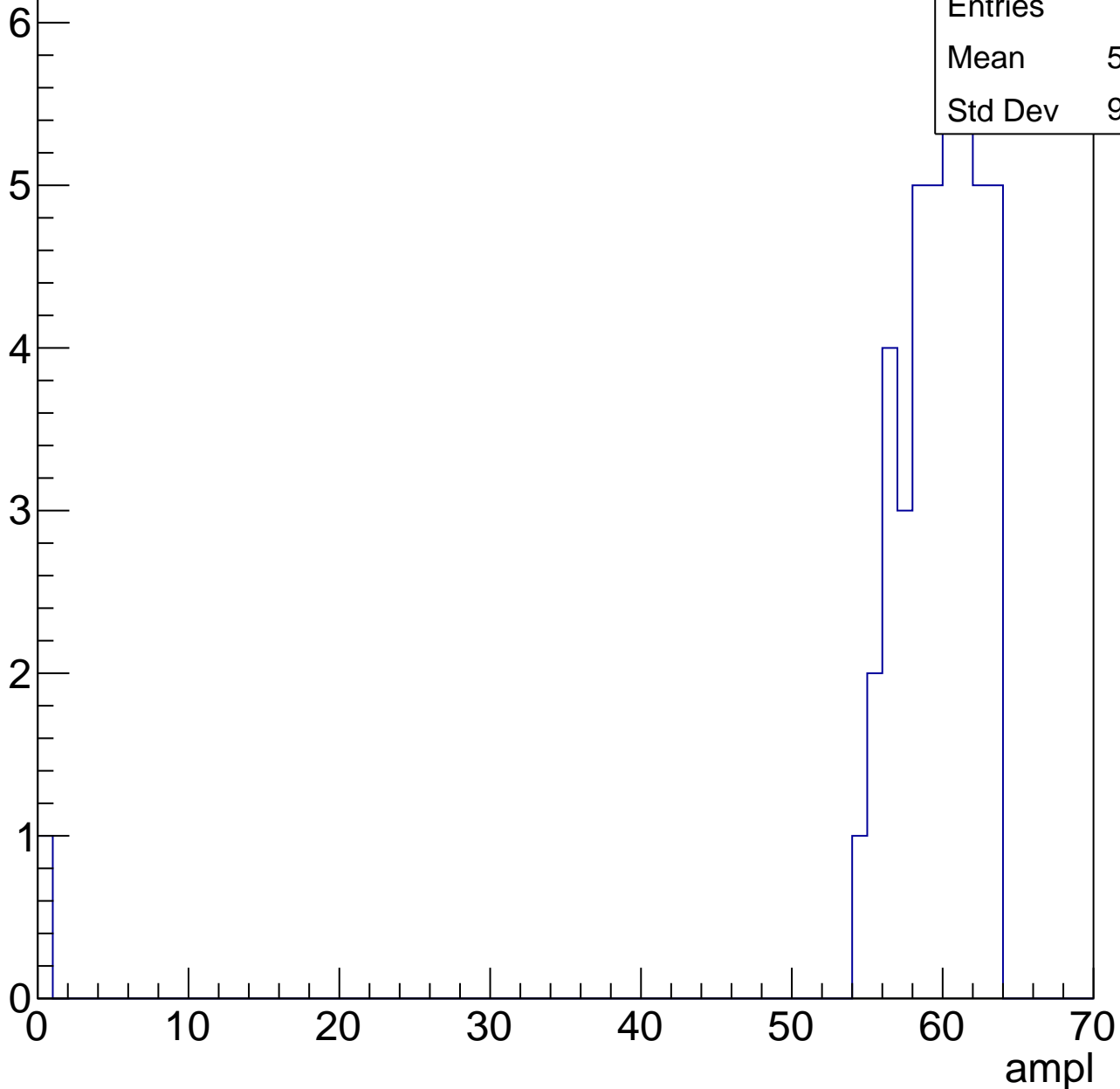


# B1L102S, U16-ch28, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	43
Mean	58.02
Std Dev	9.282



# B1L102S, U16-ch28, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries	12
Mean	60.92
Std Dev	2.1



# B1L102S, U16-ch28, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch29, adc0

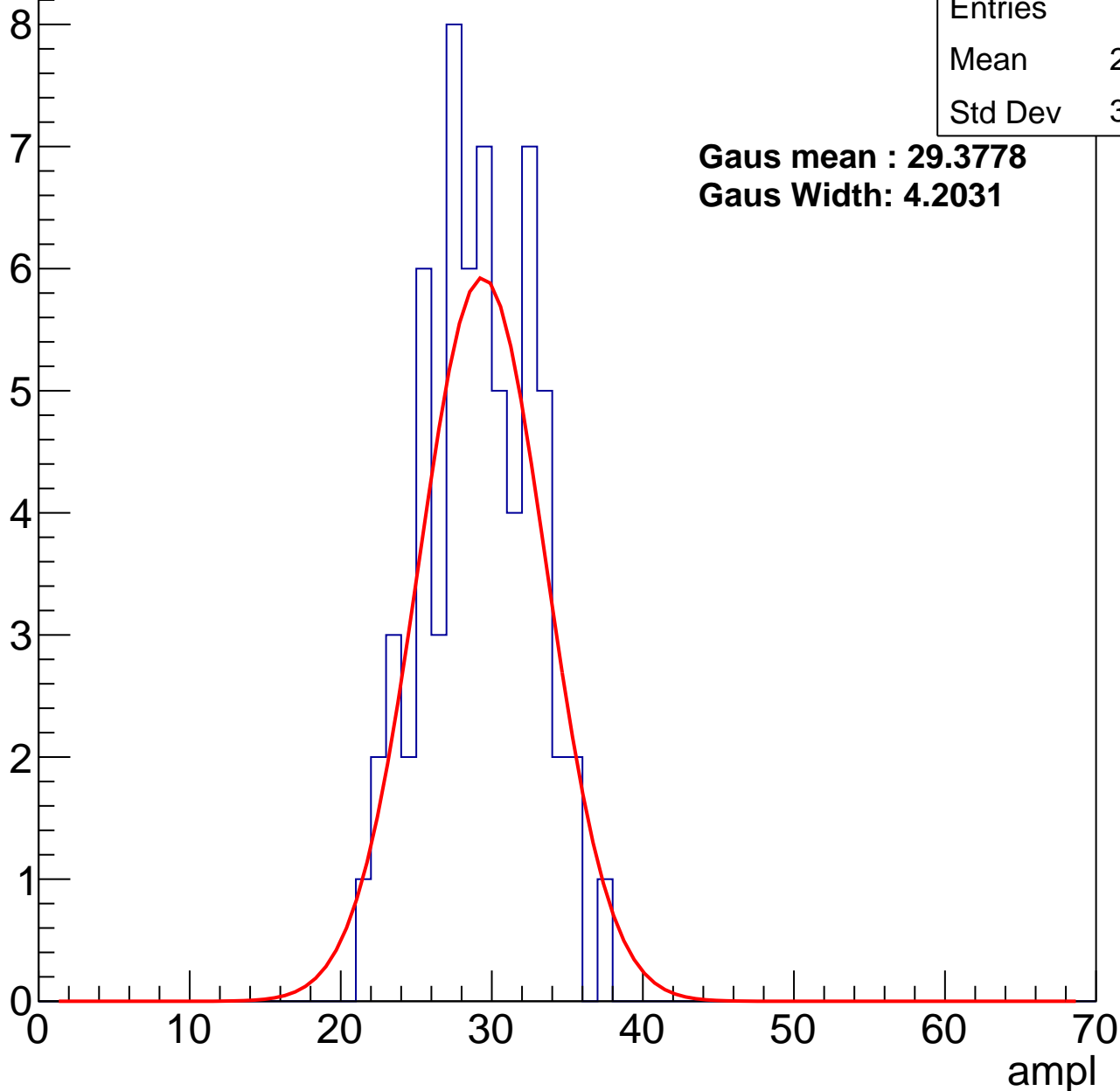
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	28.67
Std Dev	3.588

**Gaus mean : 29.3778**

**Gaus Width: 4.2031**



# B1L102S, U16-ch29, adc1

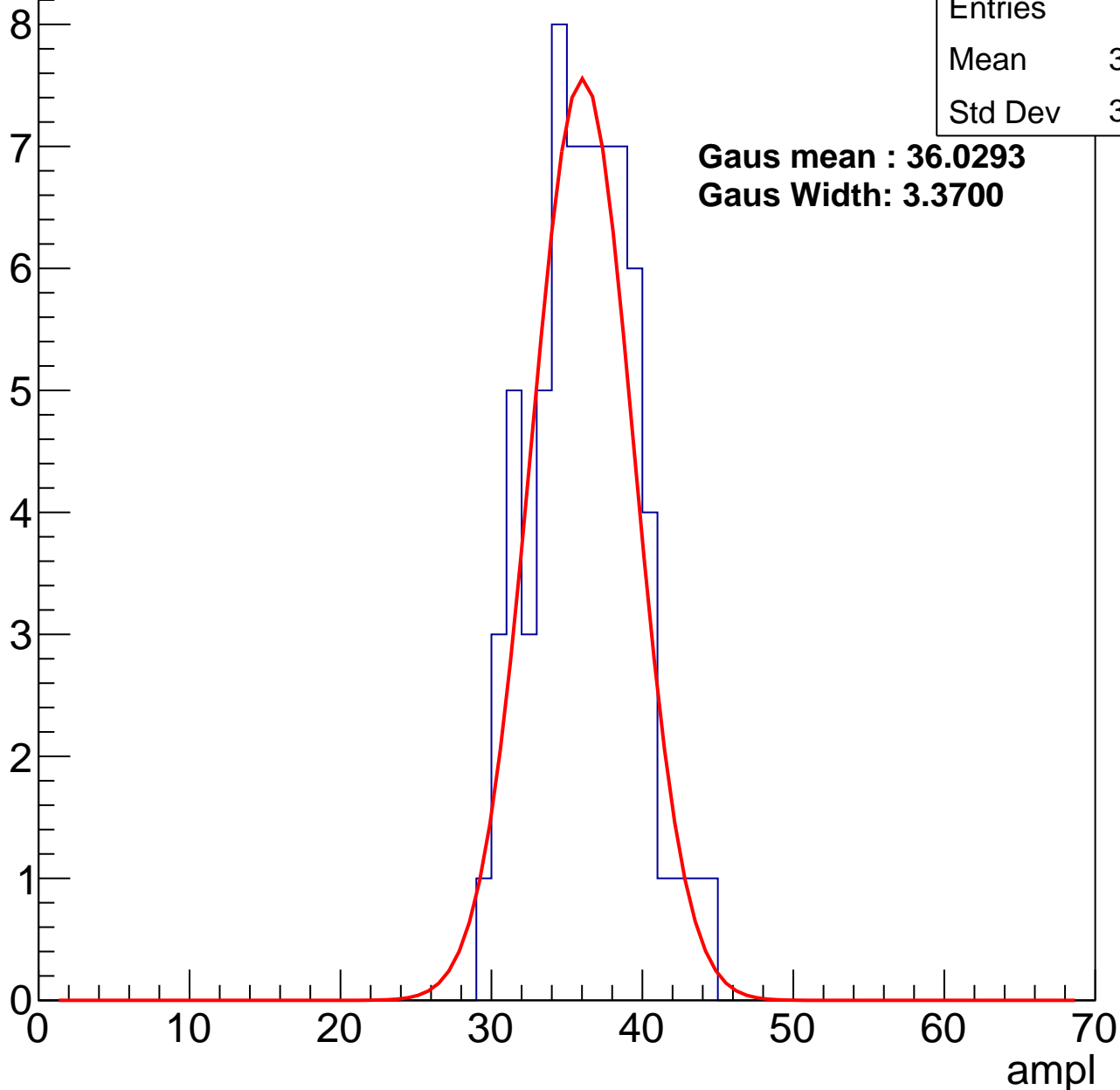
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	35.72
Std Dev	3.314

**Gaus mean : 36.0293**

**Gaus Width: 3.3700**



# B1L102S, U16-ch29, adc2

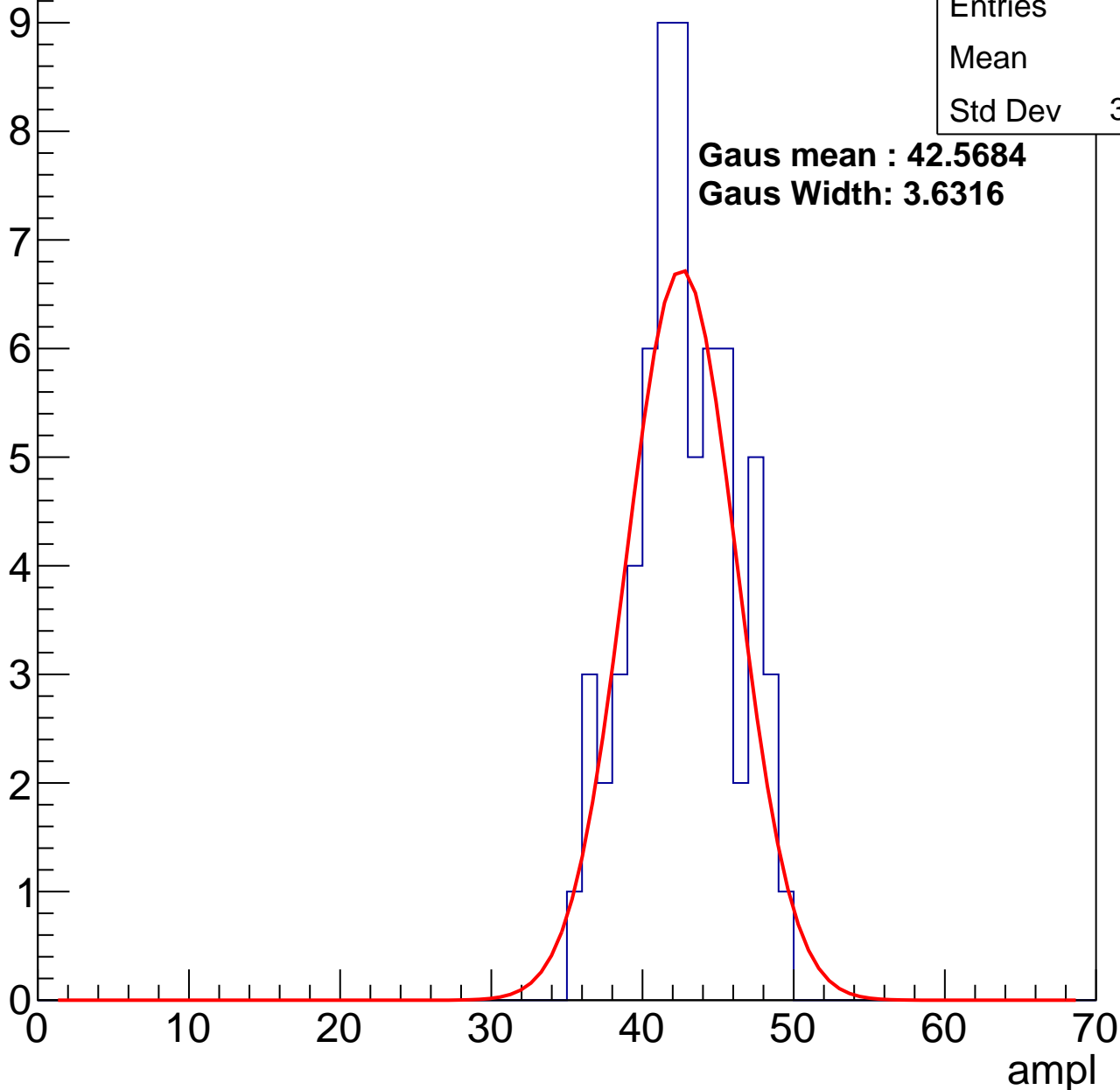
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	42.2
Std Dev	3.325

**Gaus mean : 42.5684**

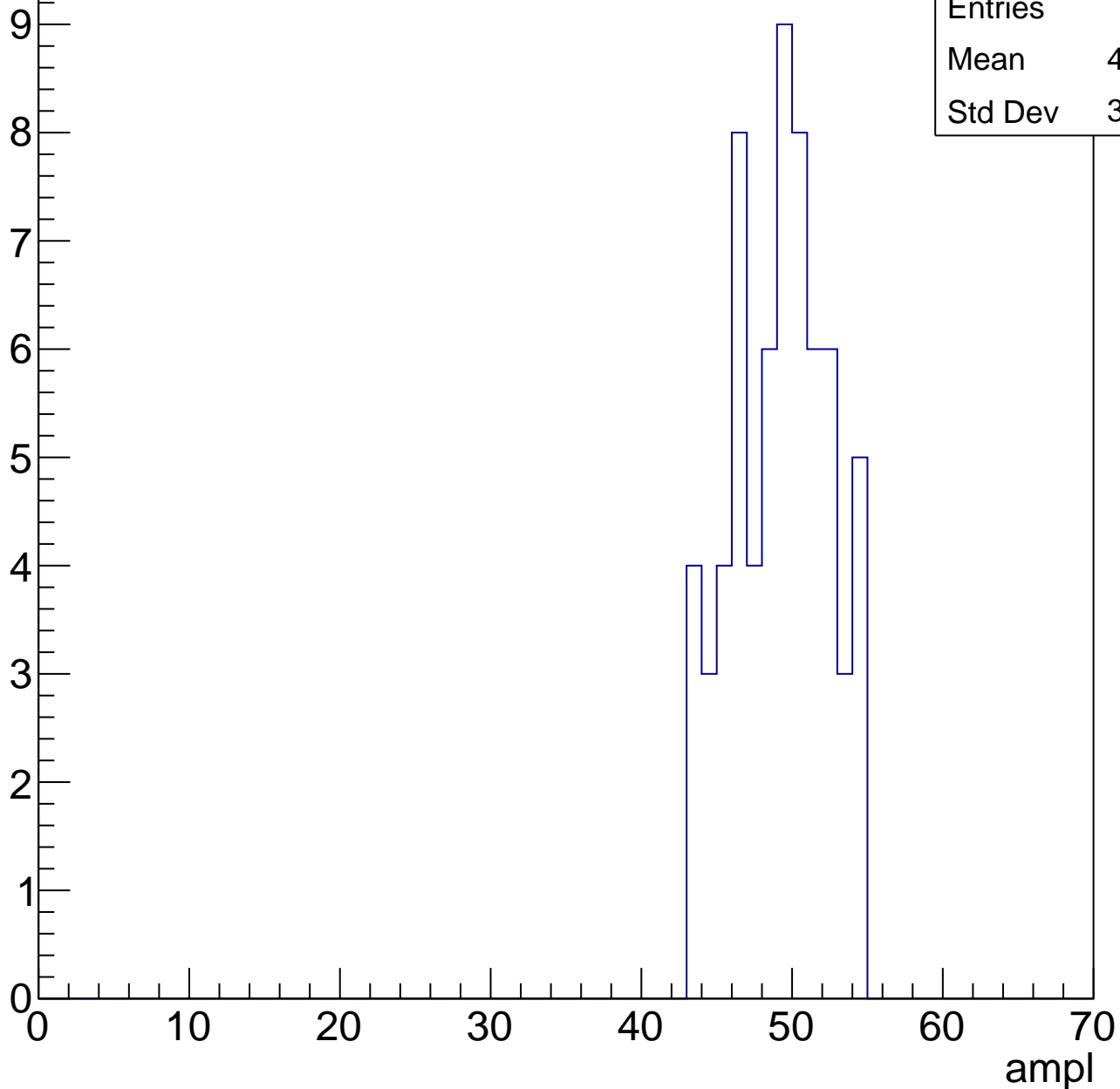
**Gaus Width: 3.6316**



# B1L102S, U16-ch29, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



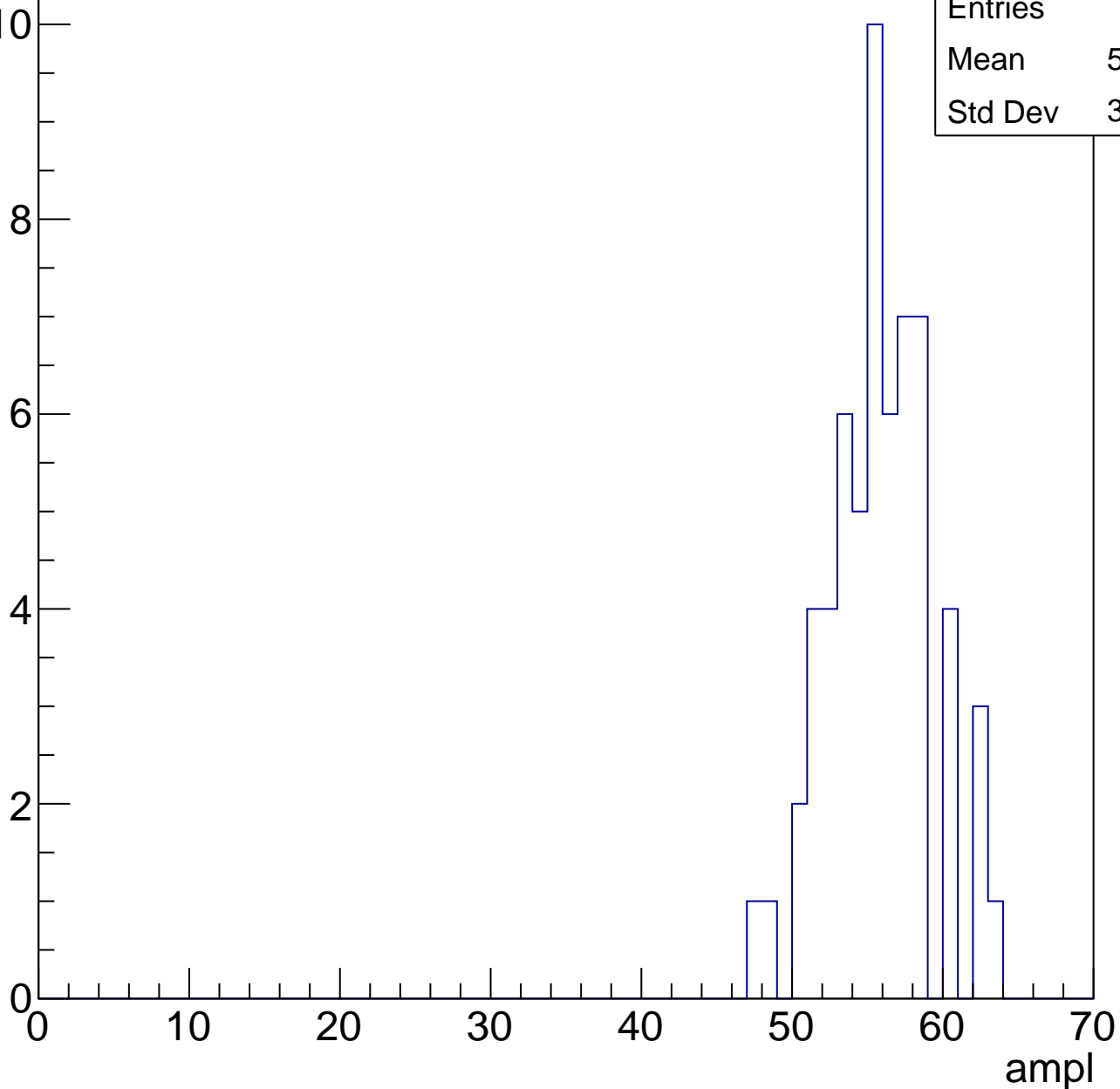
Entries	66
Mean	48.73
Std Dev	3.092

# B1L102S, U16-ch29, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

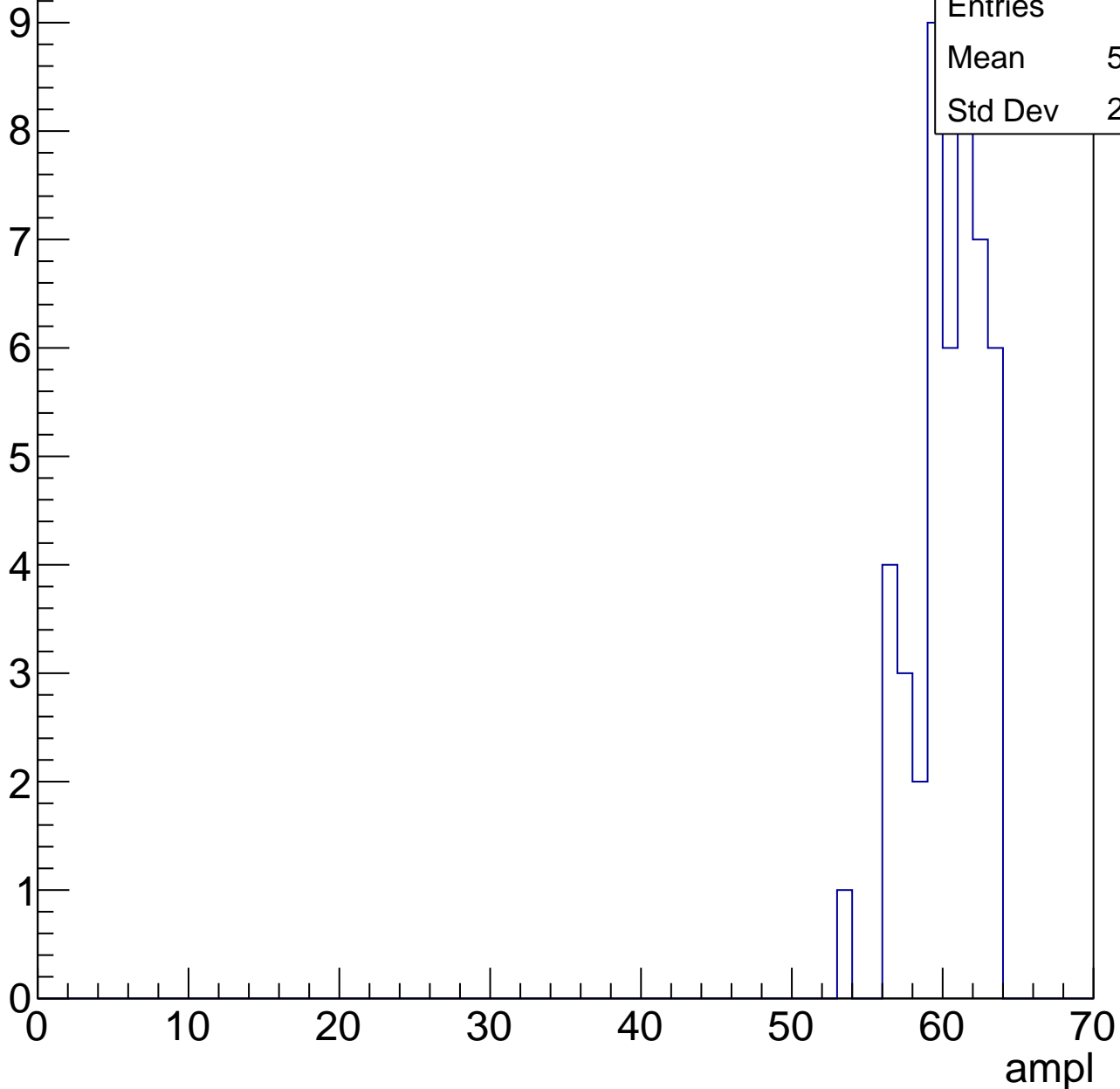
Entries	61
Mean	55.33
Std Dev	3.372



# B1L102S, U16-ch29, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

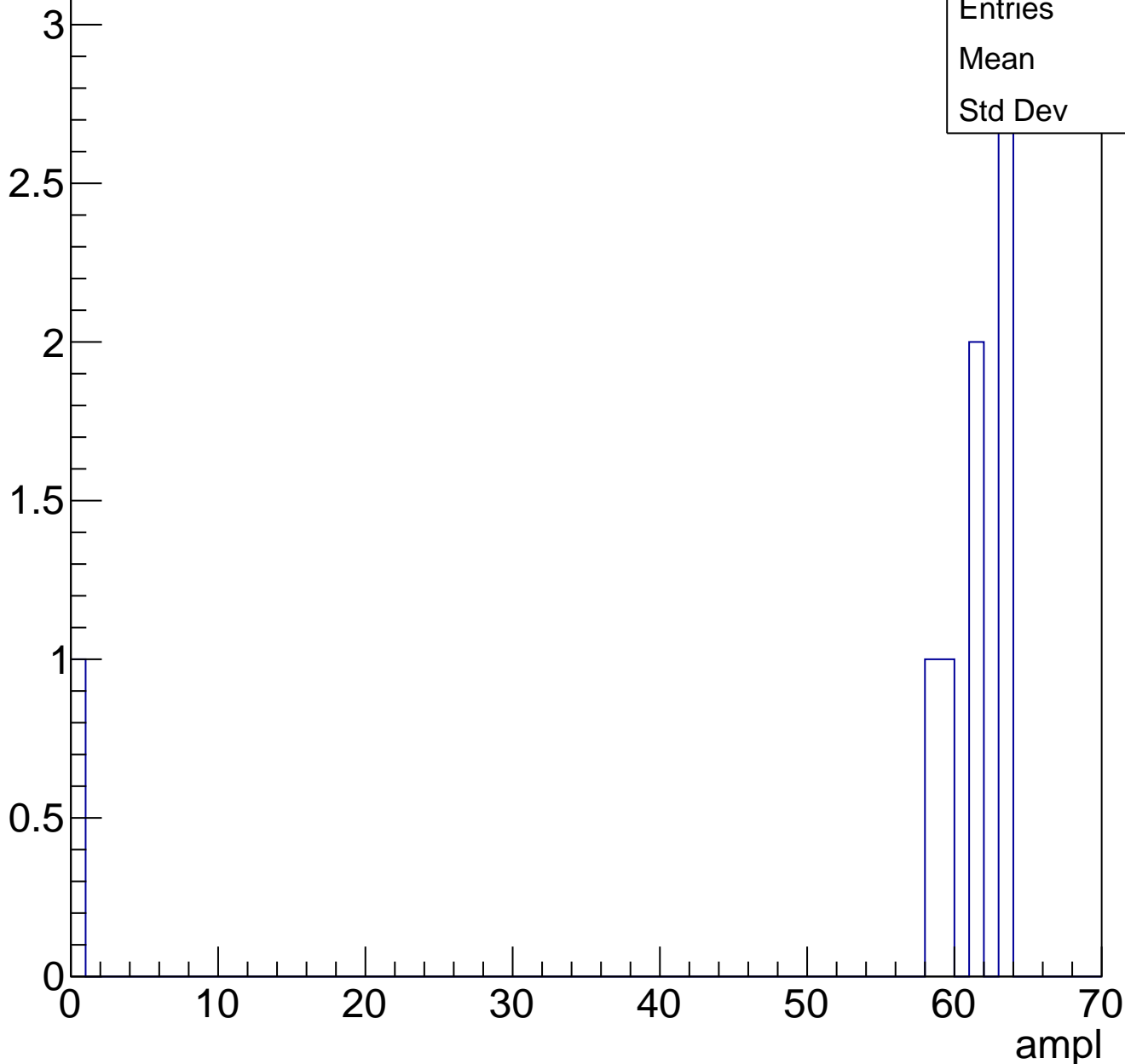
Entry



# B1L102S, U16-ch29, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch29, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U16-ch30, adc0

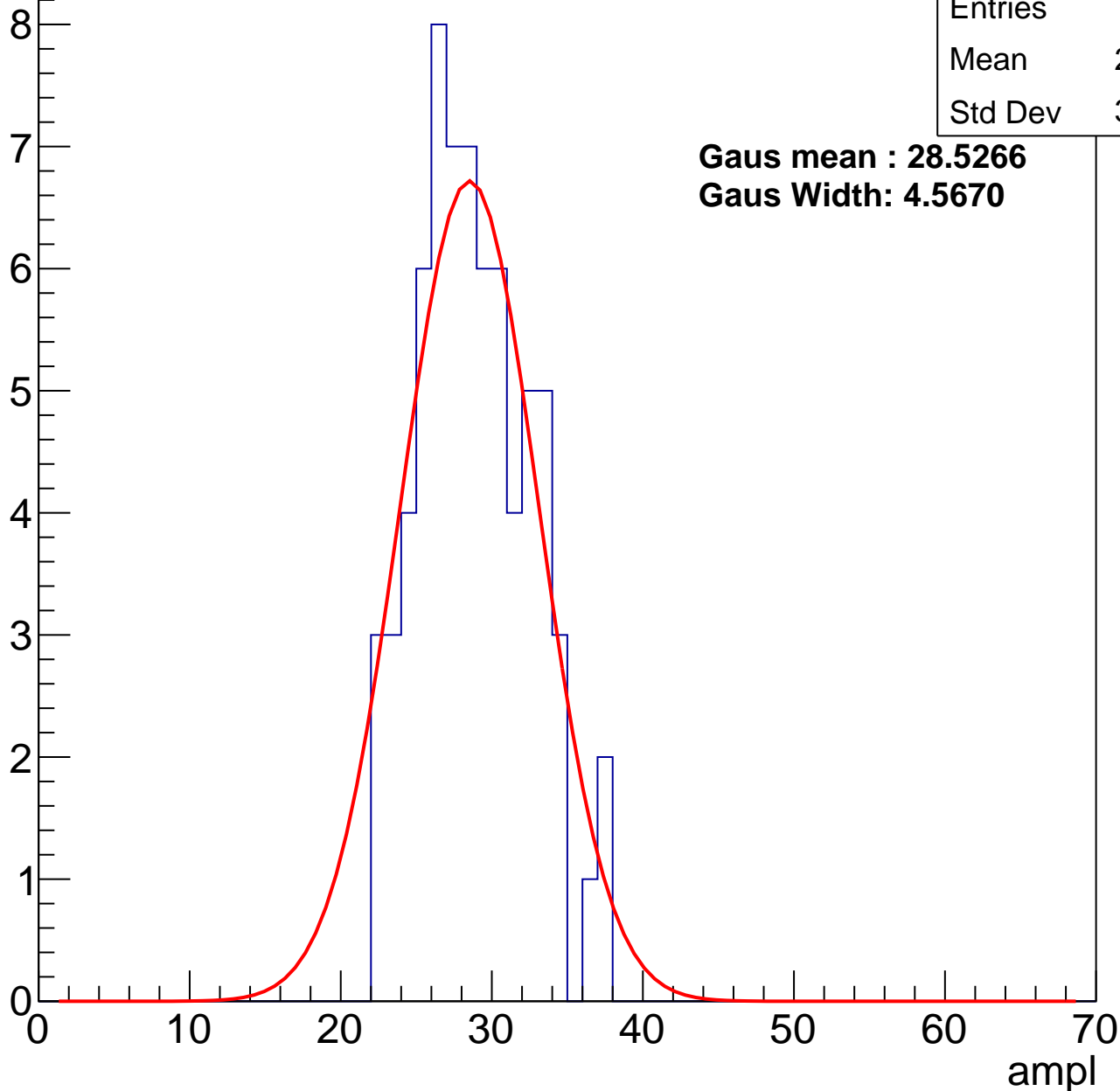
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	28.41
Std Dev	3.651

**Gaus mean : 28.5266**

**Gaus Width: 4.5670**



# B1L102S, U16-ch30, adc1

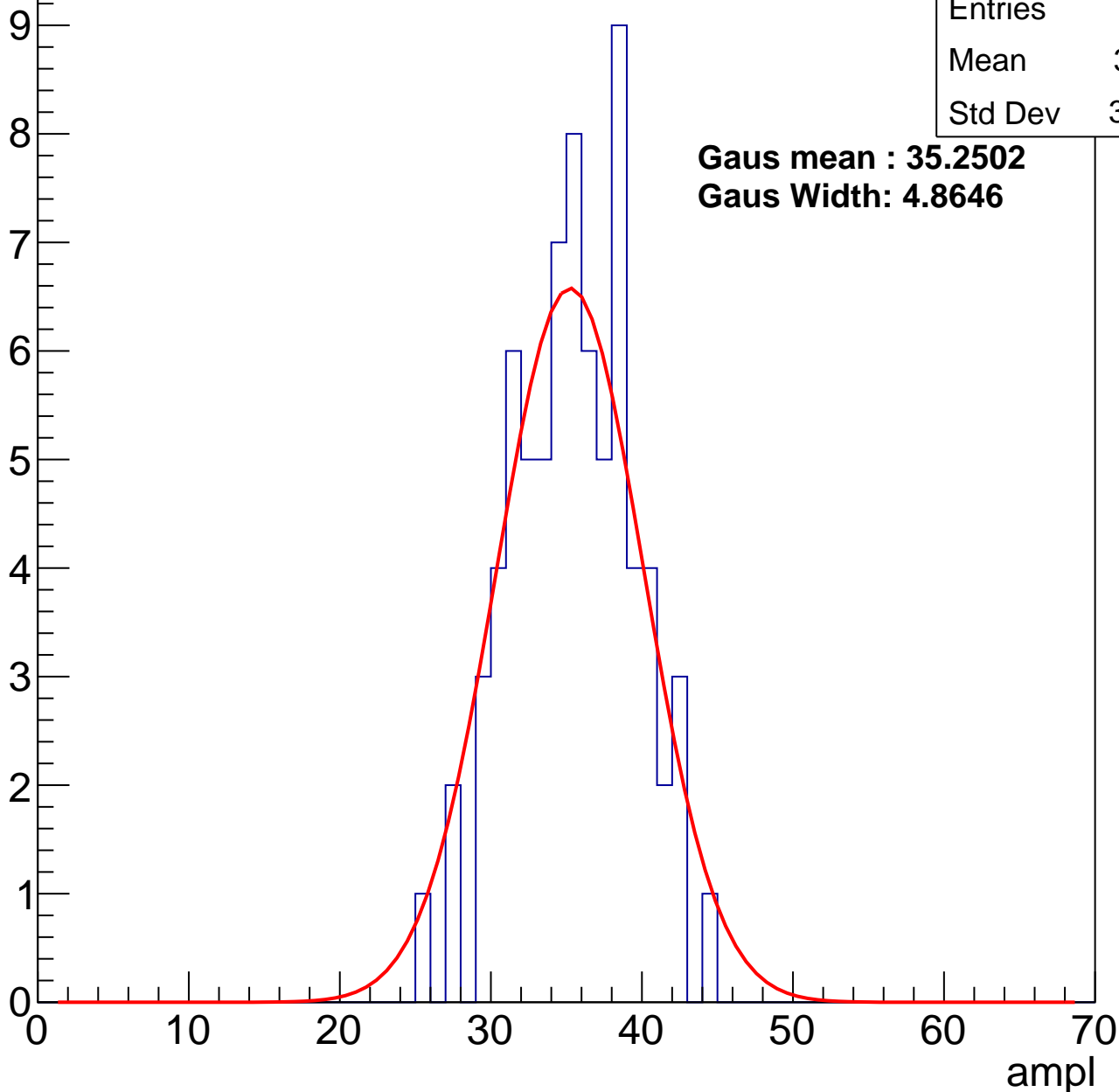
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	35.01
Std Dev	3.958

**Gaus mean : 35.2502**

**Gaus Width: 4.8646**



# B1L102S, U16-ch30, adc2

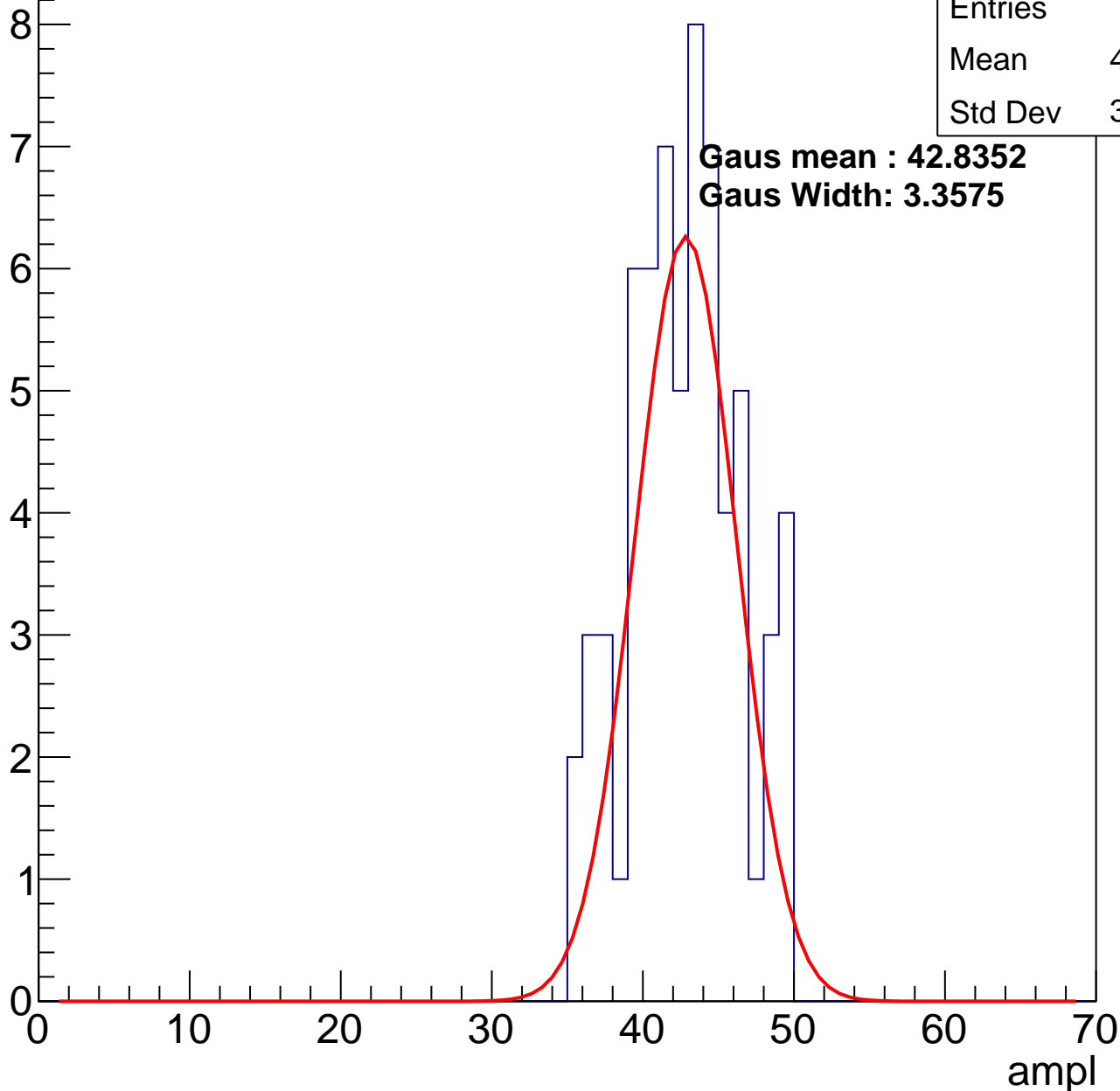
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	42.26
Std Dev	3.634

**Gaus mean : 42.8352**

**Gaus Width: 3.3575**

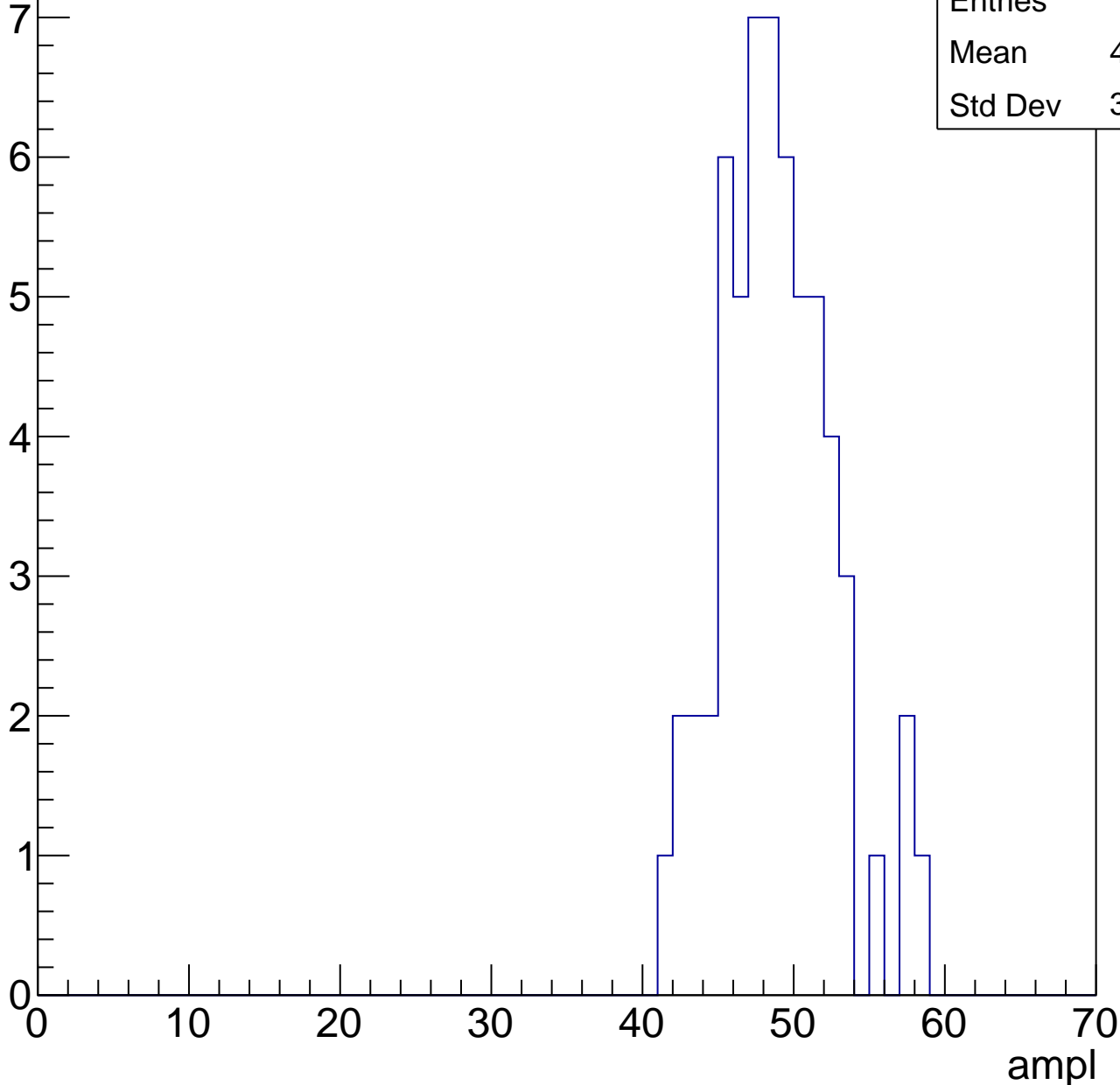


# B1L102S, U16-ch30, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	48.42
Std Dev	3.669

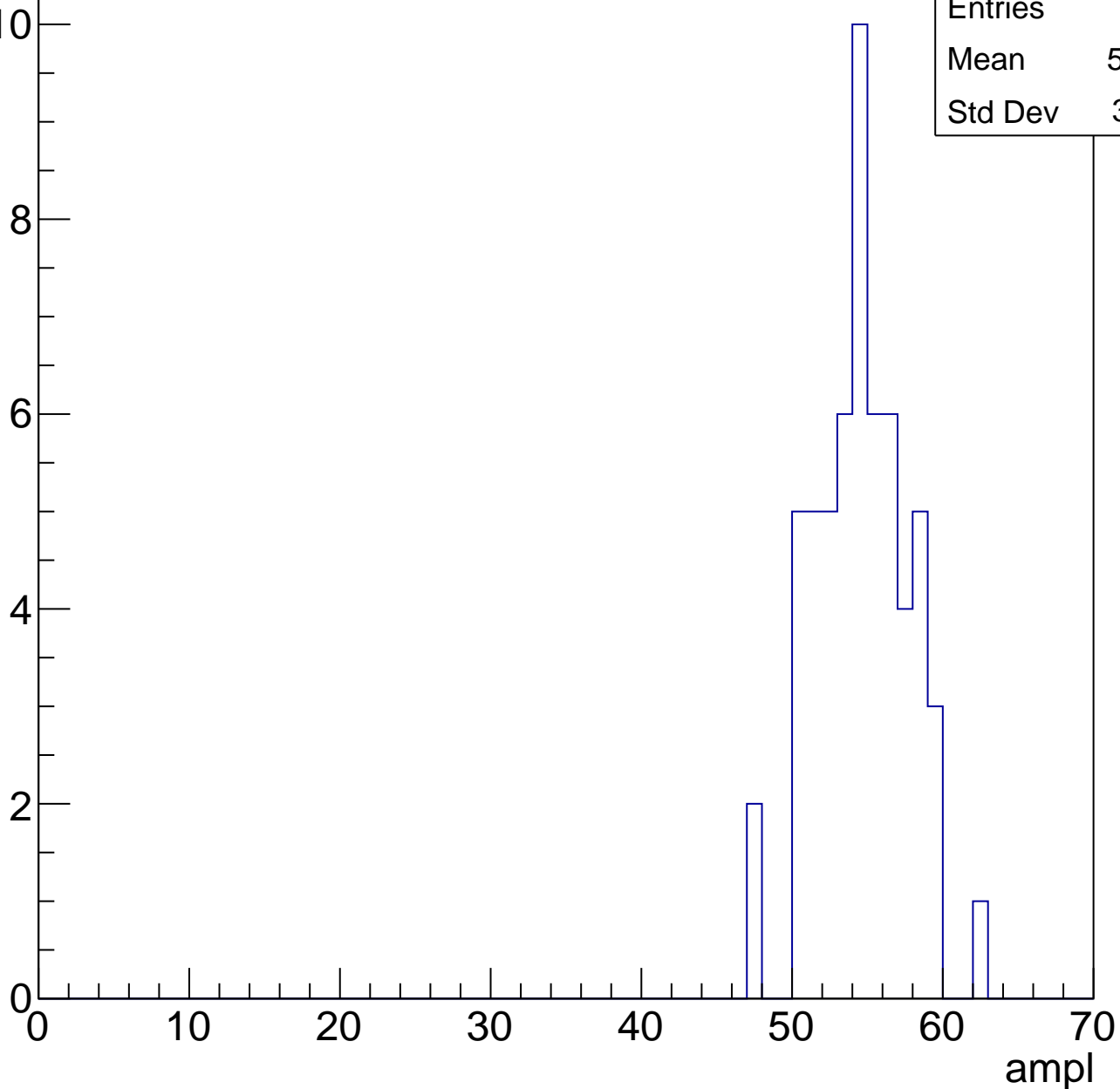


# B1L102S, U16-ch30, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	54.14
Std Dev	3.031

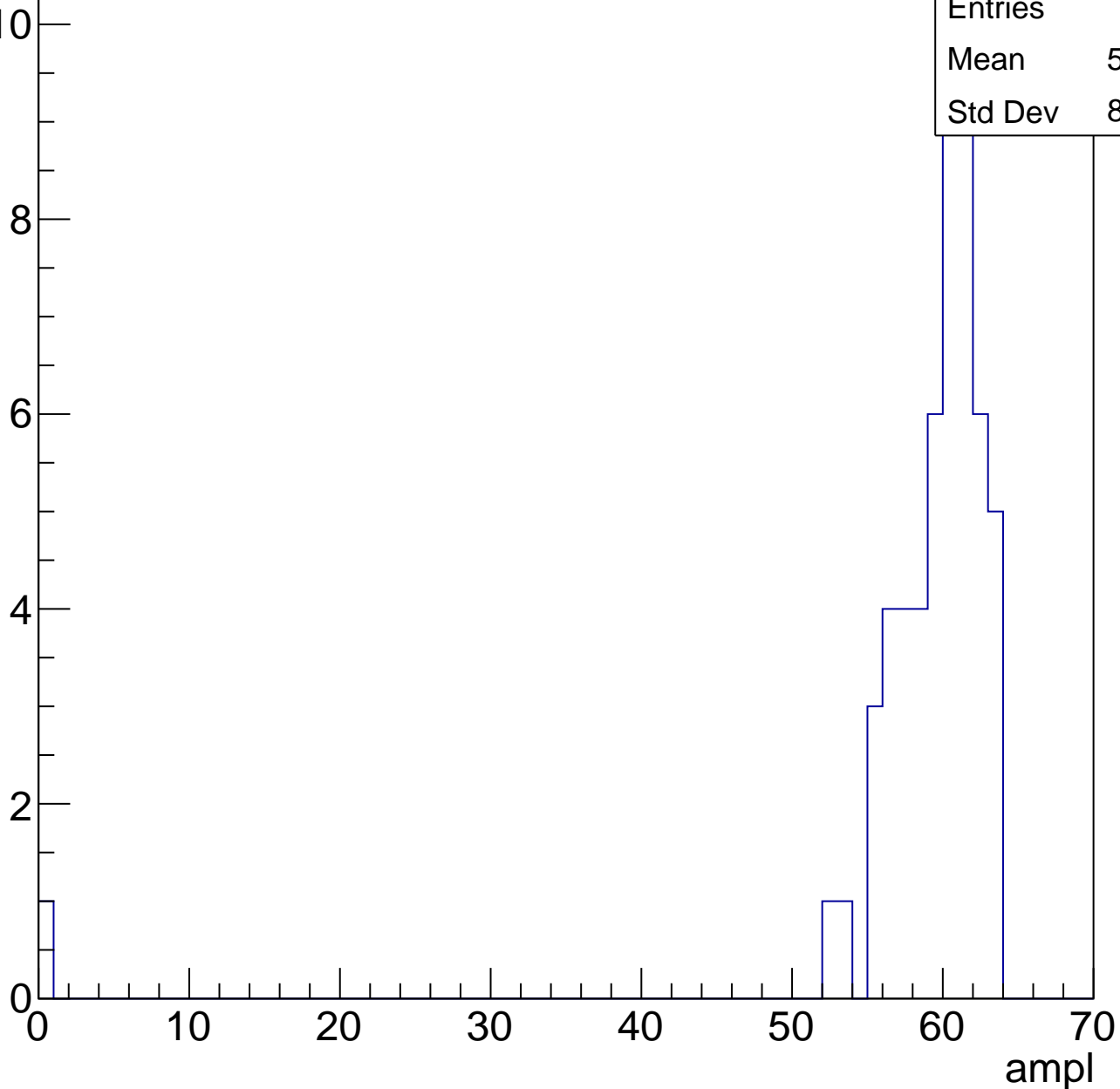


# B1L102S, U16-ch30, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	58.22
Std Dev	8.408

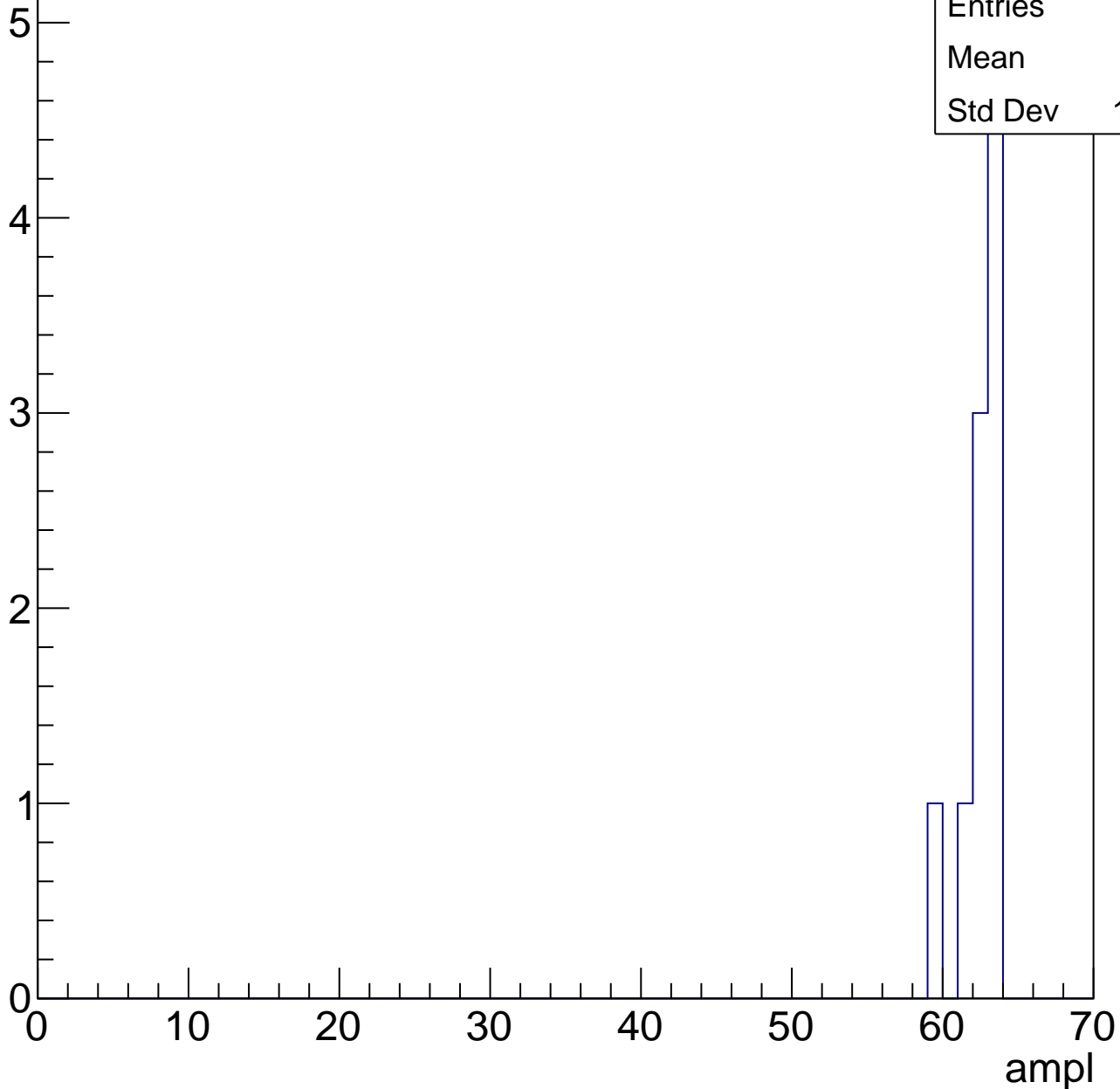


# B1L102S, U16-ch30, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	10
Mean	62.1
Std Dev	1.221





# B1L102S, U16-ch30, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	9
Std Dev	9

# B1L102S, U16-ch31, adc0

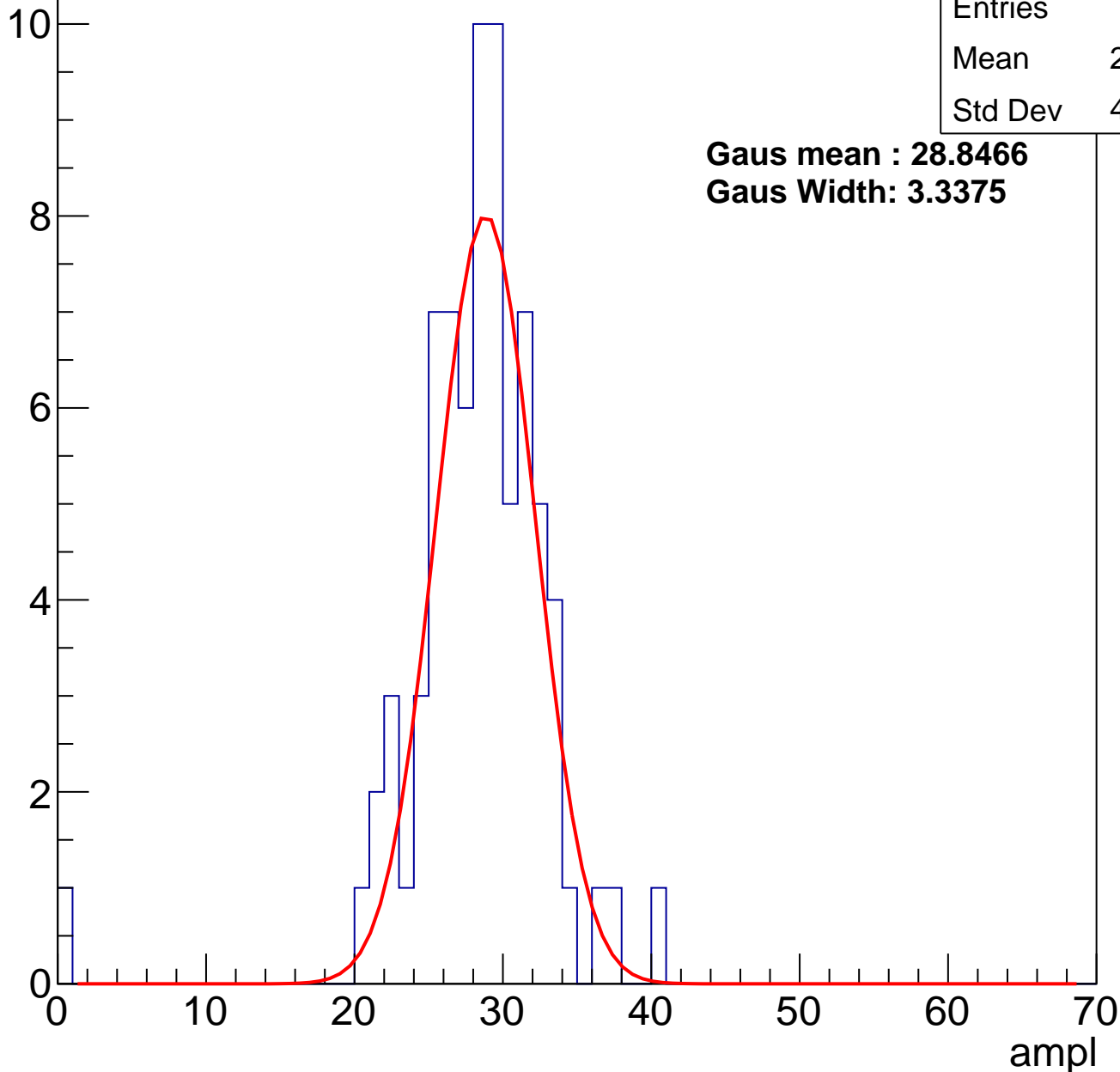
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	76
Mean	27.87
Std Dev	4.895

**Gaus mean : 28.8466**

**Gaus Width: 3.3375**

Entry



# B1L102S, U16-ch31, adc1

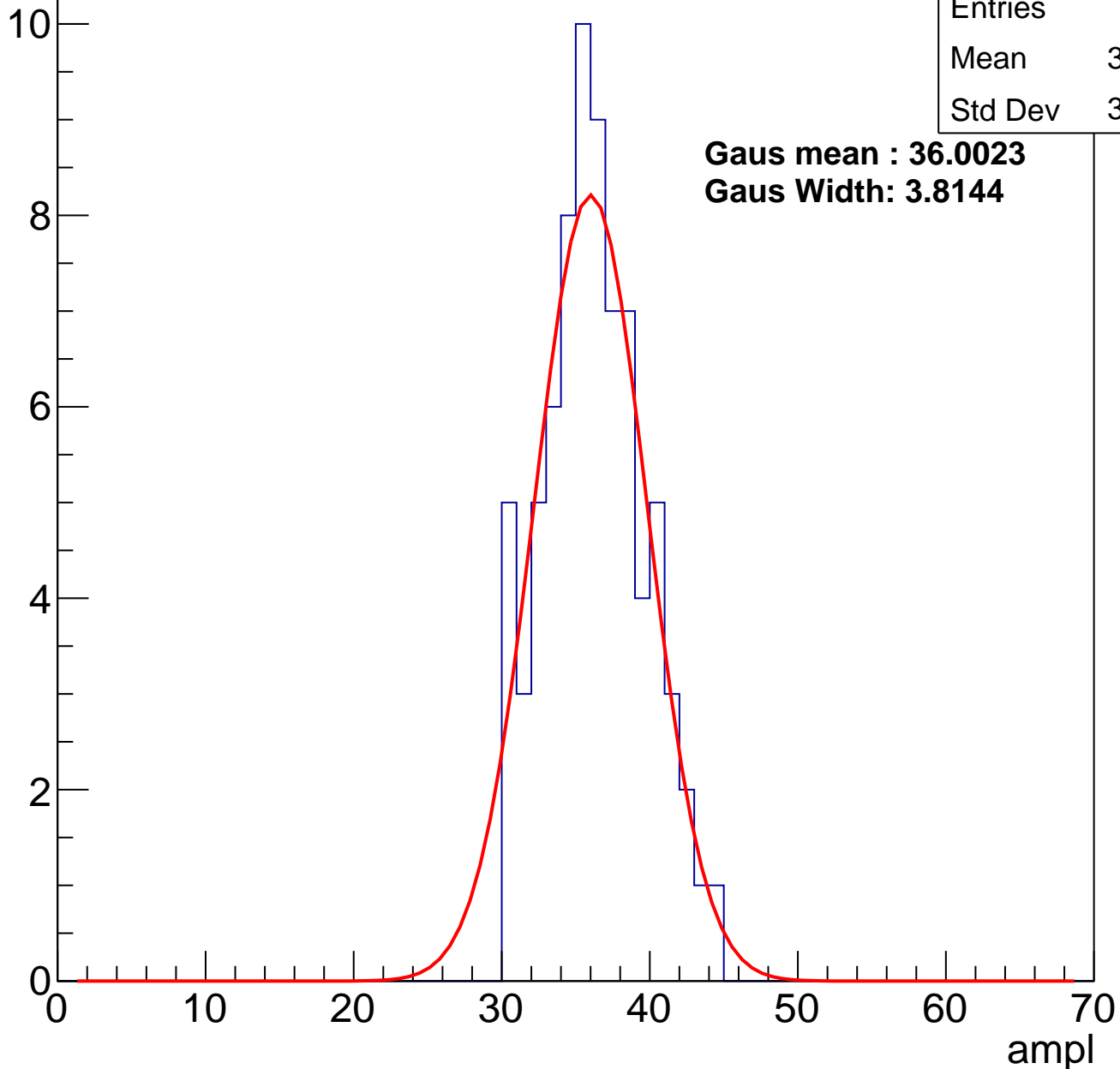
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	76
Mean	35.82
Std Dev	3.323

**Gaus mean : 36.0023**

**Gaus Width: 3.8144**

Entry



# B1L102S, U16-ch31, adc2

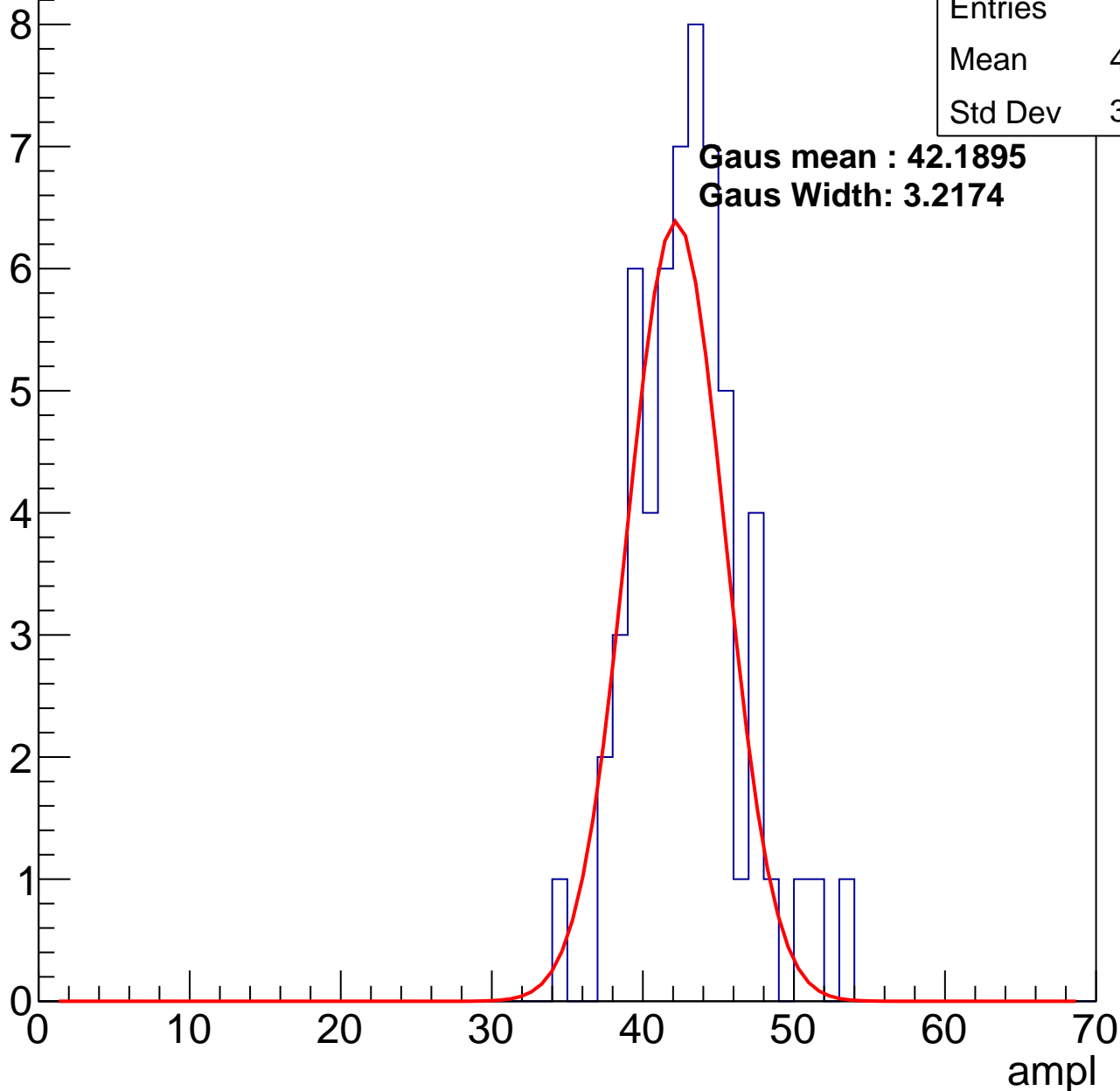
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	42.57
Std Dev	3.519

**Gaus mean : 42.1895**

**Gaus Width: 3.2174**

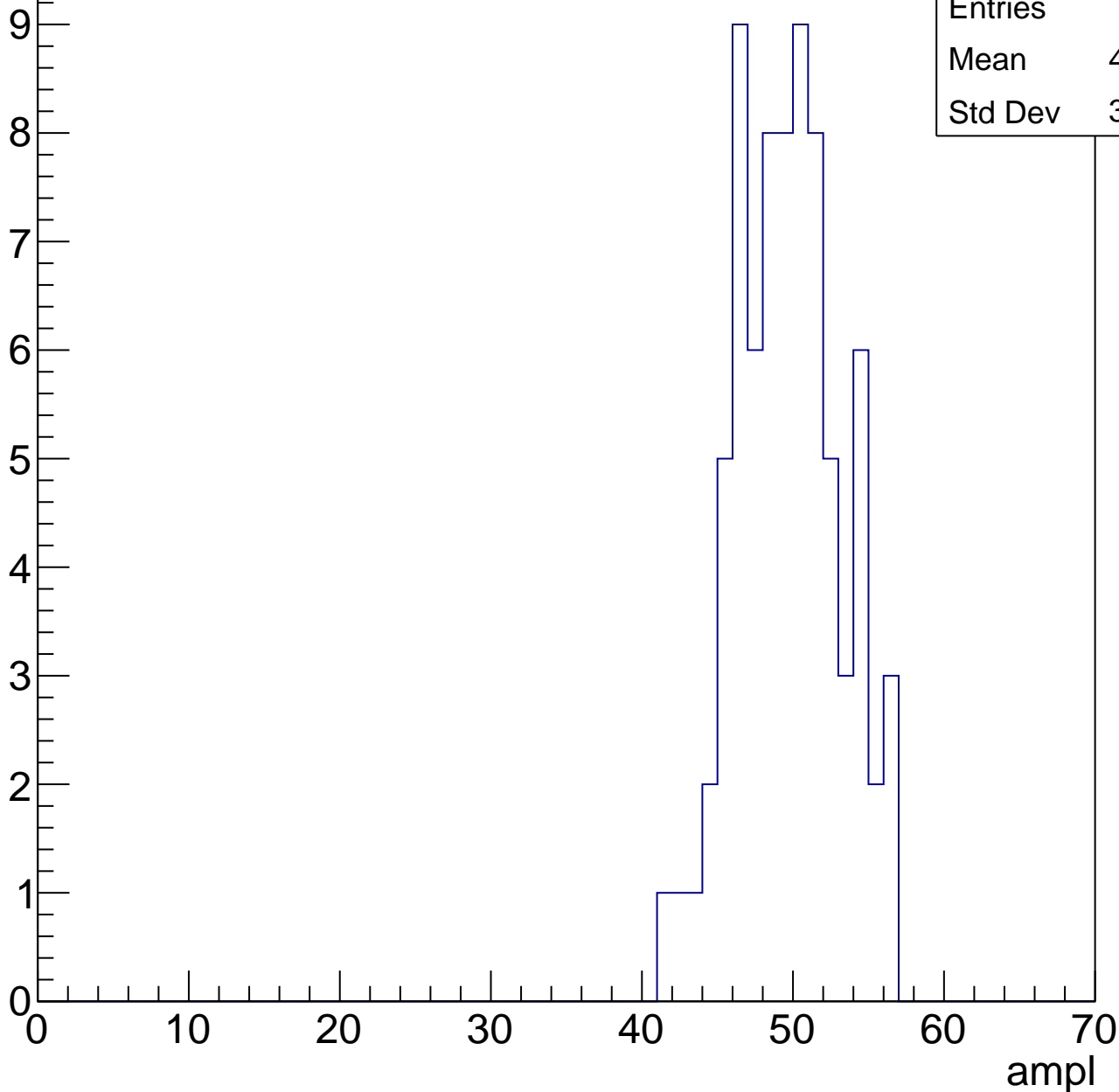


# B1L102S, U16-ch31, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	49.22
Std Dev	3.402

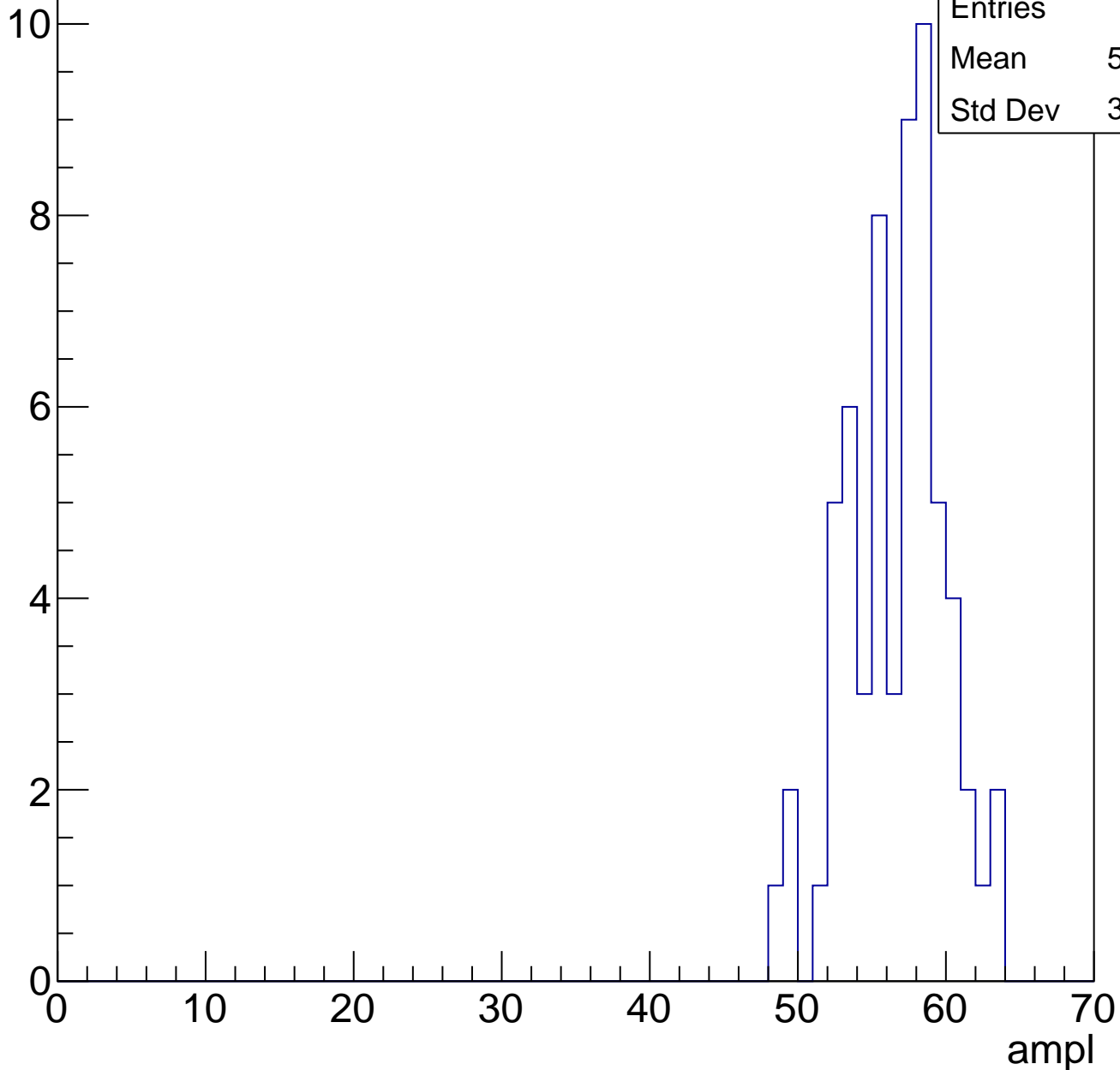


# B1L102S, U16-ch31, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	62
Mean	56.18
Std Dev	3.314

Entry

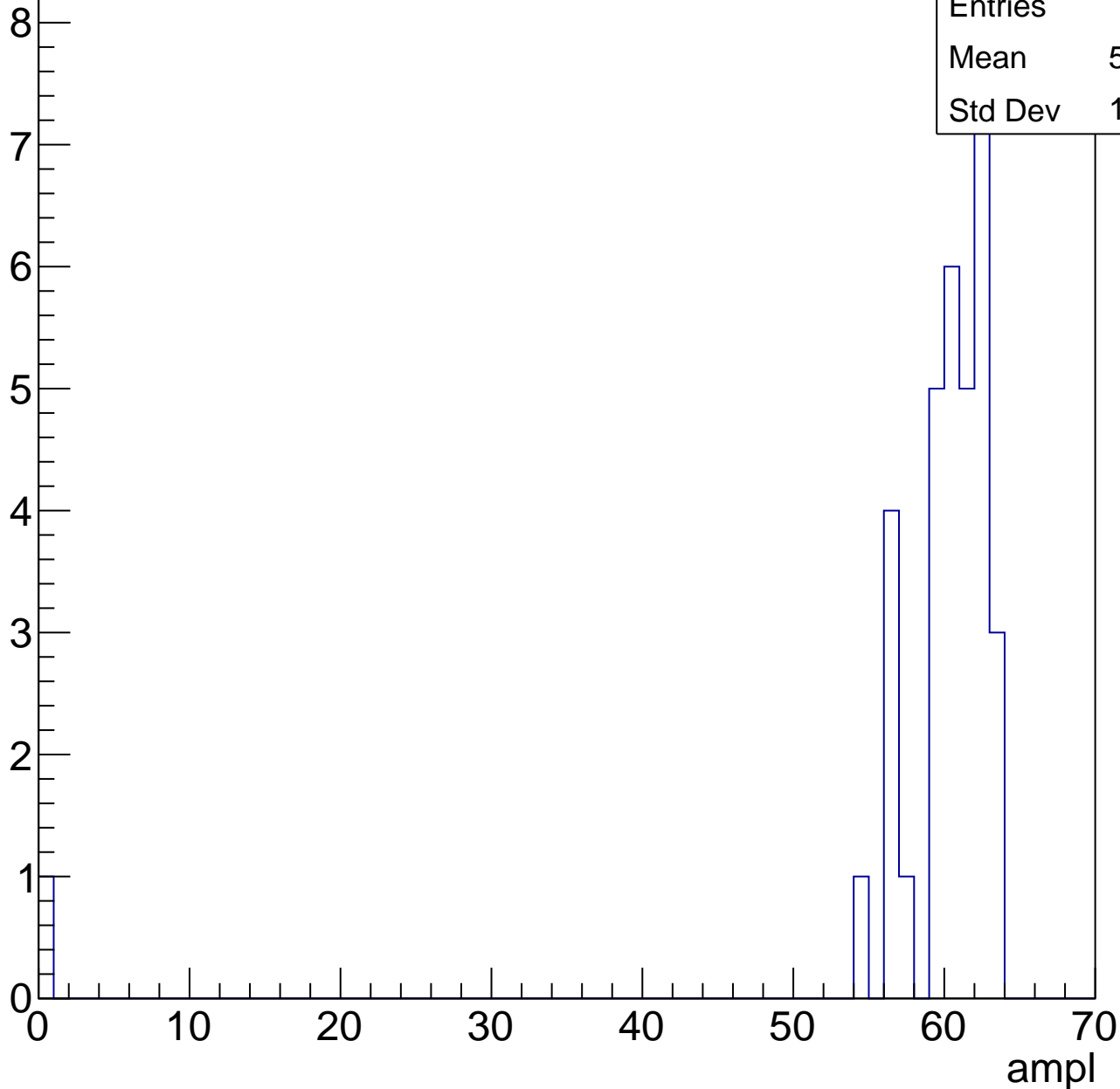


# B1L102S, U16-ch31, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	34
Mean	58.24
Std Dev	10.39

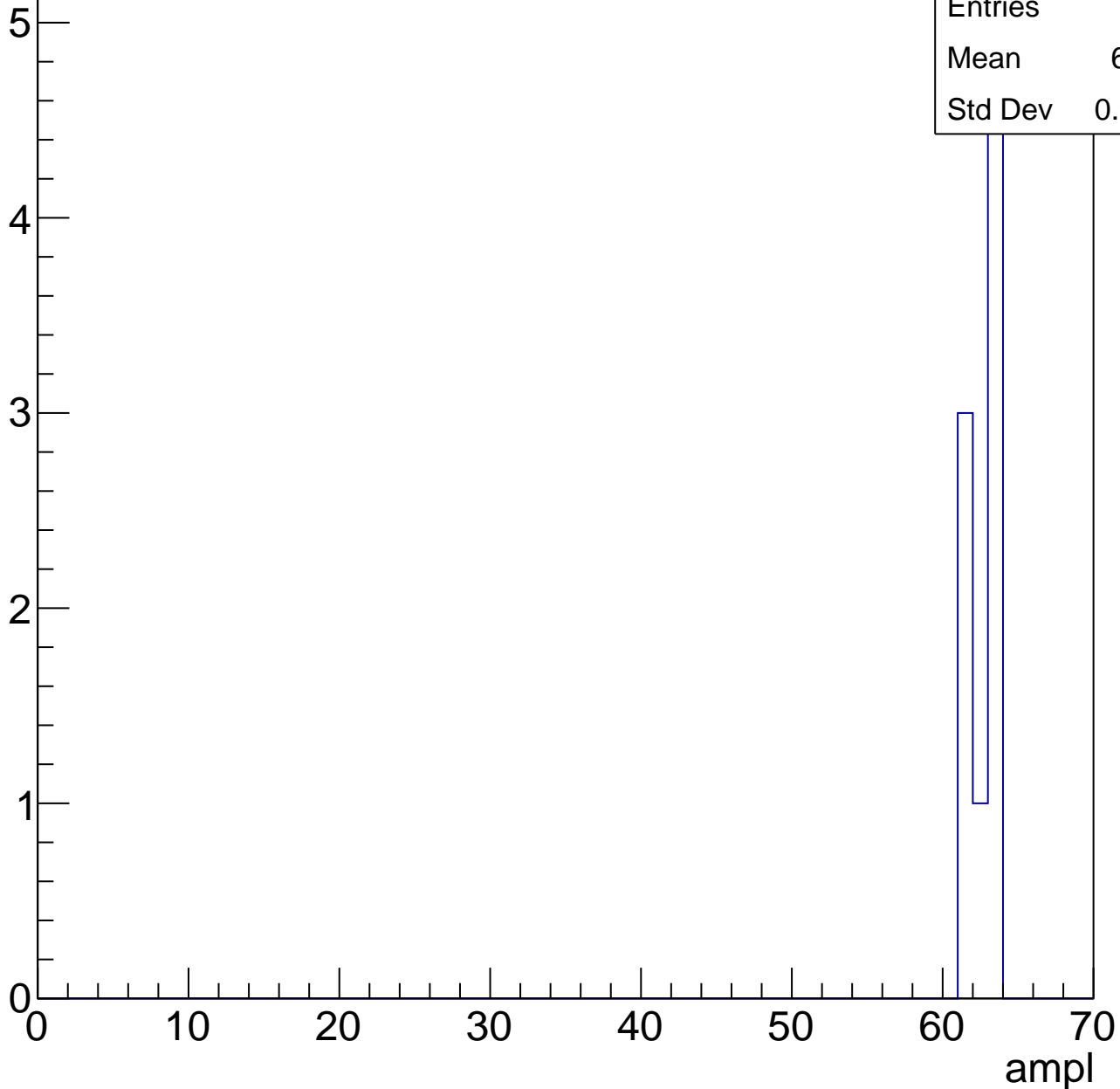


# B1L102S, U16-ch31, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	9
Mean	62.22
Std Dev	0.9162





# B1L102S, U16-ch31, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch32, adc0

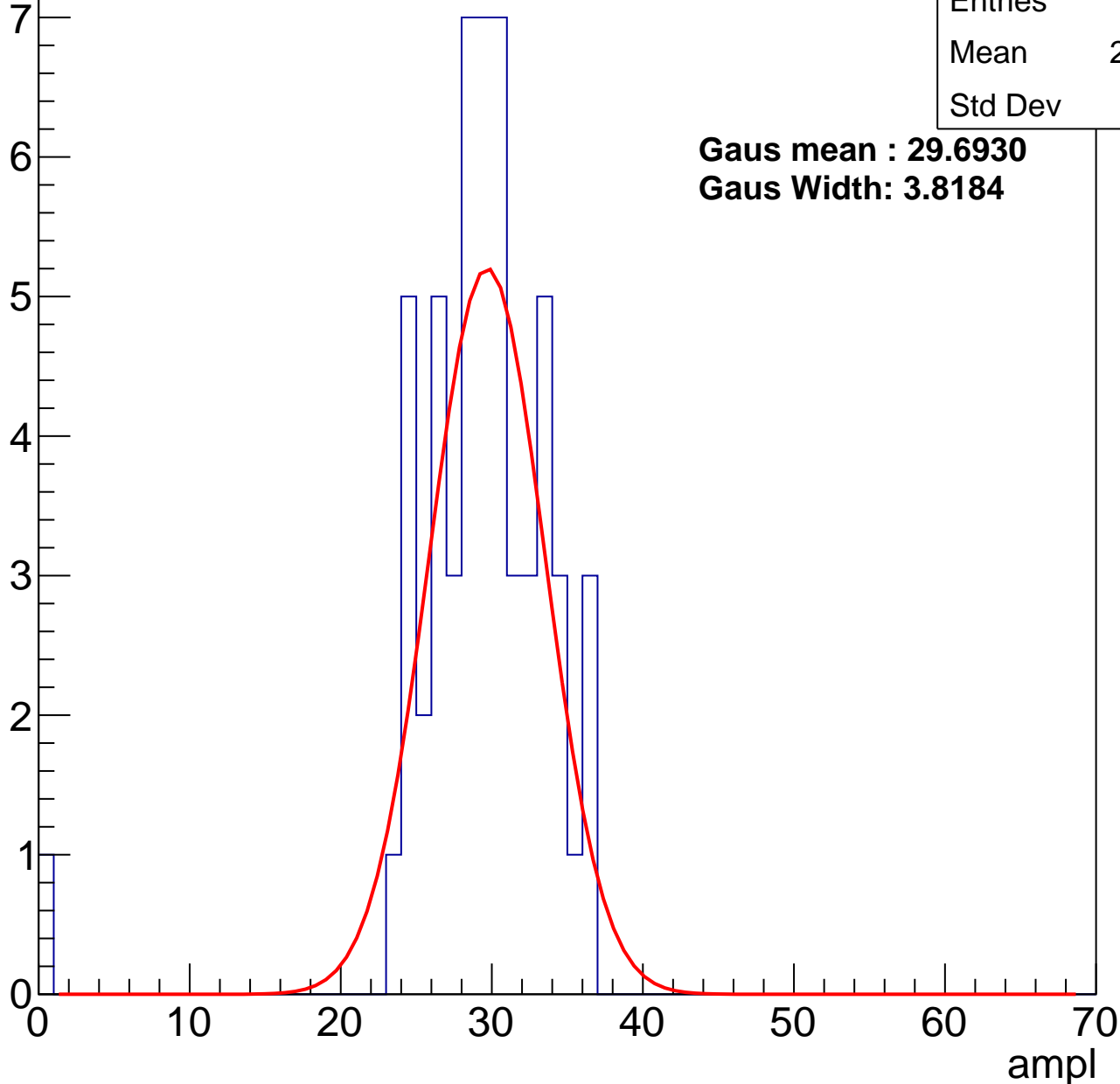
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	28.79
Std Dev	5.14

**Gaus mean : 29.6930**

**Gaus Width: 3.8184**



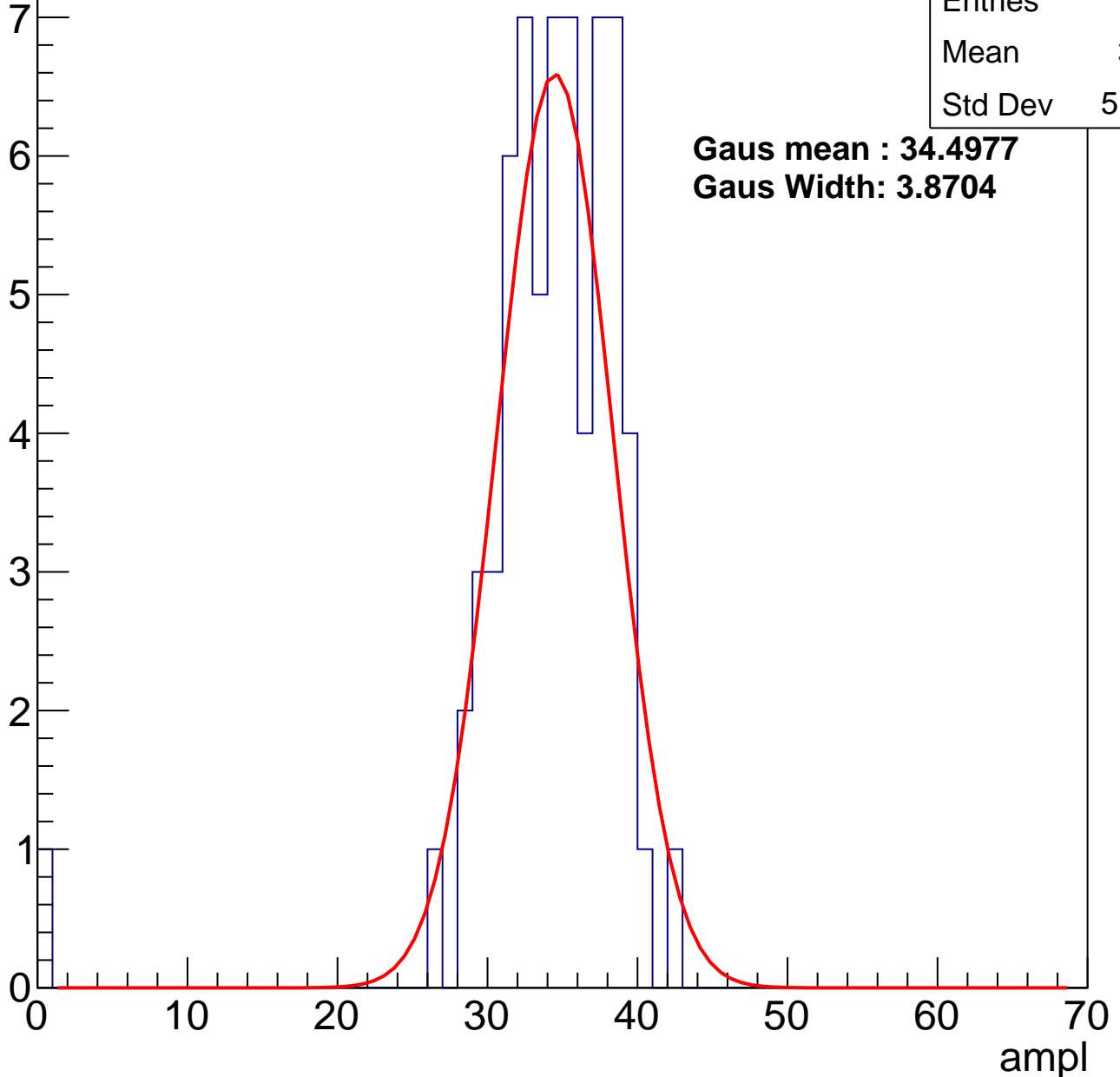
# B1L102S, U16-ch32, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	33.7
Std Dev	5.357

**Gaus mean : 34.4977**  
**Gaus Width: 3.8704**



# B1L102S, U16-ch32, adc2

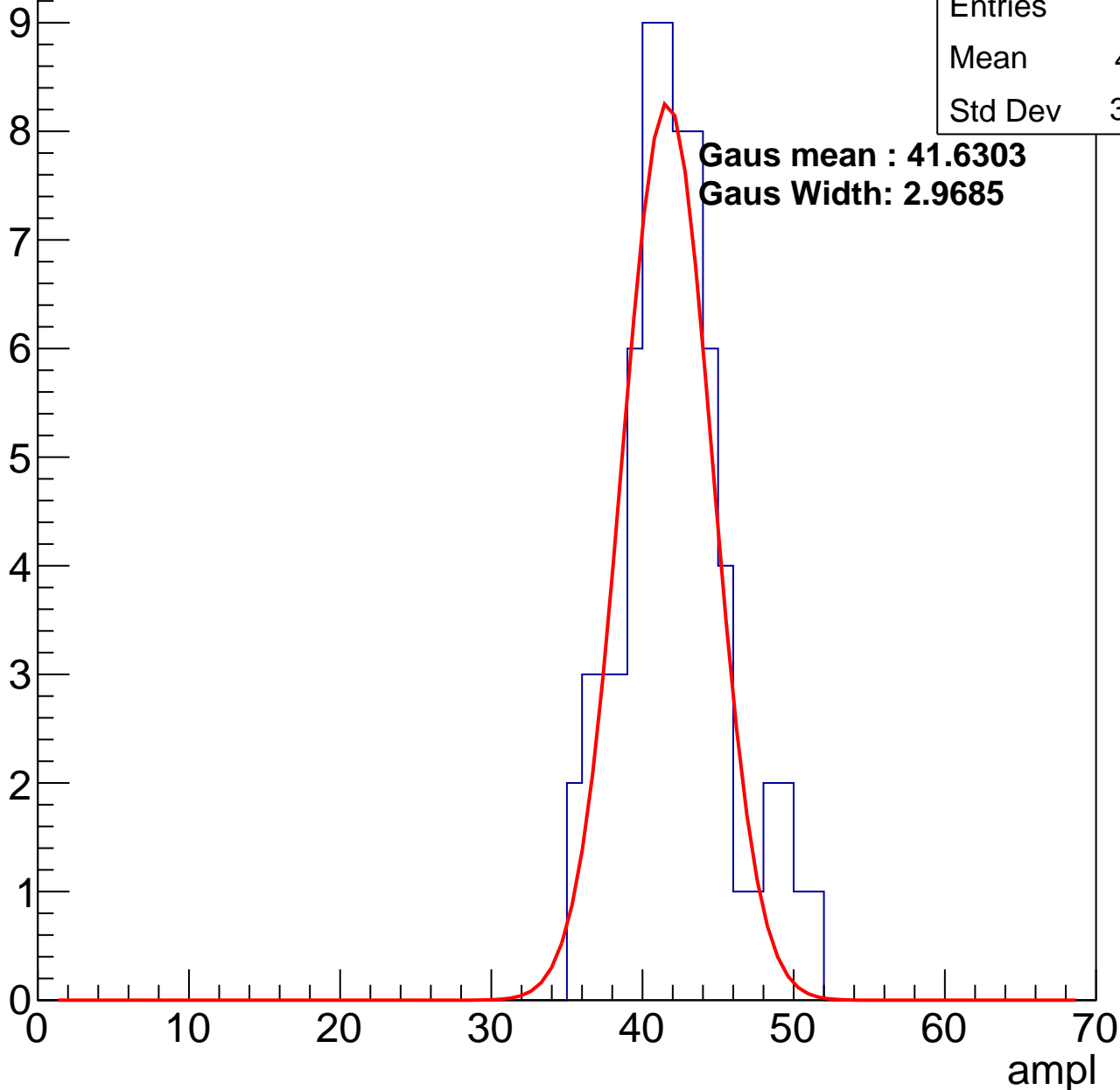
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	41.71
Std Dev	3.502

**Gaus mean : 41.6303**

**Gaus Width: 2.9685**

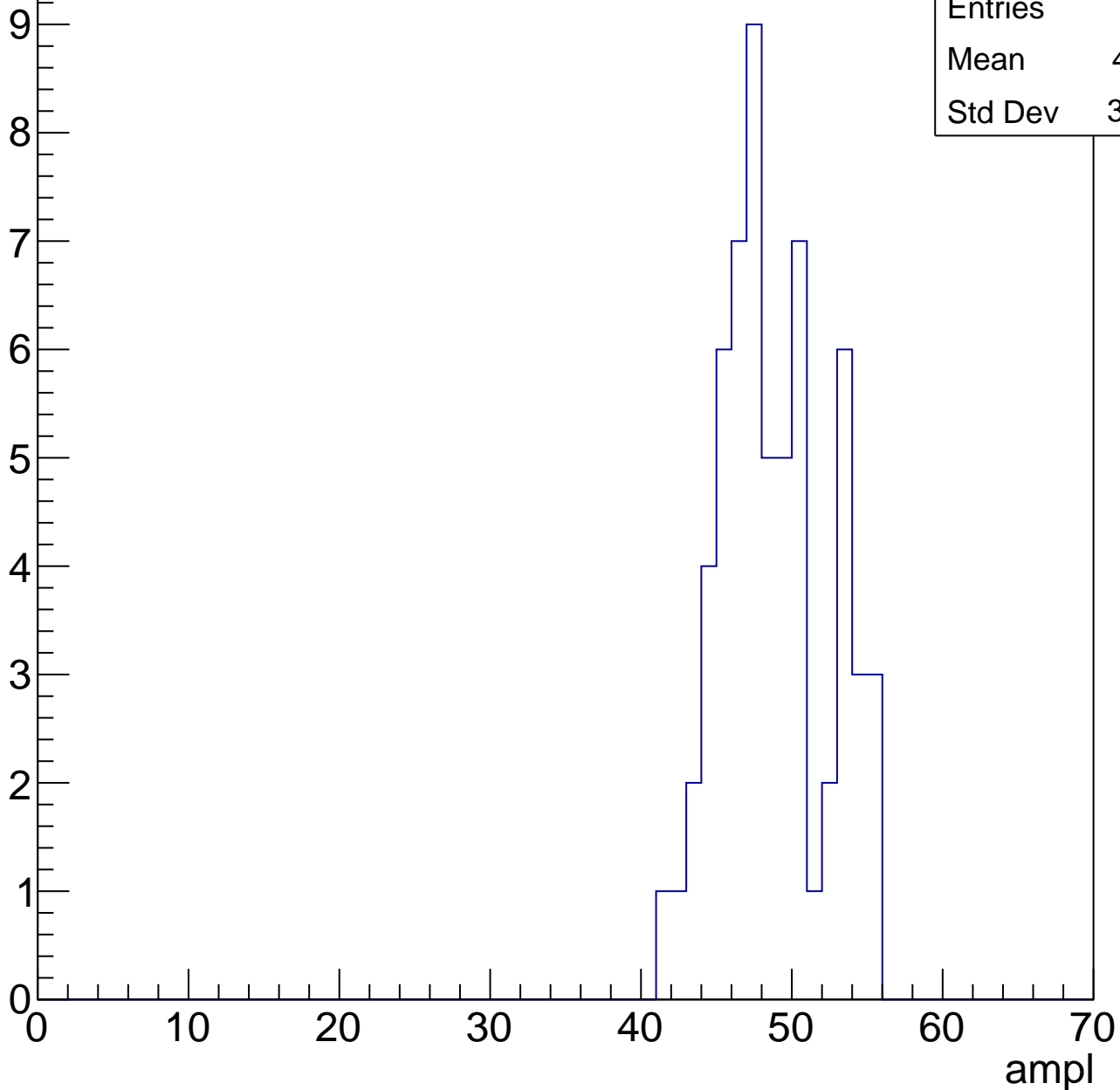


# B1L102S, U16-ch32, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	48.31
Std Dev	3.508

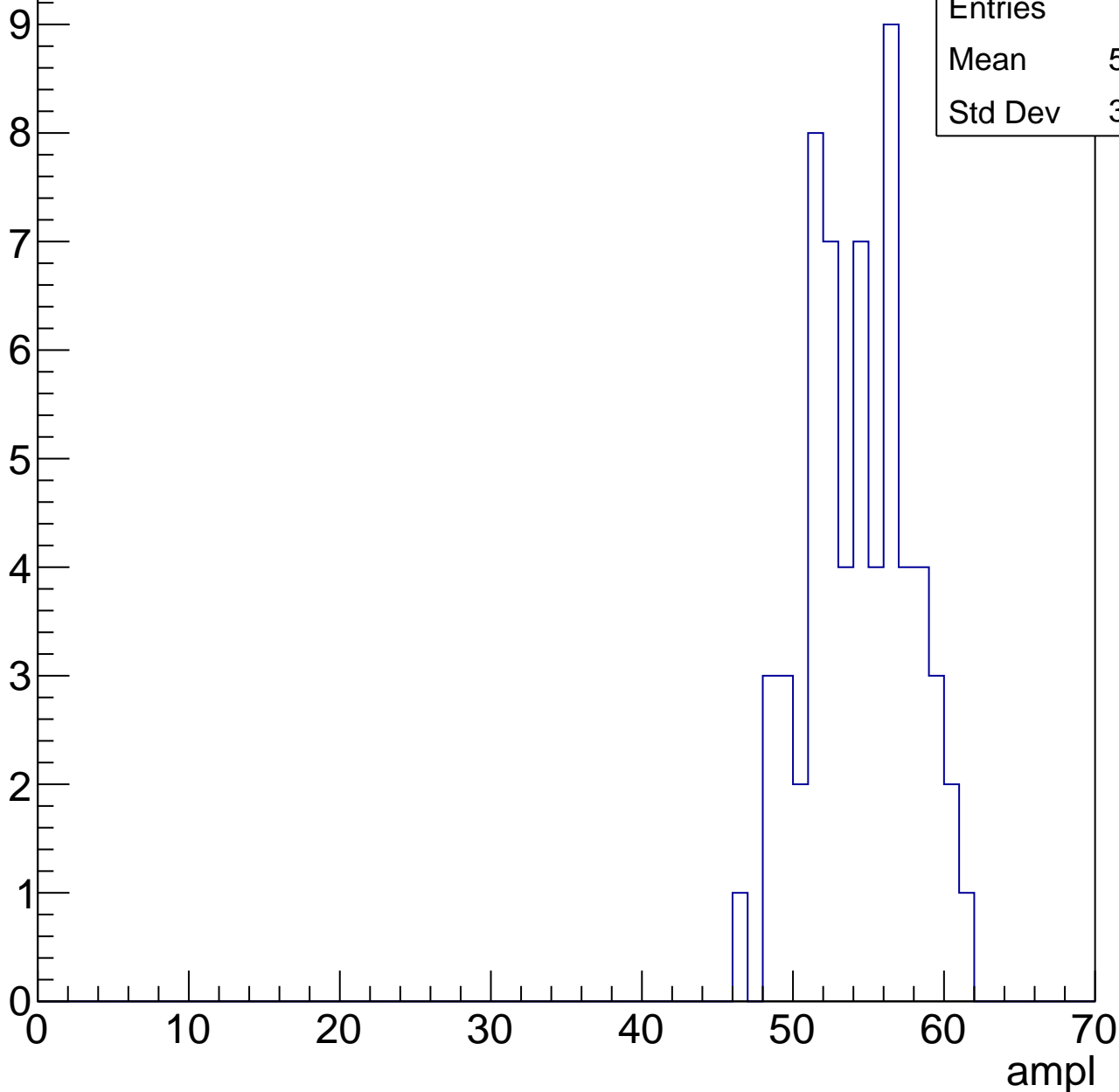


# B1L102S, U16-ch32, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	53.89
Std Dev	3.404

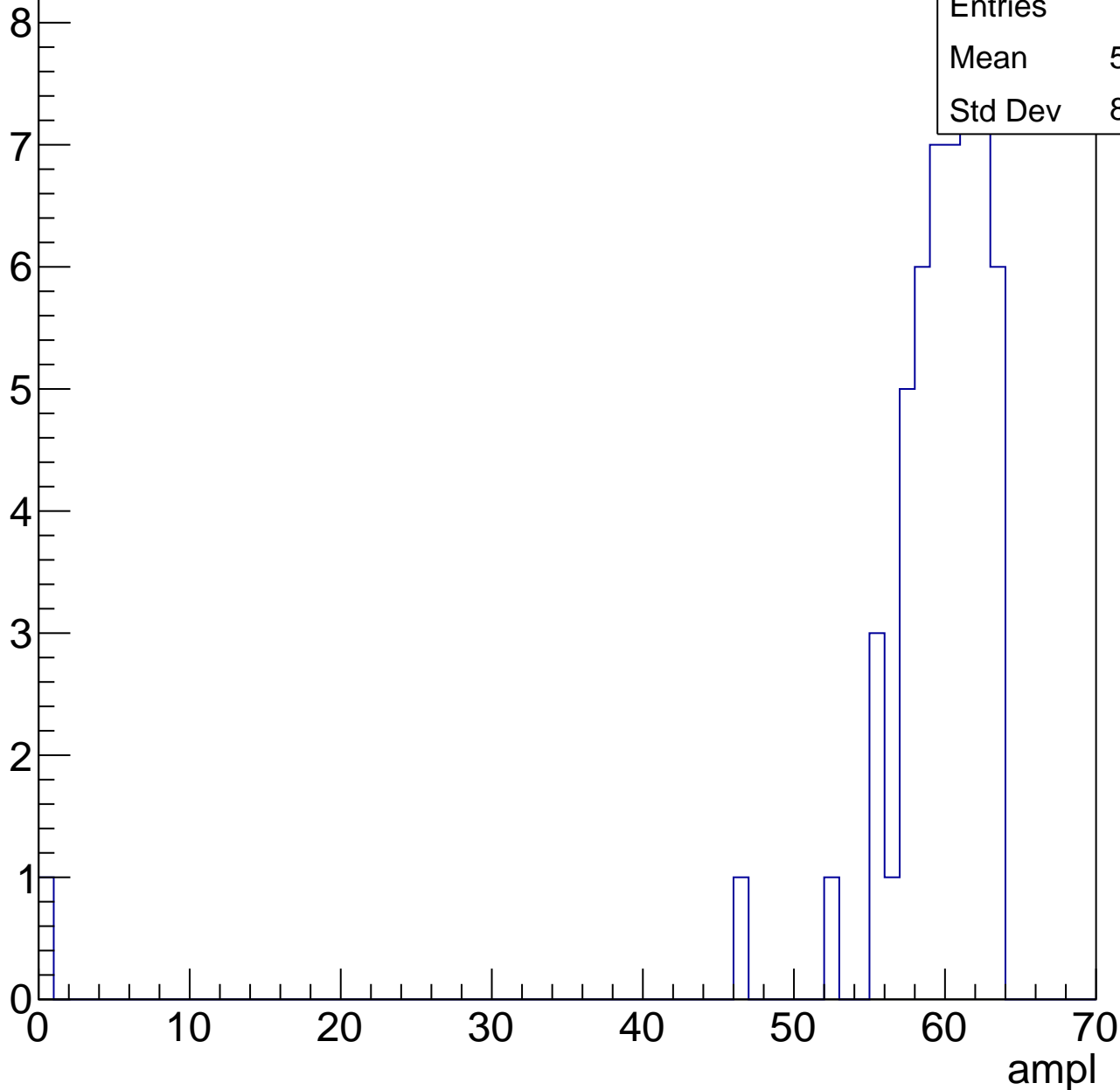


# B1L102S, U16-ch32, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

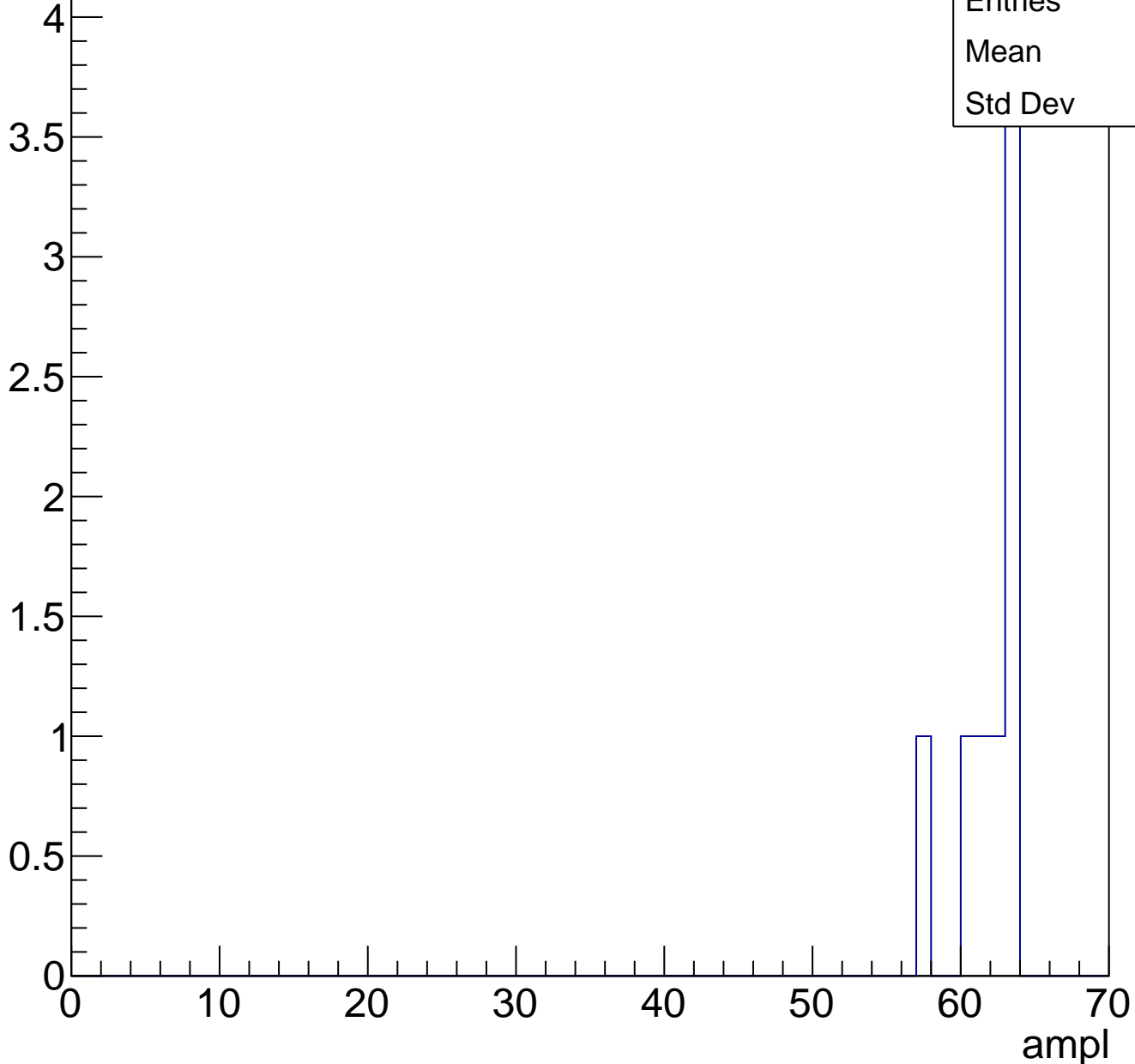
Entries	54
Mean	58.28
Std Dev	8.564



# B1L102S, U16-ch32, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch32, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch33, adc0

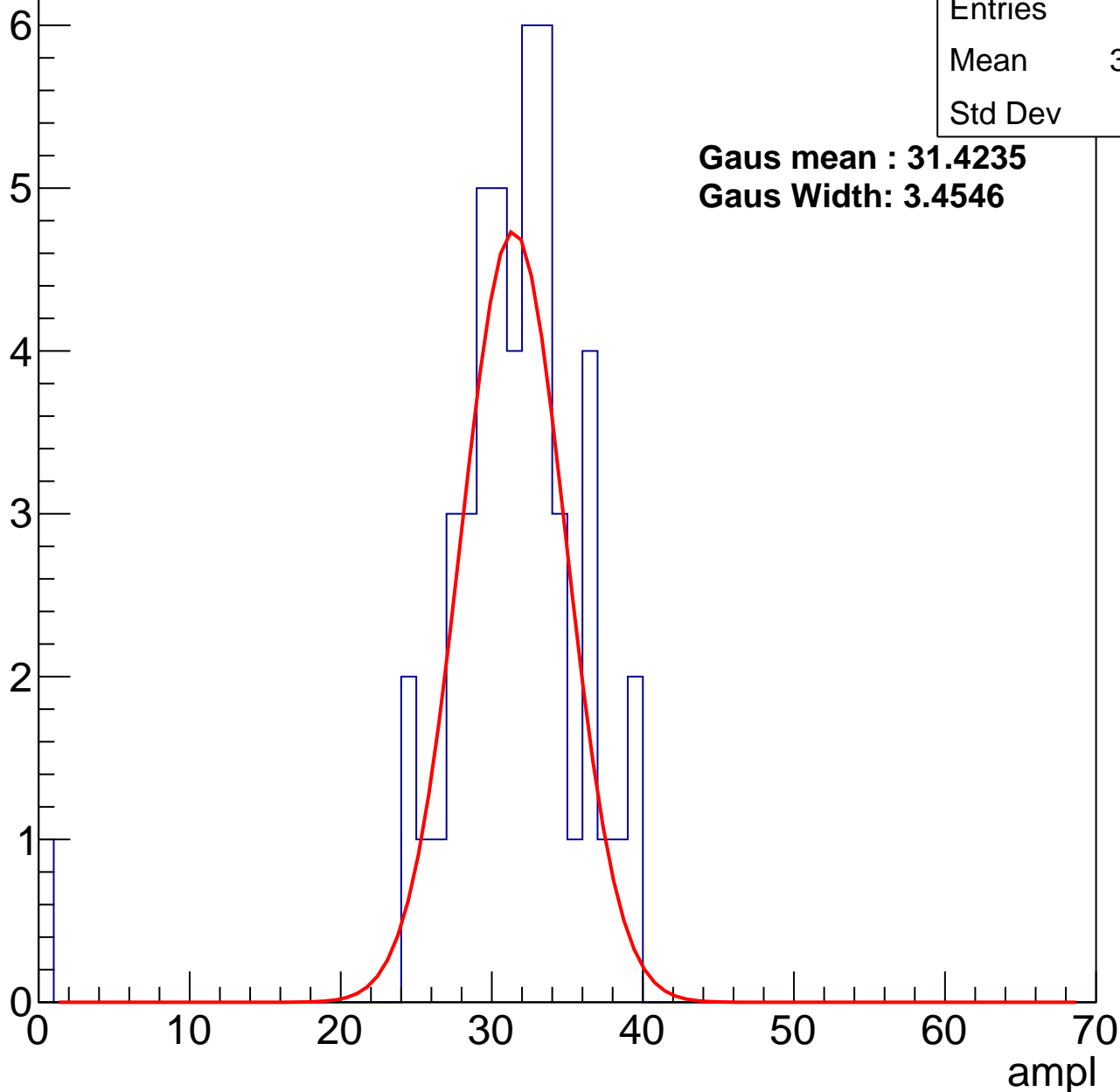
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	30.76
Std Dev	5.72

**Gaus mean : 31.4235**

**Gaus Width: 3.4546**



# B1L102S, U16-ch33, adc1

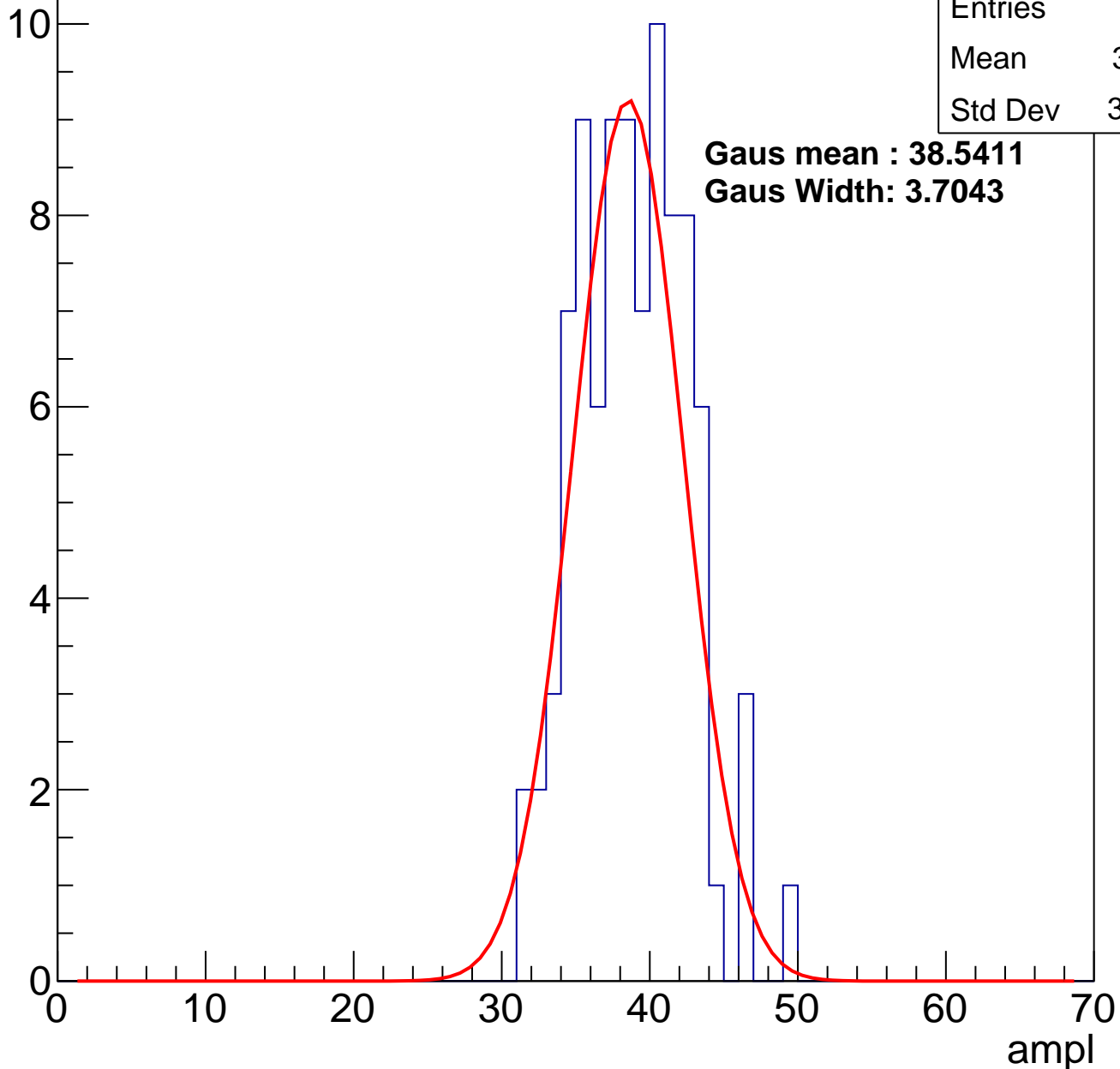
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	91
Mean	38.41
Std Dev	3.634

**Gaus mean : 38.5411**

**Gaus Width: 3.7043**

Entry



# B1L102S, U16-ch33, adc2

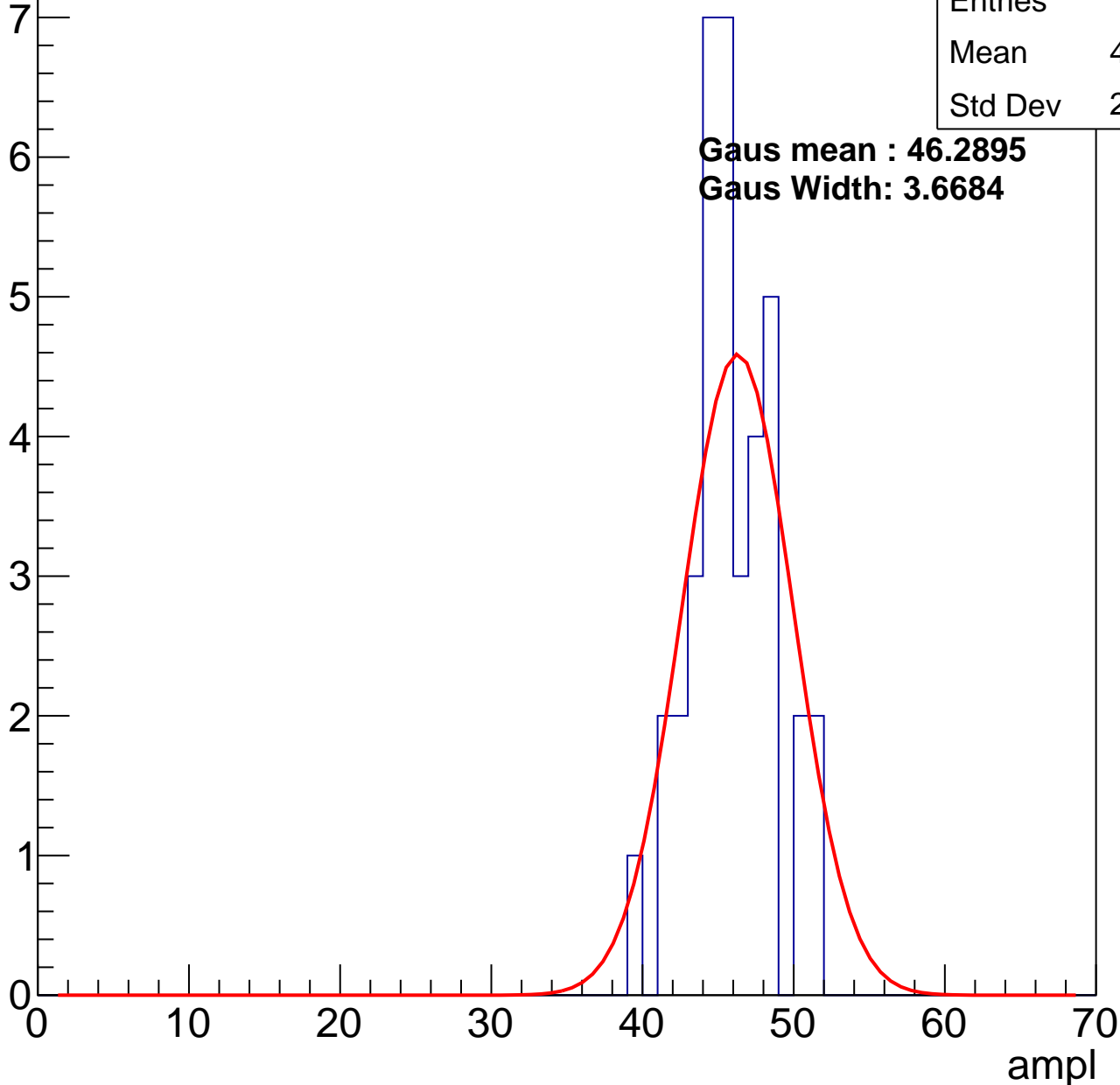
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	38
Mean	45.39
Std Dev	2.739

**Gaus mean : 46.2895**

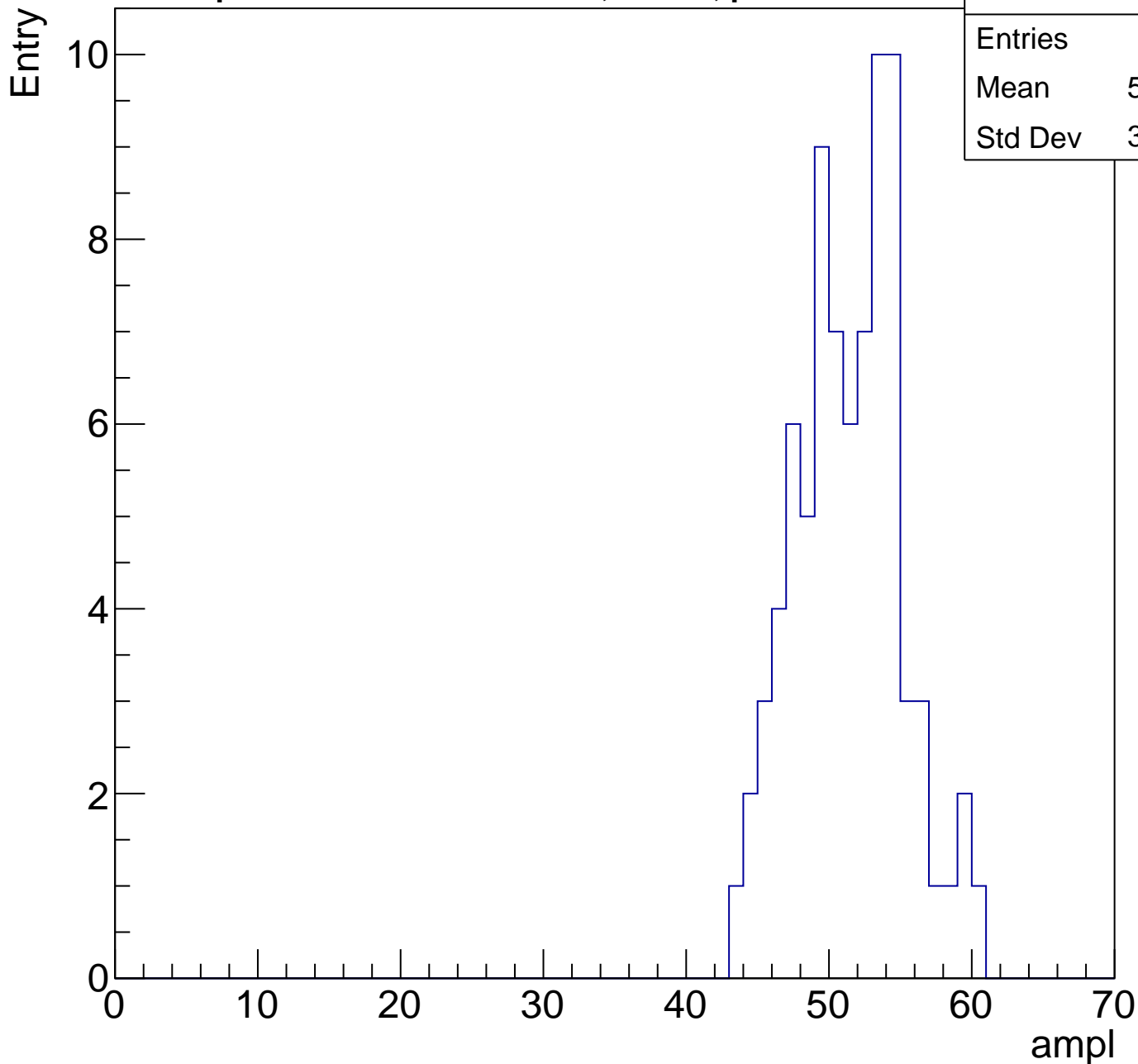
**Gaus Width: 3.6684**



# B1L102S, U16-ch33, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	81
Mean	50.98
Std Dev	3.698

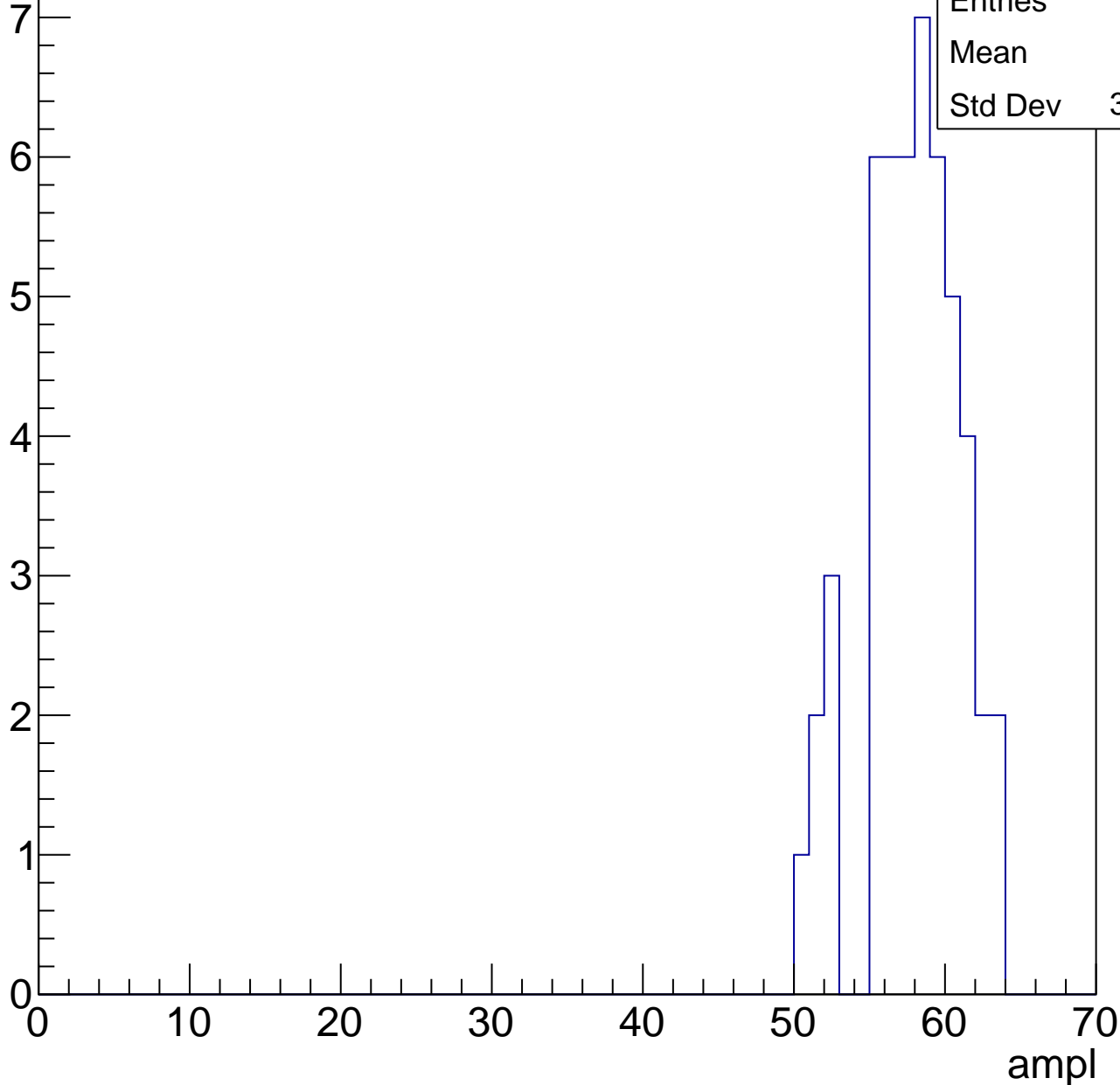


# B1L102S, U16-ch33, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	57.4
Std Dev	3.098

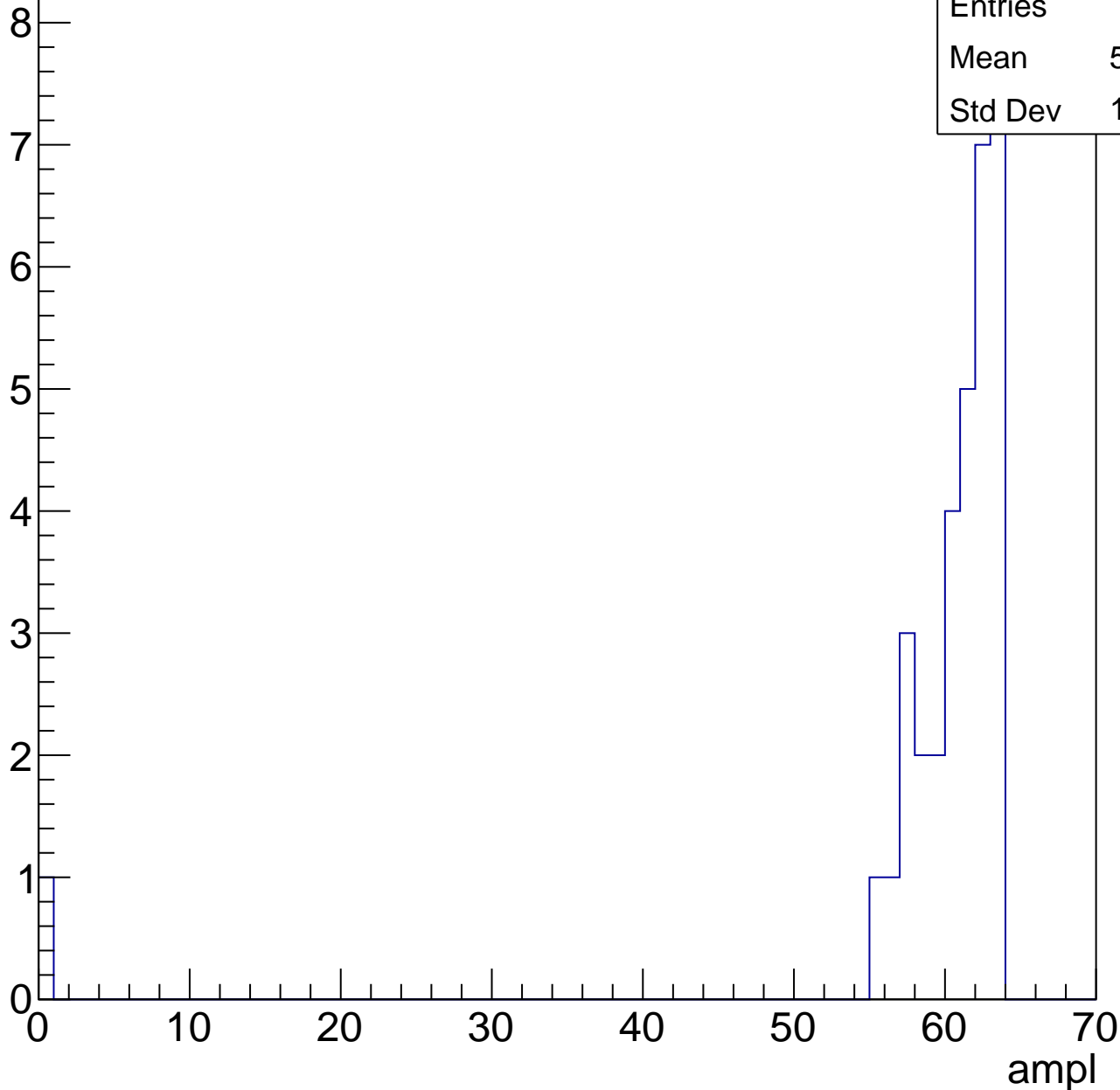


# B1L102S, U16-ch33, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	34
Mean	58.79
Std Dev	10.48



# B1L102S, U16-ch33, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch33, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U16-ch34, adc0

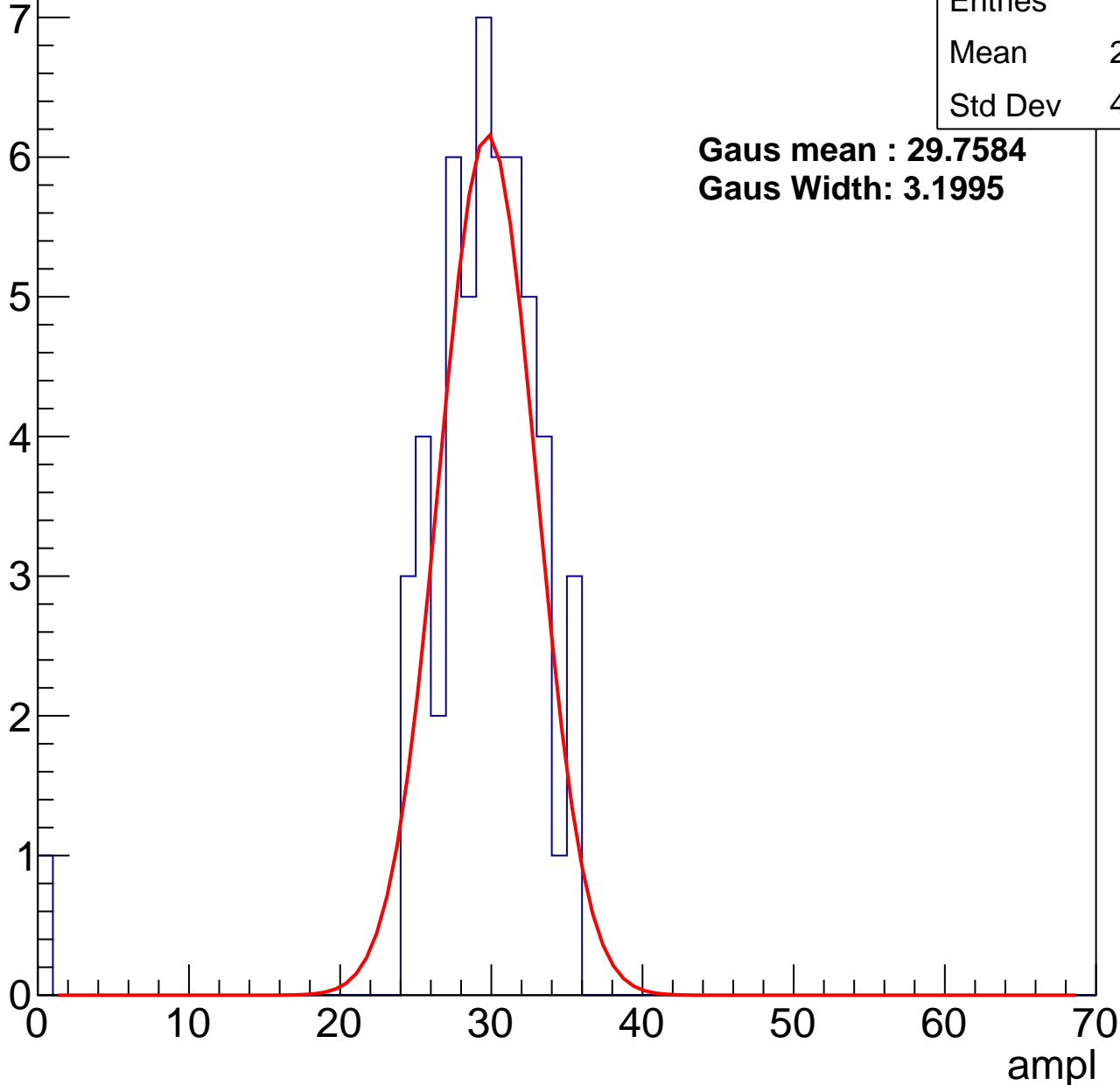
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	28.79
Std Dev	4.946

**Gaus mean : 29.7584**

**Gaus Width: 3.1995**



# B1L102S, U16-ch34, adc1

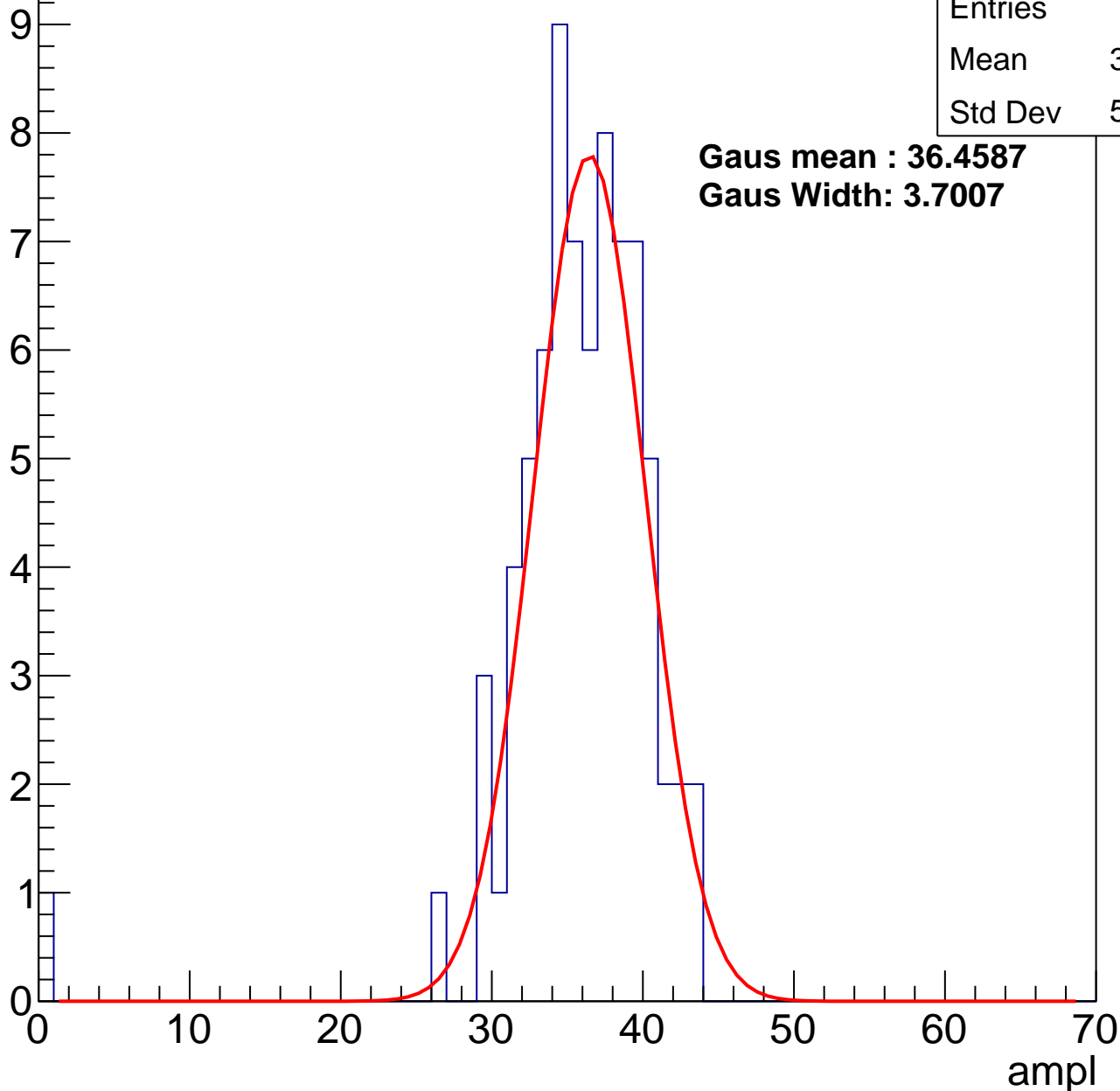
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	35.25
Std Dev	5.395

**Gaus mean : 36.4587**

**Gaus Width: 3.7007**



# B1L102S, U16-ch34, adc2

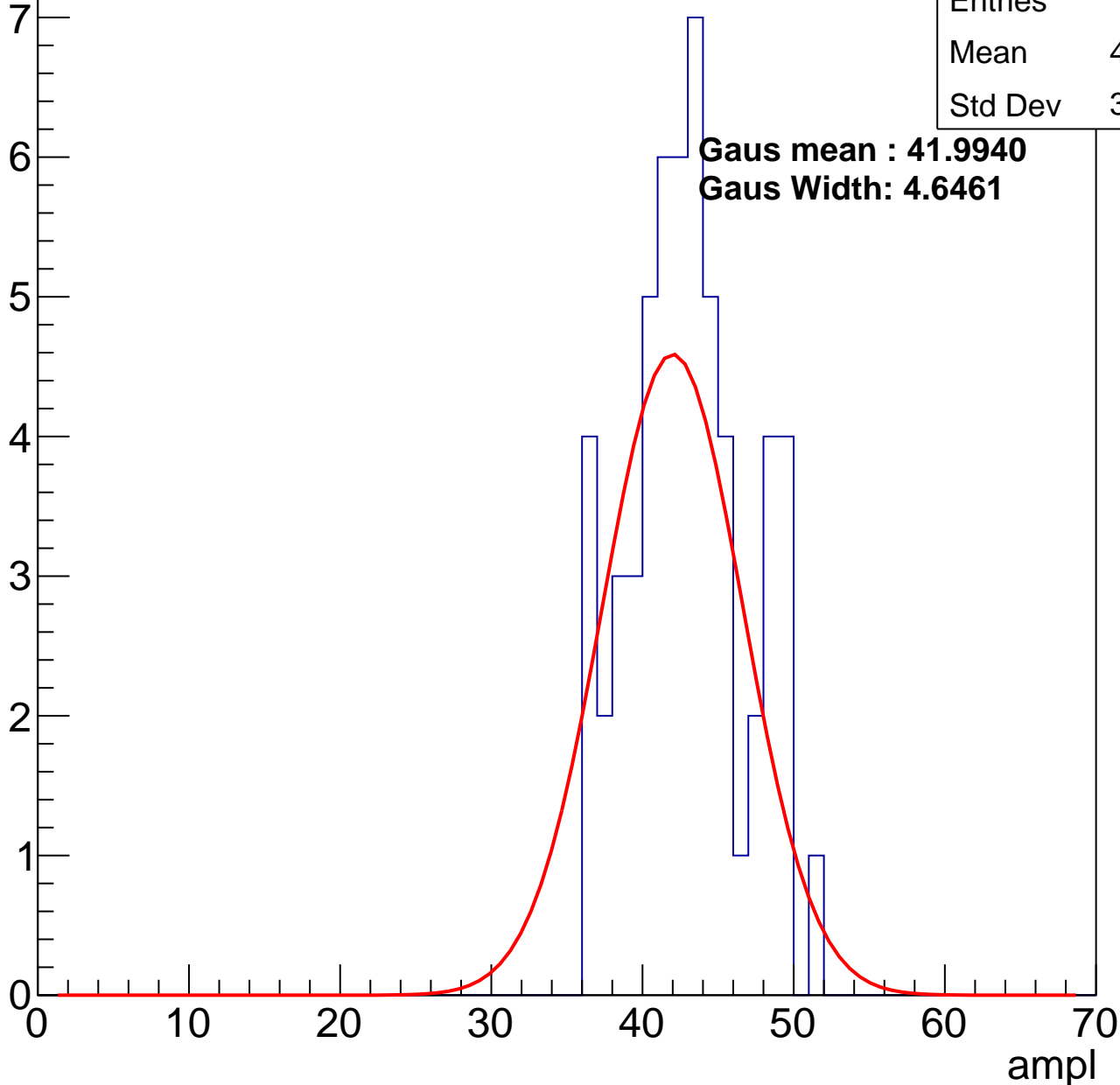
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	42.58
Std Dev	3.806

**Gaus mean : 41.9940**

**Gaus Width: 4.6461**

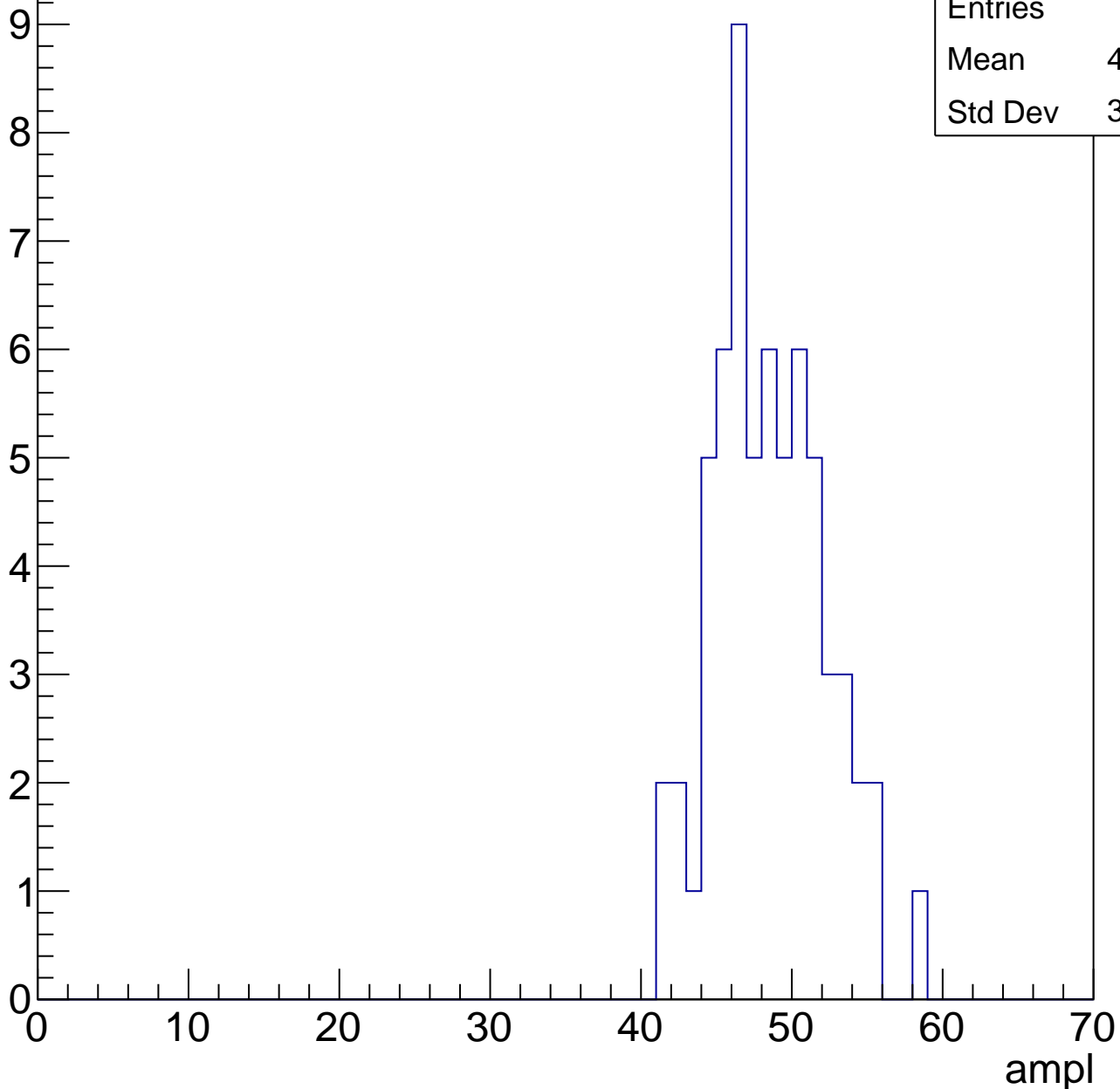


# B1L102S, U16-ch34, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	48.05
Std Dev	3.645

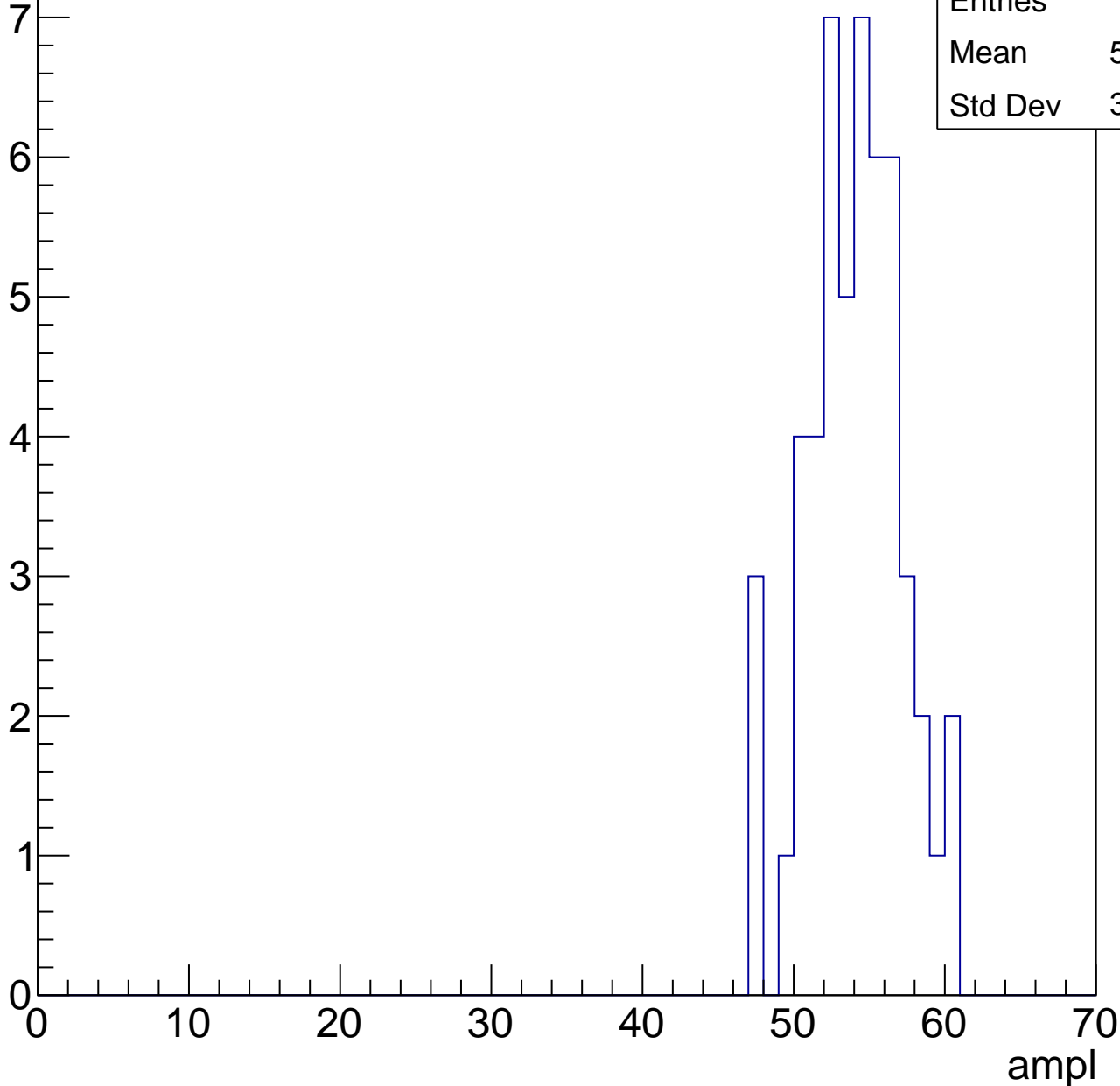


# B1L102S, U16-ch34, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

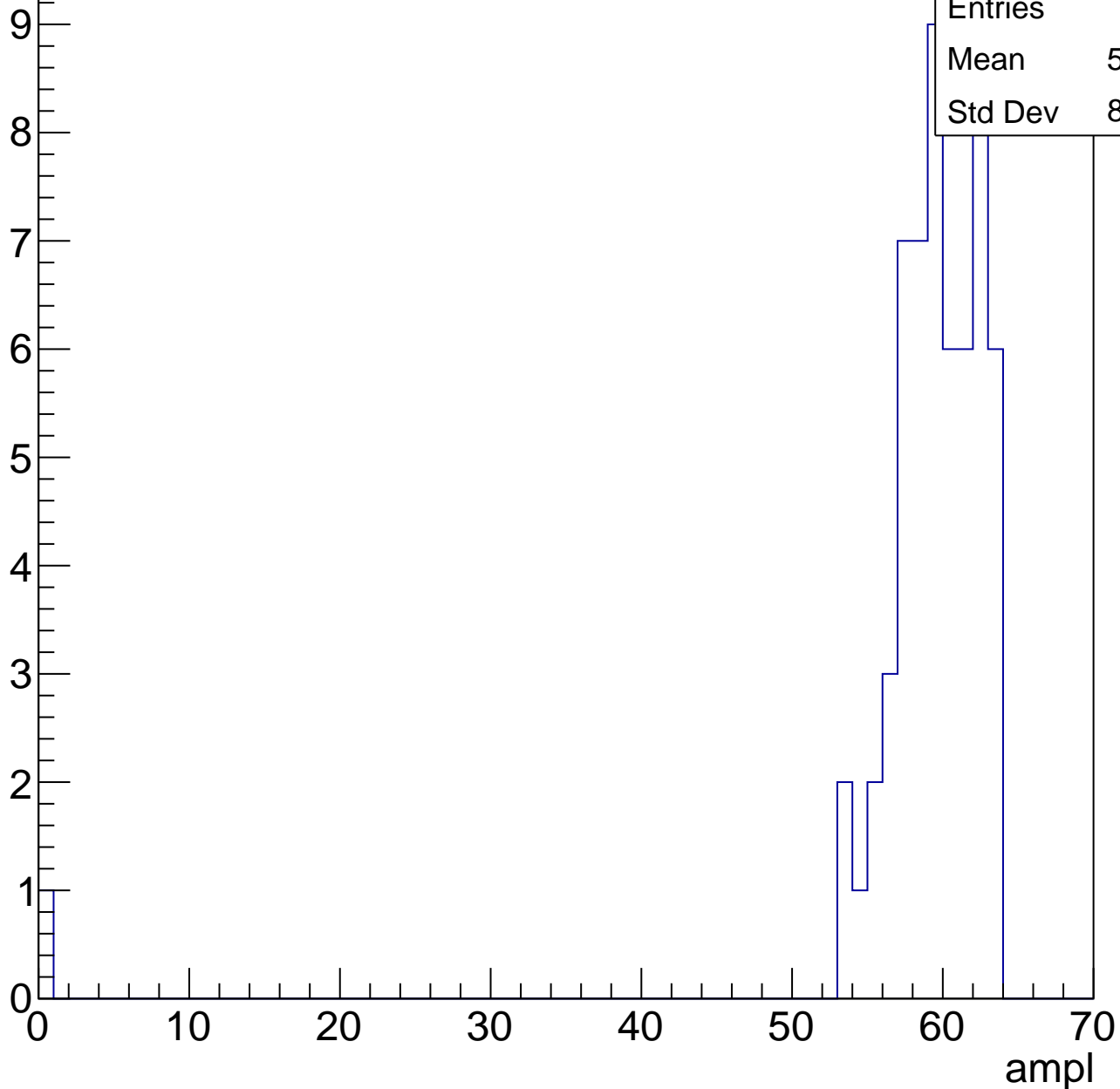
Entries	51
Mean	53.59
Std Dev	3.075



# B1L102S, U16-ch34, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

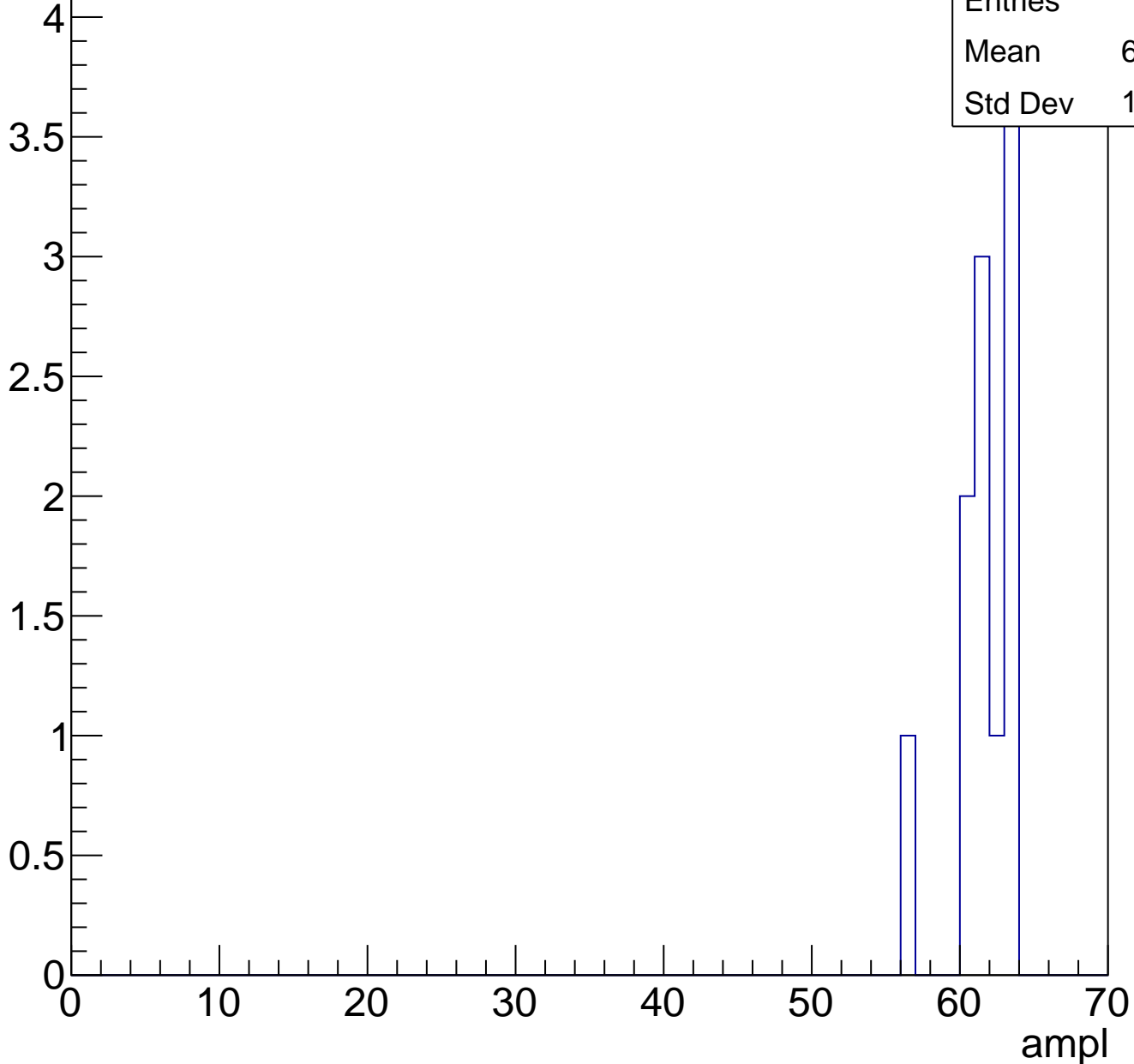
Entry



# B1L102S, U16-ch34, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

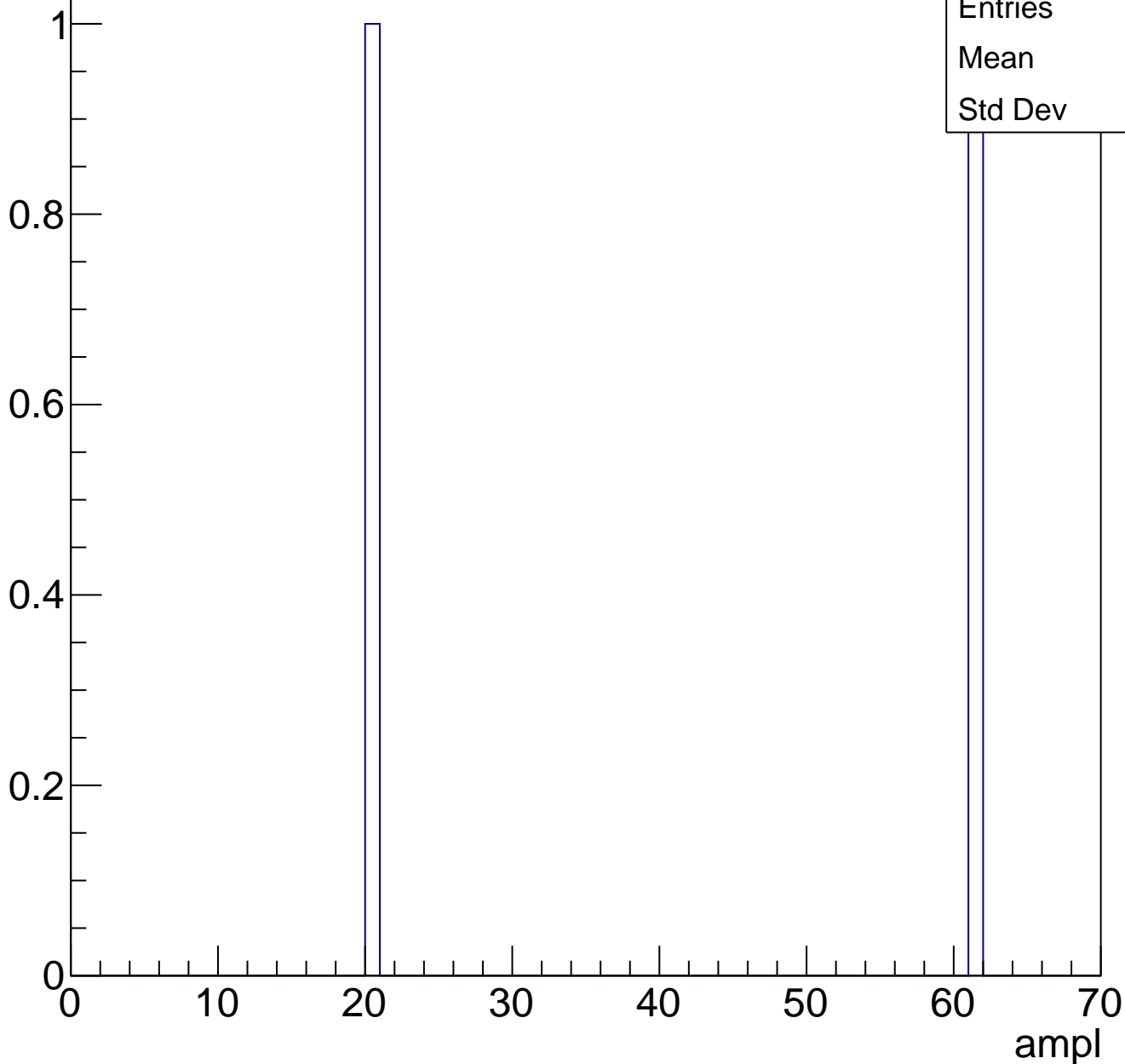




# B1L102S, U16-ch34, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch35, adc0

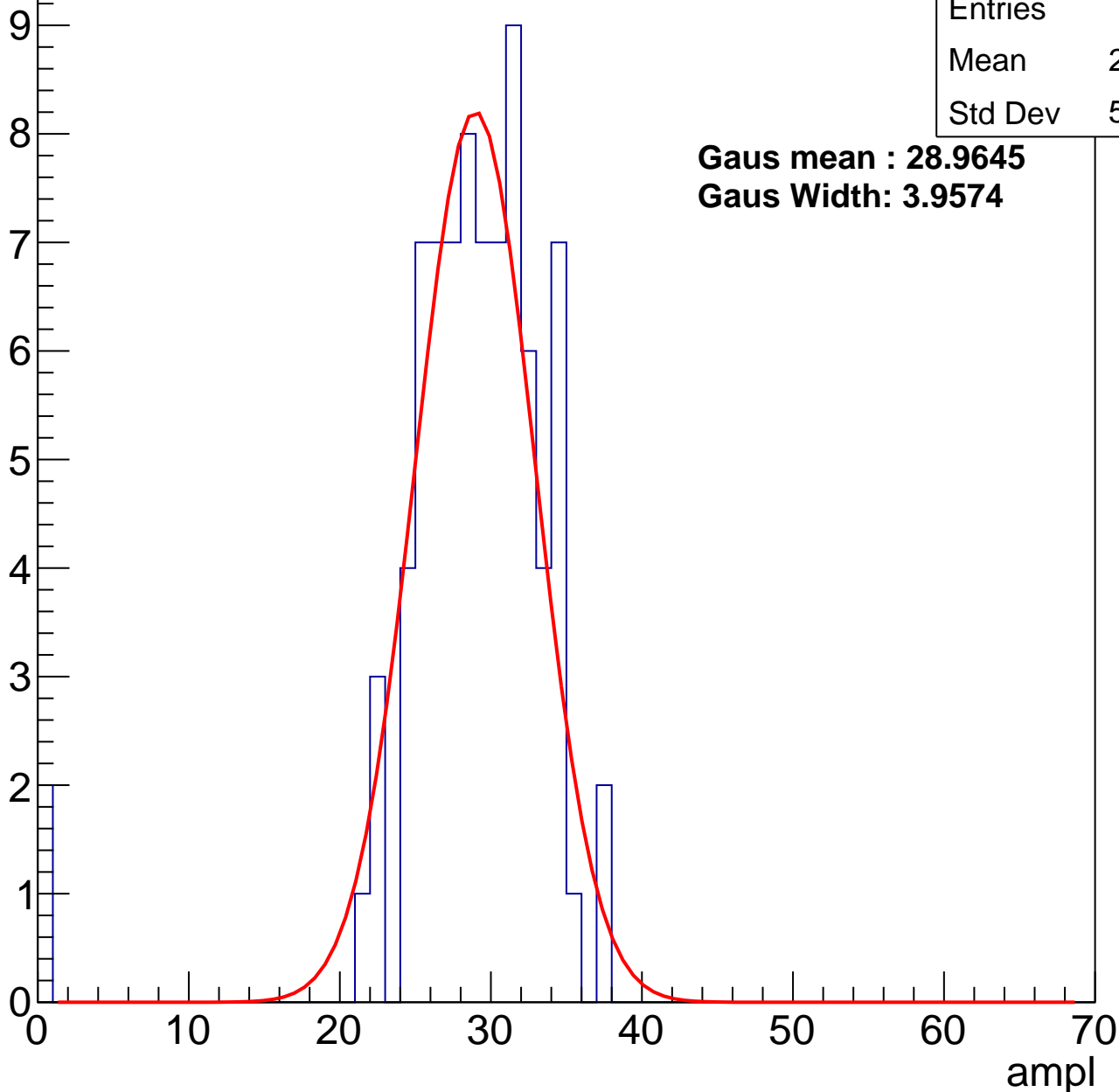
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	28.24
Std Dev	5.692

**Gaus mean : 28.9645**

**Gaus Width: 3.9574**



# B1L102S, U16-ch35, adc1

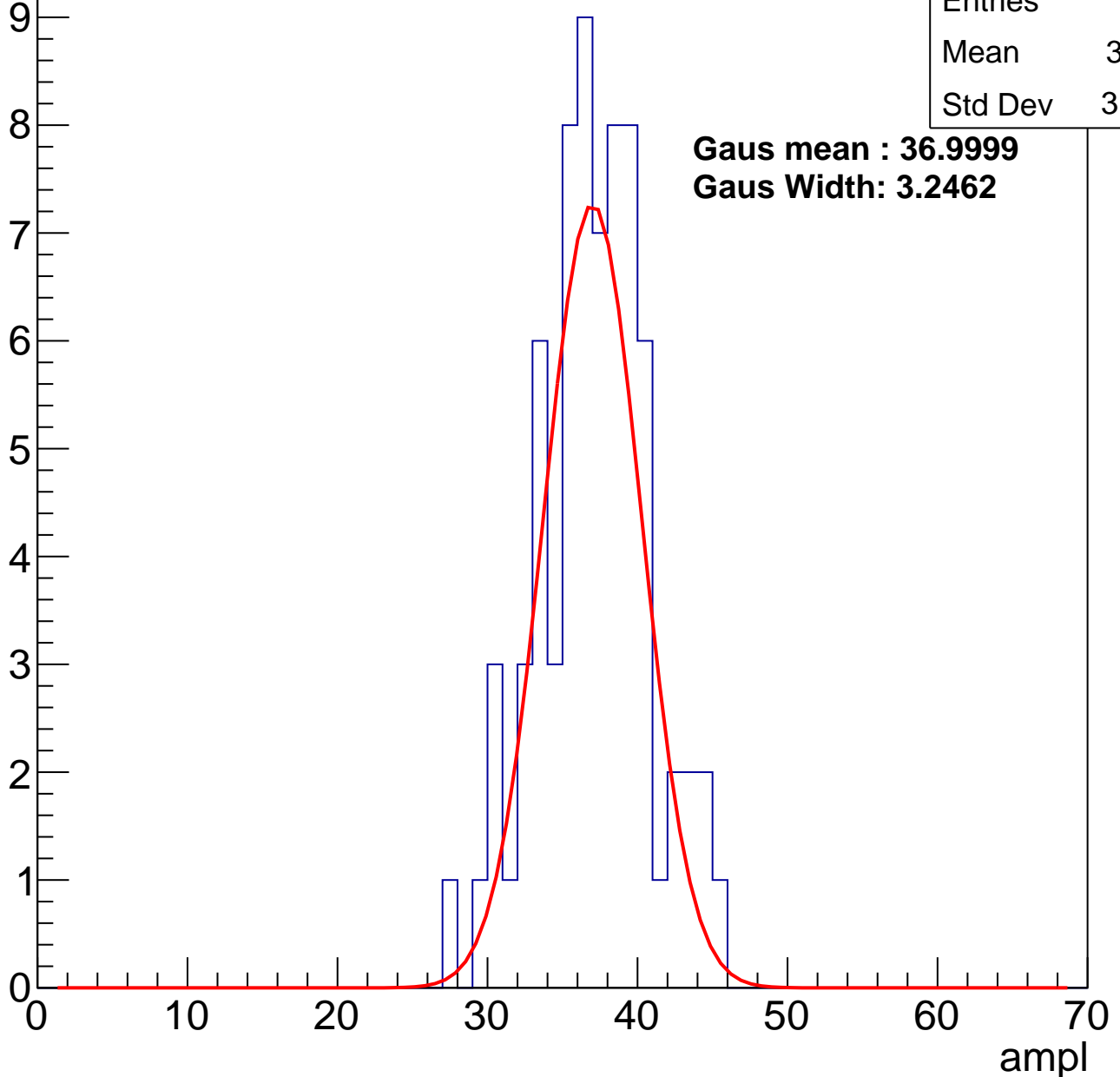
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	36.61
Std Dev	3.669

**Gaus mean : 36.9999**

**Gaus Width: 3.2462**



# B1L102S, U16-ch35, adc2

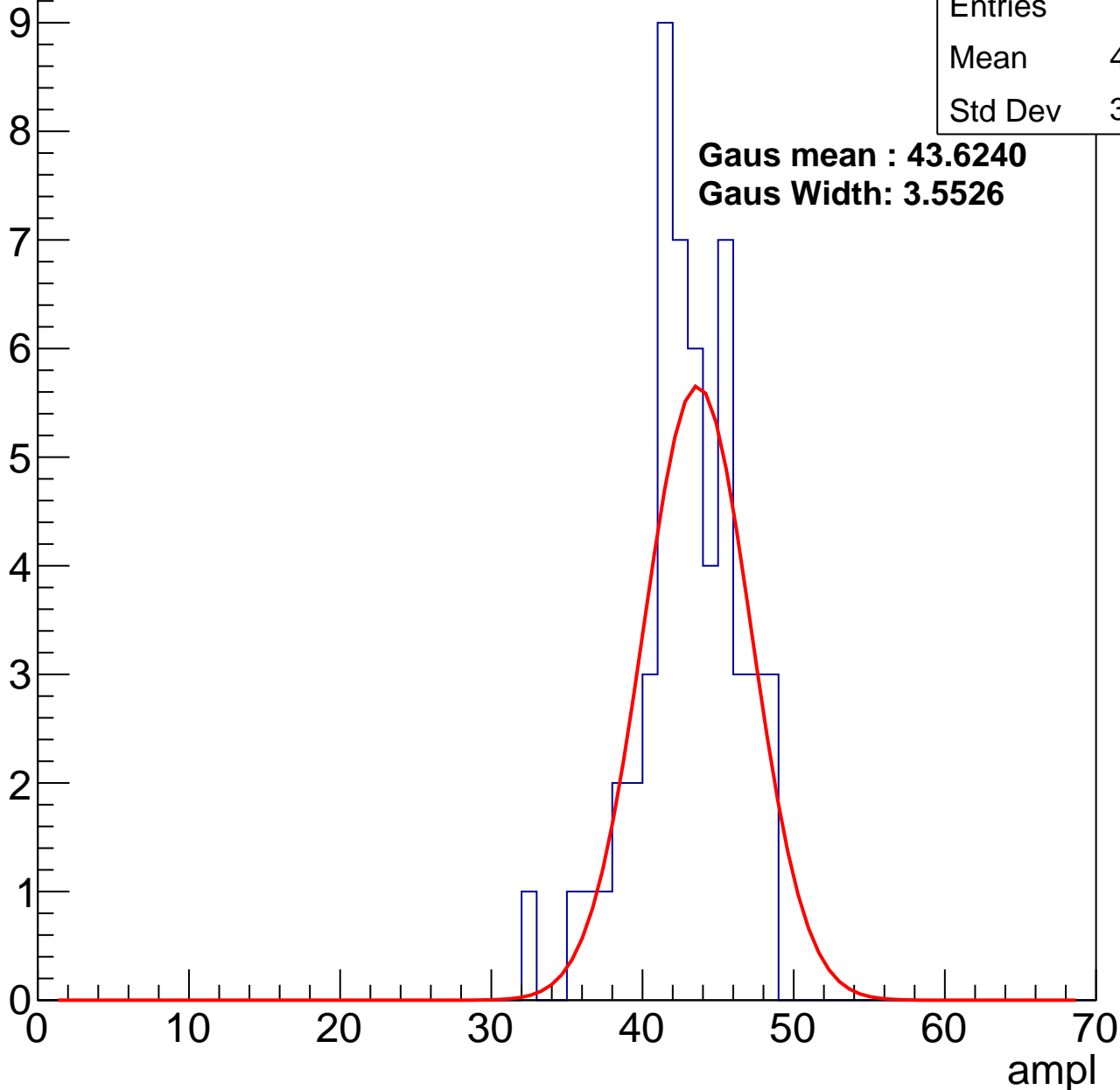
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	42.43
Std Dev	3.328

**Gaus mean : 43.6240**

**Gaus Width: 3.5526**

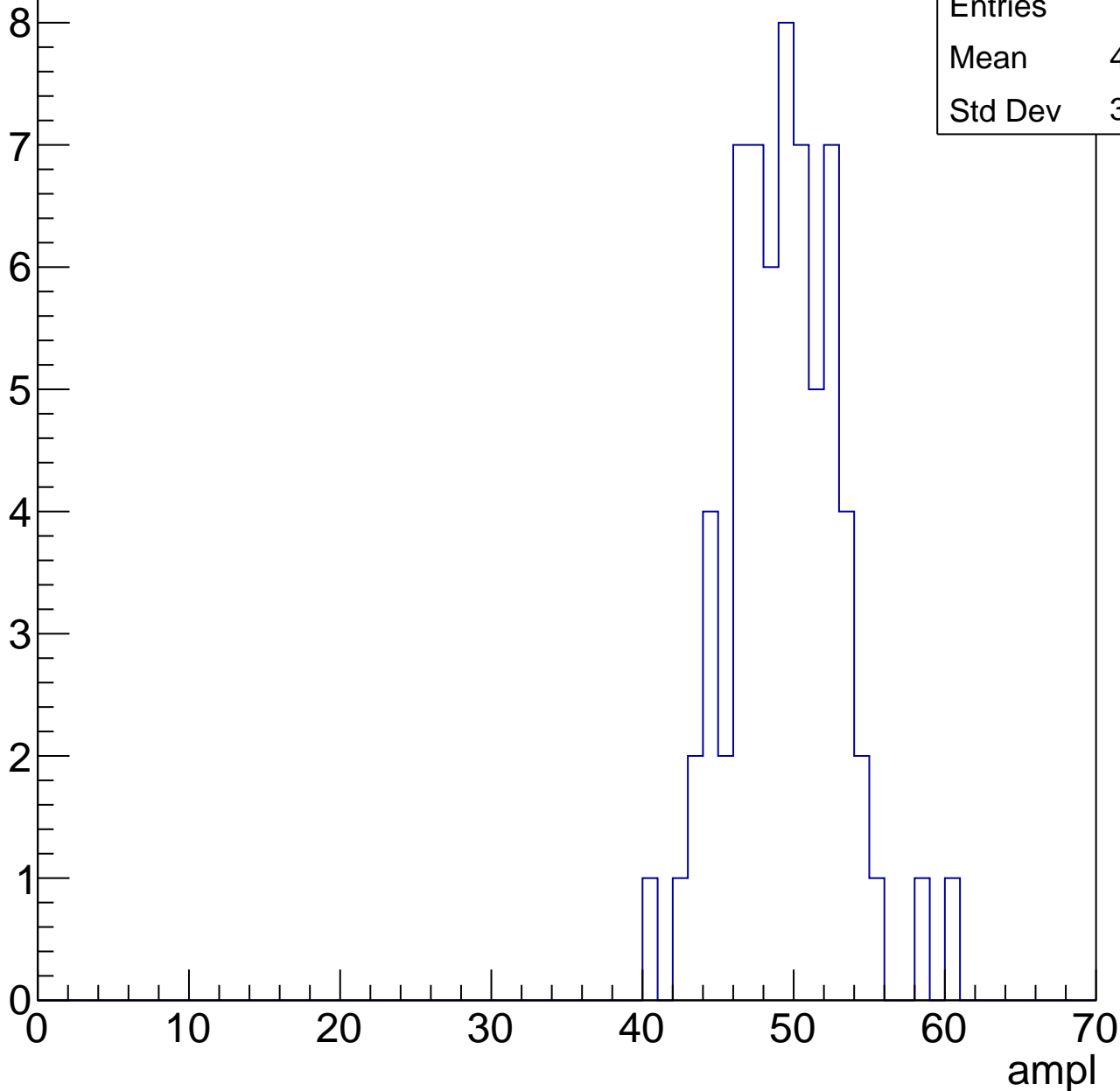


# B1L102S, U16-ch35, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

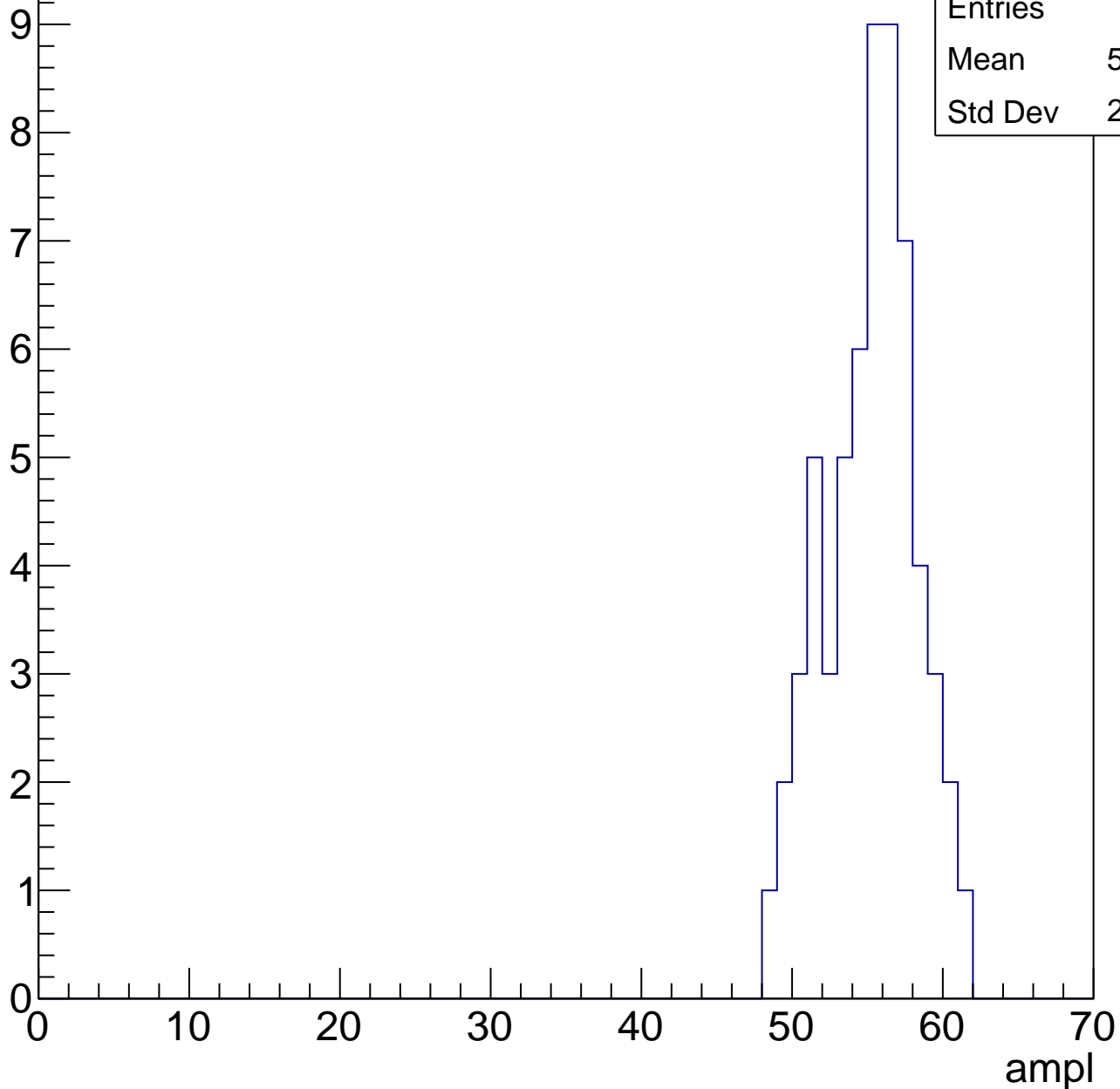
Entries	66
Mean	48.89
Std Dev	3.635



# B1L102S, U16-ch35, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

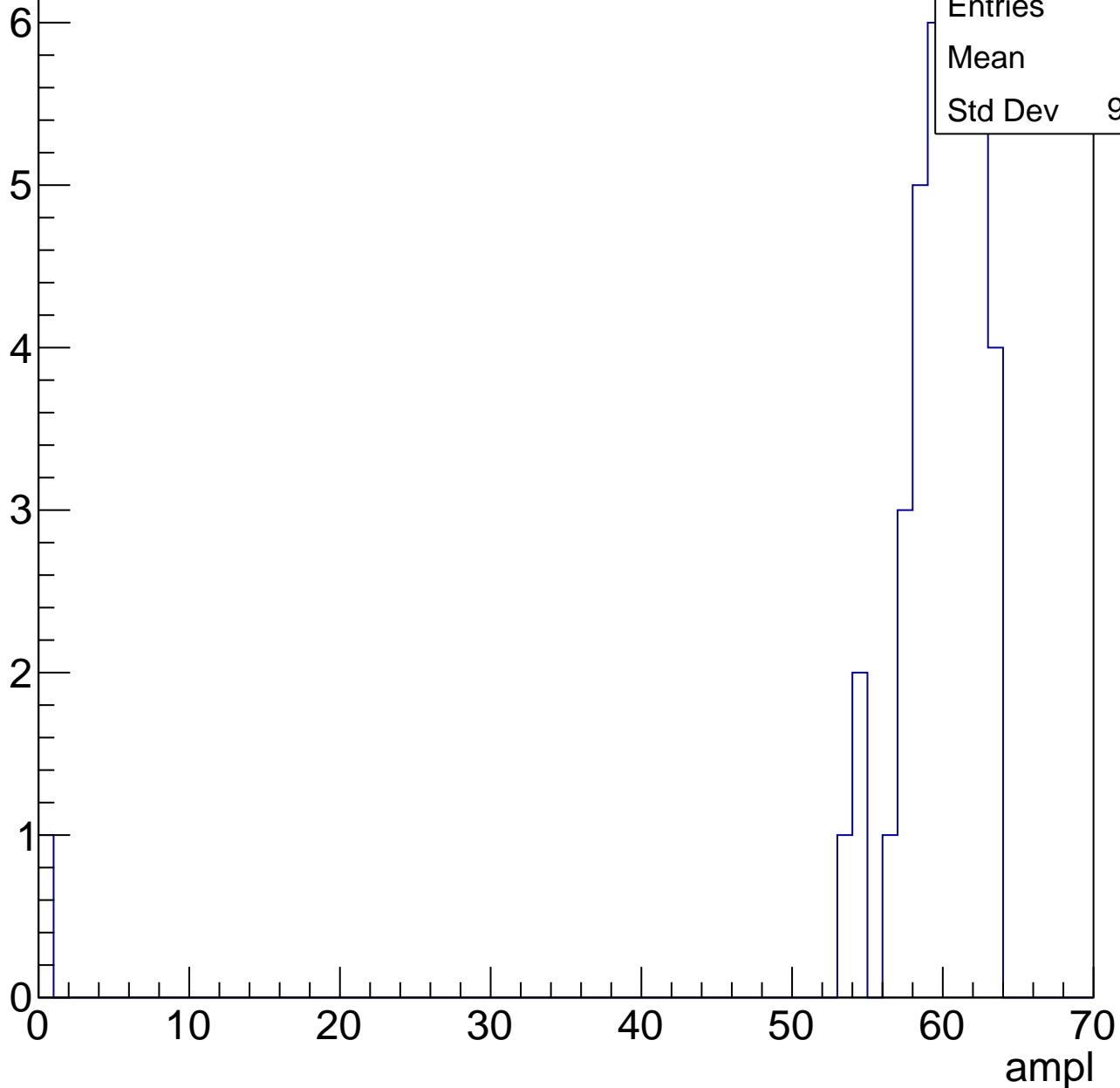
Entry



# B1L102S, U16-ch35, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

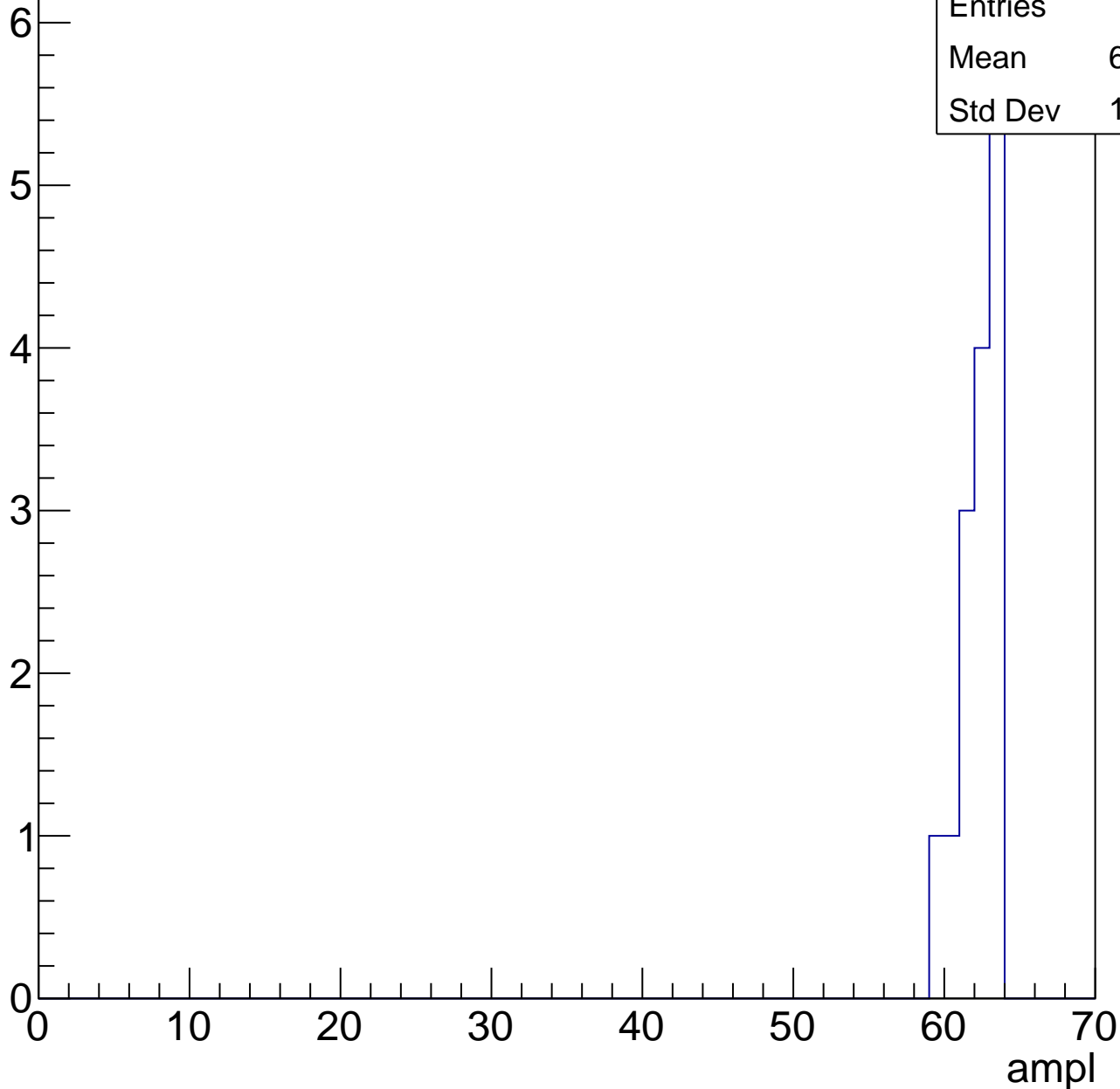


# B1L102S, U16-ch35, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	15
Mean	61.87
Std Dev	1.204





# B1L102S, U16-ch35, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	20
Std Dev	0

# B1L102S, U16-ch36, adc0

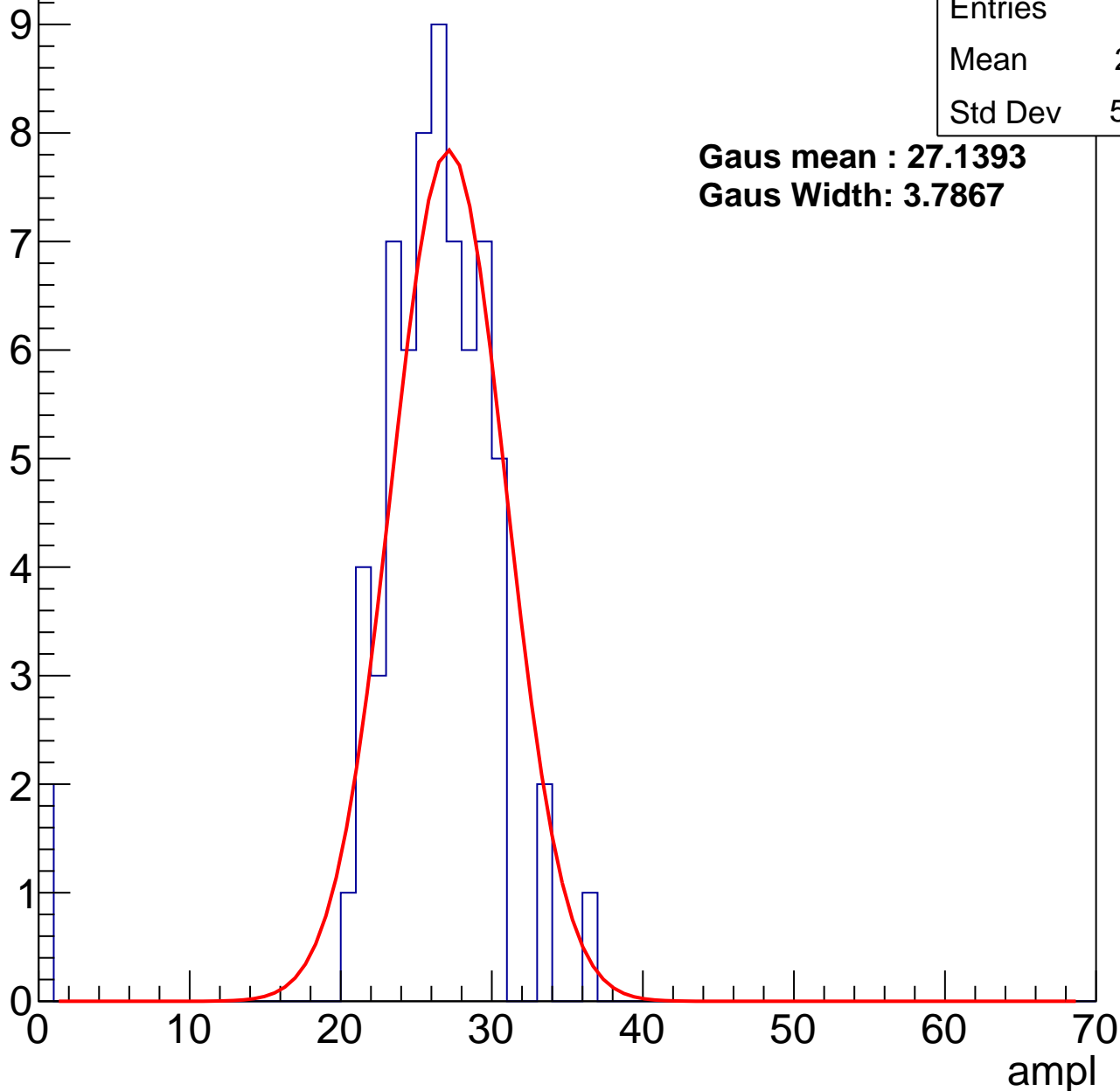
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	25.31
Std Dev	5.383

**Gaus mean : 27.1393**

**Gaus Width: 3.7867**



# B1L102S, U16-ch36, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	91
Mean	34.32
Std Dev	3.964

**Gaus mean : 34.5197**

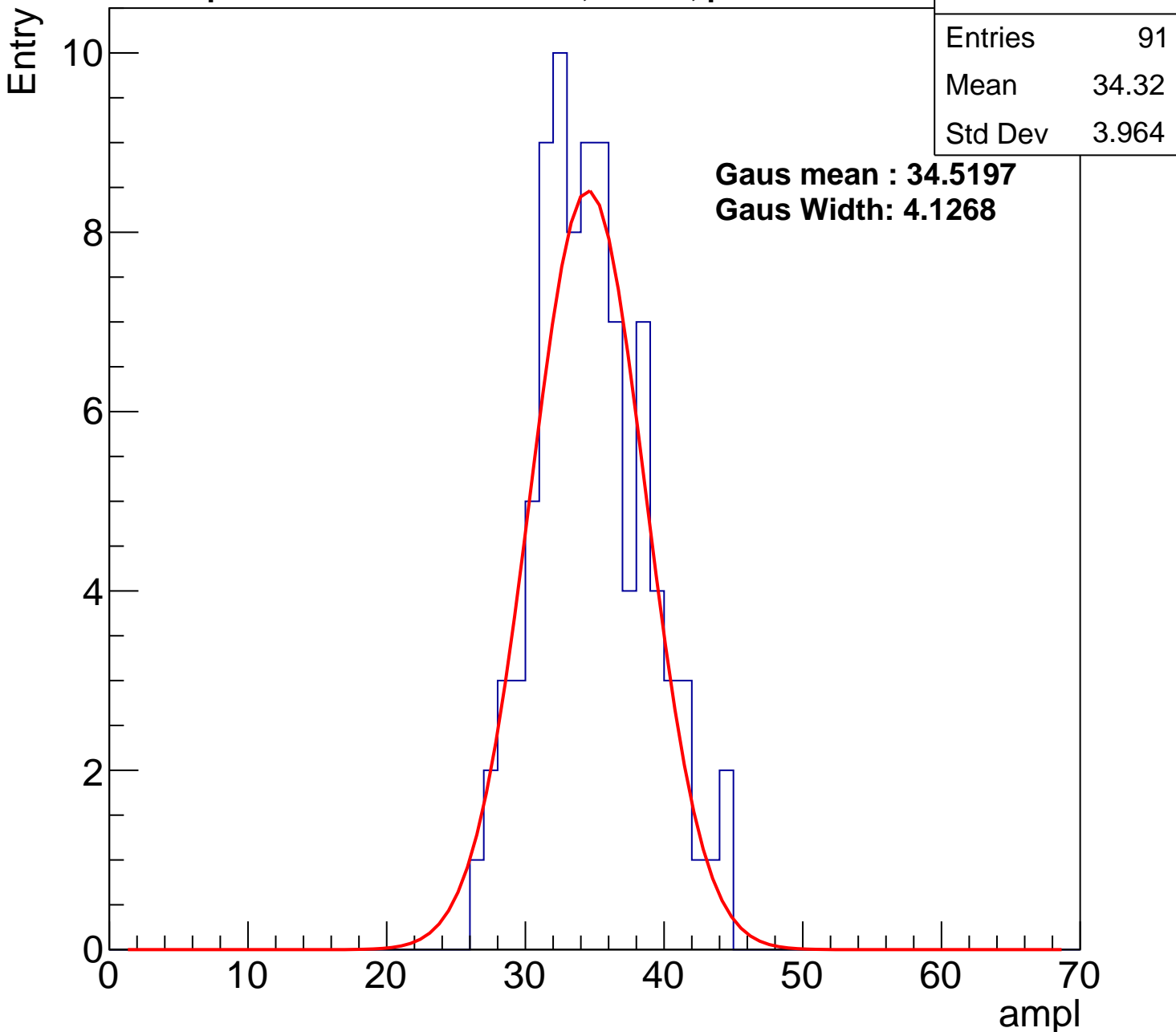
**Gaus Width: 4.1268**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U16-ch36, adc2

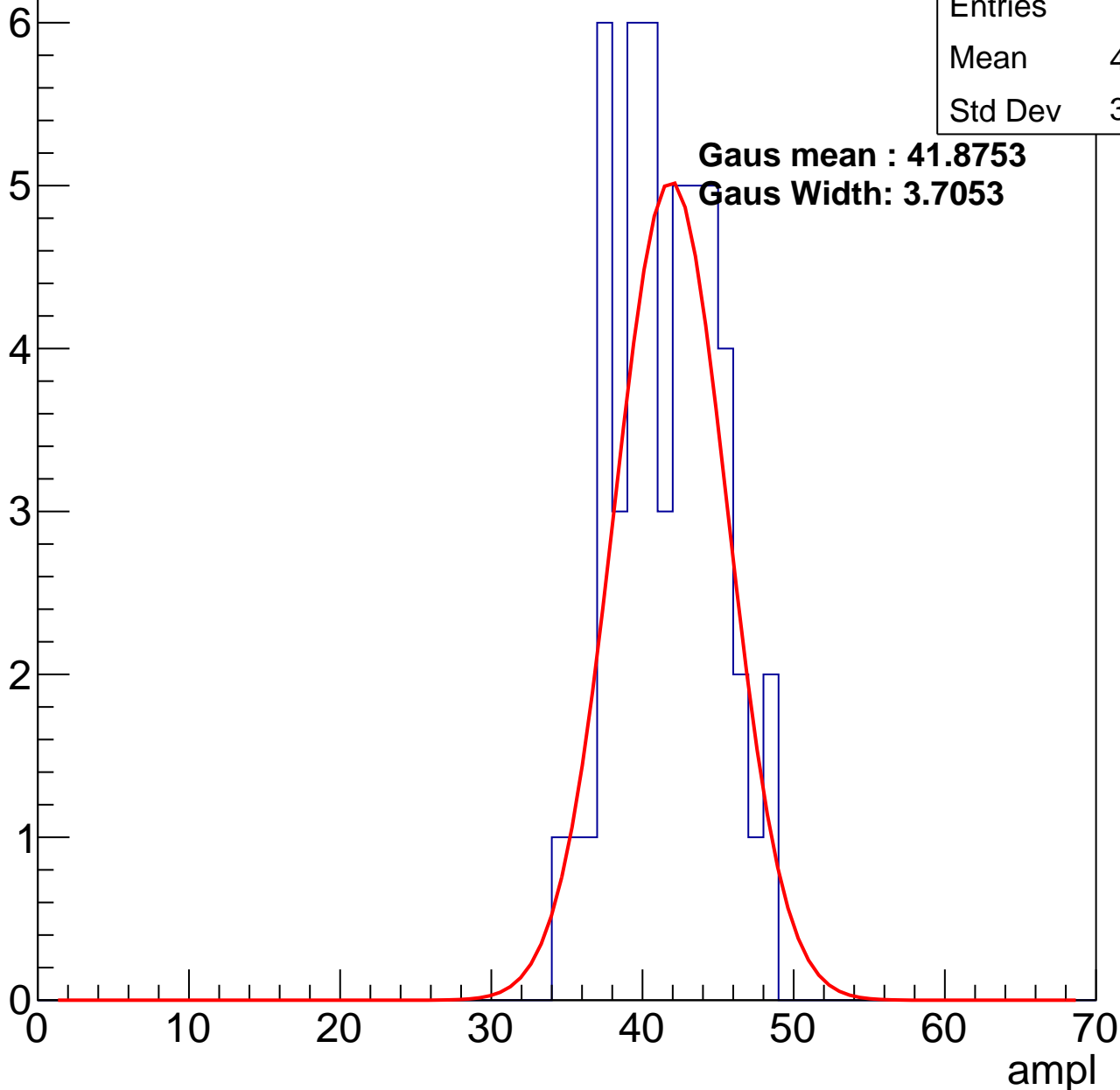
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	41.14
Std Dev	3.372

**Gaus mean : 41.8753**

**Gaus Width: 3.7053**

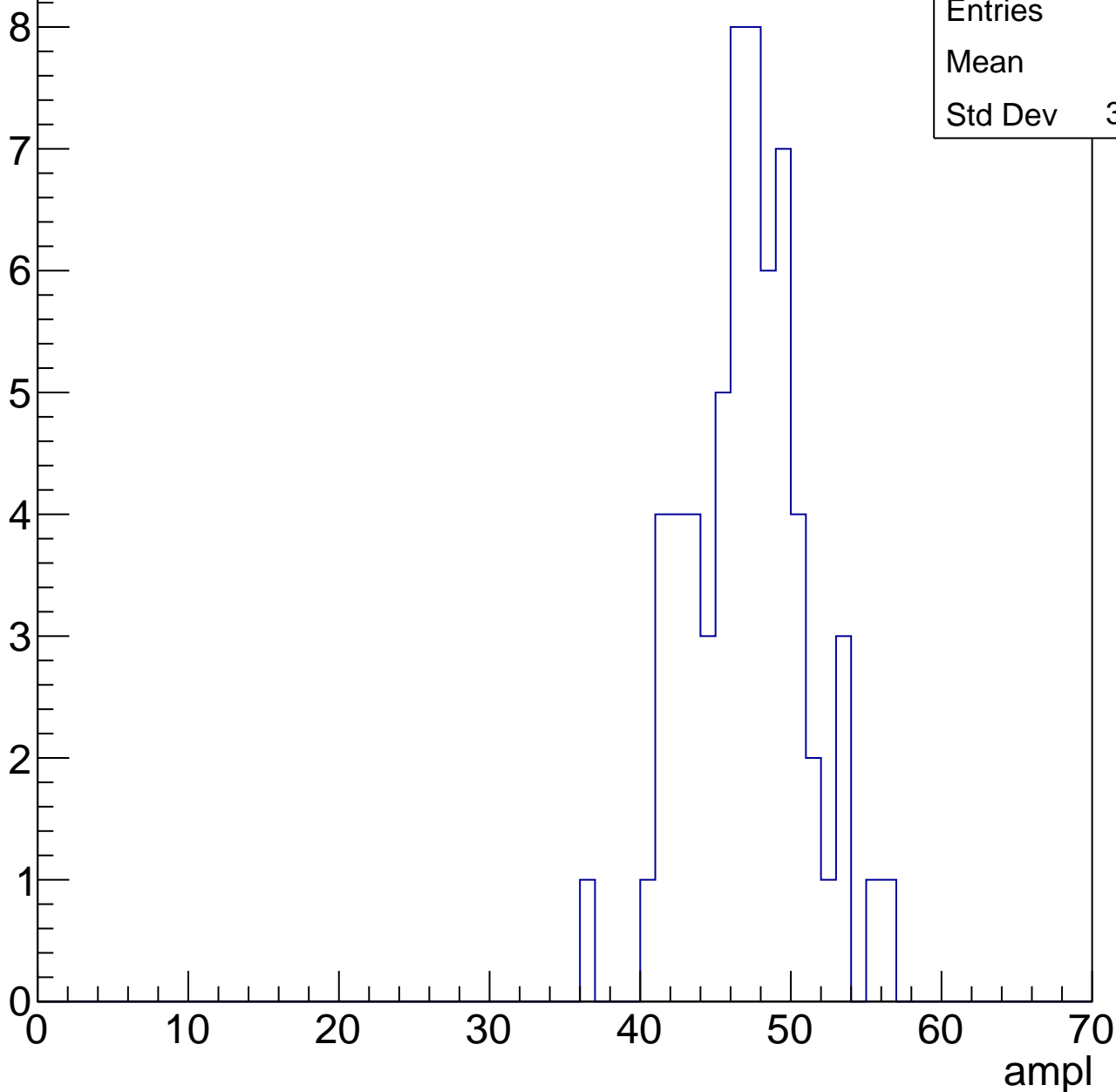


# B1L102S, U16-ch36, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	46.6
Std Dev	3.786

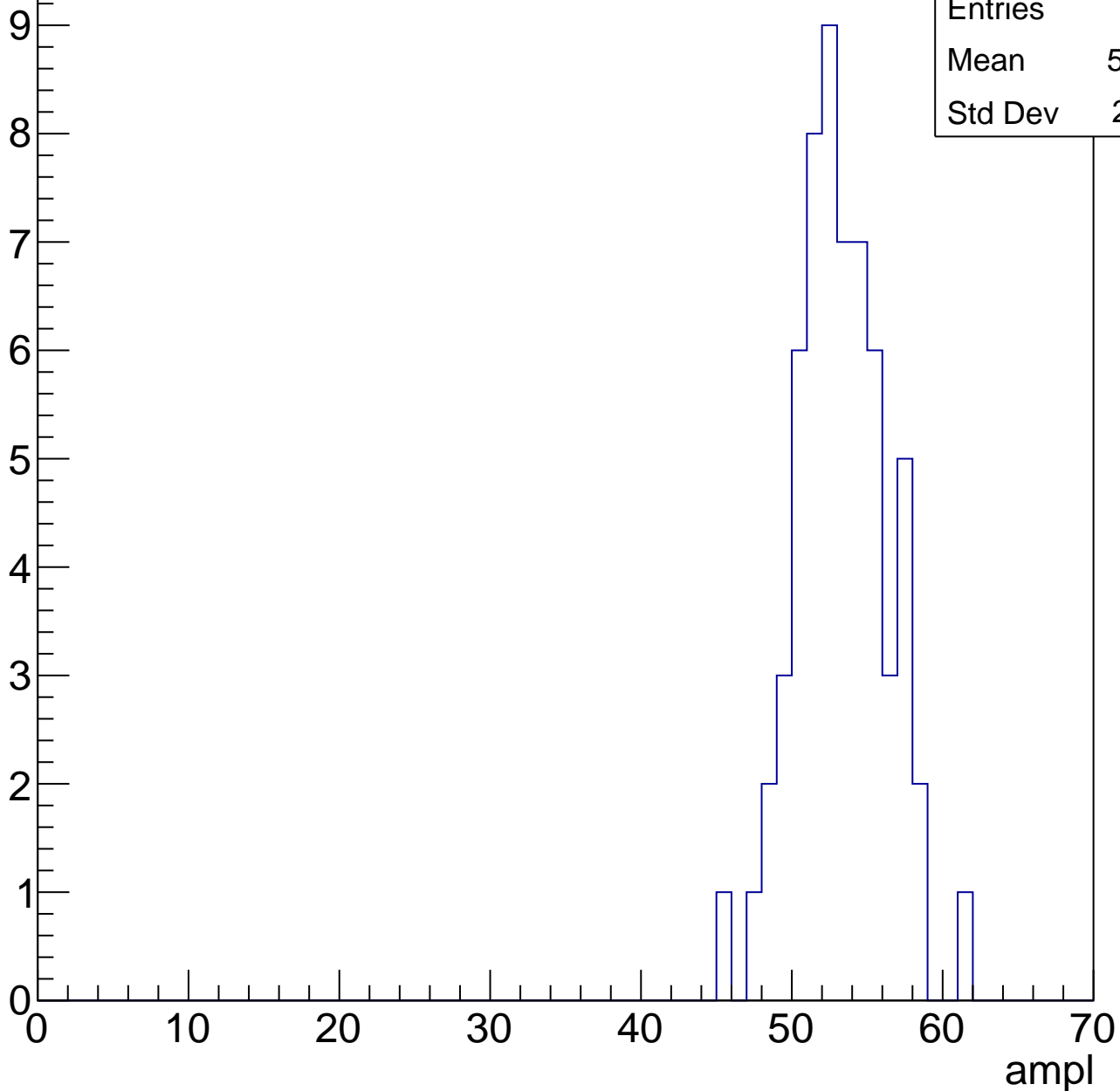


# B1L102S, U16-ch36, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	52.79
Std Dev	2.981

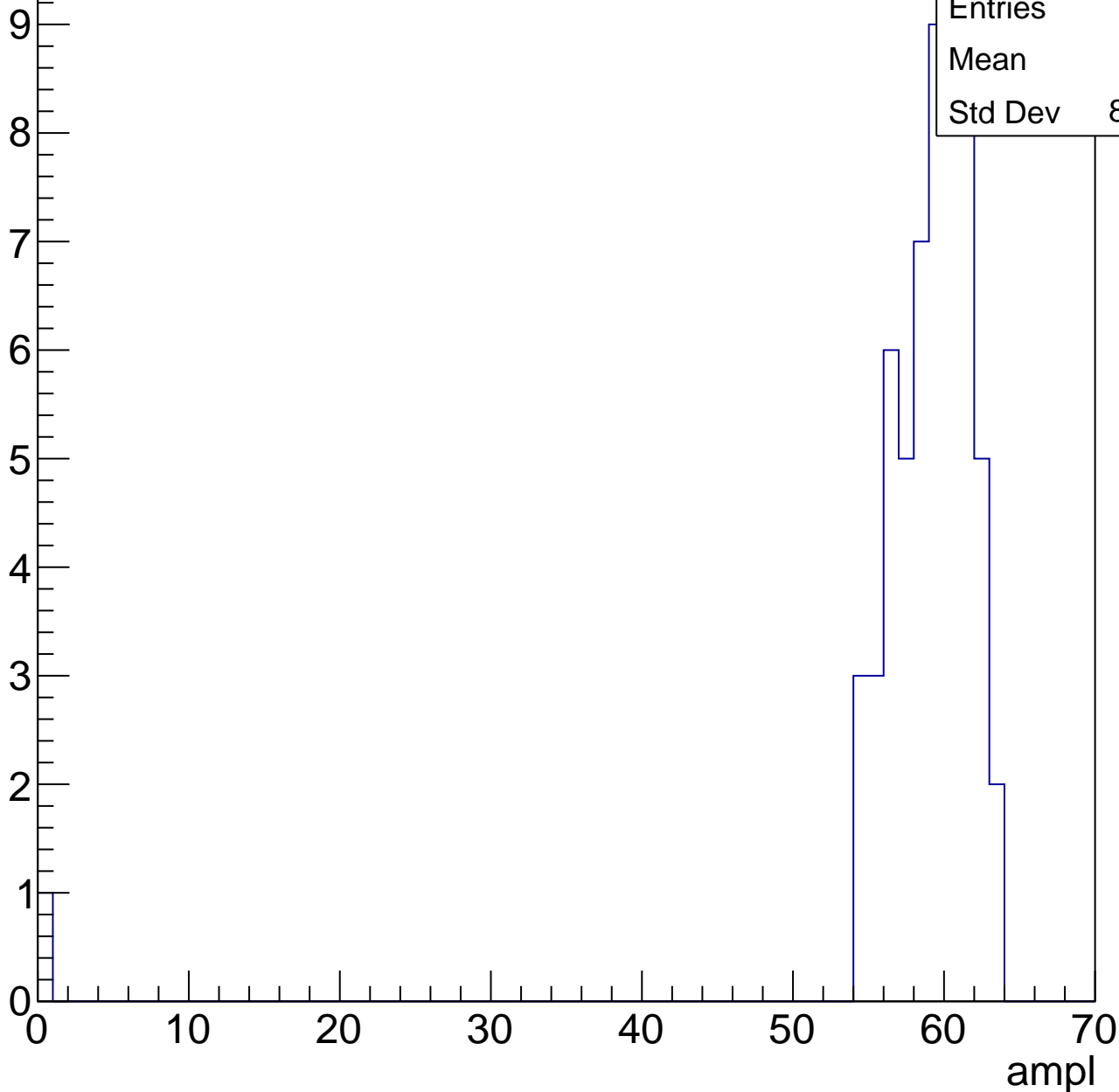


# B1L102S, U16-ch36, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	57.7
Std Dev	8.063

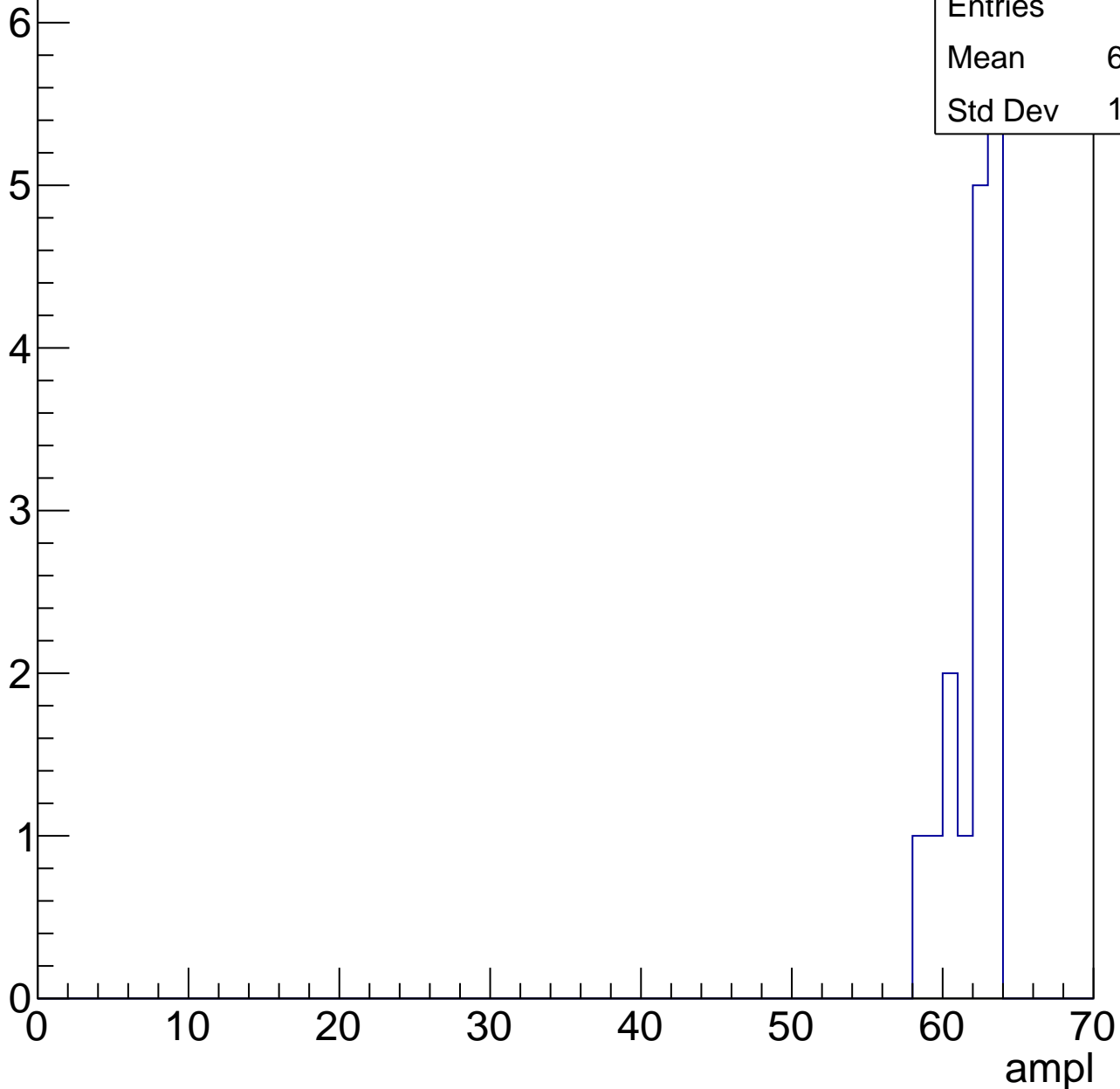


# B1L102S, U16-ch36, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	16
Mean	61.62
Std Dev	1.536

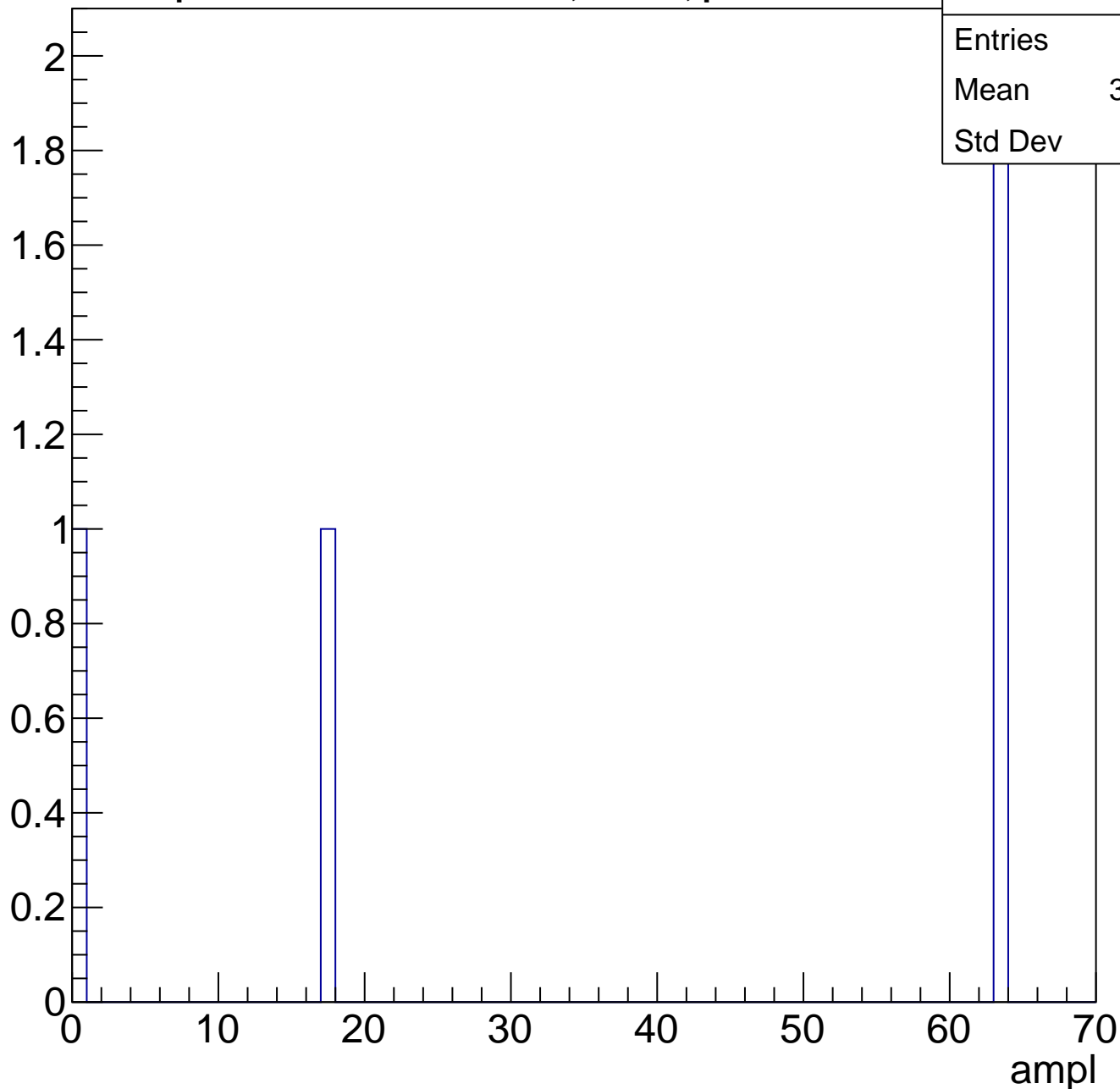




# B1L102S, U16-ch36, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	4
Mean	35.75
Std Dev	27.9

# B1L102S, U16-ch37, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	69
Mean	28.03
Std Dev	3.734

**Gaus mean : 28.5997**

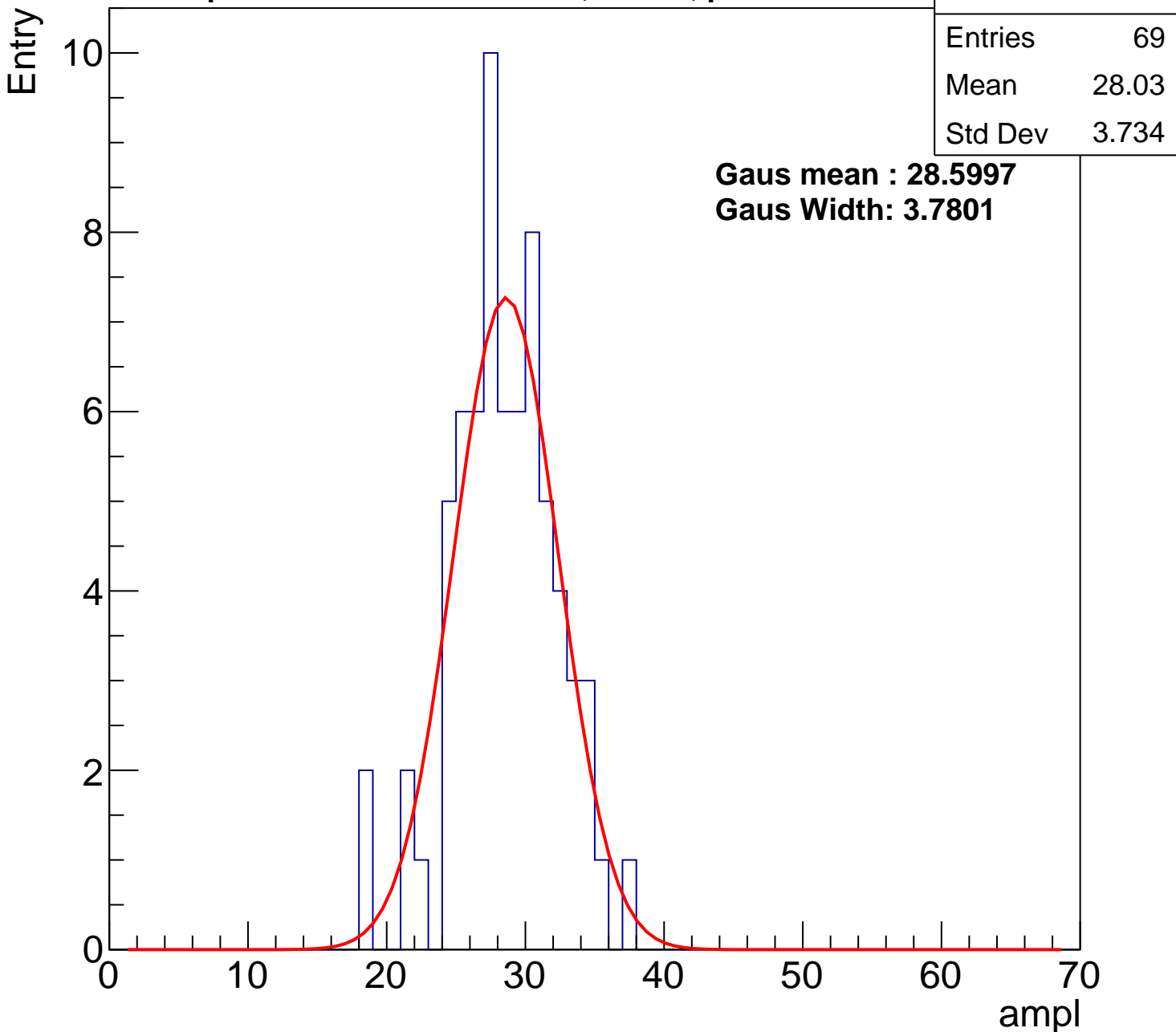
**Gaus Width: 3.7801**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U16-ch37, adc1

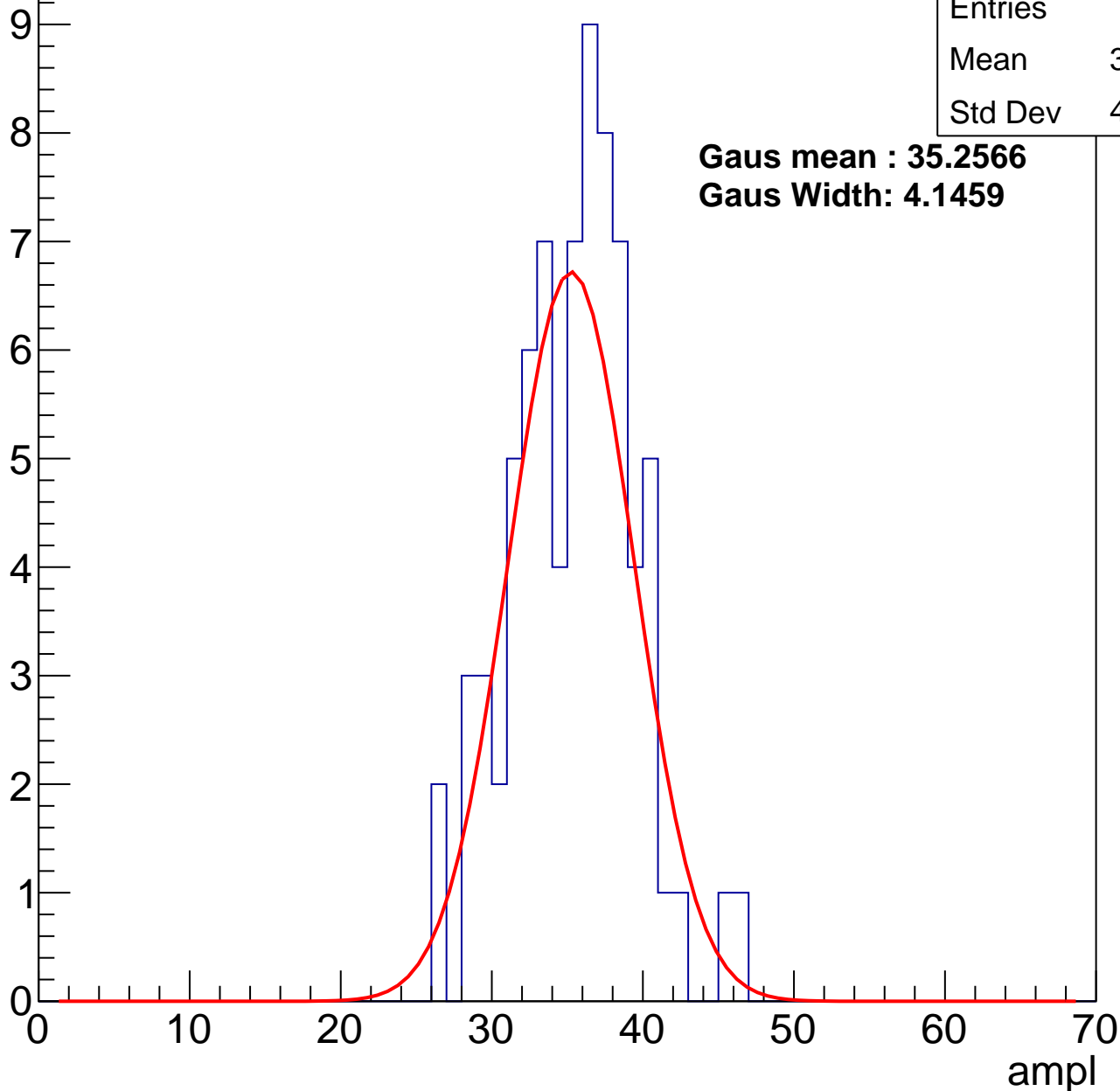
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	34.97
Std Dev	4.026

**Gaus mean : 35.2566**

**Gaus Width: 4.1459**



# B1L102S, U16-ch37, adc2

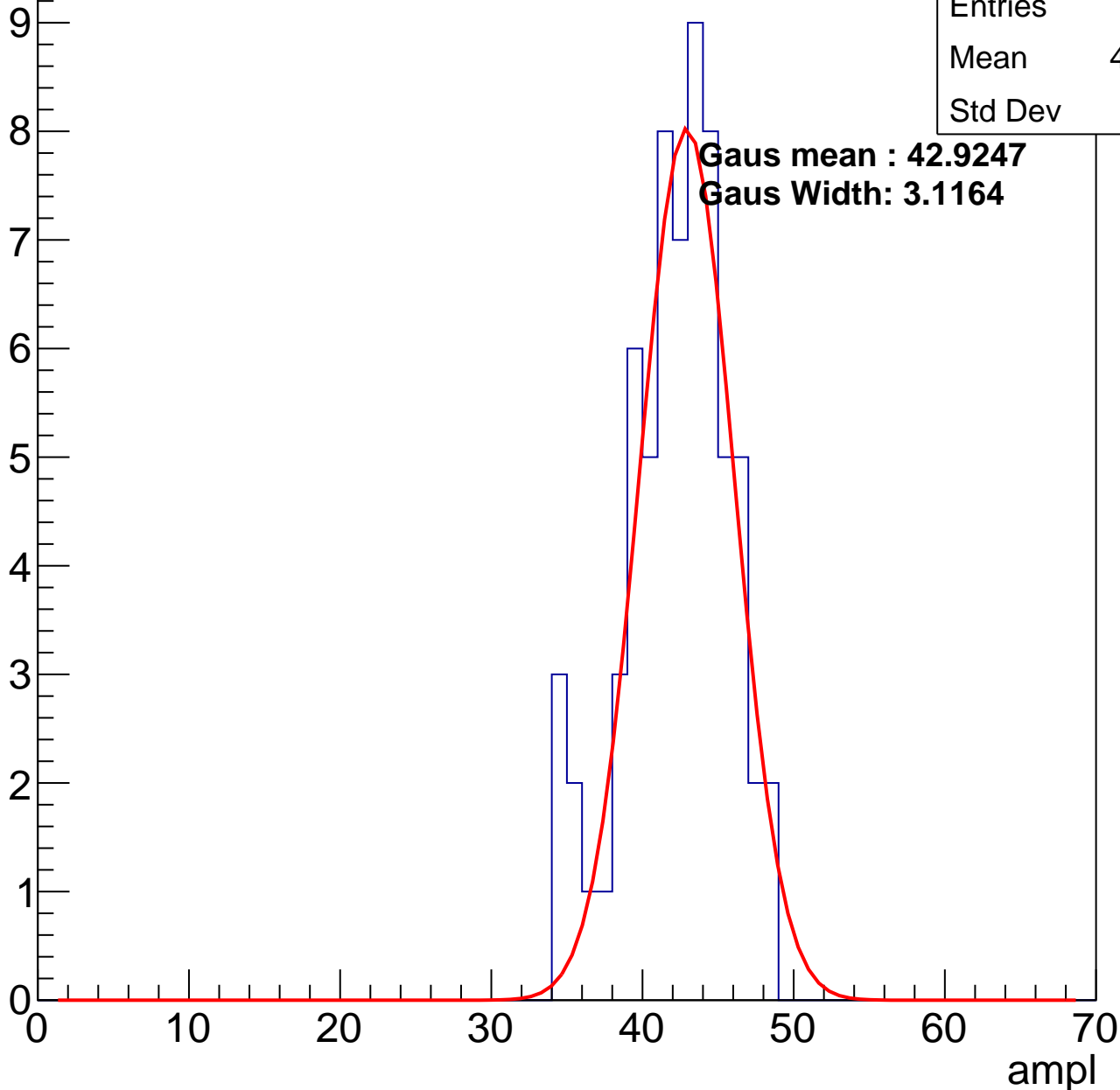
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	41.78
Std Dev	3.38

**Gaus mean : 42.9247**

**Gaus Width: 3.1164**

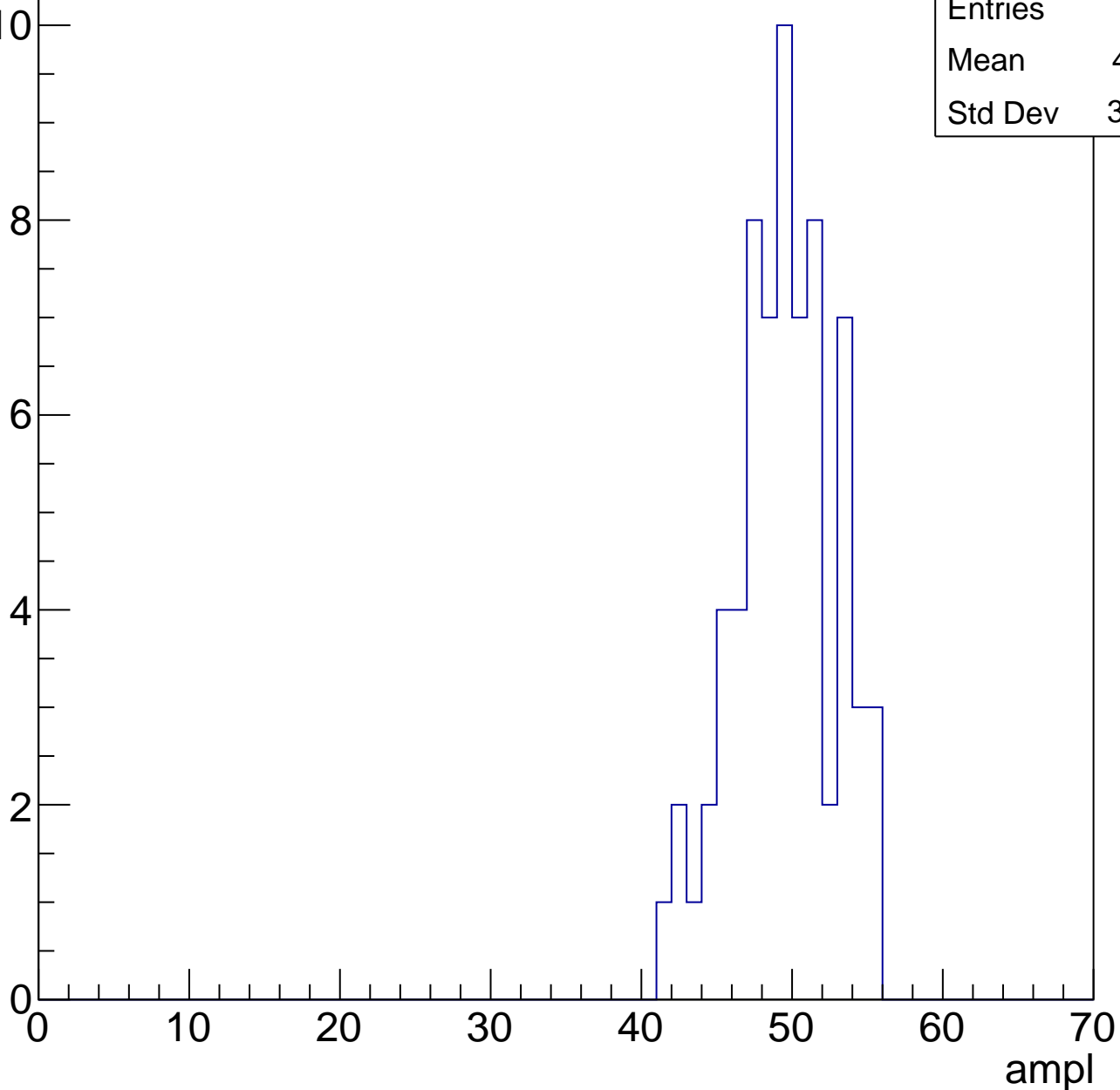


# B1L102S, U16-ch37, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	49.01
Std Dev	3.273

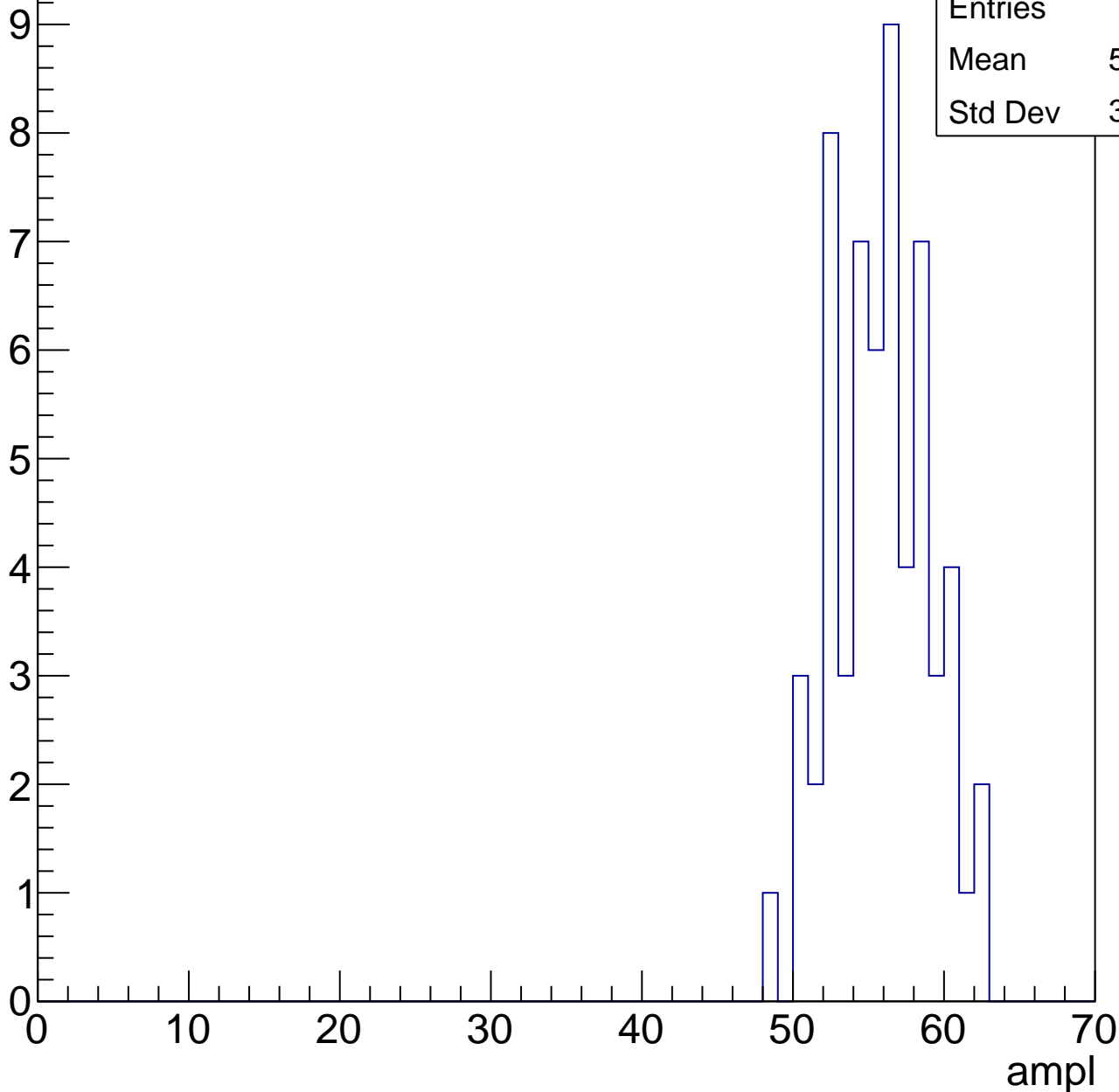


# B1L102S, U16-ch37, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	55.38
Std Dev	3.184

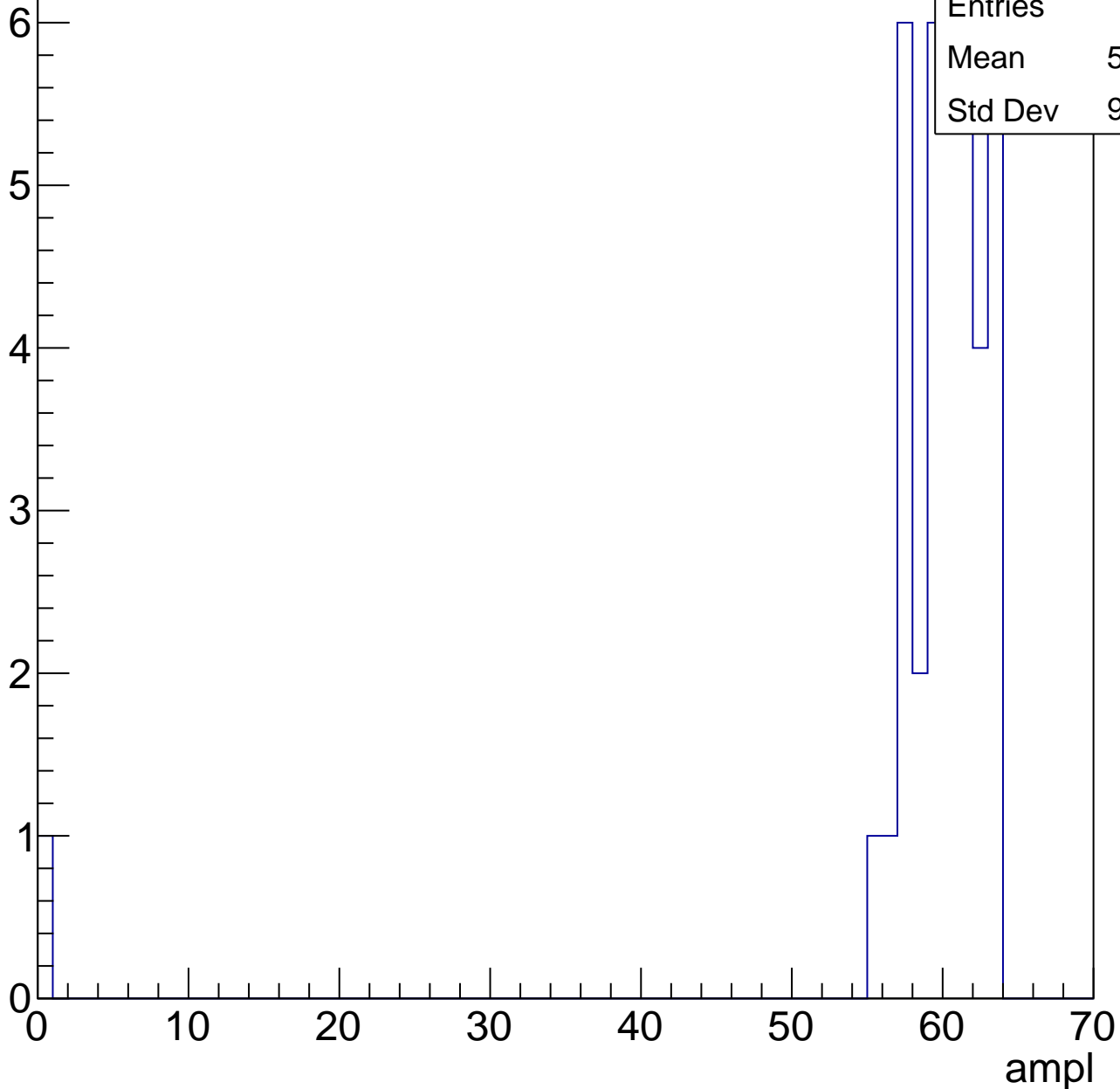


# B1L102S, U16-ch37, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

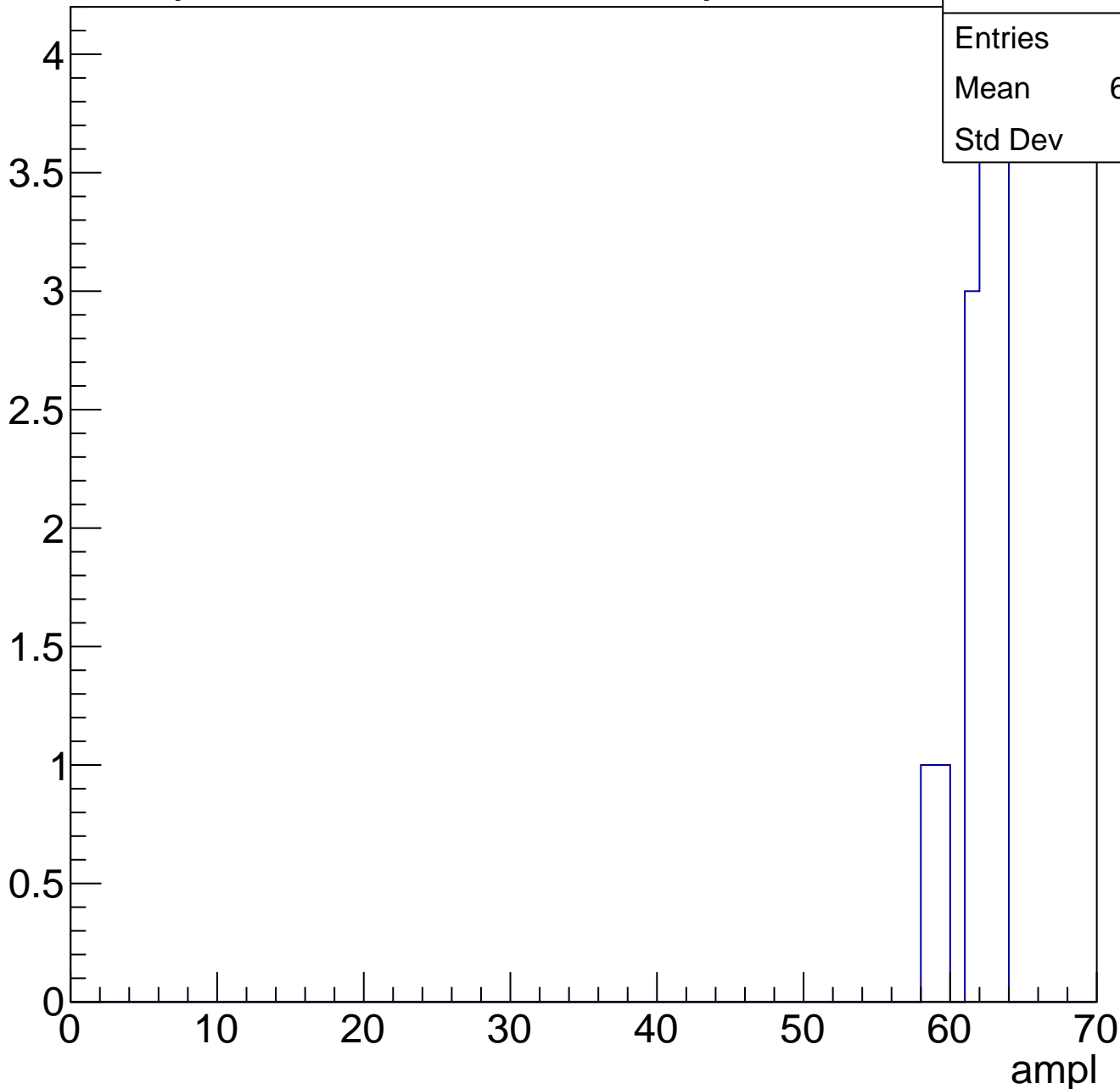
Entries	39
Mean	58.33
Std Dev	9.709



# B1L102S, U16-ch37, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch37, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1

0.8

0.6

0.4

0.2

0

0

10

20

30

40

50

60

70

ampl

Entries

0

Mean

0

Std Dev

0

# B1L102S, U16-ch38, adc0

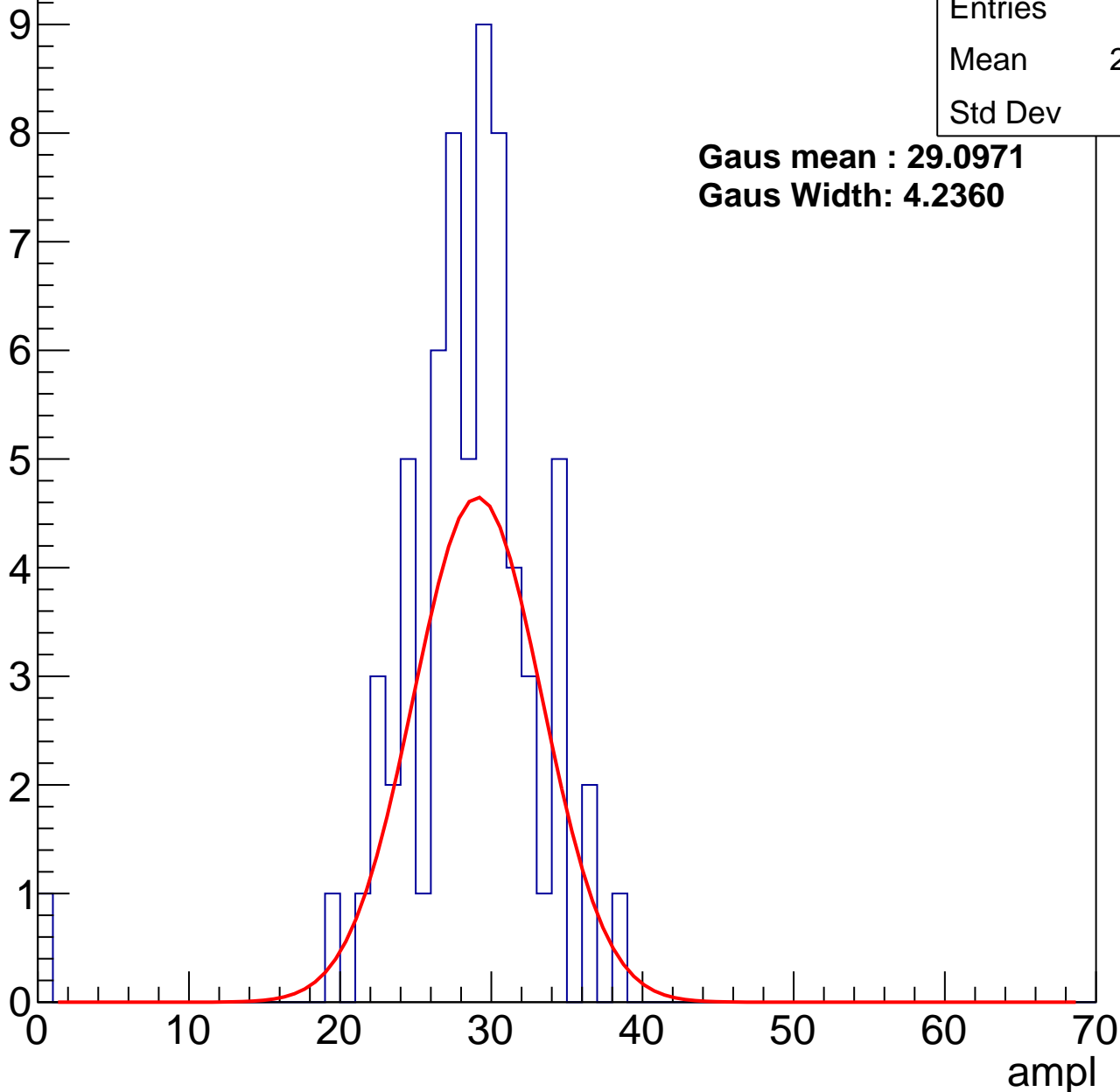
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	27.92
Std Dev	5.15

**Gaus mean : 29.0971**

**Gaus Width: 4.2360**



# B1L102S, U16-ch38, adc1

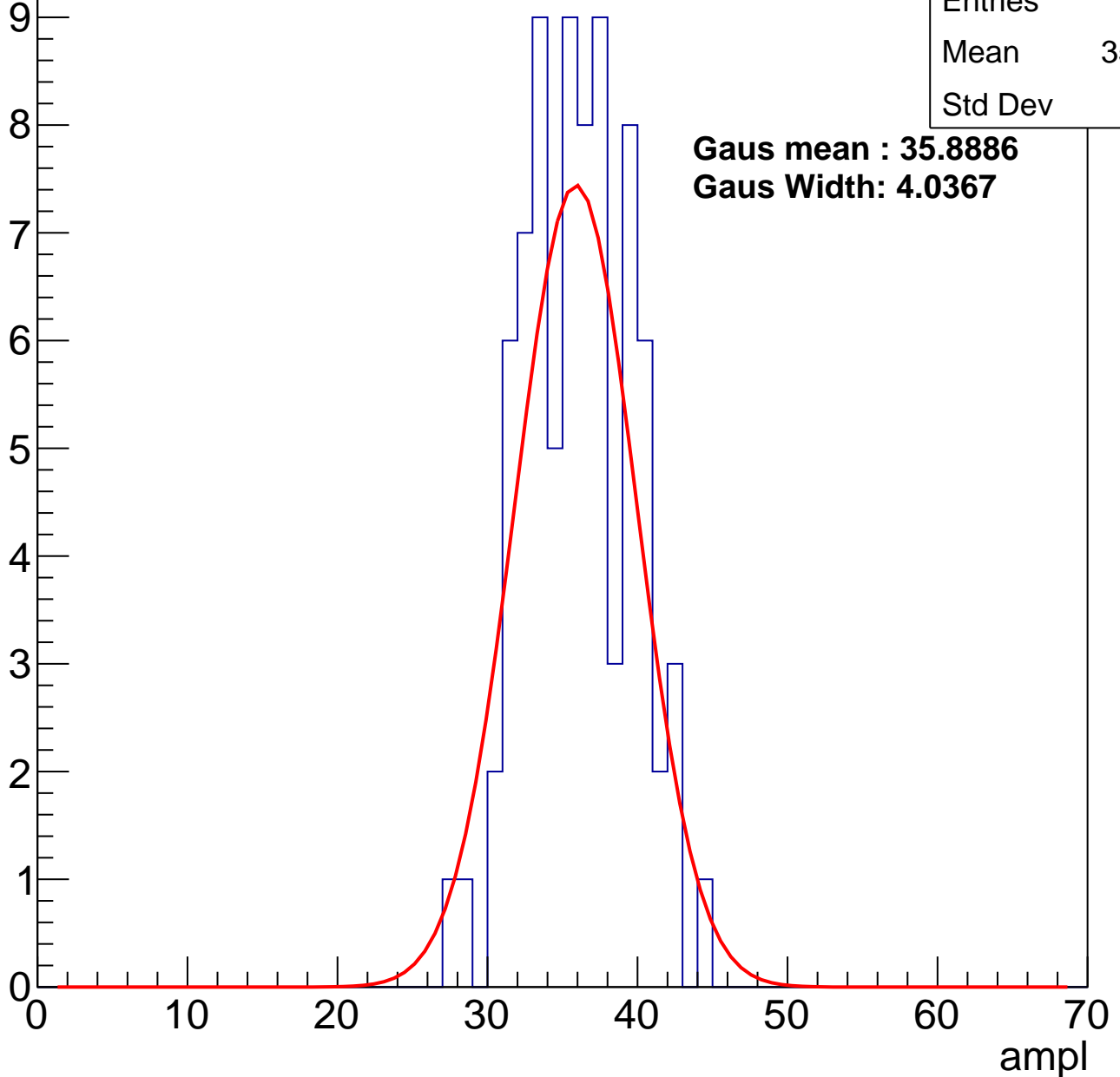
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	35.58
Std Dev	3.51

**Gaus mean : 35.8886**

**Gaus Width: 4.0367**



# B1L102S, U16-ch38, adc2

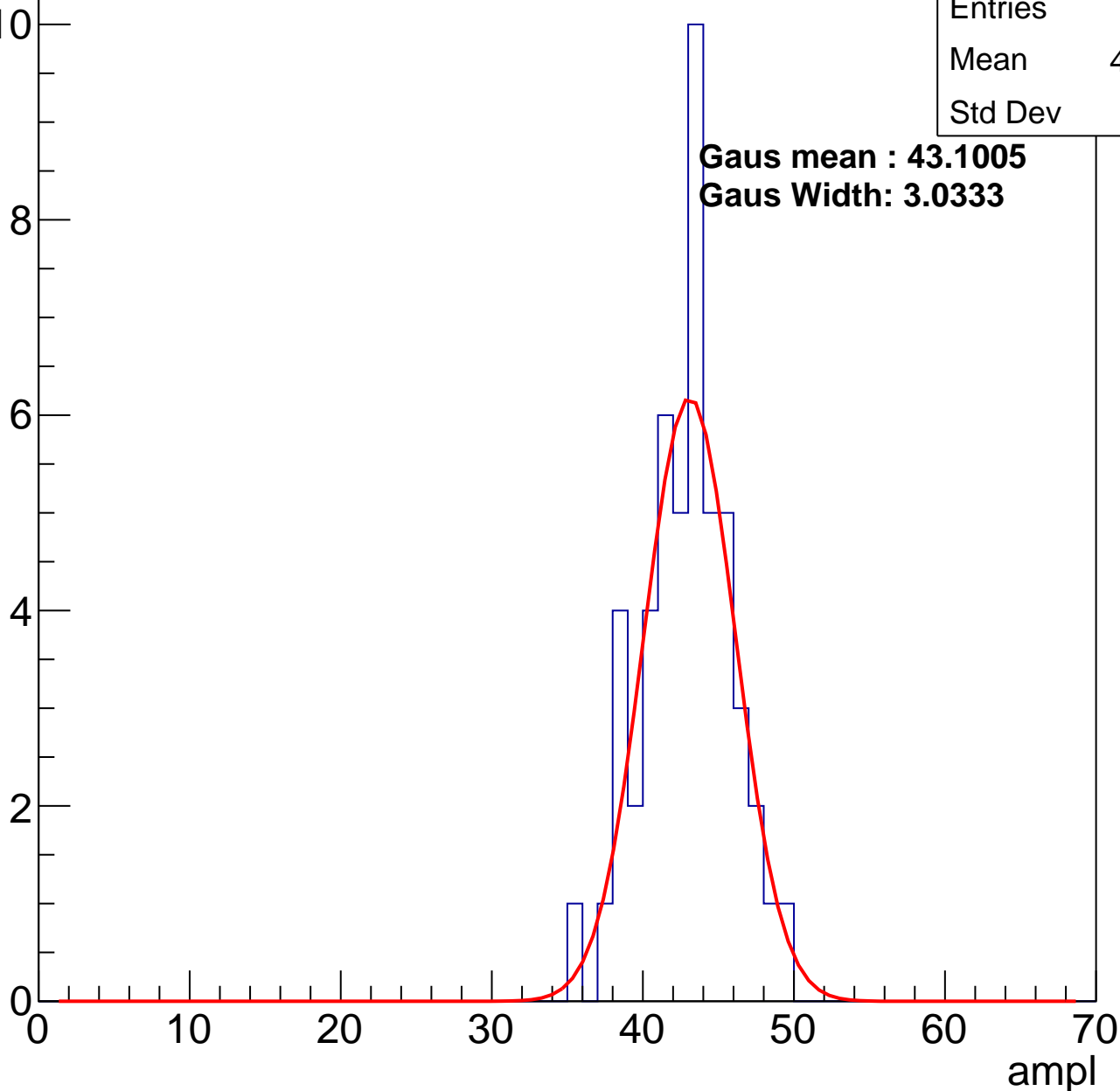
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	42.44
Std Dev	2.92

**Gaus mean : 43.1005**

**Gaus Width: 3.0333**

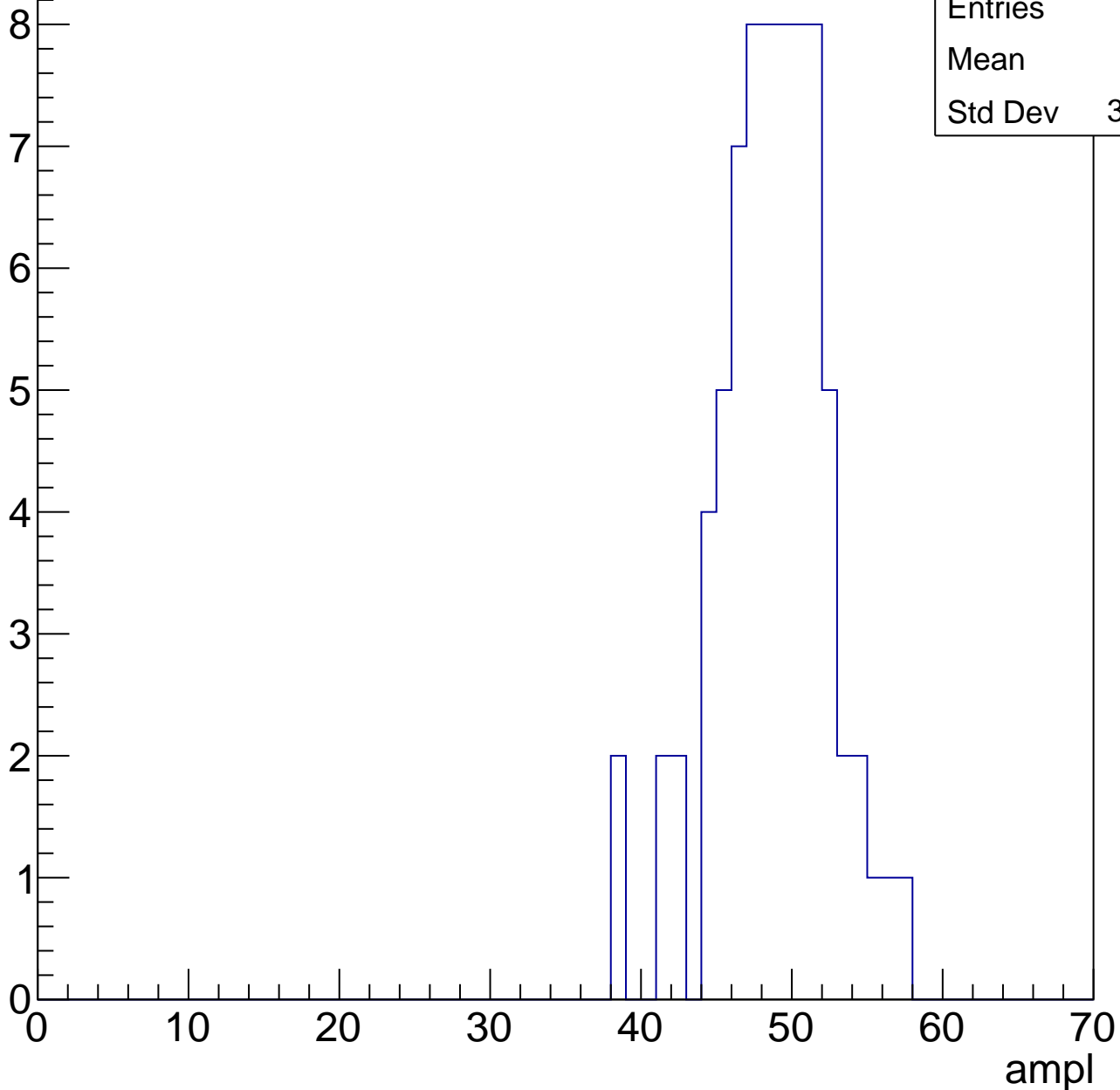


# B1L102S, U16-ch38, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	48.2
Std Dev	3.713

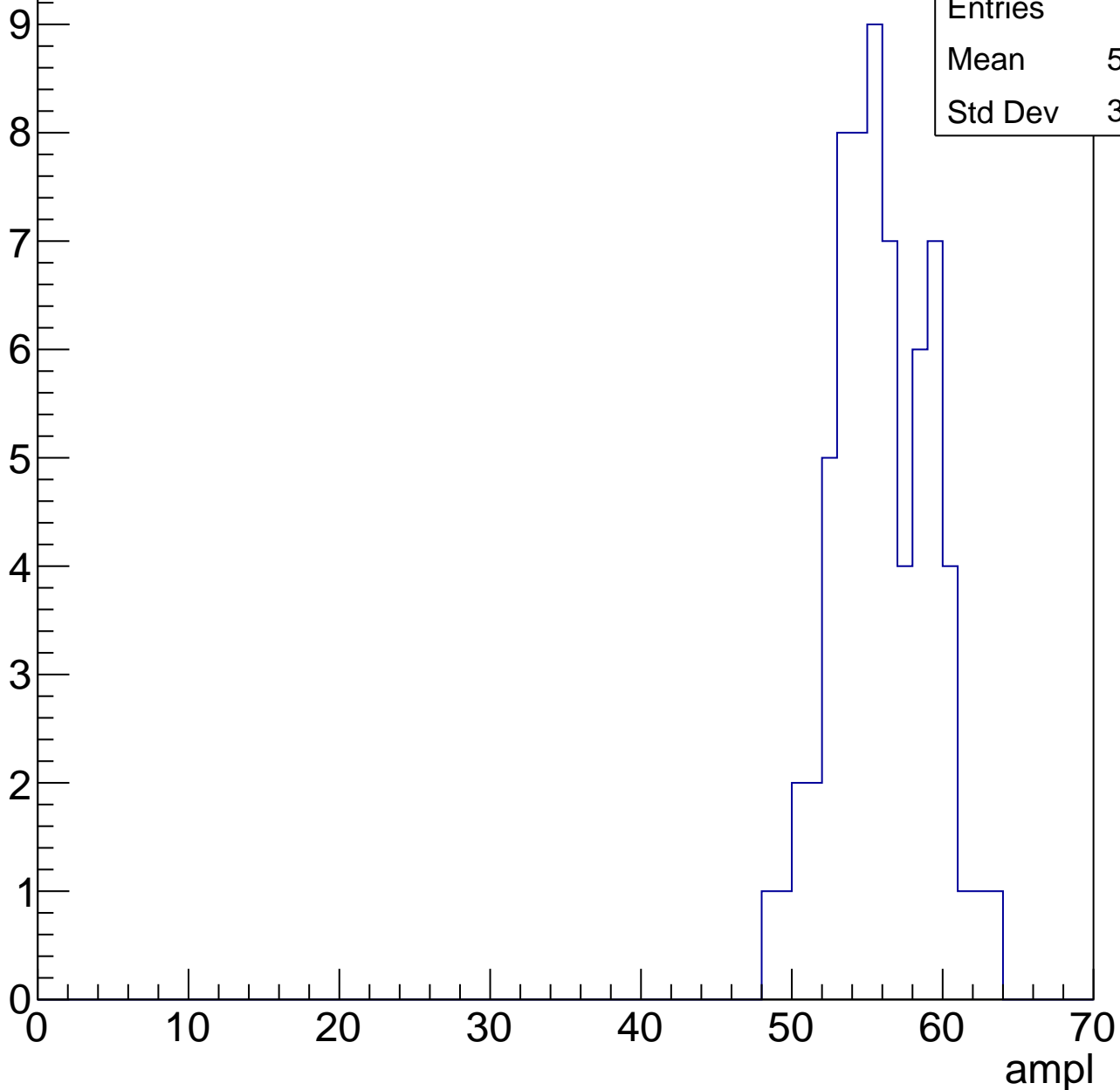


# B1L102S, U16-ch38, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	55.48
Std Dev	3.173

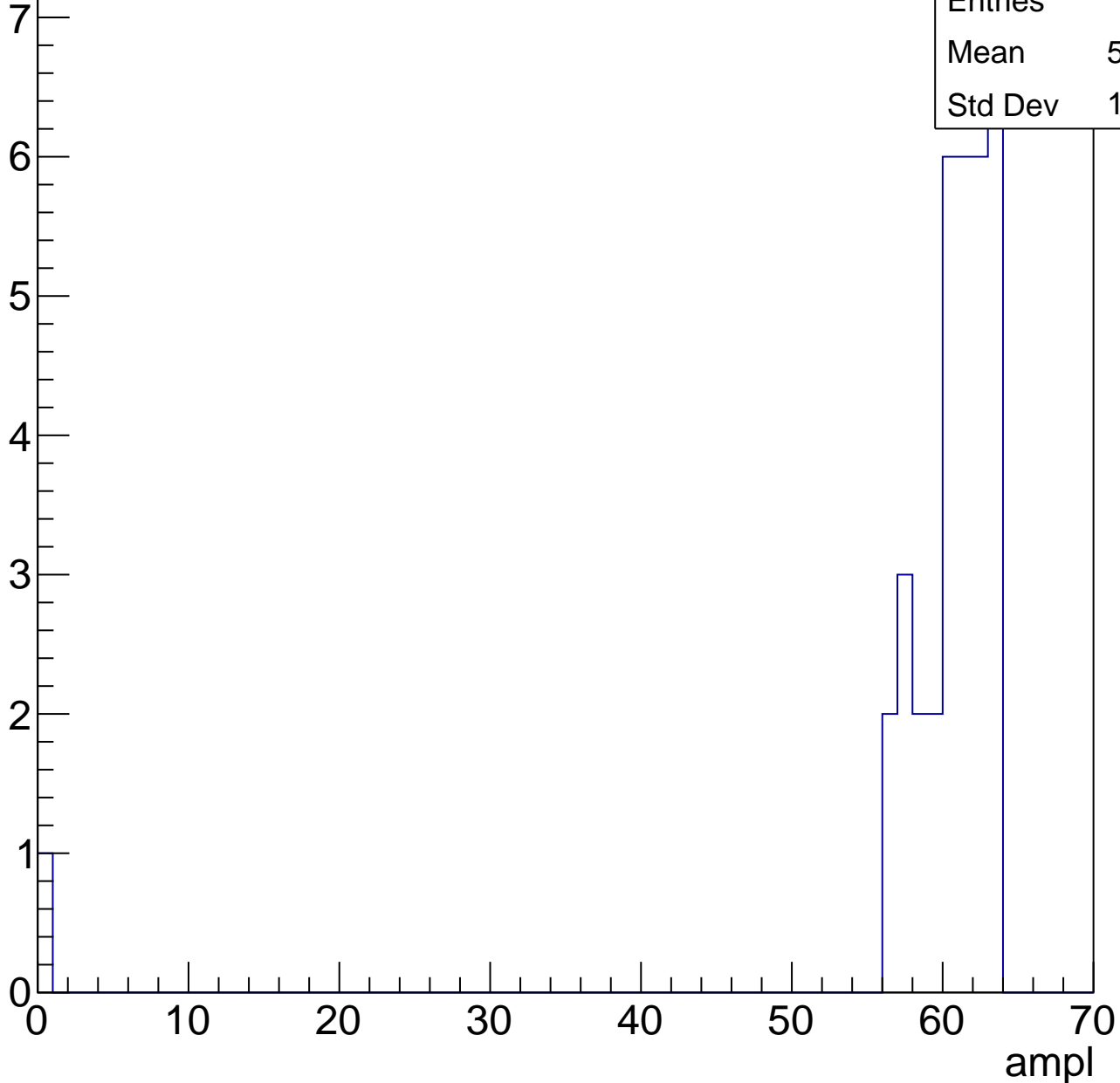


# B1L102S, U16-ch38, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

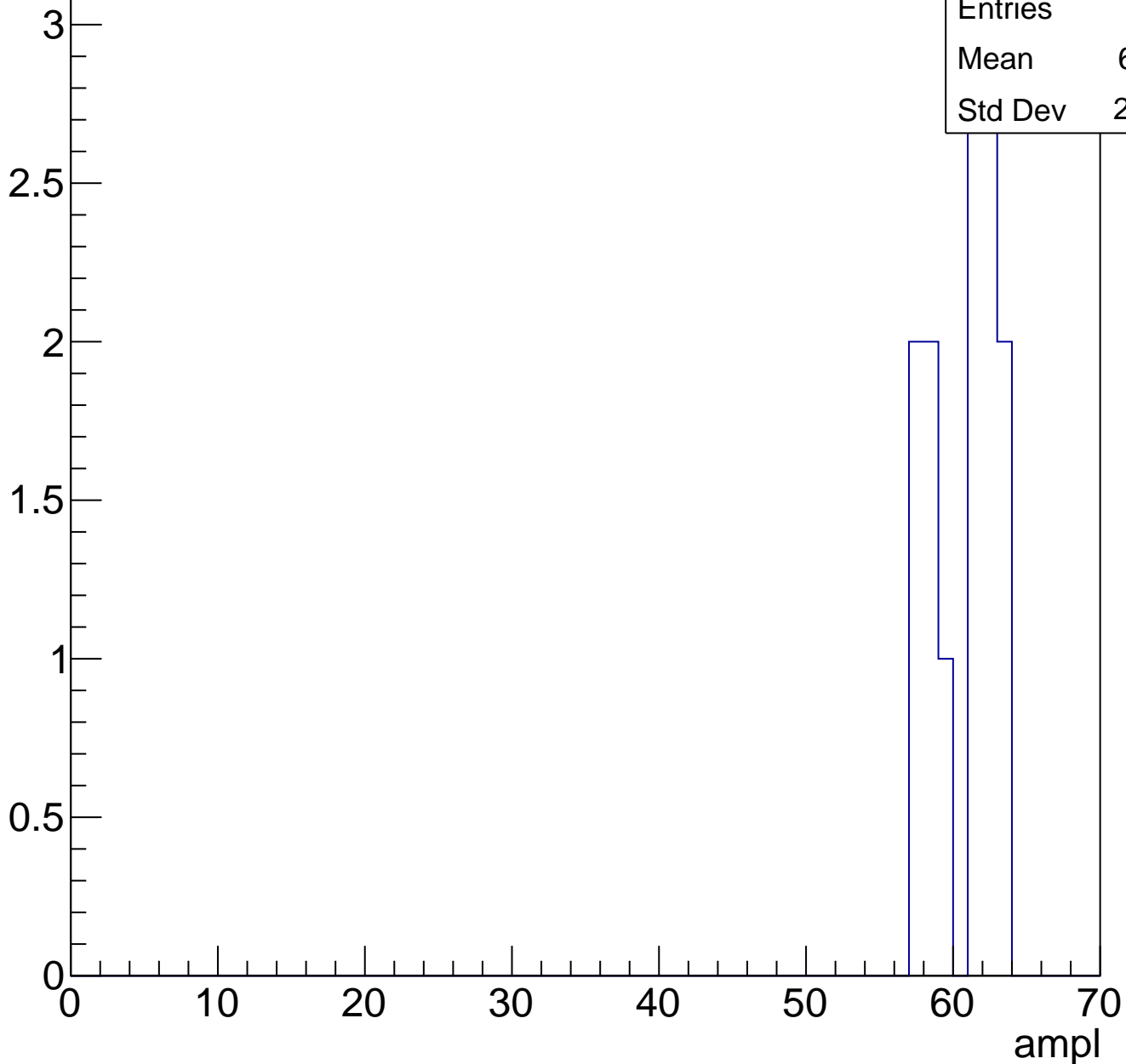
Entries	35
Mean	58.74
Std Dev	10.29



# B1L102S, U16-ch38, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

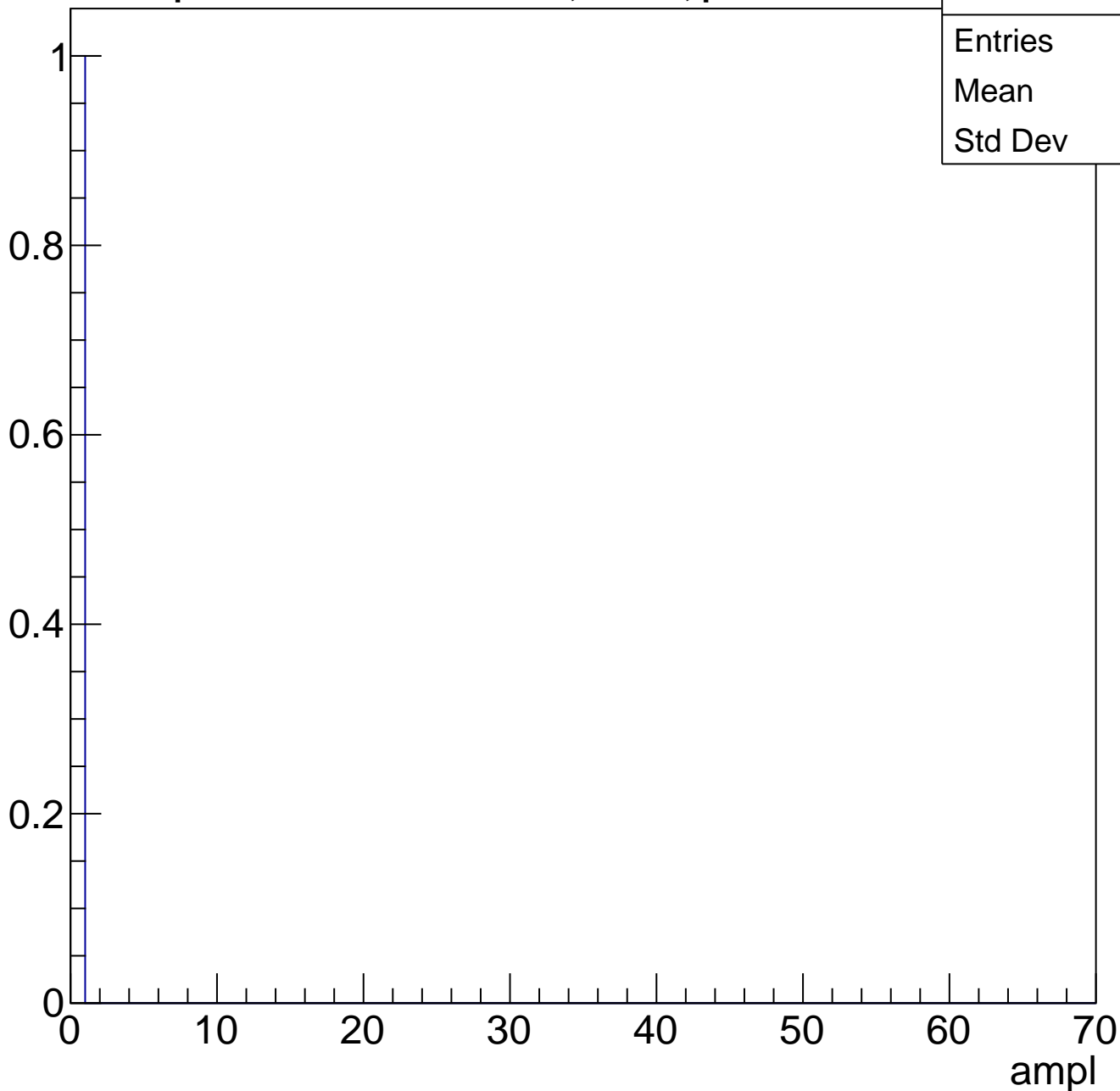




# B1L102S, U16-ch38, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U16-ch39, adc0

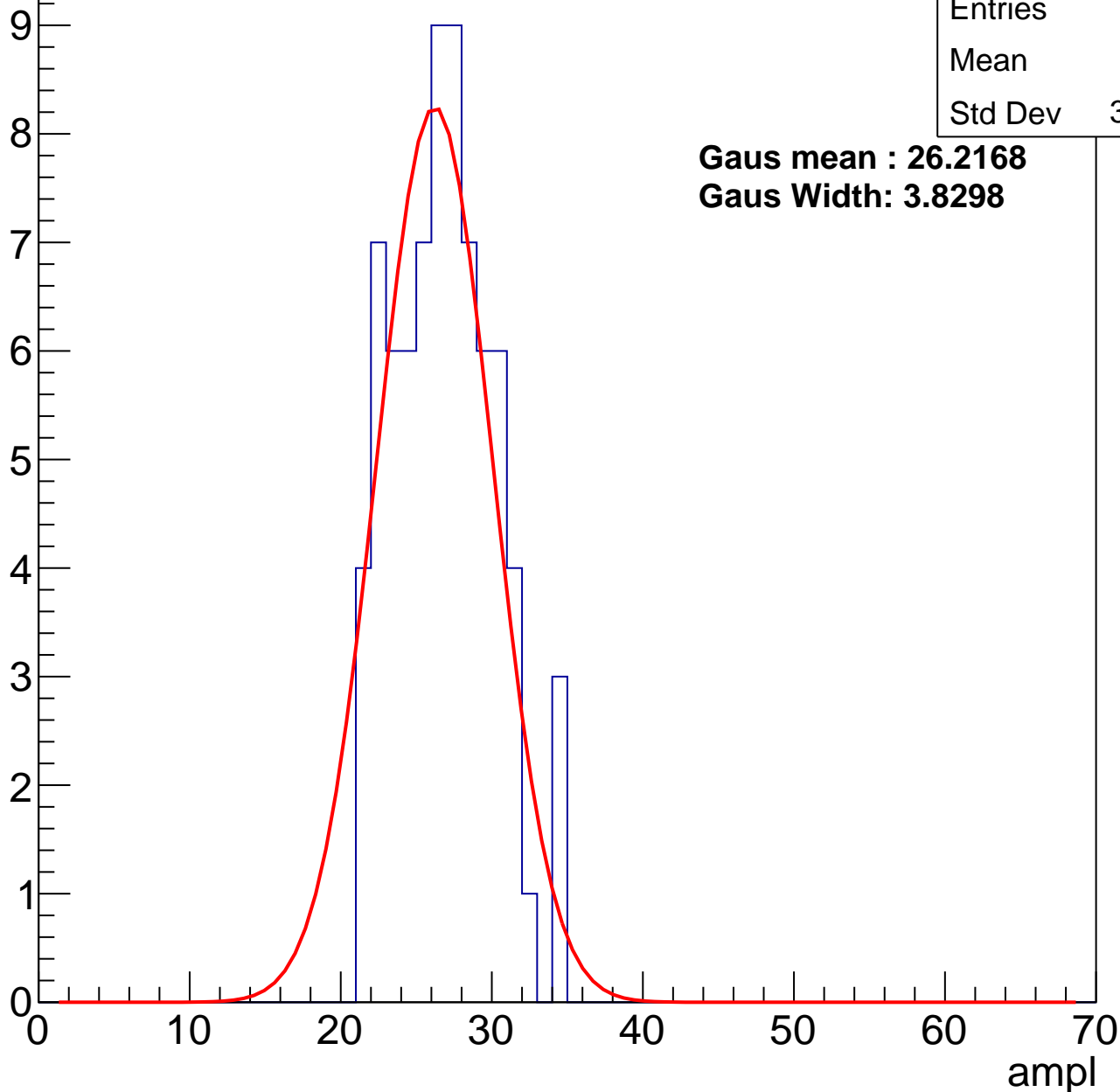
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	26.4
Std Dev	3.266

**Gaus mean : 26.2168**

**Gaus Width: 3.8298**



# B1L102S, U16-ch39, adc1

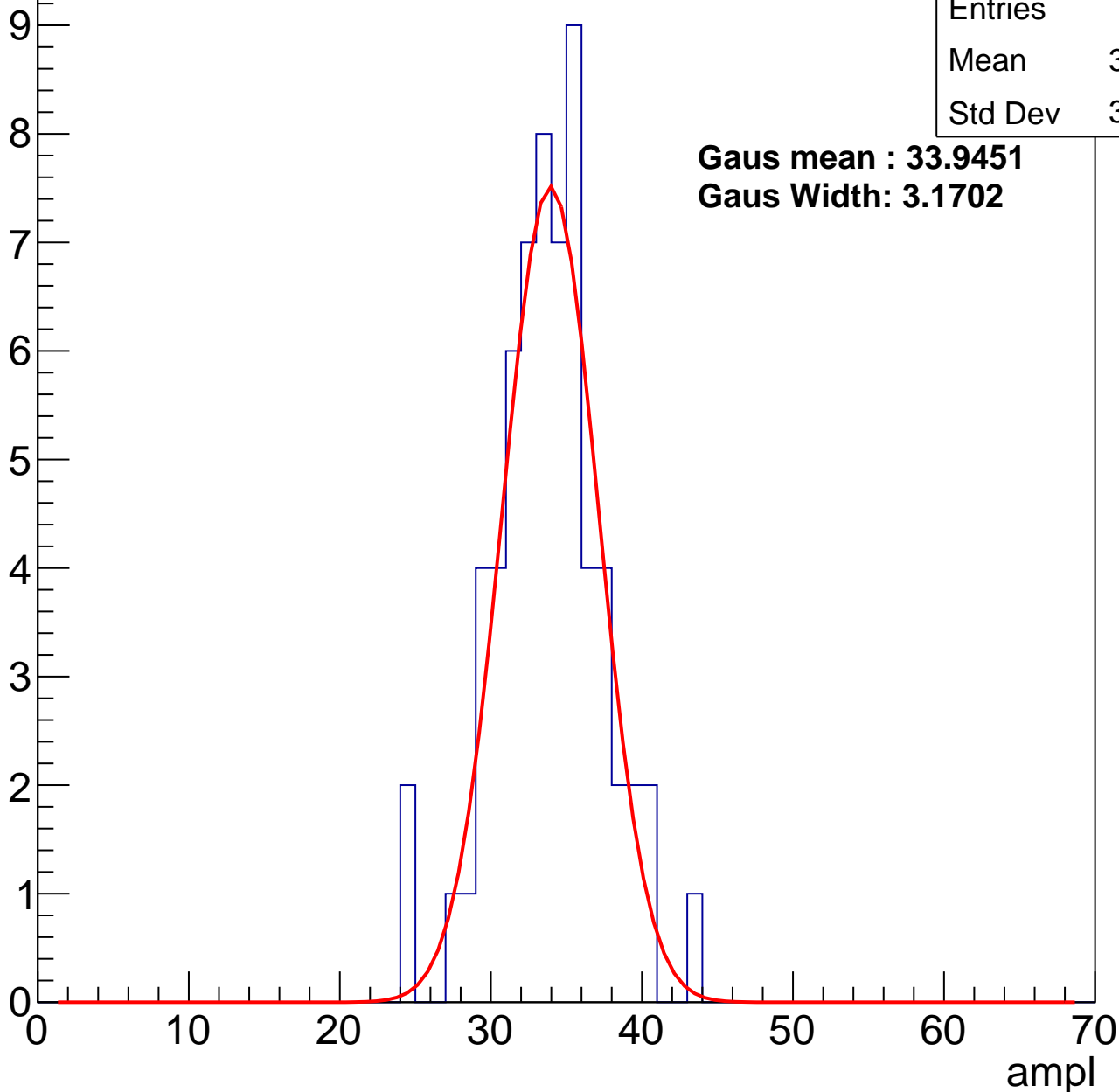
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	33.36
Std Dev	3.555

**Gaus mean : 33.9451**

**Gaus Width: 3.1702**



# B1L102S, U16-ch39, adc2

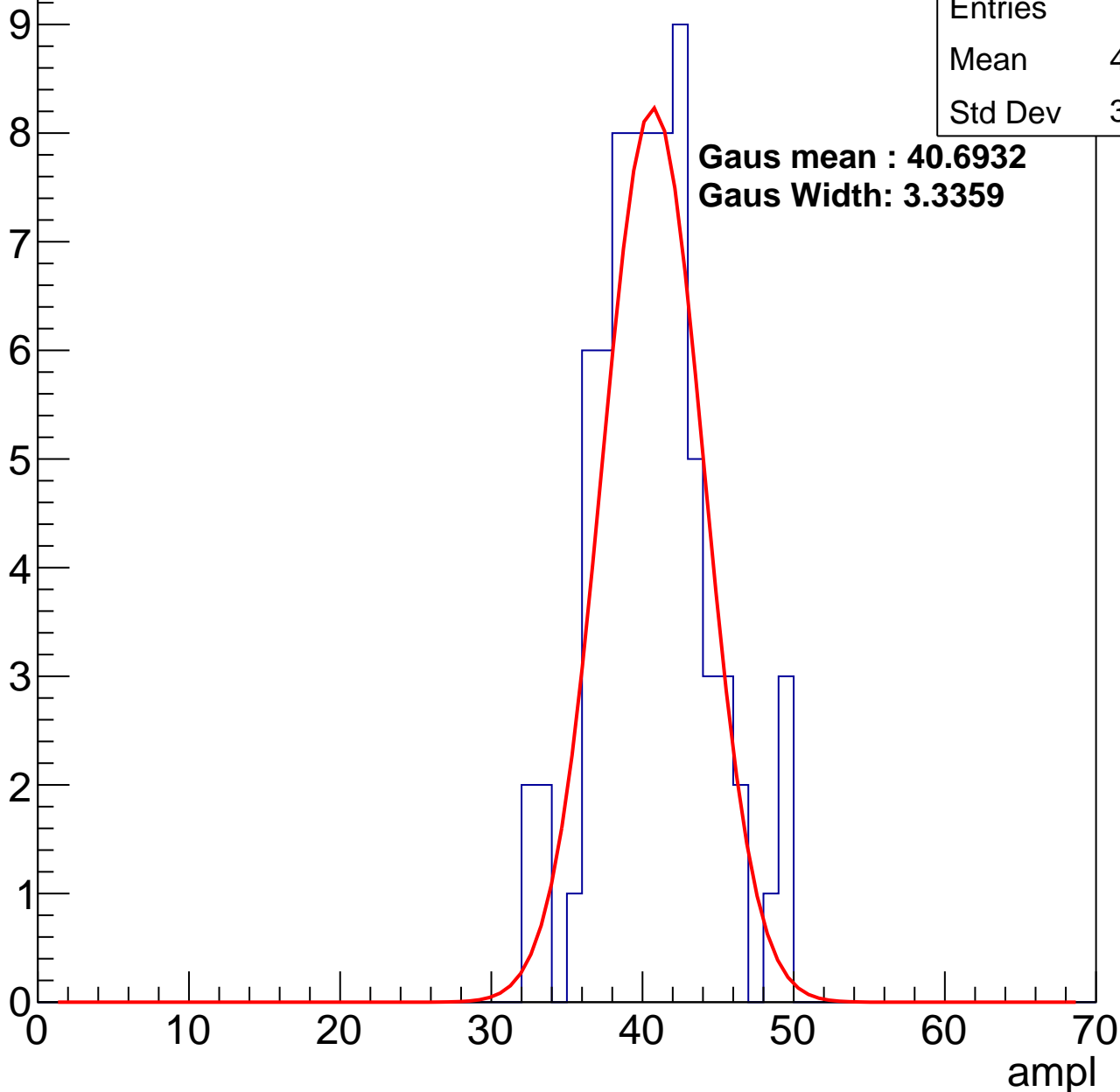
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	40.19
Std Dev	3.705

**Gaus mean : 40.6932**

**Gaus Width: 3.3359**

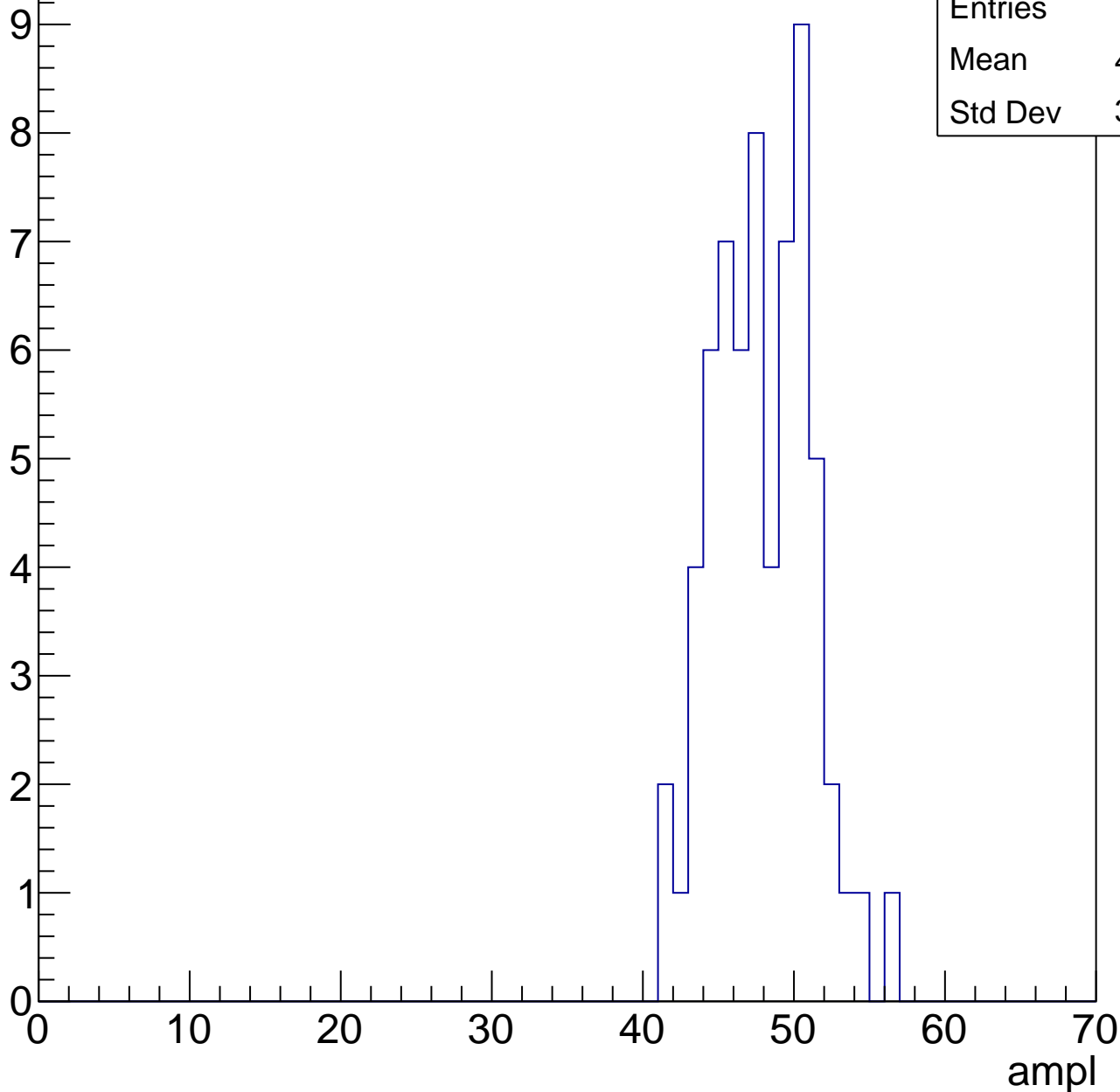


# B1L102S, U16-ch39, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	47.41
Std Dev	3.181

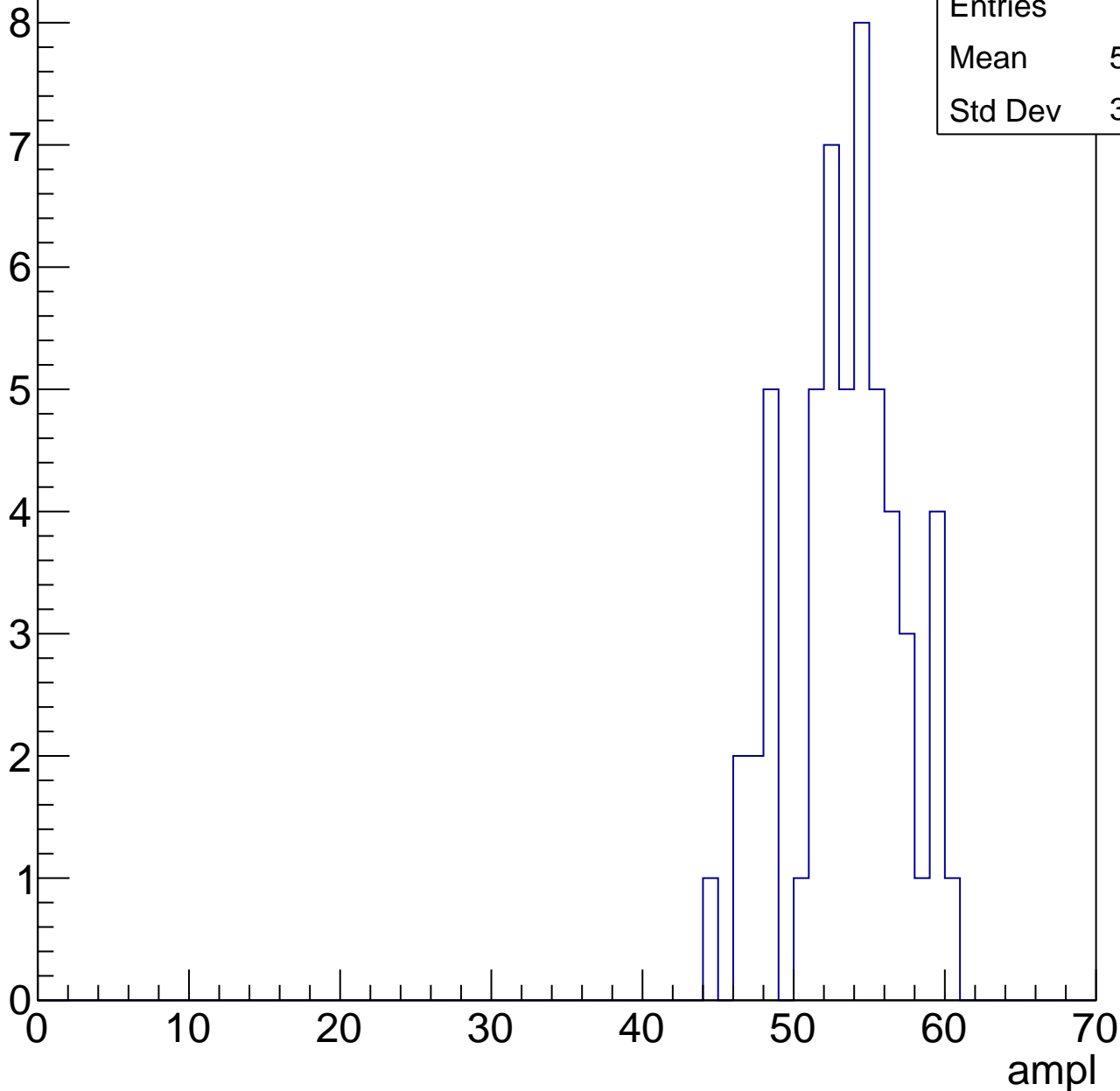


# B1L102S, U16-ch39, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

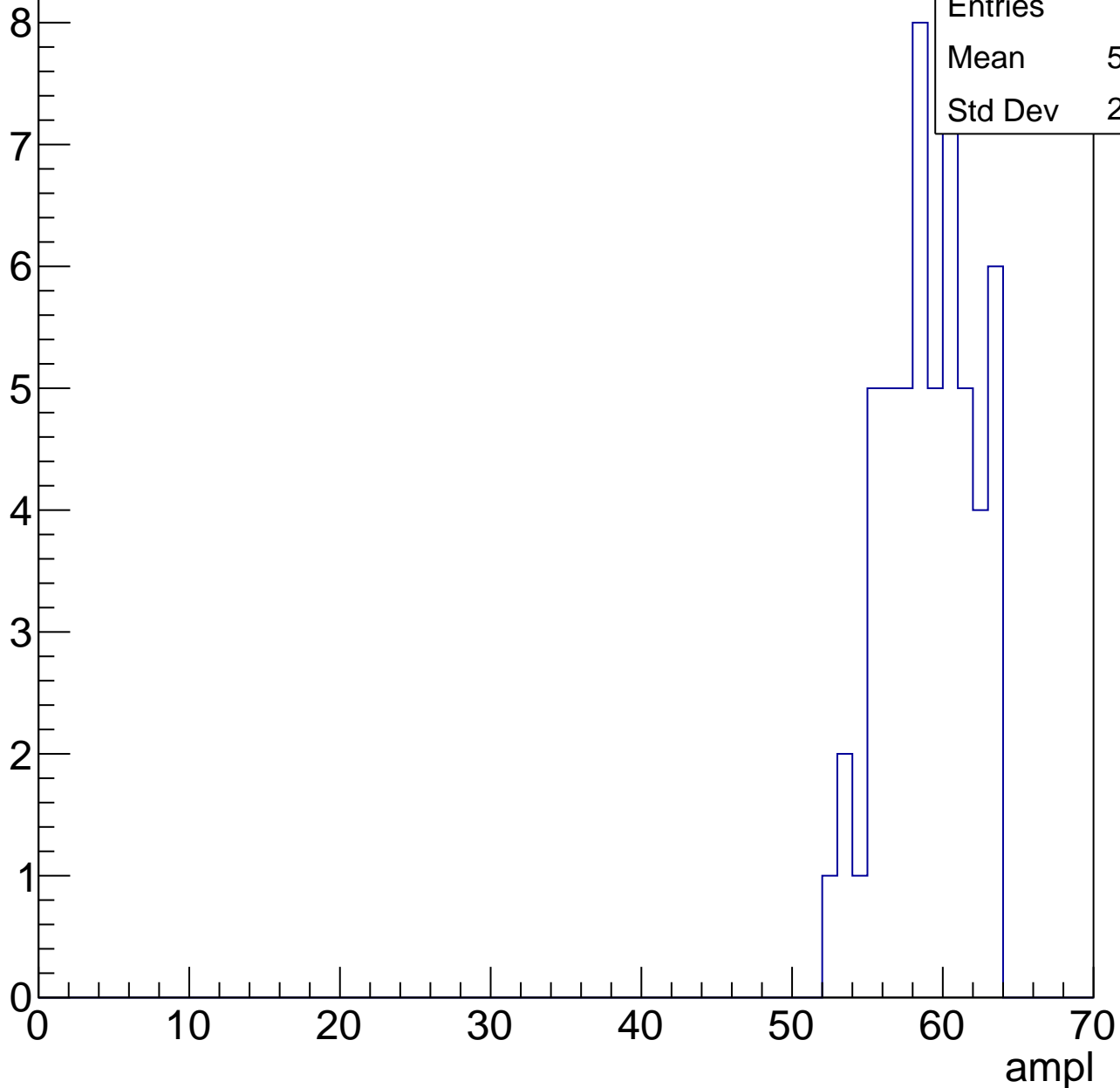
Entries	54
Mean	52.96
Std Dev	3.707



# B1L102S, U16-ch39, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

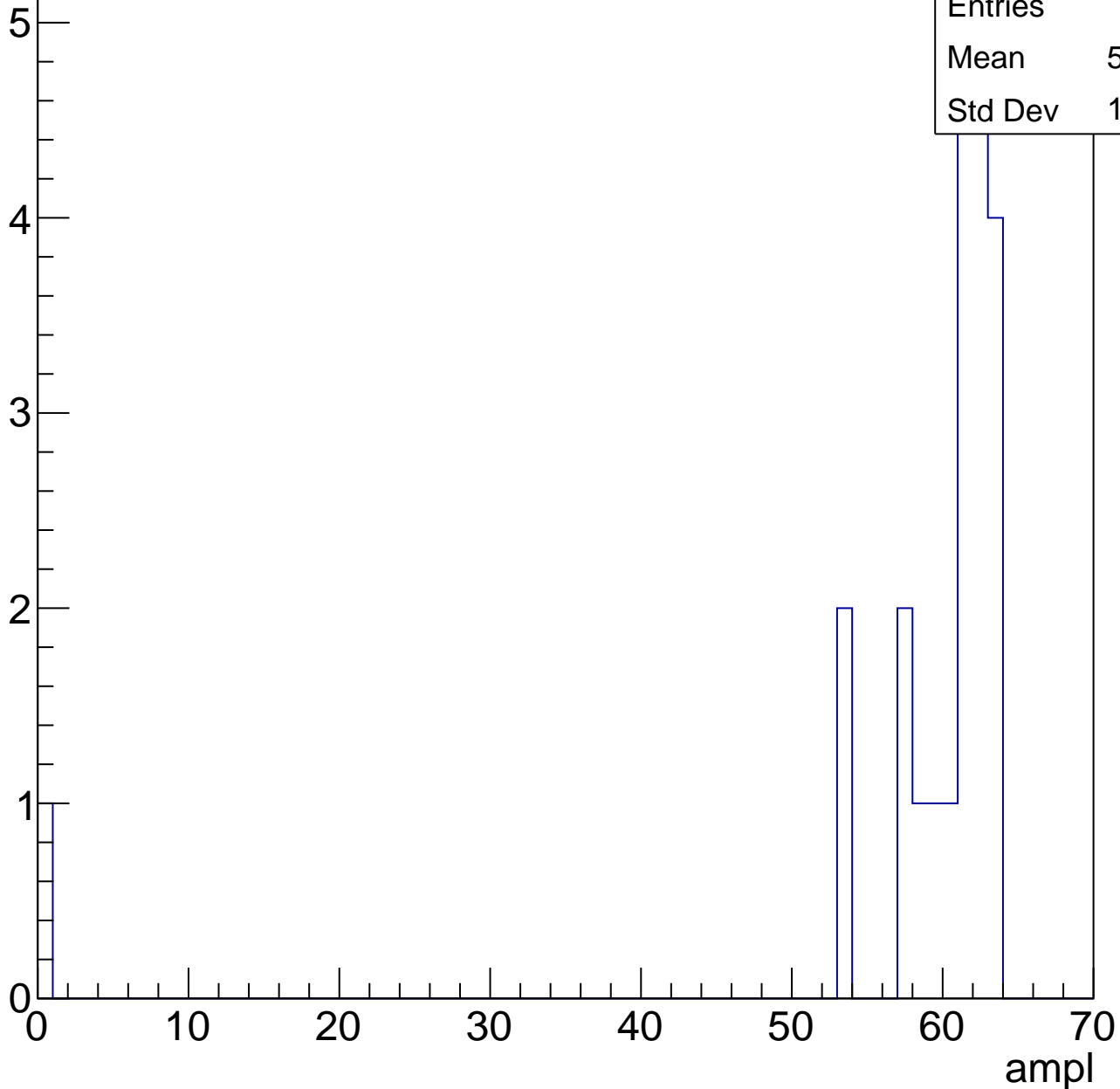


# B1L102S, U16-ch39, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	22
Mean	57.45
Std Dev	12.86

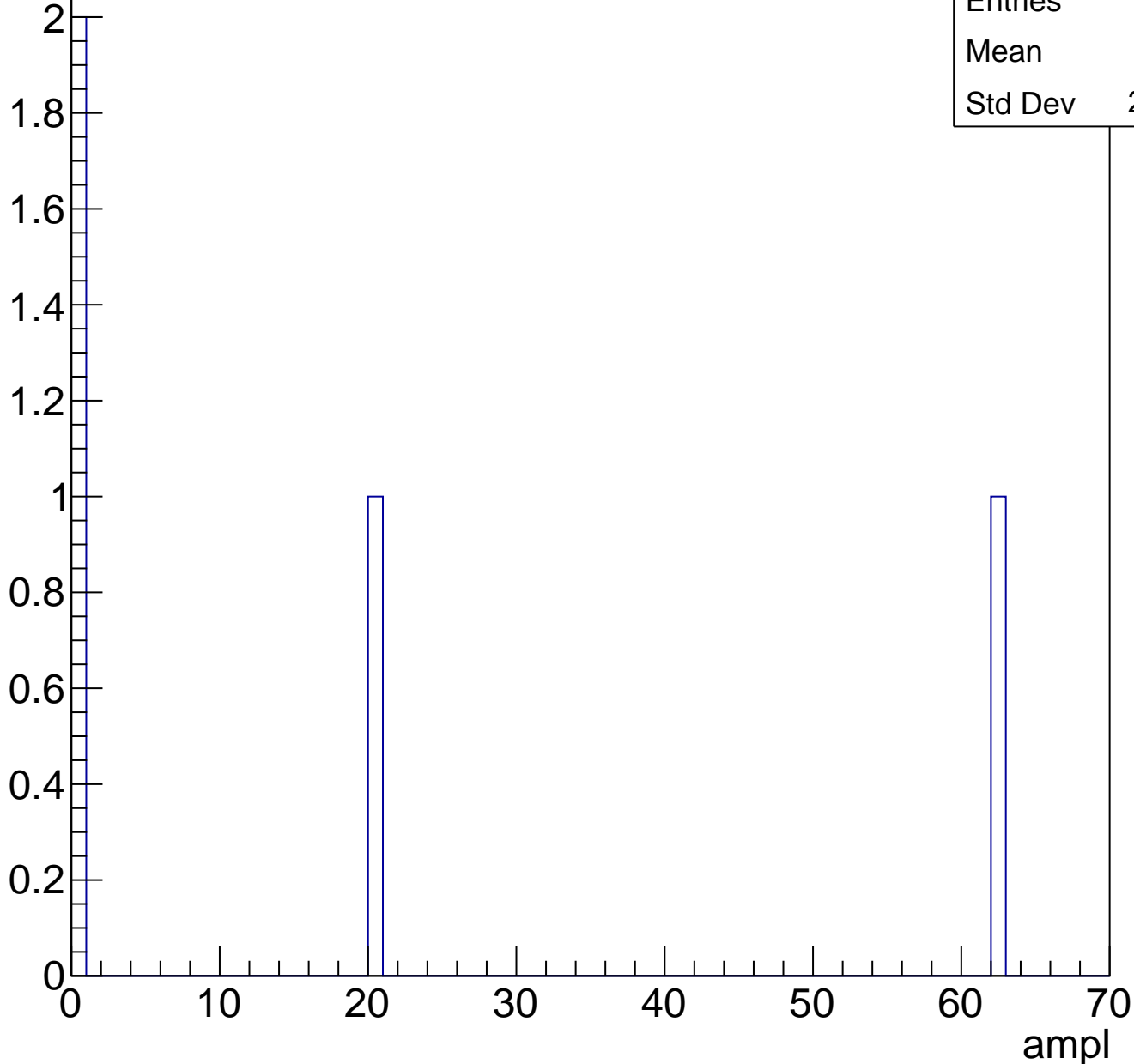




# B1L102S, U16-ch39, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	4
Mean	20.5
Std Dev	25.31

# B1L102S, U16-ch40, adc0

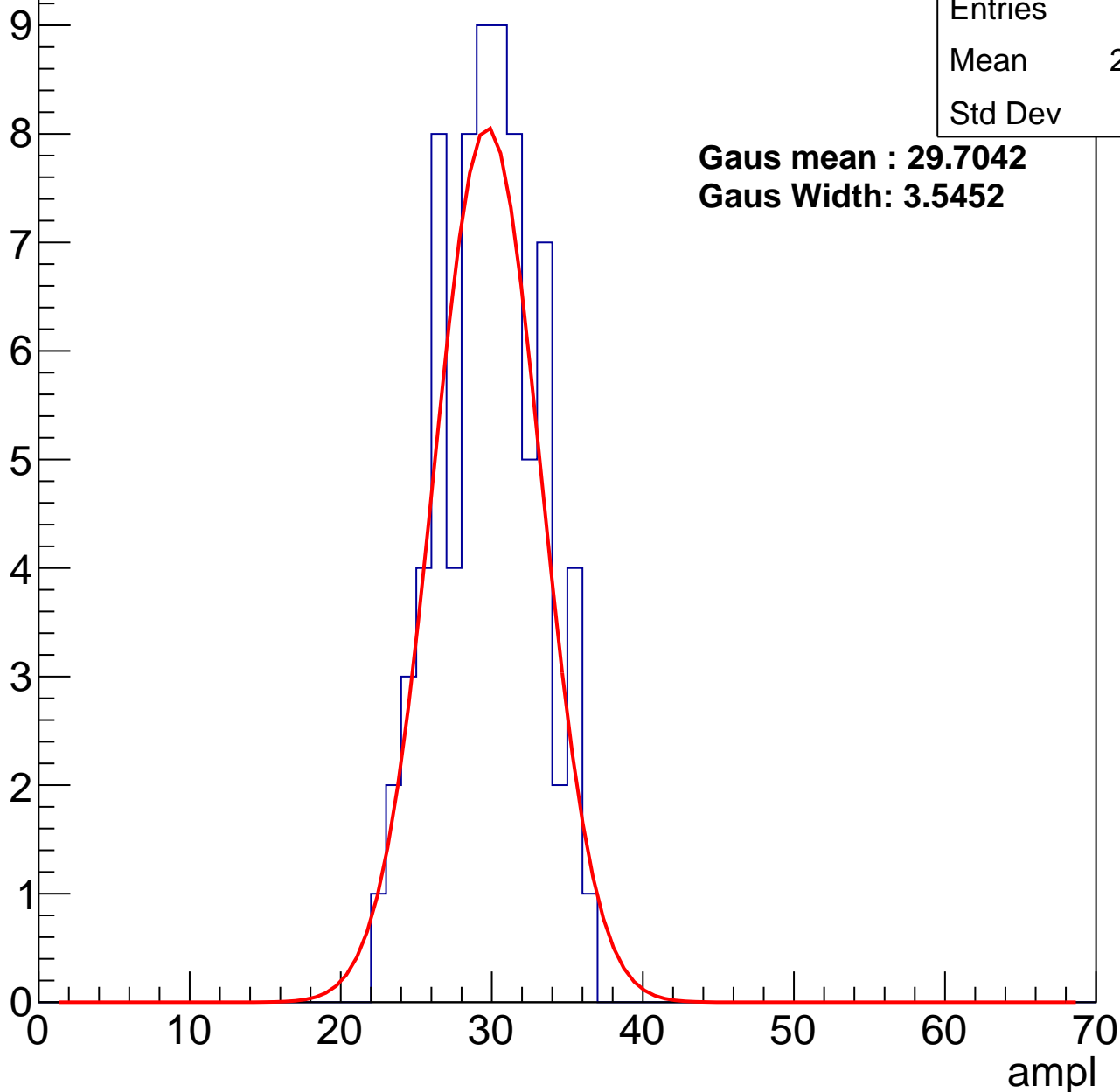
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	29.25
Std Dev	3.25

**Gaus mean : 29.7042**

**Gaus Width: 3.5452**



# B1L102S, U16-ch40, adc1

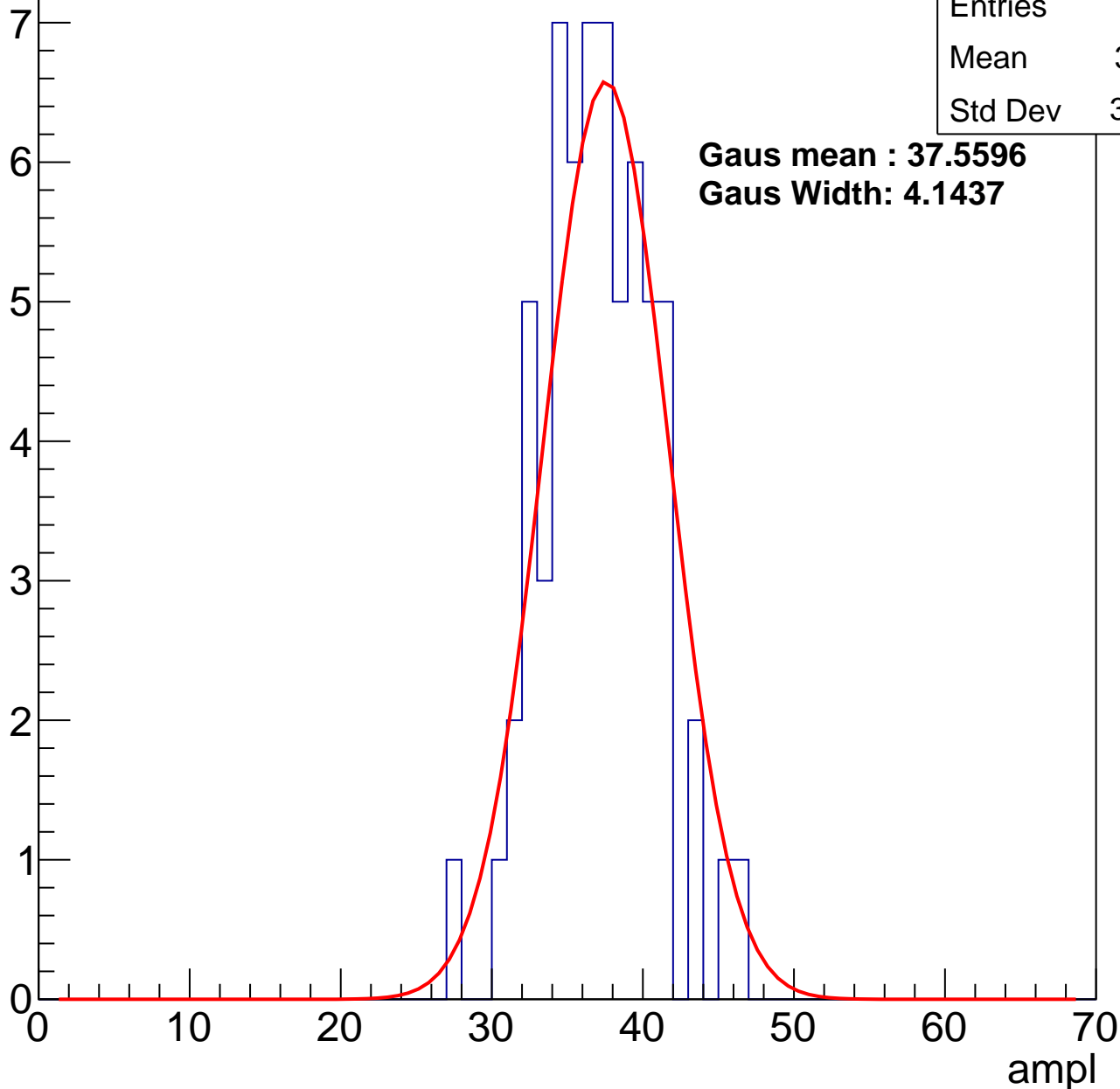
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	36.61
Std Dev	3.643

**Gaus mean : 37.5596**

**Gaus Width: 4.1437**



# B1L102S, U16-ch40, adc2

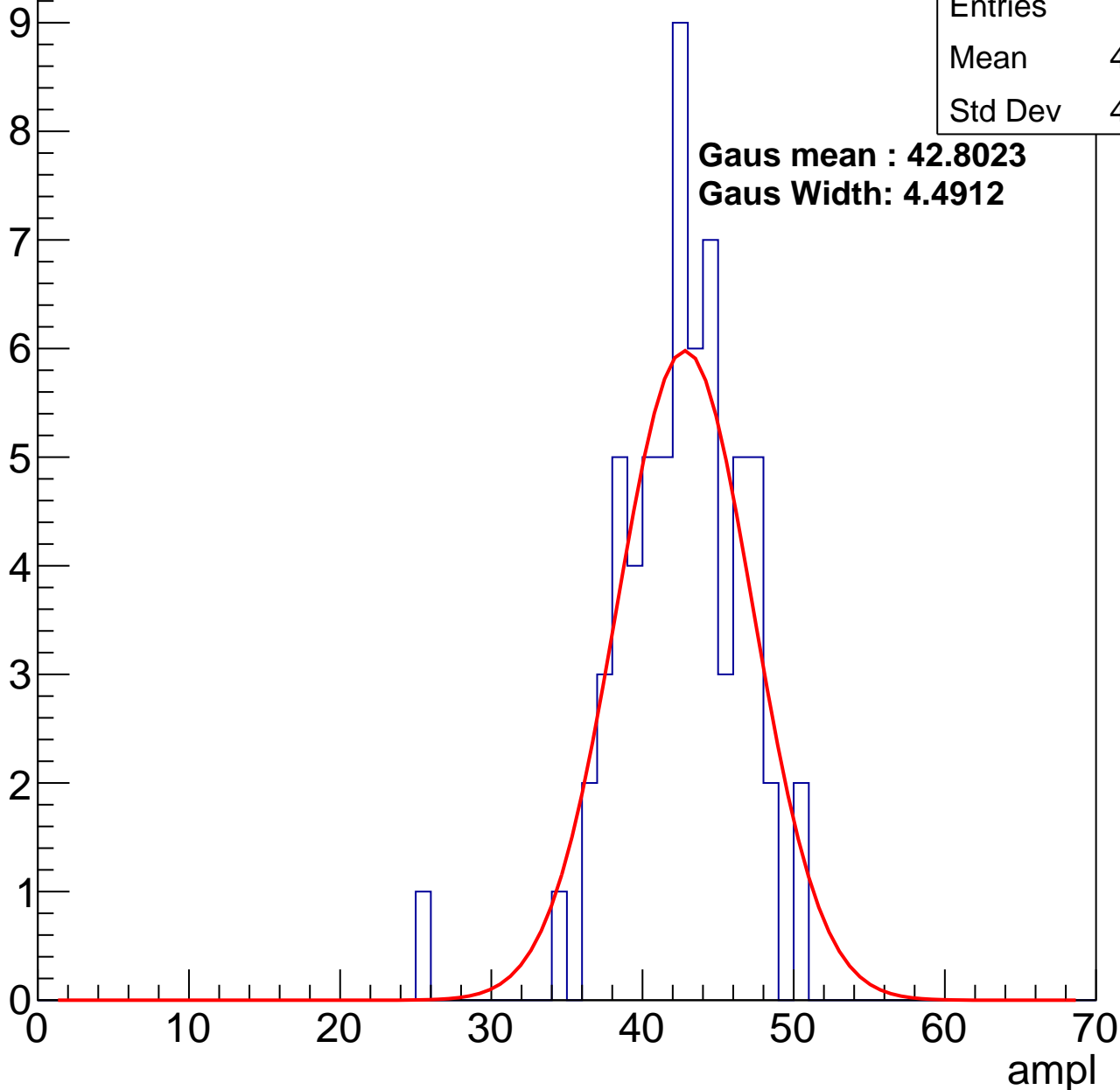
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	42.05
Std Dev	4.127

**Gaus mean : 42.8023**

**Gaus Width: 4.4912**

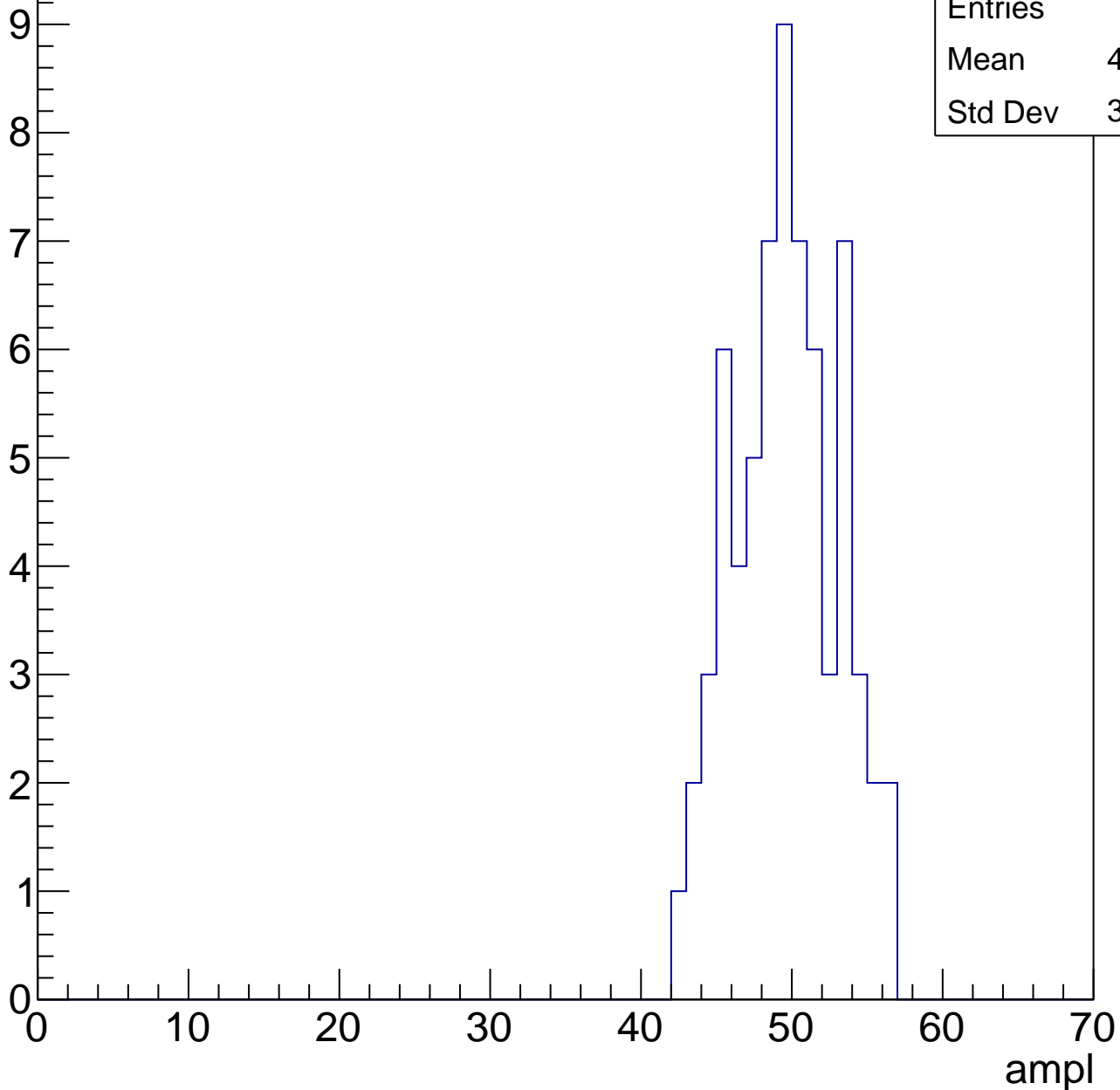


# B1L102S, U16-ch40, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	49.15
Std Dev	3.387

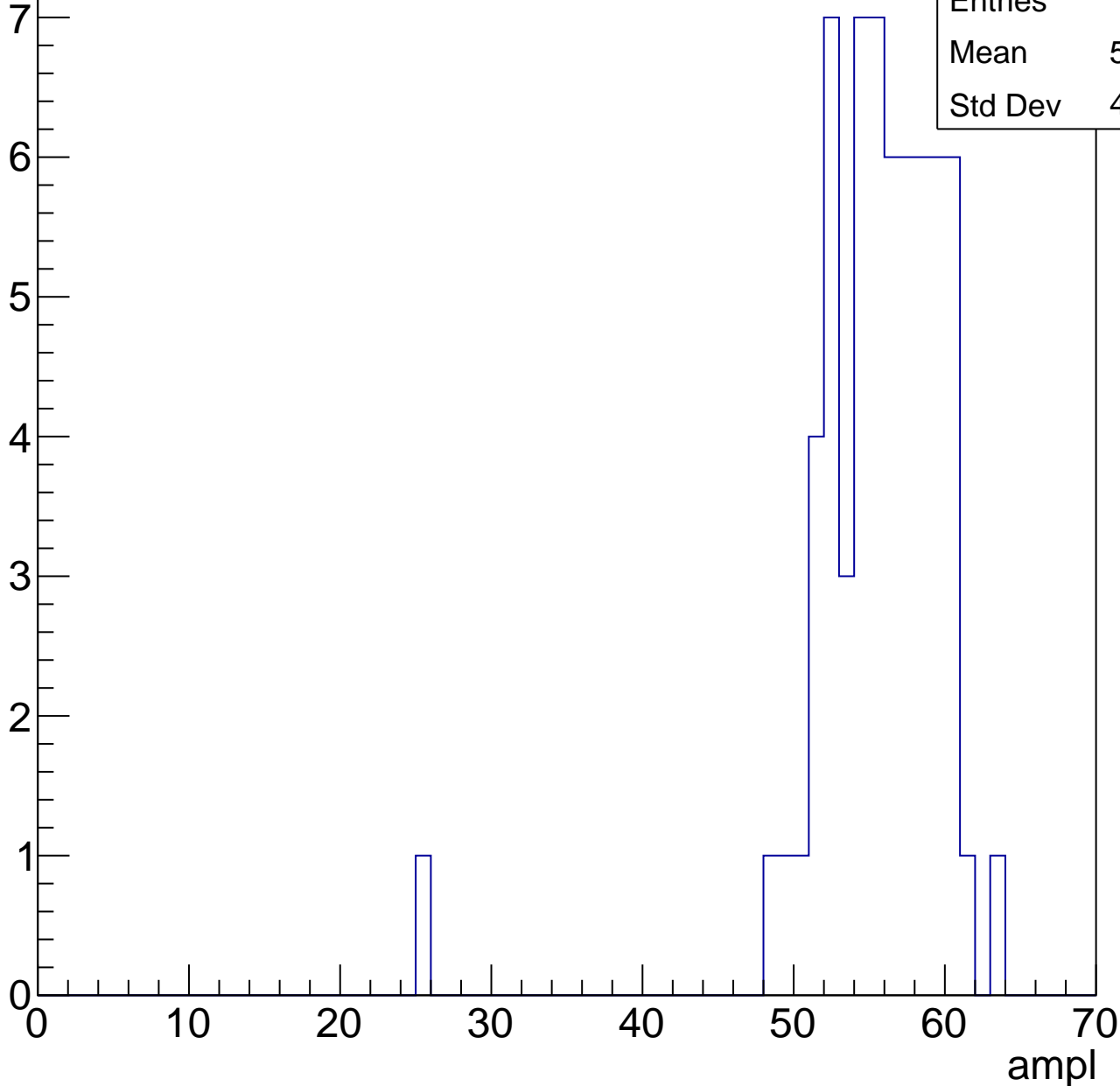


# B1L102S, U16-ch40, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	55.09
Std Dev	4.977

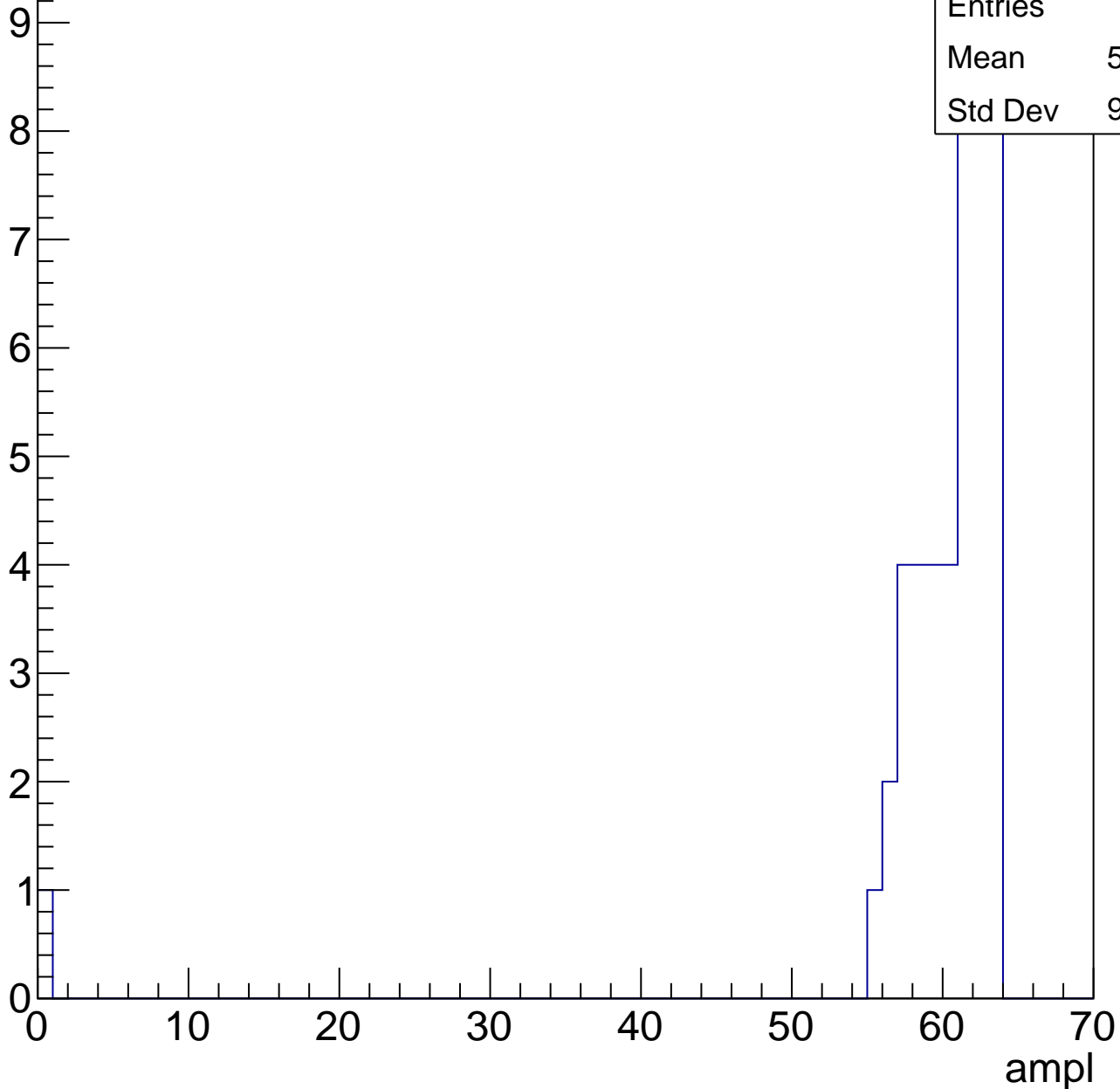


# B1L102S, U16-ch40, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	58.93
Std Dev	9.159



# B1L102S, U16-ch40, adc6

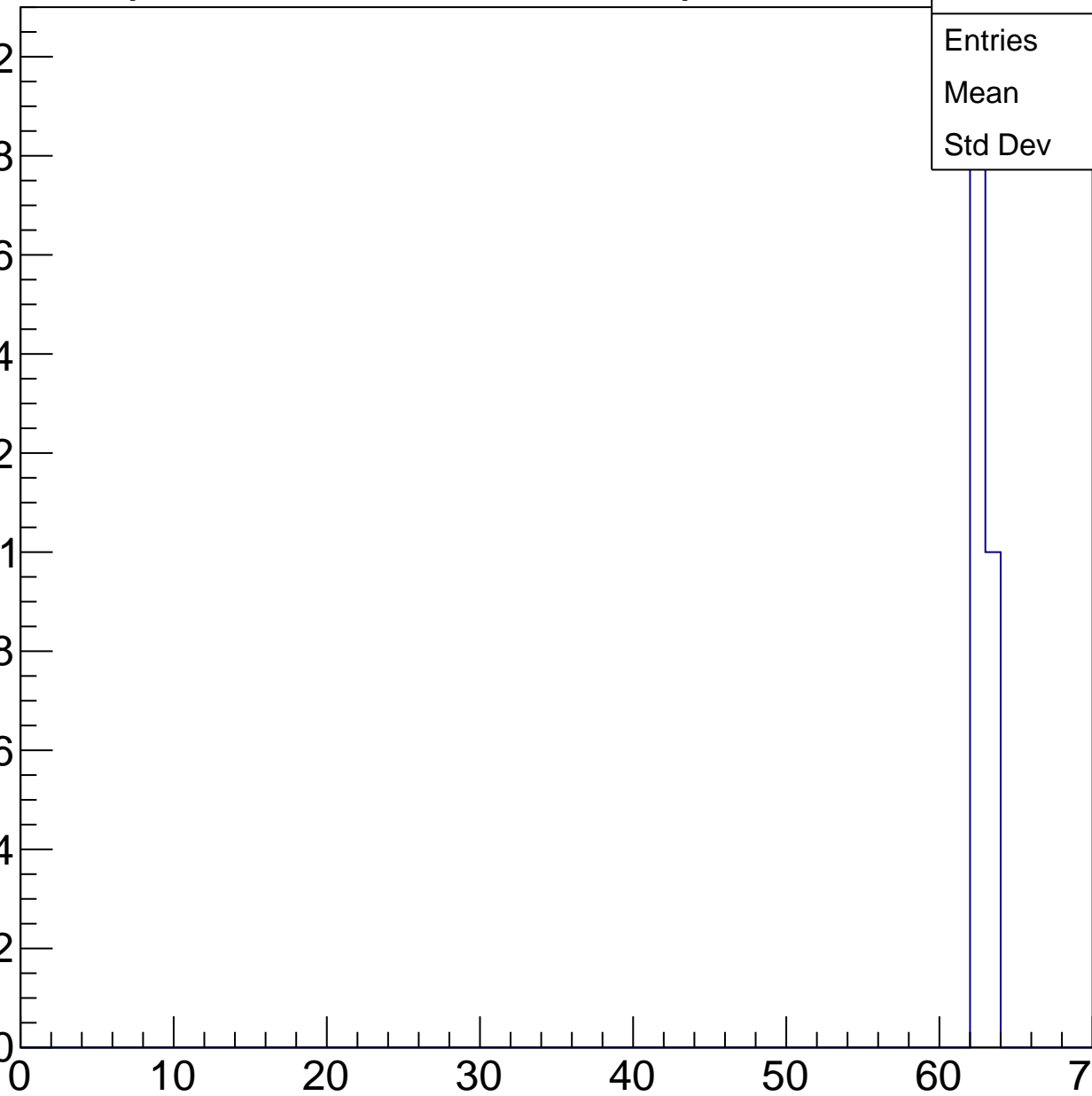
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	3
Mean	62.33
Std Dev	0.4714

ampl





# B1L102S, U16-ch40, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U16-ch41, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	74
Mean	28.09
Std Dev	3.8

**Gaus mean : 28.4708**

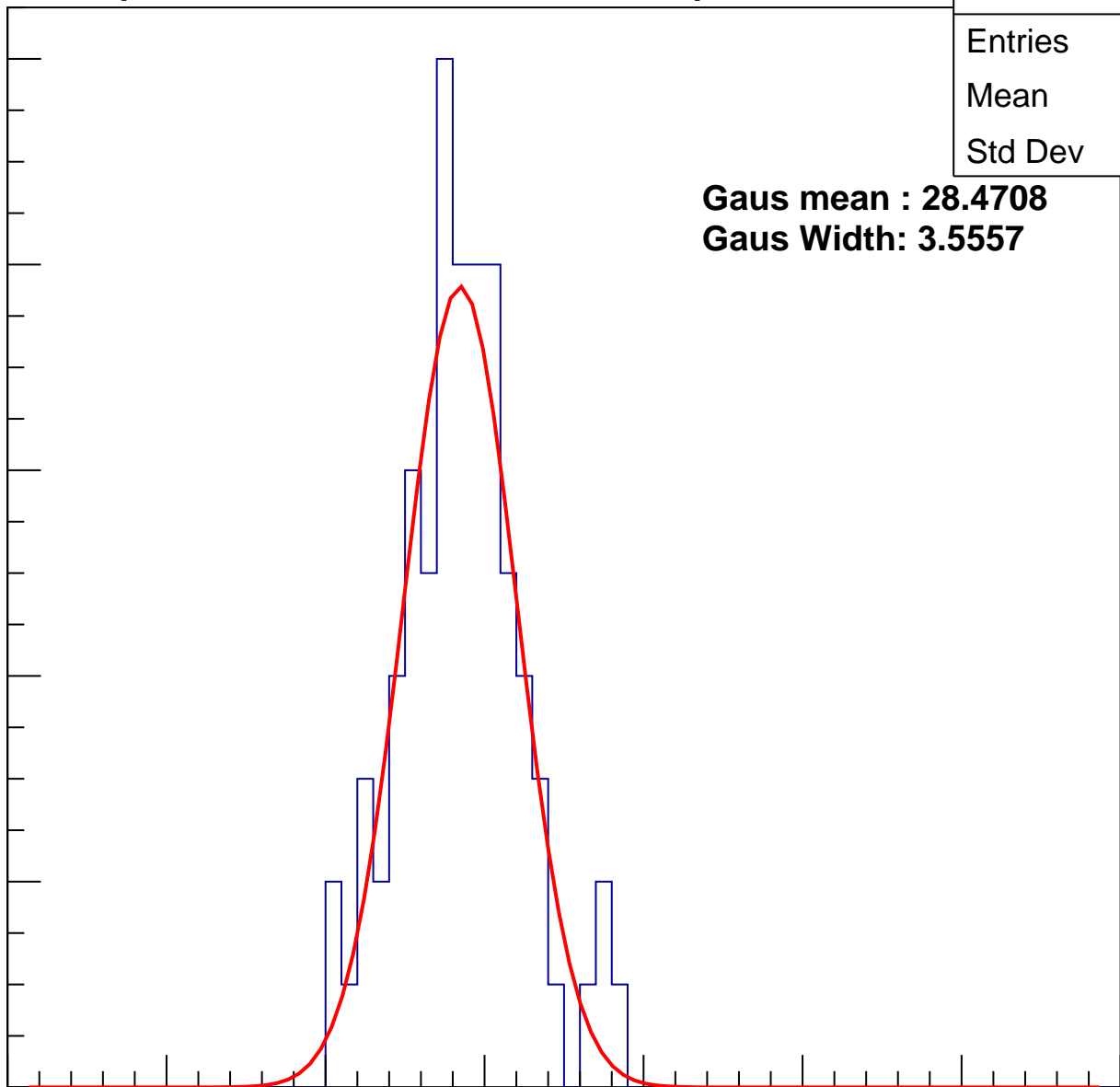
**Gaus Width: 3.5557**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U16-ch41, adc1

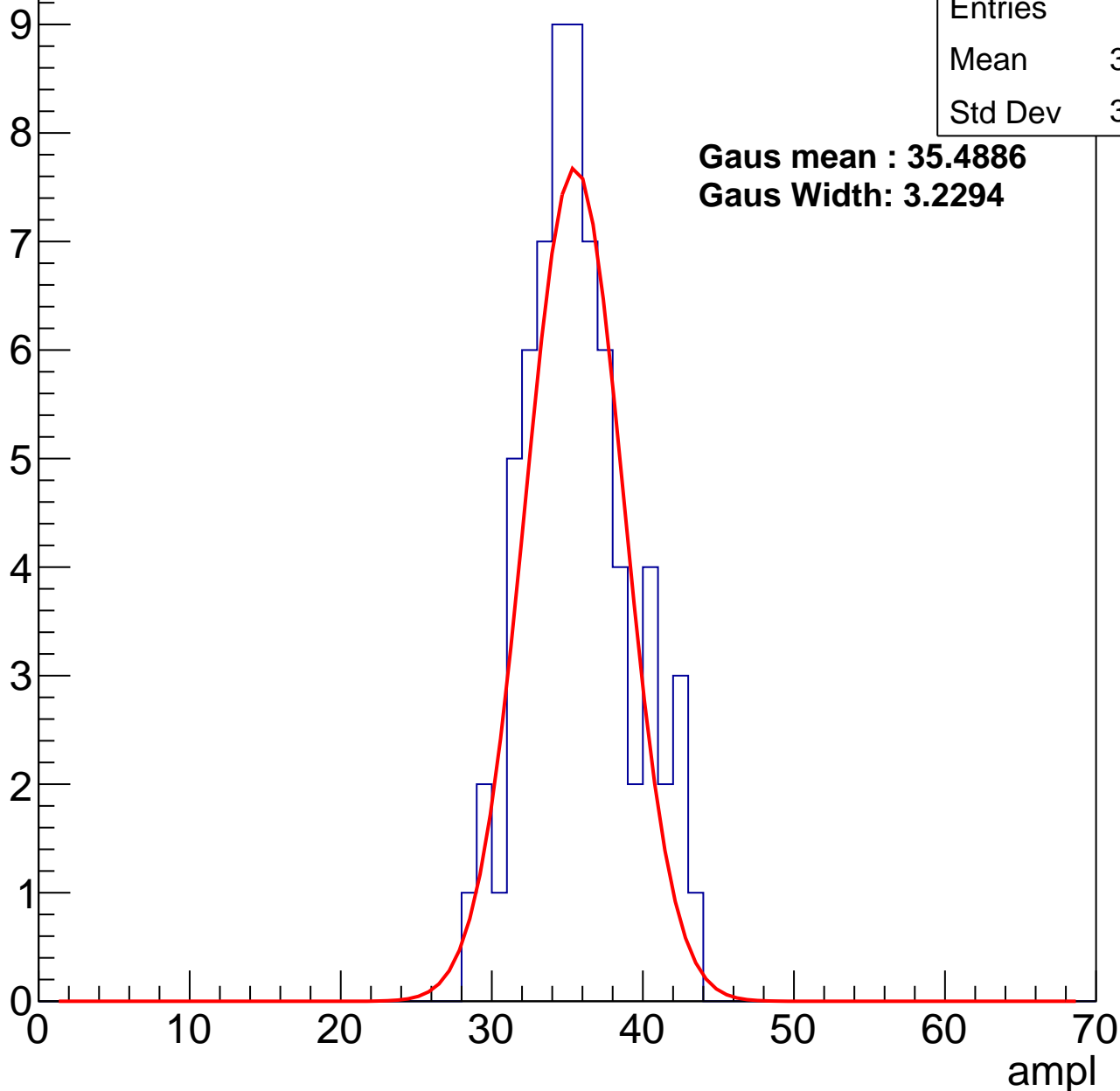
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	35.22
Std Dev	3.396

**Gaus mean : 35.4886**

**Gaus Width: 3.2294**



# B1L102S, U16-ch41, adc2

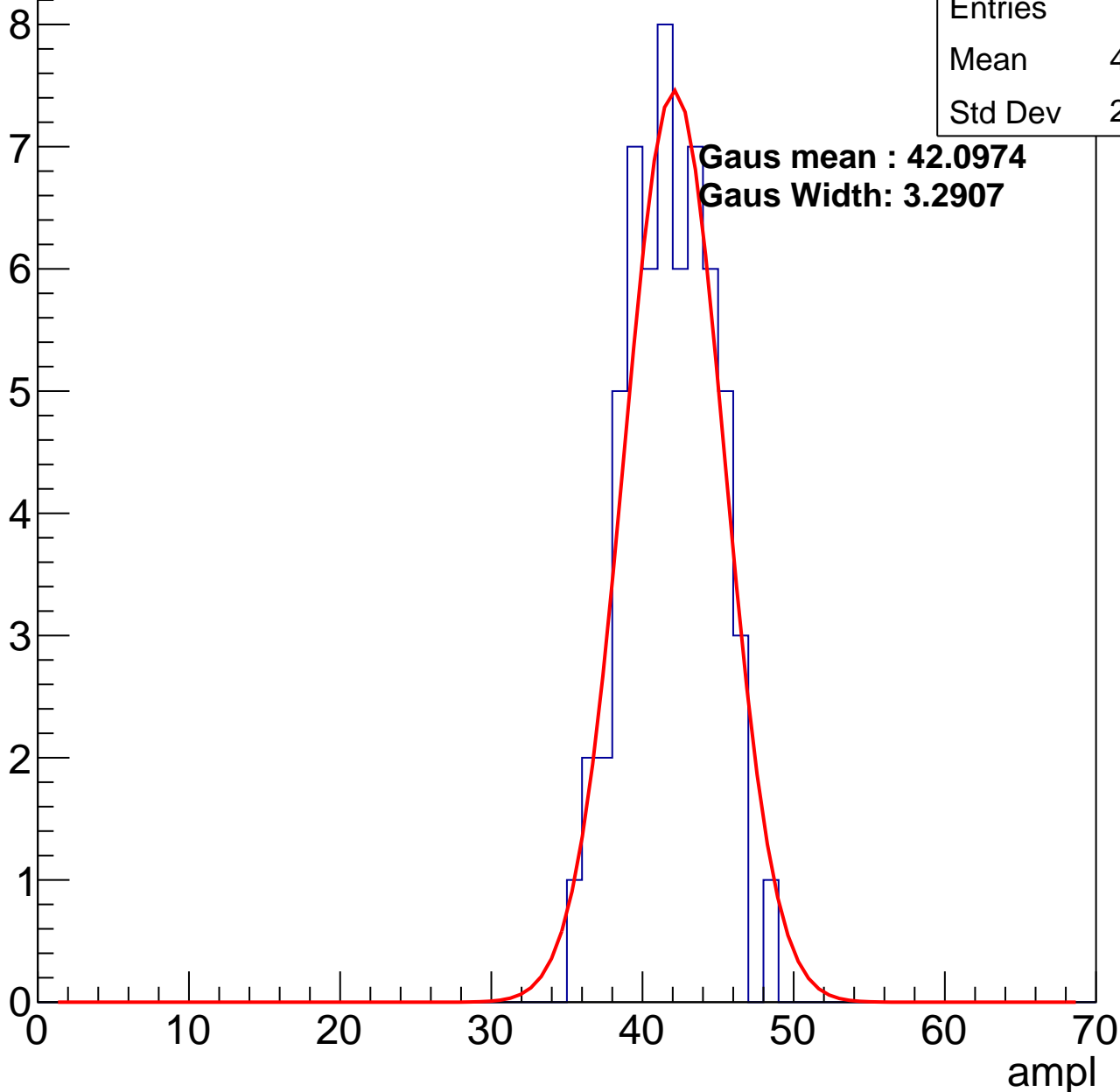
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	41.36
Std Dev	2.857

**Gaus mean : 42.0974**

**Gaus Width: 3.2907**

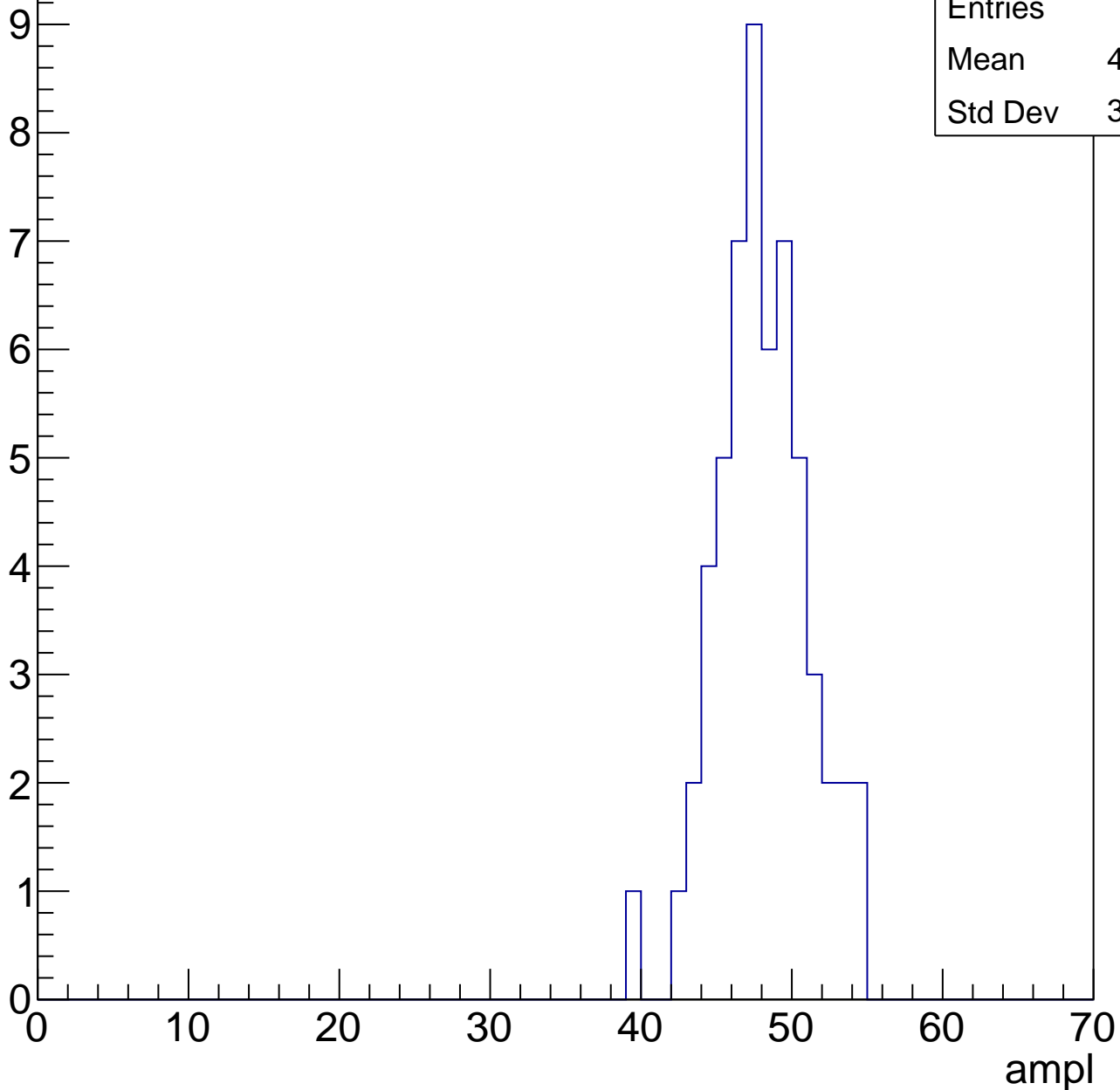


# B1L102S, U16-ch41, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	47.59
Std Dev	3.022

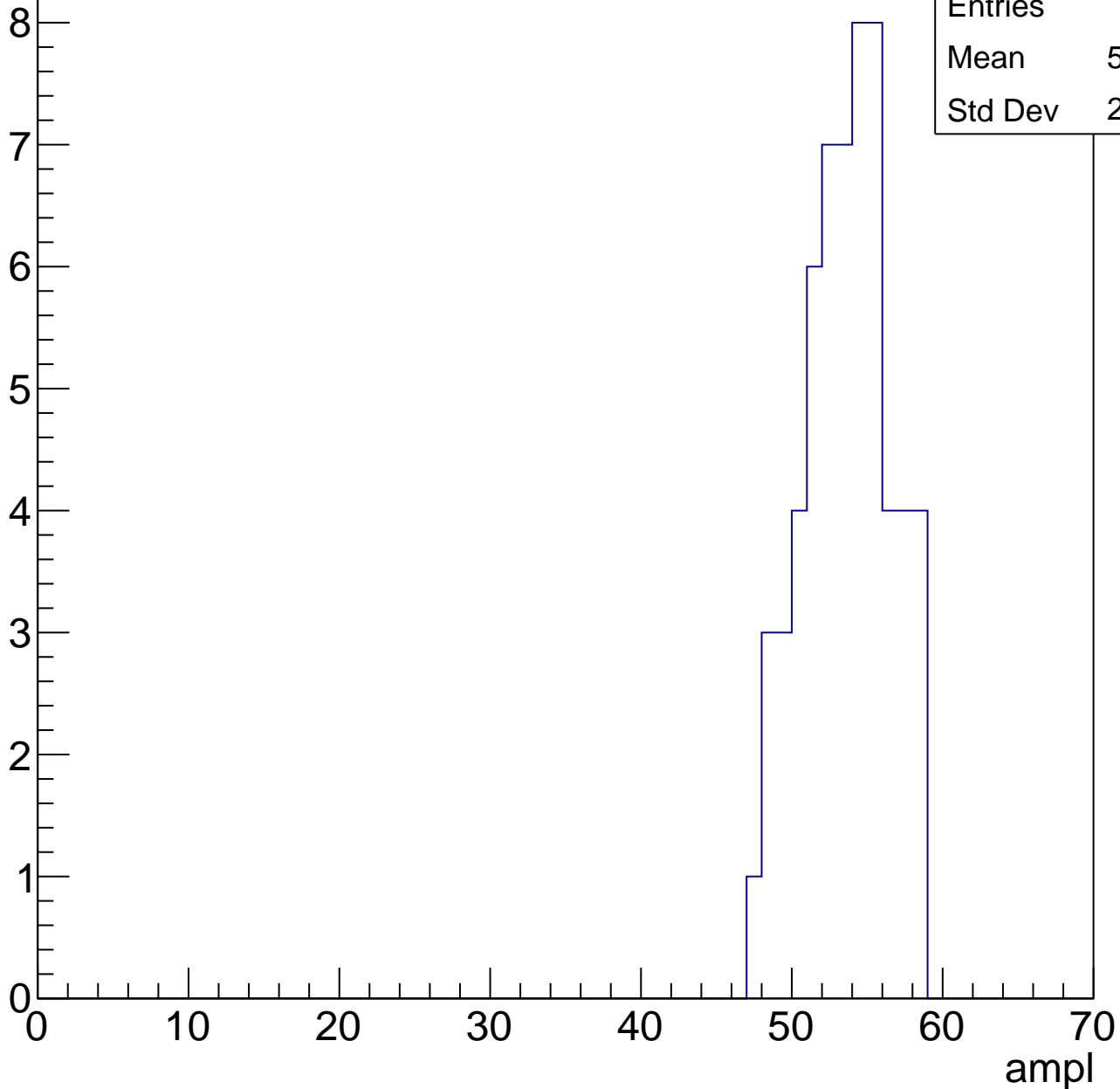


# B1L102S, U16-ch41, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	53.14
Std Dev	2.807



# B1L102S, U16-ch41, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	70
Mean	58.27
Std Dev	7.582

Entry

10

8

6

4

2

0

0

10

20

30

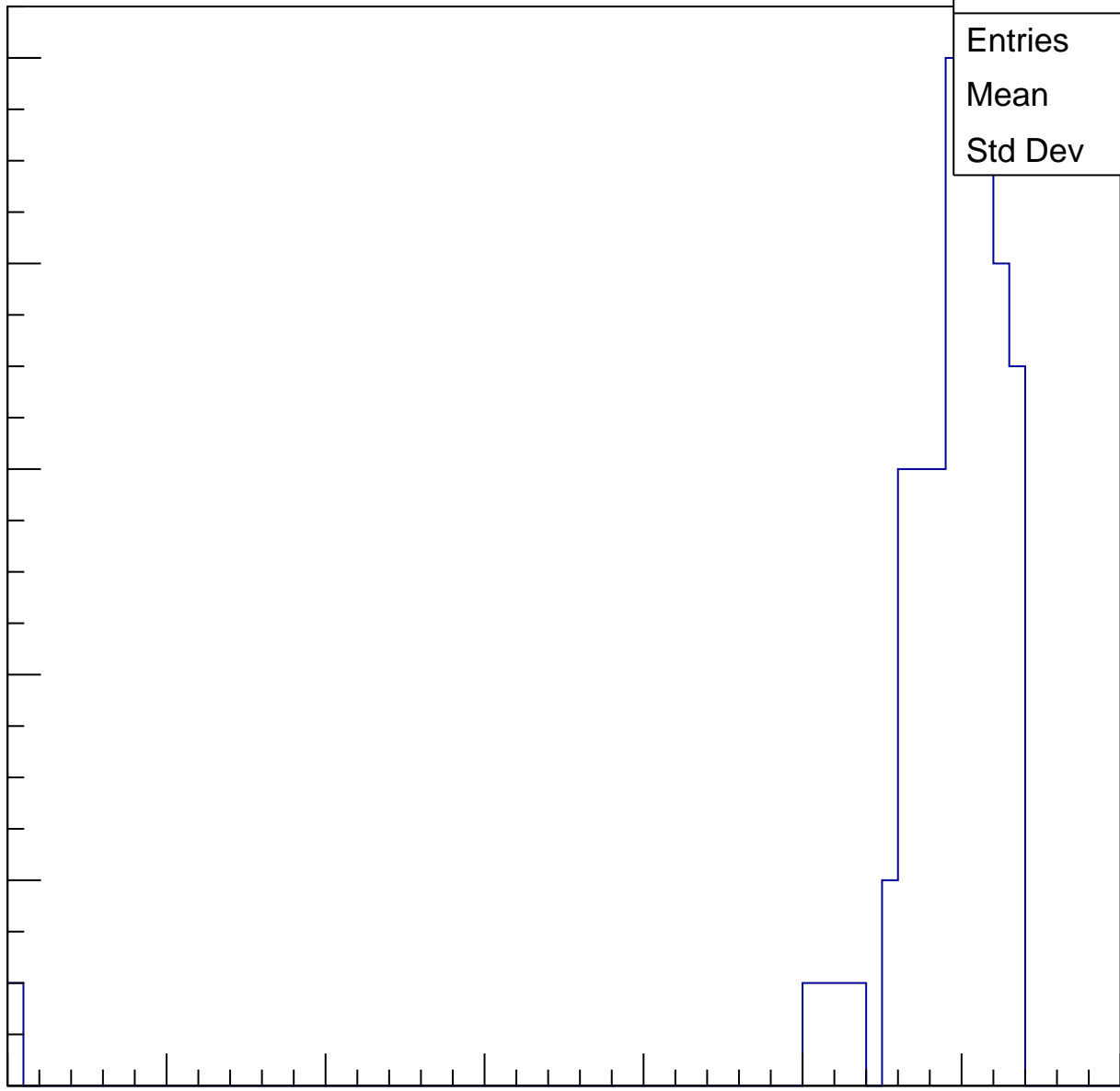
40

50

60

70

ampl



# B1L102S, U16-ch41, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch41, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch42, adc0

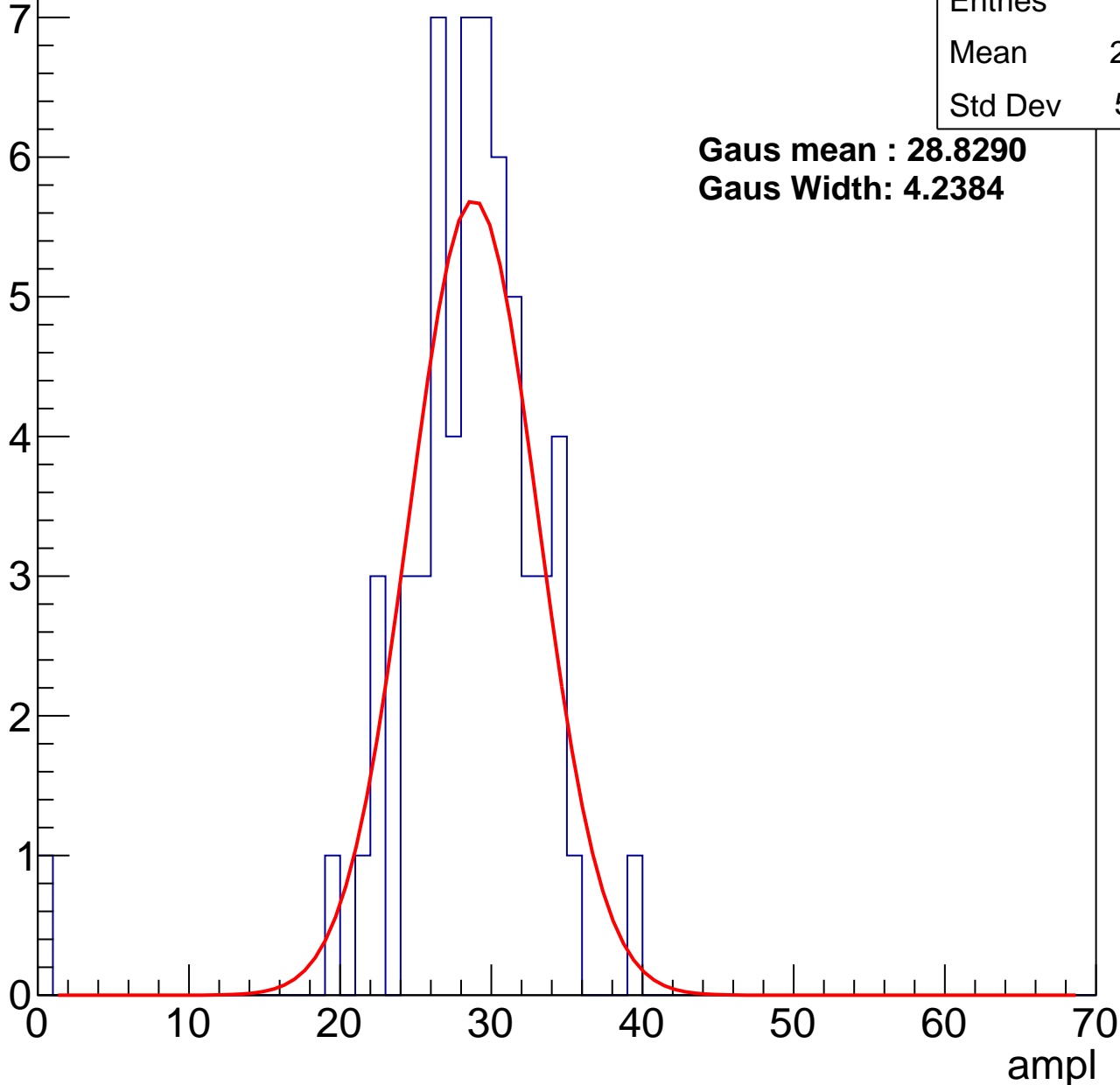
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	28.03
Std Dev	5.231

**Gaus mean : 28.8290**

**Gaus Width: 4.2384**



# B1L102S, U16-ch42, adc1

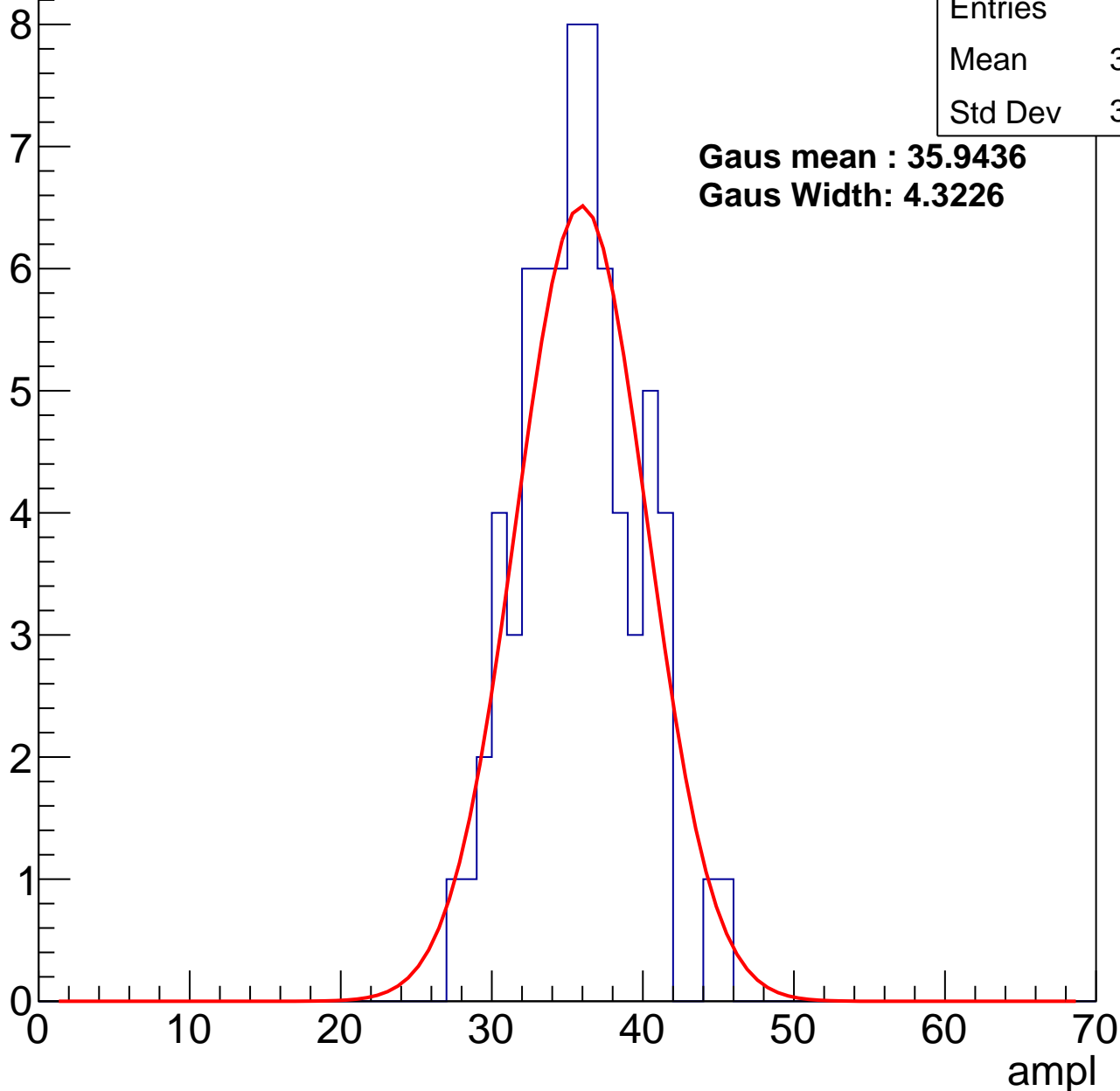
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	35.25
Std Dev	3.766

**Gaus mean : 35.9436**

**Gaus Width: 4.3226**



# B1L102S, U16-ch42, adc2

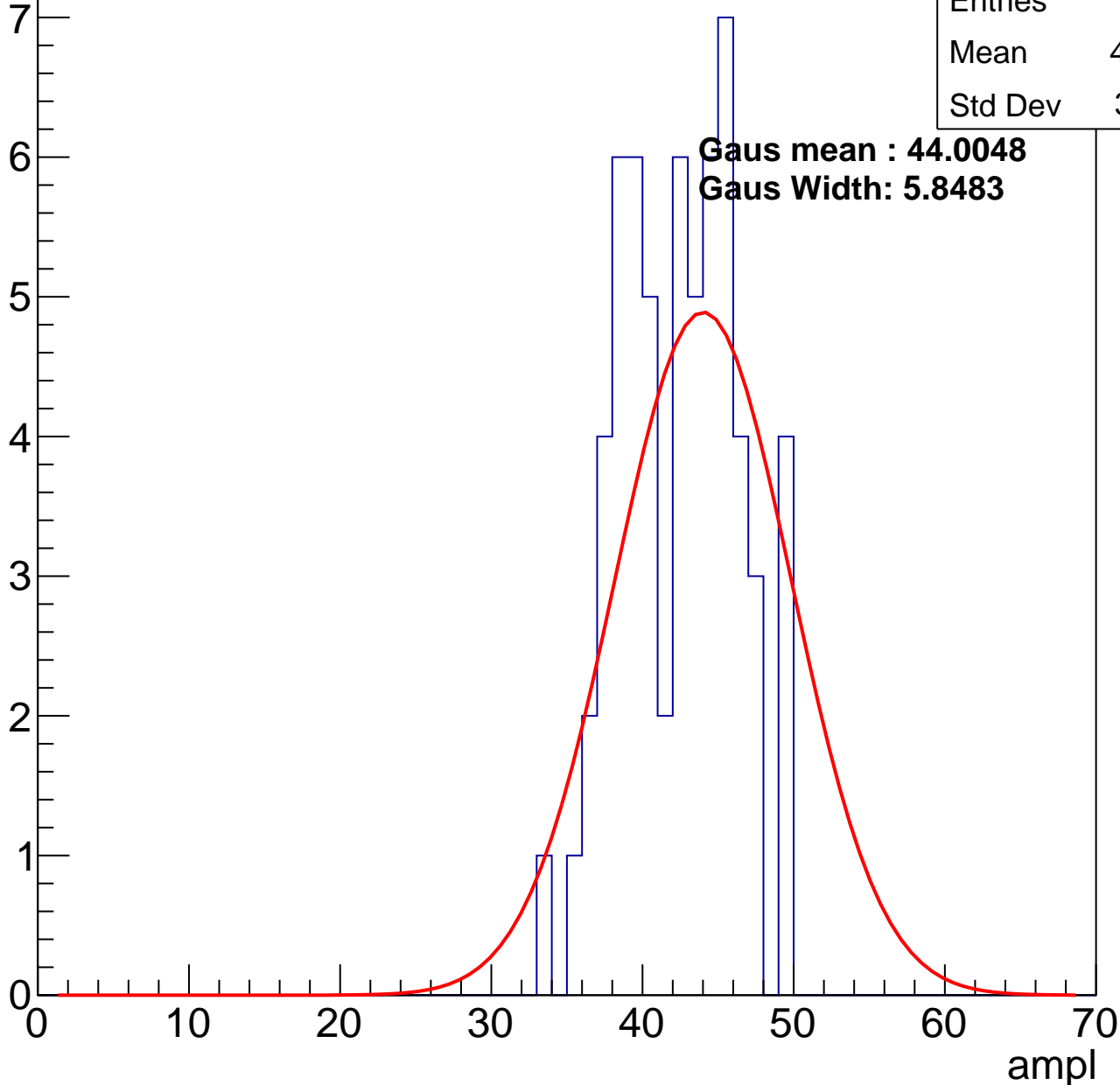
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	41.92
Std Dev	3.811

**Gaus mean : 44.0048**

**Gaus Width: 5.8483**

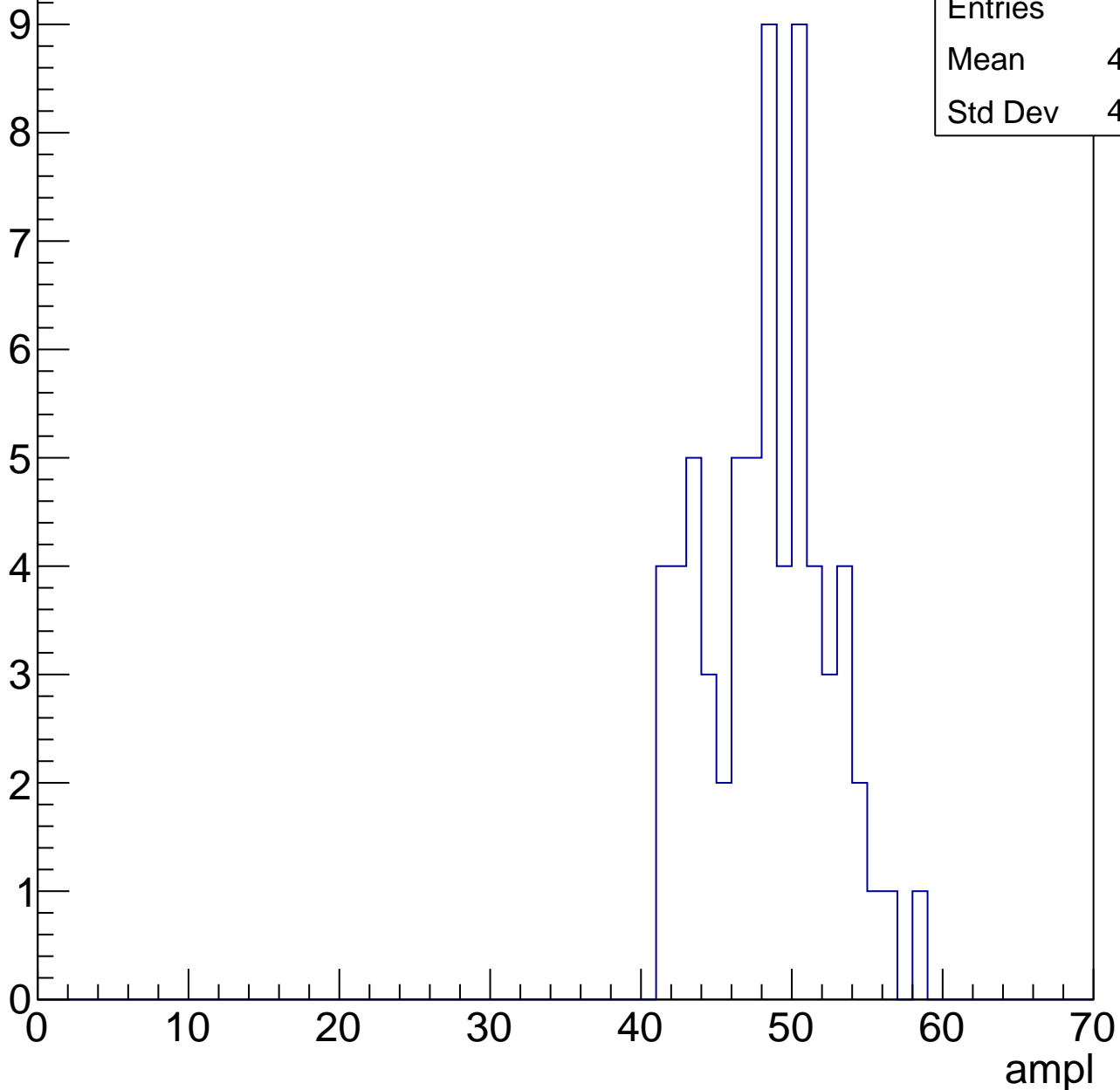


# B1L102S, U16-ch42, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	47.89
Std Dev	4.016

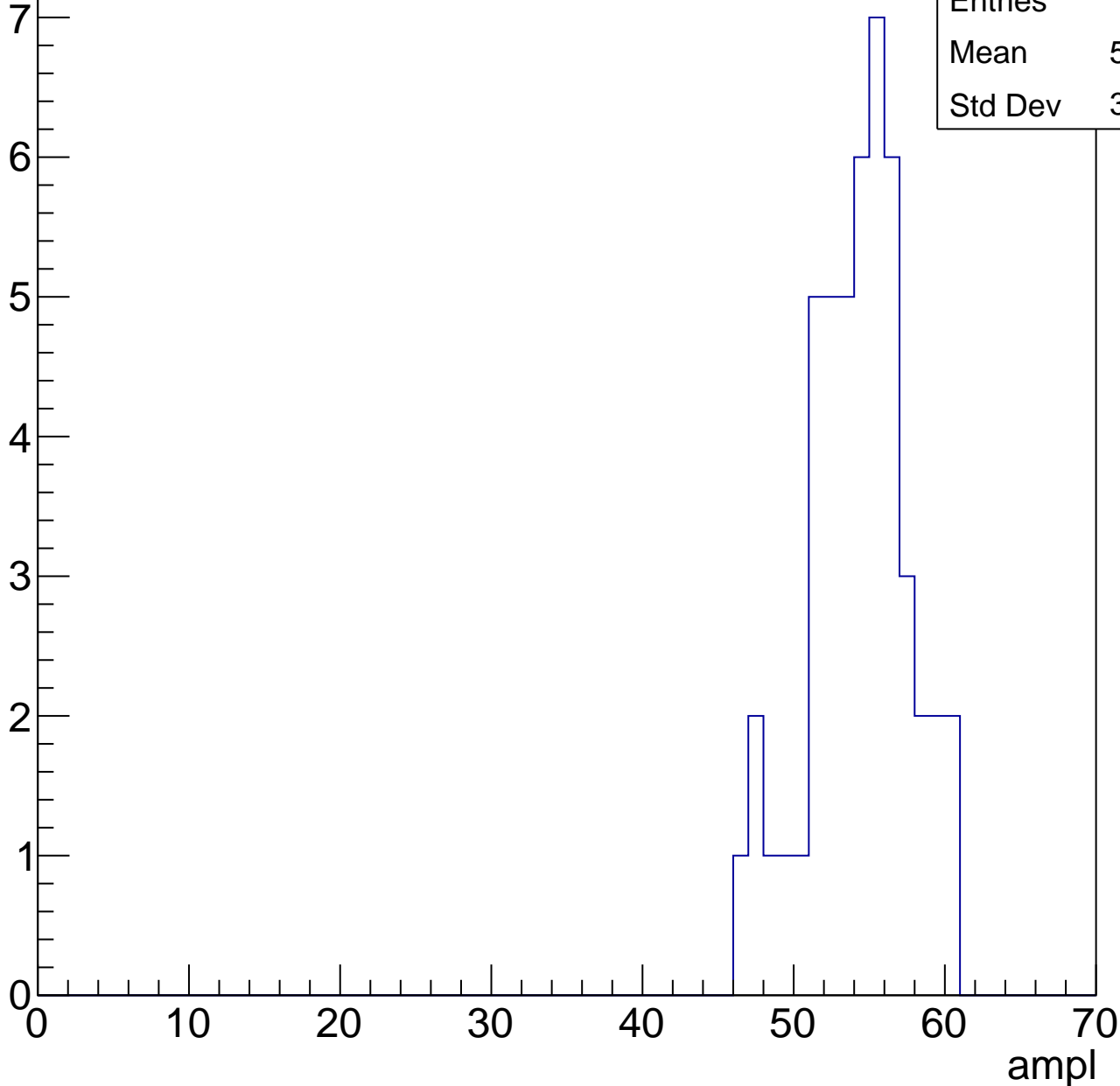


# B1L102S, U16-ch42, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	53.82
Std Dev	3.256

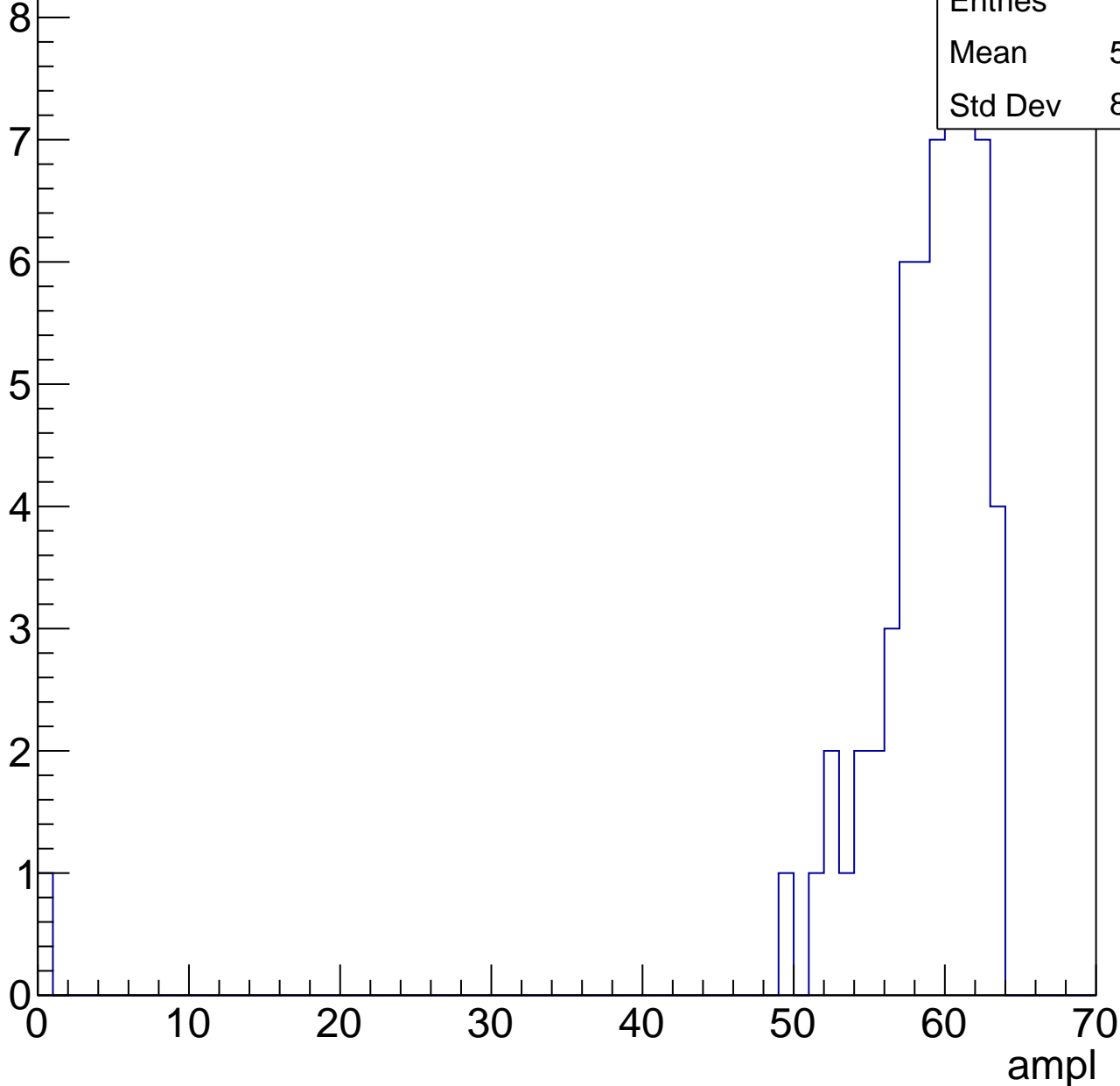


# B1L102S, U16-ch42, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	57.63
Std Dev	8.207

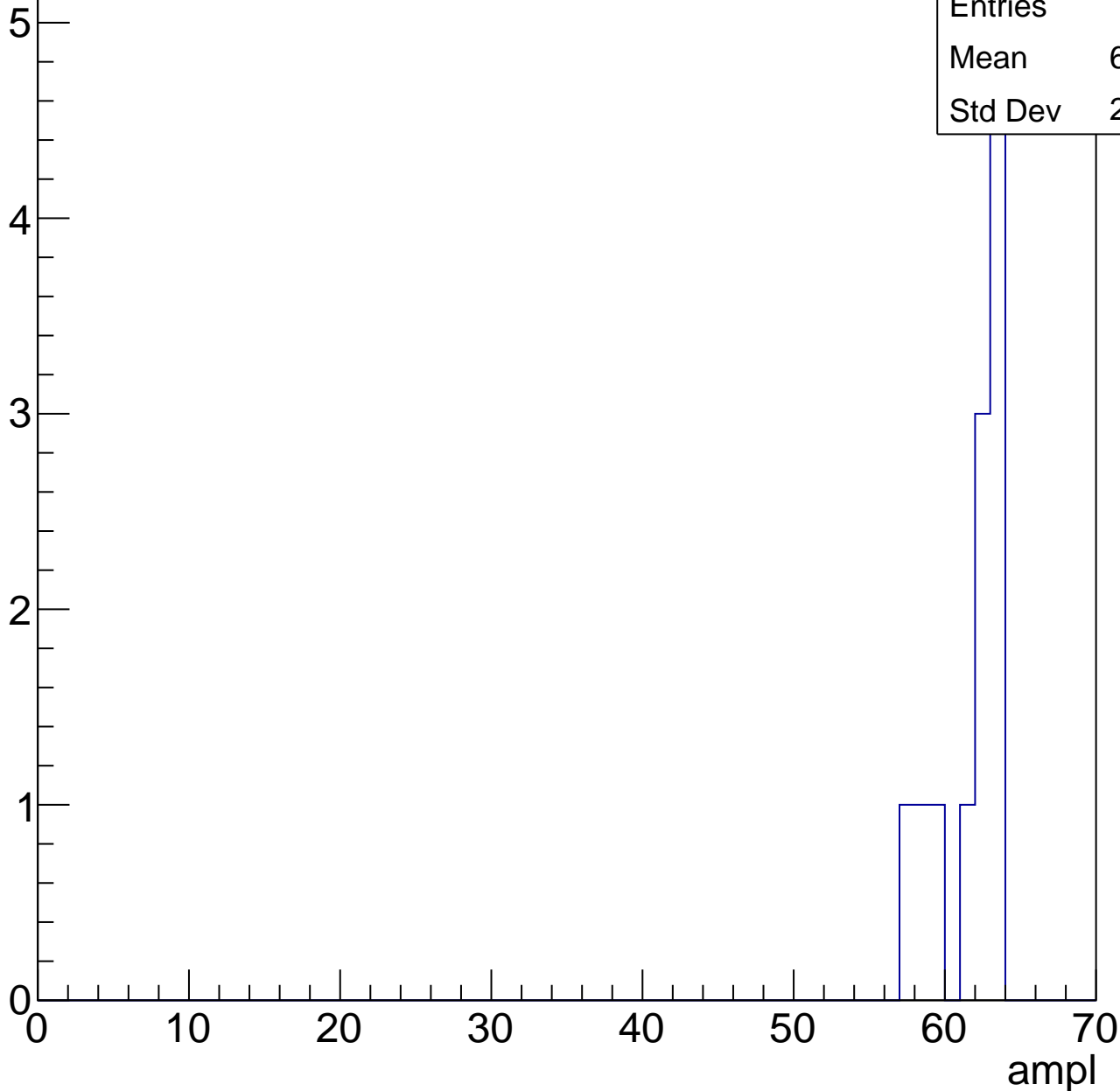


# B1L102S, U16-ch42, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	12
Mean	61.33
Std Dev	2.055

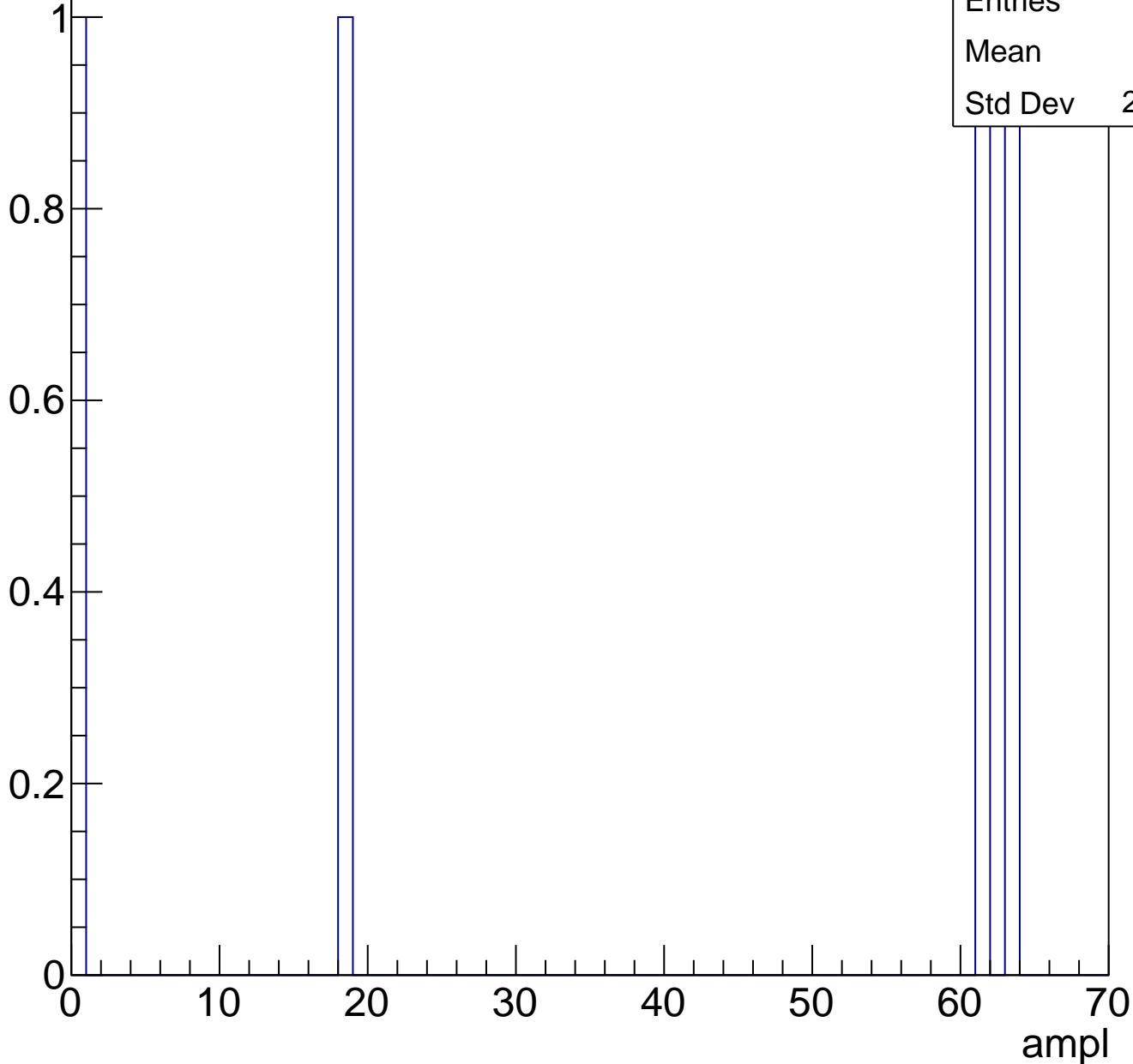




# B1L102S, U16-ch42, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch43, adc0

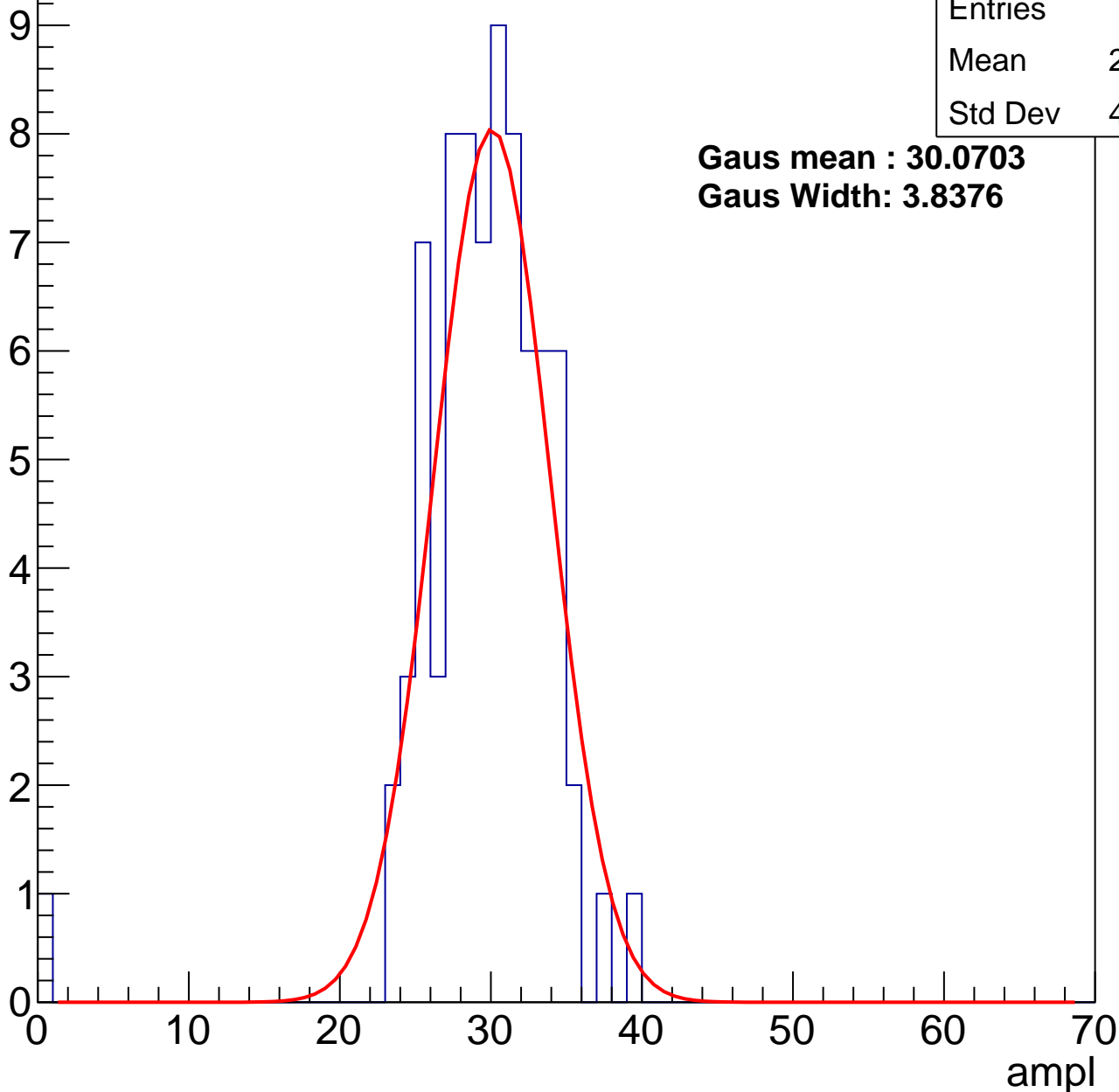
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	29.13
Std Dev	4.727

**Gaus mean : 30.0703**

**Gaus Width: 3.8376**



# B1L102S, U16-ch43, adc1

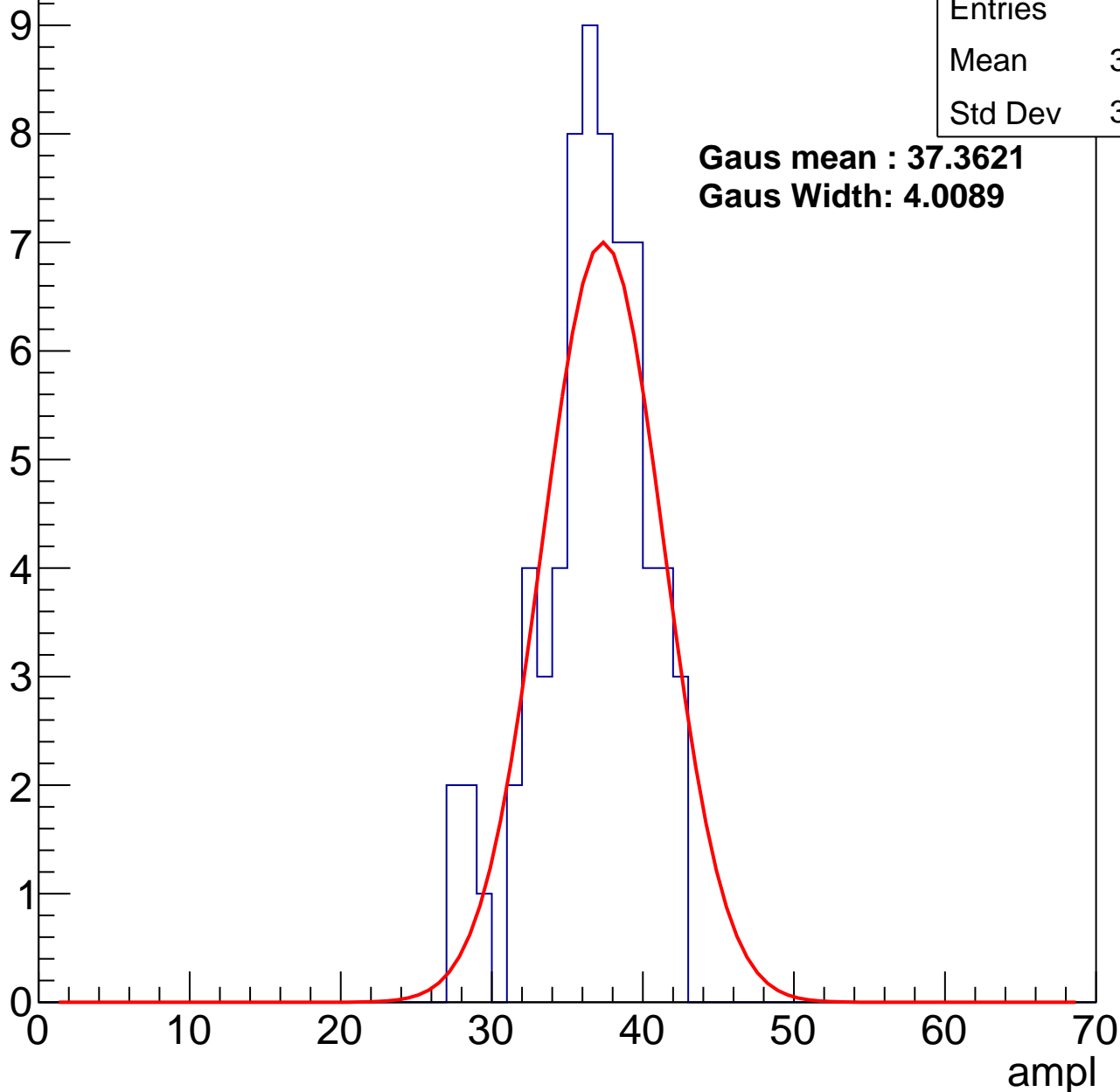
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	36.07
Std Dev	3.586

**Gaus mean : 37.3621**

**Gaus Width: 4.0089**



# B1L102S, U16-ch43, adc2

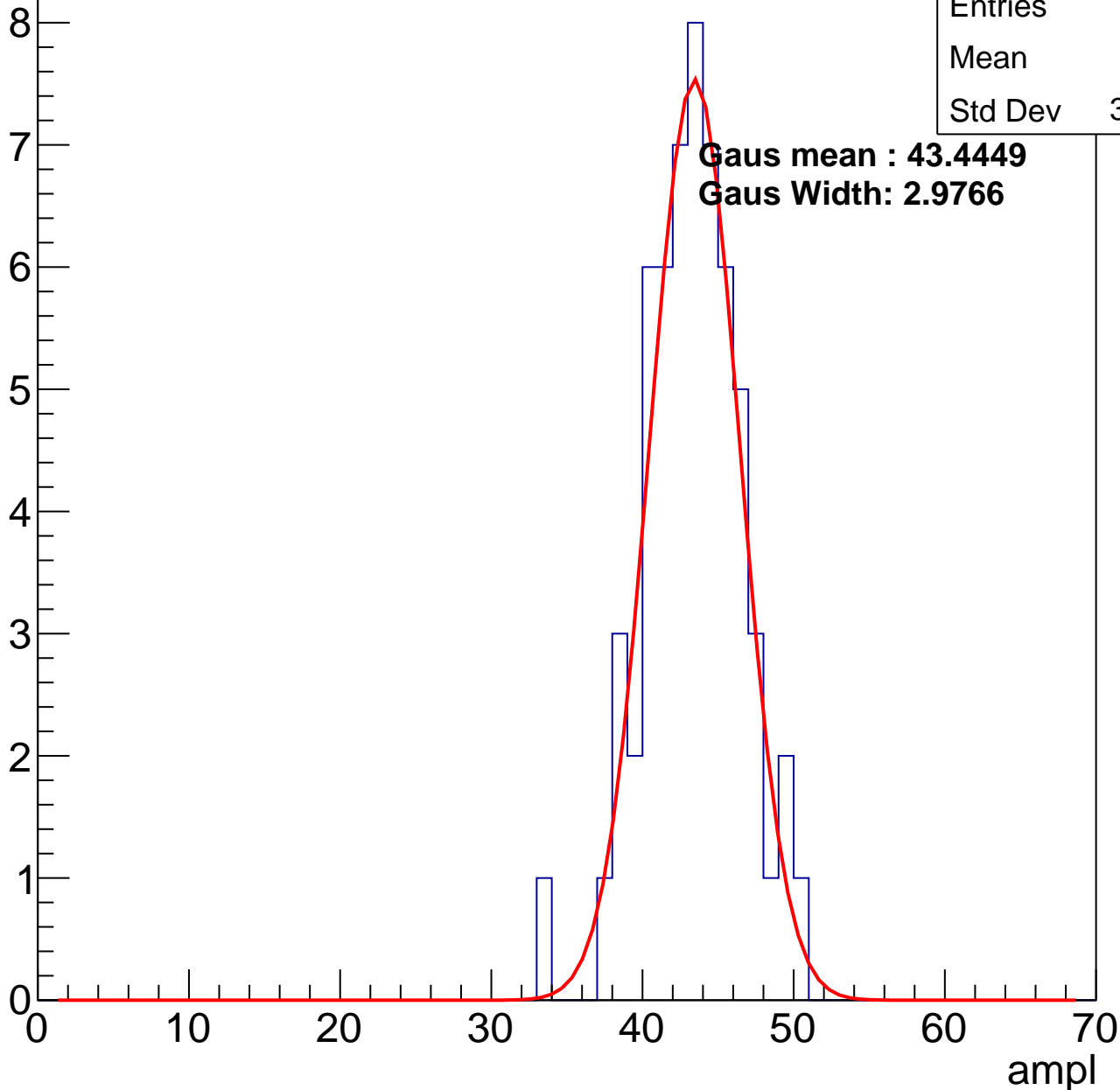
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	42.9
Std Dev	3.182

**Gaus mean : 43.4449**

**Gaus Width: 2.9766**

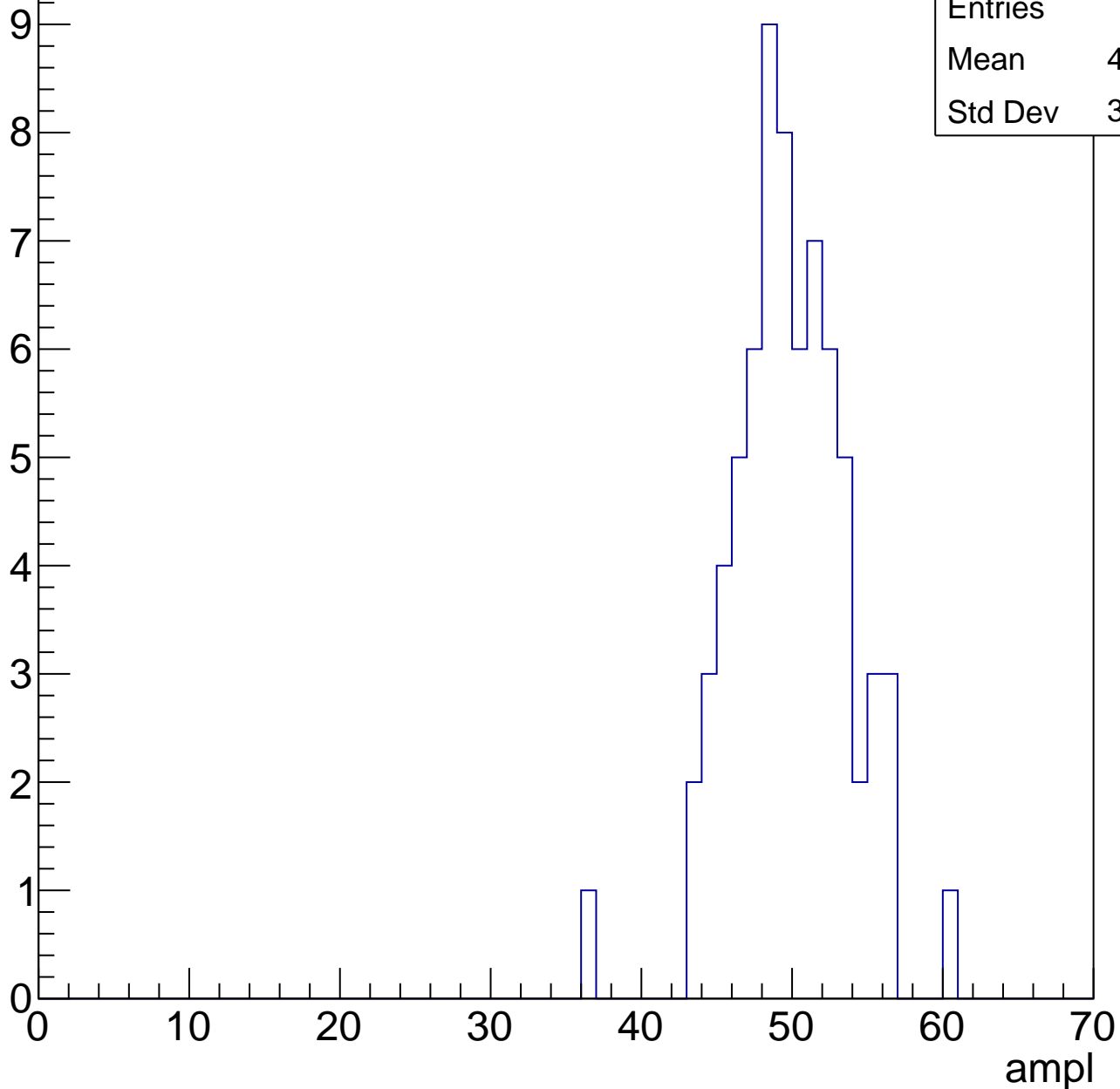


# B1L102S, U16-ch43, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	49.37
Std Dev	3.832

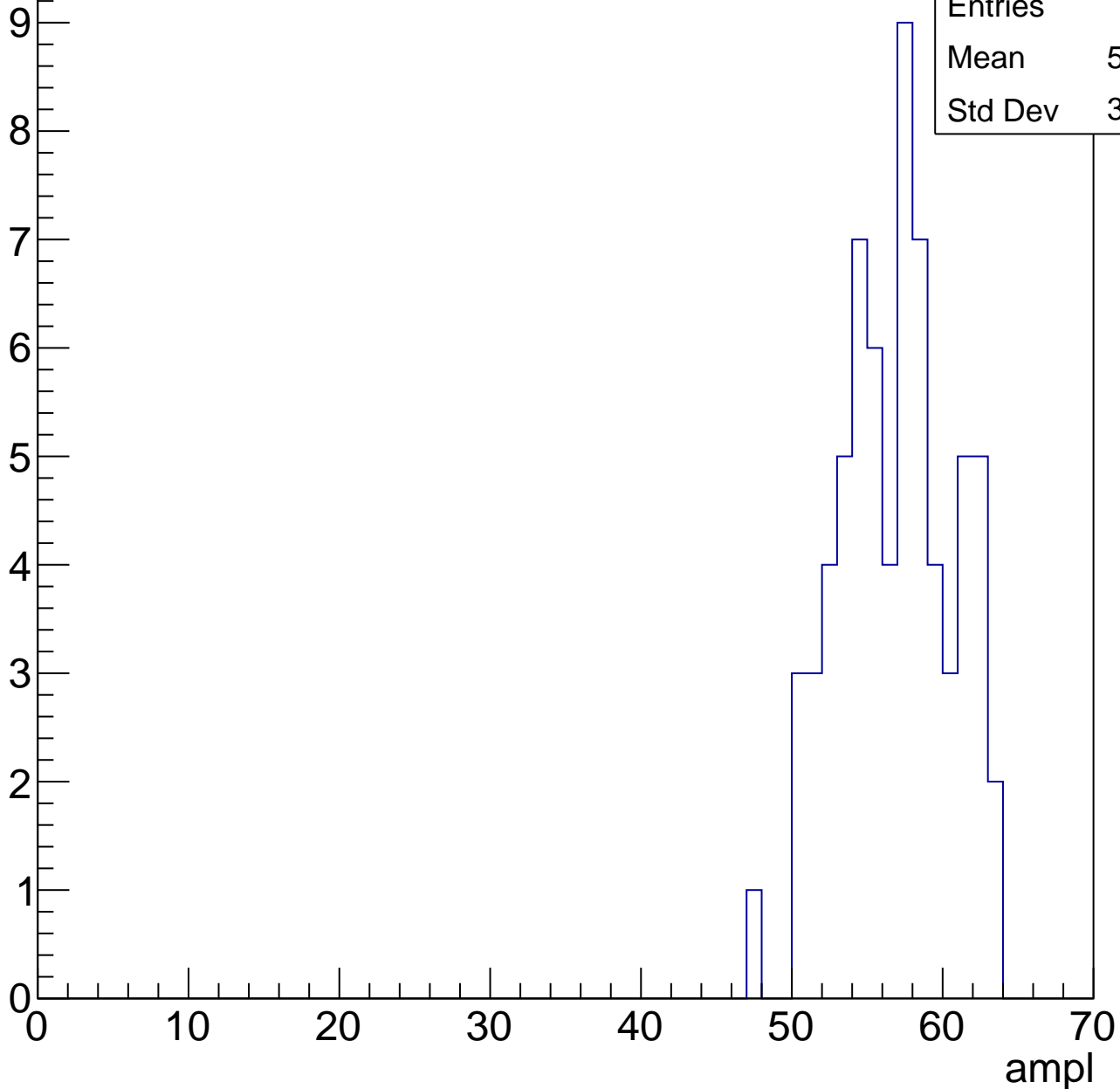


# B1L102S, U16-ch43, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

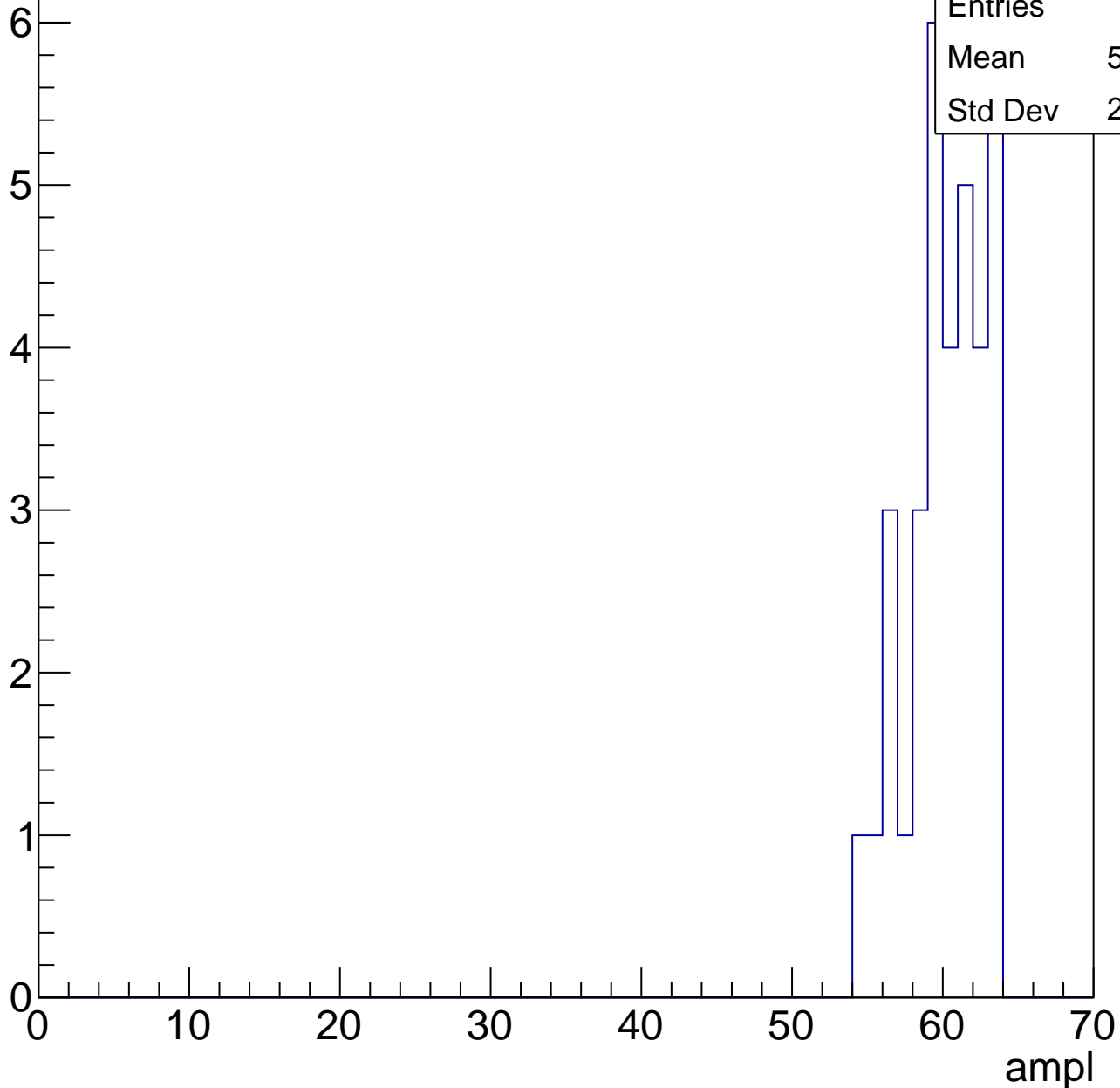
Entries	68
Mean	56.34
Std Dev	3.685



# B1L102S, U16-ch43, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch43, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

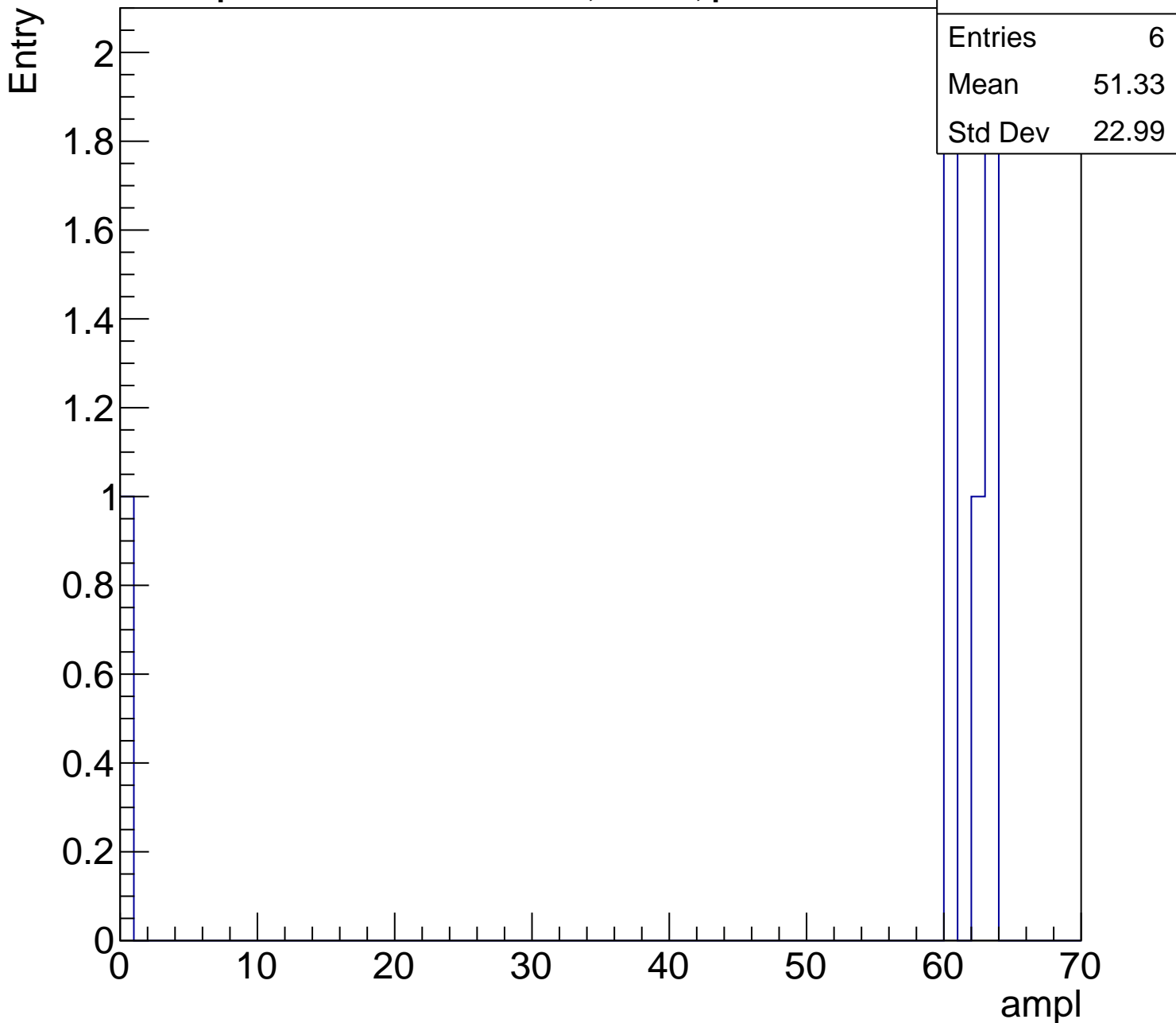
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	6
Mean	51.33
Std Dev	22.99

0 10 20 30 40 50 60 70

ampl





# B1L102S, U16-ch43, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U16-ch44, adc0

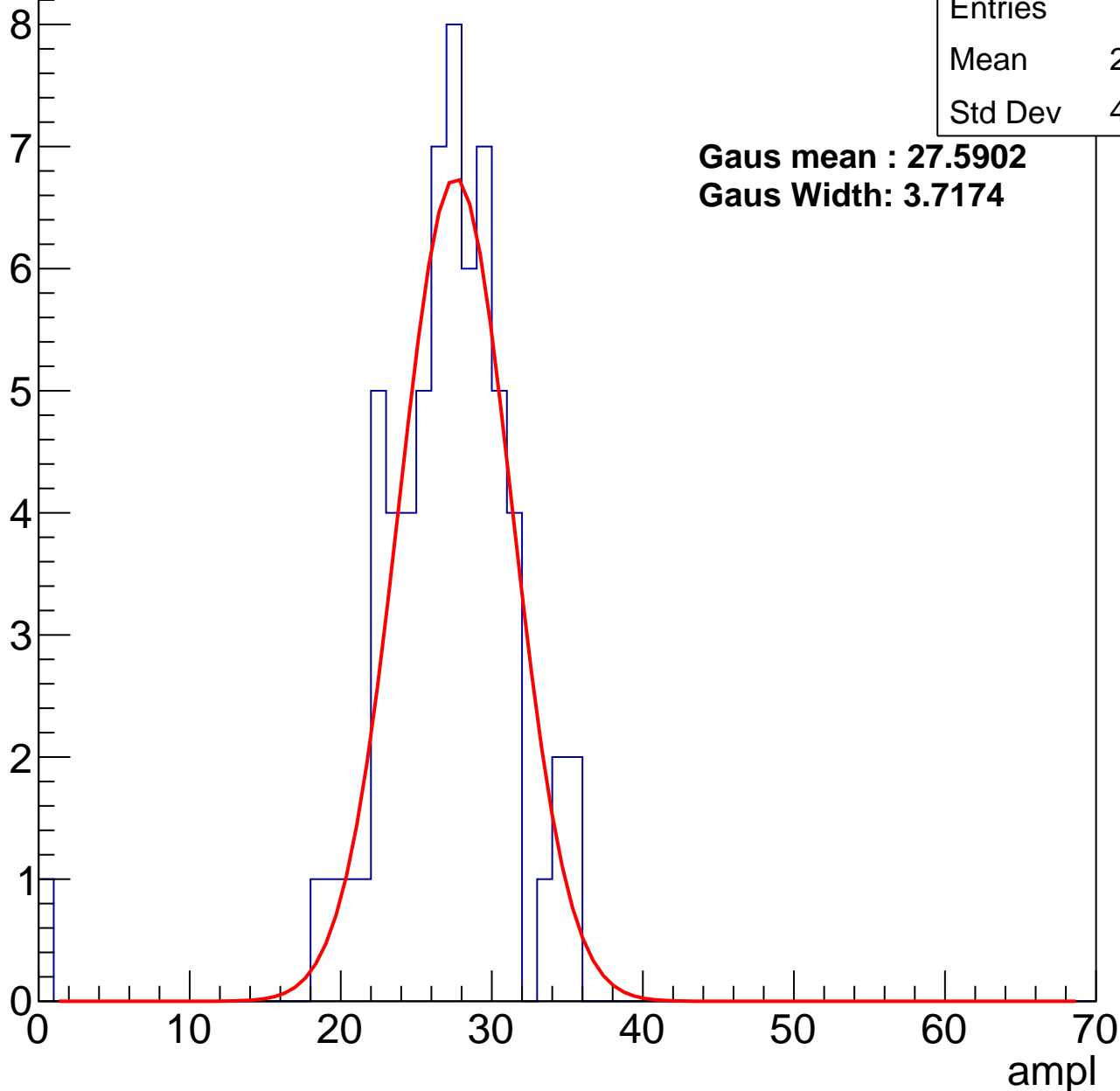
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	26.38
Std Dev	4.948

**Gaus mean : 27.5902**

**Gaus Width: 3.7174**



# B1L102S, U16-ch44, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	80
Mean	33.86
Std Dev	3.632

**Gaus mean : 34.4823**

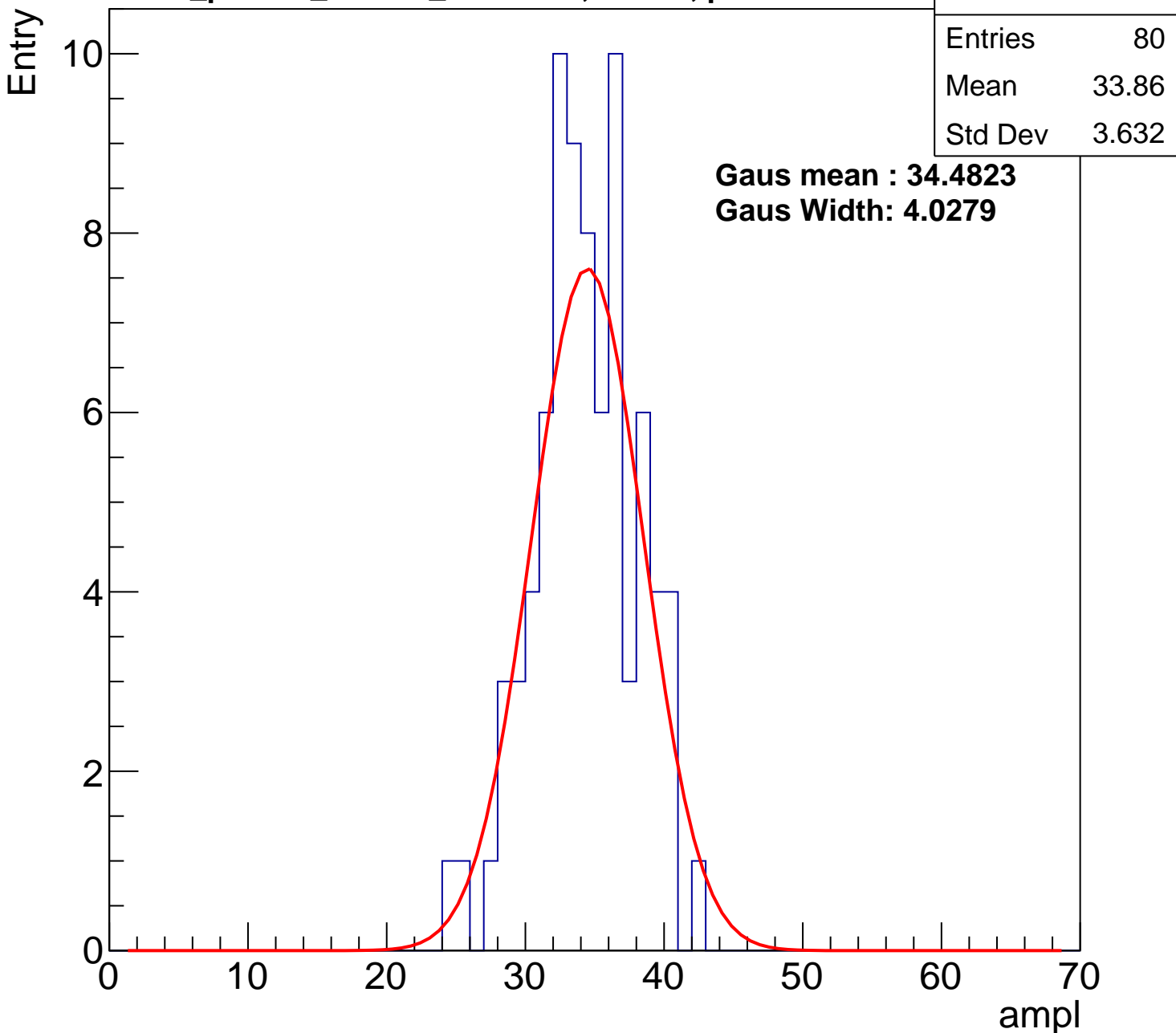
**Gaus Width: 4.0279**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U16-ch44, adc2

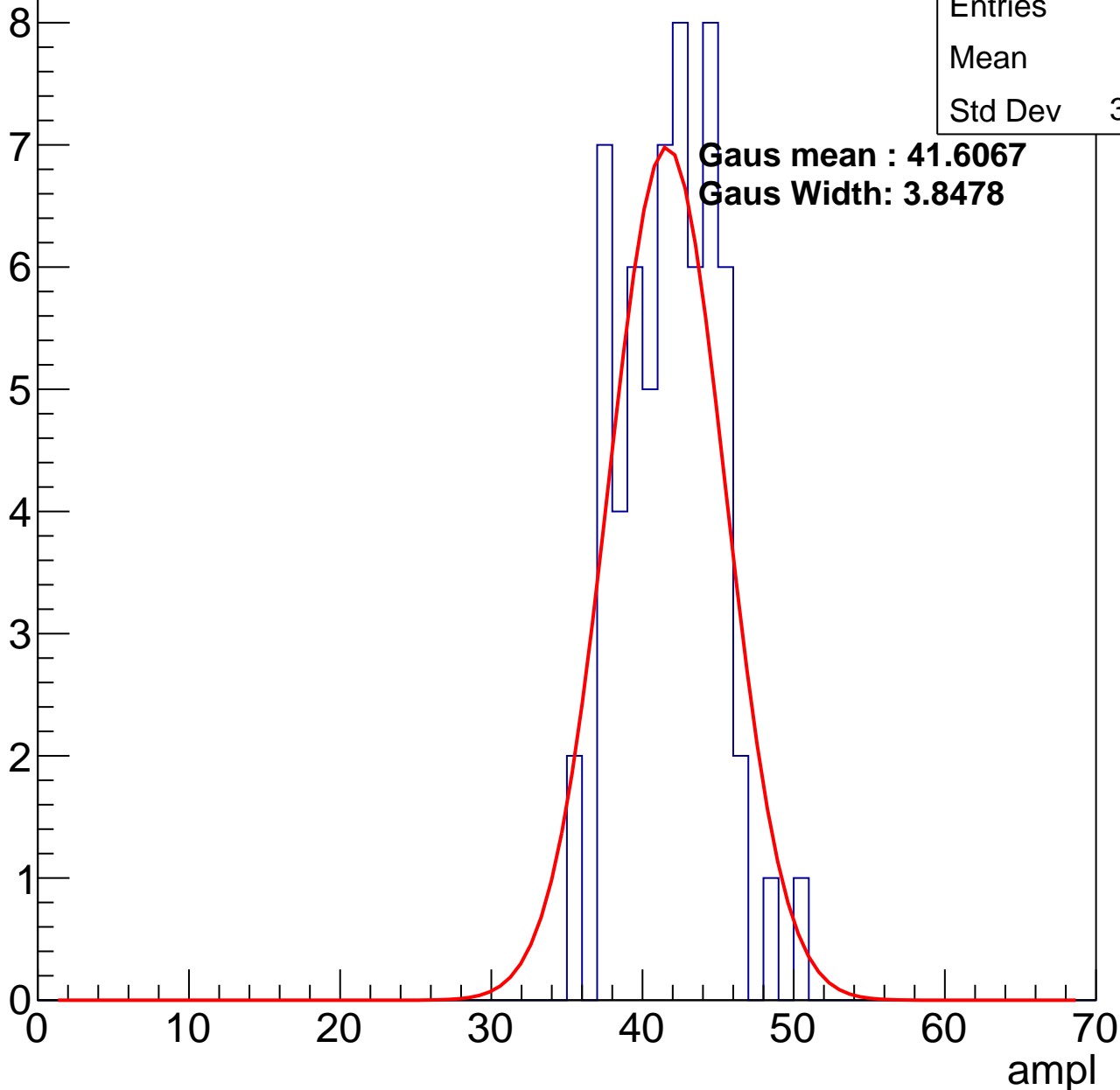
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	41.4
Std Dev	3.135

**Gaus mean : 41.6067**

**Gaus Width: 3.8478**

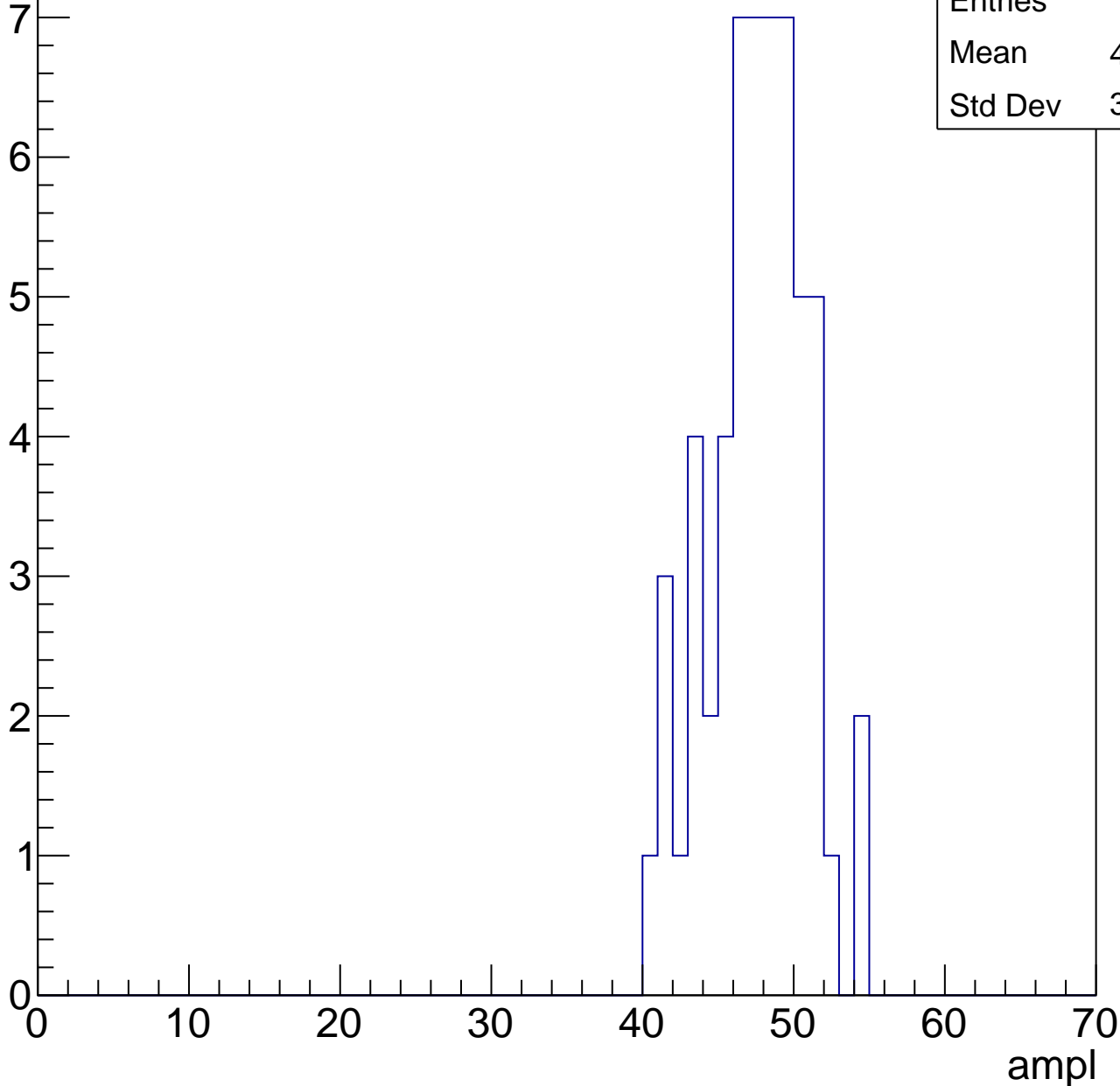


# B1L102S, U16-ch44, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	47.14
Std Dev	3.187

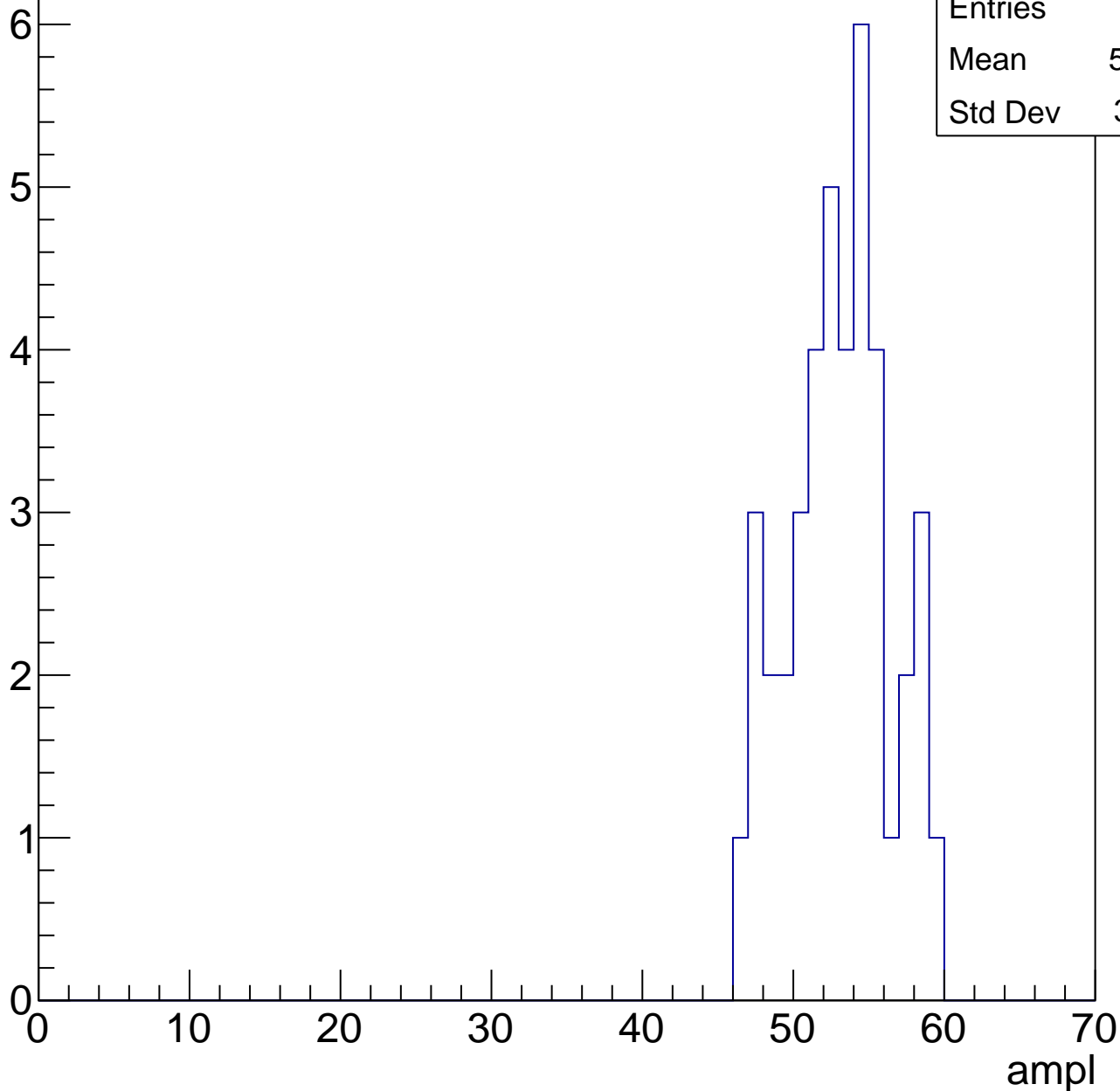


# B1L102S, U16-ch44, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	41
Mean	52.54
Std Dev	3.321

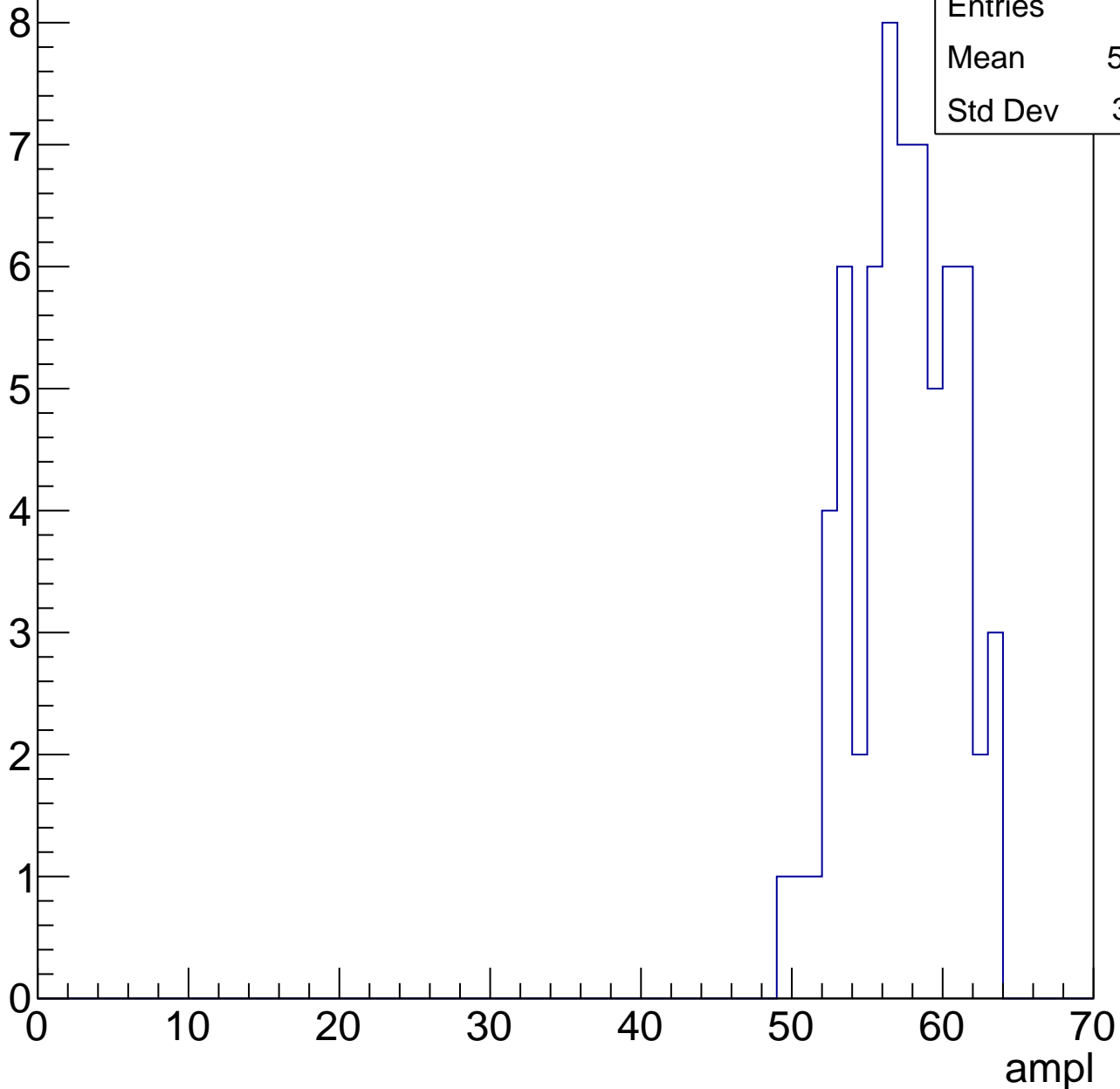


# B1L102S, U16-ch44, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	56.94
Std Dev	3.351

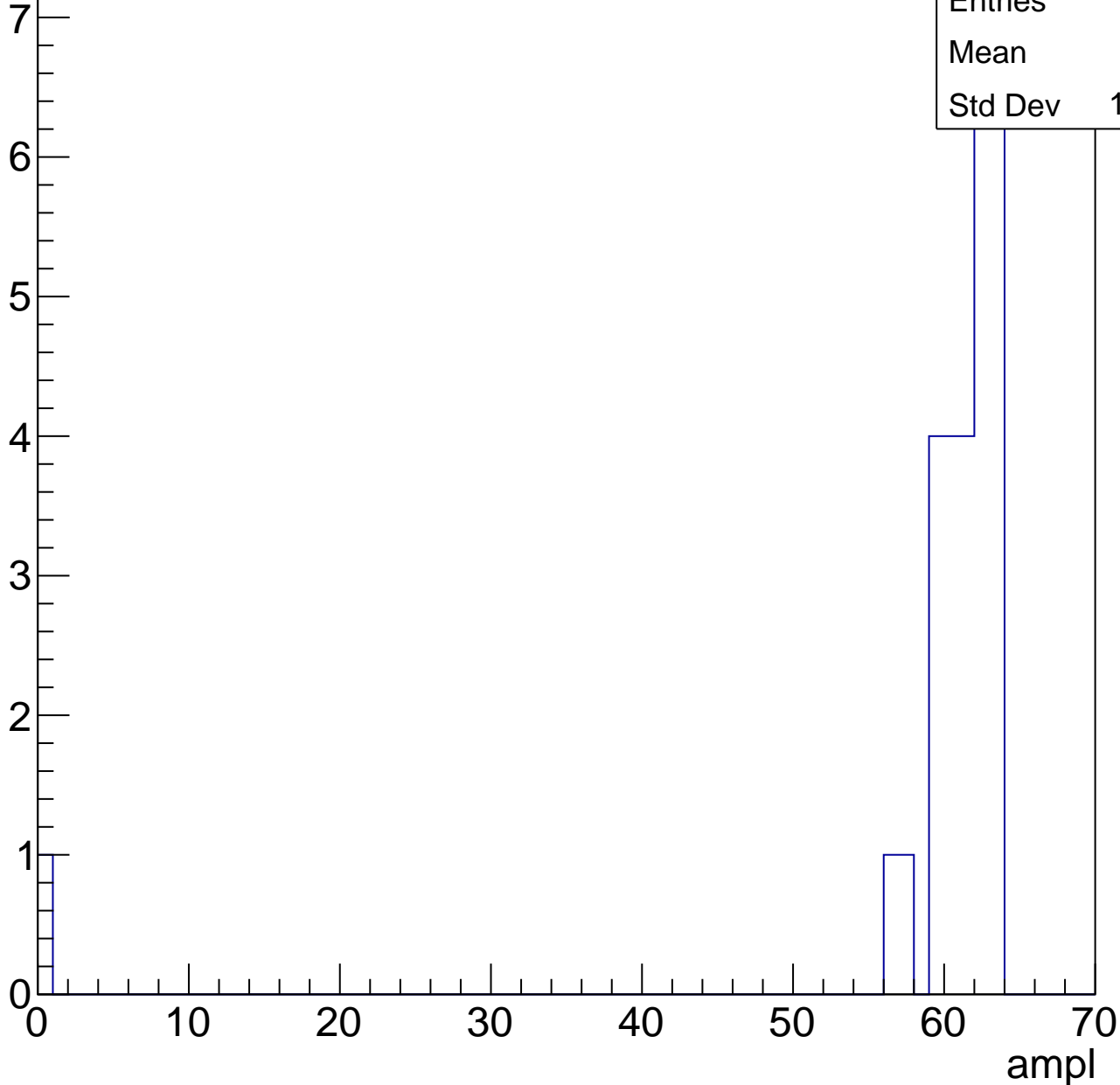


# B1L102S, U16-ch44, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	29
Mean	58.9
Std Dev	11.28

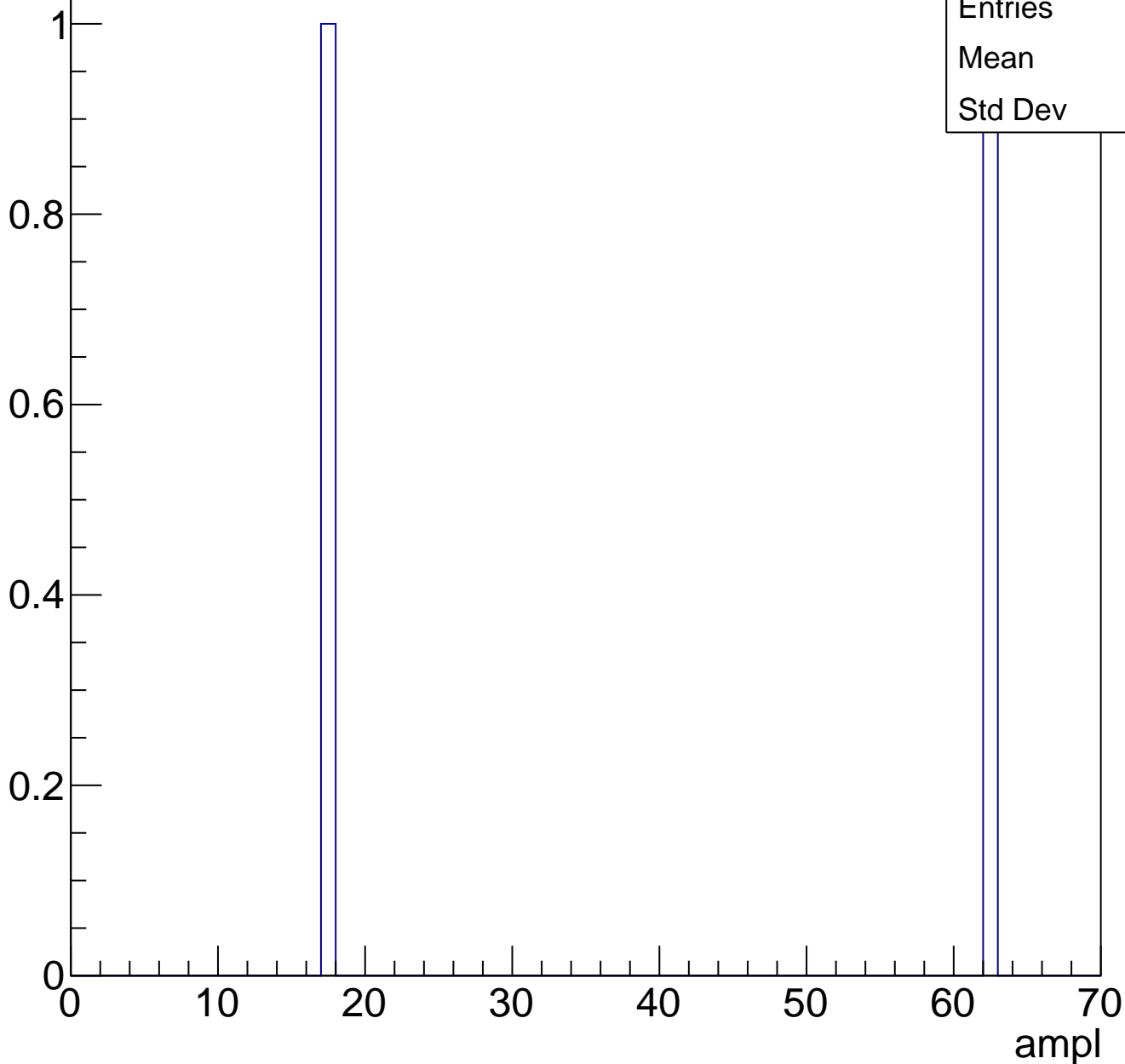




# B1L102S, U16-ch44, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch45, adc0

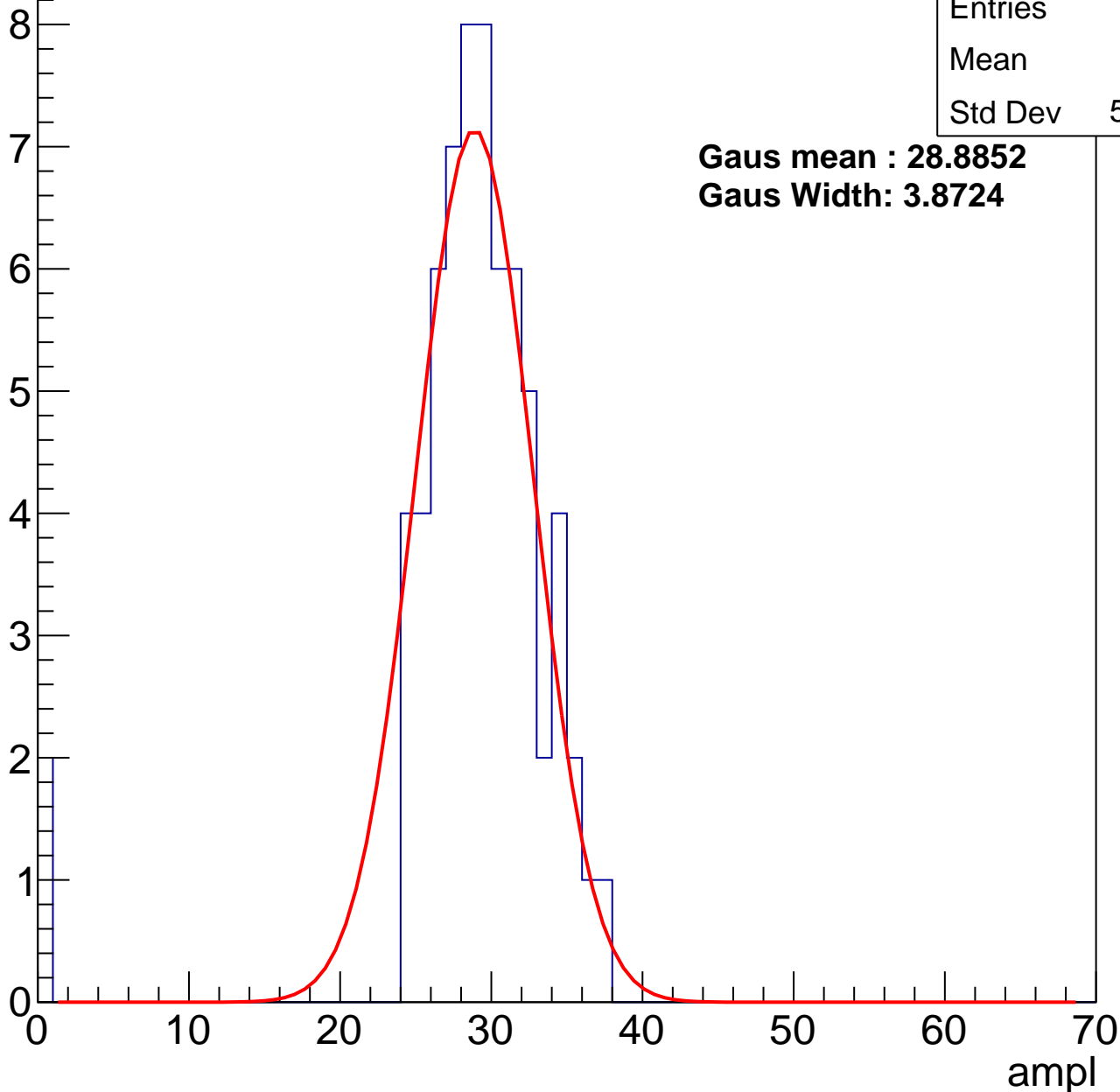
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	28.3
Std Dev	5.898

**Gaus mean : 28.8852**

**Gaus Width: 3.8724**



# B1L102S, U16-ch45, adc1

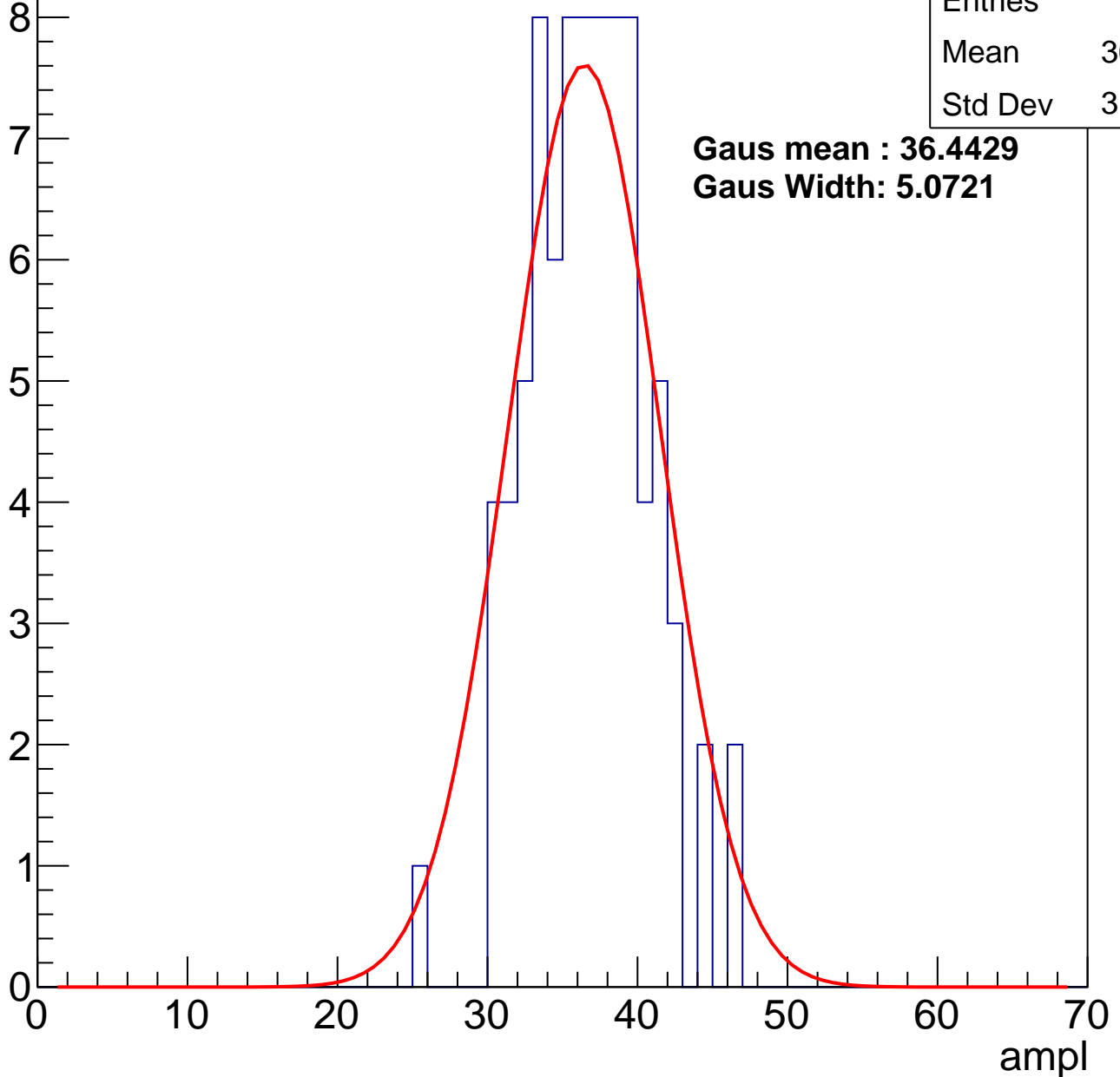
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	36.29
Std Dev	3.902

**Gaus mean : 36.4429**

**Gaus Width: 5.0721**



# B1L102S, U16-ch45, adc2

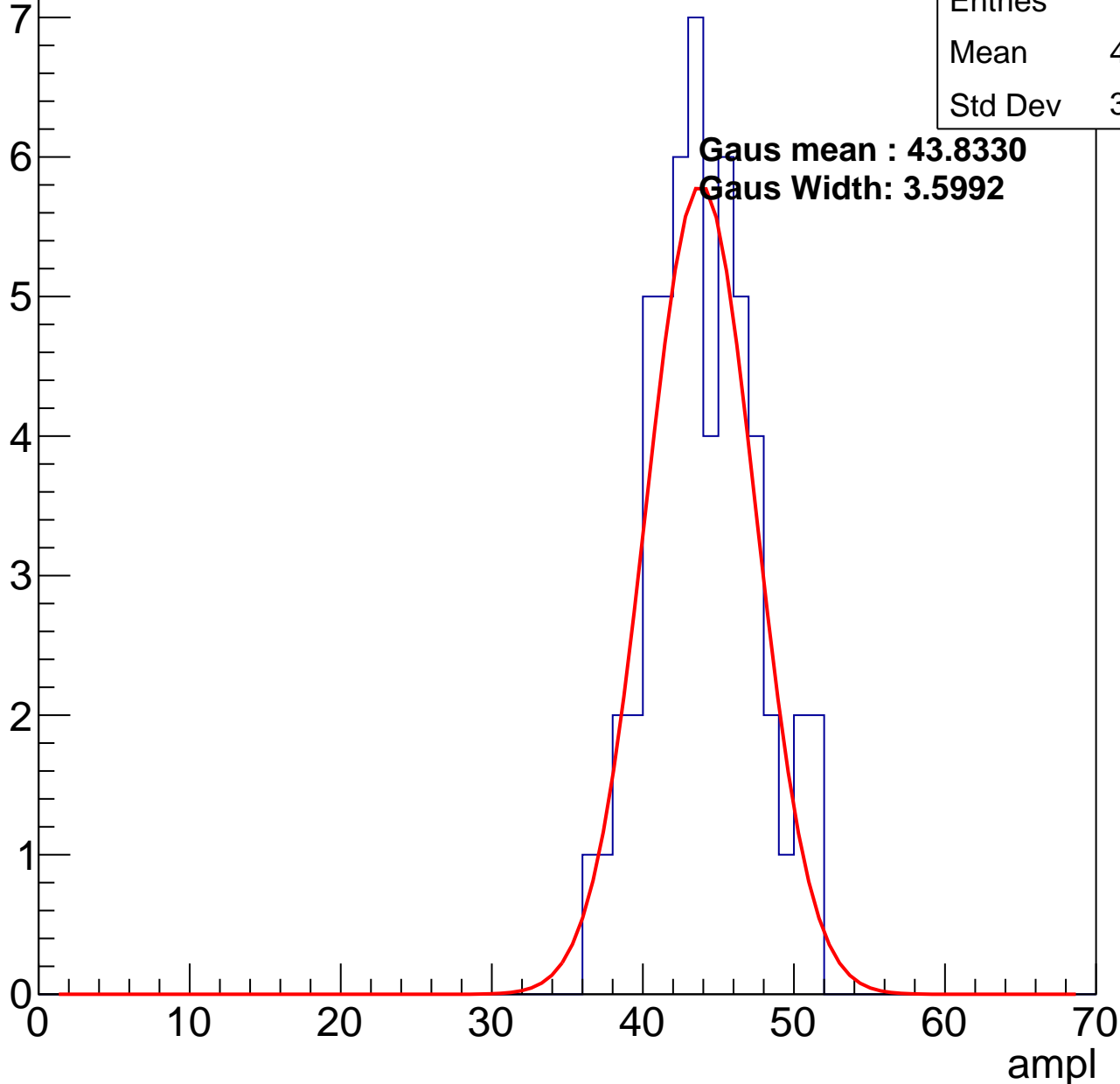
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	43.56
Std Dev	3.489

**Gaus mean : 43.8330**

**Gaus Width: 3.5992**

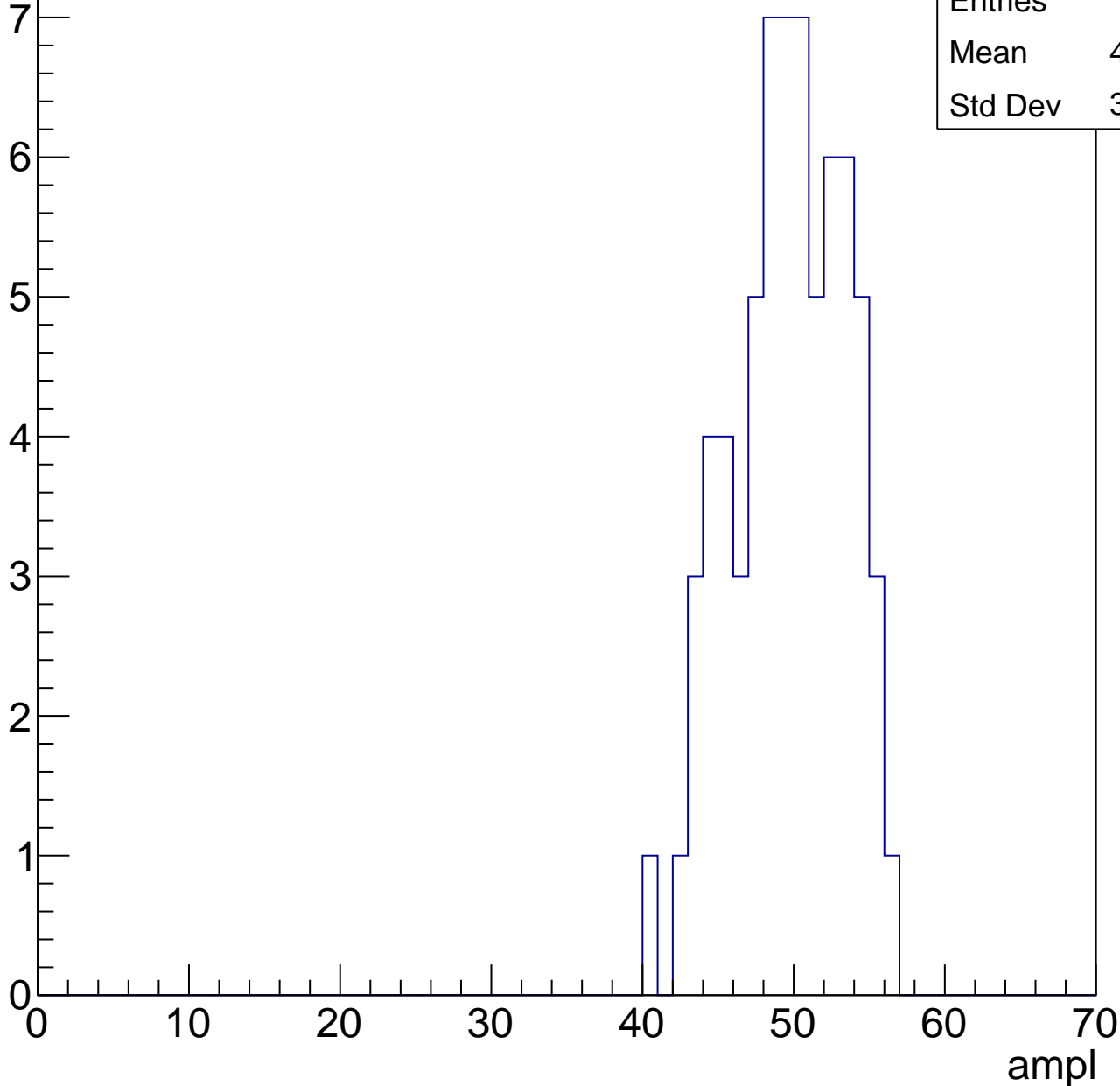


# B1L102S, U16-ch45, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	49.19
Std Dev	3.663

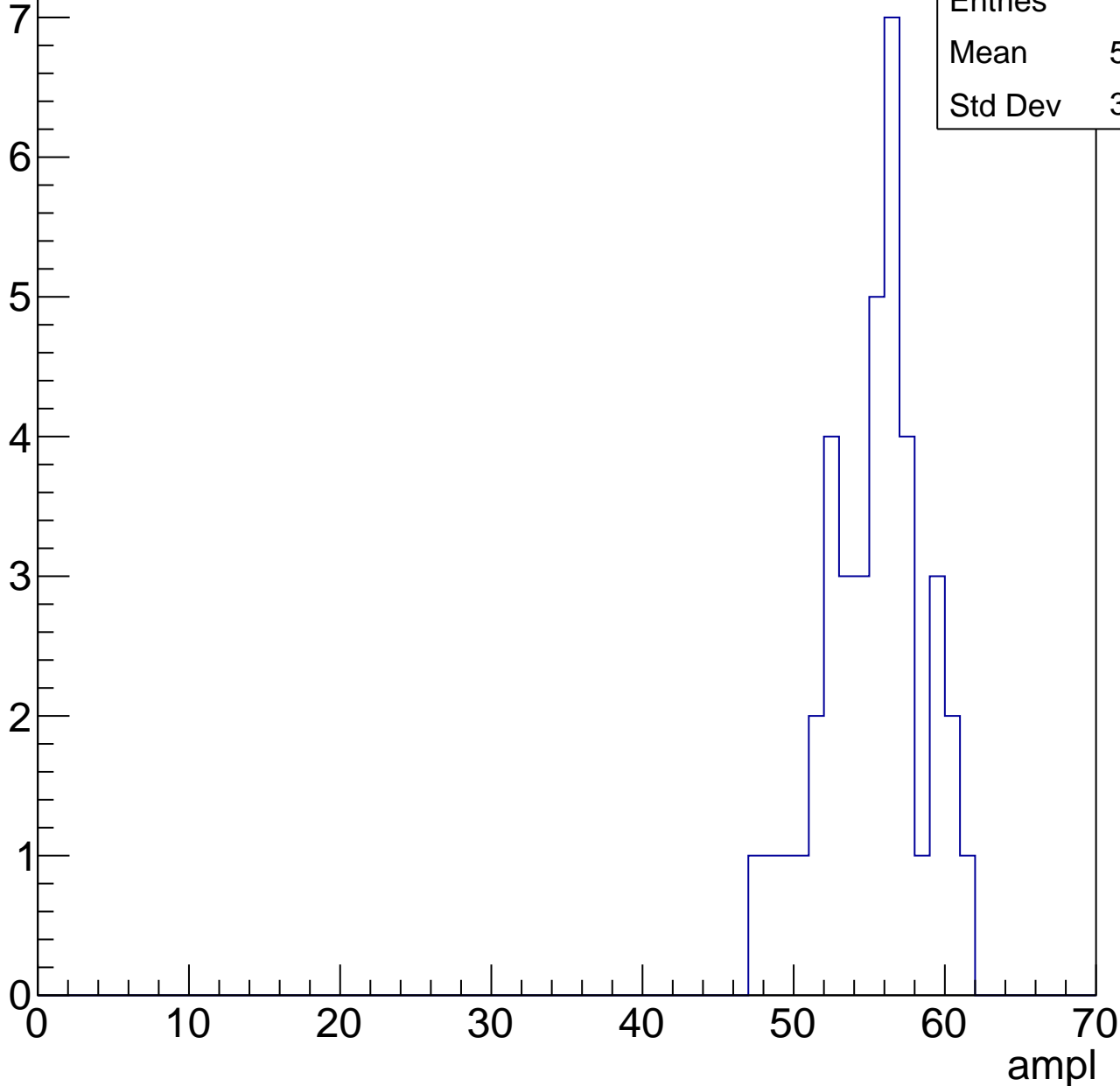


# B1L102S, U16-ch45, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

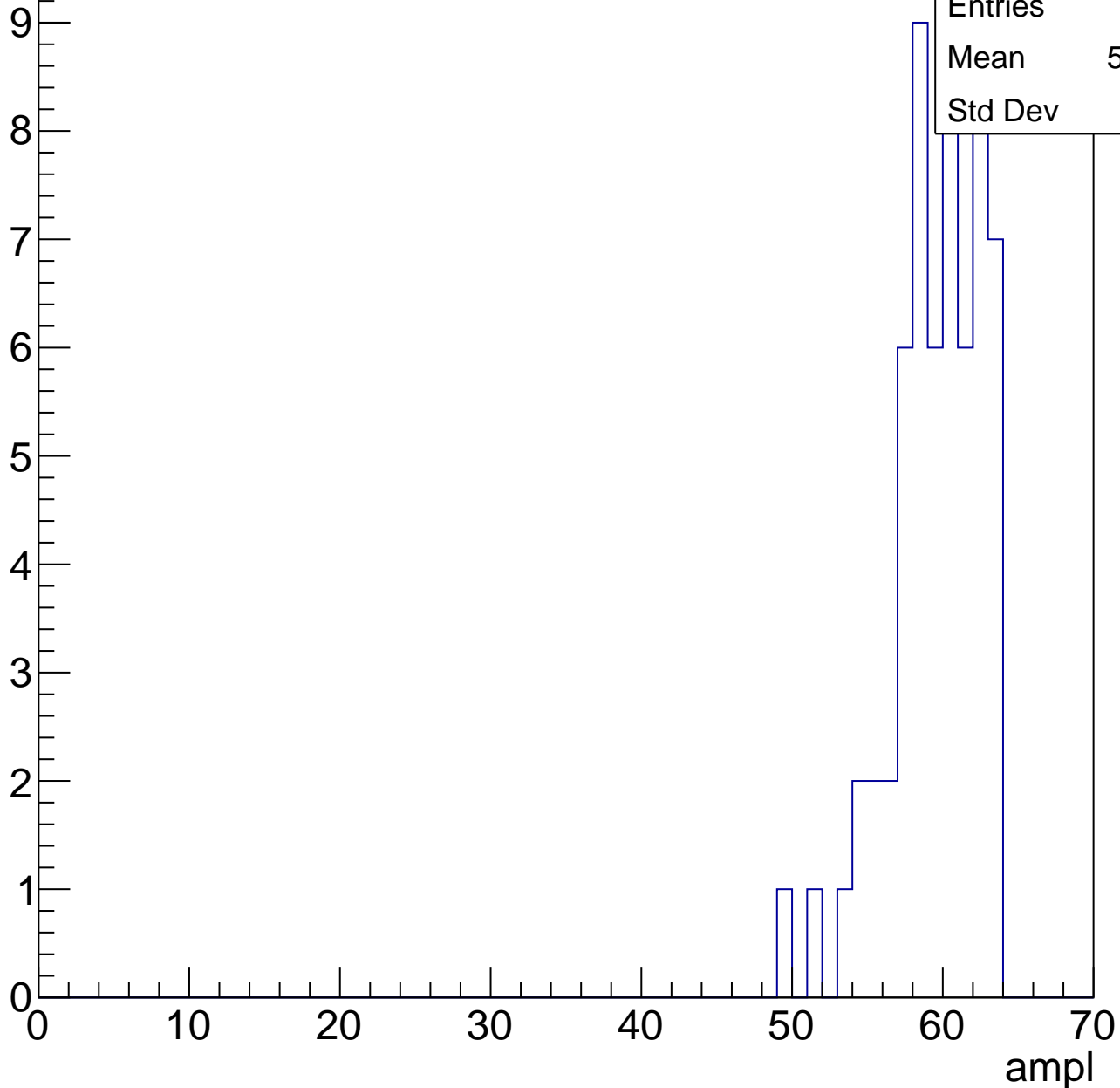
Entries	39
Mean	54.77
Std Dev	3.285



# B1L102S, U16-ch45, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

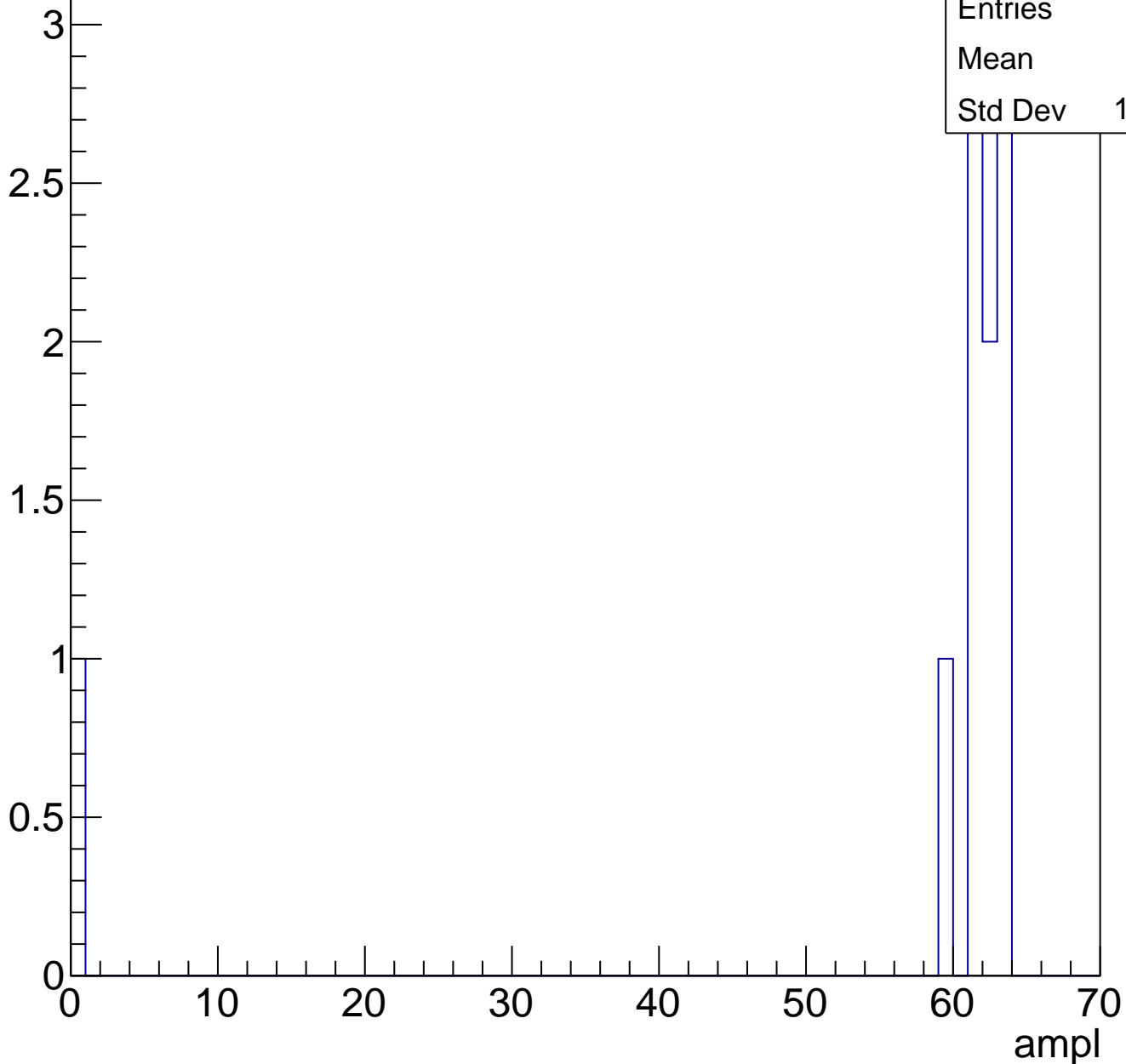
Entry



# B1L102S, U16-ch45, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch45, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch46, adc0

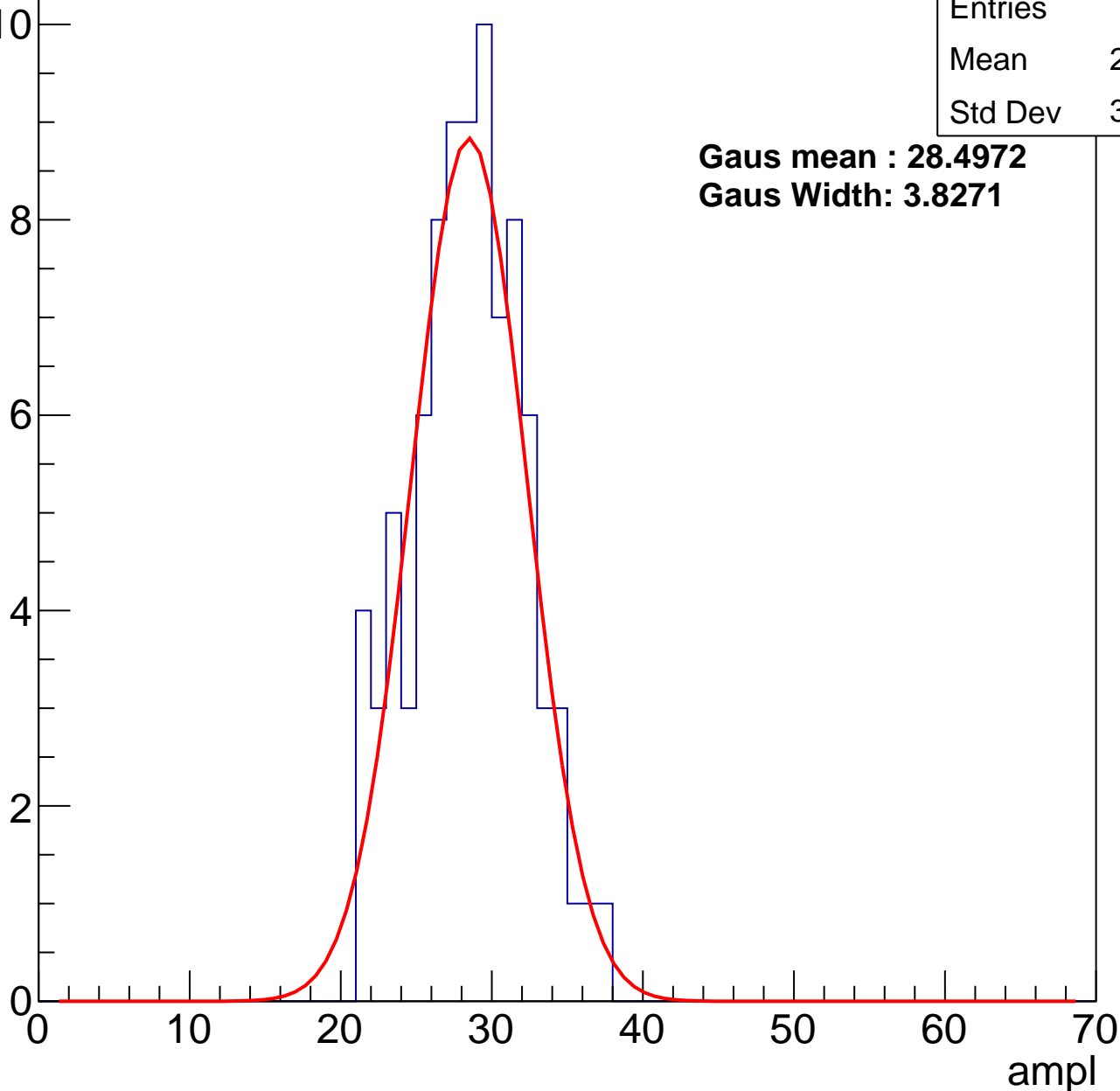
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	87
Mean	28.03
Std Dev	3.643

**Gaus mean : 28.4972**

**Gaus Width: 3.8271**



# B1L102S, U16-ch46, adc1

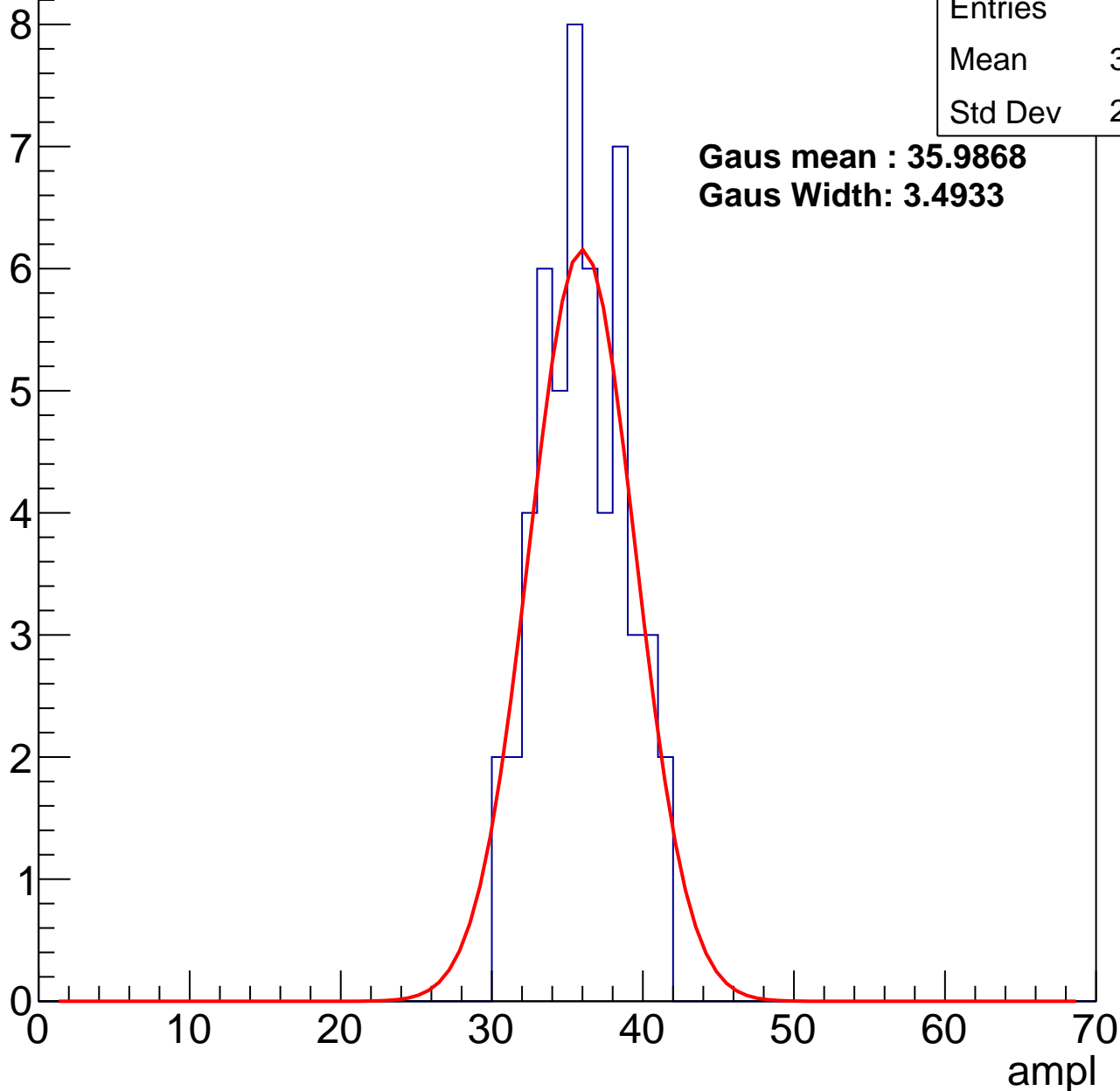
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	35.52
Std Dev	2.818

**Gaus mean : 35.9868**

**Gaus Width: 3.4933**



# B1L102S, U16-ch46, adc2

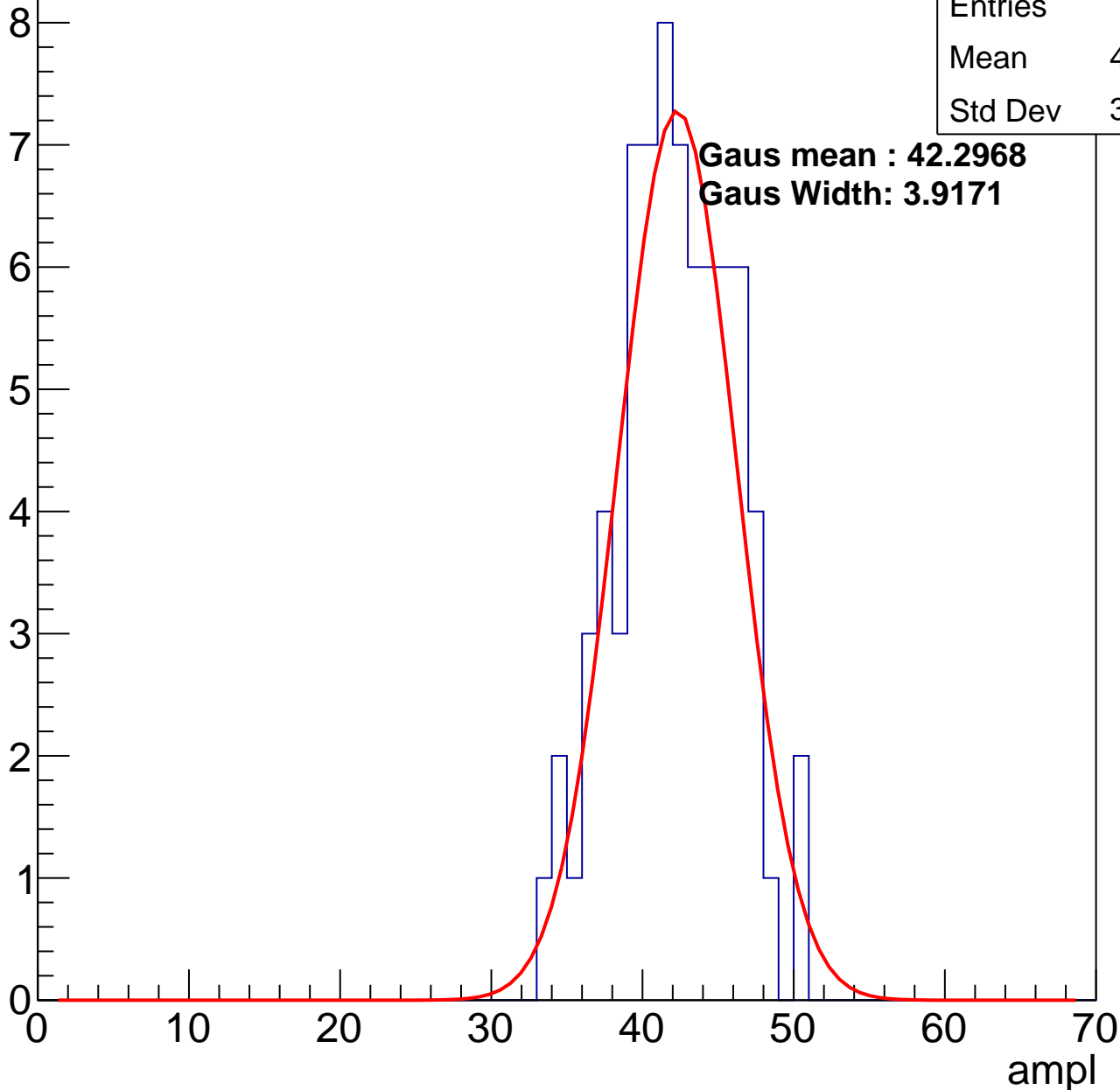
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	41.69
Std Dev	3.767

**Gaus mean : 42.2968**

**Gaus Width: 3.9171**

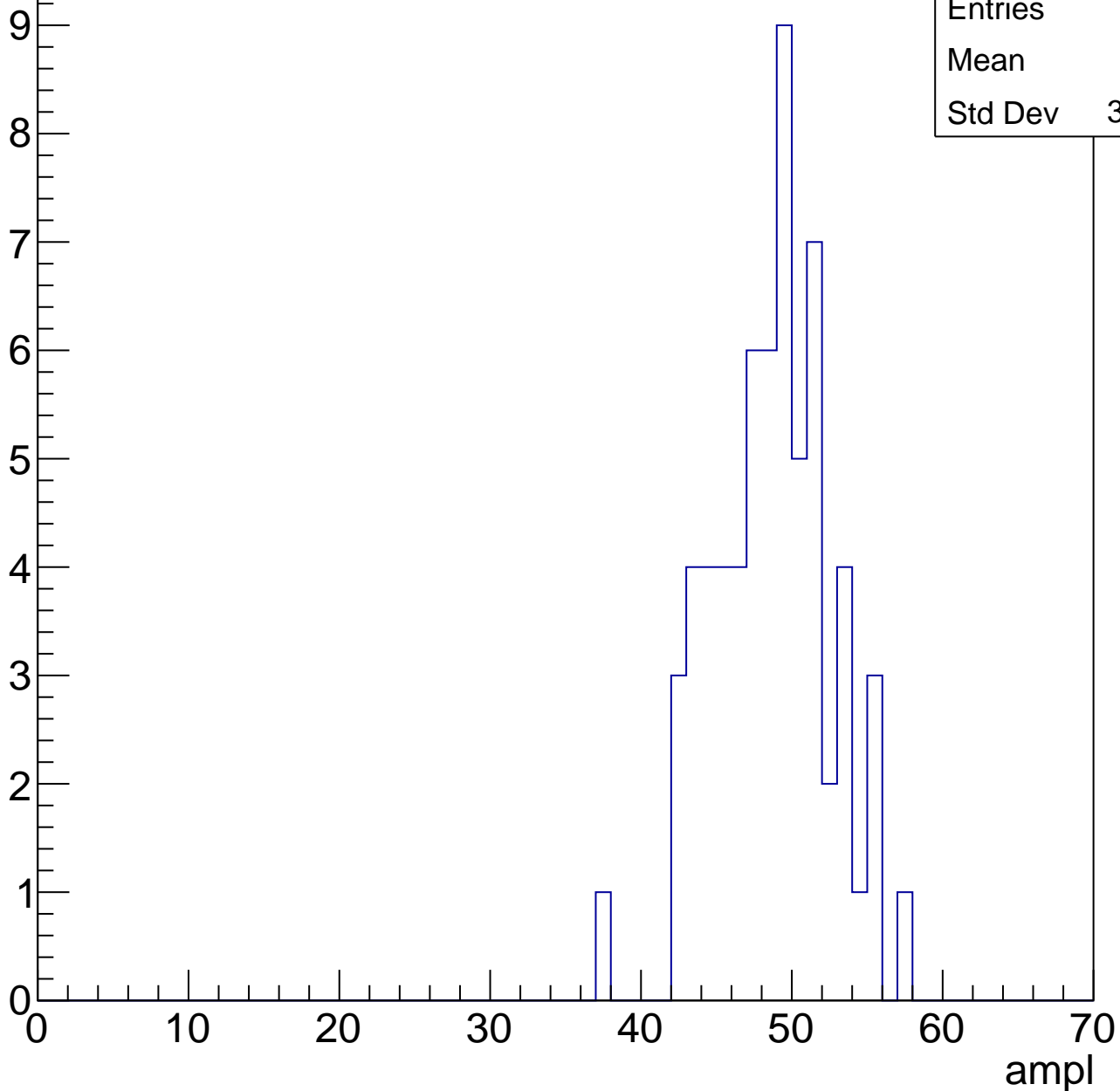


# B1L102S, U16-ch46, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

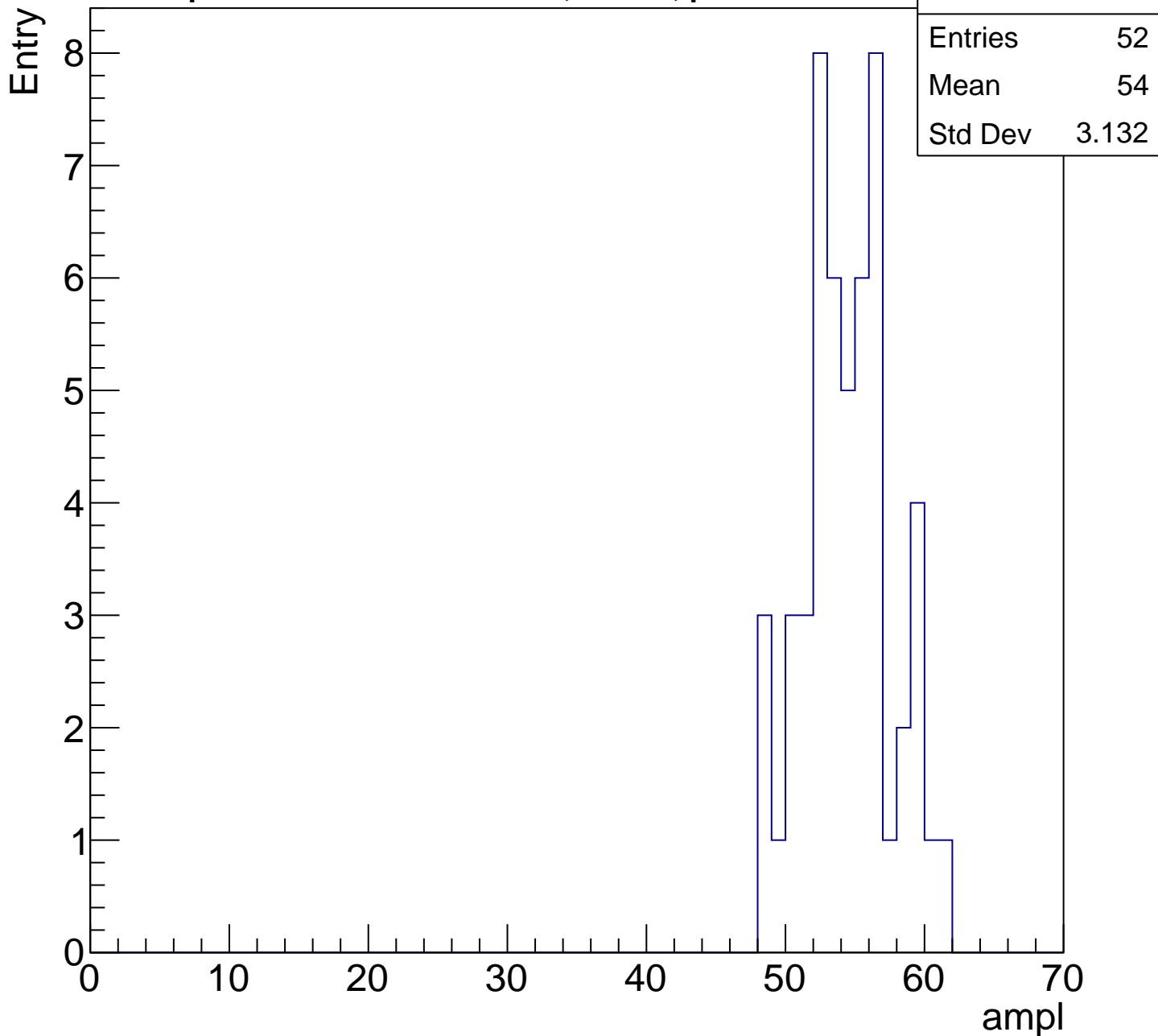
Entry

Entries	64
Mean	48.2
Std Dev	3.825



# B1L102S, U16-ch46, adc4

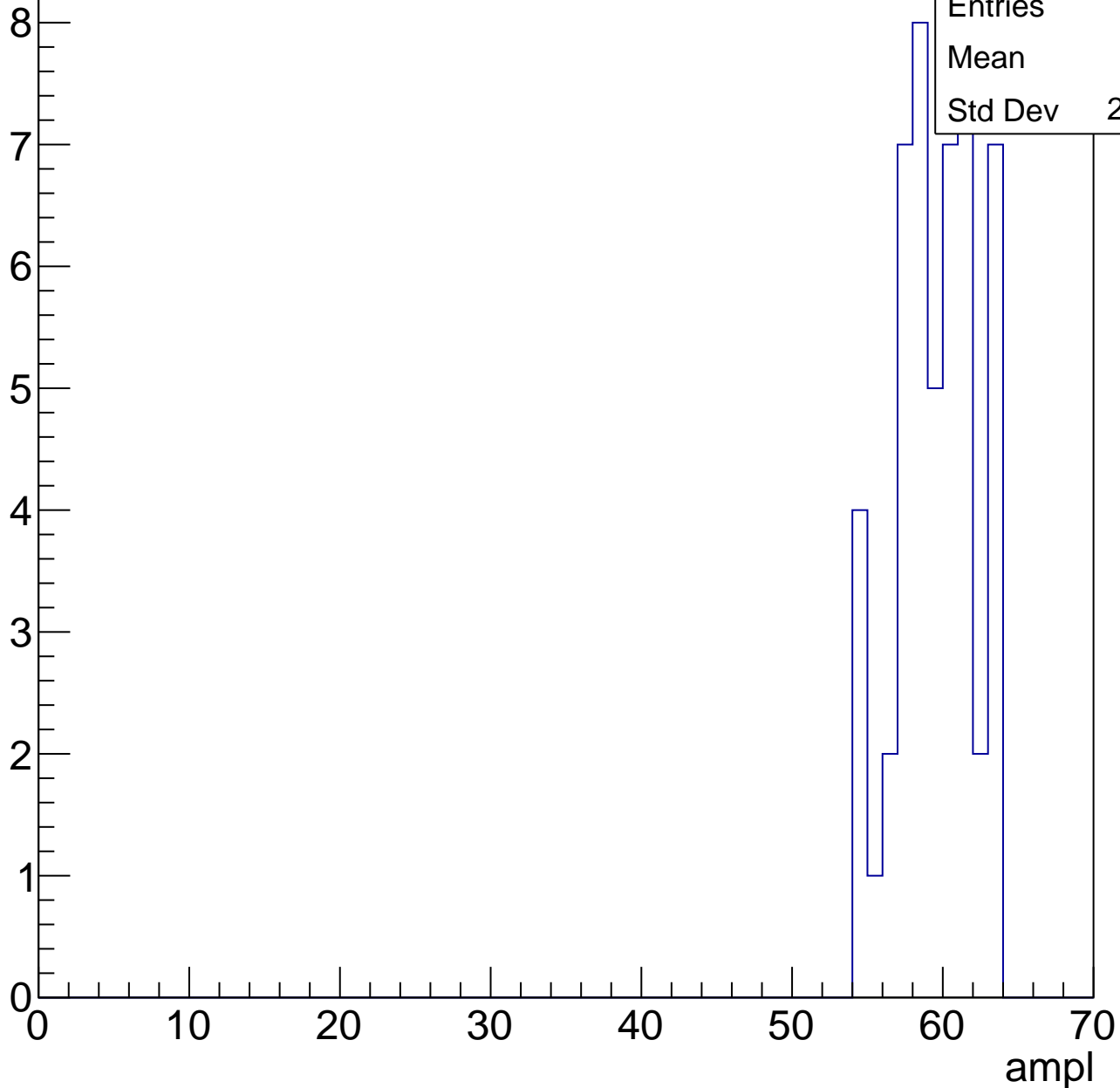
calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U16-ch46, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

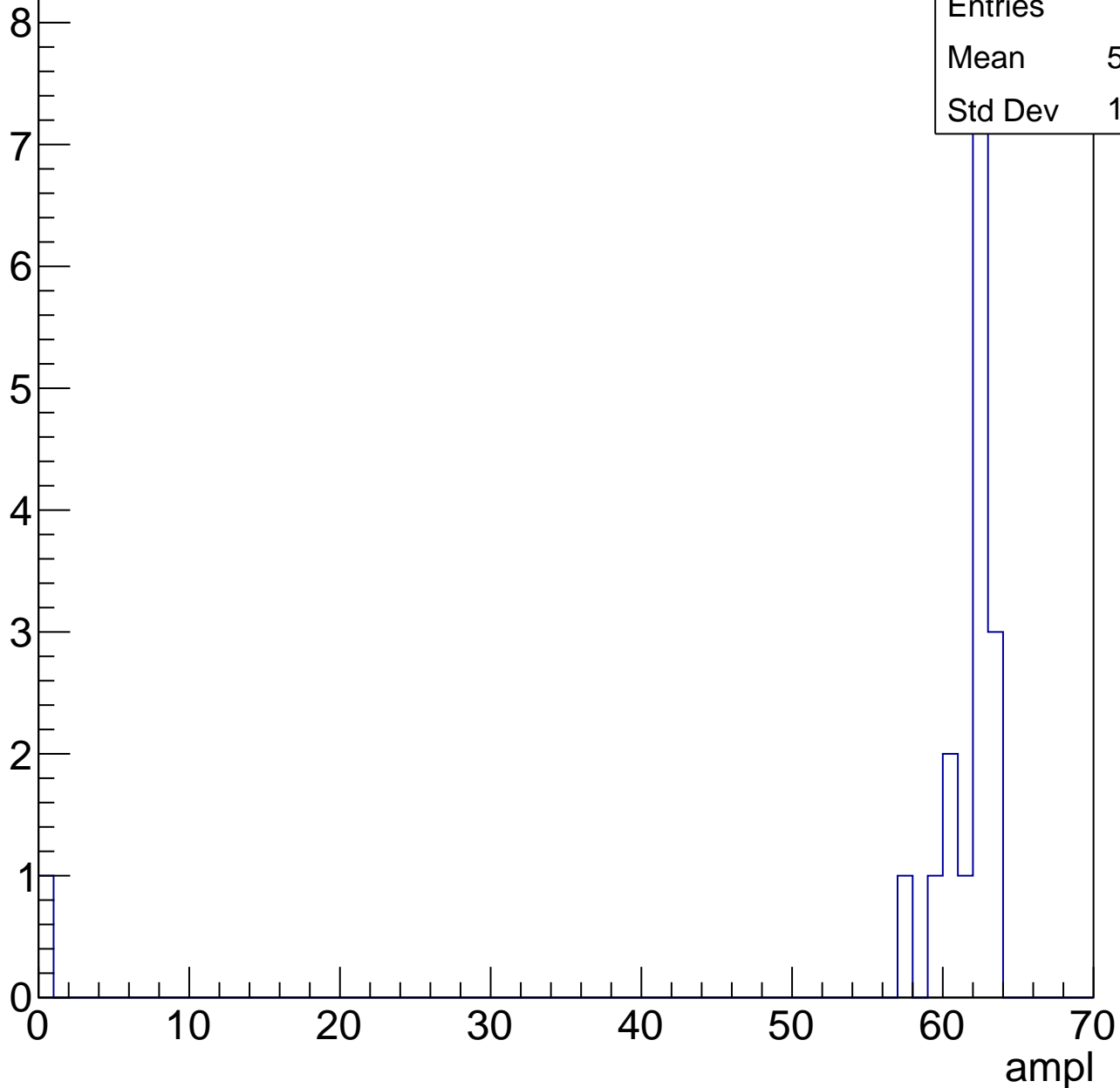


# B1L102S, U16-ch46, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	17
Mean	57.76
Std Dev	14.52

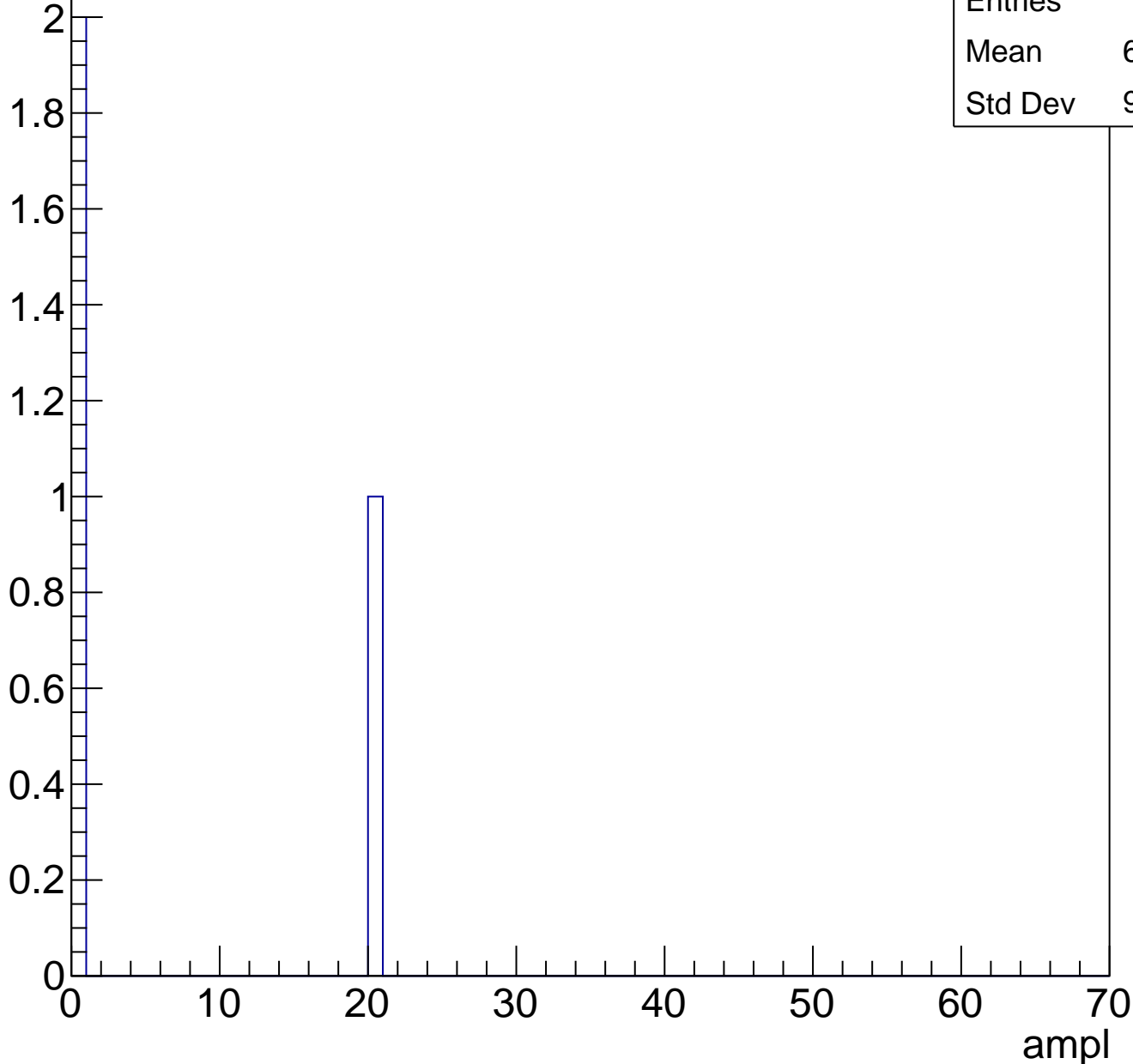




# B1L102S, U16-ch46, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch47, adc0

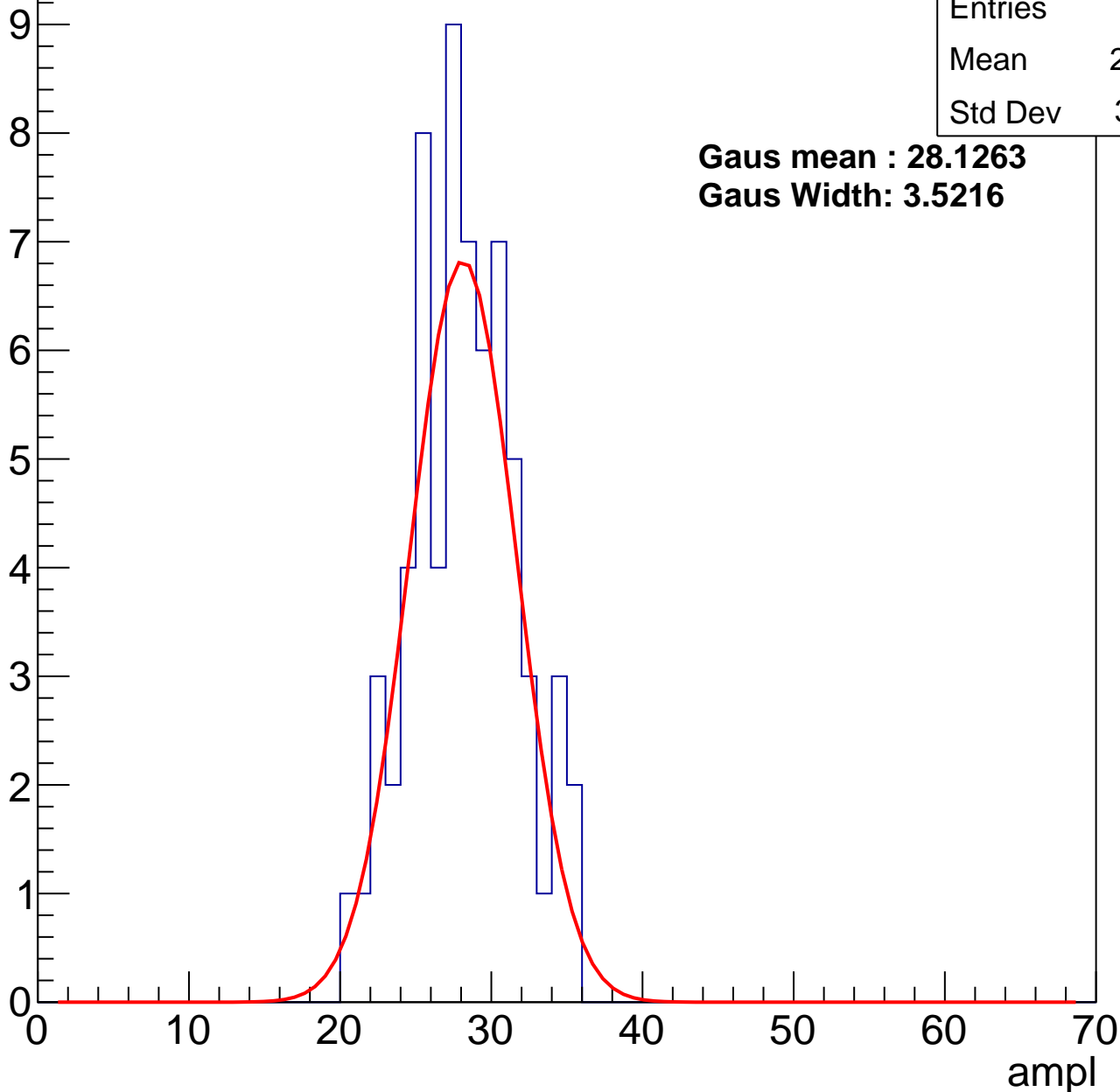
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	27.76
Std Dev	3.451

**Gaus mean : 28.1263**

**Gaus Width: 3.5216**



# B1L102S, U16-ch47, adc1

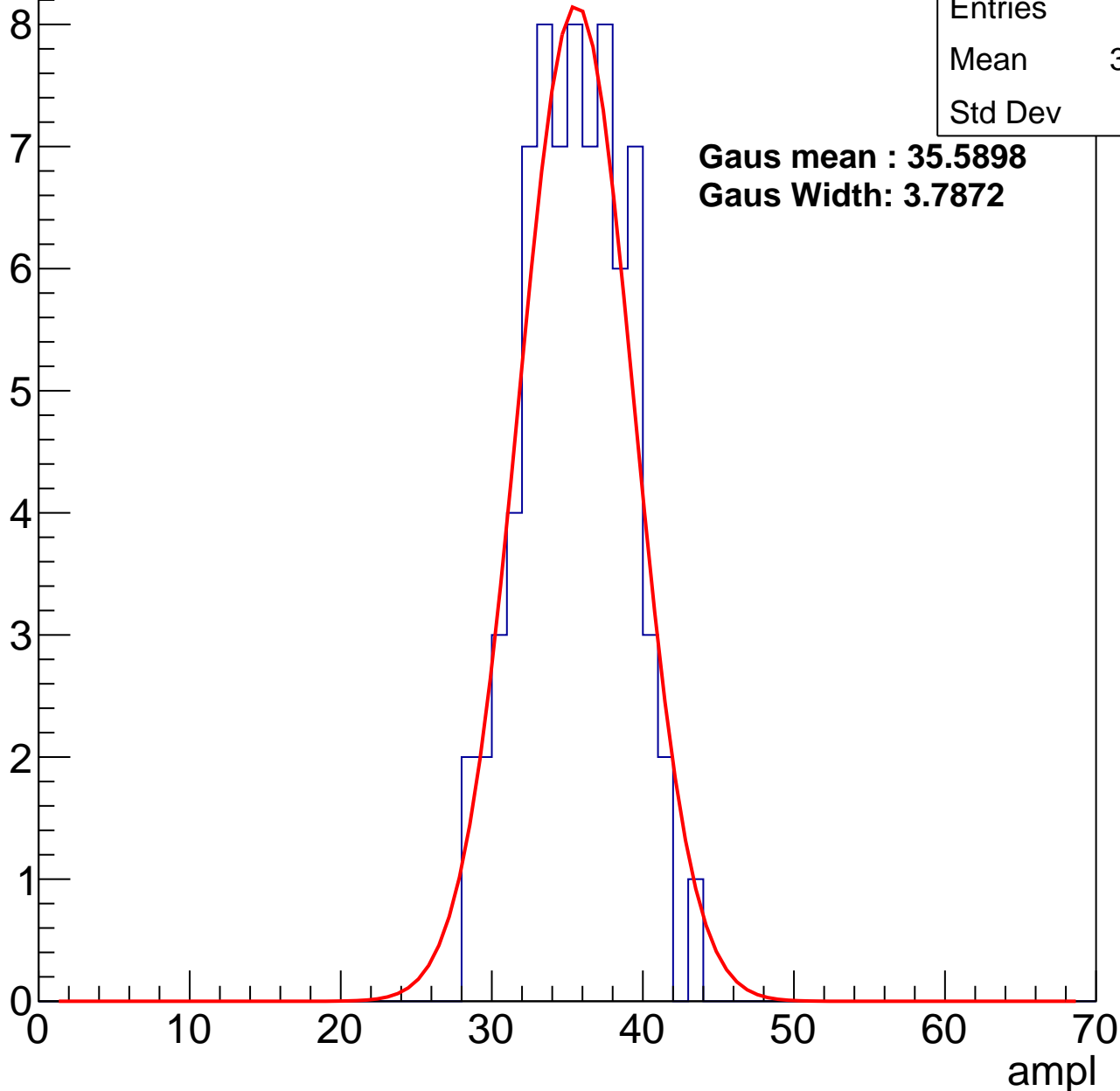
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	35.04
Std Dev	3.32

**Gaus mean : 35.5898**

**Gaus Width: 3.7872**



# B1L102S, U16-ch47, adc2

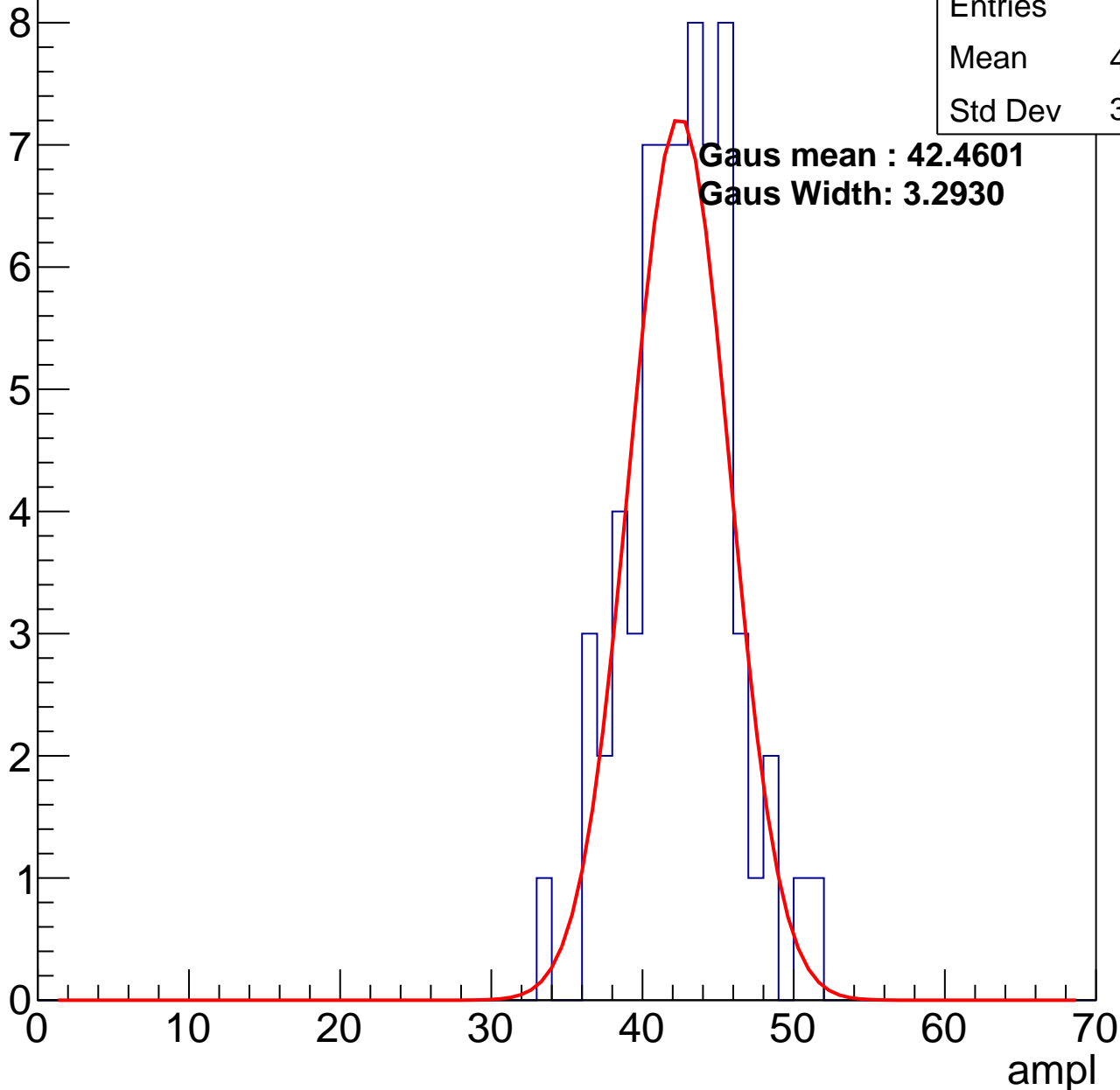
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	42.14
Std Dev	3.423

**Gaus mean : 42.4601**

**Gaus Width: 3.2930**

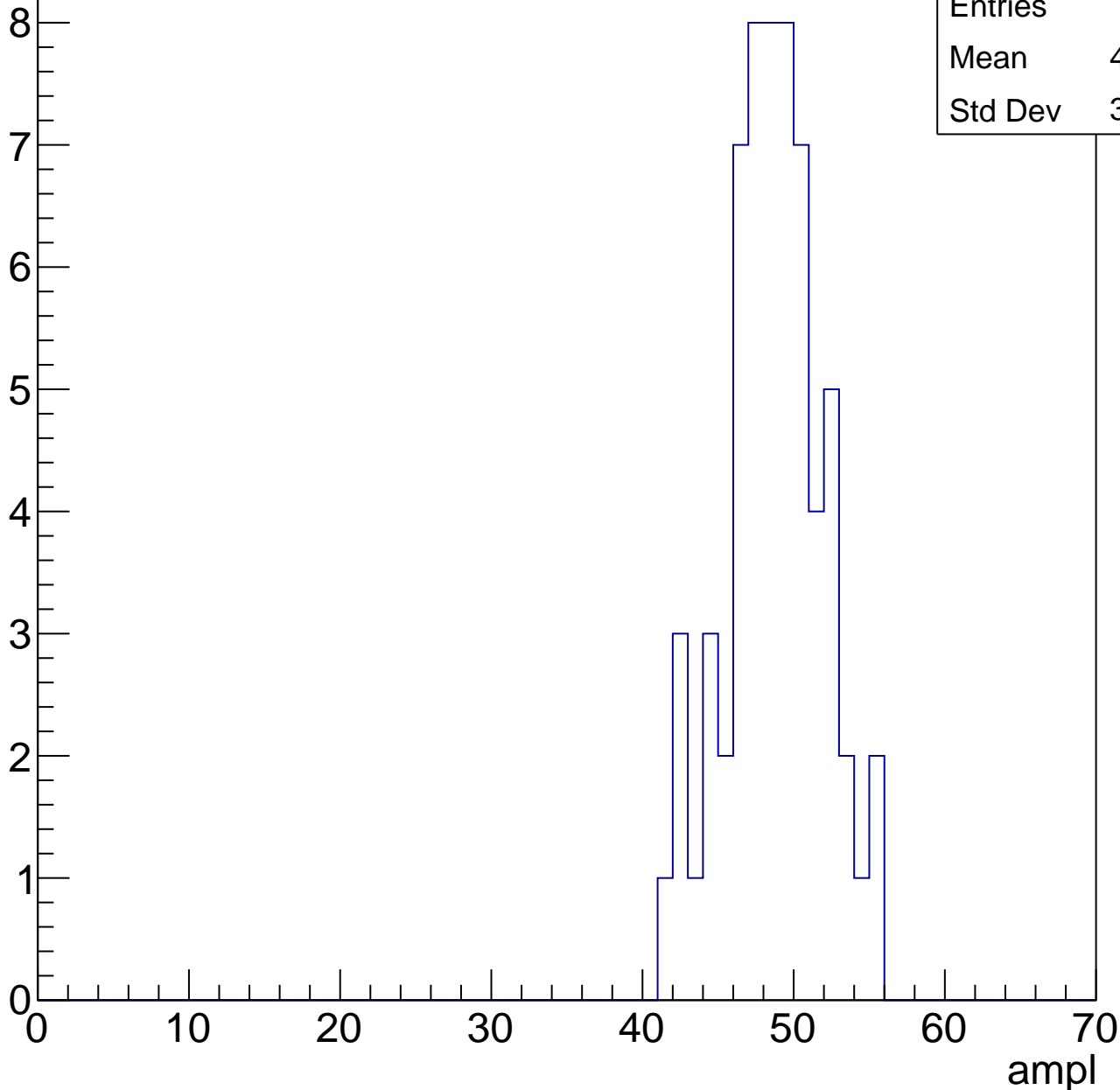


# B1L102S, U16-ch47, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	48.23
Std Dev	3.154

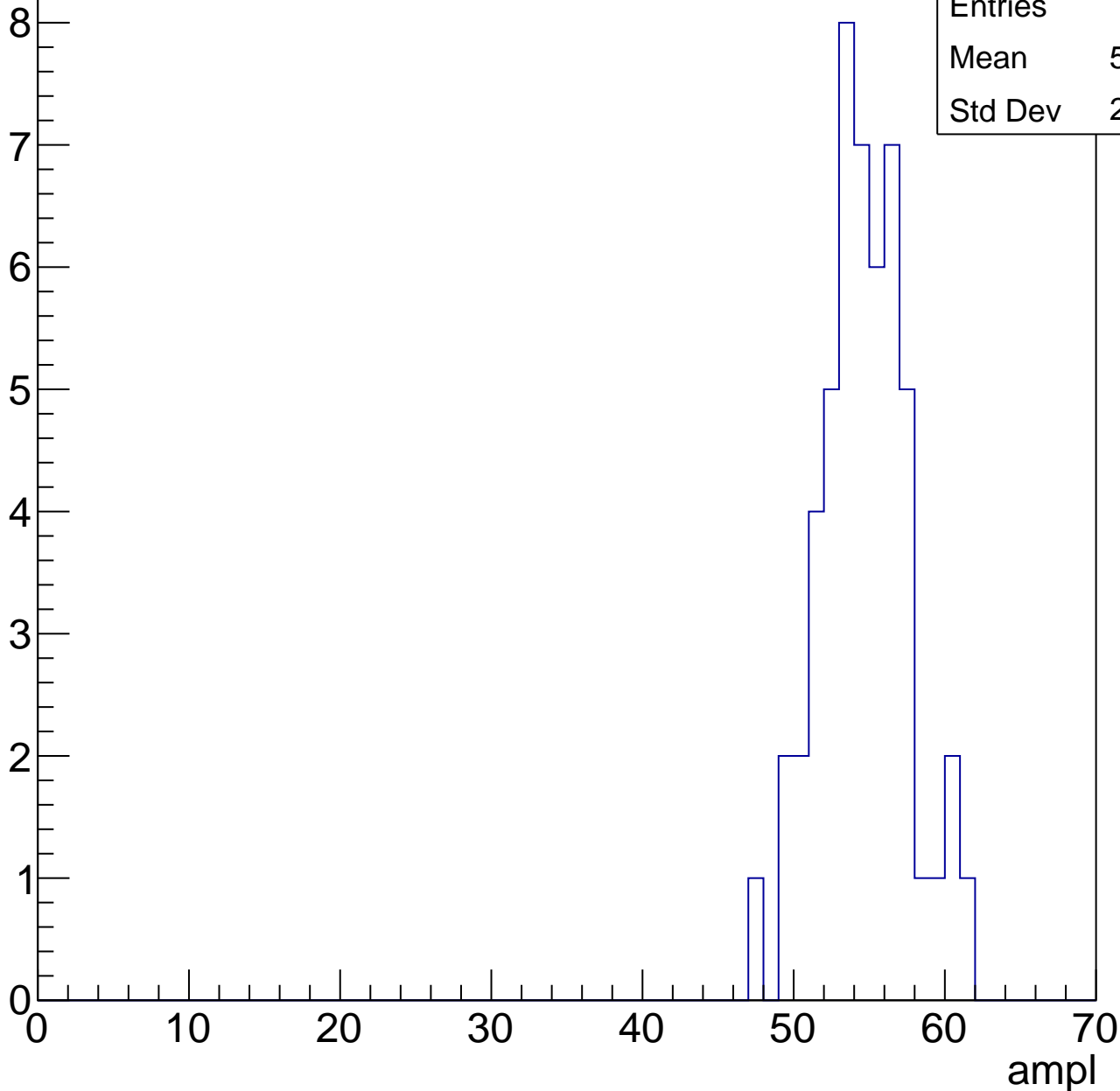


# B1L102S, U16-ch47, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	54.15
Std Dev	2.892

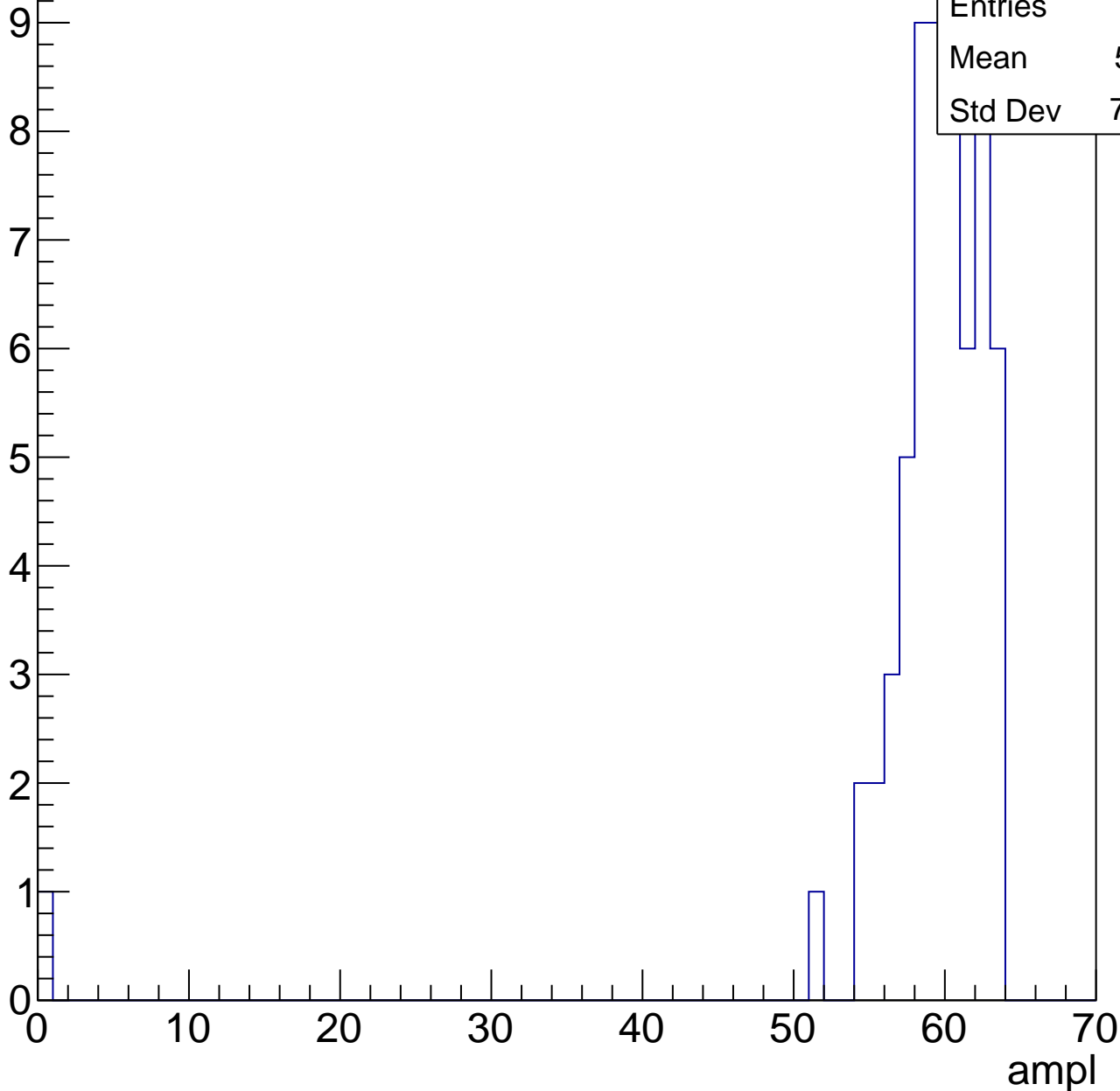


# B1L102S, U16-ch47, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

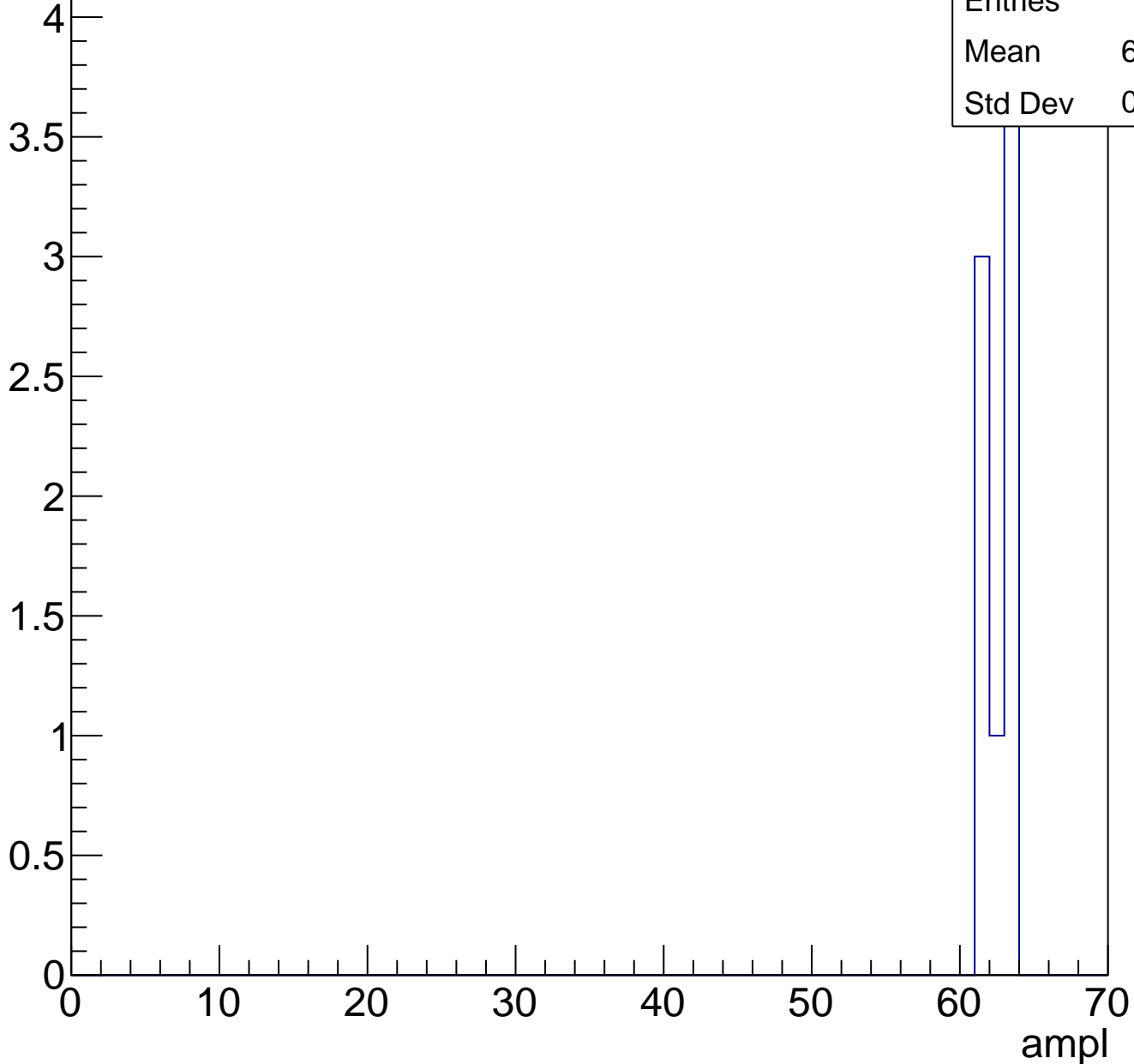
Entries	61
Mean	58.31
Std Dev	7.958



# B1L102S, U16-ch47, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch47, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch48, adc0

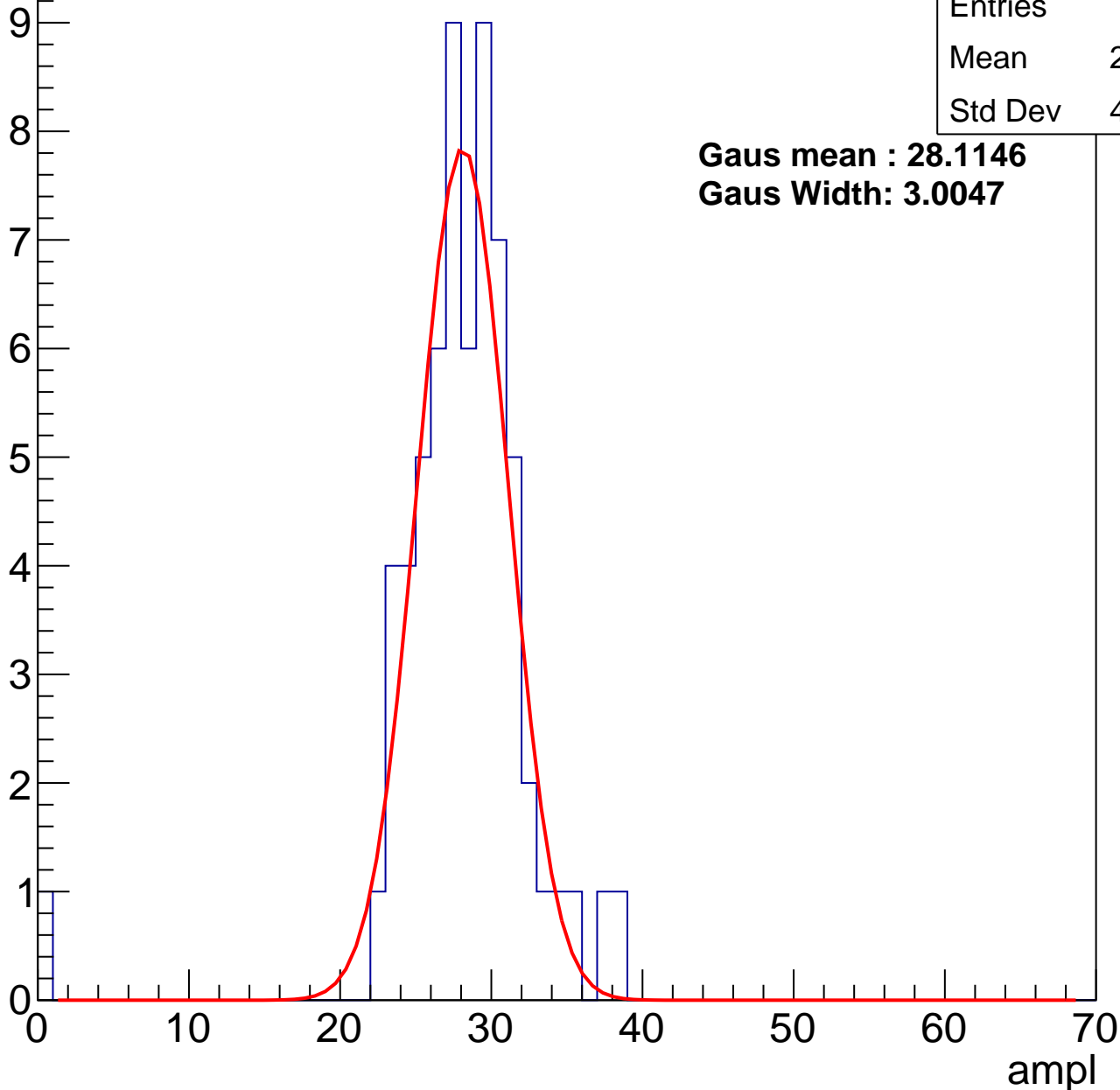
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	27.64
Std Dev	4.774

**Gaus mean : 28.1146**

**Gaus Width: 3.0047**



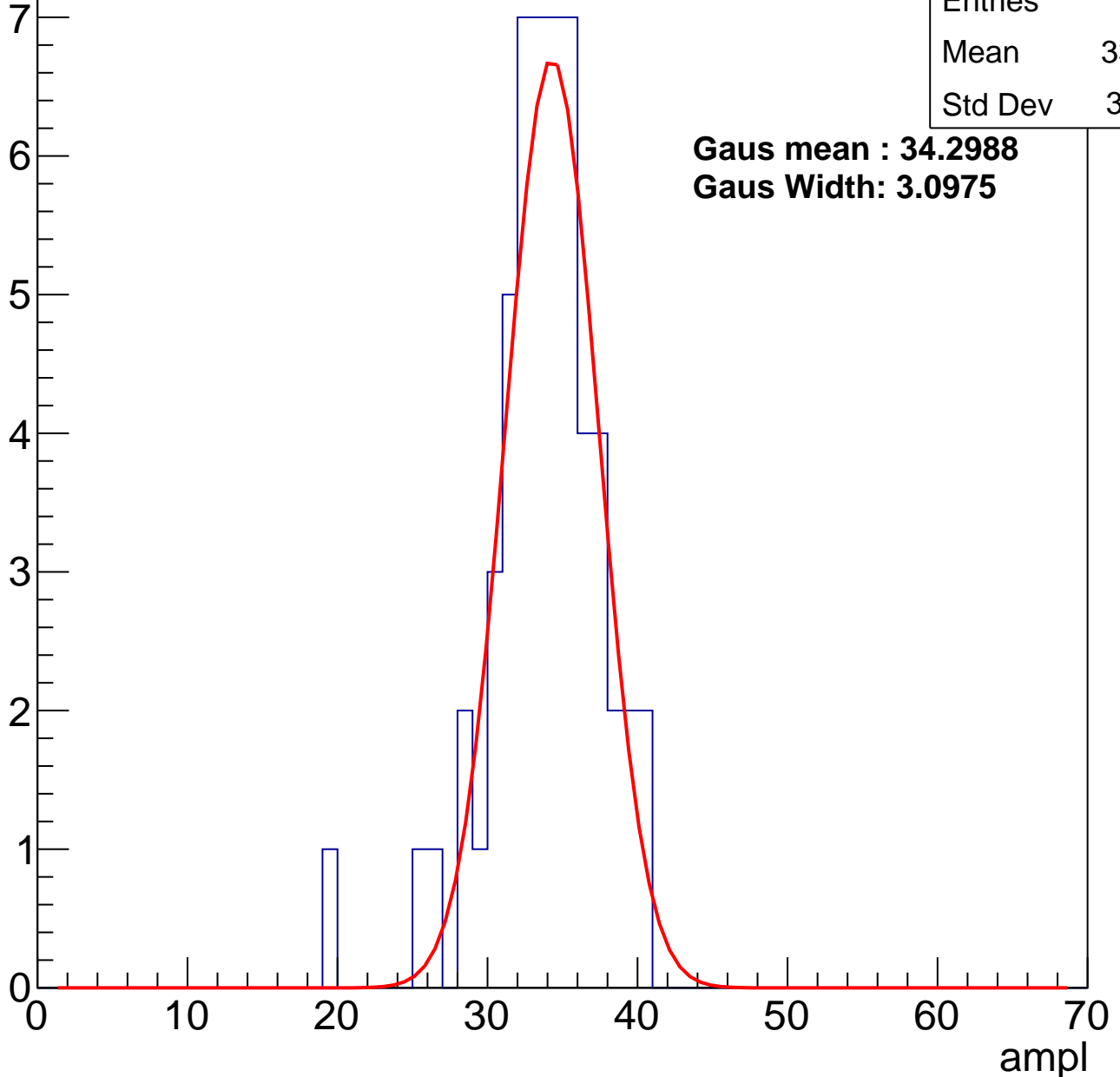
# B1L102S, U16-ch48, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	33.29
Std Dev	3.731

**Gaus mean : 34.2988**  
**Gaus Width: 3.0975**



# B1L102S, U16-ch48, adc2

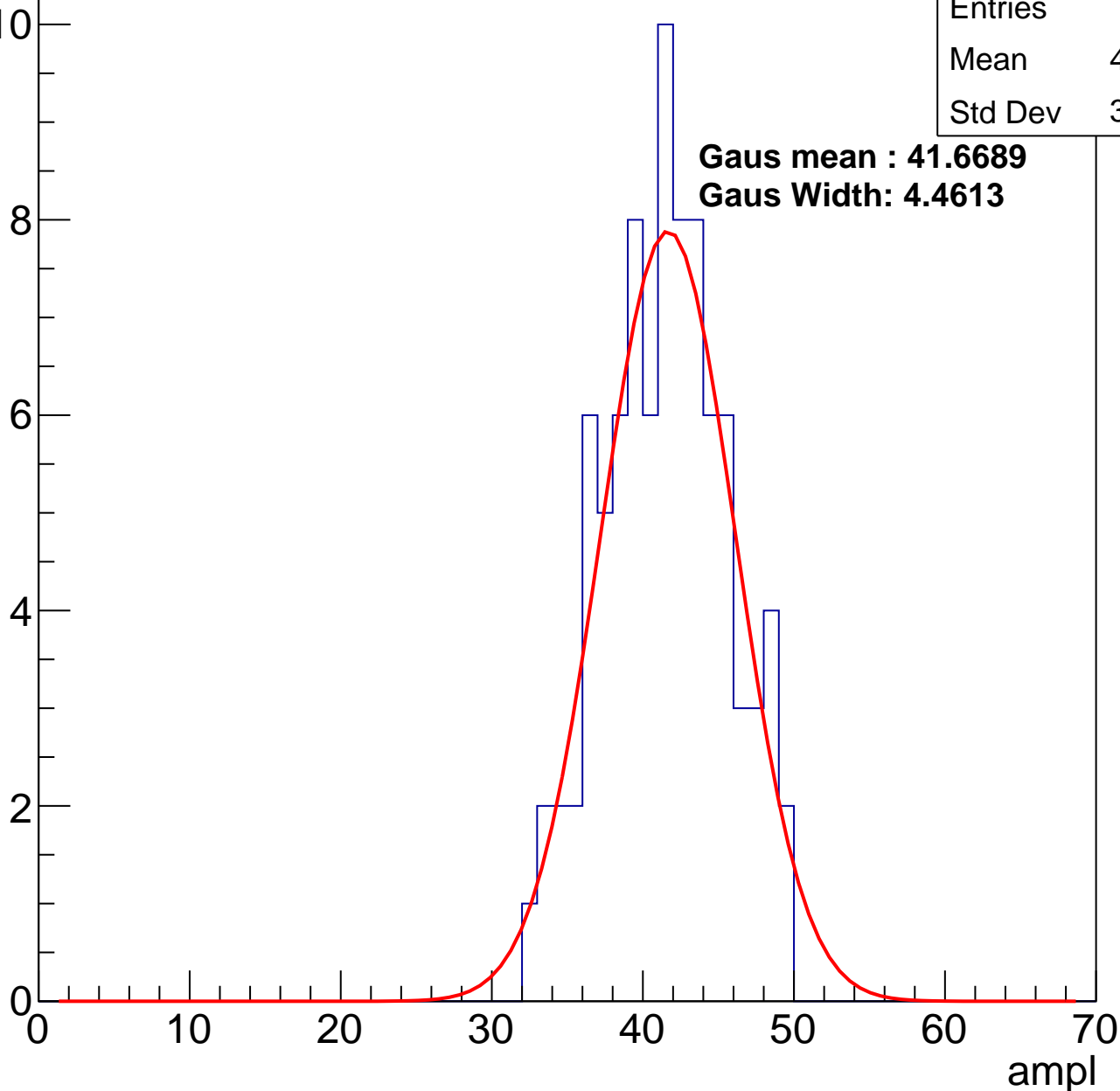
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	88
Mean	41.02
Std Dev	3.986

**Gaus mean : 41.6689**

**Gaus Width: 4.4613**

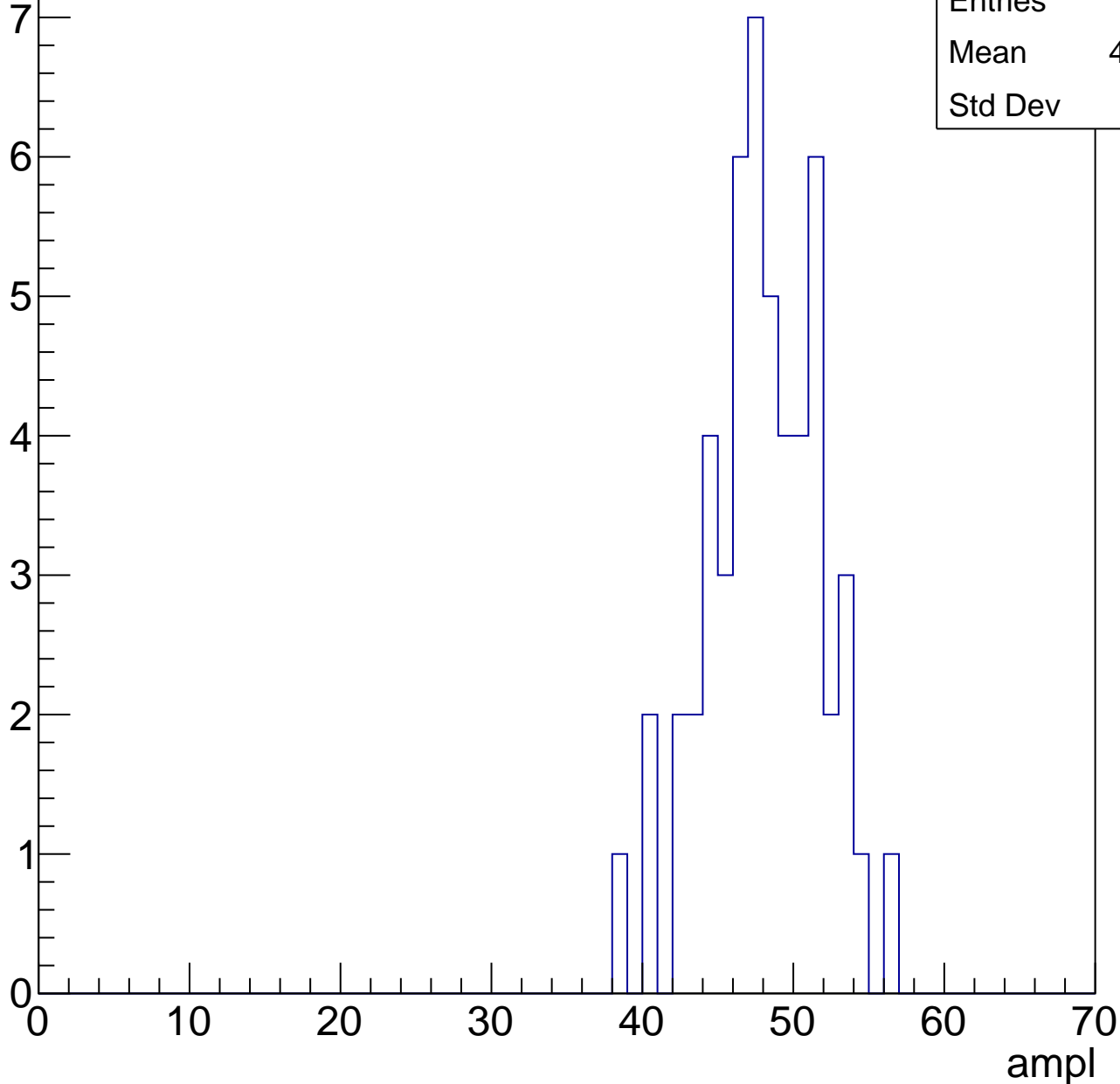


# B1L102S, U16-ch48, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	47.53
Std Dev	3.74

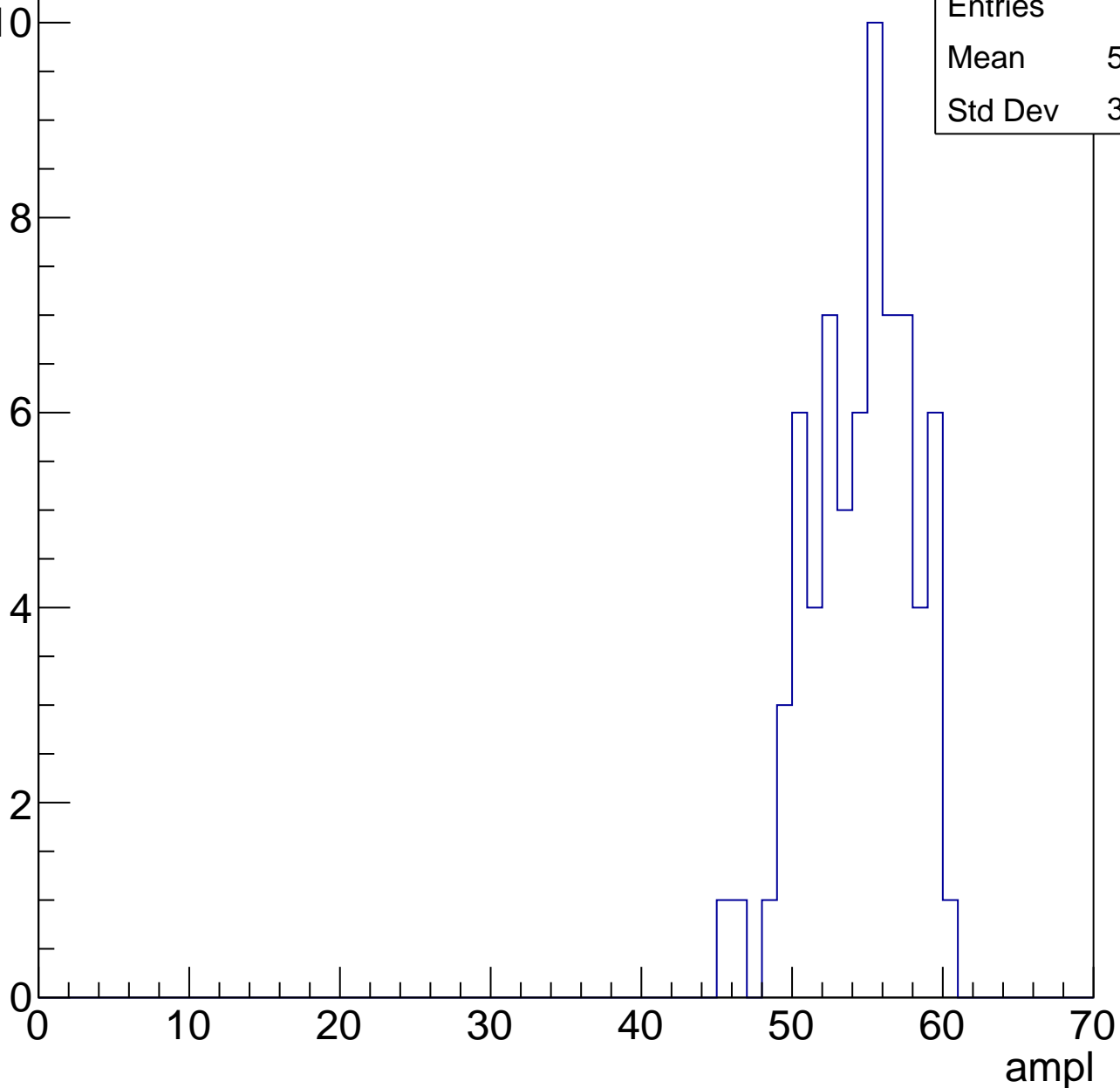


# B1L102S, U16-ch48, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	54.06
Std Dev	3.344



# B1L102S, U16-ch48, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

7

6

5

4

3

2

1

0

Entries	42
Mean	58.74
Std Dev	3.339

ampl

0

10

20

30

40

50

60

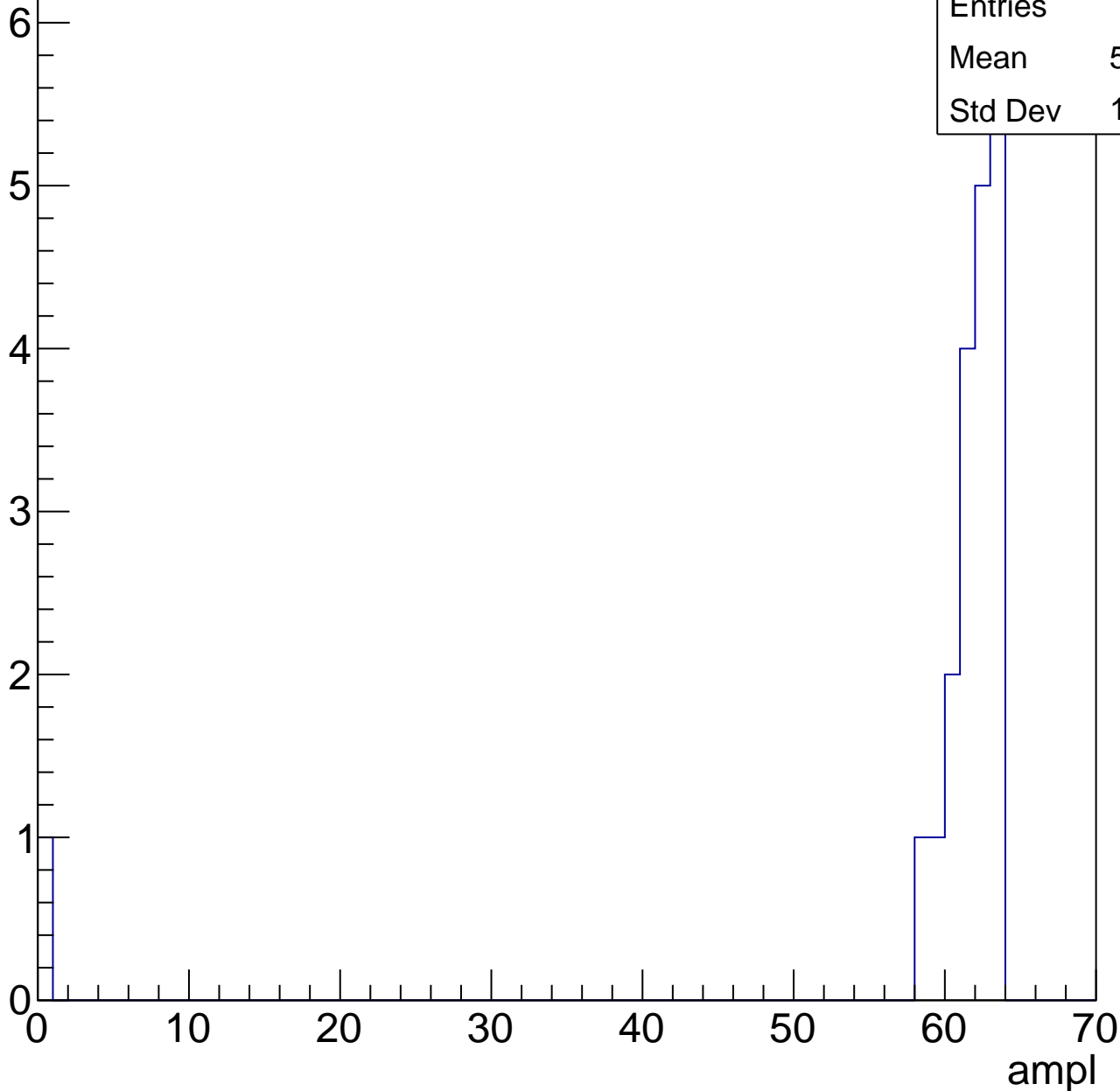
70

# B1L102S, U16-ch48, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	20
Mean	58.45
Std Dev	13.48





# B1L102S, U16-ch48, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch49, adc0

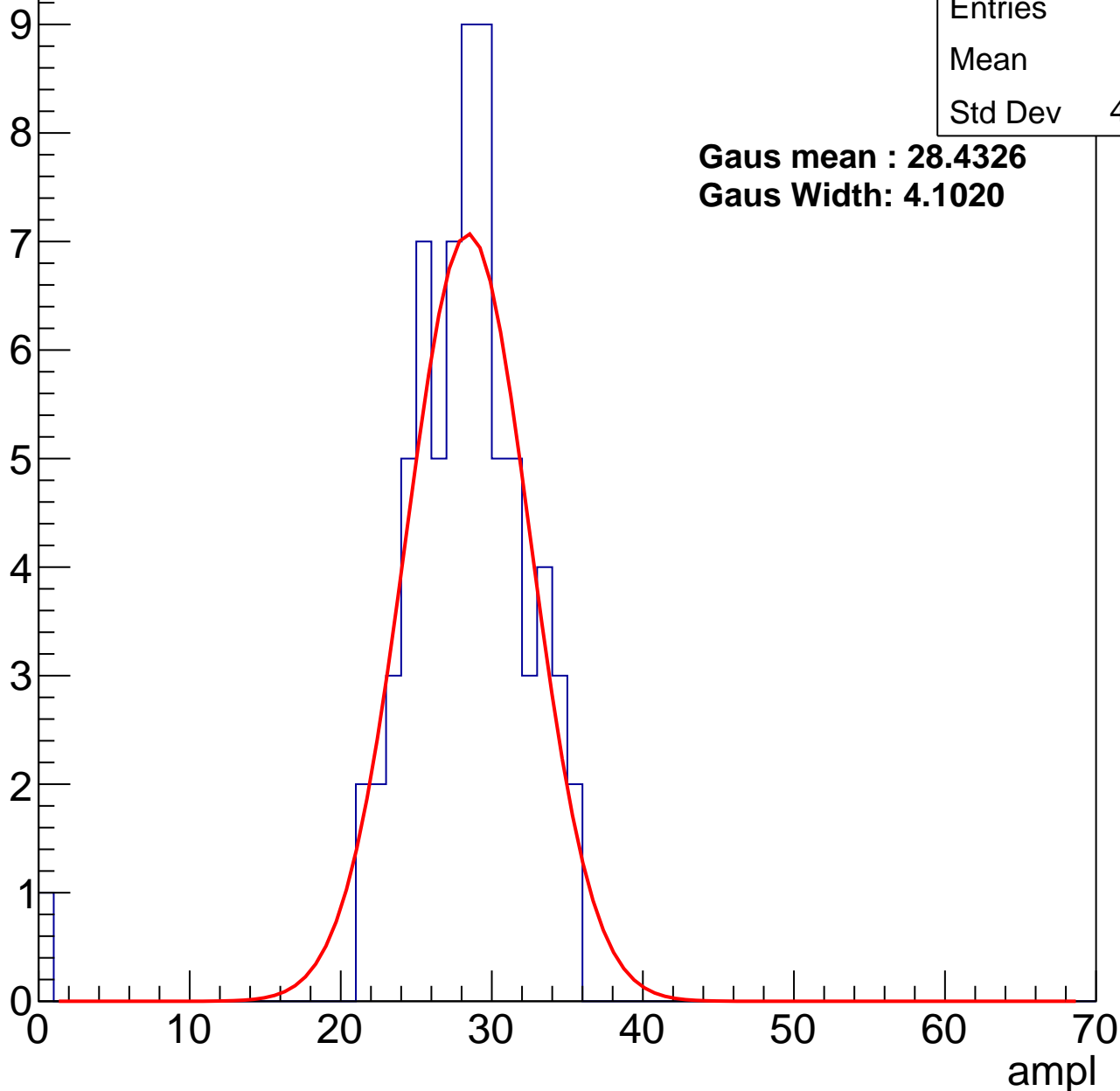
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	27.6
Std Dev	4.737

**Gaus mean : 28.4326**

**Gaus Width: 4.1020**



# B1L102S, U16-ch49, adc1

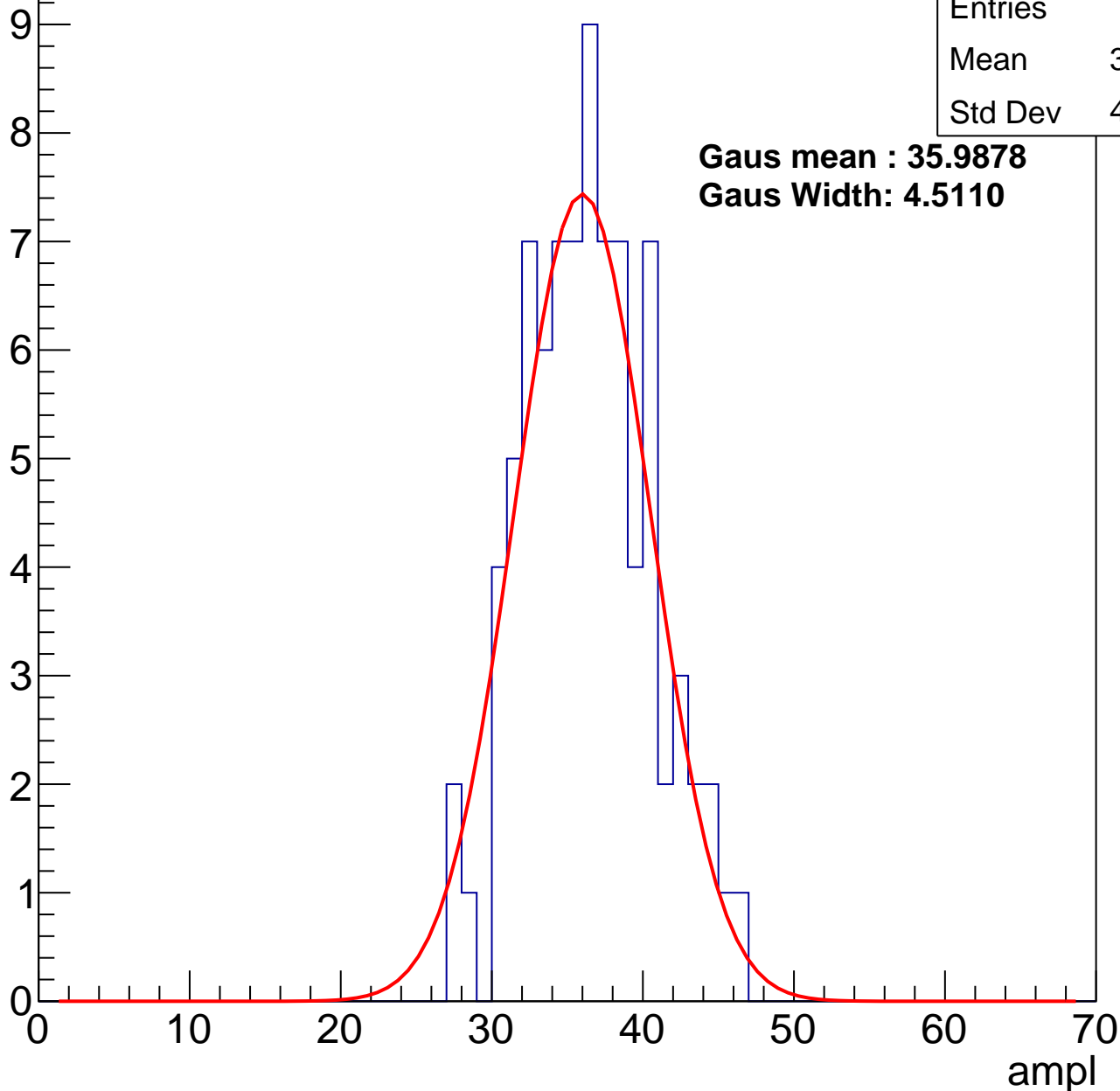
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	35.95
Std Dev	4.146

**Gaus mean : 35.9878**

**Gaus Width: 4.5110**



# B1L102S, U16-ch49, adc2

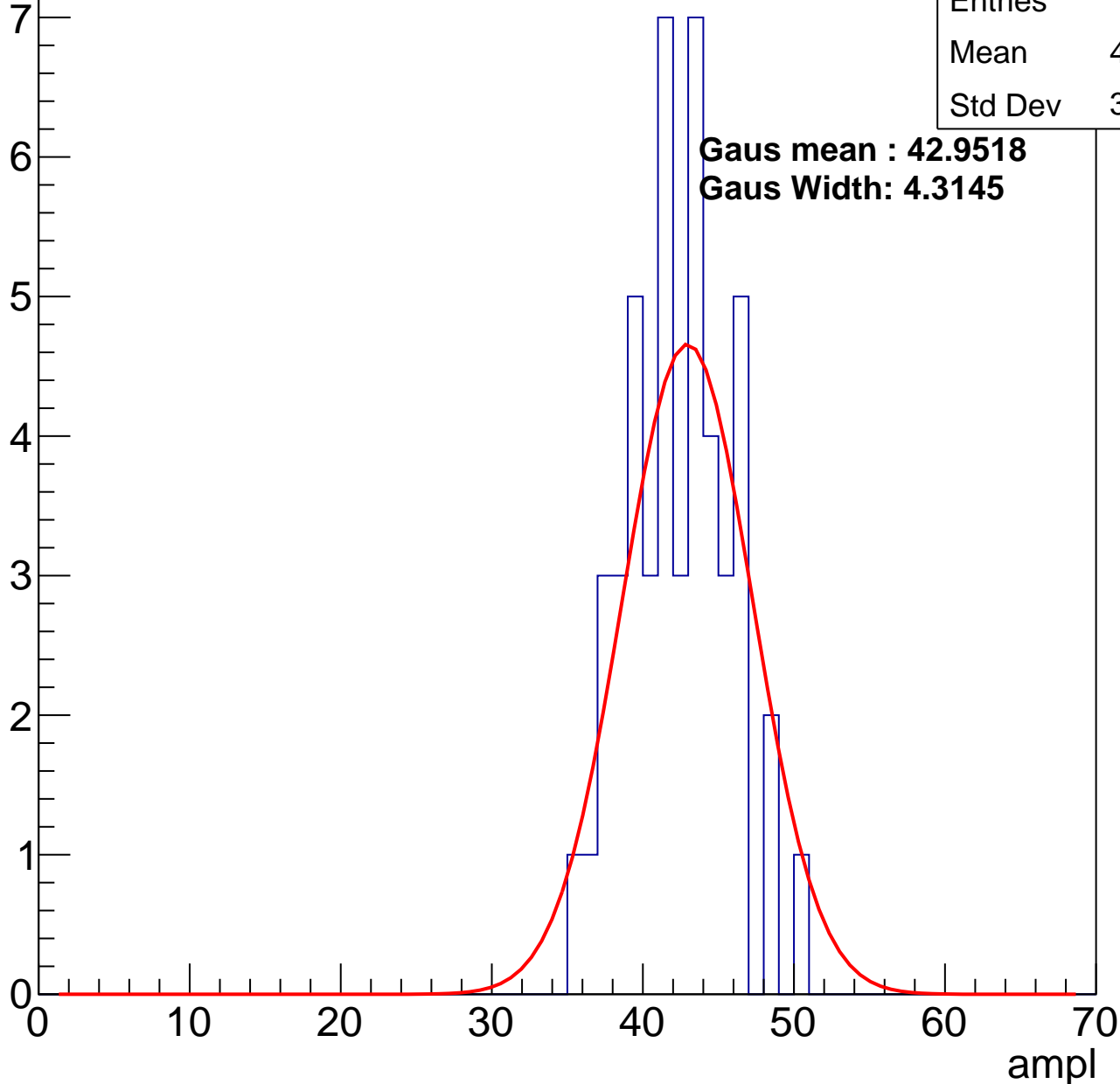
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	41.92
Std Dev	3.347

**Gaus mean : 42.9518**

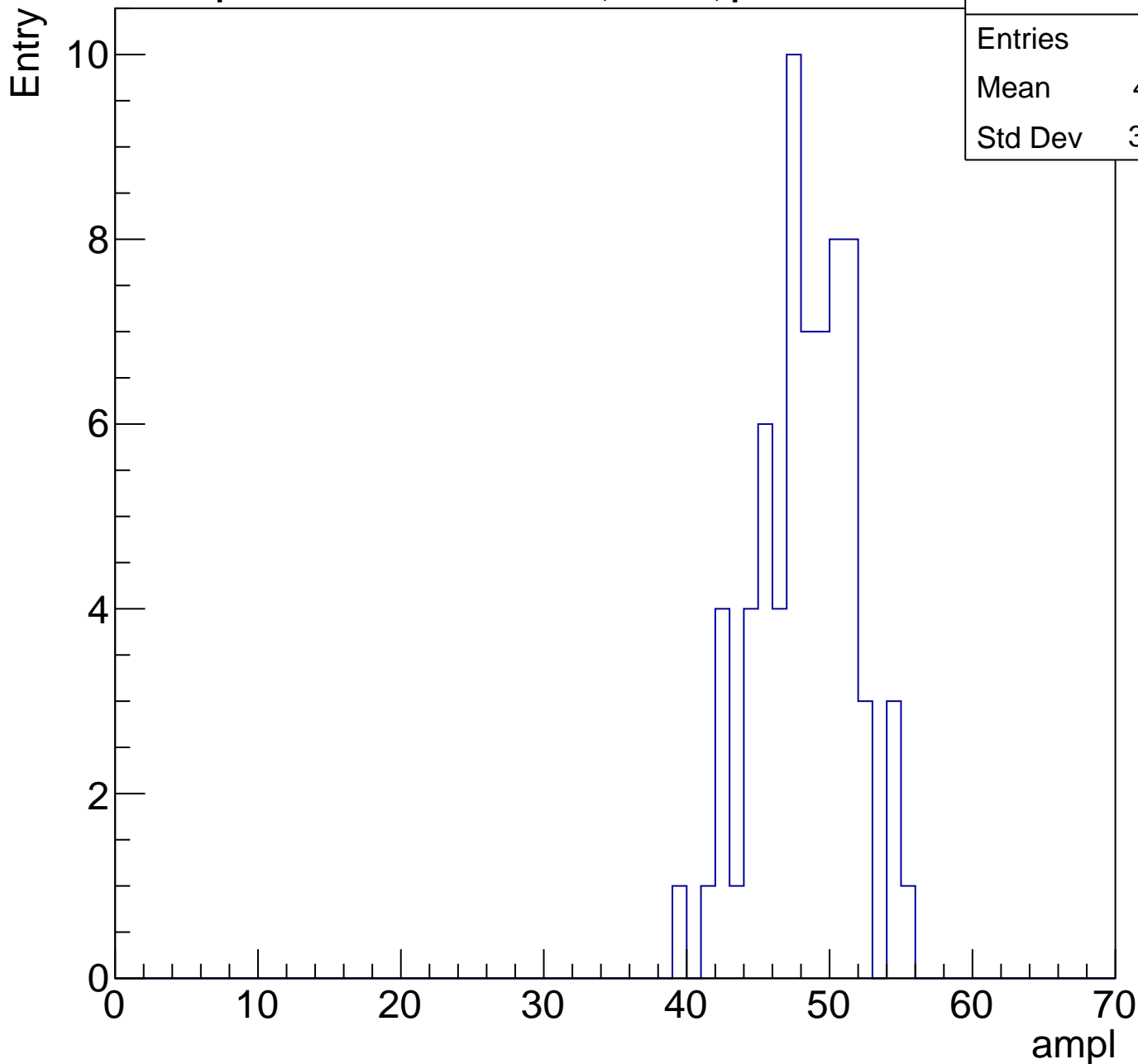
**Gaus Width: 4.3145**



# B1L102S, U16-ch49, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	68
Mean	47.81
Std Dev	3.335

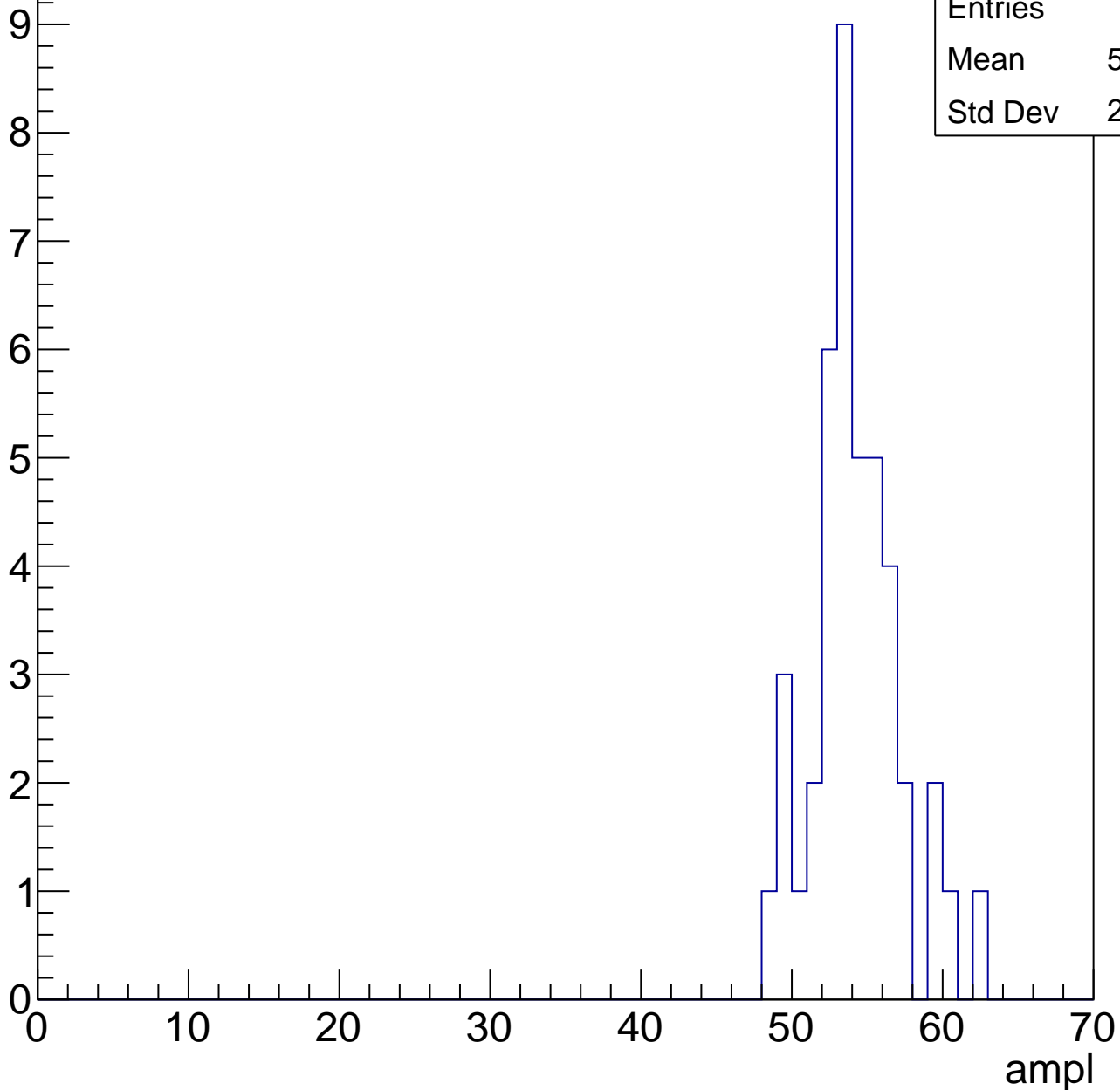


# B1L102S, U16-ch49, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	42
Mean	53.79
Std Dev	2.948



# B1L102S, U16-ch49, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

10

8

6

4

2

0

0

10

20

30

40

50

60

70

ampl

Entries	71
Mean	58.9
Std Dev	2.702

0

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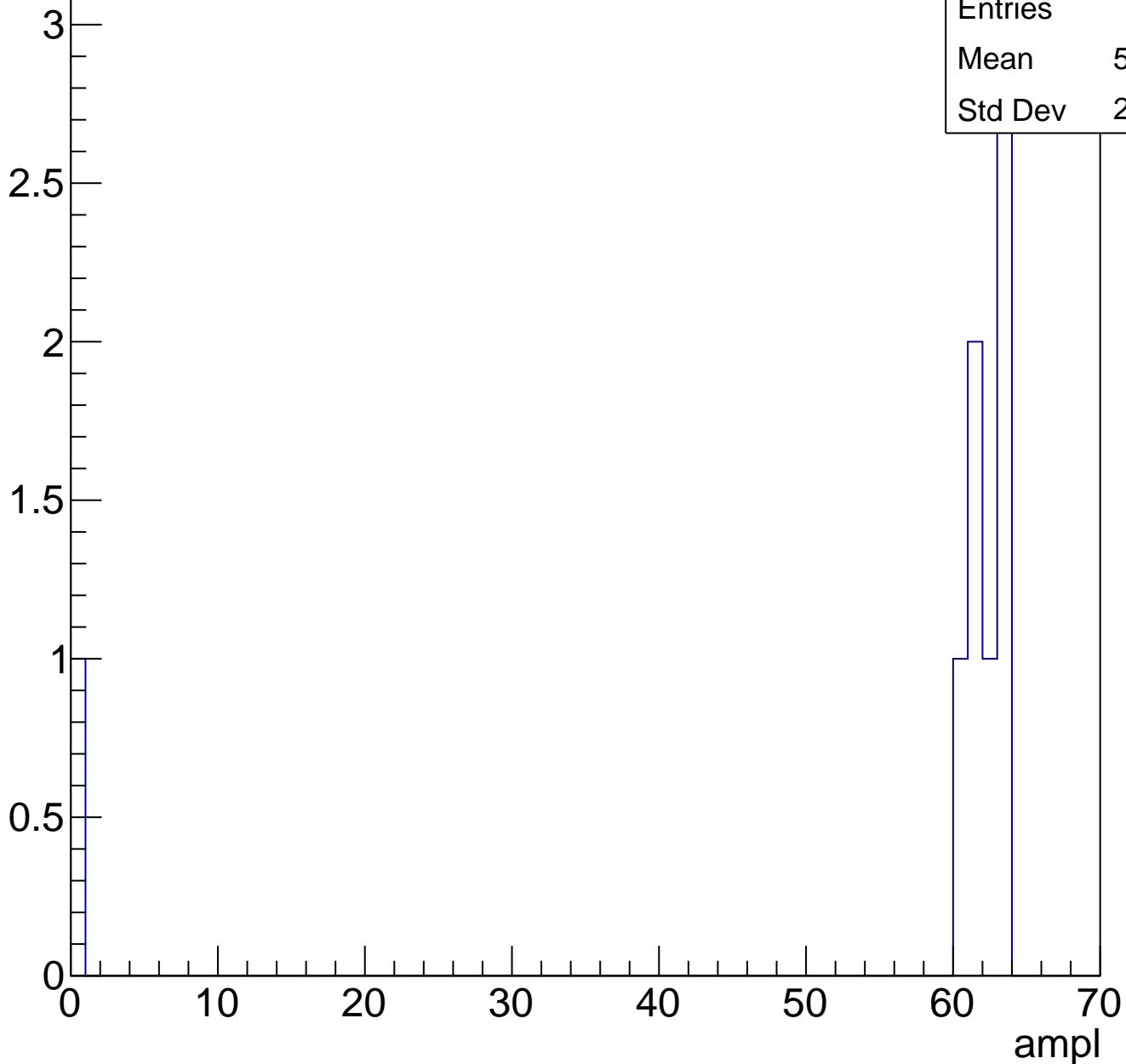
0

0

# B1L102S, U16-ch49, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch49, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U16-ch50, adc0

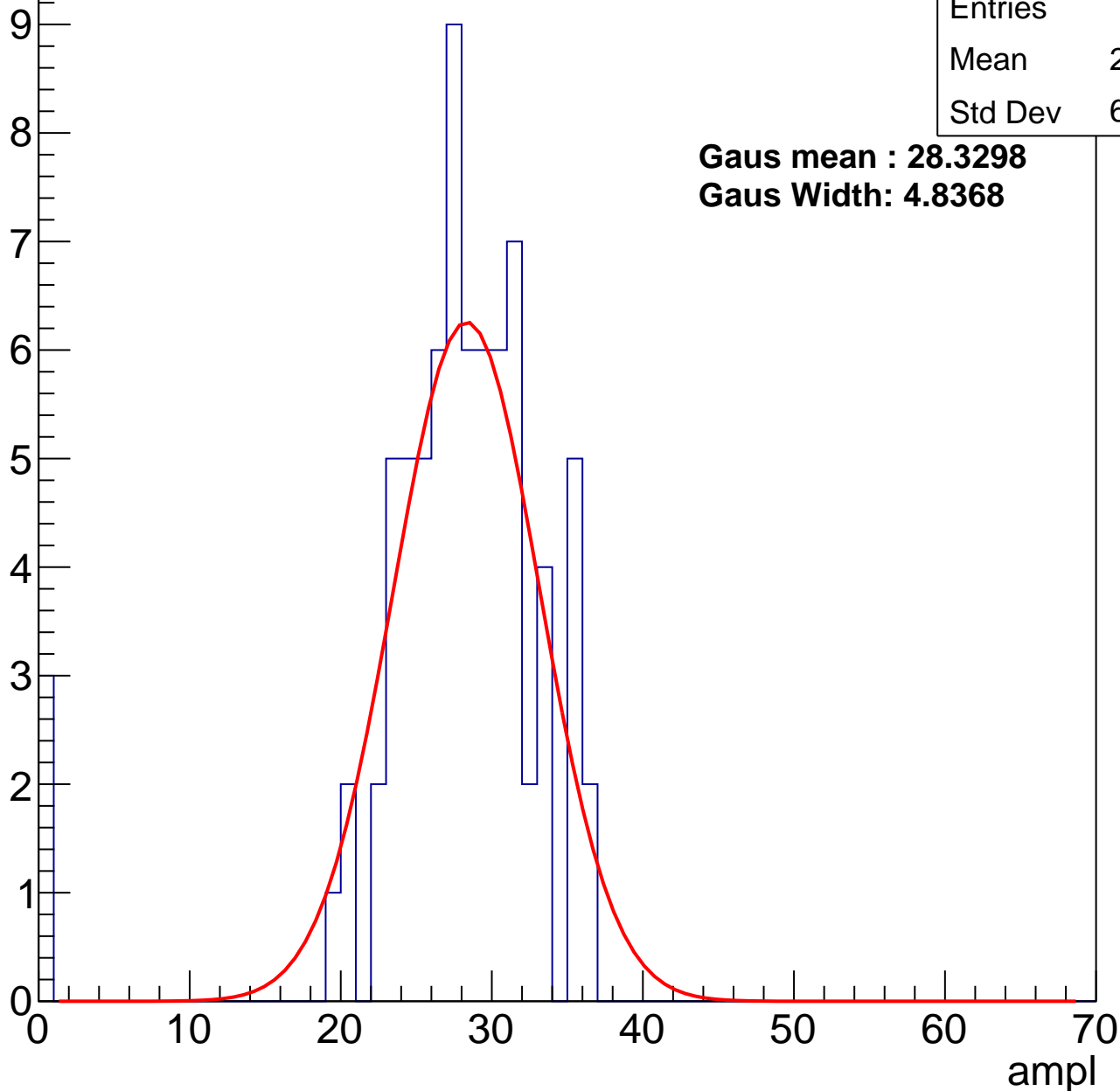
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	26.89
Std Dev	6.709

**Gaus mean : 28.3298**

**Gaus Width: 4.8368**



# B1L102S, U16-ch50, adc1

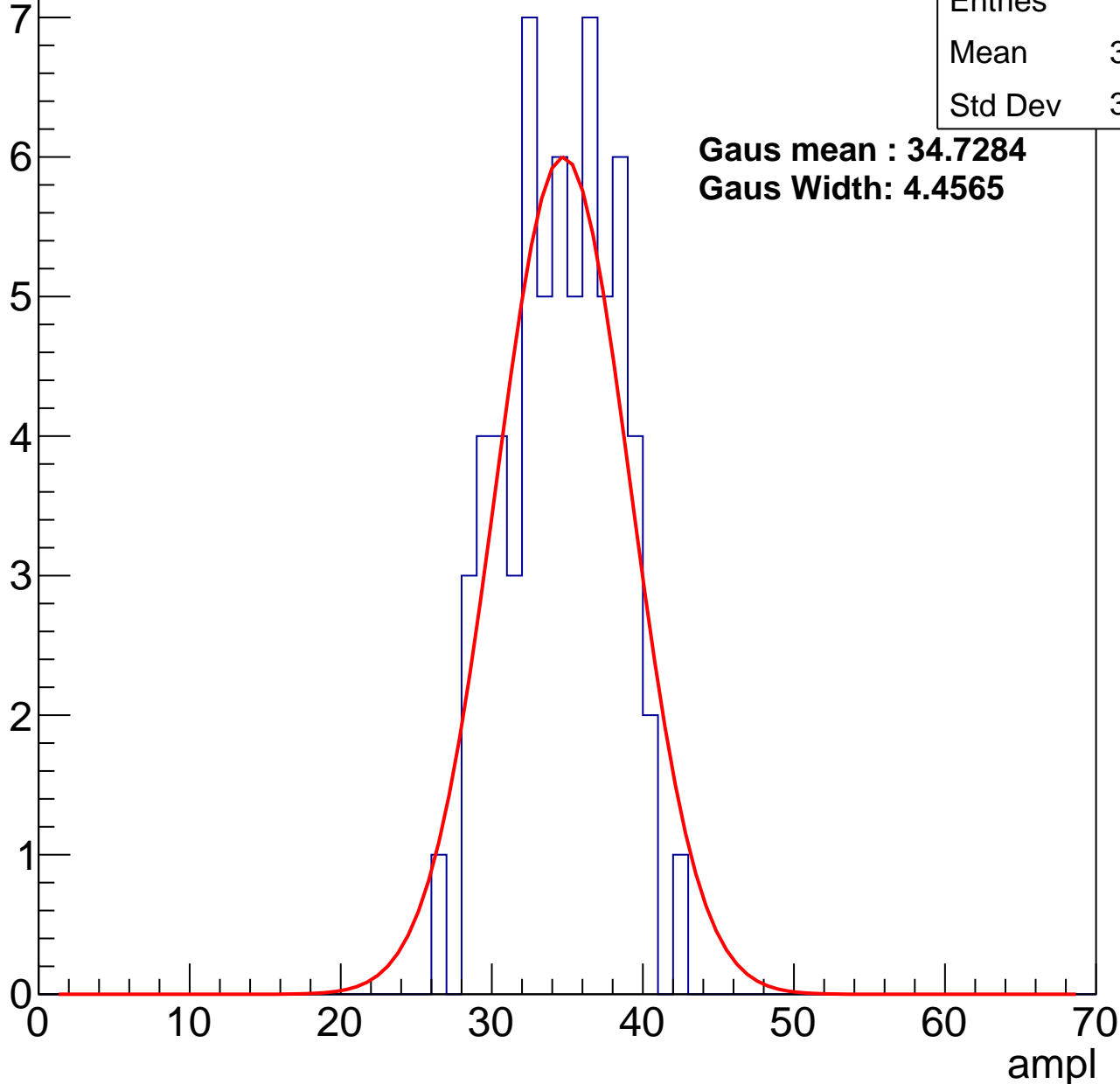
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	34.13
Std Dev	3.575

**Gaus mean : 34.7284**

**Gaus Width: 4.4565**



# B1L102S, U16-ch50, adc2

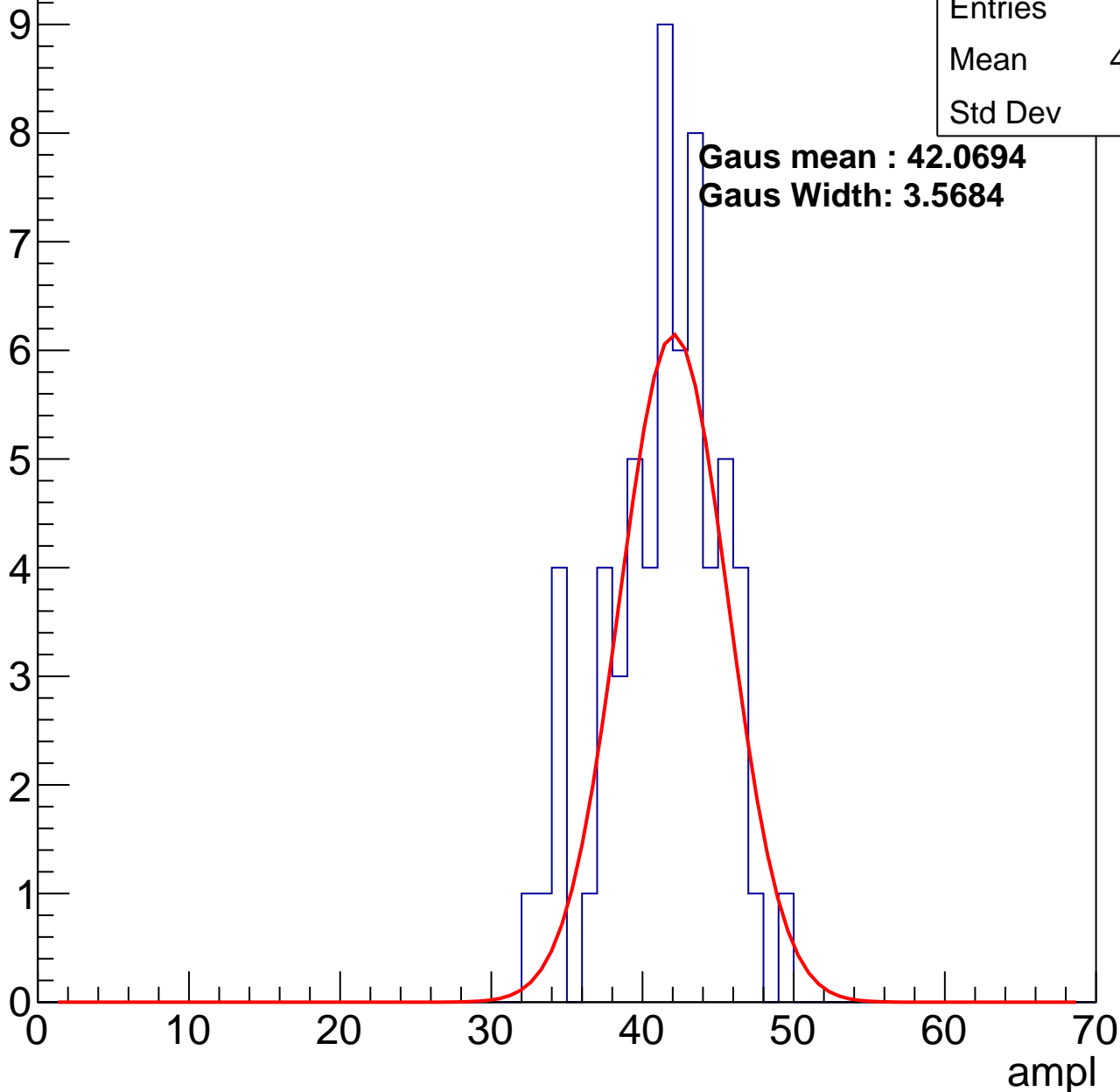
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	40.98
Std Dev	3.7

**Gaus mean : 42.0694**

**Gaus Width: 3.5684**

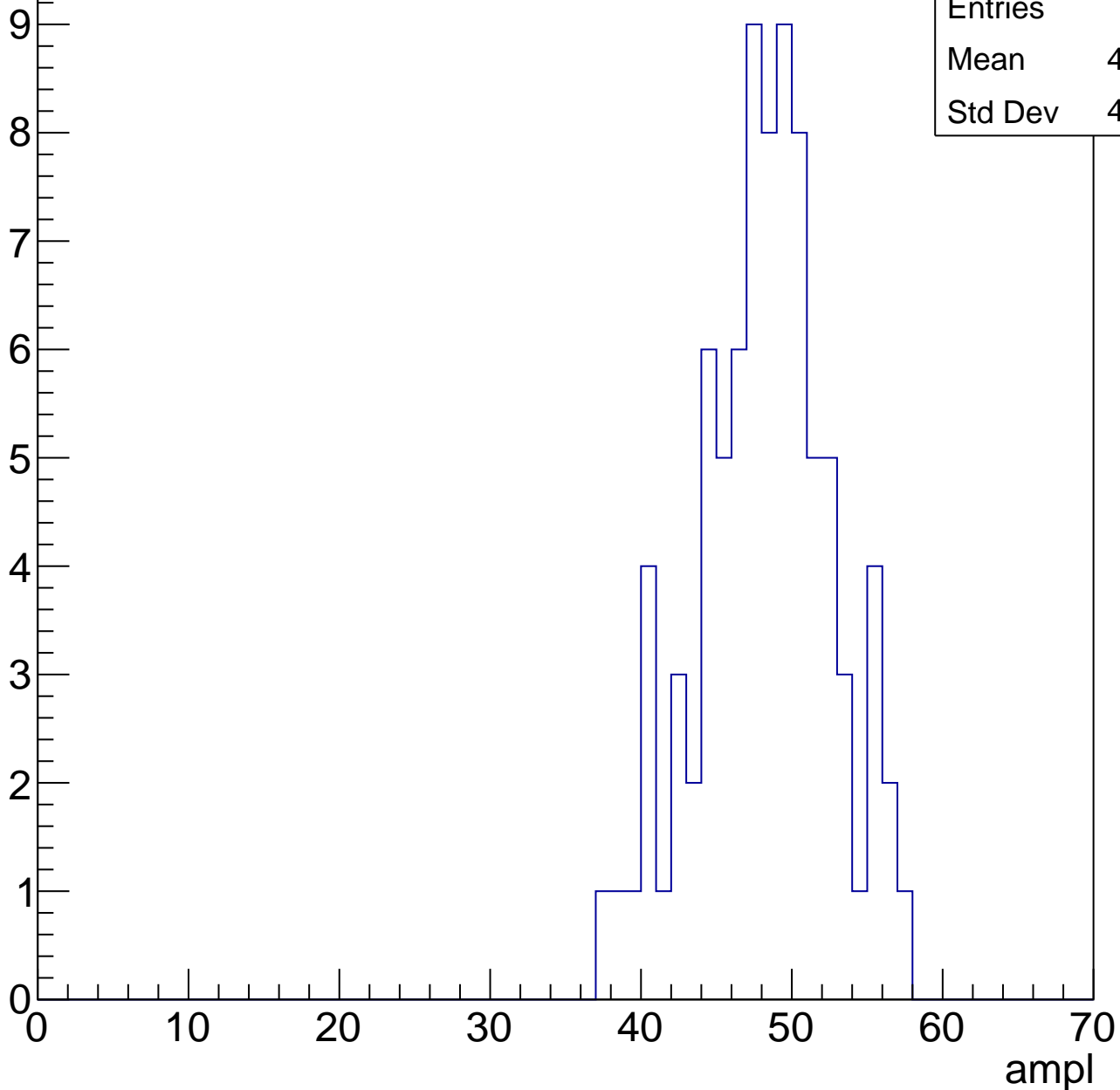


# B1L102S, U16-ch50, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

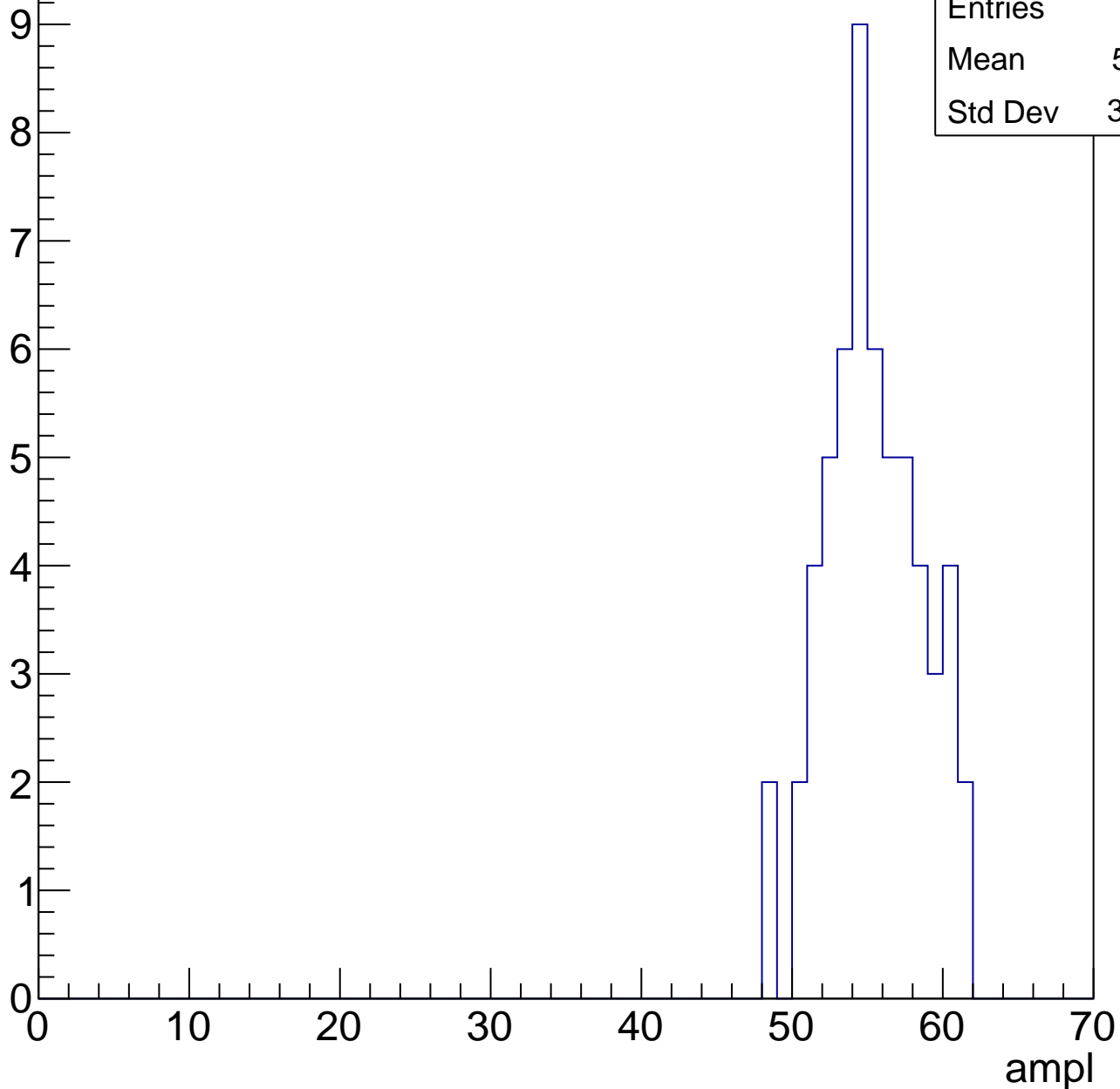
Entries	85
Mean	47.73
Std Dev	4.359



# B1L102S, U16-ch50, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

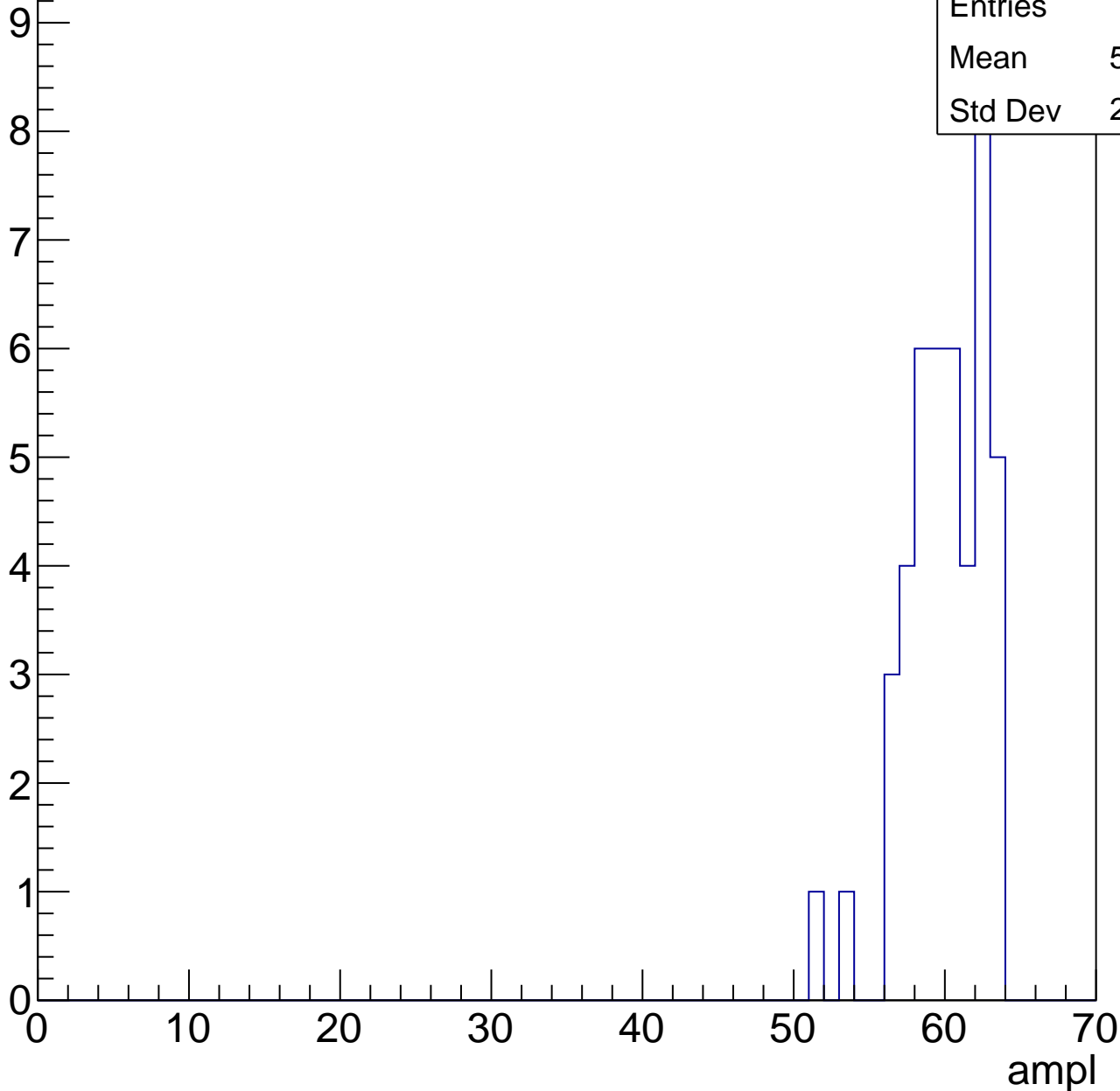


# B1L102S, U16-ch50, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

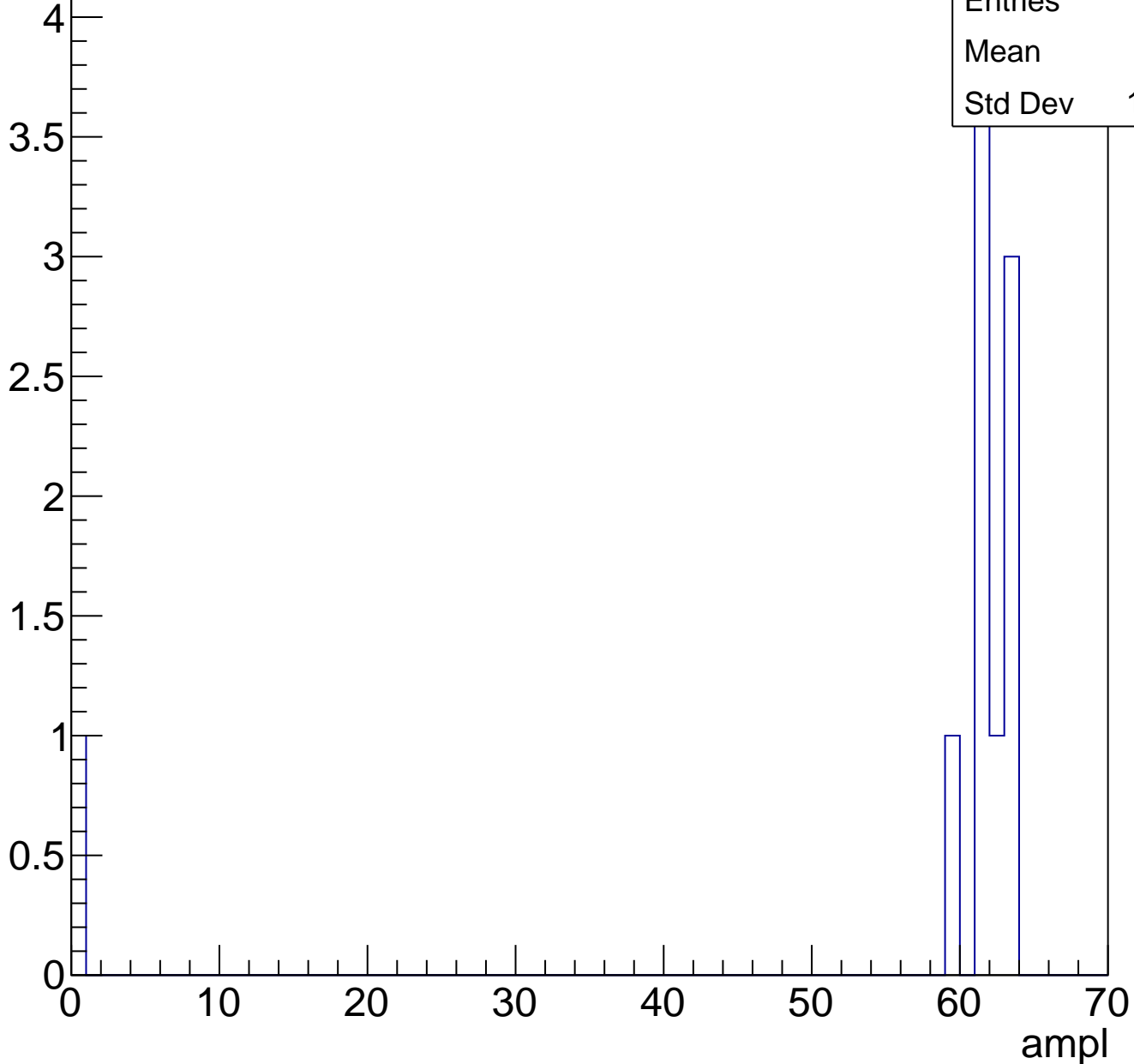
Entries	45
Mean	59.53
Std Dev	2.663



# B1L102S, U16-ch50, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch50, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	4
Mean	31.5
Std Dev	31.5

# B1L102S, U16-ch51, adc0

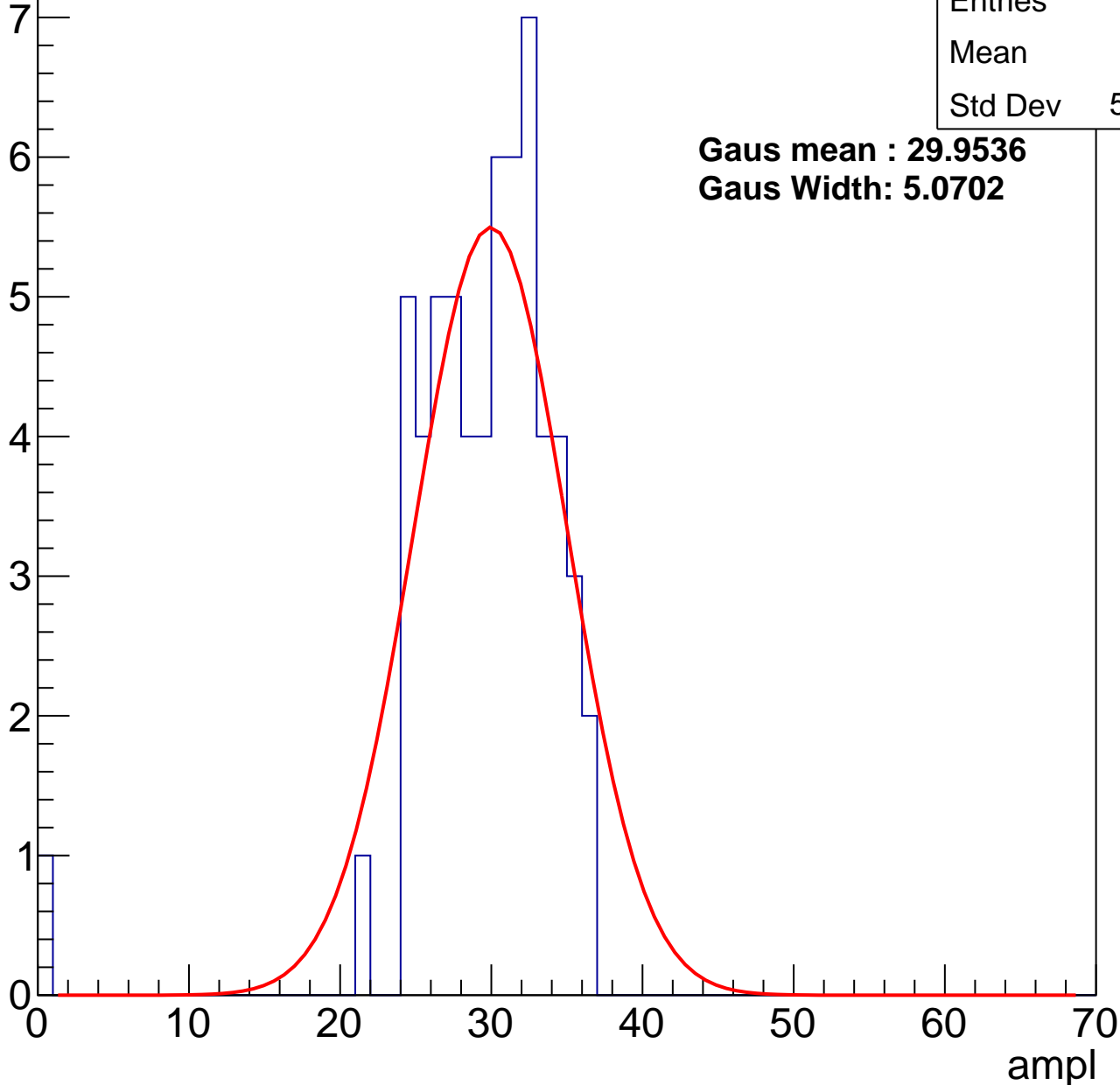
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	29
Std Dev	5.163

**Gaus mean : 29.9536**

**Gaus Width: 5.0702**



# B1L102S, U16-ch51, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	83
Mean	36.61
Std Dev	3.676

**Gaus mean : 37.0285**

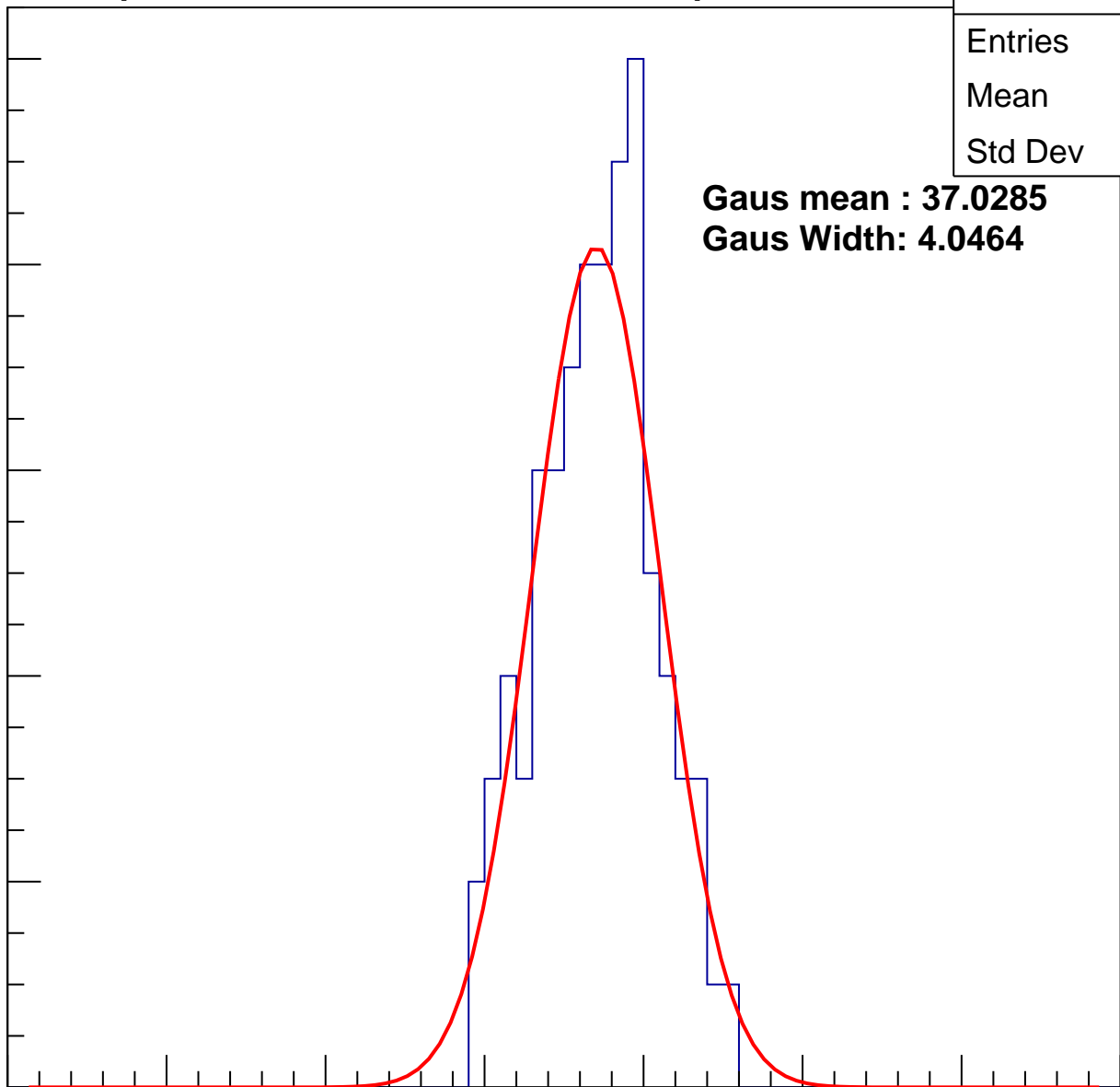
**Gaus Width: 4.0464**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U16-ch51, adc2

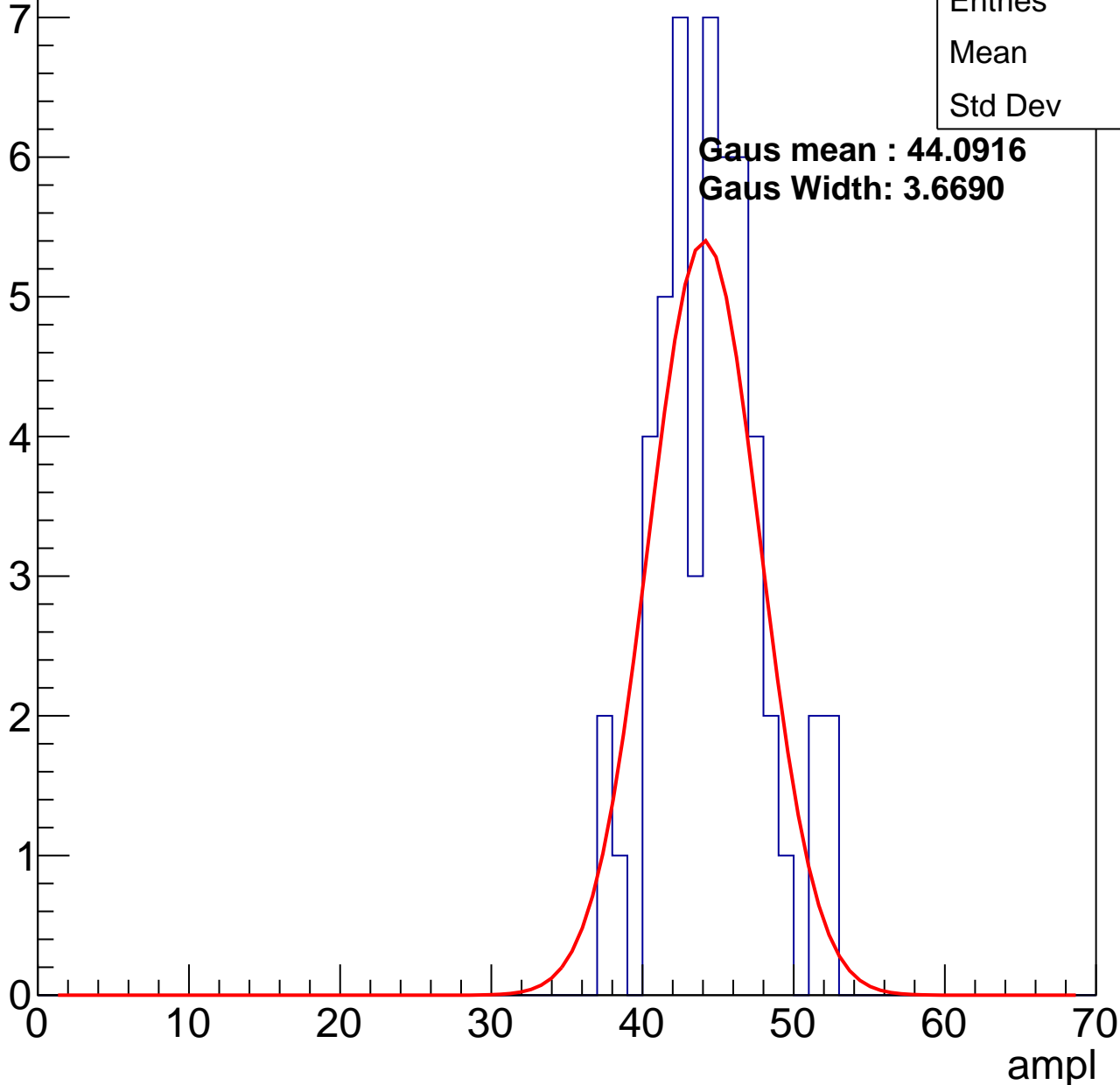
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	44.1
Std Dev	3.46

**Gaus mean : 44.0916**

**Gaus Width: 3.6690**

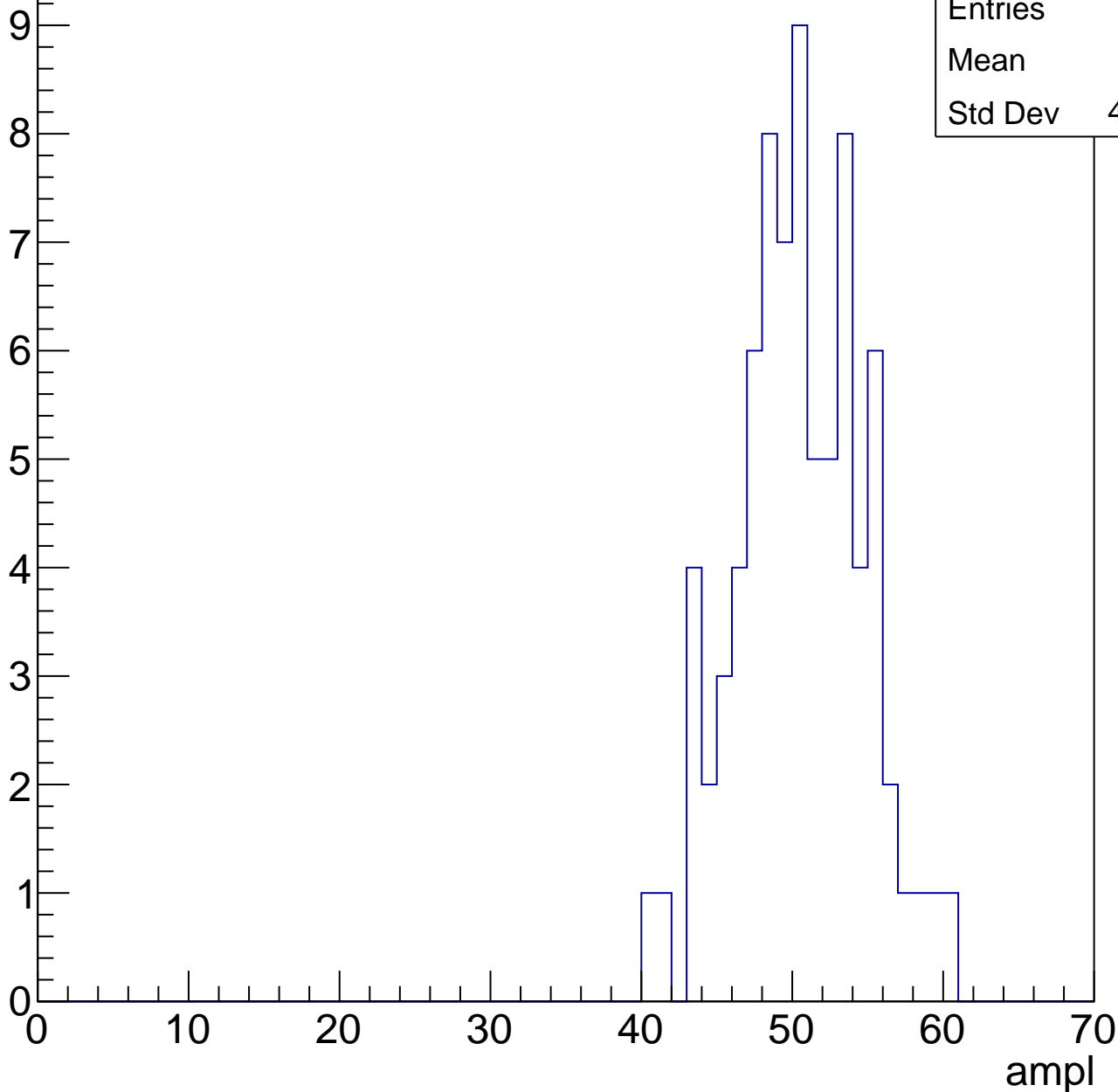


# B1L102S, U16-ch51, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

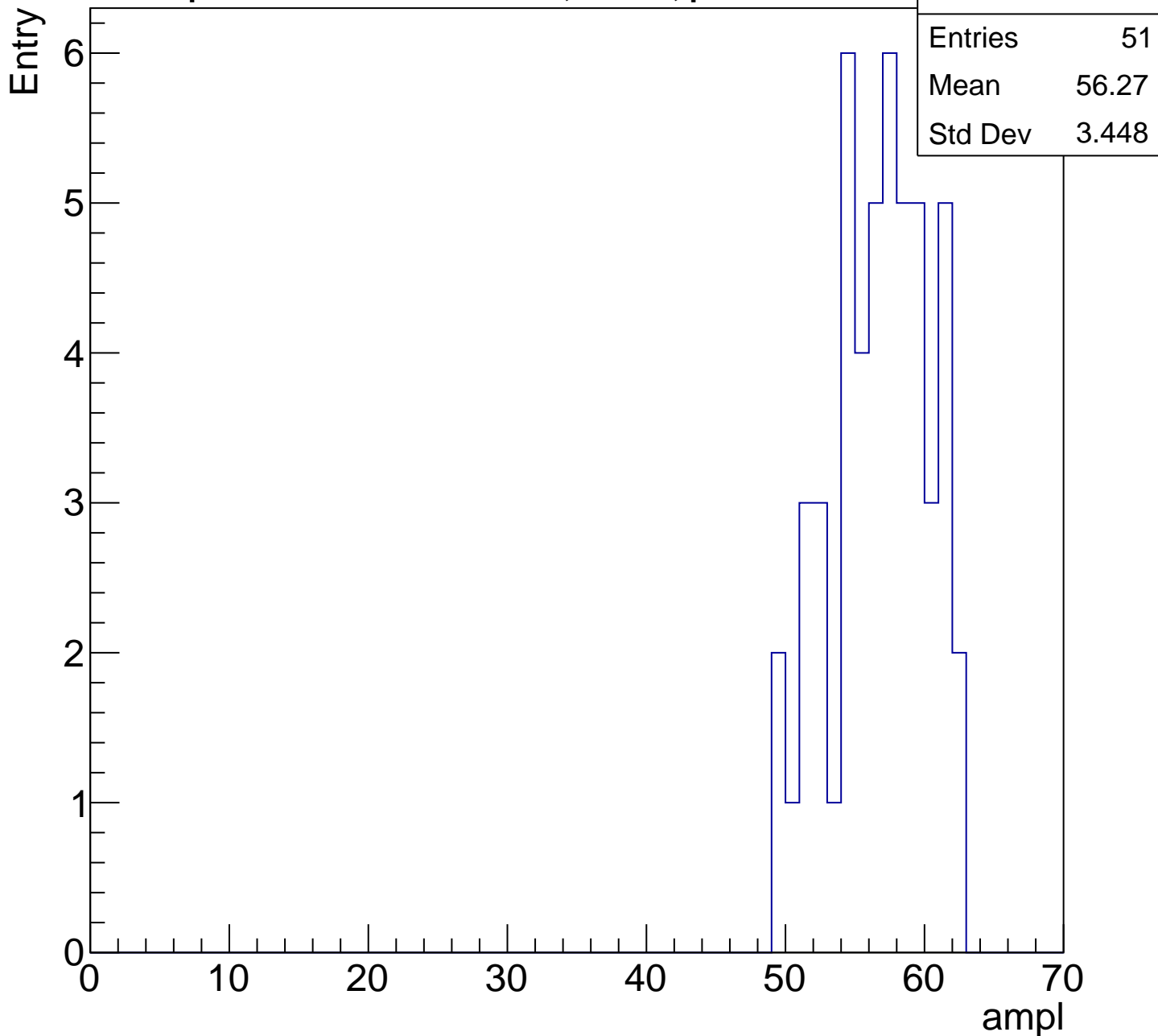
Entry

Entries	79
Mean	50
Std Dev	4.146



# B1L102S, U16-ch51, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

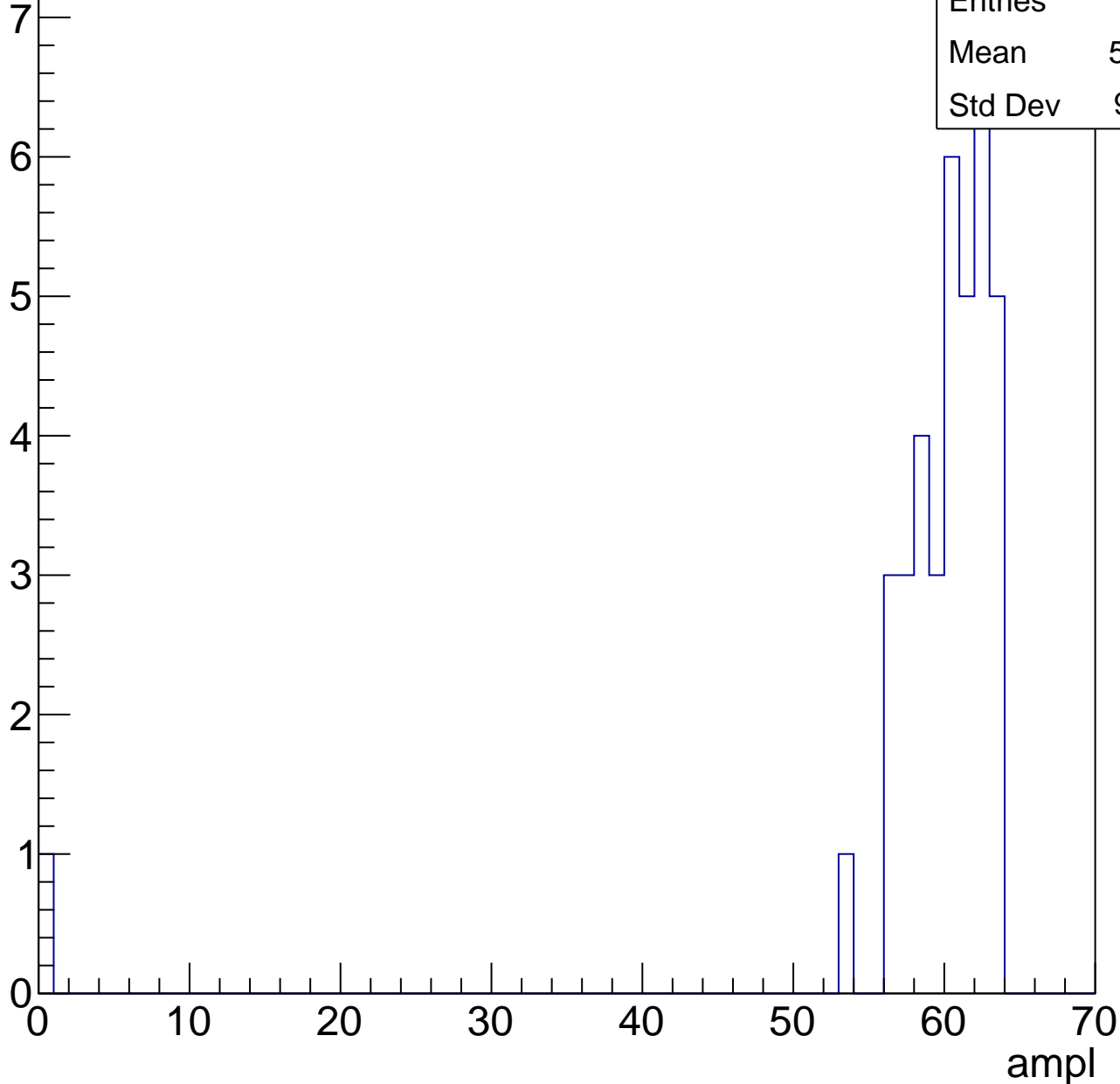


# B1L102S, U16-ch51, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	38
Mean	58.29
Std Dev	9.881

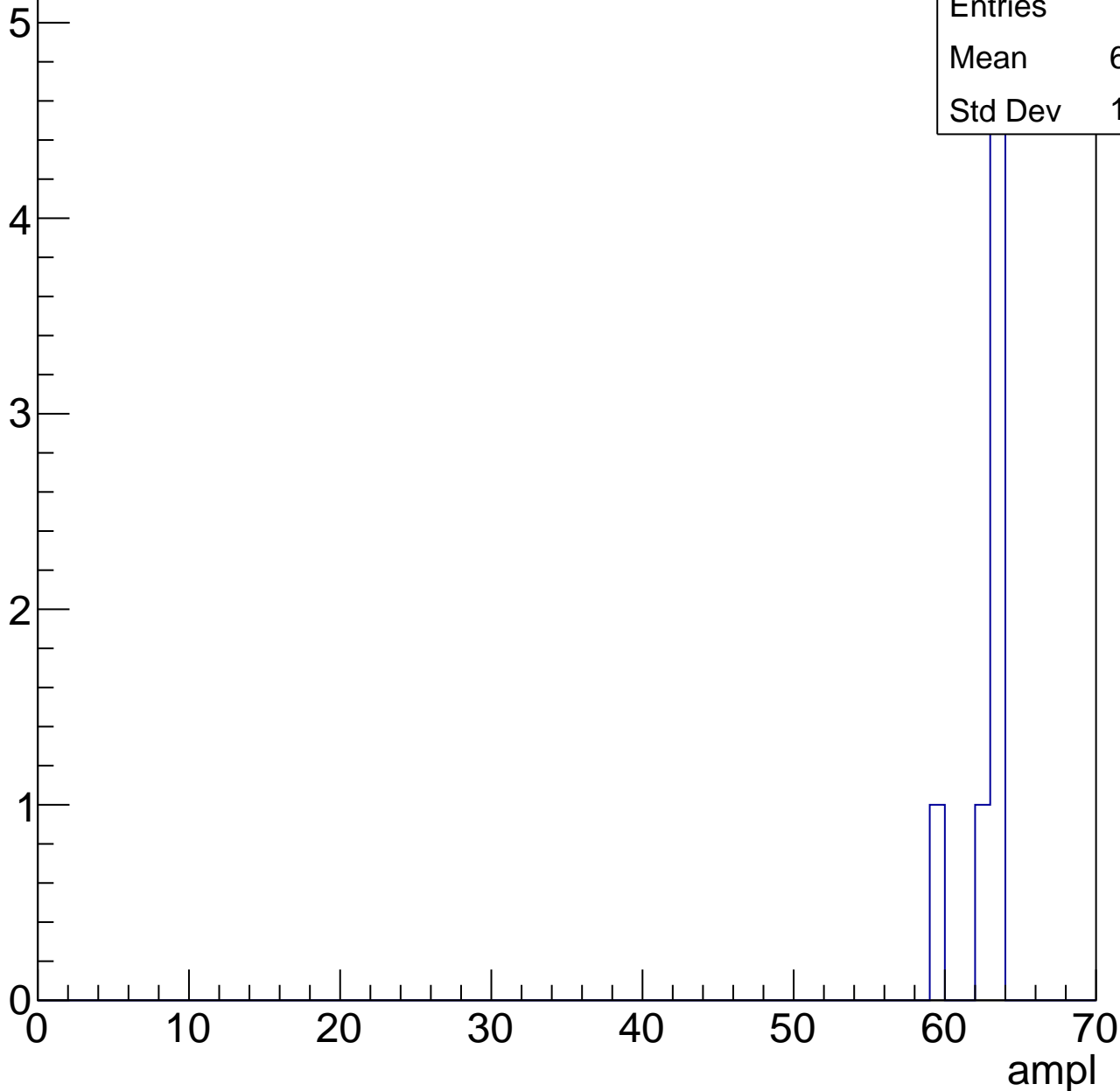


# B1L102S, U16-ch51, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	7
Mean	62.29
Std Dev	1.385

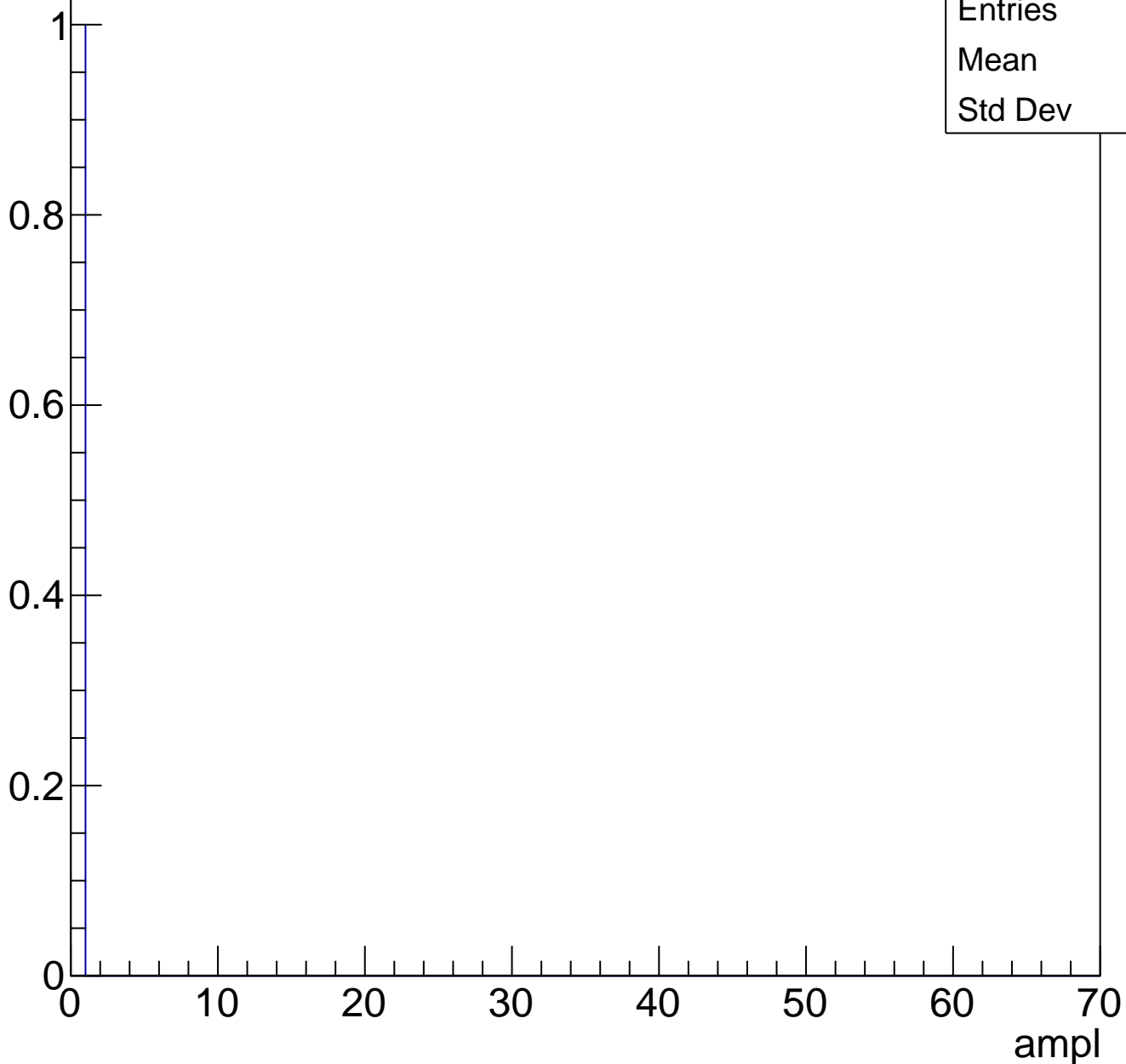




# B1L102S, U16-ch51, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch52, adc0

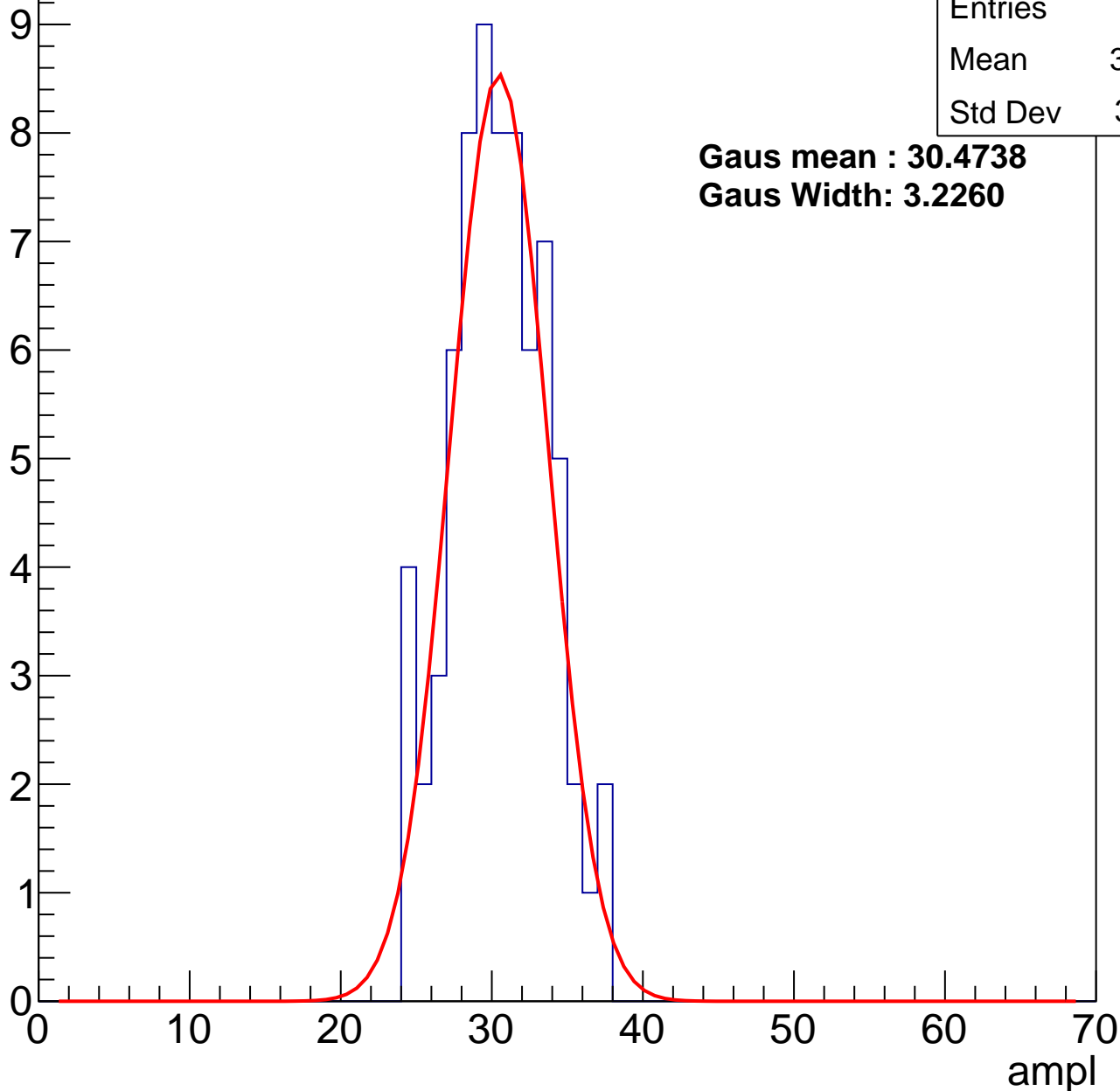
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	30.03
Std Dev	3.131

**Gaus mean : 30.4738**

**Gaus Width: 3.2260**



# B1L102S, U16-ch52, adc1

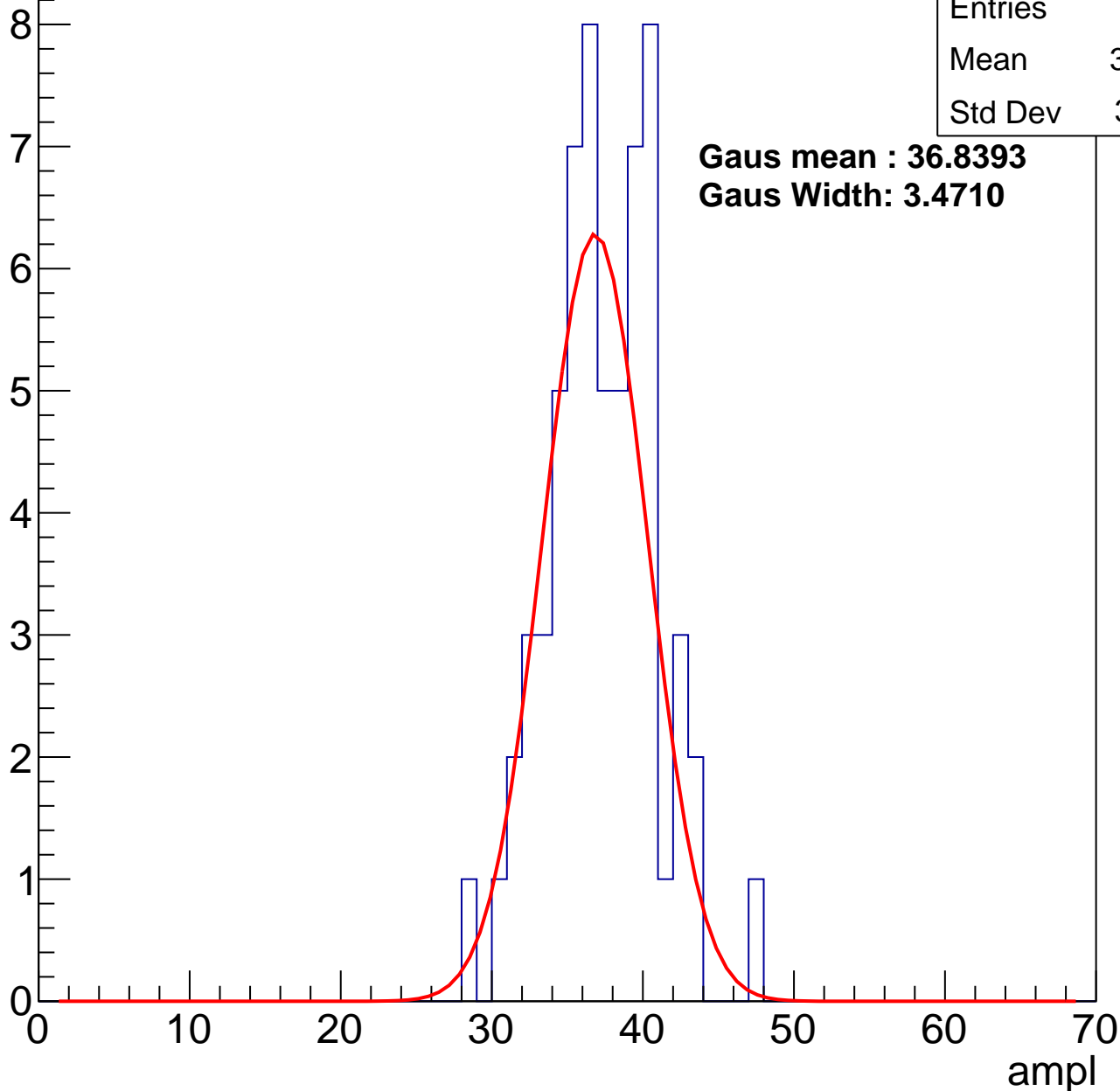
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	36.87
Std Dev	3.531

**Gaus mean : 36.8393**

**Gaus Width: 3.4710**



# B1L102S, U16-ch52, adc2

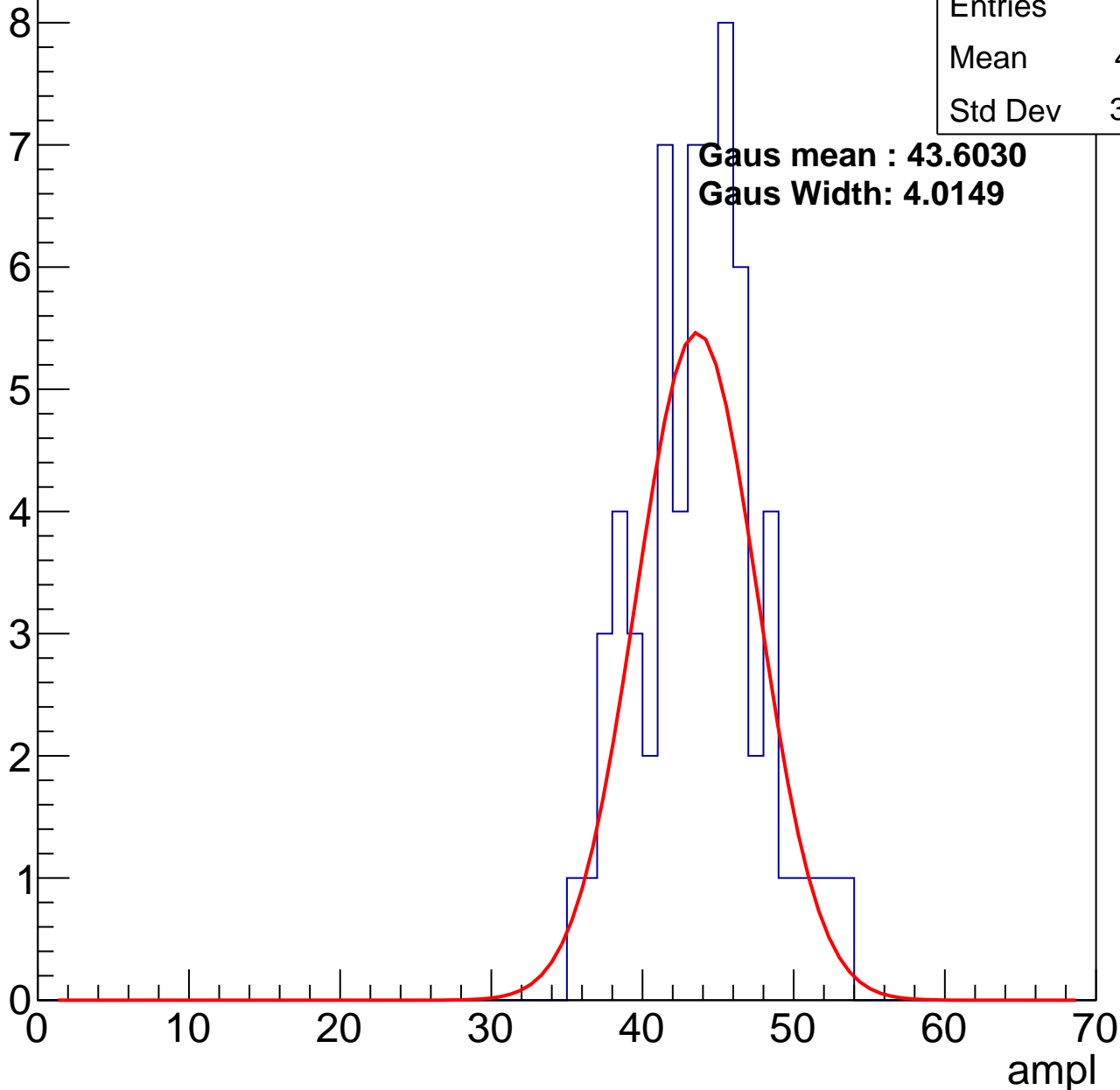
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	43.31
Std Dev	3.889

**Gaus mean : 43.6030**

**Gaus Width: 4.0149**

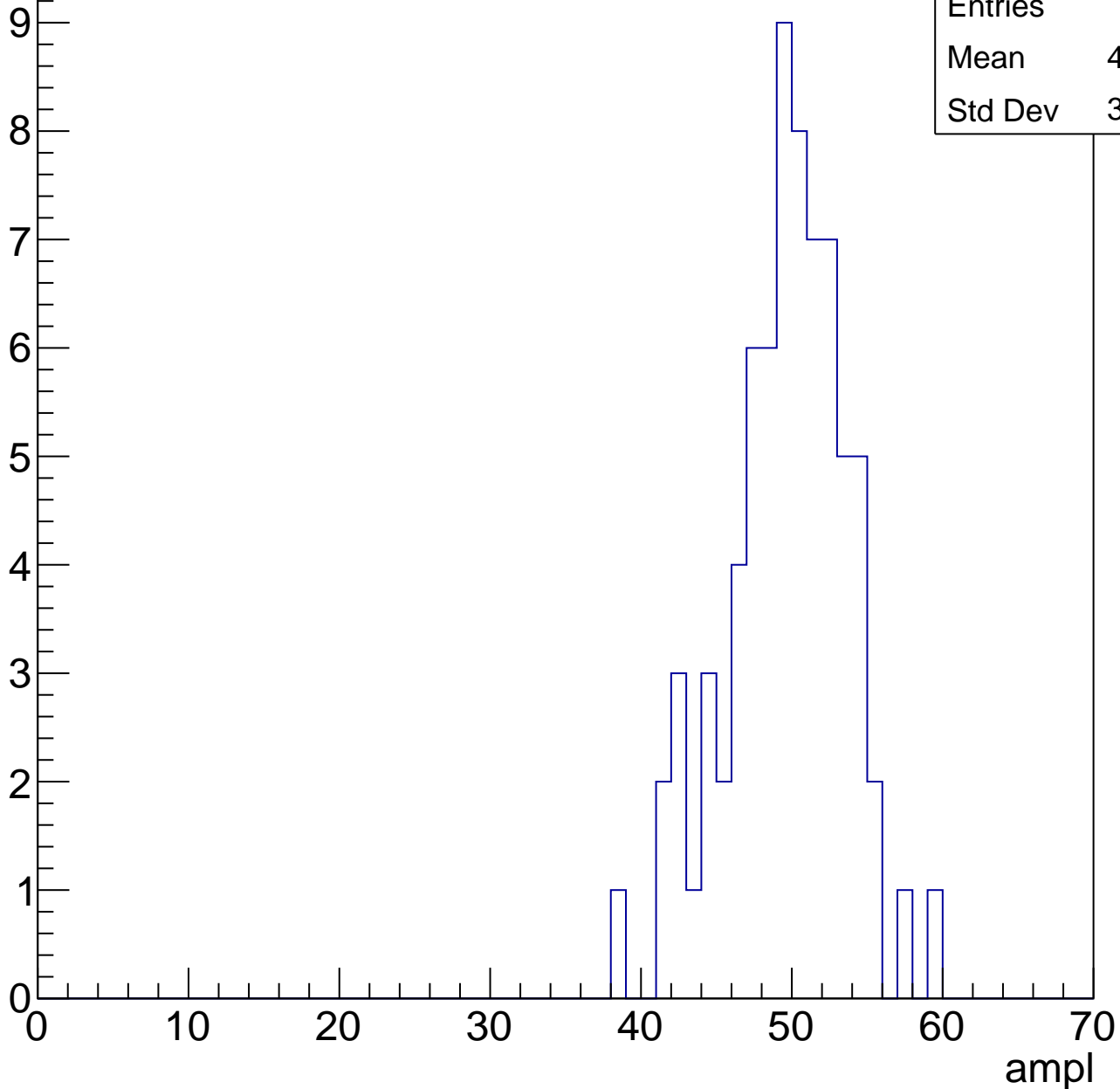


# B1L102S, U16-ch52, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	49.15
Std Dev	3.958

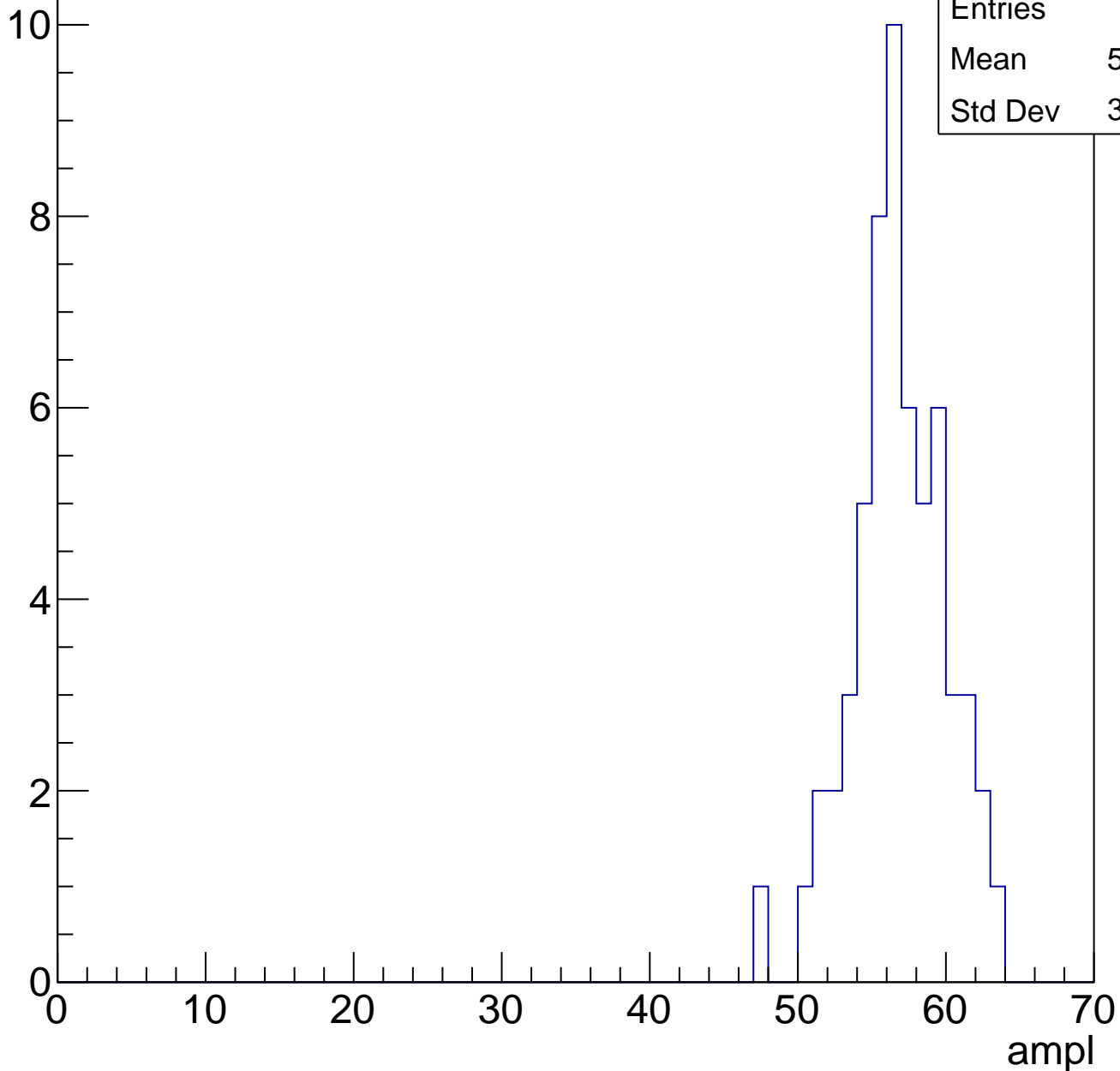


# B1L102S, U16-ch52, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	56.34
Std Dev	3.138

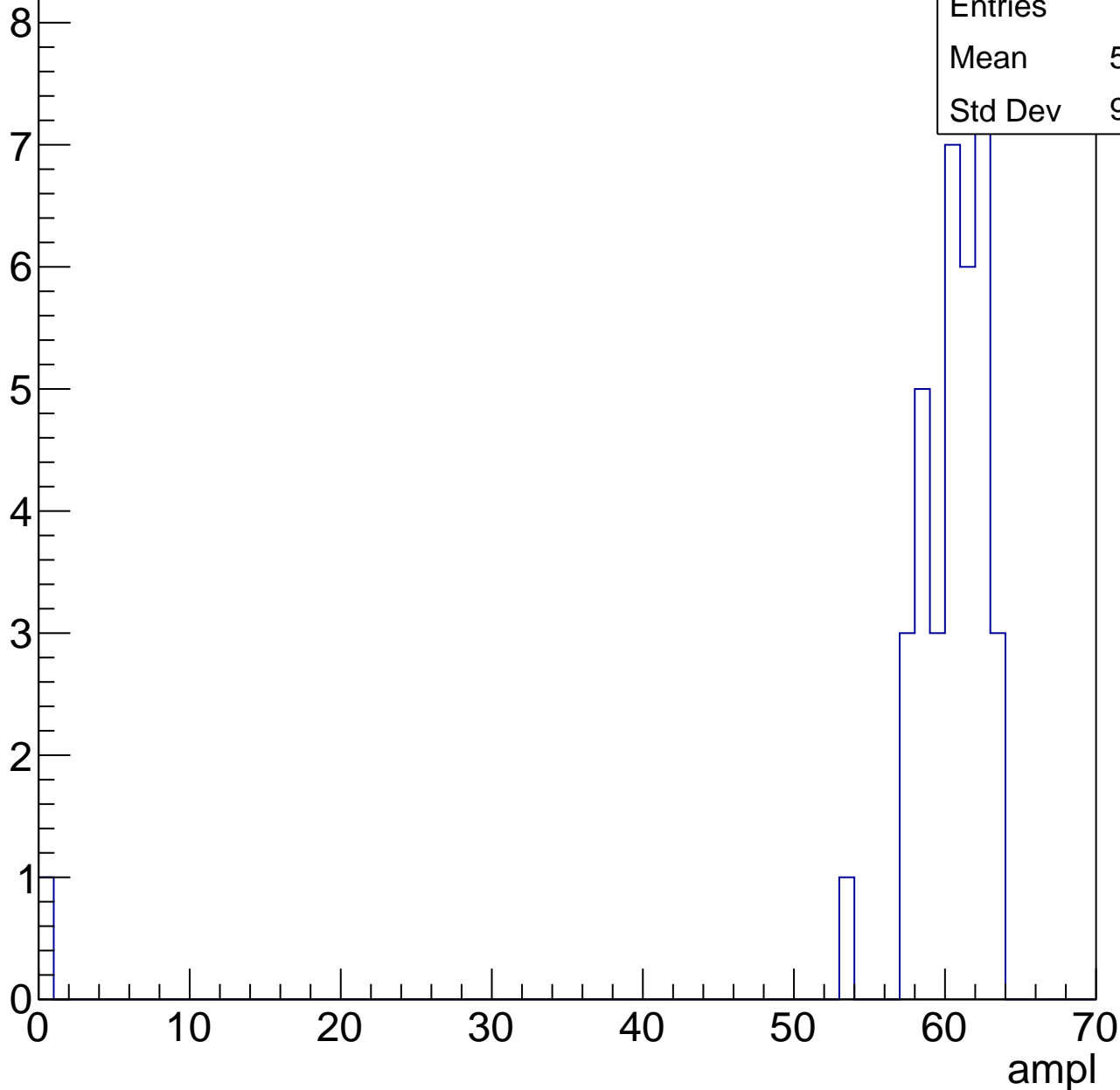


# B1L102S, U16-ch52, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	37
Mean	58.43
Std Dev	9.964

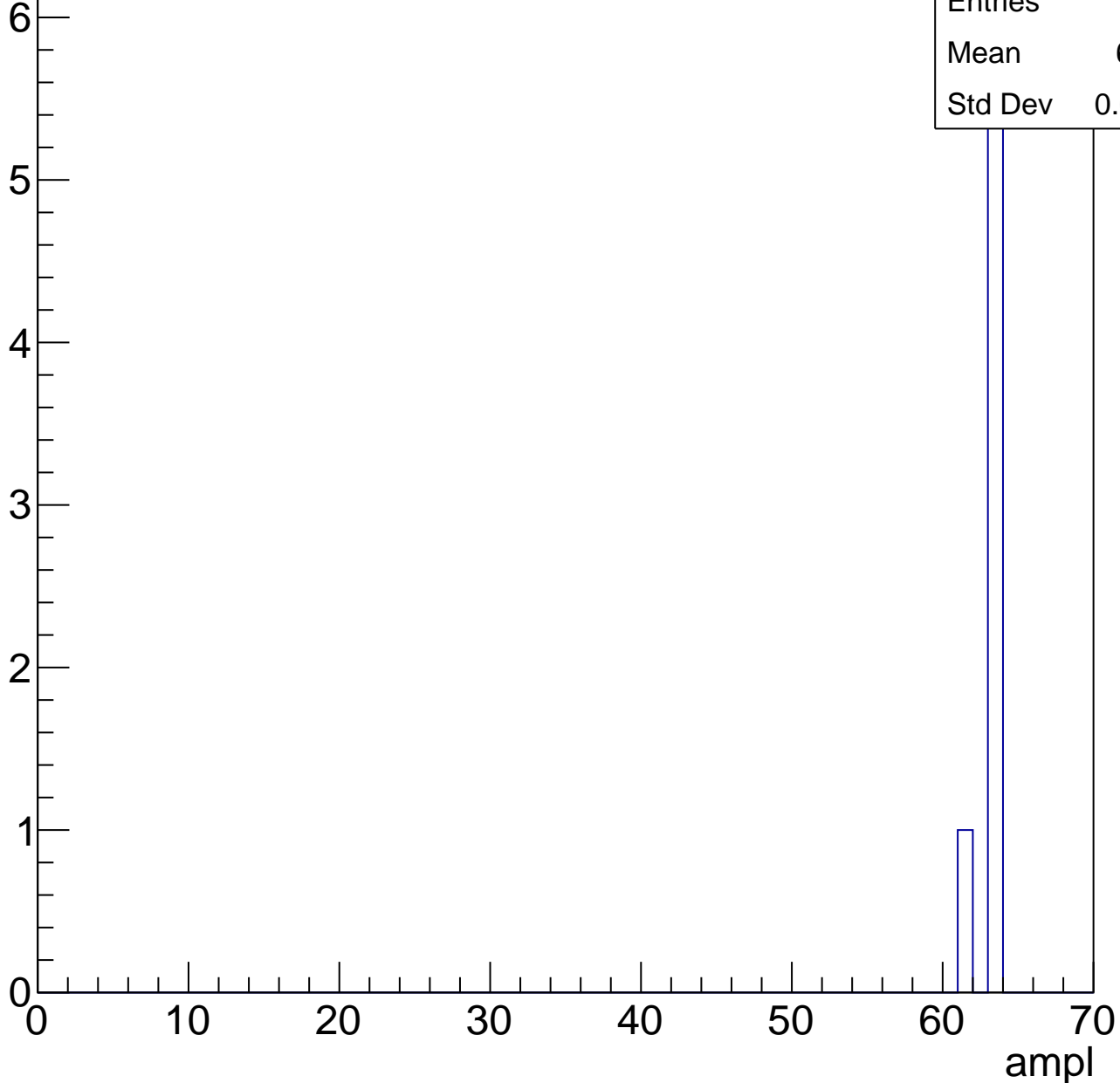


# B1L102S, U16-ch52, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	7
Mean	62.71
Std Dev	0.6999





# B1L102S, U16-ch52, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch53, adc0

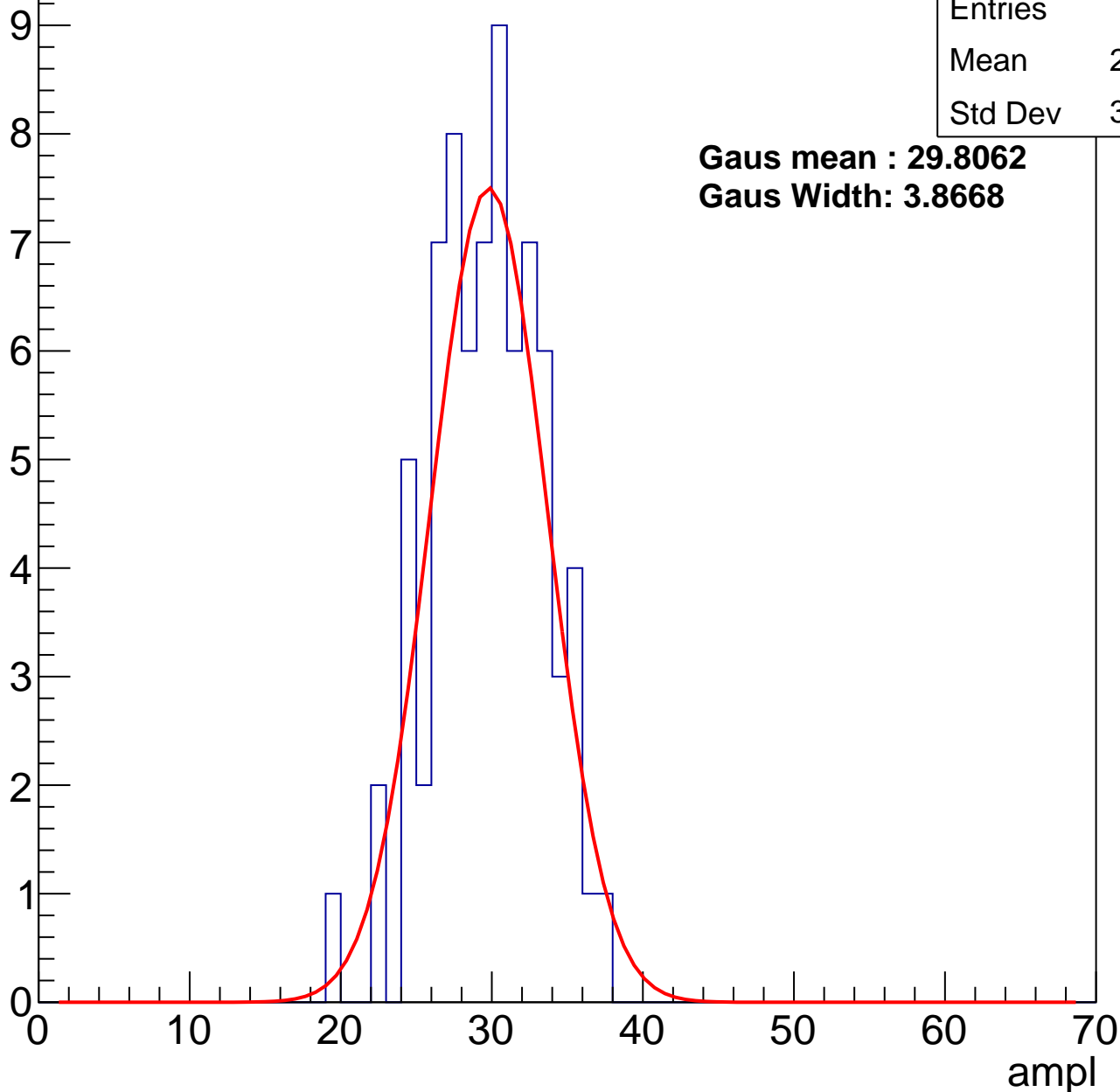
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	29.27
Std Dev	3.605

**Gaus mean : 29.8062**

**Gaus Width: 3.8668**



# B1L102S, U16-ch53, adc1

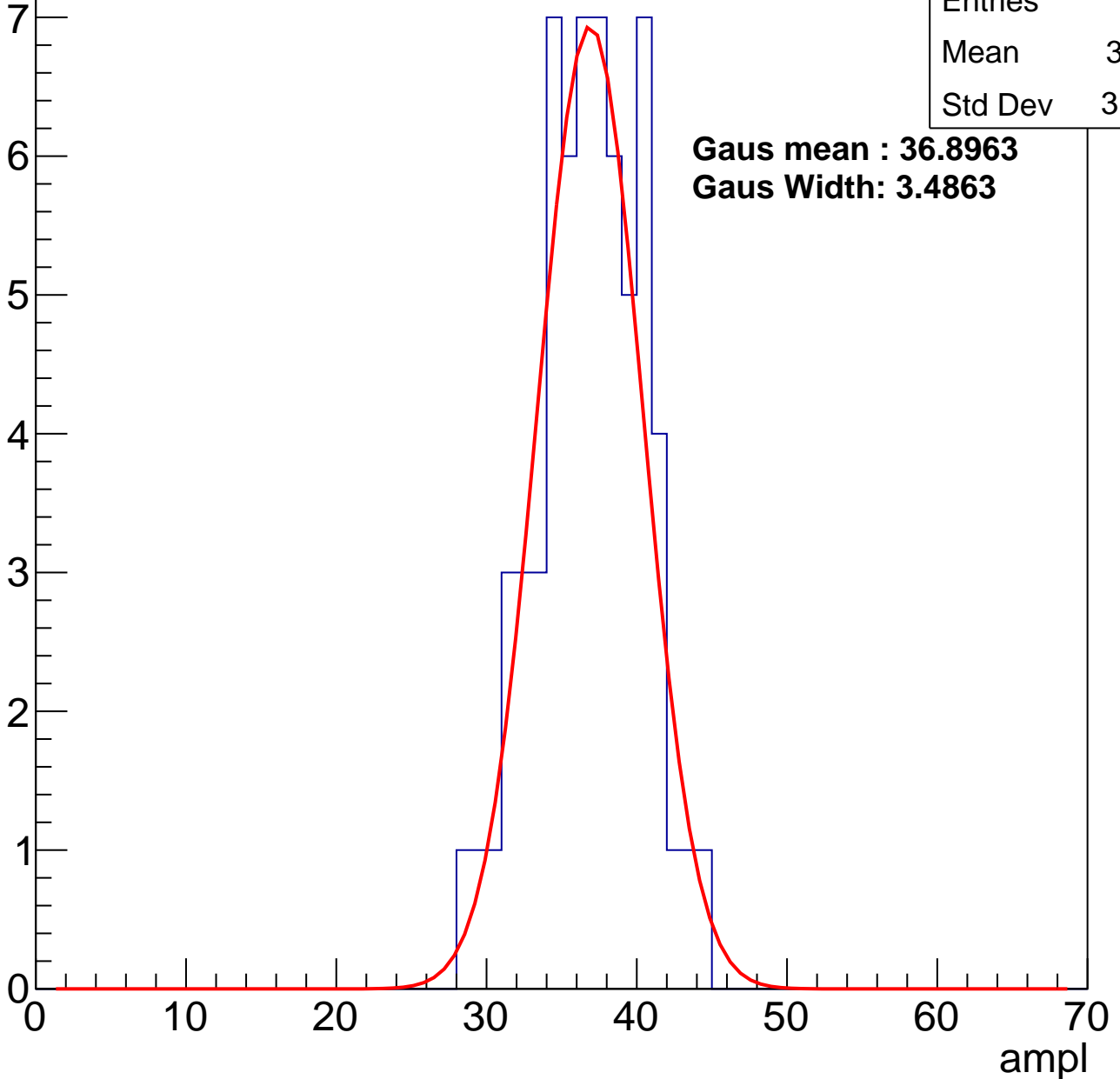
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	36.41
Std Dev	3.445

**Gaus mean : 36.8963**

**Gaus Width: 3.4863**



# B1L102S, U16-ch53, adc2

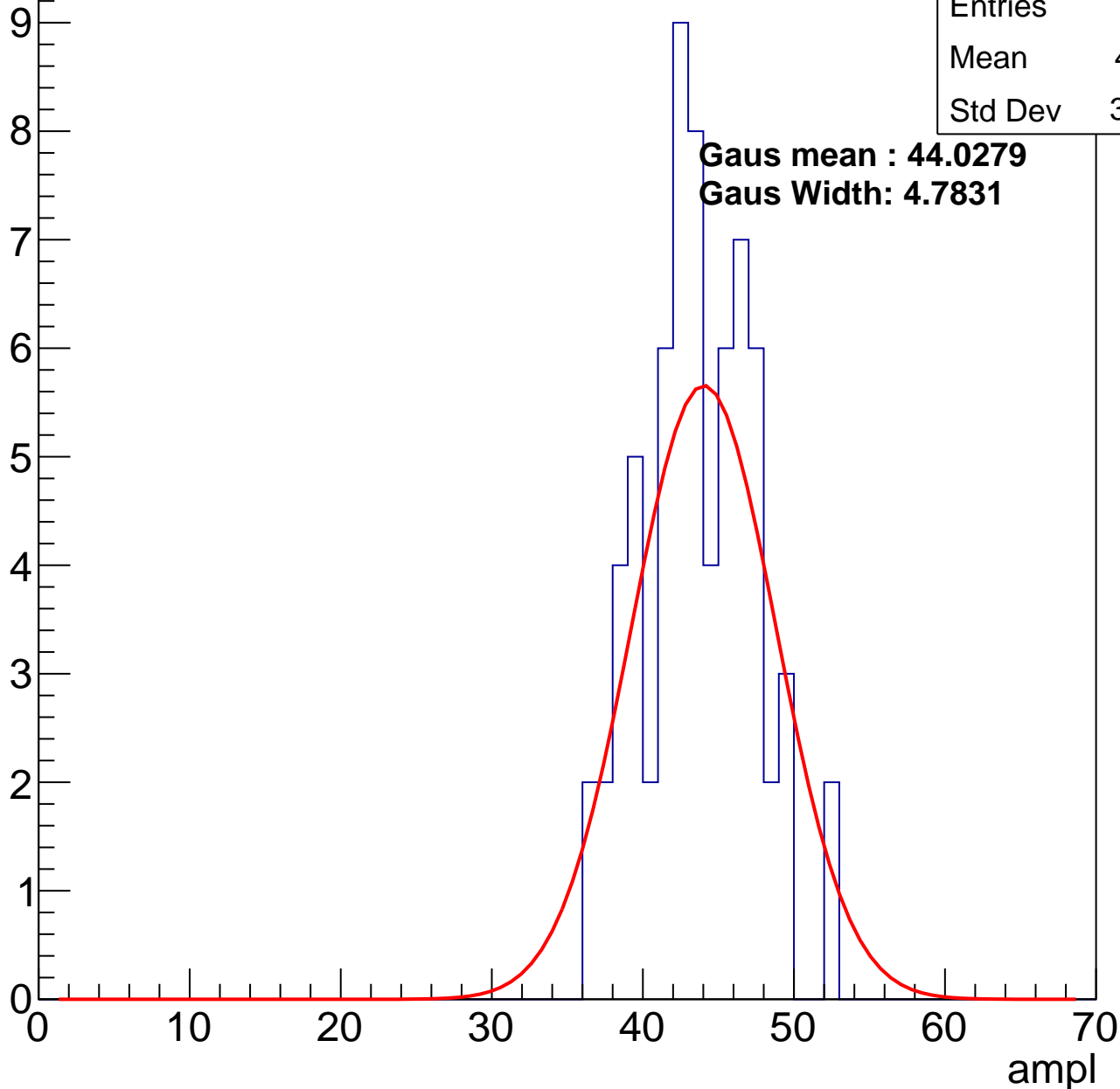
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	43.21
Std Dev	3.648

**Gaus mean : 44.0279**

**Gaus Width: 4.7831**

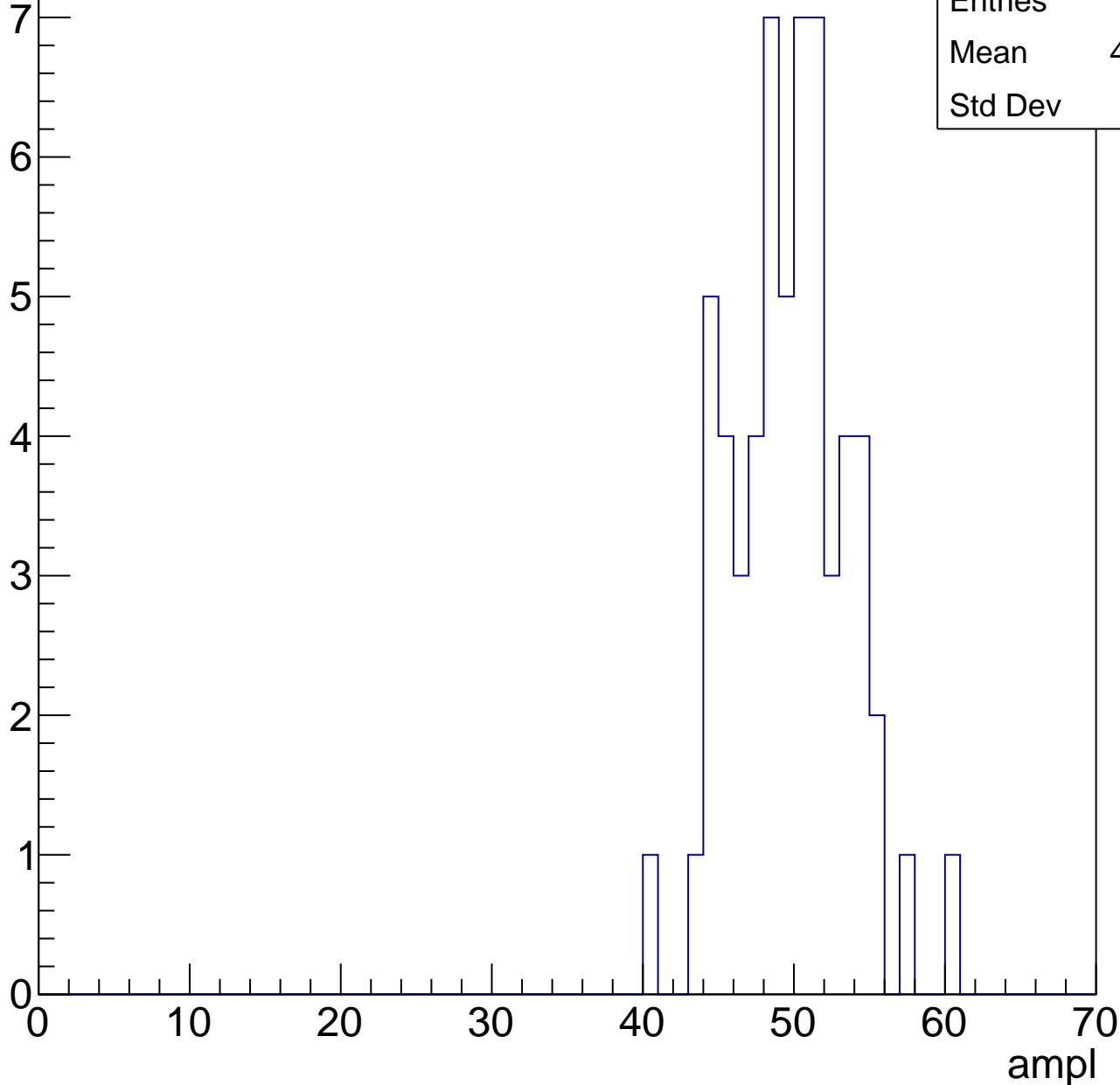


# B1L102S, U16-ch53, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	49.29
Std Dev	3.76

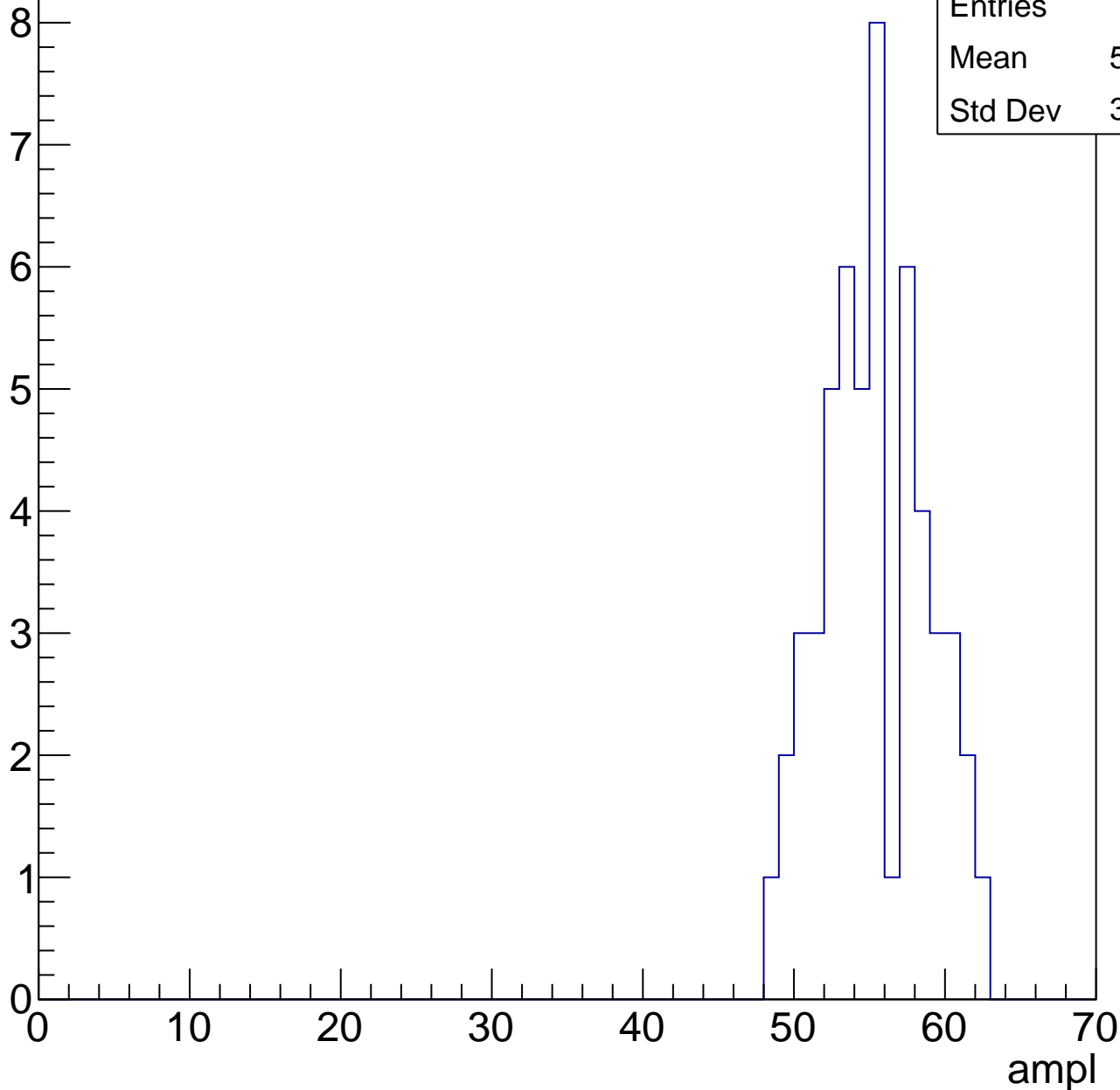


# B1L102S, U16-ch53, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

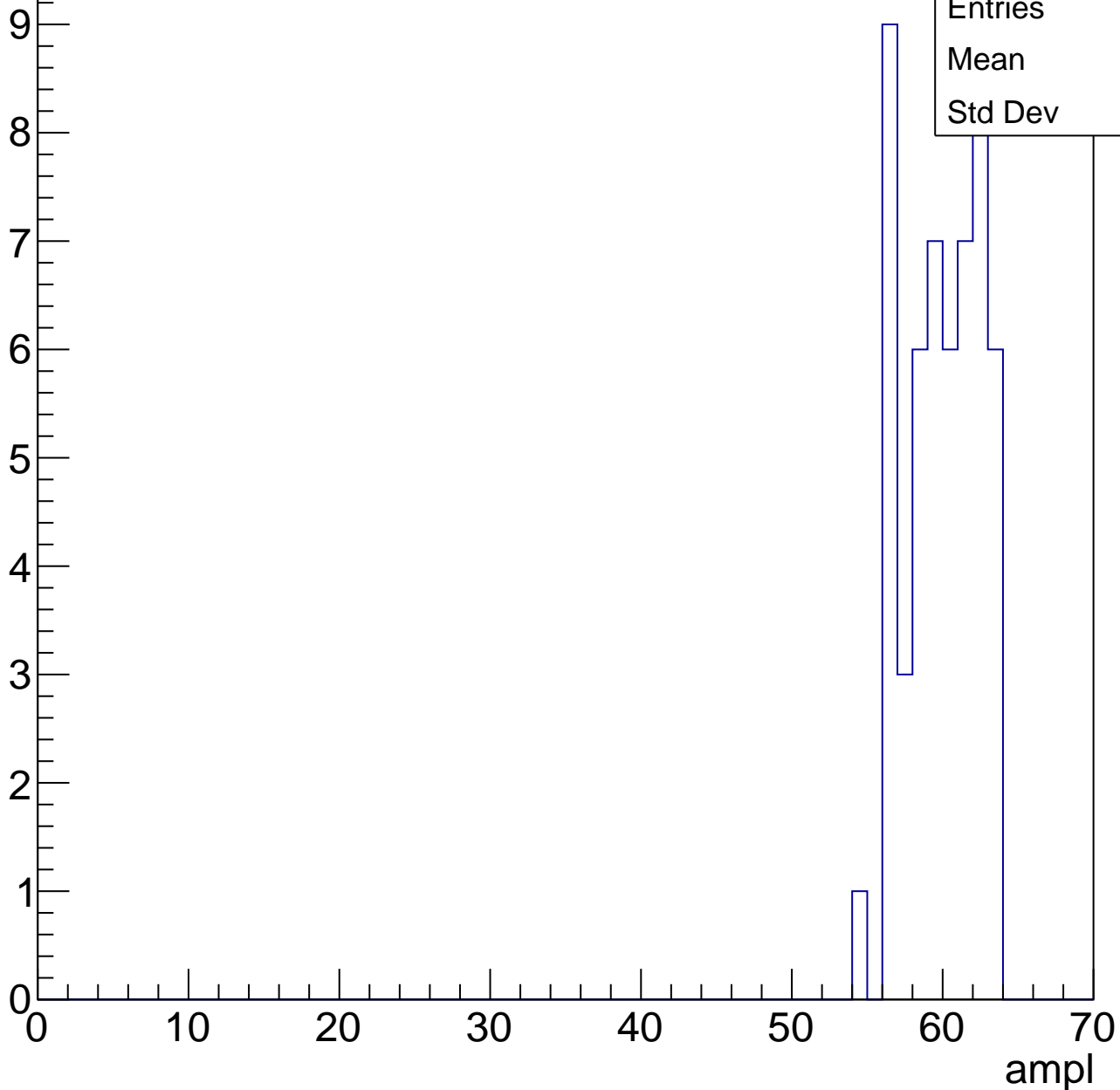
Entries	53
Mean	54.87
Std Dev	3.426



# B1L102S, U16-ch53, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

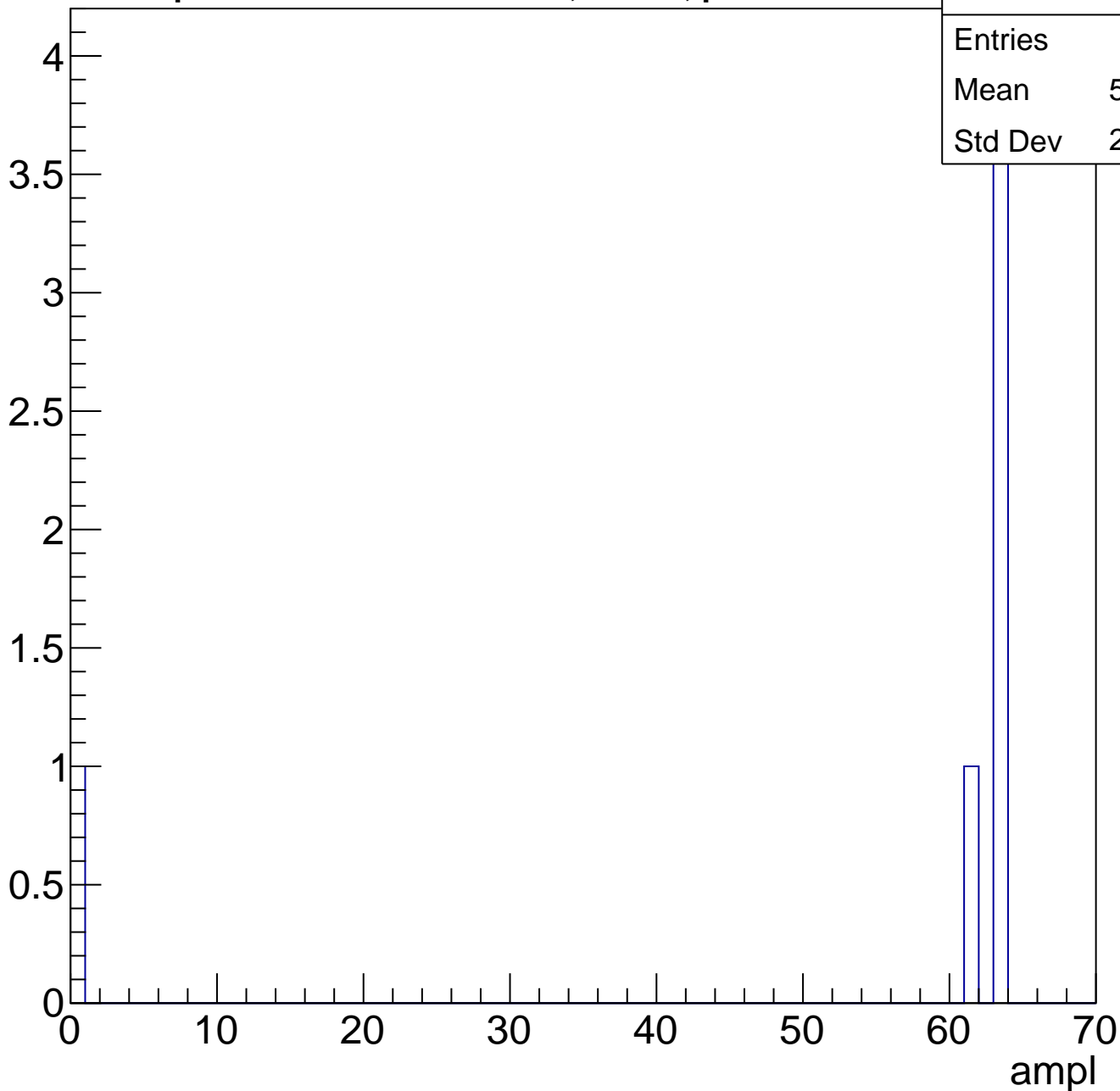
Entry



# B1L102S, U16-ch53, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

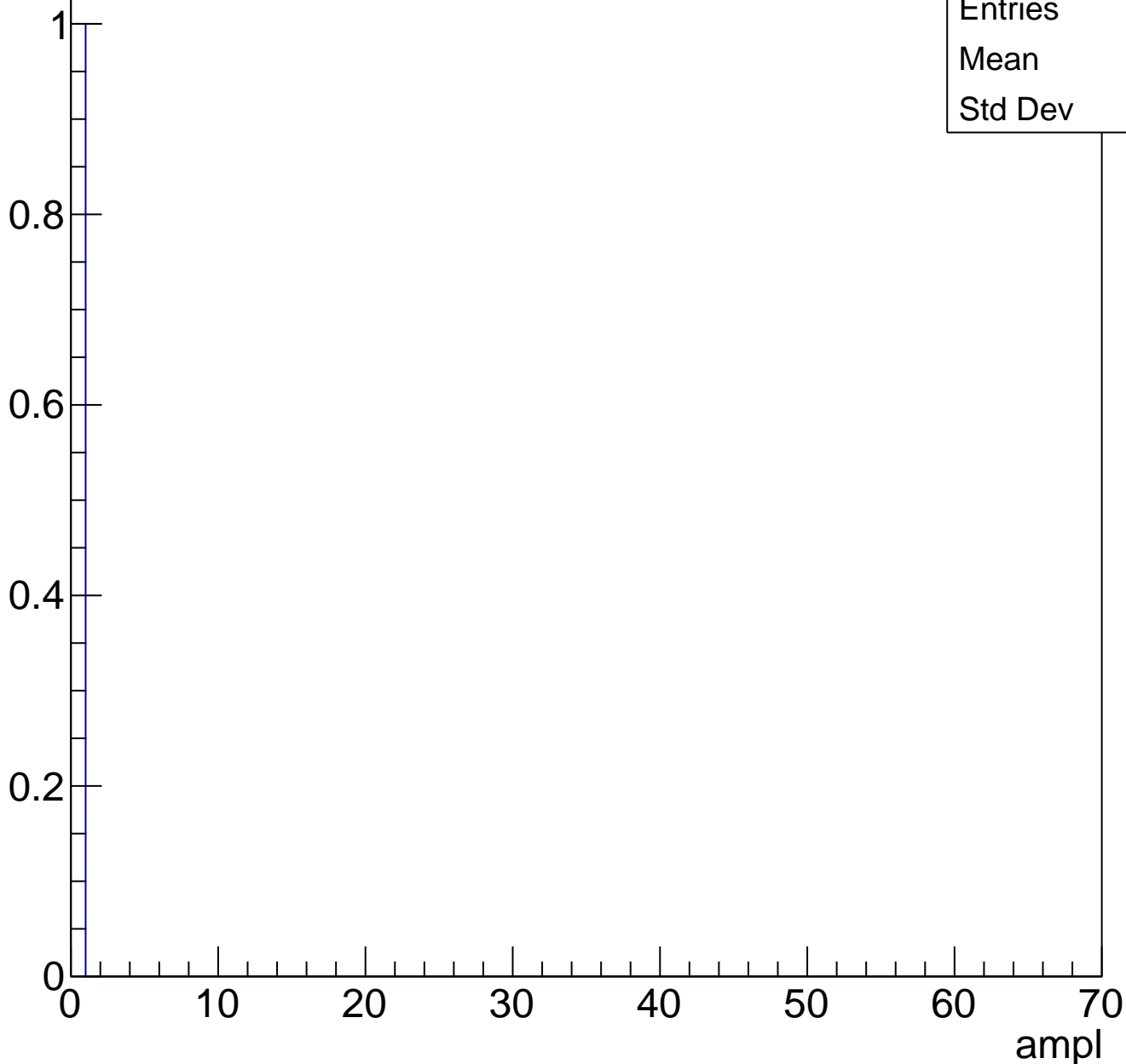




# B1L102S, U16-ch53, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch54, adc0

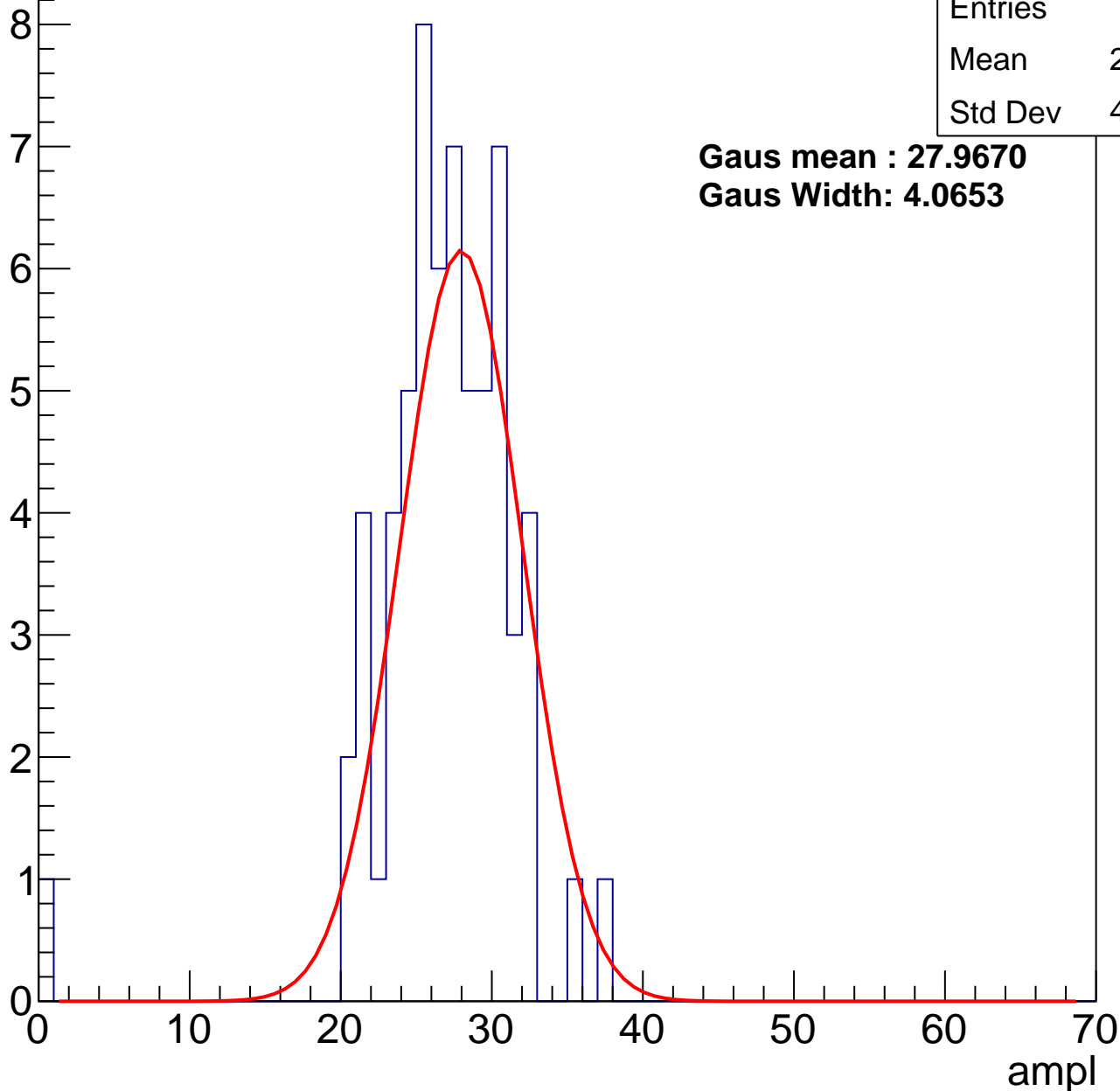
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	26.42
Std Dev	4.876

**Gaus mean : 27.9670**

**Gaus Width: 4.0653**



# B1L102S, U16-ch54, adc1

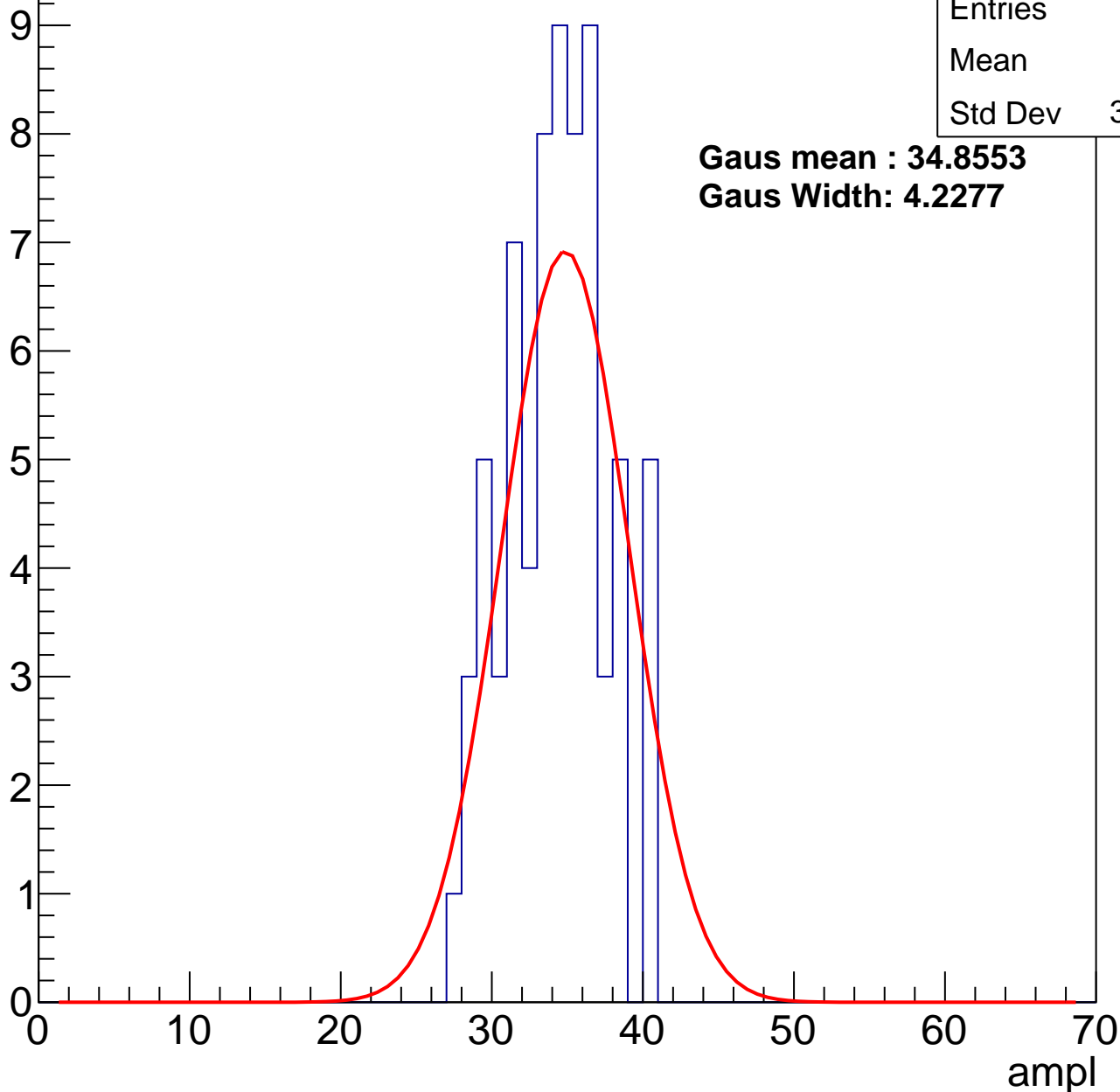
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	33.8
Std Dev	3.263

**Gaus mean : 34.8553**

**Gaus Width: 4.2277**



# B1L102S, U16-ch54, adc2

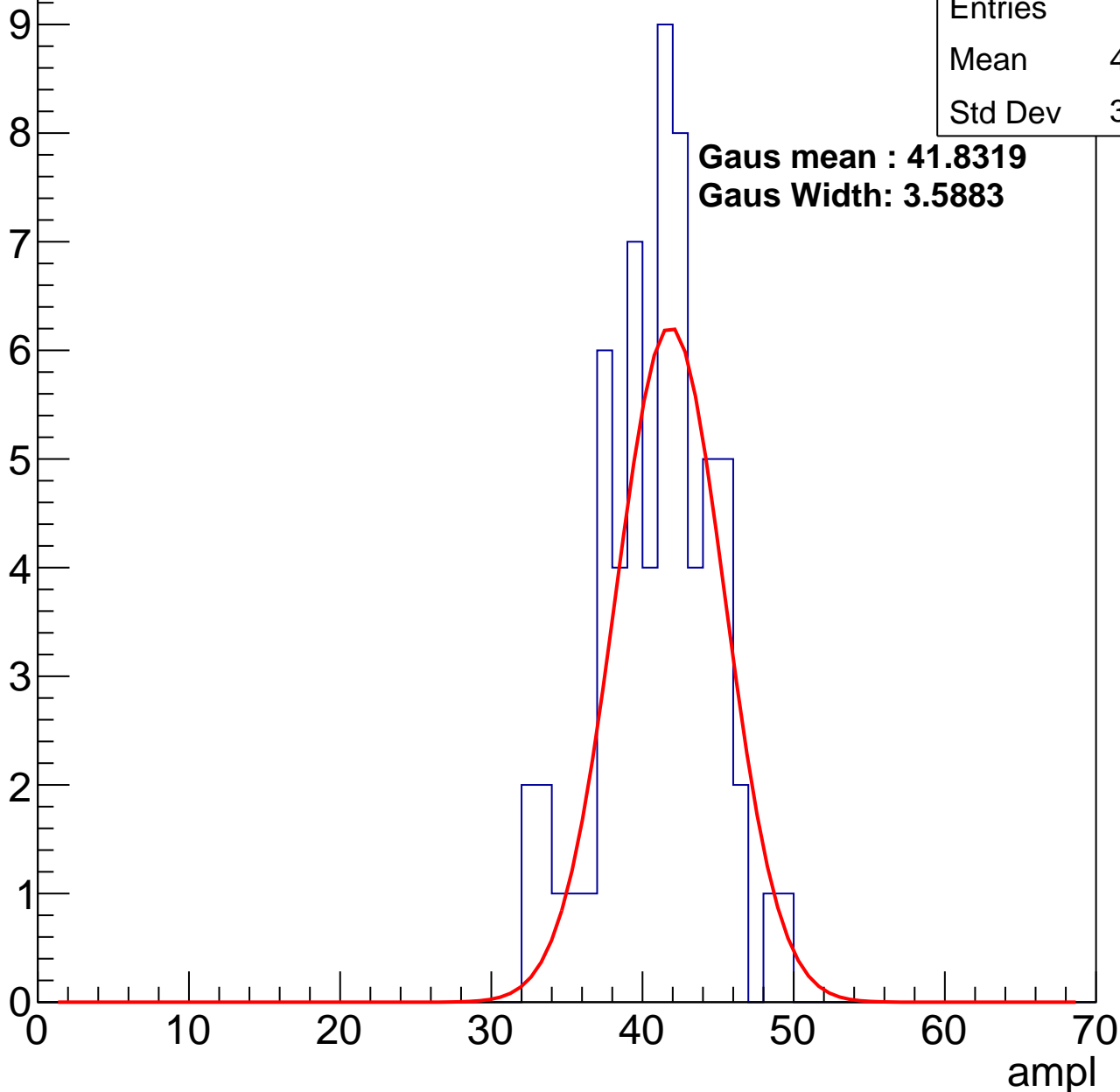
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	40.52
Std Dev	3.698

**Gaus mean : 41.8319**

**Gaus Width: 3.5883**



# B1L102S, U16-ch54, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

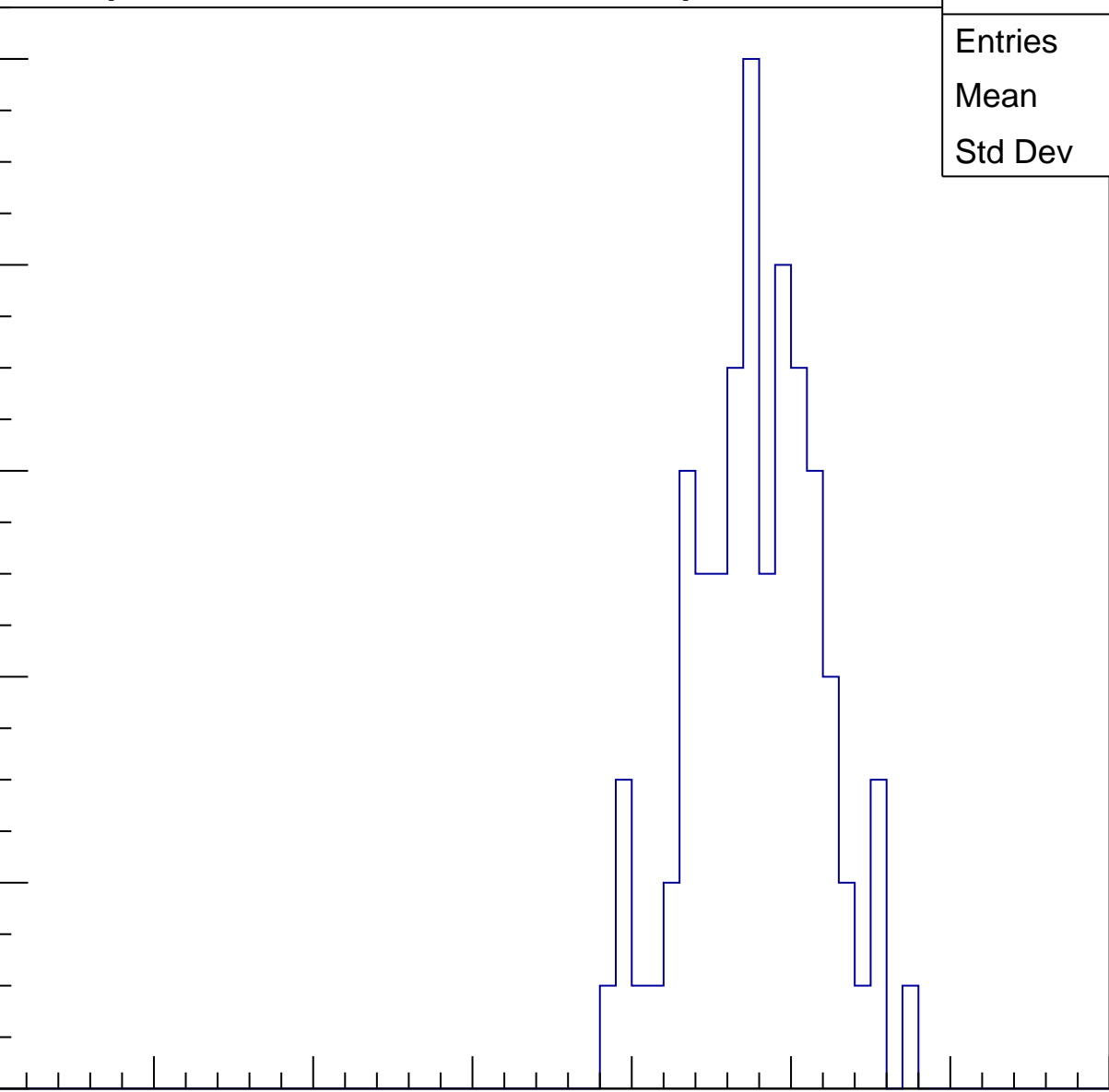
Entries	78
Mean	47.35
Std Dev	4.044

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

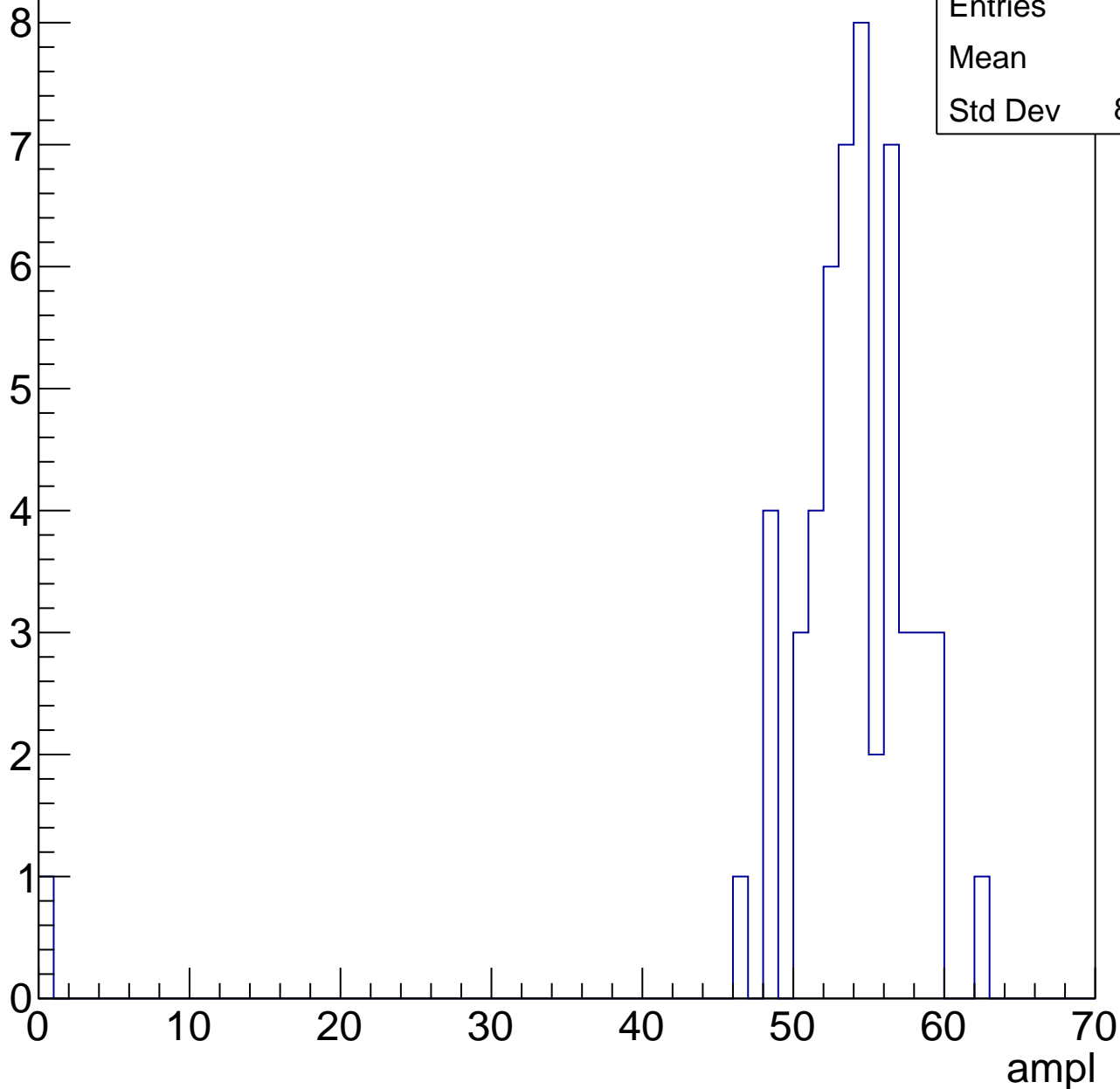


# B1L102S, U16-ch54, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	52.7
Std Dev	8.001



# B1L102S, U16-ch54, adc5

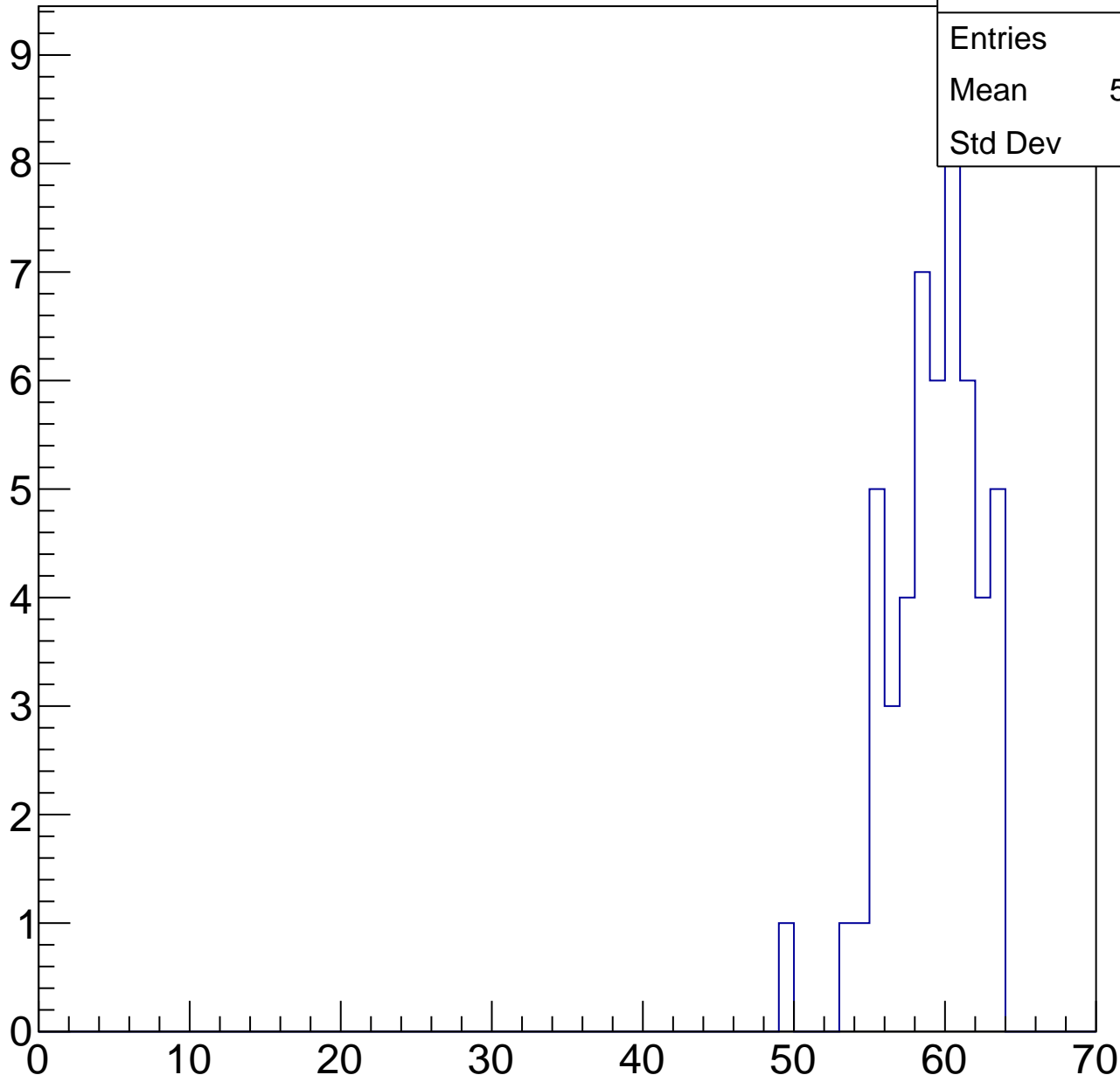
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	52
Mean	58.77
Std Dev	2.9

ampl

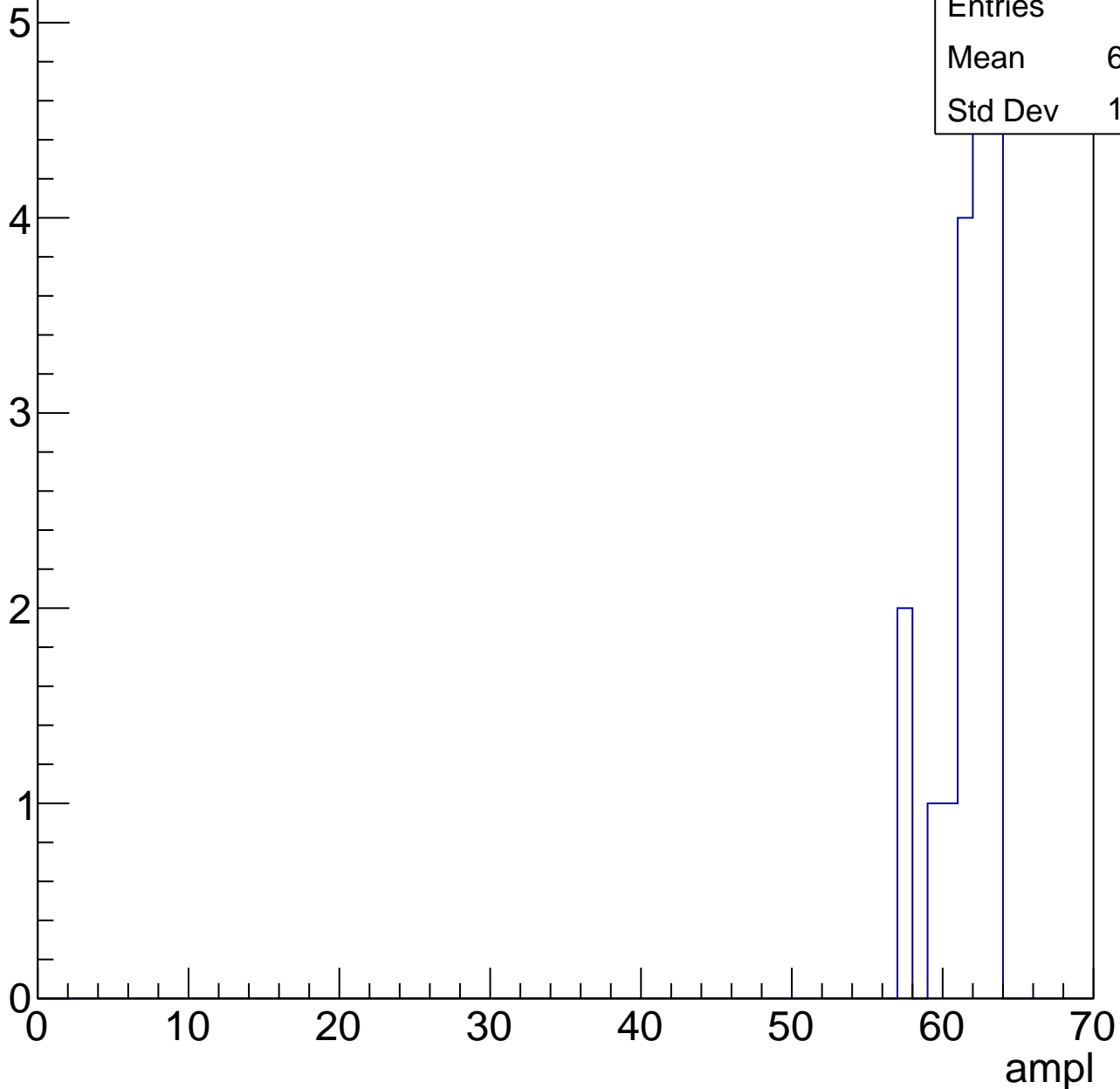


# B1L102S, U16-ch54, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	18
Mean	61.22
Std Dev	1.843





# B1L102S, U16-ch54, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch55, adc0

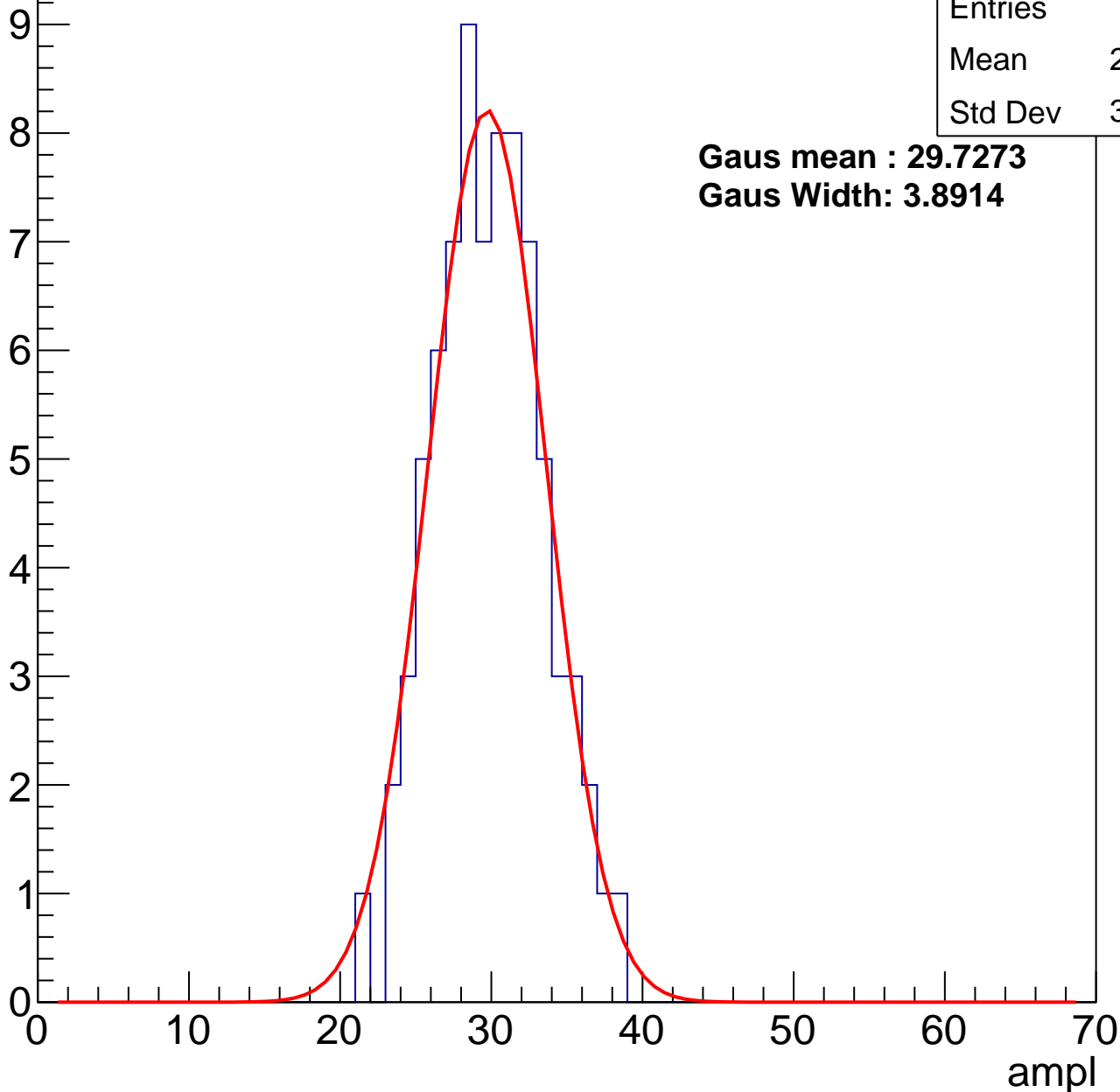
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	29.42
Std Dev	3.539

**Gaus mean : 29.7273**

**Gaus Width: 3.8914**



# B1L102S, U16-ch55, adc1

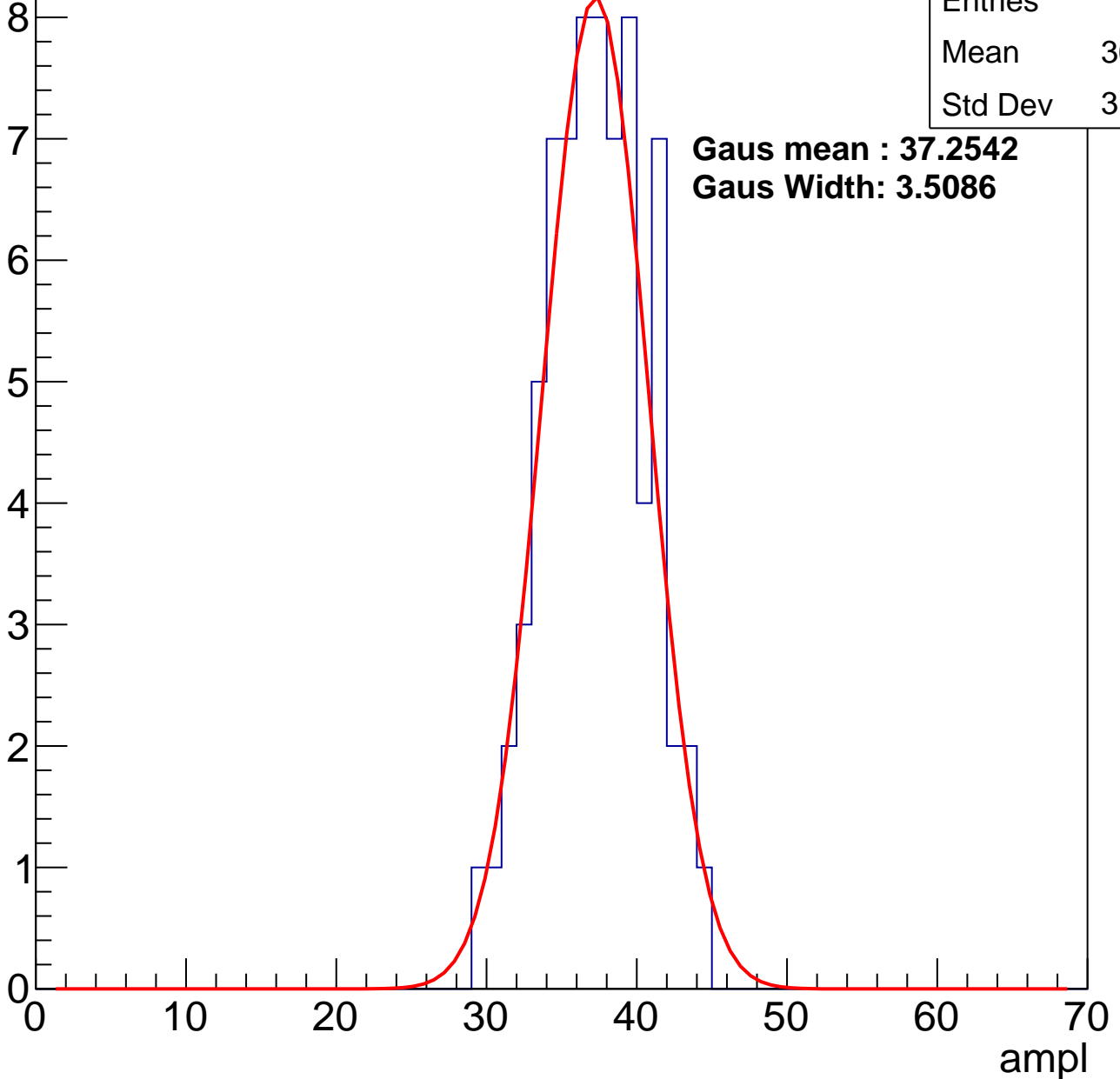
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	36.82
Std Dev	3.299

**Gaus mean : 37.2542**

**Gaus Width: 3.5086**



# B1L102S, U16-ch55, adc2

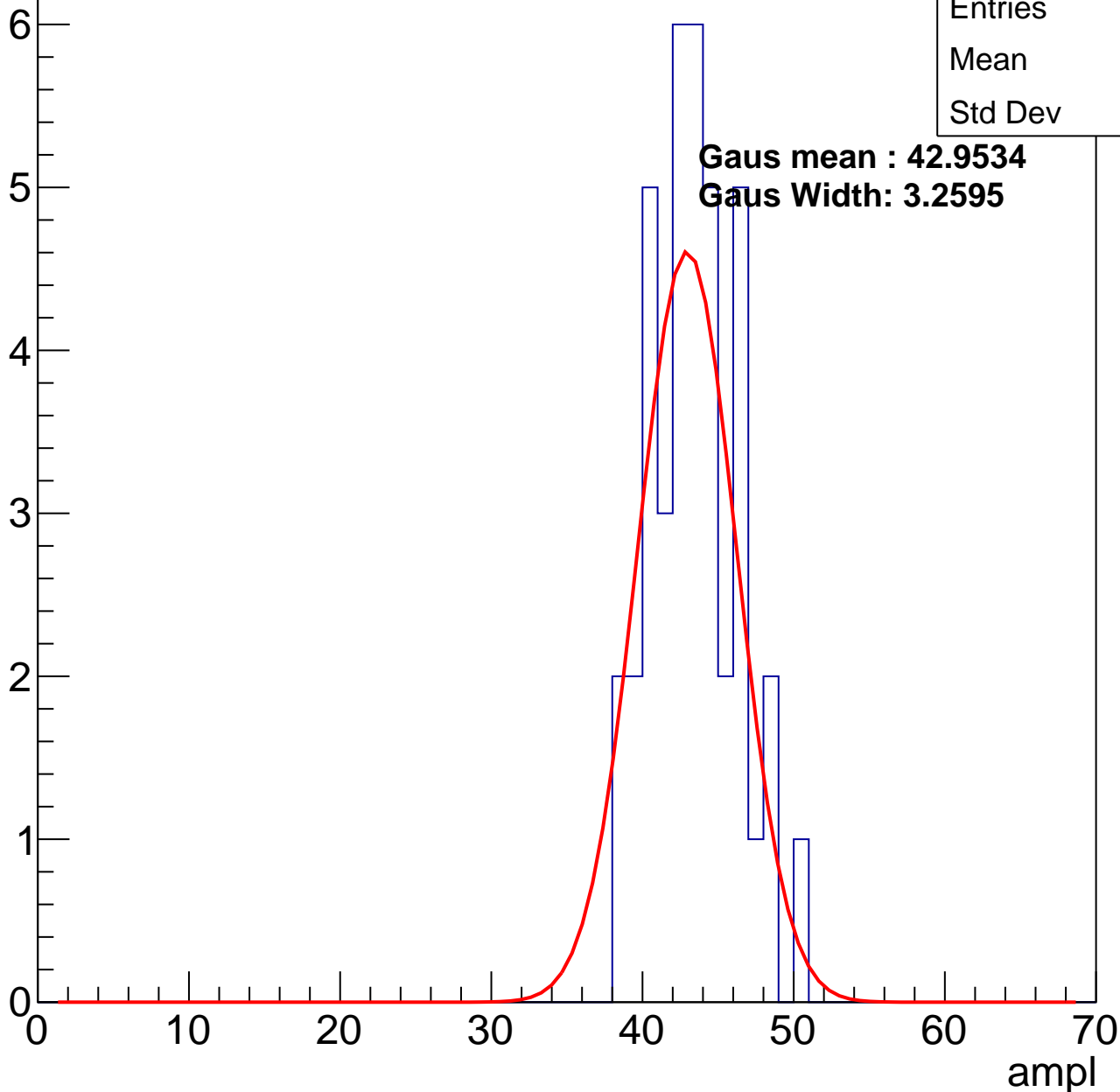
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	43
Std Dev	2.82

**Gaus mean : 42.9534**

**Gaus Width: 3.2595**

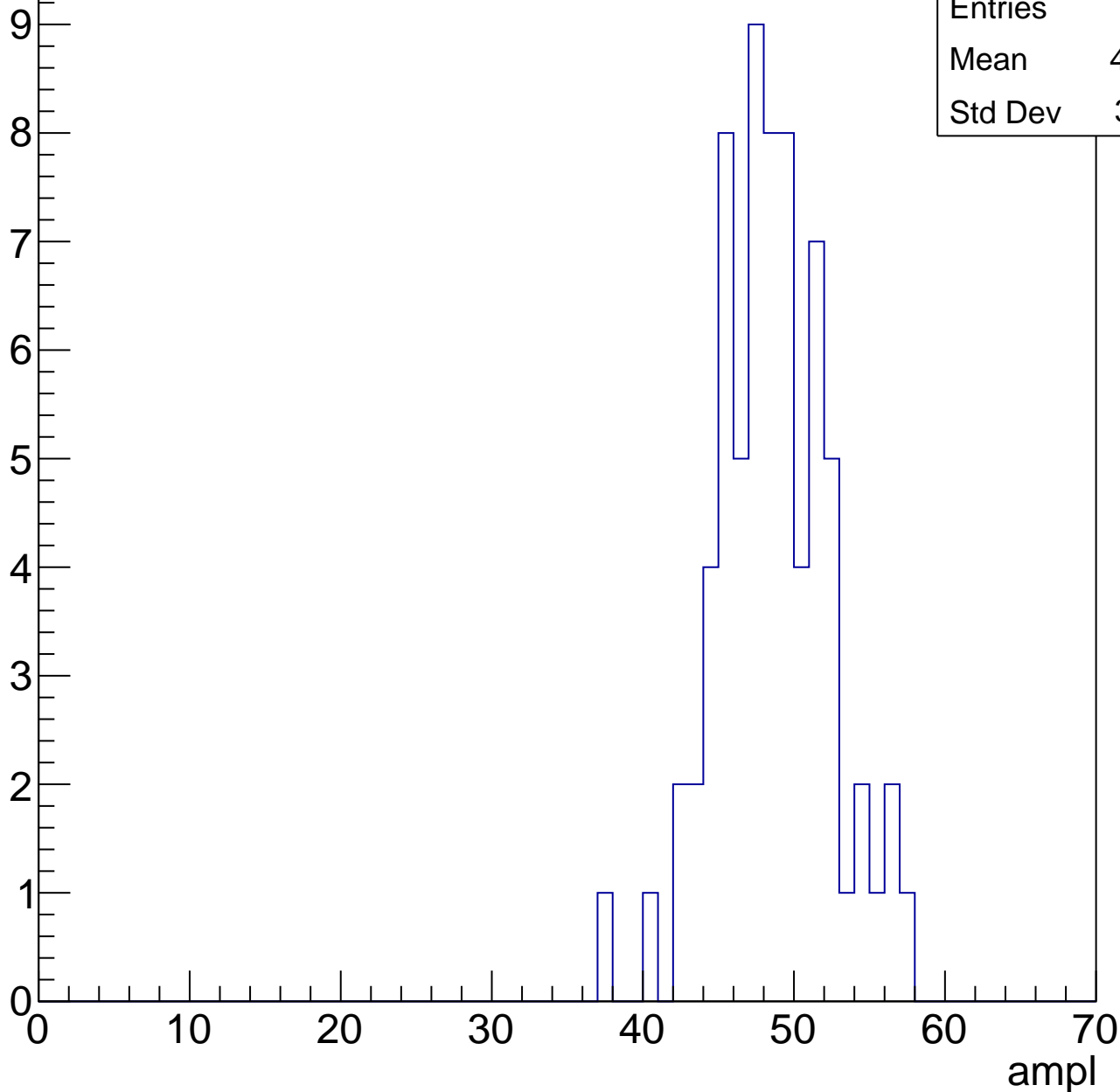


# B1L102S, U16-ch55, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

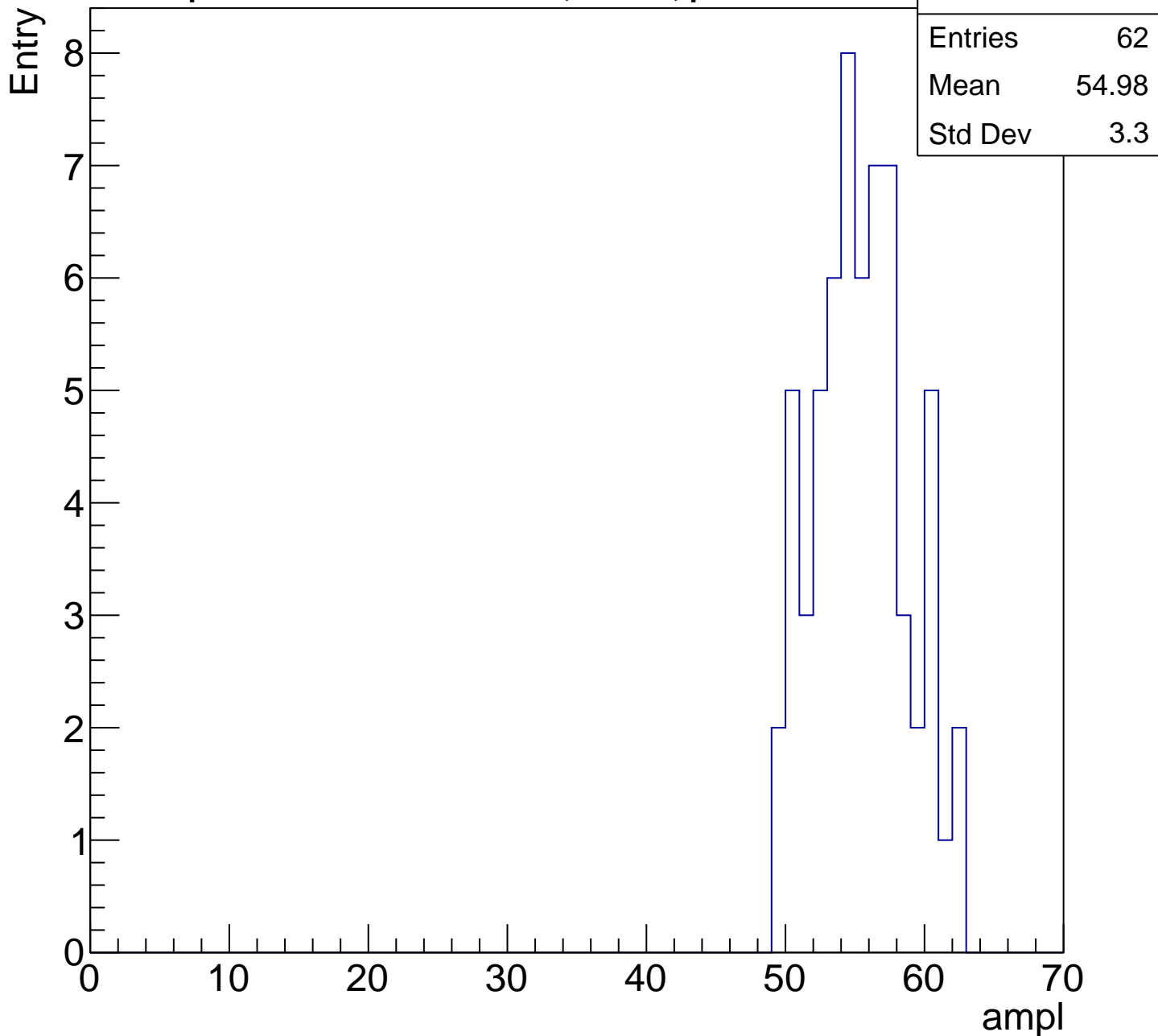
Entry

Entries	71
Mean	48.08
Std Dev	3.741



# B1L102S, U16-ch55, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U16-ch55, adc5

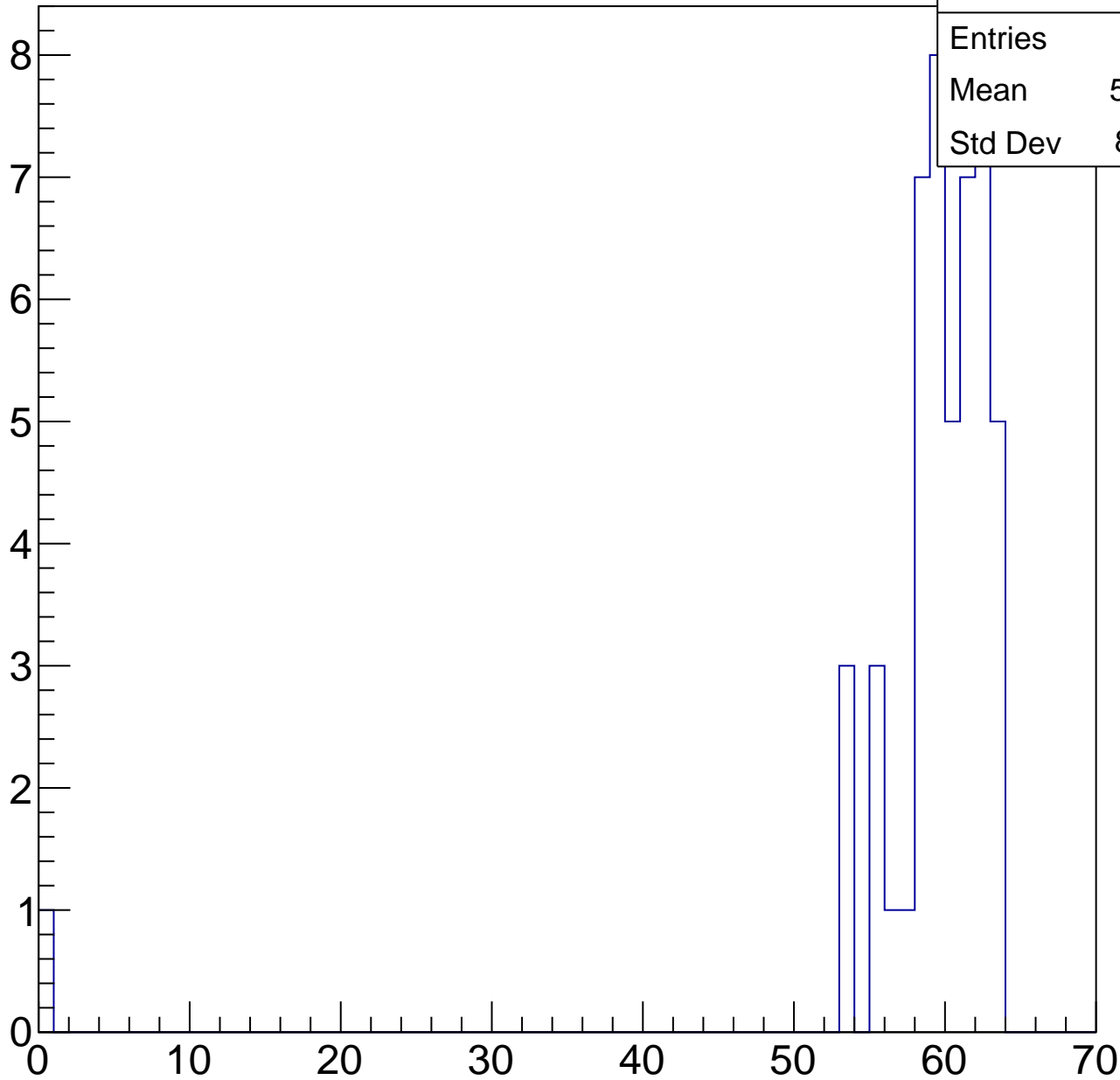
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	49
Mean	58.22
Std Dev	8.821

ampl

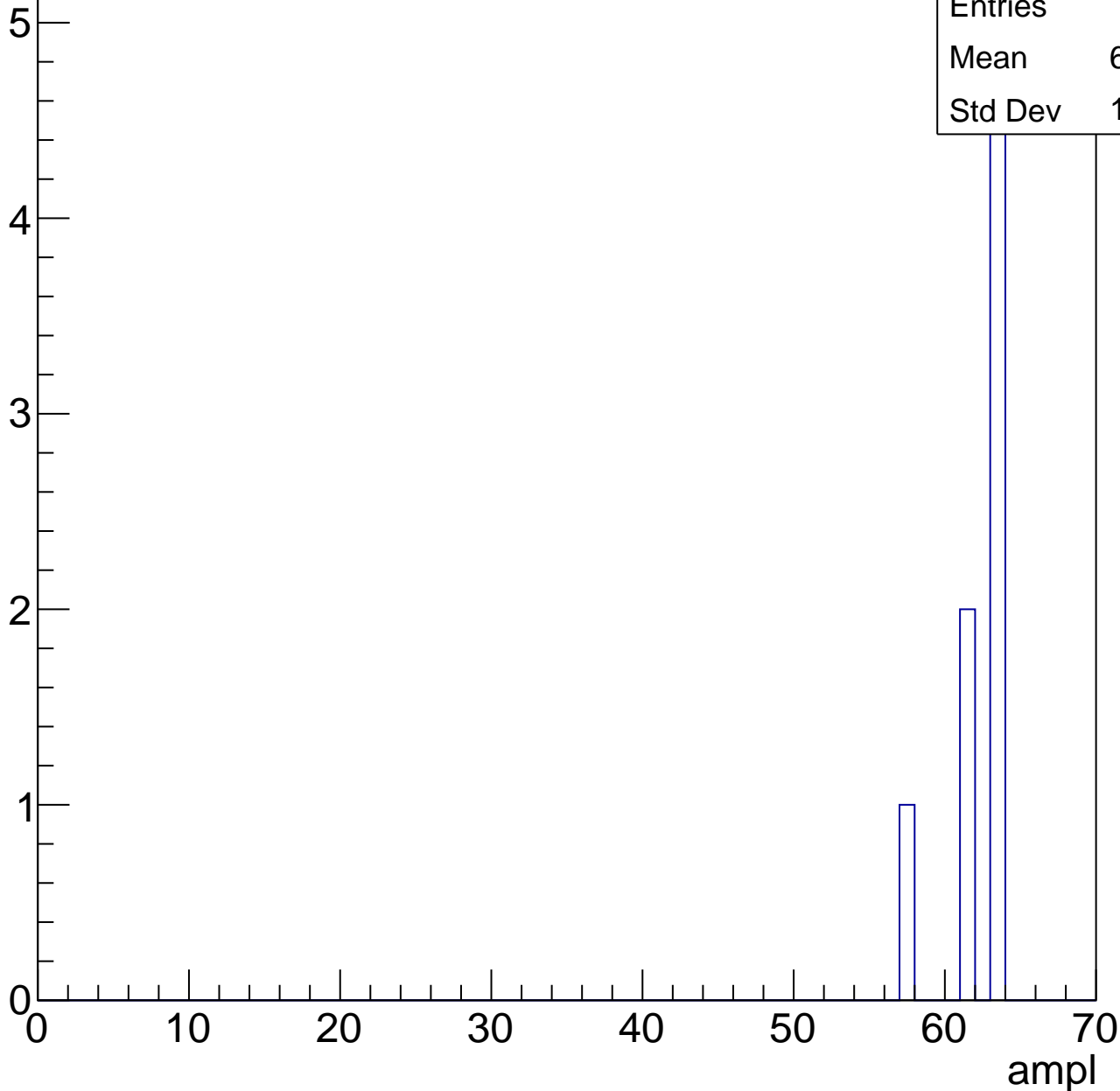


# B1L102S, U16-ch55, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	8
Mean	61.75
Std Dev	1.984





# B1L102S, U16-ch55, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U16-ch56, adc0

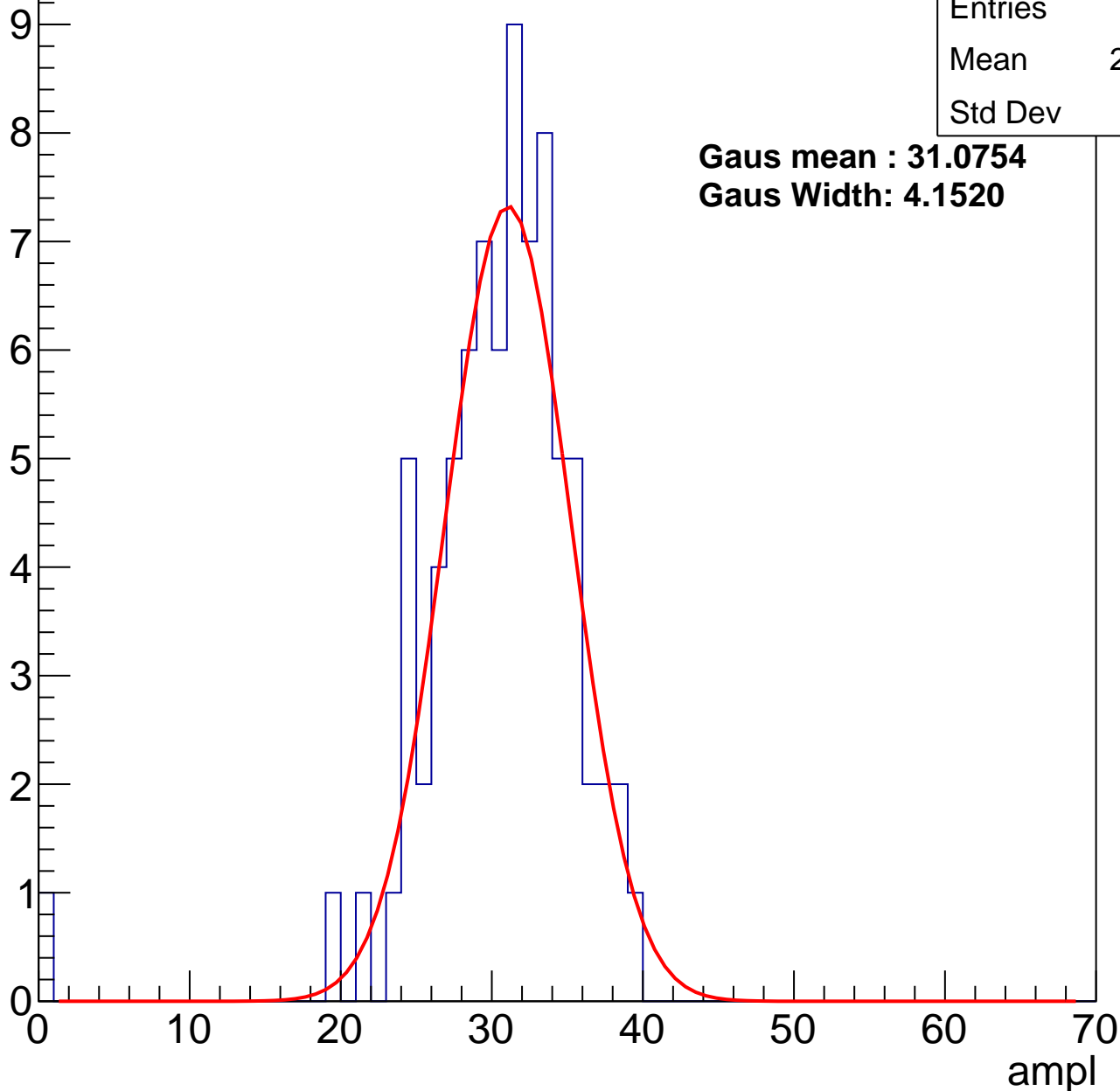
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	29.95
Std Dev	5.26

**Gaus mean : 31.0754**

**Gaus Width: 4.1520**



# B1L102S, U16-ch56, adc1

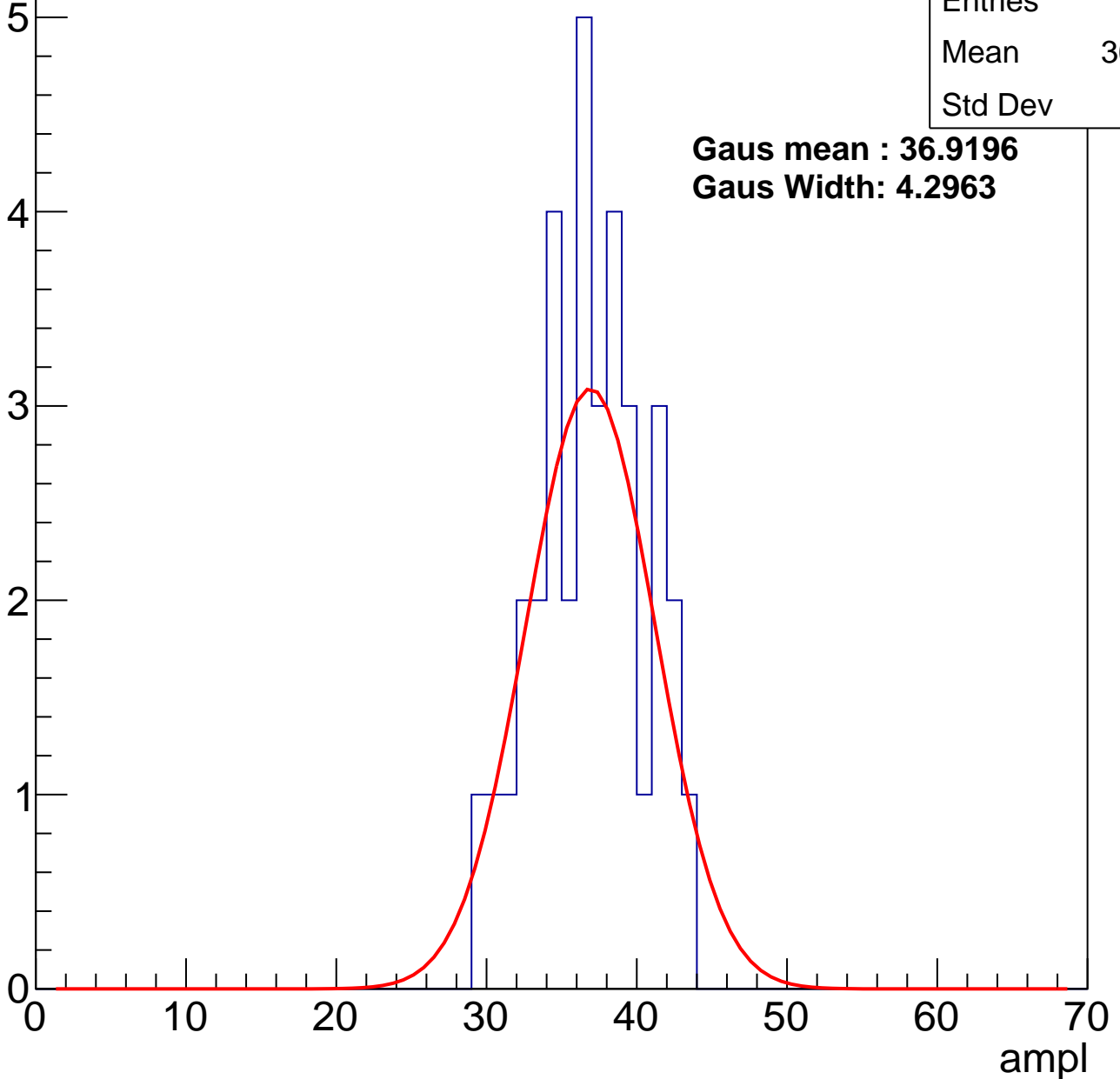
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	35
Mean	36.46
Std Dev	3.5

**Gaus mean : 36.9196**

**Gaus Width: 4.2963**



# B1L102S, U16-ch56, adc2

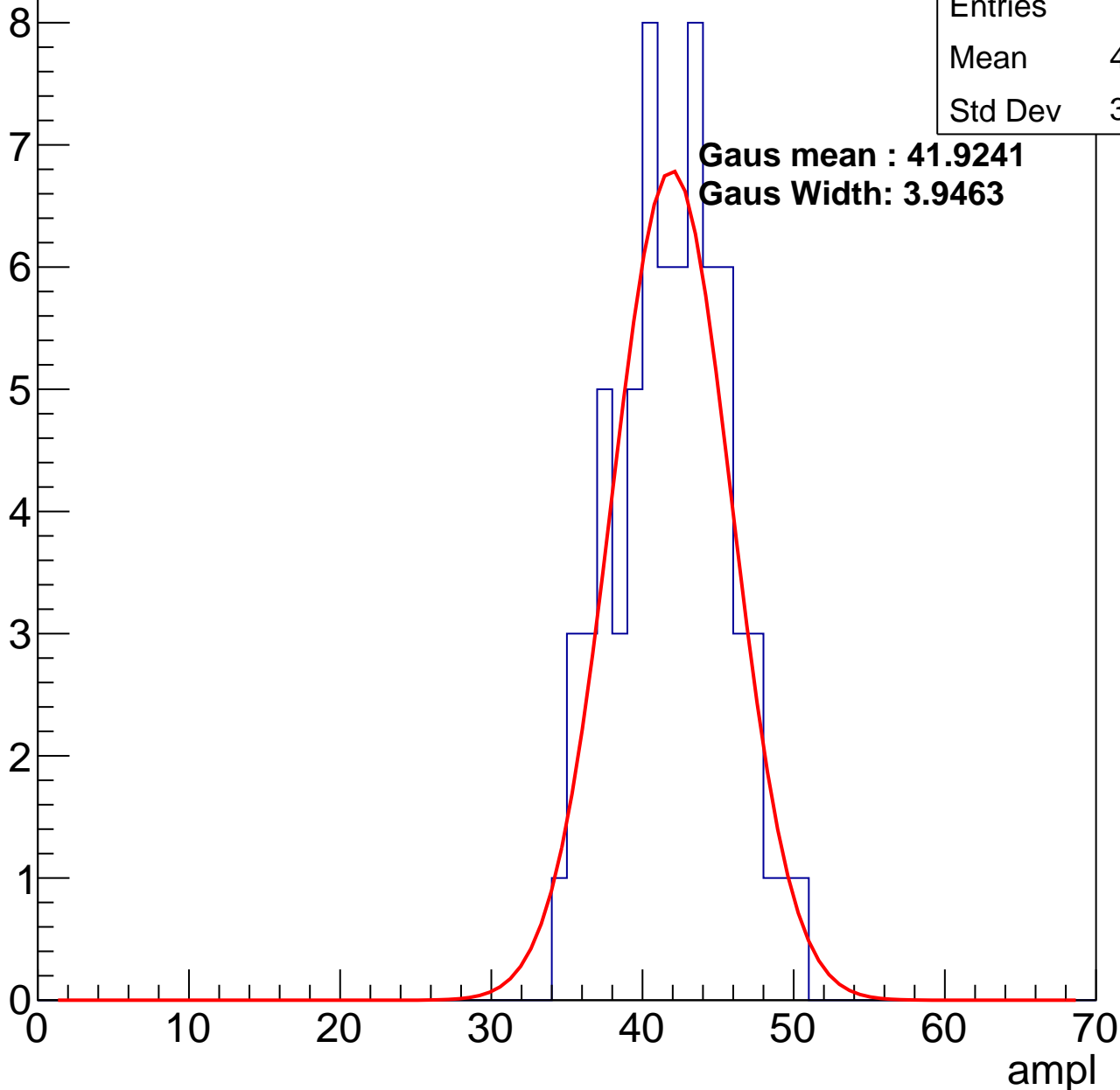
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	41.49
Std Dev	3.642

**Gaus mean : 41.9241**

**Gaus Width: 3.9463**

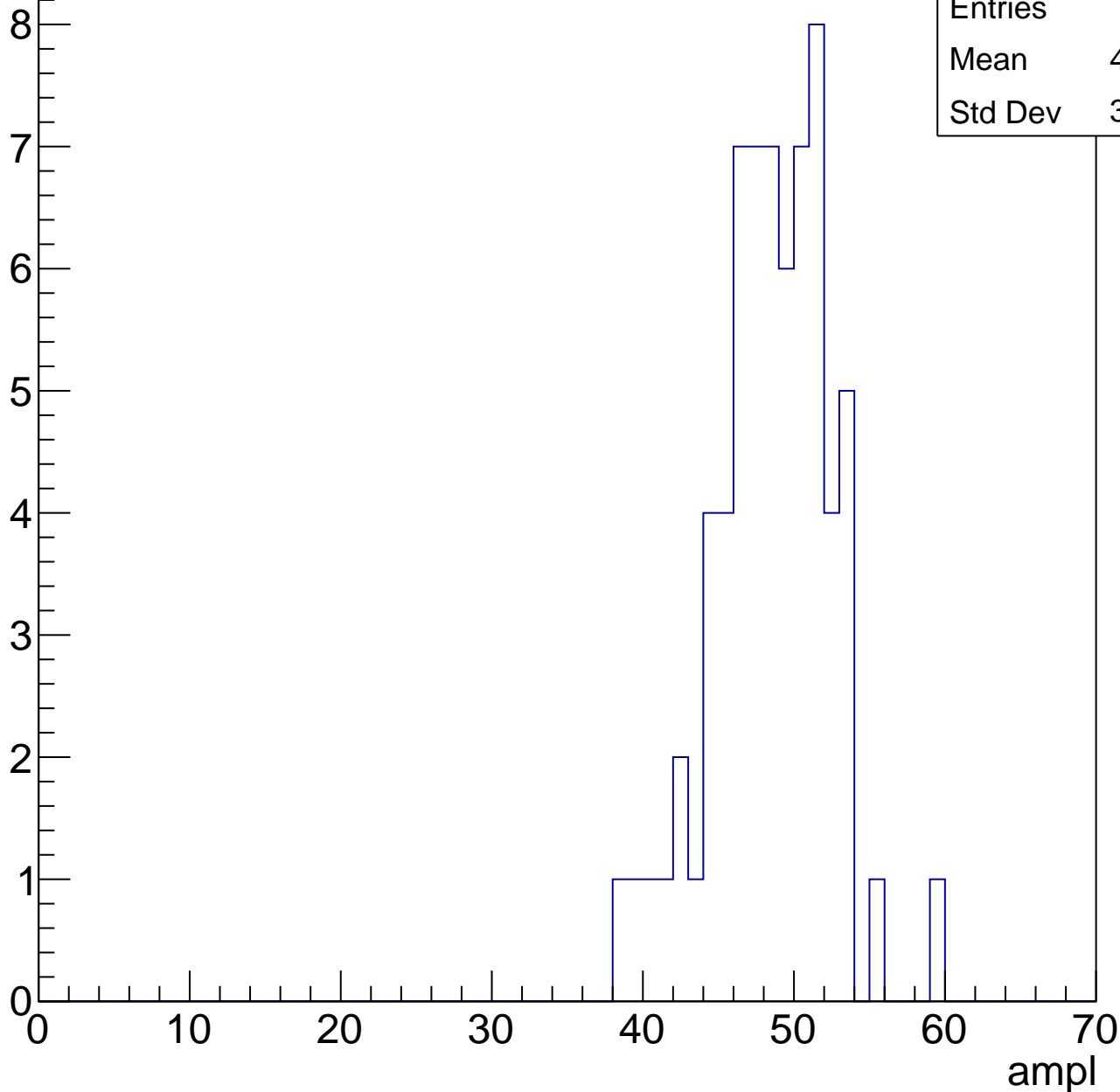


# B1L102S, U16-ch56, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	48.04
Std Dev	3.817

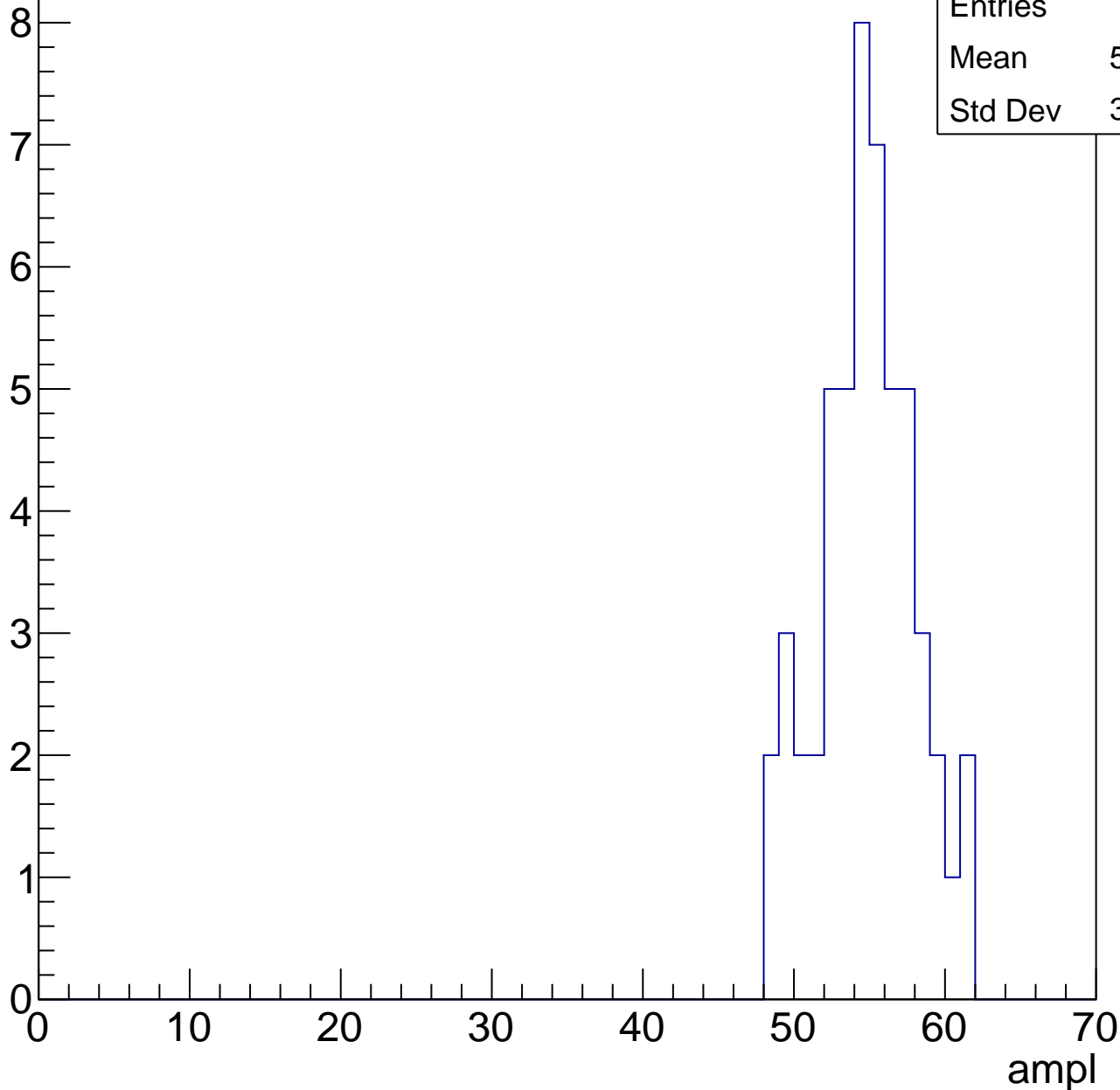


# B1L102S, U16-ch56, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	54.35
Std Dev	3.162

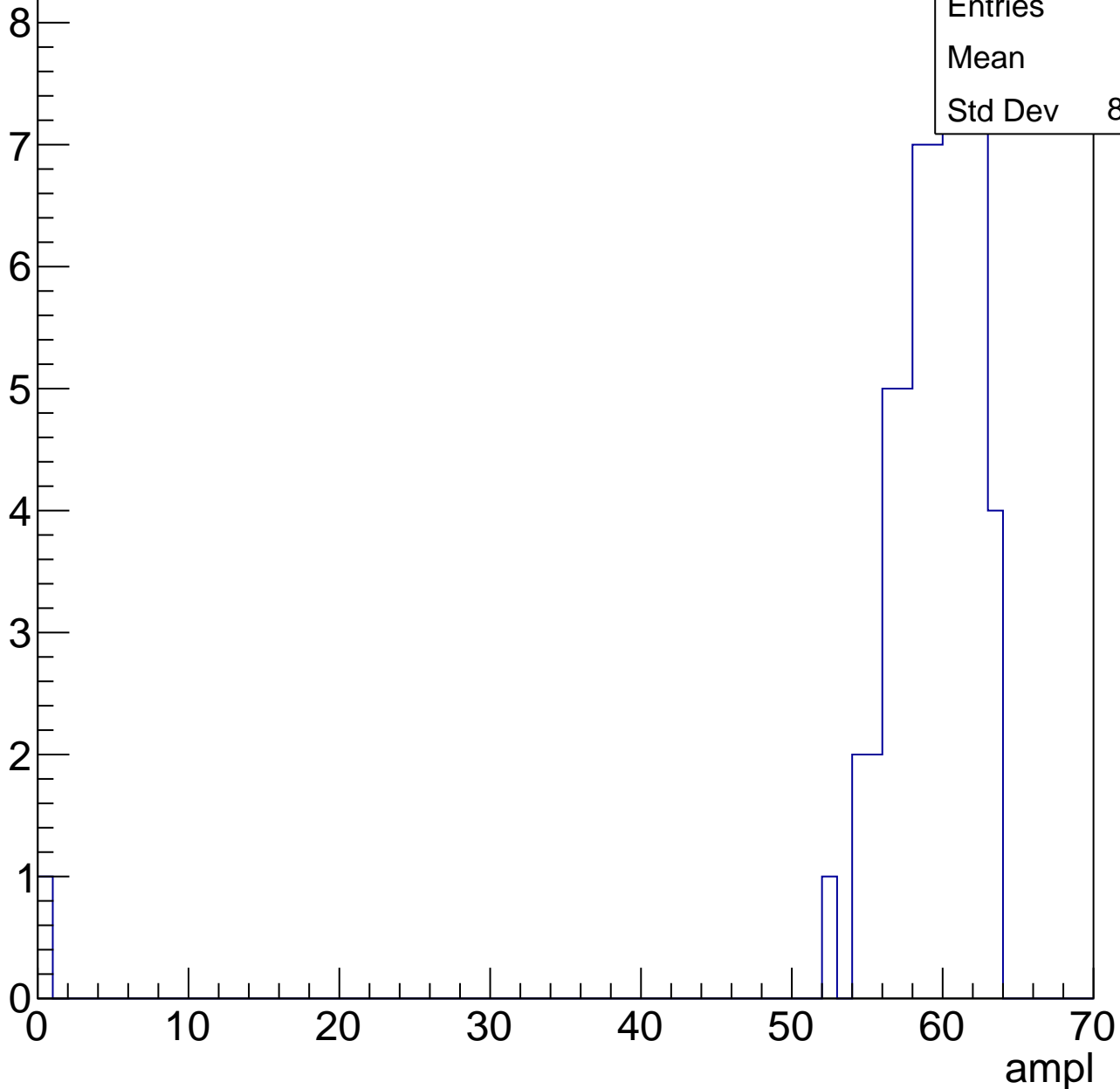


# B1L102S, U16-ch56, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	58.1
Std Dev	8.109

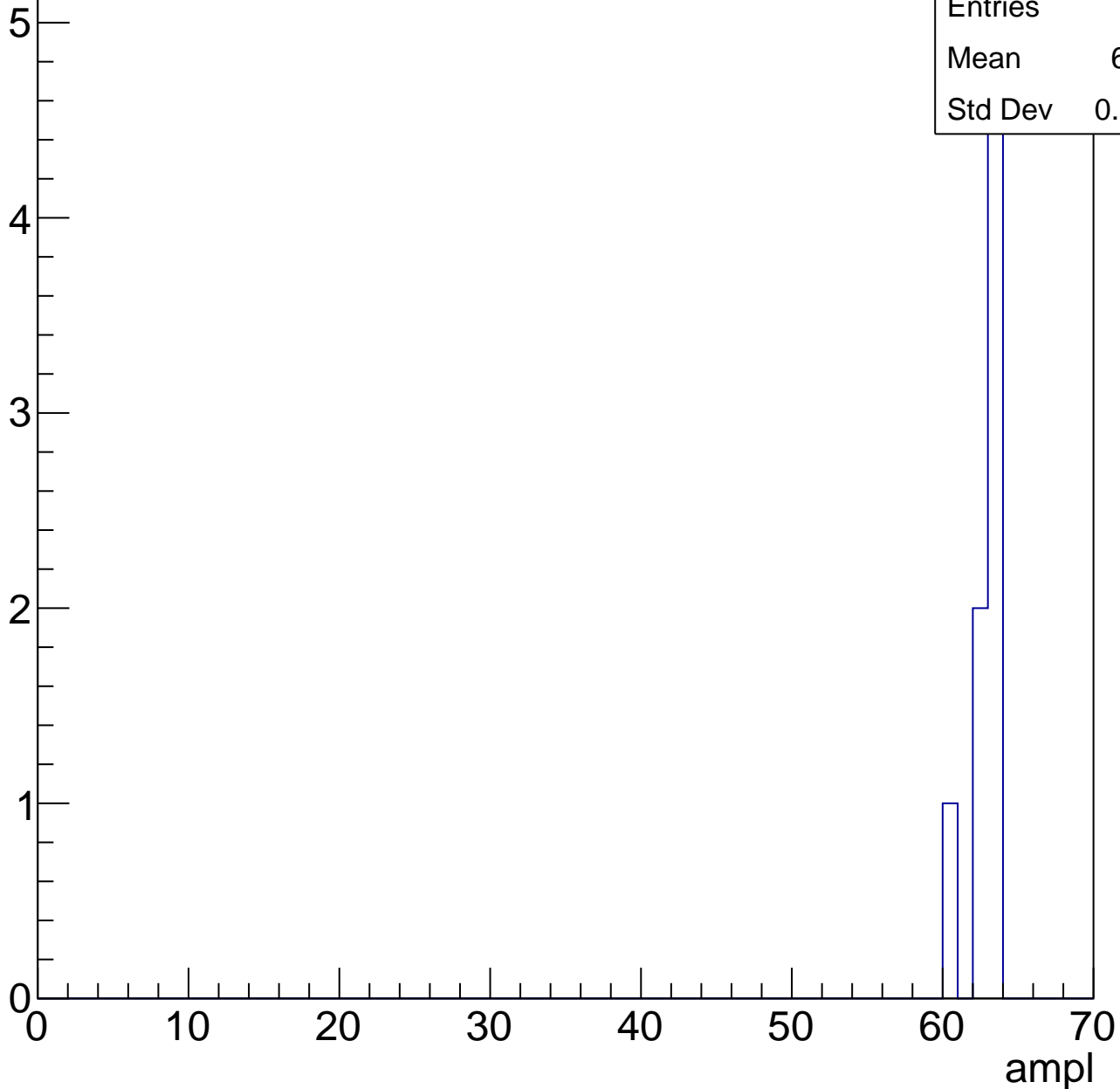


# B1L102S, U16-ch56, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	8
Mean	62.38
Std Dev	0.9922





# B1L102S, U16-ch56, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch57, adc0

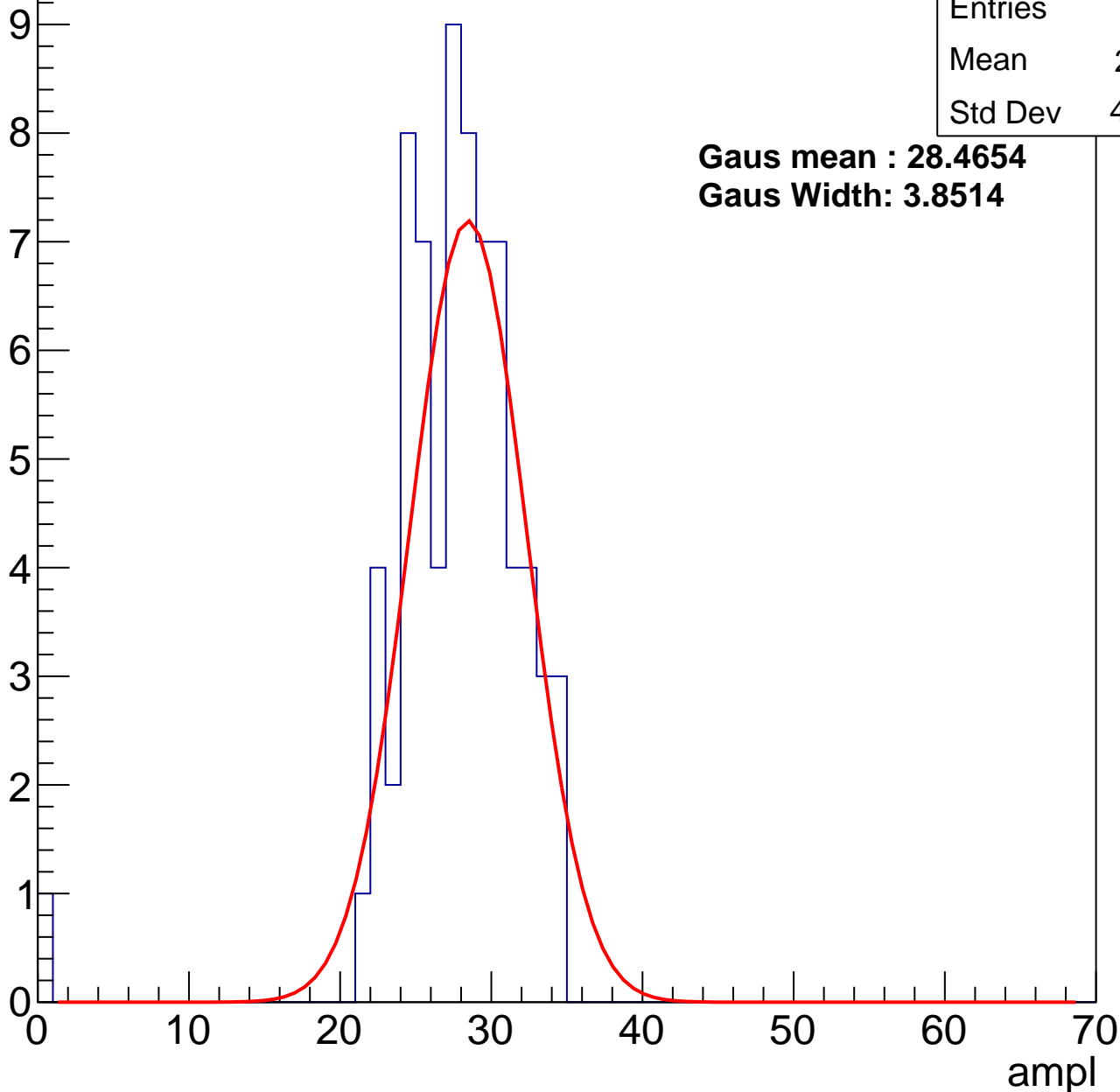
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	27.21
Std Dev	4.588

**Gaus mean : 28.4654**

**Gaus Width: 3.8514**



# B1L102S, U16-ch57, adc1

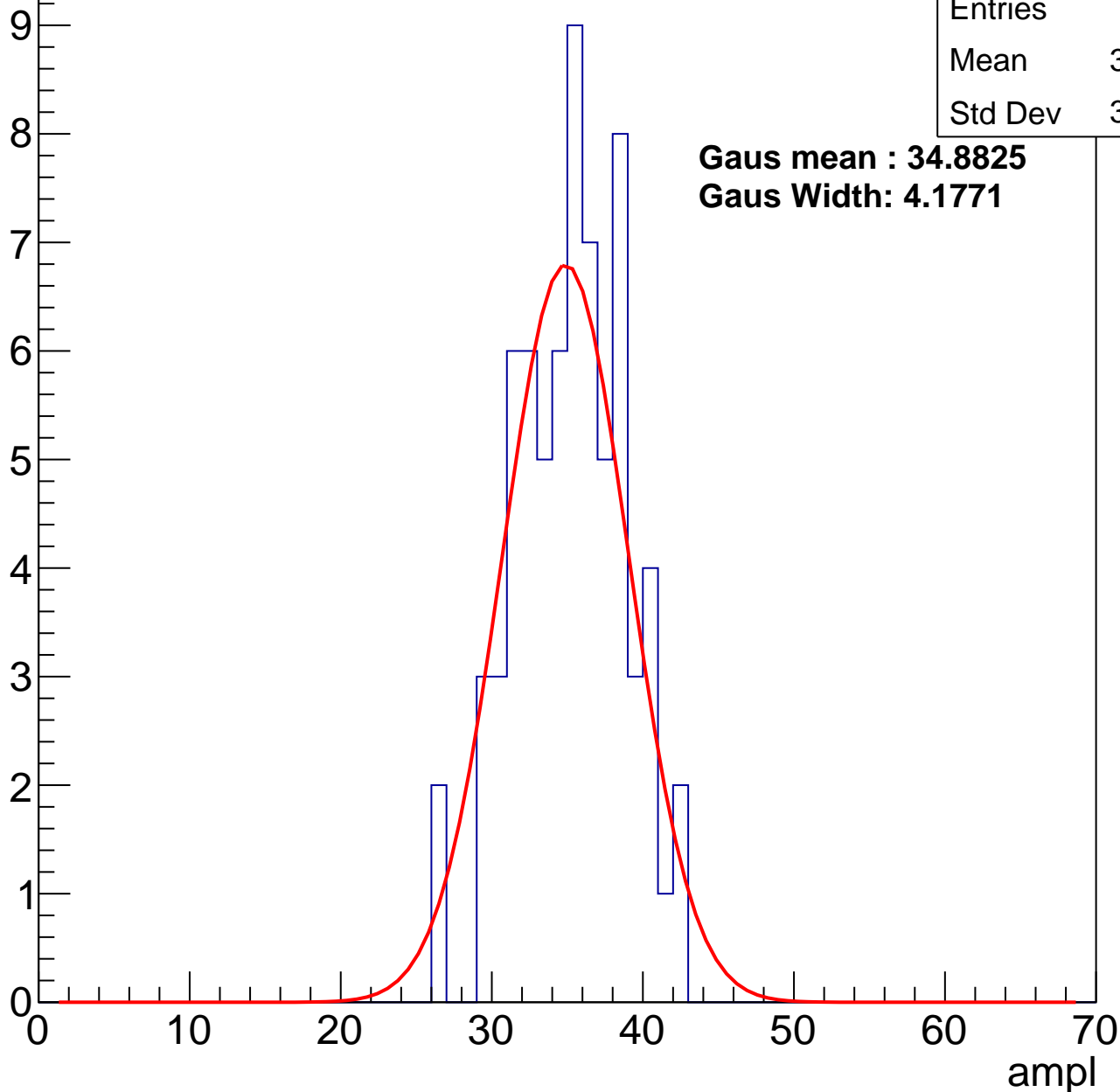
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	34.77
Std Dev	3.582

**Gaus mean : 34.8825**

**Gaus Width: 4.1771**



# B1L102S, U16-ch57, adc2

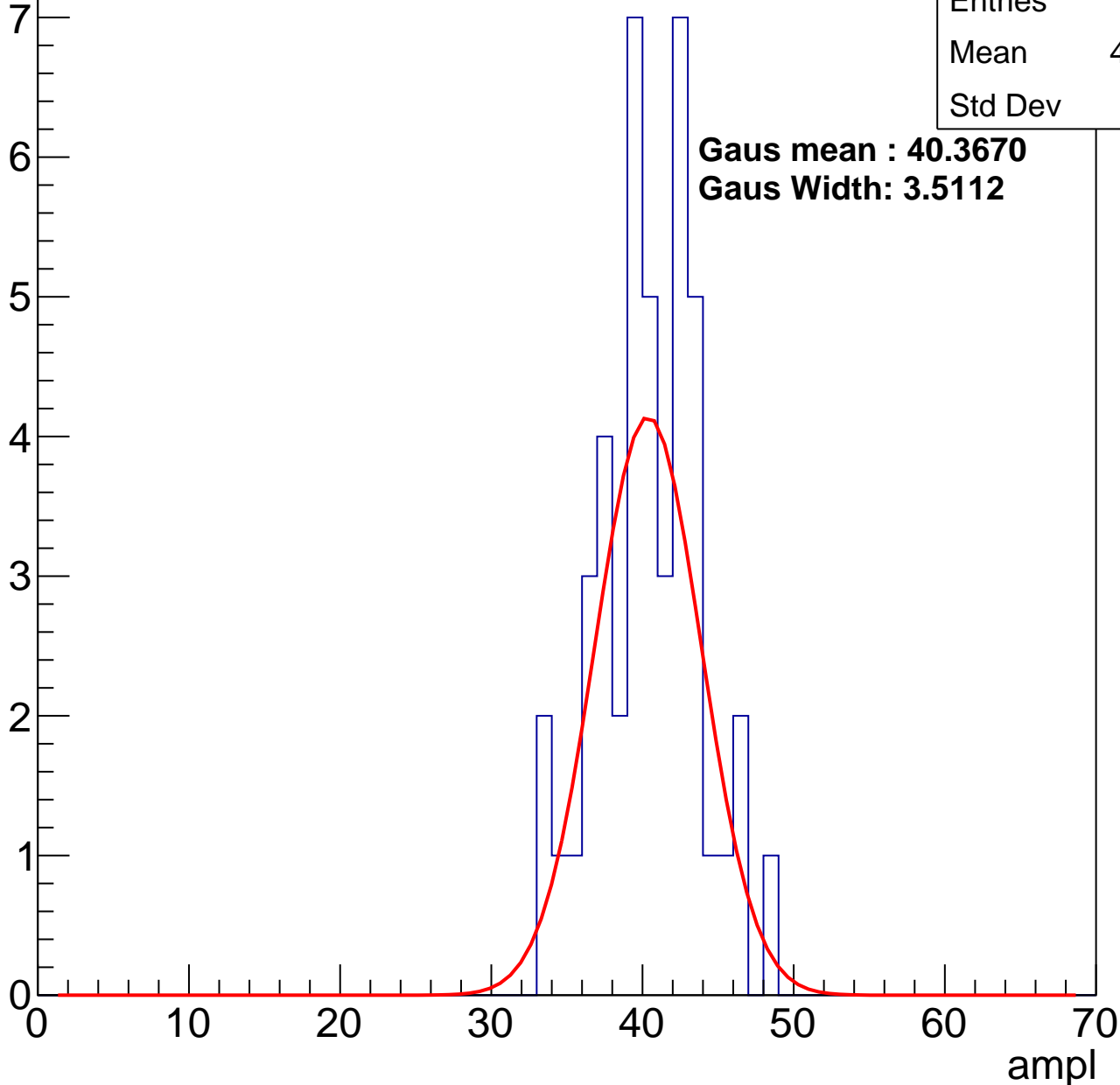
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	40.02
Std Dev	3.37

**Gaus mean : 40.3670**

**Gaus Width: 3.5112**

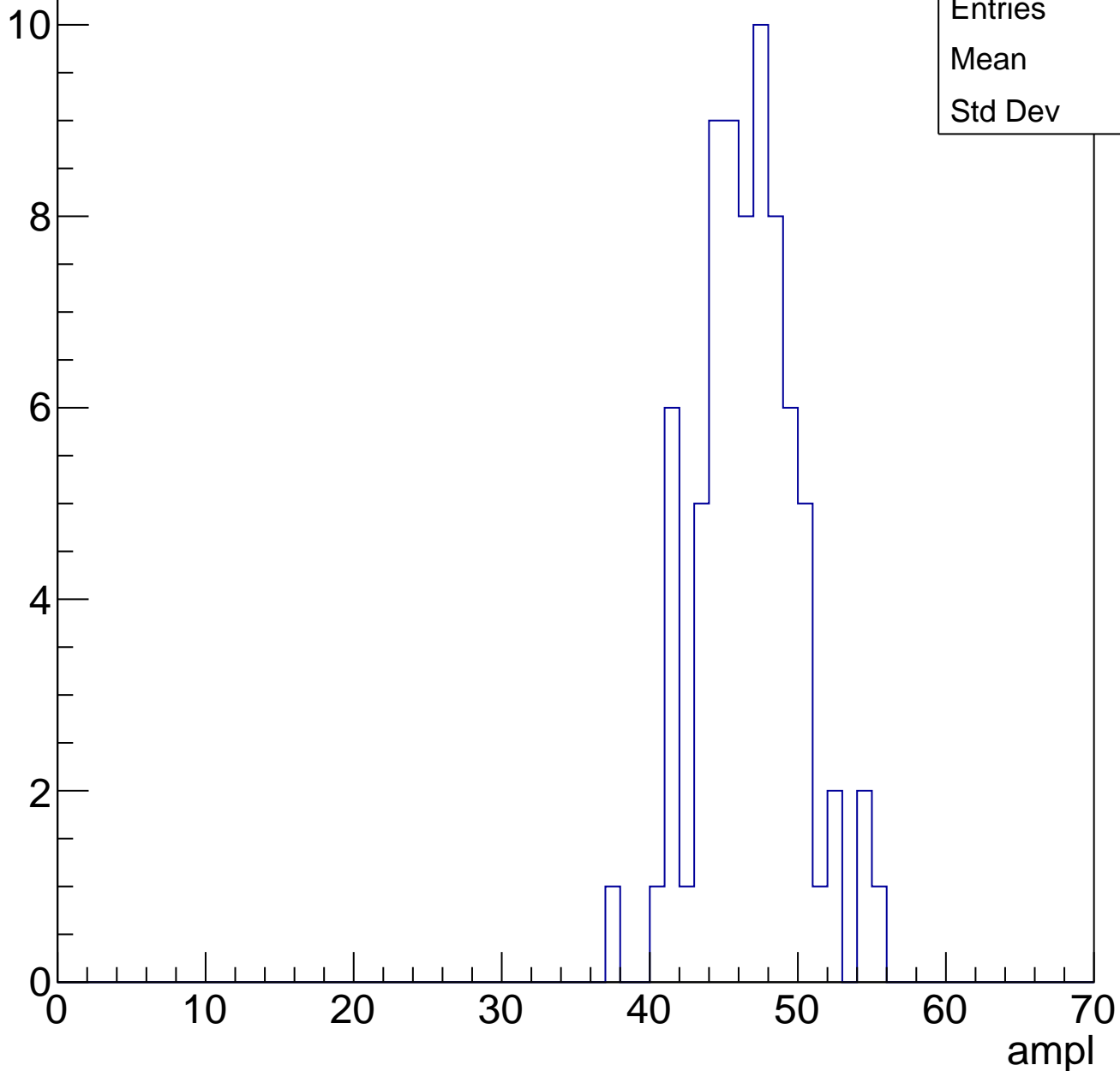


# B1L102S, U16-ch57, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	75
Mean	46.2
Std Dev	3.37

Entry

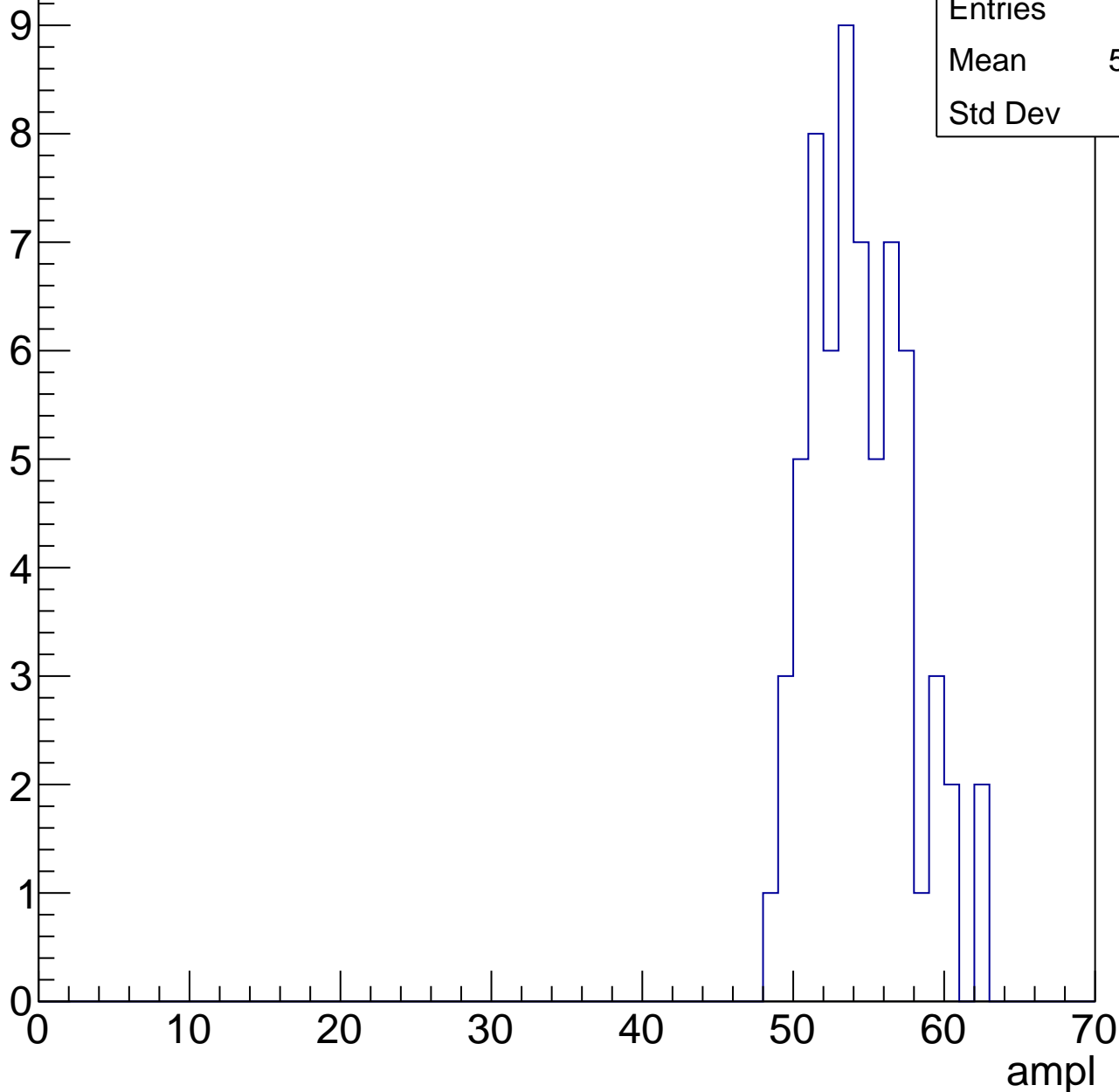


# B1L102S, U16-ch57, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	53.97
Std Dev	3.22

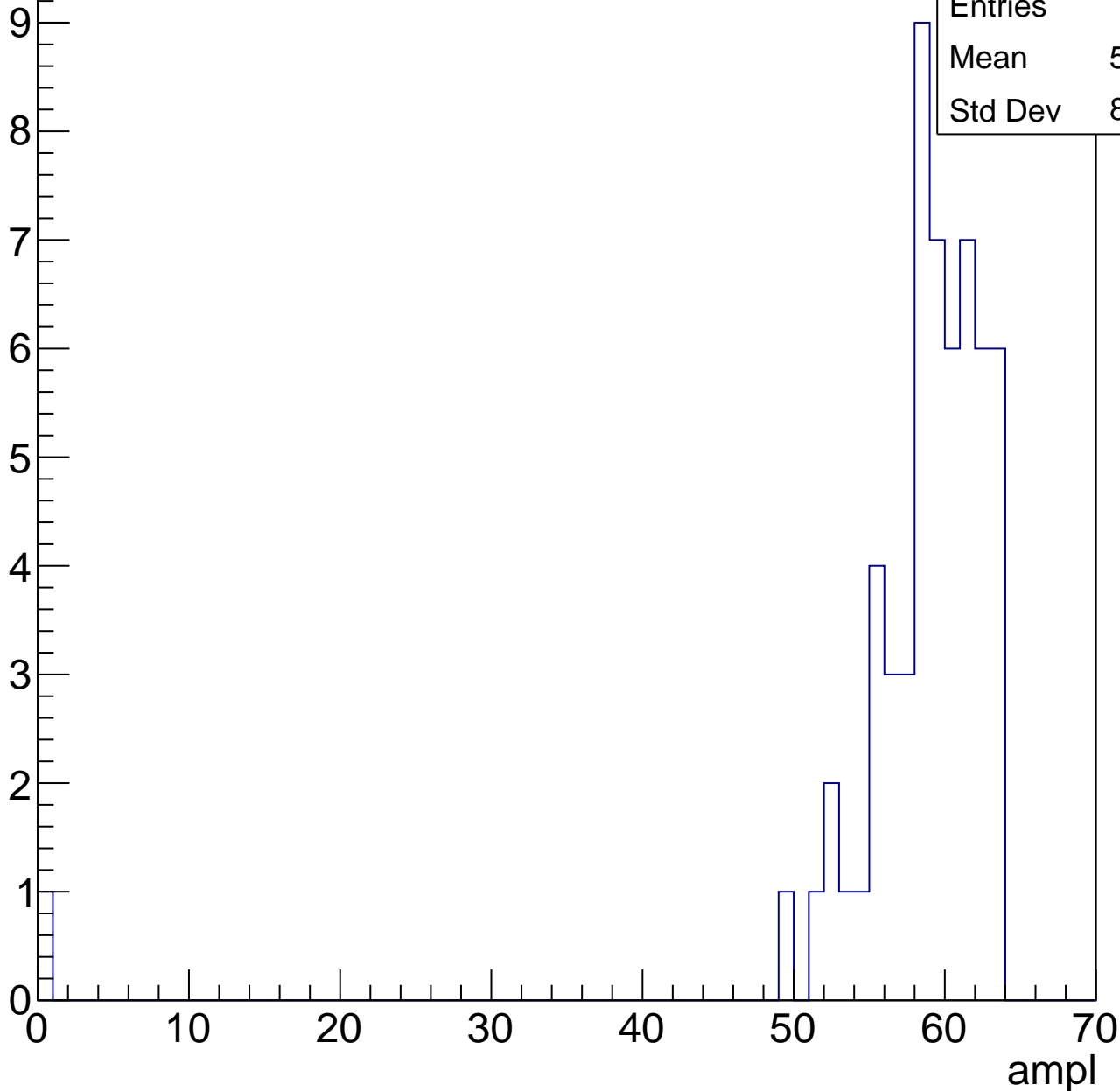


# B1L102S, U16-ch57, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

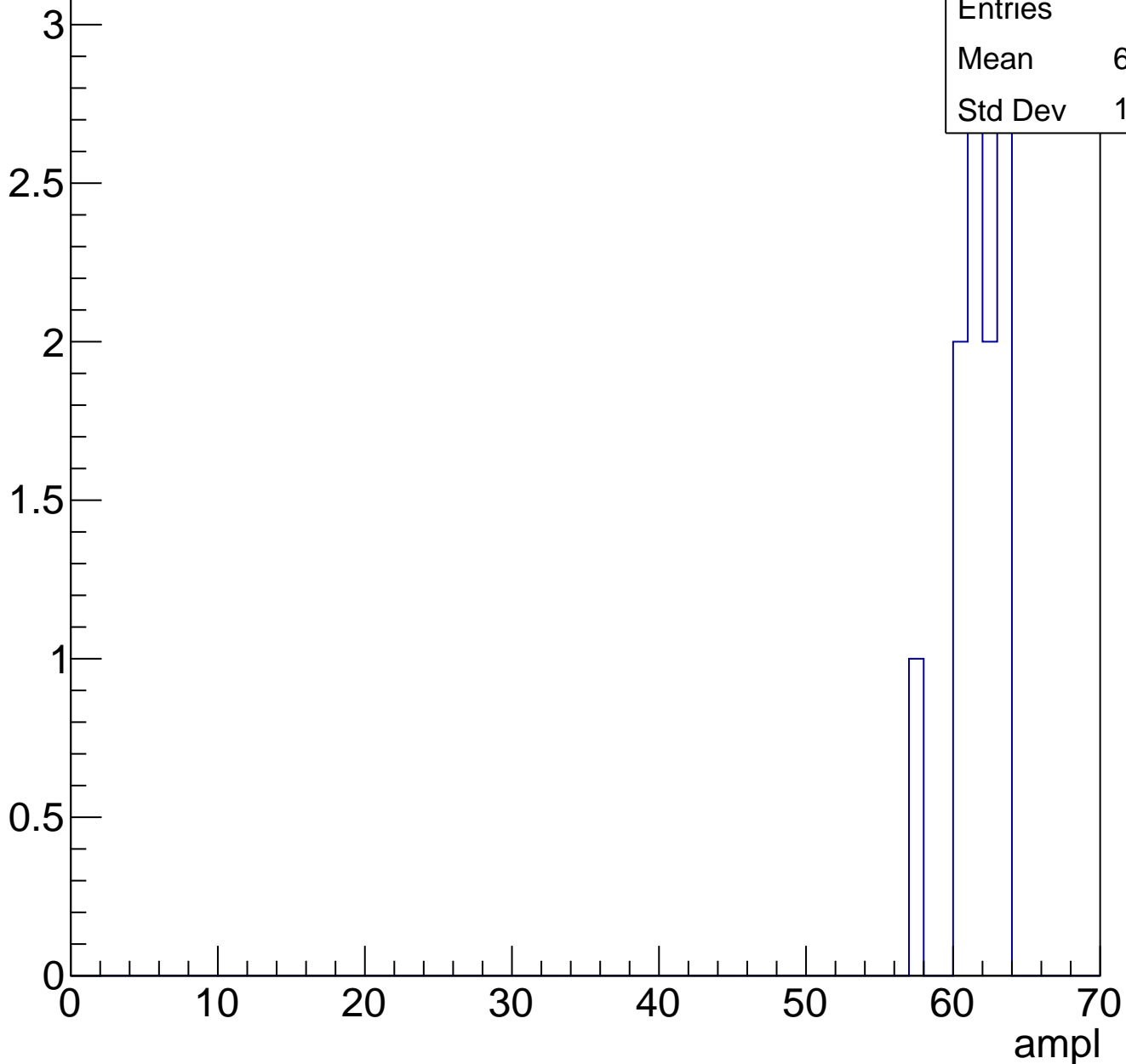
Entries	58
Mean	57.62
Std Dev	8.294



# B1L102S, U16-ch57, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

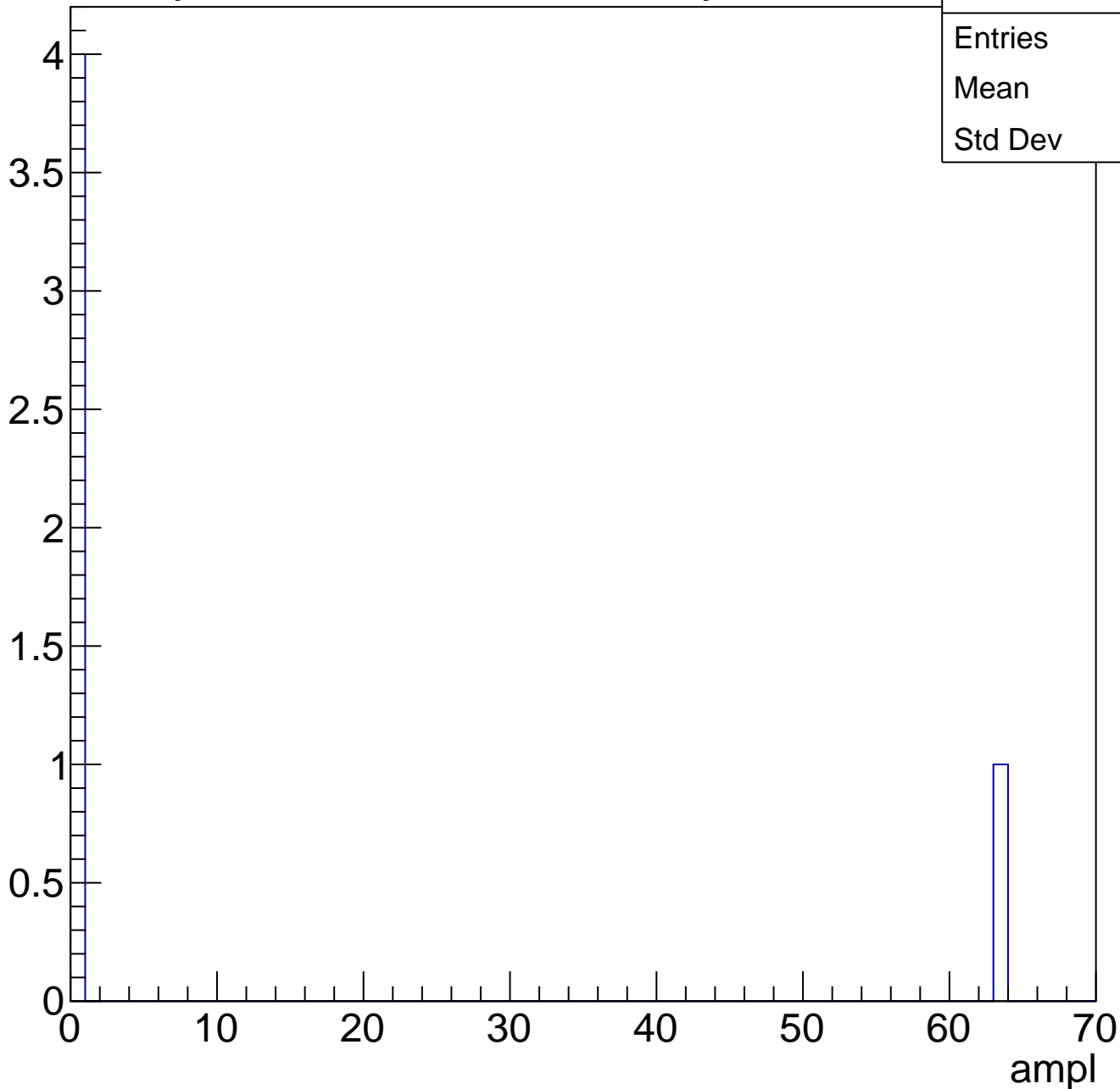




# B1L102S, U16-ch57, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch58, adc0

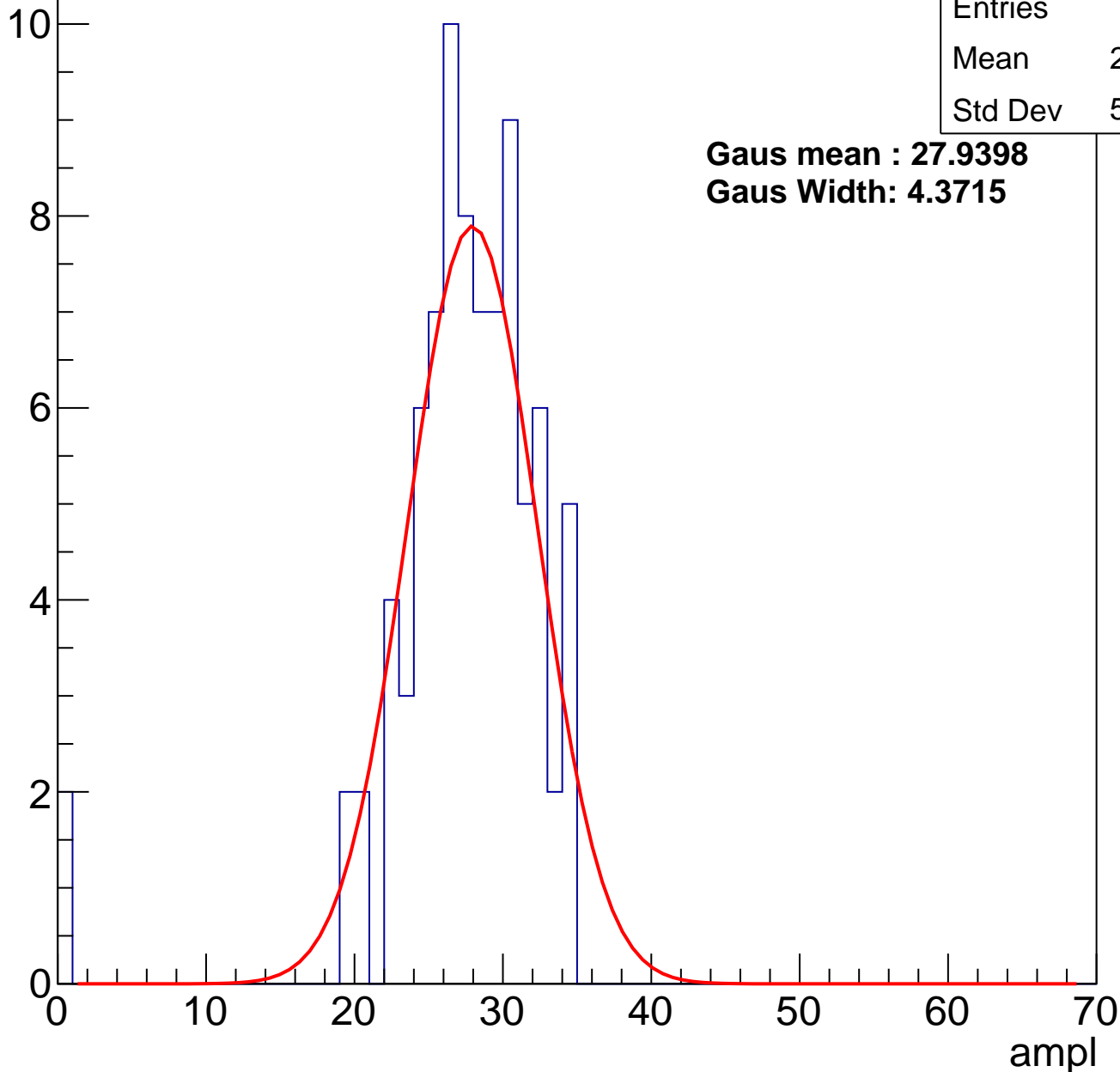
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	85
Mean	26.85
Std Dev	5.515

**Gaus mean : 27.9398**

**Gaus Width: 4.3715**

Entry



# B1L102S, U16-ch58, adc1

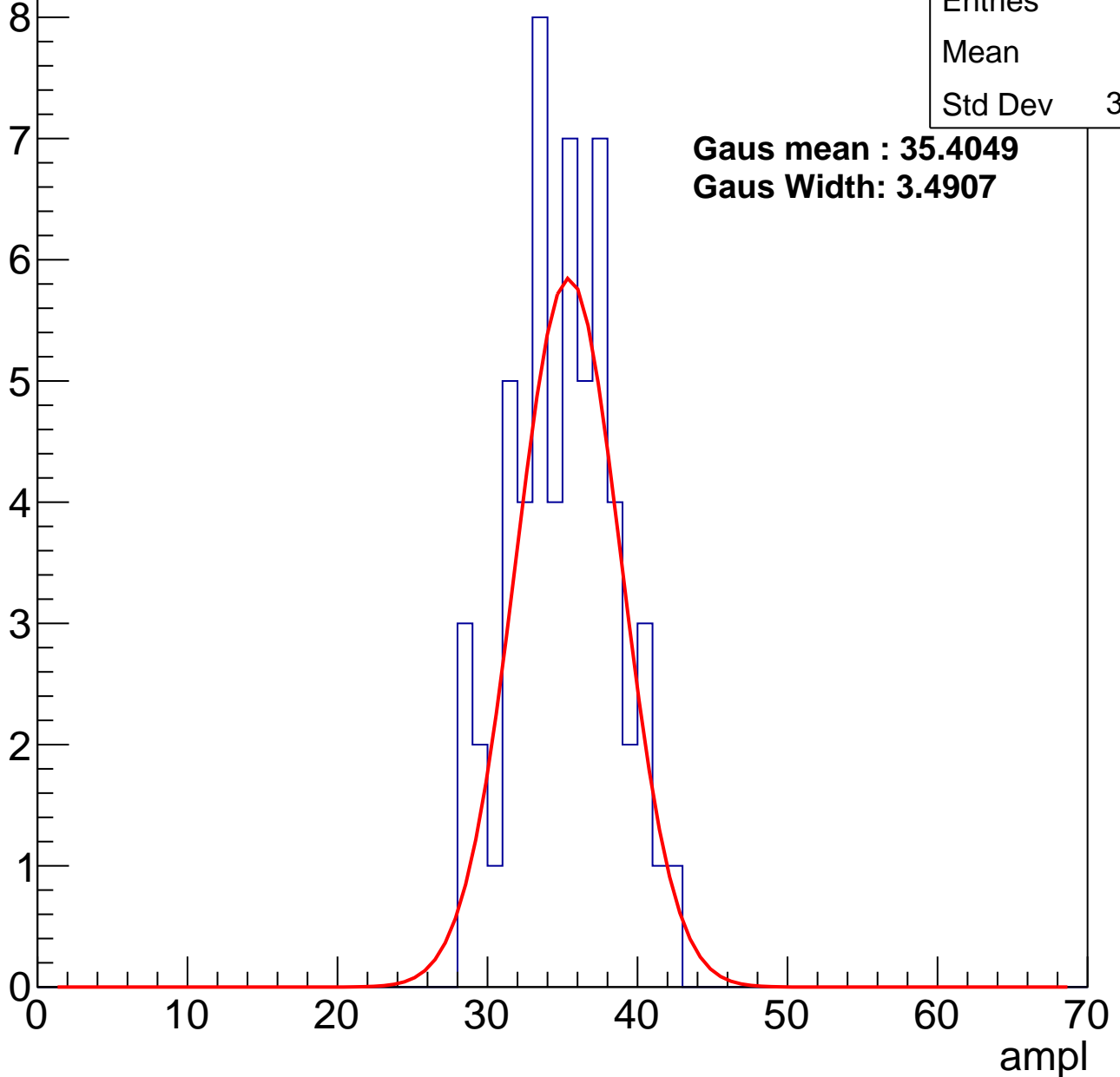
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	34.6
Std Dev	3.371

**Gaus mean : 35.4049**

**Gaus Width: 3.4907**



# B1L102S, U16-ch58, adc2

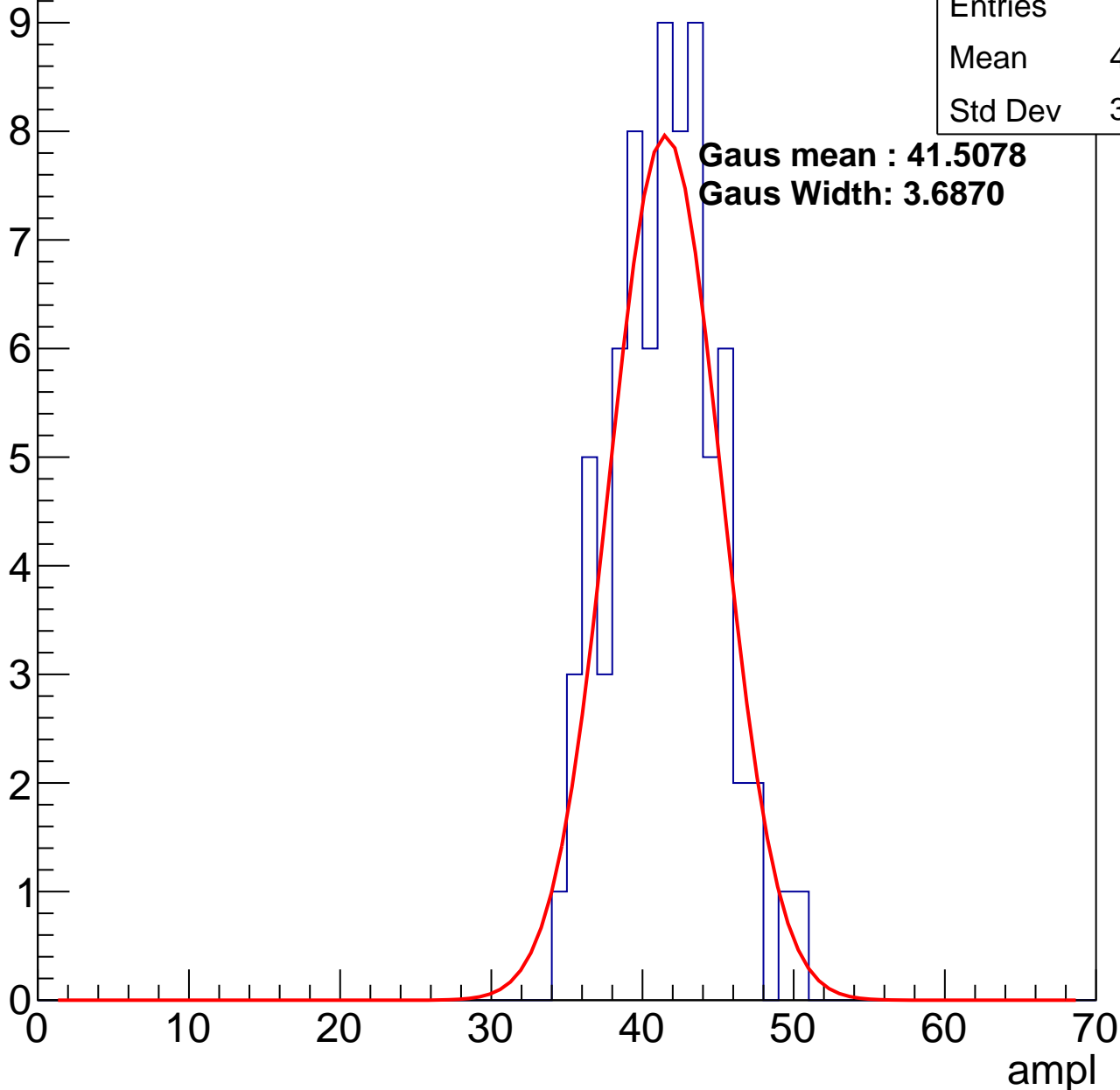
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	41.03
Std Dev	3.414

**Gaus mean : 41.5078**

**Gaus Width: 3.6870**

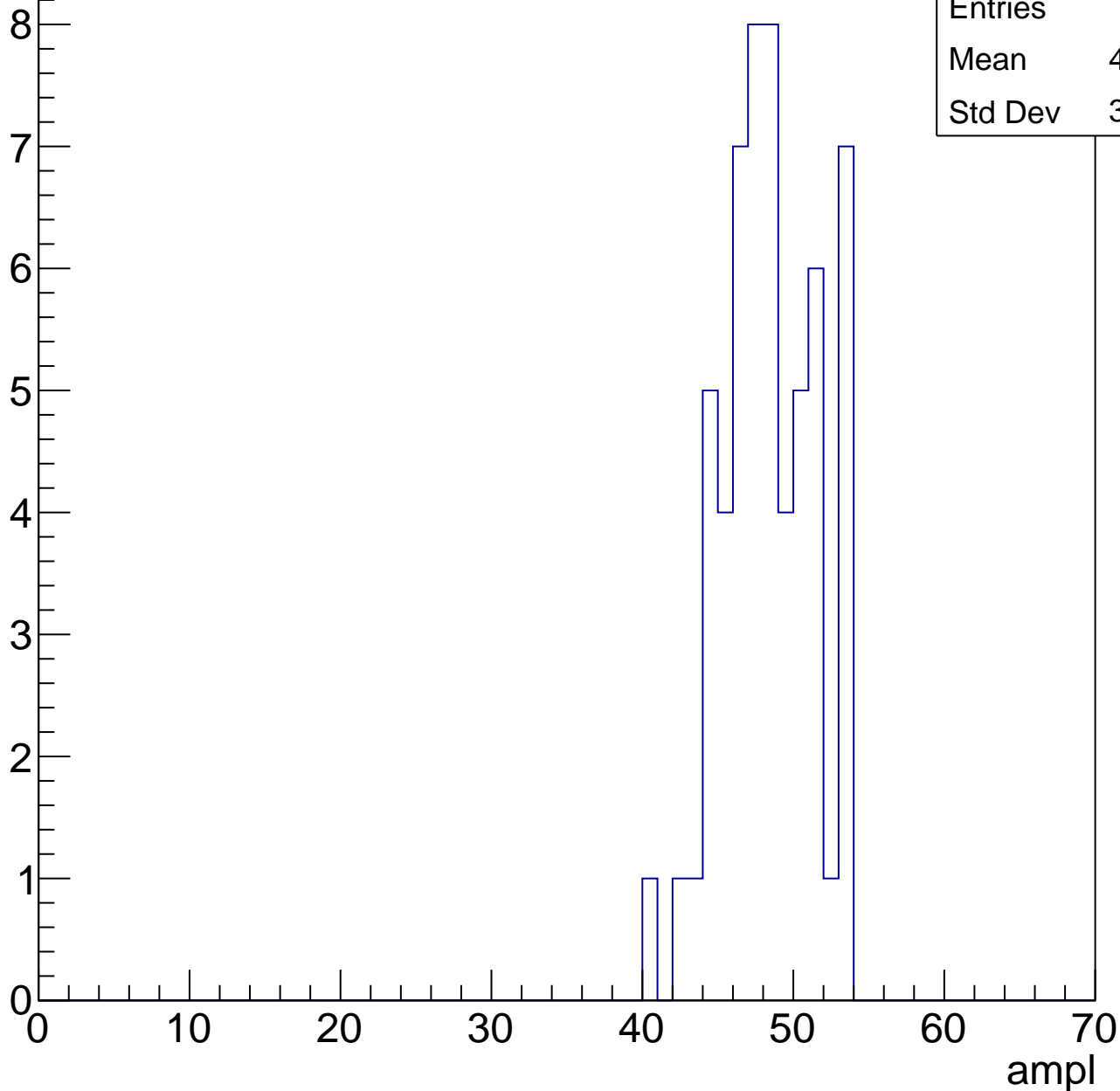


# B1L102S, U16-ch58, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	47.97
Std Dev	3.068

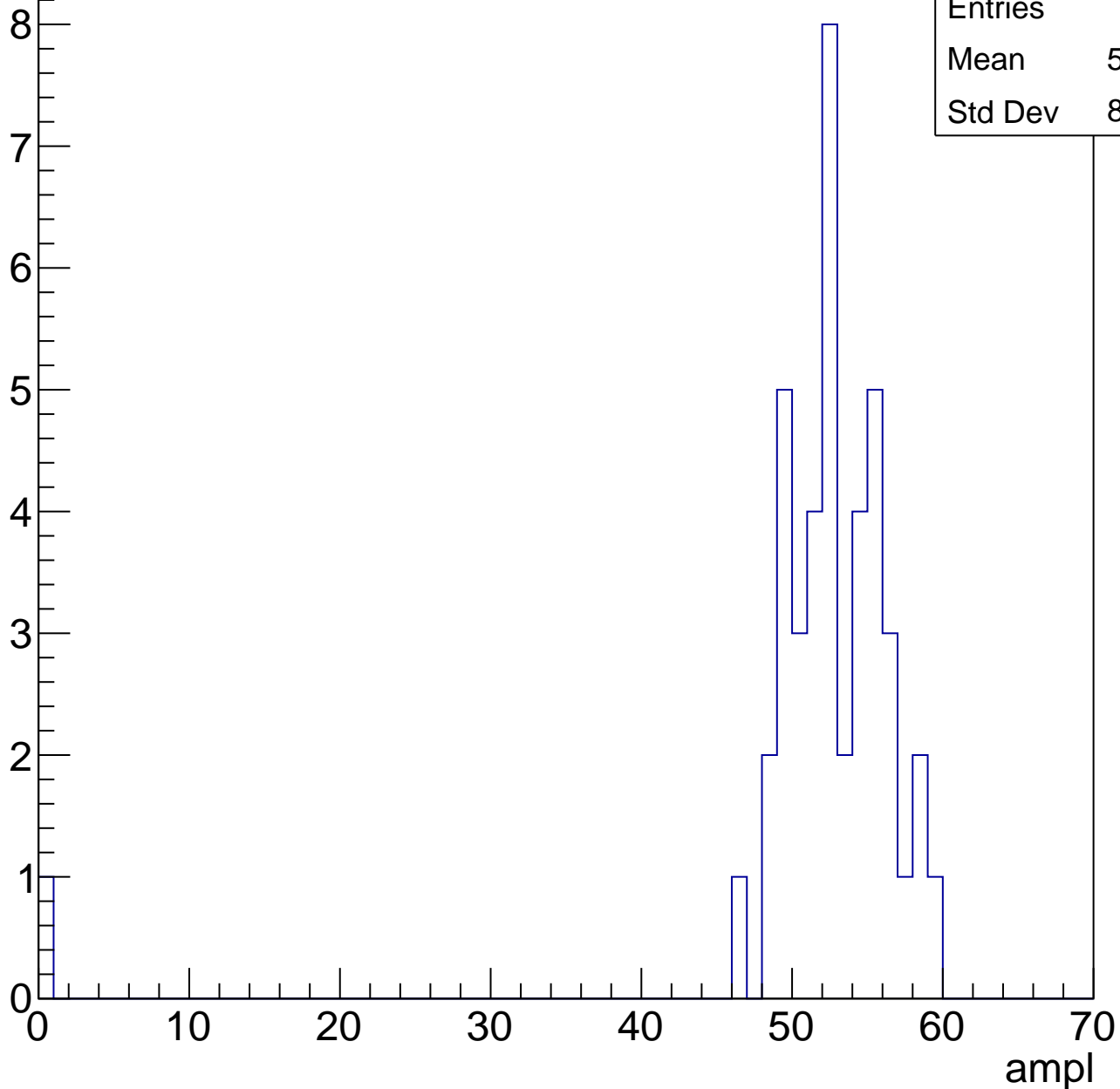


# B1L102S, U16-ch58, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

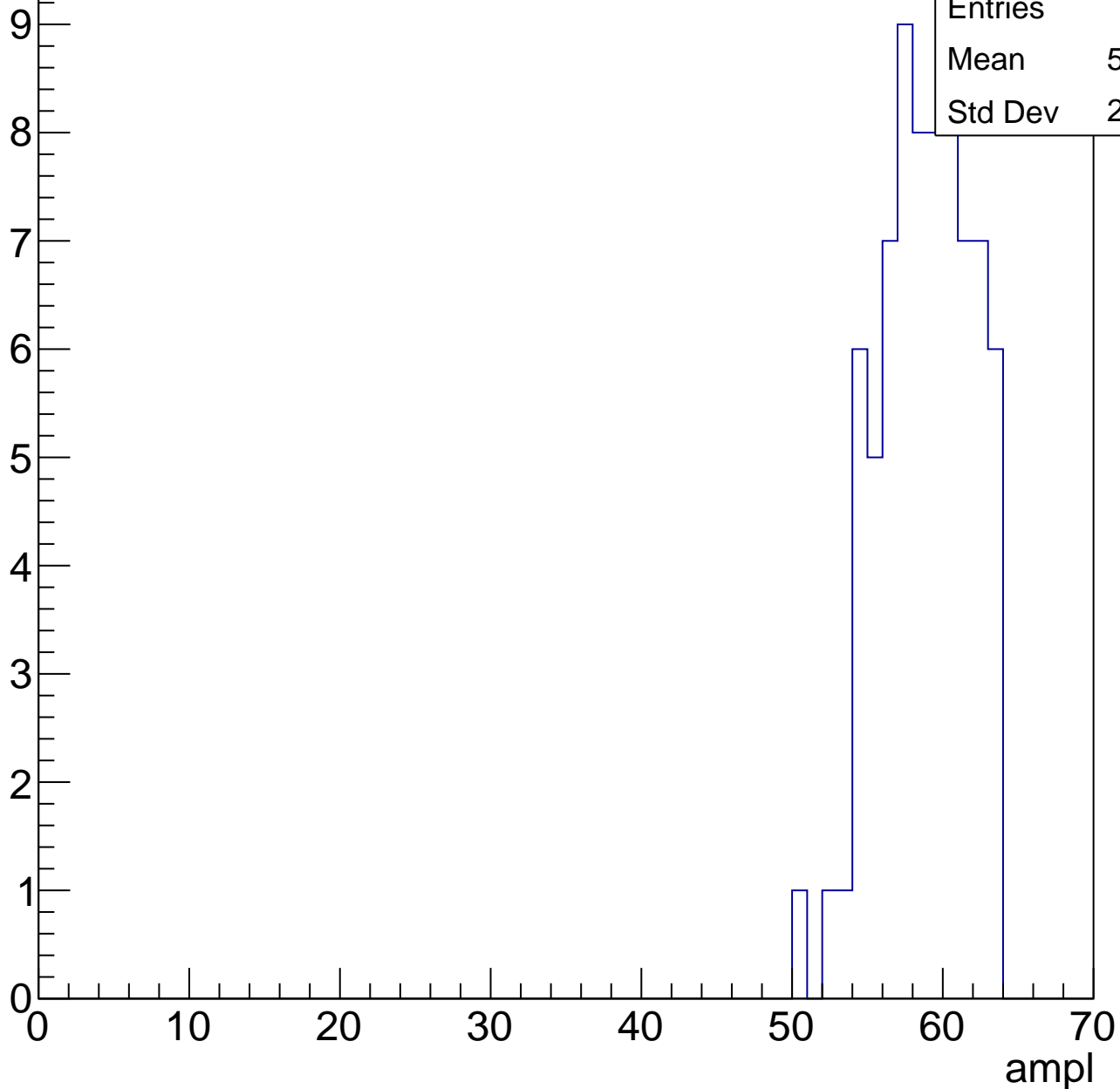
Entries	42
Mean	51.29
Std Dev	8.548



# B1L102S, U16-ch58, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

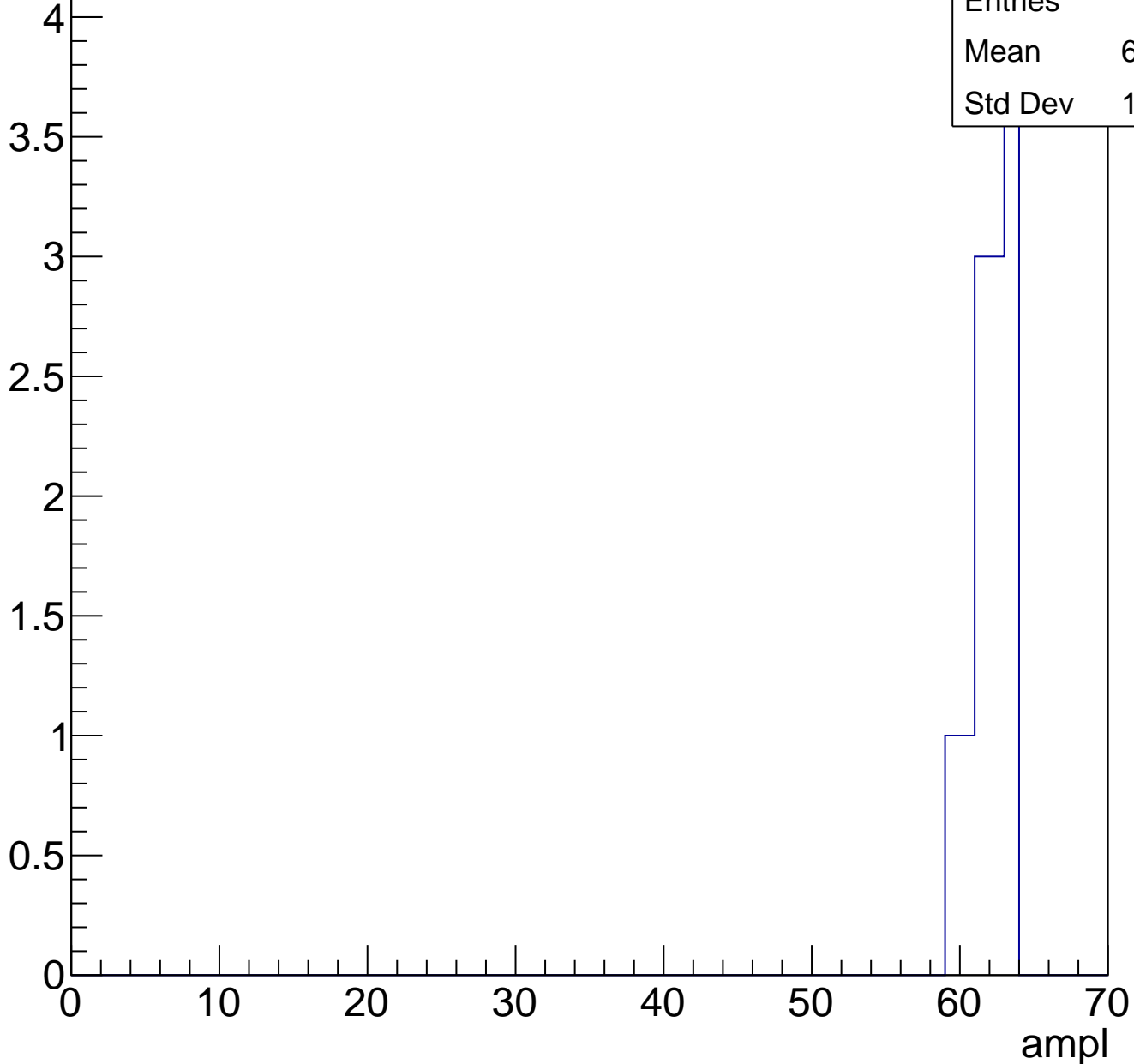


Entries	75
Mean	58.32
Std Dev	2.976

# B1L102S, U16-ch58, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch58, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch59, adc0

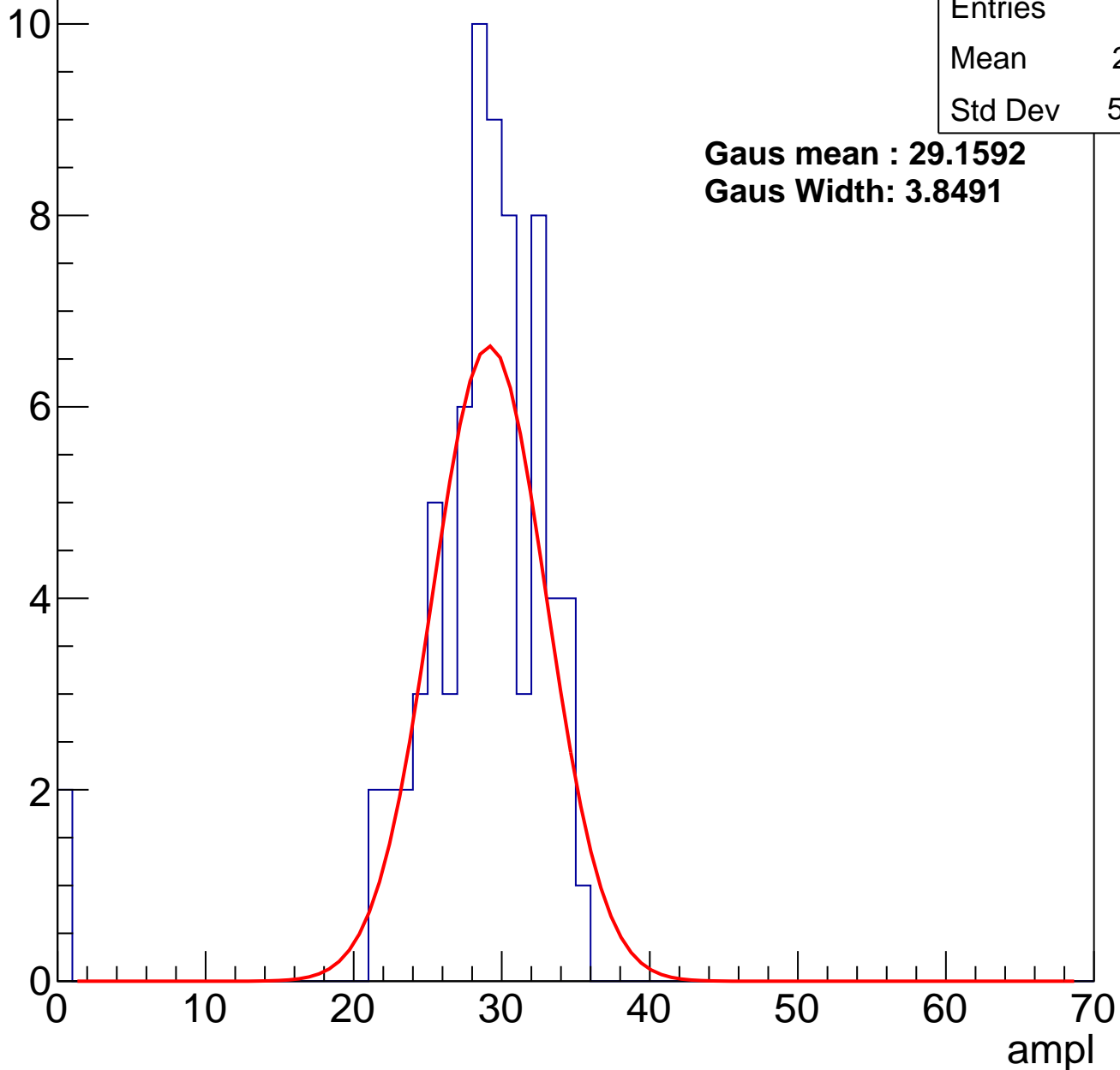
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	72
Mean	27.81
Std Dev	5.756

**Gaus mean : 29.1592**

**Gaus Width: 3.8491**

Entry

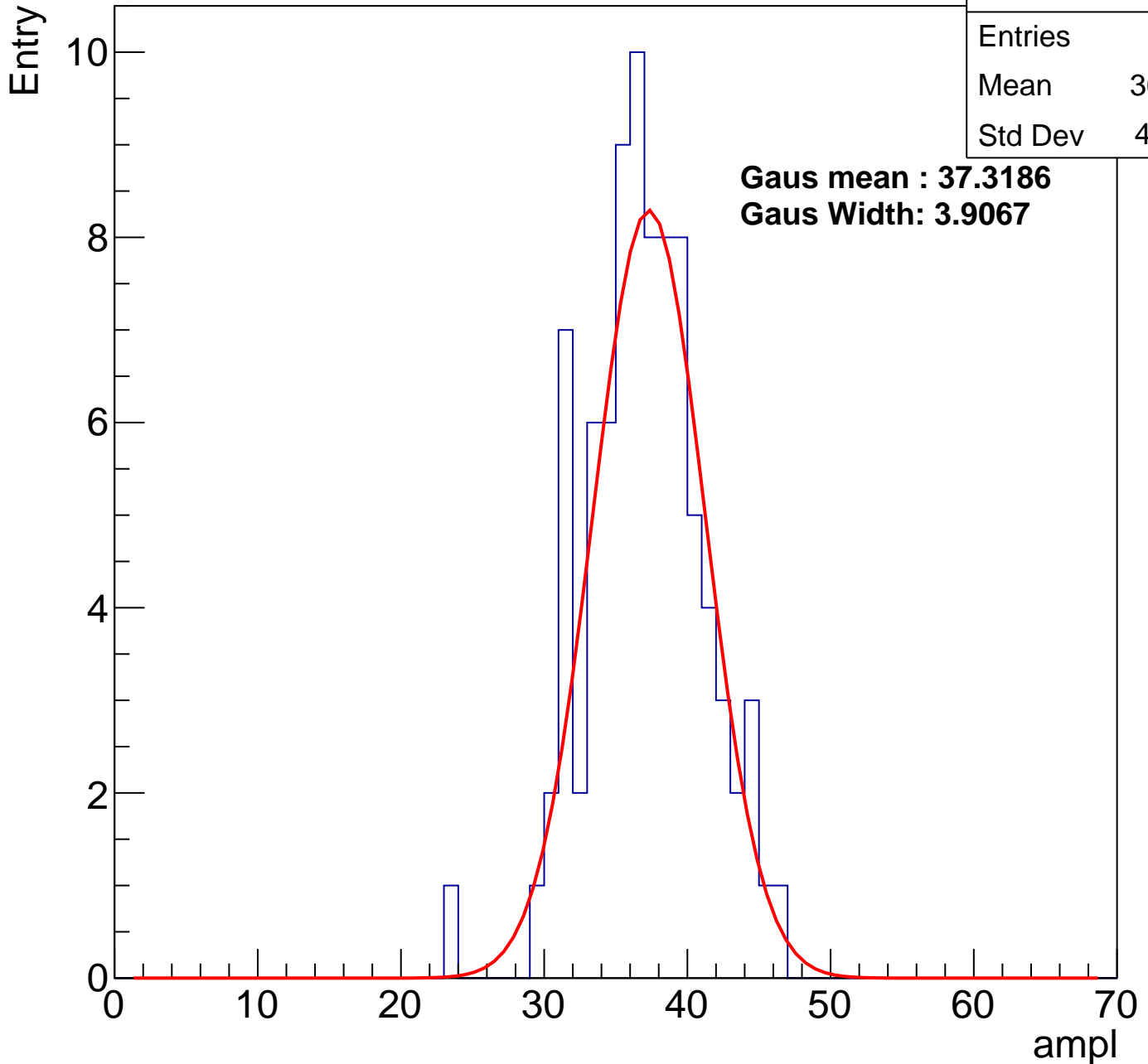


# B1L102S, U16-ch59, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	87
Mean	36.56
Std Dev	4.051

**Gaus mean : 37.3186**  
**Gaus Width: 3.9067**



# B1L102S, U16-ch59, adc2

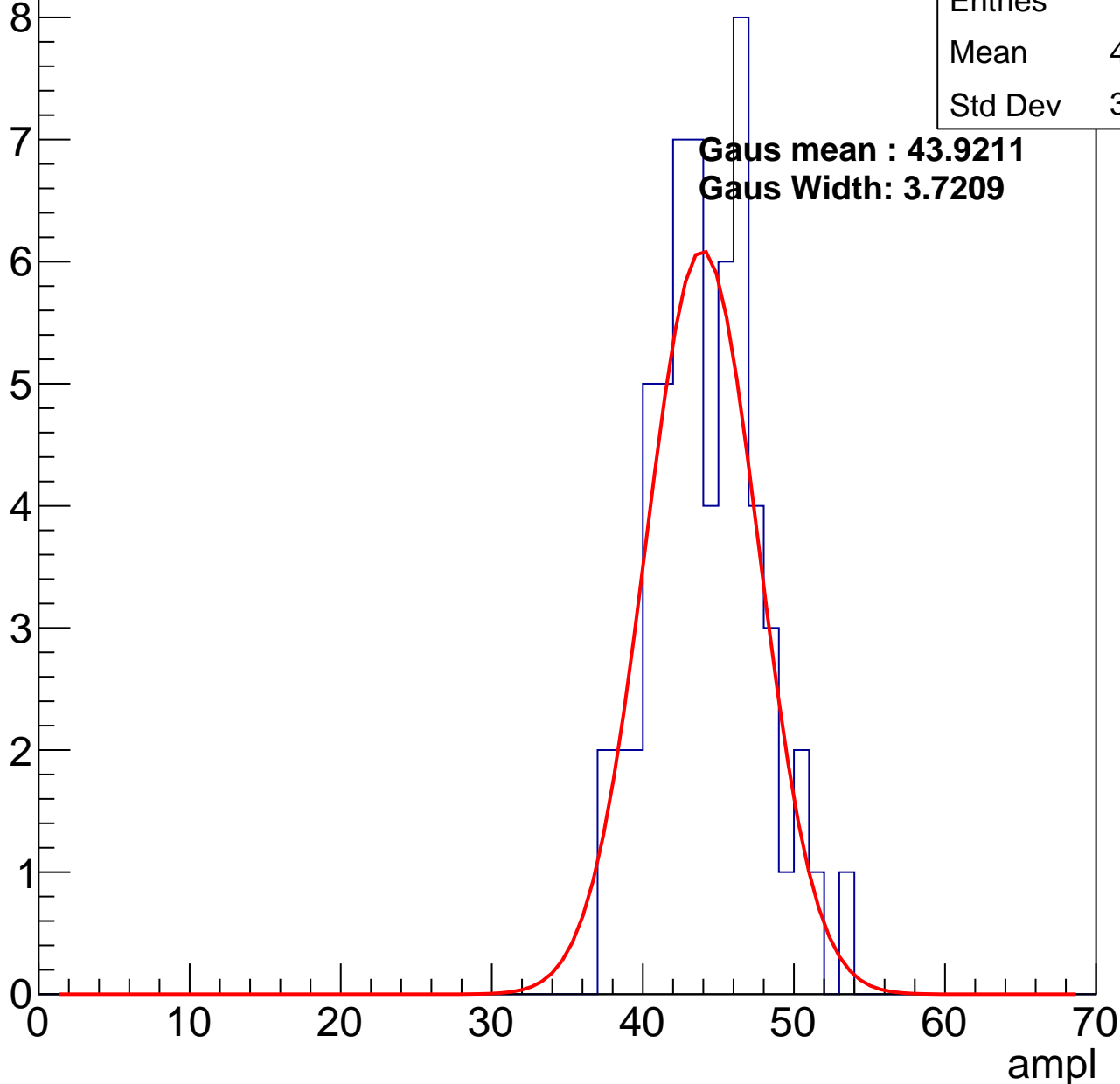
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	43.78
Std Dev	3.479

**Gaus mean : 43.9211**

**Gaus Width: 3.7209**

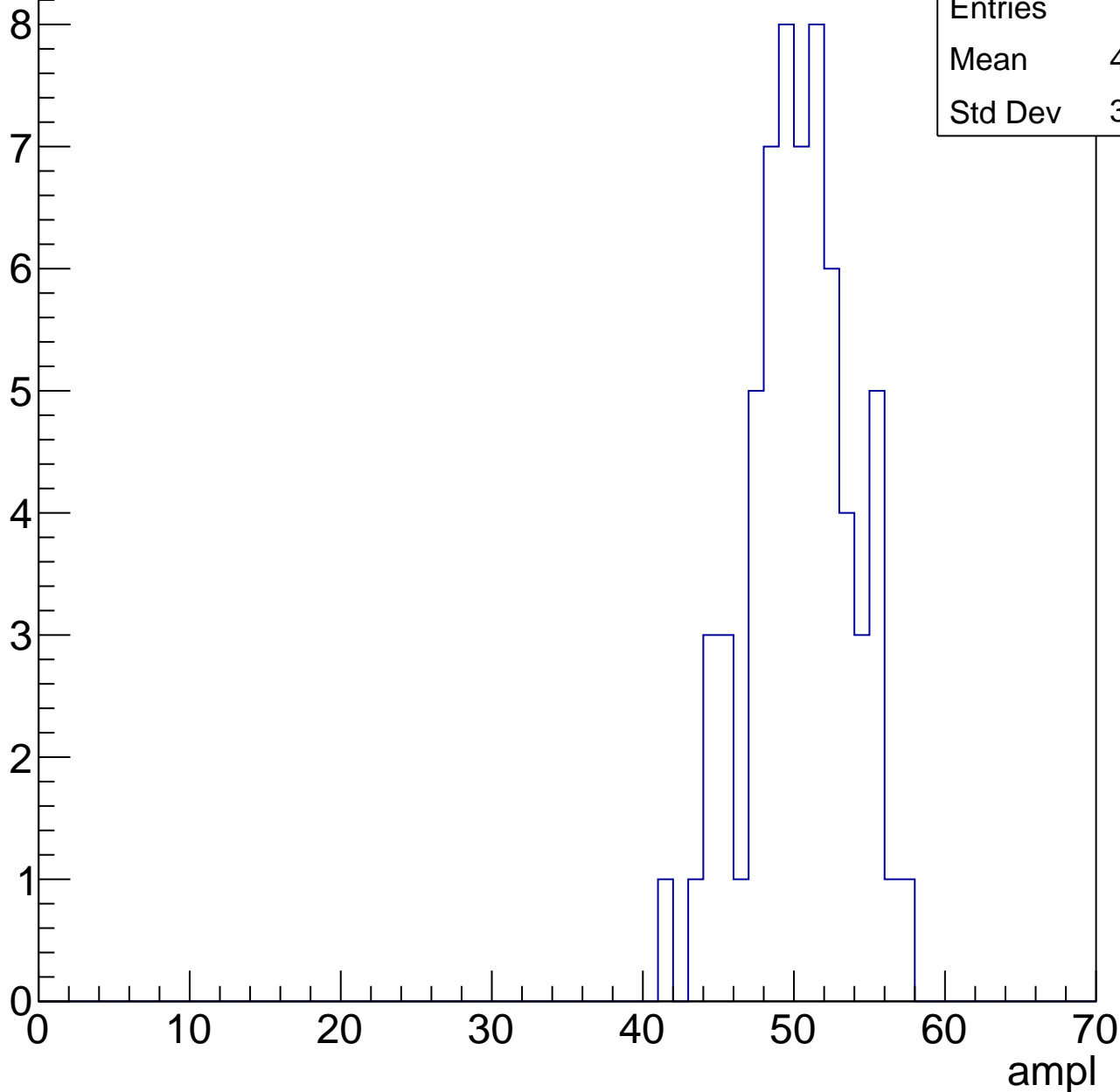


# B1L102S, U16-ch59, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	49.88
Std Dev	3.389

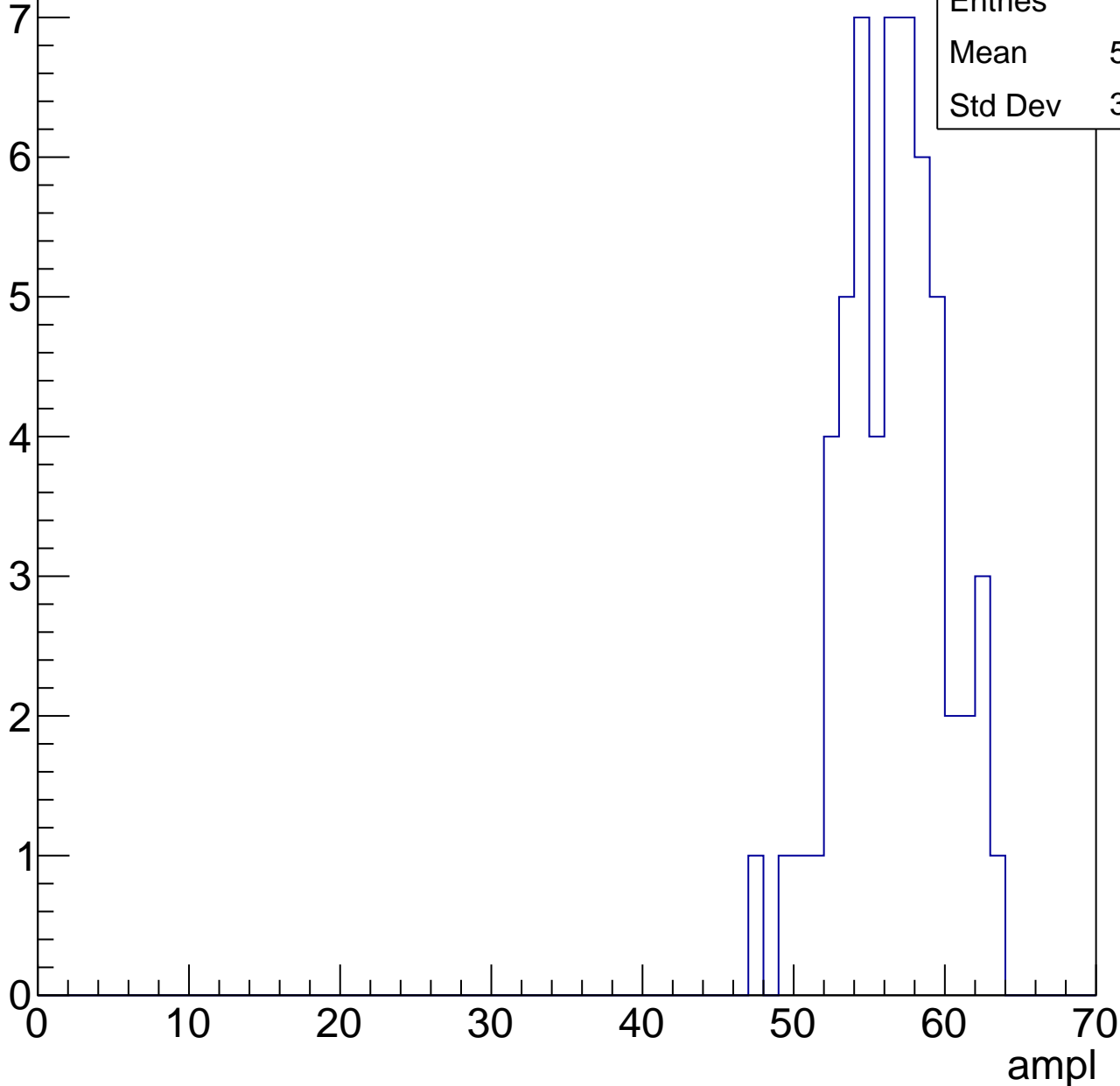


# B1L102S, U16-ch59, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	56.02
Std Dev	3.369



# B1L102S, U16-ch59, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

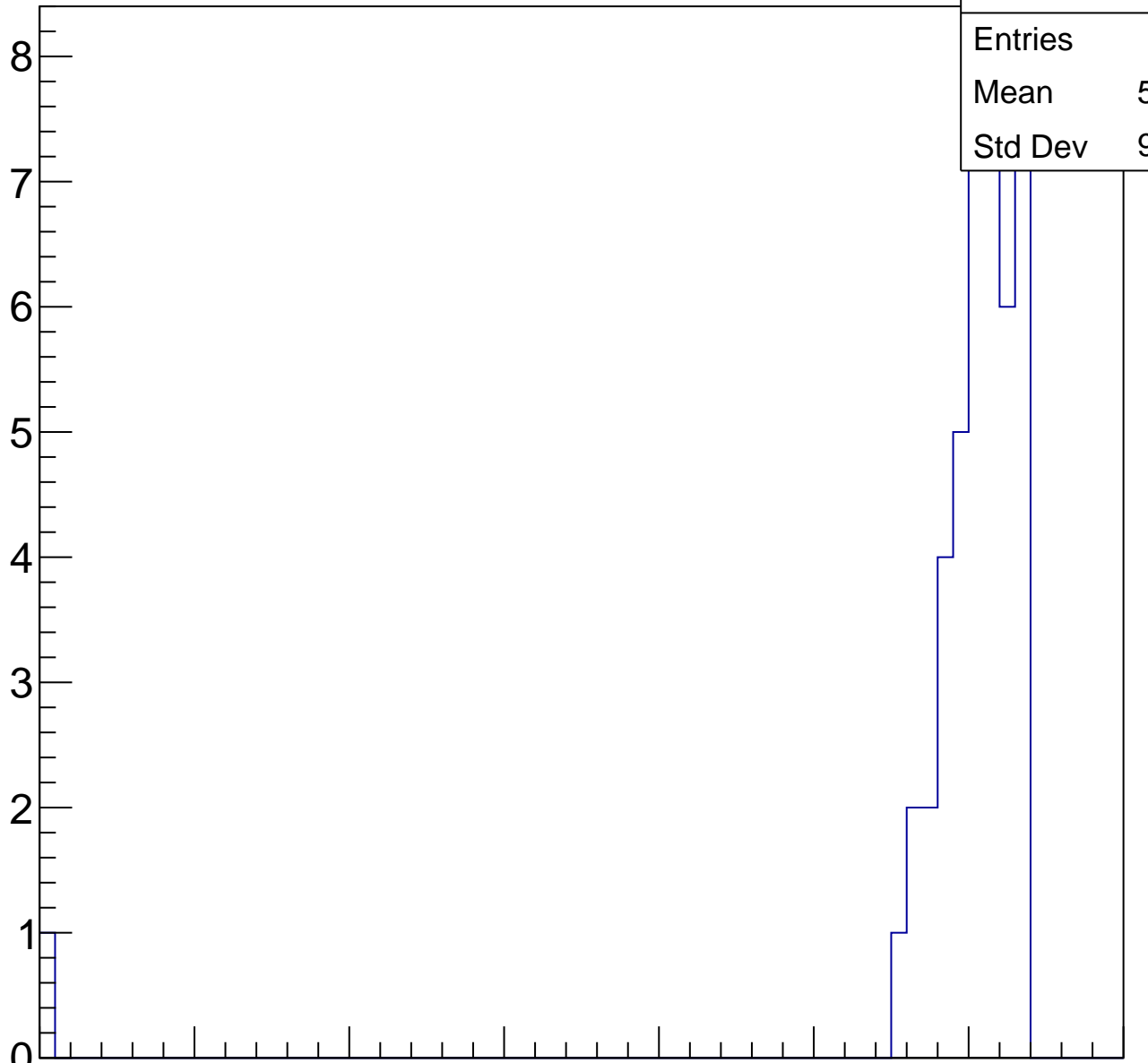
Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	45
Mean	58.93
Std Dev	9.127

ampl

0 10 20 30 40 50 60 70



# B1L102S, U16-ch59, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch59, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U16-ch60, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	68
Mean	28.01
Std Dev	3.74

**Gaus mean : 28.6878**

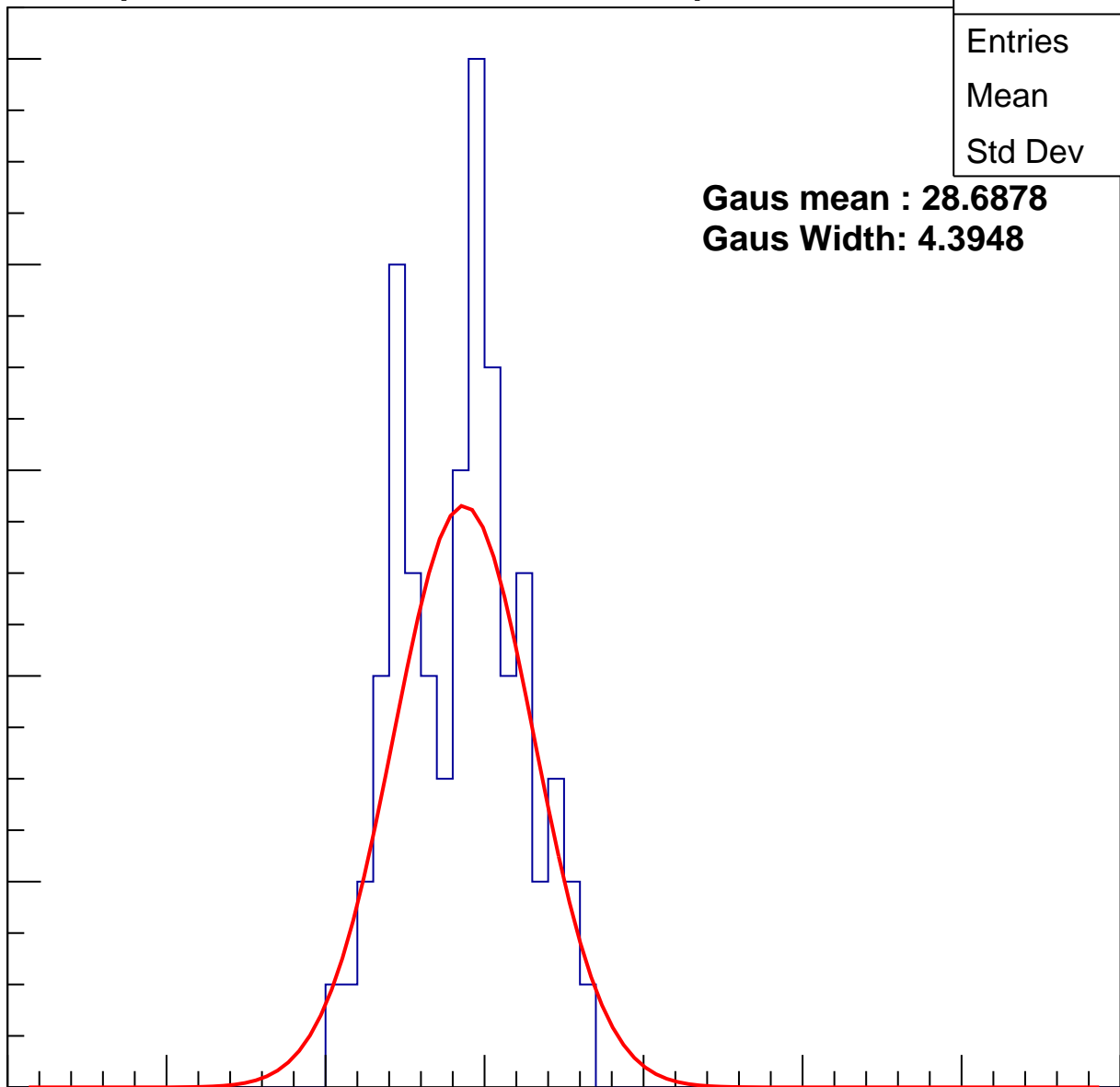
**Gaus Width: 4.3948**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U16-ch60, adc1

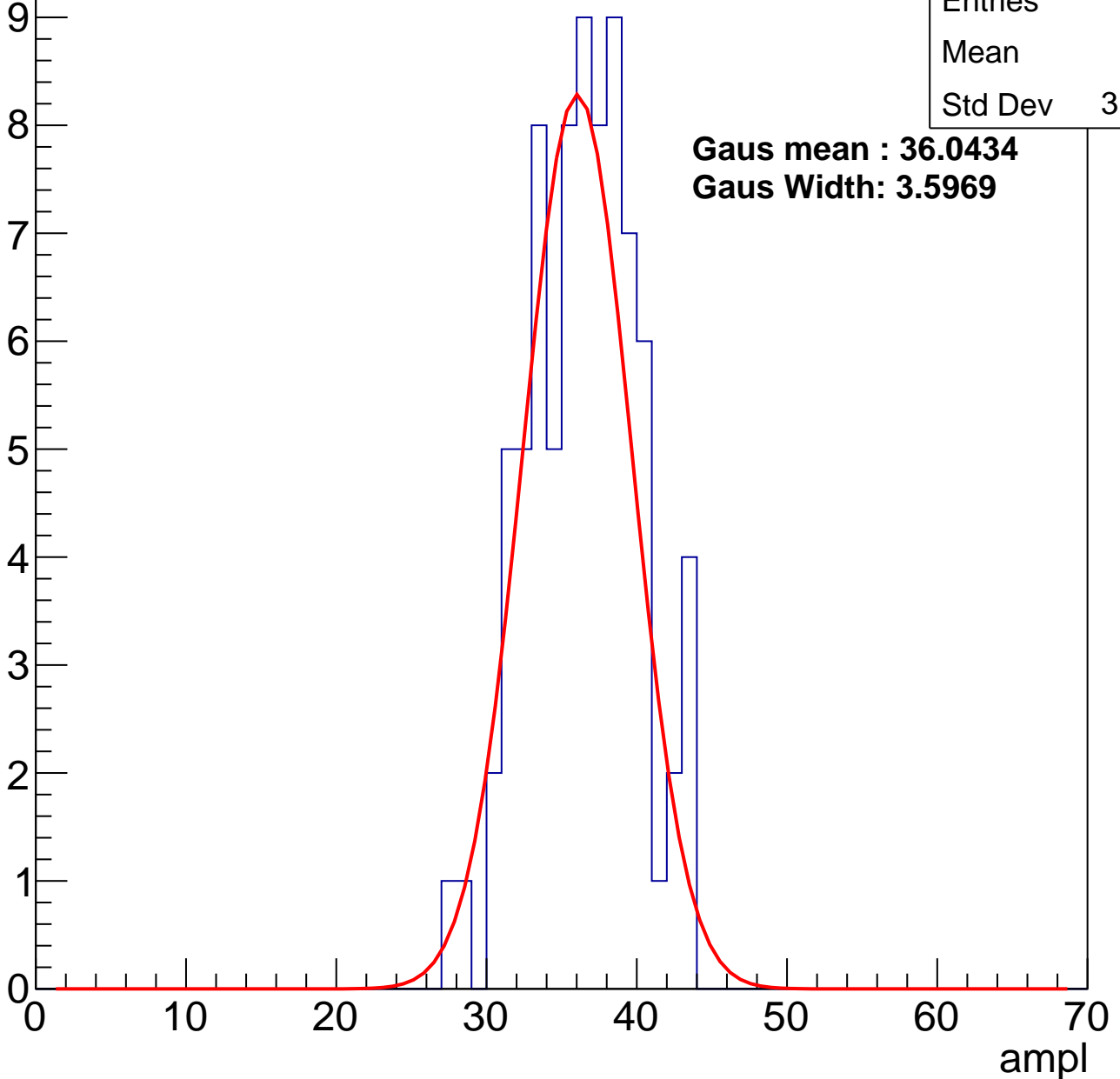
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	81
Mean	36
Std Dev	3.545

**Gaus mean : 36.0434**

**Gaus Width: 3.5969**



# B1L102S, U16-ch60, adc2

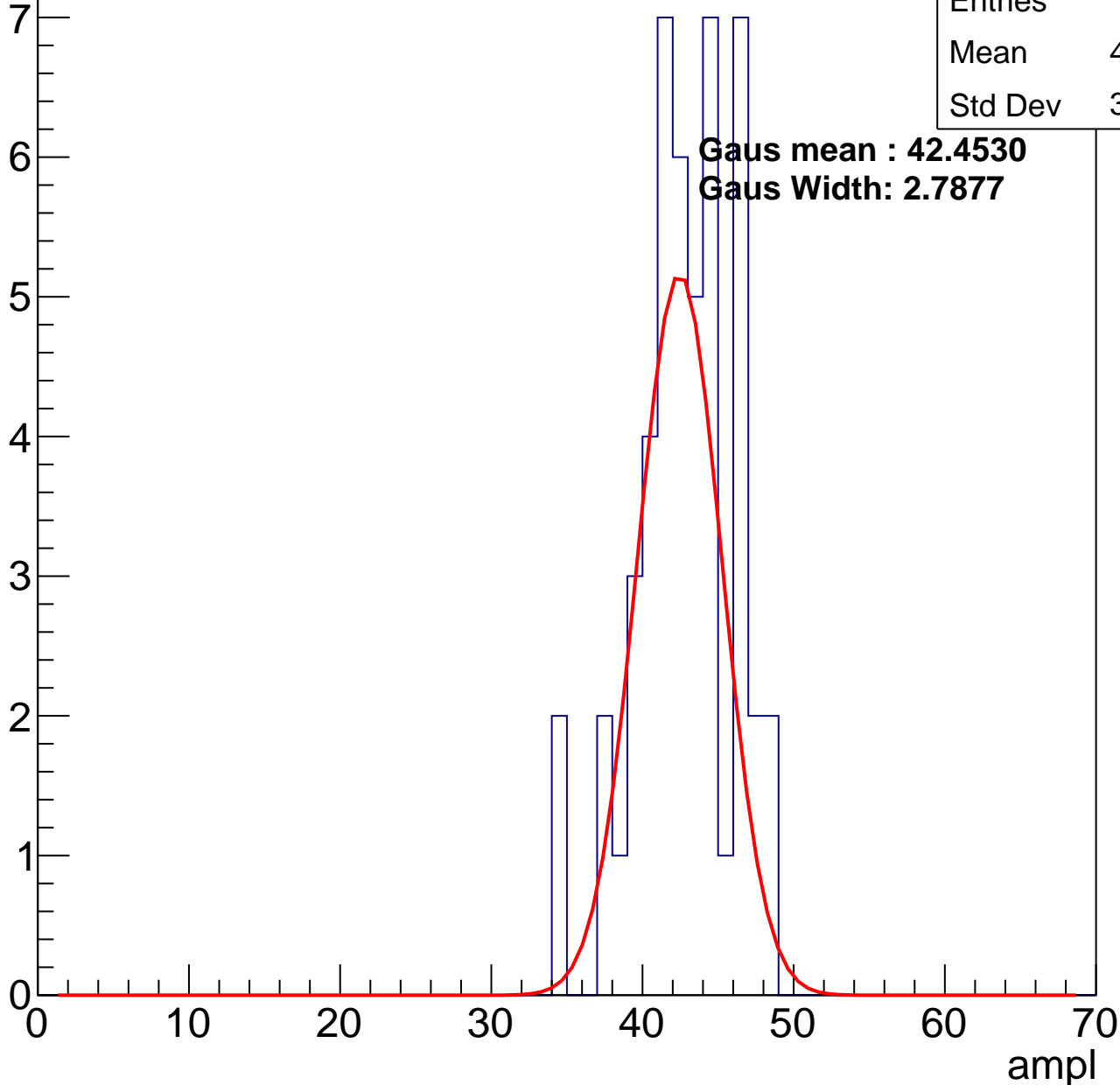
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	42.37
Std Dev	3.237

**Gaus mean : 42.4530**

**Gaus Width: 2.7877**

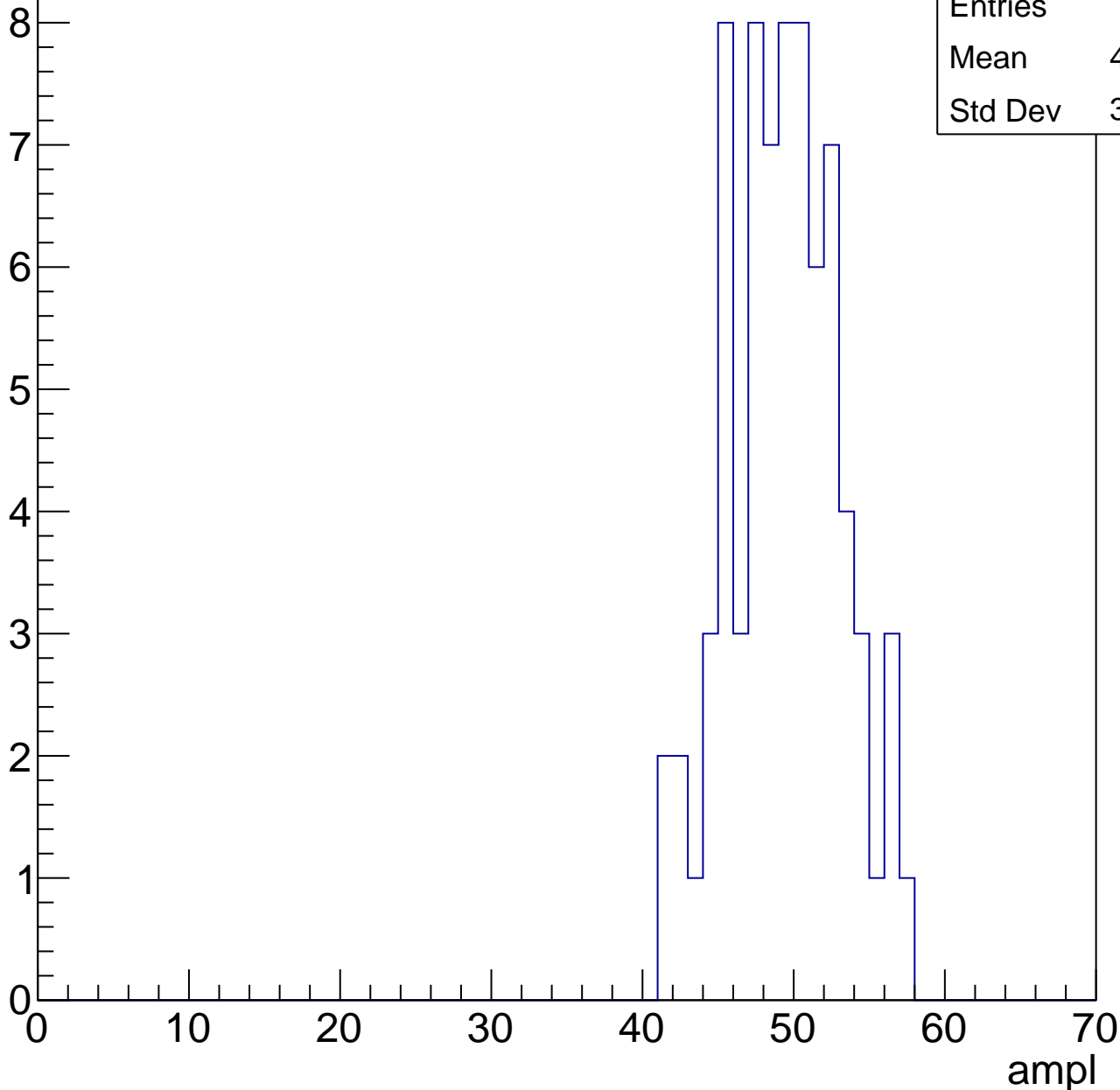


# B1L102S, U16-ch60, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	48.89
Std Dev	3.672

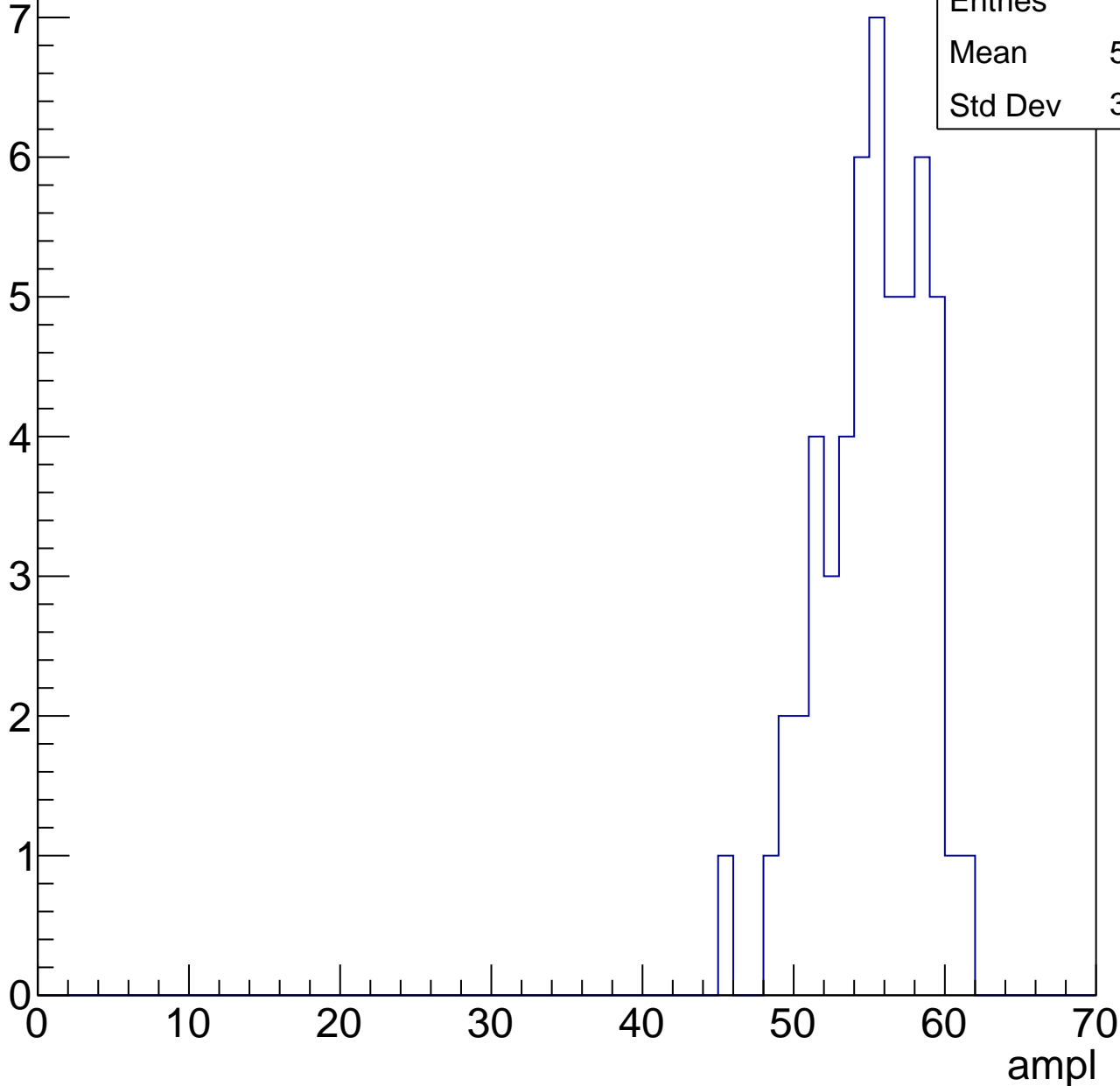


# B1L102S, U16-ch60, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	54.74
Std Dev	3.365

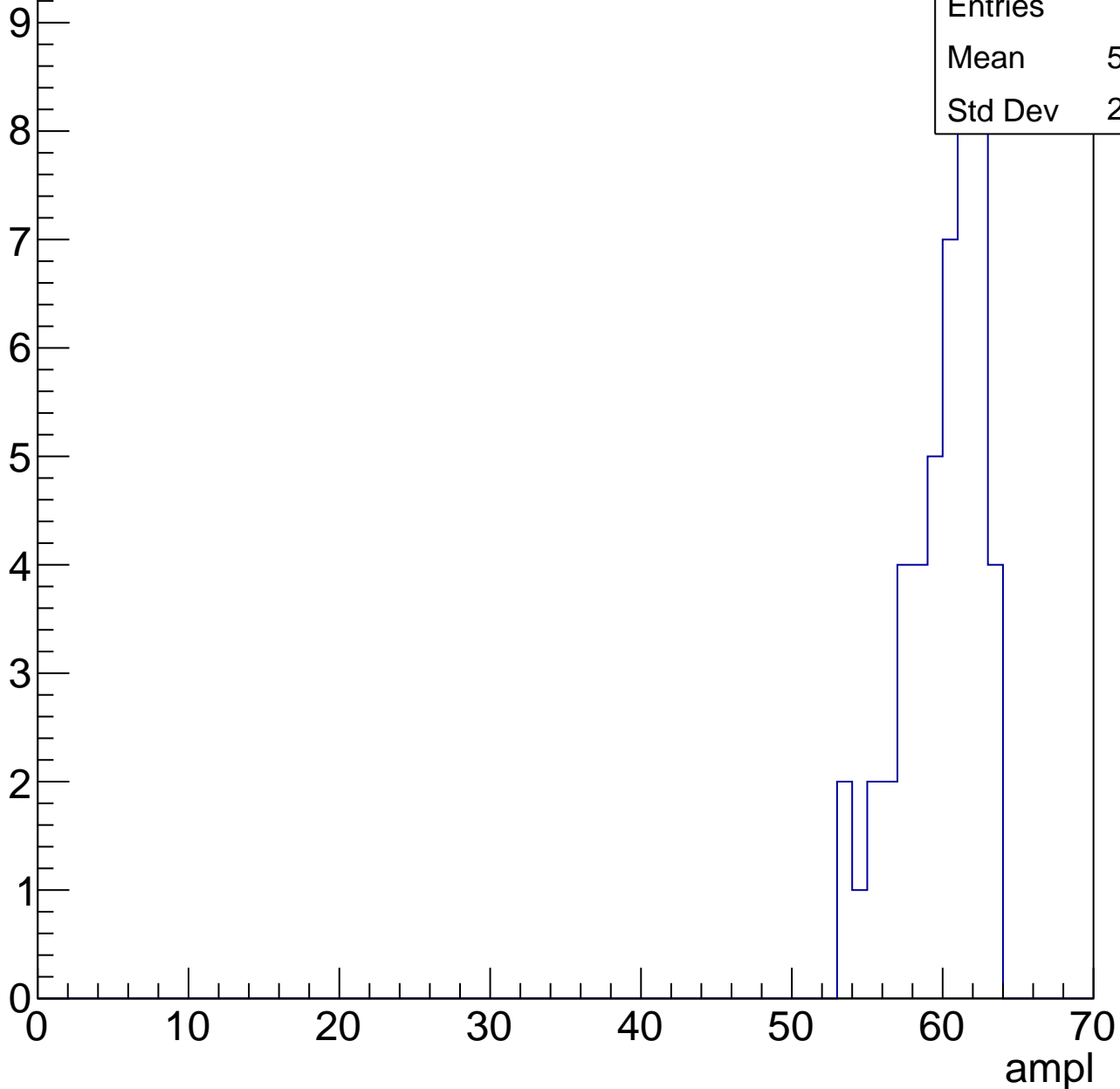


# B1L102S, U16-ch60, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

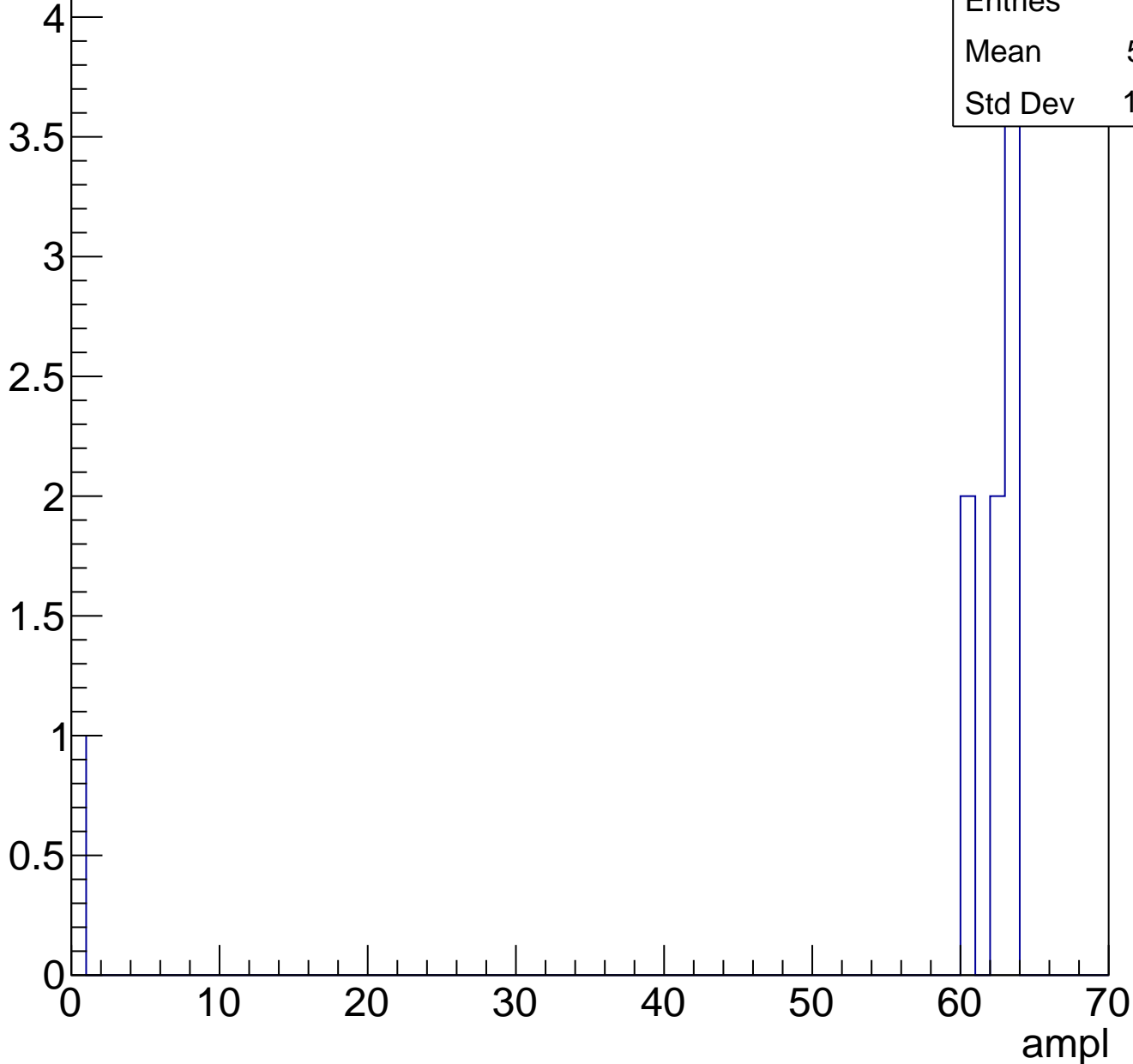
Entries	48
Mean	59.46
Std Dev	2.645



# B1L102S, U16-ch60, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch60, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	63
Std Dev	0

# B1L102S, U16-ch61, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	70
Mean	28.99
Std Dev	3.064

**Gaus mean : 29.2954**

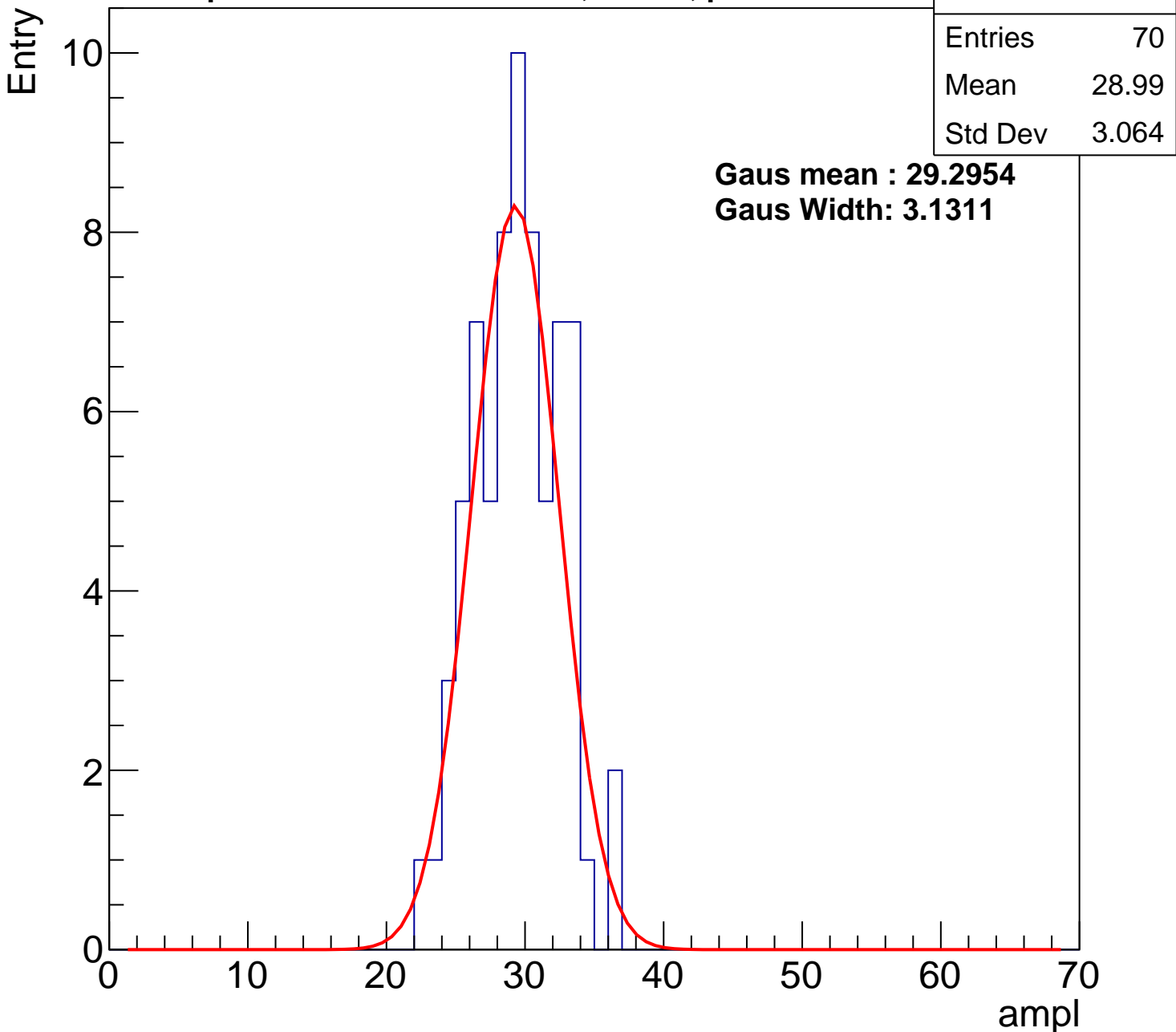
**Gaus Width: 3.1311**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U16-ch61, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	67
Mean	35.87
Std Dev	3.291

**Gaus mean : 36.6968**

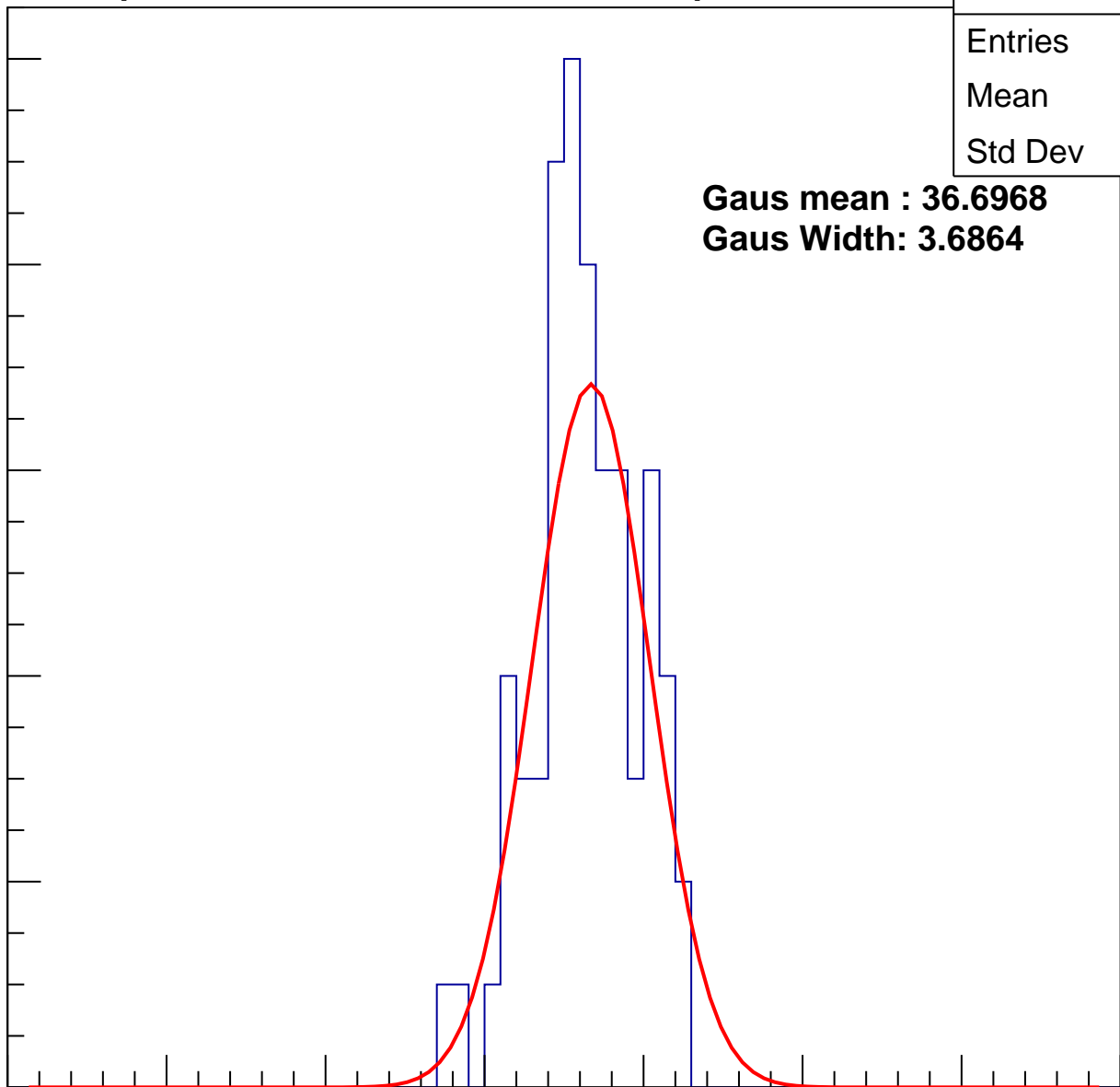
**Gaus Width: 3.6864**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U16-ch61, adc2

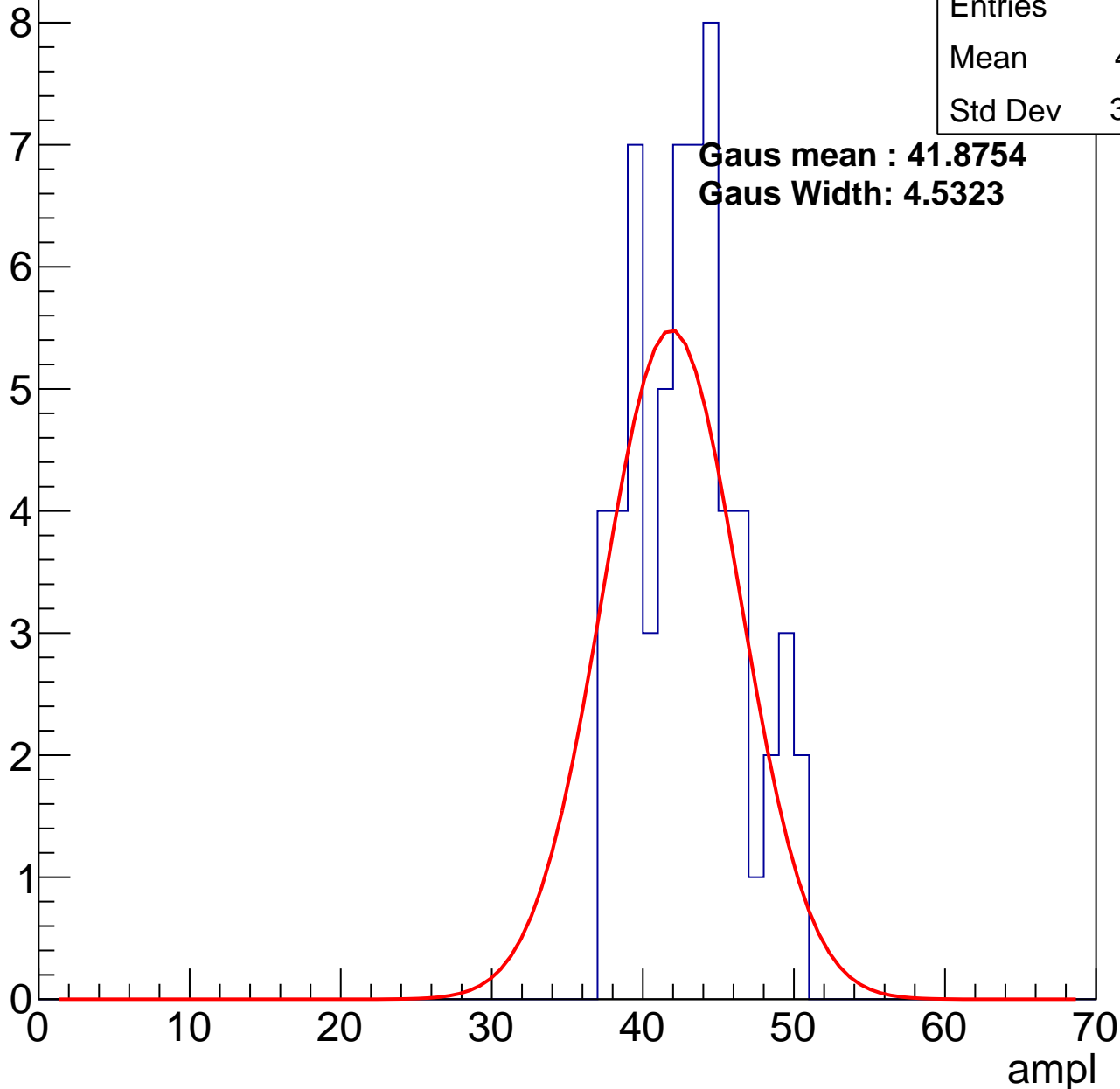
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	42.61
Std Dev	3.465

**Gaus mean : 41.8754**

**Gaus Width: 4.5323**

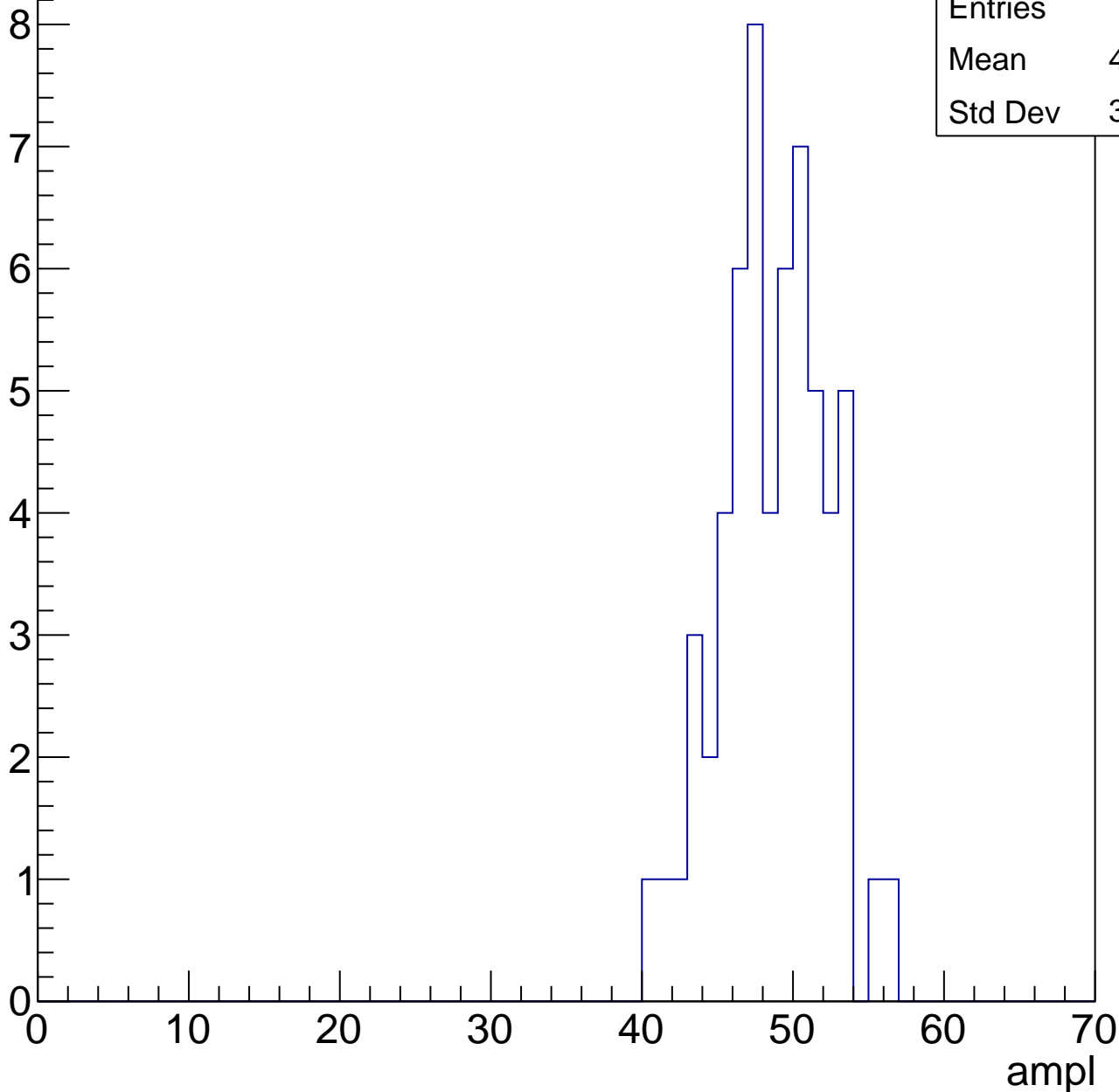


# B1L102S, U16-ch61, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	48.25
Std Dev	3.447

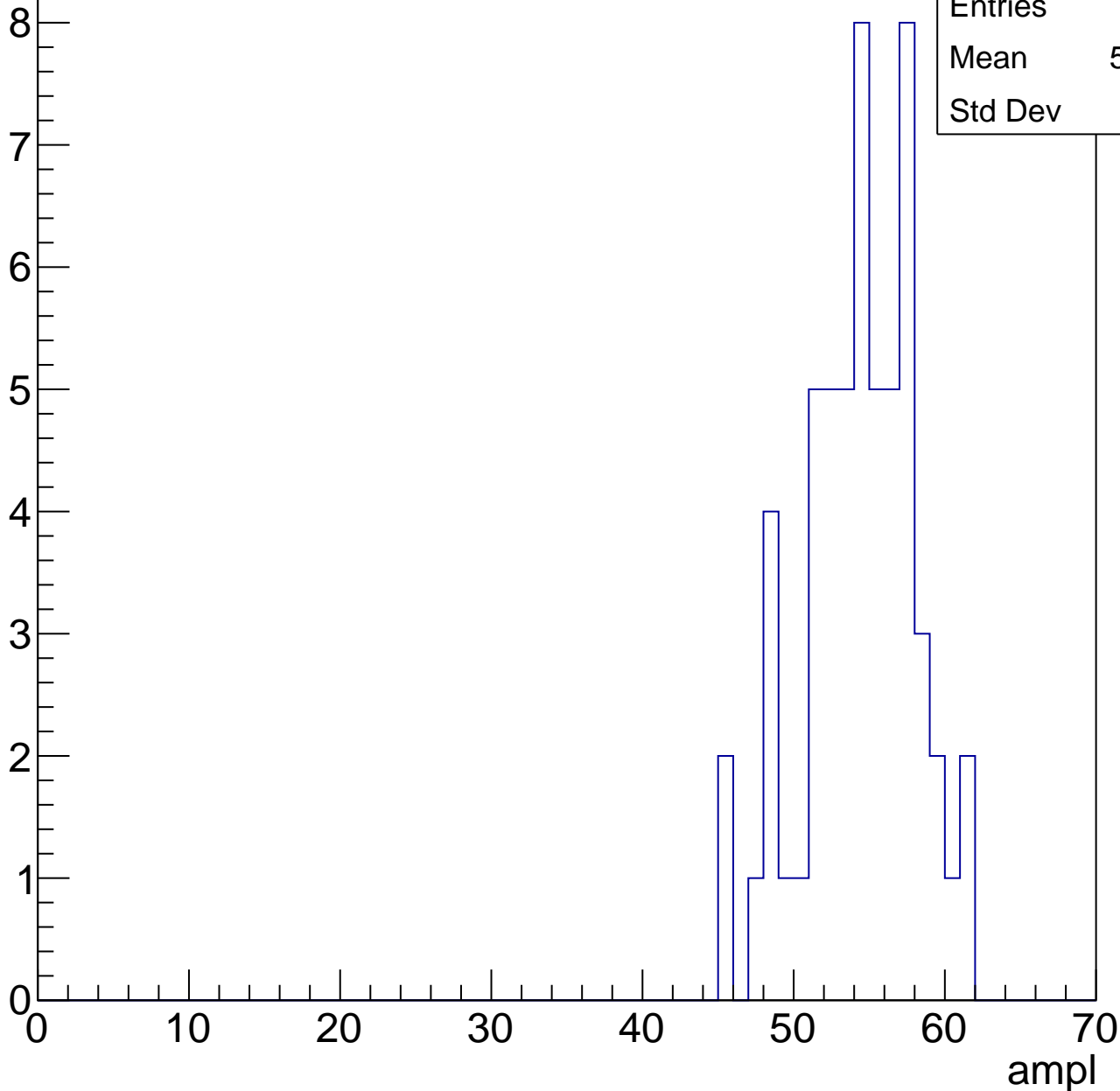


# B1L102S, U16-ch61, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	53.88
Std Dev	3.7

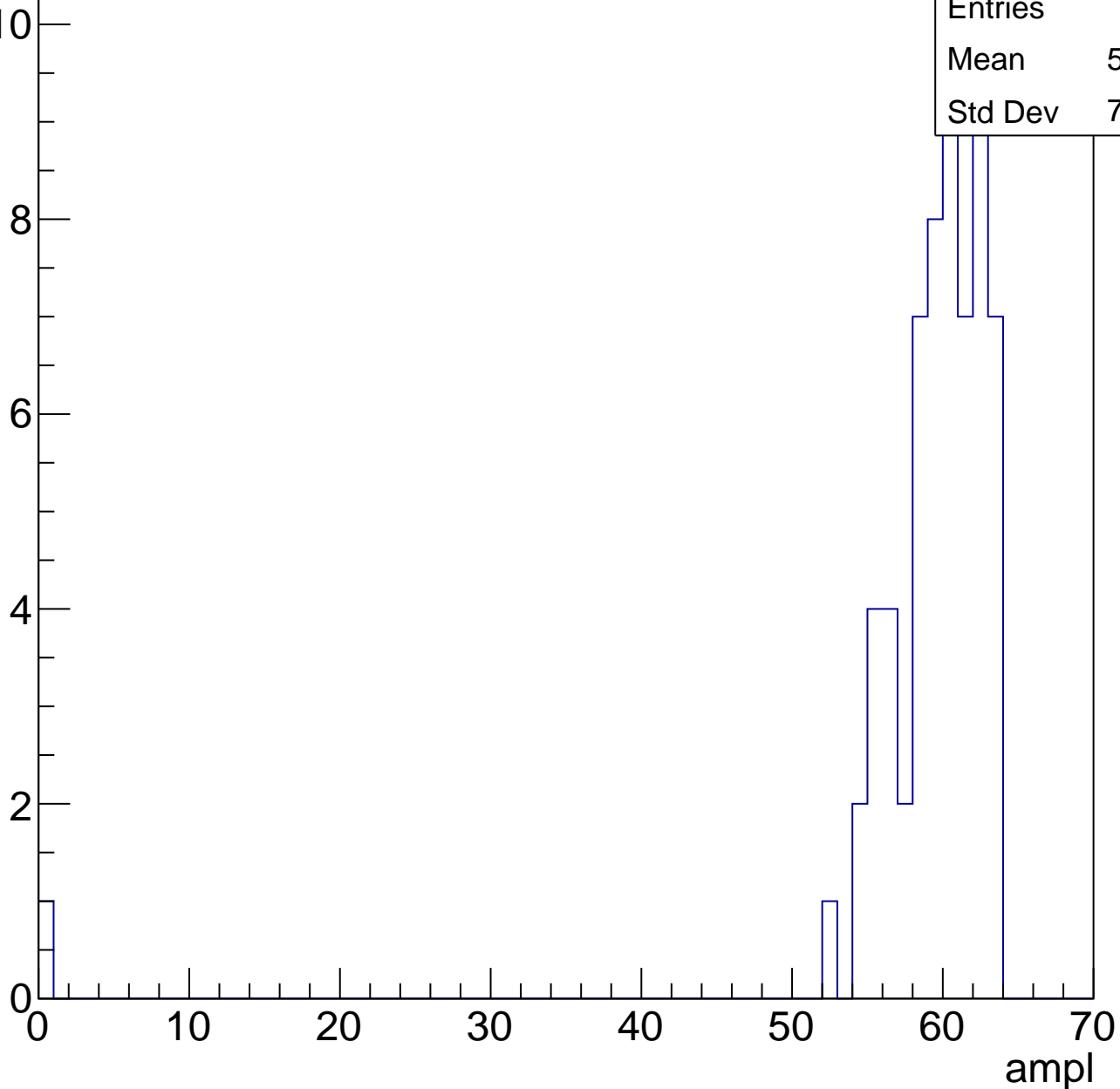


# B1L102S, U16-ch61, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	58.45
Std Dev	7.947



# B1L102S, U16-ch61, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch61, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

1  
0.8  
0.6  
0.4  
0.2  
0

Entries	1
Mean	21
Std Dev	0

ampl

# B1L102S, U16-ch62, adc0

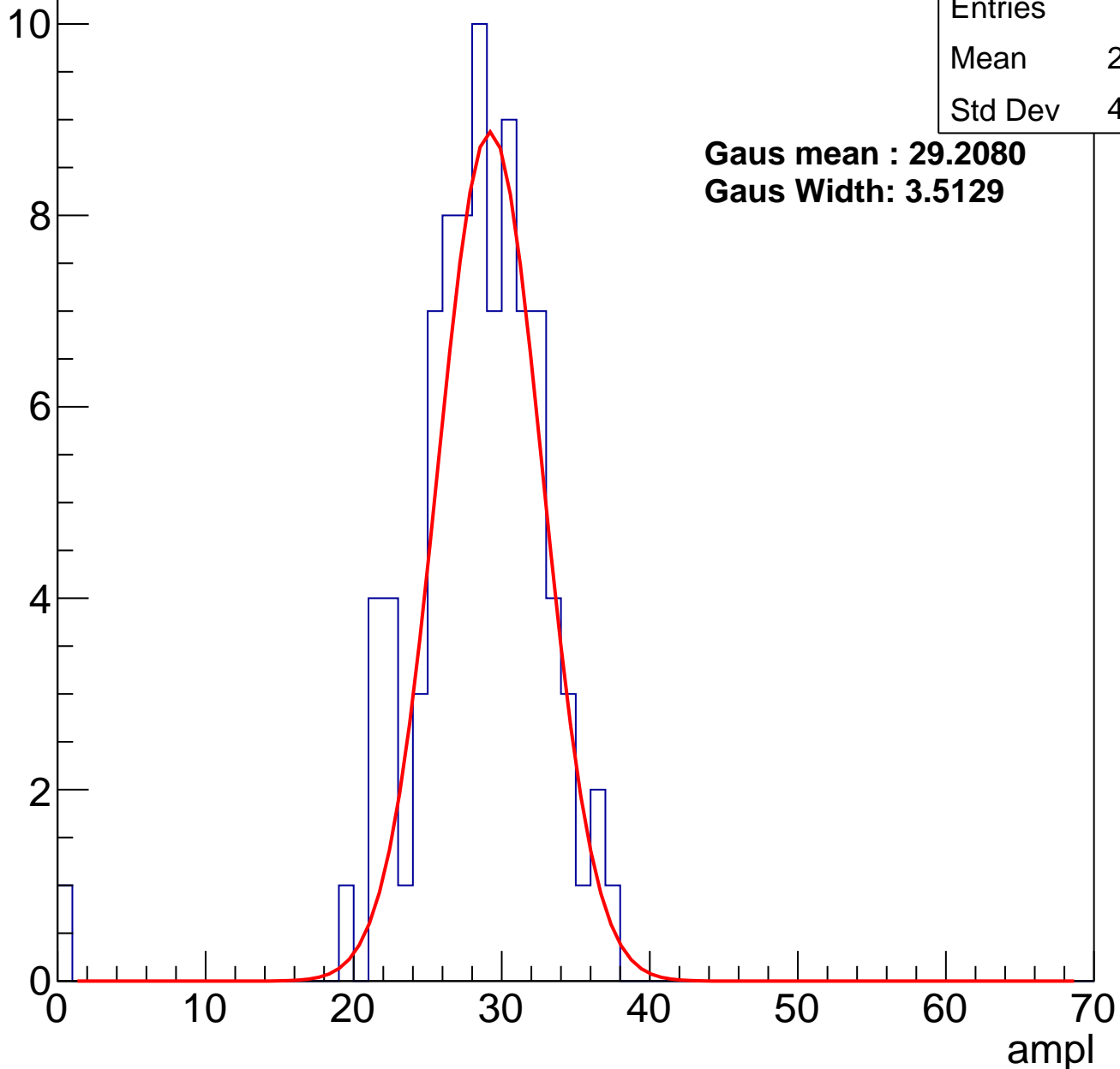
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	88
Mean	27.92
Std Dev	4.844

**Gaus mean : 29.2080**

**Gaus Width: 3.5129**

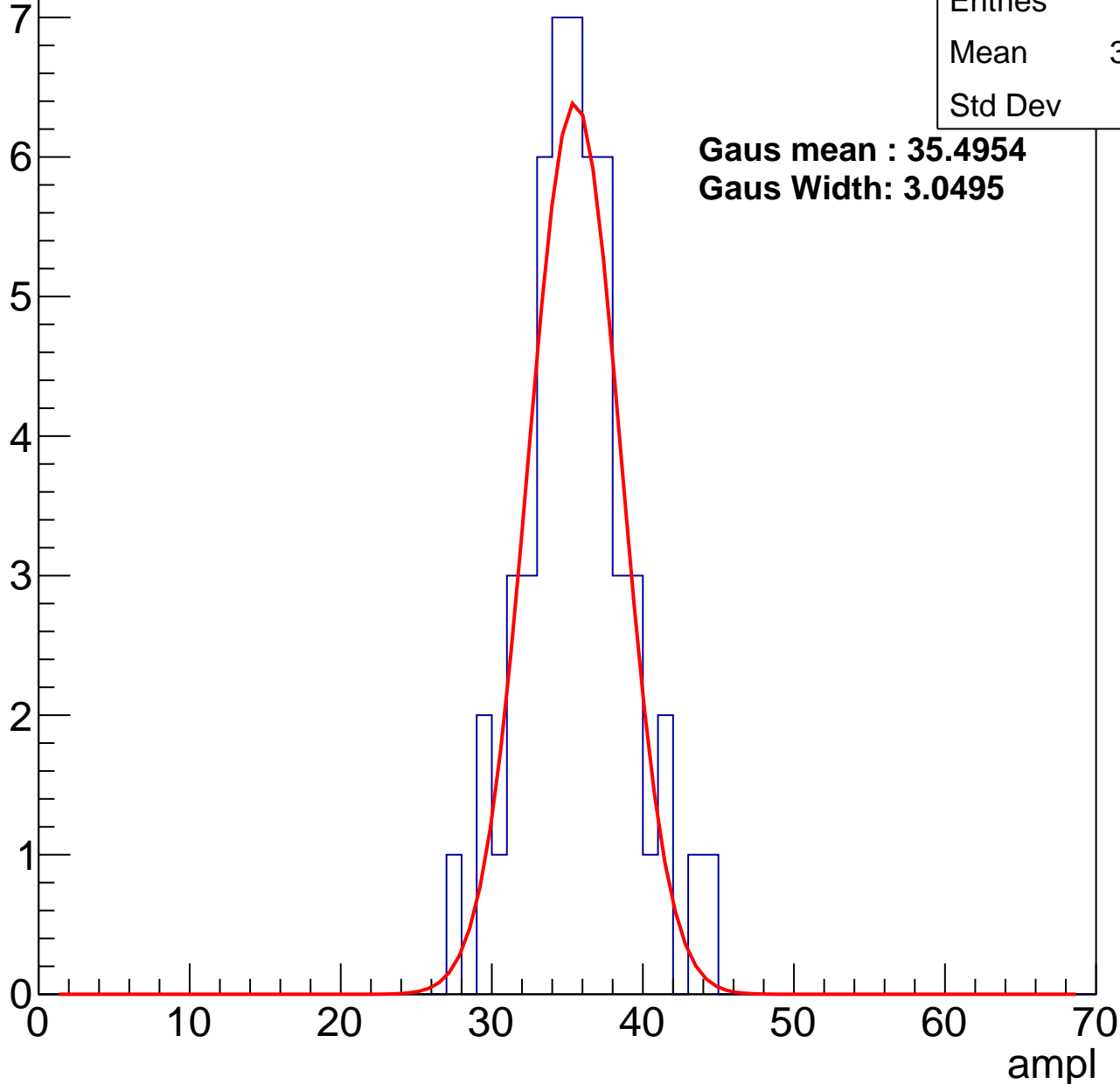
Entry



# B1L102S, U16-ch62, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch62, adc2

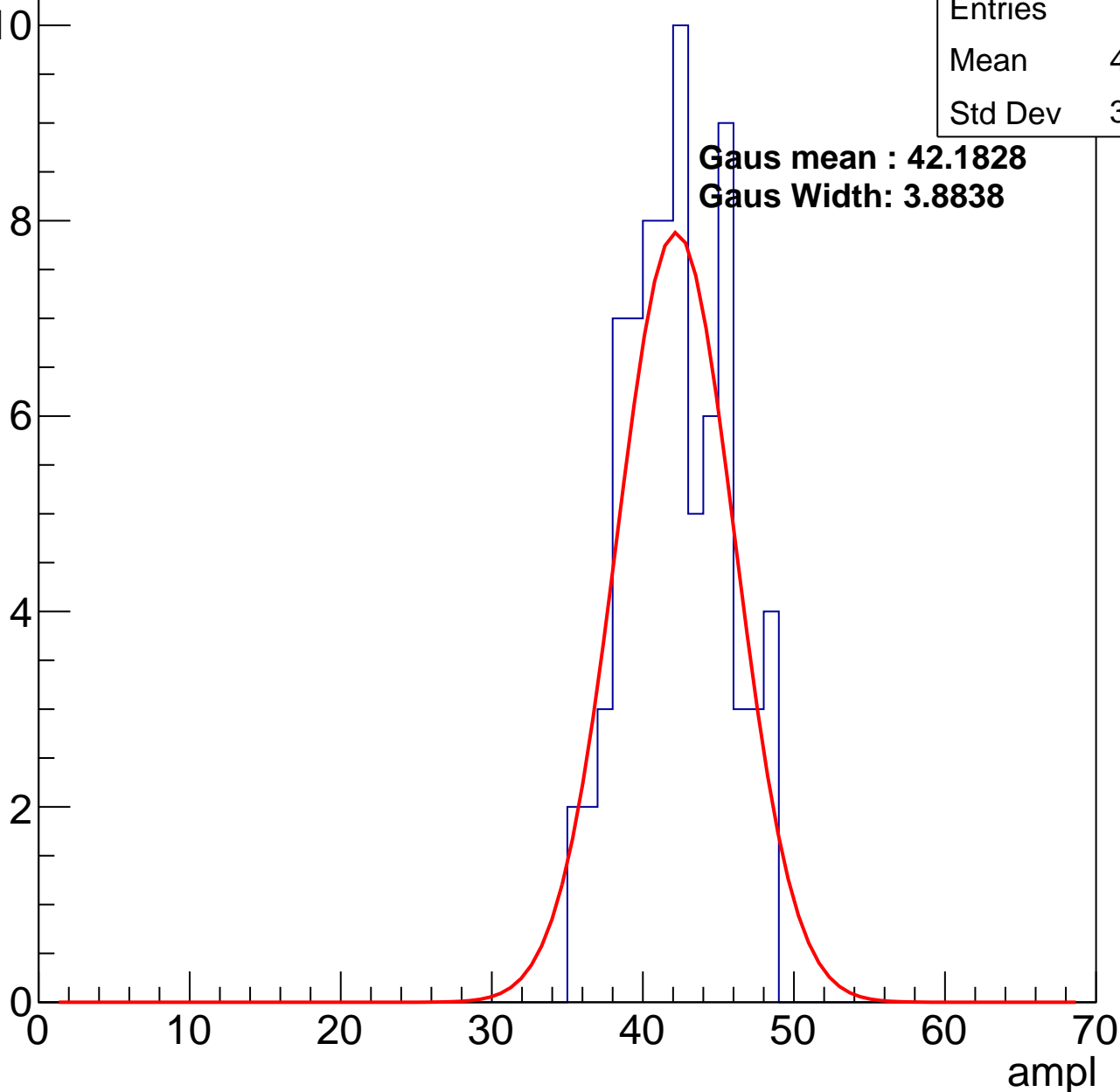
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	41.75
Std Dev	3.288

**Gaus mean : 42.1828**

**Gaus Width: 3.8838**

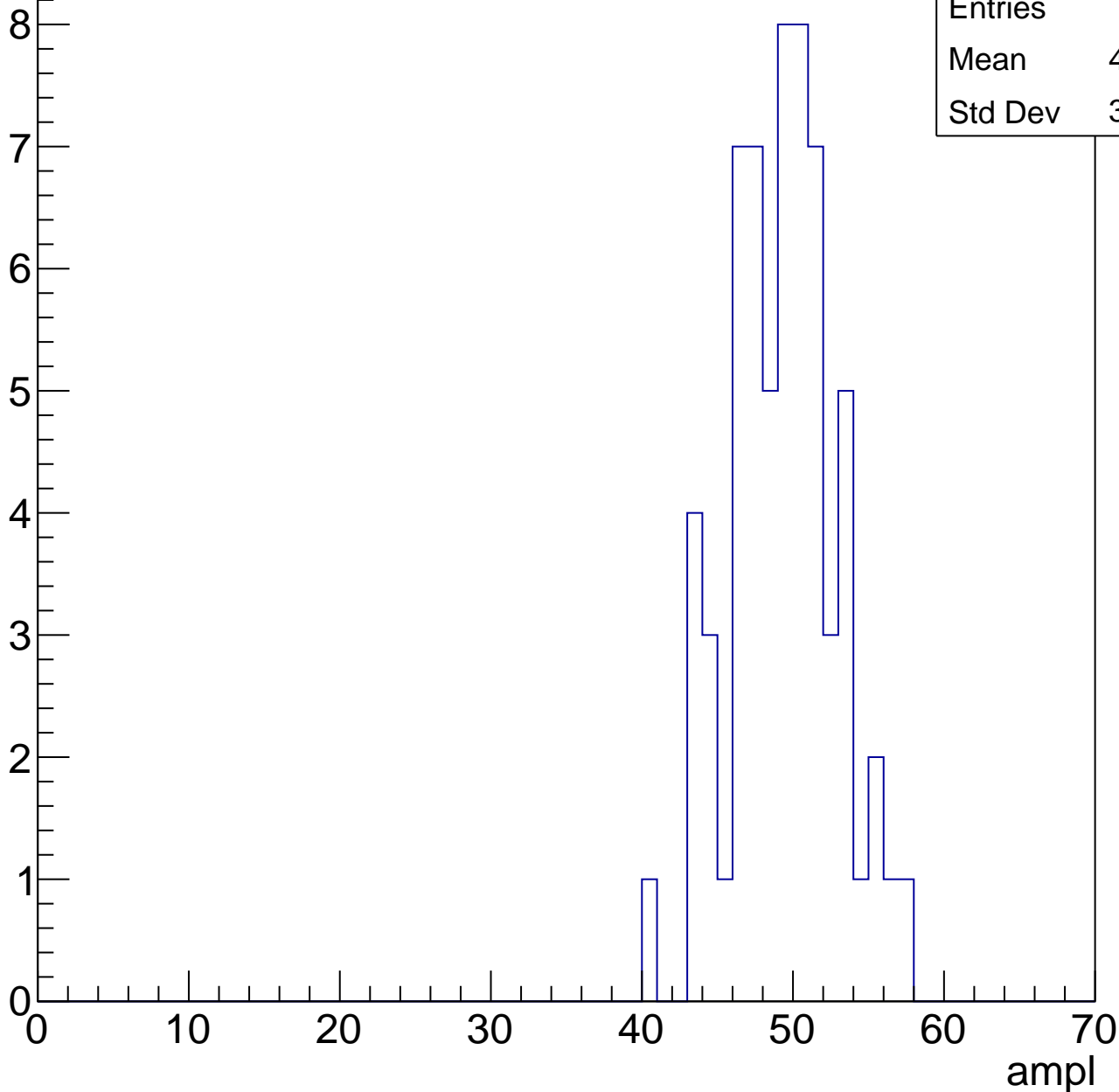


# B1L102S, U16-ch62, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	48.86
Std Dev	3.454

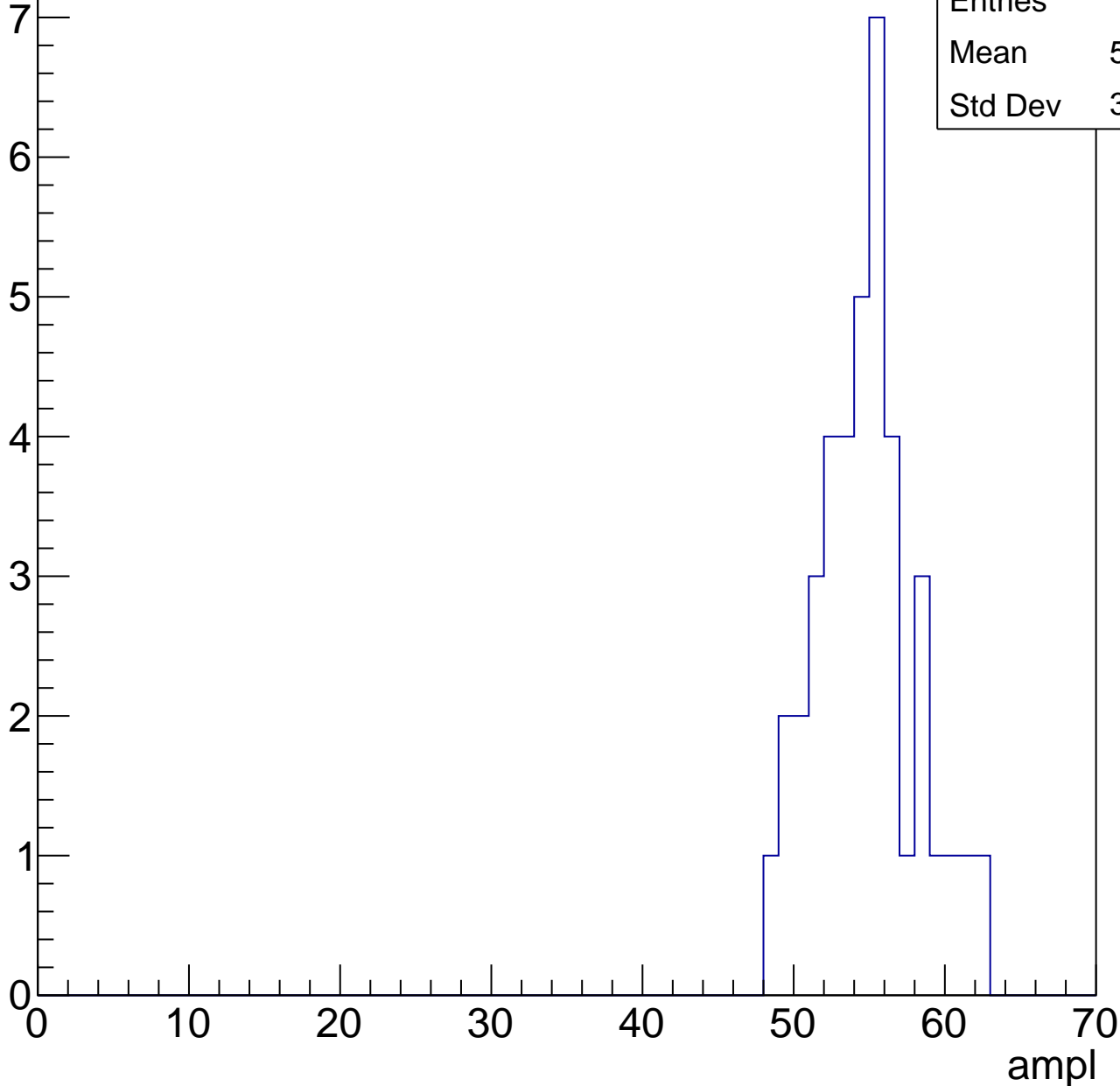


# B1L102S, U16-ch62, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

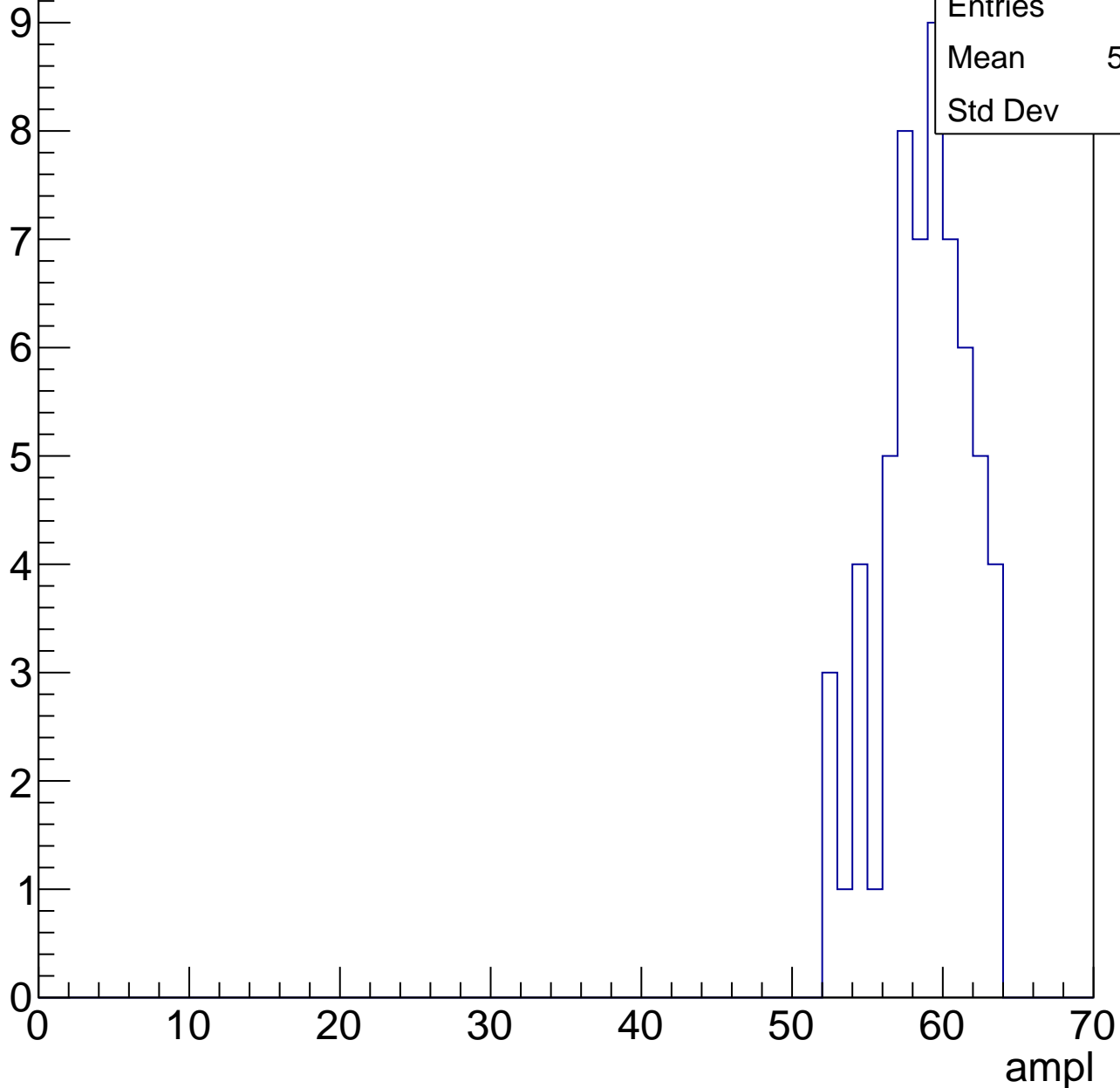
Entries	40
Mean	54.27
Std Dev	3.225



# B1L102S, U16-ch62, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

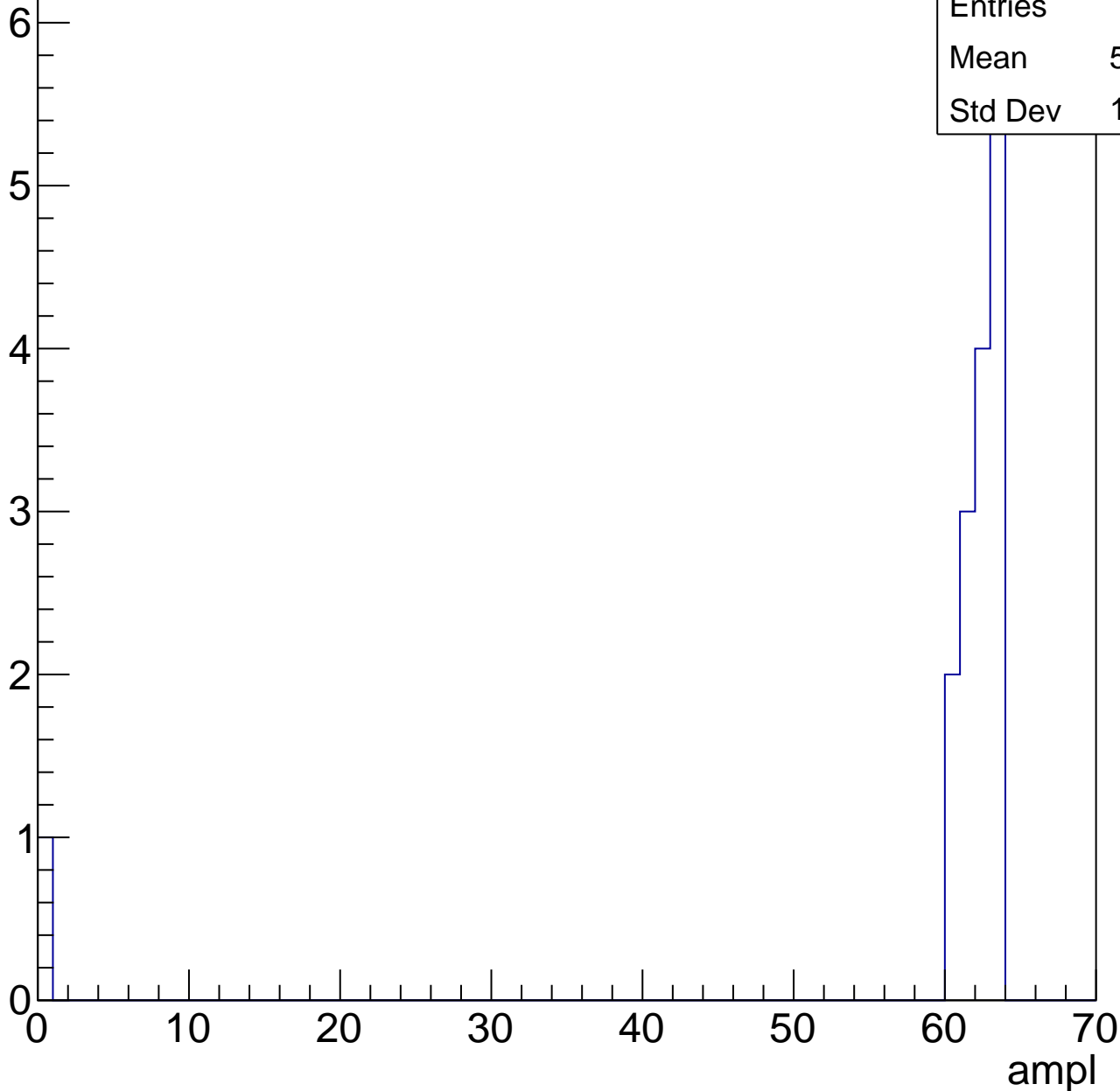


# B1L102S, U16-ch62, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	16
Mean	58.06
Std Dev	15.03





# B1L102S, U16-ch62, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U16-ch63, adc0

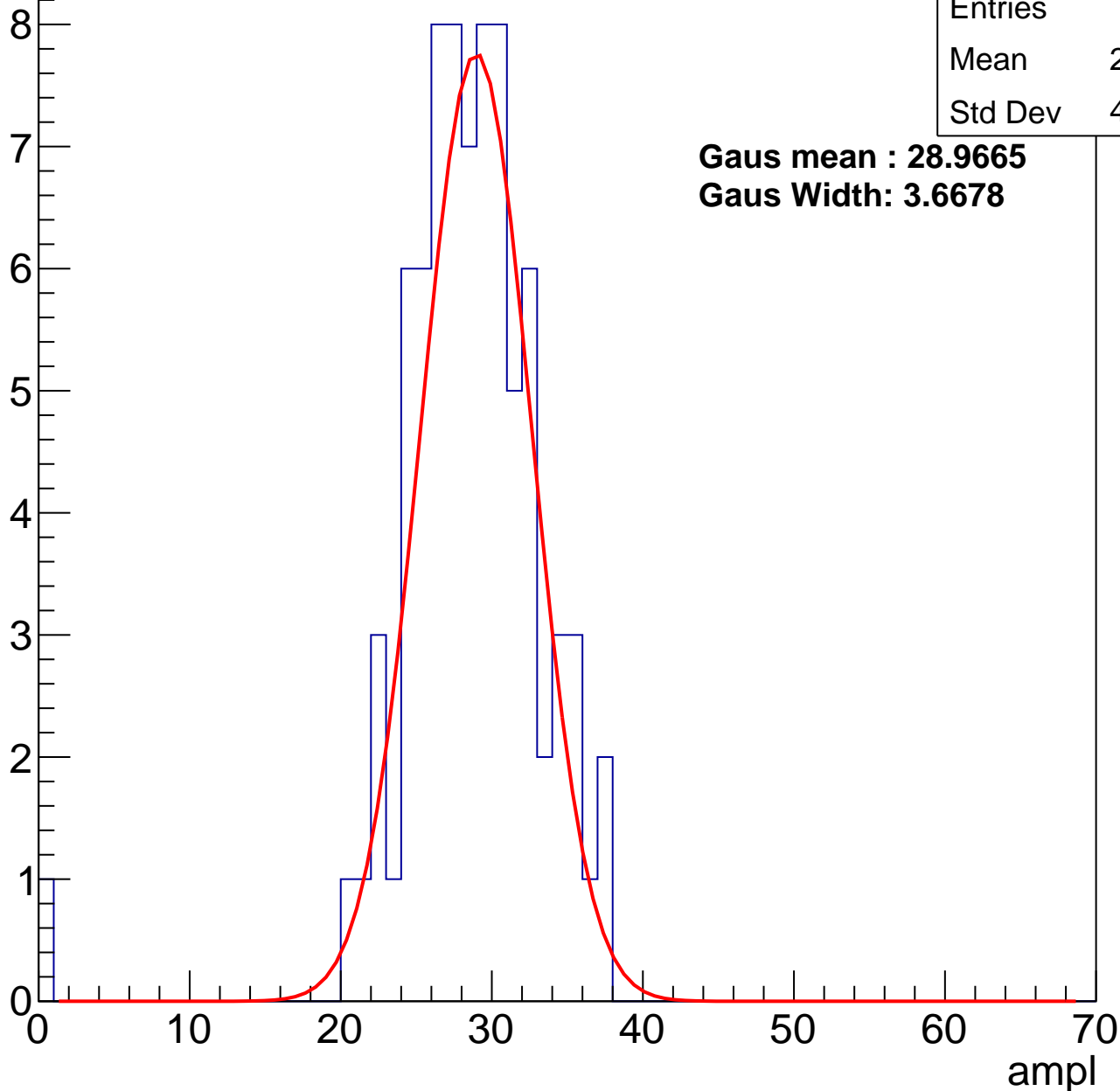
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	28.07
Std Dev	4.914

**Gaus mean : 28.9665**

**Gaus Width: 3.6678**



# B1L102S, U16-ch63, adc1

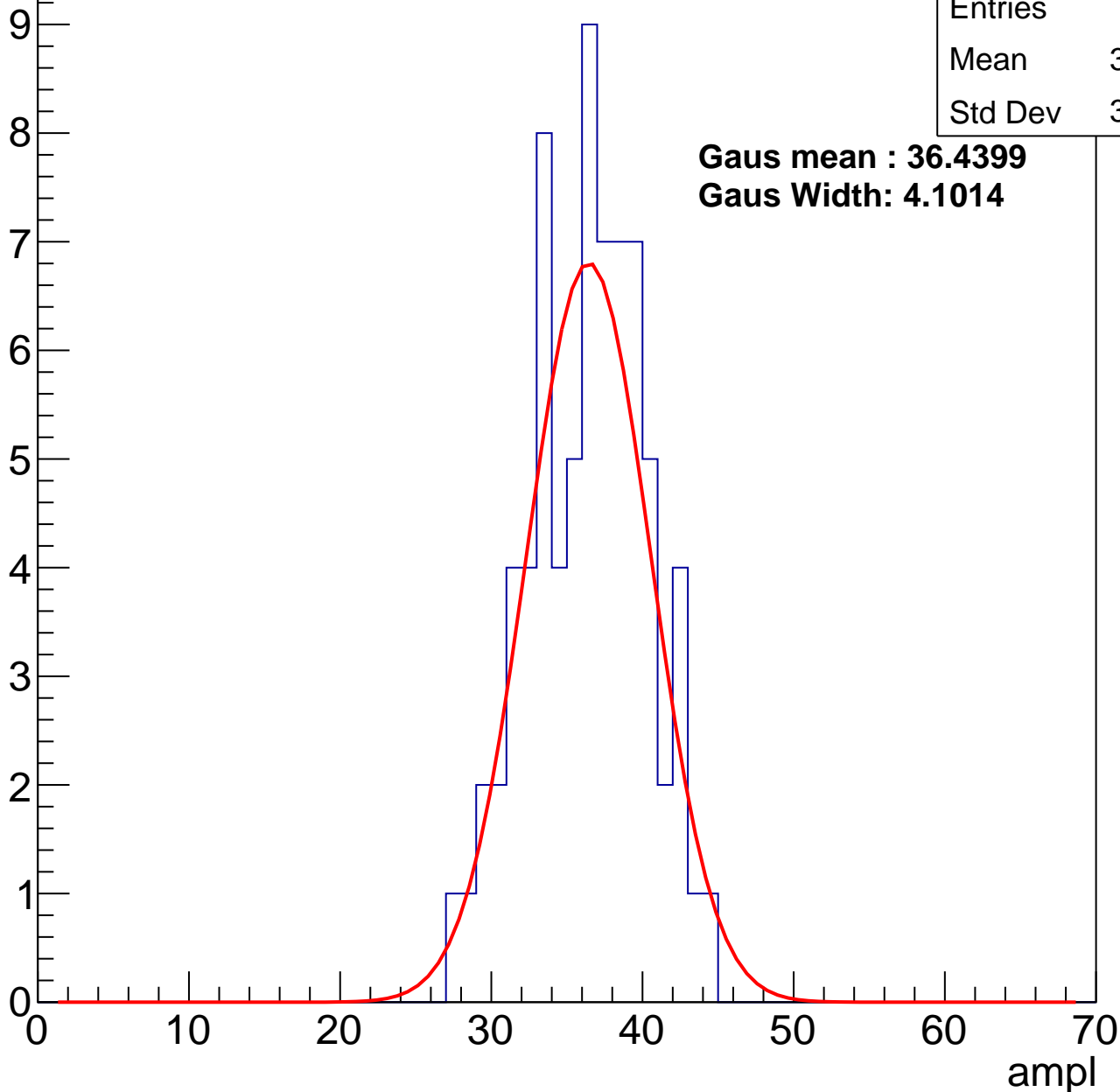
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	35.93
Std Dev	3.779

**Gaus mean : 36.4399**

**Gaus Width: 4.1014**



# B1L102S, U16-ch63, adc2

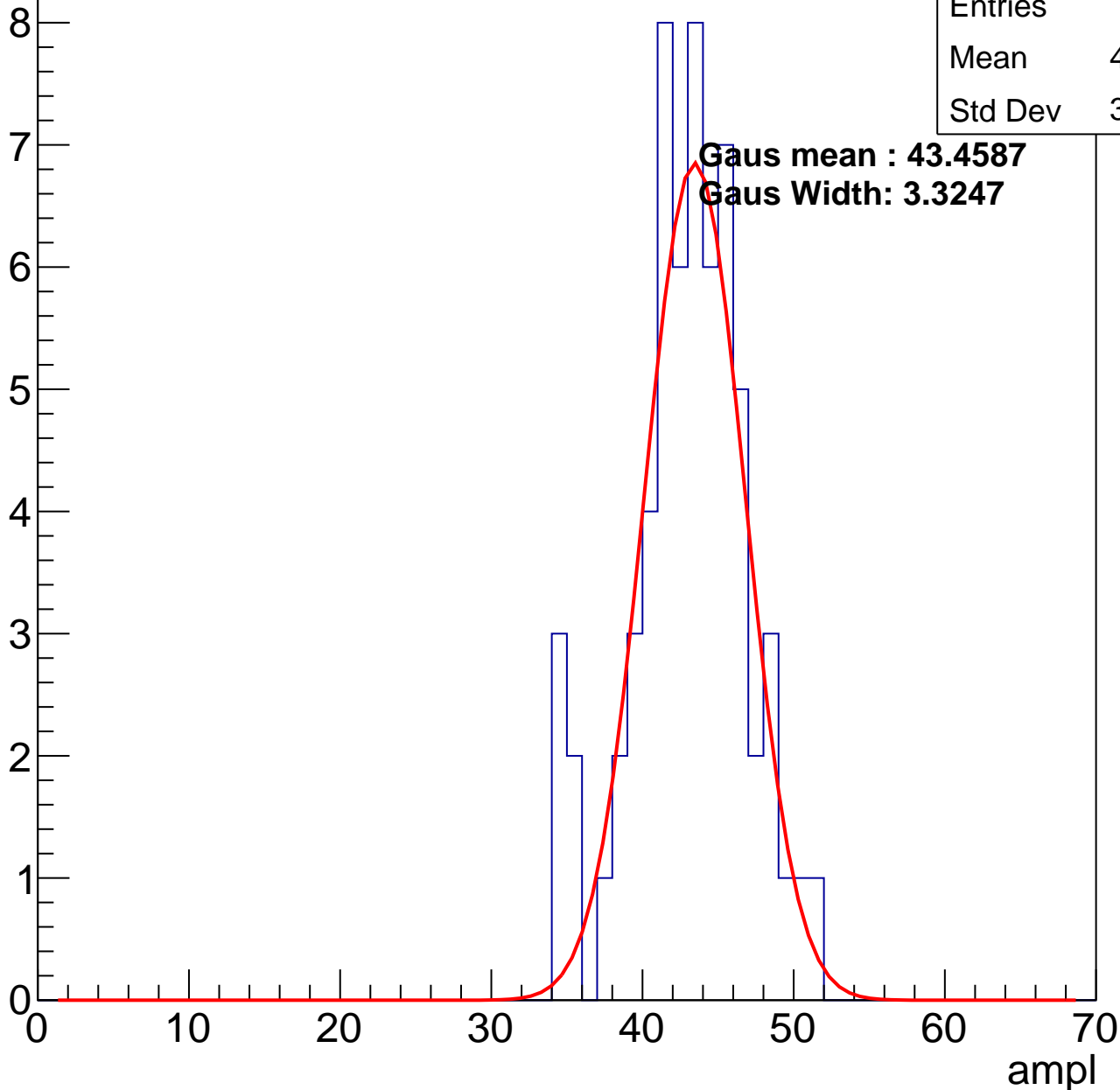
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	42.59
Std Dev	3.787

**Gaus mean : 43.4587**

**Gaus Width: 3.3247**

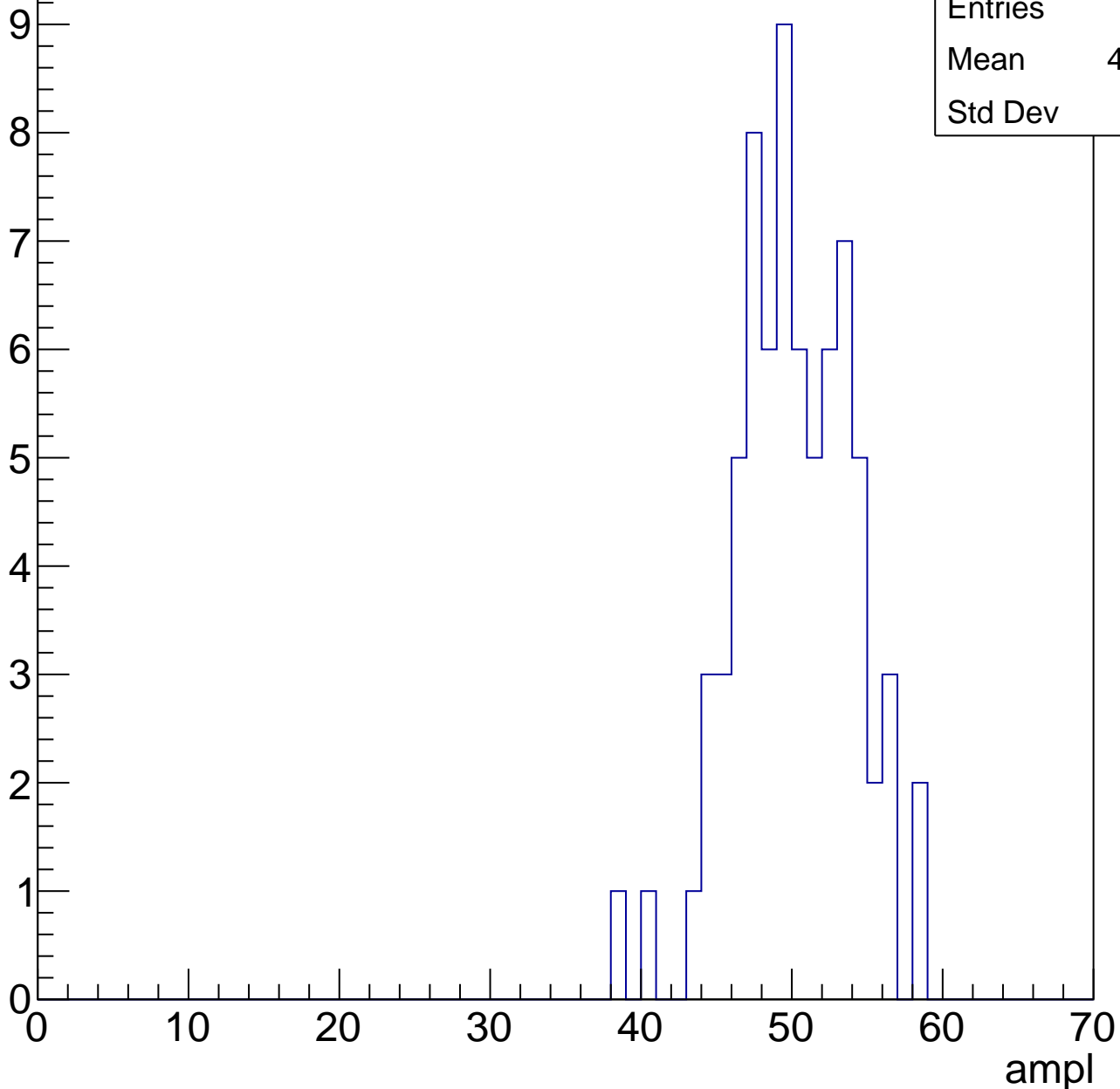


# B1L102S, U16-ch63, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	49.66
Std Dev	3.9

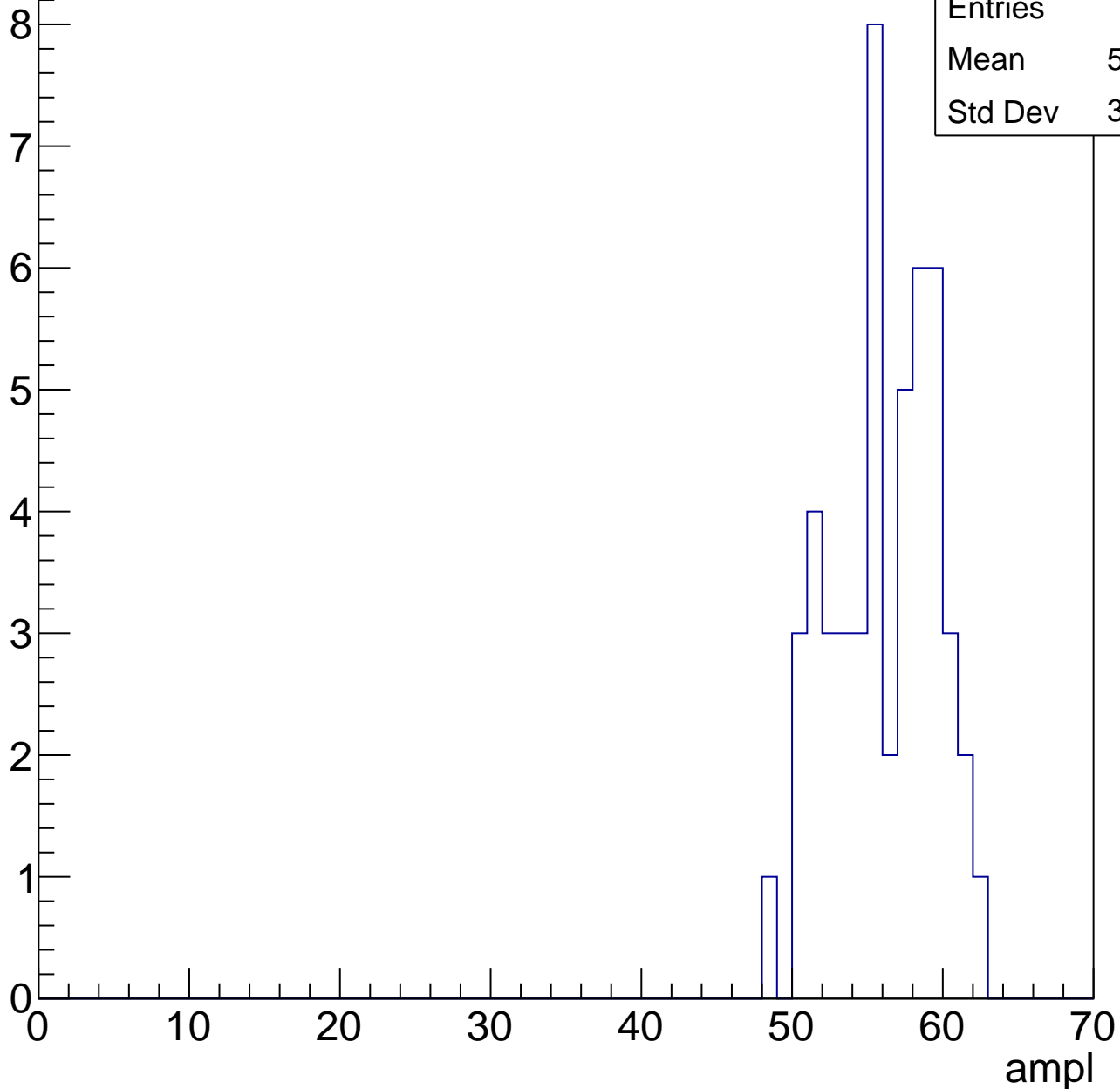


# B1L102S, U16-ch63, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	55.64
Std Dev	3.399

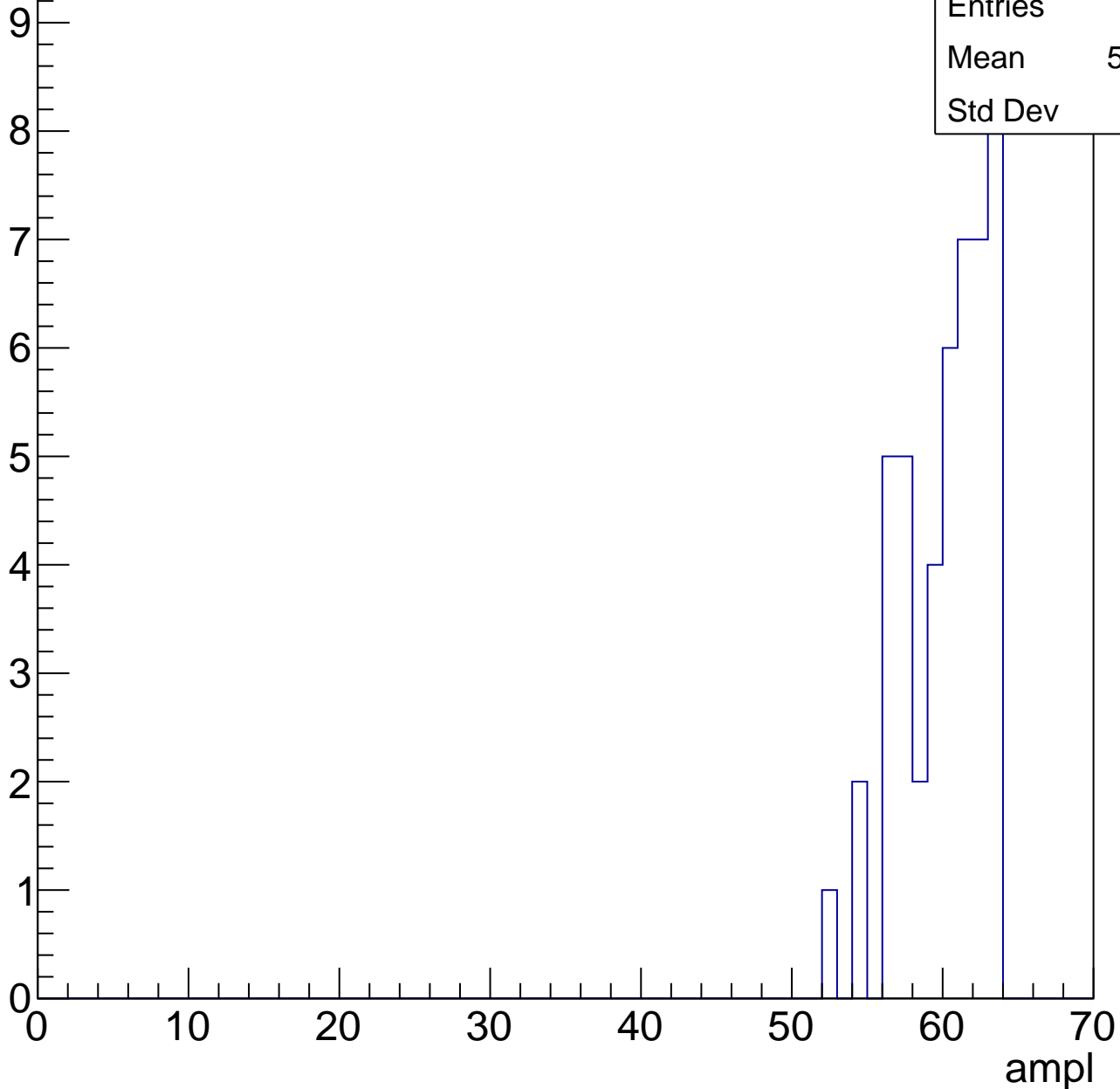


# B1L102S, U16-ch63, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

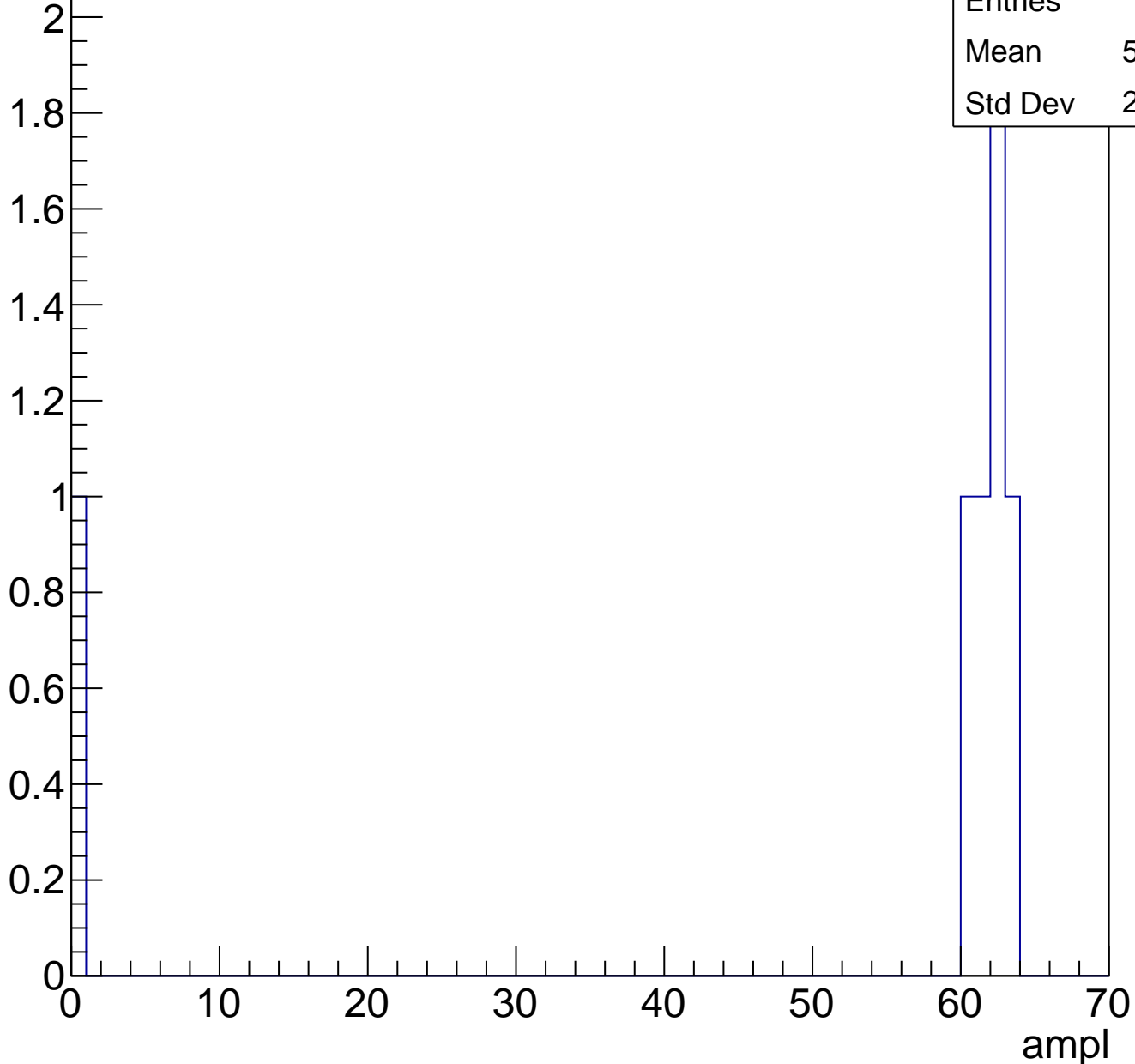
Entries	48
Mean	59.69
Std Dev	2.83



# B1L102S, U16-ch63, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



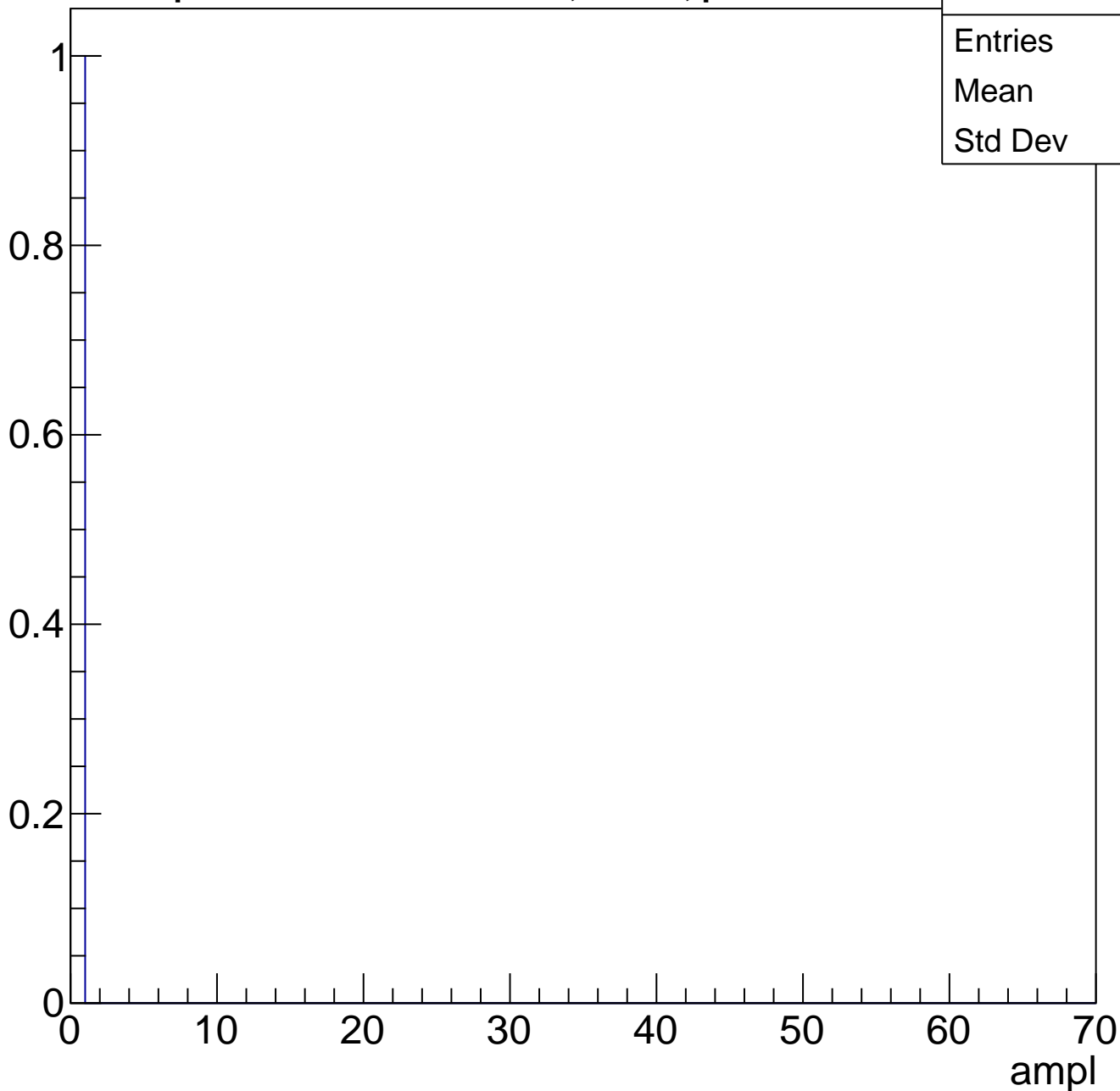
Entries	6
Mean	51.33
Std Dev	22.98



# B1L102S, U16-ch63, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U16-ch64, adc0

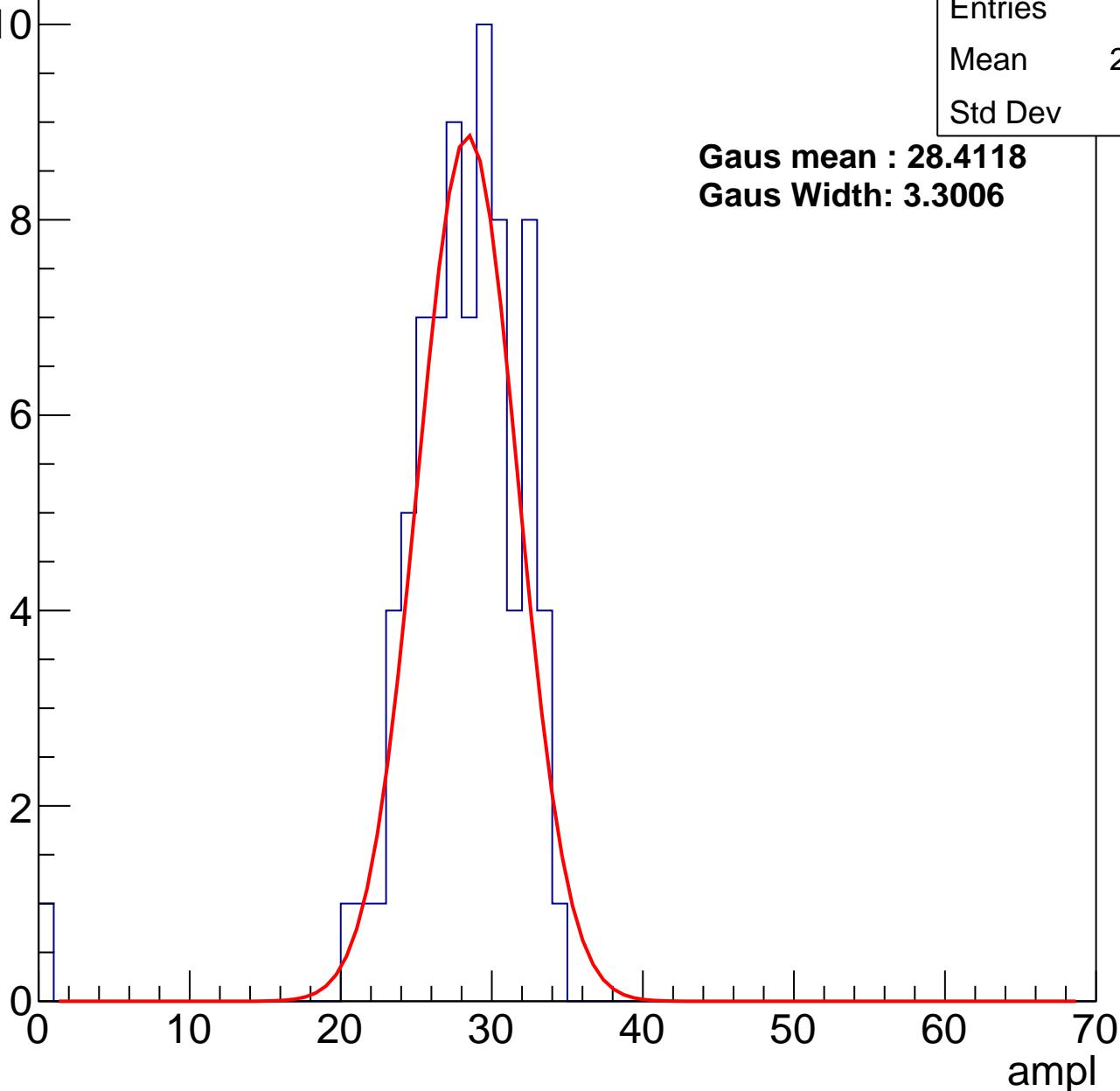
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	27.53
Std Dev	4.44

**Gaus mean : 28.4118**

**Gaus Width: 3.3006**



# B1L102S, U16-ch64, adc1

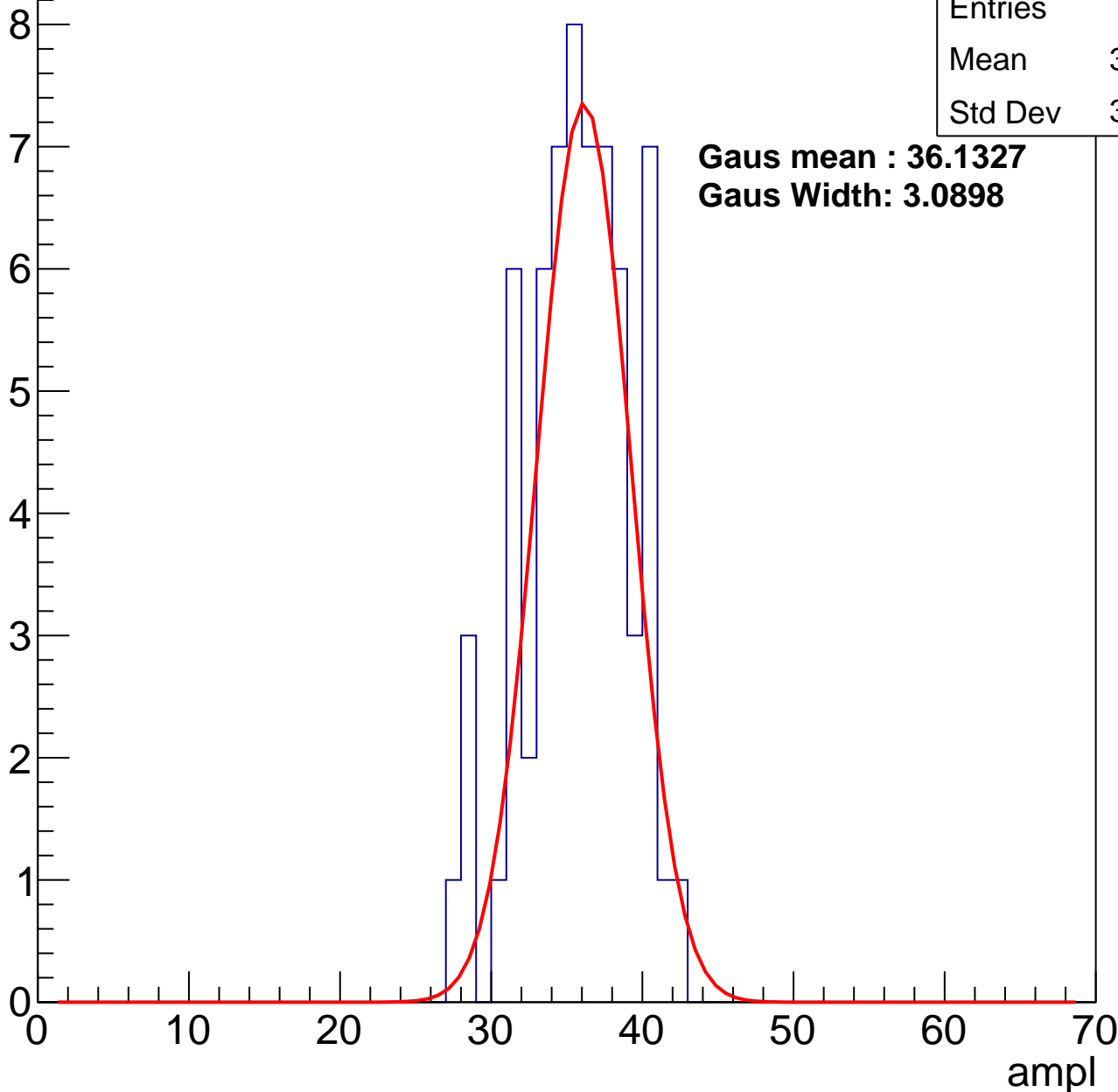
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	35.24
Std Dev	3.425

**Gaus mean : 36.1327**

**Gaus Width: 3.0898**



# B1L102S, U16-ch64, adc2

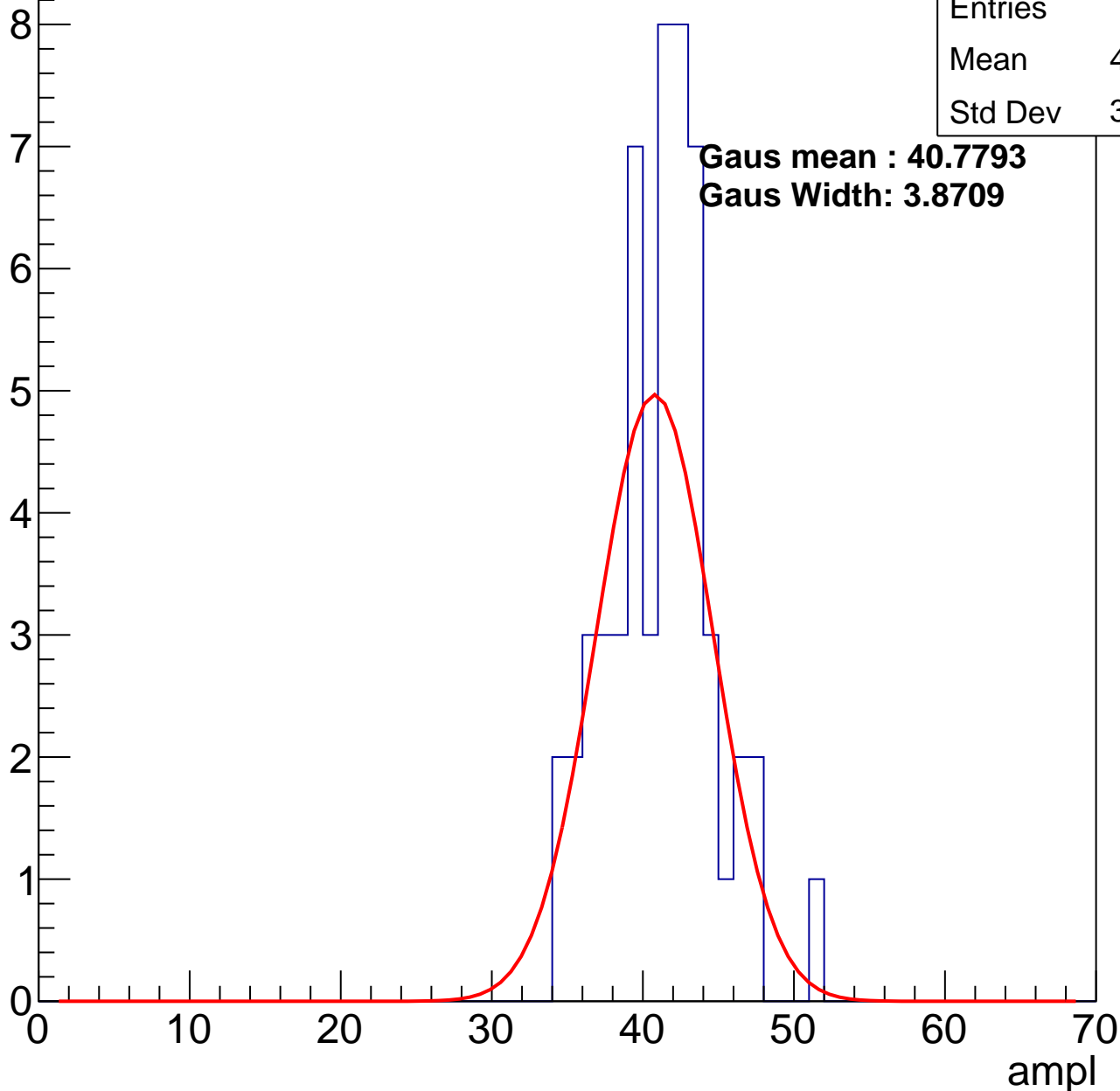
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	40.78
Std Dev	3.436

**Gaus mean : 40.7793**

**Gaus Width: 3.8709**

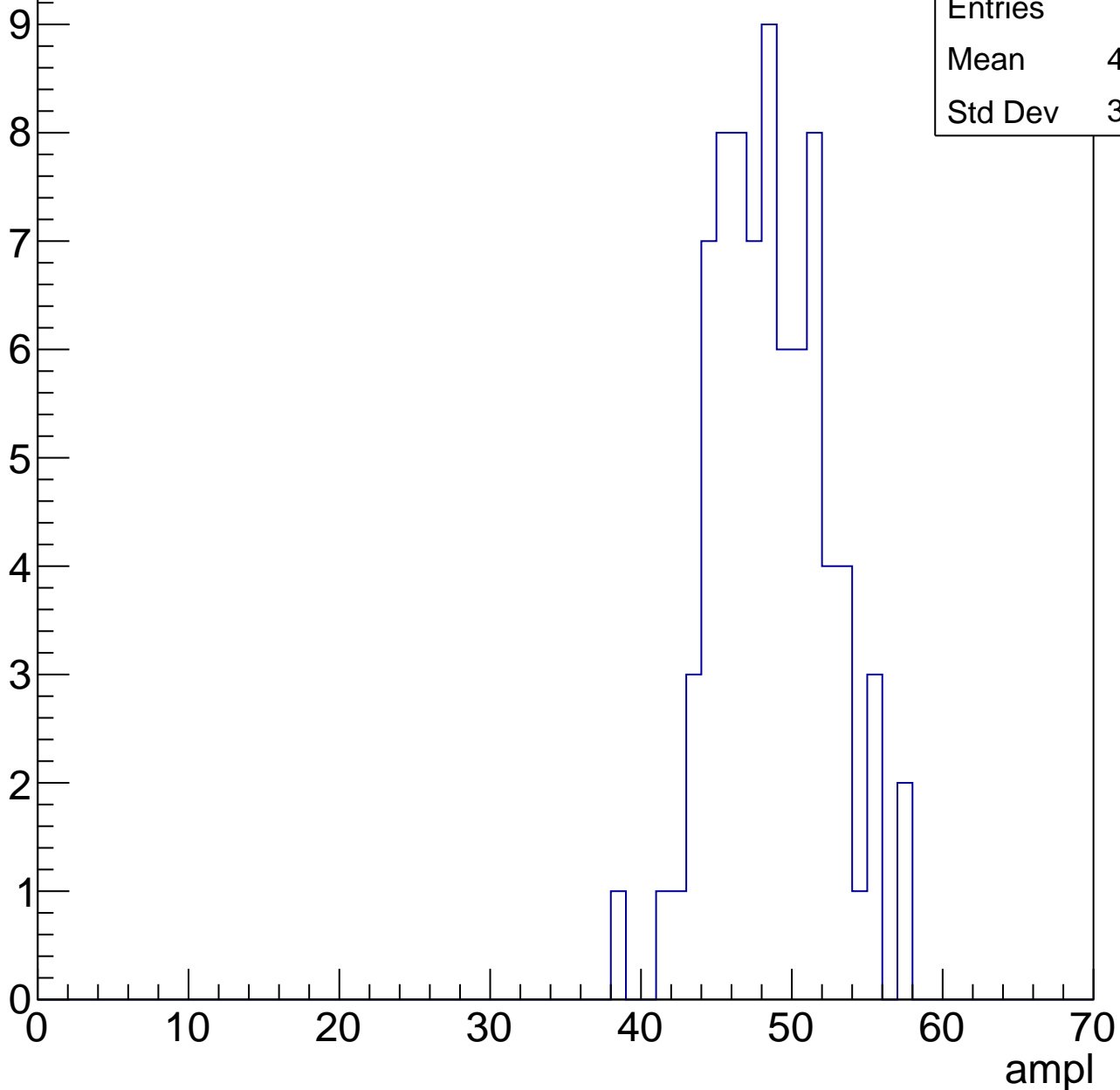


# B1L102S, U16-ch64, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	48.13
Std Dev	3.719

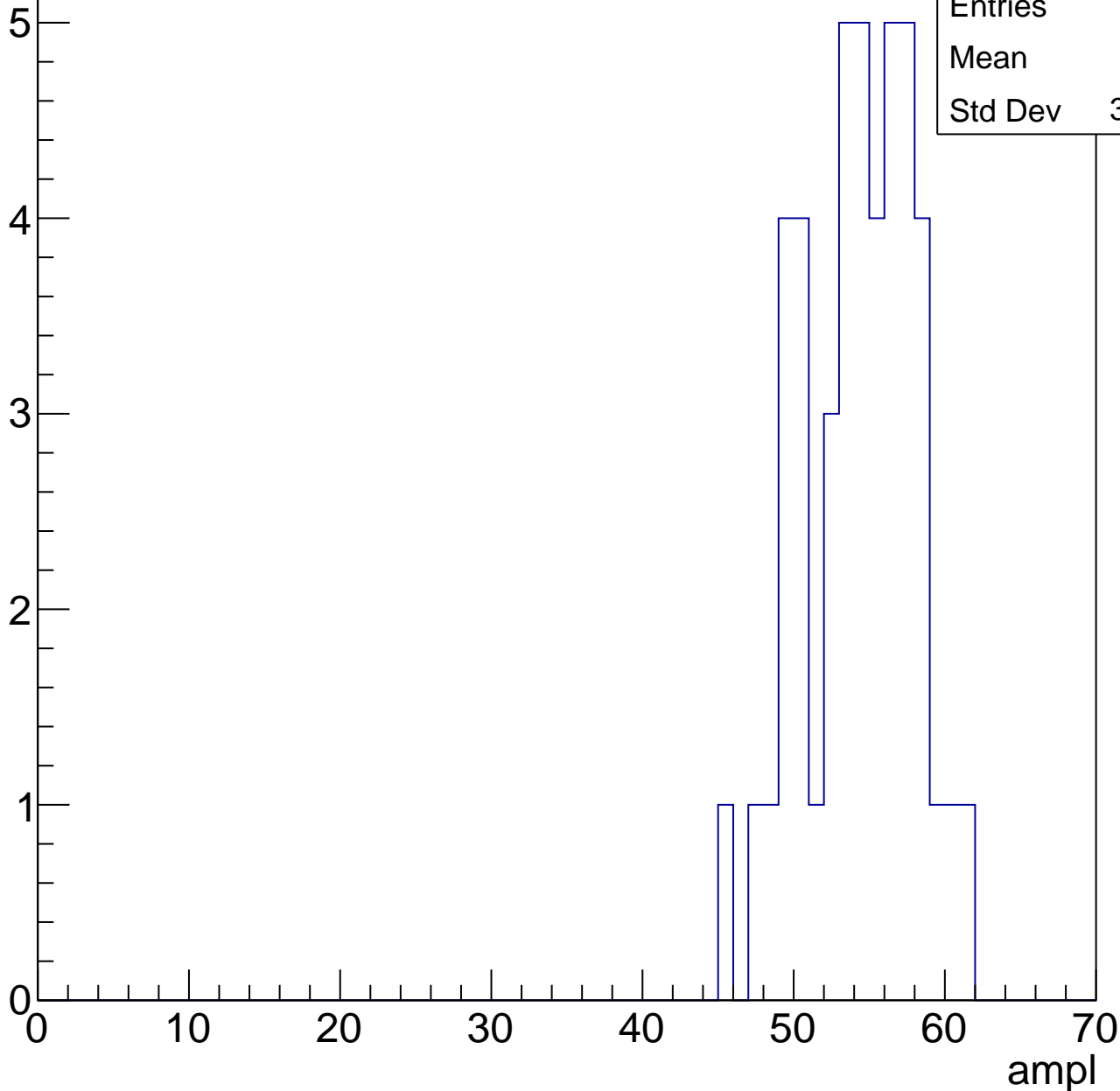


# B1L102S, U16-ch64, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

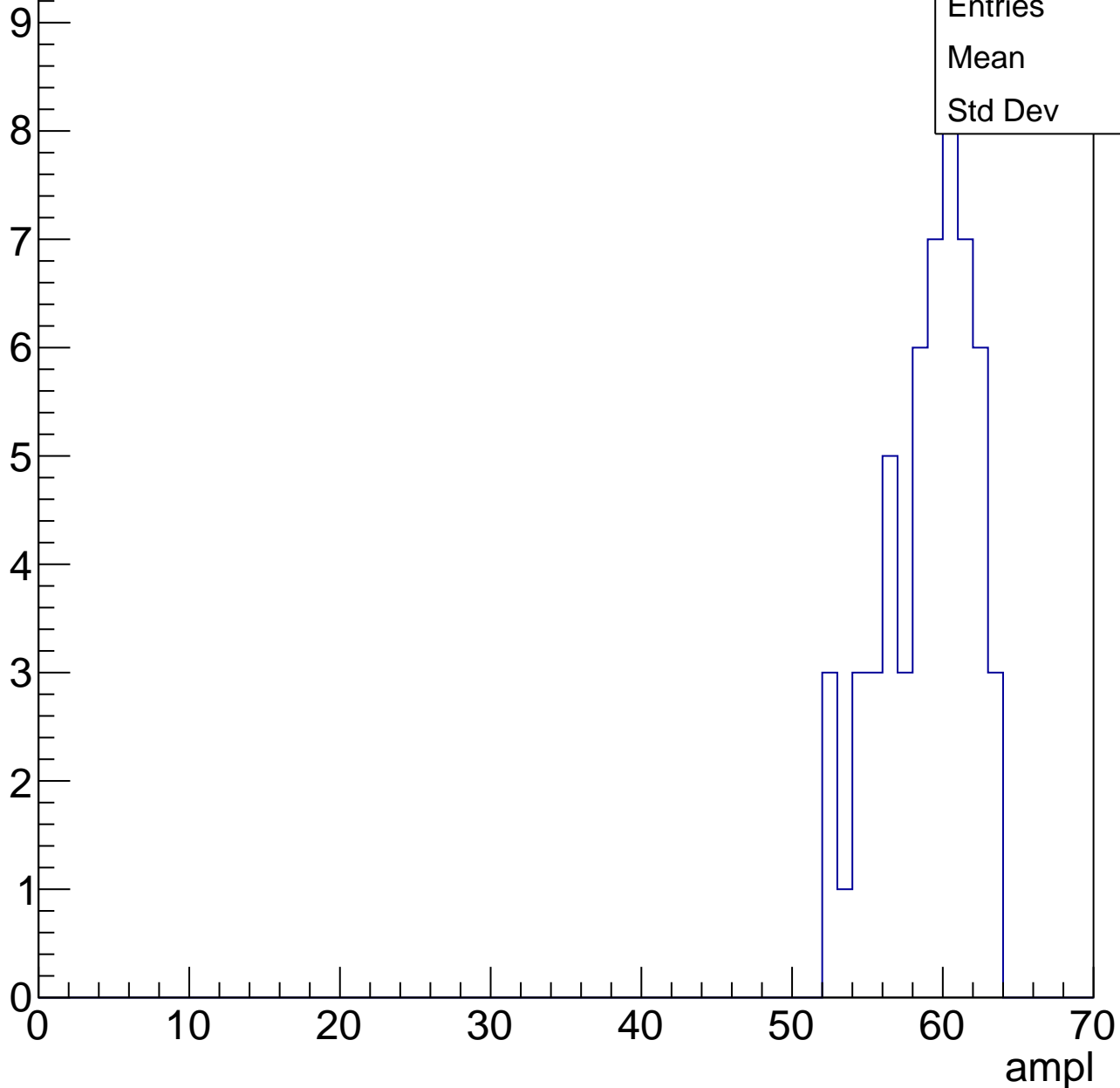
Entries	46
Mean	53.8
Std Dev	3.603



# B1L102S, U16-ch64, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

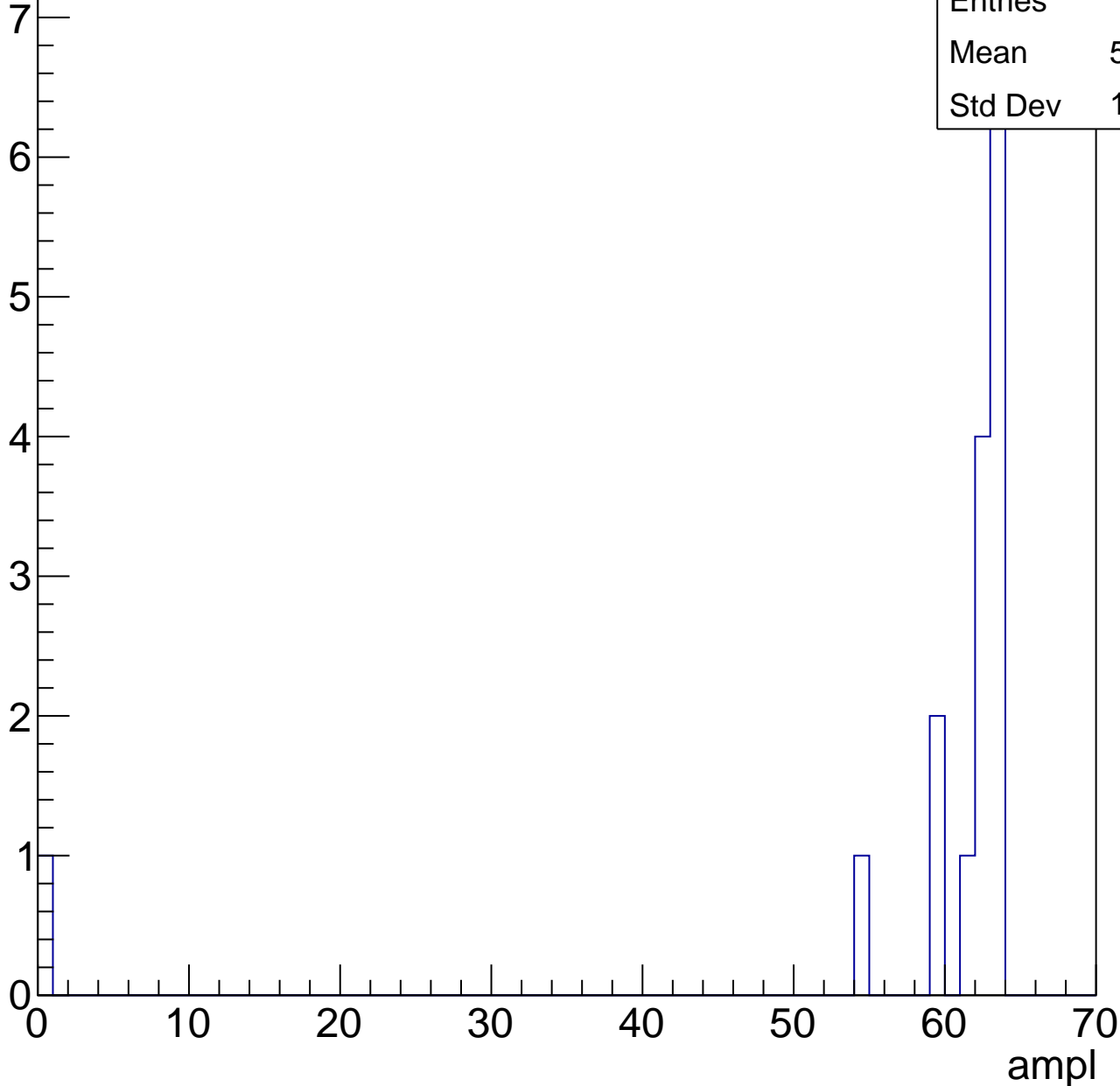


# B1L102S, U16-ch64, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	16
Mean	57.62
Std Dev	15.06





# B1L102S, U16-ch64, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch65, adc0

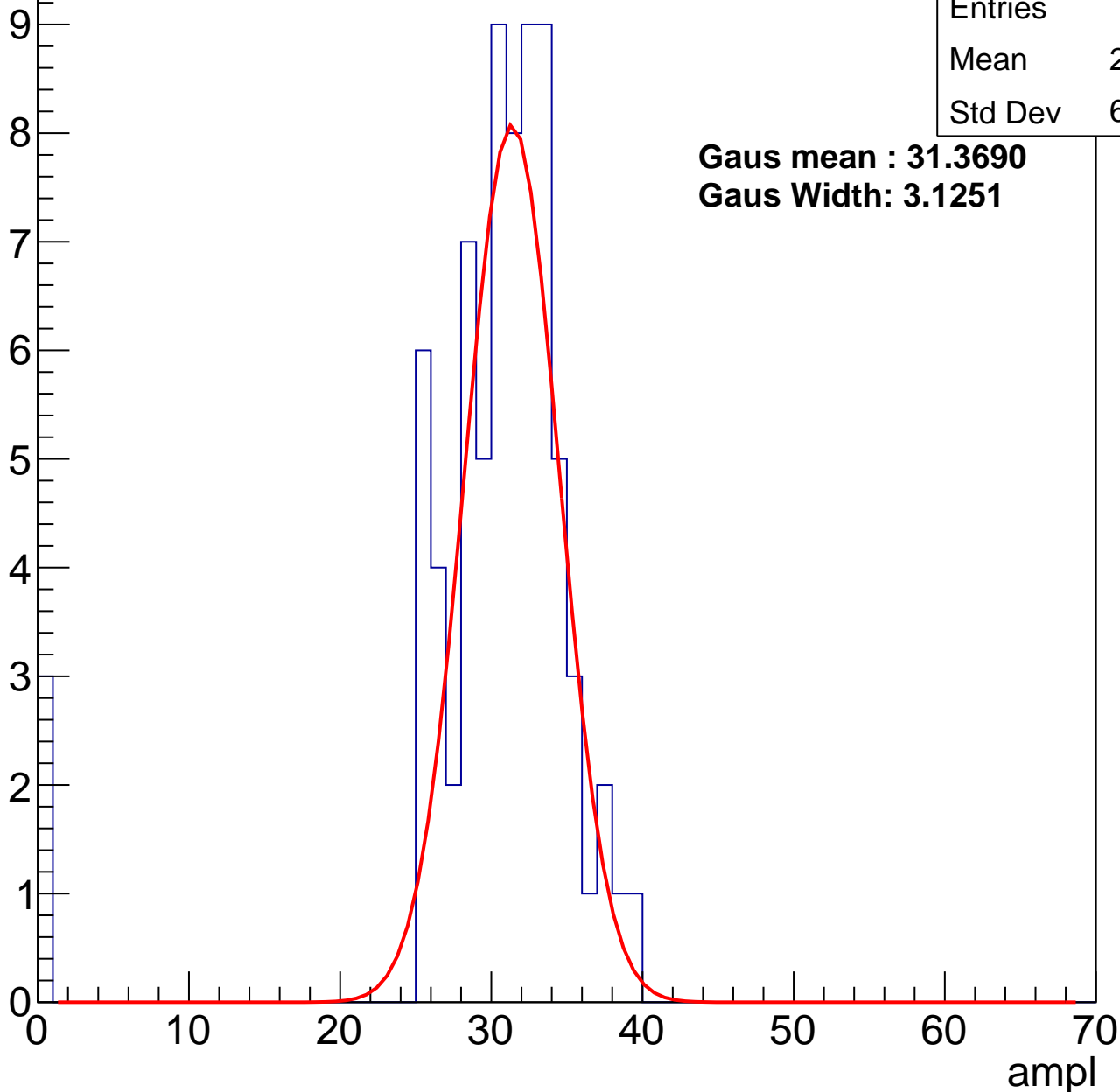
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	29.52
Std Dev	6.838

**Gaus mean : 31.3690**

**Gaus Width: 3.1251**



# B1L102S, U16-ch65, adc1

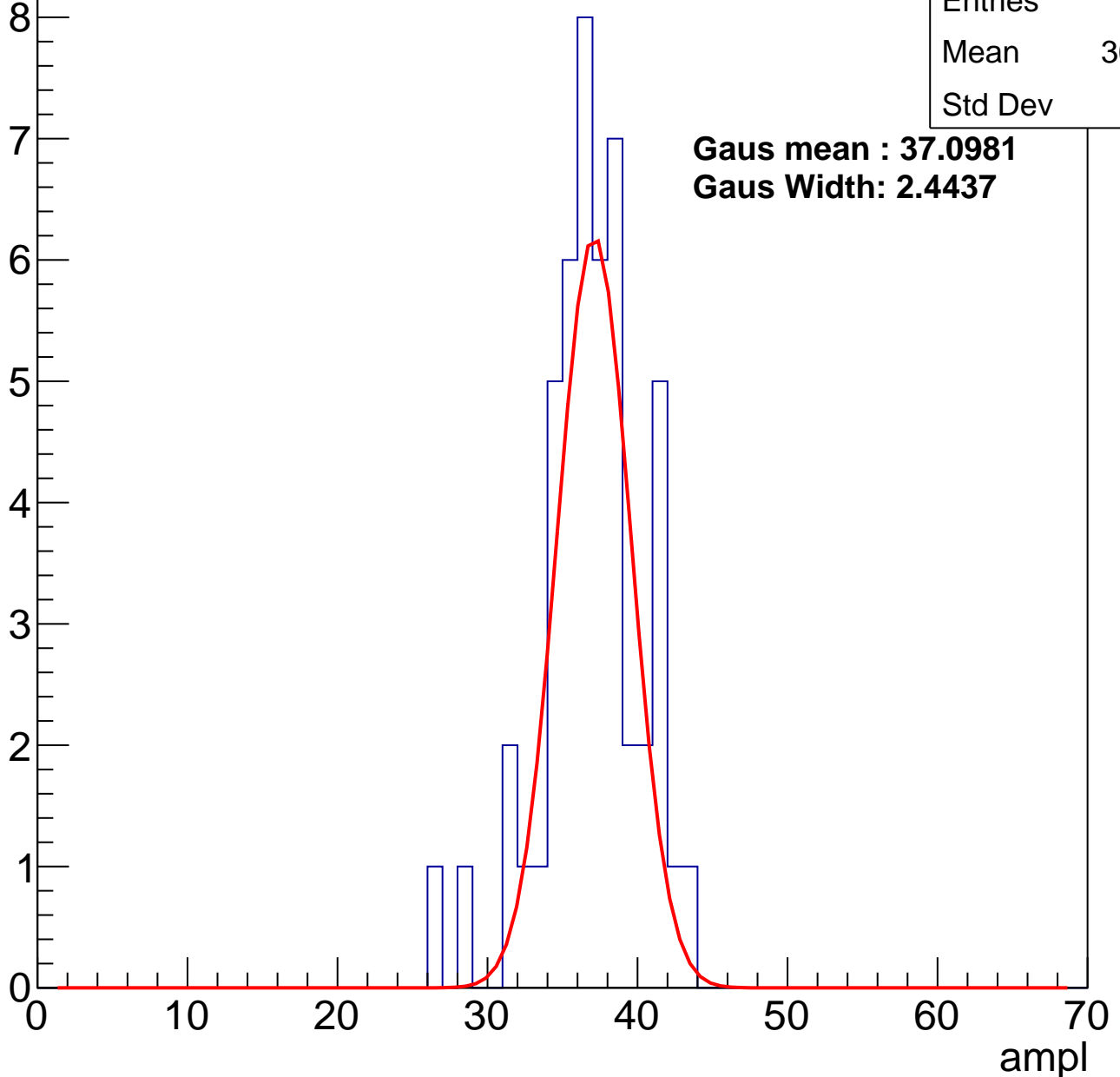
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	36.43
Std Dev	3.35

**Gaus mean : 37.0981**

**Gaus Width: 2.4437**



# B1L102S, U16-ch65, adc2

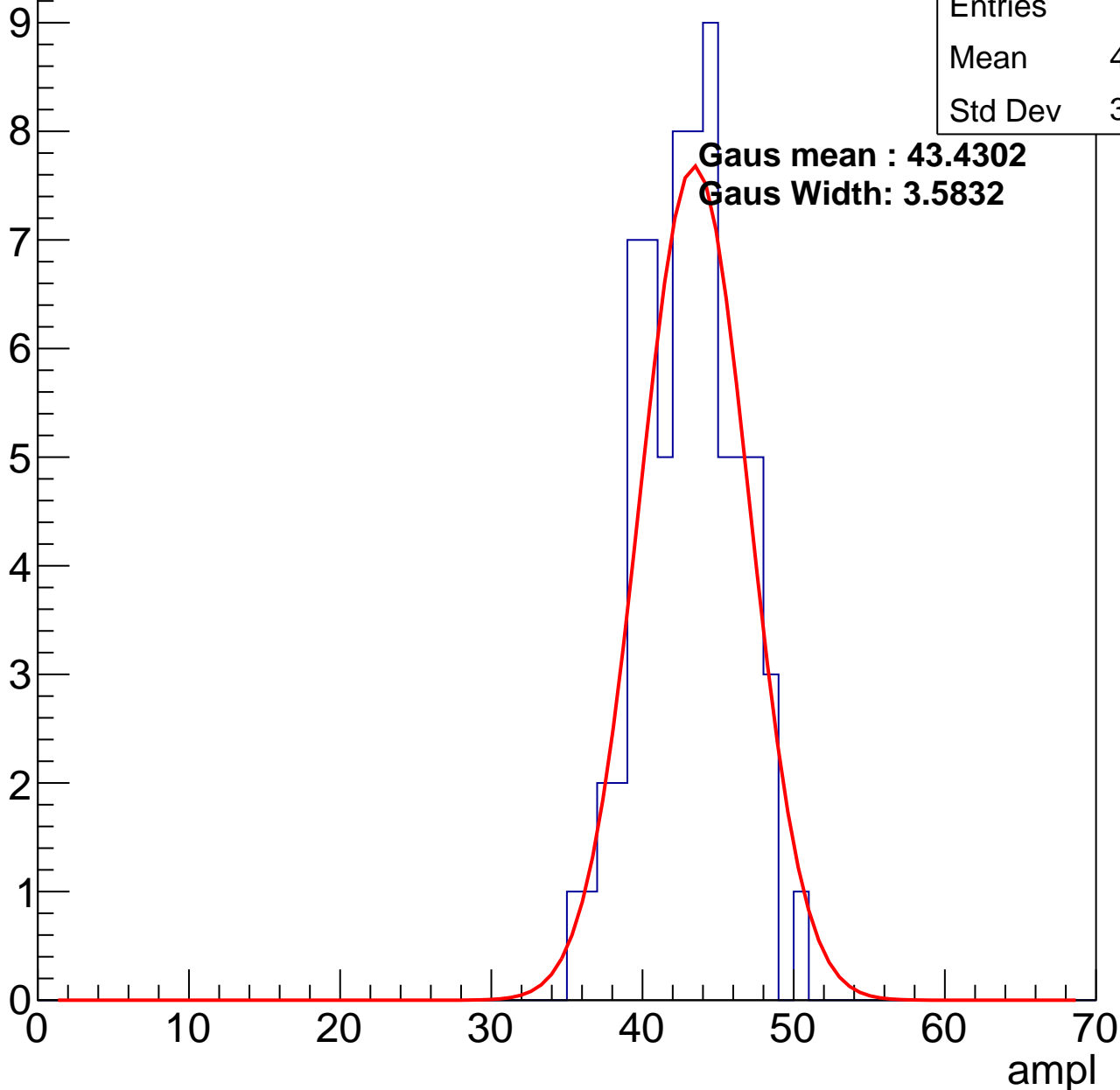
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	42.59
Std Dev	3.196

**Gaus mean : 43.4302**

**Gaus Width: 3.5832**

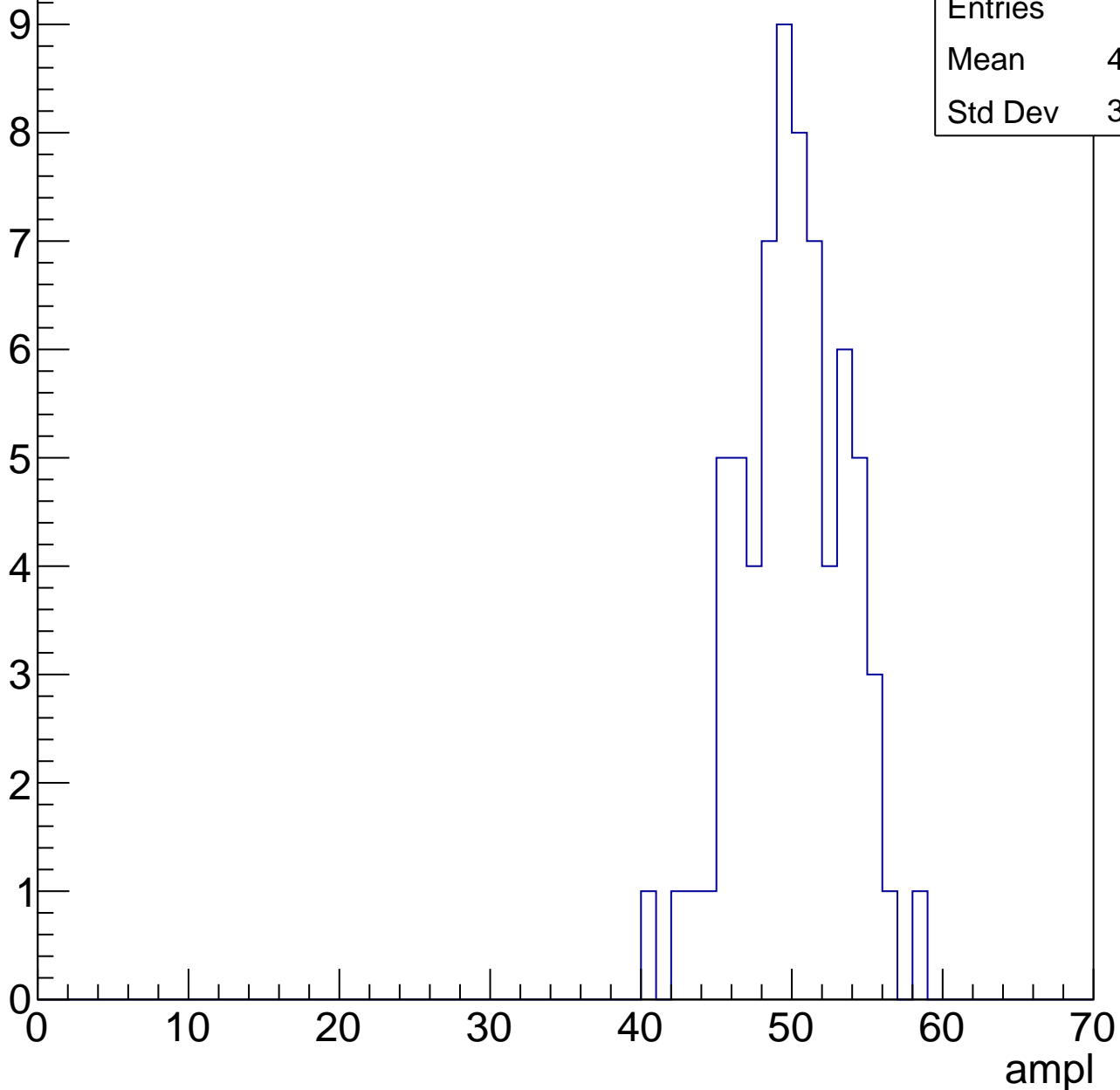


# B1L102S, U16-ch65, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

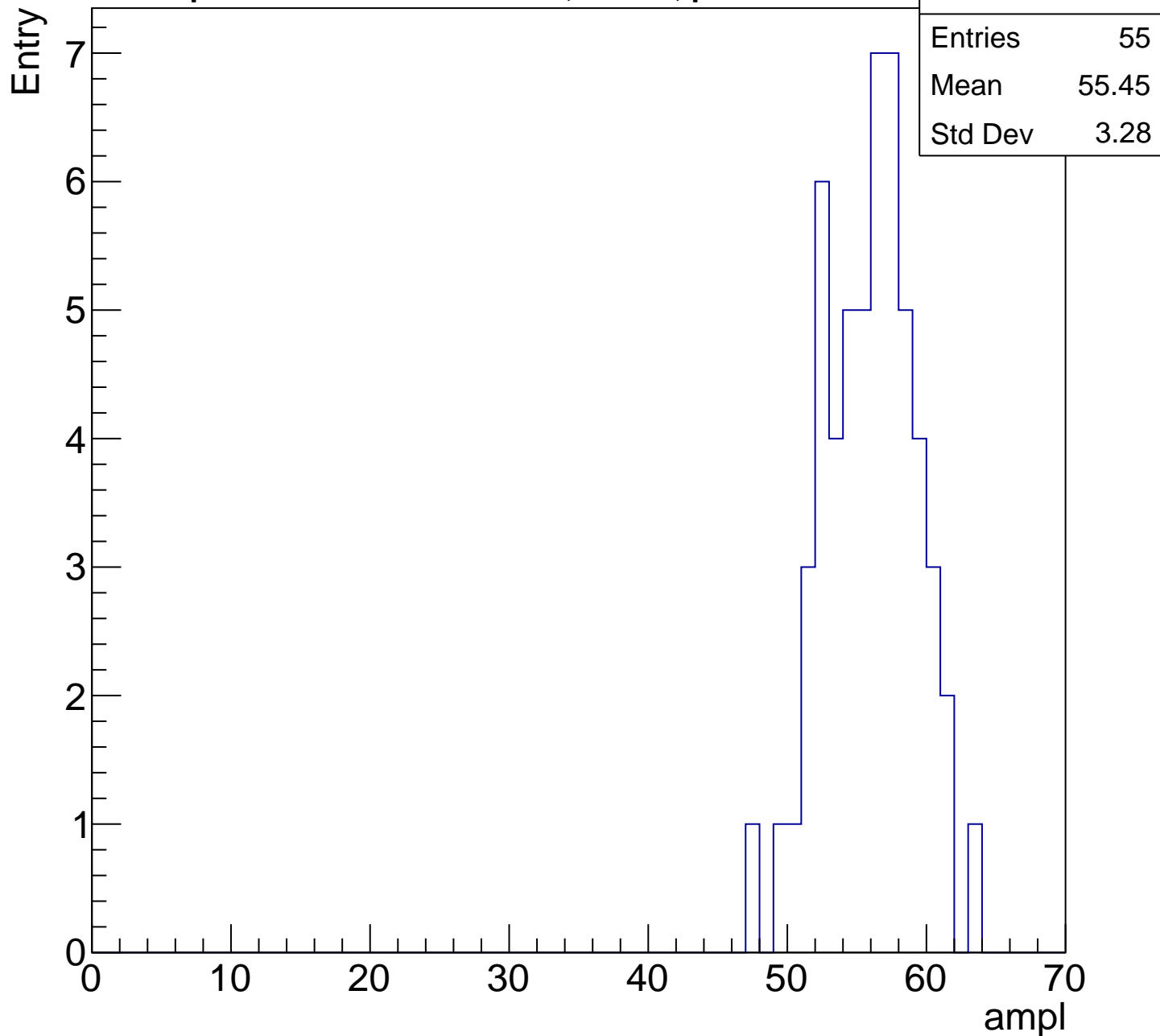
Entry

Entries	69
Mean	49.58
Std Dev	3.503



# B1L102S, U16-ch65, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

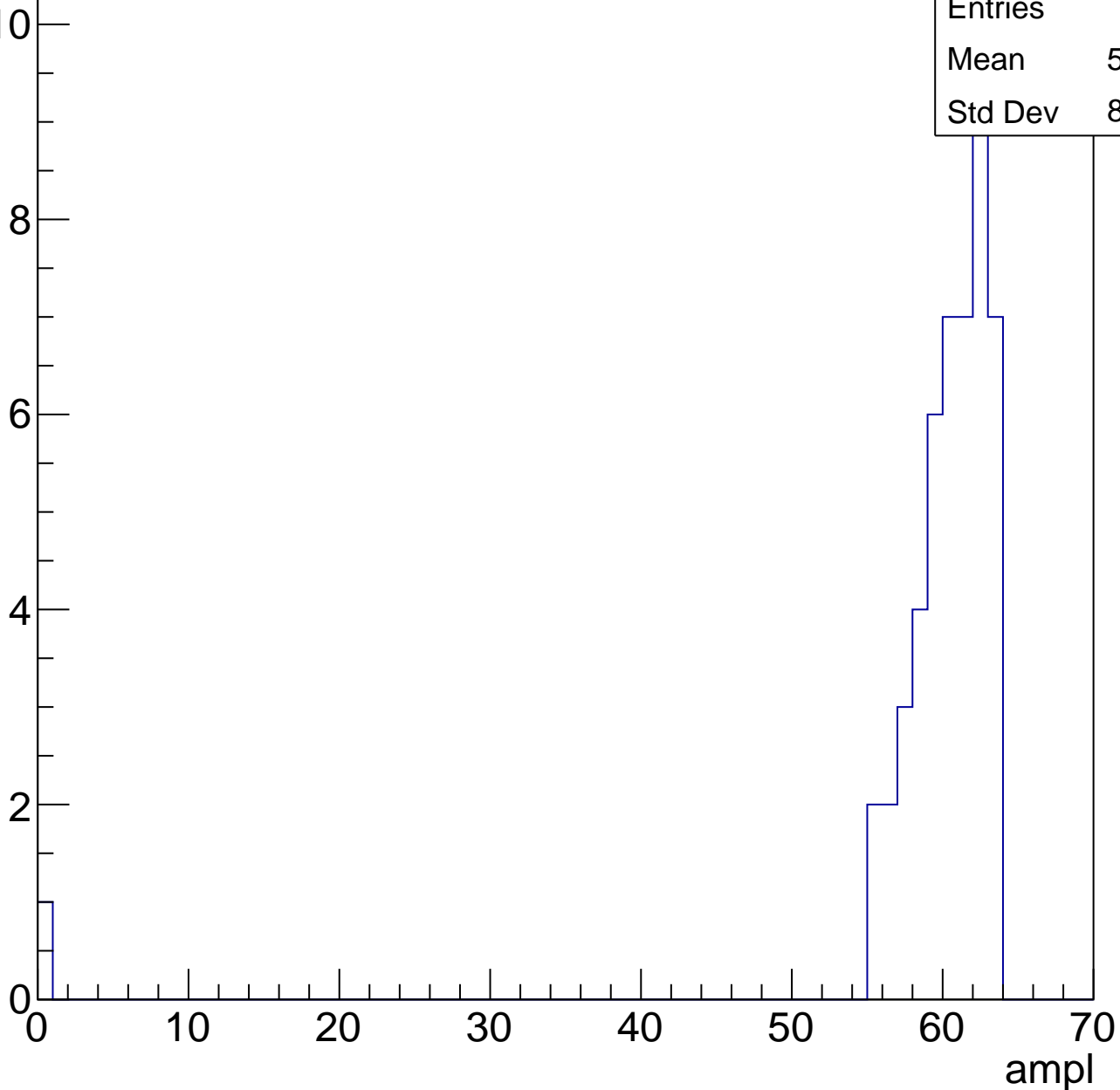


# B1L102S, U16-ch65, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	58.92
Std Dev	8.787



# B1L102S, U16-ch65, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch65, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U16-ch66, adc0

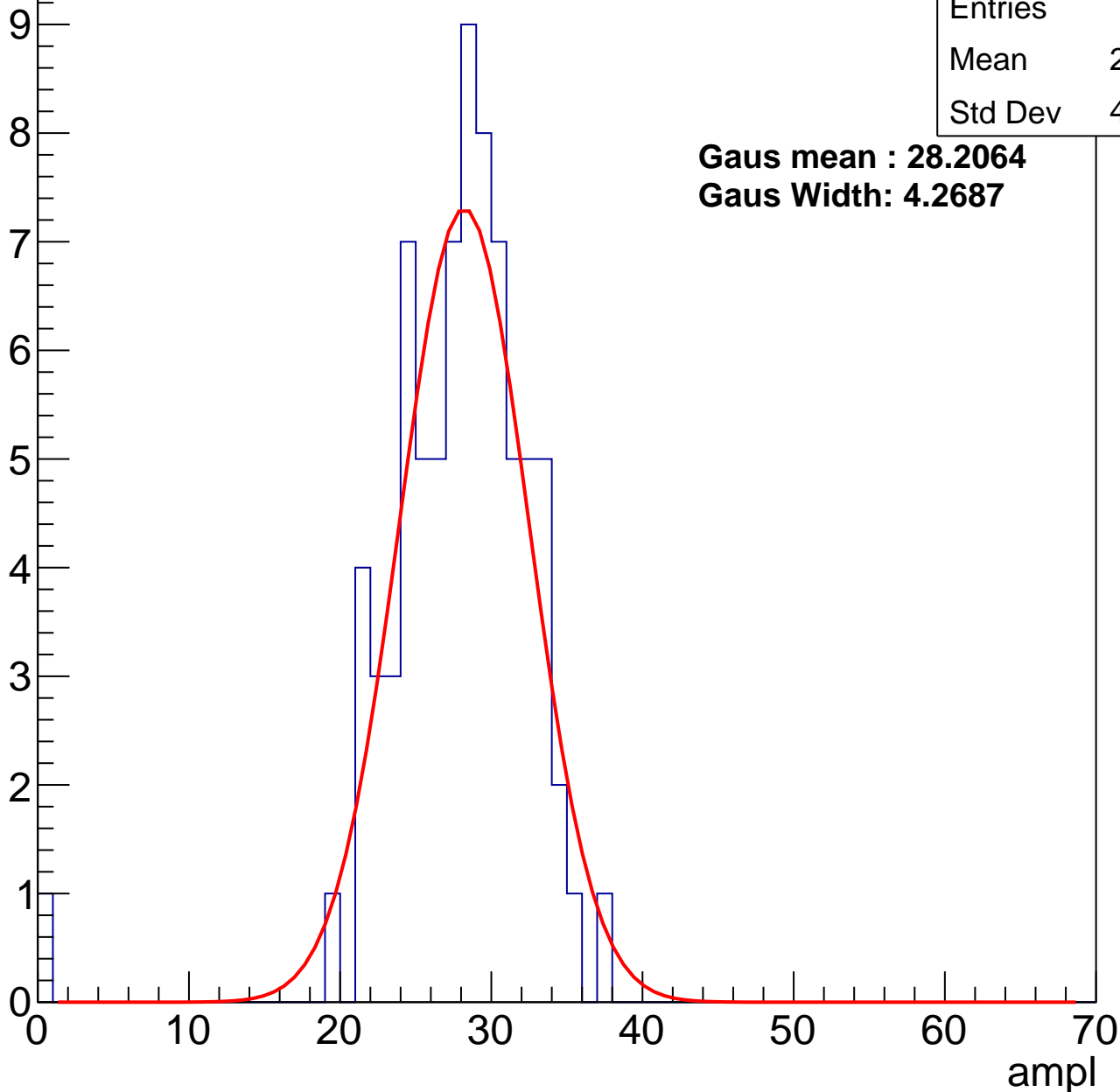
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	27.39
Std Dev	4.887

**Gaus mean : 28.2064**

**Gaus Width: 4.2687**



# B1L102S, U16-ch66, adc1

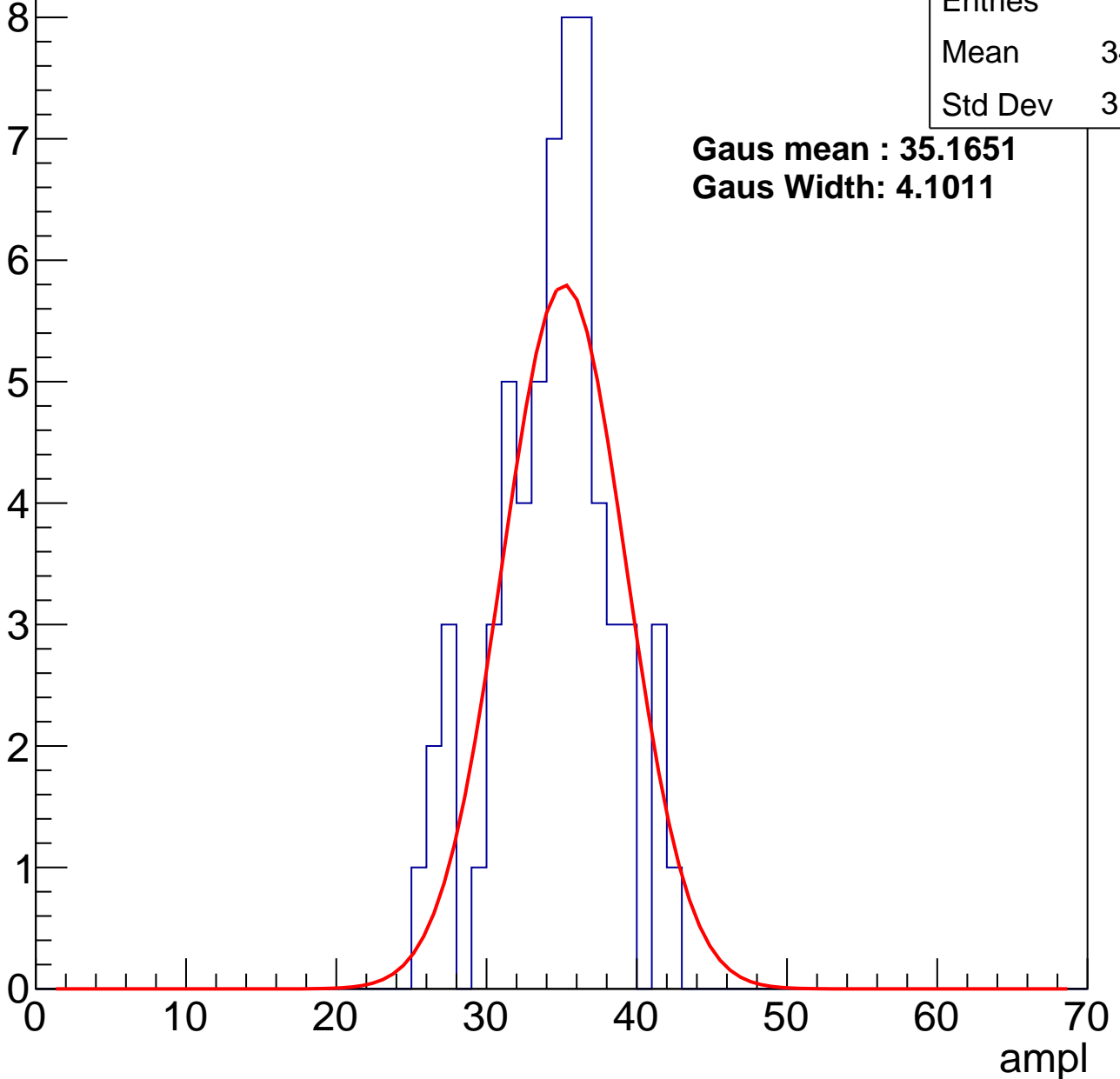
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	34.02
Std Dev	3.852

**Gaus mean : 35.1651**

**Gaus Width: 4.1011**



# B1L102S, U16-ch66, adc2

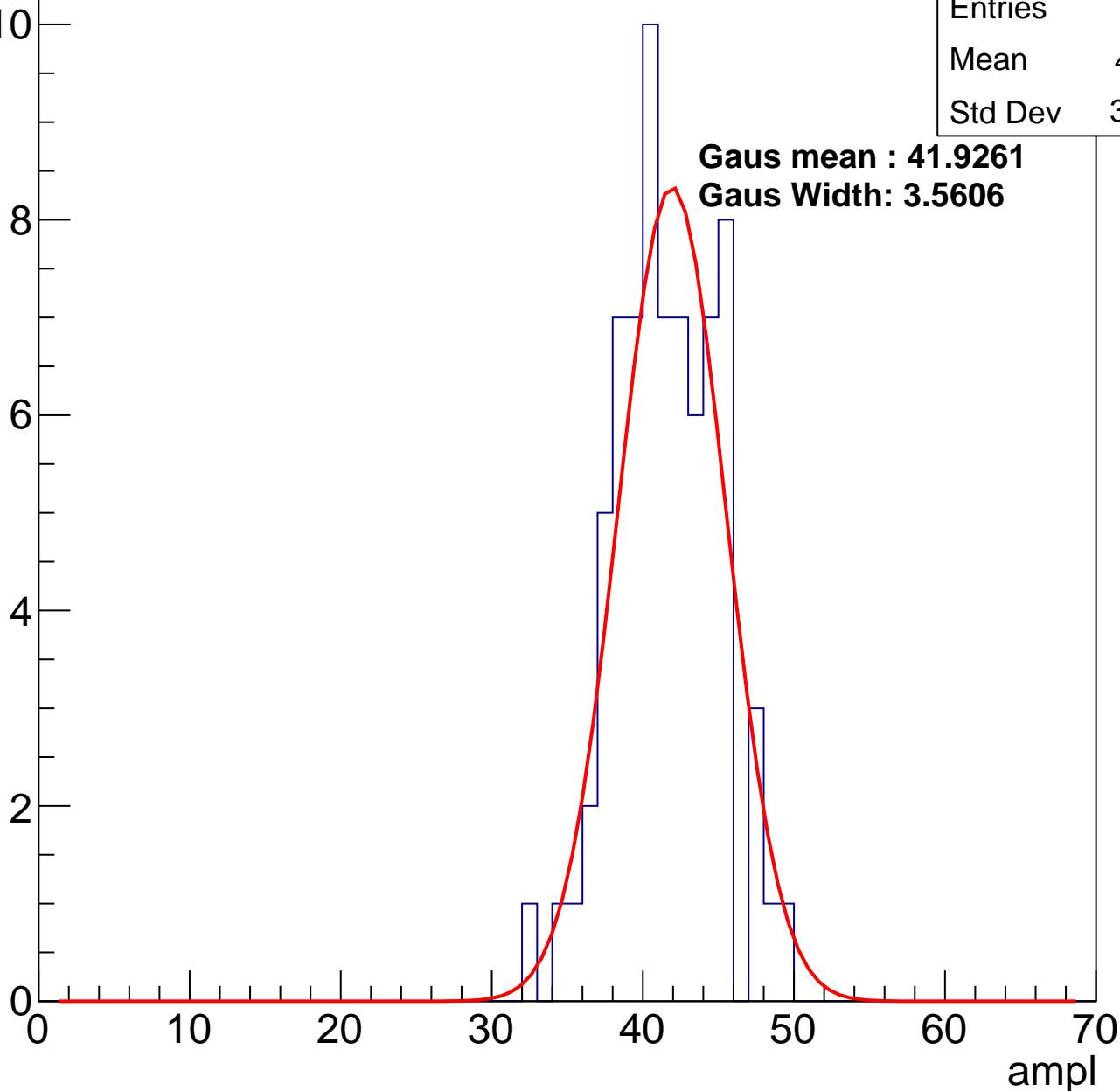
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	41.11
Std Dev	3.367

**Gaus mean : 41.9261**

**Gaus Width: 3.5606**

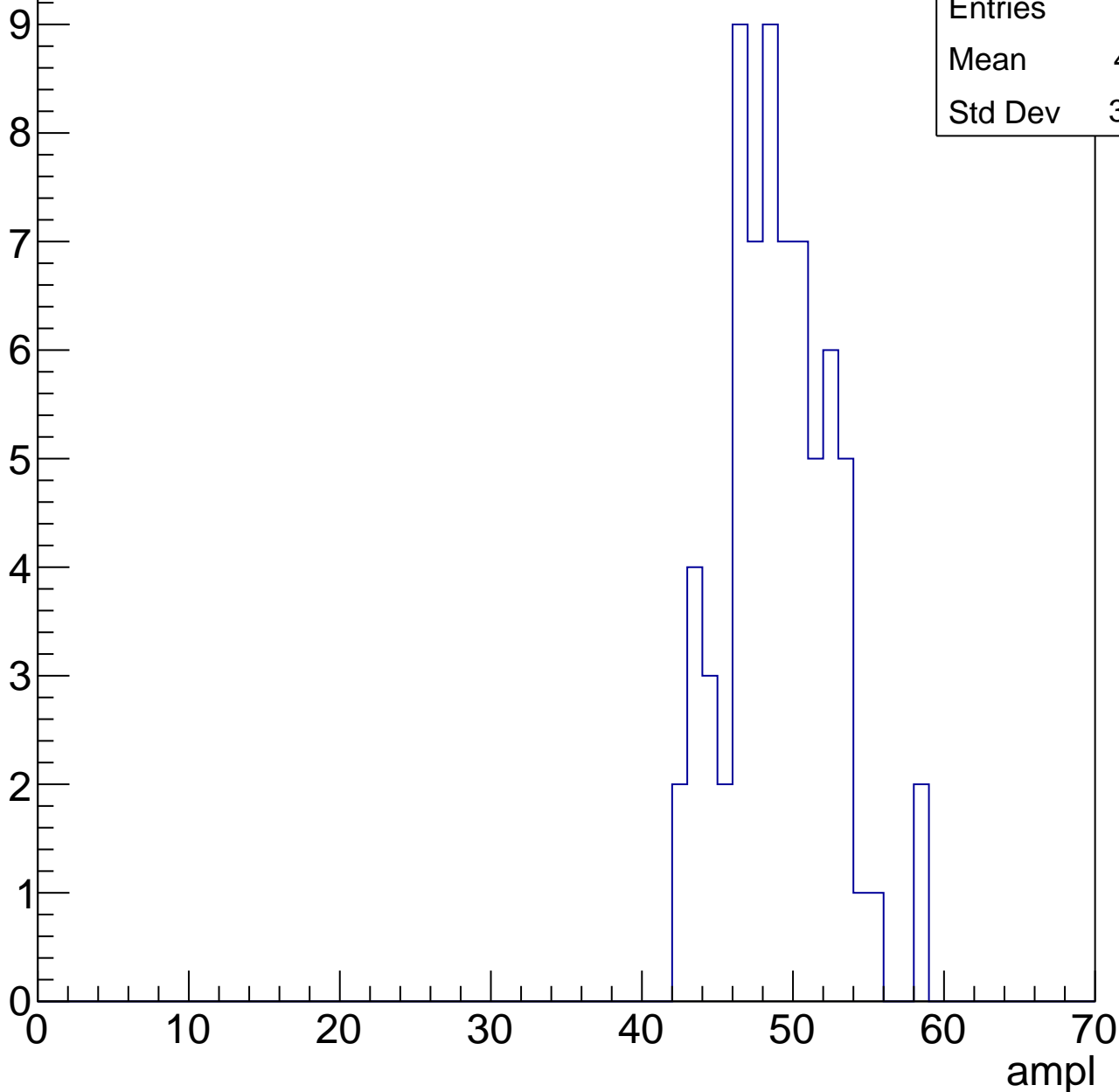


# B1L102S, U16-ch66, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	48.61
Std Dev	3.465

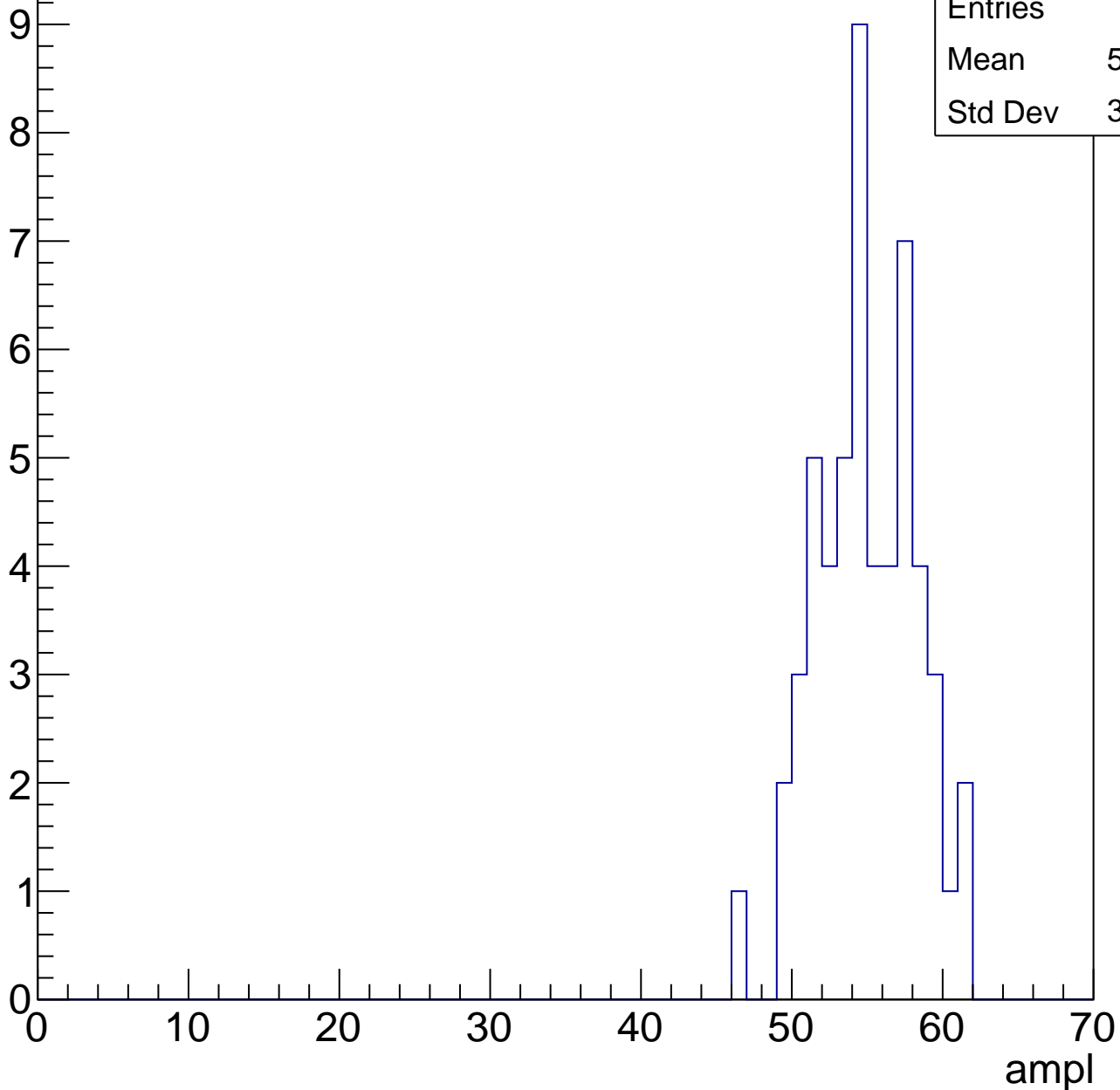


# B1L102S, U16-ch66, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	54.48
Std Dev	3.253

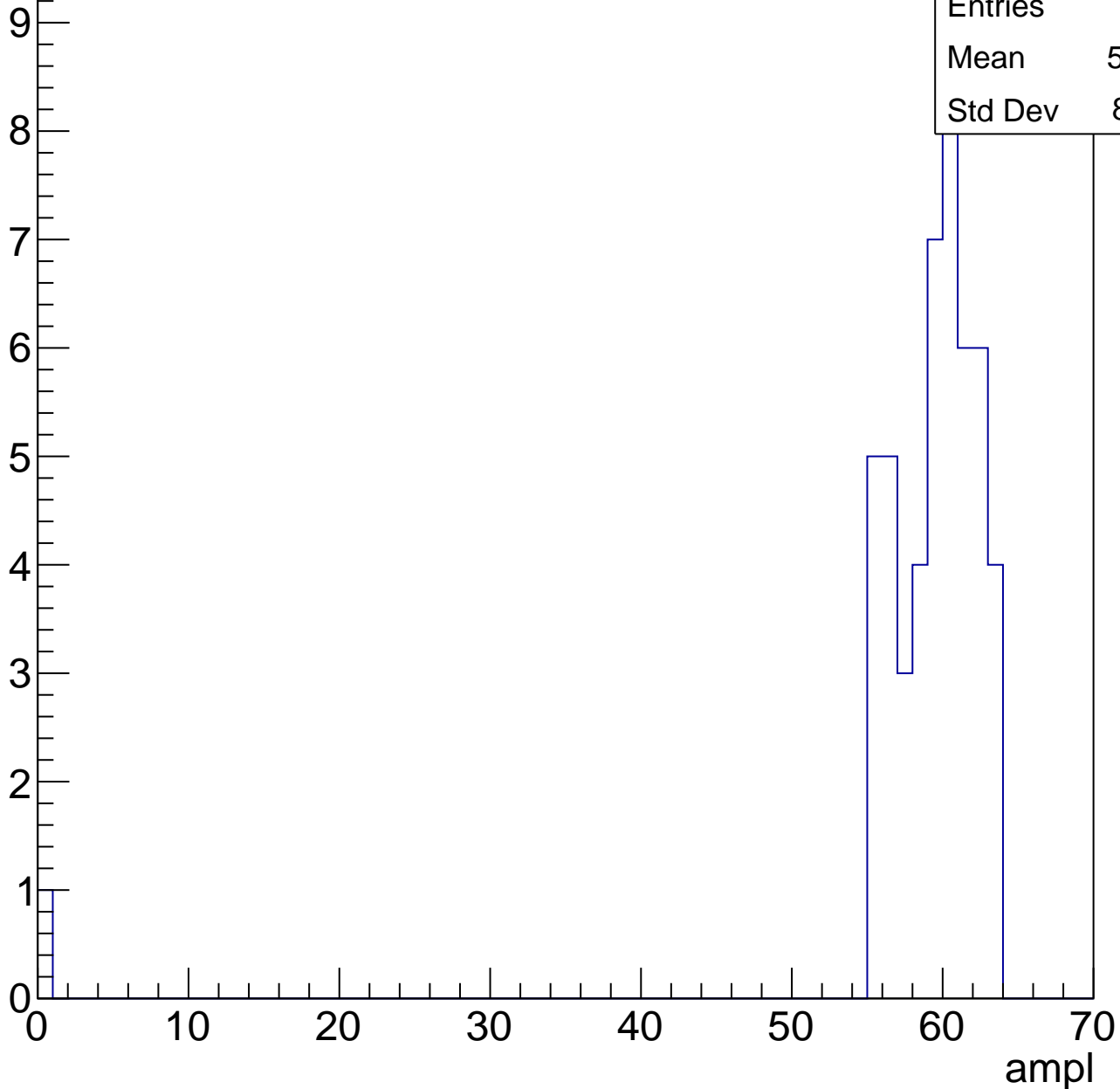


# B1L102S, U16-ch66, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

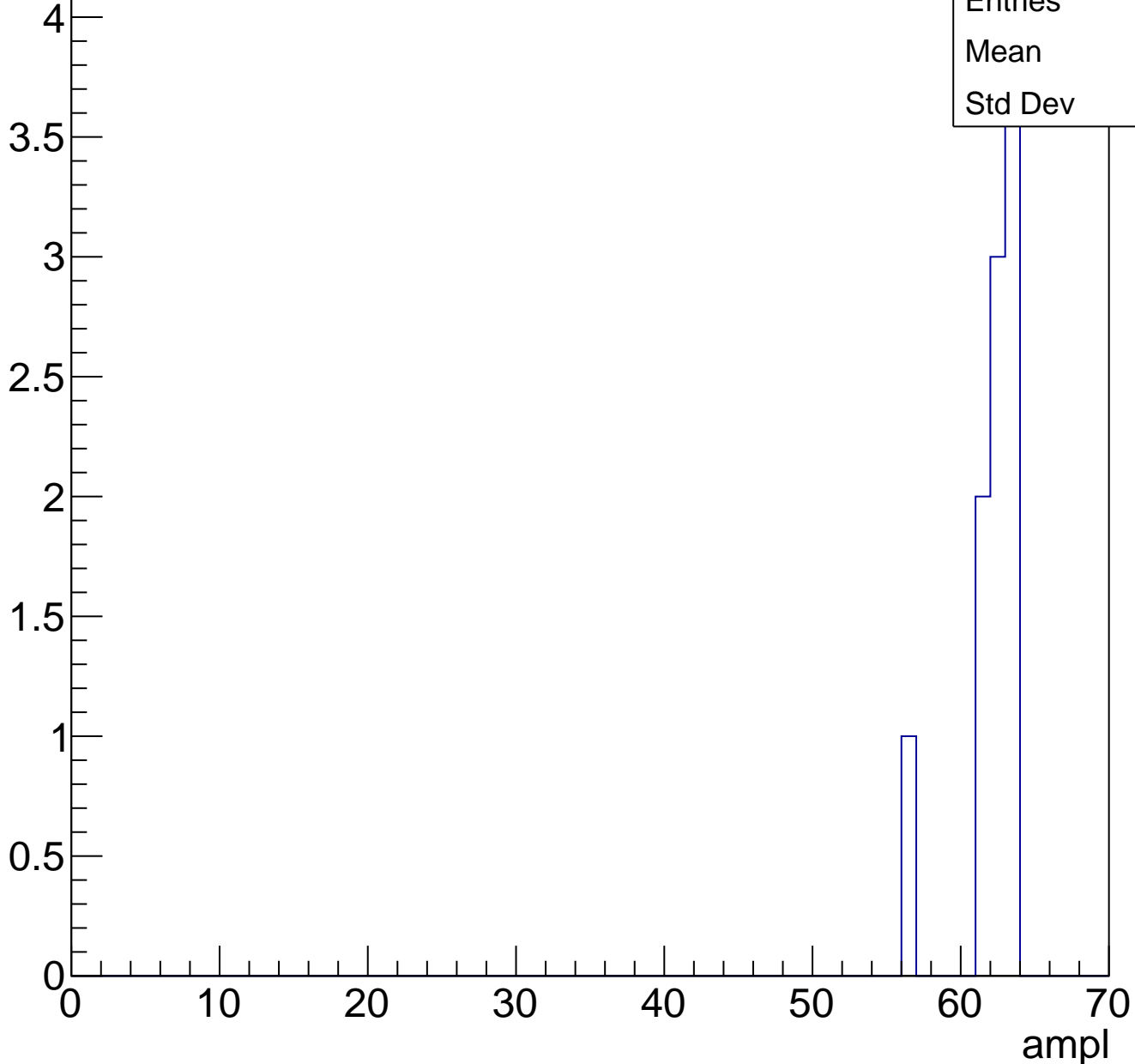
Entries	50
Mean	58.02
Std Dev	8.631



# B1L102S, U16-ch66, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



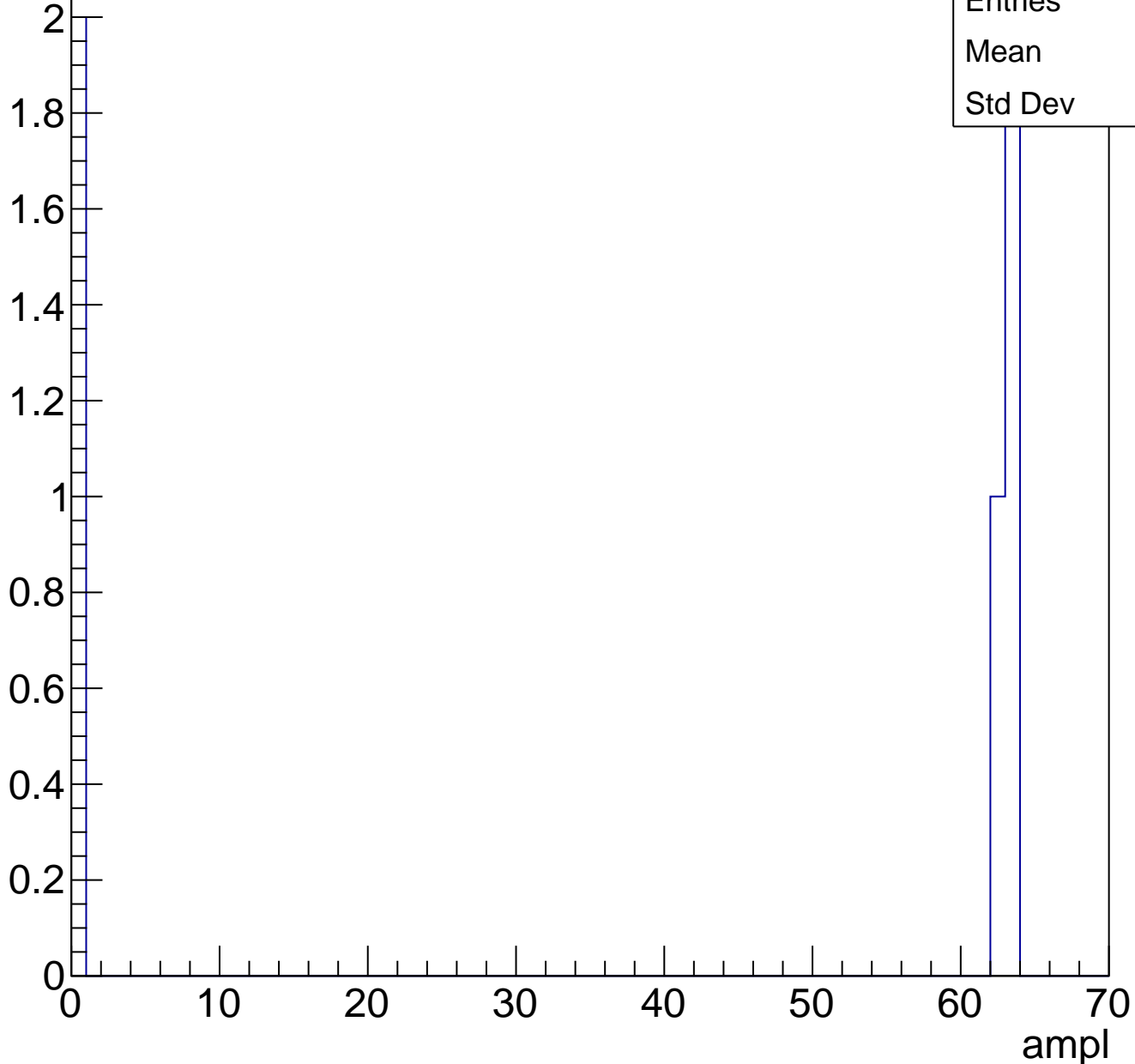
Entries	10
Mean	61.6
Std Dev	2.01



# B1L102S, U16-ch66, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch67, adc0

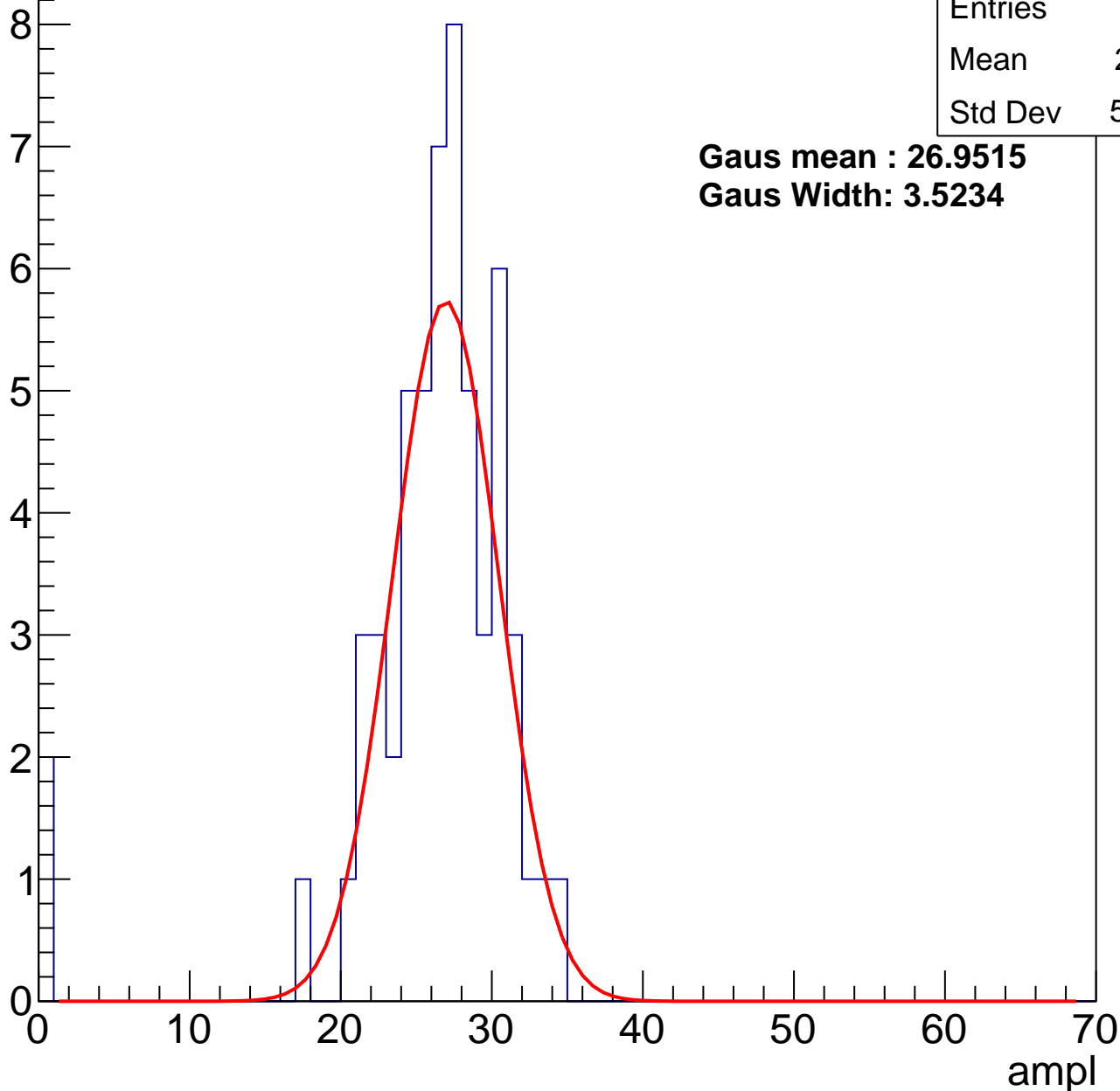
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	25.51
Std Dev	5.918

**Gaus mean : 26.9515**

**Gaus Width: 3.5234**



# B1L102S, U16-ch67, adc1

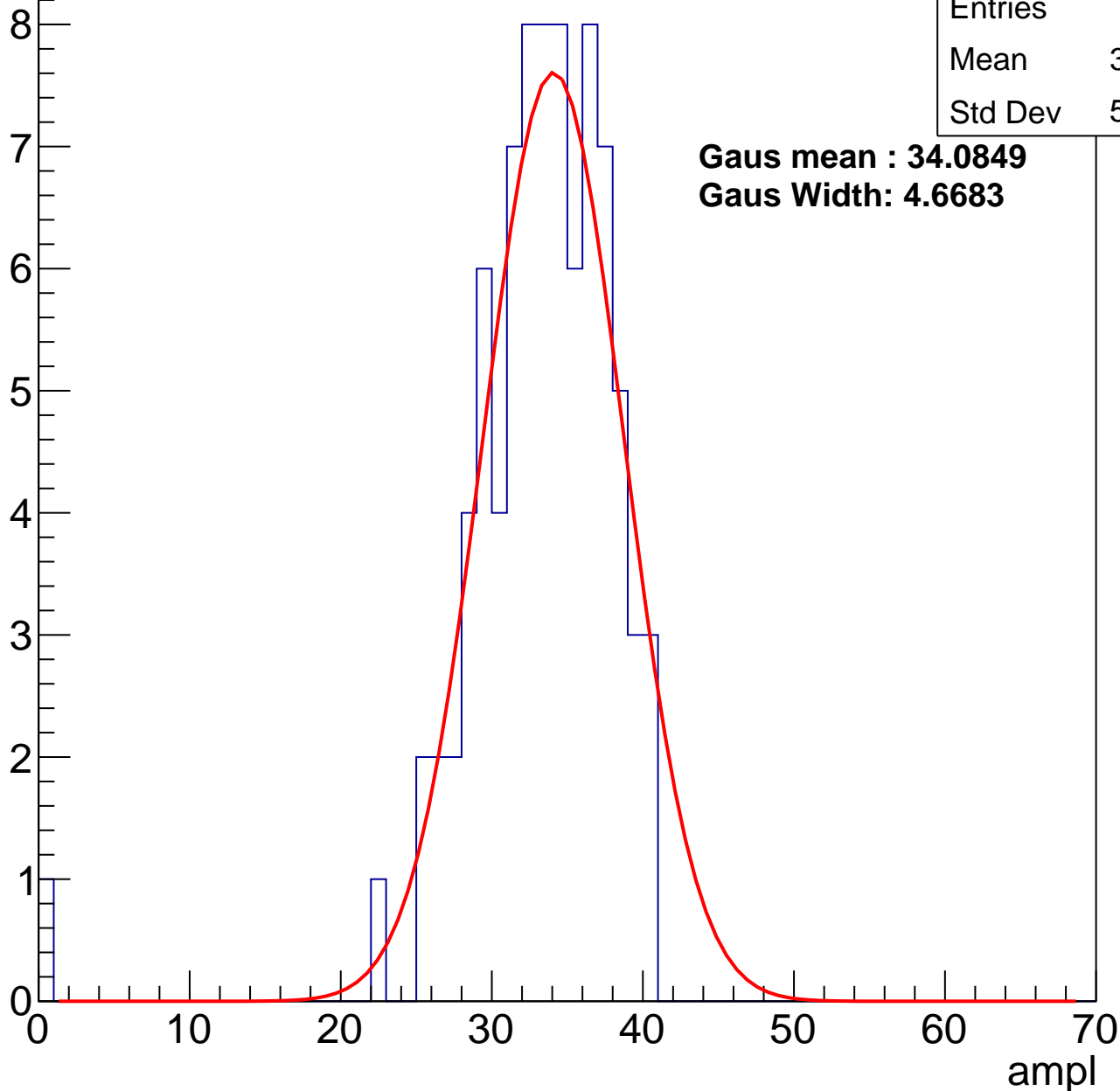
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	85
Mean	32.67
Std Dev	5.272

**Gaus mean : 34.0849**

**Gaus Width: 4.6683**



# B1L102S, U16-ch67, adc2

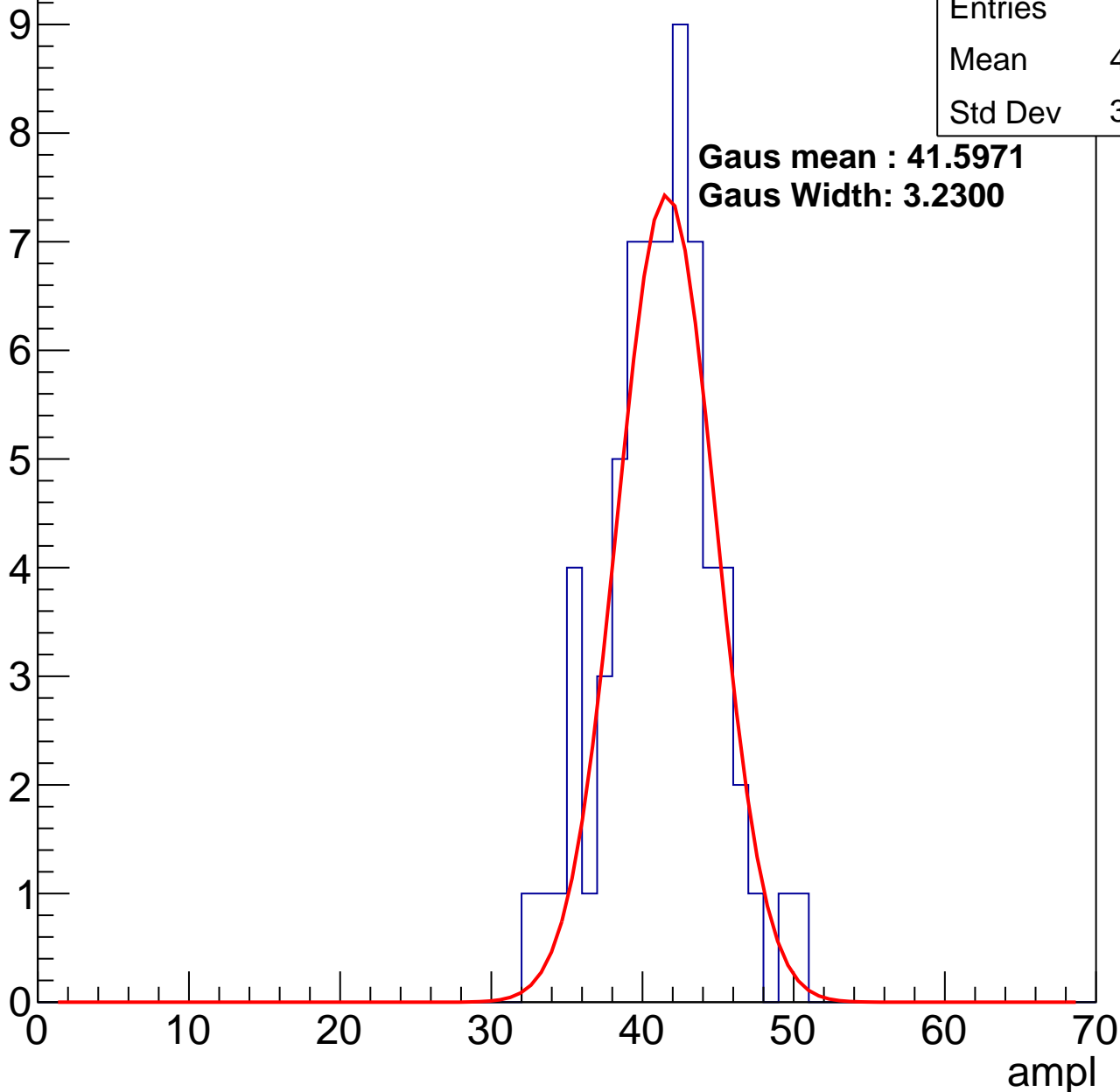
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	40.74
Std Dev	3.598

**Gaus mean : 41.5971**

**Gaus Width: 3.2300**

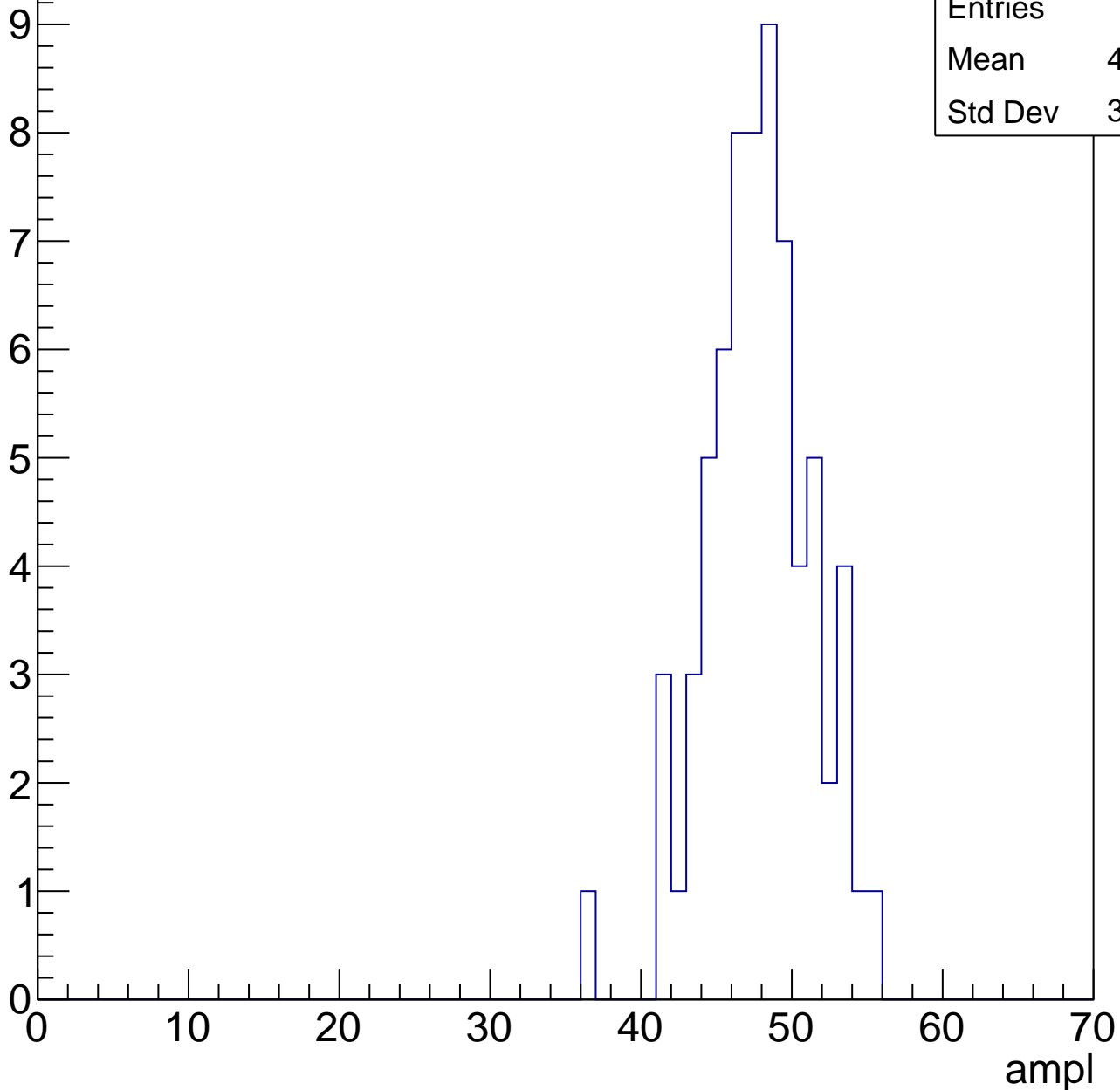


# B1L102S, U16-ch67, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

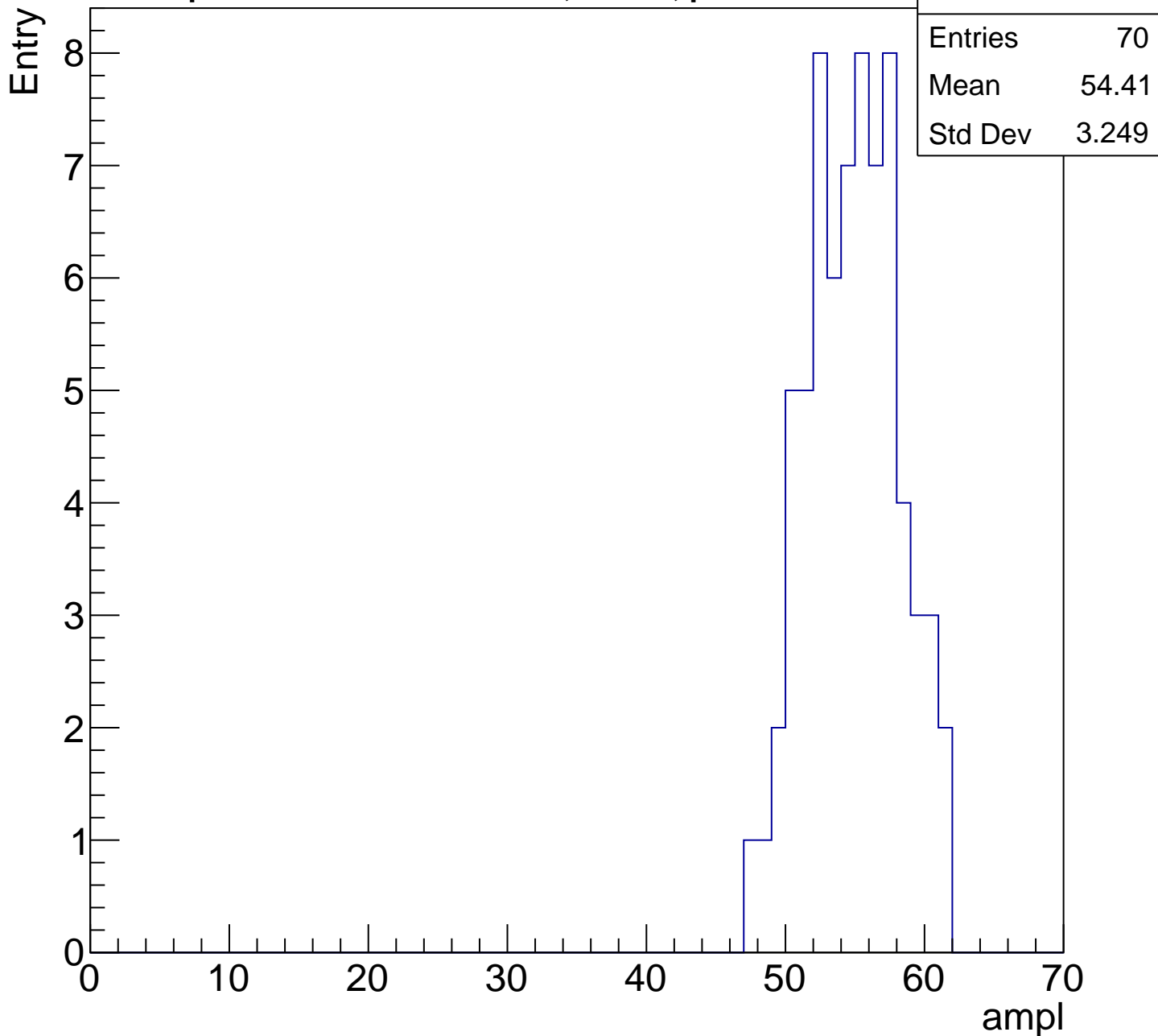
Entry

Entries	68
Mean	47.34
Std Dev	3.496



# B1L102S, U16-ch67, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

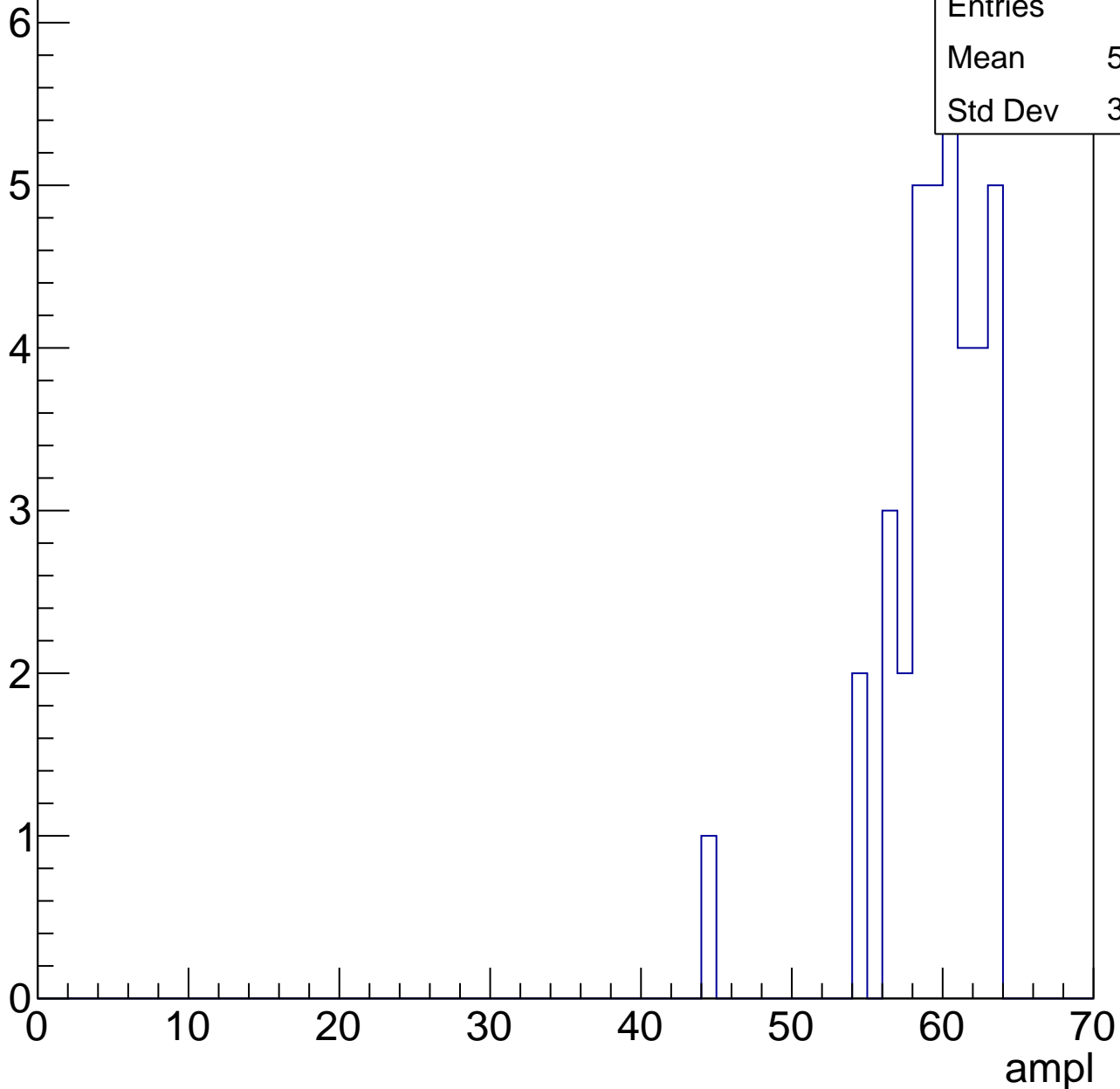


# B1L102S, U16-ch67, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	37
Mean	59.08
Std Dev	3.498

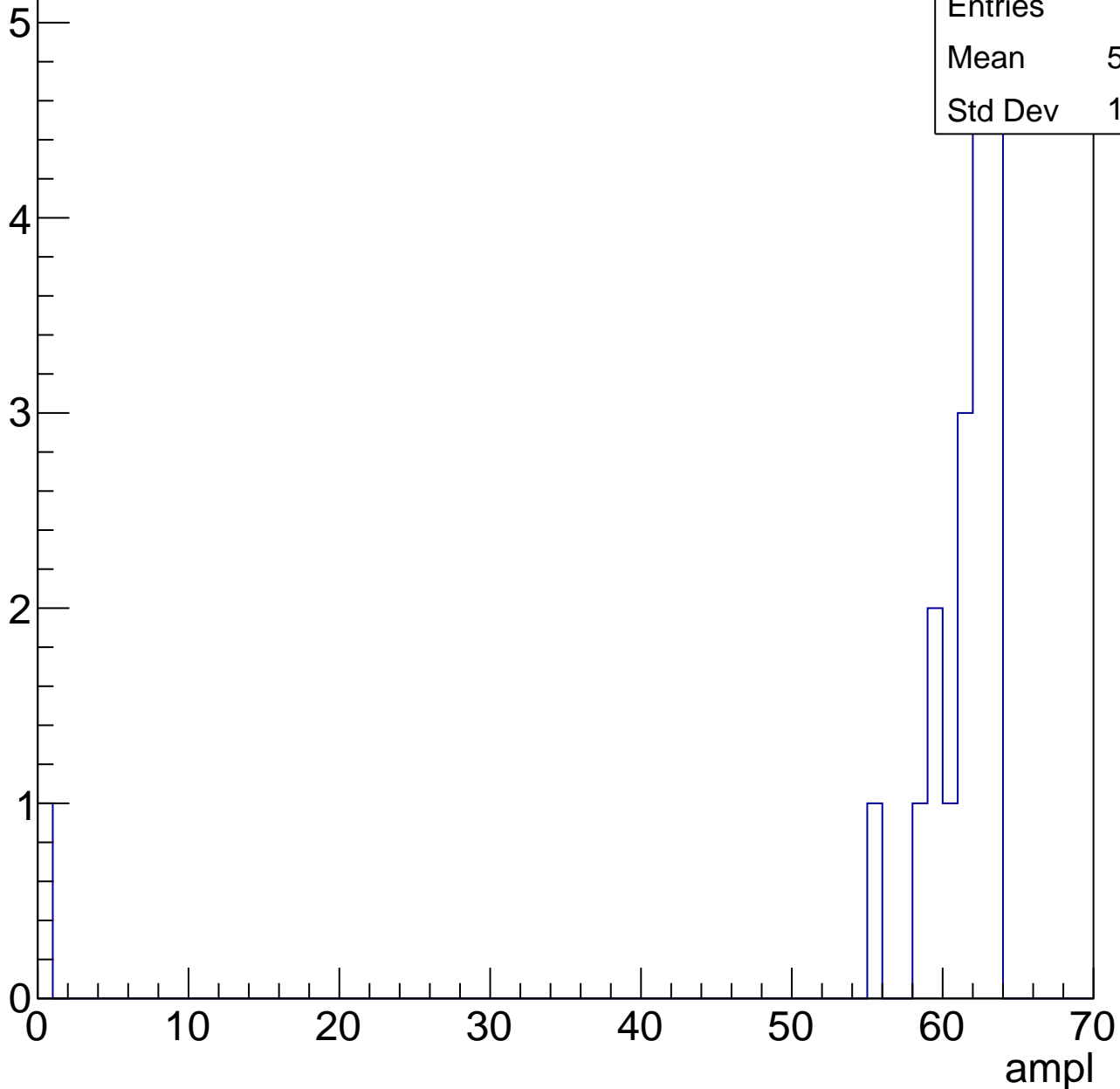


# B1L102S, U16-ch67, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	19
Mean	57.84
Std Dev	13.79

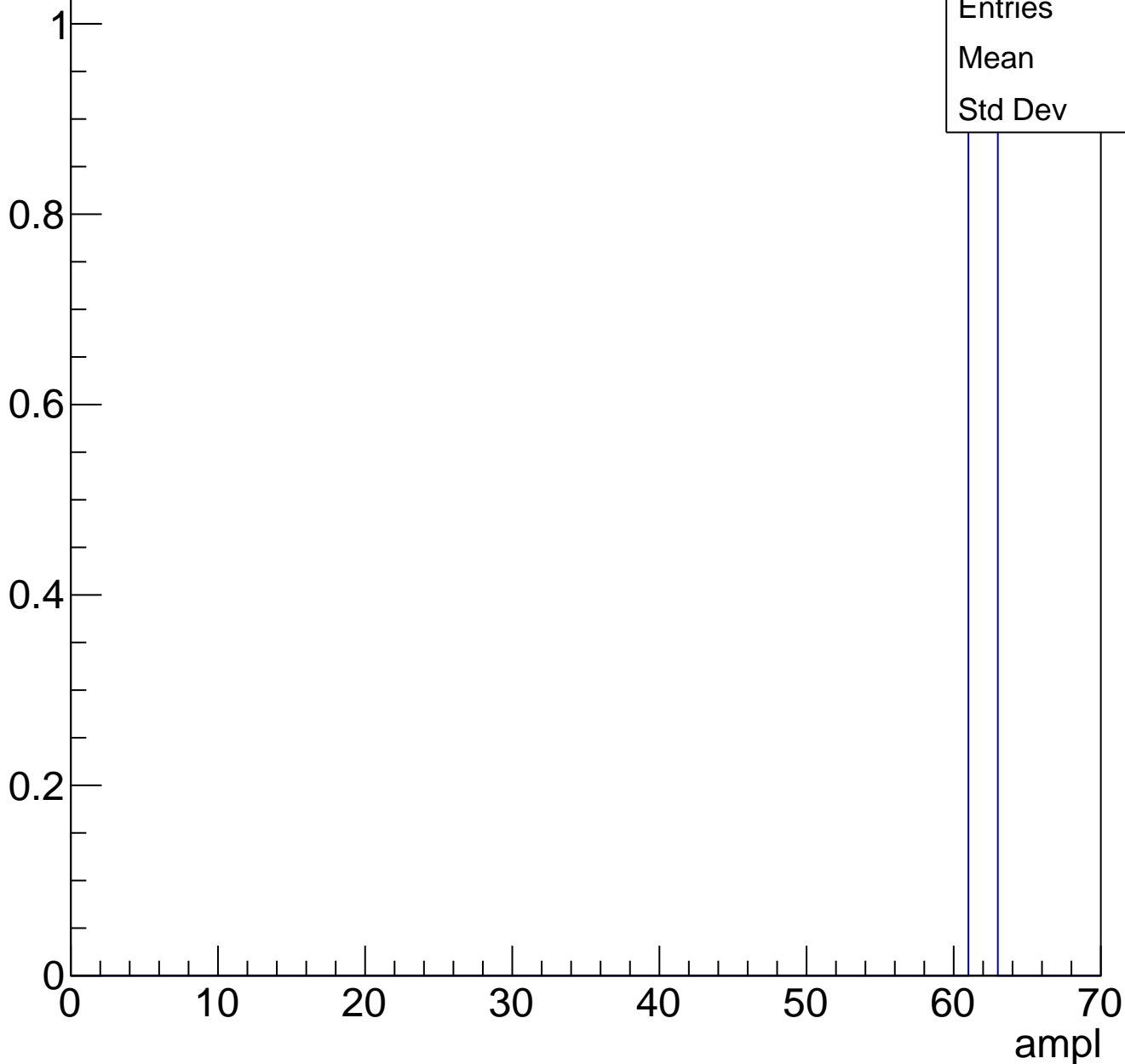




# B1L102S, U16-ch67, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch68, adc0

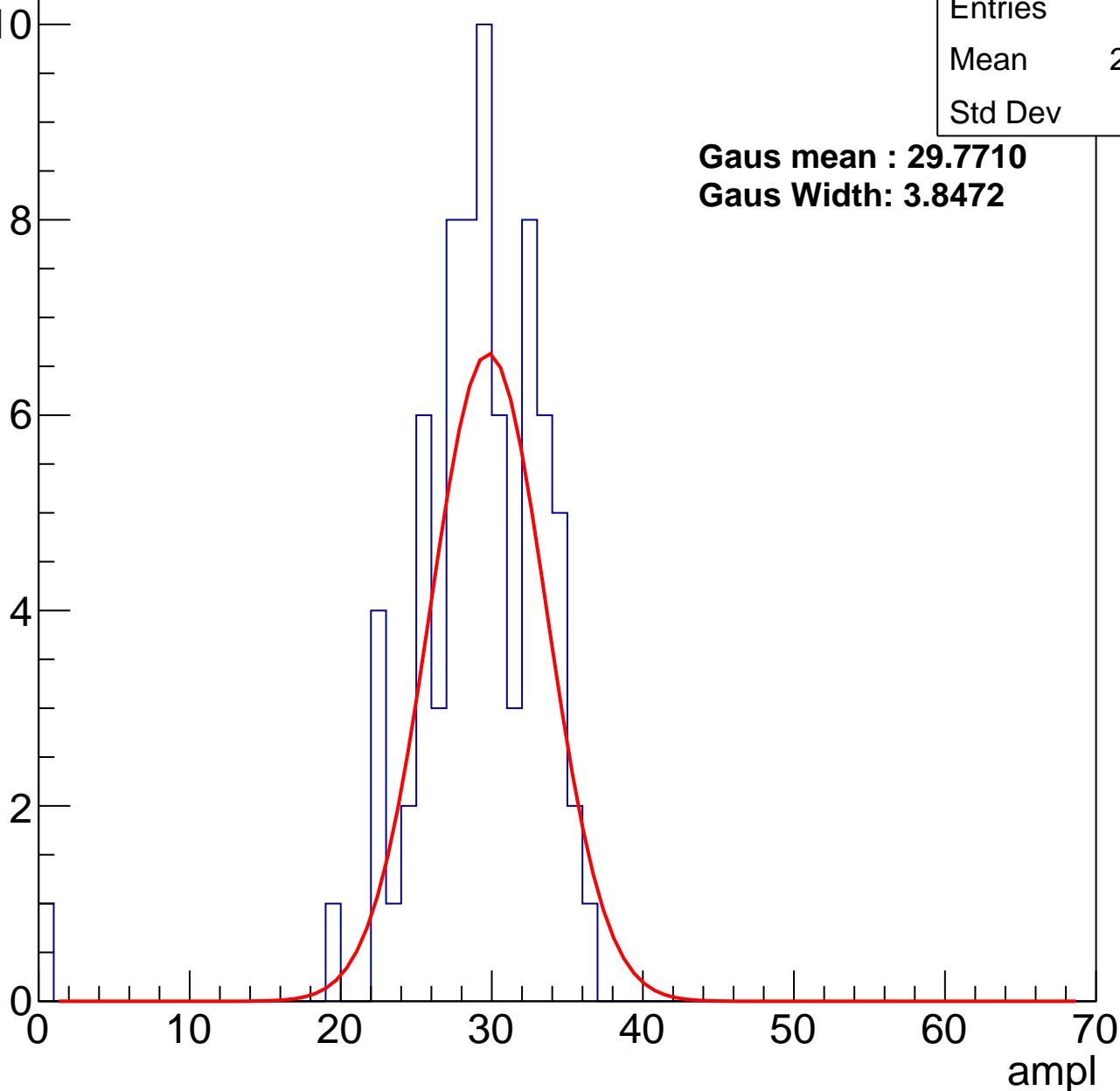
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	28.52
Std Dev	4.9

**Gaus mean : 29.7710**

**Gaus Width: 3.8472**



# B1L102S, U16-ch68, adc1

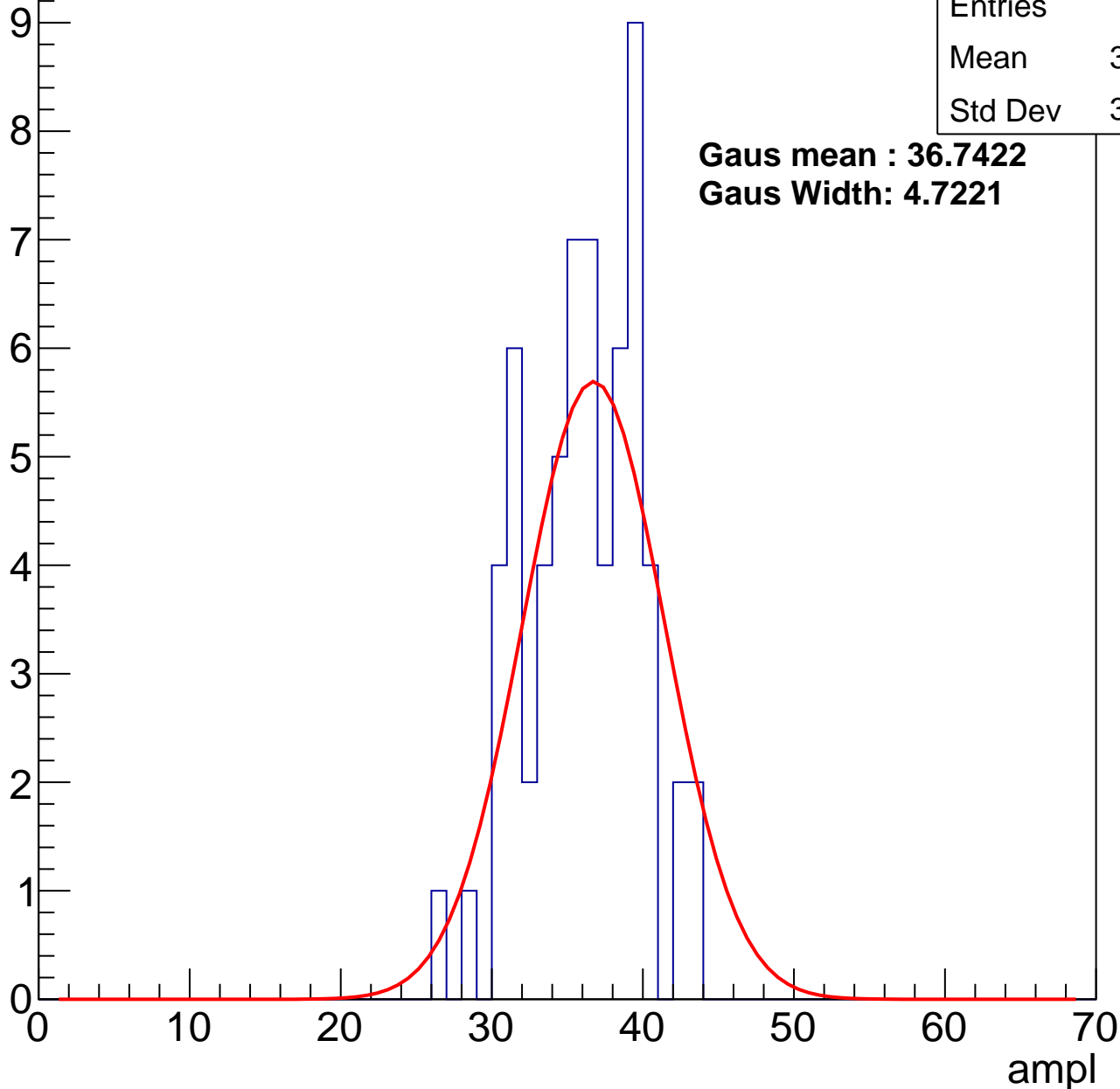
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	35.62
Std Dev	3.723

**Gaus mean : 36.7422**

**Gaus Width: 4.7221**



# B1L102S, U16-ch68, adc2

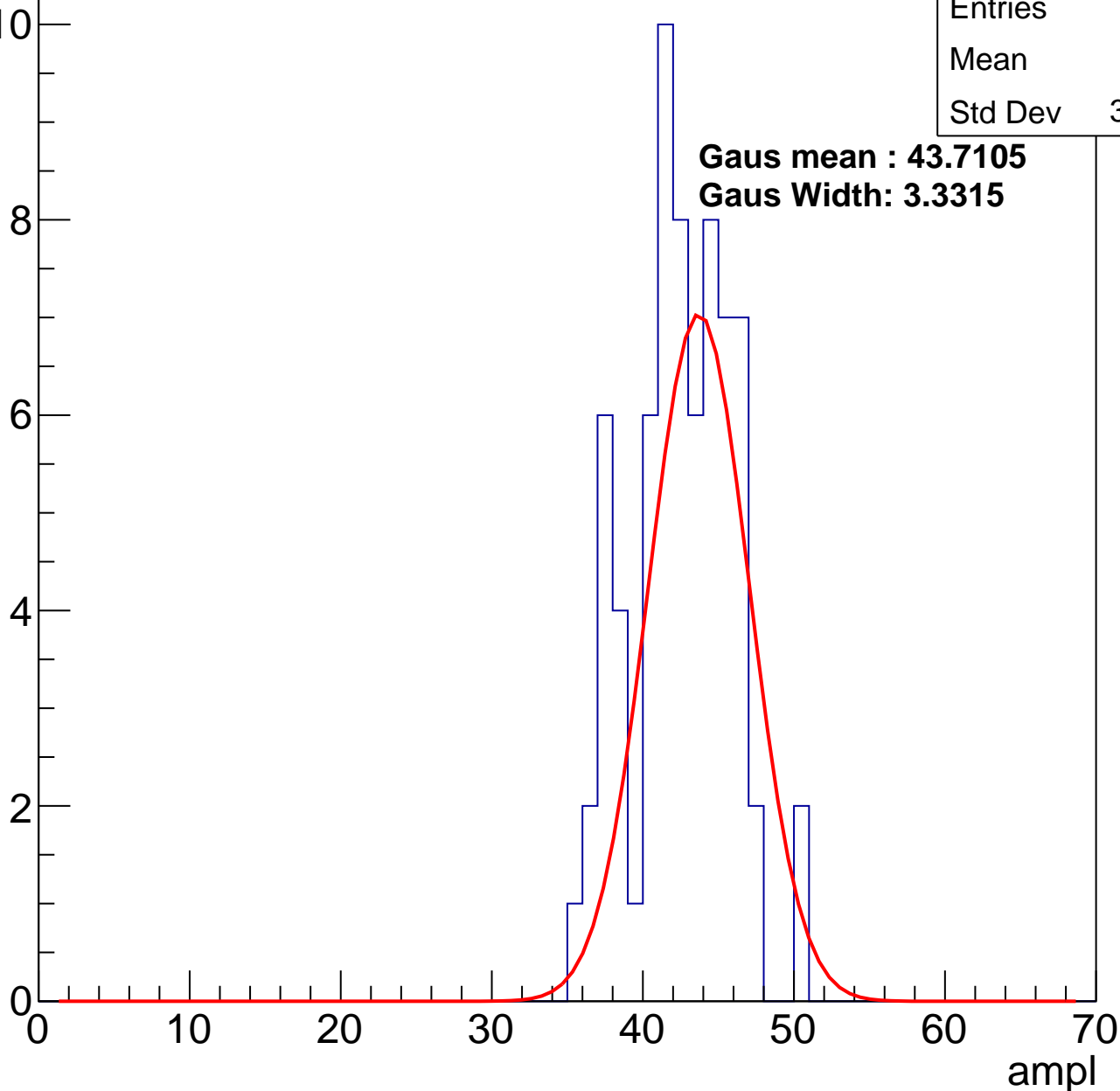
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	42.1
Std Dev	3.313

**Gaus mean : 43.7105**

**Gaus Width: 3.3315**

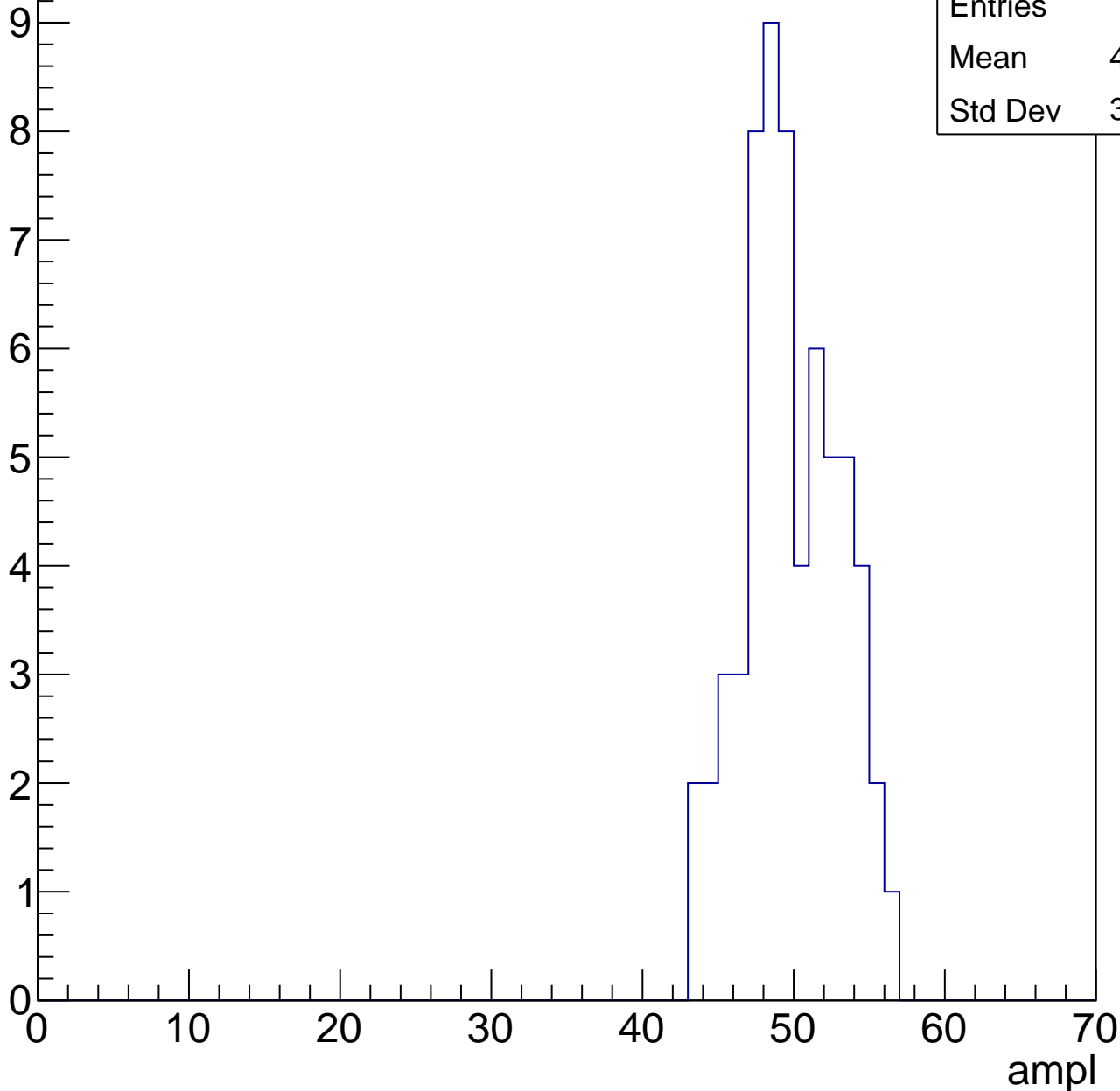


# B1L102S, U16-ch68, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	49.35
Std Dev	3.122

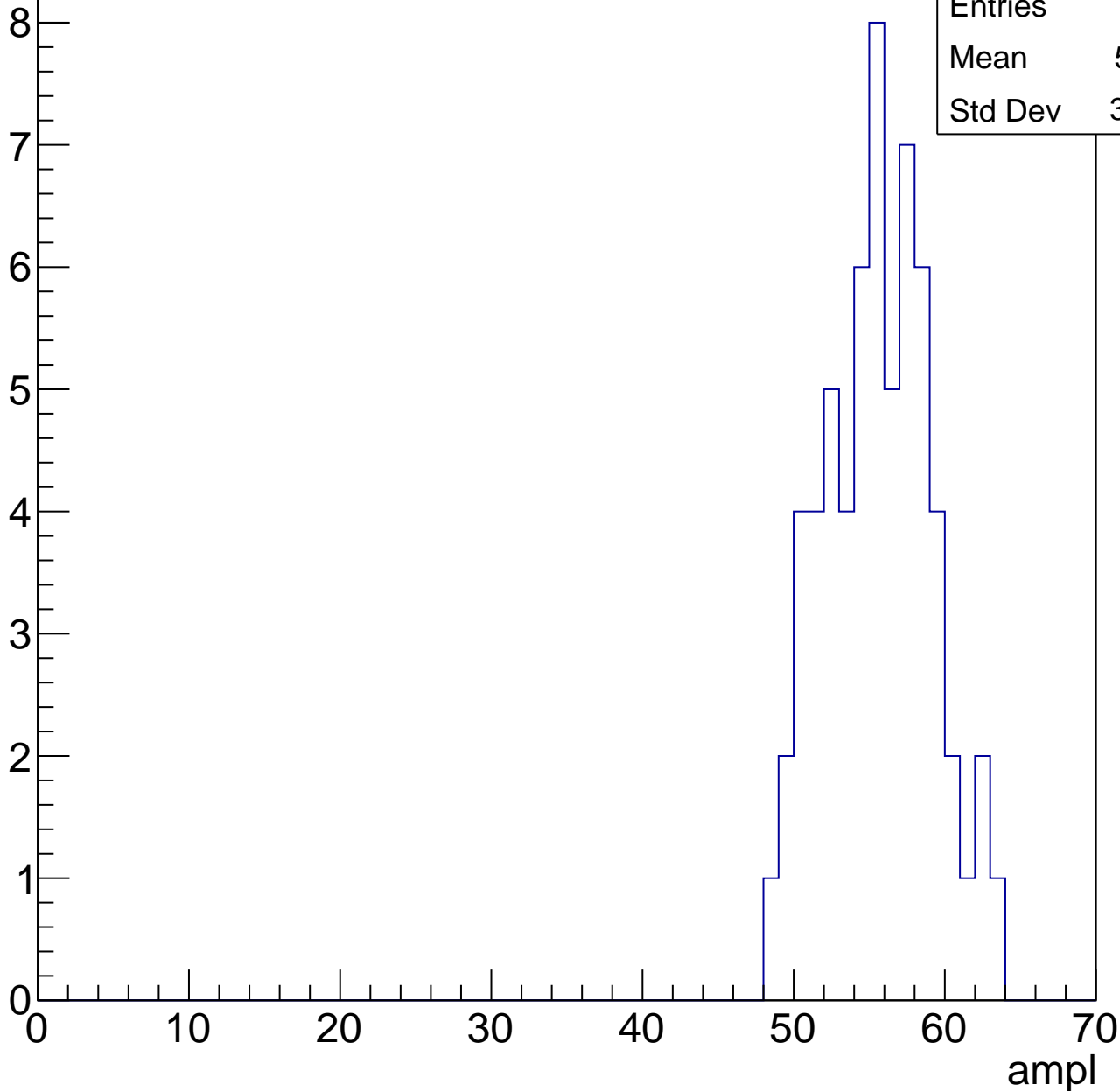


# B1L102S, U16-ch68, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	55.11
Std Dev	3.479

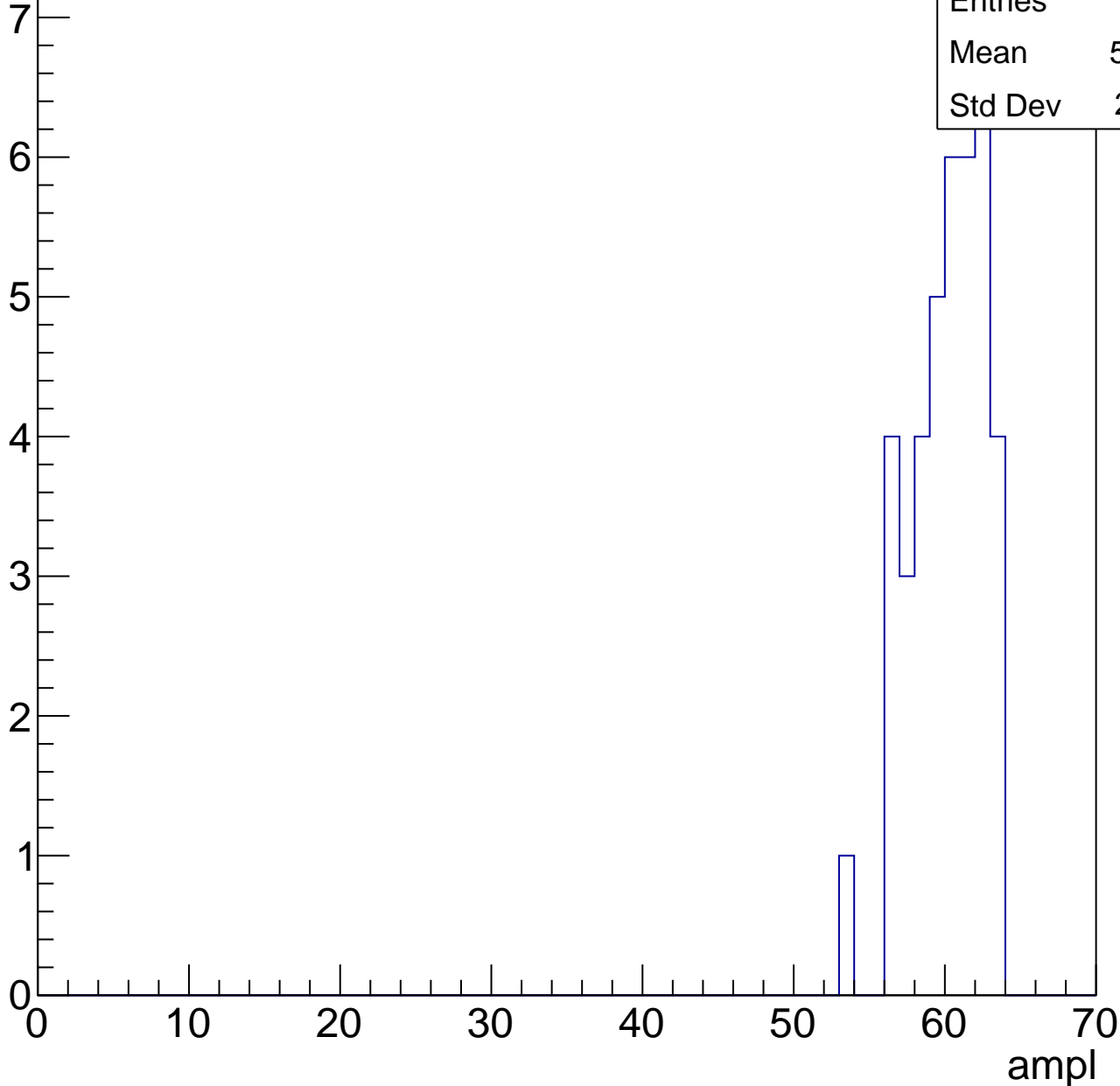


# B1L102S, U16-ch68, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	59.67
Std Dev	2.381

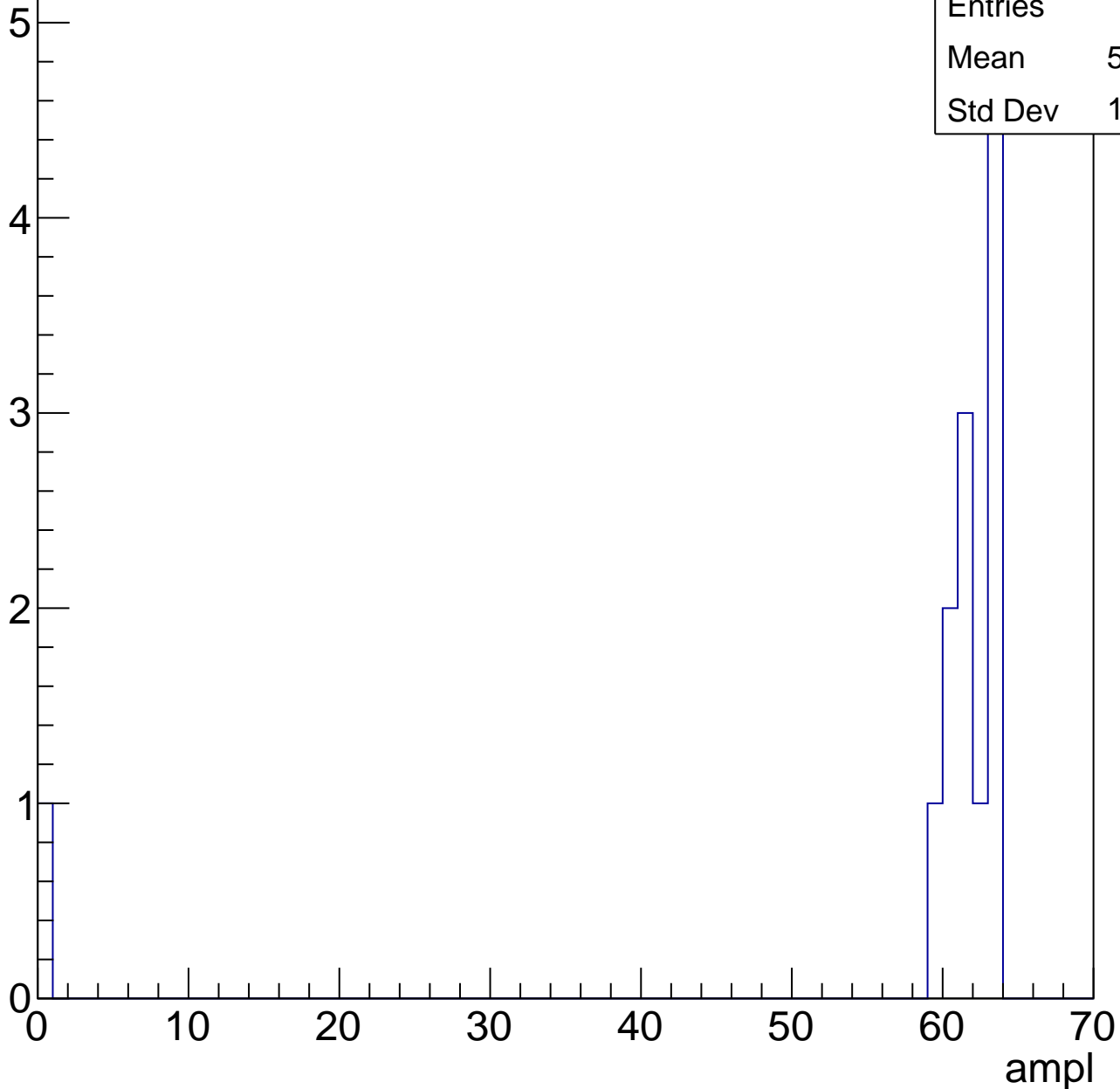


# B1L102S, U16-ch68, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	13
Mean	56.85
Std Dev	16.46





# B1L102S, U16-ch68, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U16-ch69, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	75
Mean	26.35
Std Dev	6.541

**Gaus mean : 27.9405**

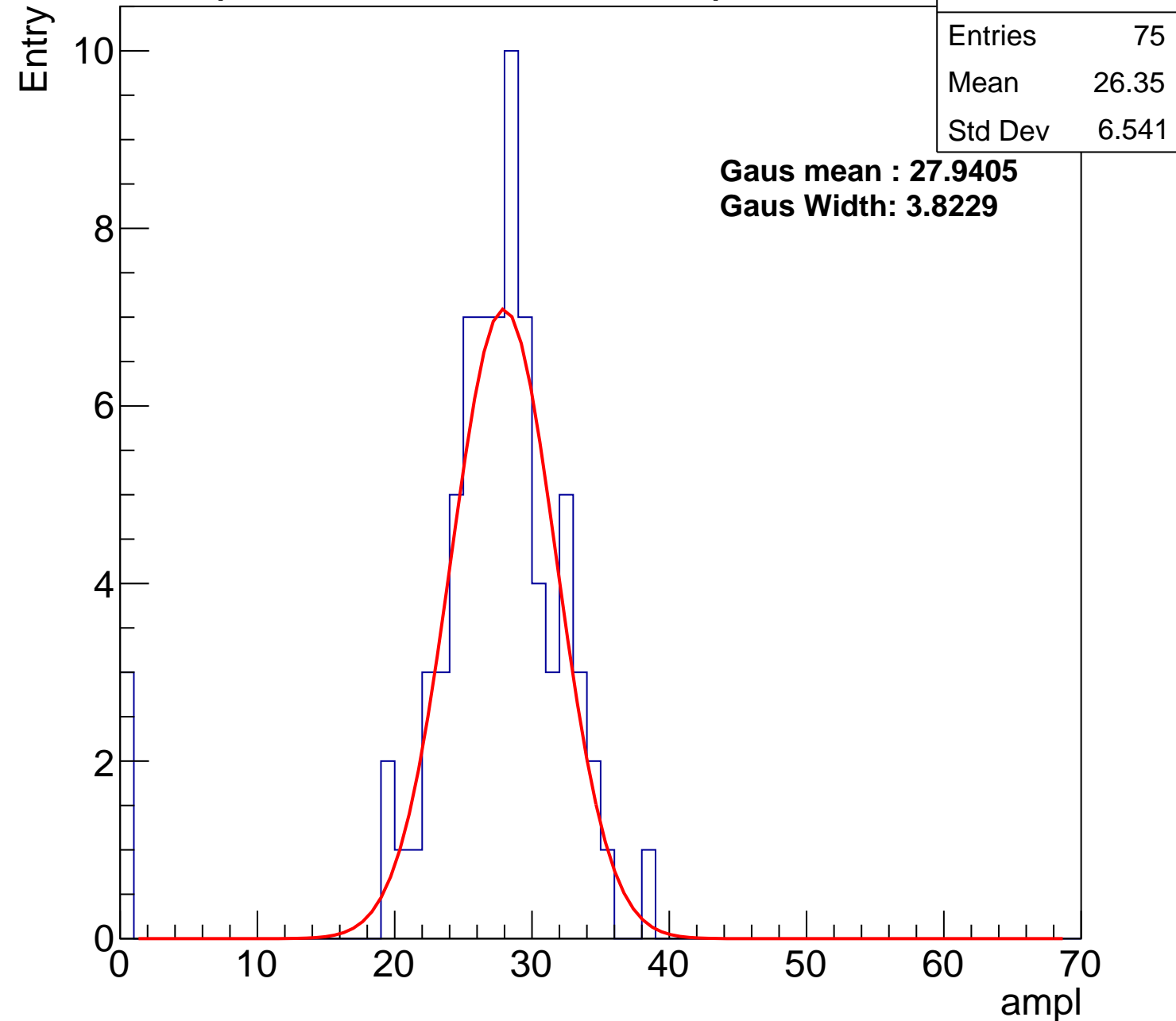
**Gaus Width: 3.8229**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U16-ch69, adc1

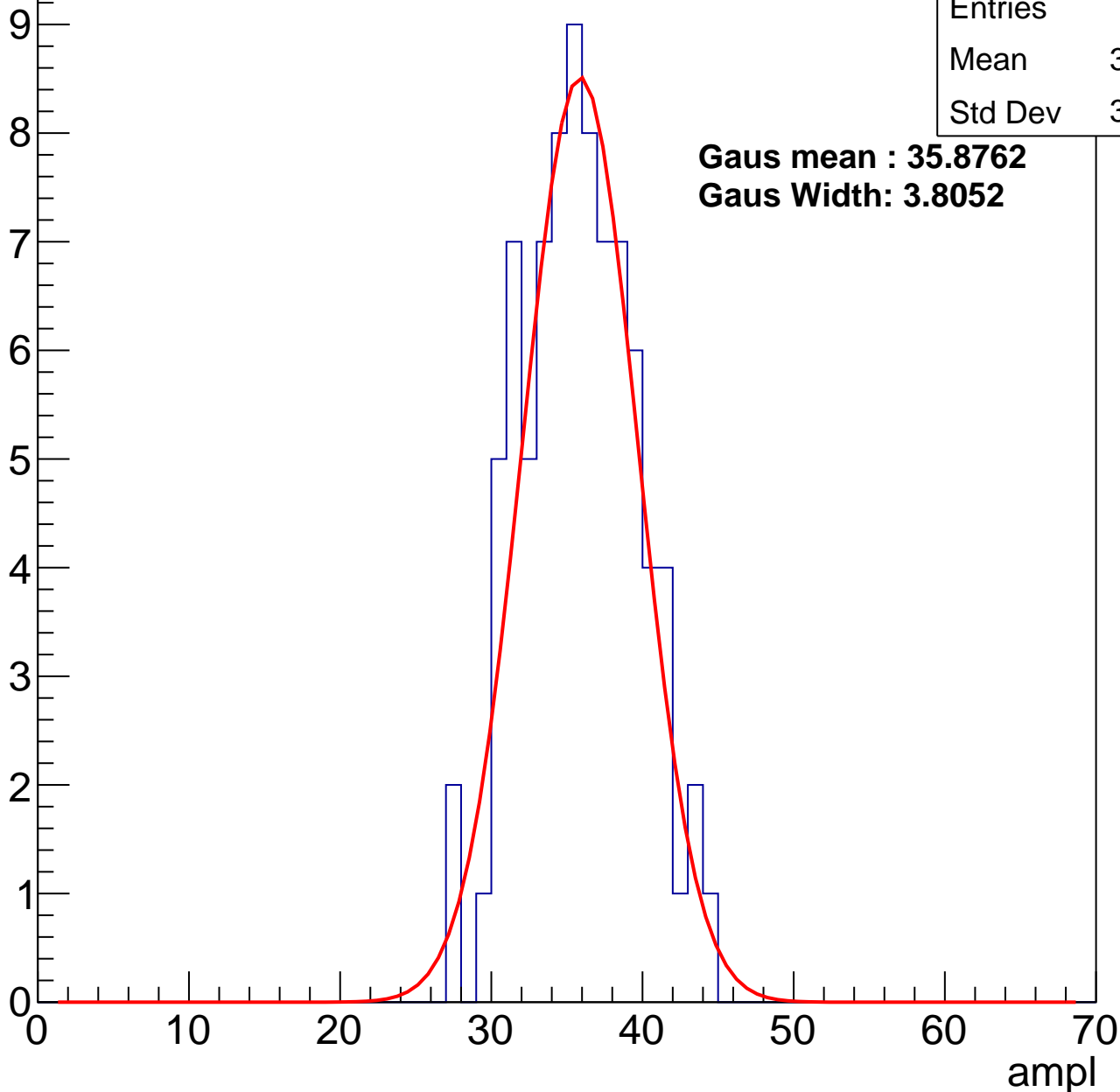
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	35.37
Std Dev	3.728

**Gaus mean : 35.8762**

**Gaus Width: 3.8052**



# B1L102S, U16-ch69, adc2

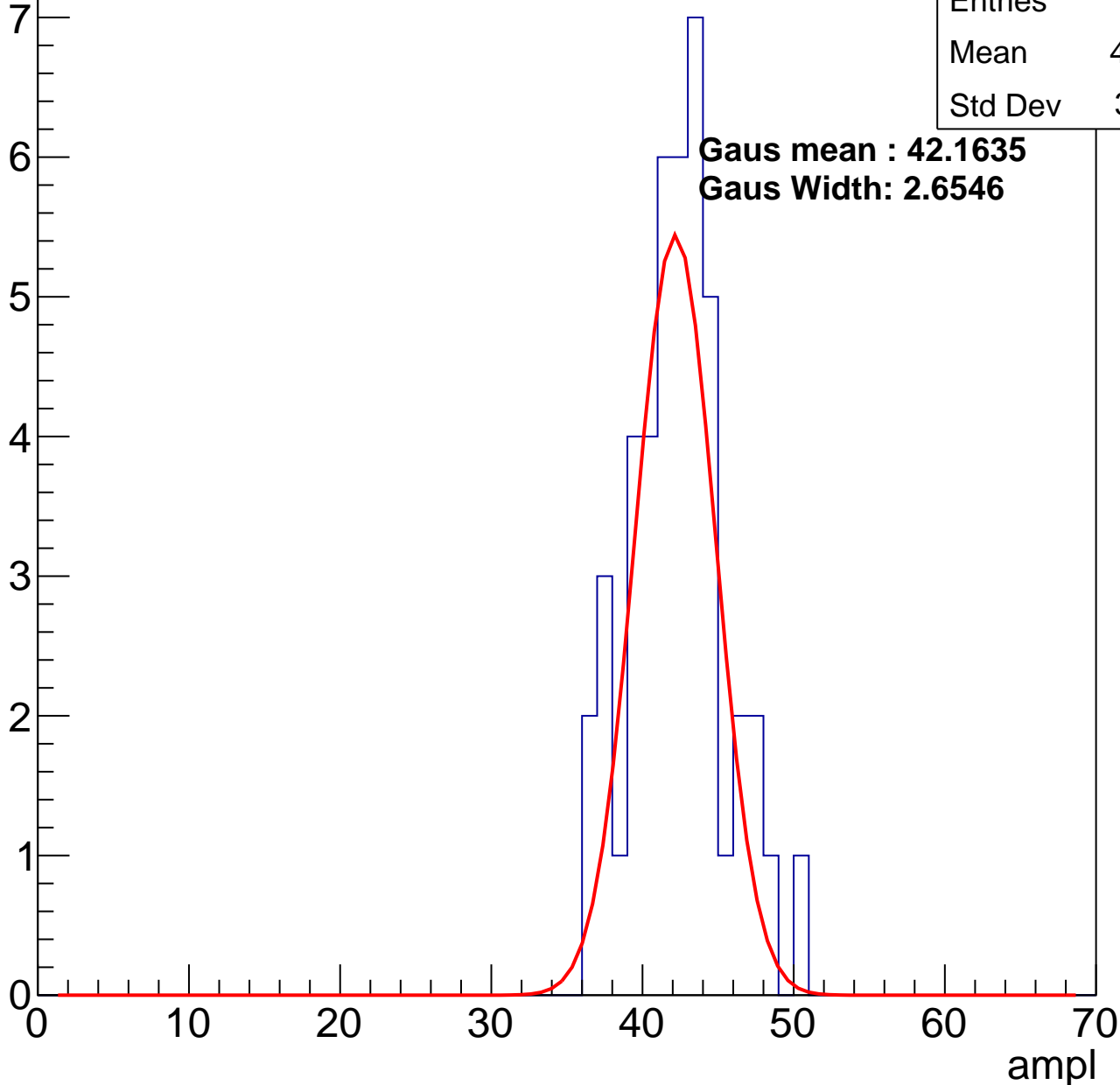
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	41.89
Std Dev	3.121

**Gaus mean : 42.1635**

**Gaus Width: 2.6546**

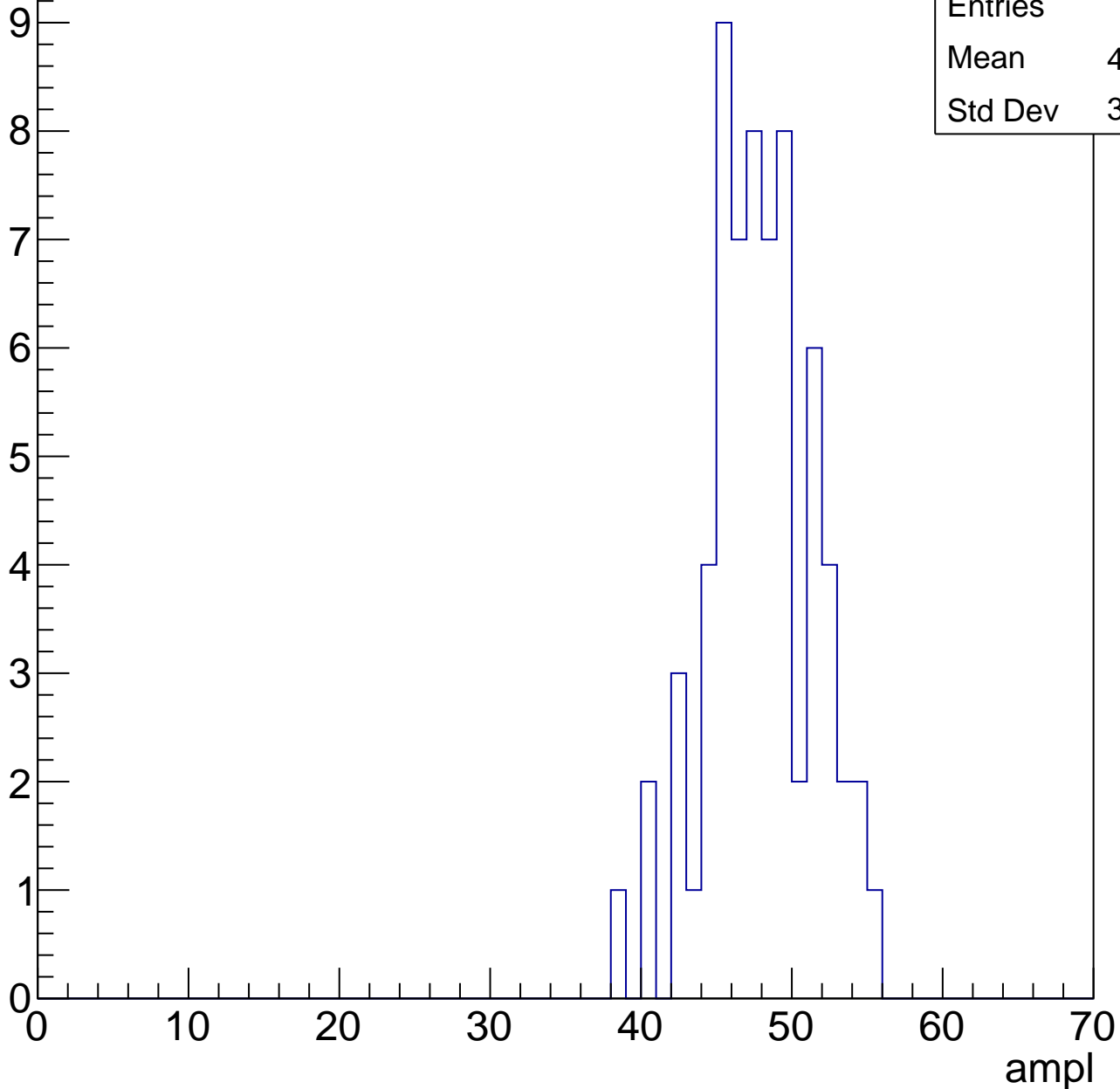


# B1L102S, U16-ch69, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

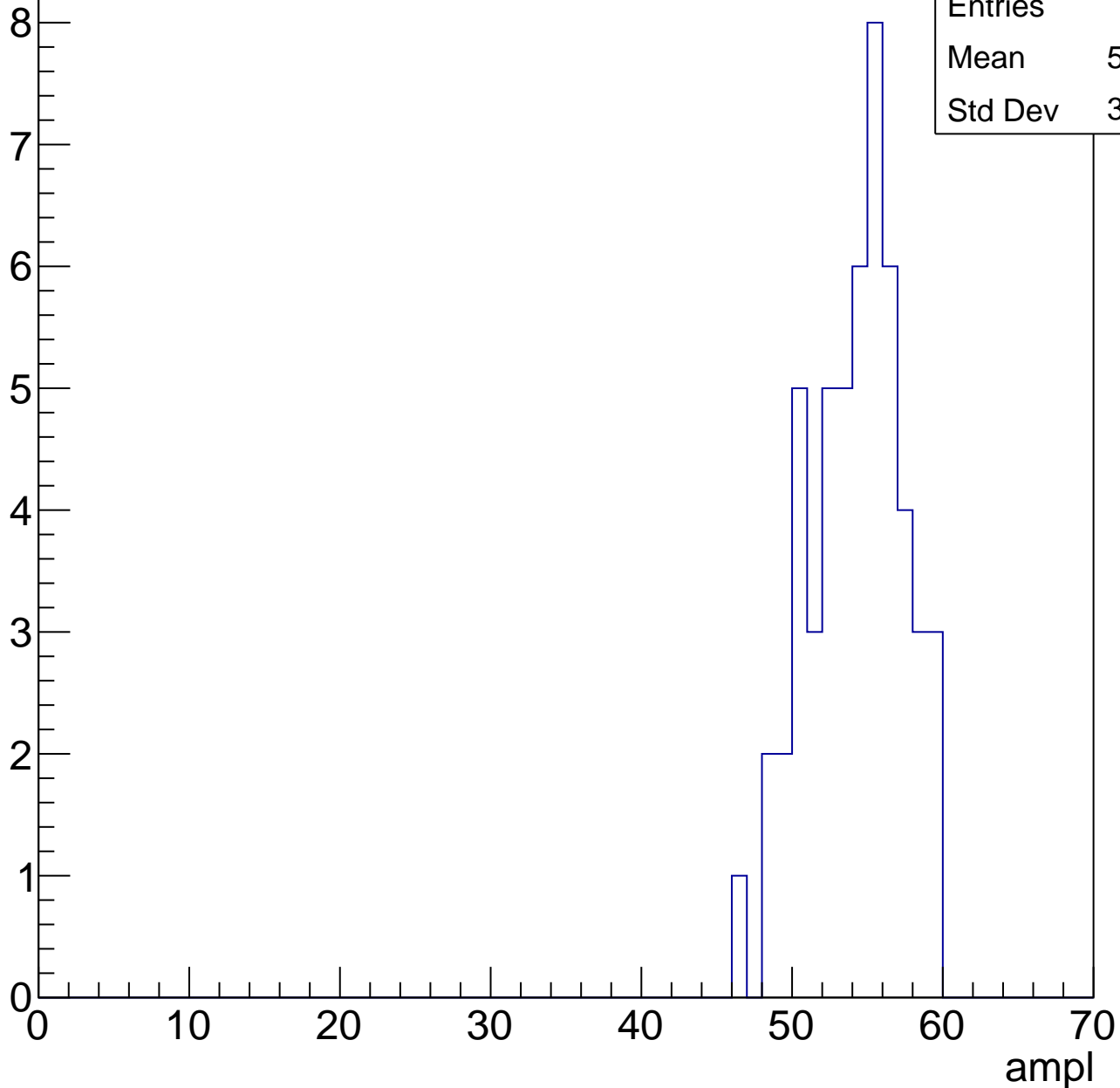
Entries	67
Mean	47.42
Std Dev	3.508



# B1L102S, U16-ch69, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

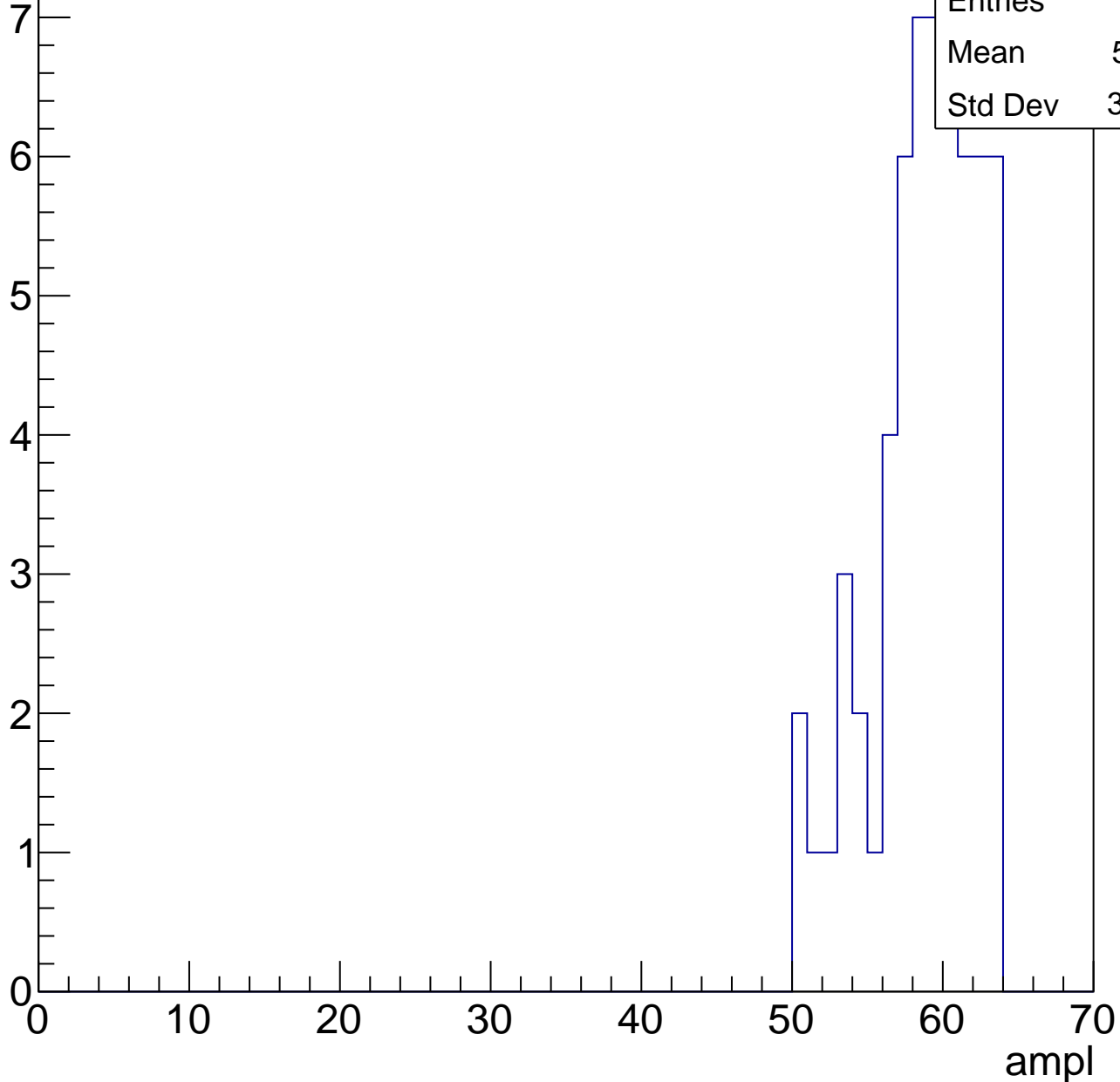


Entries	53
Mean	53.72
Std Dev	3.086

# B1L102S, U16-ch69, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

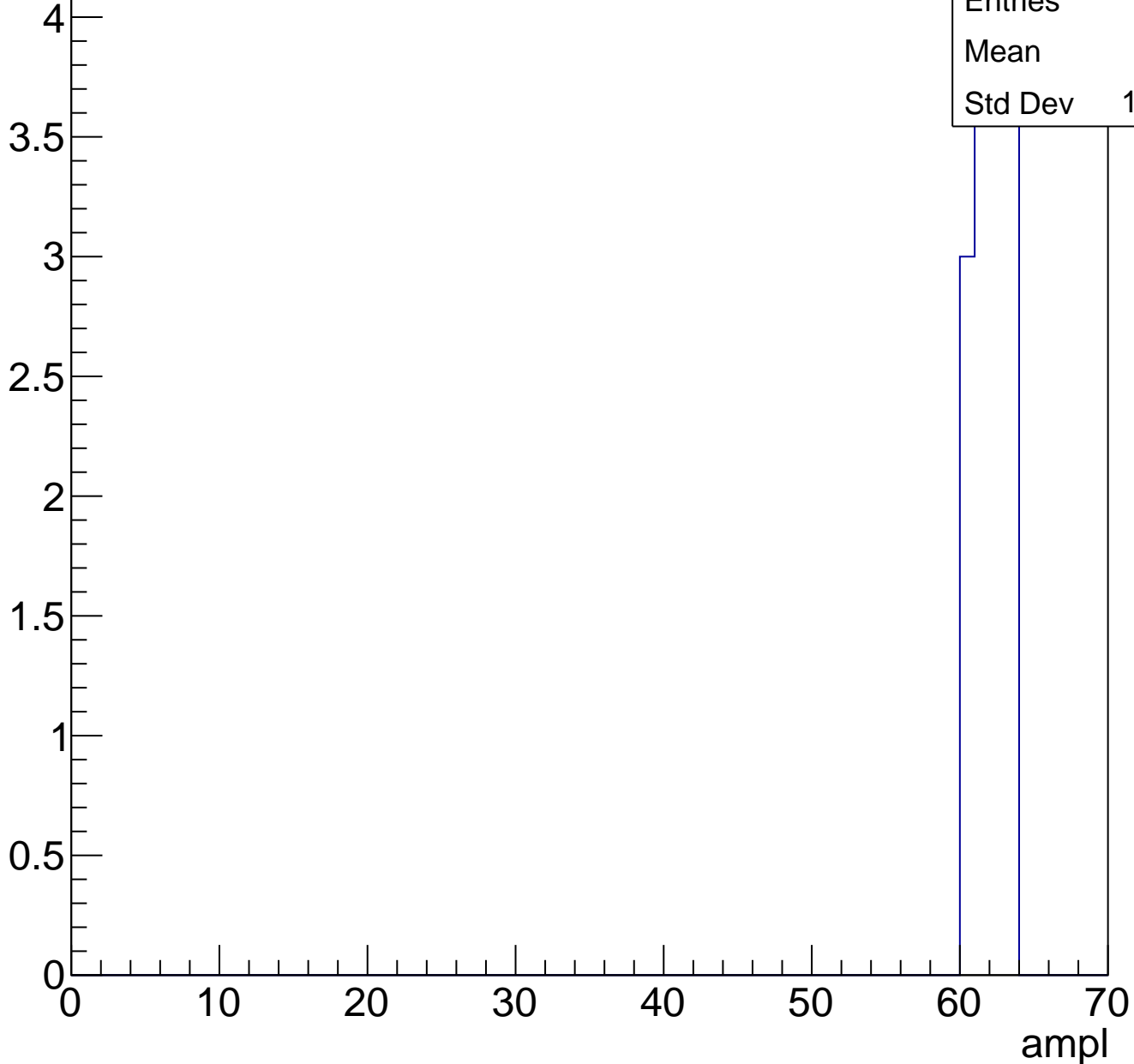


Entries	59
Mean	58.41
Std Dev	3.386

# B1L102S, U16-ch69, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch69, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch70, adc0

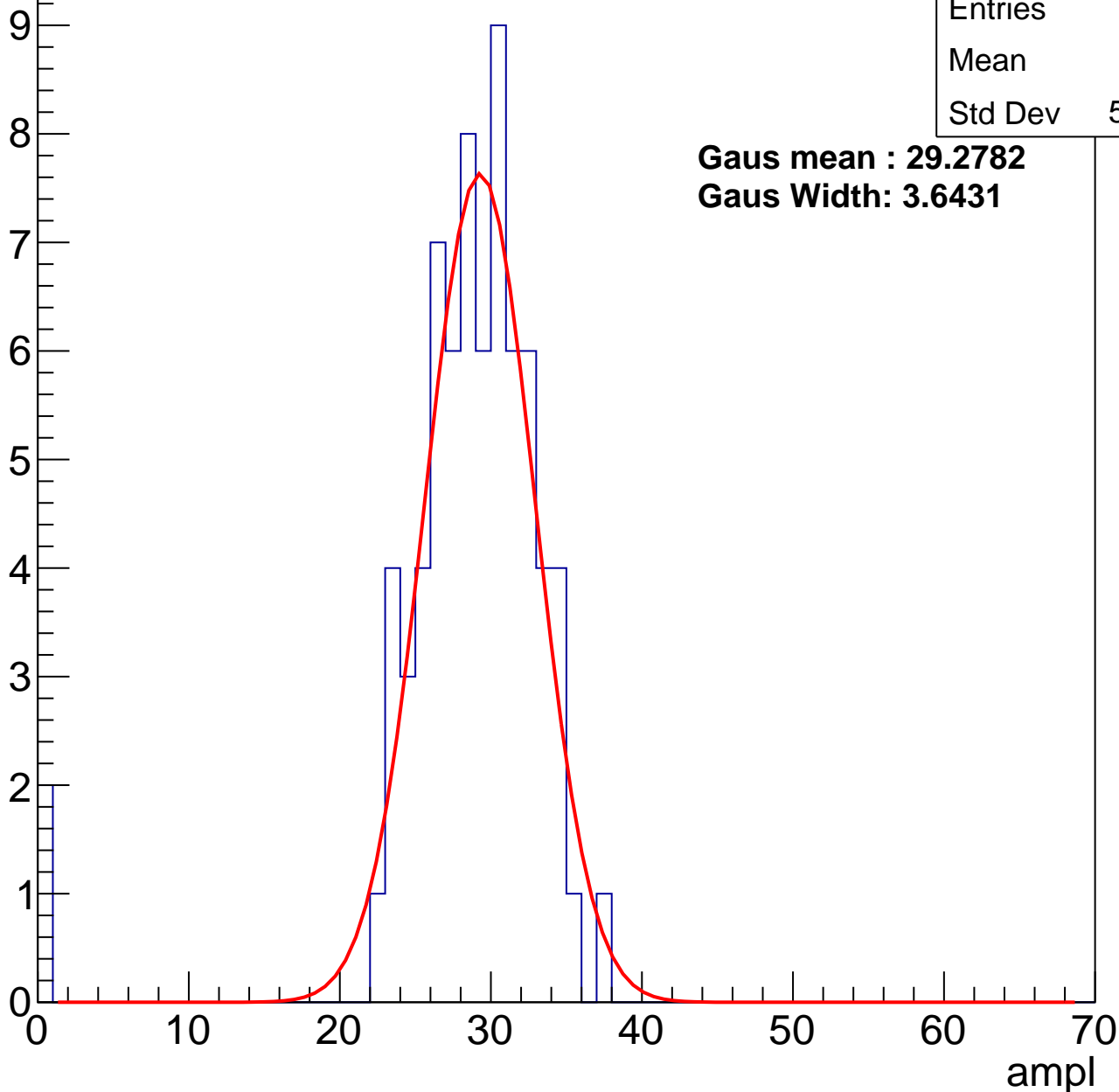
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	28
Std Dev	5.759

**Gaus mean : 29.2782**

**Gaus Width: 3.6431**



# B1L102S, U16-ch70, adc1

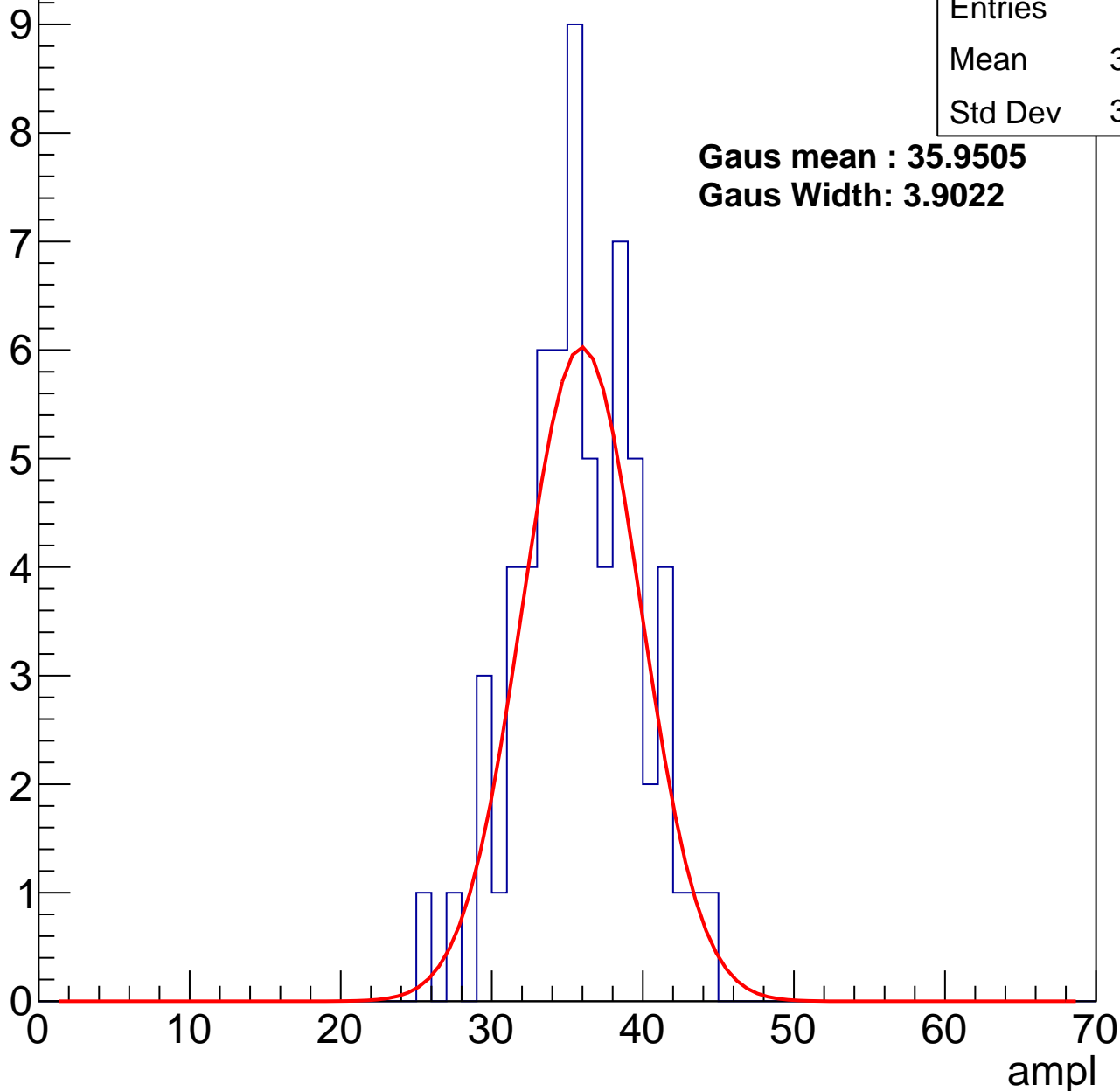
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	35.38
Std Dev	3.862

**Gaus mean : 35.9505**

**Gaus Width: 3.9022**



# B1L102S, U16-ch70, adc2

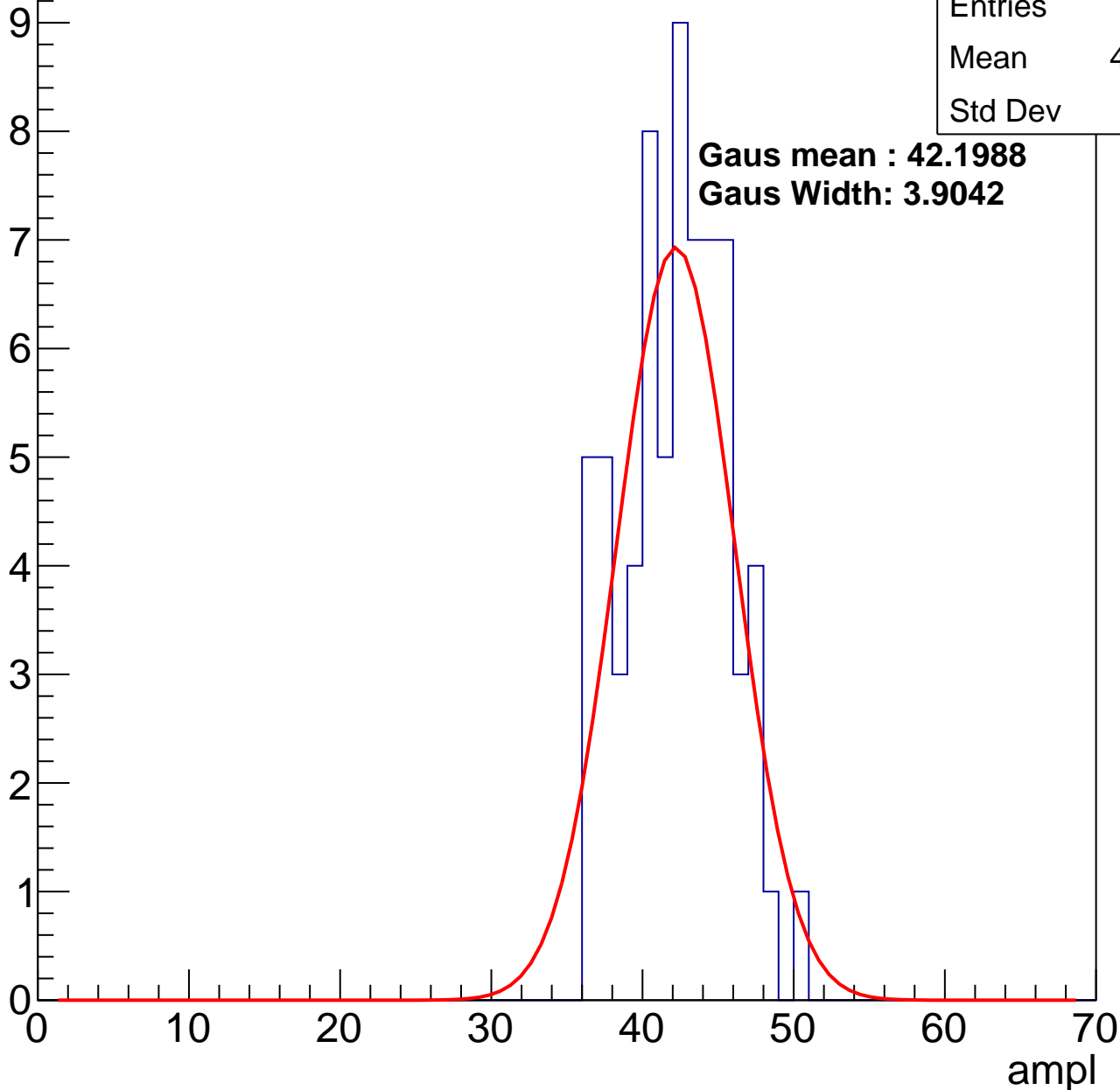
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	41.83
Std Dev	3.34

**Gaus mean : 42.1988**

**Gaus Width: 3.9042**

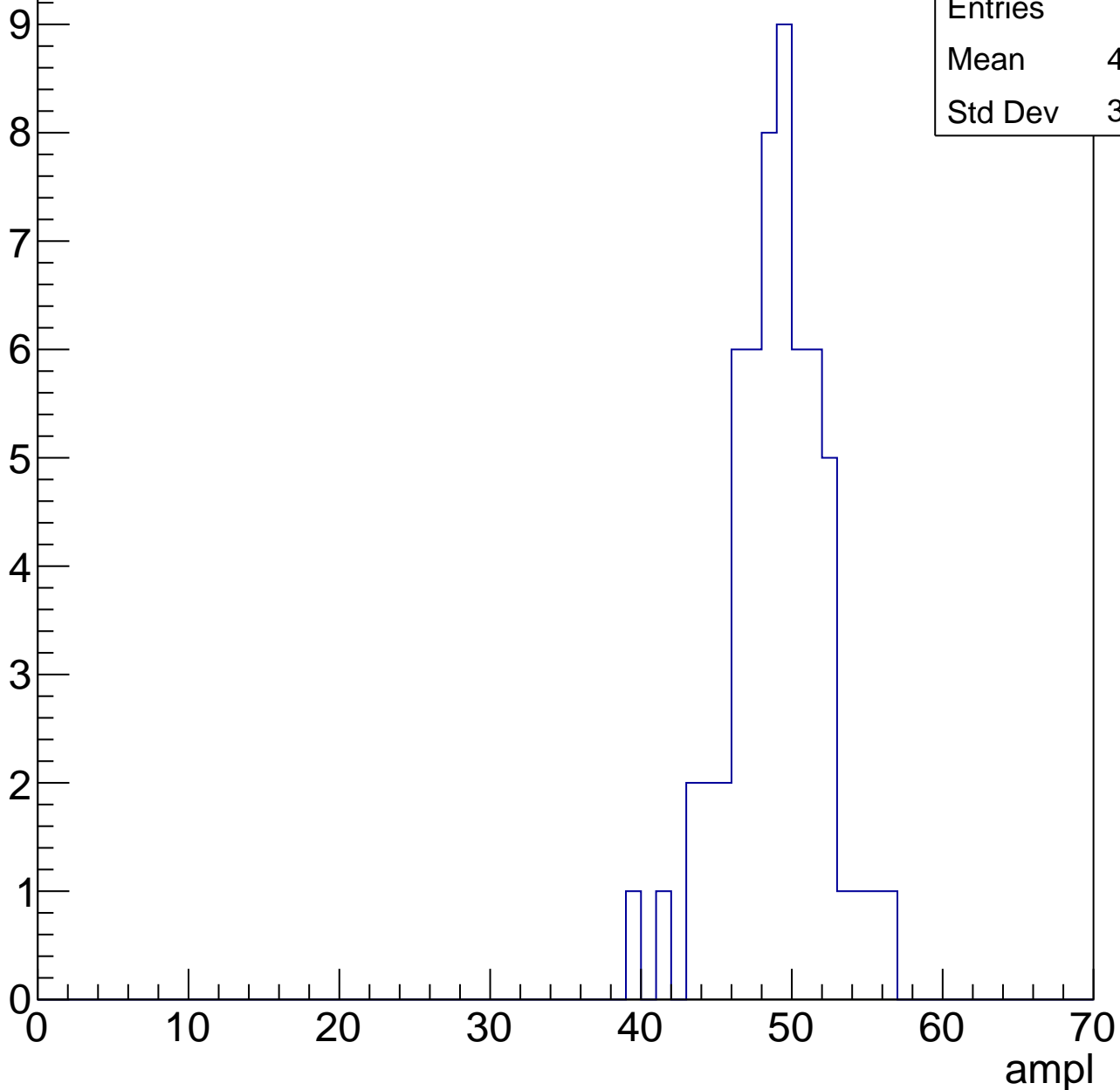


# B1L102S, U16-ch70, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

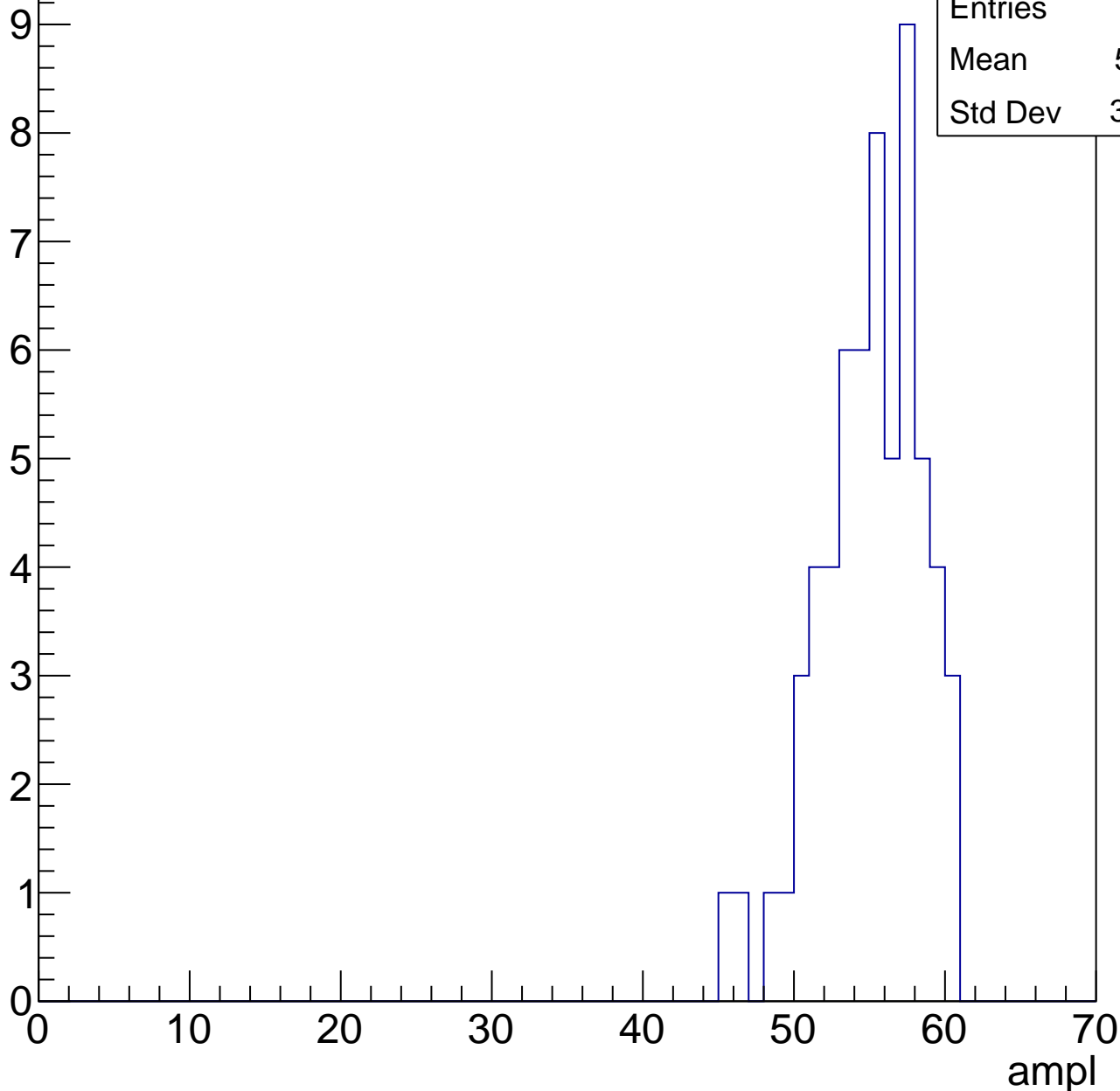
Entries	58
Mean	48.47
Std Dev	3.185



# B1L102S, U16-ch70, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



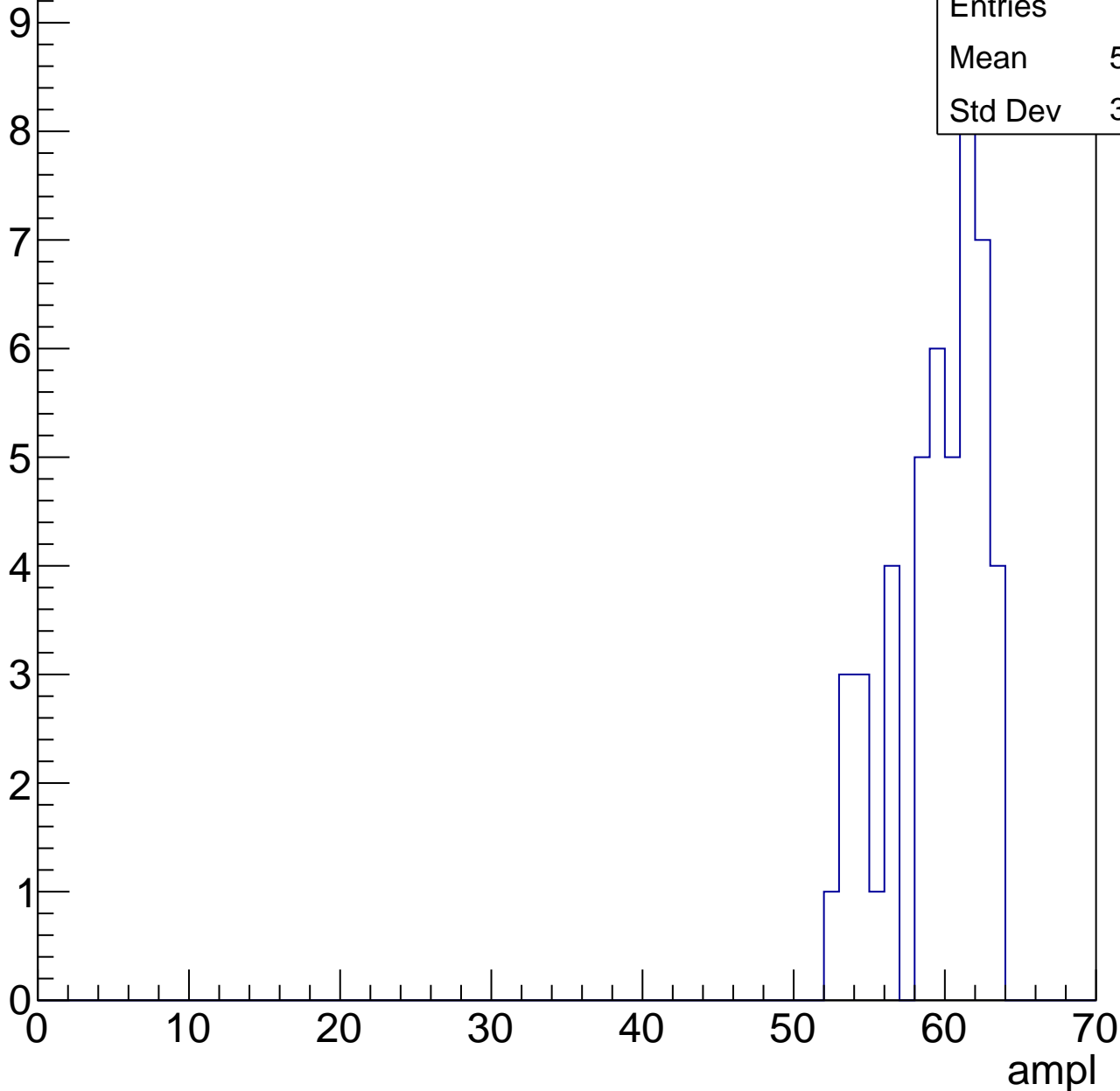
Entries	61
Mean	54.61
Std Dev	3.355

# B1L102S, U16-ch70, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	58.98
Std Dev	3.086

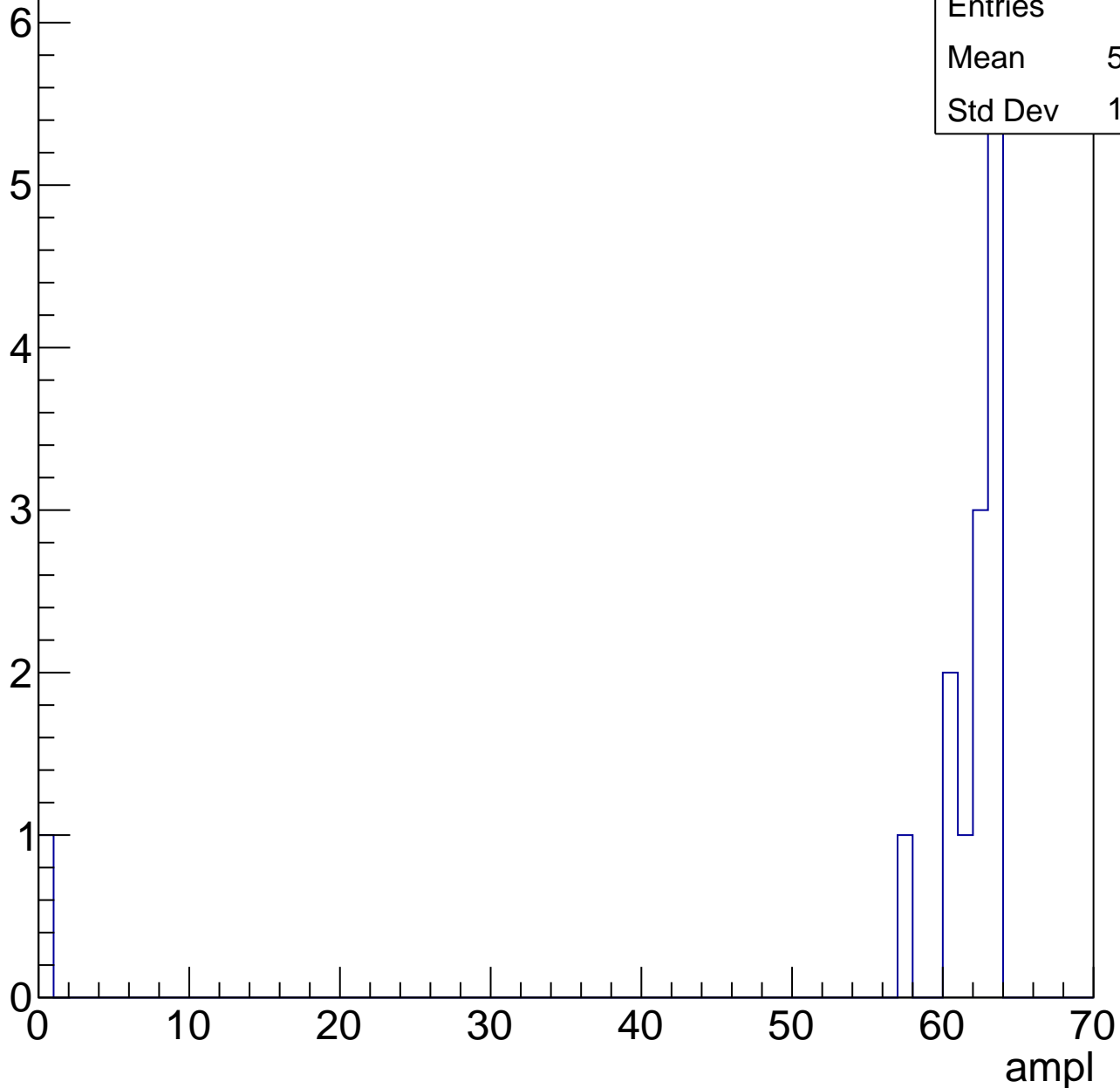


# B1L102S, U16-ch70, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	14
Mean	57.29
Std Dev	15.98





# B1L102S, U16-ch70, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U16-ch71, adc0

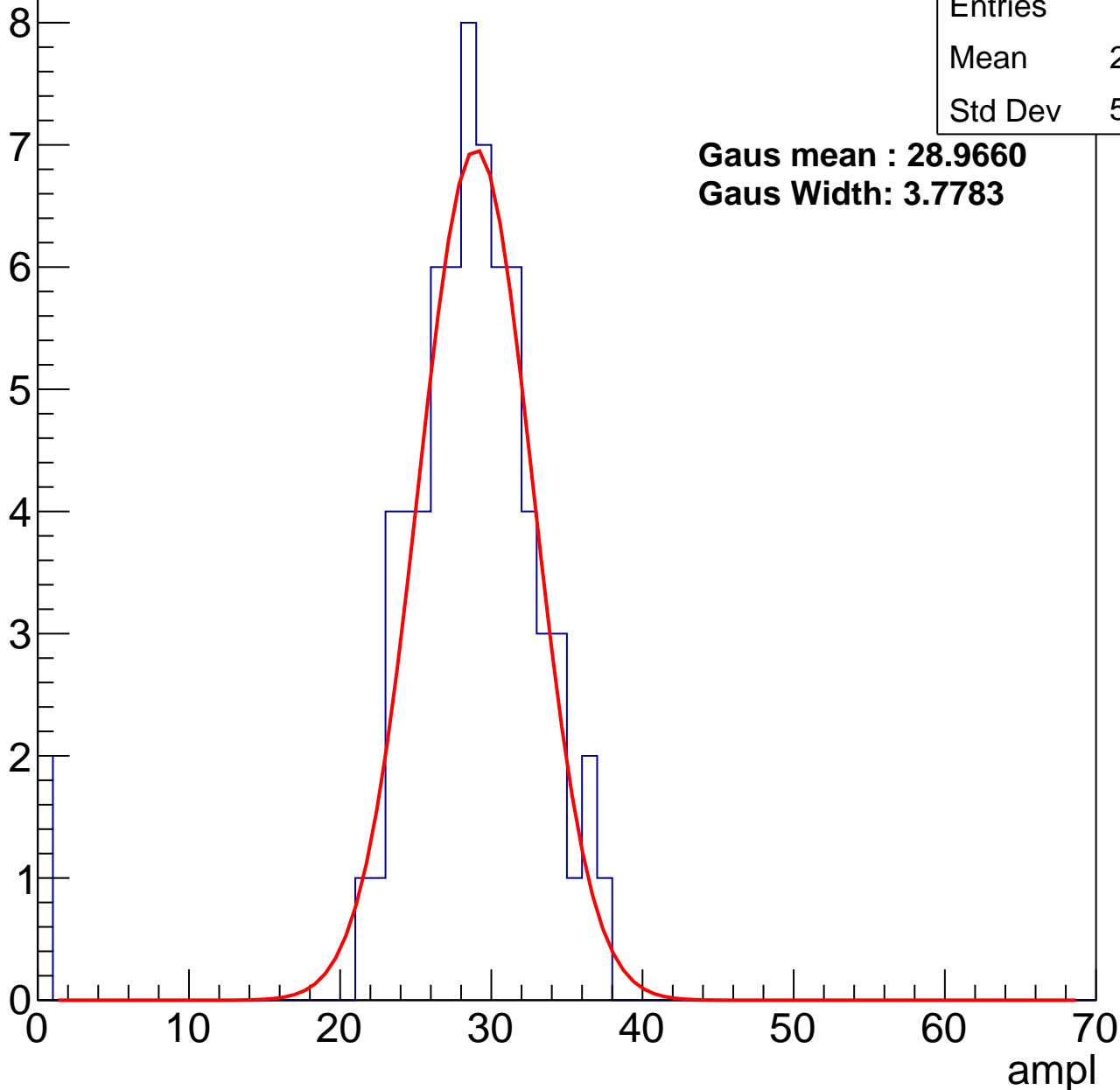
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	27.75
Std Dev	5.982

**Gaus mean : 28.9660**

**Gaus Width: 3.7783**



# B1L102S, U16-ch71, adc1

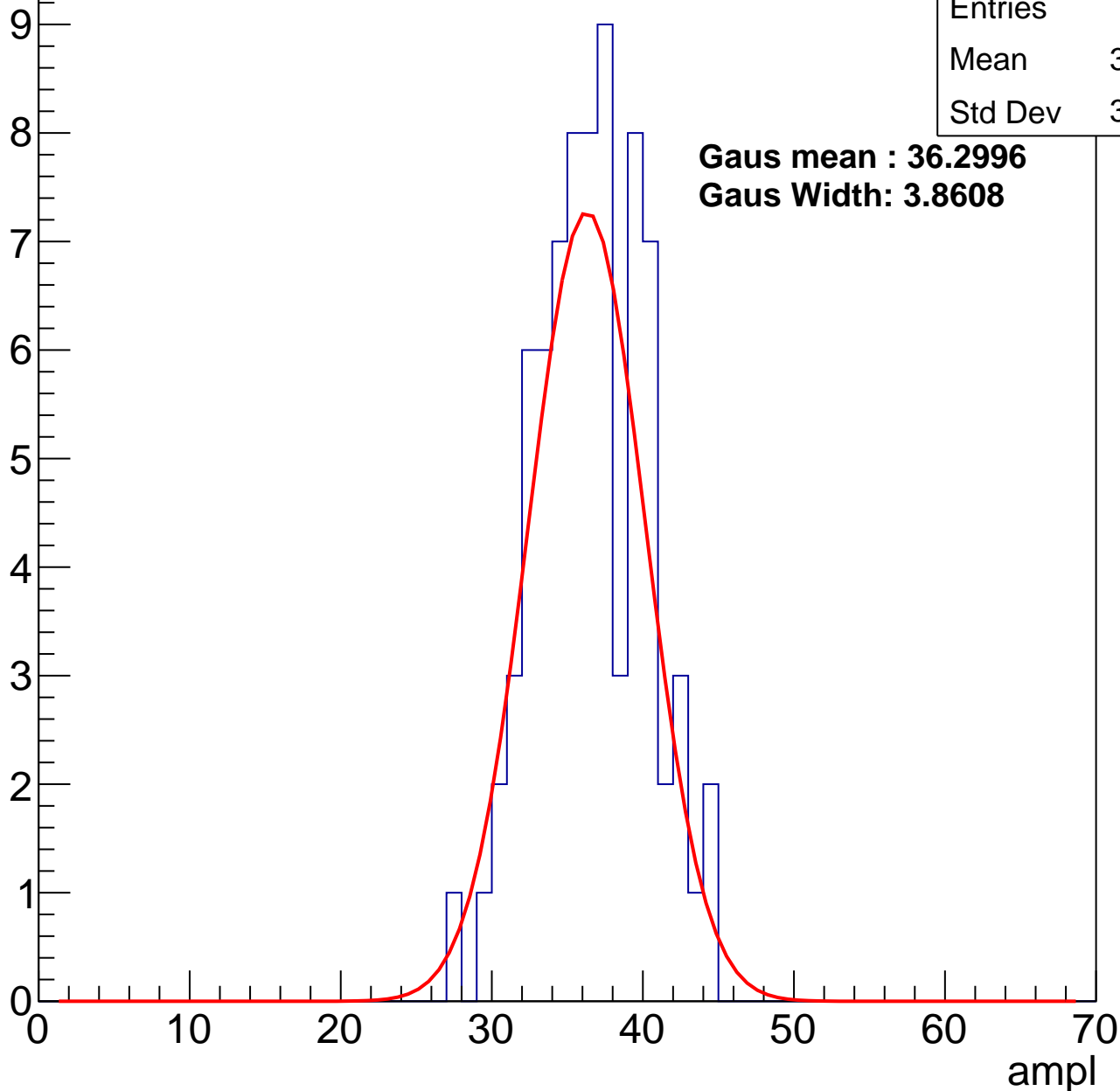
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	36.14
Std Dev	3.606

**Gaus mean : 36.2996**

**Gaus Width: 3.8608**



# B1L102S, U16-ch71, adc2

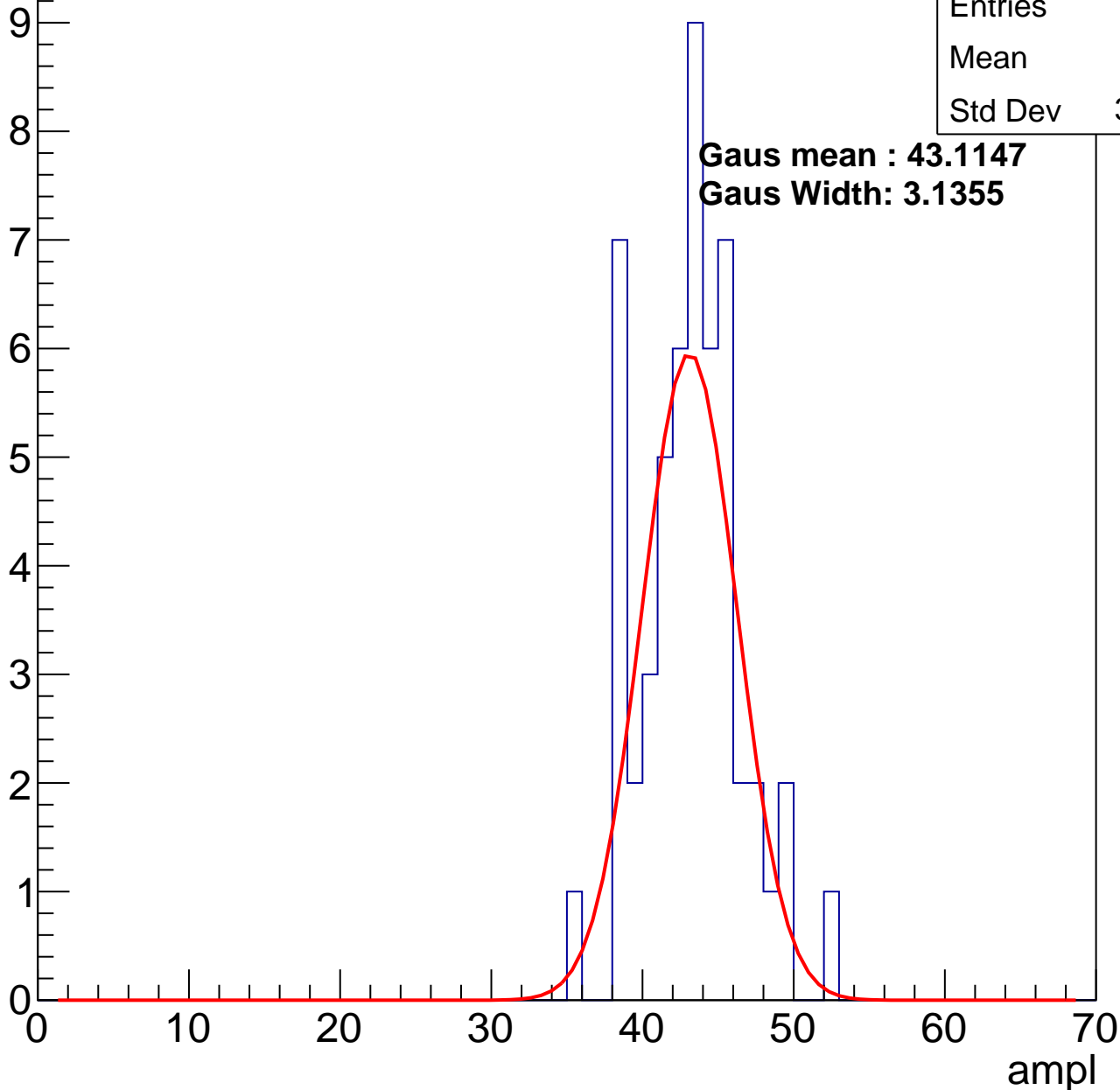
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	42.7
Std Dev	3.281

**Gaus mean : 43.1147**

**Gaus Width: 3.1355**

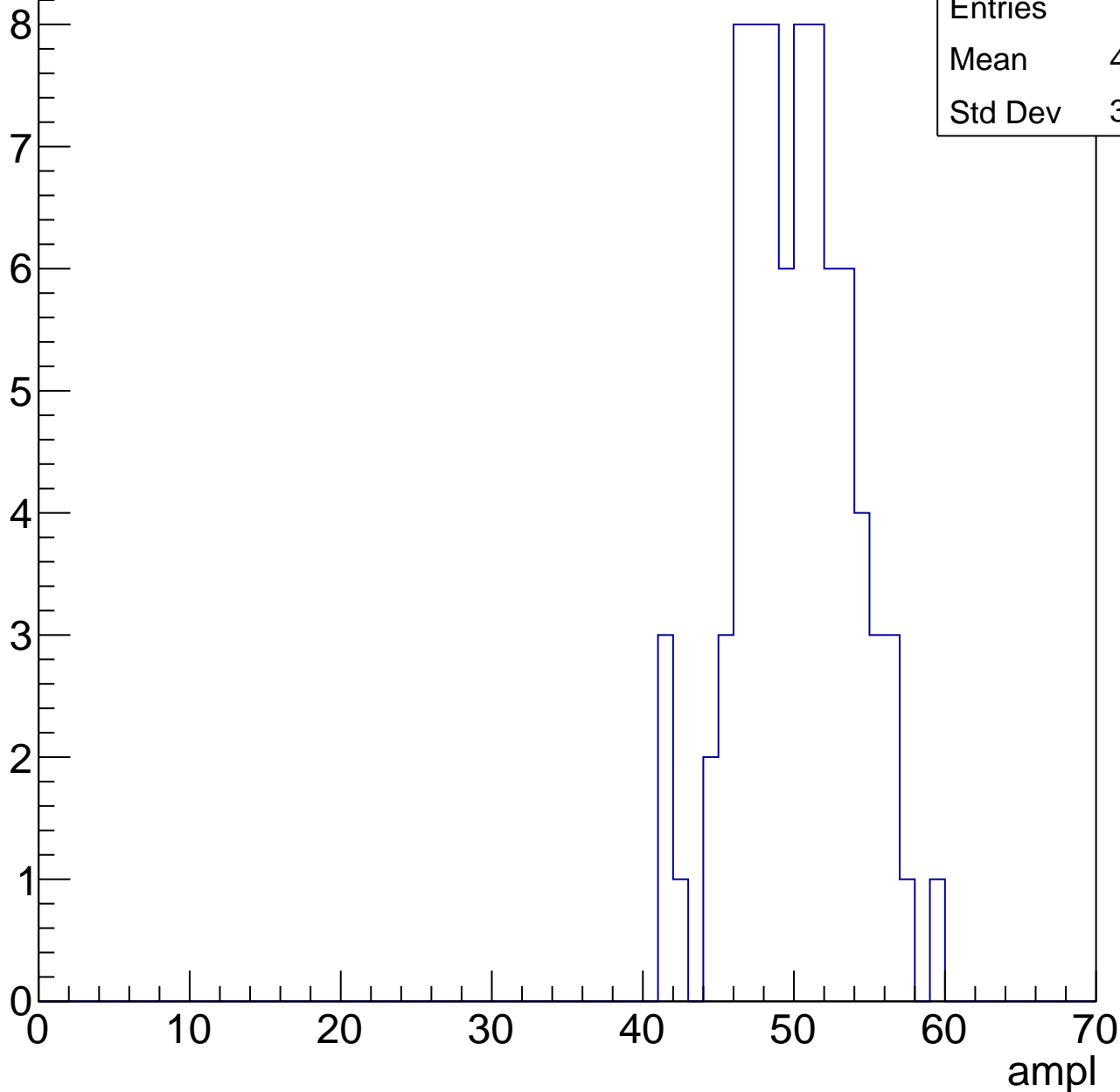


# B1L102S, U16-ch71, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	49.53
Std Dev	3.795

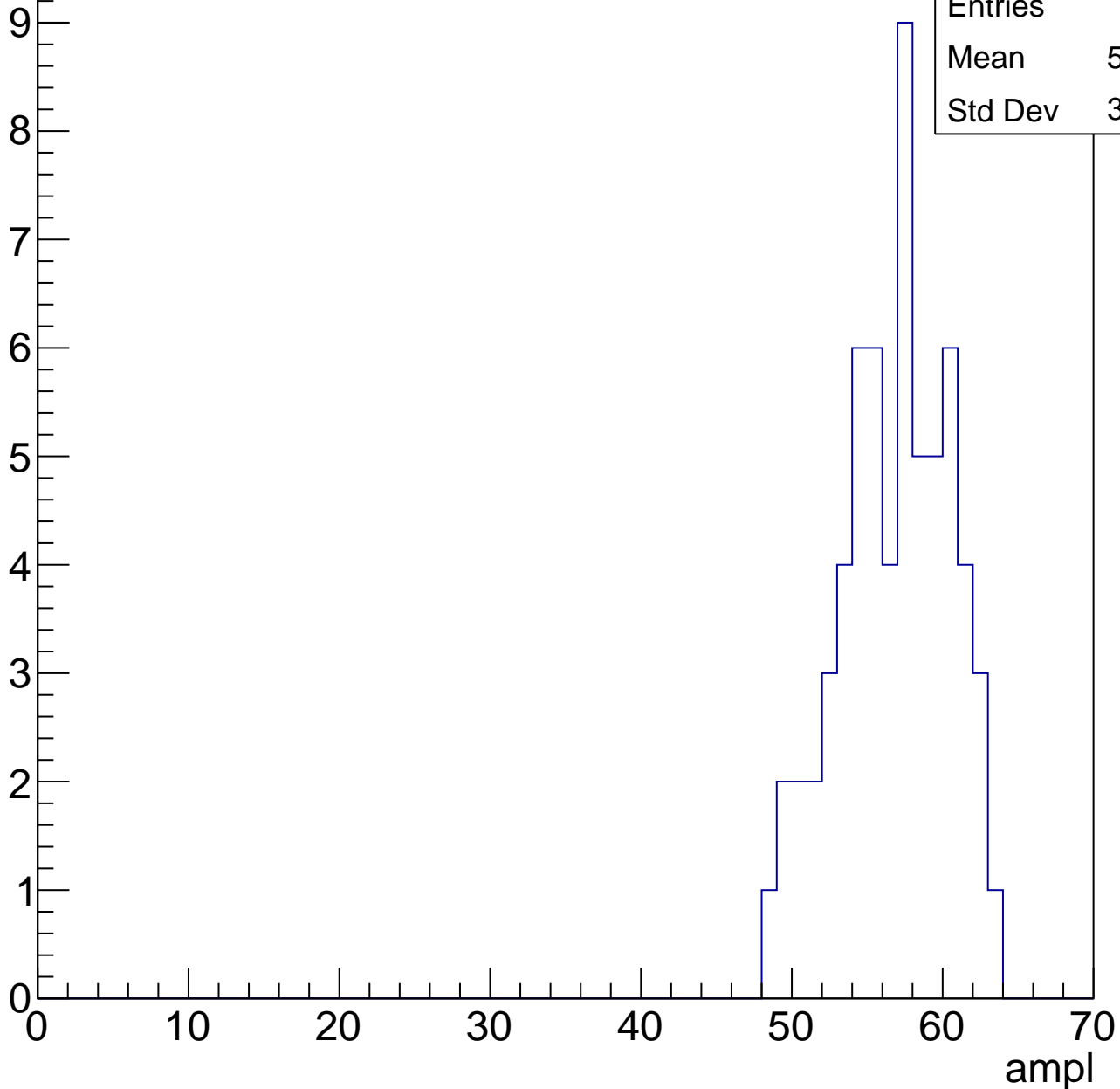


# B1L102S, U16-ch71, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	56.27
Std Dev	3.609

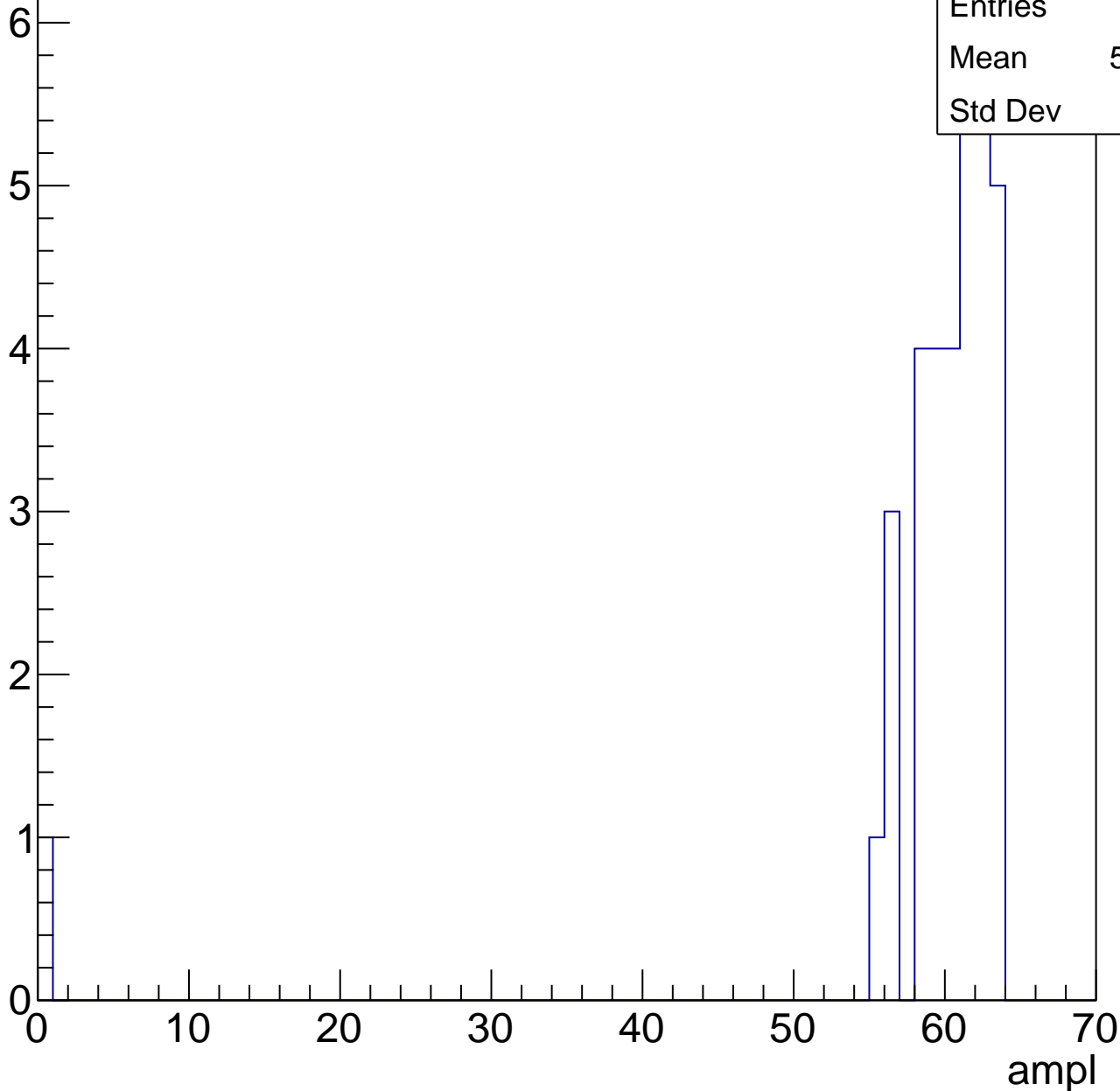


# B1L102S, U16-ch71, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

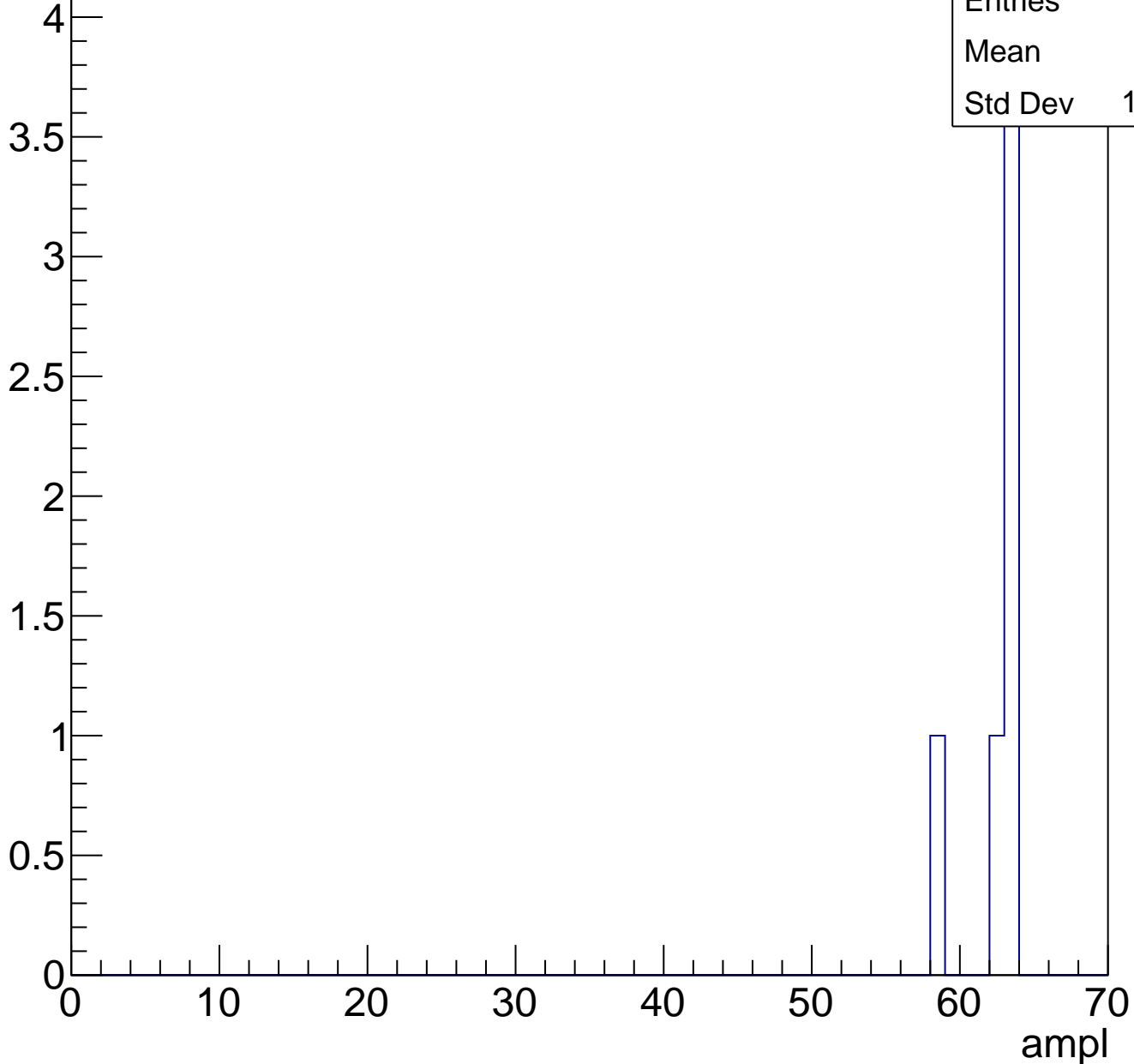
Entries	34
Mean	58.35
Std Dev	10.4



# B1L102S, U16-ch71, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch71, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U16-ch72, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	74
Mean	28.91
Std Dev	3.507

**Gaus mean : 29.4541**

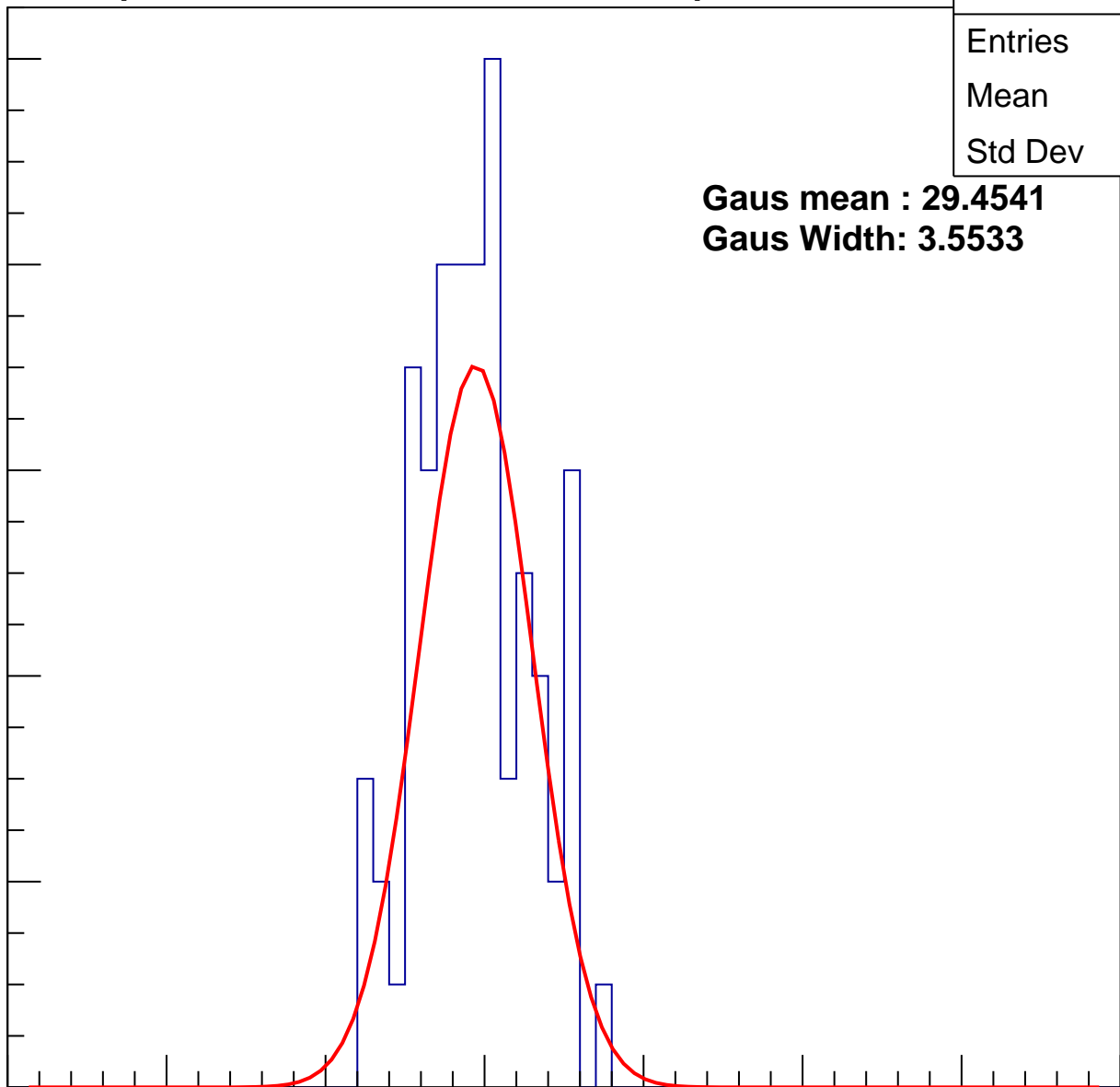
**Gaus Width: 3.5533**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U16-ch72, adc1

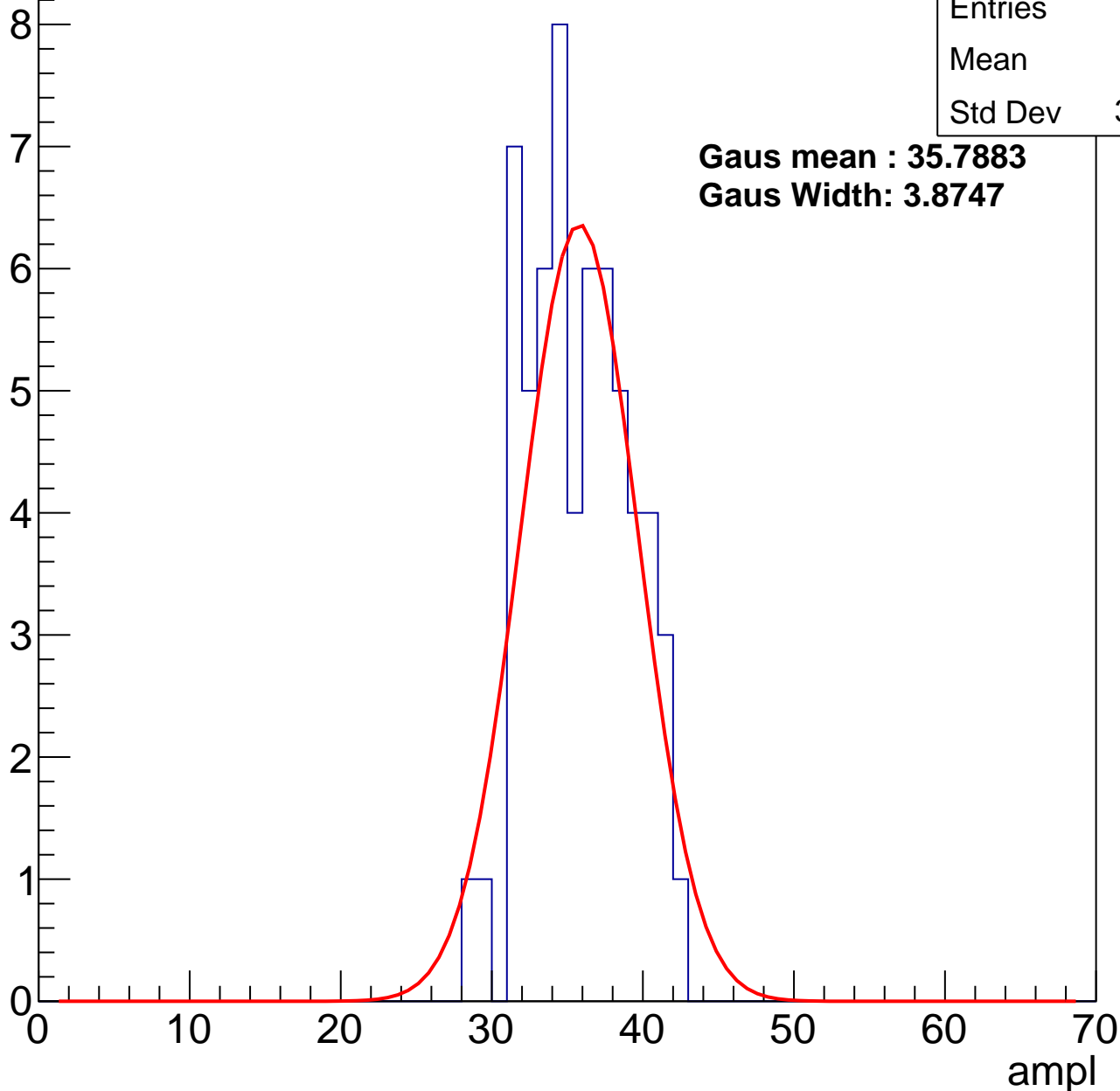
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	35.3
Std Dev	3.301

**Gaus mean : 35.7883**

**Gaus Width: 3.8747**



# B1L102S, U16-ch72, adc2

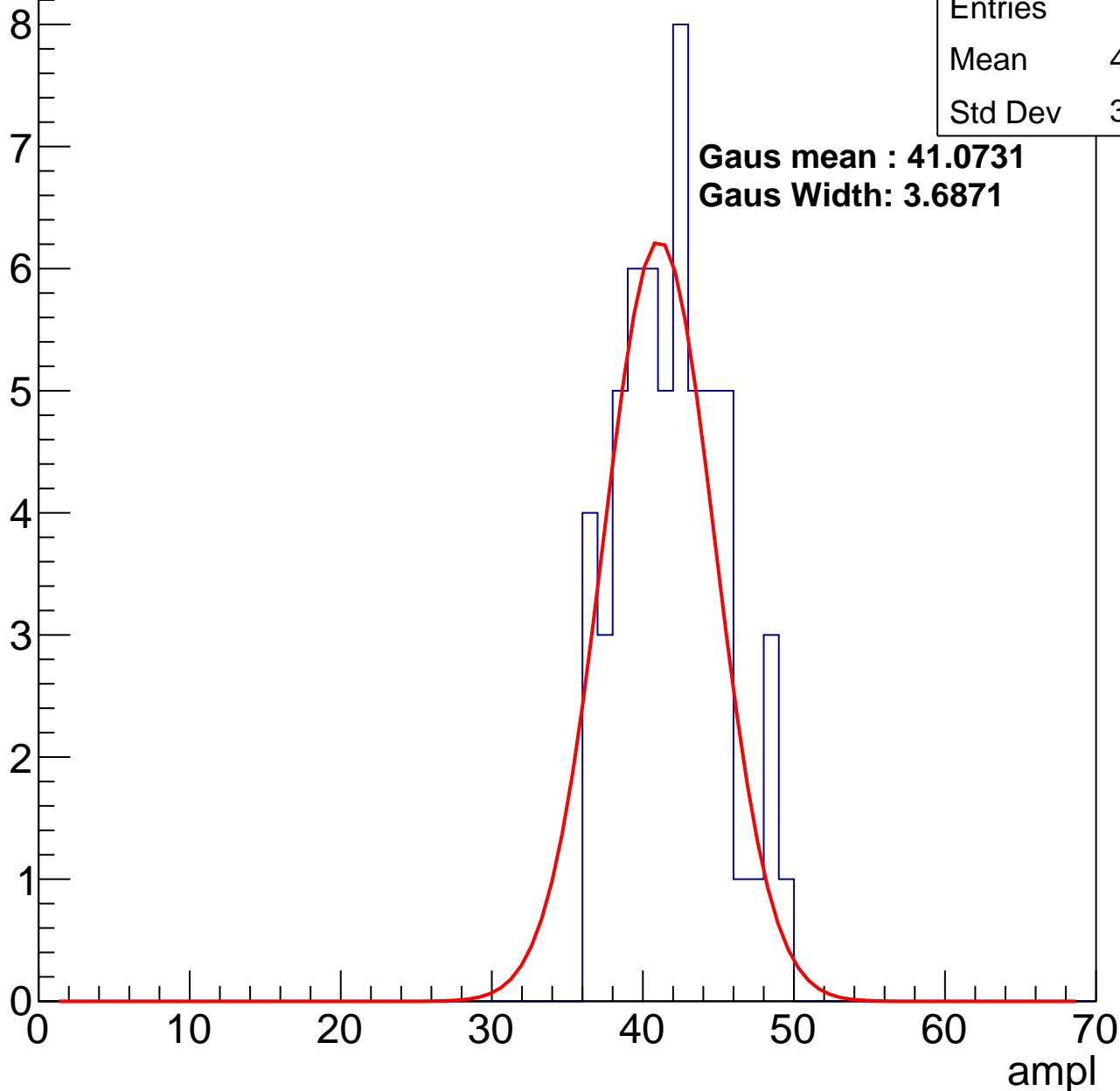
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	41.48
Std Dev	3.307

**Gaus mean : 41.0731**

**Gaus Width: 3.6871**

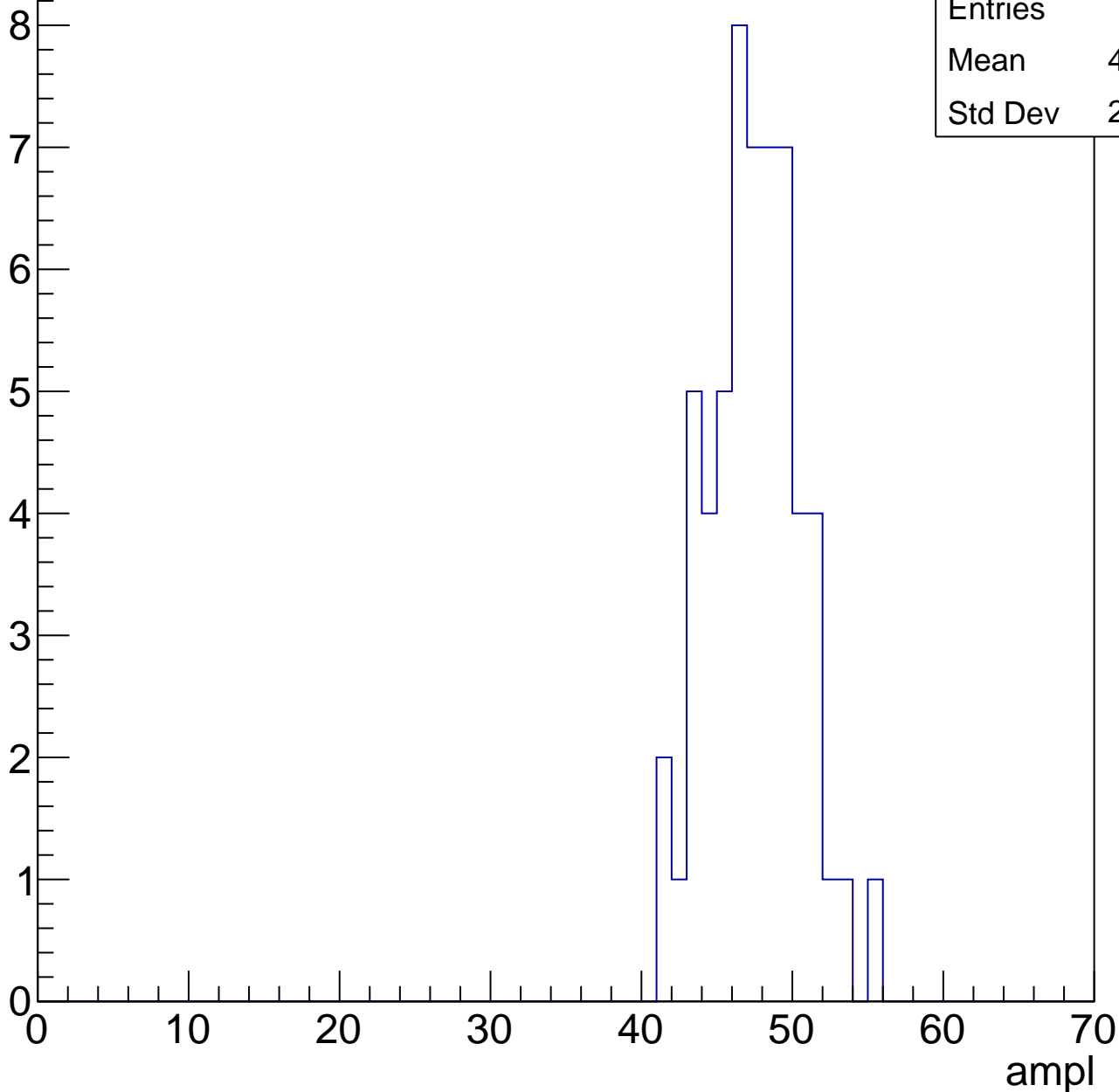


# B1L102S, U16-ch72, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	47.02
Std Dev	2.965

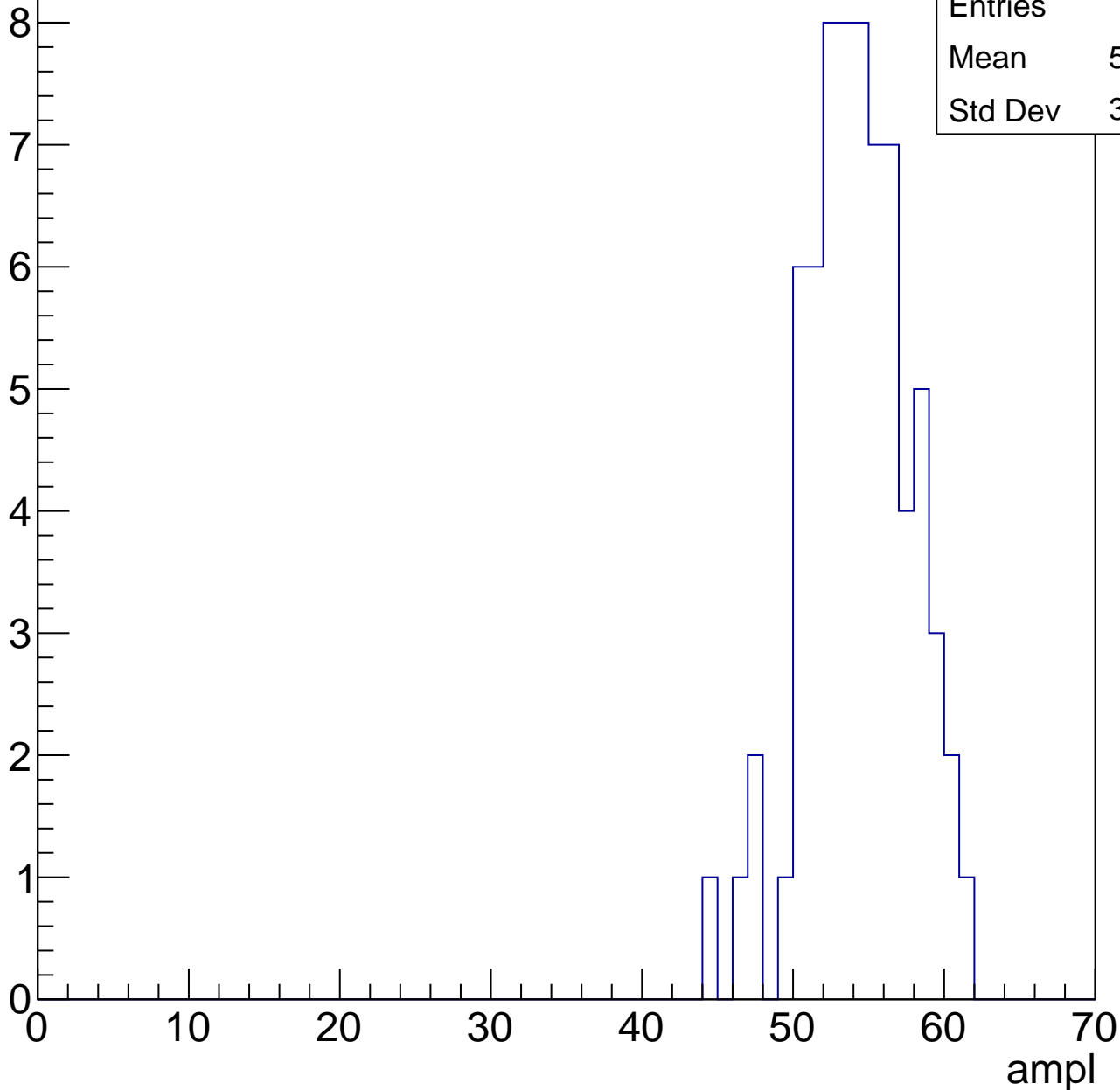


# B1L102S, U16-ch72, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

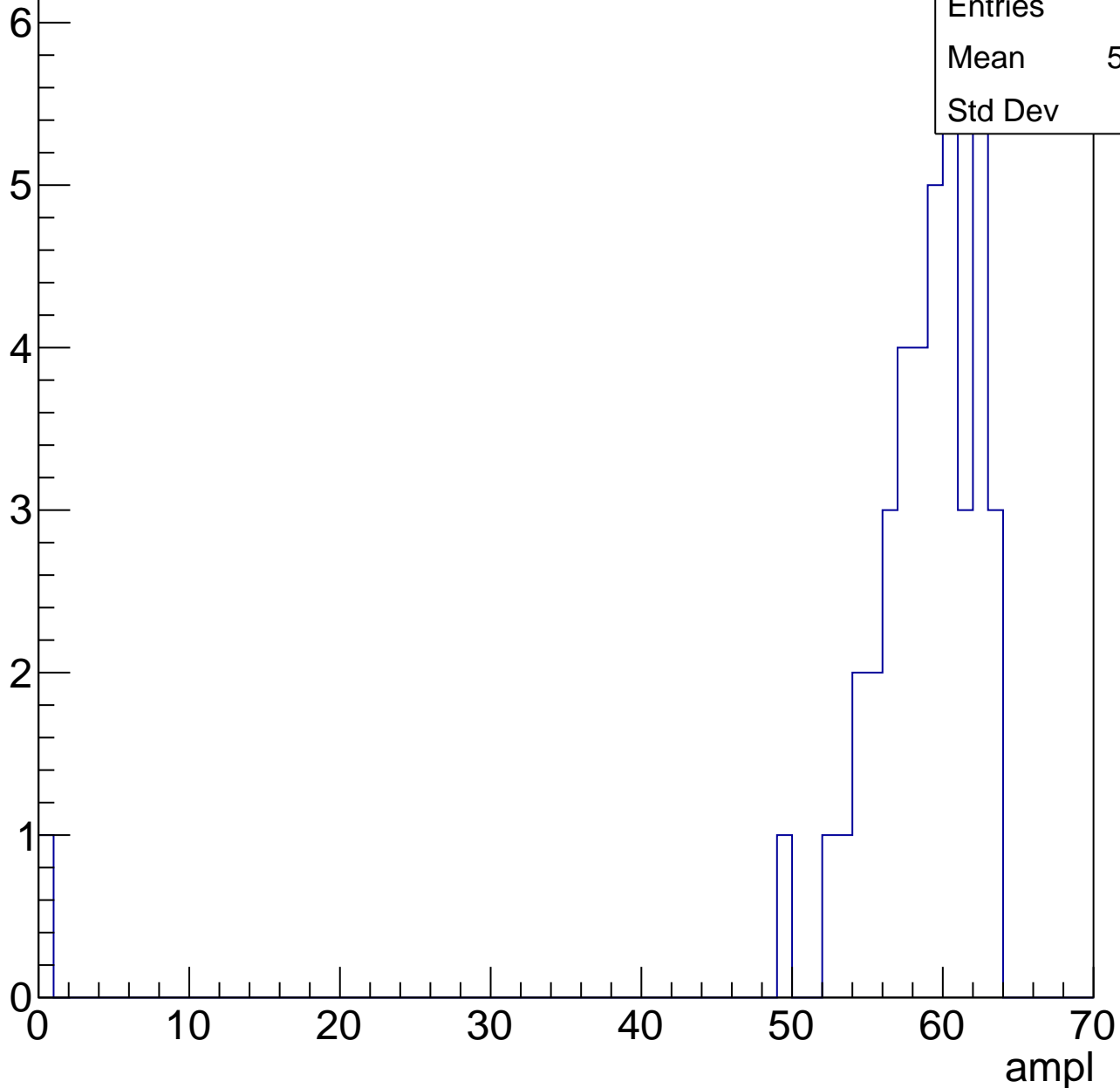
Entries	70
Mean	53.77
Std Dev	3.423



# B1L102S, U16-ch72, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

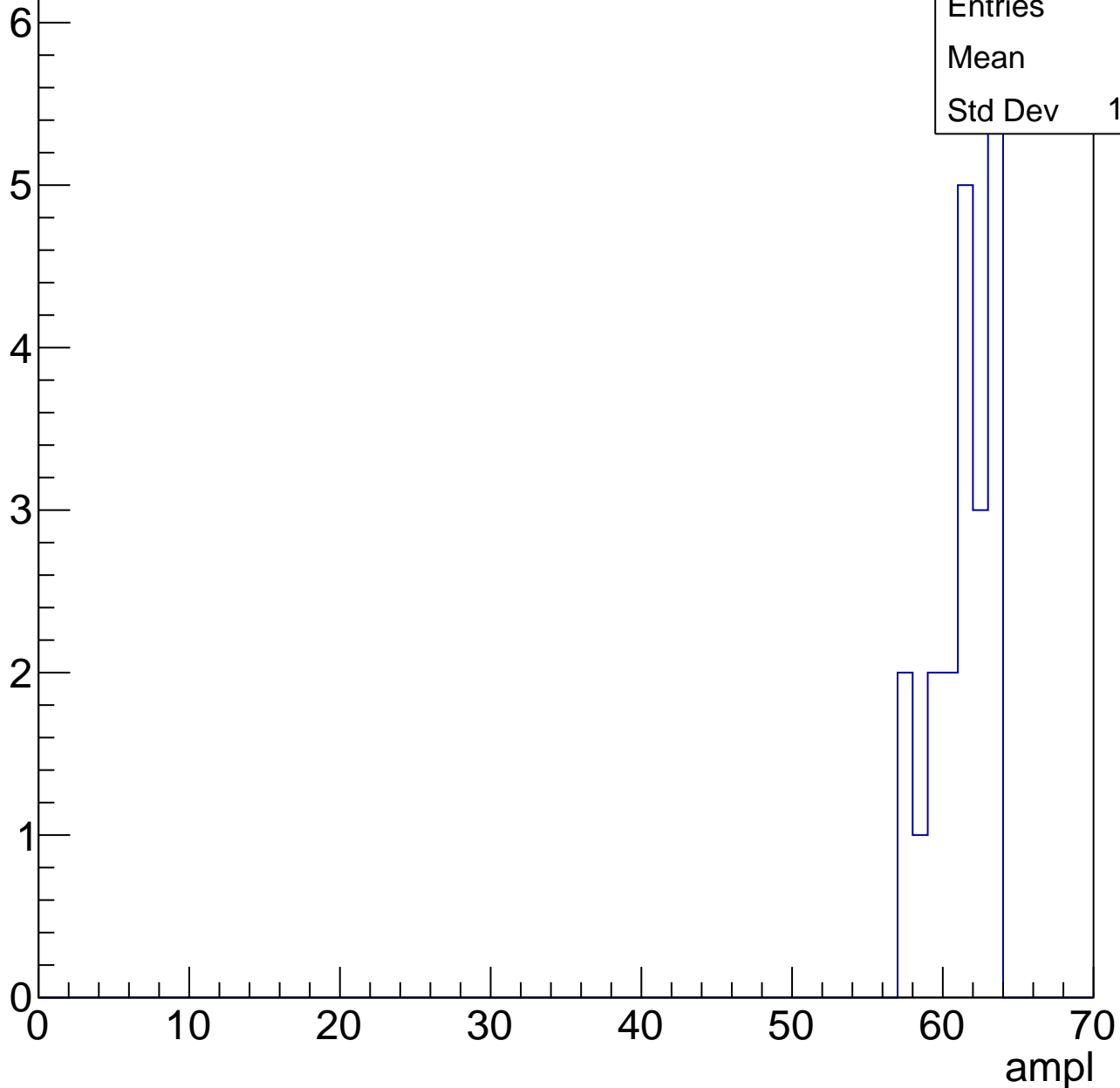


# B1L102S, U16-ch72, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	21
Mean	60.9
Std Dev	1.925

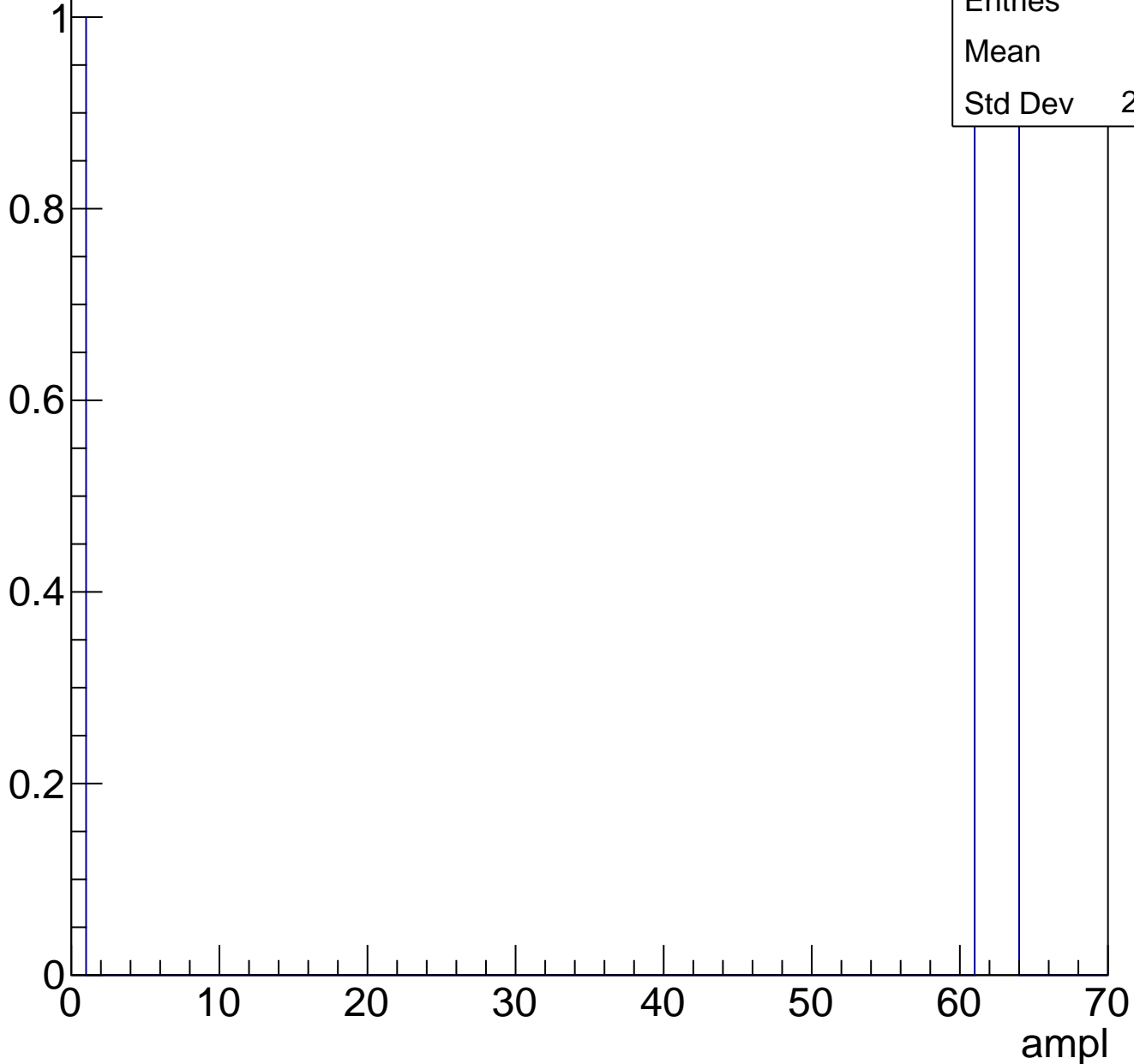




# B1L102S, U16-ch72, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch73, adc0

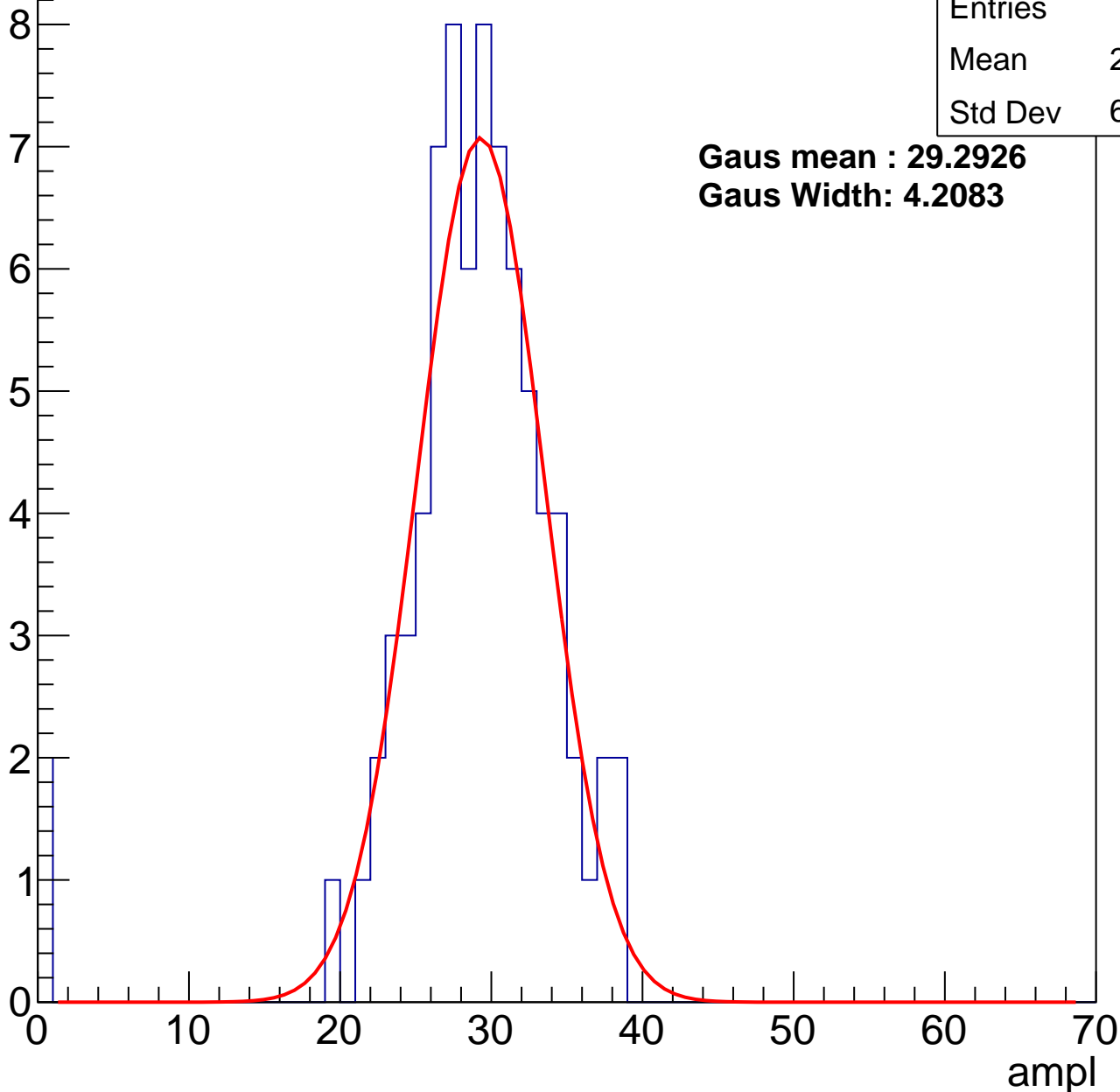
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	28.24
Std Dev	6.096

**Gaus mean : 29.2926**

**Gaus Width: 4.2083**



# B1L102S, U16-ch73, adc1

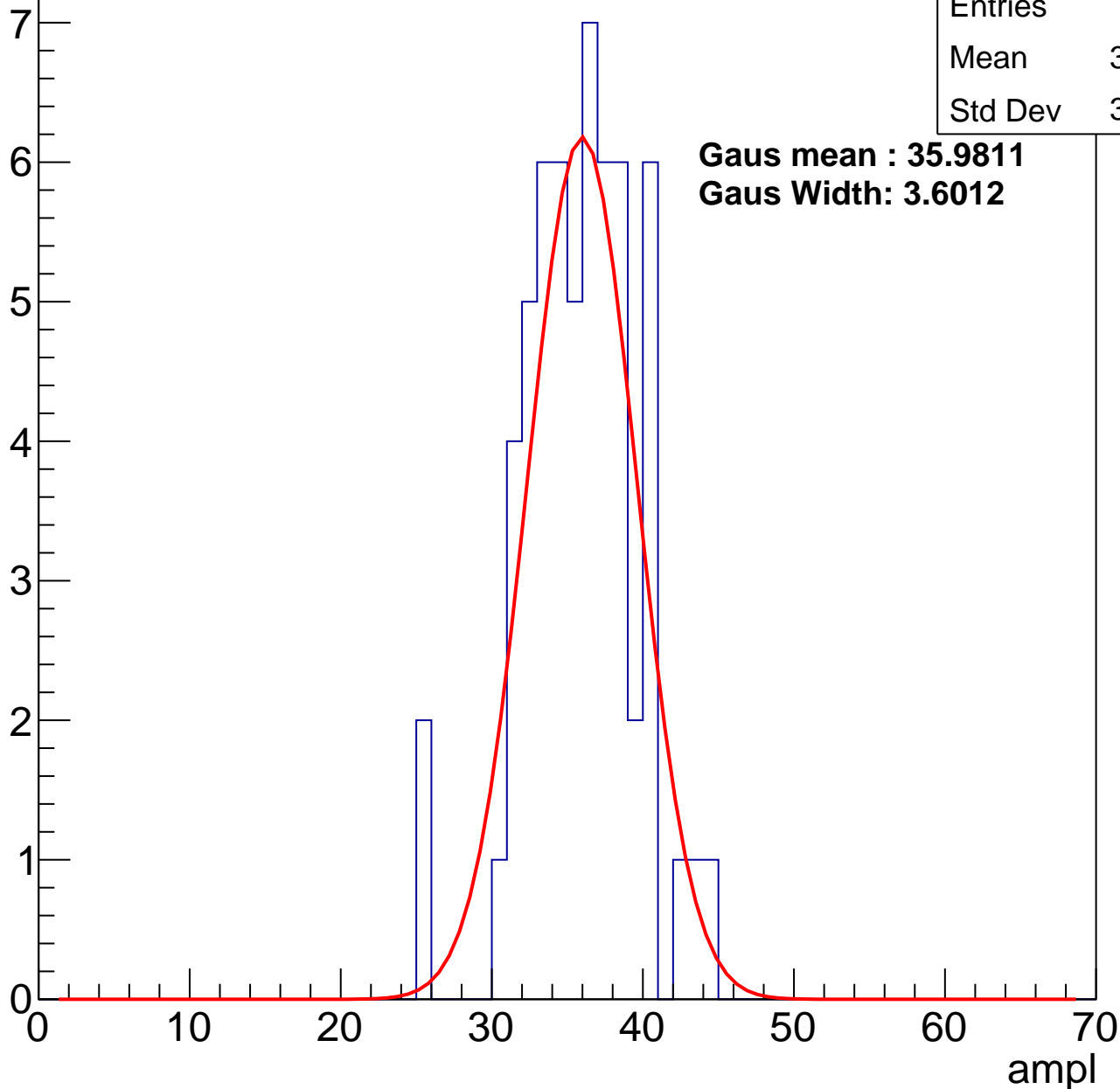
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	35.42
Std Dev	3.715

**Gaus mean : 35.9811**

**Gaus Width: 3.6012**



# B1L102S, U16-ch73, adc2

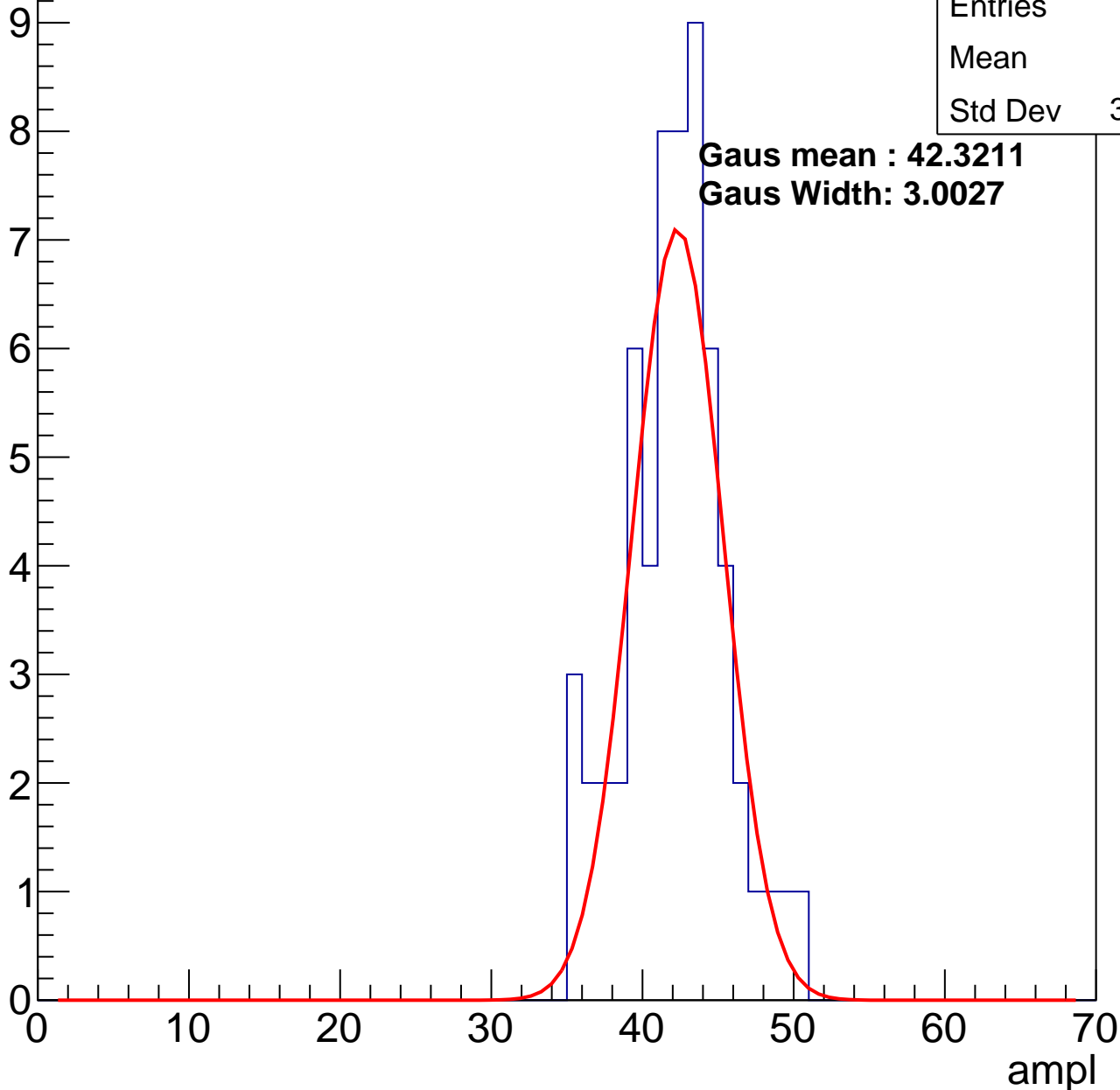
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	41.7
Std Dev	3.288

**Gaus mean : 42.3211**

**Gaus Width: 3.0027**

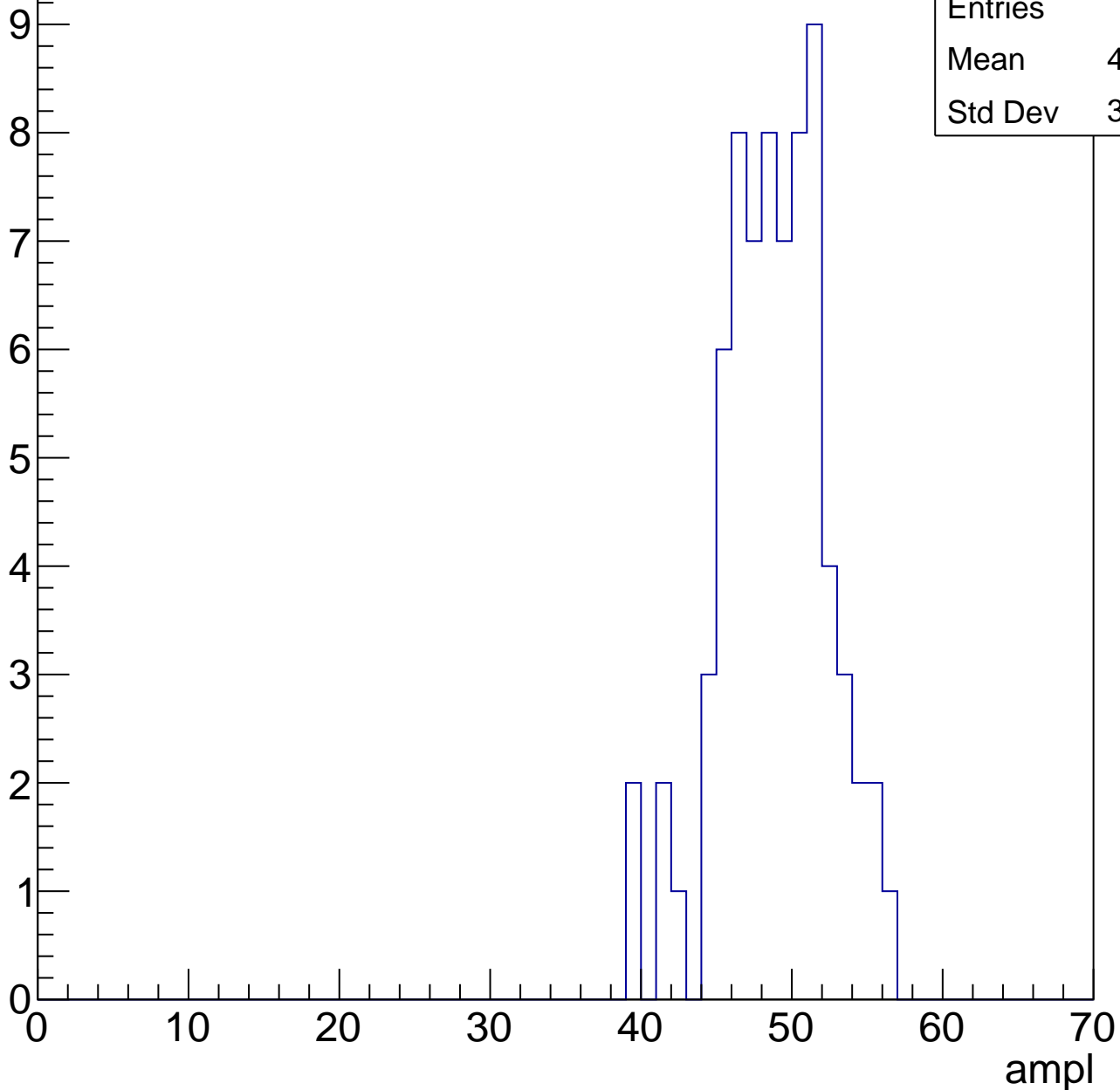


# B1L102S, U16-ch73, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	48.33
Std Dev	3.554

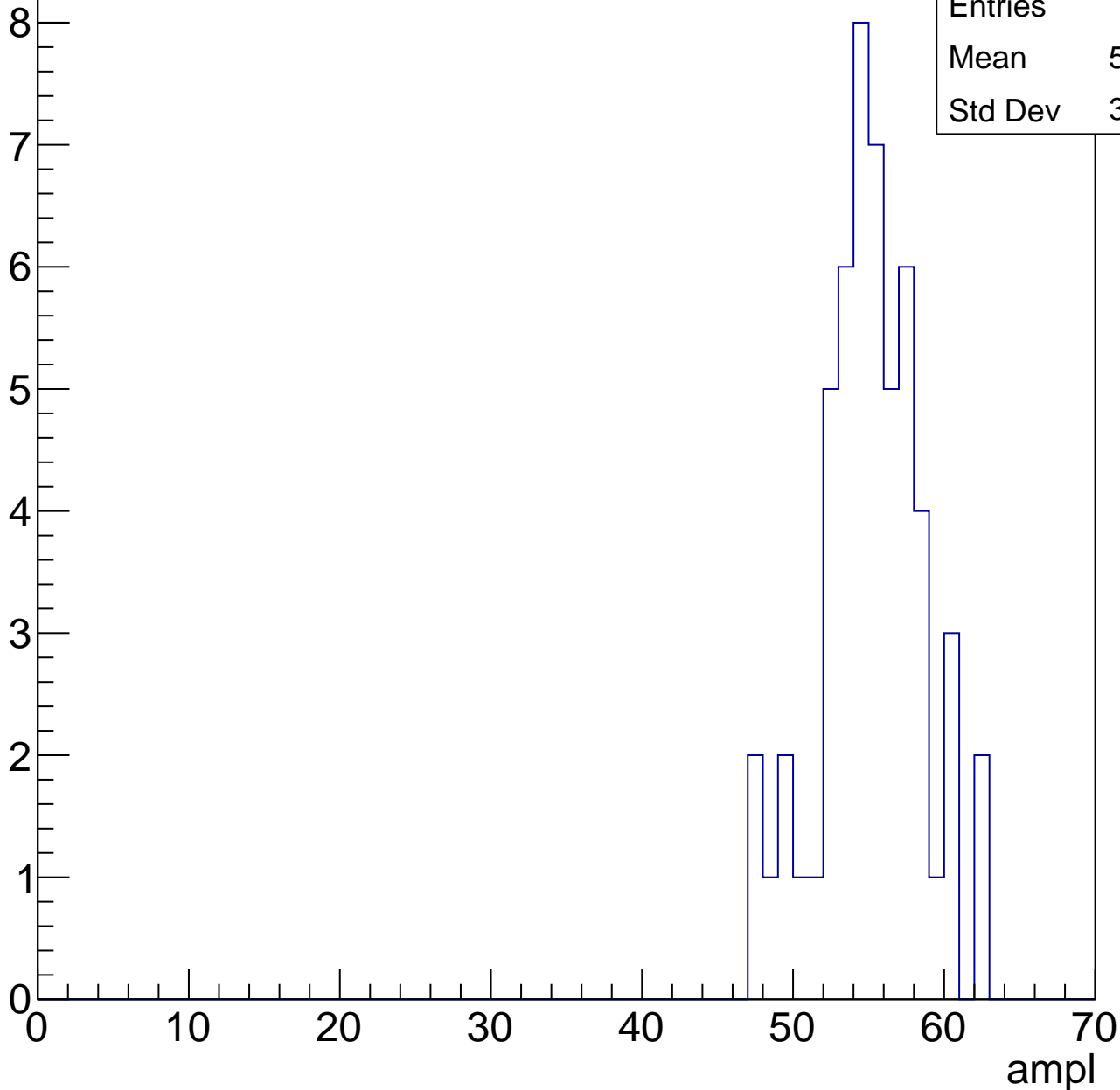


# B1L102S, U16-ch73, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	54.69
Std Dev	3.377



# B1L102S, U16-ch73, adc5

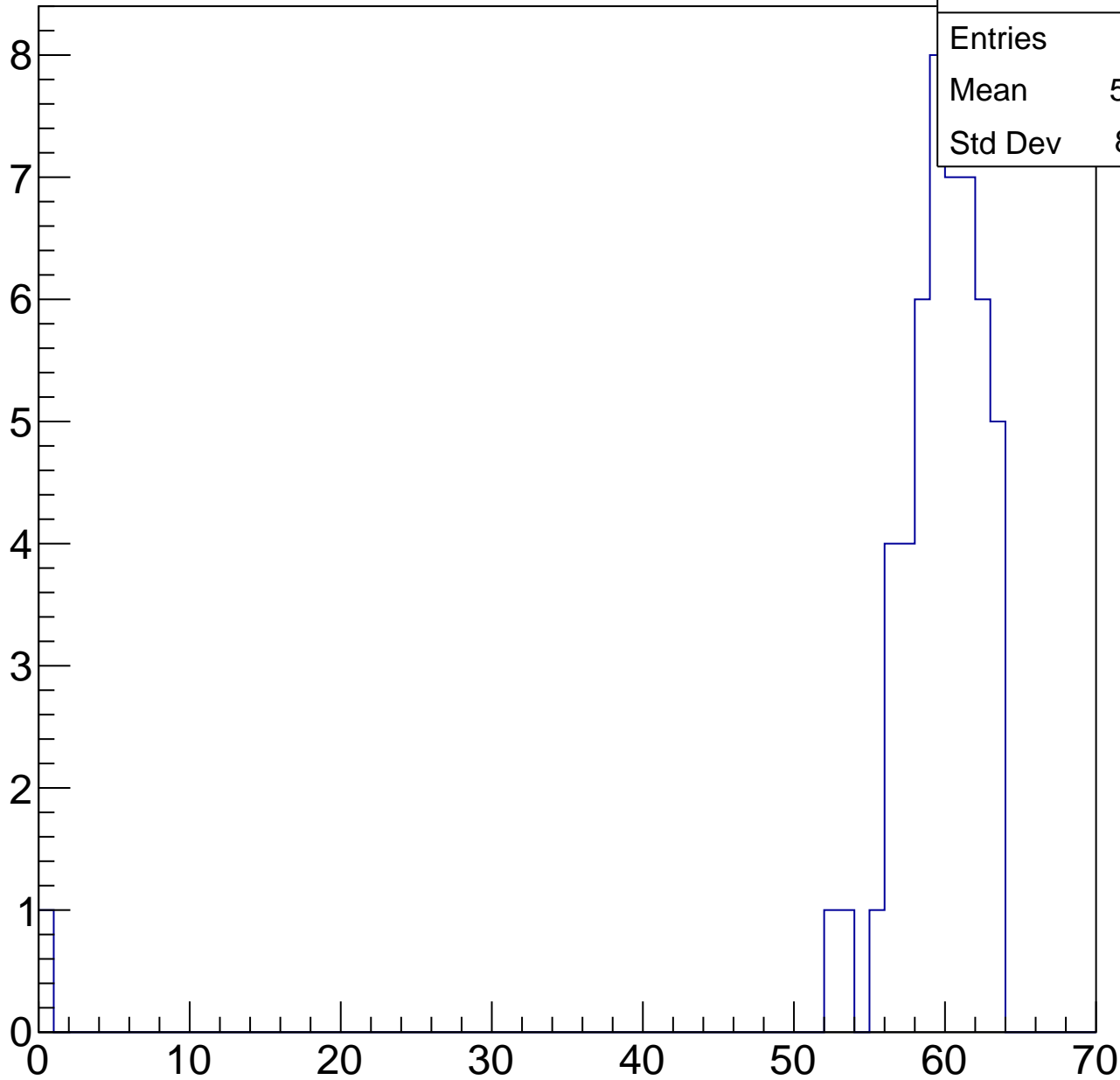
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	51
Mean	58.16
Std Dev	8.601

ampl

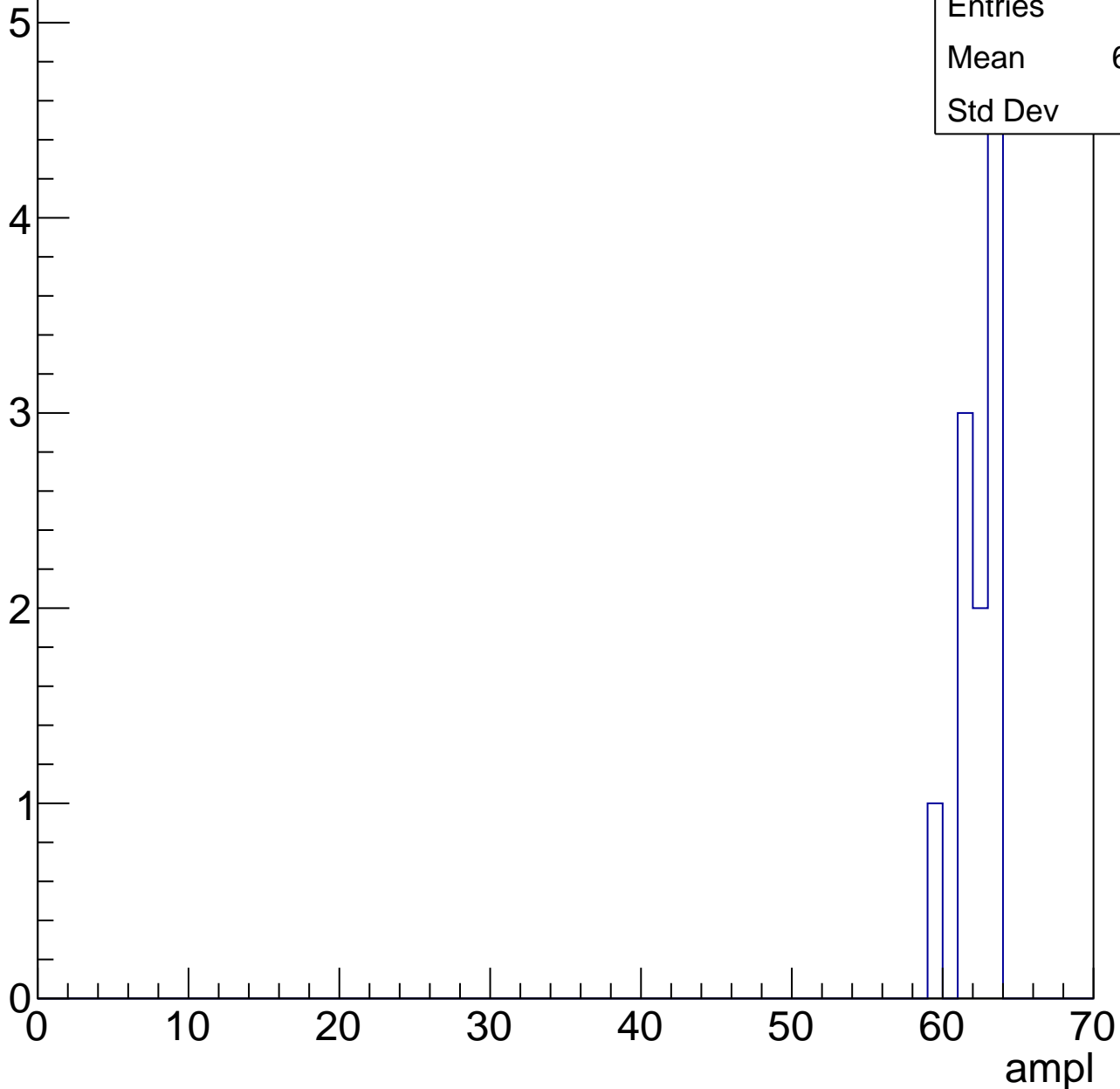


# B1L102S, U16-ch73, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	11
Mean	61.91
Std Dev	1.24





# B1L102S, U16-ch73, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch74, adc0

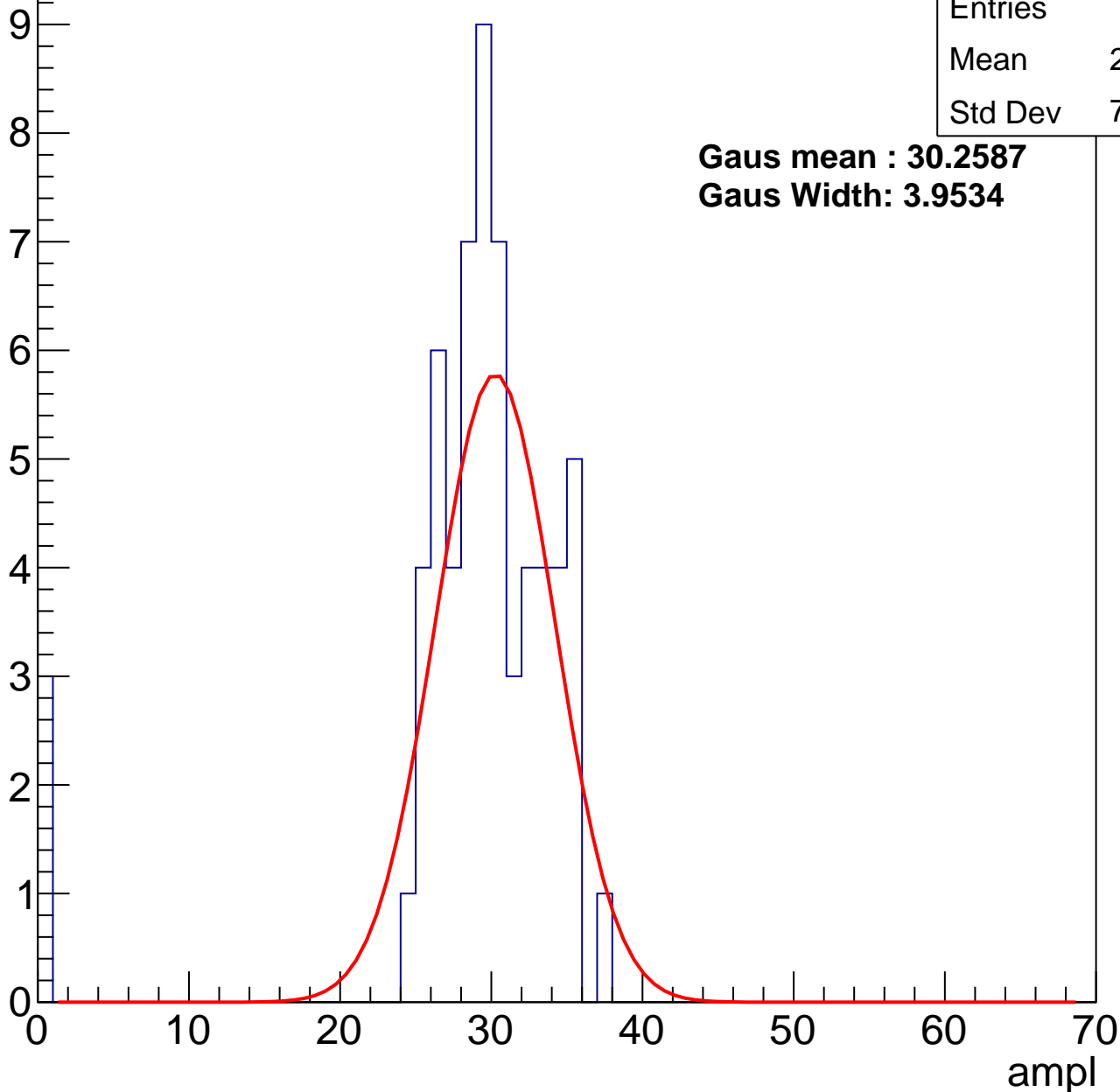
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	28.32
Std Dev	7.098

**Gaus mean : 30.2587**

**Gaus Width: 3.9534**



# B1L102S, U16-ch74, adc1

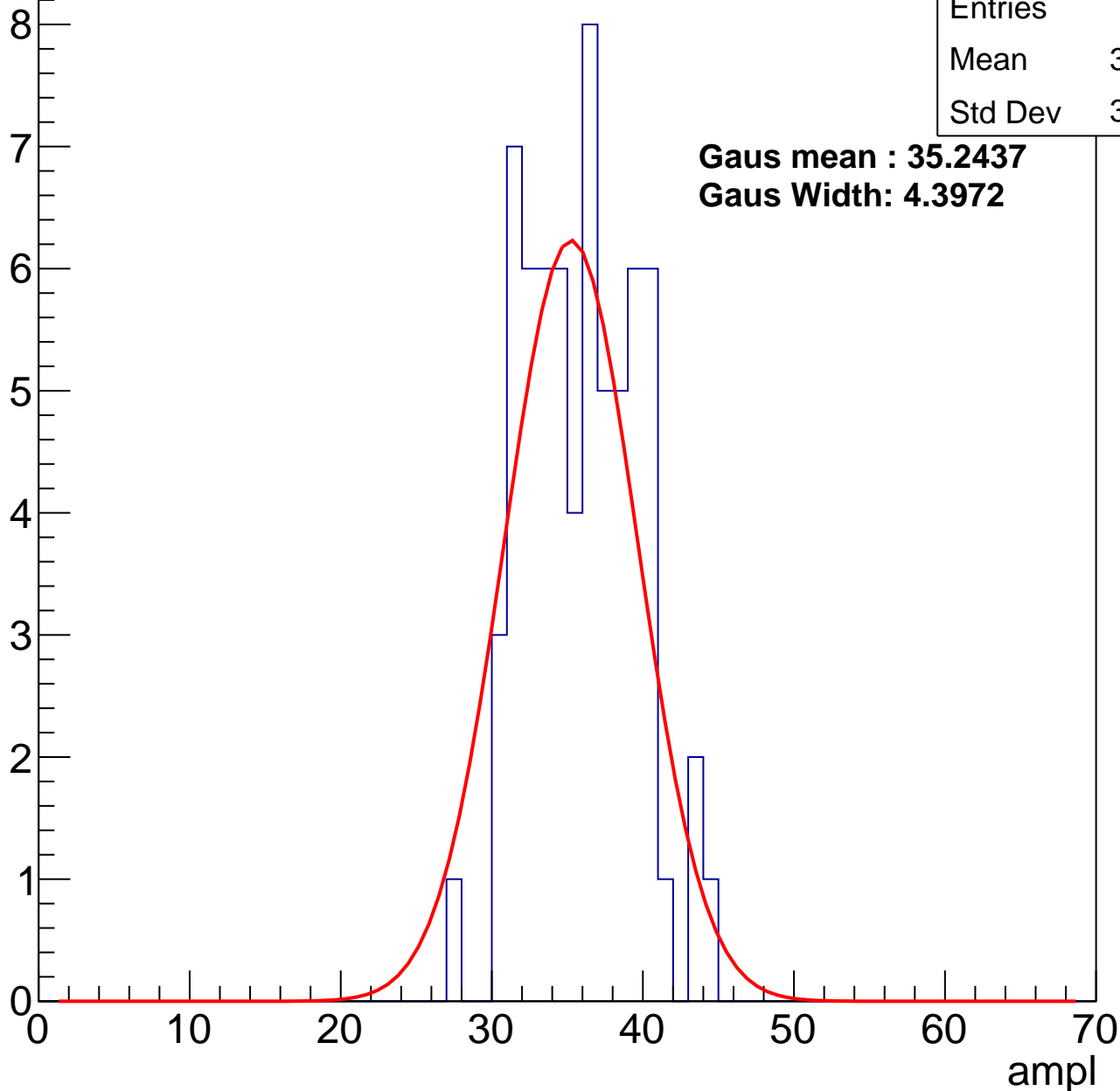
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	35.46
Std Dev	3.634

**Gaus mean : 35.2437**

**Gaus Width: 4.3972**



# B1L102S, U16-ch74, adc2

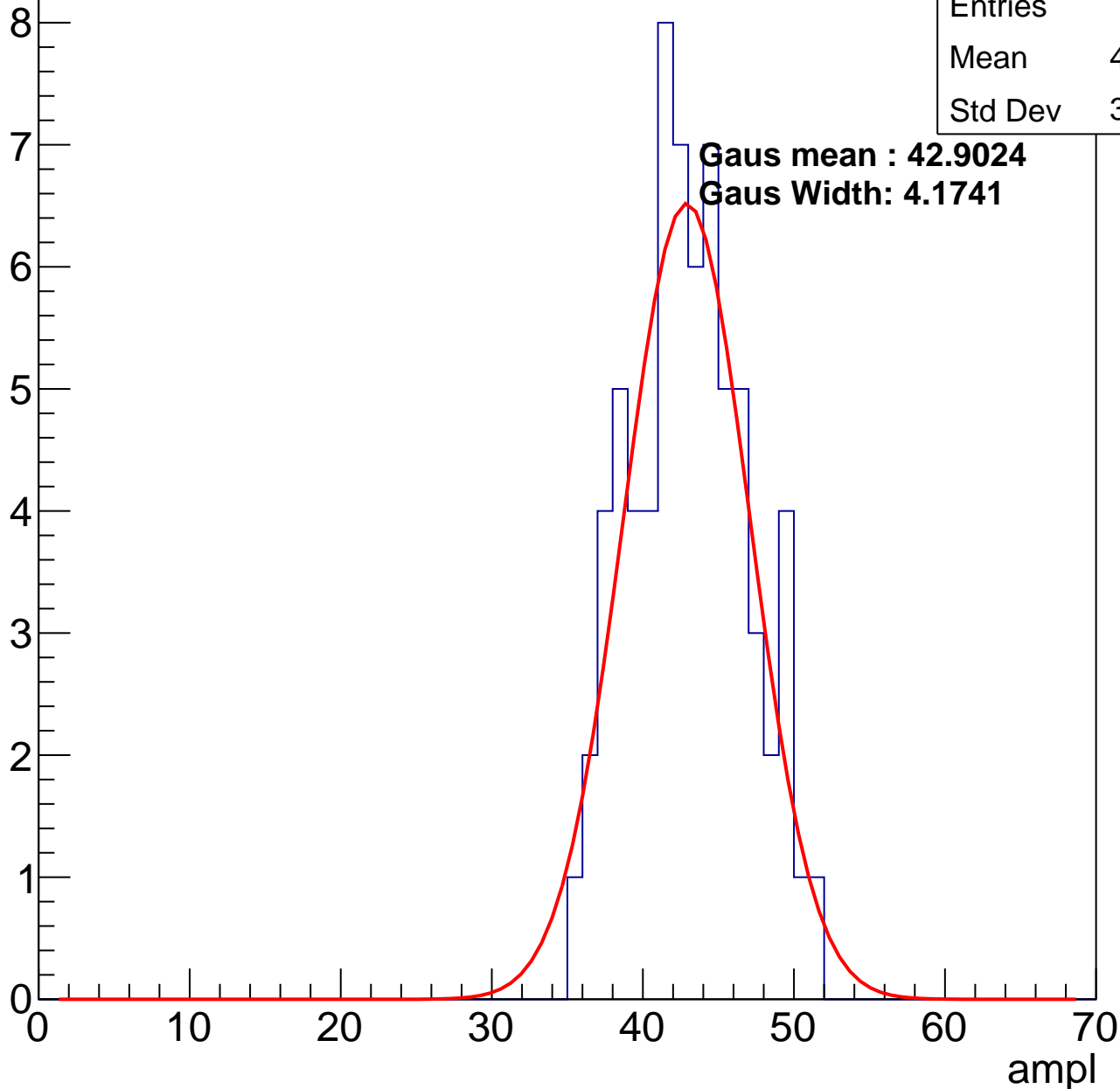
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	42.58
Std Dev	3.778

**Gaus mean : 42.9024**

**Gaus Width: 4.1741**

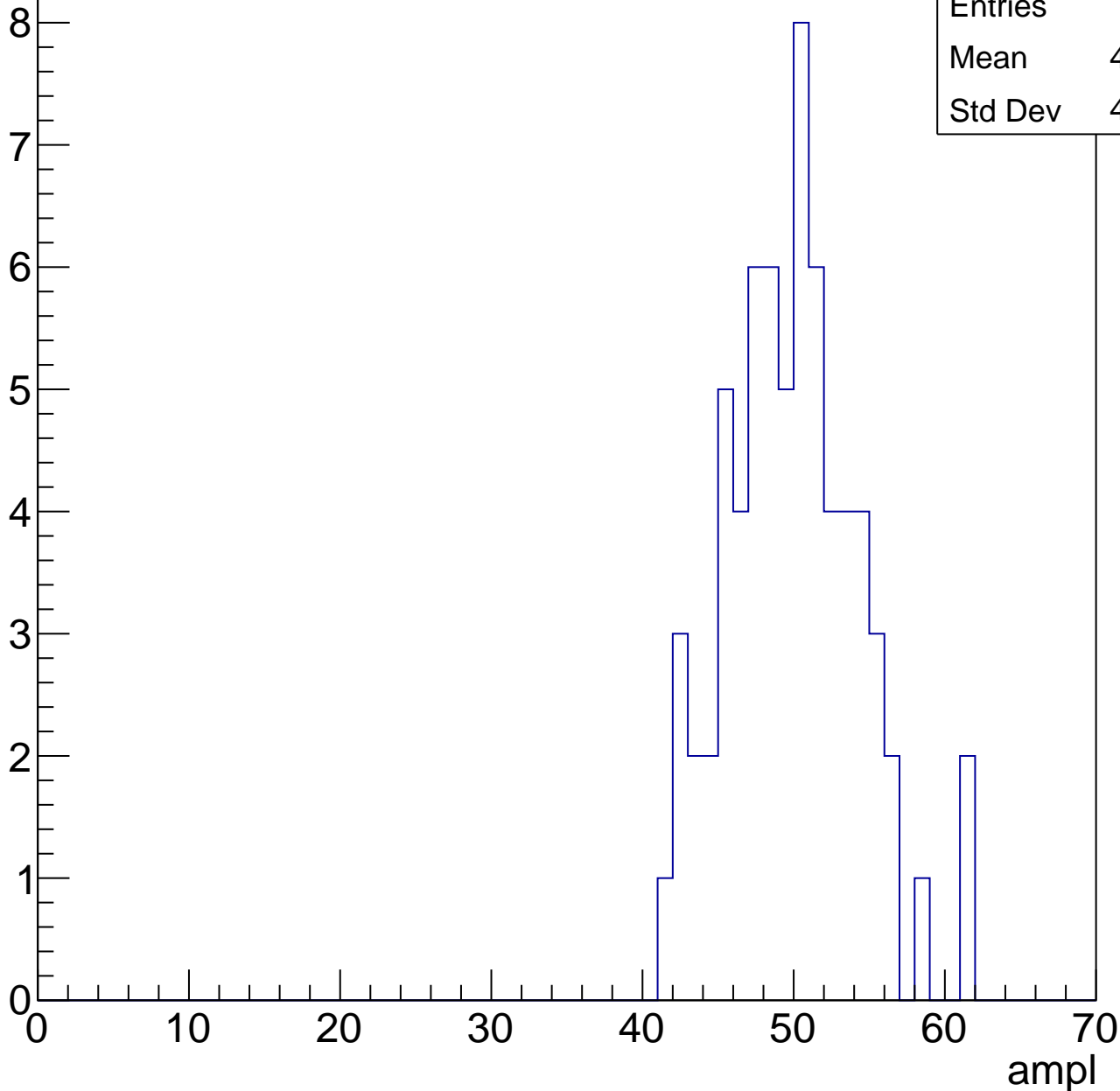


# B1L102S, U16-ch74, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	49.47
Std Dev	4.323

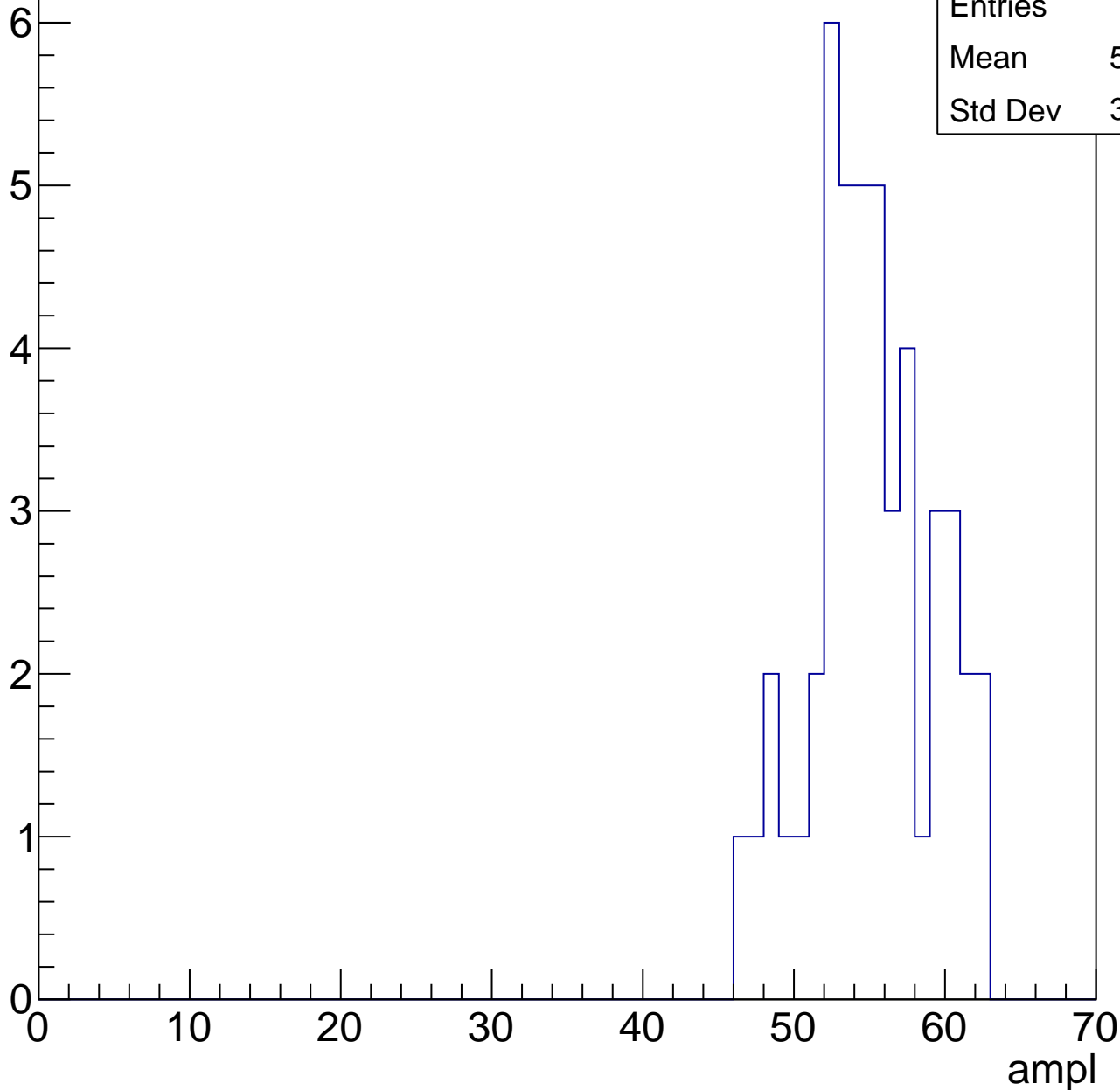


# B1L102S, U16-ch74, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	54.66
Std Dev	3.943



# B1L102S, U16-ch74, adc5

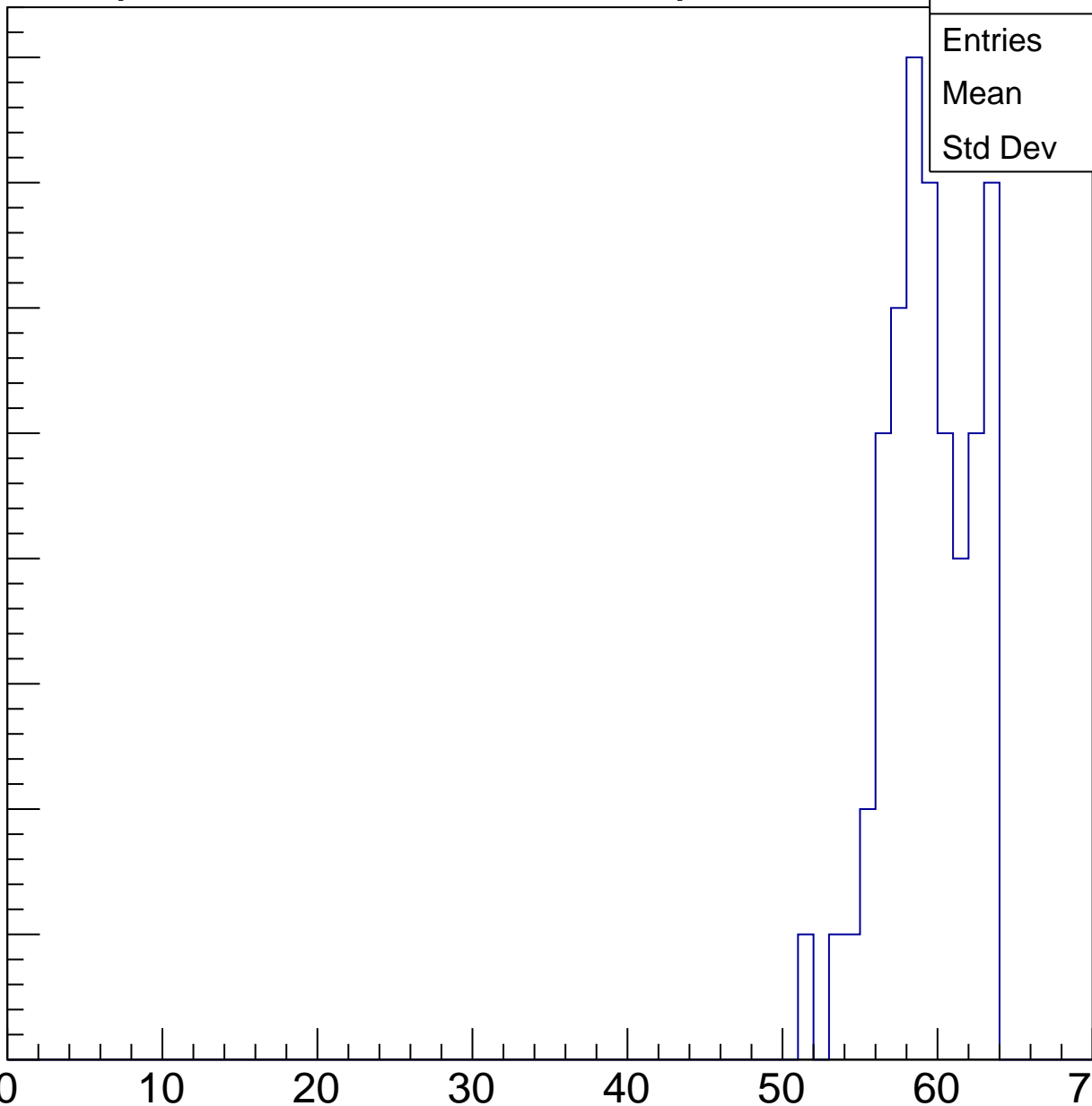
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	52
Mean	58.88
Std Dev	2.812

ampl



# B1L102S, U16-ch74, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3

2.5

2

1.5

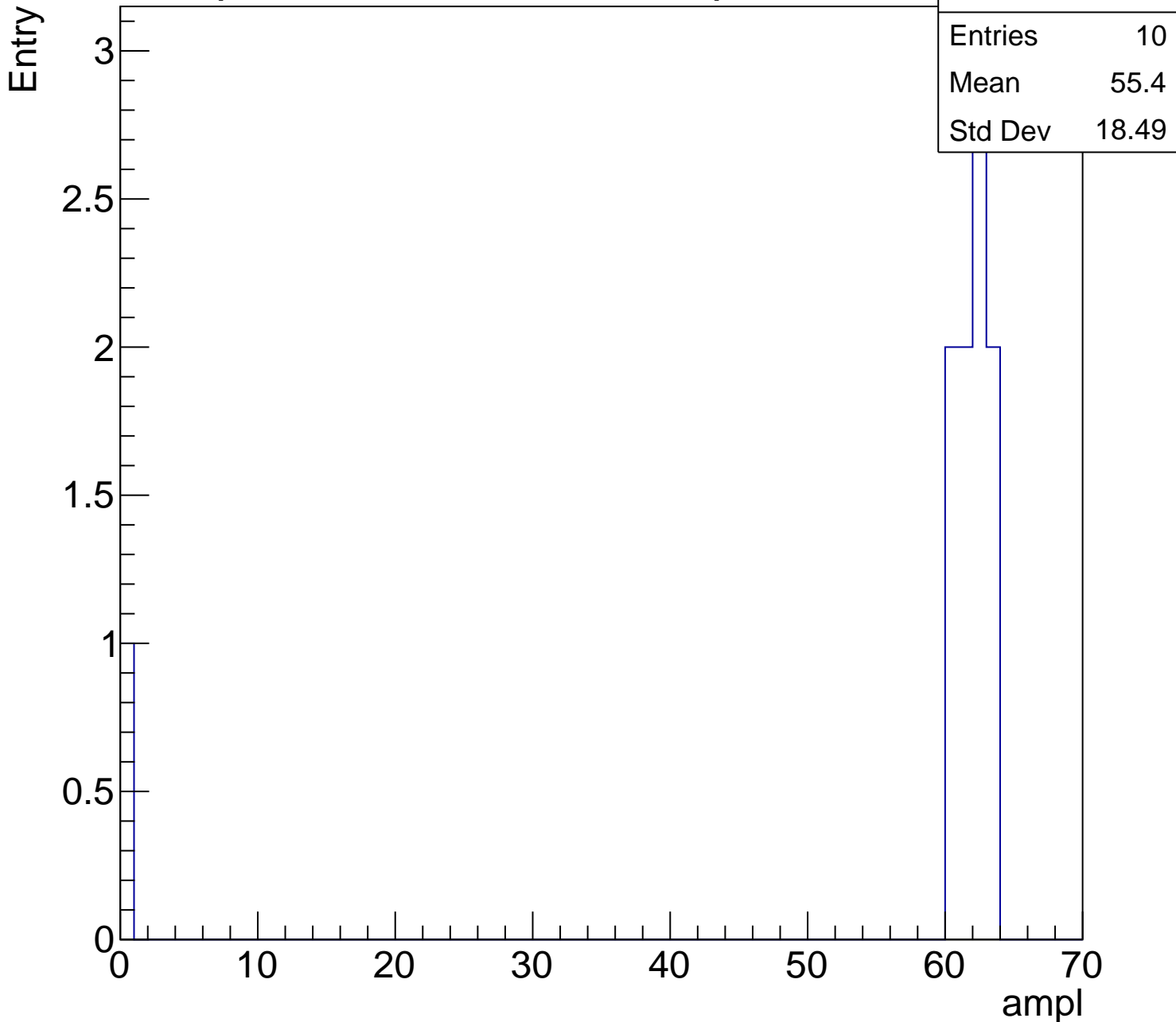
1

0.5

0

Entries	10
Mean	55.4
Std Dev	18.49

ampl





# B1L102S, U16-ch74, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch75, adc0

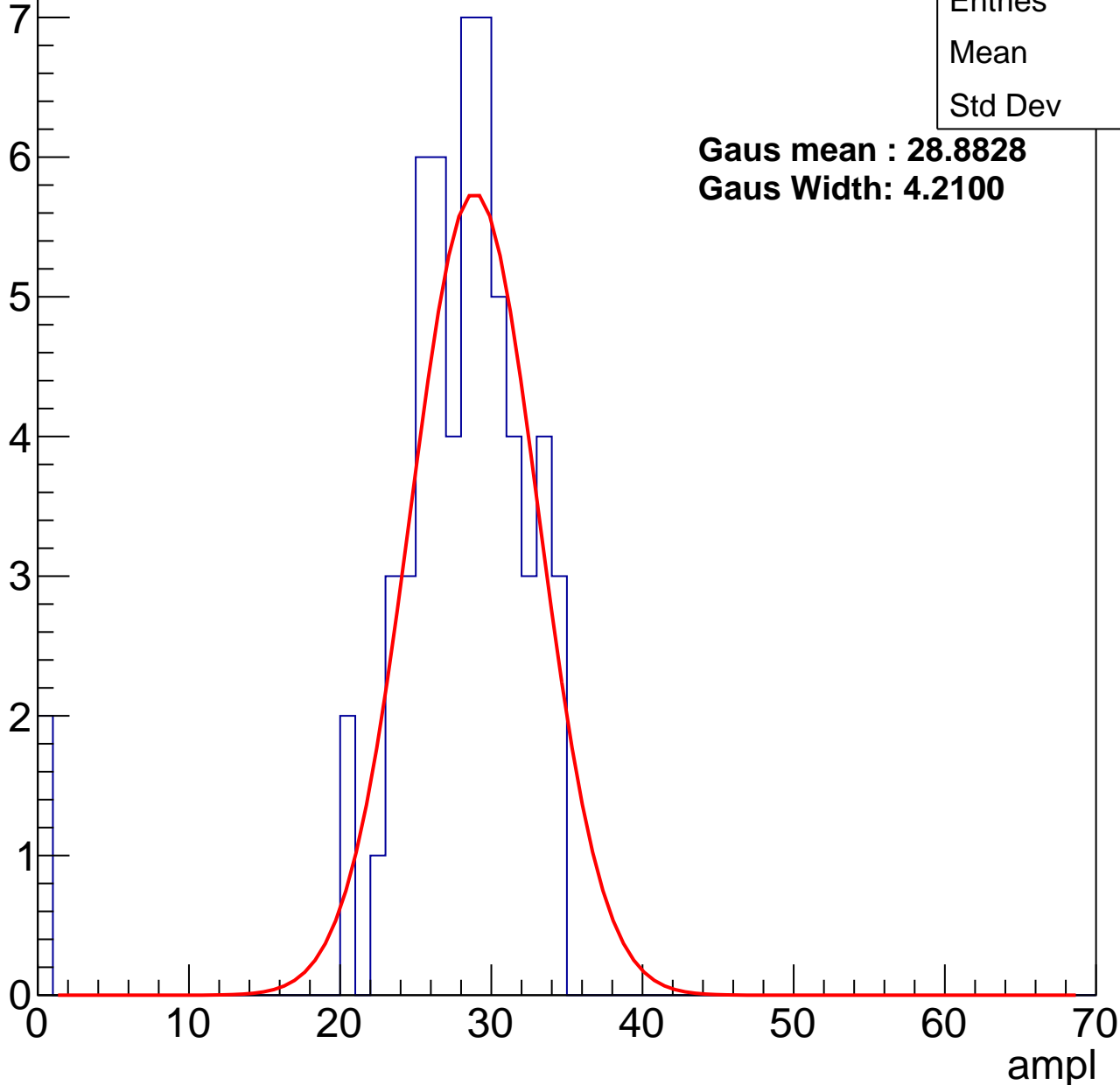
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	27
Std Dev	6.05

**Gaus mean : 28.8828**

**Gaus Width: 4.2100**



# B1L102S, U16-ch75, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	82
Mean	35.76
Std Dev	3.661

**Gaus mean : 35.8957**

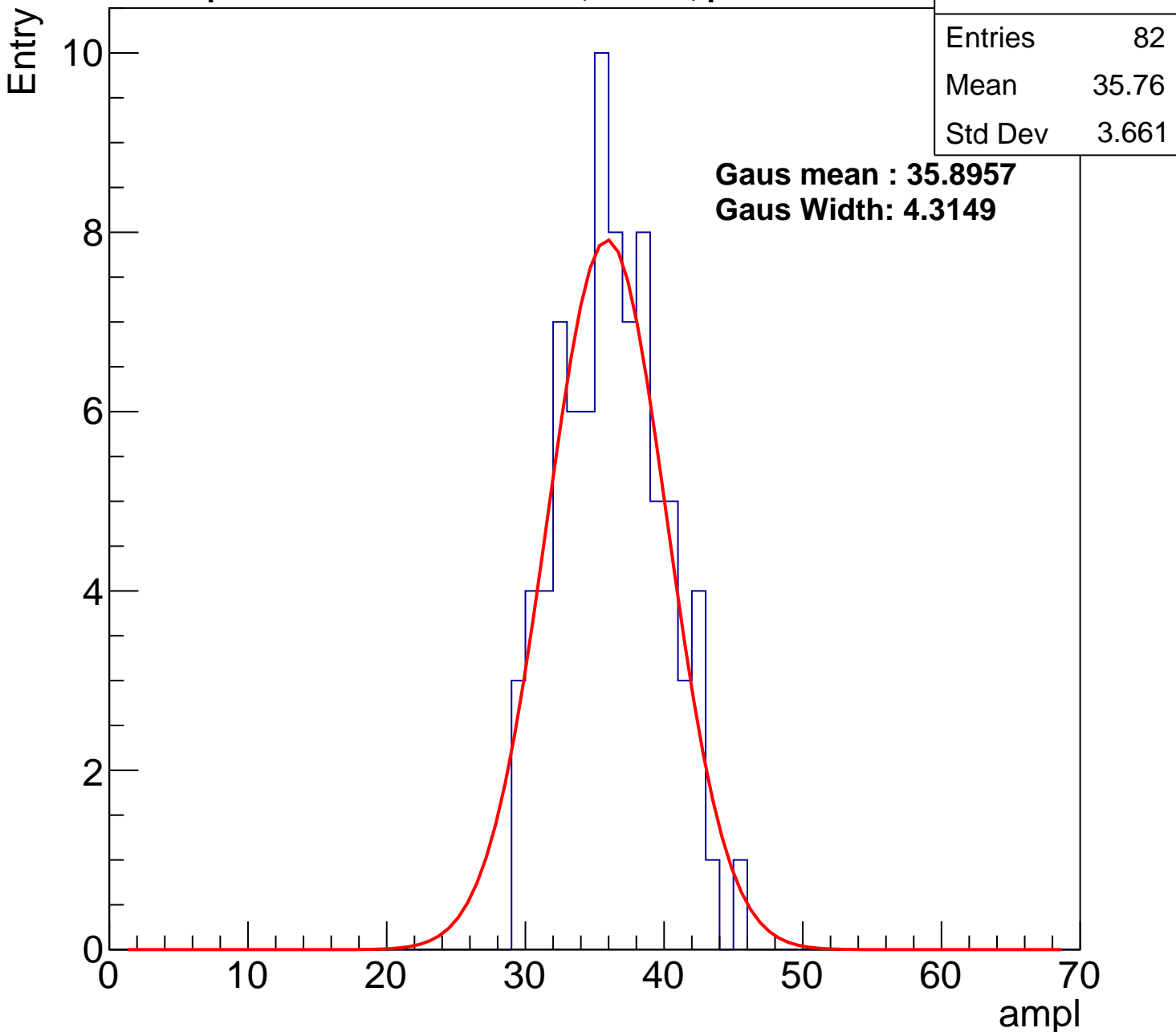
**Gaus Width: 4.3149**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U16-ch75, adc2

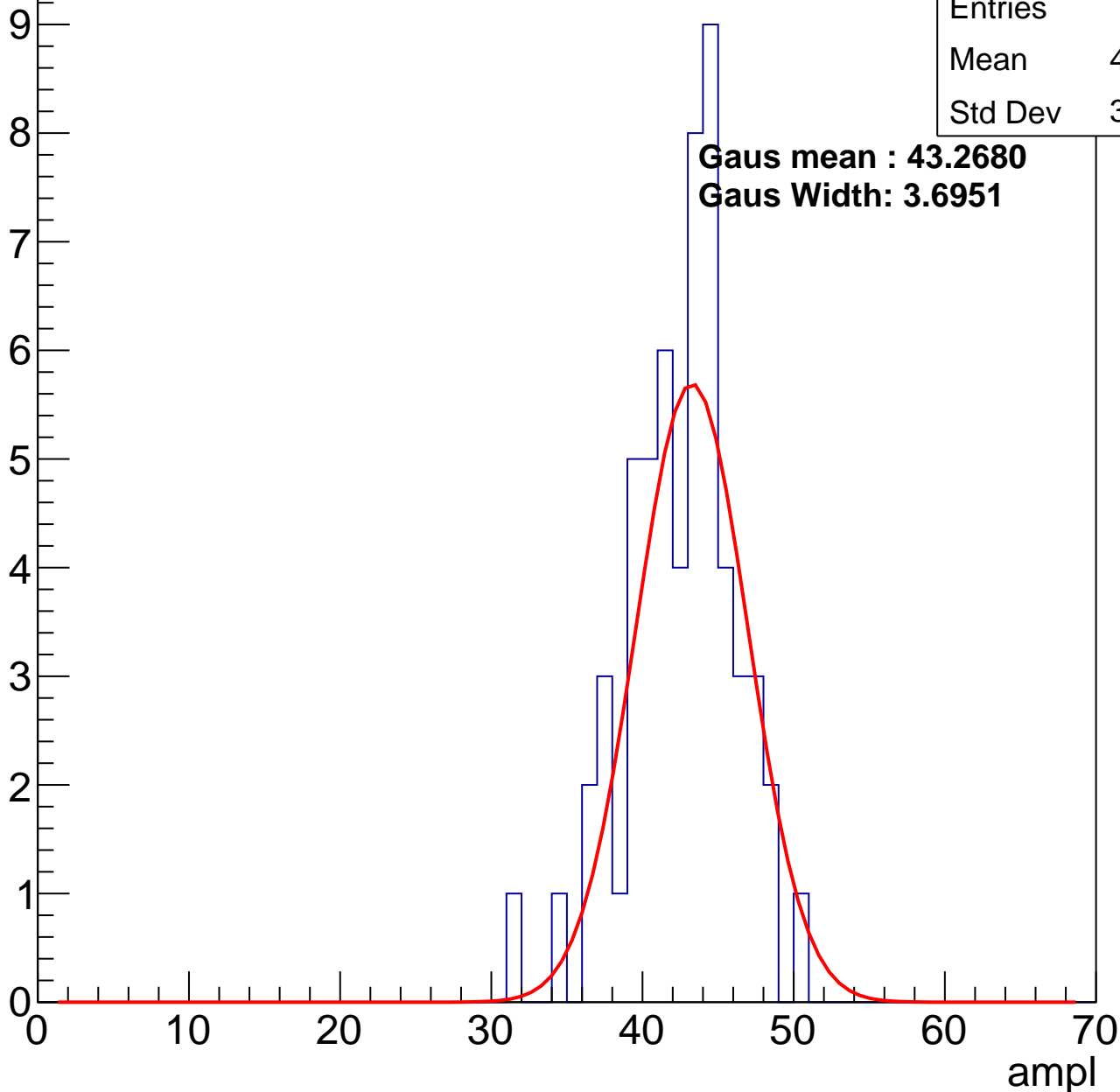
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	42.07
Std Dev	3.614

**Gaus mean : 43.2680**

**Gaus Width: 3.6951**

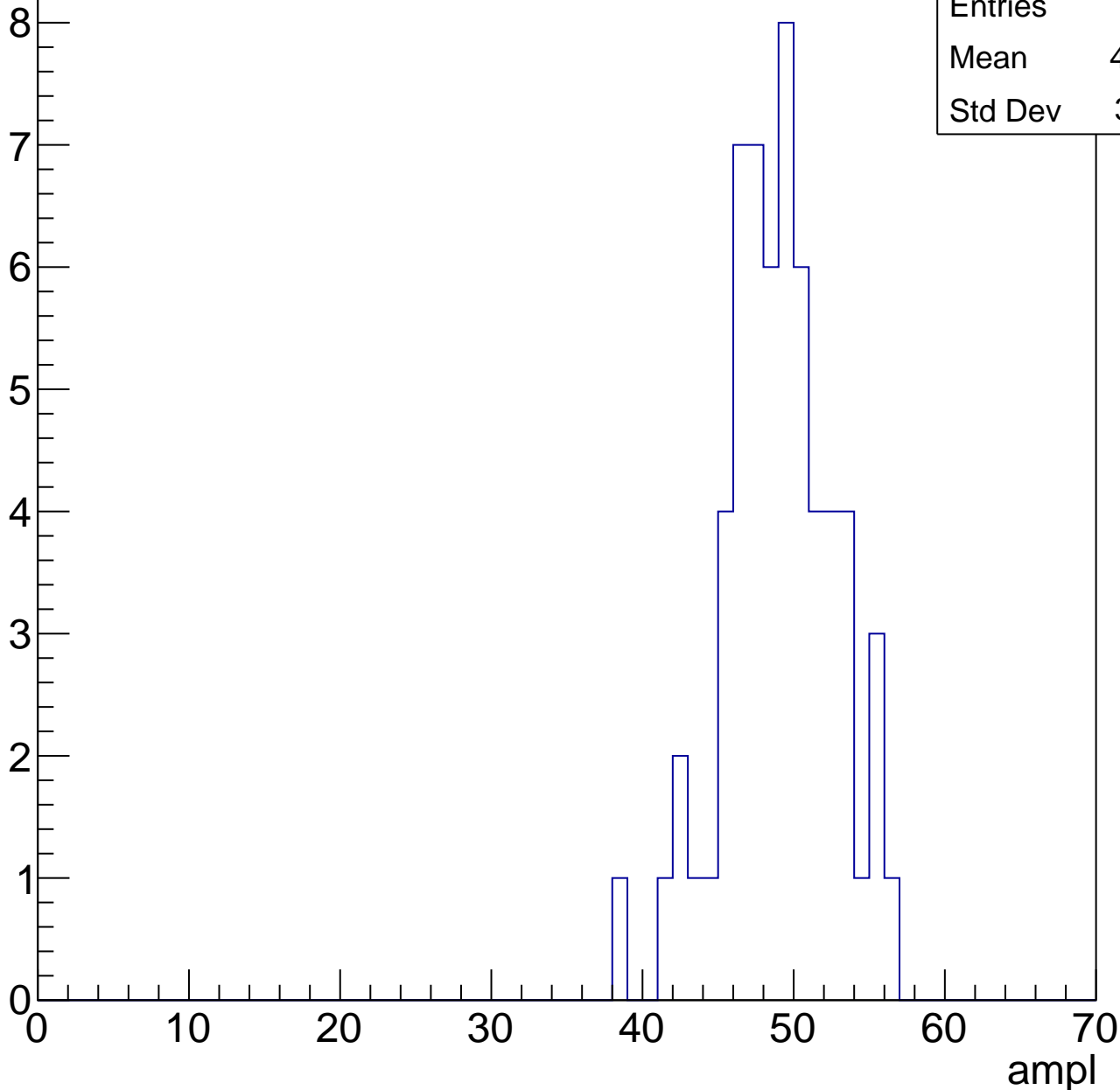


# B1L102S, U16-ch75, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	48.52
Std Dev	3.611

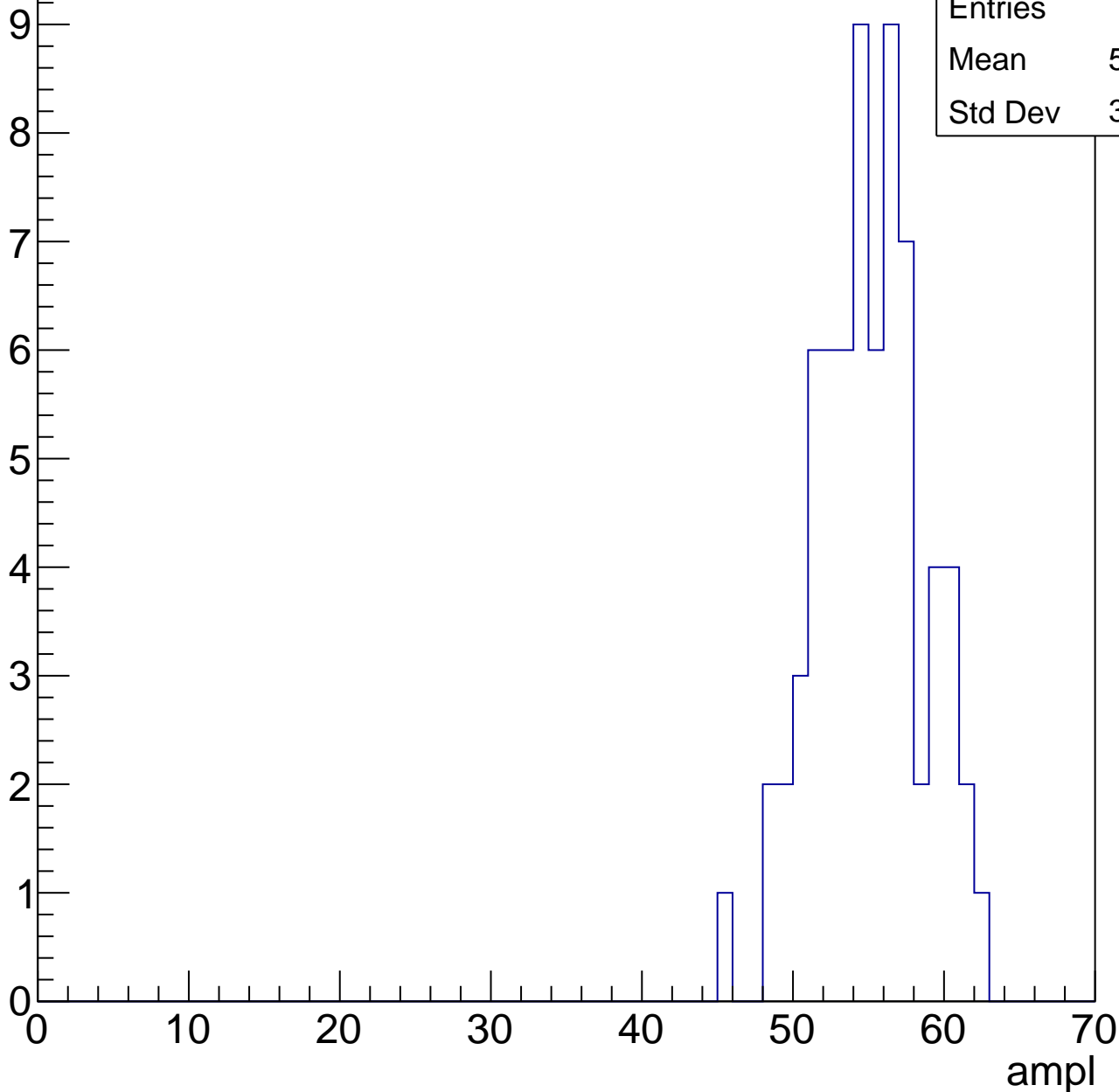


# B1L102S, U16-ch75, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	54.57
Std Dev	3.495

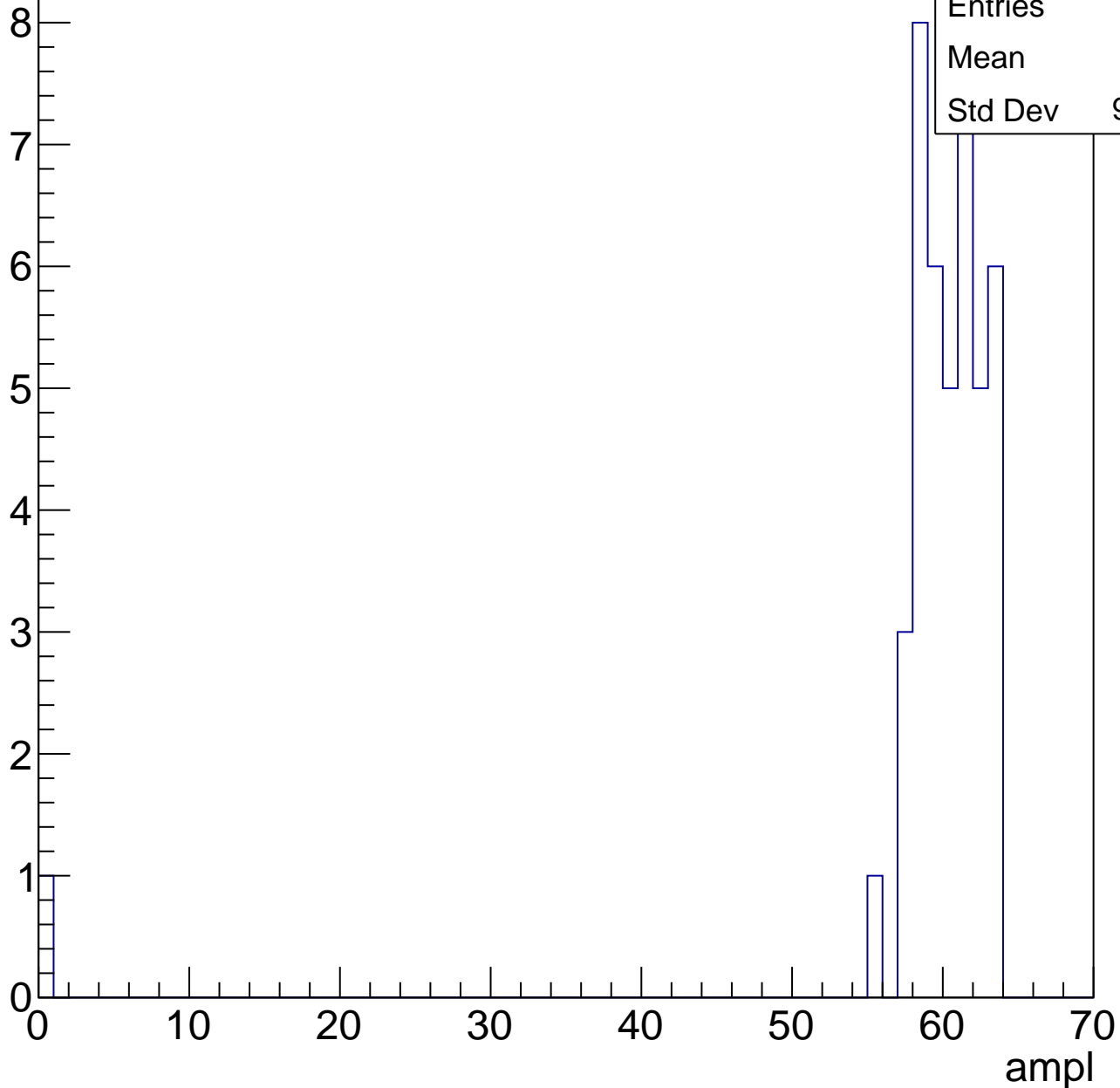


# B1L102S, U16-ch75, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

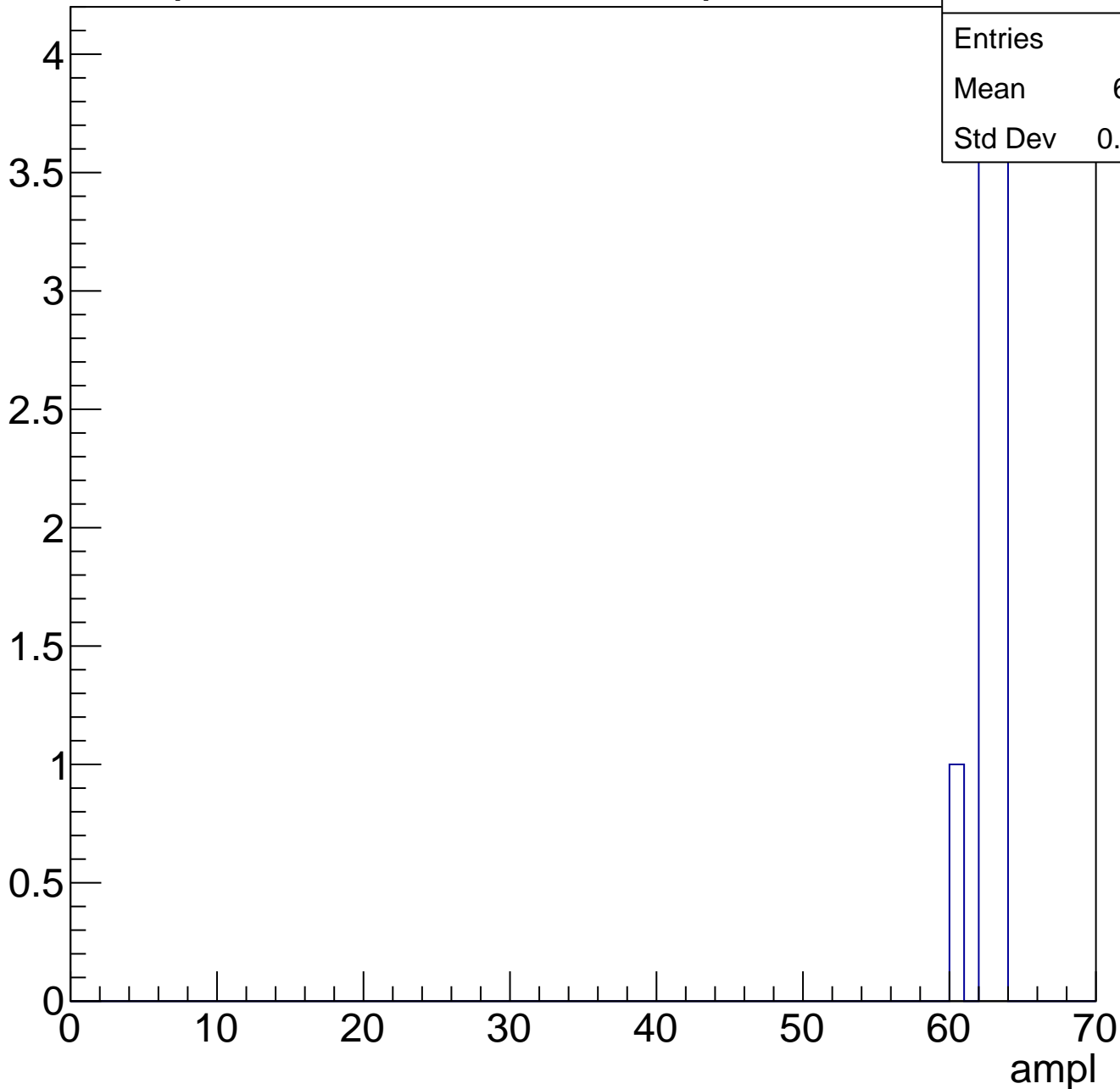
Entries	43
Mean	58.6
Std Dev	9.261



# B1L102S, U16-ch75, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch75, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U16-ch76, adc0

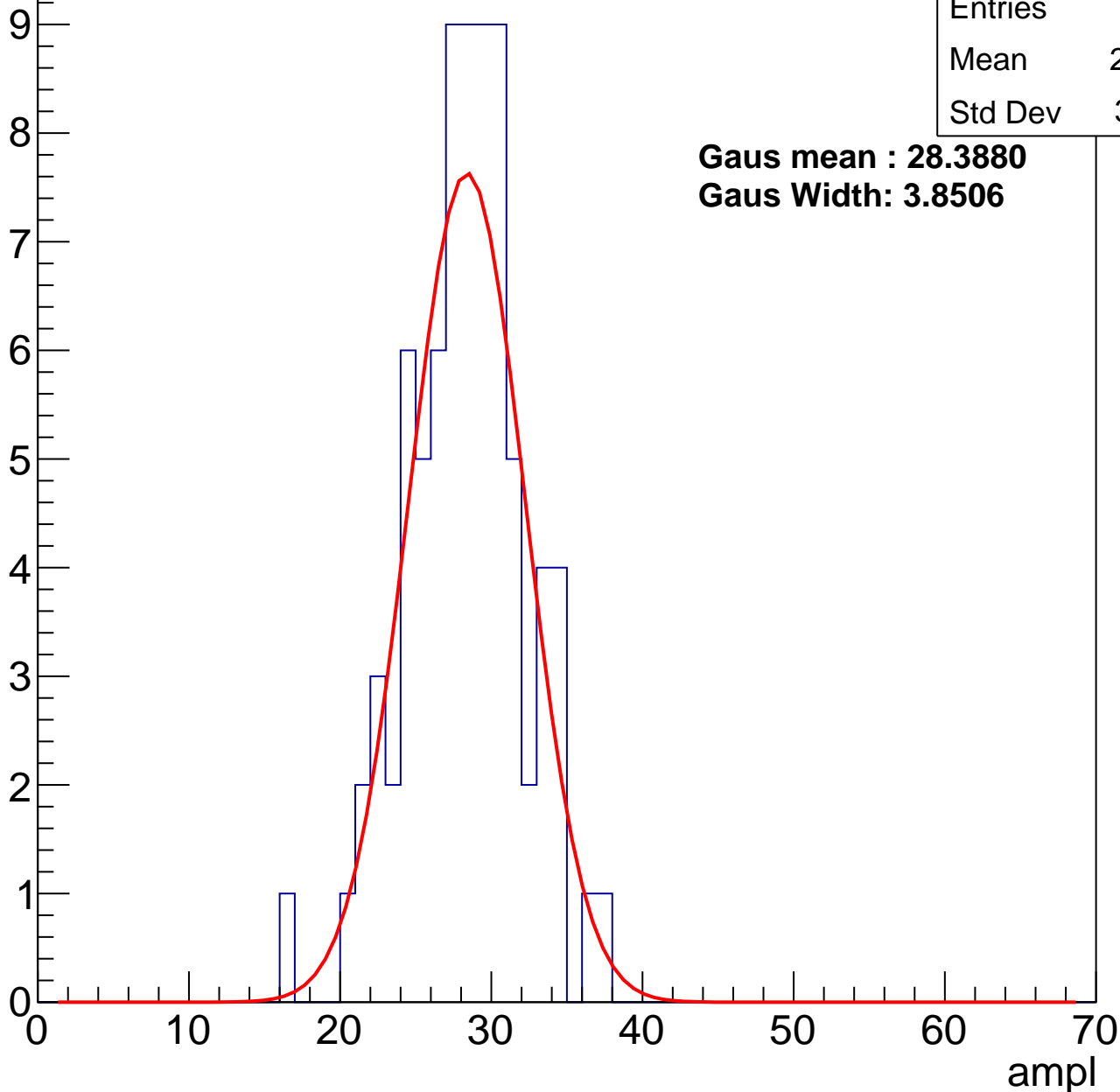
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	27.86
Std Dev	3.811

**Gaus mean : 28.3880**

**Gaus Width: 3.8506**



# B1L102S, U16-ch76, adc1

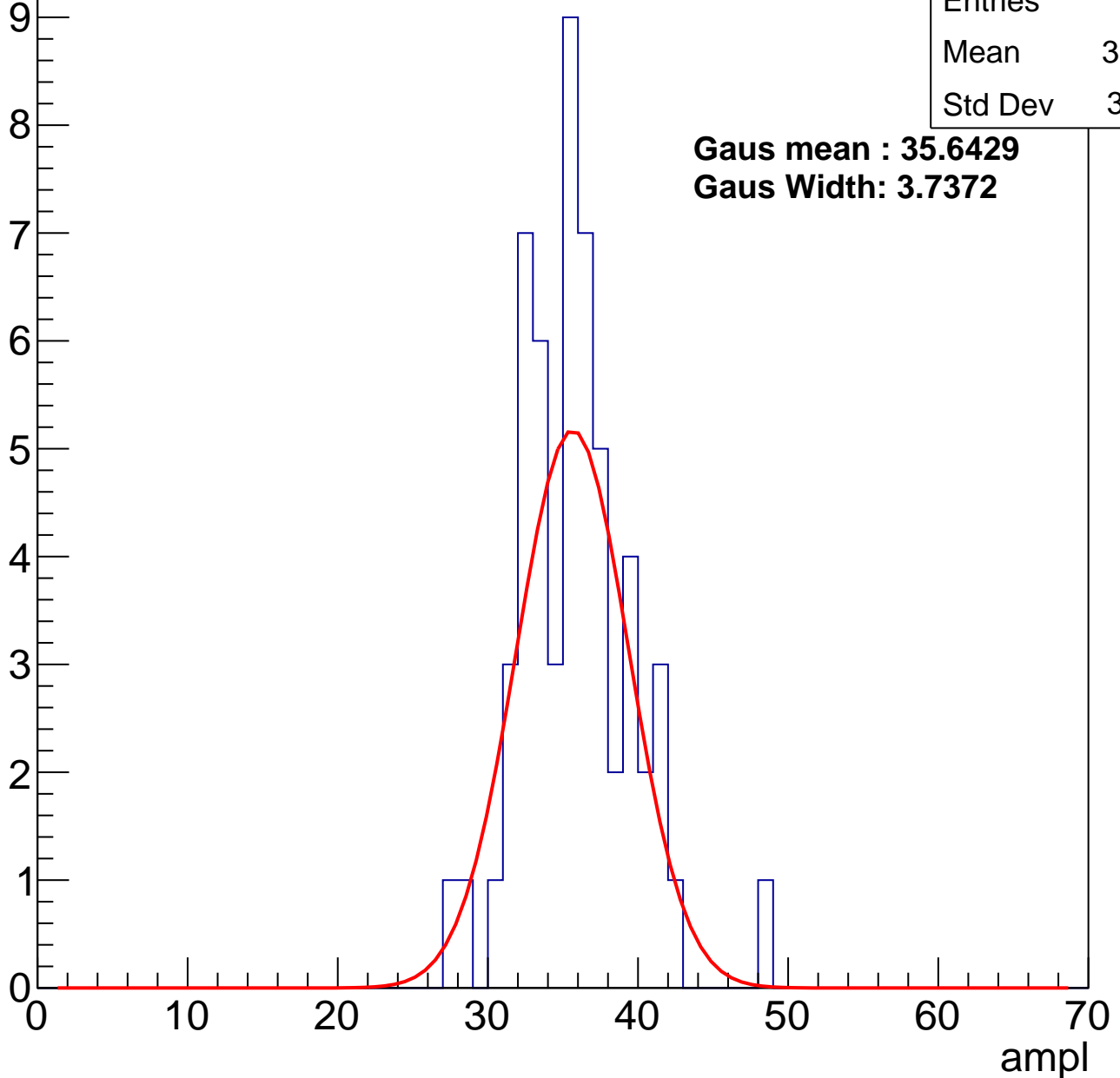
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	35.34
Std Dev	3.671

**Gaus mean : 35.6429**

**Gaus Width: 3.7372**



# B1L102S, U16-ch76, adc2

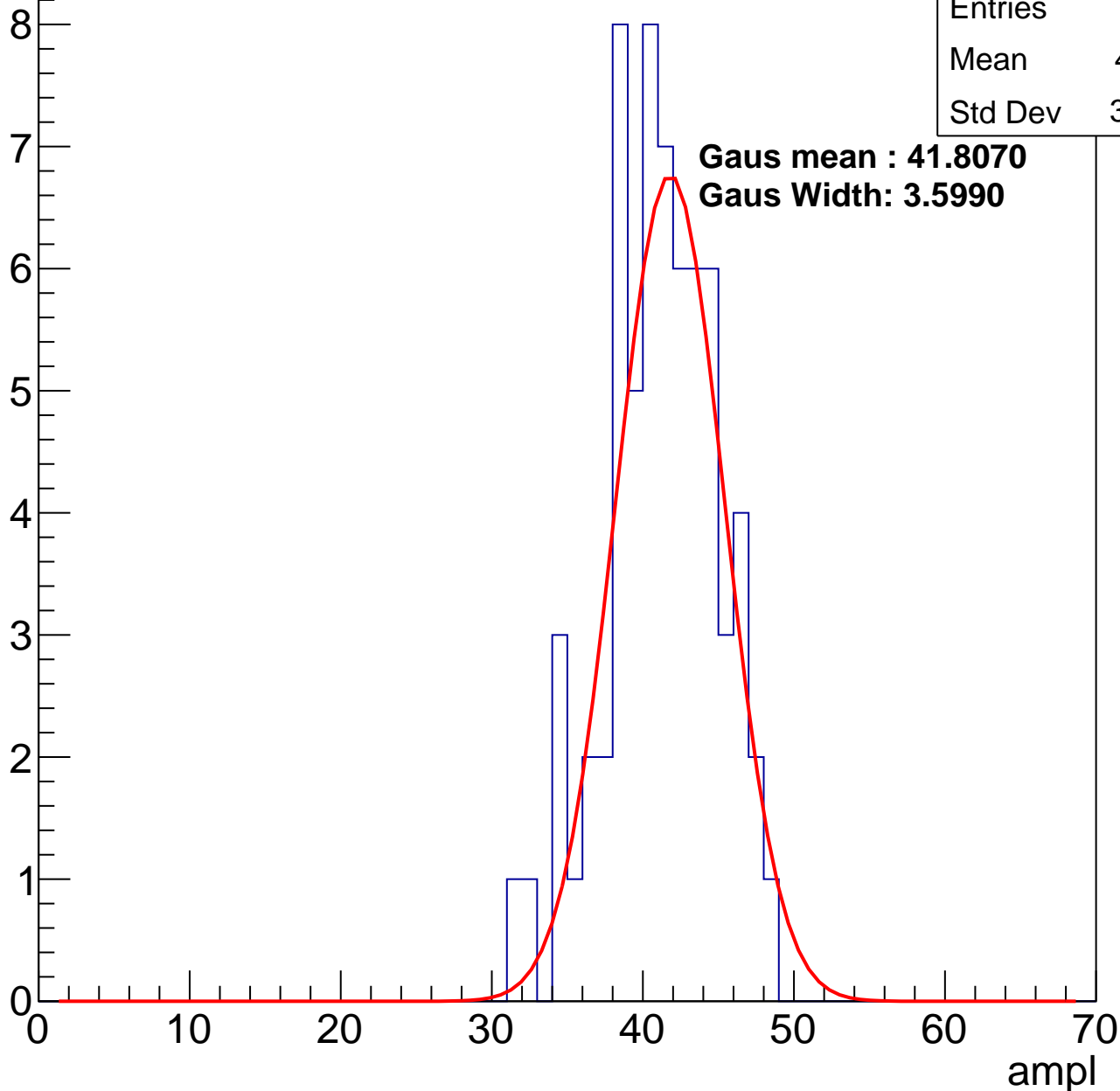
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	40.71
Std Dev	3.679

**Gaus mean : 41.8070**

**Gaus Width: 3.5990**

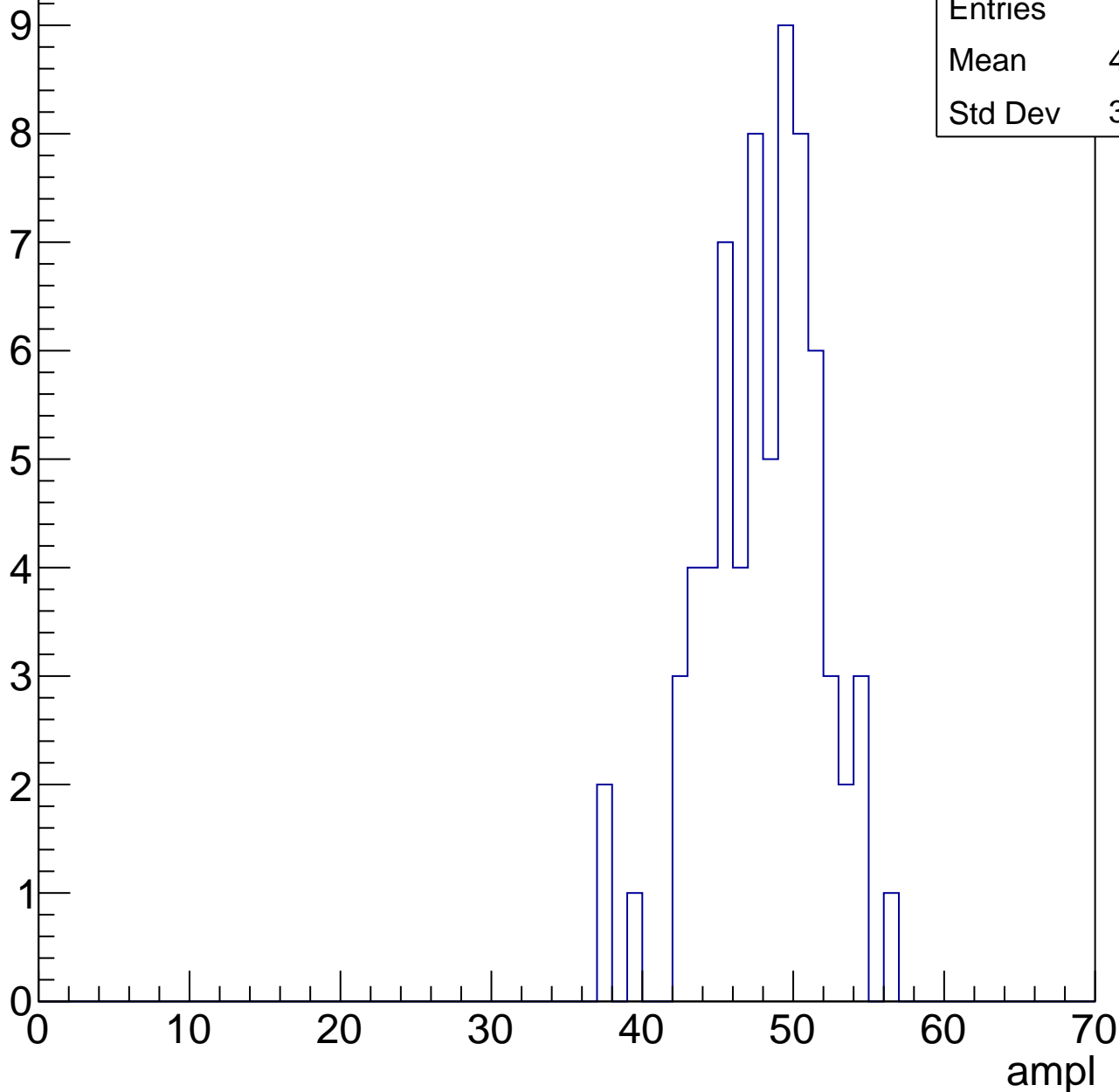


# B1L102S, U16-ch76, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	47.56
Std Dev	3.842

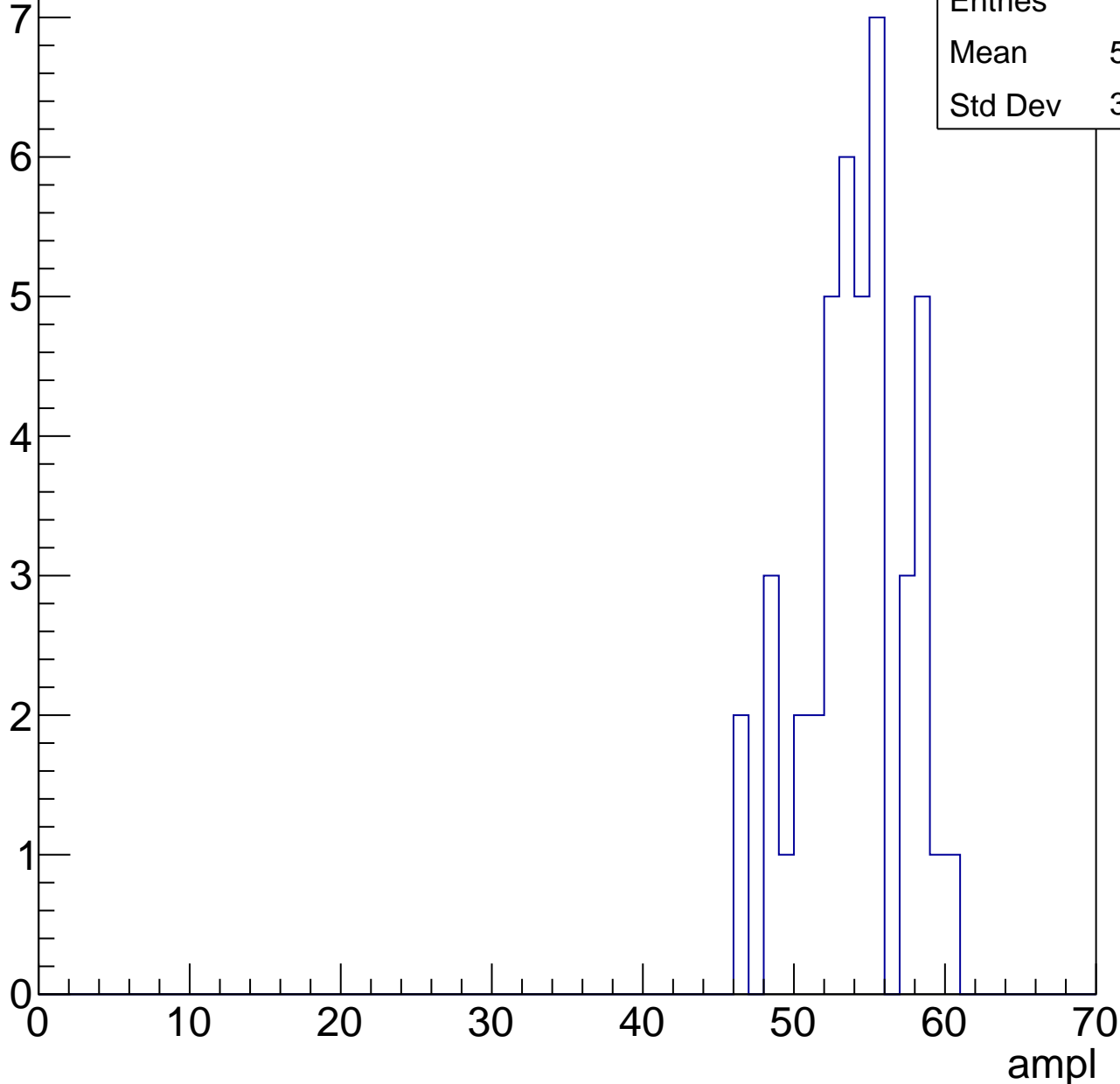


# B1L102S, U16-ch76, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

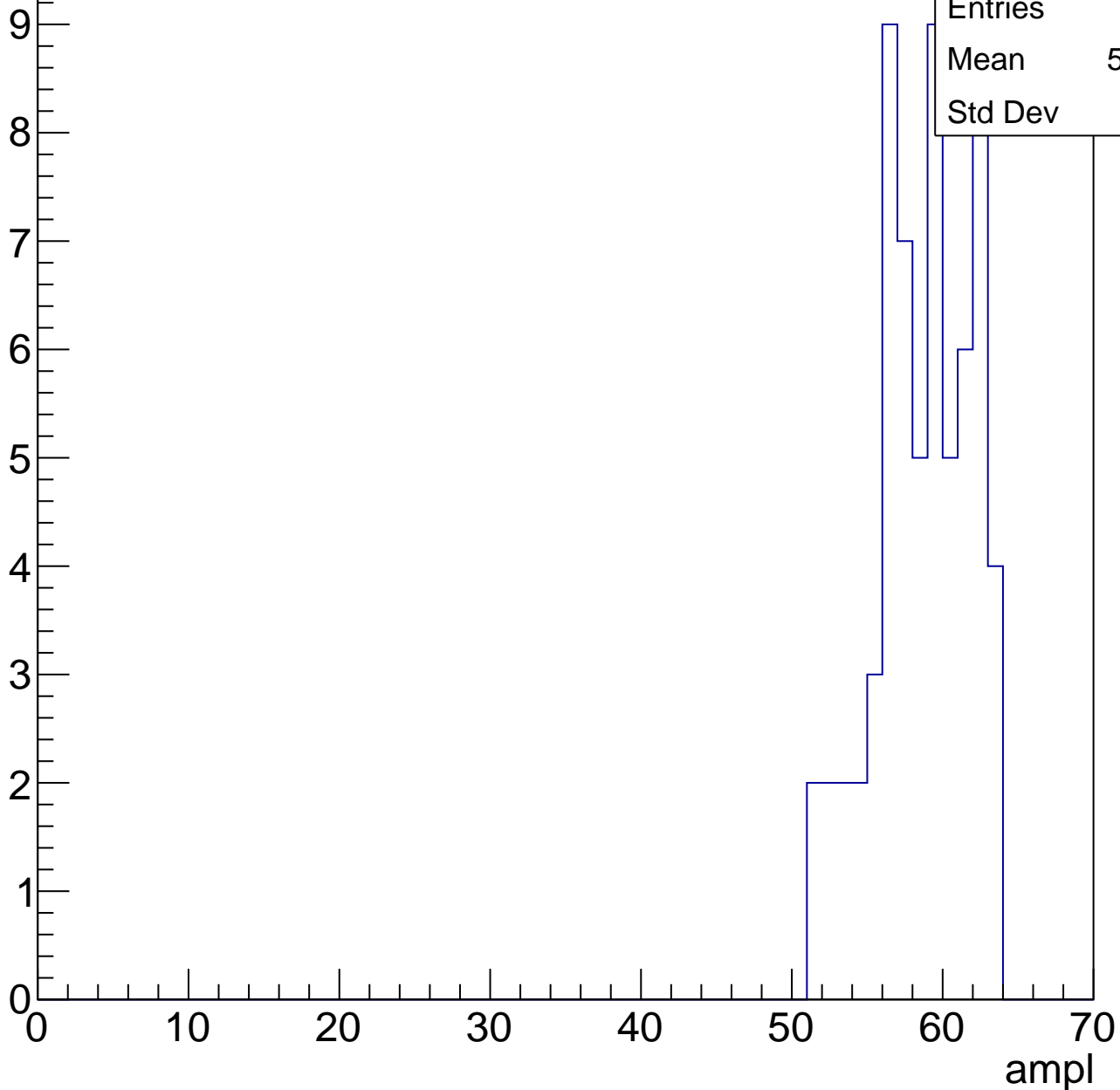
Entries	43
Mean	53.49
Std Dev	3.413



# B1L102S, U16-ch76, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



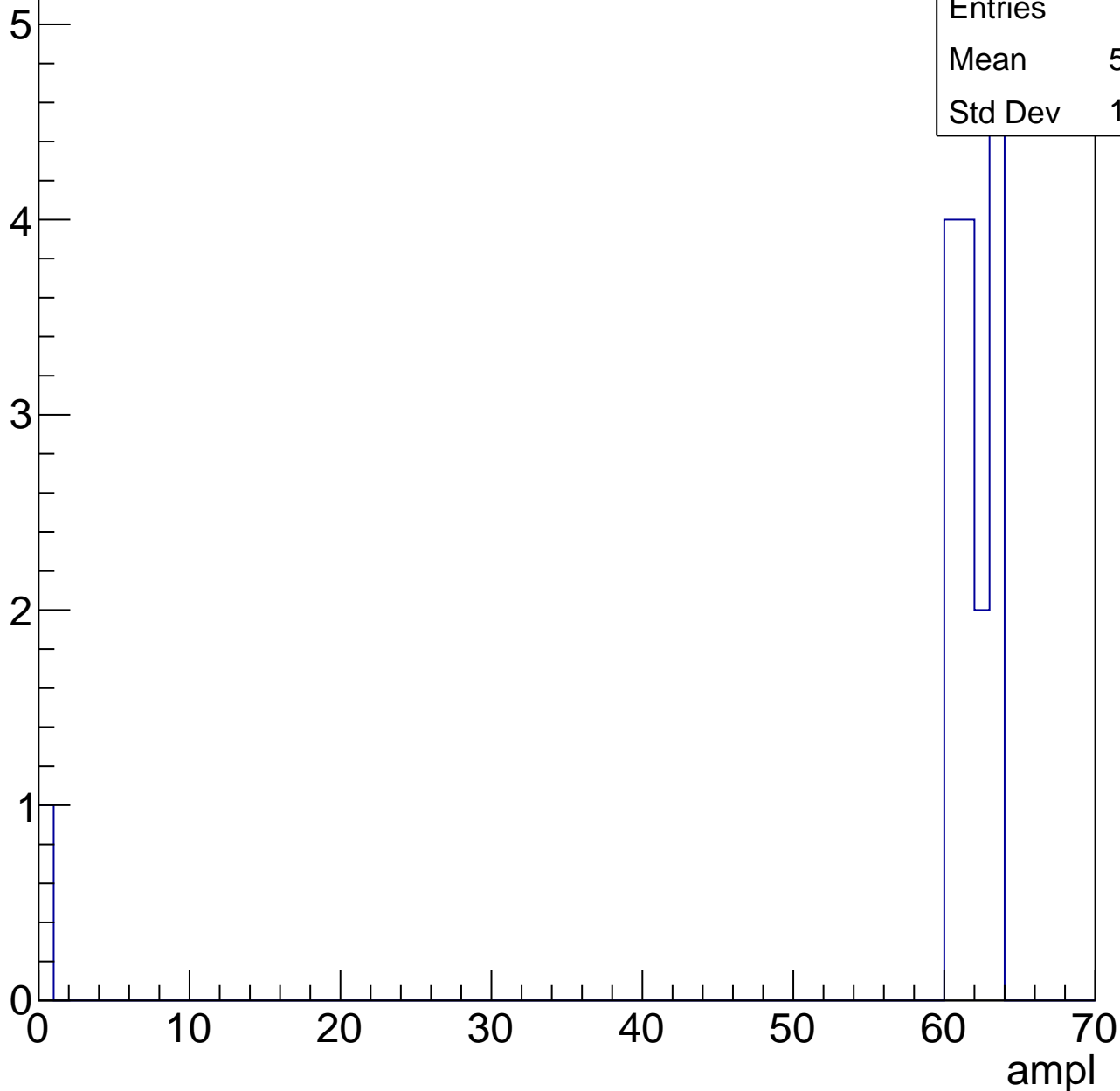
Entries	64
Mean	58.17
Std Dev	3.14

# B1L102S, U16-ch76, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	16
Mean	57.69
Std Dev	14.94





# B1L102S, U16-ch76, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch77, adc0

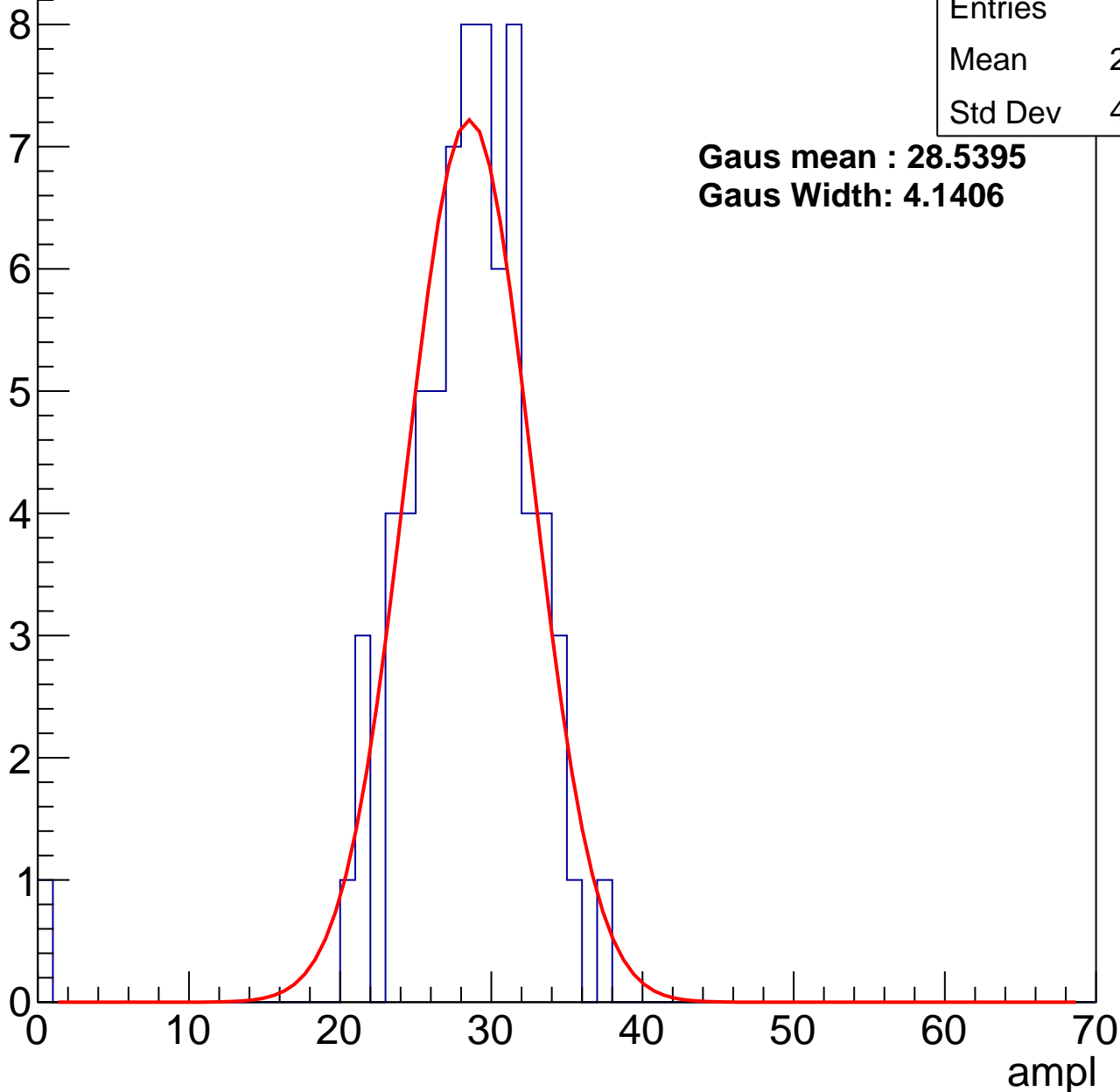
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	27.85
Std Dev	4.876

**Gaus mean : 28.5395**

**Gaus Width: 4.1406**



# B1L102S, U16-ch77, adc1

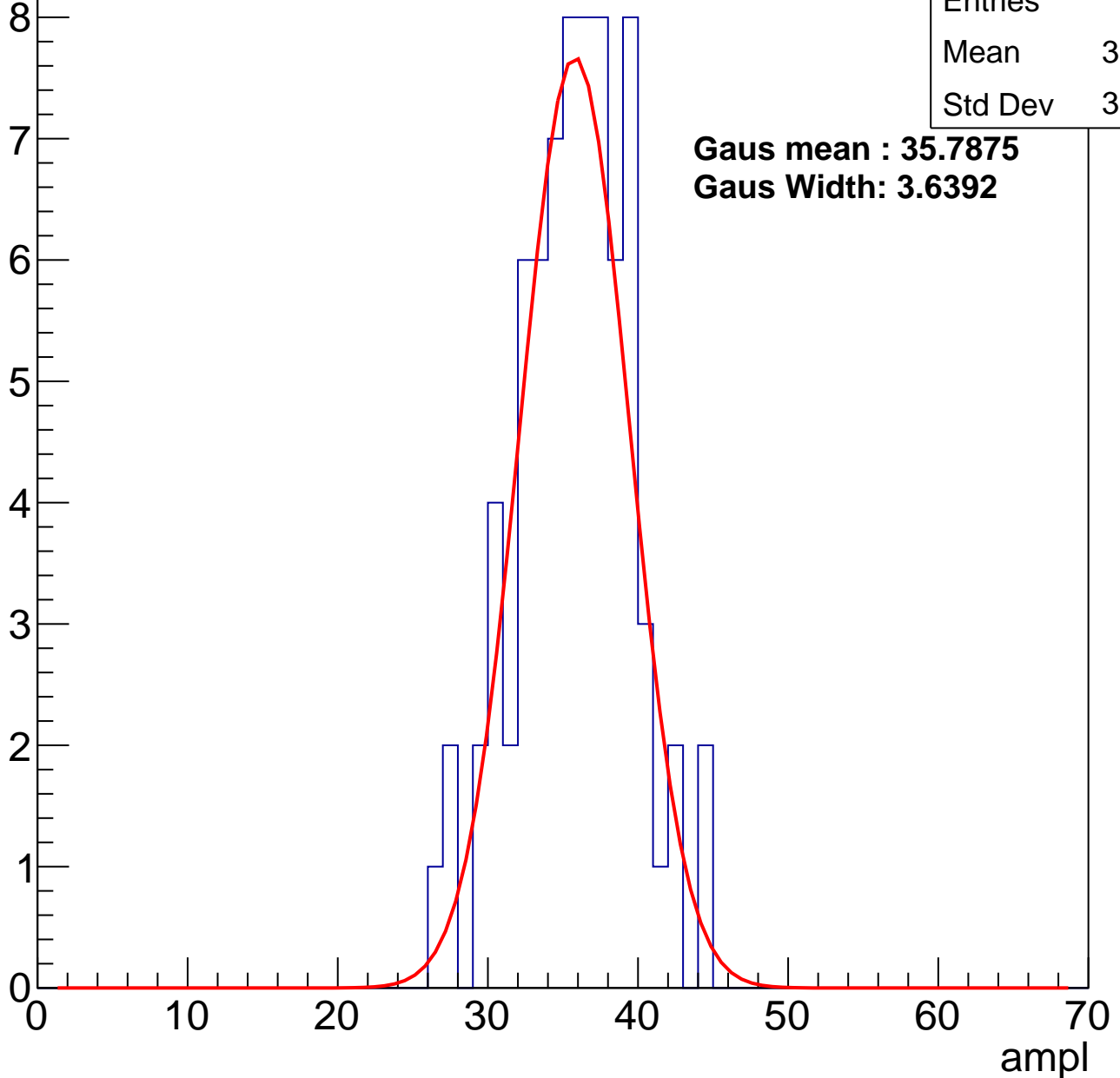
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	35.33
Std Dev	3.775

**Gaus mean : 35.7875**

**Gaus Width: 3.6392**



# B1L102S, U16-ch77, adc2

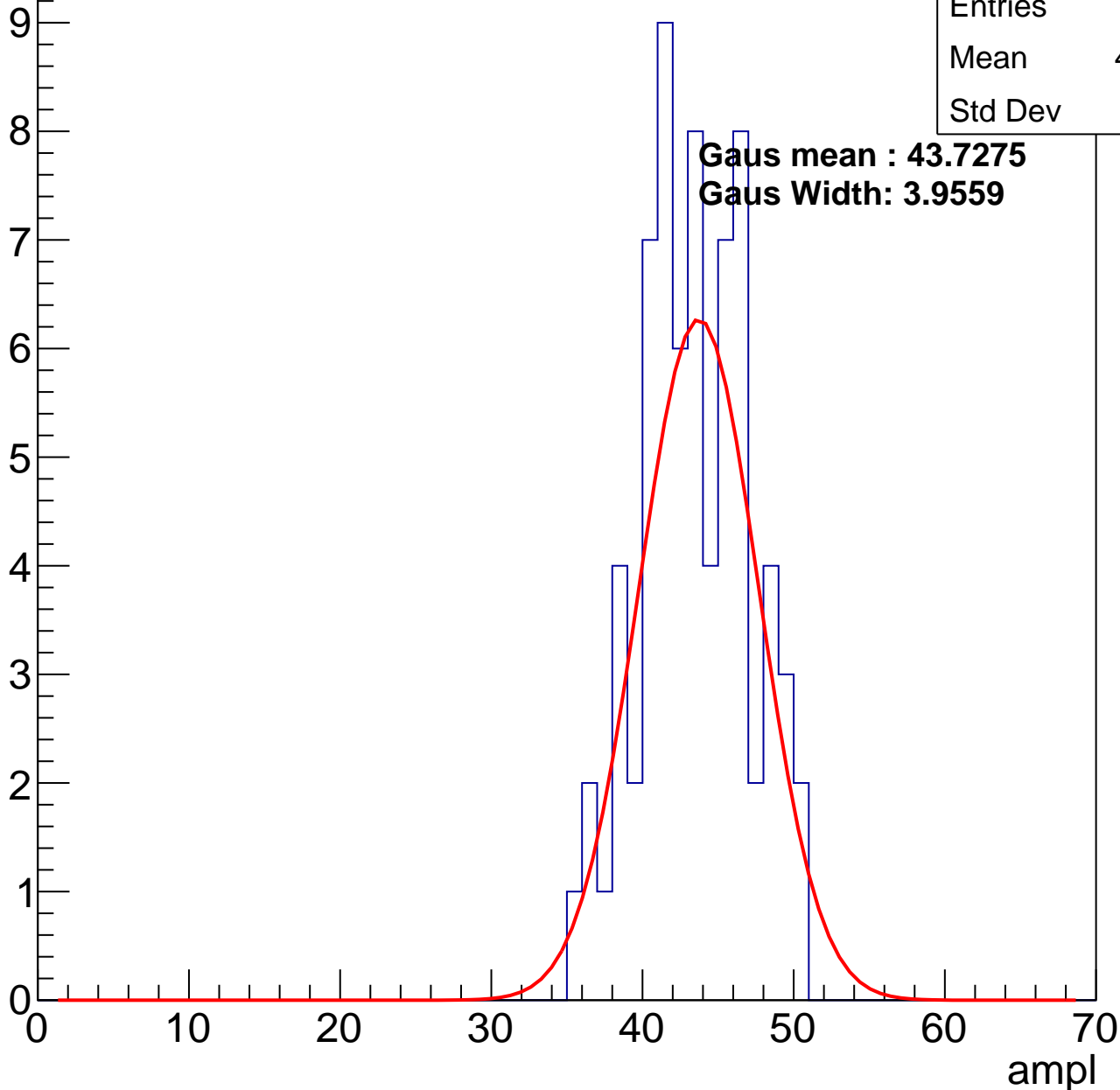
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	43.01
Std Dev	3.54

**Gaus mean : 43.7275**

**Gaus Width: 3.9559**

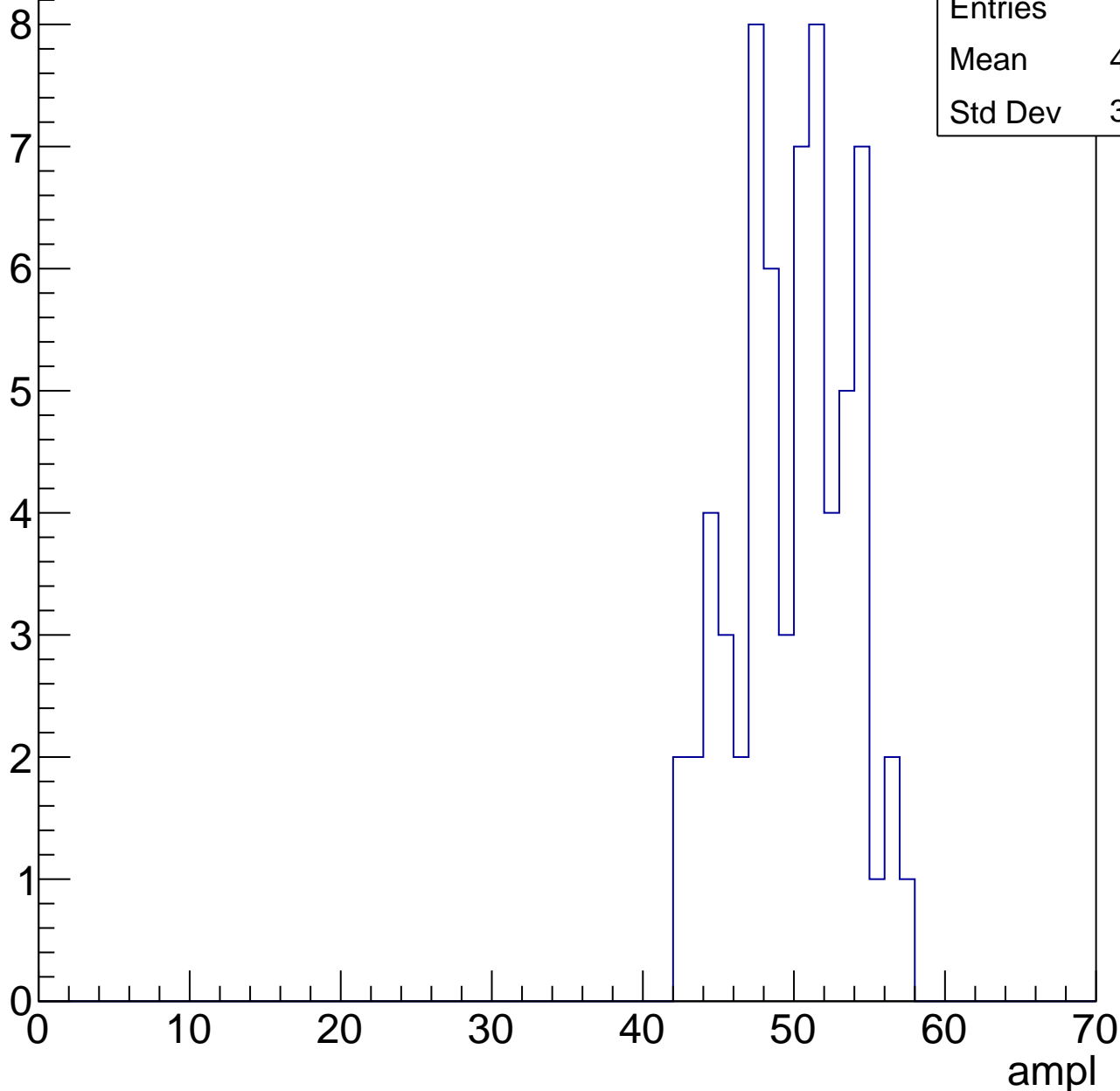


# B1L102S, U16-ch77, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	49.49
Std Dev	3.692

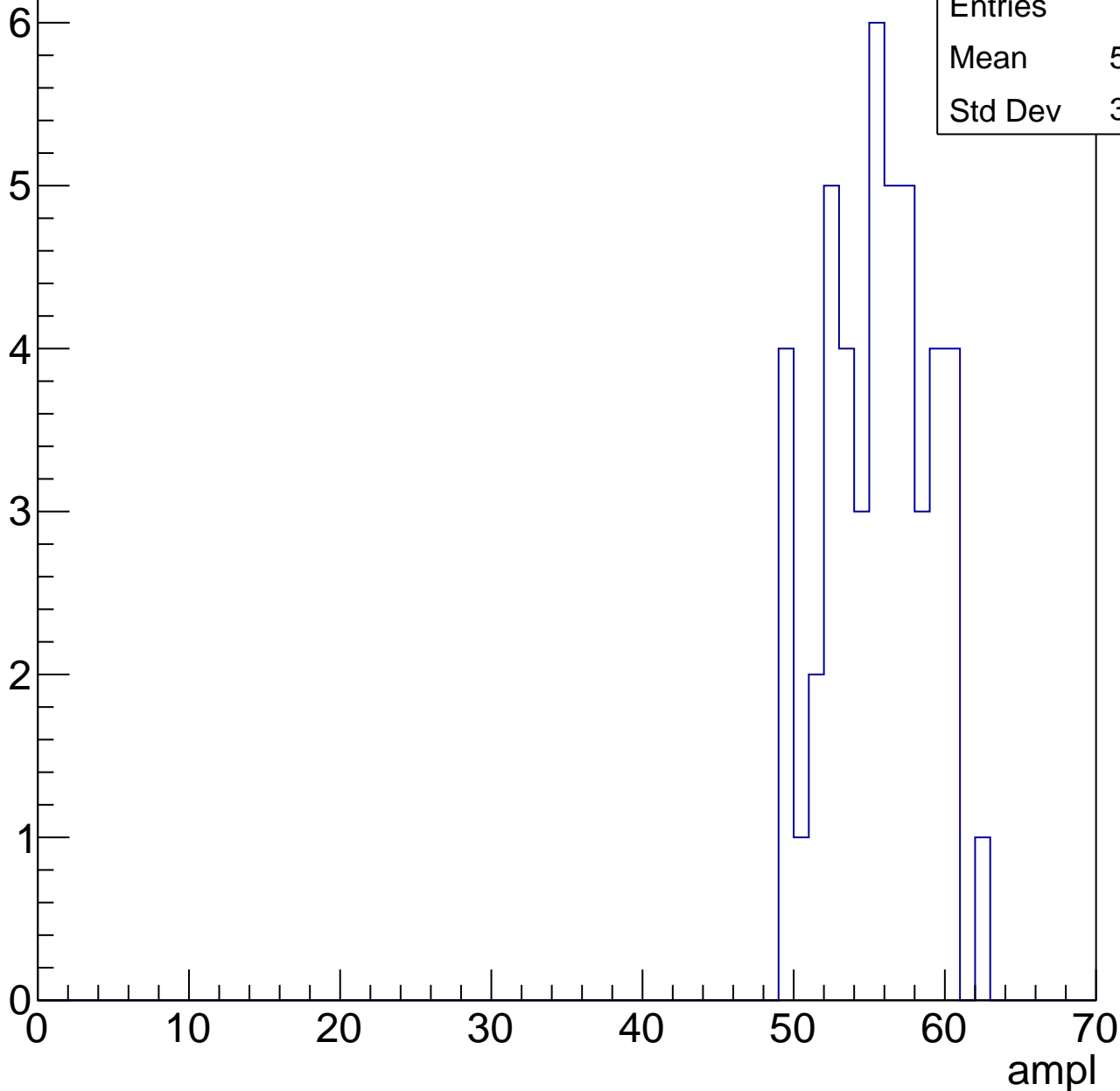


# B1L102S, U16-ch77, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	55.09
Std Dev	3.357

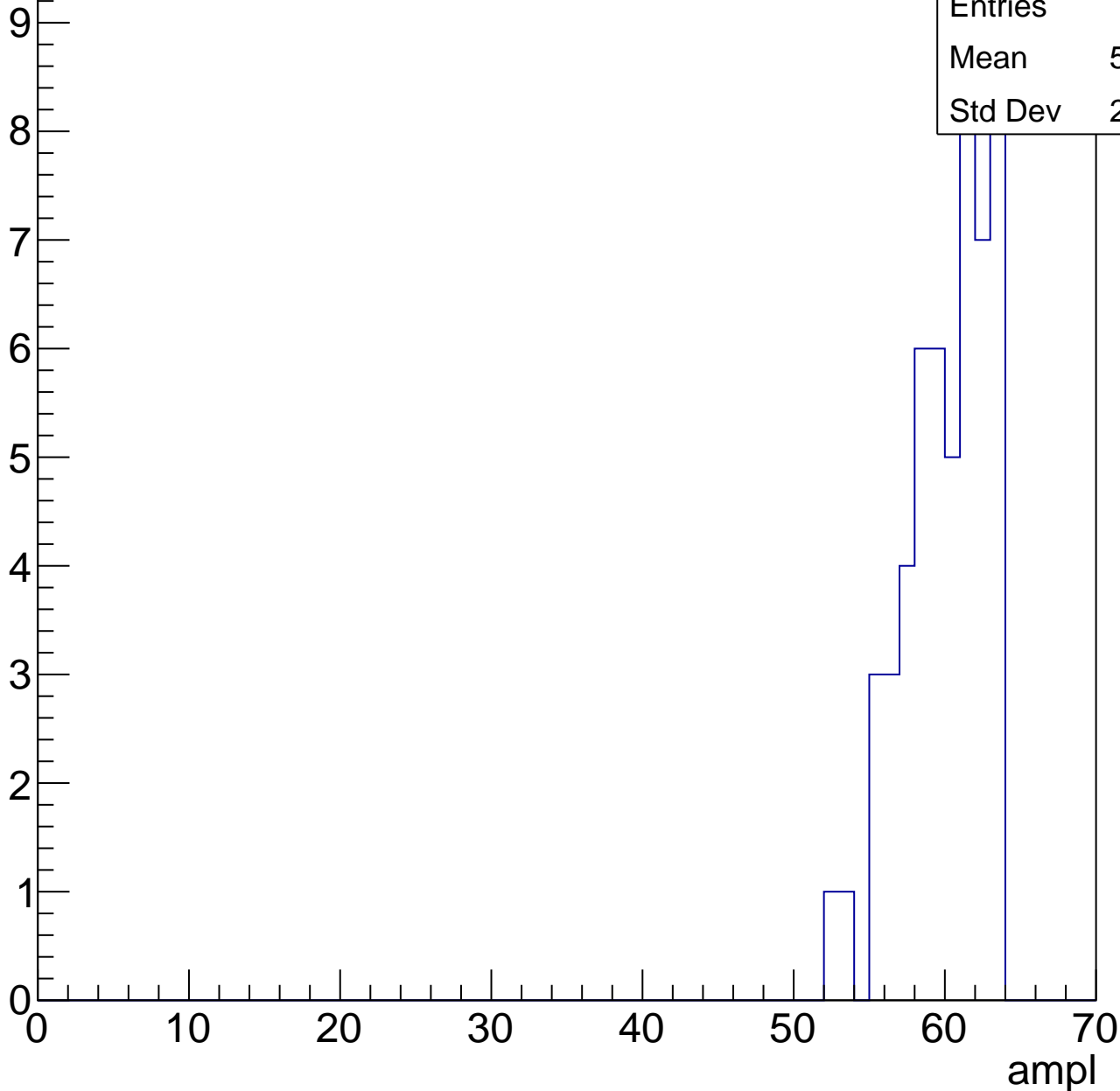


# B1L102S, U16-ch77, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

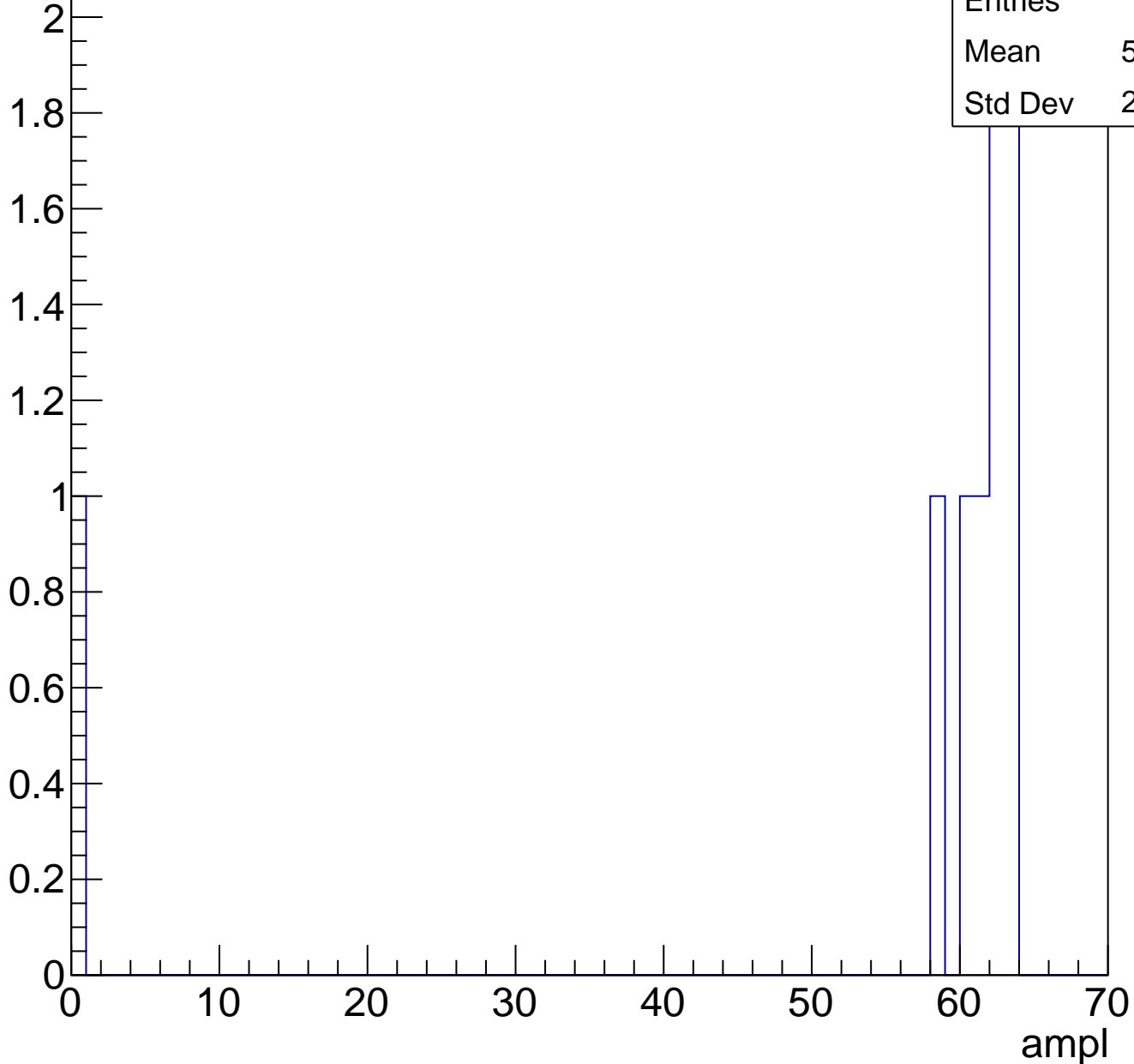
Entries	53
Mean	59.53
Std Dev	2.744



# B1L102S, U16-ch77, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch77, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U16-ch78, adc0

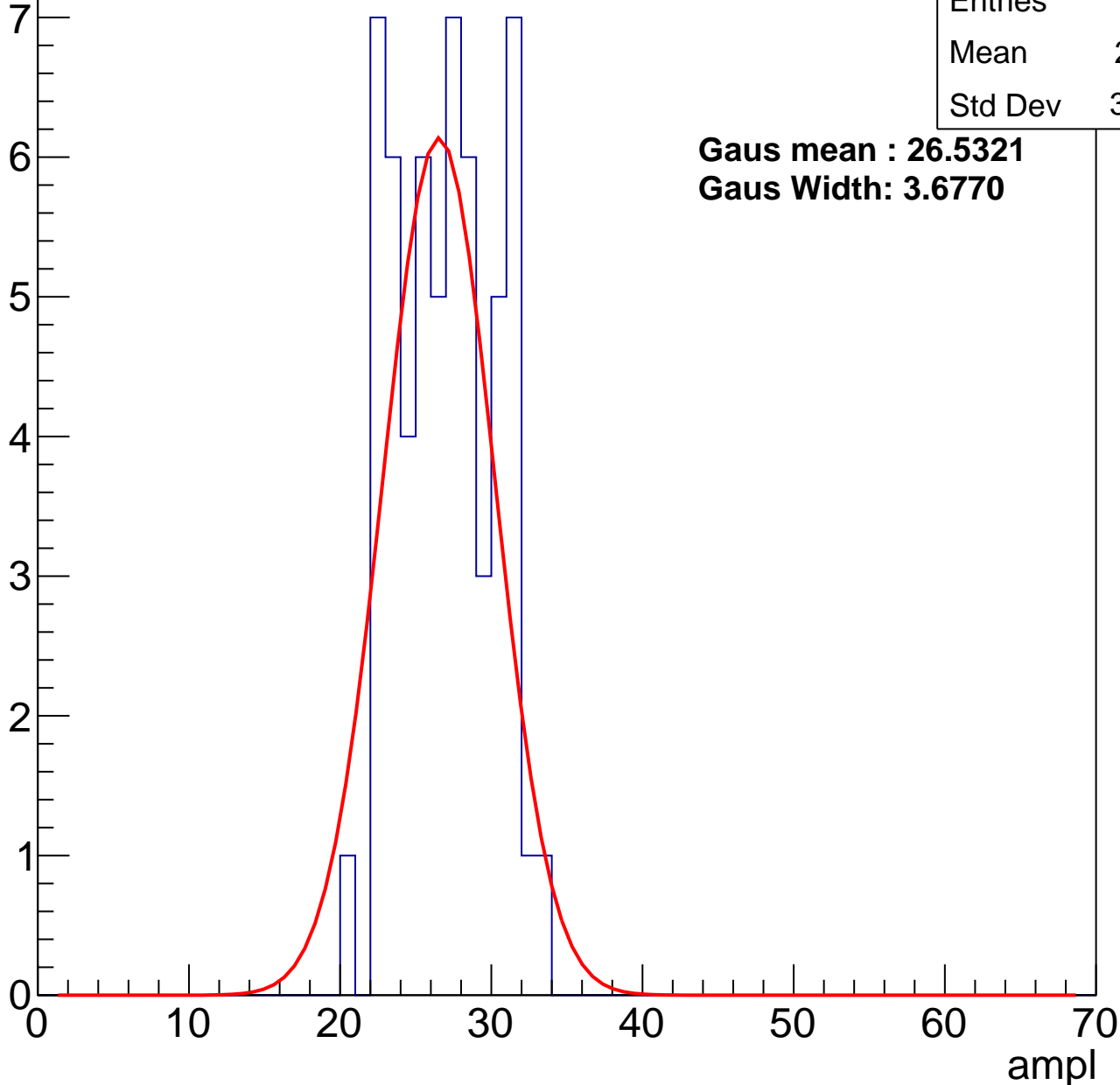
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	26.51
Std Dev	3.207

**Gaus mean : 26.5321**

**Gaus Width: 3.6770**



# B1L102S, U16-ch78, adc1

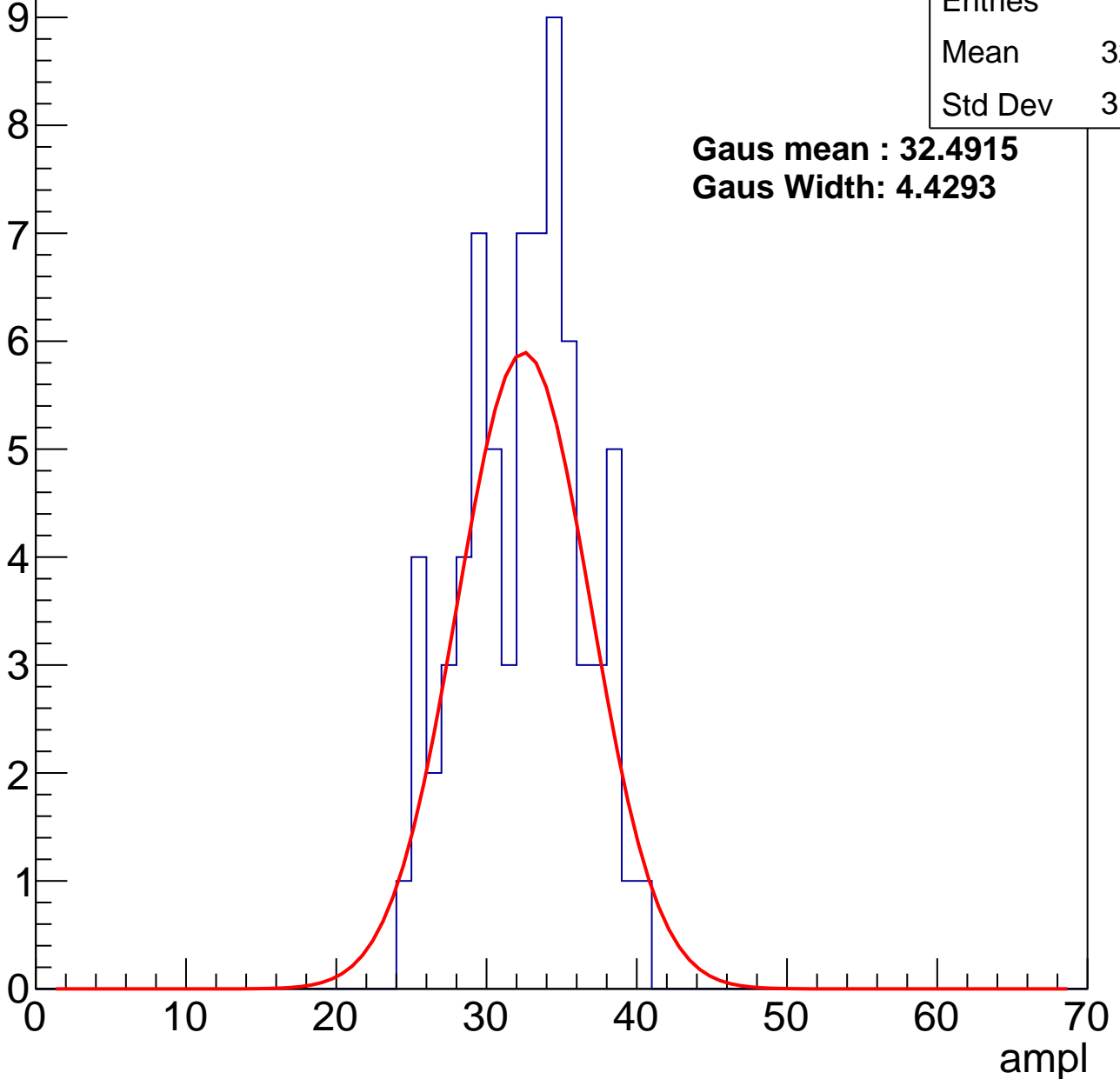
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	32.03
Std Dev	3.882

**Gaus mean : 32.4915**

**Gaus Width: 4.4293**



# B1L102S, U16-ch78, adc2

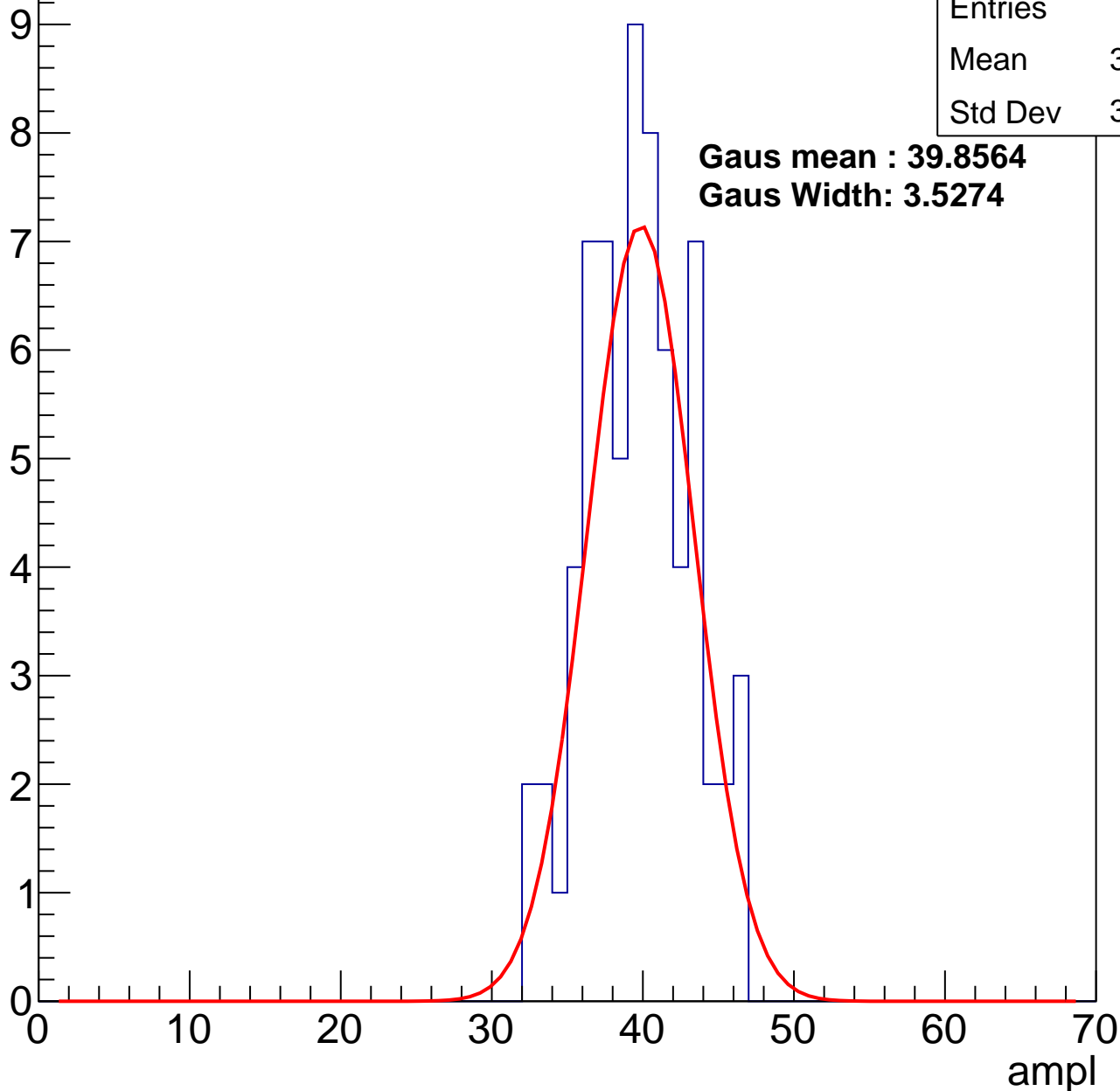
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	39.23
Std Dev	3.406

**Gaus mean : 39.8564**

**Gaus Width: 3.5274**



# B1L102S, U16-ch78, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

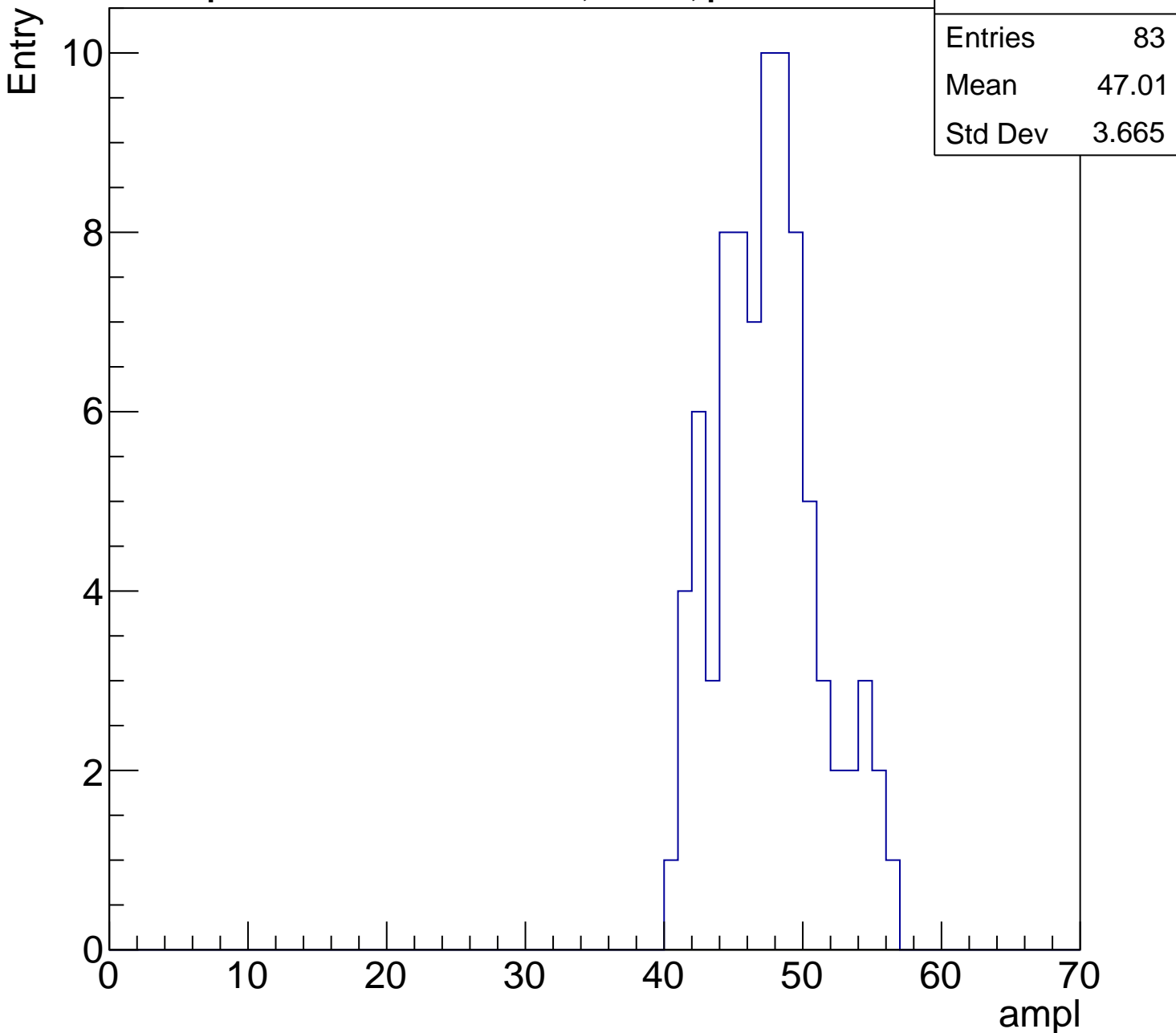
Entries	83
Mean	47.01
Std Dev	3.665

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

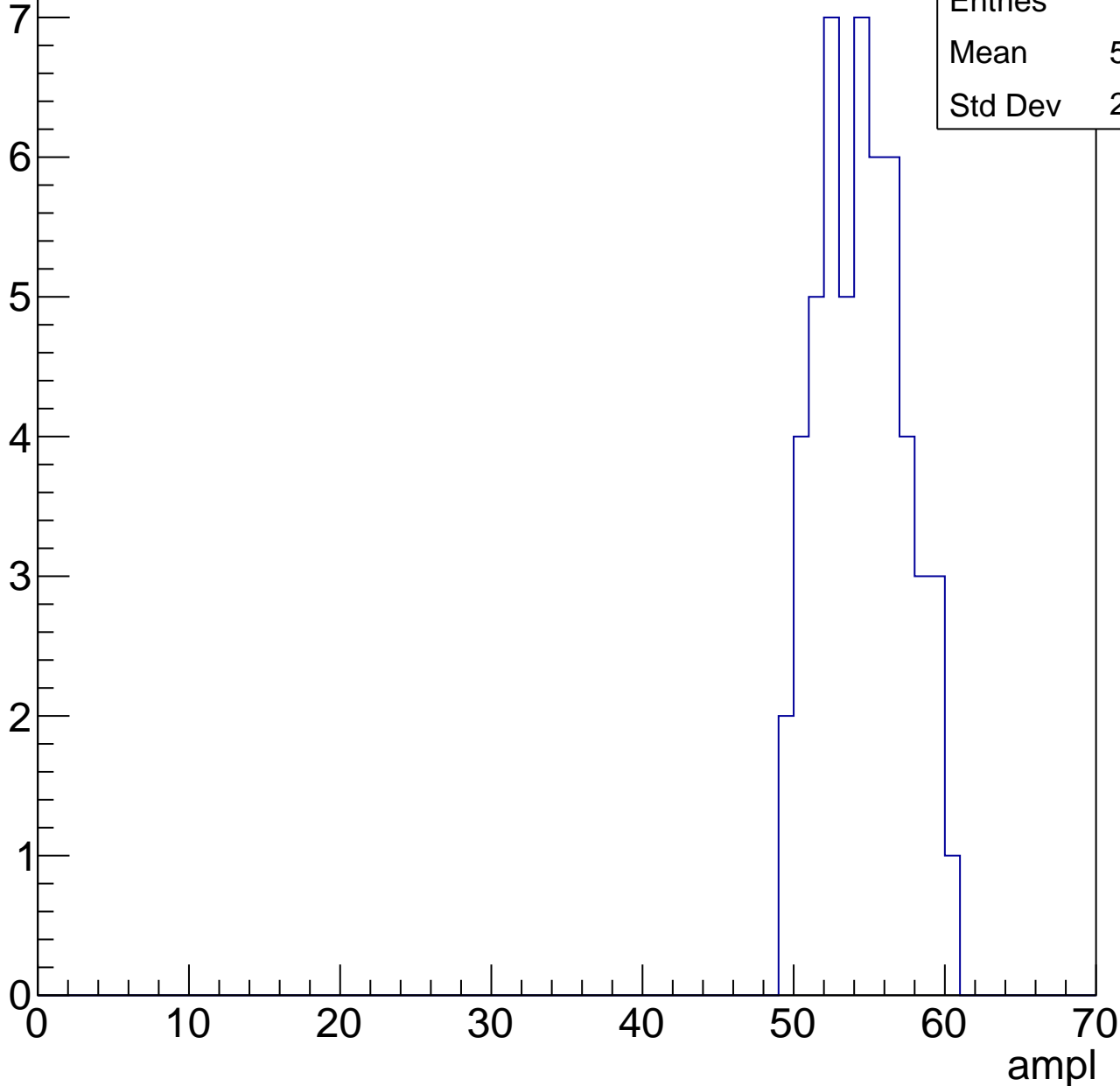


# B1L102S, U16-ch78, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	54.06
Std Dev	2.804

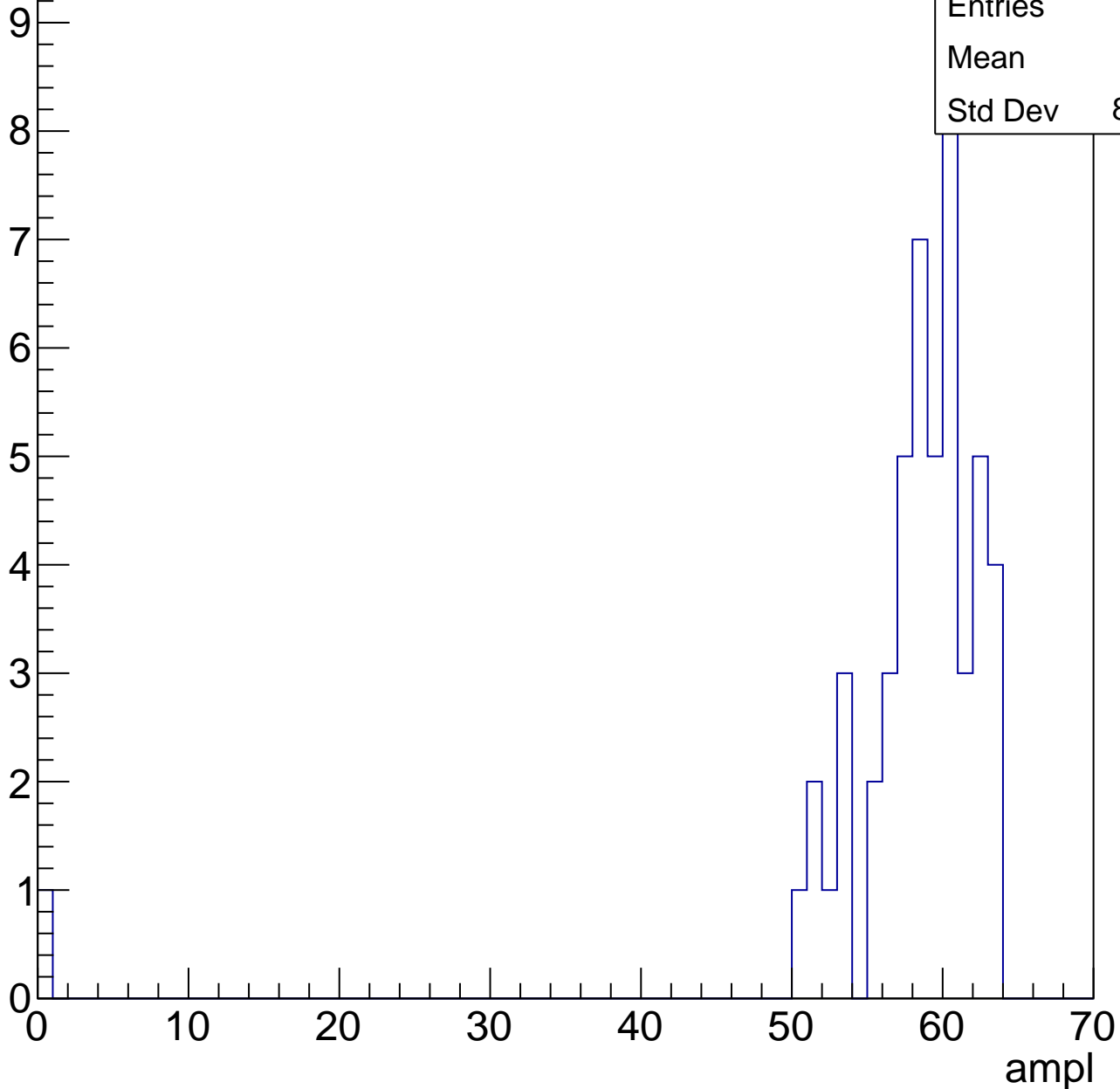


# B1L102S, U16-ch78, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

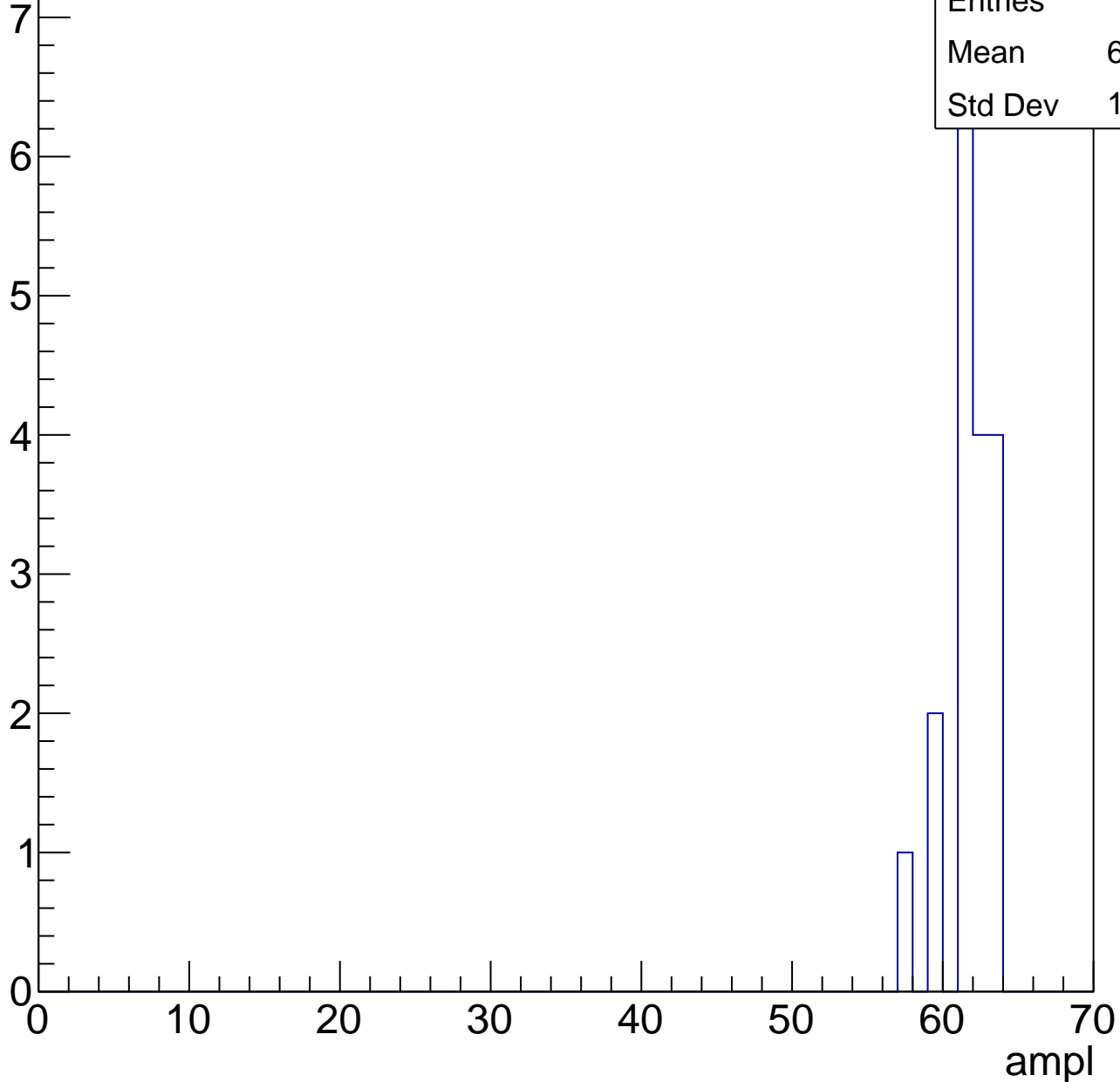
Entries	51
Mean	57.1
Std Dev	8.721



# B1L102S, U16-ch78, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch78, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch79, adc0

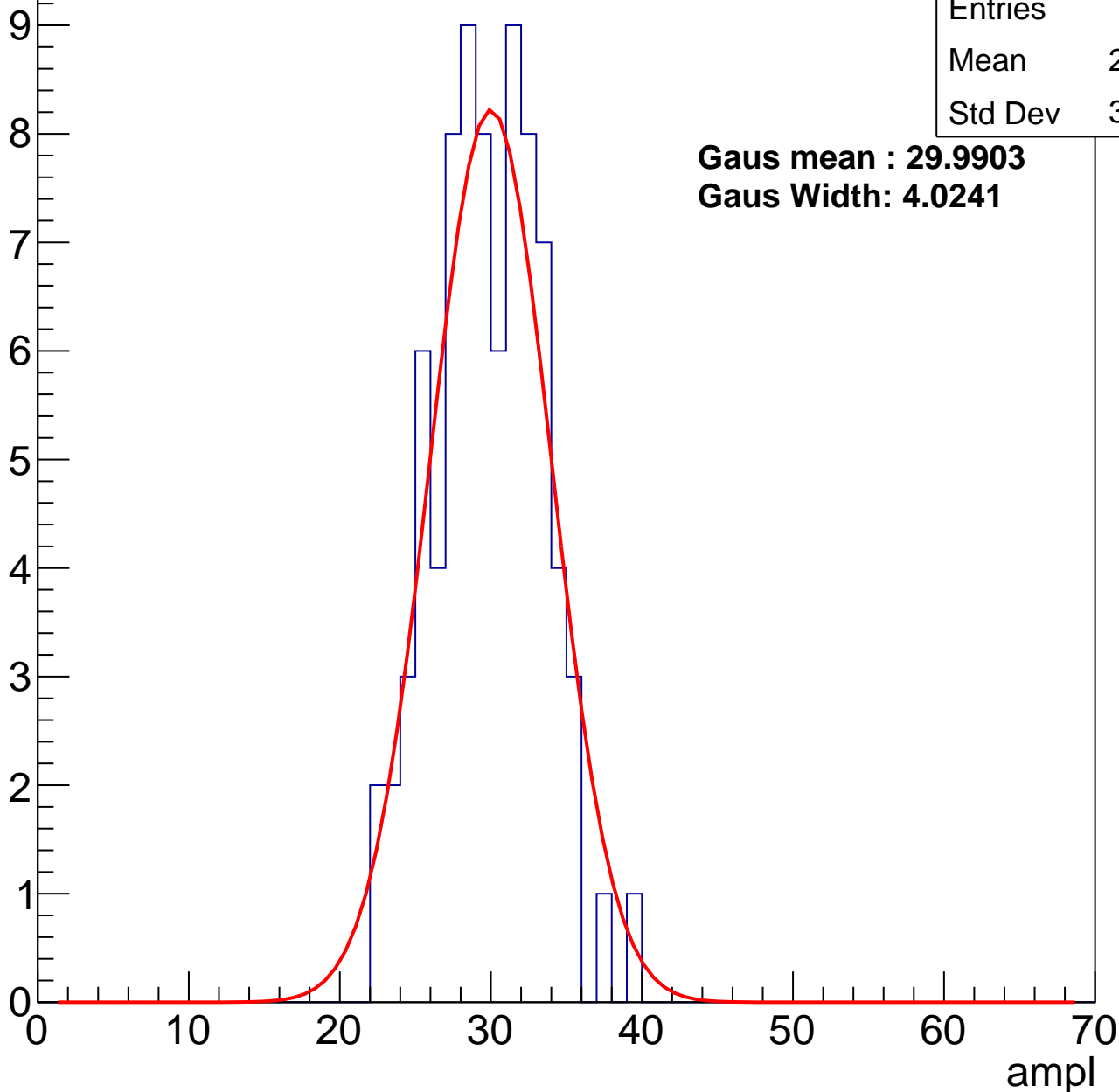
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	81
Mean	29.37
Std Dev	3.522

**Gaus mean : 29.9903**

**Gaus Width: 4.0241**



# B1L102S, U16-ch79, adc1

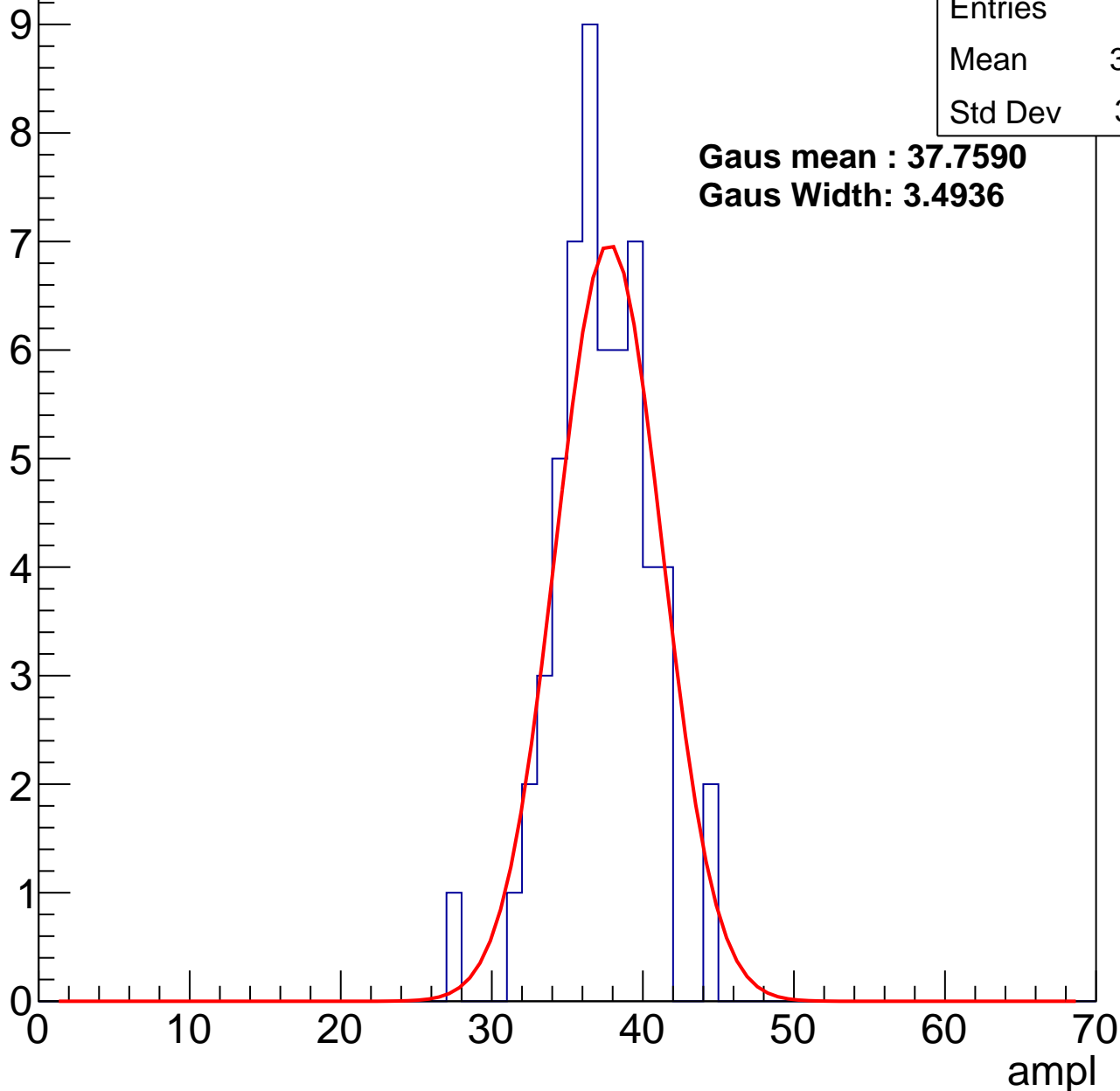
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	36.75
Std Dev	3.091

**Gaus mean : 37.7590**

**Gaus Width: 3.4936**



# B1L102S, U16-ch79, adc2

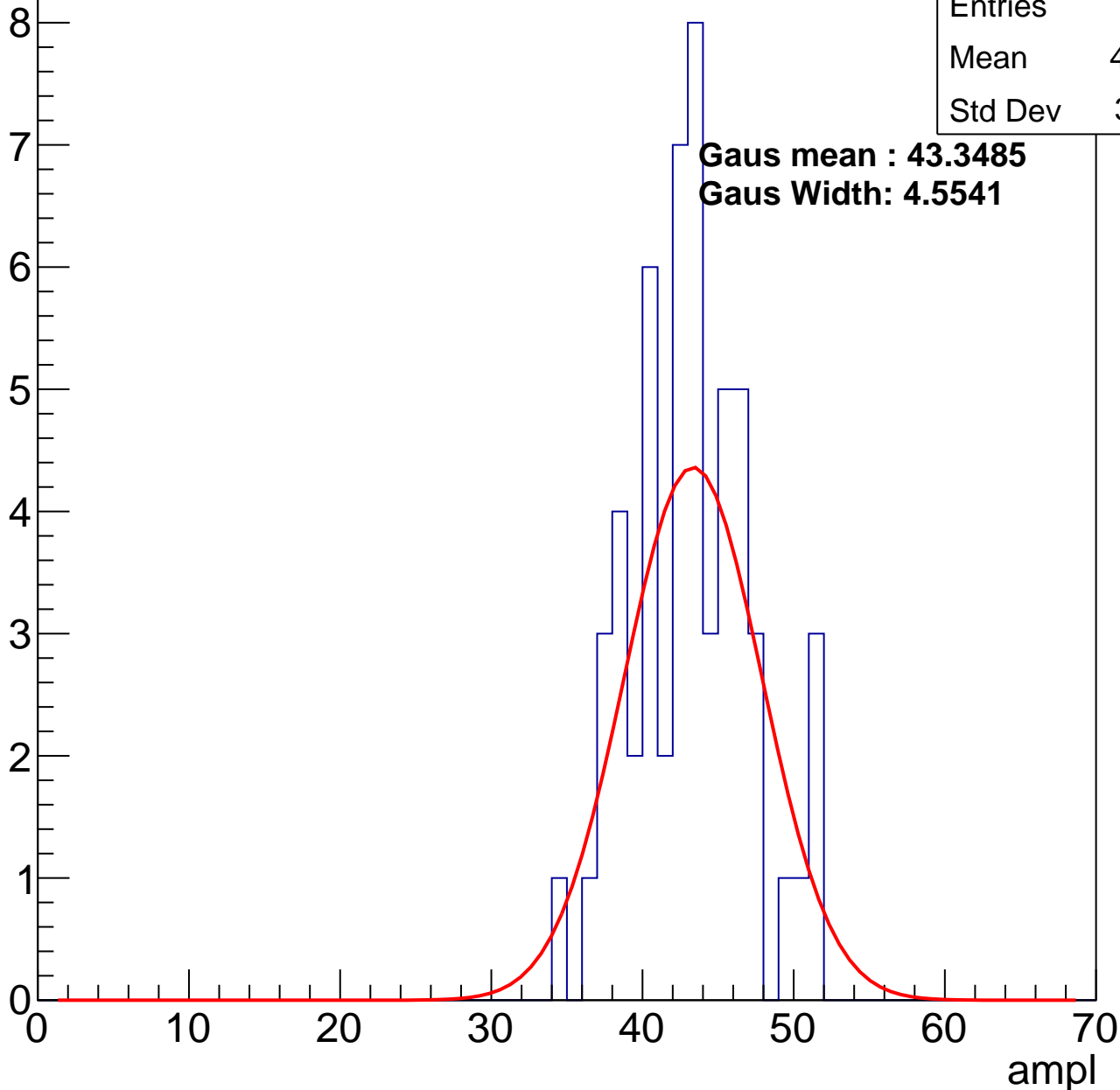
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	42.75
Std Dev	3.881

**Gaus mean : 43.3485**

**Gaus Width: 4.5541**



# B1L102S, U16-ch79, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

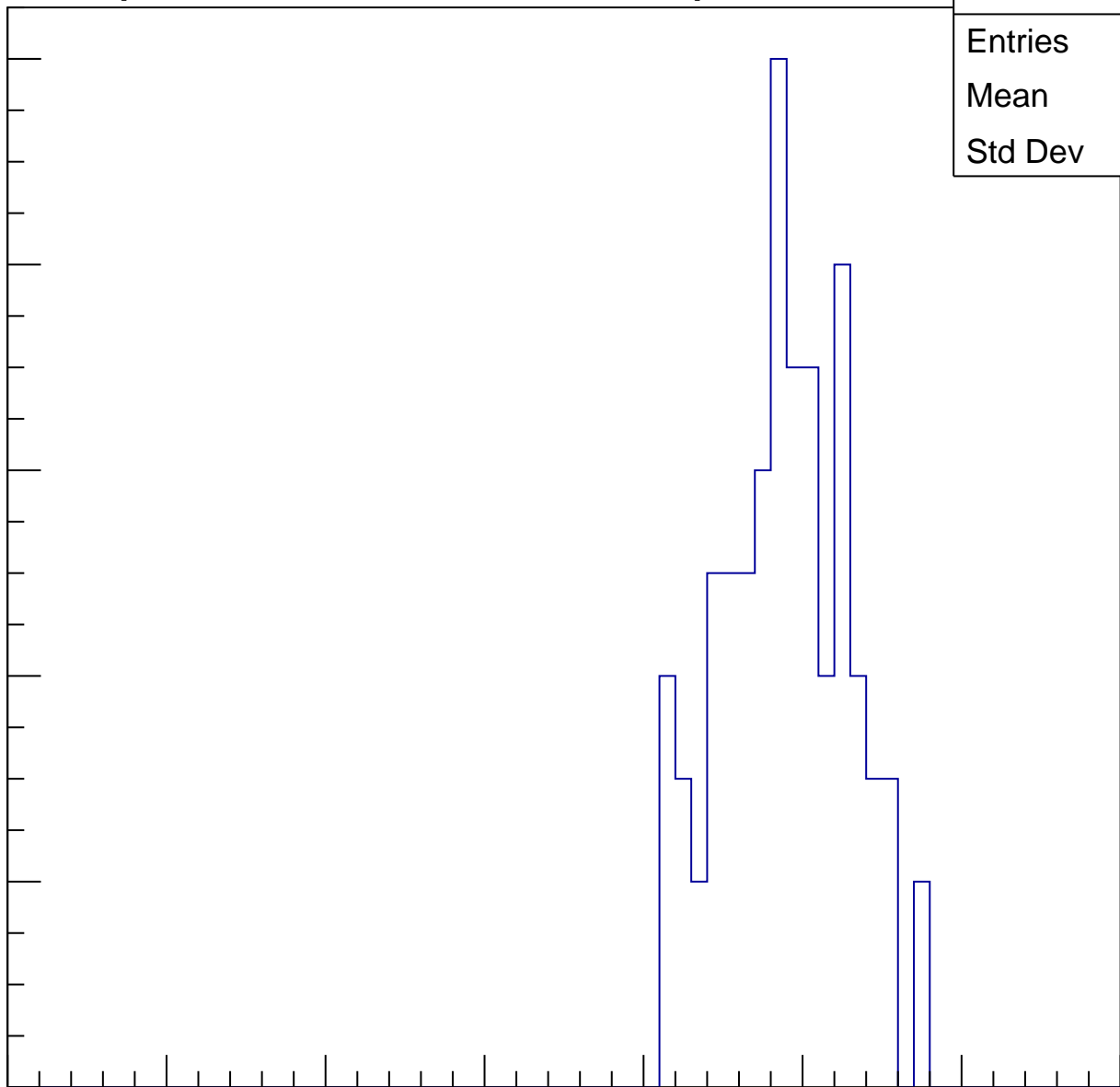
Entries	78
Mean	48.45
Std Dev	3.931

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

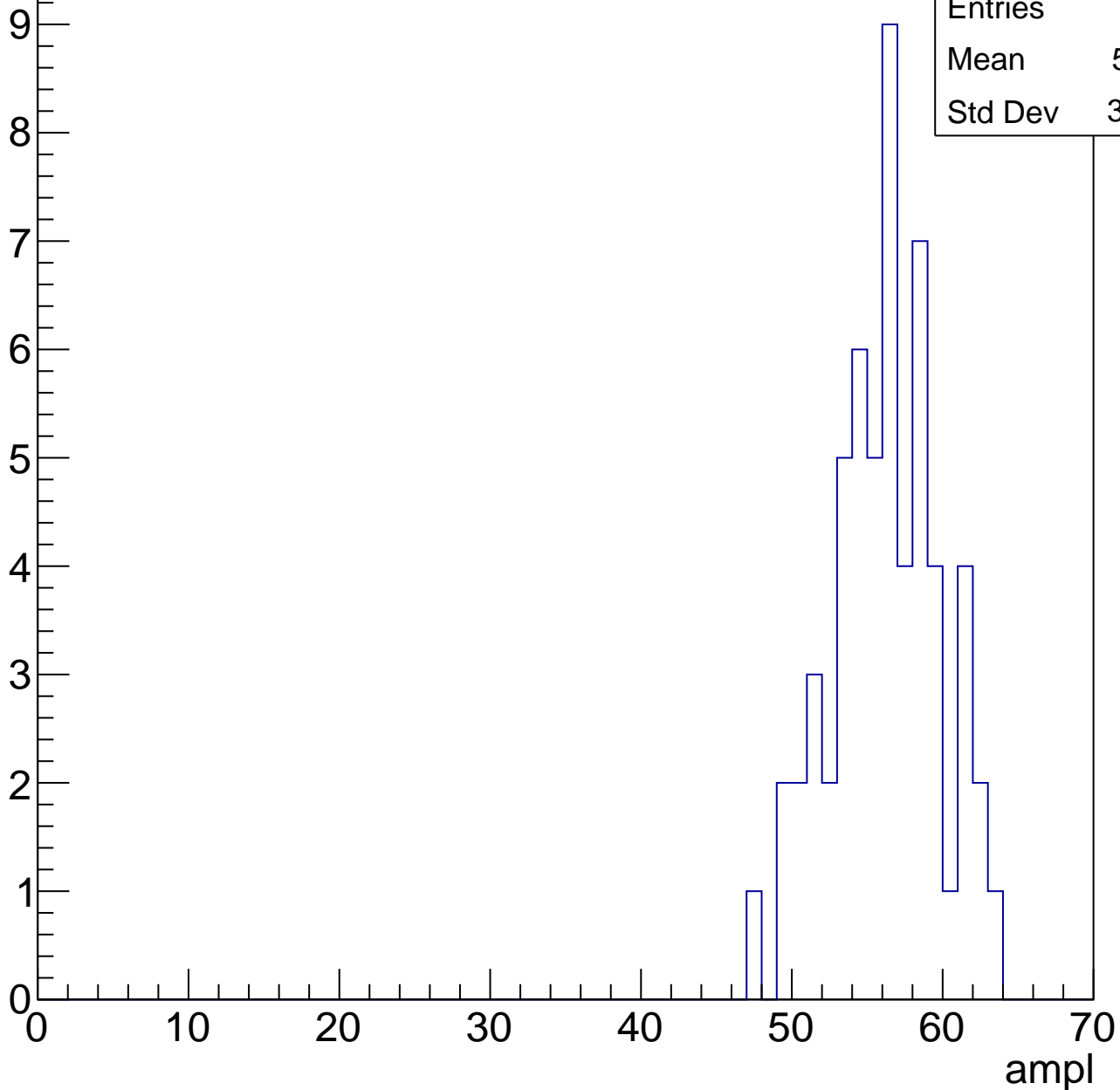


# B1L102S, U16-ch79, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

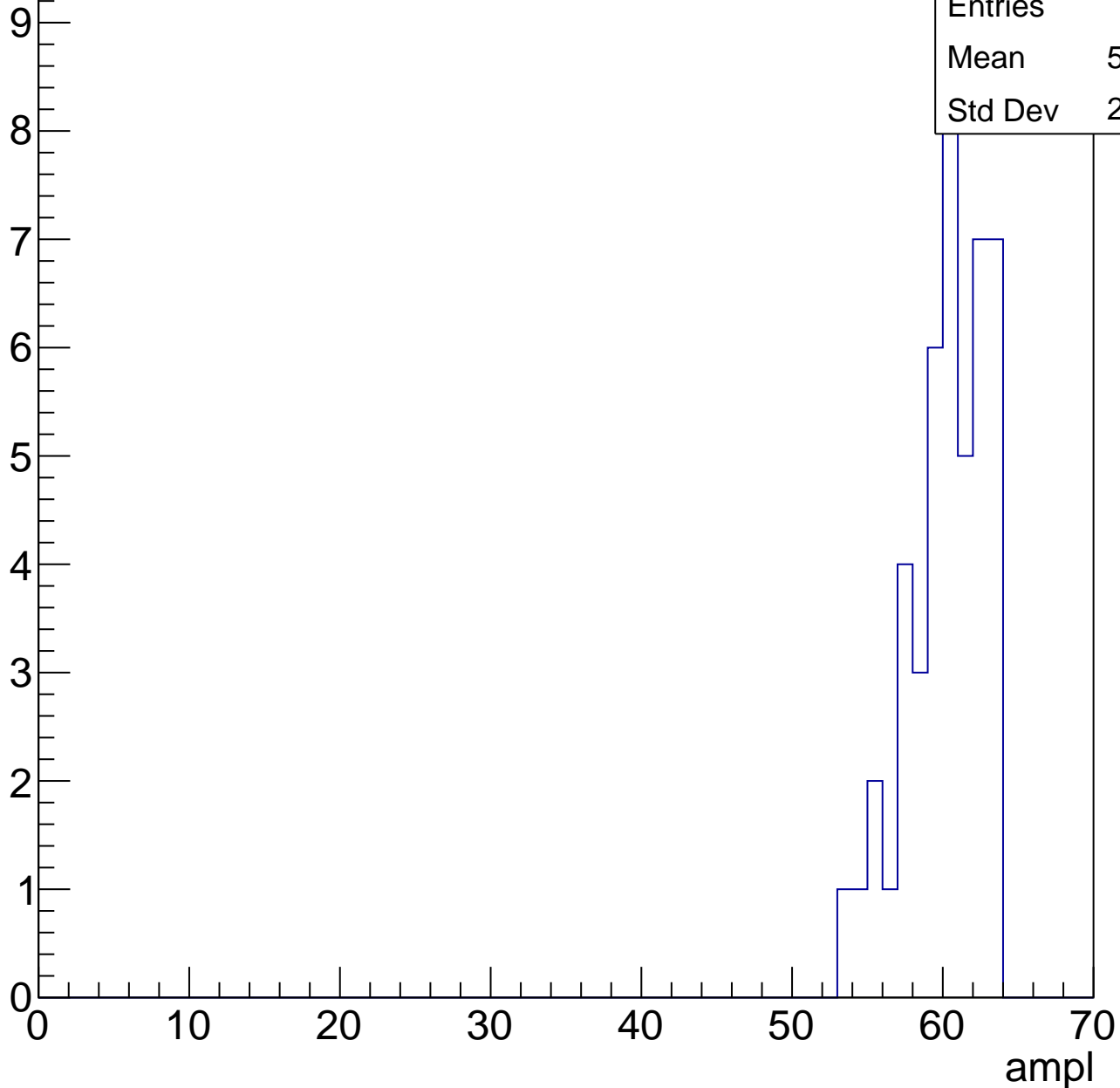
Entries	58
Mean	55.71
Std Dev	3.553



# B1L102S, U16-ch79, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch79, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

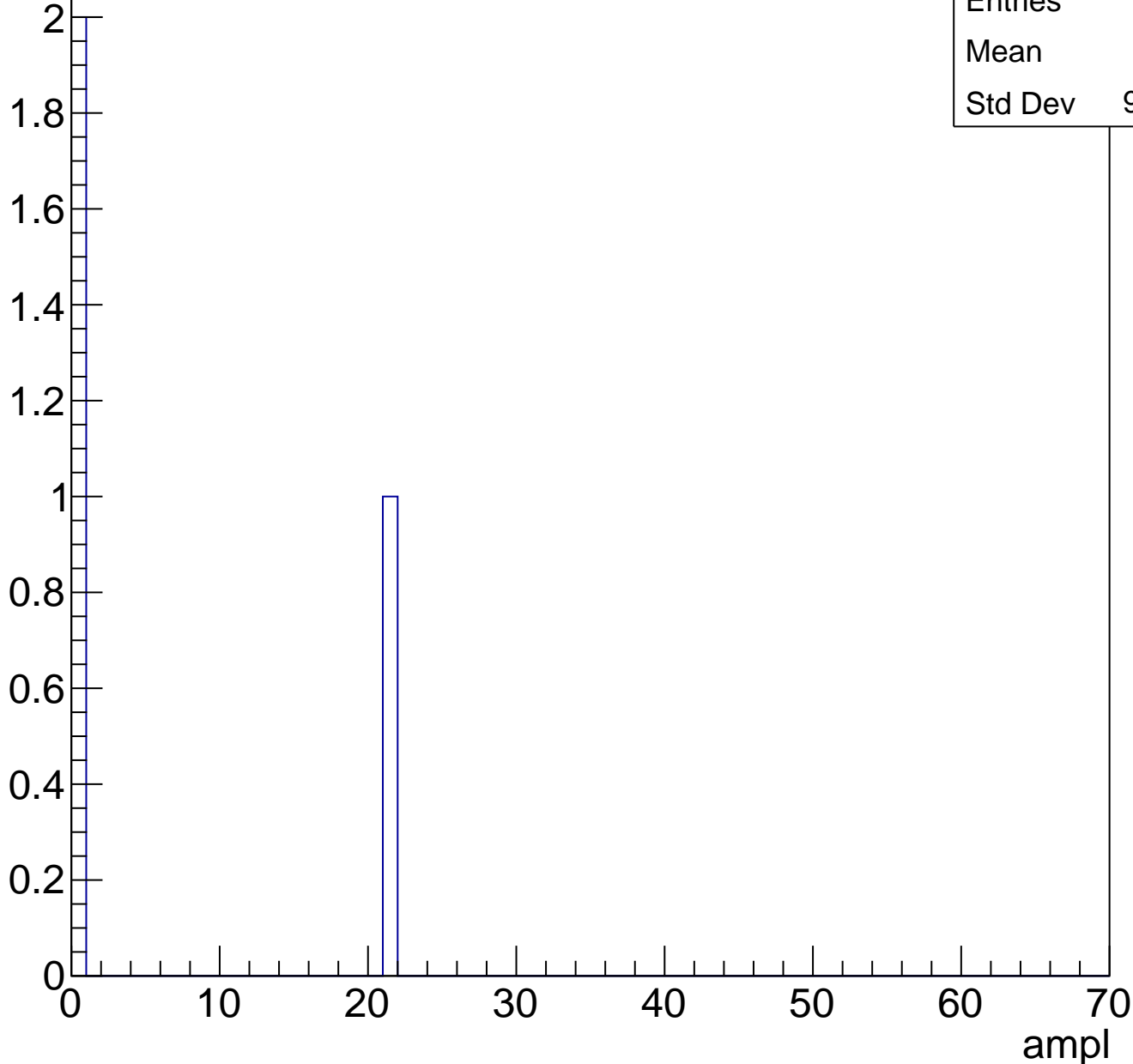




# B1L102S, U16-ch79, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	7
Std Dev	9.899

# B1L102S, U16-ch80, adc0

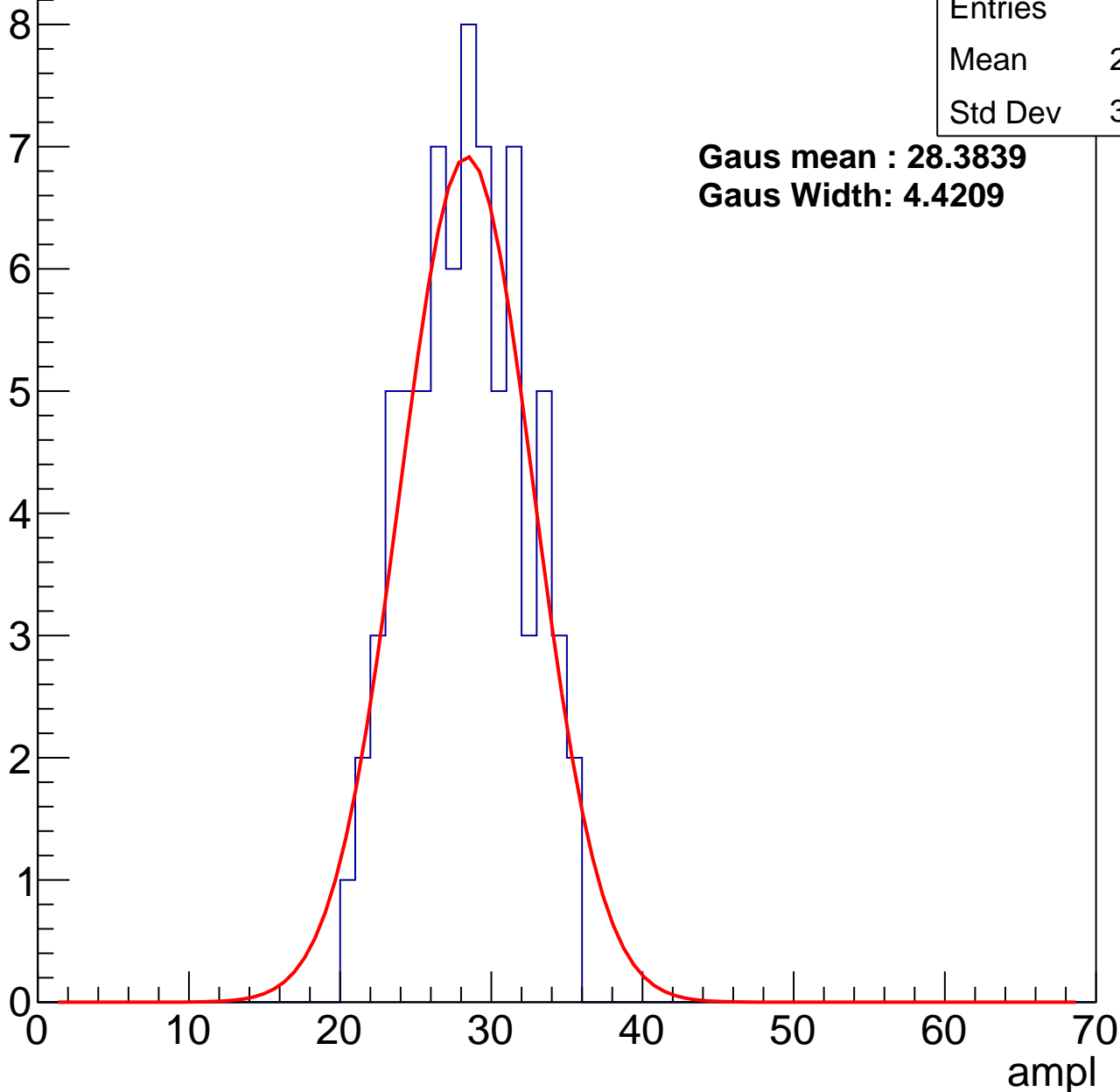
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	27.82
Std Dev	3.714

**Gaus mean : 28.3839**

**Gaus Width: 4.4209**



# B1L102S, U16-ch80, adc1

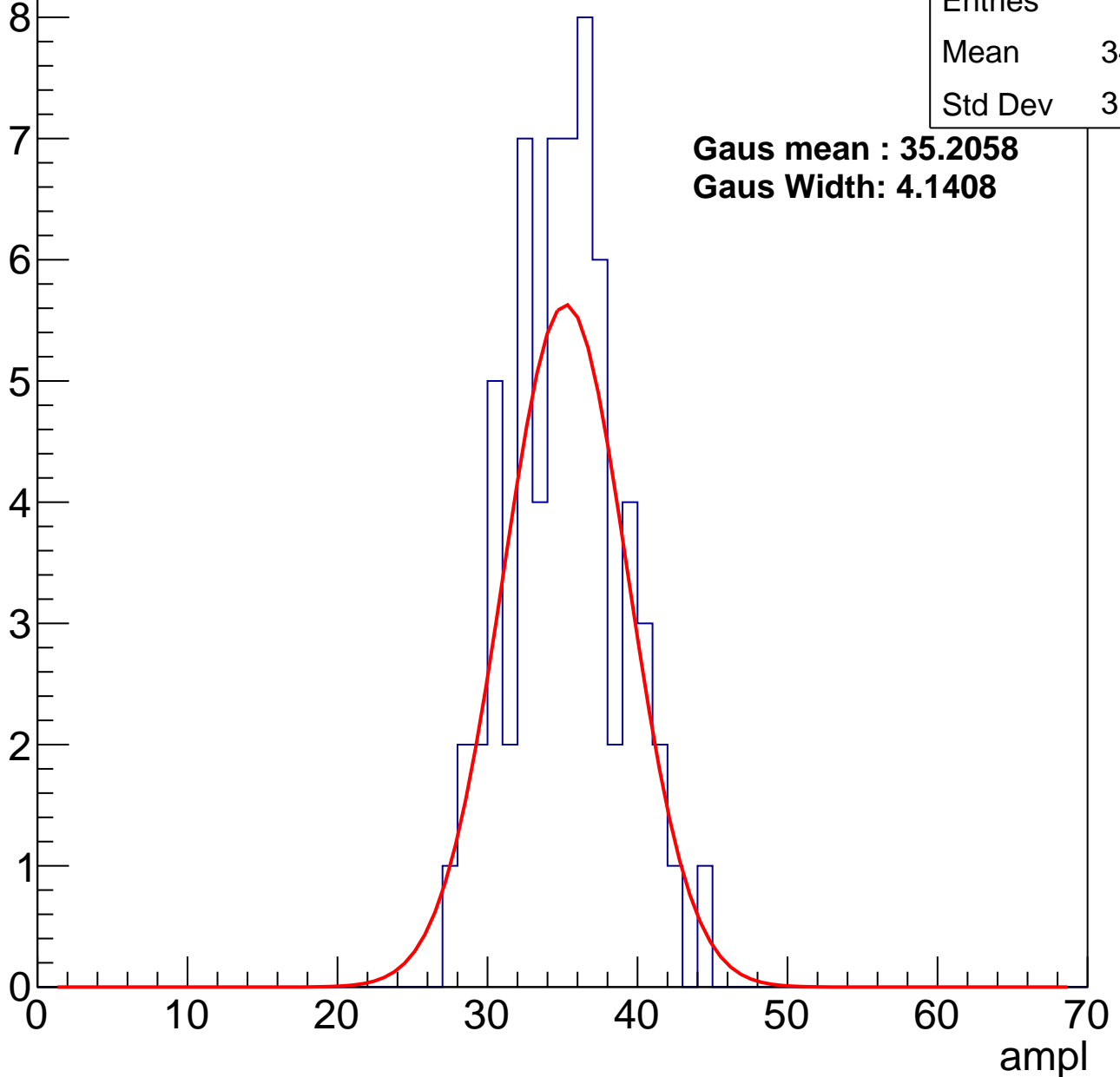
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	34.72
Std Dev	3.672

**Gaus mean : 35.2058**

**Gaus Width: 4.1408**



# B1L102S, U16-ch80, adc2

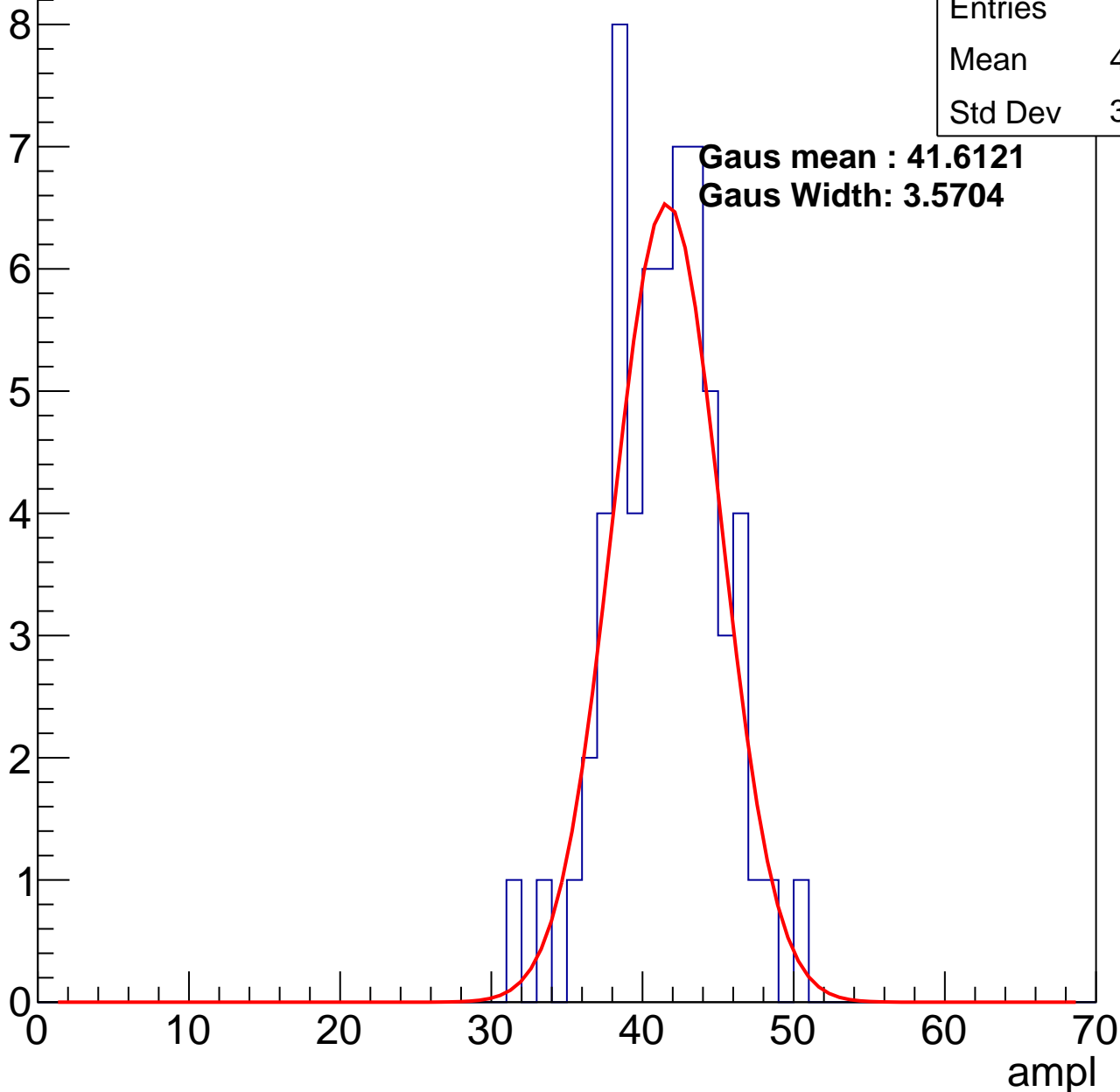
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	41.03
Std Dev	3.596

**Gaus mean : 41.6121**

**Gaus Width: 3.5704**

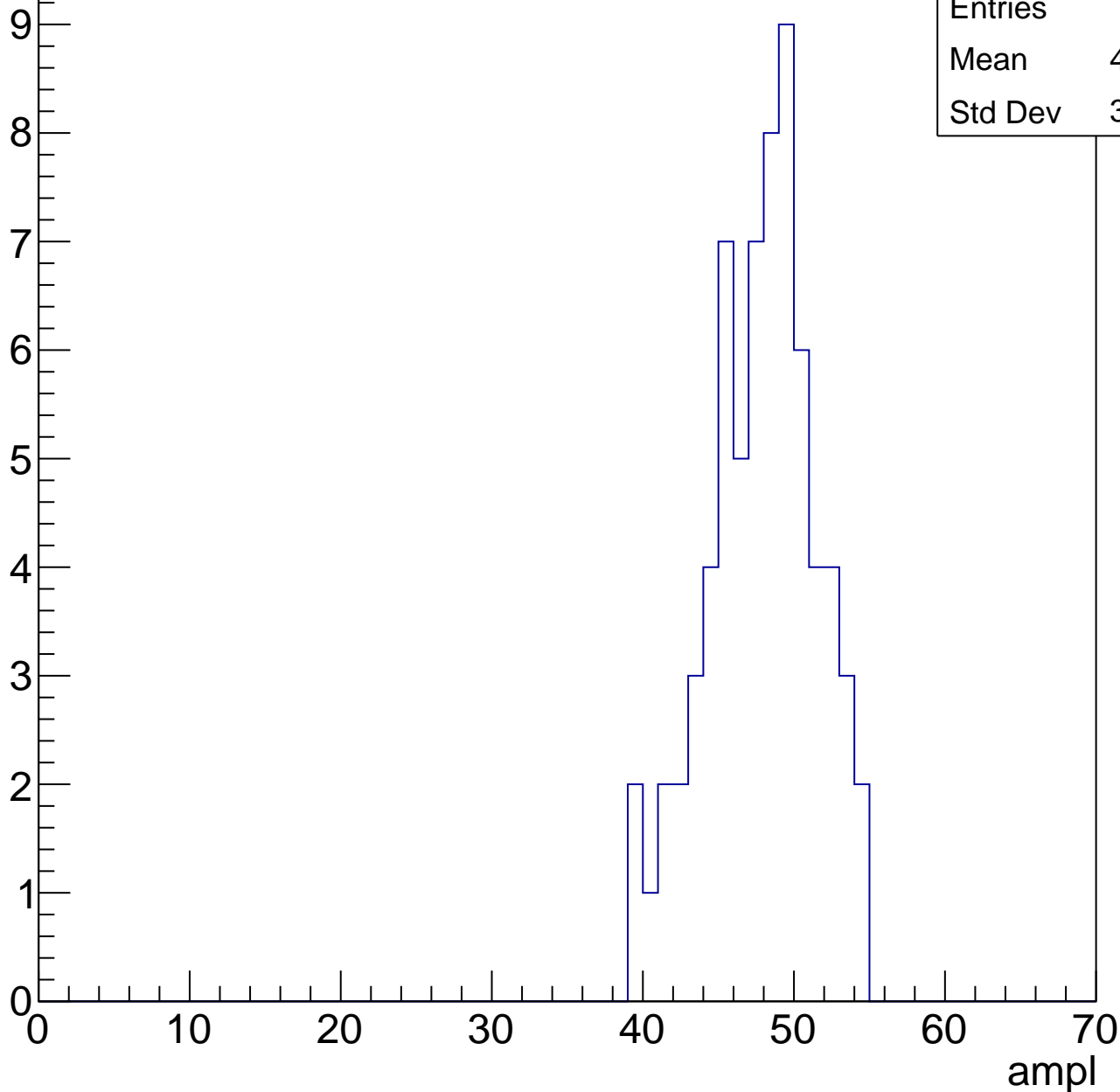


# B1L102S, U16-ch80, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	47.35
Std Dev	3.562

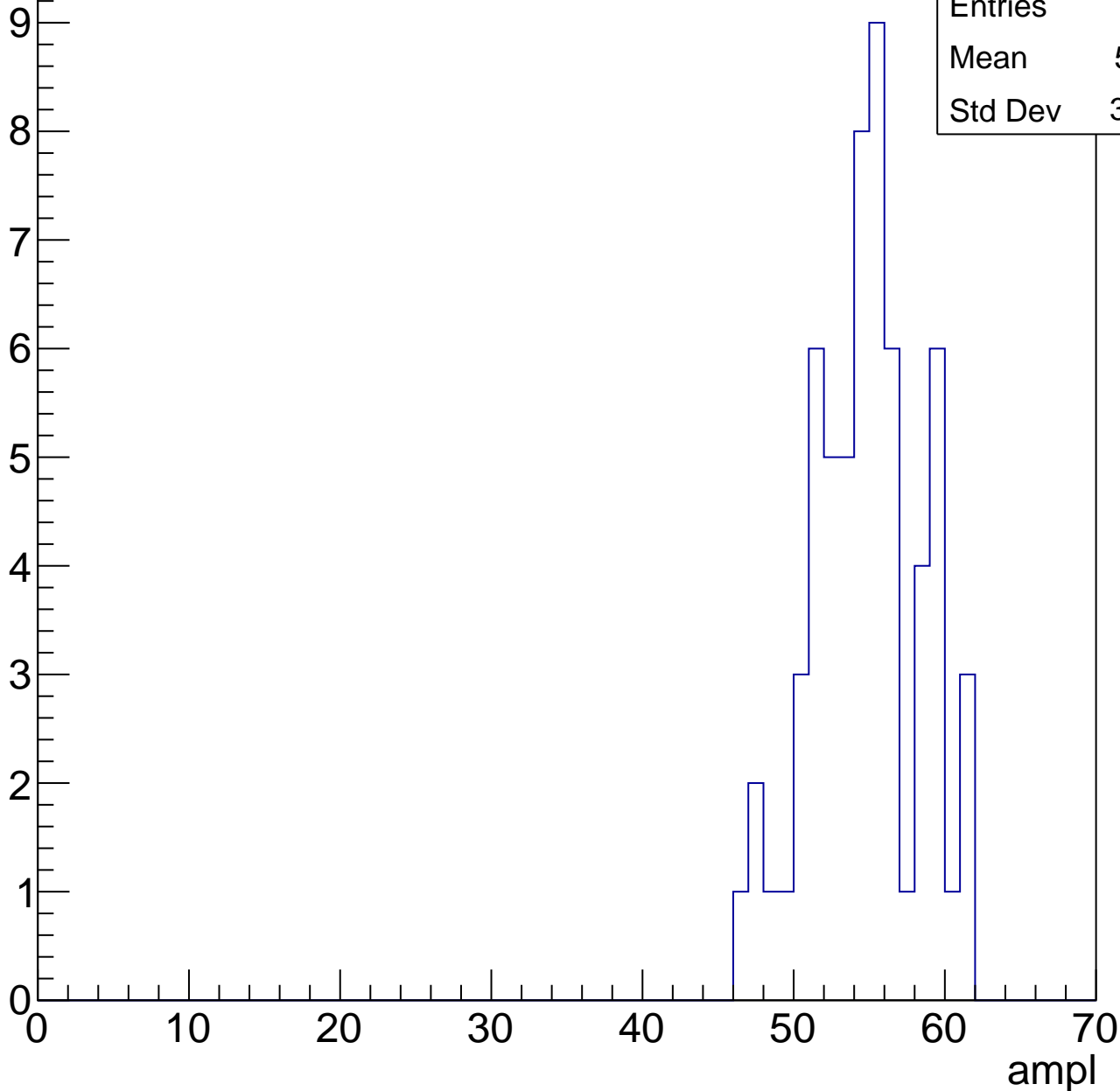


# B1L102S, U16-ch80, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

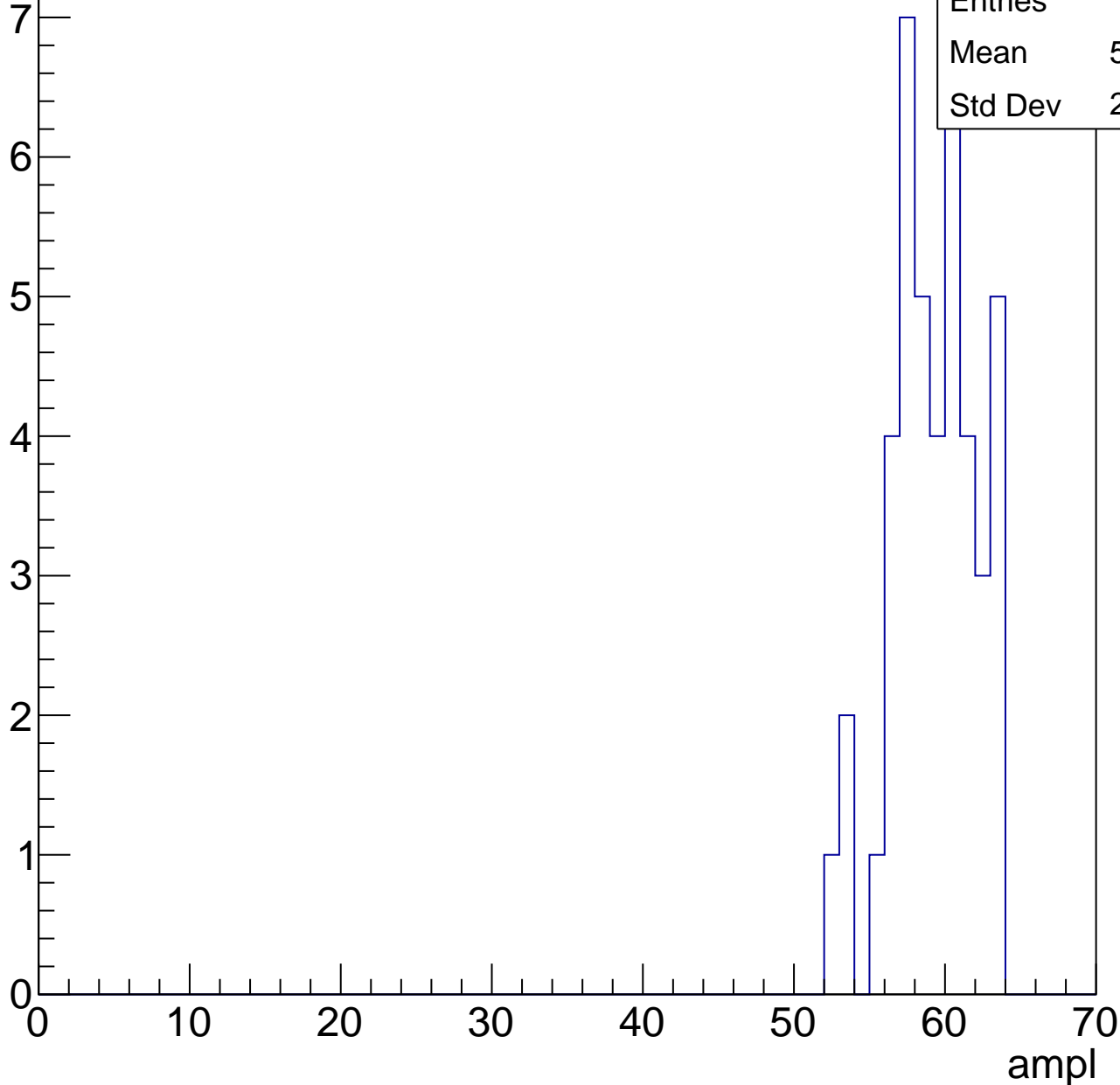
Entries	62
Mean	54.31
Std Dev	3.554



# B1L102S, U16-ch80, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

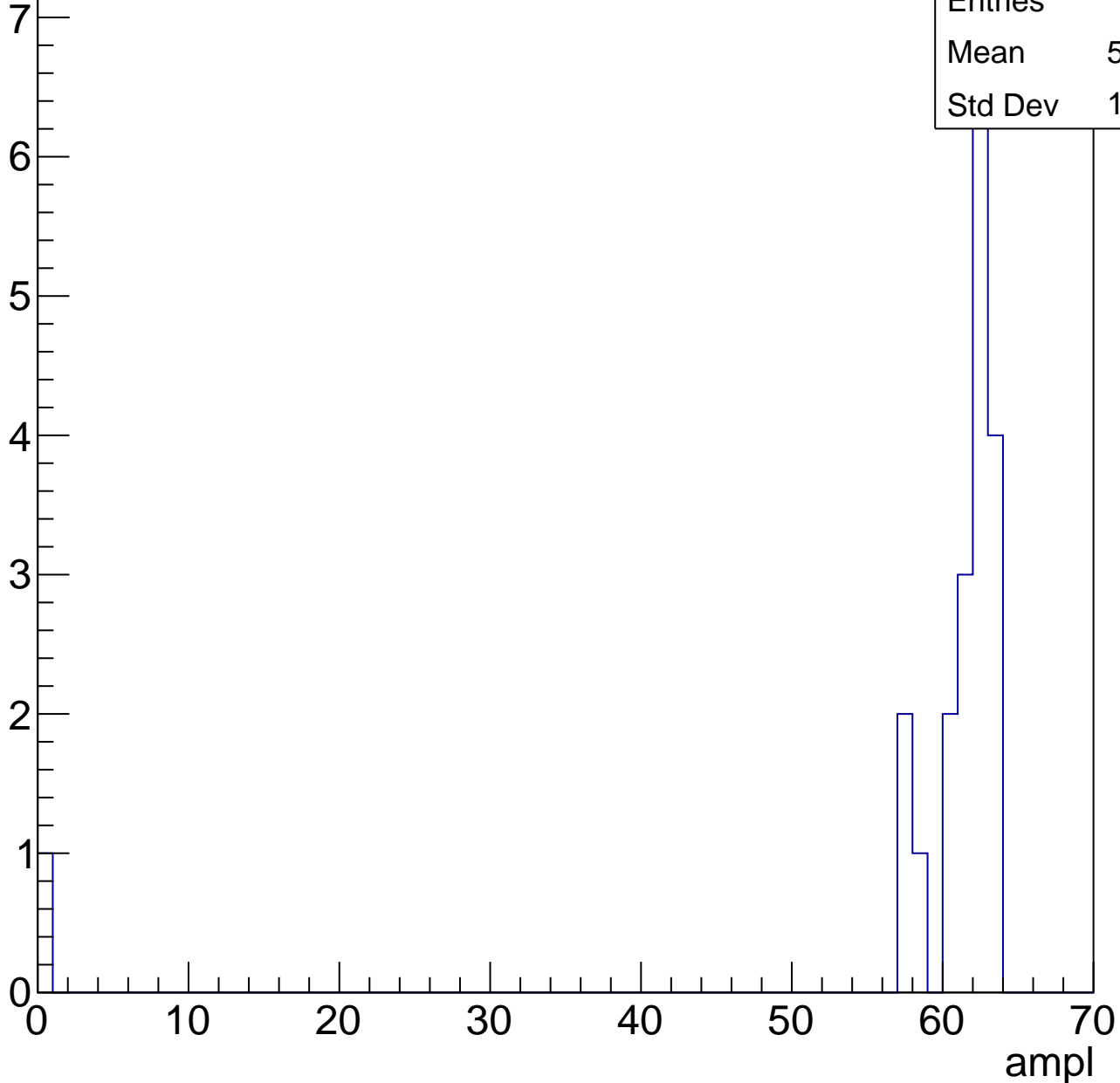


# B1L102S, U16-ch80, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	20
Mean	58.05
Std Dev	13.44





# B1L102S, U16-ch80, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch81, adc0

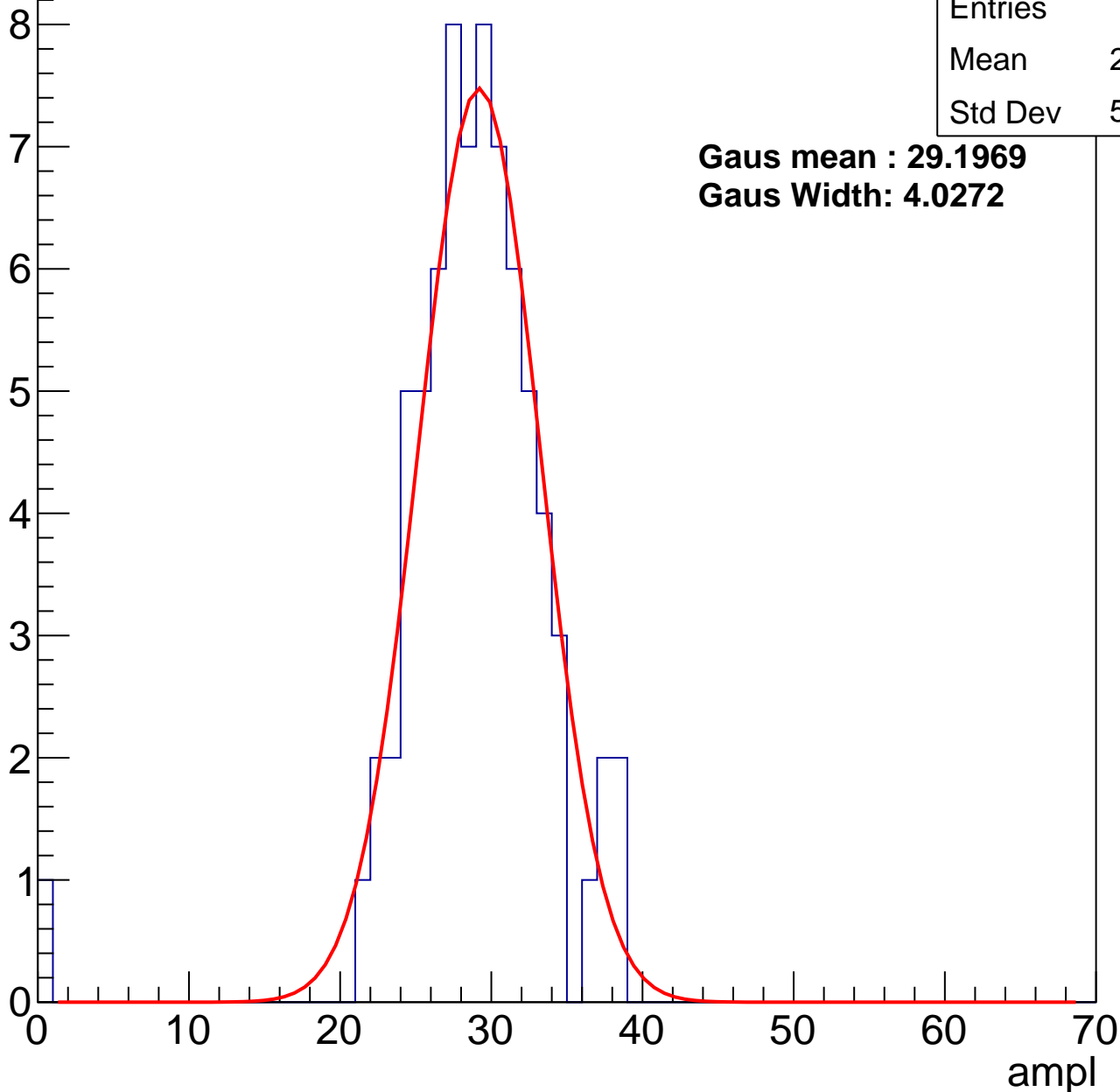
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	28.43
Std Dev	5.036

**Gaus mean : 29.1669**

**Gaus Width: 4.0272**



# B1L102S, U16-ch81, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	79
Mean	35.67
Std Dev	3.71

**Gaus mean : 36.8656**

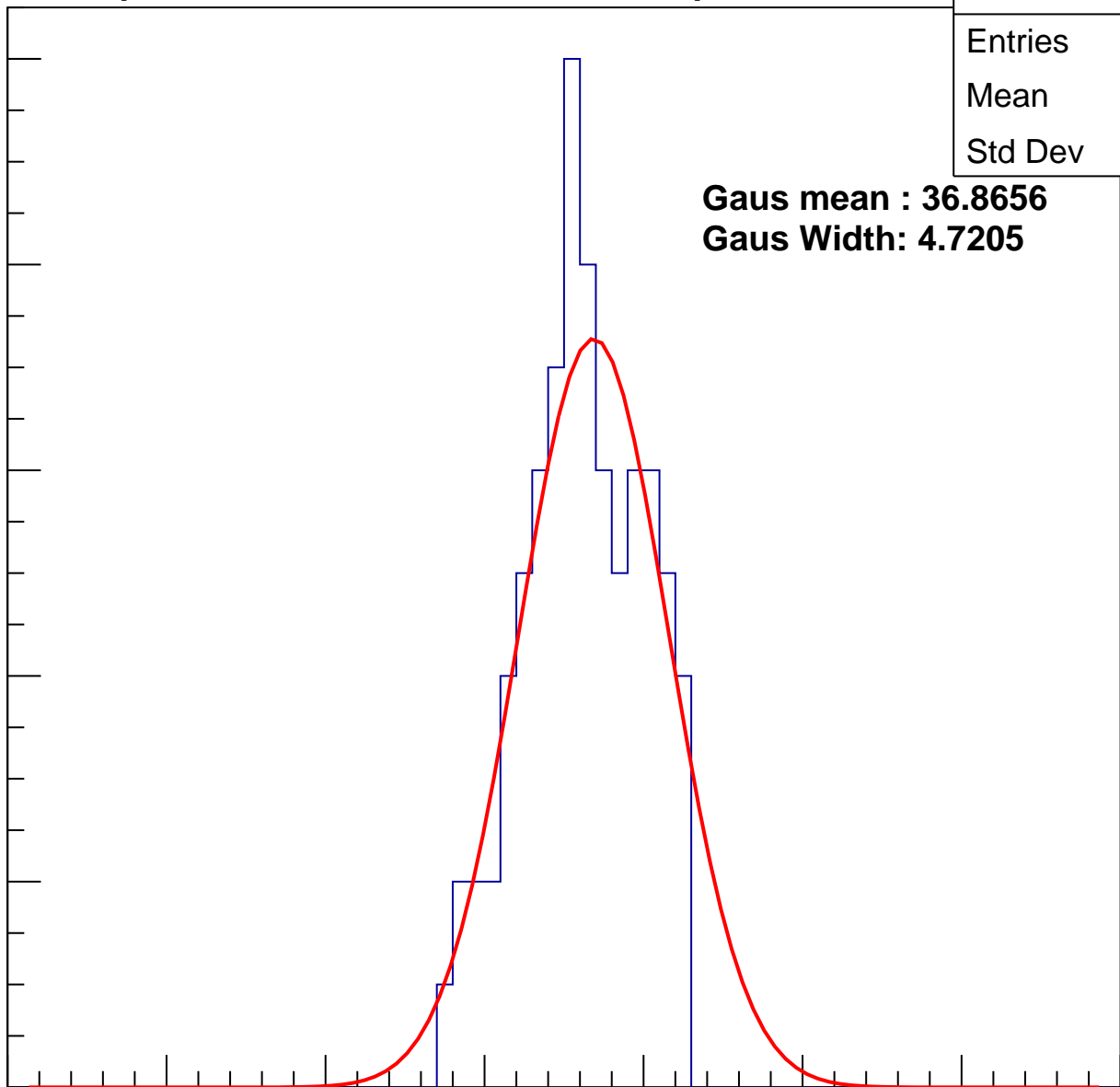
**Gaus Width: 4.7205**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U16-ch81, adc2

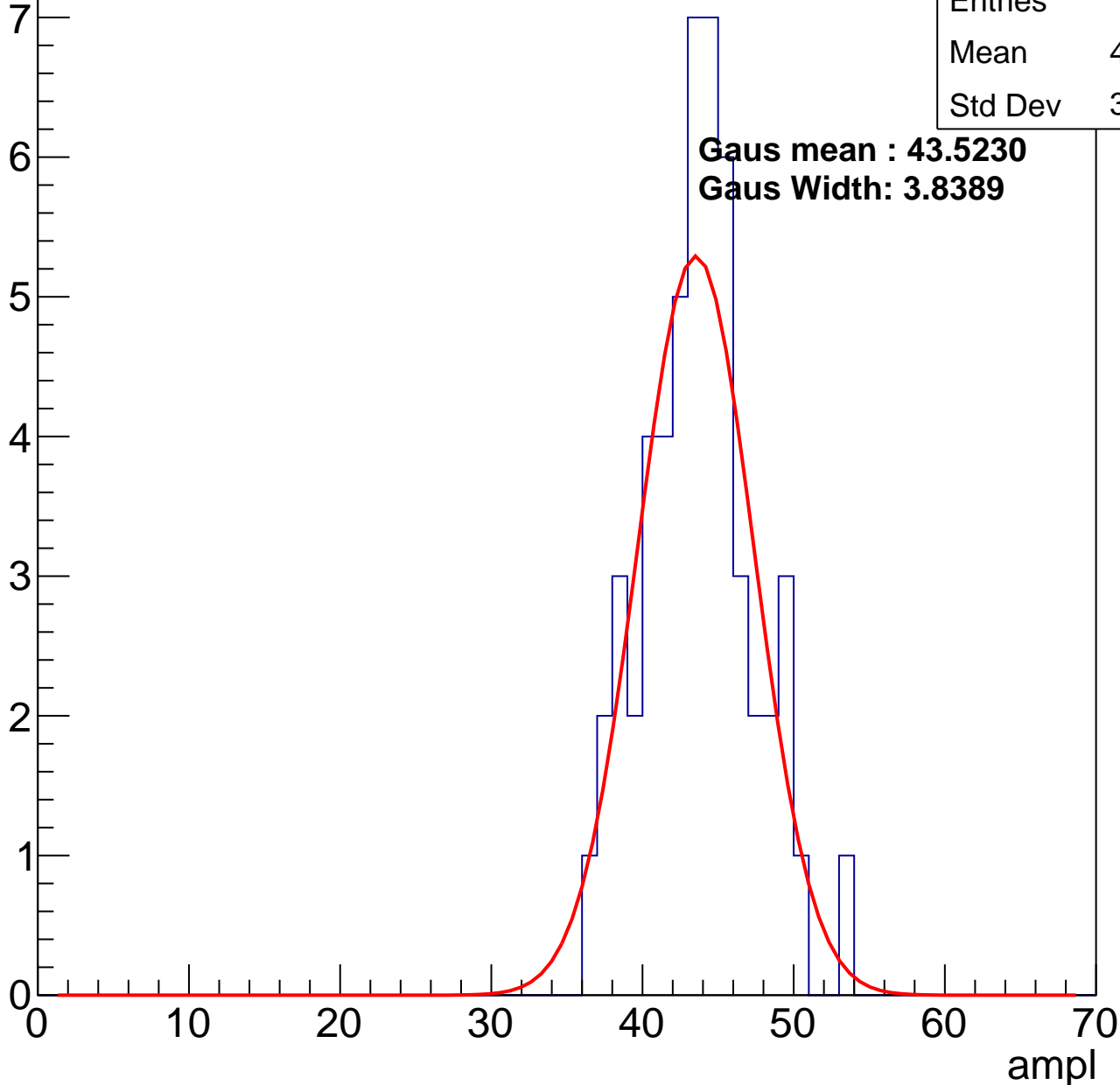
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	43.26
Std Dev	3.577

**Gaus mean : 43.5230**

**Gaus Width: 3.8389**

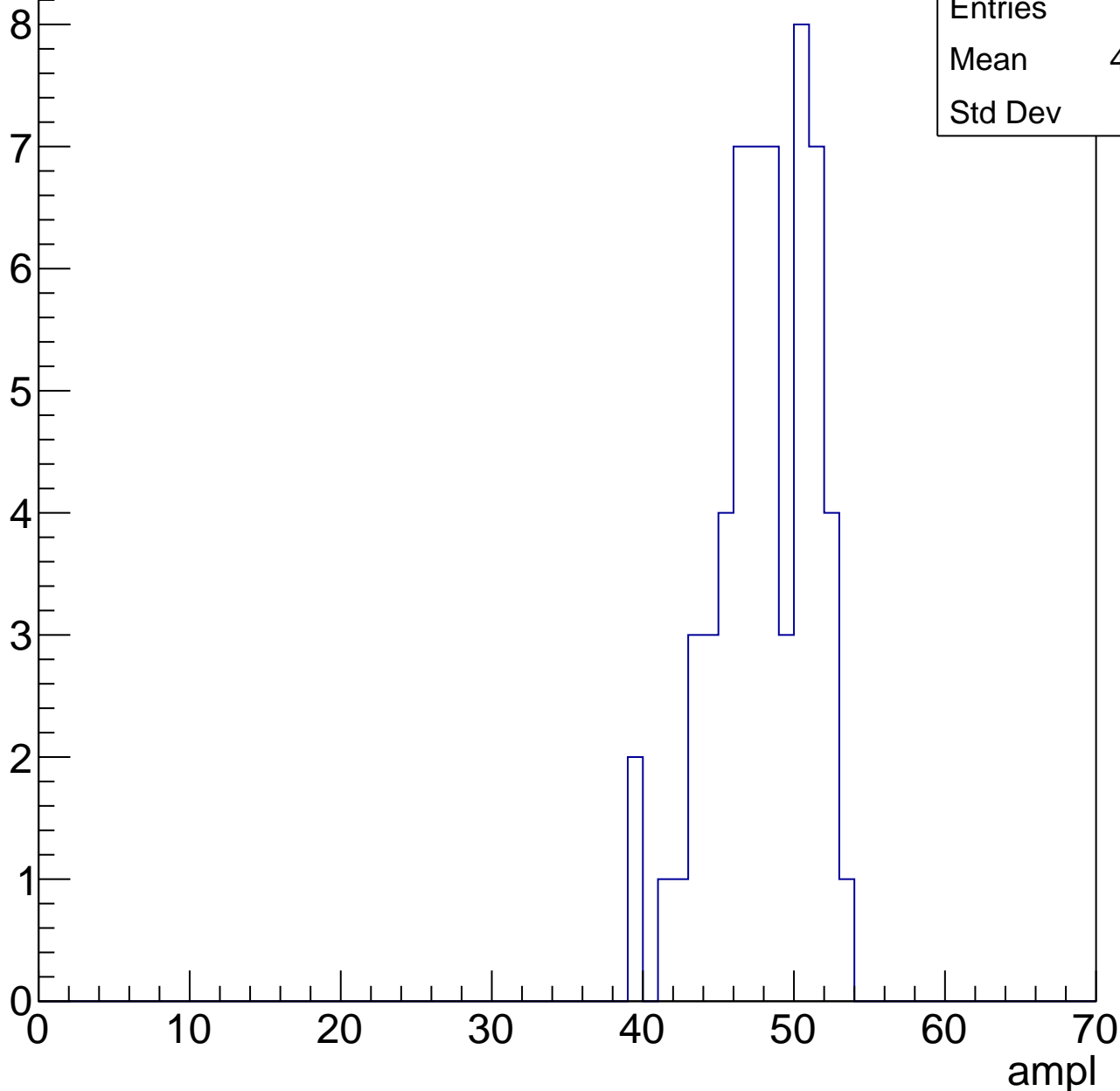


# B1L102S, U16-ch81, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	47.48
Std Dev	3.25

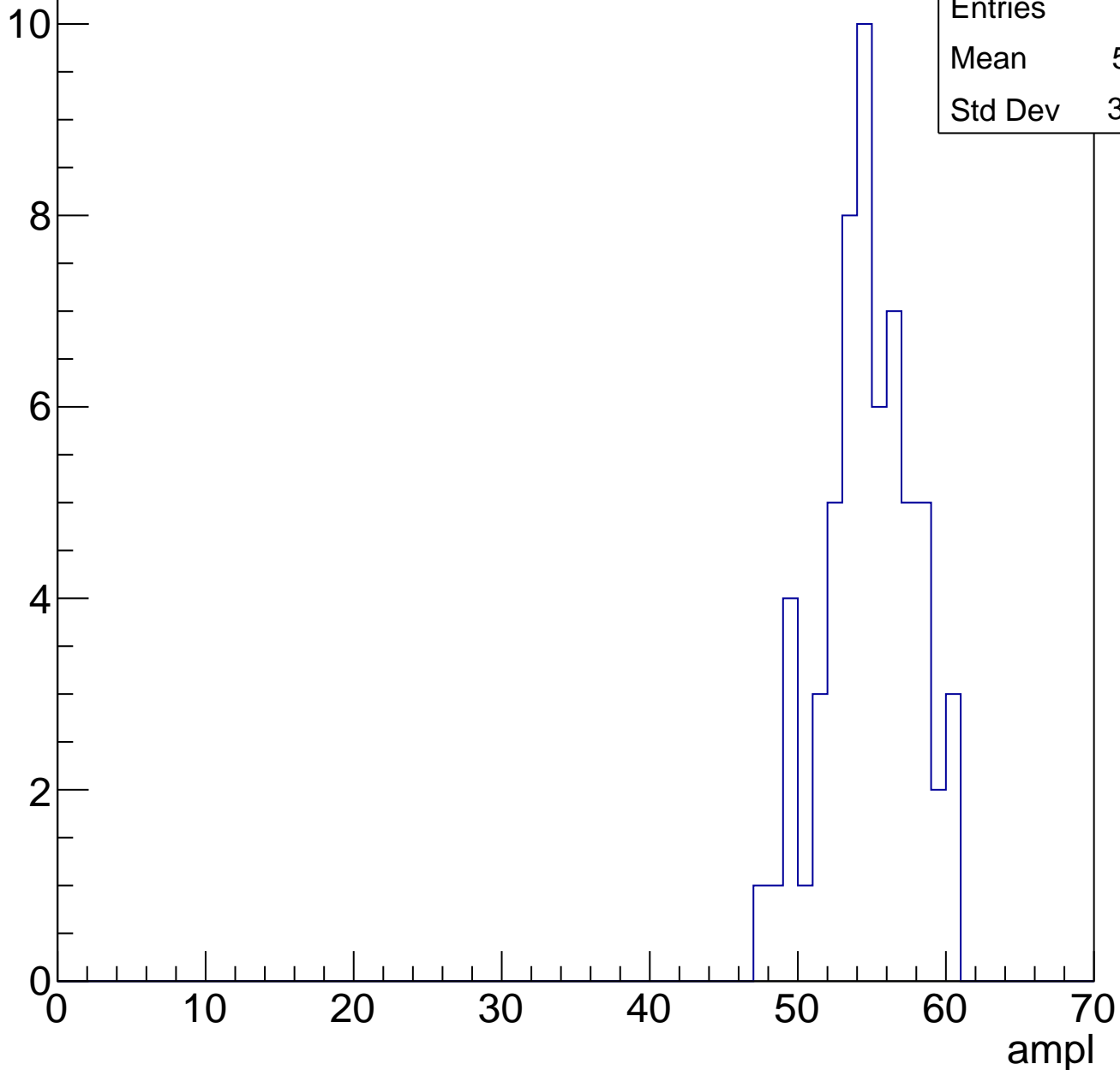


# B1L102S, U16-ch81, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	61
Mean	54.31
Std Dev	3.049

Entry

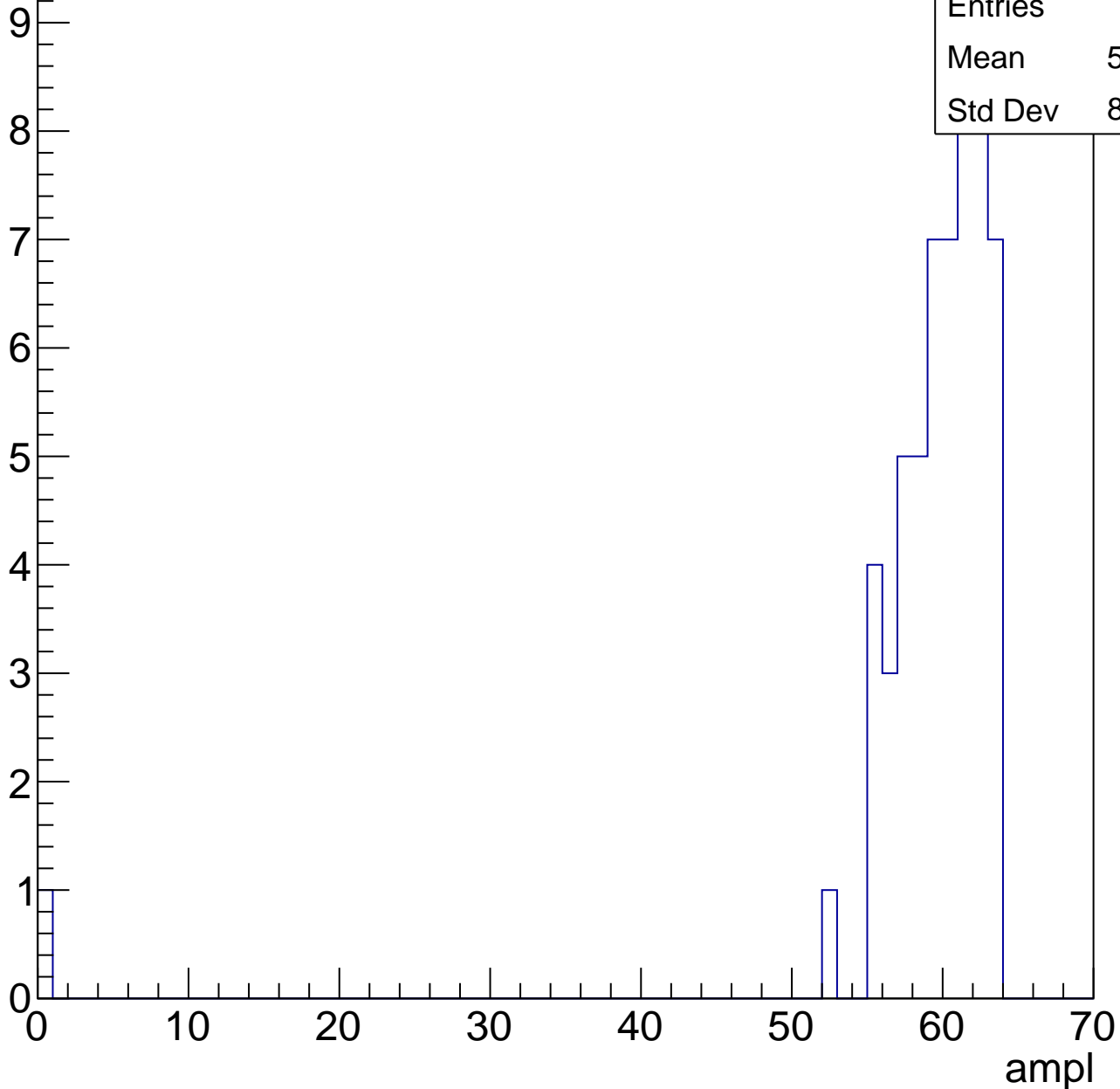


# B1L102S, U16-ch81, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	58.49
Std Dev	8.227



# B1L102S, U16-ch81, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch81, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch82, adc0

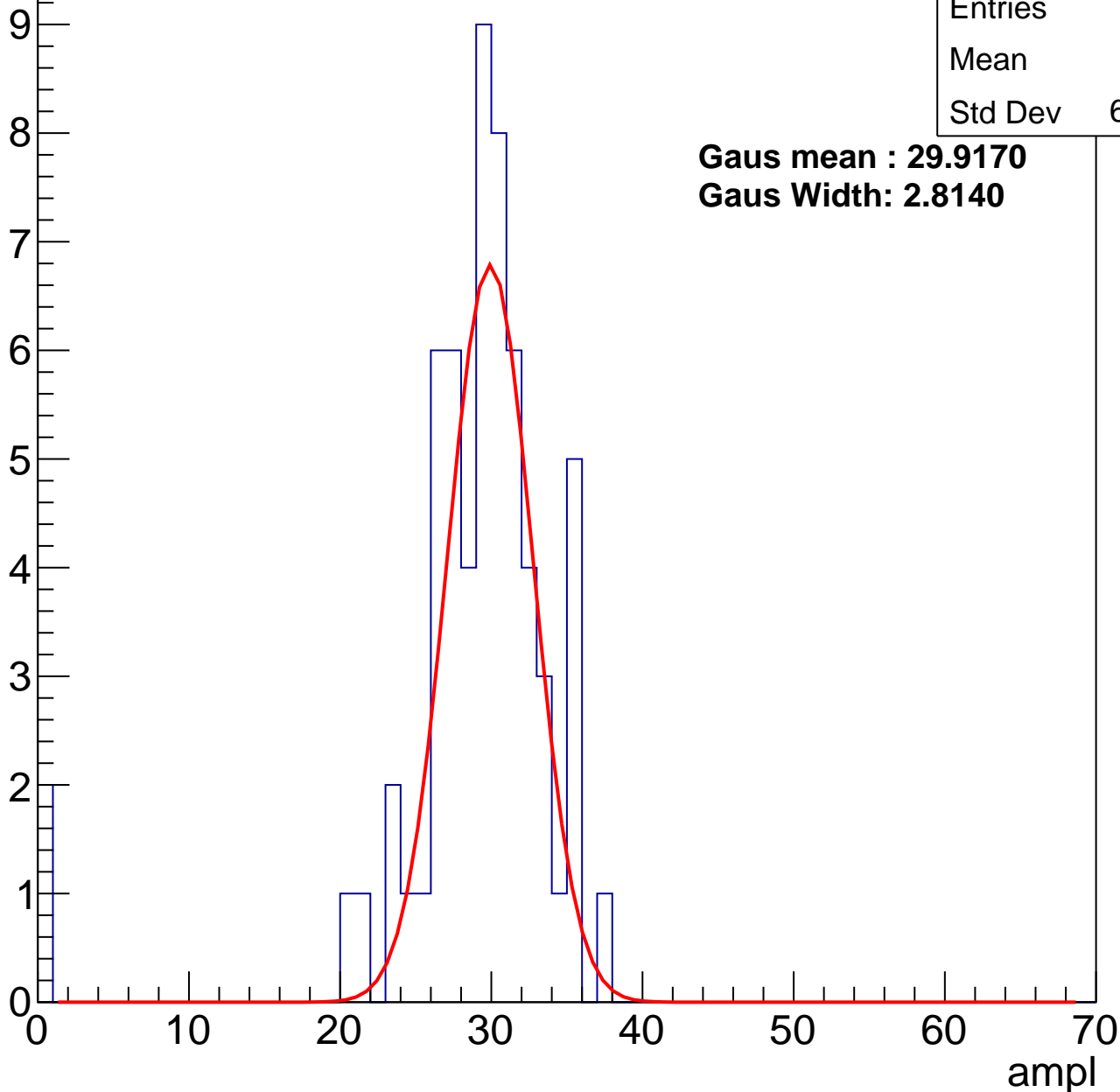
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	28.3
Std Dev	6.242

**Gaus mean : 29.9170**

**Gaus Width: 2.8140**



# B1L102S, U16-ch82, adc1

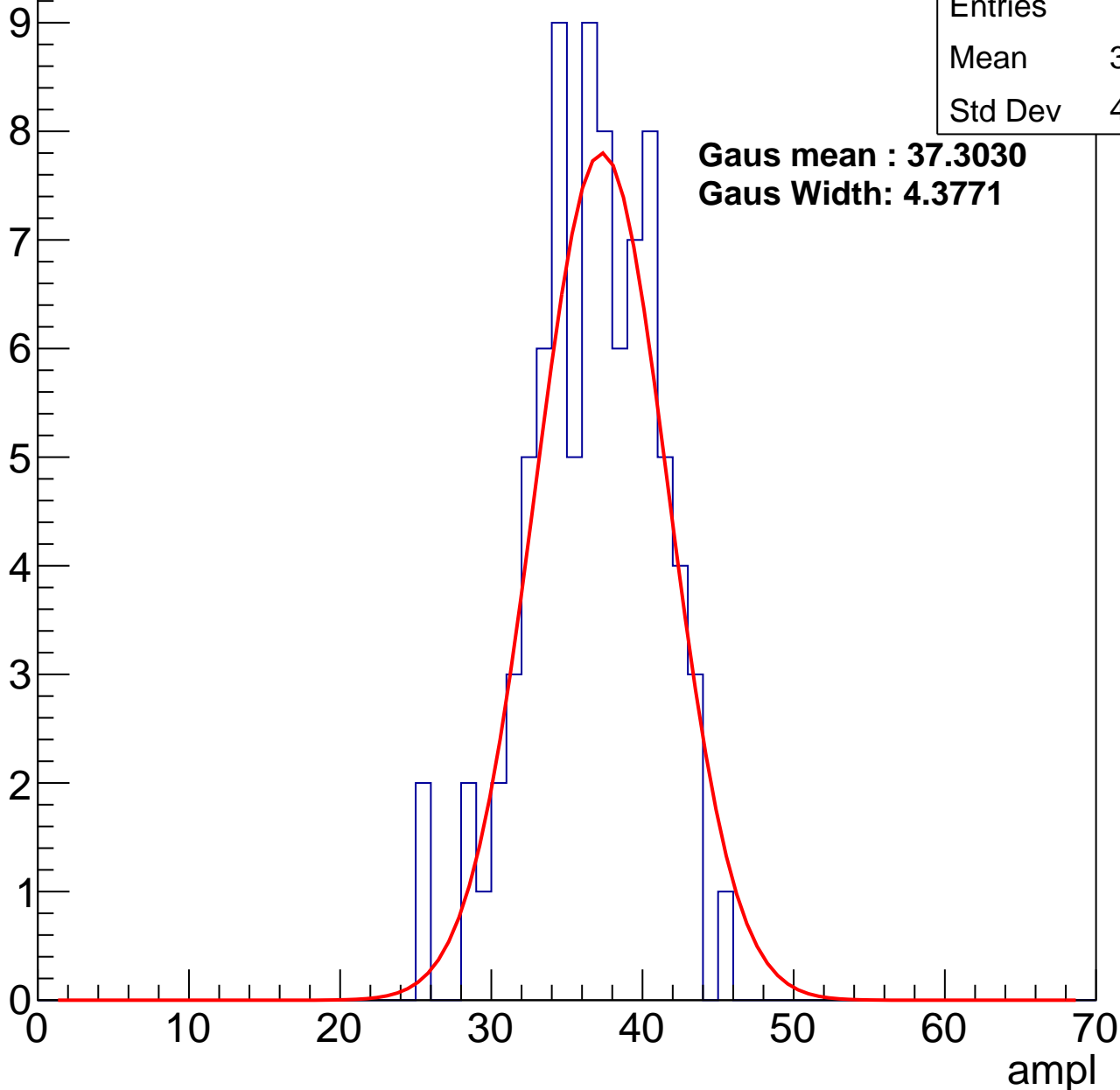
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	86
Mean	36.22
Std Dev	4.116

**Gaus mean : 37.3030**

**Gaus Width: 4.3771**



# B1L102S, U16-ch82, adc2

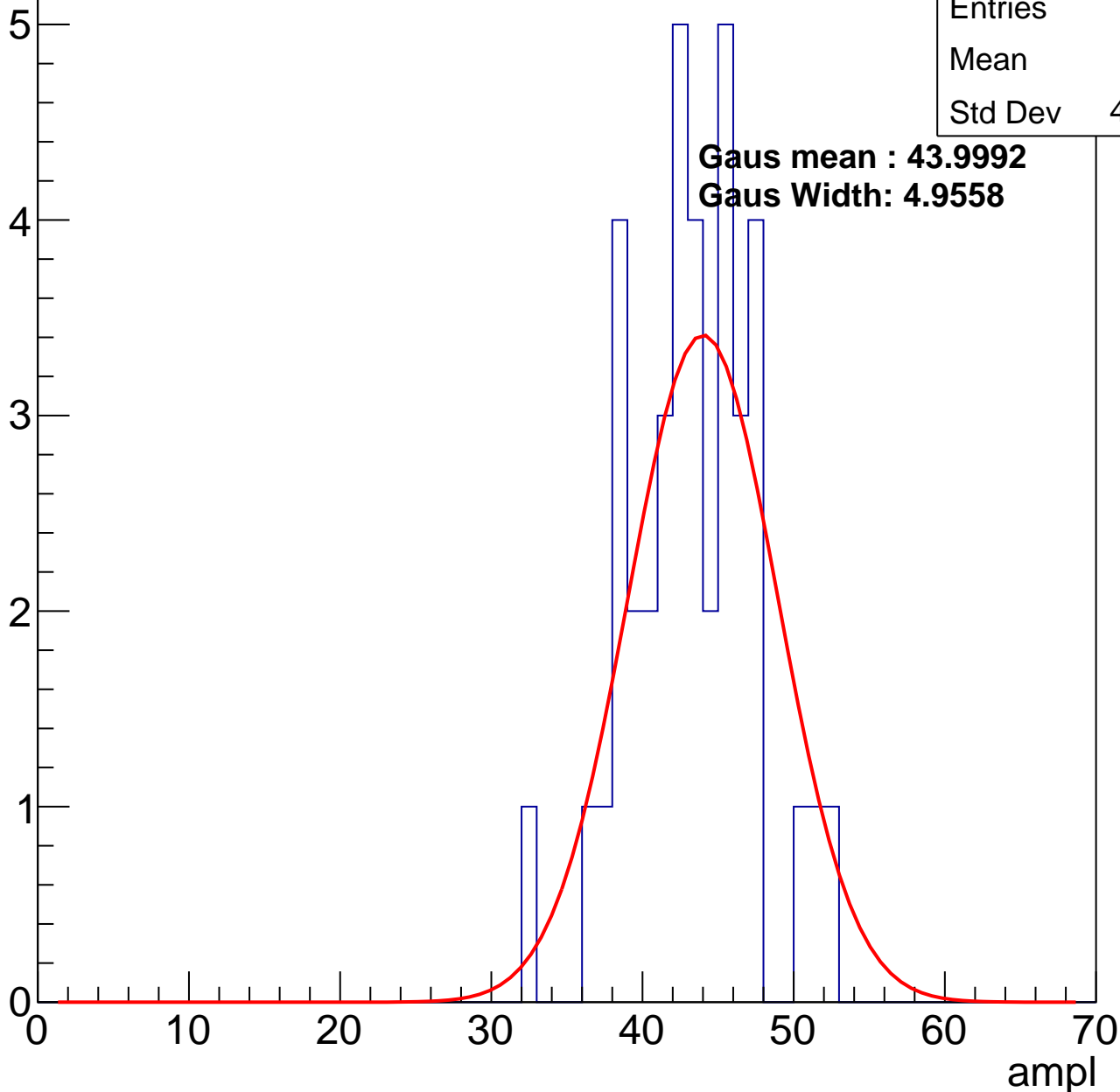
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	42.8
Std Dev	4.118

**Gaus mean : 43.9992**

**Gaus Width: 4.9558**



# B1L102S, U16-ch82, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	88
Mean	49.16
Std Dev	4.39

Entry

10

8

6

4

2

0

0

10

20

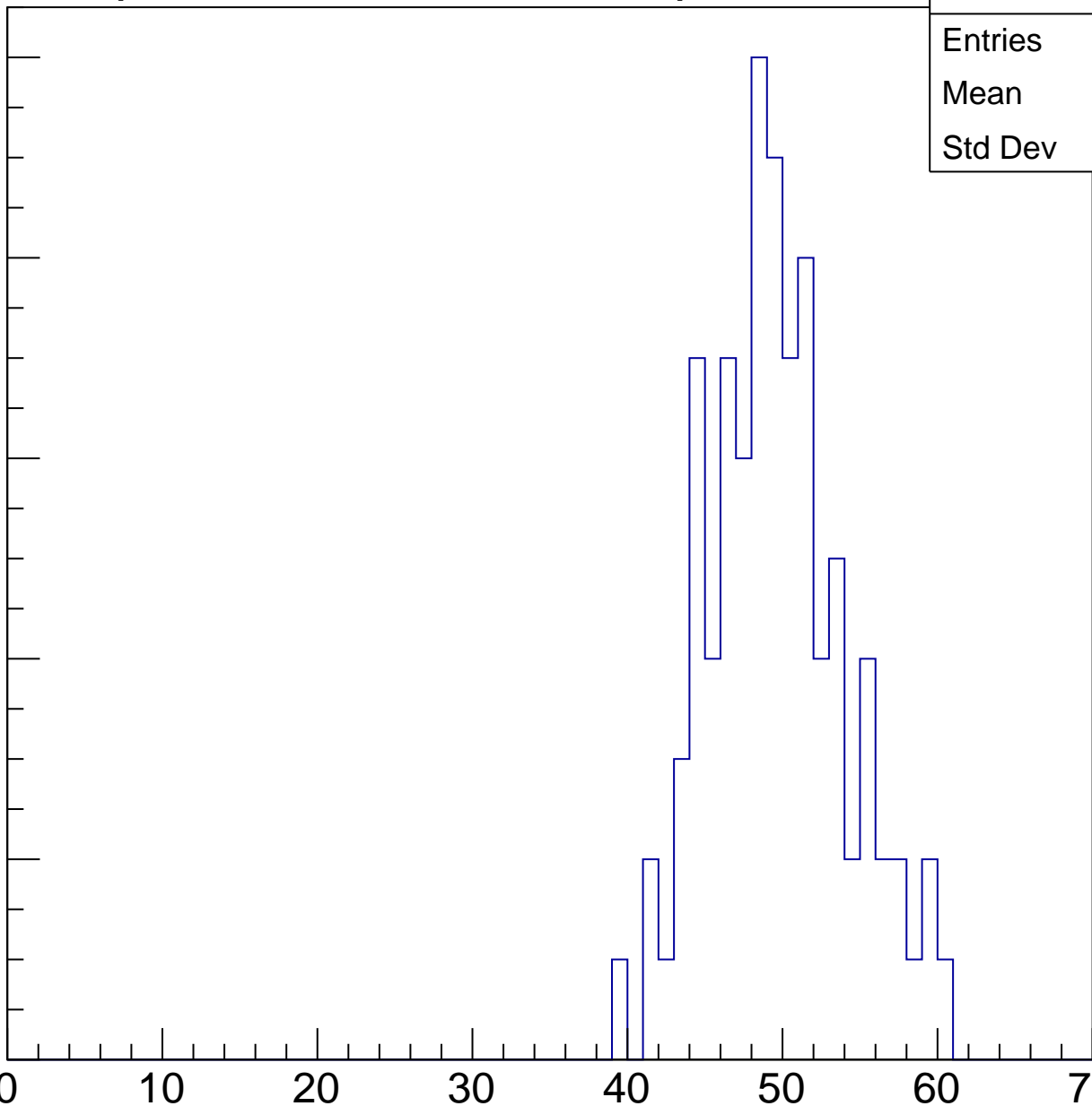
30

40

50

60

ampl

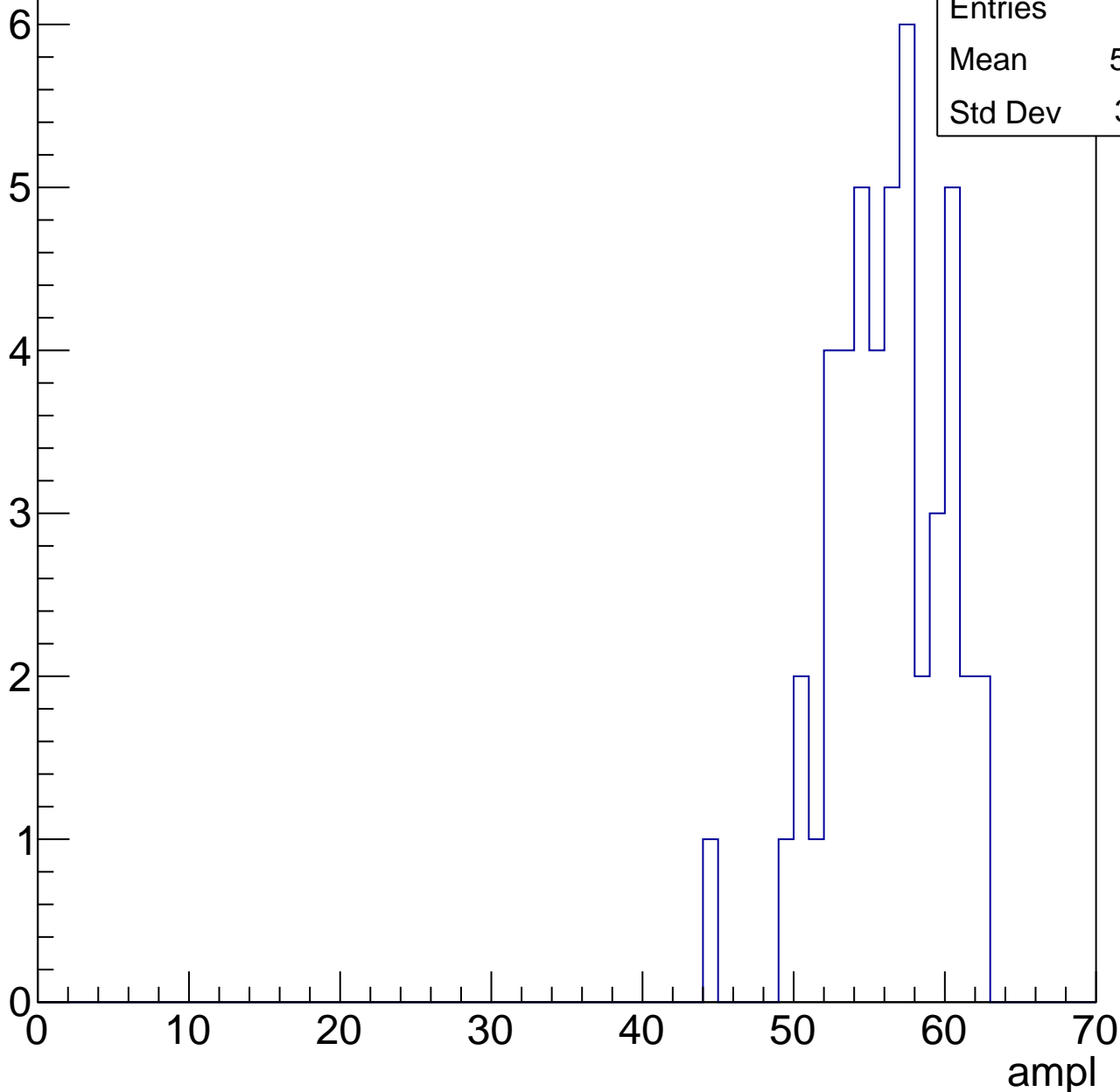


# B1L102S, U16-ch82, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	55.64
Std Dev	3.721



# B1L102S, U16-ch82, adc5

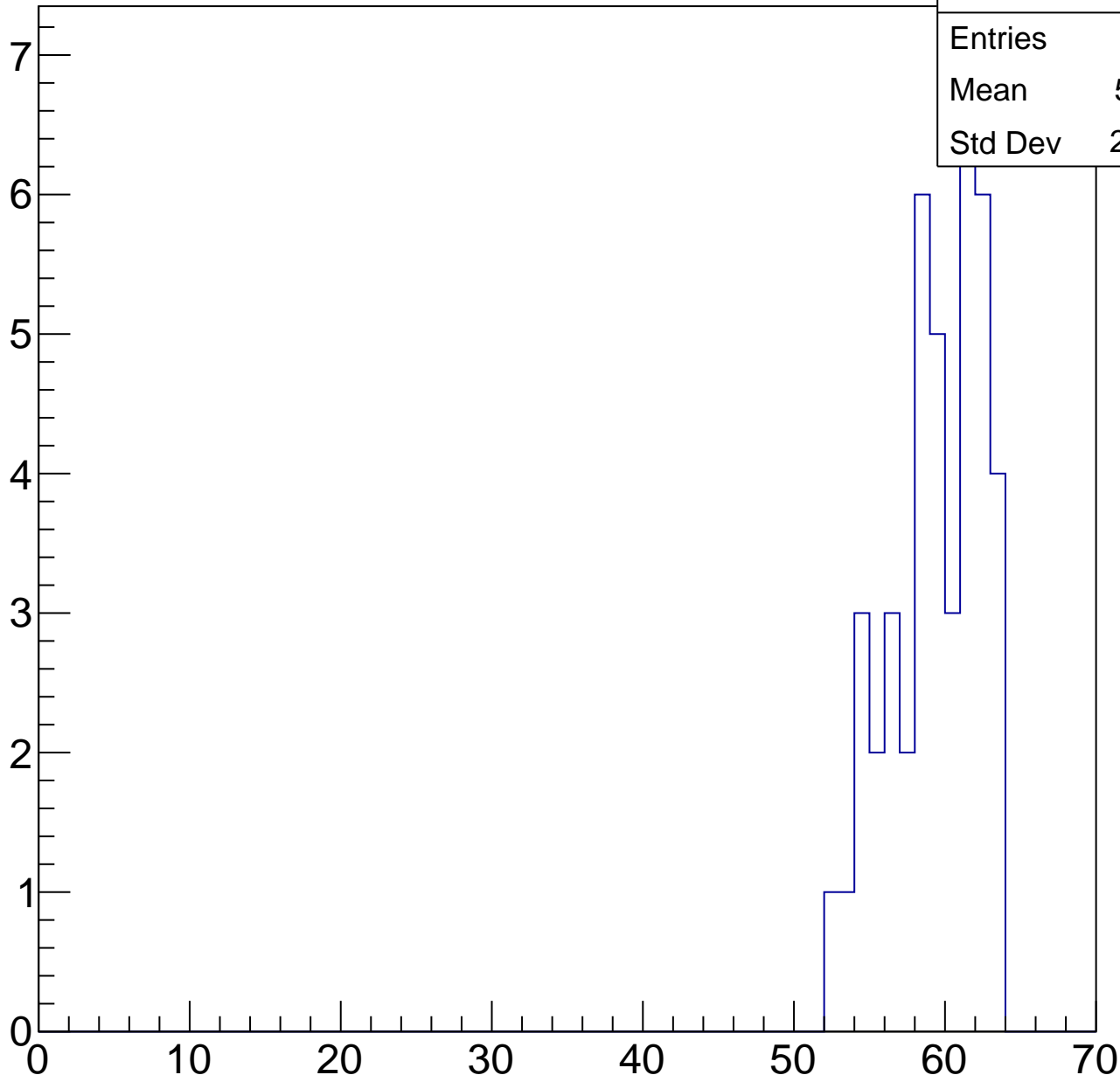
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	43
Mean	58.91
Std Dev	2.979

ampl

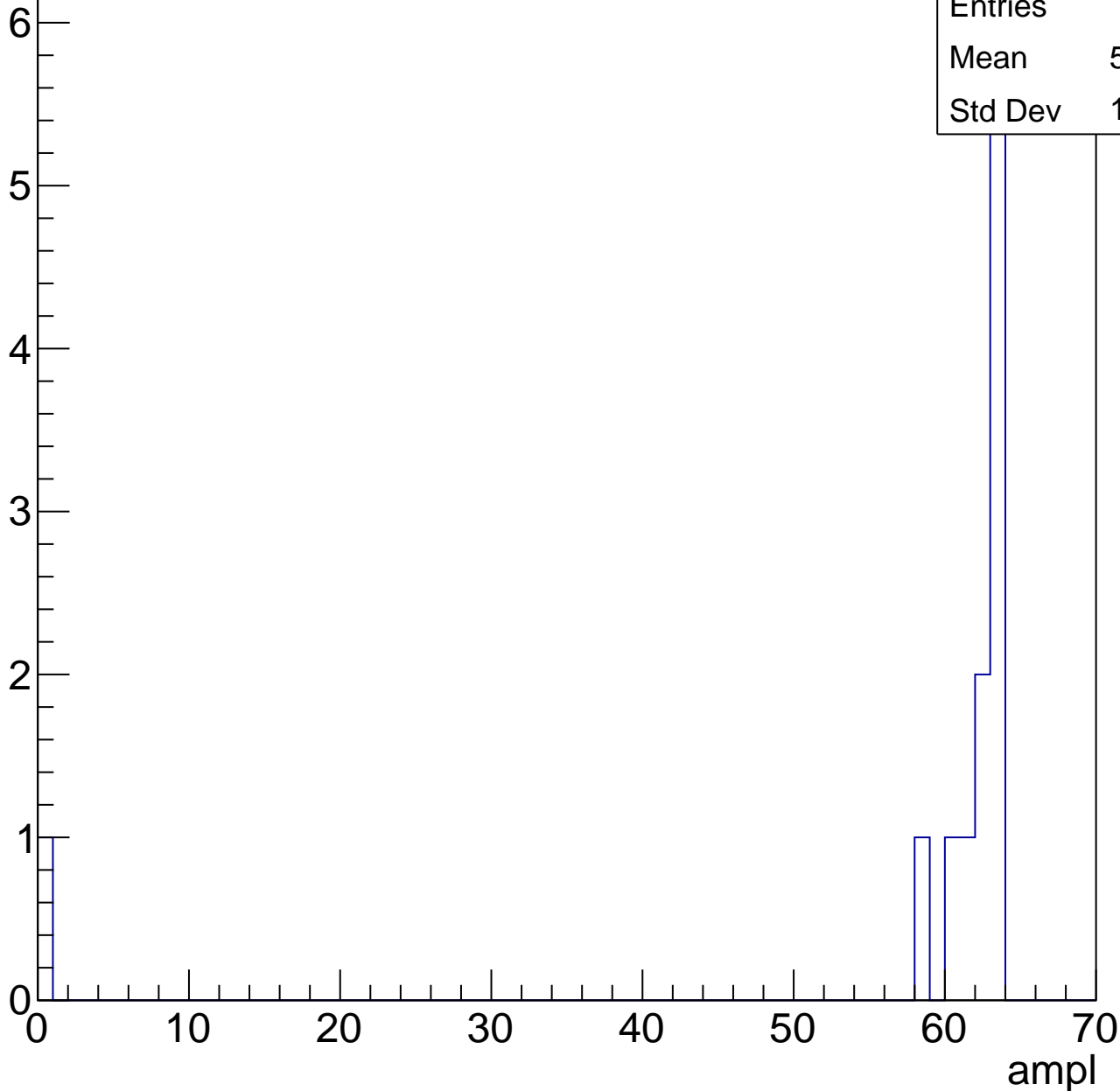


# B1L102S, U16-ch82, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	12
Mean	56.75
Std Dev	17.18

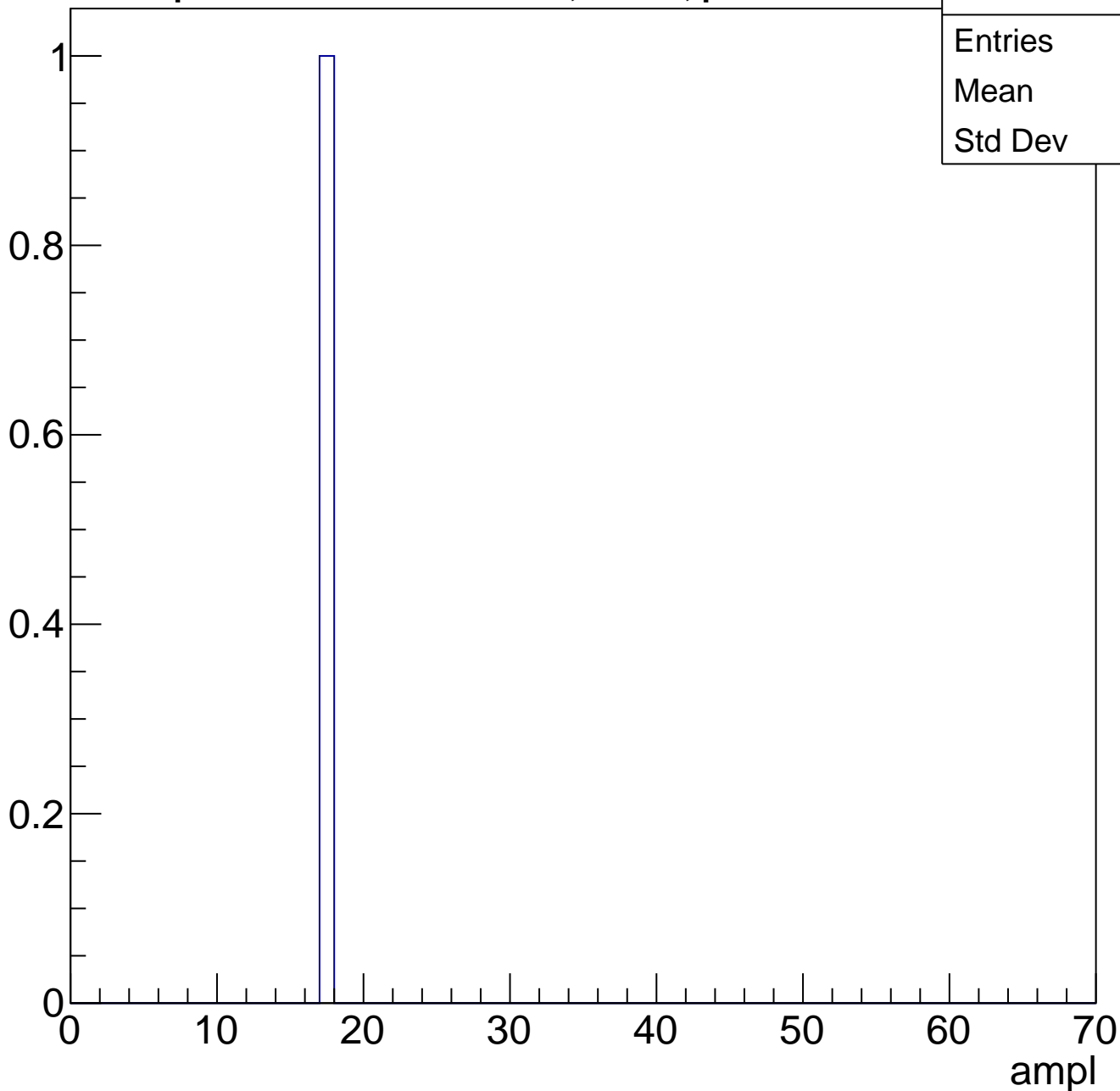




# B1L102S, U16-ch82, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch83, adc0

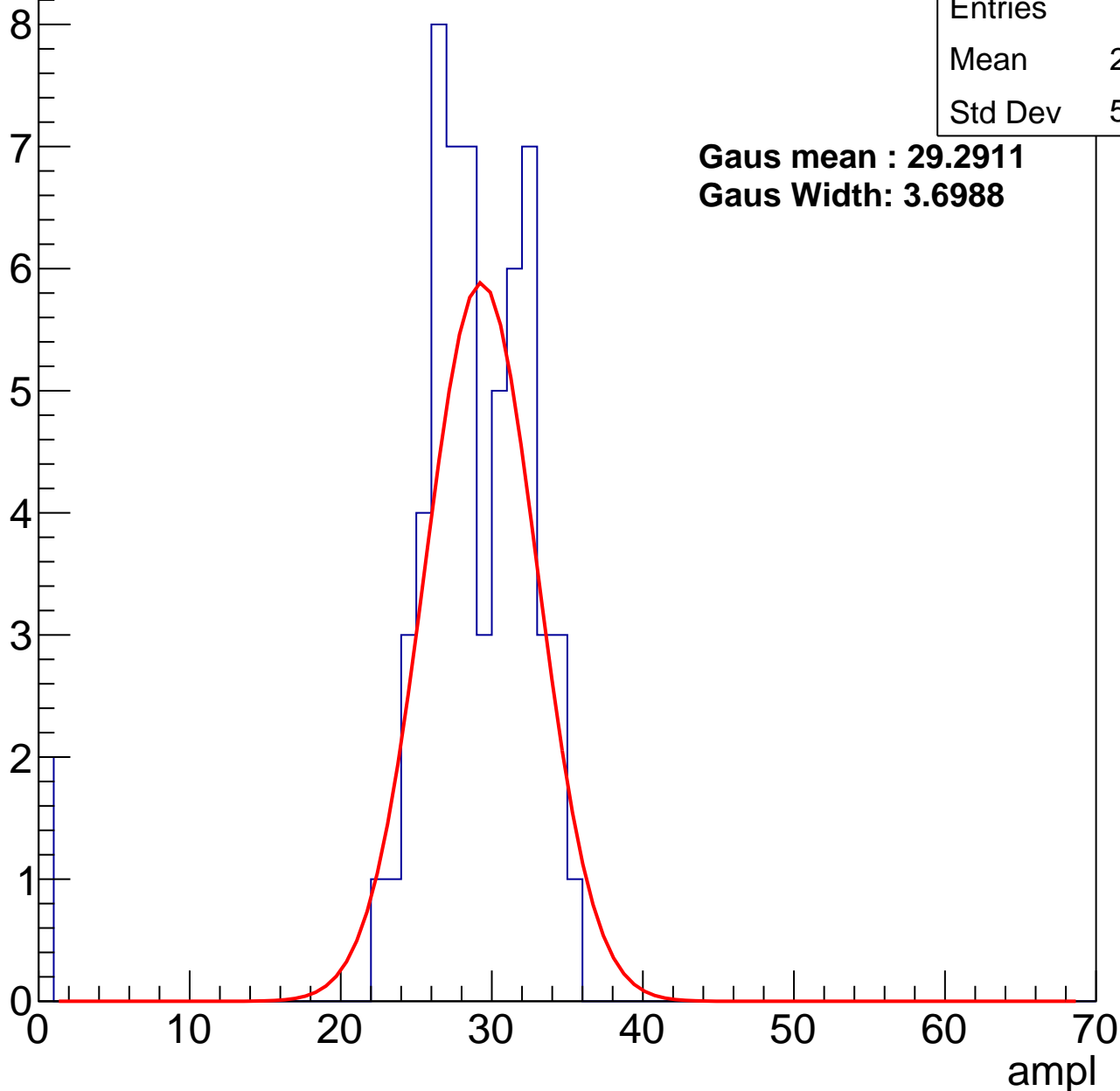
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	27.75
Std Dev	5.963

**Gaus mean : 29.2911**

**Gaus Width: 3.6988**



# B1L102S, U16-ch83, adc1

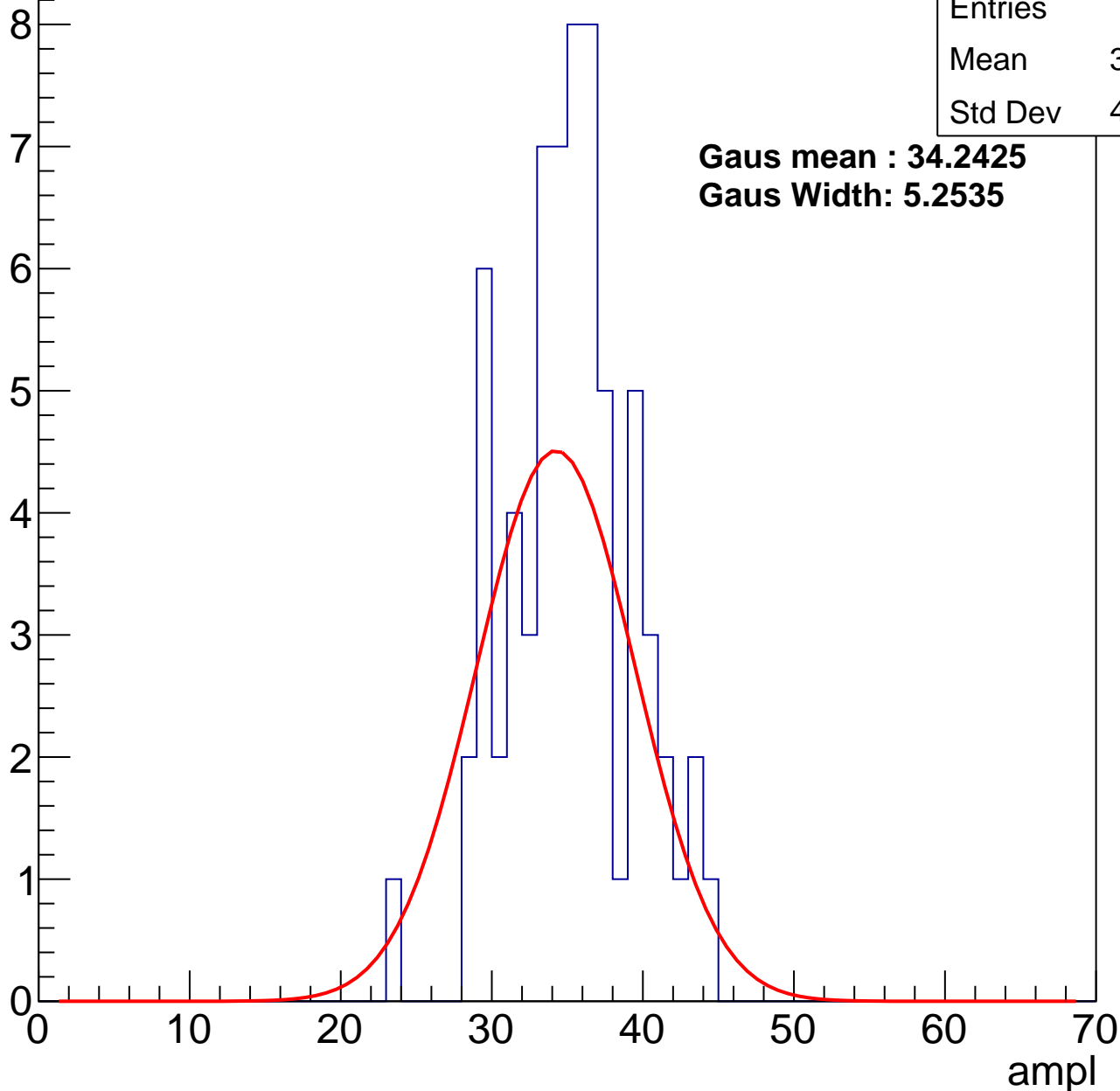
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	34.74
Std Dev	4.115

**Gaus mean : 34.2425**

**Gaus Width: 5.2535**



# B1L102S, U16-ch83, adc2

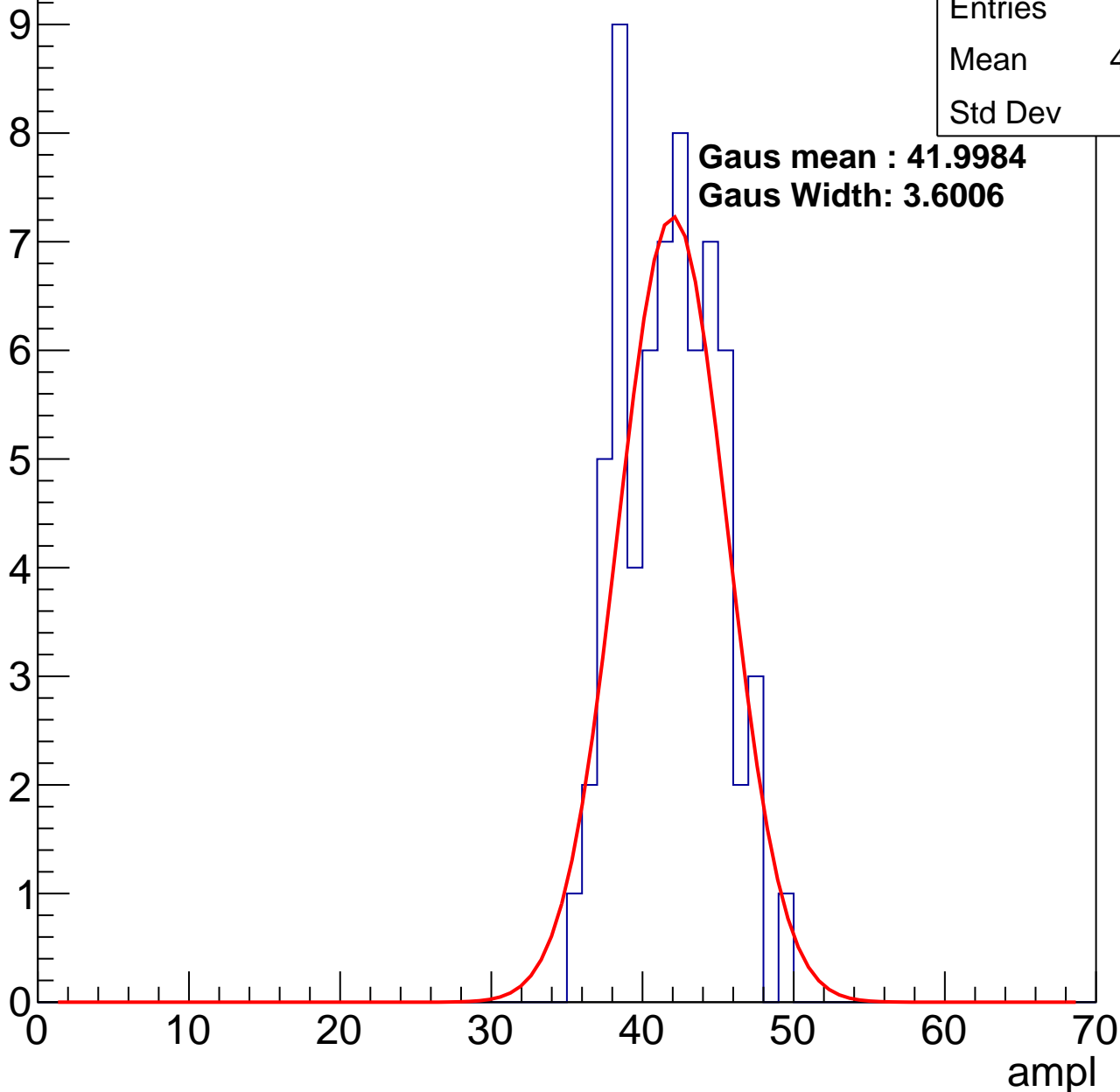
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	41.36
Std Dev	3.17

**Gaus mean : 41.9984**

**Gaus Width: 3.6006**

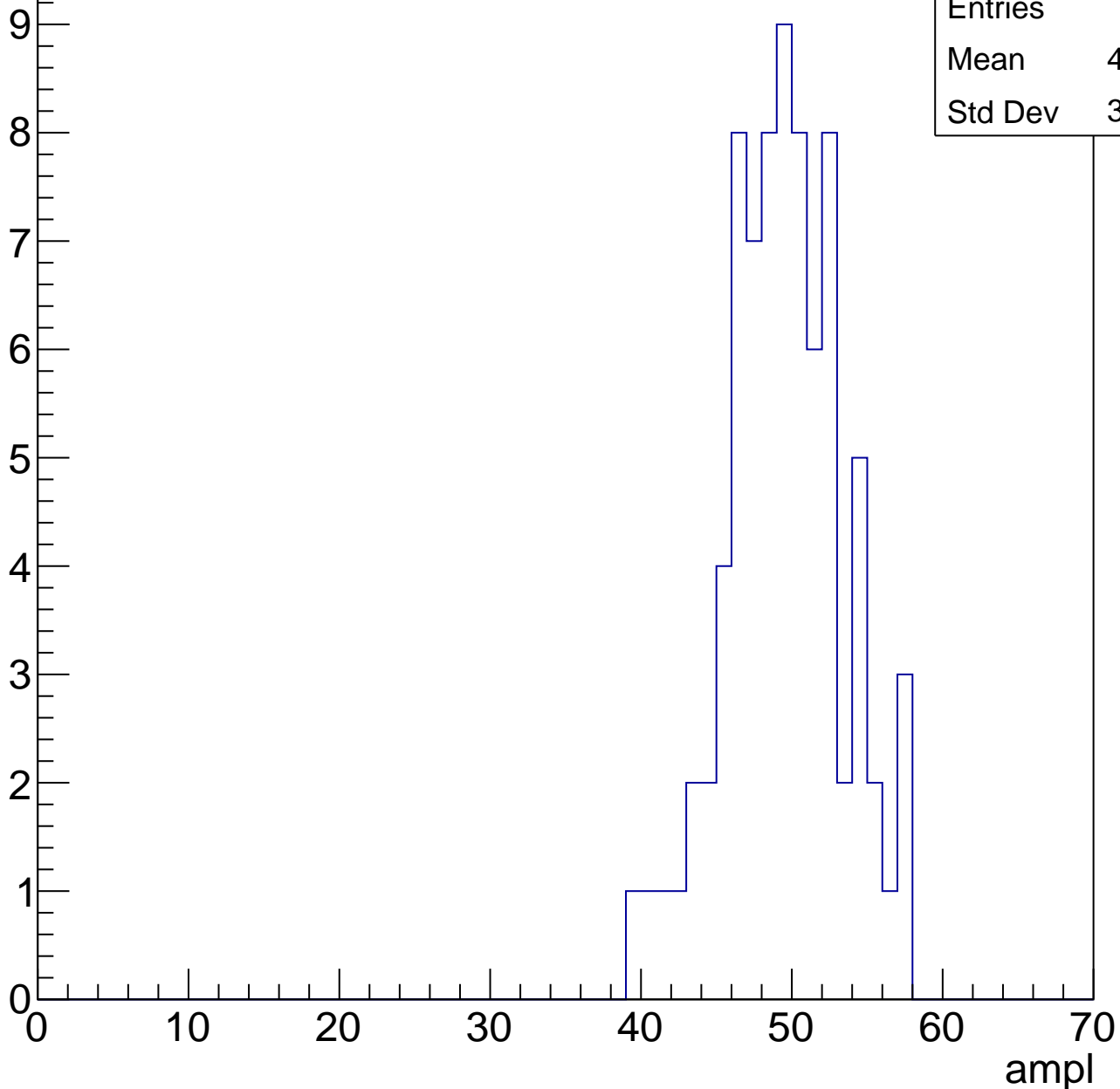


# B1L102S, U16-ch83, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

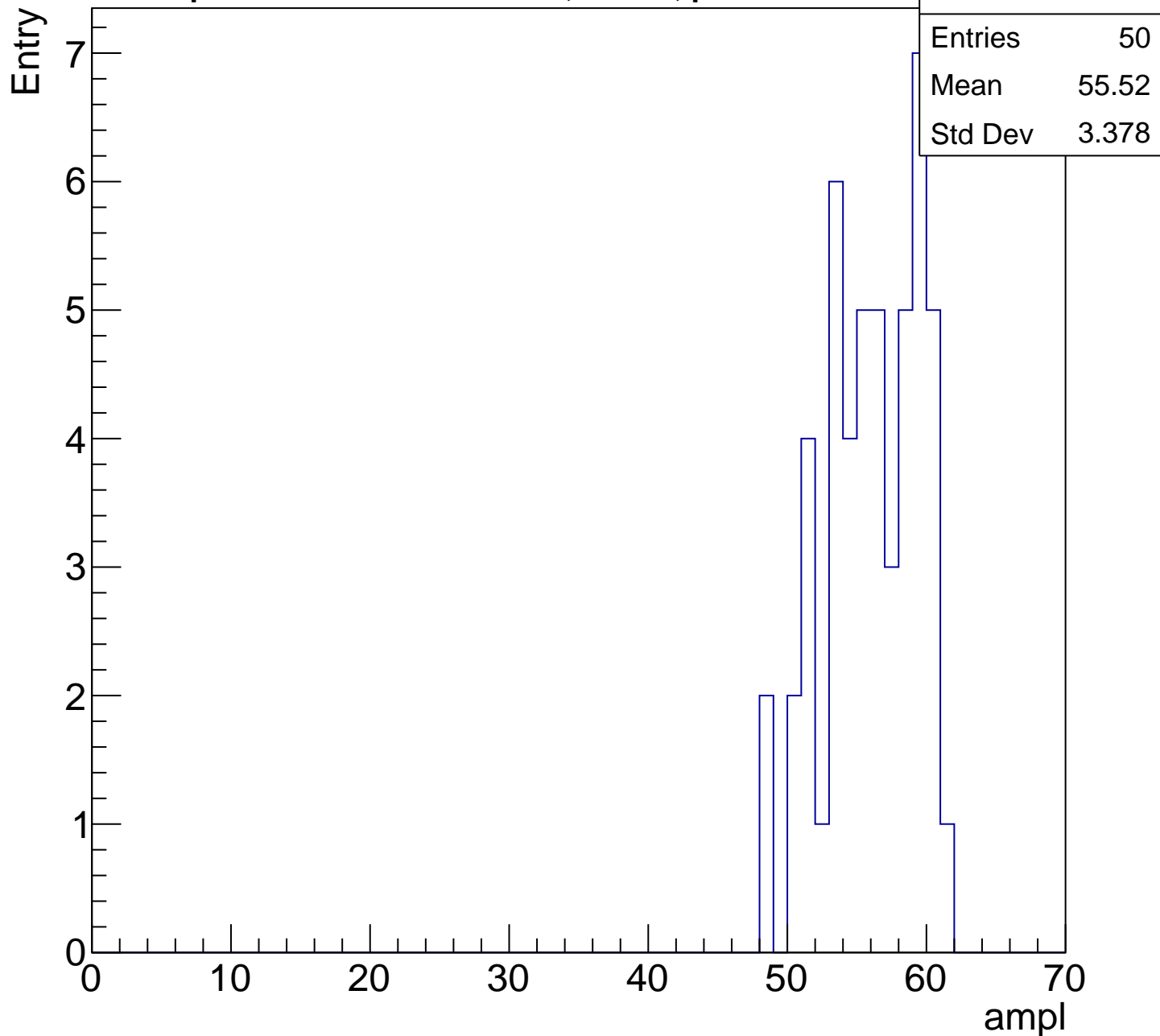
Entry

Entries	79
Mean	49.03
Std Dev	3.835



# B1L102S, U16-ch83, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

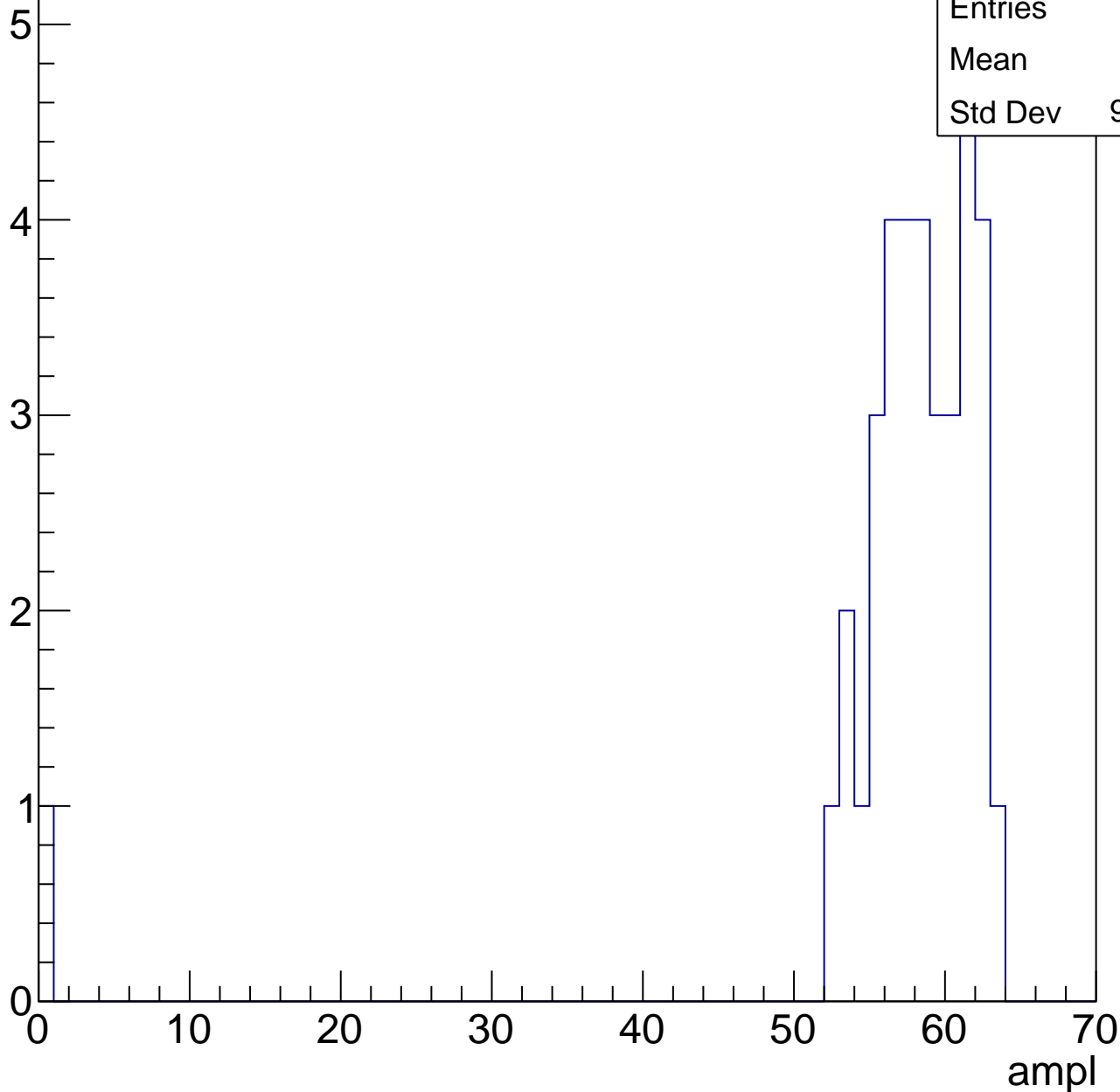


# B1L102S, U16-ch83, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	36
Mean	56.5
Std Dev	9.974

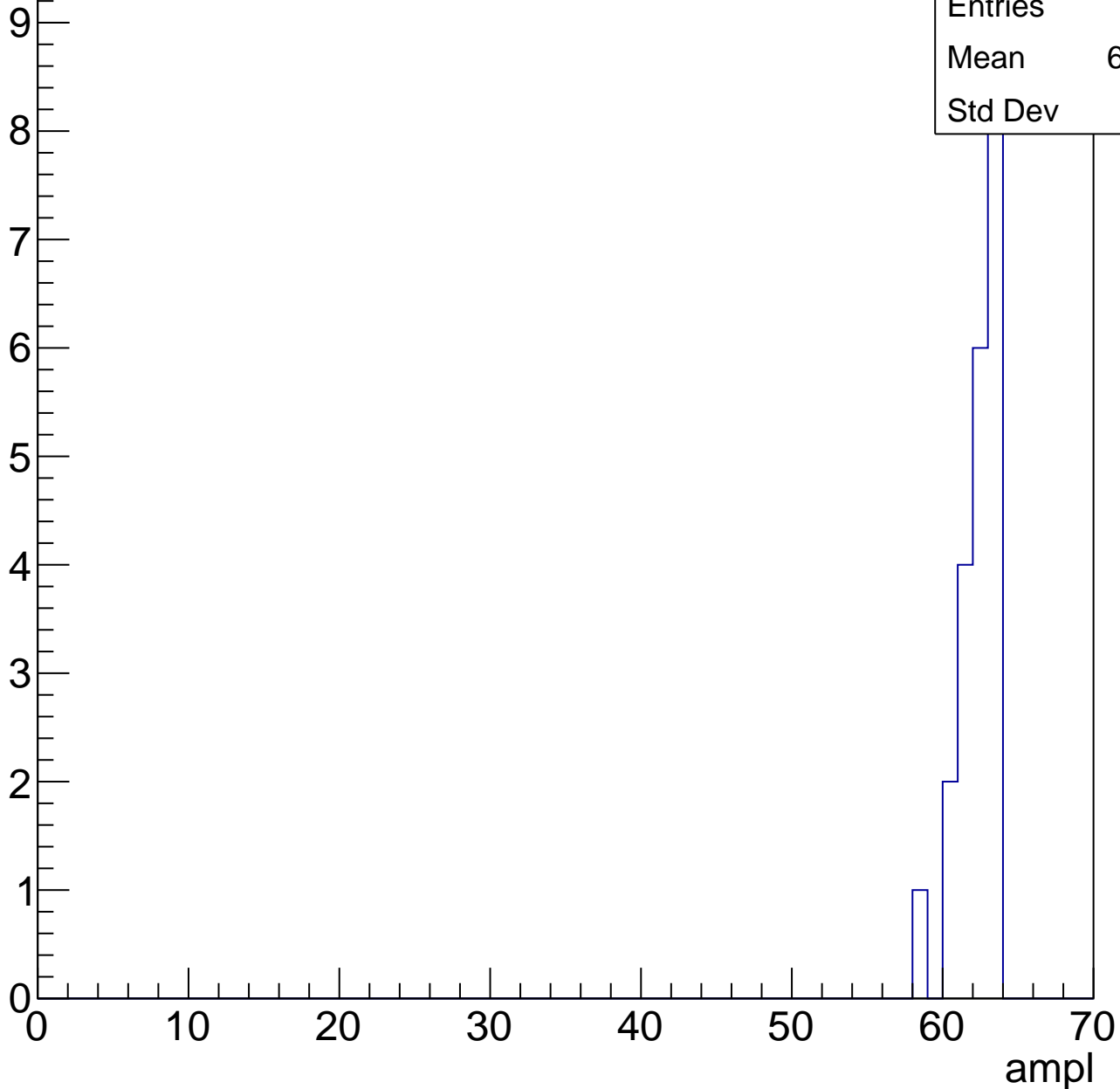


# B1L102S, U16-ch83, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	22
Mean	61.86
Std Dev	1.29





# B1L102S, U16-ch83, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U16-ch84, adc0

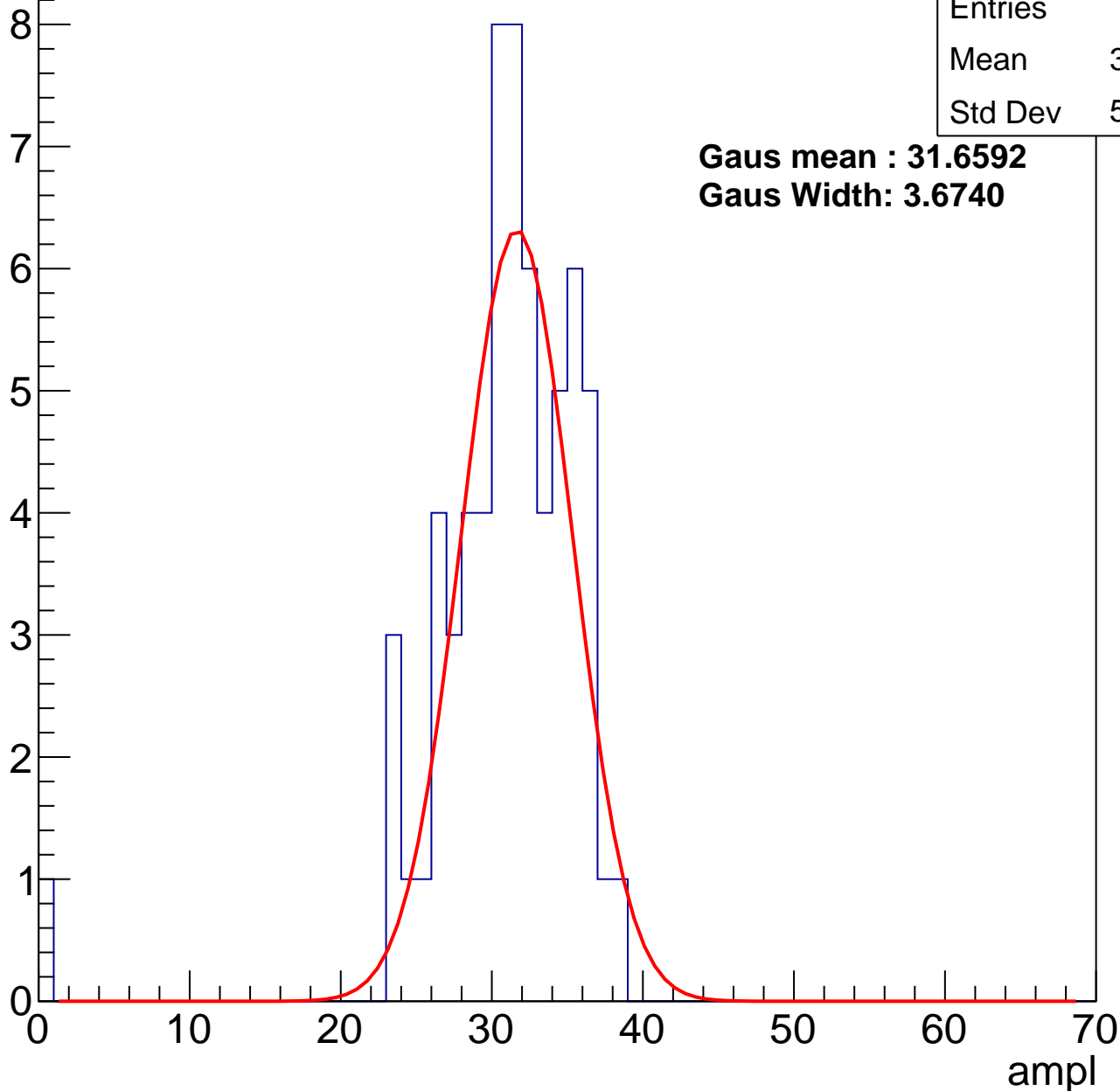
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	30.43
Std Dev	5.259

**Gaus mean : 31.6592**

**Gaus Width: 3.6740**



# B1L102S, U16-ch84, adc1

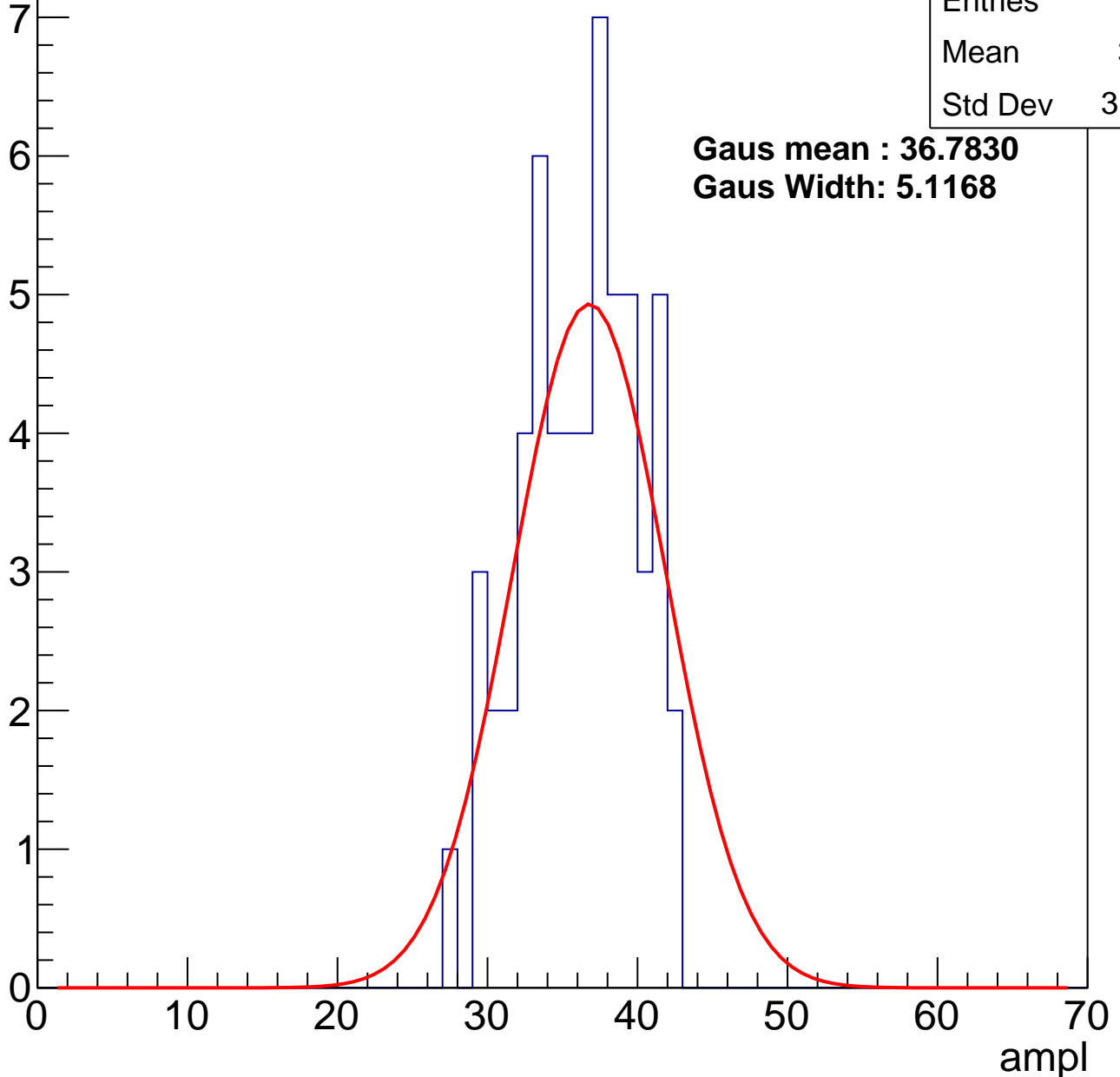
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	35.7
Std Dev	3.746

**Gaus mean : 36.7830**

**Gaus Width: 5.1168**



# B1L102S, U16-ch84, adc2

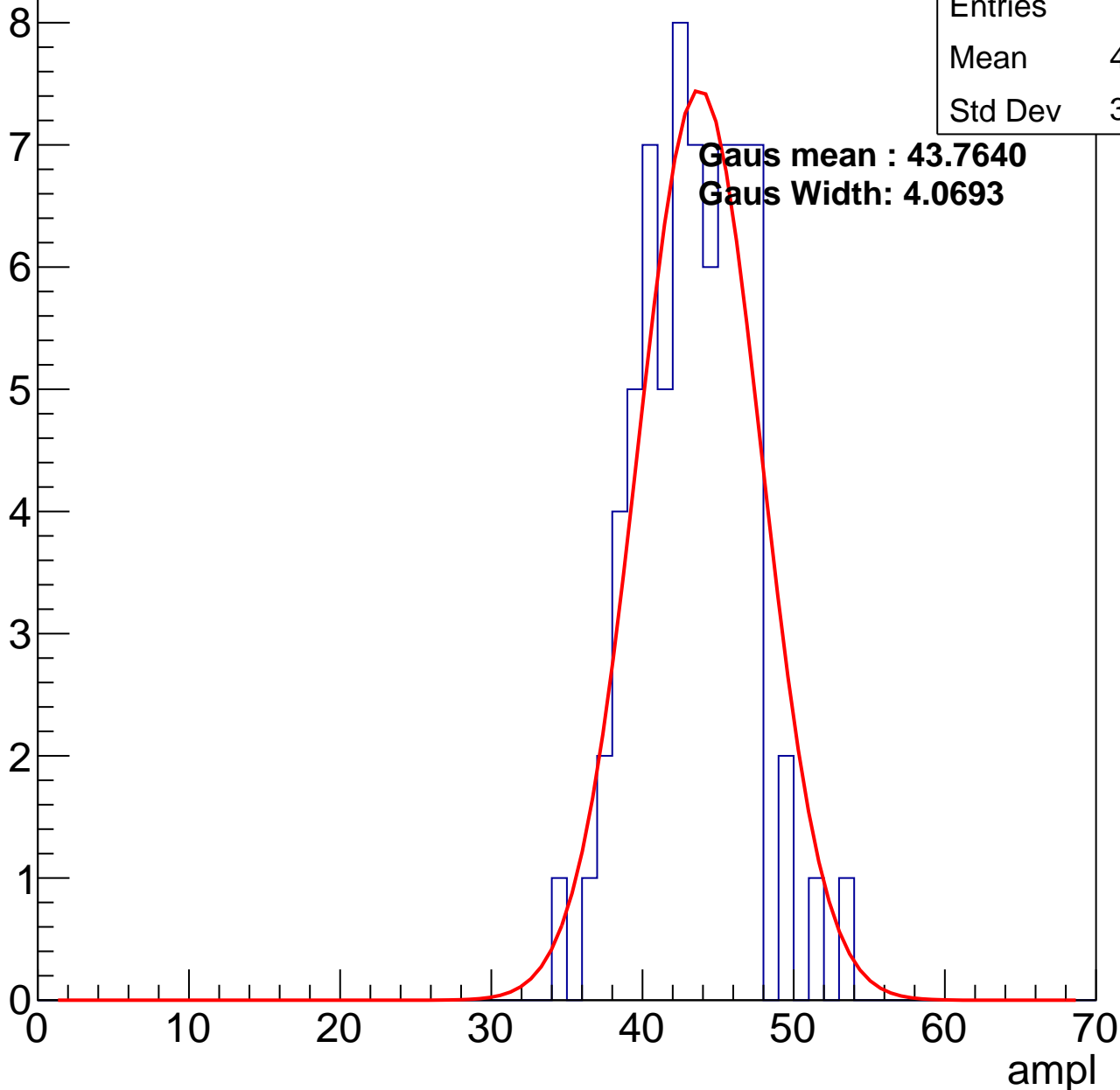
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	42.89
Std Dev	3.594

**Gaus mean : 43.7640**

**Gaus Width: 4.0693**

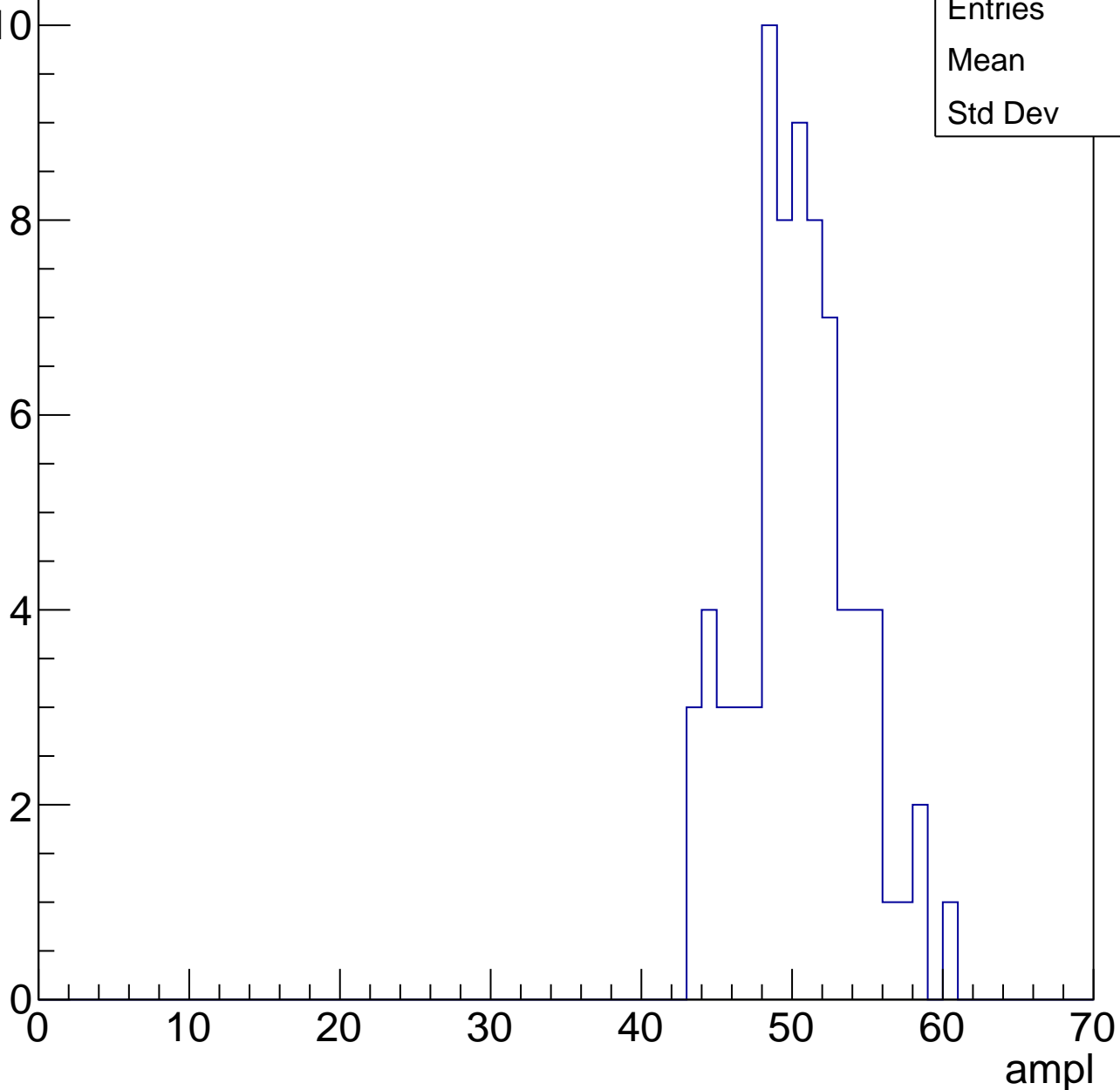


# B1L102S, U16-ch84, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

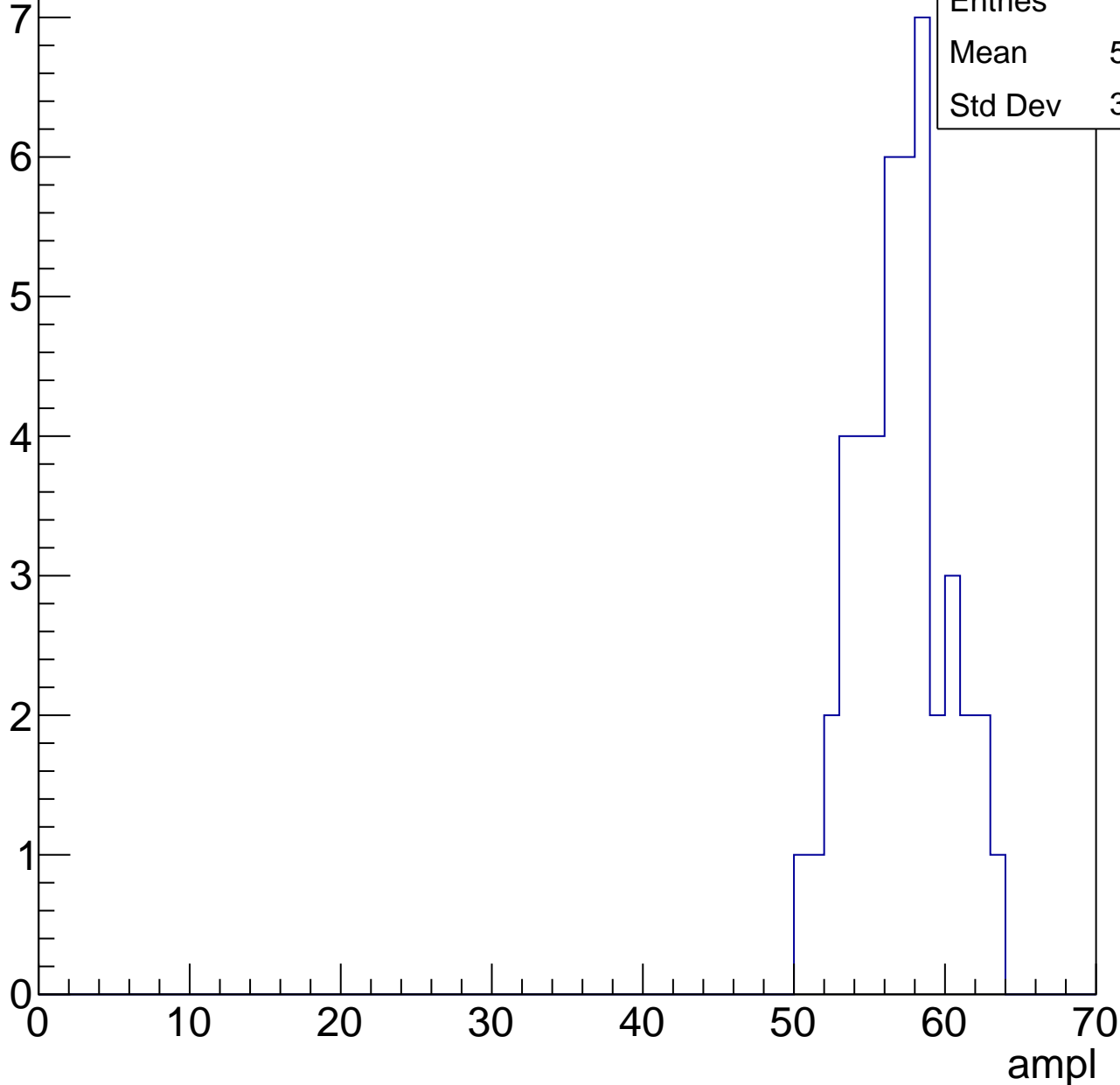
Entries	75
Mean	50
Std Dev	3.72



# B1L102S, U16-ch84, adc4

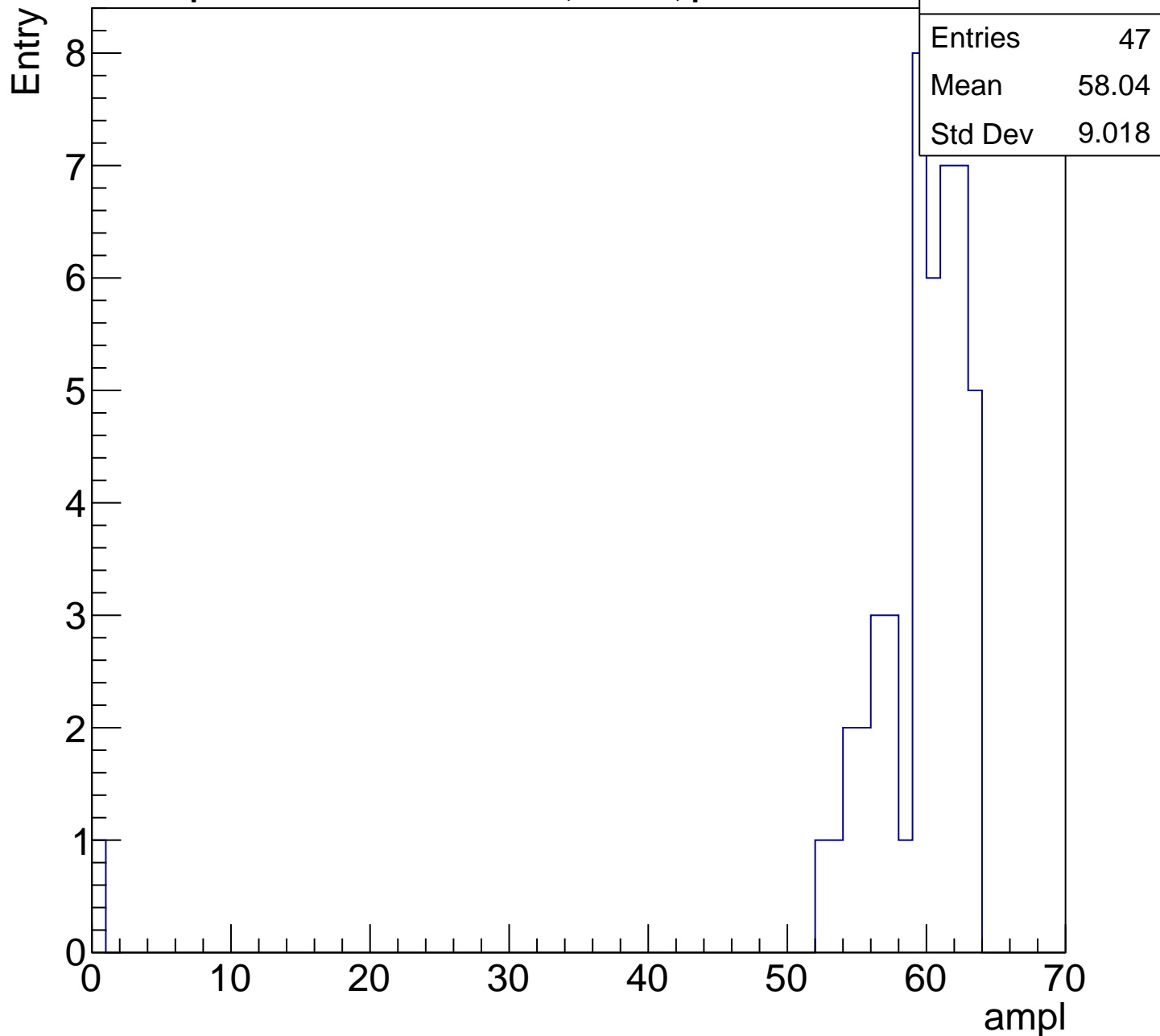
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch84, adc5

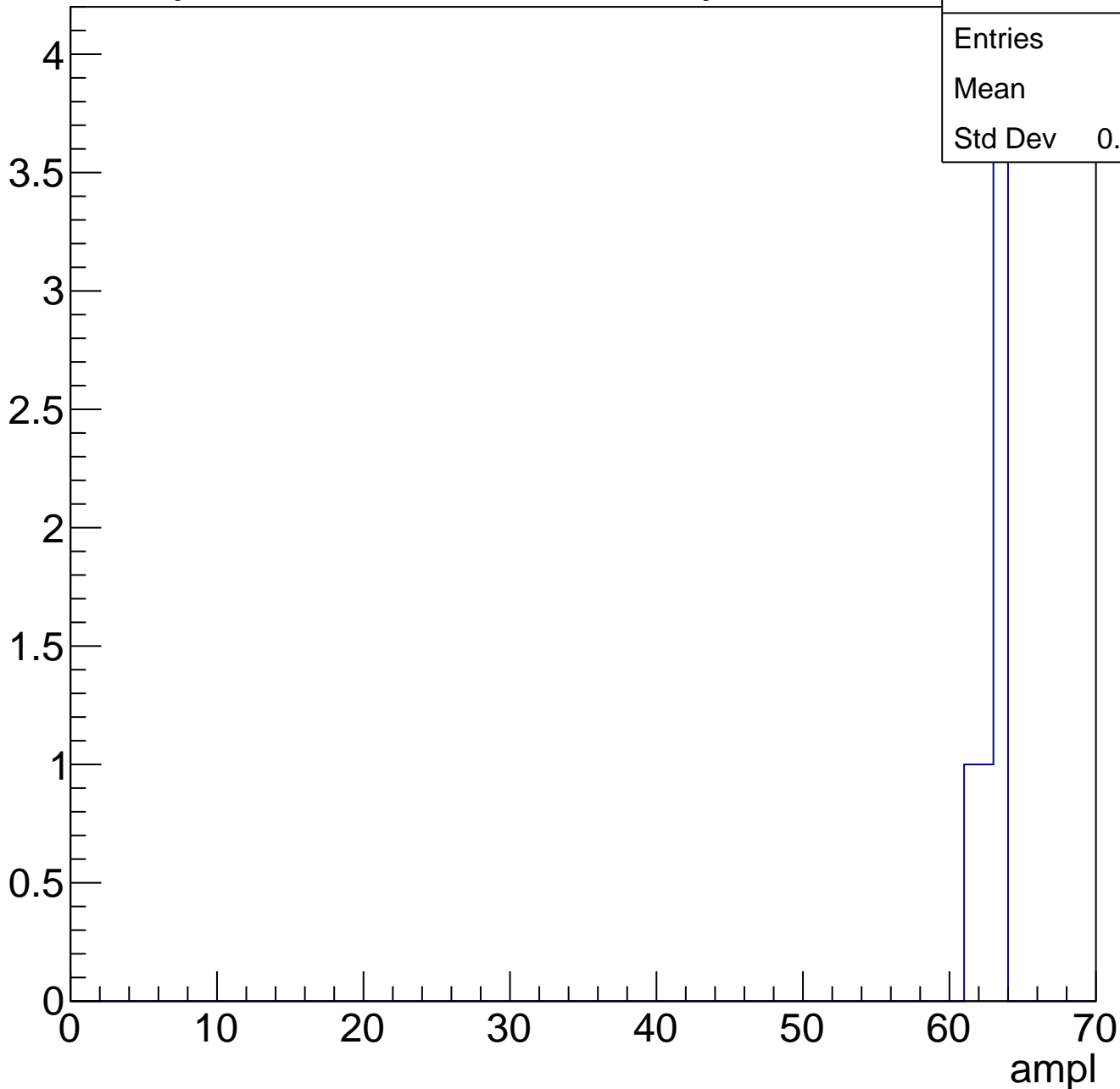
calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U16-ch84, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch84, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U16-ch85, adc0

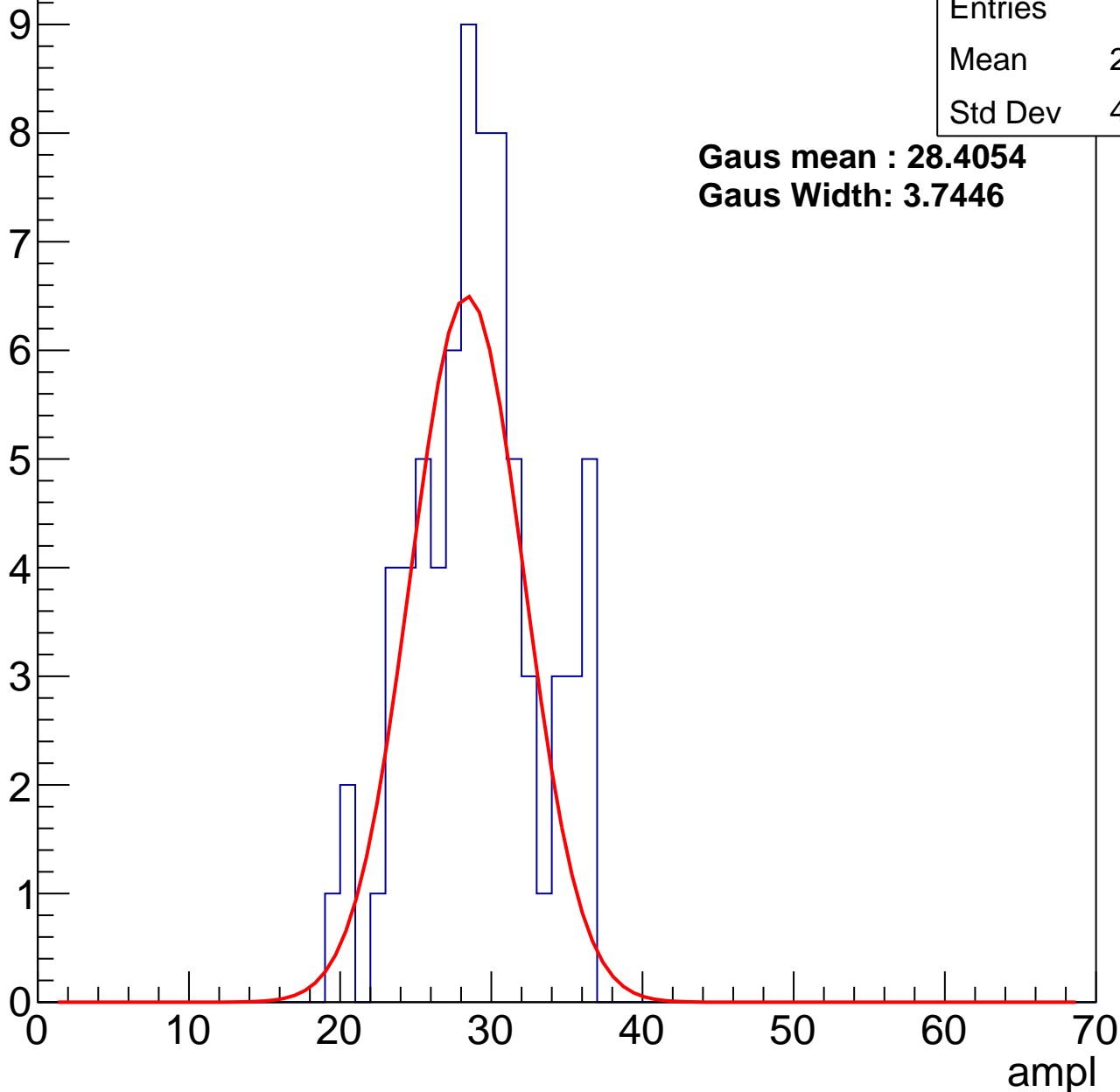
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	28.54
Std Dev	4.062

**Gaus mean : 28.4054**

**Gaus Width: 3.7446**



# B1L102S, U16-ch85, adc1

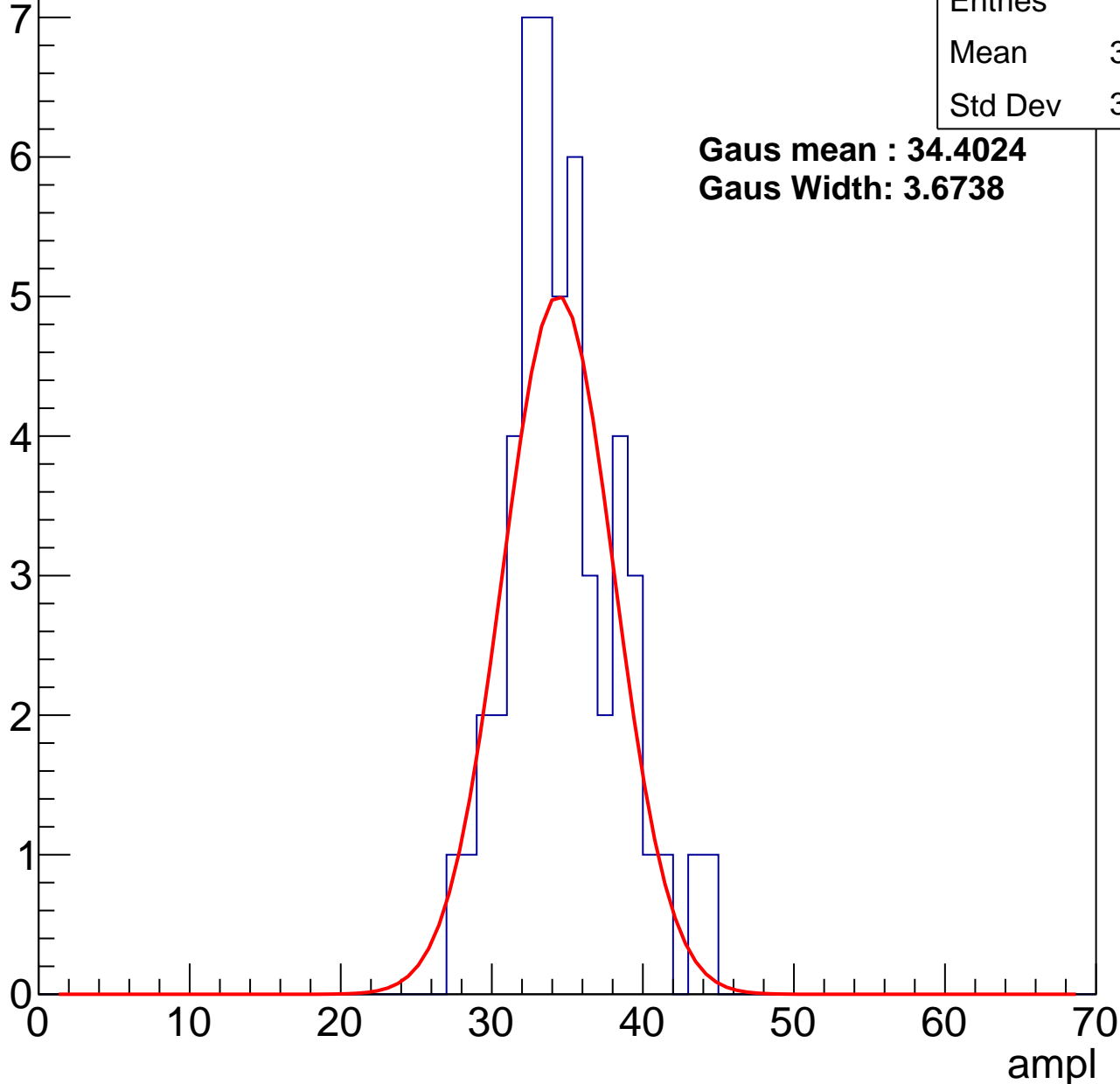
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	34.33
Std Dev	3.634

**Gaus mean : 34.4024**

**Gaus Width: 3.6738**



# B1L102S, U16-ch85, adc2

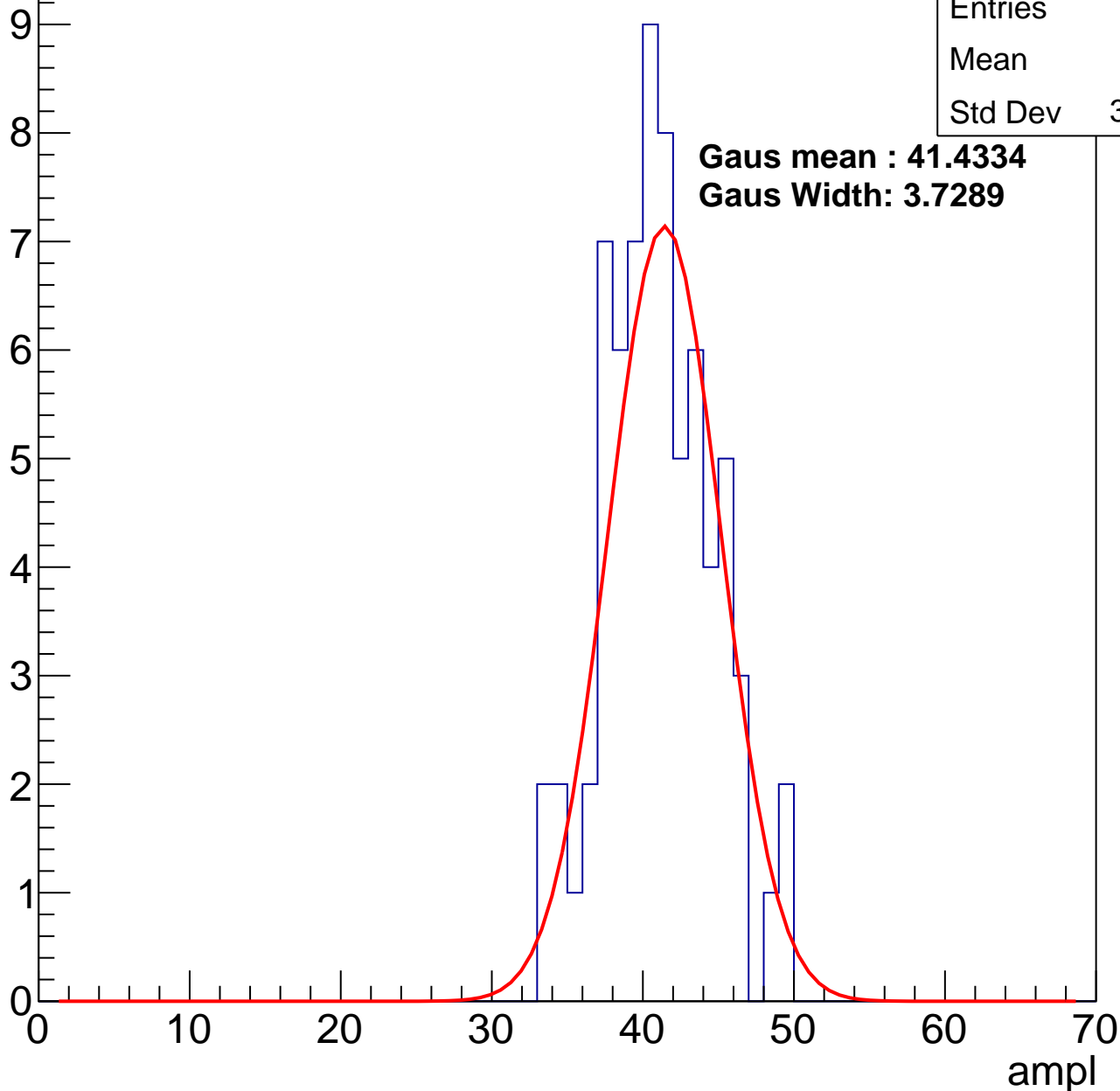
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	40.6
Std Dev	3.587

**Gaus mean : 41.4334**

**Gaus Width: 3.7289**

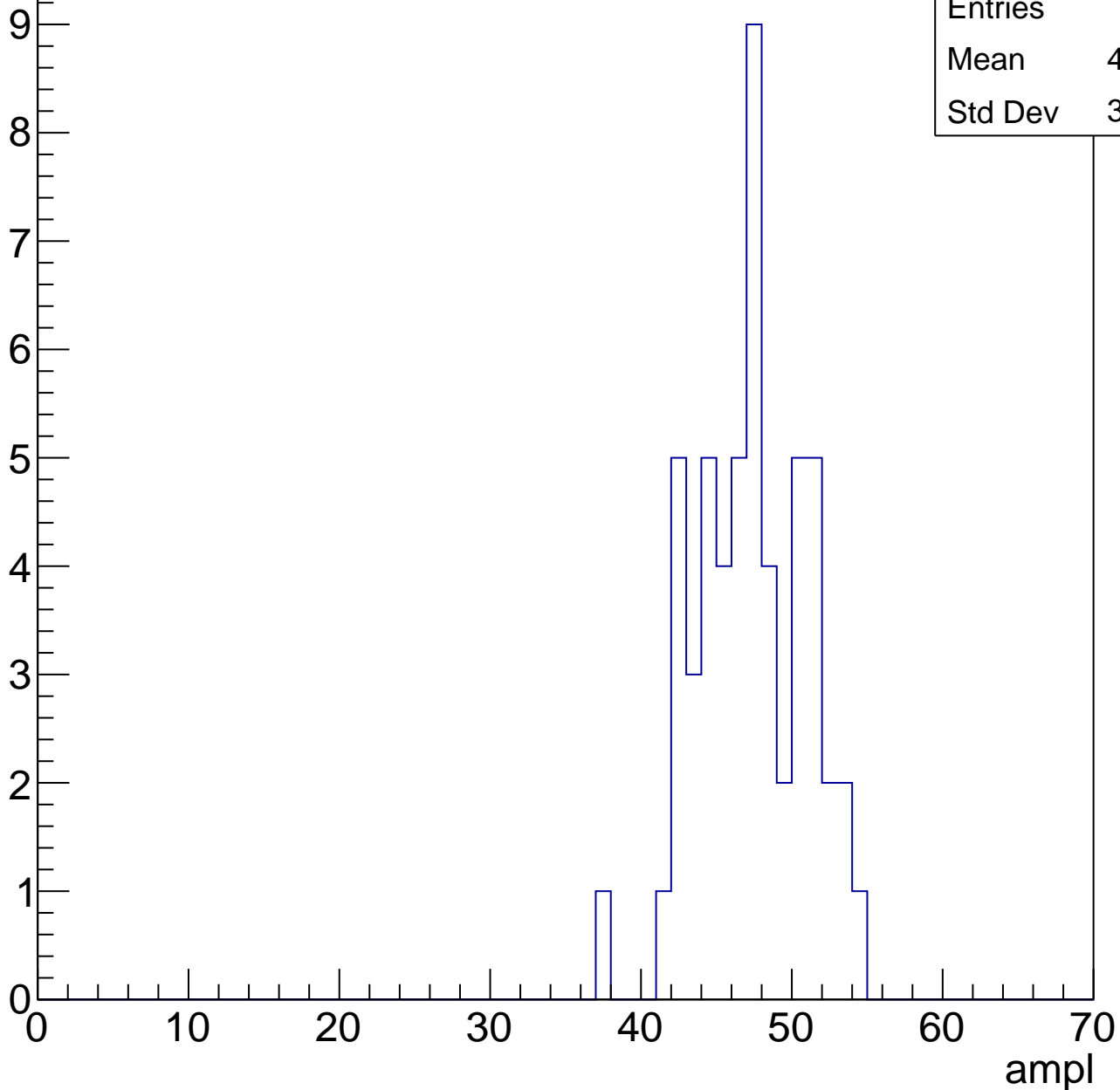


# B1L102S, U16-ch85, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	46.83
Std Dev	3.553

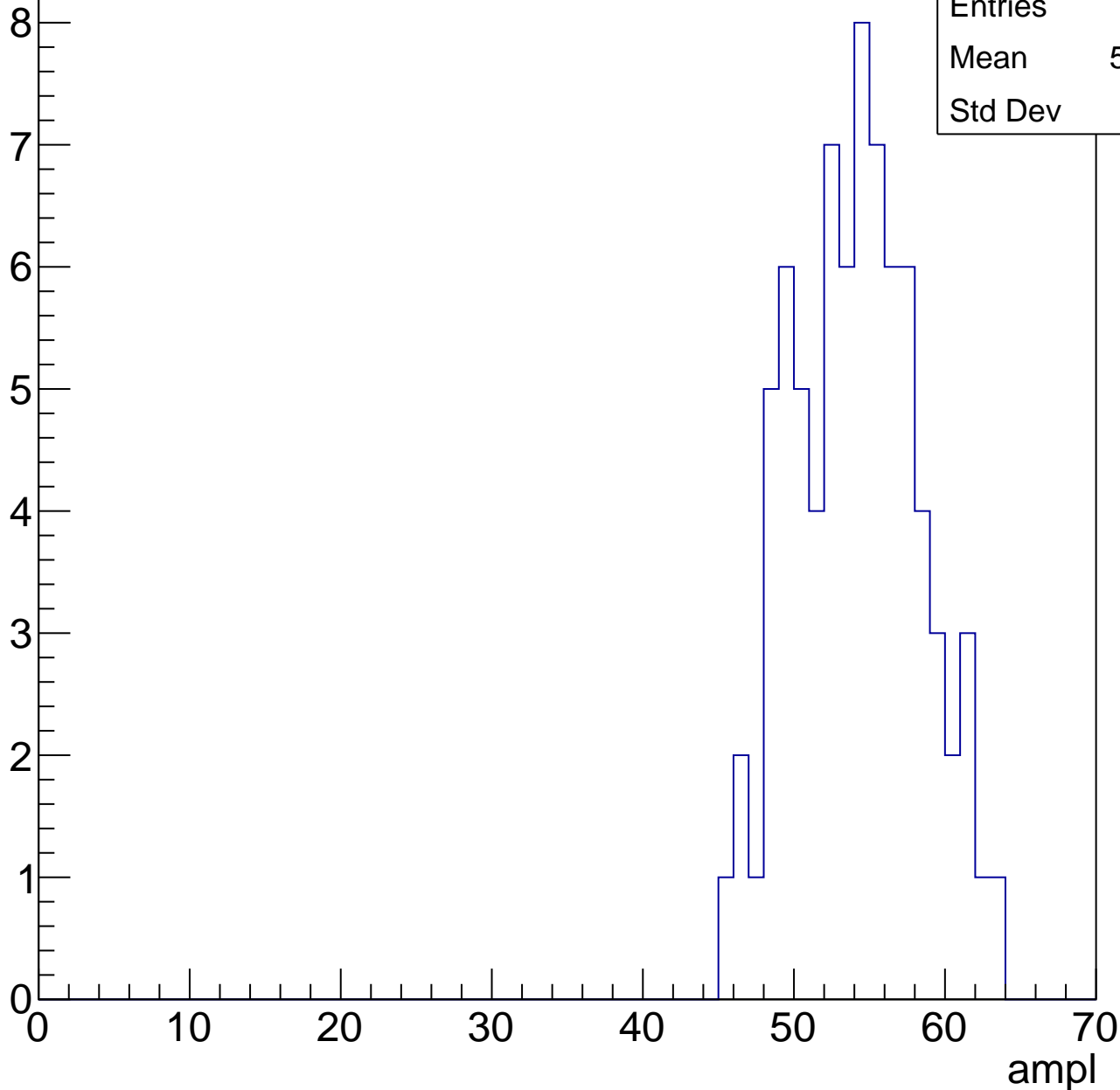


# B1L102S, U16-ch85, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	53.67
Std Dev	4.11

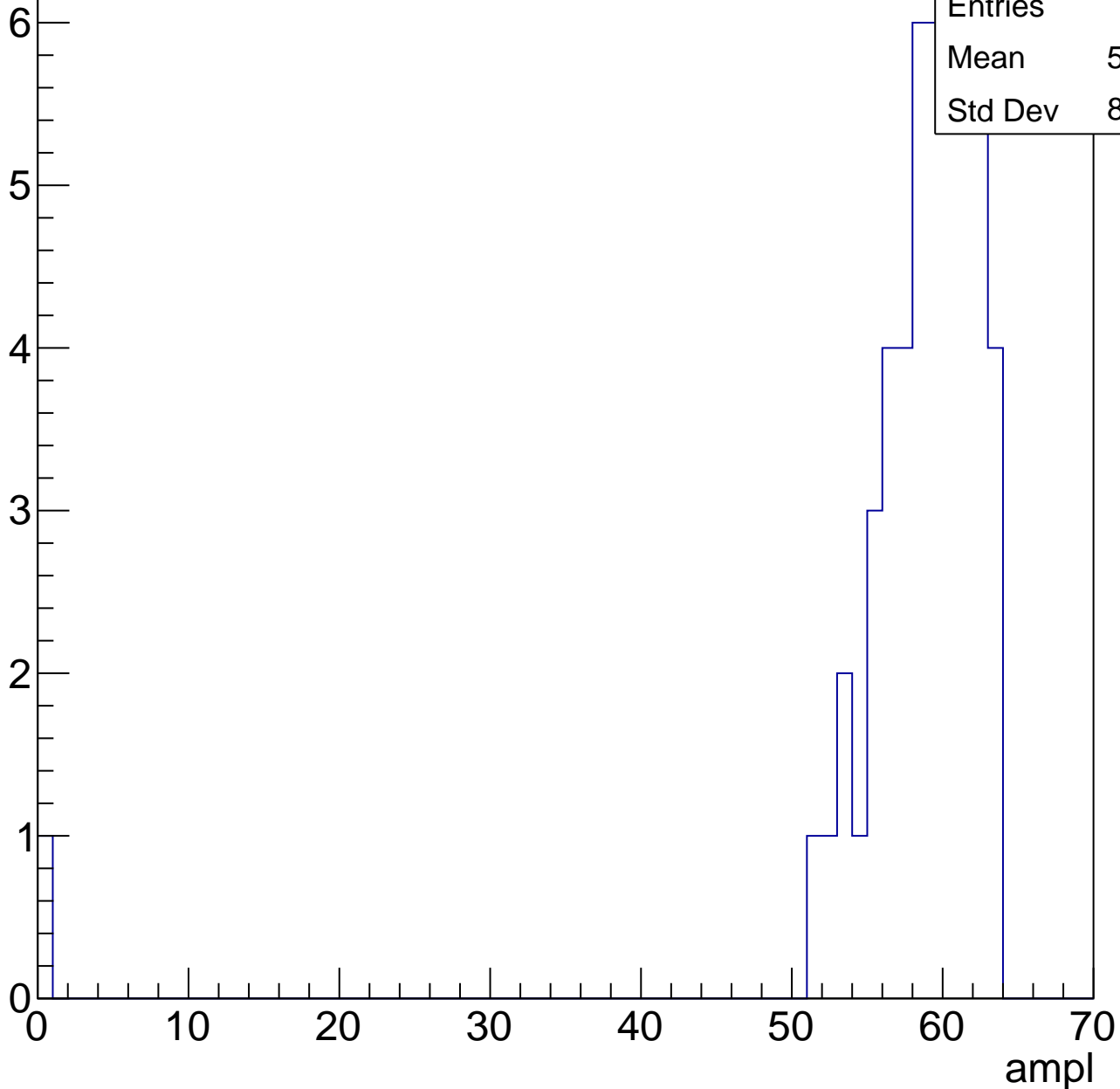


# B1L102S, U16-ch85, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	57.49
Std Dev	8.664

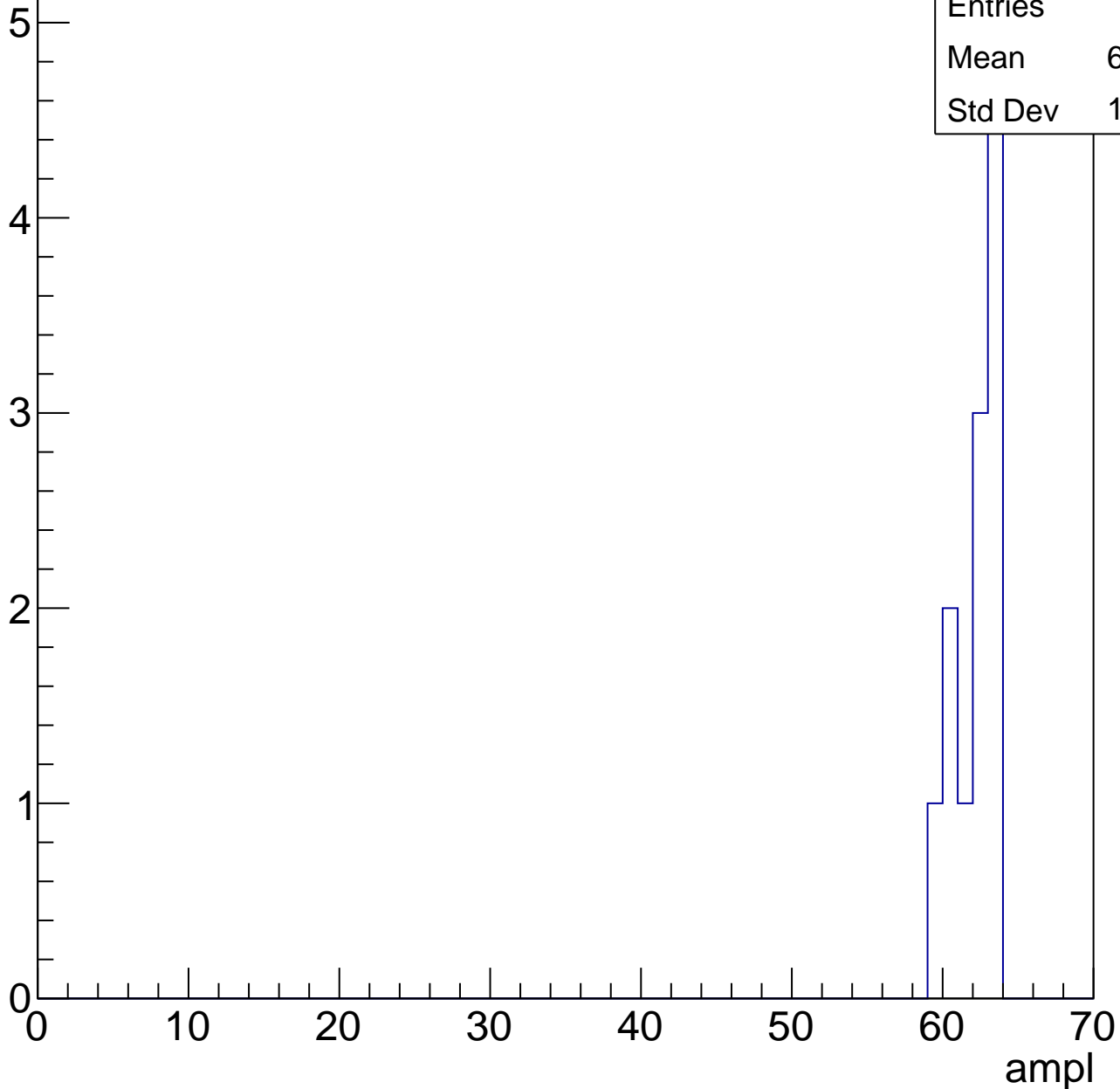


# B1L102S, U16-ch85, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	12
Mean	61.75
Std Dev	1.362





# B1L102S, U16-ch85, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U16-ch86, adc0

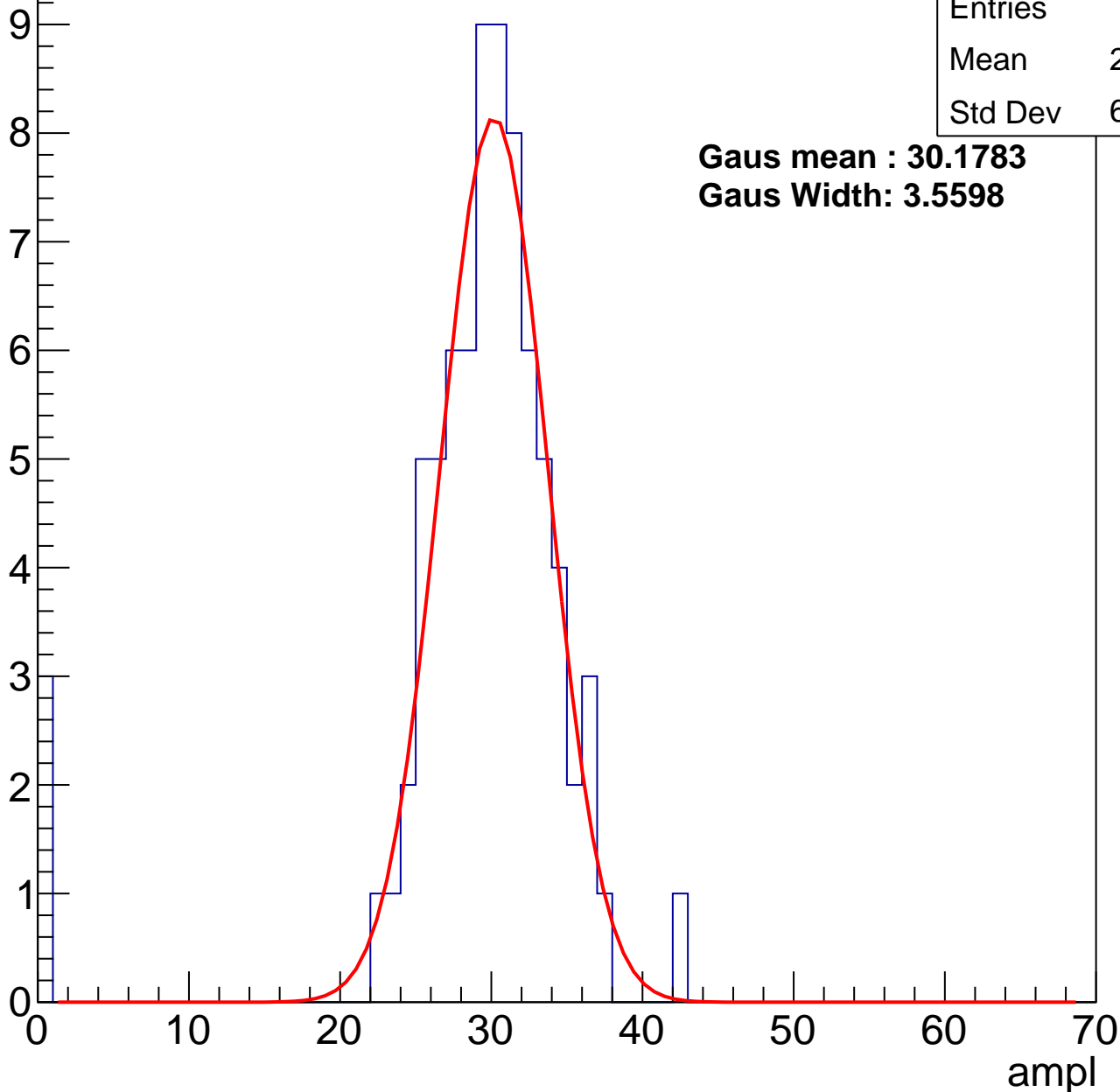
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	28.66
Std Dev	6.772

**Gaus mean : 30.1783**

**Gaus Width: 3.5598**



# B1L102S, U16-ch86, adc1

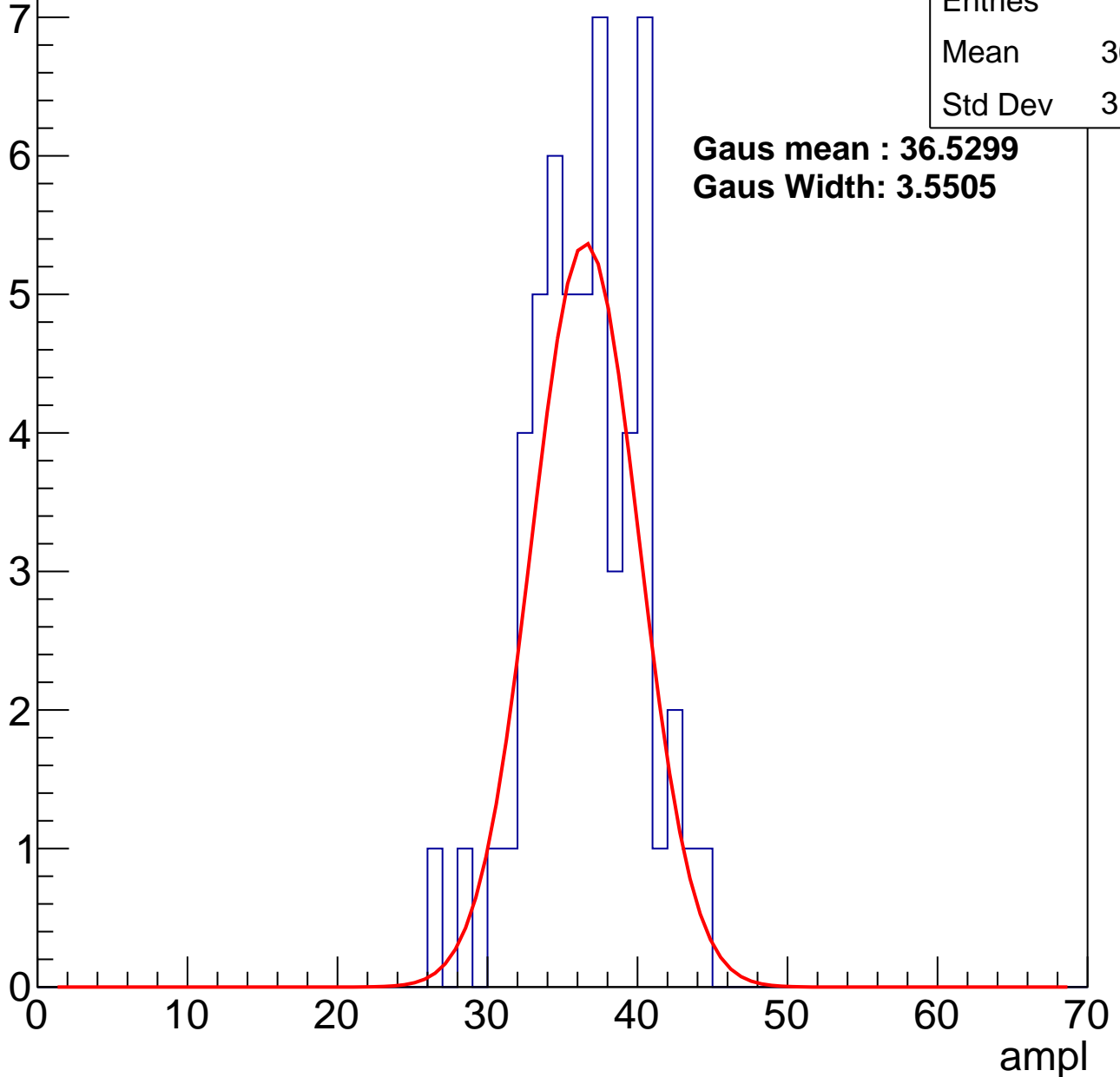
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	36.15
Std Dev	3.665

**Gaus mean : 36.5299**

**Gaus Width: 3.5505**



# B1L102S, U16-ch86, adc2

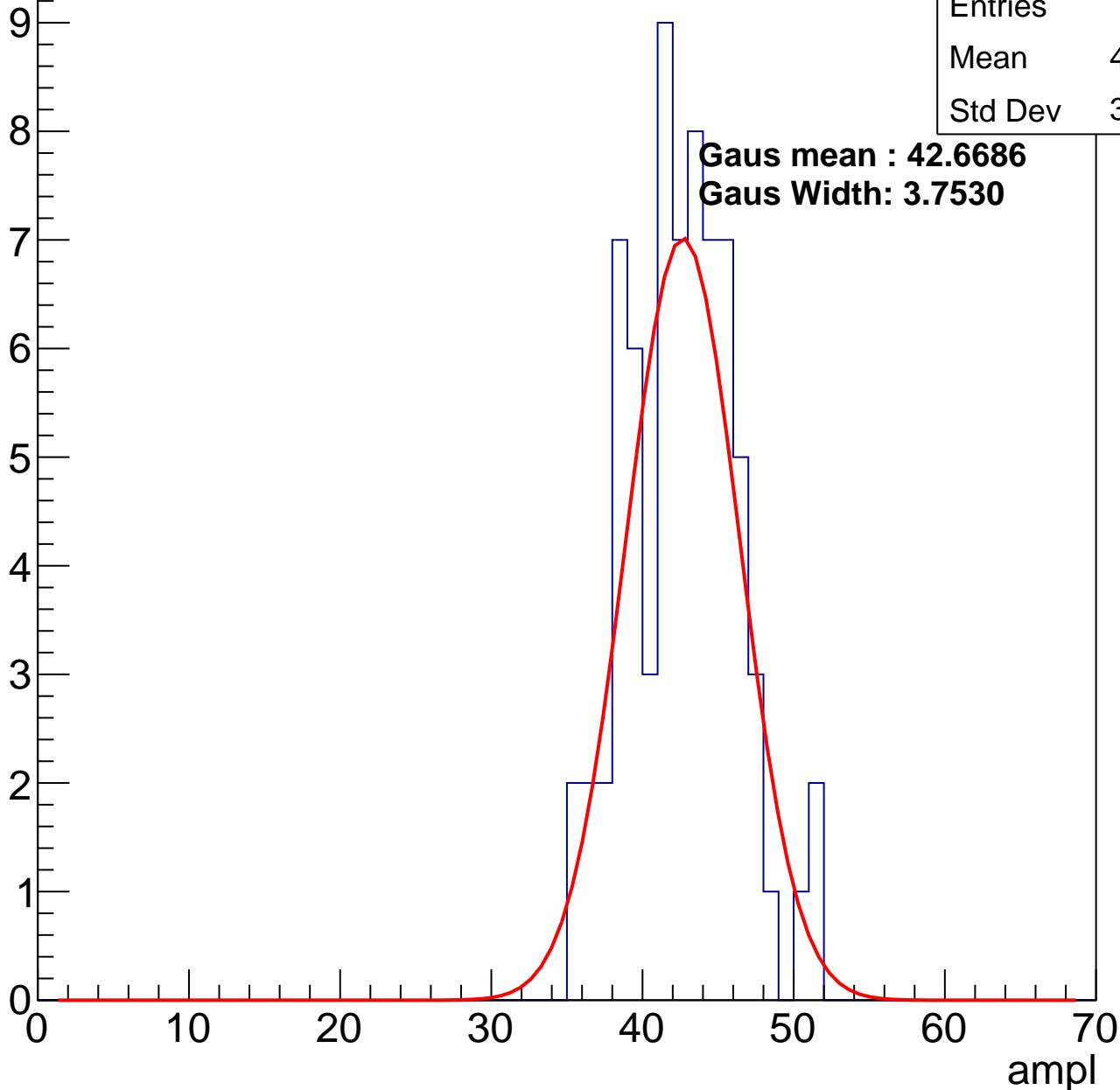
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	42.18
Std Dev	3.576

**Gaus mean : 42.6686**

**Gaus Width: 3.7530**

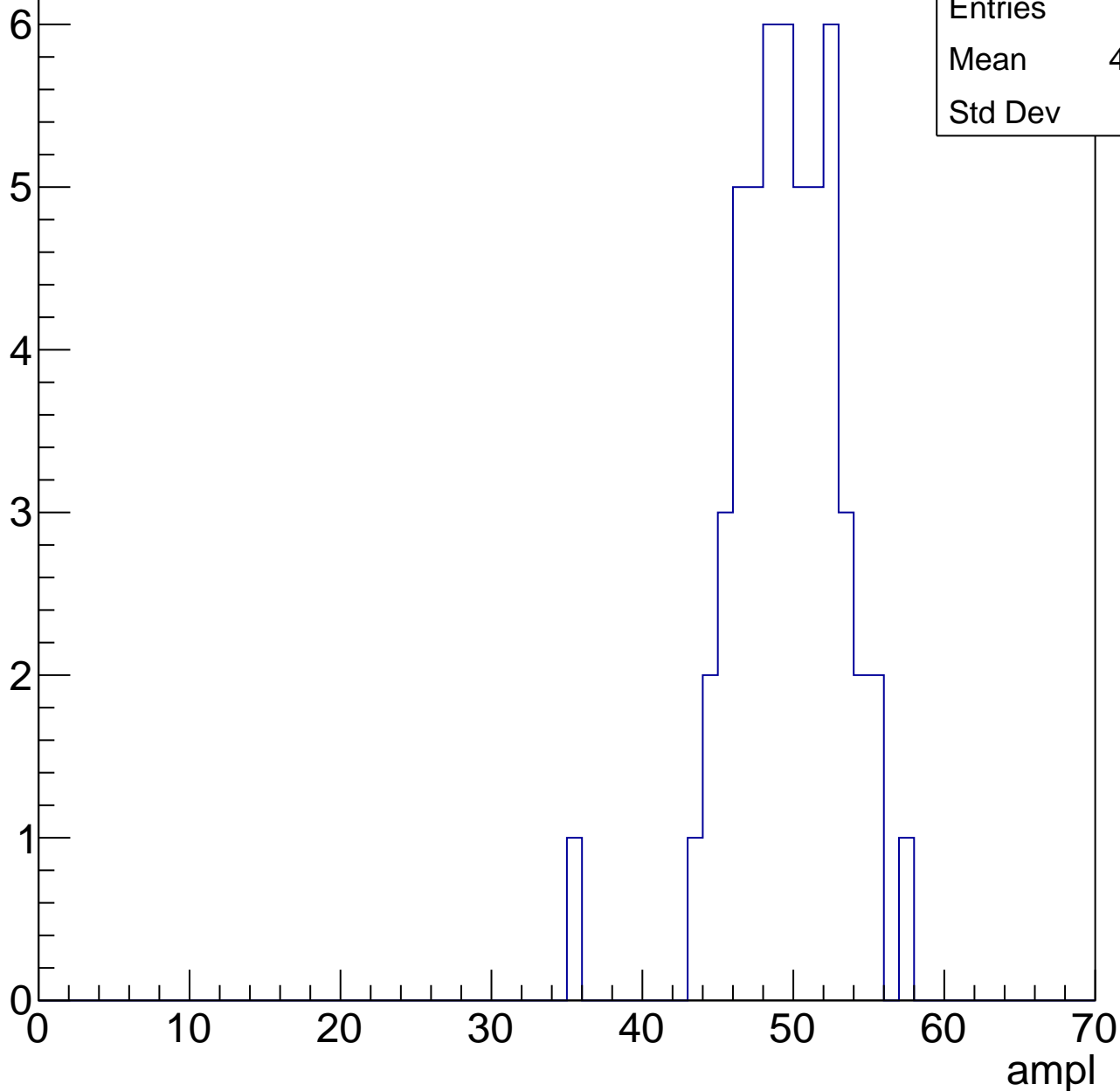


# B1L102S, U16-ch86, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	49.04
Std Dev	3.67

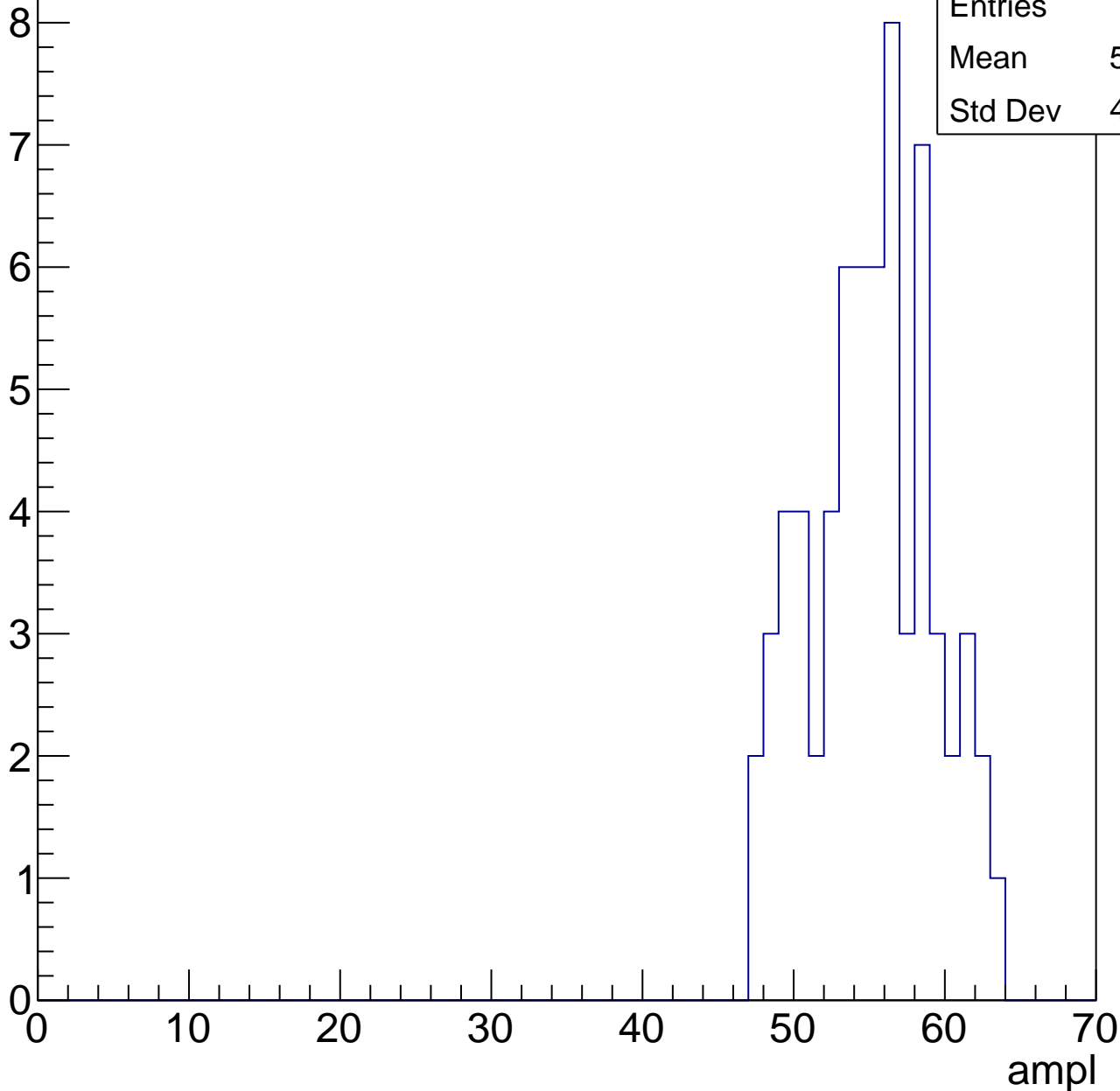


# B1L102S, U16-ch86, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	54.67
Std Dev	4.009



# B1L102S, U16-ch86, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

6

5

4

3

2

1

0

0

10

20

30

40

50

60

70

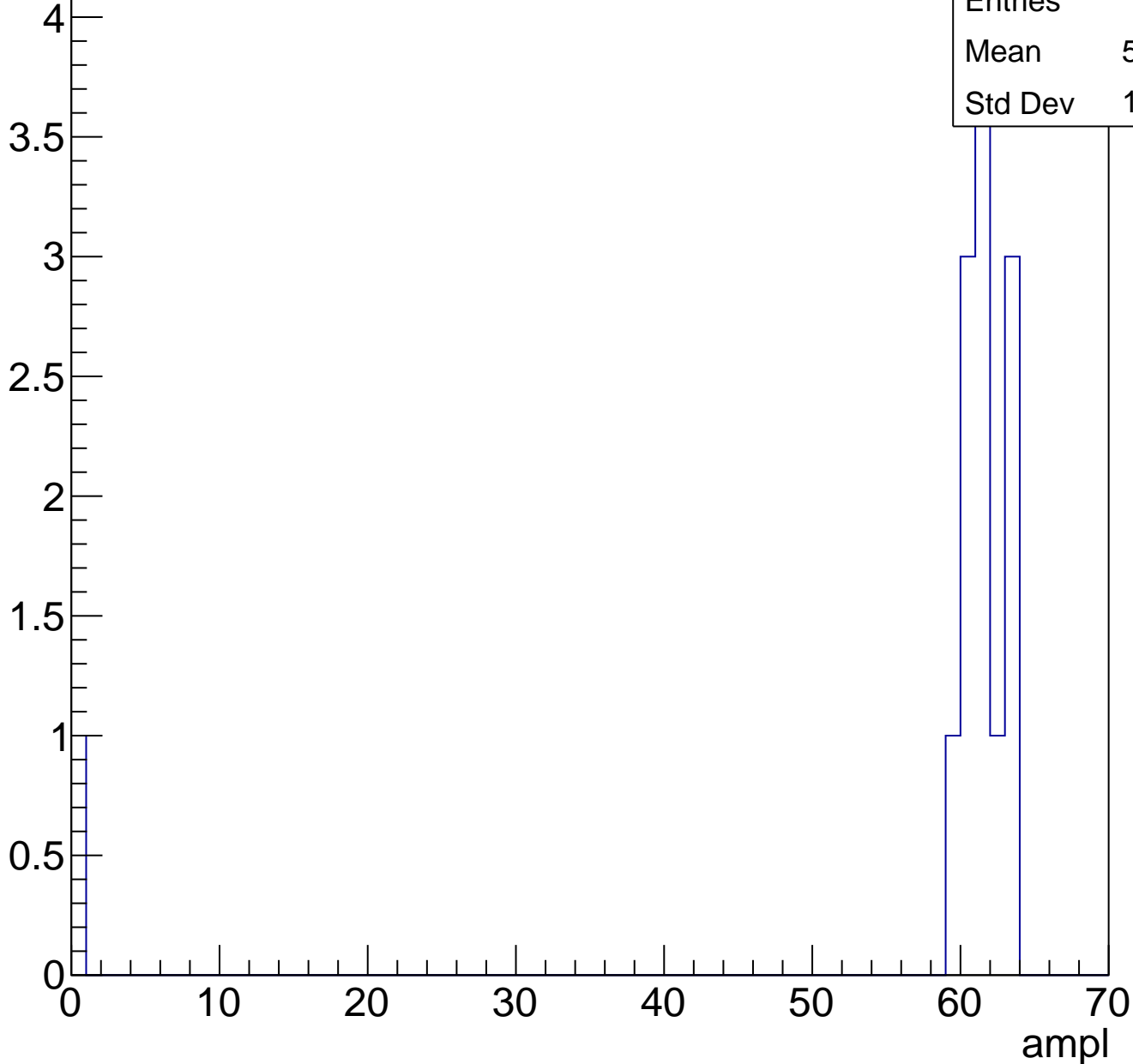
ampl

Entries	43
Mean	59
Std Dev	3.027

# B1L102S, U16-ch86, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch86, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch87, adc0

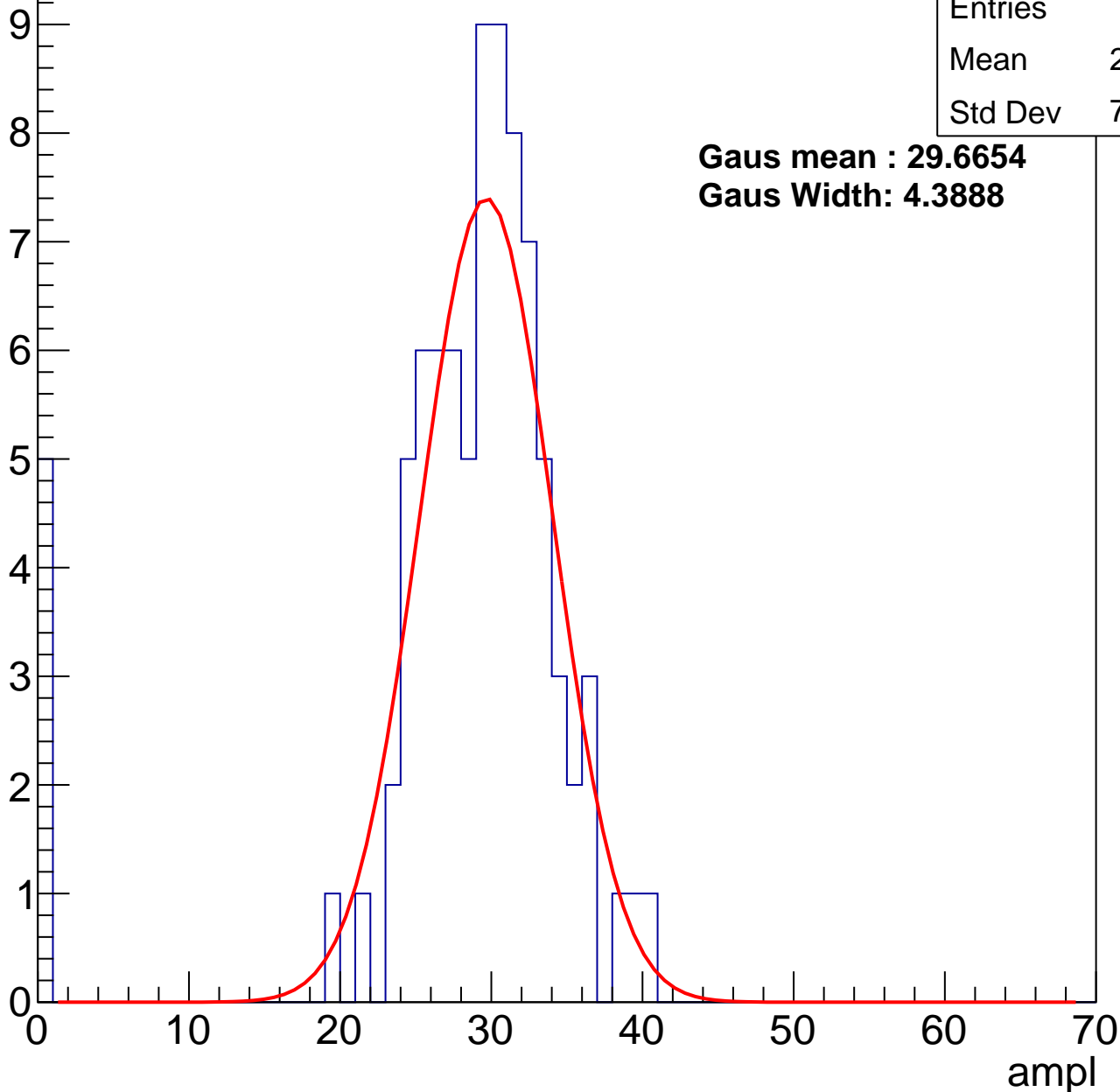
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	86
Mean	27.66
Std Dev	7.903

**Gaus mean : 29.6654**

**Gaus Width: 4.3888**



# B1L102S, U16-ch87, adc1

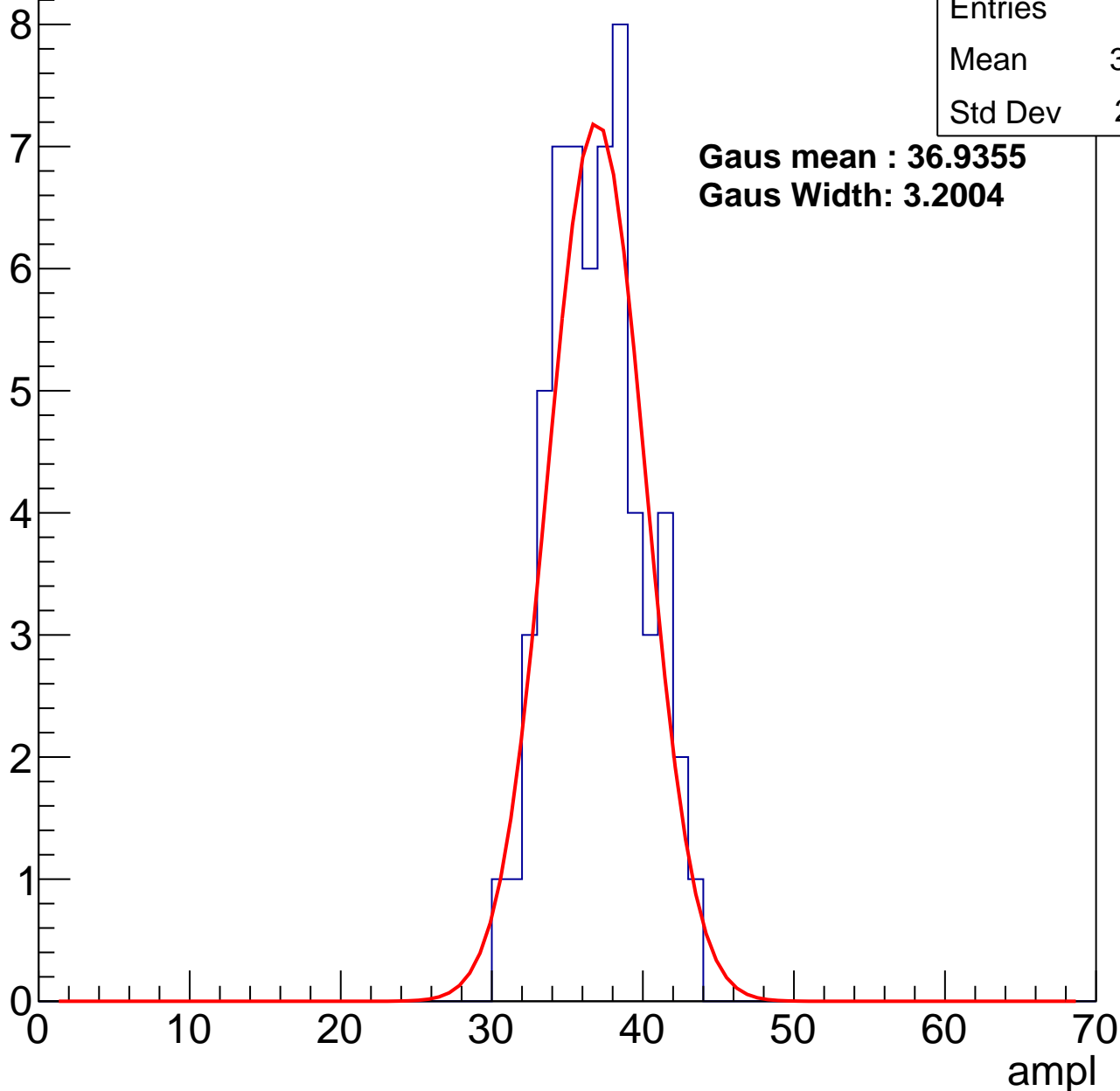
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	36.46
Std Dev	2.971

**Gaus mean : 36.9355**

**Gaus Width: 3.2004**



# B1L102S, U16-ch87, adc2

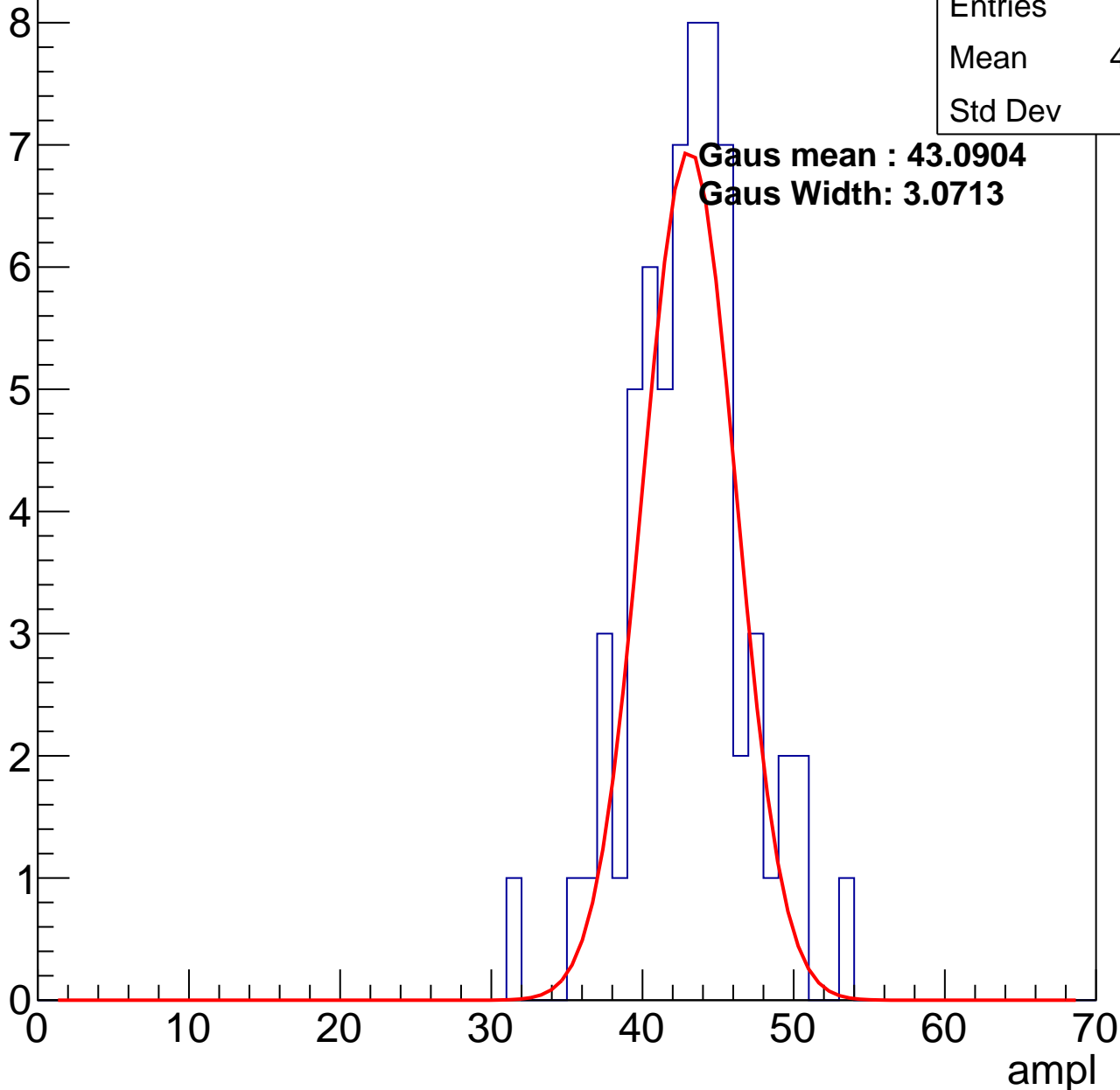
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	42.62
Std Dev	3.83

**Gaus mean : 43.0904**

**Gaus Width: 3.0713**

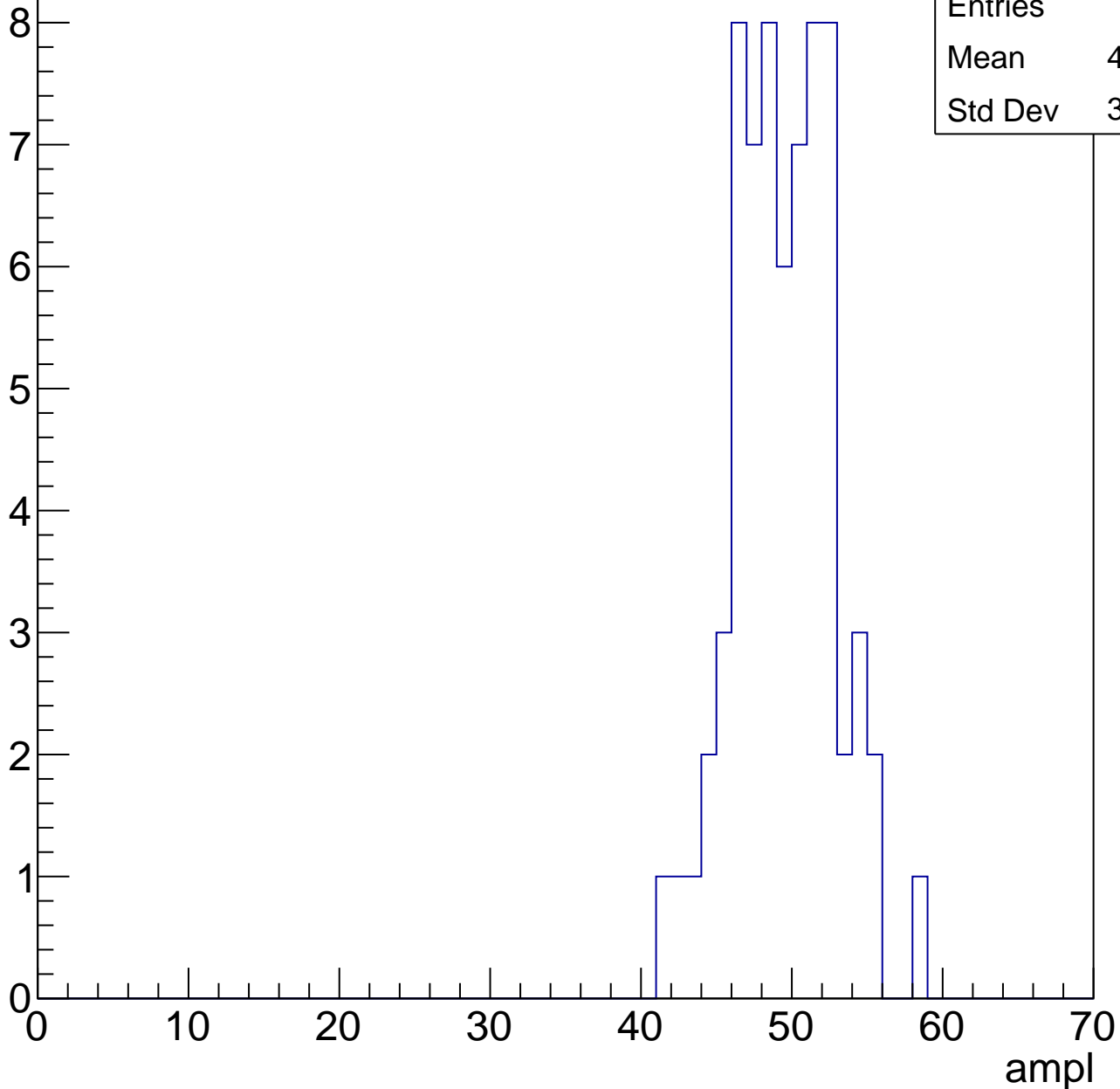


# B1L102S, U16-ch87, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	49.03
Std Dev	3.267

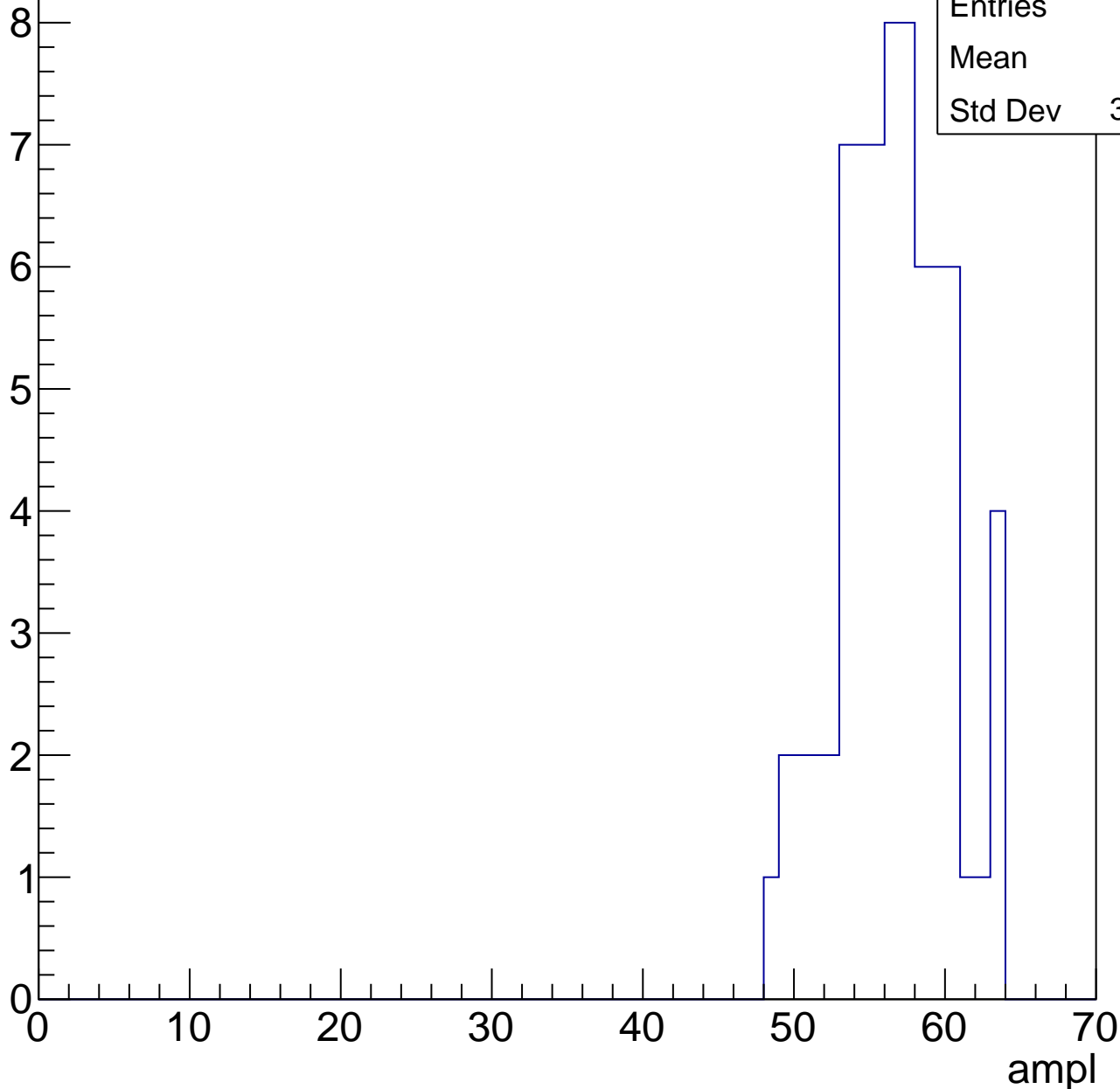


# B1L102S, U16-ch87, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	56.1
Std Dev	3.489

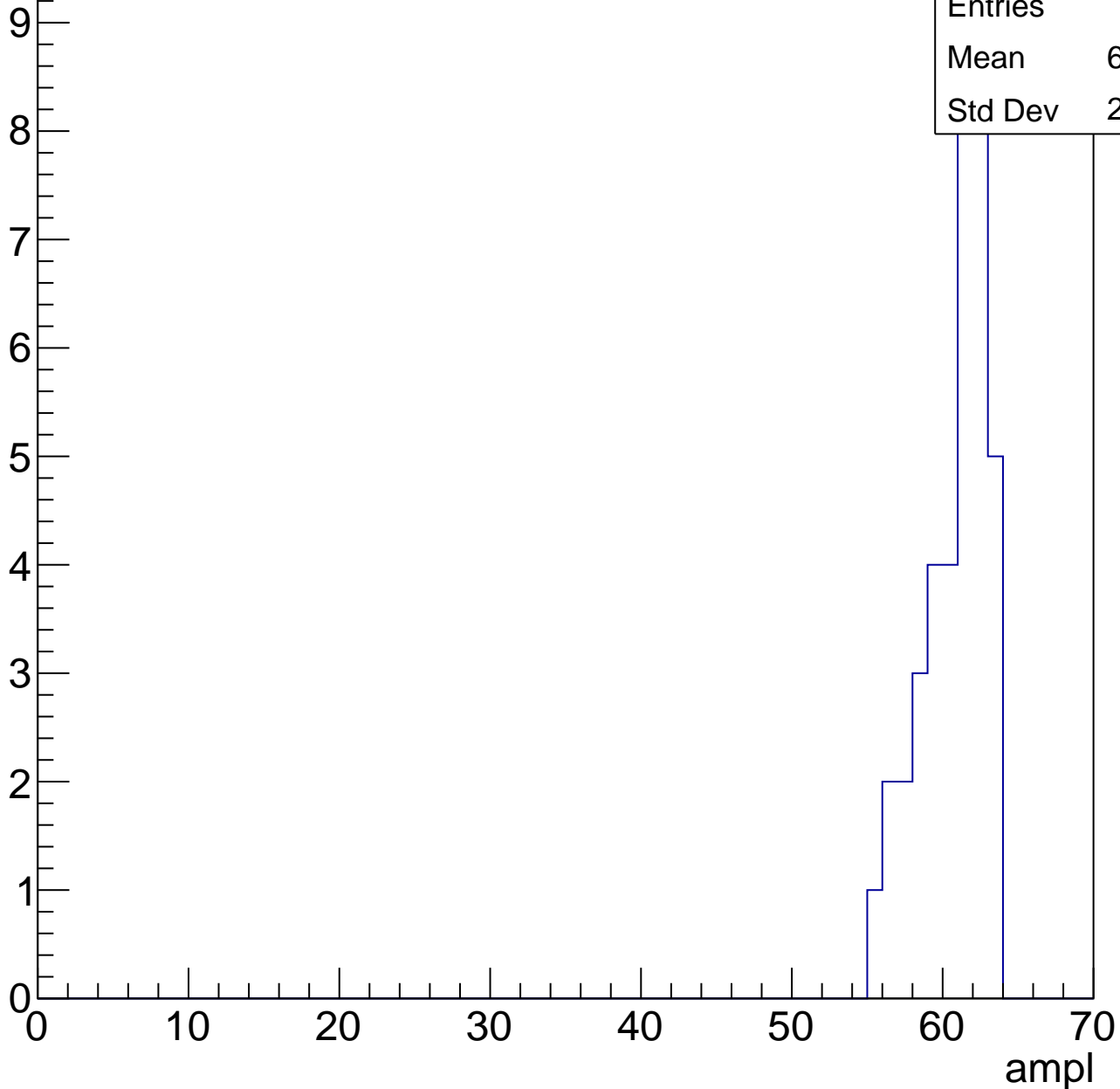


# B1L102S, U16-ch87, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	38
Mean	60.29
Std Dev	2.139



# B1L102S, U16-ch87, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch87, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	0
Std Dev	0

# B1L102S, U16-ch88, adc0

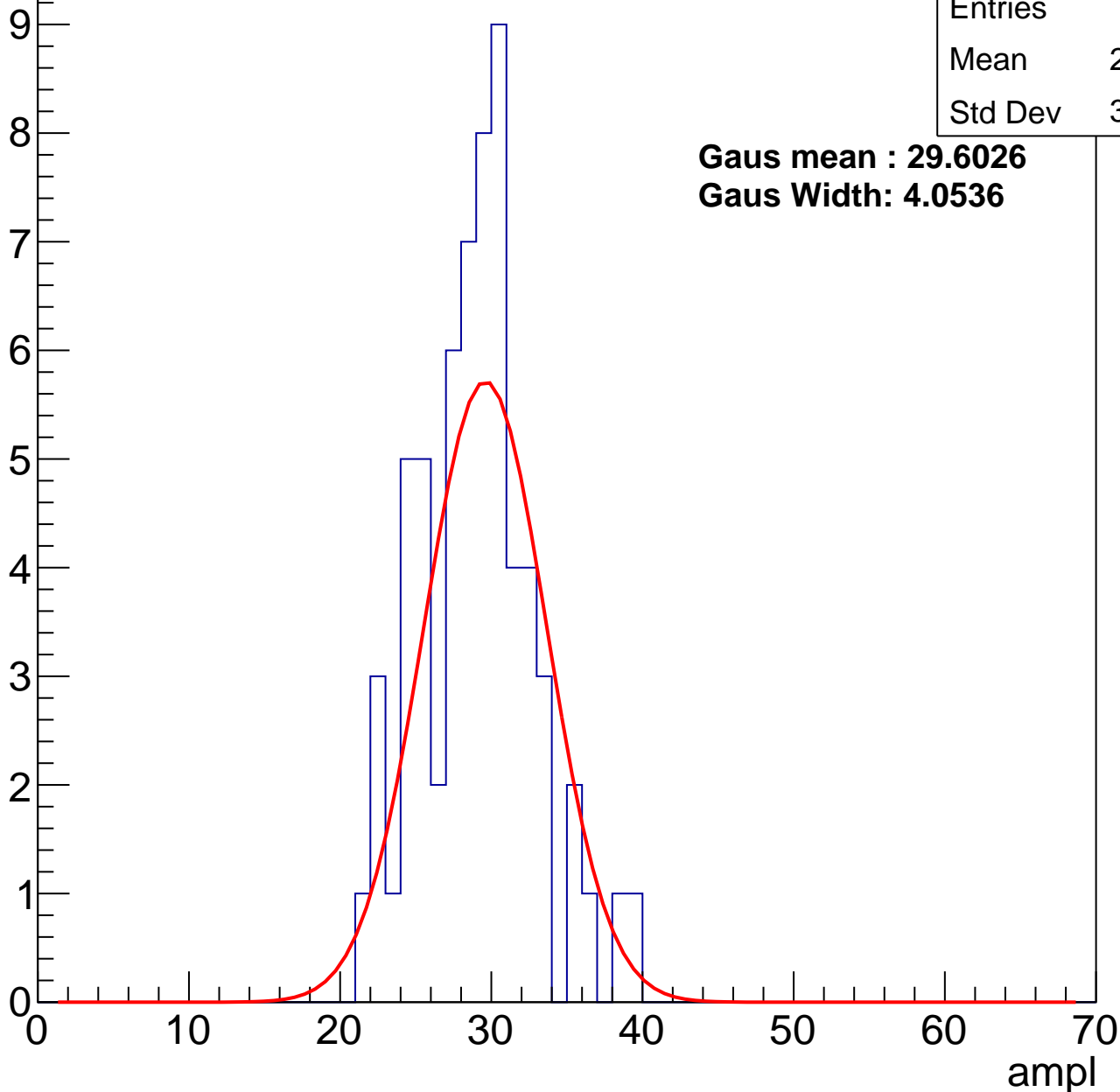
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	28.59
Std Dev	3.782

**Gaus mean : 29.6026**

**Gaus Width: 4.0536**



# B1L102S, U16-ch88, adc1

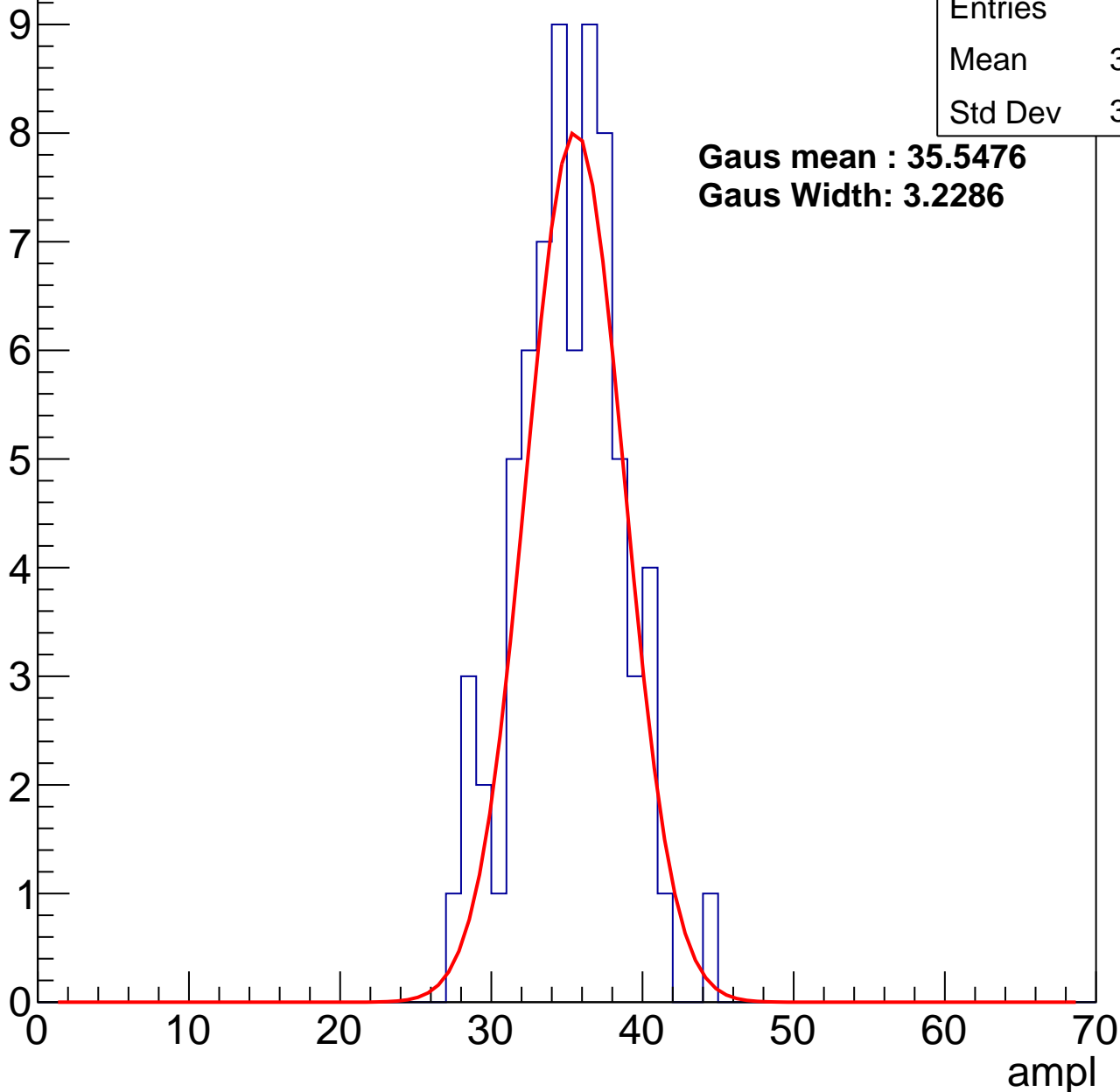
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	34.72
Std Dev	3.407

**Gaus mean : 35.5476**

**Gaus Width: 3.2286**



# B1L102S, U16-ch88, adc2

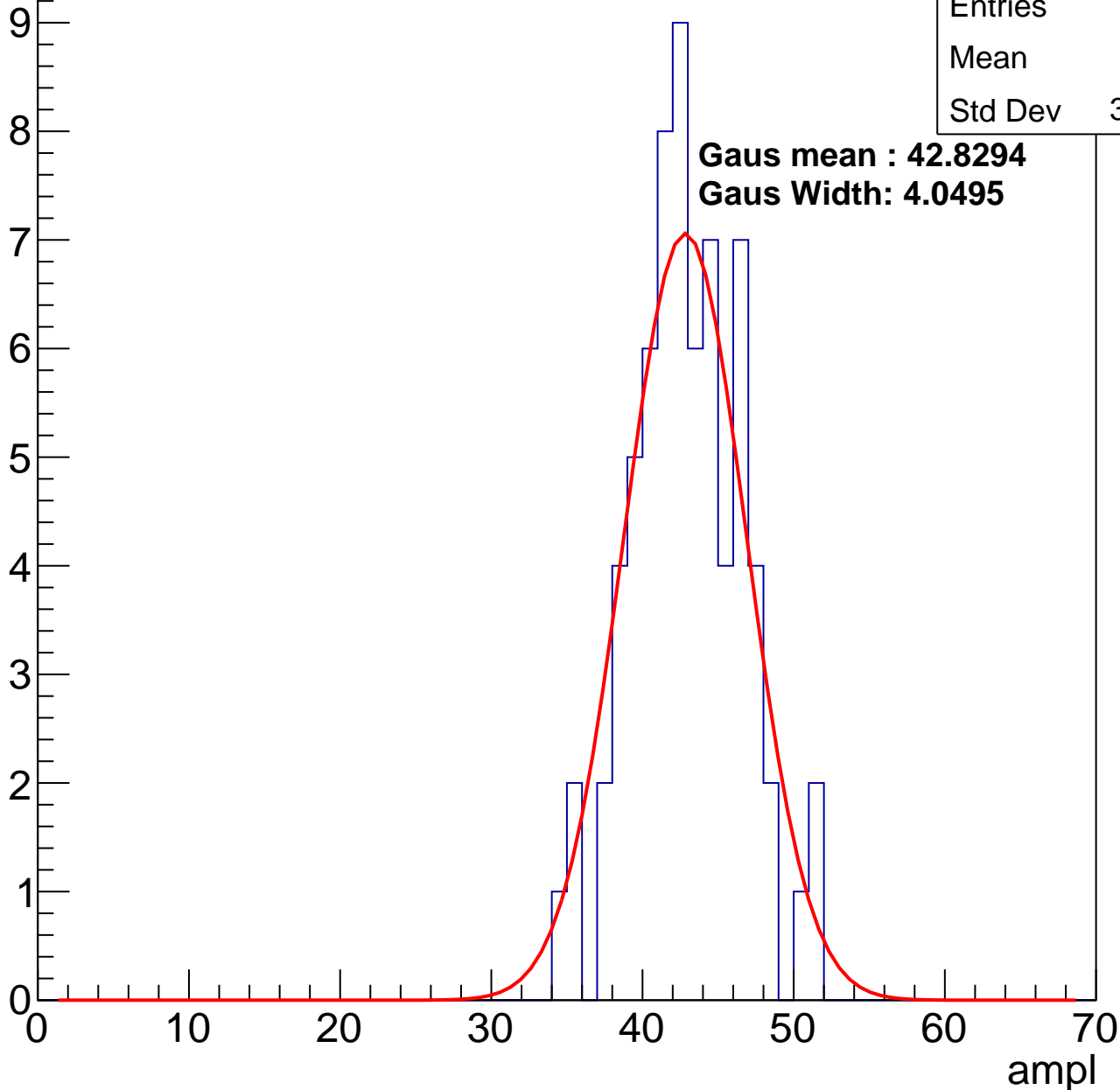
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	42.5
Std Dev	3.616

**Gaus mean : 42.8294**

**Gaus Width: 4.0495**

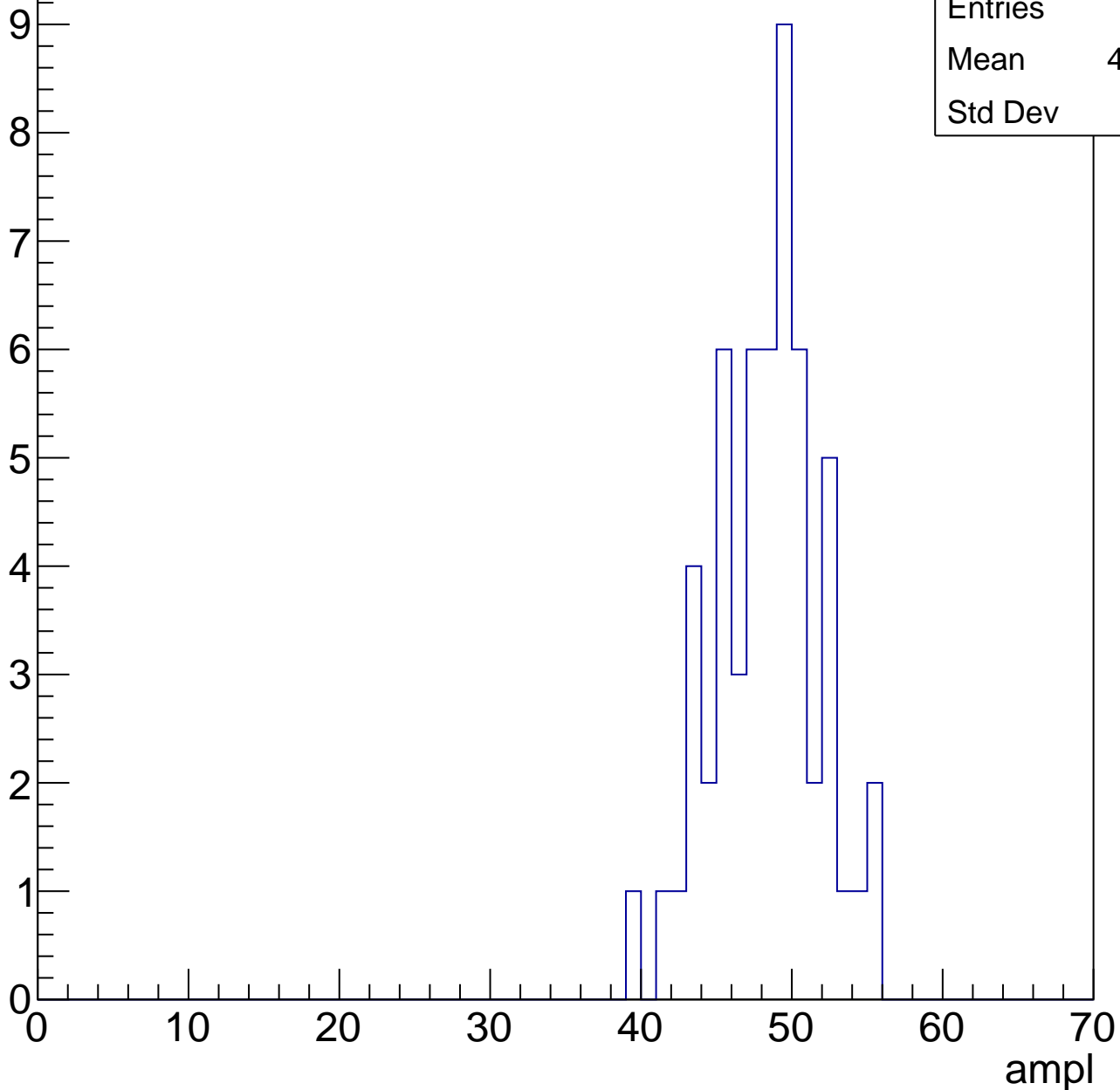


# B1L102S, U16-ch88, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

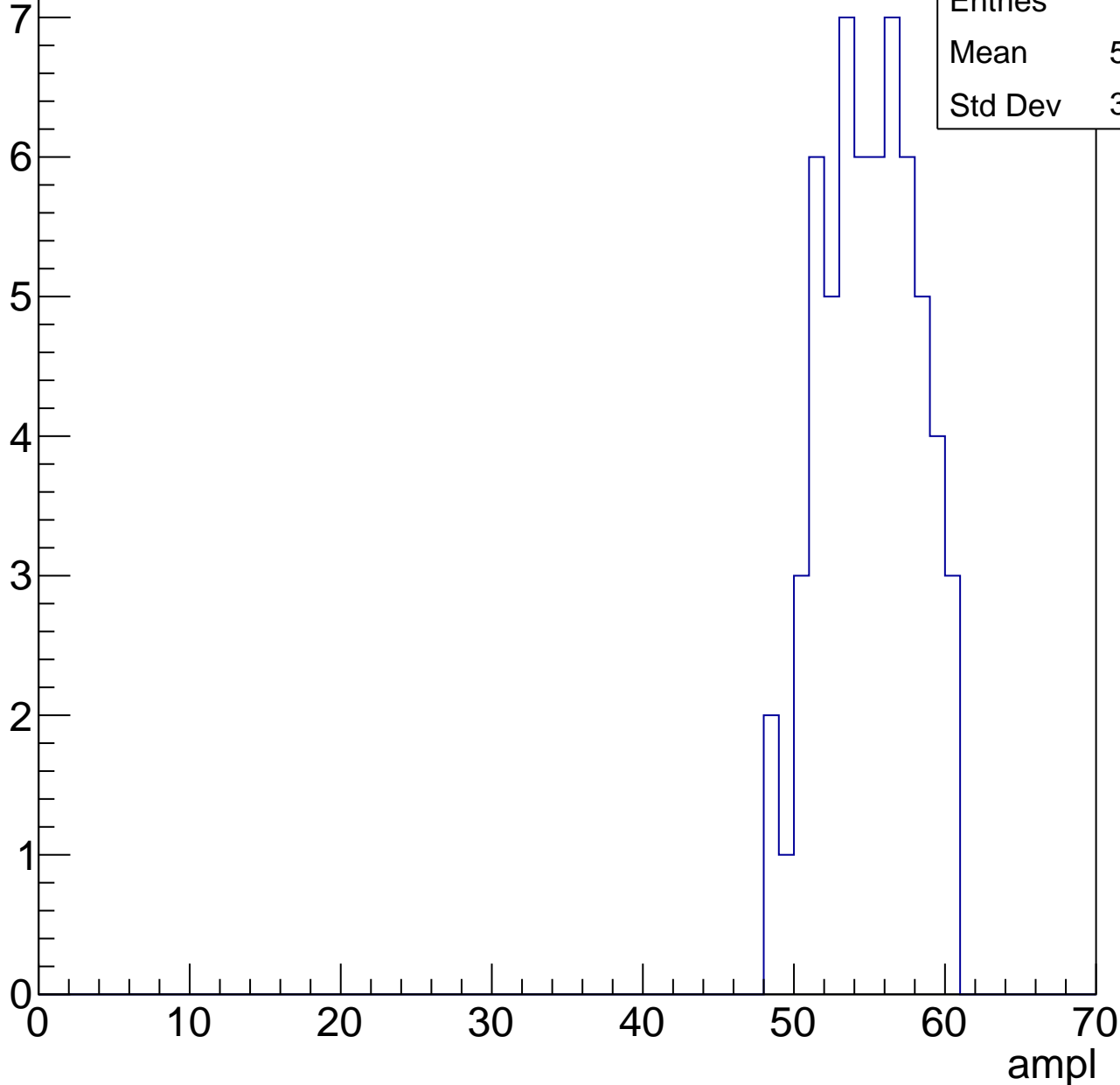
Entries	56
Mean	47.86
Std Dev	3.43



# B1L102S, U16-ch88, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

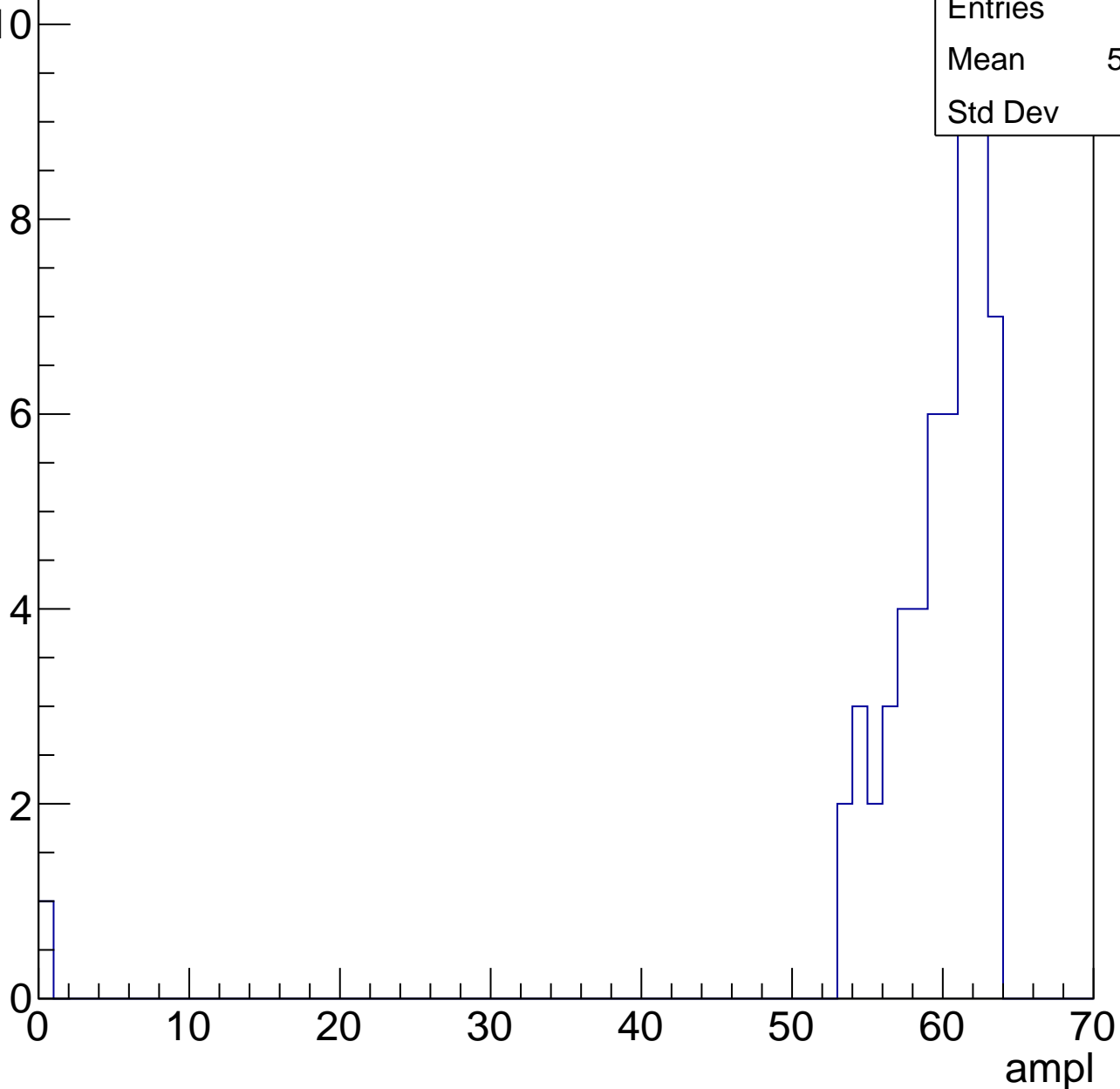


# B1L102S, U16-ch88, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

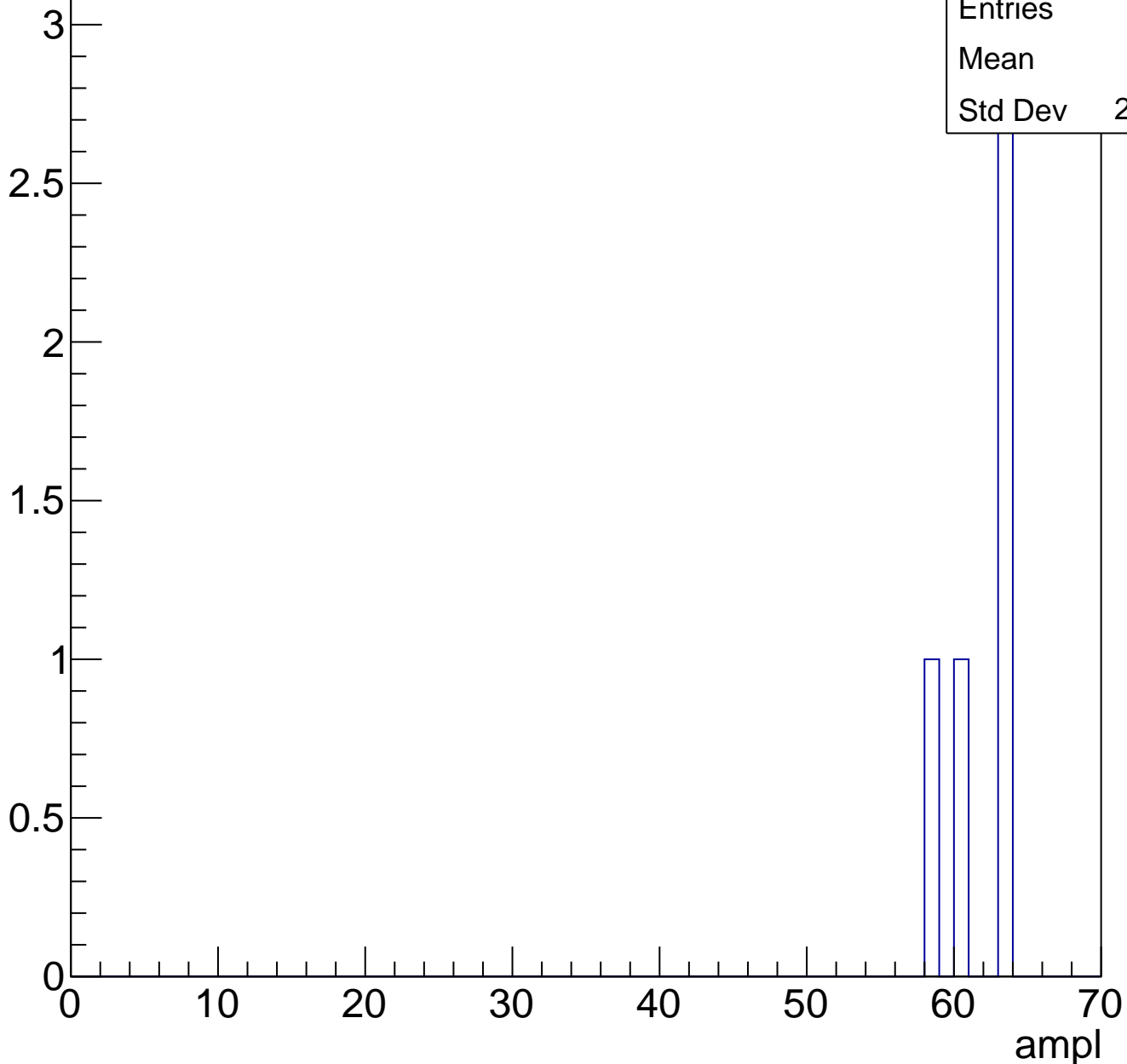
Entries	58
Mean	58.47
Std Dev	8.24



# B1L102S, U16-ch88, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	5
Mean	61.4
Std Dev	2.059



# B1L102S, U16-ch88, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U16-ch89, adc0

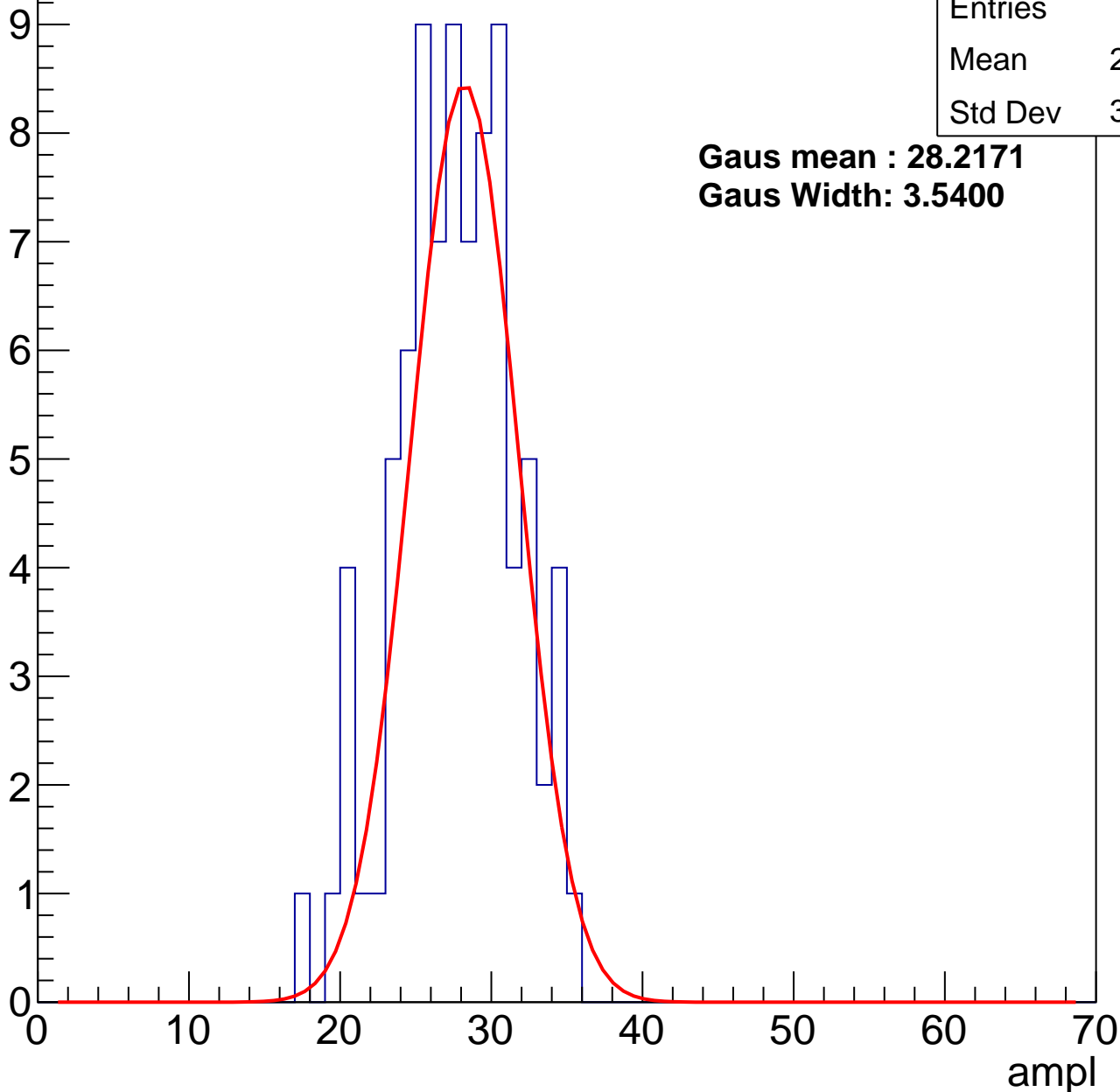
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	27.23
Std Dev	3.834

**Gaus mean : 28.2171**

**Gaus Width: 3.5400**



# B1L102S, U16-ch89, adc1

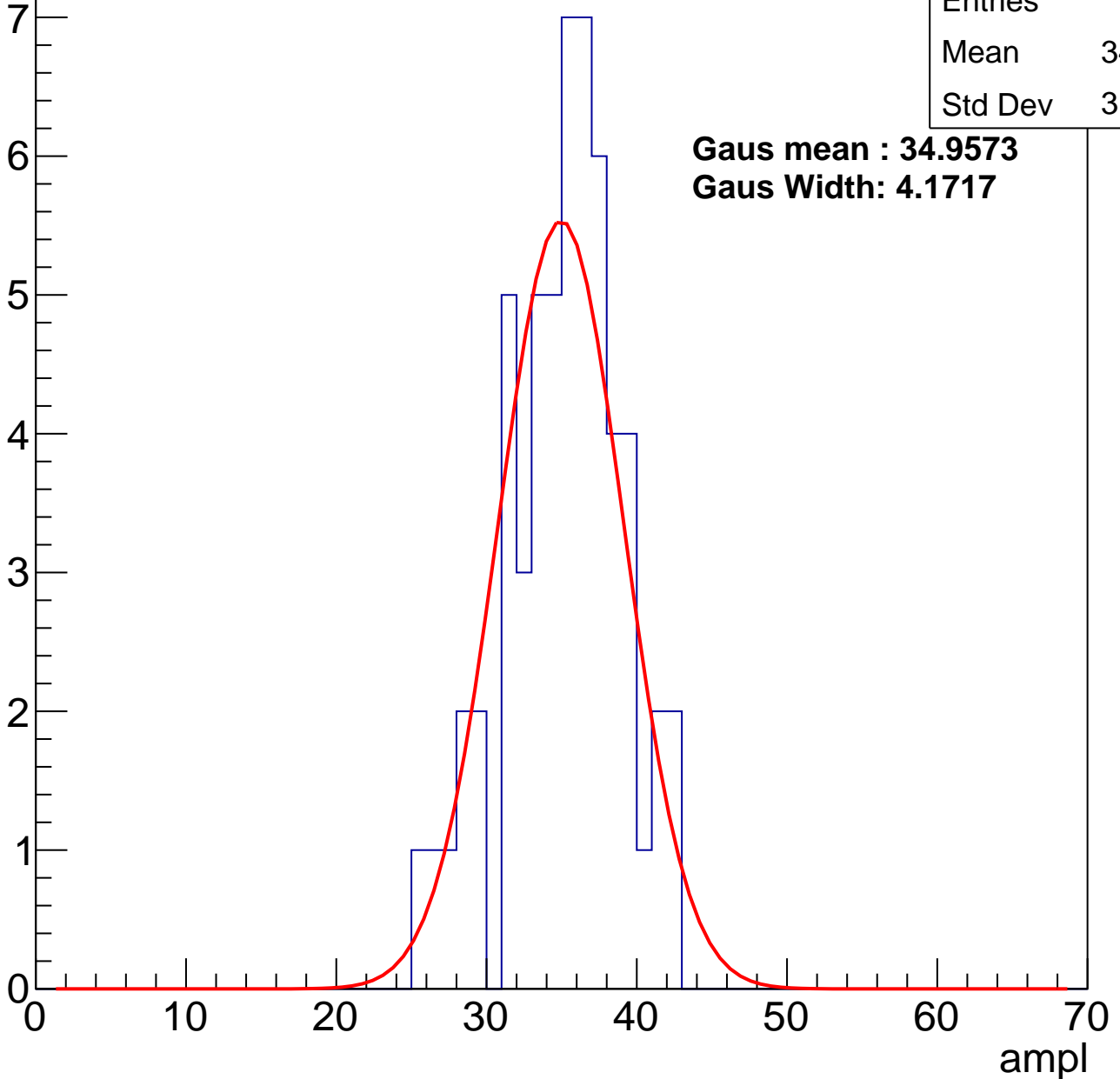
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	34.67
Std Dev	3.866

**Gaus mean : 34.9573**

**Gaus Width: 4.1717**



# B1L102S, U16-ch89, adc2

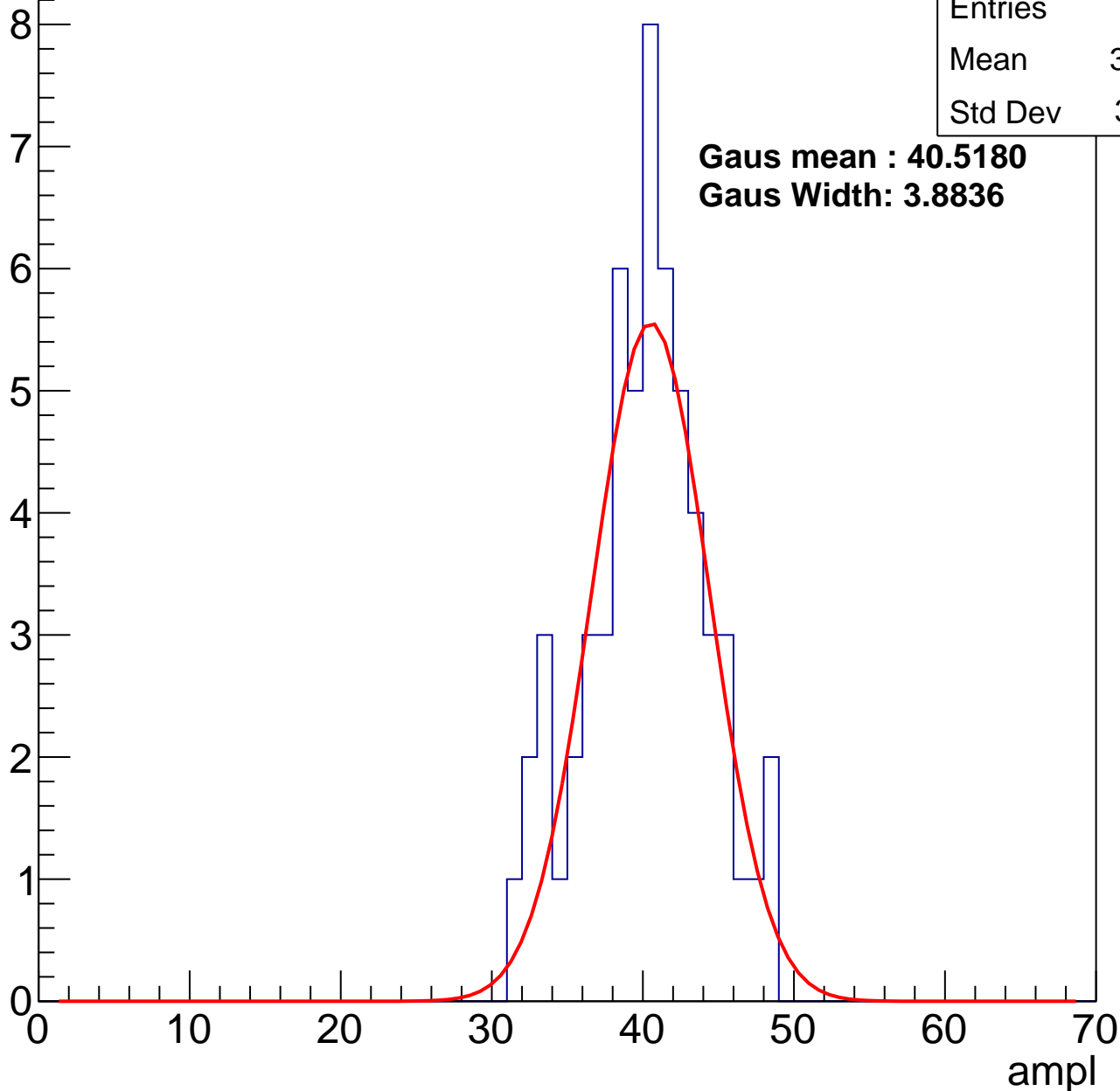
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	39.73
Std Dev	3.991

**Gaus mean : 40.5180**

**Gaus Width: 3.8836**

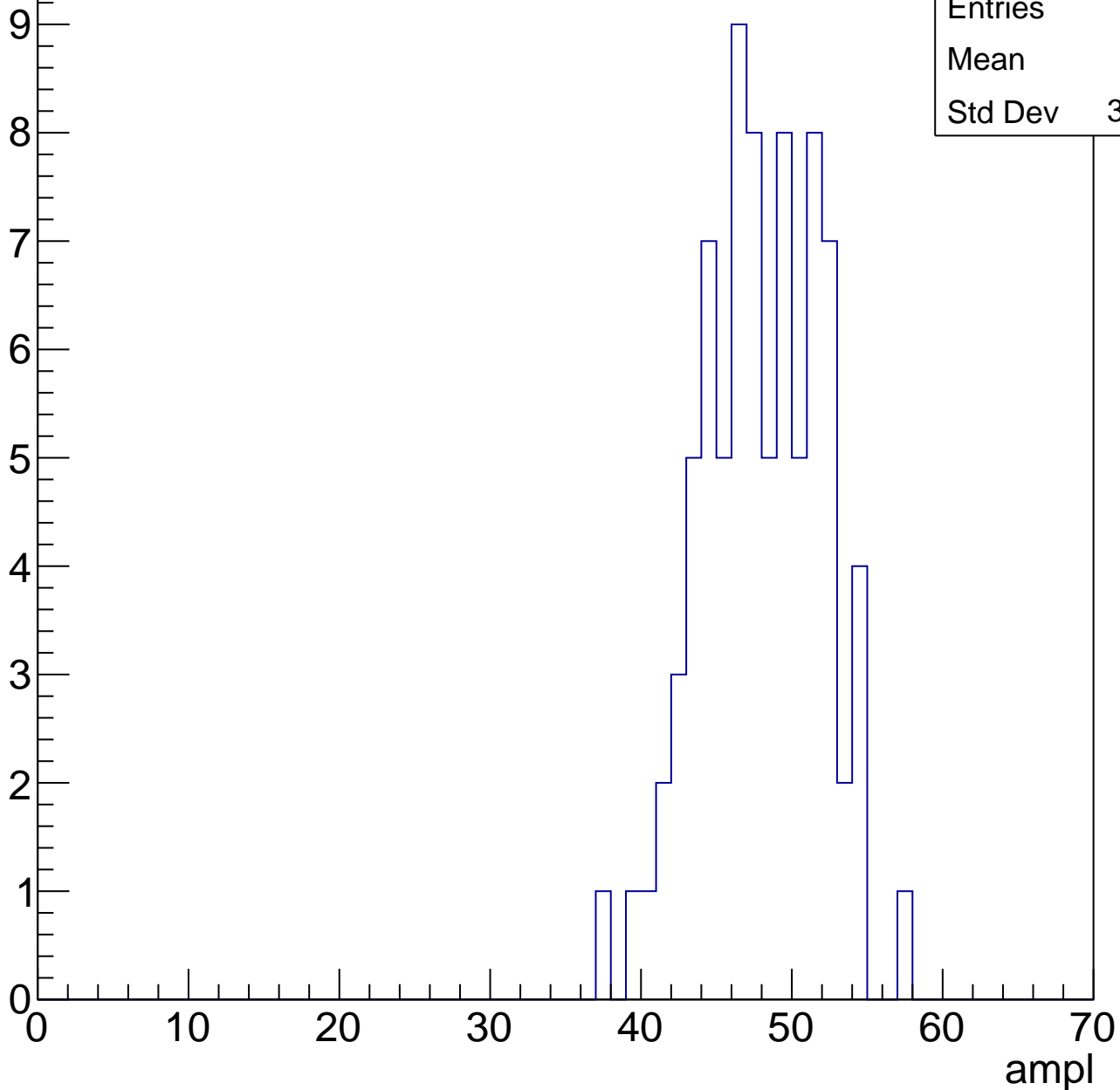


# B1L102S, U16-ch89, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

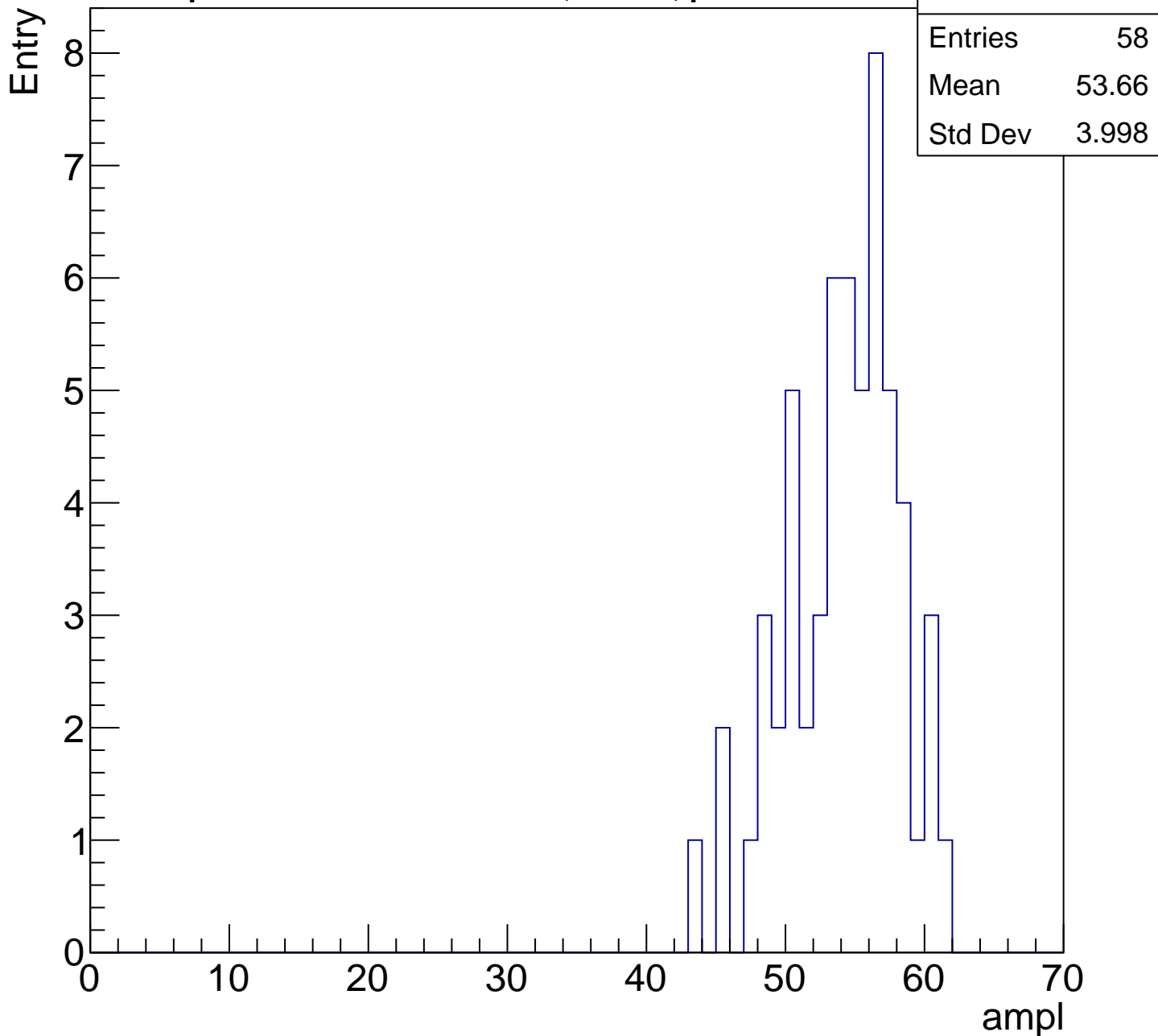
Entry

Entries	82
Mean	47.5
Std Dev	3.927



# B1L102S, U16-ch89, adc4

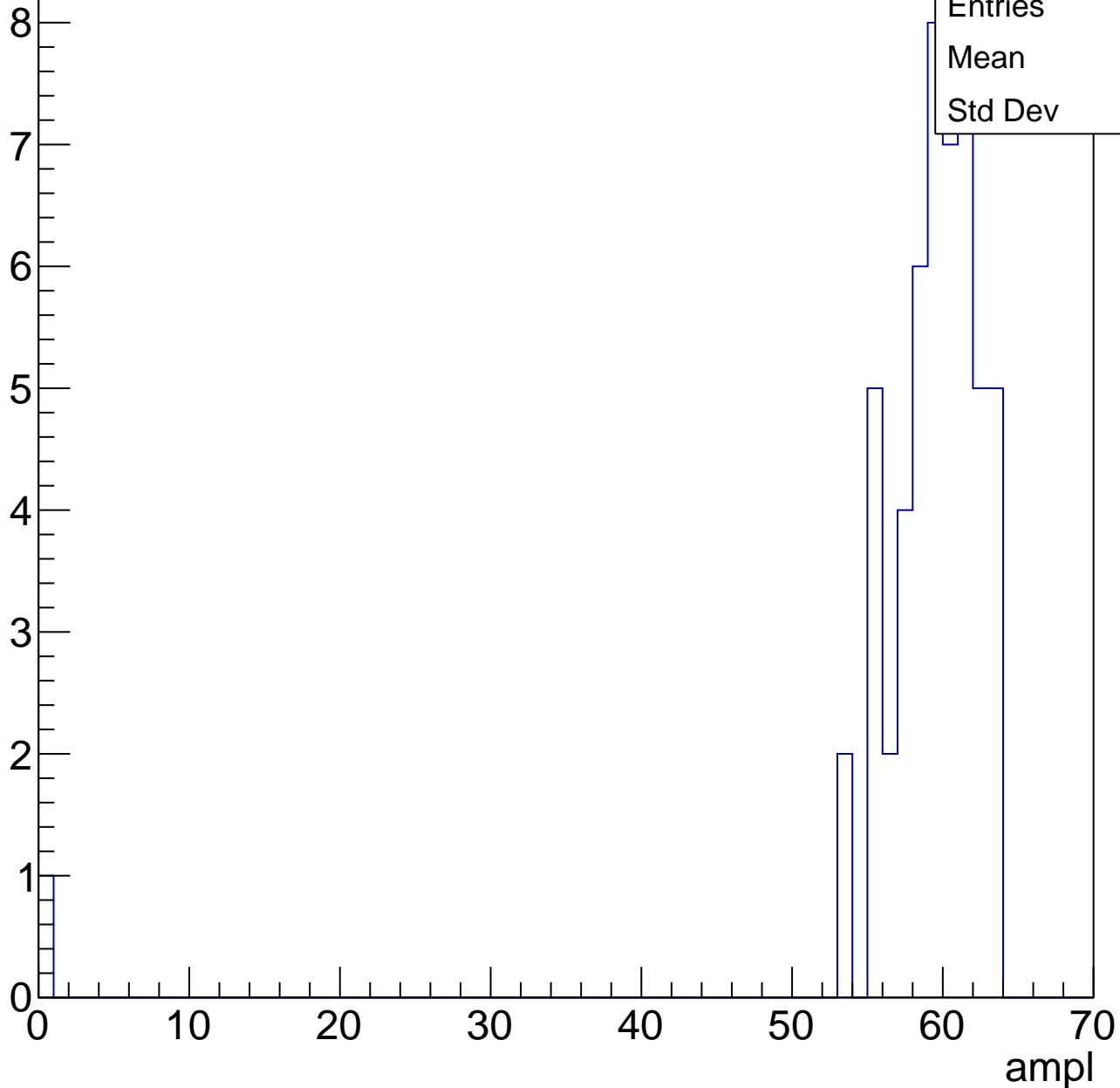
calib\_packv5\_042523\_0143.root, FC#11, port A2



# B1L102S, U16-ch89, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

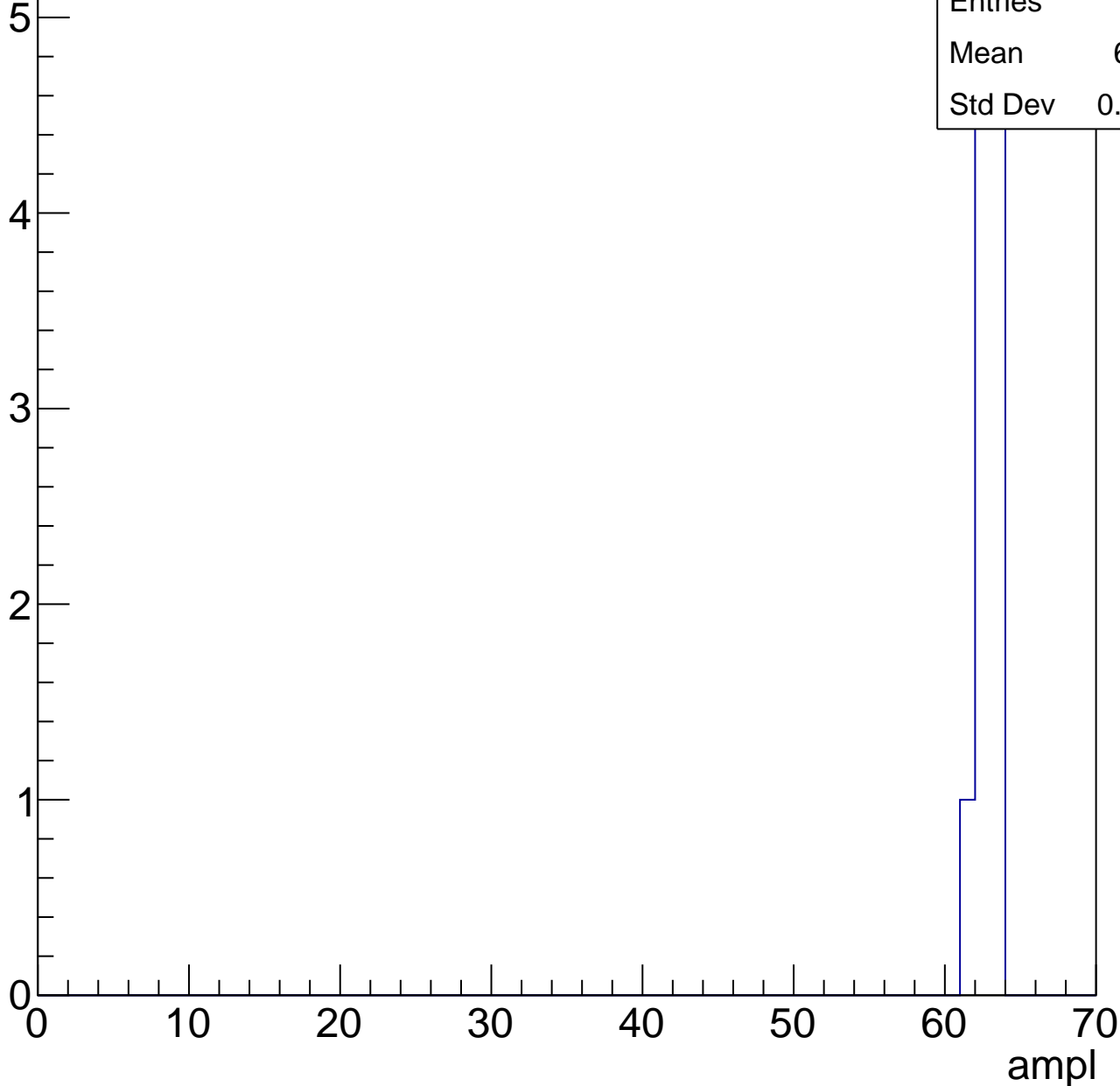


# B1L102S, U16-ch89, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	11
Mean	62.36
Std Dev	0.6428

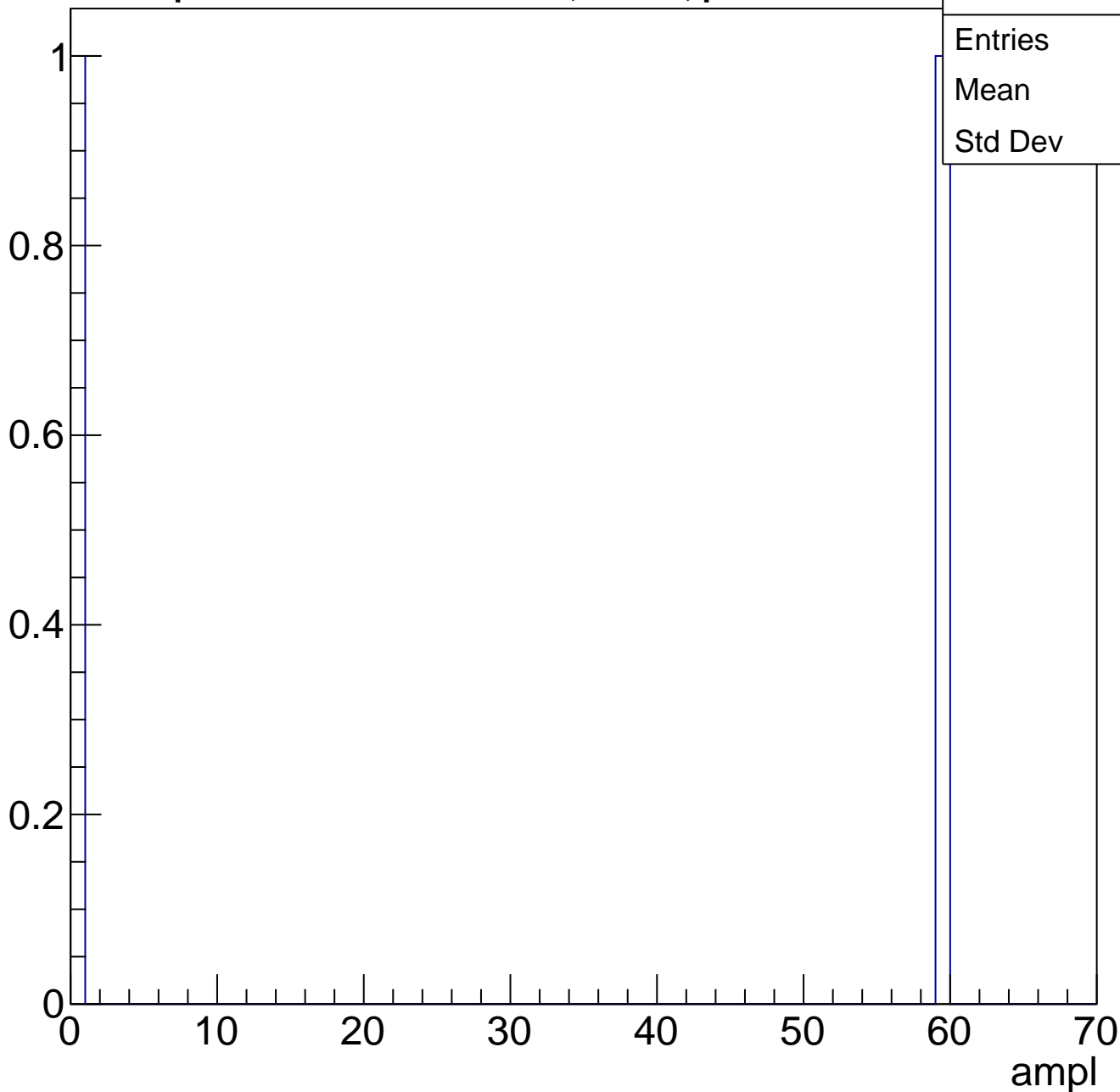




# B1L102S, U16-ch89, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch90, adc0

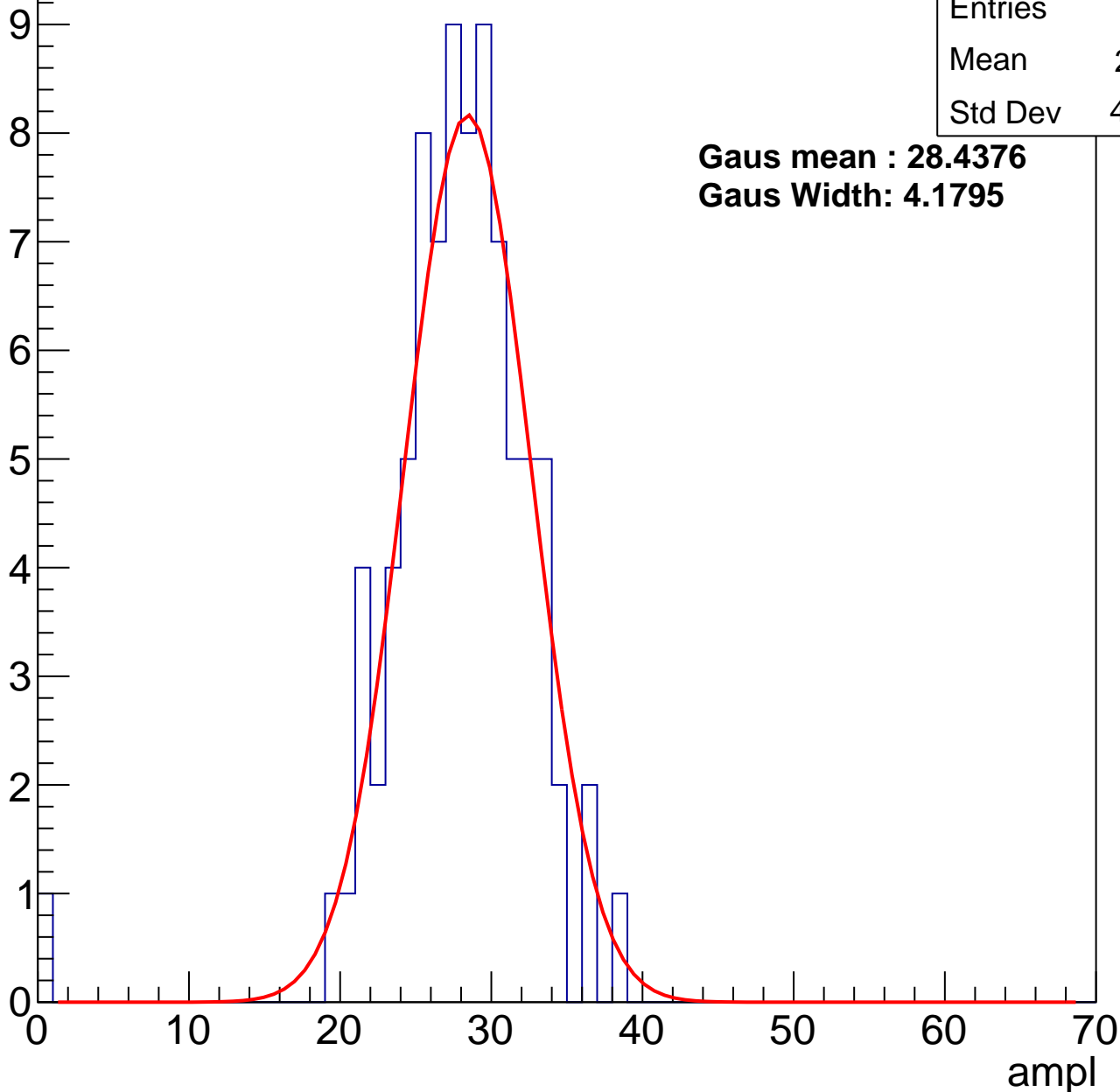
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	86
Mean	27.41
Std Dev	4.874

**Gaus mean : 28.4376**

**Gaus Width: 4.1795**



# B1L102S, U16-ch90, adc1

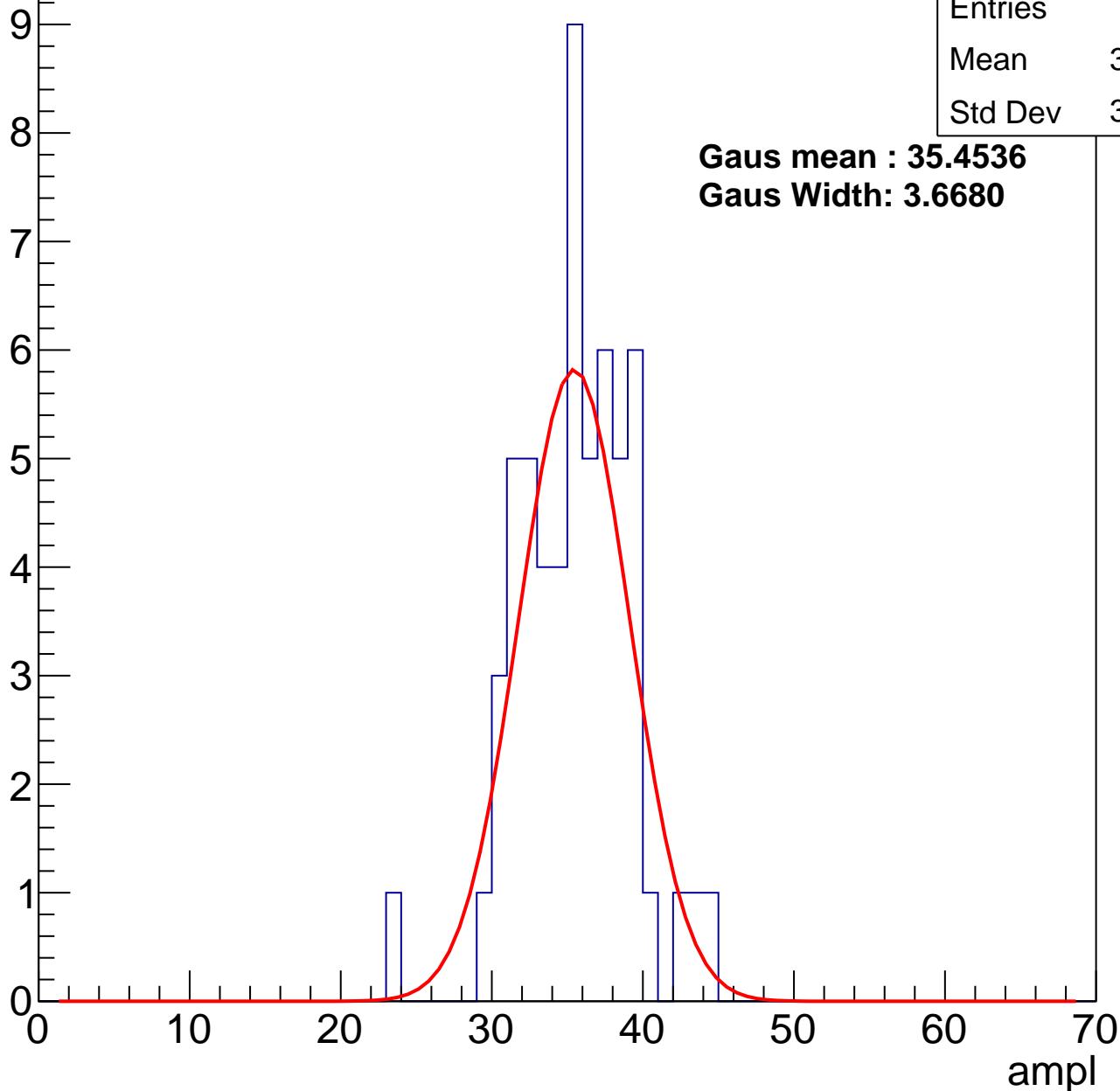
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	35.09
Std Dev	3.687

**Gaus mean : 35.4536**

**Gaus Width: 3.6680**



# B1L102S, U16-ch90, adc2

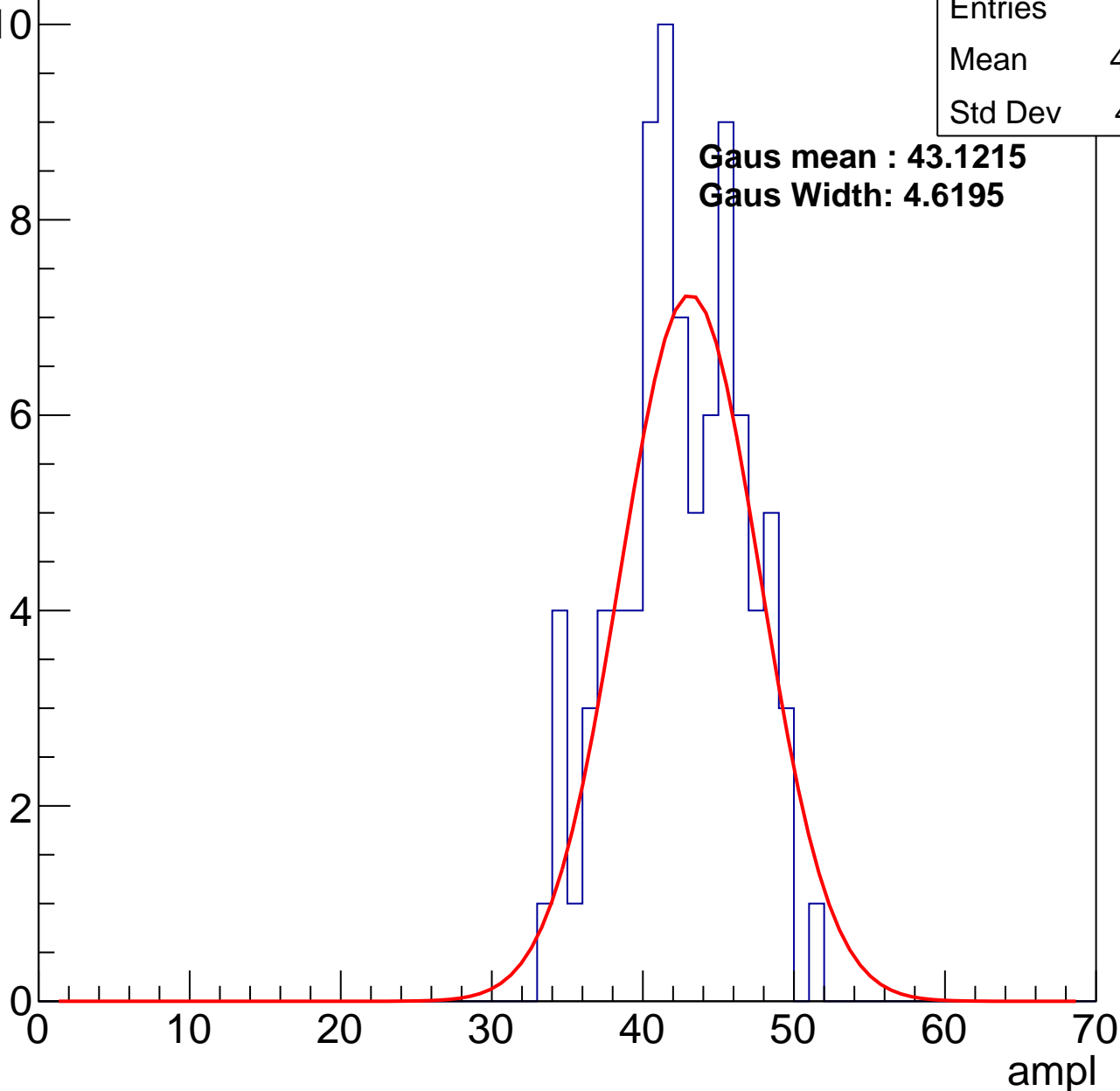
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	86
Mean	42.07
Std Dev	4.111

**Gaus mean : 43.1215**

**Gaus Width: 4.6195**

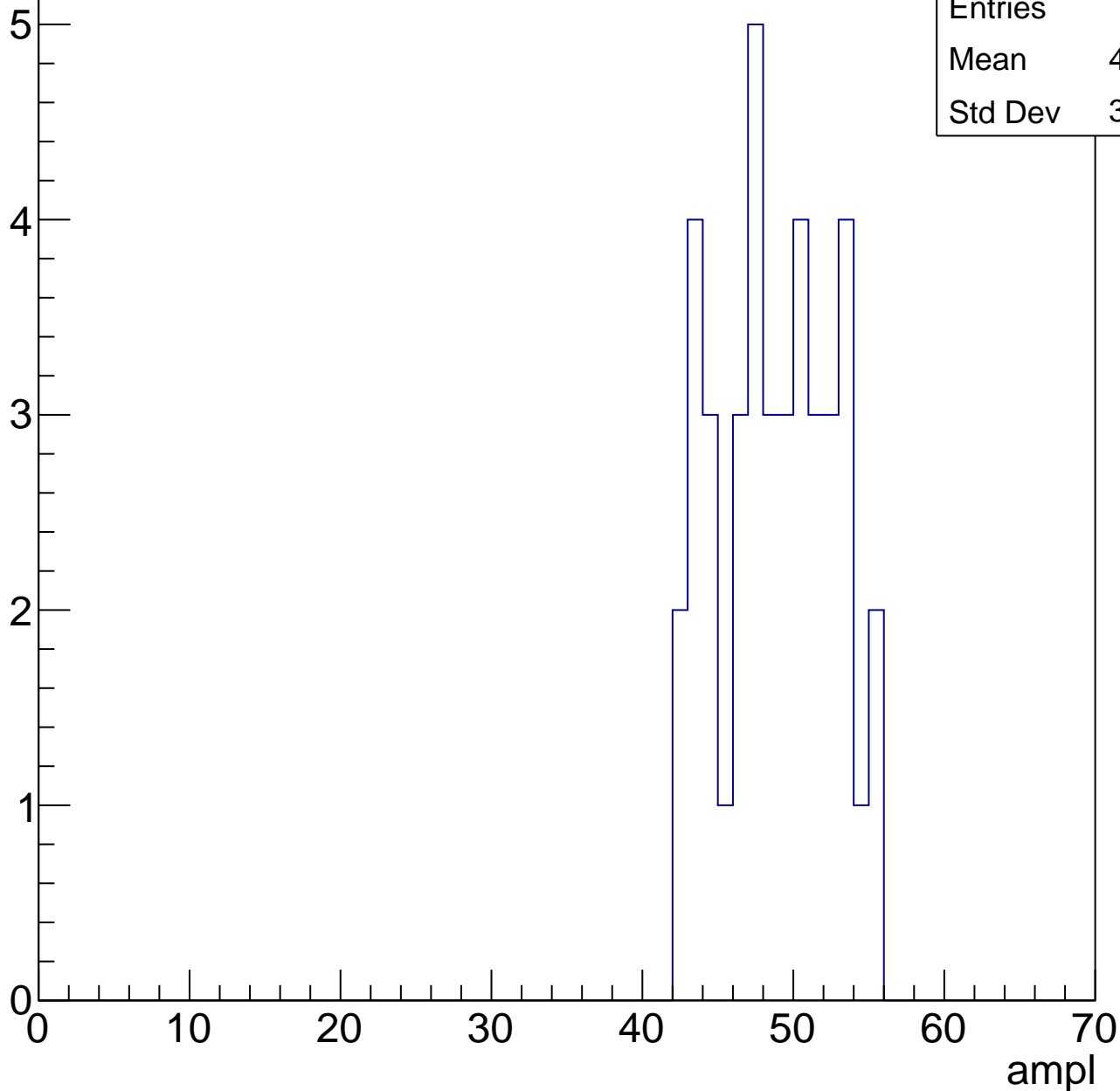


# B1L102S, U16-ch90, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	41
Mean	48.34
Std Dev	3.726



# B1L102S, U16-ch90, adc4

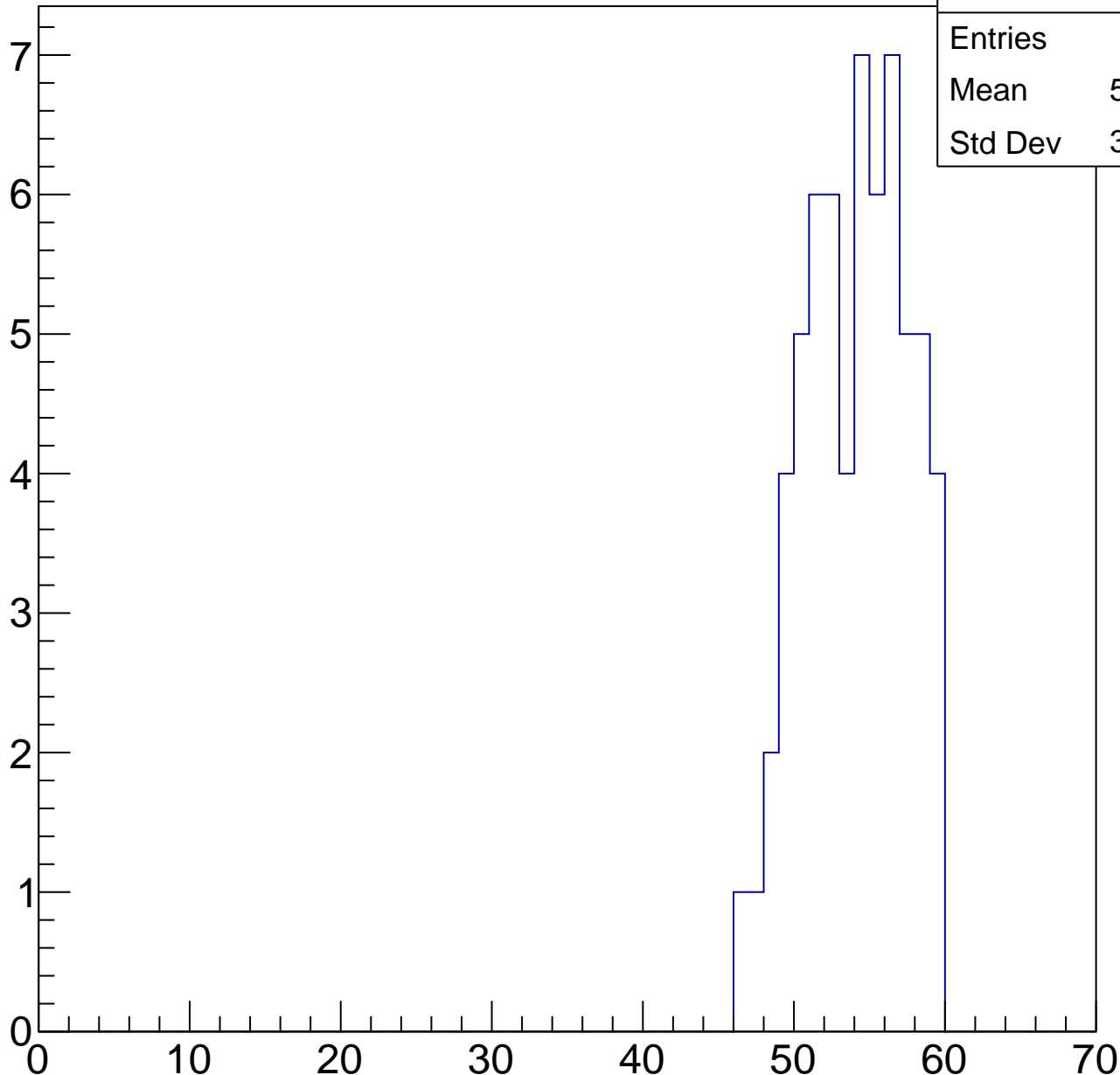
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	63
Mean	53.59
Std Dev	3.322

ampl



# B1L102S, U16-ch90, adc5

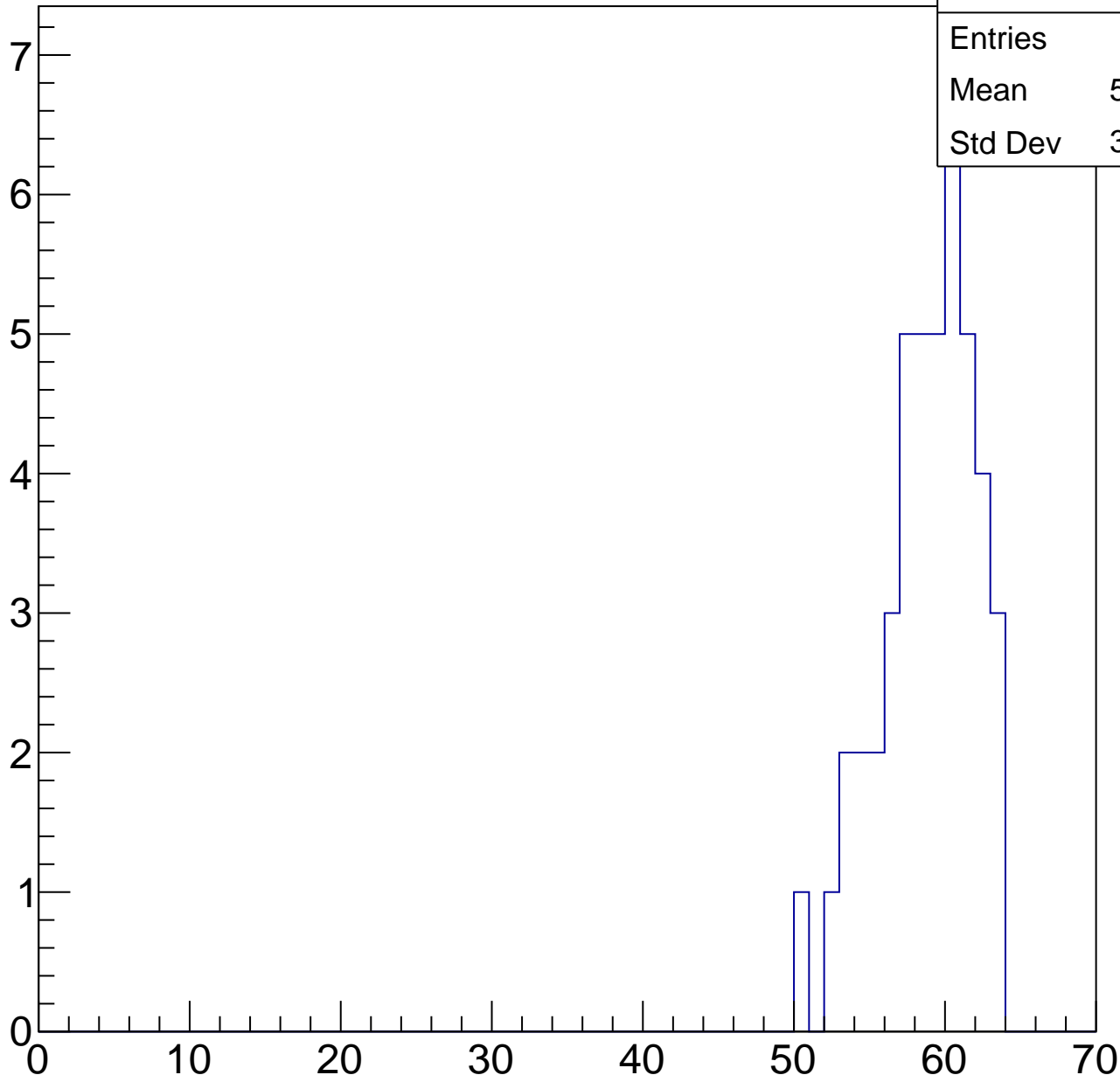
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

7  
6  
5  
4  
3  
2  
1  
0

Entries	45
Mean	58.36
Std Dev	3.085

ampl

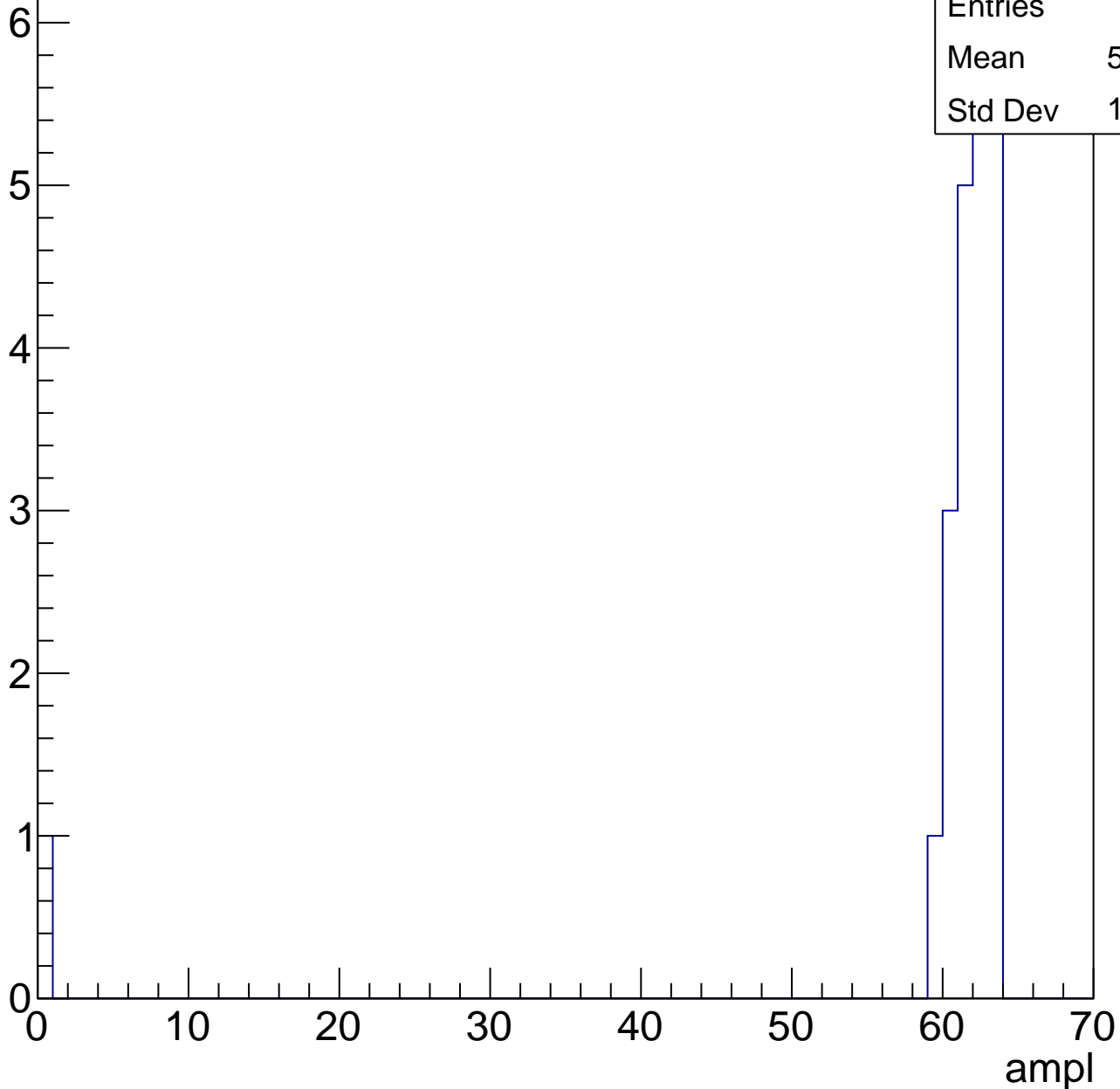


# B1L102S, U16-ch90, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	22
Mean	58.82
Std Dev	12.89





# B1L102S, U16-ch90, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	63
Std Dev	0

# B1L102S, U16-ch91, adc0

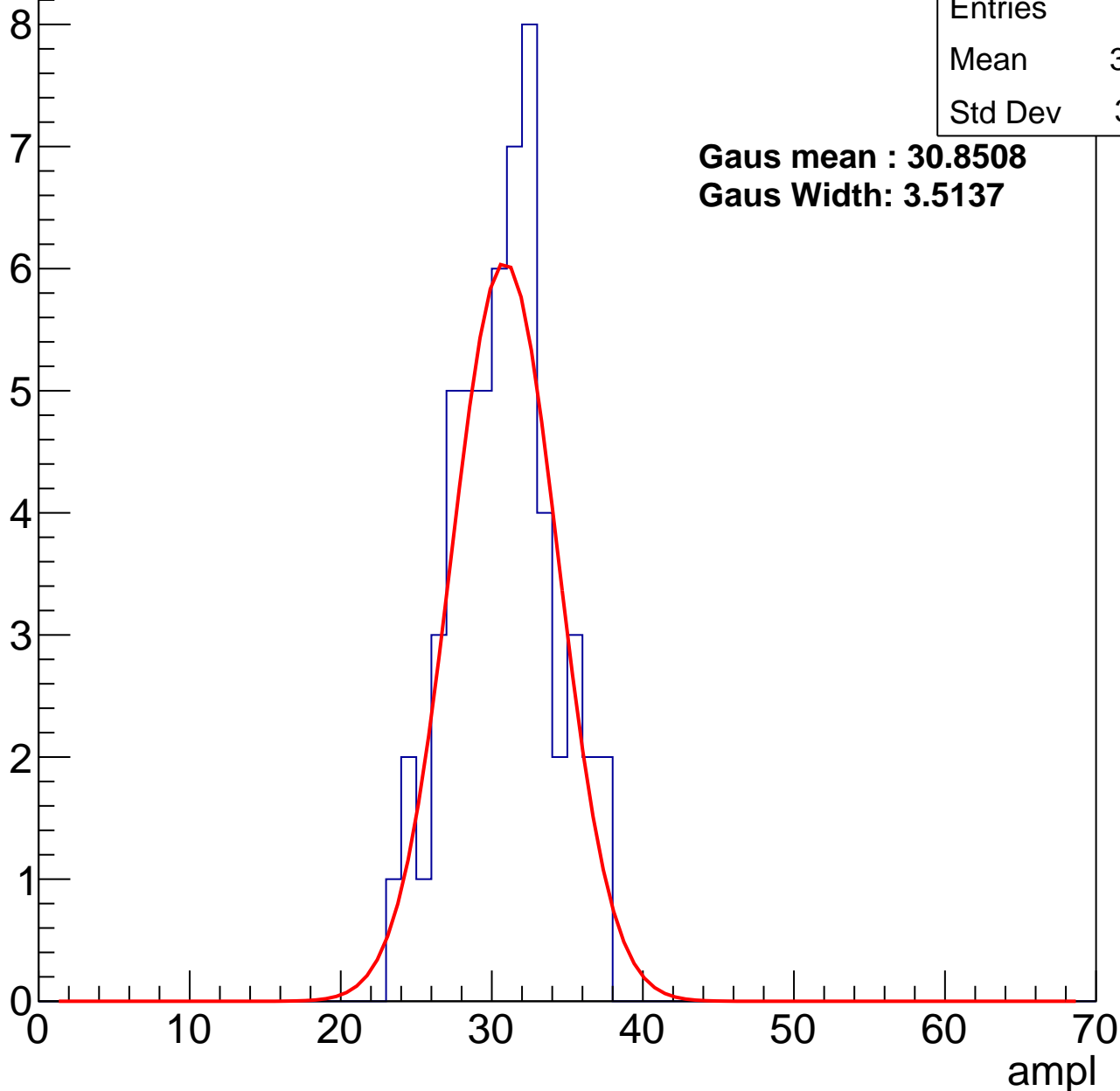
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	30.32
Std Dev	3.301

**Gaus mean : 30.8508**

**Gaus Width: 3.5137**



# B1L102S, U16-ch91, adc1

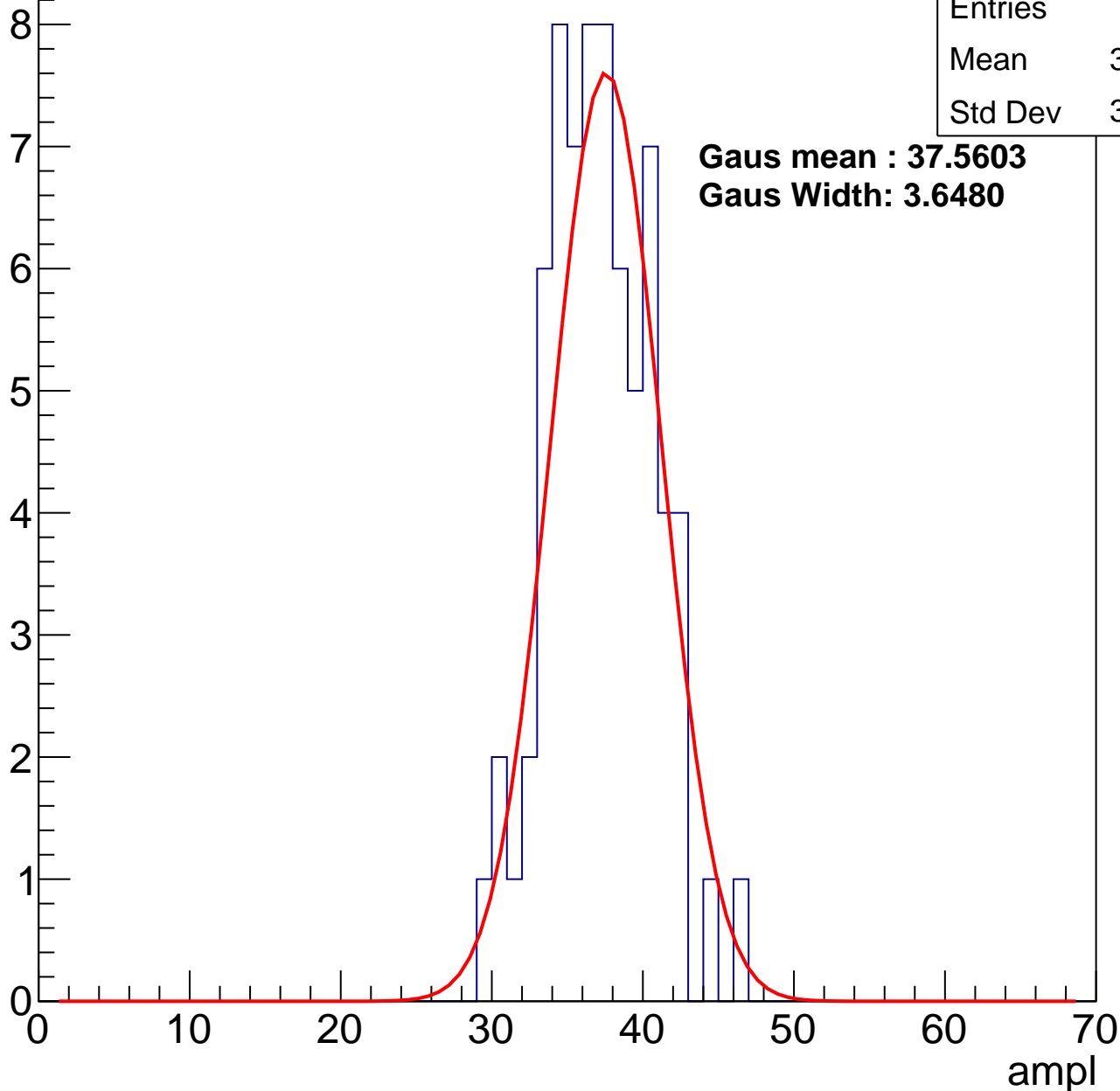
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	36.73
Std Dev	3.419

**Gaus mean : 37.5603**

**Gaus Width: 3.6480**



# B1L102S, U16-ch91, adc2

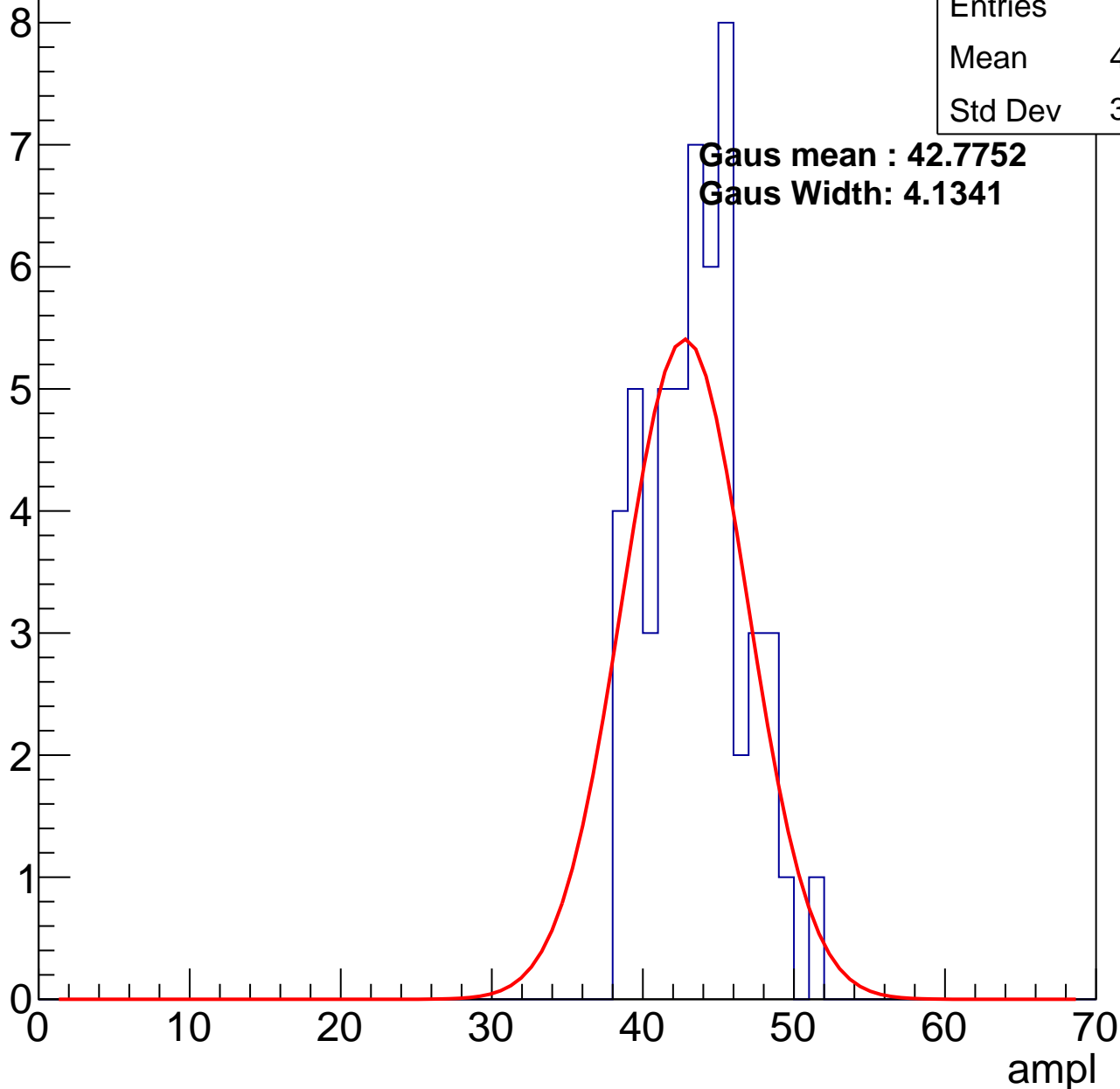
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	43.09
Std Dev	3.104

**Gaus mean : 42.7752**

**Gaus Width: 4.1341**



# B1L102S, U16-ch91, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	77
Mean	49.4
Std Dev	3.673

Entry

10

8

6

4

2

0

0

10

20

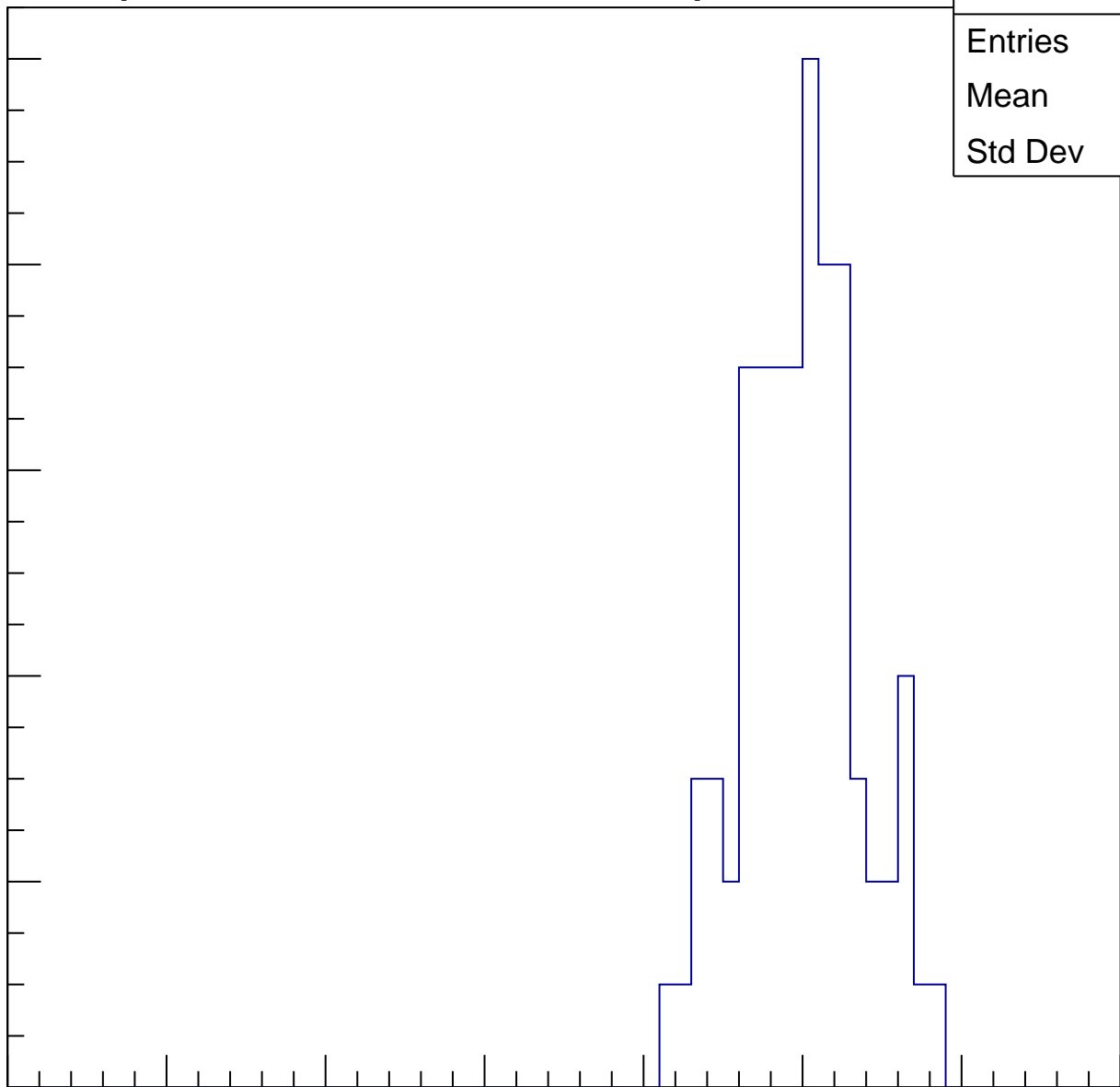
30

40

50

60

ampl

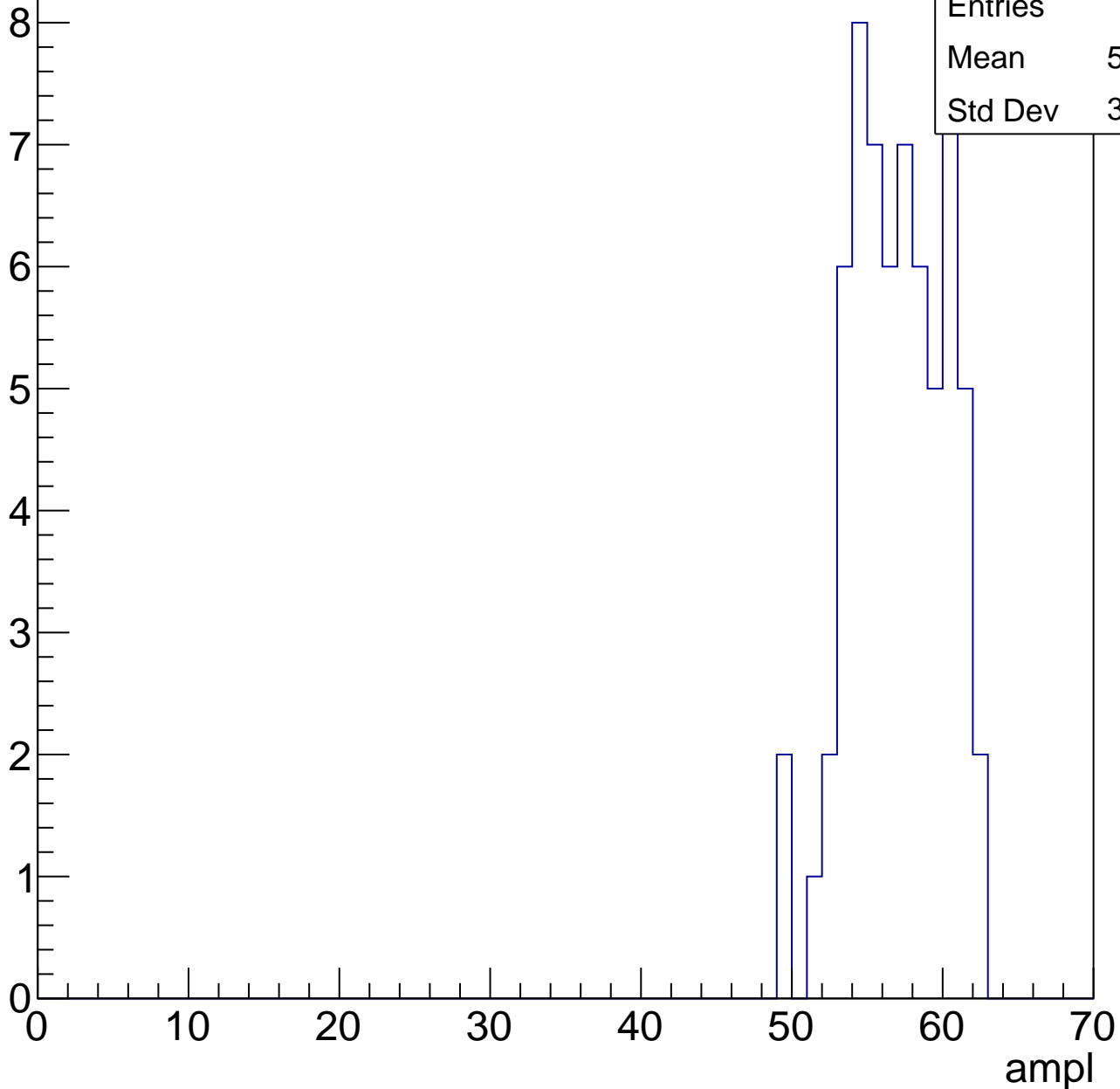


# B1L102S, U16-ch91, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	56.54
Std Dev	3.114

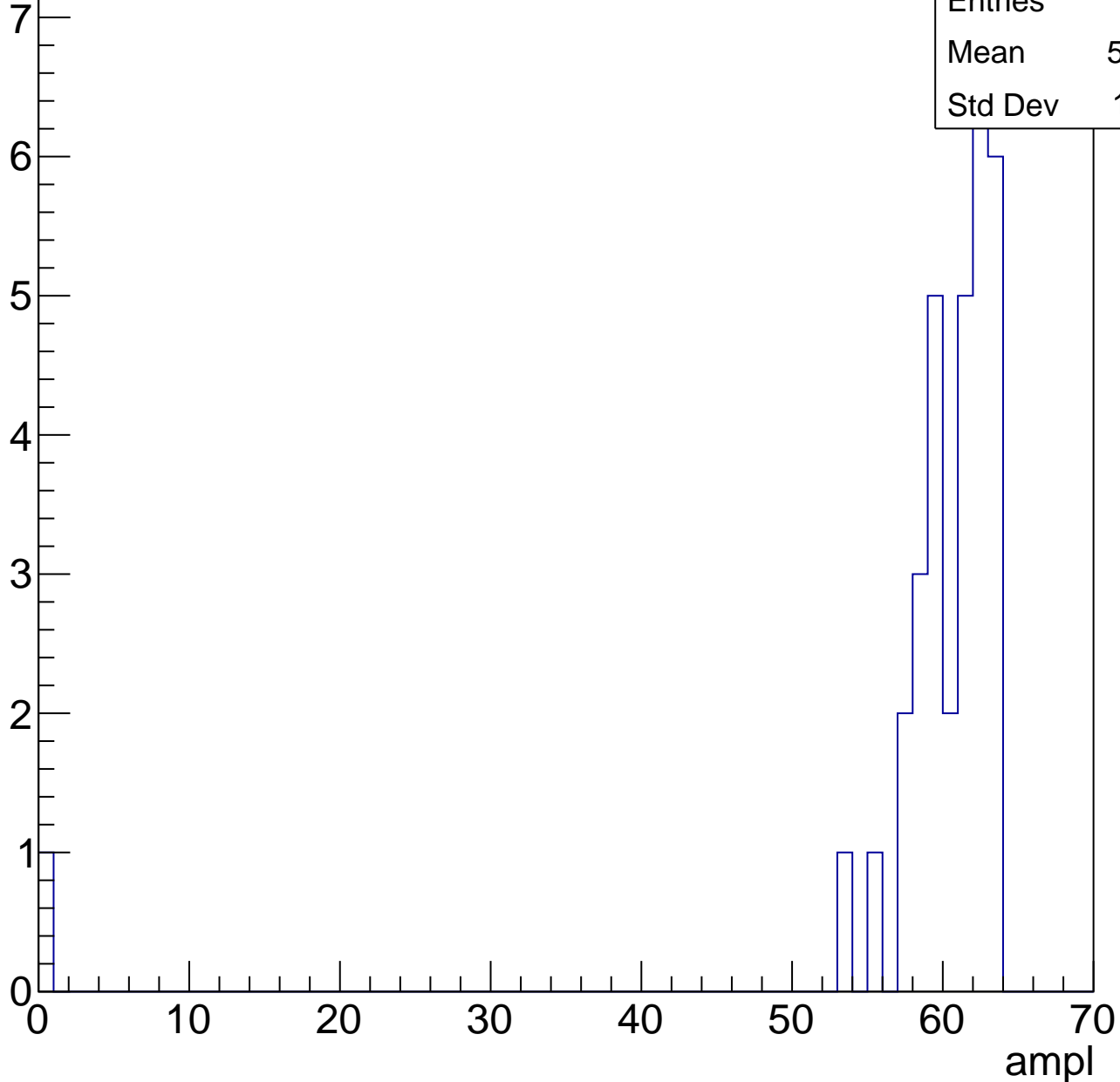


# B1L102S, U16-ch91, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	33
Mean	58.42
Std Dev	10.61



# B1L102S, U16-ch91, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

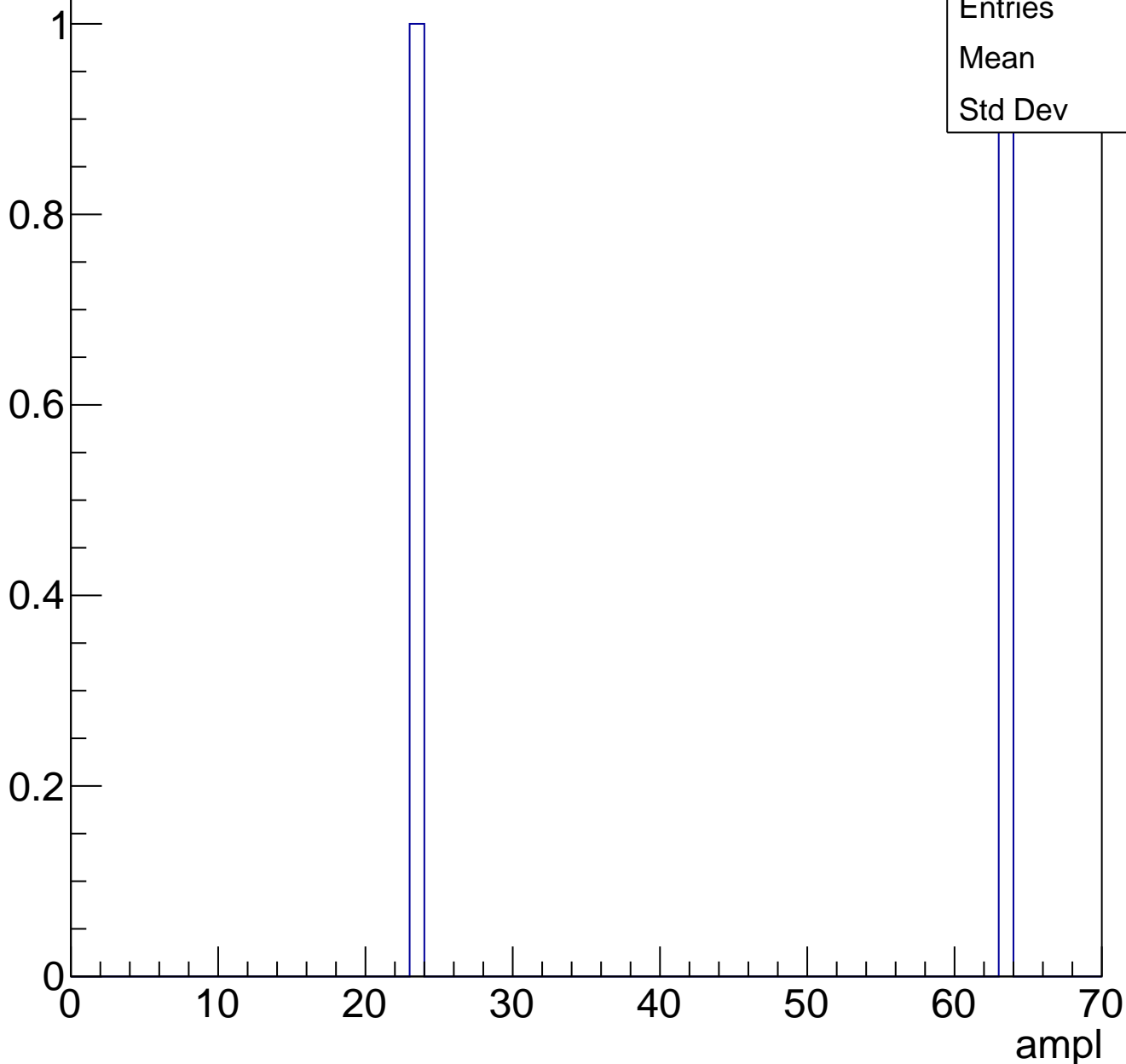




# B1L102S, U16-ch91, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch92, adc0

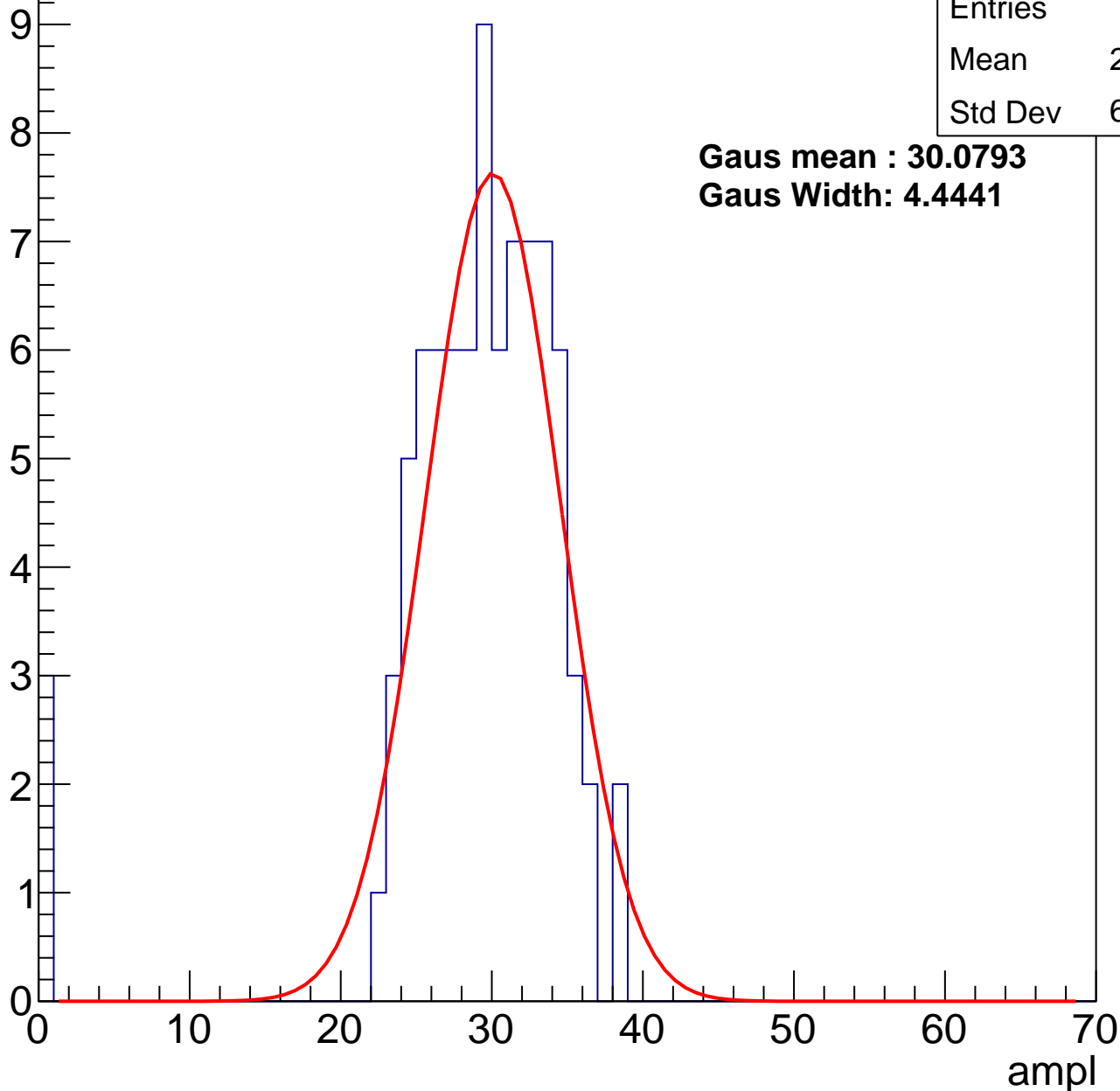
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	85
Mean	28.44
Std Dev	6.584

**Gaus mean : 30.0793**

**Gaus Width: 4.4441**

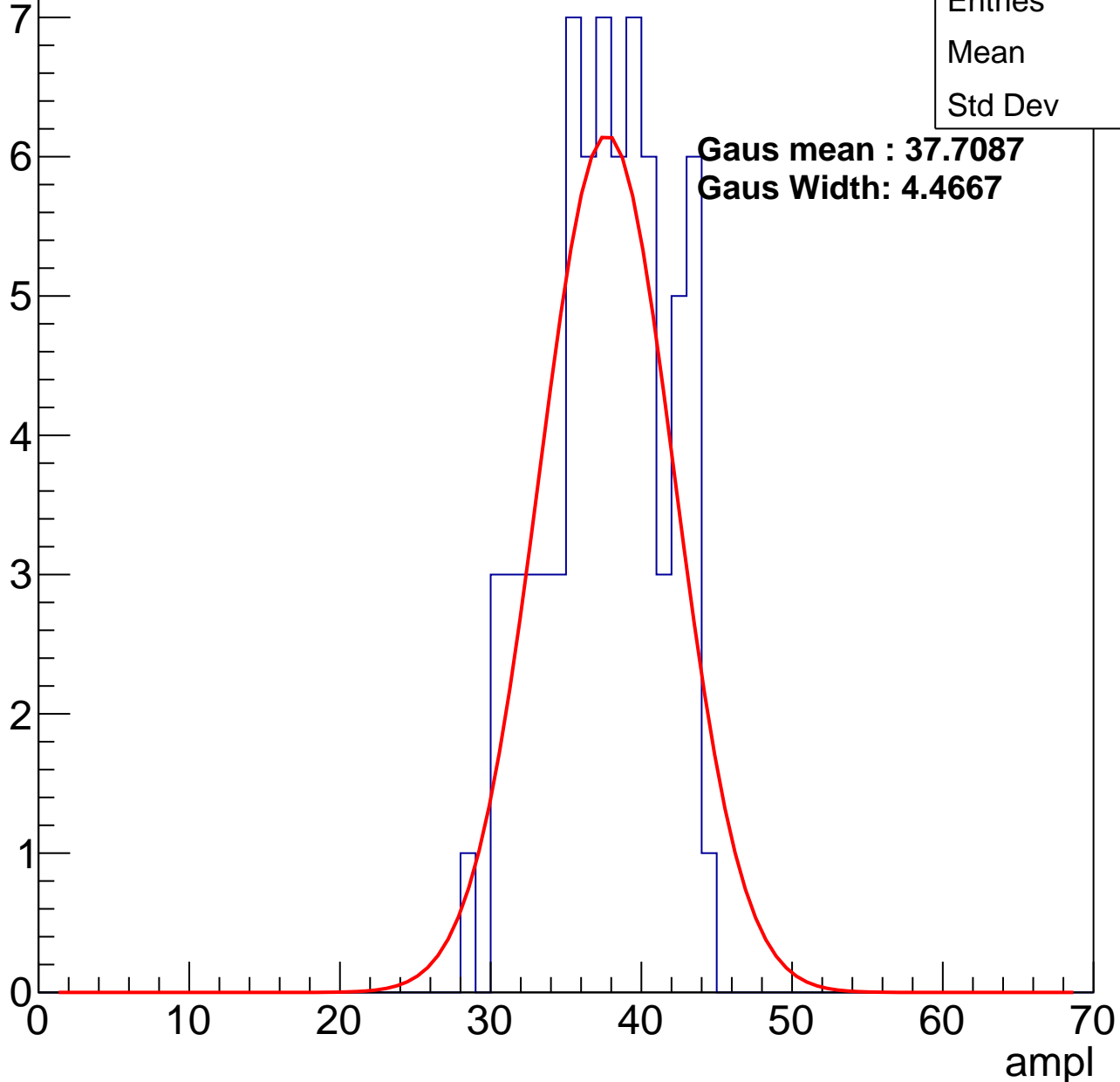


# B1L102S, U16-ch92, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	37.2
Std Dev	3.86



# B1L102S, U16-ch92, adc2

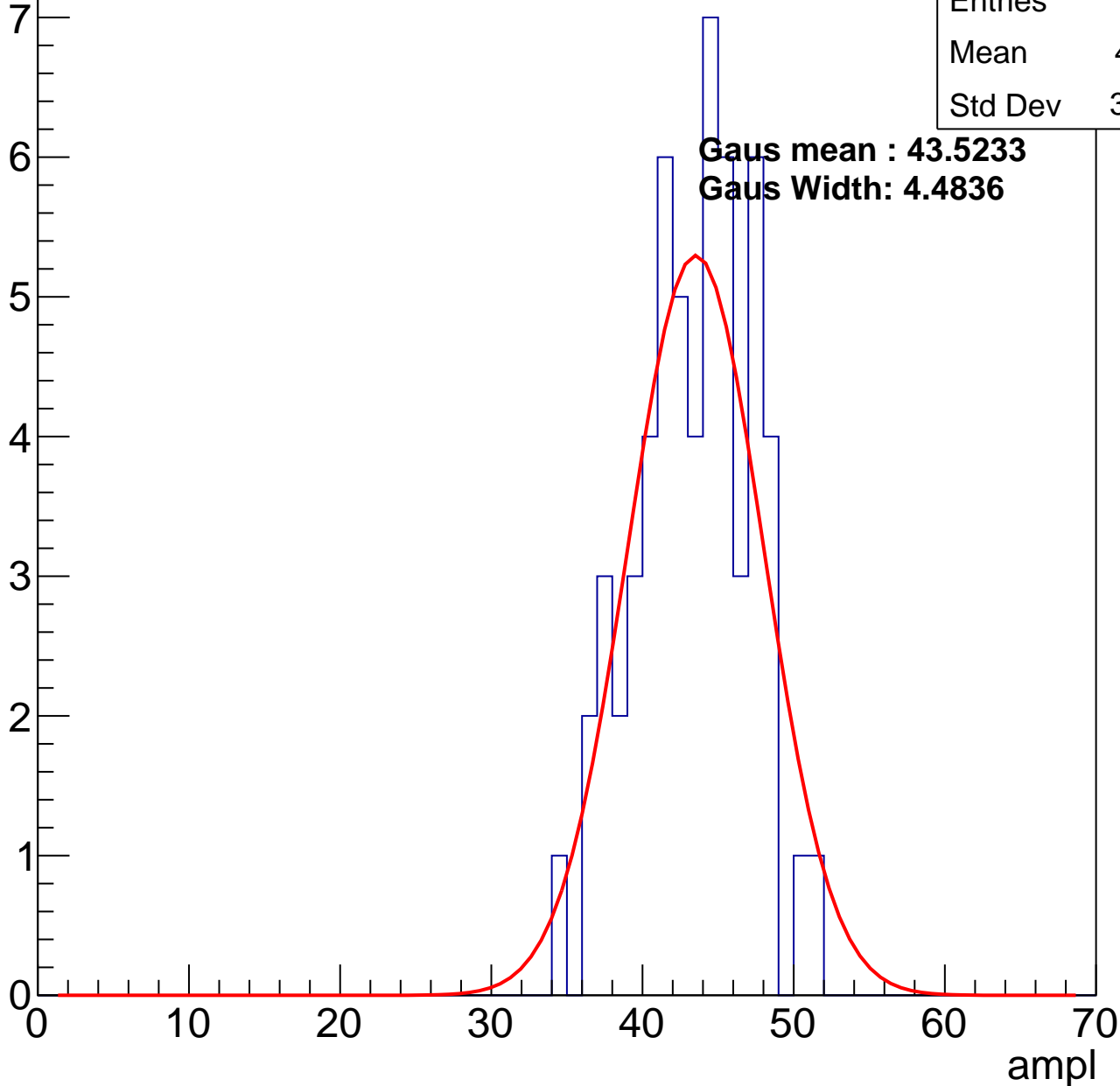
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	42.91
Std Dev	3.752

**Gaus mean : 43.5233**

**Gaus Width: 4.4836**

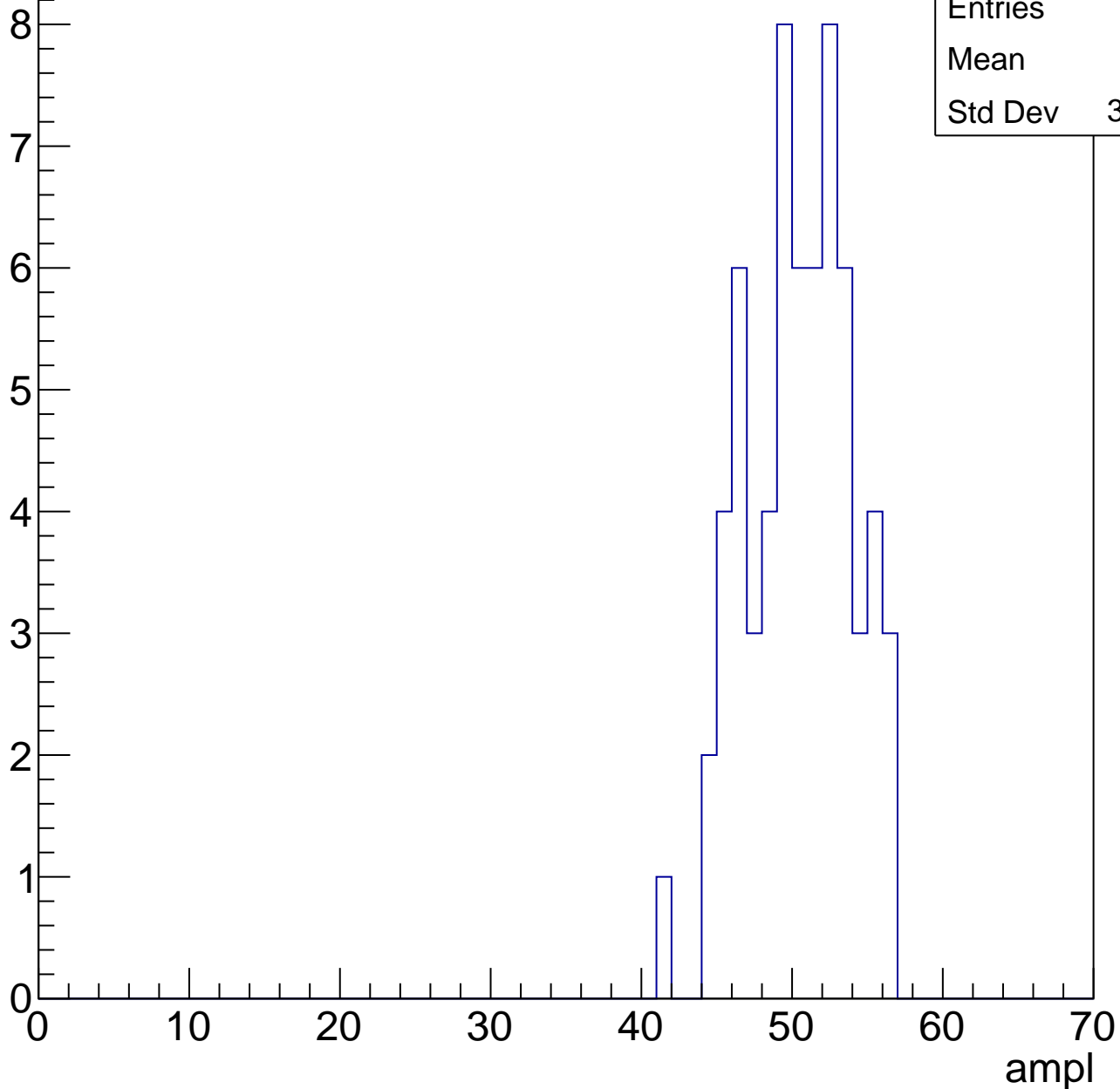


# B1L102S, U16-ch92, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	50
Std Dev	3.419

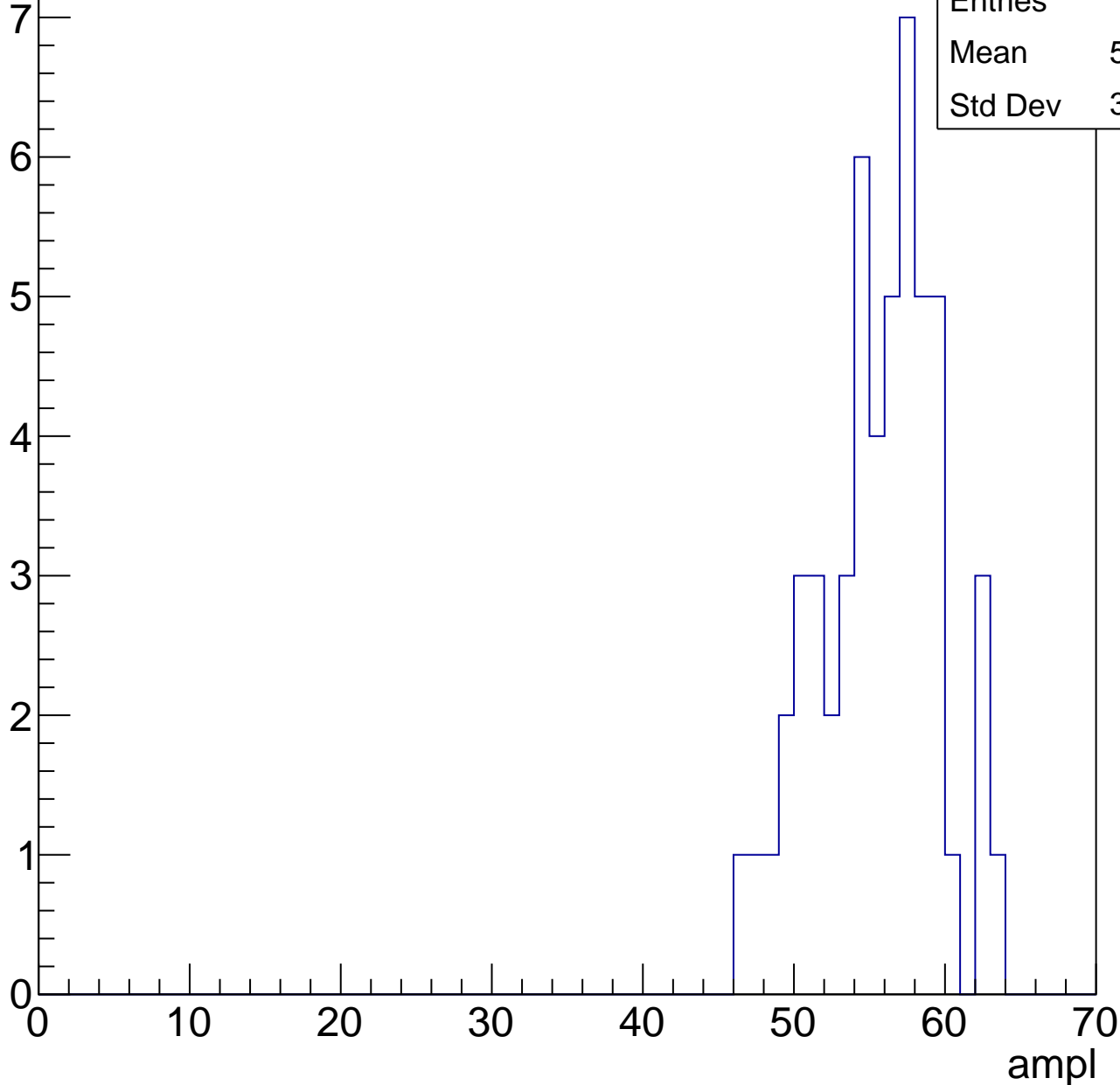


# B1L102S, U16-ch92, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	55.13
Std Dev	3.929

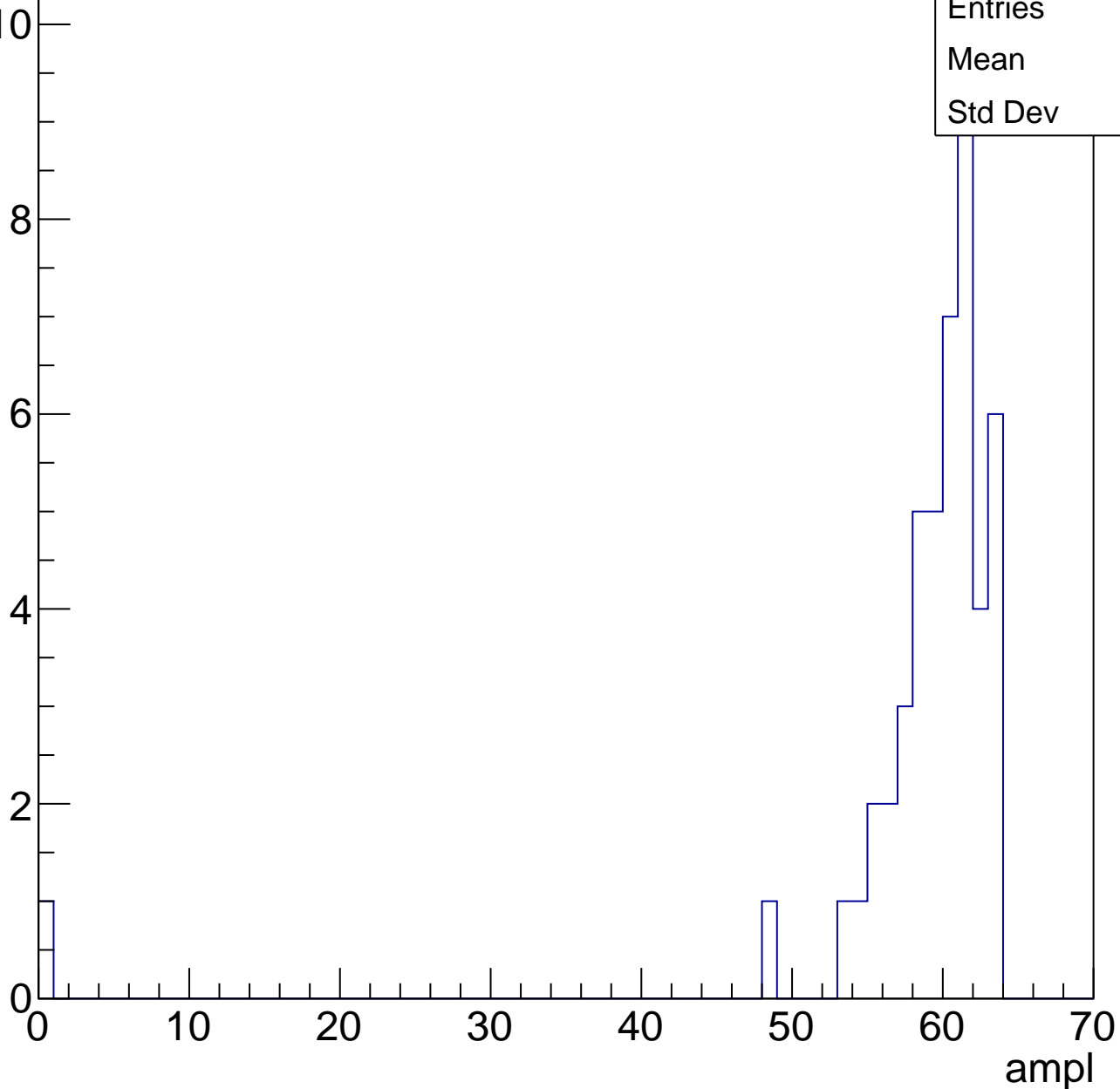


# B1L102S, U16-ch92, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

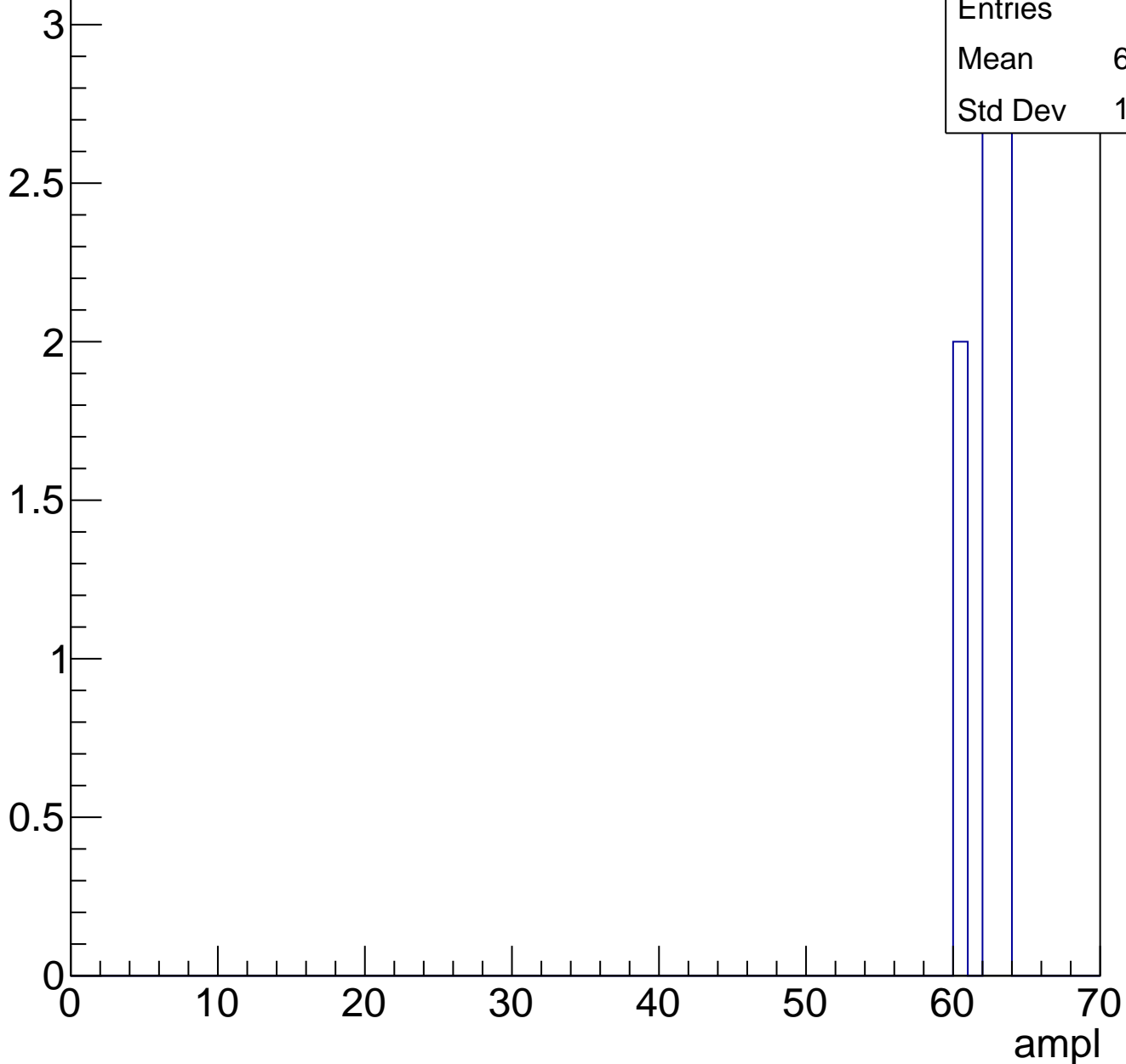
Entries	48
Mean	58.1
Std Dev	8.98



# B1L102S, U16-ch92, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch92, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U16-ch93, adc0

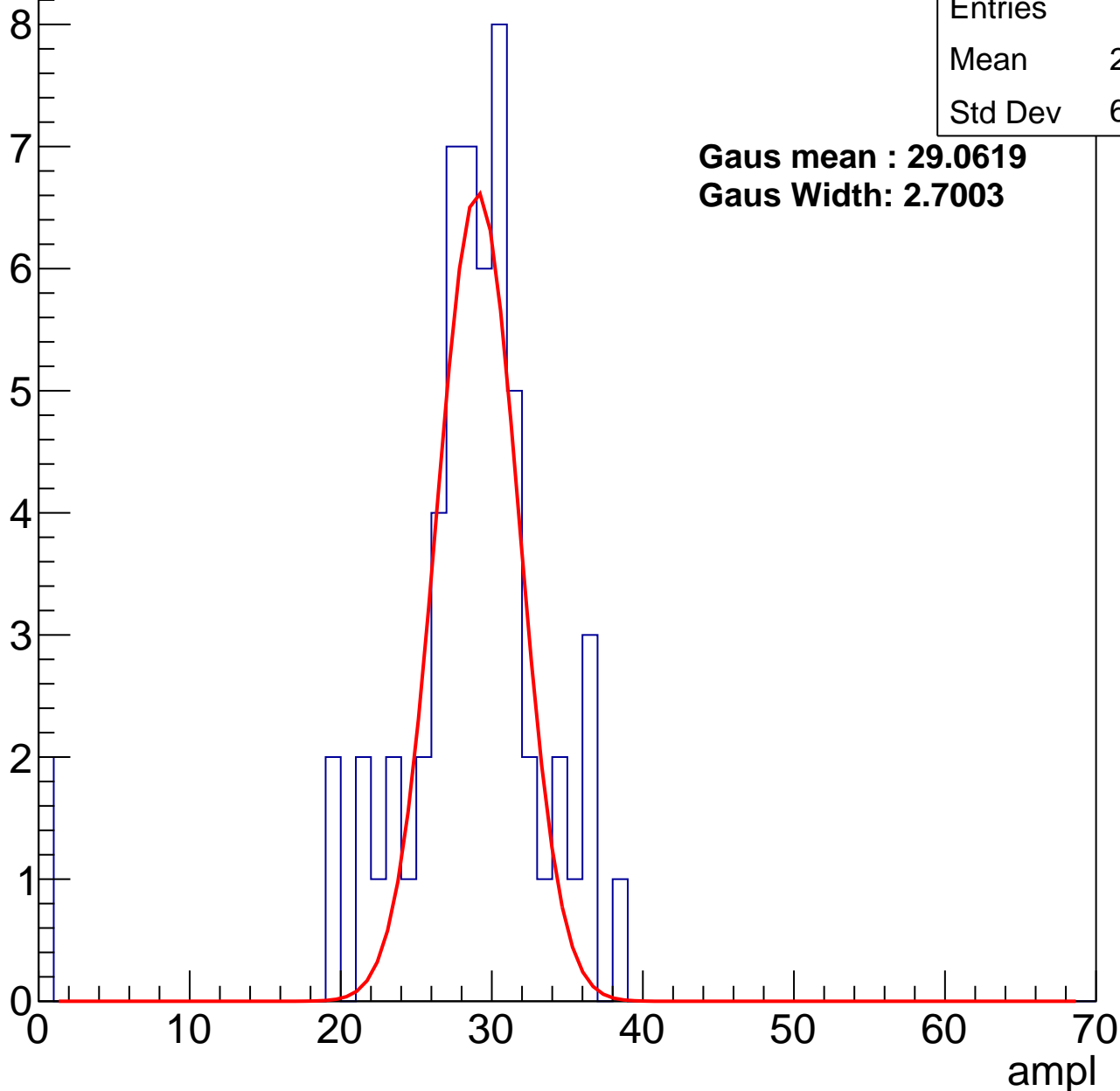
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	27.56
Std Dev	6.526

**Gaus mean : 29.0619**

**Gaus Width: 2.7003**



# B1L102S, U16-ch93, adc1

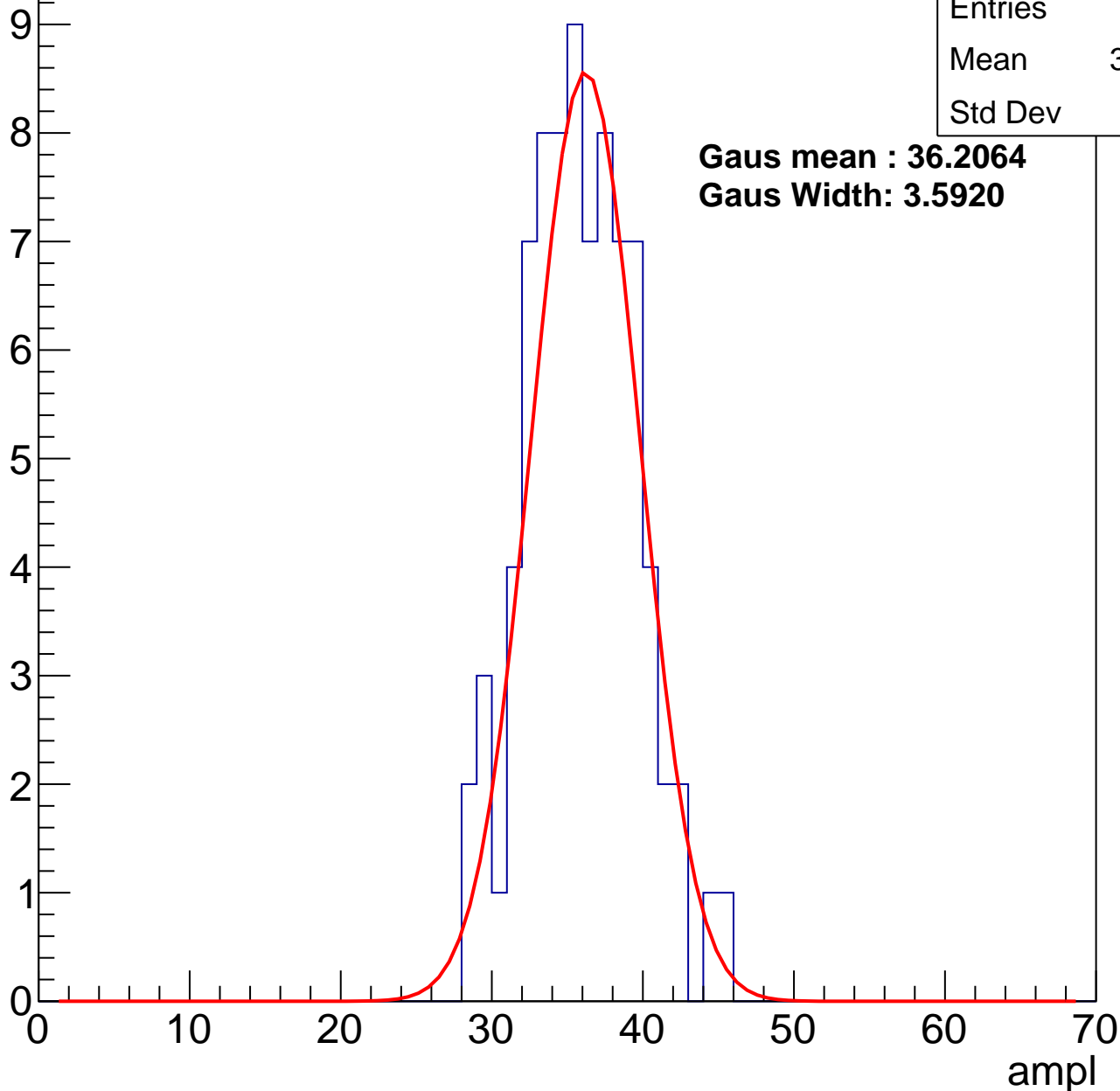
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	81
Mean	35.48
Std Dev	3.59

**Gaus mean : 36.2064**

**Gaus Width: 3.5920**



# B1L102S, U16-ch93, adc2

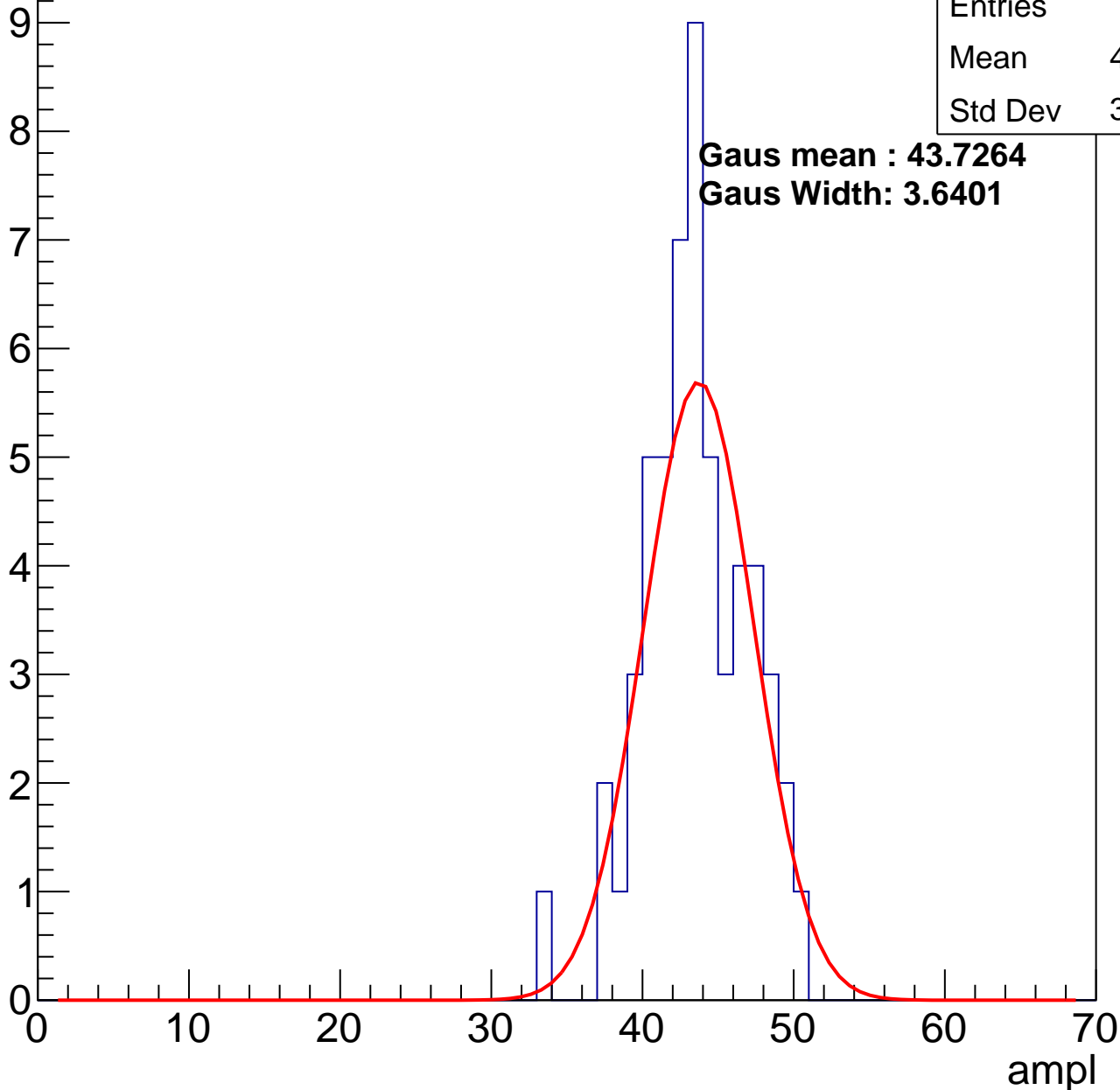
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	43.04
Std Dev	3.384

**Gaus mean : 43.7264**

**Gaus Width: 3.6401**

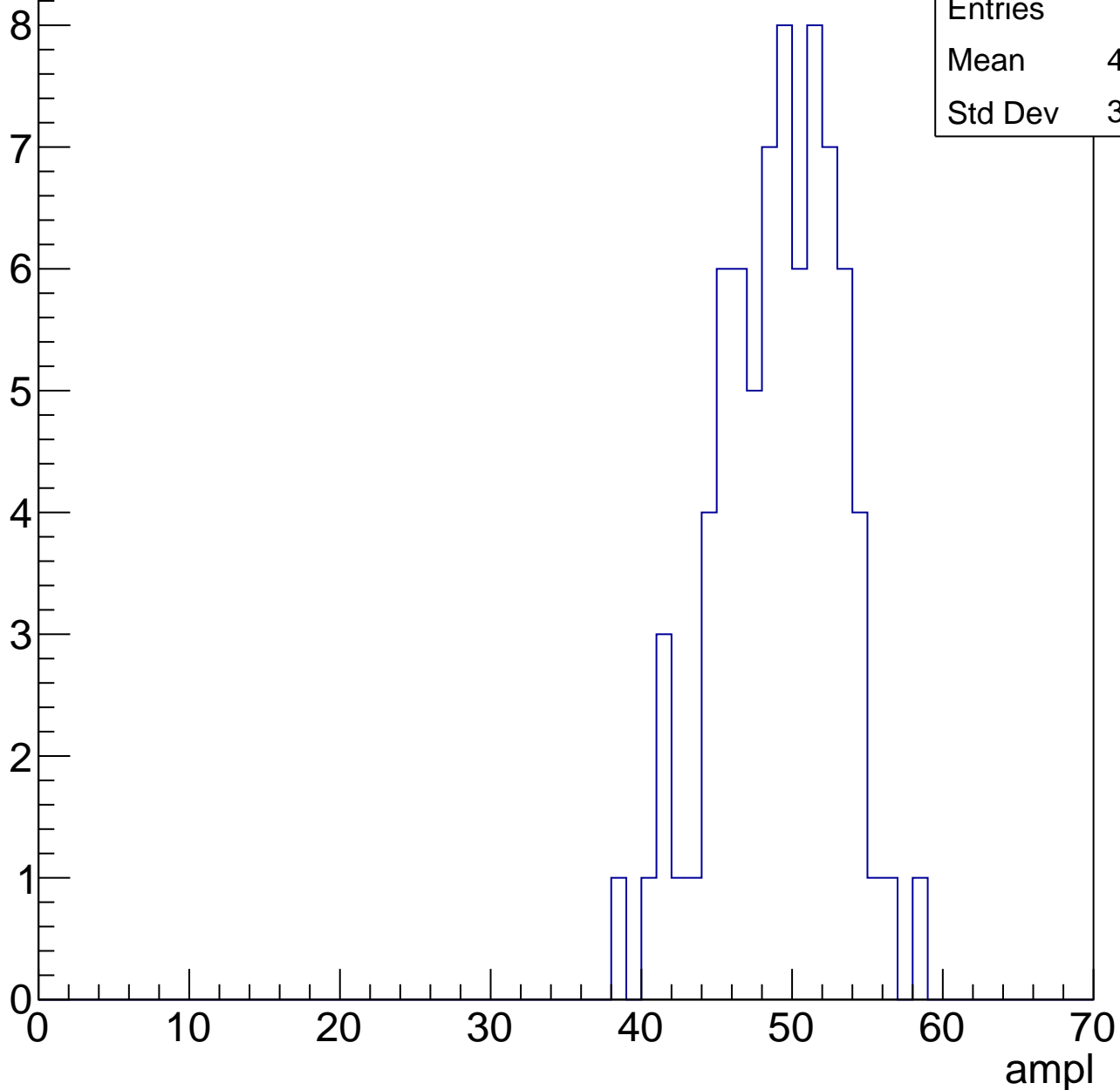


# B1L102S, U16-ch93, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	48.65
Std Dev	3.963

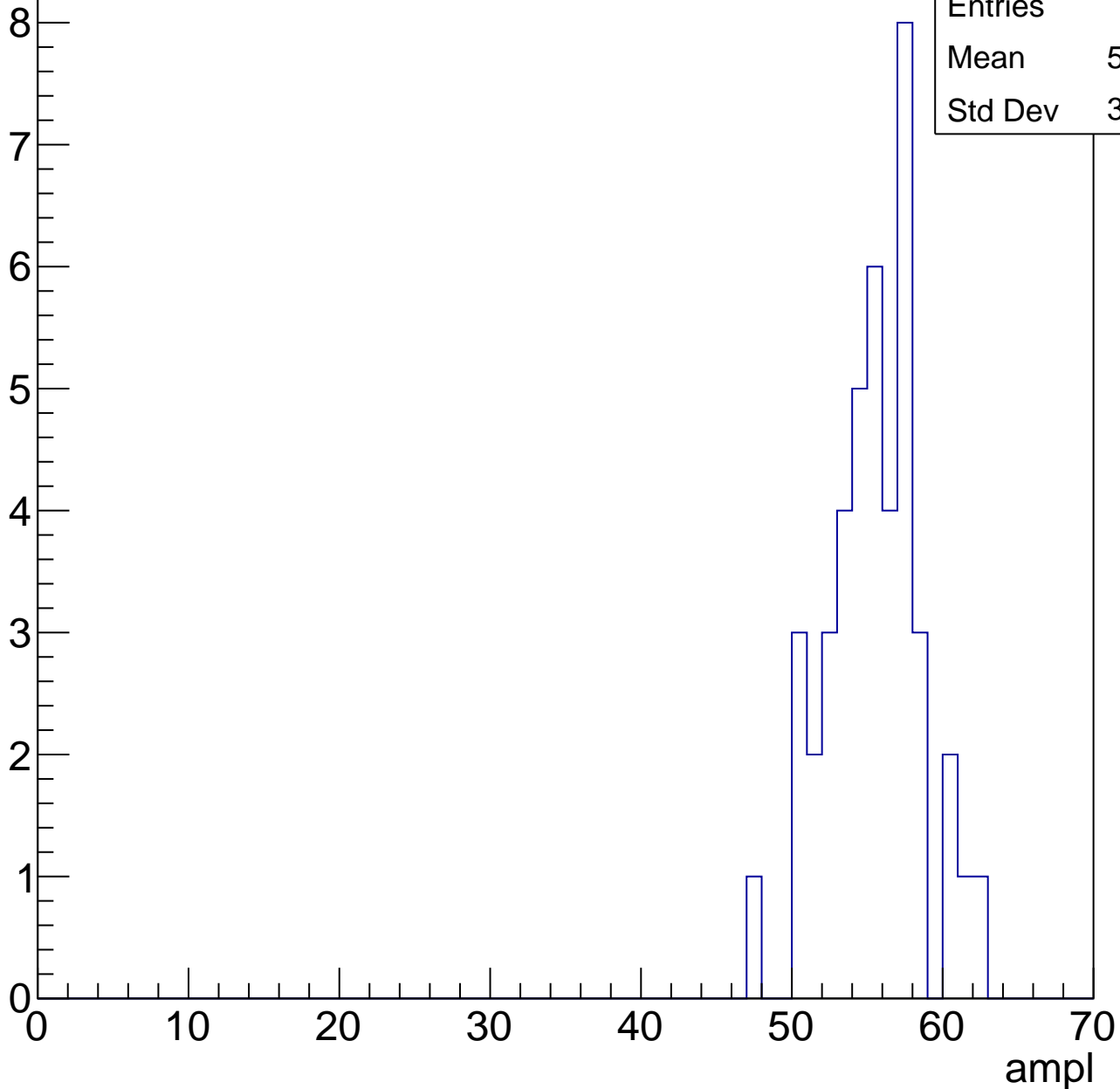


# B1L102S, U16-ch93, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

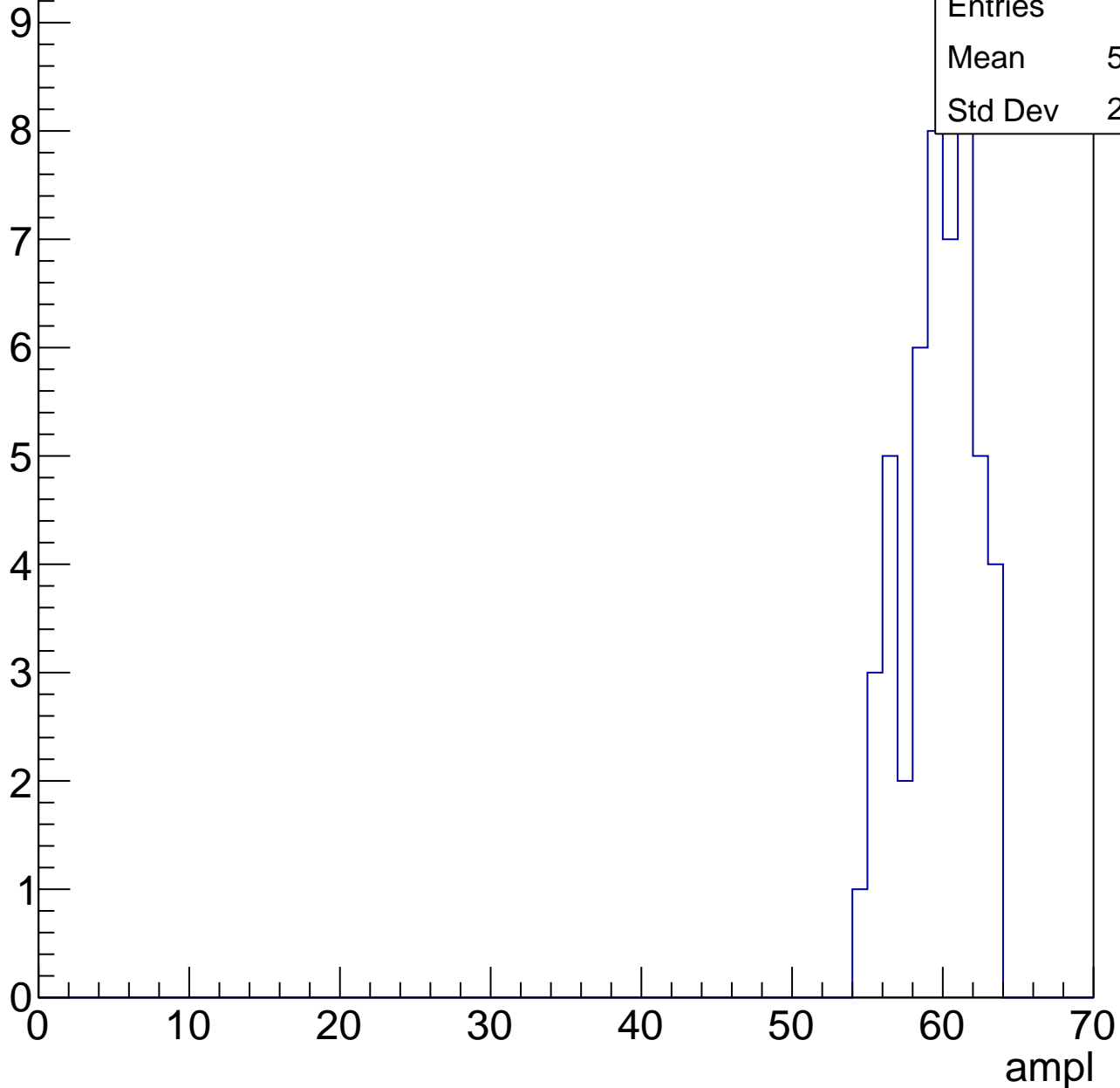
Entries	43
Mean	54.98
Std Dev	3.114



# B1L102S, U16-ch93, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

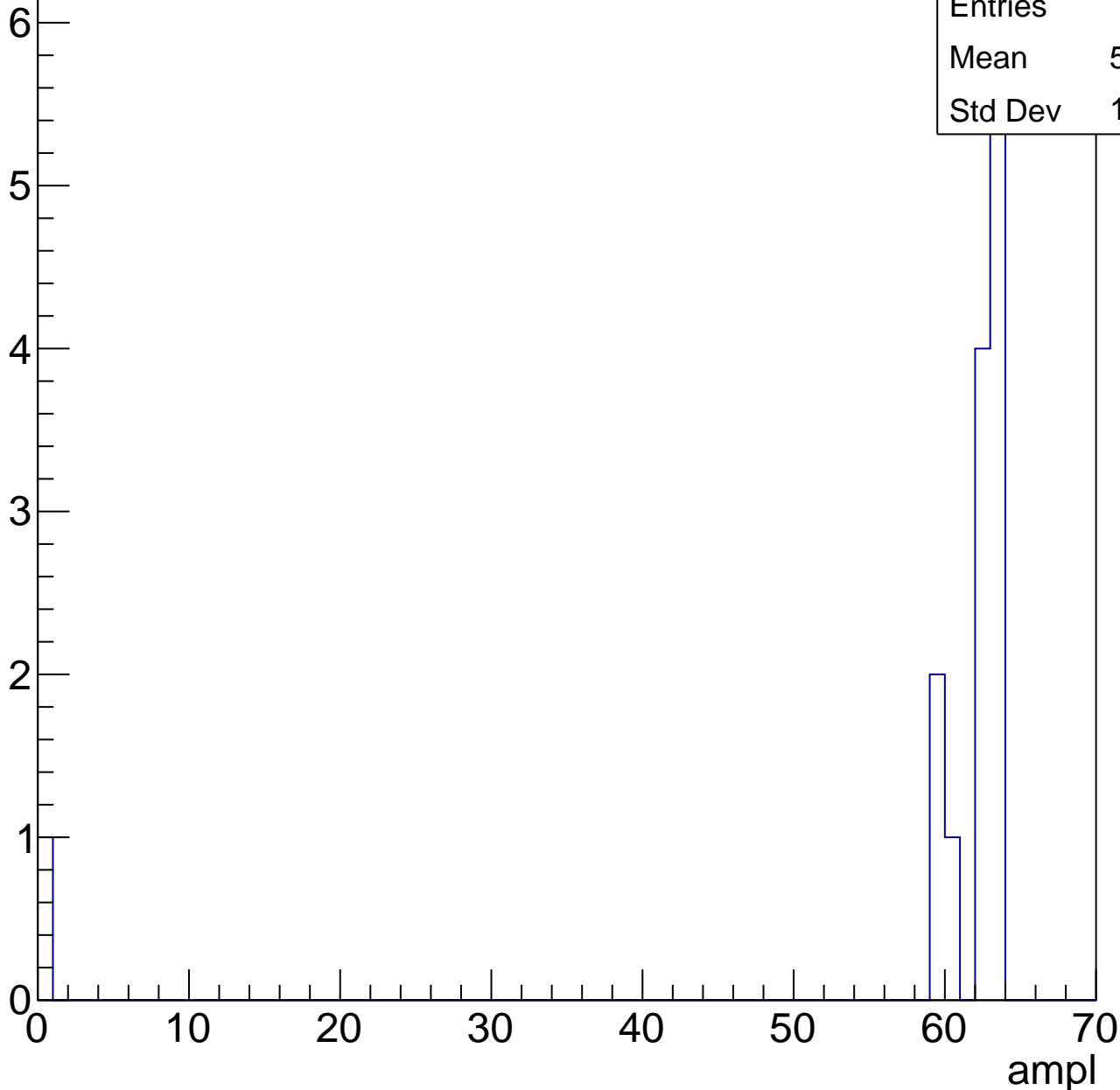


# B1L102S, U16-ch93, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	14
Mean	57.43
Std Dev	15.99





# B1L102S, U16-ch93, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U16-ch94, adc0

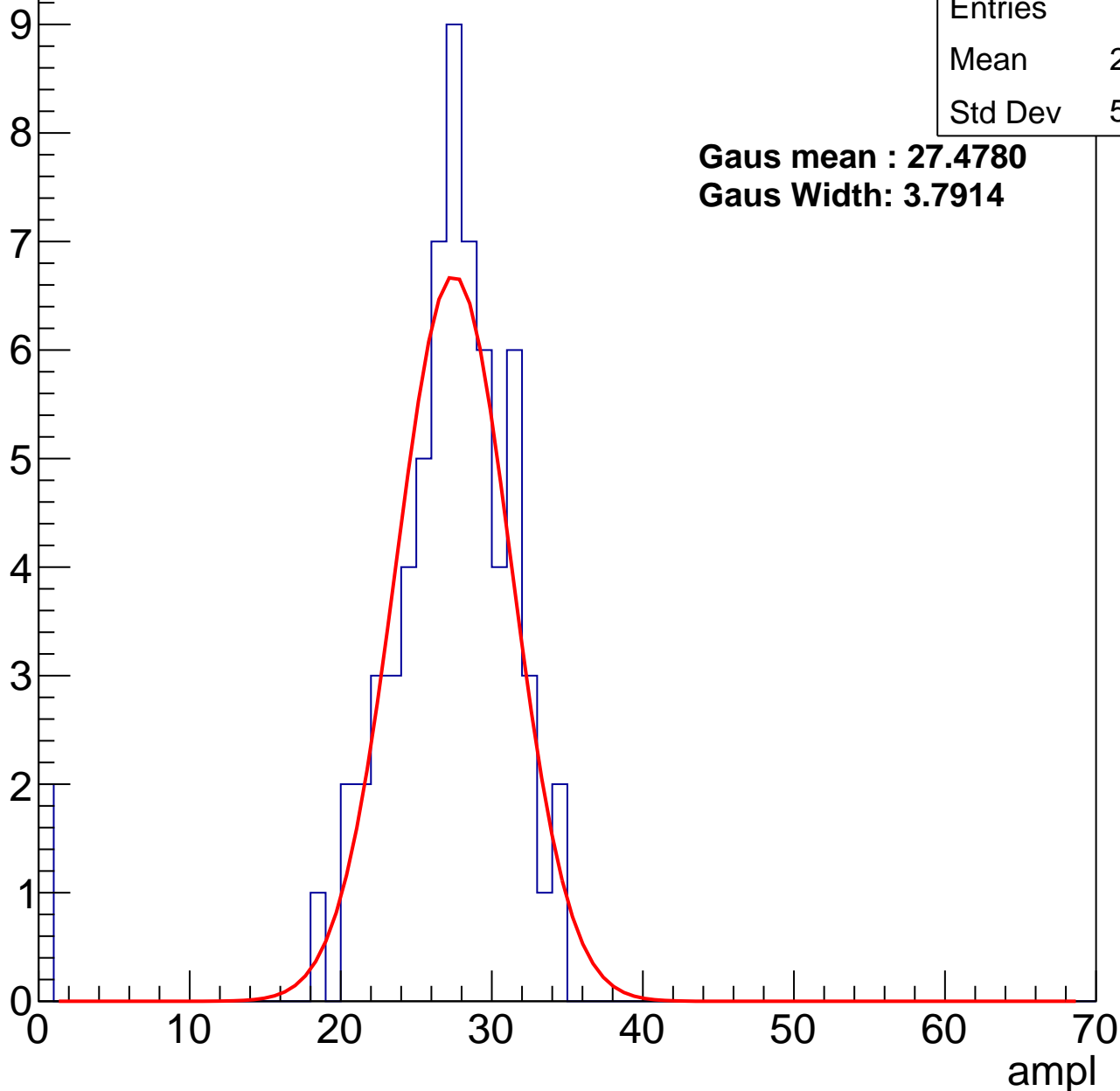
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	26.18
Std Dev	5.759

**Gaus mean : 27.4780**

**Gaus Width: 3.7914**



# B1L102S, U16-ch94, adc1

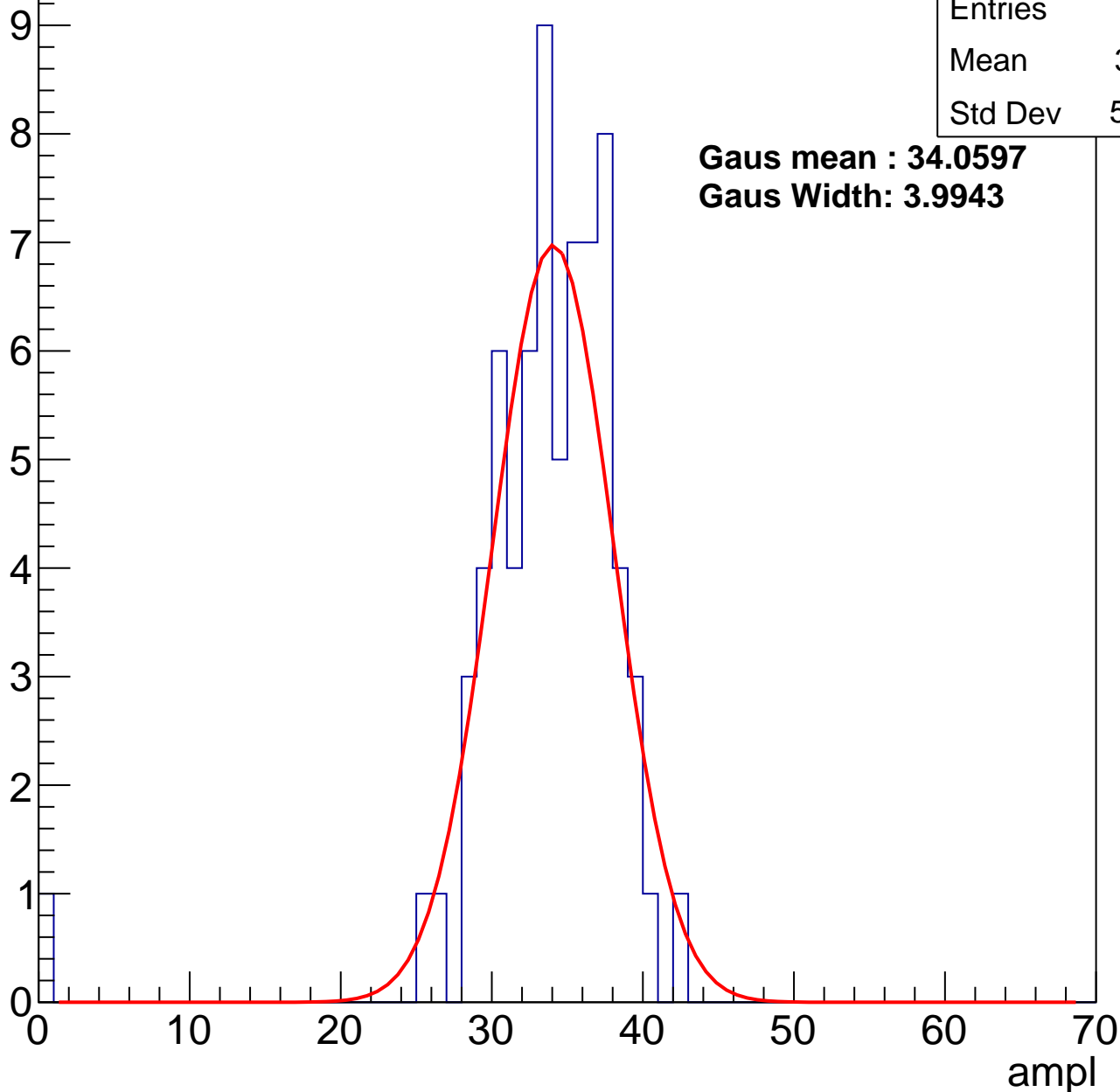
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	33.21
Std Dev	5.275

**Gaus mean : 34.0597**

**Gaus Width: 3.9943**



# B1L102S, U16-ch94, adc2

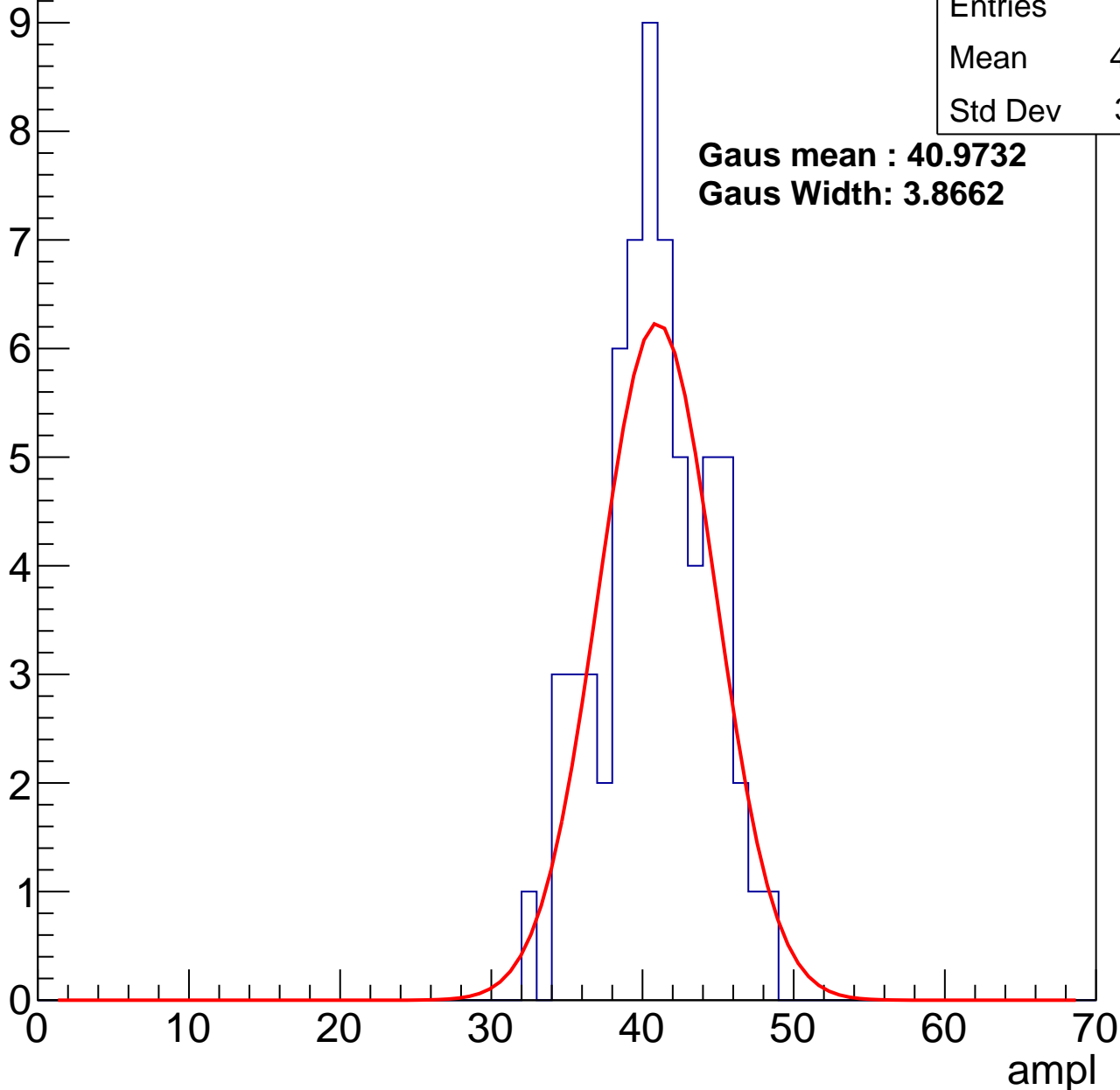
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	40.36
Std Dev	3.511

**Gaus mean : 40.9732**

**Gaus Width: 3.8662**

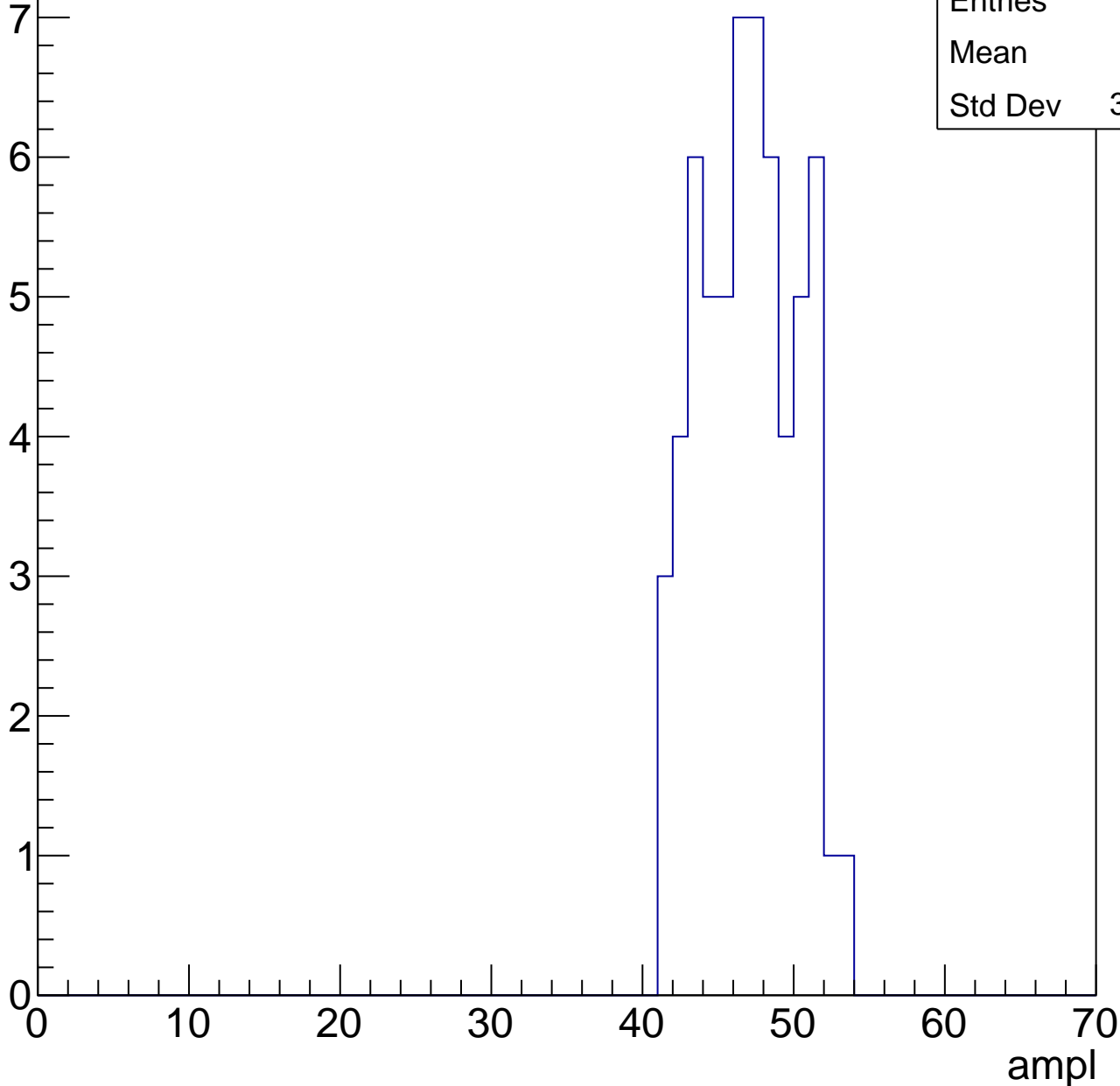


# B1L102S, U16-ch94, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	46.5
Std Dev	3.122

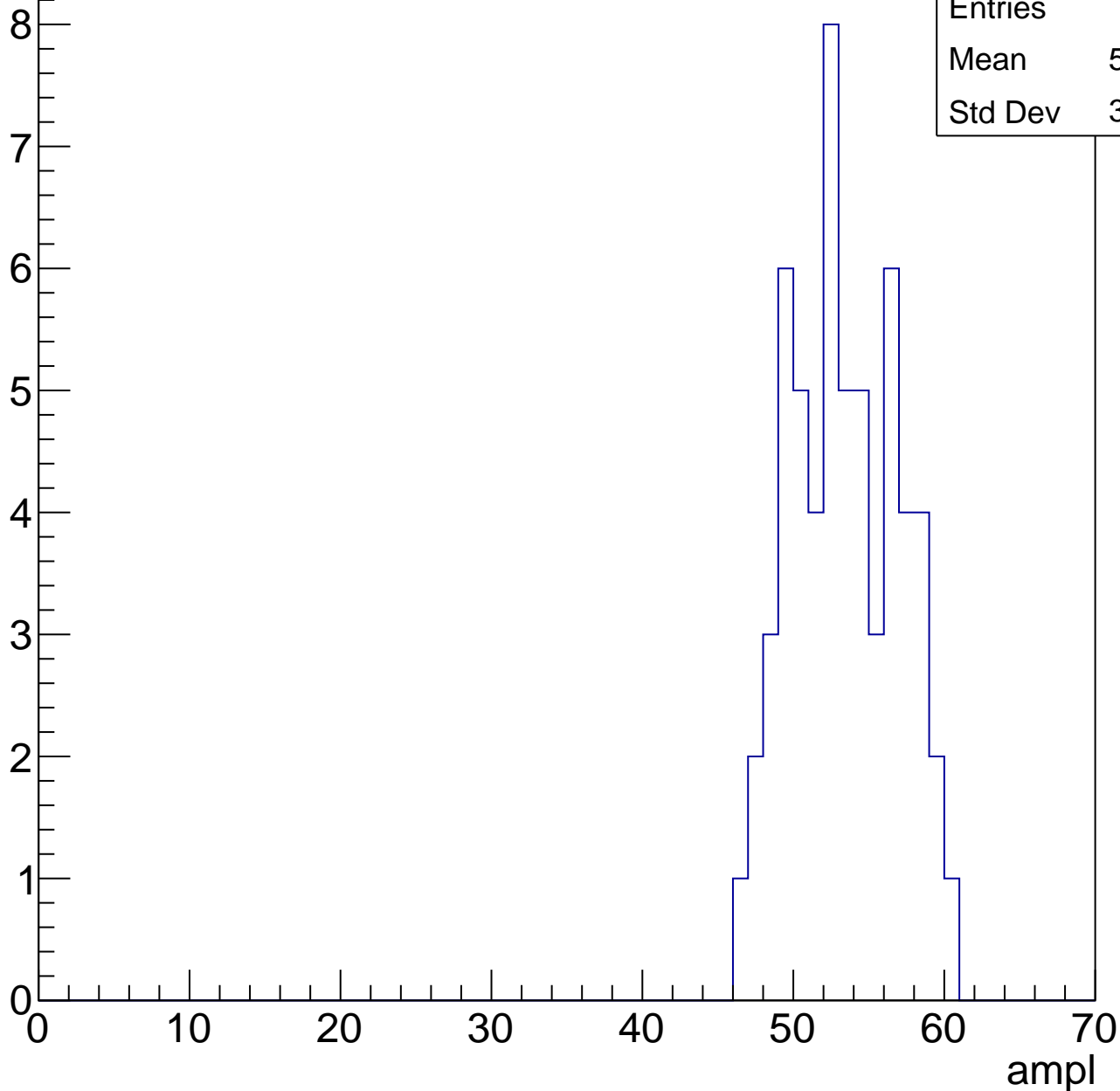


# B1L102S, U16-ch94, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	52.92
Std Dev	3.485

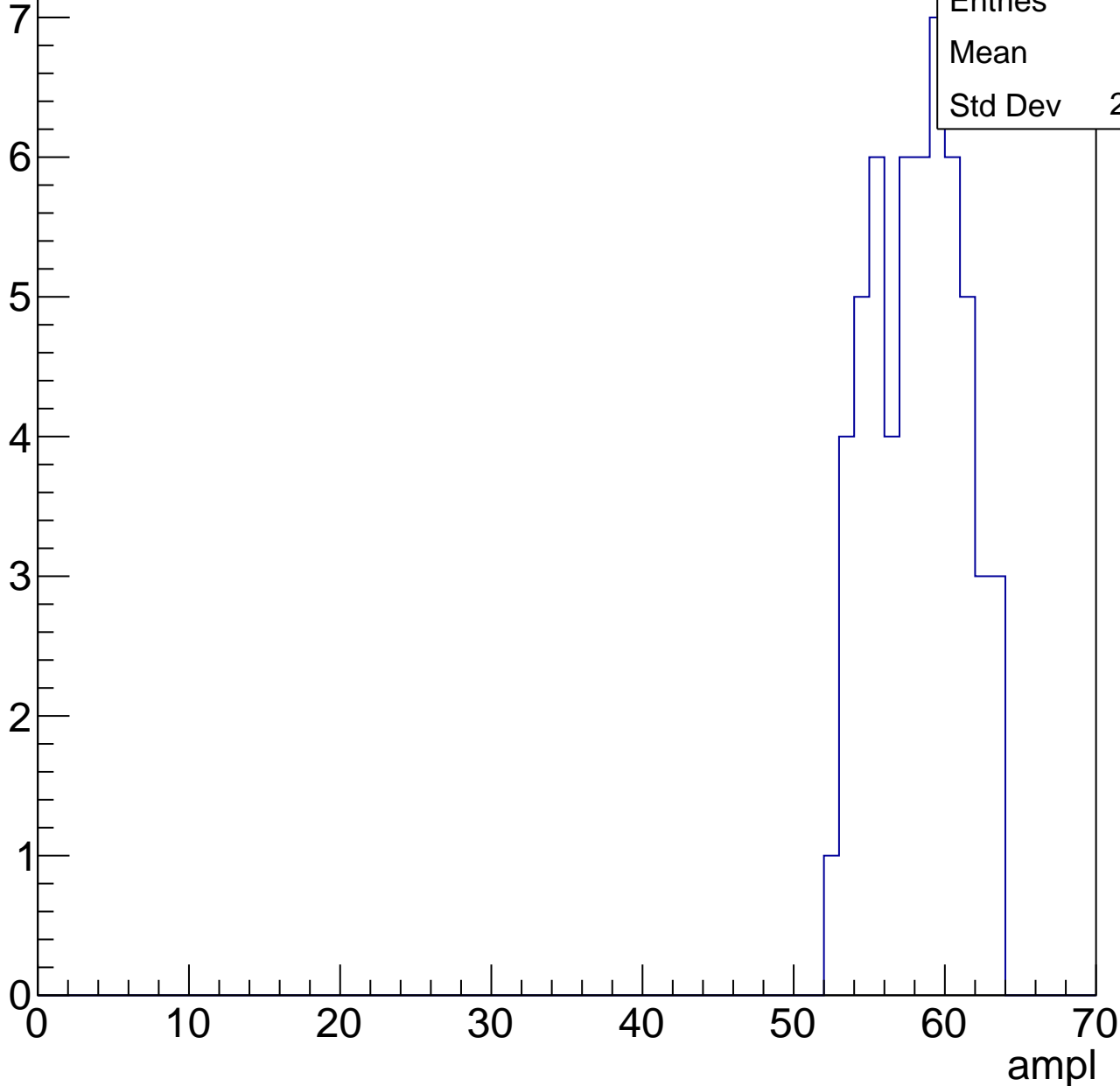


# B1L102S, U16-ch94, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	57.7
Std Dev	2.945

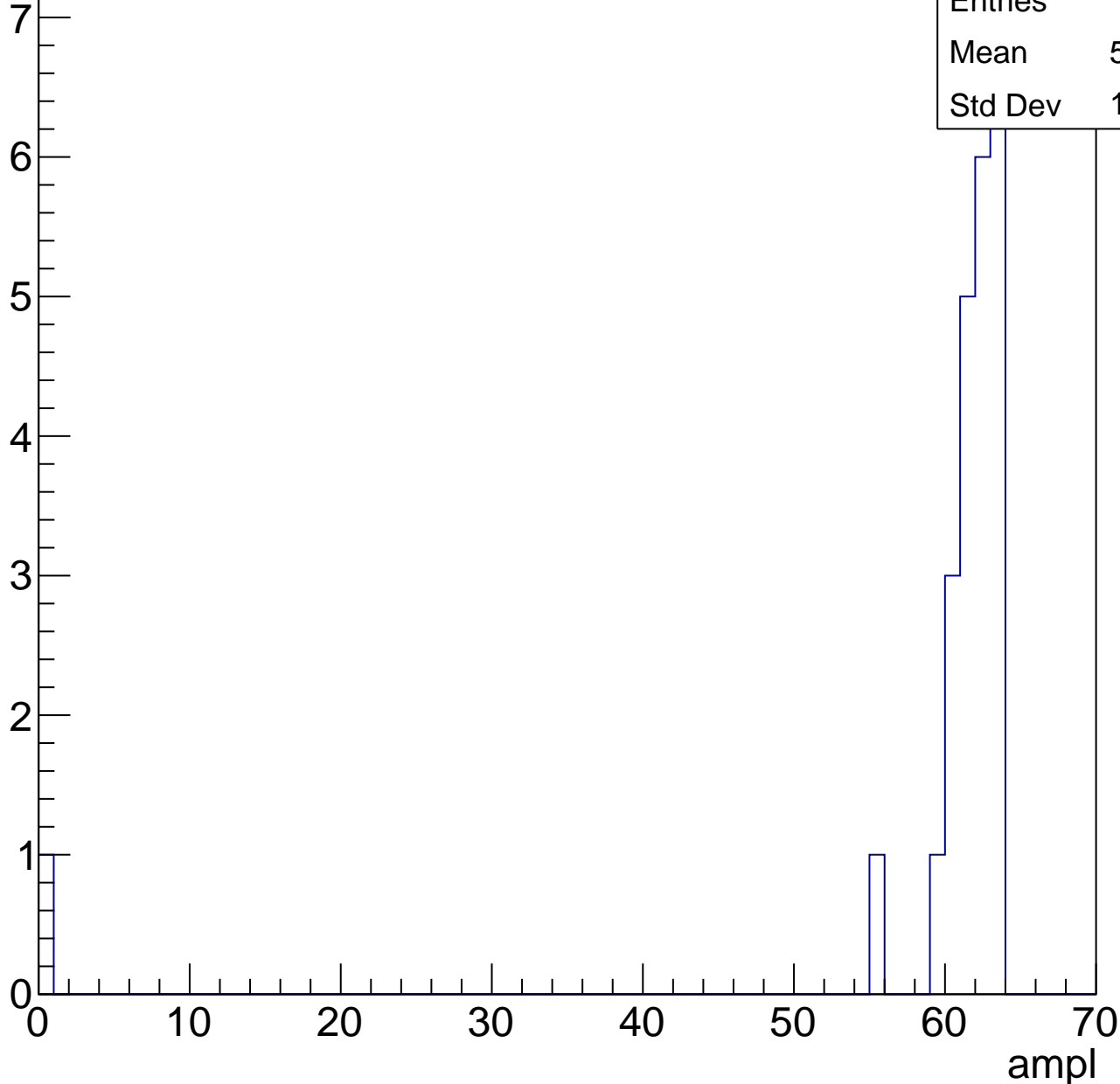


# B1L102S, U16-ch94, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	24
Mean	58.83
Std Dev	12.39





# B1L102S, U16-ch94, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch95, adc0

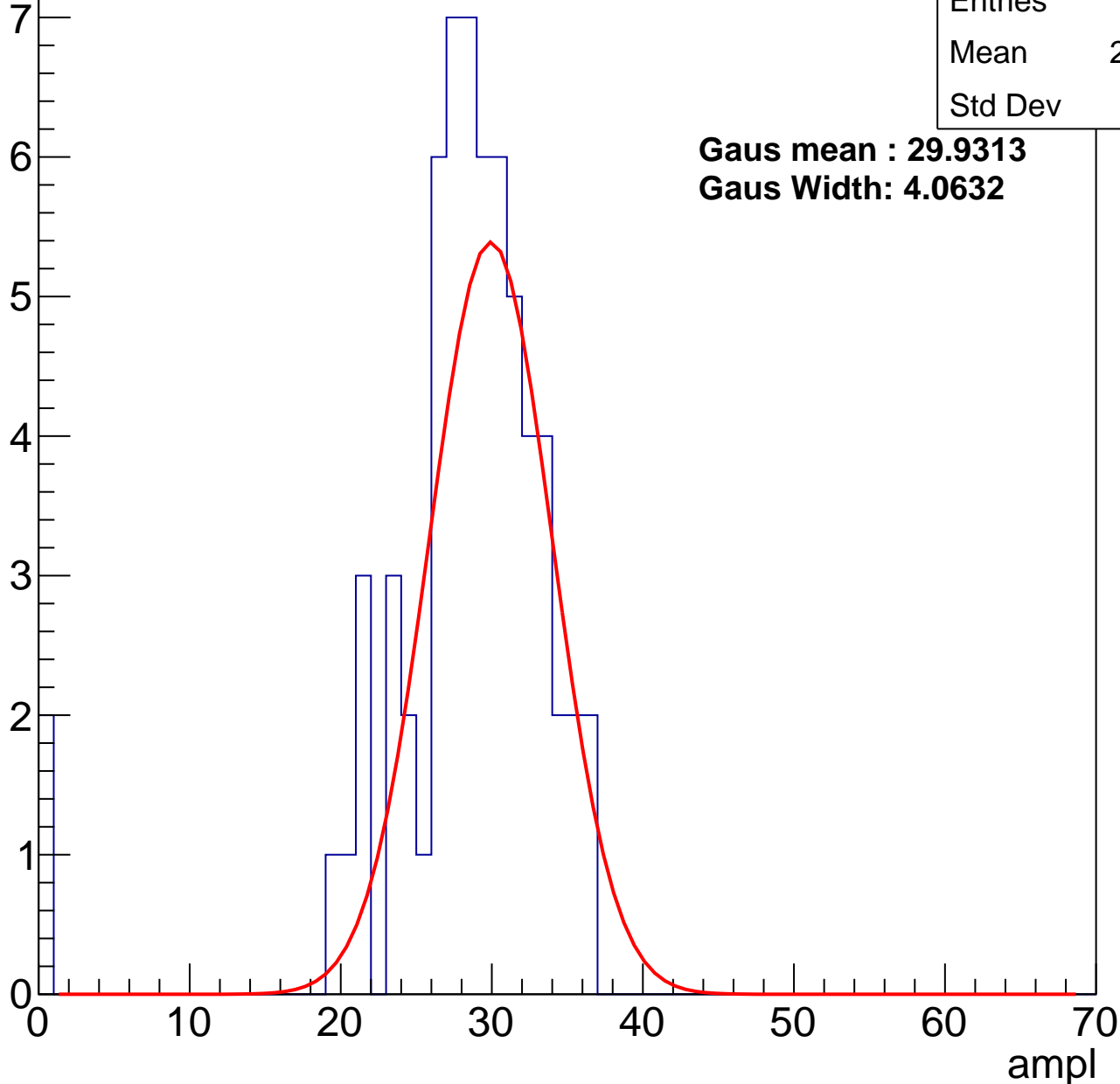
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	27.56
Std Dev	6.29

**Gaus mean : 29.9313**

**Gaus Width: 4.0632**



# B1L102S, U16-ch95, adc1

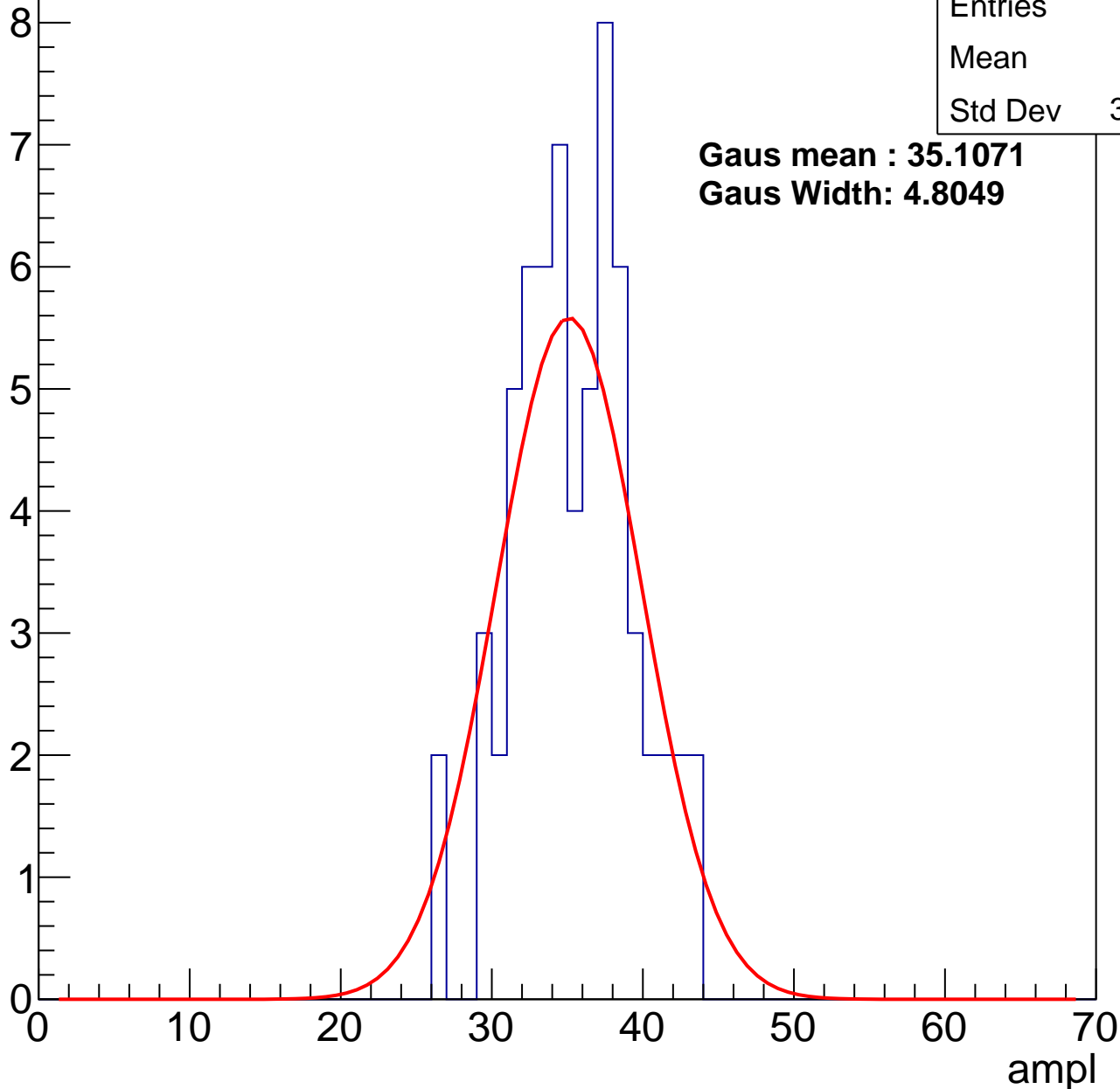
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	35
Std Dev	3.867

**Gaus mean : 35.1071**

**Gaus Width: 4.8049**



# B1L102S, U16-ch95, adc2

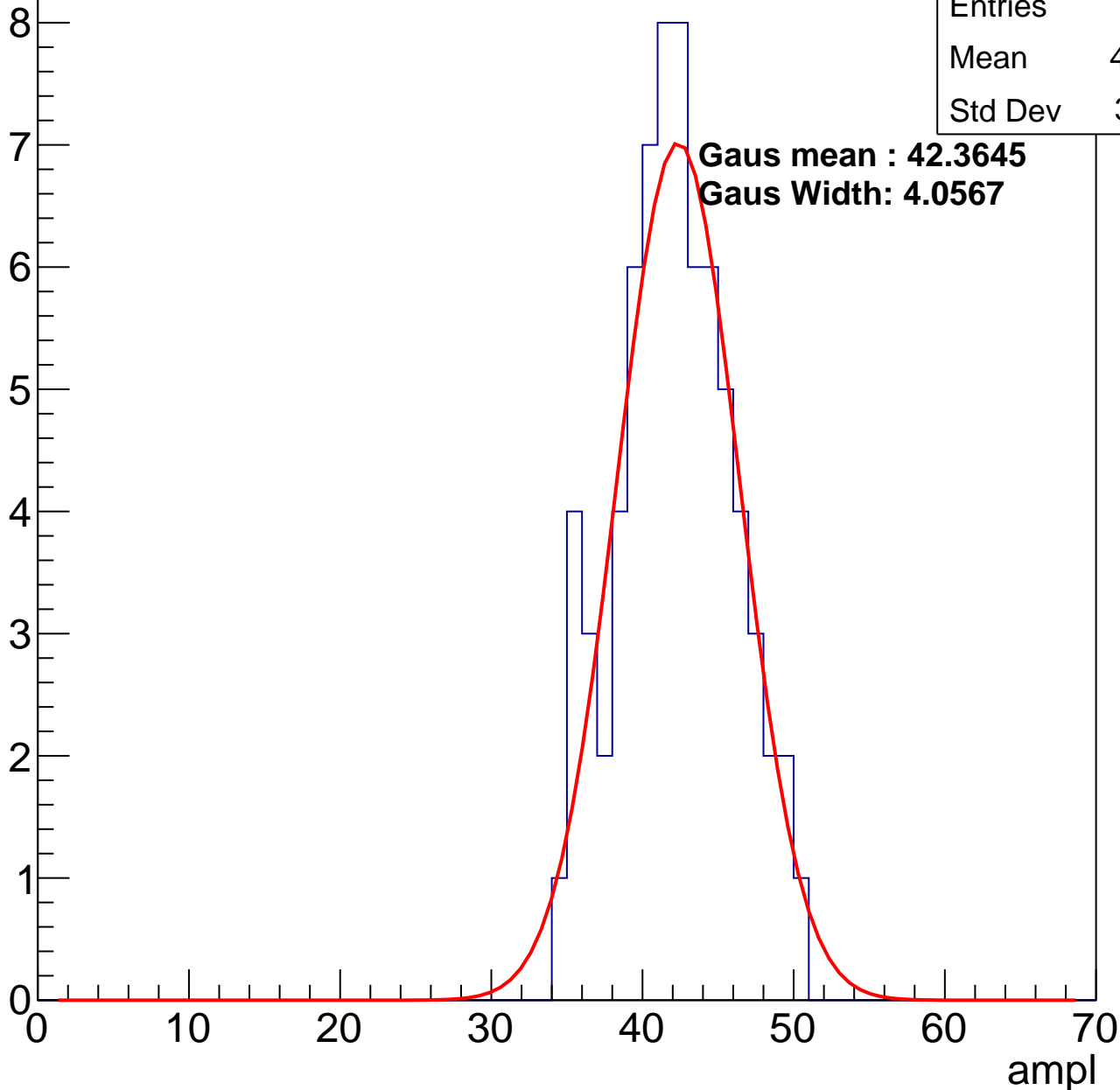
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	41.69
Std Dev	3.751

**Gaus mean : 42.3645**

**Gaus Width: 4.0567**

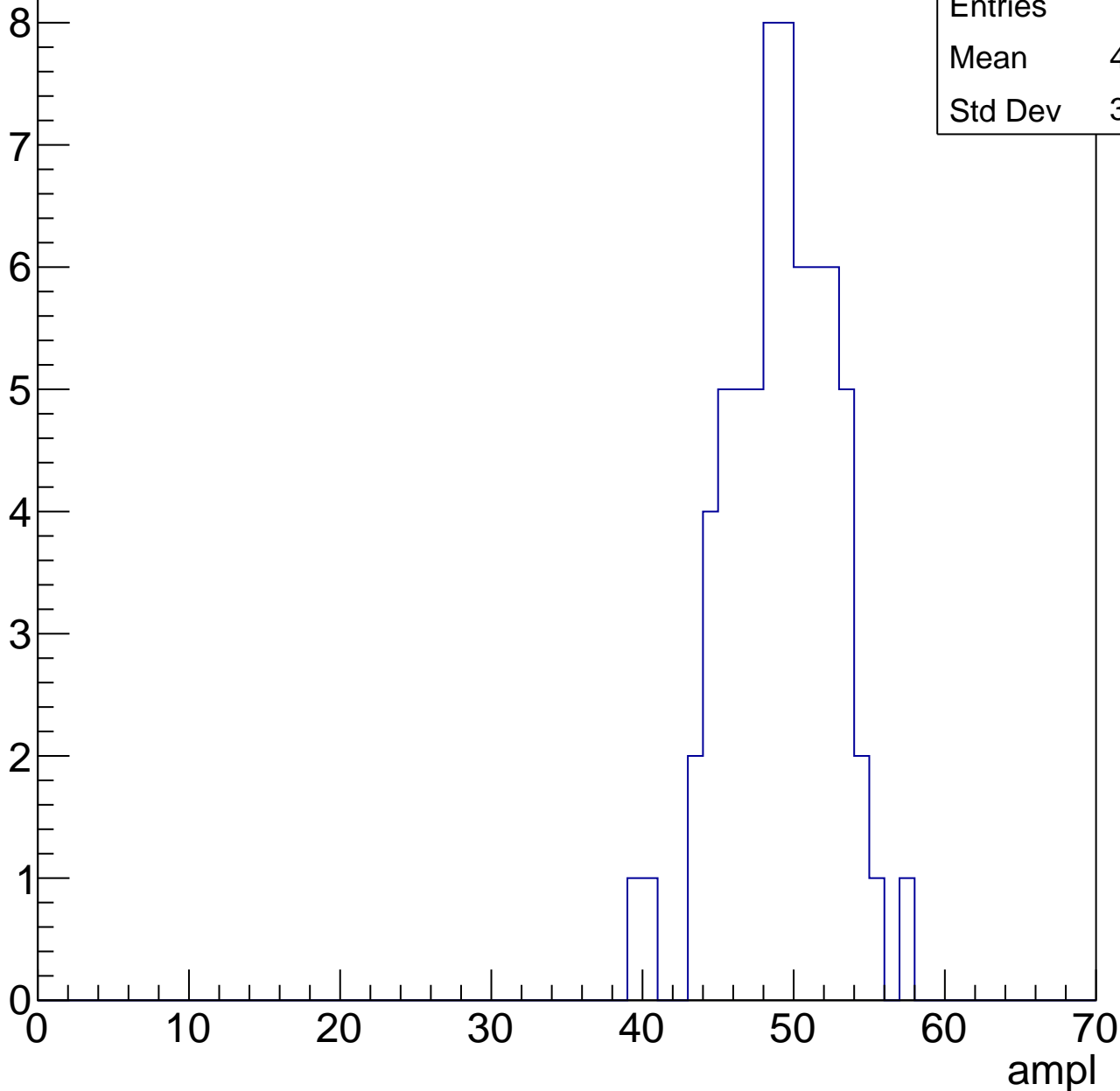


# B1L102S, U16-ch95, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	48.64
Std Dev	3.506

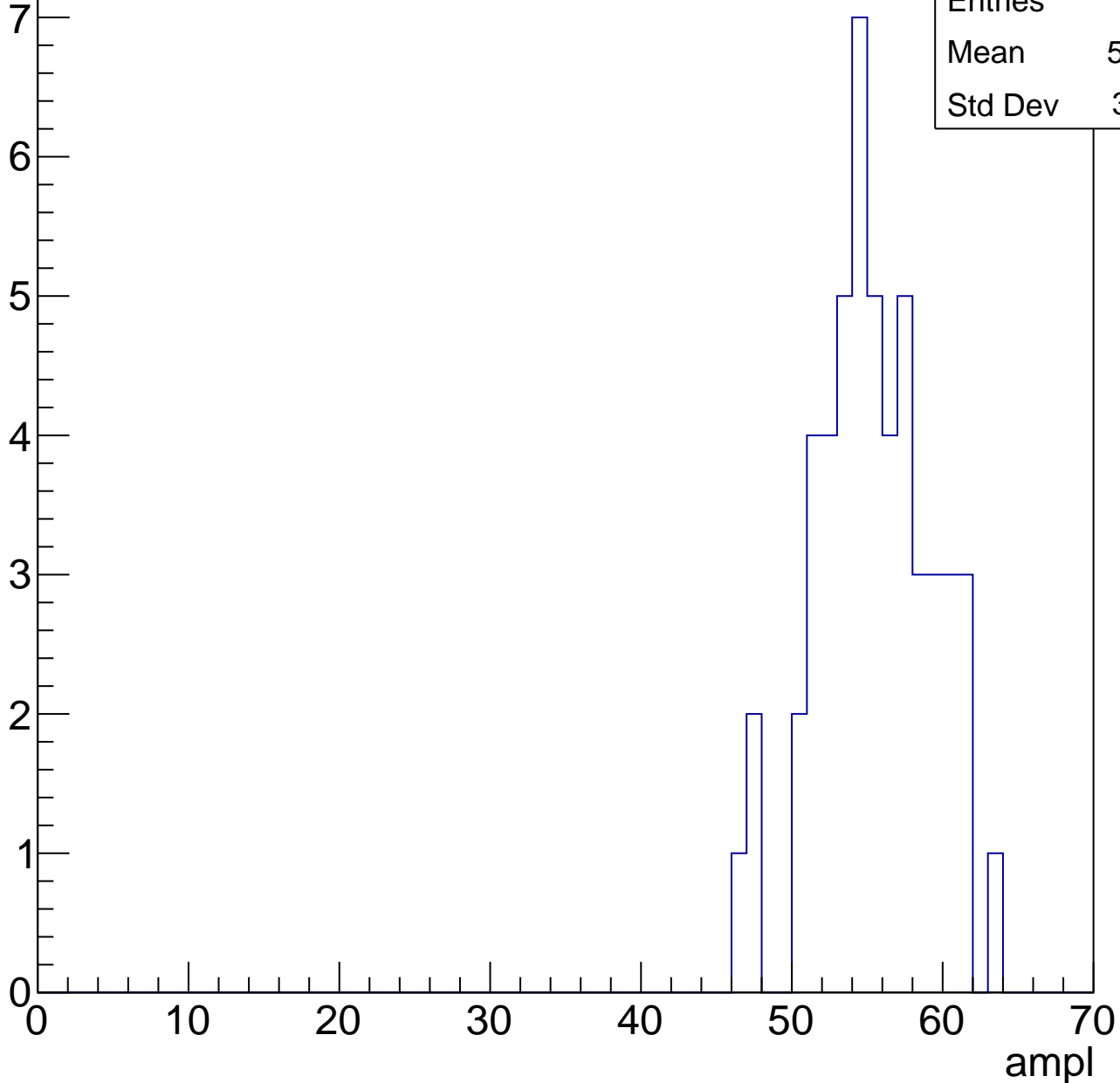


# B1L102S, U16-ch95, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	54.92
Std Dev	3.751

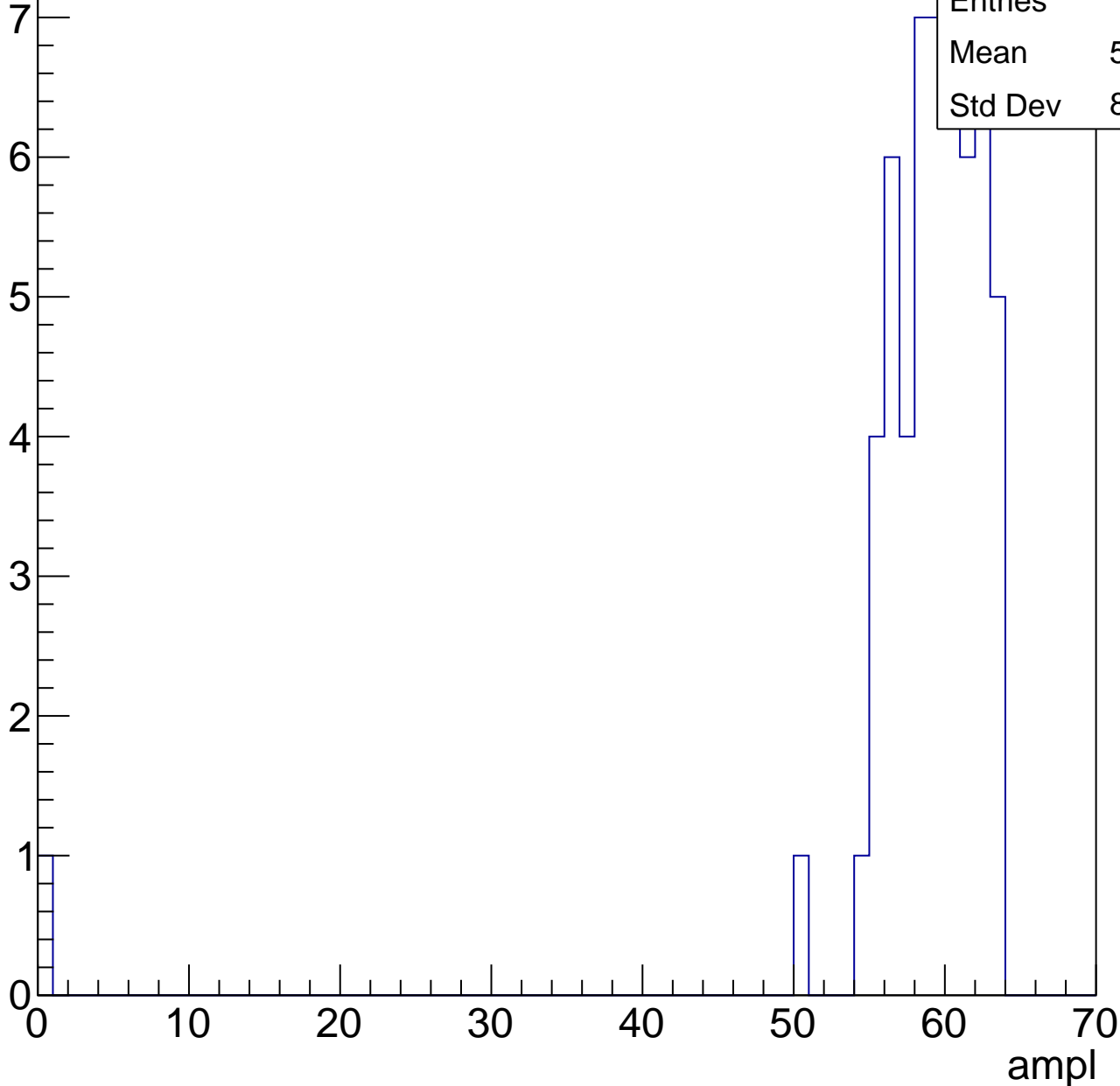


# B1L102S, U16-ch95, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

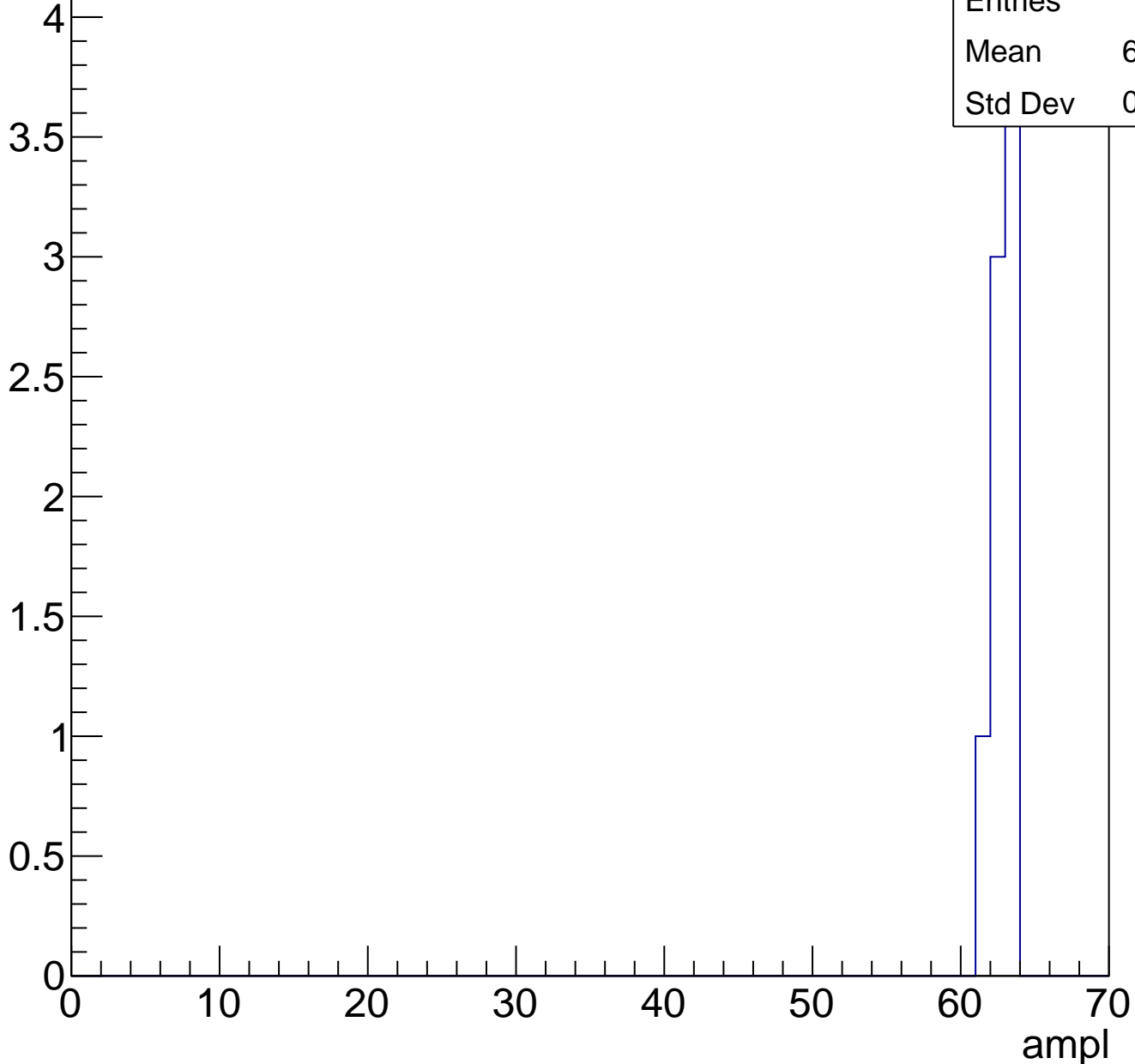
Entries	56
Mean	57.89
Std Dev	8.274



# B1L102S, U16-ch95, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch95, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U16-ch96, adc0

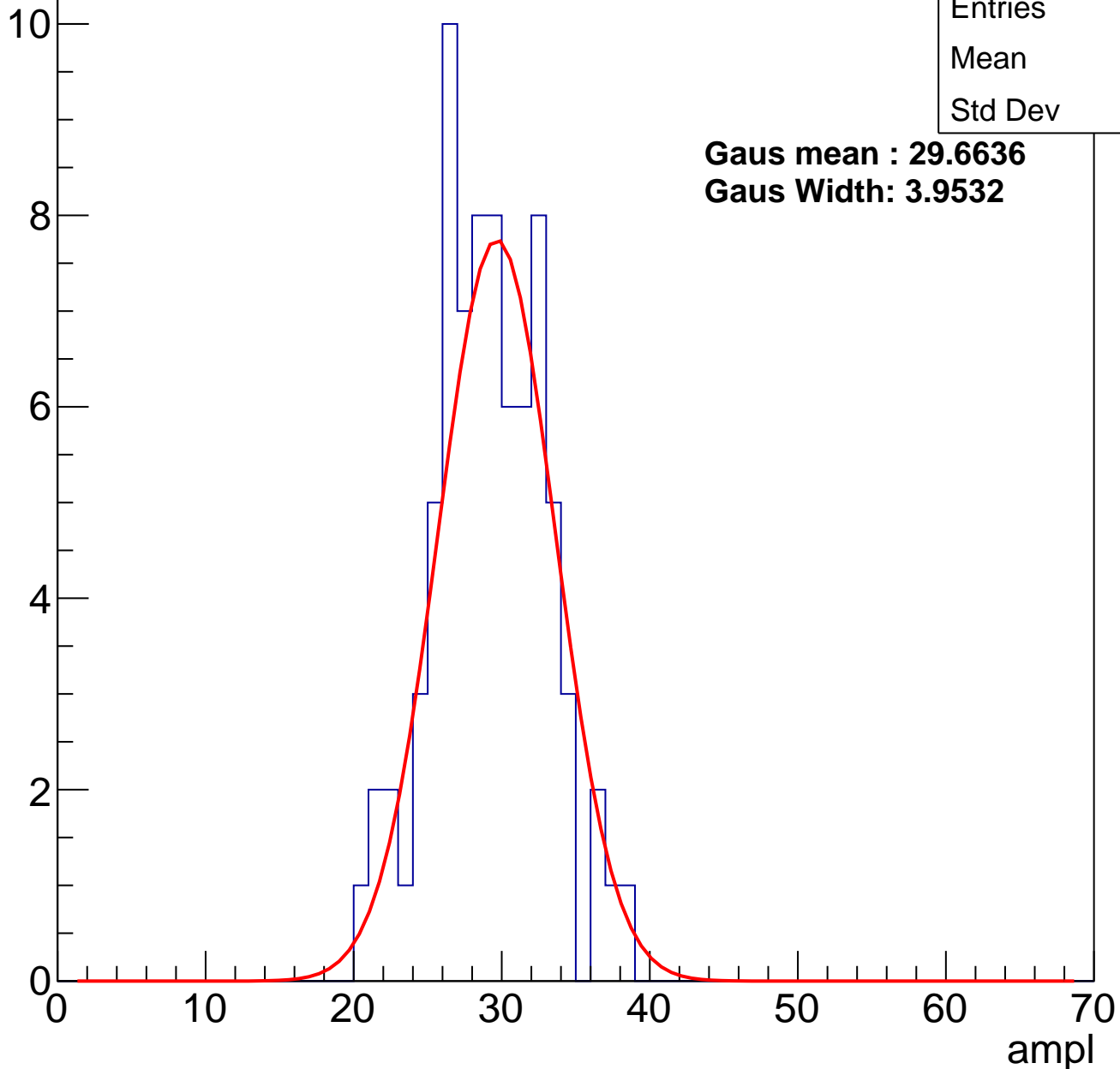
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	79
Mean	28.7
Std Dev	3.76

**Gaus mean : 29.6636**

**Gaus Width: 3.9532**

Entry



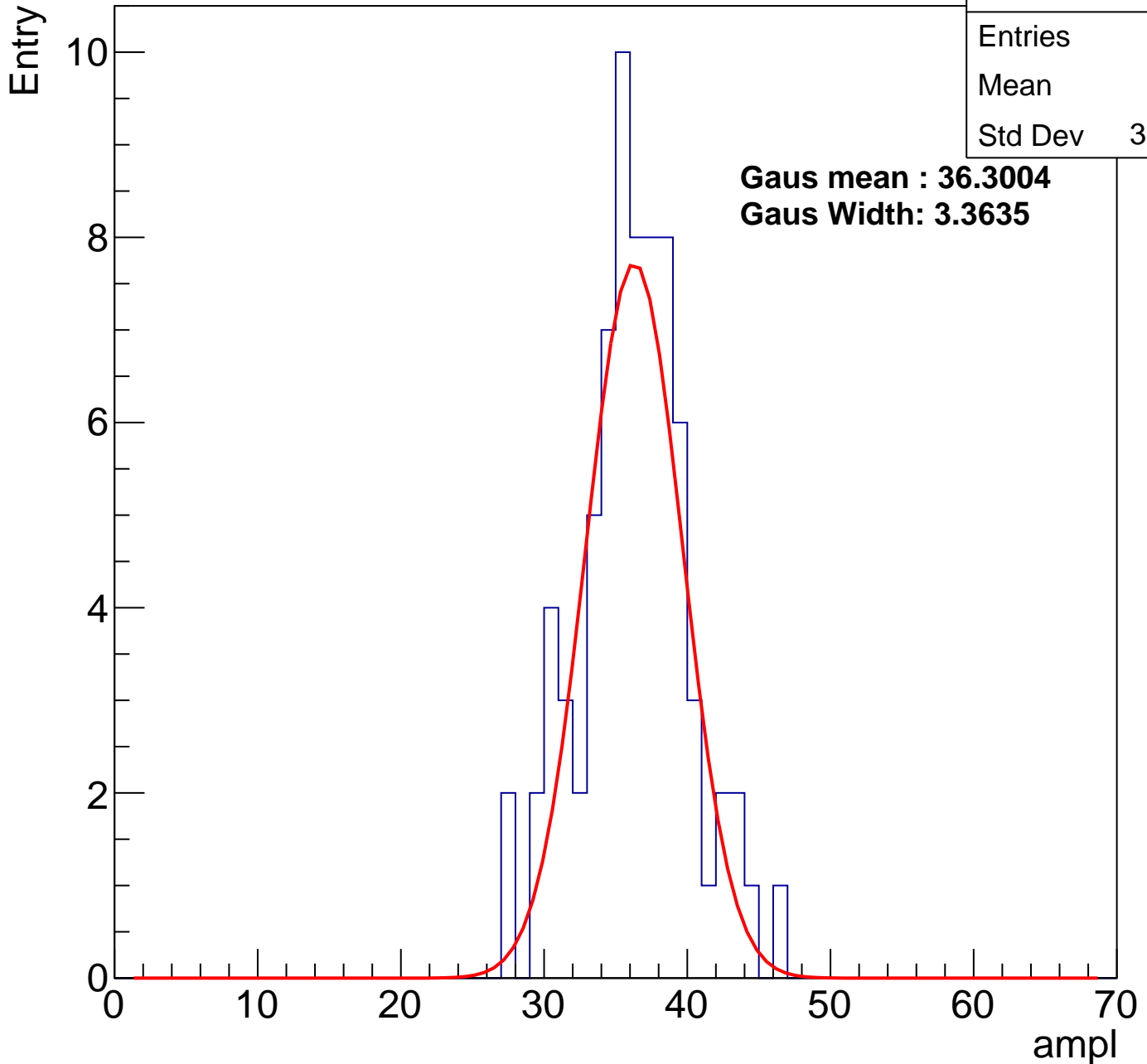
# B1L102S, U16-ch96, adc1

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	75
Mean	35.8
Std Dev	3.816

**Gaus mean : 36.3004**

**Gaus Width: 3.3635**



# B1L102S, U16-ch96, adc2

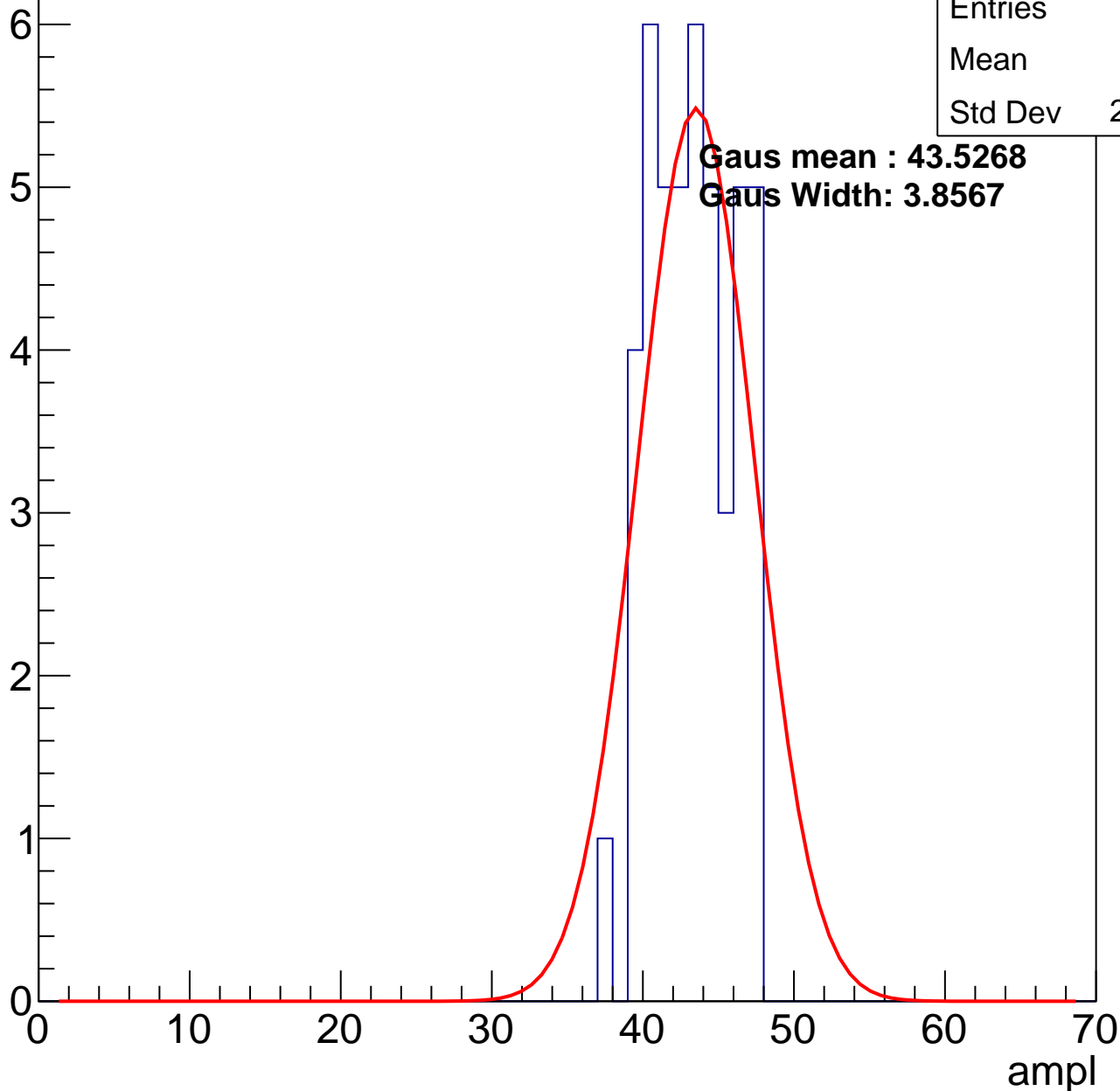
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	42.8
Std Dev	2.663

**Gaus mean : 43.5268**

**Gaus Width: 3.8567**

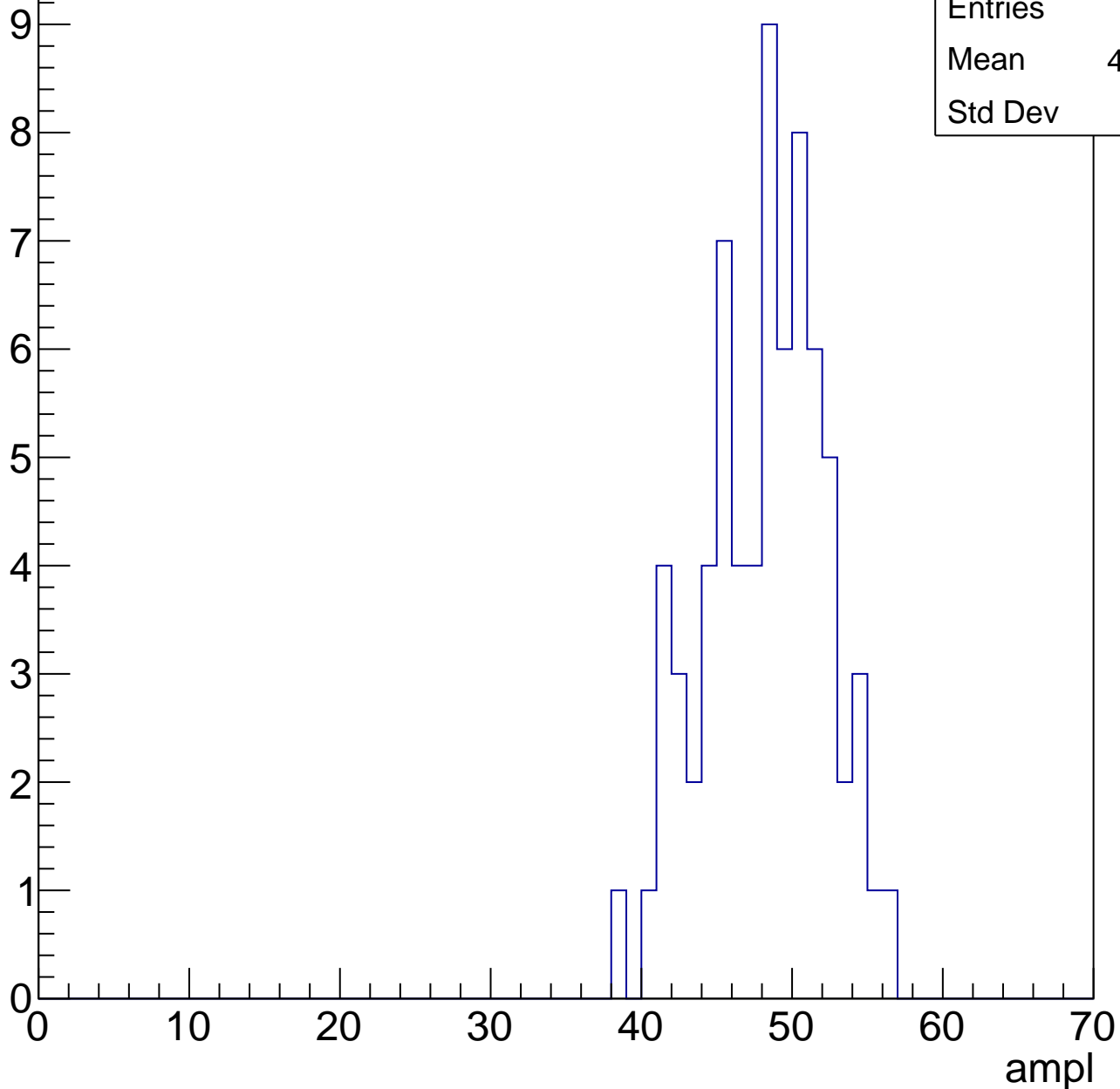


# B1L102S, U16-ch96, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	47.72
Std Dev	3.94

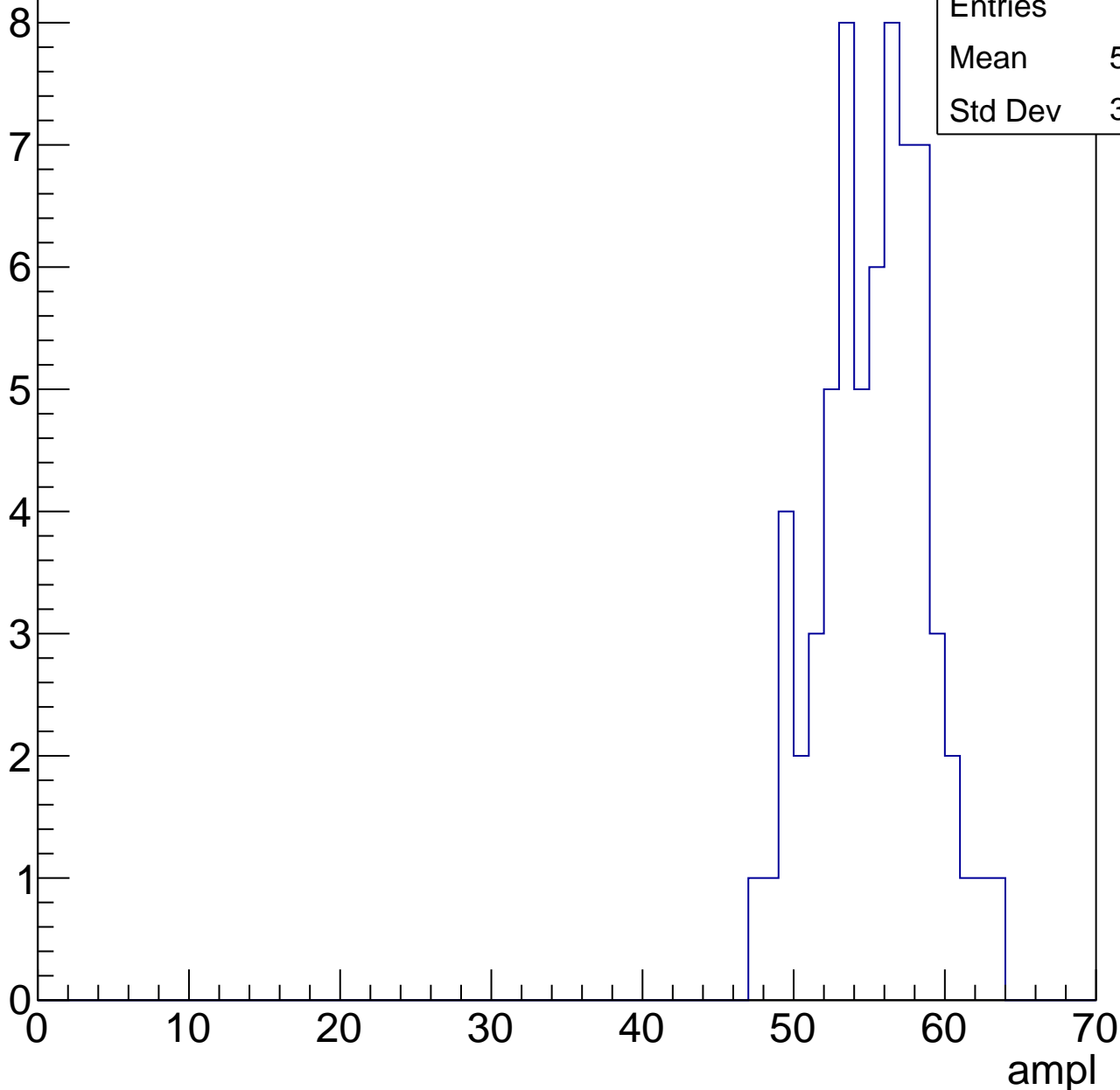


# B1L102S, U16-ch96, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	54.83
Std Dev	3.467

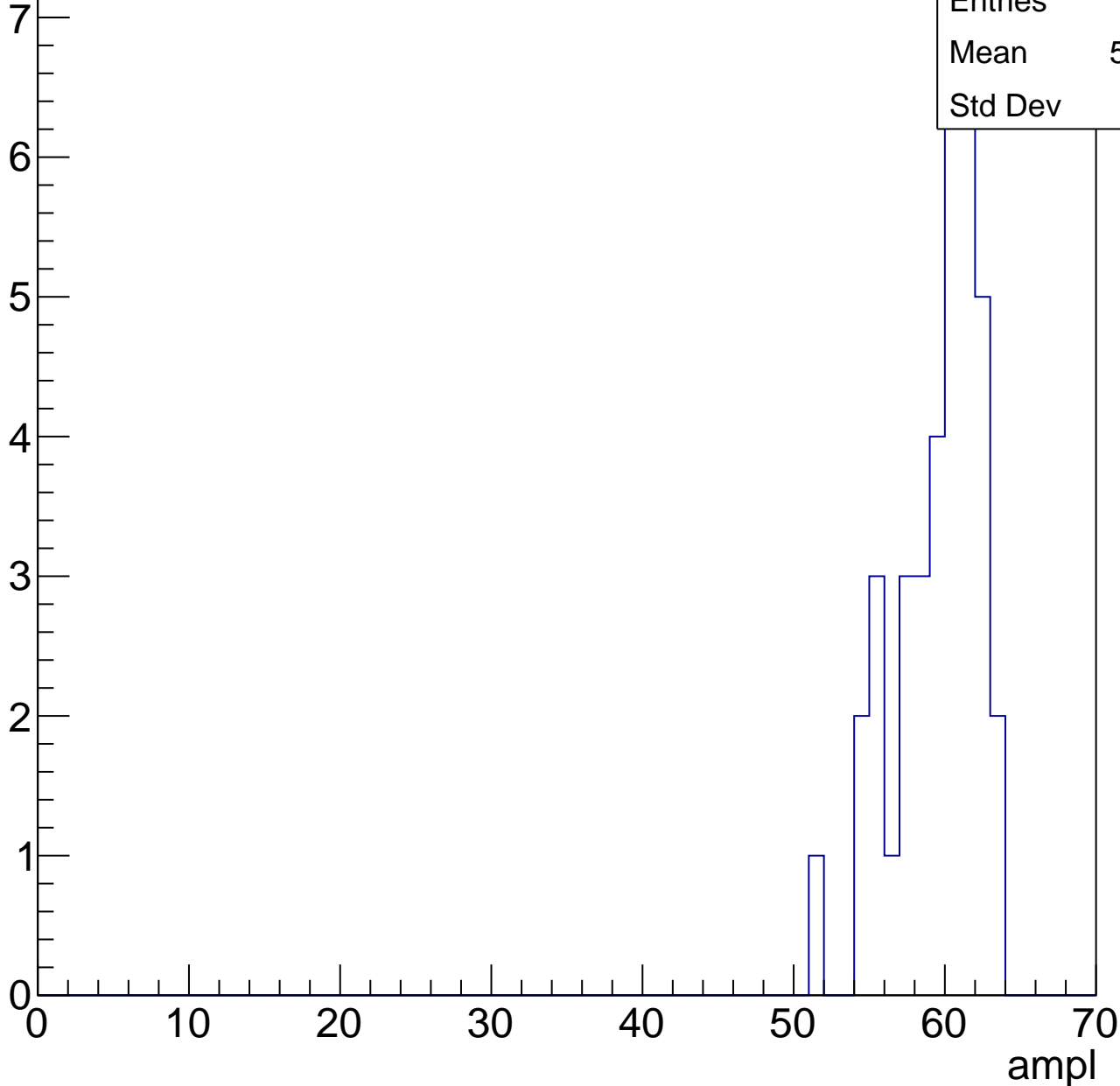


# B1L102S, U16-ch96, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	38
Mean	59.05
Std Dev	2.8

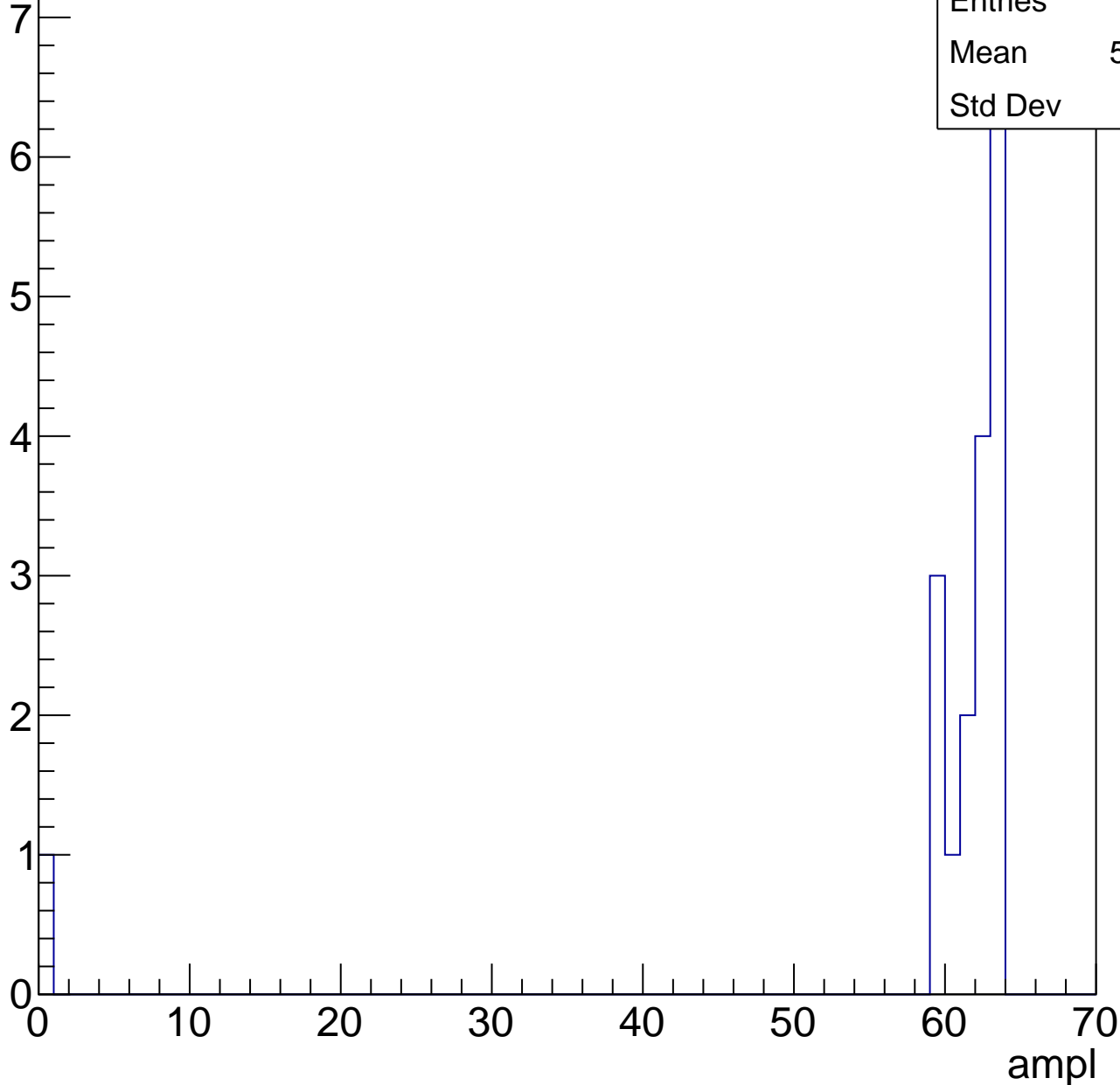


# B1L102S, U16-ch96, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	18
Mean	58.22
Std Dev	14.2





# B1L102S, U16-ch96, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U16-ch97, adc0

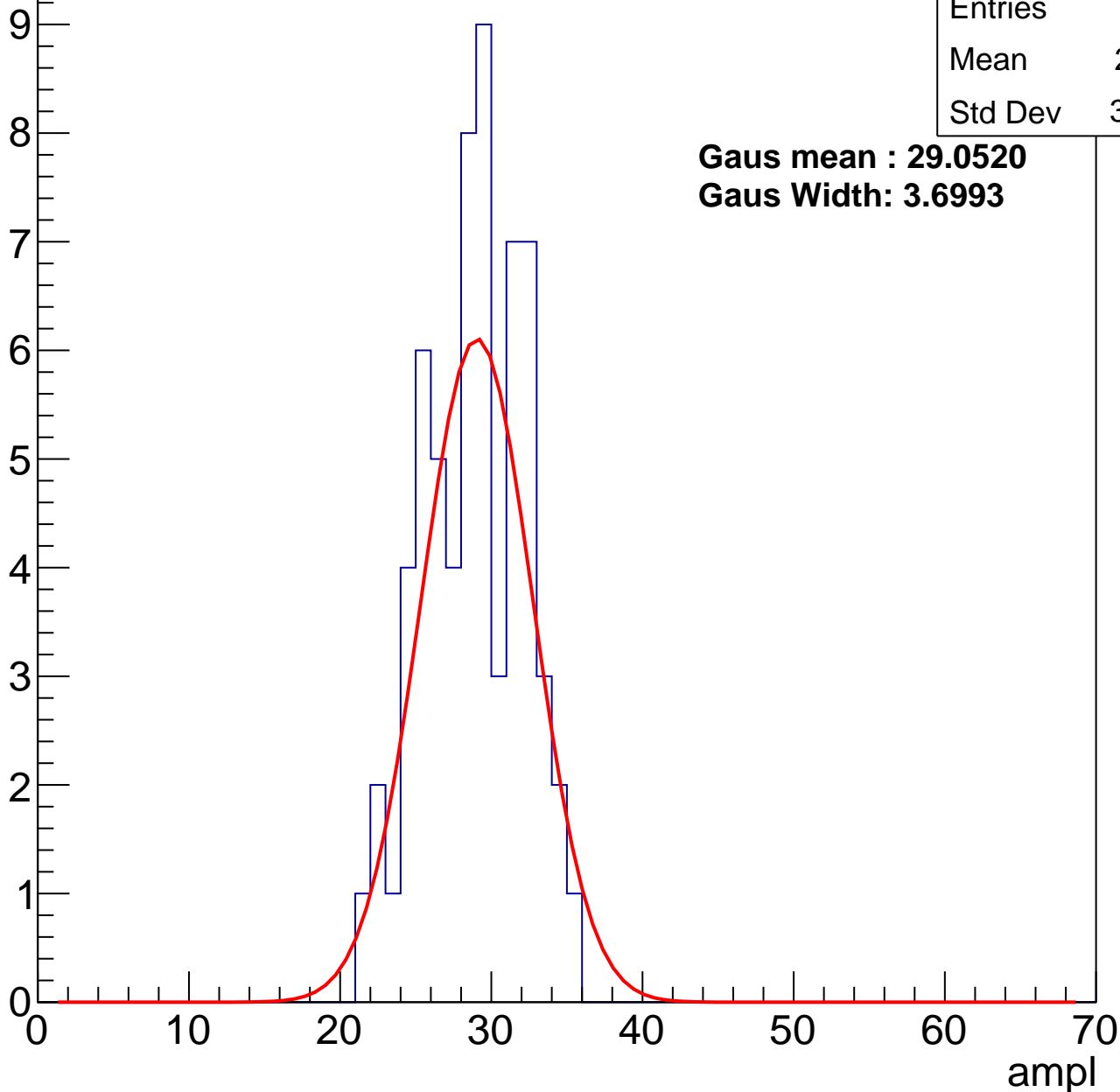
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	28.41
Std Dev	3.259

**Gaus mean : 29.0520**

**Gaus Width: 3.6993**



# B1L102S, U16-ch97, adc1

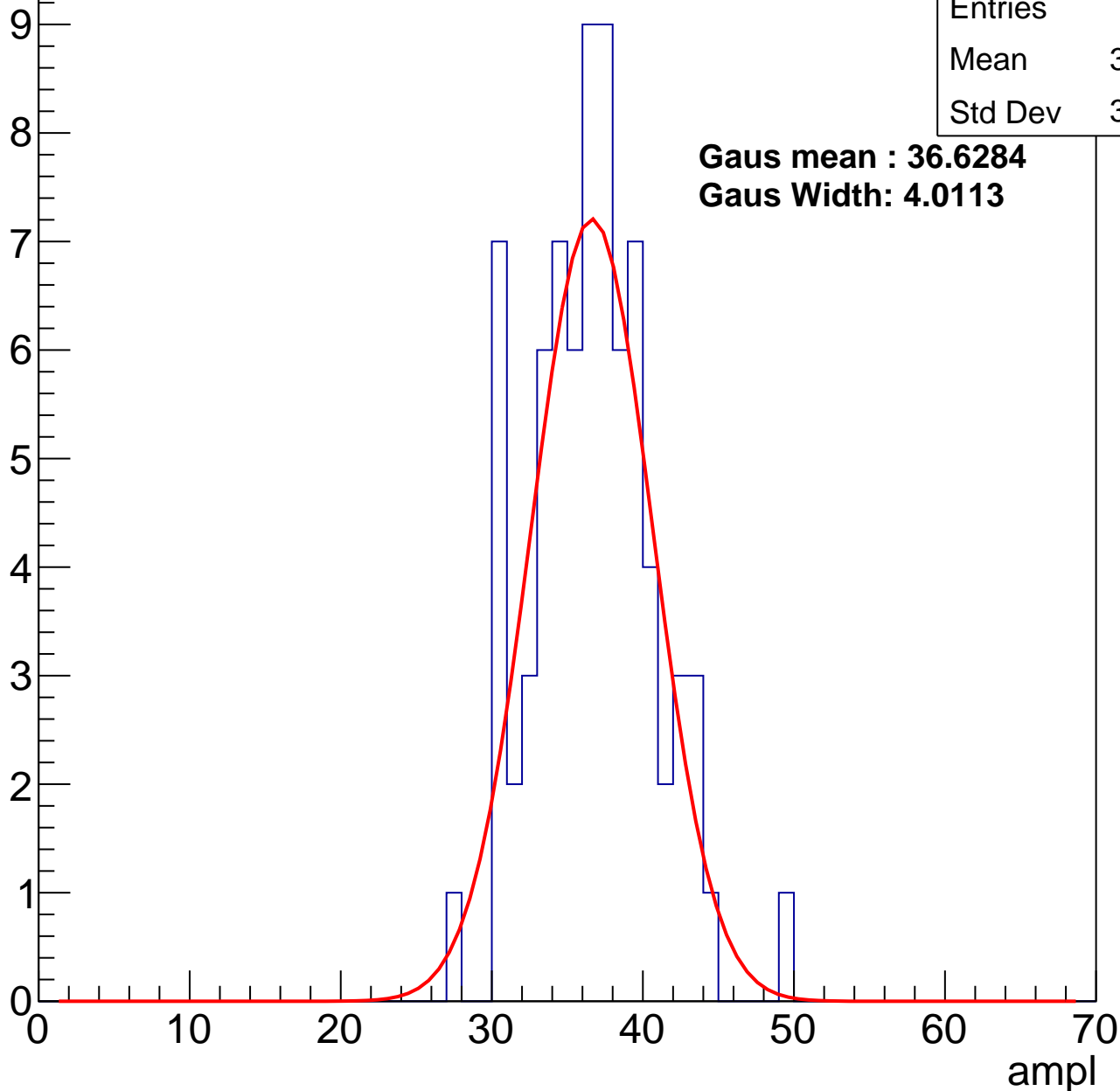
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	36.22
Std Dev	3.969

**Gaus mean : 36.6284**

**Gaus Width: 4.0113**



# B1L102S, U16-ch97, adc2

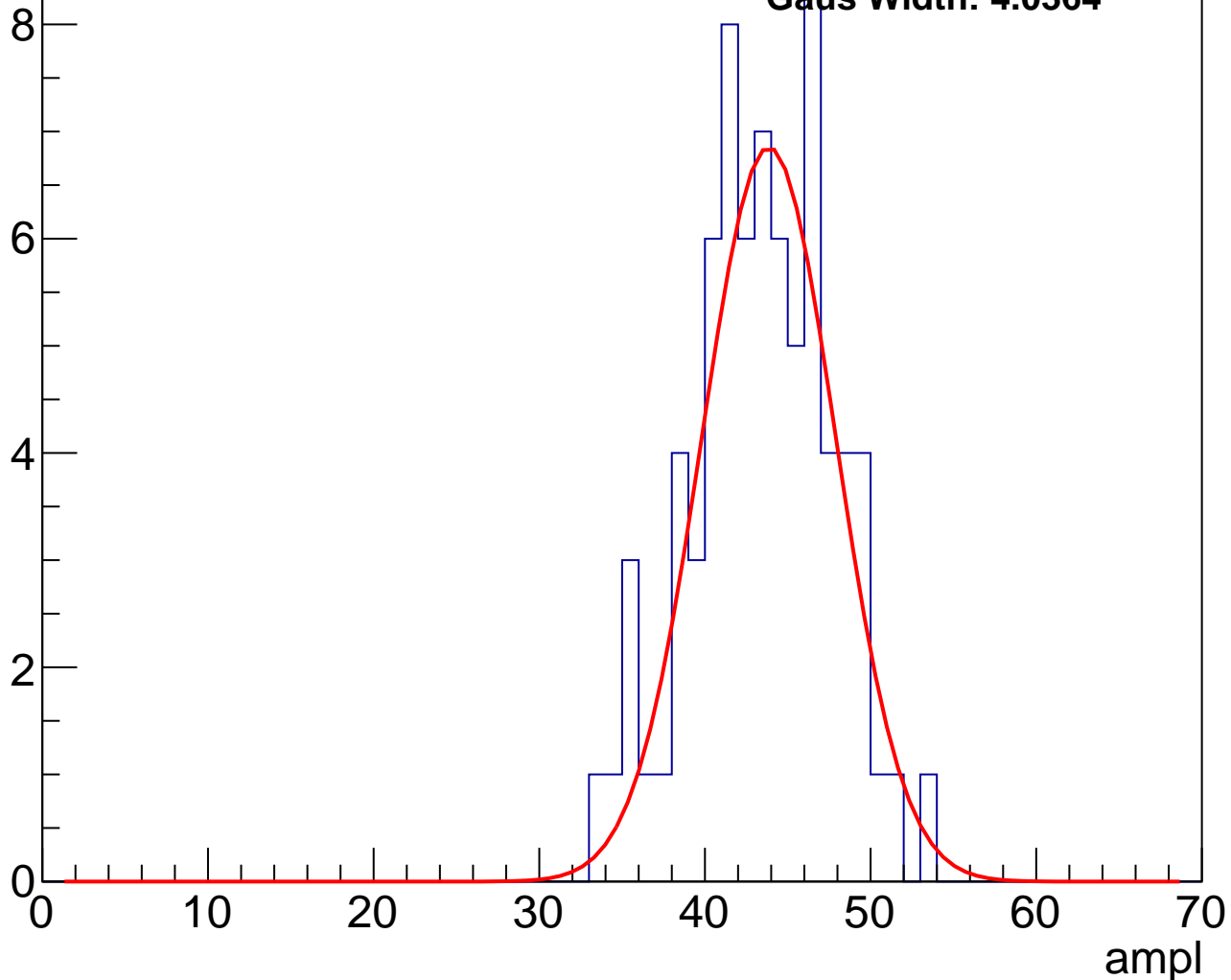
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	43.04
Std Dev	4.164

**Gaus mean : 43.8576**

**Gaus Width: 4.0364**

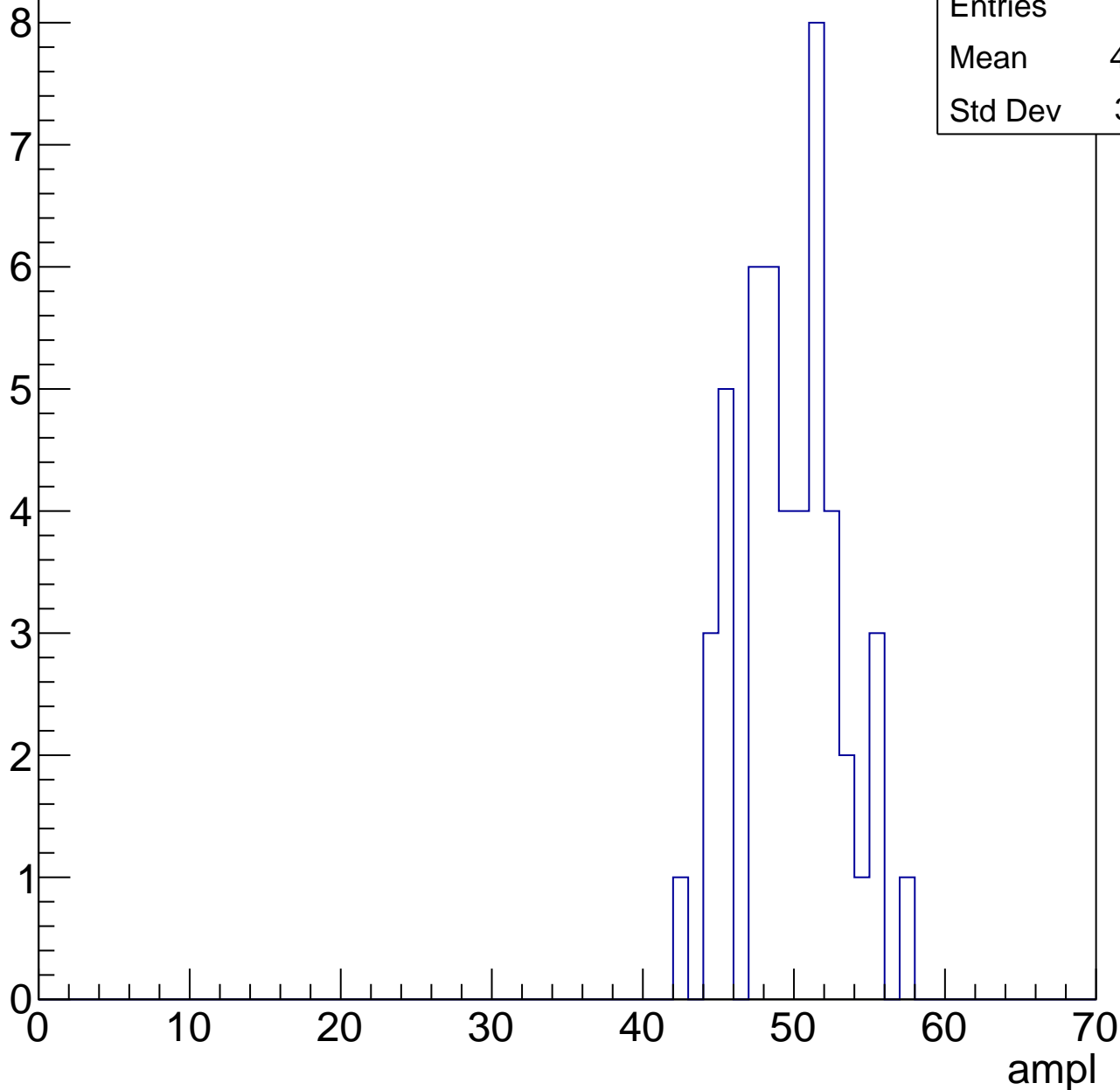


# B1L102S, U16-ch97, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	49.23
Std Dev	3.331

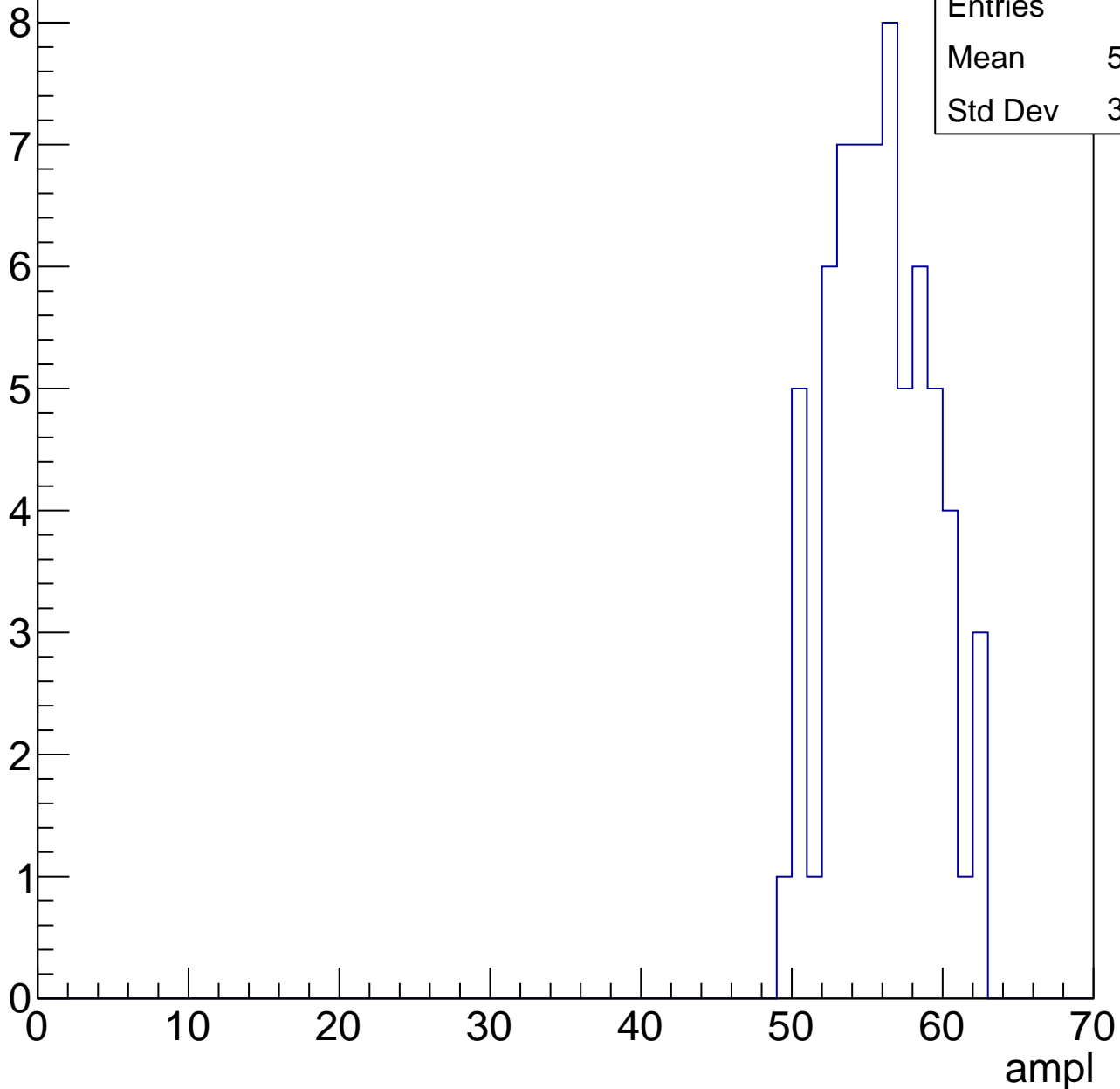


# B1L102S, U16-ch97, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	55.44
Std Dev	3.253

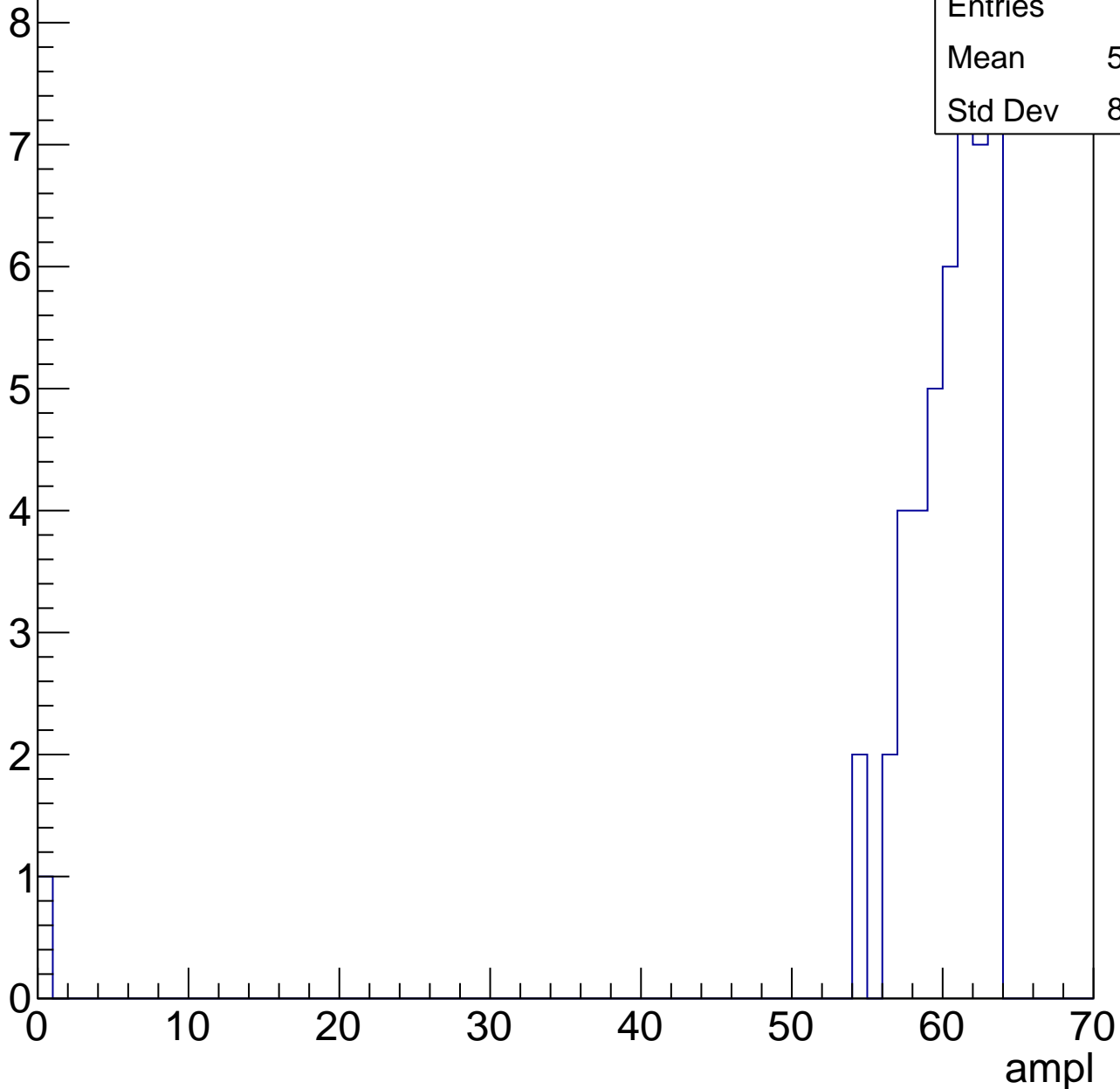


# B1L102S, U16-ch97, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	47
Mean	58.74
Std Dev	8.986



# B1L102S, U16-ch97, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

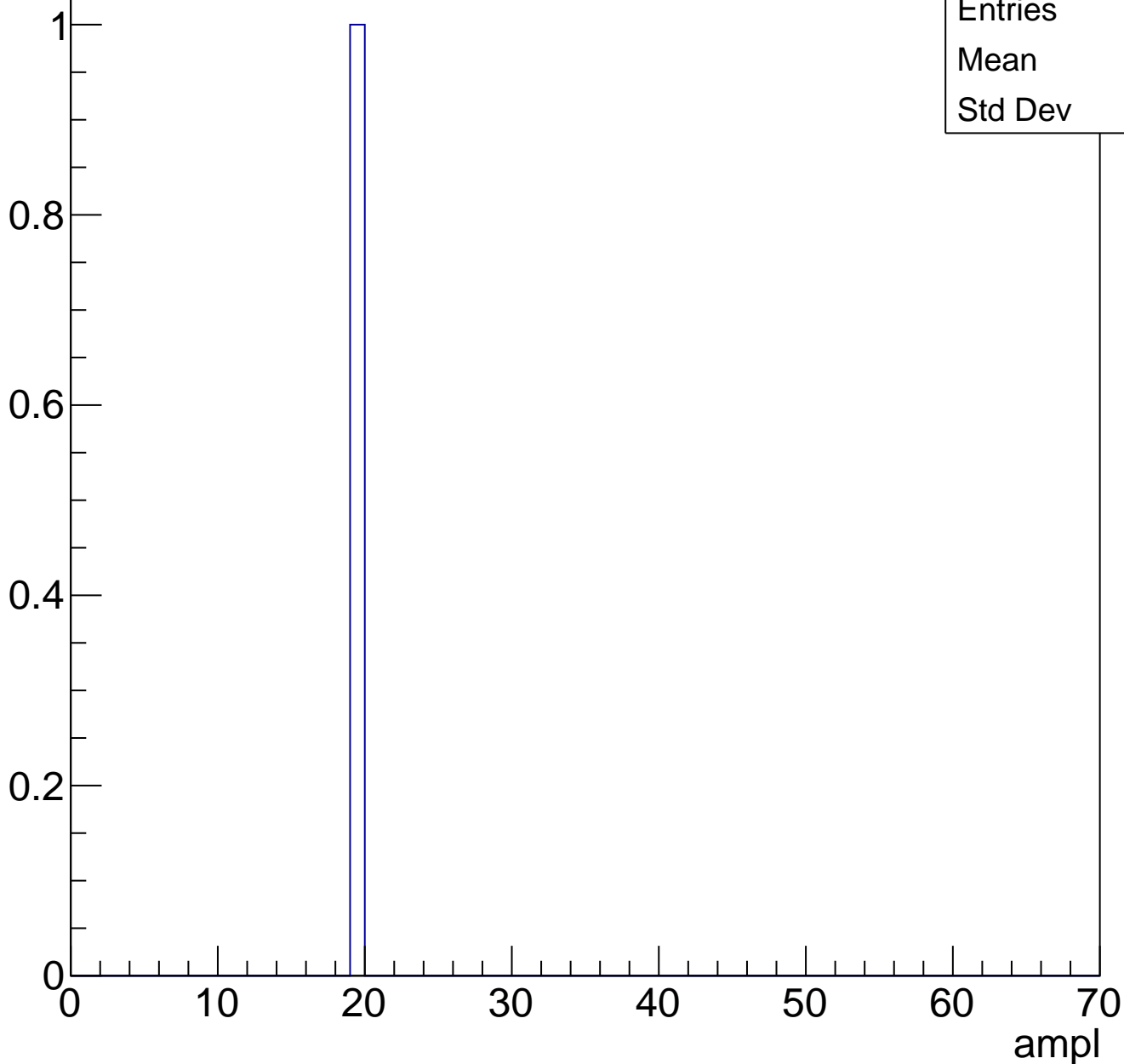




# B1L102S, U16-ch97, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch98, adc0

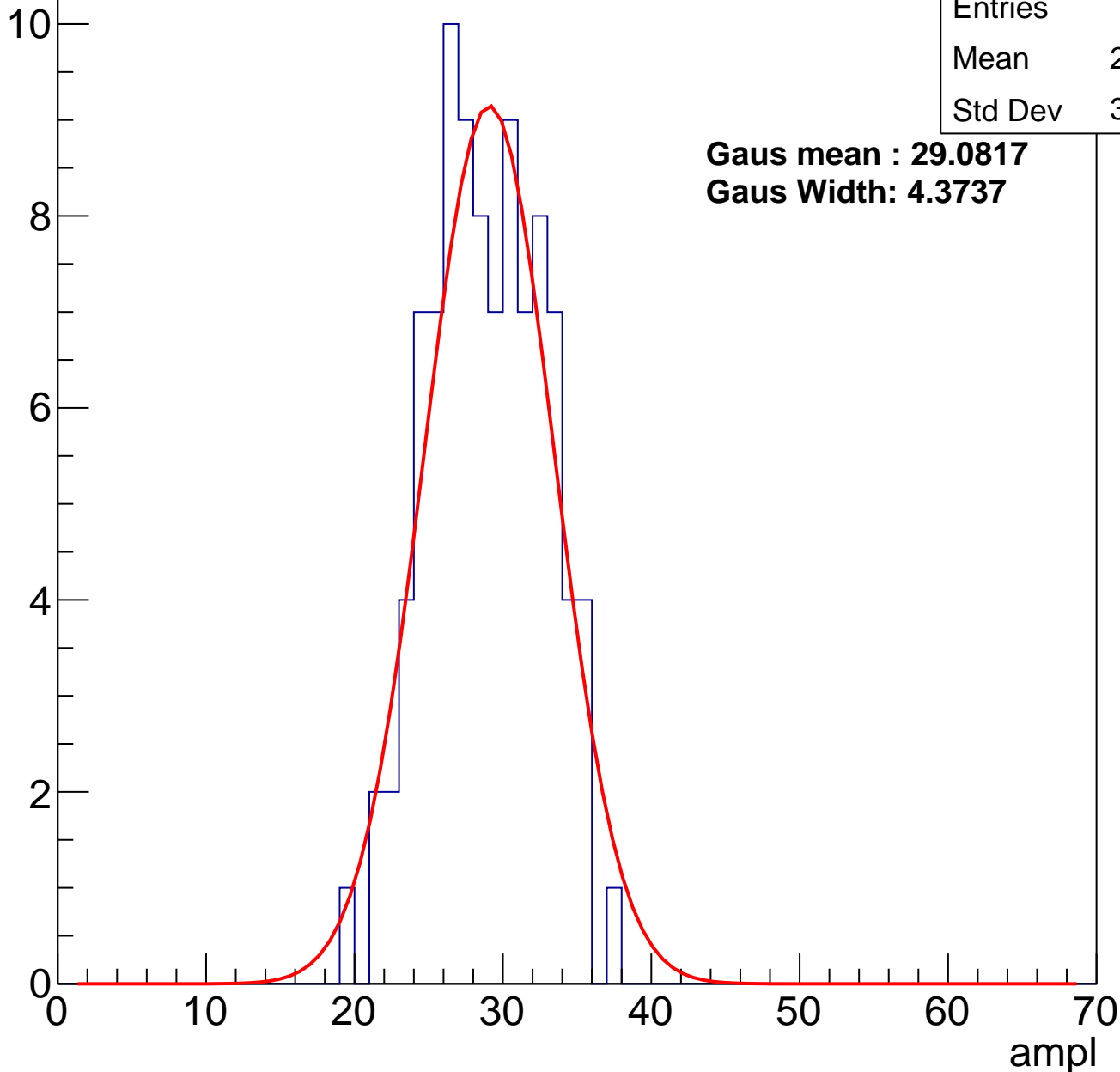
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	97
Mean	28.42
Std Dev	3.782

**Gaus mean : 29.0817**

**Gaus Width: 4.3737**

Entry



# B1L102S, U16-ch98, adc1

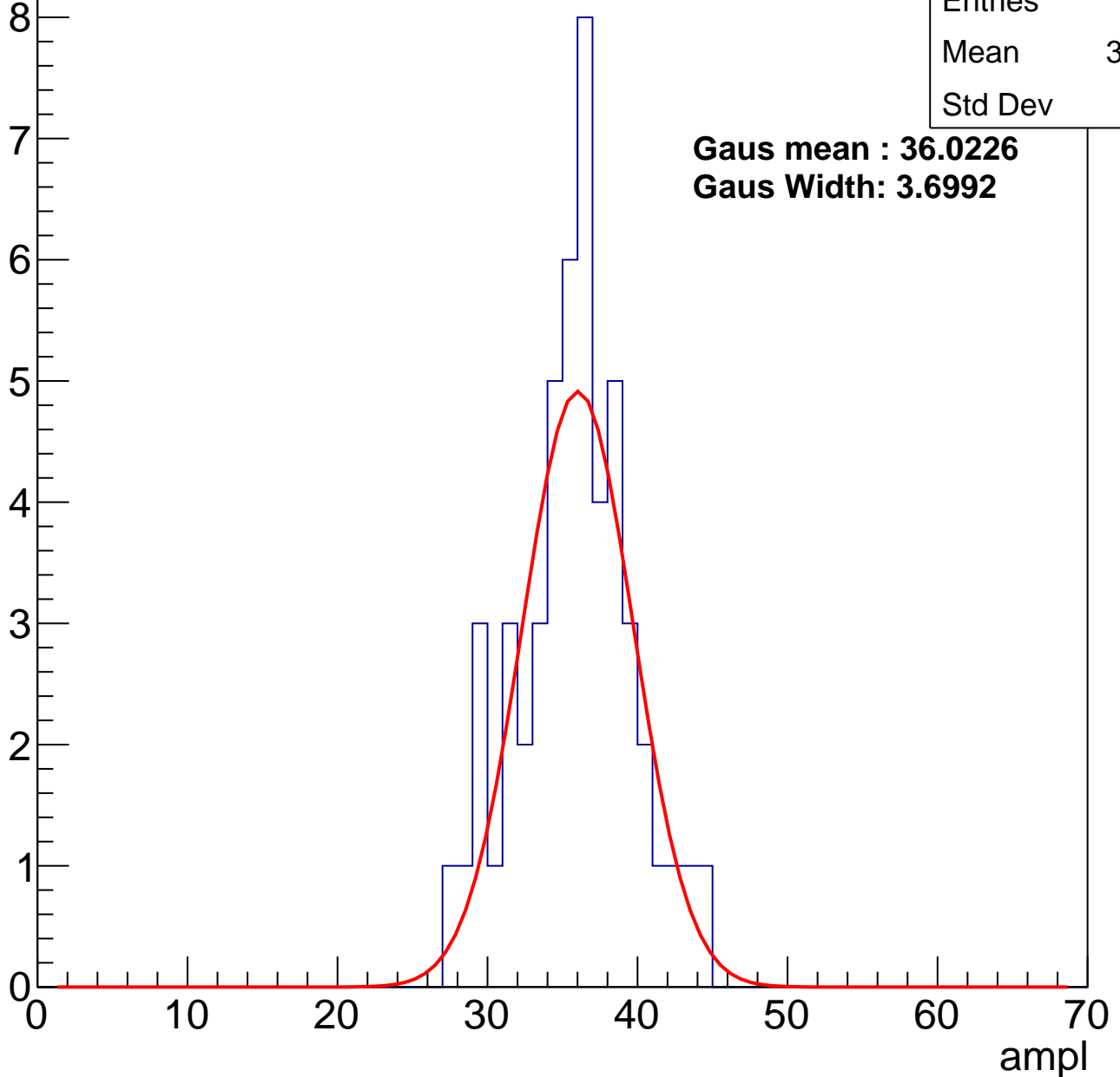
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	35.31
Std Dev	3.76

**Gaus mean : 36.0226**

**Gaus Width: 3.6992**



# B1L102S, U16-ch98, adc2

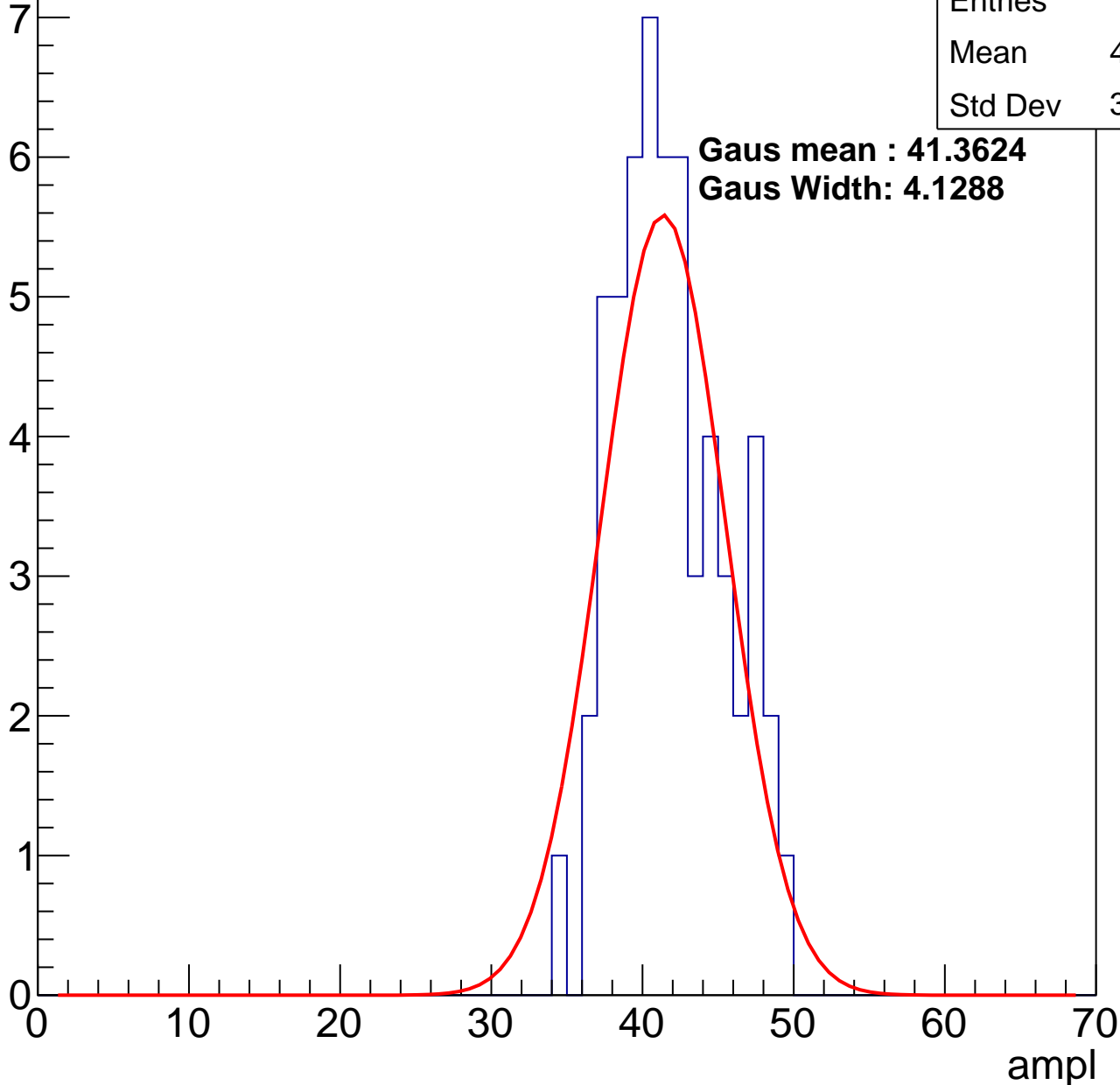
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	41.37
Std Dev	3.518

**Gaus mean : 41.3624**

**Gaus Width: 4.1288**

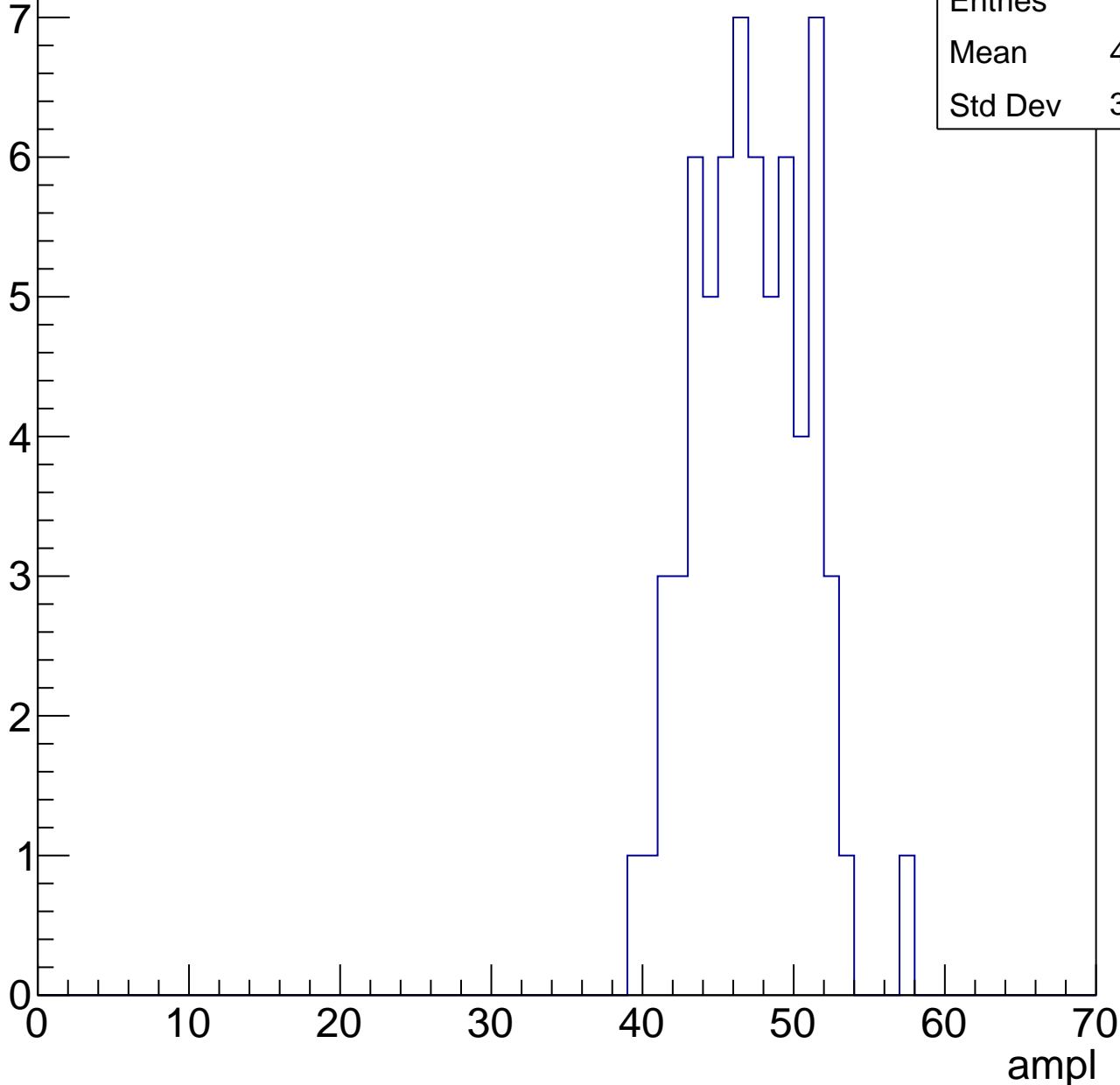


# B1L102S, U16-ch98, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	46.72
Std Dev	3.618

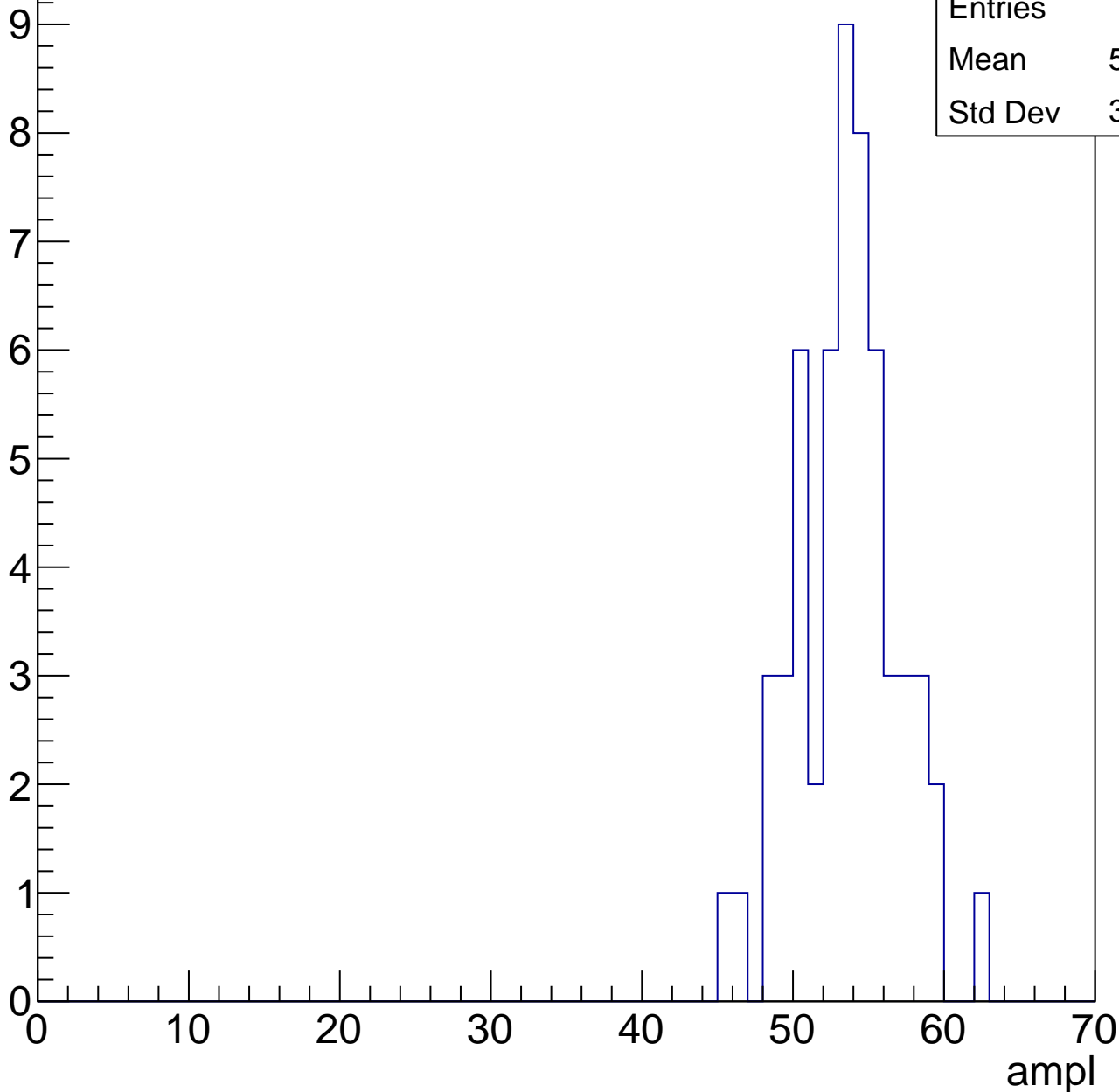


# B1L102S, U16-ch98, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	53.12
Std Dev	3.346

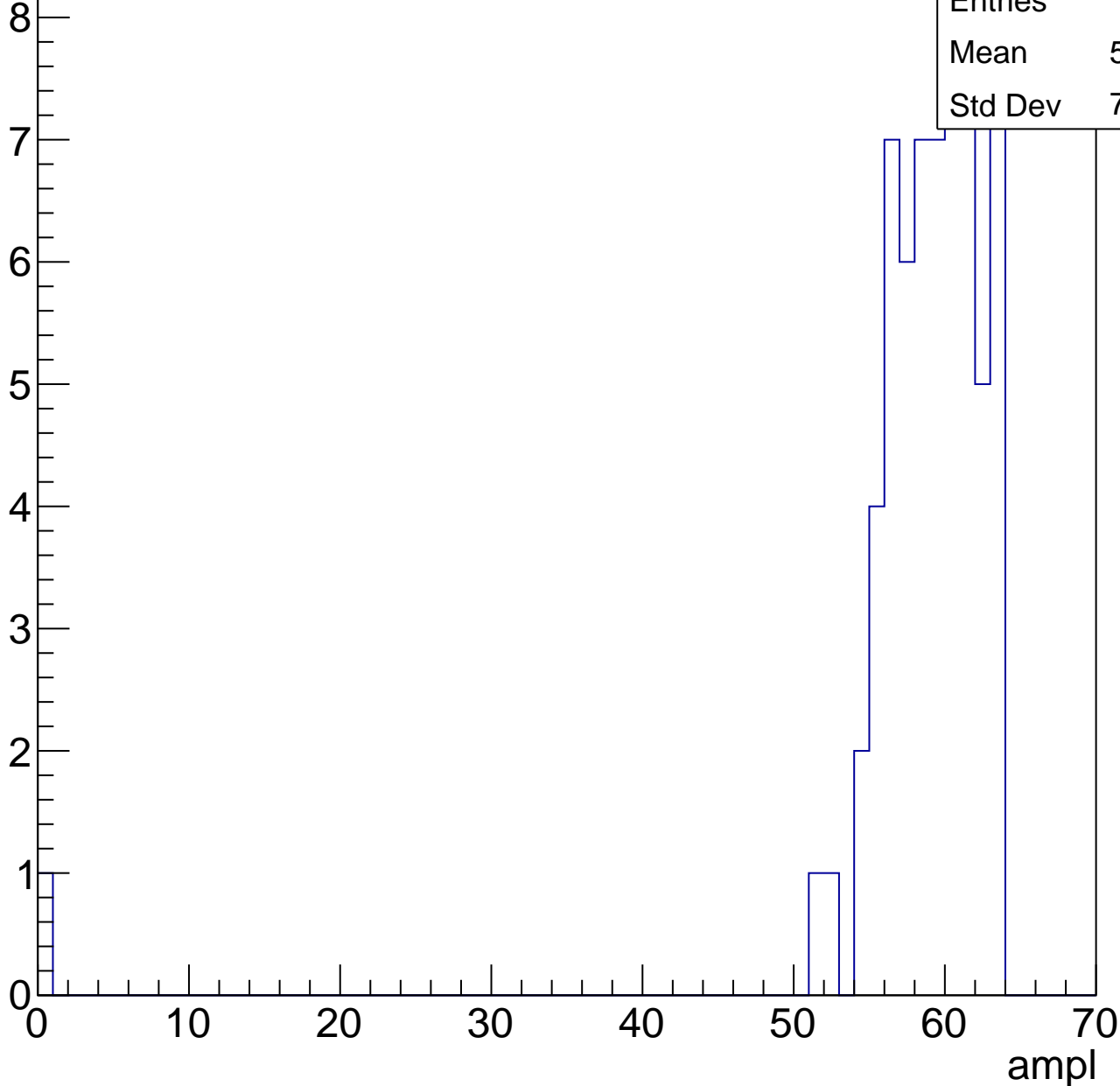


# B1L102S, U16-ch98, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

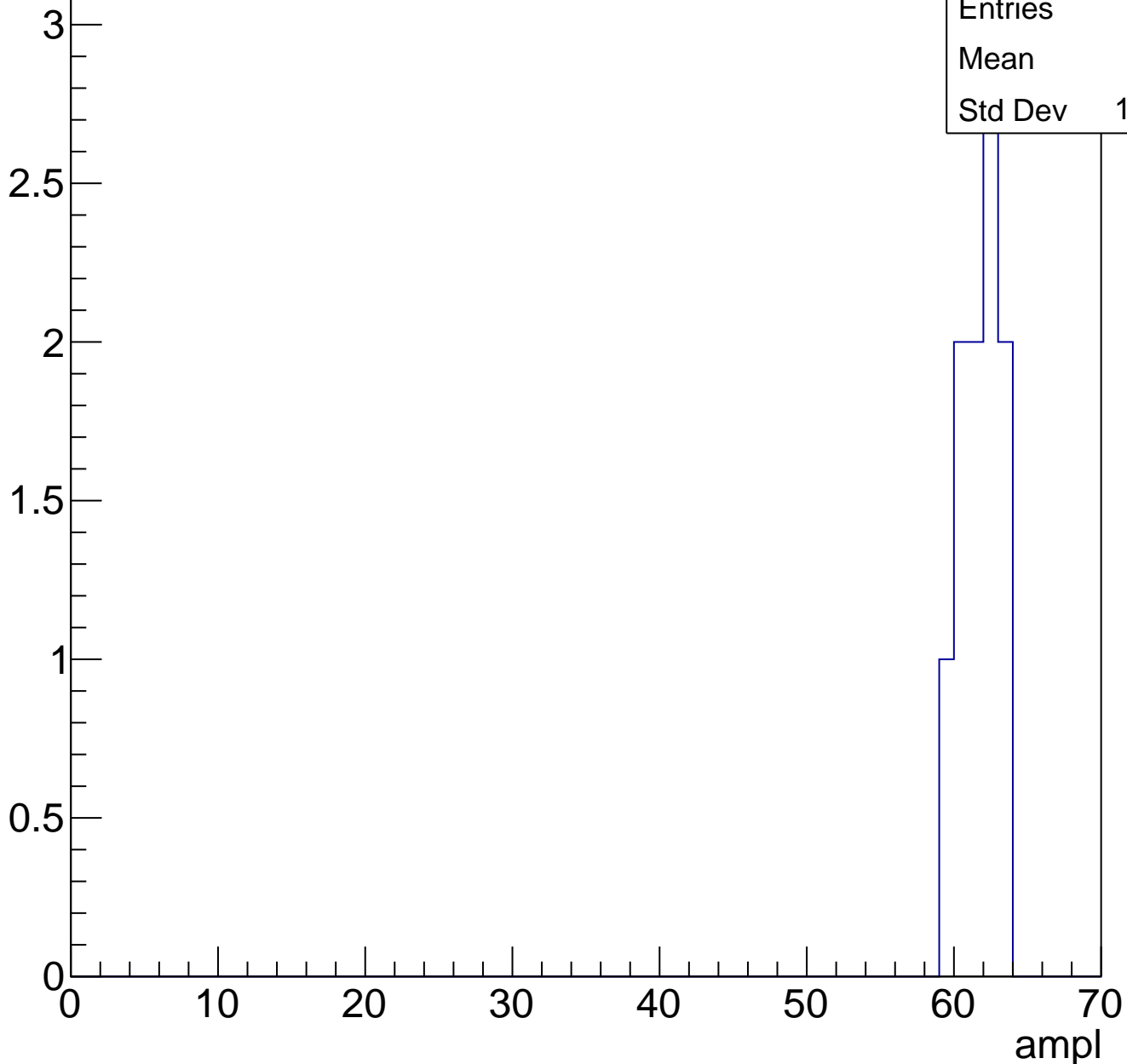
Entries	65
Mean	57.94
Std Dev	7.787



# B1L102S, U16-ch98, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	10
Mean	61.3
Std Dev	1.269



# B1L102S, U16-ch98, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch99, adc0

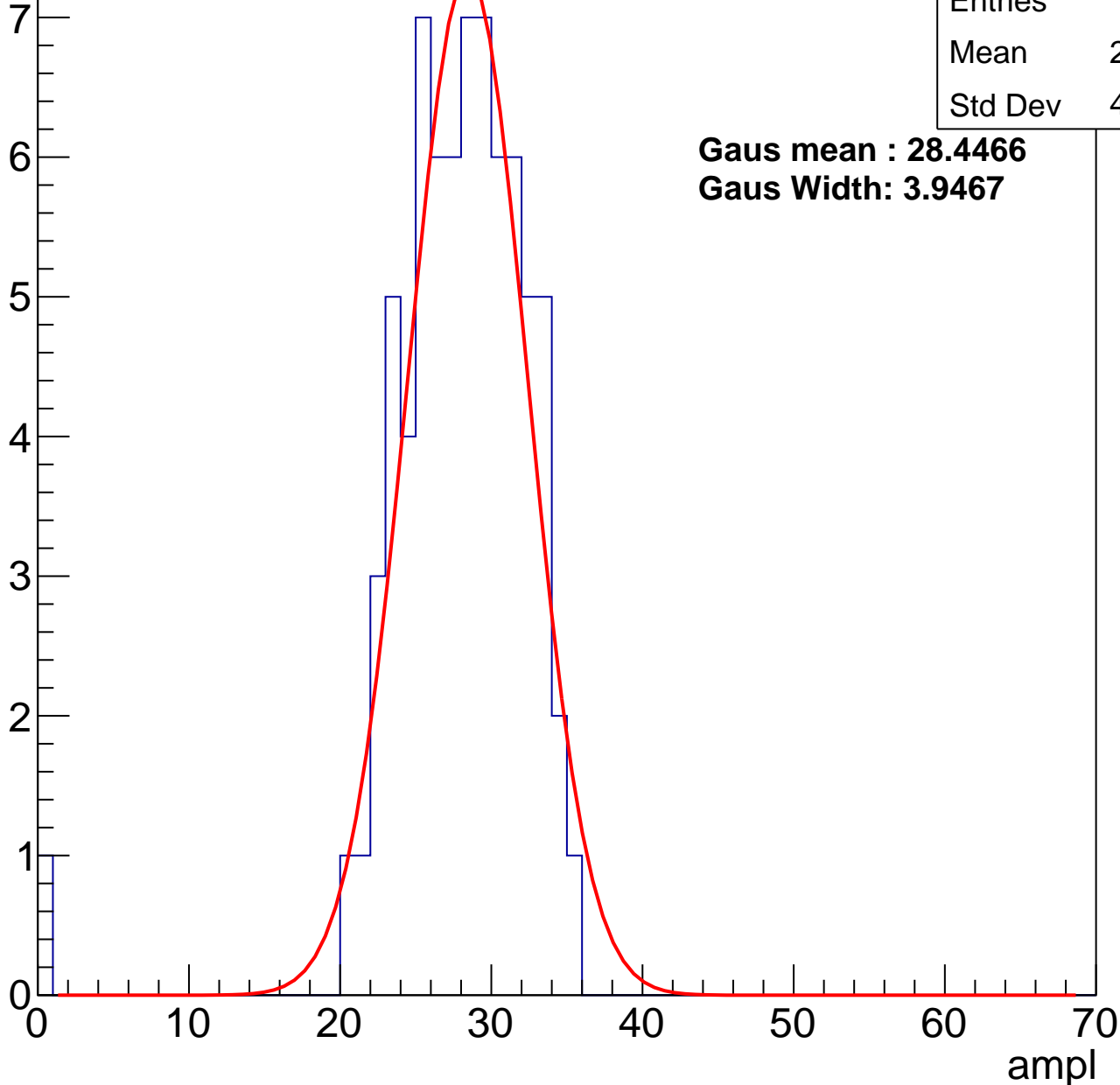
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	27.45
Std Dev	4.792

**Gaus mean : 28.4466**

**Gaus Width: 3.9467**



# B1L102S, U16-ch99, adc1

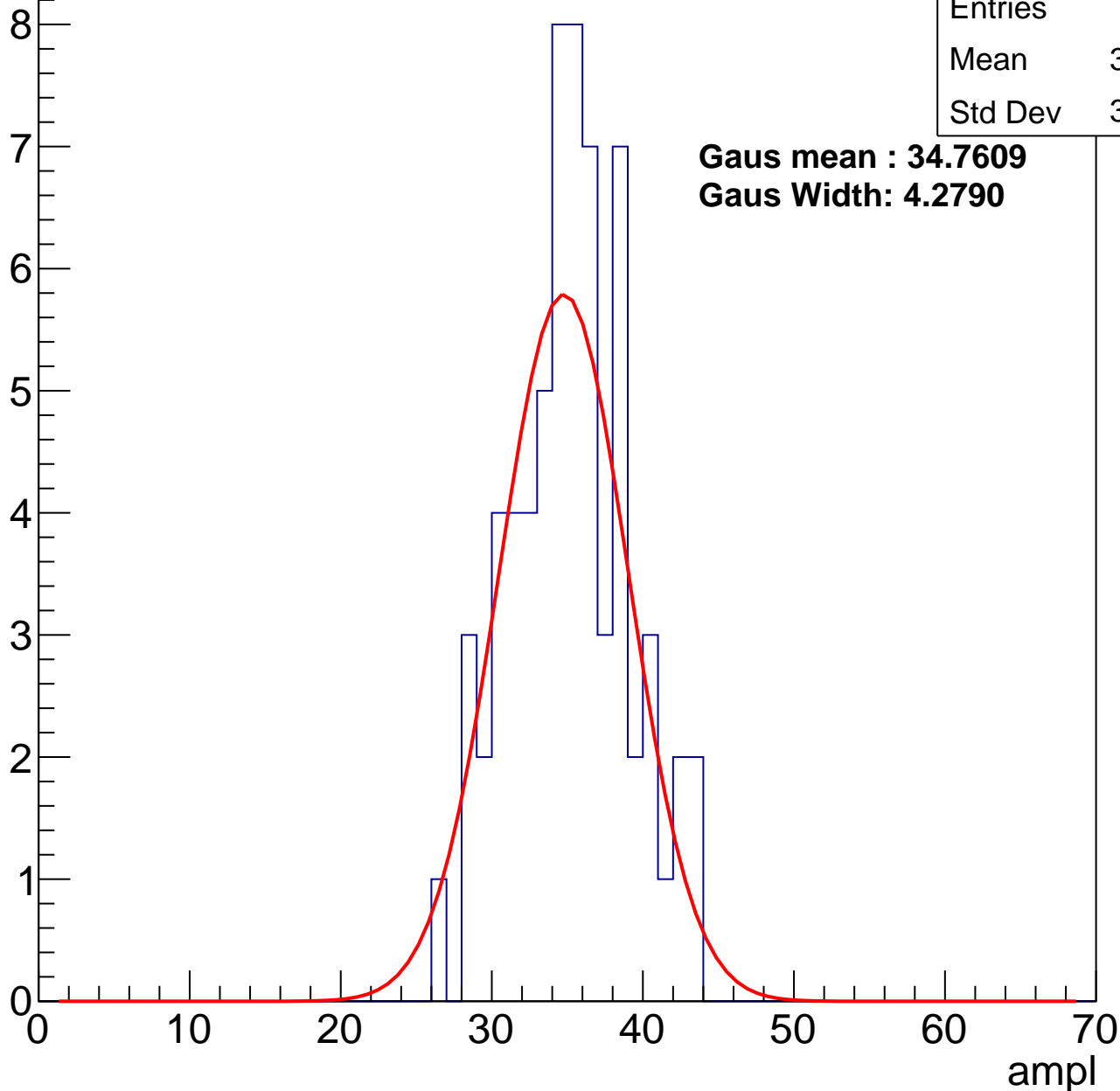
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	34.77
Std Dev	3.845

**Gaus mean : 34.7609**

**Gaus Width: 4.2790**



# B1L102S, U16-ch99, adc2

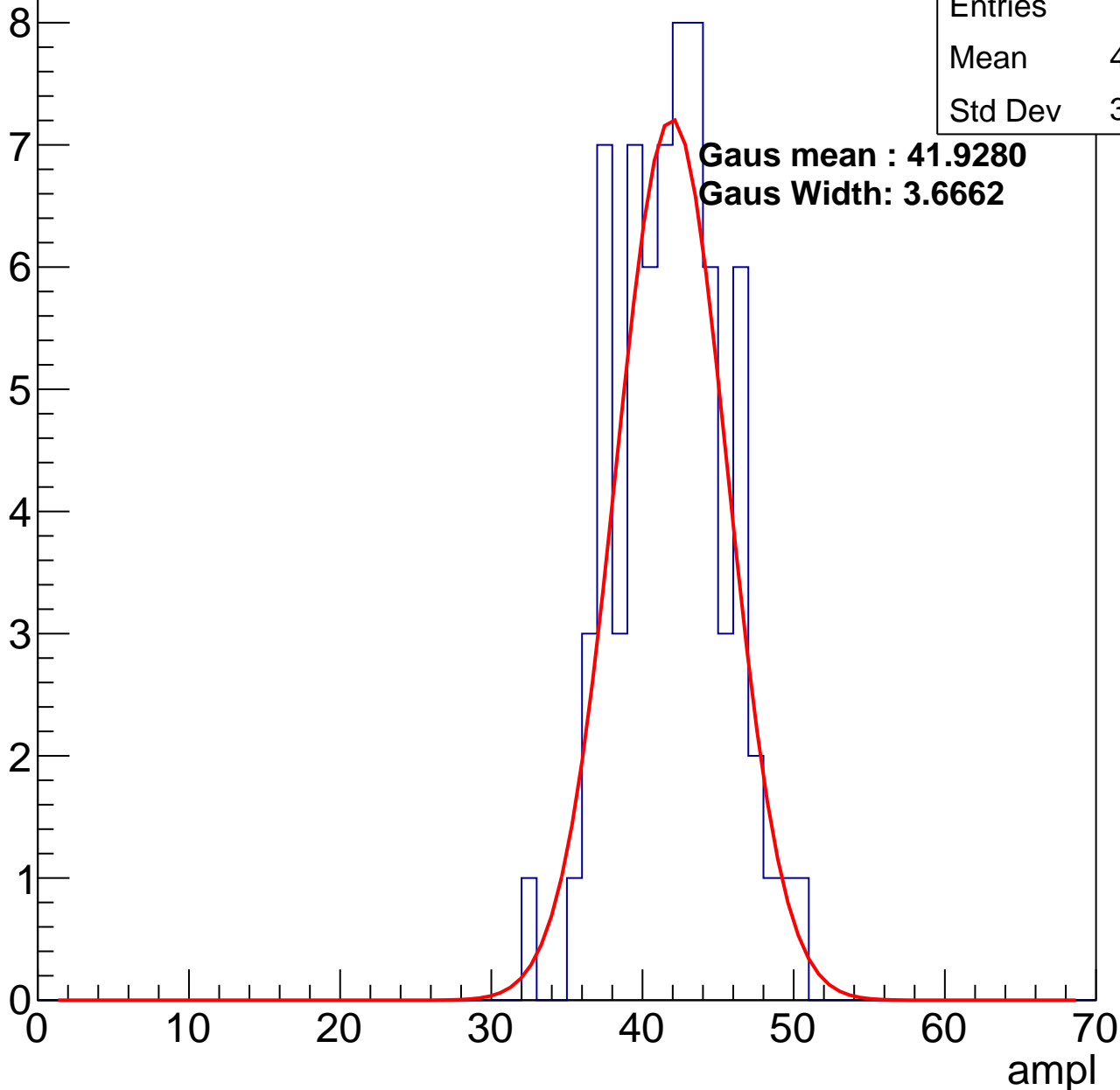
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	41.46
Std Dev	3.575

**Gaus mean : 41.9280**

**Gaus Width: 3.6662**

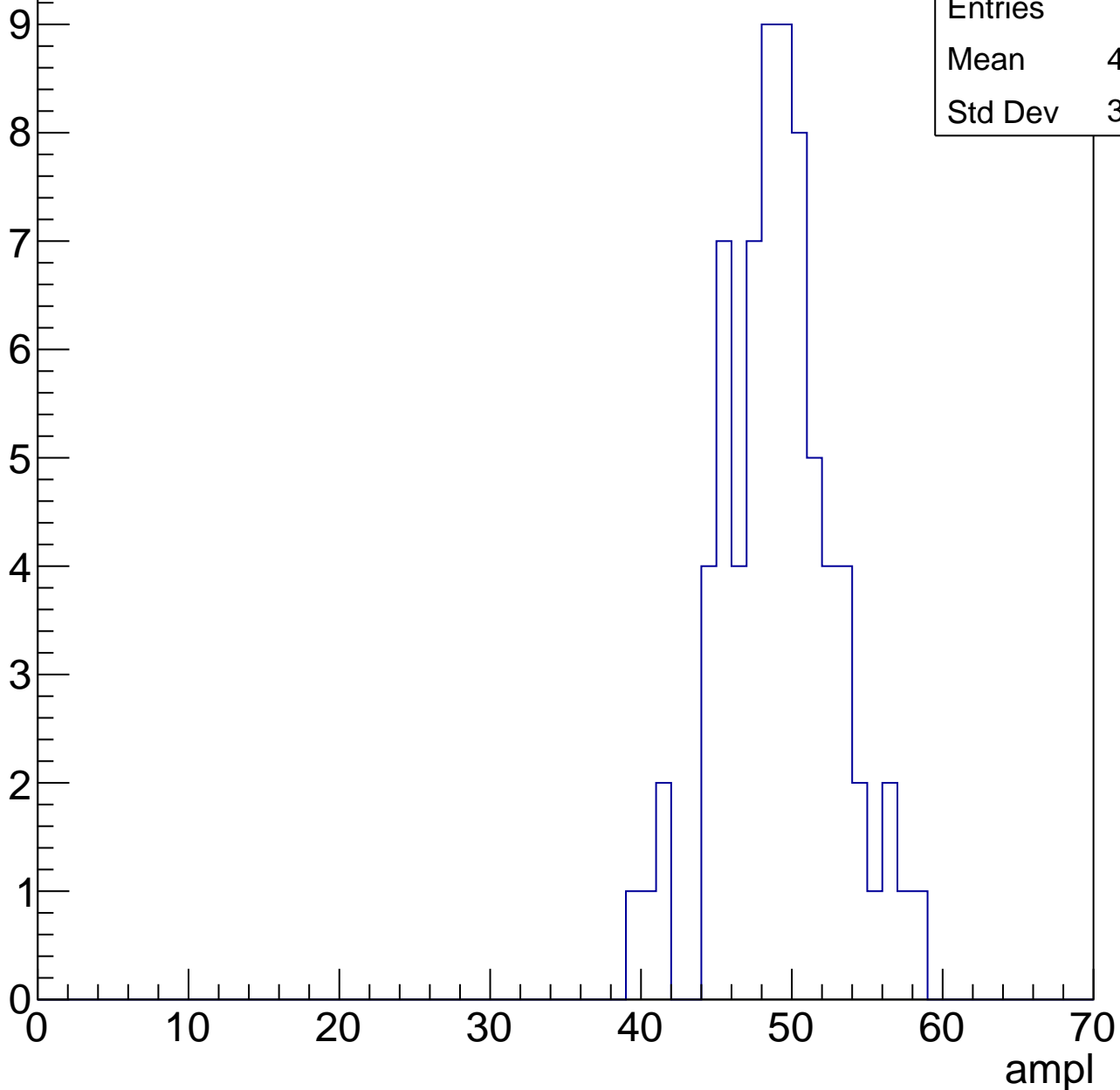


# B1L102S, U16-ch99, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	48.65
Std Dev	3.805

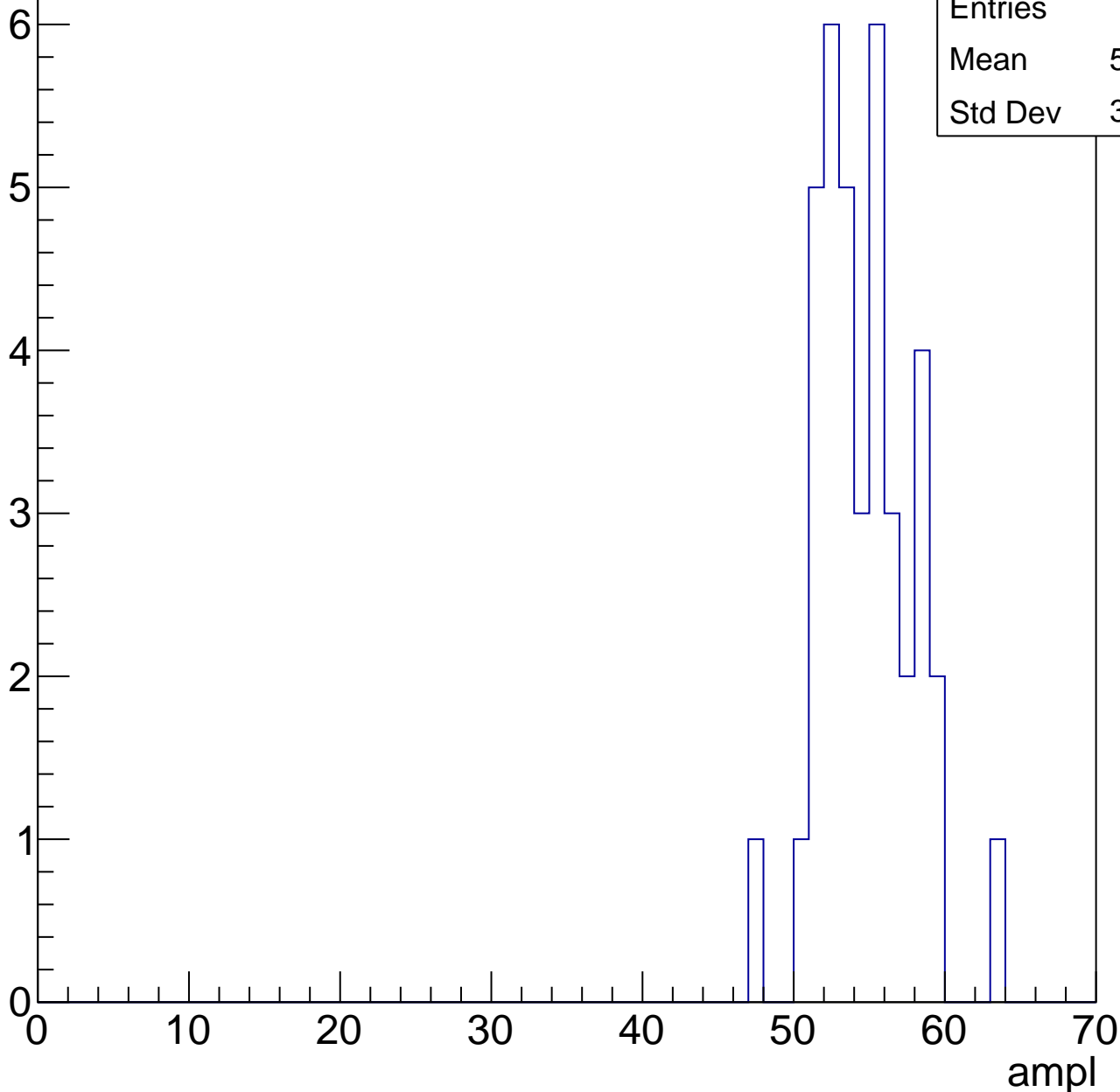


# B1L102S, U16-ch99, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	39
Mean	54.26
Std Dev	3.069



# B1L102S, U16-ch99, adc5

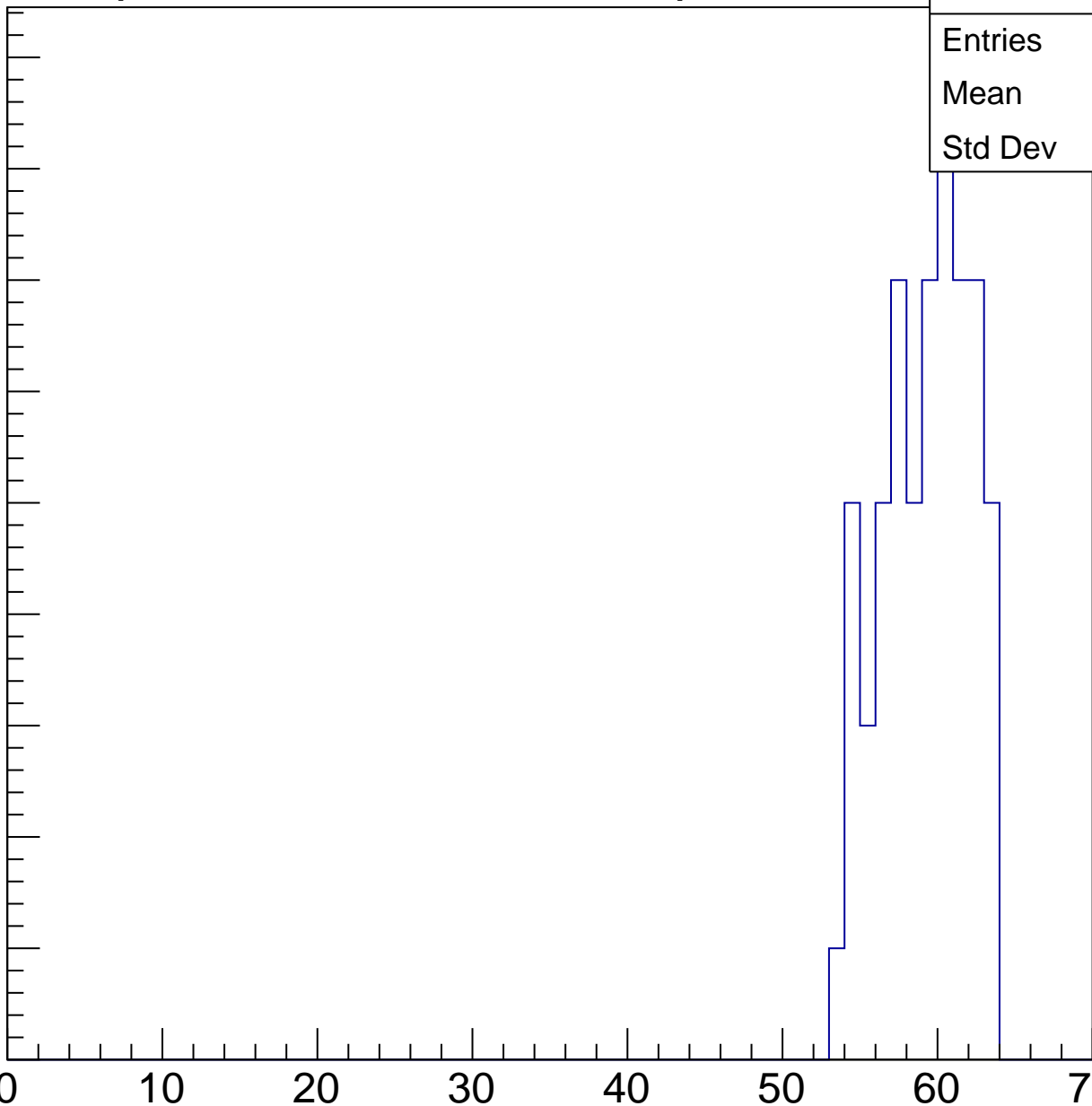
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

9  
8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	61
Mean	58.79
Std Dev	2.759

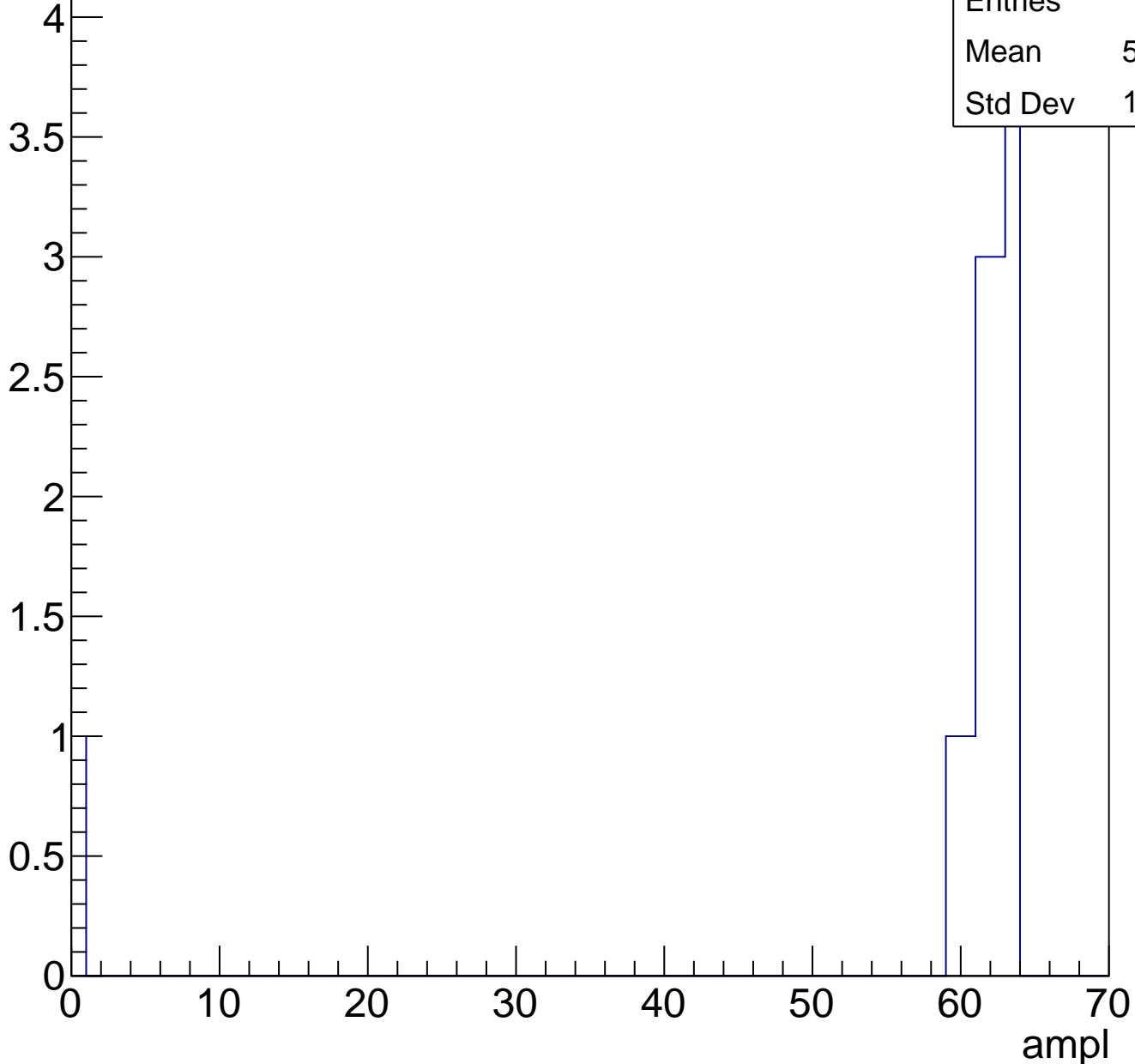
ampl



# B1L102S, U16-ch99, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch99, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	1
Mean	0
Std Dev	0

# B1L102S, U16-ch100, adc0

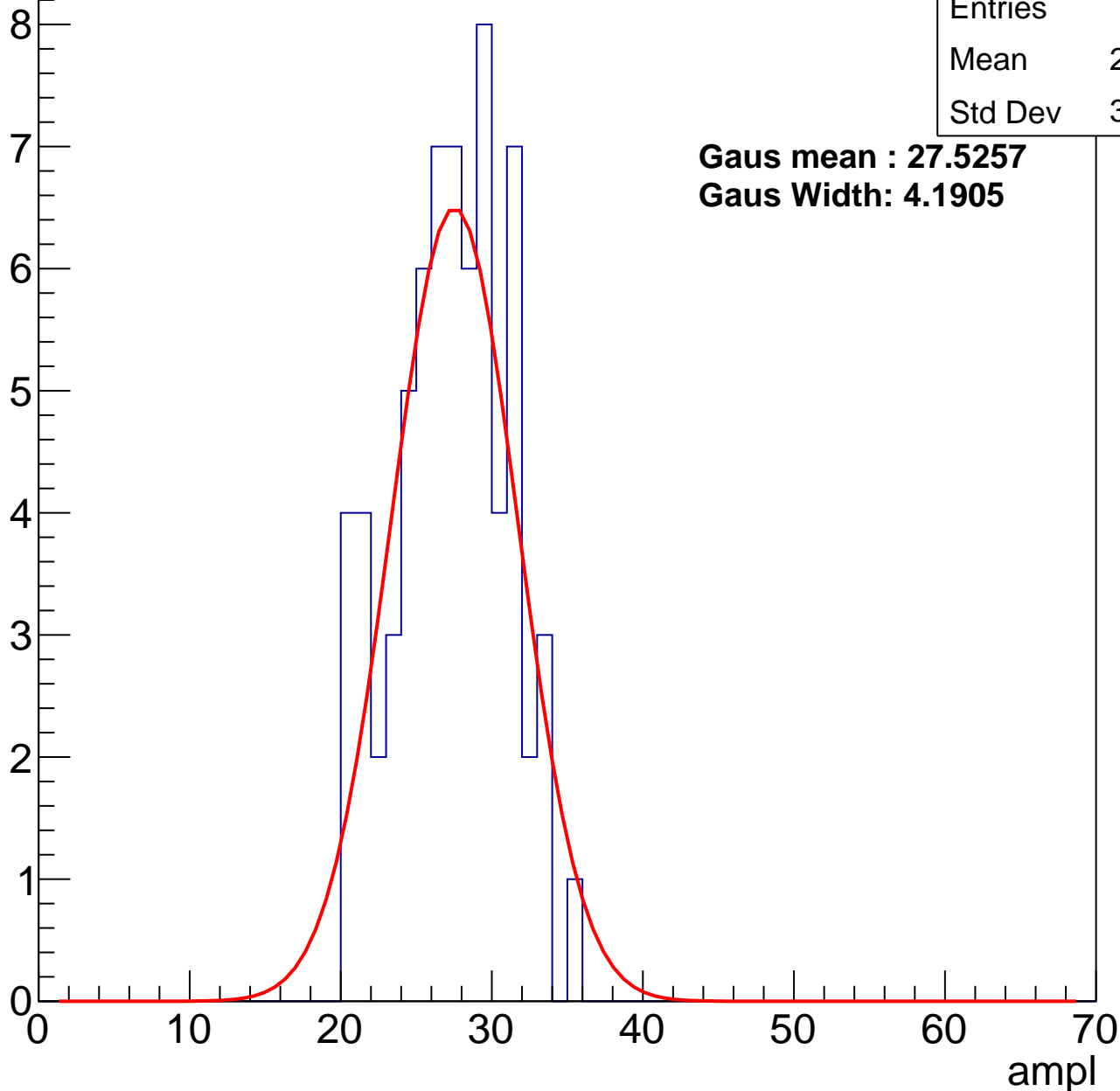
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	26.86
Std Dev	3.653

**Gaus mean : 27.5257**

**Gaus Width: 4.1905**



# B1L102S, U16-ch100, adc1

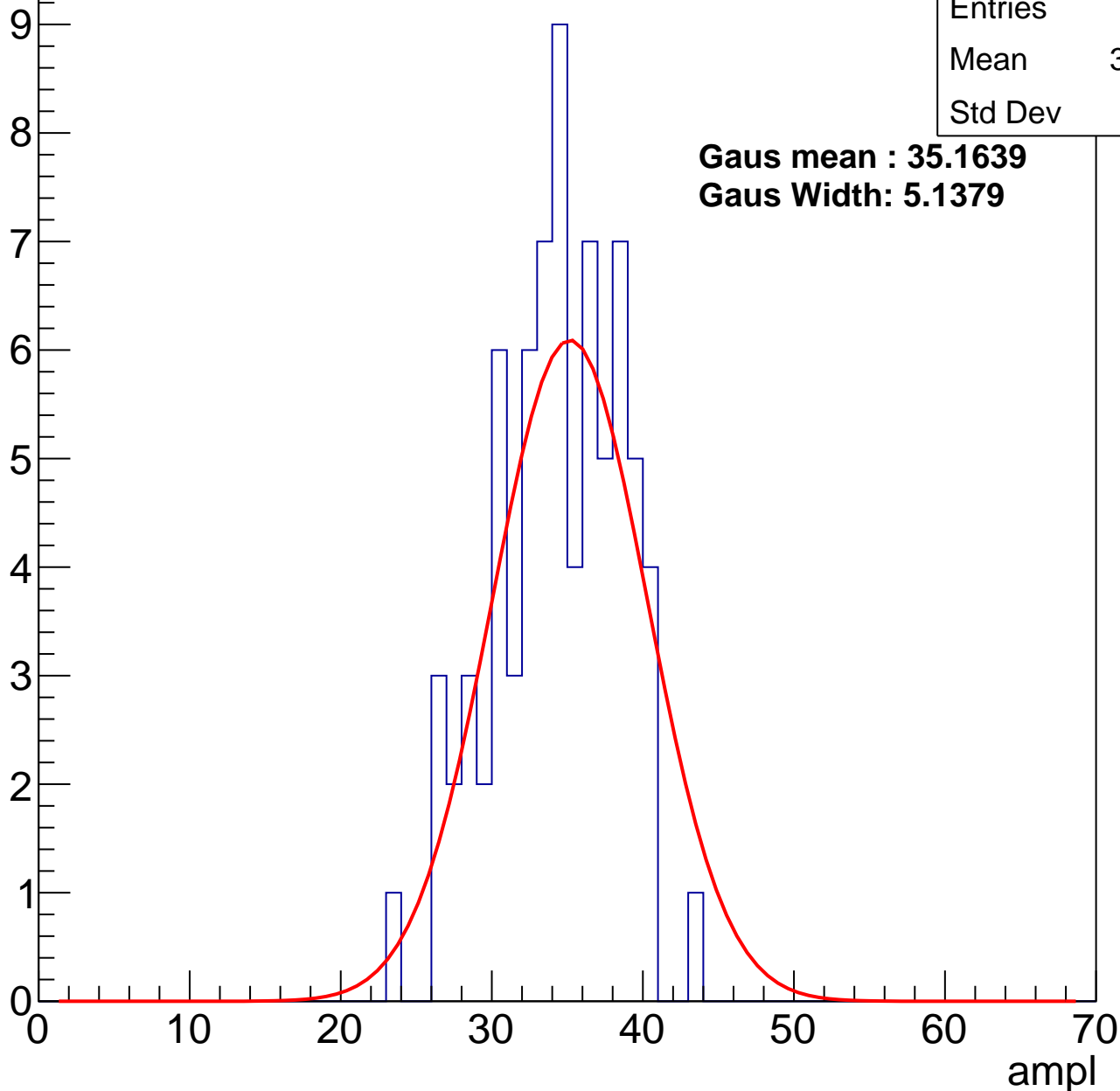
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	33.87
Std Dev	4.1

**Gaus mean : 35.1639**

**Gaus Width: 5.1379**



# B1L102S, U16-ch100, adc2

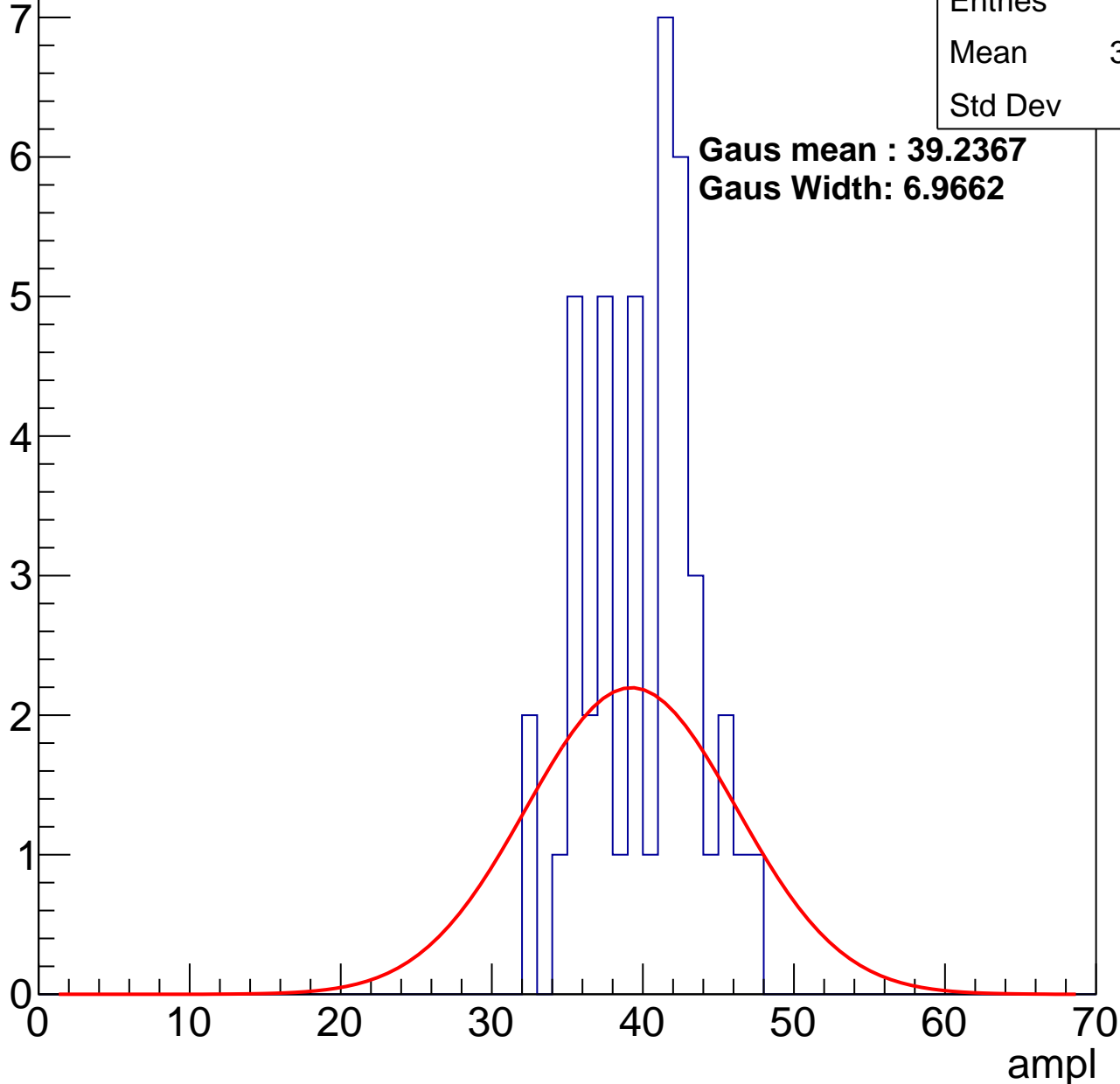
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	43
Mean	39.49
Std Dev	3.65

**Gaus mean : 39.2367**

**Gaus Width: 6.9662**

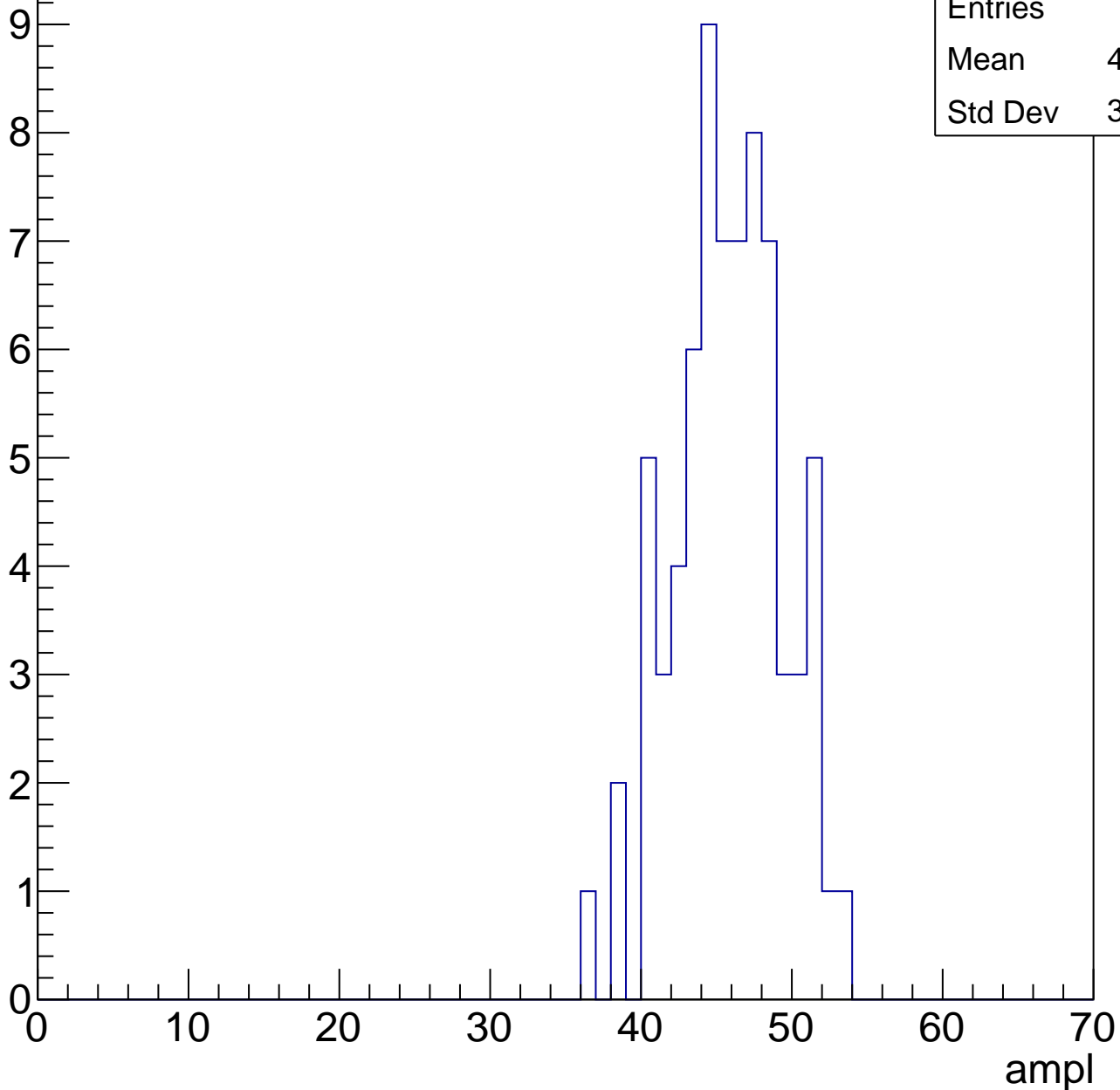


# B1L102S, U16-ch100, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	72
Mean	45.32
Std Dev	3.597

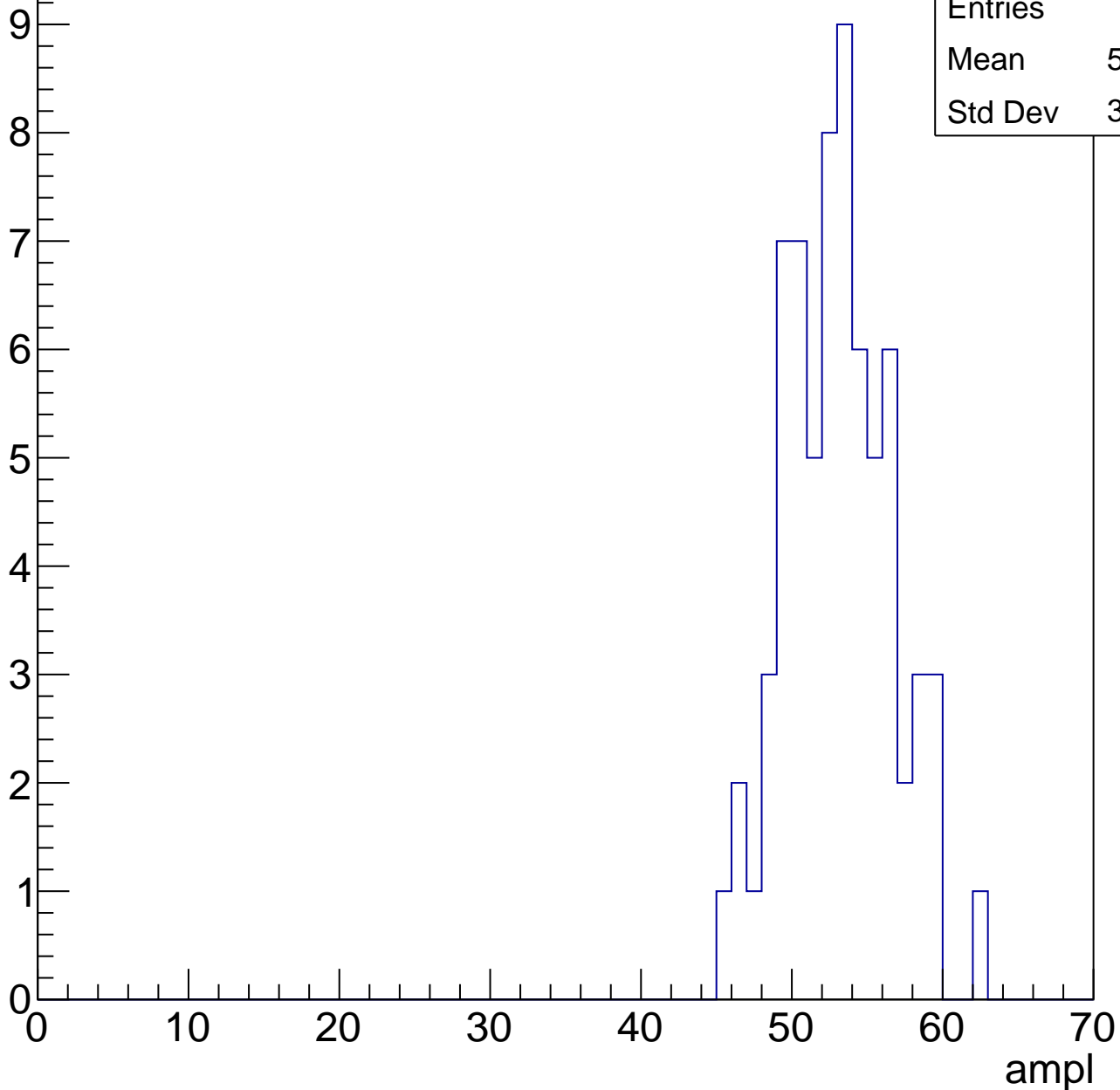


# B1L102S, U16-ch100, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	52.62
Std Dev	3.494

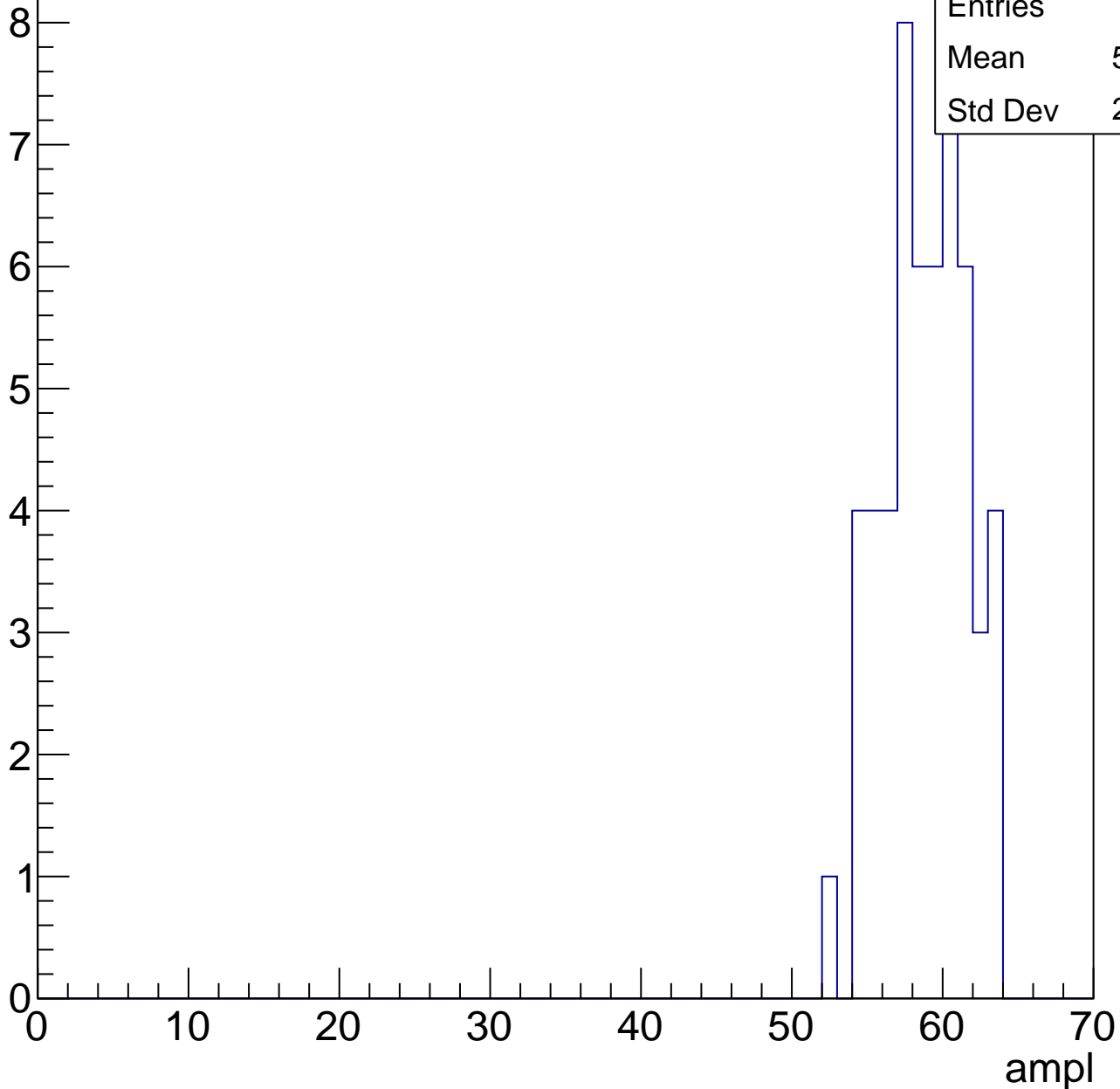


# B1L102S, U16-ch100, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	58.41
Std Dev	2.691

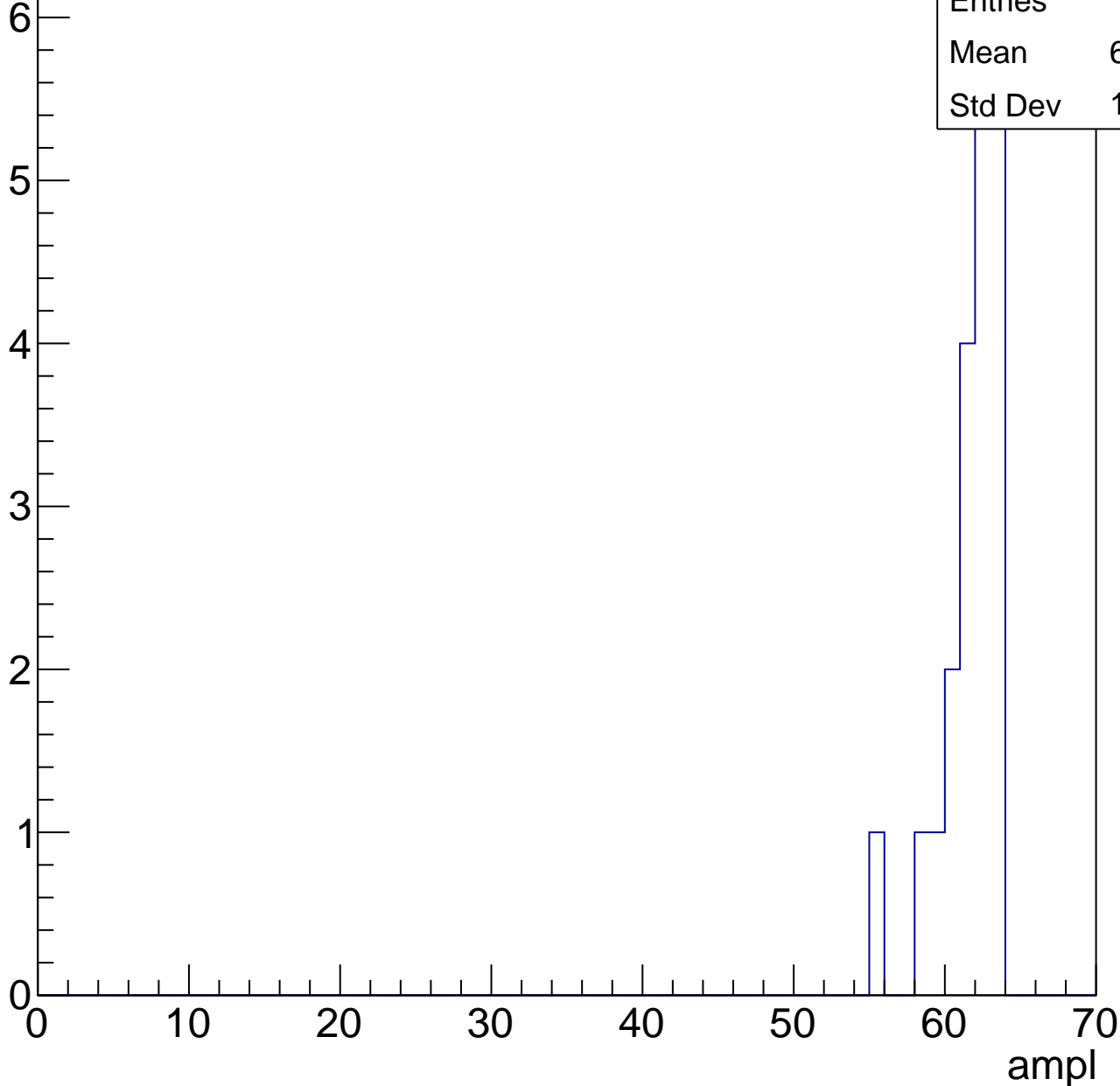


# B1L102S, U16-ch100, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	21
Mean	61.24
Std Dev	1.949





# B1L102S, U16-ch100, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch101, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	94
Mean	28.91
Std Dev	6.565

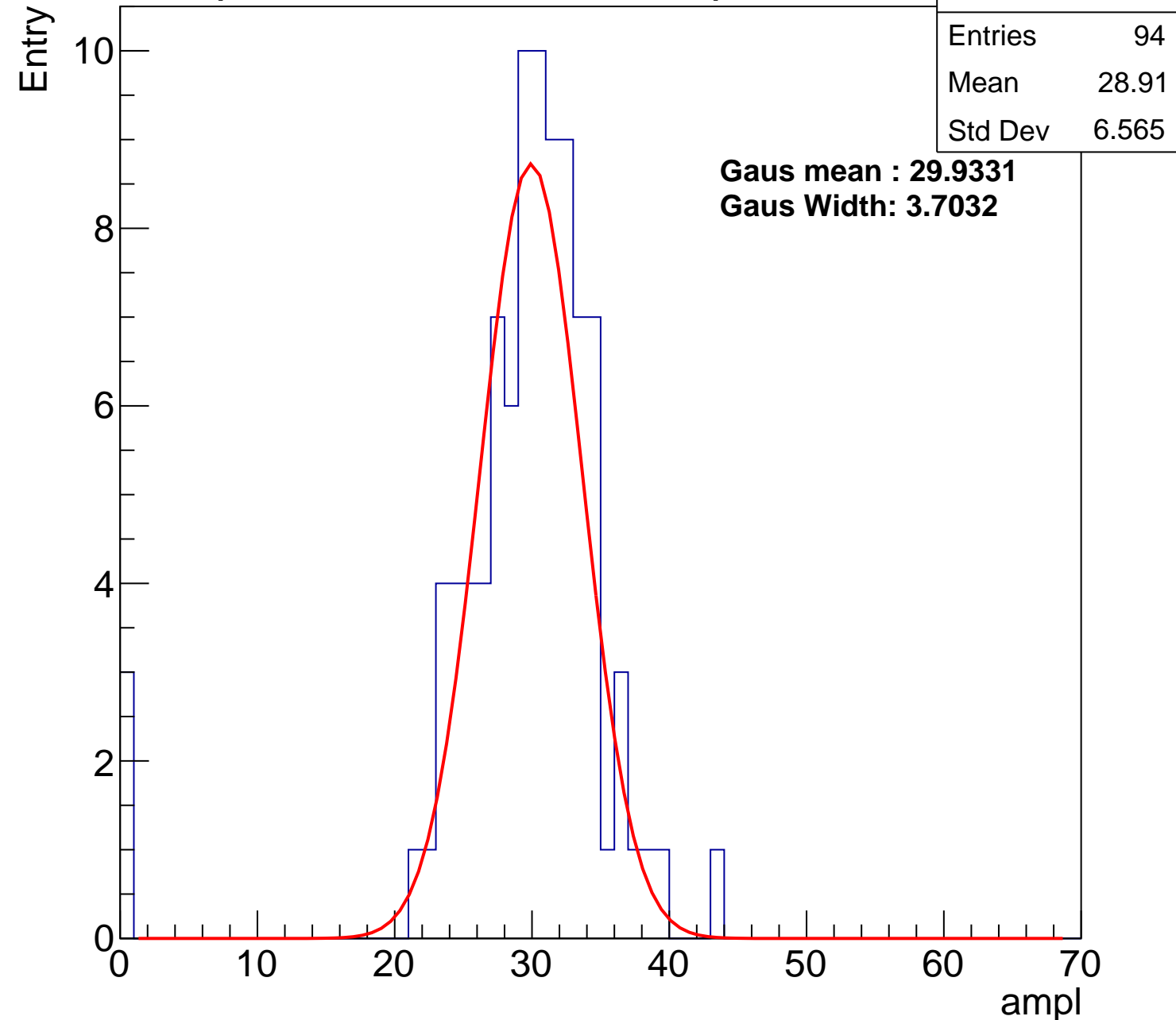
**Gaus mean : 29.9331**

**Gaus Width: 3.7032**

Entry

10  
8  
6  
4  
2  
0

ampl



# B1L102S, U16-ch101, adc1

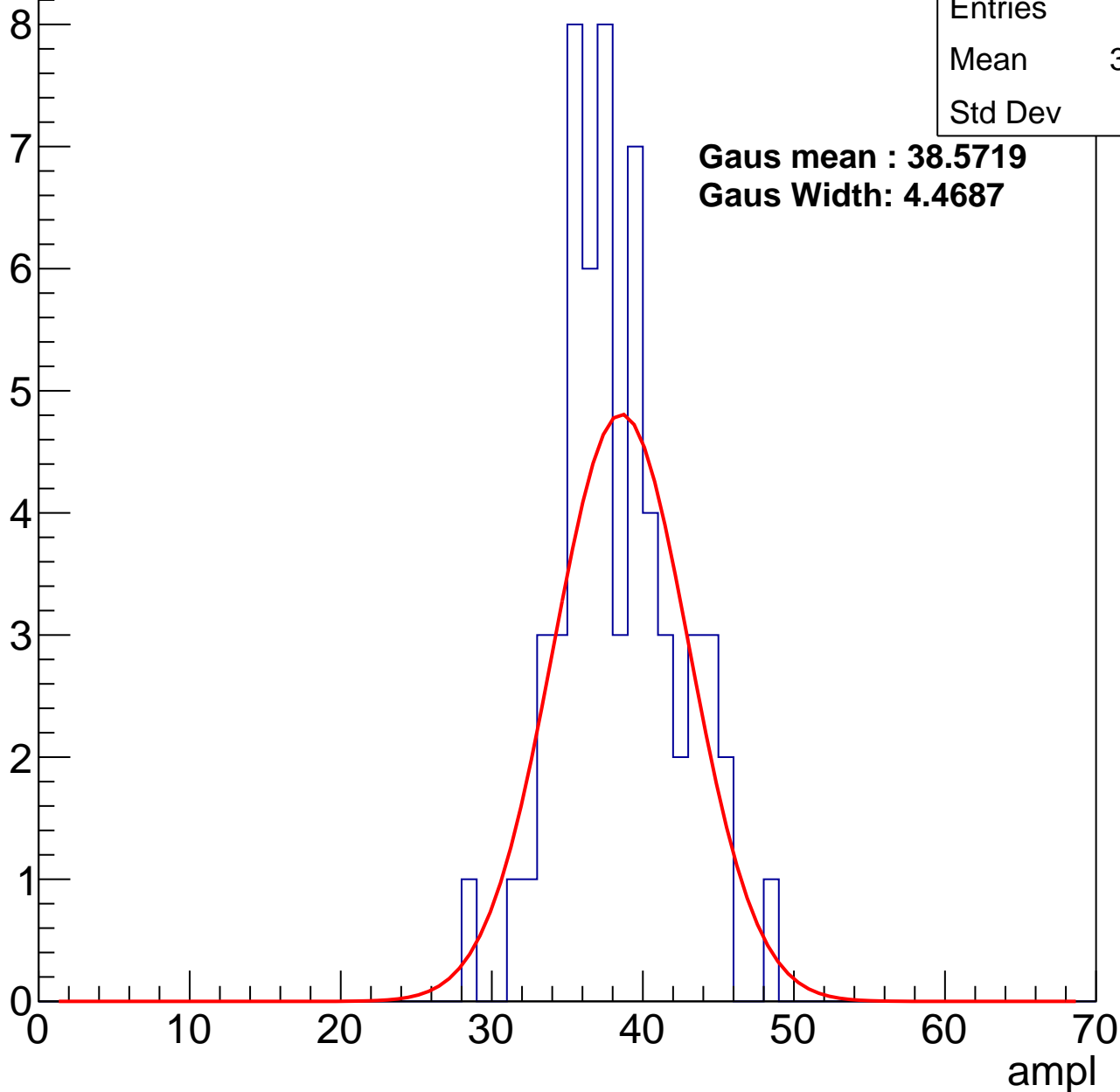
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	37.92
Std Dev	3.85

**Gaus mean : 38.5719**

**Gaus Width: 4.4687**



# B1L102S, U16-ch101, adc2

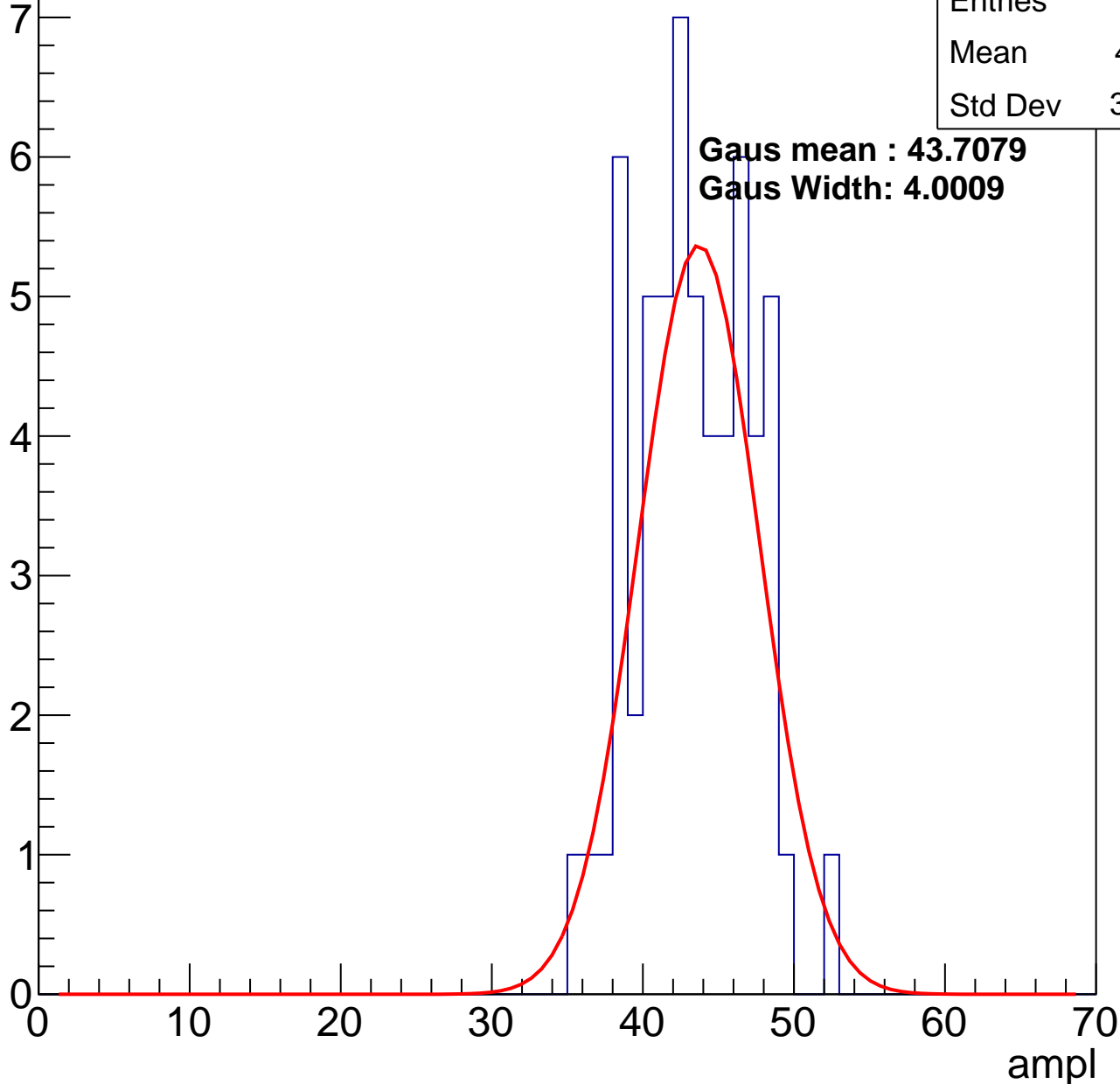
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	42.91
Std Dev	3.673

**Gaus mean : 43.7079**

**Gaus Width: 4.0009**

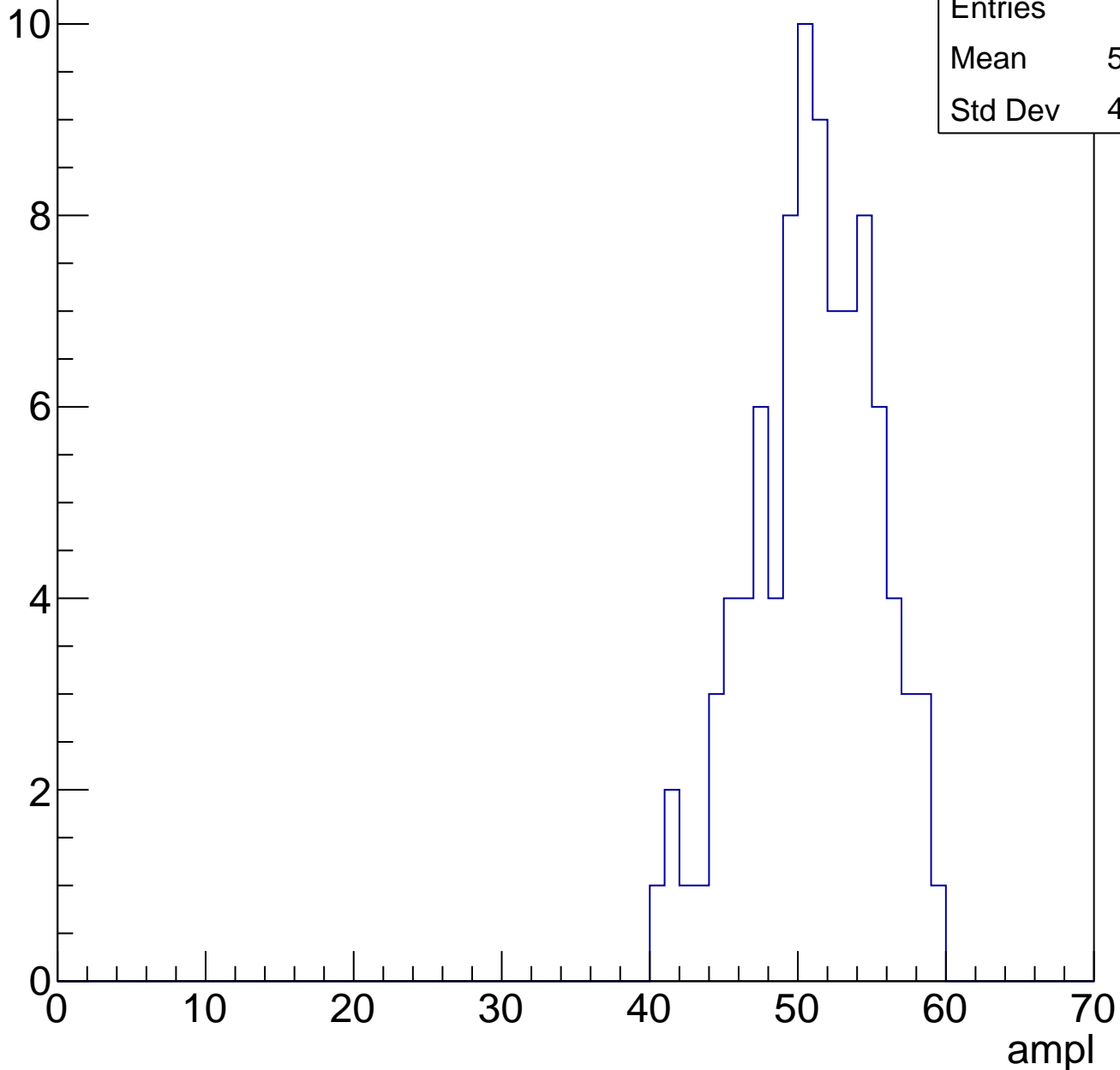


# B1L102S, U16-ch101, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	92
Mean	50.58
Std Dev	4.218

Entry

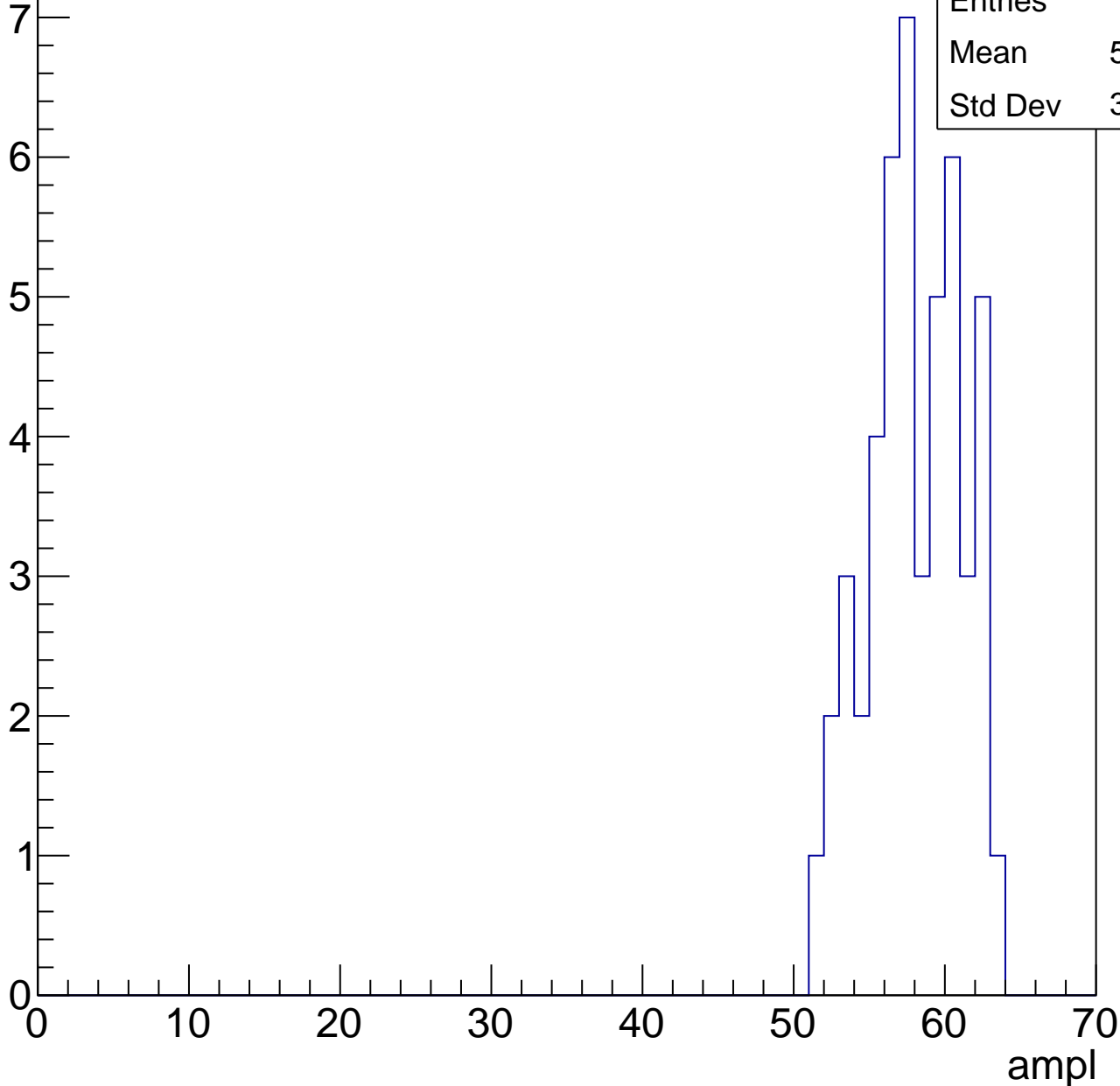


# B1L102S, U16-ch101, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	57.54
Std Dev	3.048

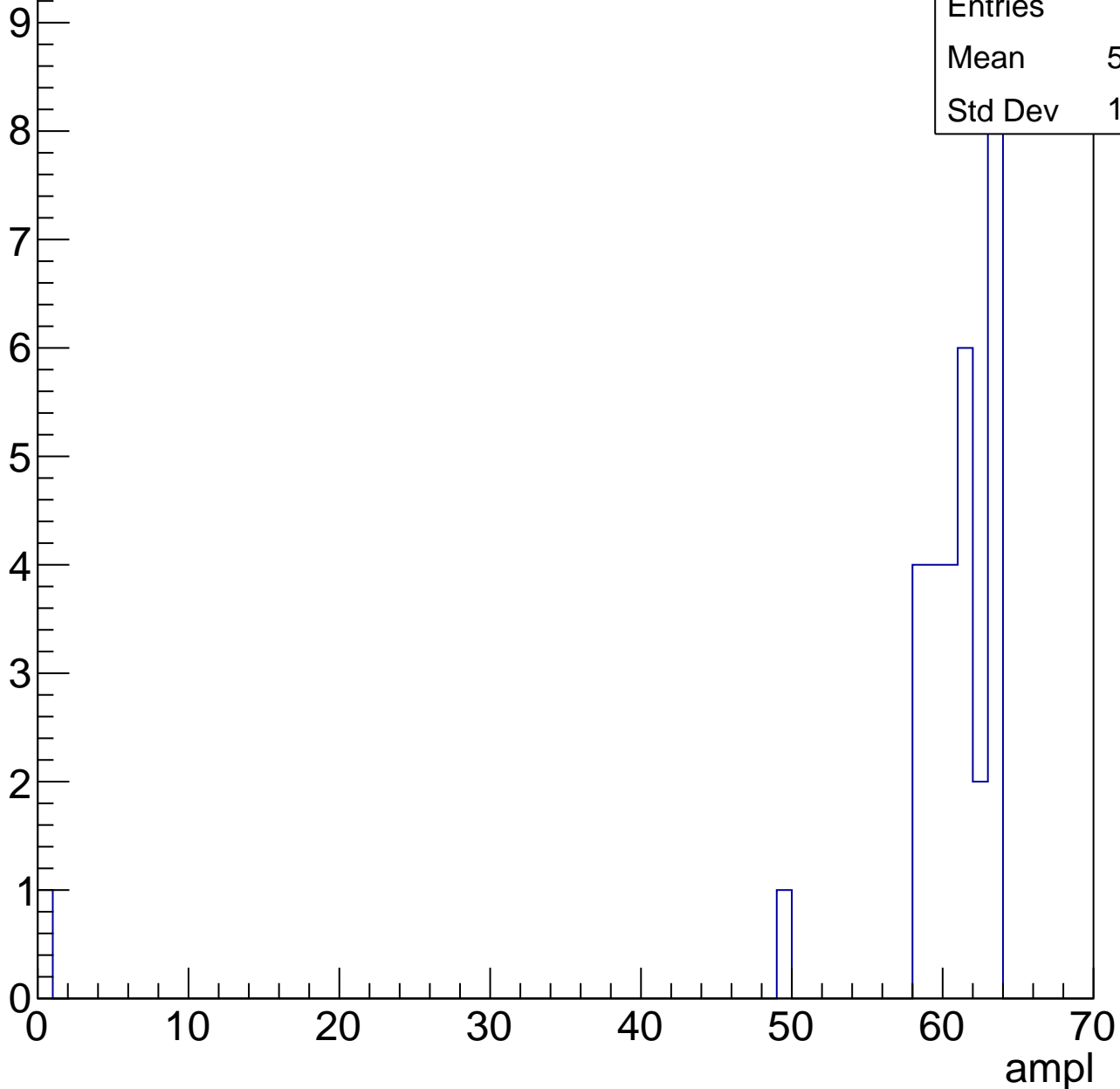


# B1L102S, U16-ch101, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

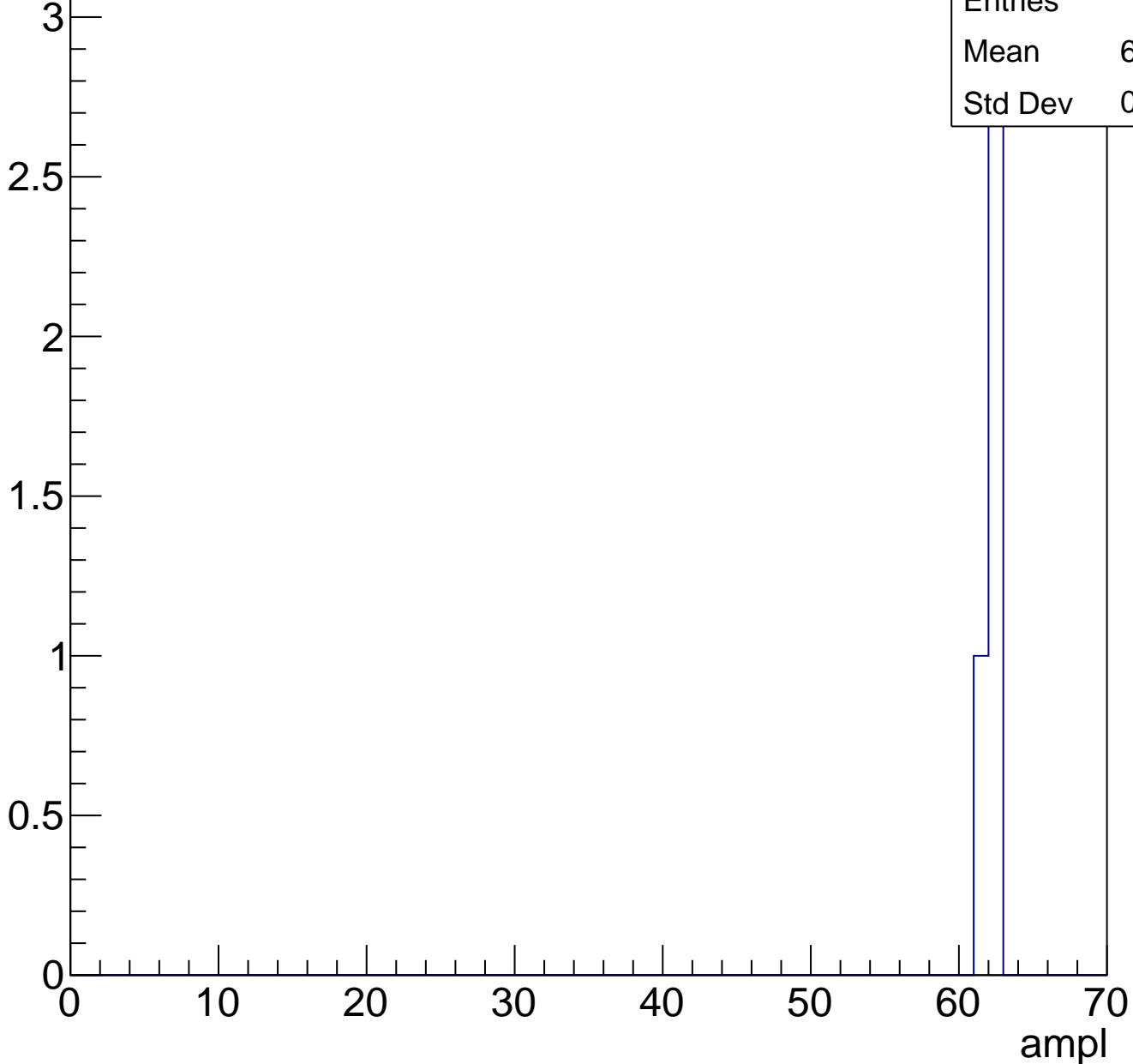
Entries	31
Mean	58.52
Std Dev	11.02



# B1L102S, U16-ch101, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	4
Mean	61.75
Std Dev	0.433



# B1L102S, U16-ch101, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch102, adc0

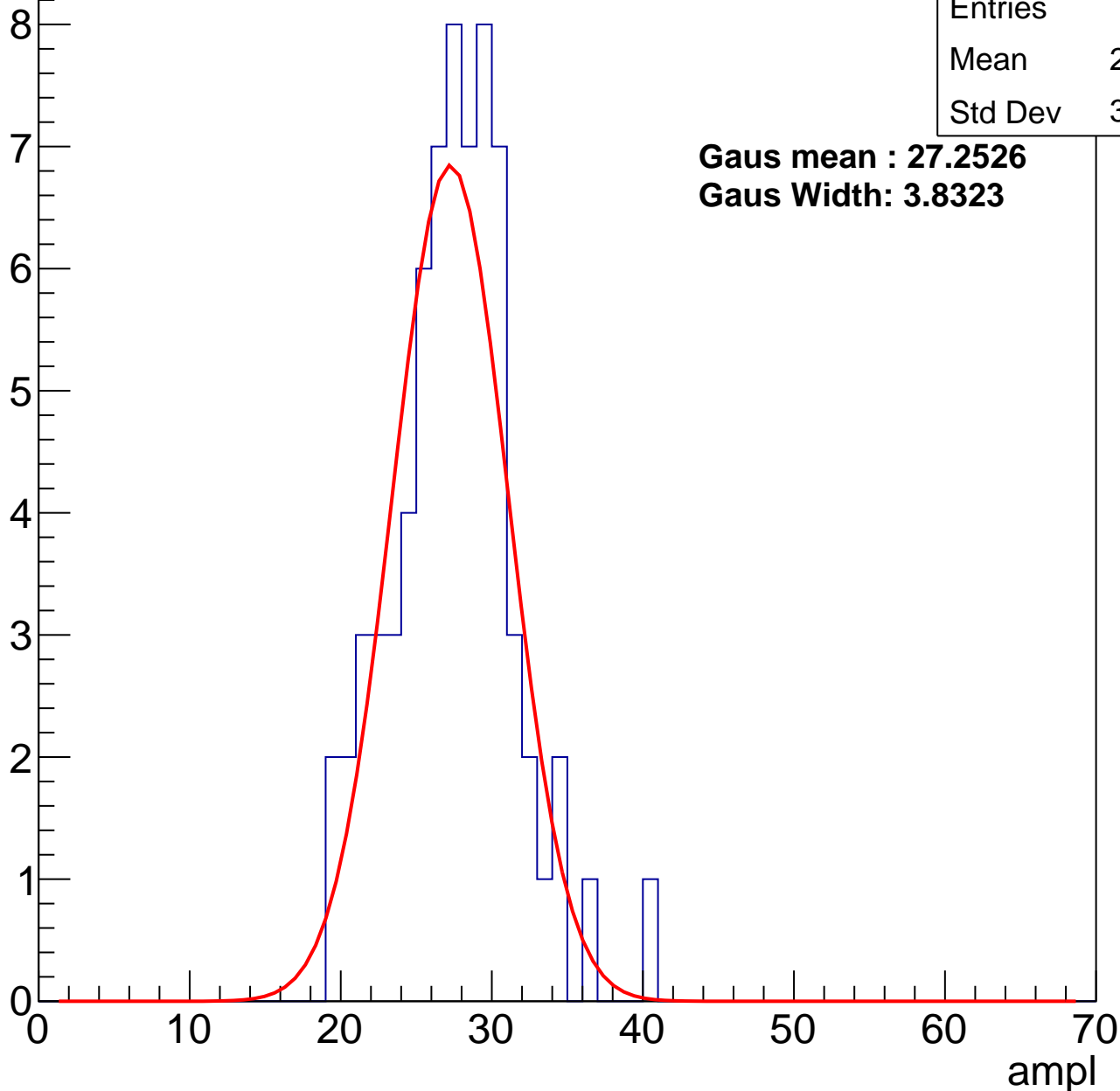
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	27.03
Std Dev	3.978

**Gaus mean : 27.2526**

**Gaus Width: 3.8323**



# B1L102S, U16-ch102, adc1

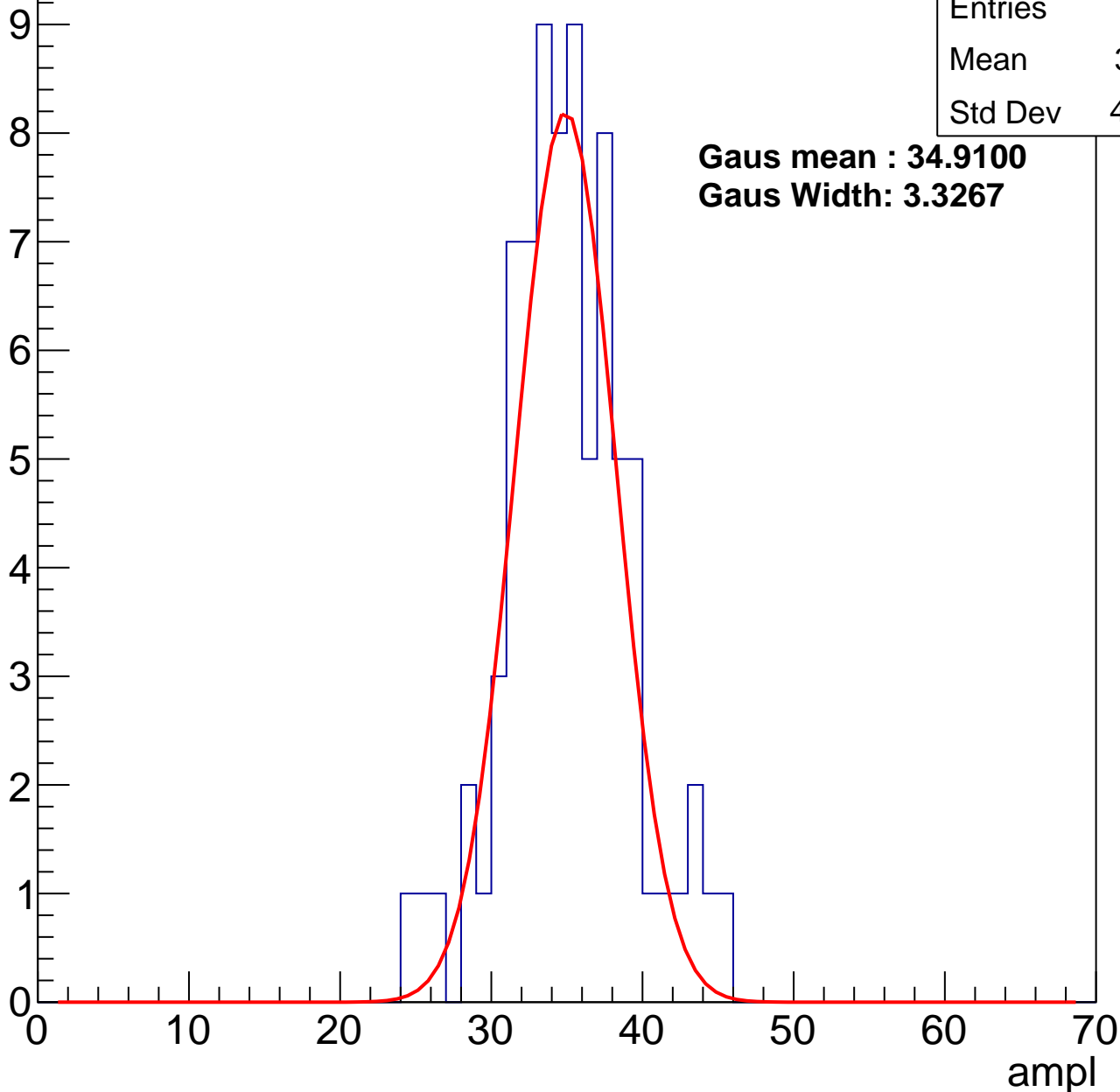
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	34.61
Std Dev	4.055

**Gaus mean : 34.9100**

**Gaus Width: 3.3267**



# B1L102S, U16-ch102, adc2

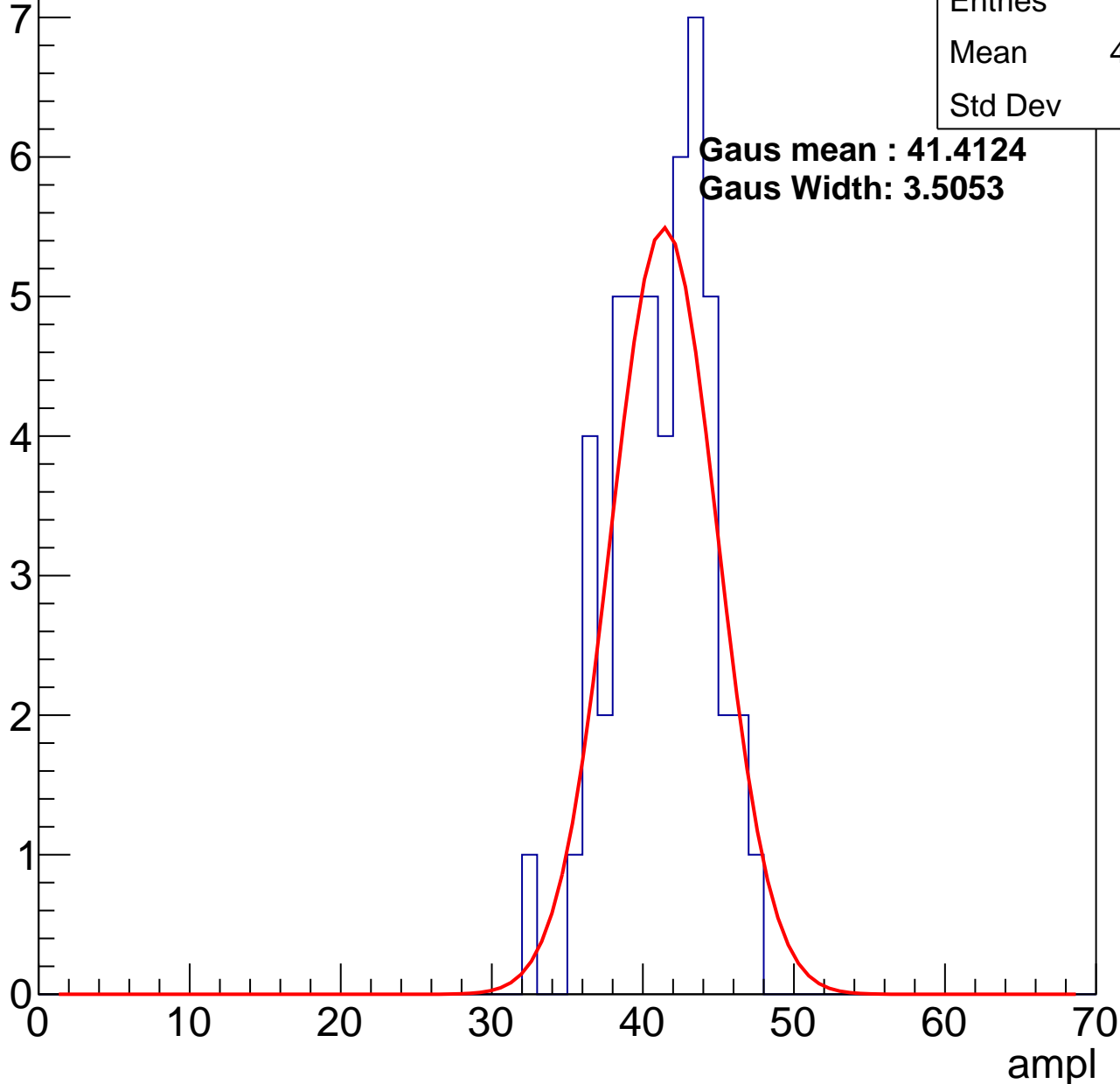
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	50
Mean	40.72
Std Dev	3.2

**Gaus mean : 41.4124**

**Gaus Width: 3.5053**

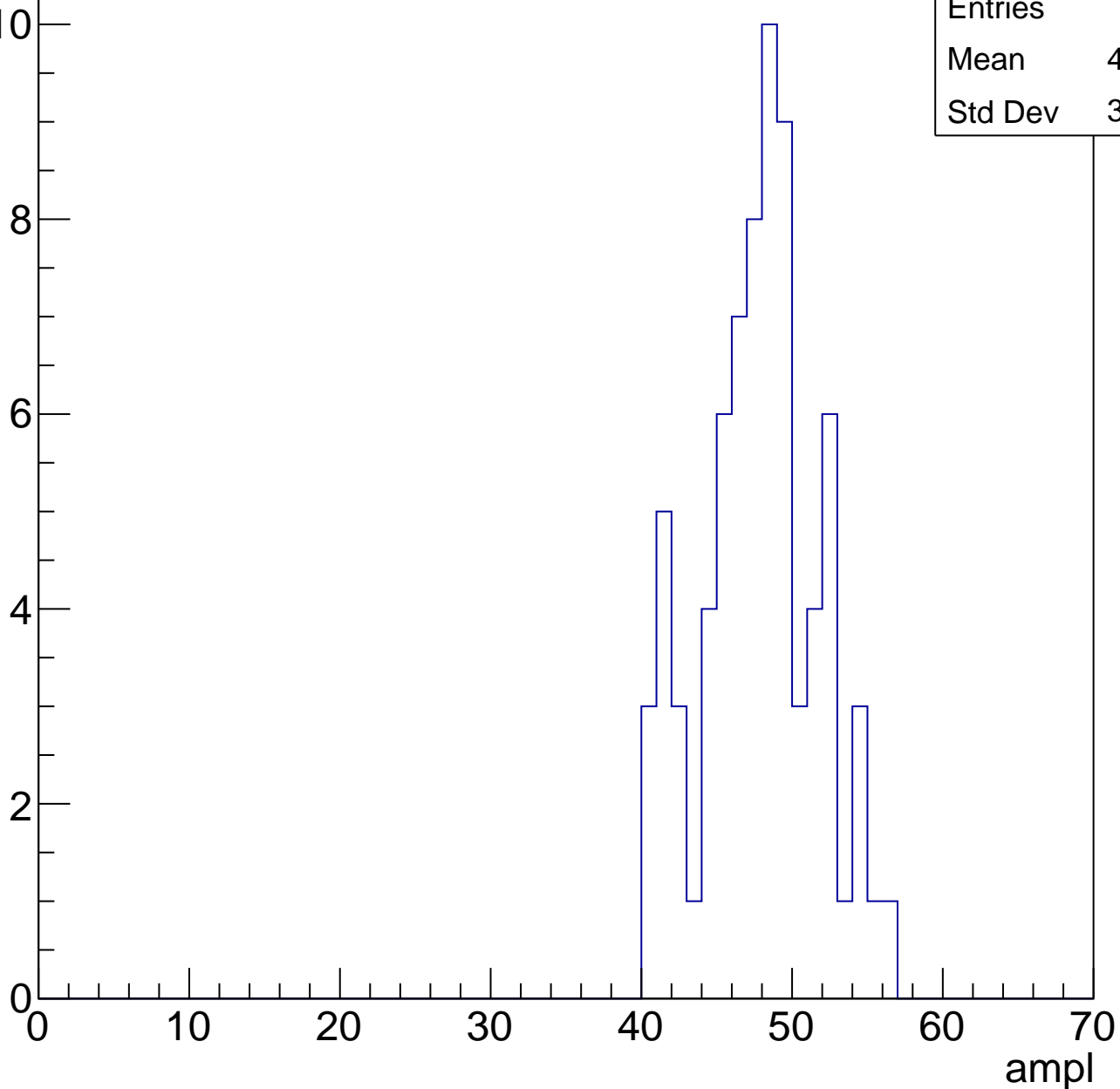


# B1L102S, U16-ch102, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	47.35
Std Dev	3.814

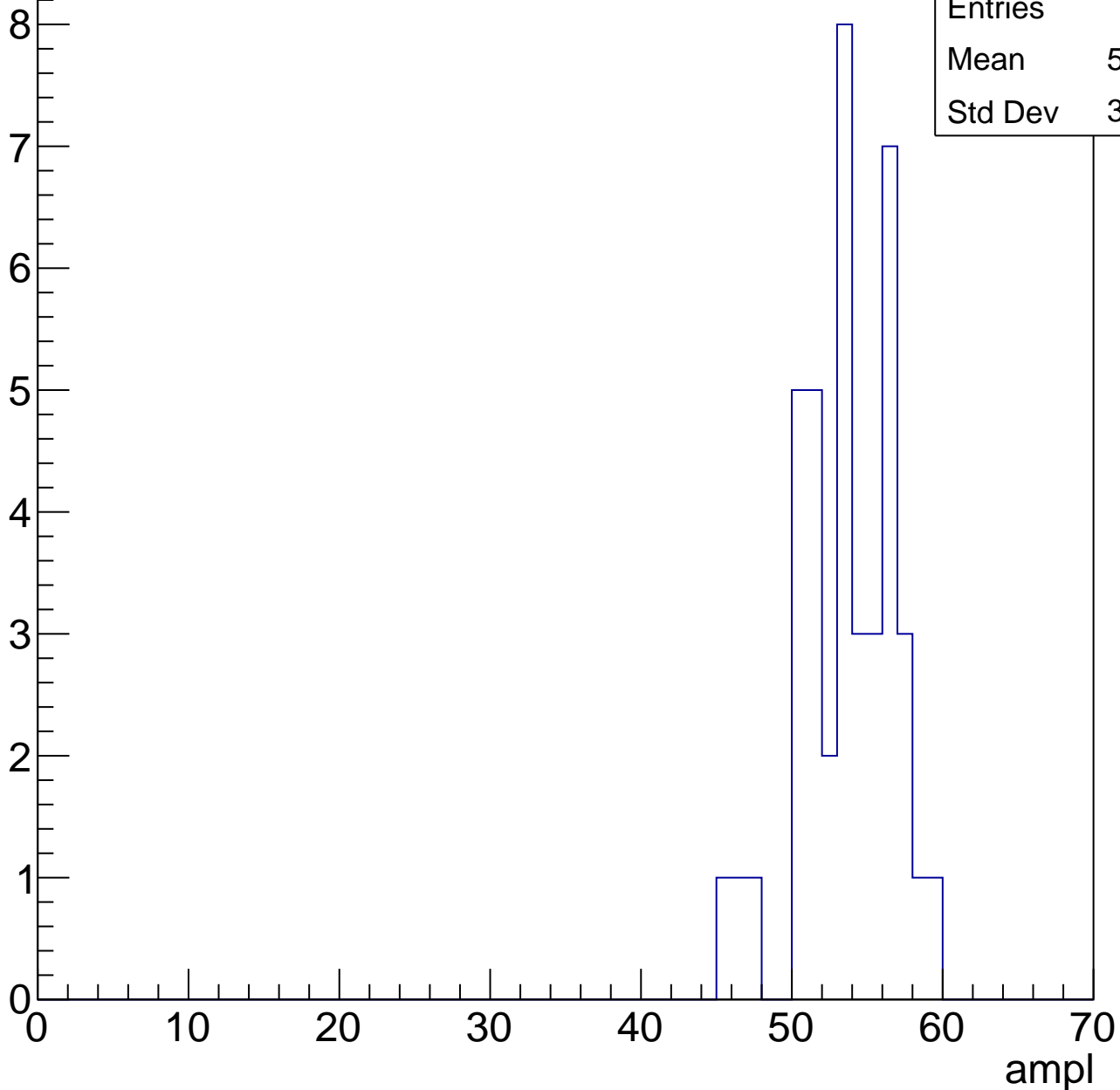


# B1L102S, U16-ch102, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	41
Mean	53.12
Std Dev	3.133

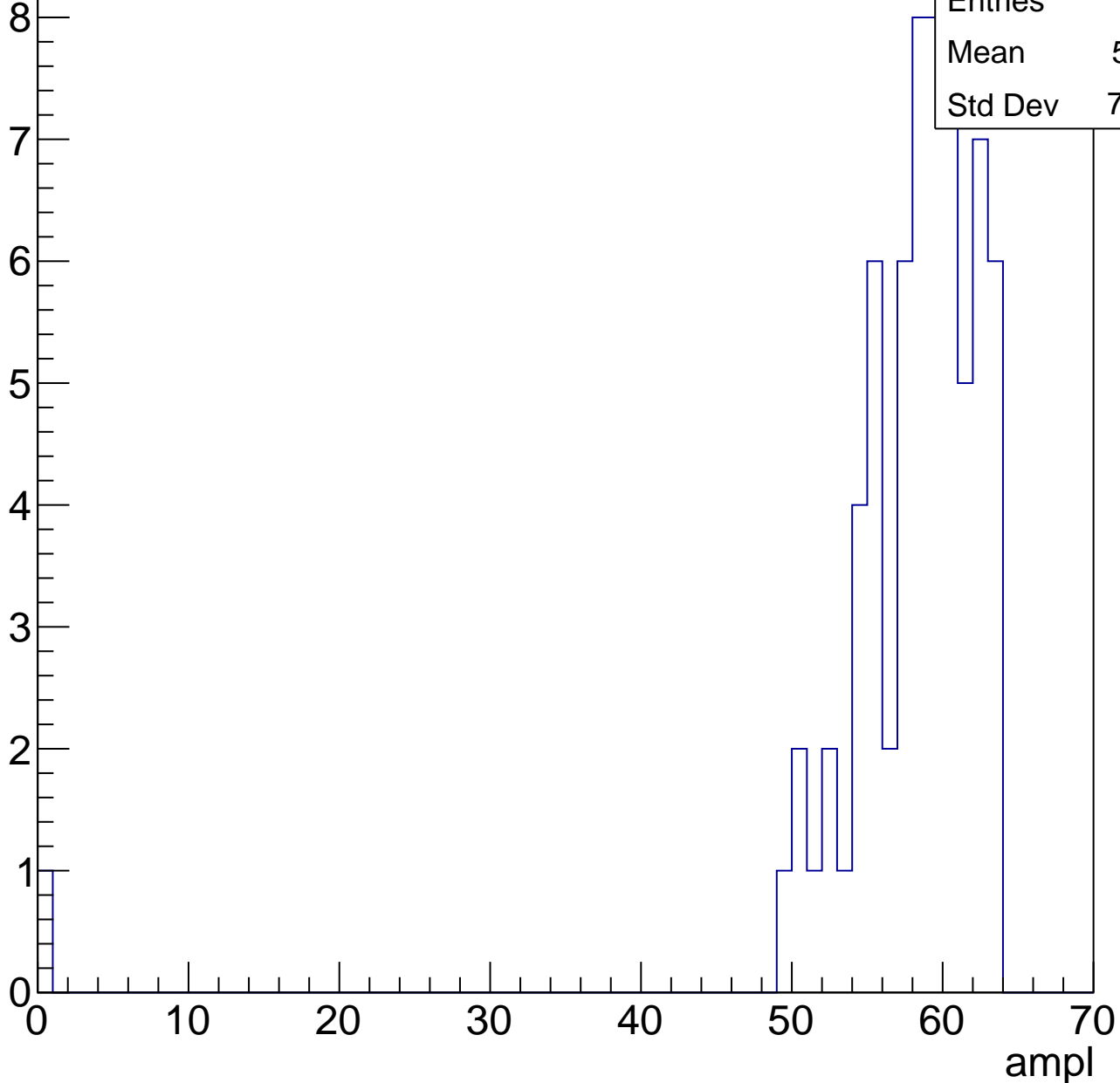


# B1L102S, U16-ch102, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

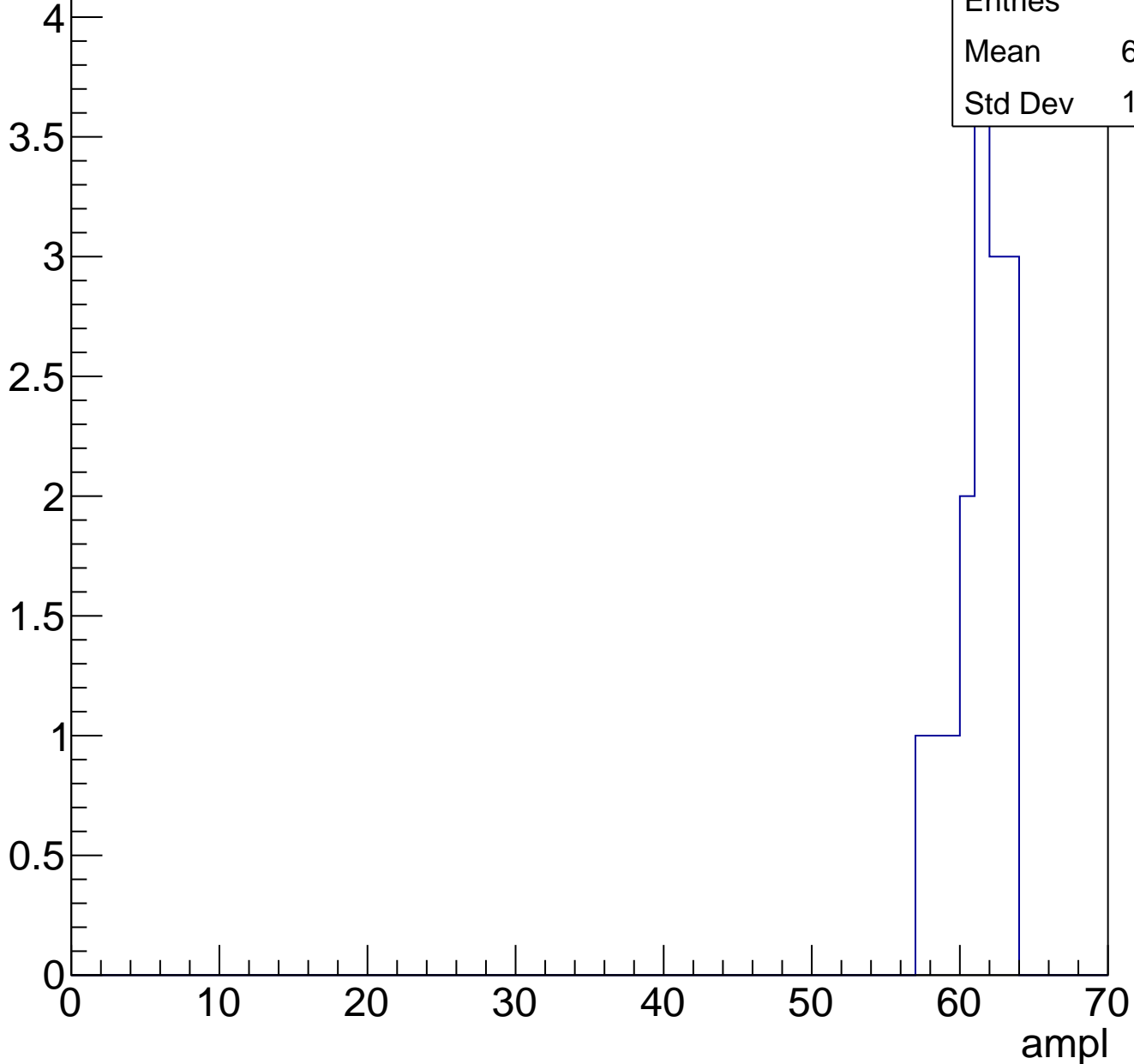
Entries	68
Mean	57.21
Std Dev	7.817



# B1L102S, U16-ch102, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch102, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch103, adc0

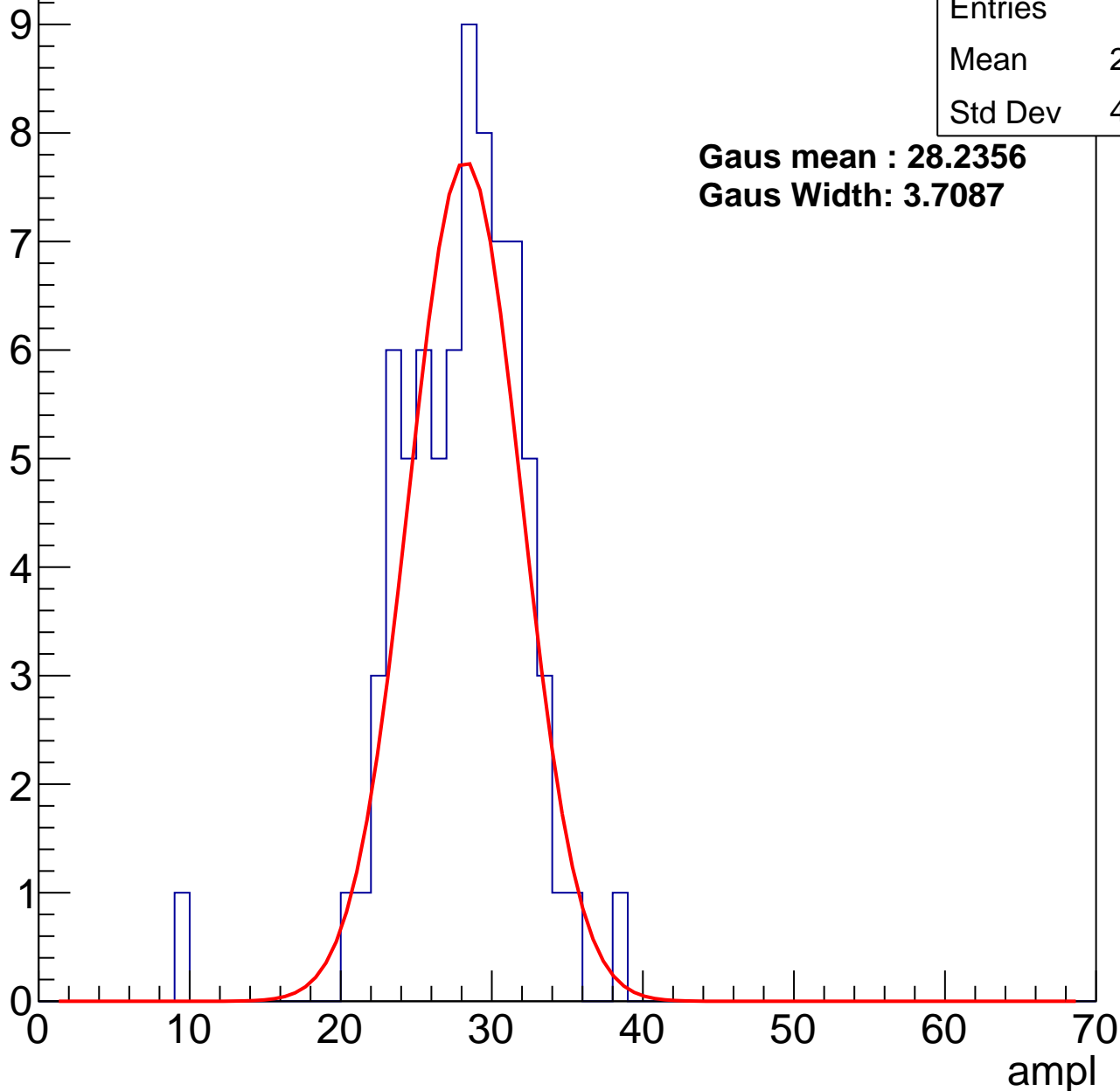
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	27.54
Std Dev	4.159

**Gaus mean : 28.2356**

**Gaus Width: 3.7087**



# B1L102S, U16-ch103, adc1

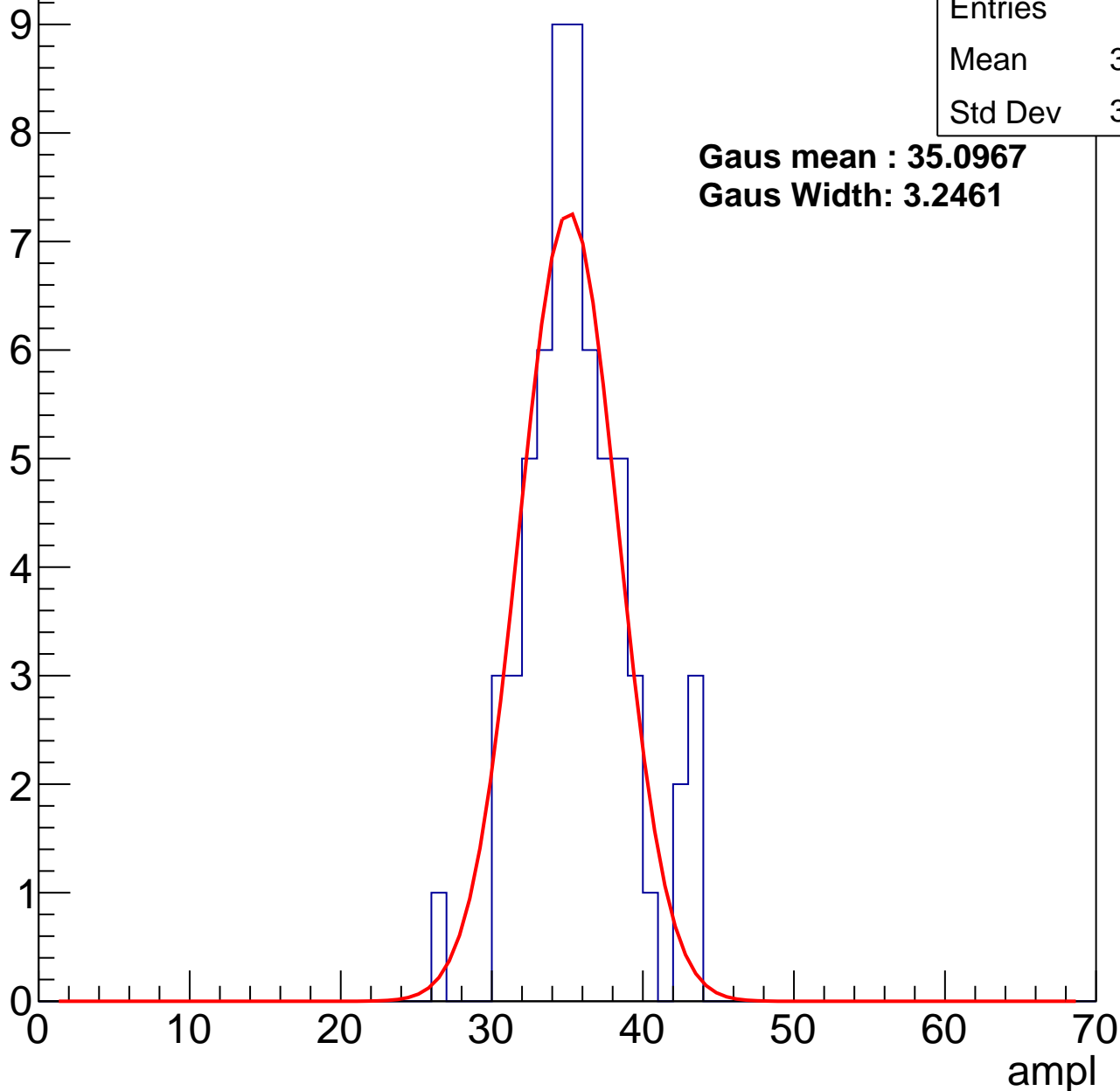
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	35.23
Std Dev	3.418

**Gaus mean : 35.0967**

**Gaus Width: 3.2461**



# B1L102S, U16-ch103, adc2

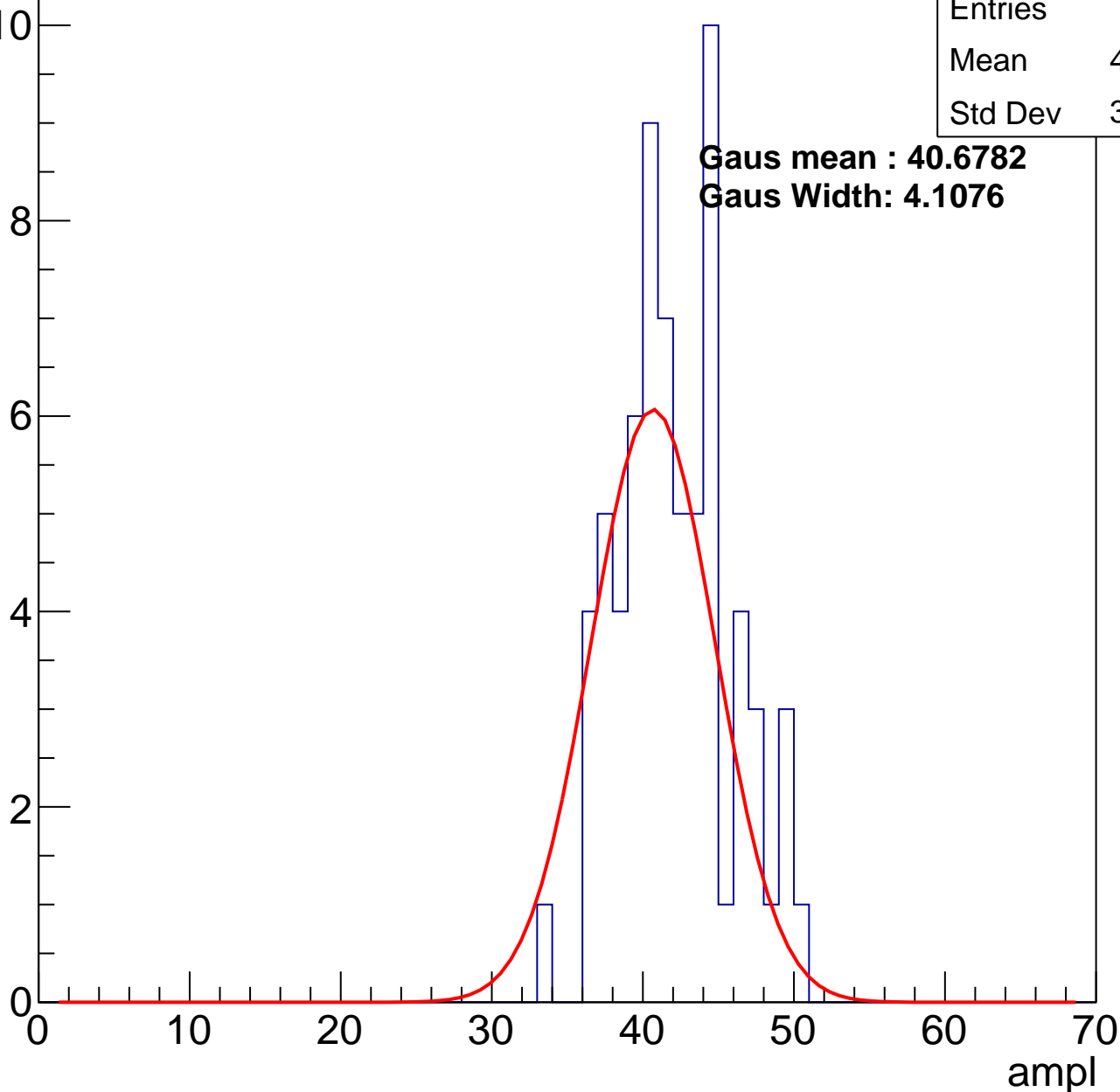
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	41.67
Std Dev	3.697

**Gaus mean : 40.6782**

**Gaus Width: 4.1076**

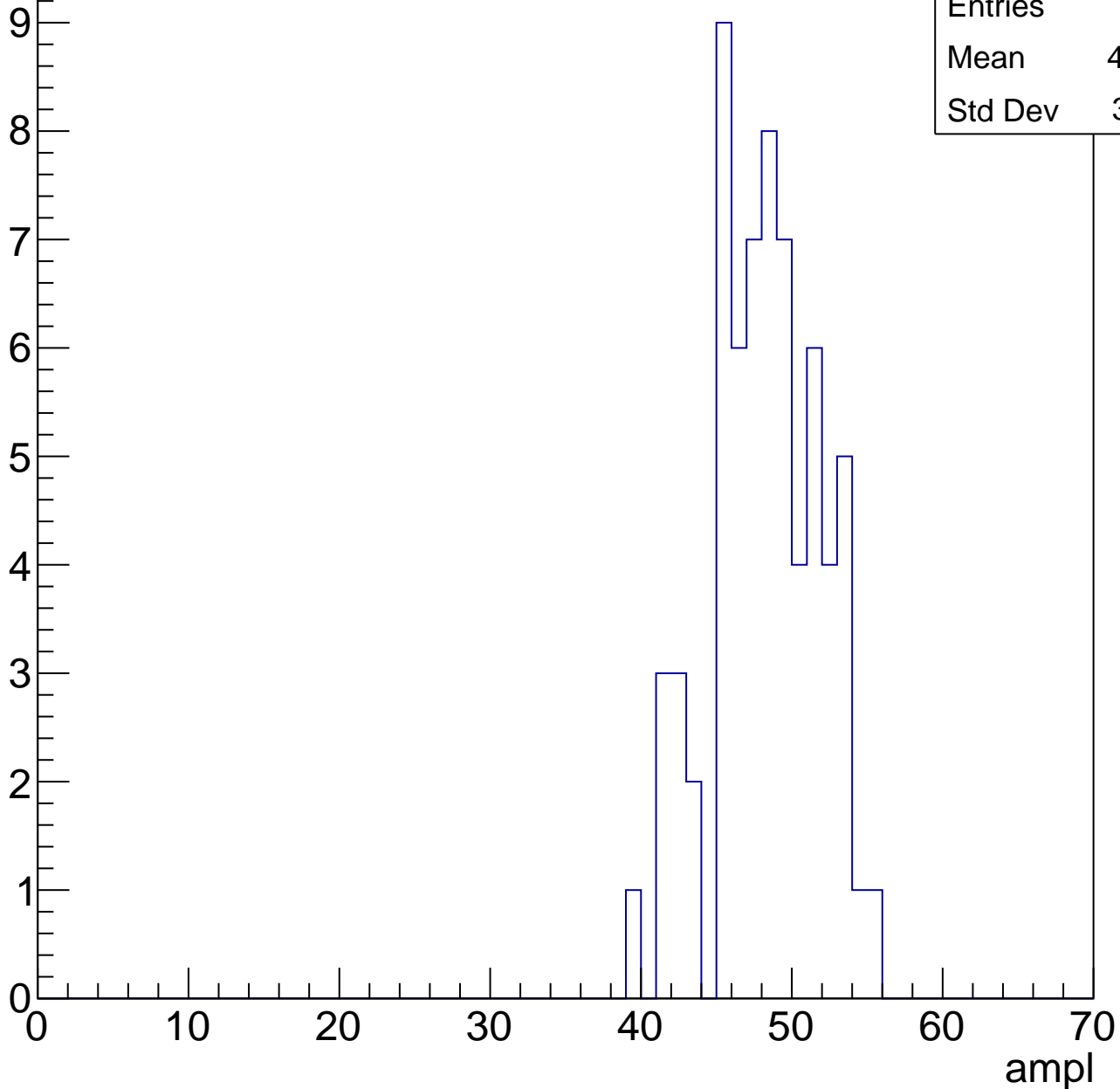


# B1L102S, U16-ch103, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	47.75
Std Dev	3.551

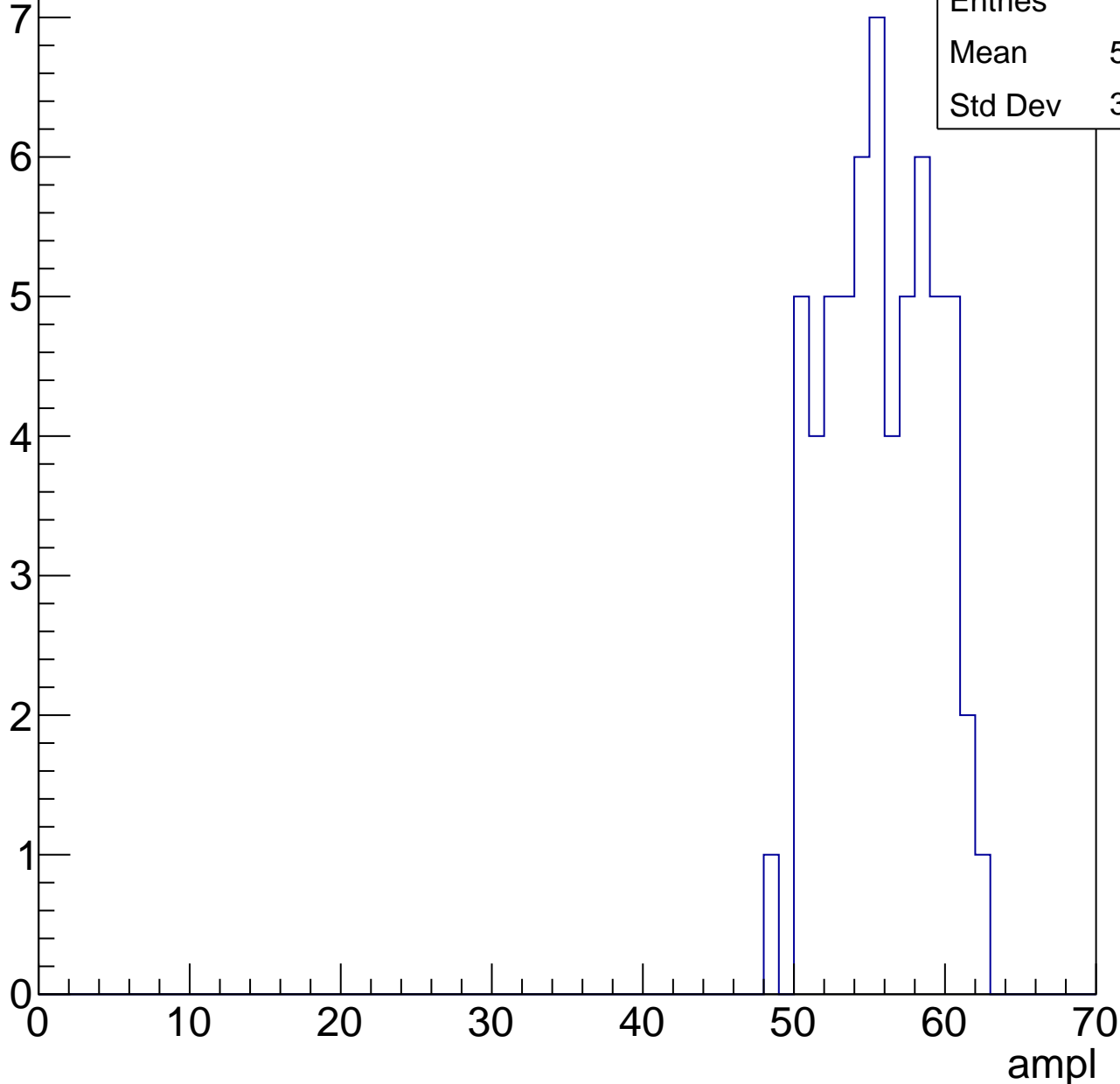


# B1L102S, U16-ch103, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	55.28
Std Dev	3.407

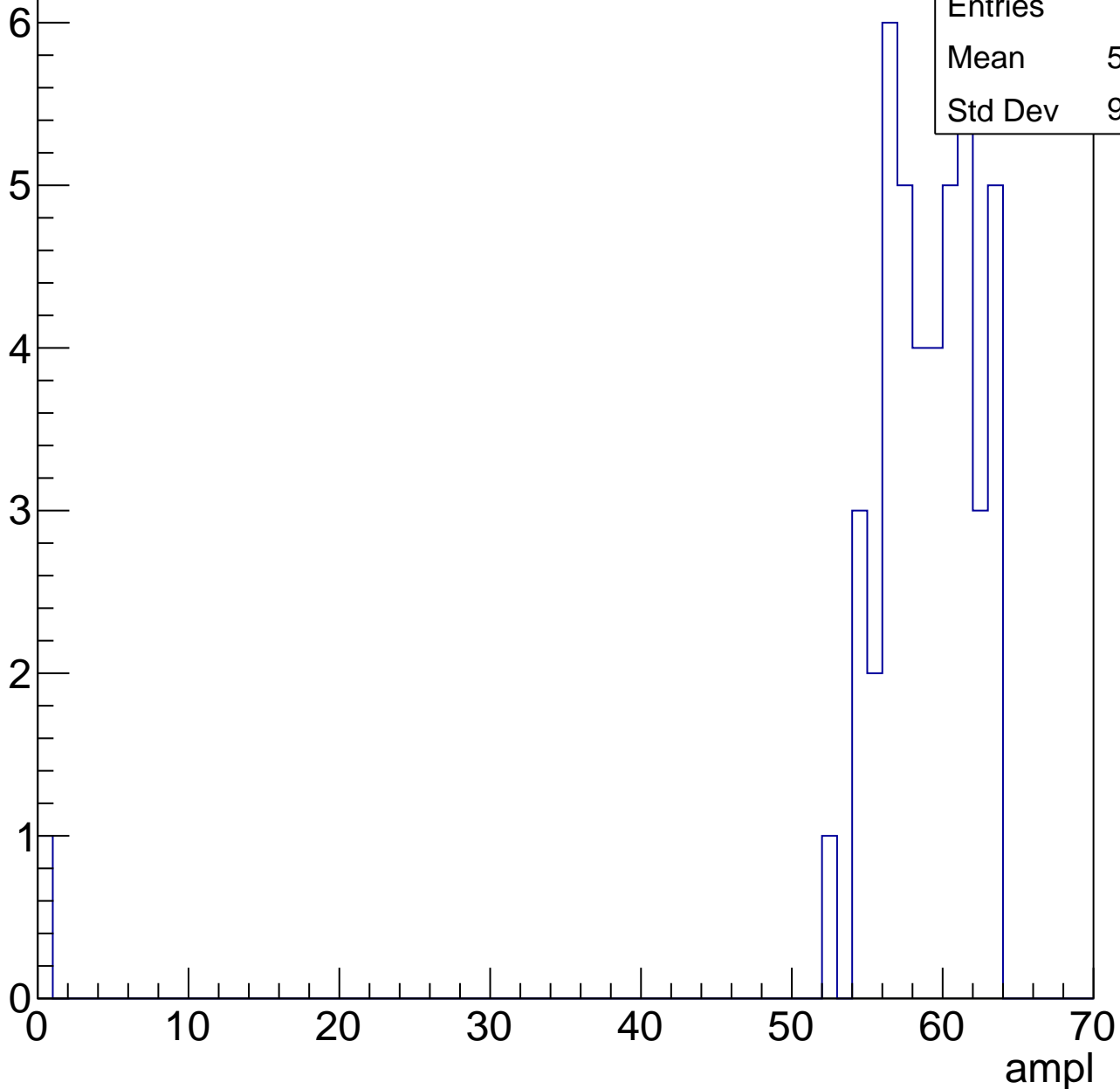


# B1L102S, U16-ch103, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	57.33
Std Dev	9.099

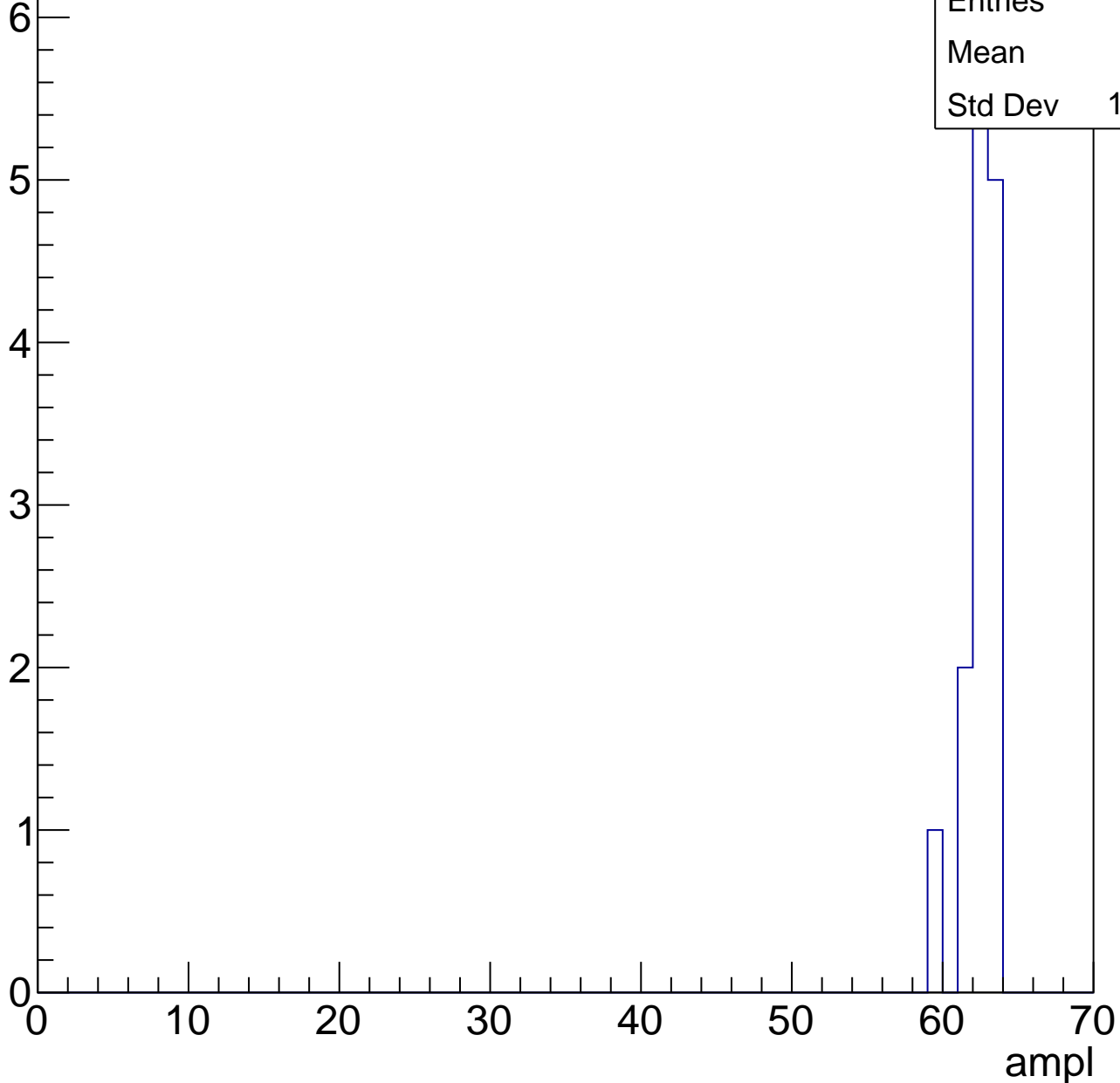


# B1L102S, U16-ch103, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	14
Mean	62
Std Dev	1.069





# B1L102S, U16-ch103, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U16-ch104, adc0

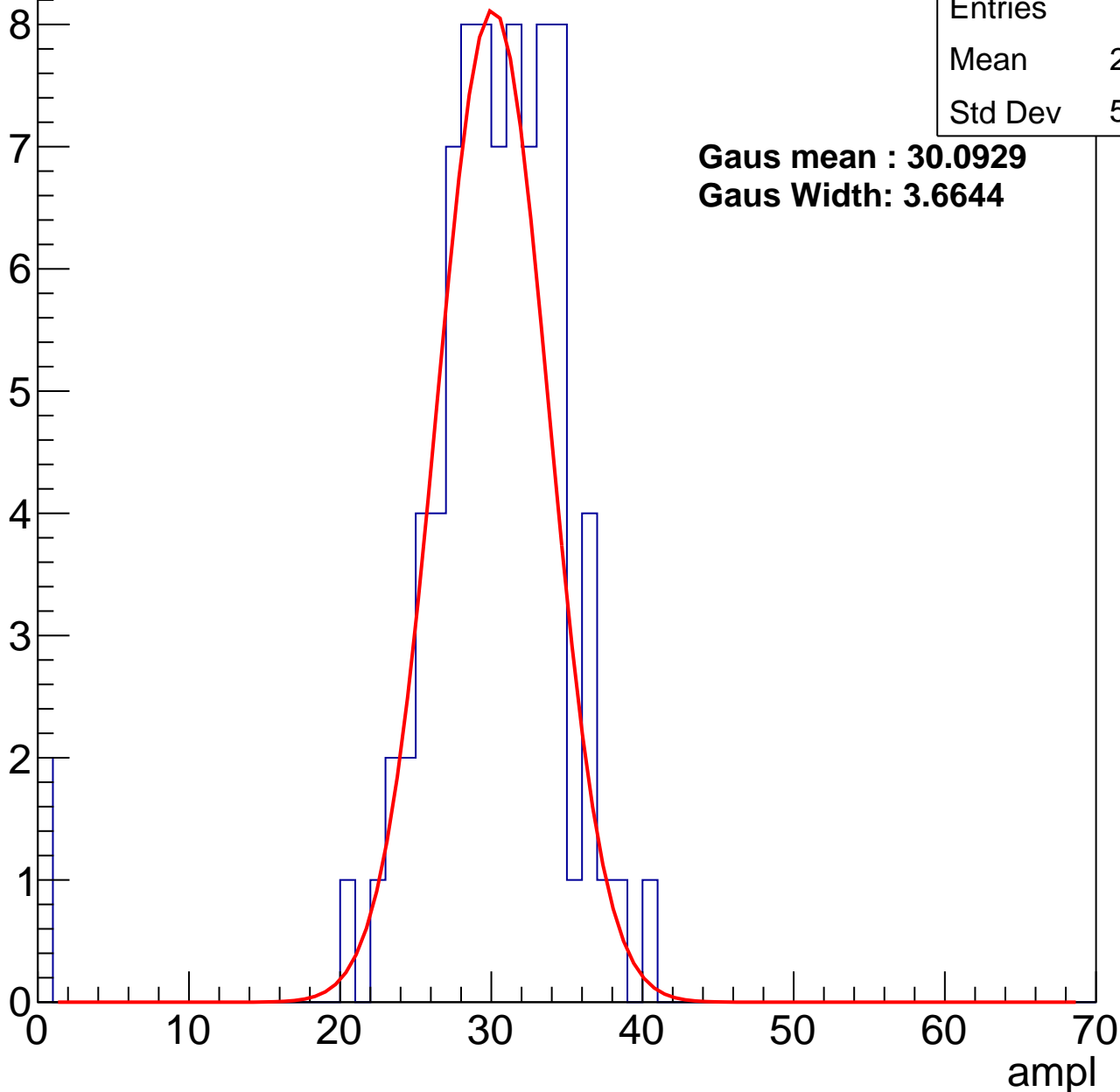
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	85
Mean	29.38
Std Dev	5.927

**Gaus mean : 30.0929**

**Gaus Width: 3.6644**



# B1L102S, U16-ch104, adc1

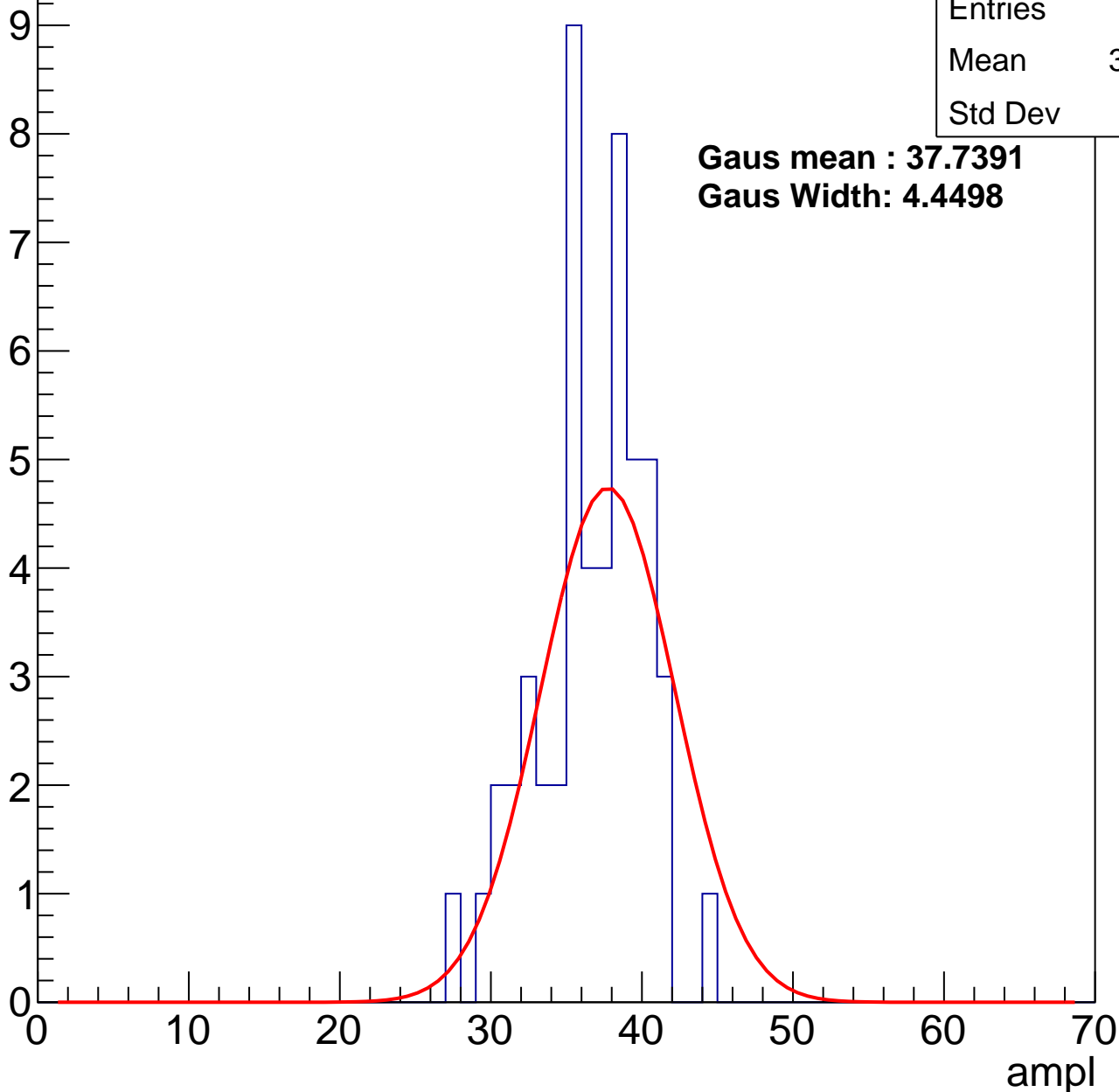
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	36.17
Std Dev	3.49

**Gaus mean : 37.7391**

**Gaus Width: 4.4498**



# B1L102S, U16-ch104, adc2

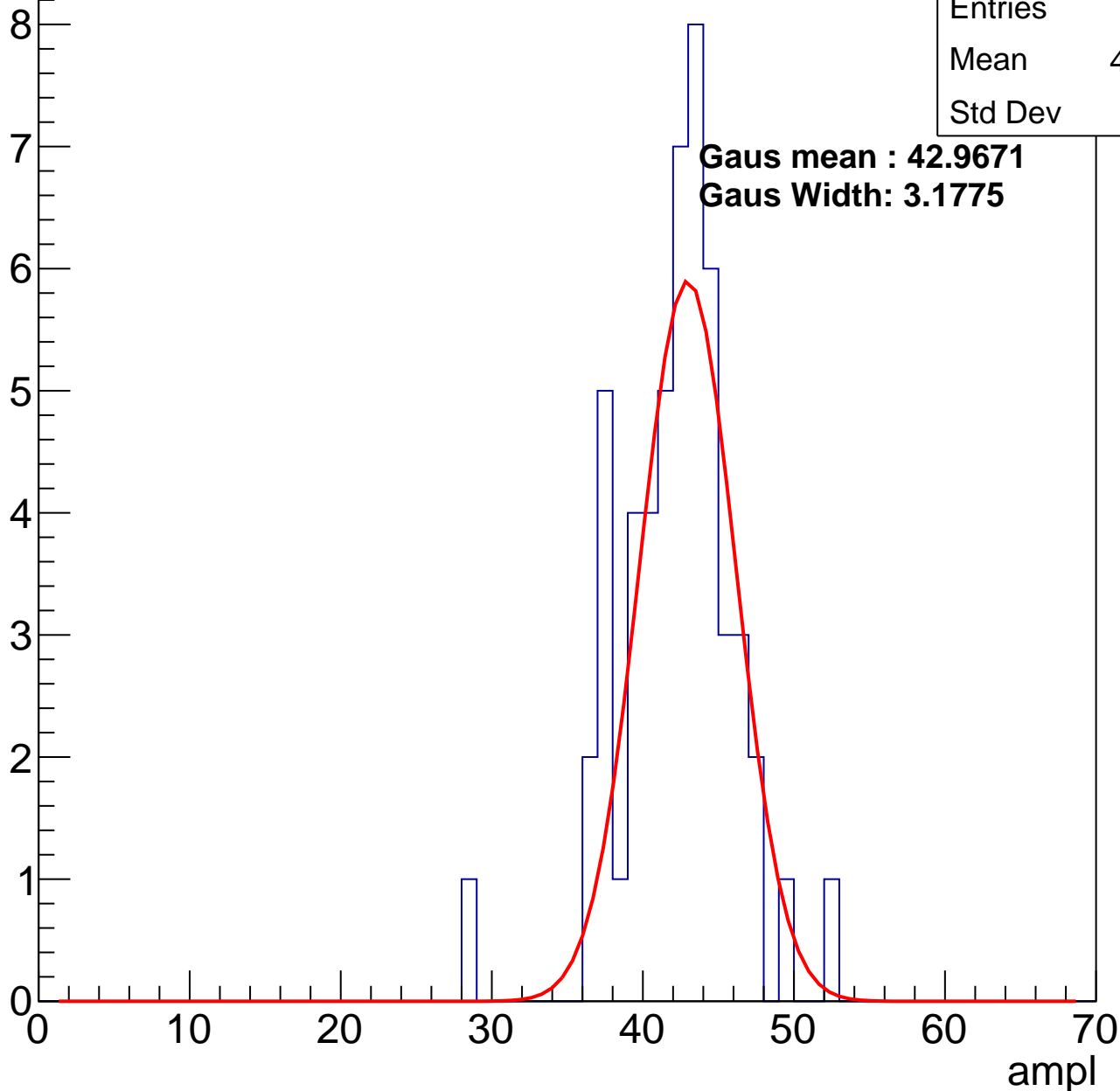
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	53
Mean	41.77
Std Dev	3.81

**Gaus mean : 42.9671**

**Gaus Width: 3.1775**

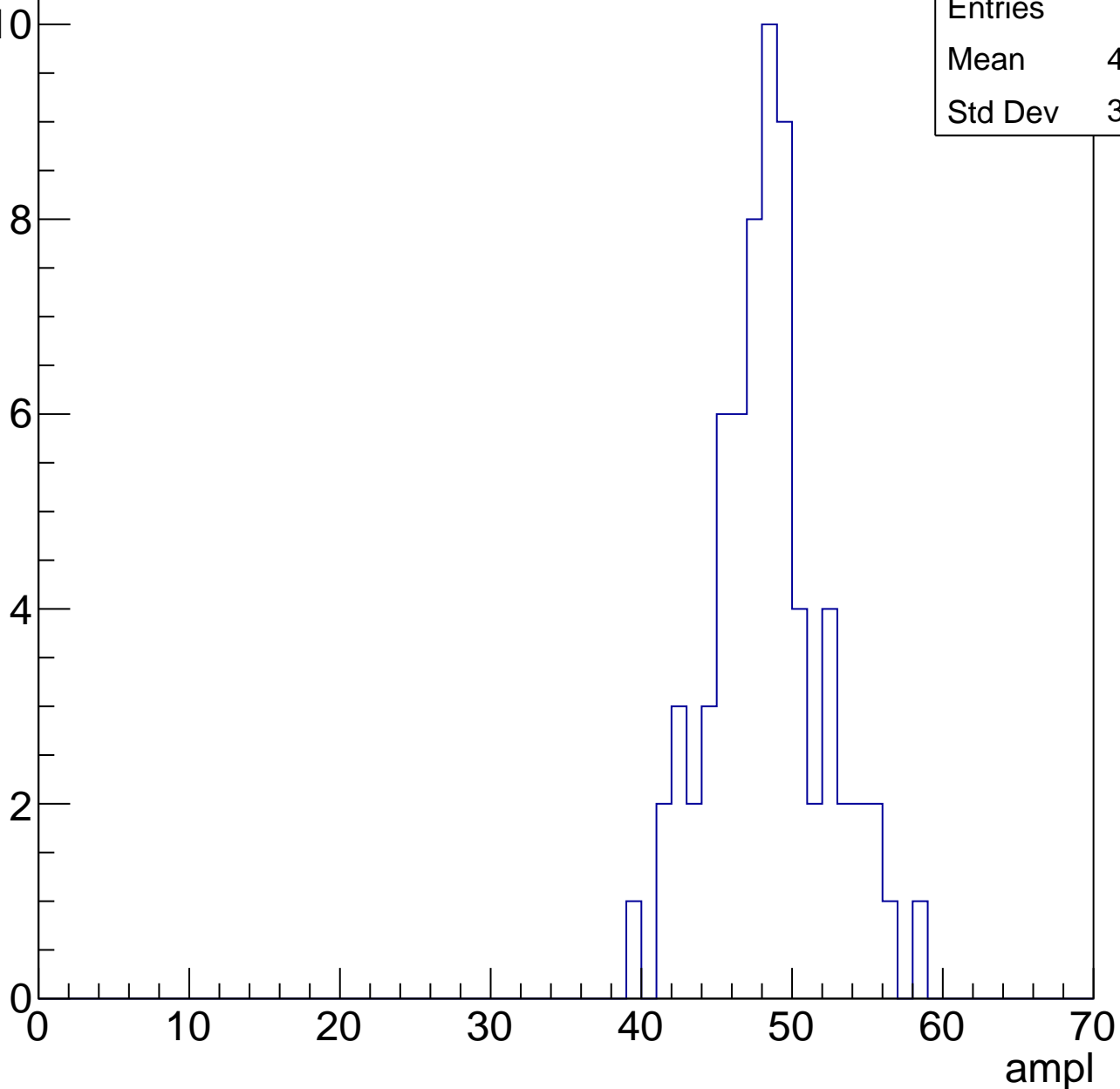


# B1L102S, U16-ch104, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	47.88
Std Dev	3.759

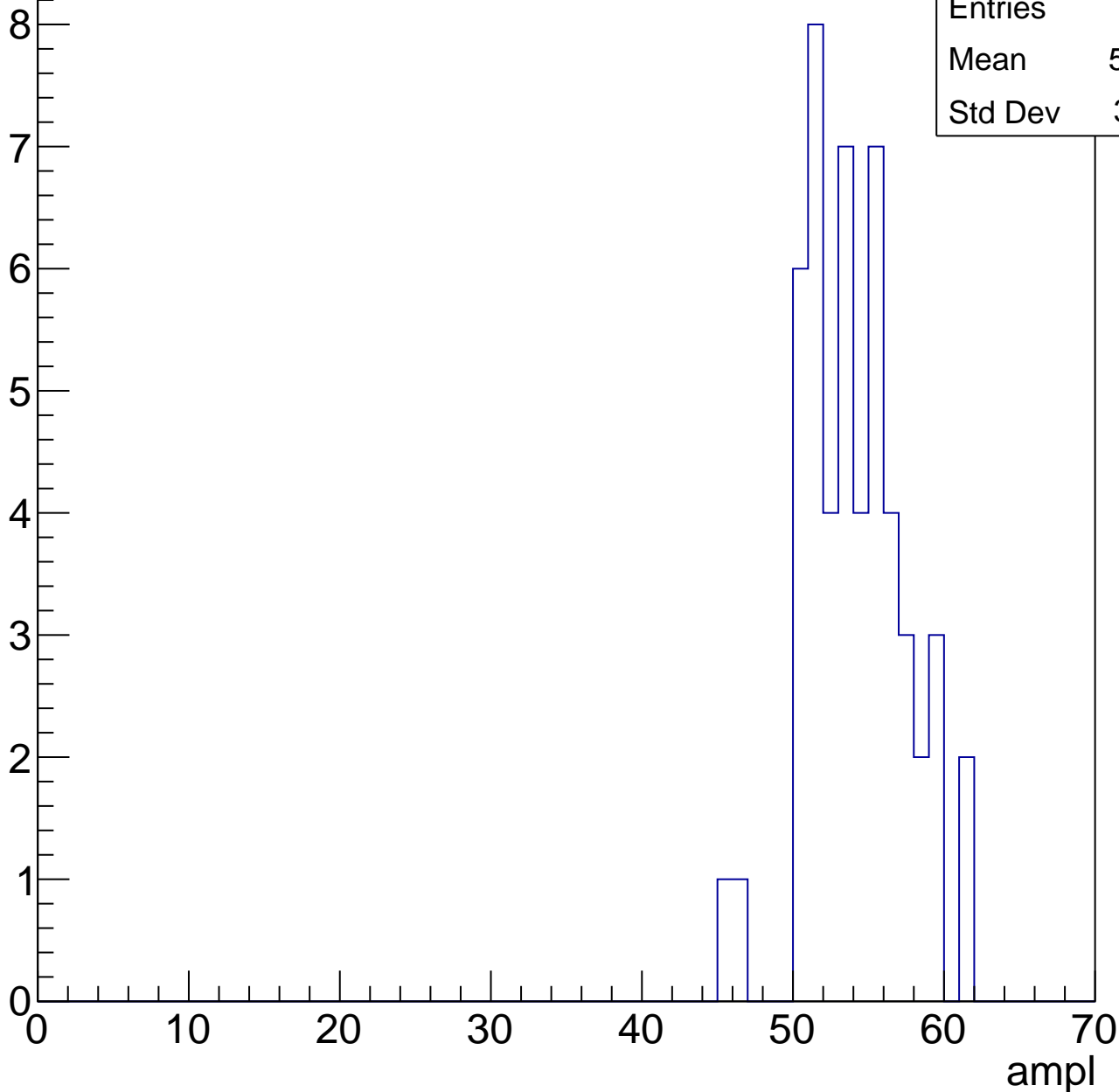


# B1L102S, U16-ch104, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	53.63
Std Dev	3.351

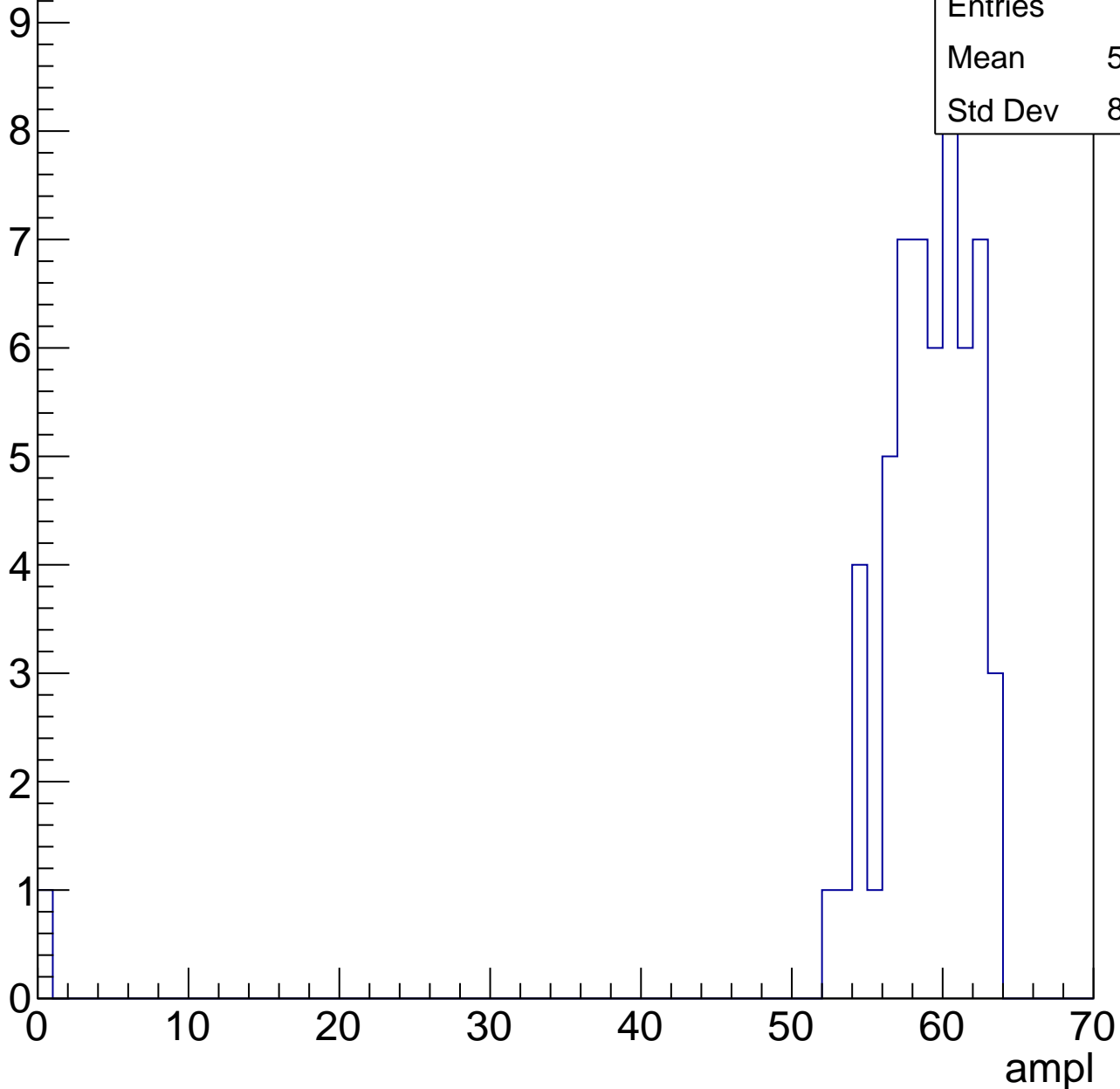


# B1L102S, U16-ch104, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	57.66
Std Dev	8.095

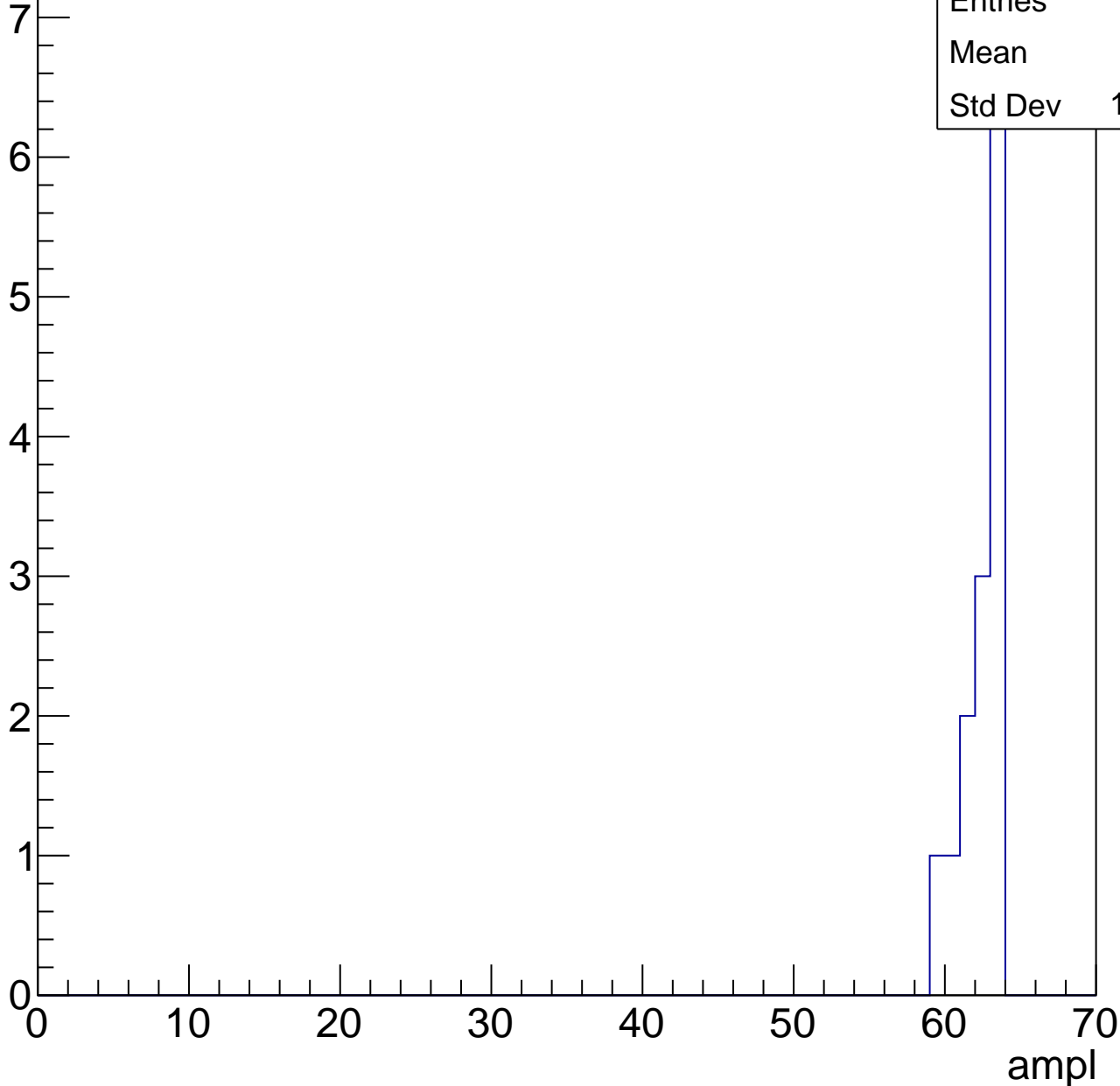


# B1L102S, U16-ch104, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	14
Mean	62
Std Dev	1.254





# B1L102S, U16-ch104, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U16-ch105, adc0

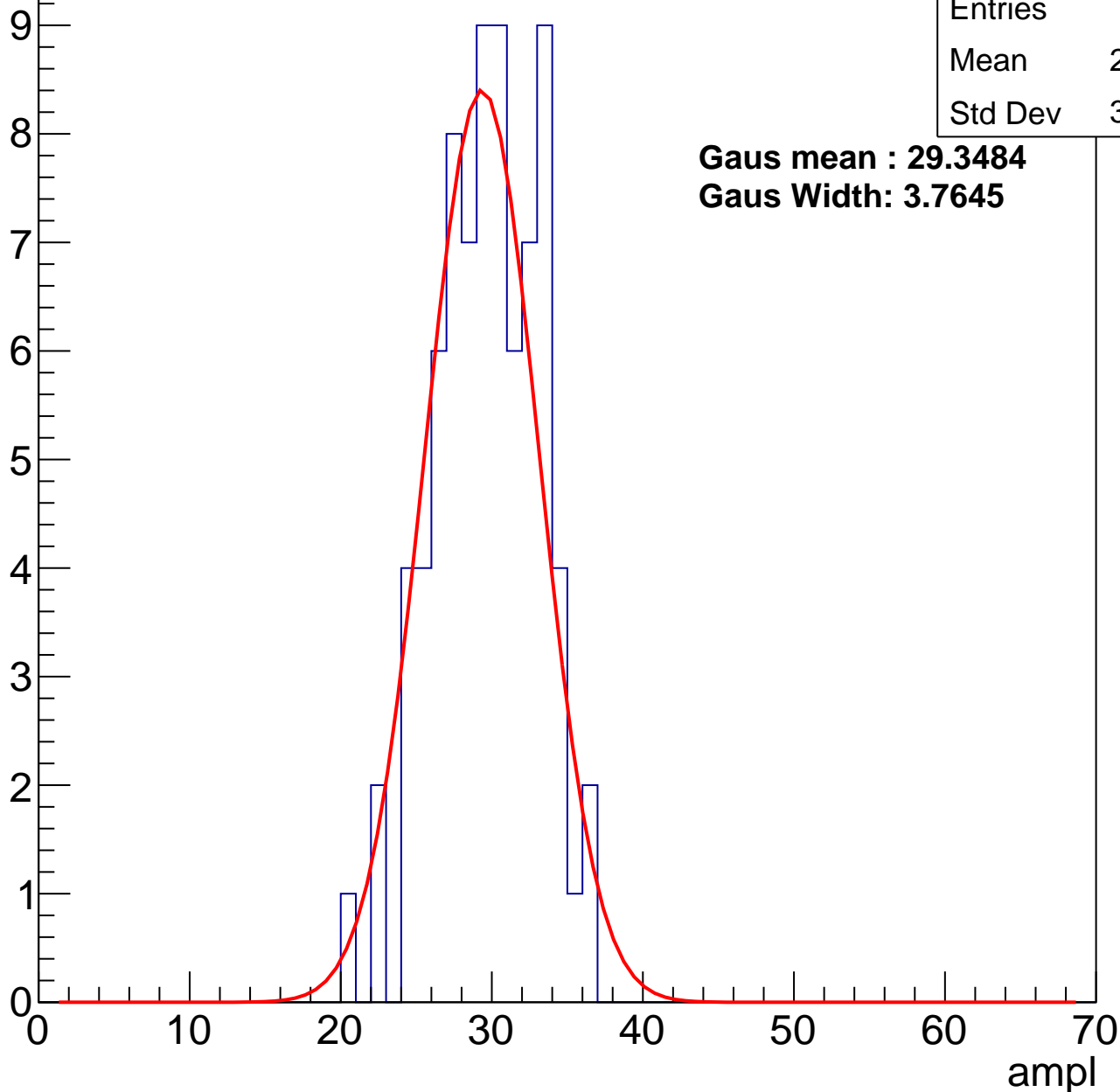
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	79
Mean	29.23
Std Dev	3.386

**Gaus mean : 29.3484**

**Gaus Width: 3.7645**



# B1L102S, U16-ch105, adc1

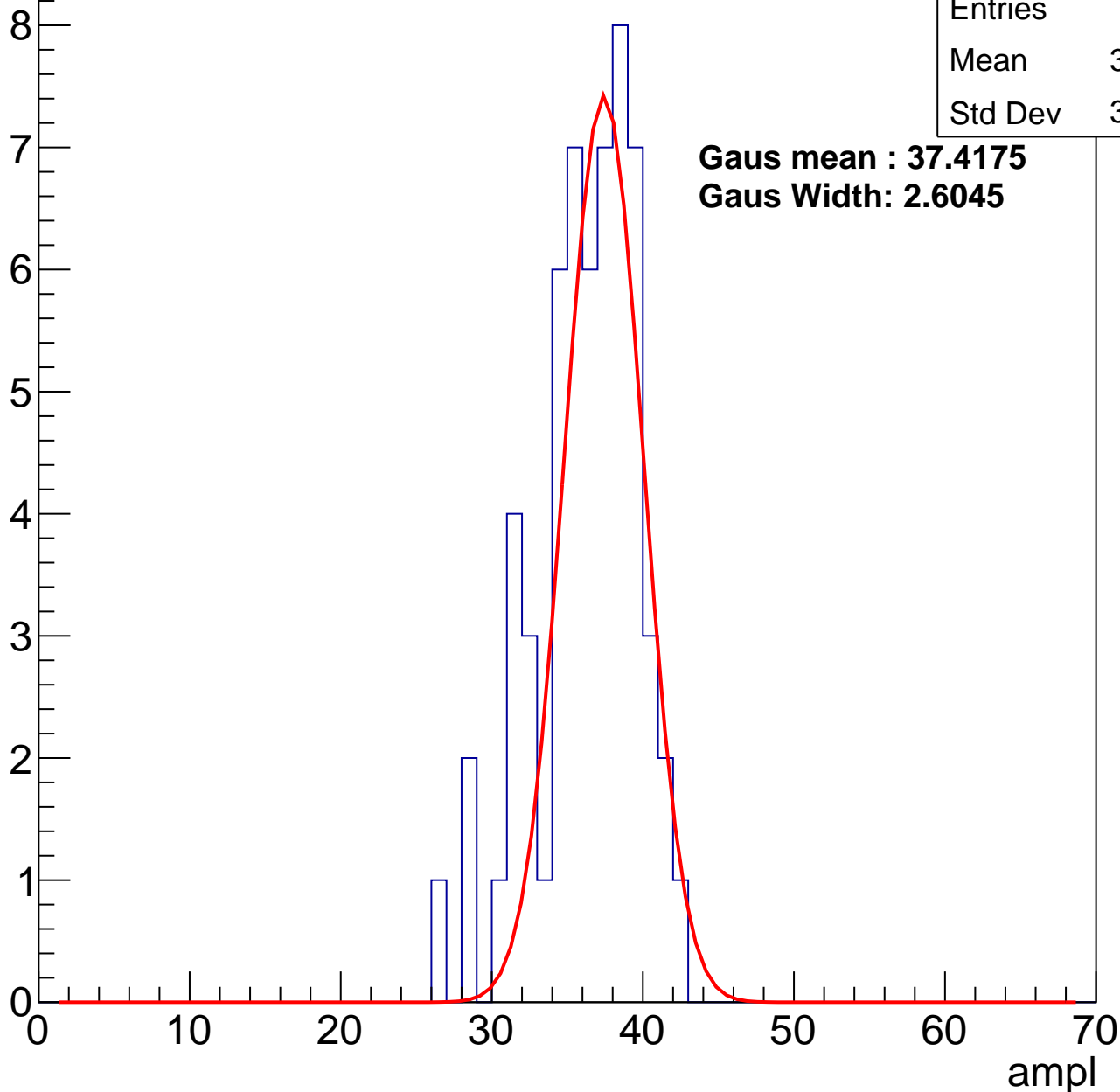
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	35.76
Std Dev	3.407

**Gaus mean : 37.4175**

**Gaus Width: 2.6045**



# B1L102S, U16-ch105, adc2

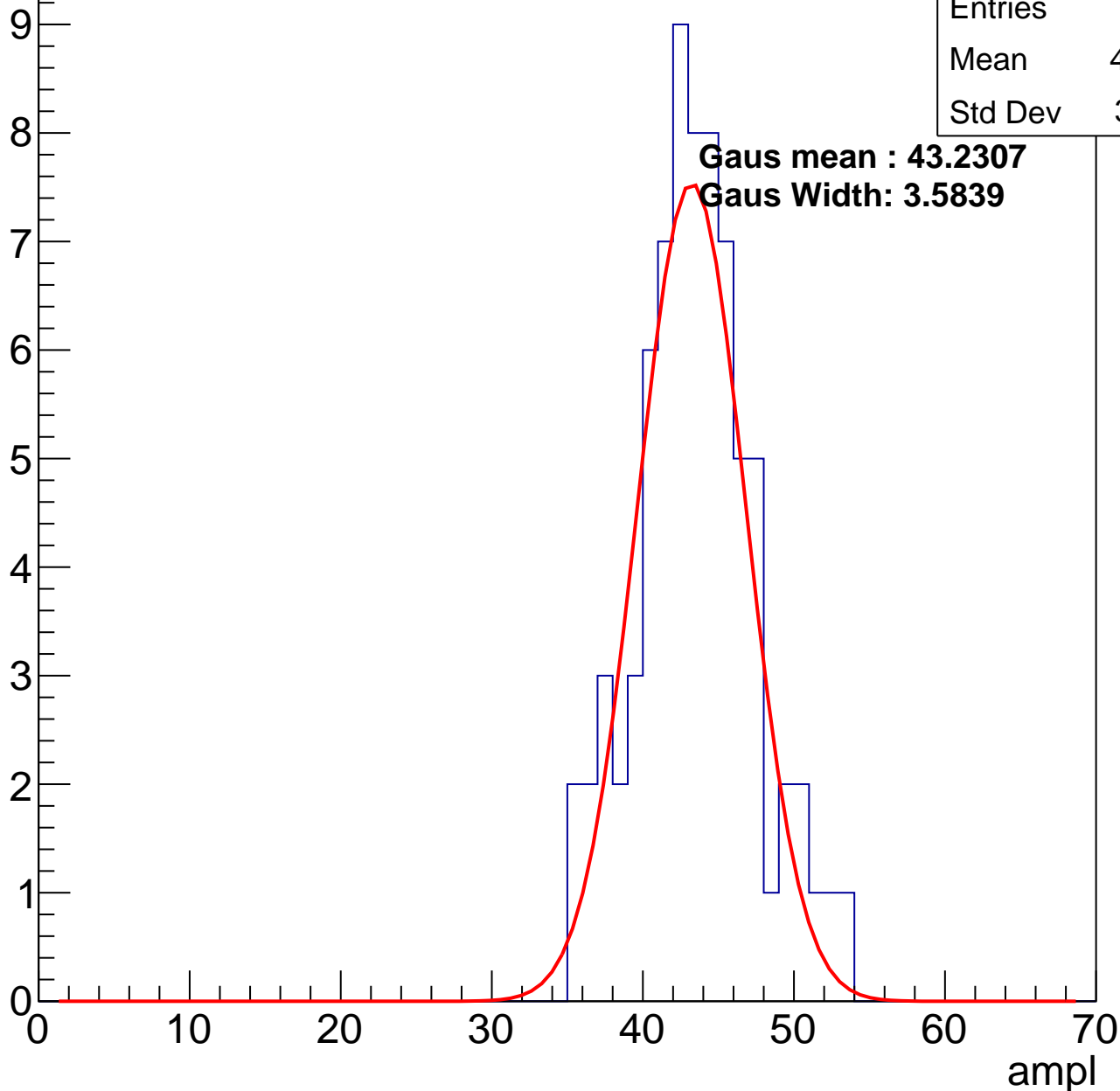
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	43.05
Std Dev	3.871

**Gaus mean : 43.2307**

**Gaus Width: 3.5839**

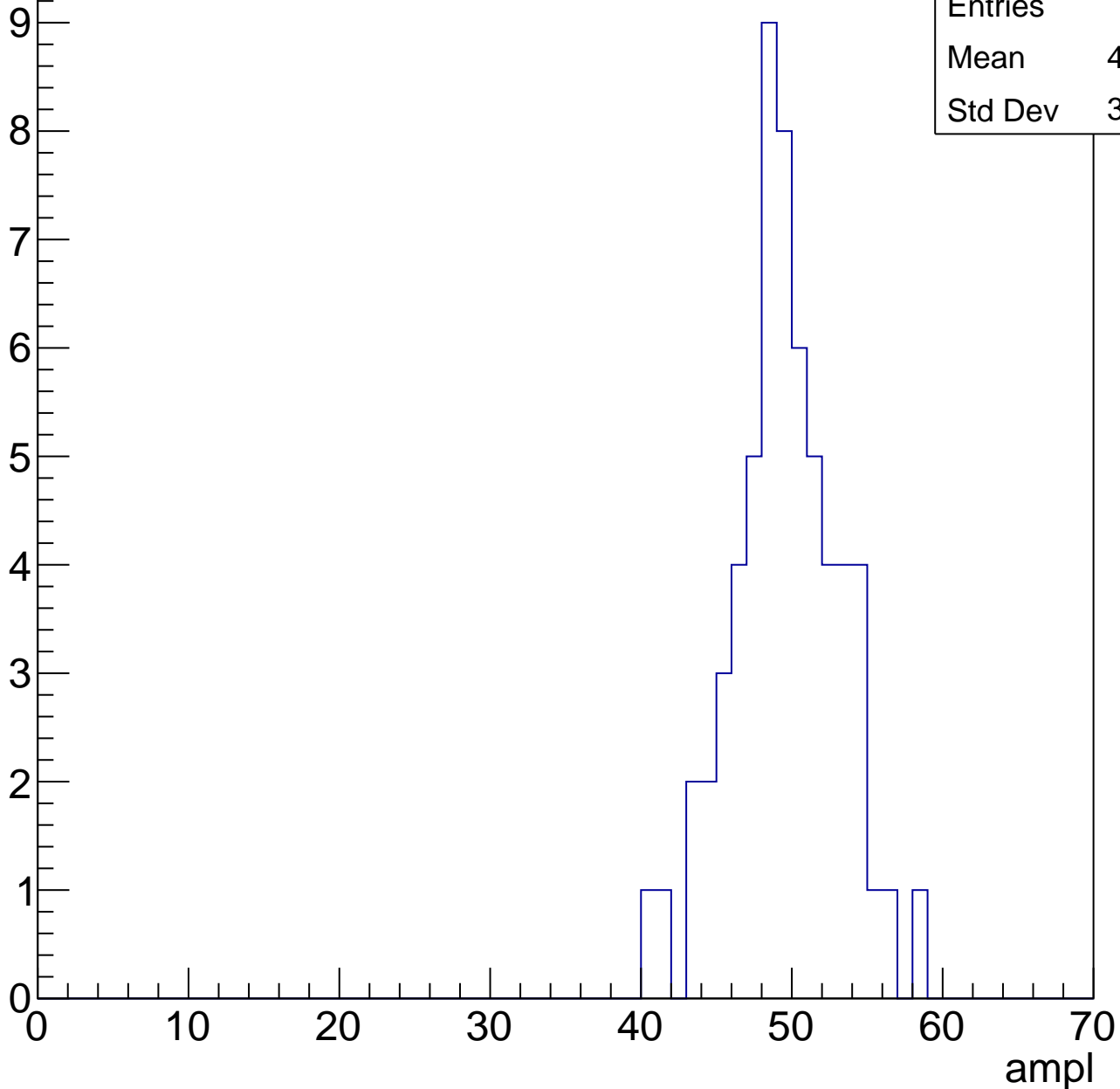


# B1L102S, U16-ch105, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	49.07
Std Dev	3.557

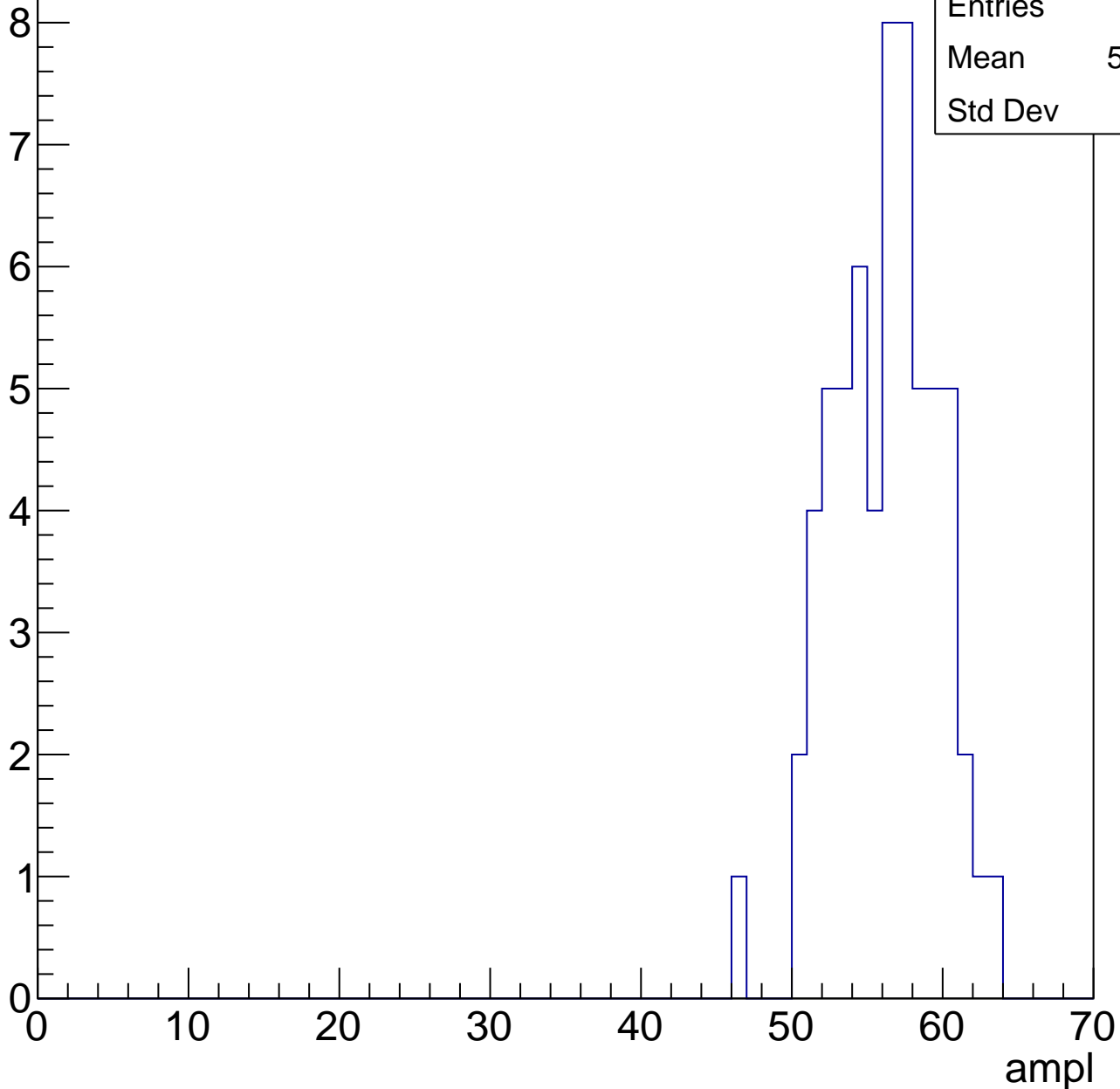


# B1L102S, U16-ch105, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	55.73
Std Dev	3.38

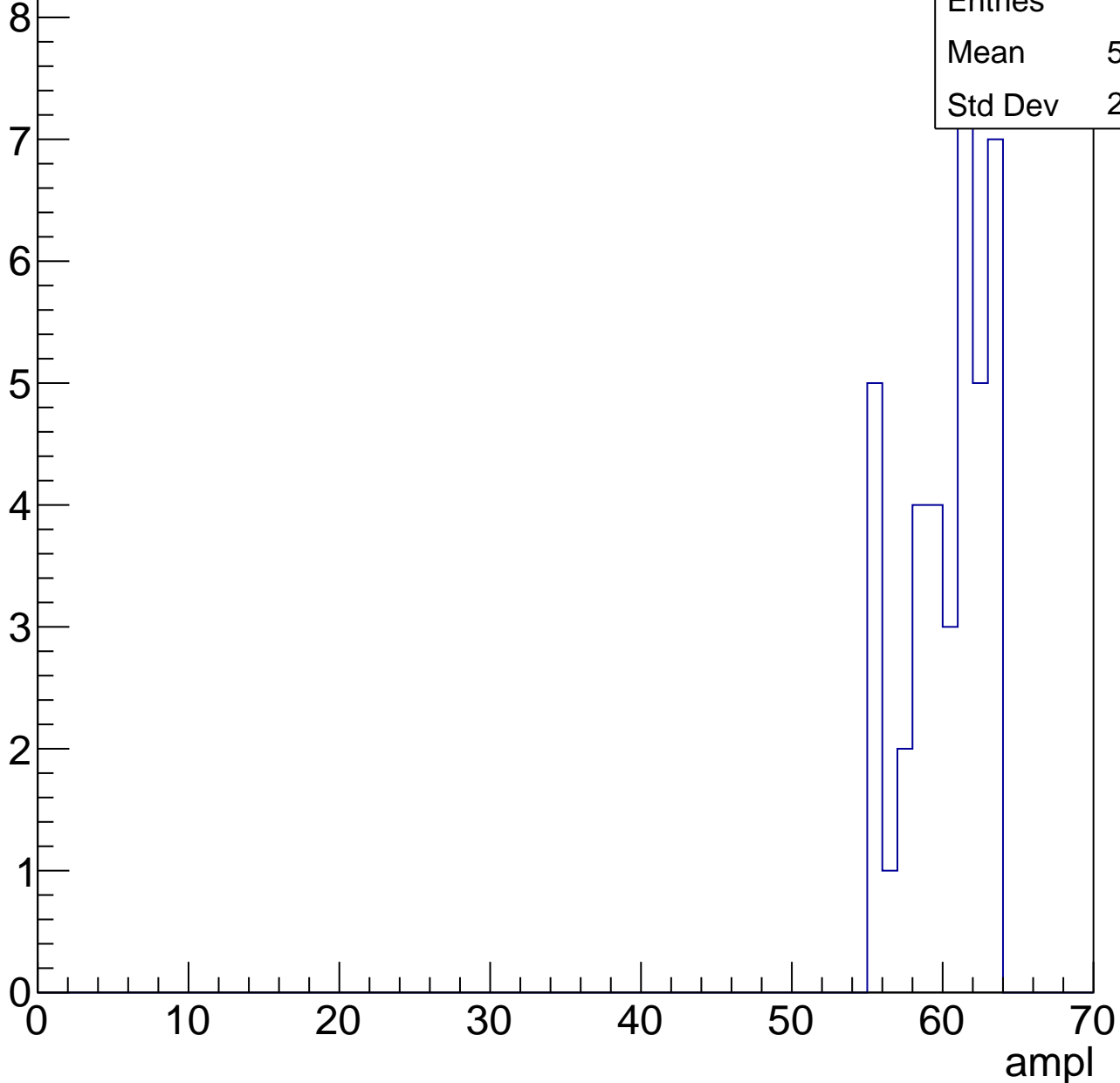


# B1L102S, U16-ch105, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

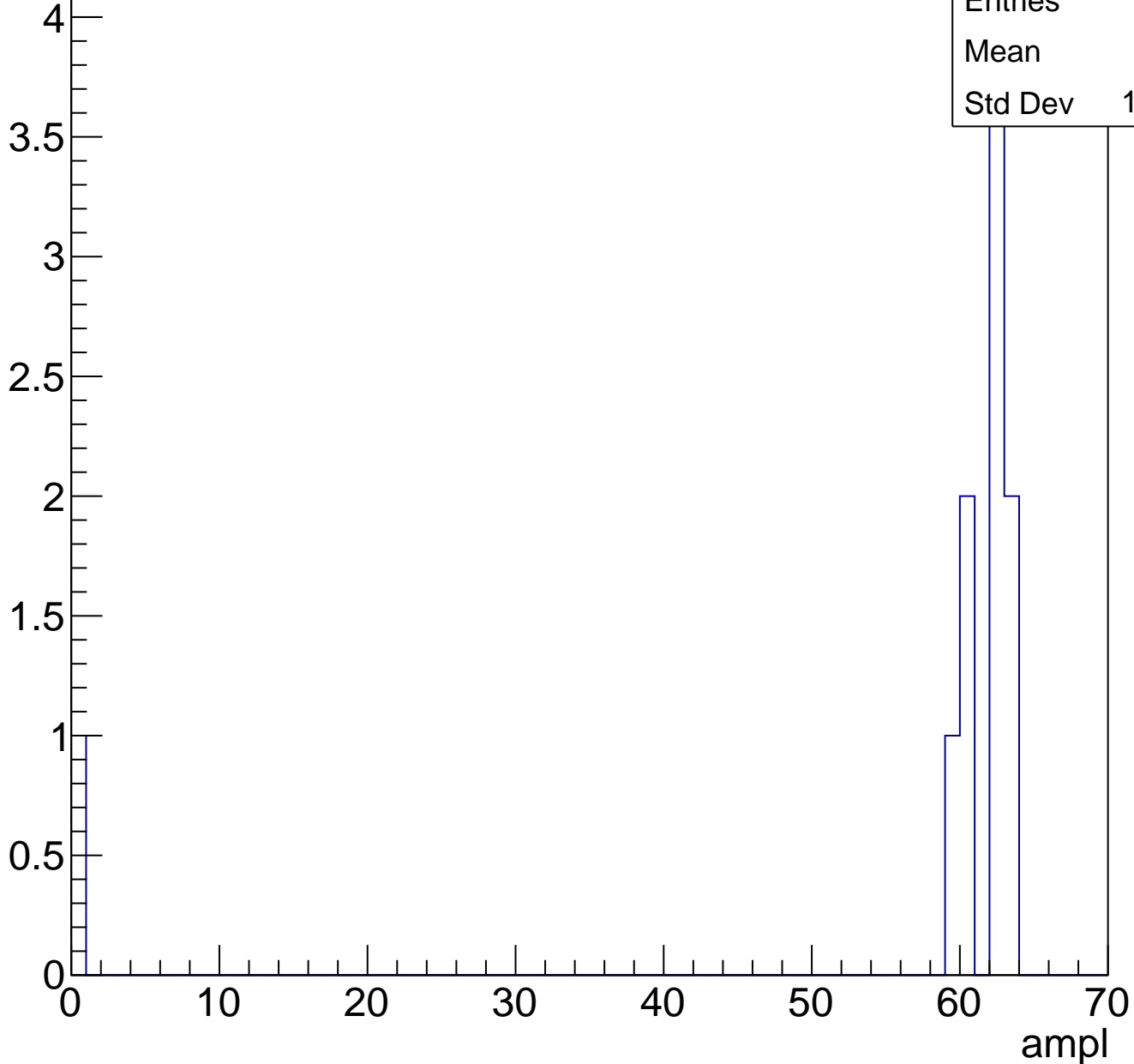
Entries	39
Mean	59.79
Std Dev	2.623



# B1L102S, U16-ch105, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch105, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U16-ch106, adc0

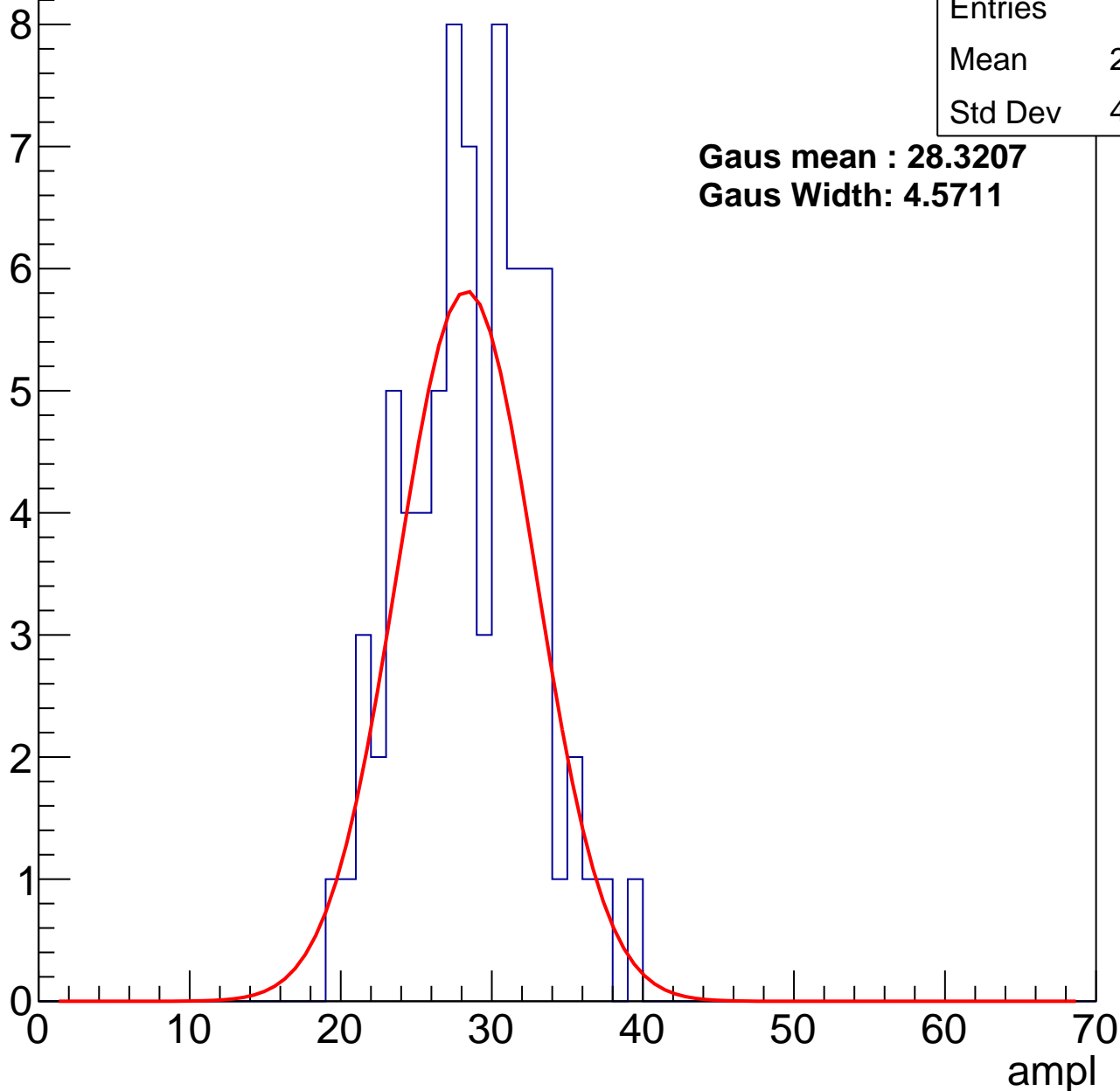
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	28.24
Std Dev	4.239

**Gaus mean : 28.3207**

**Gaus Width: 4.5711**



# B1L102S, U16-ch106, adc1

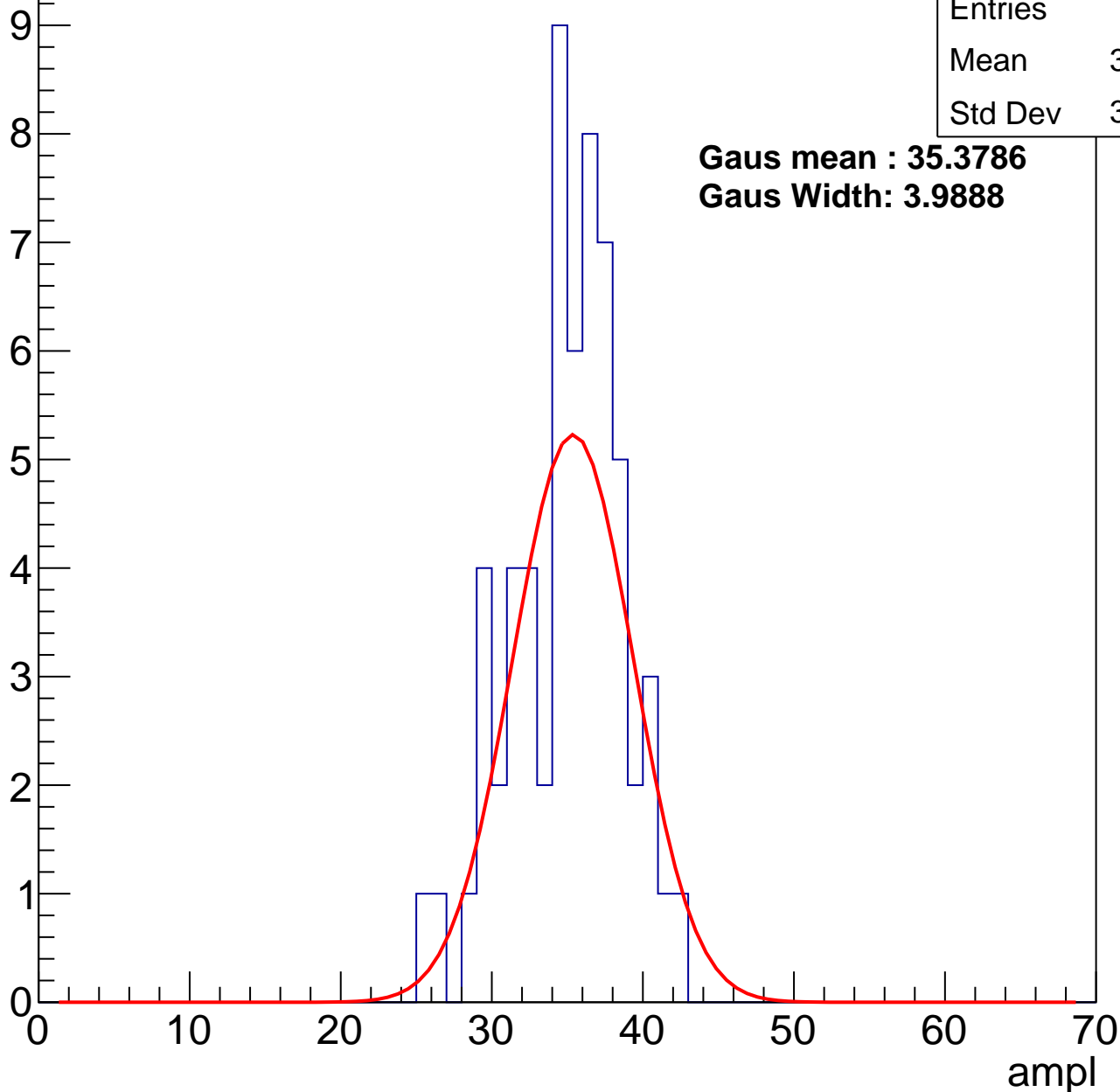
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	34.54
Std Dev	3.624

**Gaus mean : 35.3786**

**Gaus Width: 3.9888**



# B1L102S, U16-ch106, adc2

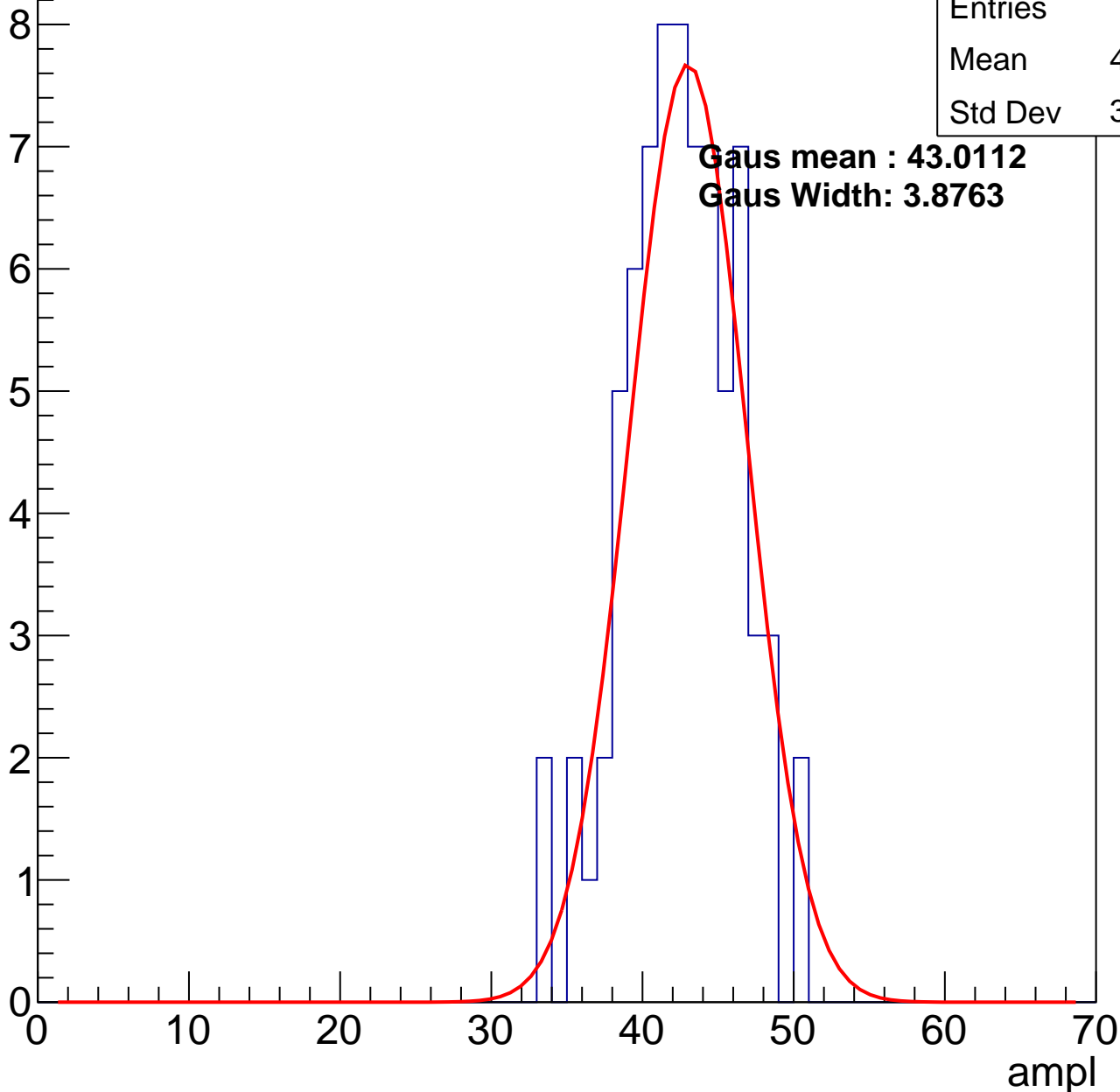
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	75
Mean	42.07
Std Dev	3.685

**Gaus mean : 43.0112**

**Gaus Width: 3.8763**

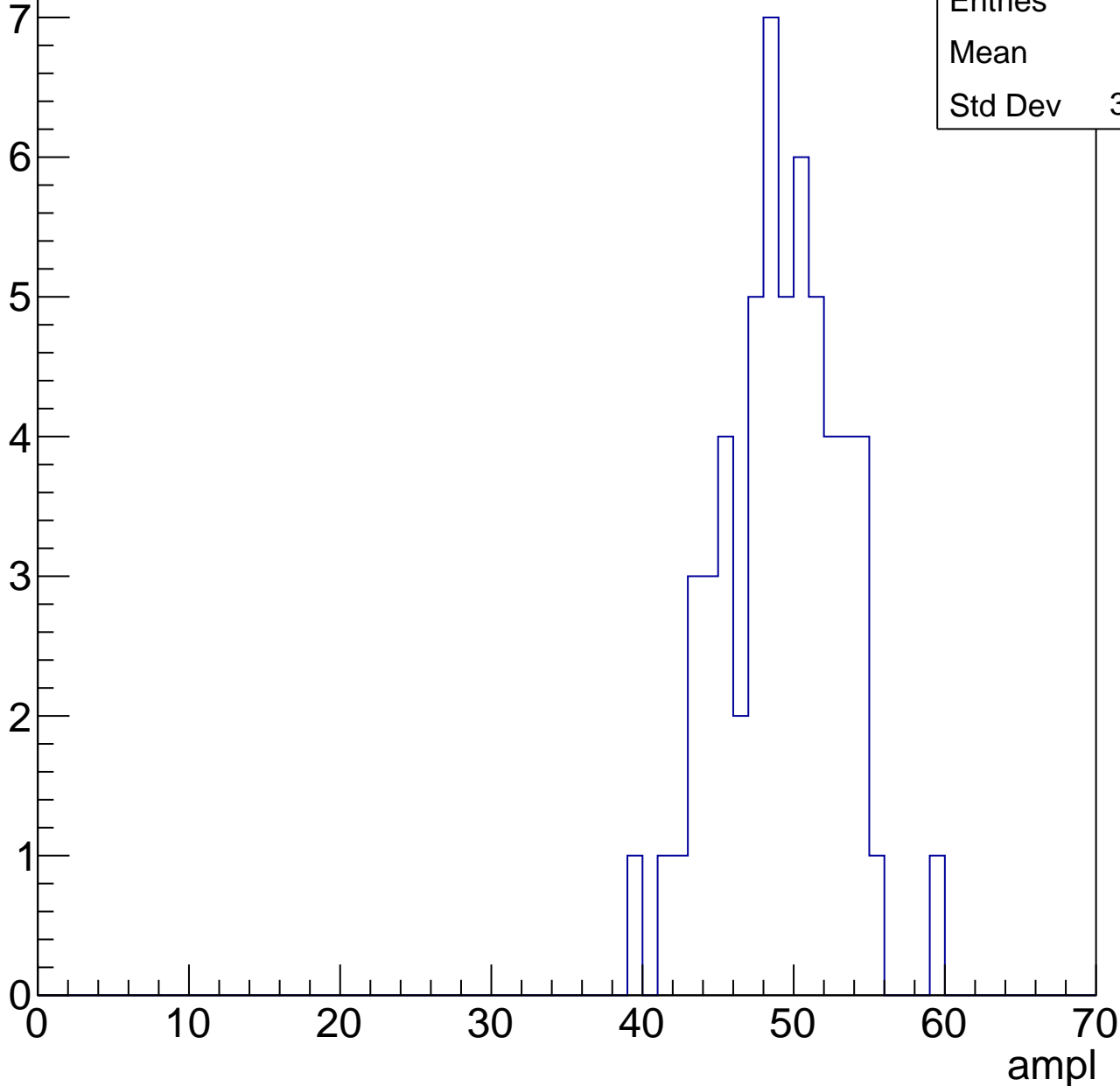


# B1L102S, U16-ch106, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	48.7
Std Dev	3.889

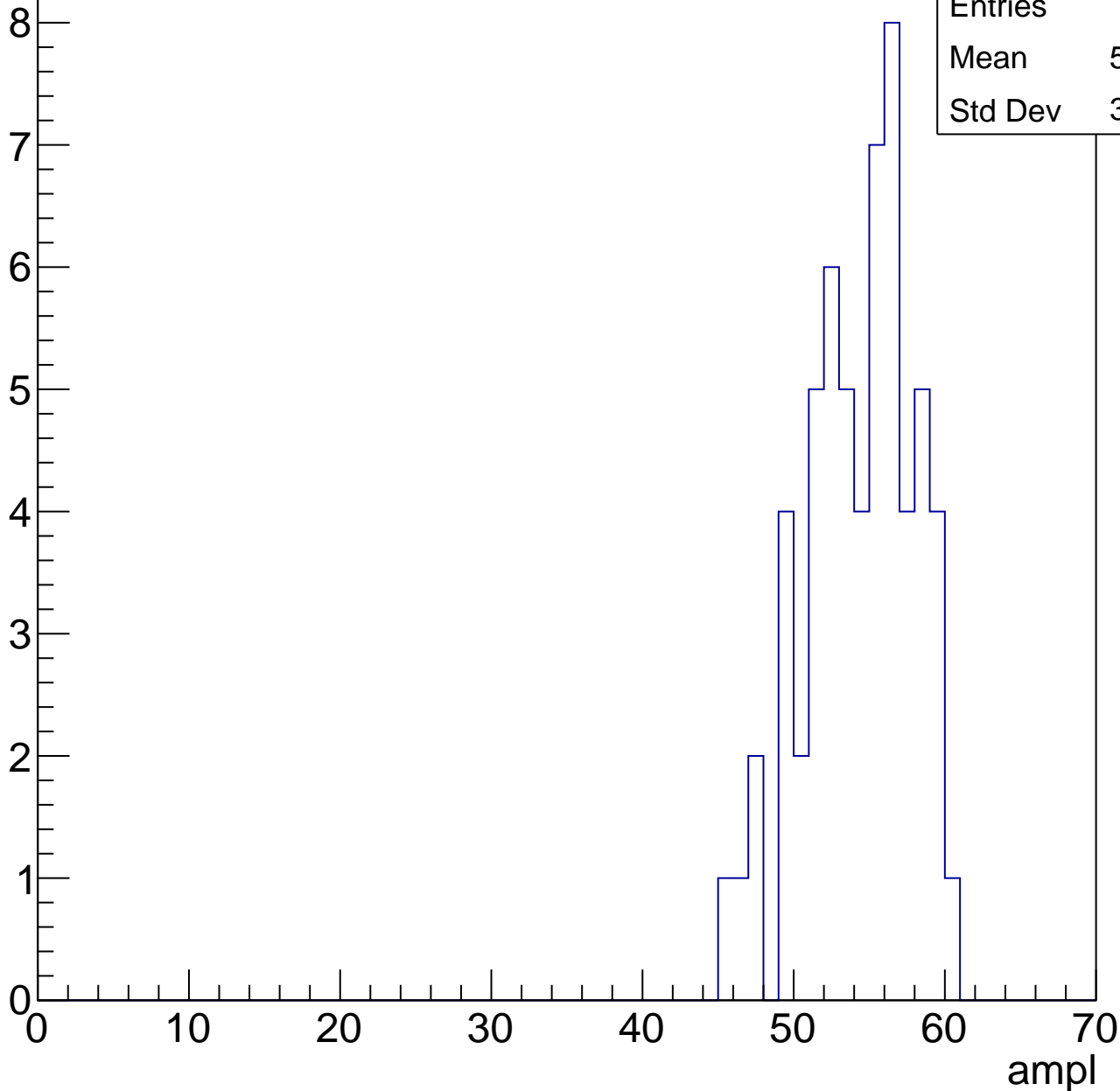


# B1L102S, U16-ch106, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	53.83
Std Dev	3.537

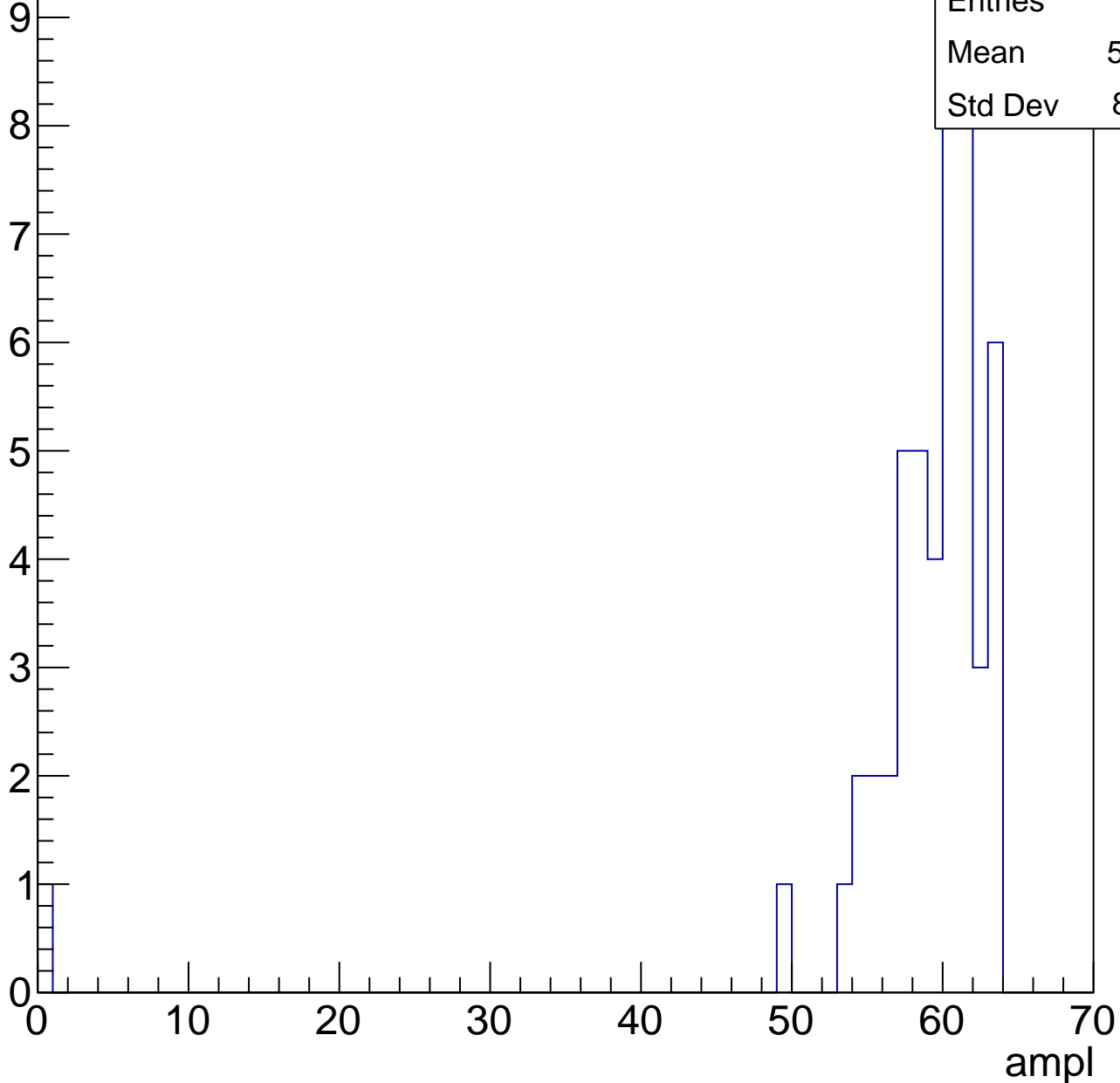


# B1L102S, U16-ch106, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	57.88
Std Dev	8.861

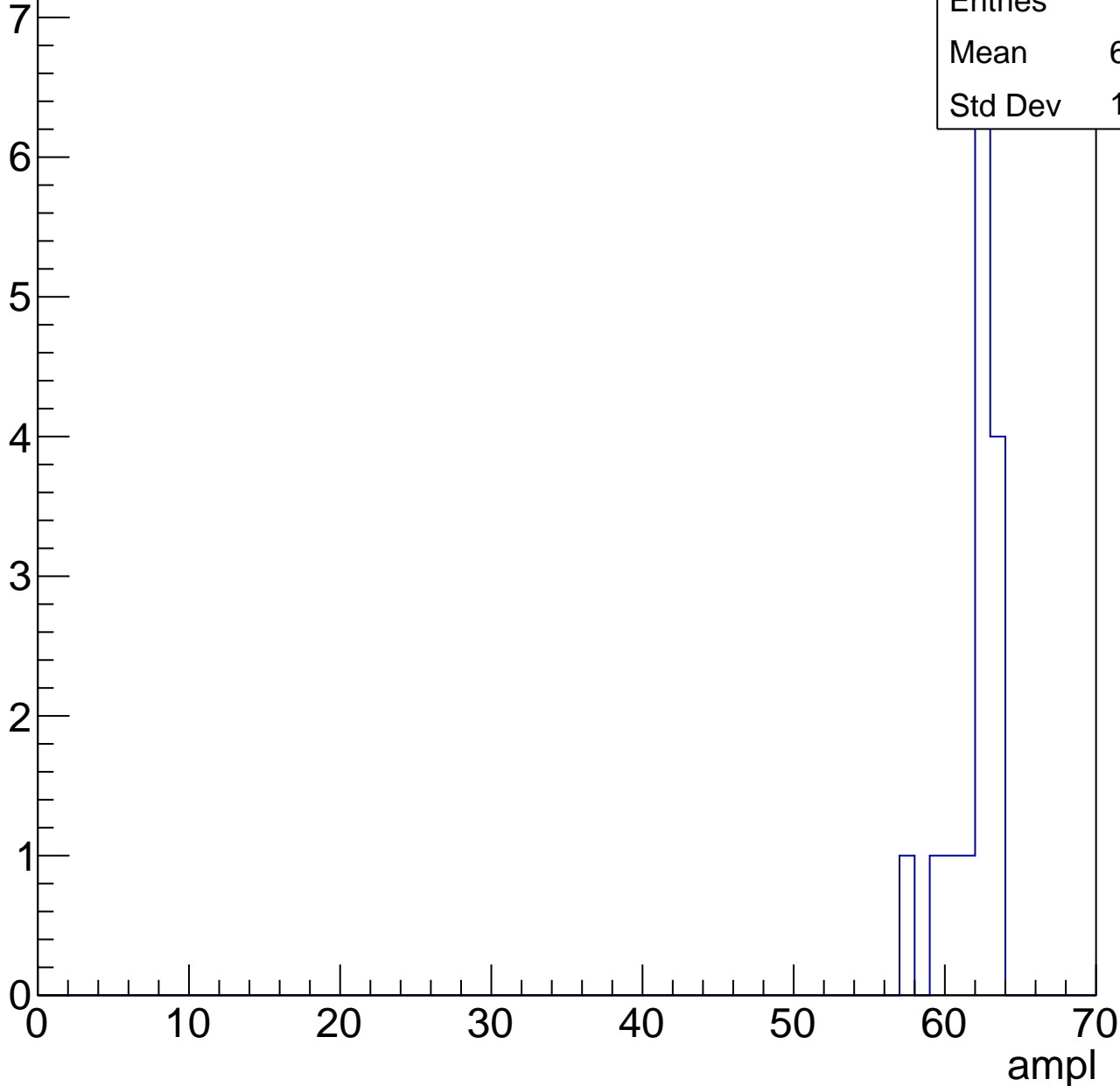


# B1L102S, U16-ch106, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	15
Mean	61.53
Std Dev	1.628





# B1L102S, U16-ch106, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch107, adc0

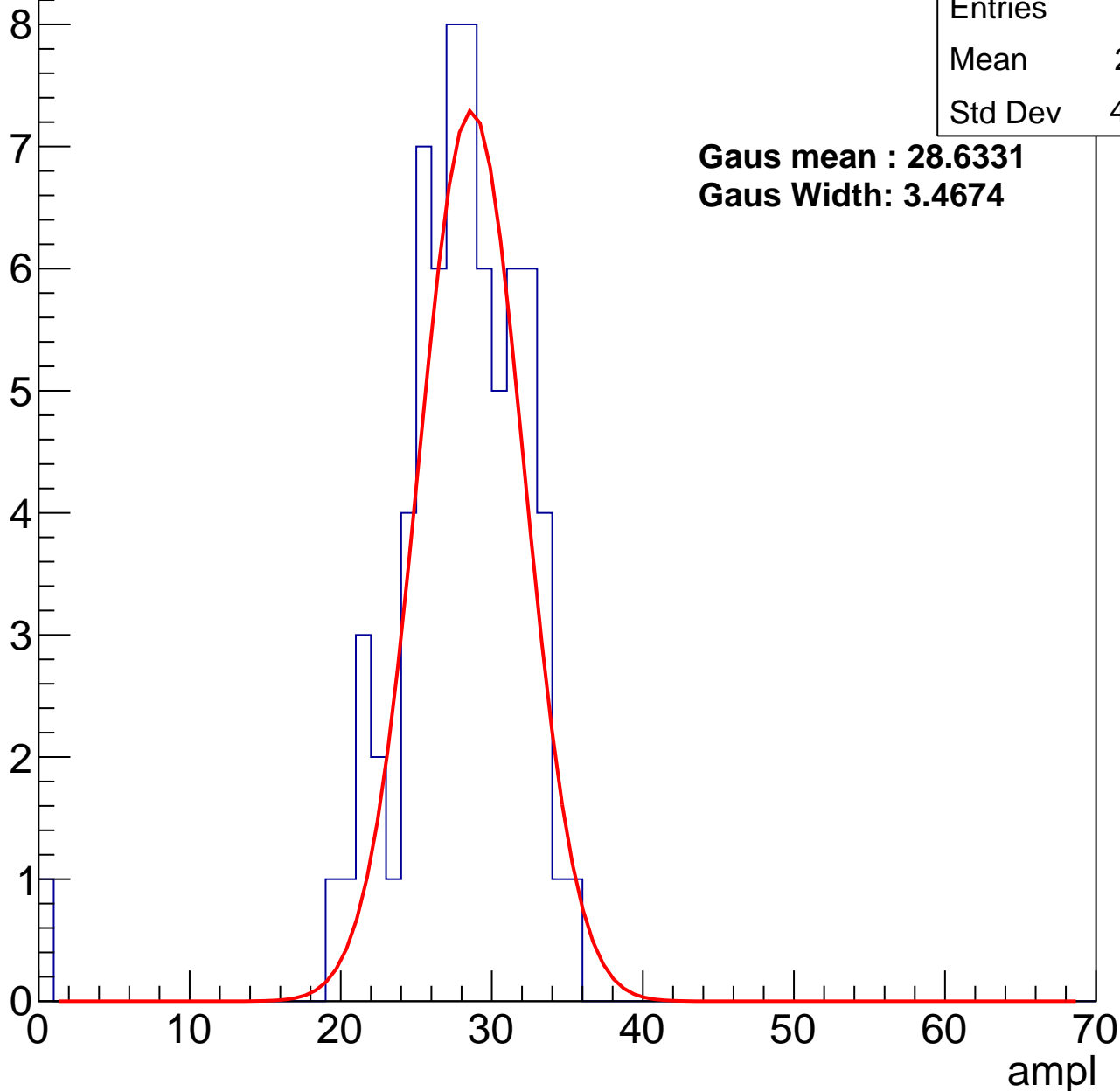
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	27.31
Std Dev	4.834

**Gaus mean : 28.6331**

**Gaus Width: 3.4674**



# B1L102S, U16-ch107, adc1

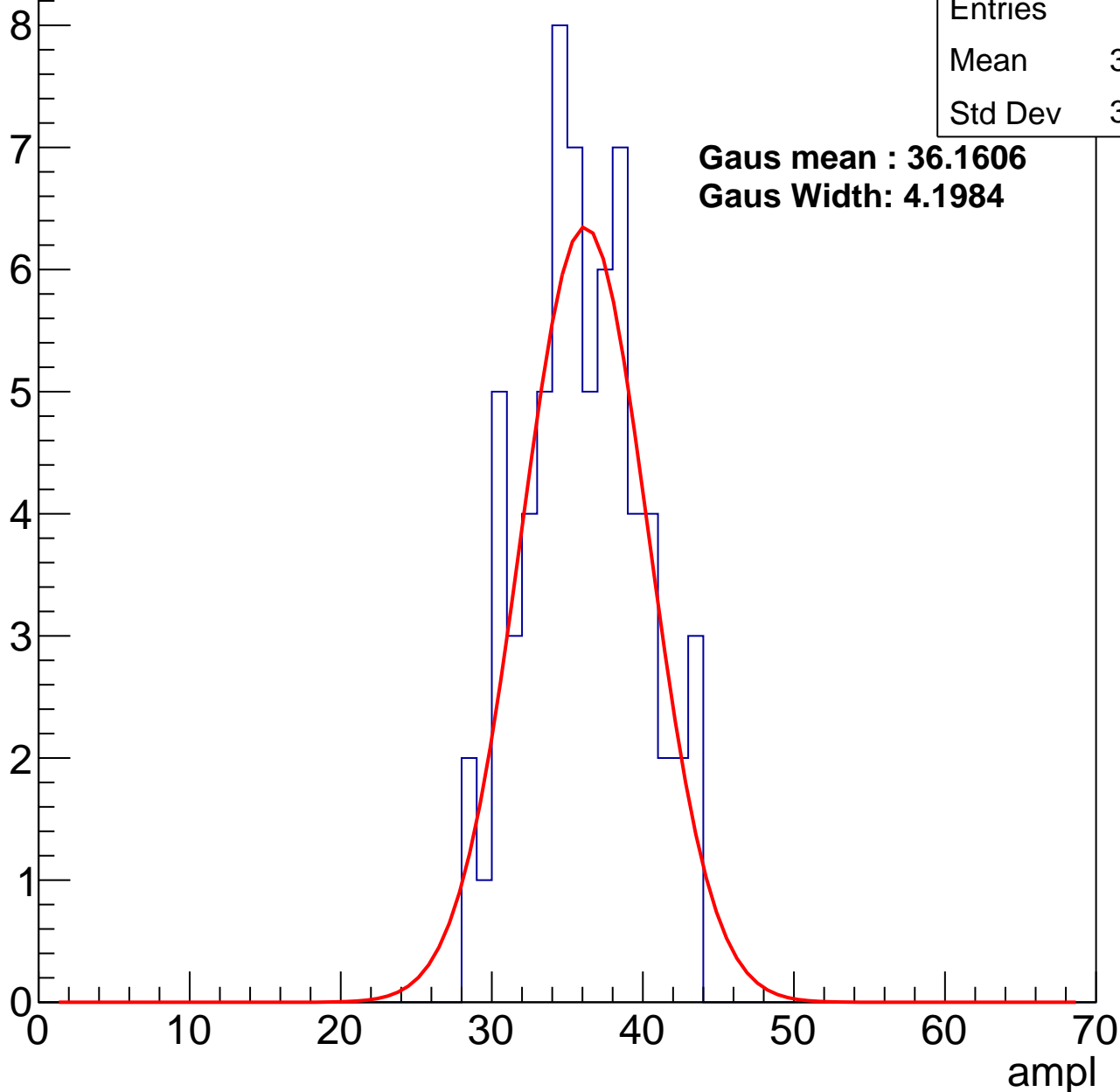
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	35.54
Std Dev	3.775

**Gaus mean : 36.1606**

**Gaus Width: 4.1984**



# B1L102S, U16-ch107, adc2

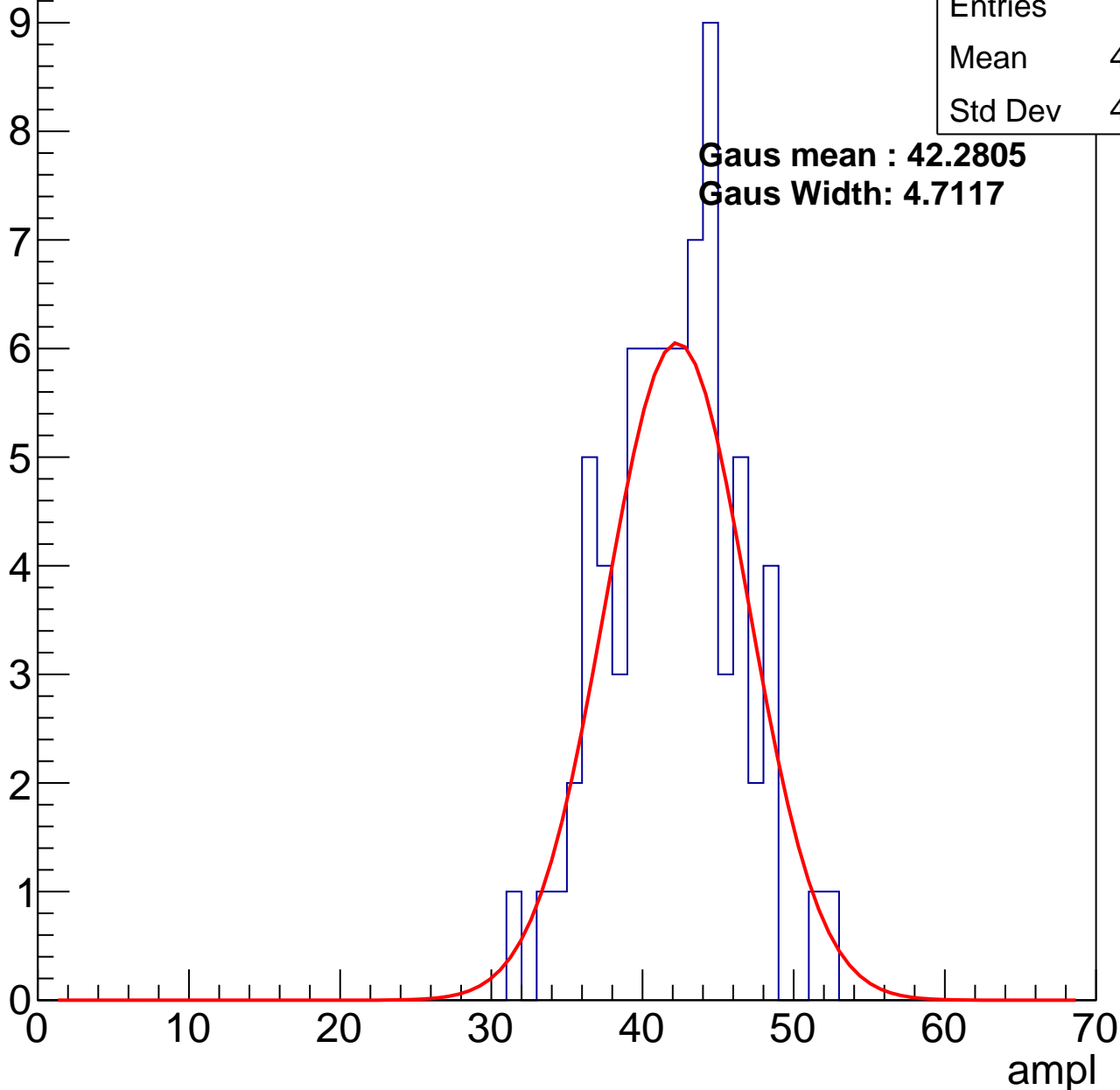
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	73
Mean	41.55
Std Dev	4.197

**Gaus mean : 42.2805**

**Gaus Width: 4.7117**

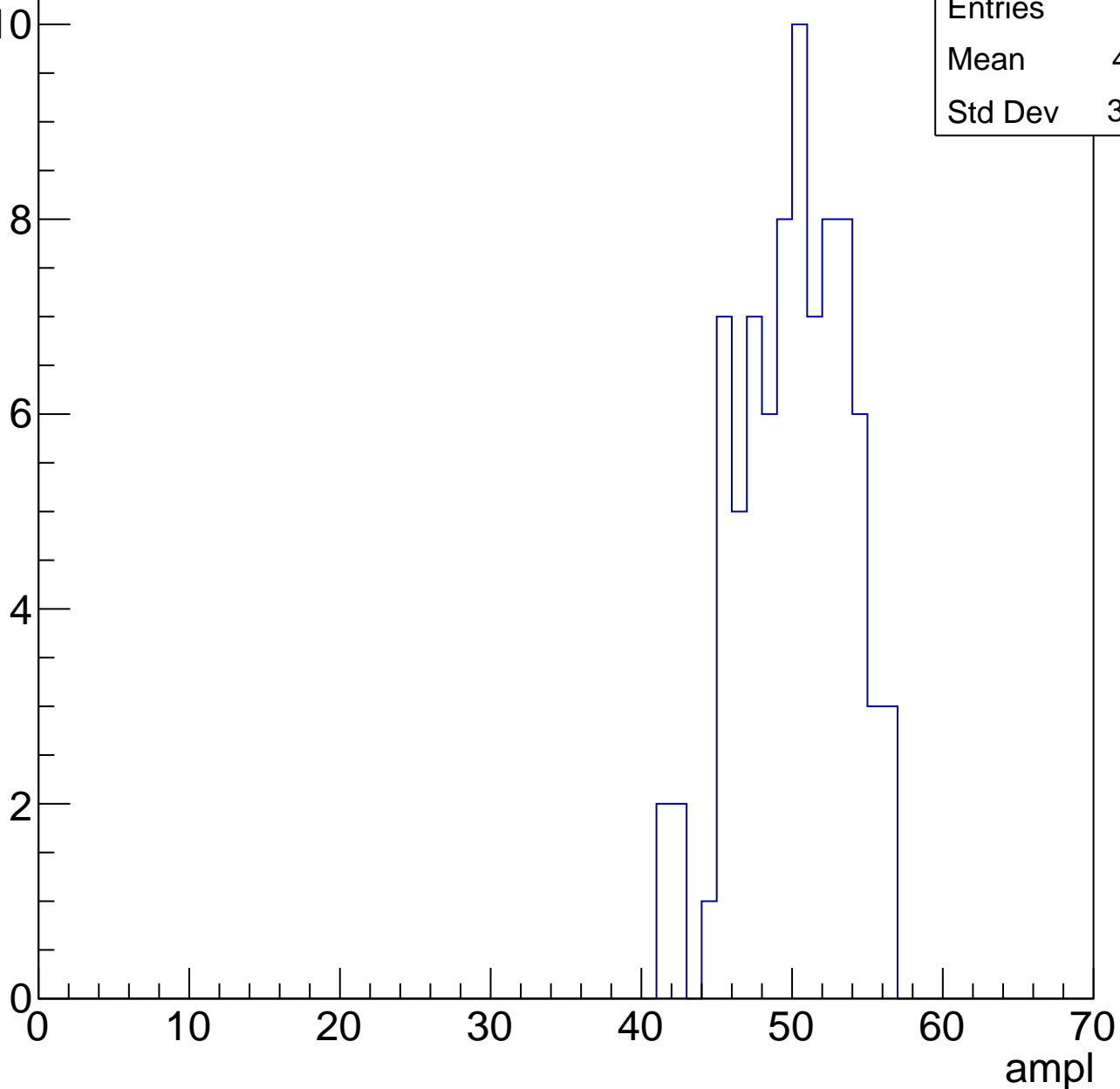


# B1L102S, U16-ch107, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	83
Mean	49.61
Std Dev	3.563

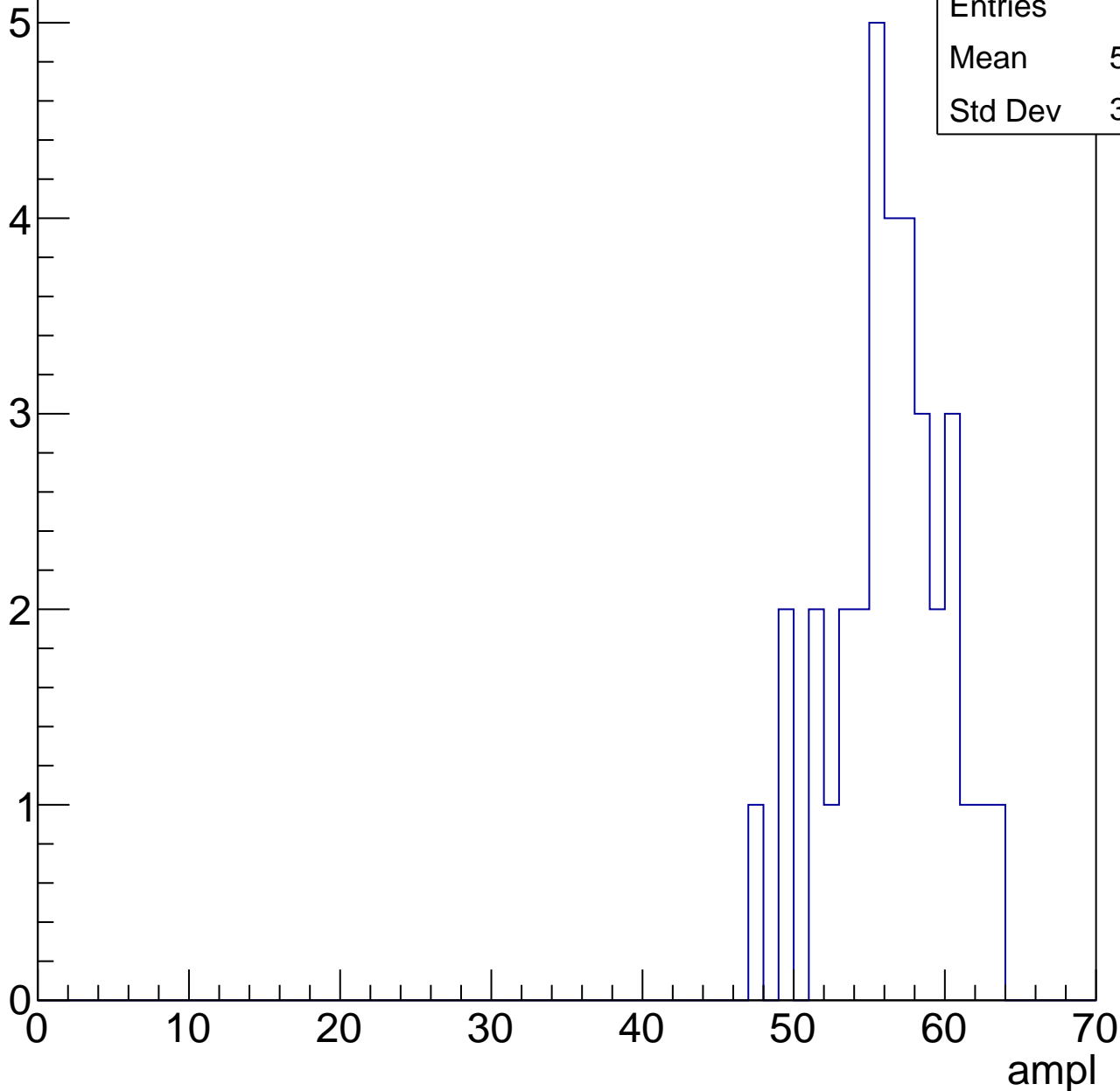


# B1L102S, U16-ch107, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	34
Mean	55.82
Std Dev	3.706

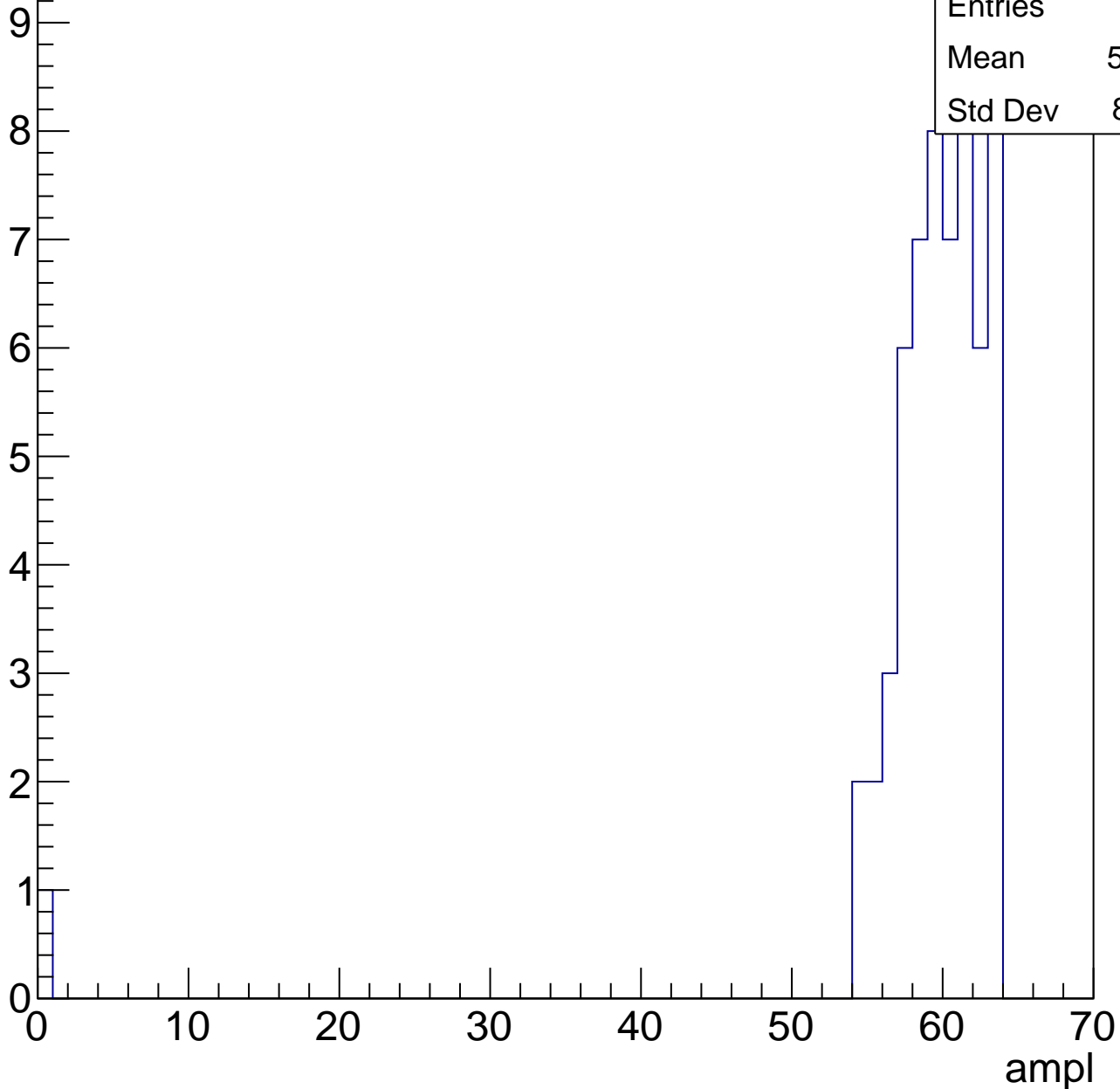


# B1L102S, U16-ch107, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	58.57
Std Dev	8.011



# B1L102S, U16-ch107, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch107, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U16-ch108, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	74
Mean	28.84
Std Dev	3.598

**Gaus mean : 29.1454**

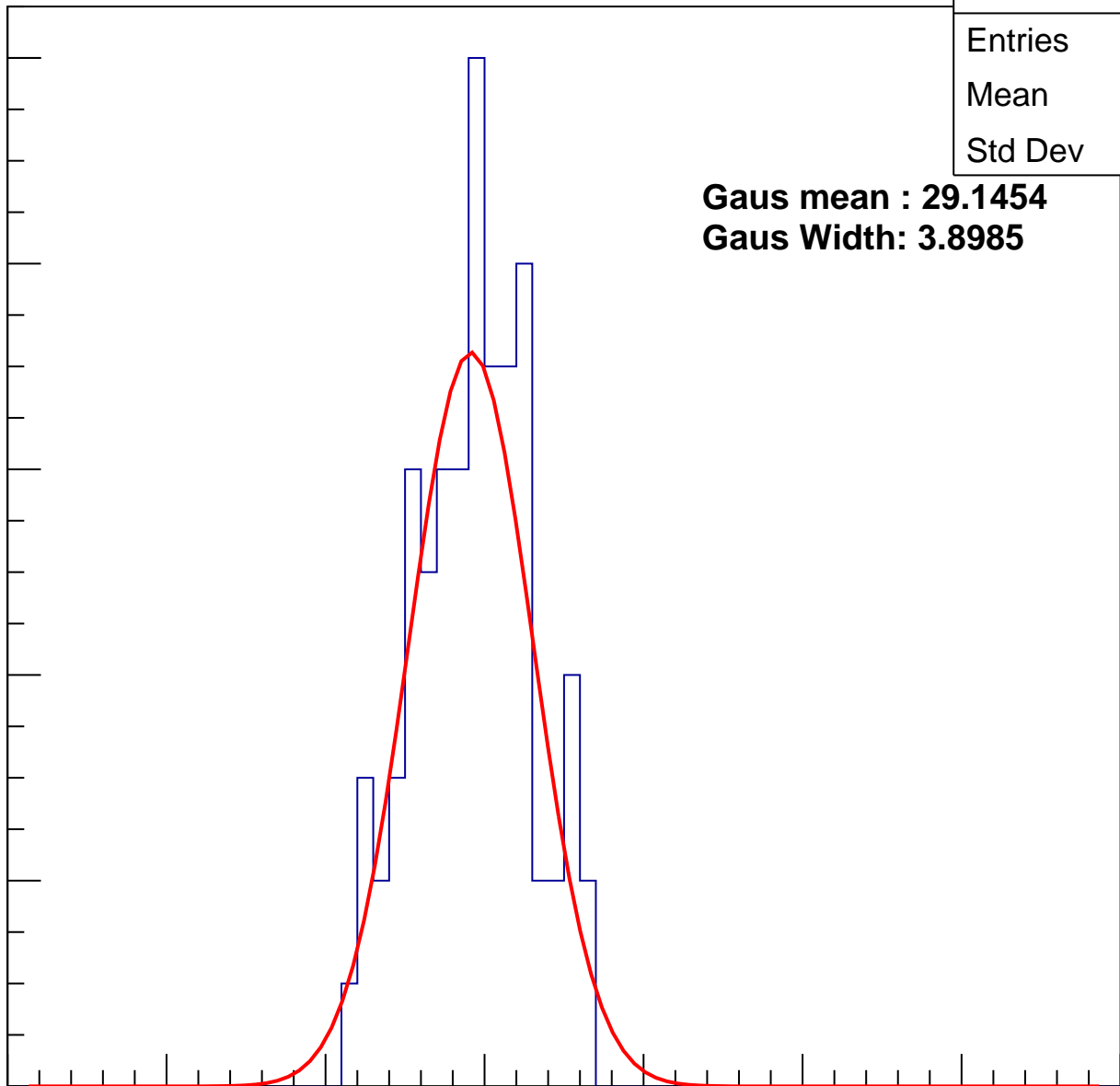
**Gaus Width: 3.8985**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U16-ch108, adc1

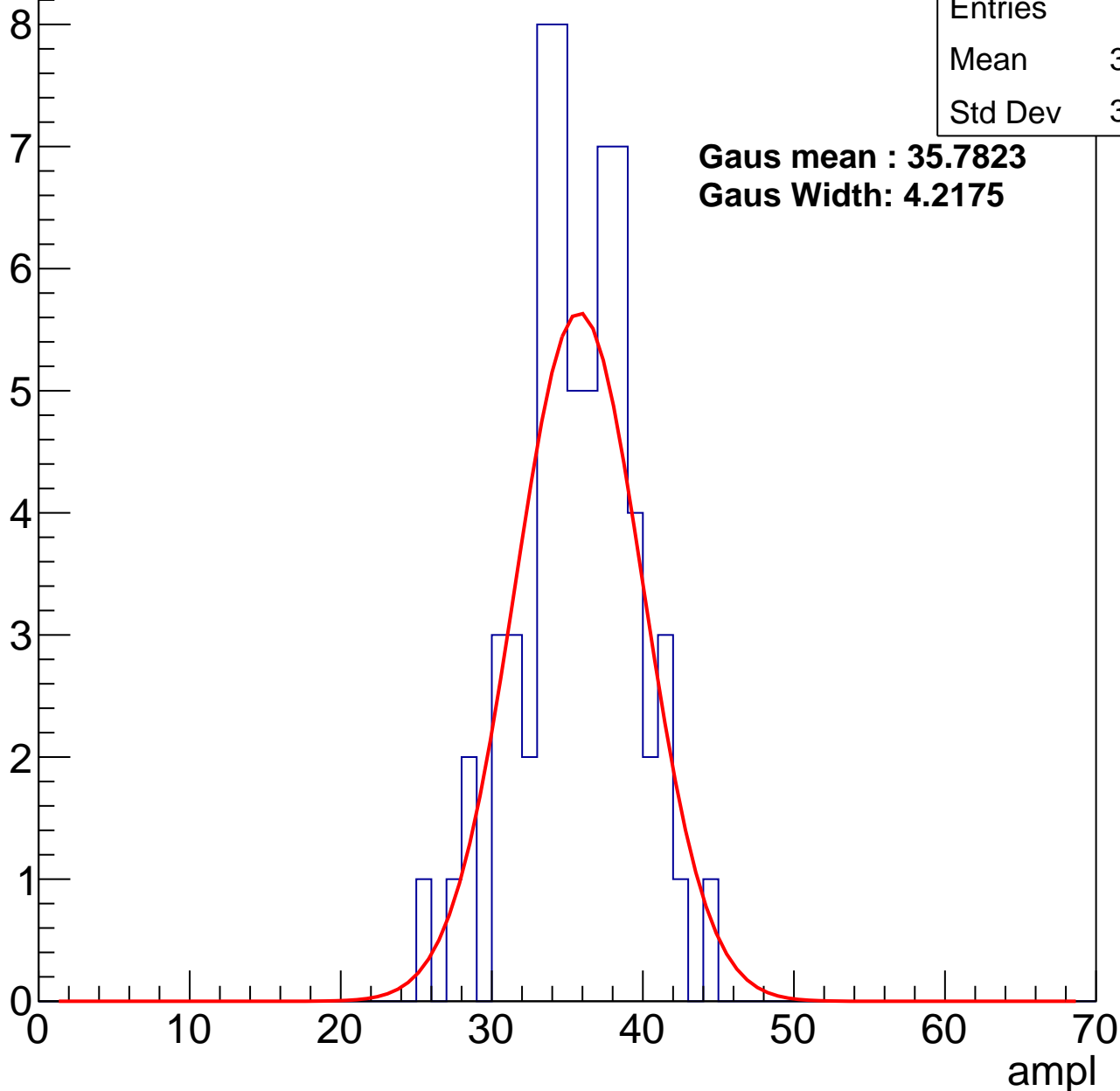
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	35.17
Std Dev	3.757

**Gaus mean : 35.7823**

**Gaus Width: 4.2175**



# B1L102S, U16-ch108, adc2

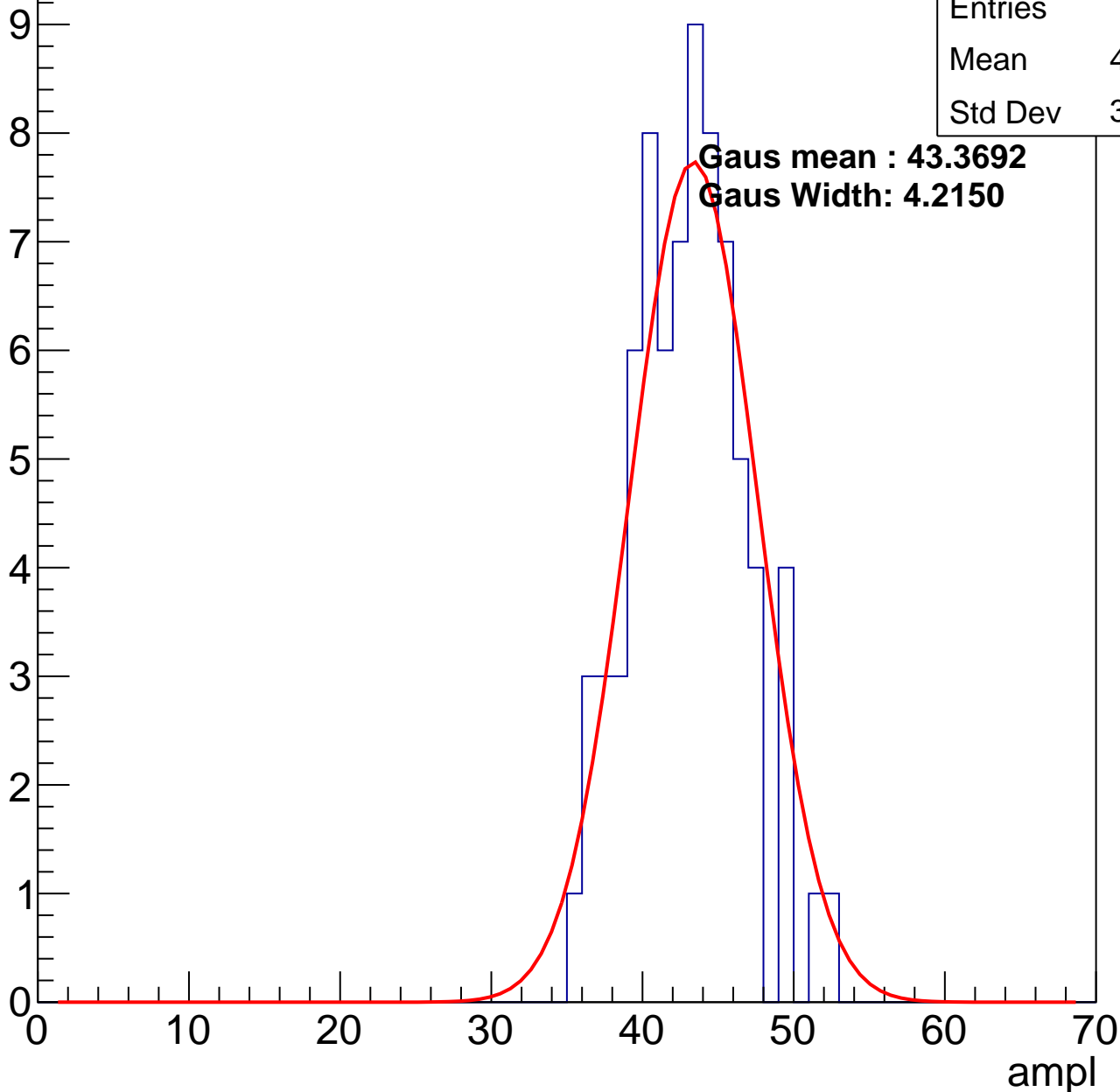
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	42.54
Std Dev	3.647

**Gaus mean : 43.3692**

**Gaus Width: 4.2150**

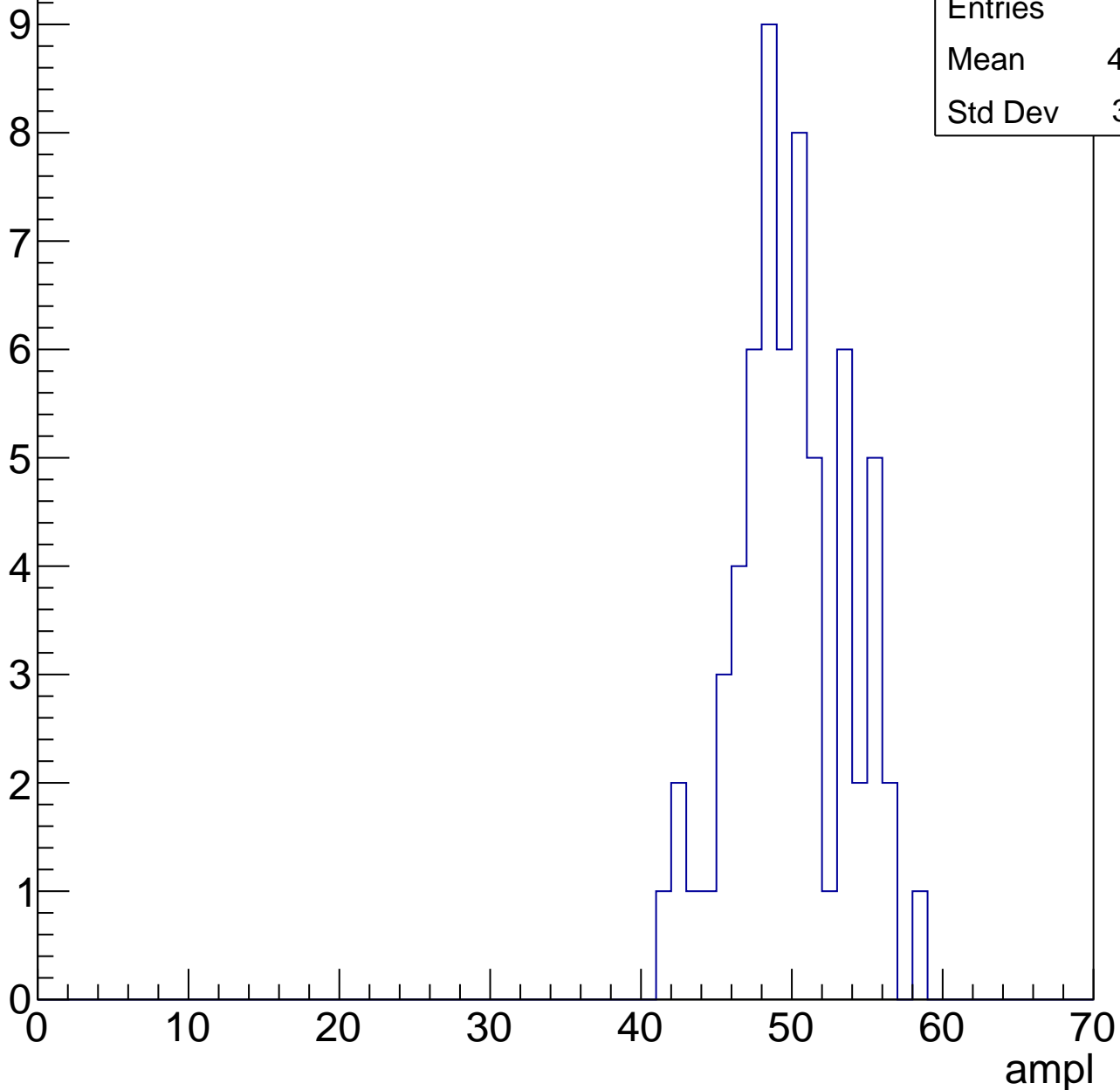


# B1L102S, U16-ch108, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	49.48
Std Dev	3.711

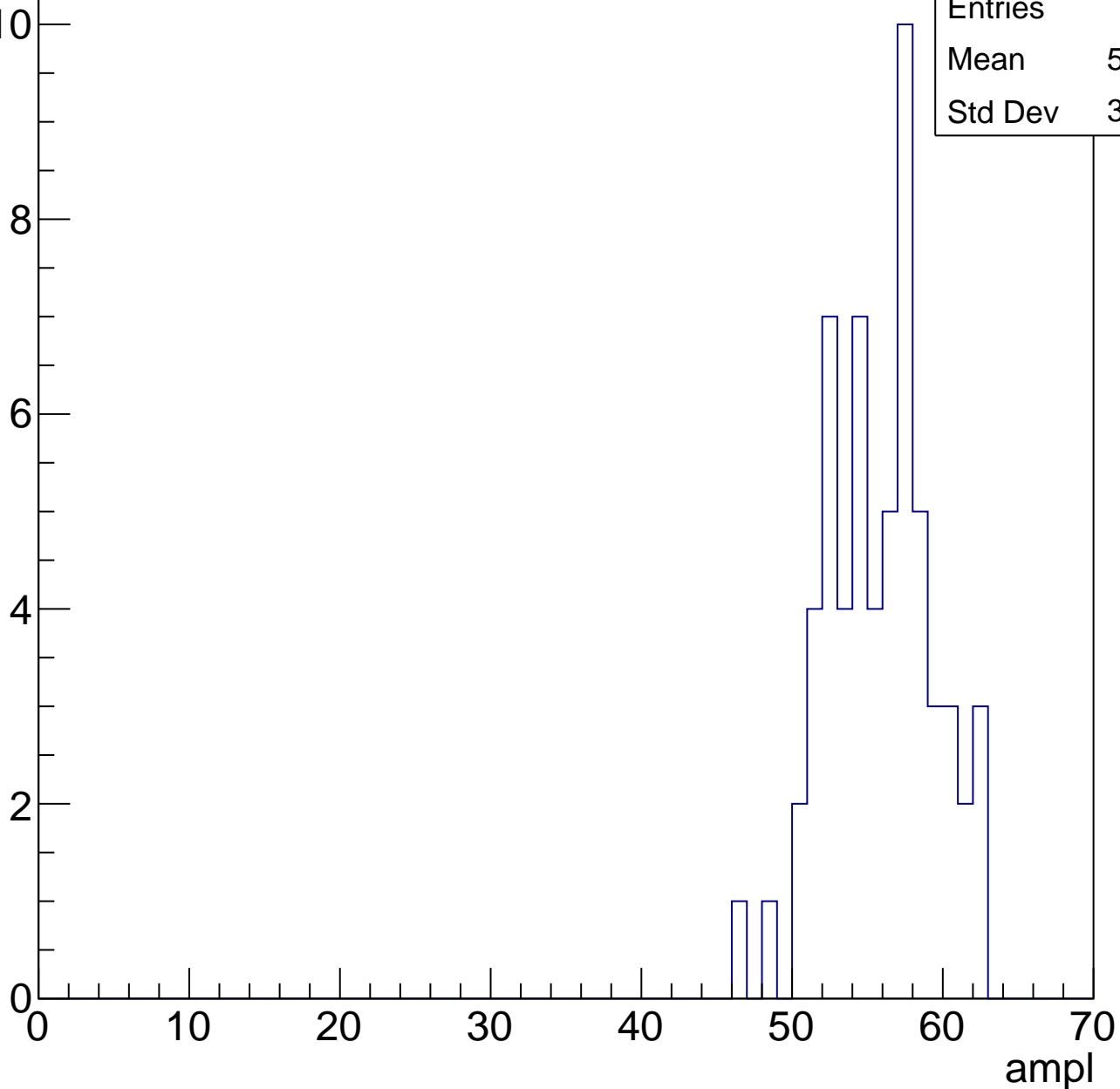


# B1L102S, U16-ch108, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	55.36
Std Dev	3.516

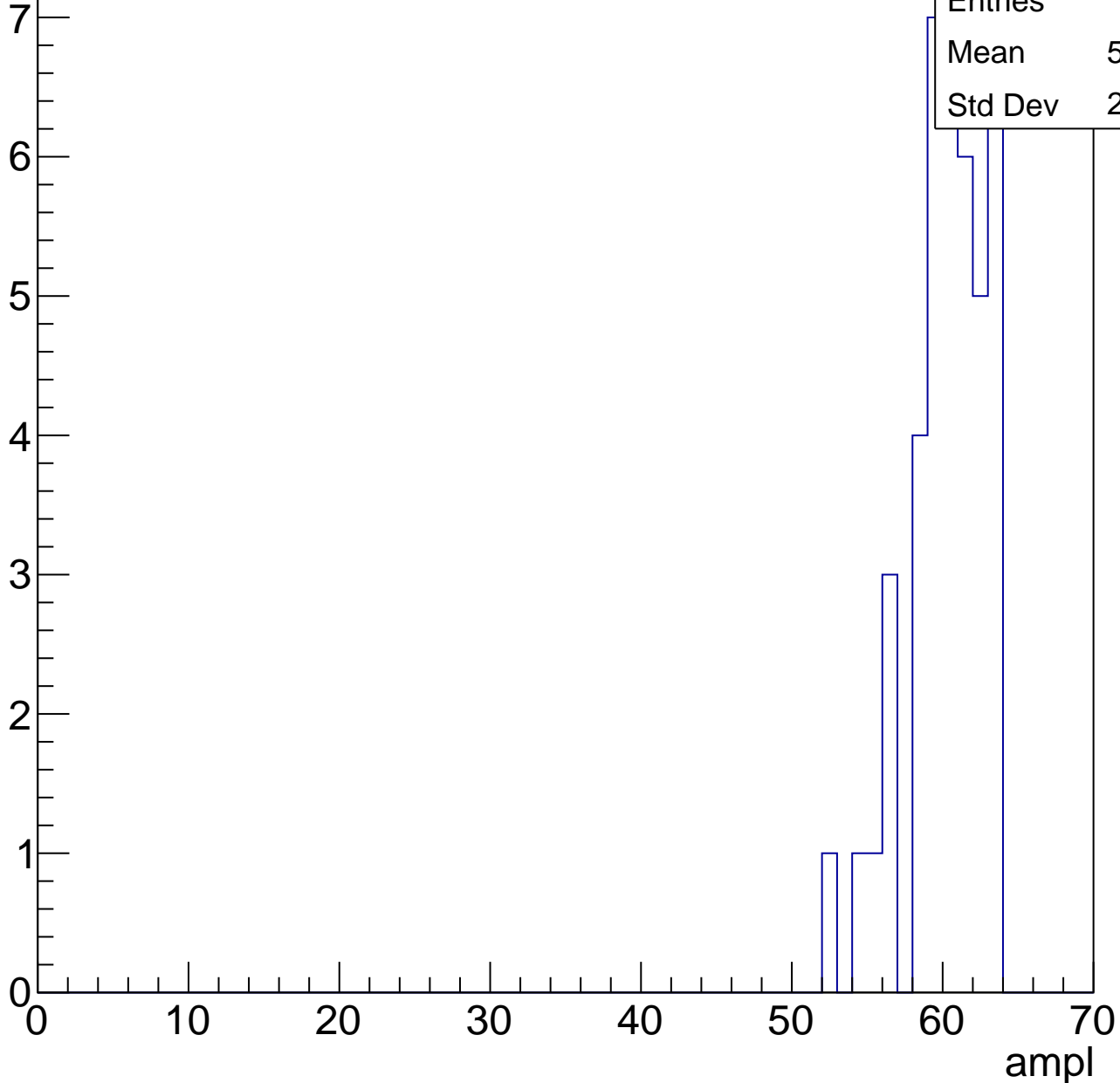


# B1L102S, U16-ch108, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

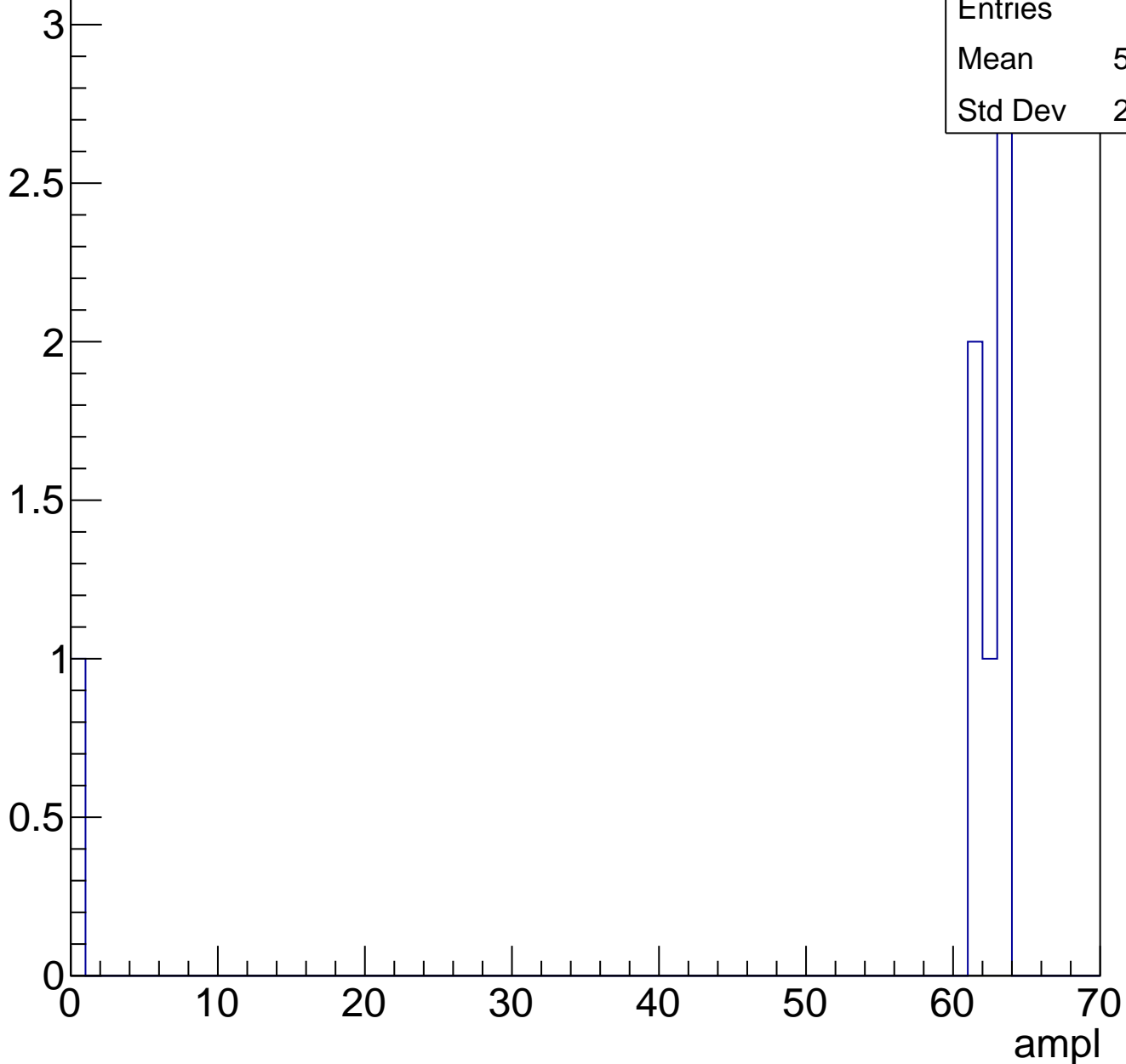
Entries	42
Mean	59.79
Std Dev	2.596



# B1L102S, U16-ch108, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch108, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch109, adc0

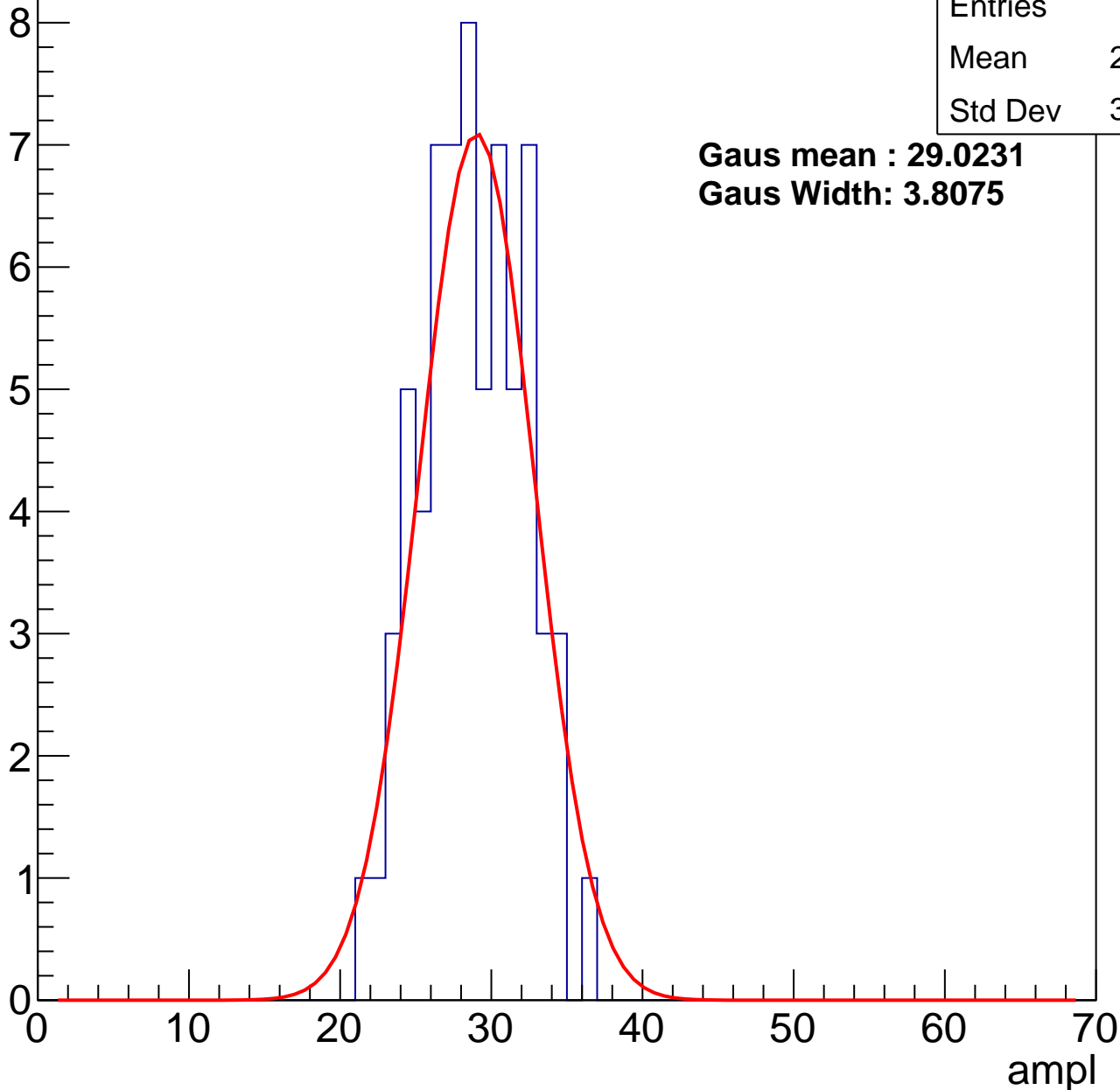
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	28.33
Std Dev	3.325

**Gaus mean : 29.0231**

**Gaus Width: 3.8075**



# B1L102S, U16-ch109, adc1

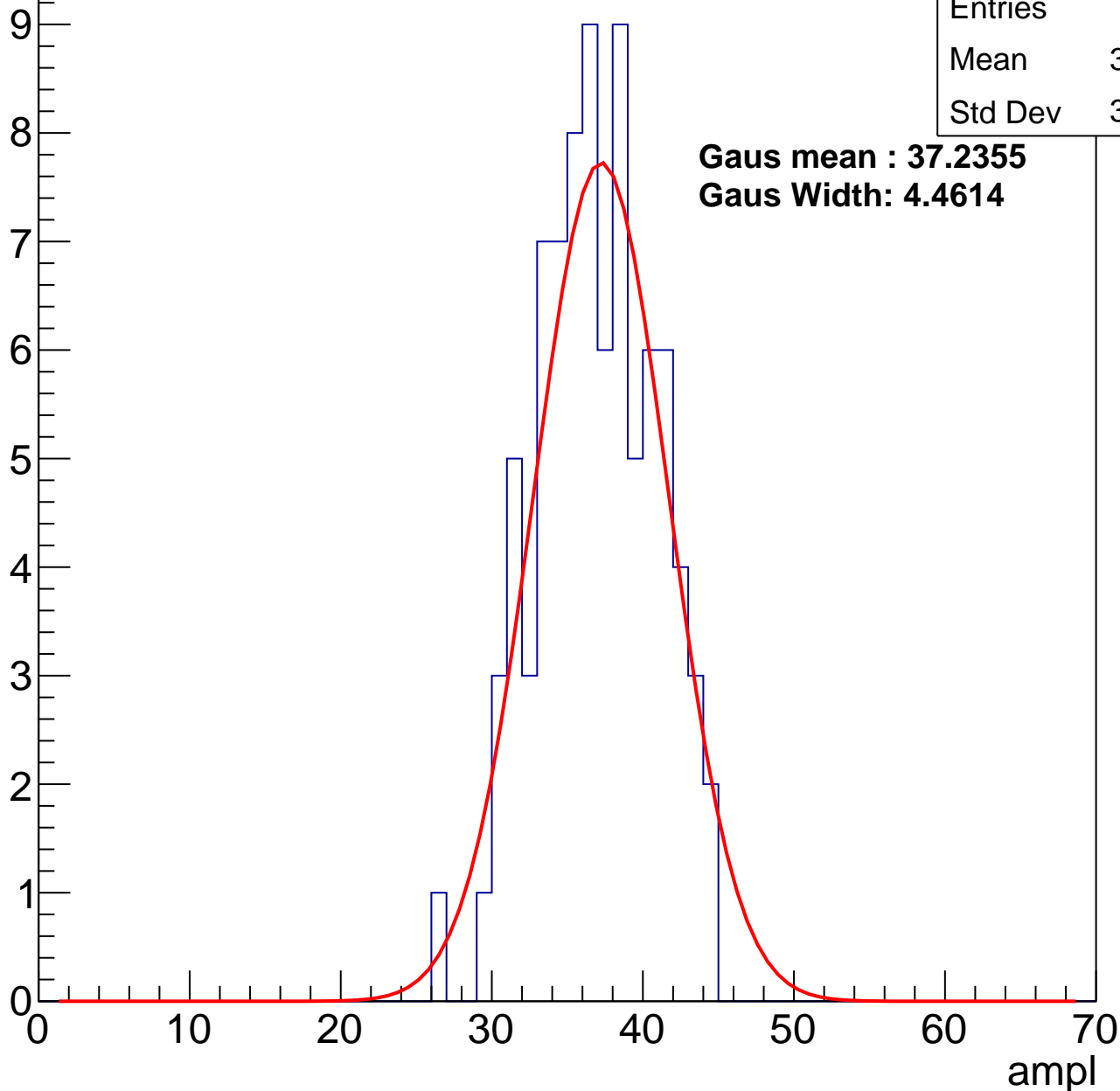
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	85
Mean	36.46
Std Dev	3.855

**Gaus mean : 37.2355**

**Gaus Width: 4.4614**



# B1L102S, U16-ch109, adc2

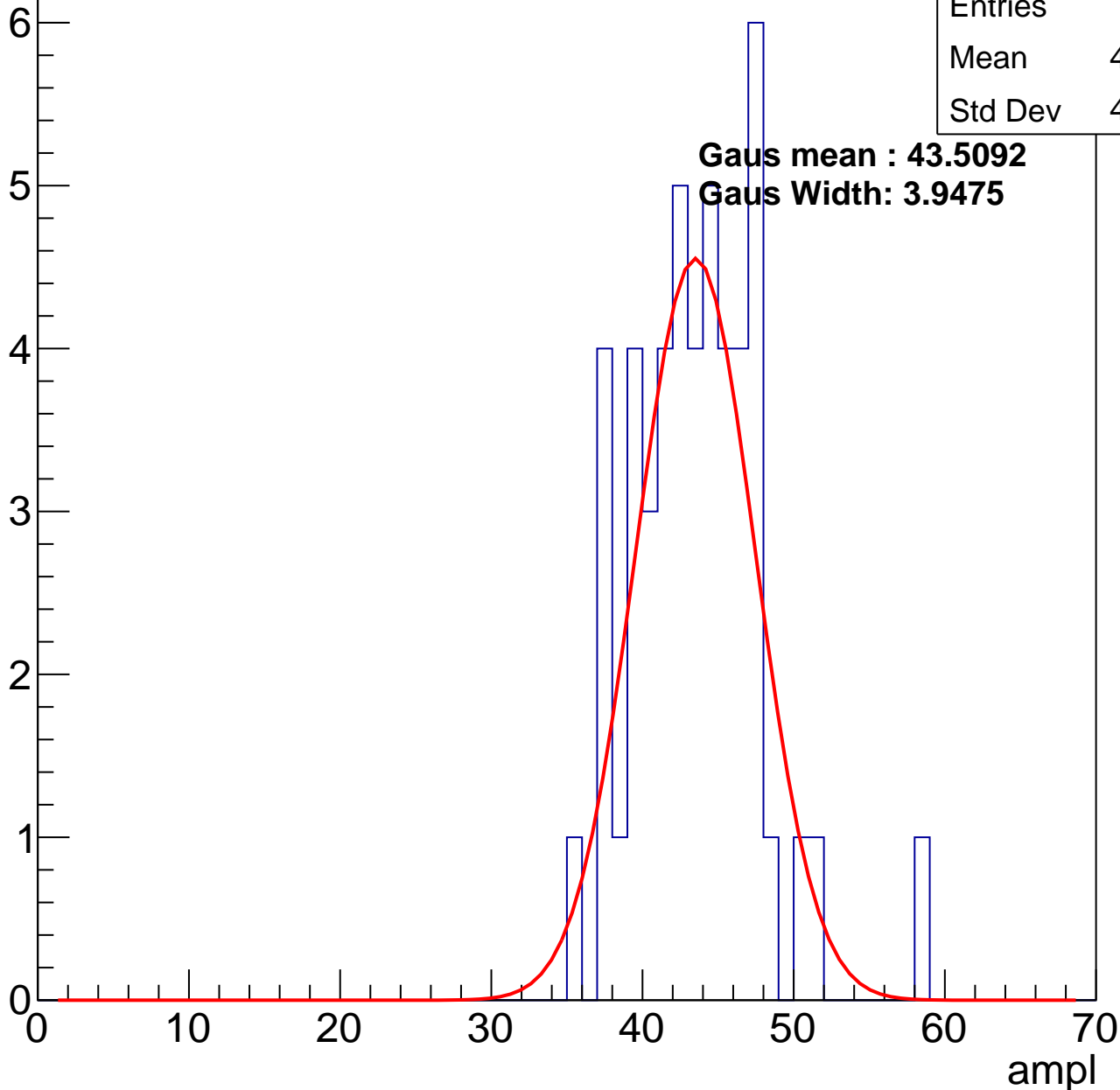
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	49
Mean	43.18
Std Dev	4.188

**Gaus mean : 43.5092**

**Gaus Width: 3.9475**

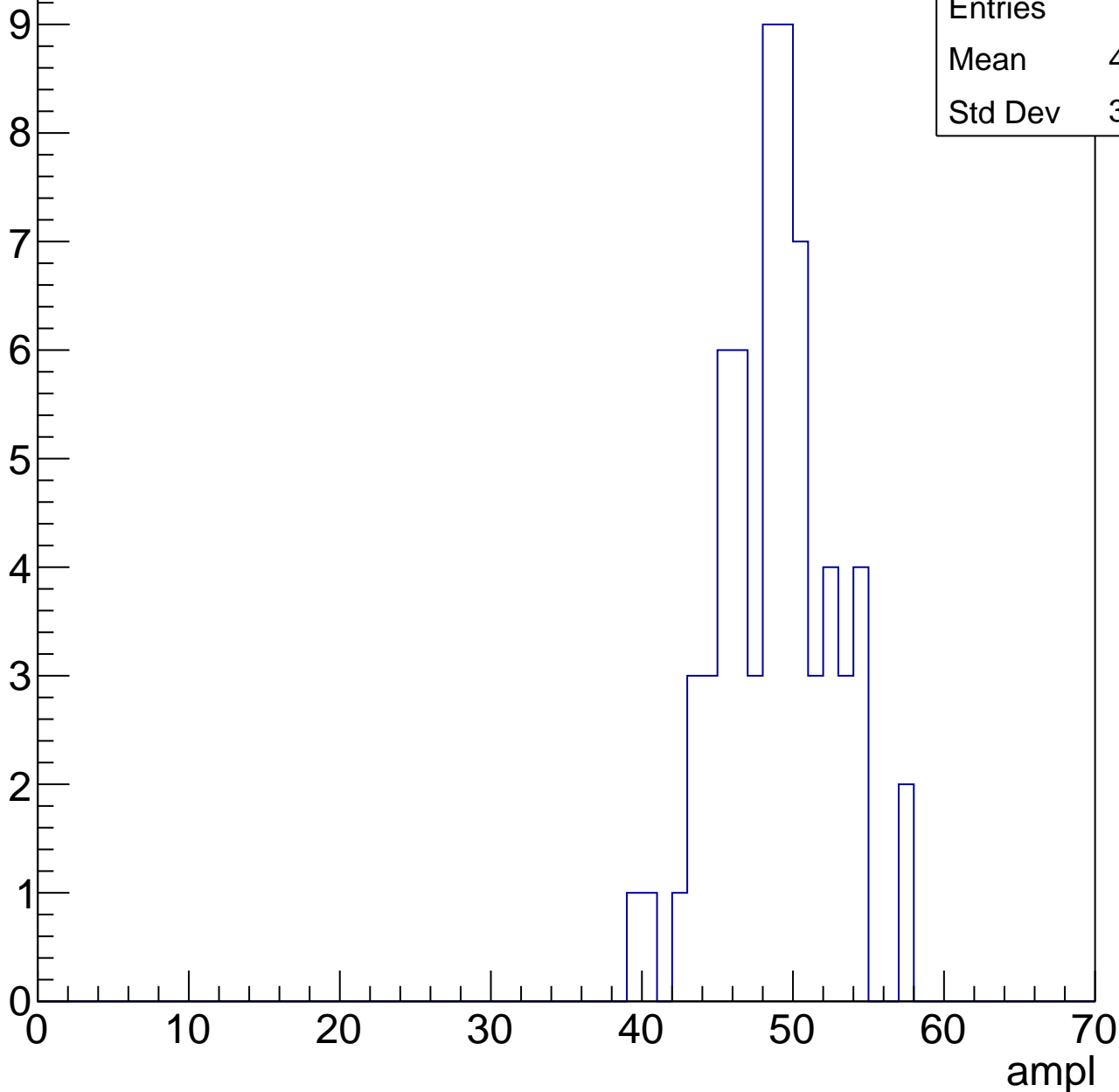


# B1L102S, U16-ch109, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	48.34
Std Dev	3.693

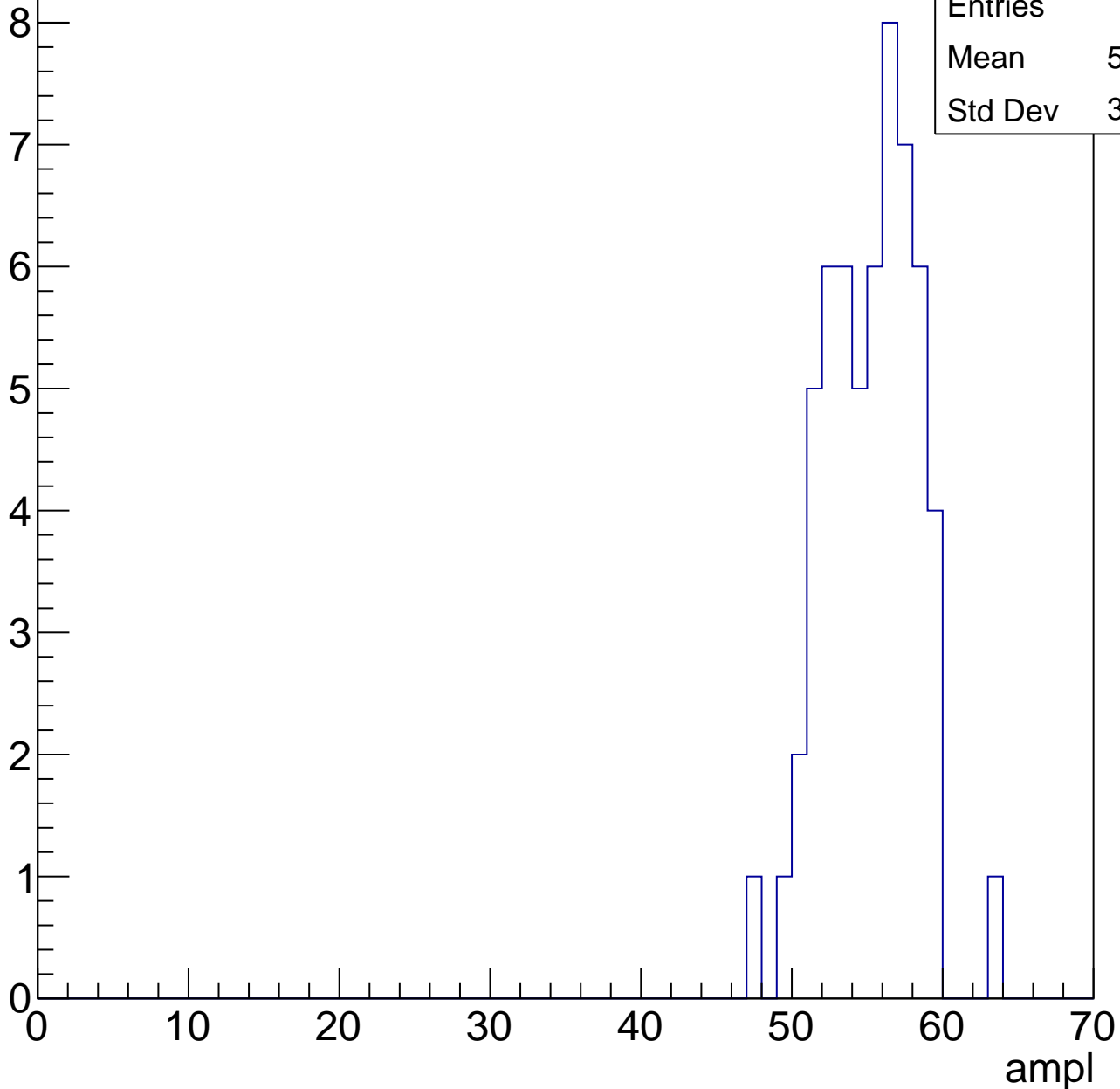


# B1L102S, U16-ch109, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	54.74
Std Dev	3.015

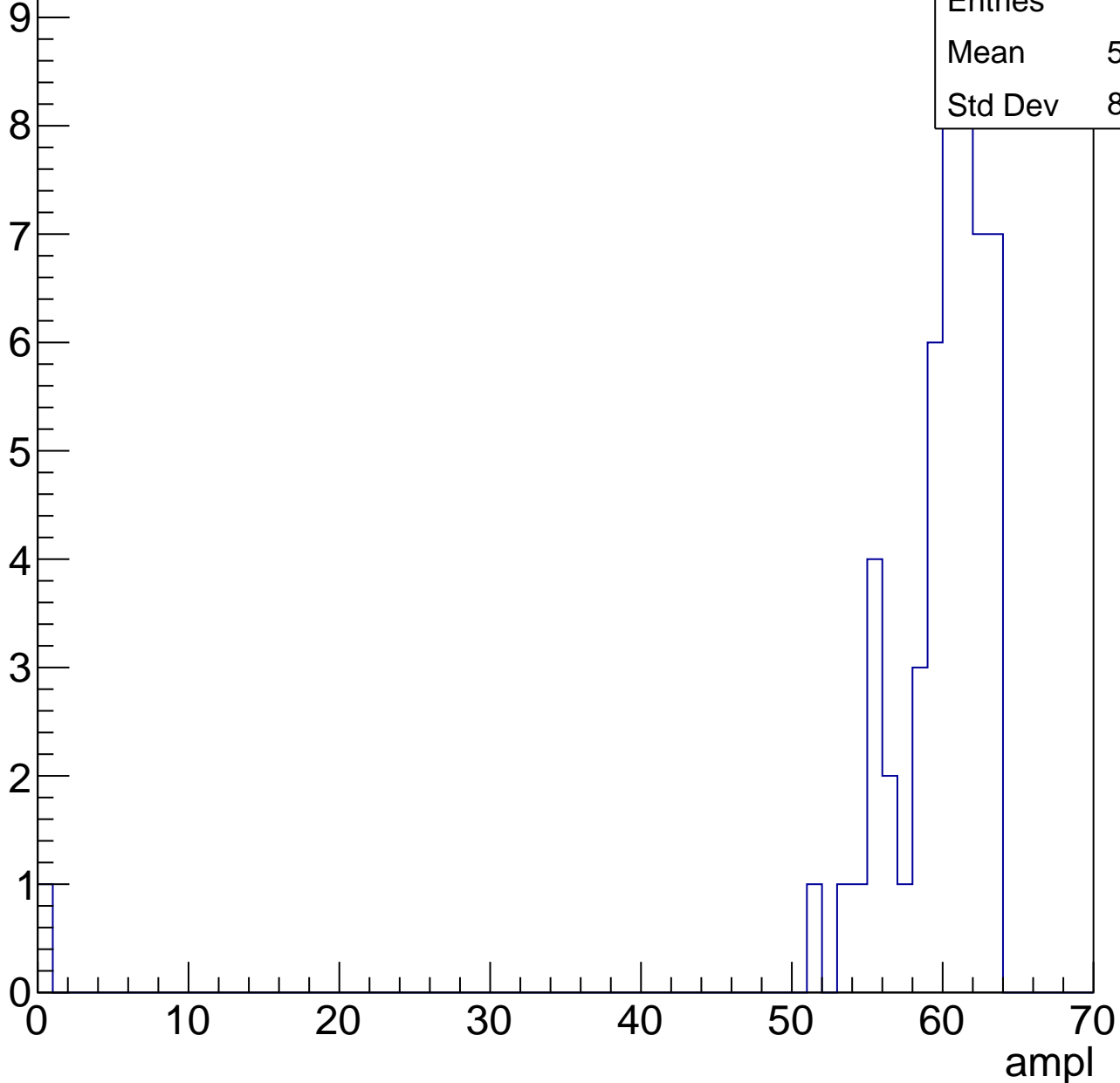


# B1L102S, U16-ch109, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	52
Mean	58.44
Std Dev	8.659



# B1L102S, U16-ch109, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

3

2.5

2

1.5

1

0.5

0

0

10

20

30

40

50

60

70

ampl

Entries

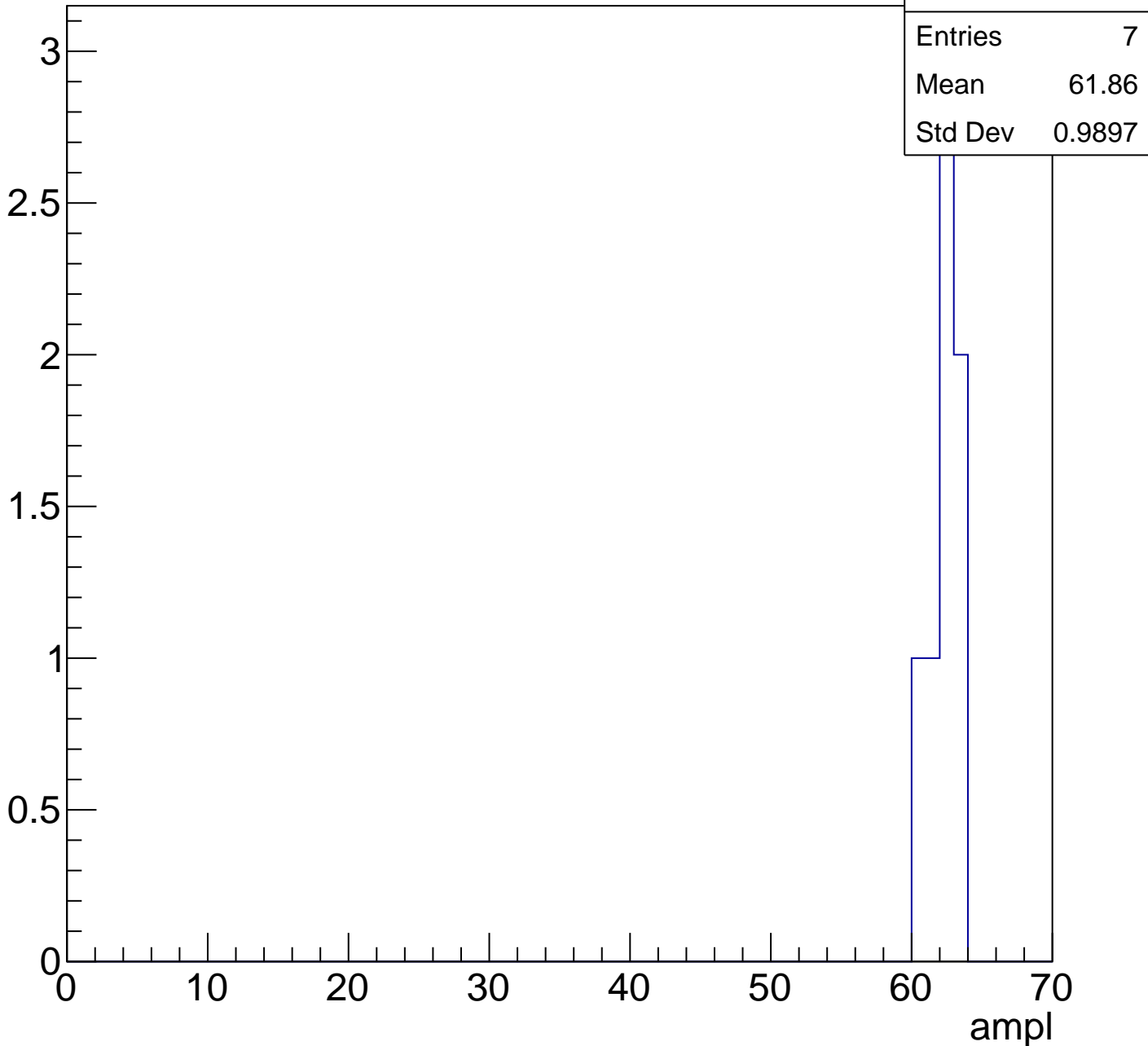
7

Mean

61.86

Std Dev

0.9897

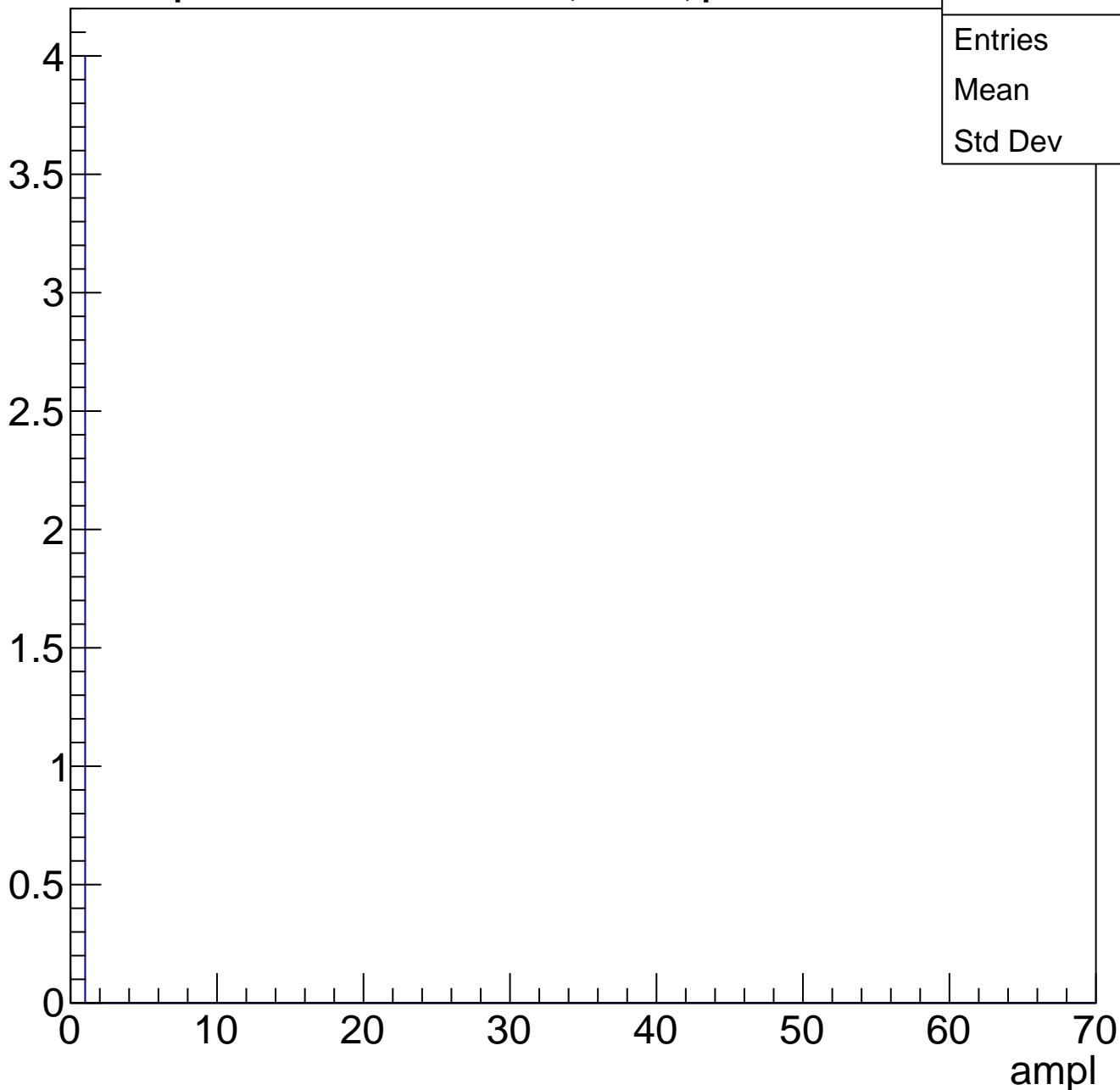




# B1L102S, U16-ch109, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	4
Mean	0
Std Dev	0

# B1L102S, U16-ch110, adc0

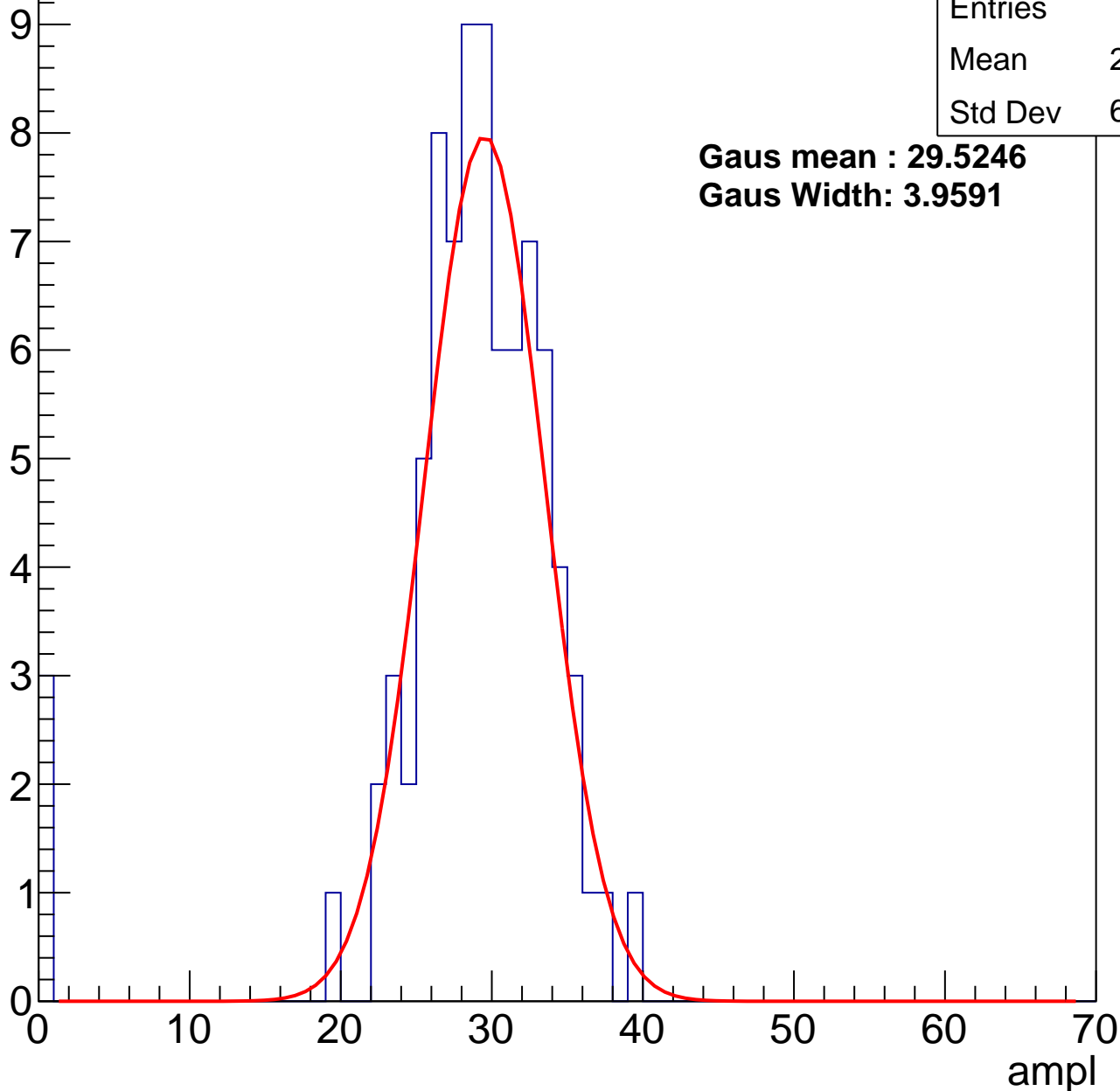
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	28.05
Std Dev	6.548

**Gaus mean : 29.5246**

**Gaus Width: 3.9591**



# B1L102S, U16-ch110, adc1

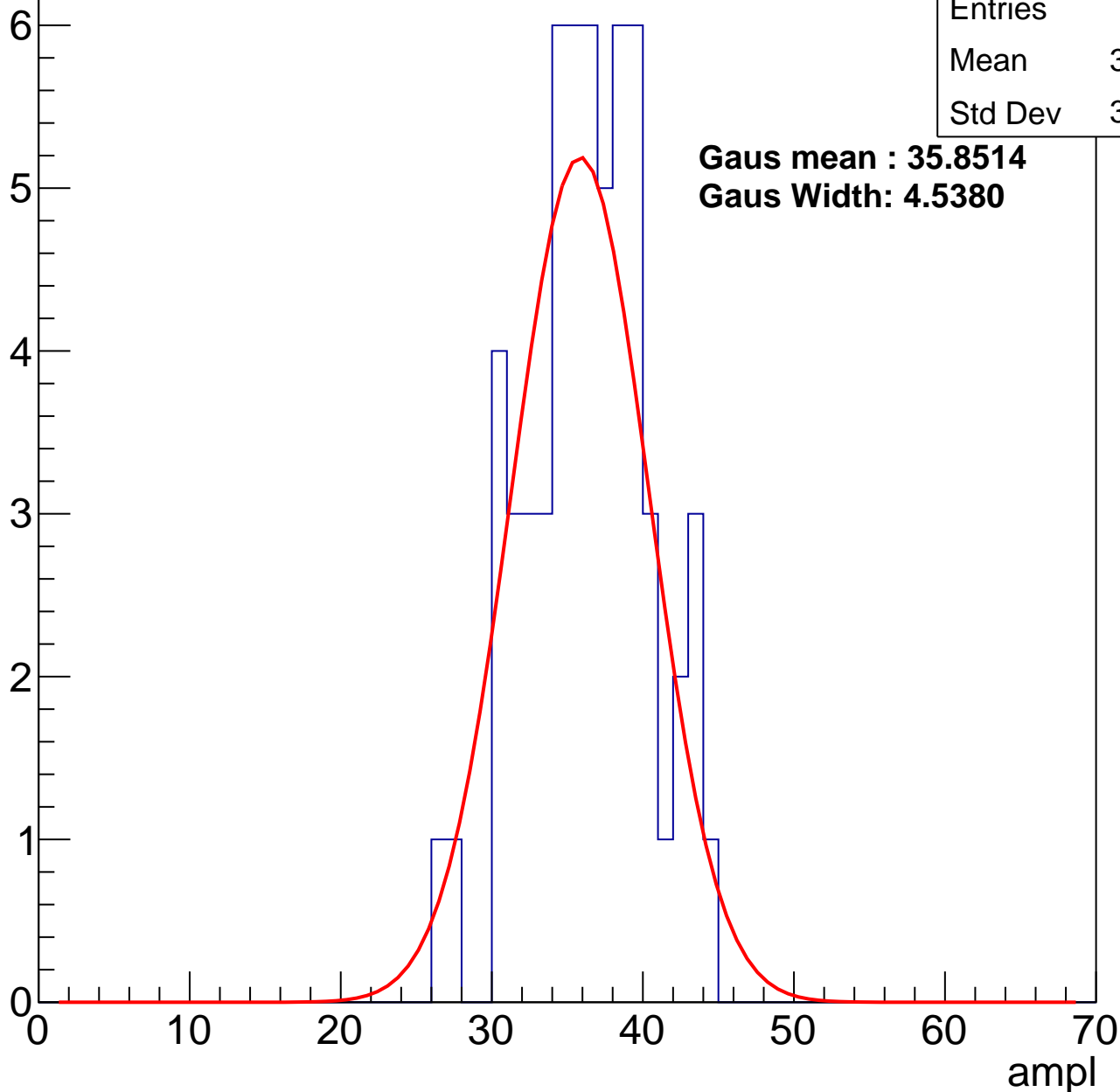
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	35.93
Std Dev	3.966

**Gaus mean : 35.8514**

**Gaus Width: 4.5380**



# B1L102S, U16-ch110, adc2

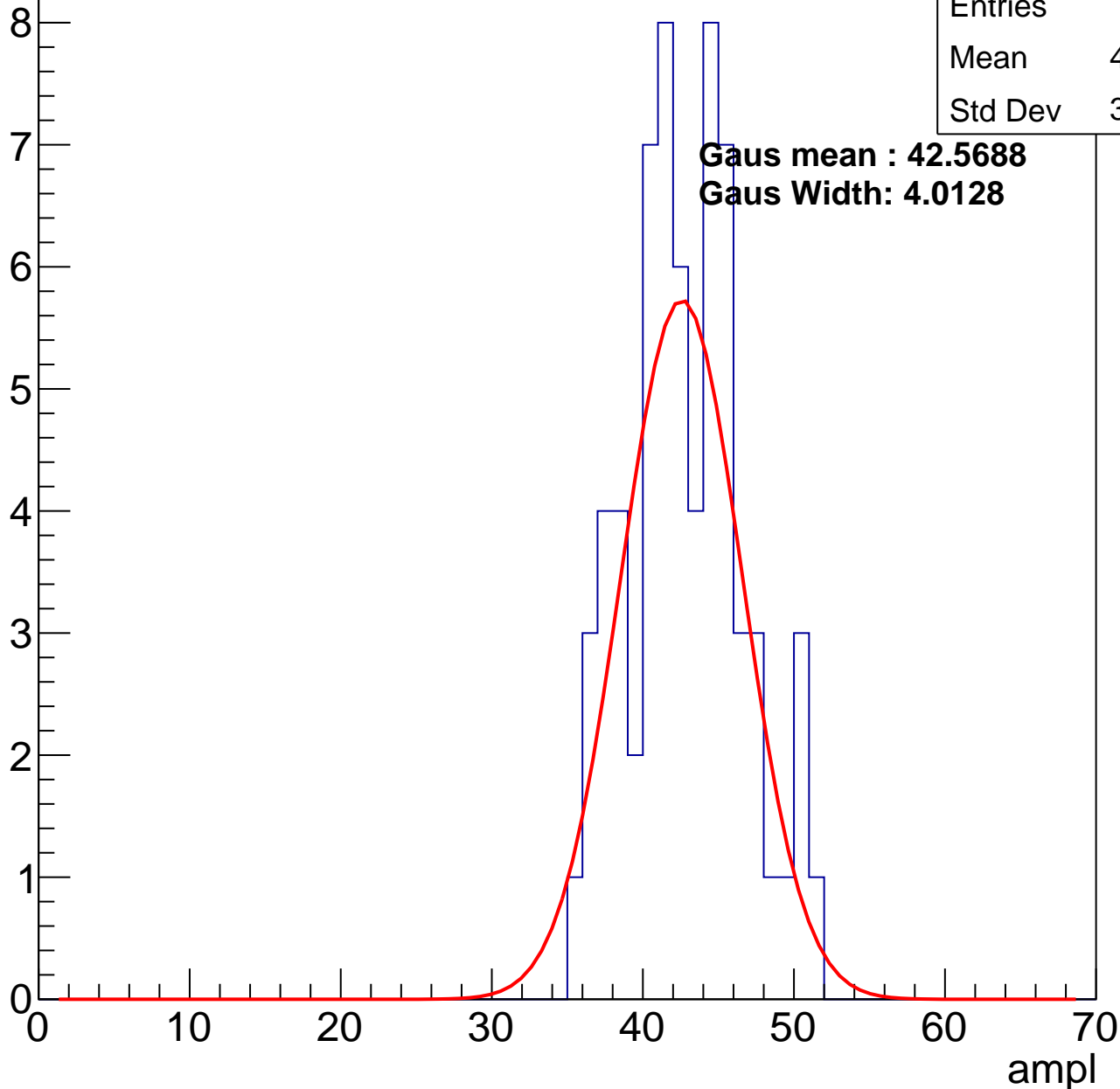
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	42.38
Std Dev	3.785

**Gaus mean : 42.5688**

**Gaus Width: 4.0128**

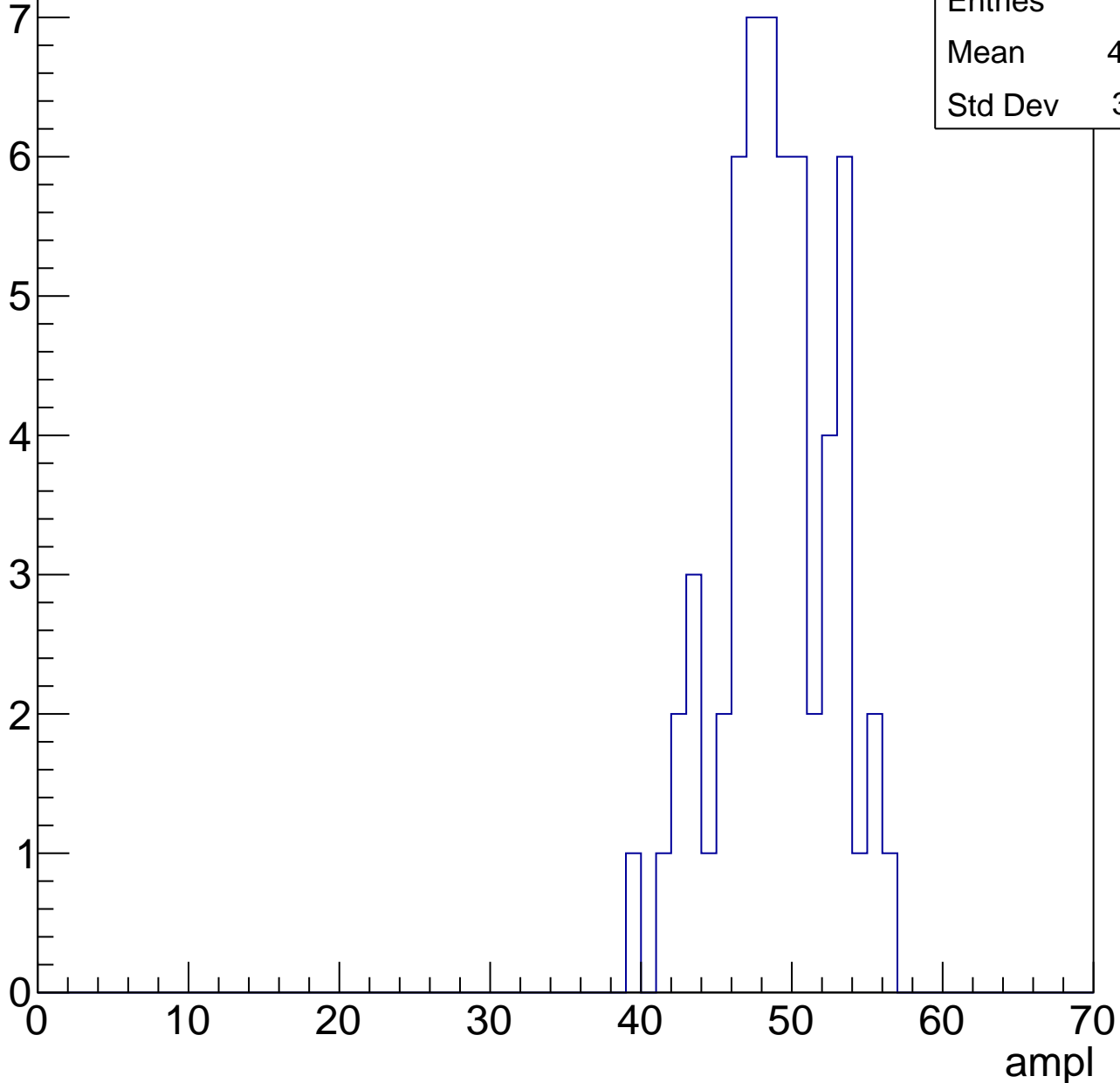


# B1L102S, U16-ch110, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	48.45
Std Dev	3.691

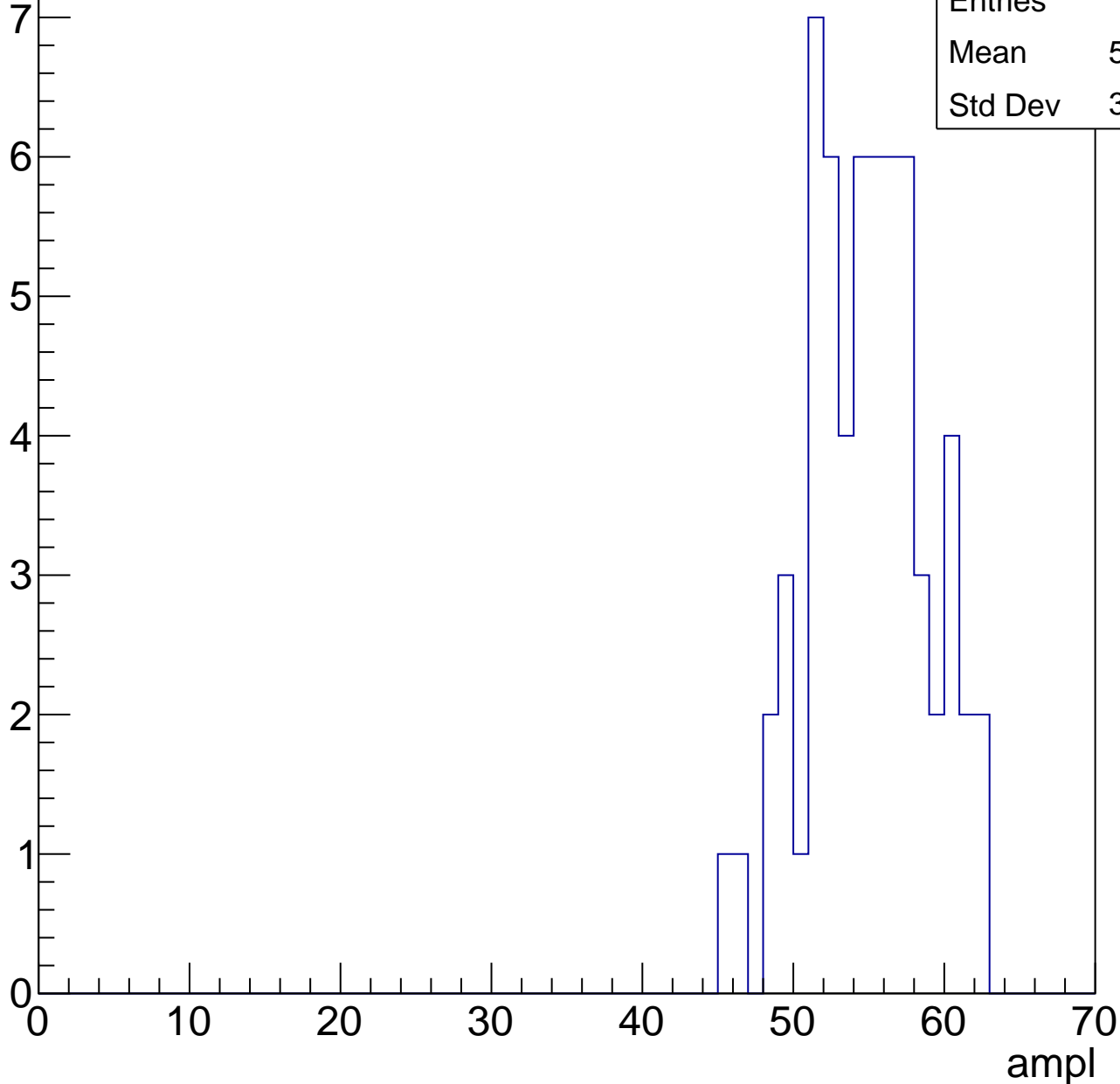


# B1L102S, U16-ch110, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	54.44
Std Dev	3.892



# B1L102S, U16-ch110, adc5

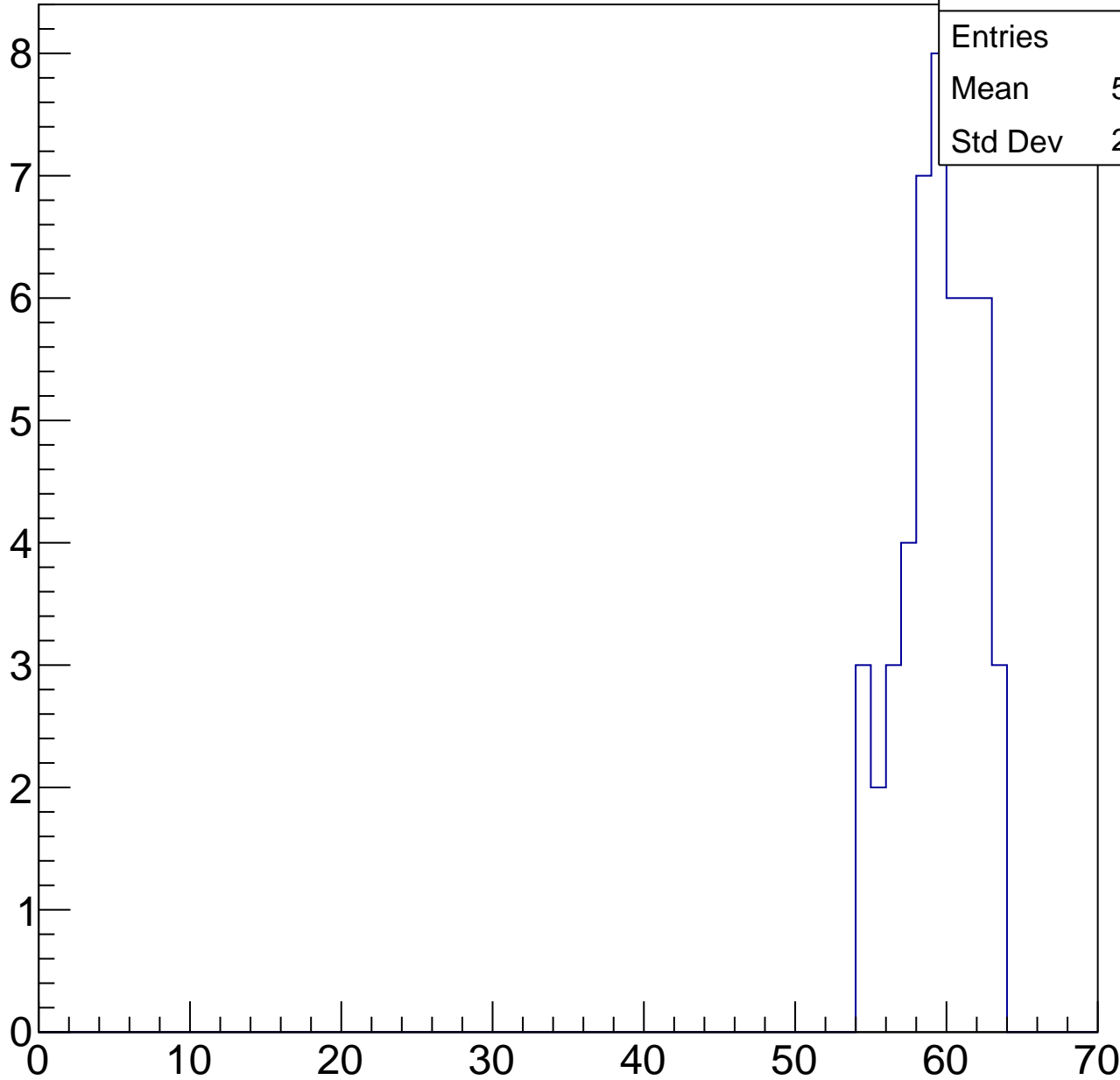
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

8  
7  
6  
5  
4  
3  
2  
1  
0

Entries	48
Mean	59.02
Std Dev	2.454

ampl

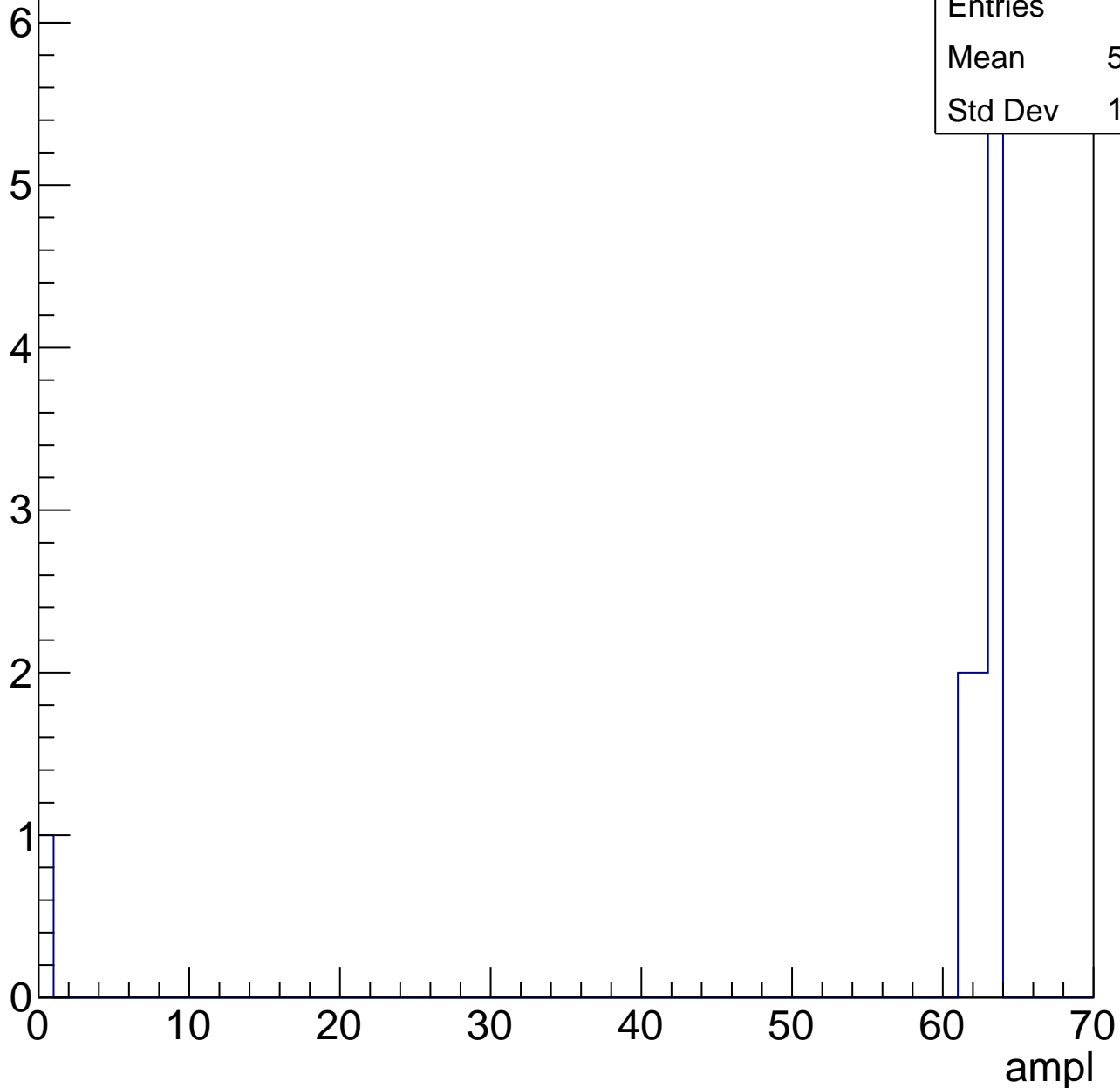


# B1L102S, U16-ch110, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	11
Mean	56.73
Std Dev	17.95





# B1L102S, U16-ch110, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	21
Std Dev	29.7

# B1L102S, U16-ch111, adc0

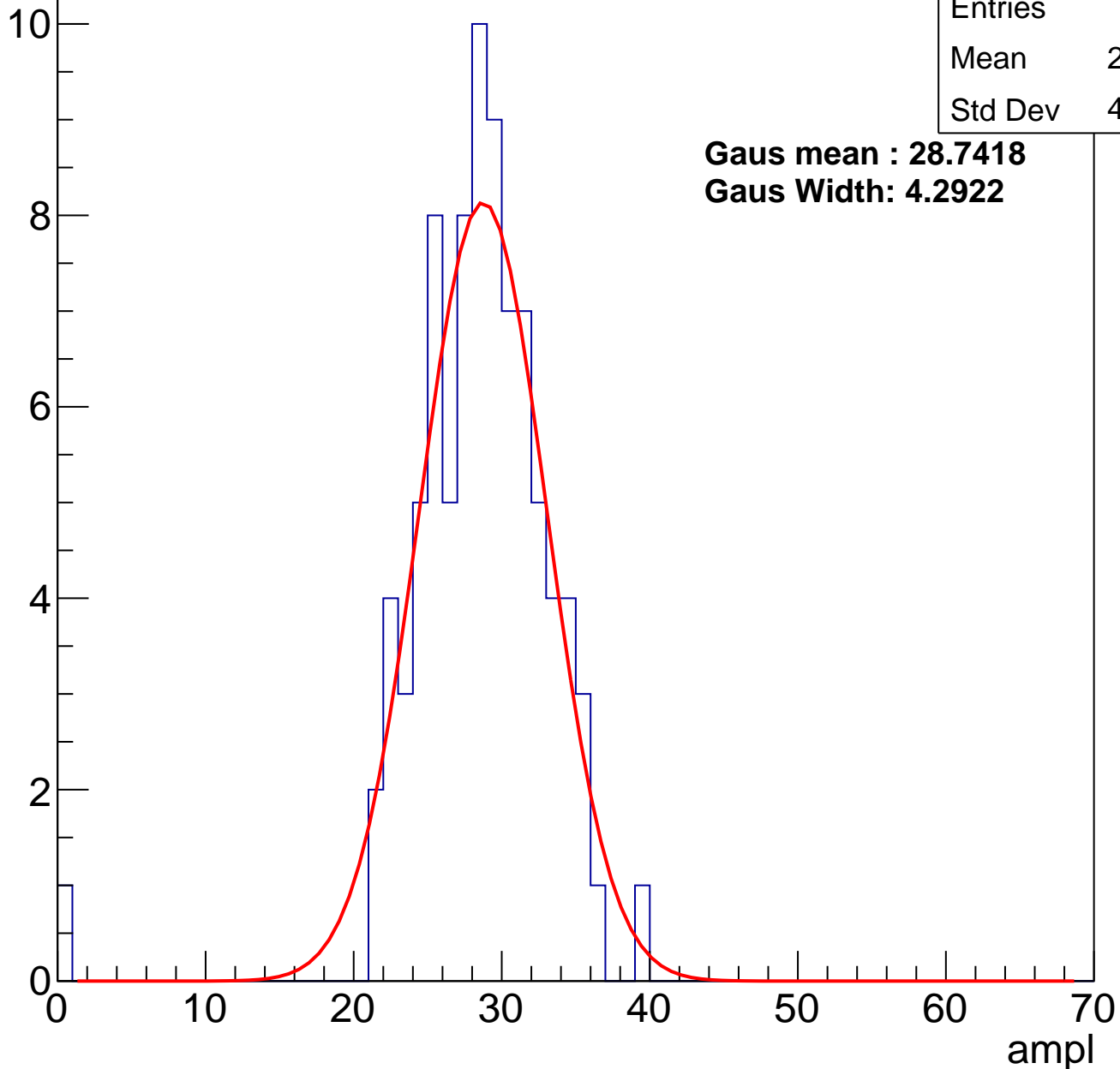
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	87
Mean	28.06
Std Dev	4.838

**Gaus mean : 28.7418**

**Gaus Width: 4.2922**

Entry



# B1L102S, U16-ch111, adc1

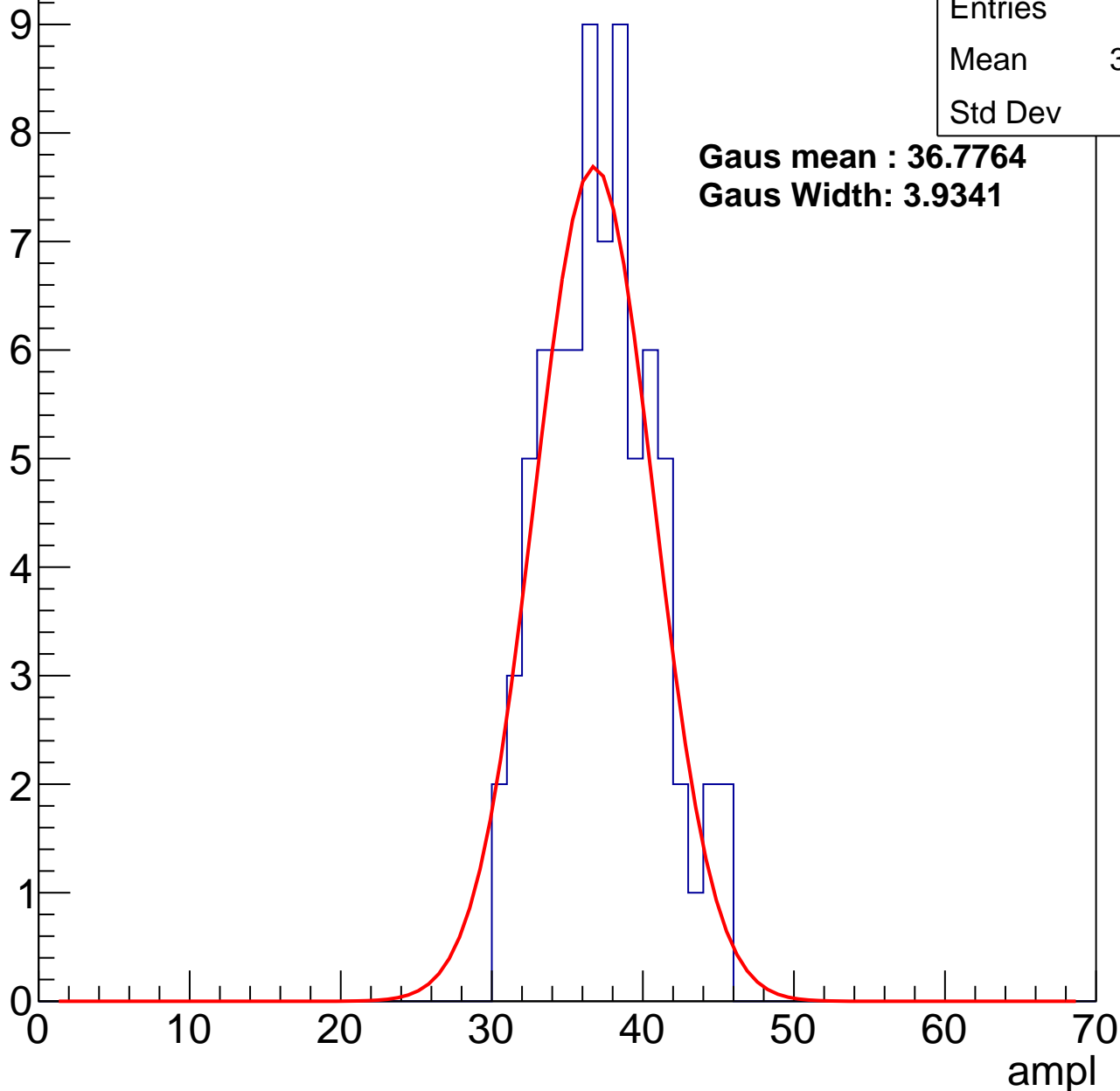
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	36.78
Std Dev	3.6

**Gaus mean : 36.7764**

**Gaus Width: 3.9341**



# B1L102S, U16-ch111, adc2

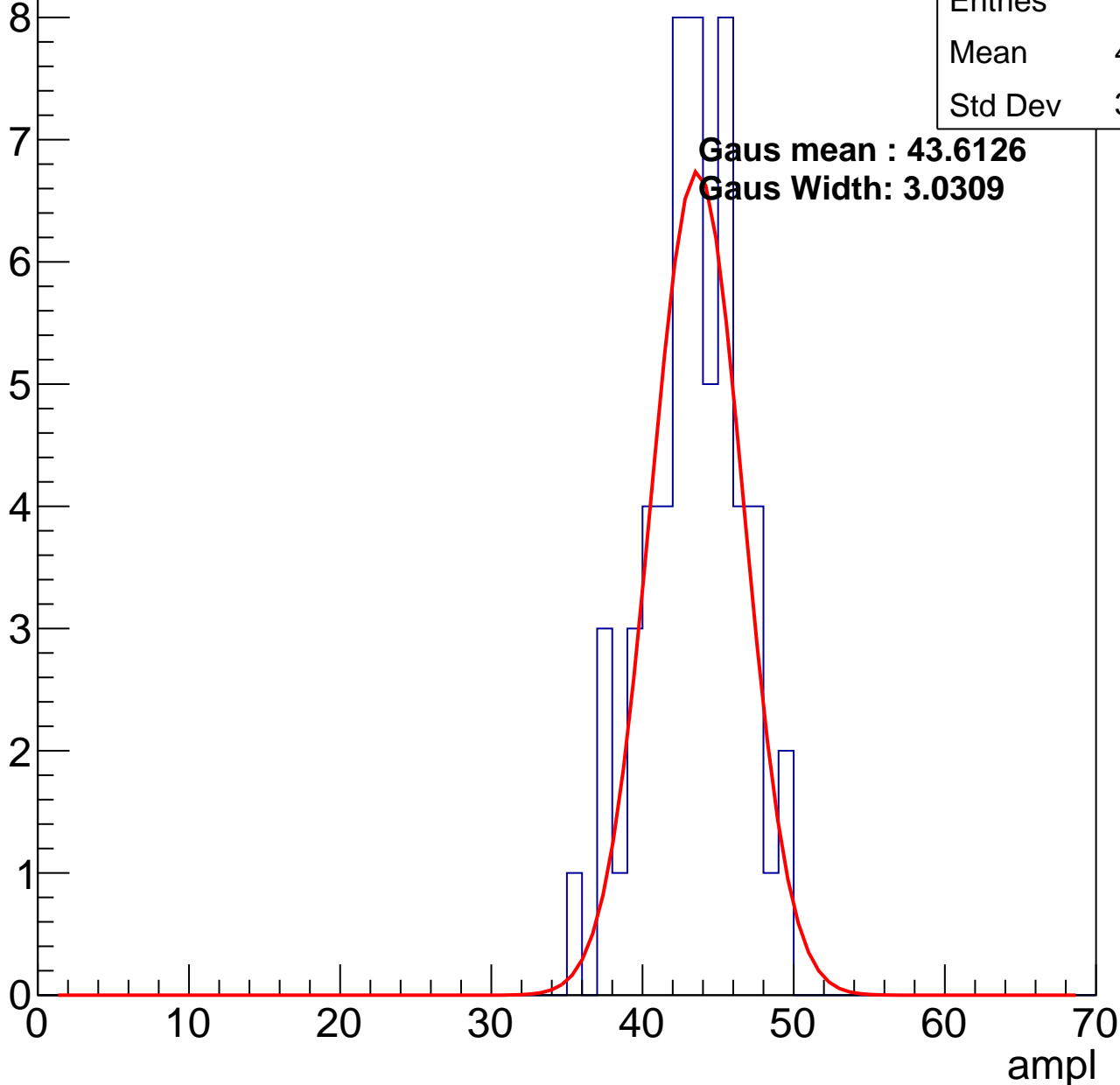
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	42.91
Std Dev	3.101

**Gaus mean : 43.6126**

**Gaus Width: 3.0309**

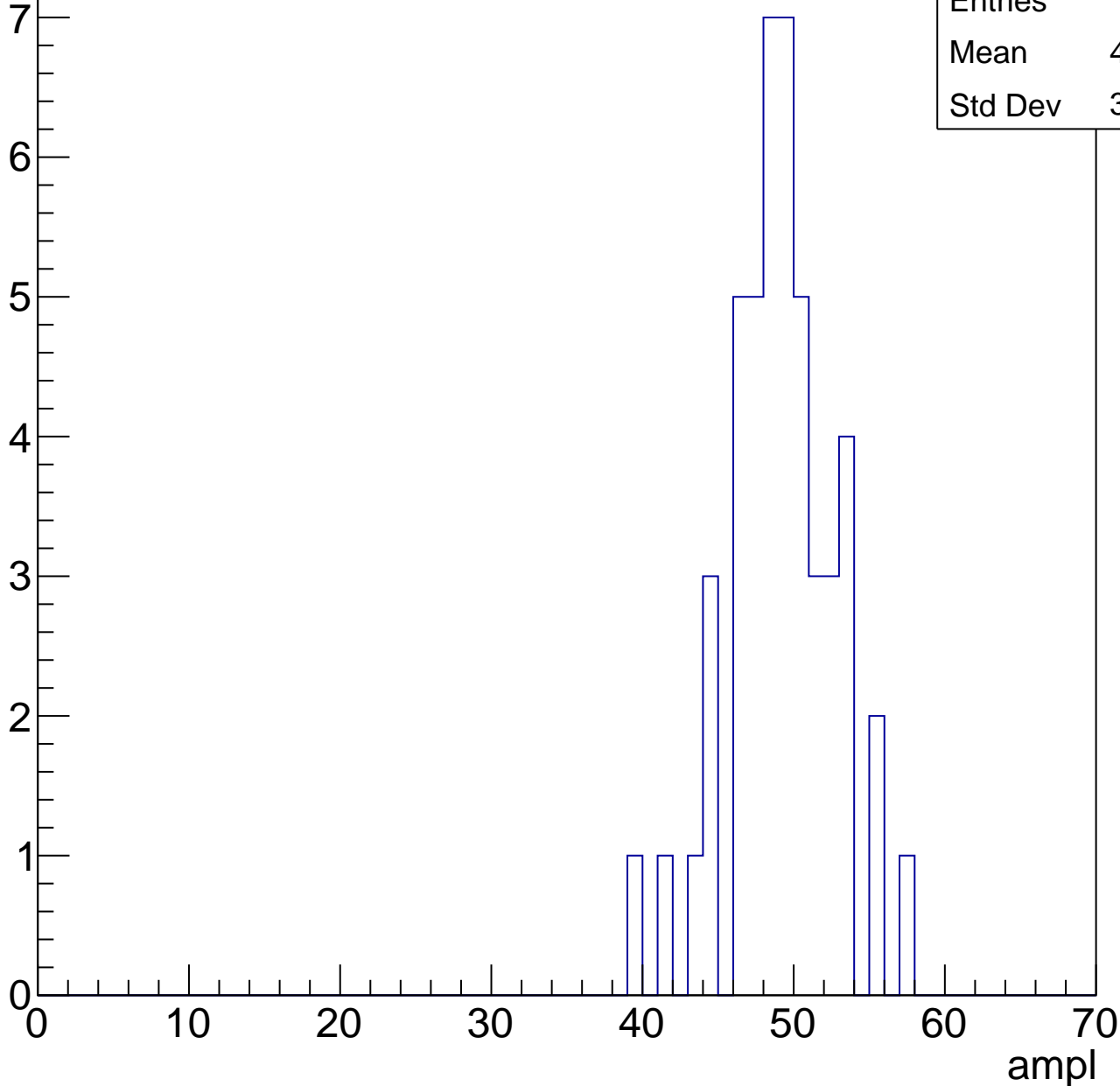


# B1L102S, U16-ch111, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	48.69
Std Dev	3.495



# B1L102S, U16-ch111, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

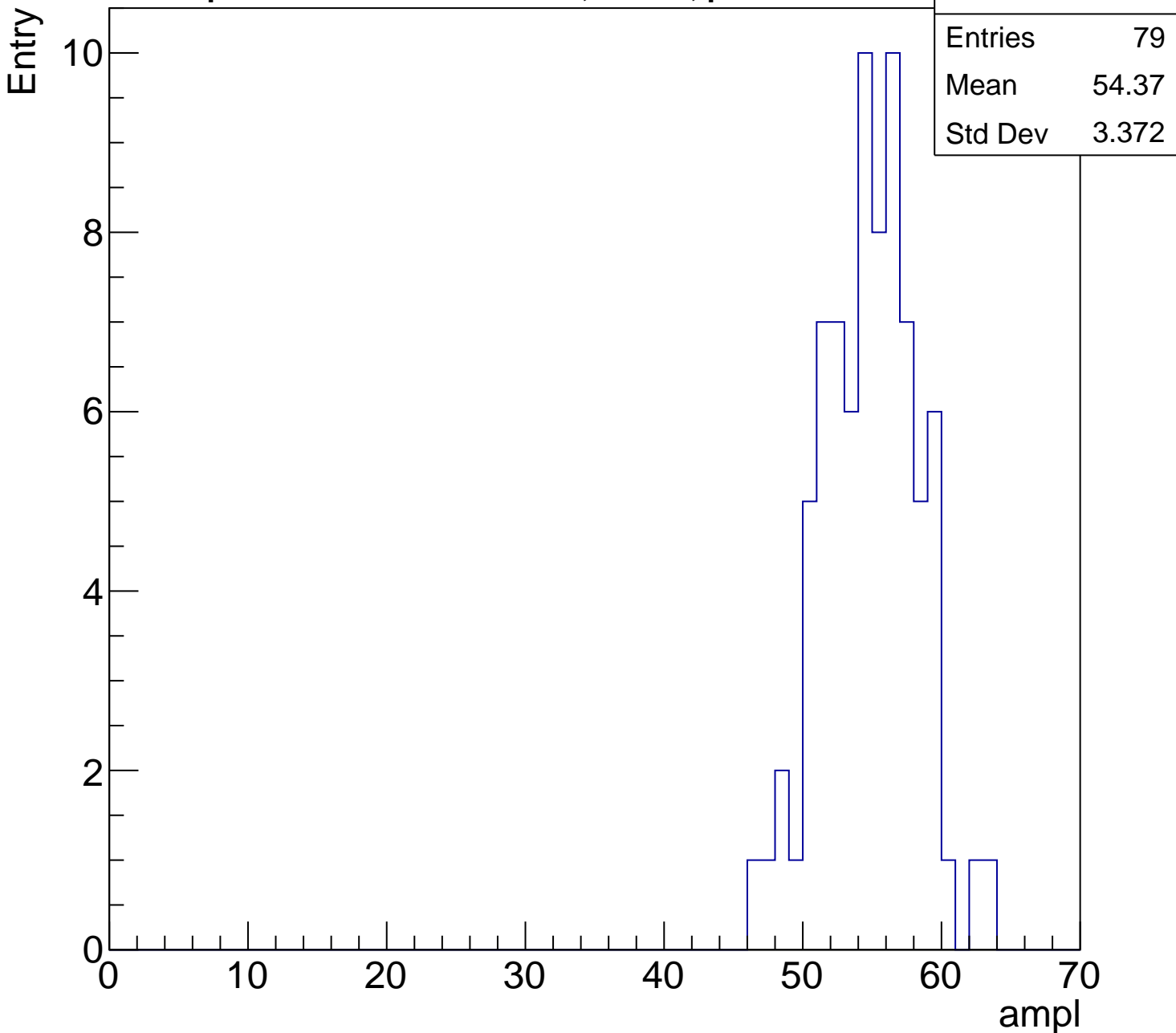
Entries	79
Mean	54.37
Std Dev	3.372

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

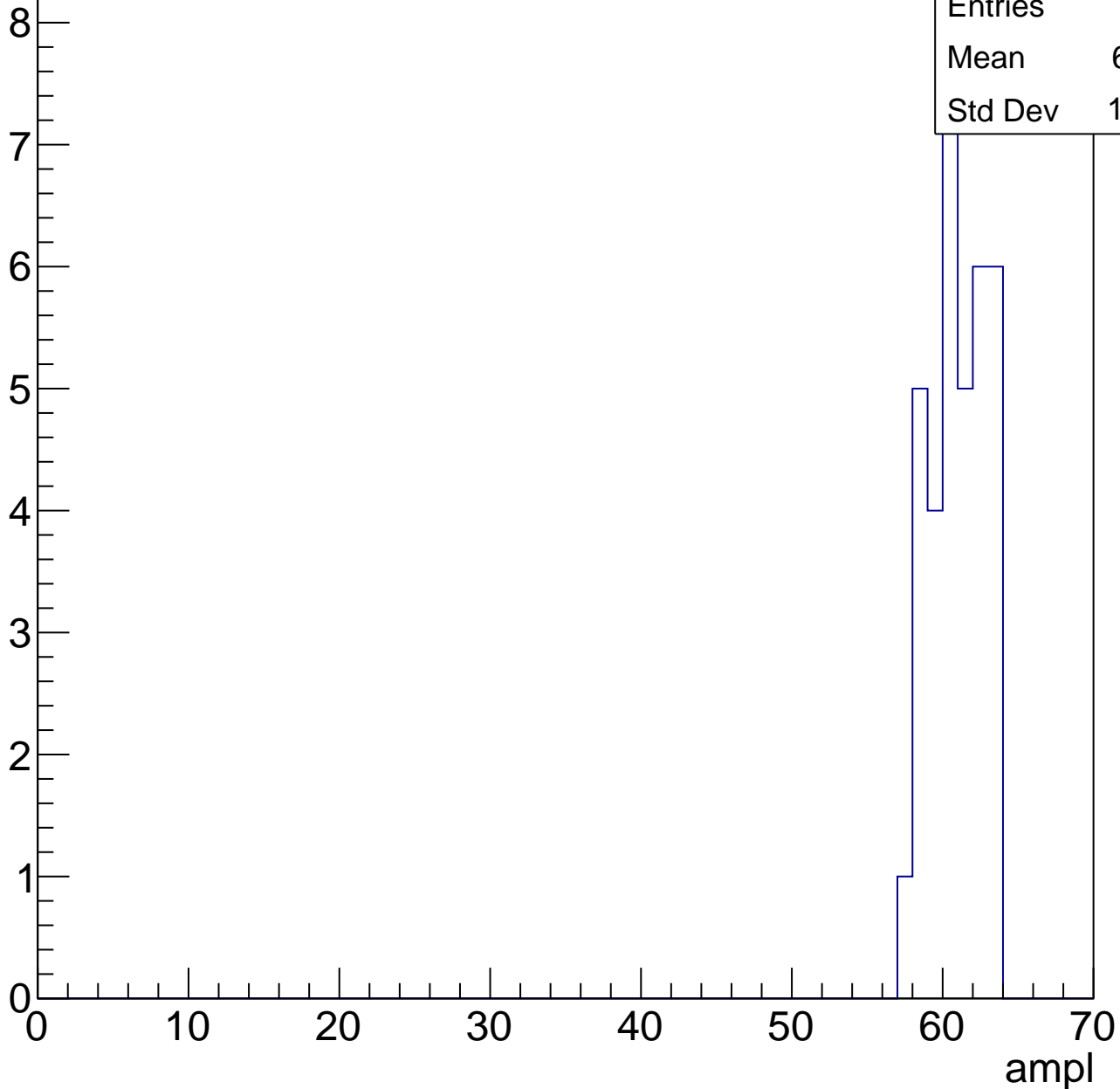


# B1L102S, U16-ch111, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	35
Mean	60.51
Std Dev	1.746

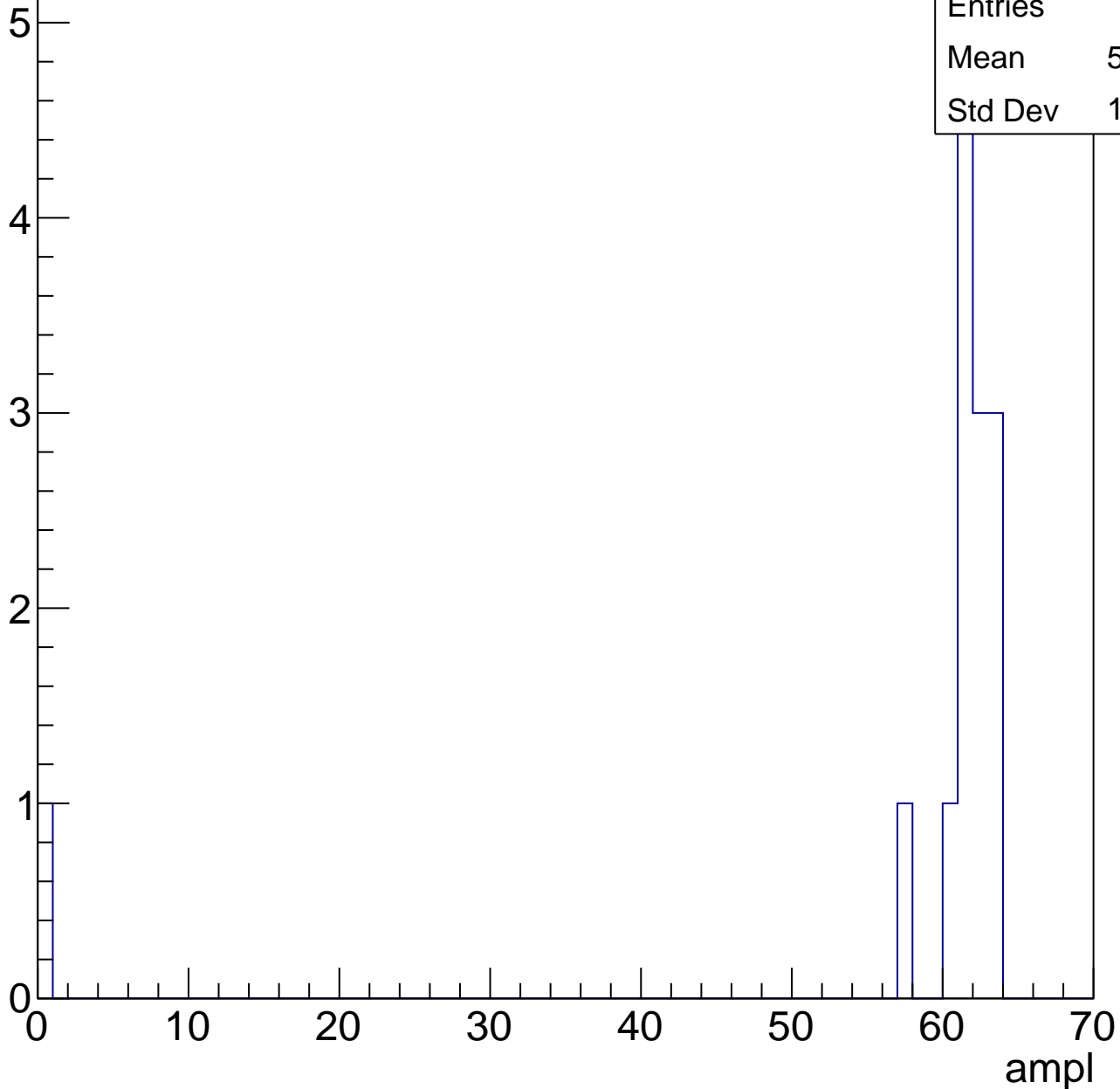


# B1L102S, U16-ch111, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	14
Mean	56.93
Std Dev	15.86





# B1L102S, U16-ch111, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U16-ch112, adc0

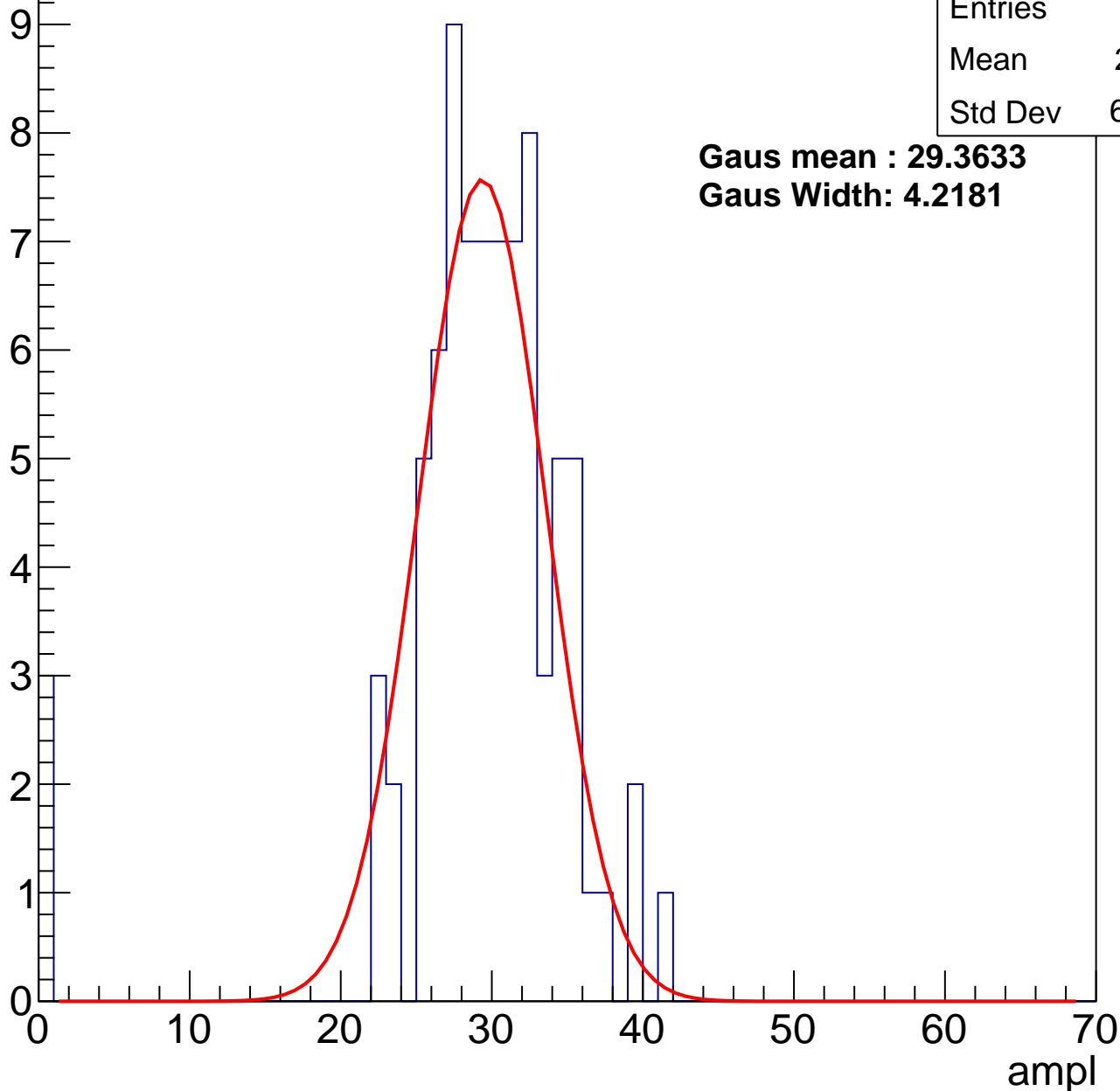
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	28.71
Std Dev	6.833

**Gaus mean : 29.3633**

**Gaus Width: 4.2181**



# B1L102S, U16-ch112, adc1

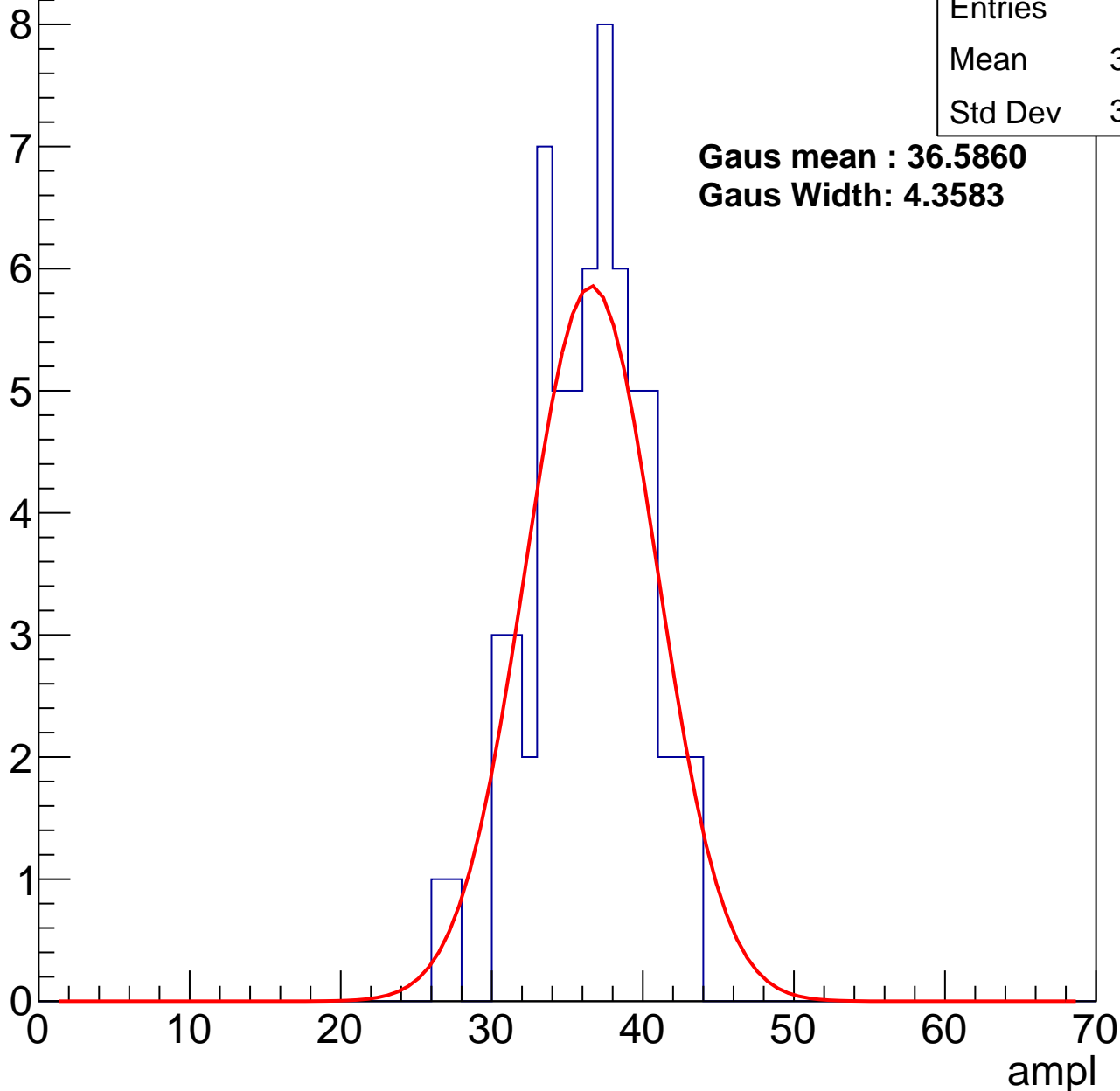
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	35.92
Std Dev	3.696

**Gaus mean : 36.5860**

**Gaus Width: 4.3583**



# B1L102S, U16-ch112, adc2

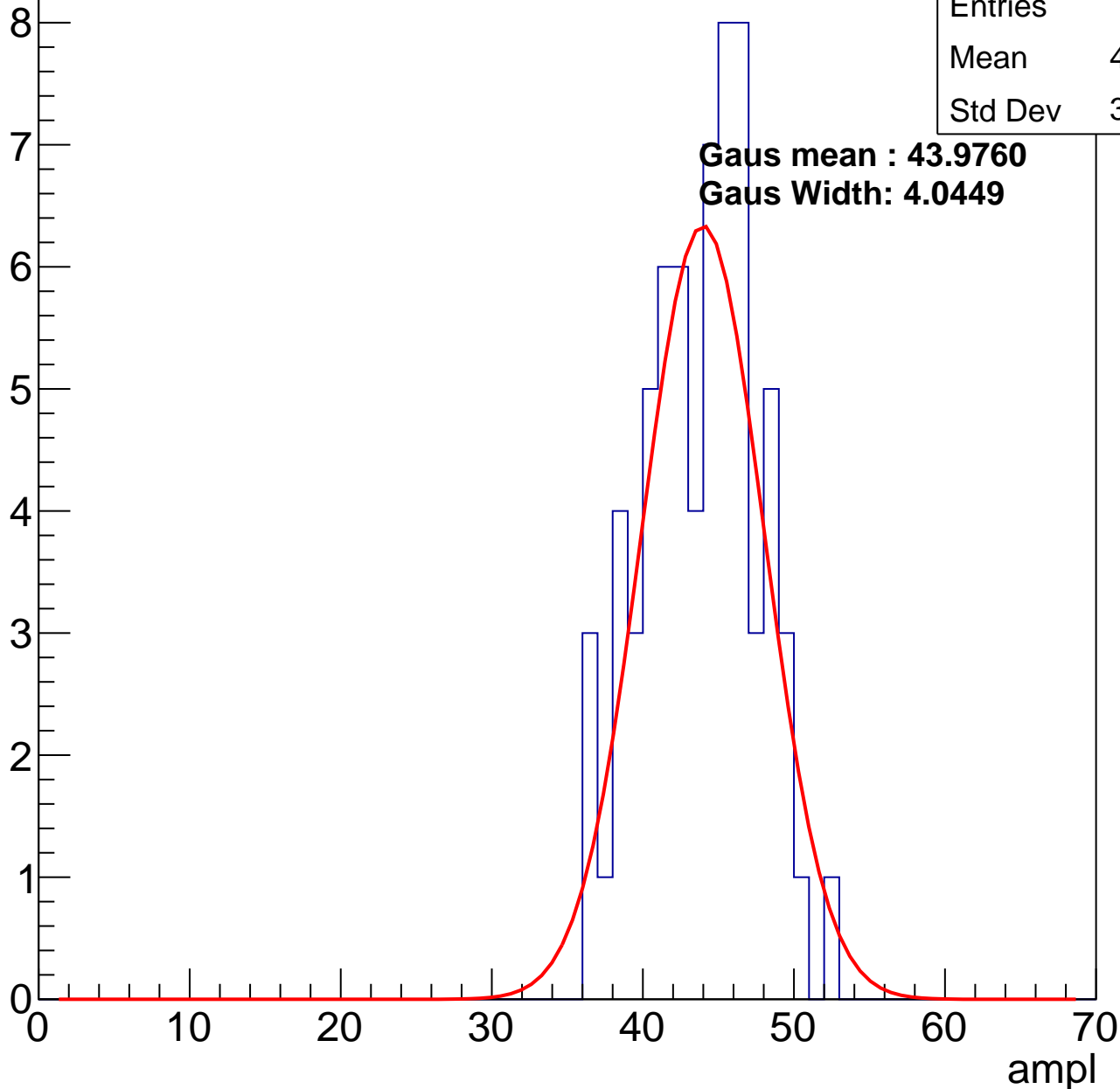
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	43.38
Std Dev	3.674

**Gaus mean : 43.9760**

**Gaus Width: 4.0449**

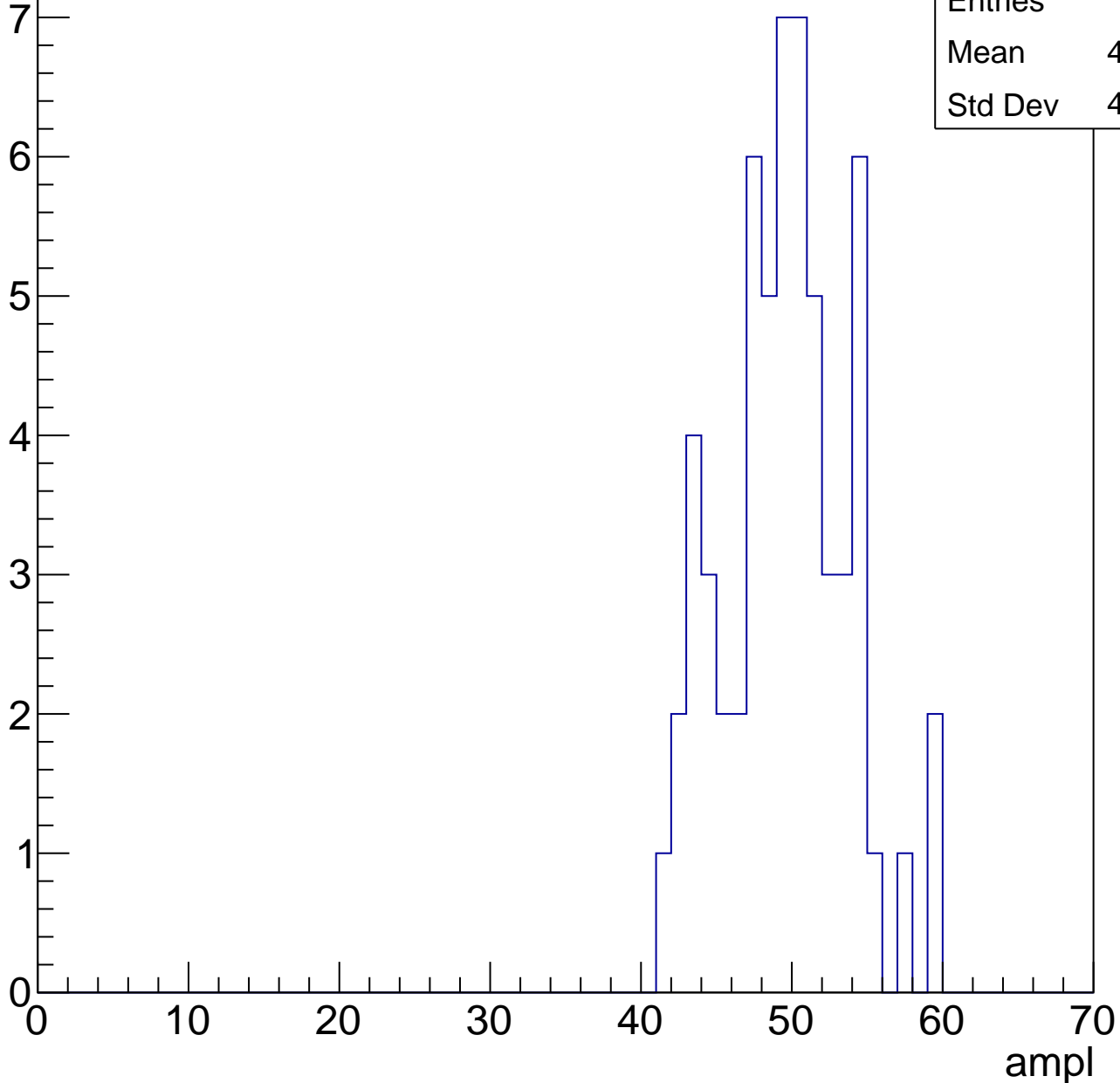


# B1L102S, U16-ch112, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	49.17
Std Dev	4.104

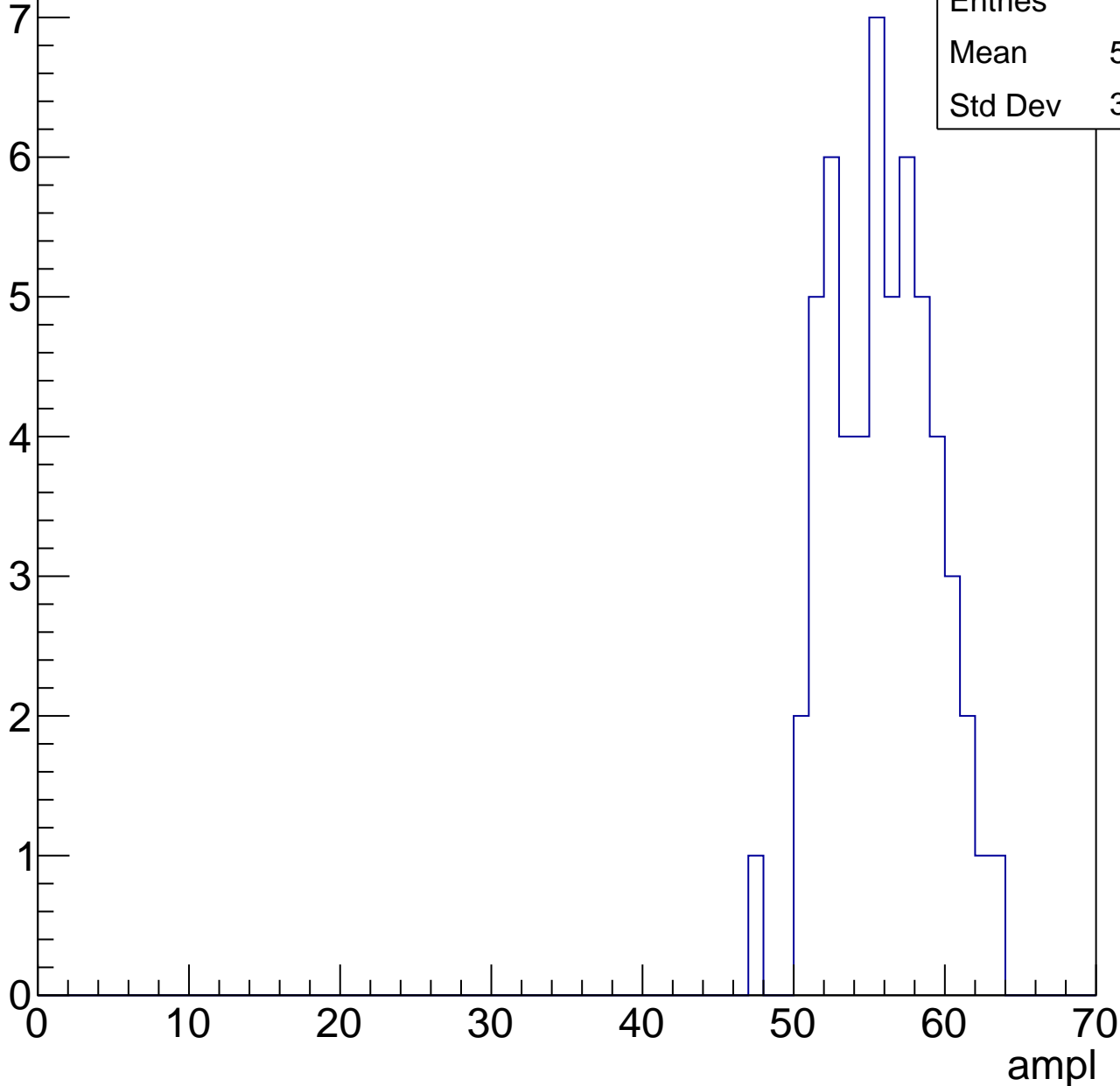


# B1L102S, U16-ch112, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	55.39
Std Dev	3.426

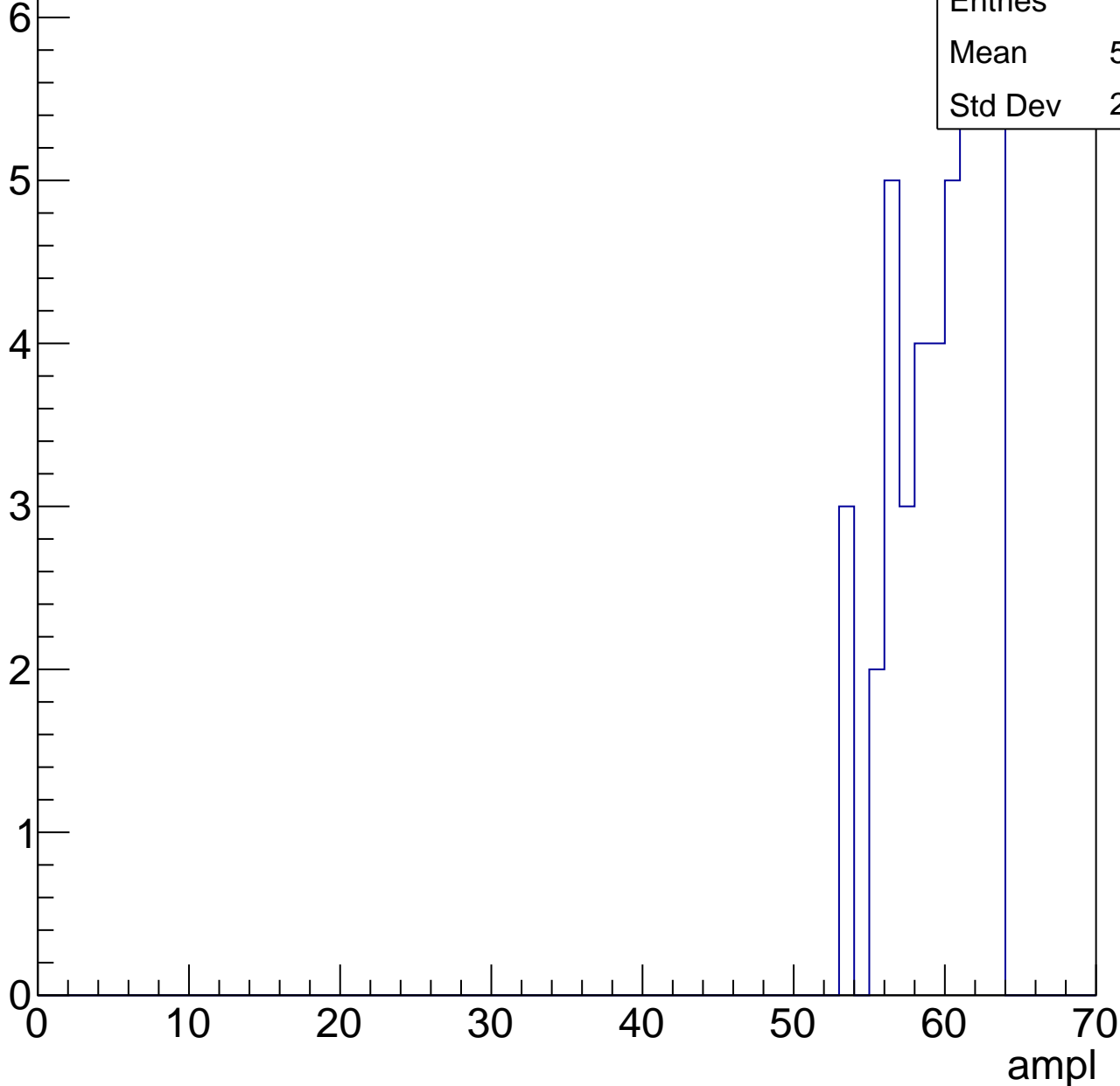


# B1L102S, U16-ch112, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

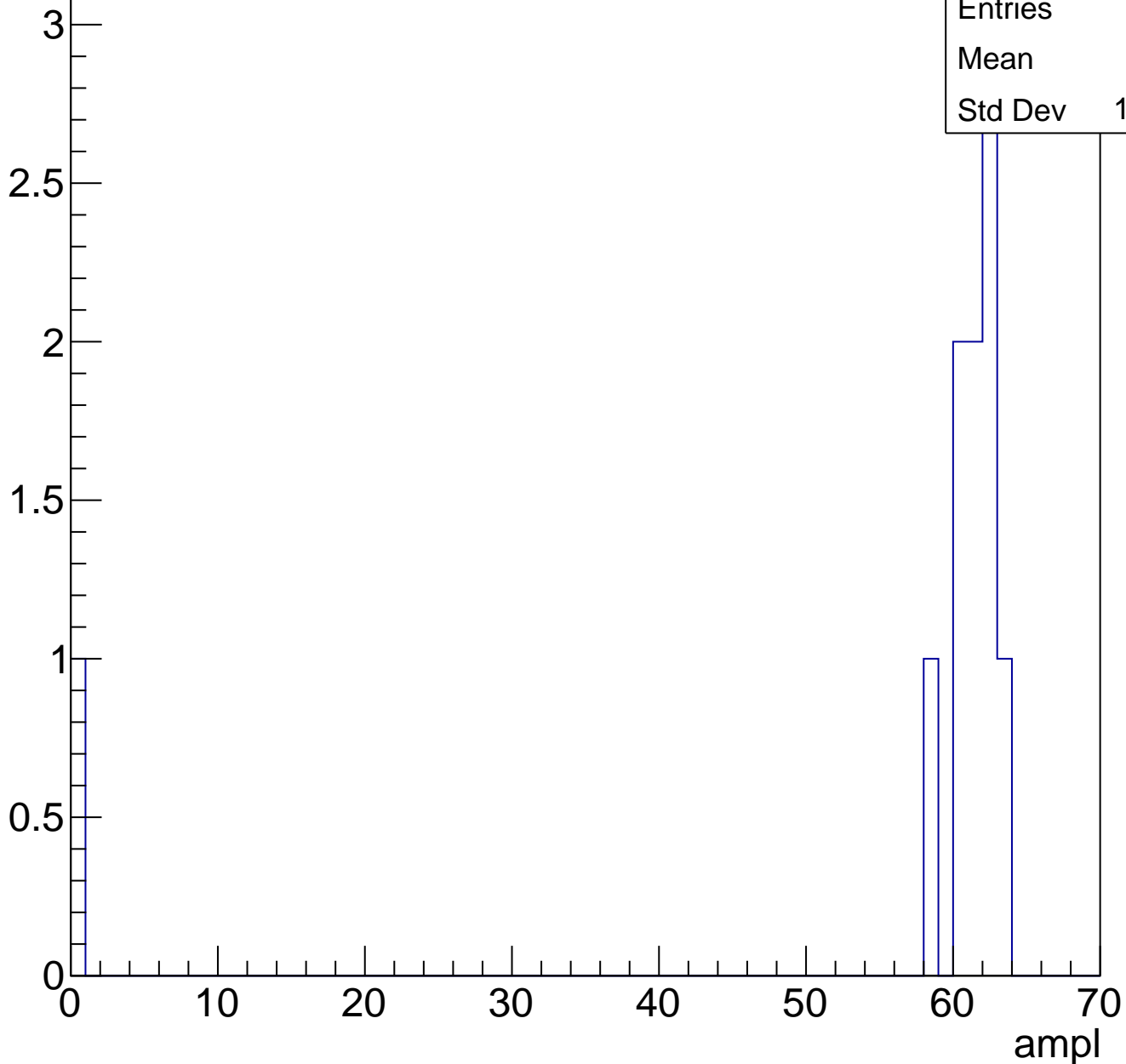
Entries	44
Mean	59.18
Std Dev	2.933



# B1L102S, U16-ch112, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

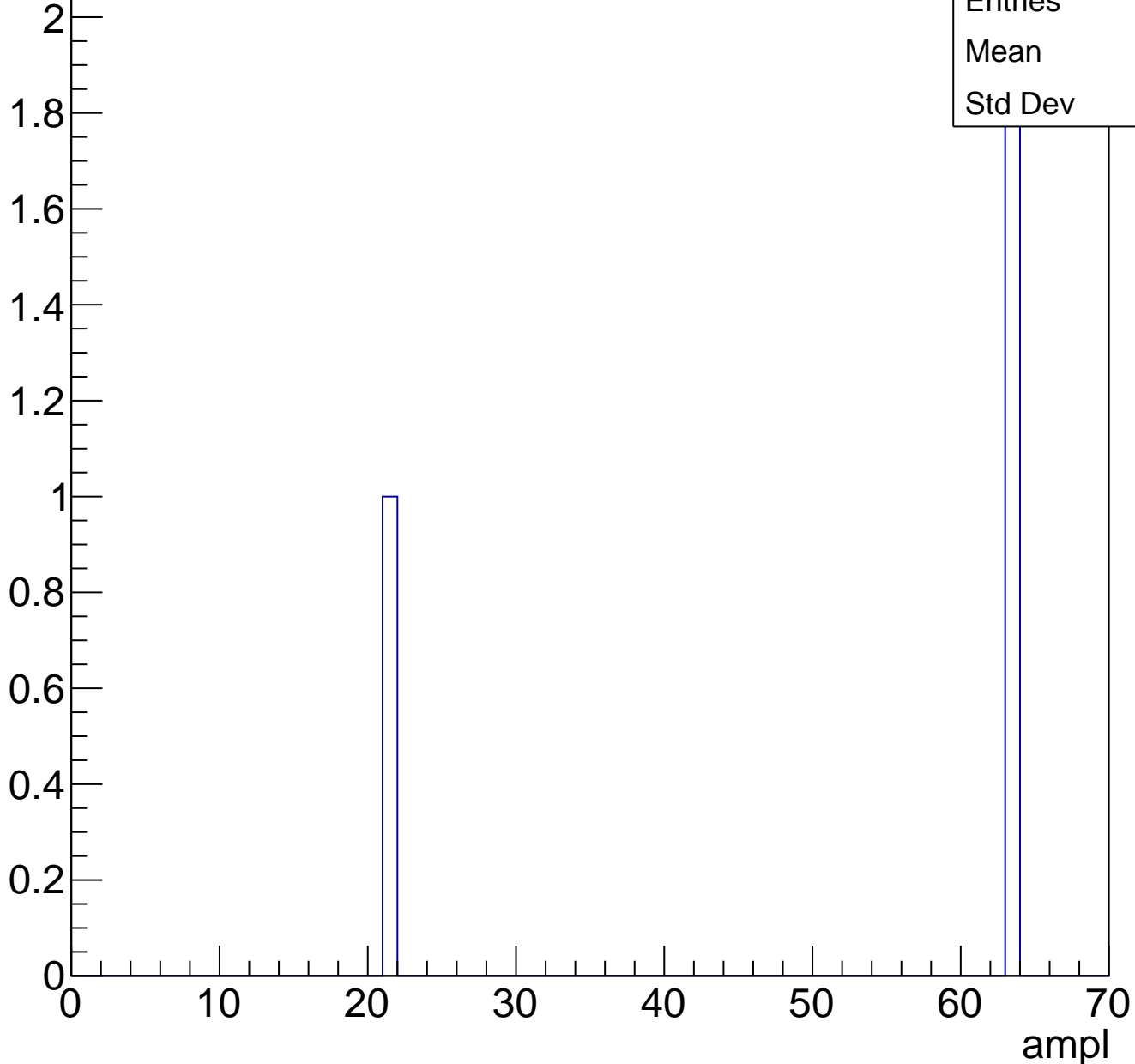




# B1L102S, U16-ch112, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch113, adc0

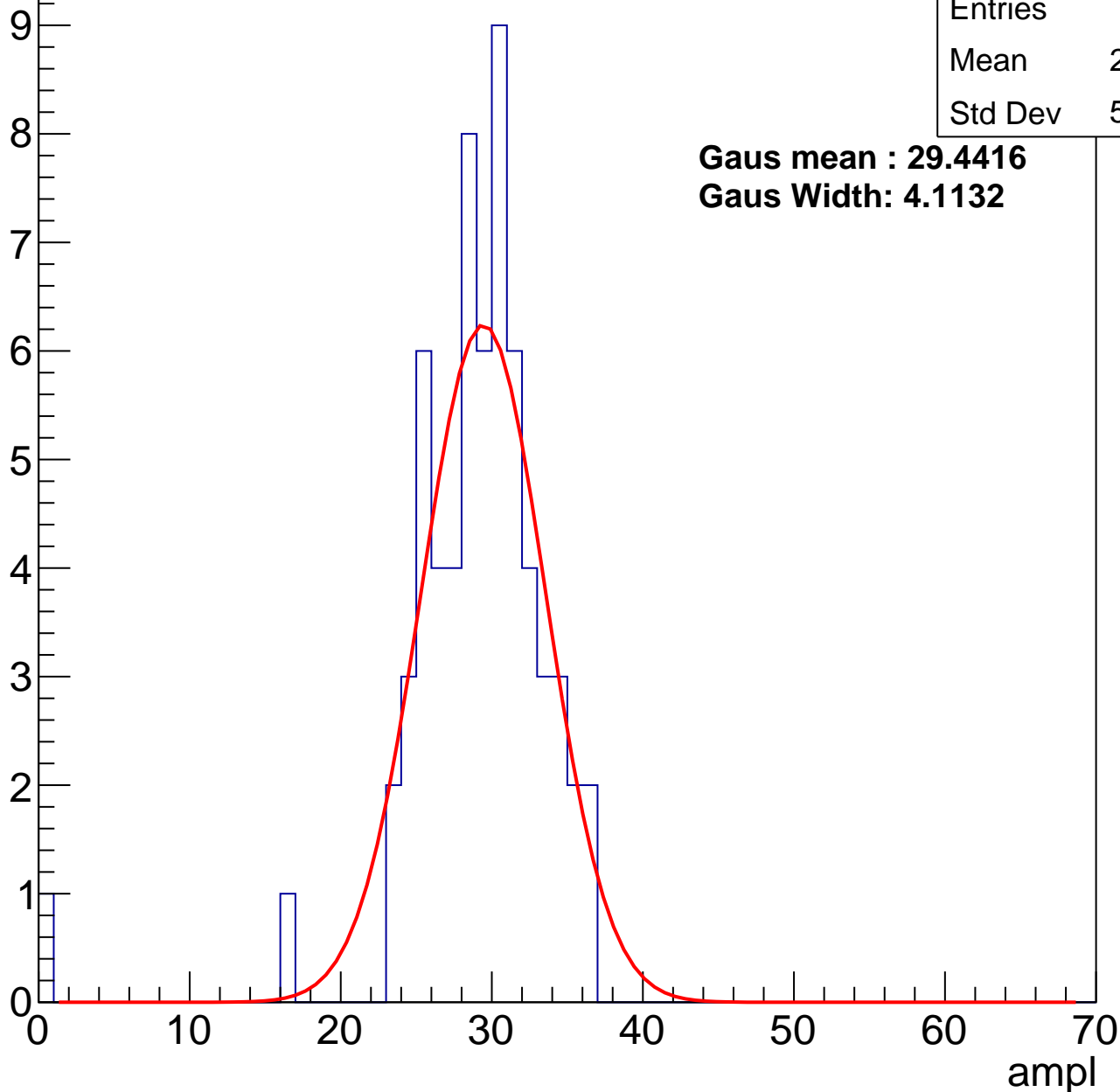
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	28.45
Std Dev	5.087

**Gaus mean : 29.4416**

**Gaus Width: 4.1132**



# B1L102S, U16-ch113, adc1

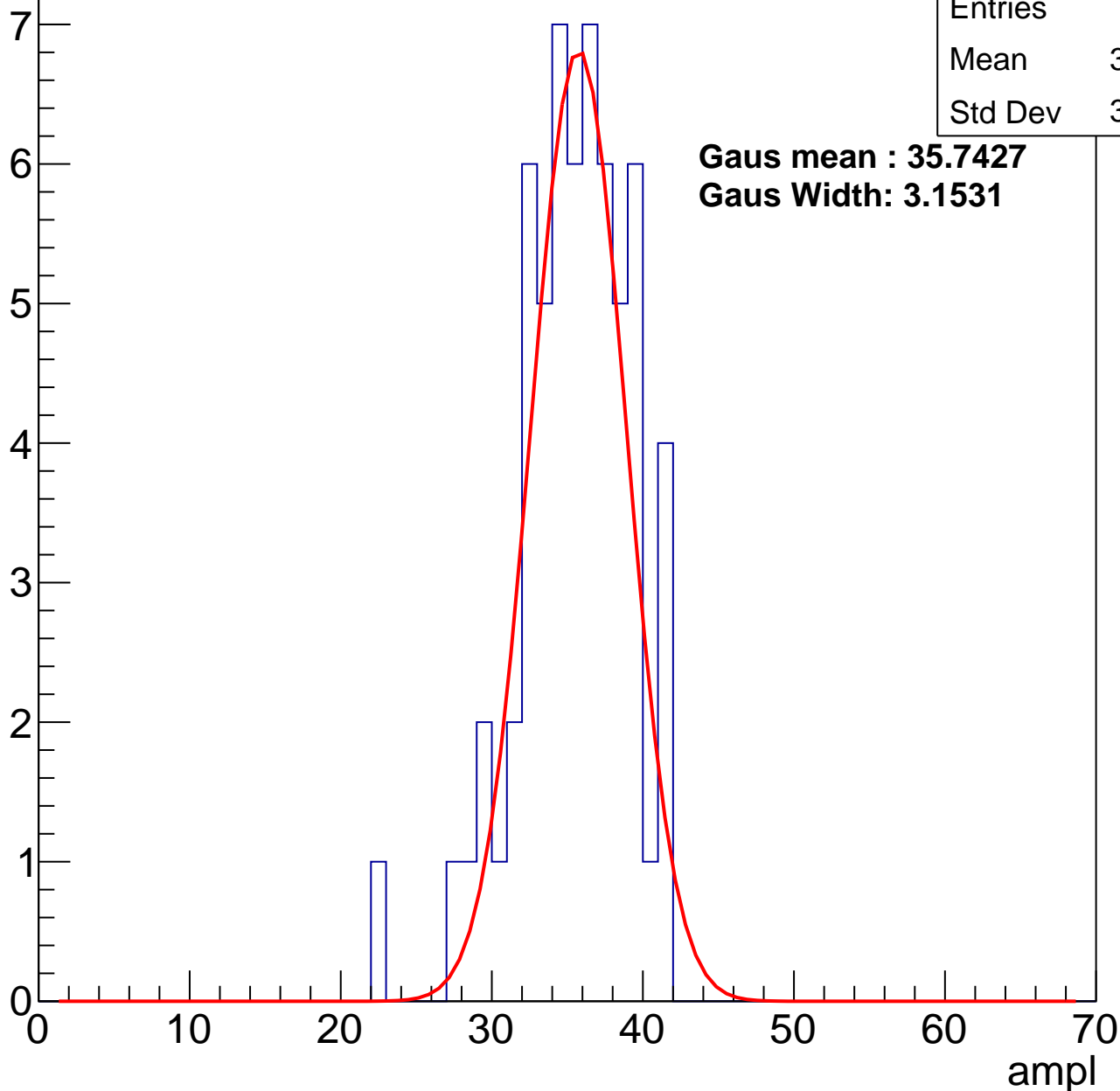
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	34.98
Std Dev	3.695

**Gaus mean : 35.7427**

**Gaus Width: 3.1531**



# B1L102S, U16-ch113, adc2

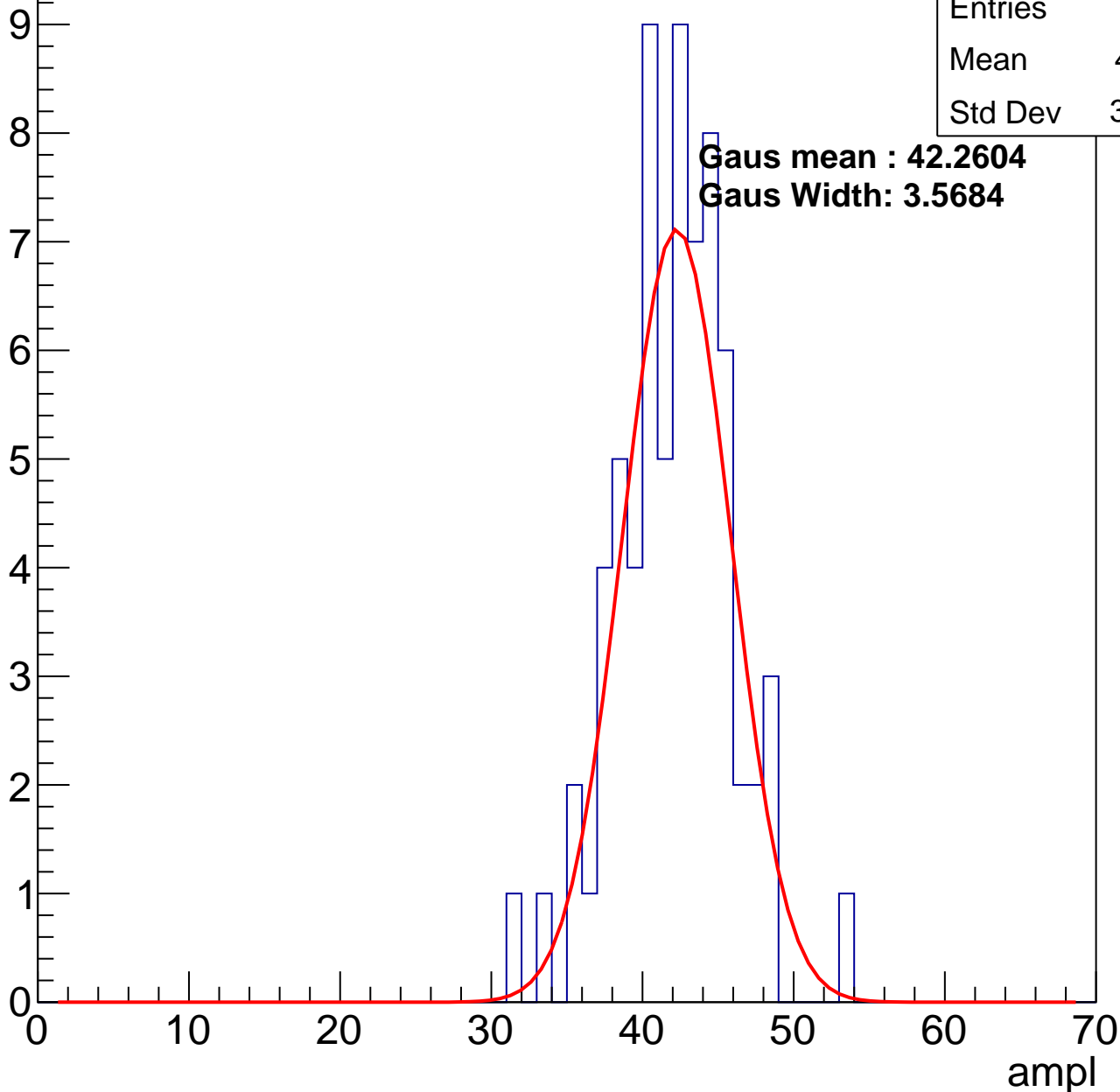
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	41.61
Std Dev	3.754

**Gaus mean : 42.2604**

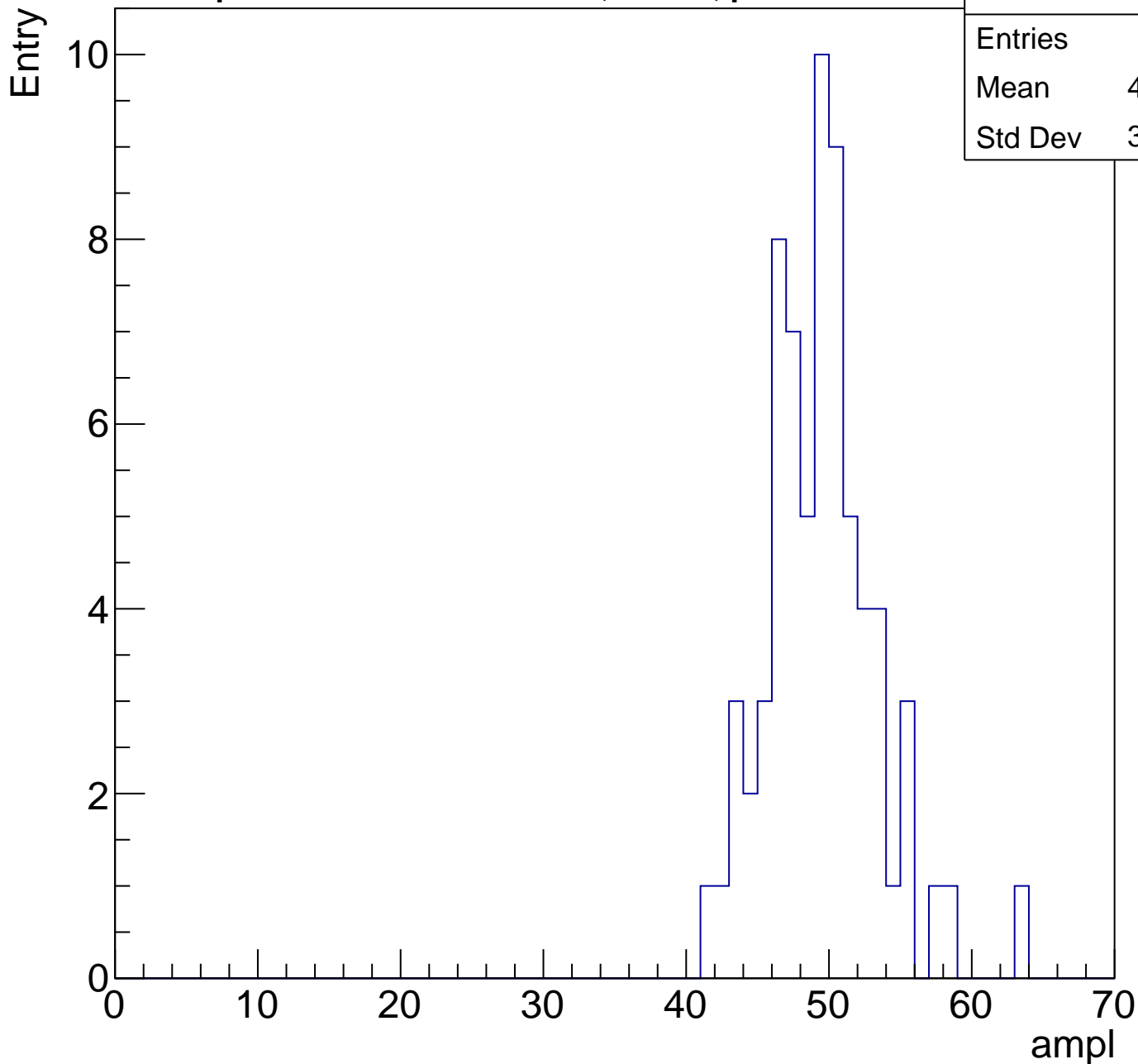
**Gaus Width: 3.5684**



# B1L102S, U16-ch113, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	69
Mean	49.04
Std Dev	3.858

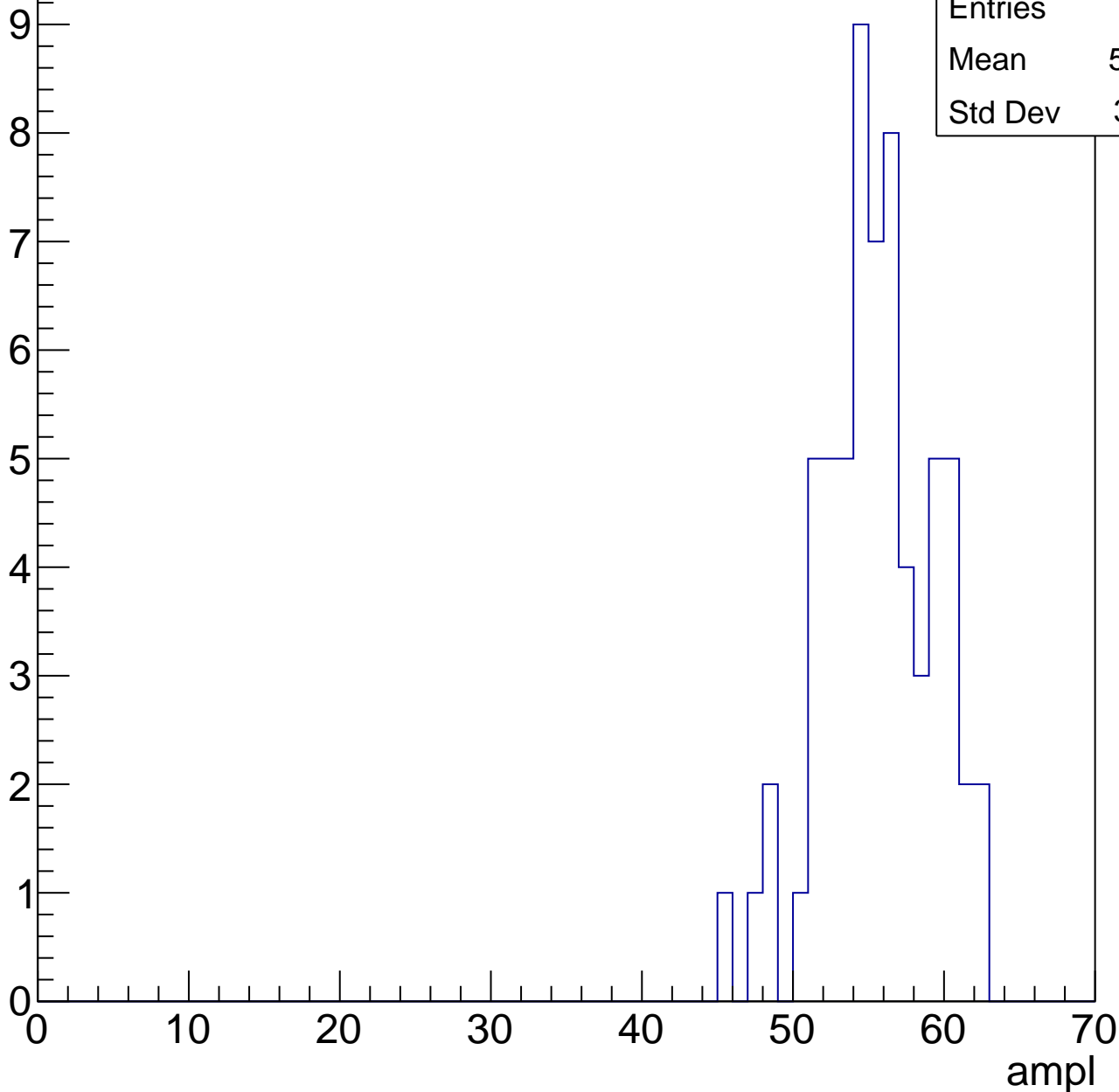


# B1L102S, U16-ch113, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	55.08
Std Dev	3.651

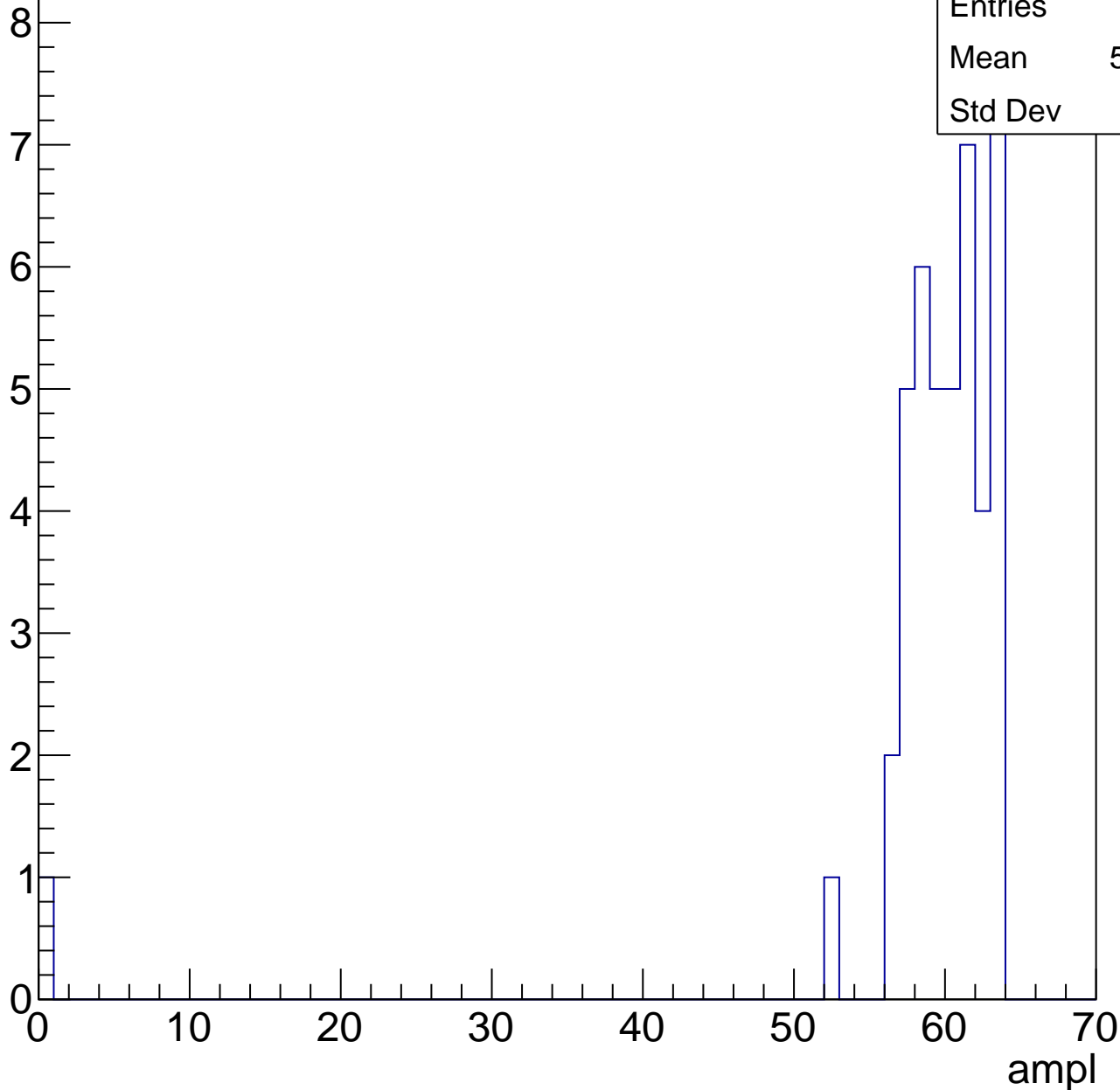


# B1L102S, U16-ch113, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

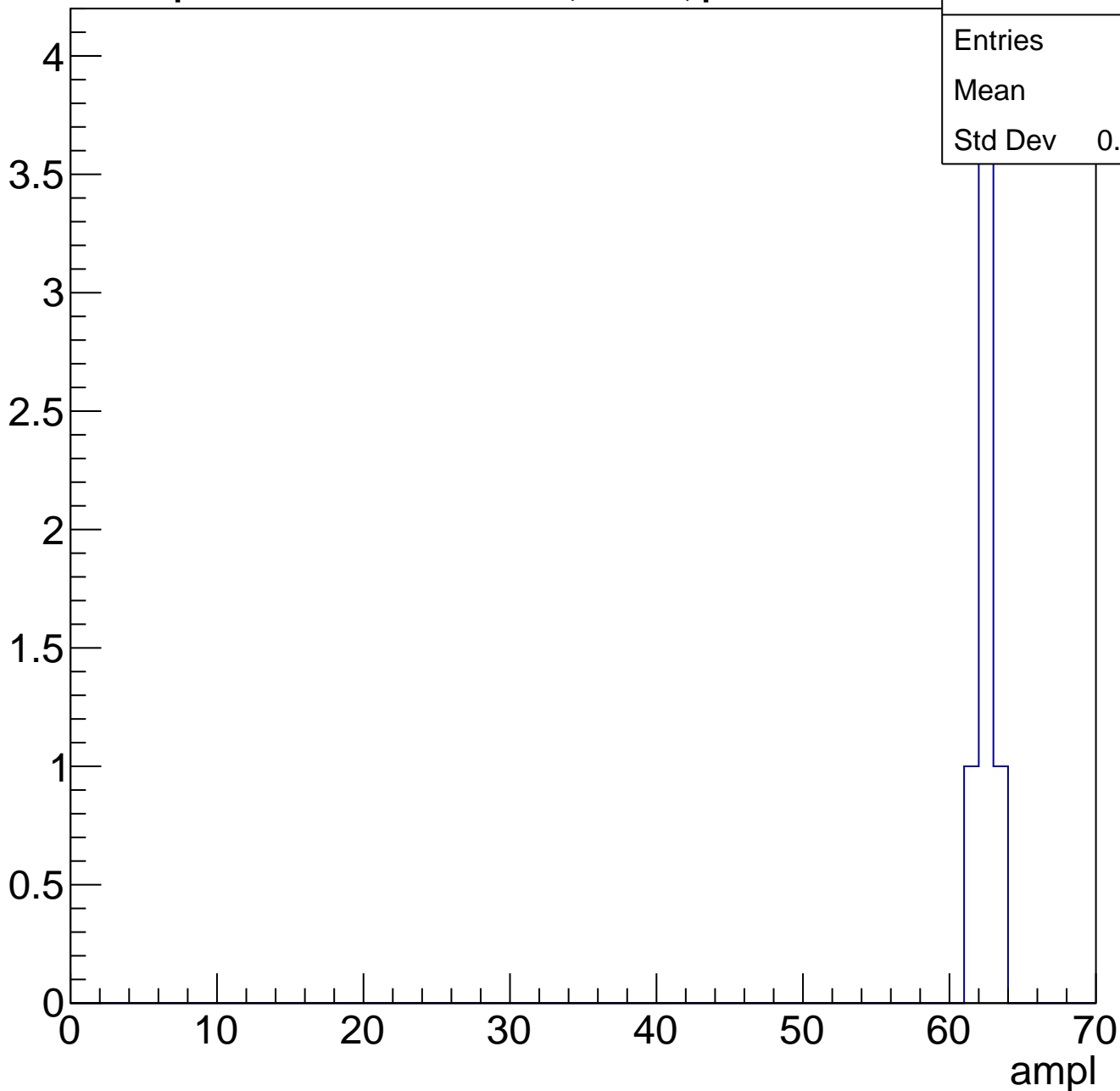
Entries	44
Mean	58.43
Std Dev	9.24



# B1L102S, U16-ch113, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch113, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U16-ch114, adc0

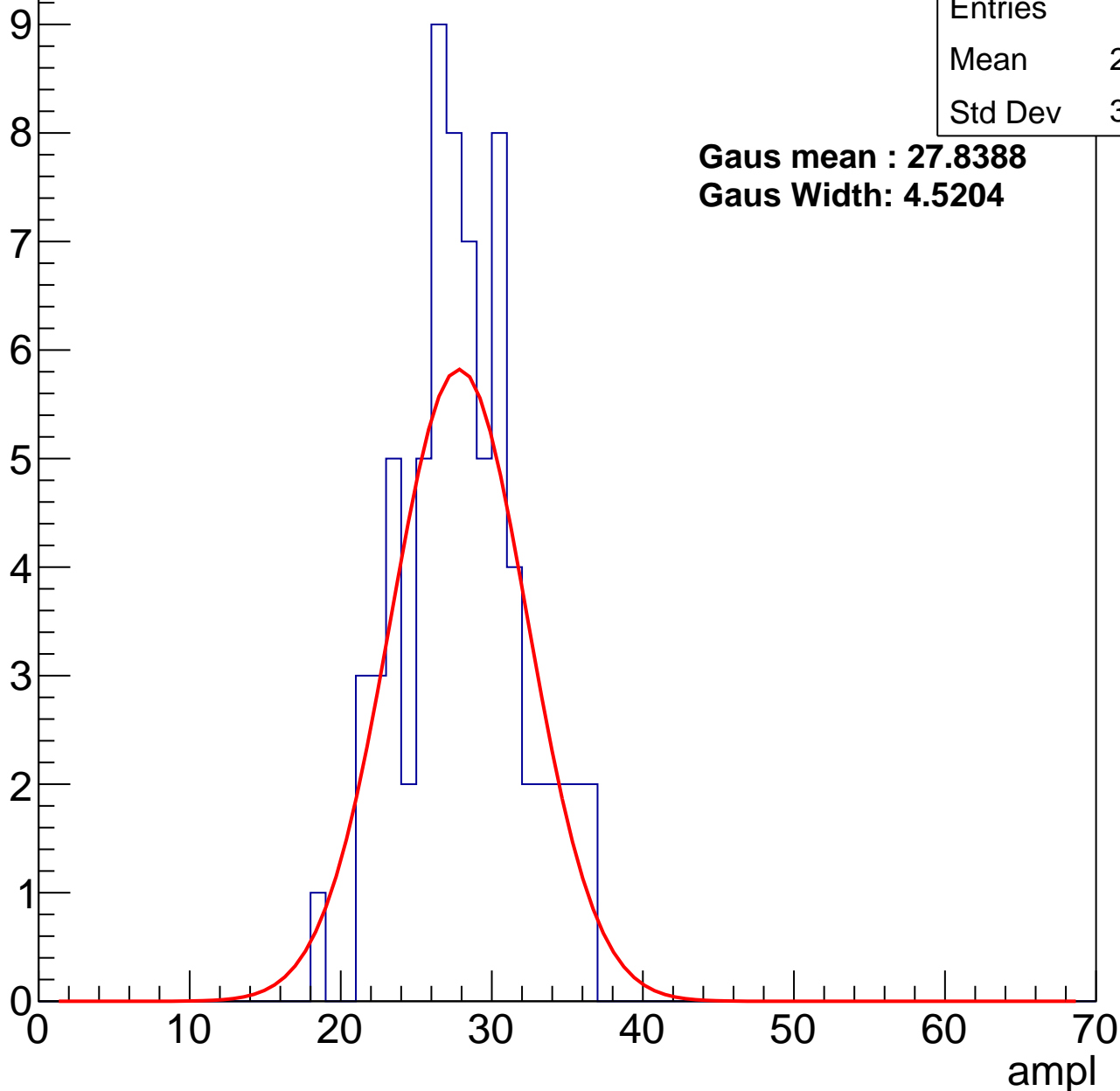
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	70
Mean	27.57
Std Dev	3.857

**Gaus mean : 27.8388**

**Gaus Width: 4.5204**



# B1L102S, U16-ch114, adc1

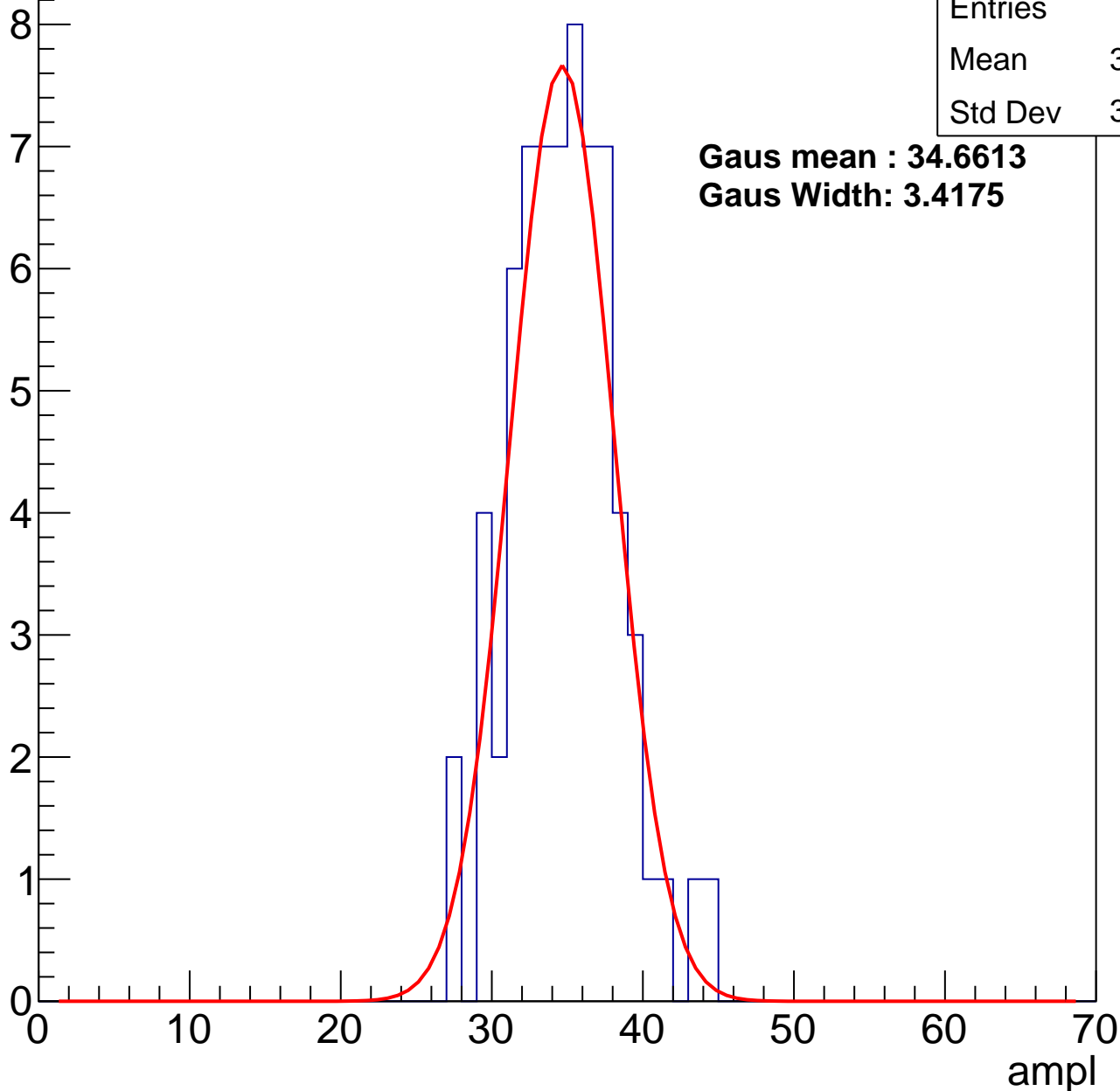
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	68
Mean	34.37
Std Dev	3.459

**Gaus mean : 34.6613**

**Gaus Width: 3.4175**



# B1L102S, U16-ch114, adc2

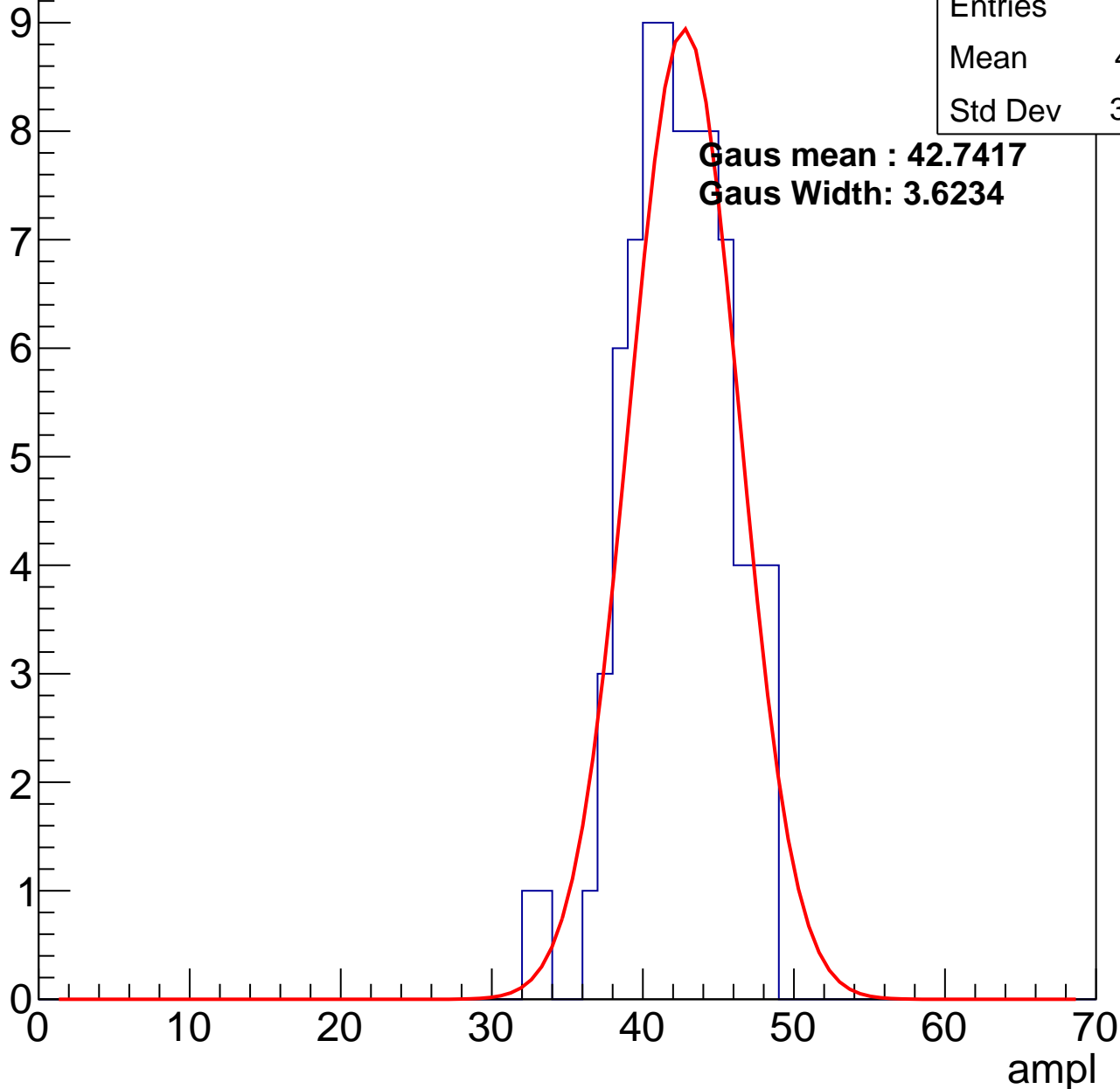
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	41.91
Std Dev	3.366

**Gaus mean : 42.7417**

**Gaus Width: 3.6234**

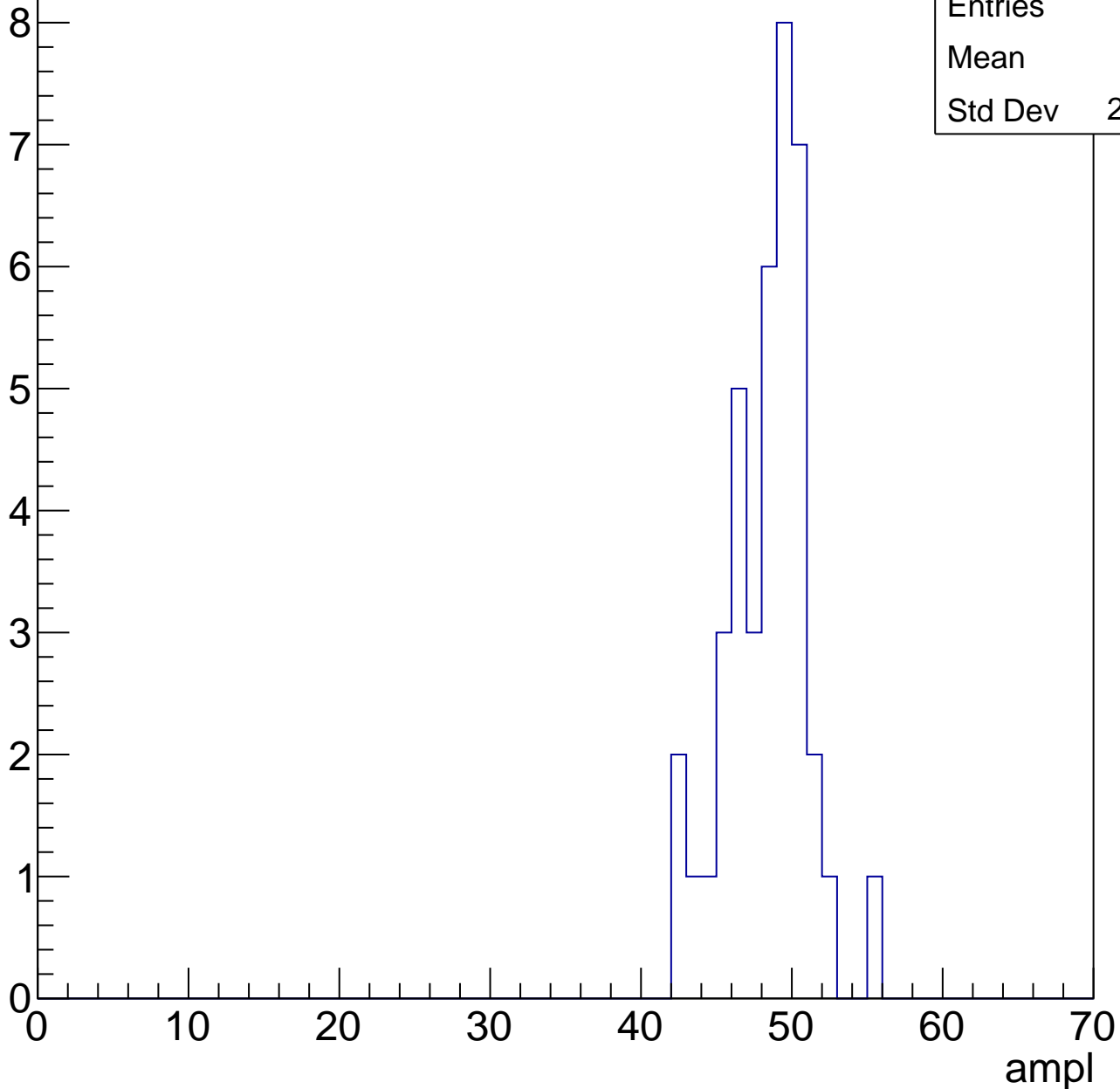


# B1L102S, U16-ch114, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	47.9
Std Dev	2.653

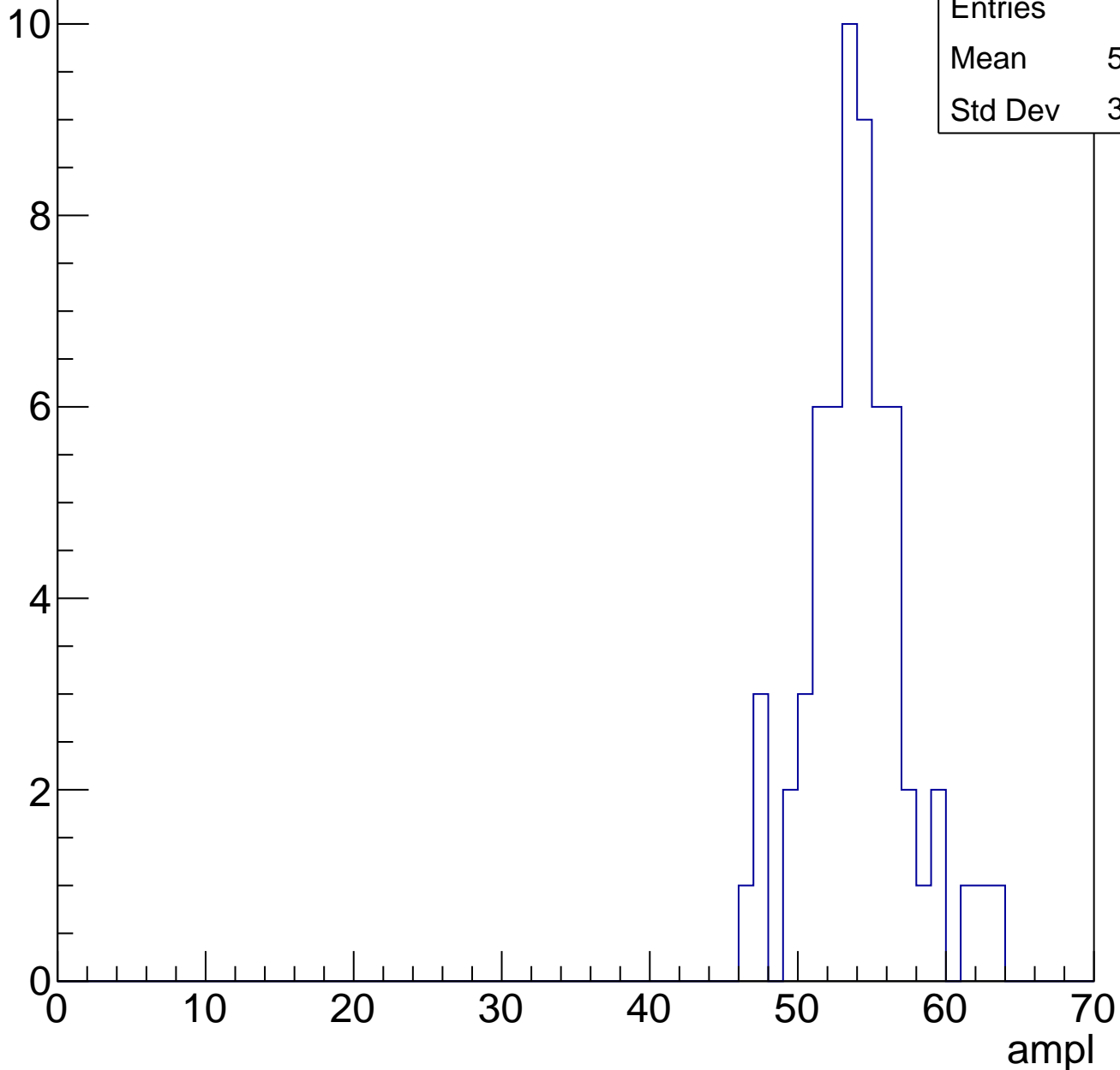


# B1L102S, U16-ch114, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	60
Mean	53.52
Std Dev	3.394

Entry

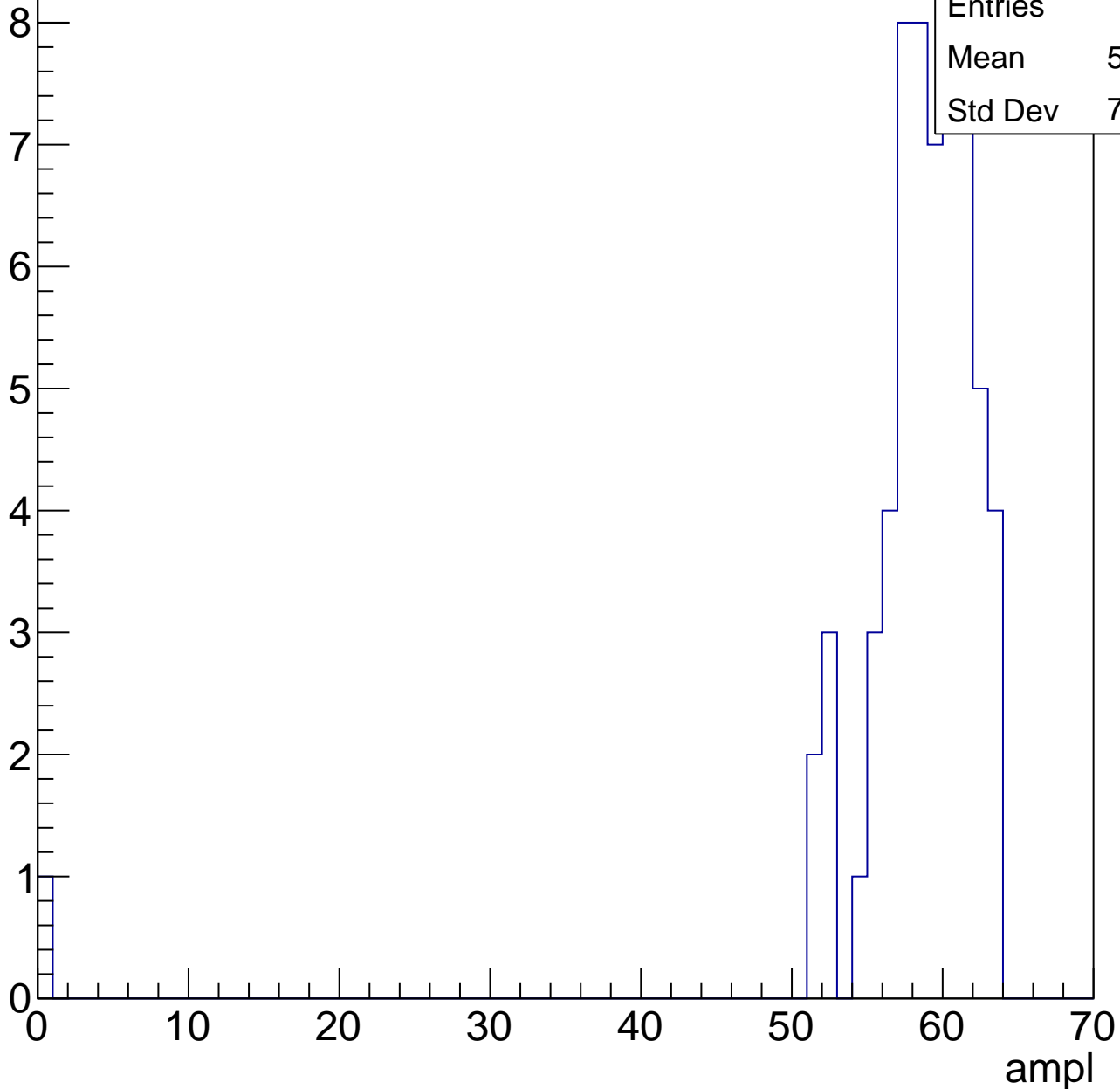


# B1L102S, U16-ch114, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	57.48
Std Dev	7.943

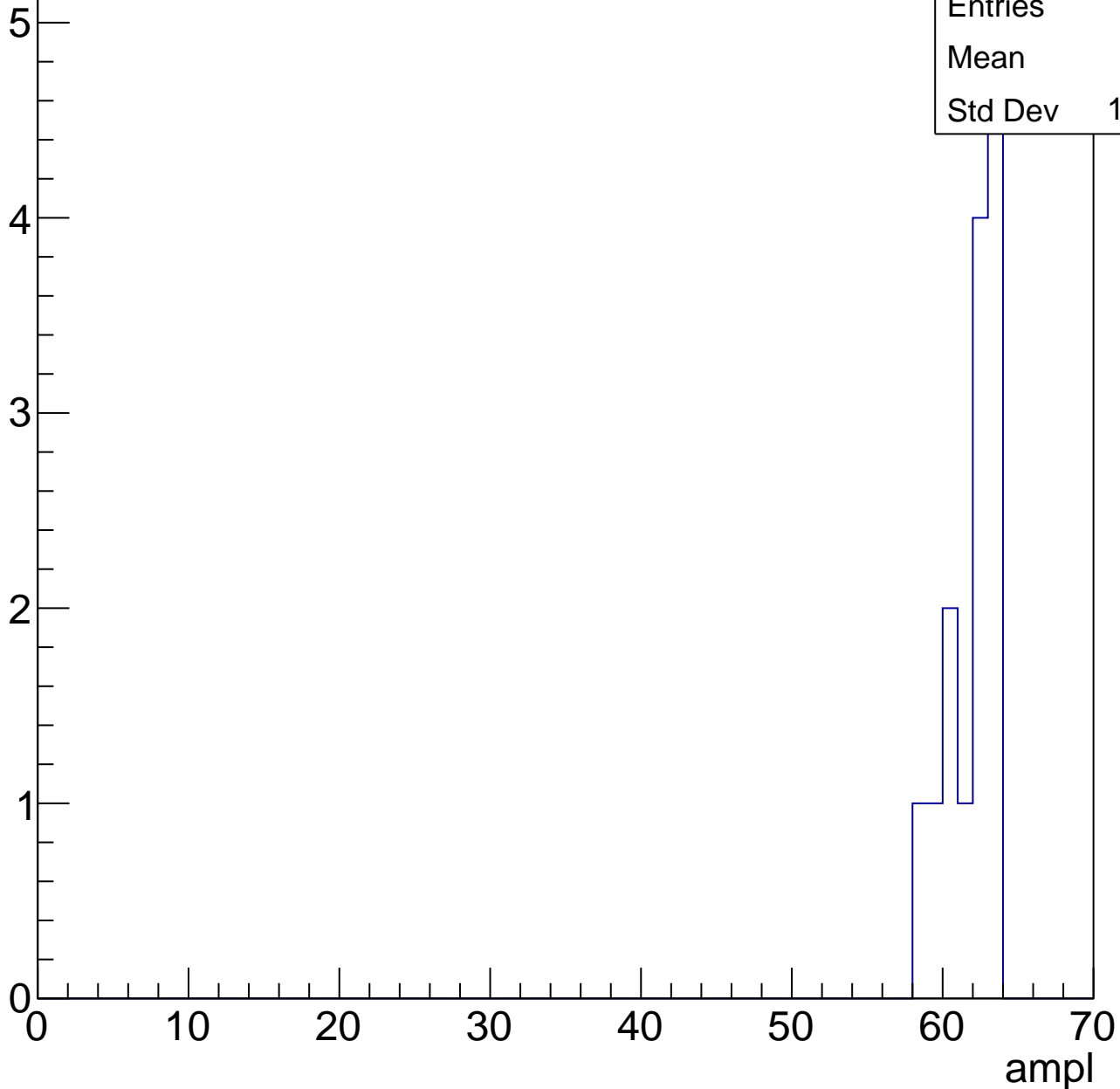


# B1L102S, U16-ch114, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	14
Mean	61.5
Std Dev	1.592





# B1L102S, U16-ch114, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0

# B1L102S, U16-ch115, adc0

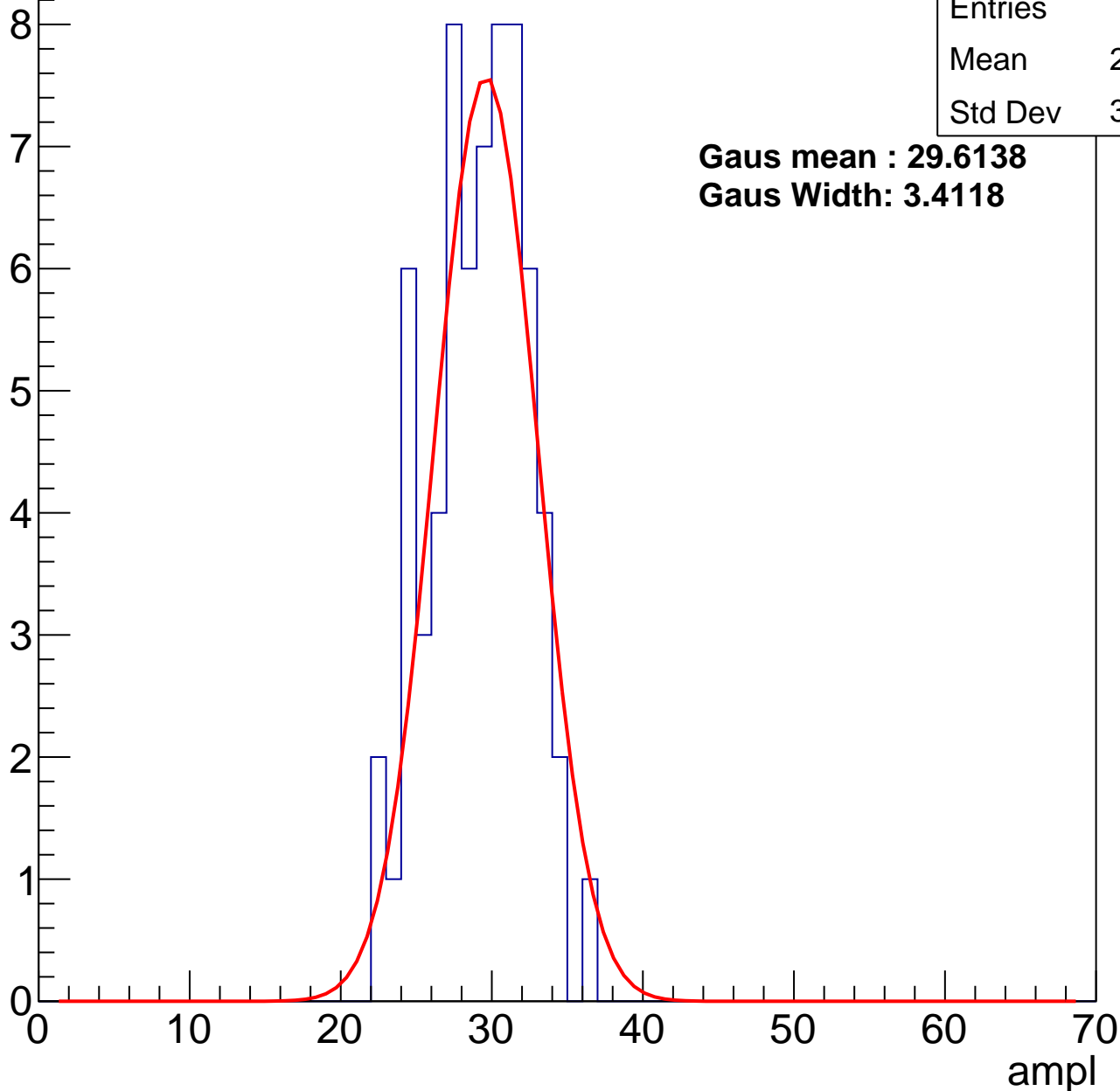
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	28.68
Std Dev	3.153

**Gaus mean : 29.6138**

**Gaus Width: 3.4118**



# B1L102S, U16-ch115, adc1

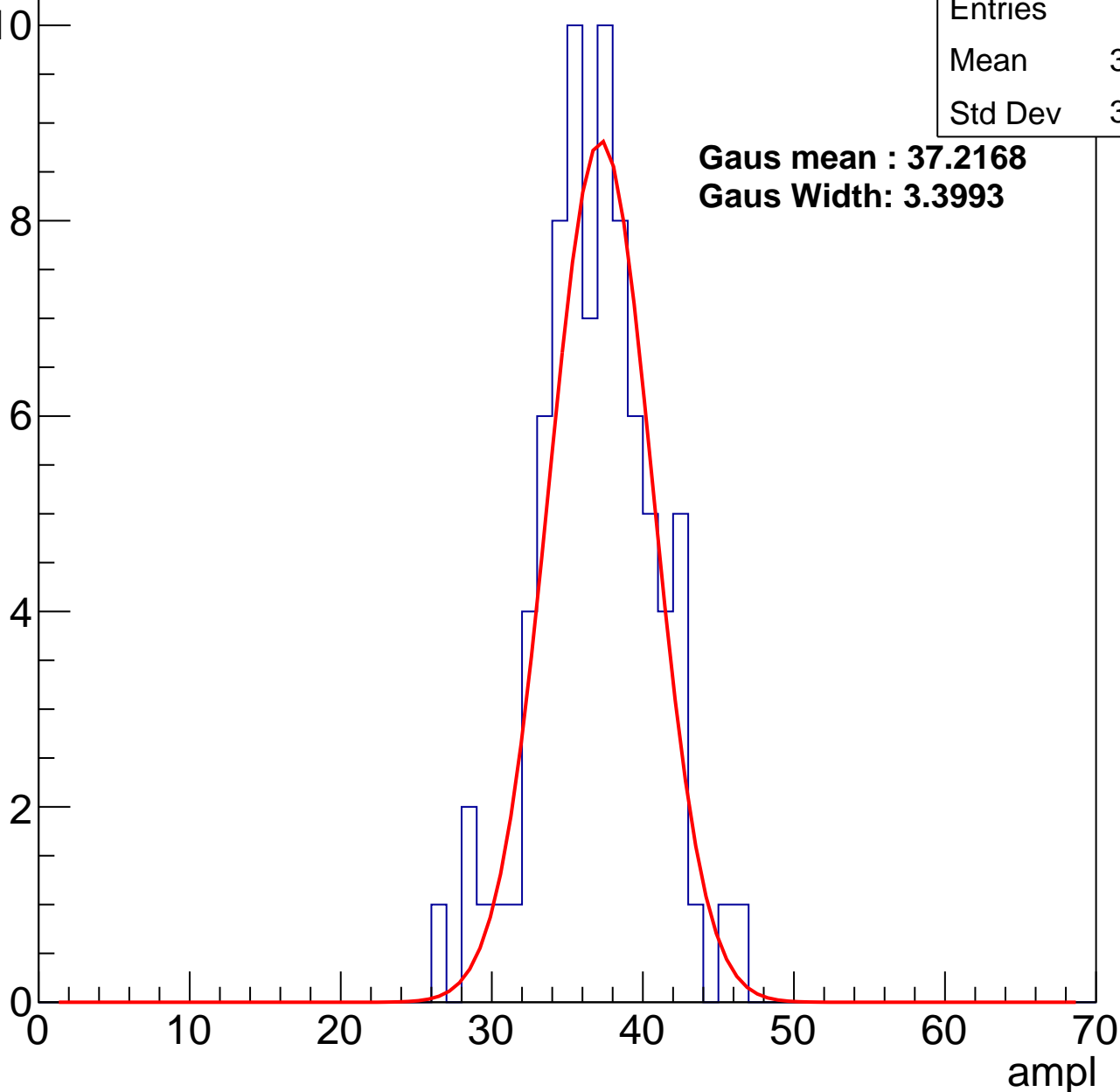
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	82
Mean	36.44
Std Dev	3.774

**Gaus mean : 37.2168**

**Gaus Width: 3.3993**



# B1L102S, U16-ch115, adc2

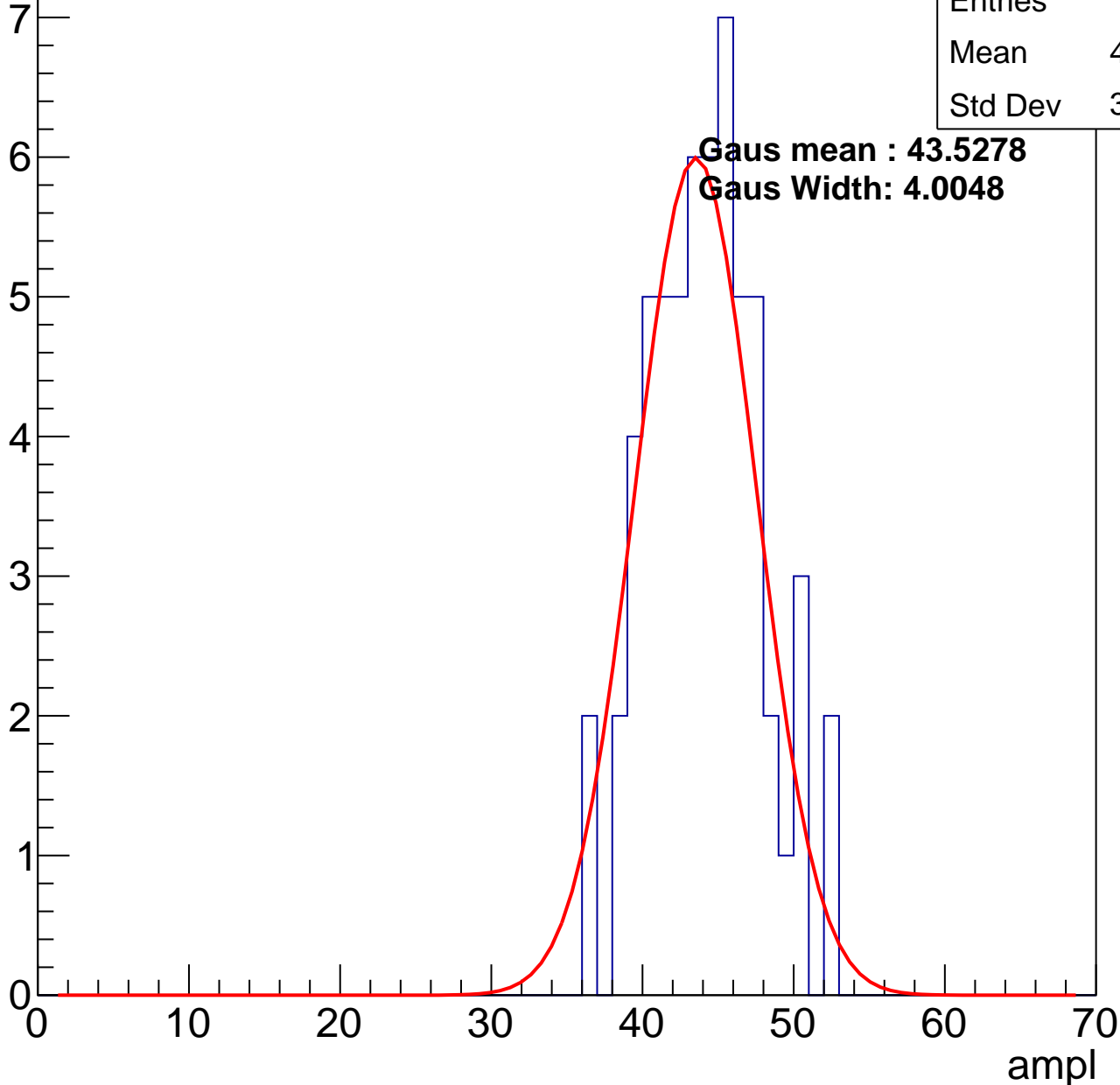
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	60
Mean	43.67
Std Dev	3.673

**Gaus mean : 43.5278**

**Gaus Width: 4.0048**

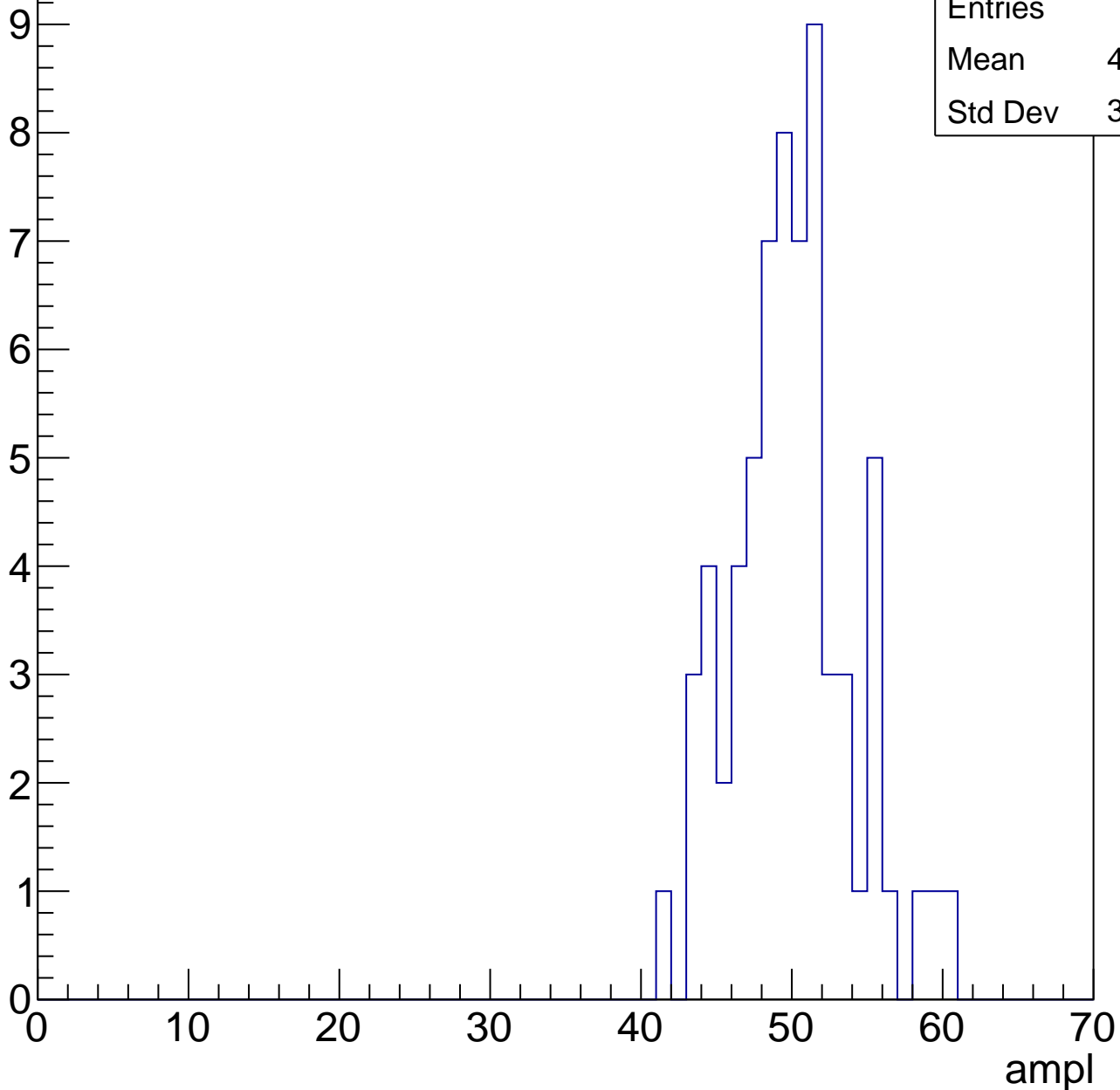


# B1L102S, U16-ch115, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	49.53
Std Dev	3.936

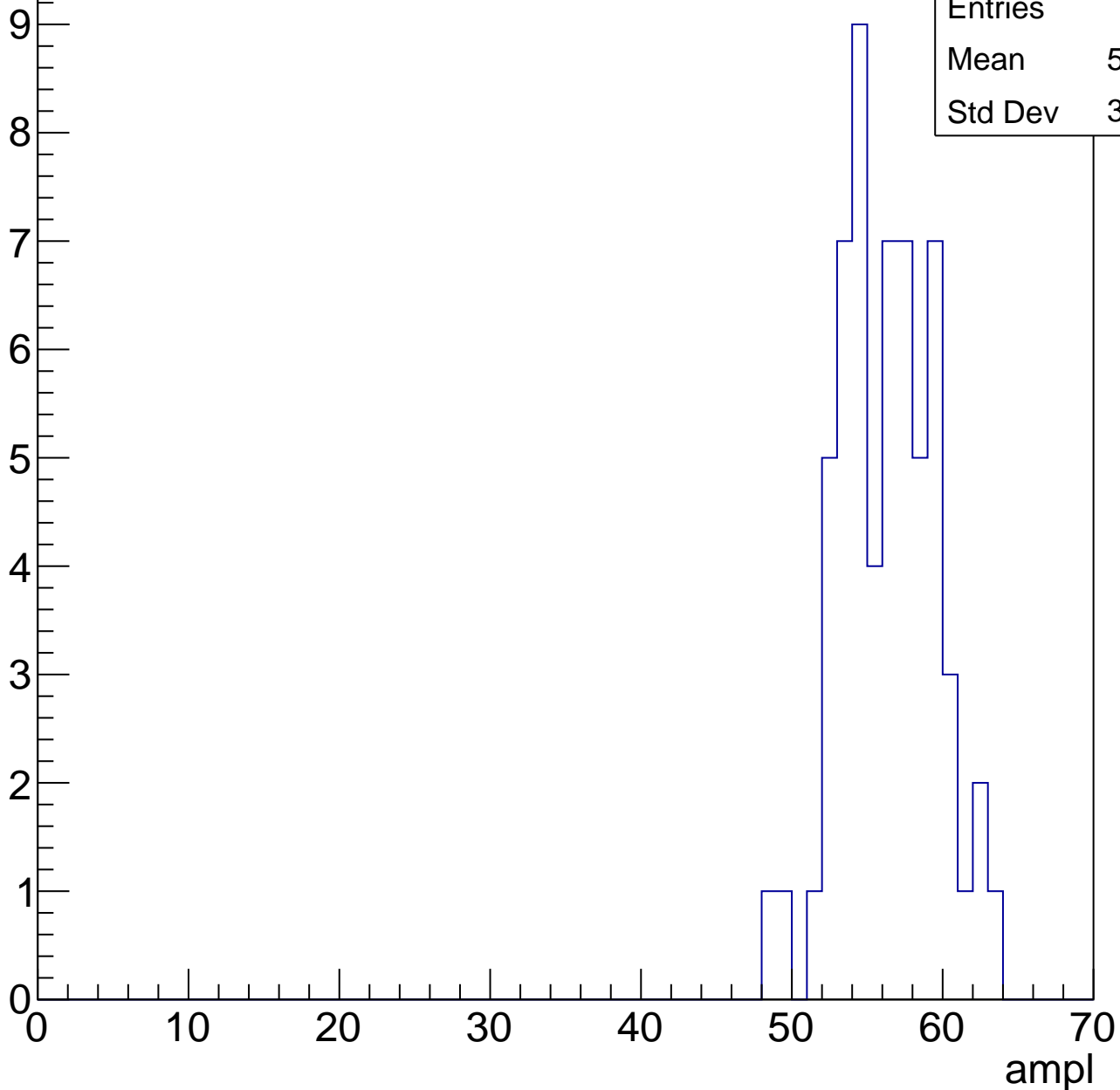


# B1L102S, U16-ch115, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	55.85
Std Dev	3.146

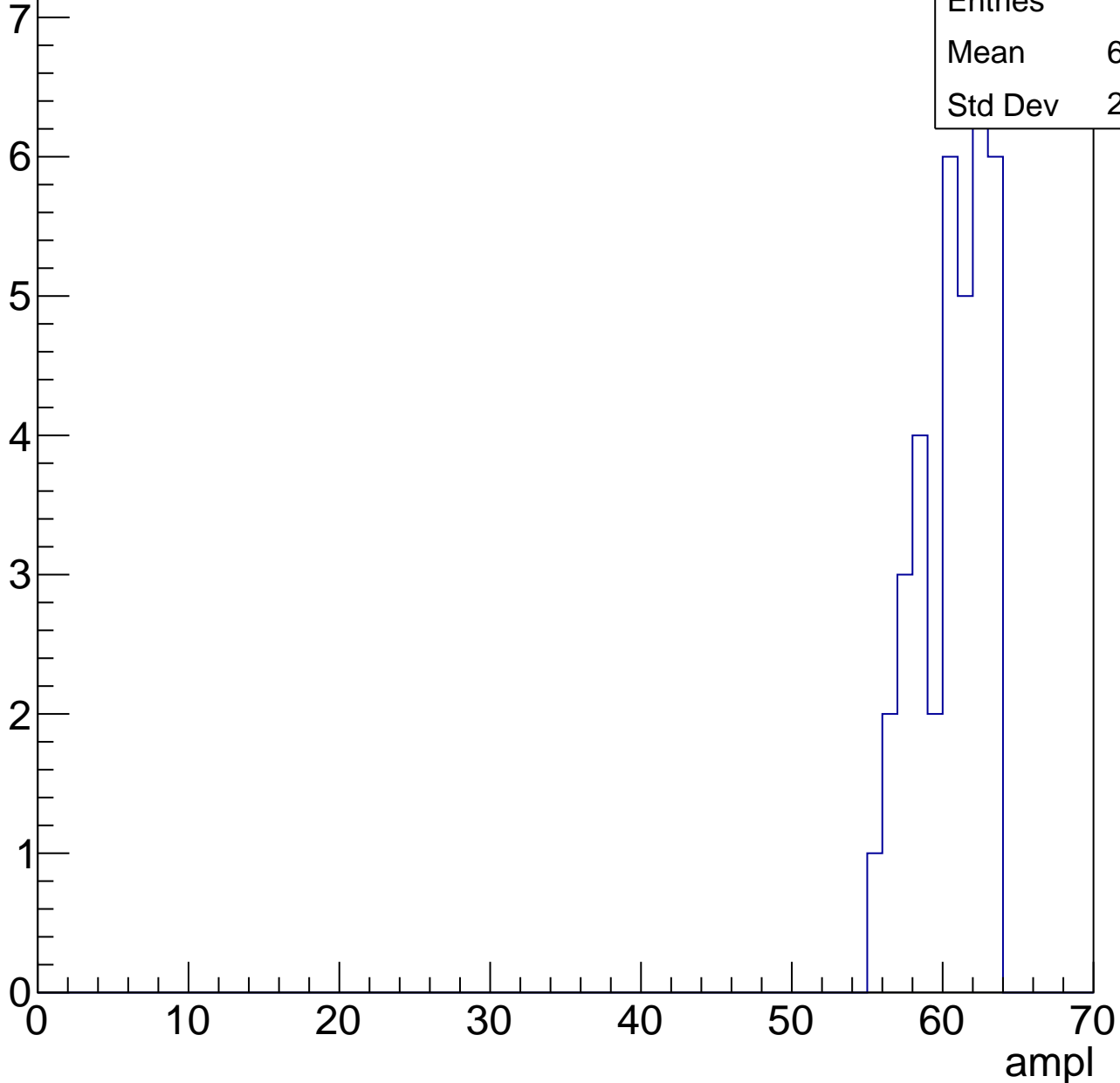


# B1L102S, U16-ch115, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

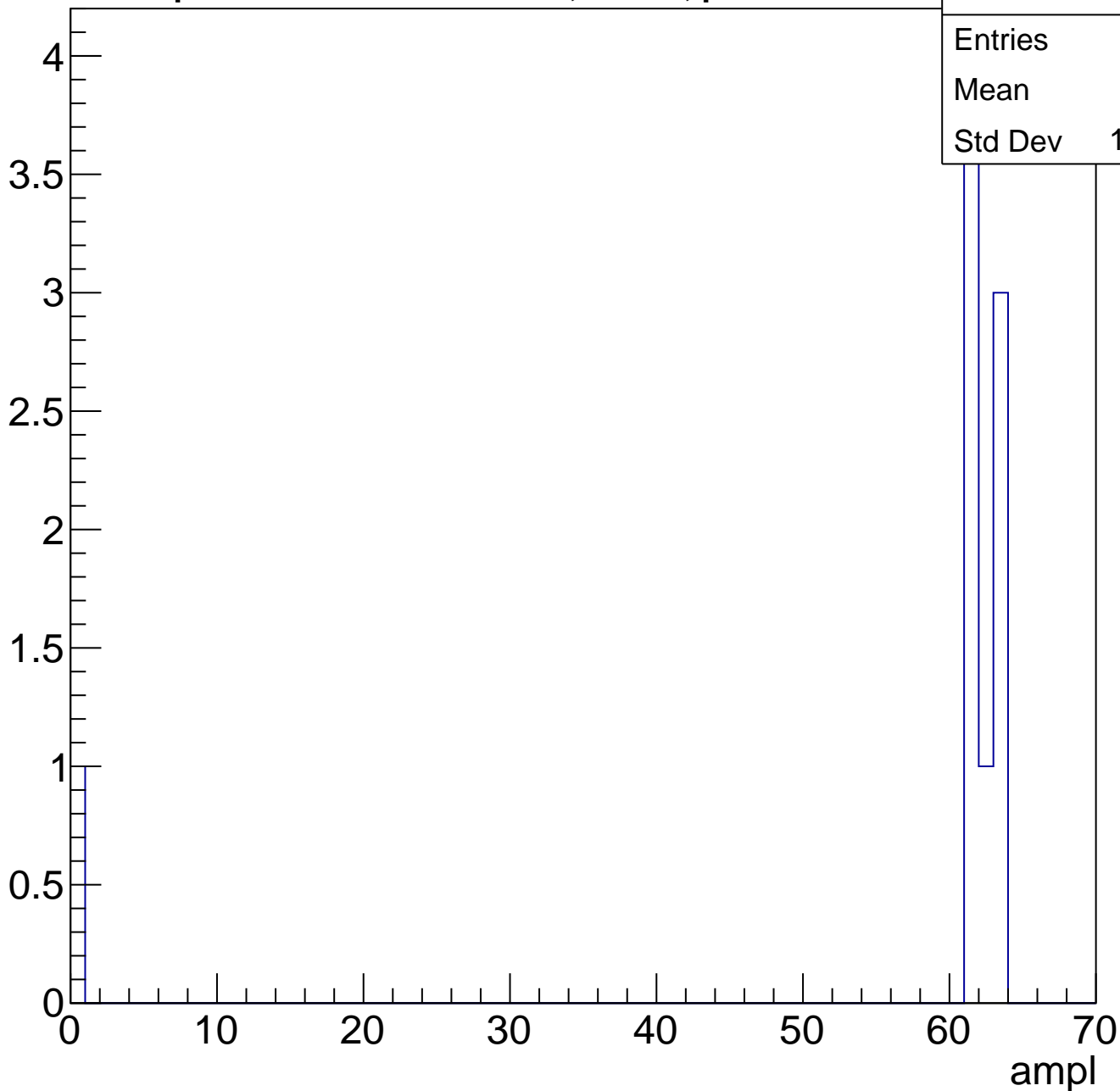
Entries	36
Mean	60.14
Std Dev	2.287



# B1L102S, U16-ch115, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch115, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U16-ch116, adc0

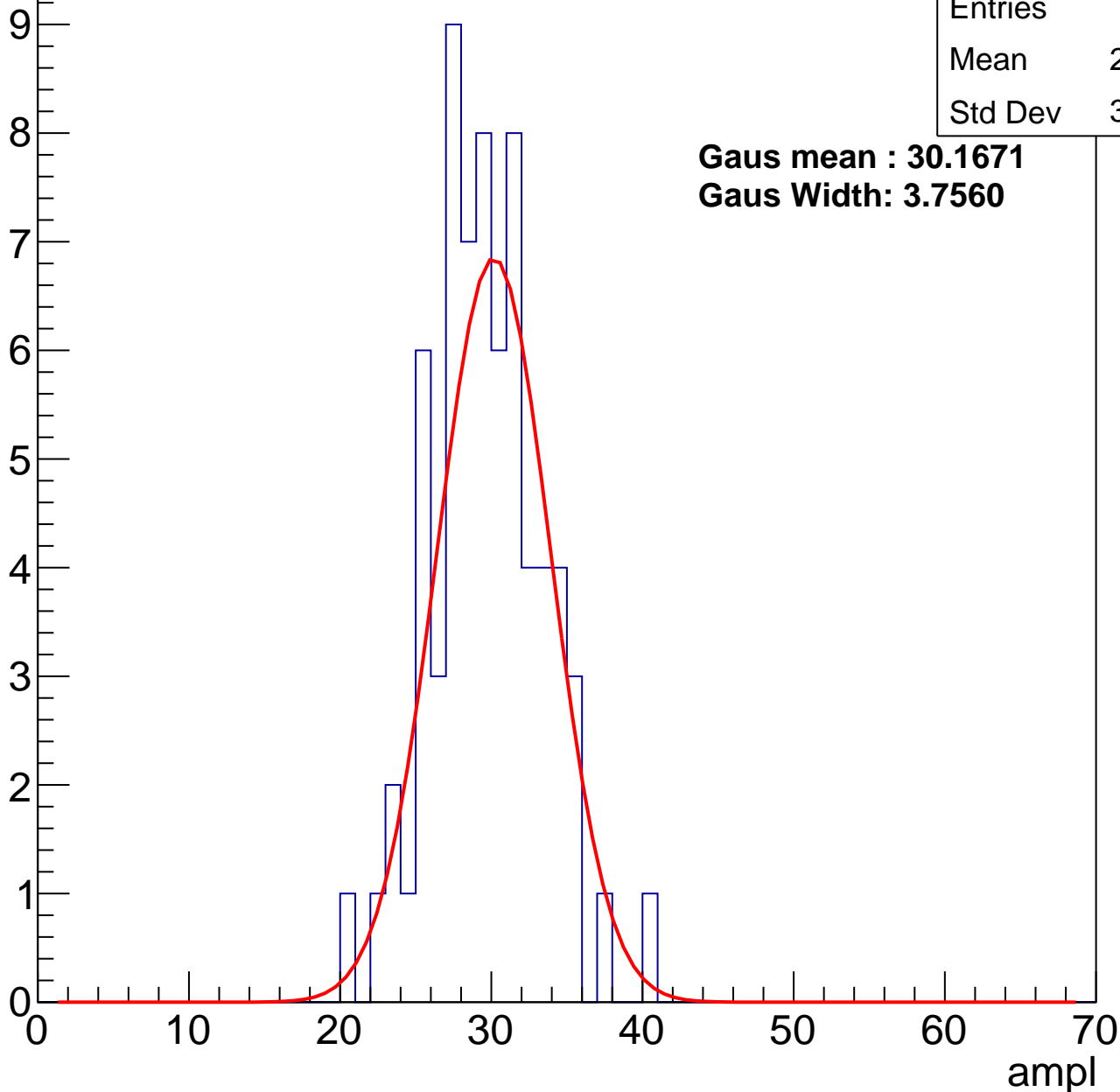
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	29.23
Std Dev	3.652

**Gaus mean : 30.1671**

**Gaus Width: 3.7560**



# B1L102S, U16-ch116, adc1

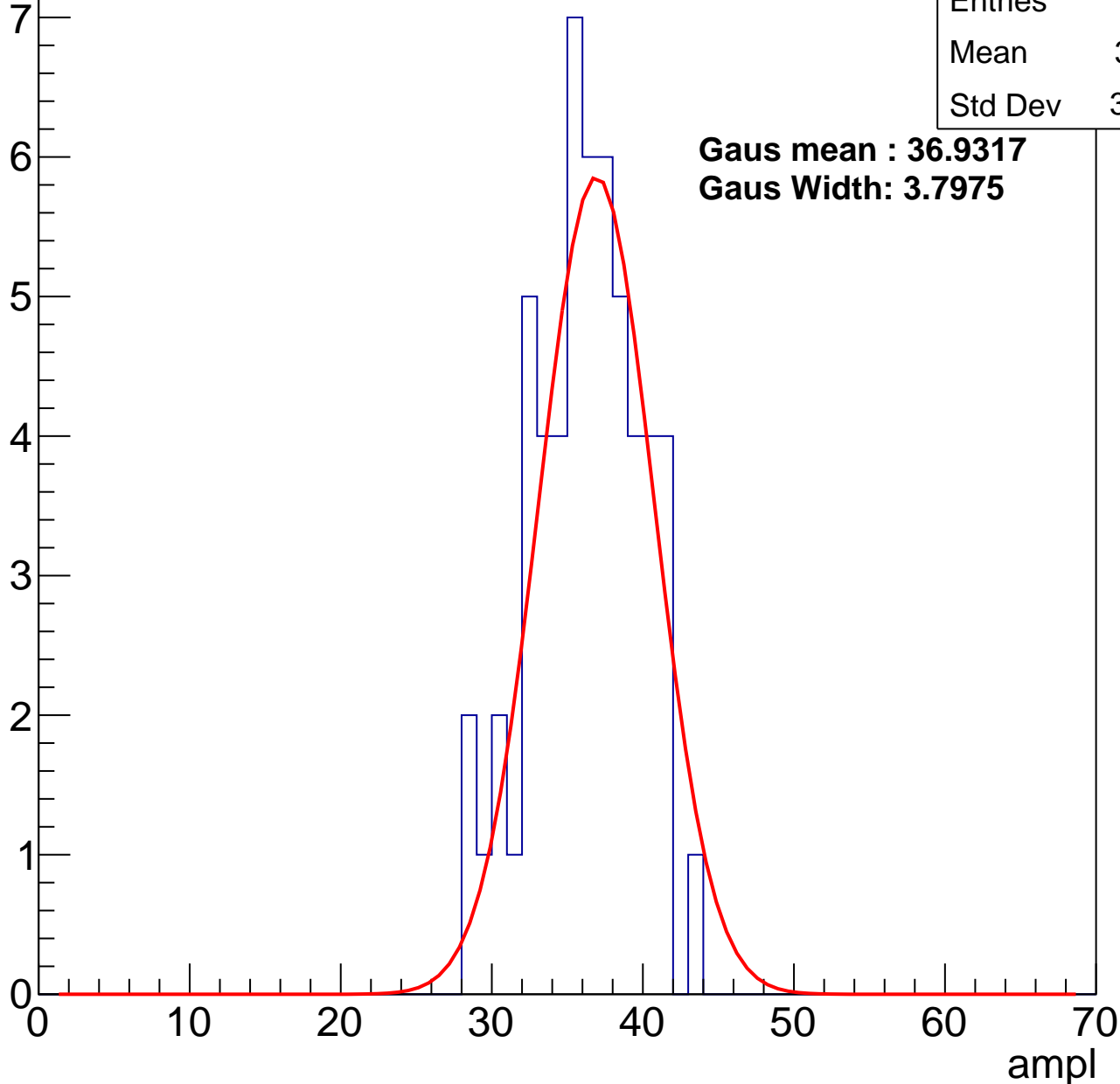
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	35.71
Std Dev	3.493

**Gaus mean : 36.9317**

**Gaus Width: 3.7975**



# B1L102S, U16-ch116, adc2

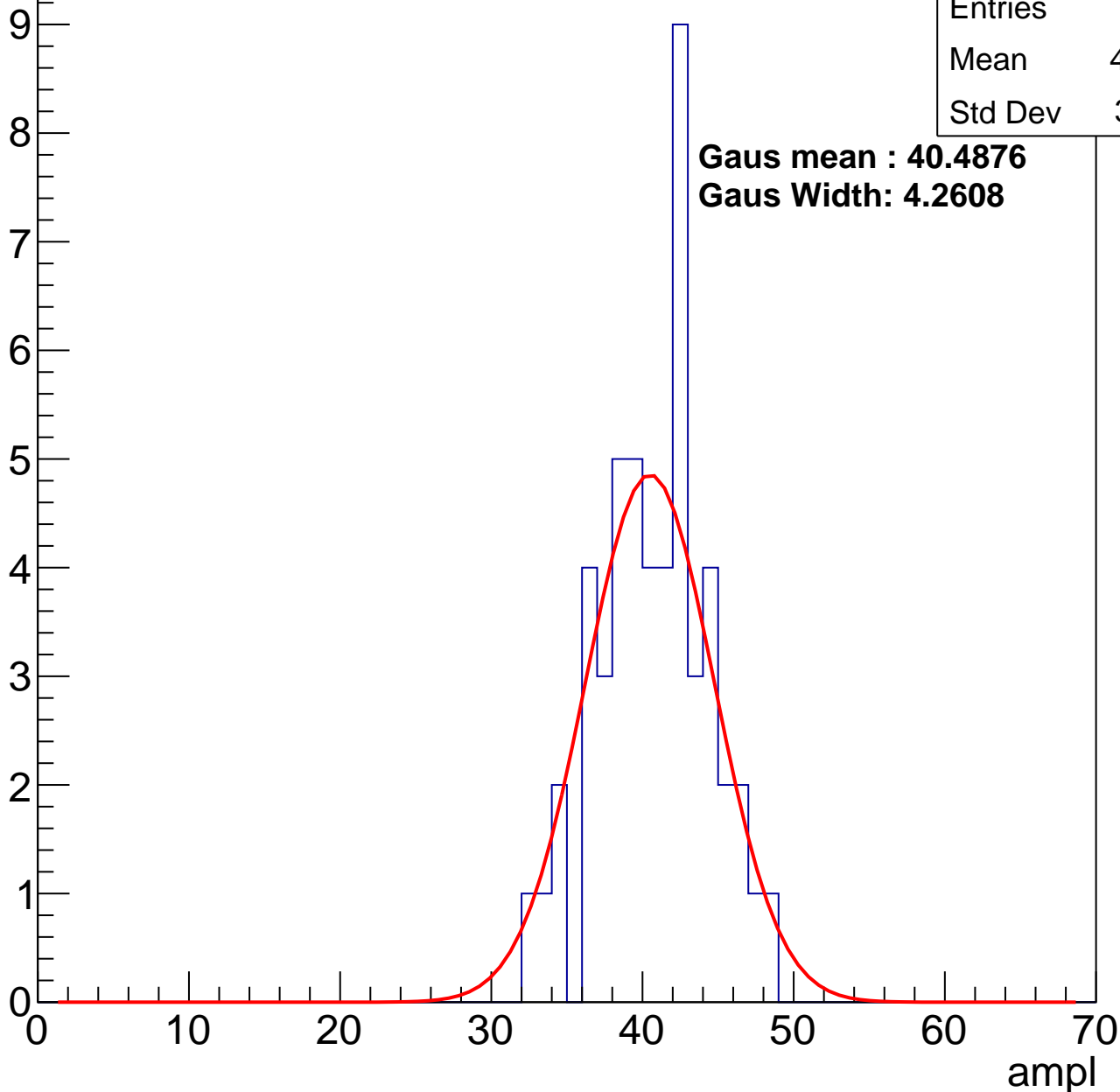
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	51
Mean	40.33
Std Dev	3.601

**Gaus mean : 40.4876**

**Gaus Width: 4.2608**

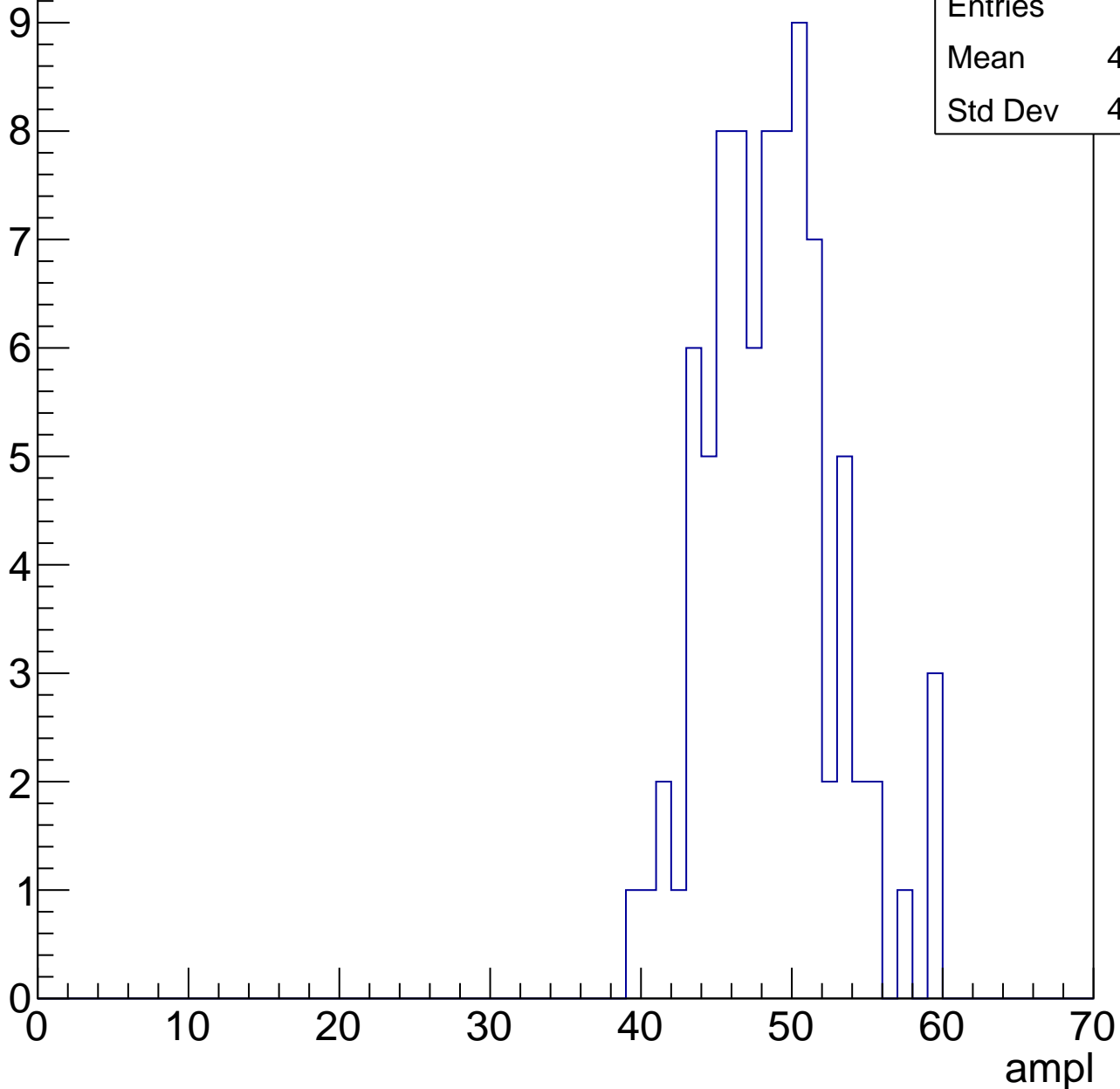


# B1L102S, U16-ch116, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	85
Mean	48.18
Std Dev	4.193

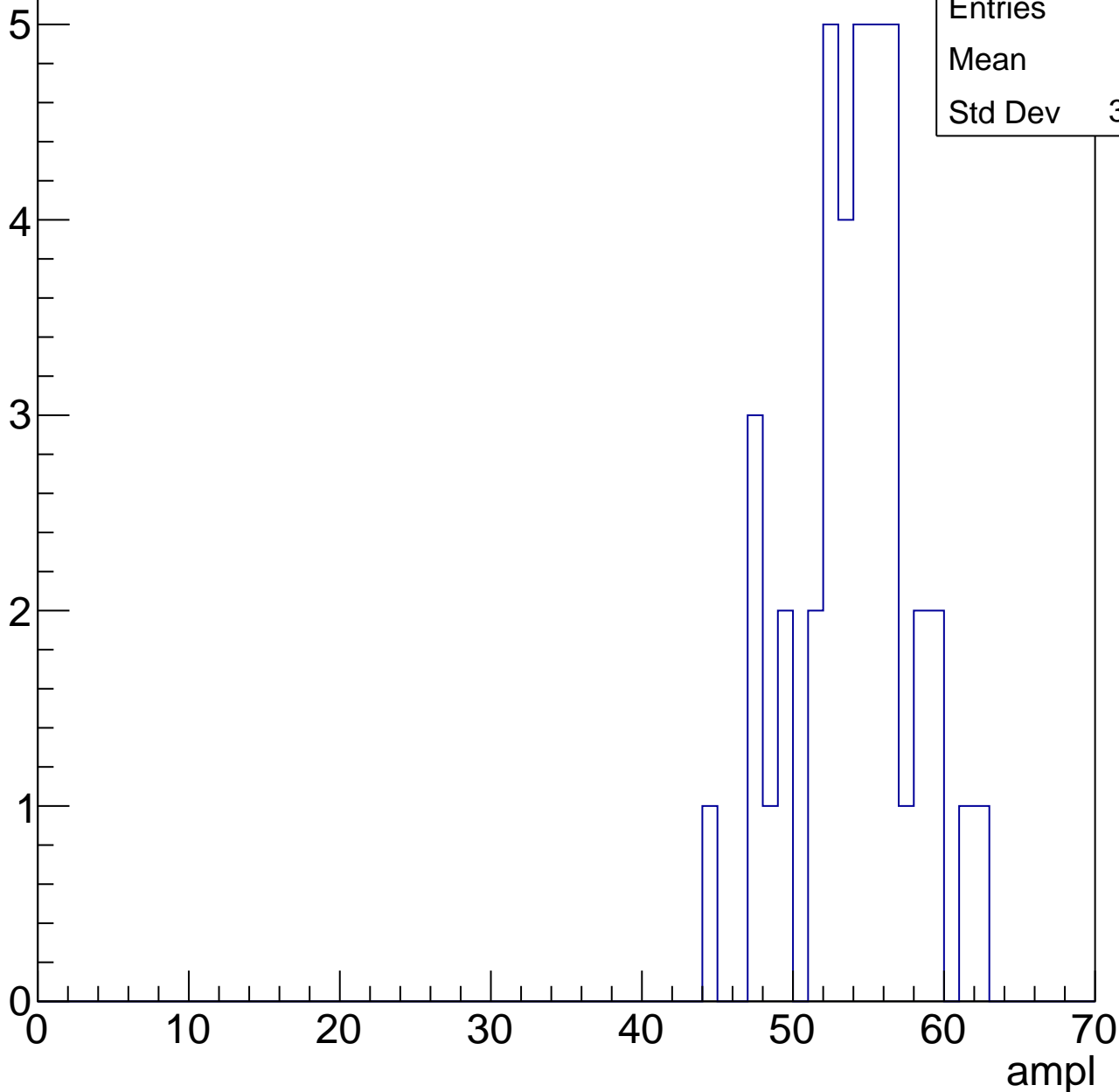


# B1L102S, U16-ch116, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	53.6
Std Dev	3.865



# B1L102S, U16-ch116, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

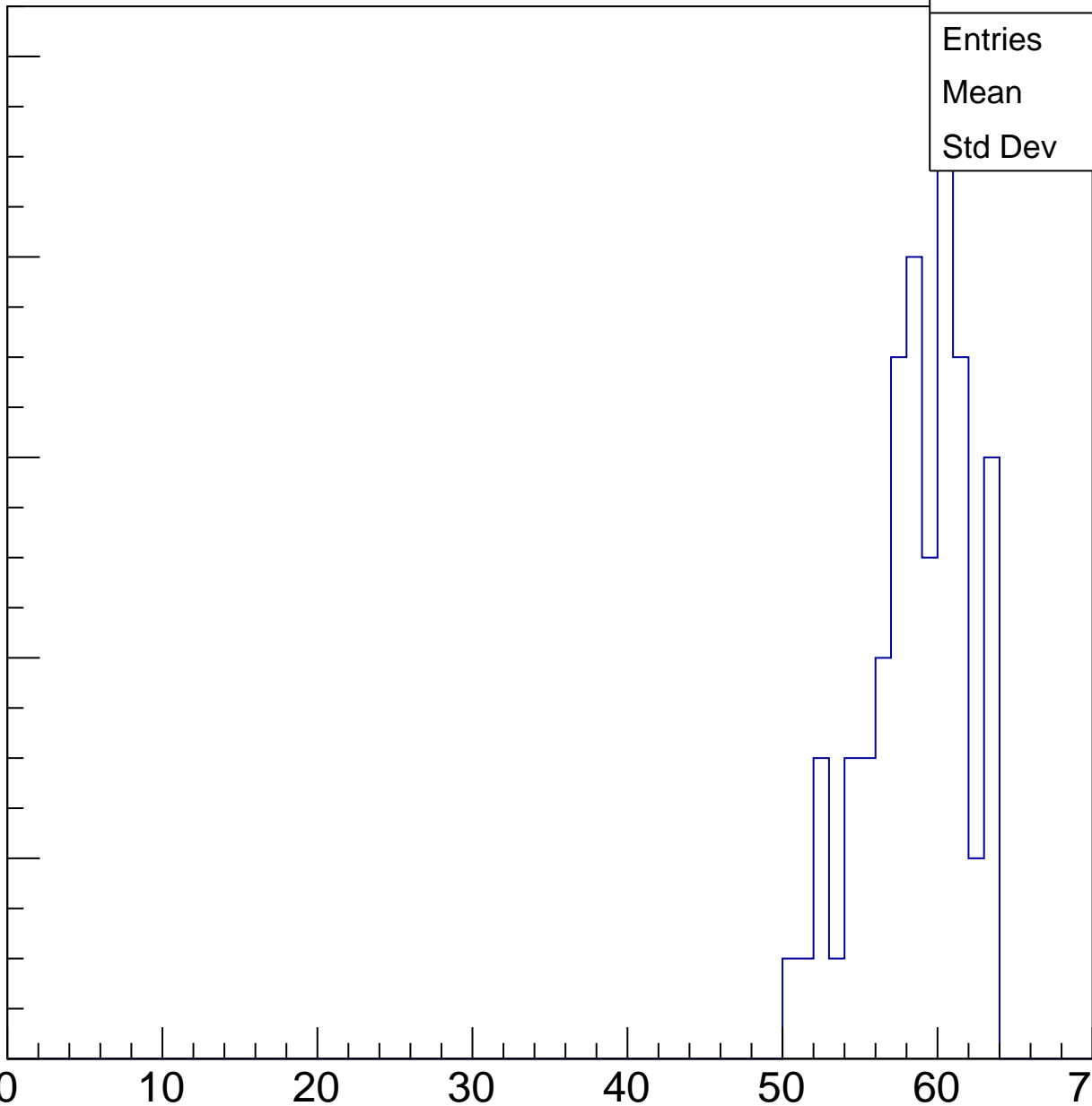
Entries	61
Mean	58.16
Std Dev	3.22

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl

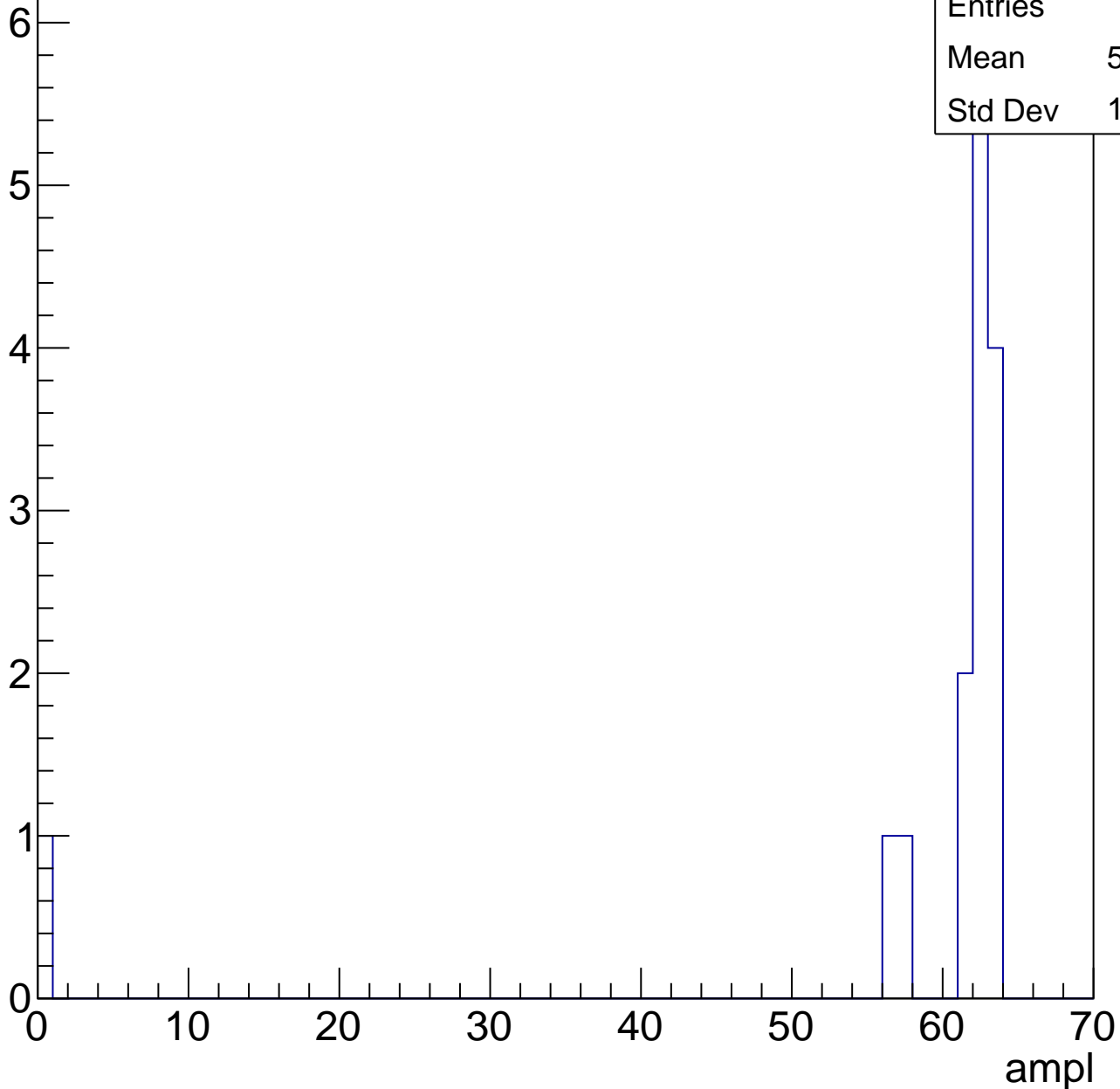


# B1L102S, U16-ch116, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	15
Mean	57.27
Std Dev	15.44





# B1L102S, U16-ch116, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch117, adc0

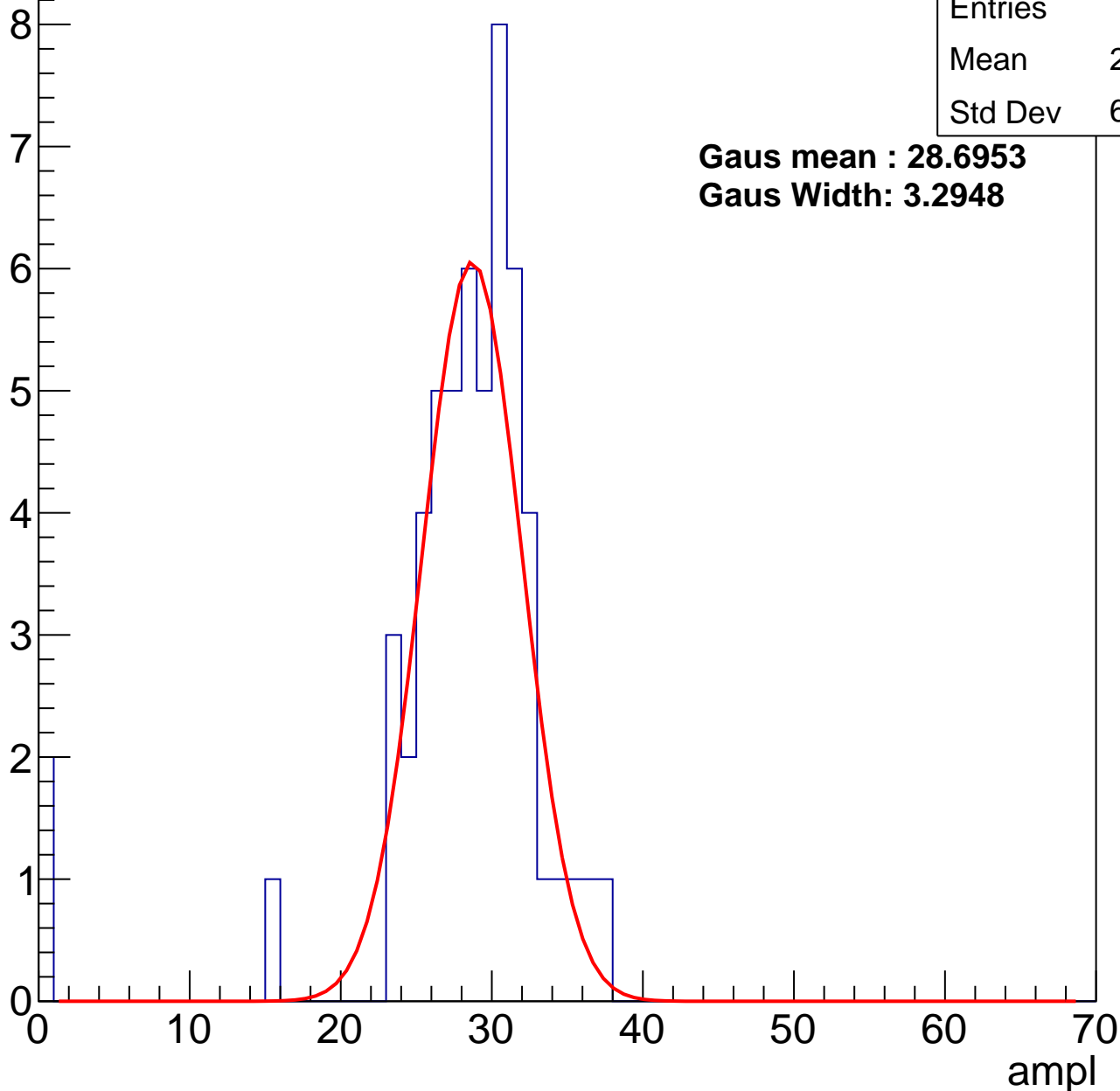
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	27.48
Std Dev	6.409

**Gaus mean : 28.6953**

**Gaus Width: 3.2948**



# B1L102S, U16-ch117, adc1

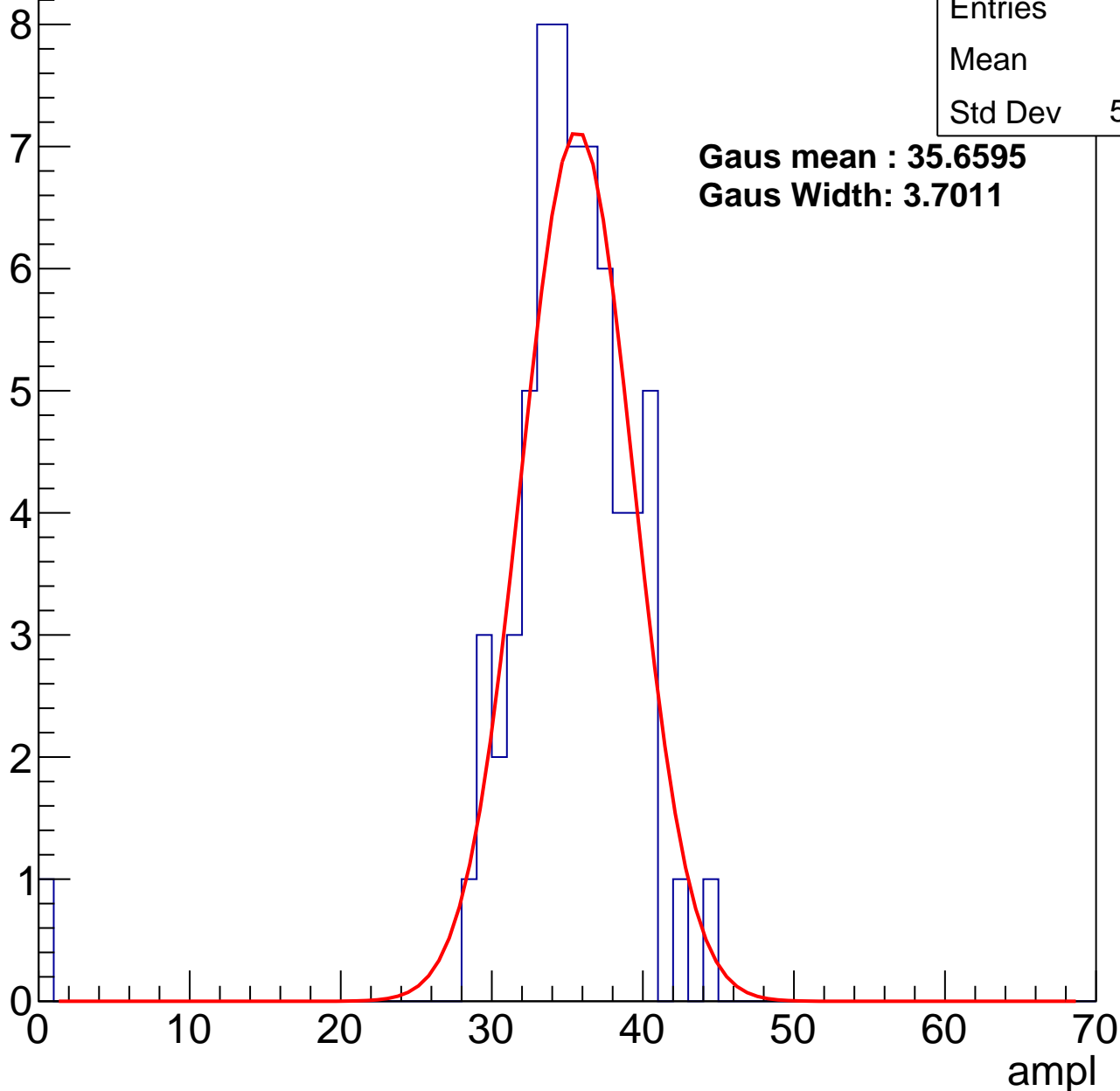
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	34.5
Std Dev	5.414

**Gaus mean : 35.6595**

**Gaus Width: 3.7011**



# B1L102S, U16-ch117, adc2

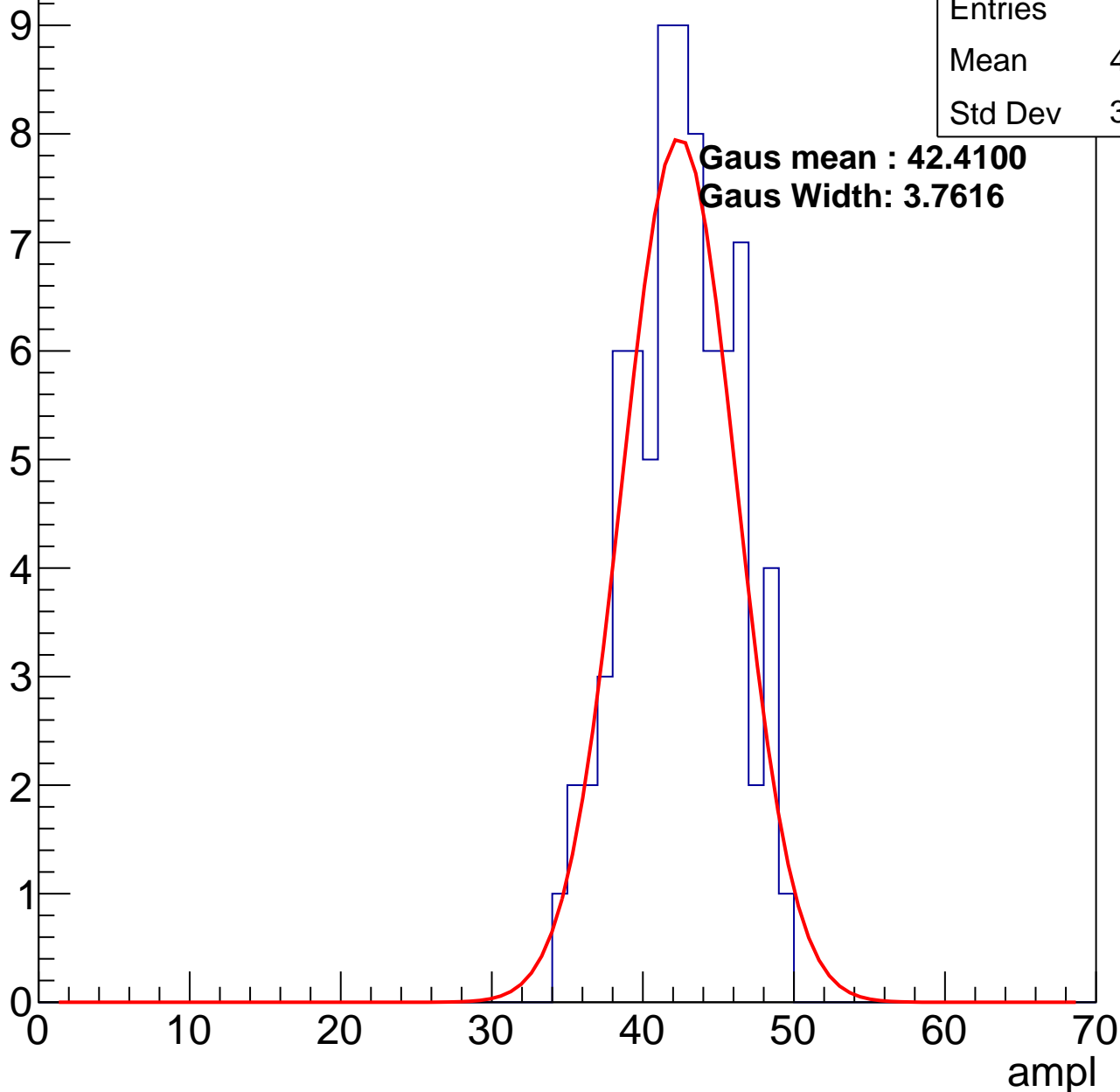
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	77
Mean	41.96
Std Dev	3.473

**Gaus mean : 42.4100**

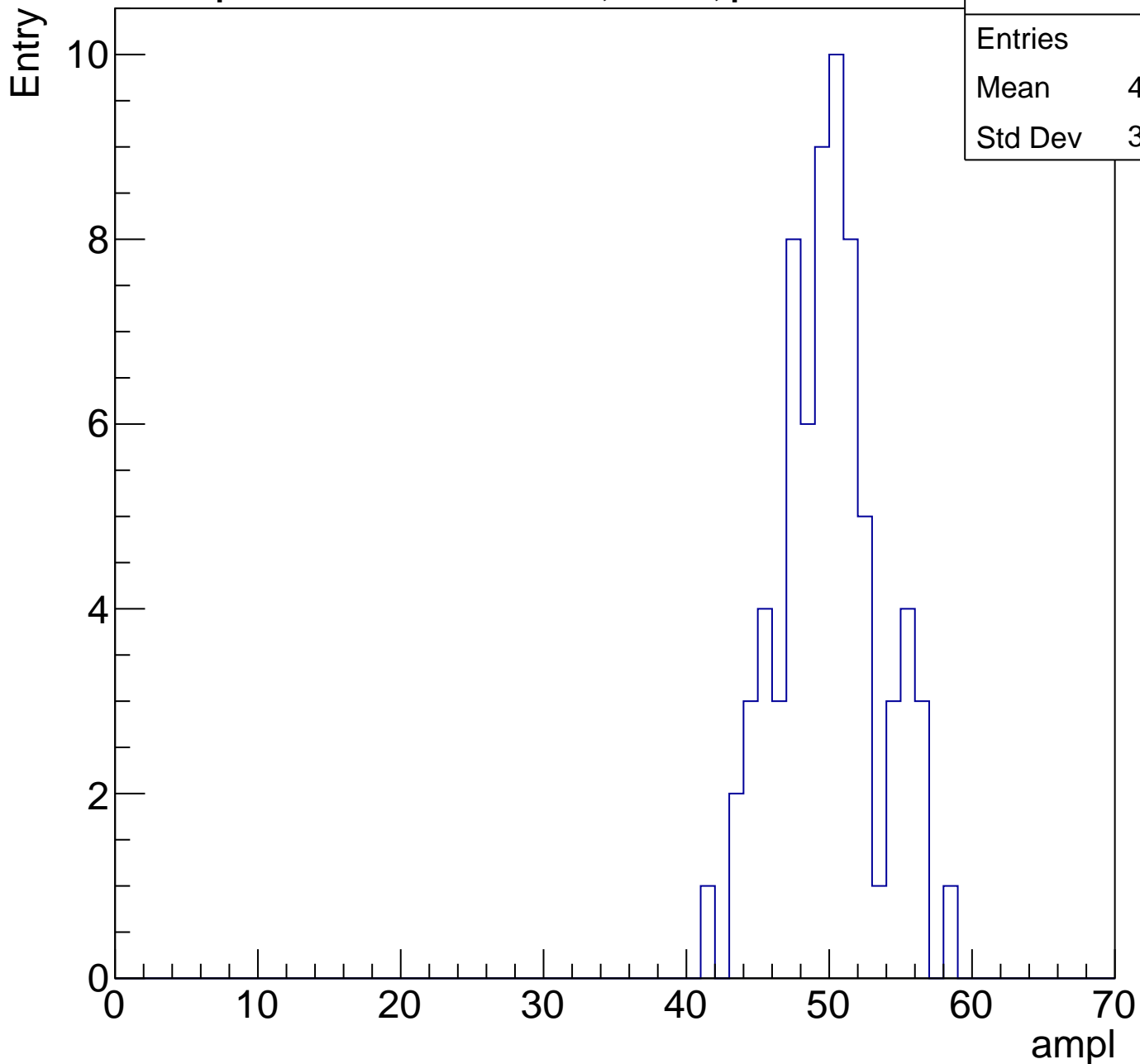
**Gaus Width: 3.7616**



# B1L102S, U16-ch117, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

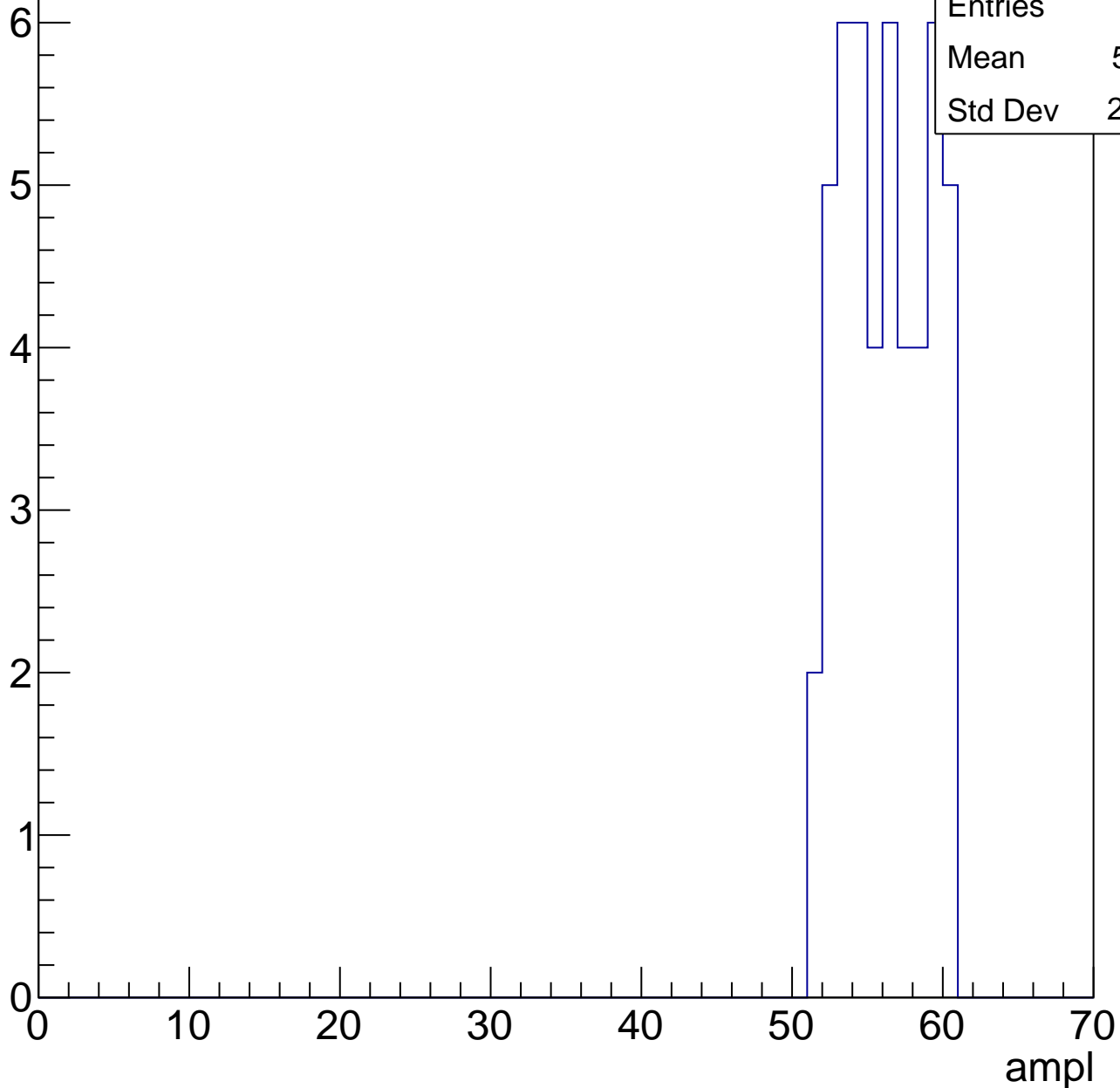
Entries	71
Mean	49.45
Std Dev	3.512



# B1L102S, U16-ch117, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



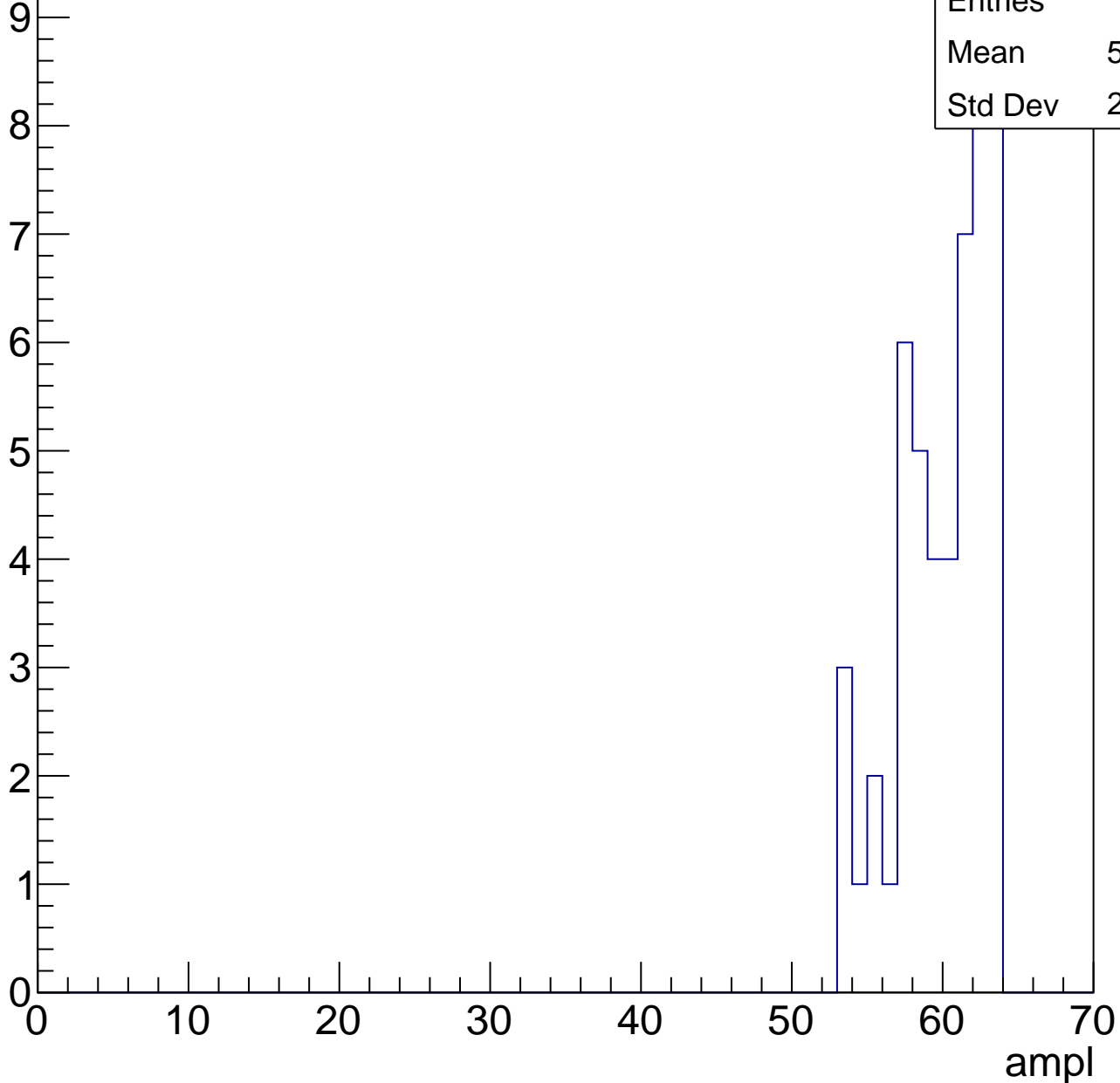
Entries	48
Mean	55.71
Std Dev	2.746

# B1L102S, U16-ch117, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

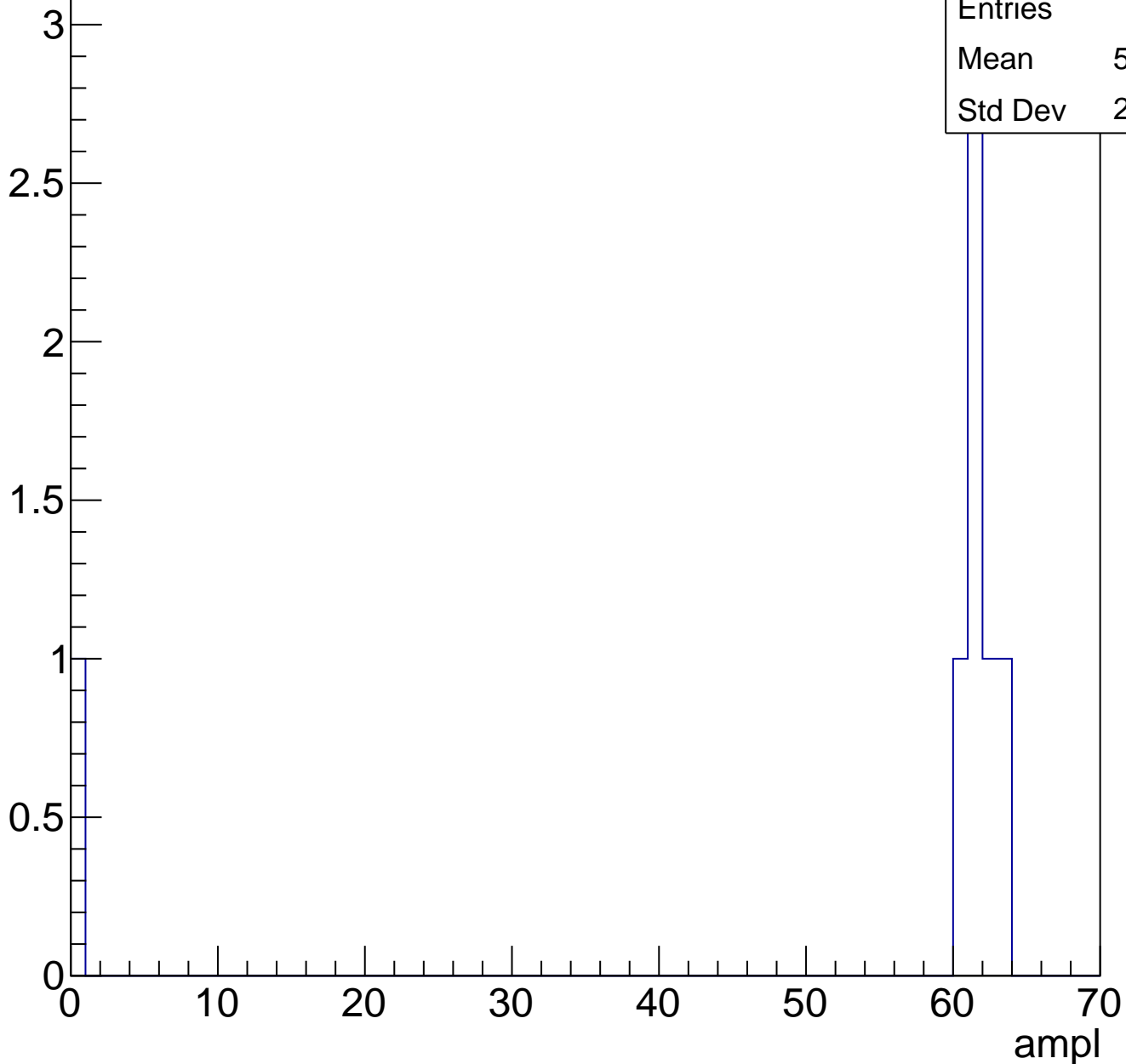
Entries	51
Mean	59.59
Std Dev	2.945



# B1L102S, U16-ch117, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

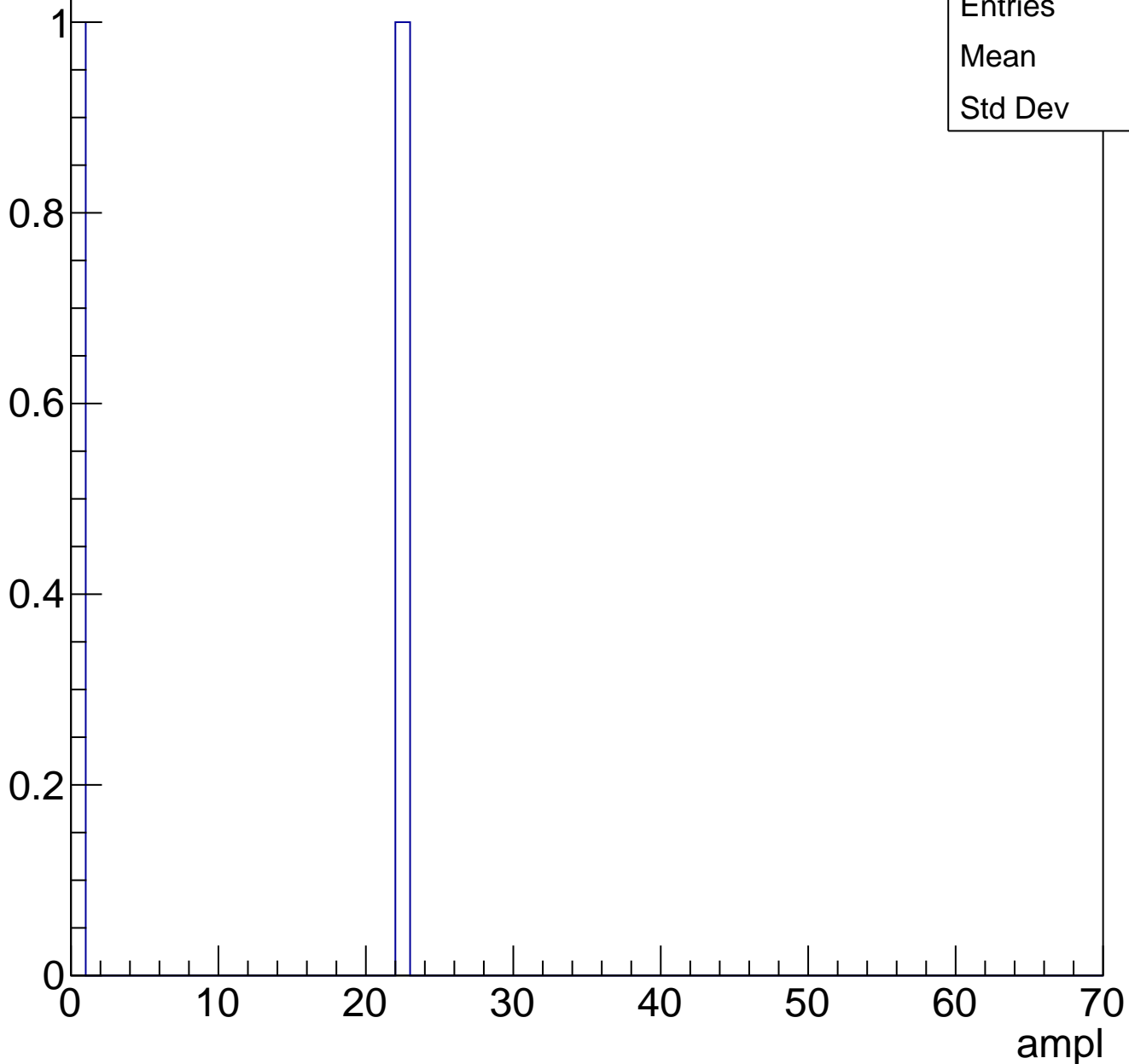




# B1L102S, U16-ch117, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch118, adc0

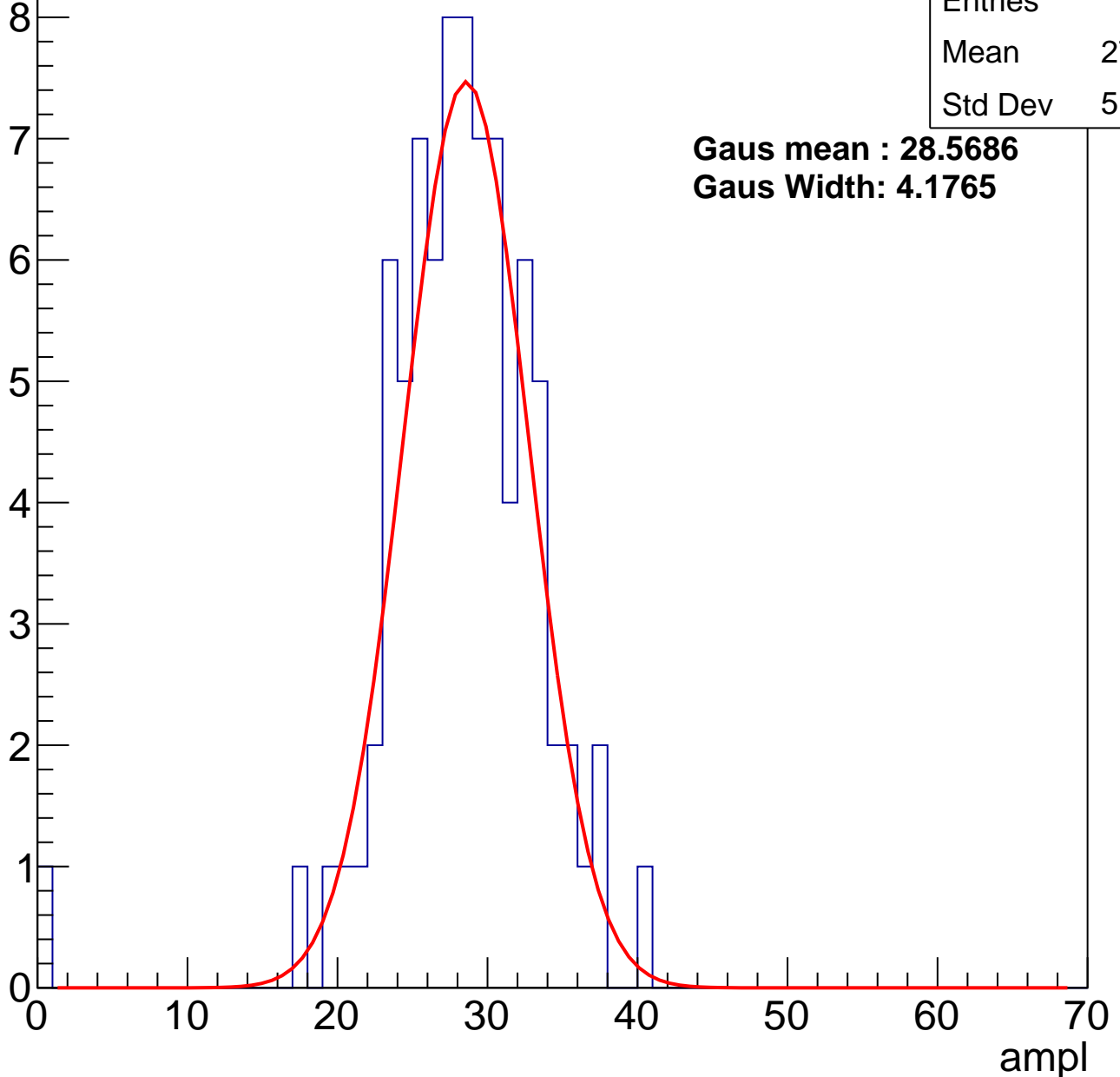
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	84
Mean	27.76
Std Dev	5.259

**Gaus mean : 28.5686**

**Gaus Width: 4.1765**



# B1L102S, U16-ch118, adc1

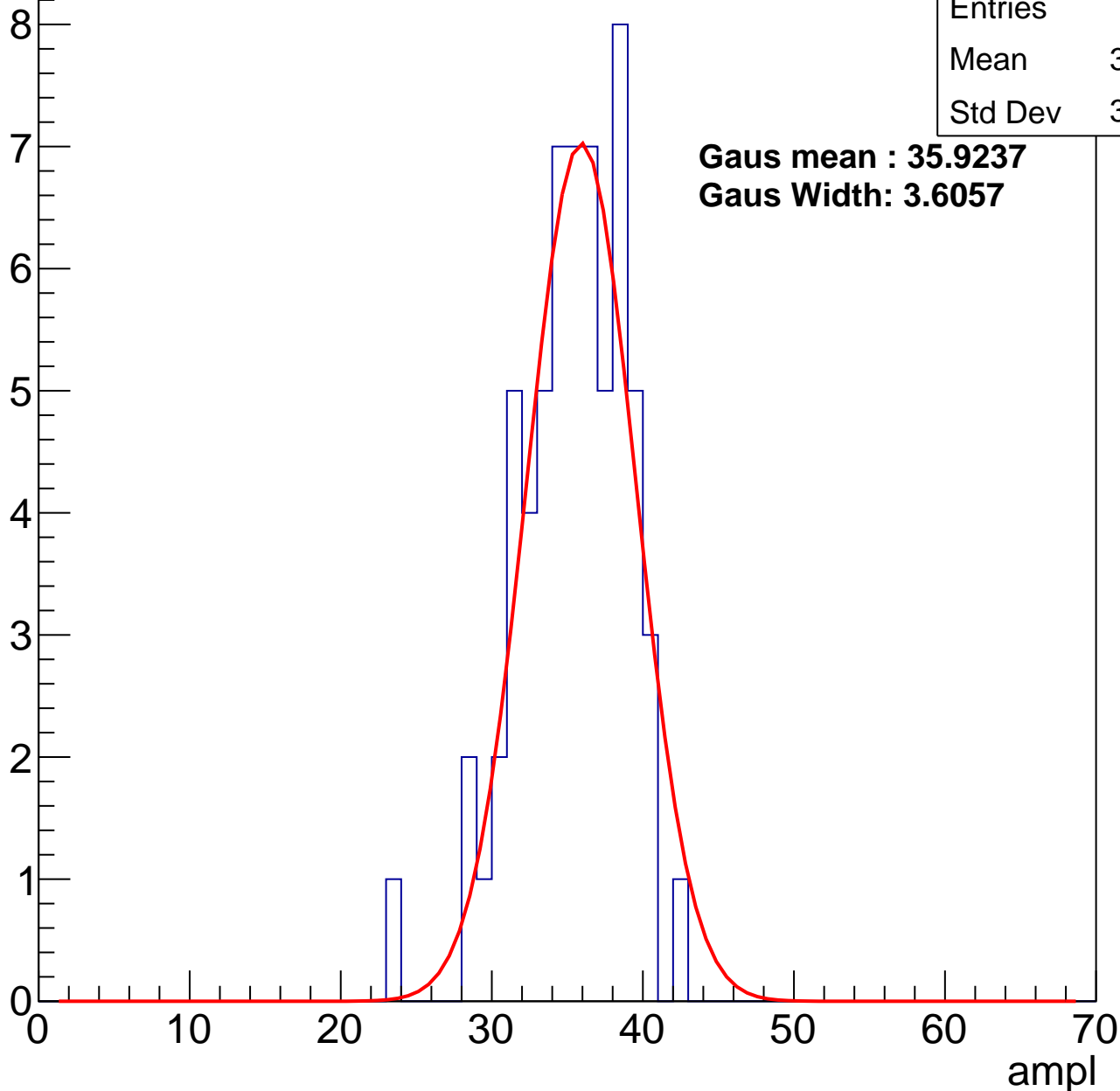
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	34.87
Std Dev	3.503

**Gaus mean : 35.9237**

**Gaus Width: 3.6057**



# B1L102S, U16-ch118, adc2

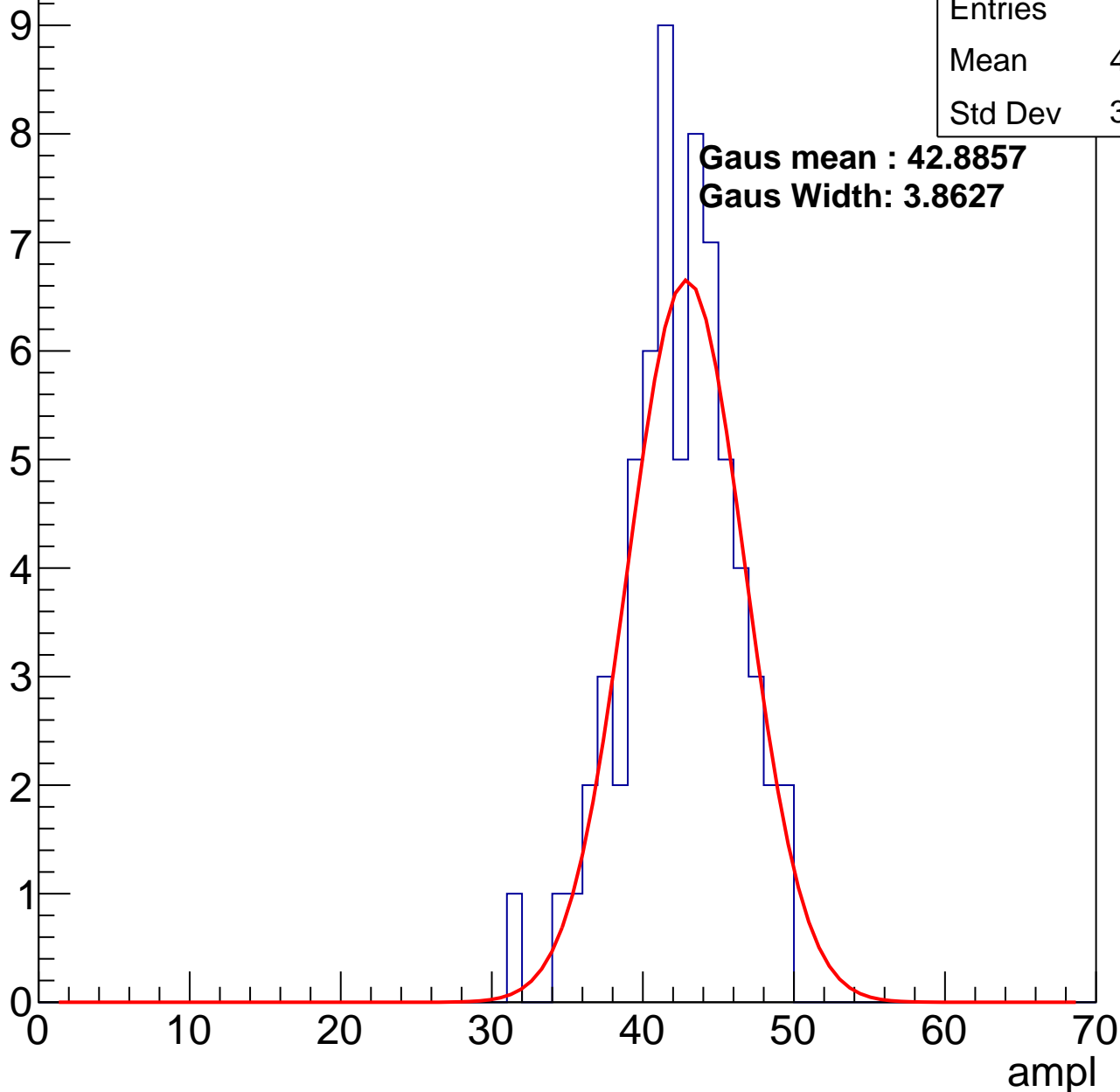
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	41.95
Std Dev	3.653

**Gaus mean : 42.8857**

**Gaus Width: 3.8627**

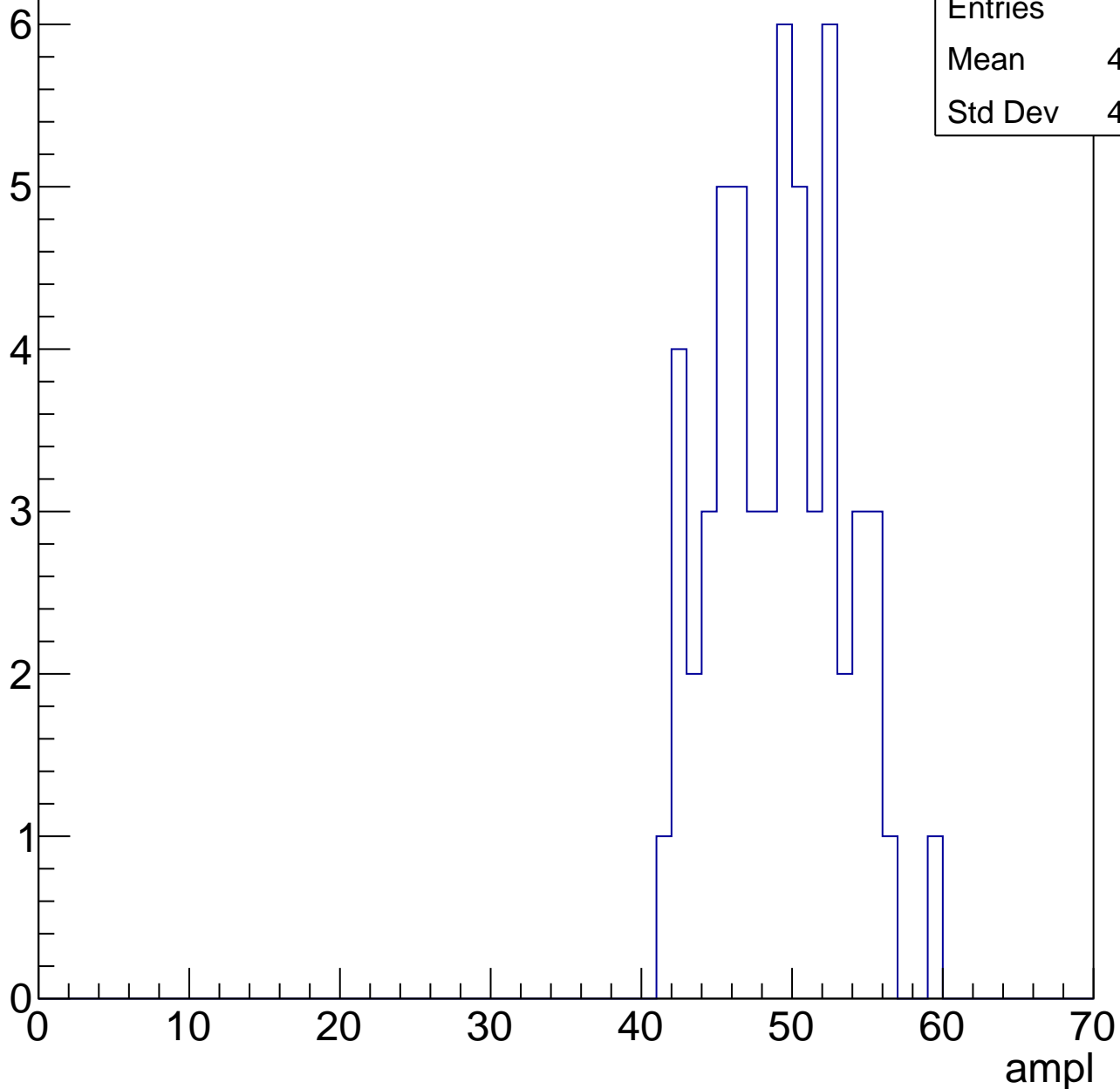


# B1L102S, U16-ch118, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	48.64
Std Dev	4.172

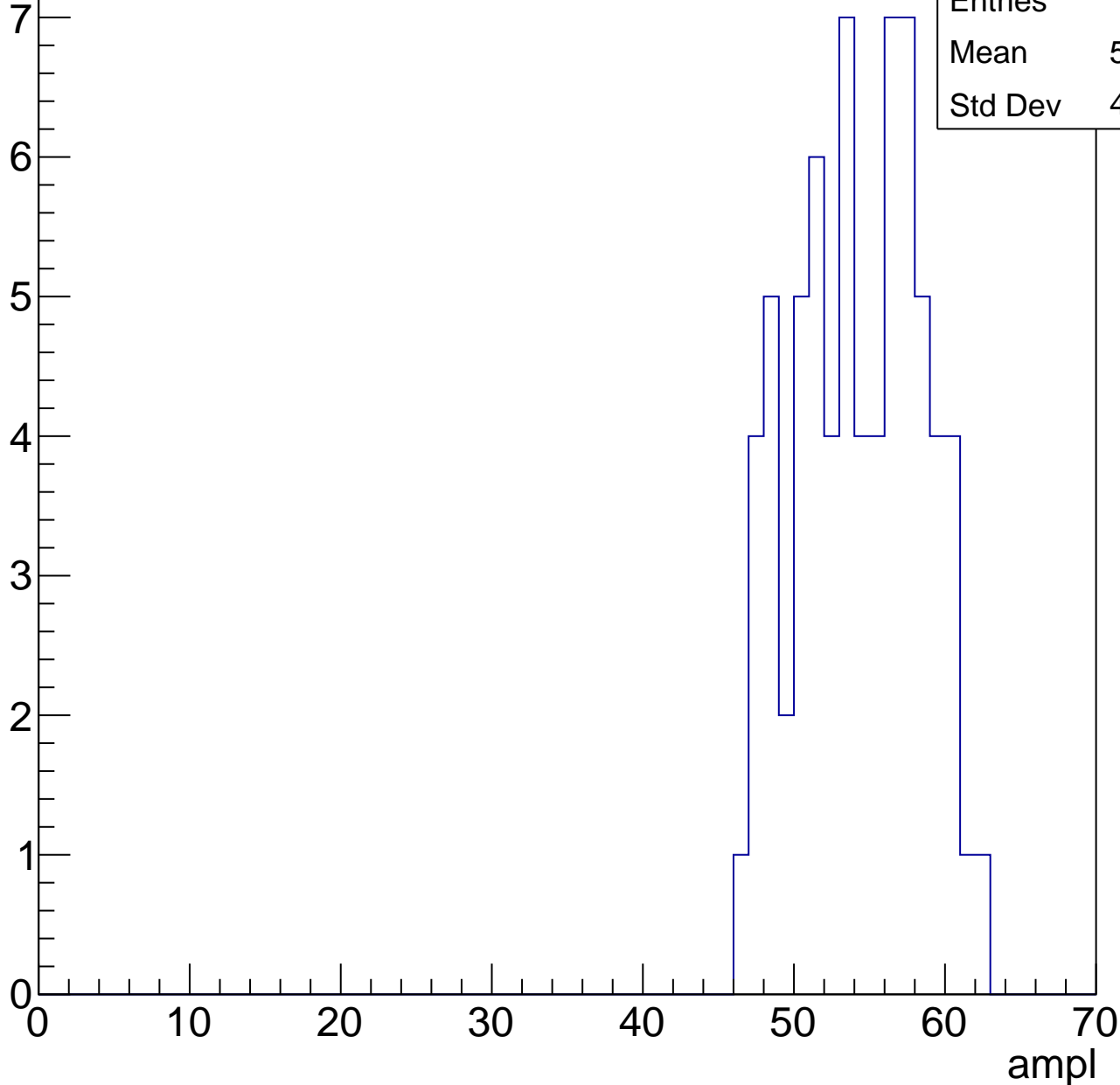


# B1L102S, U16-ch118, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	53.85
Std Dev	4.072

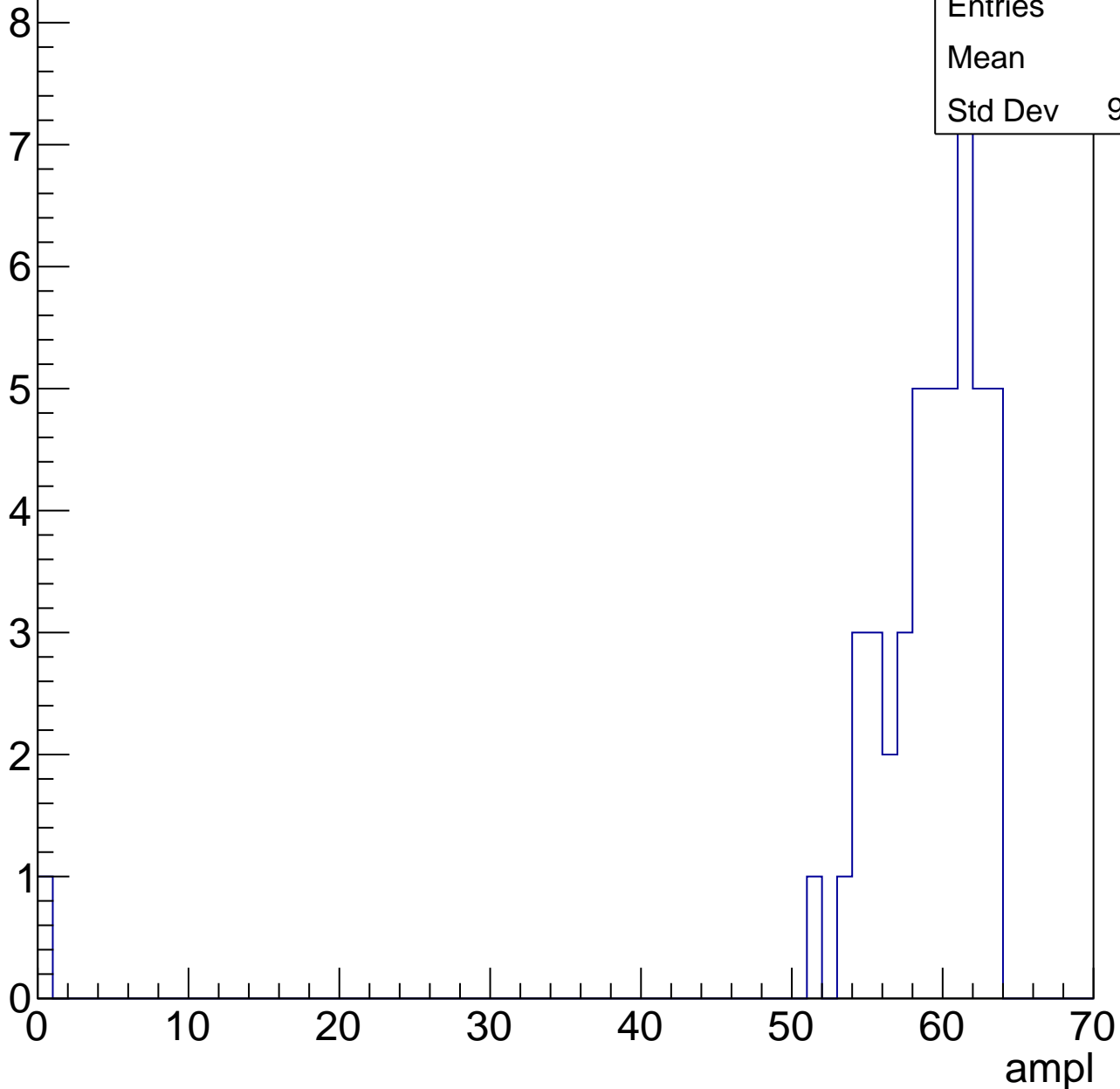


# B1L102S, U16-ch118, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

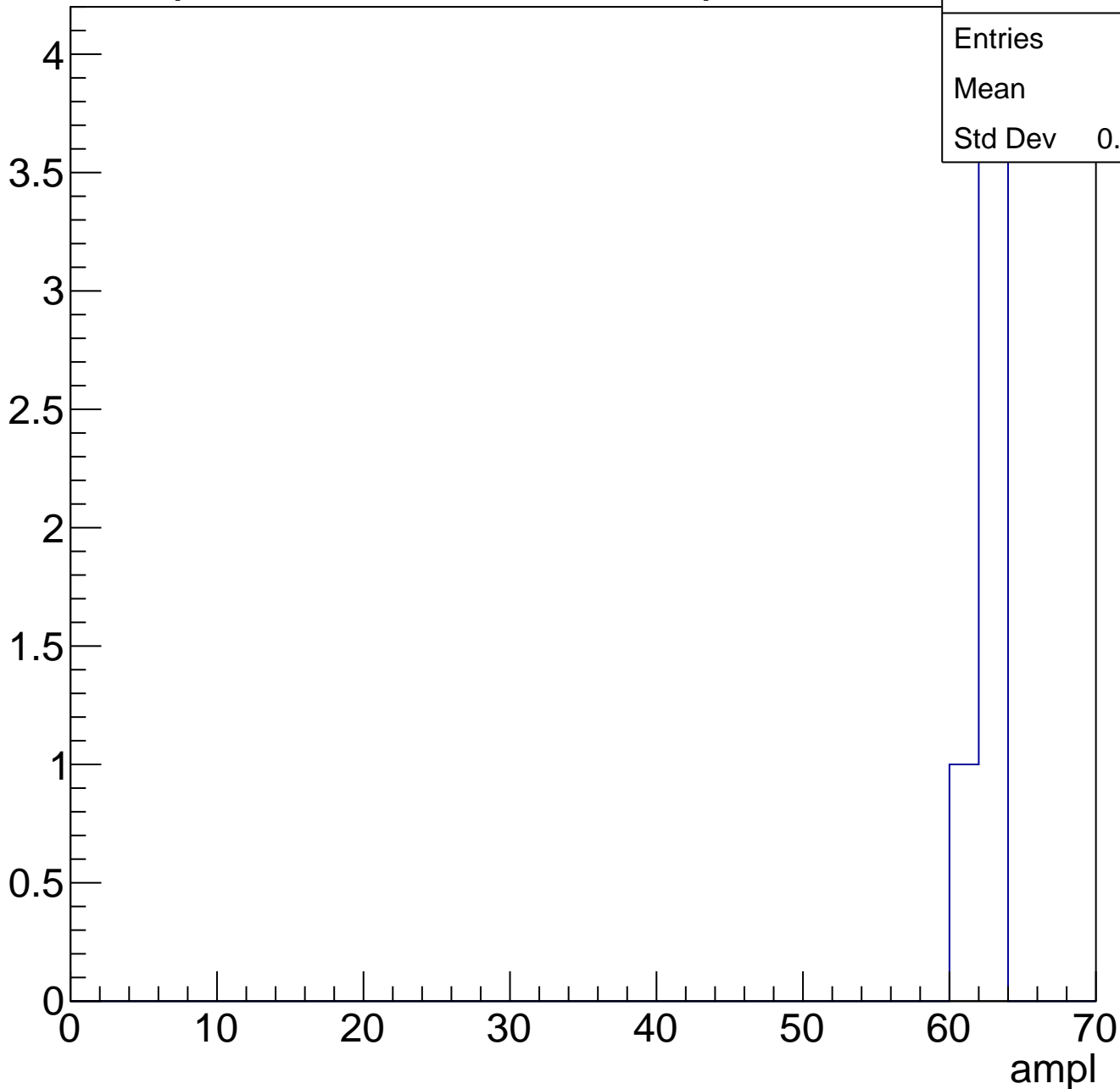
Entries	47
Mean	57.7
Std Dev	9.018



# B1L102S, U16-ch118, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	10
Mean	62.1
Std Dev	0.9434



# B1L102S, U16-ch118, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch119, adc0

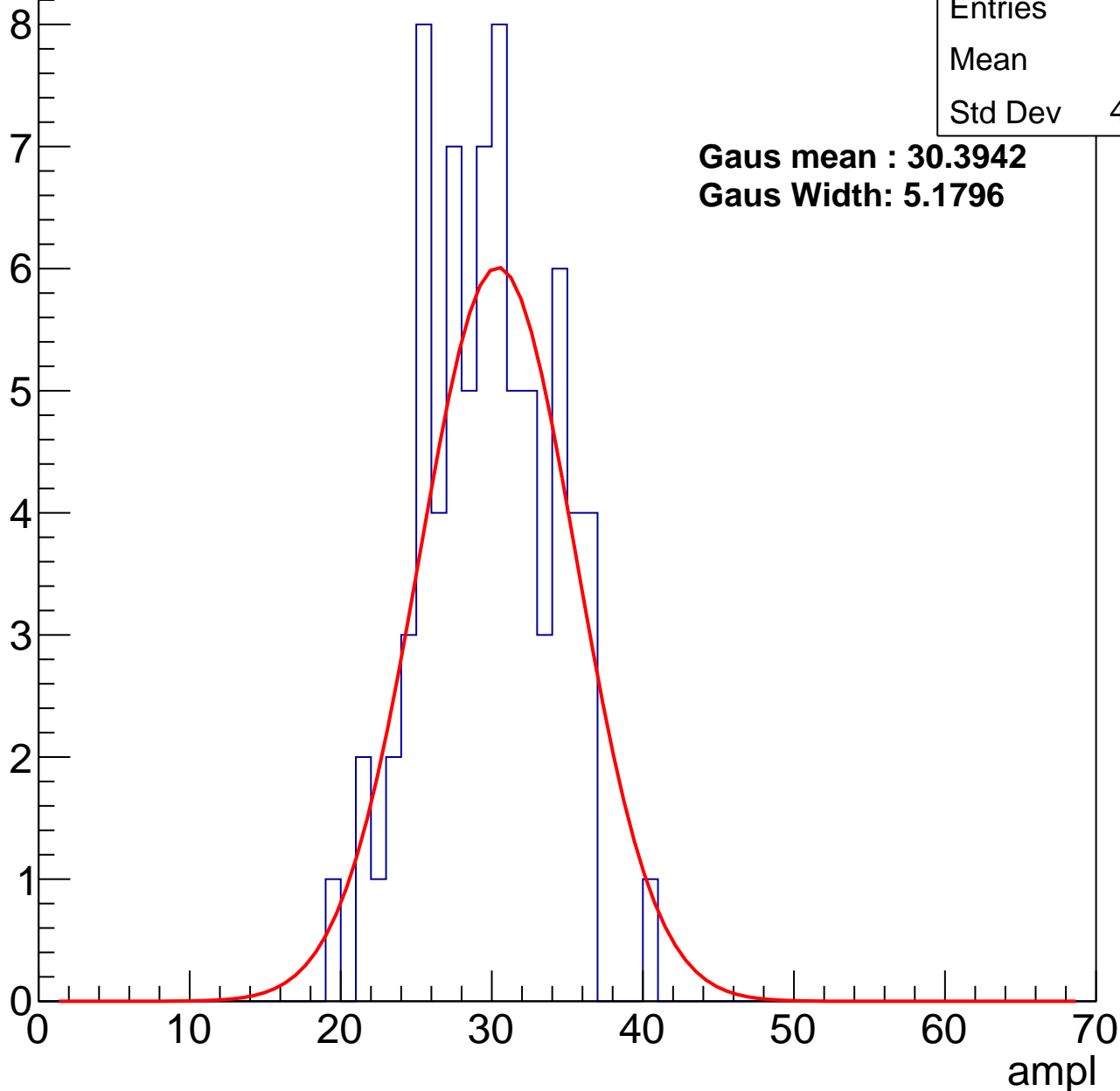
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	29.2
Std Dev	4.215

**Gaus mean : 30.3942**

**Gaus Width: 5.1796**



# B1L102S, U16-ch119, adc1

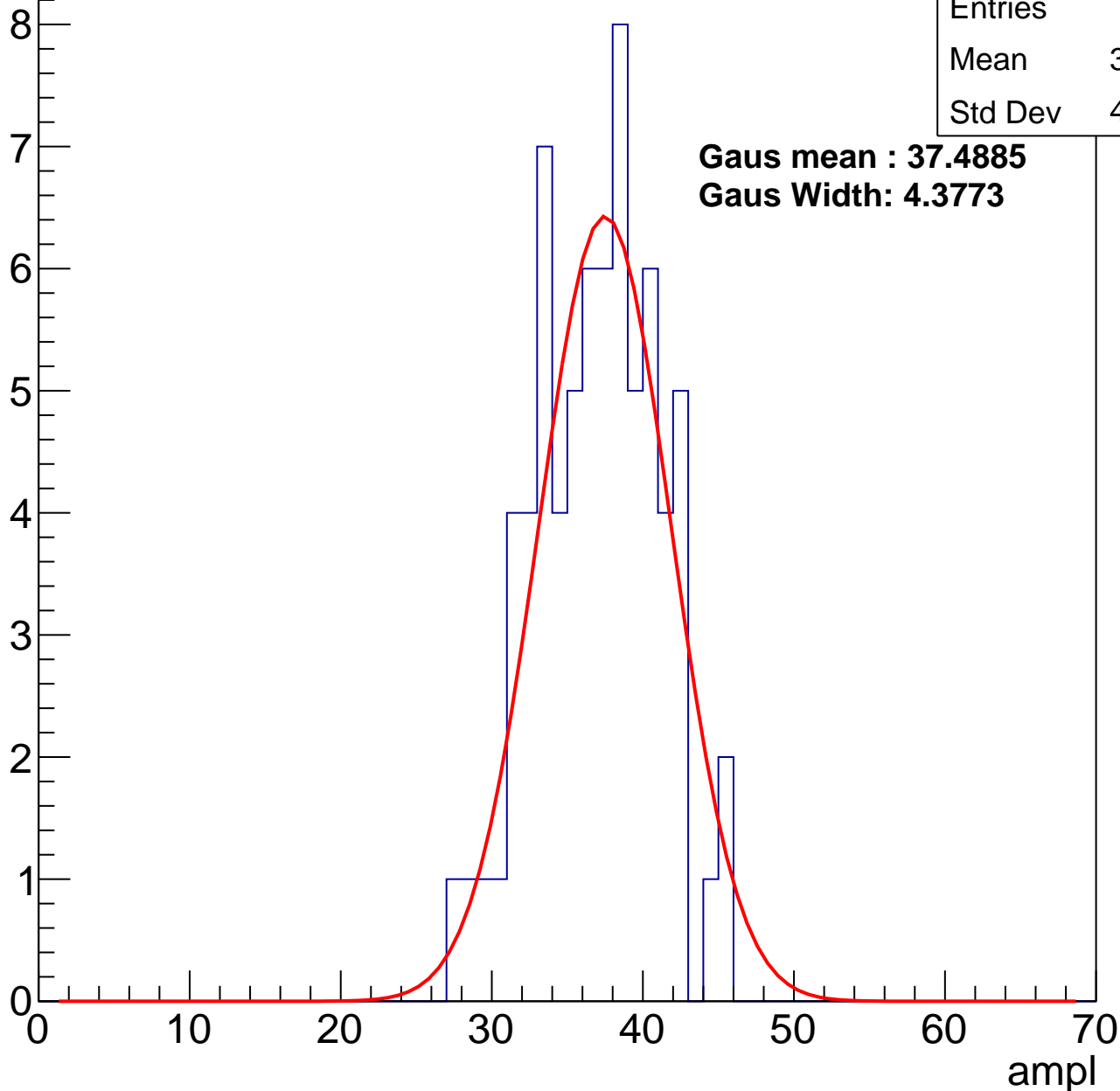
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	36.52
Std Dev	4.014

**Gaus mean : 37.4885**

**Gaus Width: 4.3773**



# B1L102S, U16-ch119, adc2

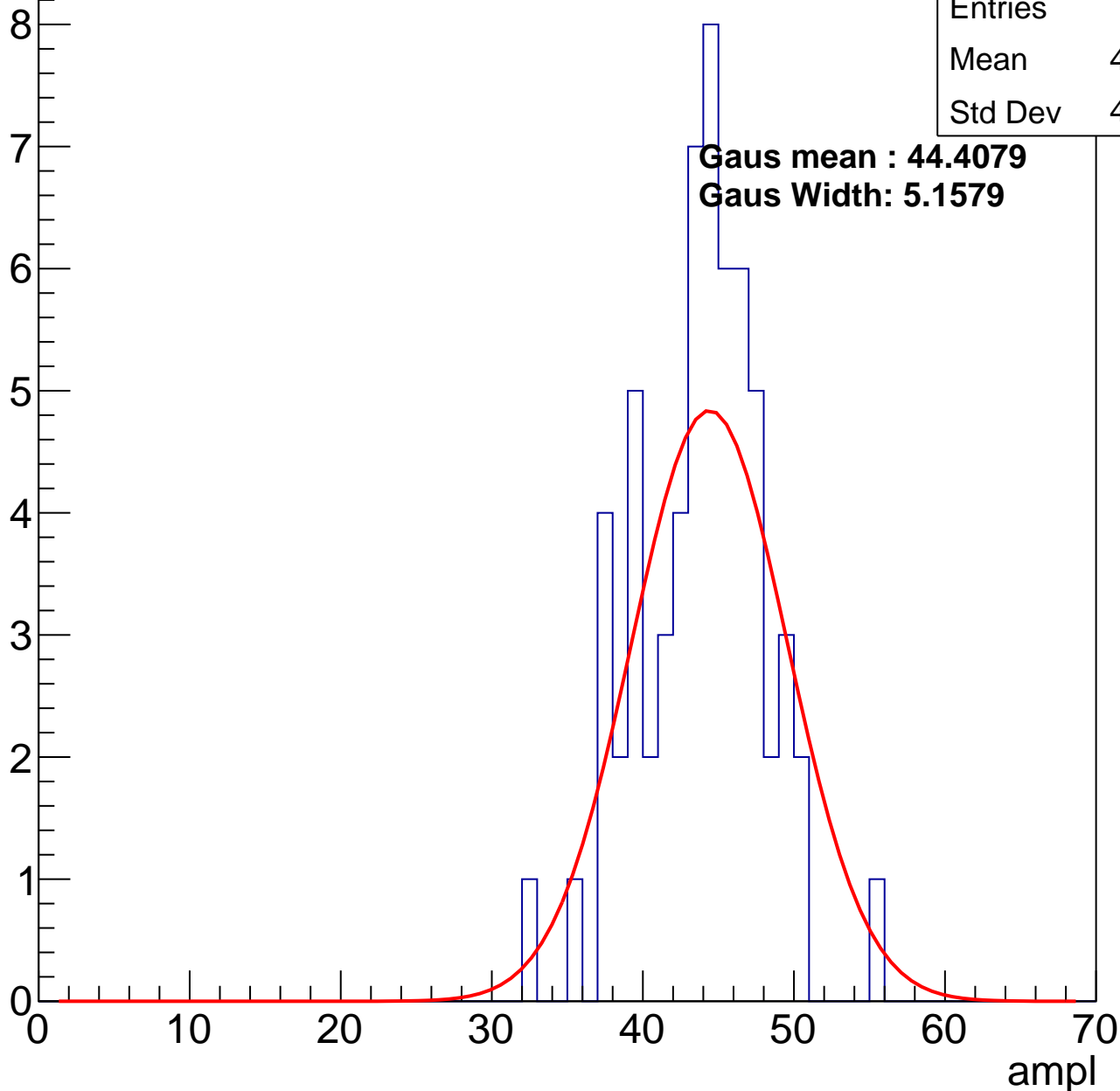
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	62
Mean	43.37
Std Dev	4.116

**Gaus mean : 44.4079**

**Gaus Width: 5.1579**

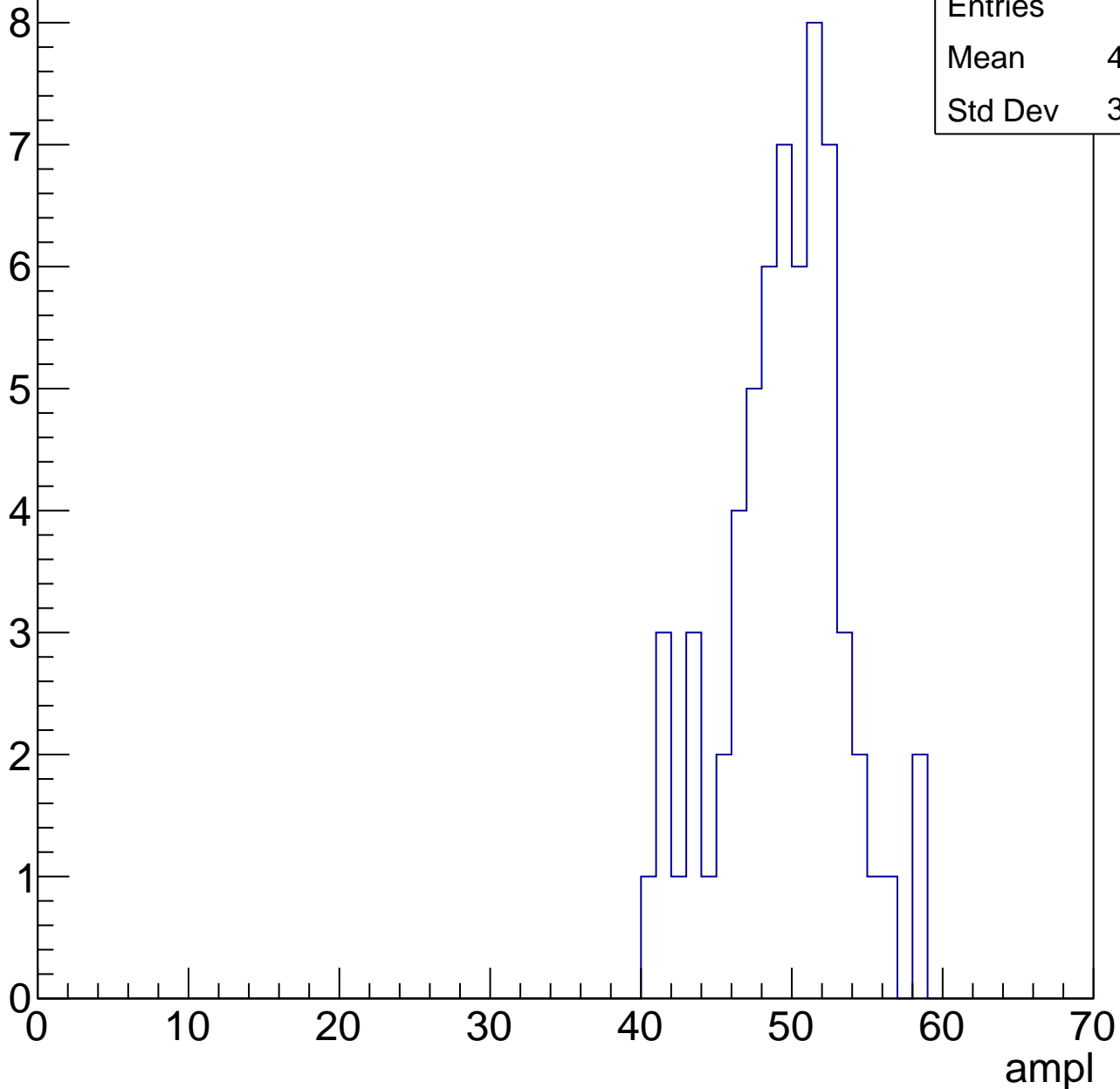


# B1L102S, U16-ch119, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	48.95
Std Dev	3.974

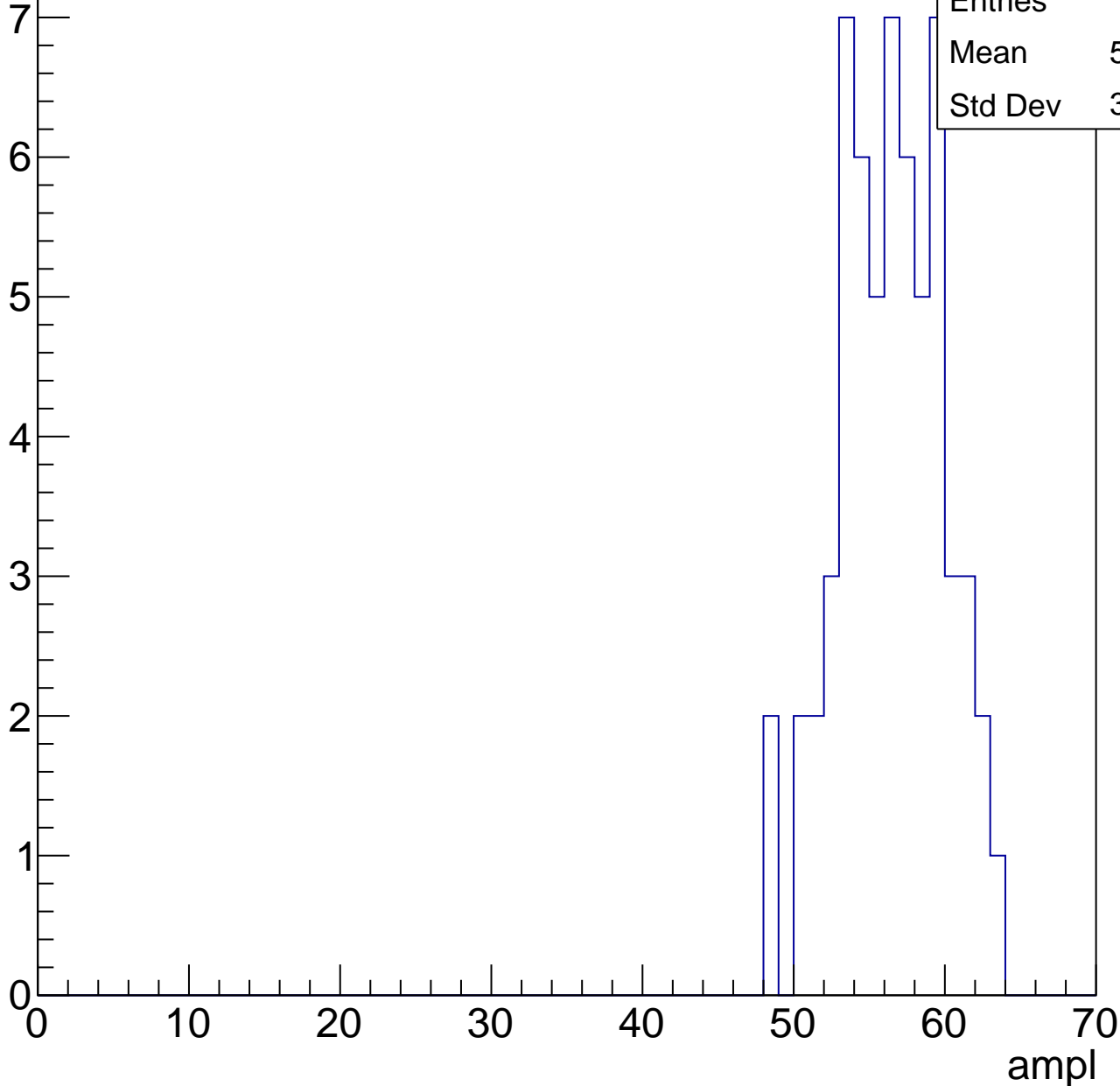


# B1L102S, U16-ch119, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	61
Mean	55.92
Std Dev	3.442

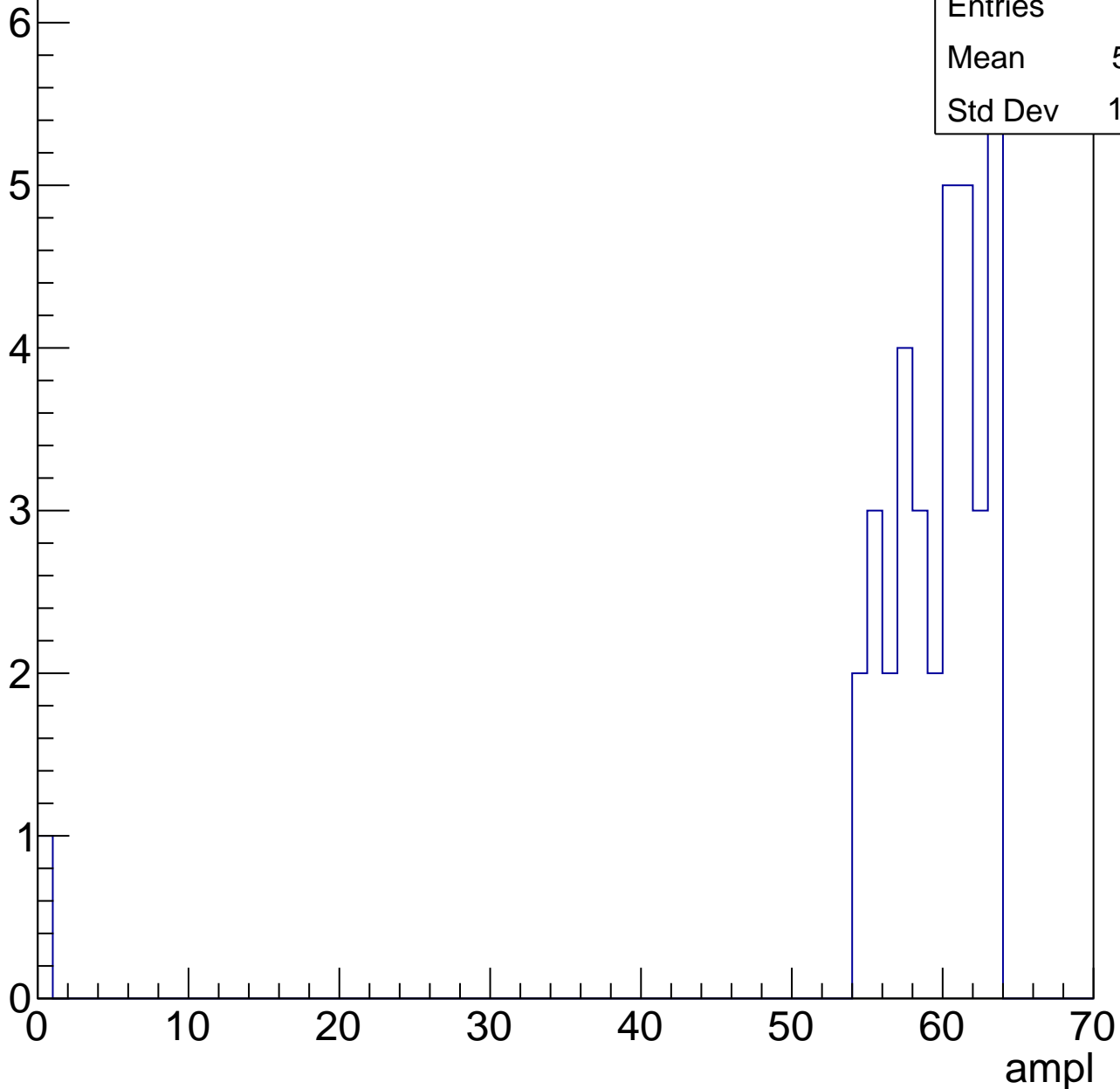


# B1L102S, U16-ch119, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	36
Mean	57.61
Std Dev	10.13

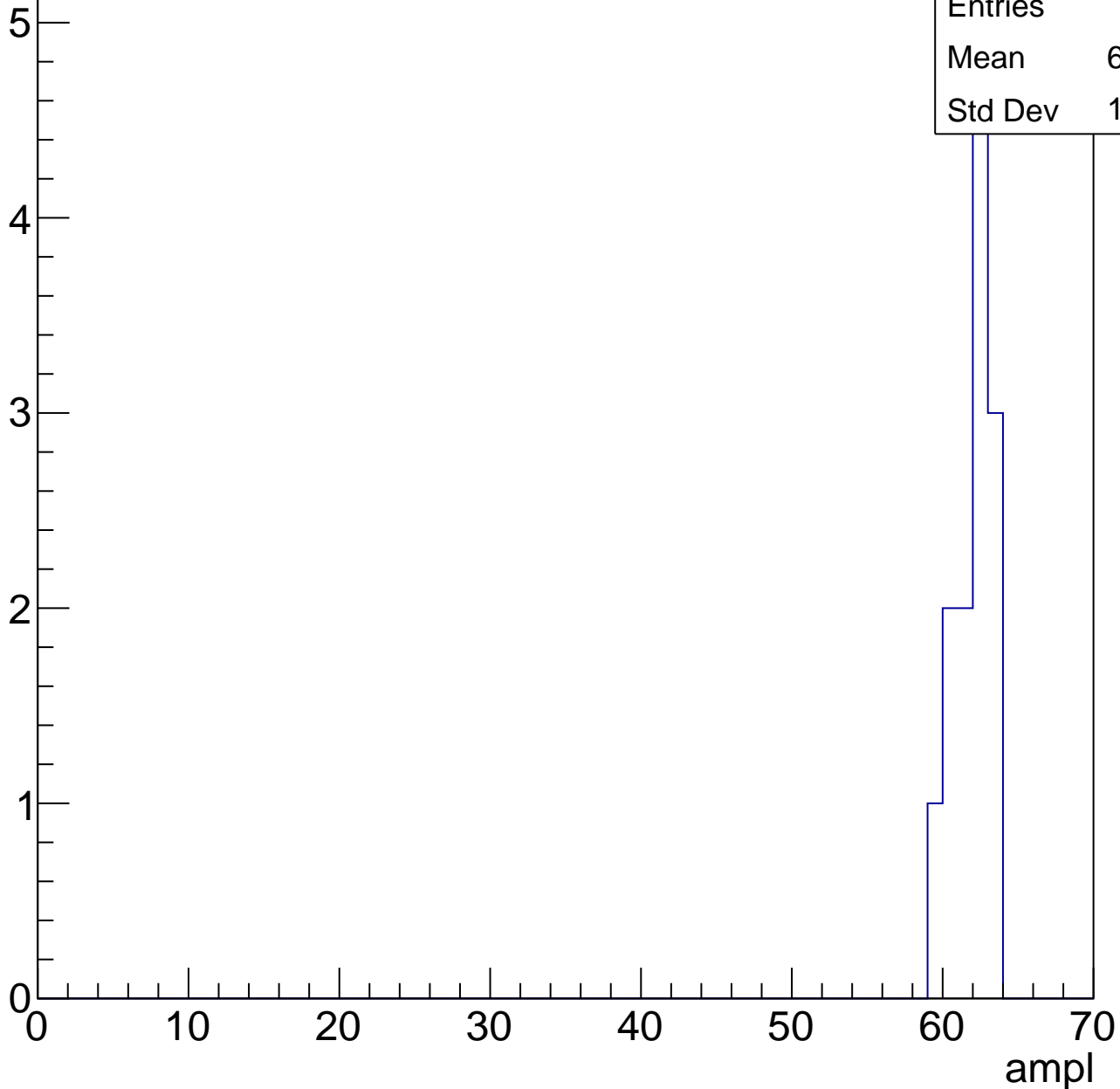


# B1L102S, U16-ch119, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	13
Mean	61.54
Std Dev	1.216

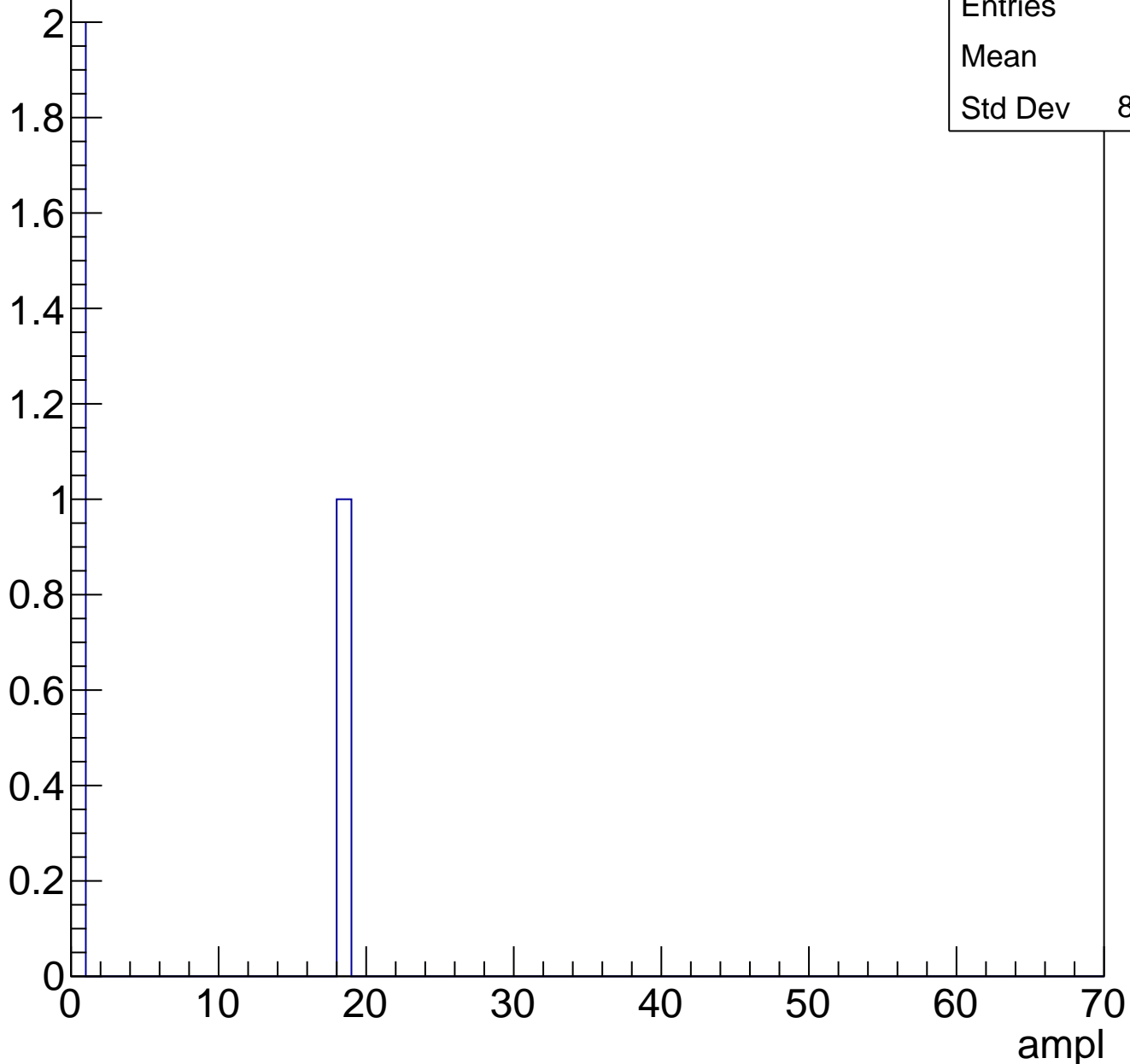




# B1L102S, U16-ch119, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	3
Mean	6
Std Dev	8.485

# B1L102S, U16-ch120, adc0

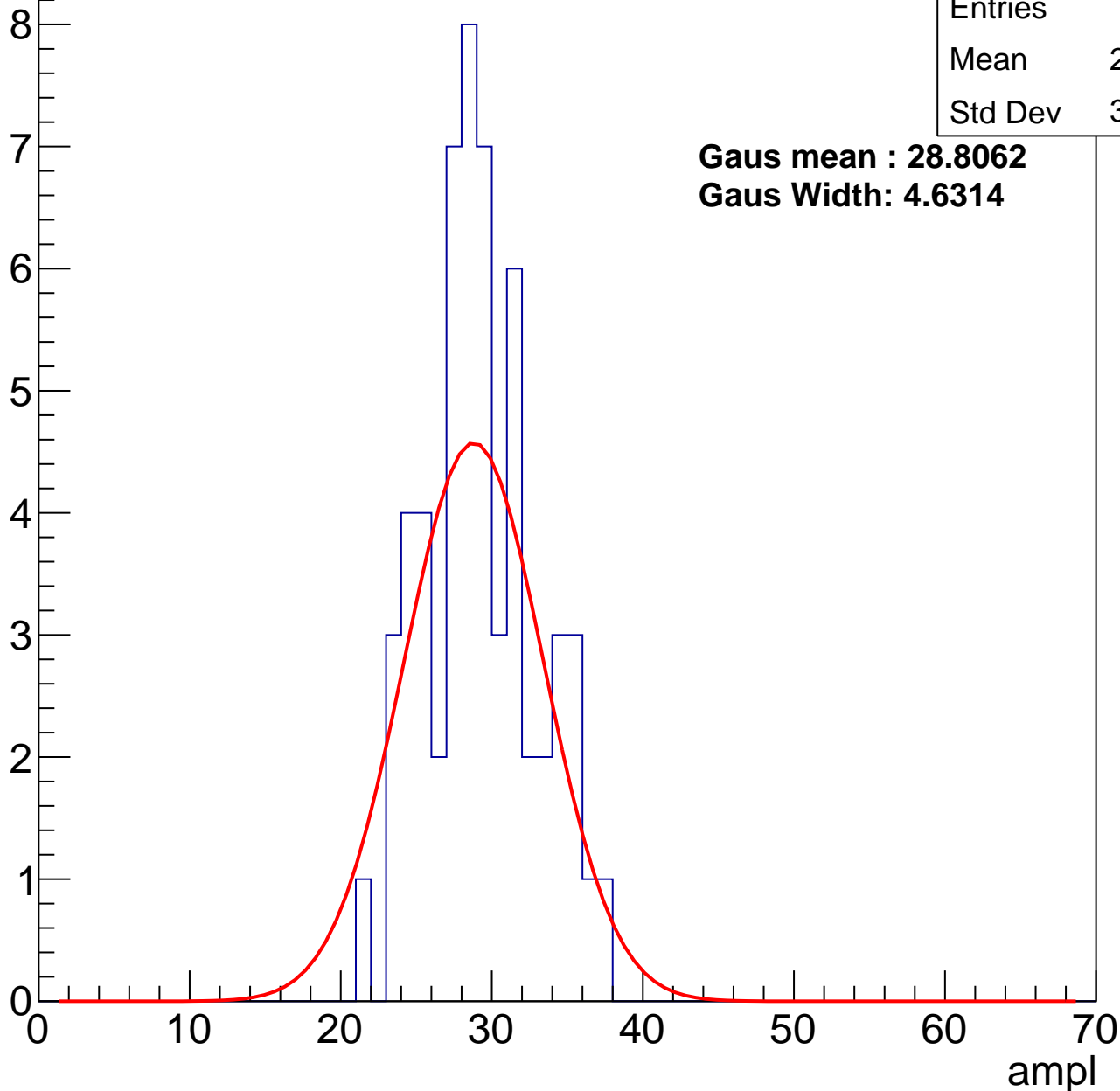
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	28.77
Std Dev	3.652

**Gaus mean : 28.8062**

**Gaus Width: 4.6314**



# B1L102S, U16-ch120, adc1

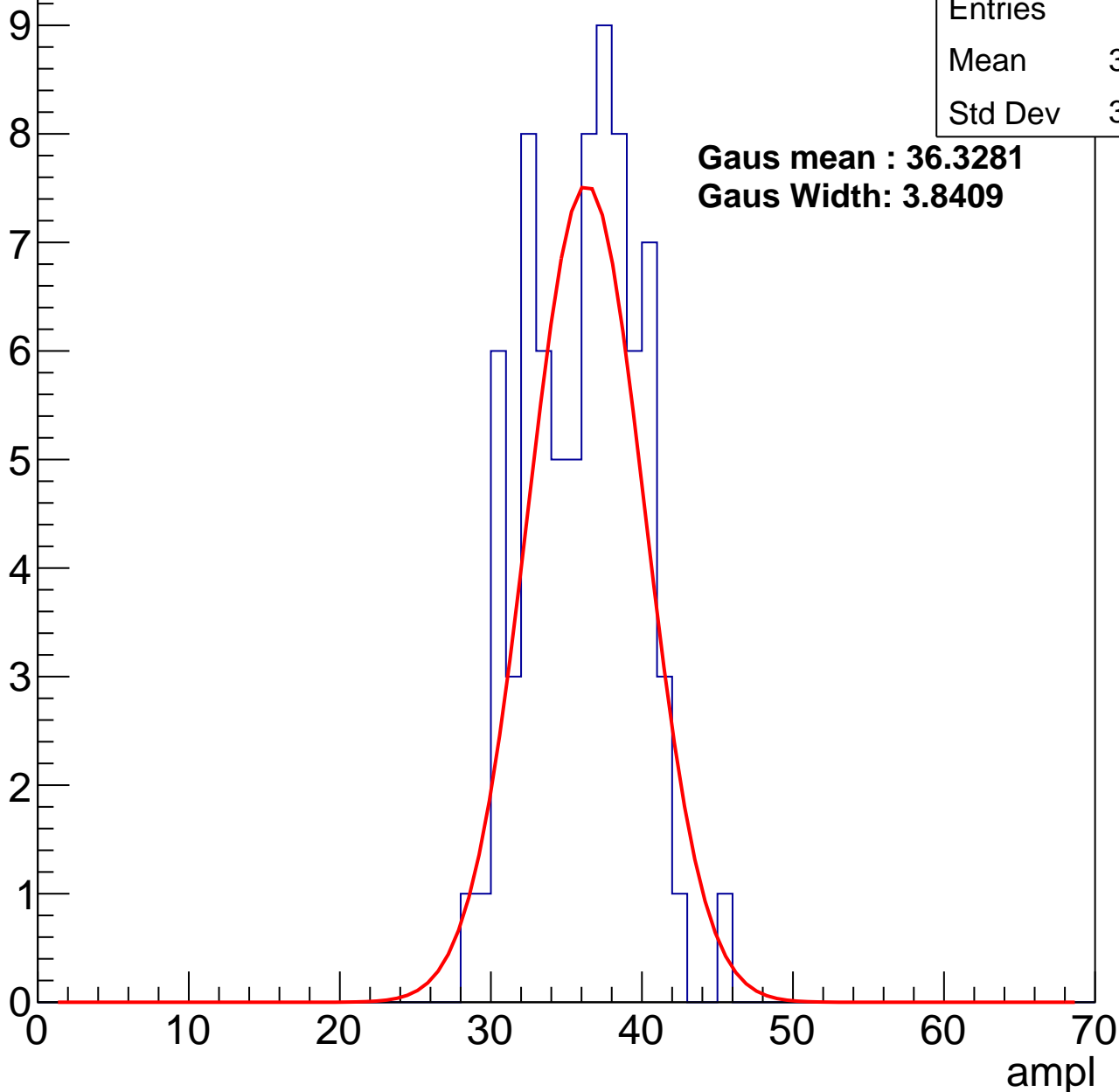
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	35.62
Std Dev	3.578

**Gaus mean : 36.3281**

**Gaus Width: 3.8409**



# B1L102S, U16-ch120, adc2

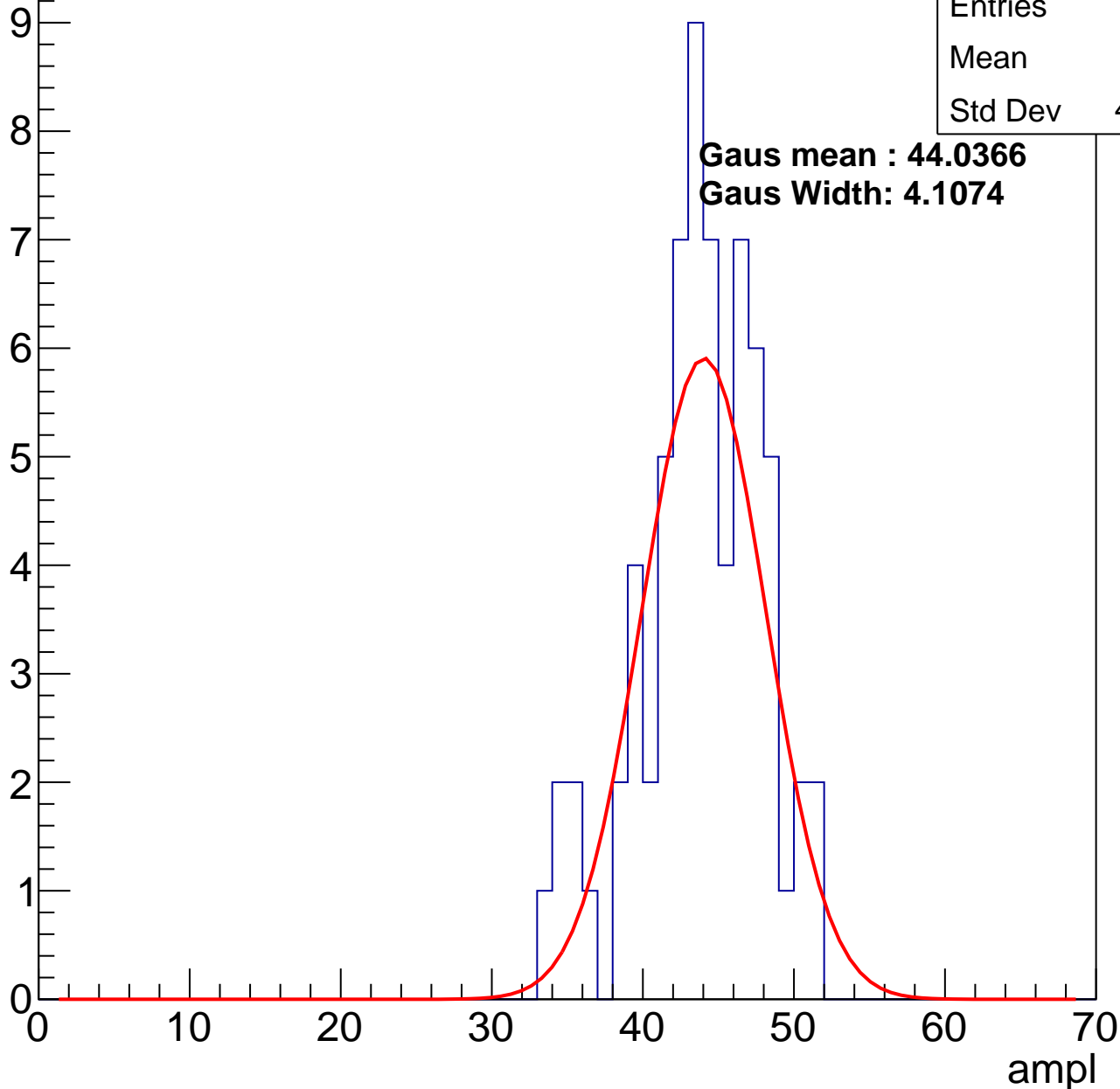
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	43.3
Std Dev	4.101

**Gaus mean : 44.0366**

**Gaus Width: 4.1074**

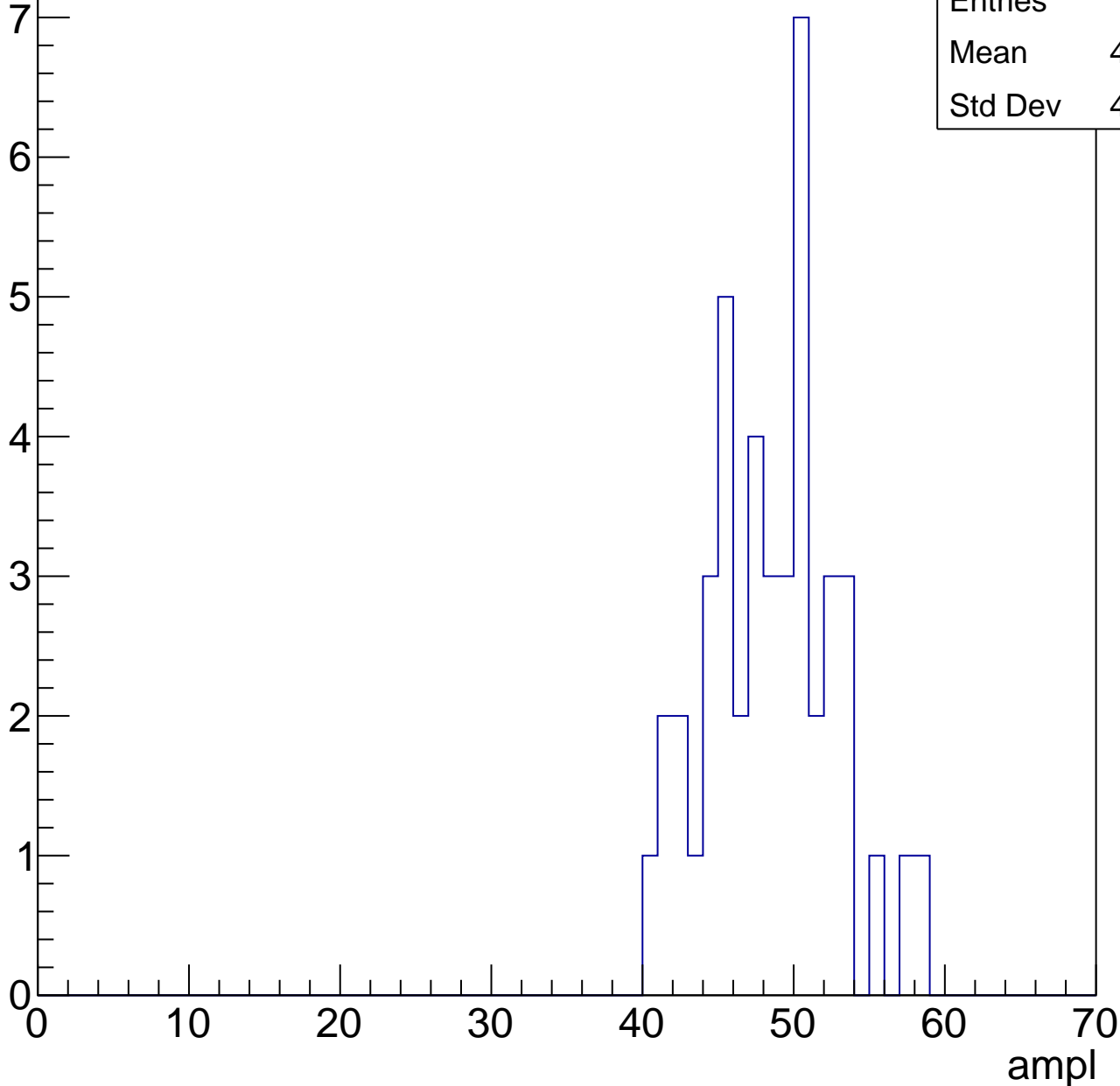


# B1L102S, U16-ch120, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	44
Mean	48.05
Std Dev	4.172

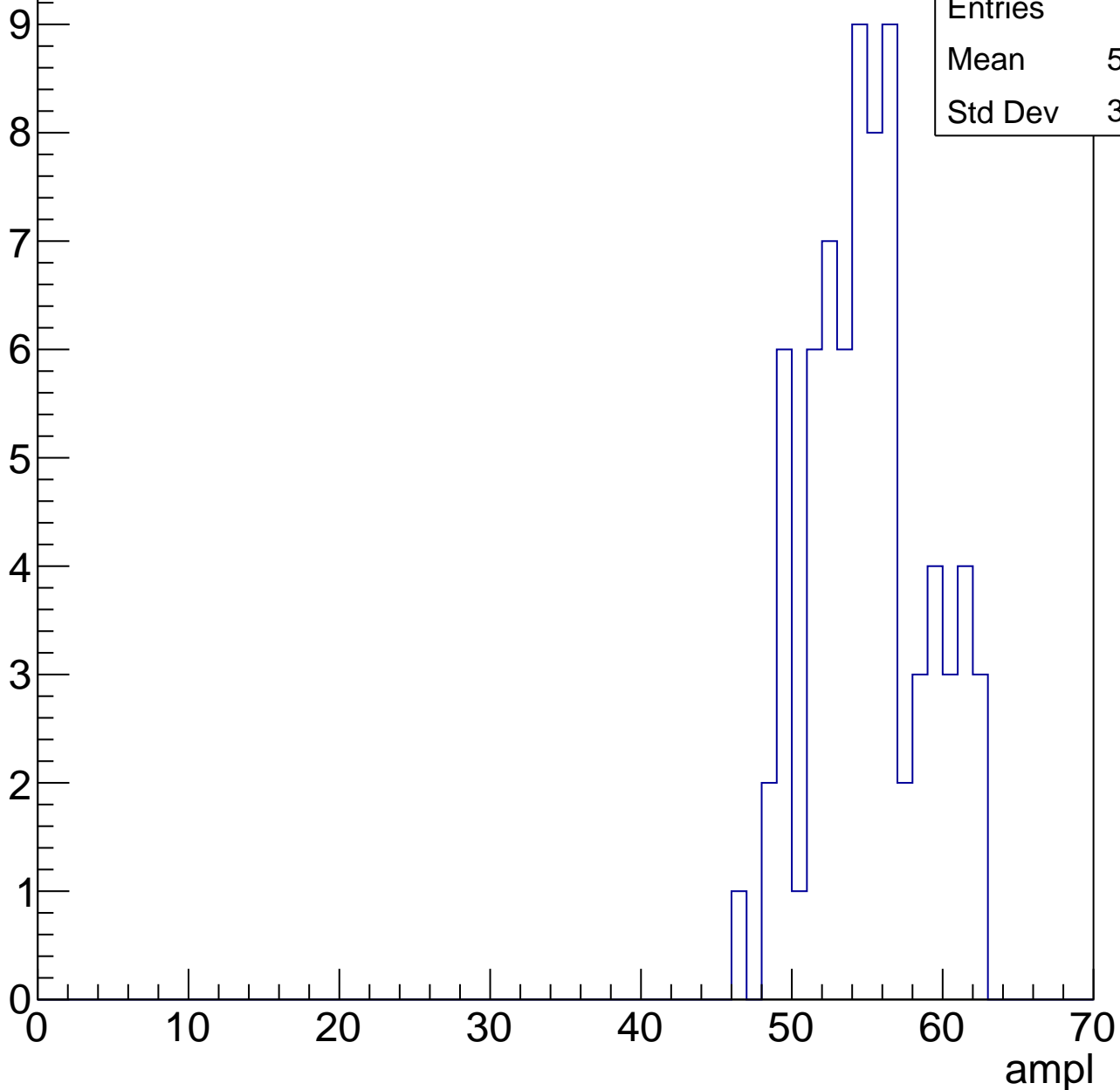


# B1L102S, U16-ch120, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	74
Mean	54.57
Std Dev	3.806

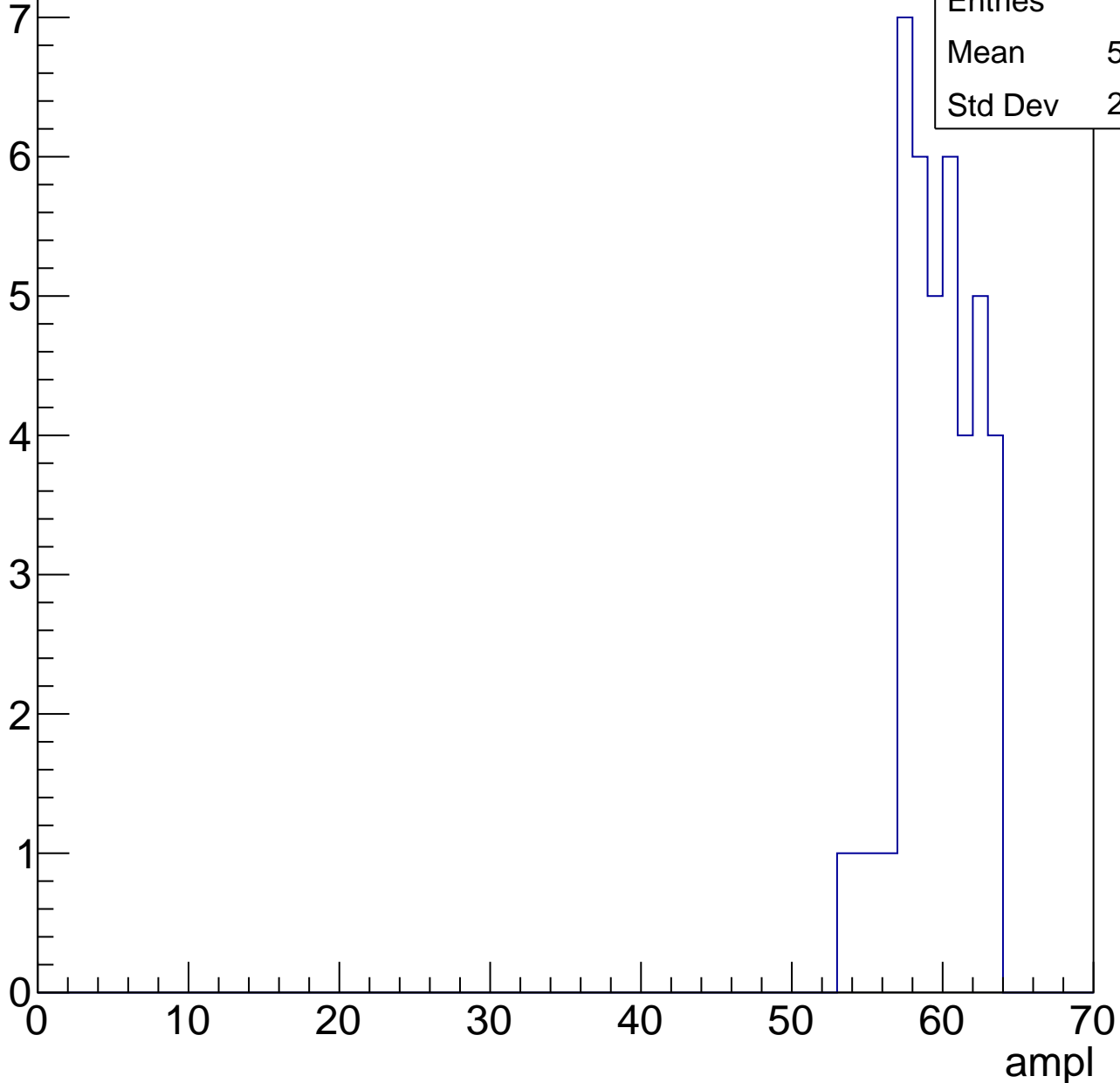


# B1L102S, U16-ch120, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

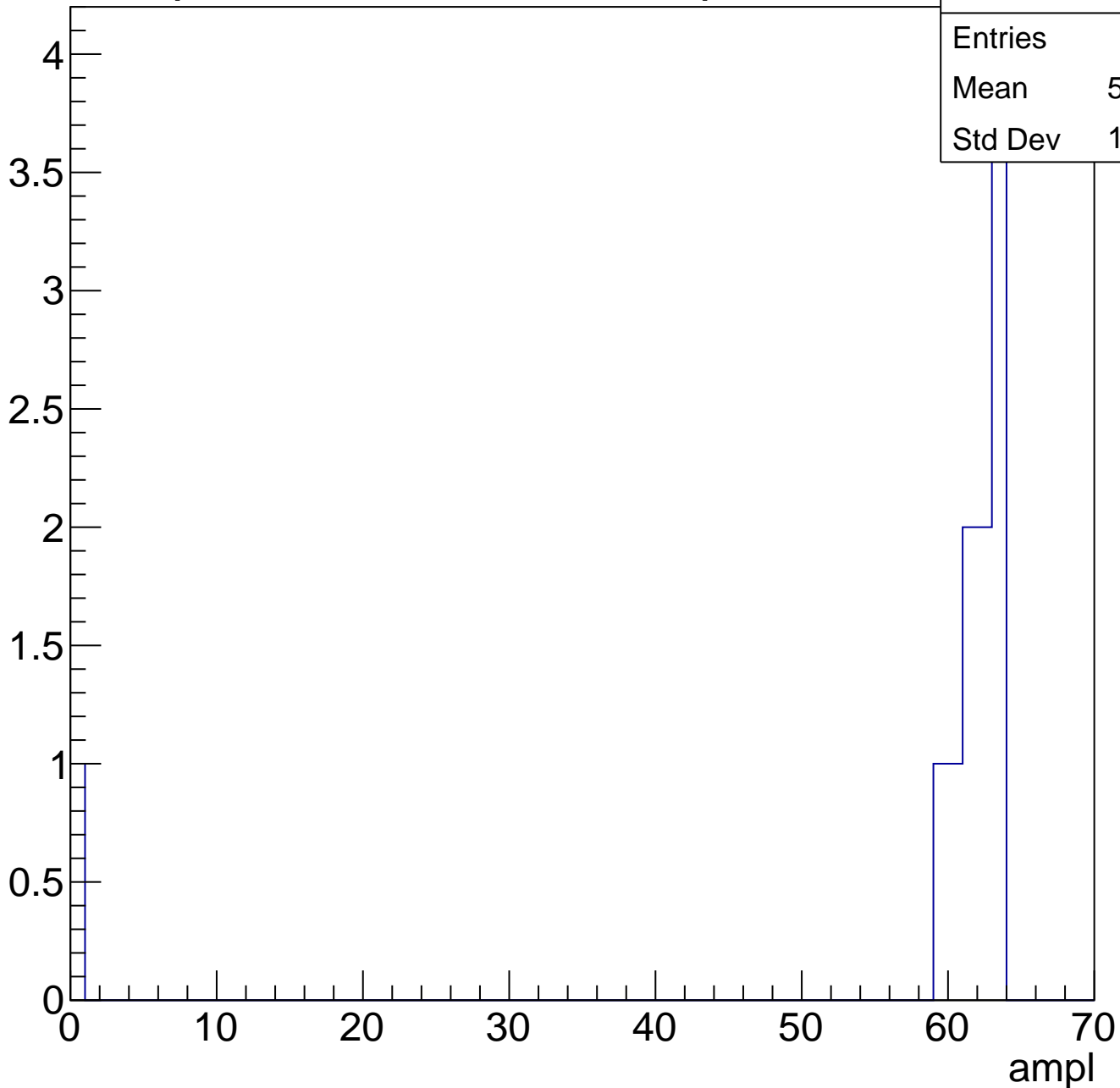
Entries	41
Mean	59.17
Std Dev	2.468



# B1L102S, U16-ch120, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch120, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch121, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	68
Mean	29.34
Std Dev	5.054

**Gaus mean : 30.5846**

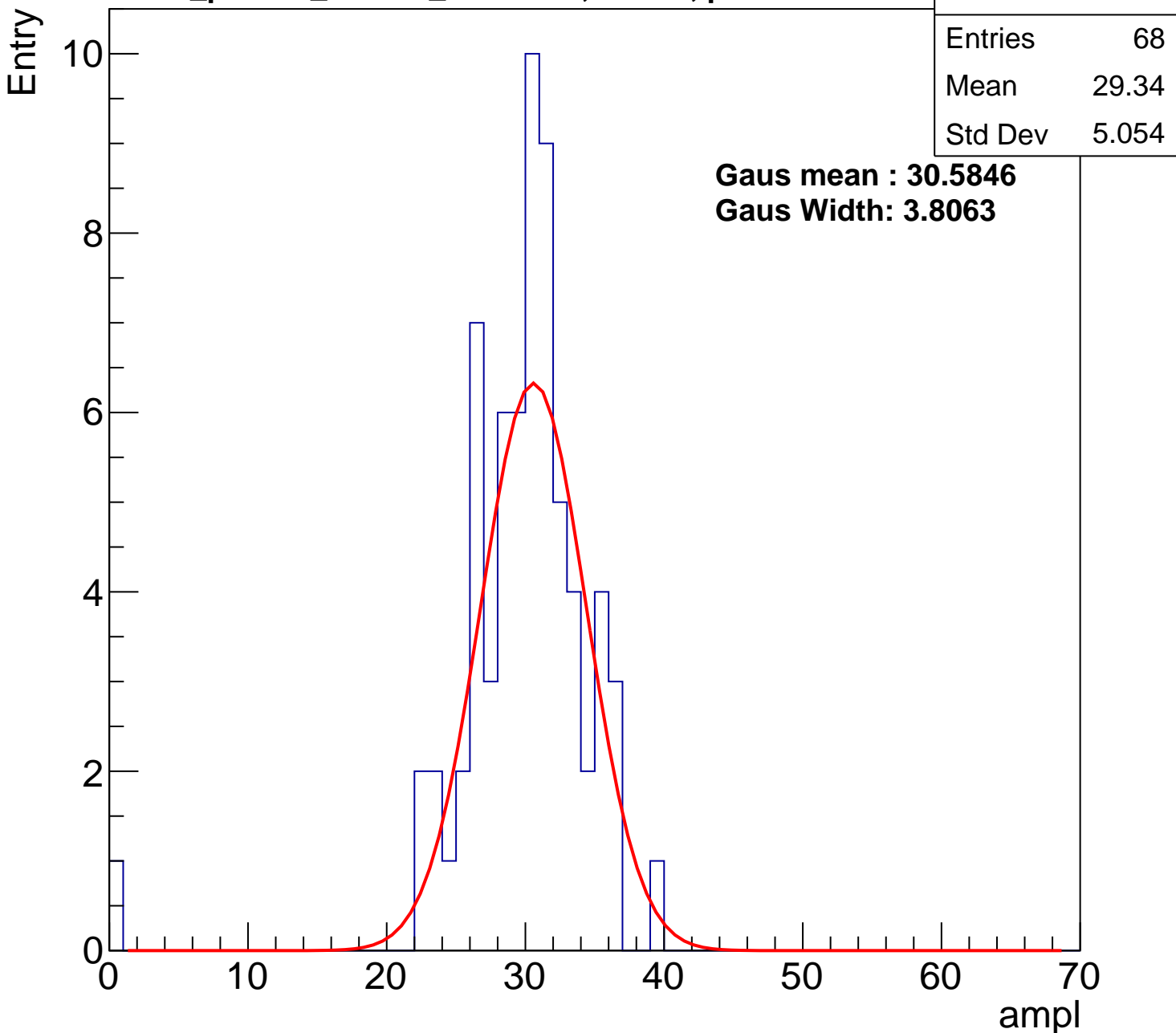
**Gaus Width: 3.8063**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U16-ch121, adc1

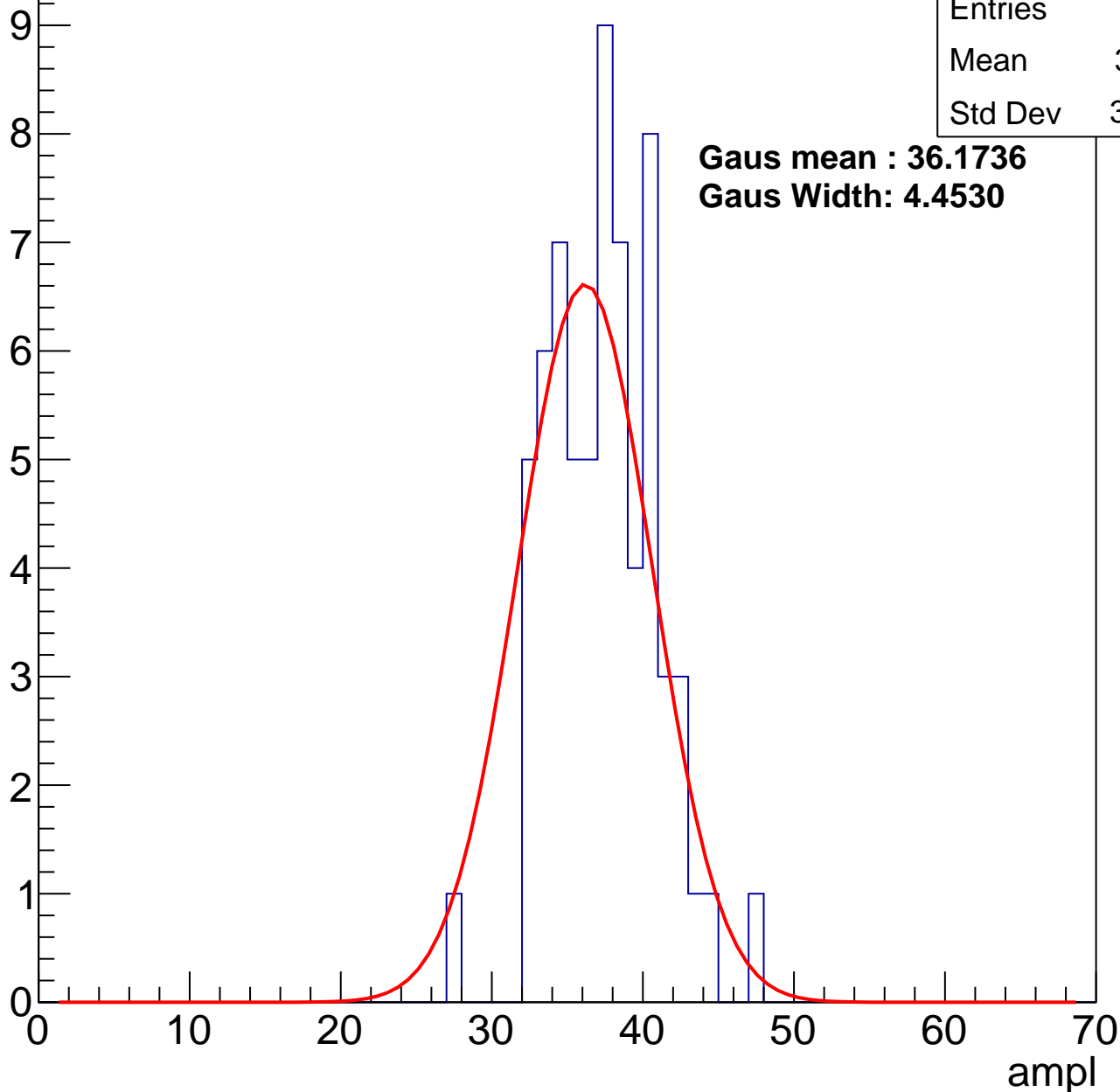
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	36.91
Std Dev	3.506

**Gaus mean : 36.1736**

**Gaus Width: 4.4530**



# B1L102S, U16-ch121, adc2

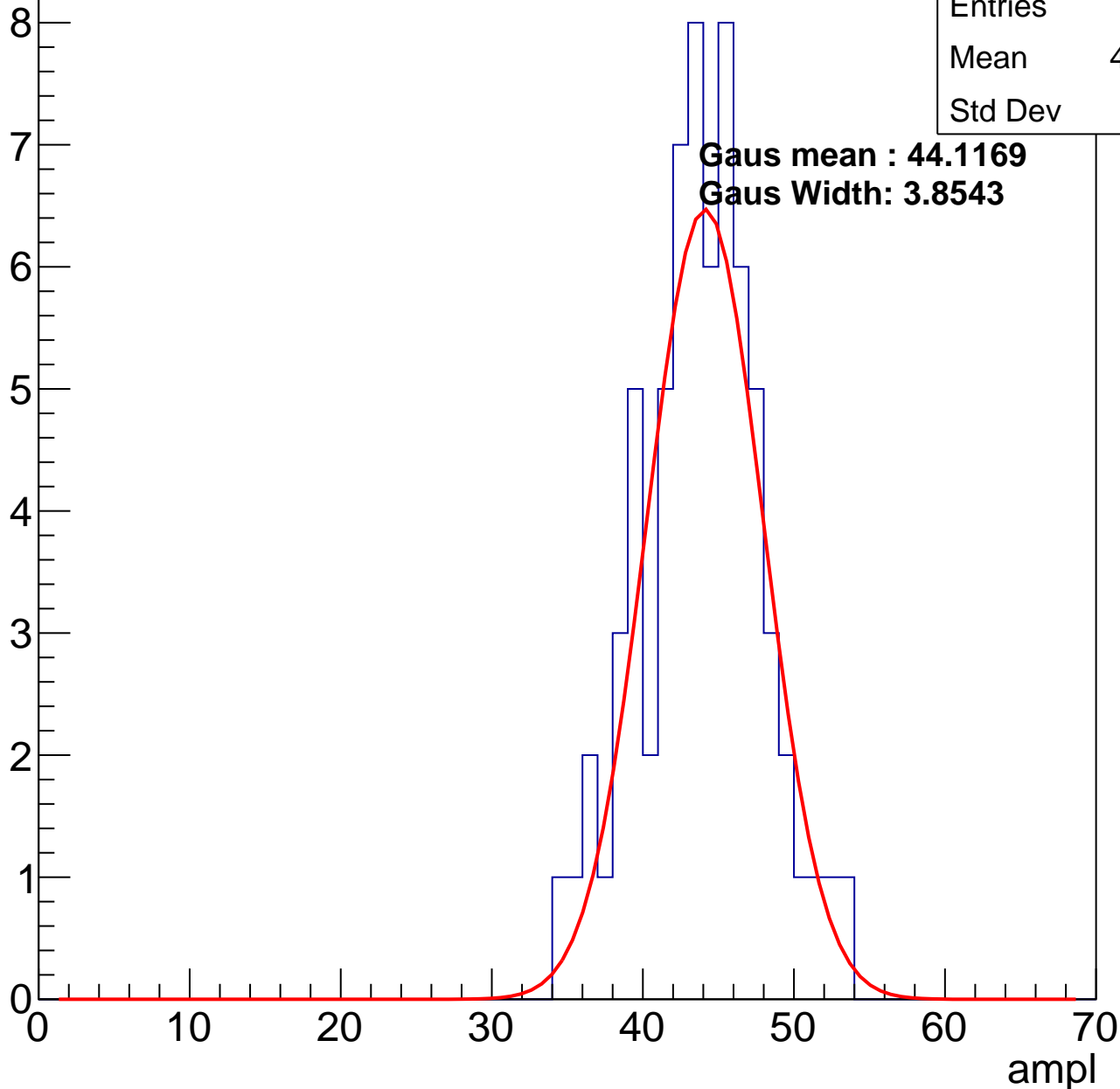
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	43.38
Std Dev	3.96

**Gaus mean : 44.1169**

**Gaus Width: 3.8543**

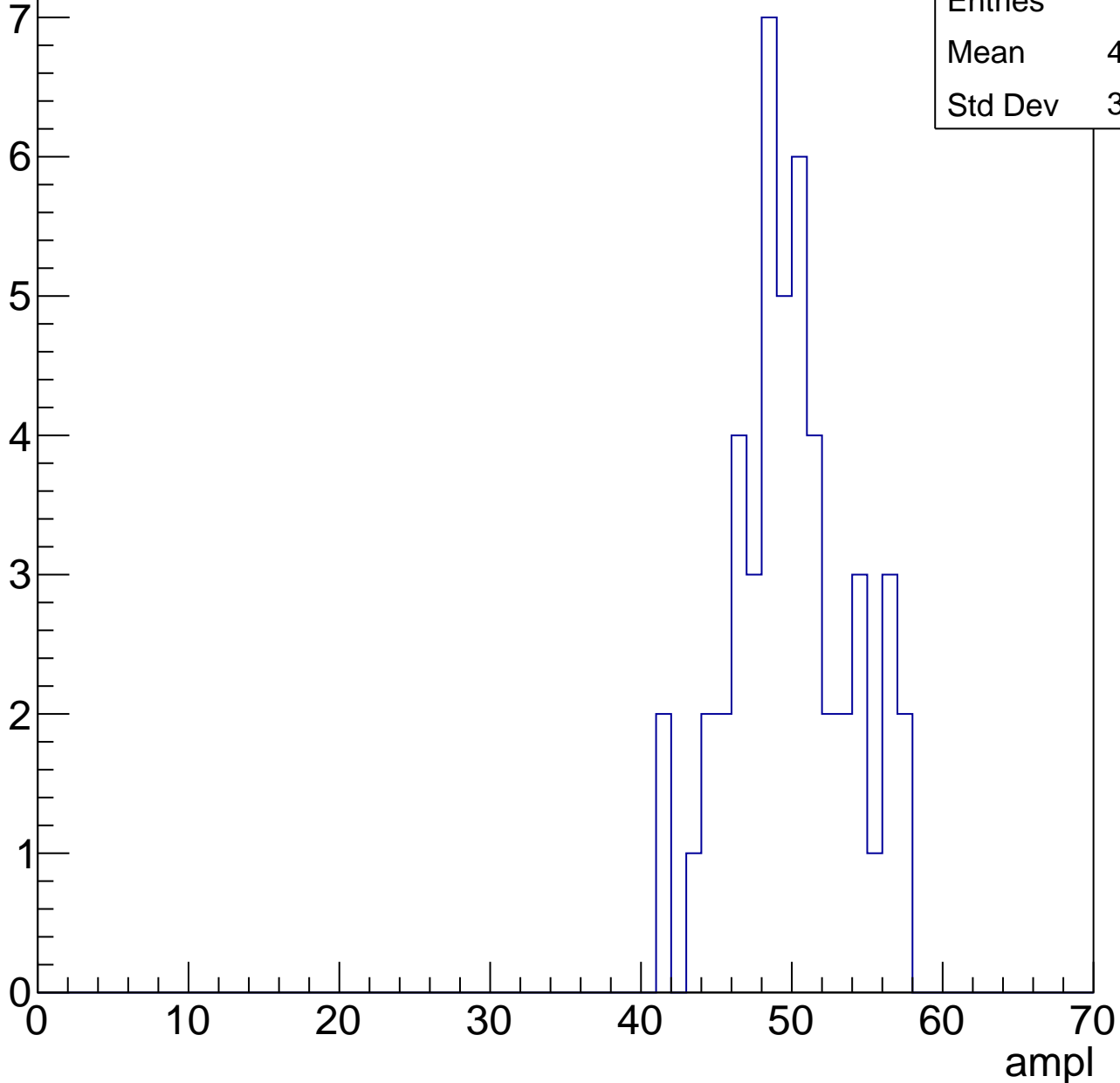


# B1L102S, U16-ch121, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

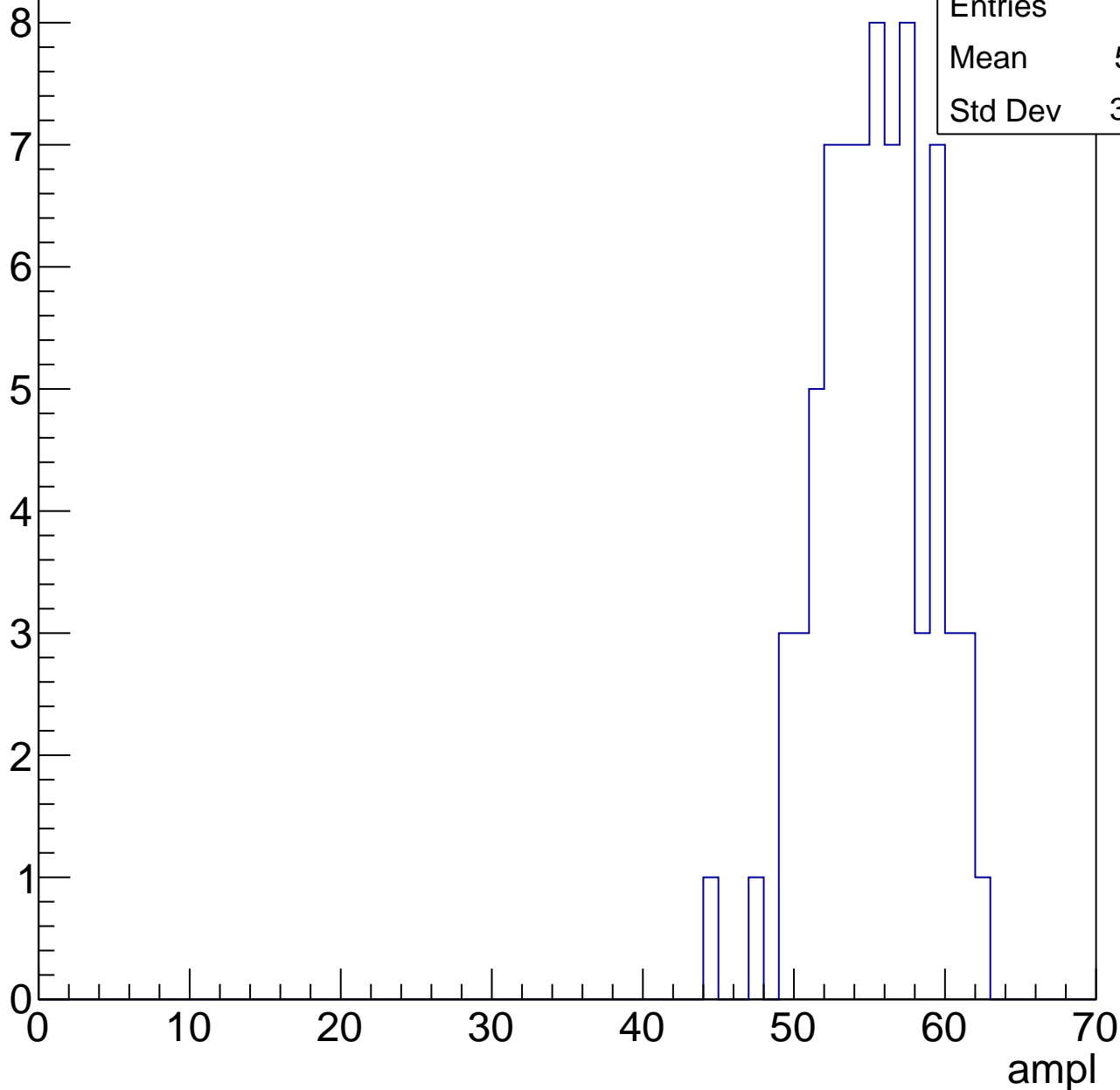
Entries	49
Mean	49.43
Std Dev	3.912



# B1L102S, U16-ch121, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

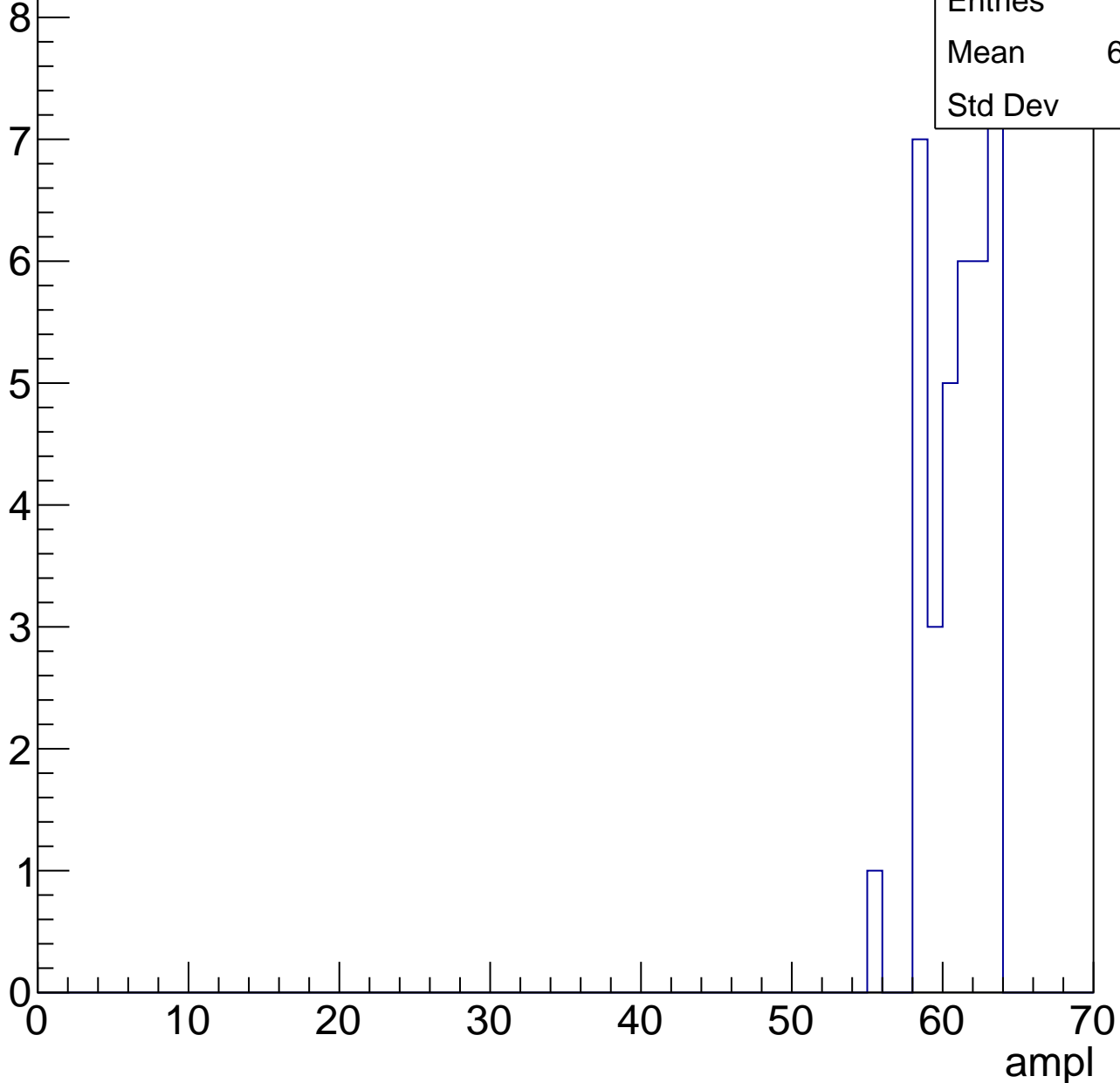


# B1L102S, U16-ch121, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

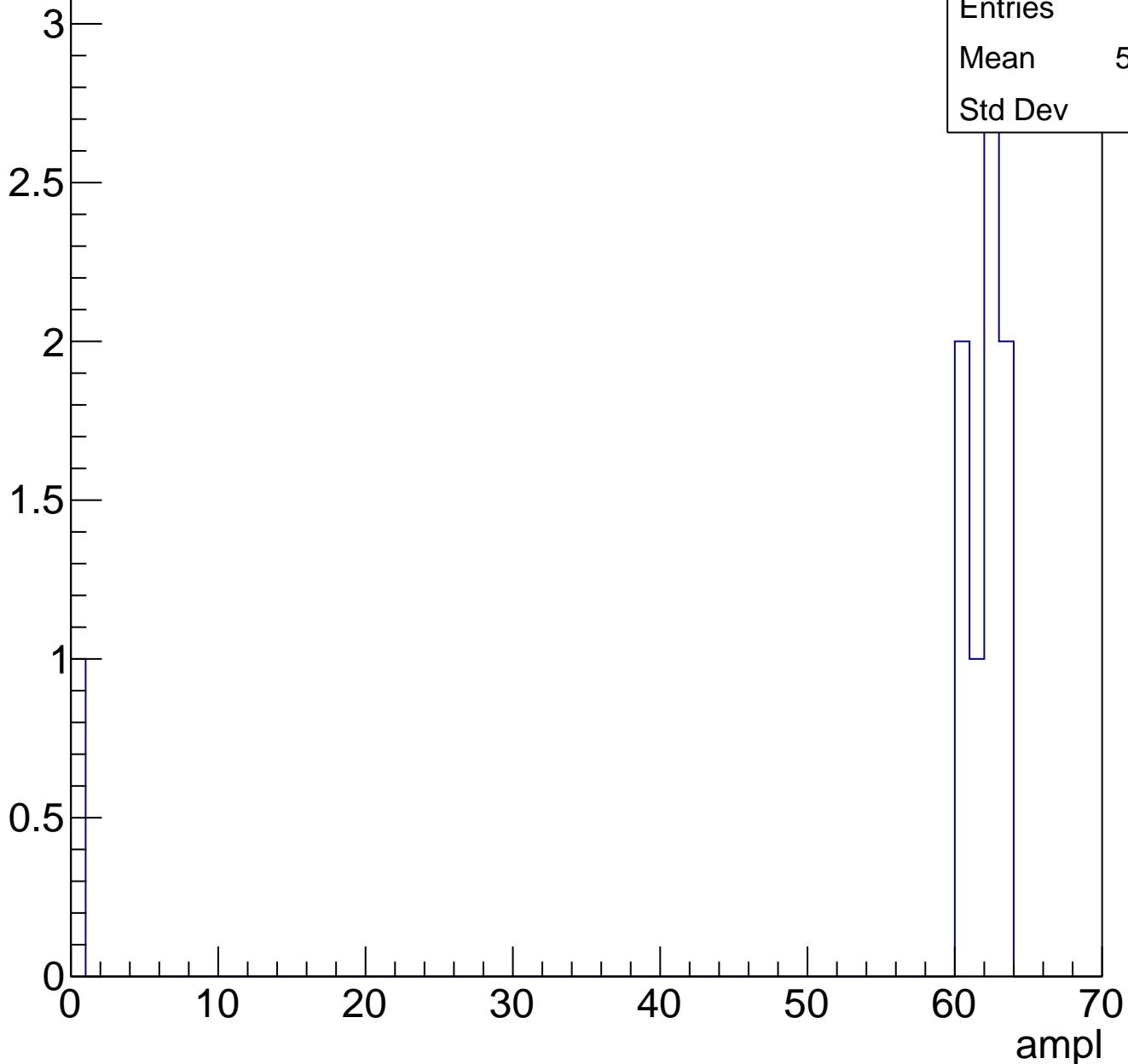
Entries	36
Mean	60.56
Std Dev	2.02



# B1L102S, U16-ch121, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch121, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch122, adc0

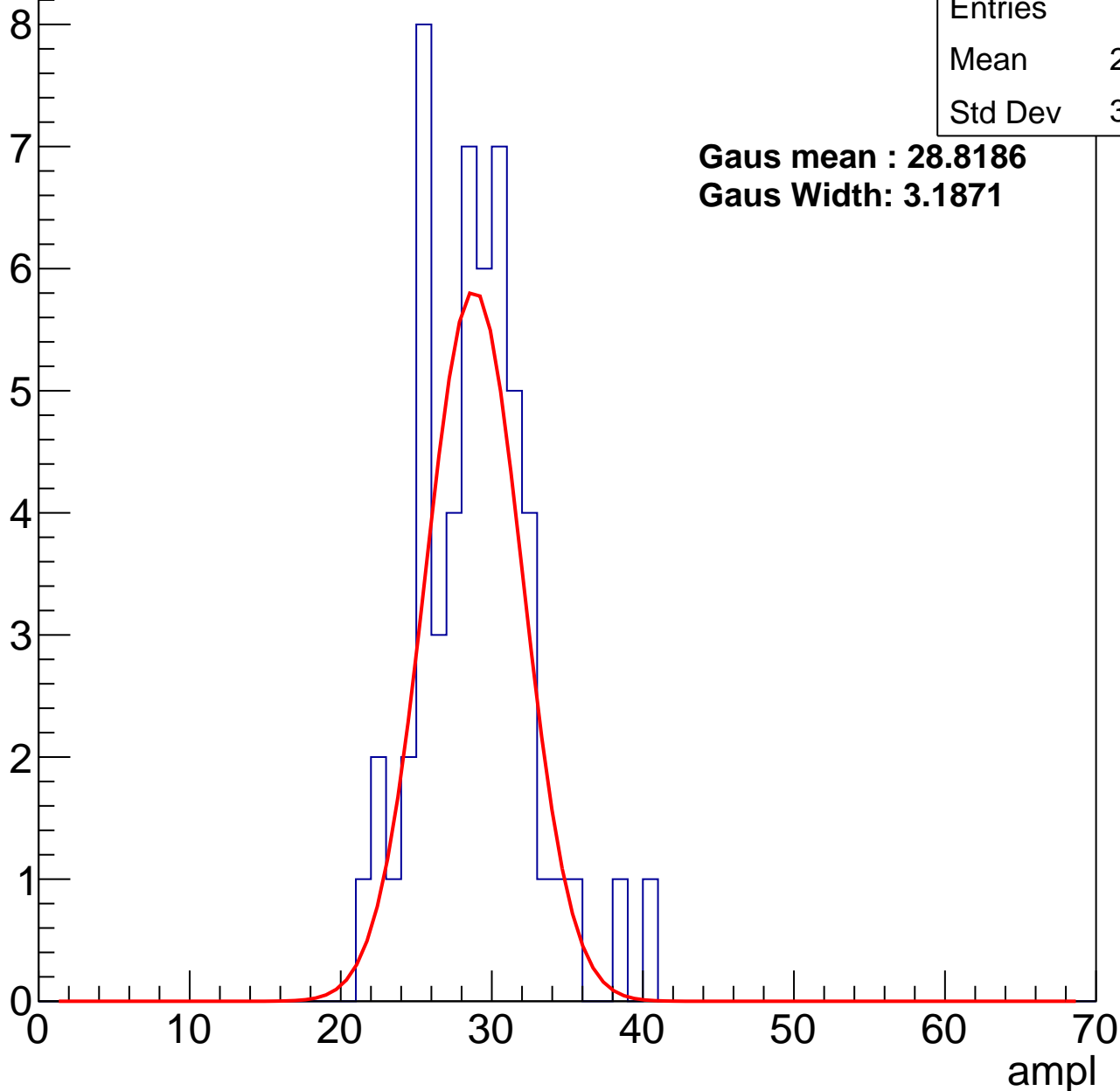
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	55
Mean	28.45
Std Dev	3.697

**Gaus mean : 28.8186**

**Gaus Width: 3.1871**



# B1L102S, U16-ch122, adc1

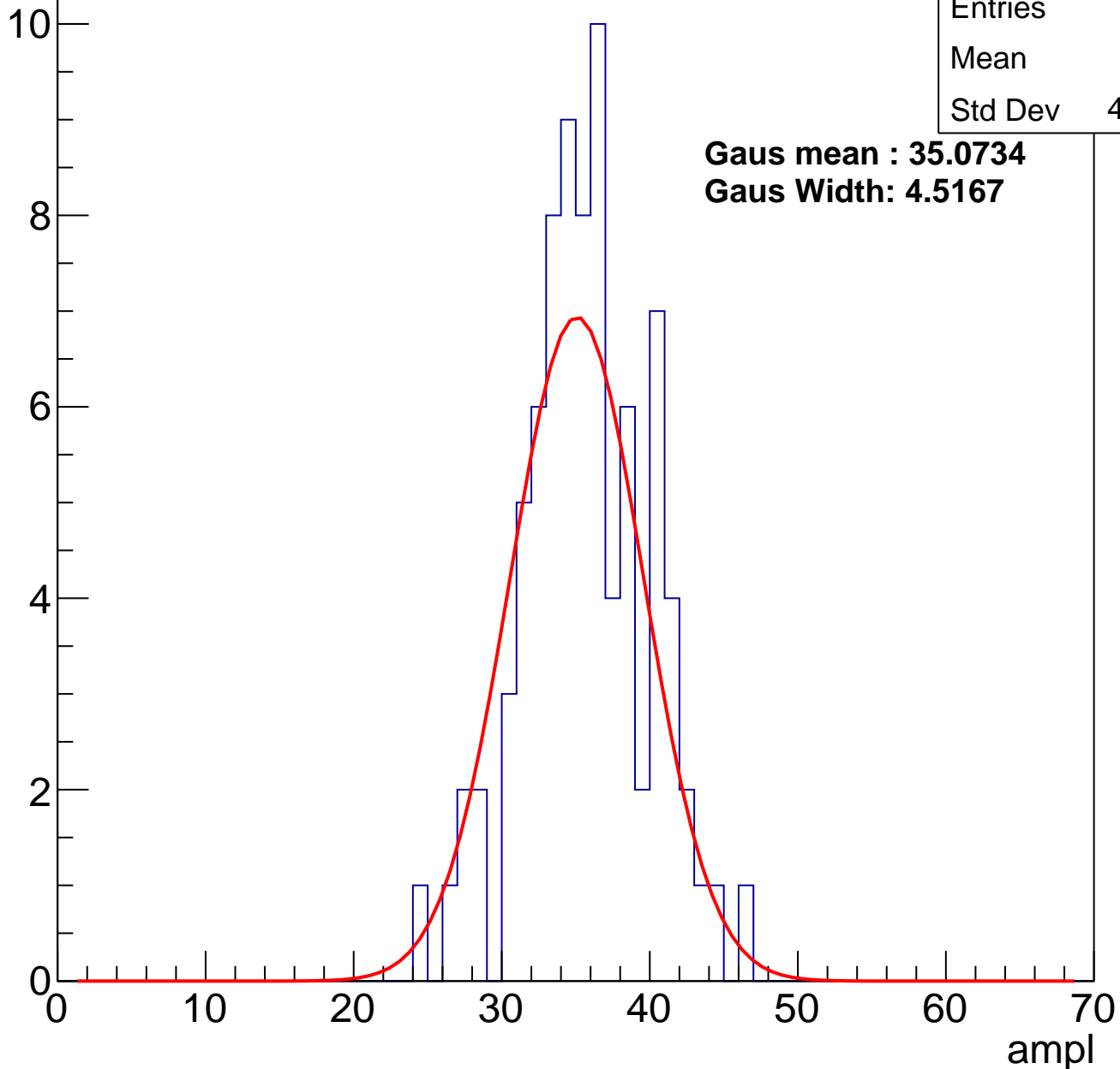
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	83
Mean	35.2
Std Dev	4.208

**Gaus mean : 35.0734**

**Gaus Width: 4.5167**

Entry



# B1L102S, U16-ch122, adc2

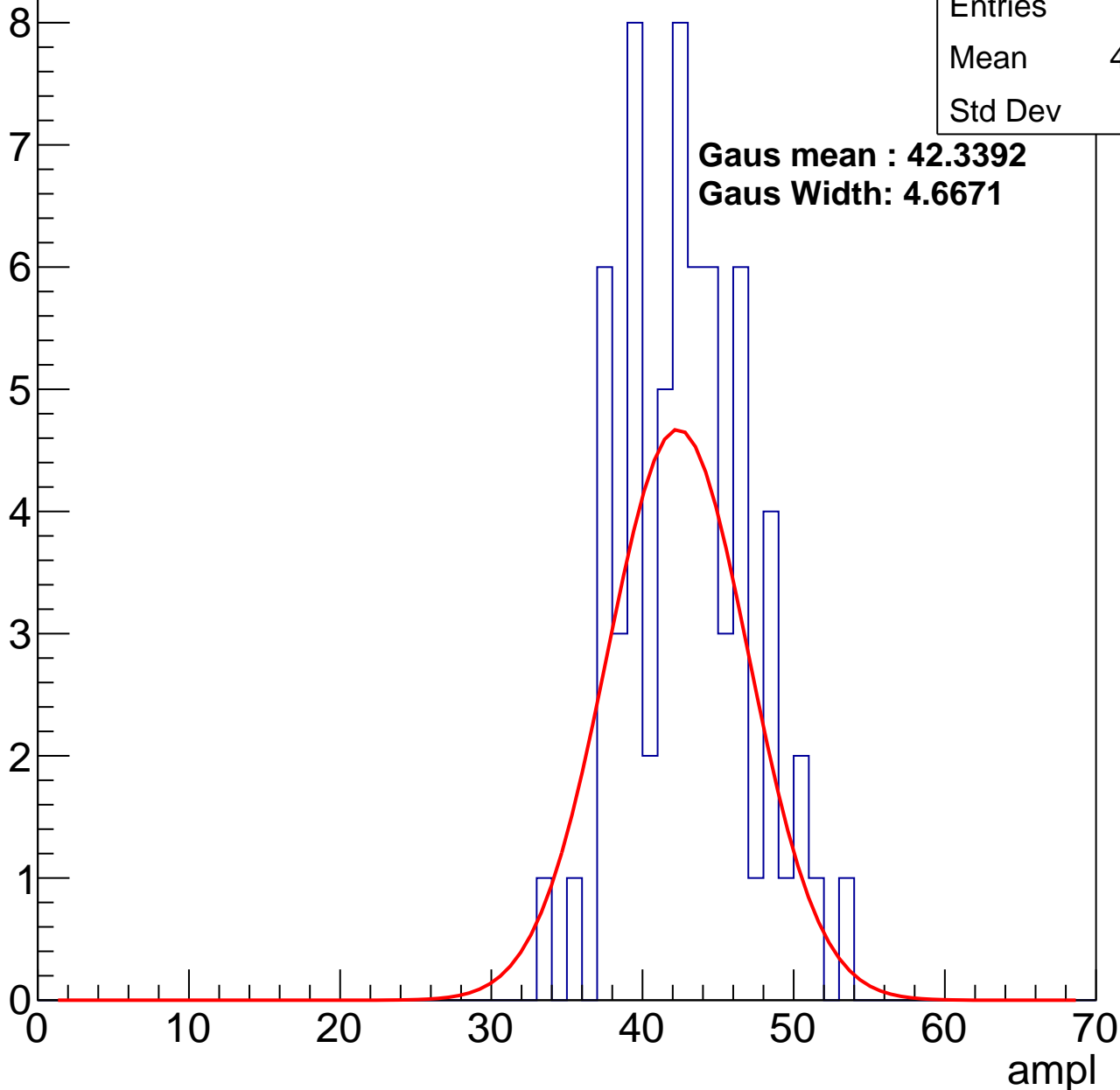
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	42.49
Std Dev	4.11

**Gaus mean : 42.3392**

**Gaus Width: 4.6671**

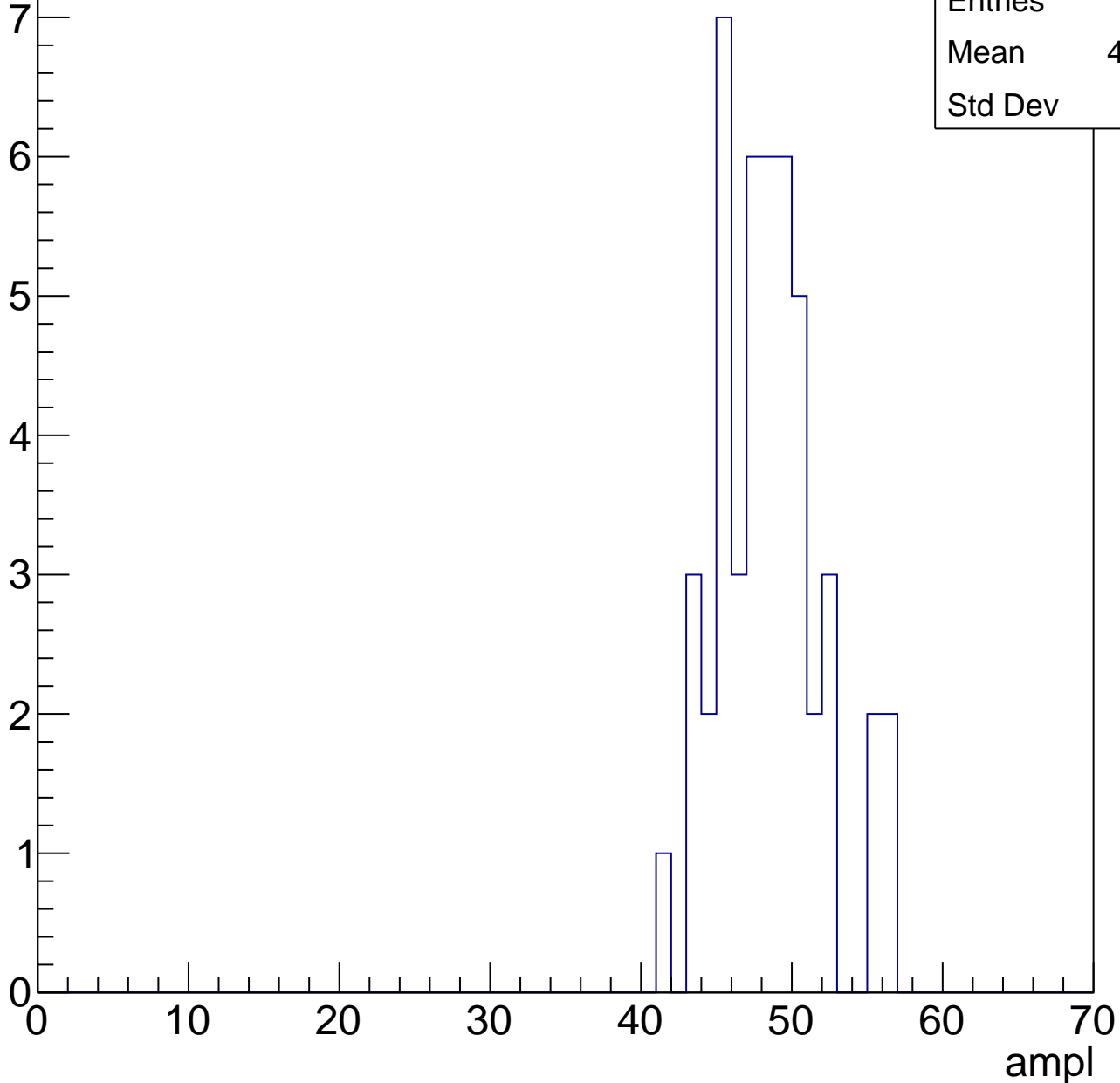


# B1L102S, U16-ch122, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	48.02
Std Dev	3.4

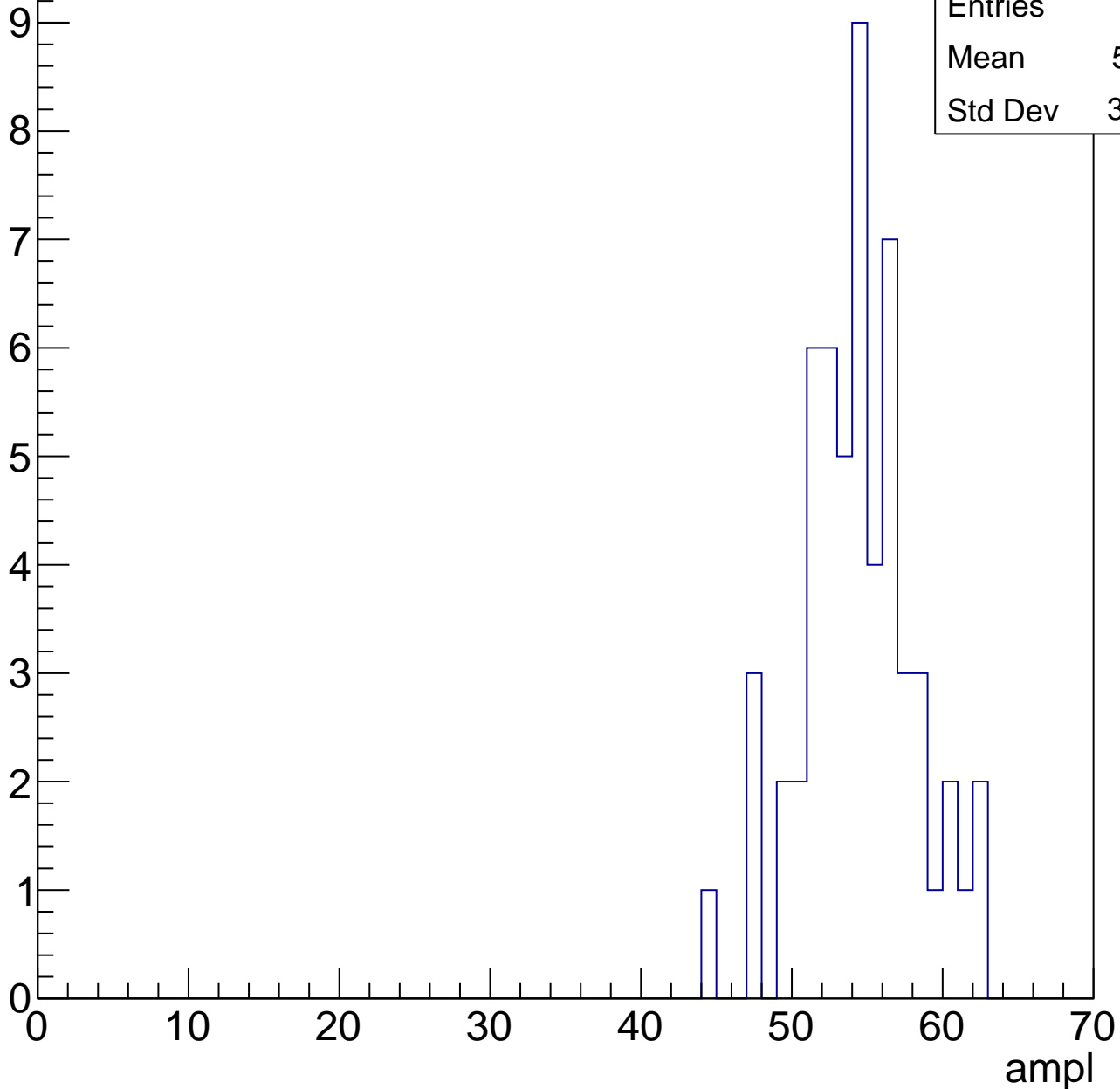


# B1L102S, U16-ch122, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	53.91
Std Dev	3.729

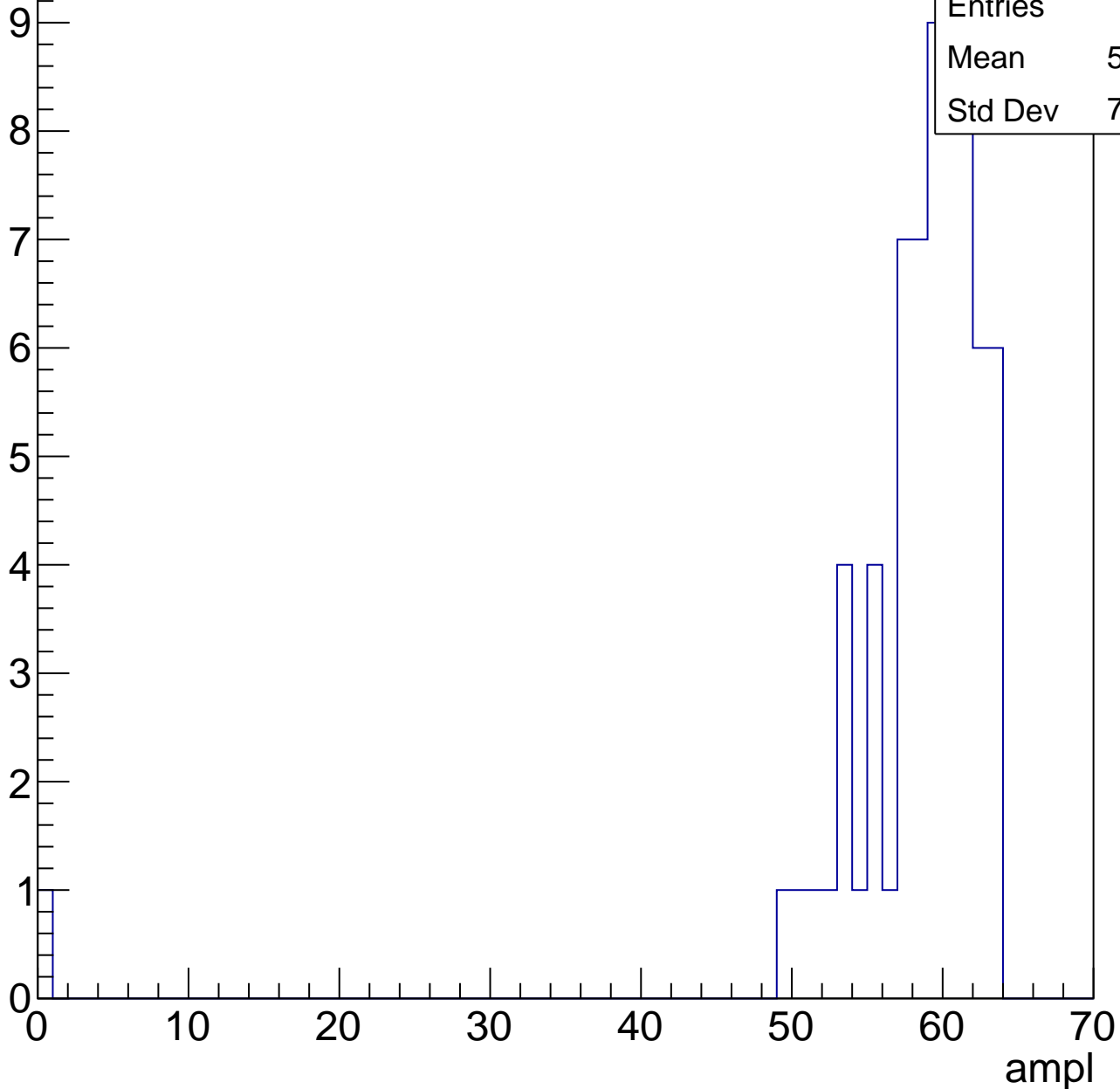


# B1L102S, U16-ch122, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	66
Mean	57.55
Std Dev	7.884



# B1L102S, U16-ch122, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

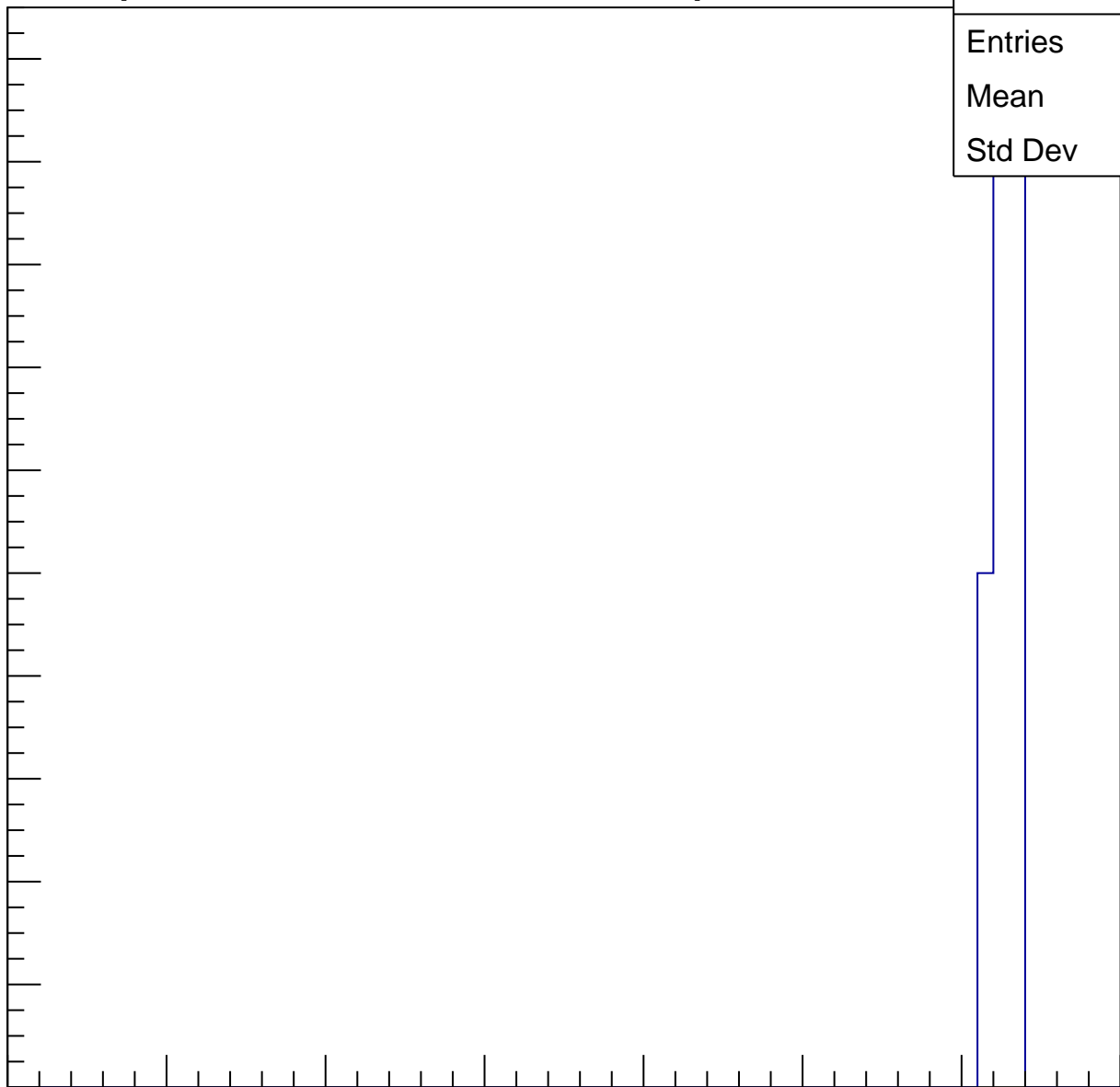
Entry

2  
1.8  
1.6  
1.4  
1.2  
1  
0.8  
0.6  
0.4  
0.2  
0

Entries	5
Mean	62.2
Std Dev	0.7483

0 10 20 30 40 50 60 70

ampl

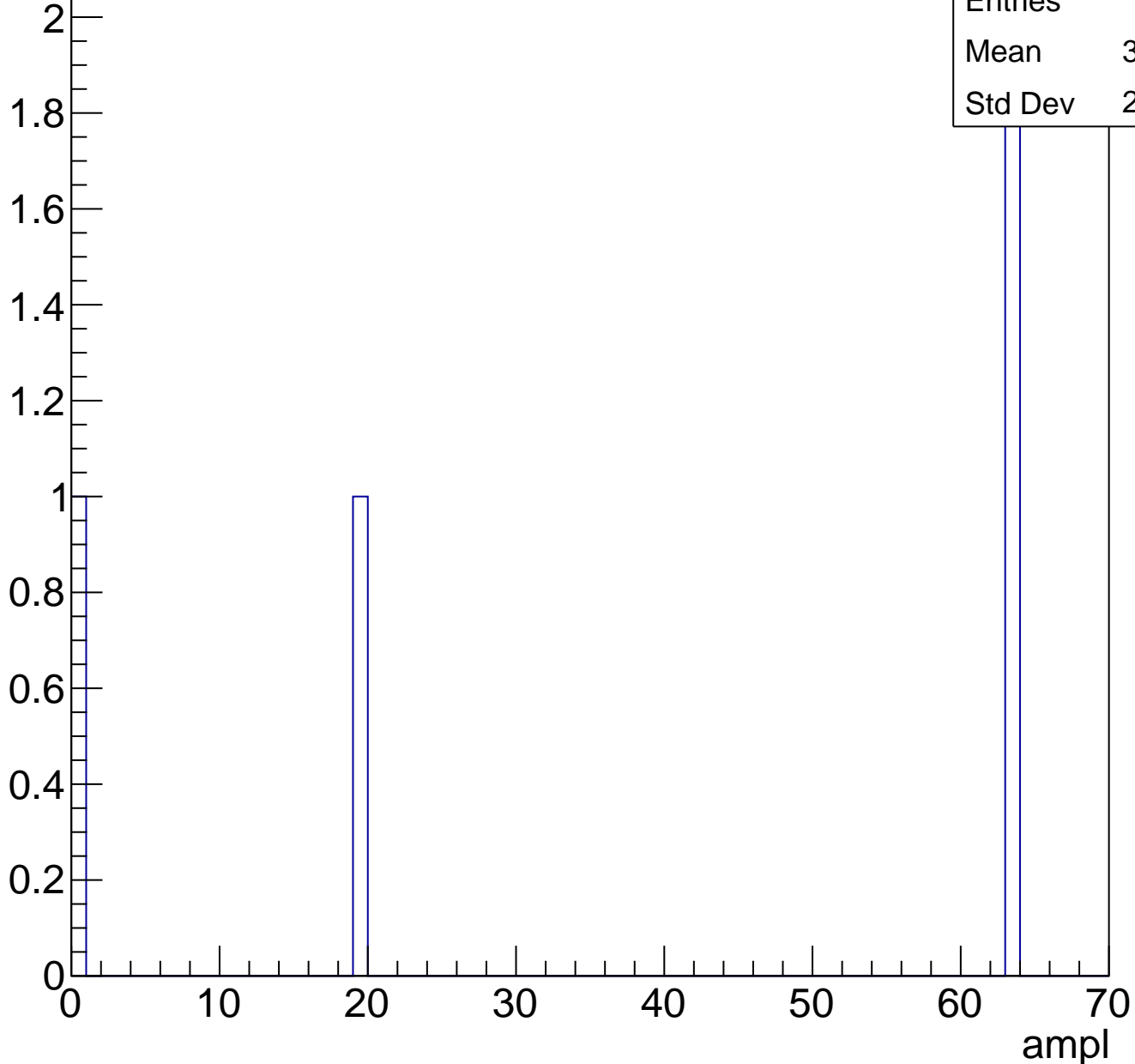




# B1L102S, U16-ch122, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch123, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	64
Mean	29.3
Std Dev	3.868

**Gaus mean : 30.6875**

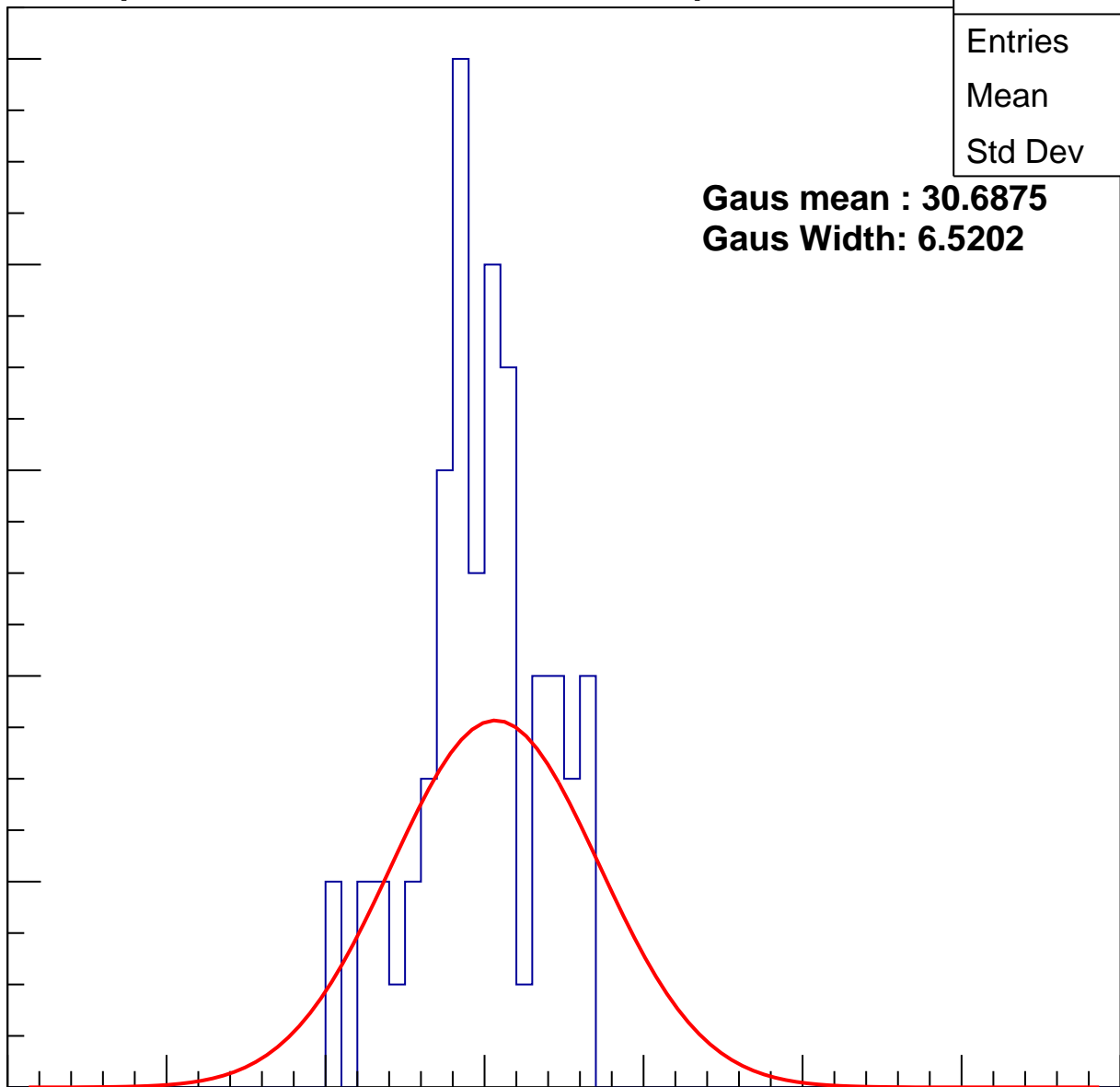
**Gaus Width: 6.5202**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U16-ch123, adc1

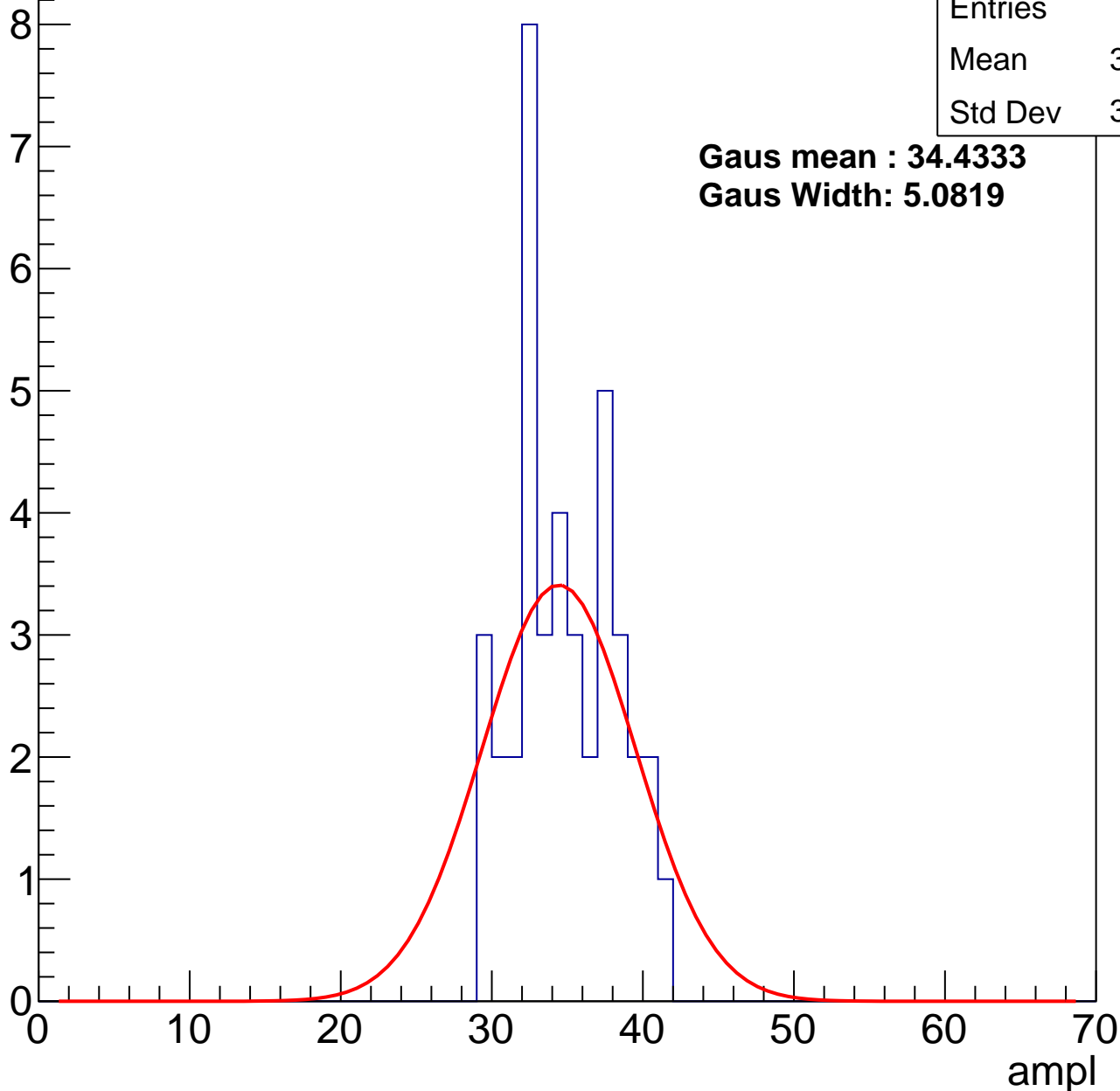
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	40
Mean	34.38
Std Dev	3.276

**Gaus mean : 34.4333**

**Gaus Width: 5.0819**



# B1L102S, U16-ch123, adc2

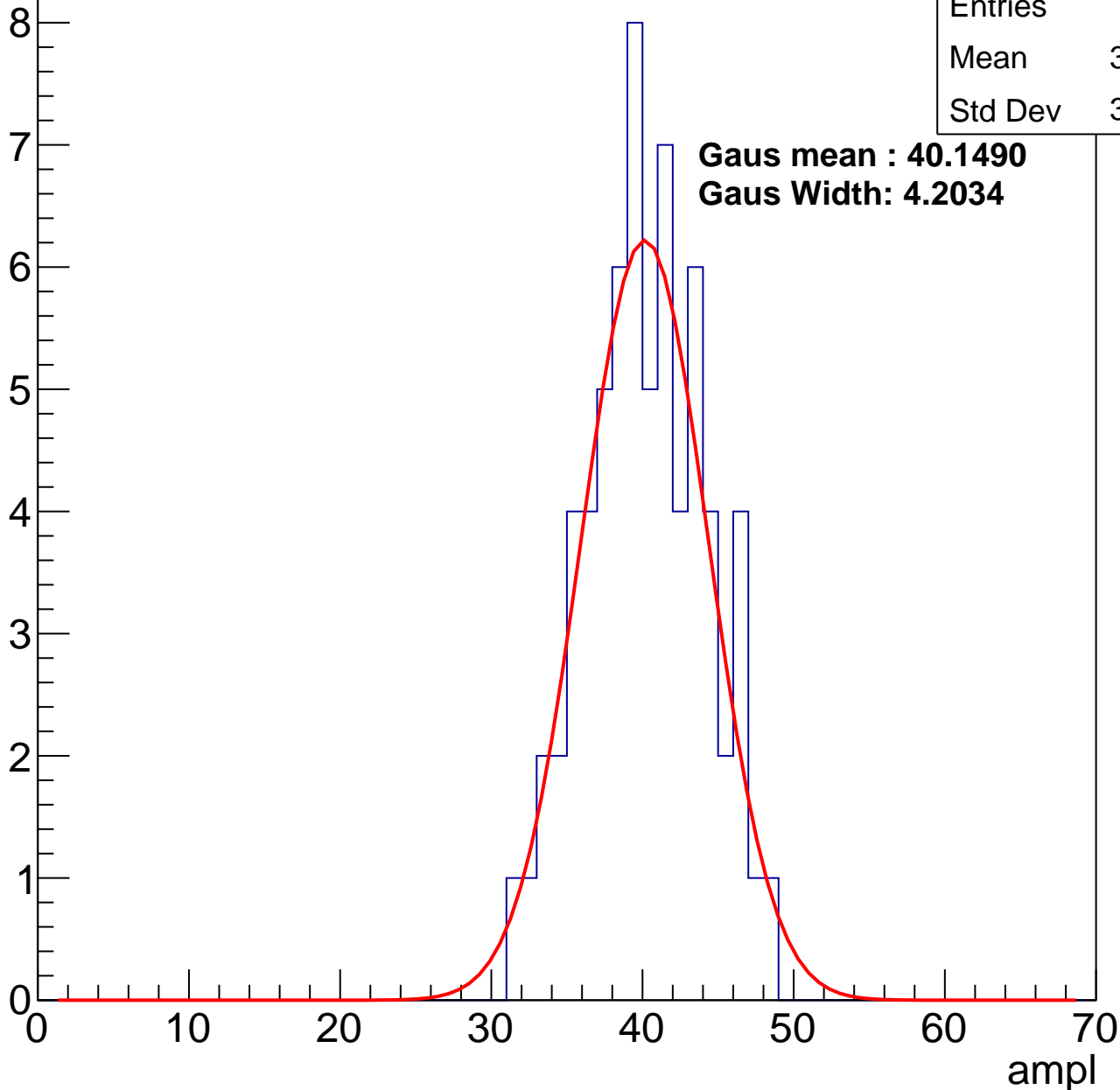
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	67
Mean	39.76
Std Dev	3.864

**Gaus mean : 40.1490**

**Gaus Width: 4.2034**

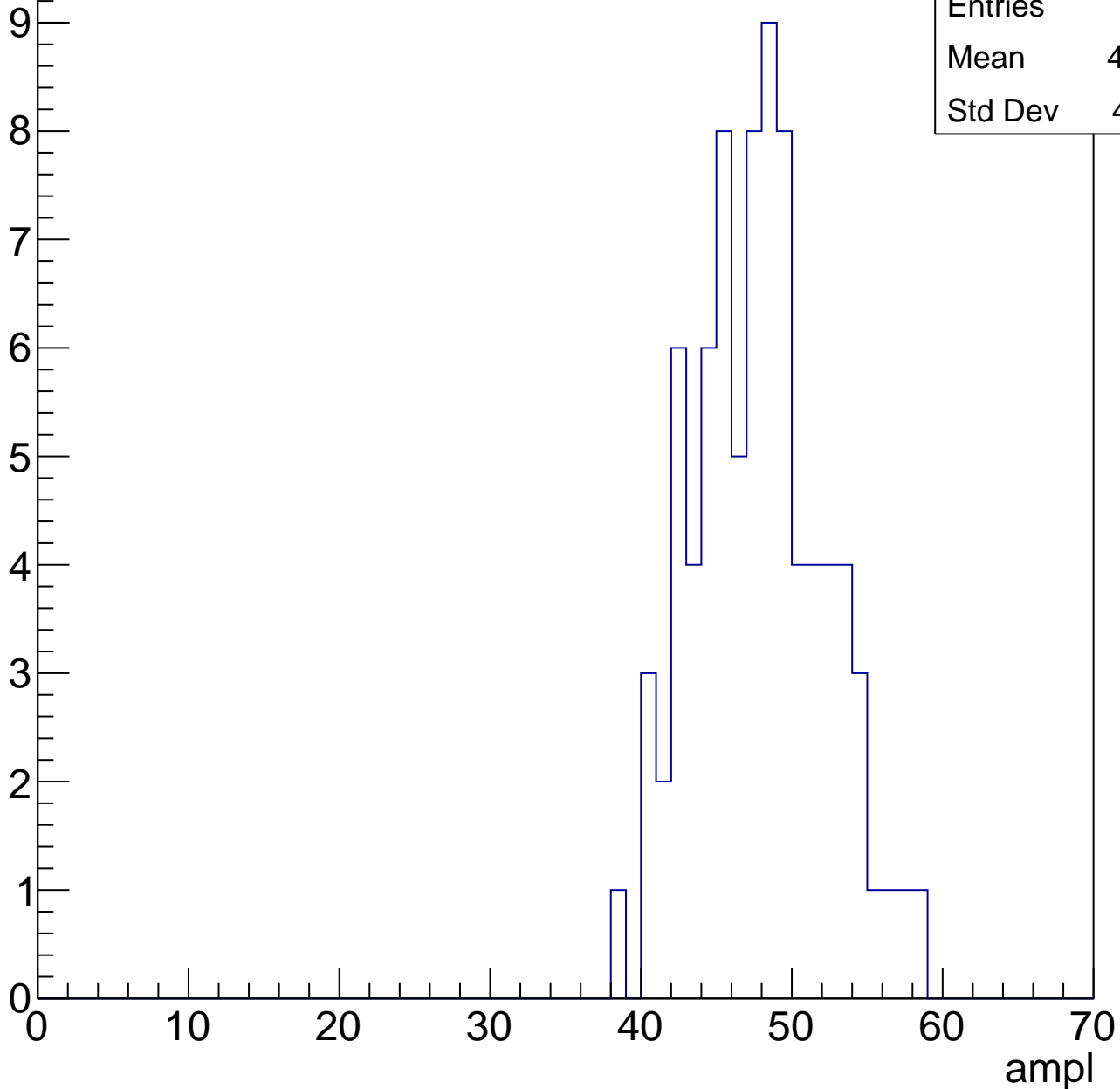


# B1L102S, U16-ch123, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	83
Mean	47.35
Std Dev	4.241

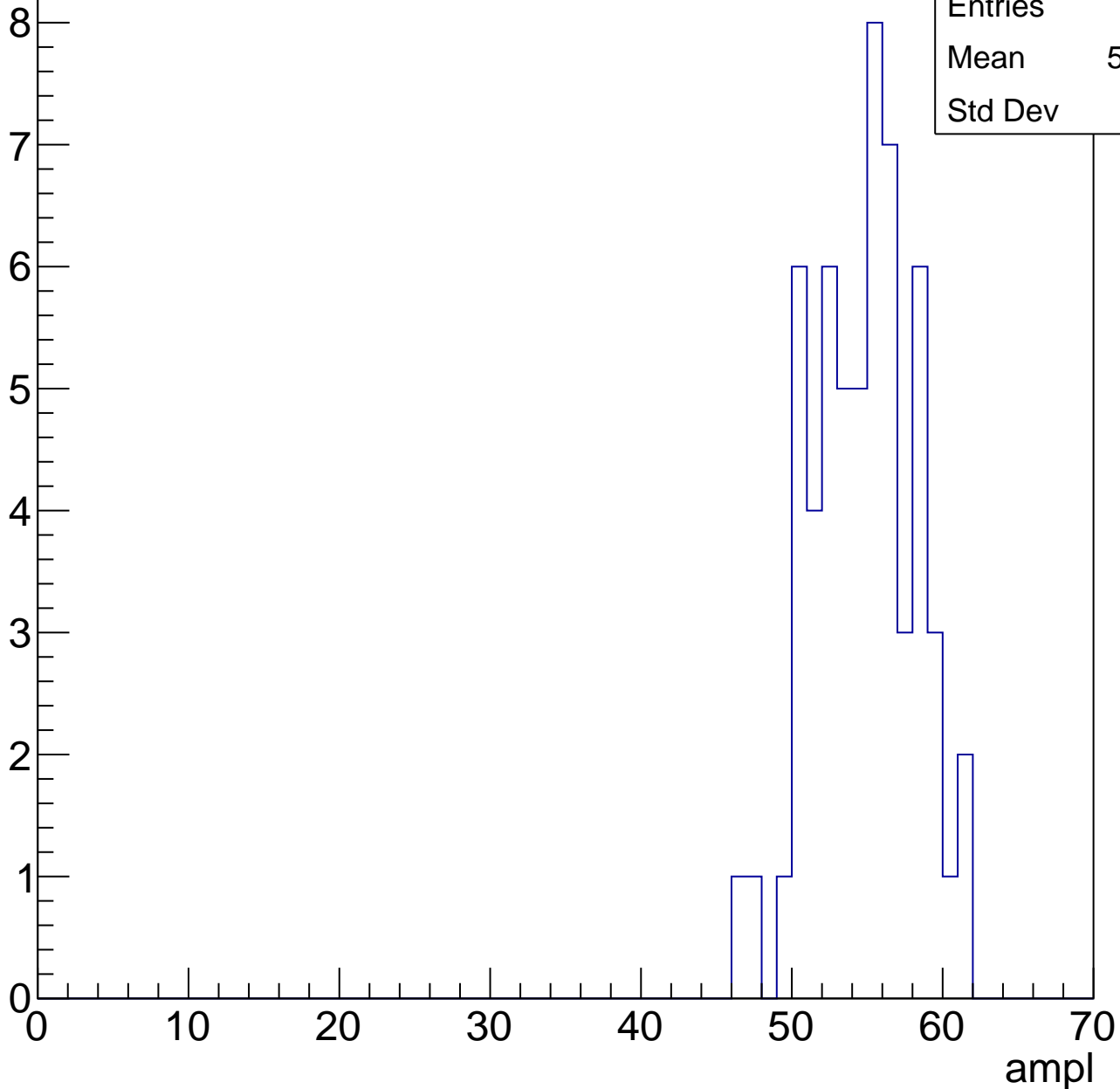


# B1L102S, U16-ch123, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	59
Mean	54.29
Std Dev	3.35

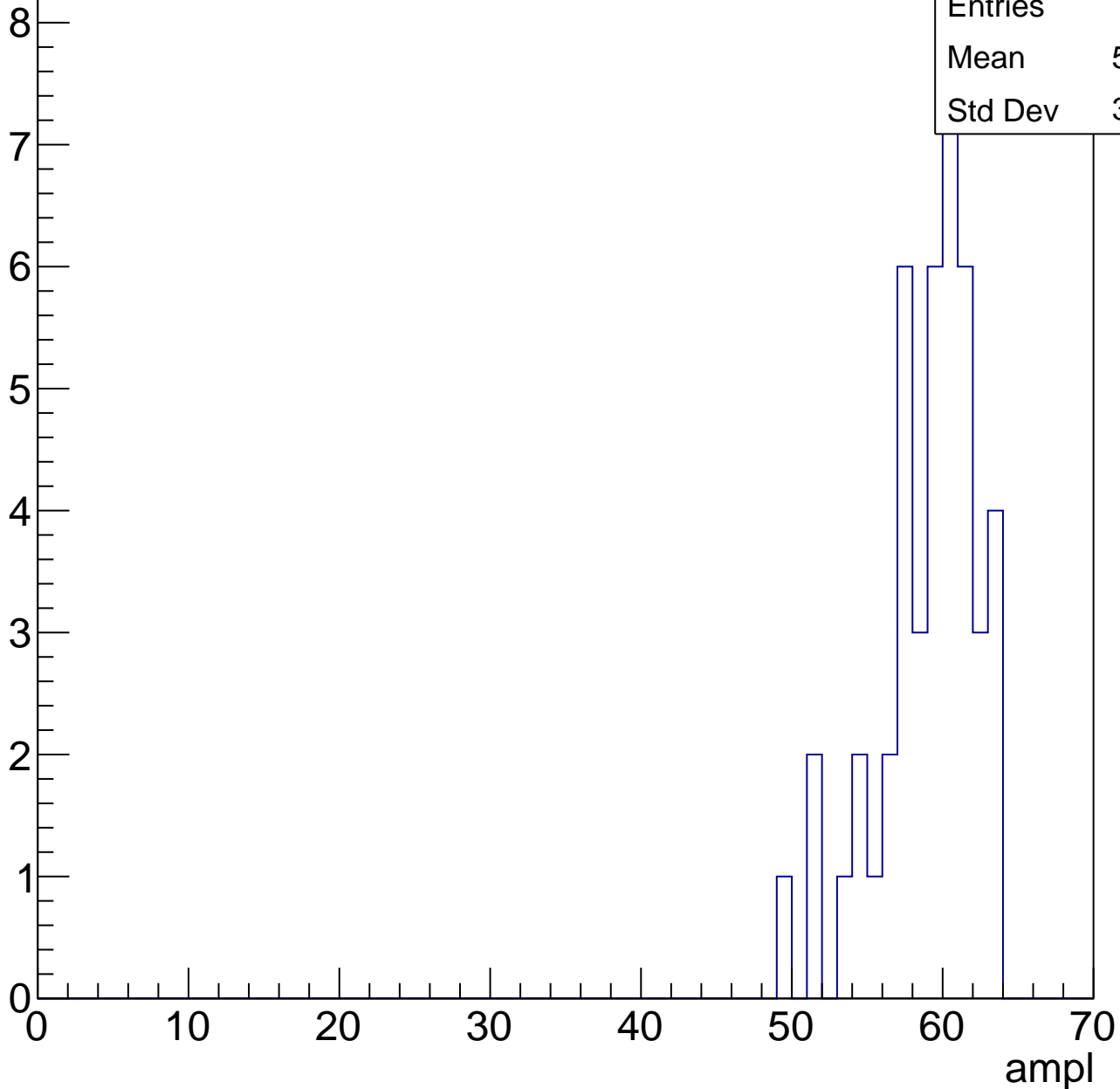


# B1L102S, U16-ch123, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	45
Mean	58.51
Std Dev	3.291

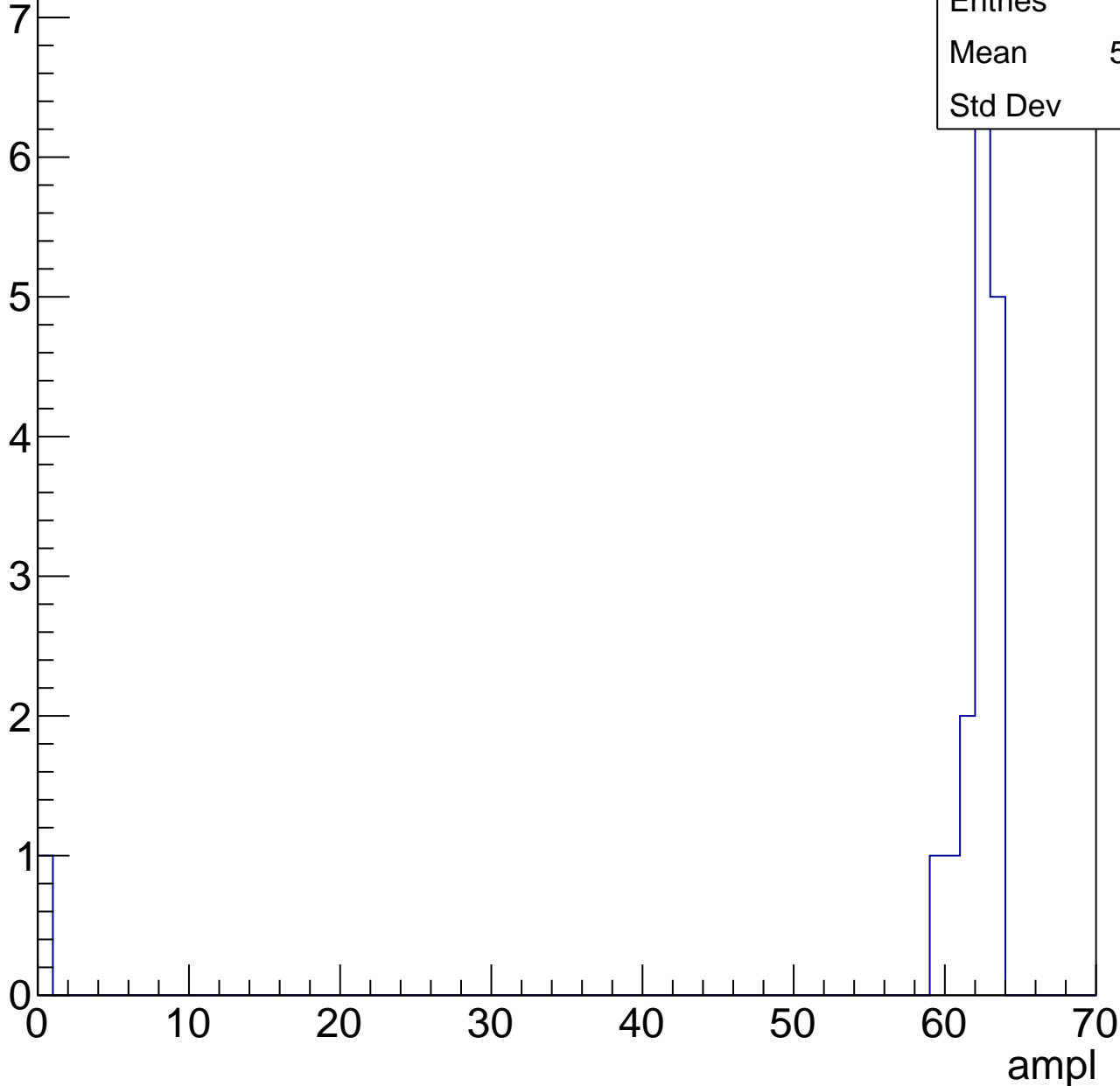


# B1L102S, U16-ch123, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	17
Mean	58.24
Std Dev	14.6

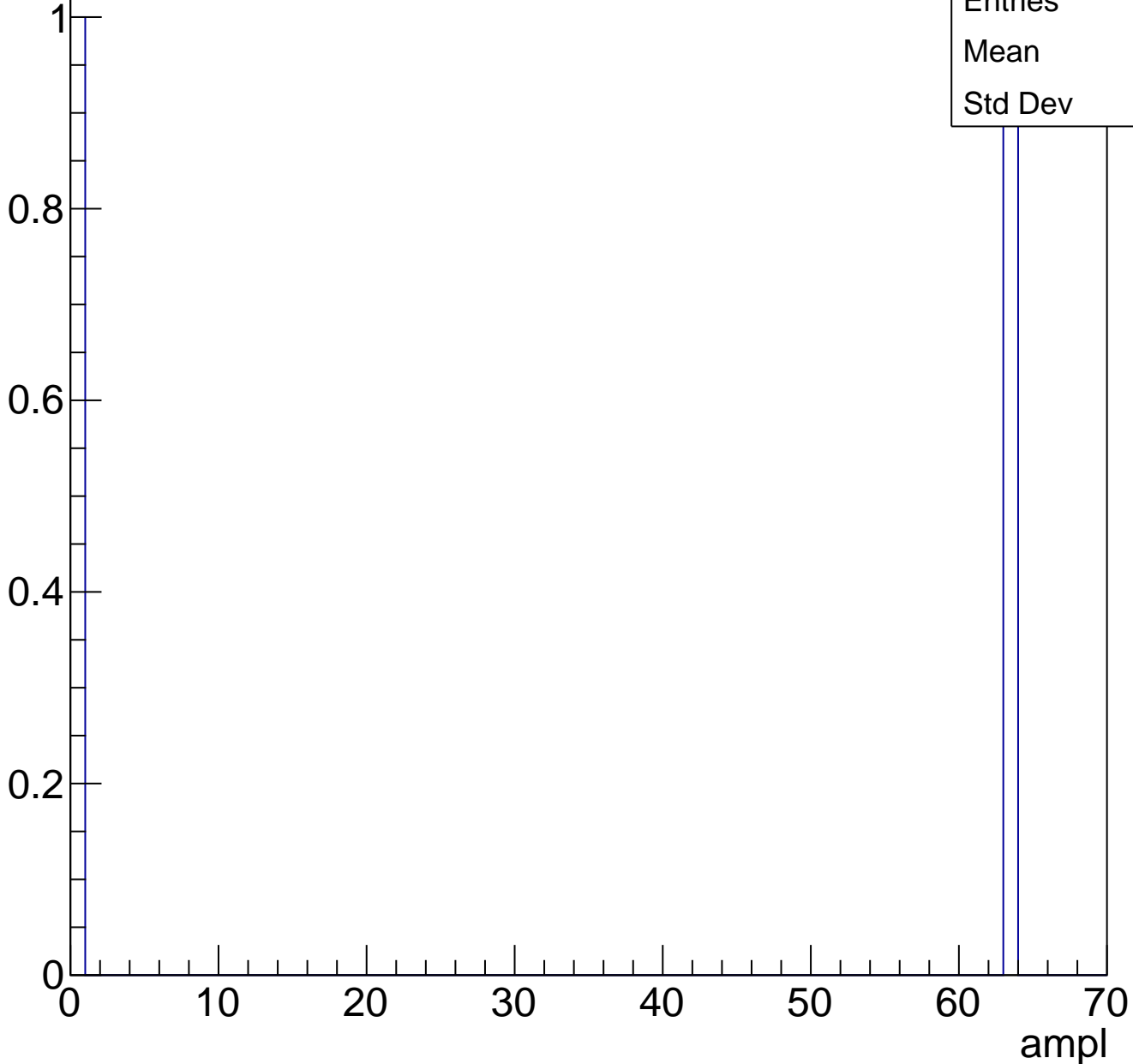




# B1L102S, U16-ch123, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch124, adc0

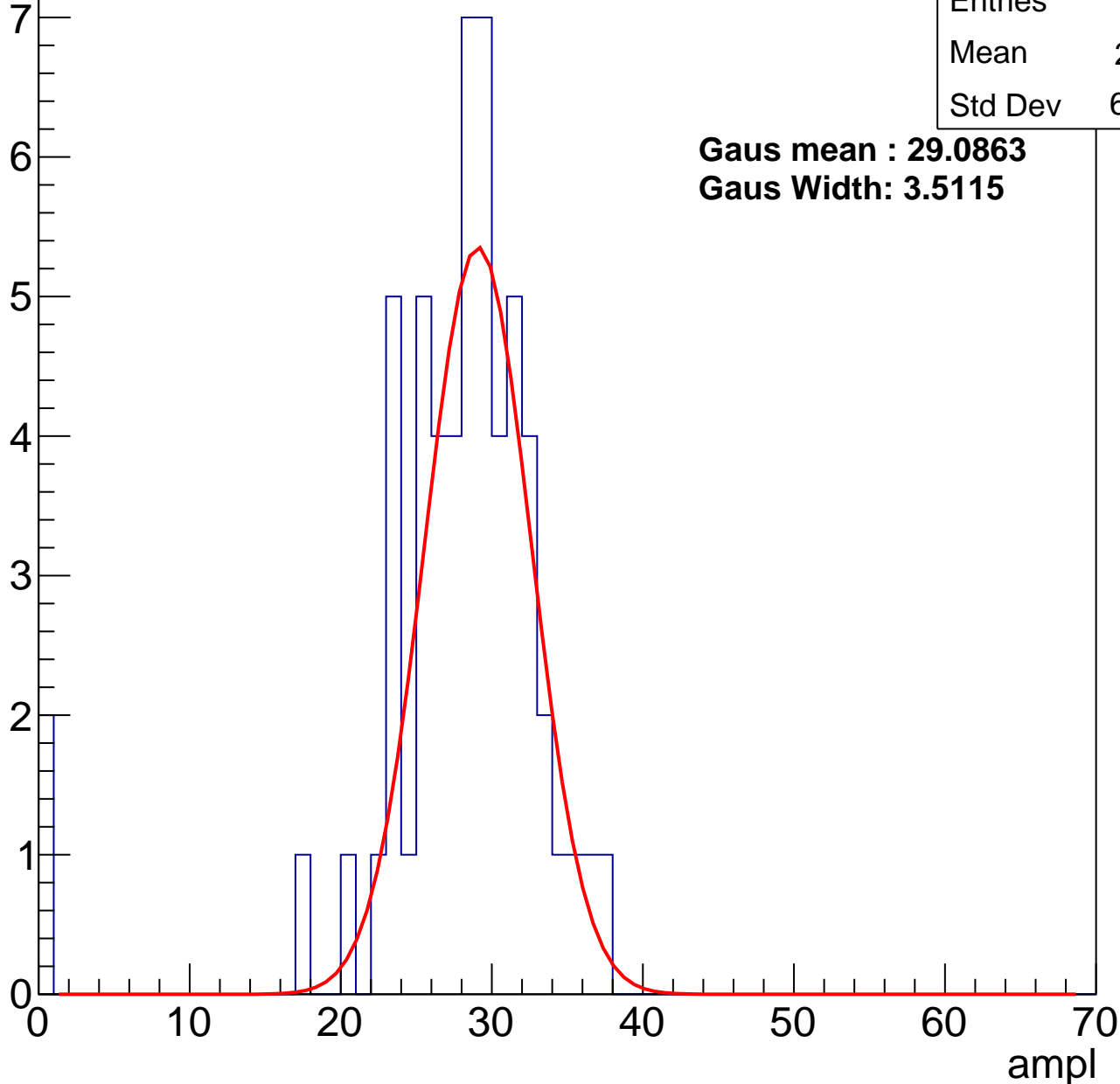
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	27.11
Std Dev	6.436

**Gaus mean : 29.0863**

**Gaus Width: 3.5115**



# B1L102S, U16-ch124, adc1

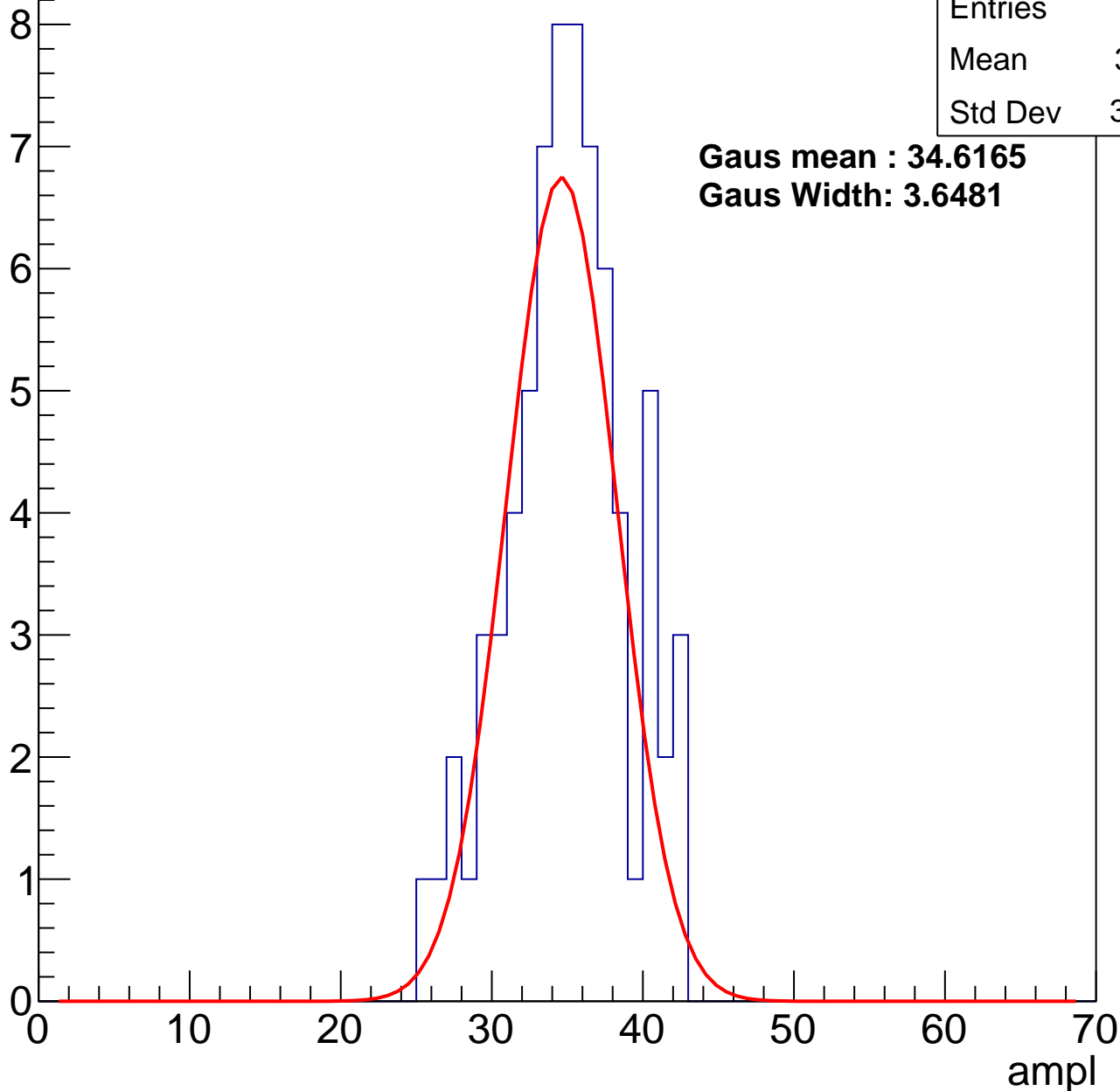
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	71
Mean	34.51
Std Dev	3.928

**Gaus mean : 34.6165**

**Gaus Width: 3.6481**



# B1L102S, U16-ch124, adc2

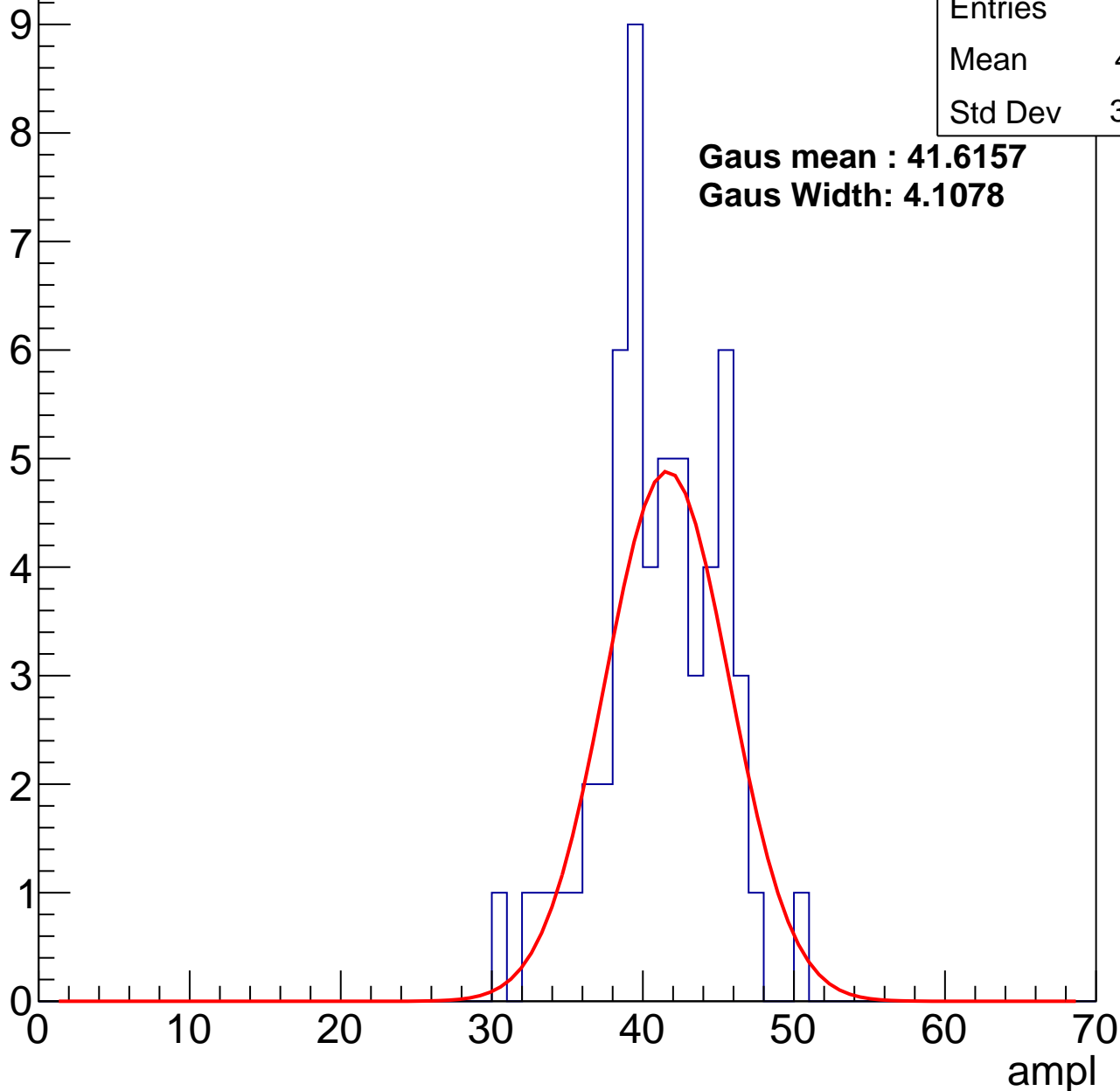
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	56
Mean	40.61
Std Dev	3.917

**Gaus mean : 41.6157**

**Gaus Width: 4.1078**

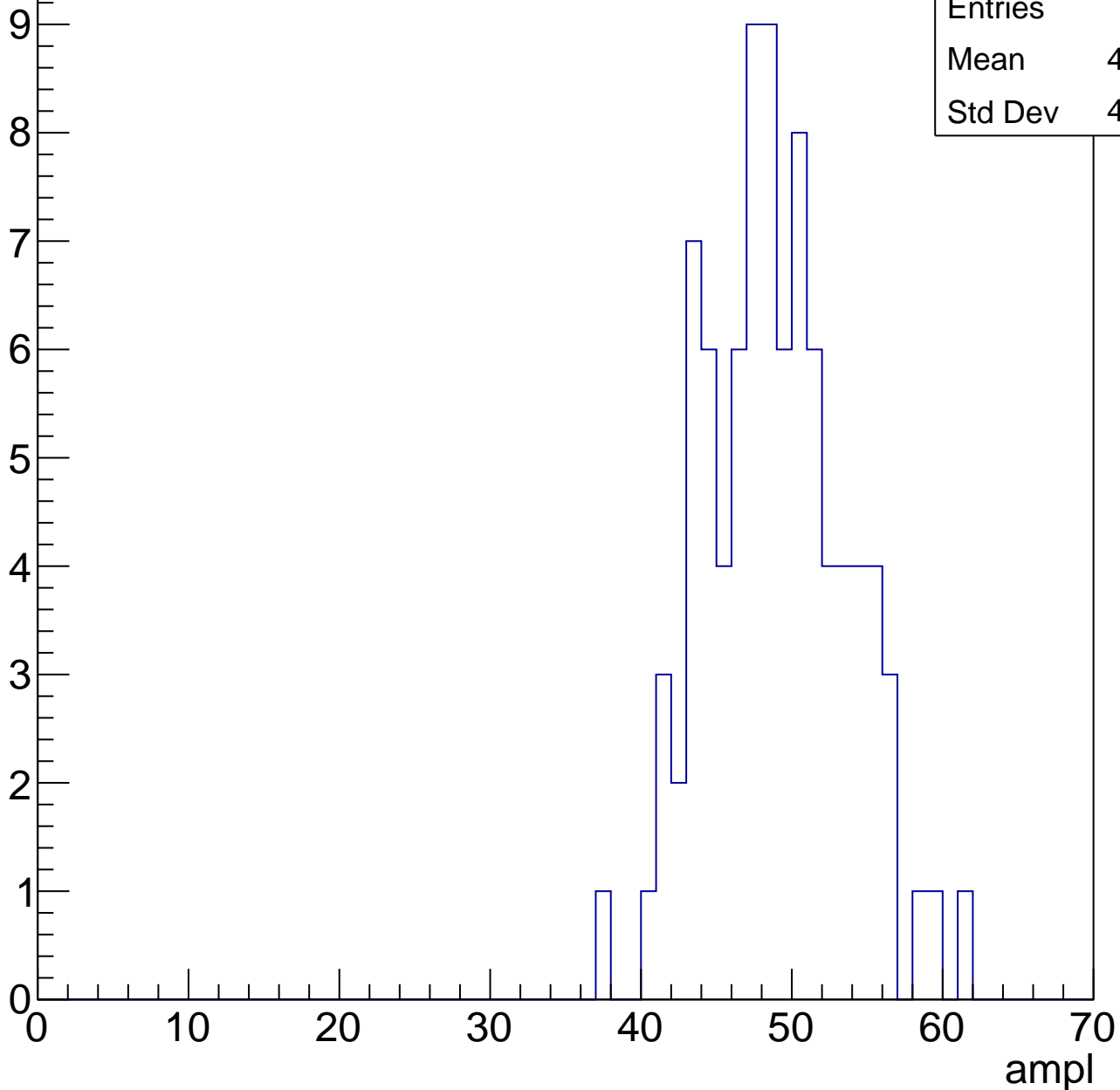


# B1L102S, U16-ch124, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	90
Mean	48.47
Std Dev	4.598

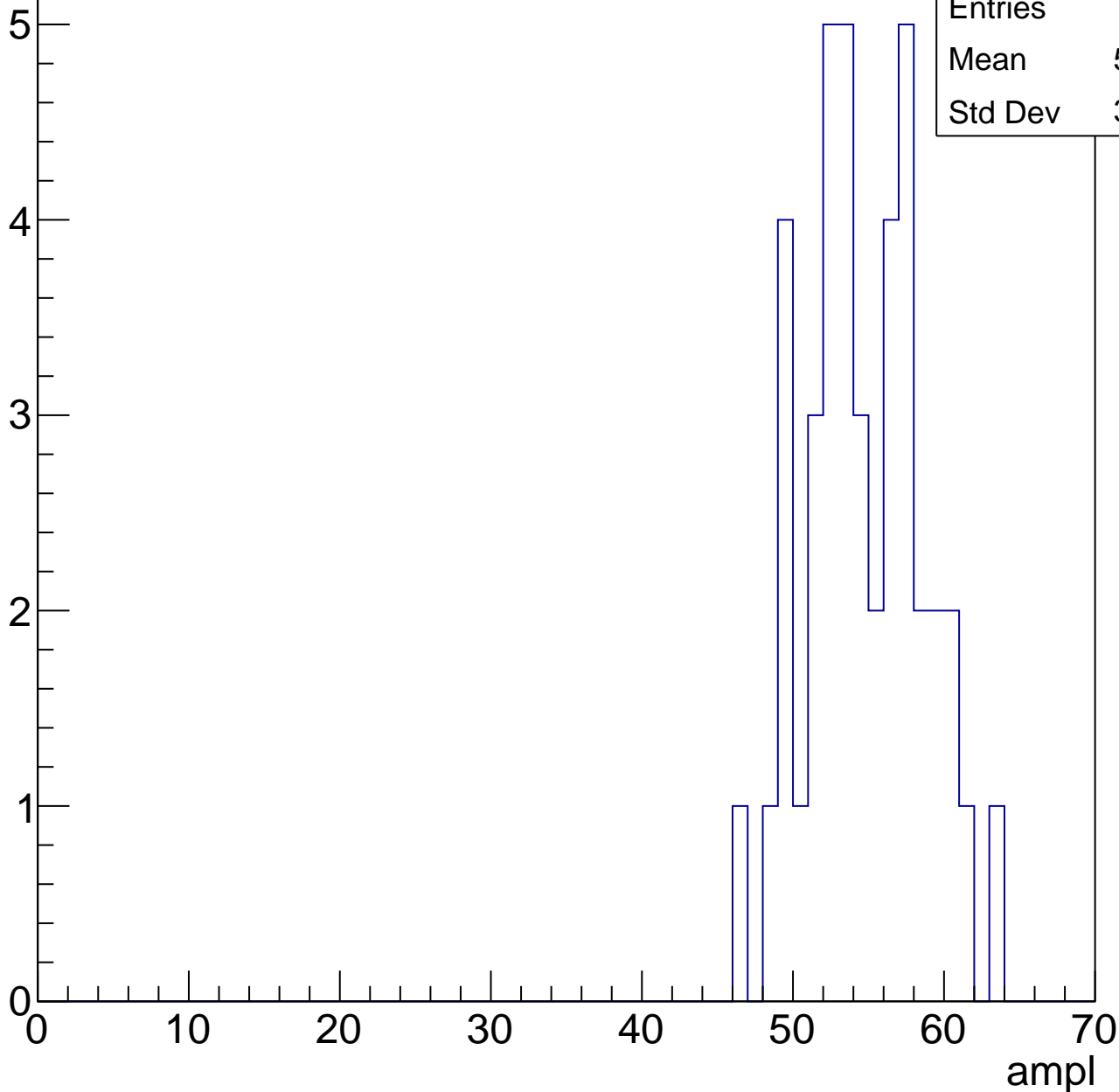


# B1L102S, U16-ch124, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	42
Mean	54.21
Std Dev	3.821

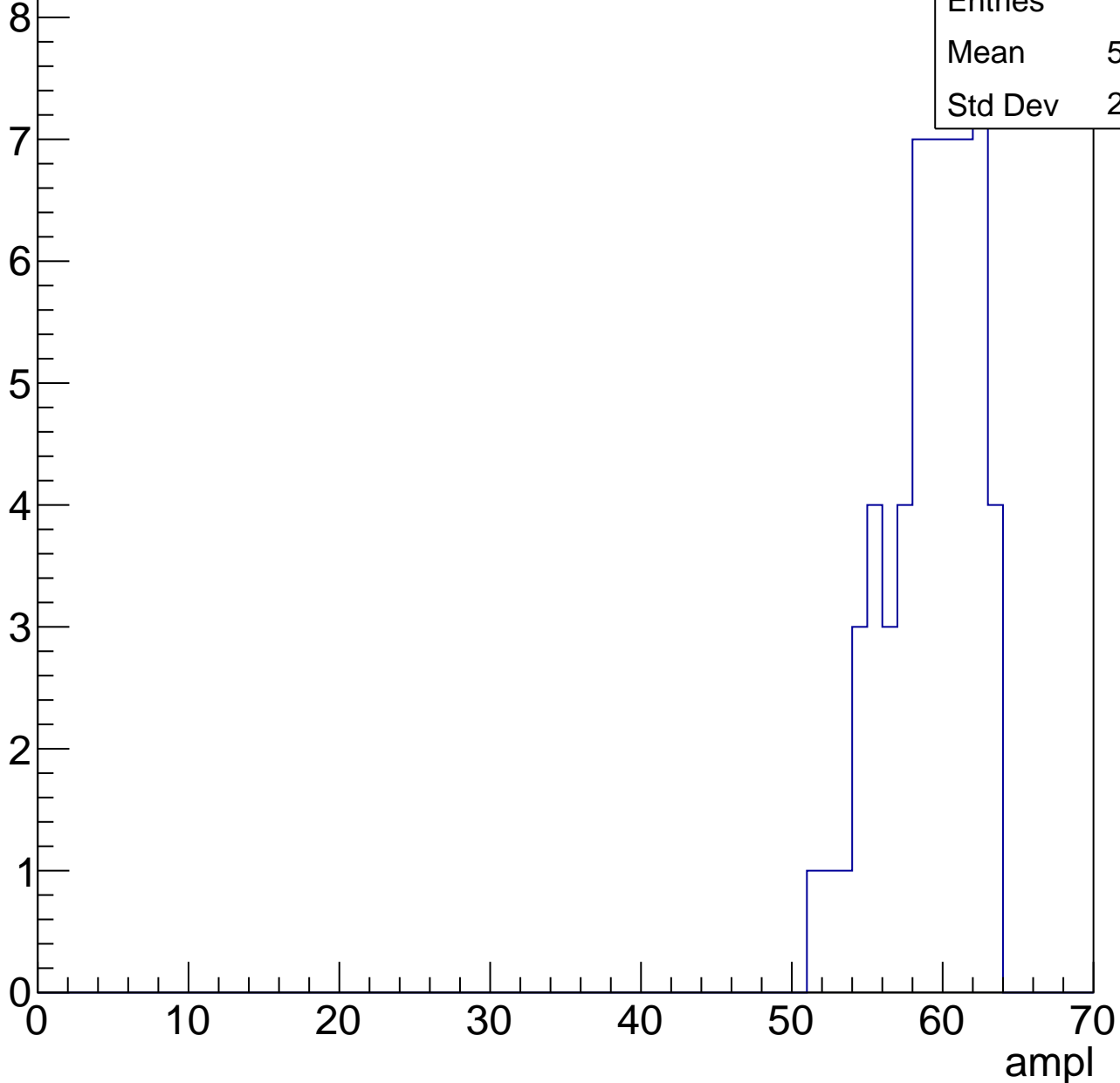


# B1L102S, U16-ch124, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	57
Mean	58.74
Std Dev	2.977

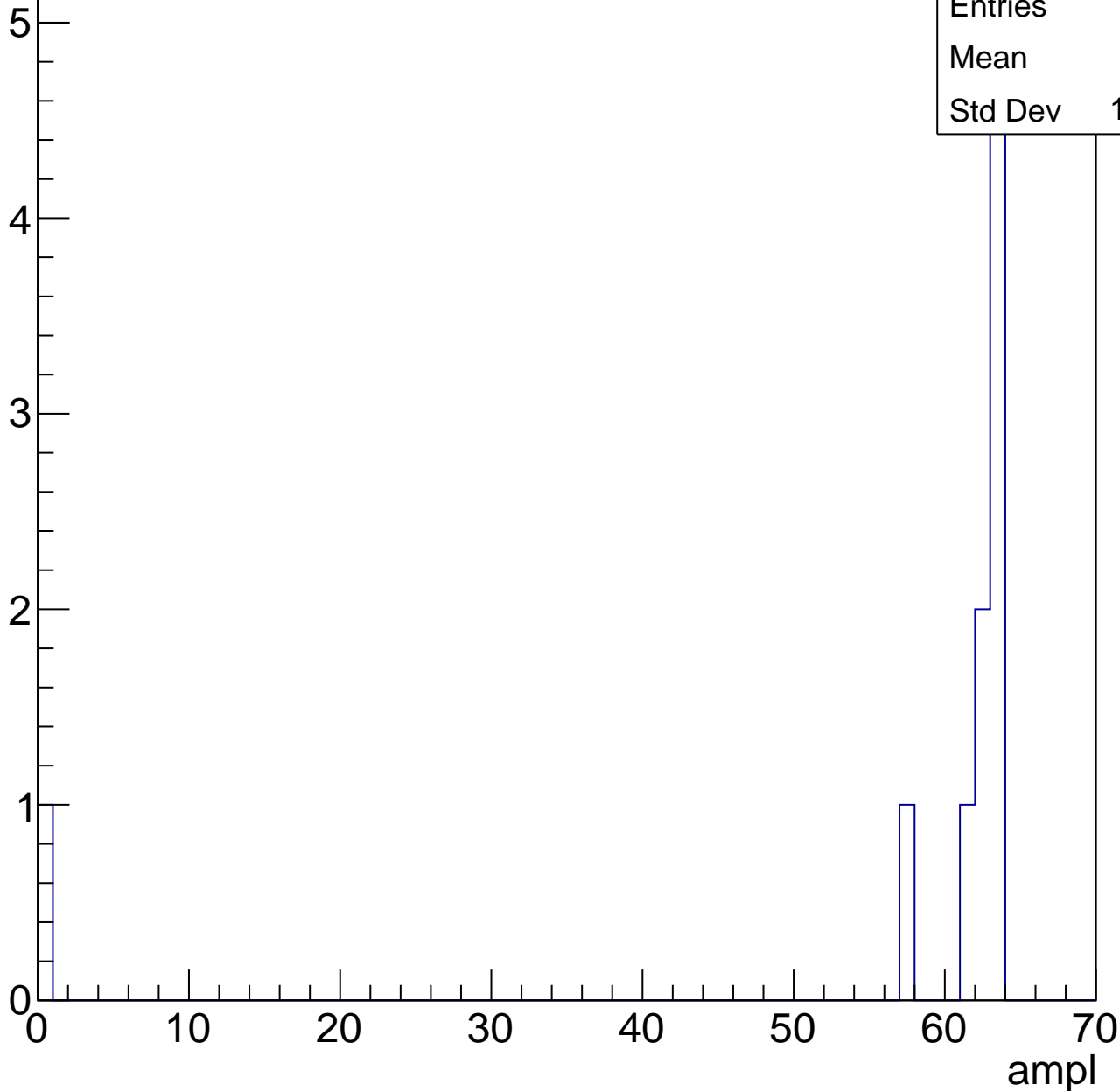


# B1L102S, U16-ch124, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	10
Mean	55.7
Std Dev	18.65





# B1L102S, U16-ch124, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch125, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	76
Mean	29.58
Std Dev	5.192

**Gaus mean : 31.0044**

**Gaus Width: 3.9689**

Entry

10  
8  
6  
4  
2  
0

ampl

0

10

20

30

40

50

60

70

# B1L102S, U16-ch125, adc1

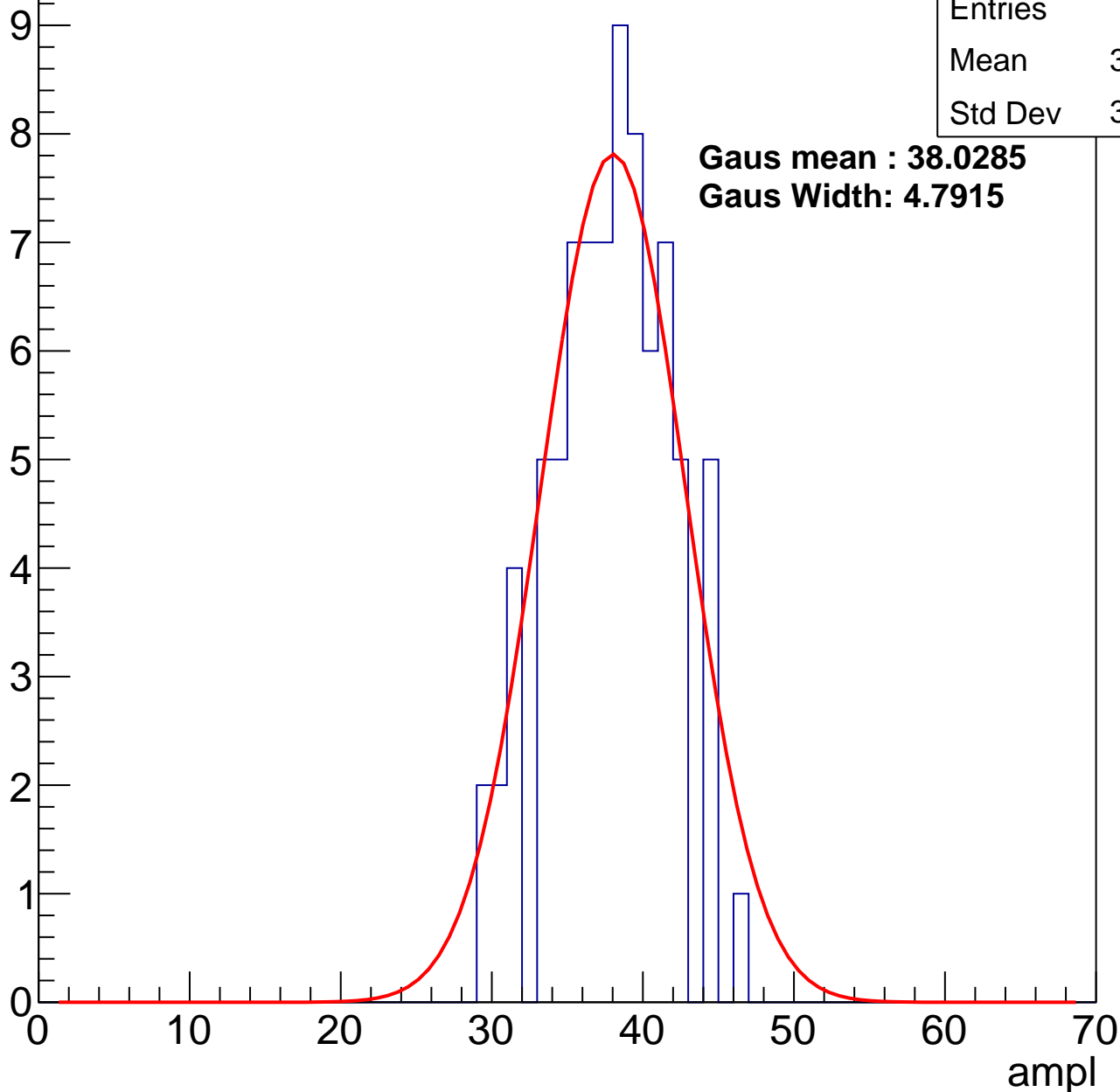
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	80
Mean	37.38
Std Dev	3.835

**Gaus mean : 38.0285**

**Gaus Width: 4.7915**



# B1L102S, U16-ch125, adc2

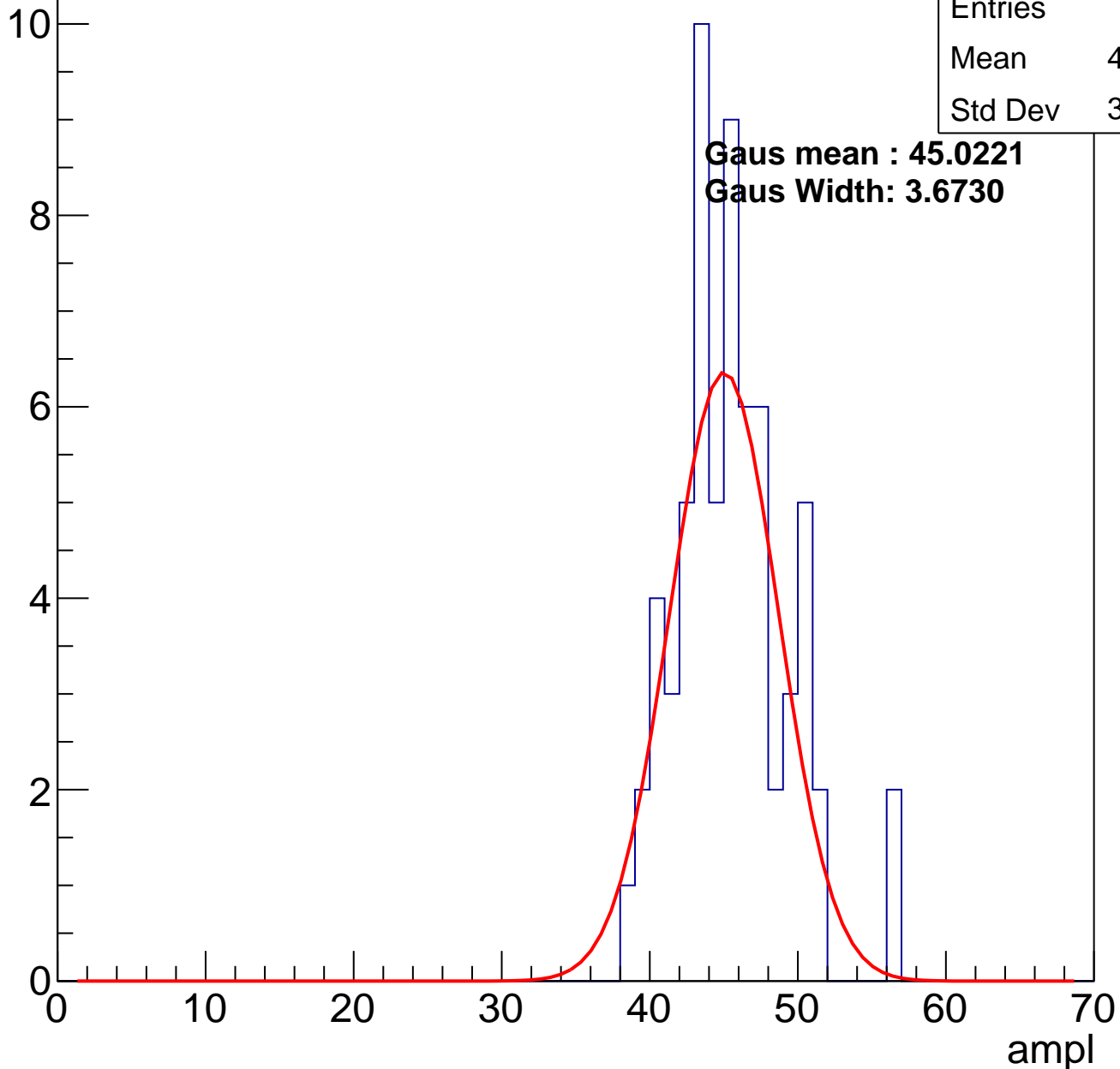
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	65
Mean	45.06
Std Dev	3.708

**Gaus mean : 45.0221**

**Gaus Width: 3.6730**

Entry

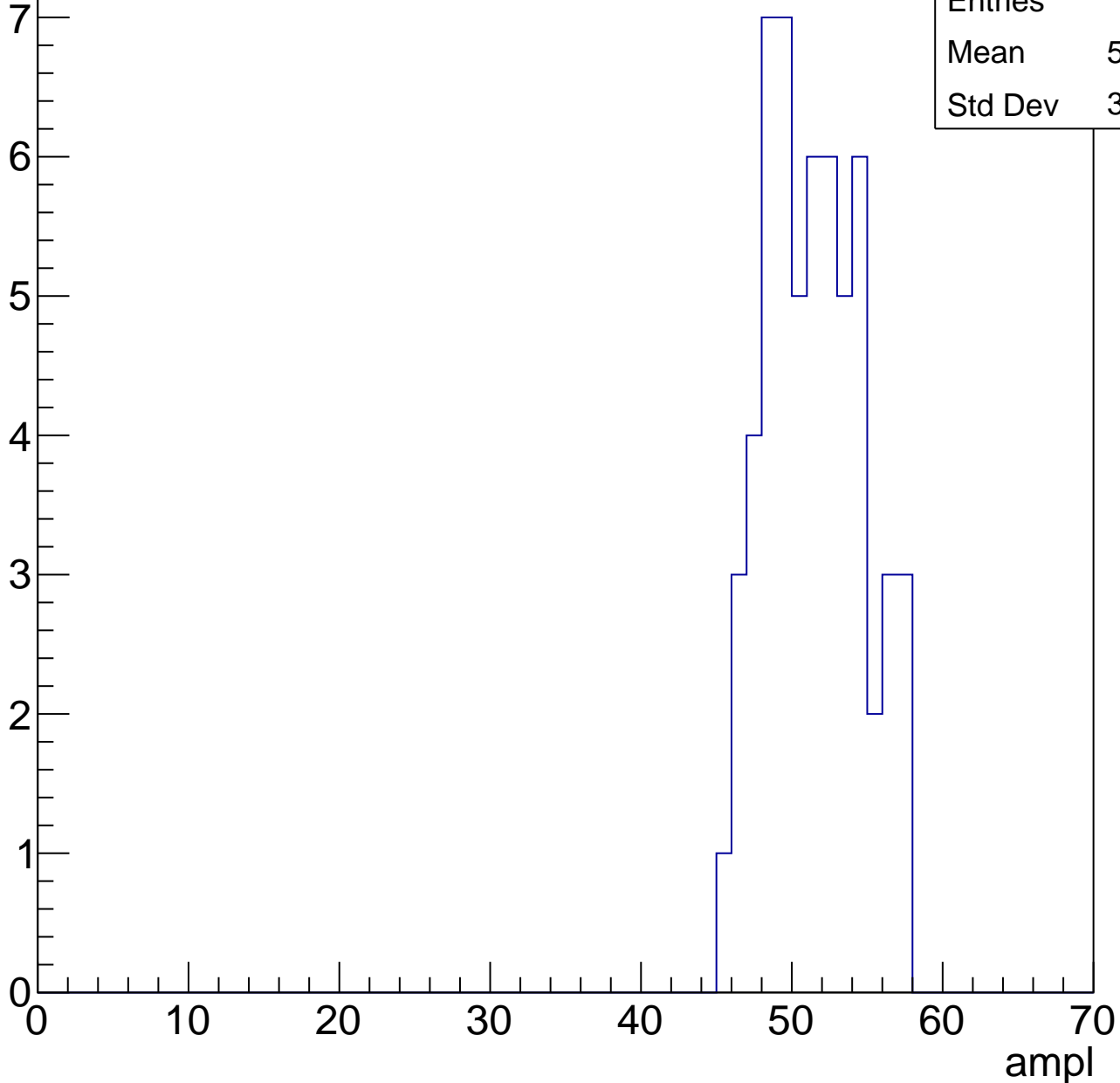


# B1L102S, U16-ch125, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	50.97
Std Dev	3.124

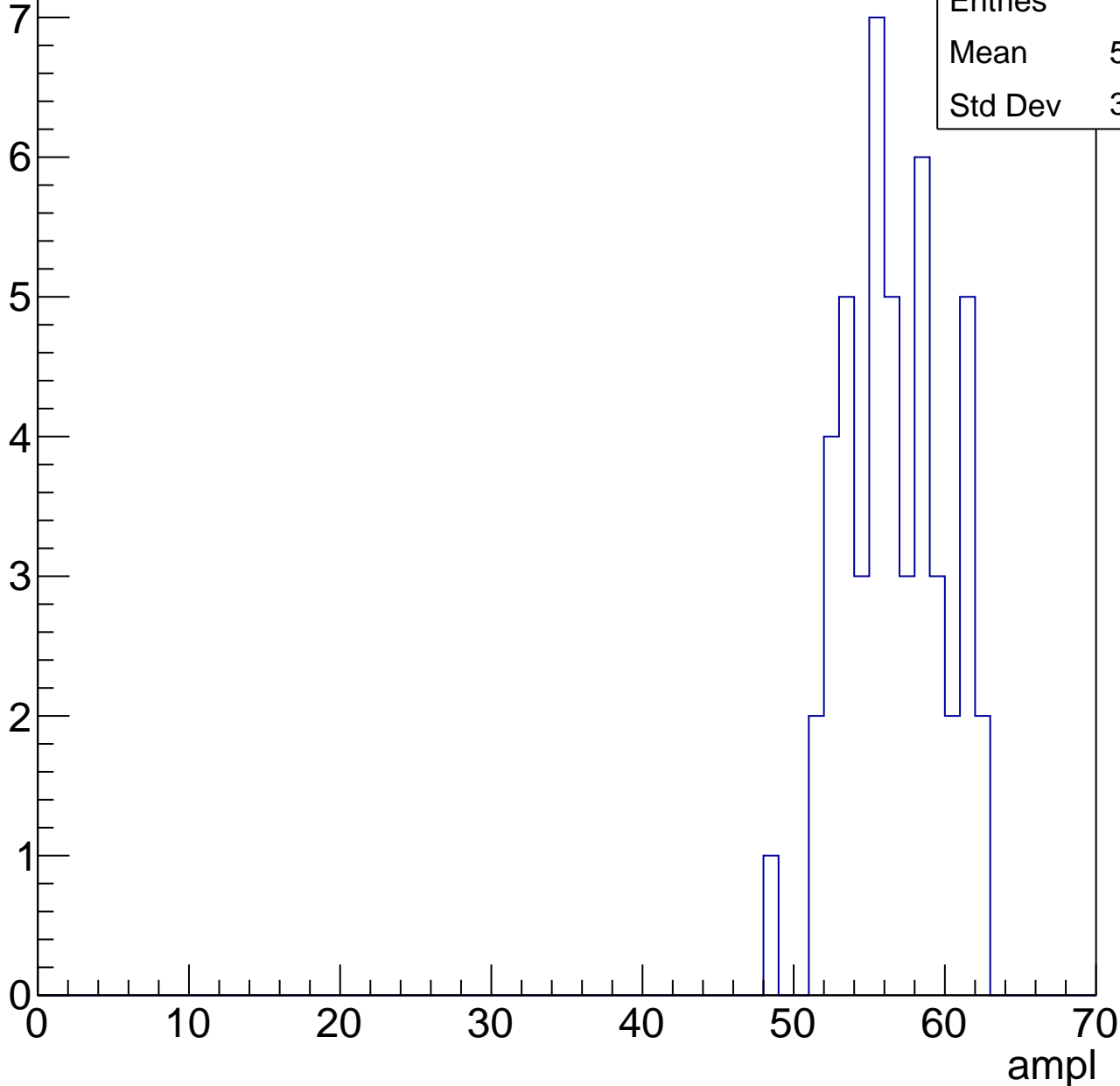


# B1L102S, U16-ch125, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	48
Mean	56.15
Std Dev	3.304

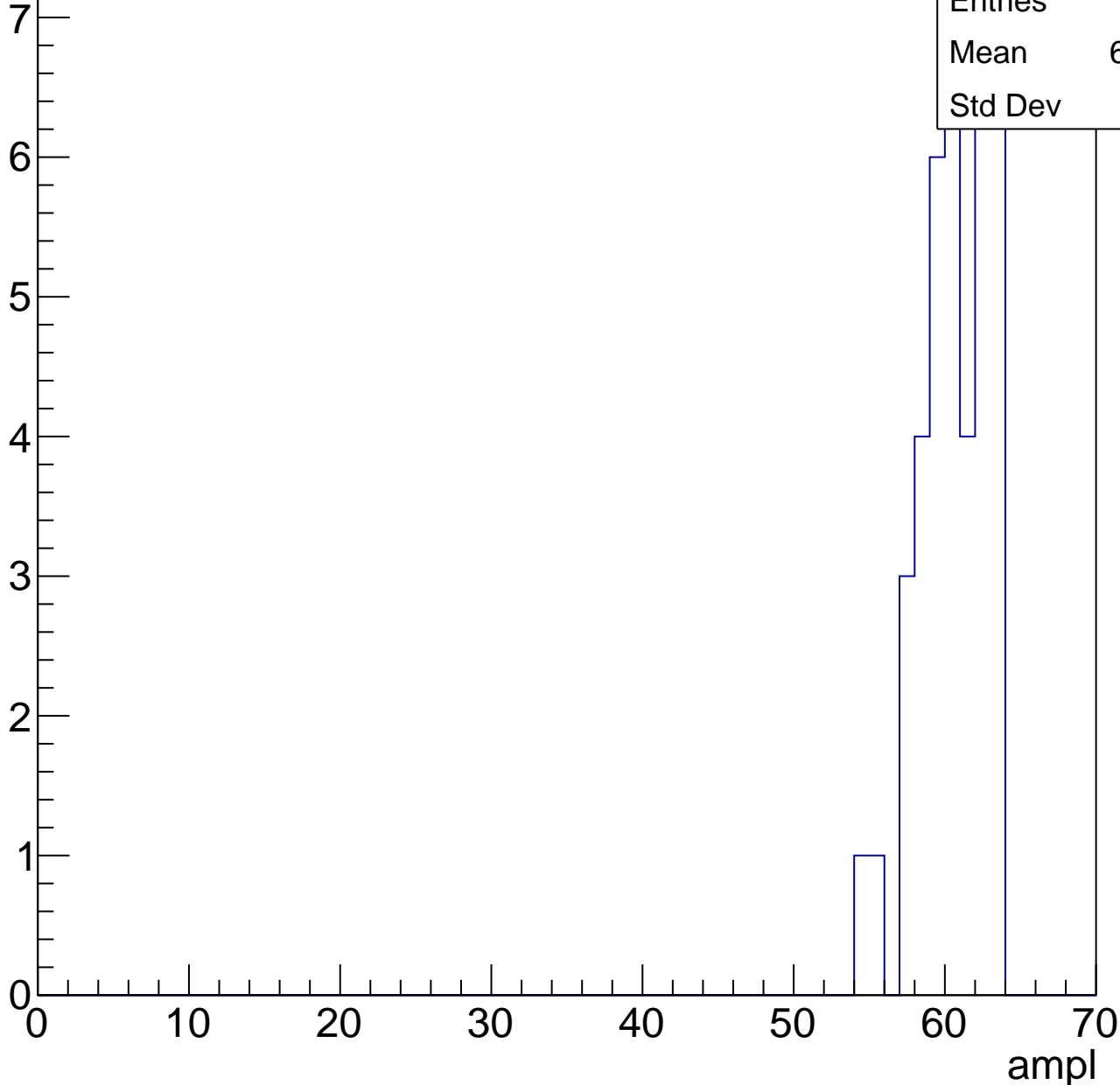


# B1L102S, U16-ch125, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

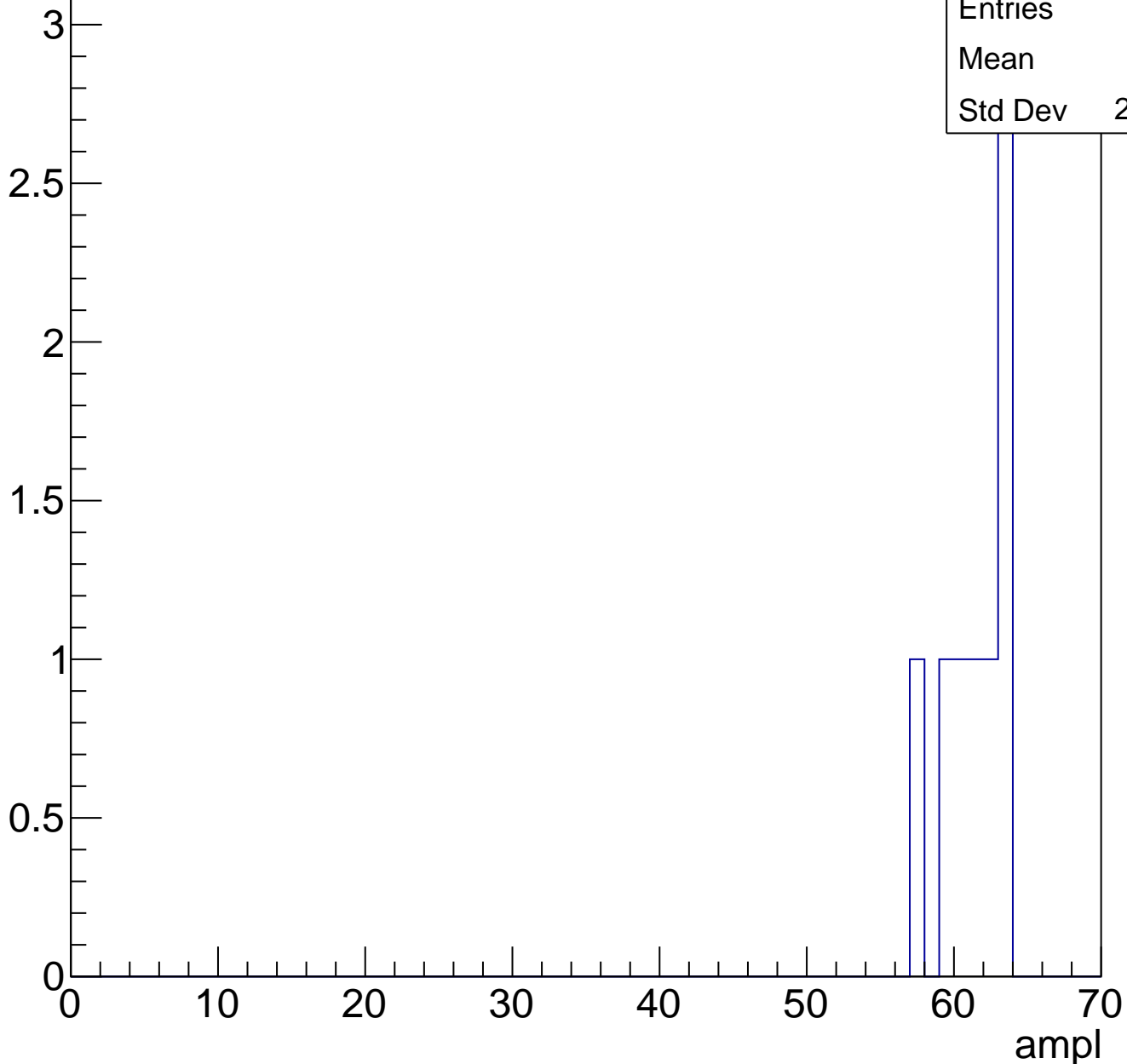
Entries	40
Mean	60.12
Std Dev	2.26



# B1L102S, U16-ch125, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch125, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



# B1L102S, U16-ch126, adc0

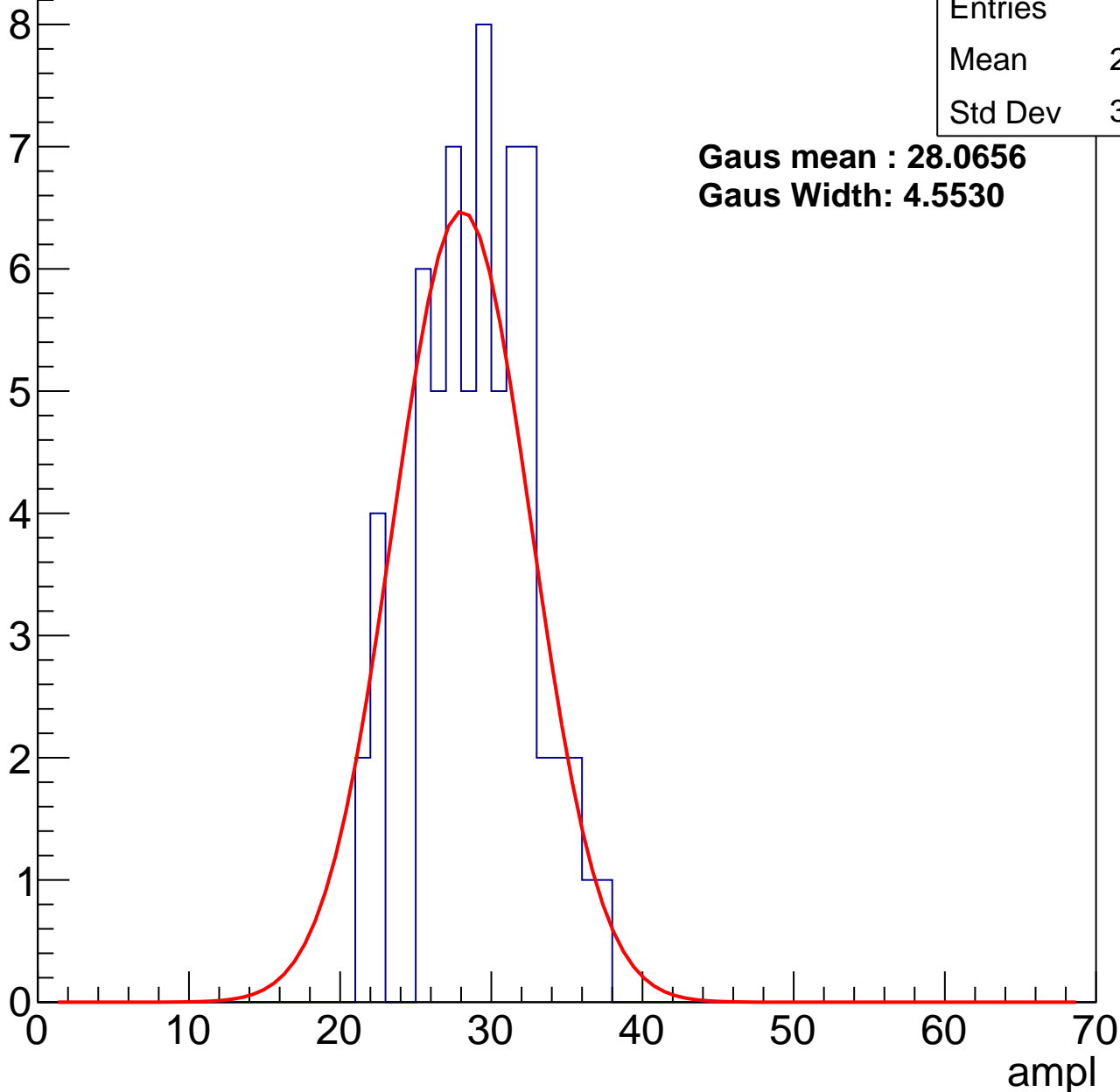
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	64
Mean	28.73
Std Dev	3.658

**Gaus mean : 28.0656**

**Gaus Width: 4.5530**



# B1L102S, U16-ch126, adc1

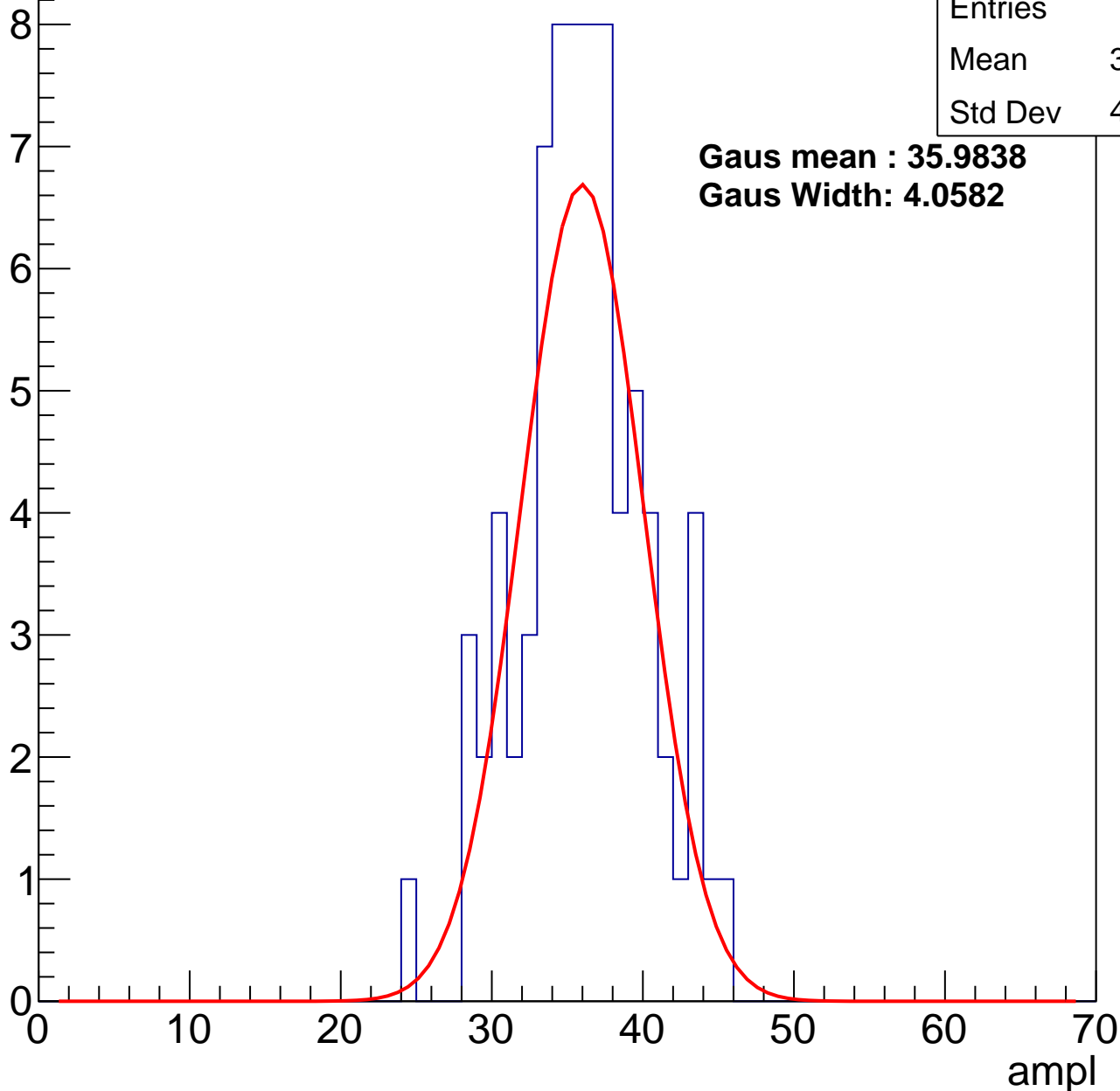
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	76
Mean	35.57
Std Dev	4.175

**Gaus mean : 35.9838**

**Gaus Width: 4.0582**



# B1L102S, U16-ch126, adc2

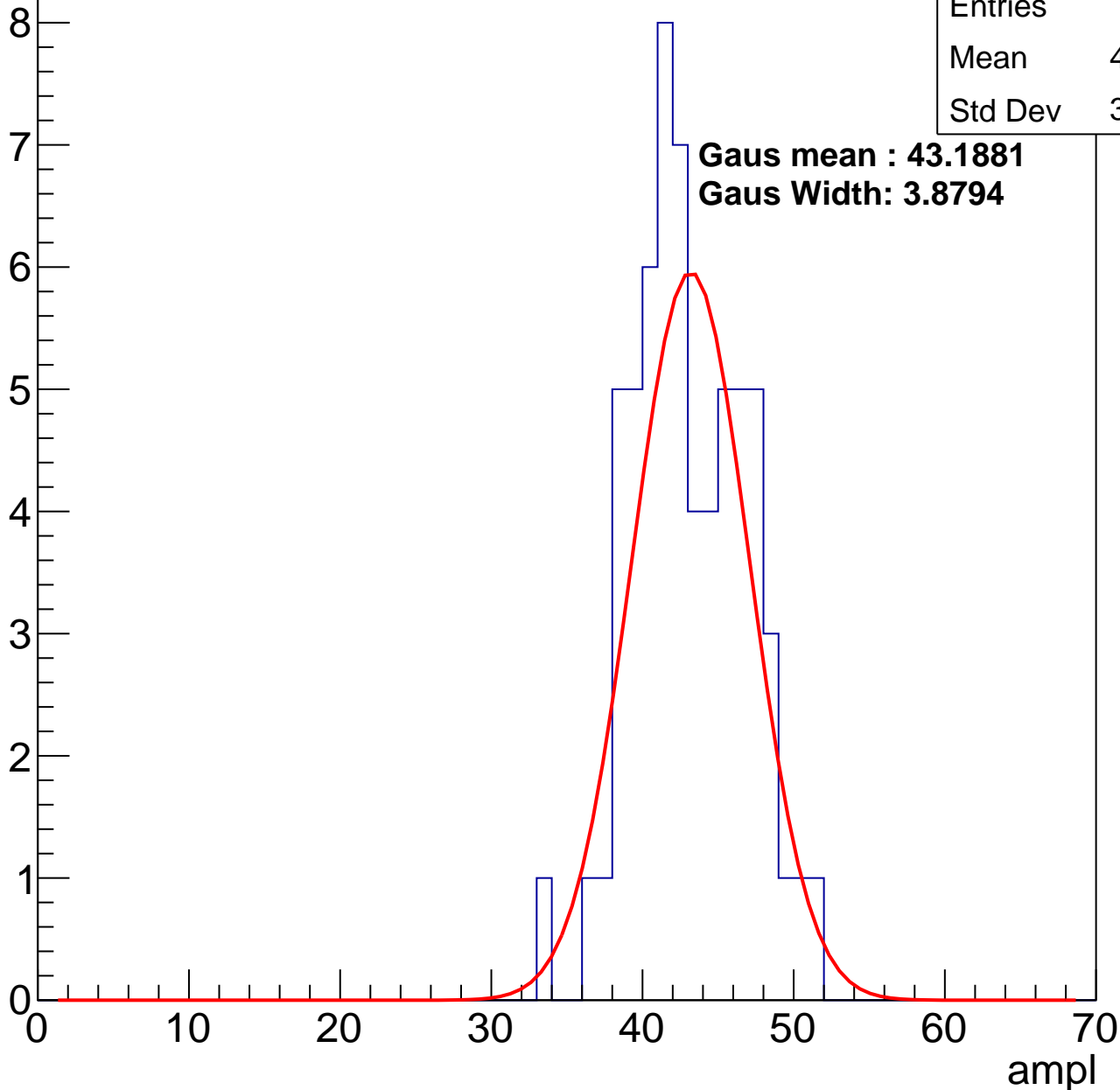
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	63
Mean	42.62
Std Dev	3.666

**Gaus mean : 43.1881**

**Gaus Width: 3.8794**

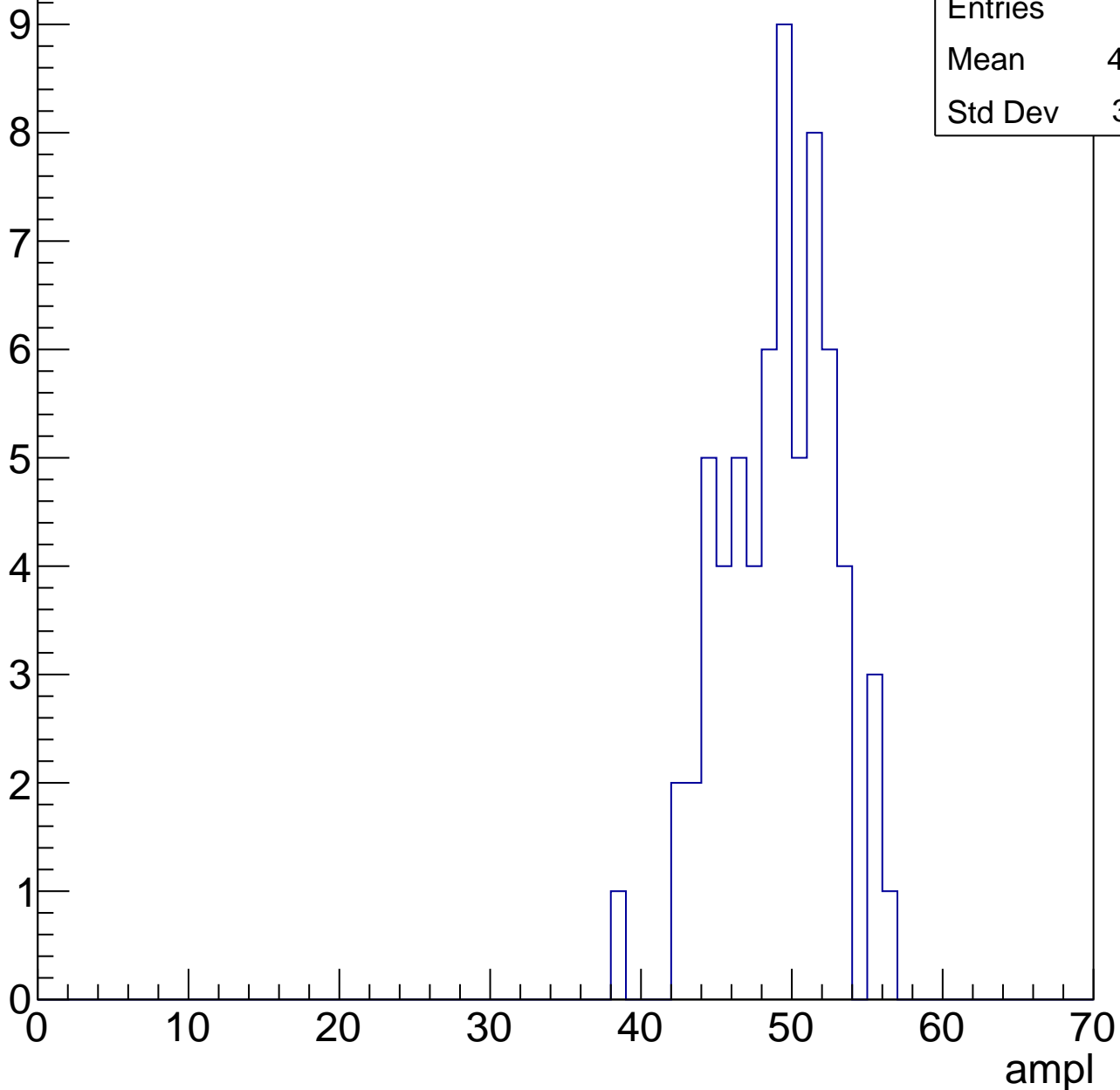


# B1L102S, U16-ch126, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	65
Mean	48.58
Std Dev	3.611

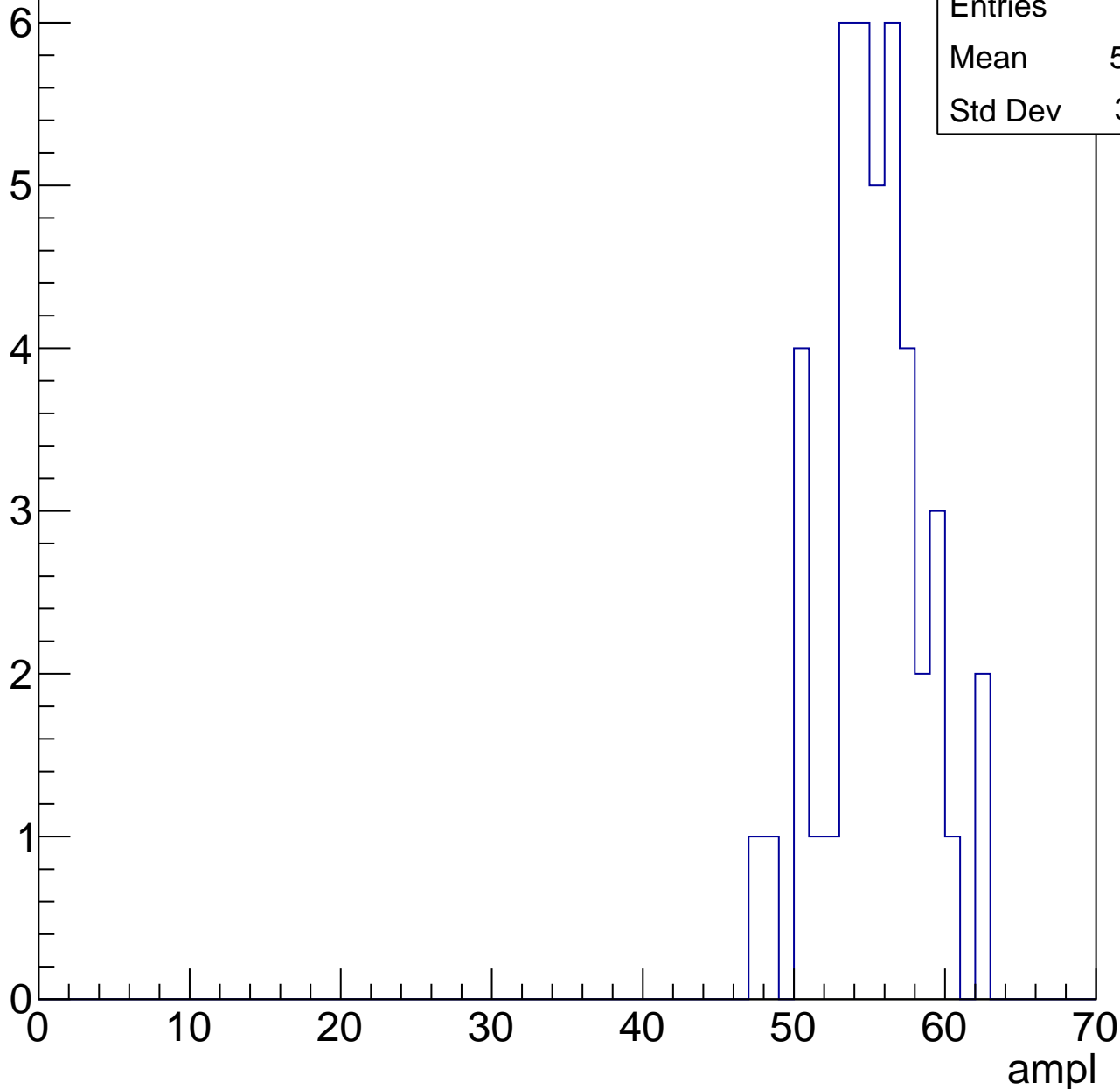


# B1L102S, U16-ch126, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	43
Mean	54.79
Std Dev	3.331

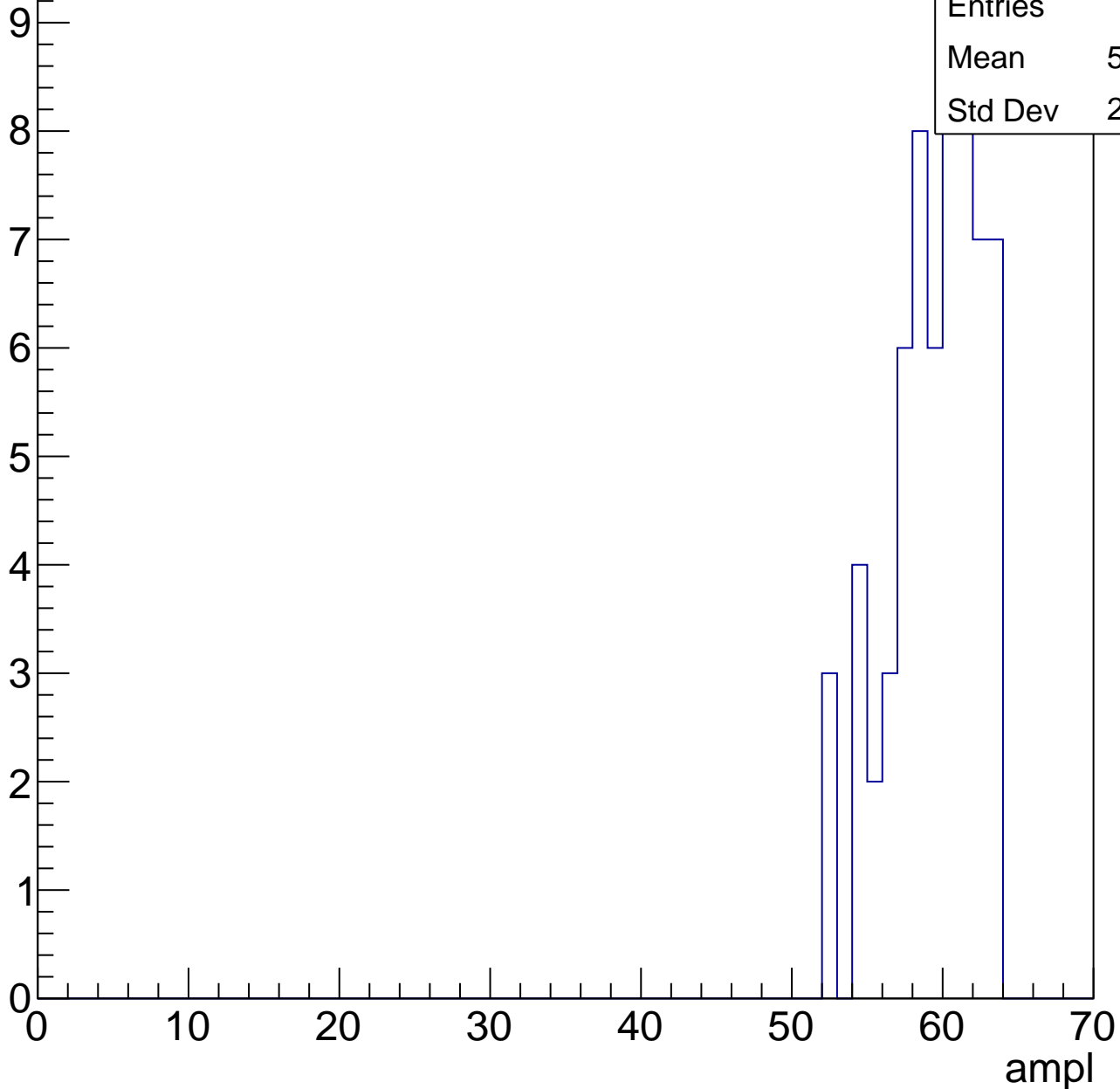


# B1L102S, U16-ch126, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

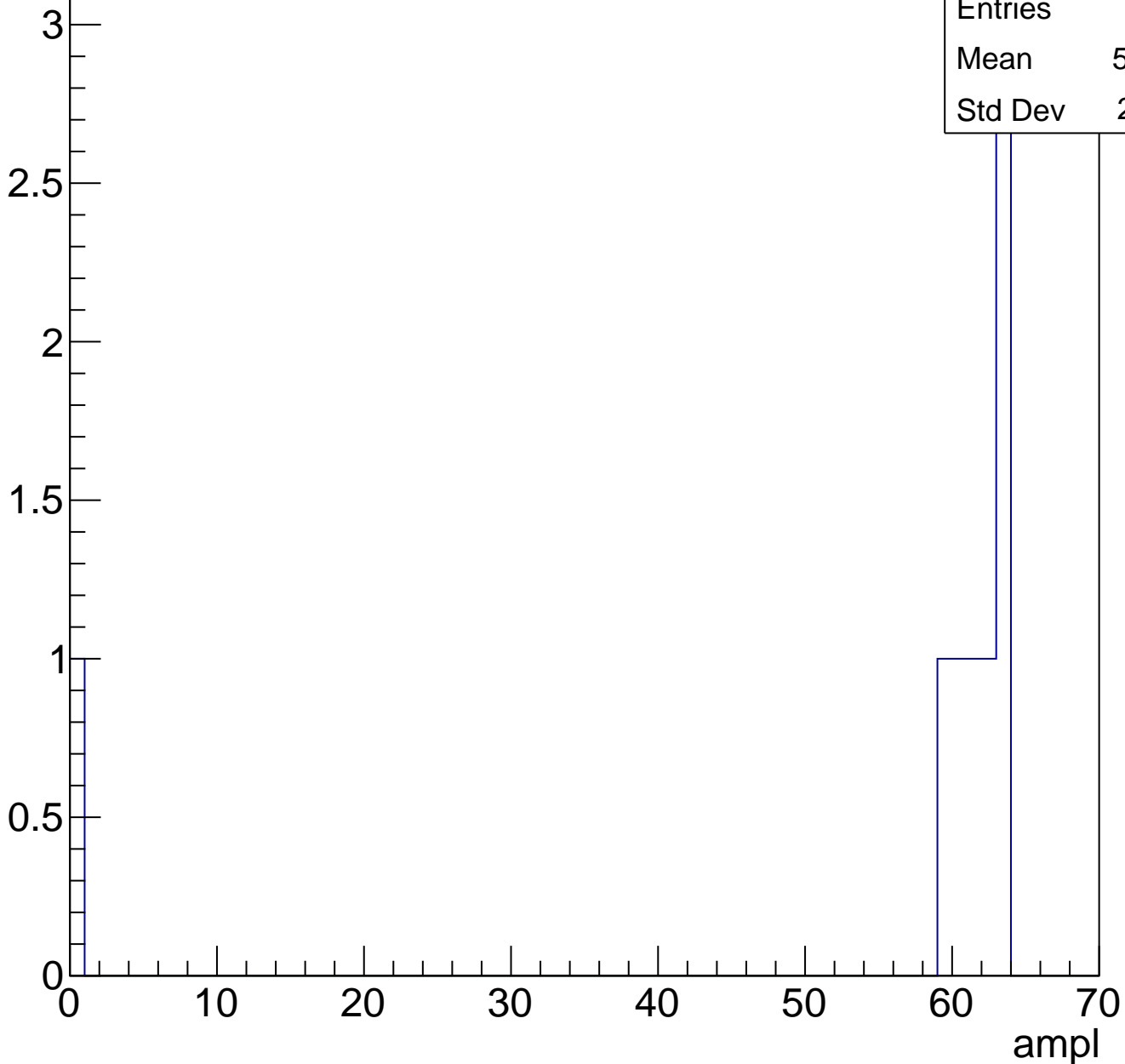
Entries	63
Mean	58.95
Std Dev	2.973



# B1L102S, U16-ch126, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch126, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	0
Mean	0
Std Dev	0

# B1L102S, U16-ch127, adc0

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entries	70
Mean	28.69
Std Dev	3.479

**Gaus mean : 28.7724**

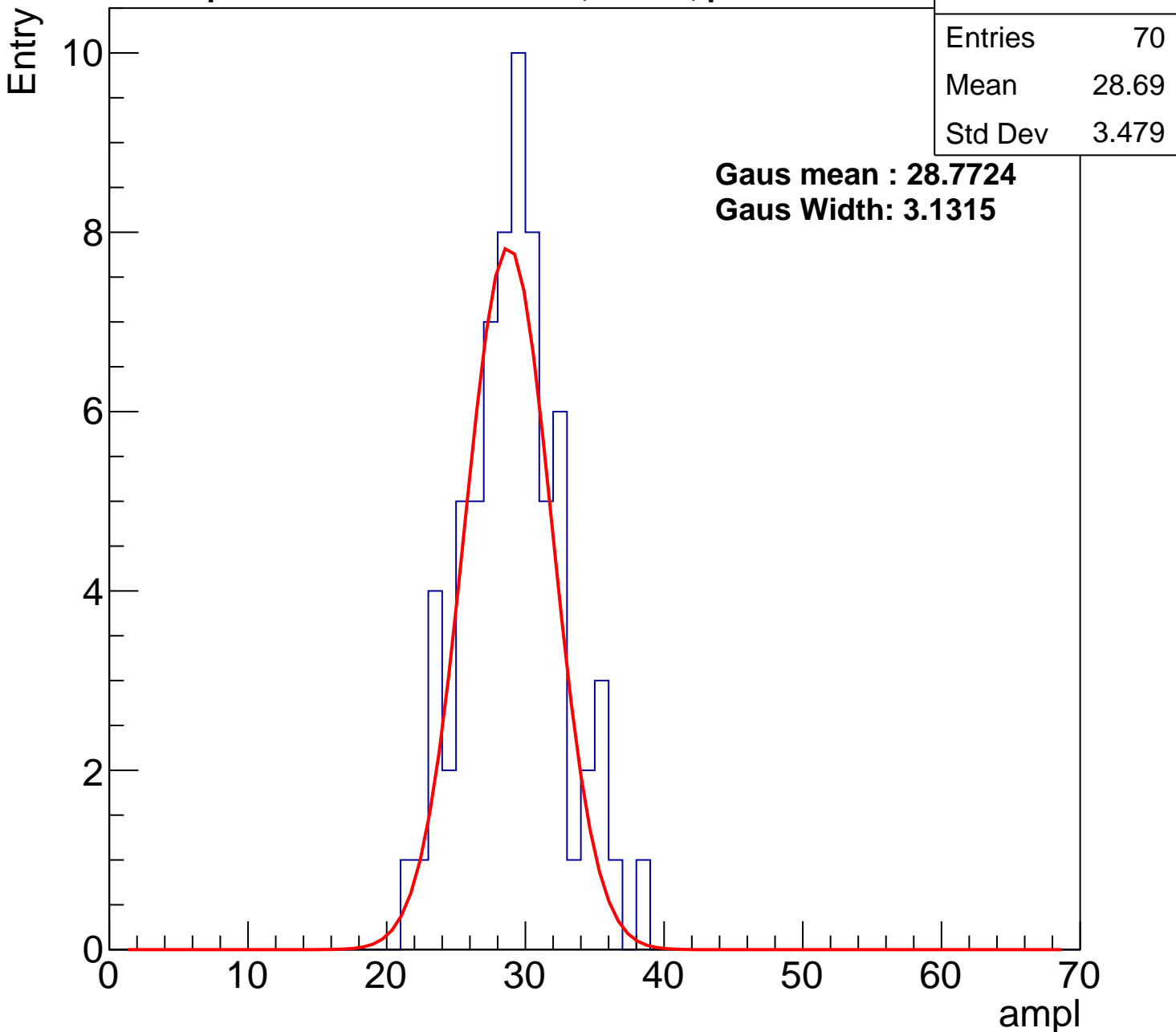
**Gaus Width: 3.1315**

Entry

10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L102S, U16-ch127, adc1

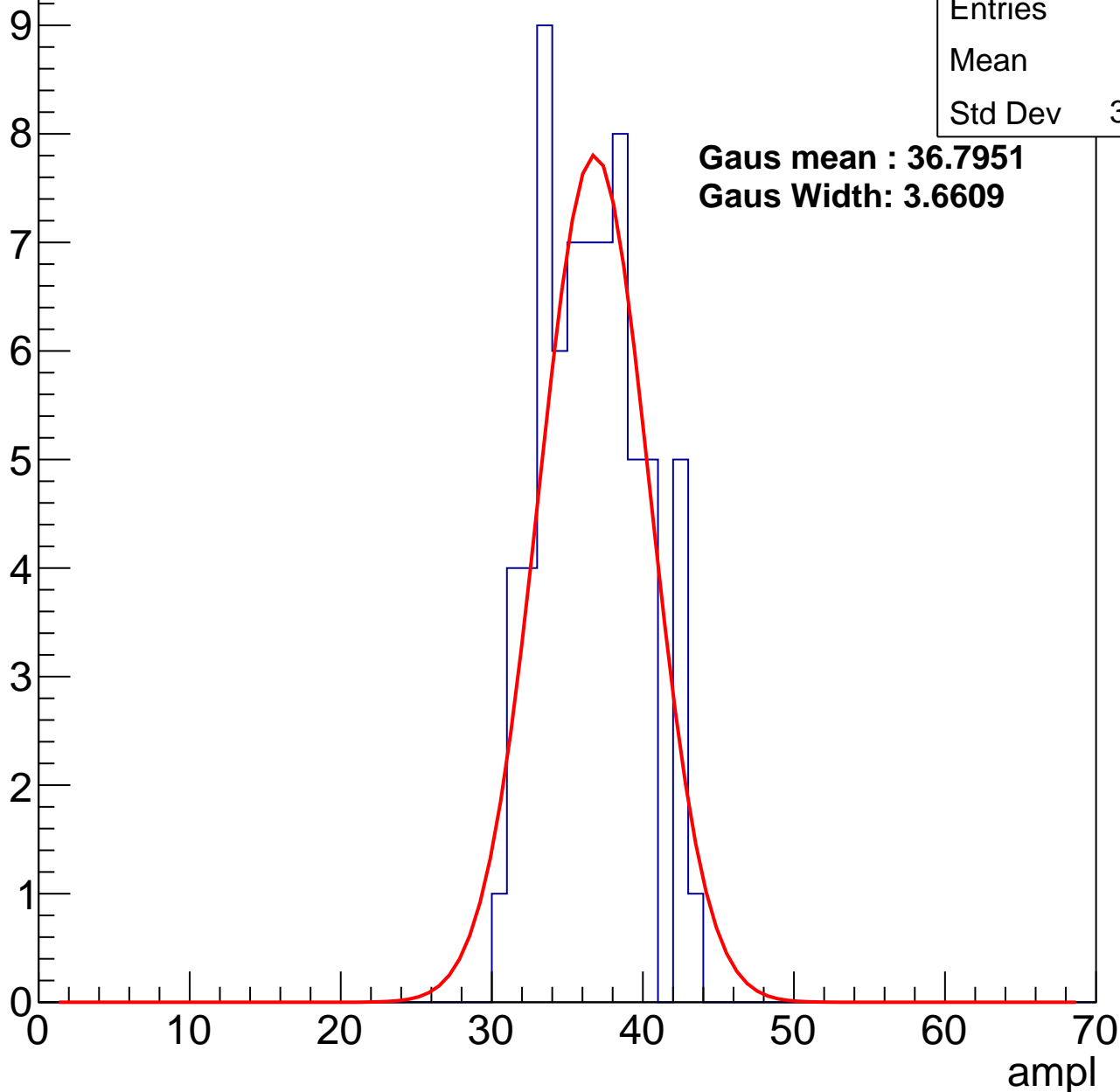
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	69
Mean	36.1
Std Dev	3.195

**Gaus mean : 36.7951**

**Gaus Width: 3.6609**



# B1L102S, U16-ch127, adc2

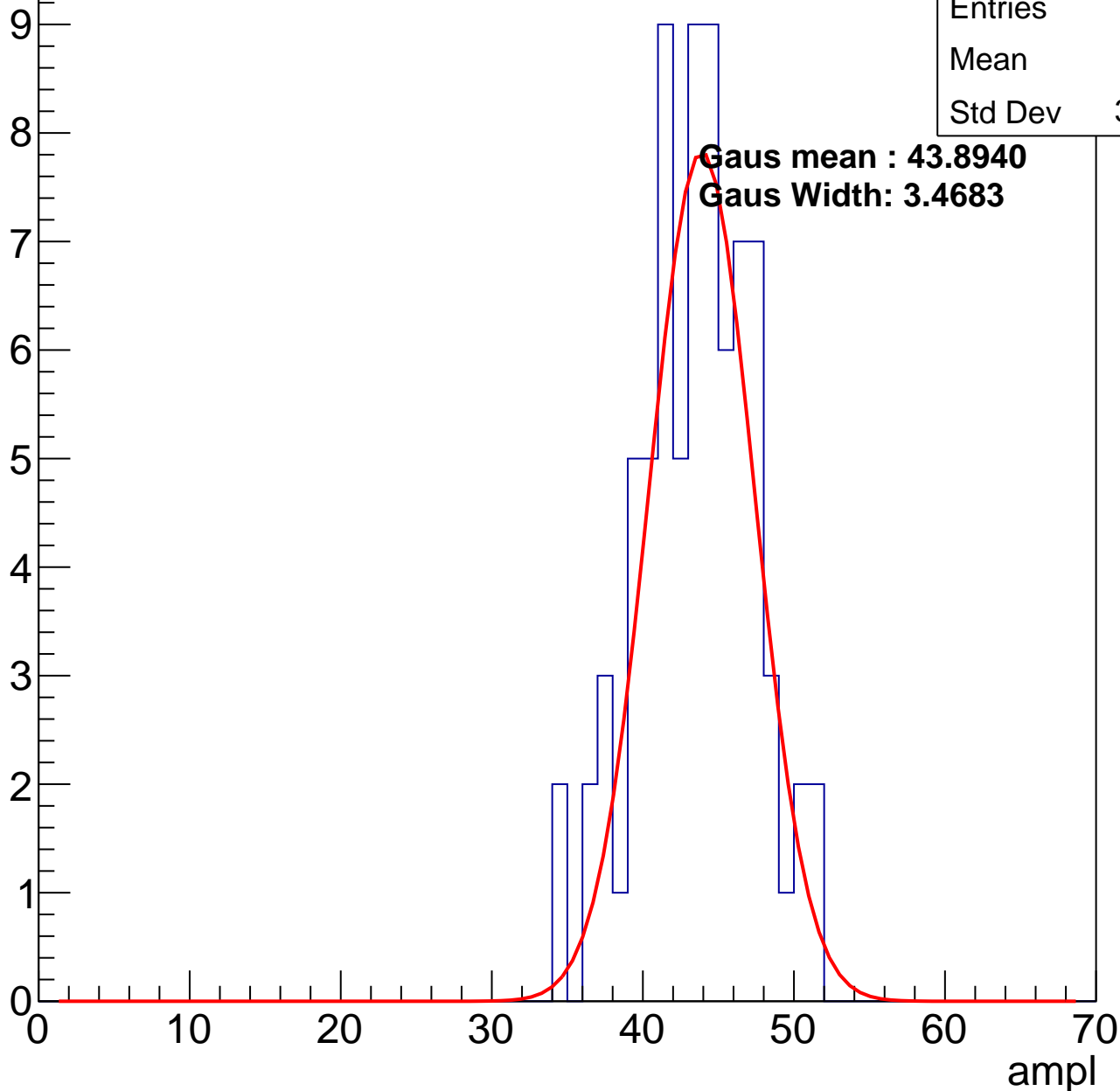
calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	78
Mean	43.1
Std Dev	3.761

**Gaus mean : 43.8940**

**Gaus Width: 3.4683**

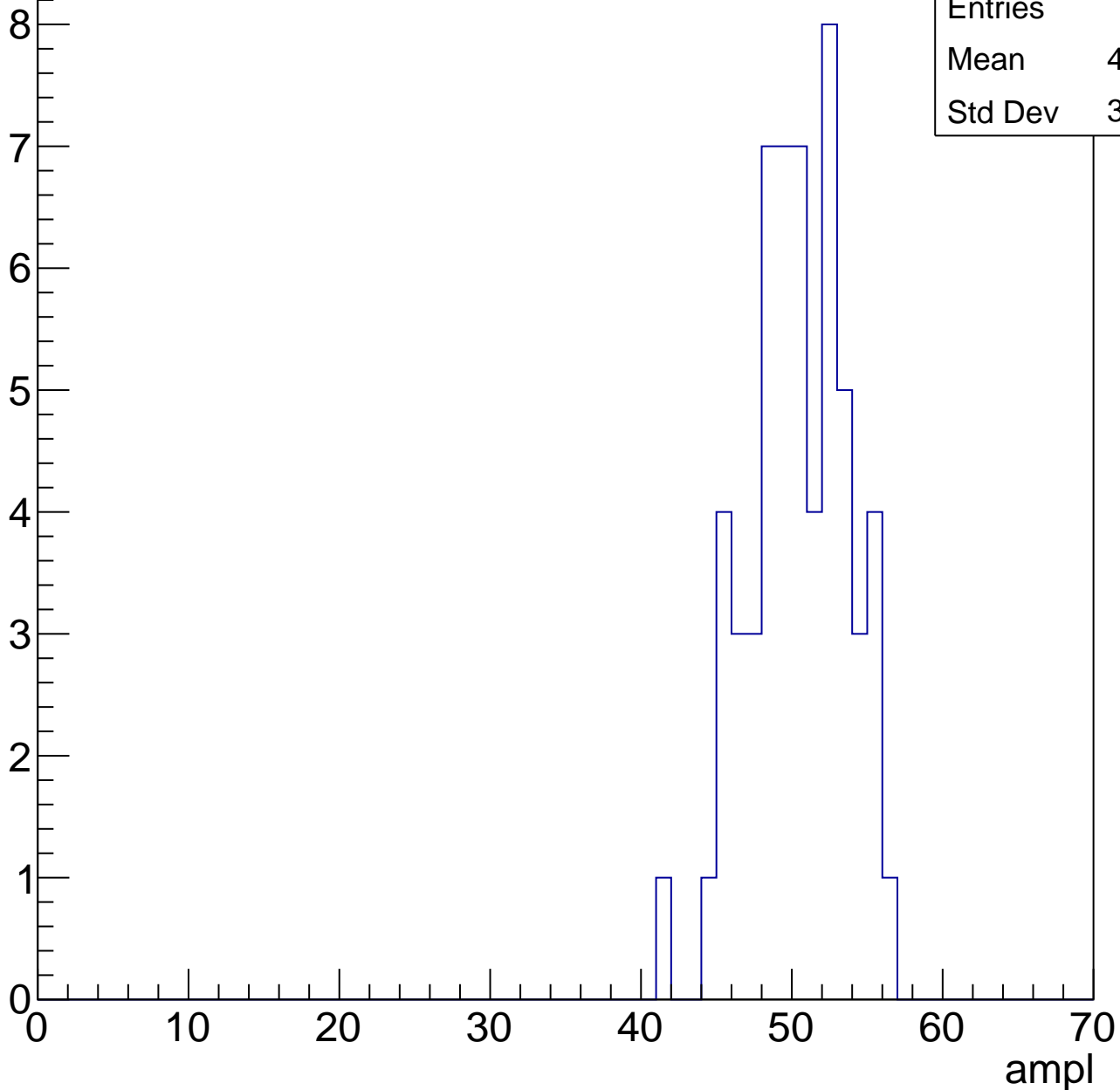


# B1L102S, U16-ch127, adc3

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	58
Mean	49.93
Std Dev	3.194

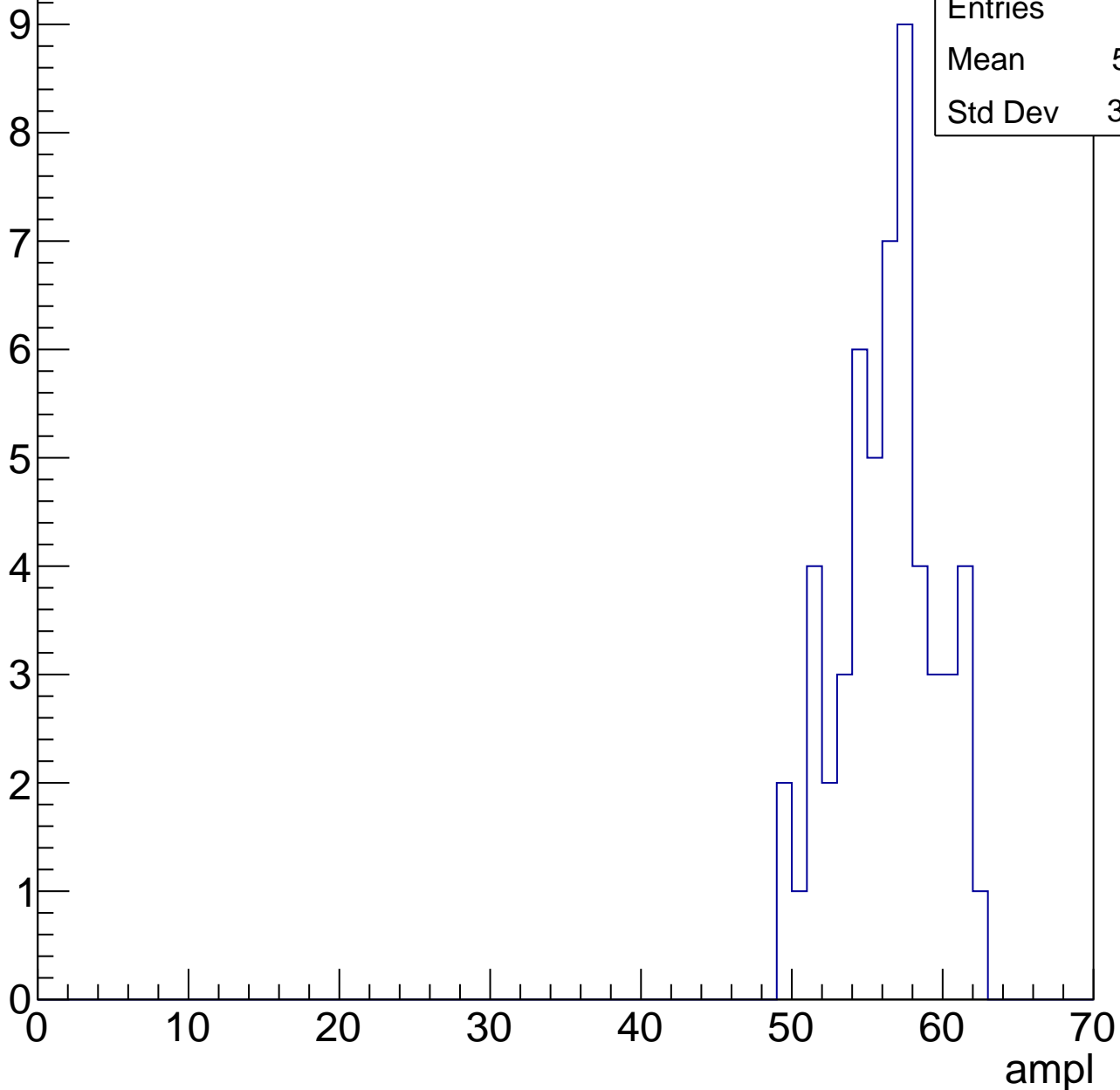


# B1L102S, U16-ch127, adc4

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

Entries	54
Mean	55.81
Std Dev	3.209



# B1L102S, U16-ch127, adc5

calib\_packv5\_042523\_0143.root, FC#11, port A2

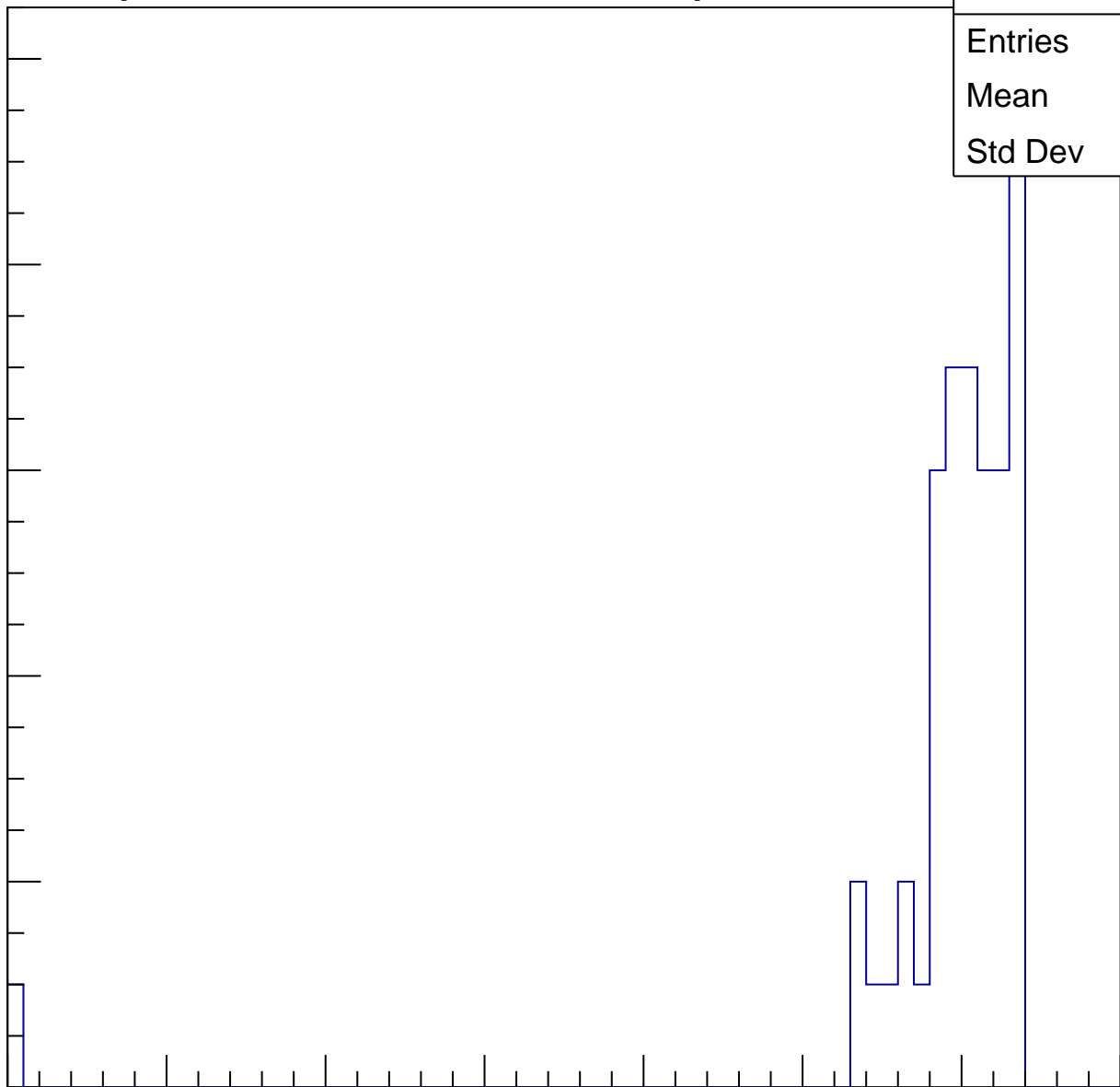
Entries	50
Mean	58.66
Std Dev	8.788

Entry

10  
8  
6  
4  
2  
0

0 10 20 30 40 50 60 70

ampl



# B1L102S, U16-ch127, adc6

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry





# B1L102S, U16-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry

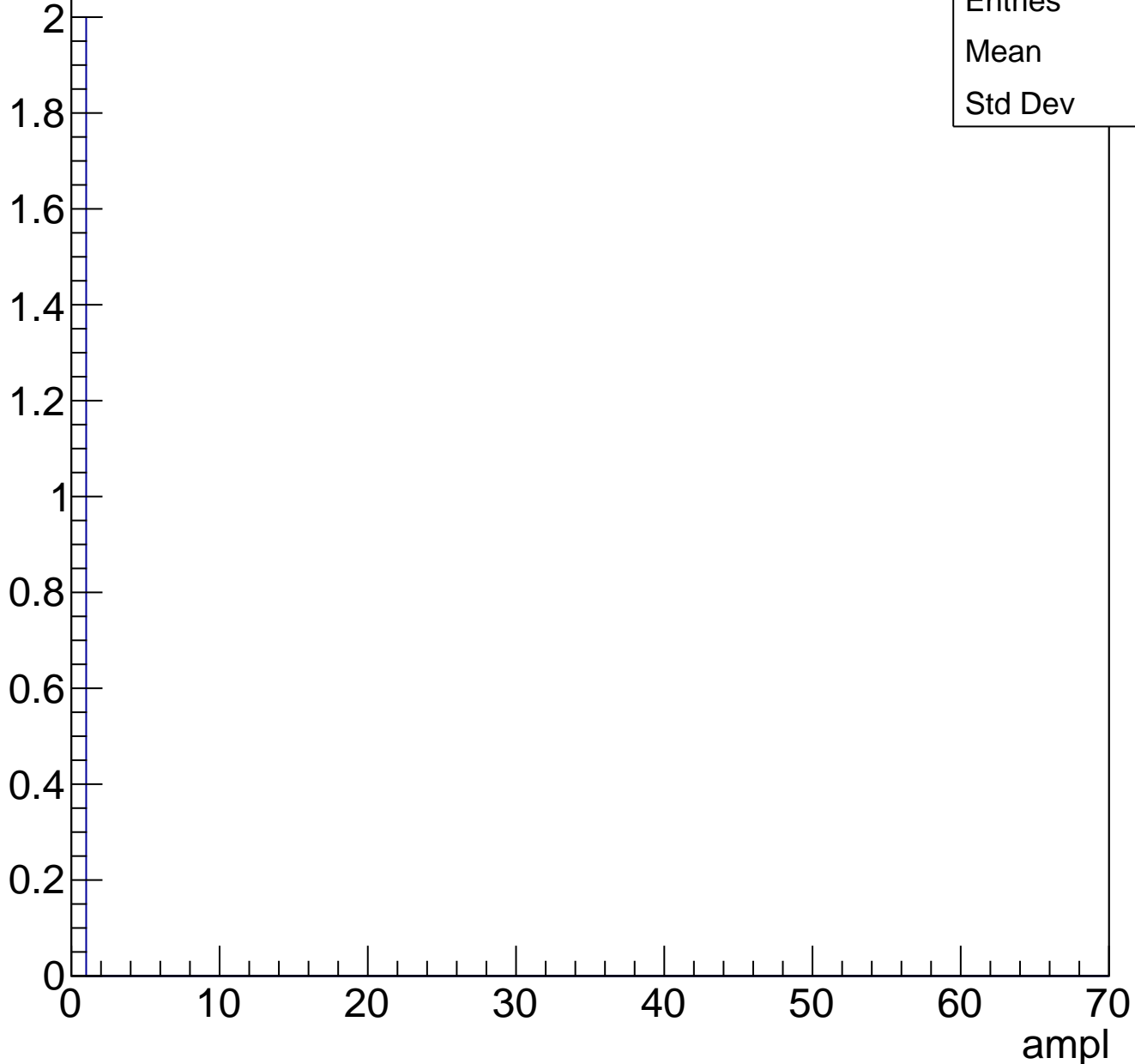


Entries	2
Mean	0
Std Dev	0

# B1L102S, U16-ch127, adc7

calib\_packv5\_042523\_0143.root, FC#11, port A2

Entry



Entries	2
Mean	0
Std Dev	0