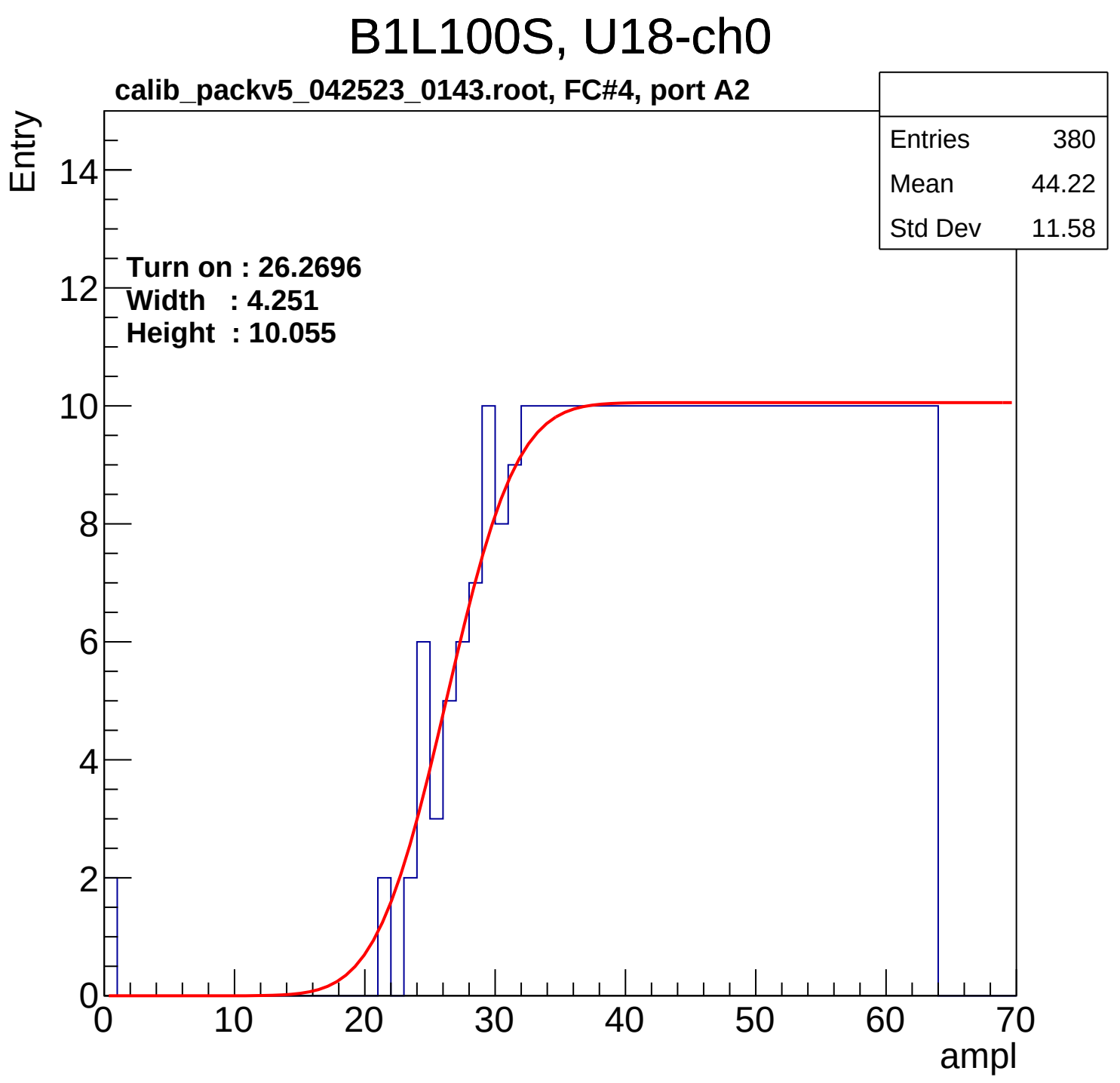
B1L100S, U18-ch0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.22
Std Dev 11.58
Turn on : 26.2696
Width : 4.251
Height : 10.055
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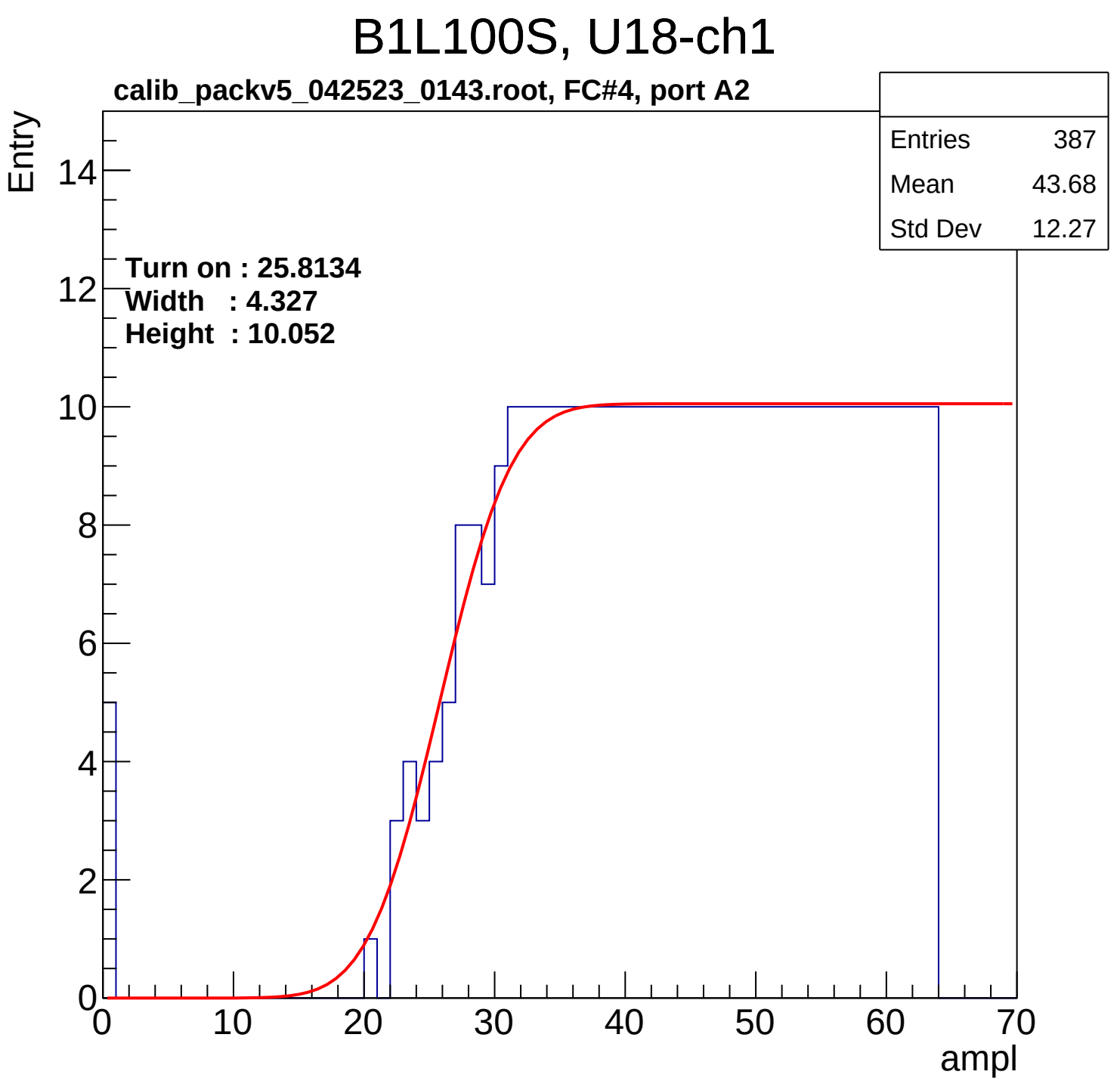
B1L100S, U18-ch1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 387
Mean 43.68
Std Dev 12.27
Turn on : 25.8134
Width : 4.327
Height : 10.052
Entry
ampl
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2
4
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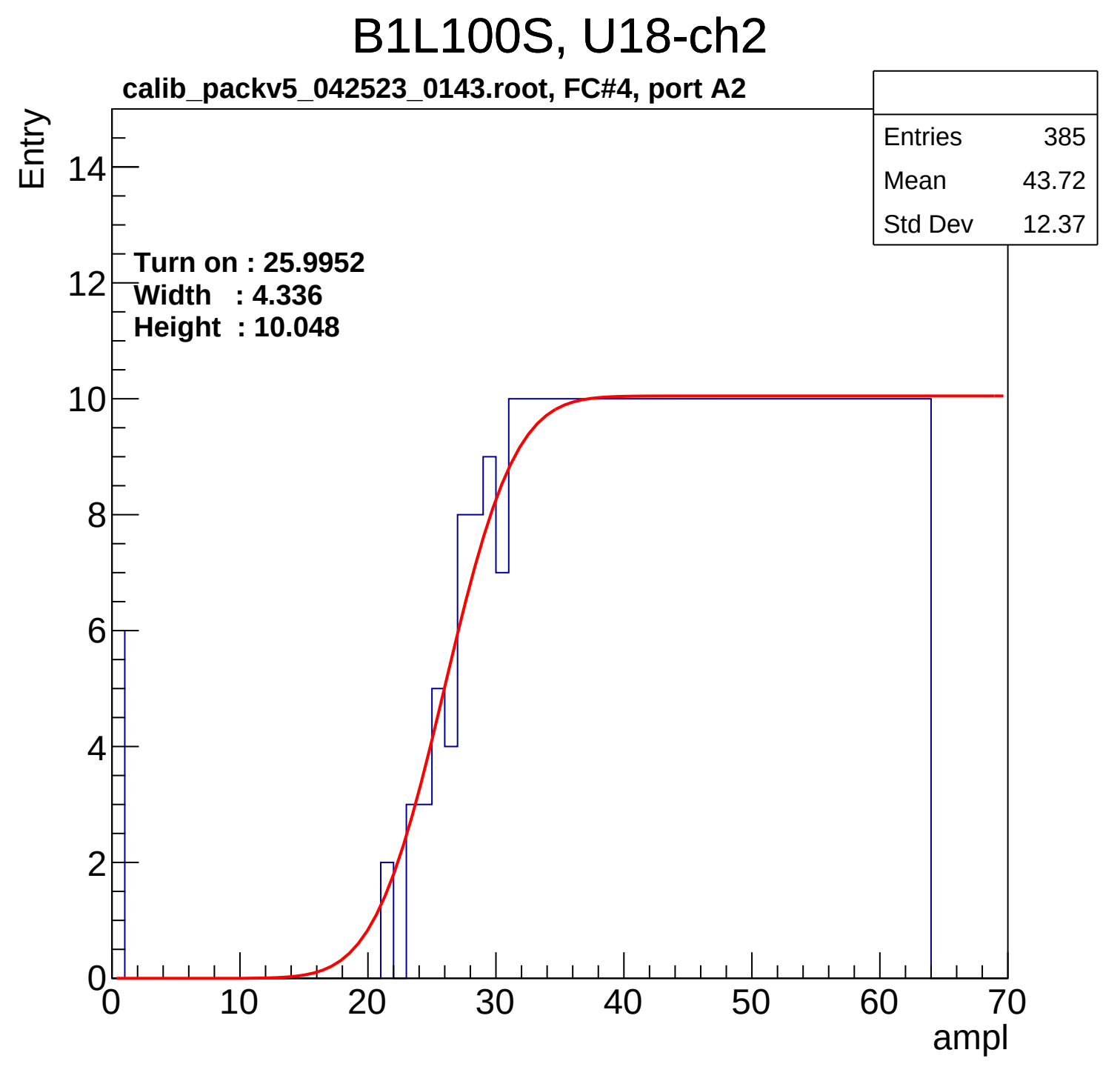
B1L100S, U18-ch2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 385
Mean 43.72
Std Dev 12.37
Turn on : 25.9952
Width : 4.336
Height : 10.048
Entry
ampl
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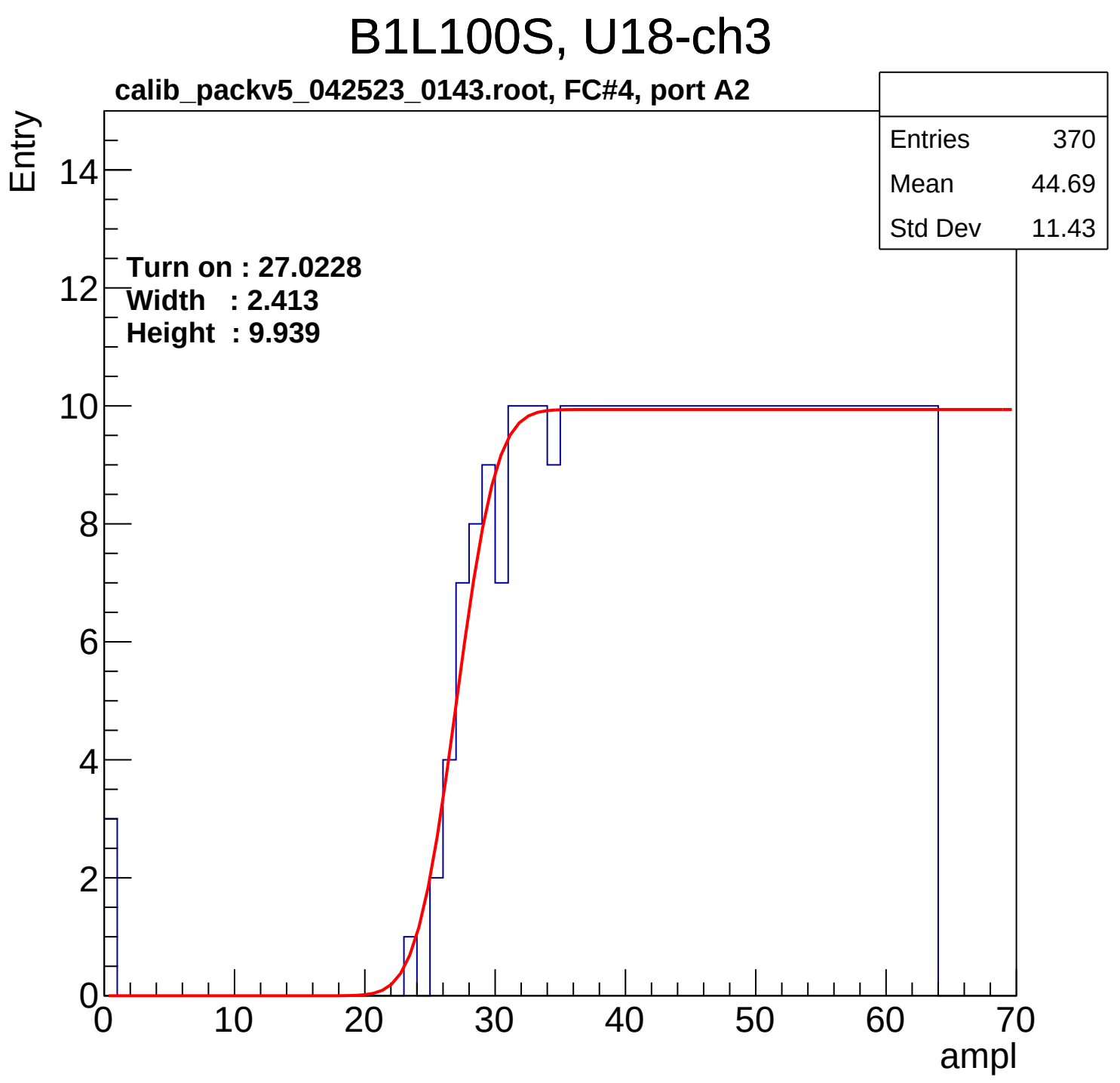
B1L100S, U18-ch3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 370
Mean 44.69
Std Dev 11.43
Turn on : 27.0228
Width : 2.413
Height : 9.939
Entry
ampl
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2
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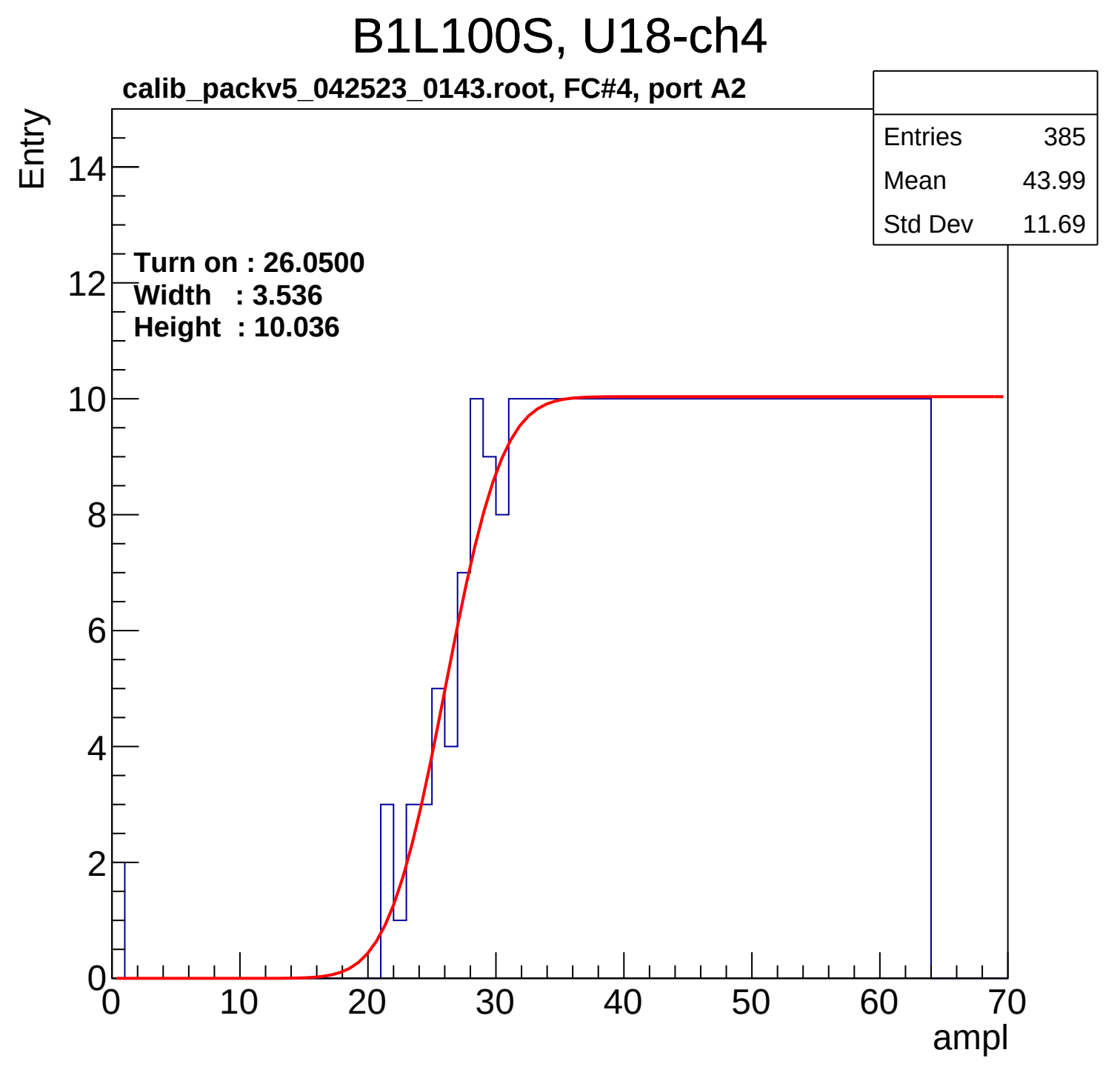
B1L100S, U18-ch4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 385
Mean 43.99
Std Dev 11.69
Turn on : 26.0500
Width : 3.536
Height : 10.036
Entry
ampl
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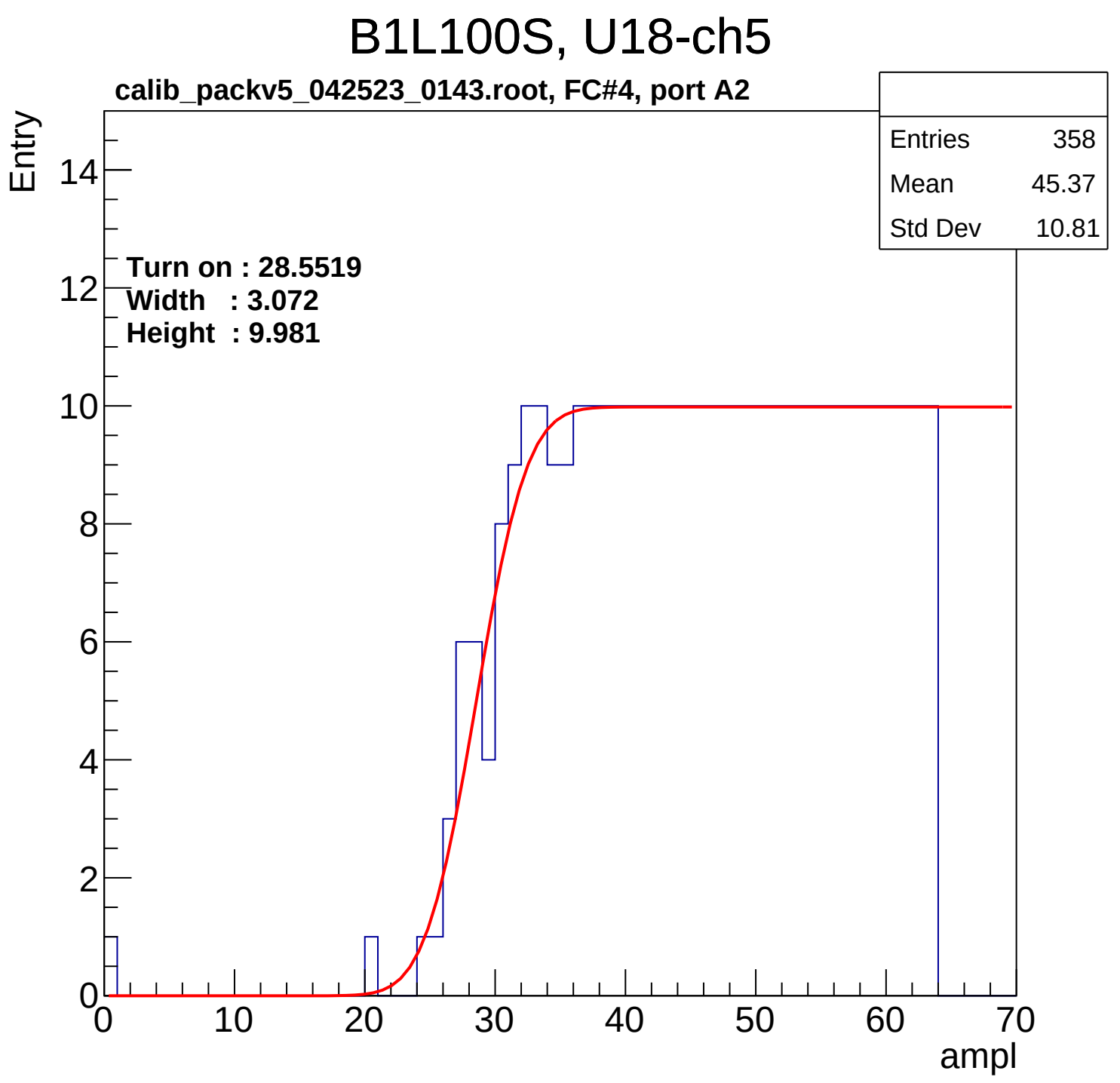
B1L100S, U18-ch5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 358
Mean 45.37
Std Dev 10.81
Turn on : 28.5519
Width : 3.072
Height : 9.981
Entry
ampl
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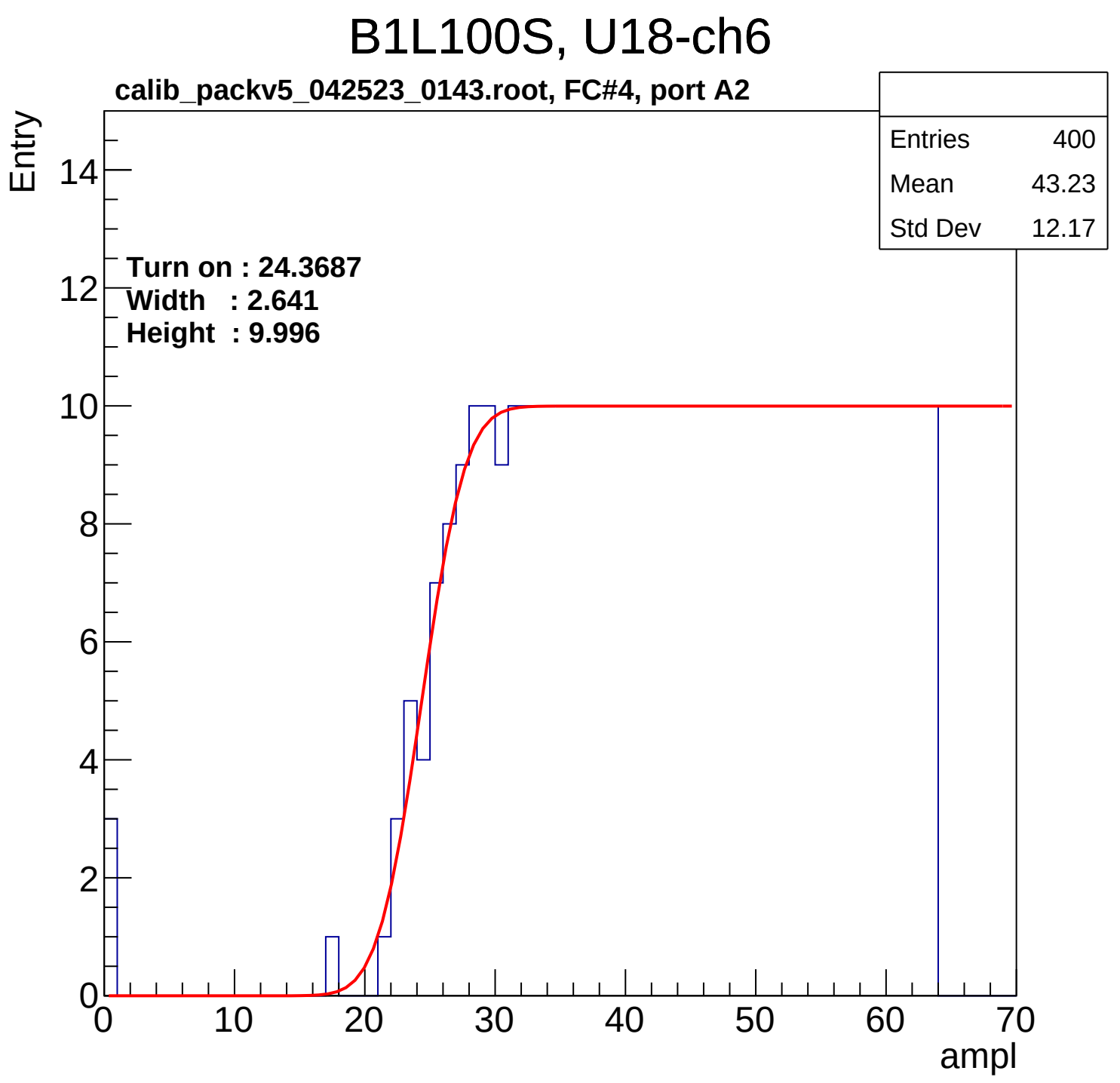
B1L100S, U18-ch6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 400
Mean 43.23
Std Dev 12.17
Turn on : 24.3687
Width : 2.641
Height : 9.996
Entry
ampl
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2
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6
8
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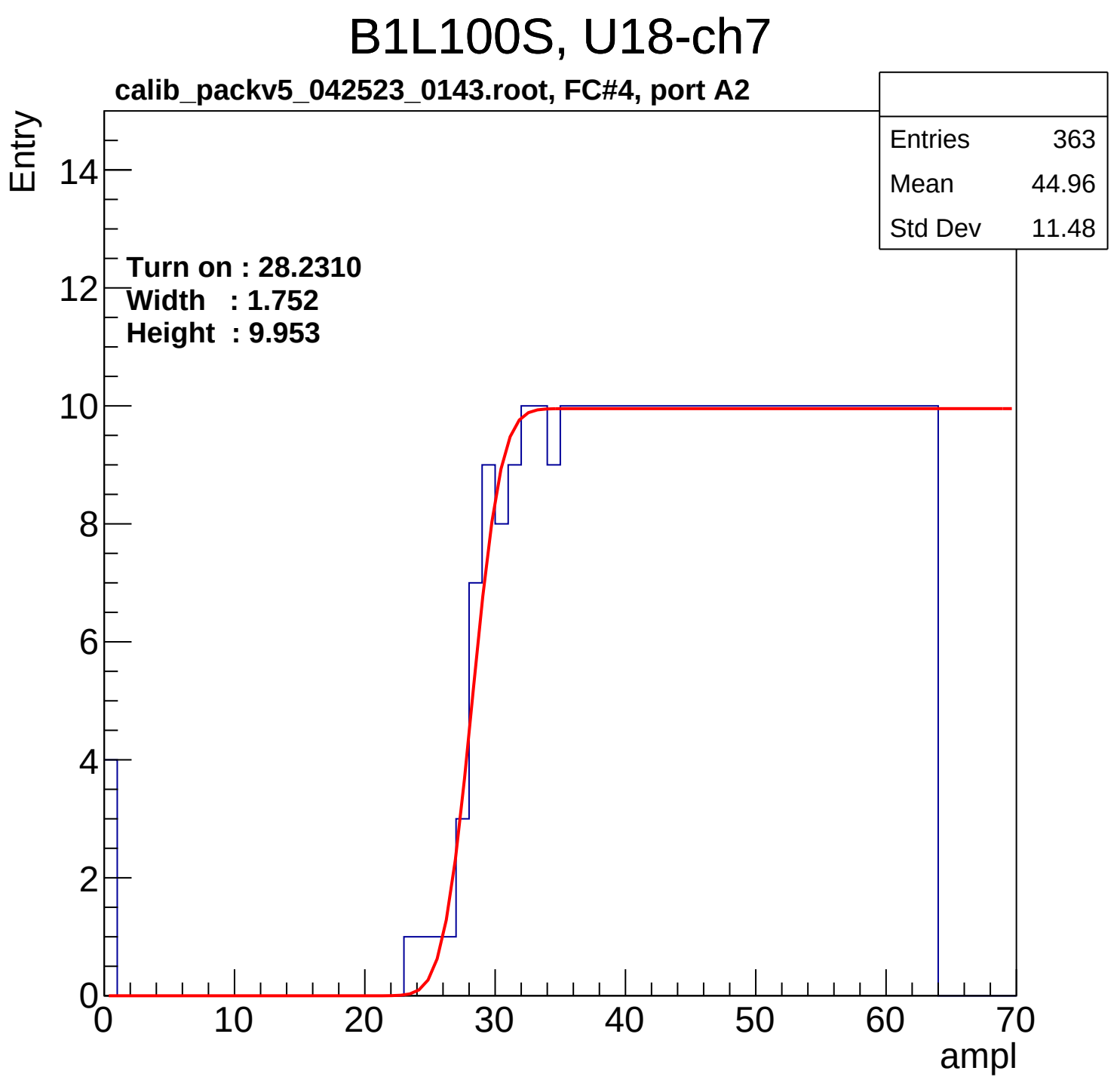
B1L100S, U18-ch7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 363
Mean 44.96
Std Dev 11.48
Turn on : 28.2310
Width : 1.752
Height : 9.953
Entry
ampl
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8
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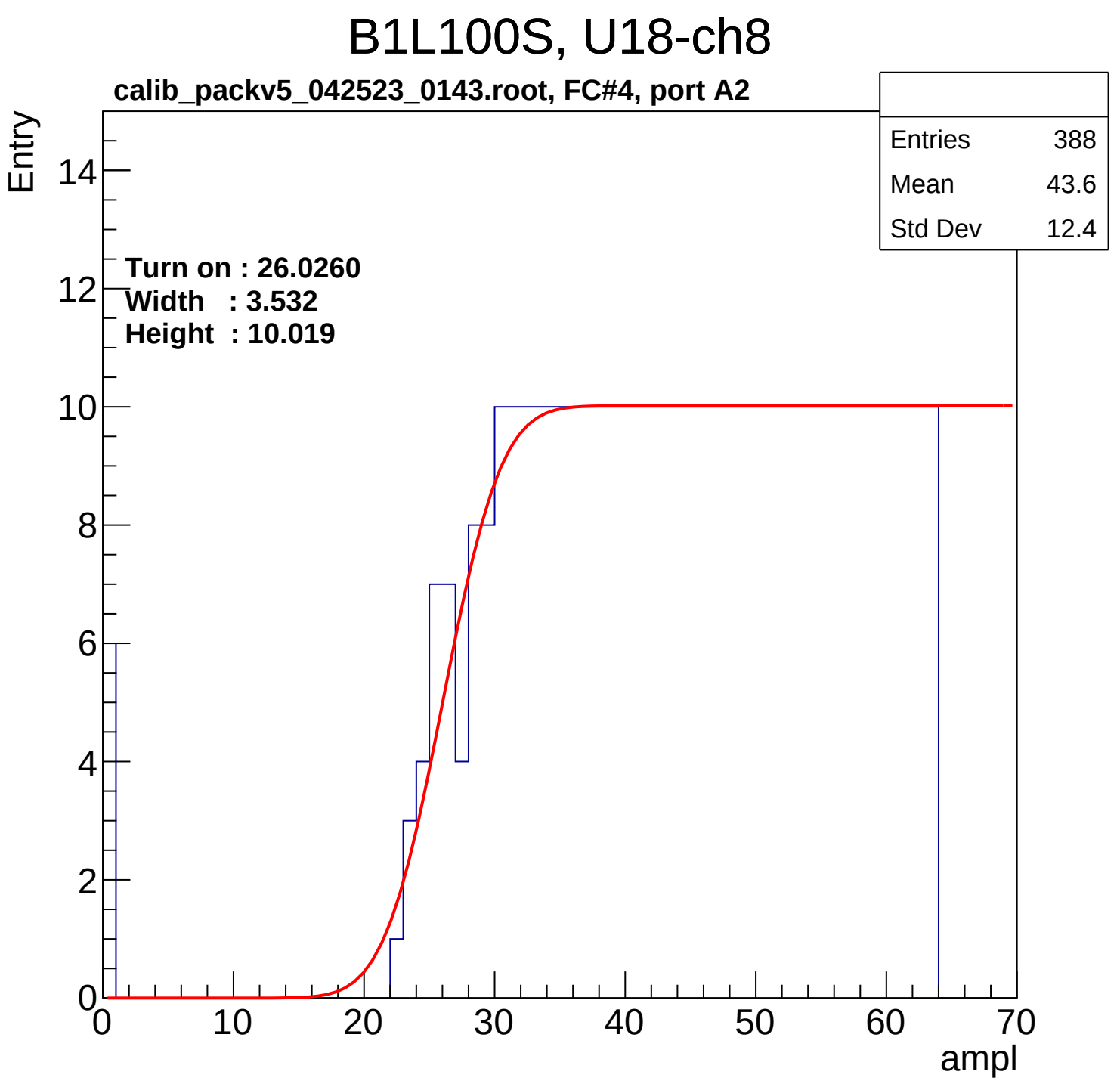
B1L100S, U18-ch8
calib_packv5_042523_0143.root, FC#4, port A2
Entries 388
Mean 43.6
Std Dev 12.4
Turn on : 26.0260
Width : 3.532
Height : 10.019
Entry
ampl
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8
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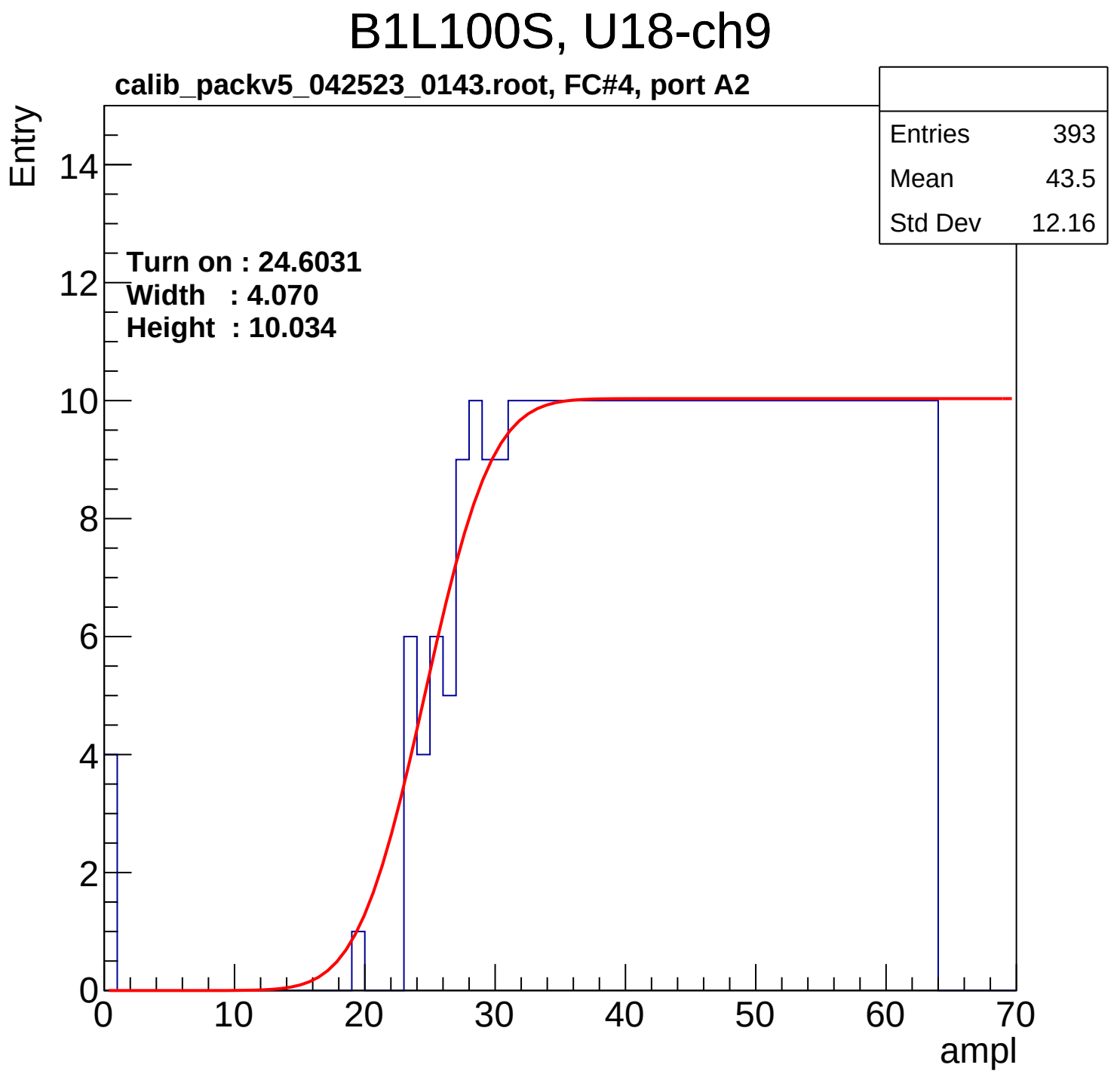
B1L100S, U18-ch9
calib_packv5_042523_0143.root, FC#4, port A2
Entries 393
Mean 43.5
Std Dev 12.16
Turn on : 24.6031
Width : 4.070
Height : 10.034
Entry
ampl
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6
8
10
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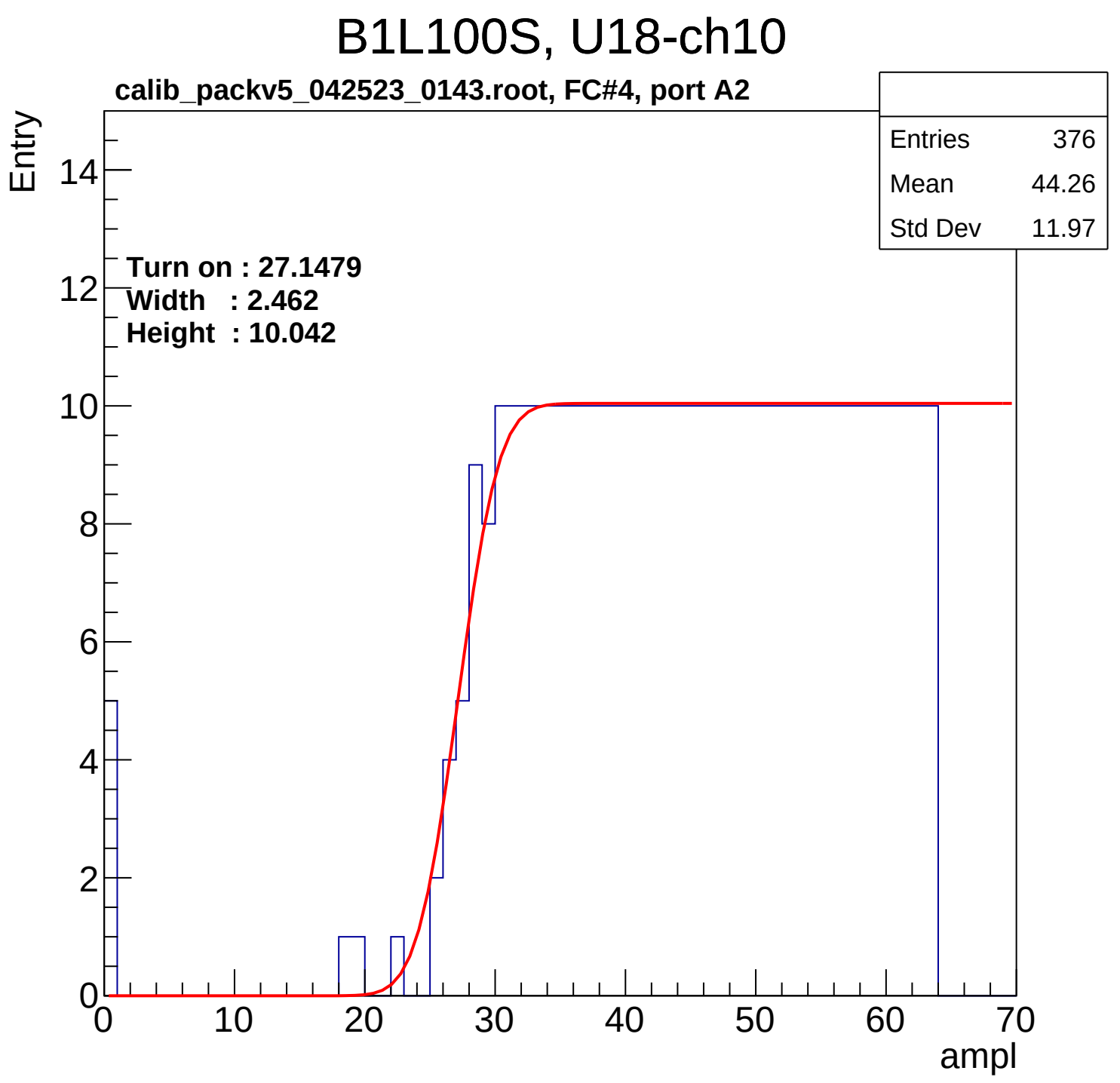
B1L100S, U18-ch10
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.26
Std Dev 11.97
Turn on : 27.1479
Width : 2.462
Height : 10.042
Entry
ampl
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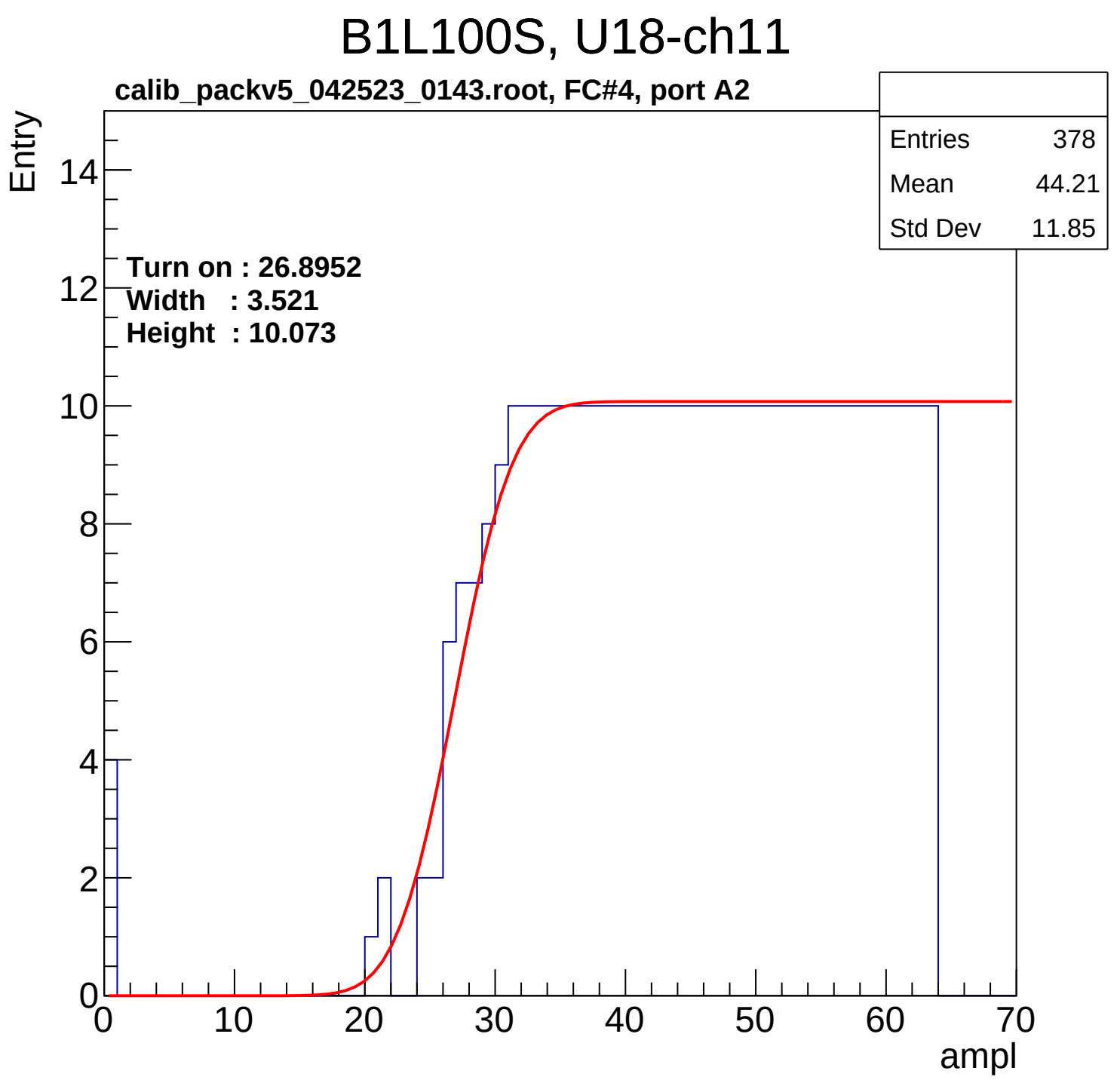
B1L100S, U18-ch11
calib_packv5_042523_0143.root, FC#4, port A2
Entries 378
Mean 44.21
Std Dev 11.85
Turn on : 26.8952
Width : 3.521
Height : 10.073
Entry
ampl
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8
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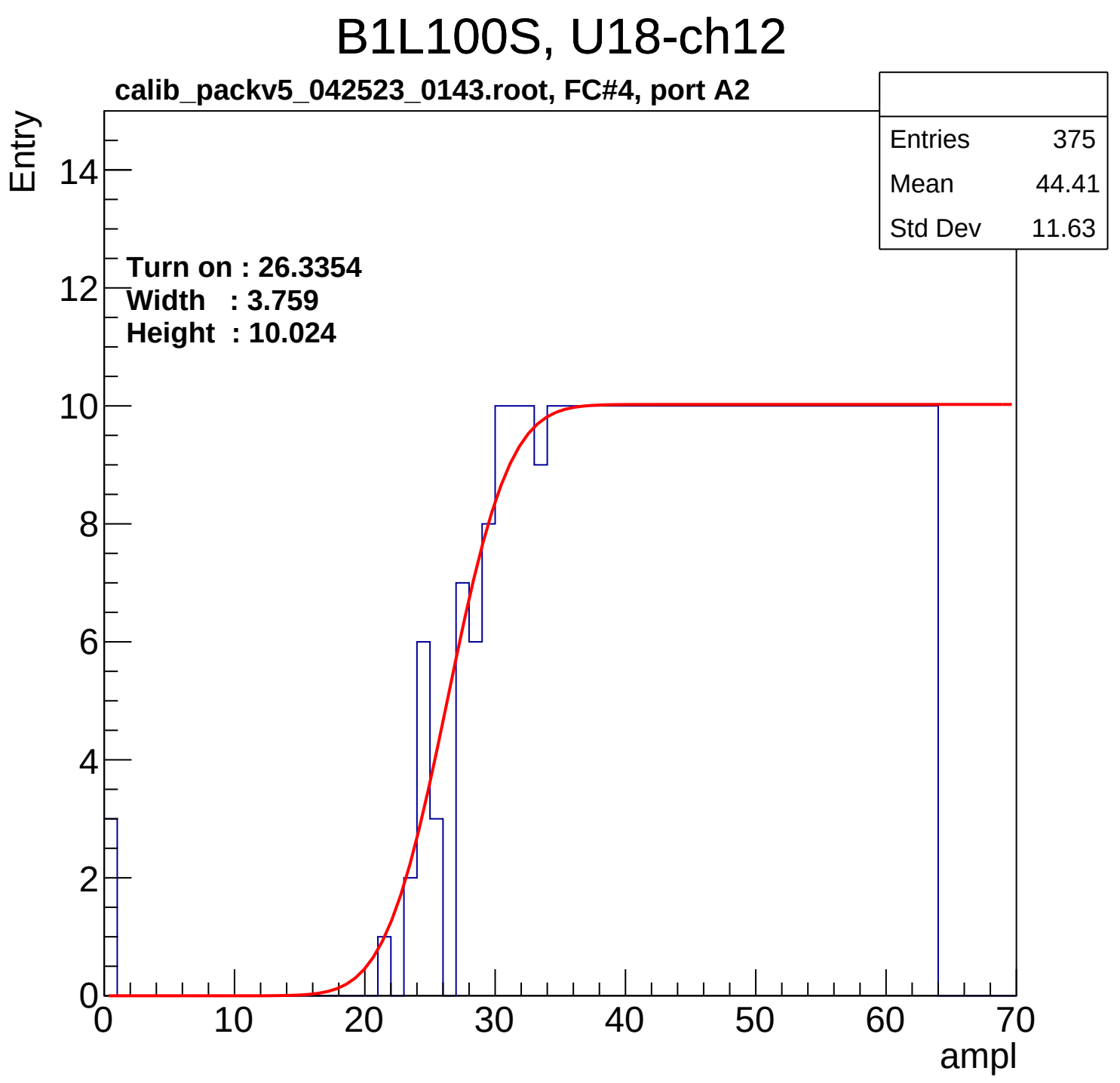
B1L100S, U18-ch12
calib_packv5_042523_0143.root, FC#4, port A2
Entries 375
Mean 44.41
Std Dev 11.63
Turn on : 26.3354
Width : 3.759
Height : 10.024
Entry
ampl
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8
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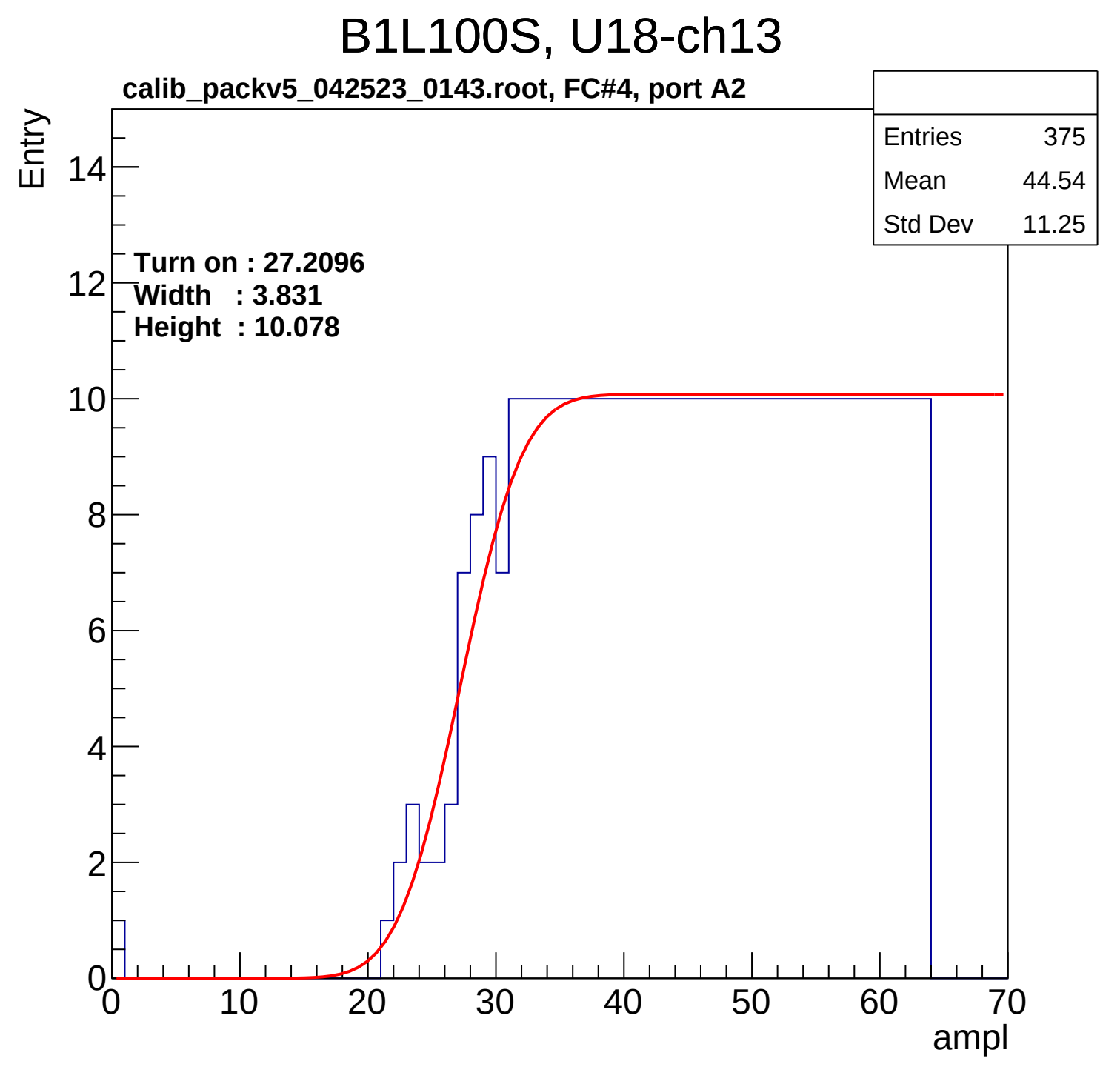
B1L100S, U18-ch13
calib_packv5_042523_0143.root, FC#4, port A2
Entries 375
Mean 44.54
Std Dev 11.25
Turn on : 27.2096
Width : 3.831
Height : 10.078
Entry
ampl
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6
8
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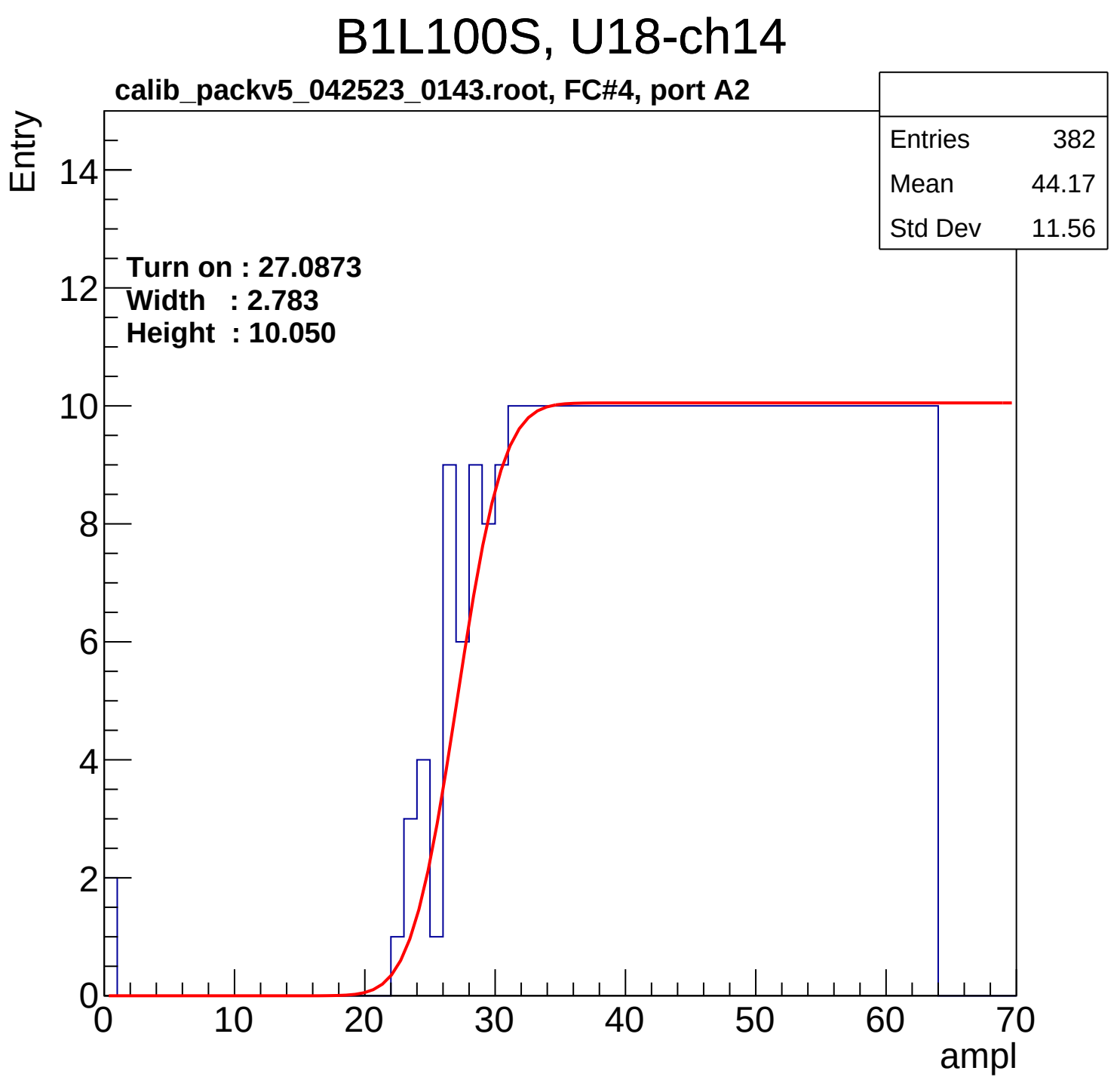
B1L100S, U18-ch14
calib_packv5_042523_0143.root, FC#4, port A2
Entries 382
Mean 44.17
Std Dev 11.56
Turn on : 27.0873
Width : 2.783
Height : 10.050
Entry
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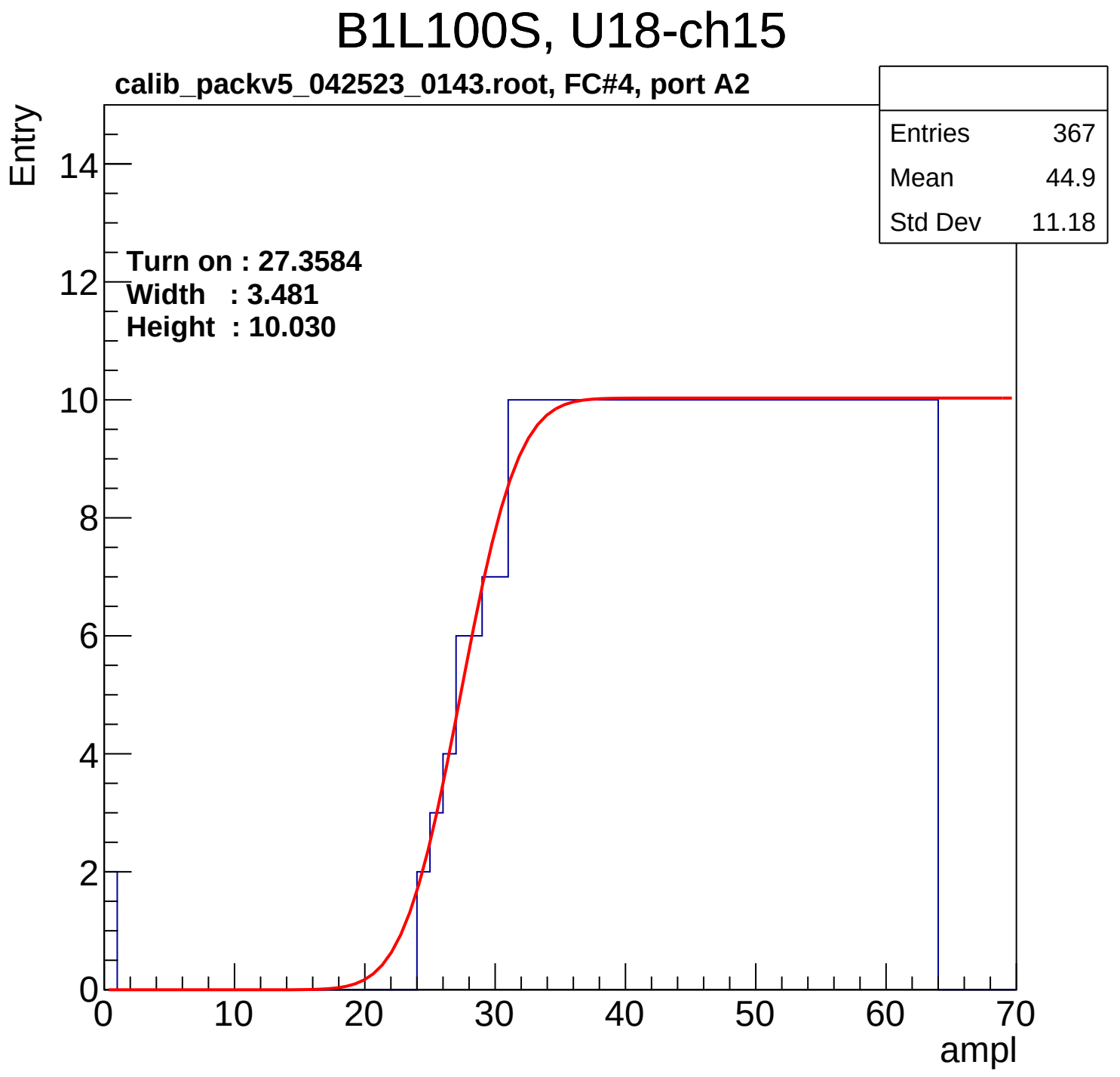
B1L100S, U18-ch15
calib_packv5_042523_0143.root, FC#4, port A2
Entries 367
Mean 44.9
Std Dev 11.18
Turn on : 27.3584
Width : 3.481
Height : 10.030
Entry
ampl
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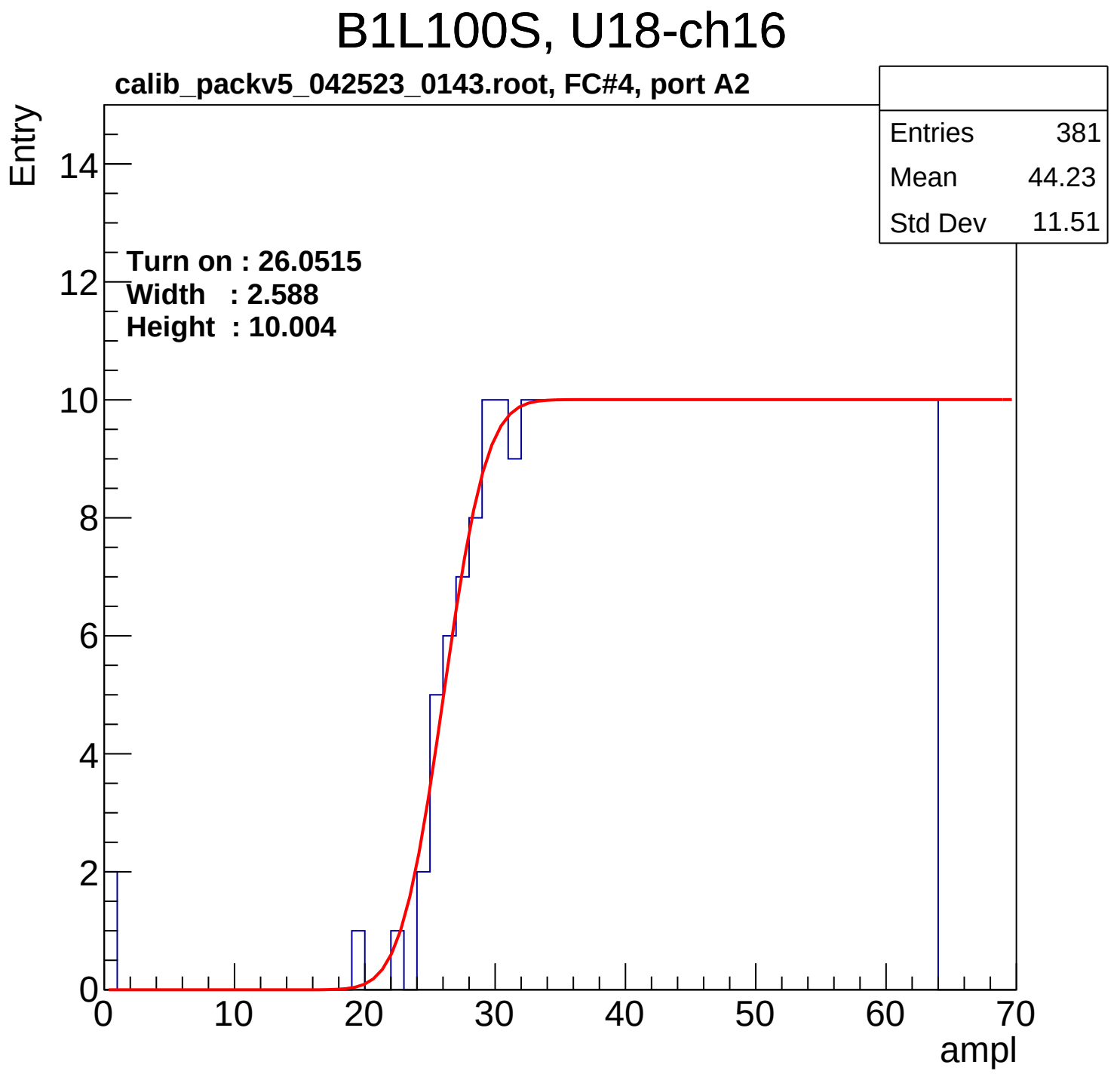
B1L100S, U18-ch16
calib_packv5_042523_0143.root, FC#4, port A2
Entries 381
Mean 44.23
Std Dev 11.51
Turn on : 26.0515
Width : 2.588
Height : 10.004
Entry
ampl
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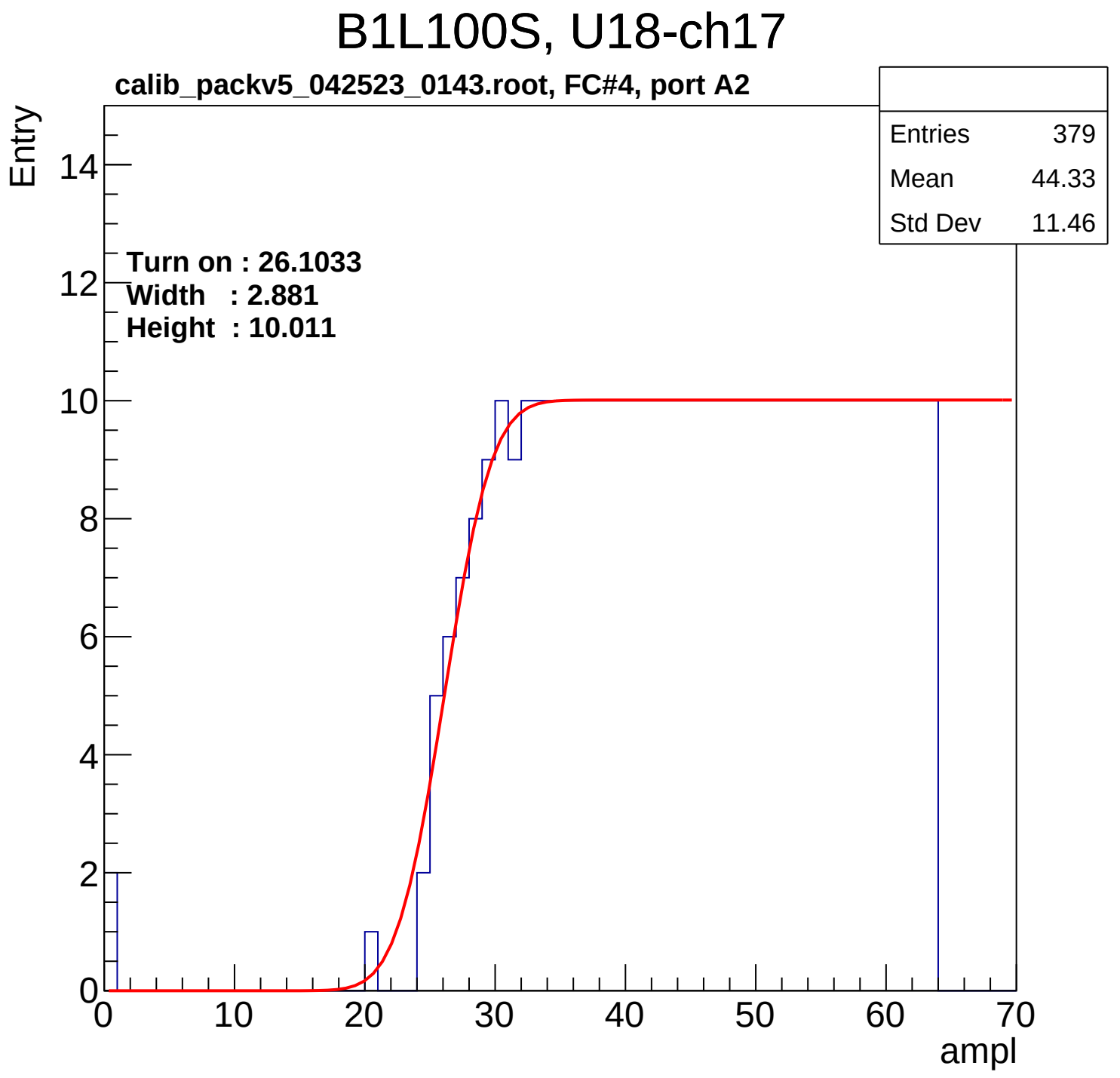
B1L100S, U18-ch17
calib_packv5_042523_0143.root, FC#4, port A2
Entries 379
Mean 44.33
Std Dev 11.46
Turn on : 26.1033
Width : 2.881
Height : 10.011
Entry
ampl
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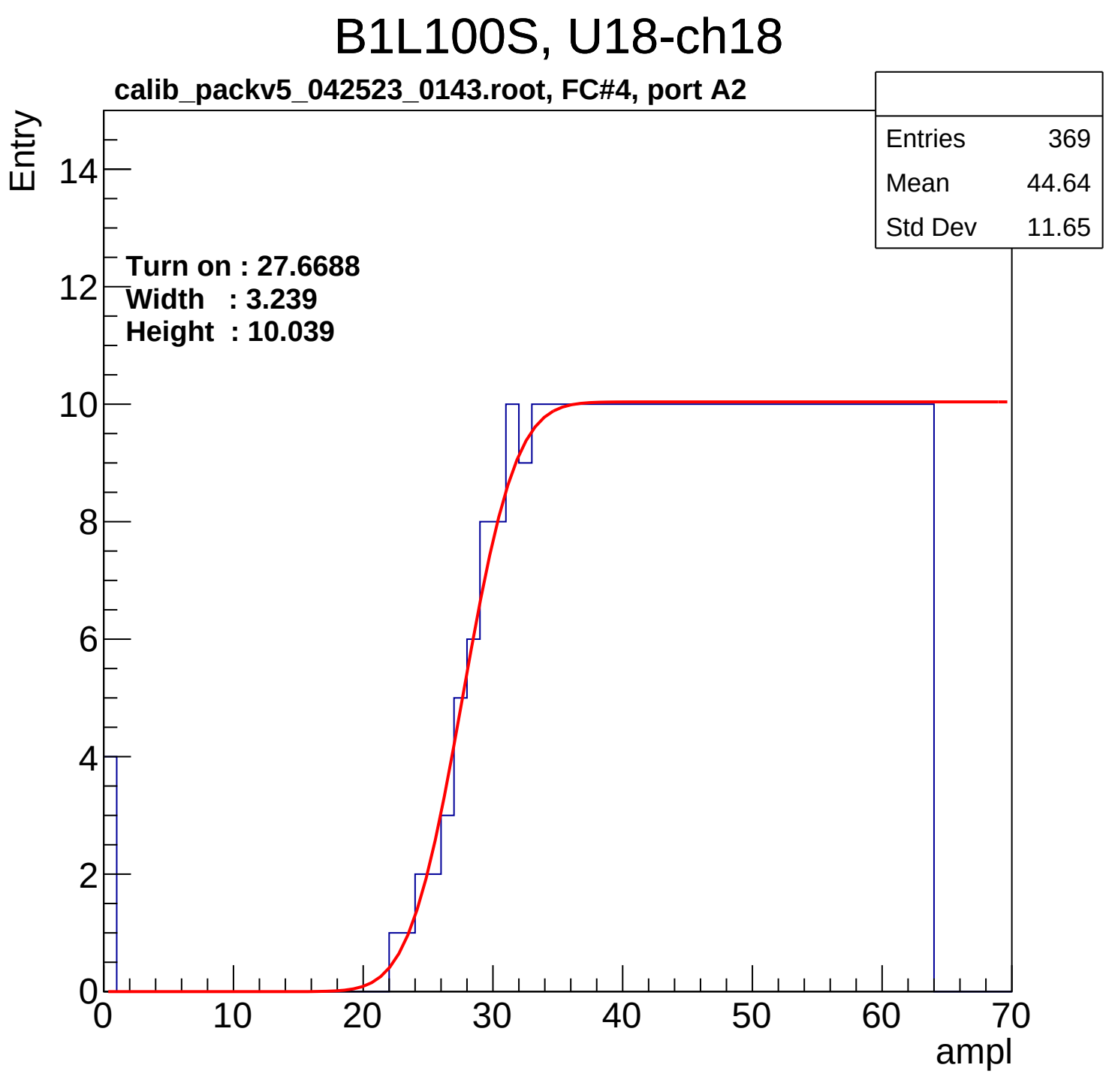
B1L100S, U18-ch18
calib_packv5_042523_0143.root, FC#4, port A2
Entries 369
Mean 44.64
Std Dev 11.65
Turn on : 27.6688
Width : 3.239
Height : 10.039
Entry
ampl
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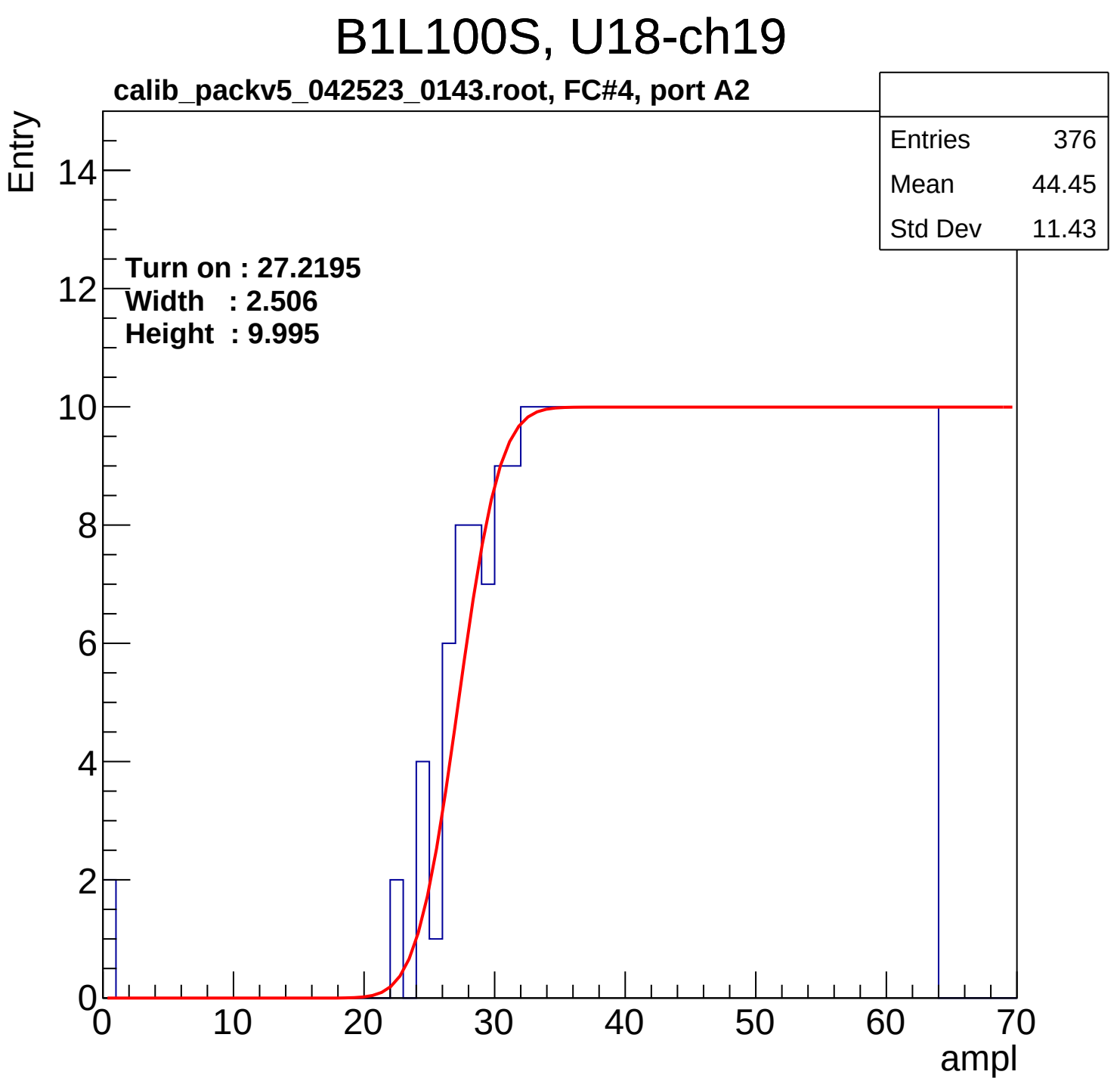
B1L100S, U18-ch19
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.45
Std Dev 11.43
Turn on : 27.2195
Width : 2.506
Height : 9.995
Entry
ampl
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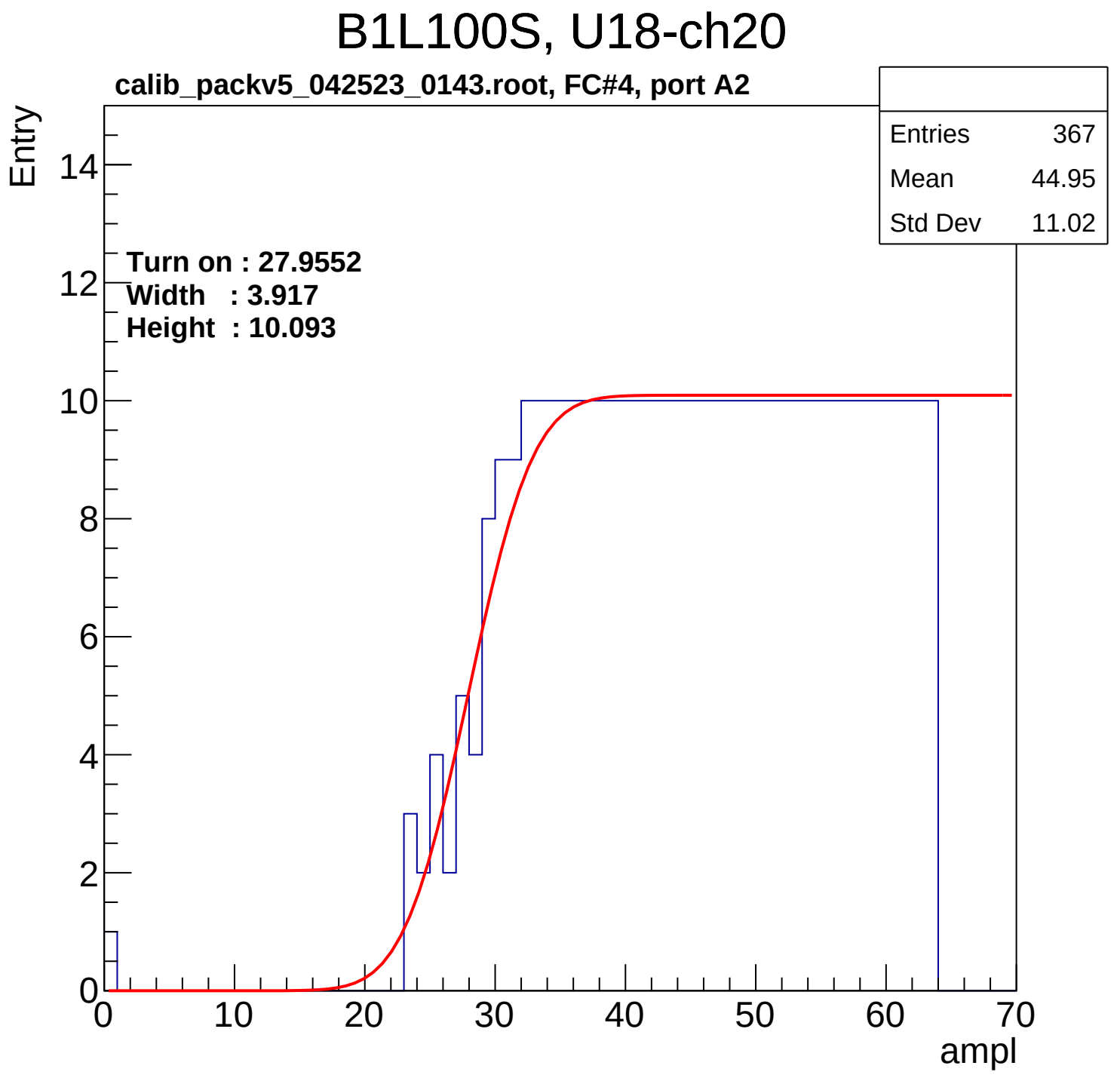
B1L100S, U18-ch20
calib_packv5_042523_0143.root, FC#4, port A2
Entries 367
Mean 44.95
Std Dev 11.02
Turn on : 27.9552
Width : 3.917
Height : 10.093
Entry
ampl
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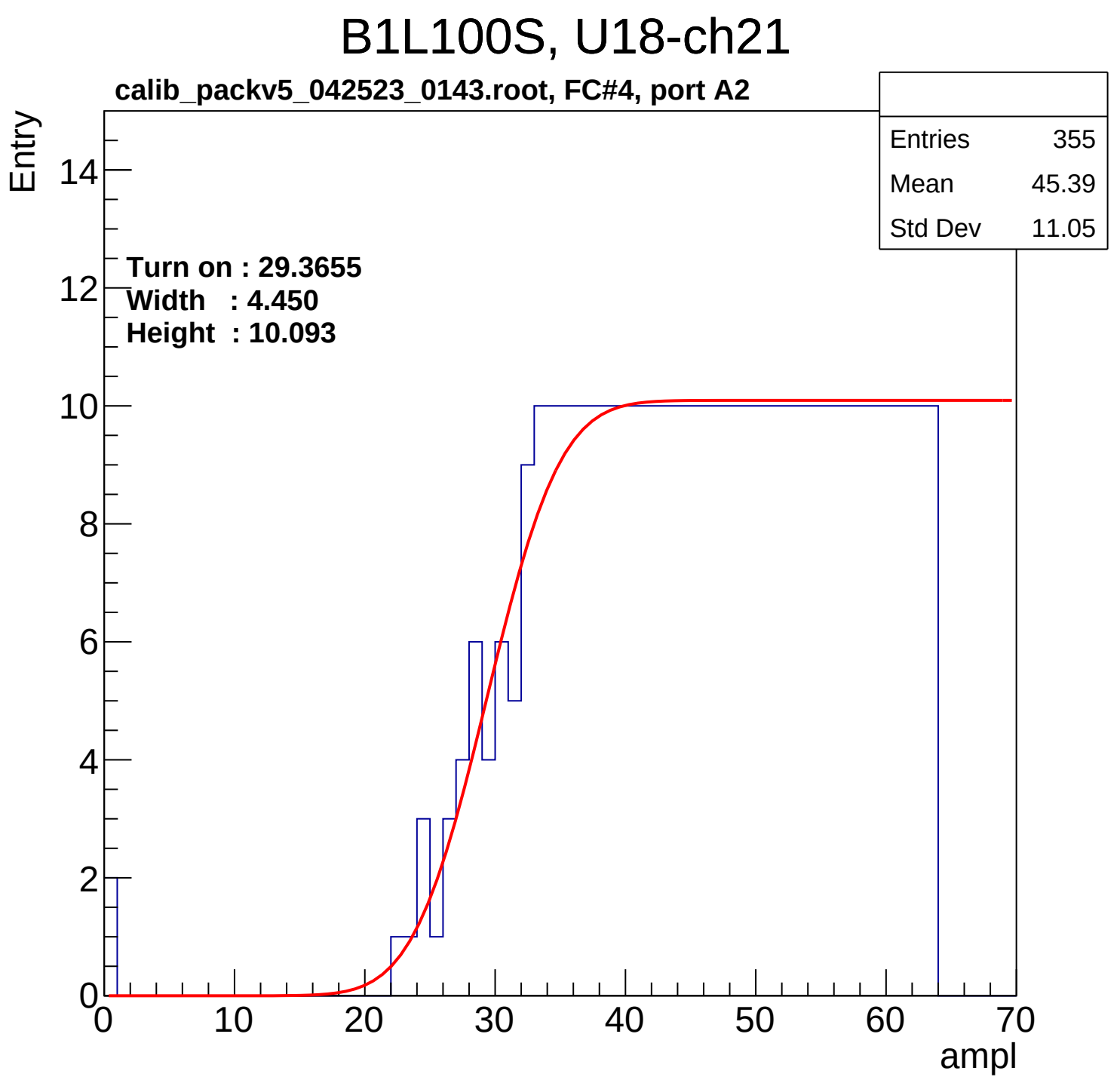
B1L100S, U18-ch21
calib_packv5_042523_0143.root, FC#4, port A2
Entries 355
Mean 45.39
Std Dev 11.05
Turn on : 29.3655
Width : 4.450
Height : 10.093
Entry
ampl
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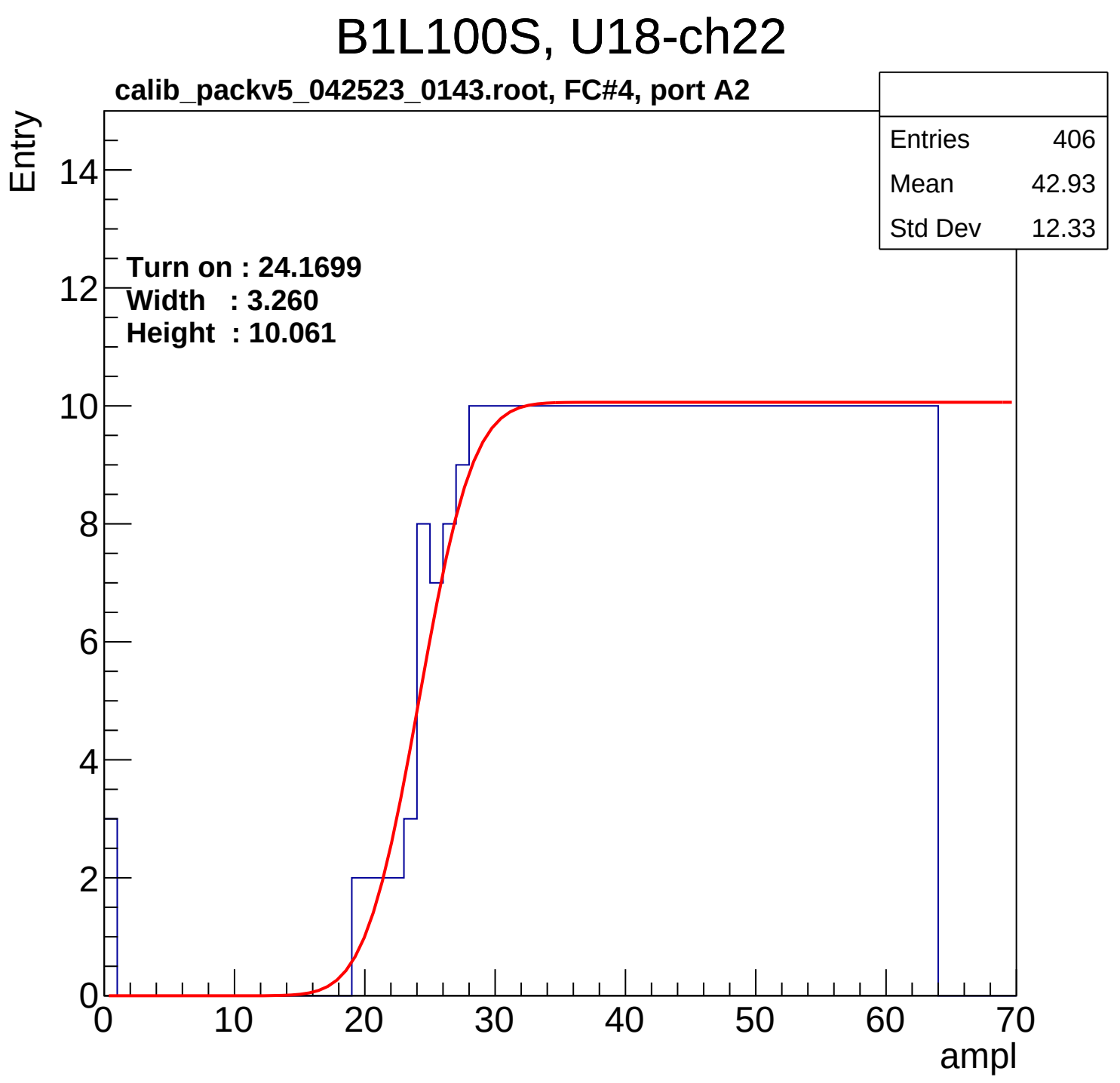
B1L100S, U18-ch22
calib_packv5_042523_0143.root, FC#4, port A2
Entries 406
Mean 42.93
Std Dev 12.33
Turn on : 24.1699
Width : 3.260
Height : 10.061
Entry
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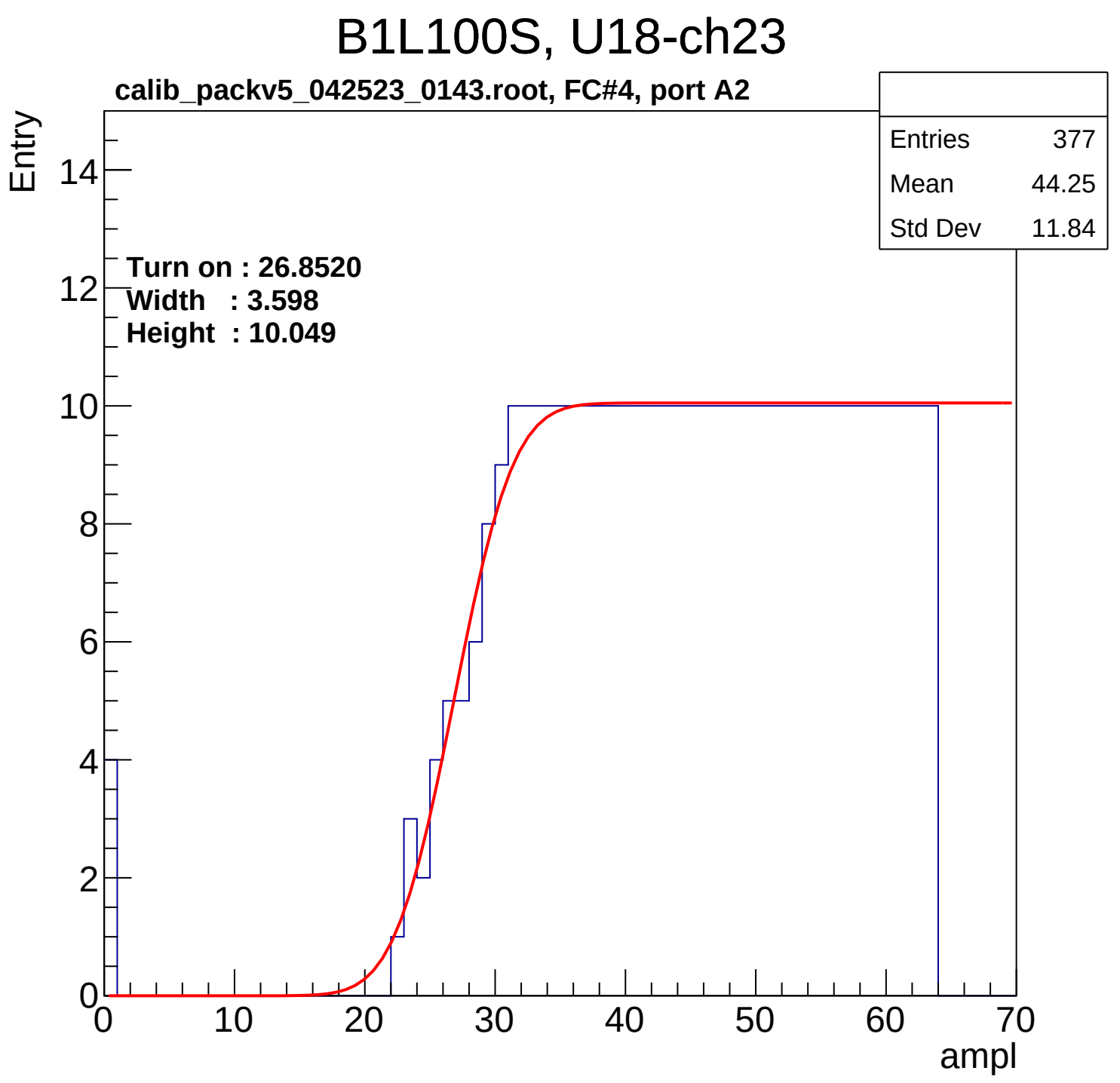
B1L100S, U18-ch23
calib_packv5_042523_0143.root, FC#4, port A2
Entries 377
Mean 44.25
Std Dev 11.84
Turn on : 26.8520
Width : 3.598
Height : 10.049
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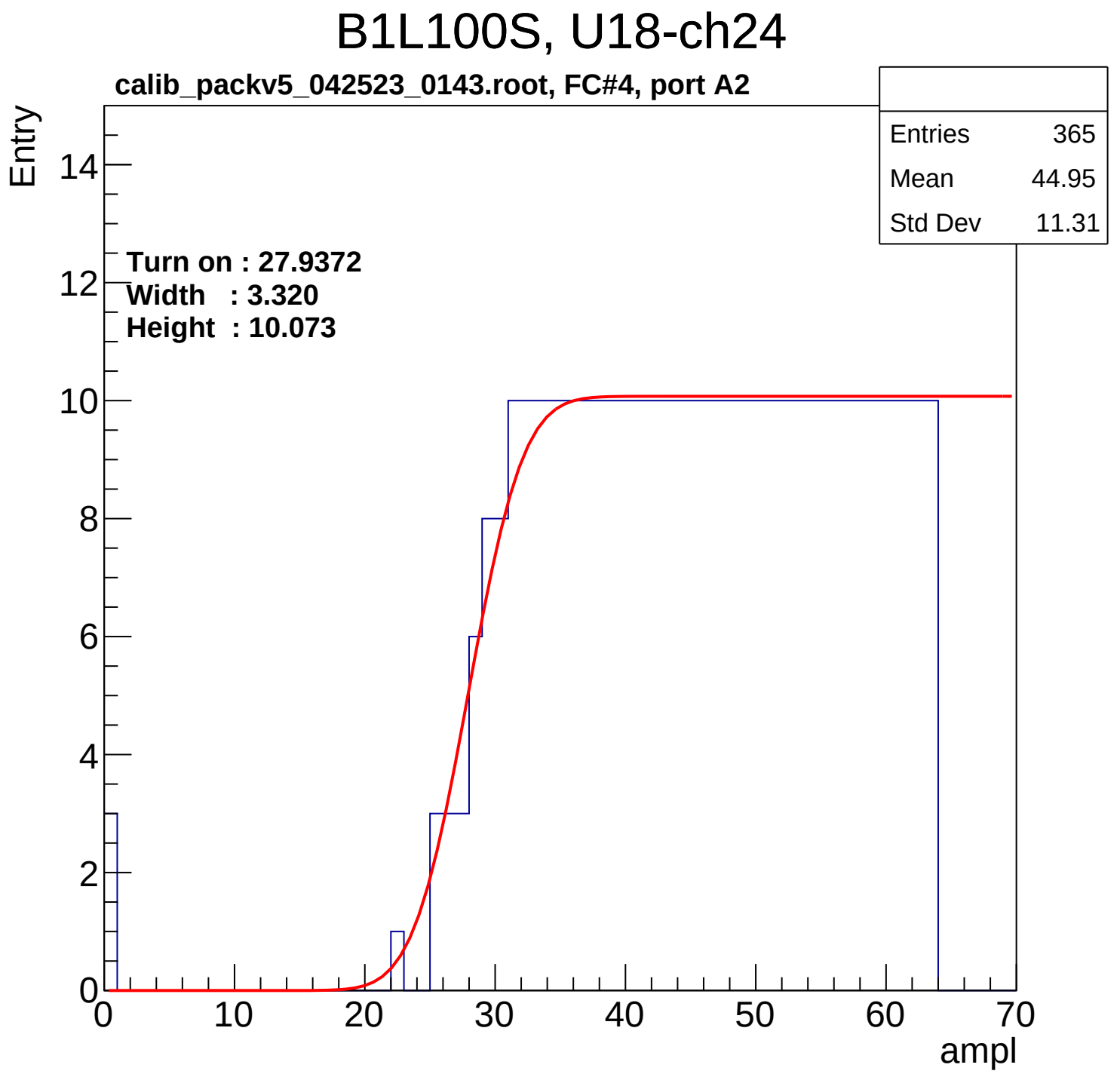
B1L100S, U18-ch24
calib_packv5_042523_0143.root, FC#4, port A2
Entries 365
Mean 44.95
Std Dev 11.31
Turn on : 27.9372
Width : 3.320
Height : 10.073
Entry
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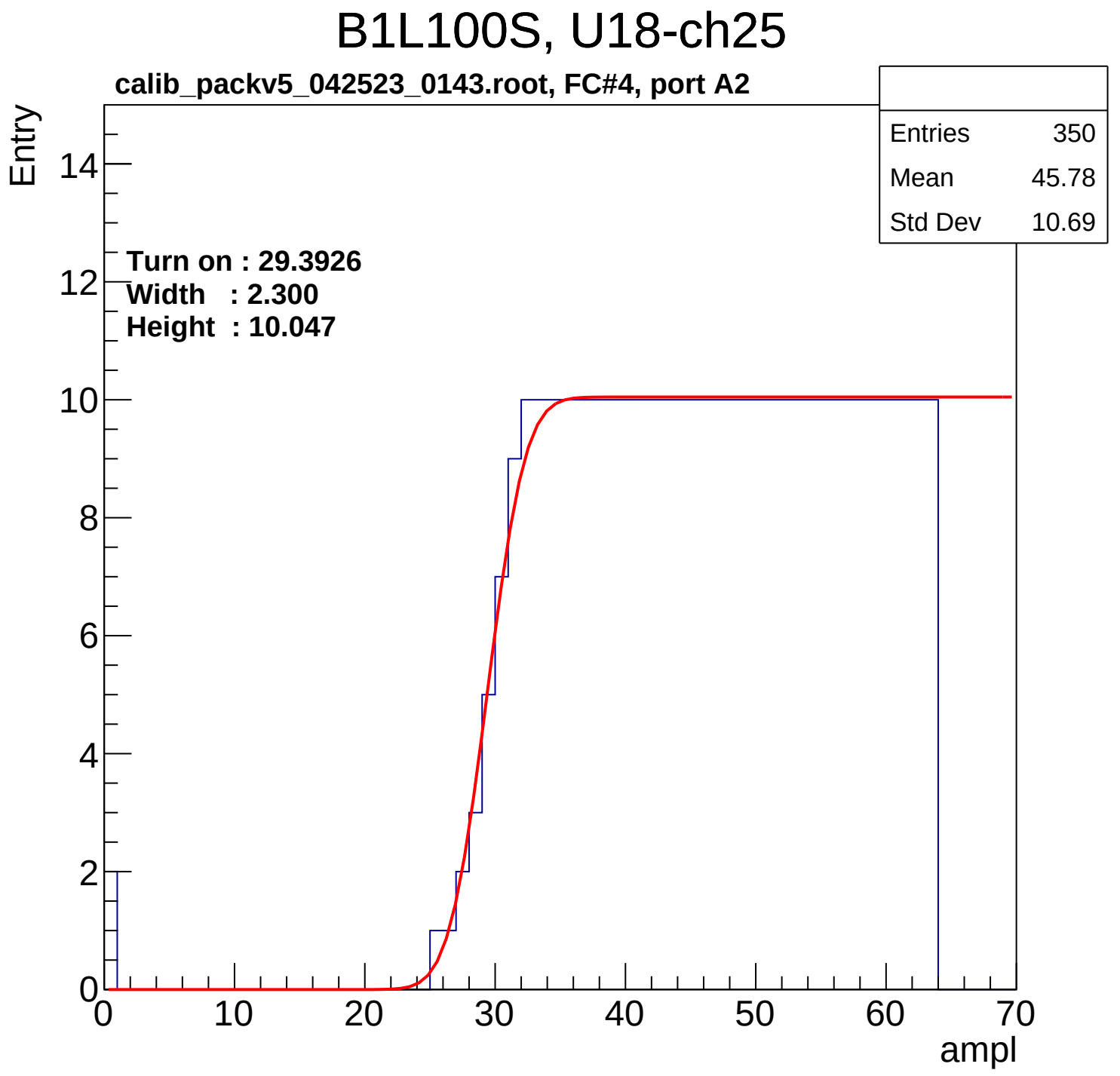
B1L100S, U18-ch25
calib_packv5_042523_0143.root, FC#4, port A2
Entries 350
Mean 45.78
Std Dev 10.69
Turn on : 29.3926
Width : 2.300
Height : 10.047
Entry
ampl
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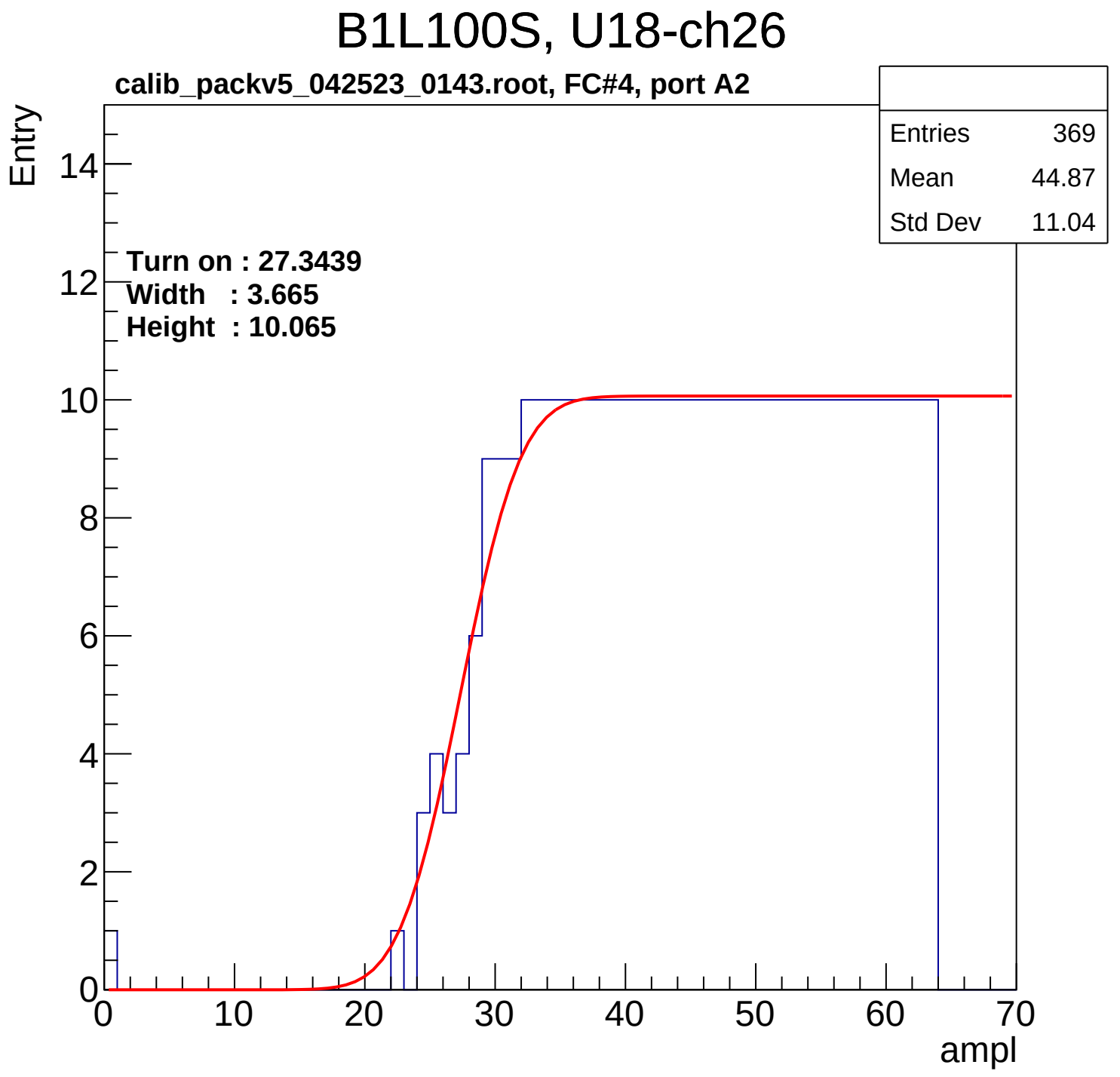
B1L100S, U18-ch26
calib_packv5_042523_0143.root, FC#4, port A2
Entries 369
Mean 44.87
Std Dev 11.04
Turn on : 27.3439
Width : 3.665
Height : 10.065
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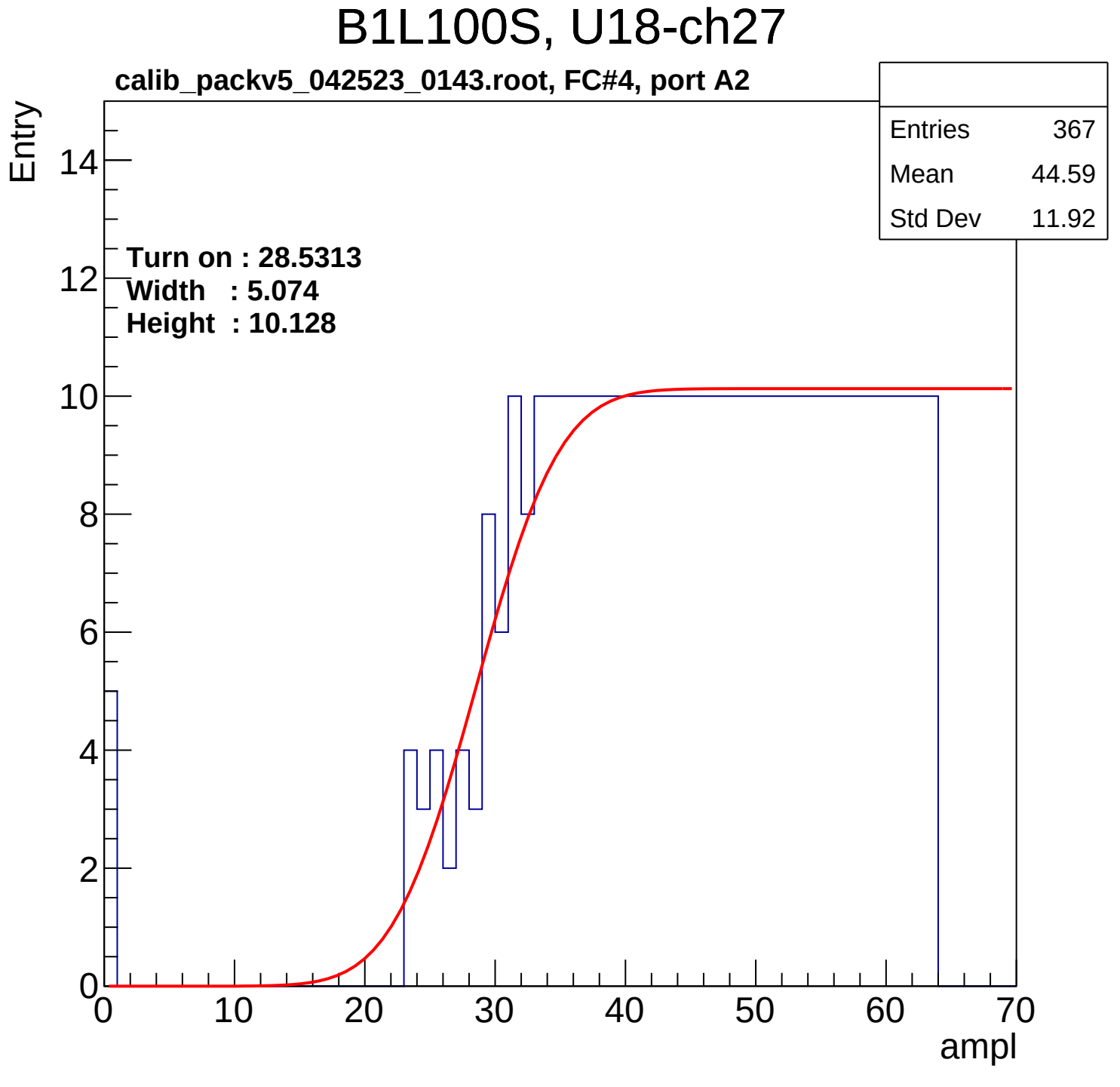
B1L100S, U18-ch27
calib_packv5_042523_0143.root, FC#4, port A2
Entries 367
Mean 44.59
Std Dev 11.92
Turn on : 28.5313
Width : 5.074
Height : 10.128
Entry
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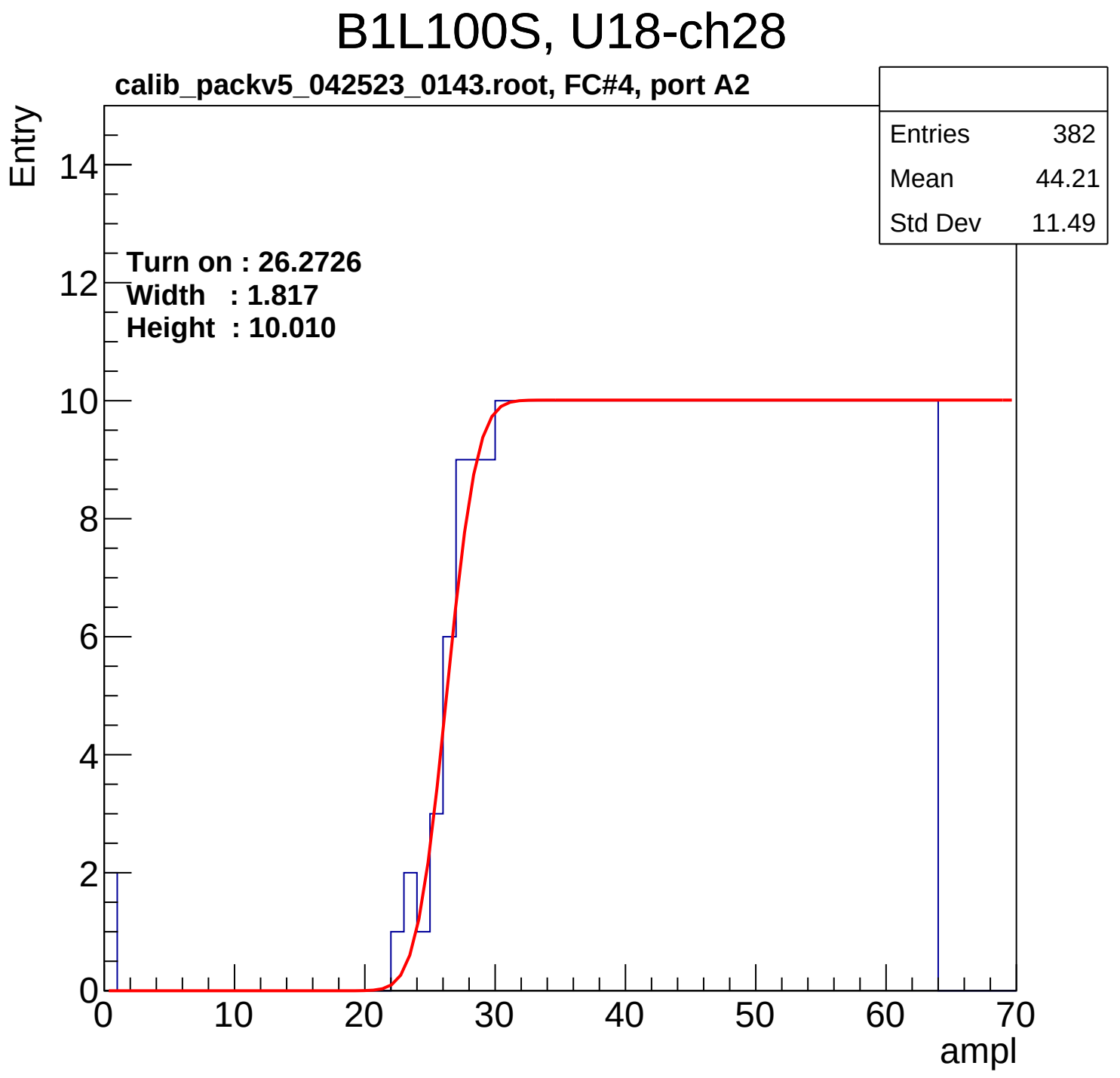
B1L100S, U18-ch28
calib_packv5_042523_0143.root, FC#4, port A2
Entries 382
Mean 44.21
Std Dev 11.49
Turn on : 26.2726
Width : 1.817
Height : 10.010
Entry
ampl
0
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4
6
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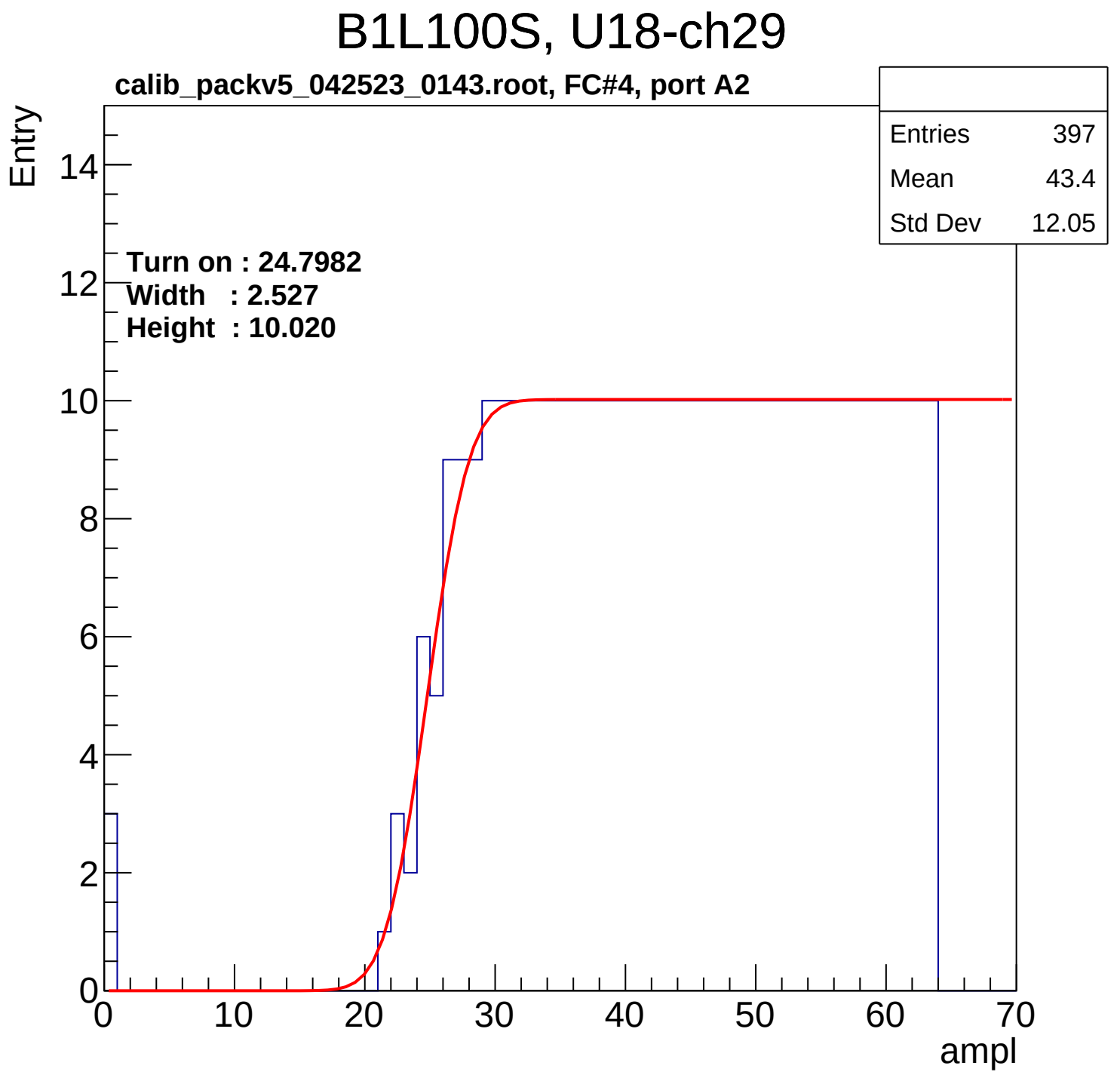
B1L100S, U18-ch29
calib_packv5_042523_0143.root, FC#4, port A2
Entries 397
Mean 43.4
Std Dev 12.05
Turn on : 24.7982
Width : 2.527
Height : 10.020
Entry
ampl
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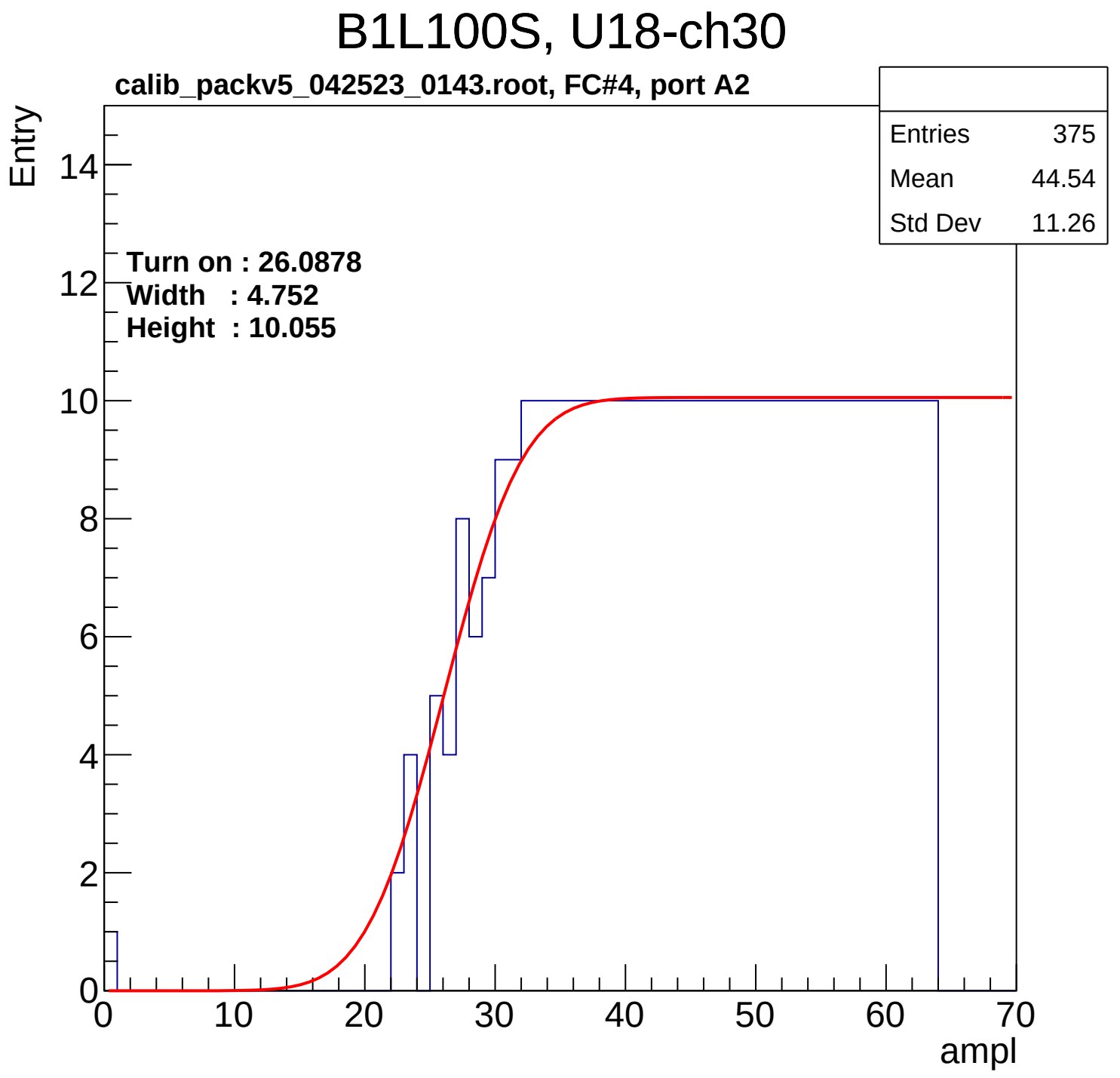
B1L100S, U18-ch30
calib_packv5_042523_0143.root, FC#4, port A2
Entries 375
Mean 44.54
Std Dev 11.26
Turn on : 26.0878
Width : 4.752
Height : 10.055
Entry
ampl
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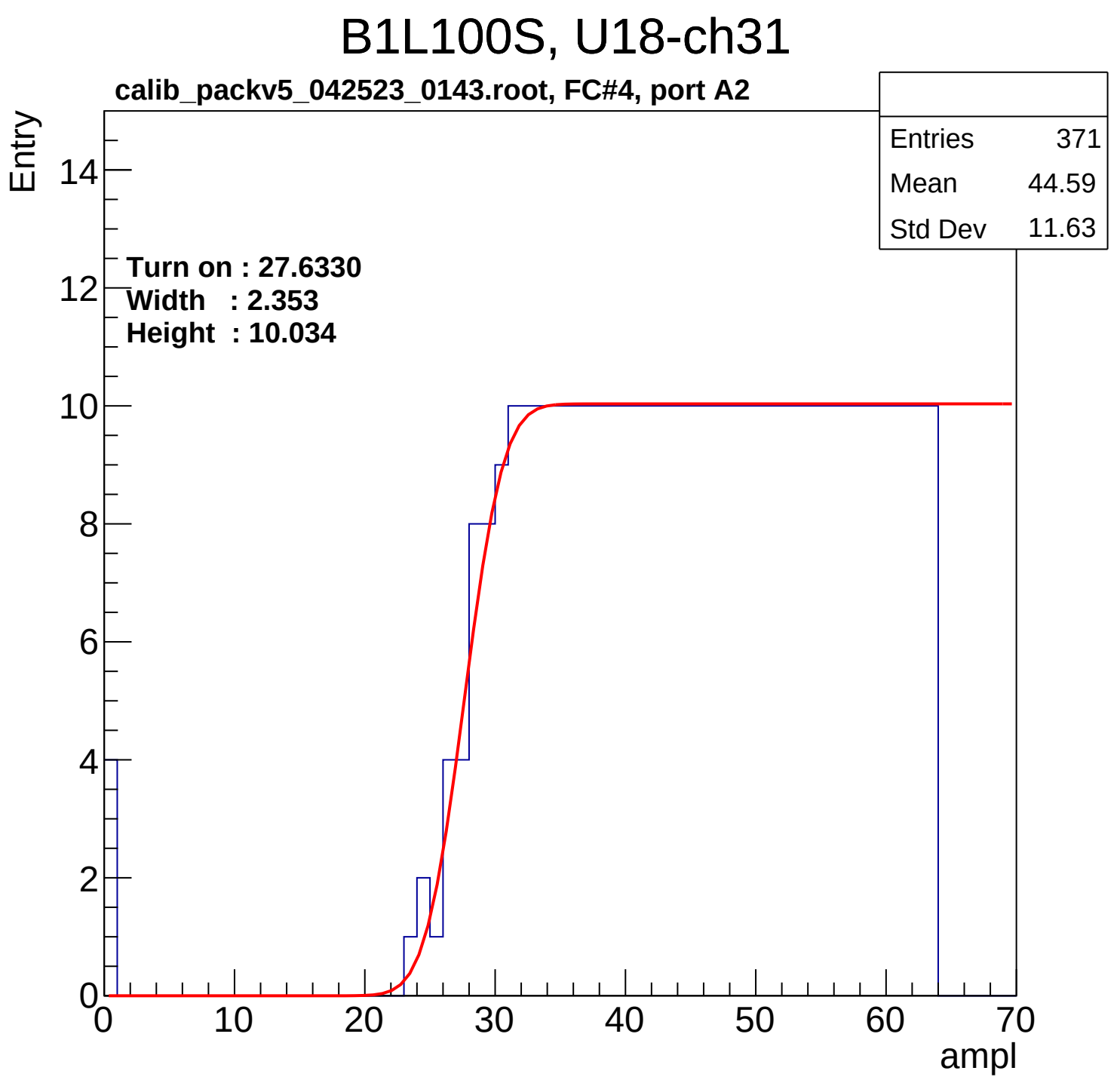
B1L100S, U18-ch31
calib_packv5_042523_0143.root, FC#4, port A2
Entries 371
Mean 44.59
Std Dev 11.63
Turn on : 27.6330
Width : 2.353
Height : 10.034
Entry
ampl
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4
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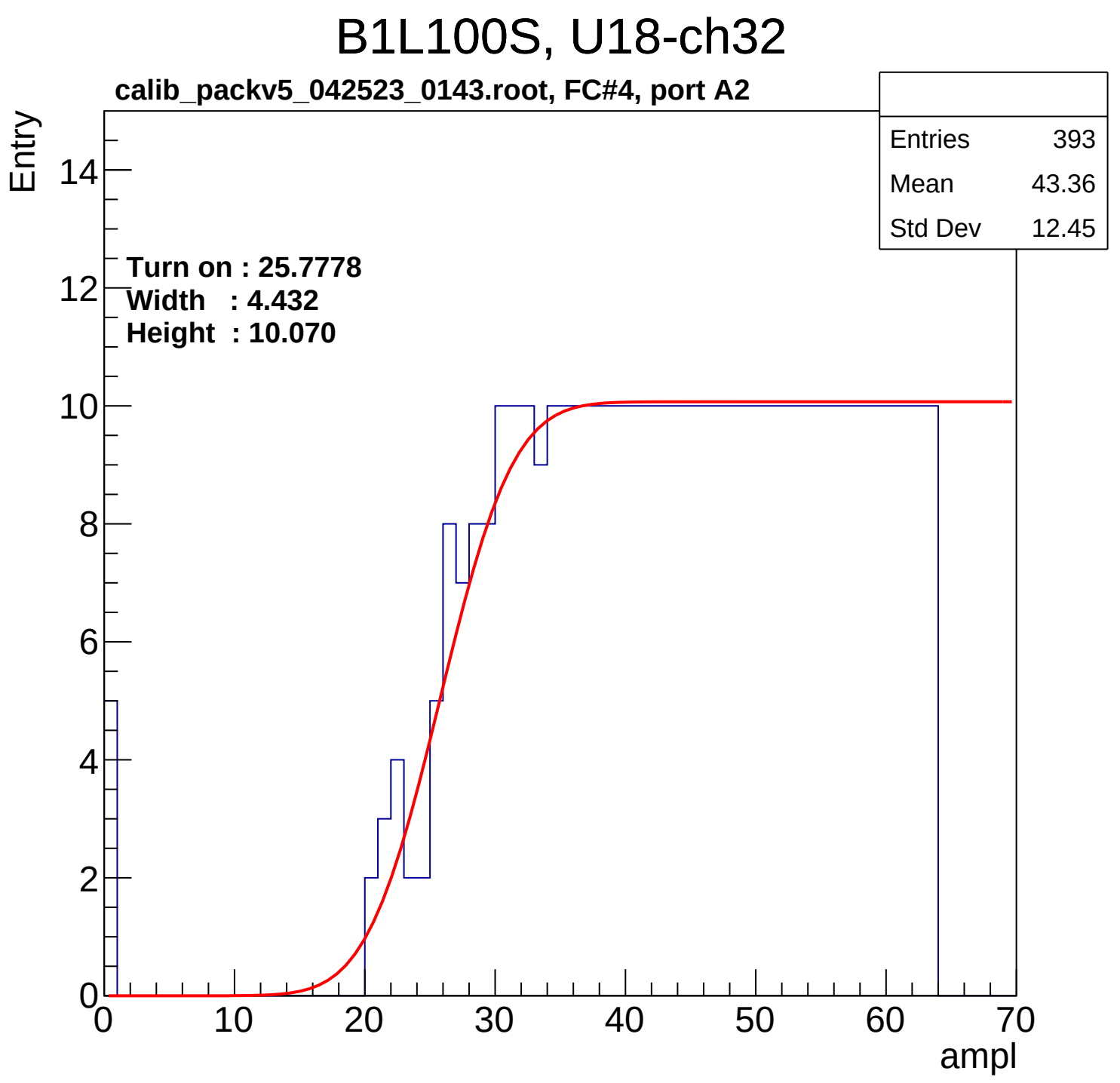
B1L100S, U18-ch32
calib_packv5_042523_0143.root, FC#4, port A2
Entries 393
Mean 43.36
Std Dev 12.45
Turn on : 25.7778
Width : 4.432
Height : 10.070
Entry
ampl
0
2
4
6
8
10
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0
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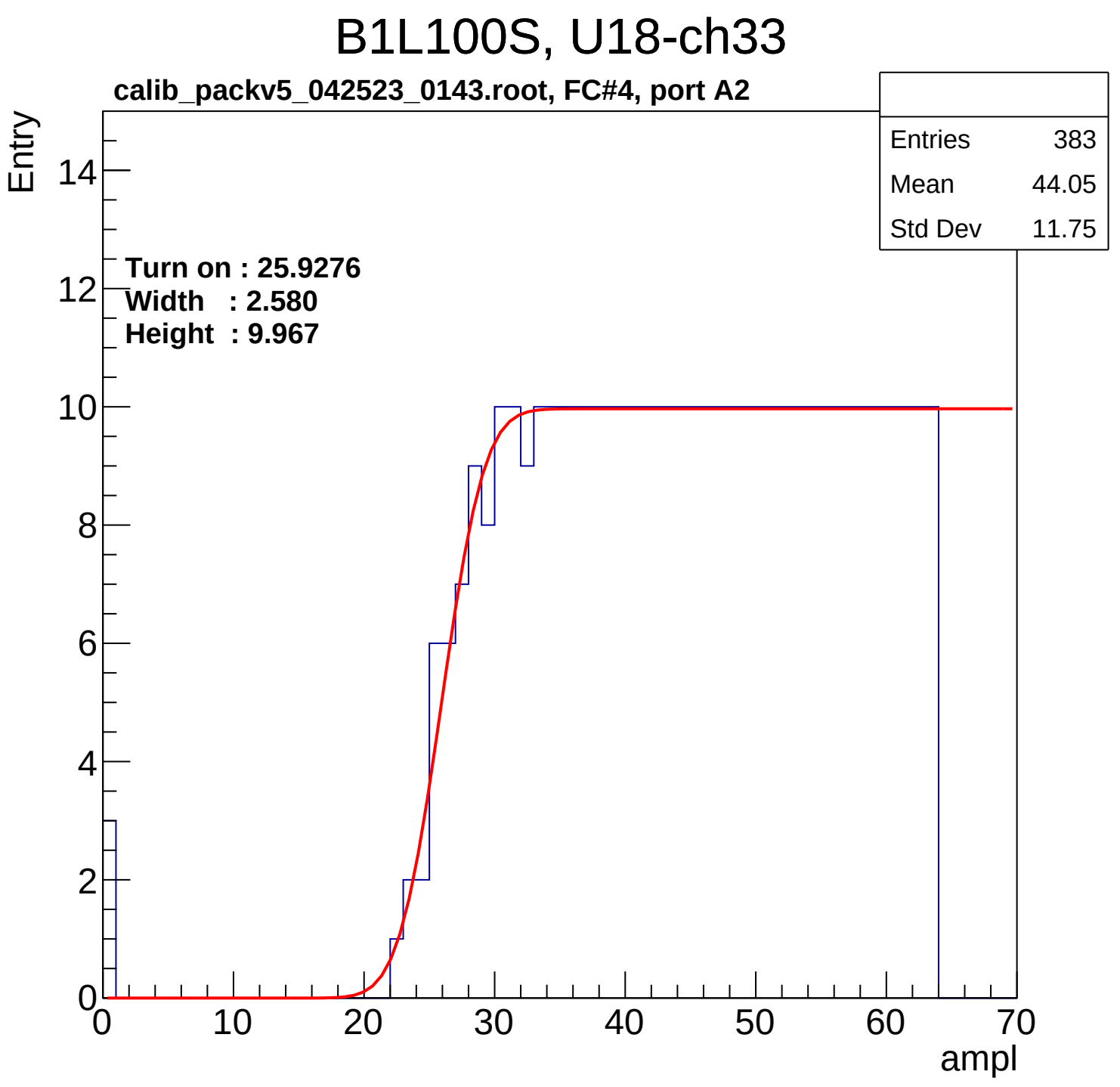
B1L100S, U18-ch33
calib_packv5_042523_0143.root, FC#4, port A2
Entries 383
Mean 44.05
Std Dev 11.75
Turn on : 25.9276
Width : 2.580
Height : 9.967
Entry
ampl
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2
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6
8
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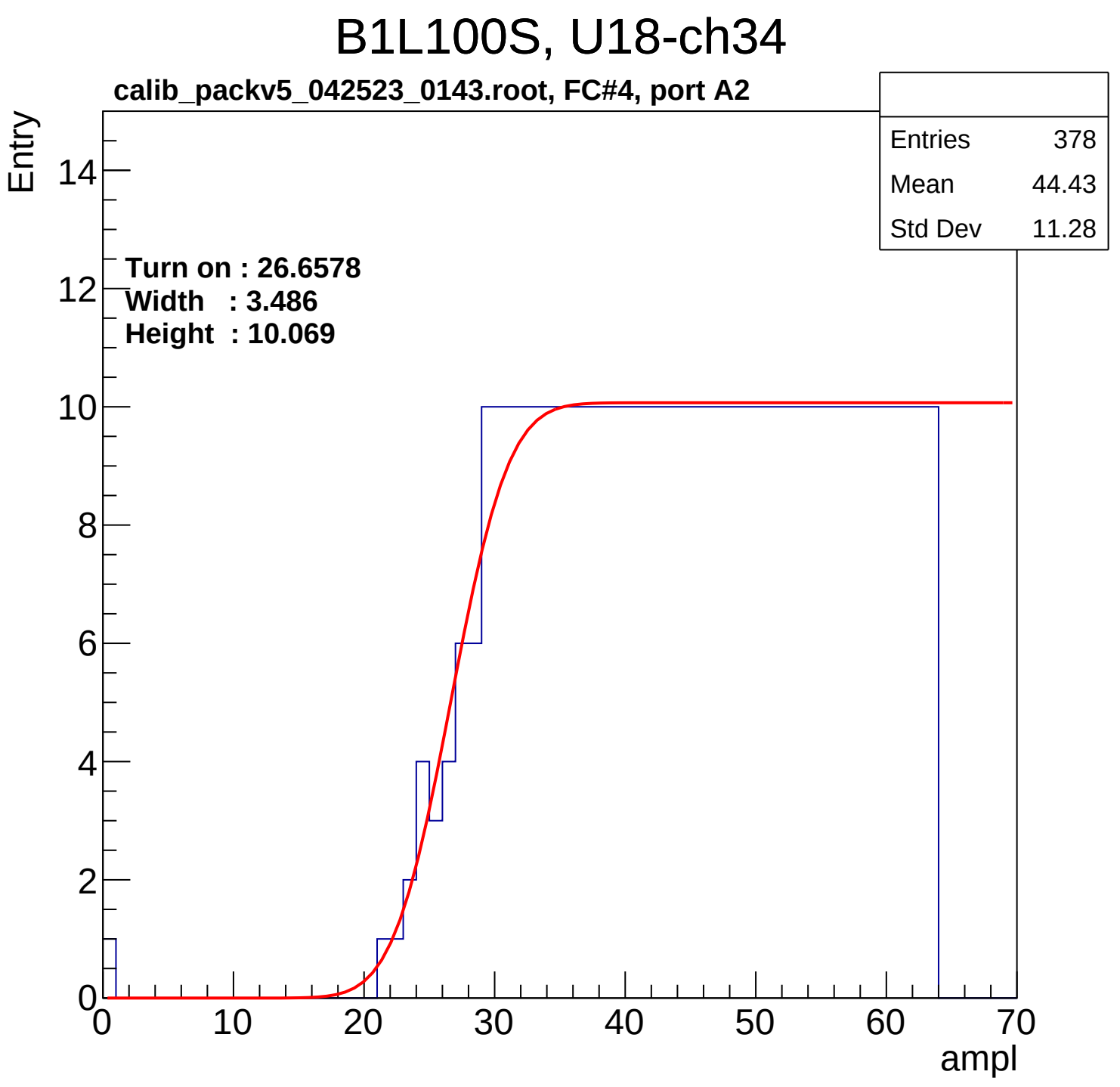
B1L100S, U18-ch34
calib_packv5_042523_0143.root, FC#4, port A2
Entries 378
Mean 44.43
Std Dev 11.28
Turn on : 26.6578
Width : 3.486
Height : 10.069
Entry
ampl
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2
4
6
8
10
12
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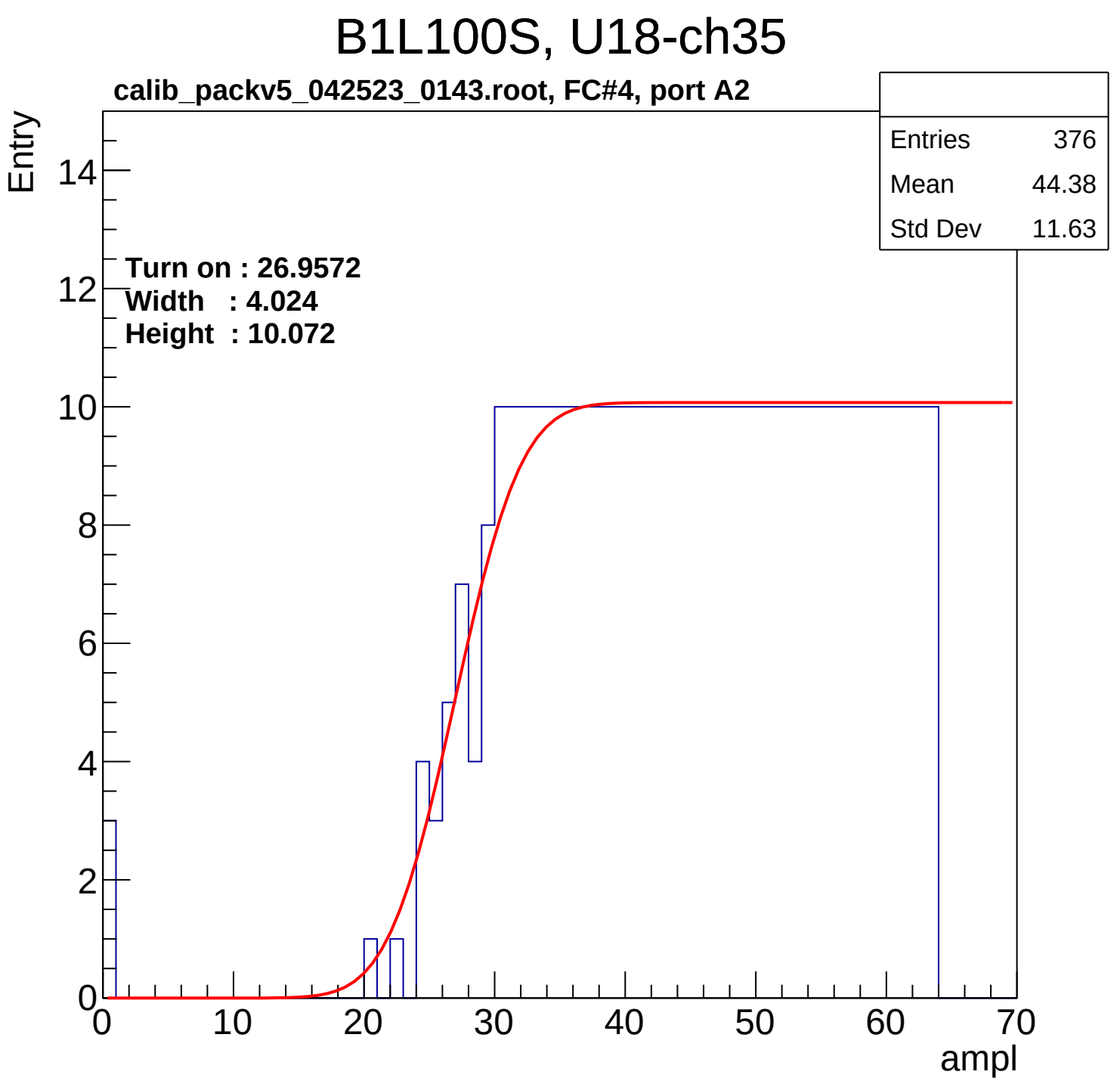
B1L100S, U18-ch35
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.38
Std Dev 11.63
Turn on : 26.9572
Width : 4.024
Height : 10.072
Entry
ampl
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4
6
8
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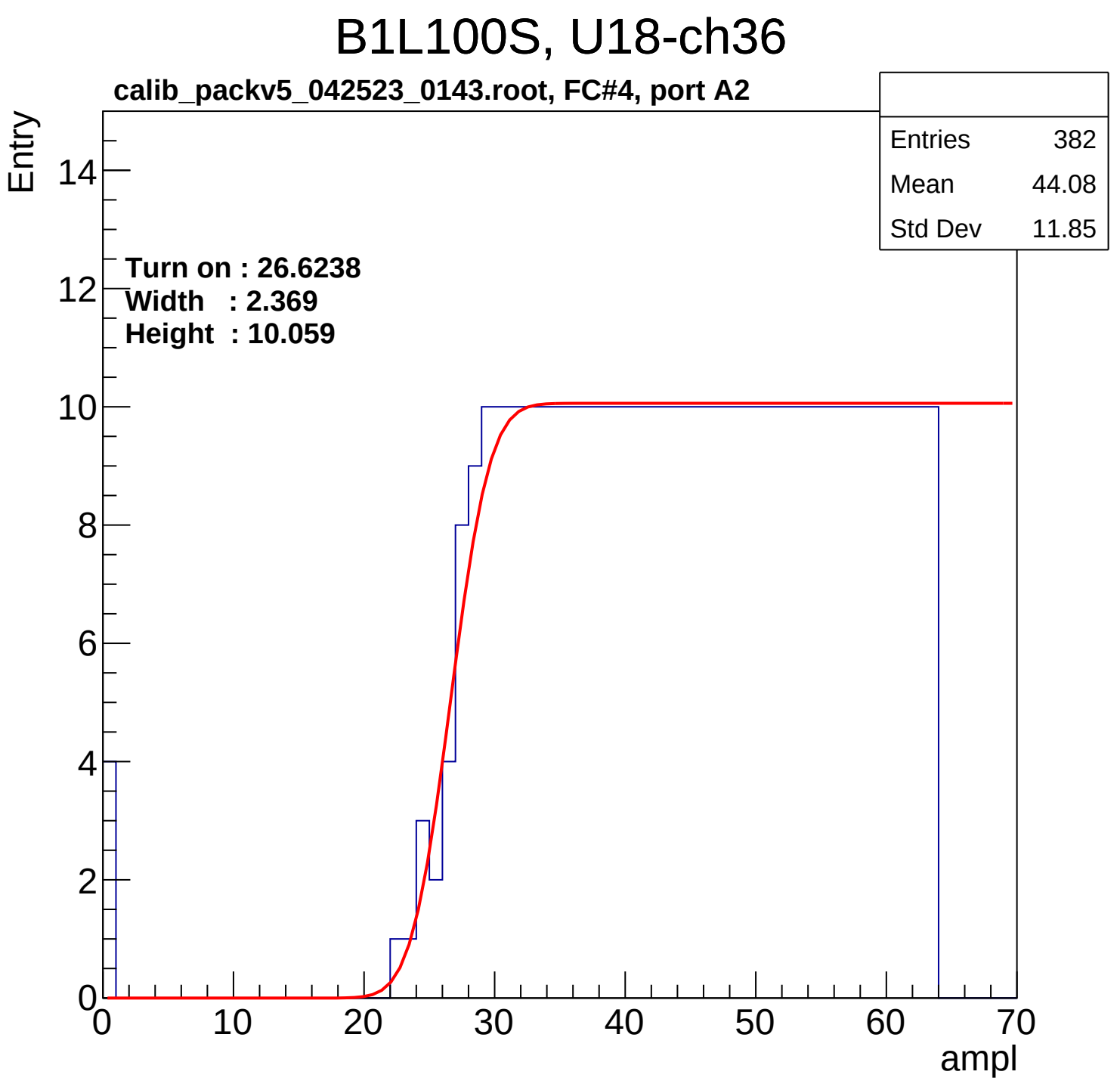
B1L100S, U18-ch36
calib_packv5_042523_0143.root, FC#4, port A2
Entries 382
Mean 44.08
Std Dev 11.85
Turn on : 26.6238
Width : 2.369
Height : 10.059
Entry
ampl
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2
4
6
8
10
12
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0
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60
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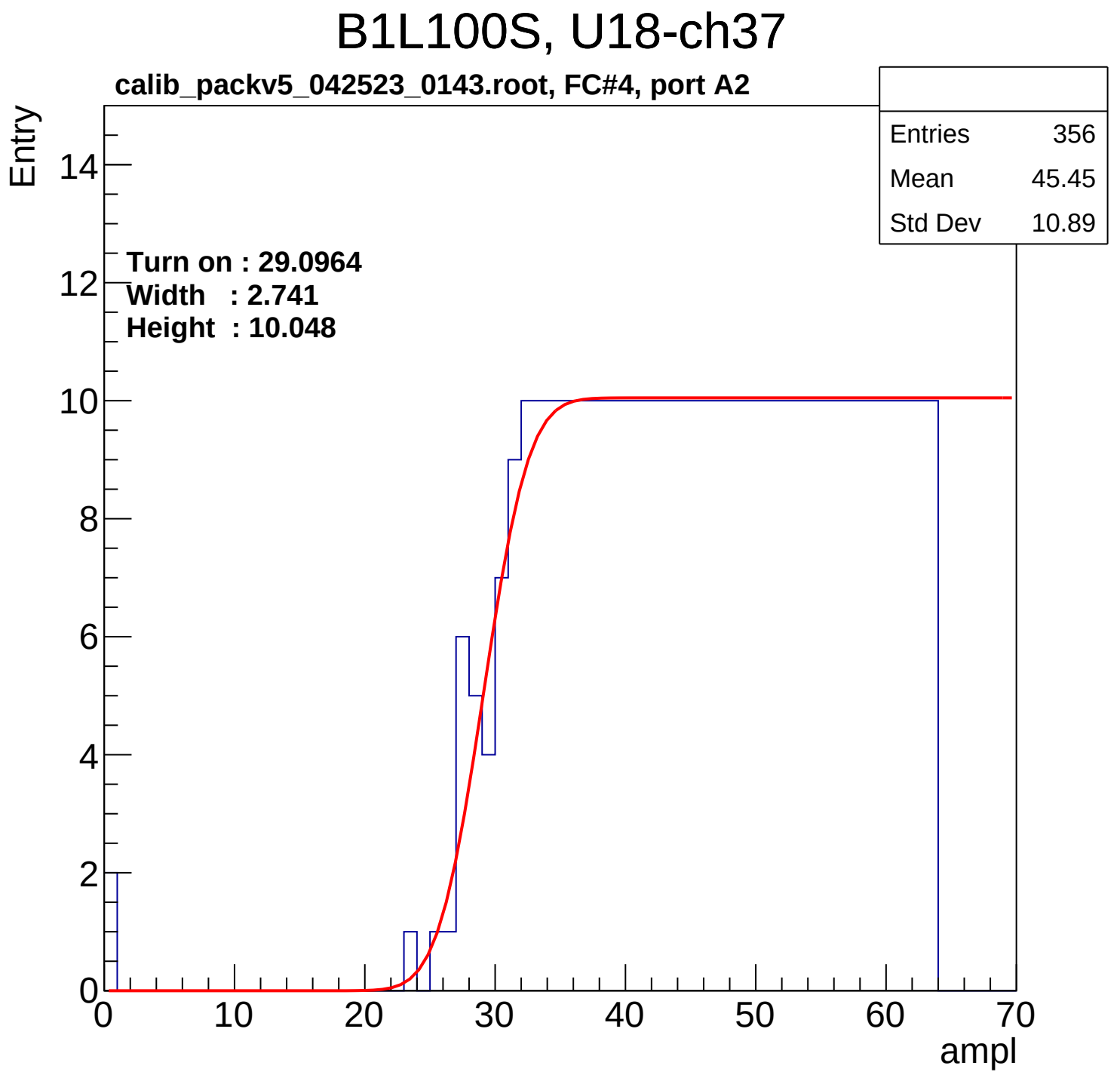
B1L100S, U18-ch37
calib_packv5_042523_0143.root, FC#4, port A2
Entries 356
Mean 45.45
Std Dev 10.89
Turn on : 29.0964
Width : 2.741
Height : 10.048
Entry
ampl
0
2
4
6
8
10
12
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0
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60
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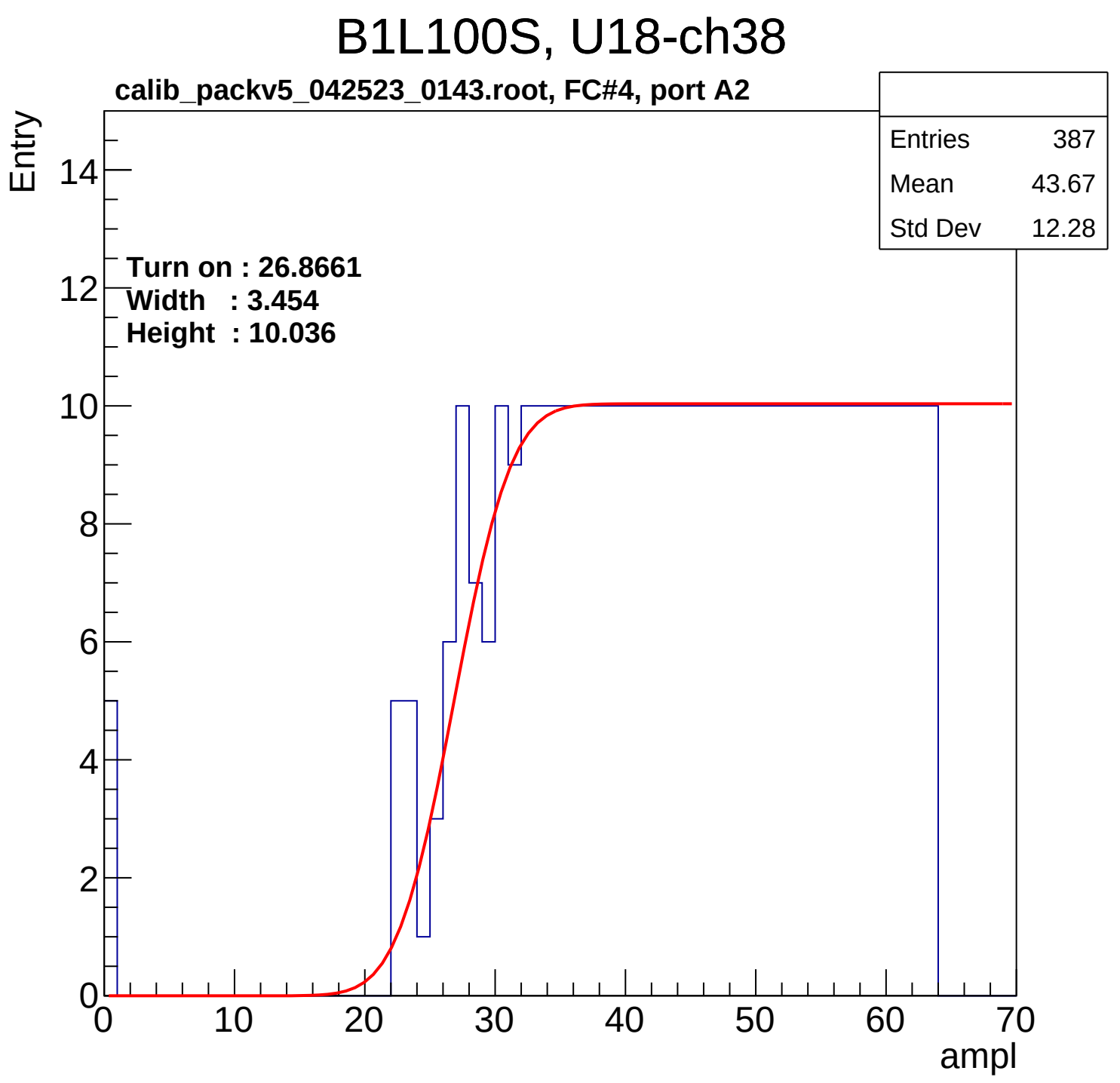
B1L100S, U18-ch38
calib_packv5_042523_0143.root, FC#4, port A2
Entries 387
Mean 43.67
Std Dev 12.28
Turn on : 26.8661
Width : 3.454
Height : 10.036
Entry
ampl
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6
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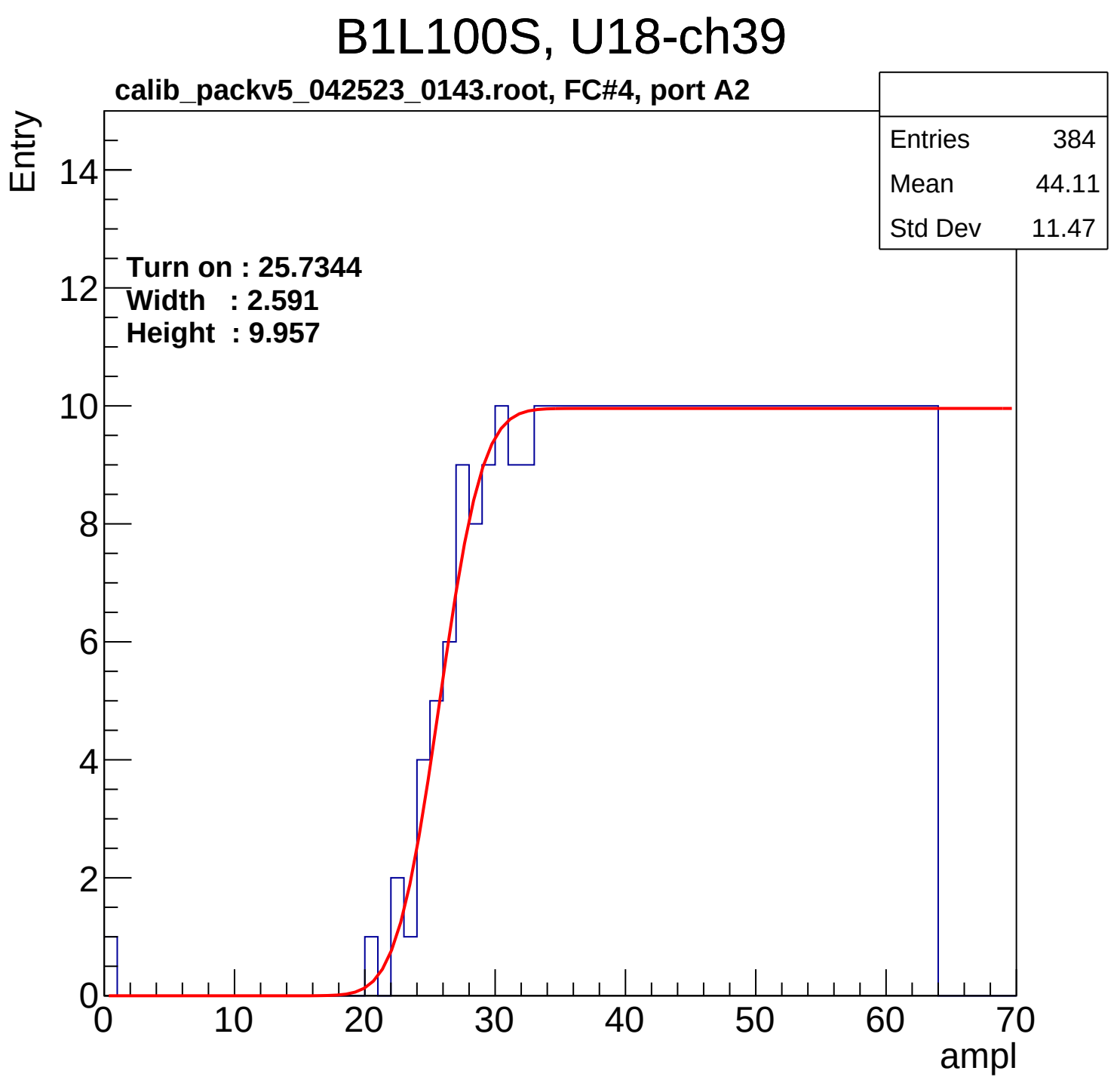
B1L100S, U18-ch39
calib_packv5_042523_0143.root, FC#4, port A2
Entries 384
Mean 44.11
Std Dev 11.47
Turn on : 25.7344
Width : 2.591
Height : 9.957
Entry
ampl
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6
8
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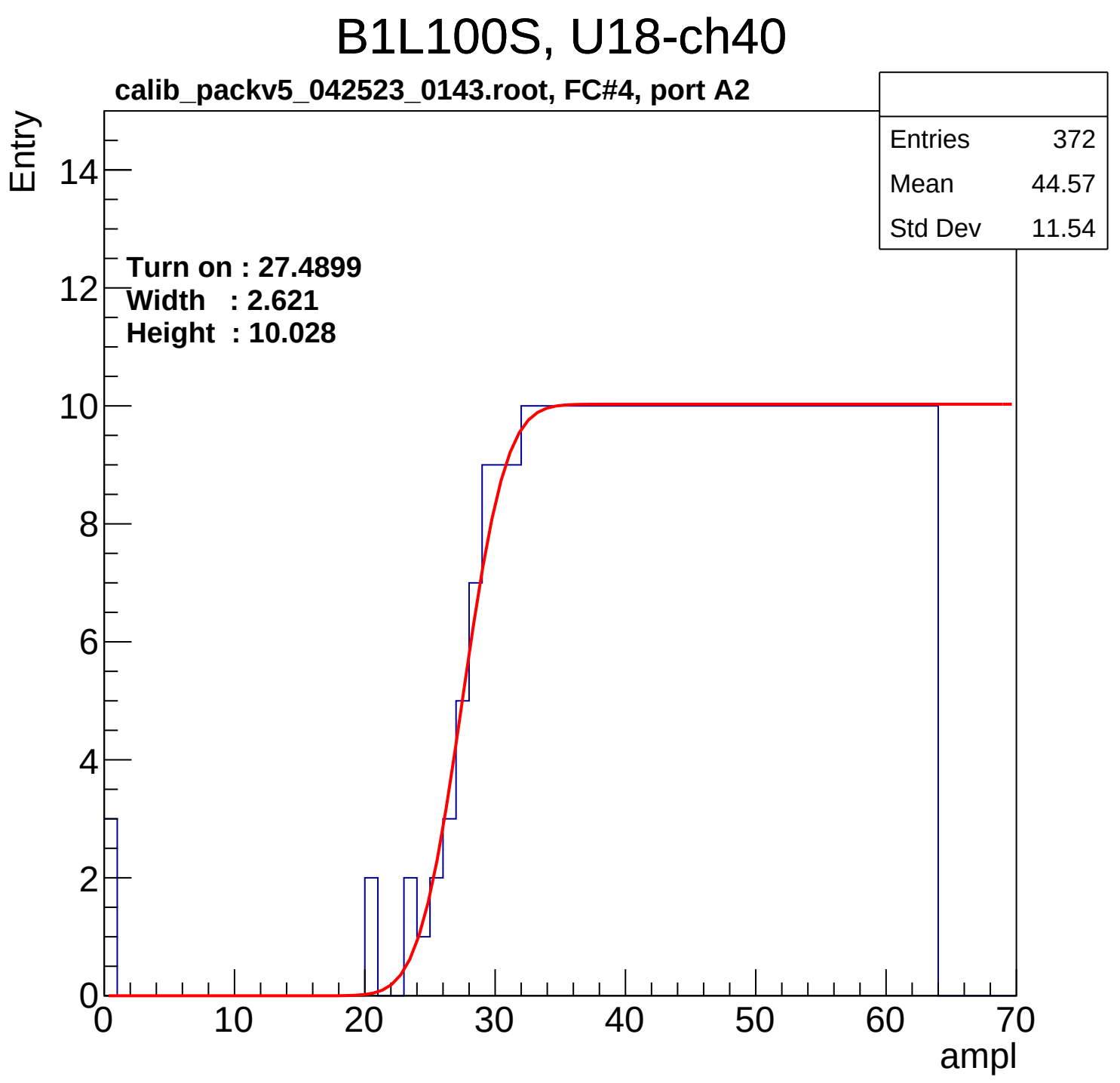
B1L100S, U18-ch40
calib_packv5_042523_0143.root, FC#4, port A2
Entries 372
Mean 44.57
Std Dev 11.54
Turn on : 27.4899
Width : 2.621
Height : 10.028
Entry
ampl
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6
8
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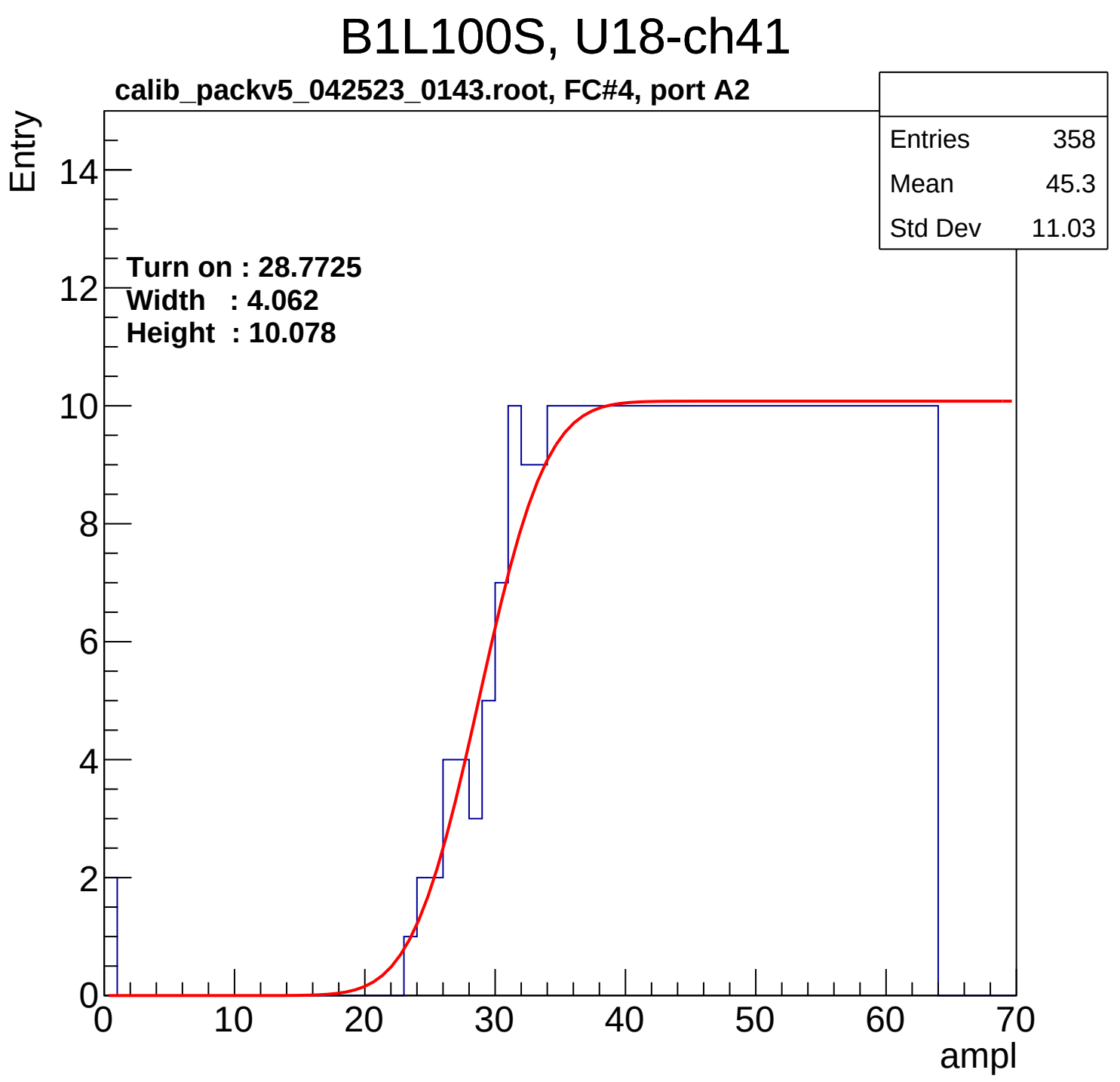
B1L100S, U18-ch41
calib_packv5_042523_0143.root, FC#4, port A2
Entries 358
Mean 45.3
Std Dev 11.03
Turn on : 28.7725
Width : 4.062
Height : 10.078
Entry
ampl
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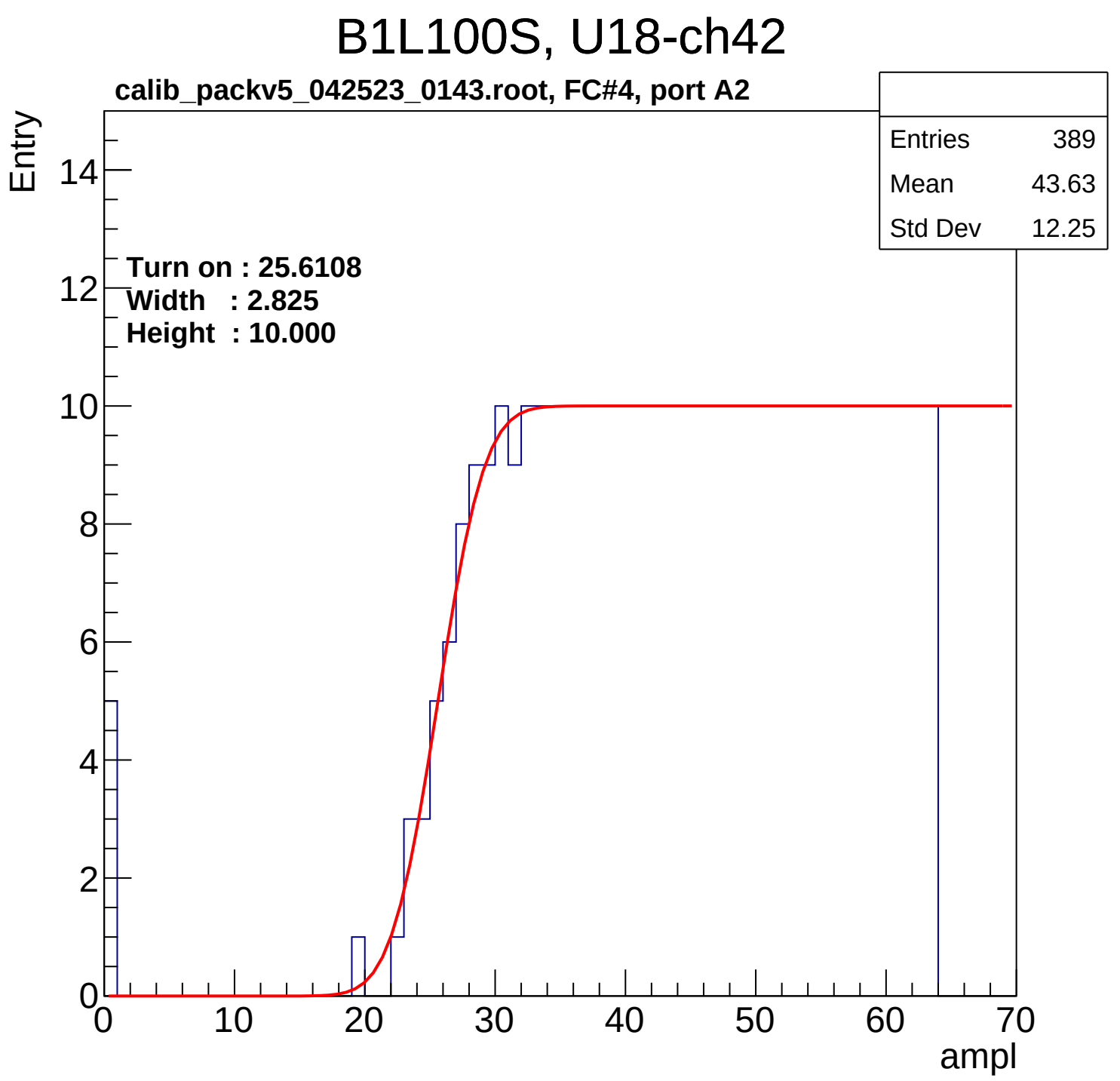
B1L100S, U18-ch42
calib_packv5_042523_0143.root, FC#4, port A2
Entries 389
Mean 43.63
Std Dev 12.25
Turn on : 25.6108
Width : 2.825
Height : 10.000
Entry
ampl
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6
8
10
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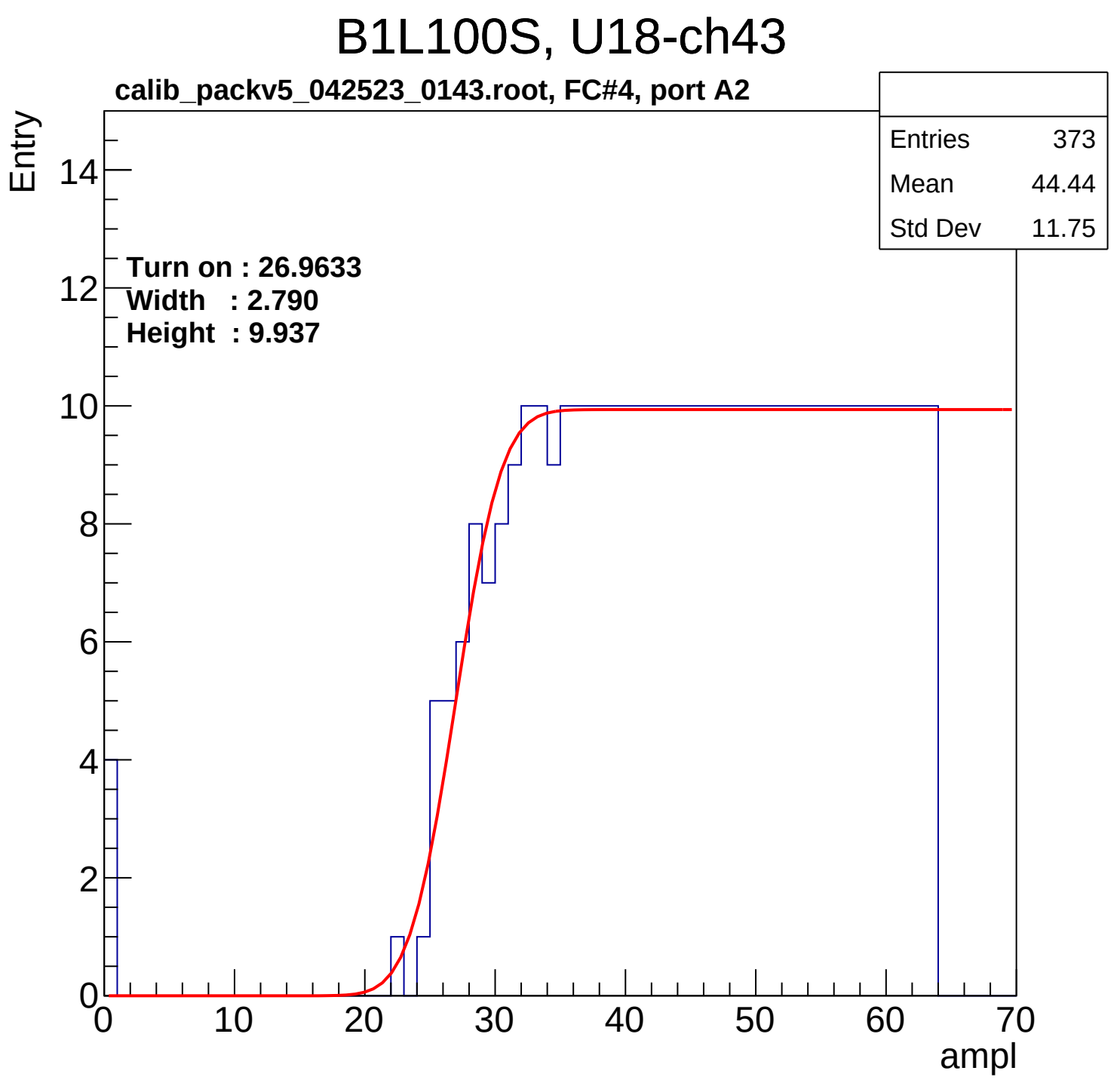
B1L100S, U18-ch43
calib_packv5_042523_0143.root, FC#4, port A2
Entries 373
Mean 44.44
Std Dev 11.75
Turn on : 26.9633
Width : 2.790
Height : 9.937
Entry
ampl
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6
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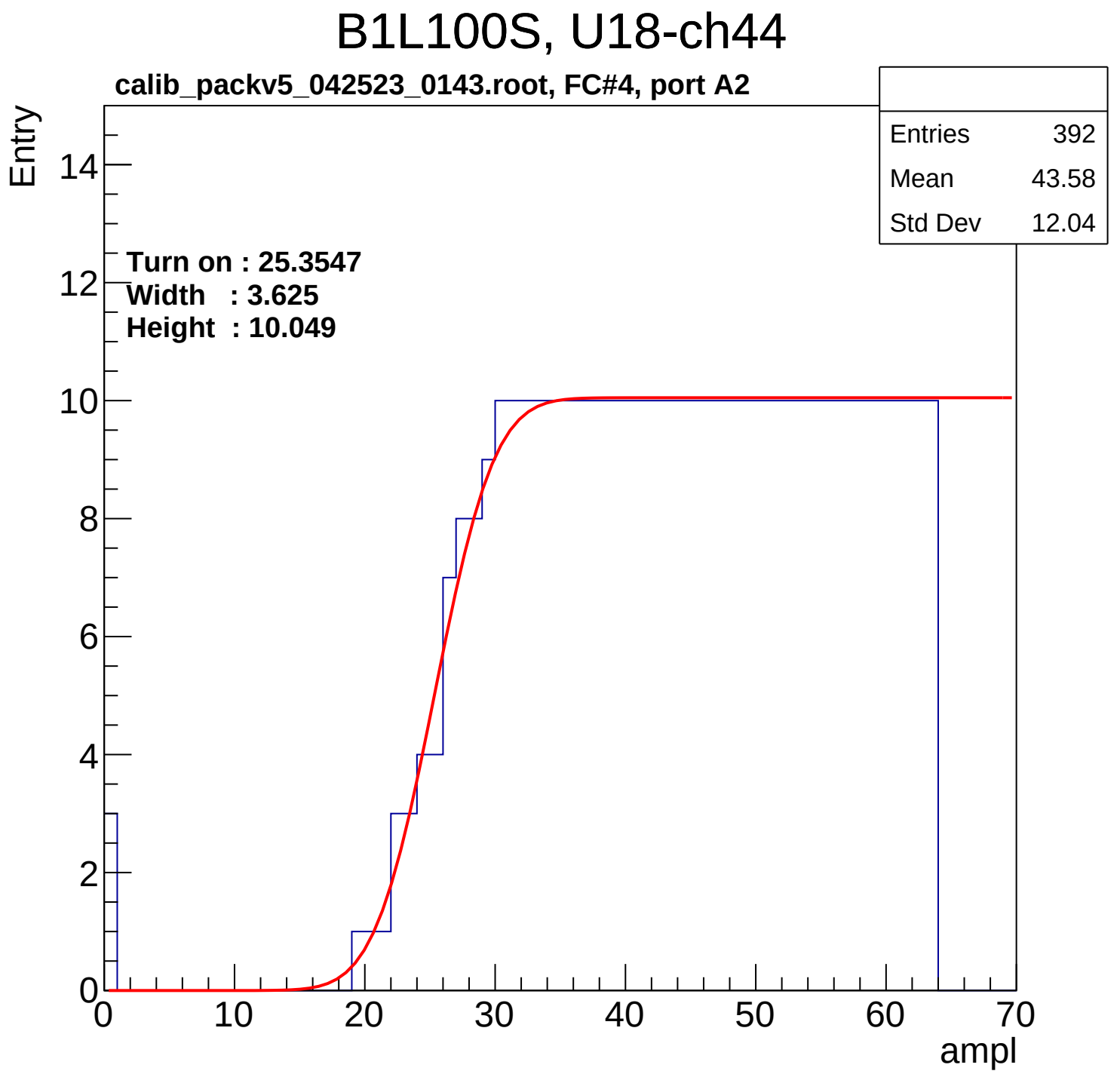
B1L100S, U18-ch44
calib_packv5_042523_0143.root, FC#4, port A2
Entries 392
Mean 43.58
Std Dev 12.04
Turn on : 25.3547
Width : 3.625
Height : 10.049
Entry
ampl
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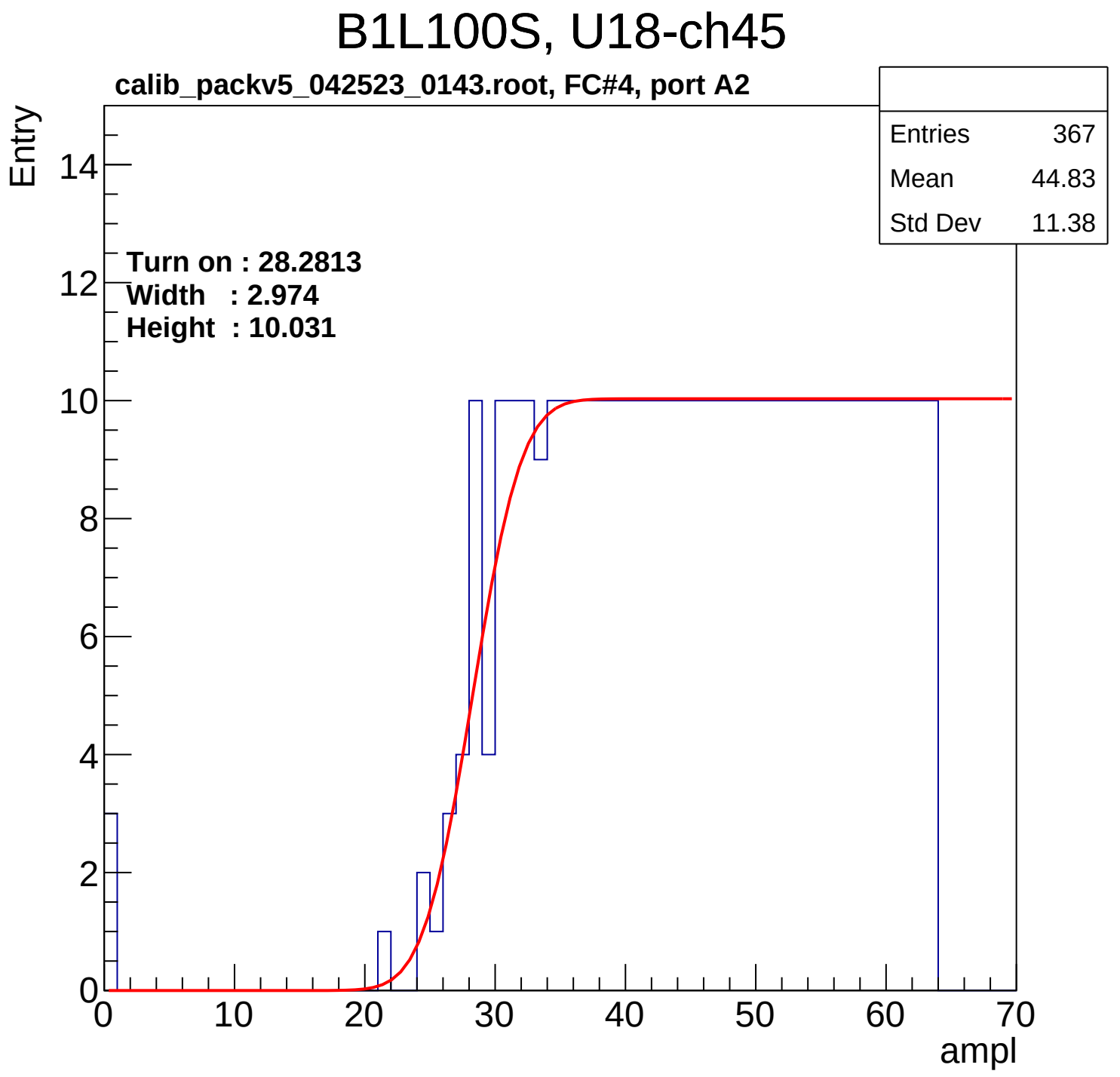
B1L100S, U18-ch45
calib_packv5_042523_0143.root, FC#4, port A2
Entries 367
Mean 44.83
Std Dev 11.38
Turn on : 28.2813
Width : 2.974
Height : 10.031
Entry
ampl
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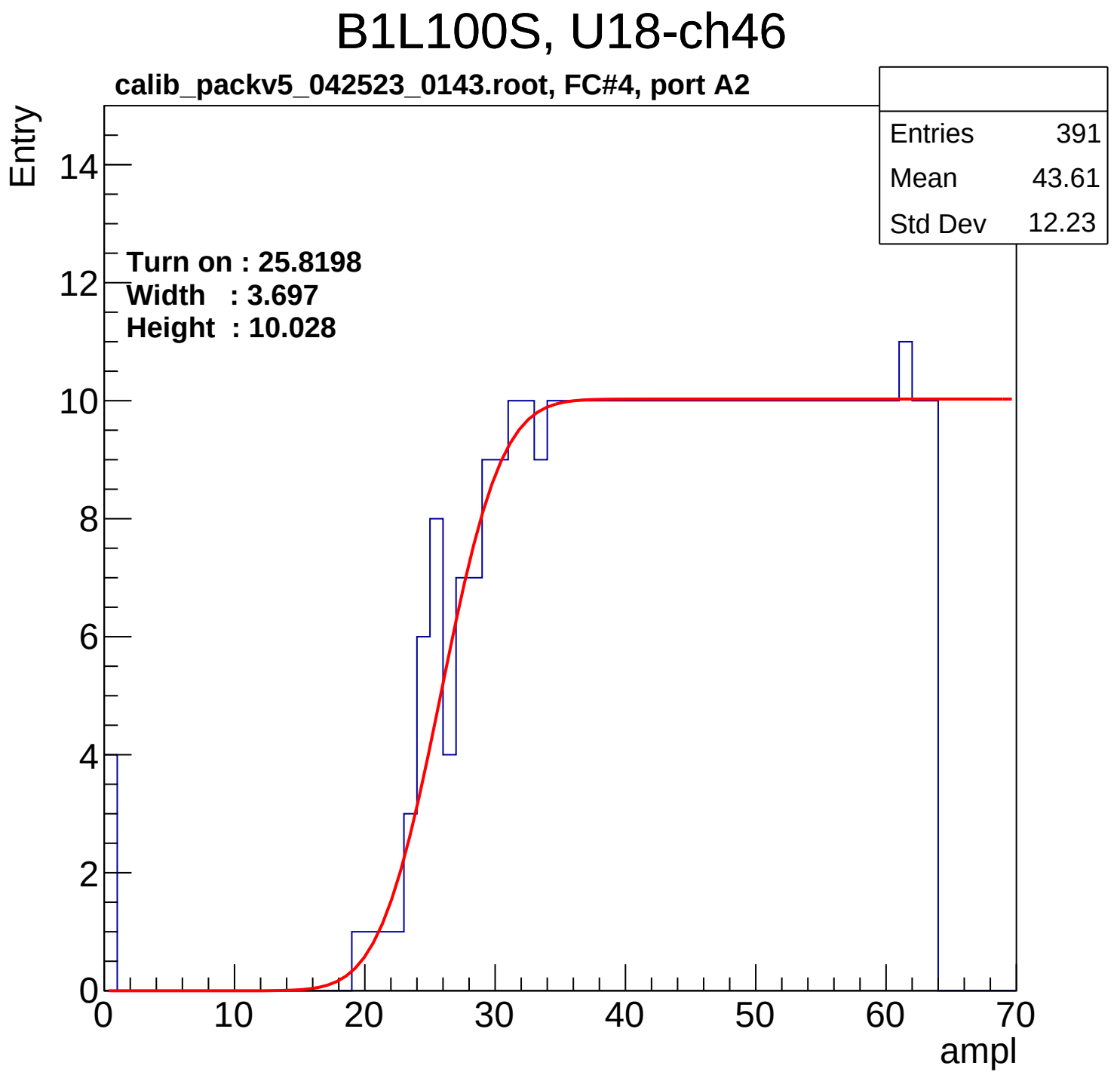
B1L100S, U18-ch46
calib_packv5_042523_0143.root, FC#4, port A2
Entries 391
Mean 43.61
Std Dev 12.23
Turn on : 25.8198
Width : 3.697
Height : 10.028
Entry
ampl
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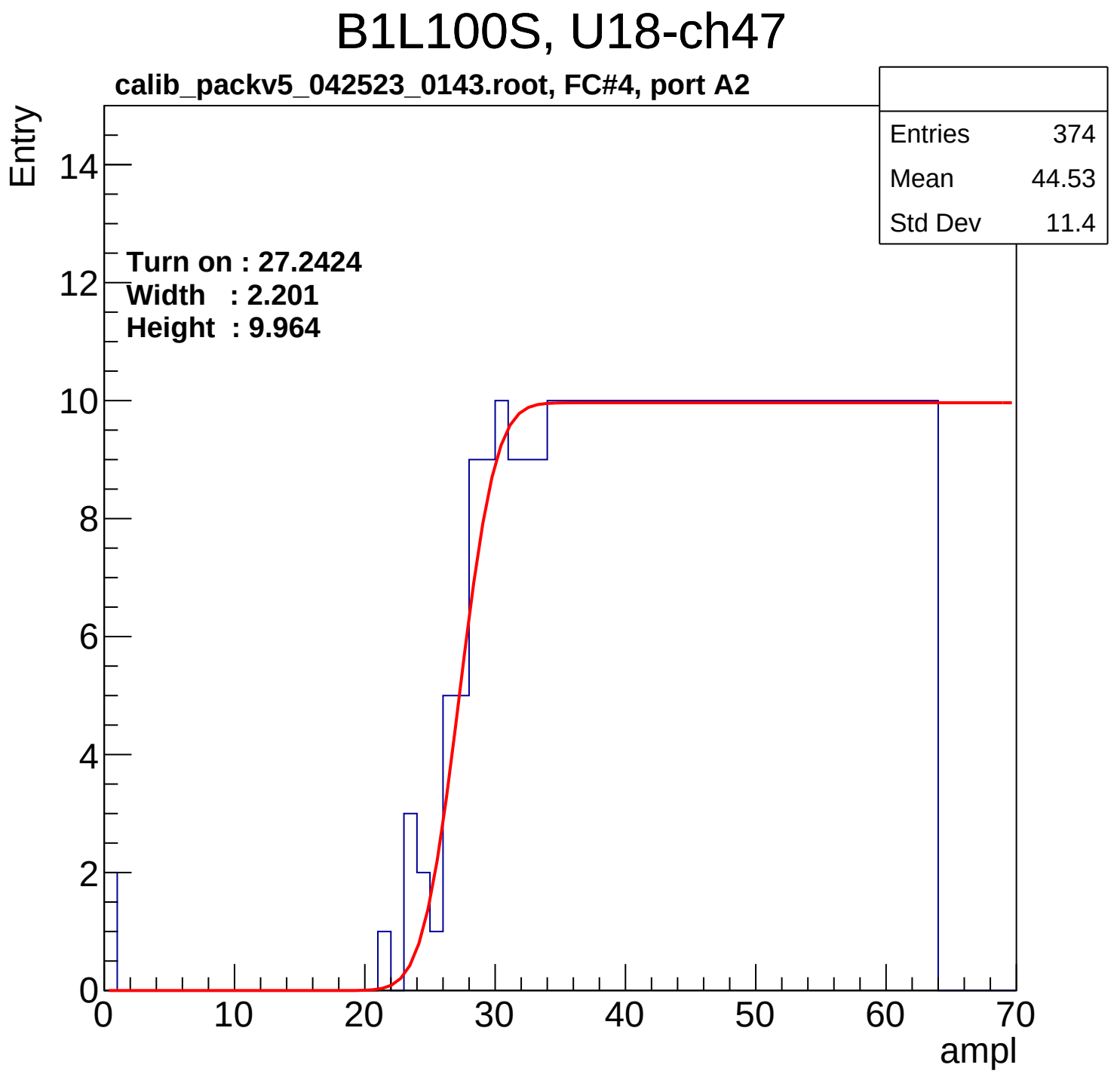
B1L100S, U18-ch47
calib_packv5_042523_0143.root, FC#4, port A2
Entries 374
Mean 44.53
Std Dev 11.4
Turn on : 27.2424
Width : 2.201
Height : 9.964
Entry
ampl
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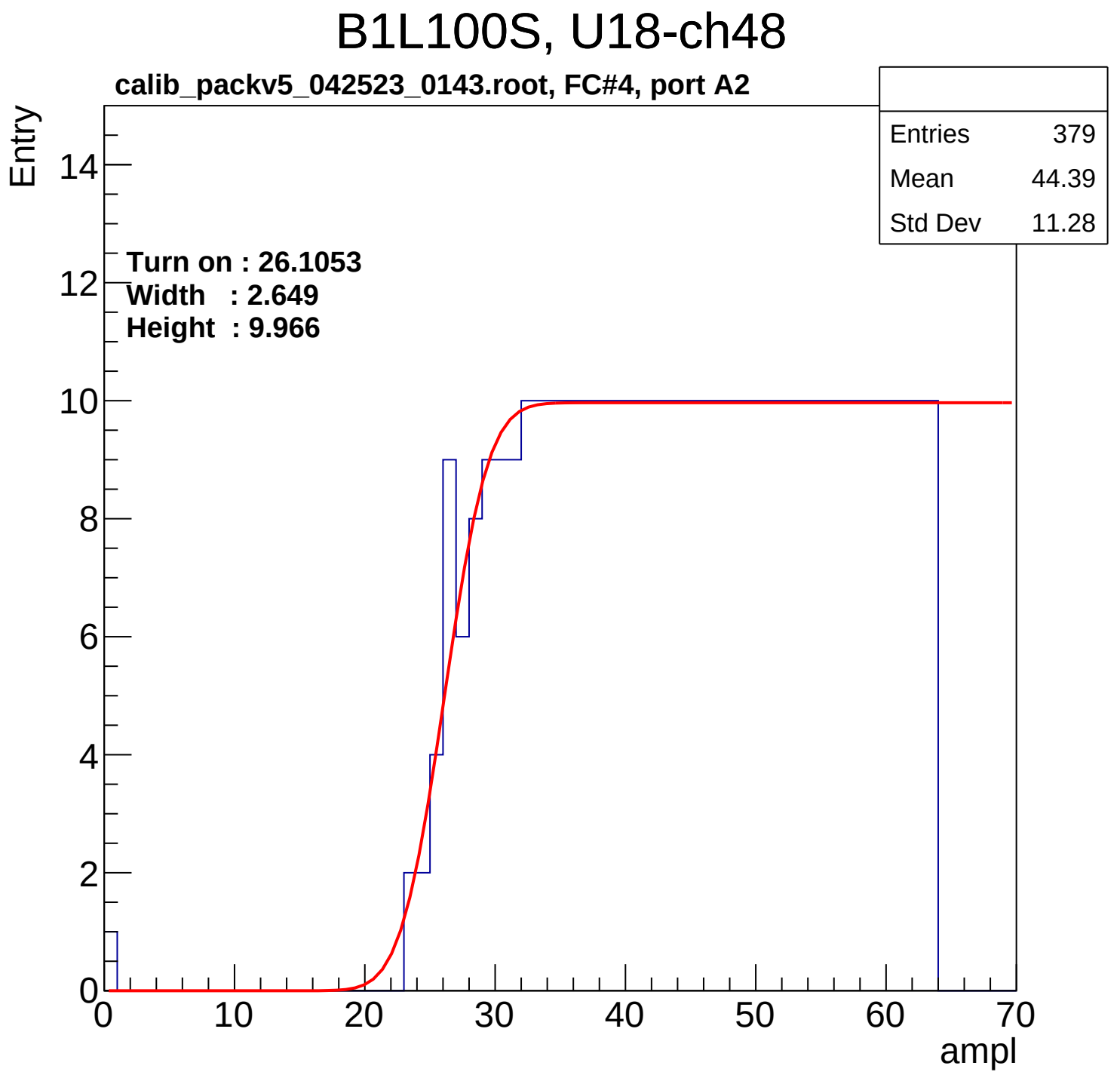
B1L100S, U18-ch48
calib_packv5_042523_0143.root, FC#4, port A2
Entries 379
Mean 44.39
Std Dev 11.28
Turn on : 26.1053
Width : 2.649
Height : 9.966
Entry
ampl
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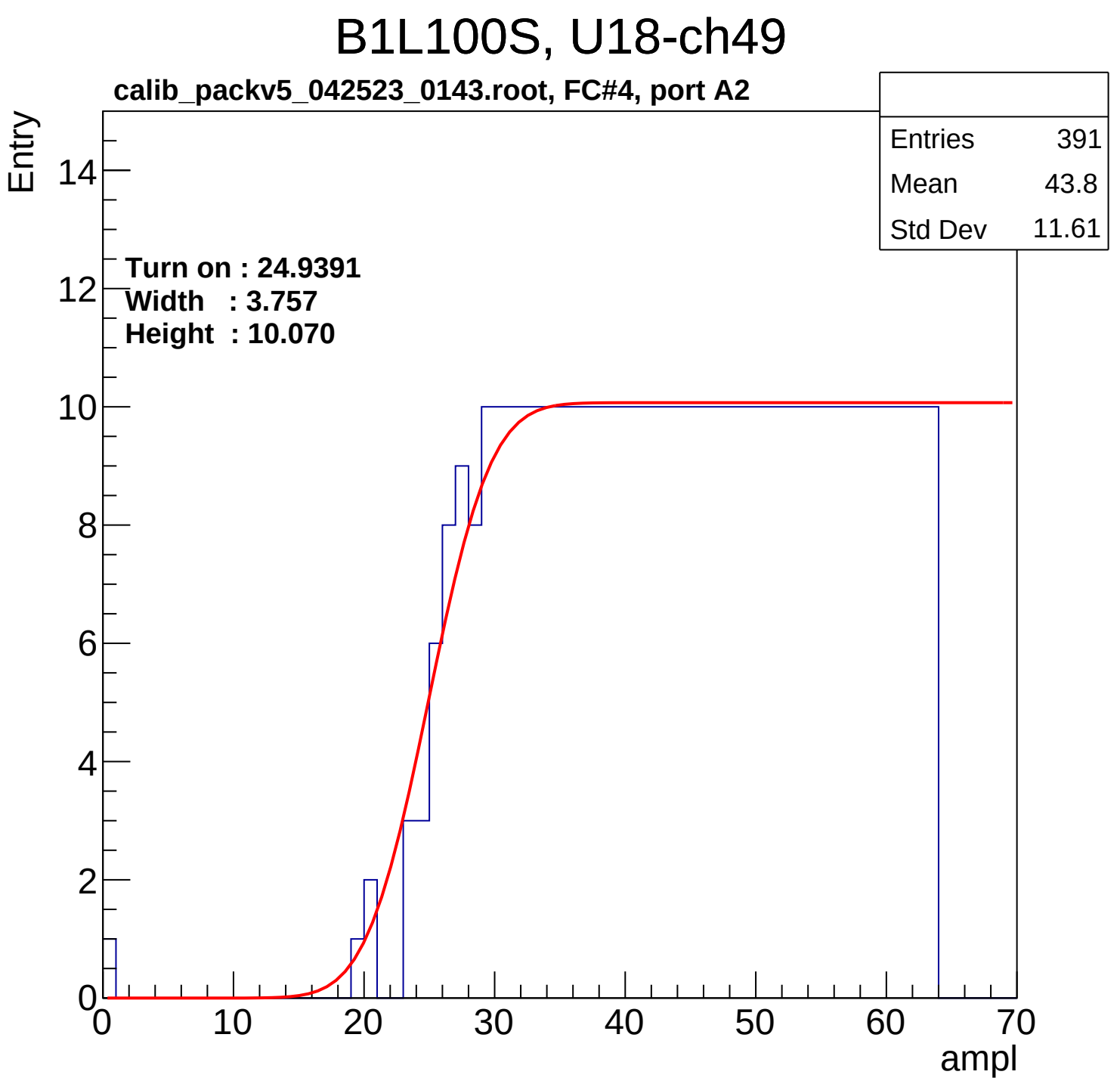
B1L100S, U18-ch49
calib_packv5_042523_0143.root, FC#4, port A2
Entries 391
Mean 43.8
Std Dev 11.61
Turn on : 24.9391
Width : 3.757
Height : 10.070
Entry
ampl
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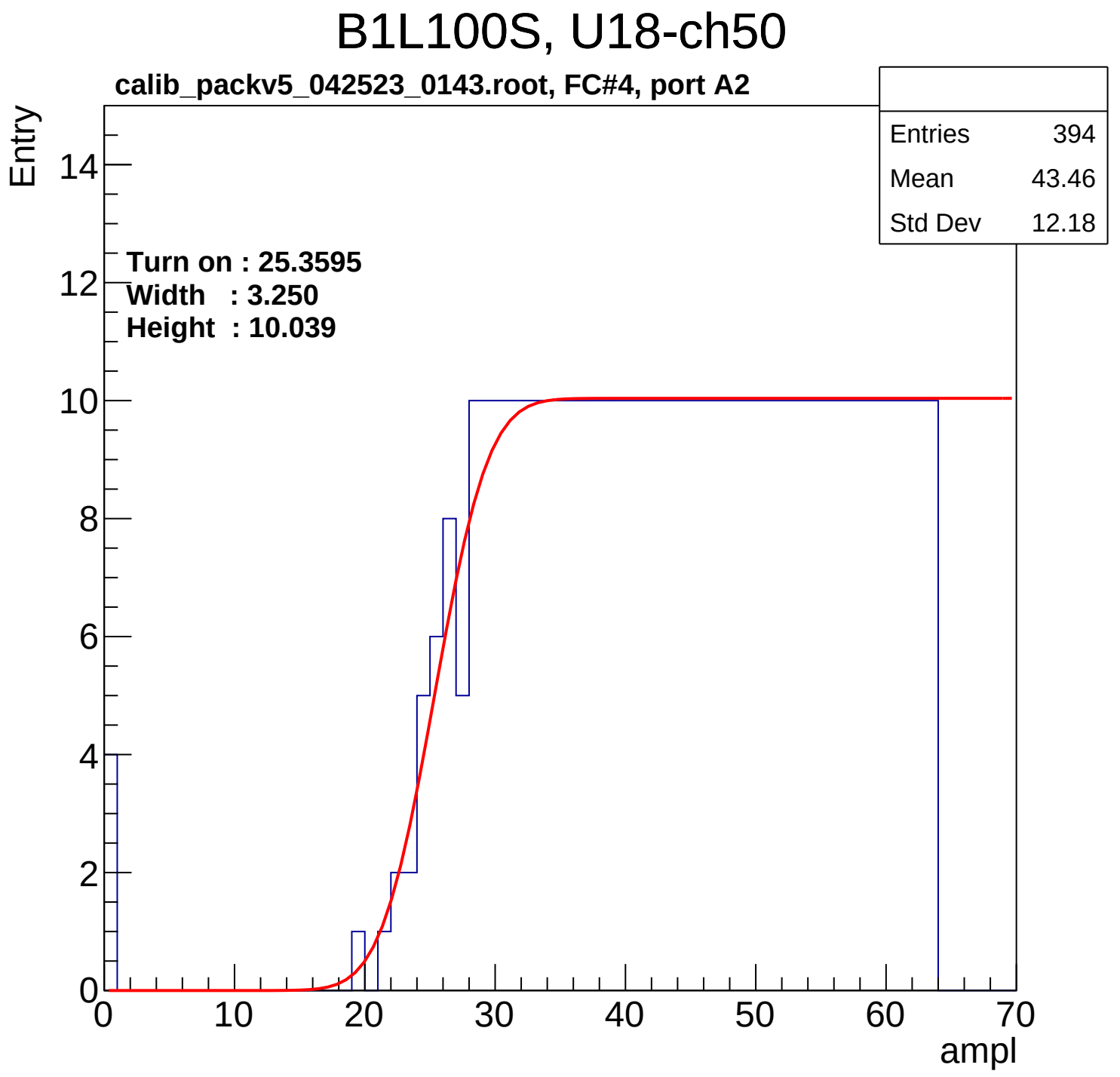
B1L100S, U18-ch50
calib_packv5_042523_0143.root, FC#4, port A2
Entries 394
Mean 43.46
Std Dev 12.18
Turn on : 25.3595
Width : 3.250
Height : 10.039
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ampl
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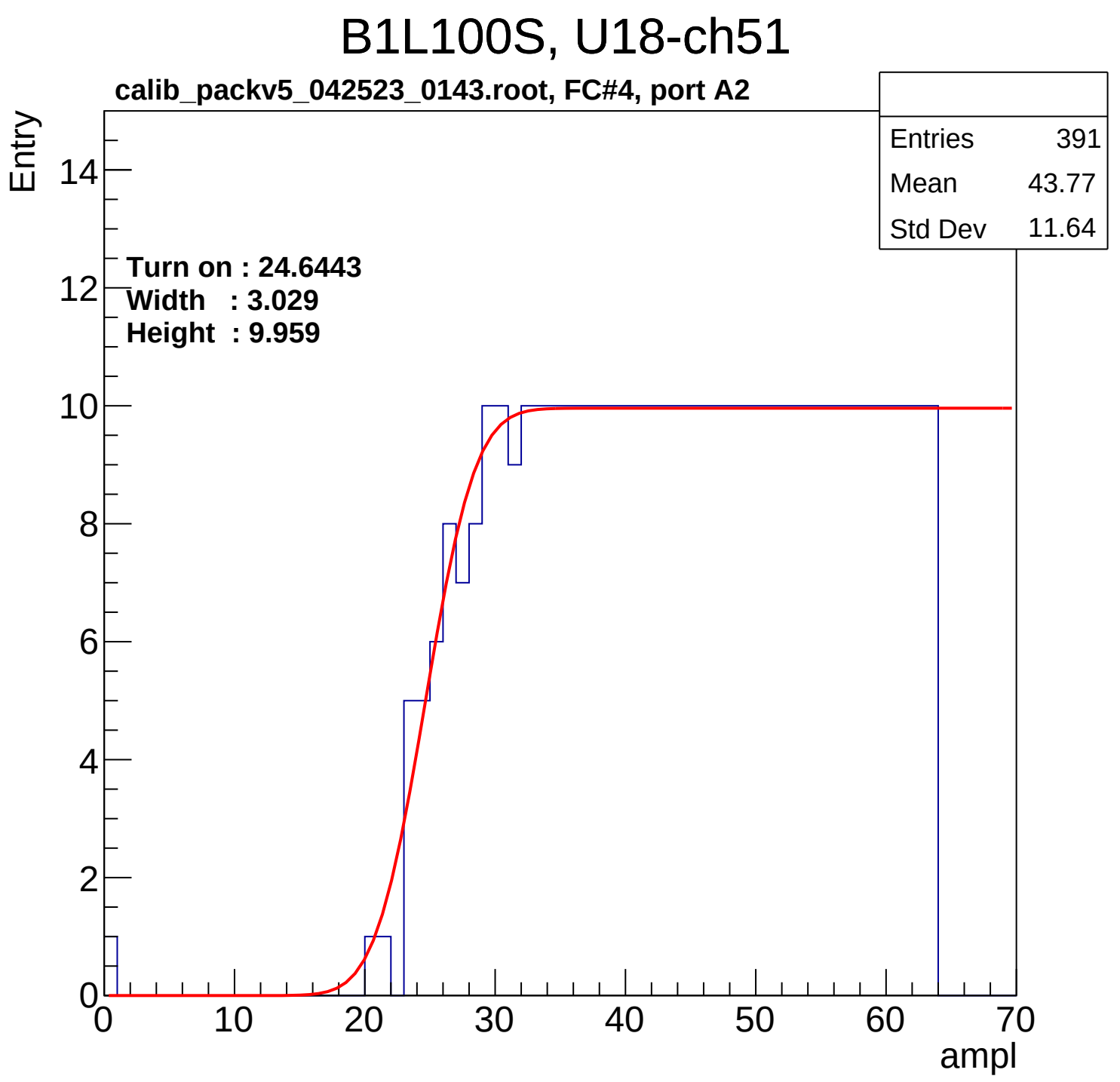
B1L100S, U18-ch51
calib_packv5_042523_0143.root, FC#4, port A2
Entries 391
Mean 43.77
Std Dev 11.64
Turn on : 24.6443
Width : 3.029
Height : 9.959
Entry
ampl
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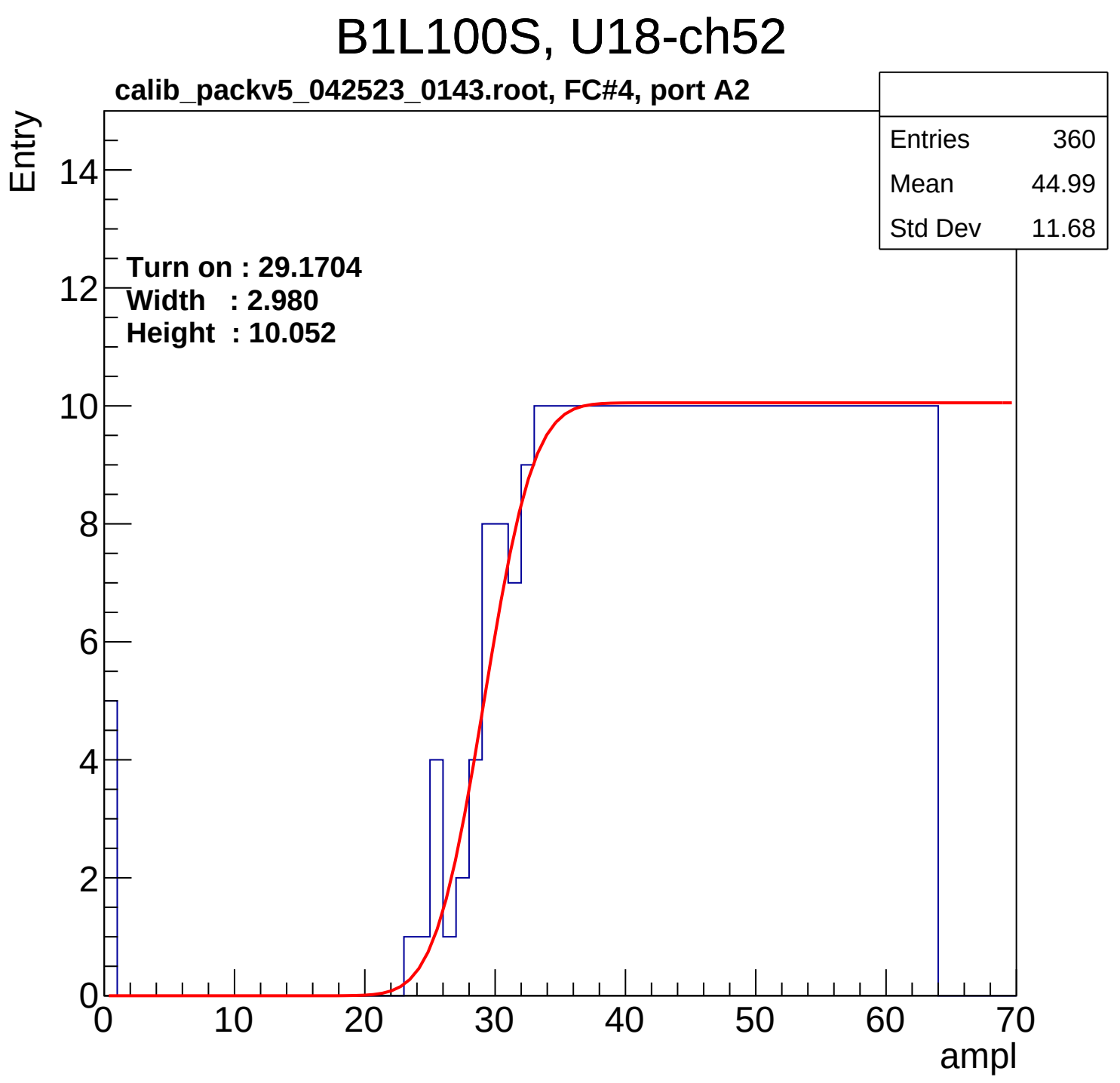
B1L100S, U18-ch52
calib_packv5_042523_0143.root, FC#4, port A2
Entries 360
Mean 44.99
Std Dev 11.68
Turn on : 29.1704
Width : 2.980
Height : 10.052
Entry
ampl
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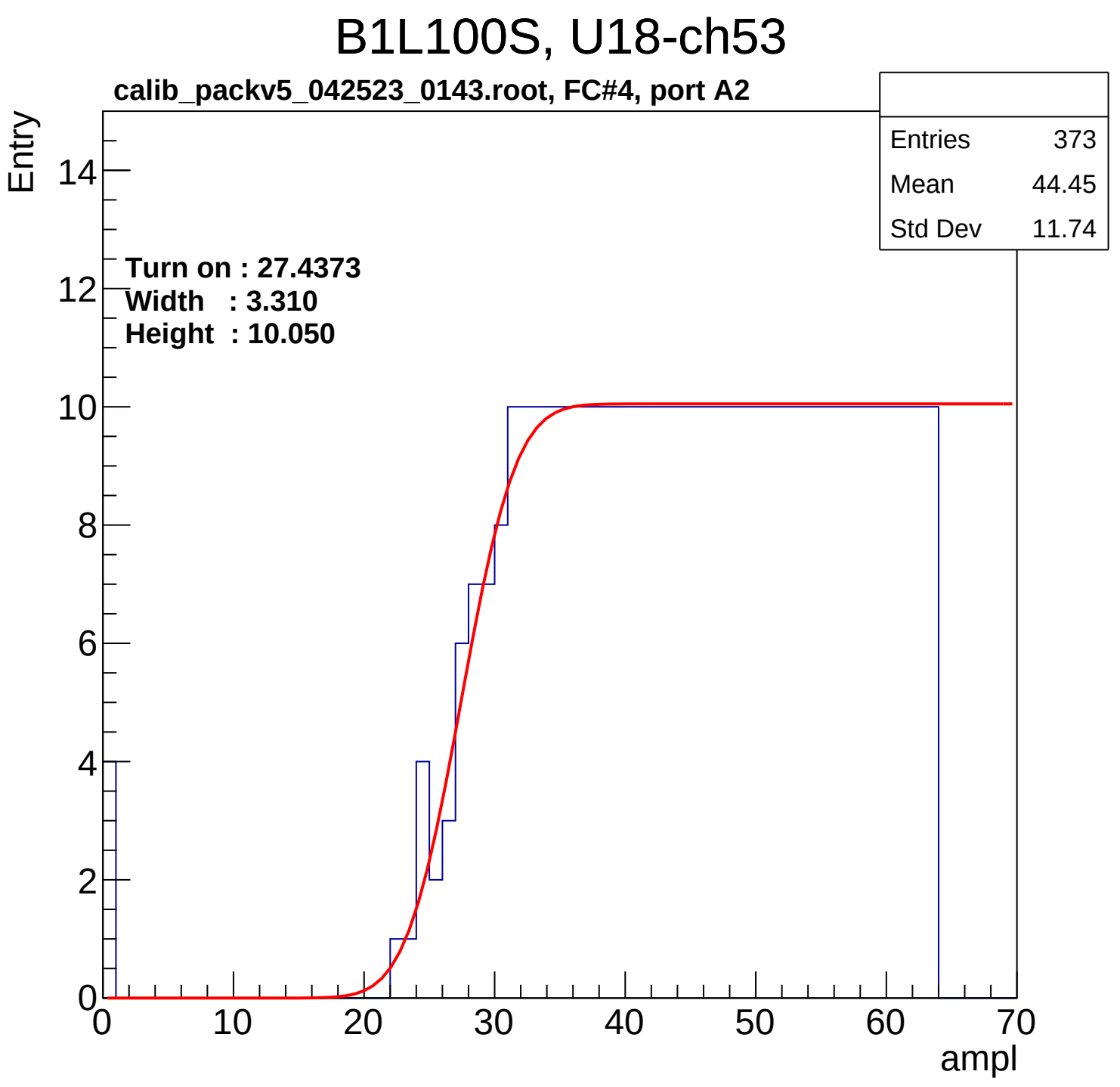
B1L100S, U18-ch53
calib_packv5_042523_0143.root, FC#4, port A2
Entries 373
Mean 44.45
Std Dev 11.74
Turn on : 27.4373
Width : 3.310
Height : 10.050
Entry
ampl
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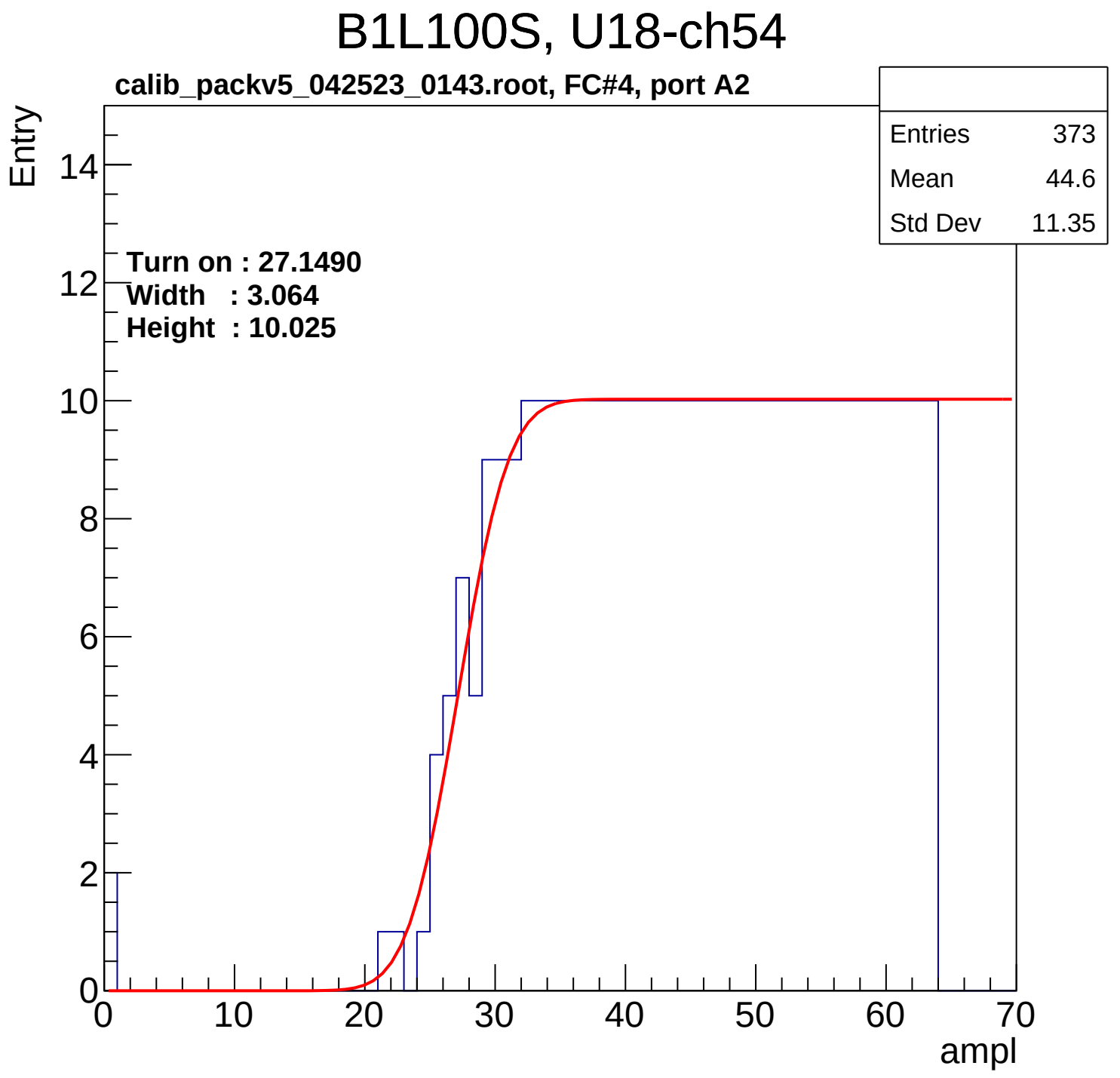
B1L100S, U18-ch54
calib_packv5_042523_0143.root, FC#4, port A2
Entries 373
Mean 44.6
Std Dev 11.35
Turn on : 27.1490
Width : 3.064
Height : 10.025
Entry
ampl
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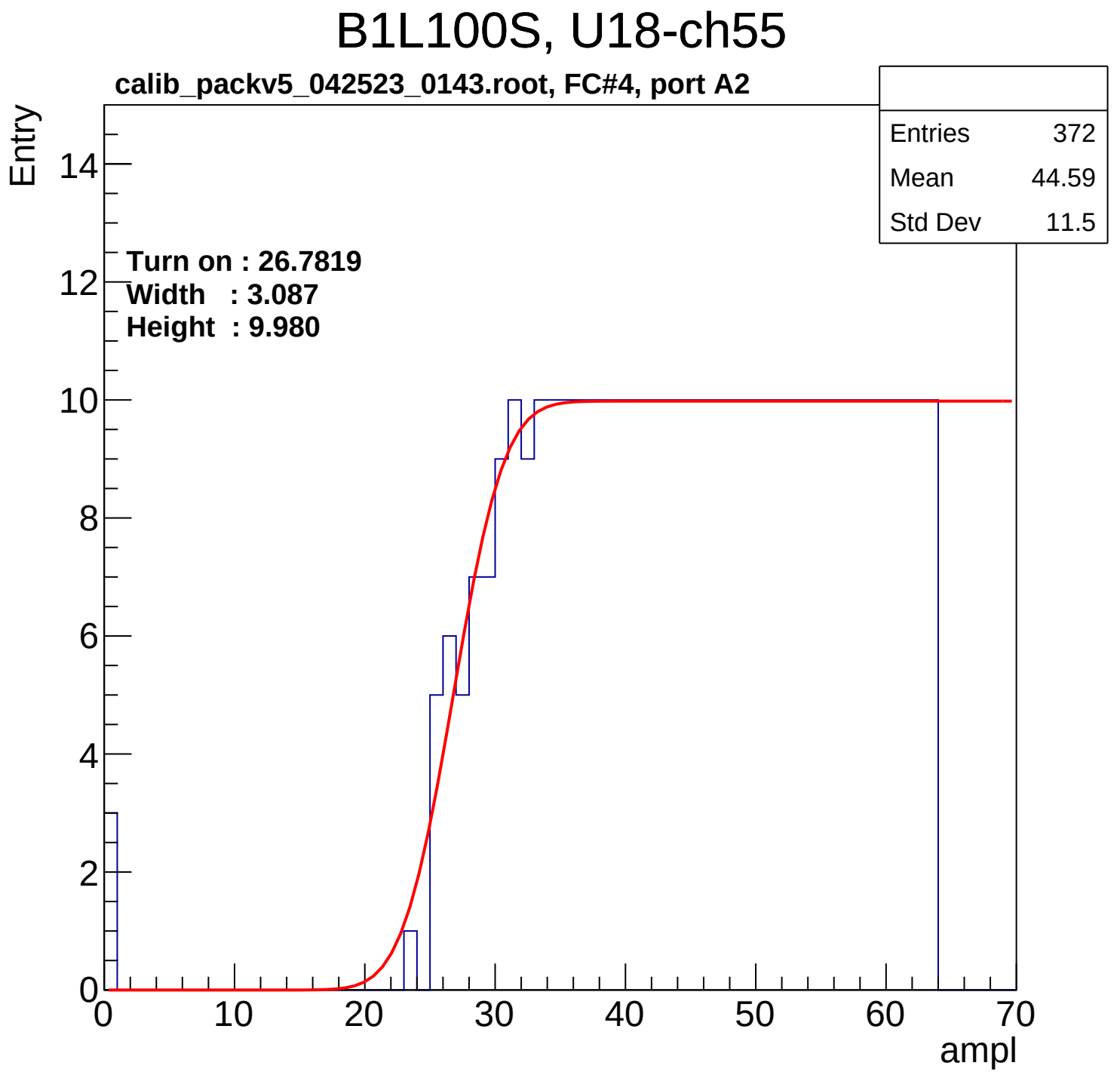
B1L100S, U18-ch55
calib_packv5_042523_0143.root, FC#4, port A2
Entries 372
Mean 44.59
Std Dev 11.5
Turn on : 26.7819
Width : 3.087
Height : 9.980
Entry
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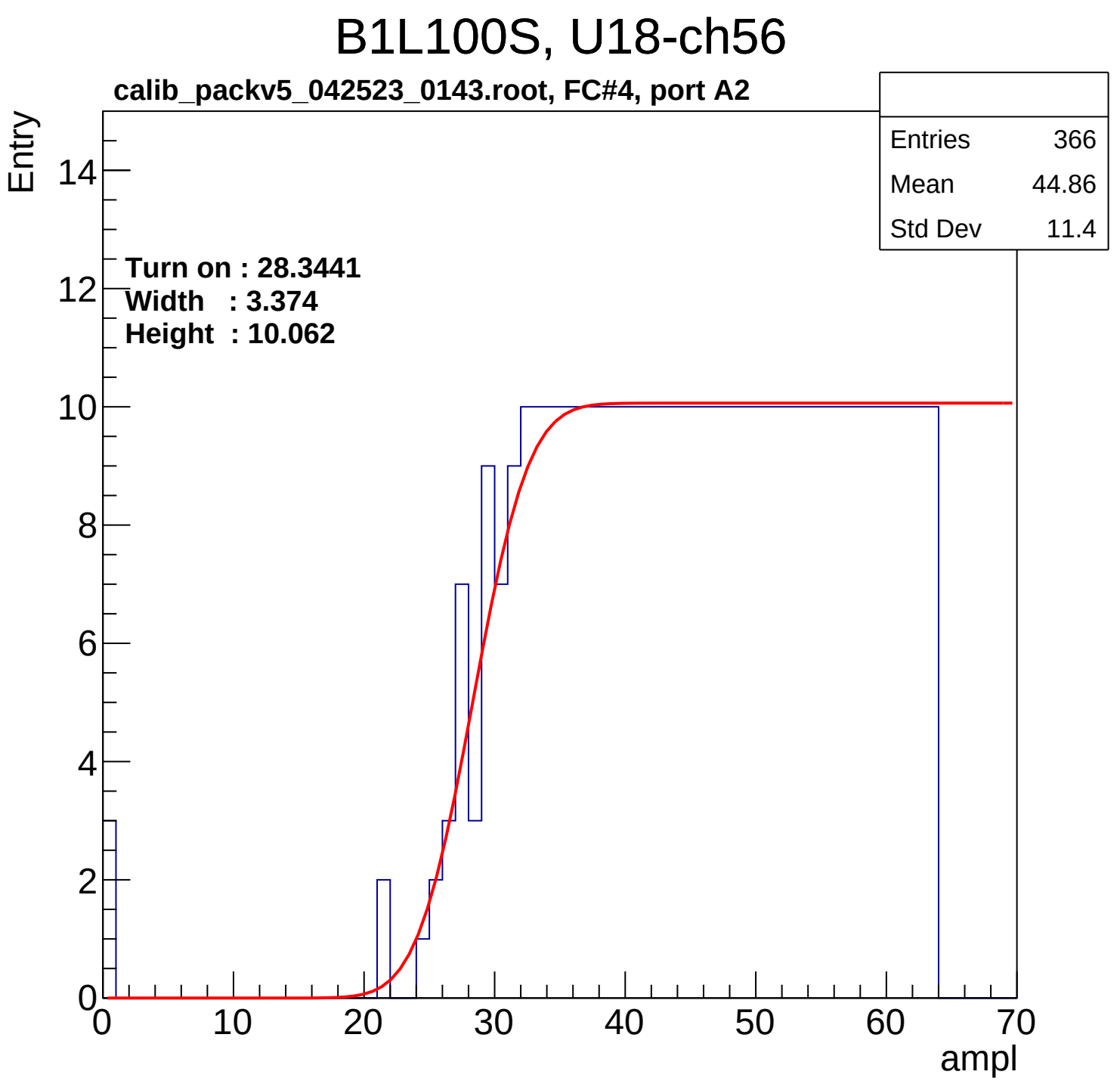
B1L100S, U18-ch56
calib_packv5_042523_0143.root, FC#4, port A2
Entries 366
Mean 44.86
Std Dev 11.4
Turn on : 28.3441
Width : 3.374
Height : 10.062
Entry
ampl
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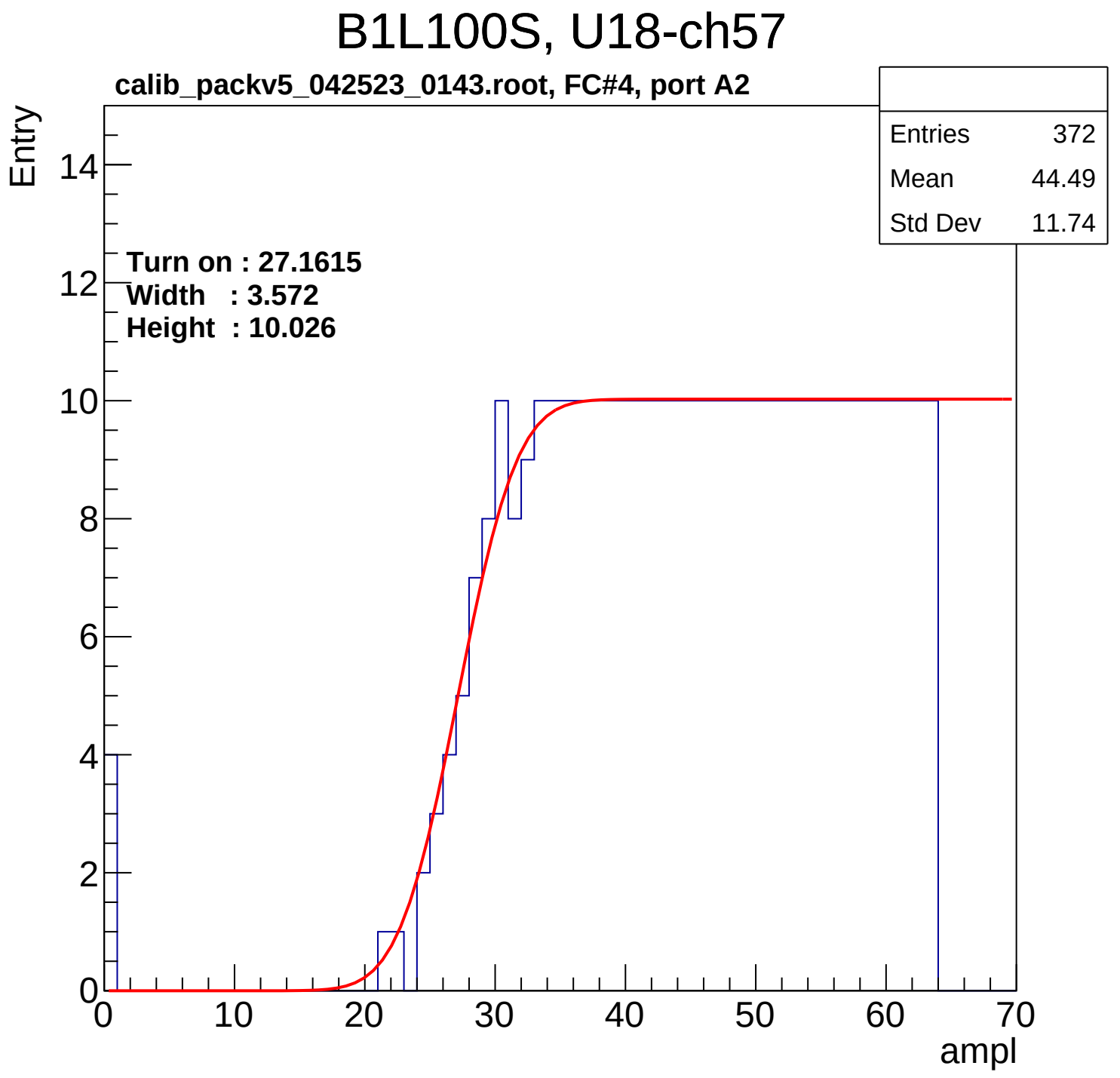
B1L100S, U18-ch57
calib_packv5_042523_0143.root, FC#4, port A2
Entries 372
Mean 44.49
Std Dev 11.74
Turn on : 27.1615
Width : 3.572
Height : 10.026
Entry
ampl
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6
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20
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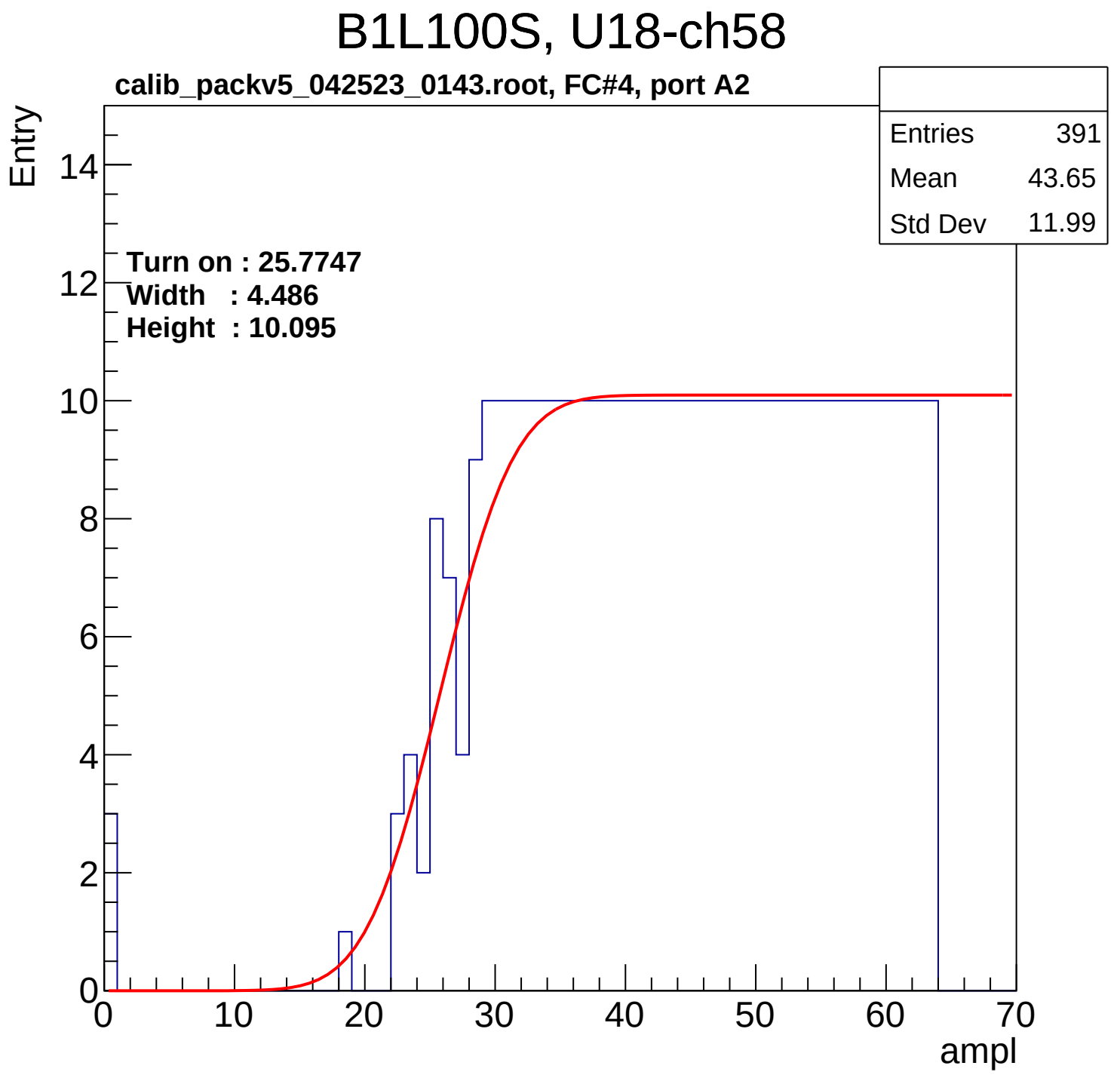
B1L100S, U18-ch58
calib_packv5_042523_0143.root, FC#4, port A2
Entries 391
Mean 43.65
Std Dev 11.99
Turn on : 25.7747
Width : 4.486
Height : 10.095
Entry
ampl
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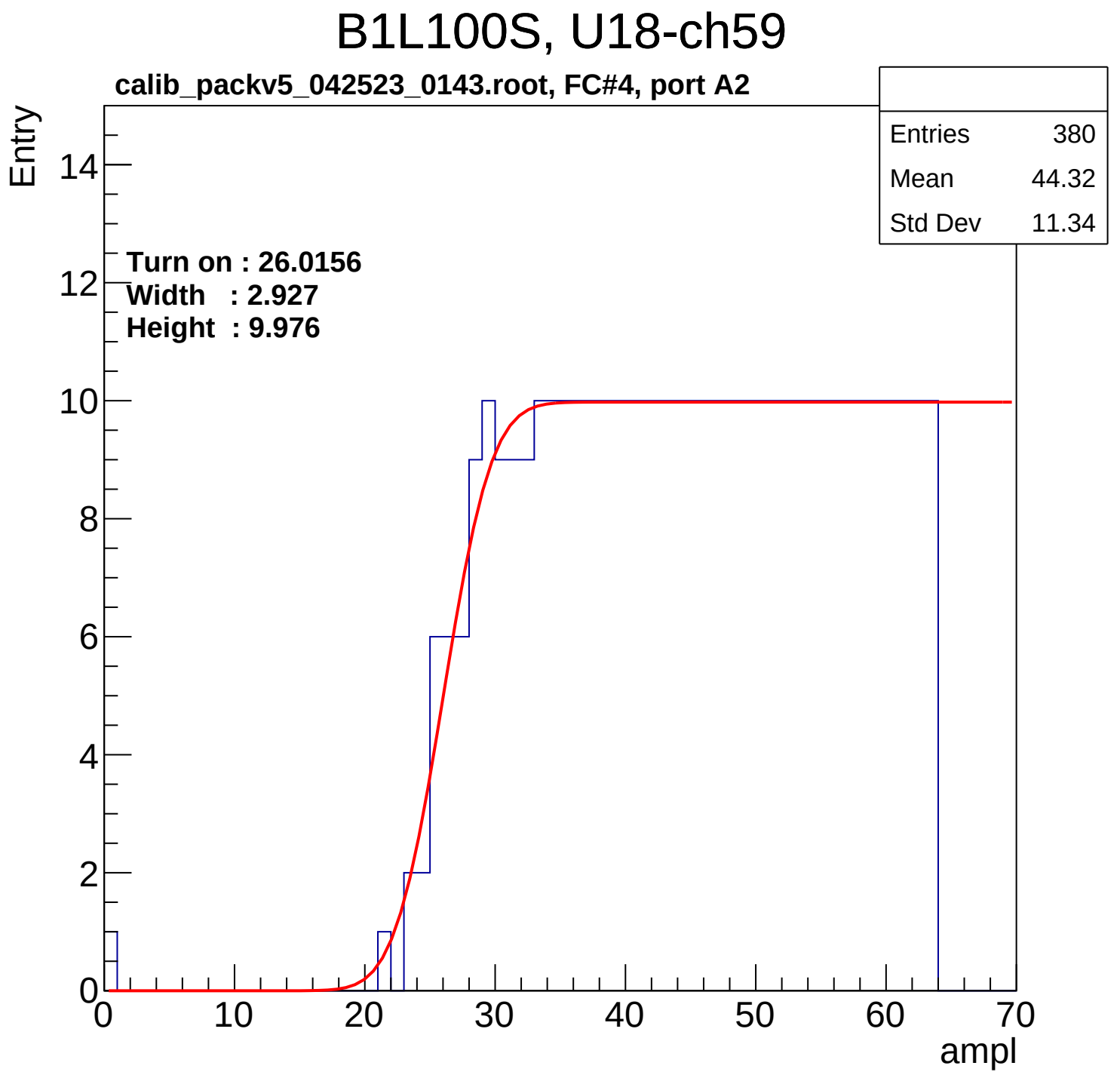
B1L100S, U18-ch59
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.32
Std Dev 11.34
Turn on : 26.0156
Width : 2.927
Height : 9.976
Entry
ampl
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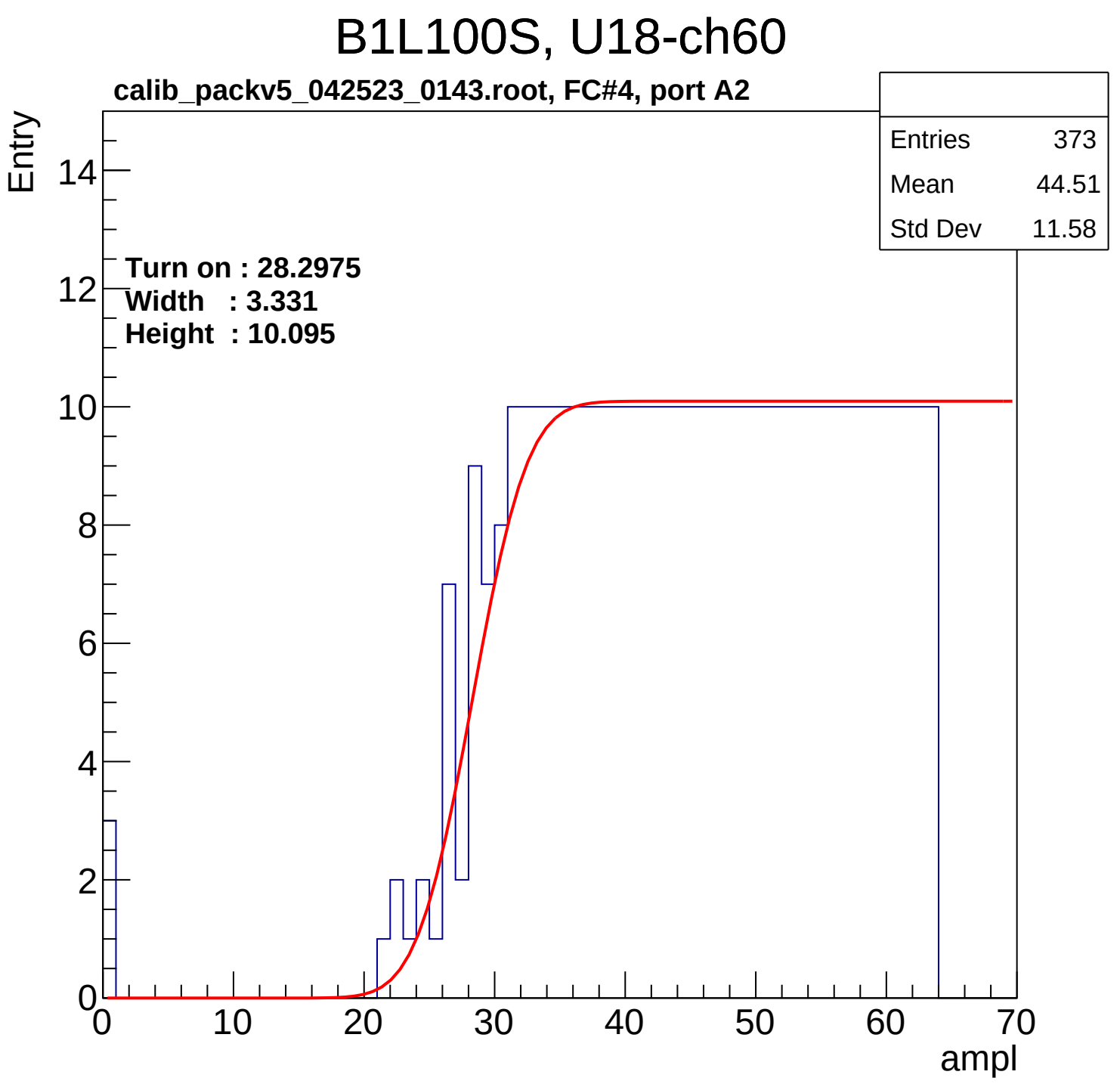
B1L100S, U18-ch60
calib_packv5_042523_0143.root, FC#4, port A2
Entries 373
Mean 44.51
Std Dev 11.58
Turn on : 28.2975
Width : 3.331
Height : 10.095
Entry
ampl
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2
4
6
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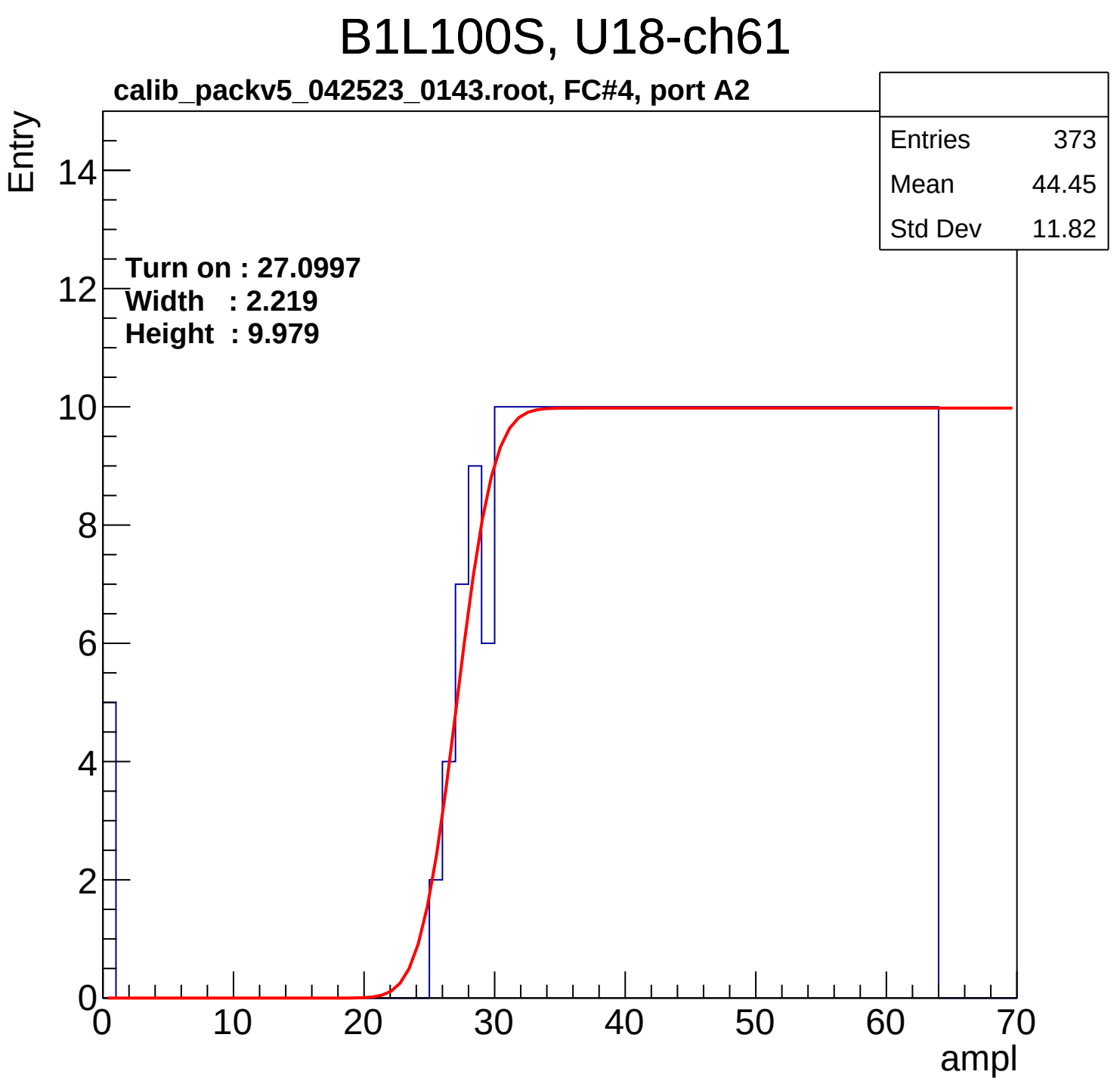
B1L100S, U18-ch61
calib_packv5_042523_0143.root, FC#4, port A2
Entries 373
Mean 44.45
Std Dev 11.82
Turn on : 27.0997
Width : 2.219
Height : 9.979
Entry
ampl
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2
4
6
8
10
12
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0
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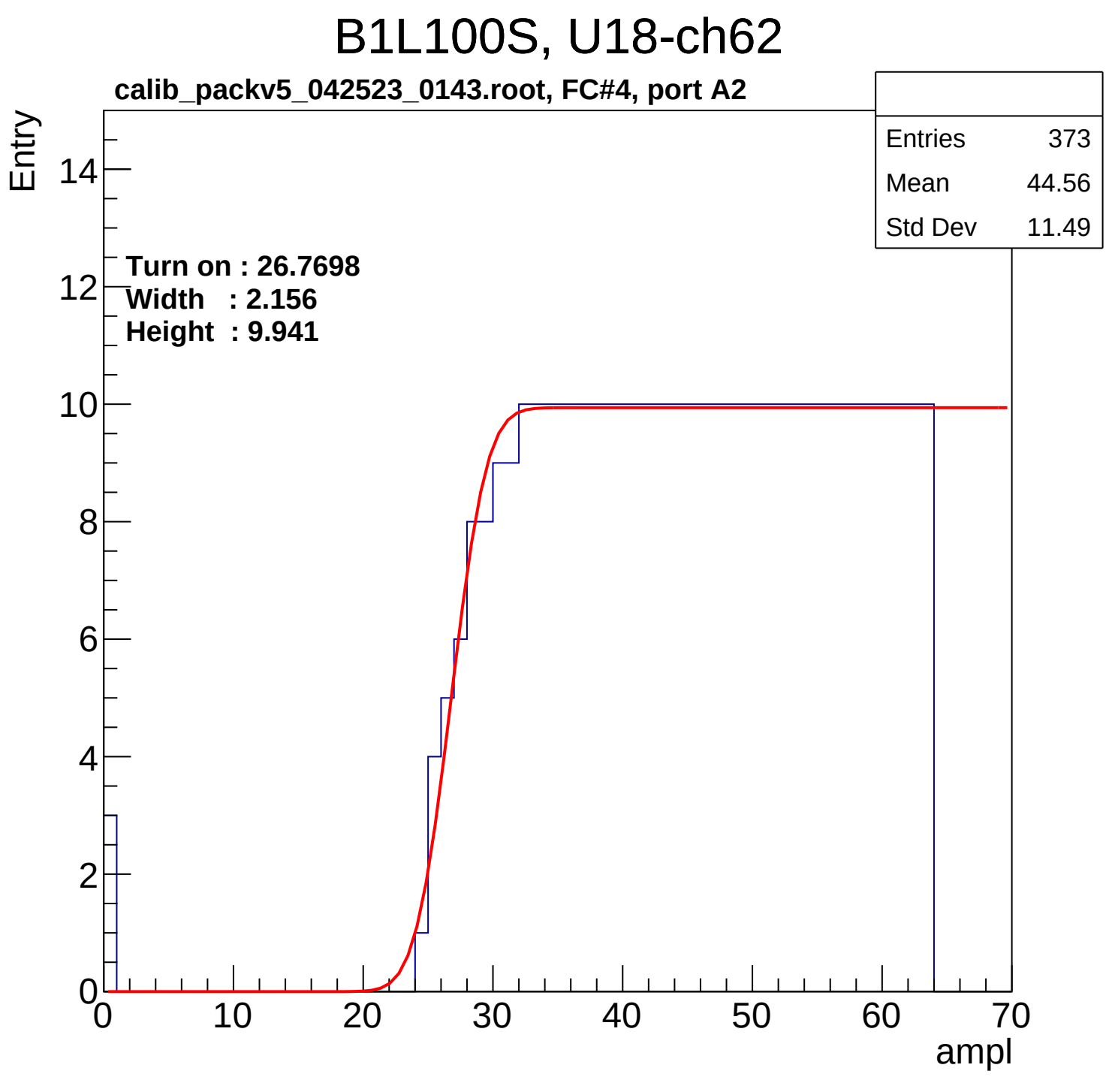
B1L100S, U18-ch62
calib_packv5_042523_0143.root, FC#4, port A2
Entries 373
Mean 44.56
Std Dev 11.49
Turn on : 26.7698
Width : 2.156
Height : 9.941
Entry
ampl
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2
4
6
8
10
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14
0
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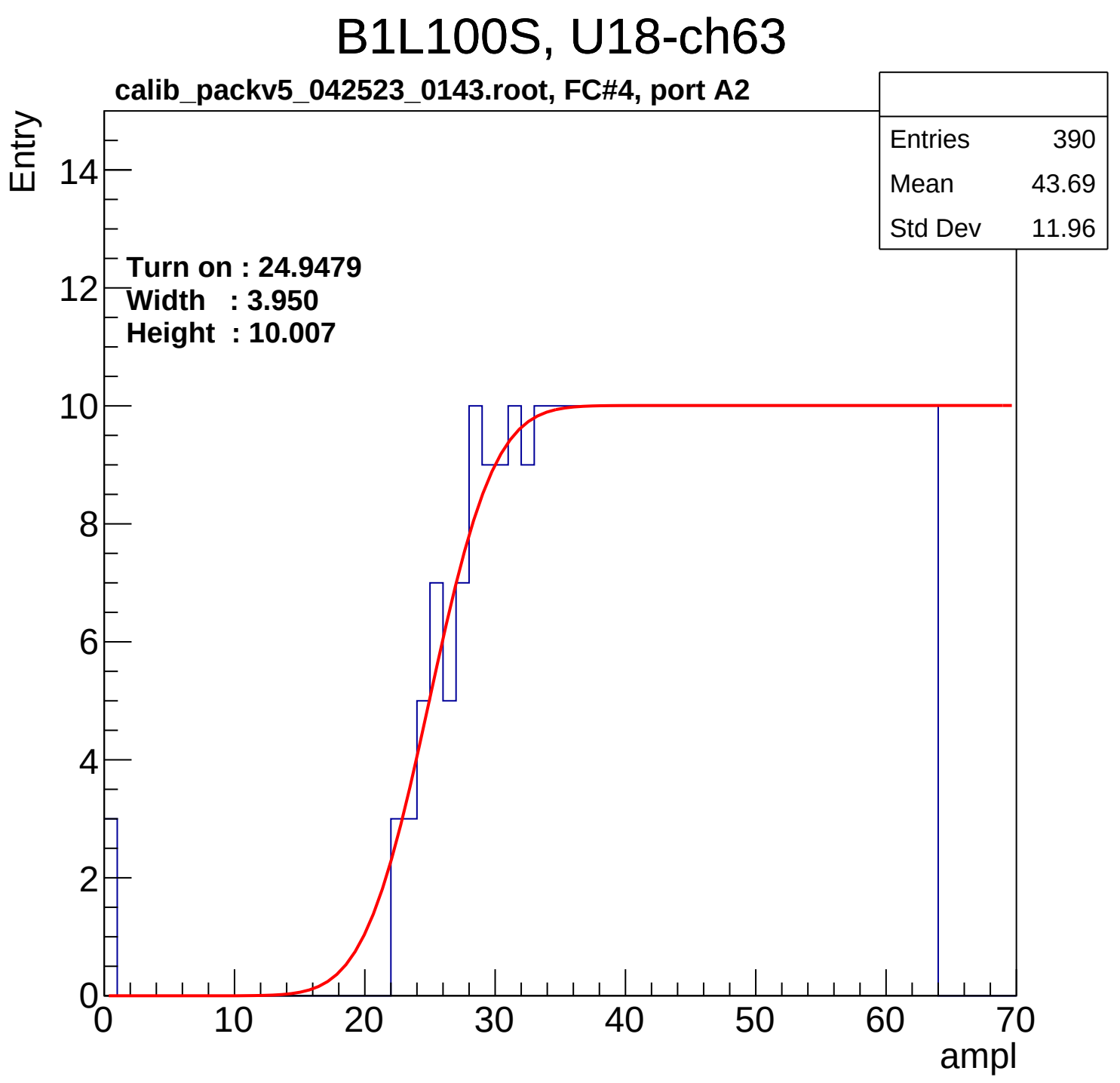
B1L100S, U18-ch63
calib_packv5_042523_0143.root, FC#4, port A2
Entries 390
Mean 43.69
Std Dev 11.96
Turn on : 24.9479
Width : 3.950
Height : 10.007
Entry
ampl
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2
4
6
8
10
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0
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60
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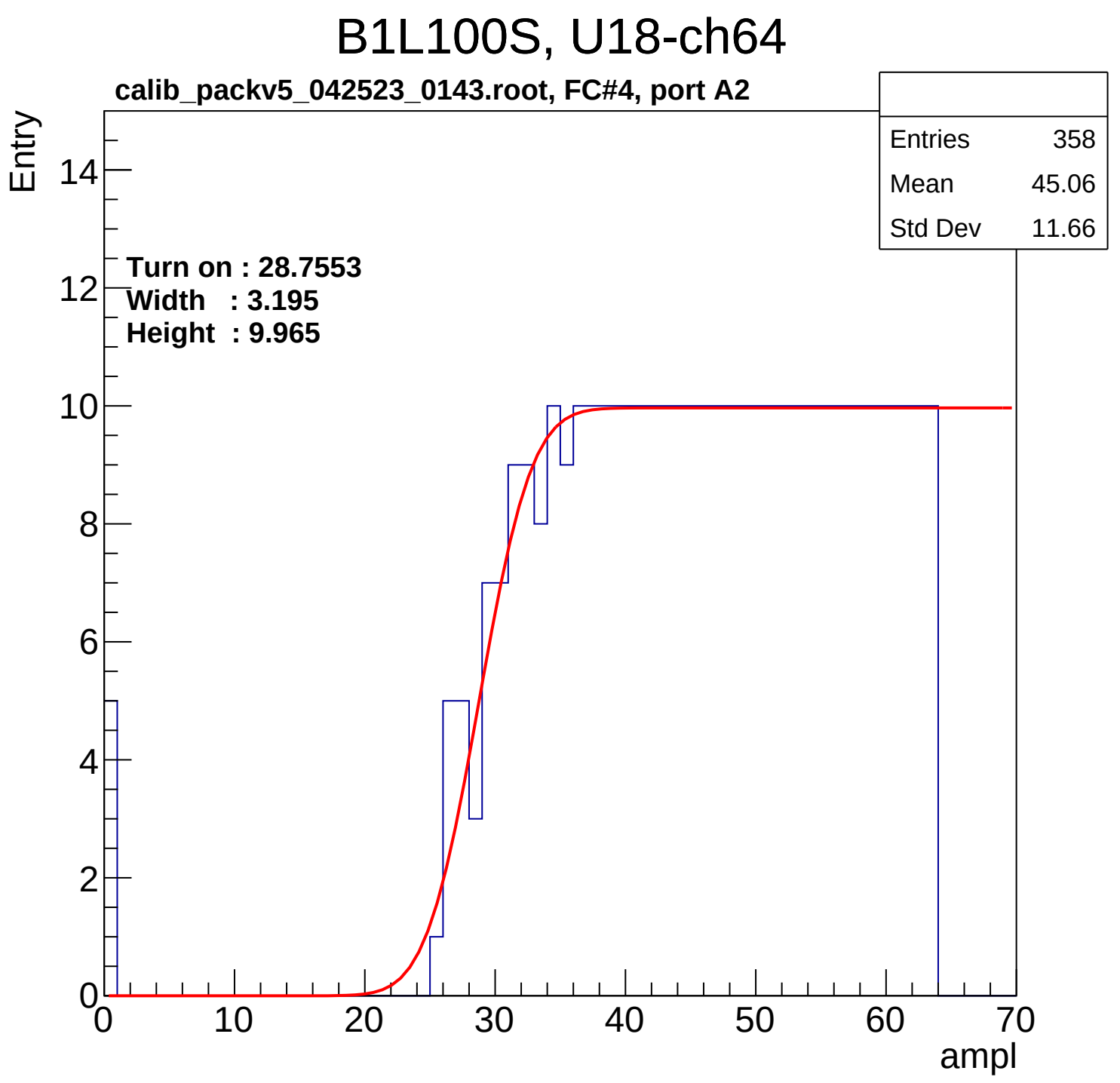
B1L100S, U18-ch64
calib_packv5_042523_0143.root, FC#4, port A2
Entries 358
Mean 45.06
Std Dev 11.66
Turn on : 28.7553
Width : 3.195
Height : 9.965
Entry
ampl
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2
4
6
8
10
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0
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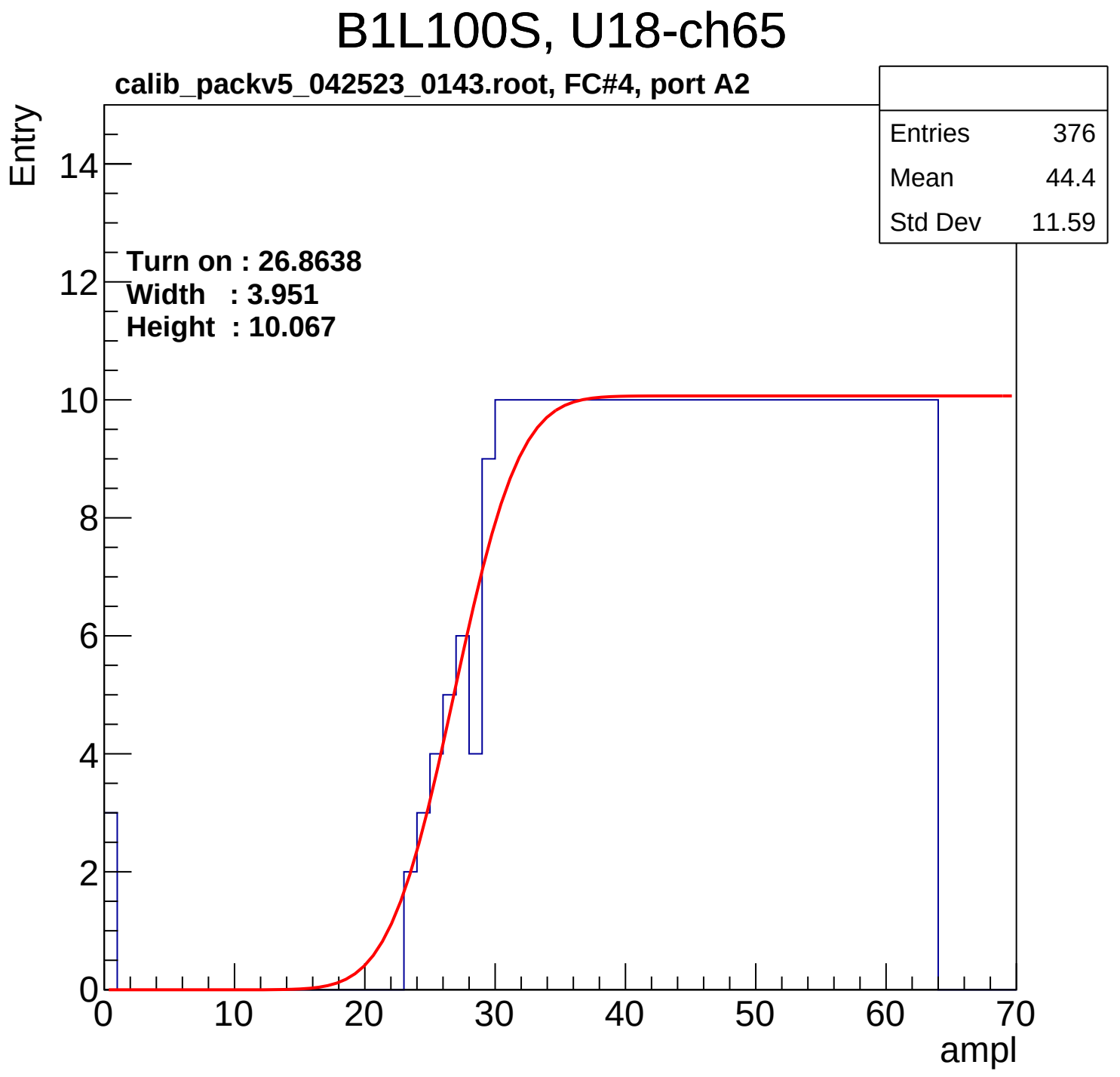
B1L100S, U18-ch65
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.4
Std Dev 11.59
Turn on : 26.8638
Width : 3.951
Height : 10.067
Entry
ampl
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2
4
6
8
10
12
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0
10
20
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40
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60
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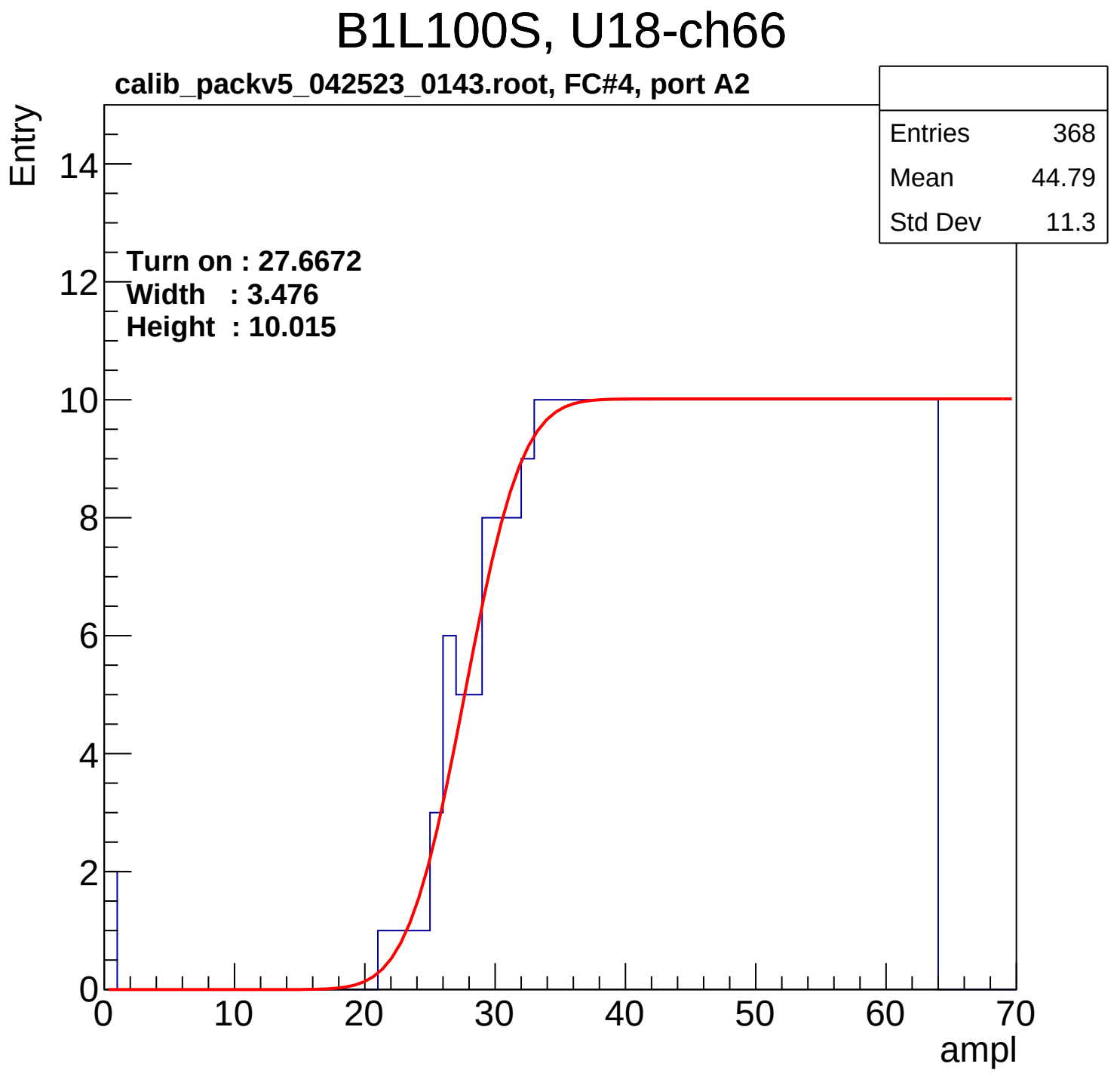
B1L100S, U18-ch66
calib_packv5_042523_0143.root, FC#4, port A2
Entries 368
Mean 44.79
Std Dev 11.3
Turn on : 27.6672
Width : 3.476
Height : 10.015
Entry
ampl
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4
6
8
10
12
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0
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40
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60
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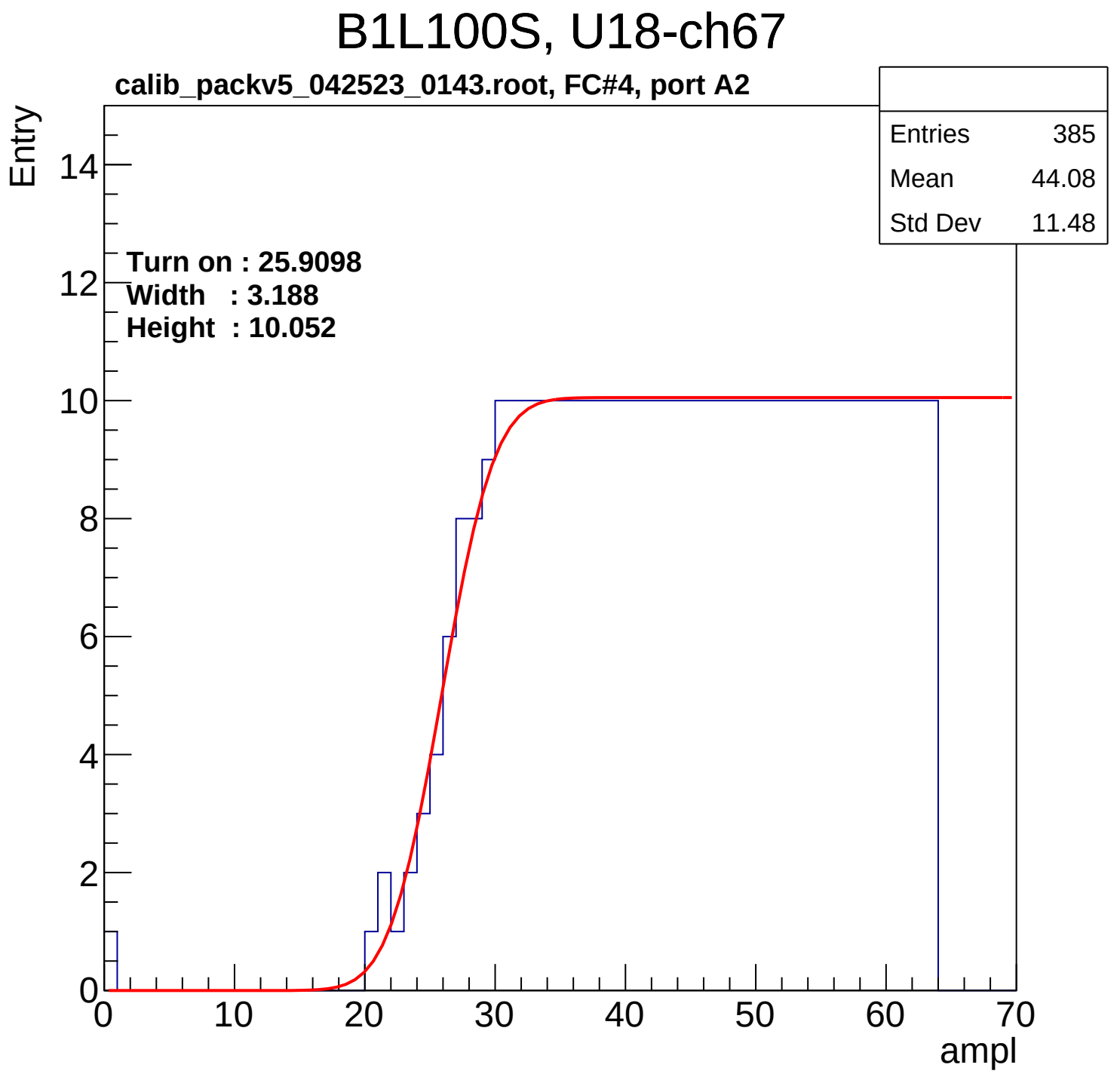
B1L100S, U18-ch67
calib_packv5_042523_0143.root, FC#4, port A2
Entries 385
Mean 44.08
Std Dev 11.48
Turn on : 25.9098
Width : 3.188
Height : 10.052
Entry
ampl
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2
4
6
8
10
12
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0
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20
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60
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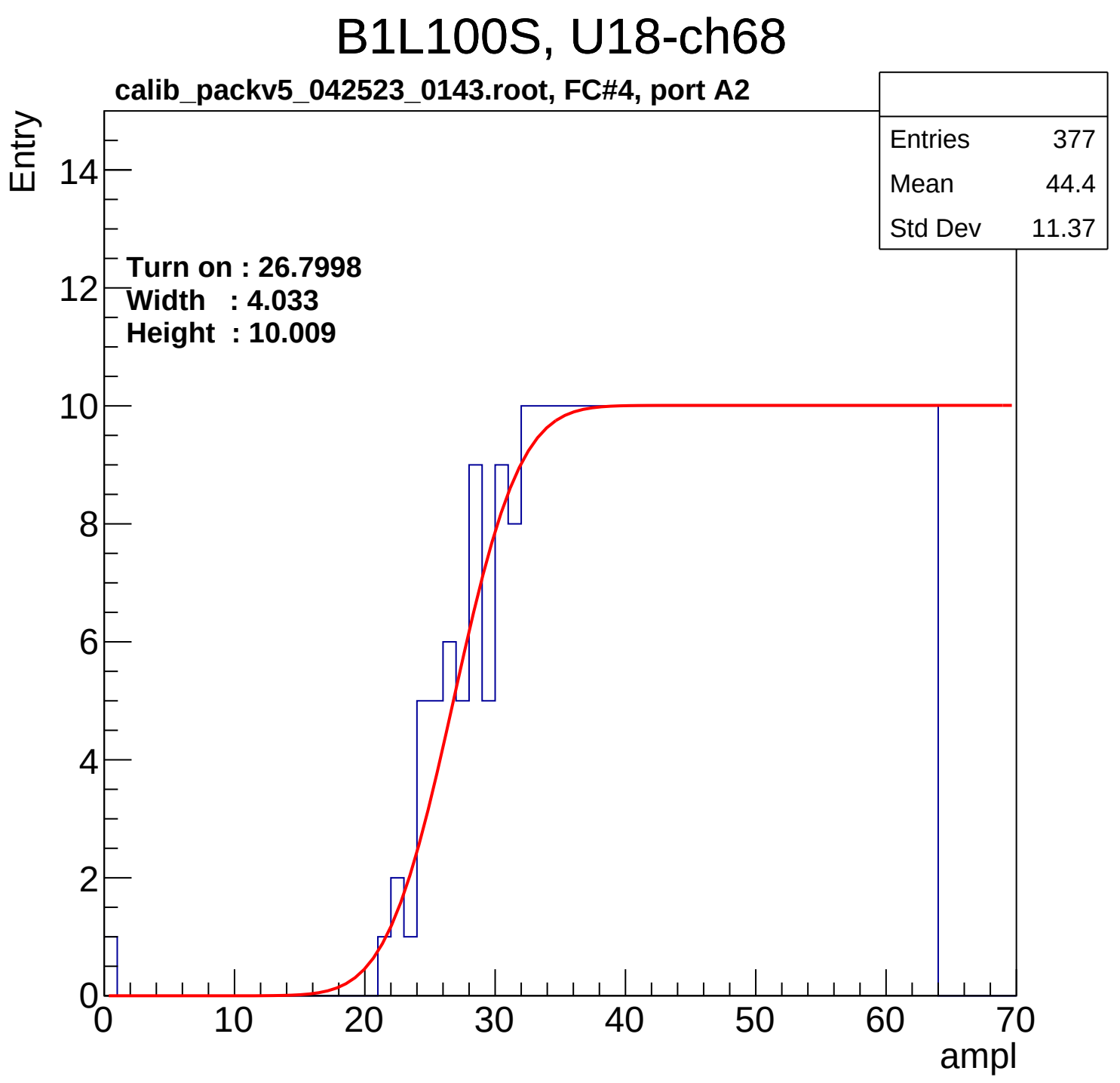
B1L100S, U18-ch68
calib_packv5_042523_0143.root, FC#4, port A2
Entries 377
Mean 44.4
Std Dev 11.37
Turn on : 26.7998
Width : 4.033
Height : 10.009
Entry
ampl
0
2
4
6
8
10
12
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0
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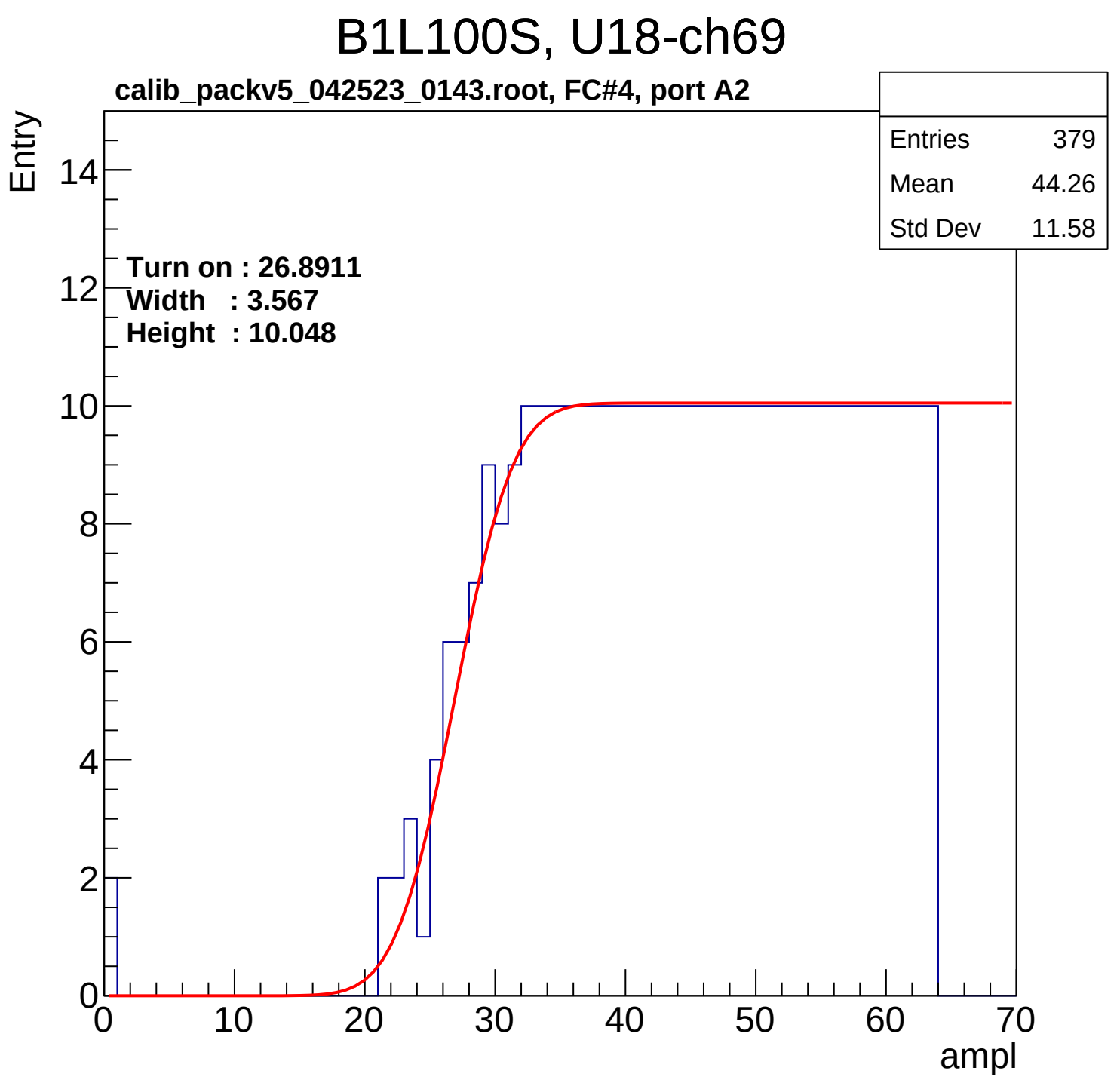
B1L100S, U18-ch69
calib_packv5_042523_0143.root, FC#4, port A2
Entries 379
Mean 44.26
Std Dev 11.58
Turn on : 26.8911
Width : 3.567
Height : 10.048
Entry
ampl
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4
6
8
10
12
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0
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20
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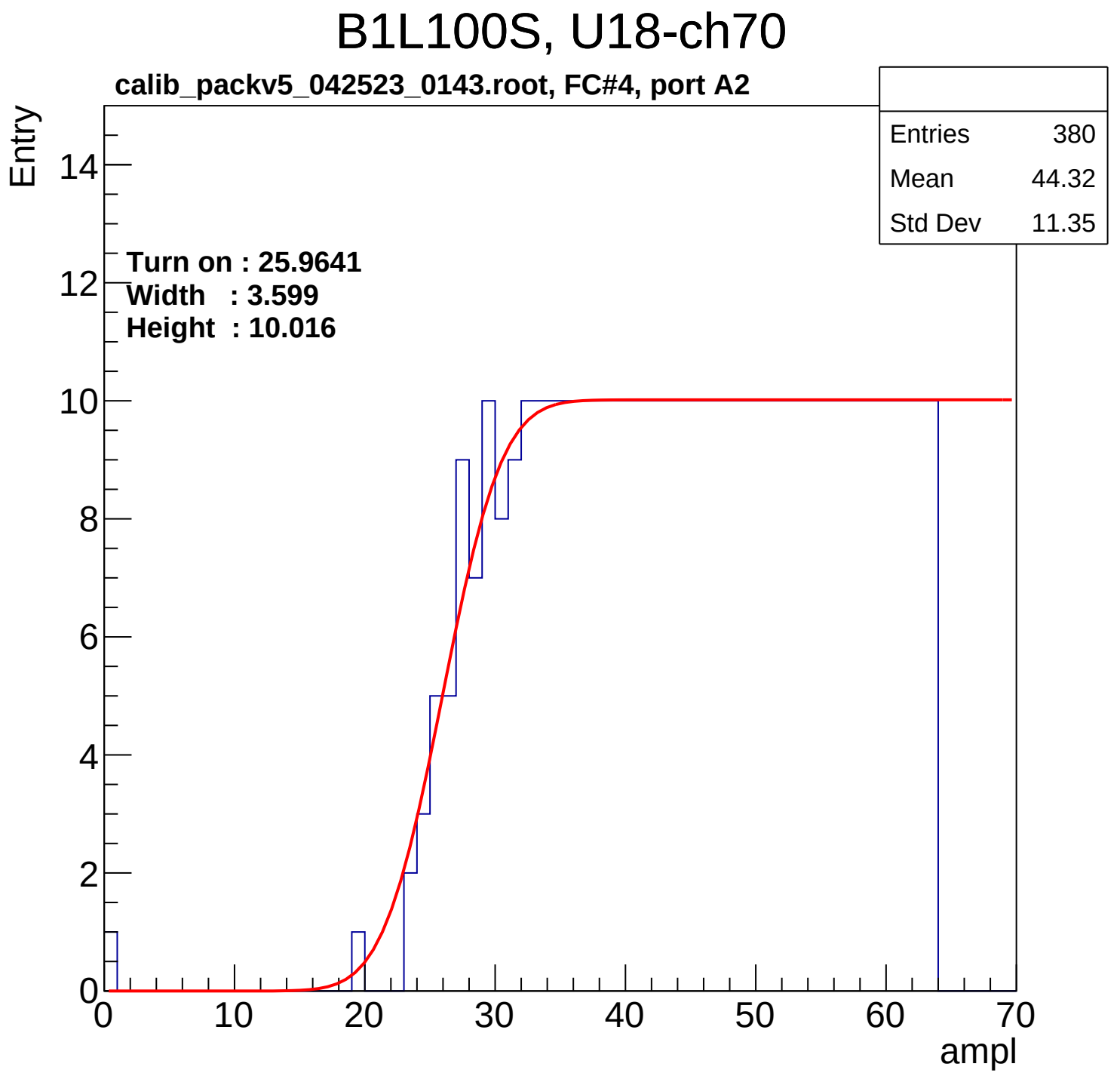
B1L100S, U18-ch70
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.32
Std Dev 11.35
Turn on : 25.9641
Width : 3.599
Height : 10.016
Entry
ampl
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6
8
10
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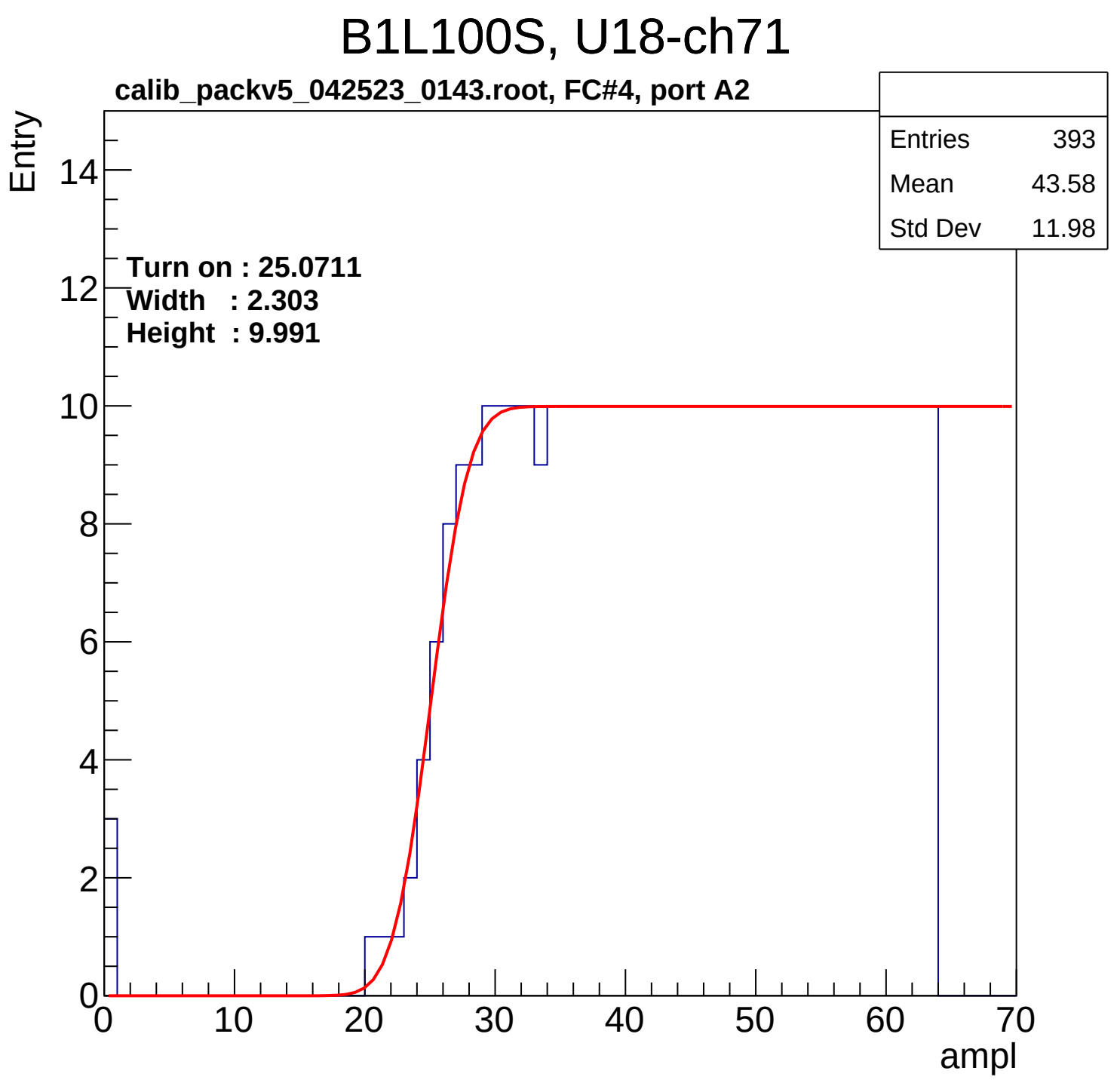
B1L100S, U18-ch71
calib_packv5_042523_0143.root, FC#4, port A2
Entries 393
Mean 43.58
Std Dev 11.98
Turn on : 25.0711
Width : 2.303
Height : 9.991
Entry
ampl
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6
8
10
12
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0
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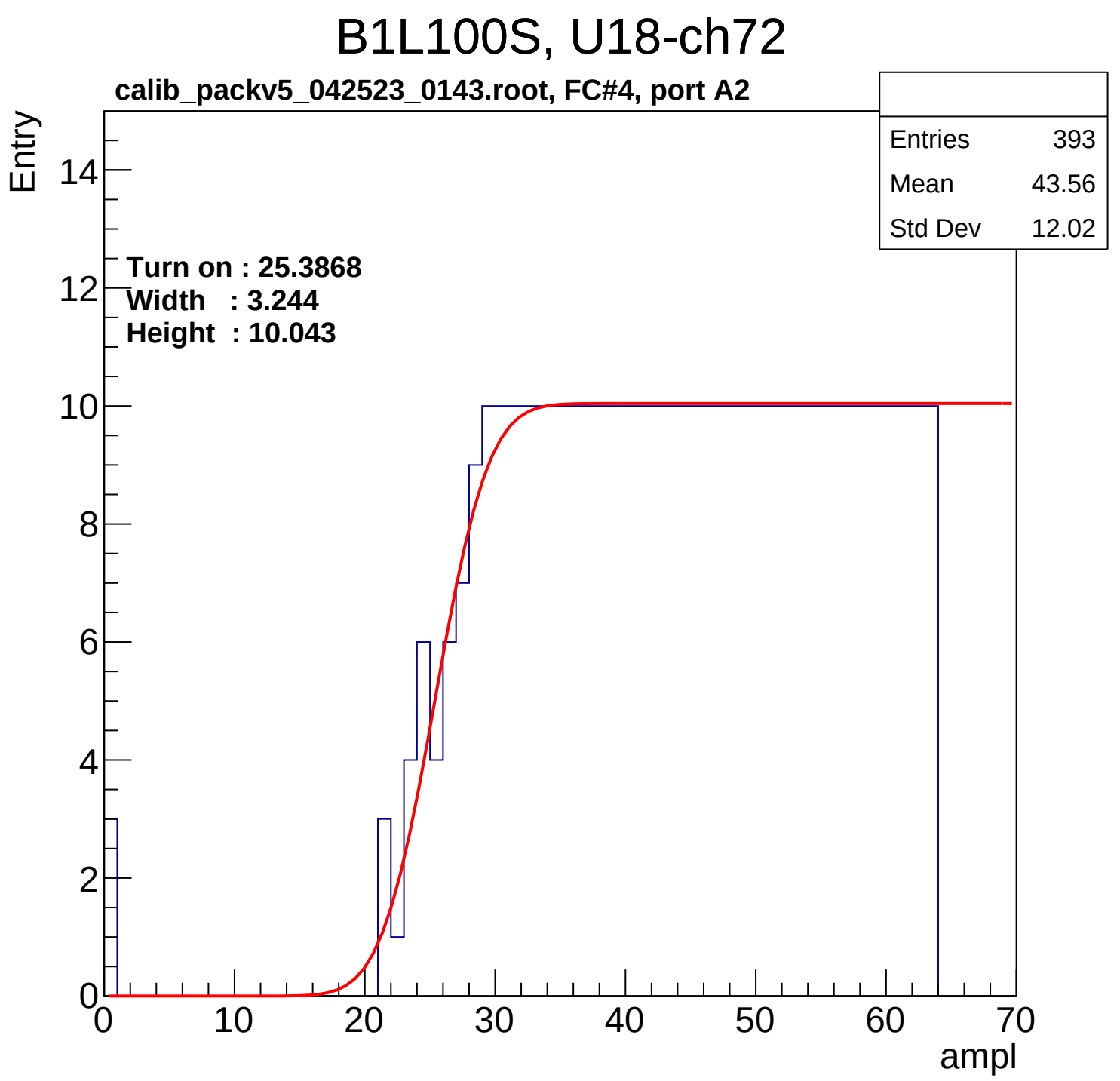
B1L100S, U18-ch72
calib_packv5_042523_0143.root, FC#4, port A2
Entries 393
Mean 43.56
Std Dev 12.02
Turn on : 25.3868
Width : 3.244
Height : 10.043
Entry
ampl
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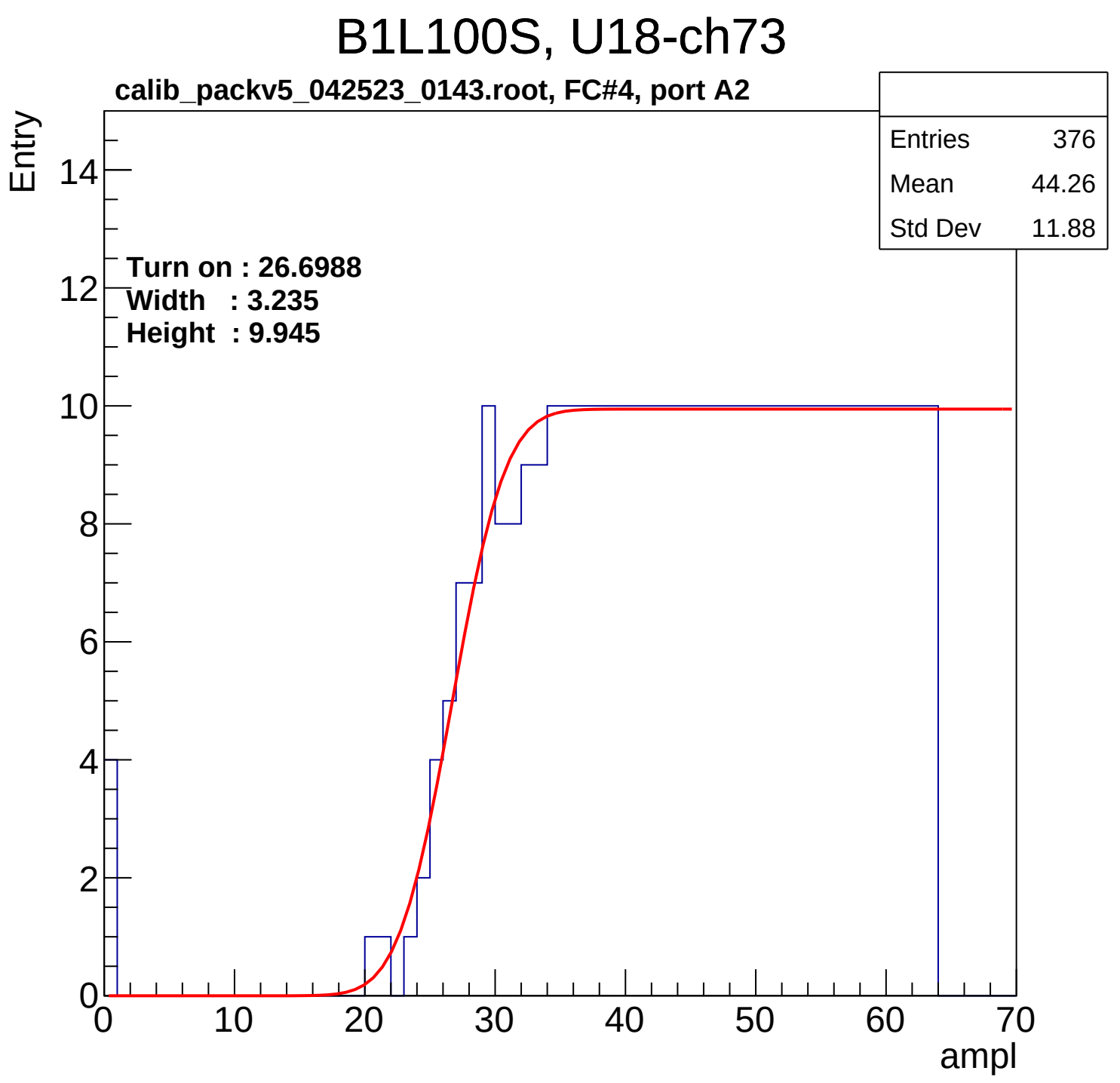
B1L100S, U18-ch73
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.26
Std Dev 11.88
Turn on : 26.6988
Width : 3.235
Height : 9.945
Entry
ampl
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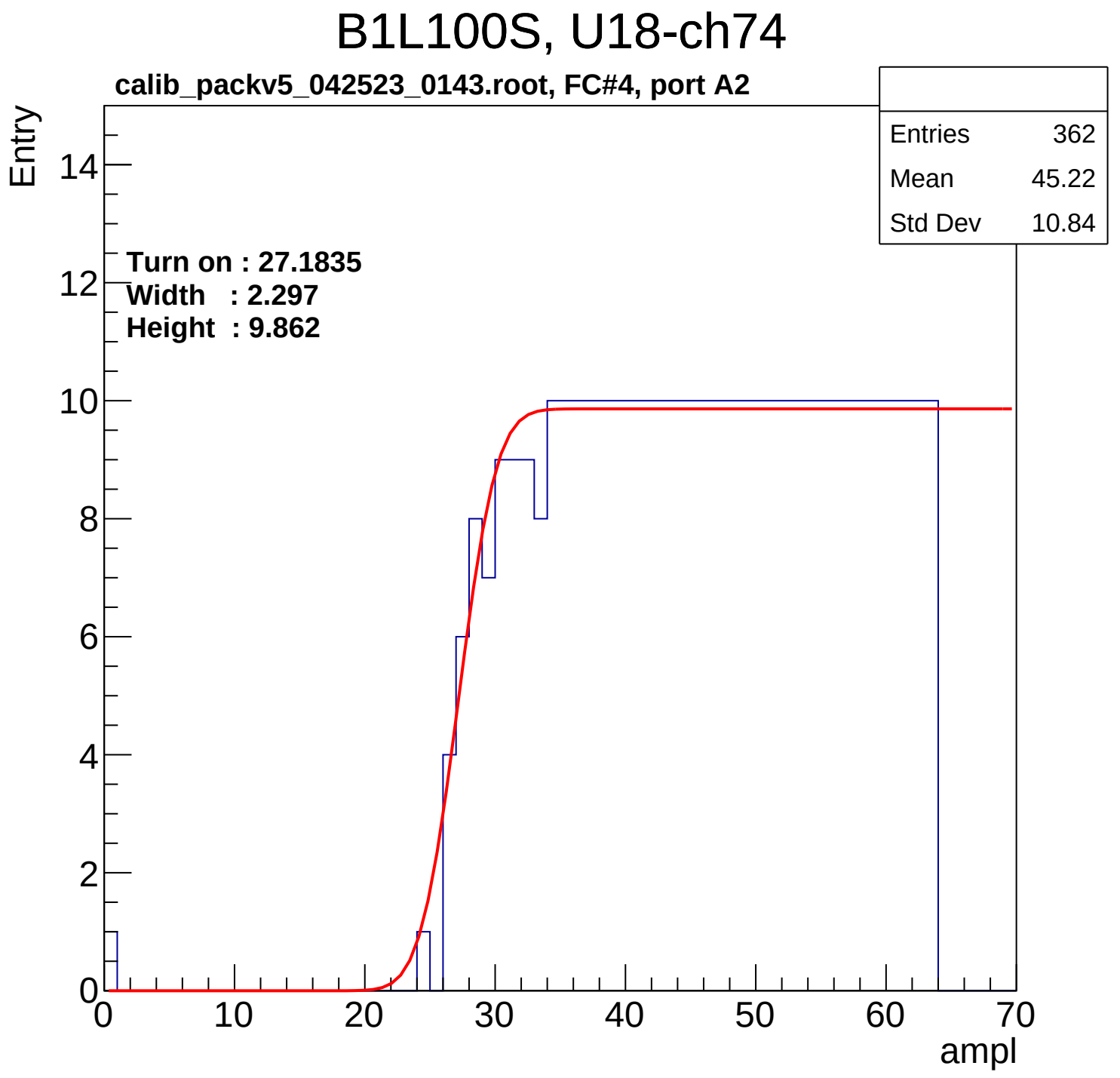
B1L100S, U18-ch74
calib_packv5_042523_0143.root, FC#4, port A2
Entries 362
Mean 45.22
Std Dev 10.84
Turn on : 27.1835
Width : 2.297
Height : 9.862
Entry
ampl
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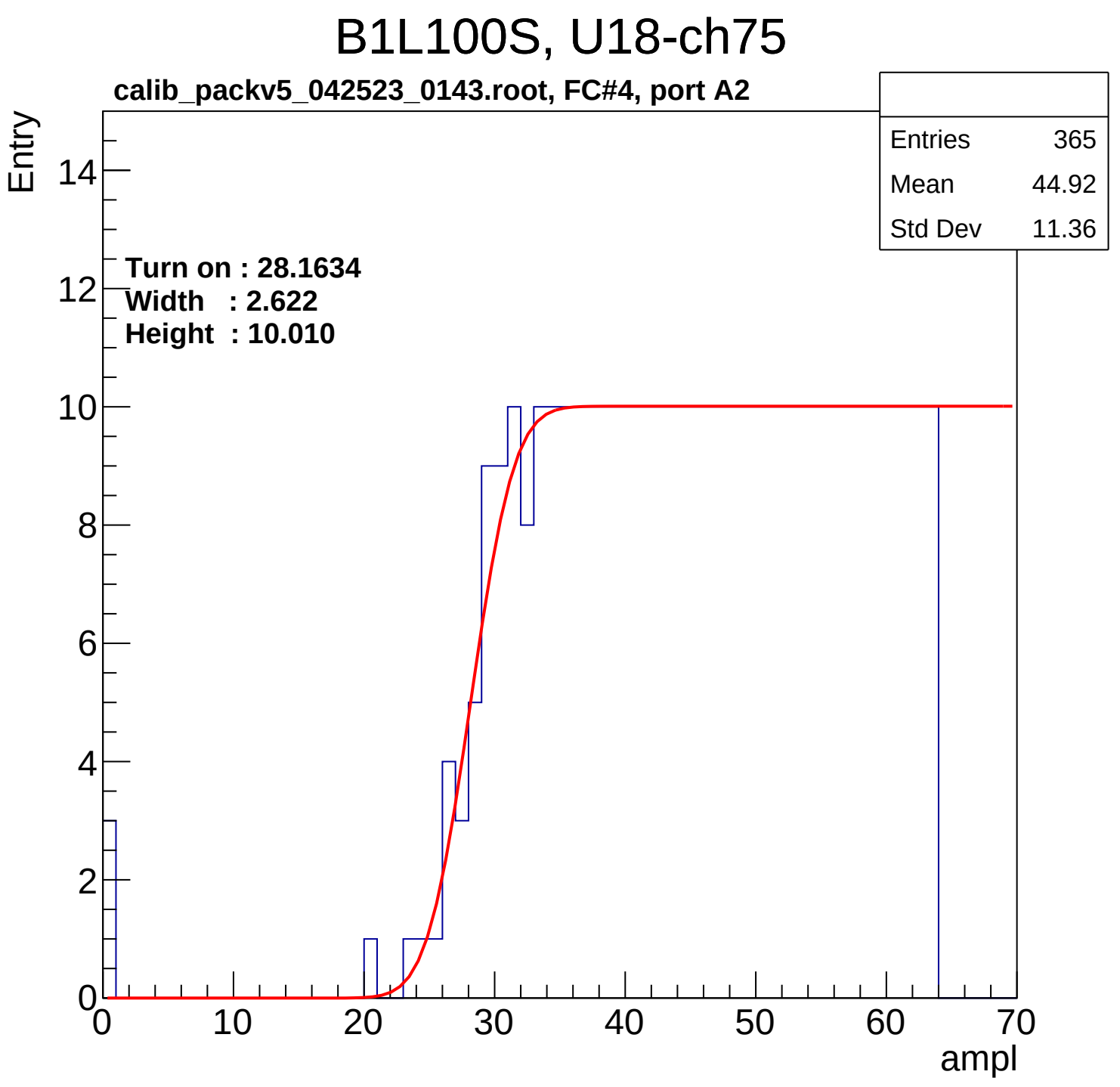
B1L100S, U18-ch75
calib_packv5_042523_0143.root, FC#4, port A2
Entries 365
Mean 44.92
Std Dev 11.36
Turn on : 28.1634
Width : 2.622
Height : 10.010
Entry
ampl
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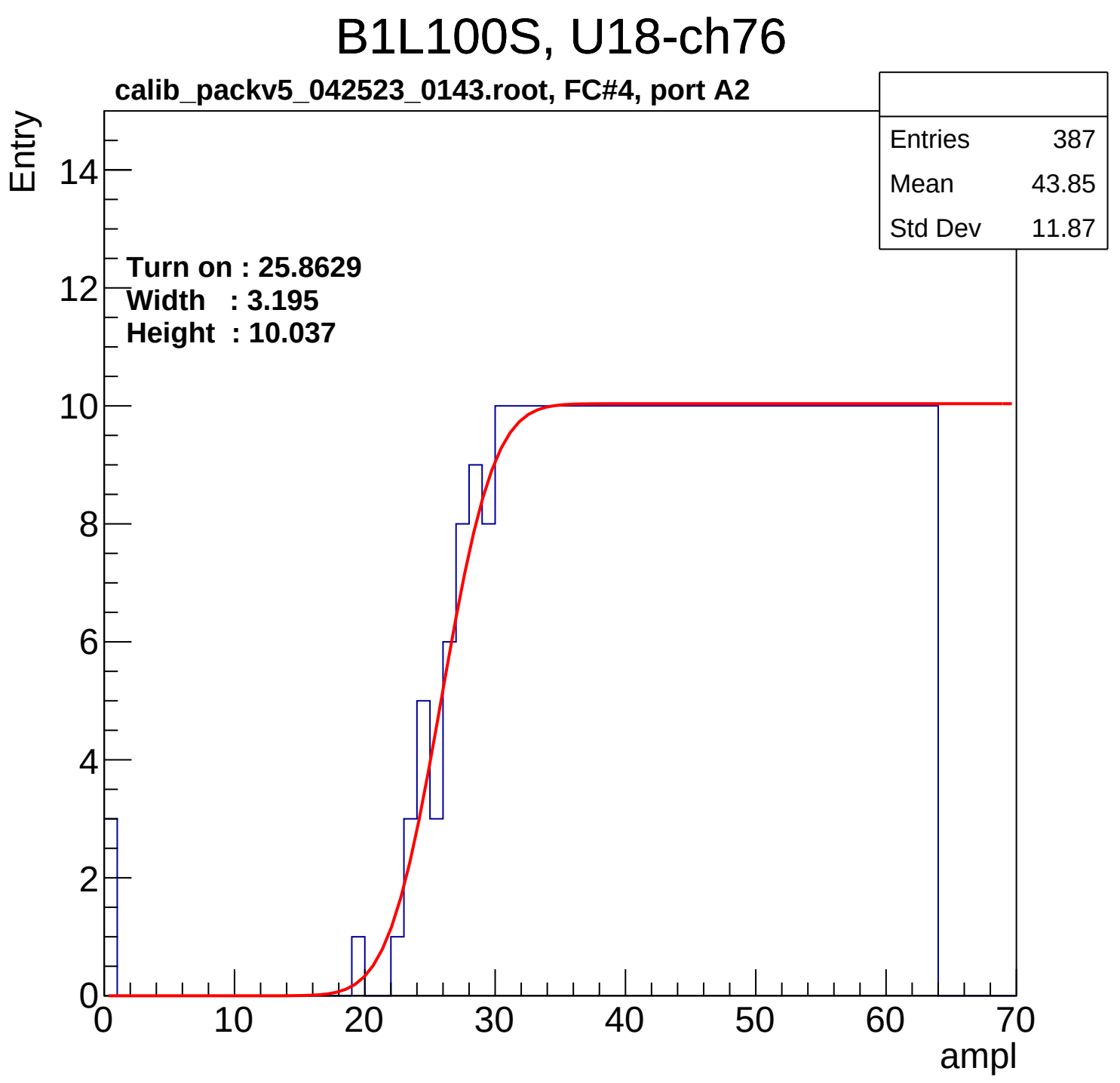
B1L100S, U18-ch76
calib_packv5_042523_0143.root, FC#4, port A2
Entries 387
Mean 43.85
Std Dev 11.87
Turn on : 25.8629
Width : 3.195
Height : 10.037
Entry
ampl
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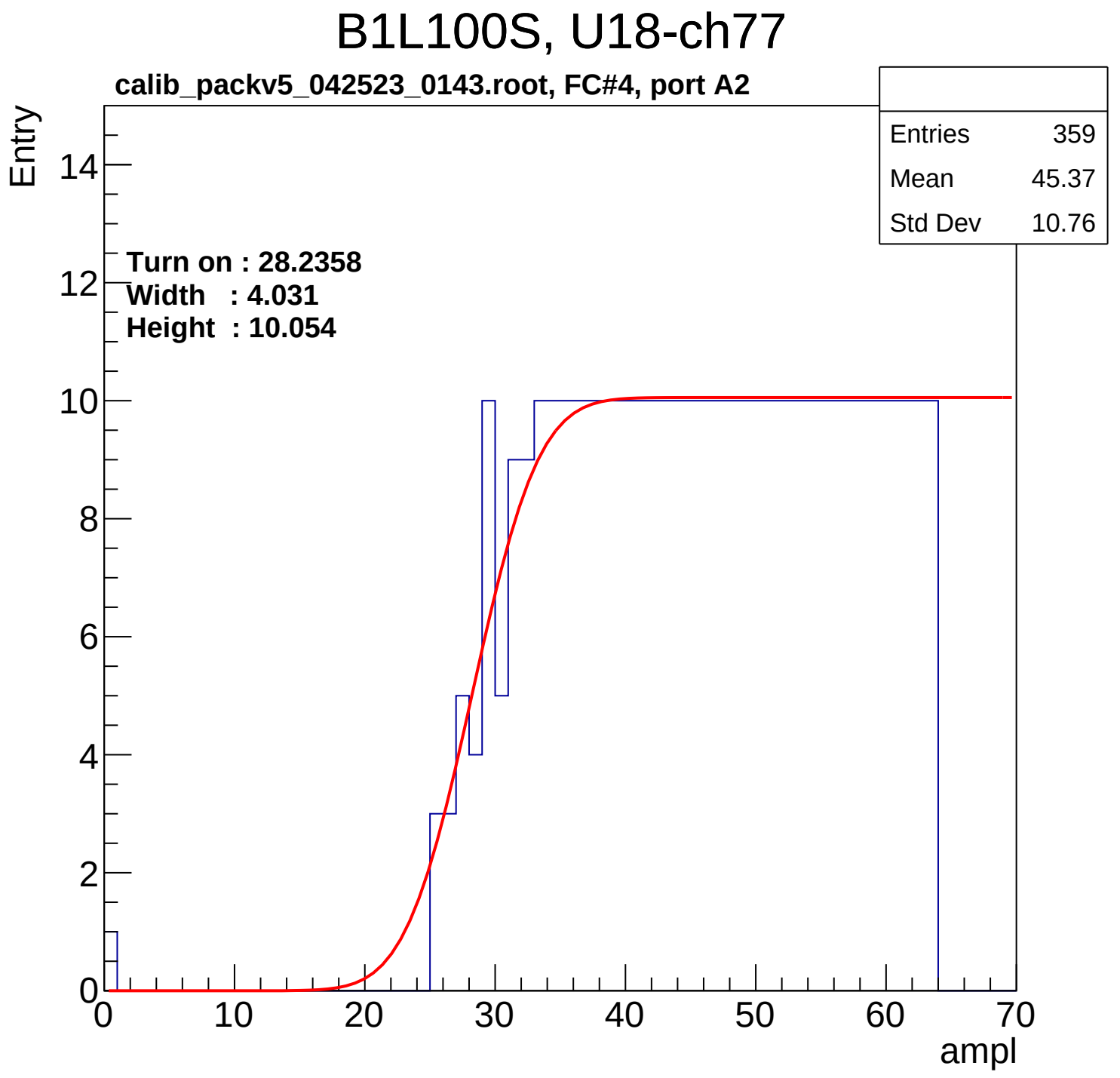
B1L100S, U18-ch77
calib_packv5_042523_0143.root, FC#4, port A2
Entries 359
Mean 45.37
Std Dev 10.76
Turn on : 28.2358
Width : 4.031
Height : 10.054
Entry
ampl
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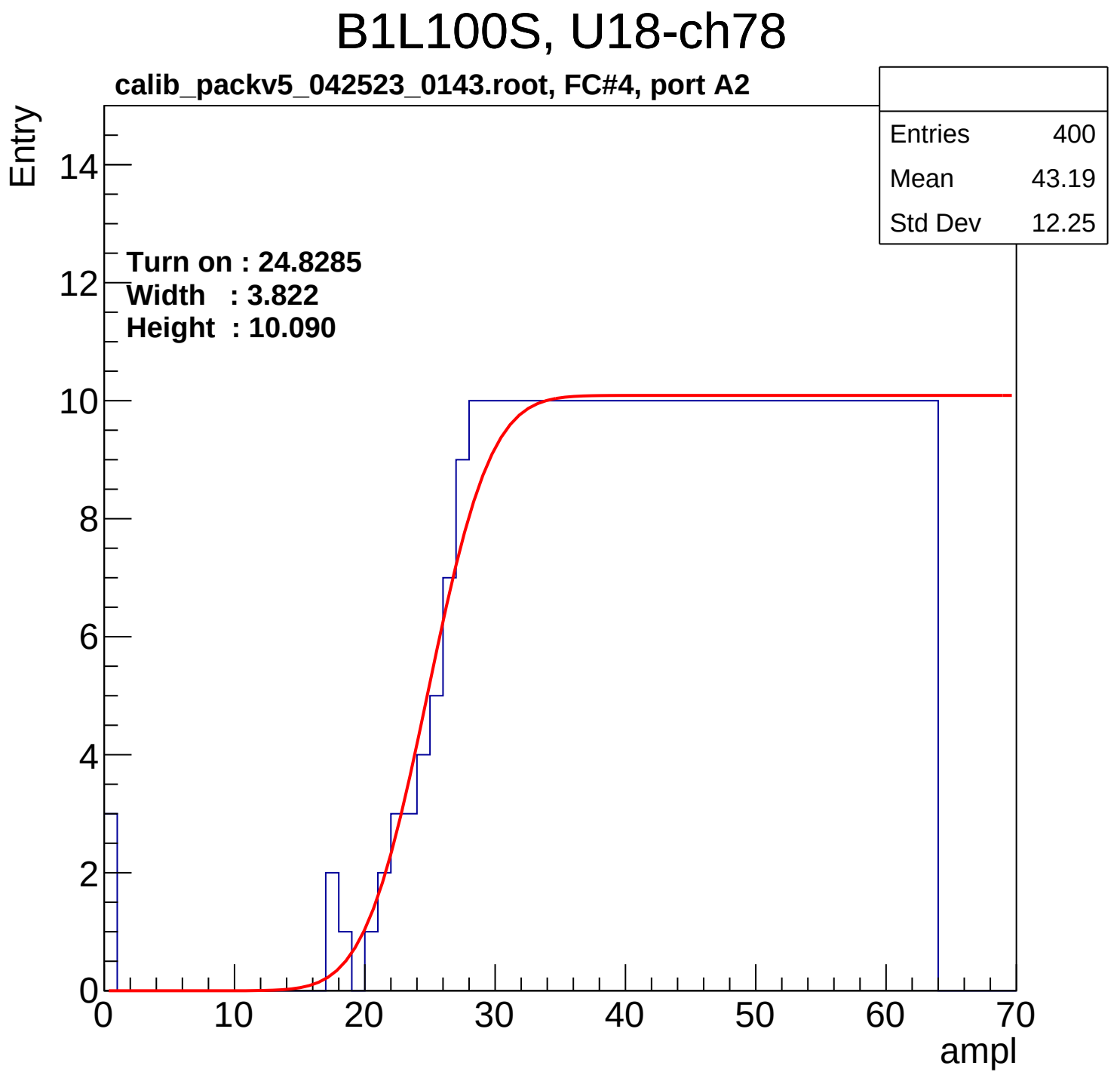
B1L100S, U18-ch78
calib_packv5_042523_0143.root, FC#4, port A2
Entries 400
Mean 43.19
Std Dev 12.25
Turn on : 24.8285
Width : 3.822
Height : 10.090
Entry
ampl
0
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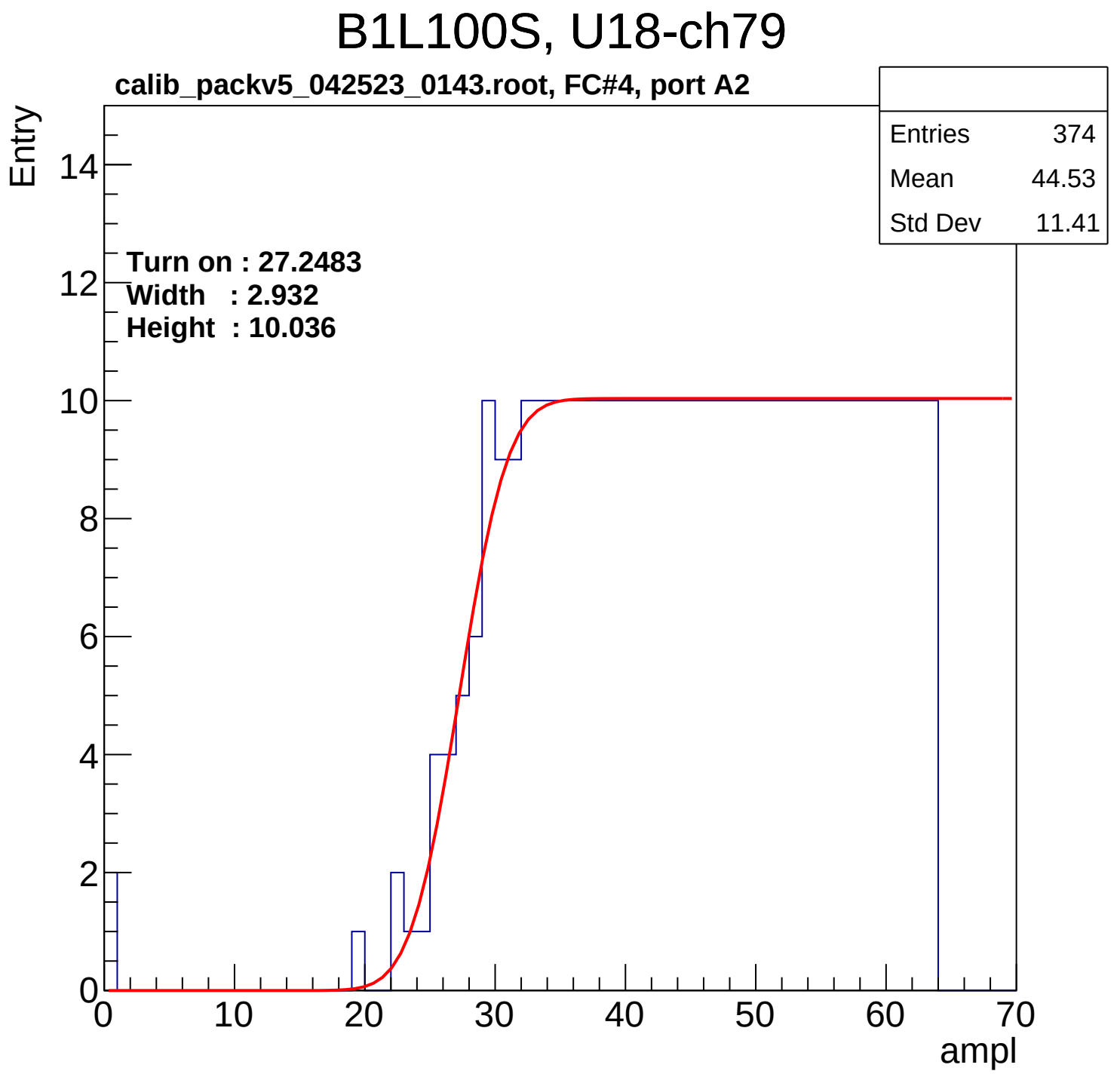
B1L100S, U18-ch79
calib_packv5_042523_0143.root, FC#4, port A2
Entries 374
Mean 44.53
Std Dev 11.41
Turn on : 27.2483
Width : 2.932
Height : 10.036
Entry
ampl
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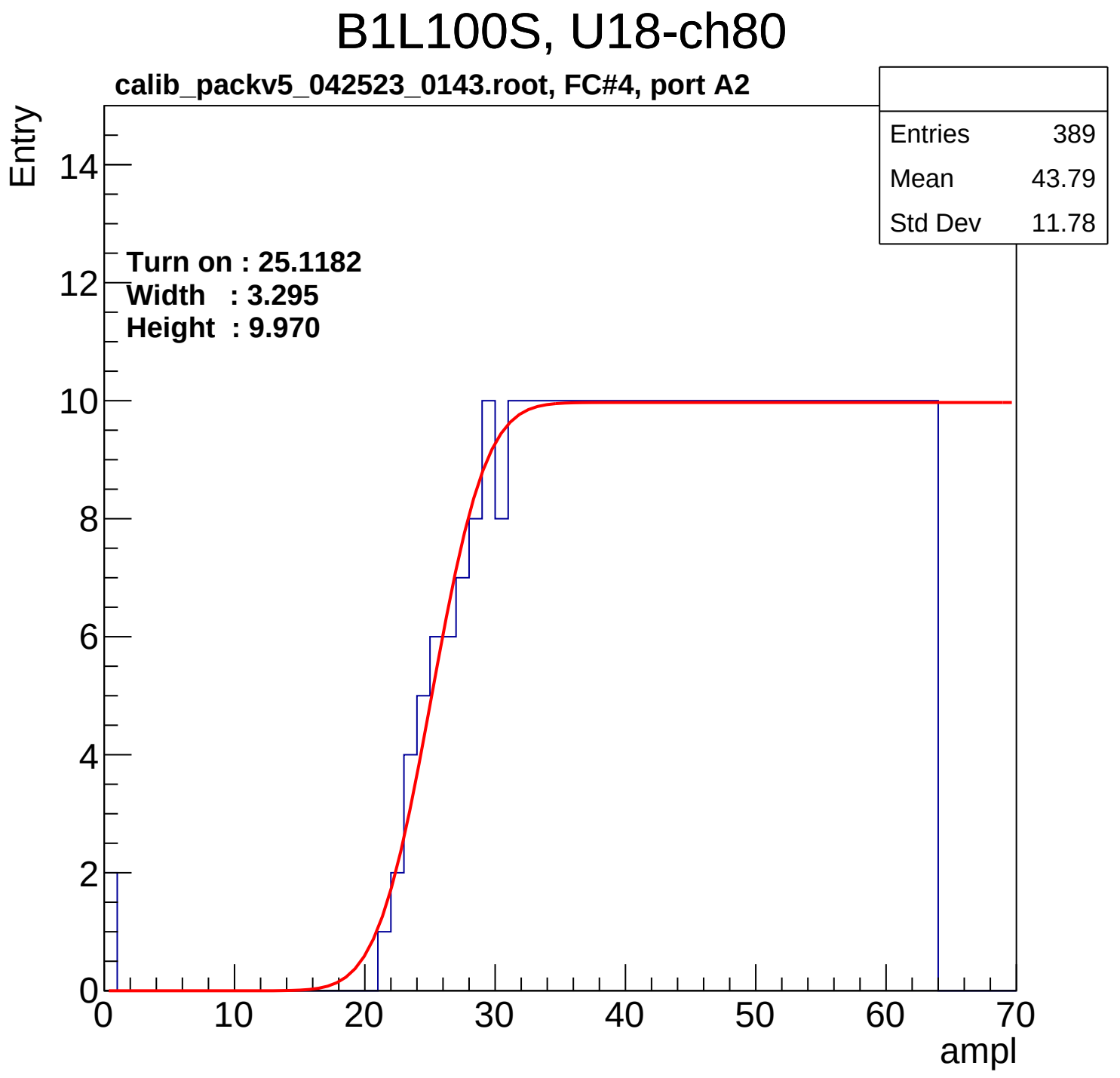
B1L100S, U18-ch80
calib_packv5_042523_0143.root, FC#4, port A2
Entries 389
Mean 43.79
Std Dev 11.78
Turn on : 25.1182
Width : 3.295
Height : 9.970
Entry
ampl
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2
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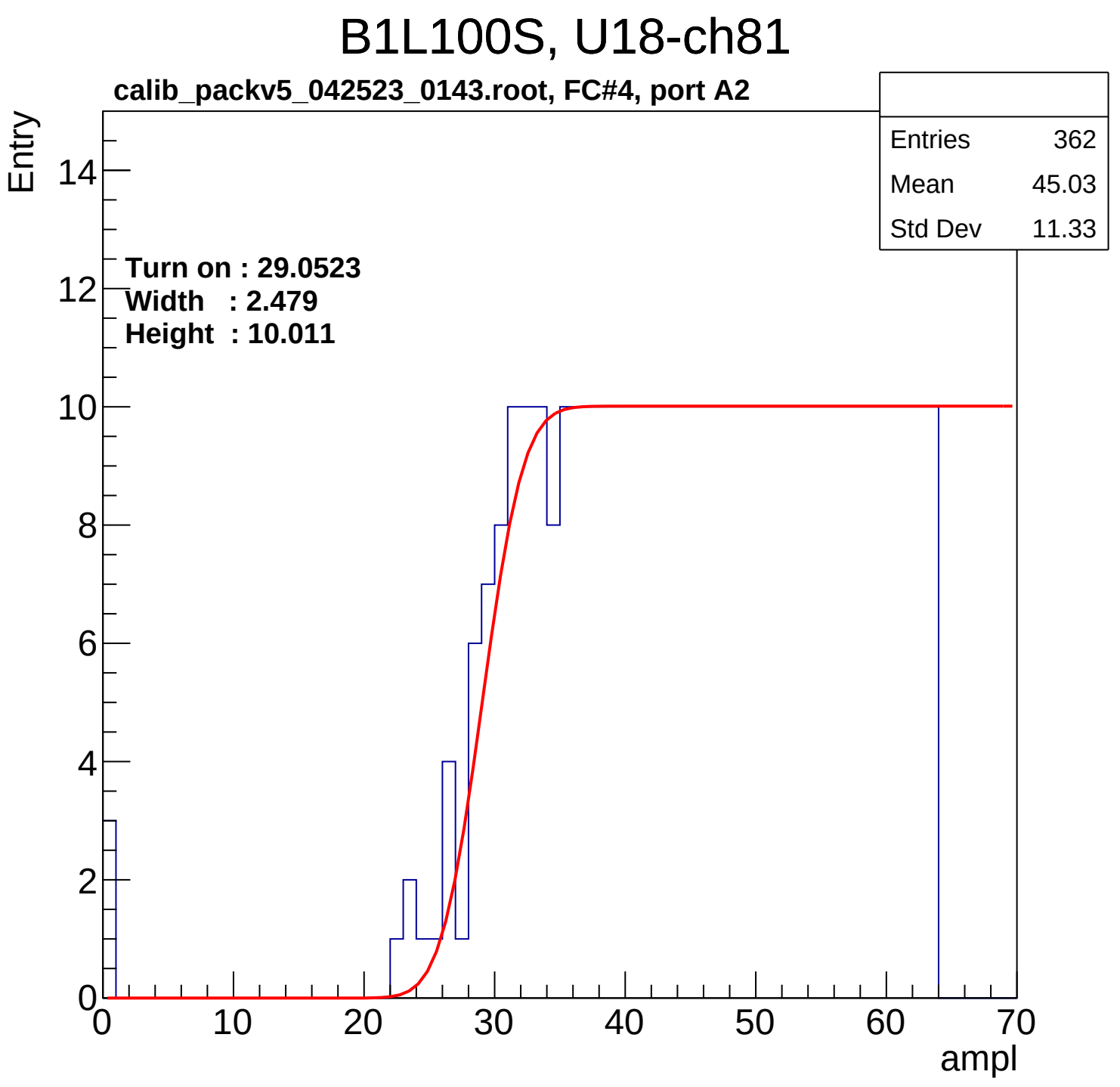
B1L100S, U18-ch81
calib_packv5_042523_0143.root, FC#4, port A2
Entries 362
Mean 45.03
Std Dev 11.33
Turn on : 29.0523
Width : 2.479
Height : 10.011
Entry
ampl
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4
6
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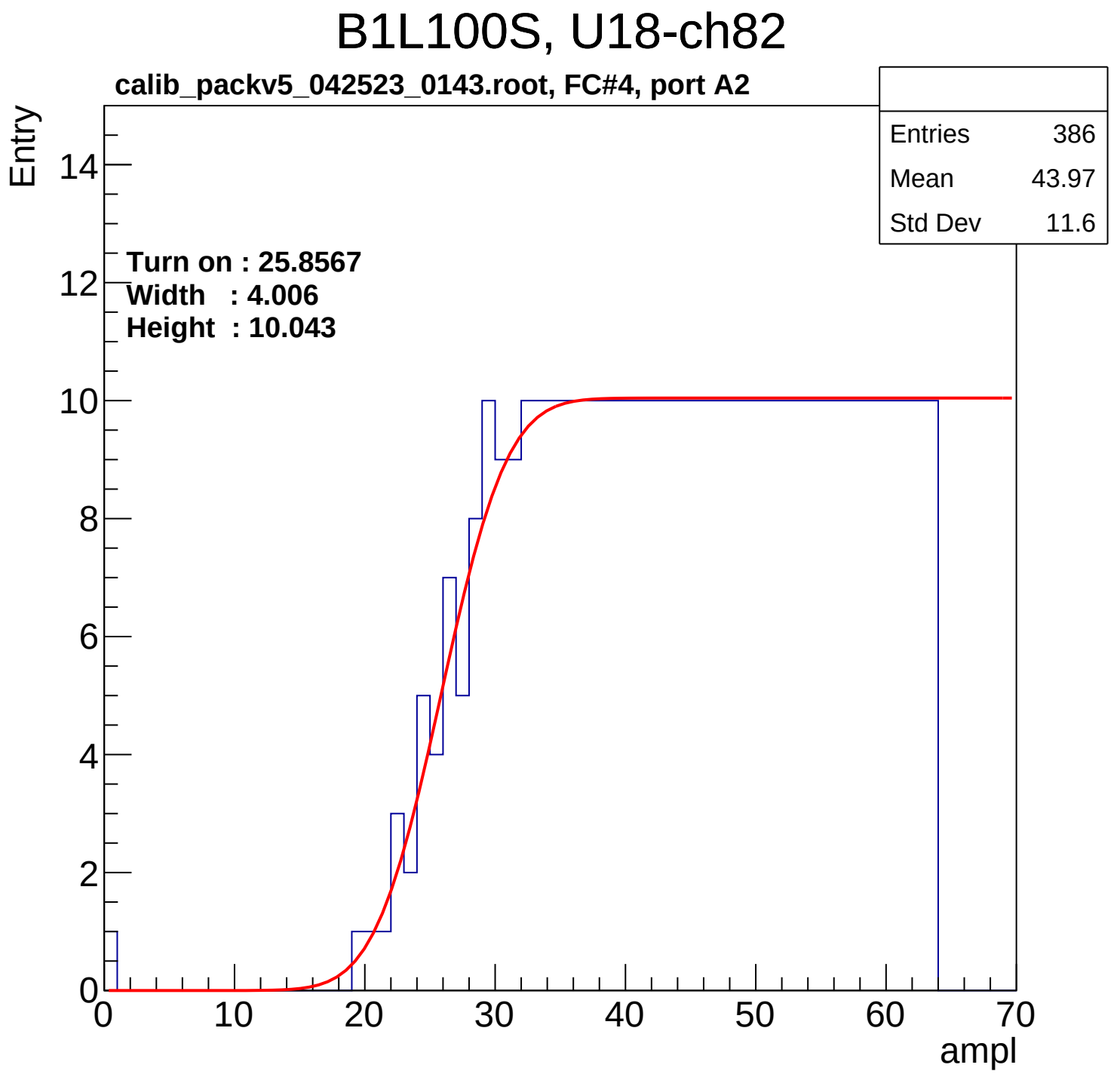
B1L100S, U18-ch82
calib_packv5_042523_0143.root, FC#4, port A2
Entries 386
Mean 43.97
Std Dev 11.6
Turn on : 25.8567
Width : 4.006
Height : 10.043
Entry
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6
8
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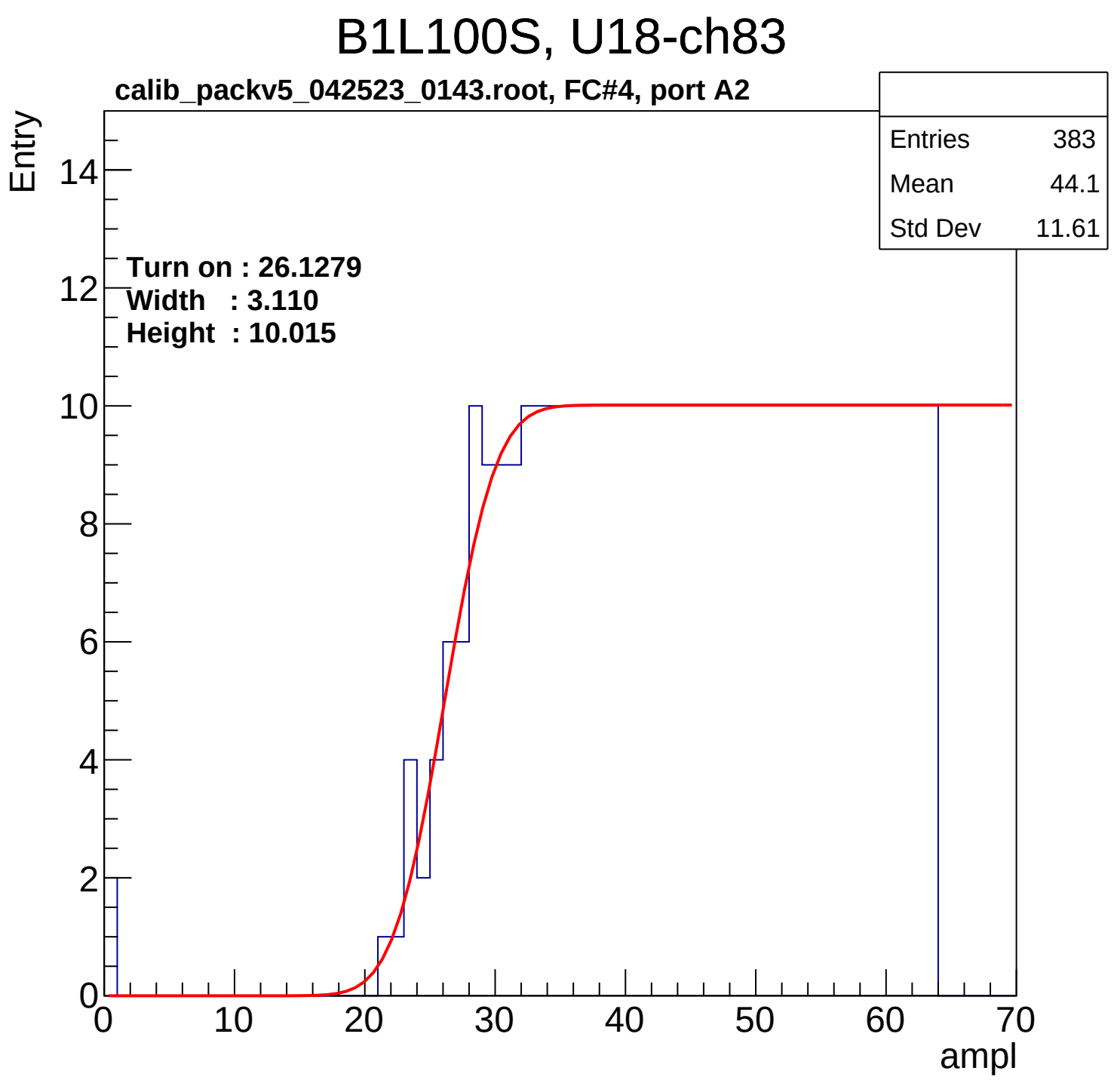
B1L100S, U18-ch83
calib_packv5_042523_0143.root, FC#4, port A2
Entries 383
Mean 44.1
Std Dev 11.61
Turn on : 26.1279
Width : 3.110
Height : 10.015
Entry
ampl
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8
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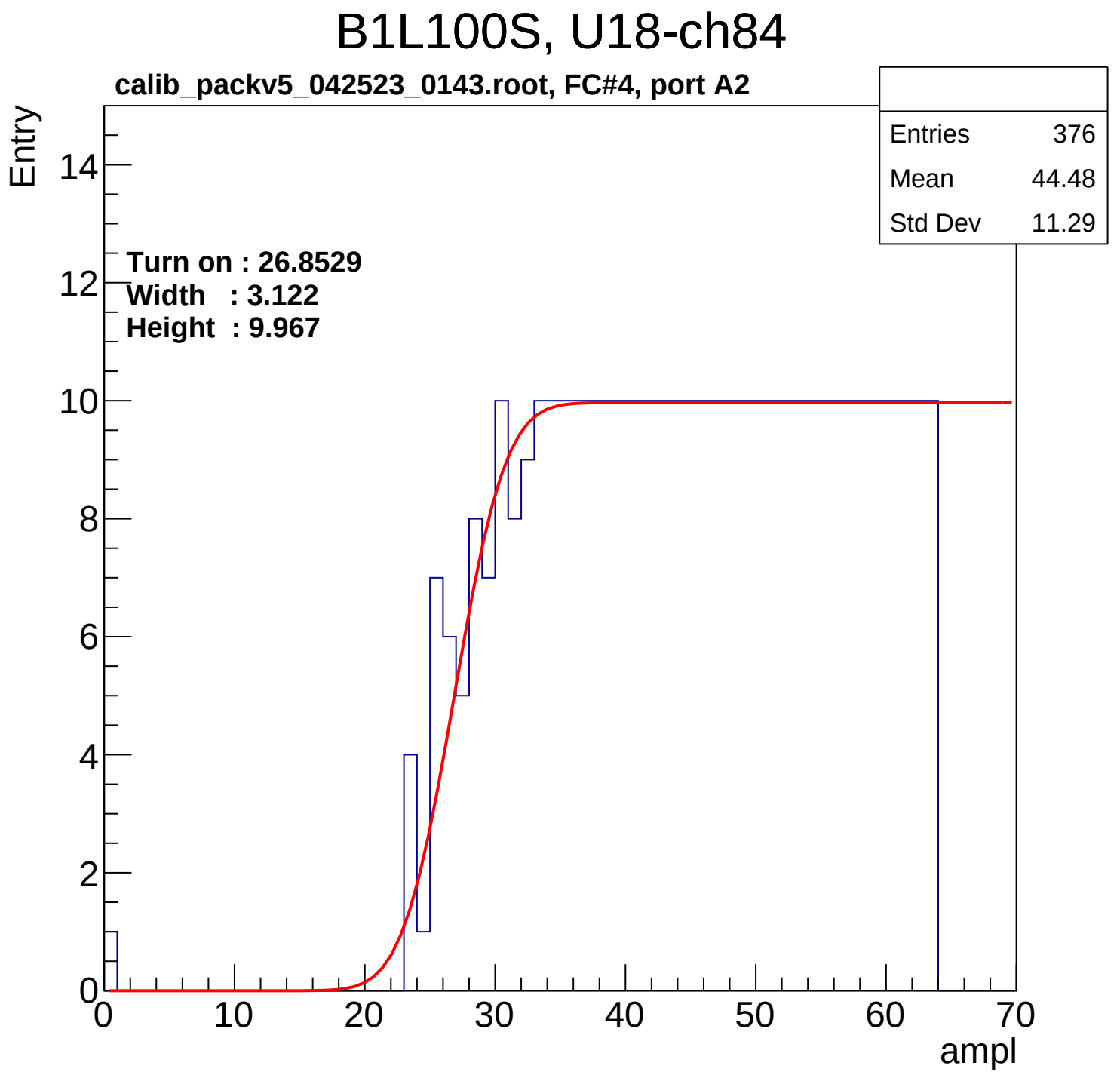
B1L100S, U18-ch84
calib_packv5_042523_0143.root, FC#4, port A2
Entries 376
Mean 44.48
Std Dev 11.29
Turn on : 26.8529
Width : 3.122
Height : 9.967
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ampl
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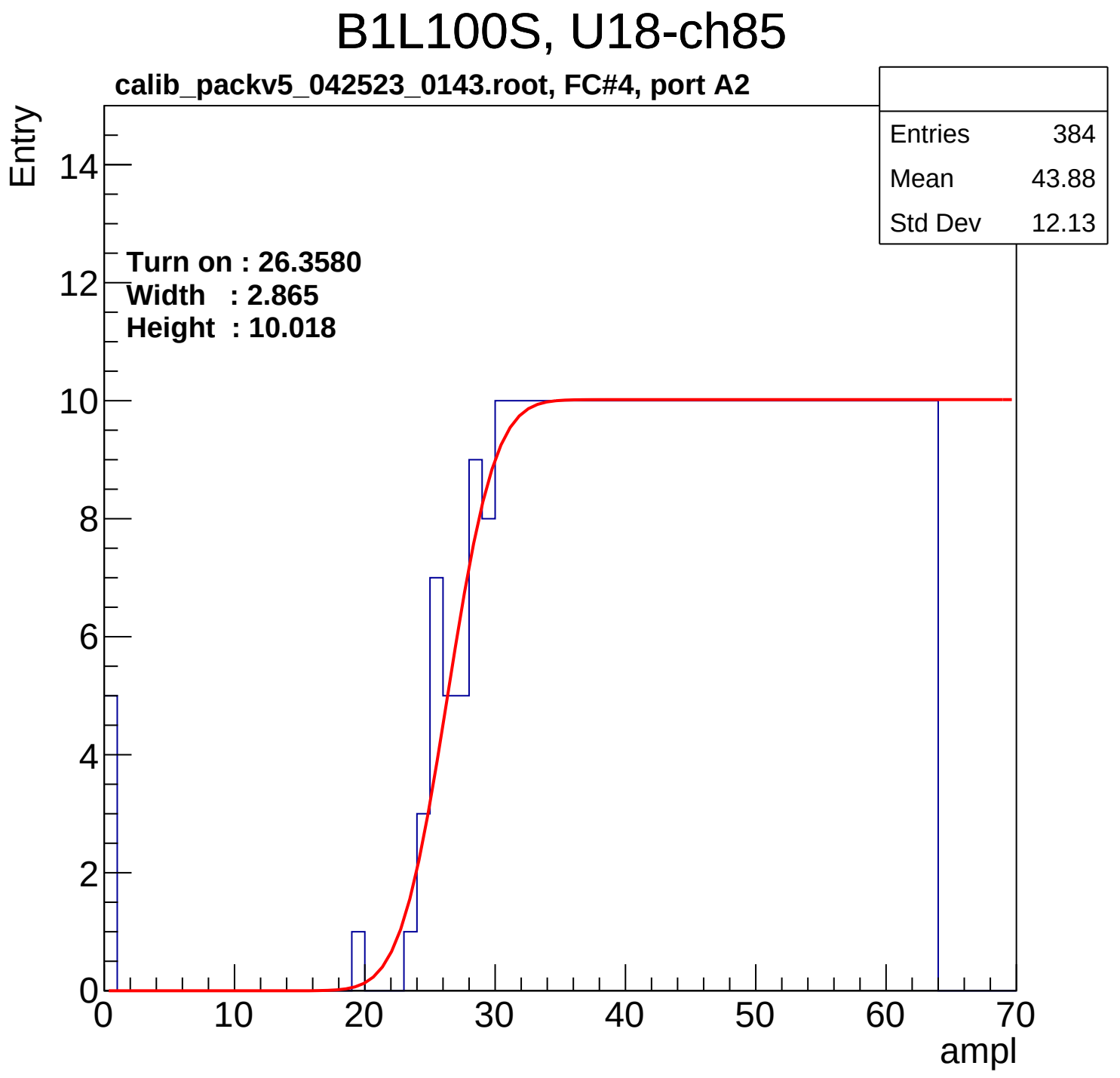
B1L100S, U18-ch85
calib_packv5_042523_0143.root, FC#4, port A2
Entries 384
Mean 43.88
Std Dev 12.13
Turn on : 26.3580
Width : 2.865
Height : 10.018
Entry
ampl
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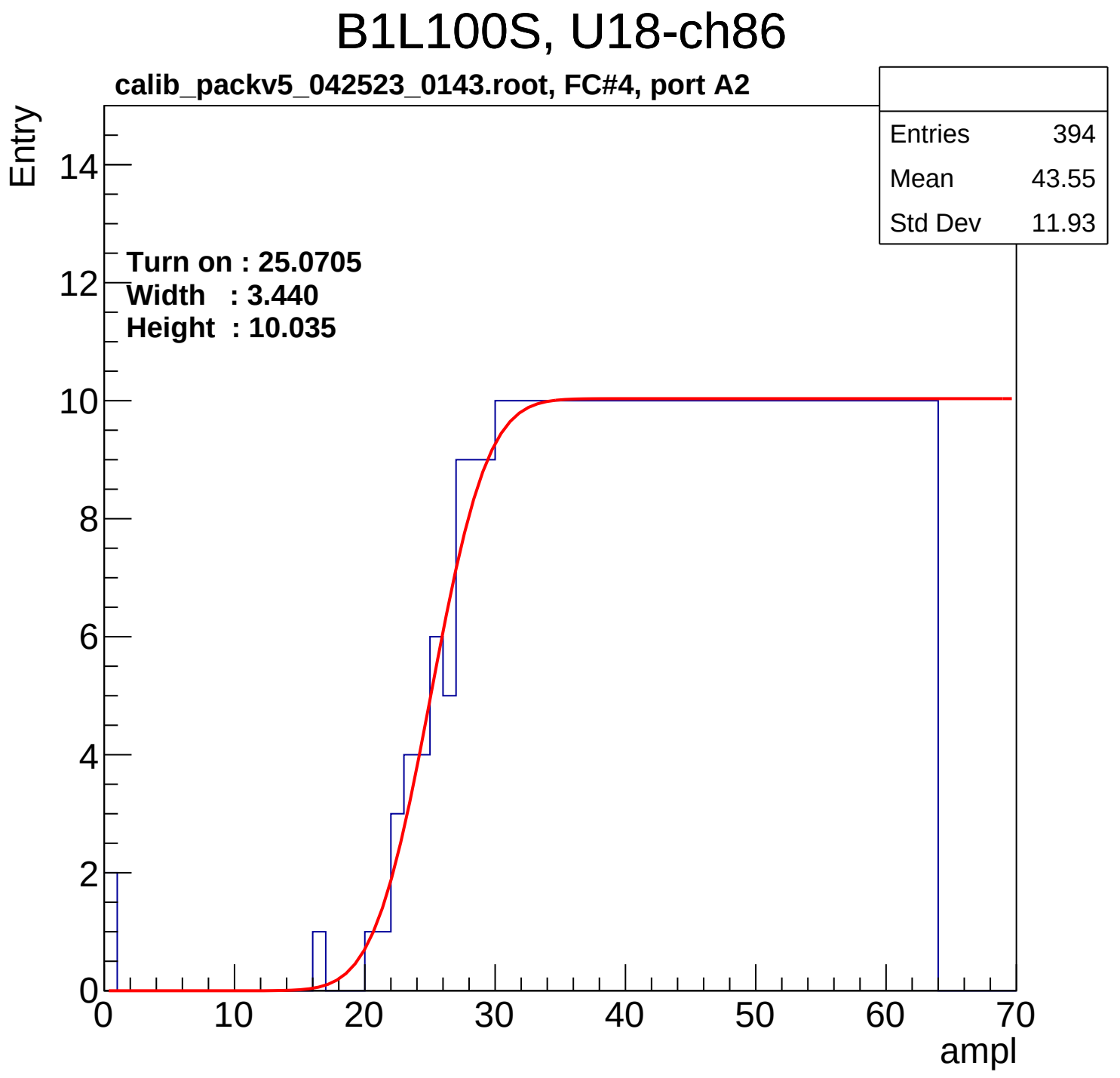
B1L100S, U18-ch86
calib_packv5_042523_0143.root, FC#4, port A2
Entries 394
Mean 43.55
Std Dev 11.93
Turn on : 25.0705
Width : 3.440
Height : 10.035
Entry
ampl
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4
6
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12
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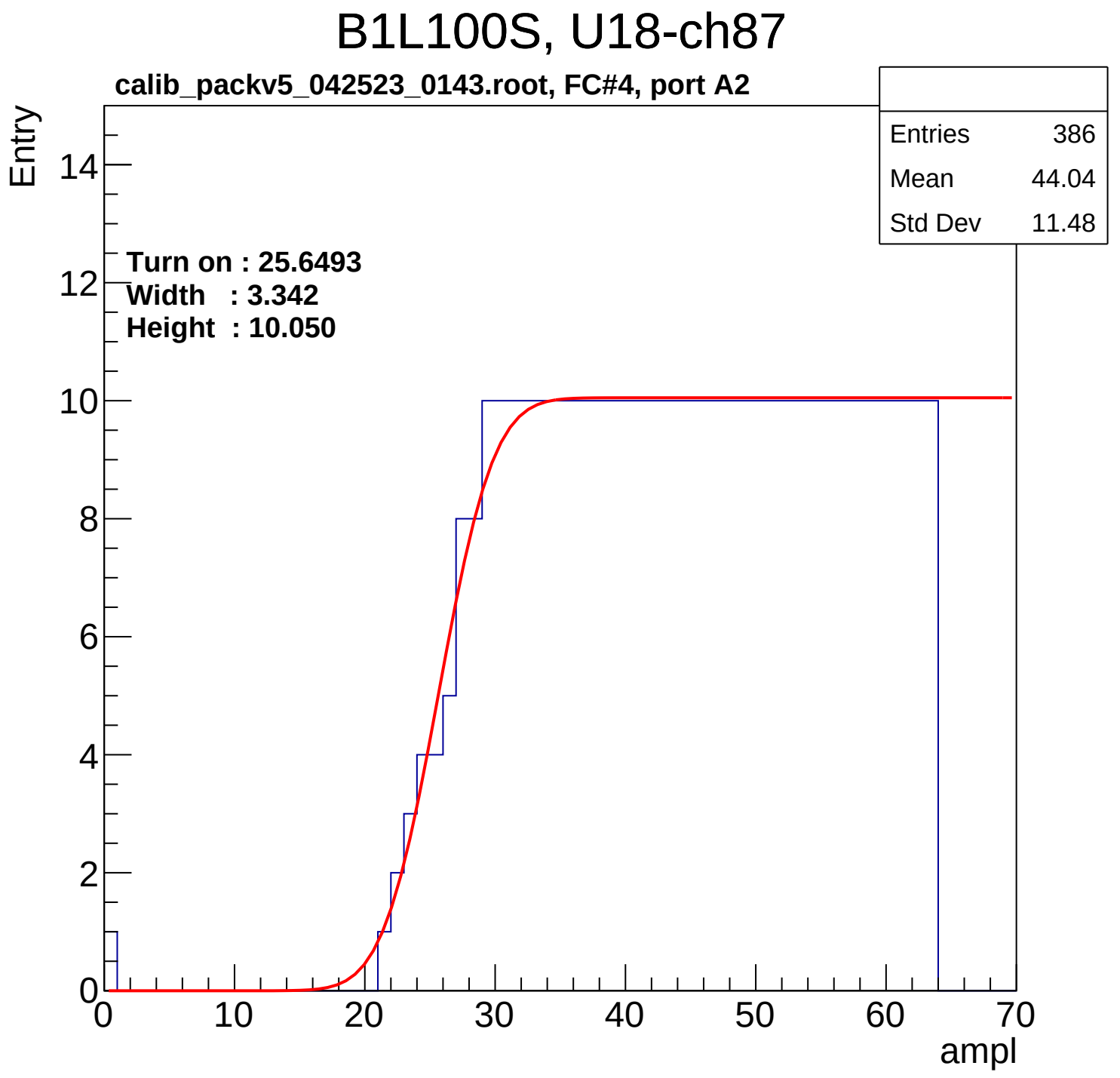
B1L100S, U18-ch87
calib_packv5_042523_0143.root, FC#4, port A2
Entries 386
Mean 44.04
Std Dev 11.48
Turn on : 25.6493
Width : 3.342
Height : 10.050
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ampl
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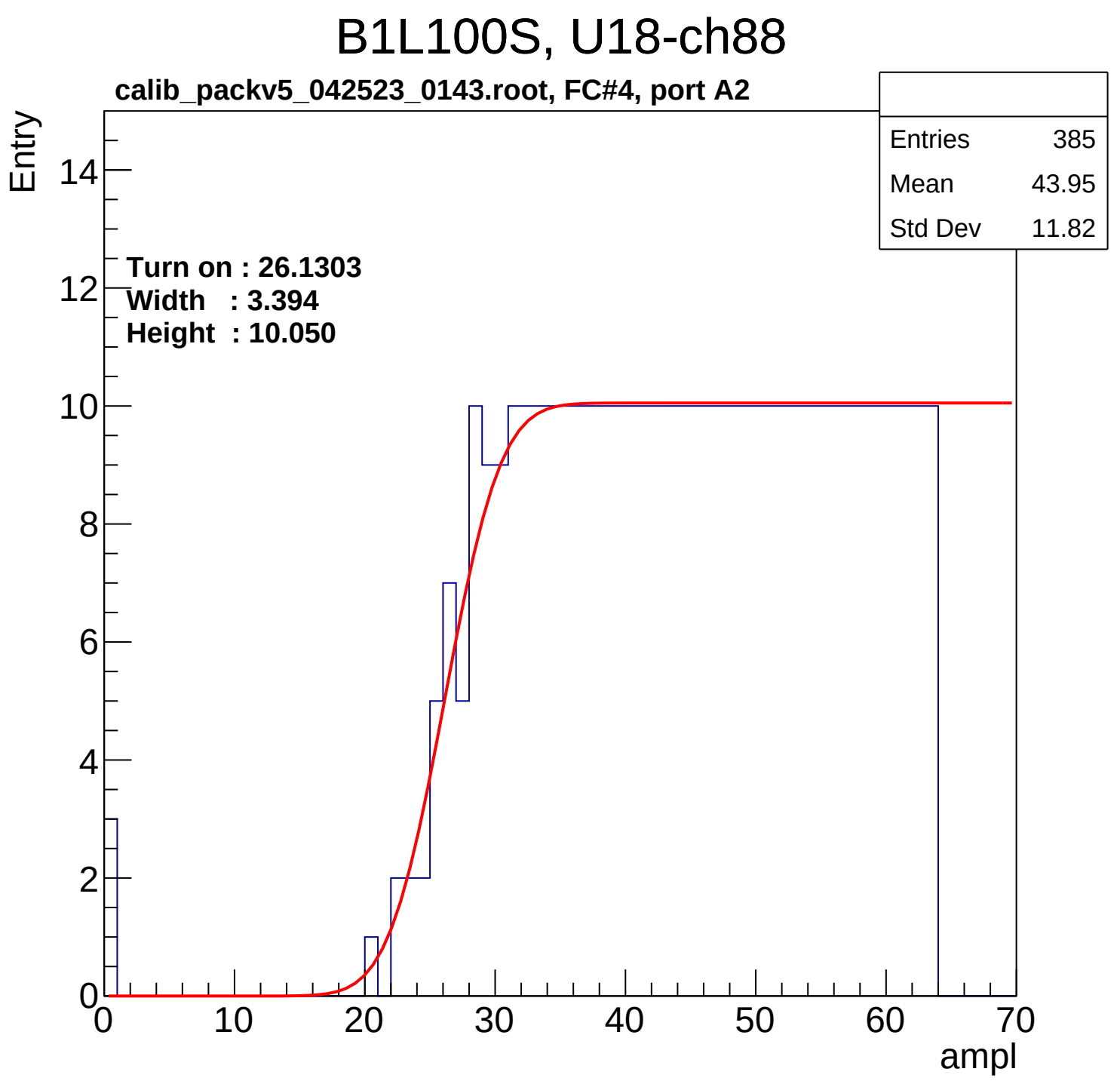
B1L100S, U18-ch88
calib_packv5_042523_0143.root, FC#4, port A2
Entries 385
Mean 43.95
Std Dev 11.82
Turn on : 26.1303
Width : 3.394
Height : 10.050
Entry
ampl
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4
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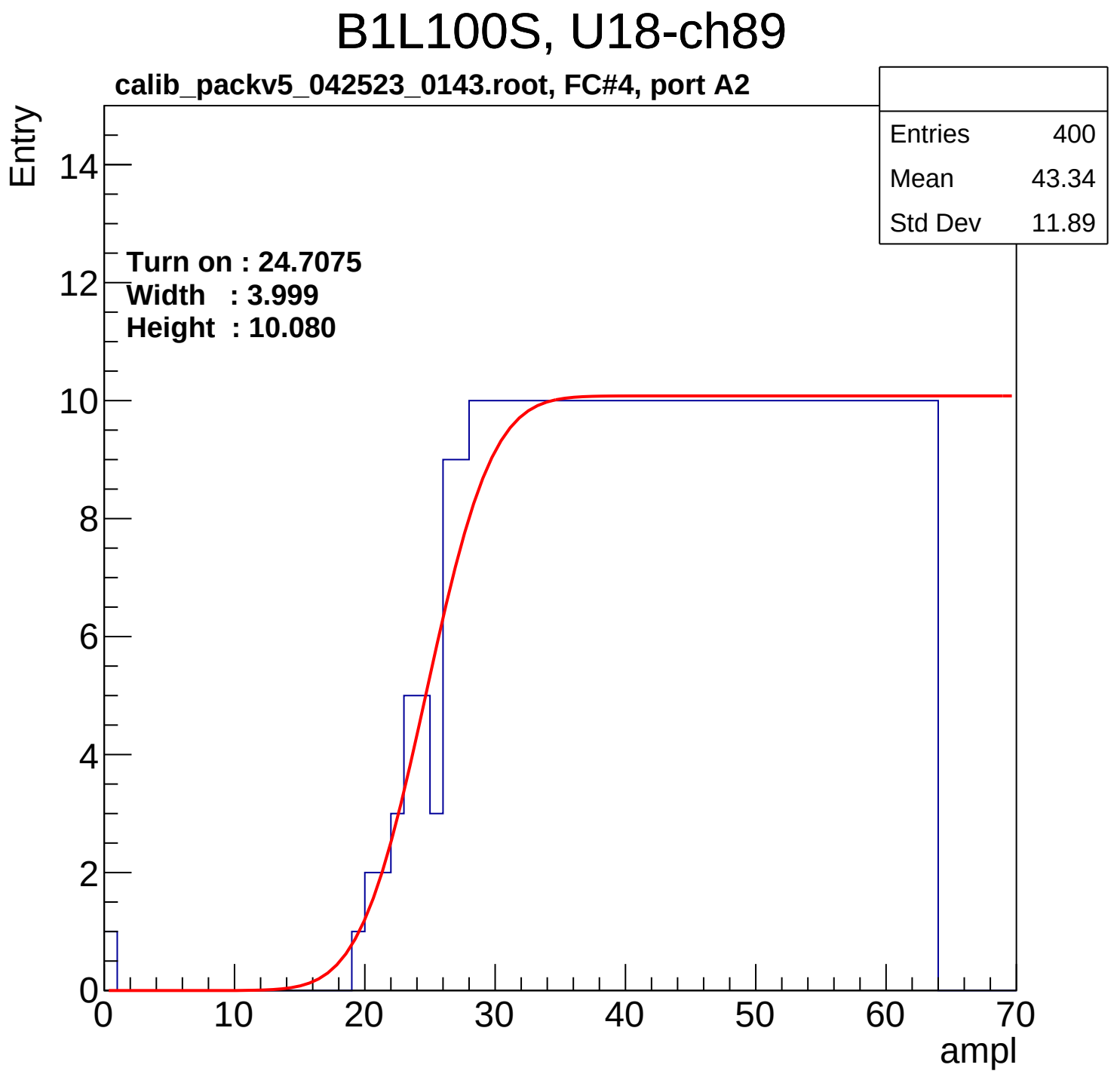
B1L100S, U18-ch89
calib_packv5_042523_0143.root, FC#4, port A2
Entries 400
Mean 43.34
Std Dev 11.89
Turn on : 24.7075
Width : 3.999
Height : 10.080
Entry
ampl
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4
6
8
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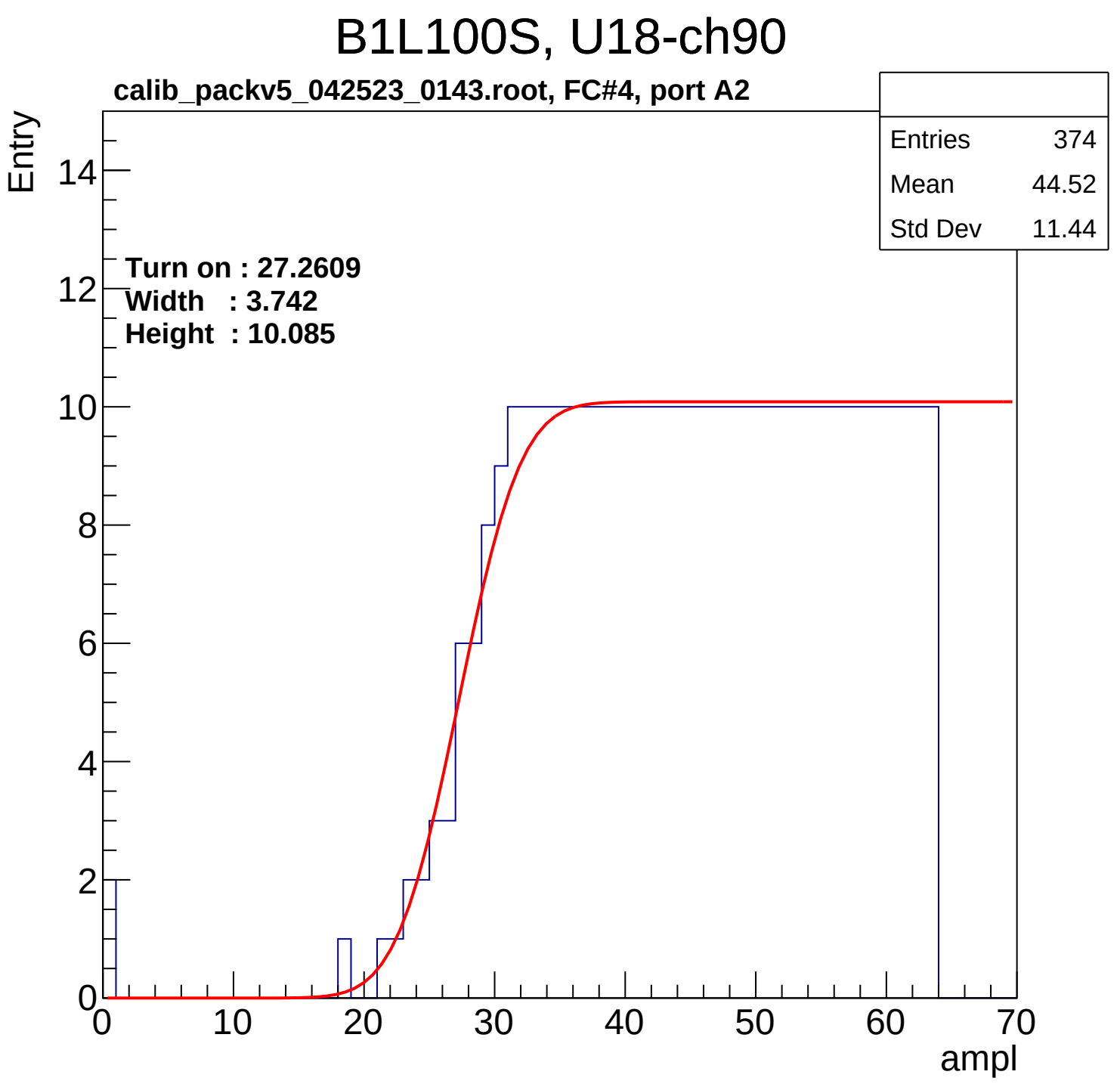
B1L100S, U18-ch90
calib_packv5_042523_0143.root, FC#4, port A2
Entries 374
Mean 44.52
Std Dev 11.44
Turn on : 27.2609
Width : 3.742
Height : 10.085
Entry
ampl
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2
4
6
8
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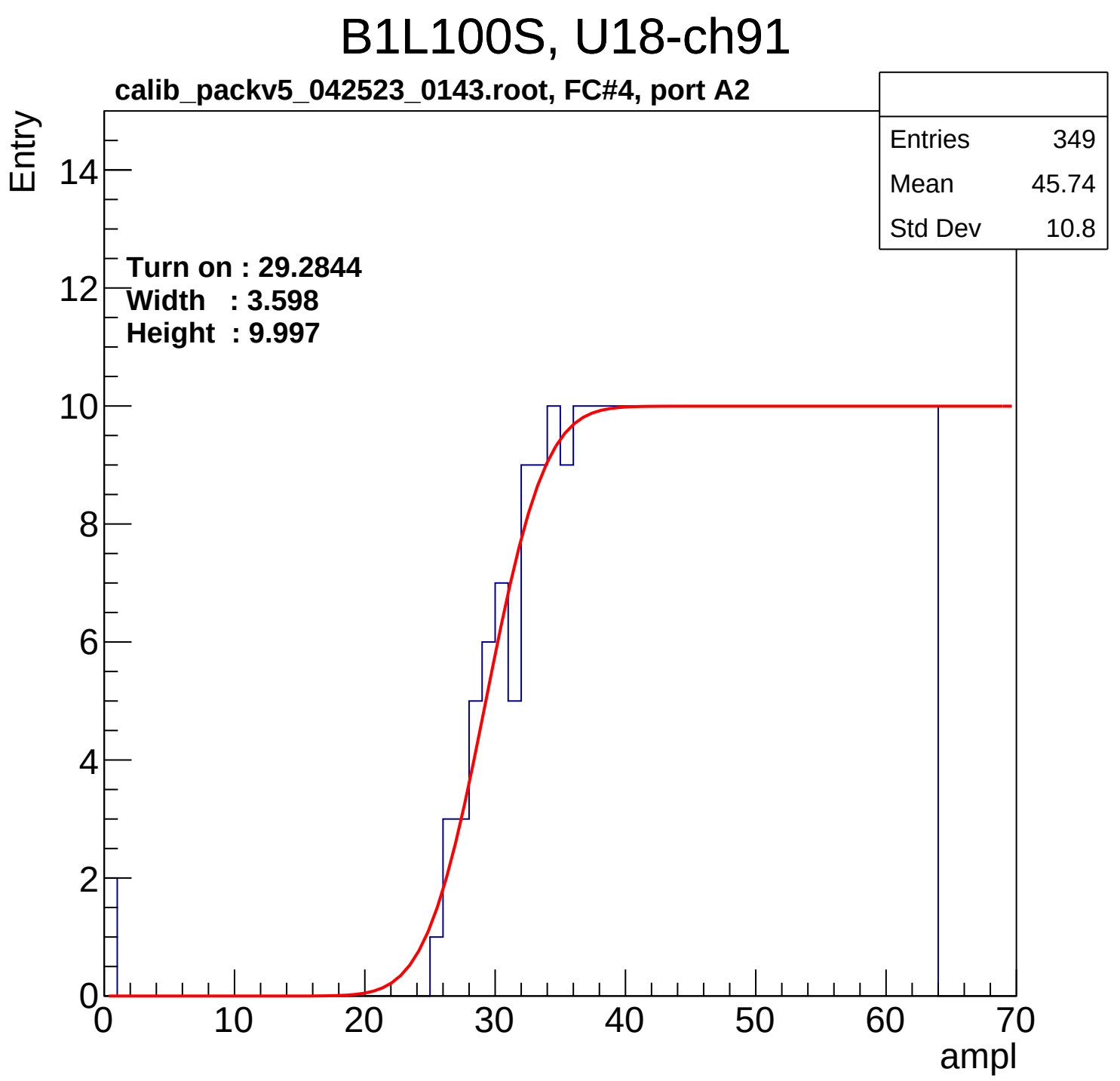
B1L100S, U18-ch91
calib_packv5_042523_0143.root, FC#4, port A2
Entries 349
Mean 45.74
Std Dev 10.8
Turn on : 29.2844
Width : 3.598
Height : 9.997
Entry
ampl
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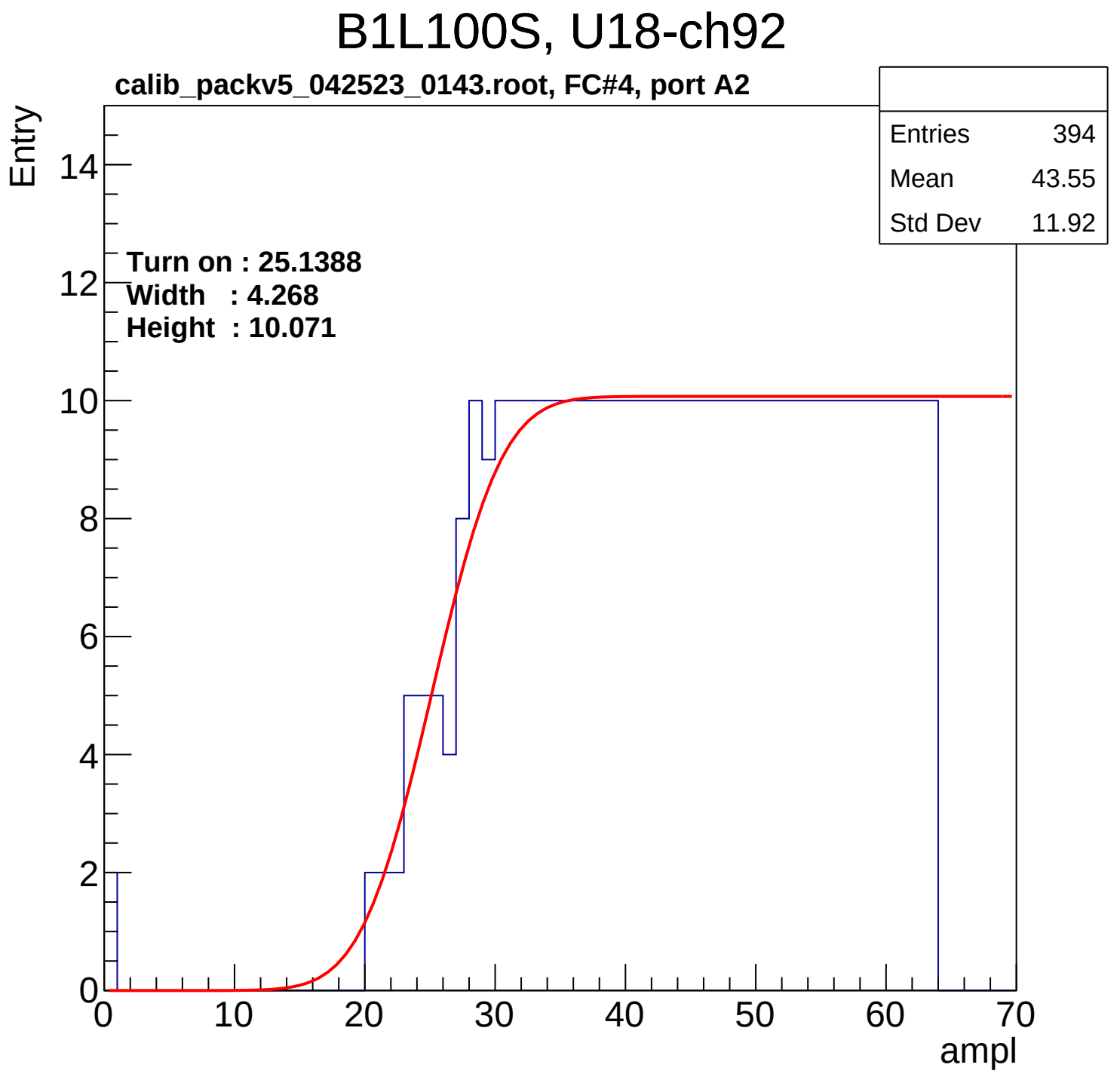
B1L100S, U18-ch92
calib_packv5_042523_0143.root, FC#4, port A2
Entries 394
Mean 43.55
Std Dev 11.92
Turn on : 25.1388
Width : 4.268
Height : 10.071
Entry
ampl
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2
4
6
8
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12
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0
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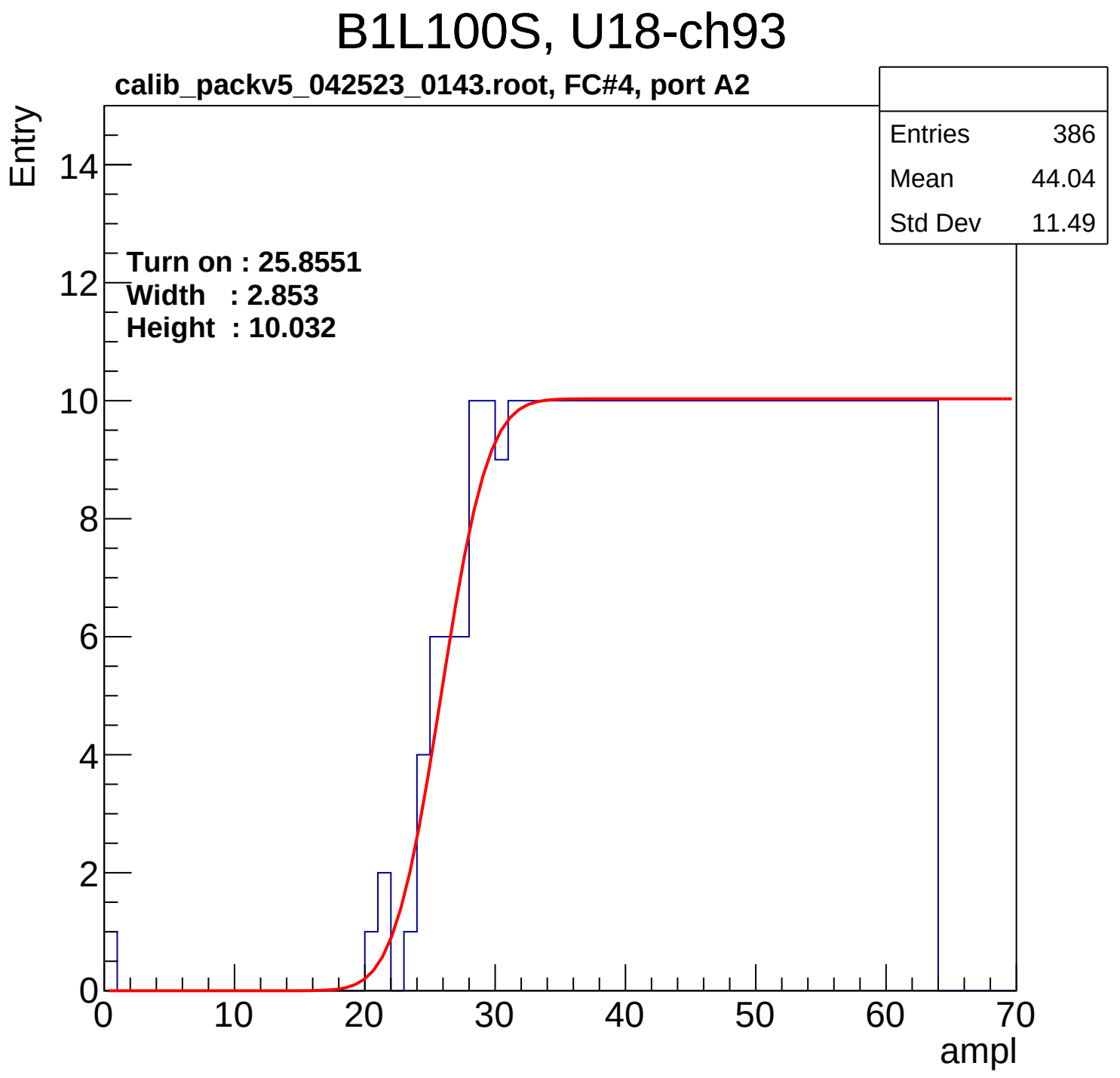
B1L100S, U18-ch93
calib_packv5_042523_0143.root, FC#4, port A2
Entries 386
Mean 44.04
Std Dev 11.49
Turn on : 25.8551
Width : 2.853
Height : 10.032
Entry
ampl
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6
8
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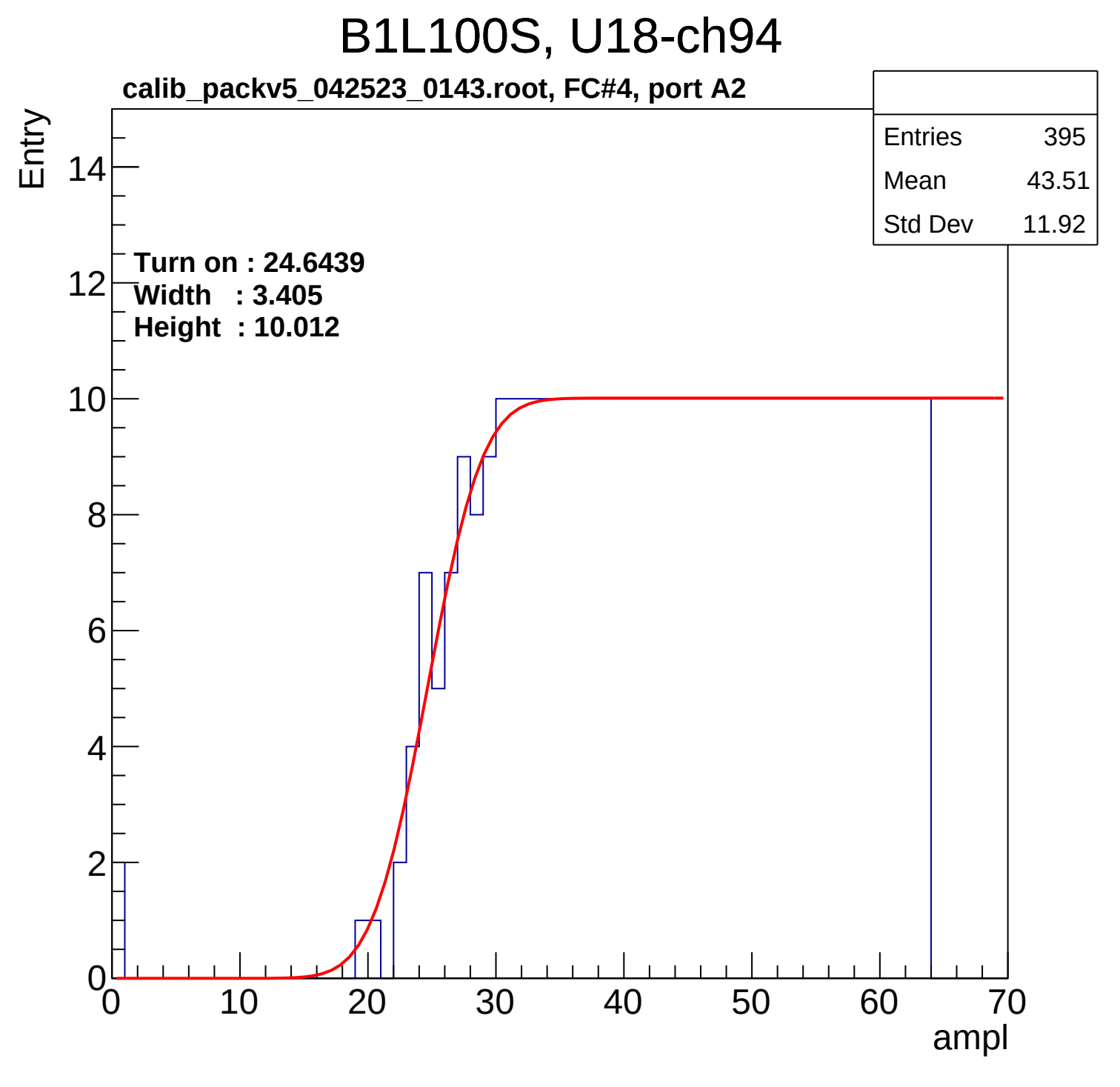
B1L100S, U18-ch94
calib_packv5_042523_0143.root, FC#4, port A2
Entries 395
Mean 43.51
Std Dev 11.92
Turn on : 24.6439
Width : 3.405
Height : 10.012
Entry
ampl
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2
4
6
8
10
12
14
0
10
20
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60
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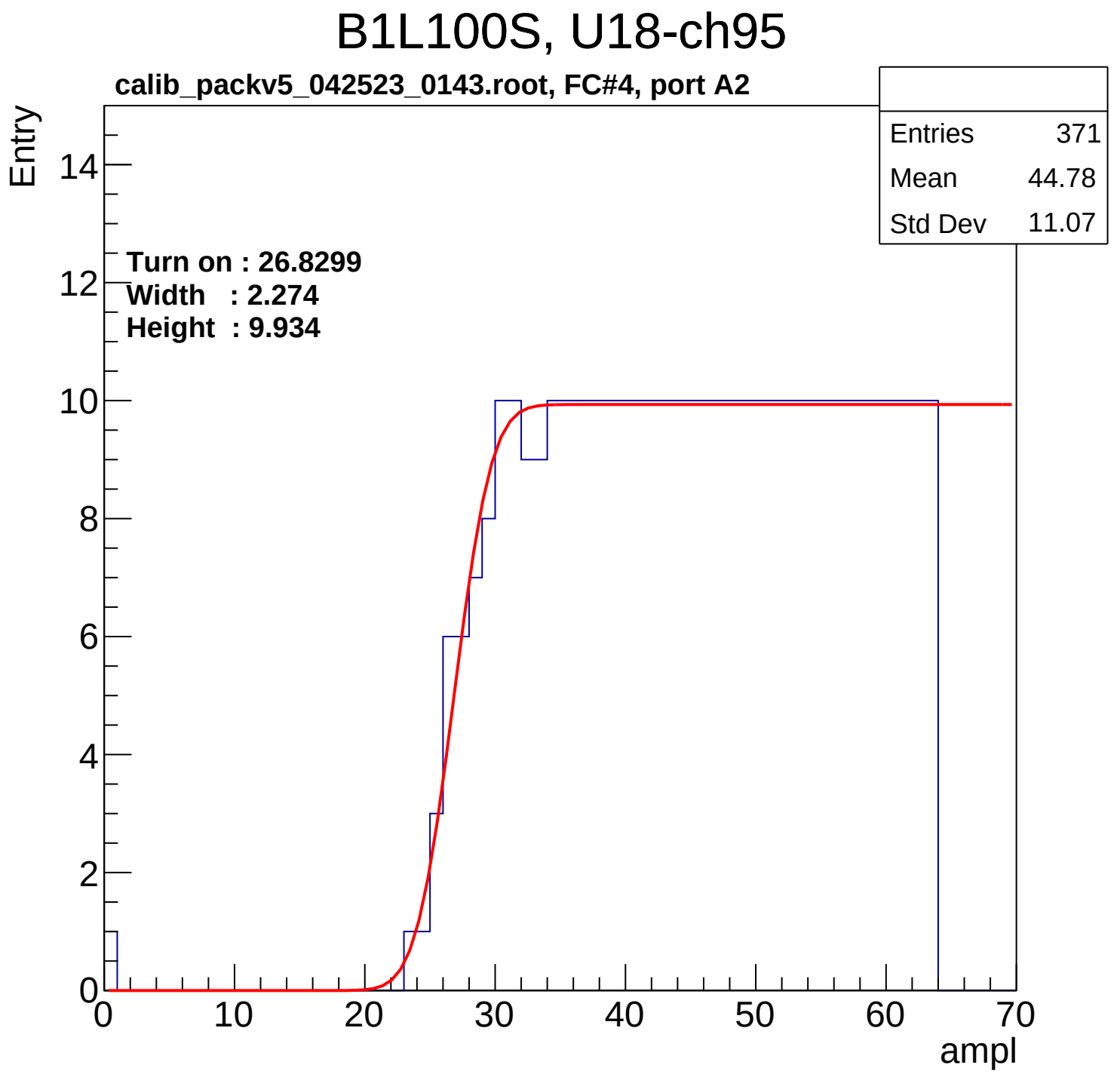
B1L100S, U18-ch95
calib_packv5_042523_0143.root, FC#4, port A2
Entries 371
Mean 44.78
Std Dev 11.07
Turn on : 26.8299
Width : 2.274
Height : 9.934
Entry
ampl
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2
4
6
8
10
12
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0
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20
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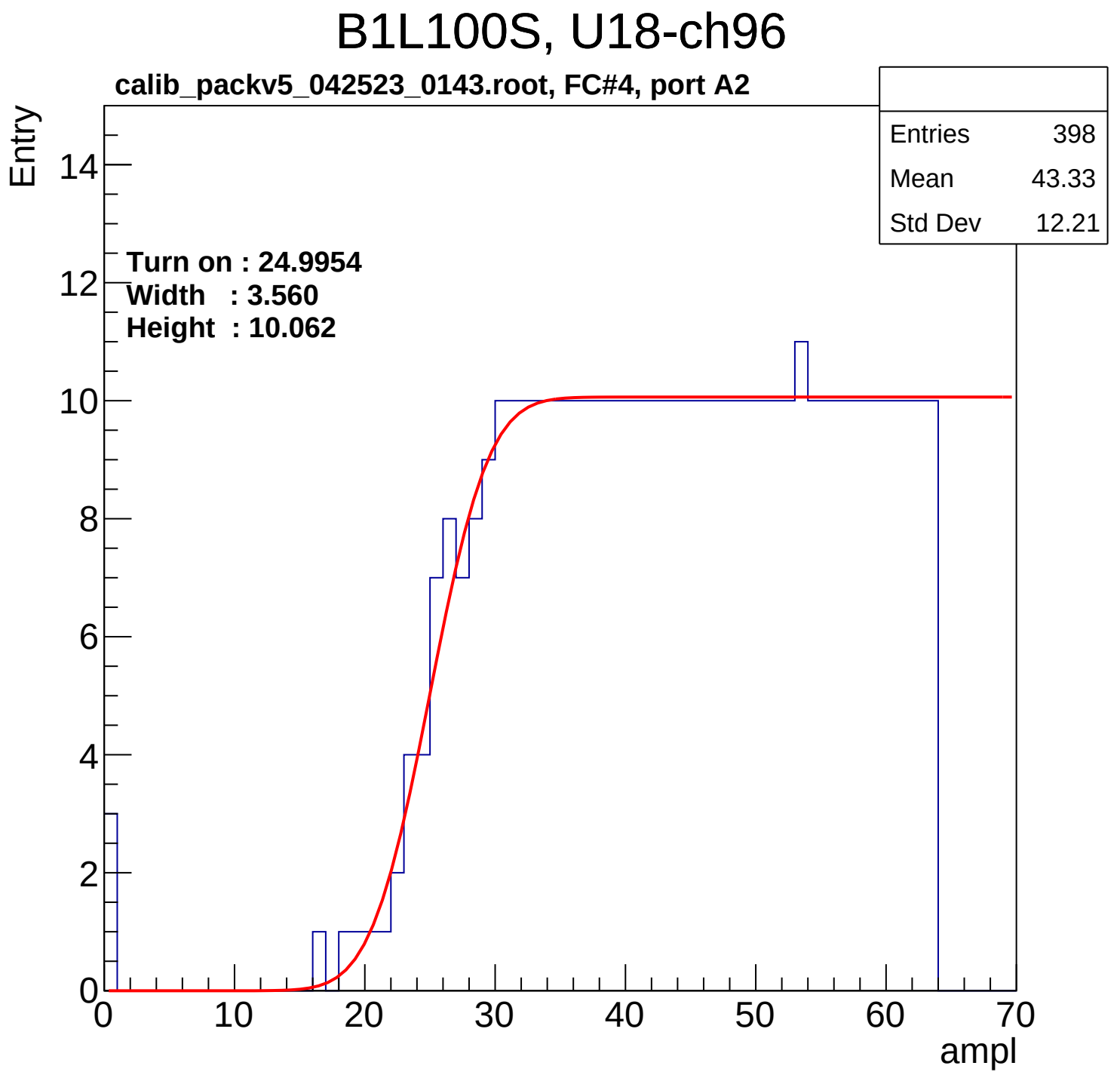
B1L100S, U18-ch96
calib_packv5_042523_0143.root, FC#4, port A2
Entries 398
Mean 43.33
Std Dev 12.21
Turn on : 24.9954
Width : 3.560
Height : 10.062
Entry
ampl
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2
4
6
8
10
12
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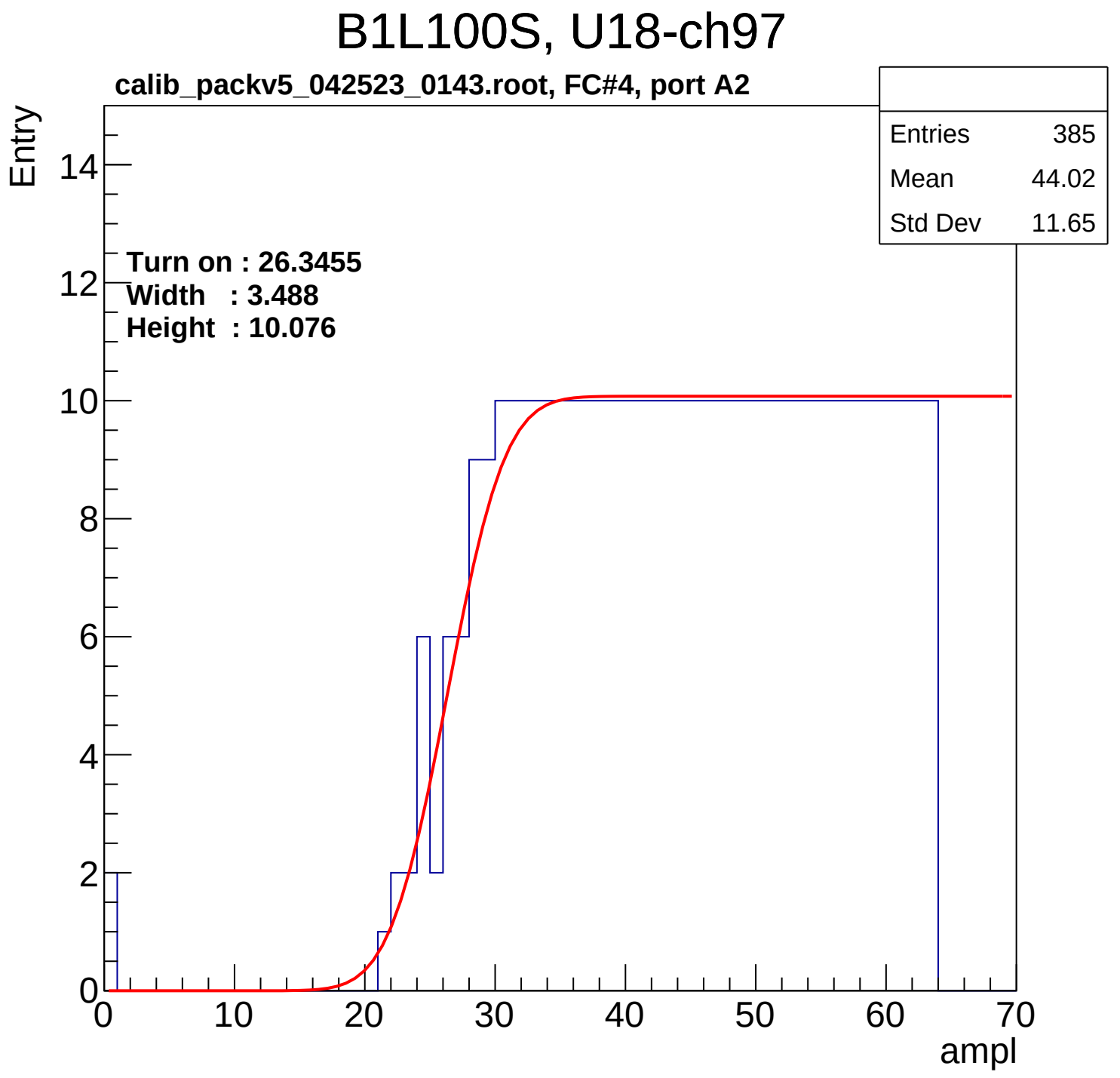
B1L100S, U18-ch97
calib_packv5_042523_0143.root, FC#4, port A2
Entries 385
Mean 44.02
Std Dev 11.65
Turn on : 26.3455
Width : 3.488
Height : 10.076
Entry
ampl
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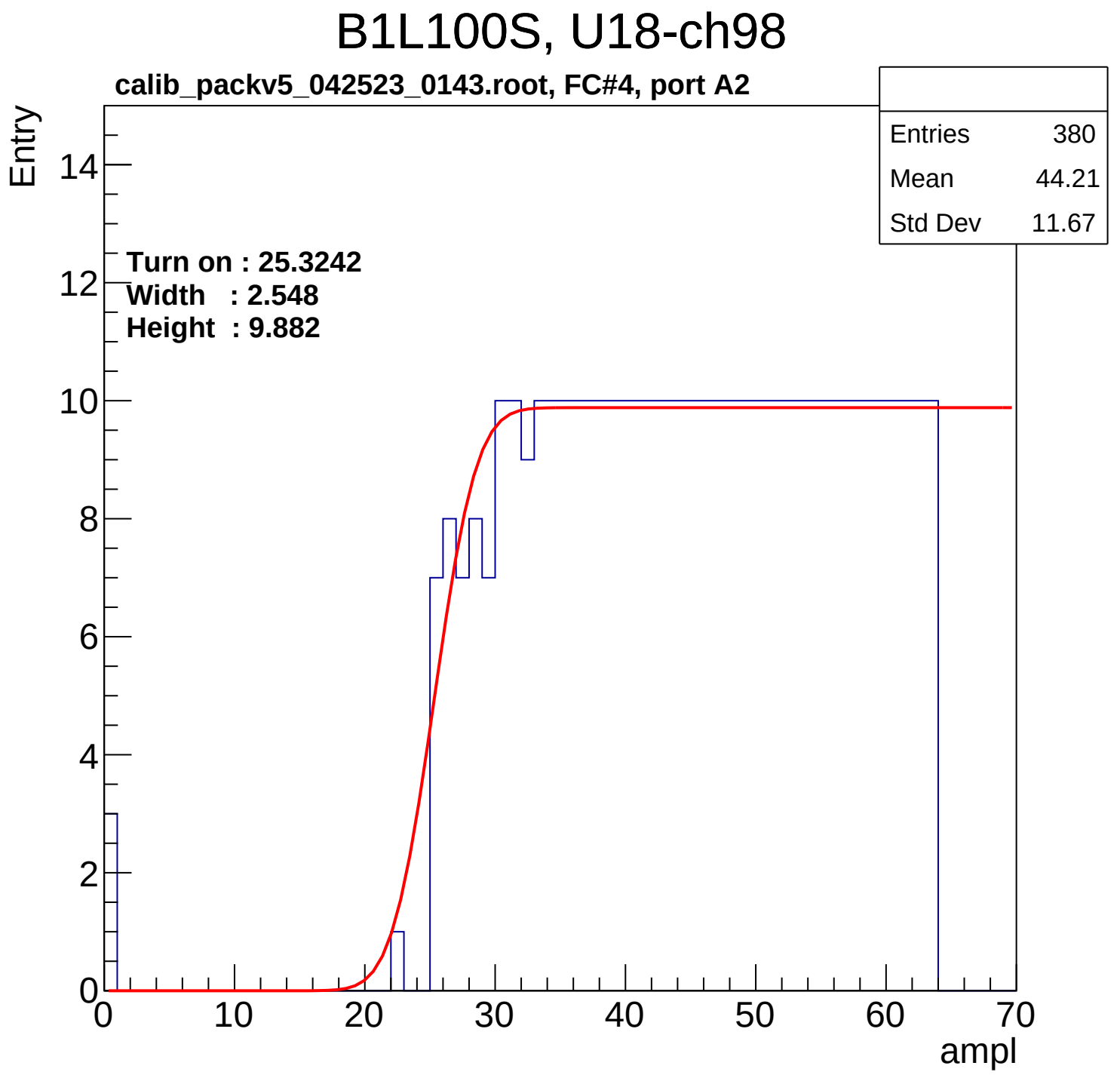
B1L100S, U18-ch98
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.21
Std Dev 11.67
Turn on : 25.3242
Width : 2.548
Height : 9.882
Entry
ampl
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6
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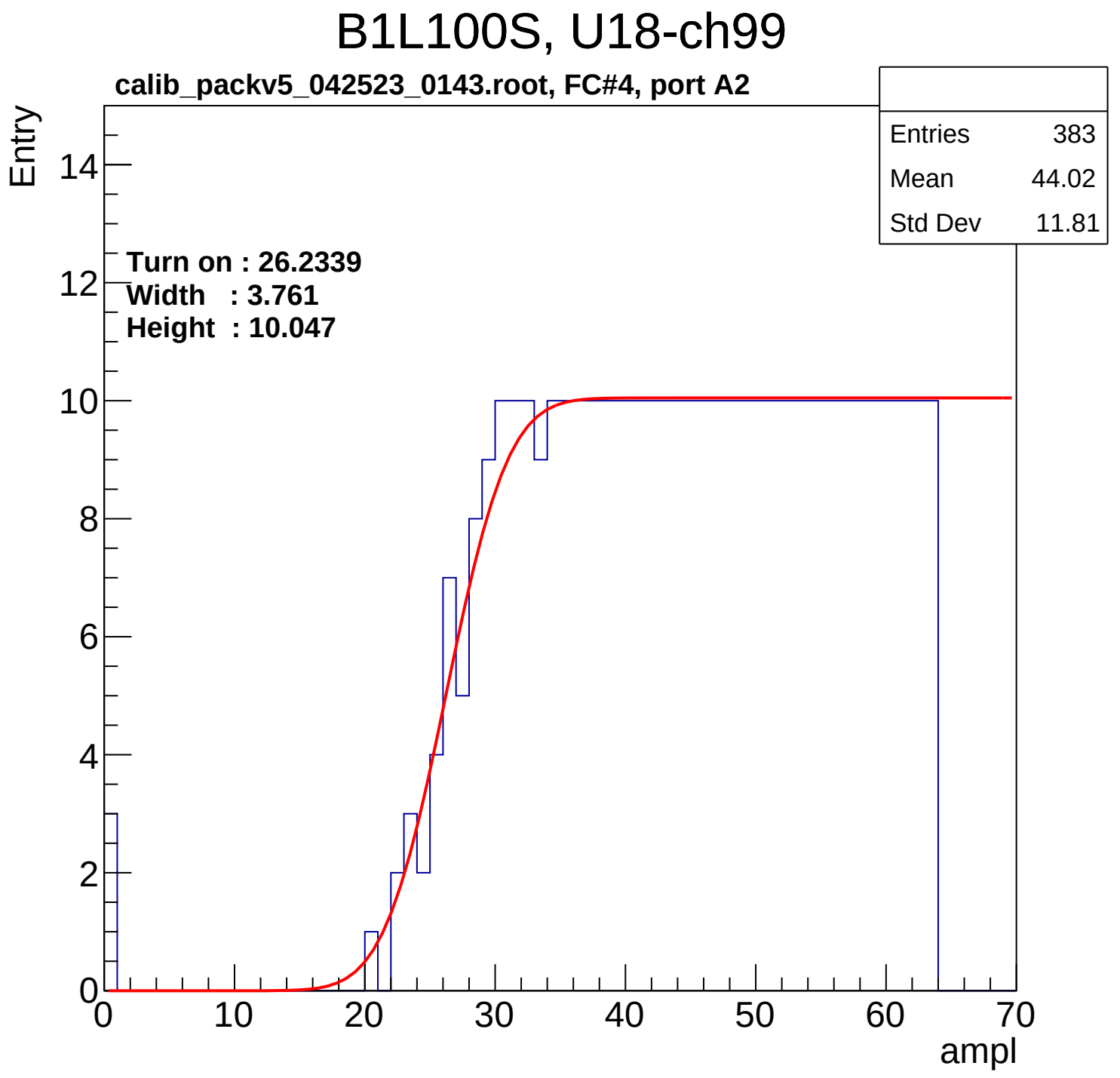
B1L100S, U18-ch99
calib_packv5_042523_0143.root, FC#4, port A2
Entries 383
Mean 44.02
Std Dev 11.81
Turn on : 26.2339
Width : 3.761
Height : 10.047
Entry
ampl
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6
8
10
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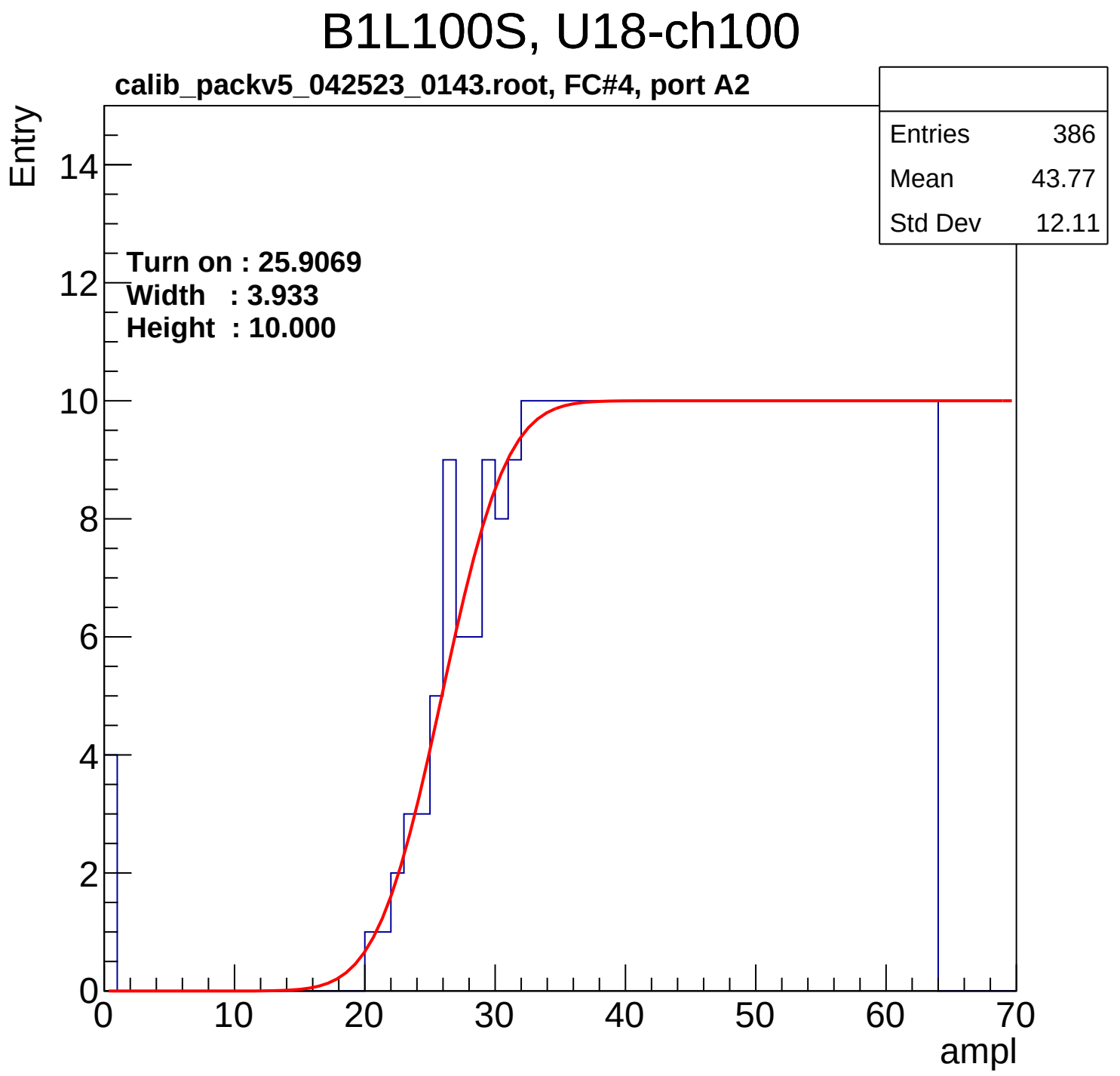
B1L100S, U18-ch100
calib_packv5_042523_0143.root, FC#4, port A2
Entries 386
Mean 43.77
Std Dev 12.11
Turn on : 25.9069
Width : 3.933
Height : 10.000
Entry
ampl
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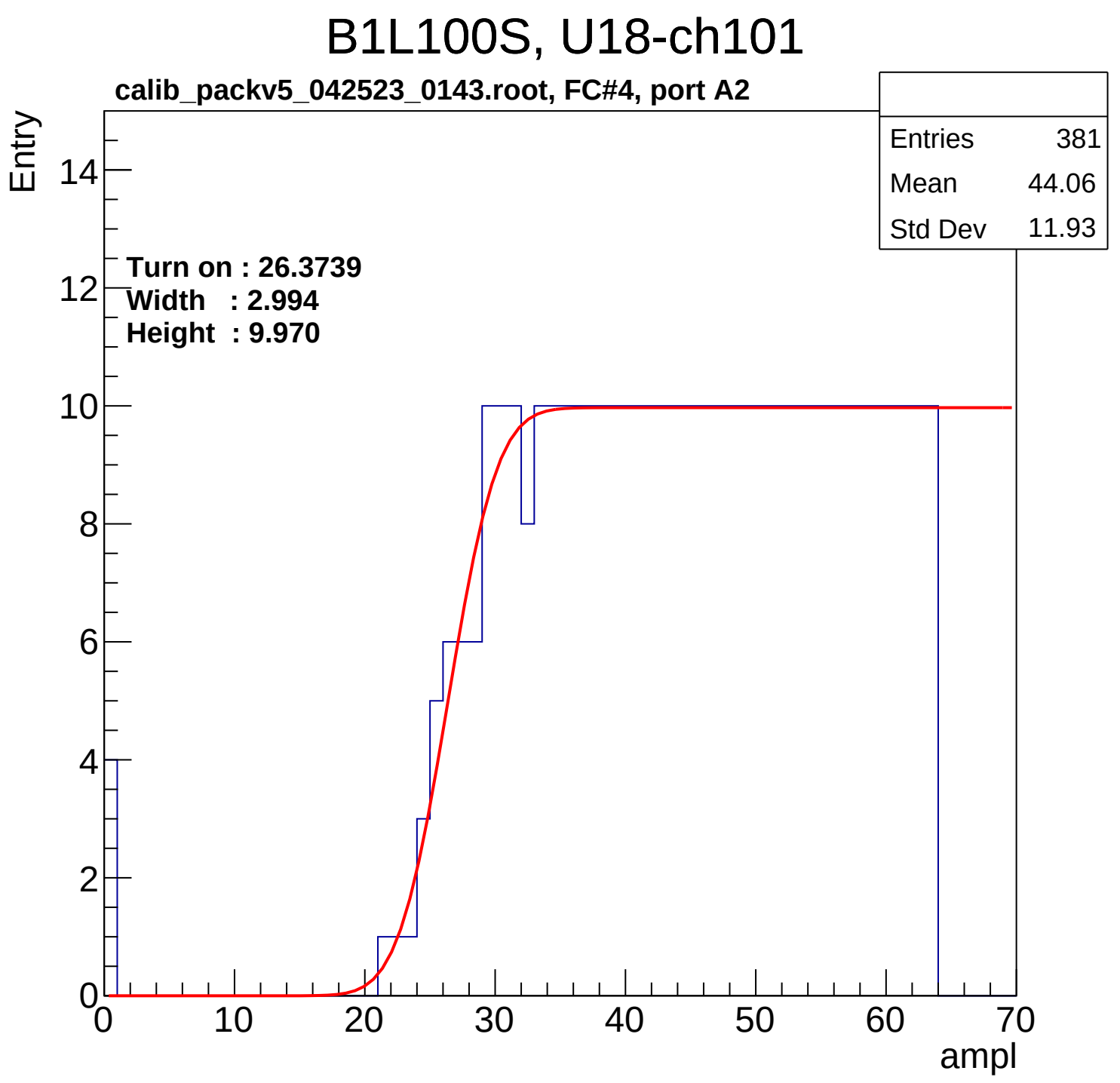
B1L100S, U18-ch101
calib_packv5_042523_0143.root, FC#4, port A2
Entries 381
Mean 44.06
Std Dev 11.93
Turn on : 26.3739
Width : 2.994
Height : 9.970
Entry
ampl
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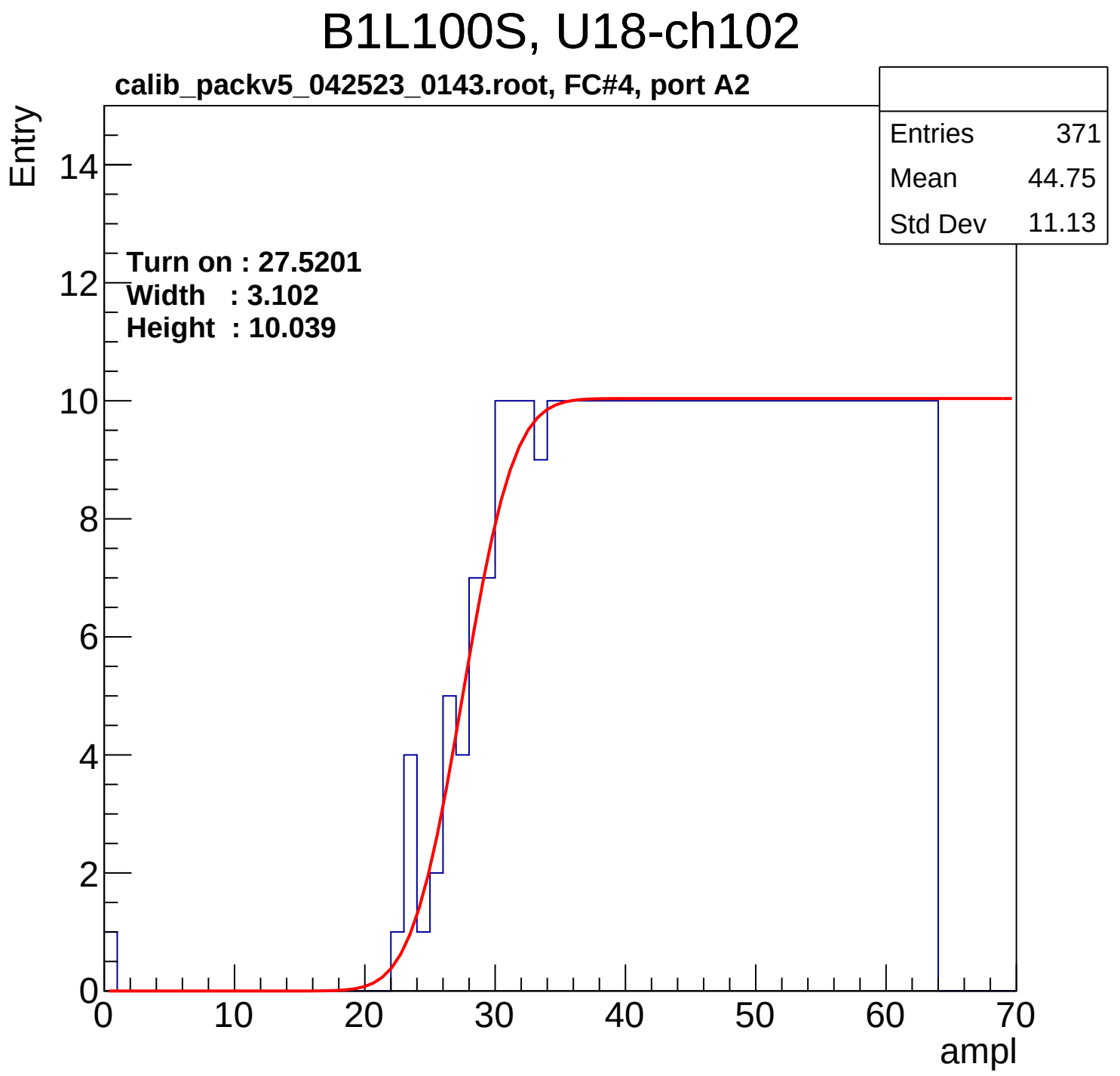
B1L100S, U18-ch102
calib_packv5_042523_0143.root, FC#4, port A2
Entries 371
Mean 44.75
Std Dev 11.13
Turn on : 27.5201
Width : 3.102
Height : 10.039
Entry
ampl
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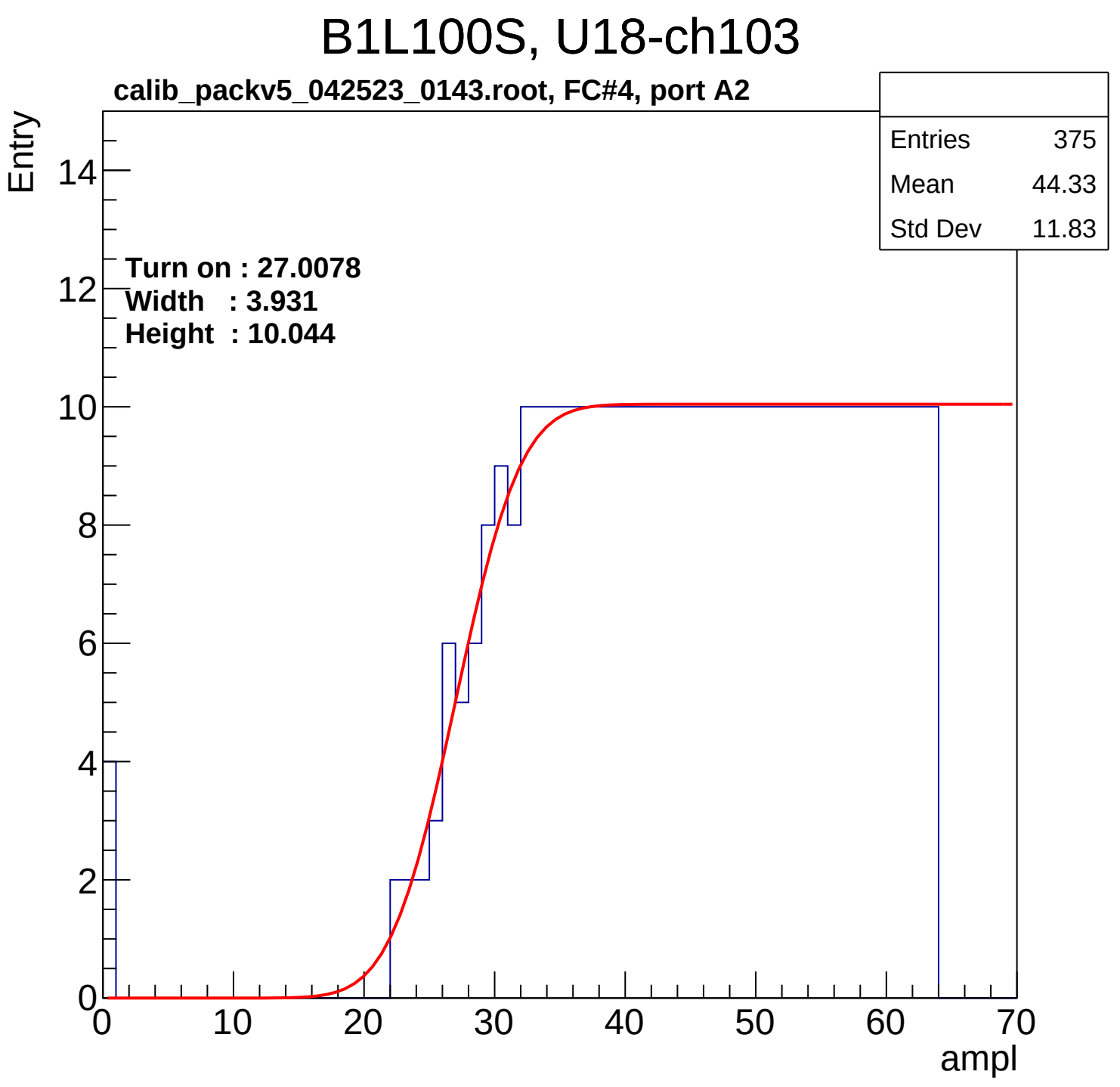
B1L100S, U18-ch103
calib_packv5_042523_0143.root, FC#4, port A2
Entries 375
Mean 44.33
Std Dev 11.83
Turn on : 27.0078
Width : 3.931
Height : 10.044
Entry
ampl
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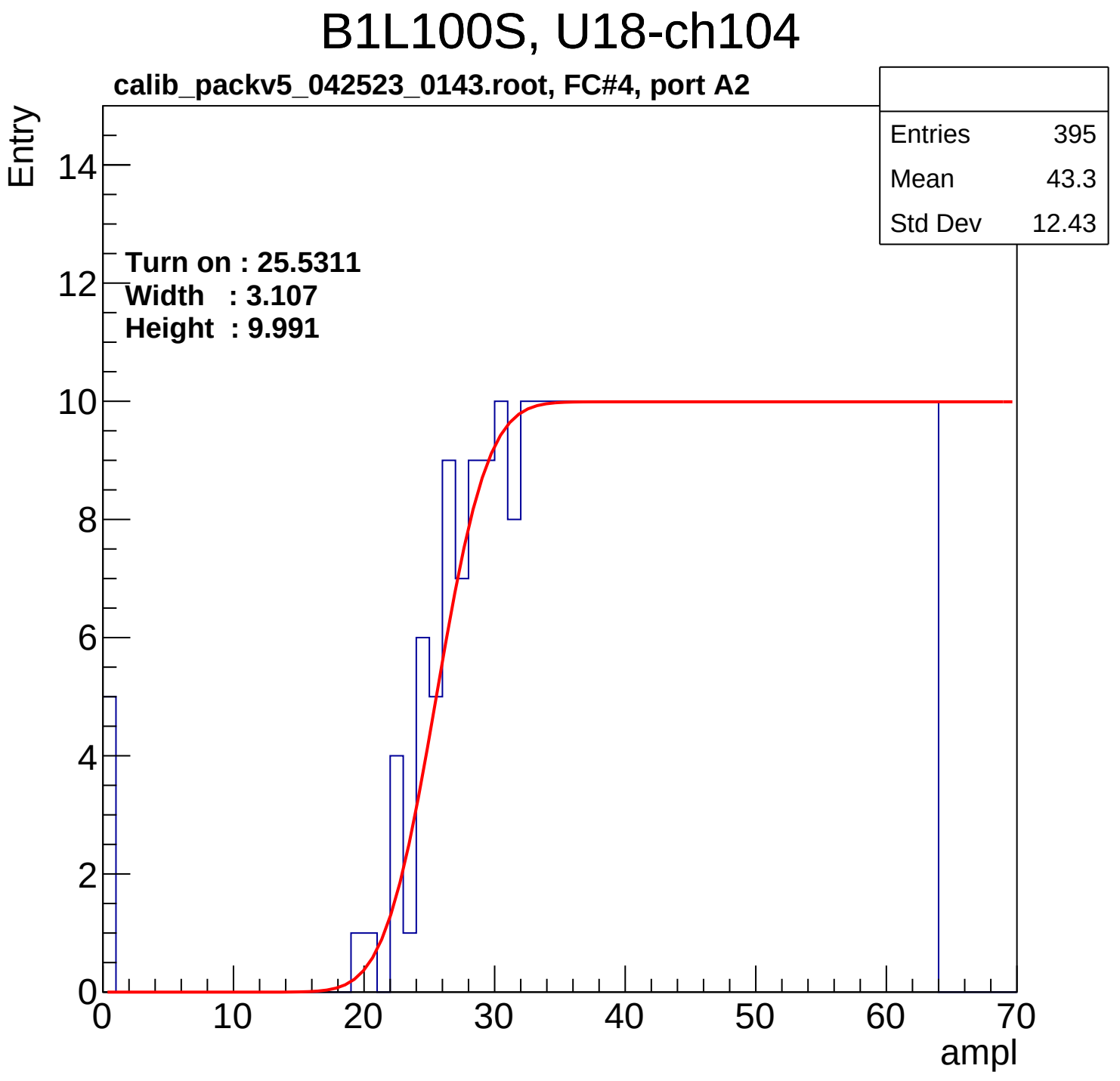
B1L100S, U18-ch104
calib_packv5_042523_0143.root, FC#4, port A2
Entries 395
Mean 43.3
Std Dev 12.43
Turn on : 25.5311
Width : 3.107
Height : 9.991
Entry
ampl
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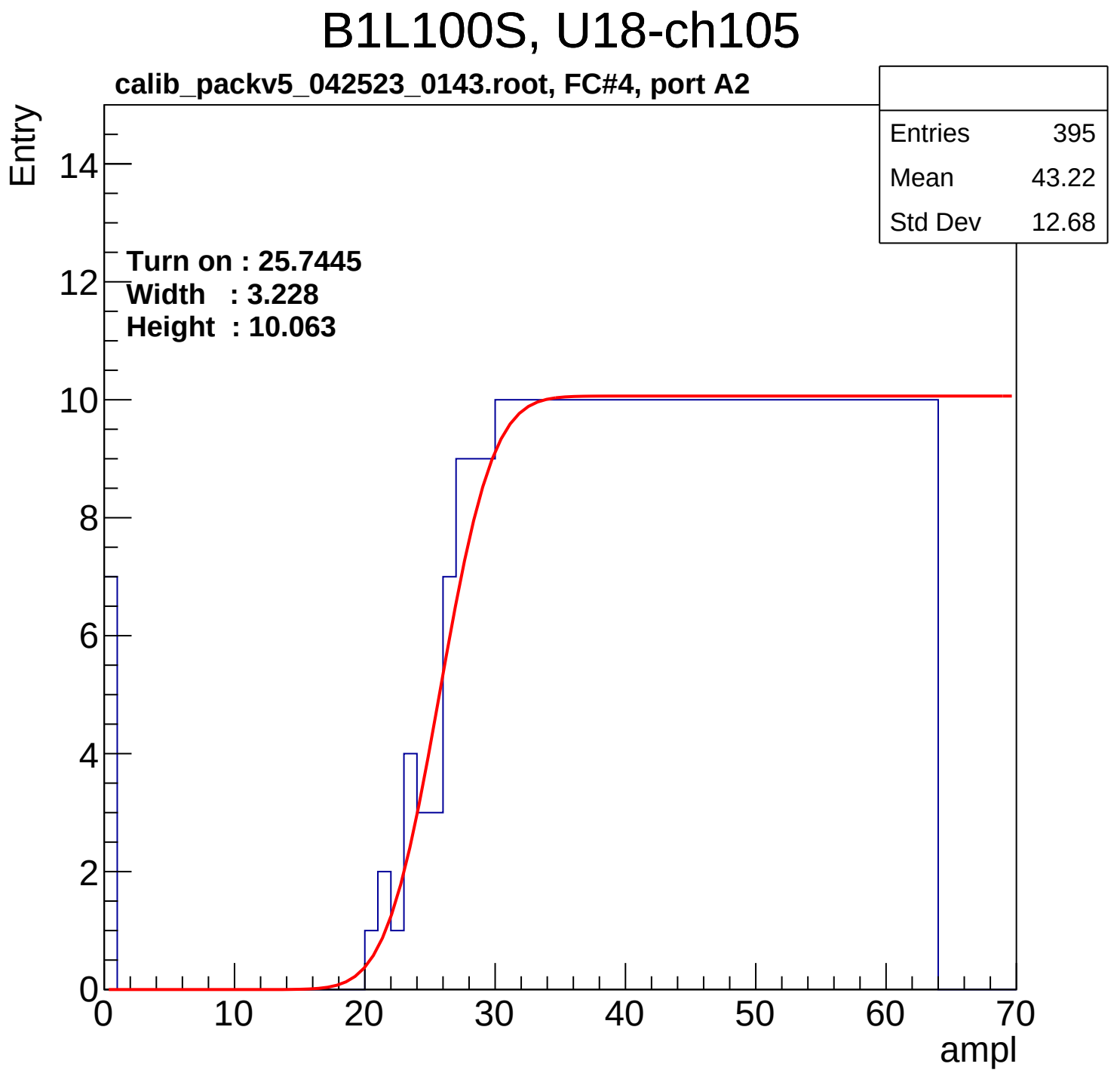
B1L100S, U18-ch105
calib_packv5_042523_0143.root, FC#4, port A2
Entries 395
Mean 43.22
Std Dev 12.68
Turn on : 25.7445
Width : 3.228
Height : 10.063
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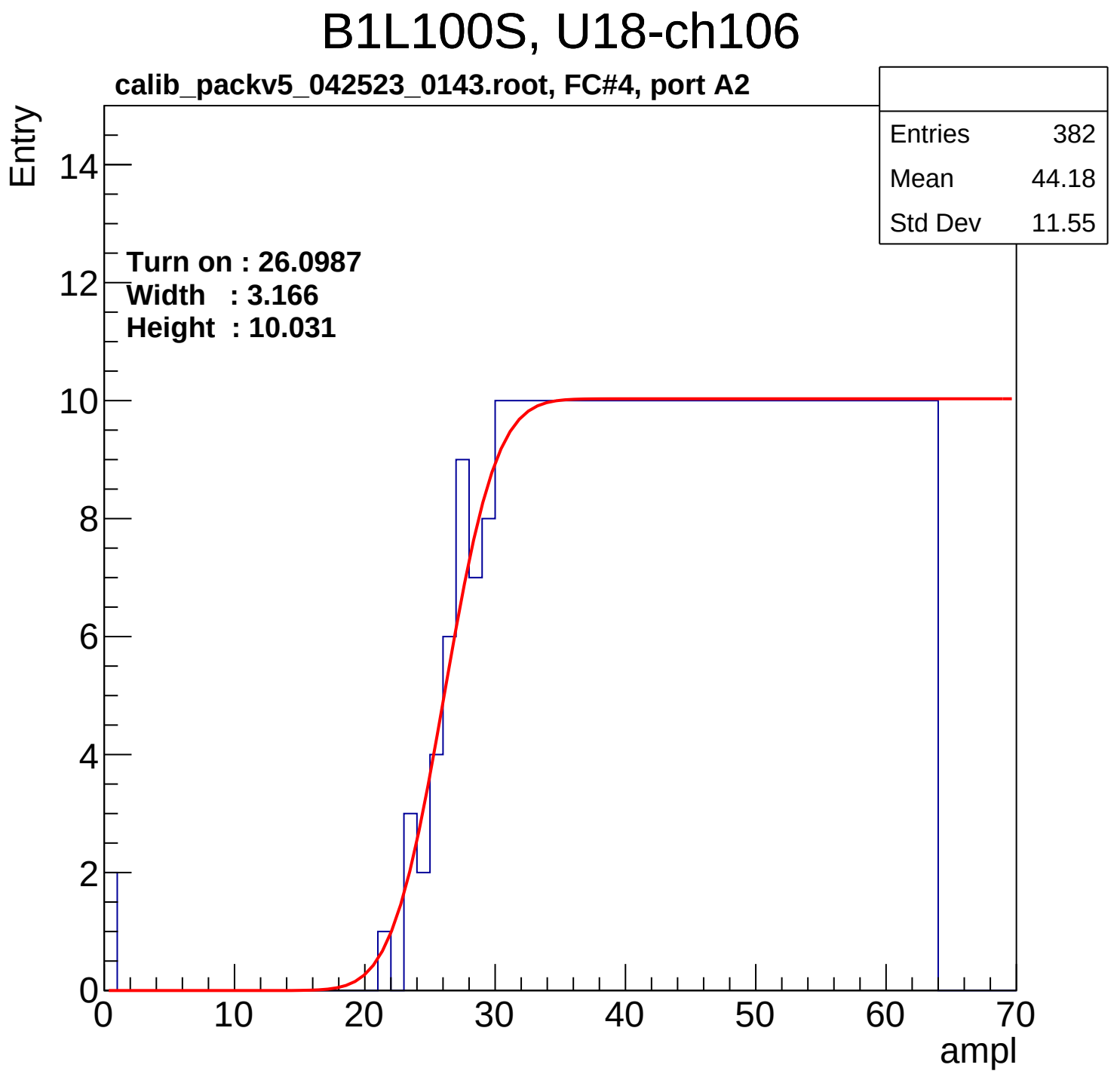
B1L100S, U18-ch106
calib_packv5_042523_0143.root, FC#4, port A2
Entries 382
Mean 44.18
Std Dev 11.55
Turn on : 26.0987
Width : 3.166
Height : 10.031
Entry
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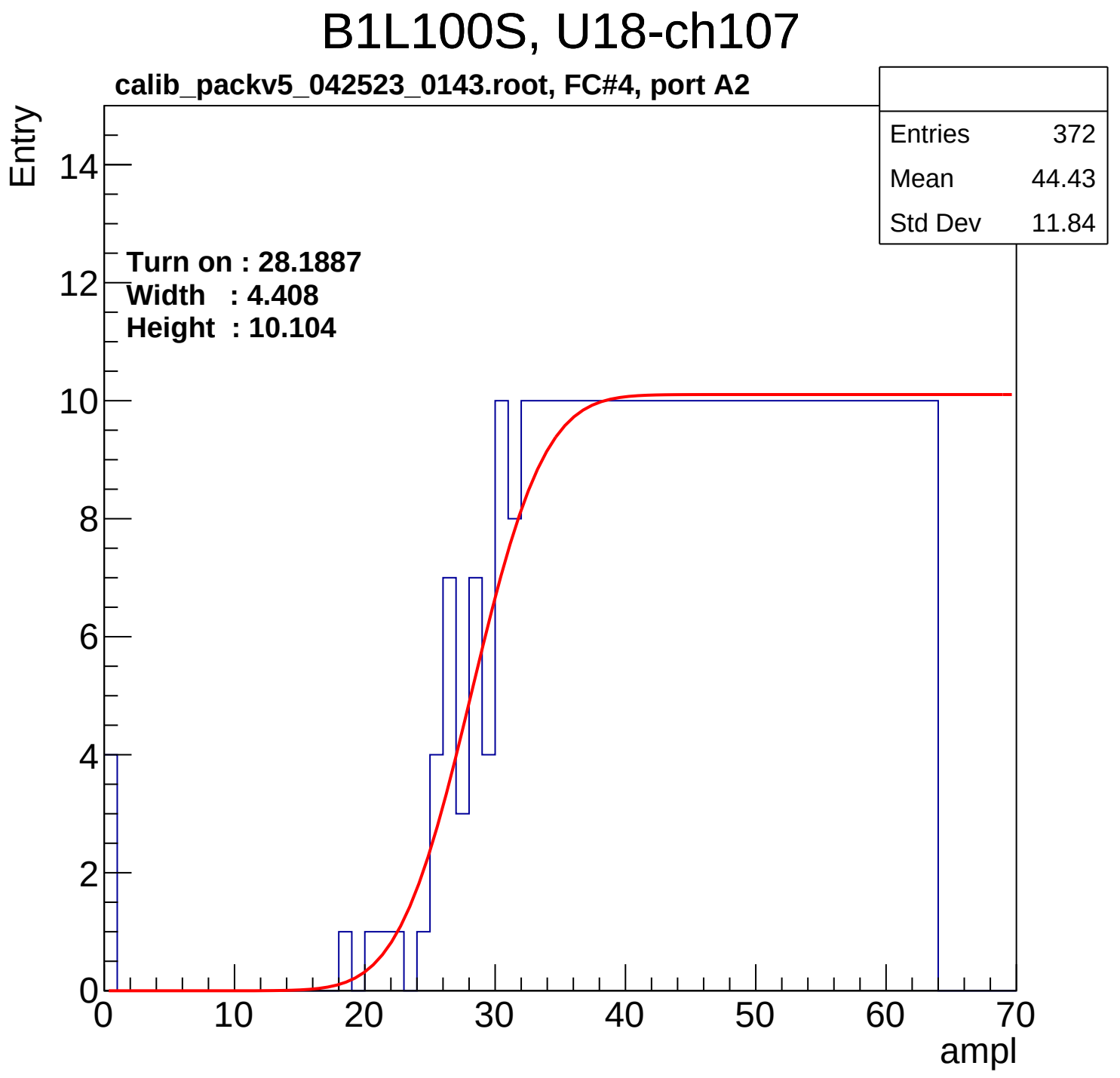
B1L100S, U18-ch107
calib_packv5_042523_0143.root, FC#4, port A2
Entries 372
Mean 44.43
Std Dev 11.84
Turn on : 28.1887
Width : 4.408
Height : 10.104
Entry
ampl
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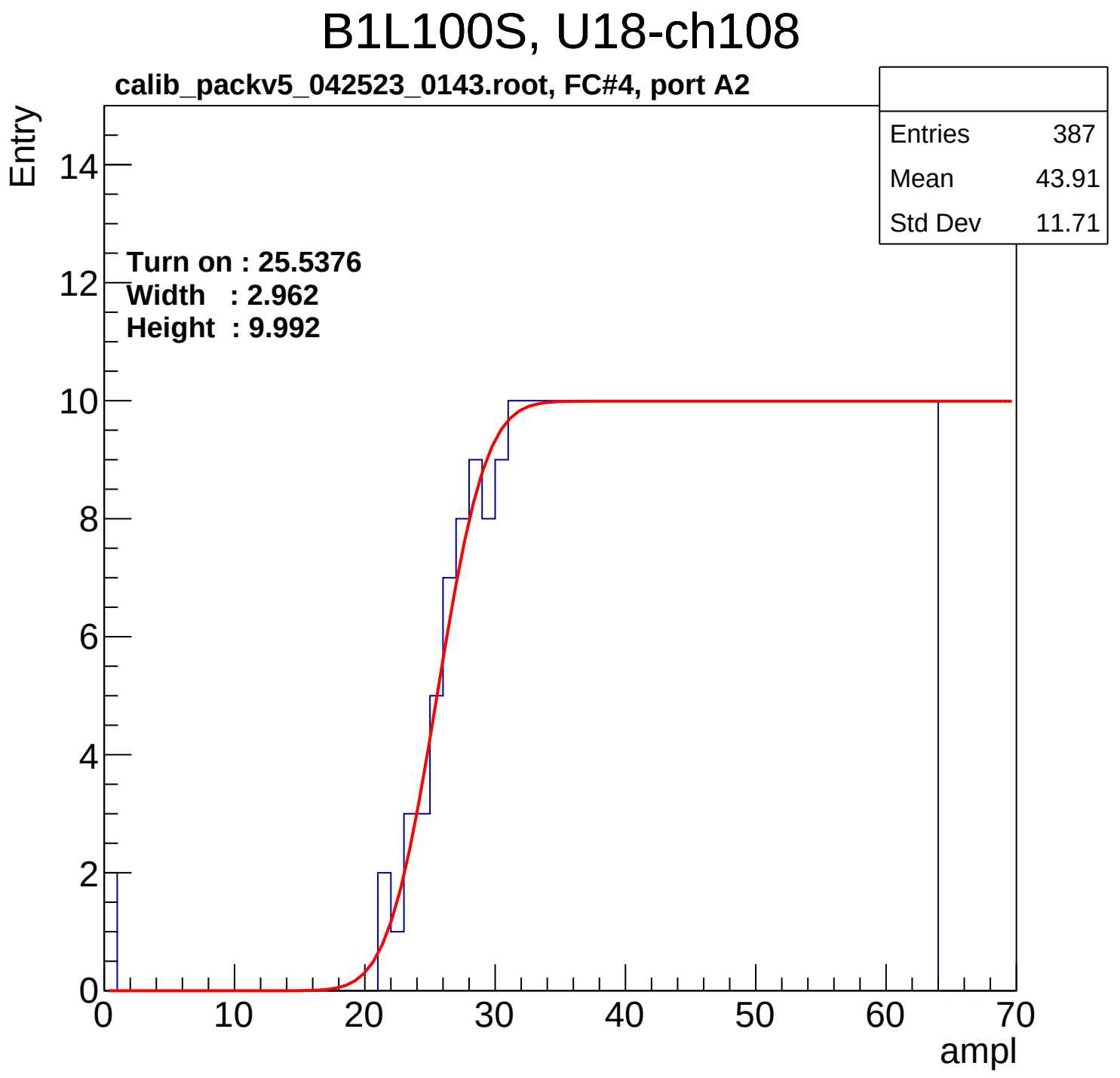
B1L100S, U18-ch108
calib_packv5_042523_0143.root, FC#4, port A2
Entries 387
Mean 43.91
Std Dev 11.71
Turn on : 25.5376
Width : 2.962
Height : 9.992
Entry
ampl
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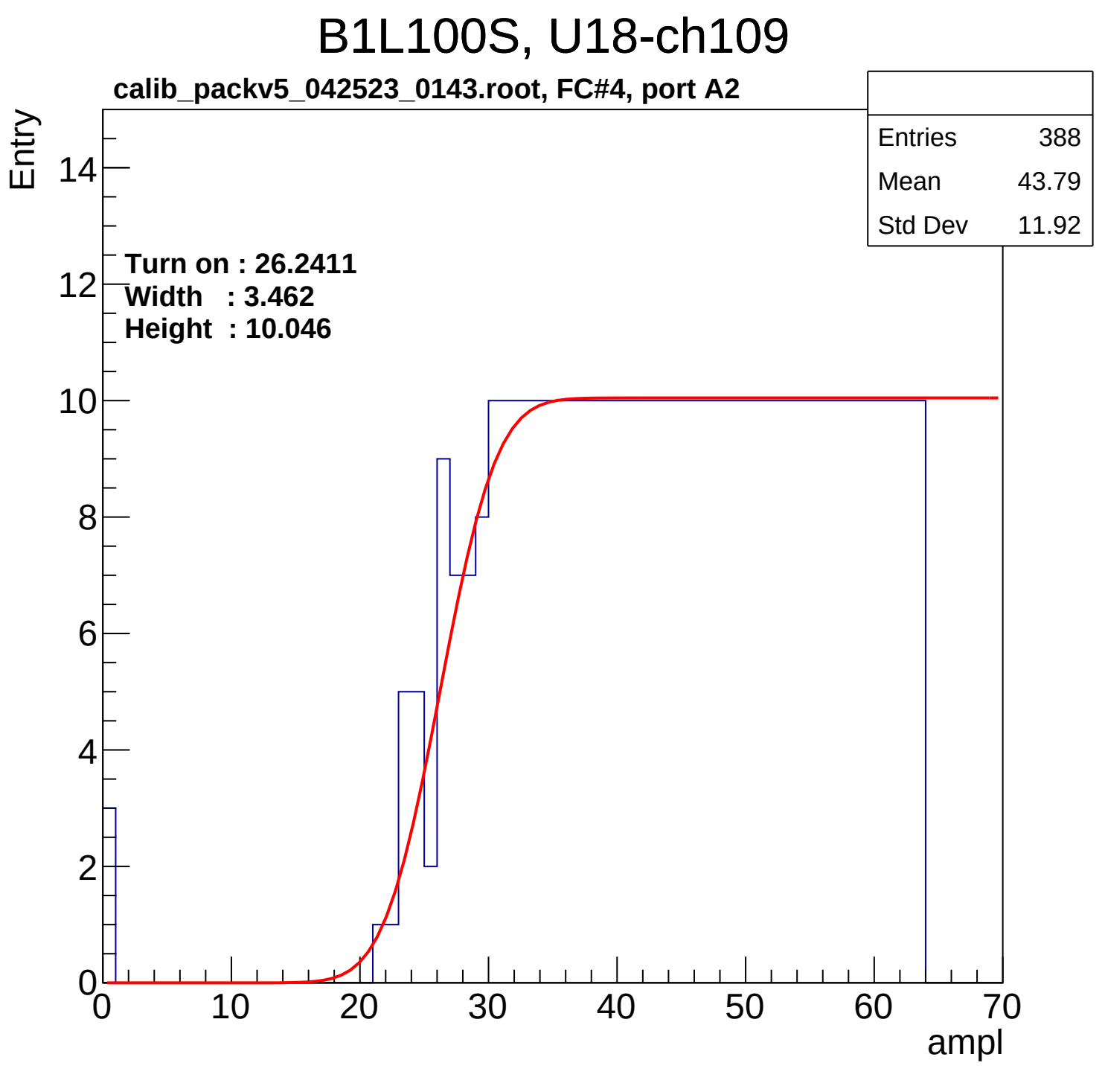
B1L100S, U18-ch109
calib_packv5_042523_0143.root, FC#4, port A2
Entries 388
Mean 43.79
Std Dev 11.92
Turn on : 26.2411
Width : 3.462
Height : 10.046
Entry
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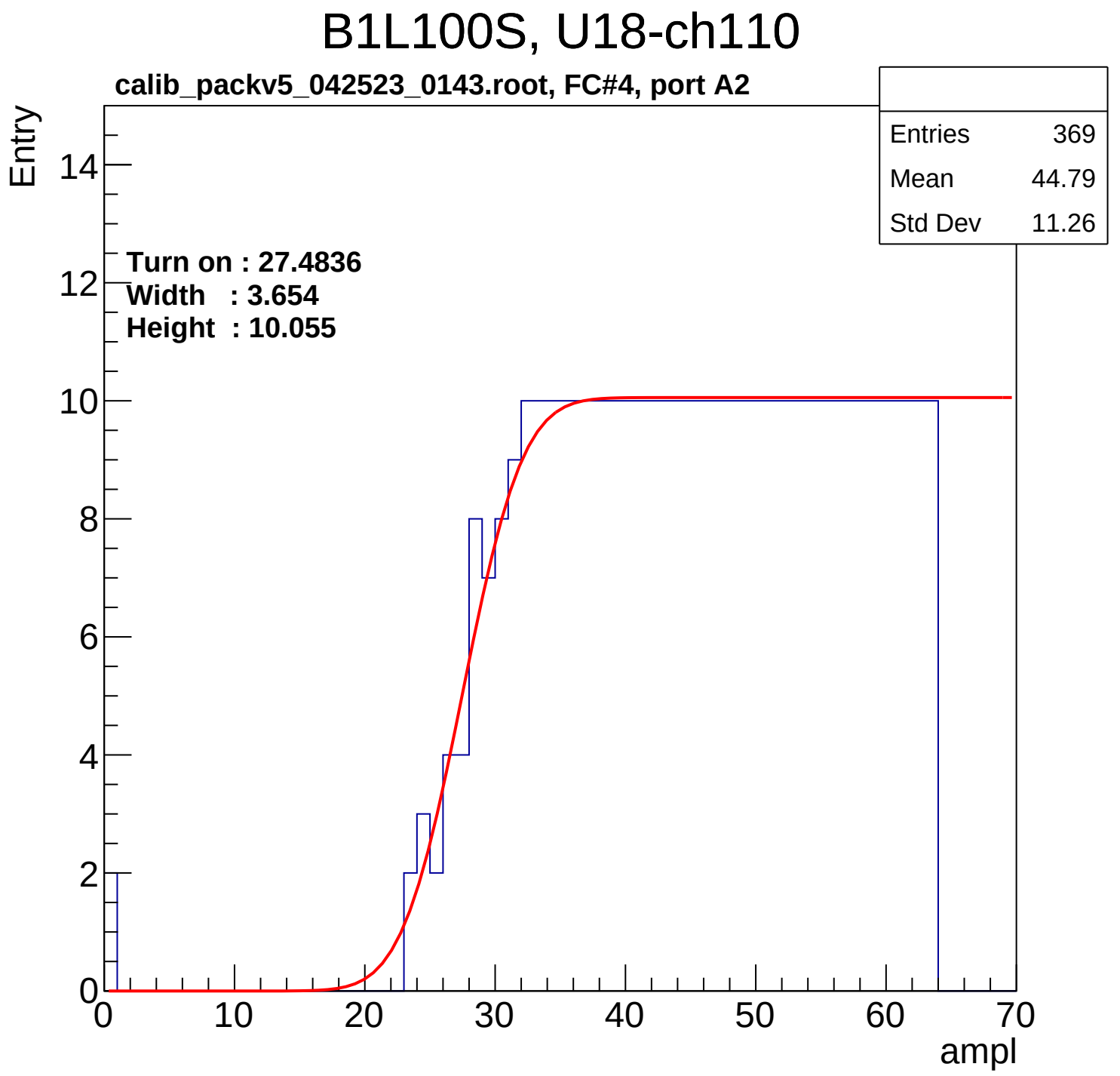
B1L100S, U18-ch110
calib_packv5_042523_0143.root, FC#4, port A2
Entries 369
Mean 44.79
Std Dev 11.26
Turn on : 27.4836
Width : 3.654
Height : 10.055
Entry
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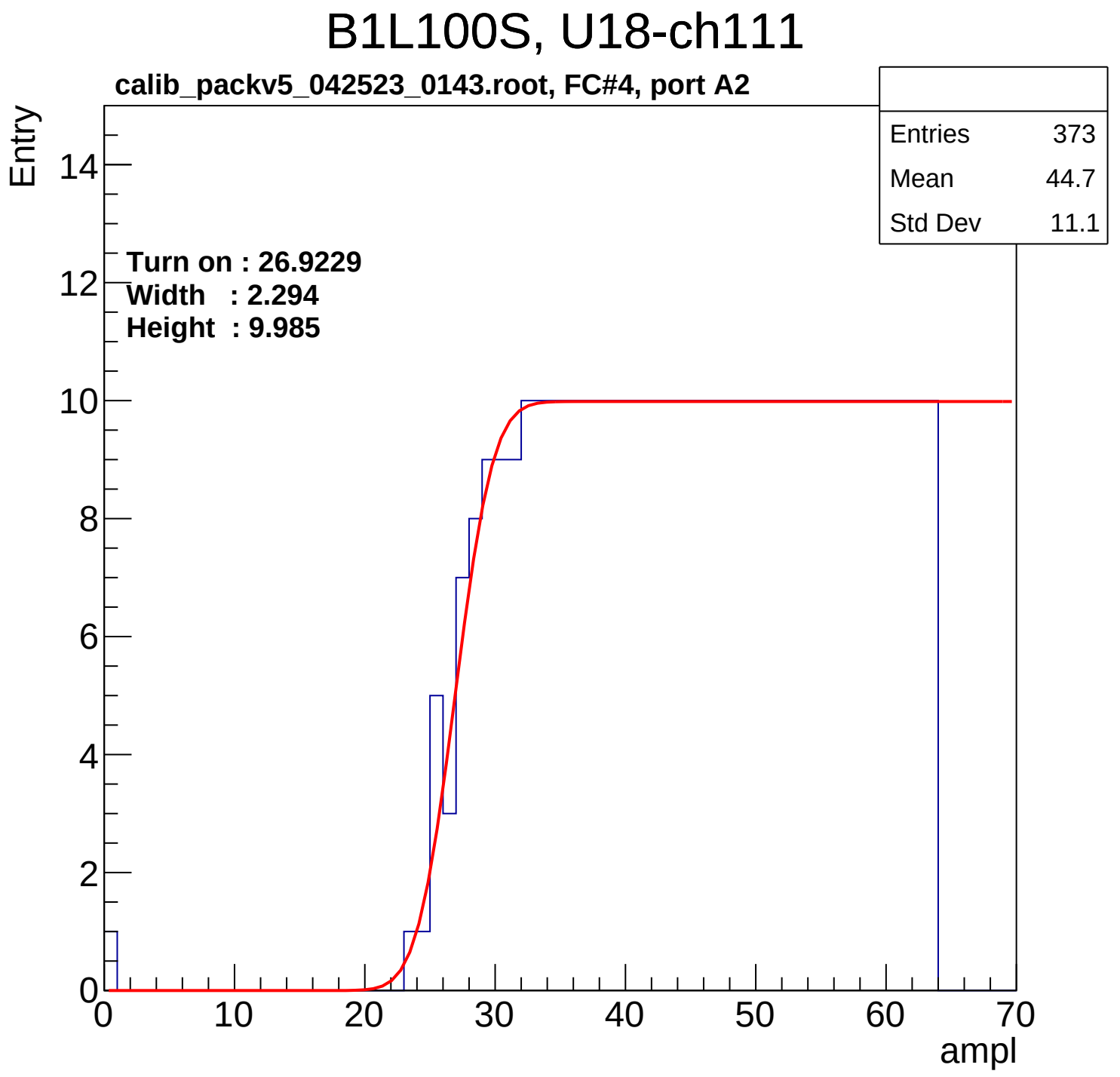
B1L100S, U18-ch111
calib_packv5_042523_0143.root, FC#4, port A2
Entries 373
Mean 44.7
Std Dev 11.1
Turn on : 26.9229
Width : 2.294
Height : 9.985
Entry
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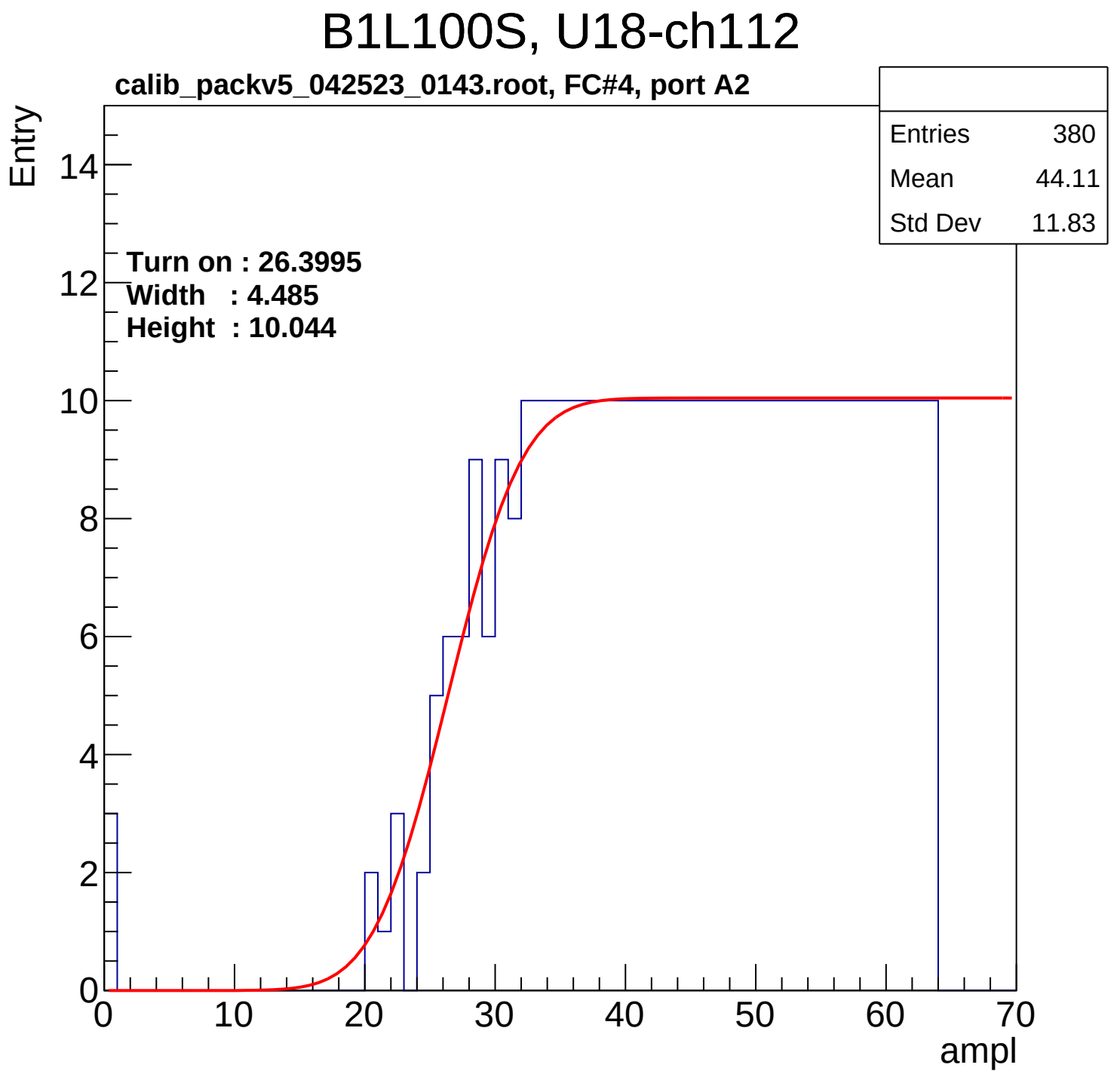
B1L100S, U18-ch112
calib_packv5_042523_0143.root, FC#4, port A2
Entries 380
Mean 44.11
Std Dev 11.83
Turn on : 26.3995
Width : 4.485
Height : 10.044
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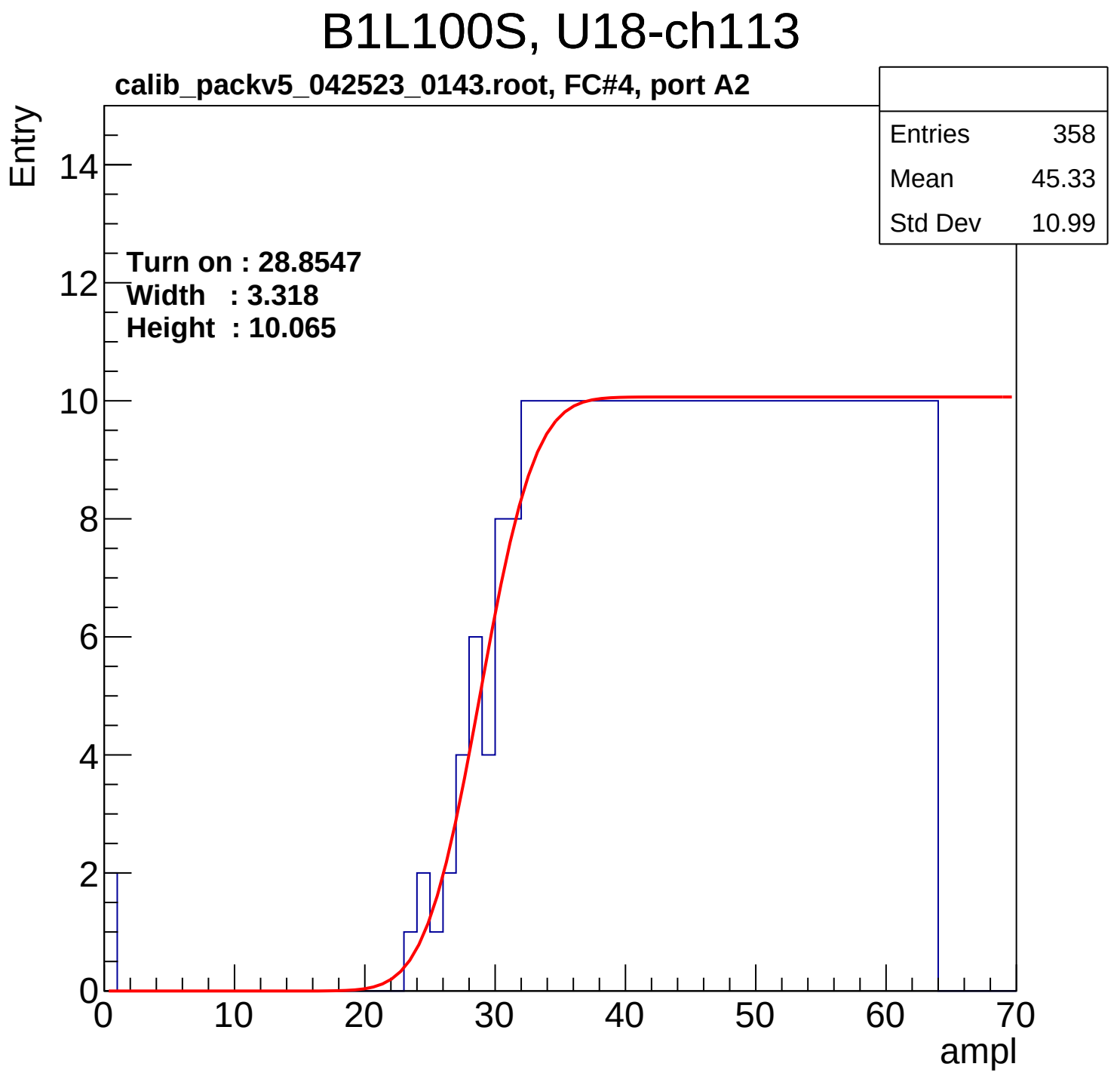
B1L100S, U18-ch113
calib_packv5_042523_0143.root, FC#4, port A2
Entries 358
Mean 45.33
Std Dev 10.99
Turn on : 28.8547
Width : 3.318
Height : 10.065
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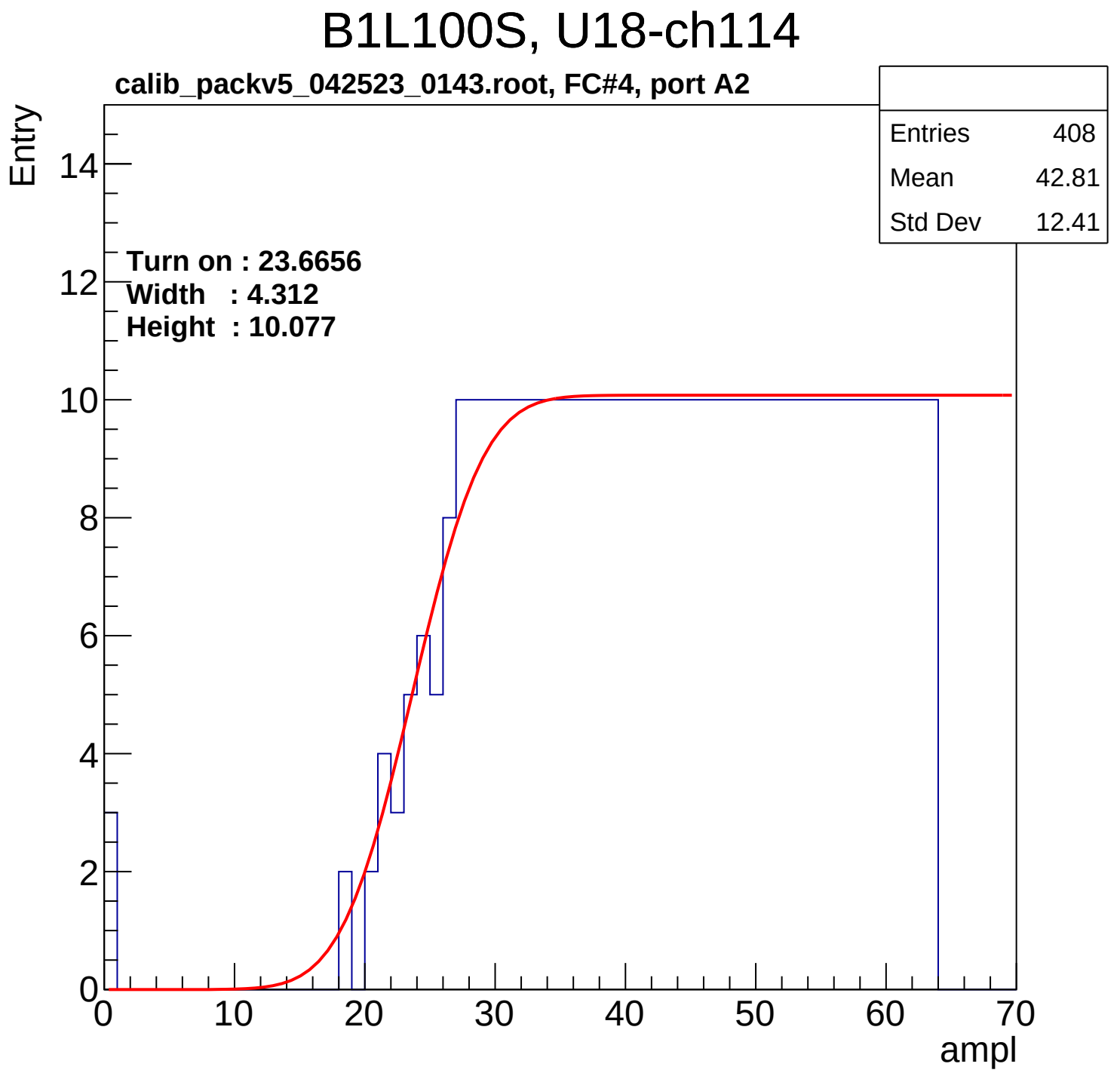
B1L100S, U18-ch114
calib_packv5_042523_0143.root, FC#4, port A2
Entries 408
Mean 42.81
Std Dev 12.41
Turn on : 23.6656
Width : 4.312
Height : 10.077
Entry
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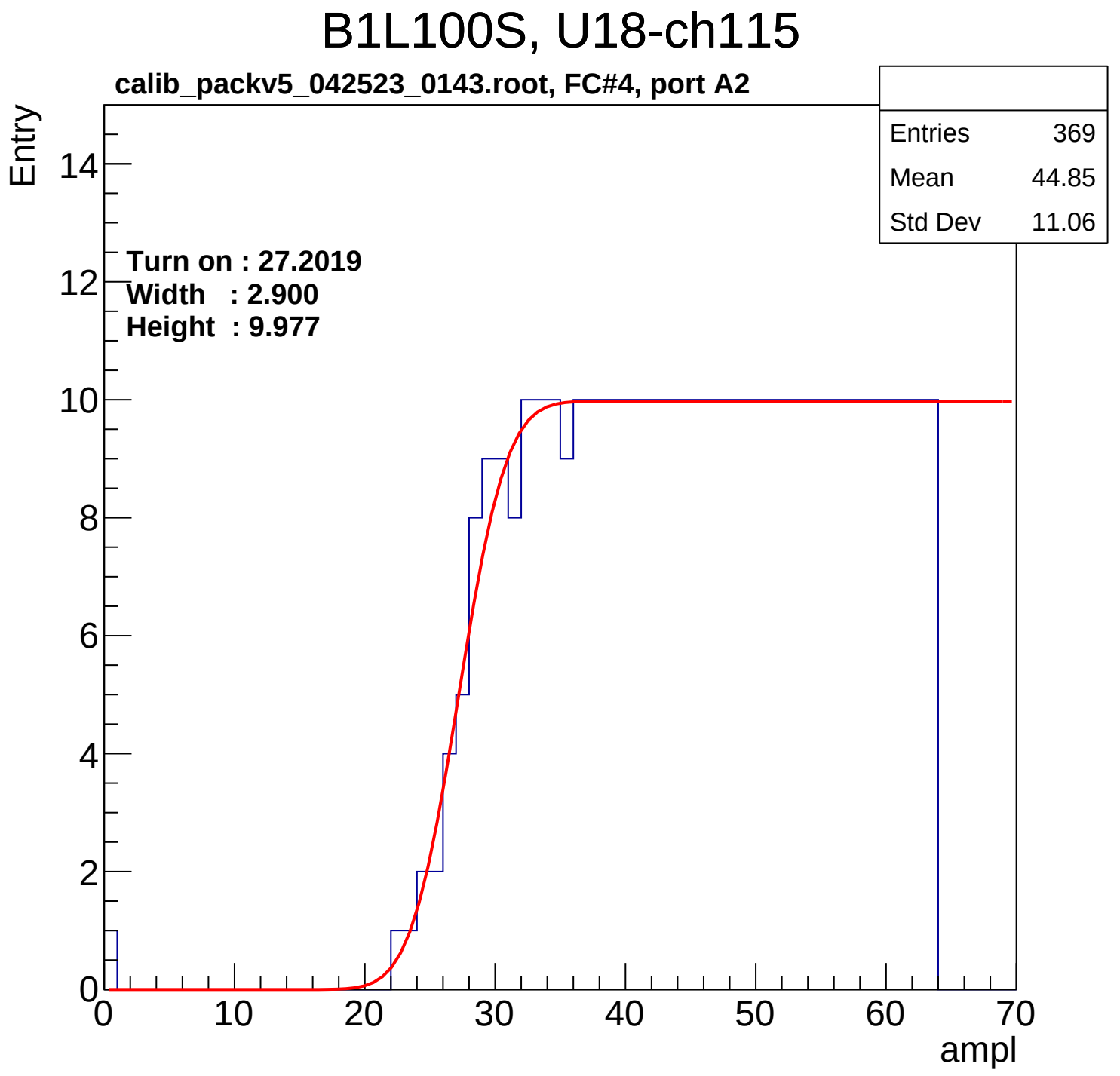
B1L100S, U18-ch115
calib_packv5_042523_0143.root, FC#4, port A2
Entries 369
Mean 44.85
Std Dev 11.06
Turn on : 27.2019
Width : 2.900
Height : 9.977
Entry
ampl
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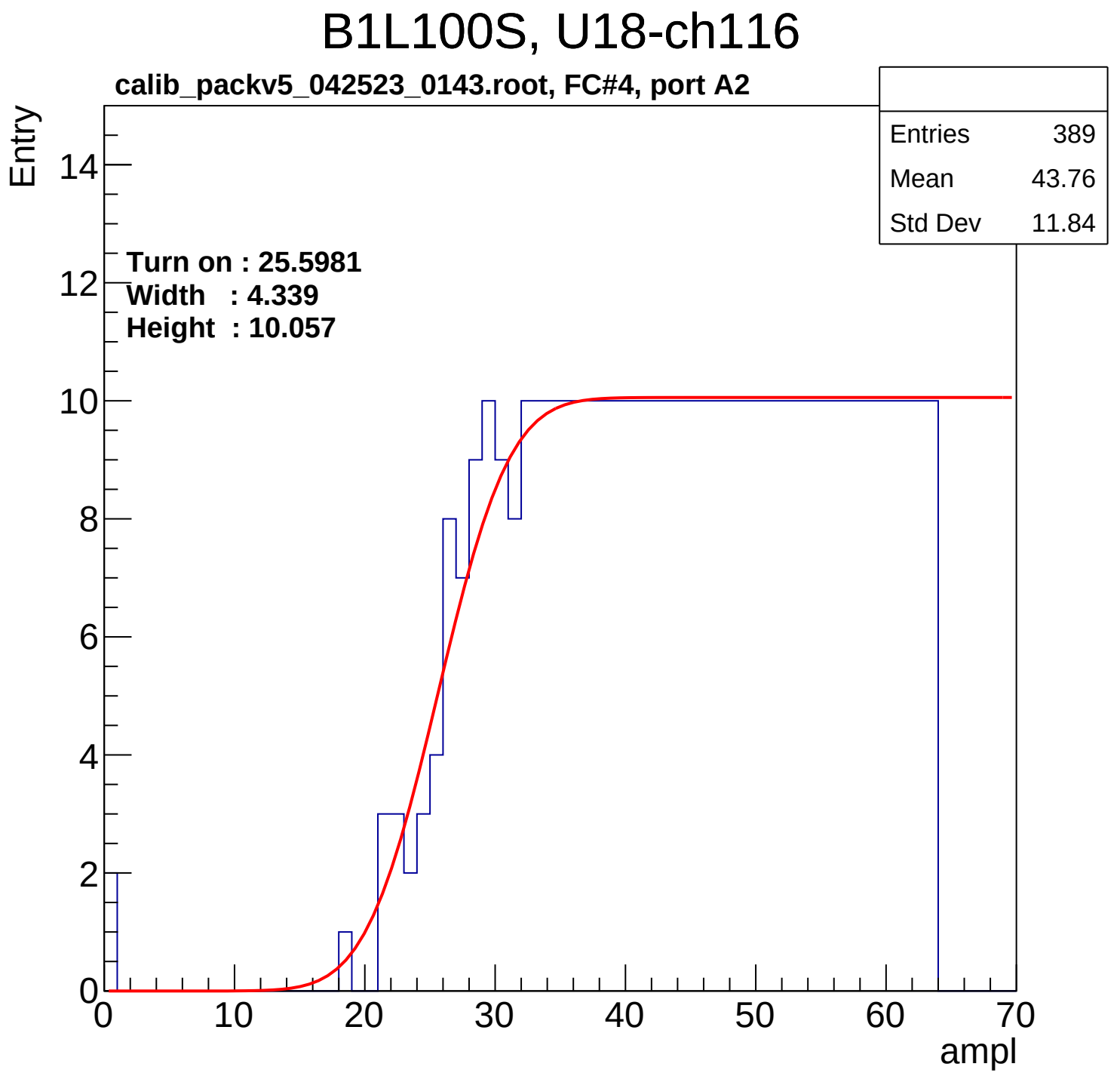
B1L100S, U18-ch116
calib_packv5_042523_0143.root, FC#4, port A2
Entries 389
Mean 43.76
Std Dev 11.84
Turn on : 25.5981
Width : 4.339
Height : 10.057
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
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40
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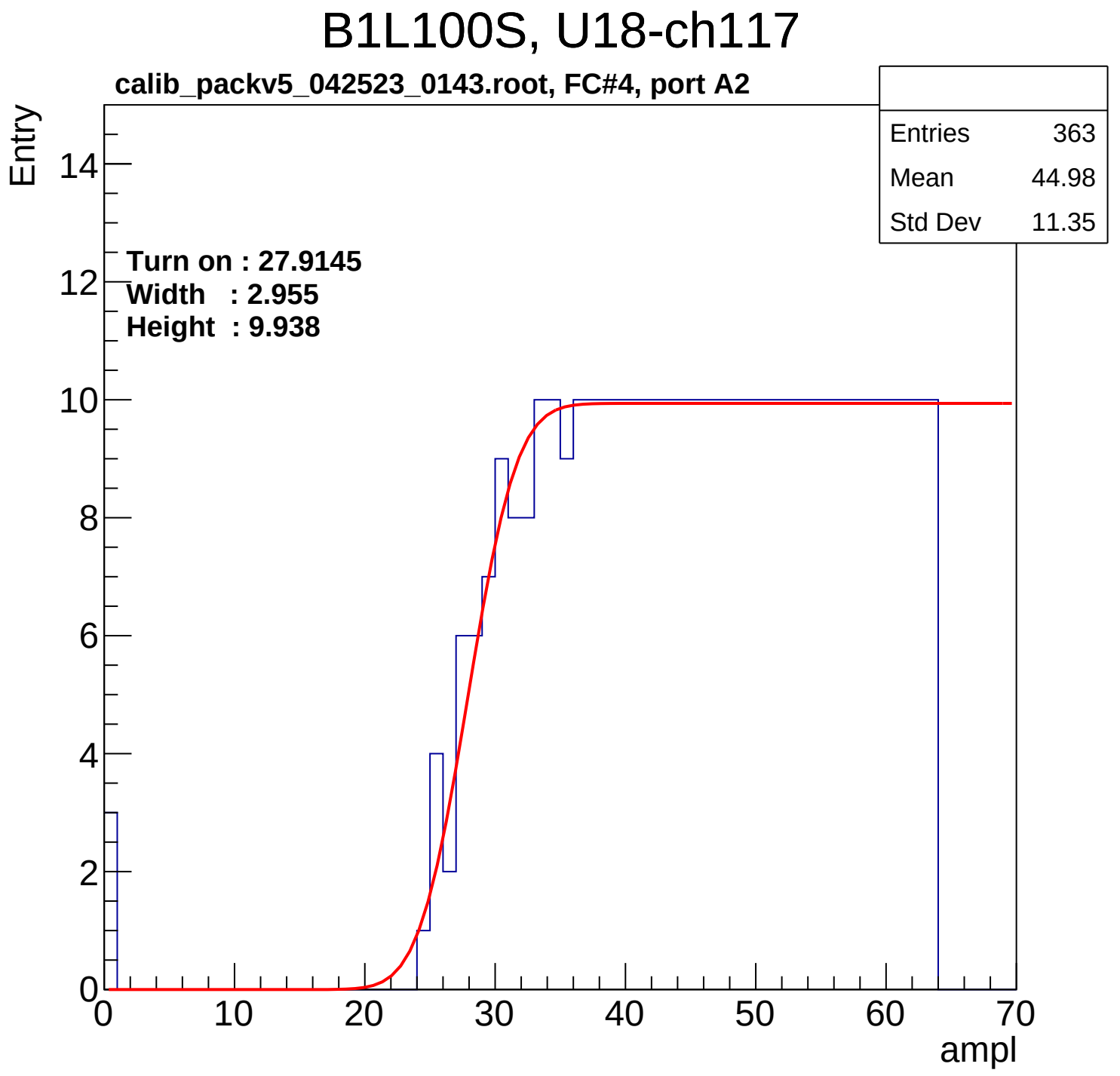
B1L100S, U18-ch117
calib_packv5_042523_0143.root, FC#4, port A2
Entries 363
Mean 44.98
Std Dev 11.35
Turn on : 27.9145
Width : 2.955
Height : 9.938
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
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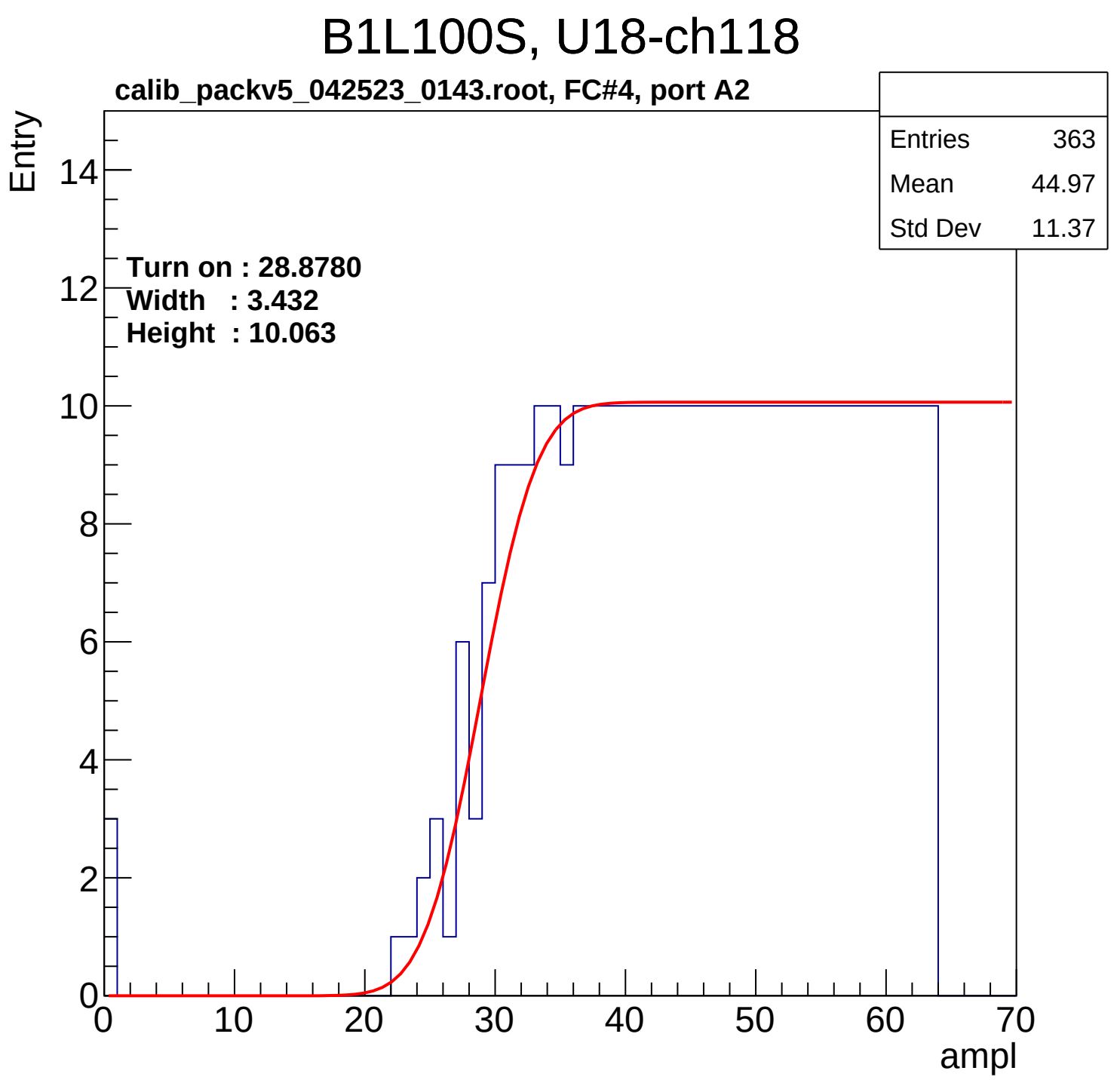
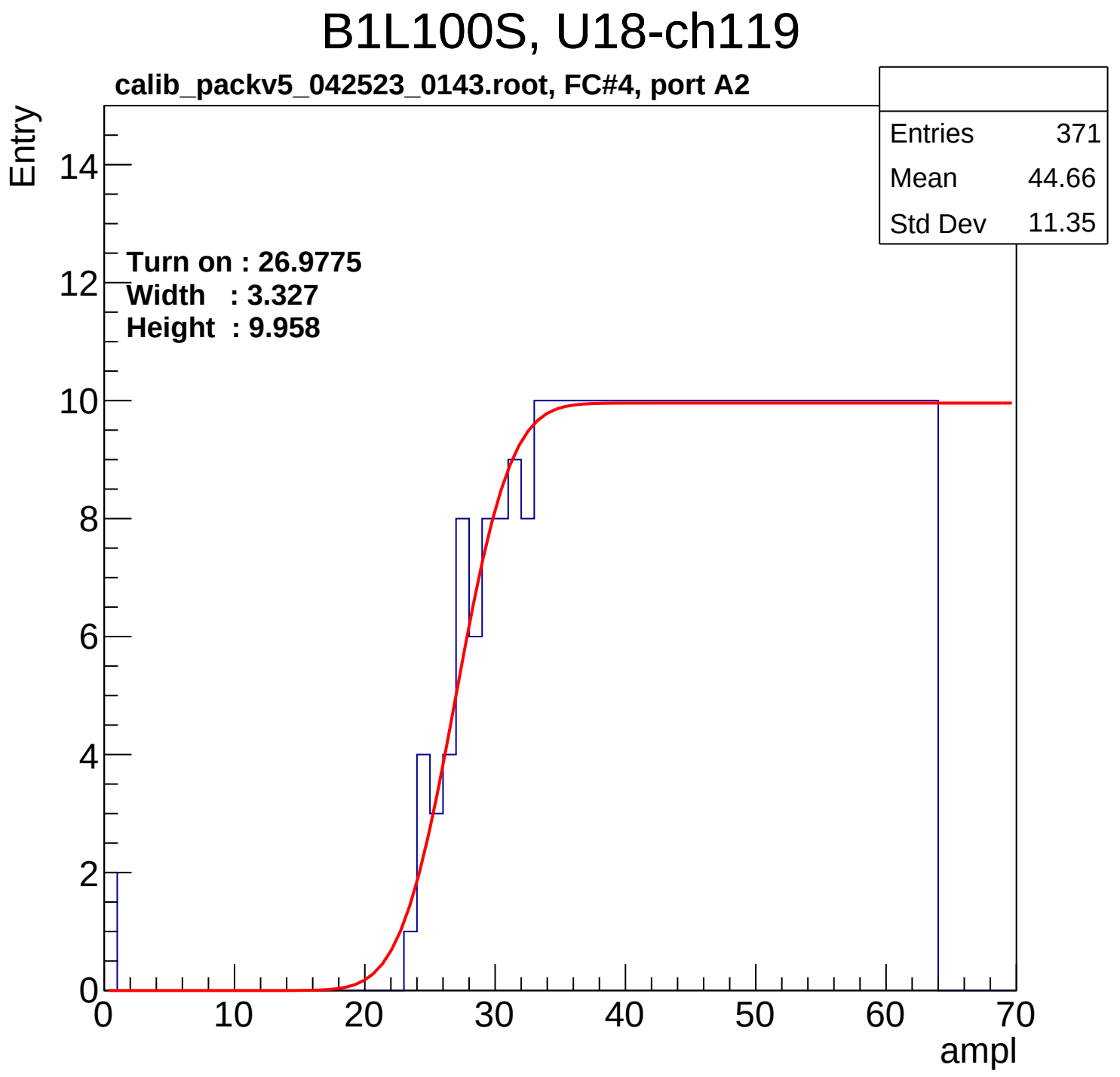
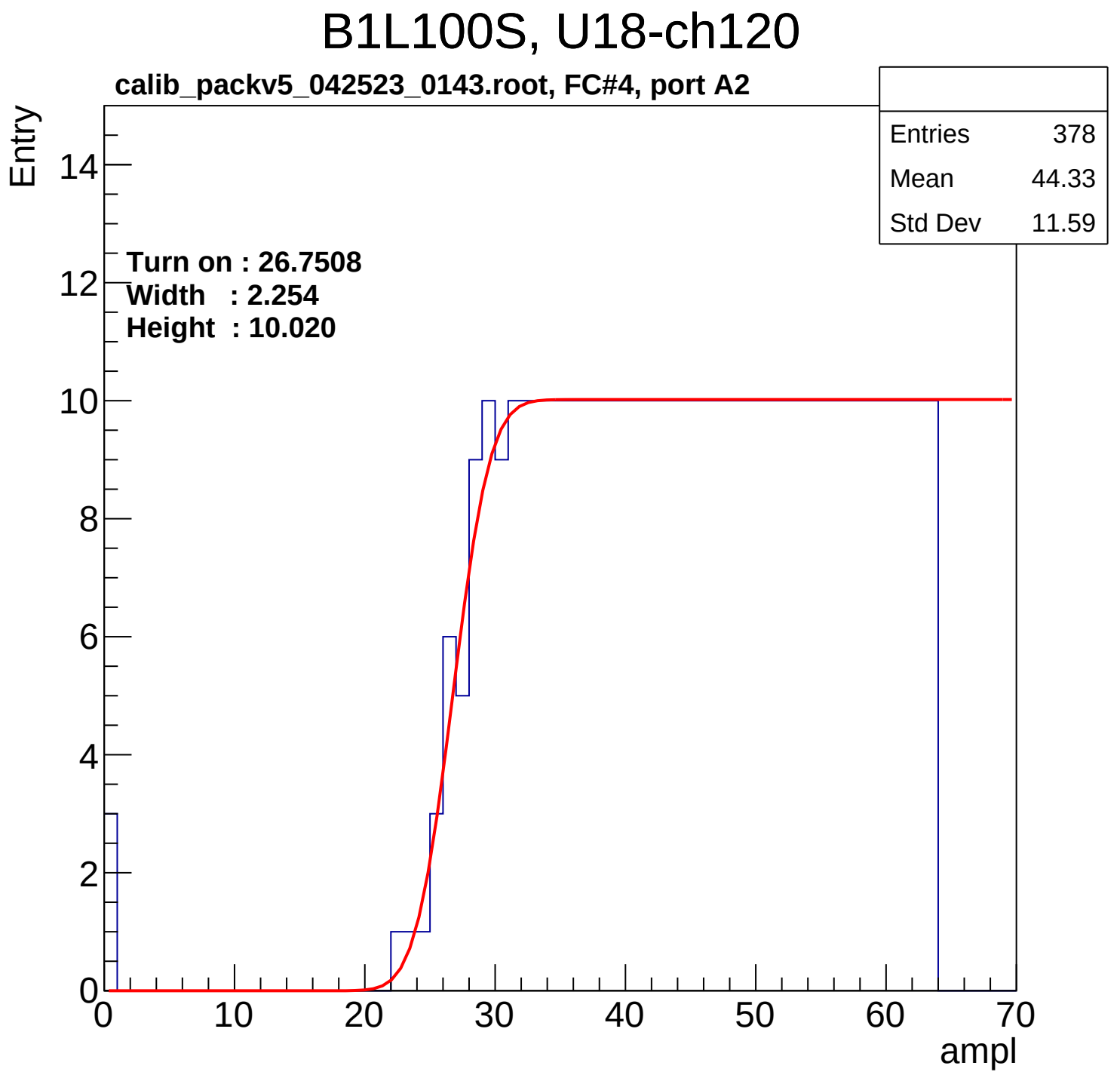
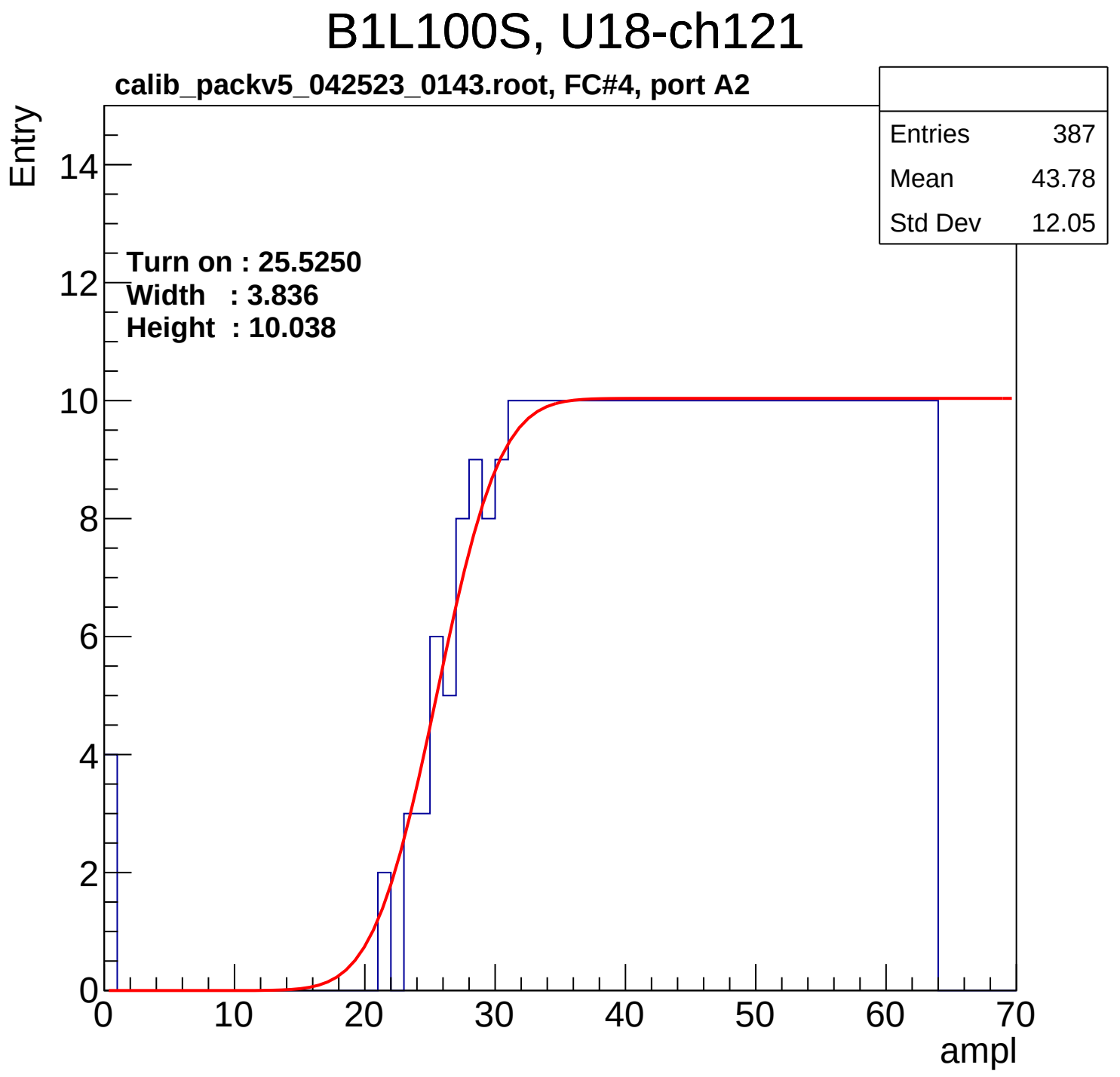
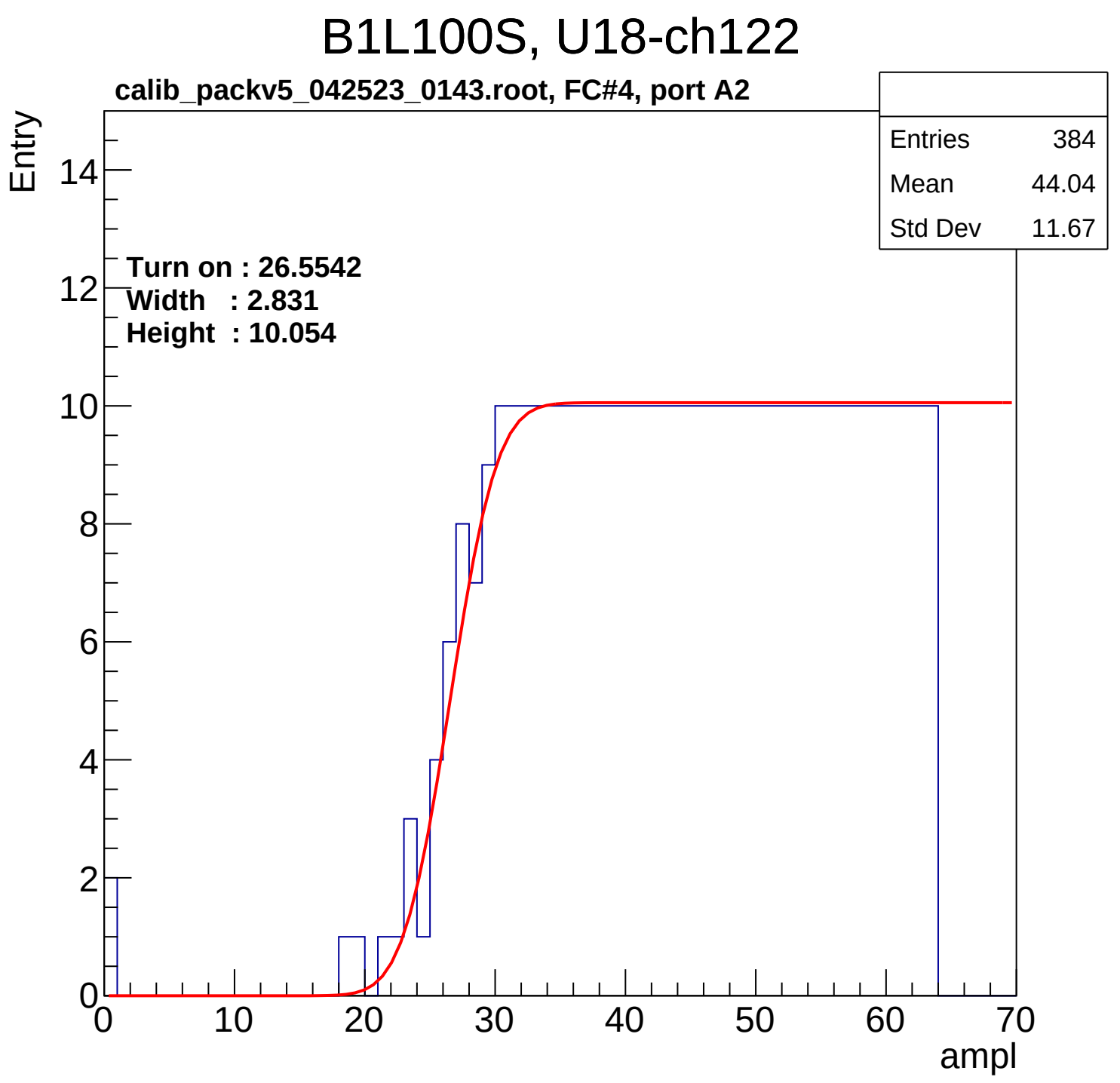
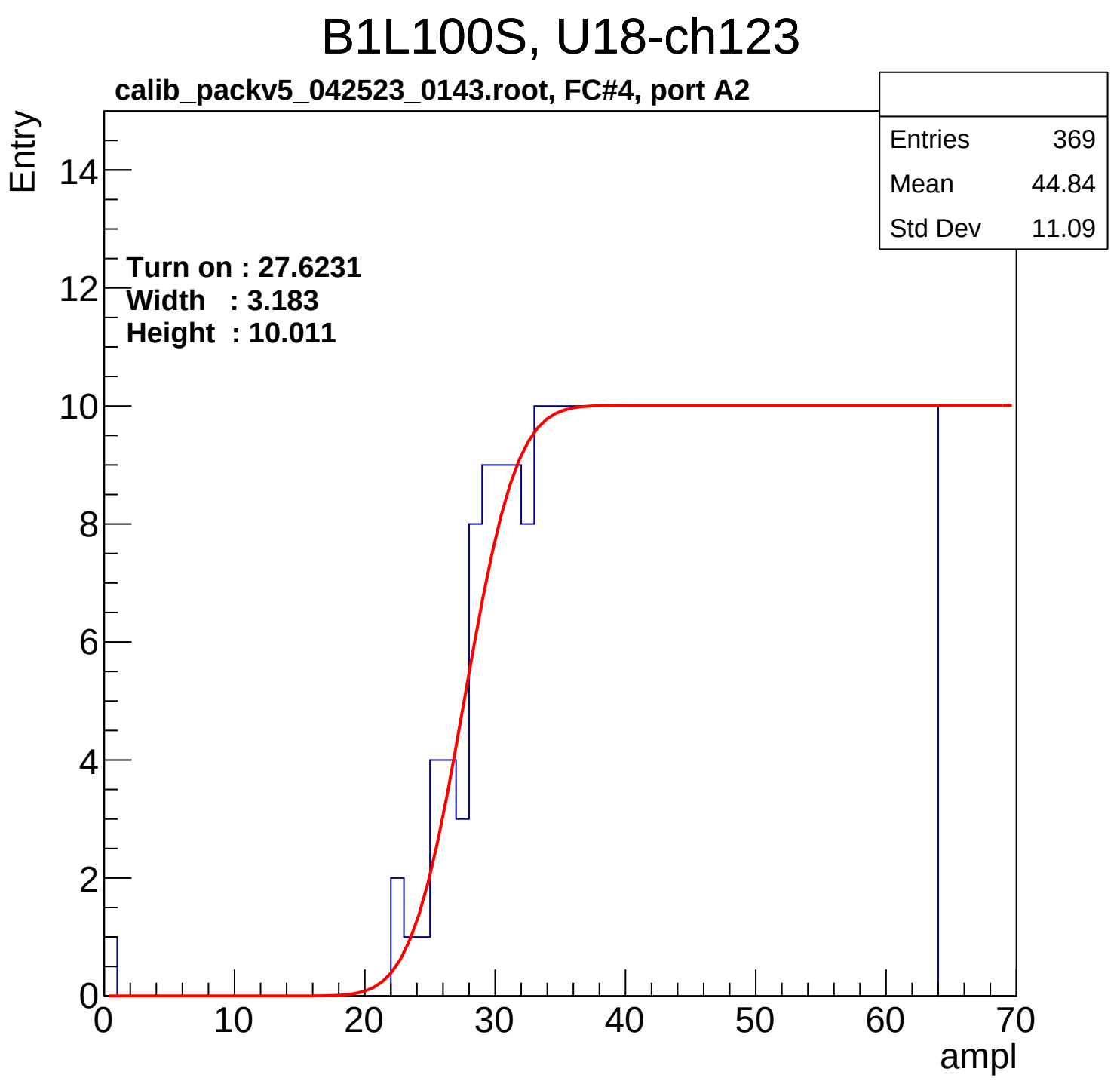

B1L100S, U18-ch118
calib_packv5_042523_0143.root, FC#4, port A2
Entries 363
Mean 44.97
Std Dev 11.37
Turn on : 28.8780
Width : 3.432
Height : 10.063
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70

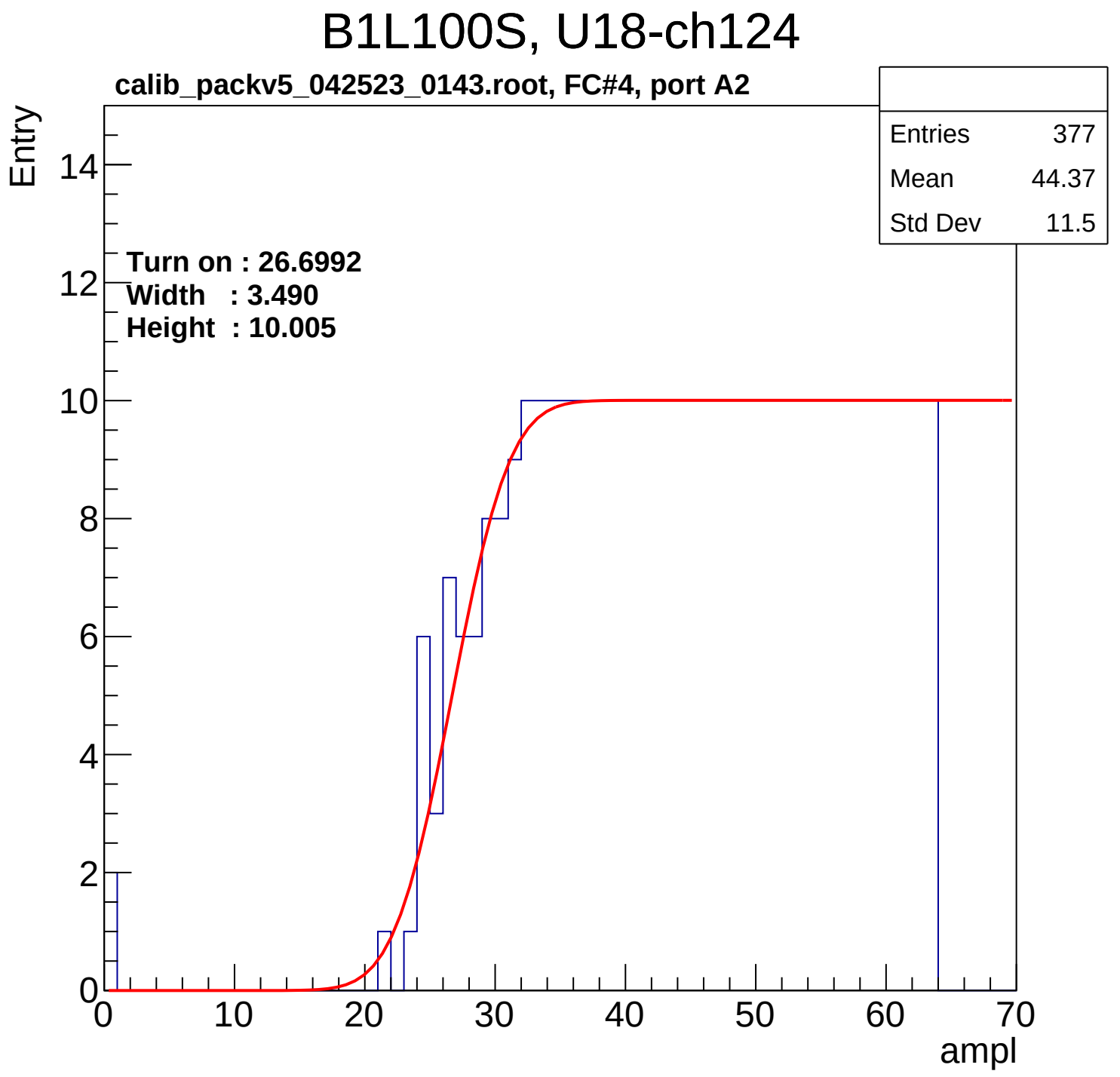

B1L100S, U18-ch119
calib_packv5_042523_0143.root, FC#4, port A2
Entries 371
Mean 44.66
Std Dev 11.35
Turn on : 26.9775
Width : 3.327
Height : 9.958
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L100S, U18-ch120
calib_packv5_042523_0143.root, FC#4, port A2
Entries 378
Mean 44.33
Std Dev 11.59
Turn on : 26.7508
Width : 2.254
Height : 10.020
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L100S, U18-ch121
calib_packv5_042523_0143.root, FC#4, port A2
Entries 387
Mean 43.78
Std Dev 12.05
Turn on : 25.5250
Width : 3.836
Height : 10.038
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L100S, U18-ch122
calib_packv5_042523_0143.root, FC#4, port A2
Entries 384
Mean 44.04
Std Dev 11.67
Turn on : 26.5542
Width : 2.831
Height : 10.054
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L100S, U18-ch123
calib_packv5_042523_0143.root, FC#4, port A2
Entries 369
Mean 44.84
Std Dev 11.09
Turn on : 27.6231
Width : 3.183
Height : 10.011
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L100S, U18-ch124
calib_packv5_042523_0143.root, FC#4, port A2
Entries 377
Mean 44.37
Std Dev 11.5
Turn on : 26.6992
Width : 3.490
Height : 10.005
Entry
ampl
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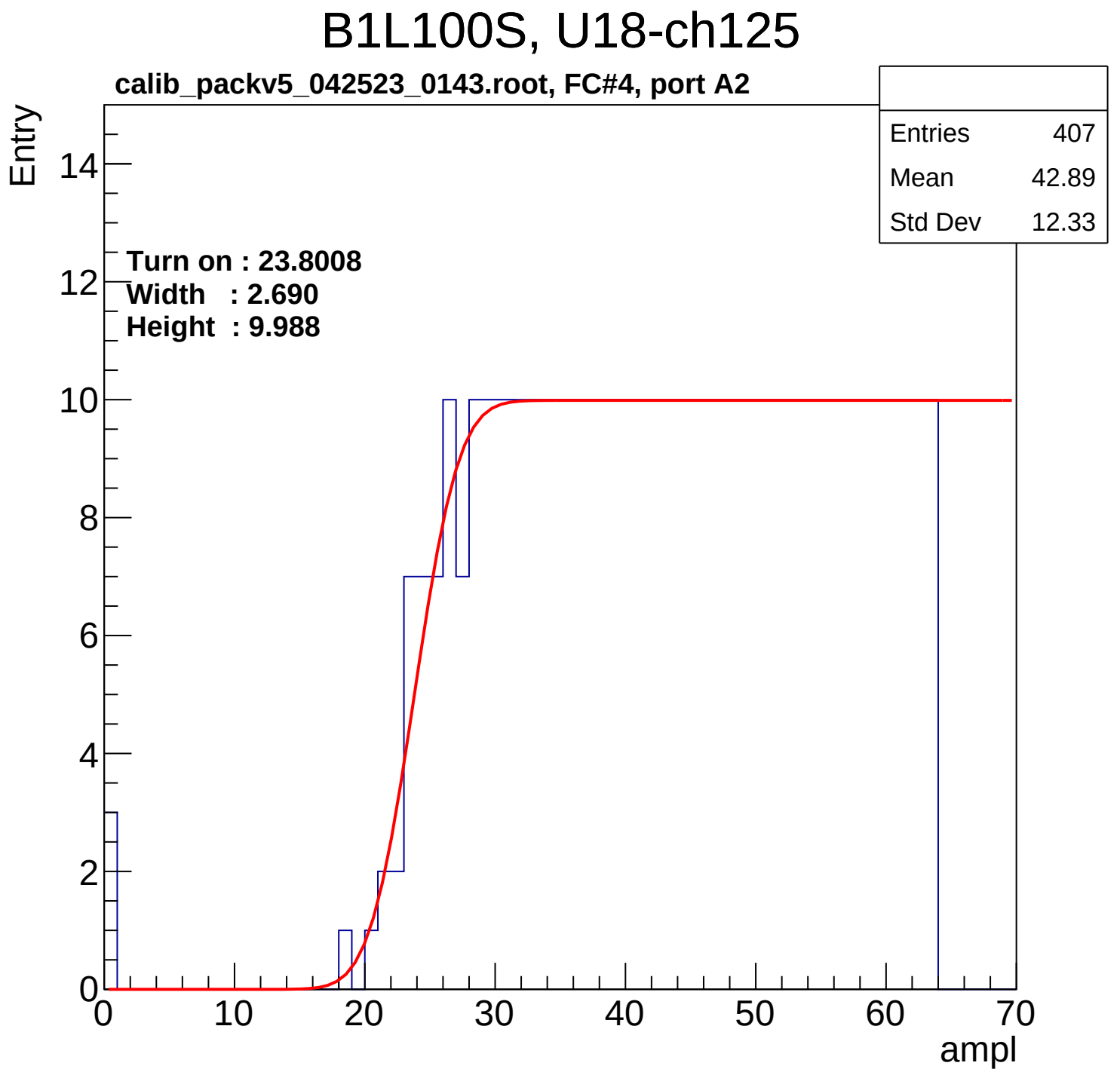
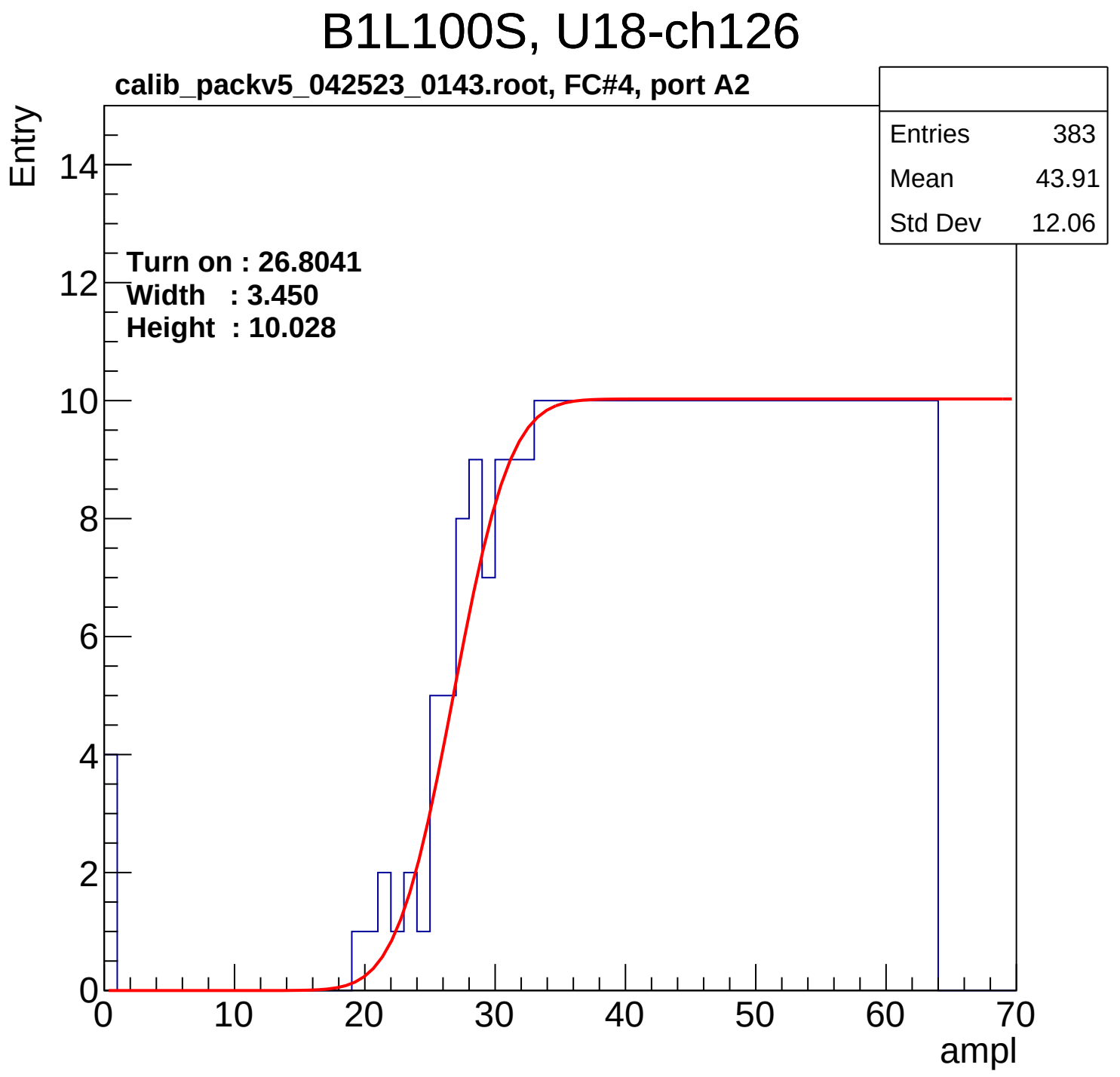
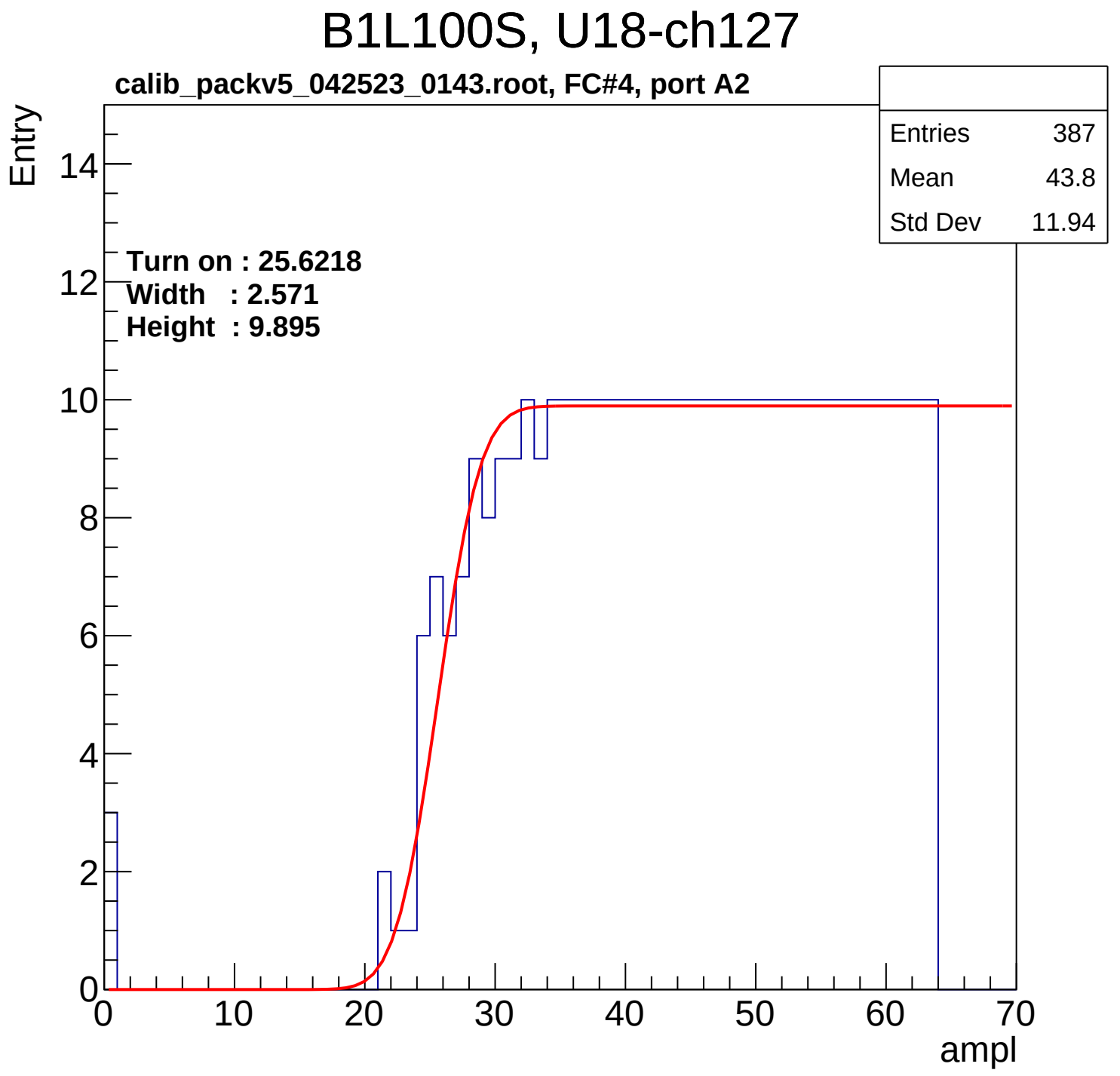
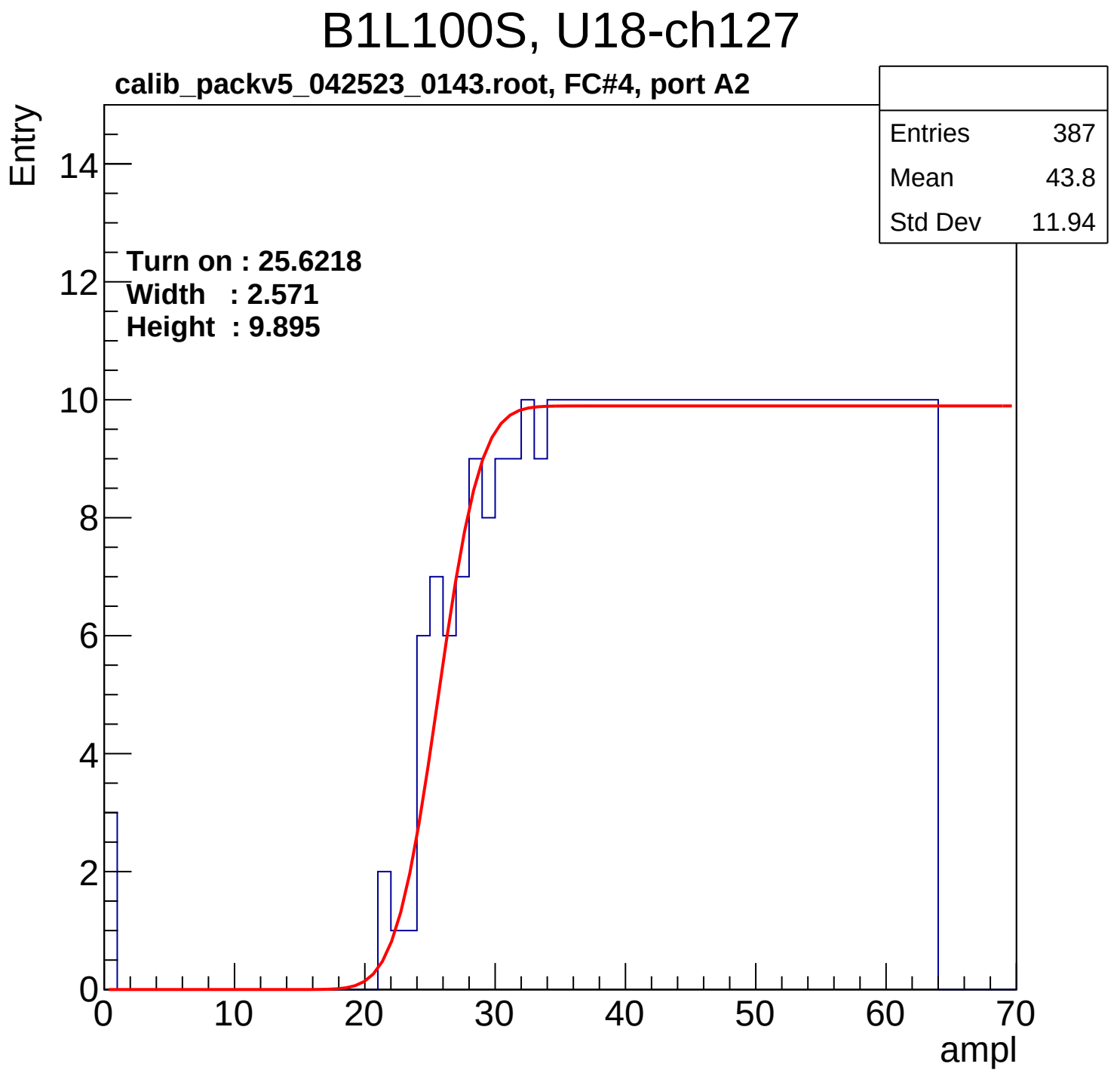
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L100S, U18-ch125
calib_packv5_042523_0143.root, FC#4, port A2
Entries 407
Mean 42.89
Std Dev 12.33
Turn on : 23.8008
Width : 2.690
Height : 9.988
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L100S, U18-ch126
calib_packv5_042523_0143.root, FC#4, port A2
Entries 383
Mean 43.91
Std Dev 12.06
Turn on : 26.8041
Width : 3.450
Height : 10.028
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L100S, U18-ch127
calib_packv5_042523_0143.root, FC#4, port A2
Entries 387
Mean 43.8
Std Dev 11.94
Turn on : 25.6218
Width : 2.571
Height : 9.895
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70


B1L100S, U18-ch127
calib_packv5_042523_0143.root, FC#4, port A2
Entries 387
Mean 43.8
Std Dev 11.94
Turn on : 25.6218
Width : 2.571
Height : 9.895
Entry
ampl
0
2
4
6
8
10
12
14
0
10
20
30
40
50
60
70