

B0L001S, U1-ch0

calib_packv5_042523_0143.root, FC#9, port A1

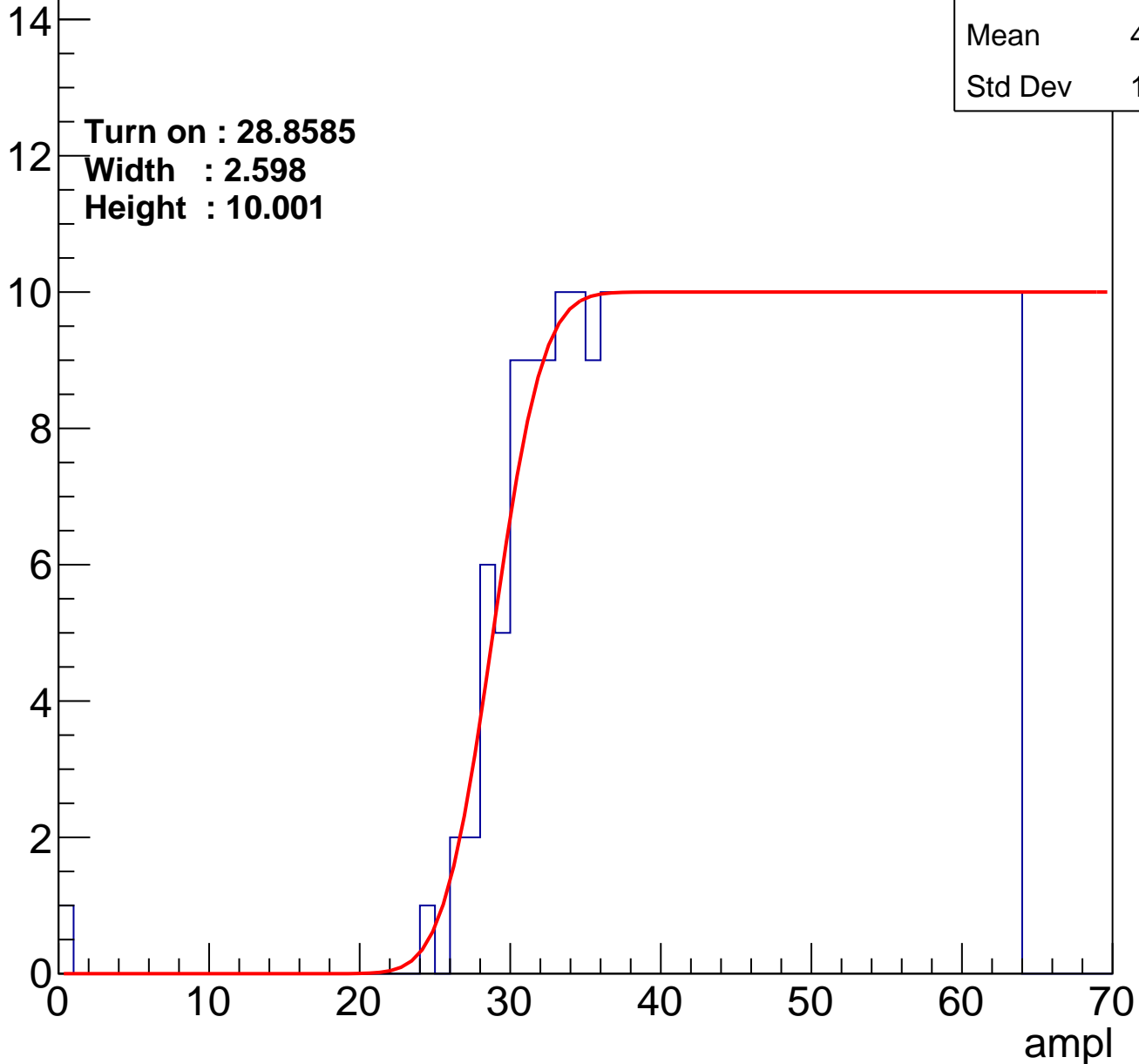
Entries	353
Mean	45.68
Std Dev	10.58

Turn on : 28.8585

Width : 2.598

Height : 10.001

Entry



B0L001S, U1-ch1

calib_packv5_042523_0143.root, FC#9, port A1

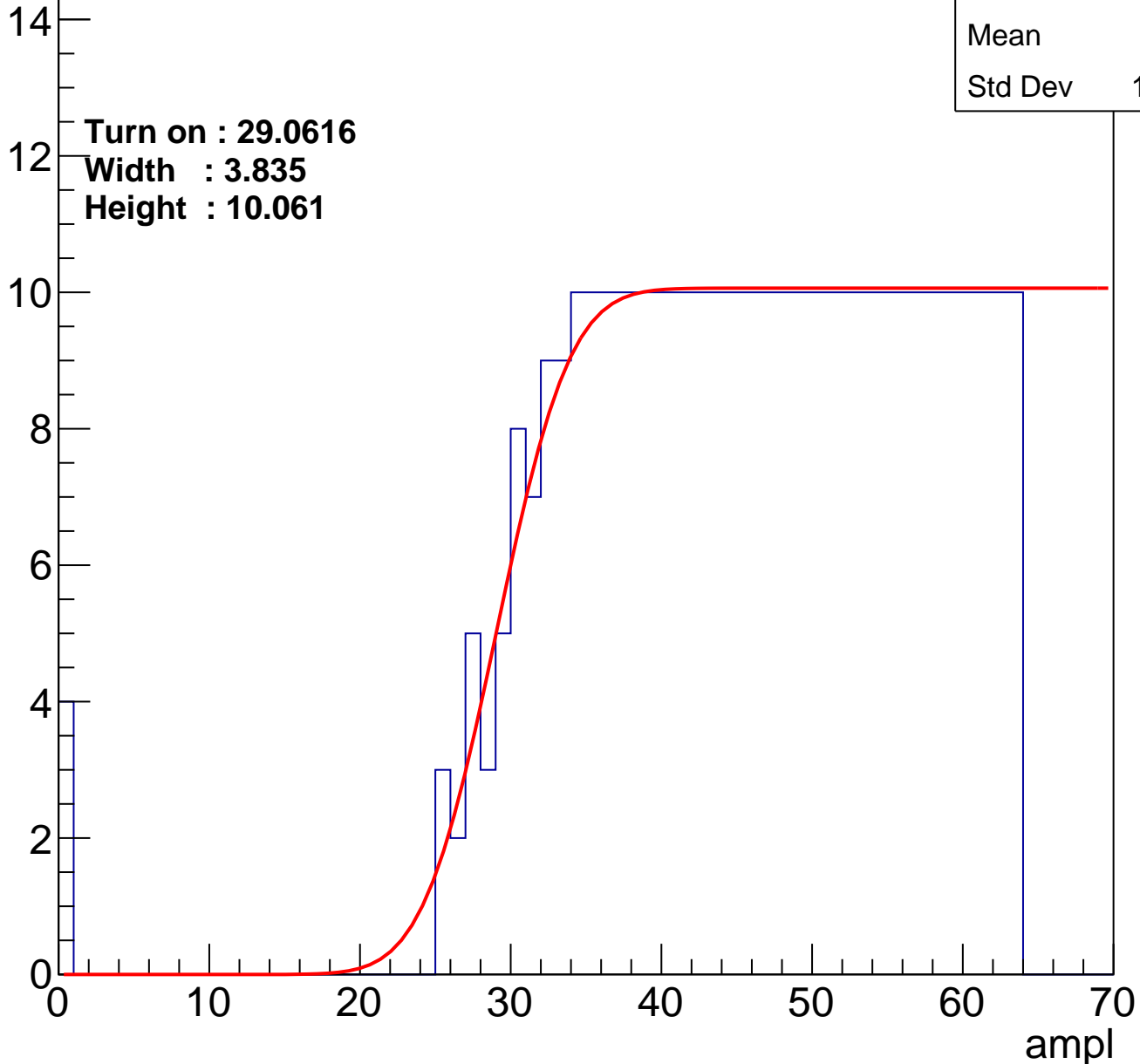
Entries	355
Mean	45.3
Std Dev	11.37

Turn on : 29.0616

Width : 3.835

Height : 10.061

Entry



B0L001S, U1-ch2

calib_packv5_042523_0143.root, FC#9, port A1

Entries	372
Mean	44.52
Std Dev	11.62

Turn on : 27.9895

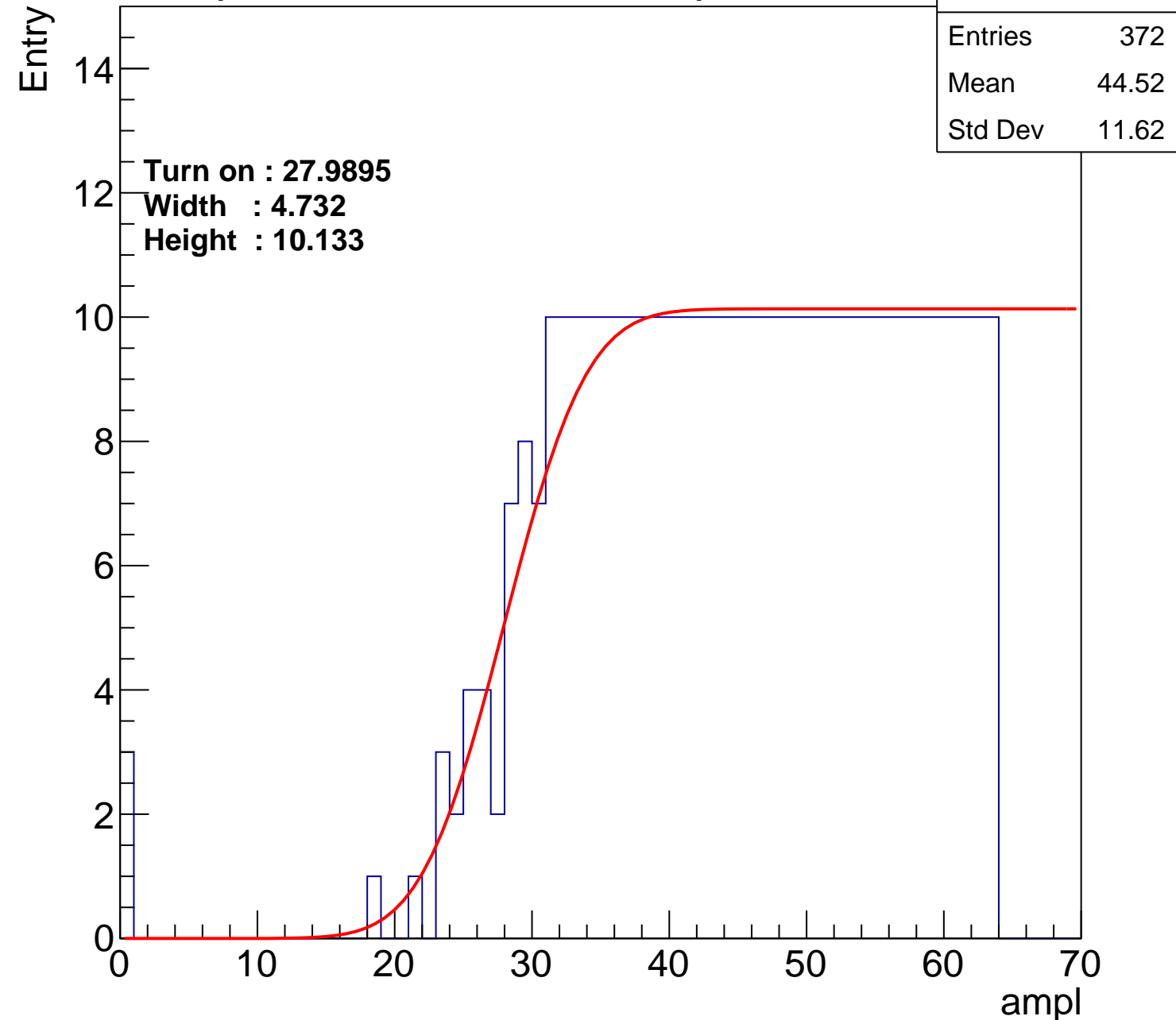
Width : 4.732

Height : 10.133

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch3

calib_packv5_042523_0143.root, FC#9, port A1

Entries	379
Mean	44.34
Std Dev	11.43

Turn on : 25.8657

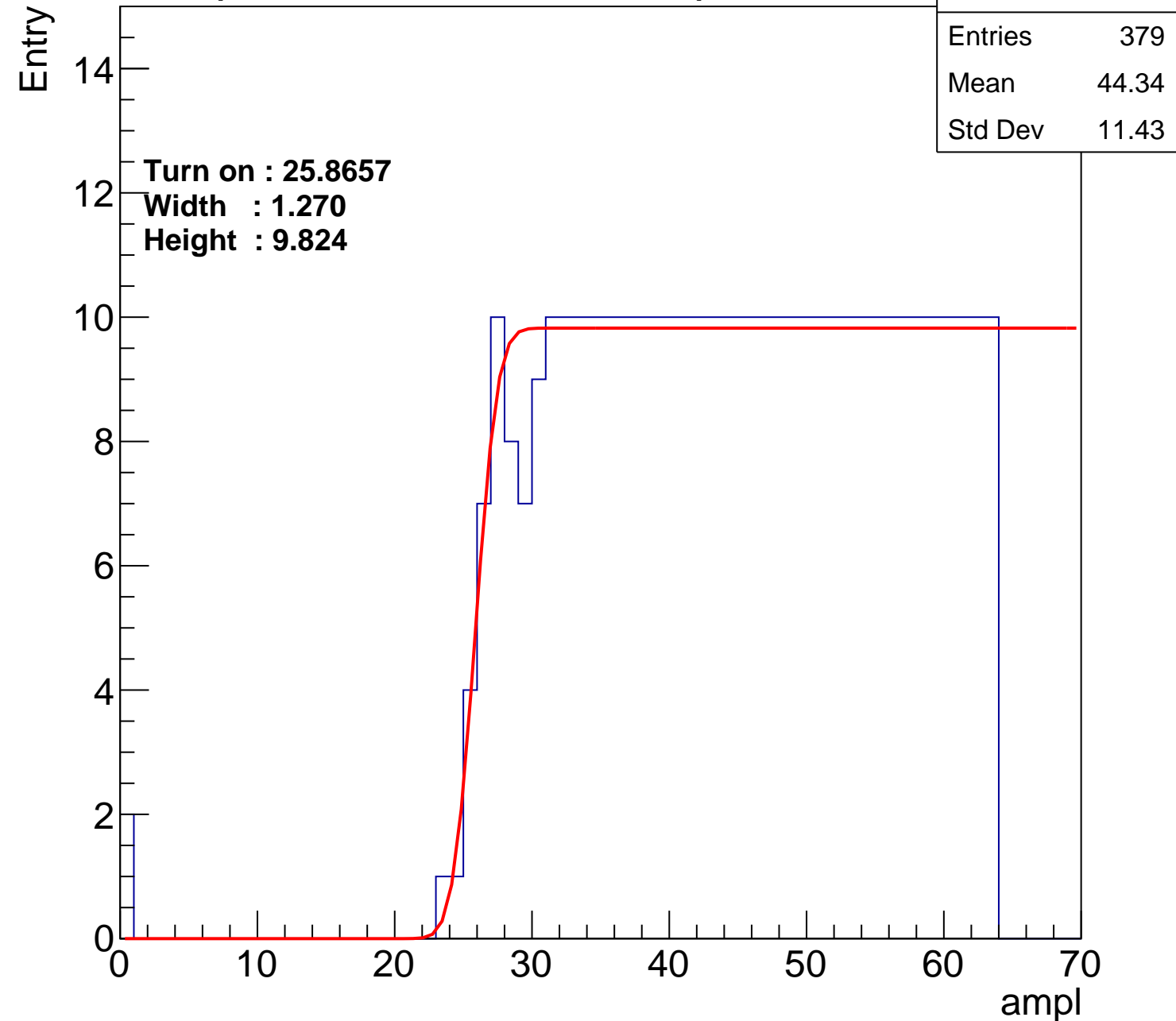
Width : 1.270

Height : 9.824

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch4

calib_packv5_042523_0143.root, FC#9, port A1

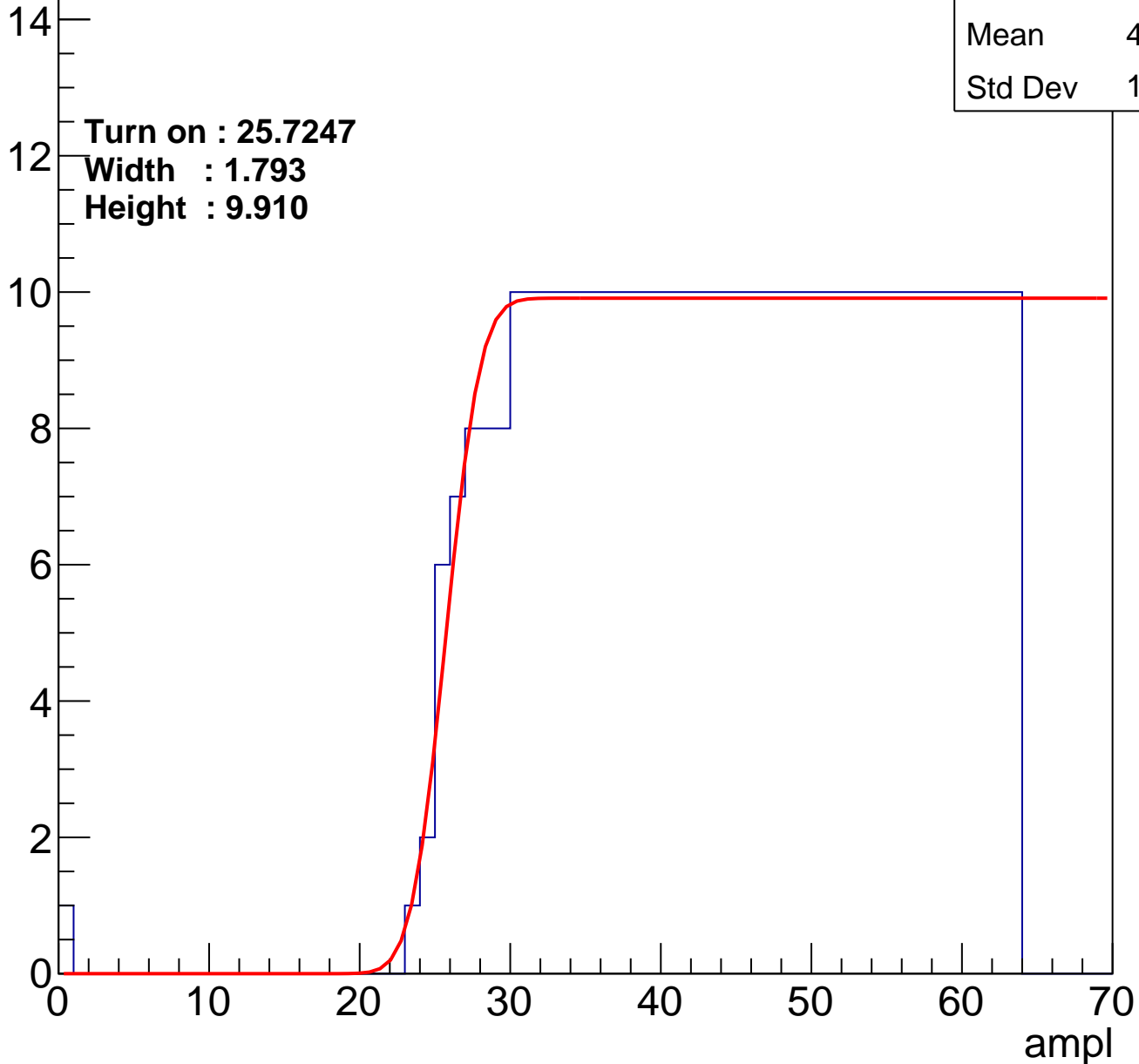
Entries	381
Mean	44.32
Std Dev	11.29

Turn on : 25.7247

Width : 1.793

Height : 9.910

Entry



B0L001S, U1-ch5

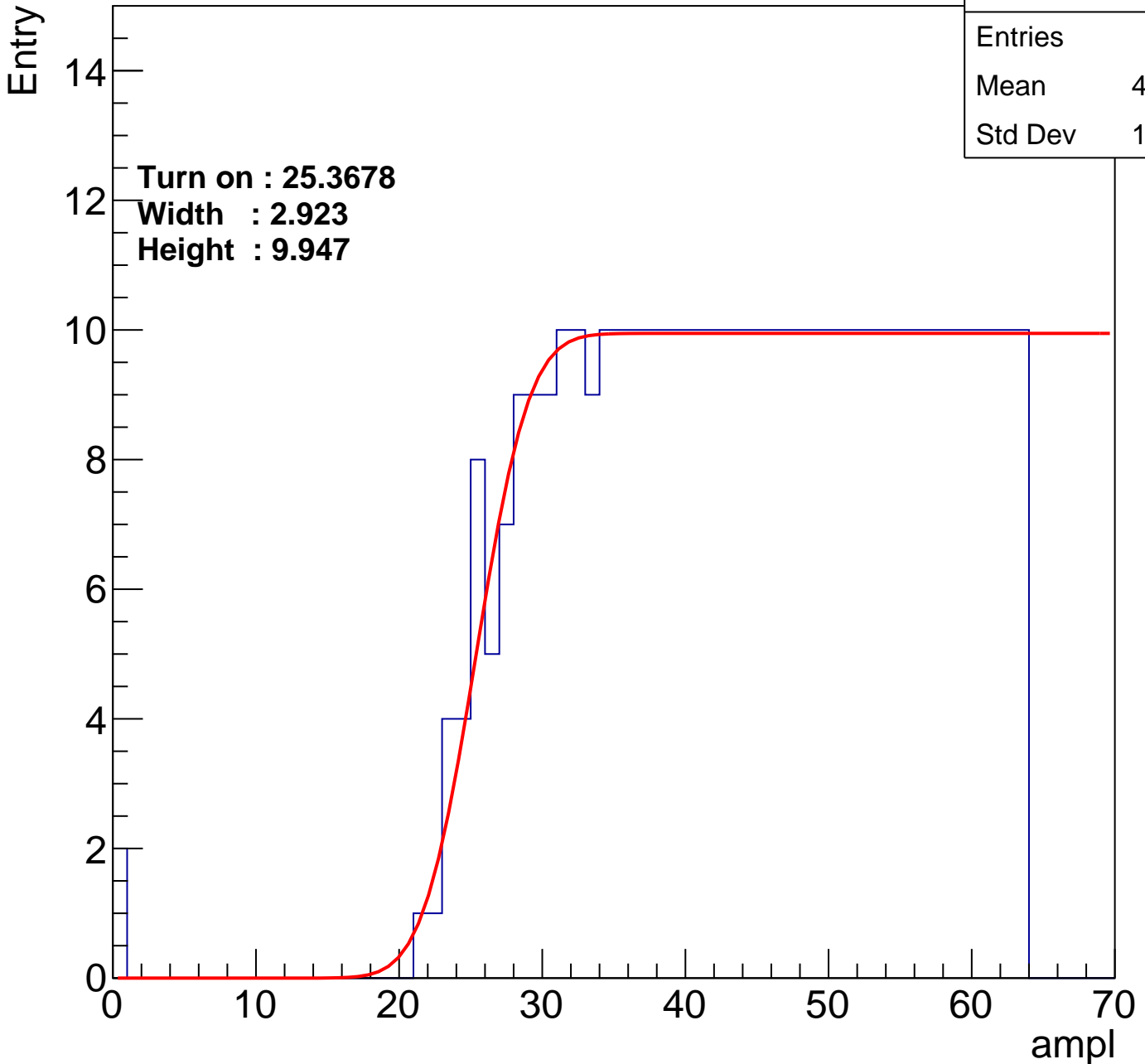
calib_packv5_042523_0143.root, FC#9, port A1

Entries	388
Mean	43.84
Std Dev	11.76

Turn on : 25.3678

Width : 2.923

Height : 9.947



B0L001S, U1-ch6

calib_packv5_042523_0143.root, FC#9, port A1

Entries	372
Mean	44.49
Std Dev	11.72

Turn on : 27.2726

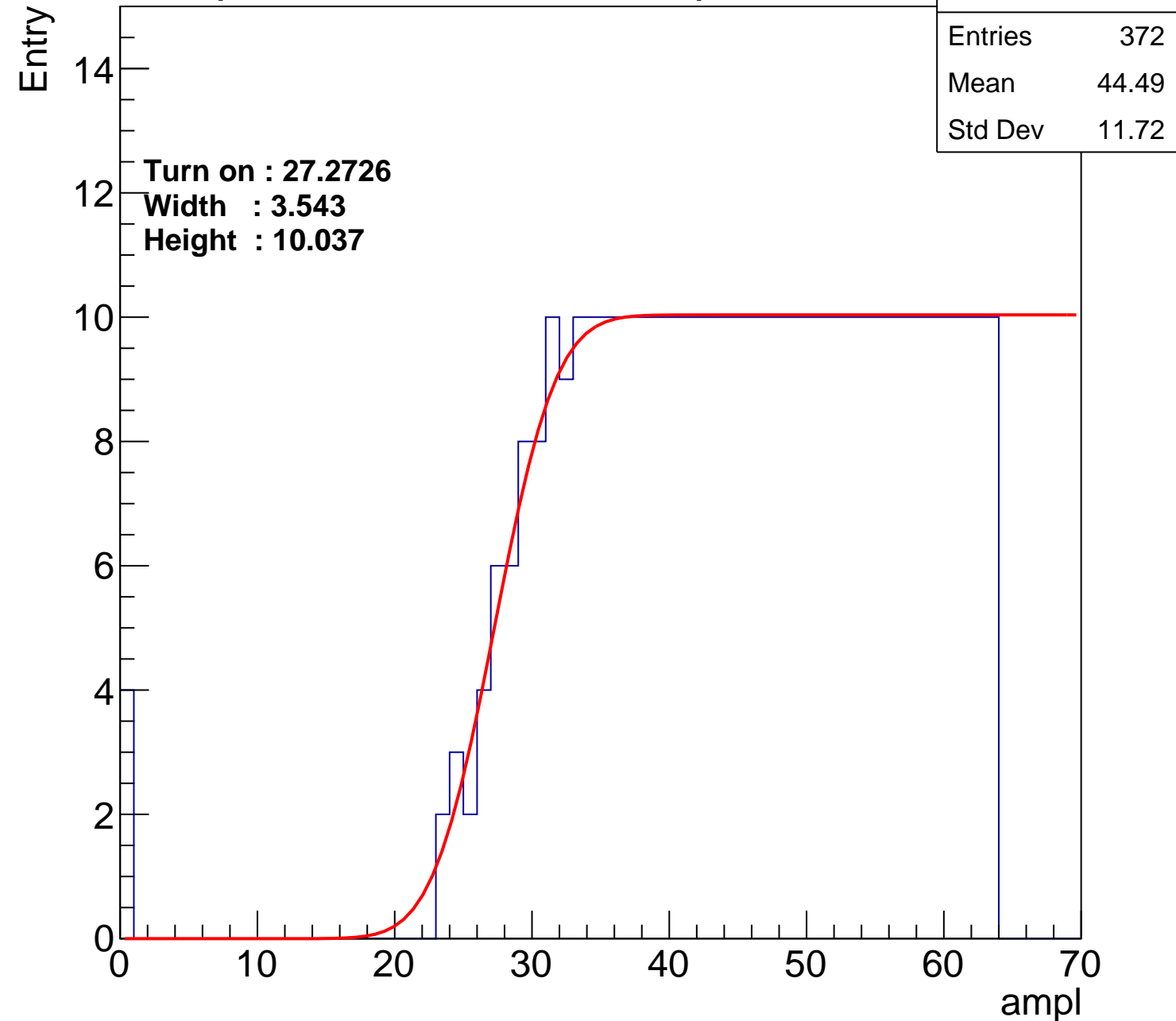
Width : 3.543

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch7

calib_packv5_042523_0143.root, FC#9, port A1

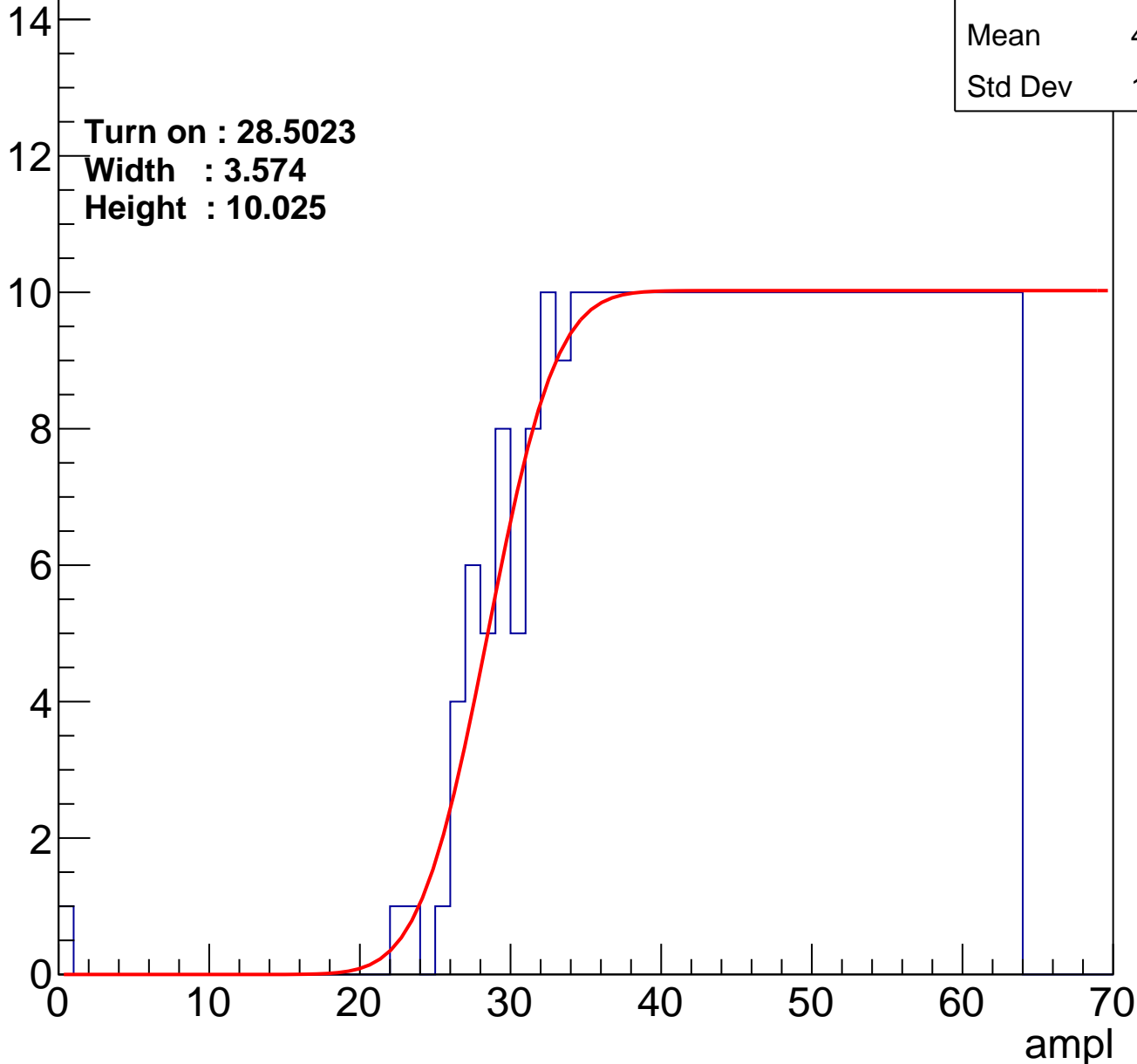
Entries	359
Mean	45.33
Std Dev	10.83

Turn on : 28.5023

Width : 3.574

Height : 10.025

Entry



B0L001S, U1-ch8

calib_packv5_042523_0143.root, FC#9, port A1

Entries	387
Mean	43.74
Std Dev	12.17

Turn on : 25.8419

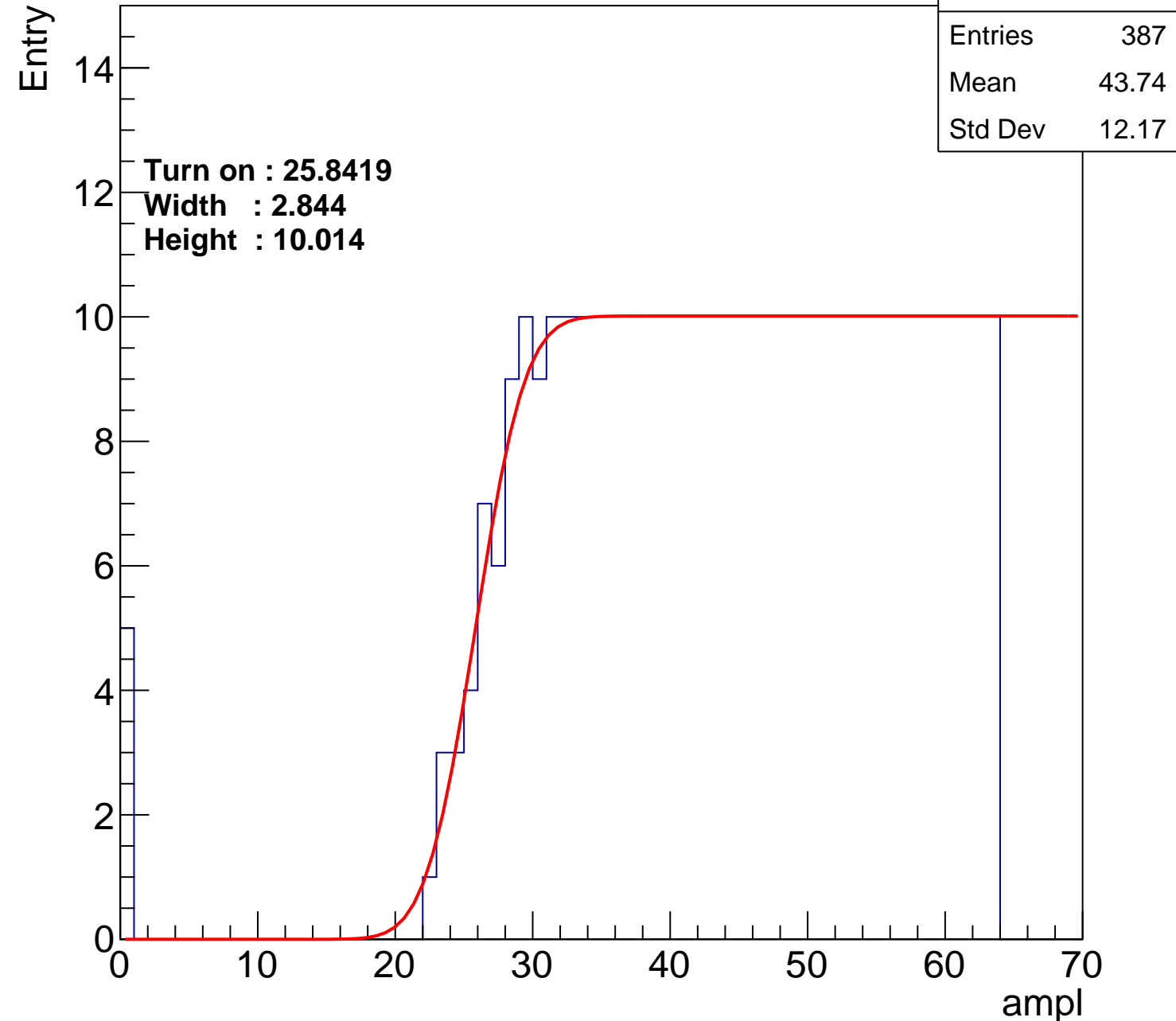
Width : 2.844

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch9

calib_packv5_042523_0143.root, FC#9, port A1

Entries	363
Mean	45.07
Std Dev	11.22

Turn on : 28.2204

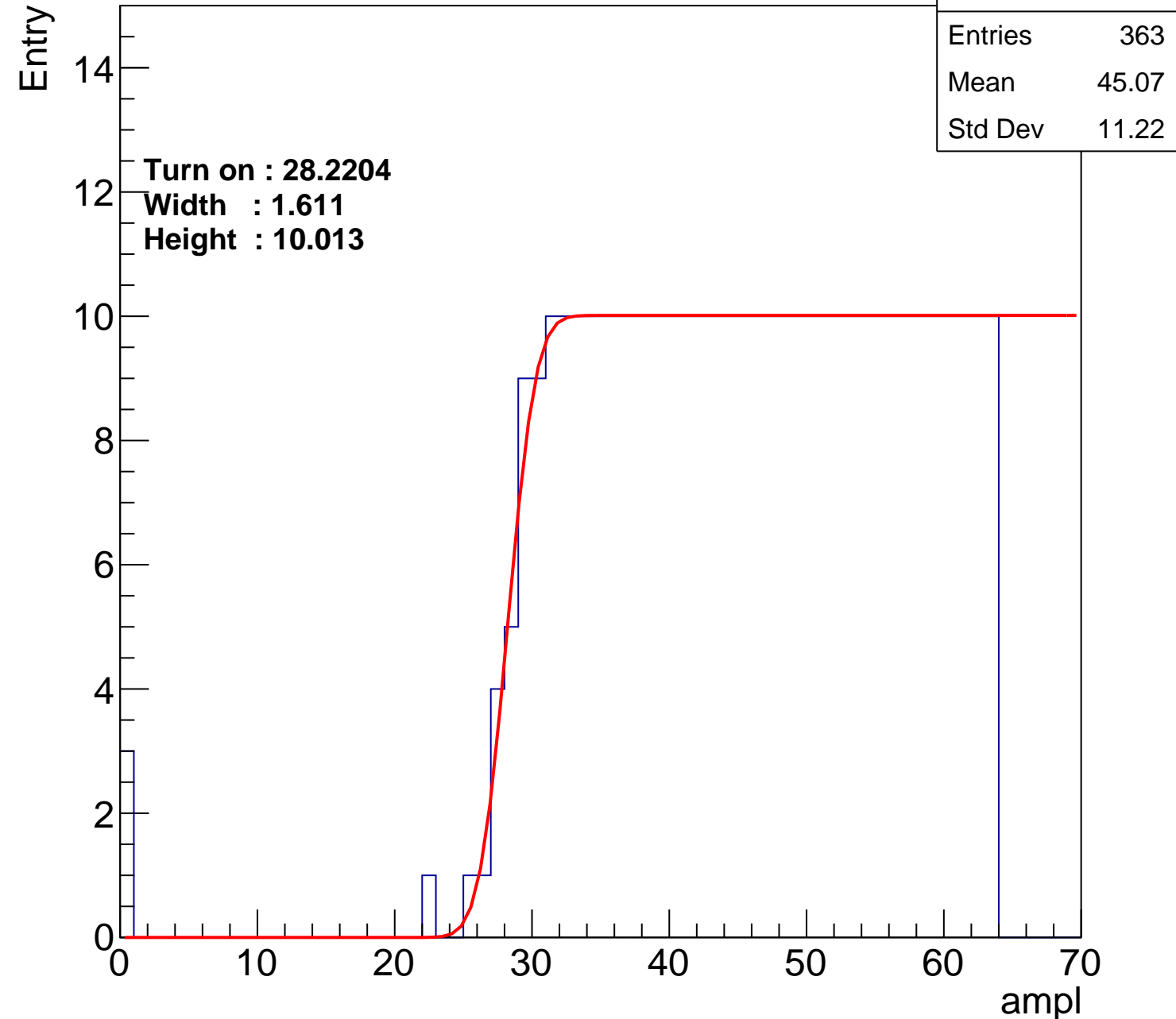
Width : 1.611

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch10

calib_packv5_042523_0143.root, FC#9, port A1

Entries	371
Mean	44.61
Std Dev	11.51

Turn on : 27.6445

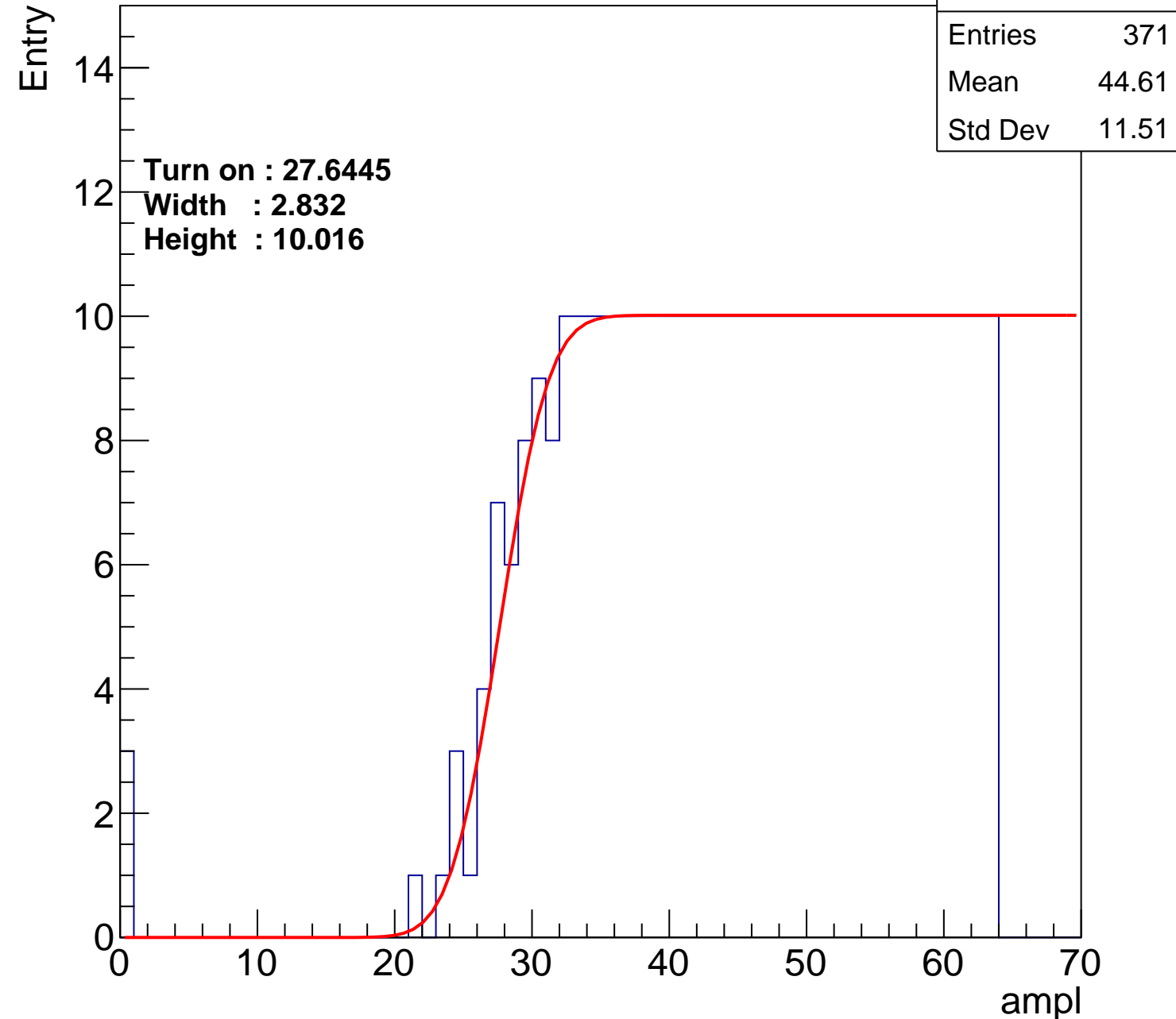
Width : 2.832

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch11

calib_packv5_042523_0143.root, FC#9, port A1

Entries	372
Mean	44.75
Std Dev	11.07

Turn on : 26.9438

Width : 1.685

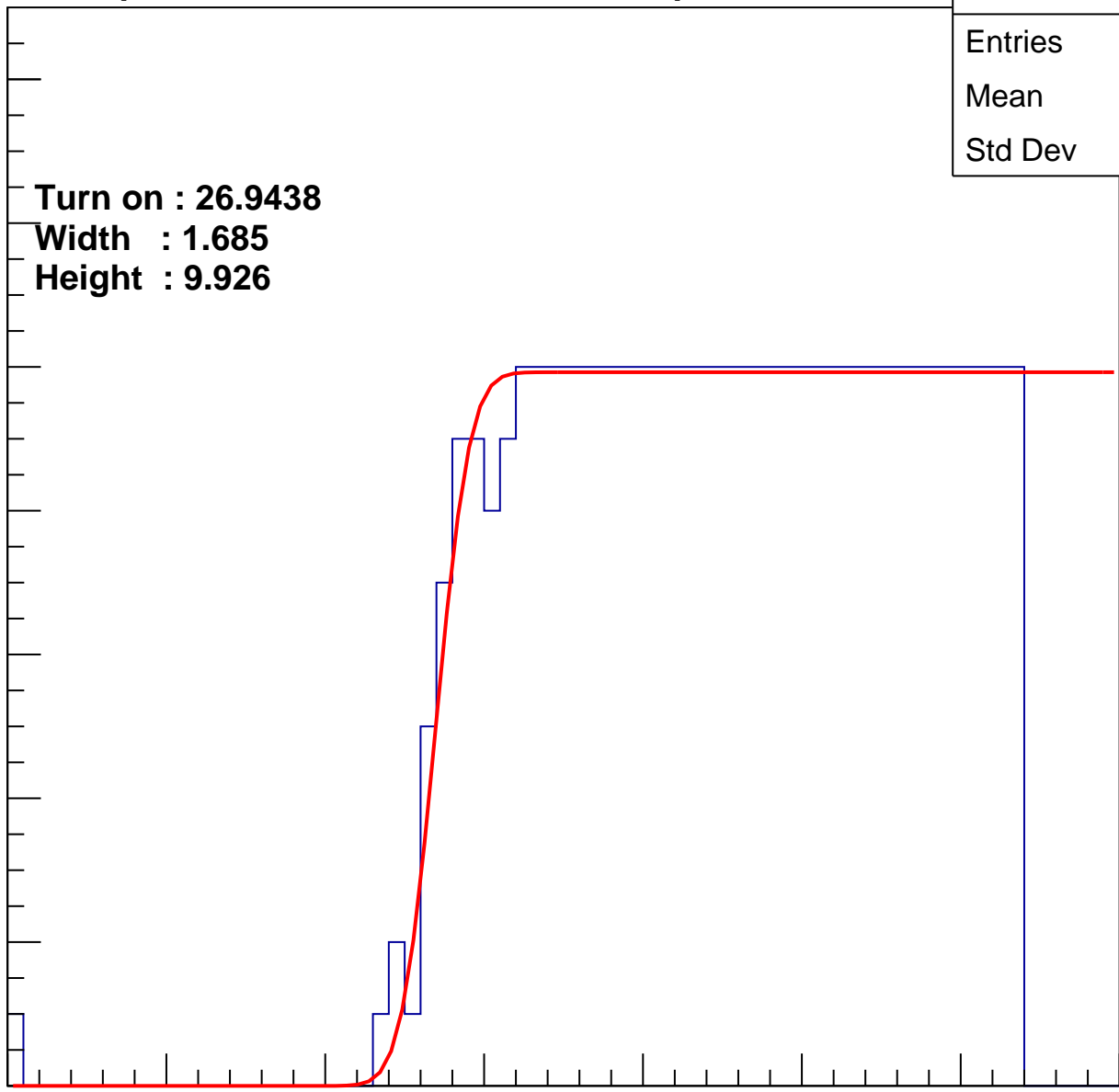
Height : 9.926

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B0L001S, U1-ch12

calib_packv5_042523_0143.root, FC#9, port A1

Entries	379
Mean	44.21
Std Dev	11.73

Turn on : 27.2682

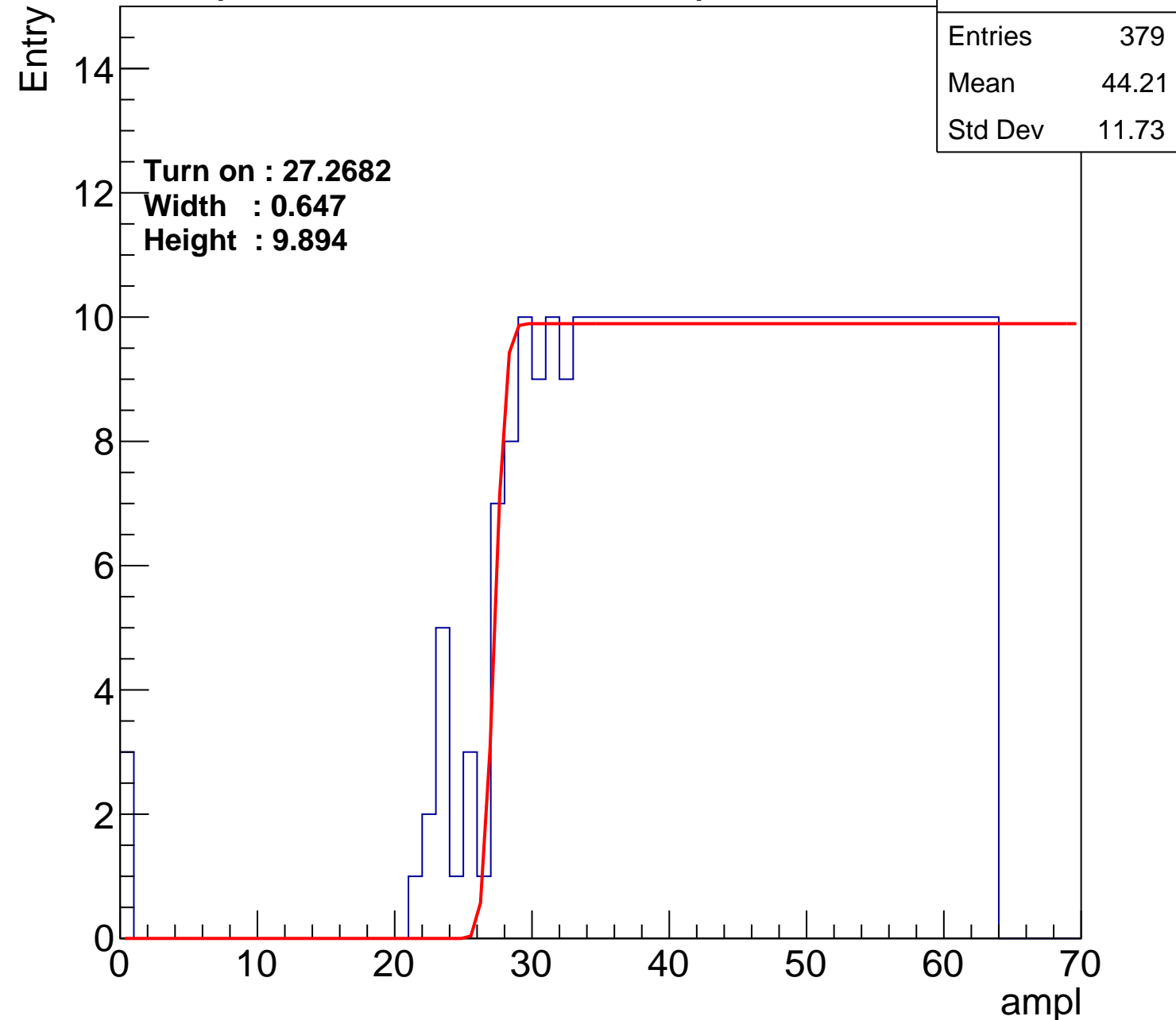
Width : 0.647

Height : 9.894

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch13

calib_packv5_042523_0143.root, FC#9, port A1

Entries	378
Mean	44.21
Std Dev	11.85

Turn on : 26.4506

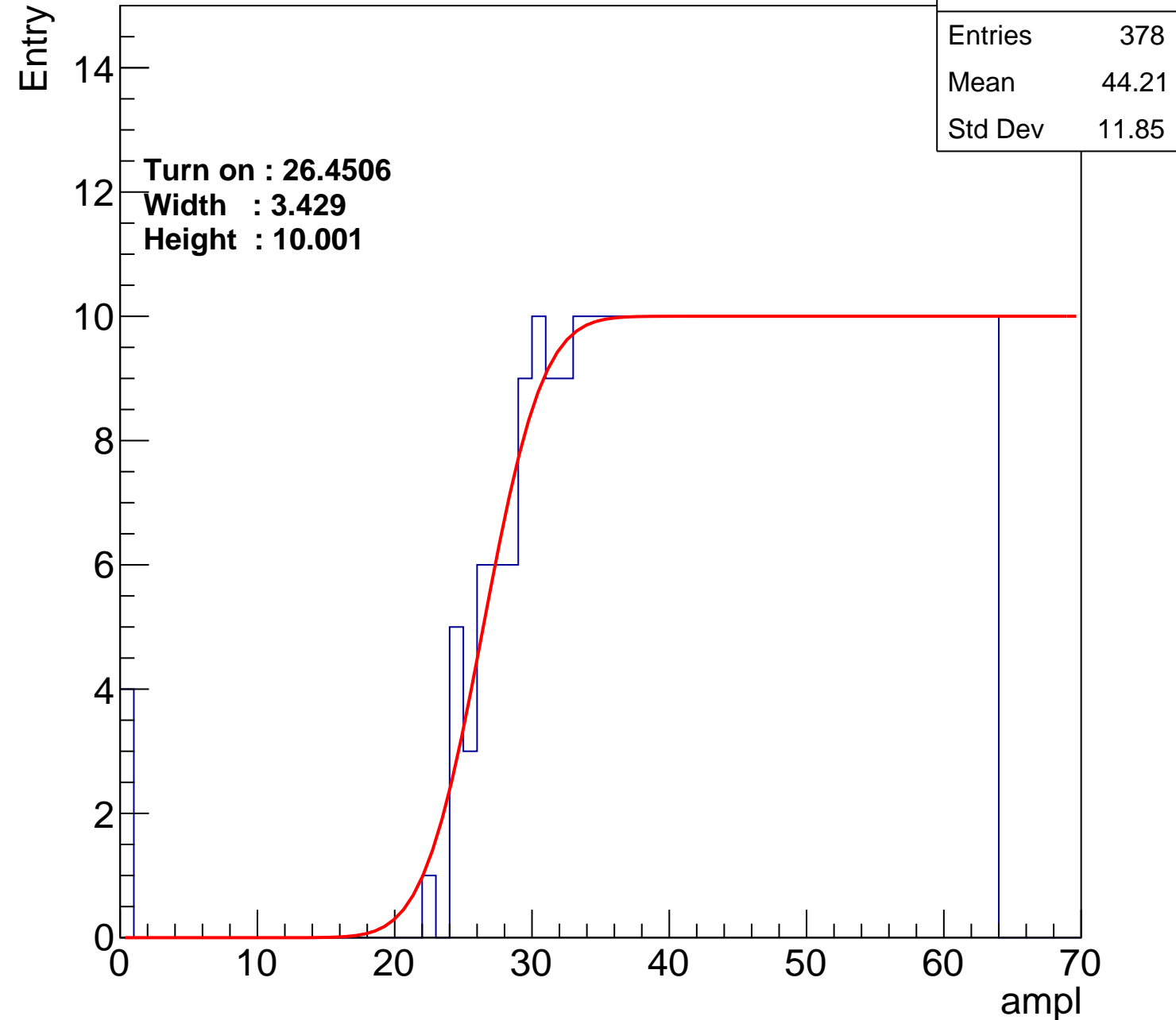
Width : 3.429

Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch14

calib_packv5_042523_0143.root, FC#9, port A1

Entries	382
Mean	44.18
Std Dev	11.54

Turn on : 25.8758

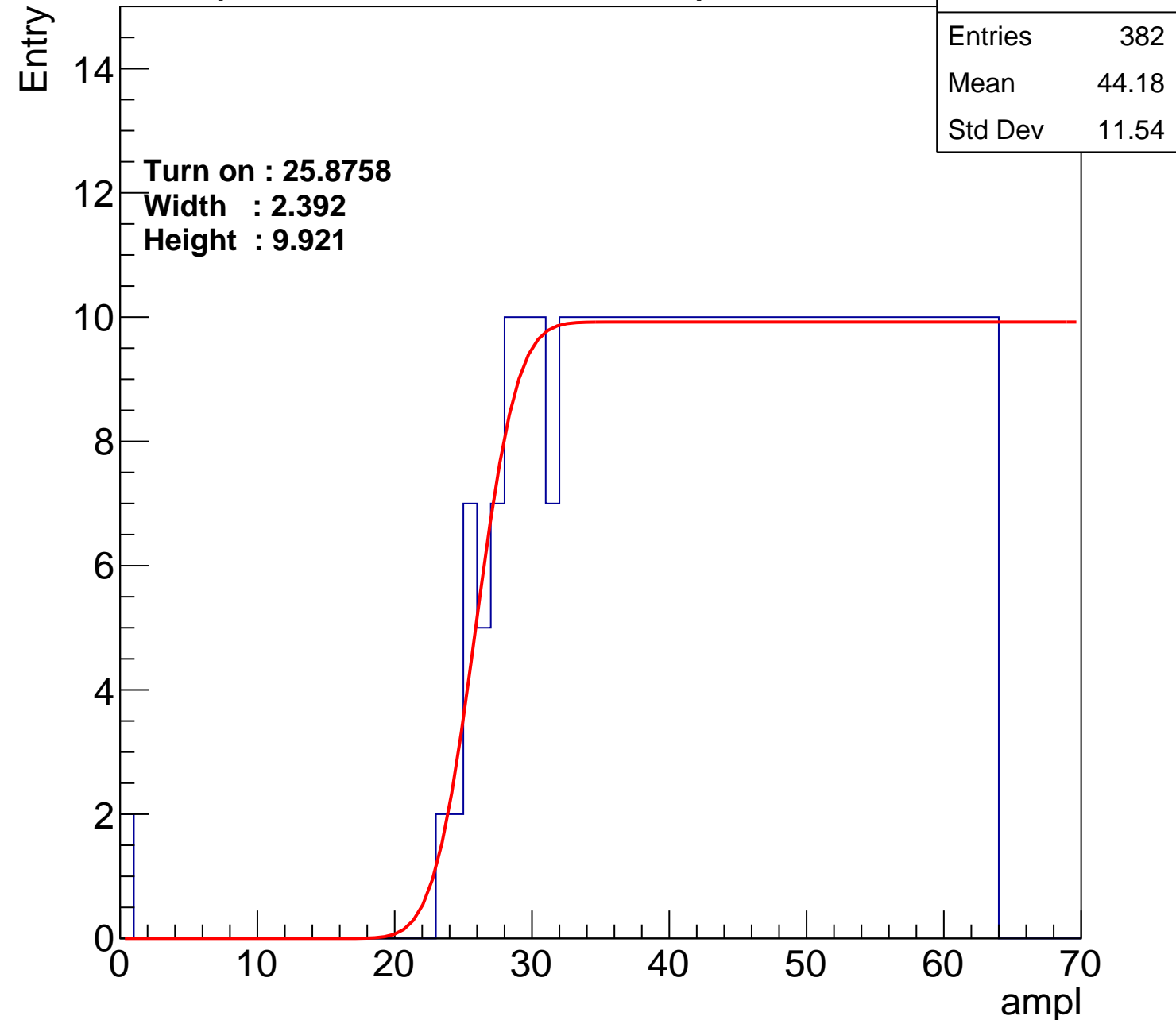
Width : 2.392

Height : 9.921

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch15

calib_packv5_042523_0143.root, FC#9, port A1

Entries	368
Mean	44.79
Std Dev	11.39

Turn on : 27.5777

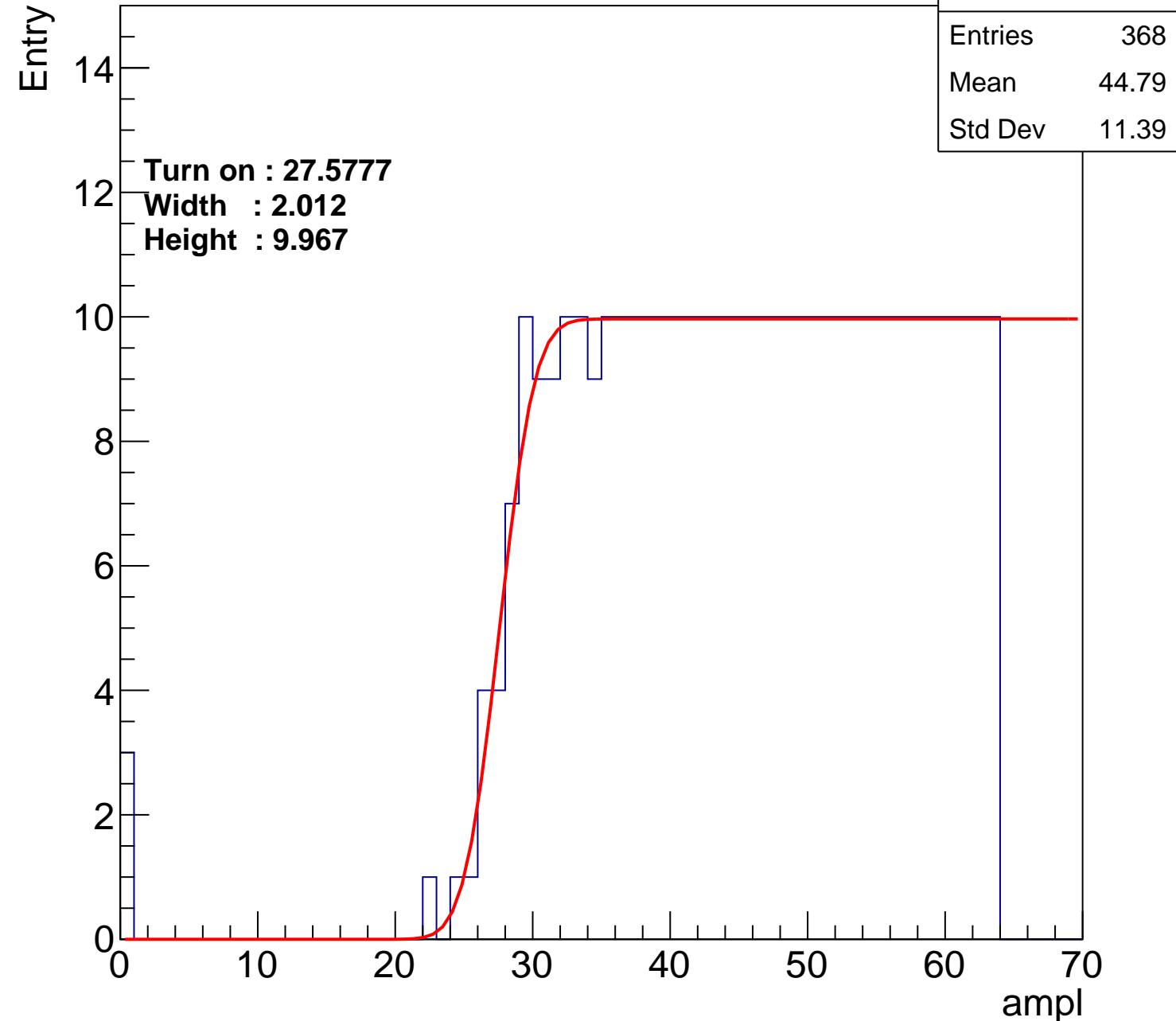
Width : 2.012

Height : 9.967

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch16

calib_packv5_042523_0143.root, FC#9, port A1

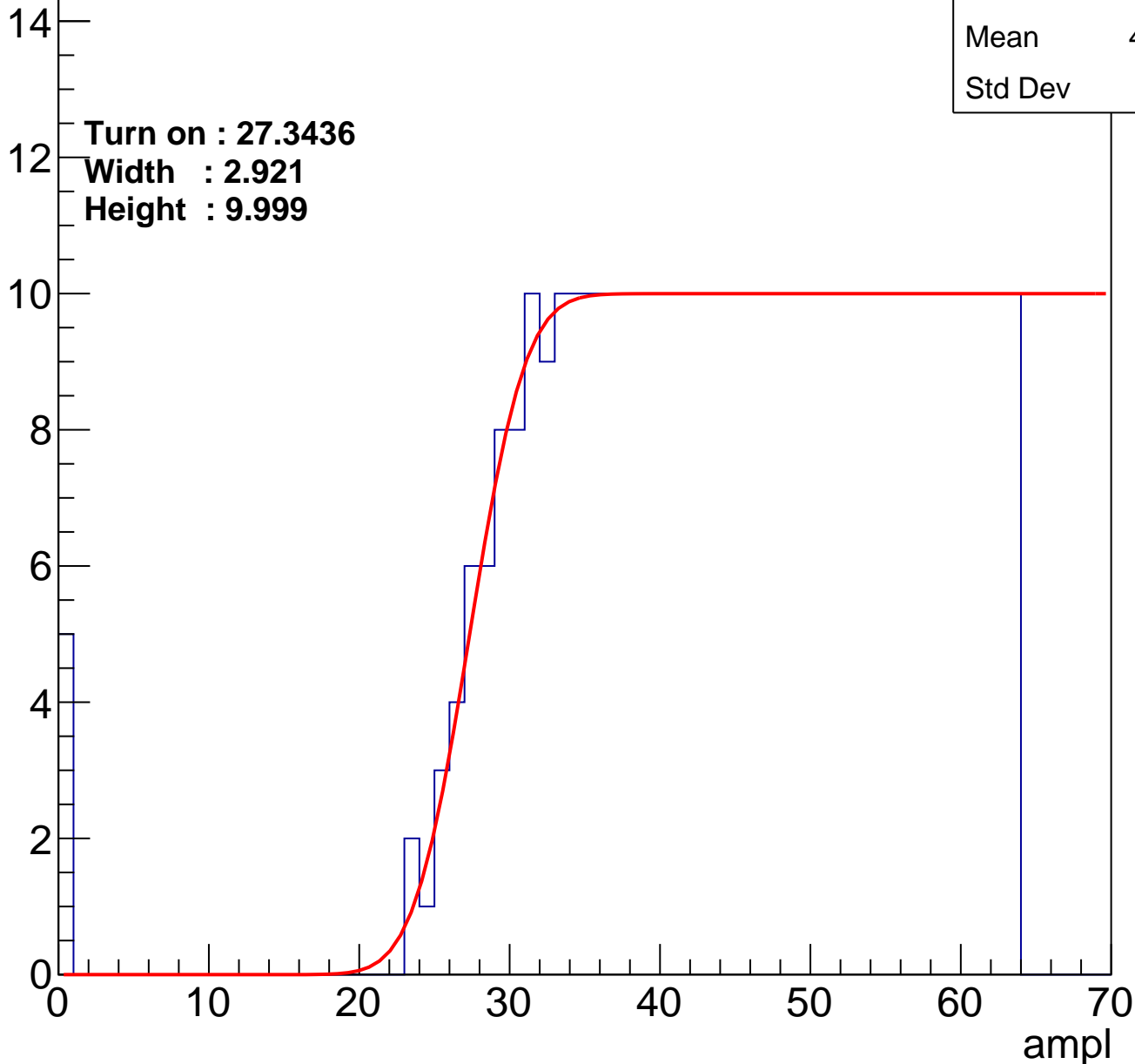
Entry

Entries	372
Mean	44.43
Std Dev	11.9

Turn on : 27.3436

Width : 2.921

Height : 9.999



B0L001S, U1-ch17

calib_packv5_042523_0143.root, FC#9, port A1

Entries	372
Mean	44.28
Std Dev	12.27

Turn on : 27.4108

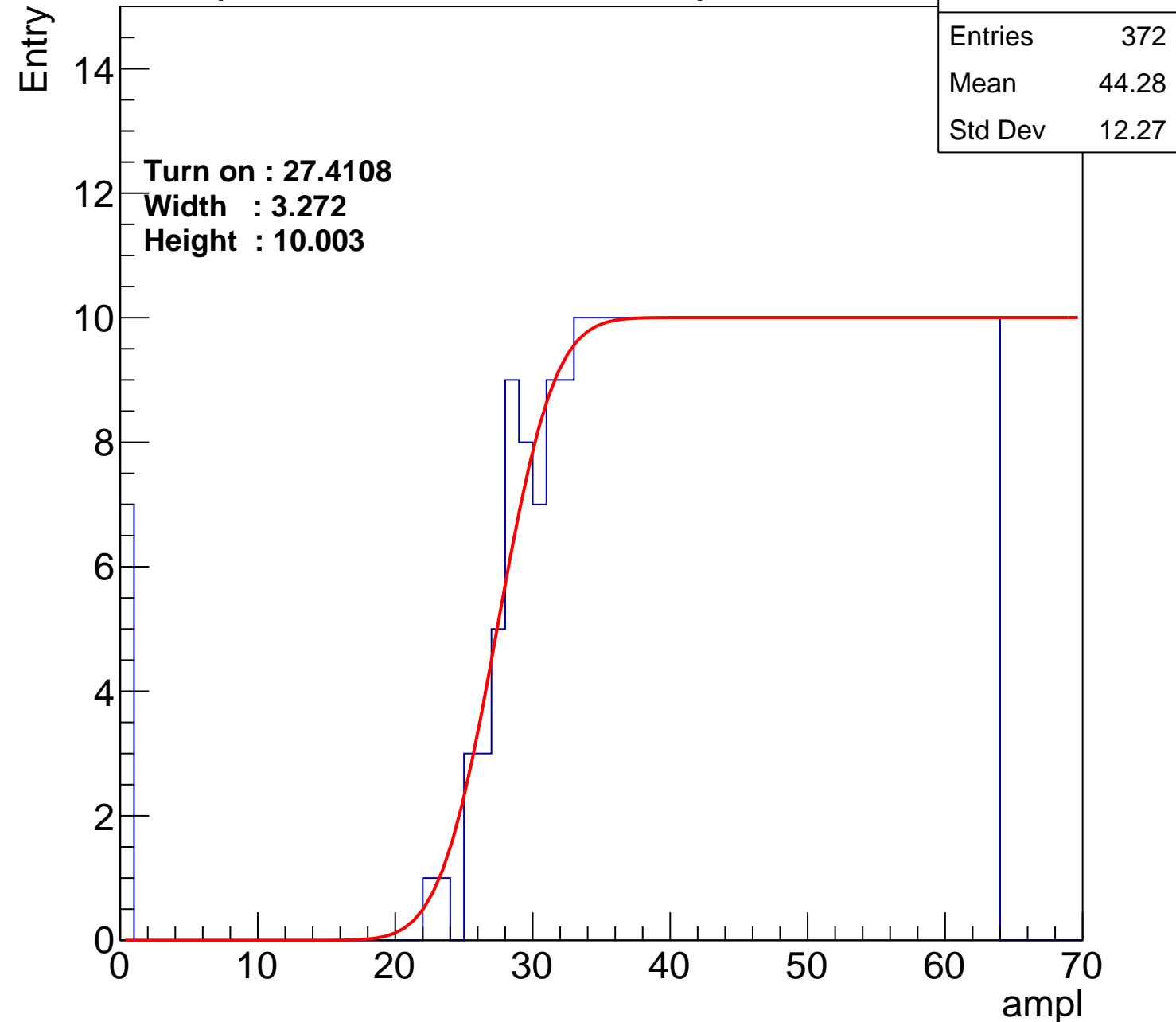
Width : 3.272

Height : 10.003

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch18

calib_packv5_042523_0143.root, FC#9, port A1

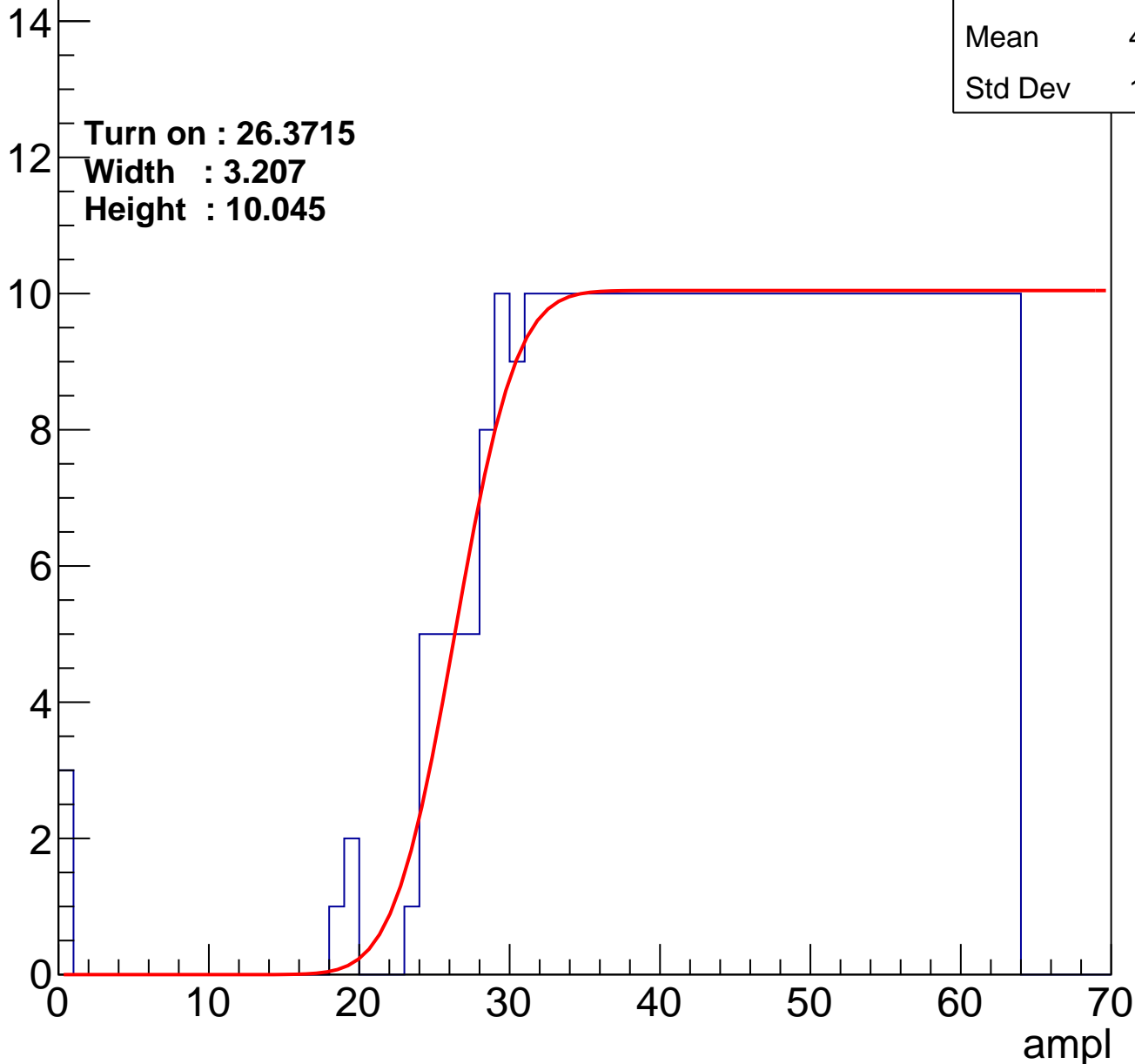
Entry

Entries	384
Mean	43.97
Std Dev	11.86

Turn on : 26.3715

Width : 3.207

Height : 10.045



B0L001S, U1-ch19

calib_packv5_042523_0143.root, FC#9, port A1

Entries	363
Mean	44.91
Std Dev	11.55

Turn on : 28.3107

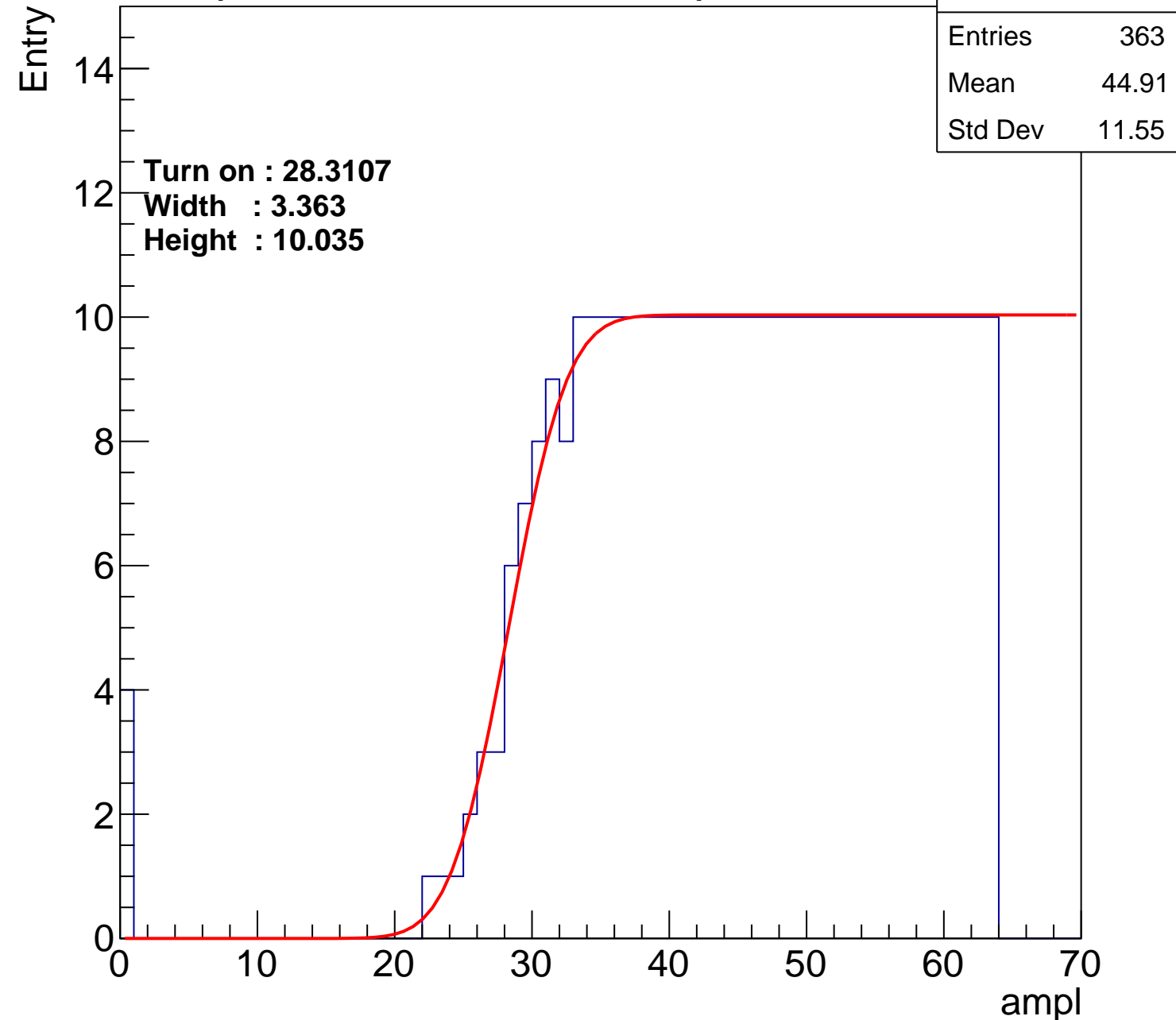
Width : 3.363

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch20

calib_packv5_042523_0143.root, FC#9, port A1

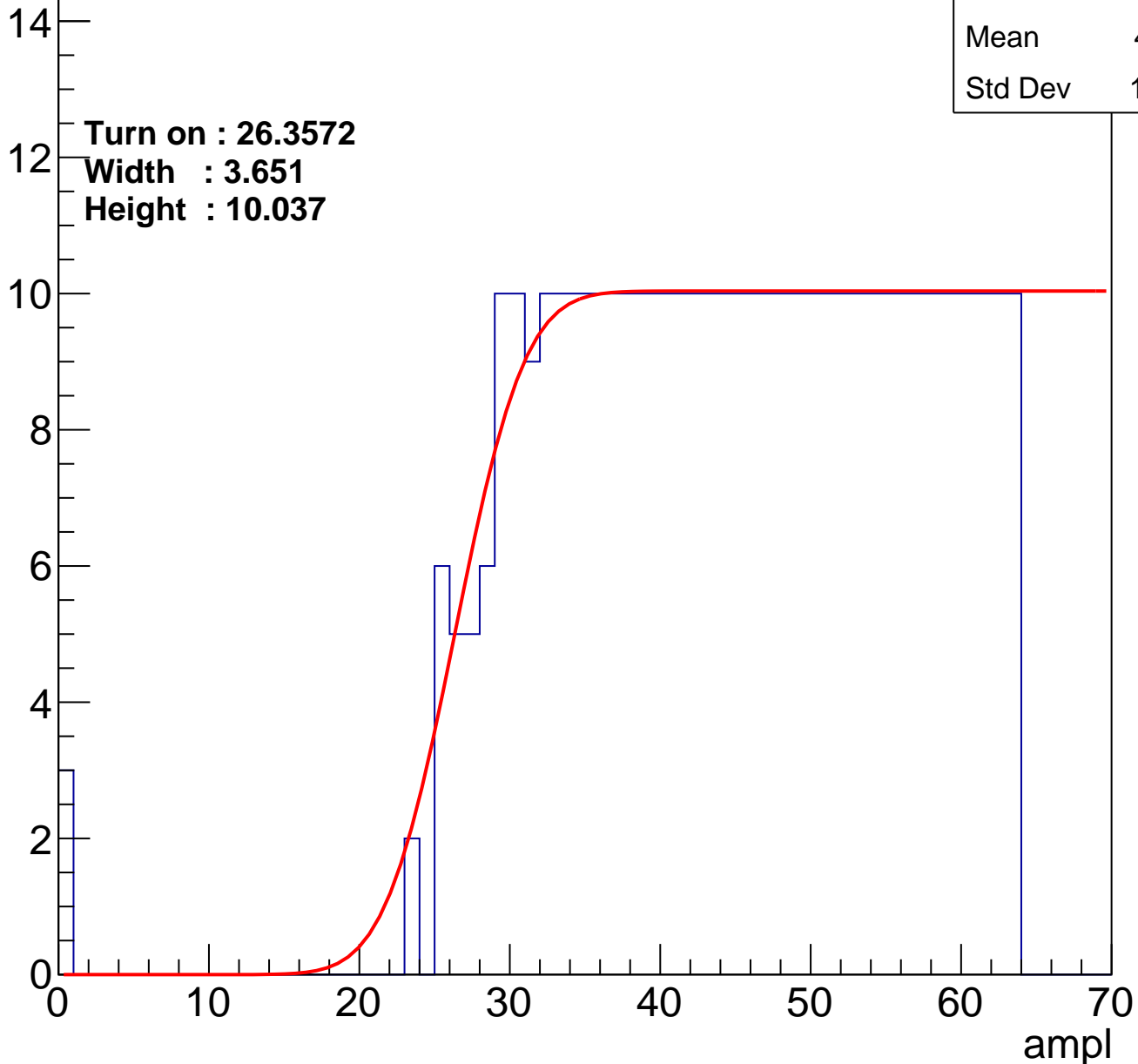
Entries	376
Mean	44.41
Std Dev	11.57

Turn on : 26.3572

Width : 3.651

Height : 10.037

Entry



B0L001S, U1-ch21

calib_packv5_042523_0143.root, FC#9, port A1

Entries	372
Mean	44.66
Std Dev	11.3

Turn on : 26.8662

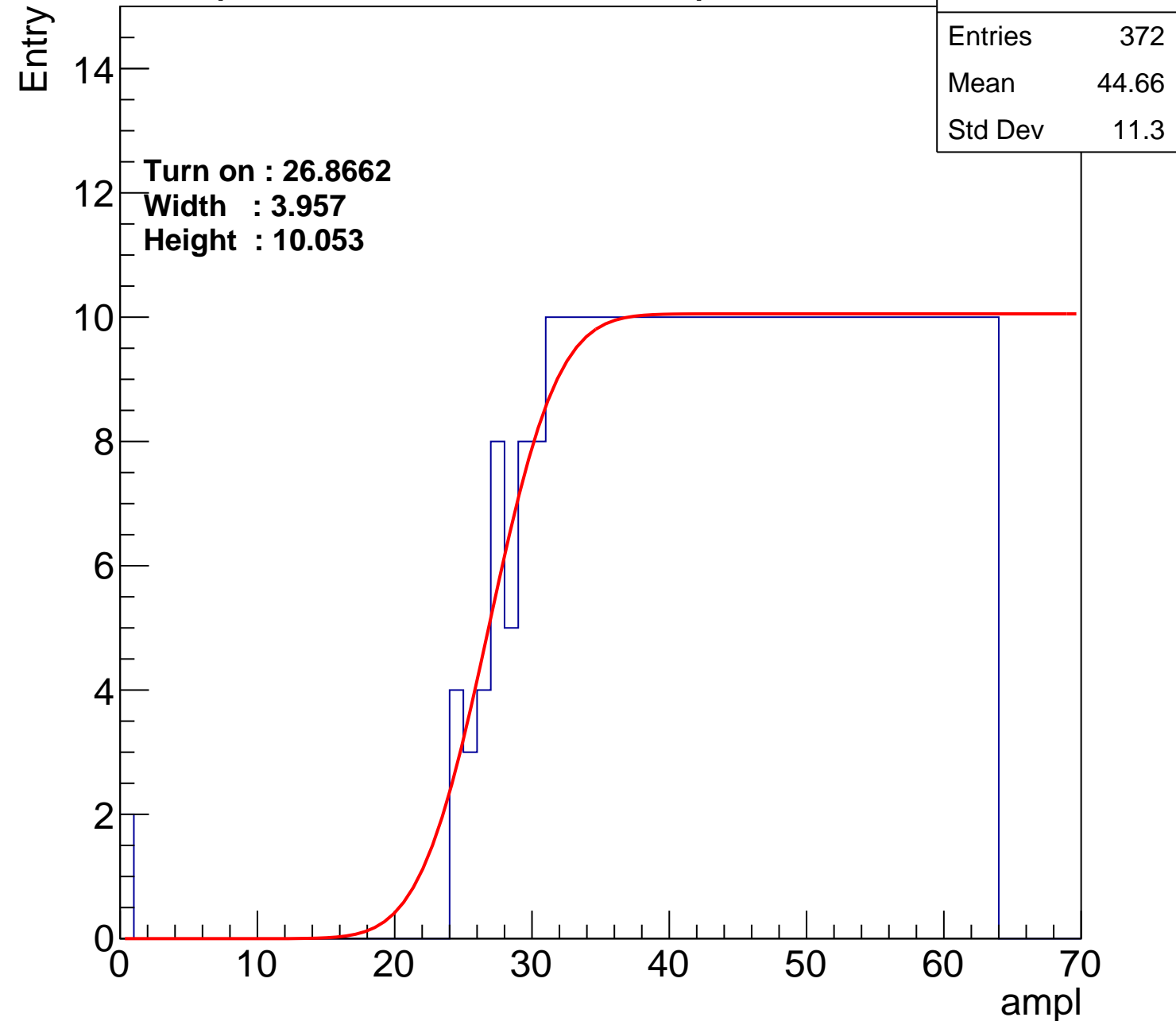
Width : 3.957

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch22

calib_packv5_042523_0143.root, FC#9, port A1

Entries	375
Mean	44.35
Std Dev	11.79

Turn on : 26.9607

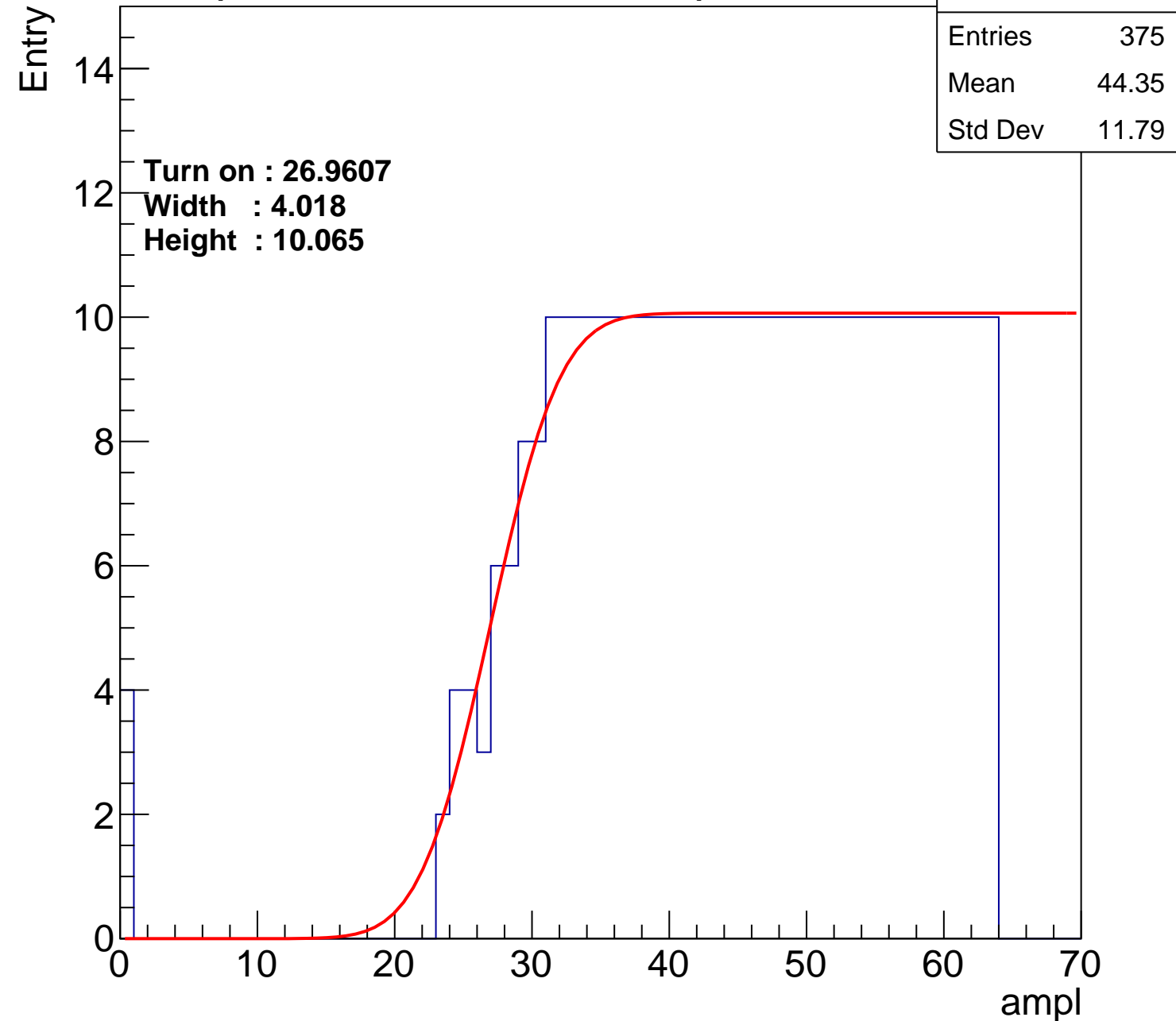
Width : 4.018

Height : 10.065

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch23

calib_packv5_042523_0143.root, FC#9, port A1

Entries	361
Mean	45.01
Std Dev	11.5

Turn on : 28.6674

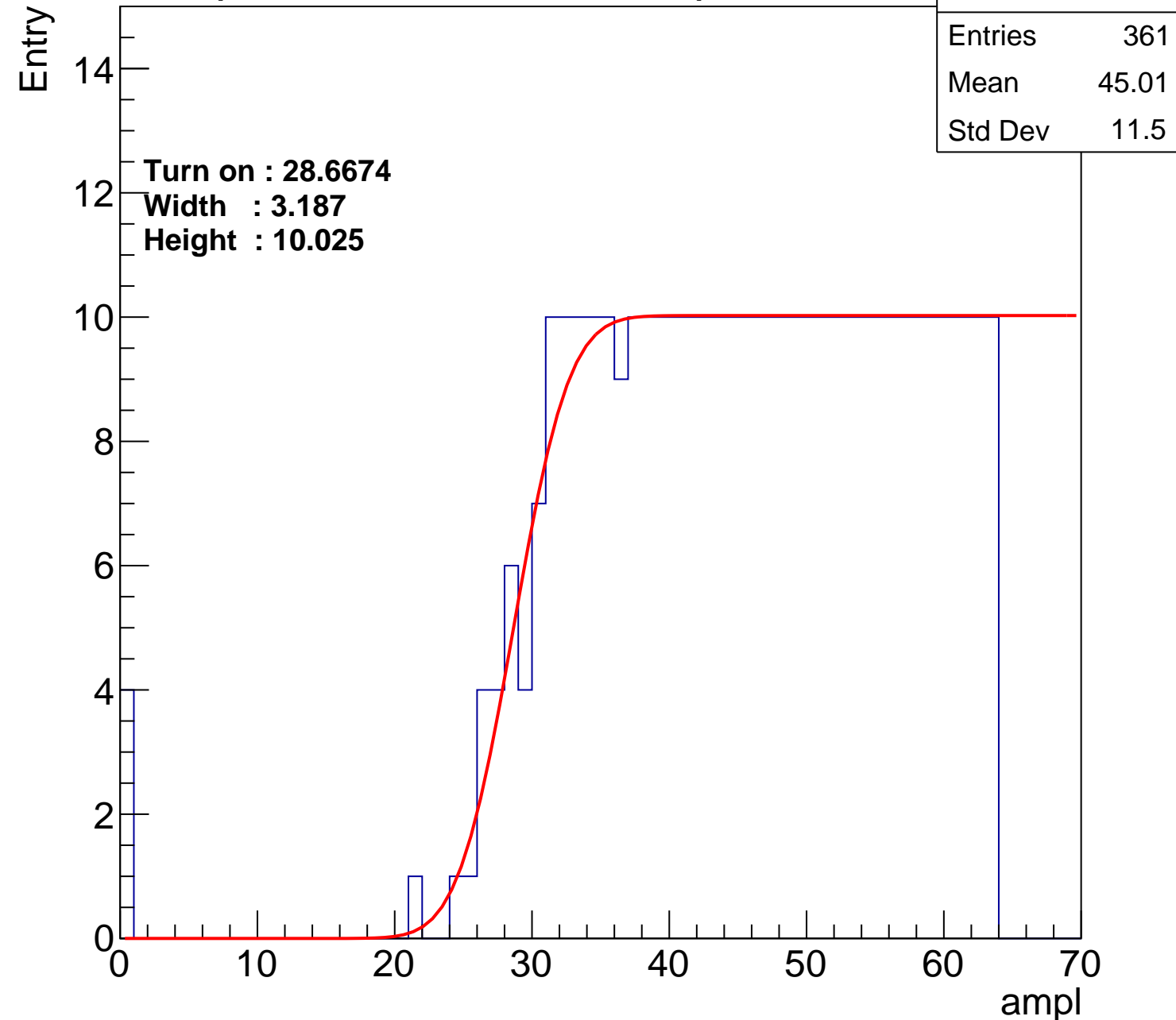
Width : 3.187

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch24

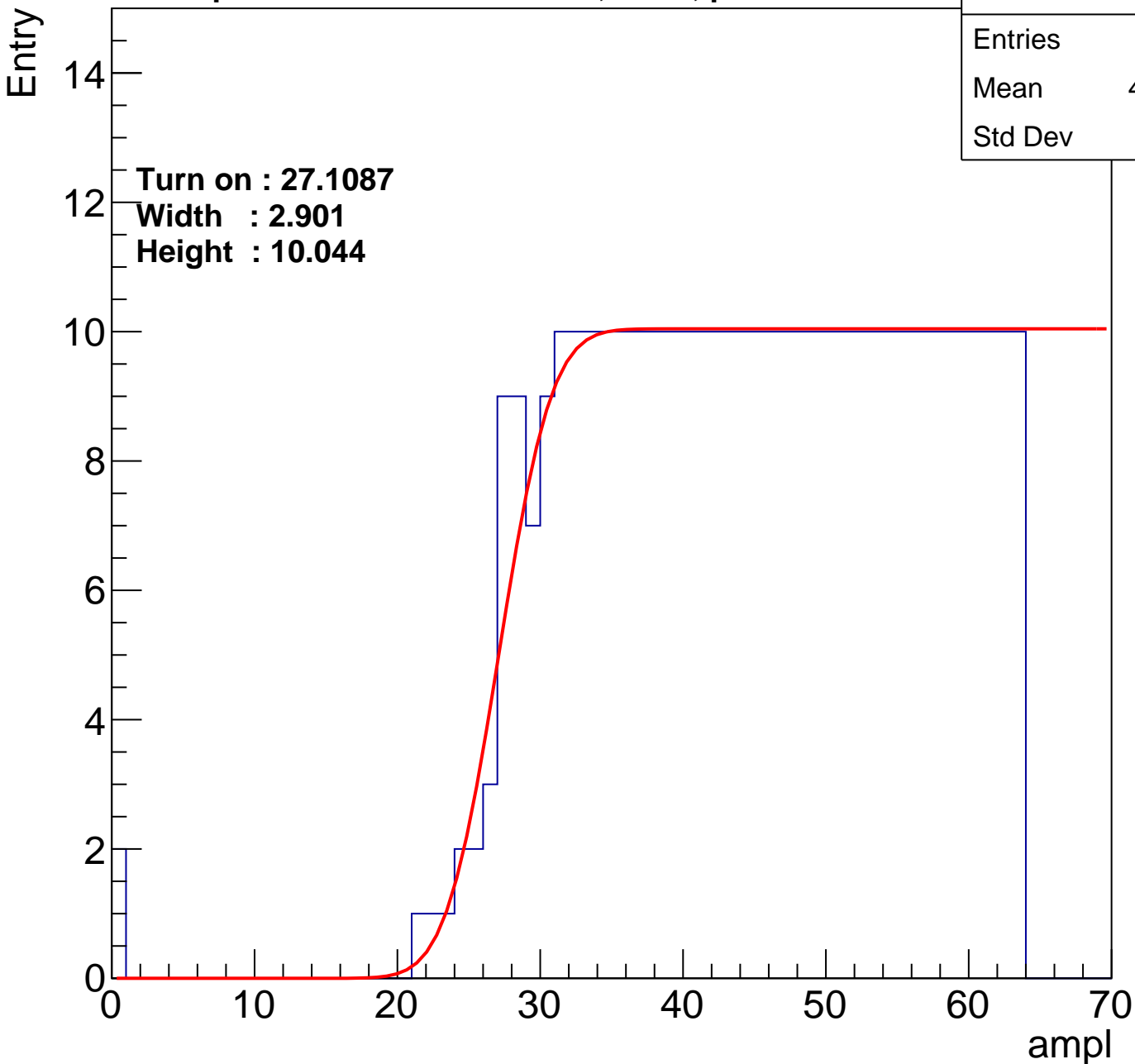
calib_packv5_042523_0143.root, FC#9, port A1

Turn on : 27.1087

Width : 2.901

Height : 10.044

Entries	376
Mean	44.47
Std Dev	11.4



B0L001S, U1-ch25

calib_packv5_042523_0143.root, FC#9, port A1

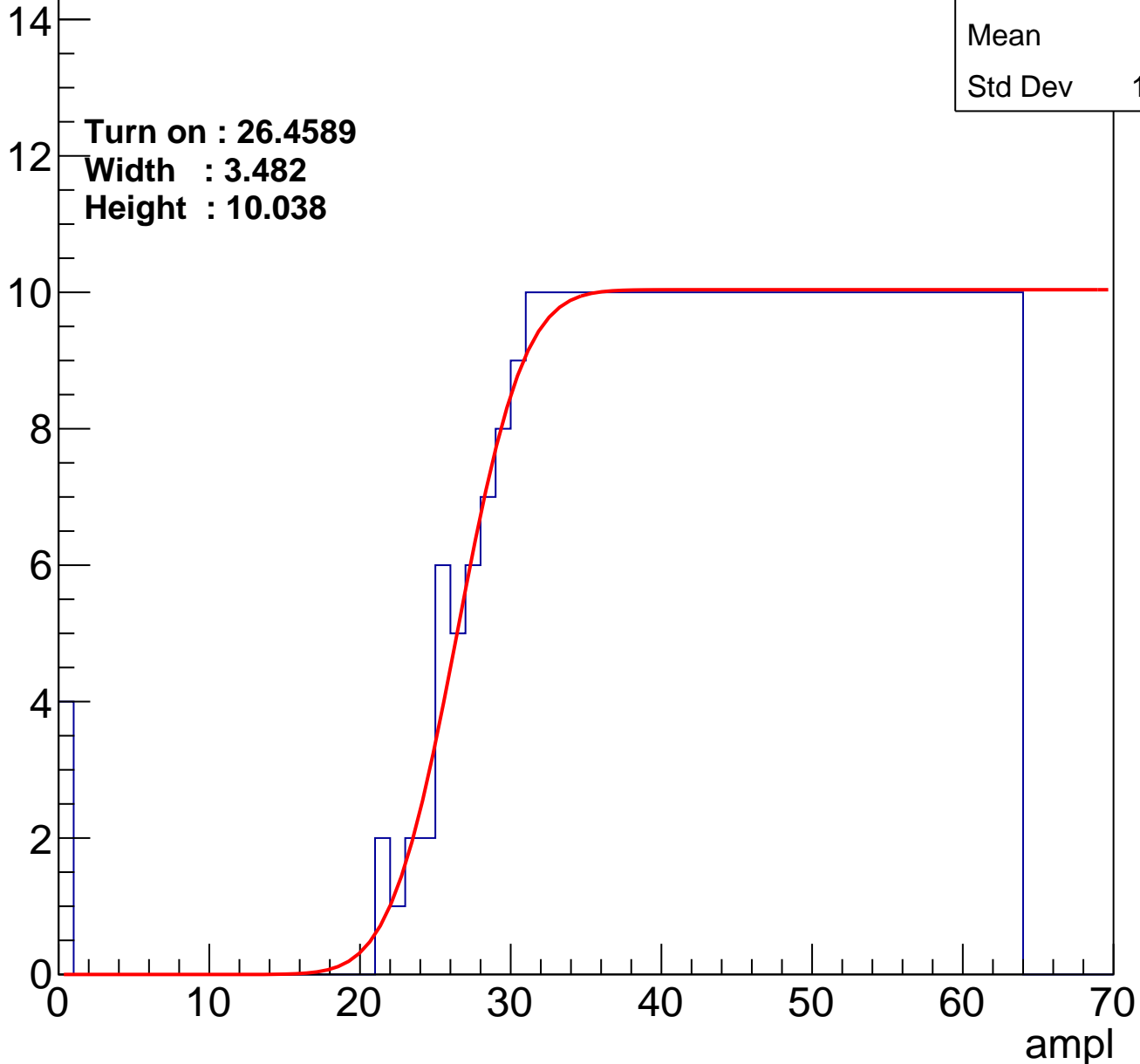
Entries	382
Mean	44
Std Dev	11.97

Turn on : 26.4589

Width : 3.482

Height : 10.038

Entry



B0L001S, U1-ch26

calib_packv5_042523_0143.root, FC#9, port A1

Entries	365
Mean	45.08
Std Dev	10.91

Turn on : 28.0670

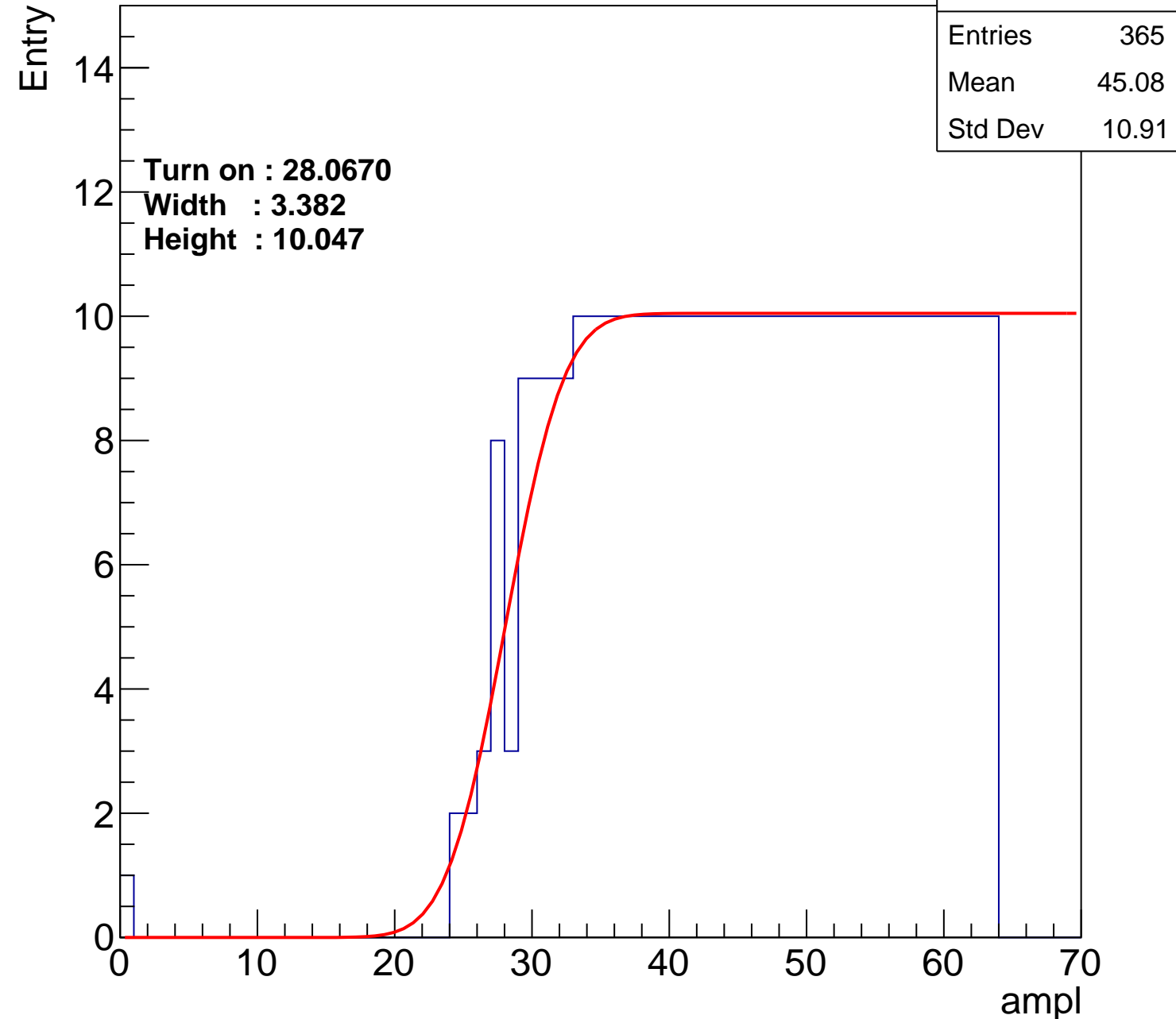
Width : 3.382

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch27

calib_packv5_042523_0143.root, FC#9, port A1

Entries	361
Mean	45.21
Std Dev	11.01

Turn on : 28.4406

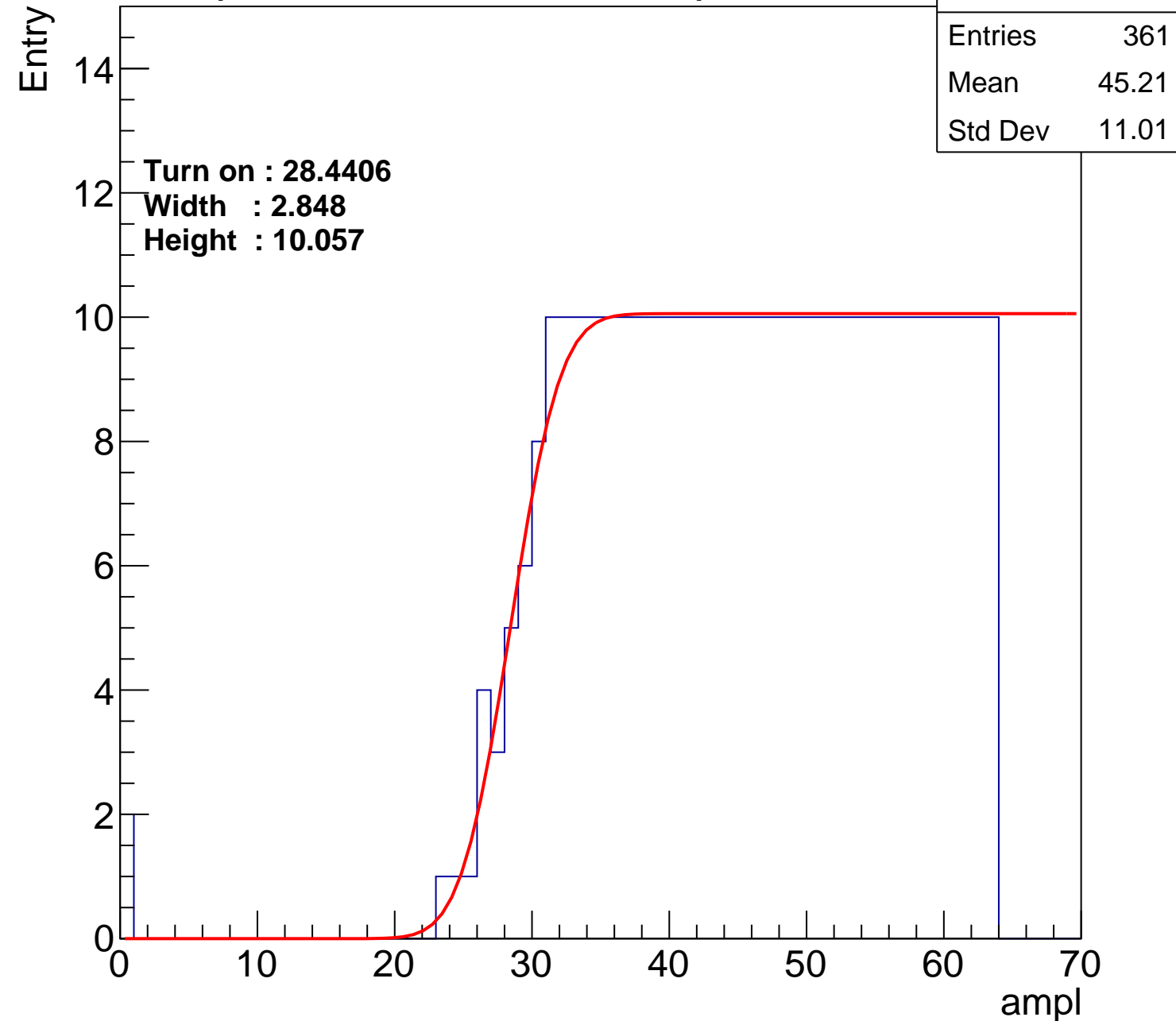
Width : 2.848

Height : 10.057

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch28

calib_packv5_042523_0143.root, FC#9, port A1

Entries	351
Mean	45.57
Std Dev	11.08

Turn on : 29.5835

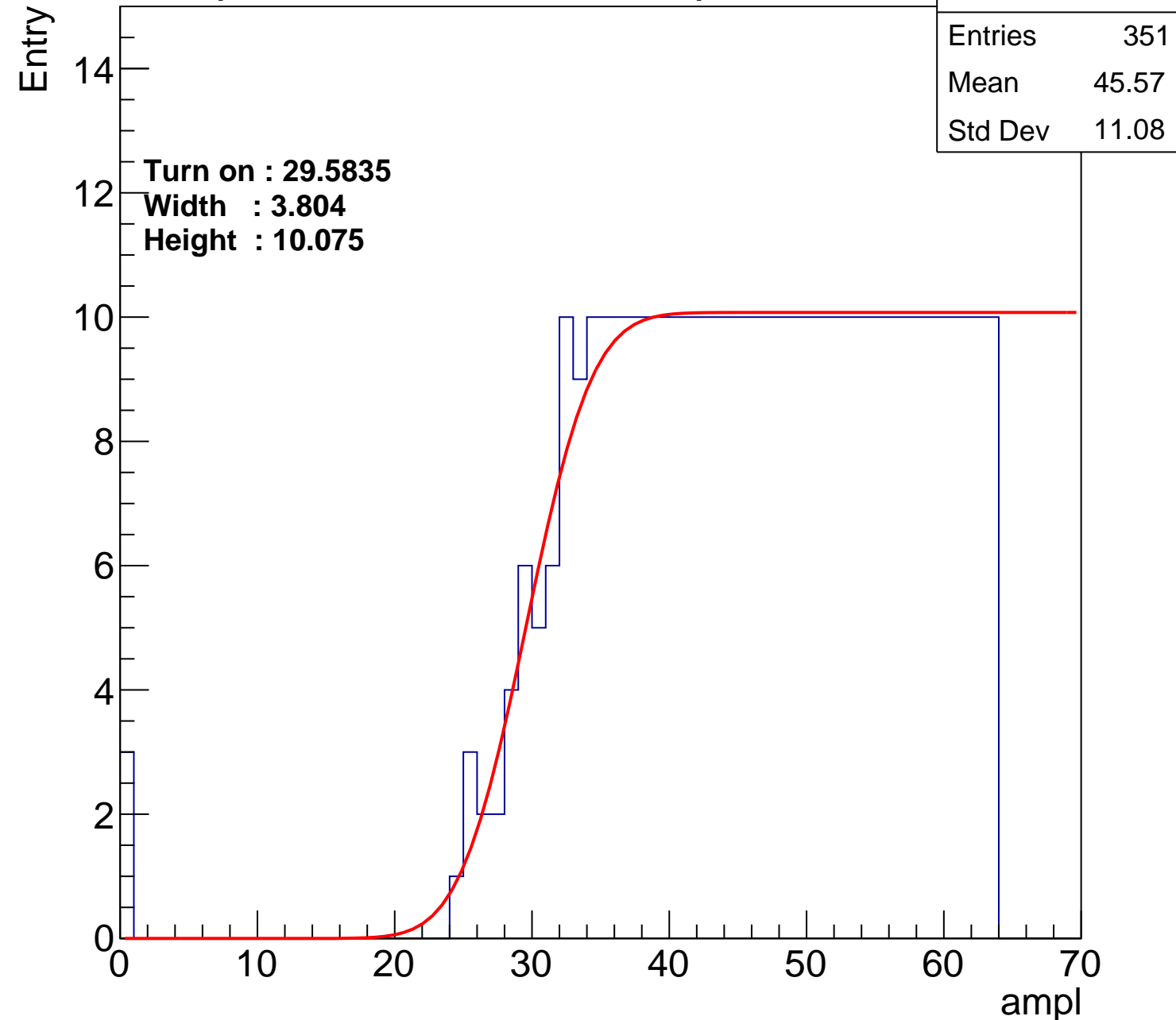
Width : 3.804

Height : 10.075

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch29

calib_packv5_042523_0143.root, FC#9, port A1

Entries	371
Mean	44.59
Std Dev	11.63

Turn on : 27.3155

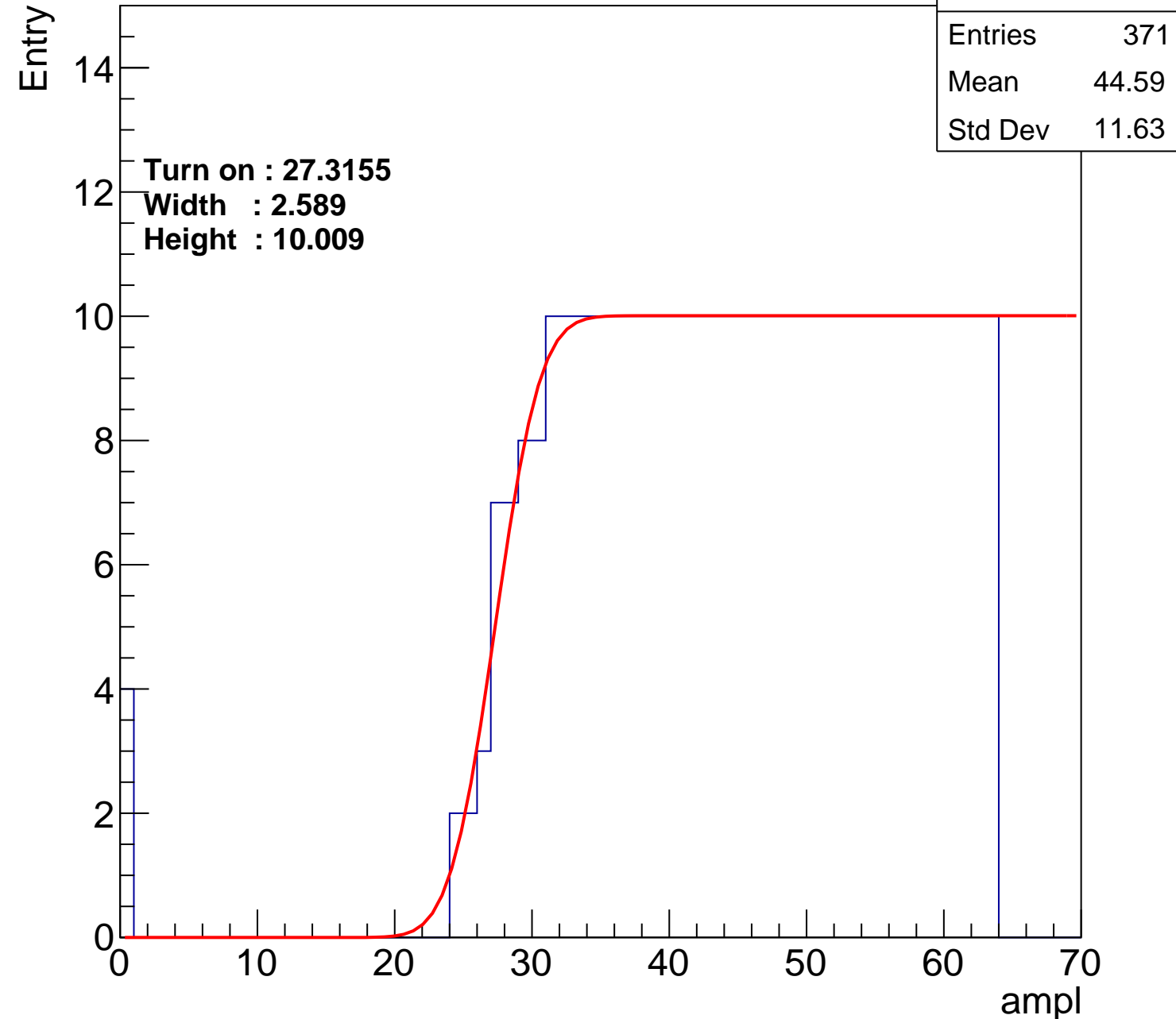
Width : 2.589

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch30

calib_packv5_042523_0143.root, FC#9, port A1

Entries	372
Mean	44.58
Std Dev	11.52

Turn on : 27.5950

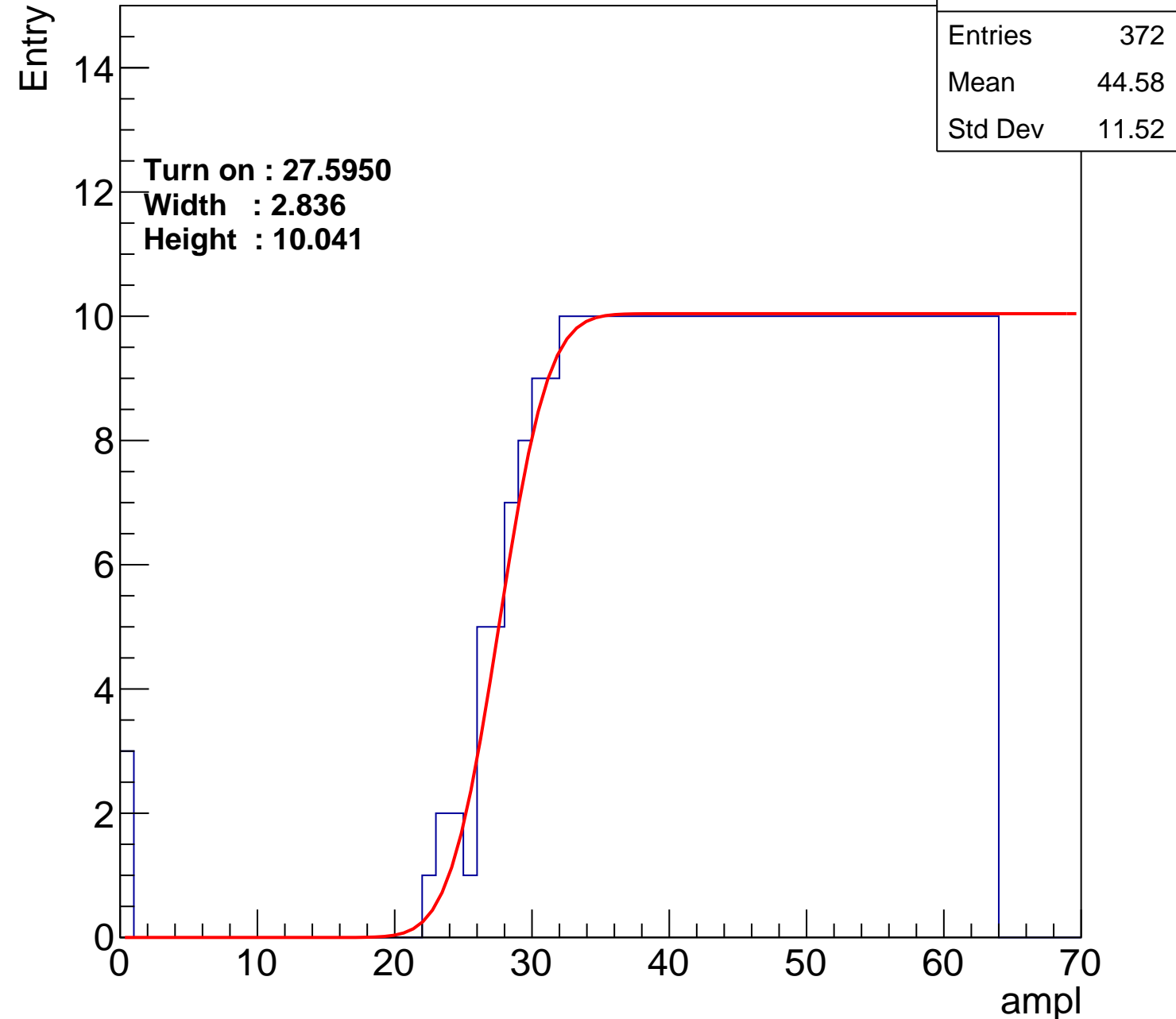
Width : 2.836

Height : 10.041

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch31

calib_packv5_042523_0143.root, FC#9, port A1

Entries	336
Mean	46.31
Std Dev	10.72

Turn on : 30.9829

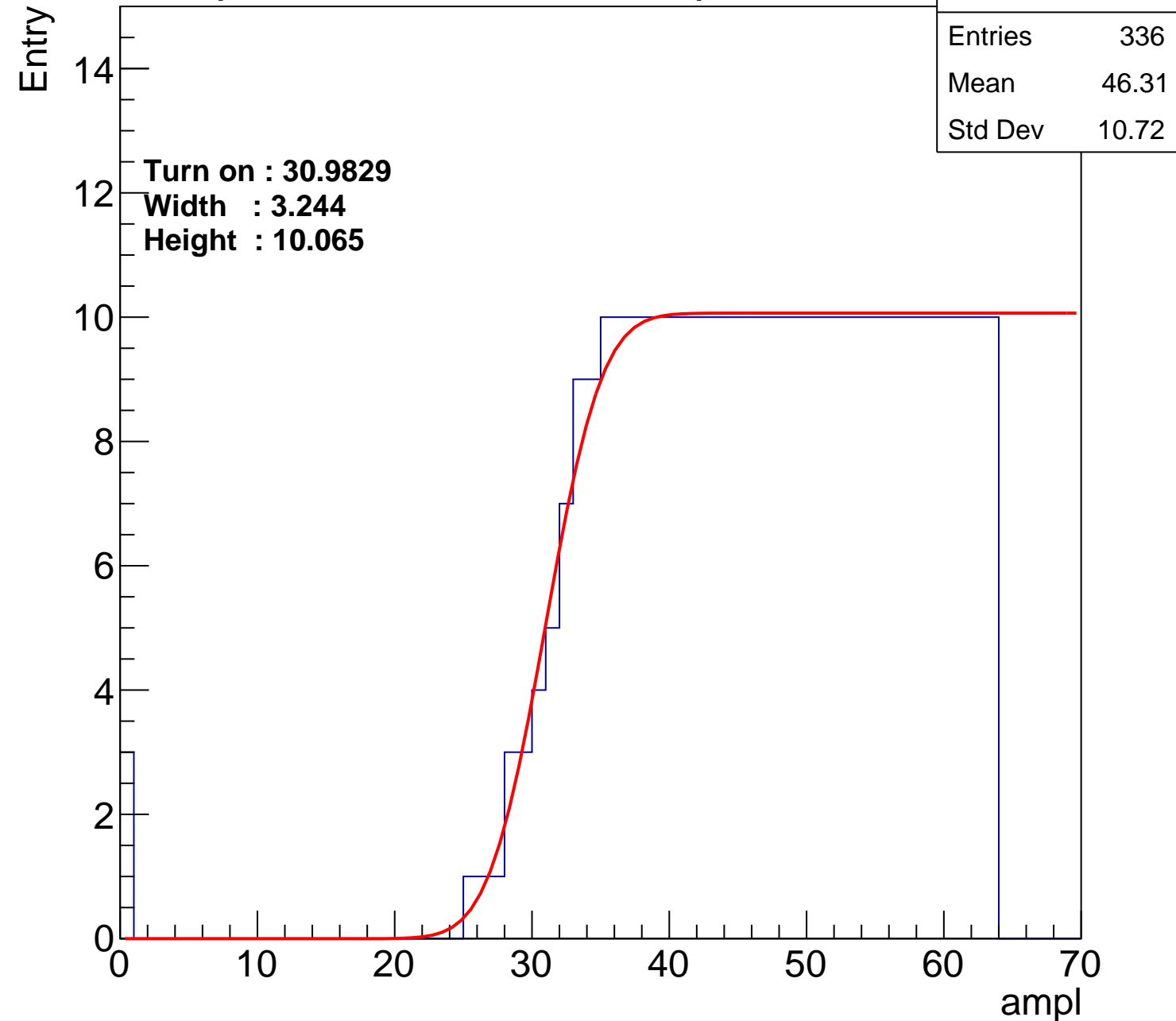
Width : 3.244

Height : 10.065

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch32

calib_packv5_042523_0143.root, FC#9, port A1

Entries	371
Mean	44.59
Std Dev	11.55

Turn on : 27.2610

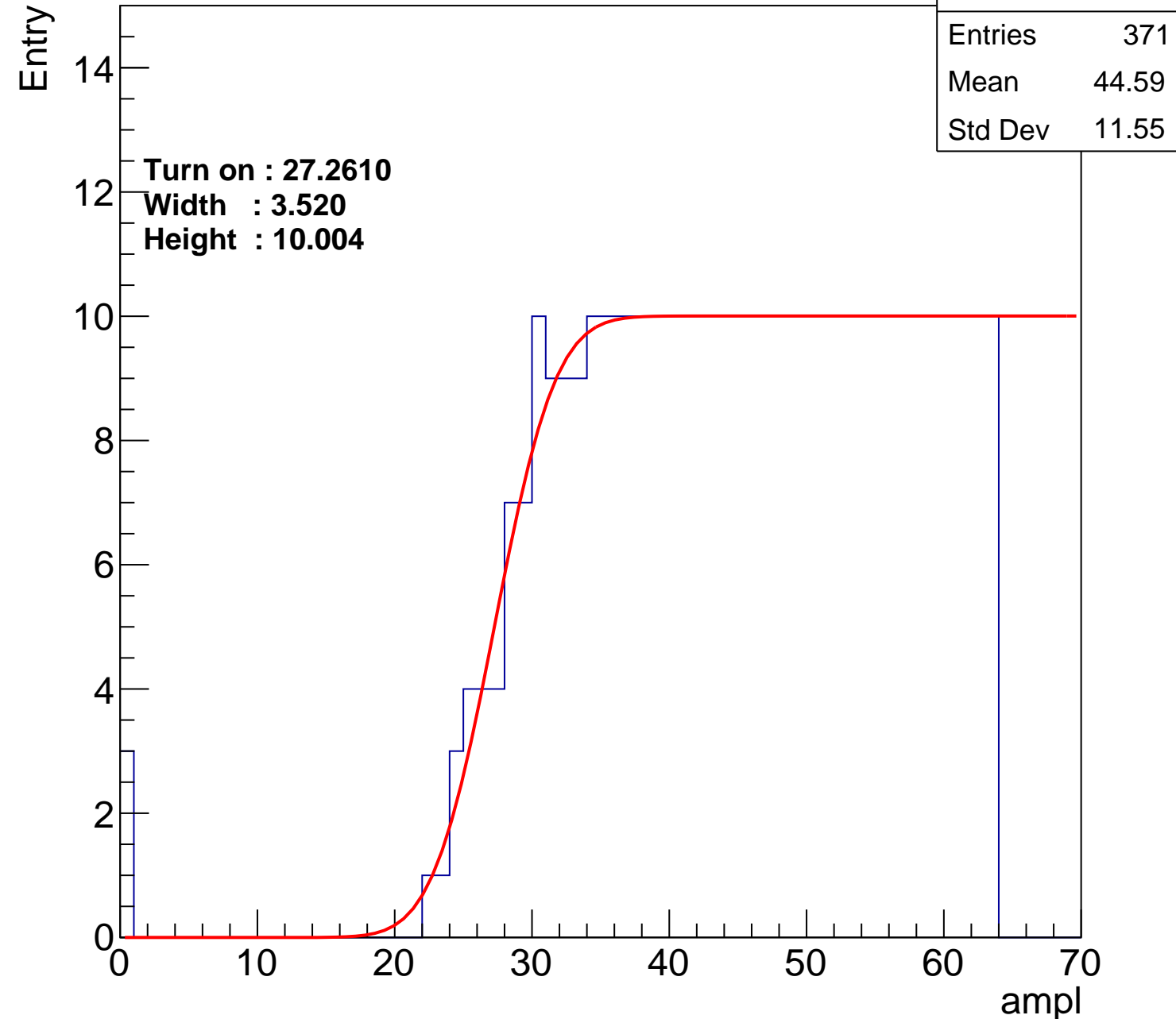
Width : 3.520

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch33

calib_packv5_042523_0143.root, FC#9, port A1

Entries	354
Mean	45.46
Std Dev	11.09

Turn on : 29.2063

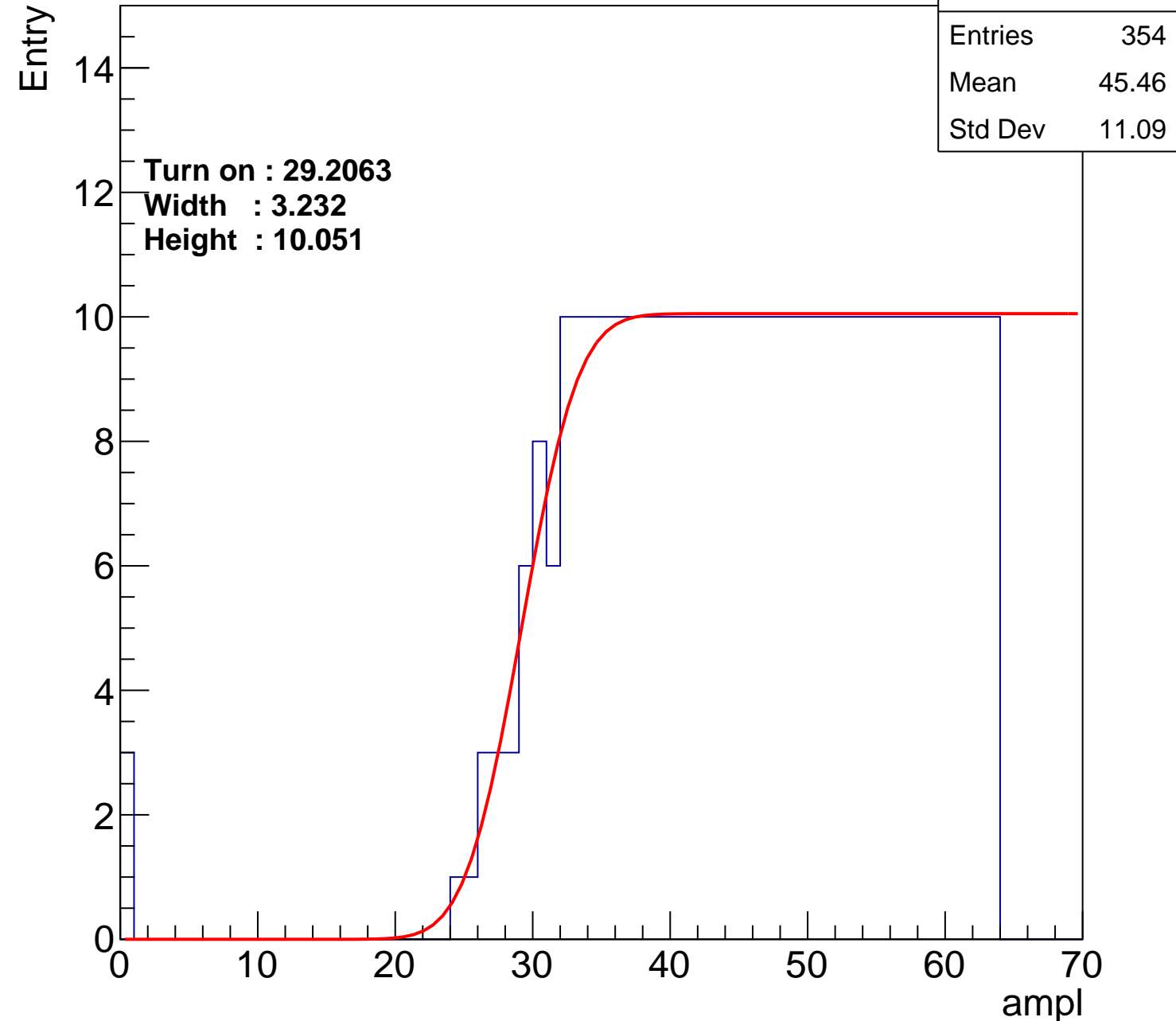
Width : 3.232

Height : 10.051

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch34

calib_packv5_042523_0143.root, FC#9, port A1

Entries	363
Mean	44.98
Std Dev	11.35

Turn on : 27.6604

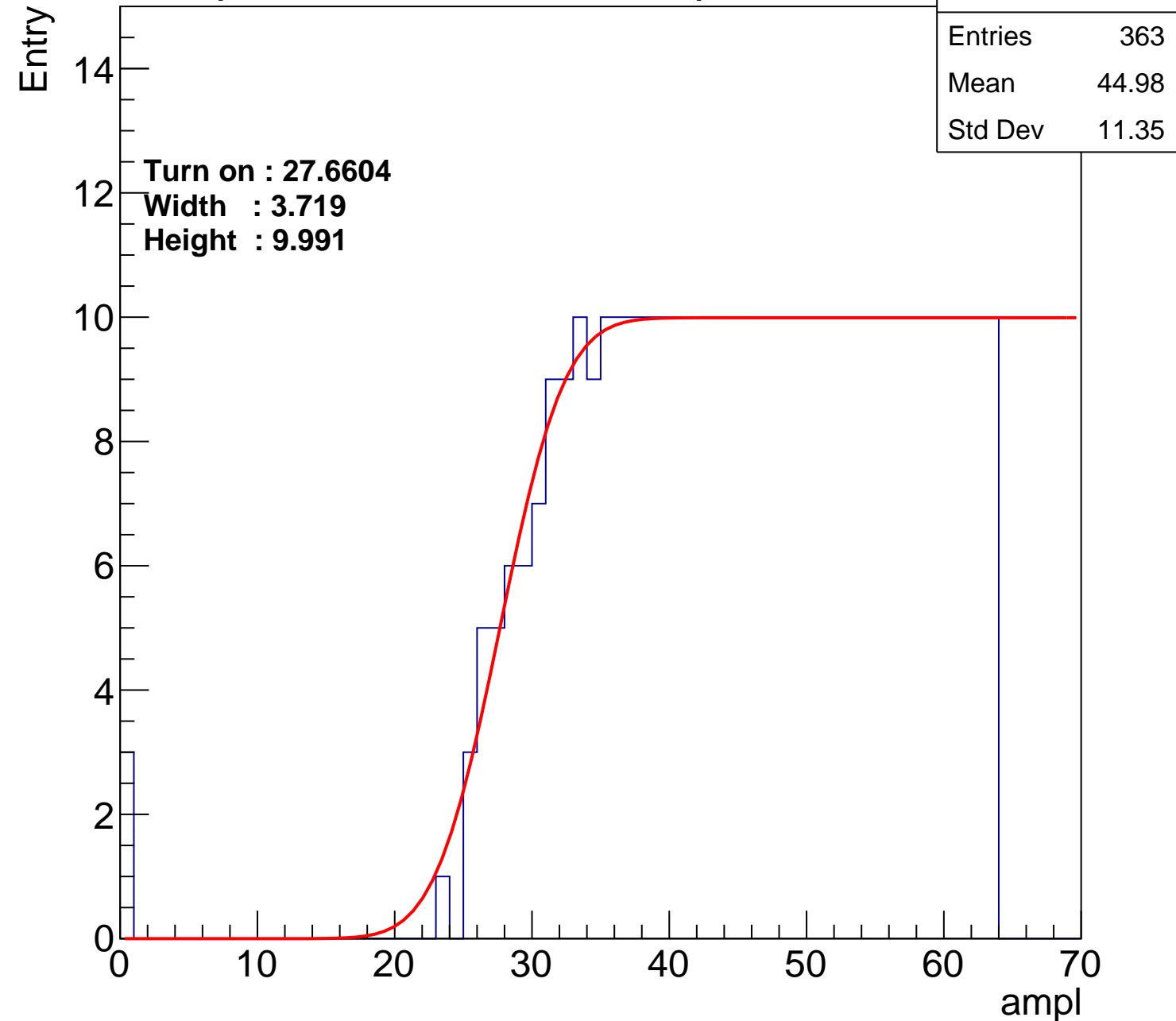
Width : 3.719

Height : 9.991

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch35

calib_packv5_042523_0143.root, FC#9, port A1

Entries	375
Mean	44.53
Std Dev	11.35

Turn on : 26.8081

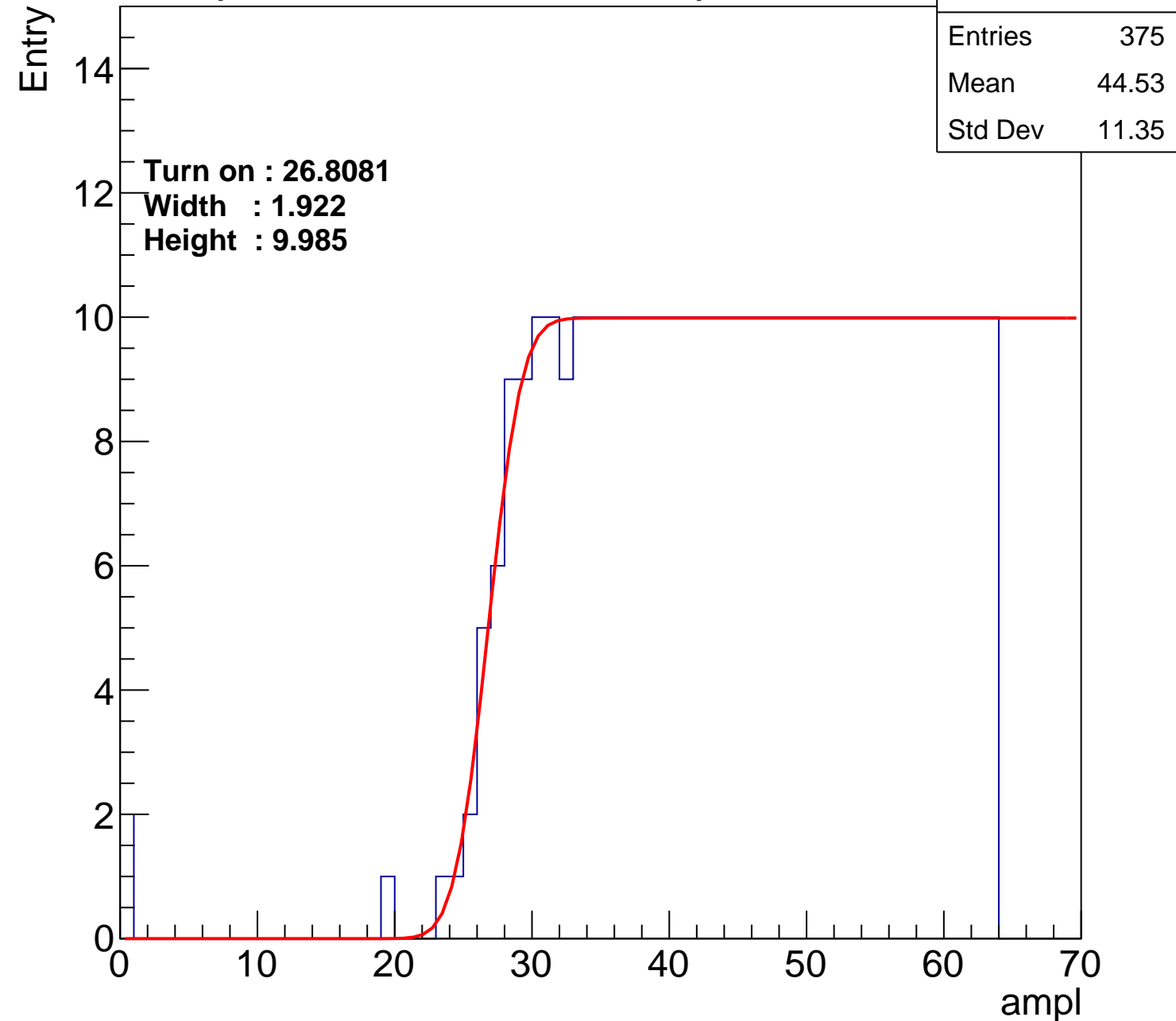
Width : 1.922

Height : 9.985

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch36

calib_packv5_042523_0143.root, FC#9, port A1

Entries	378
Mean	44.29
Std Dev	11.65

Turn on : 26.7312

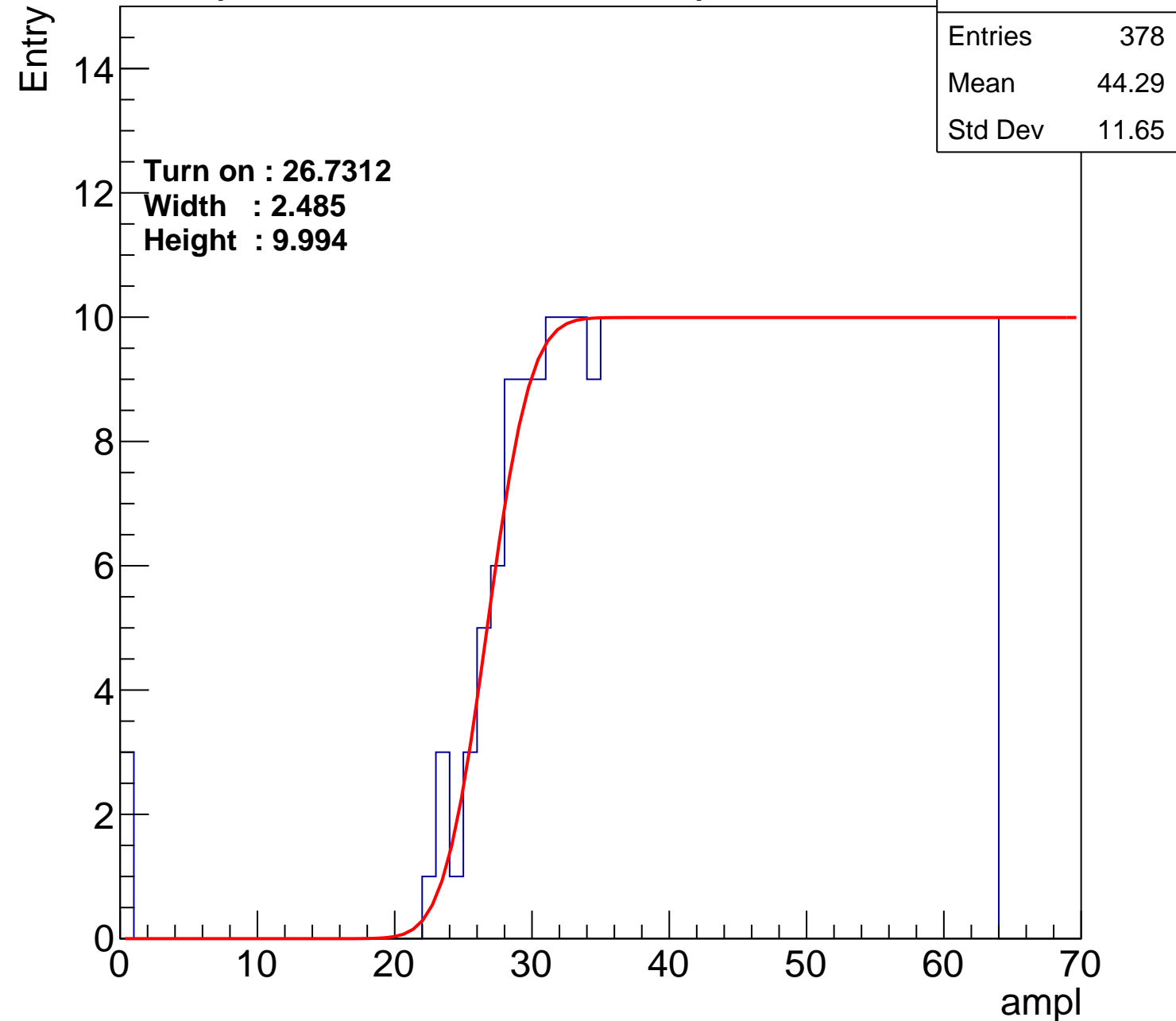
Width : 2.485

Height : 9.994

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch37

calib_packv5_042523_0143.root, FC#9, port A1

Entries	383
Mean	44.19
Std Dev	11.39

Turn on : 26.4822

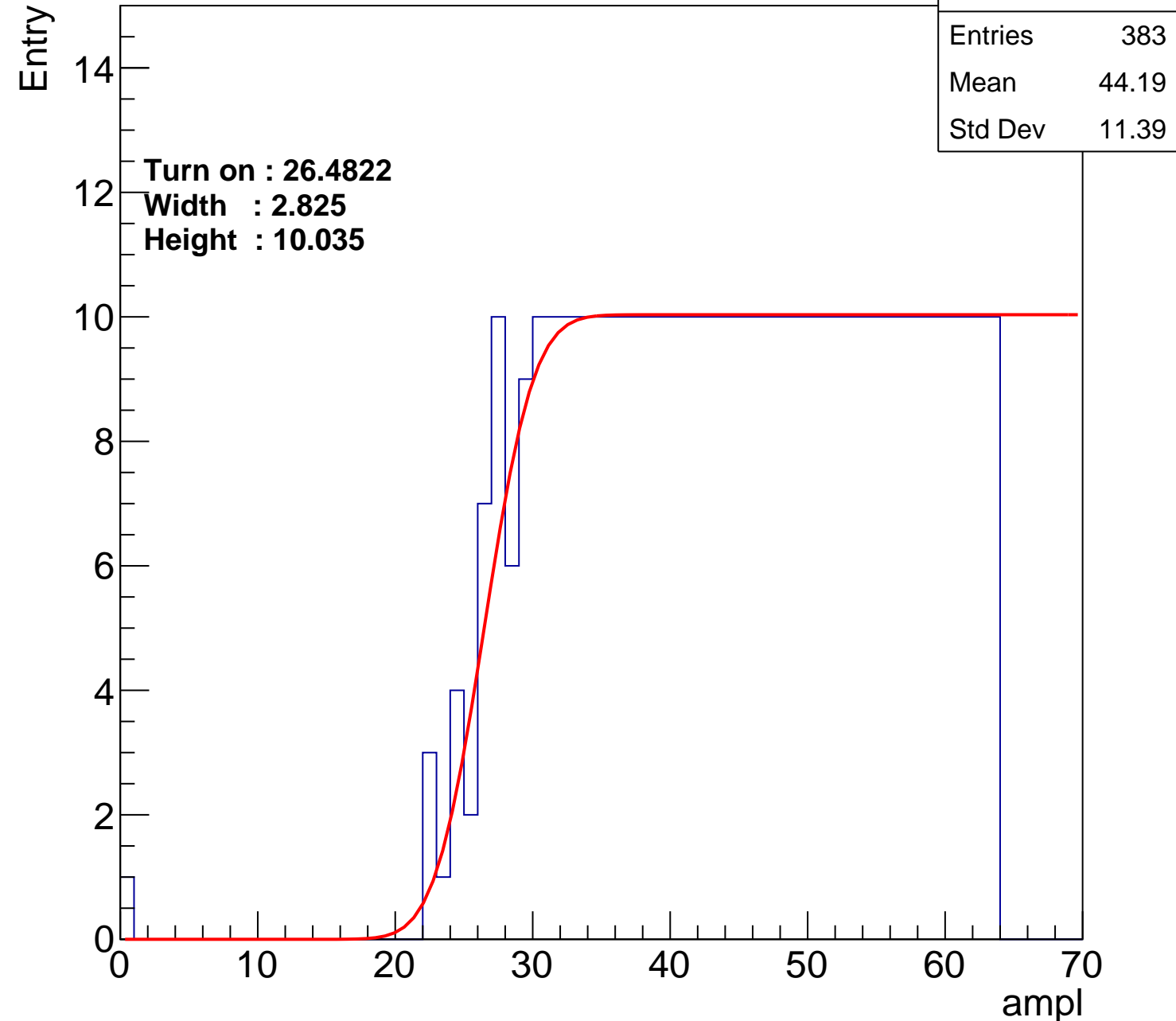
Width : 2.825

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch38

calib_packv5_042523_0143.root, FC#9, port A1

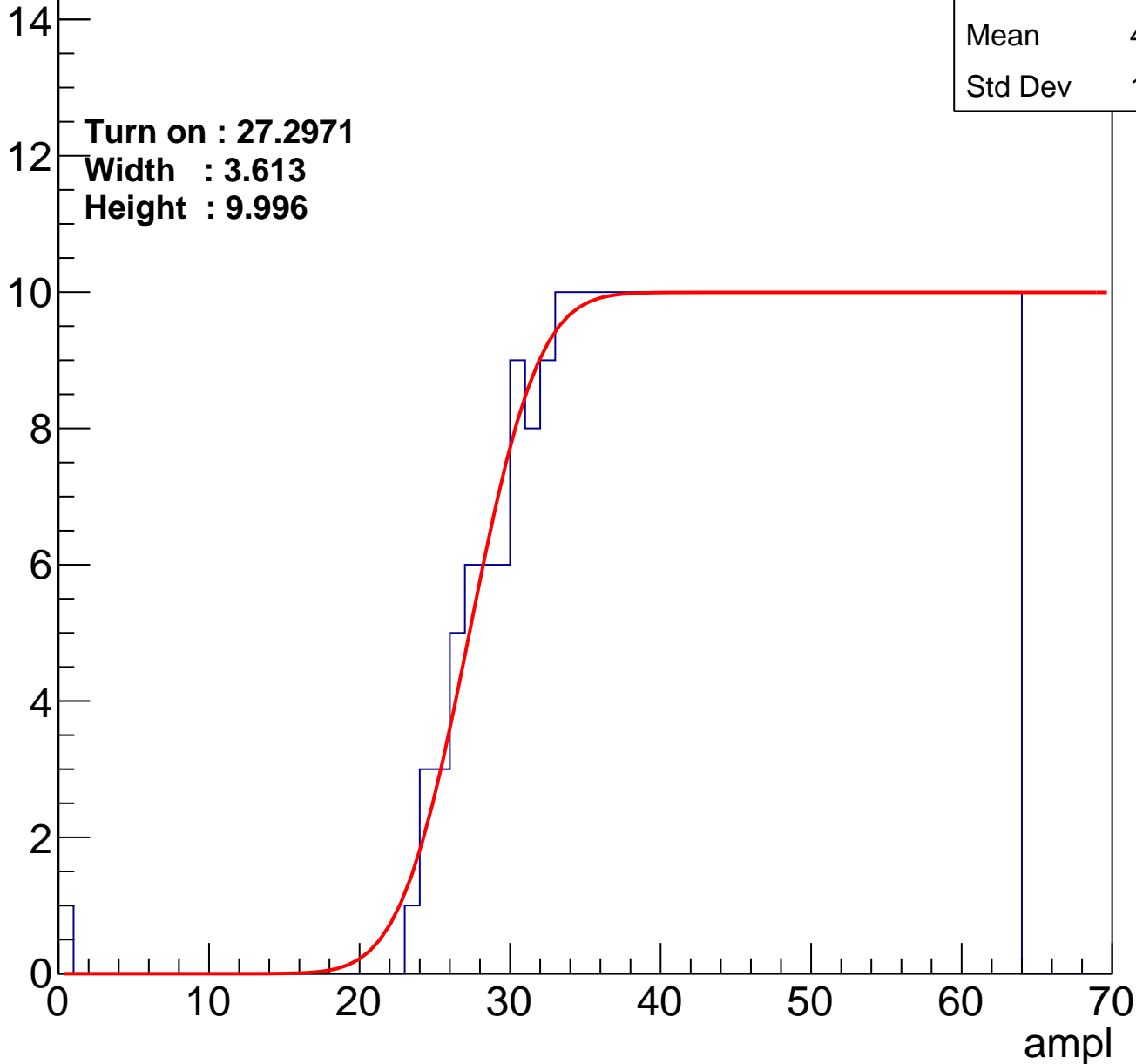
Entry

Entries	367
Mean	44.93
Std Dev	11.04

Turn on : 27.2971

Width : 3.613

Height : 9.996



B0L001S, U1-ch39

calib_packv5_042523_0143.root, FC#9, port A1

Entries	360
Mean	45.13
Std Dev	11.29

Turn on : 28.5814

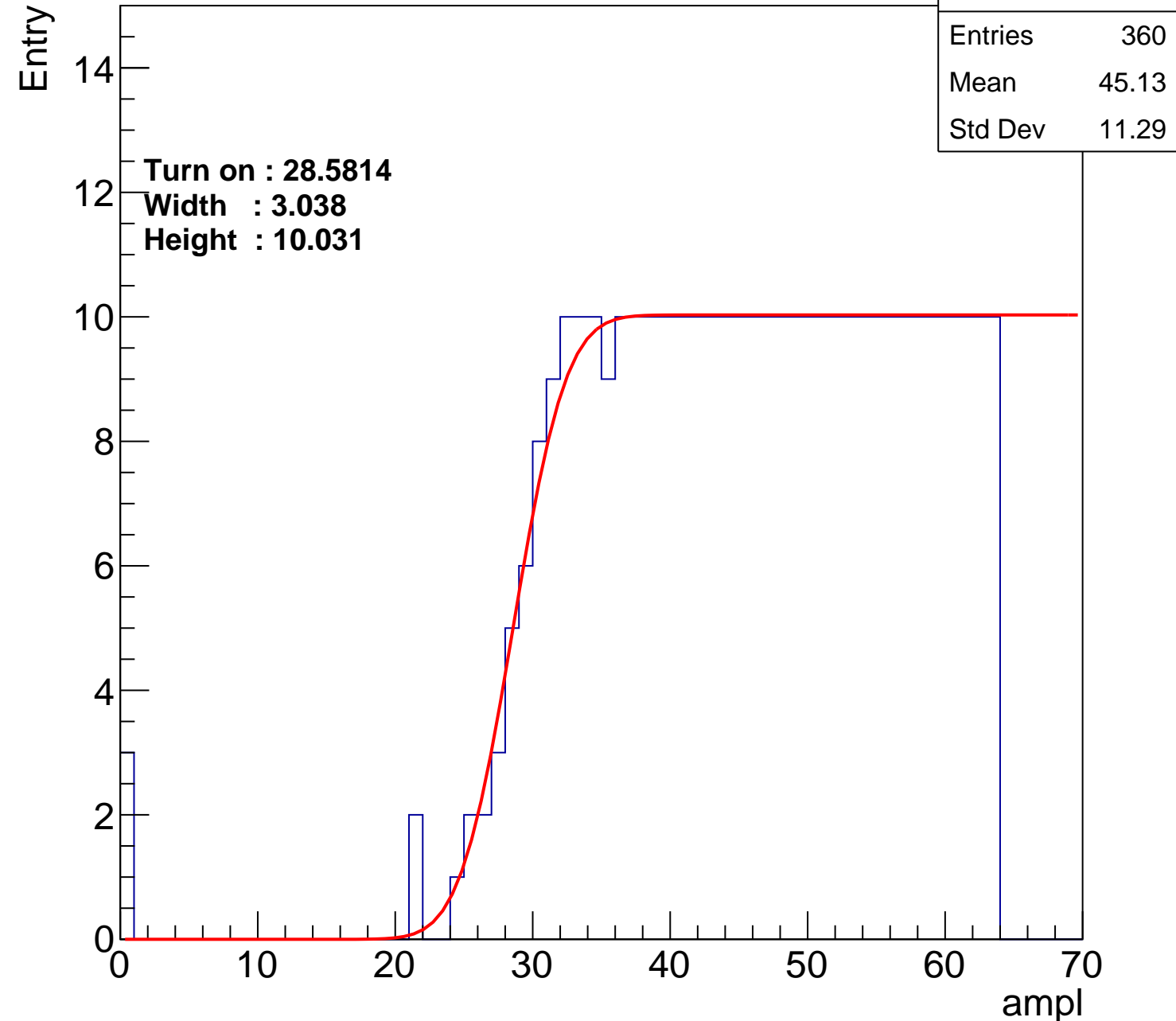
Width : 3.038

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch40

calib_packv5_042523_0143.root, FC#9, port A1

Entries	369
Mean	44.7
Std Dev	11.5

Turn on : 27.7462

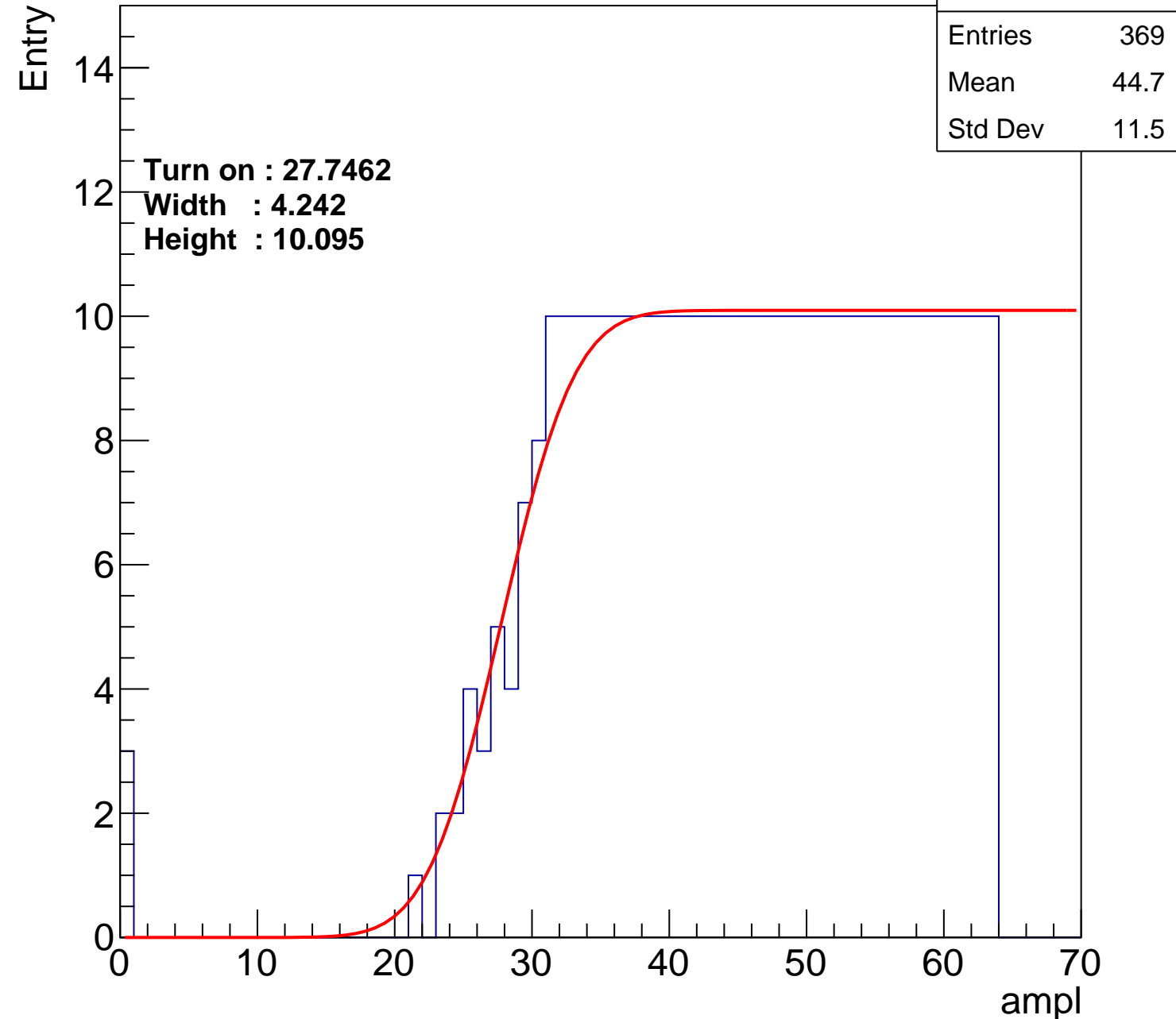
Width : 4.242

Height : 10.095

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch41

calib_packv5_042523_0143.root, FC#9, port A1

Entries	360
Mean	45.26
Std Dev	10.99

Turn on : 28.5957

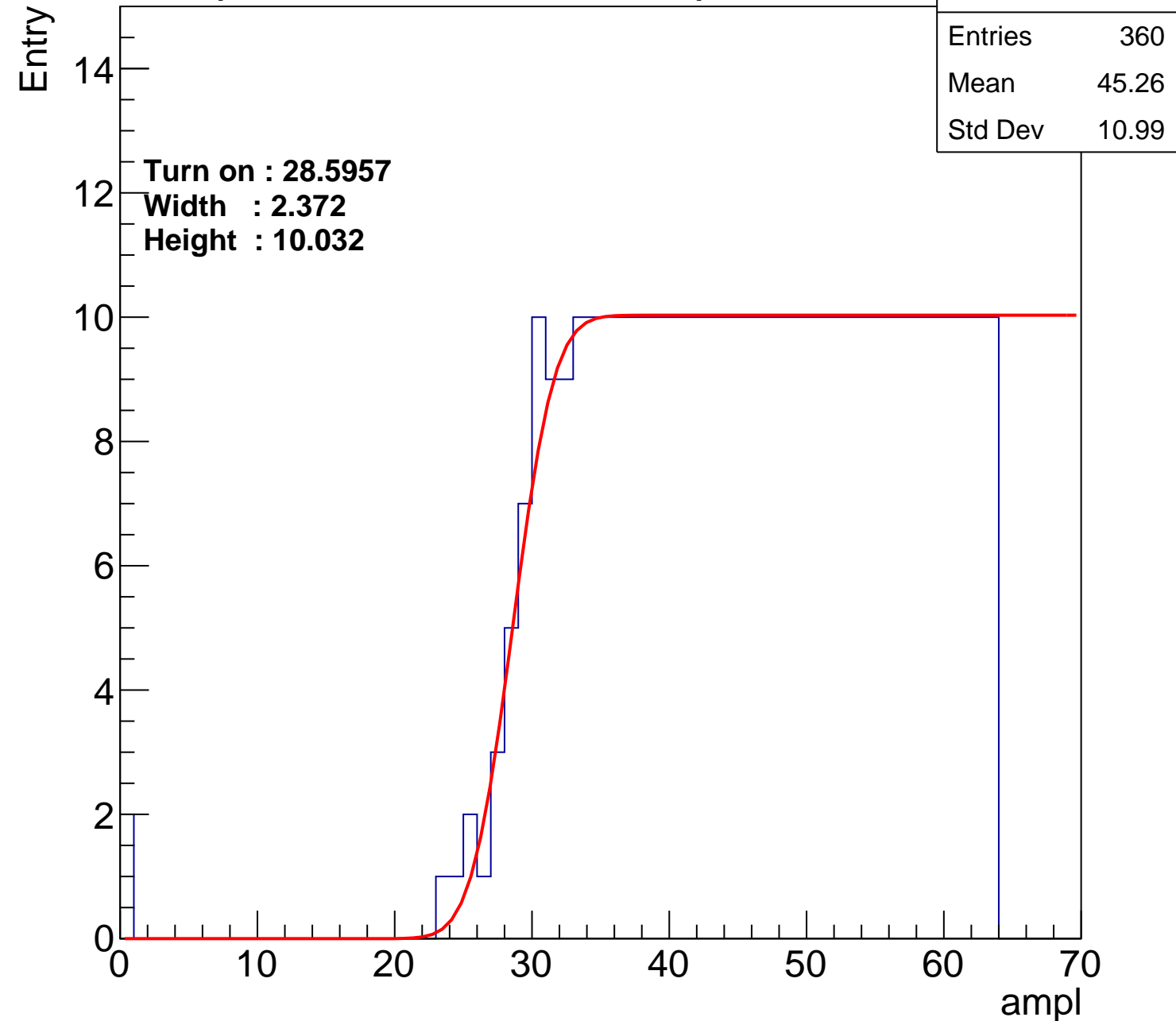
Width : 2.372

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch42

calib_packv5_042523_0143.root, FC#9, port A1

Entries	348
Mean	45.91
Std Dev	10.48

Turn on : 29.2336

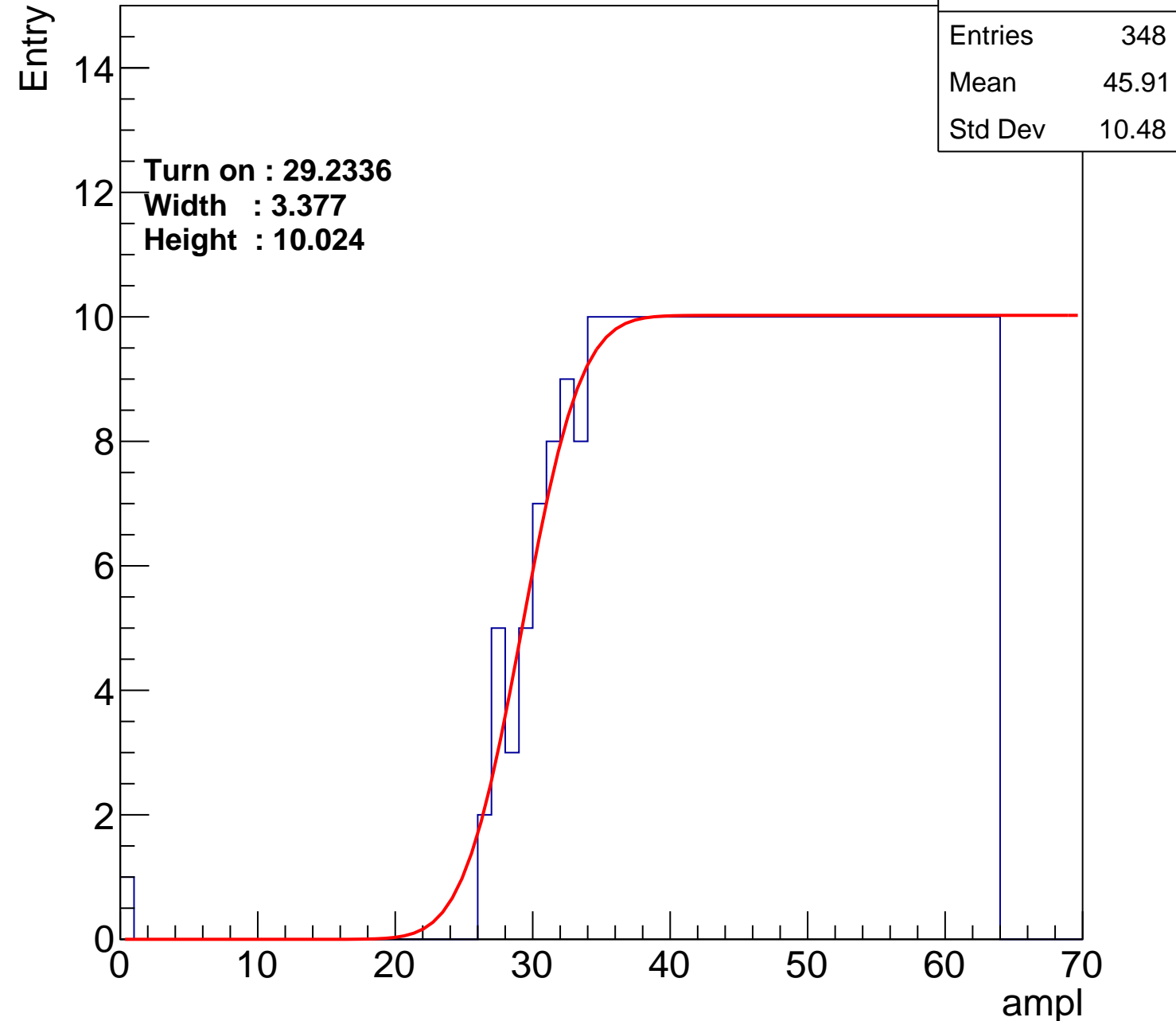
Width : 3.377

Height : 10.024

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch43

calib_packv5_042523_0143.root, FC#9, port A1

Entries	374
Mean	44.57
Std Dev	11.36

Turn on : 27.2250

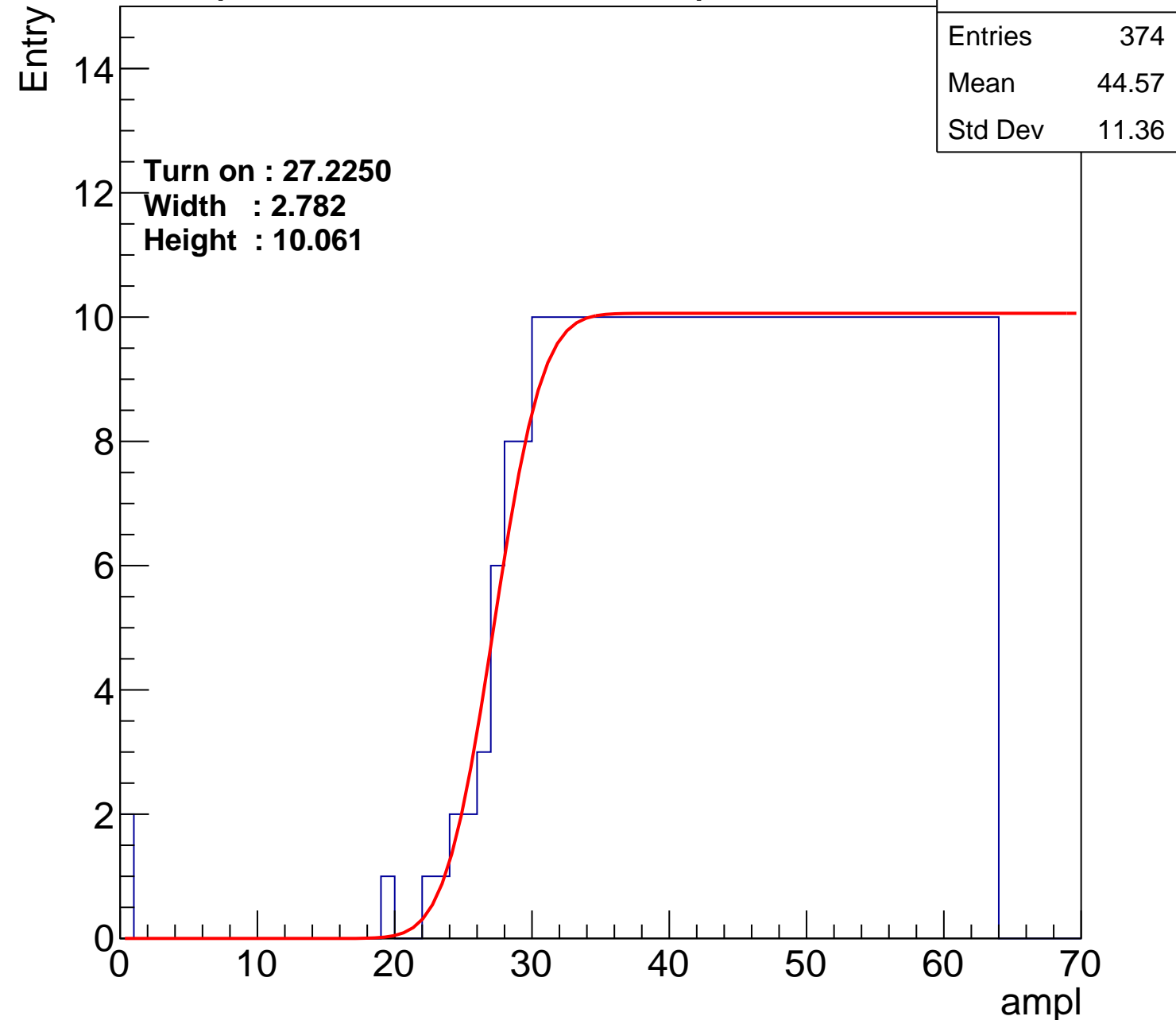
Width : 2.782

Height : 10.061

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch44

calib_packv5_042523_0143.root, FC#9, port A1

Entries	361
Mean	45.3
Std Dev	10.76

Turn on : 27.8845

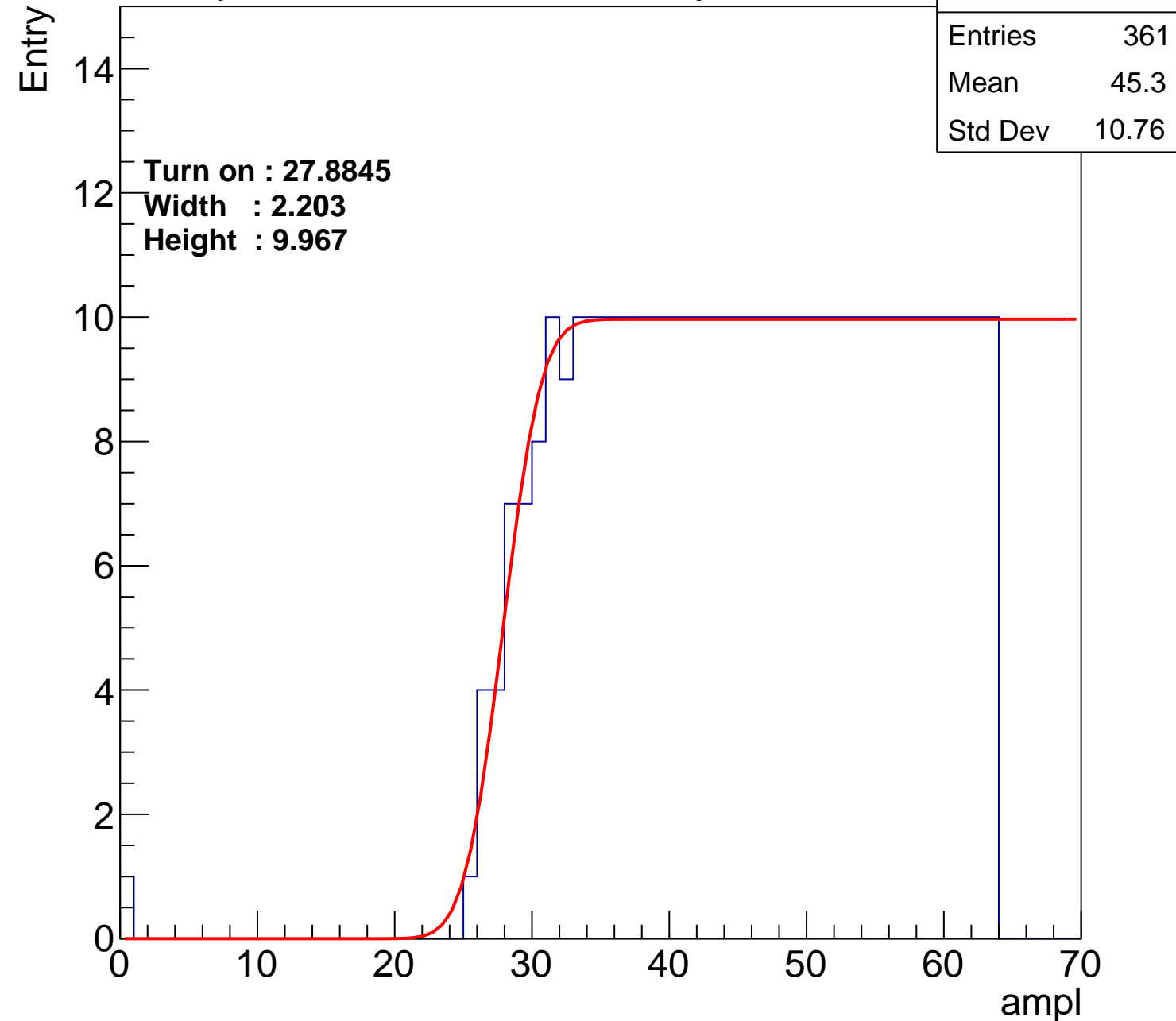
Width : 2.203

Height : 9.967

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch45

calib_packv5_042523_0143.root, FC#9, port A1

Entries	370
Mean	44.8
Std Dev	11.18

Turn on : 26.5198

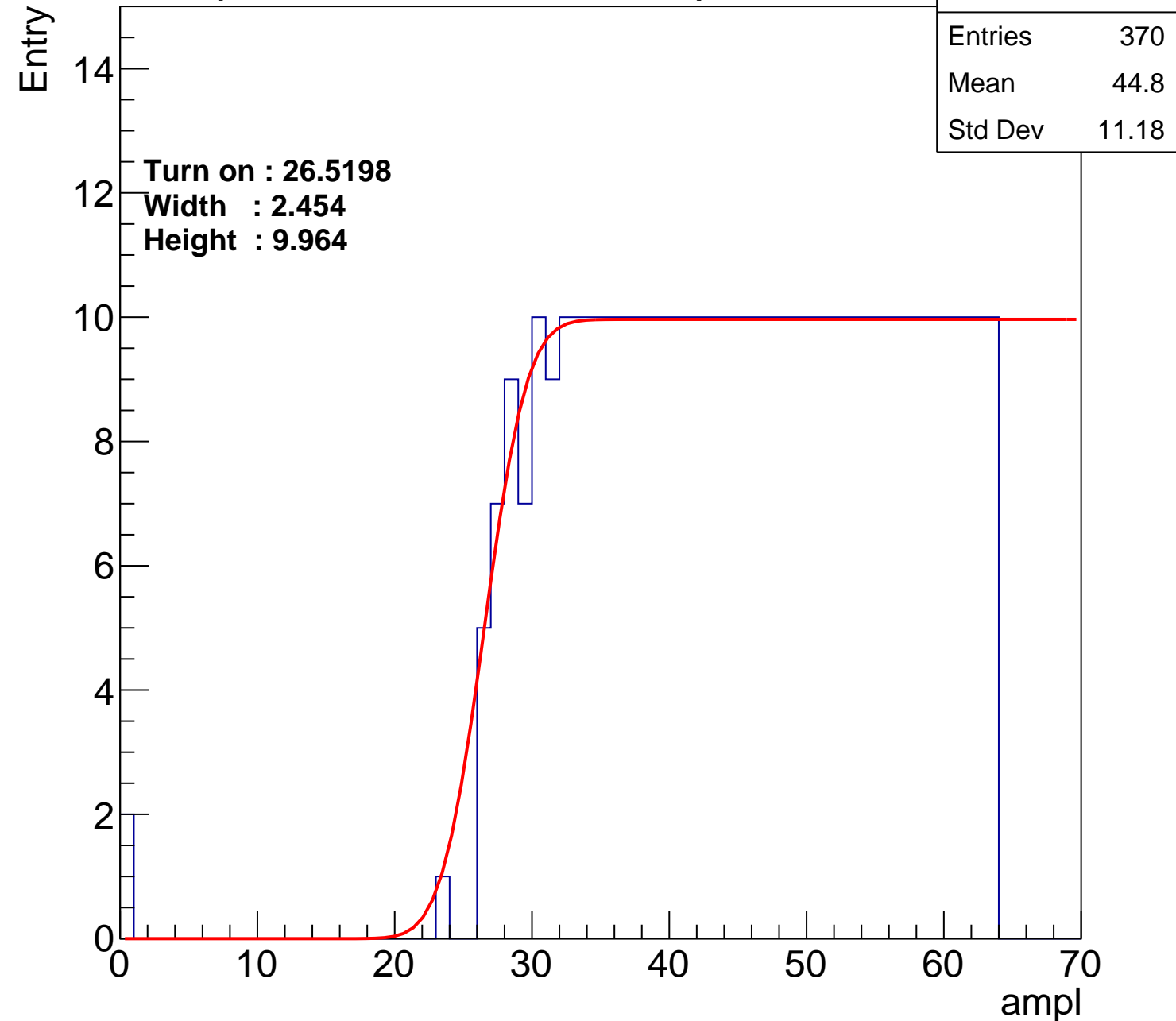
Width : 2.454

Height : 9.964

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch46

calib_packv5_042523_0143.root, FC#9, port A1

Entries	383
Mean	44.11
Std Dev	11.59

Turn on : 26.3584

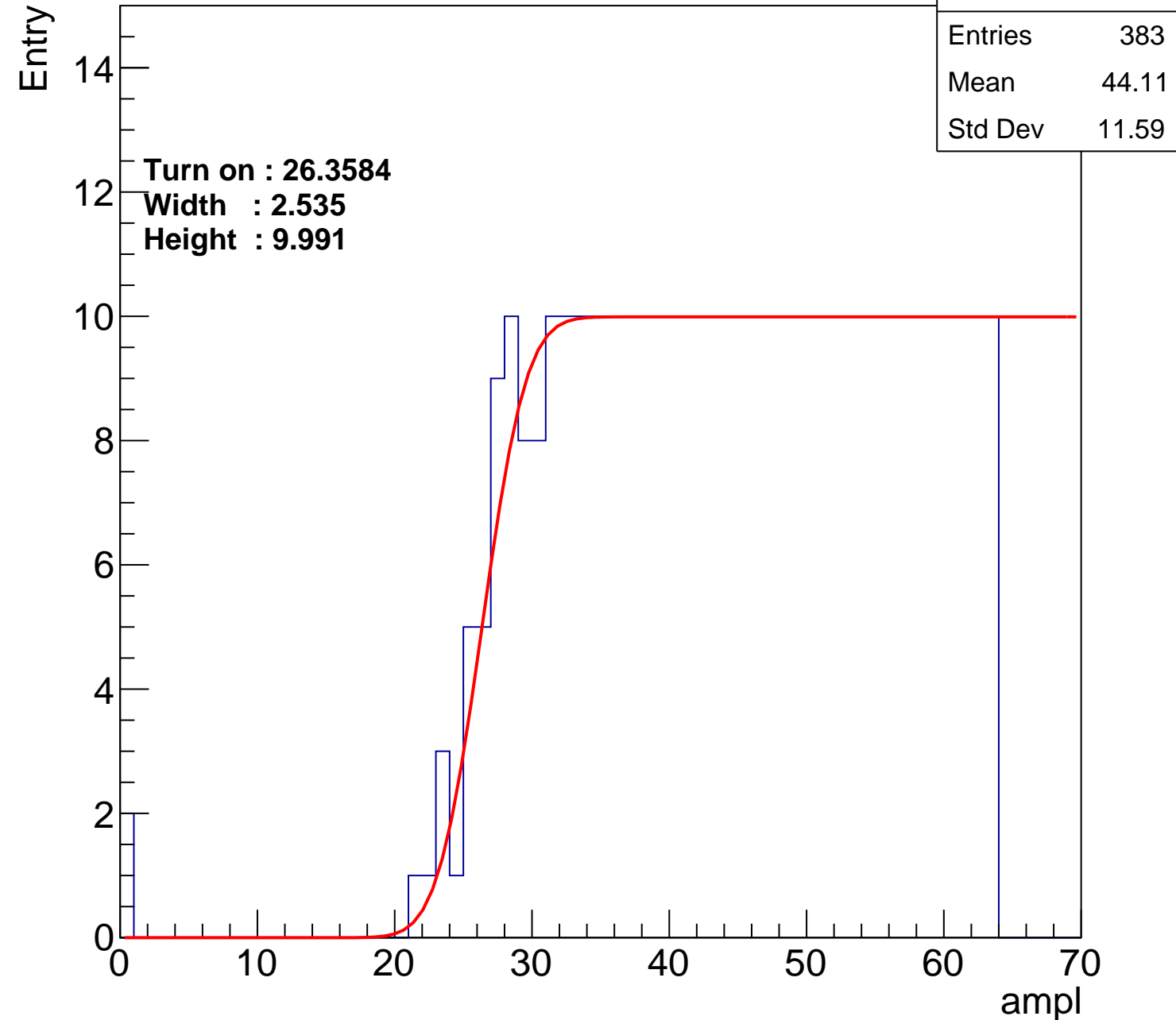
Width : 2.535

Height : 9.991

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch47

calib_packv5_042523_0143.root, FC#9, port A1

Entries	360
Mean	45.32
Std Dev	10.79

Turn on : 28.7214

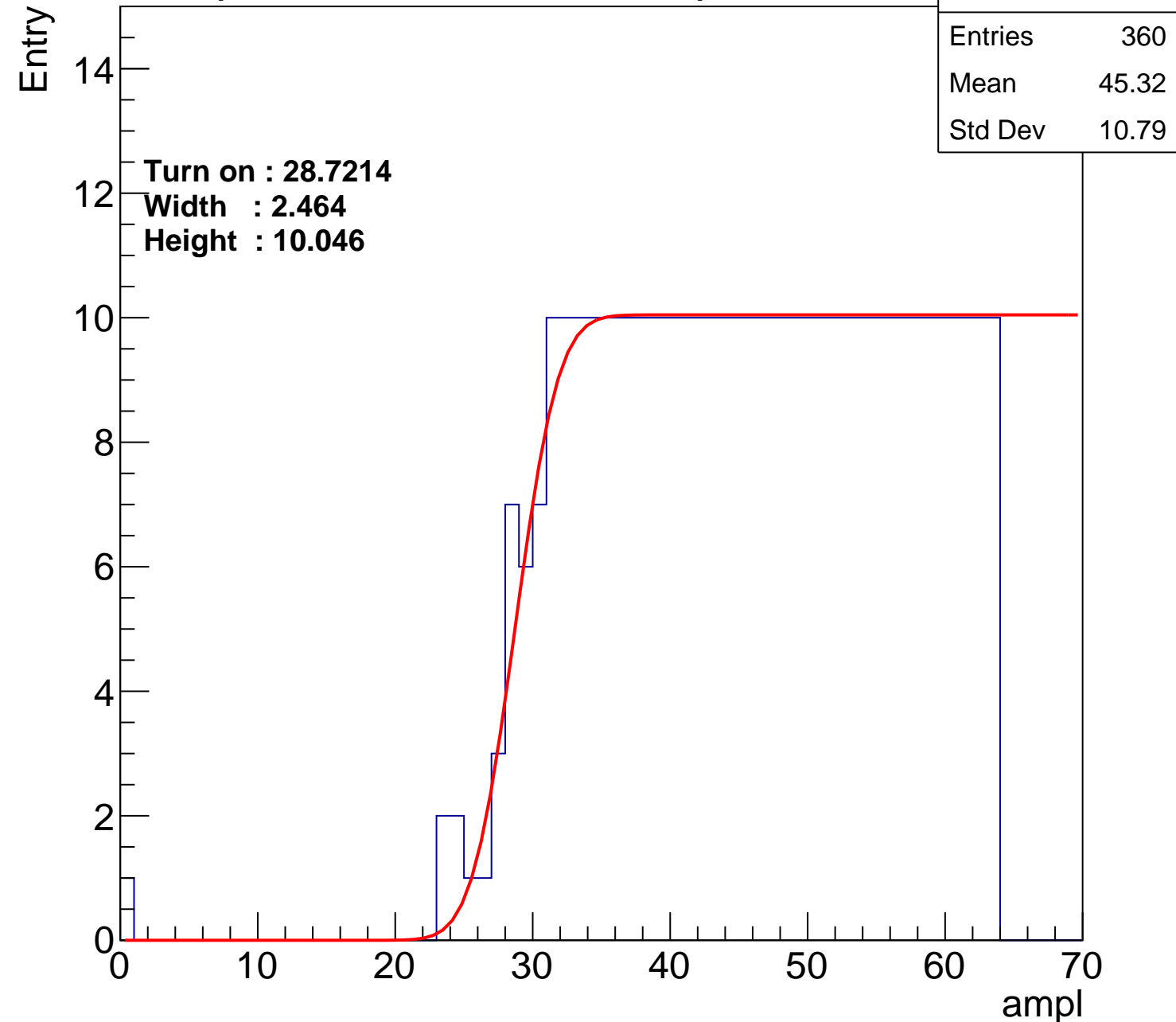
Width : 2.464

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch48

calib_packv5_042523_0143.root, FC#9, port A1

Entries	387
Mean	43.76
Std Dev	12.06

Turn on : 25.6991

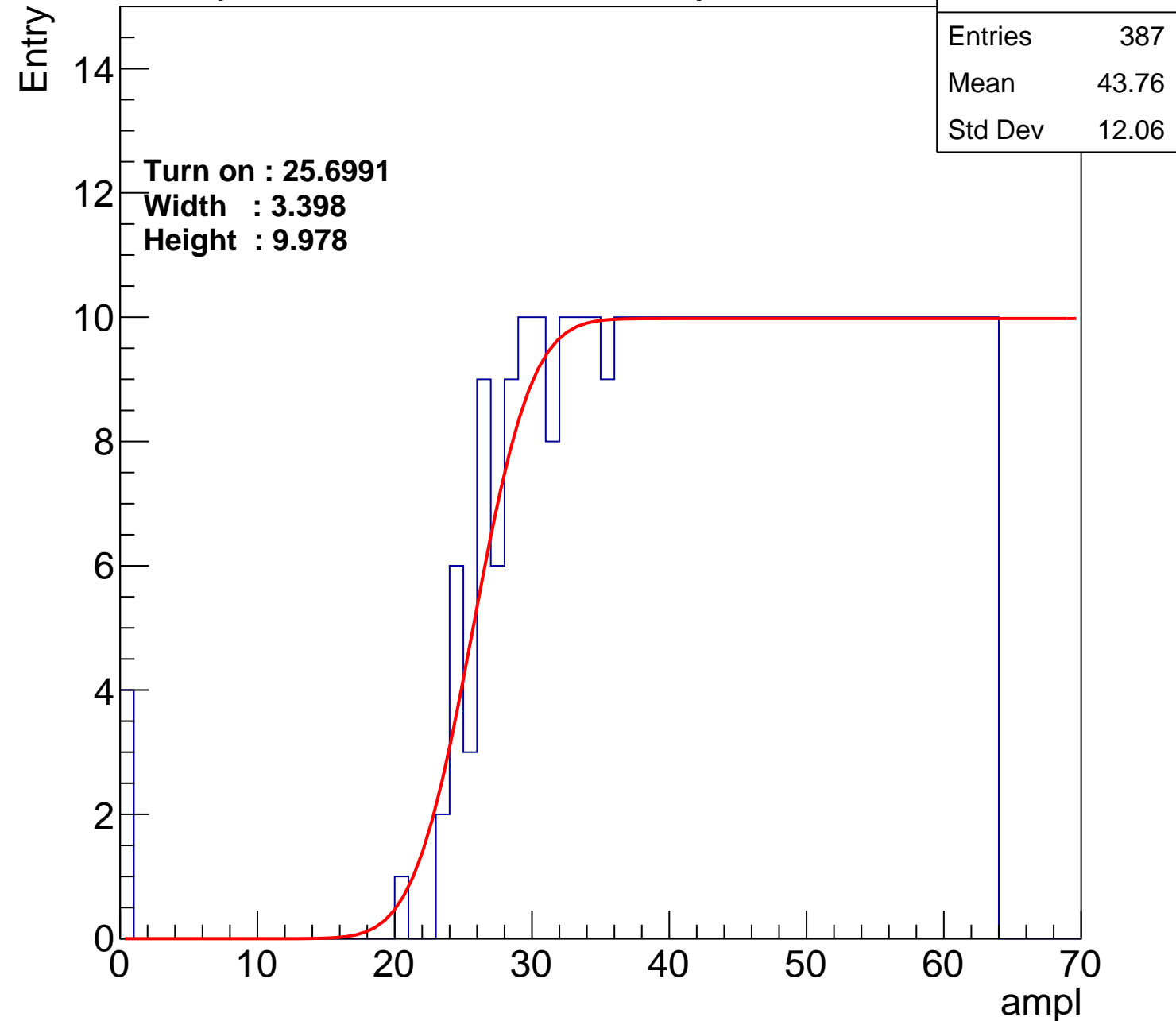
Width : 3.398

Height : 9.978

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch49

calib_packv5_042523_0143.root, FC#9, port A1

Entries	371
Mean	44.57
Std Dev	11.66

Turn on : 27.5099

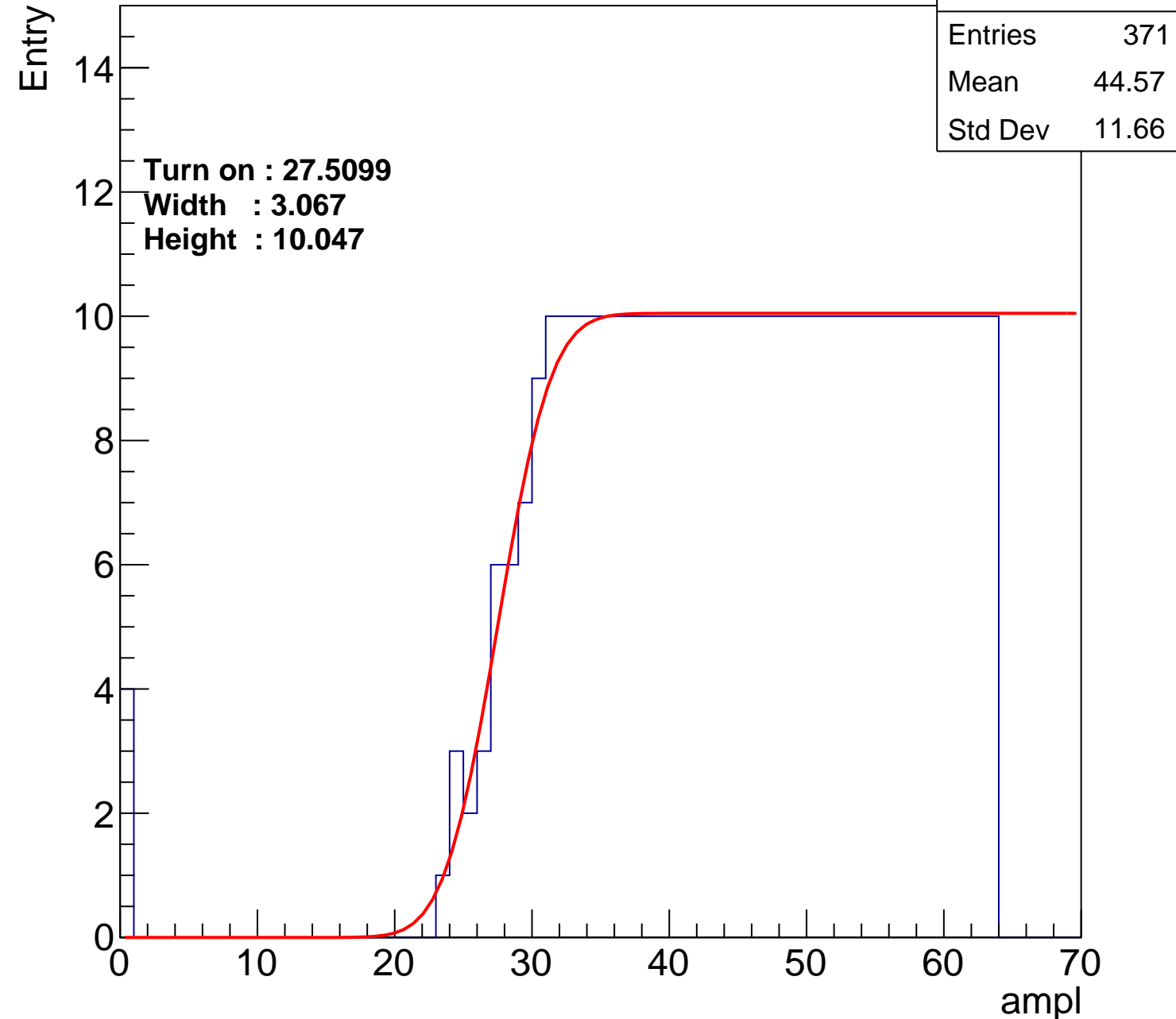
Width : 3.067

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch50

calib_packv5_042523_0143.root, FC#9, port A1

Entries	378
Mean	44.33
Std Dev	11.51

Turn on : 25.7495

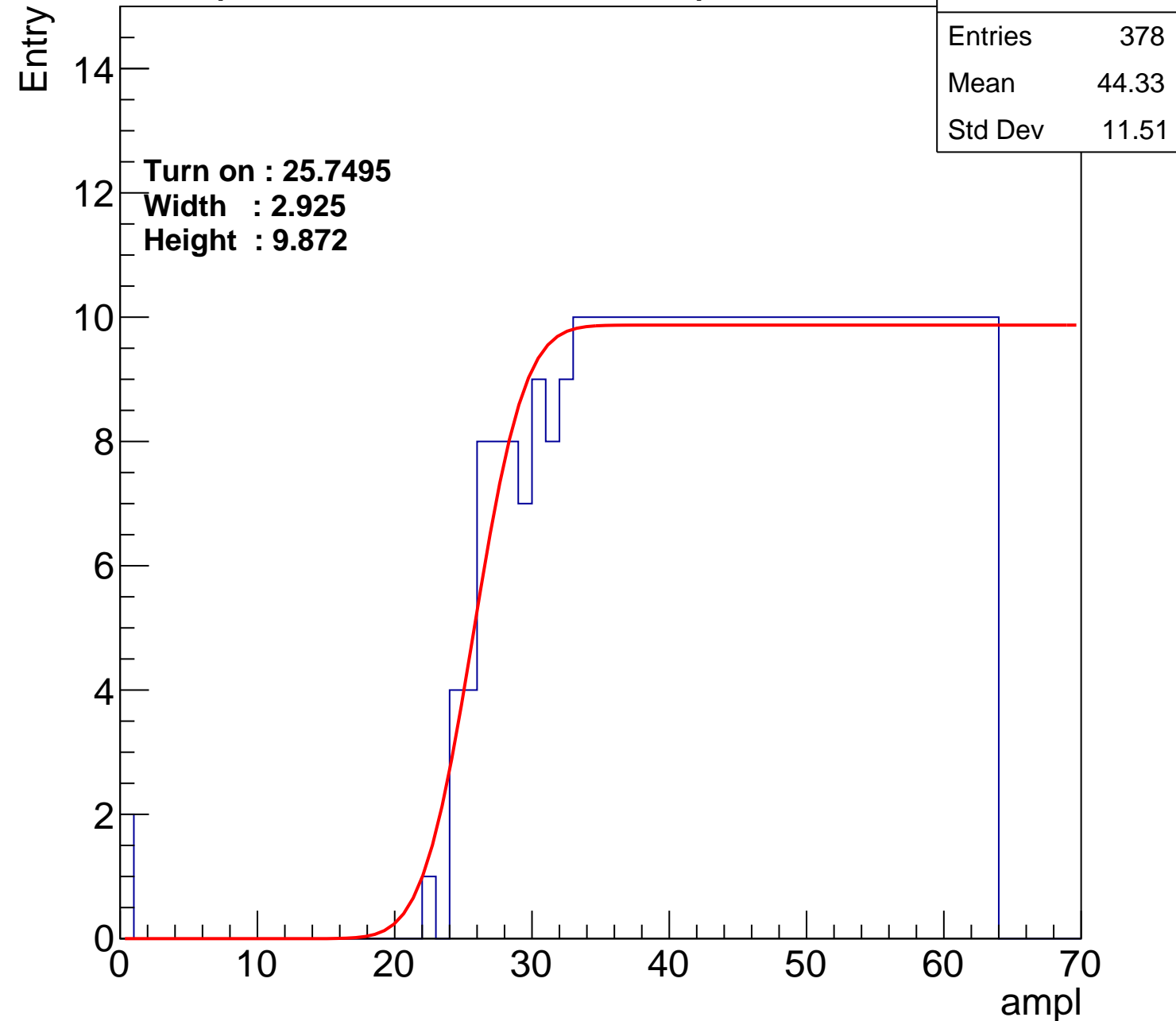
Width : 2.925

Height : 9.872

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch51

calib_packv5_042523_0143.root, FC#9, port A1

Entries	353
Mean	45.65
Std Dev	10.62

Turn on : 29.3441

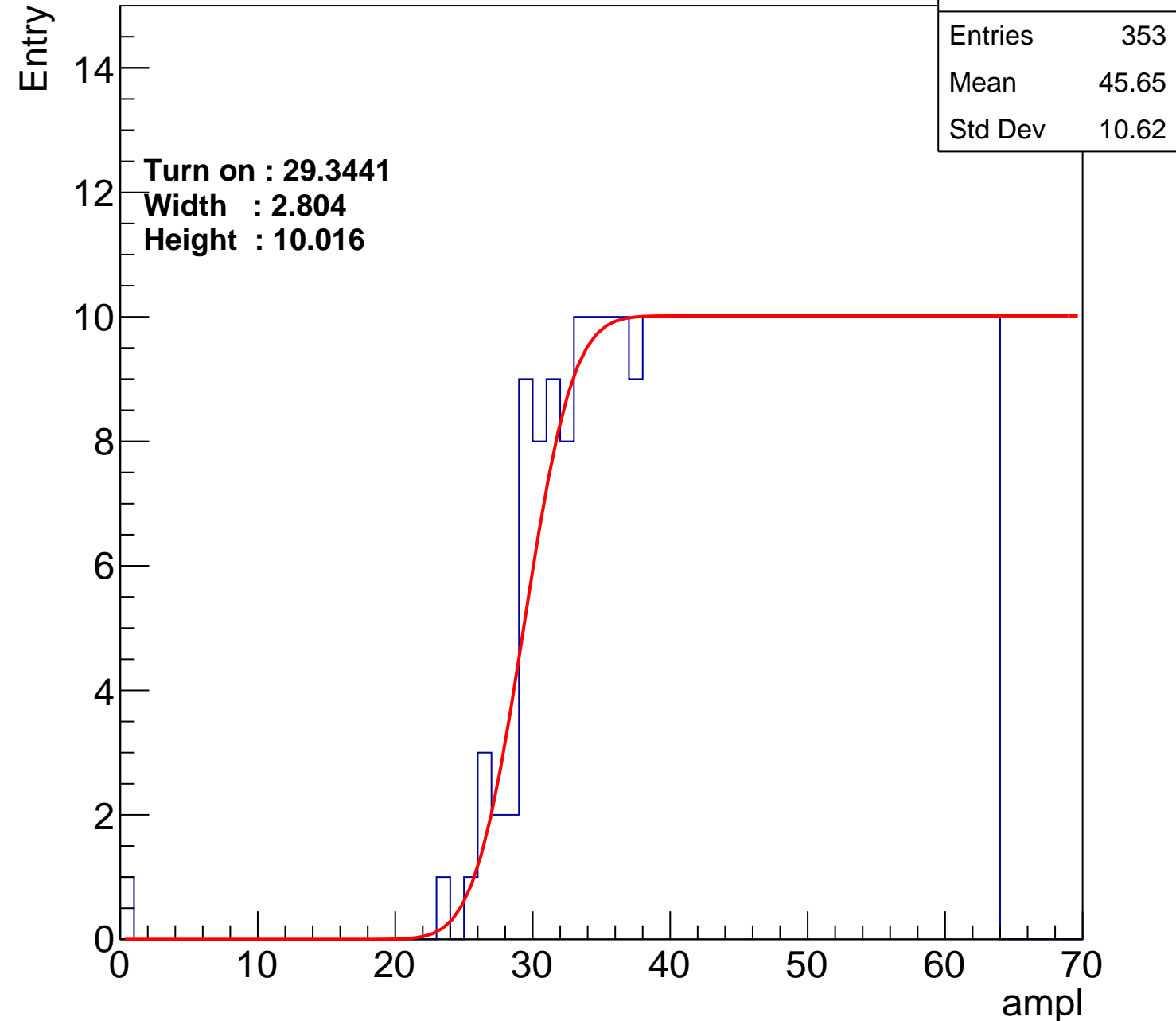
Width : 2.804

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch52

calib_packv5_042523_0143.root, FC#9, port A1

Entries	364
Mean	44.93
Std Dev	11.39

Turn on : 28.7462

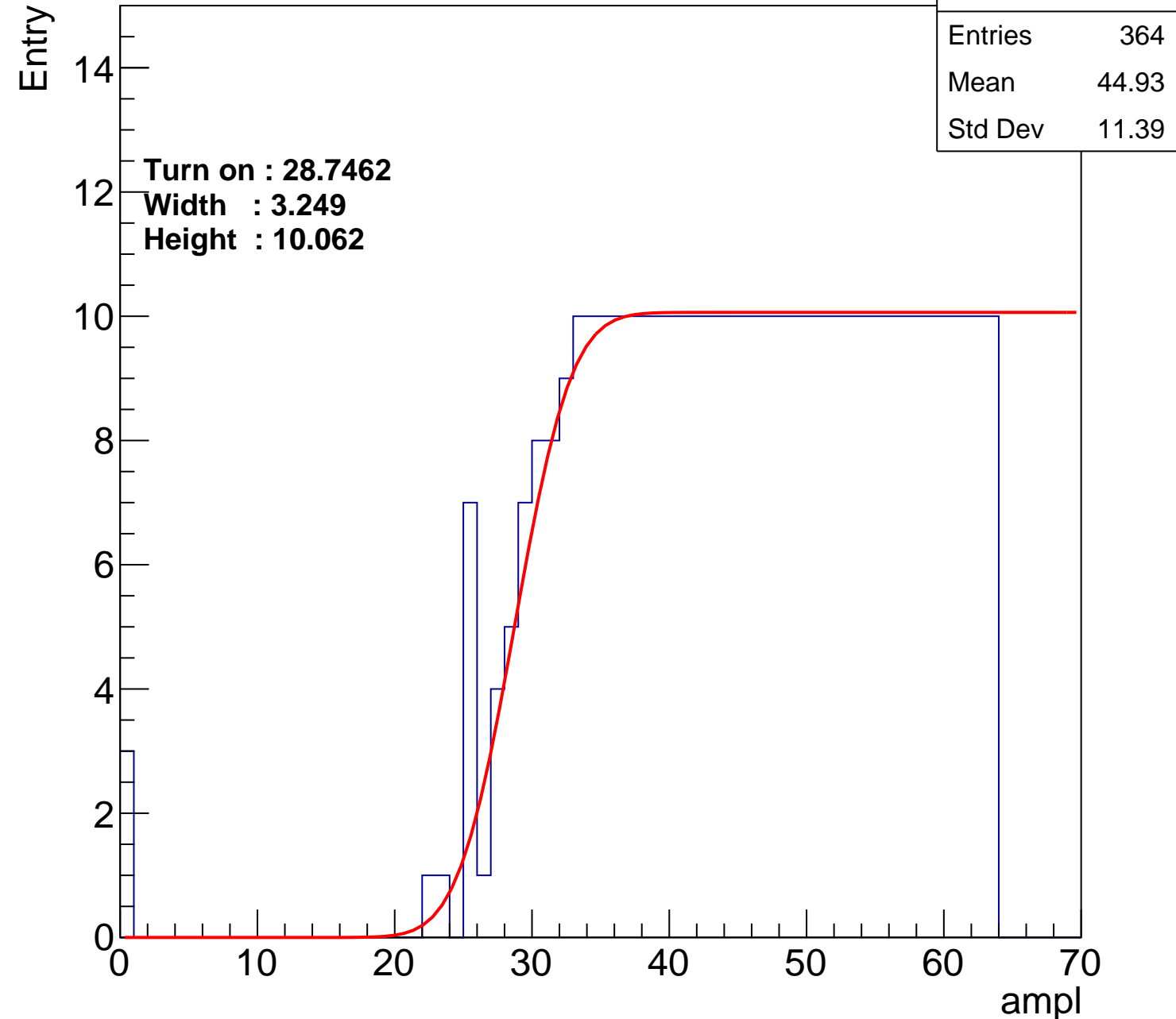
Width : 3.249

Height : 10.062

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch53

calib_packv5_042523_0143.root, FC#9, port A1

Entries	383
Mean	43.96
Std Dev	11.98

Turn on : 26.2905

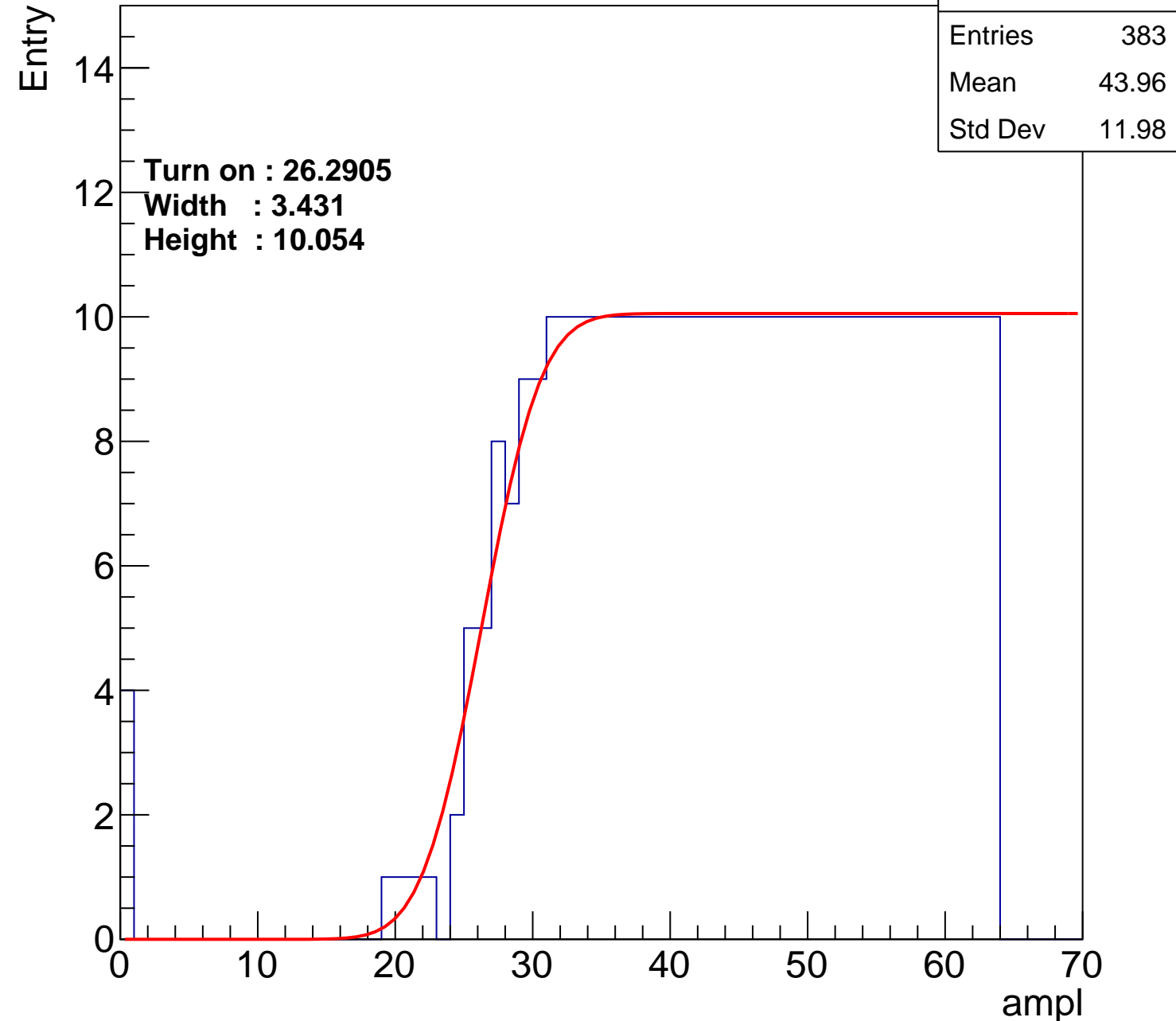
Width : 3.431

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch54

calib_packv5_042523_0143.root, FC#9, port A1

Entries	370
Mean	44.55
Std Dev	11.74

Turn on : 27.5957

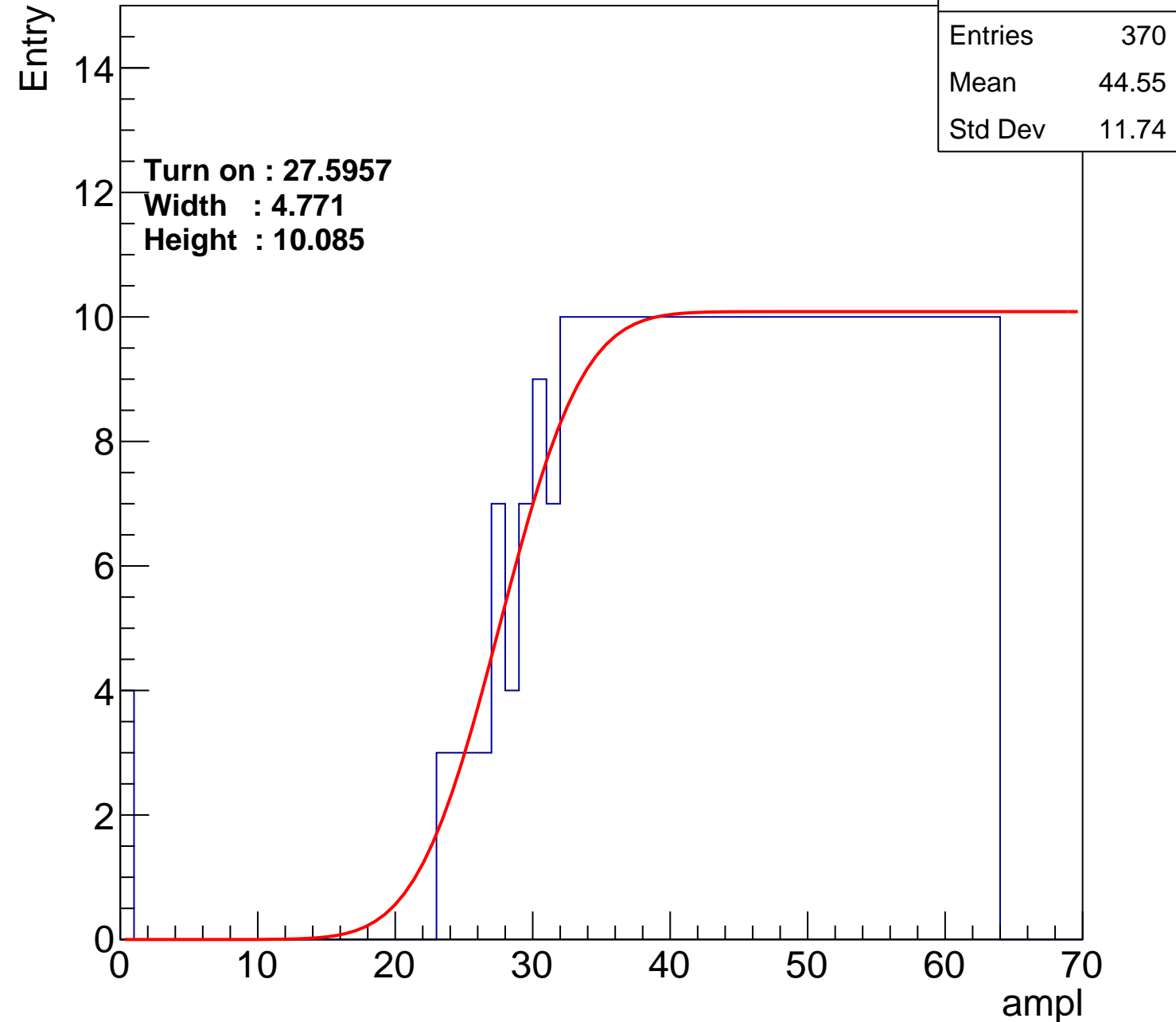
Width : 4.771

Height : 10.085

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch55

calib_packv5_042523_0143.root, FC#9, port A1

Entries	385
Mean	43.74
Std Dev	12.28

Turn on : 26.3136

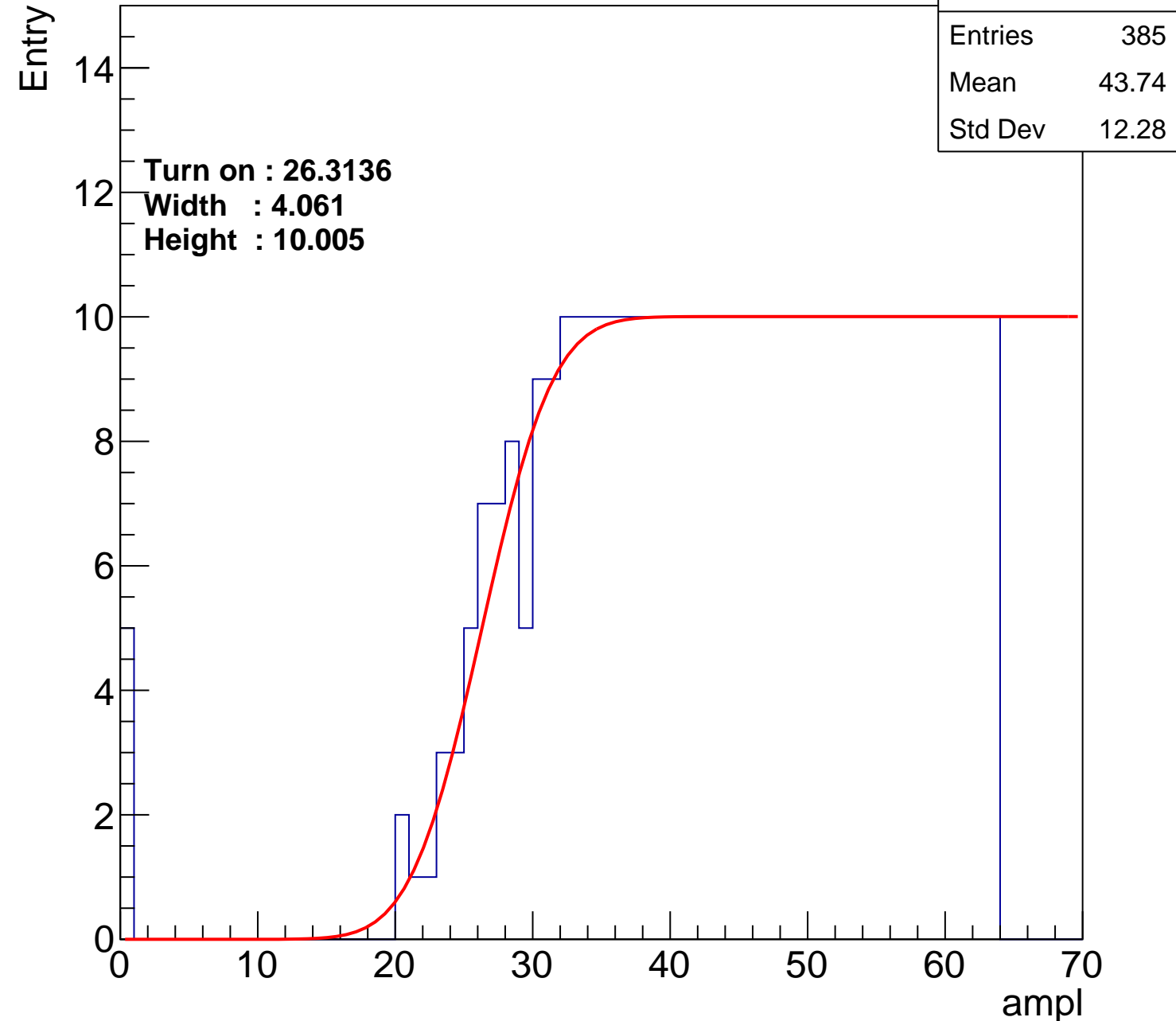
Width : 4.061

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch56

calib_packv5_042523_0143.root, FC#9, port A1

Entries	380
Mean	44.21
Std Dev	11.67

Turn on : 26.3997

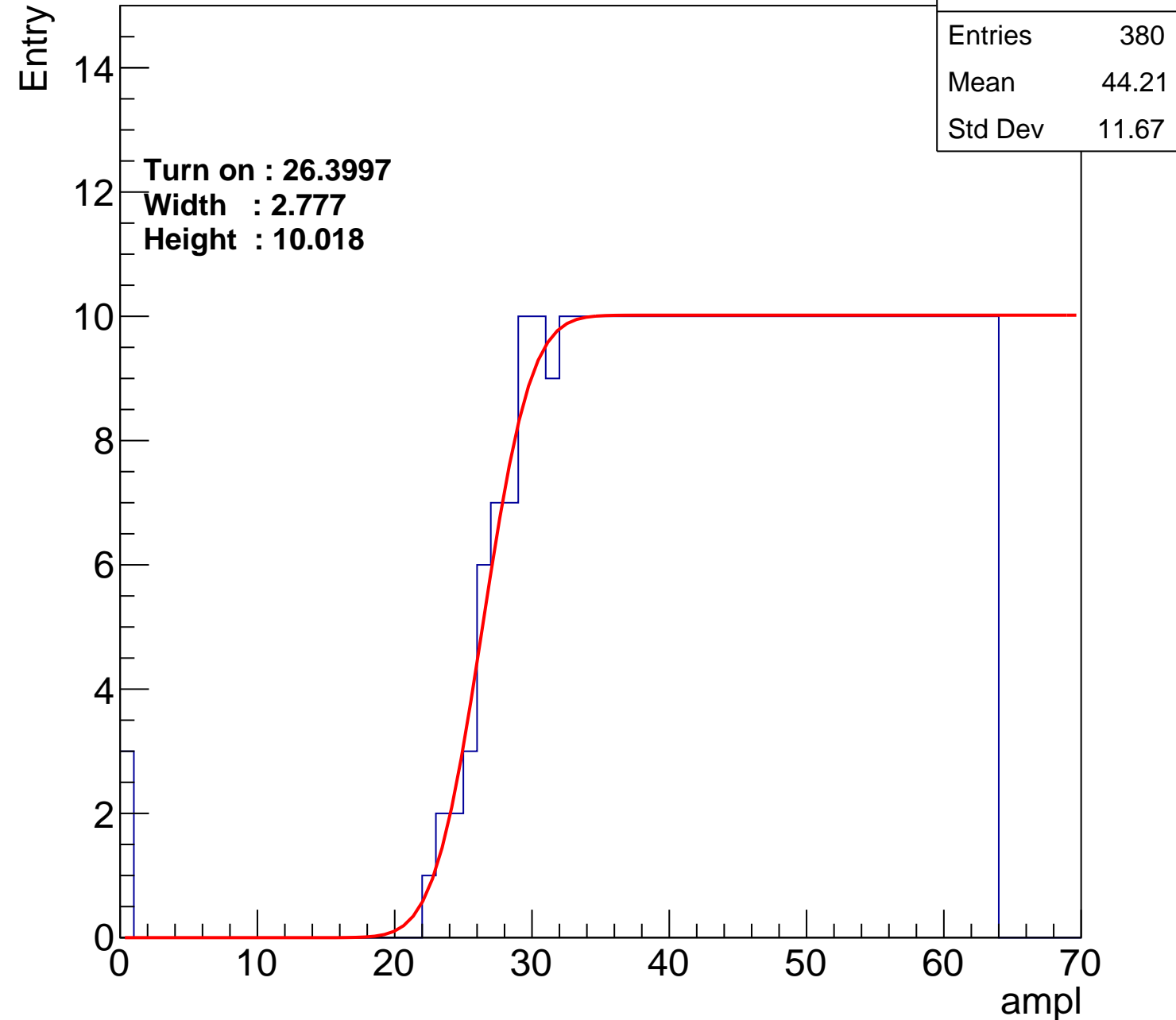
Width : 2.777

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch57

calib_packv5_042523_0143.root, FC#9, port A1

Entries	357
Mean	45.46
Std Dev	10.73

Turn on : 28.4601

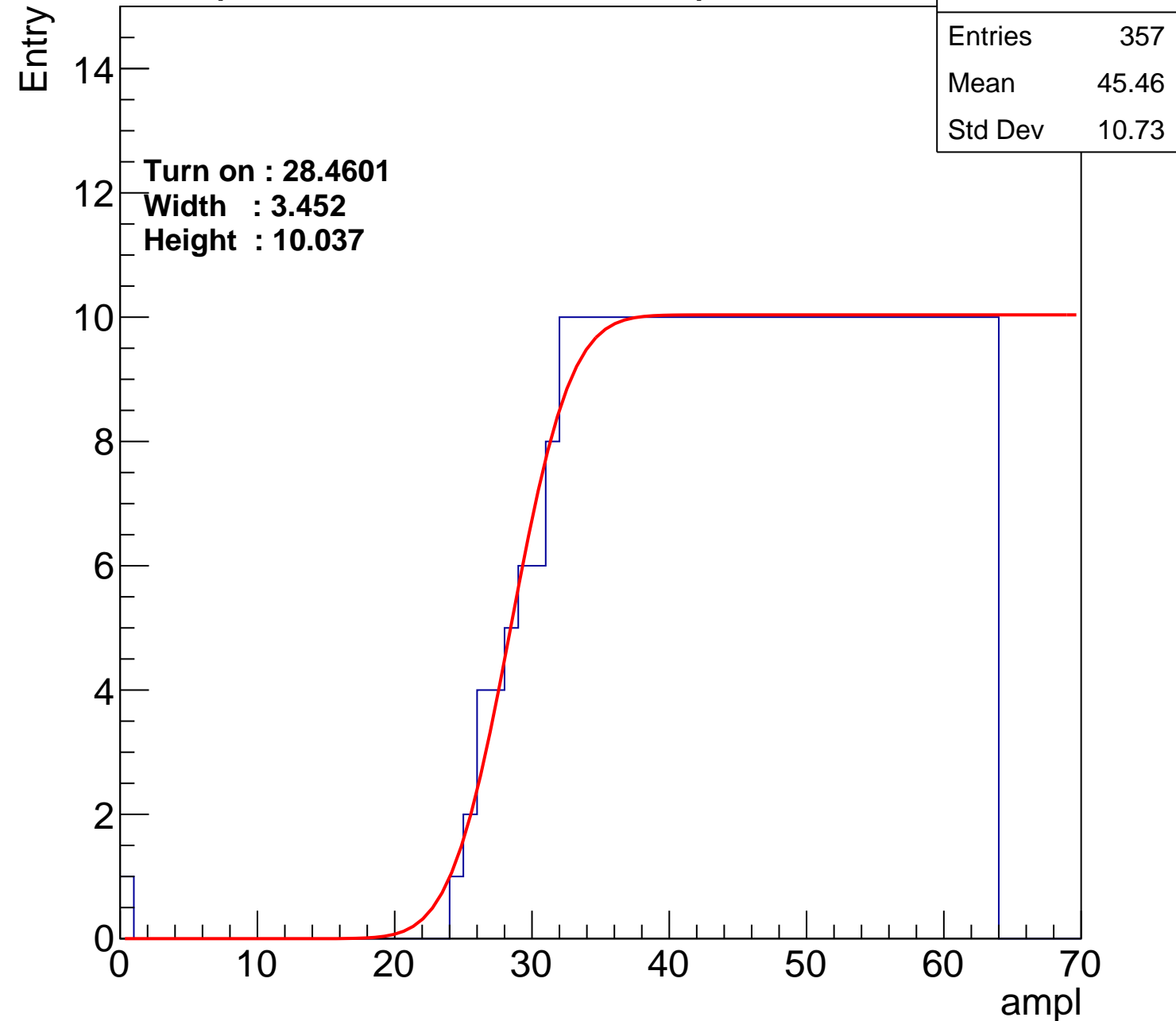
Width : 3.452

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch58

calib_packv5_042523_0143.root, FC#9, port A1

Entries	368
Mean	44.62
Std Dev	11.74

Turn on : 27.7990

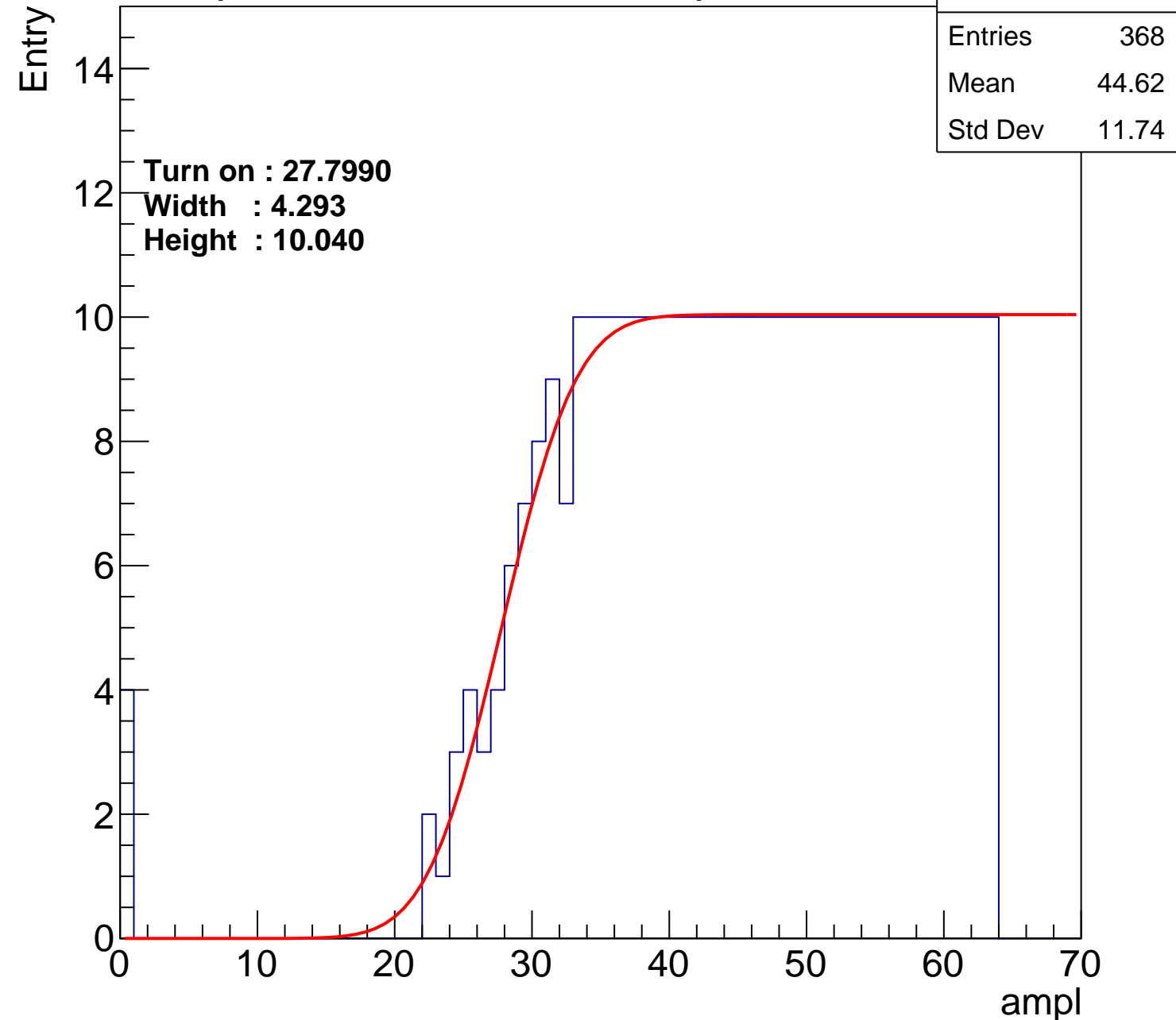
Width : 4.293

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch59

calib_packv5_042523_0143.root, FC#9, port A1

Entries	359
Mean	45.21
Std Dev	11.21

Turn on : 28.1601

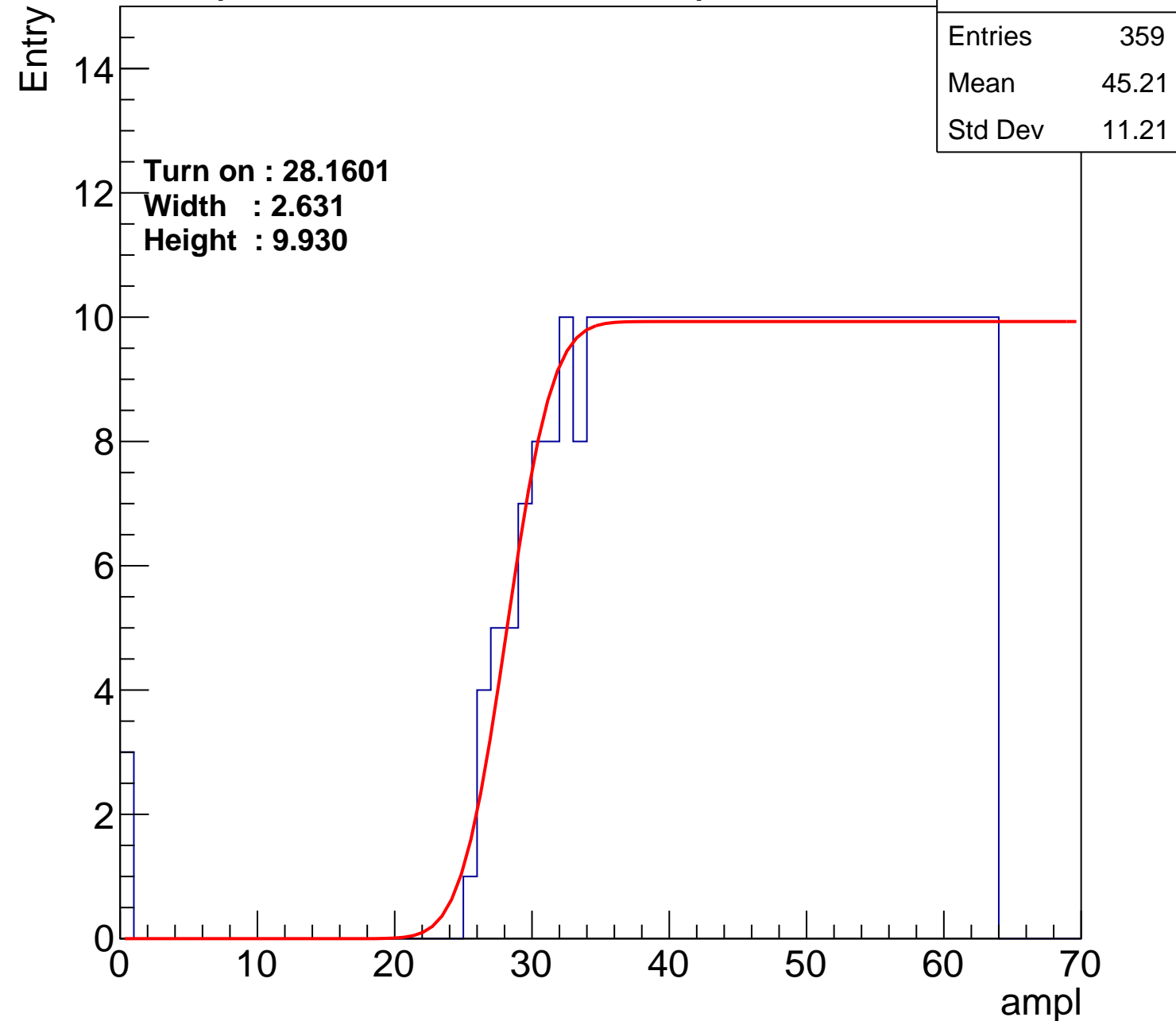
Width : 2.631

Height : 9.930

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch60

calib_packv5_042523_0143.root, FC#9, port A1

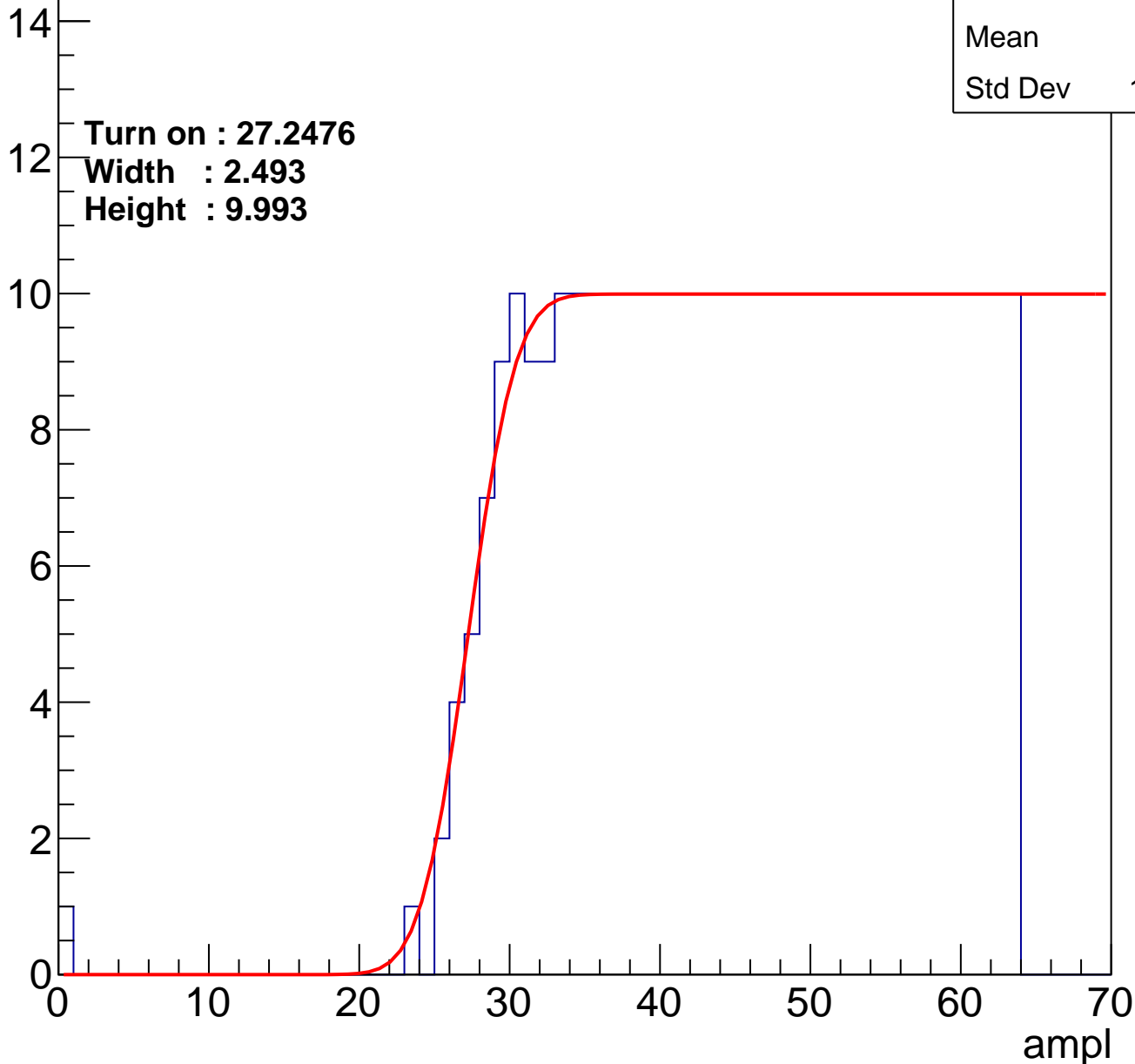
Entry

Entries	367
Mean	45
Std Dev	10.93

Turn on : 27.2476

Width : 2.493

Height : 9.993



B0L001S, U1-ch61

calib_packv5_042523_0143.root, FC#9, port A1

Entries	372
Mean	44.68
Std Dev	11.28

Turn on : 27.2738

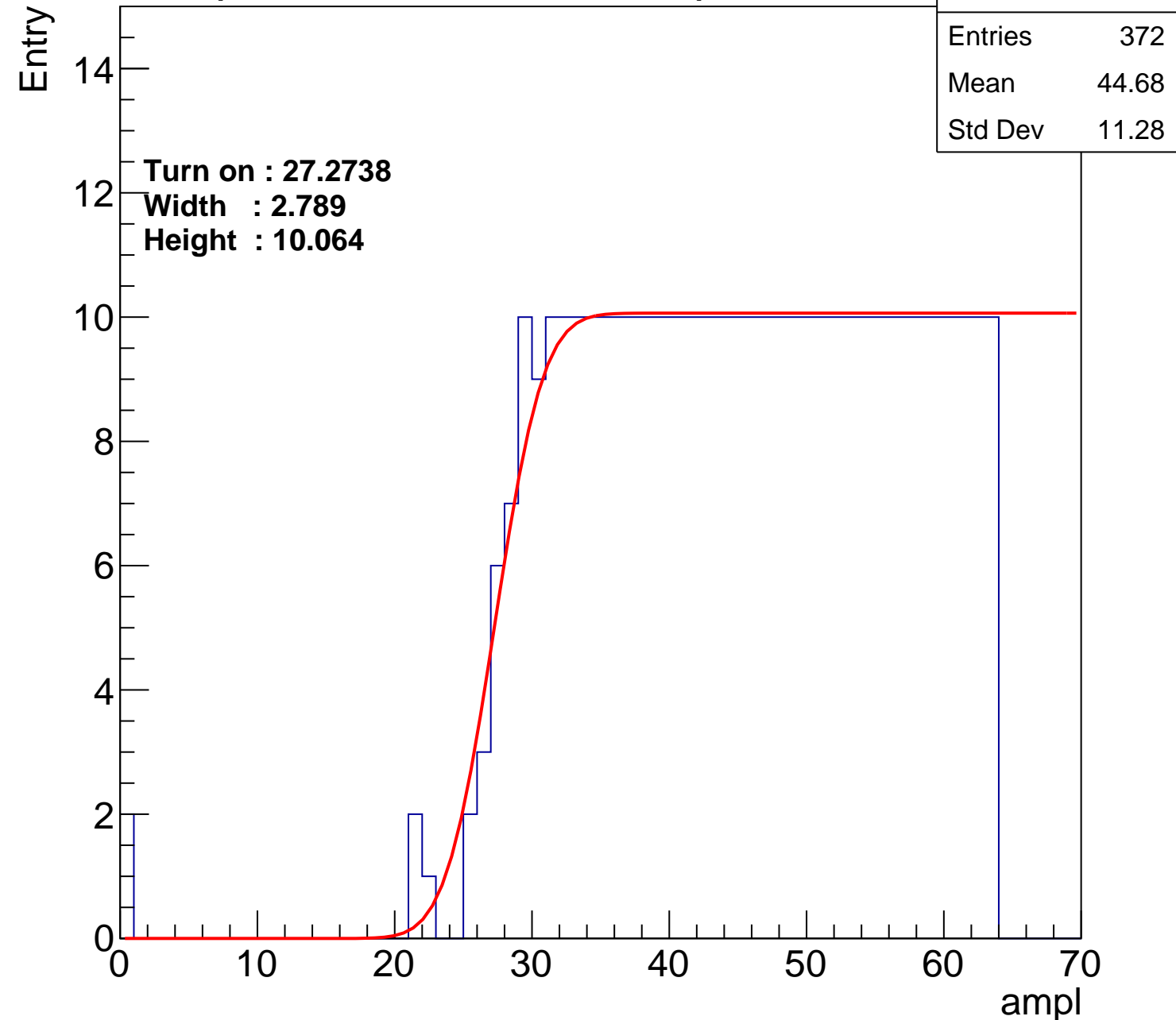
Width : 2.789

Height : 10.064

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch62

calib_packv5_042523_0143.root, FC#9, port A1

Entries	377
Mean	44.52
Std Dev	11.18

Turn on : 26.1136

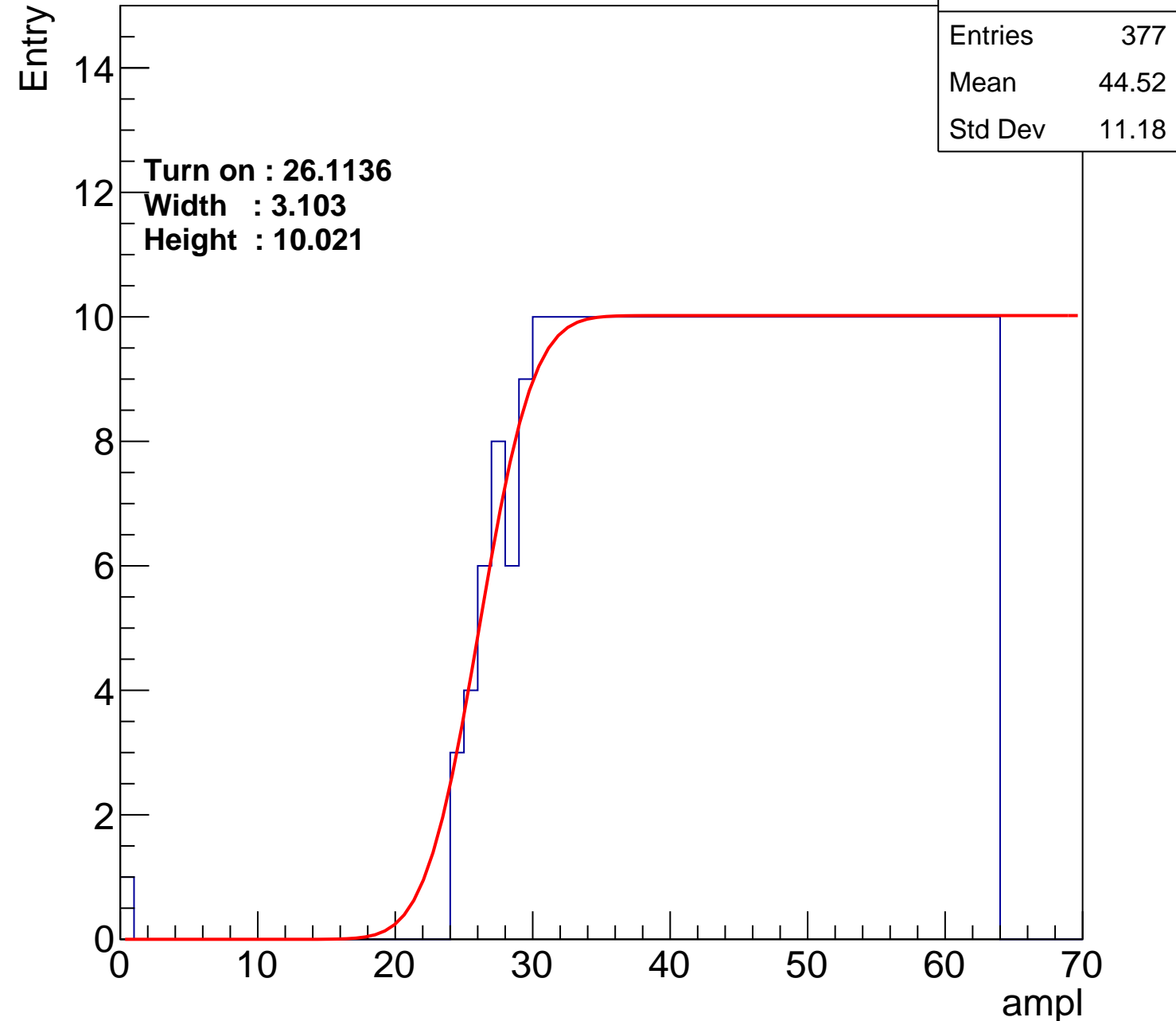
Width : 3.103

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch63

calib_packv5_042523_0143.root, FC#9, port A1

Entries	349
Mean	45.84
Std Dev	10.54

Turn on : 29.4121

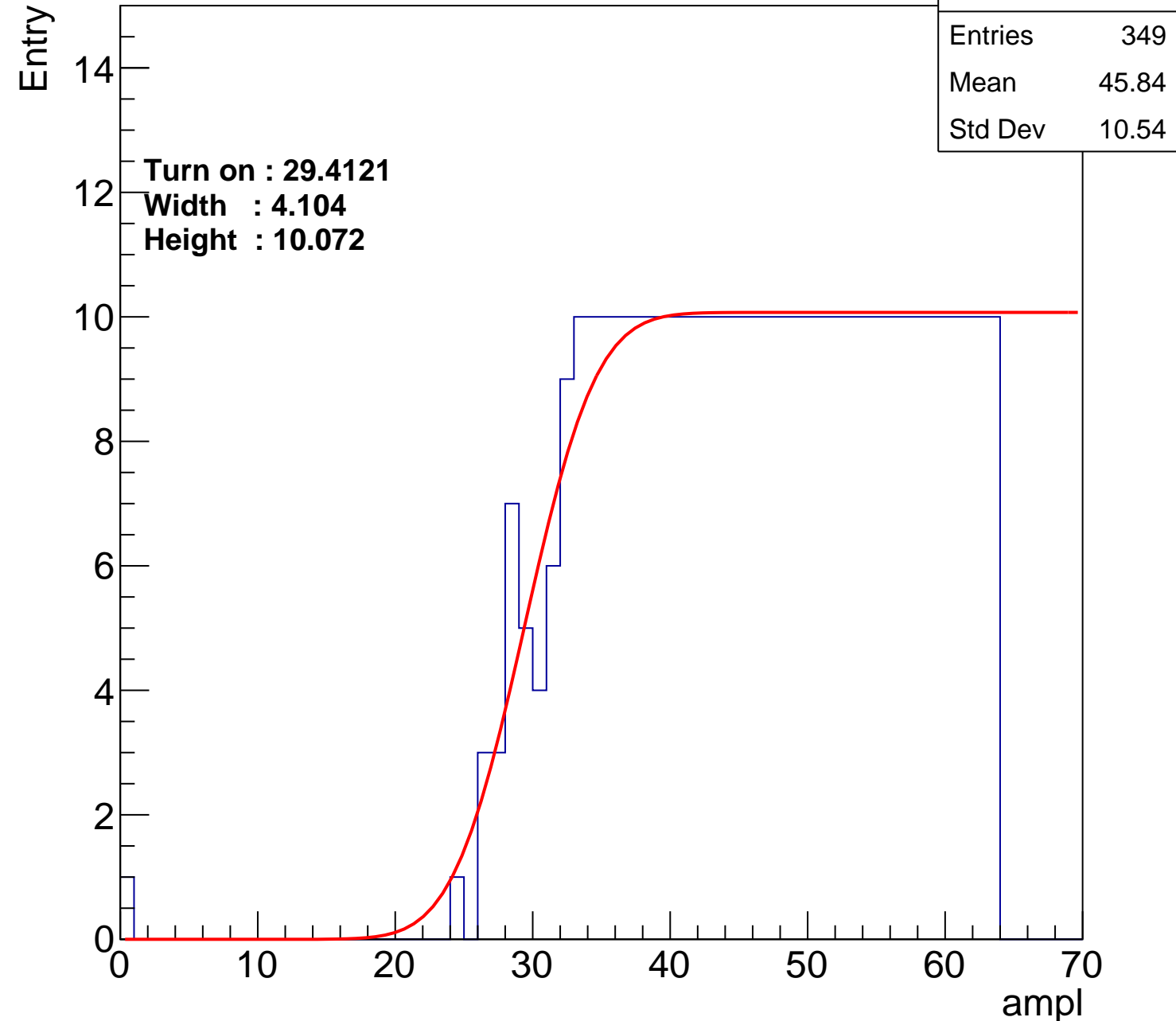
Width : 4.104

Height : 10.072

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch64

calib_packv5_042523_0143.root, FC#9, port A1

Entries	369
Mean	44.61
Std Dev	11.69

Turn on : 27.8400

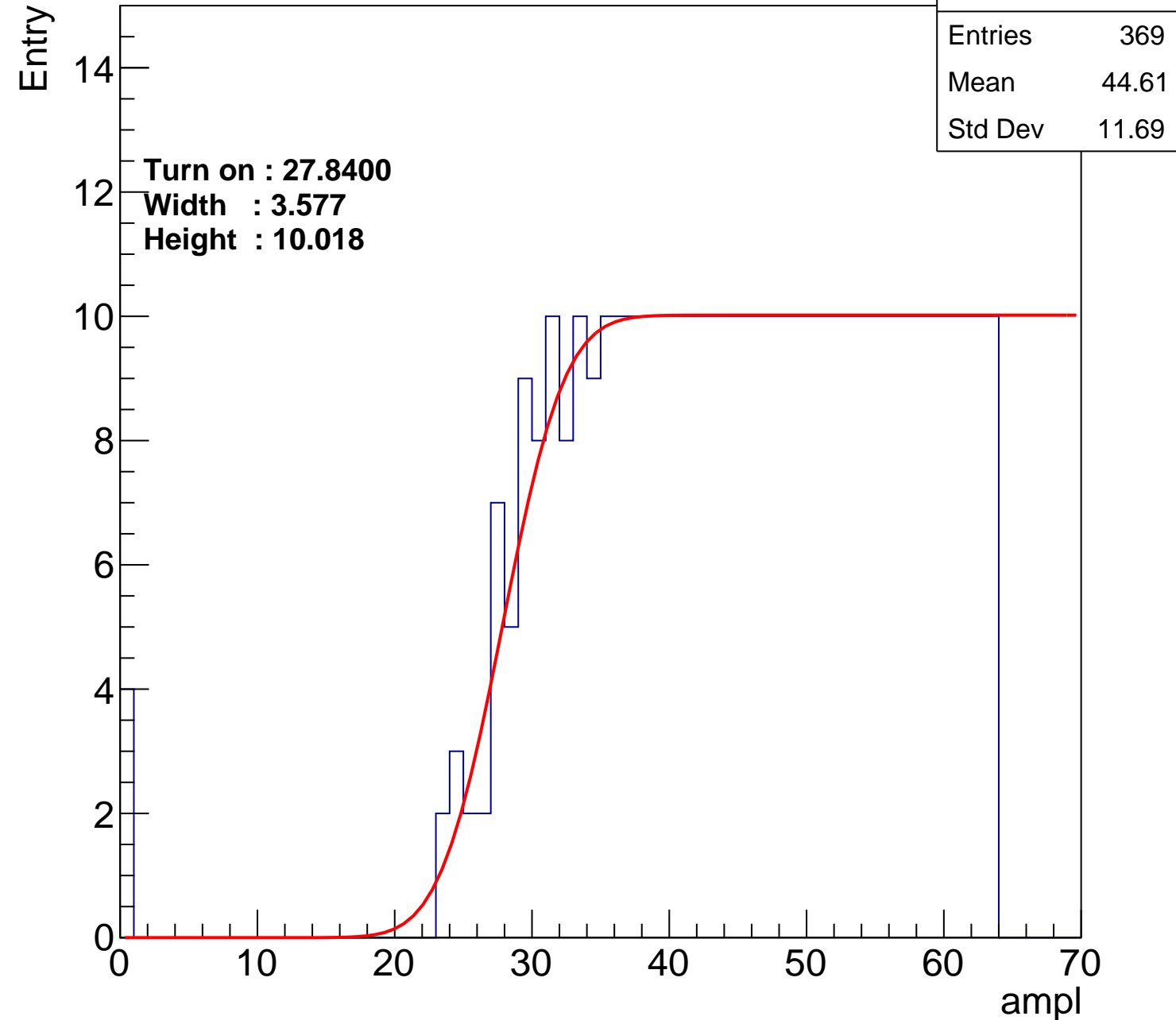
Width : 3.577

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch65

calib_packv5_042523_0143.root, FC#9, port A1

Entries	377
Mean	44.49
Std Dev	11.23

Turn on : 26.2922

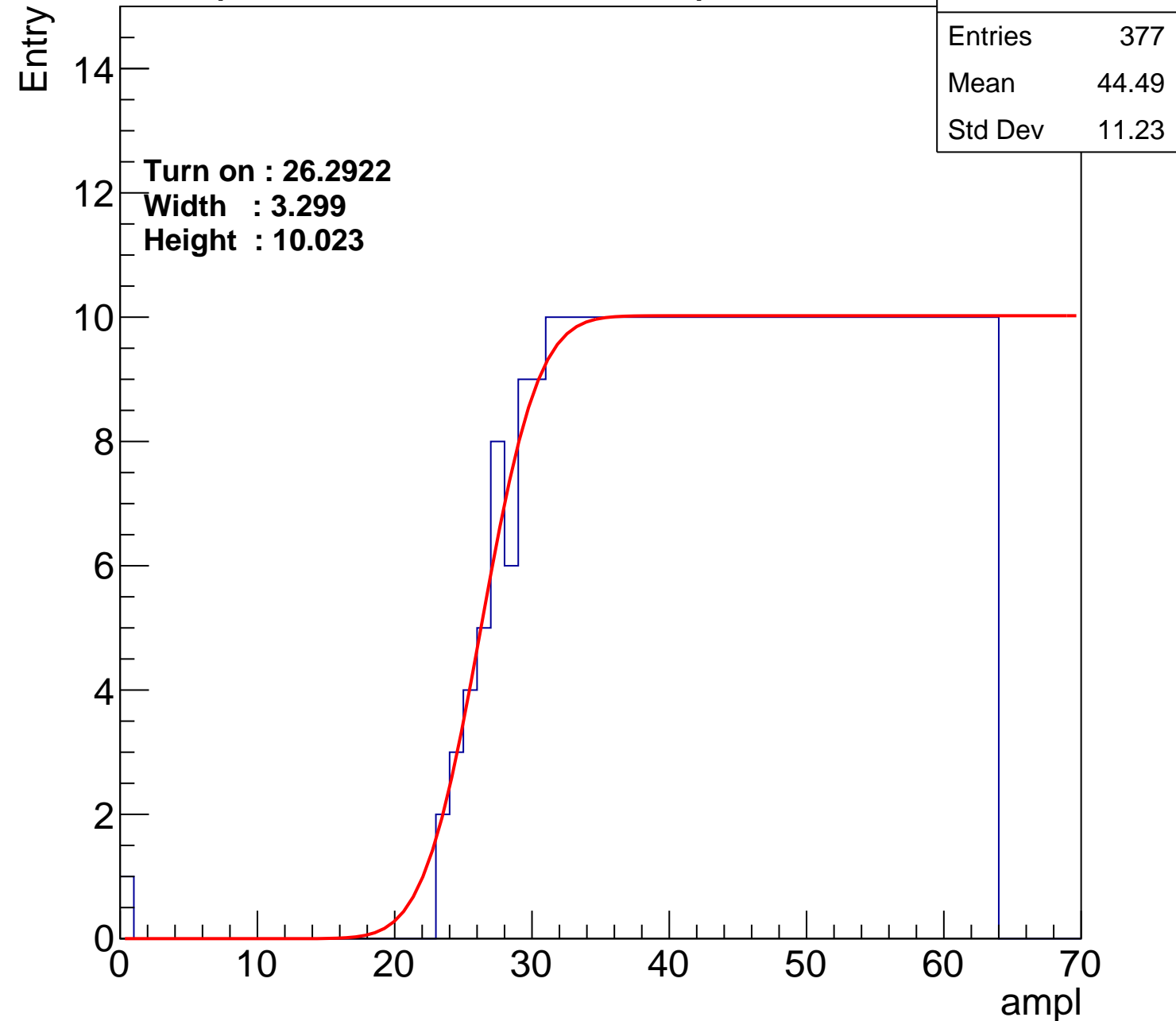
Width : 3.299

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch66

calib_packv5_042523_0143.root, FC#9, port A1

Entries	382
Mean	44.13
Std Dev	11.7

Turn on : 26.1684

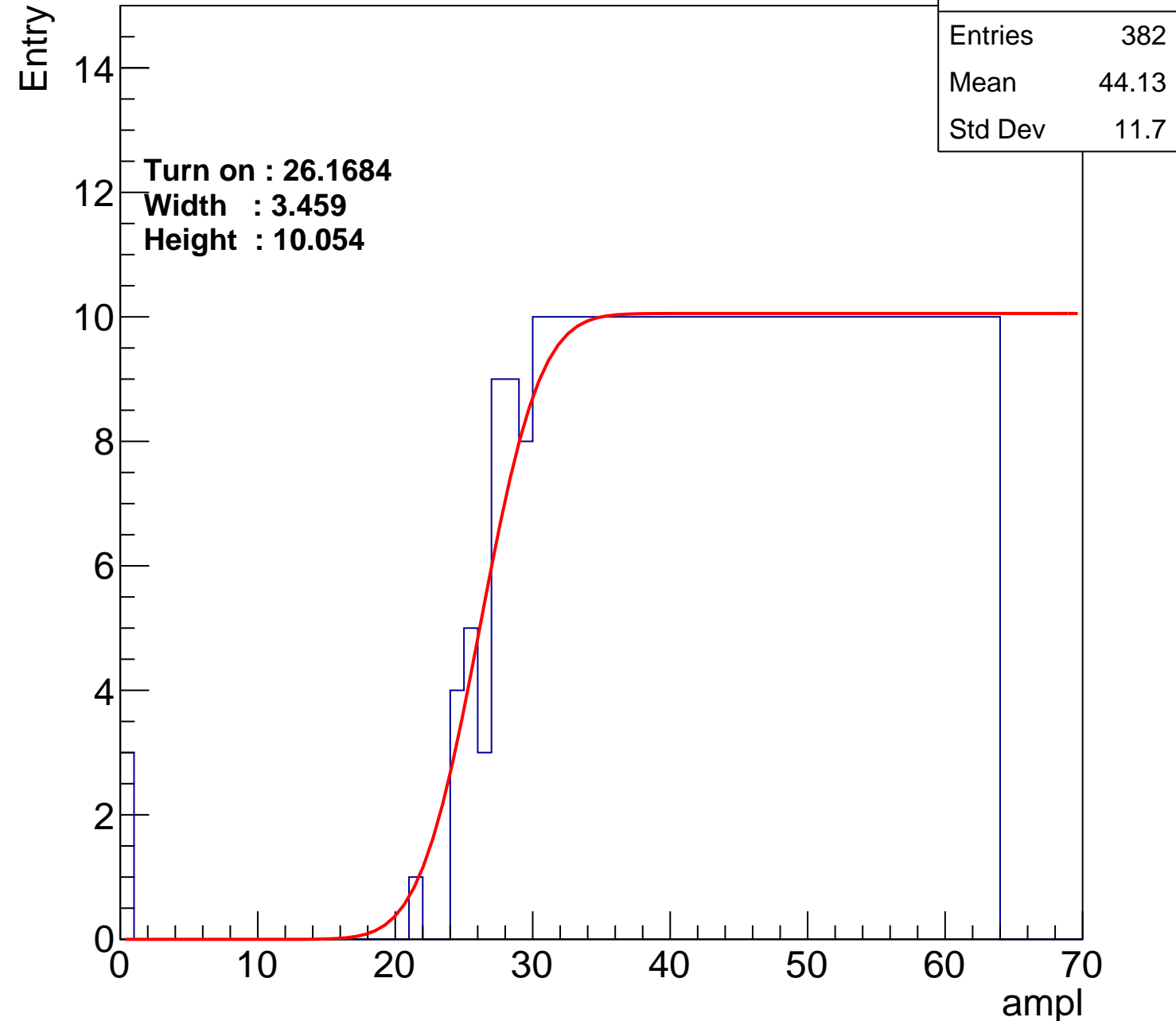
Width : 3.459

Height : 10.054

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch67

calib_packv5_042523_0143.root, FC#9, port A1

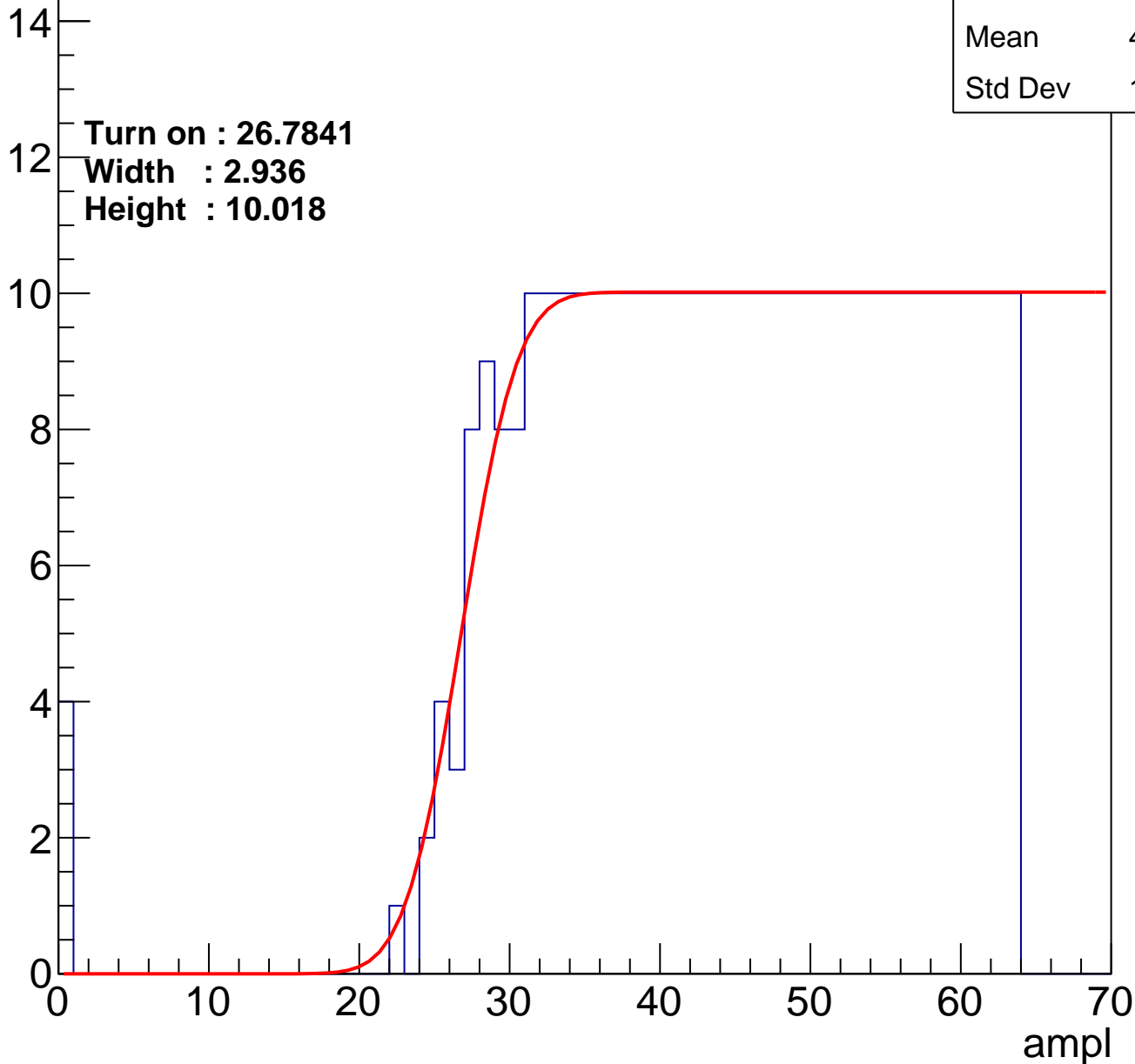
Entry

Entries	377
Mean	44.29
Std Dev	11.78

Turn on : 26.7841

Width : 2.936

Height : 10.018



B0L001S, U1-ch68

calib_packv5_042523_0143.root, FC#9, port A1

Entries	370
Mean	44.73
Std Dev	11.3

Turn on : 27.7567

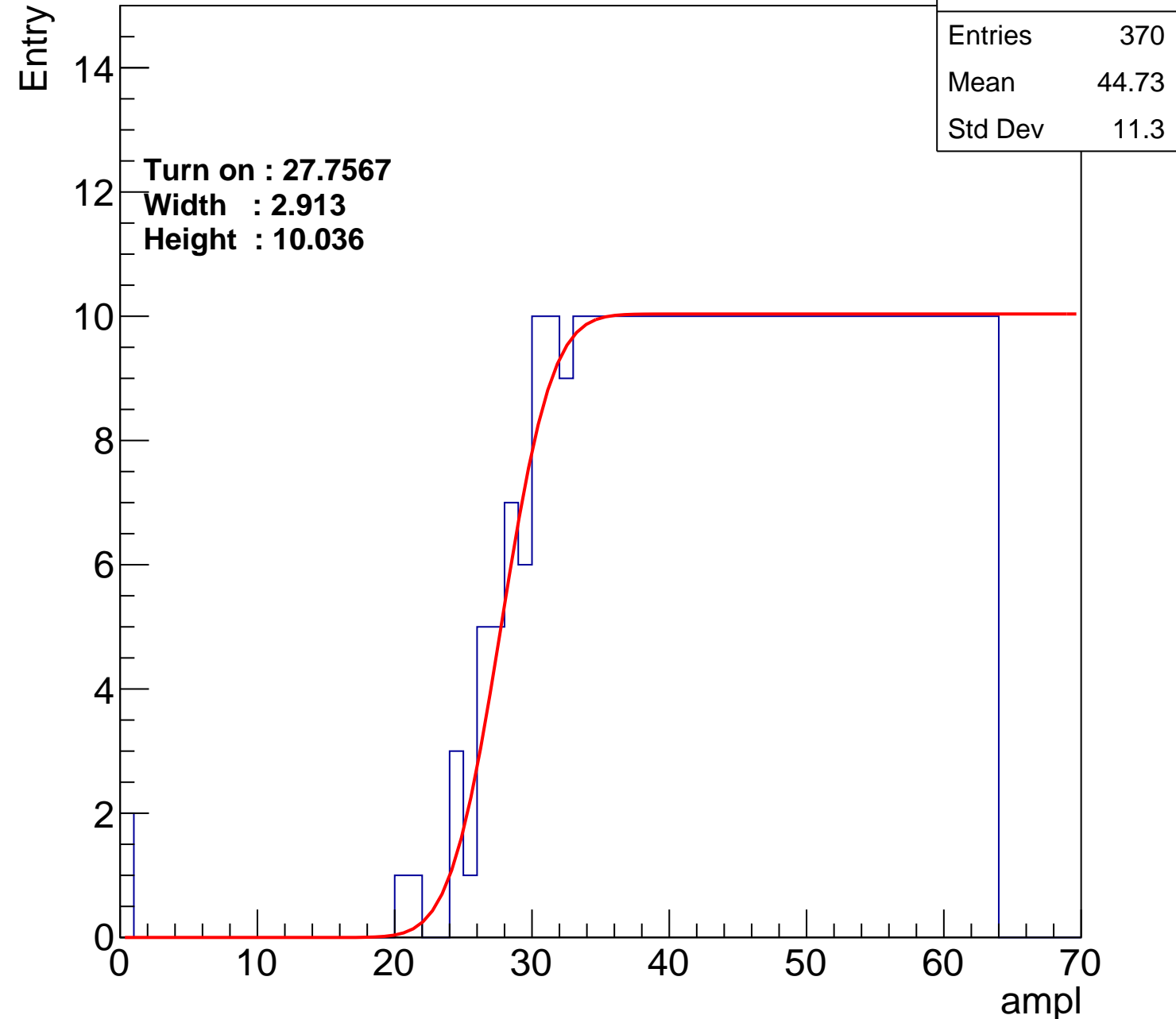
Width : 2.913

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch69

calib_packv5_042523_0143.root, FC#9, port A1

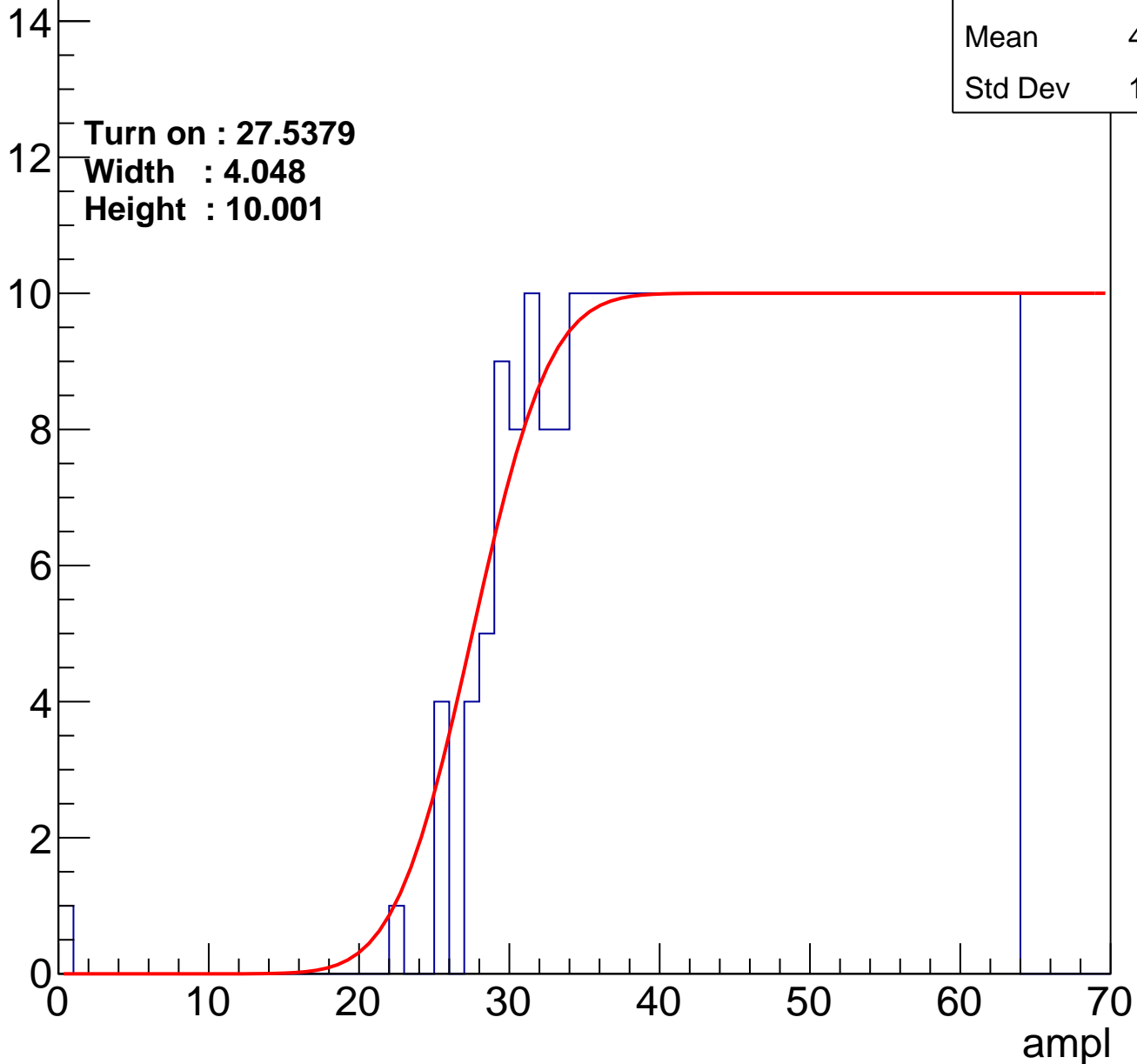
Entry

Entries	358
Mean	45.39
Std Dev	10.77

Turn on : 27.5379

Width : 4.048

Height : 10.001



B0L001S, U1-ch70

calib_packv5_042523_0143.root, FC#9, port A1

Entries	369
Mean	44.62
Std Dev	11.68

Turn on : 27.5459

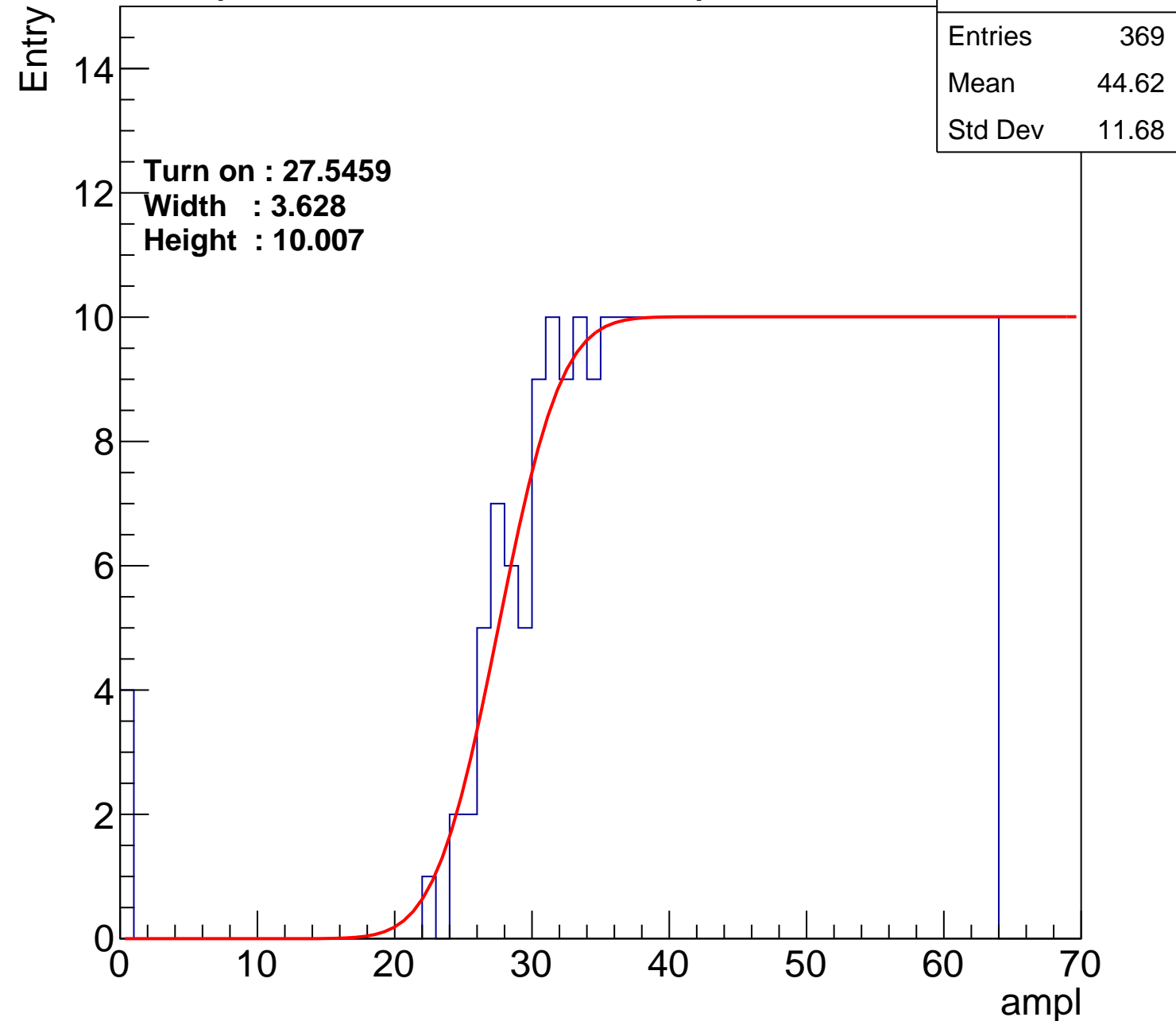
Width : 3.628

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch71

calib_packv5_042523_0143.root, FC#9, port A1

Entries	349
Mean	45.87
Std Dev	10.49

Turn on : 29.5837

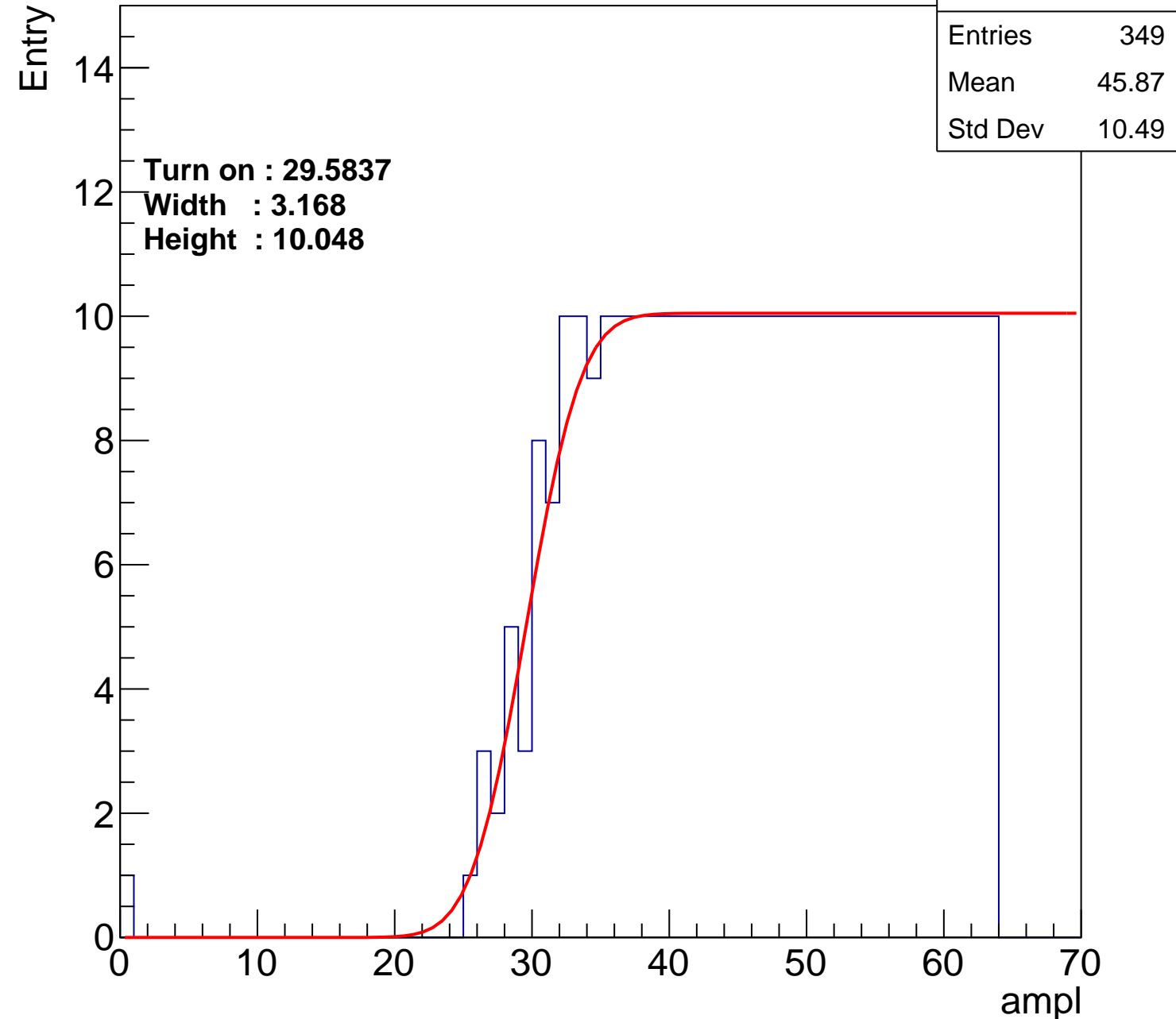
Width : 3.168

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch72

calib_packv5_042523_0143.root, FC#9, port A1

Entries	364
Mean	44.94
Std Dev	11.36

Turn on : 27.8517

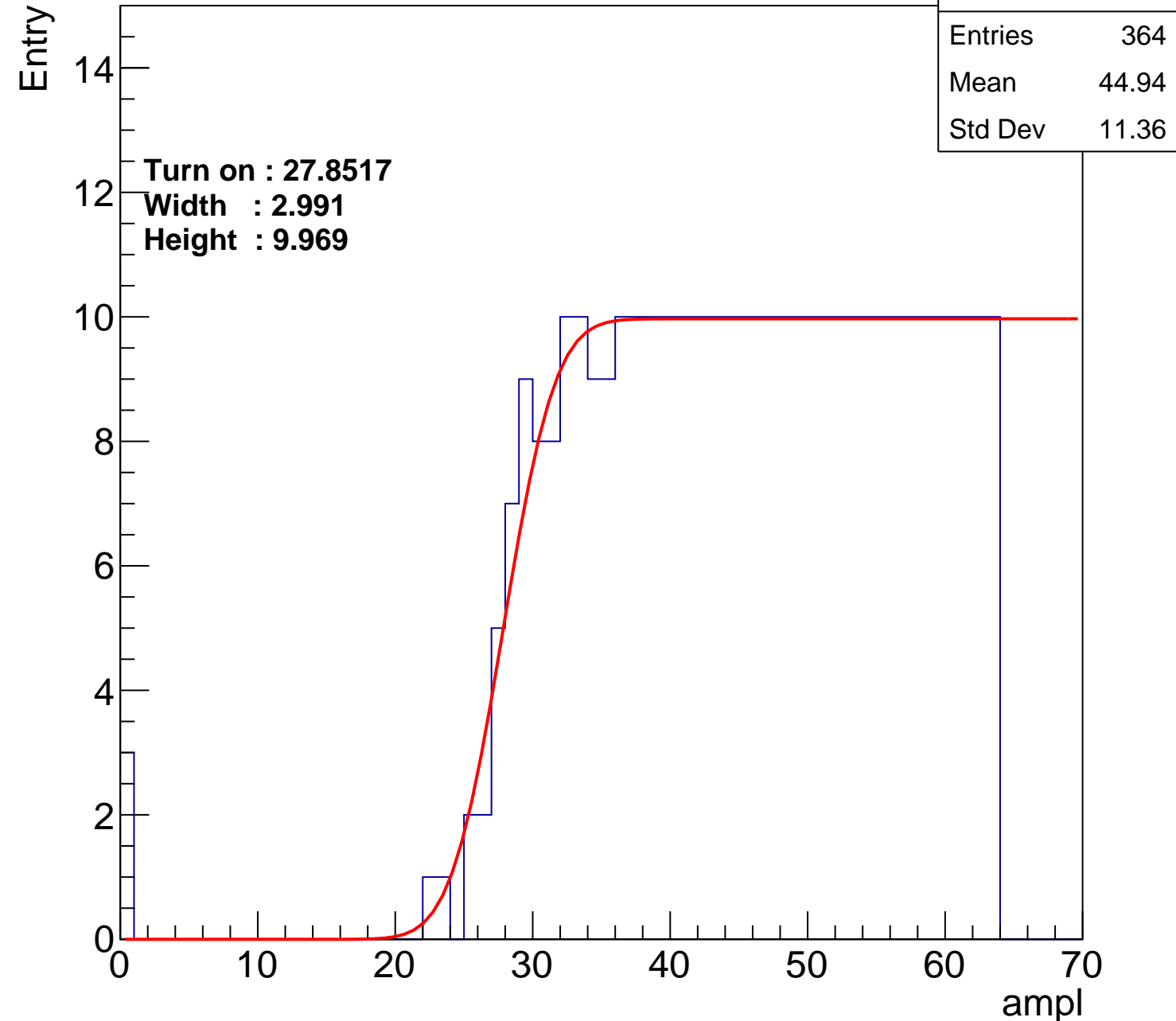
Width : 2.991

Height : 9.969

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch73

calib_packv5_042523_0143.root, FC#9, port A1

Entries	363
Mean	44.9
Std Dev	11.57

Turn on : 28.4069

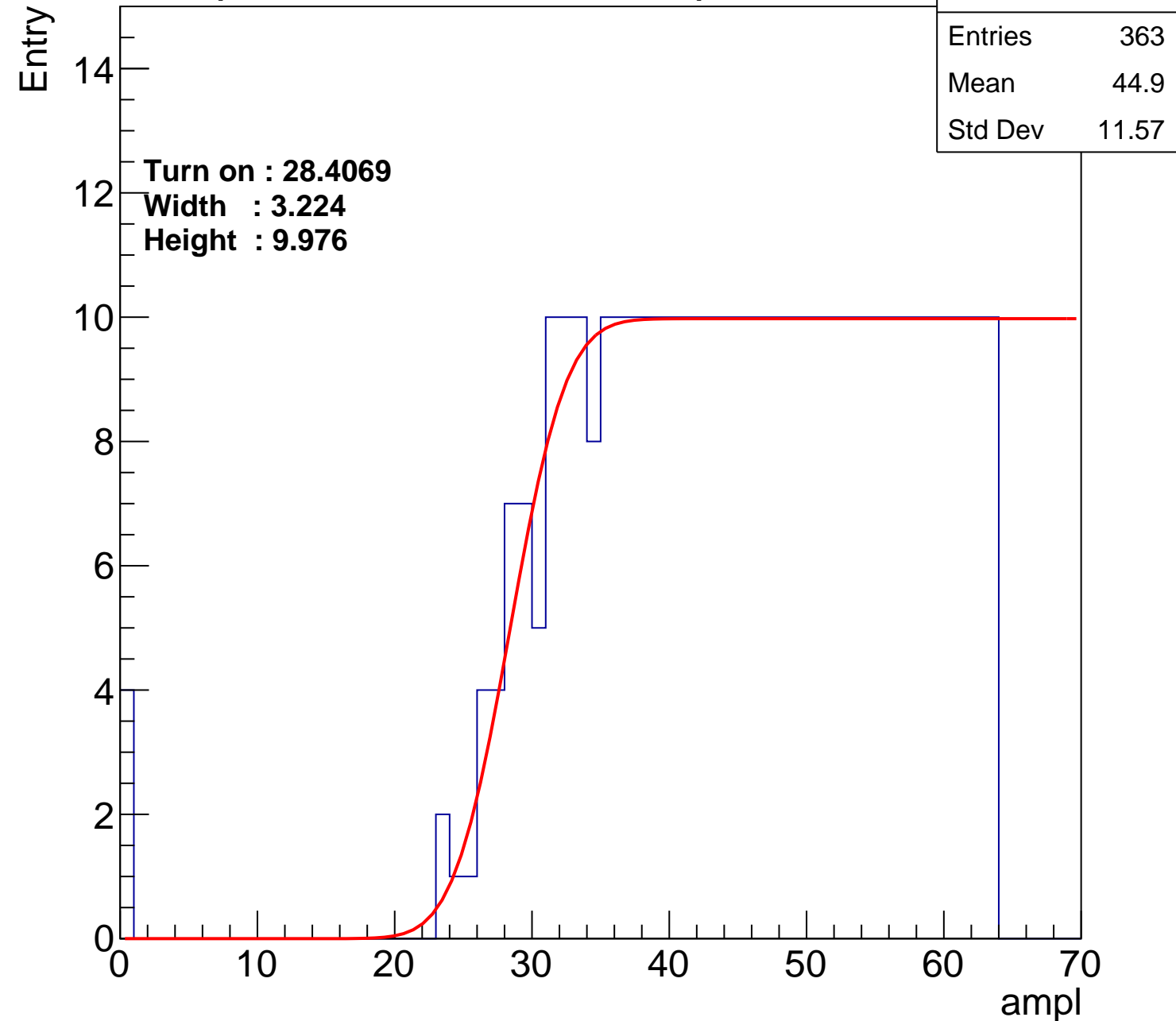
Width : 3.224

Height : 9.976

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch74

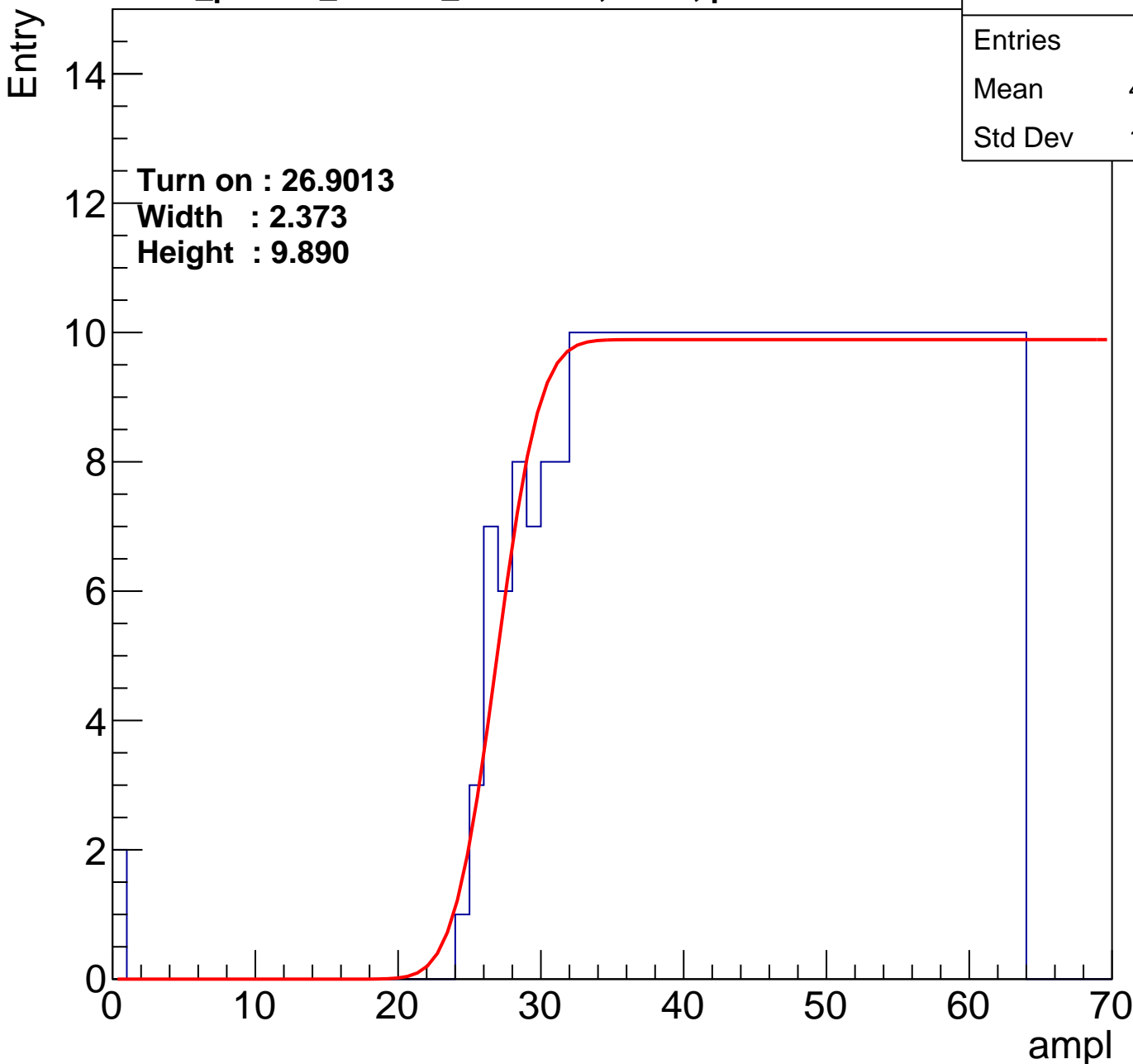
calib_packv5_042523_0143.root, FC#9, port A1

Entries	370
Mean	44.75
Std Dev	11.26

Turn on : 26.9013

Width : 2.373

Height : 9.890



B0L001S, U1-ch75

calib_packv5_042523_0143.root, FC#9, port A1

Entries	368
Mean	44.84
Std Dev	11.23

Turn on : 27.5669

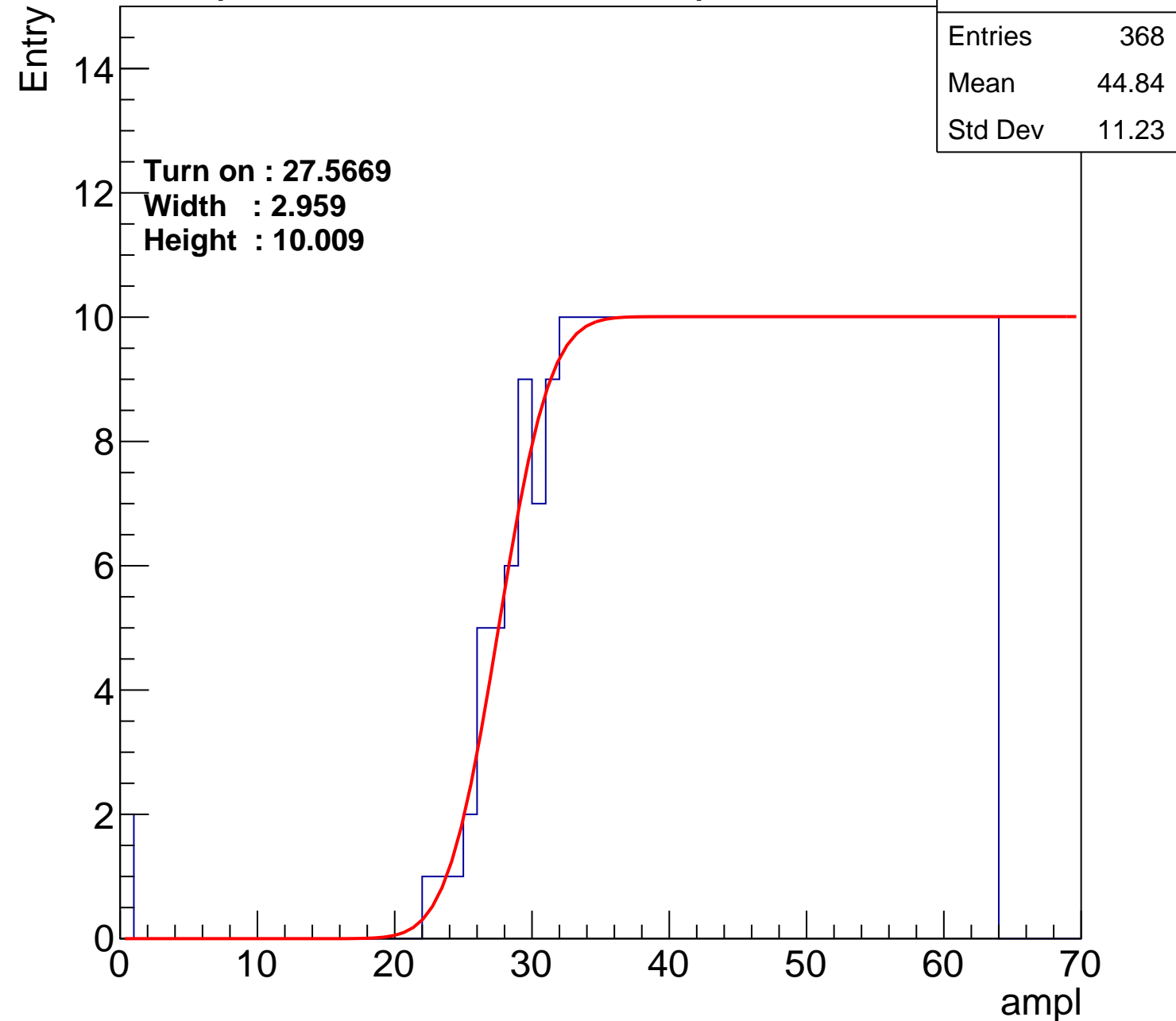
Width : 2.959

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch76

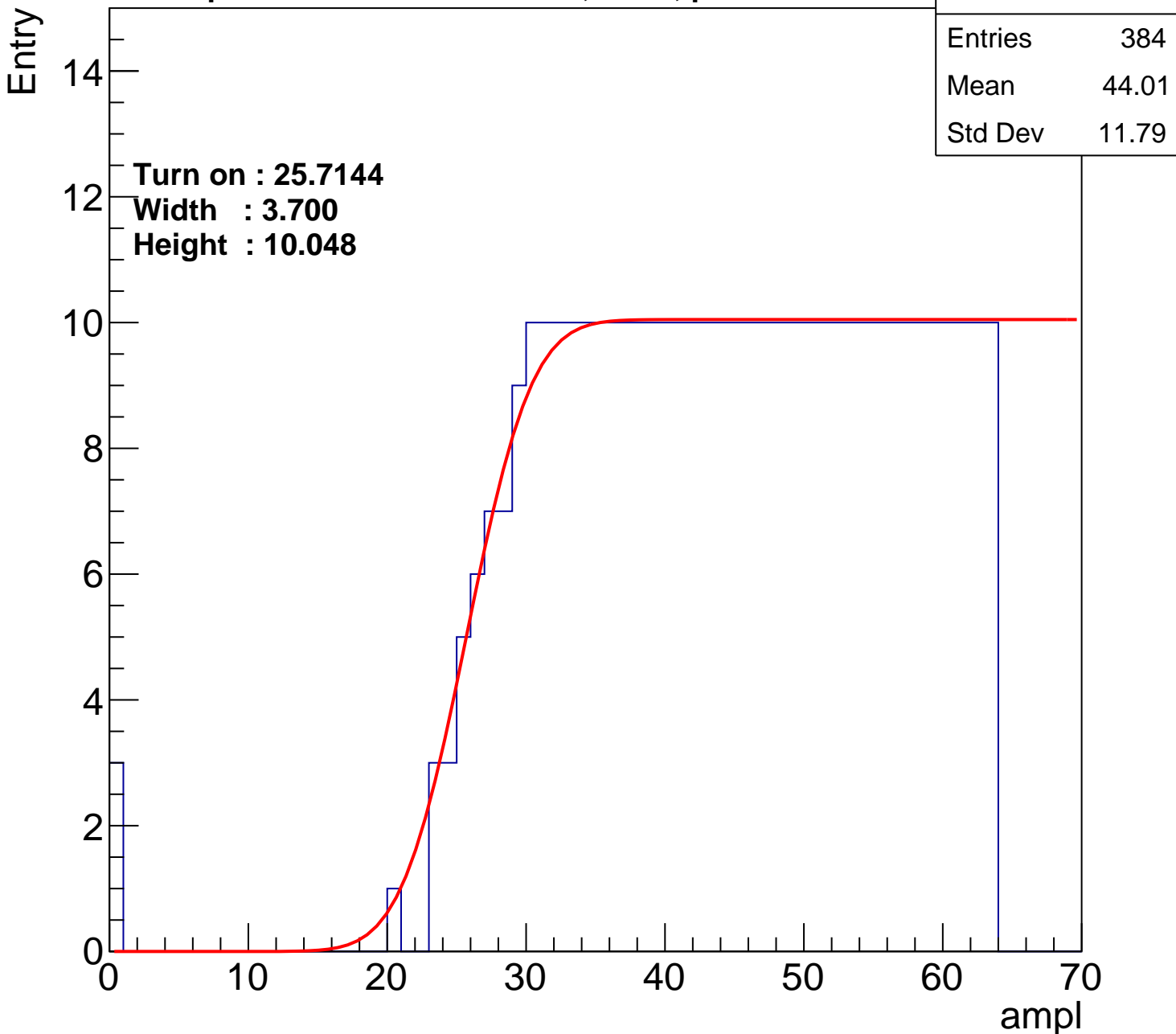
calib_packv5_042523_0143.root, FC#9, port A1

Entries	384
Mean	44.01
Std Dev	11.79

Turn on : 25.7144

Width : 3.700

Height : 10.048



B0L001S, U1-ch77

calib_packv5_042523_0143.root, FC#9, port A1

Entries	361
Mean	45.21
Std Dev	11.01

Turn on : 28.2670

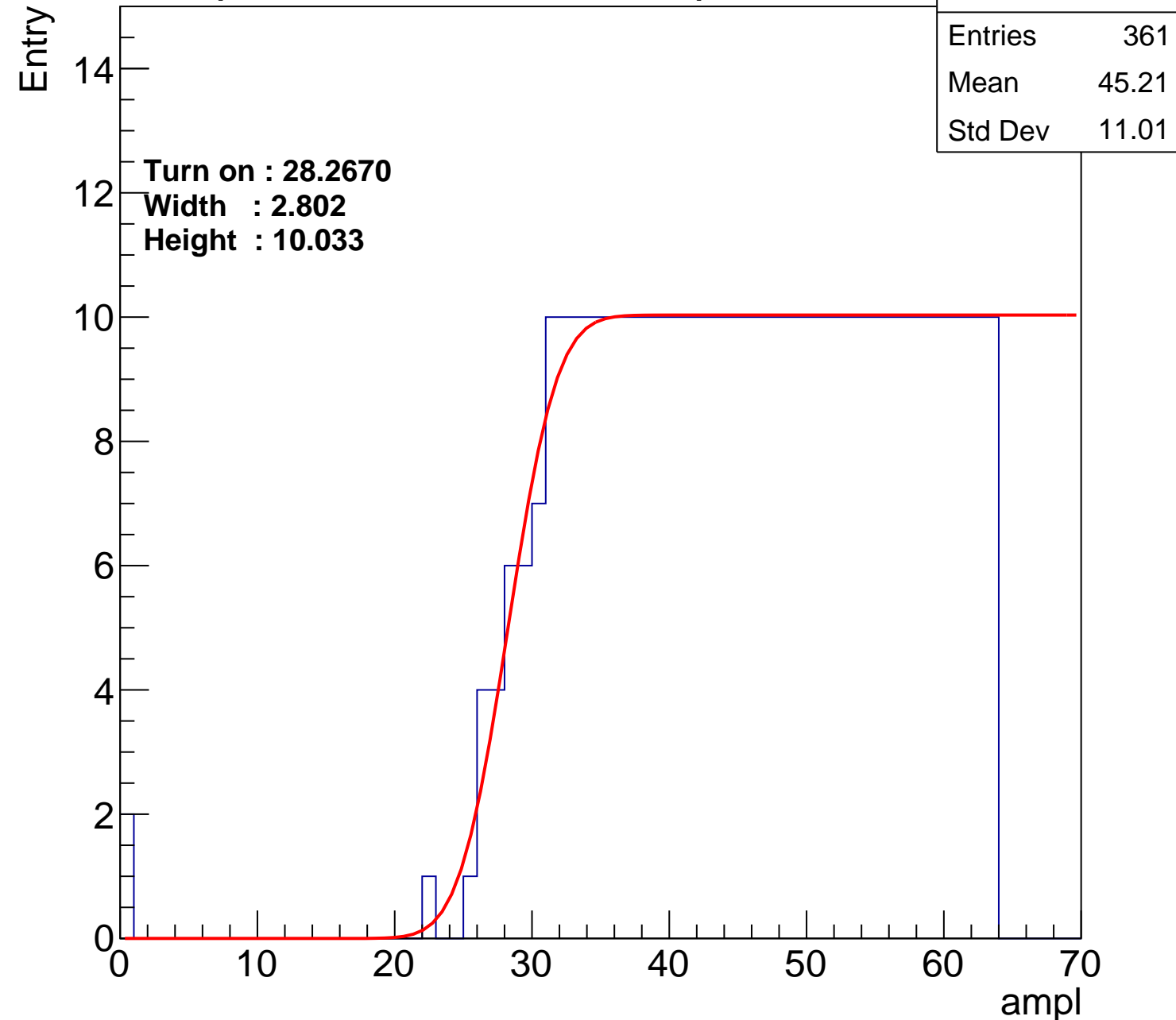
Width : 2.802

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch78

calib_packv5_042523_0143.root, FC#9, port A1

Entries	371
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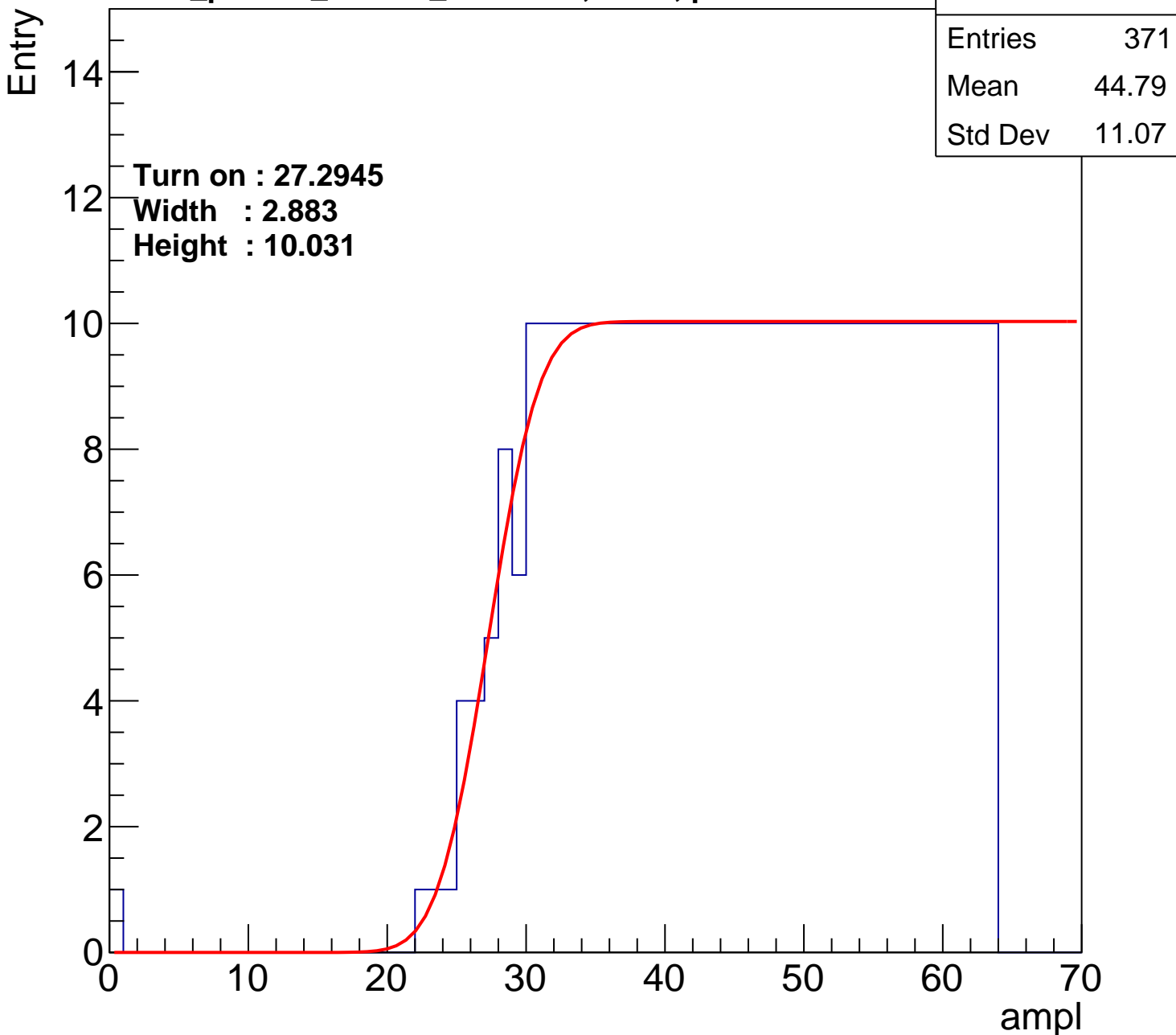
Mean	44.79
------	-------

Std Dev	11.07
---------	-------

Turn on : 27.2945

Width : 2.883

Height : 10.031



B0L001S, U1-ch79

calib_packv5_042523_0143.root, FC#9, port A1

Entries	381
Mean	44.24
Std Dev	11.5

Turn on : 26.3157

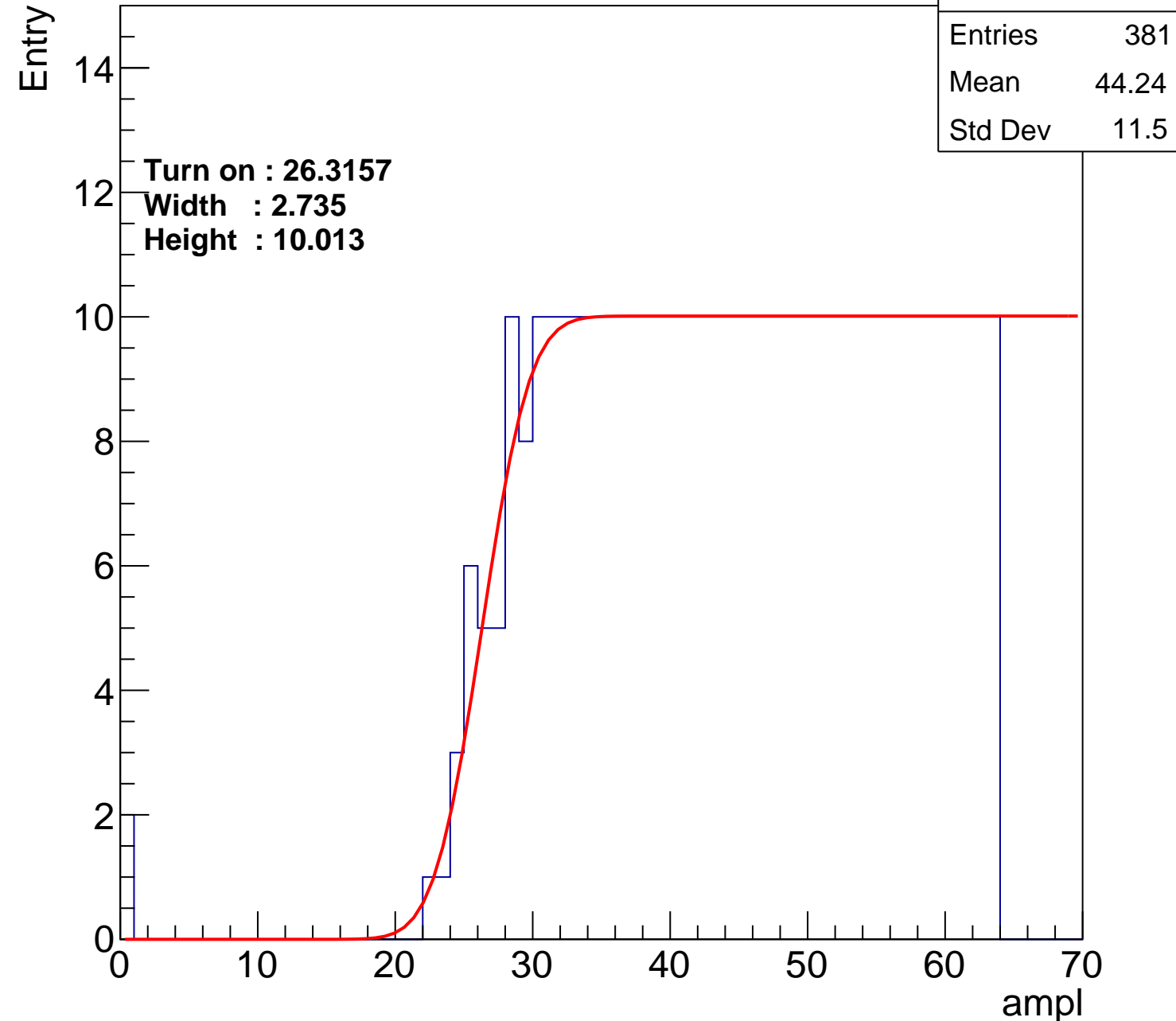
Width : 2.735

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch80

calib_packv5_042523_0143.root, FC#9, port A1

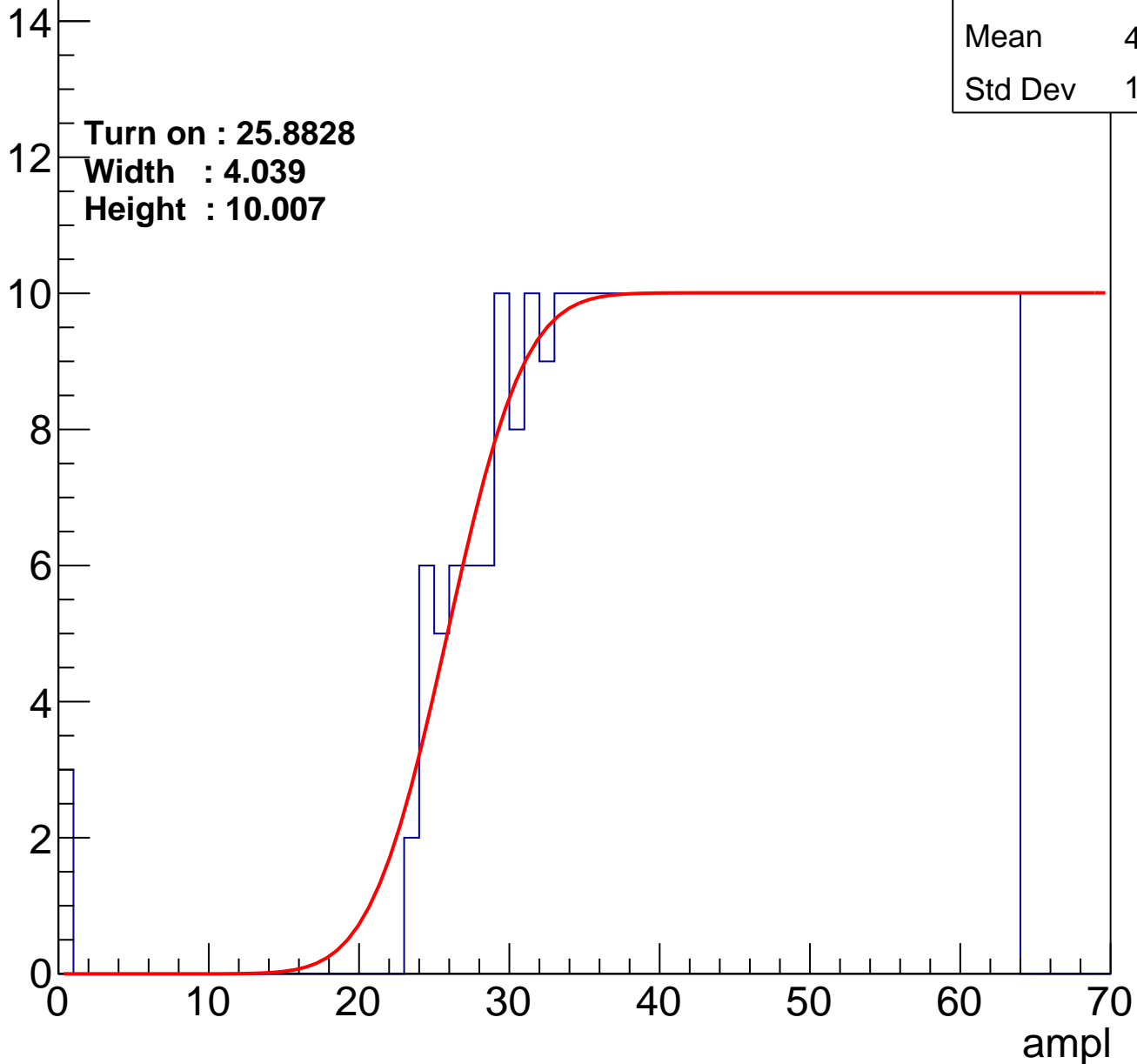
Entries	381
Mean	44.12
Std Dev	11.76

Turn on : 25.8828

Width : 4.039

Height : 10.007

Entry



B0L001S, U1-ch81

calib_packv5_042523_0143.root, FC#9, port A1

Entries	356
Mean	45.31
Std Dev	11.31

Turn on : 28.6847

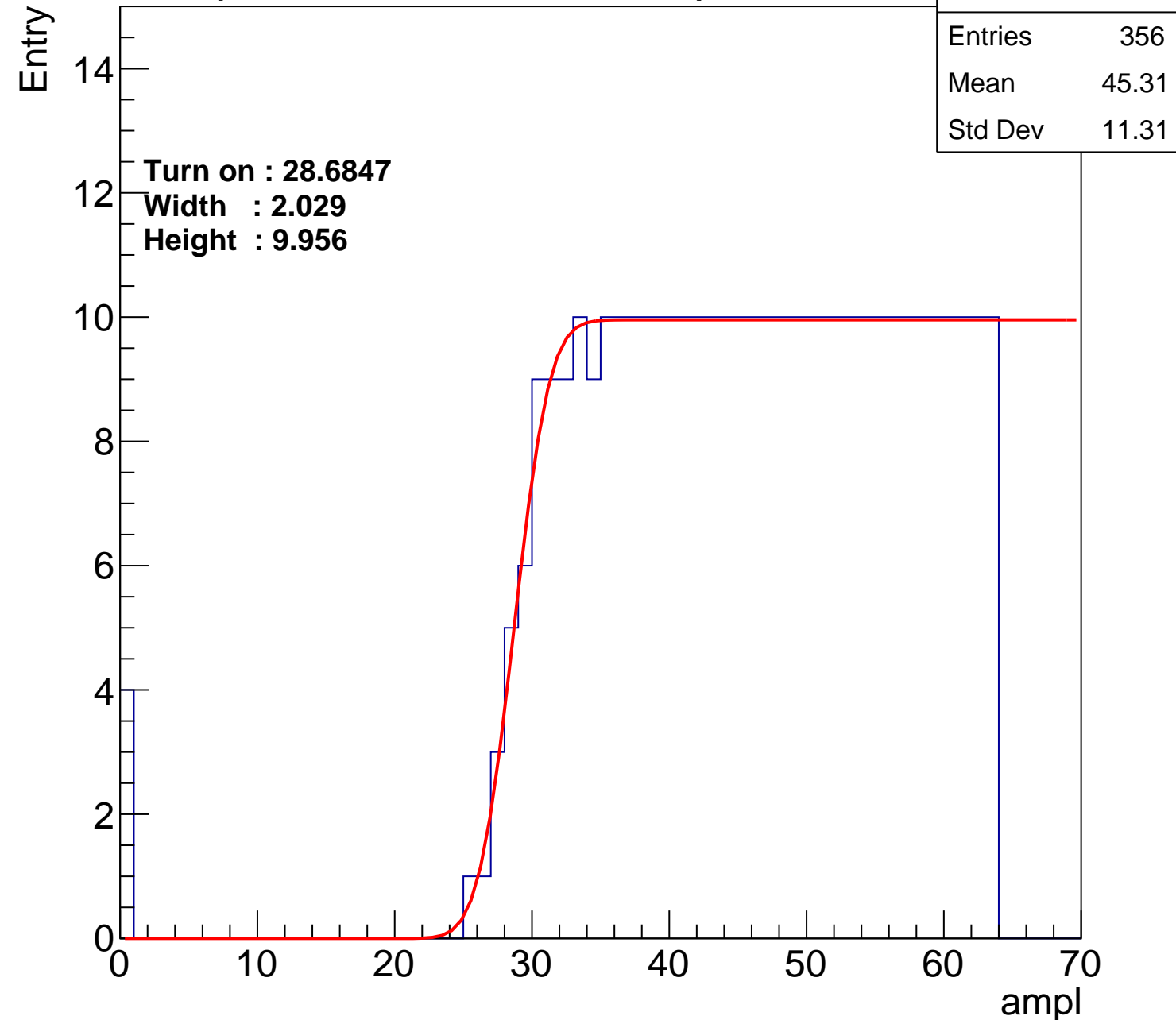
Width : 2.029

Height : 9.956

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch82

calib_packv5_042523_0143.root, FC#9, port A1

Entries	355
Mean	45.35
Std Dev	11.21

Turn on : 29.7643

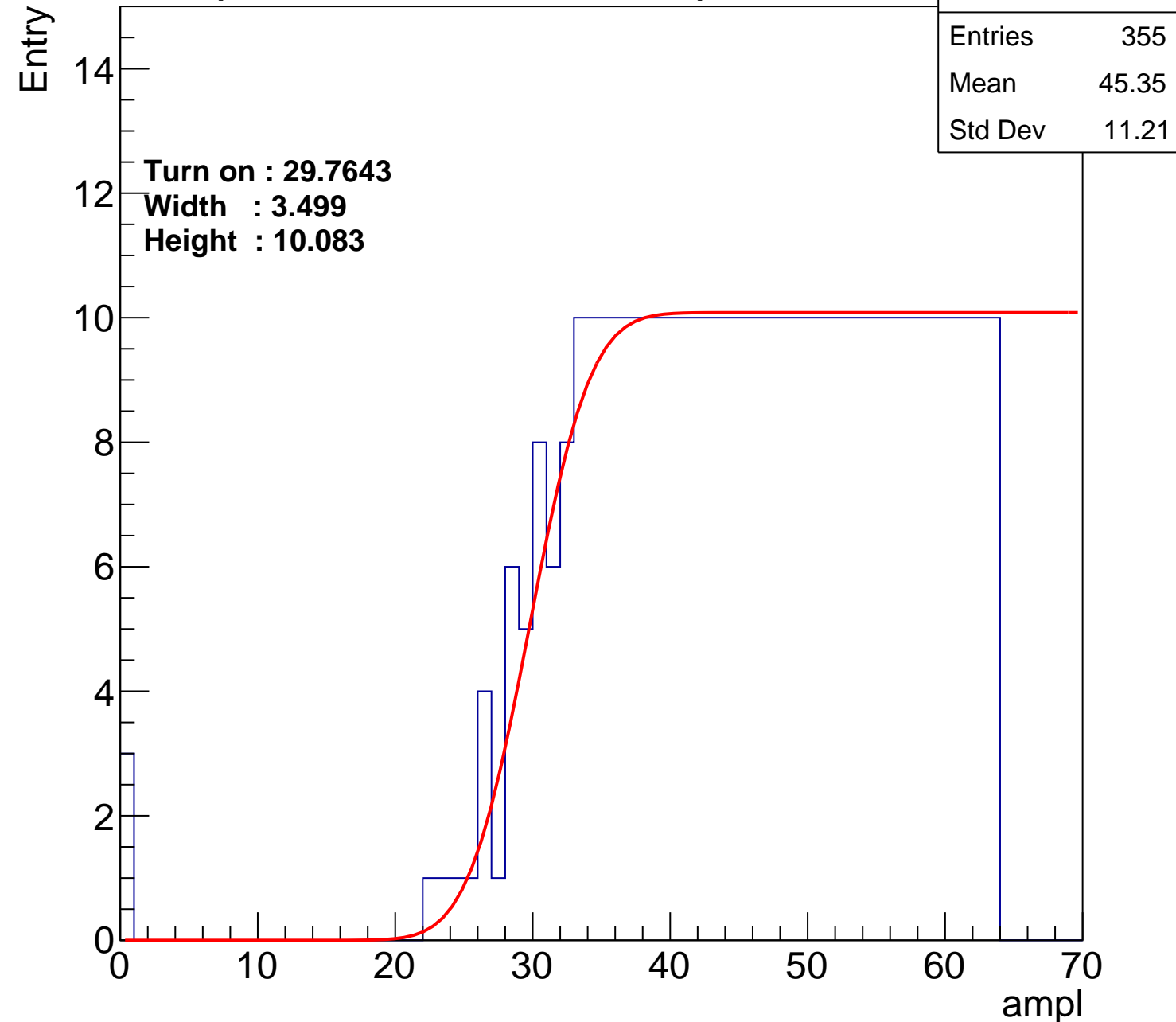
Width : 3.499

Height : 10.083

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch83

calib_packv5_042523_0143.root, FC#9, port A1

Entries	369
Mean	44.44
Std Dev	12.2

Turn on : 27.8462

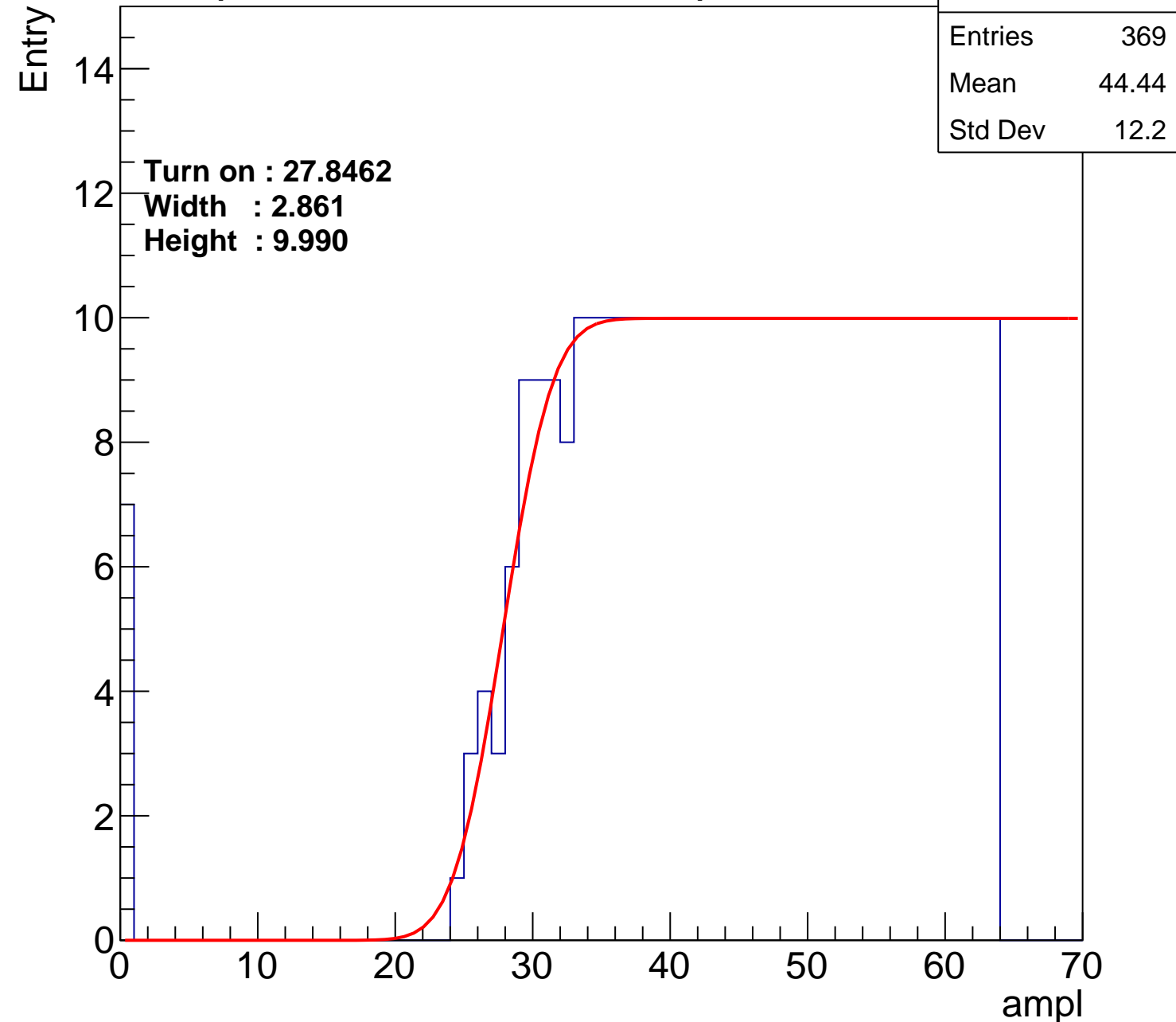
Width : 2.861

Height : 9.990

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch84

calib_packv5_042523_0143.root, FC#9, port A1

Entries	370
Mean	44.65
Std Dev	11.51

Turn on : 27.5458

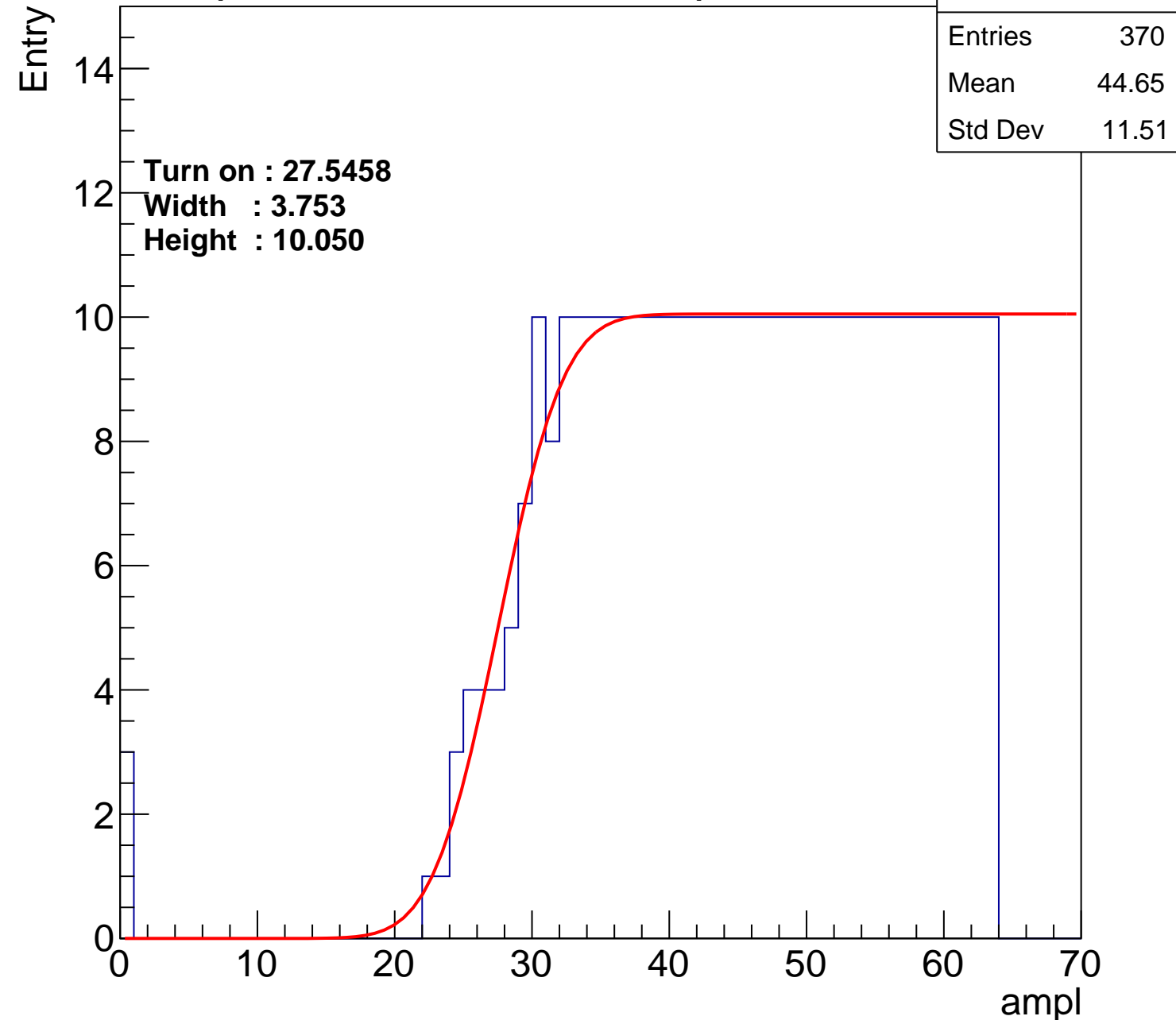
Width : 3.753

Height : 10.050

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch85

calib_packv5_042523_0143.root, FC#9, port A1

Entries	374
Mean	44.47
Std Dev	11.58

Turn on : 27.0148

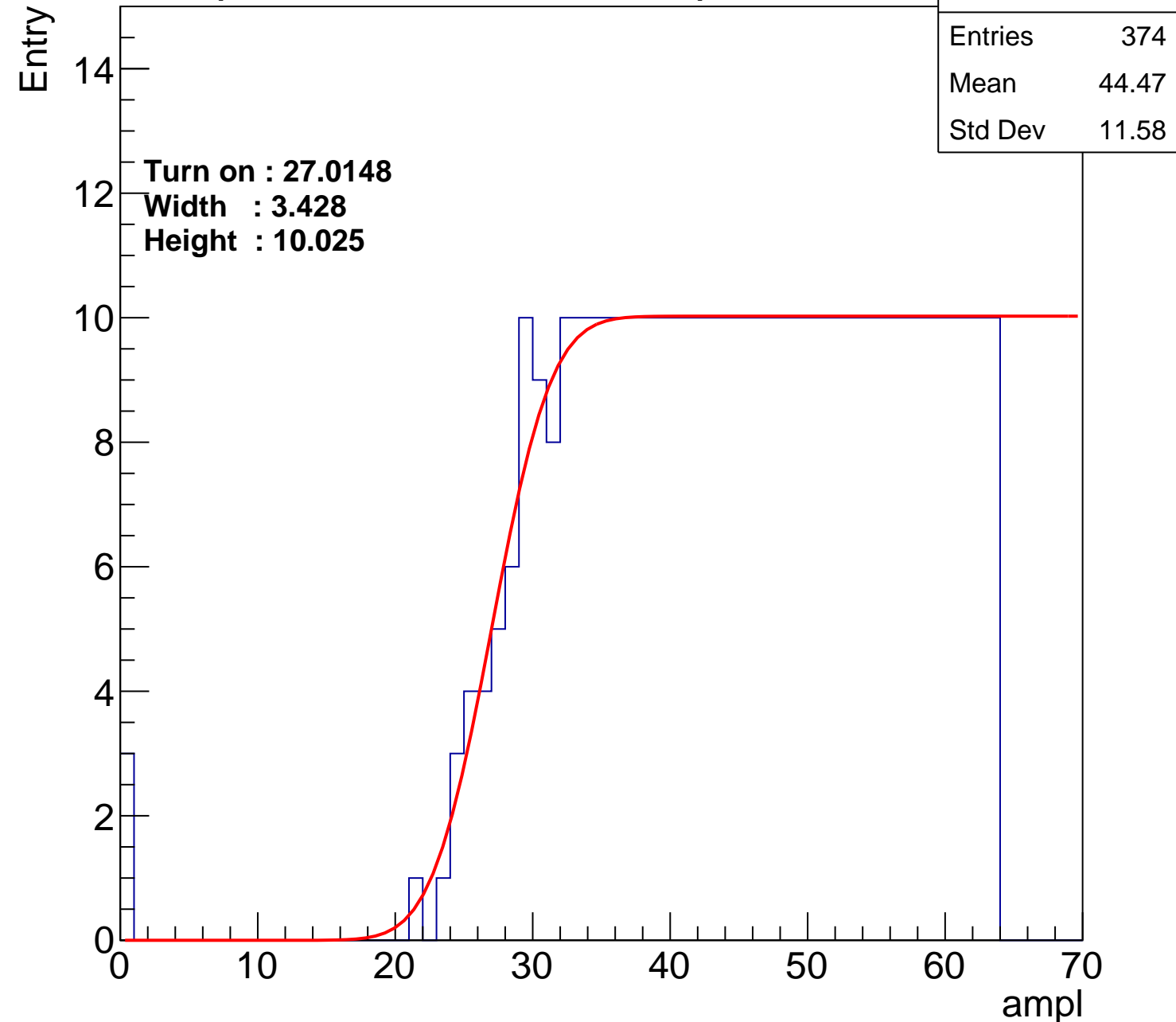
Width : 3.428

Height : 10.025

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch86

calib_packv5_042523_0143.root, FC#9, port A1

Entries	371
Mean	44.61
Std Dev	11.53

Turn on : 27.6912

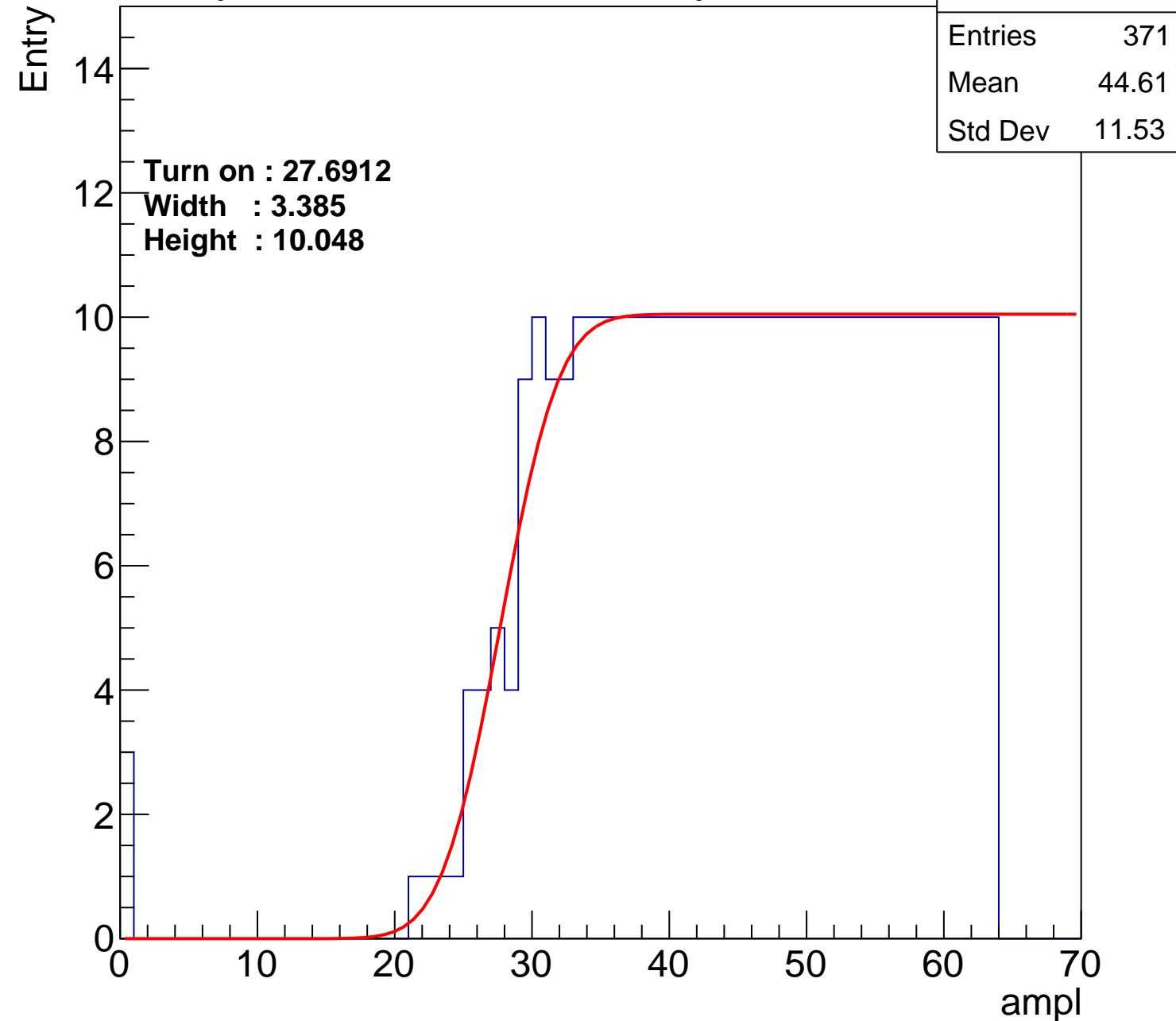
Width : 3.385

Height : 10.048

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch87

calib_packv5_042523_0143.root, FC#9, port A1

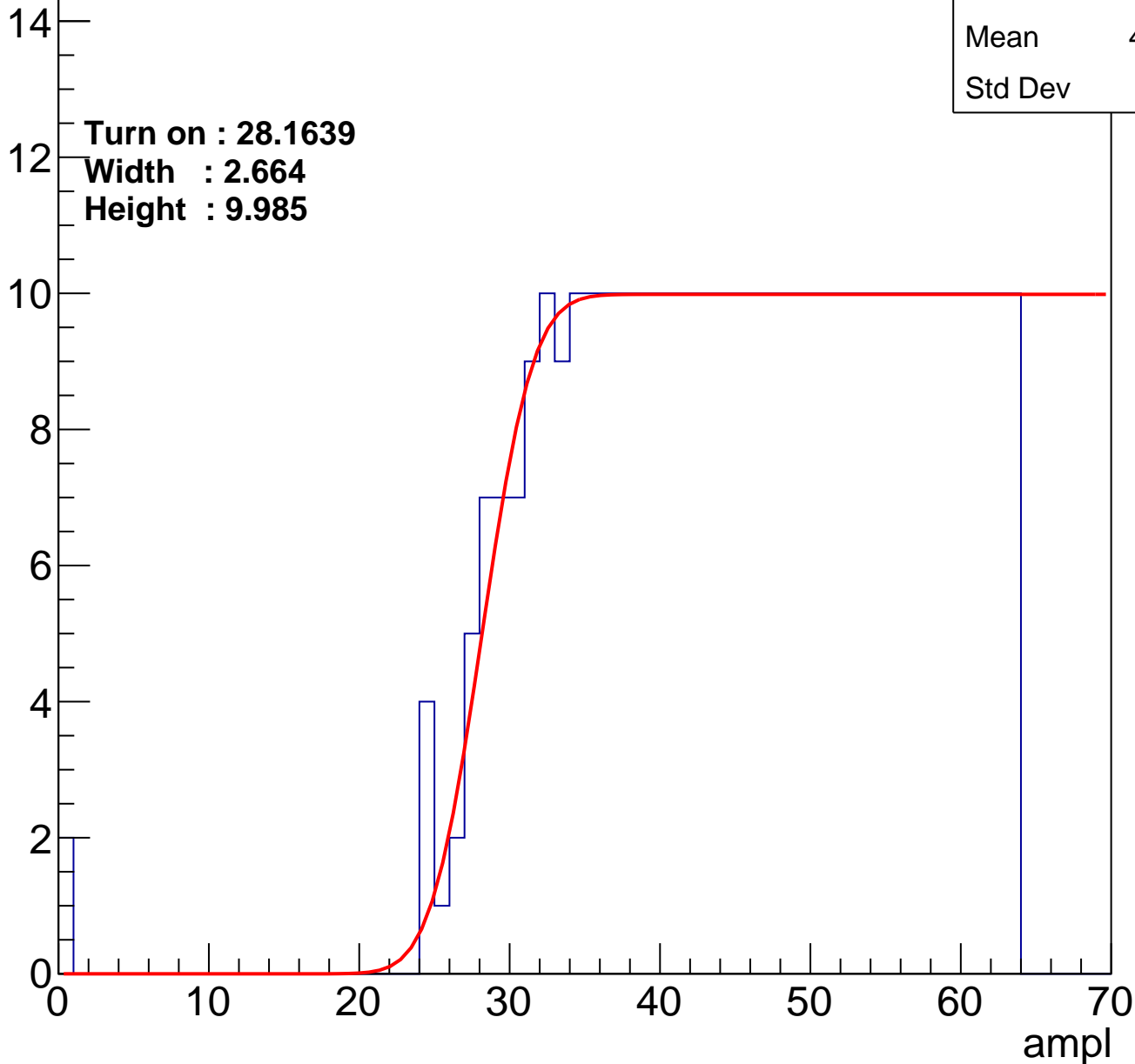
Entry

Entries	363
Mean	45.08
Std Dev	11.11

Turn on : 28.1639

Width : 2.664

Height : 9.985



B0L001S, U1-ch88

calib_packv5_042523_0143.root, FC#9, port A1

Entries	392
Mean	43.43
Std Dev	12.39

Turn on : 25.6345

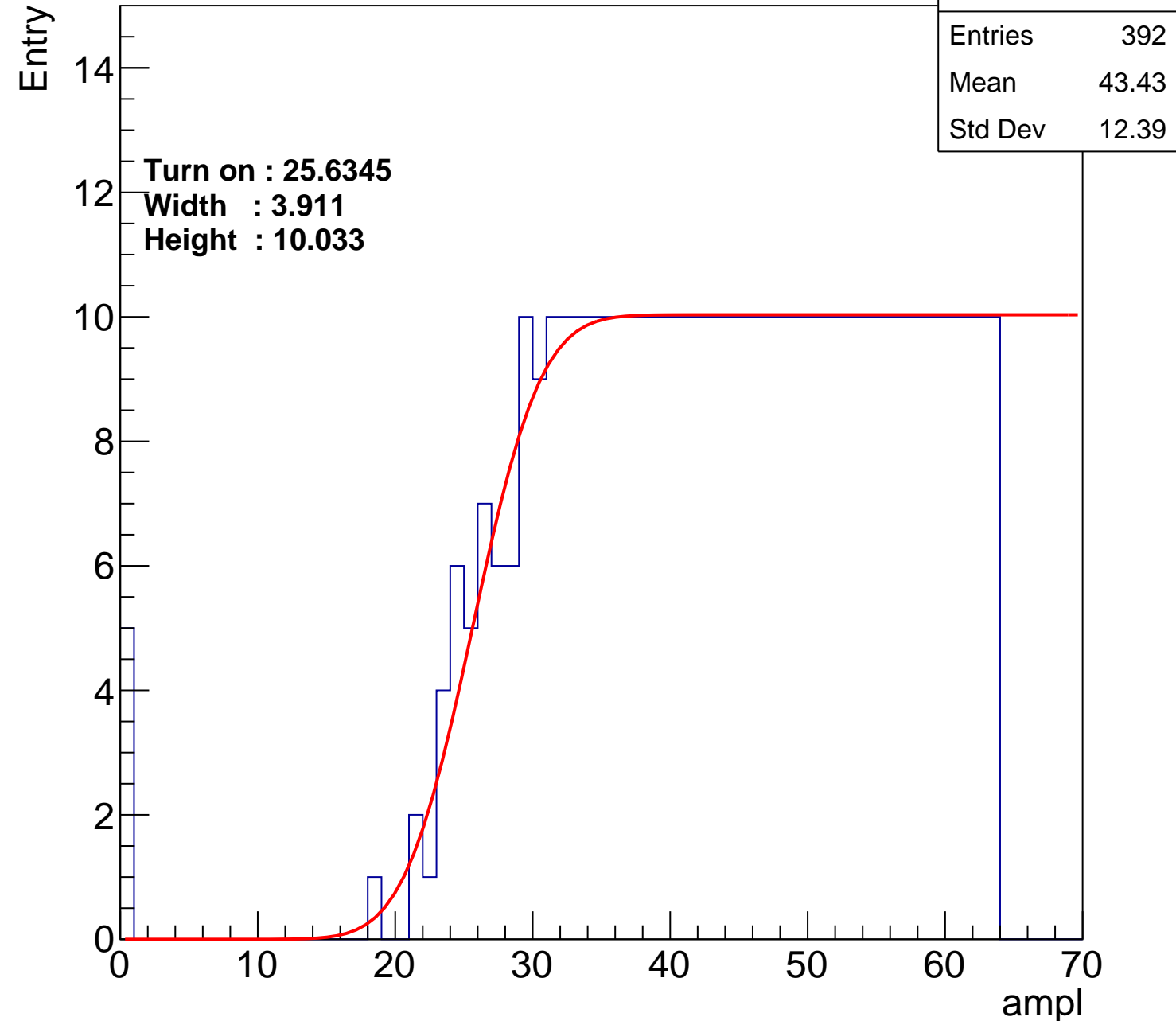
Width : 3.911

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch89

calib_packv5_042523_0143.root, FC#9, port A1

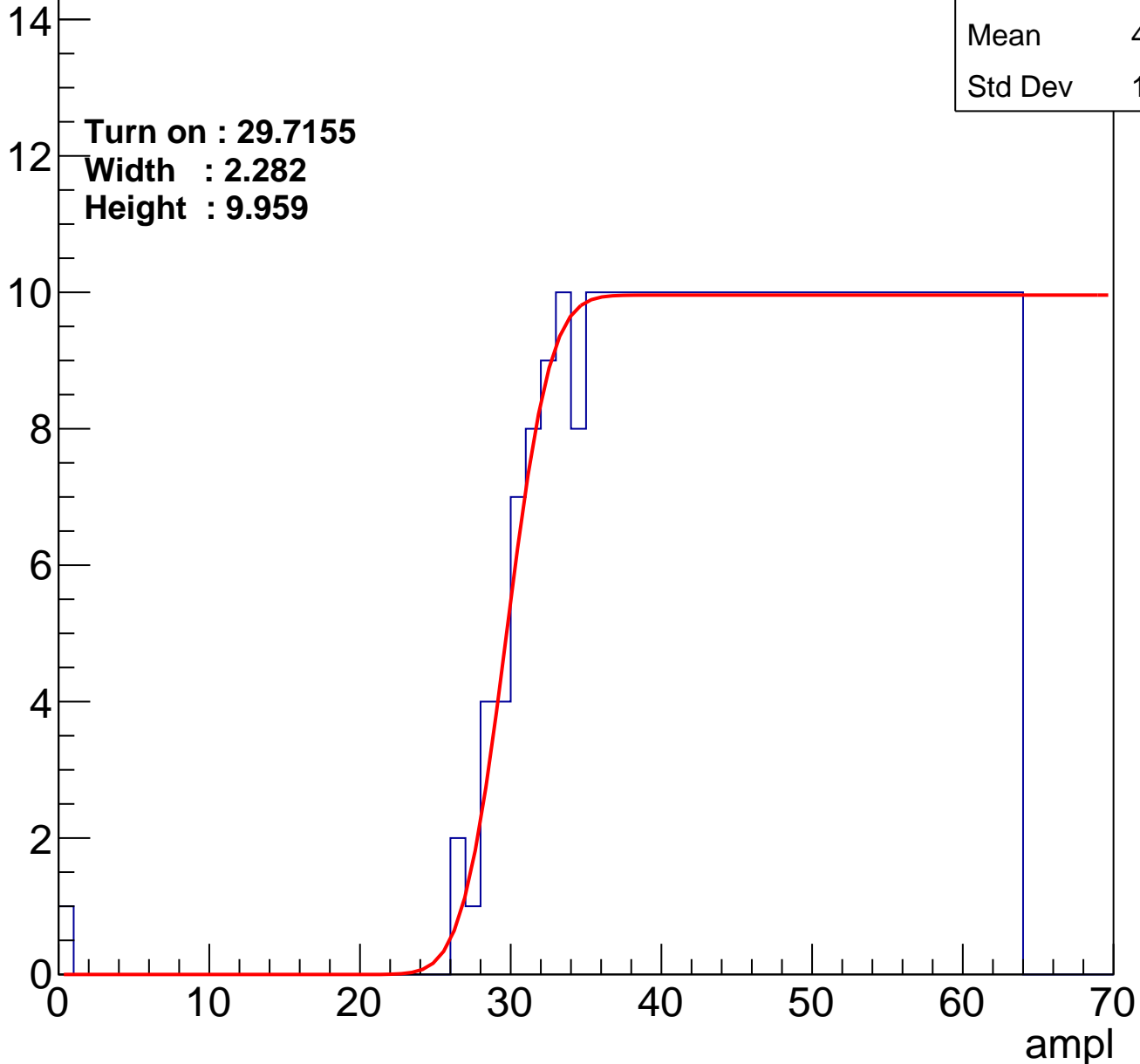
Entries	344
Mean	46.12
Std Dev	10.35

Turn on : 29.7155

Width : 2.282

Height : 9.959

Entry



B0L001S, U1-ch90

calib_packv5_042523_0143.root, FC#9, port A1

Entries	377
Mean	44.4
Std Dev	11.44

Turn on : 26.4820

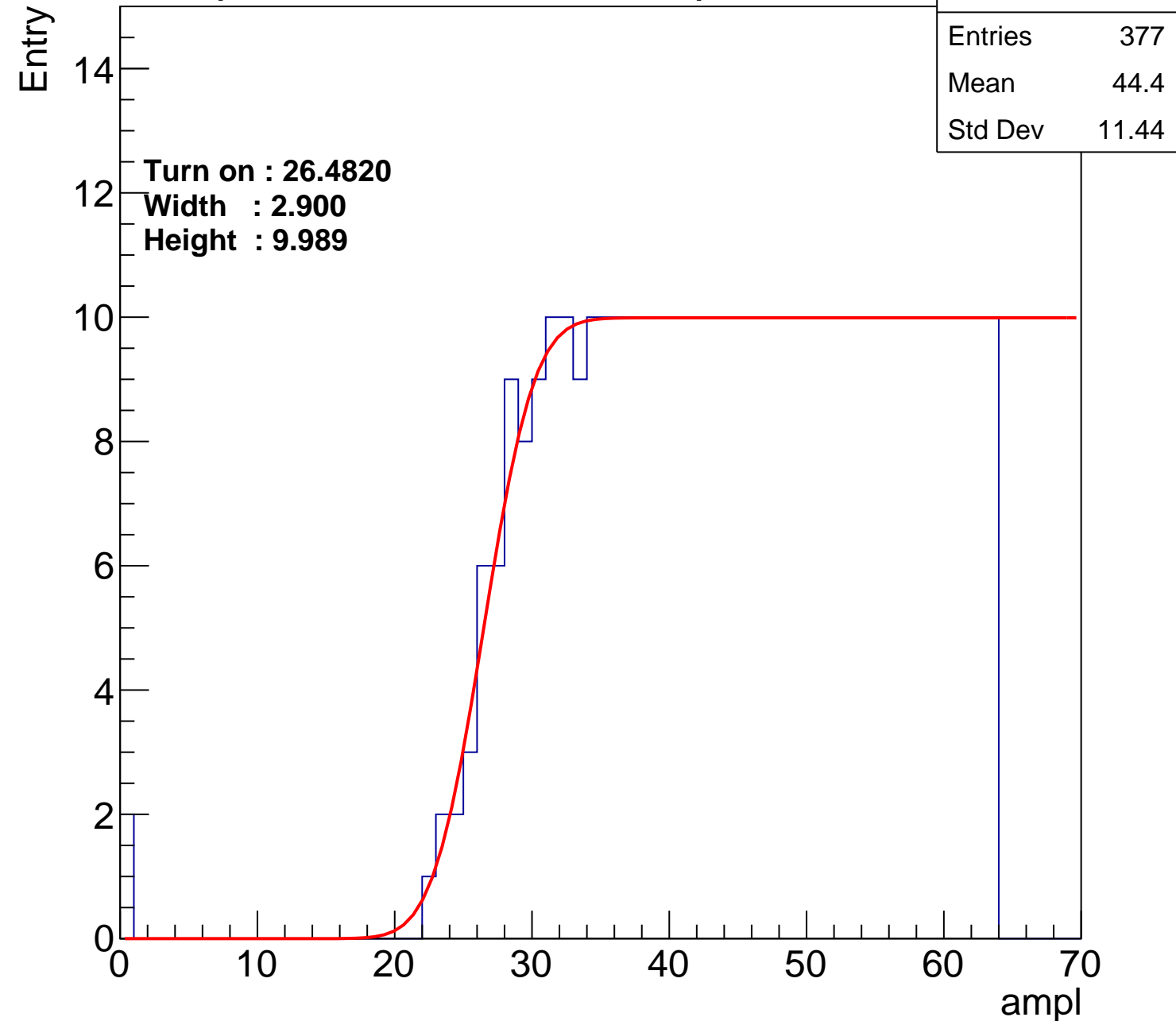
Width : 2.900

Height : 9.989

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch91

calib_packv5_042523_0143.root, FC#9, port A1

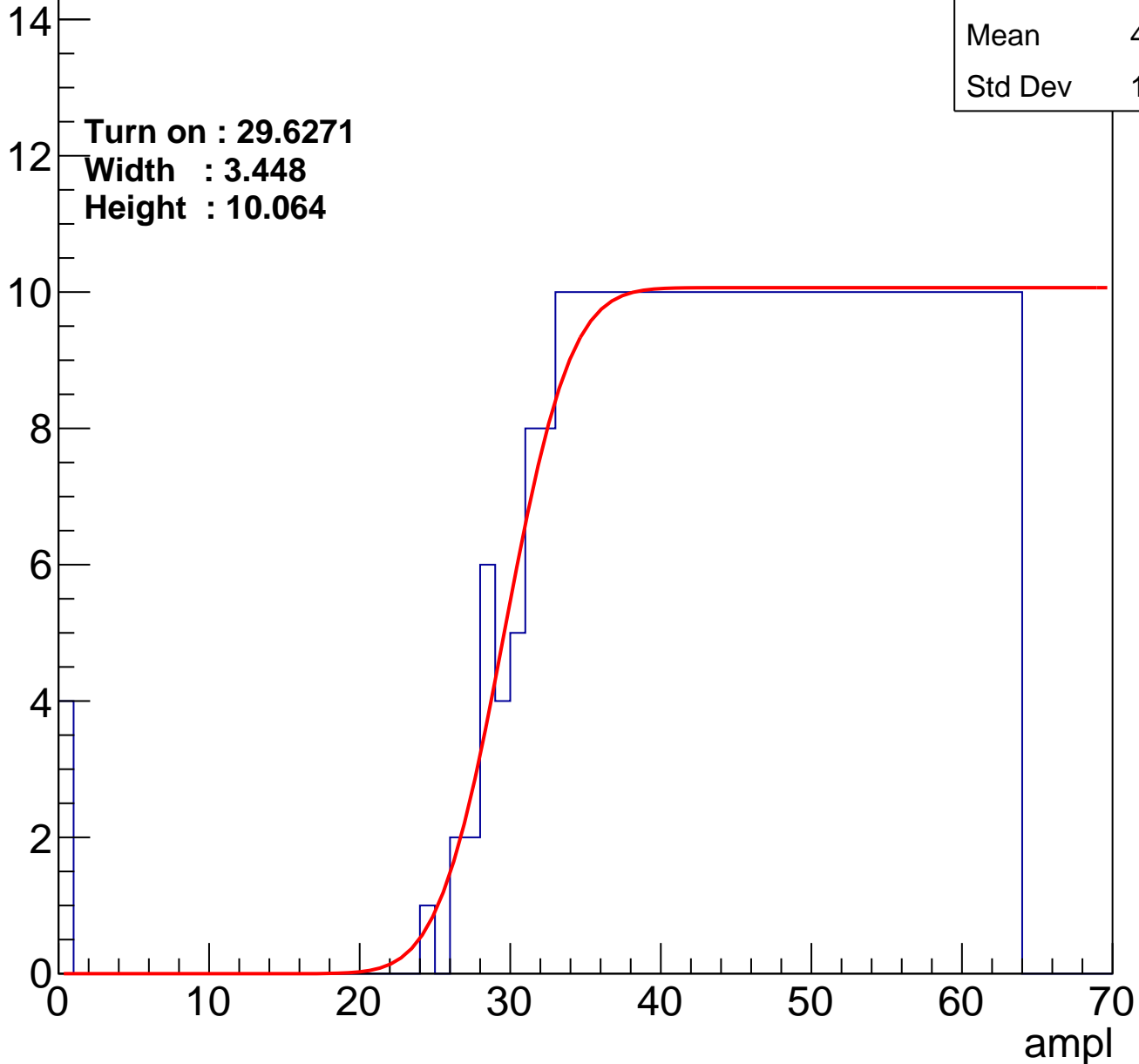
Entries	350
Mean	45.57
Std Dev	11.24

Turn on : 29.6271

Width : 3.448

Height : 10.064

Entry



B0L001S, U1-ch92

calib_packv5_042523_0143.root, FC#9, port A1

Entries	370
Mean	44.7
Std Dev	11.36

Turn on : 27.8311

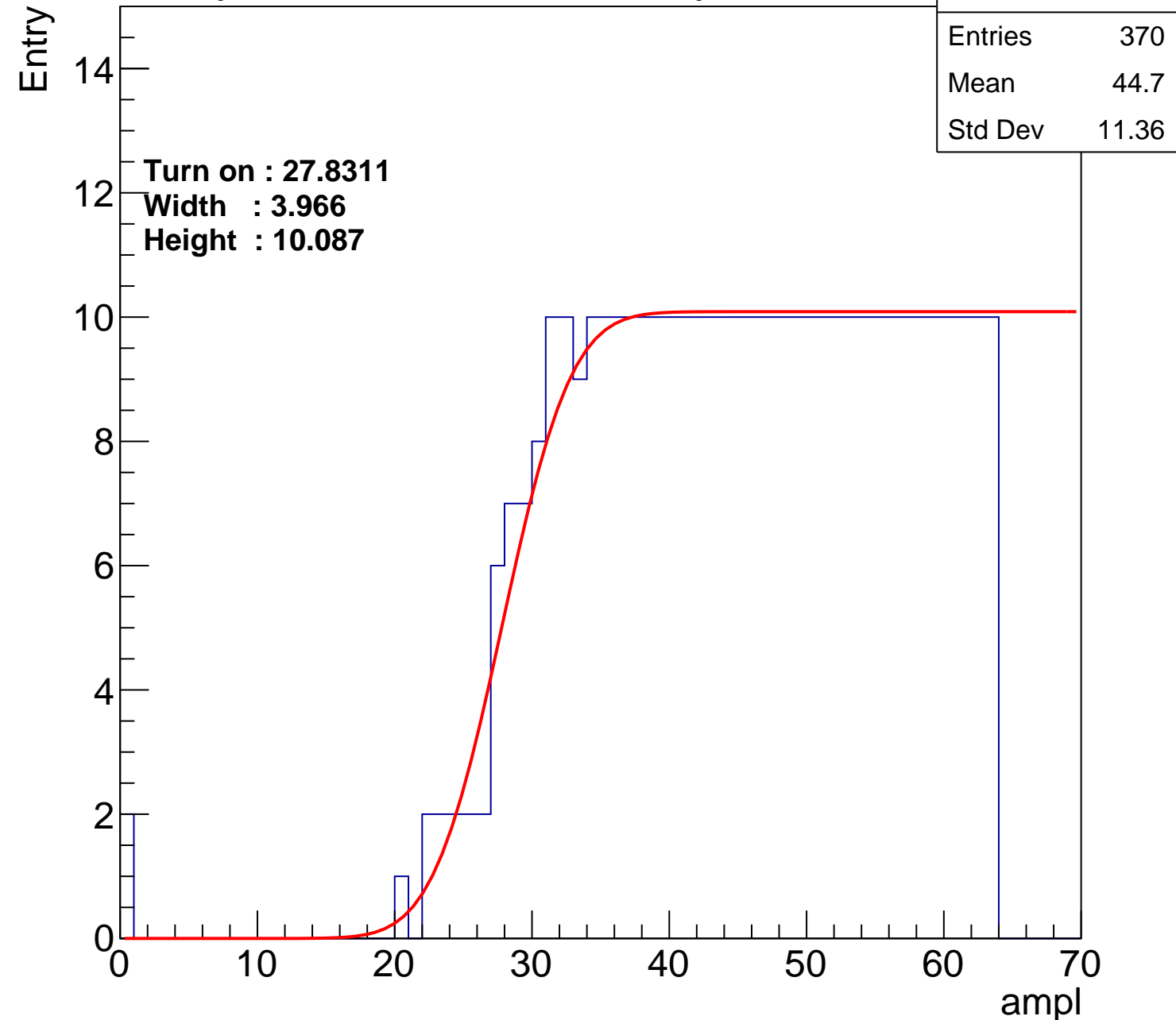
Width : 3.966

Height : 10.087

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch93

calib_packv5_042523_0143.root, FC#9, port A1

Entries	369
Mean	44.72
Std Dev	11.45

Turn on : 27.7468

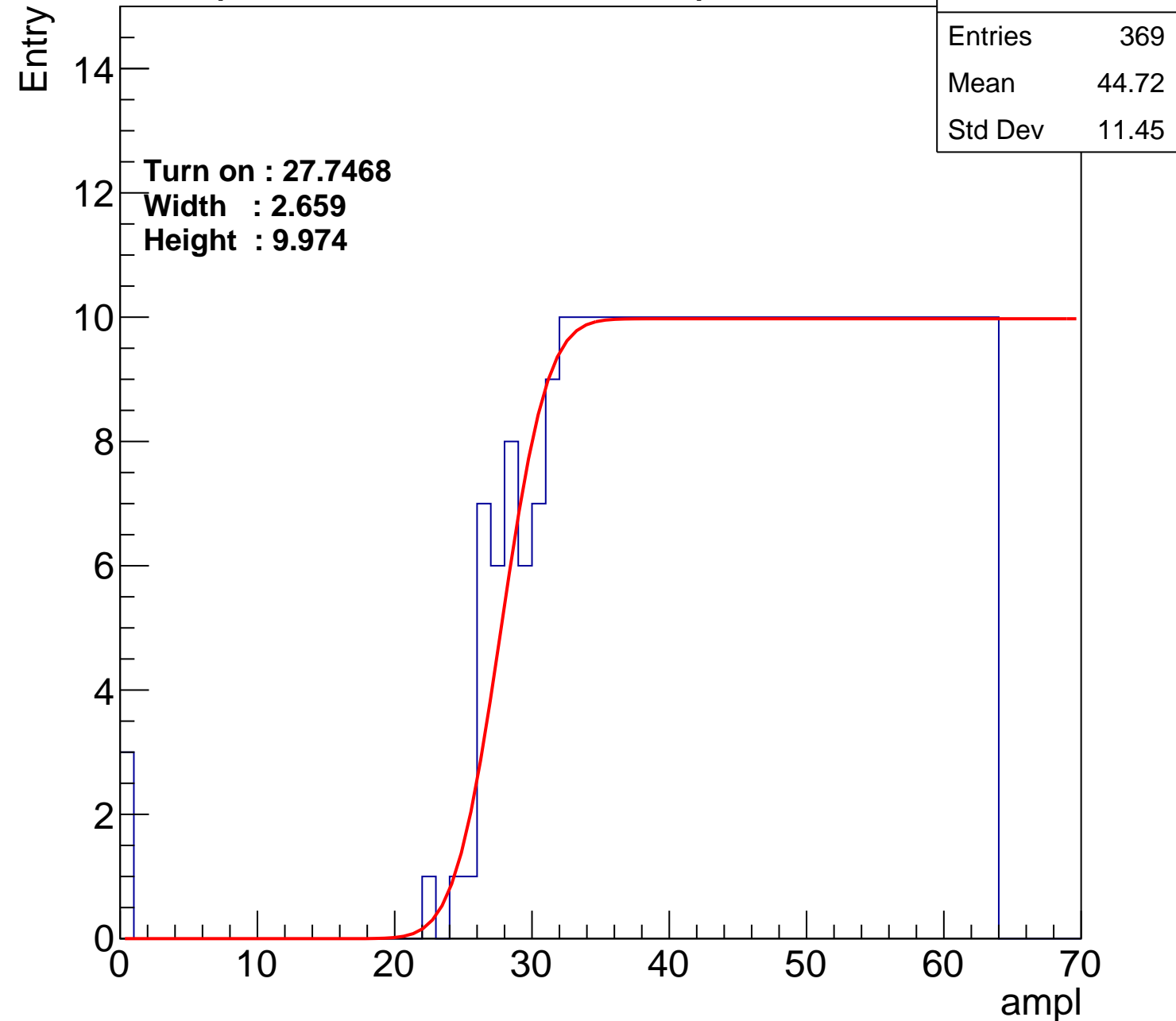
Width : 2.659

Height : 9.974

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch94

calib_packv5_042523_0143.root, FC#9, port A1

Entries	373
Mean	44.49
Std Dev	11.69

Turn on : 27.2279

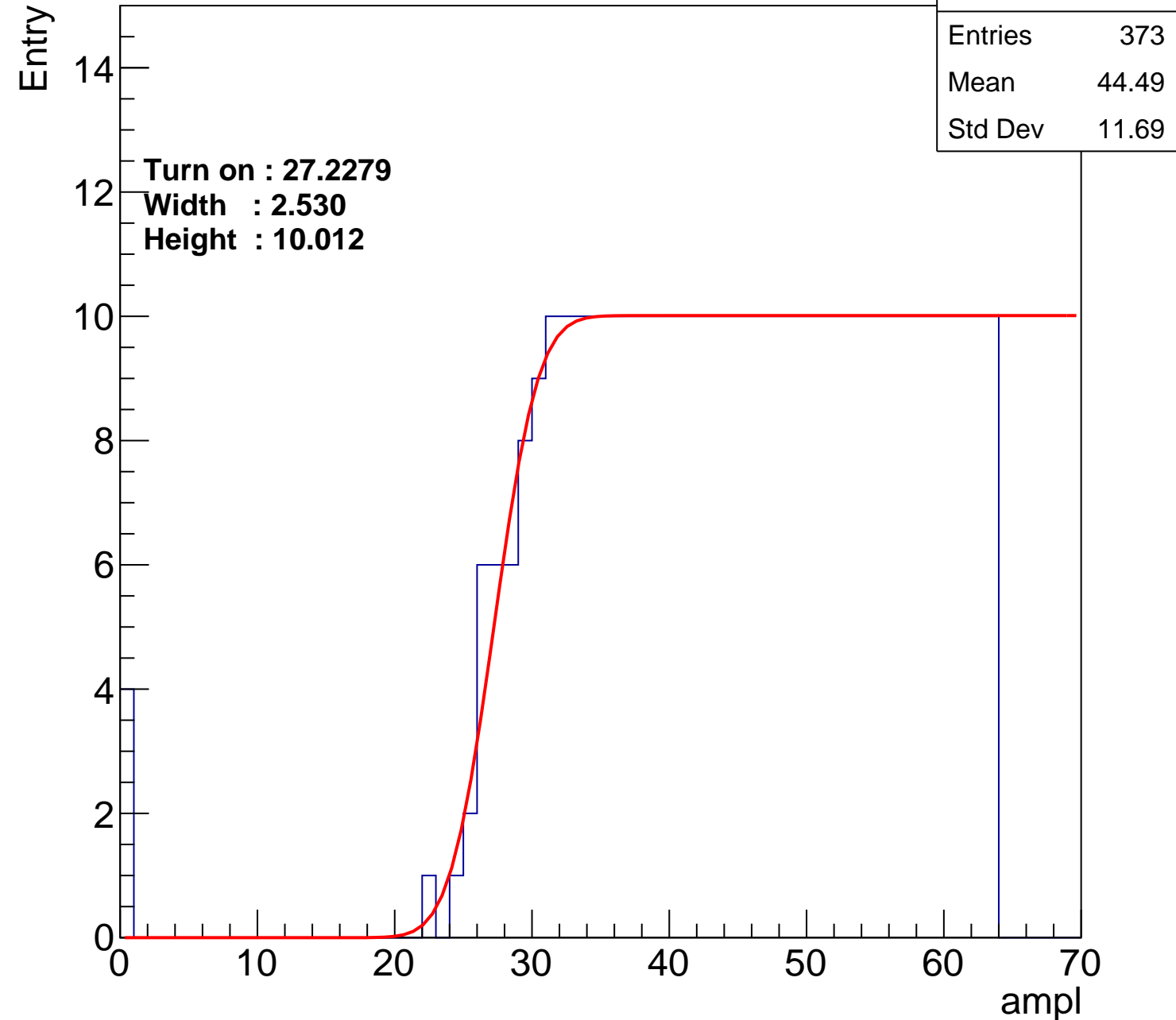
Width : 2.530

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch95

calib_packv5_042523_0143.root, FC#9, port A1

Entries	367
Mean	44.81
Std Dev	11.42

Turn on : 27.9443

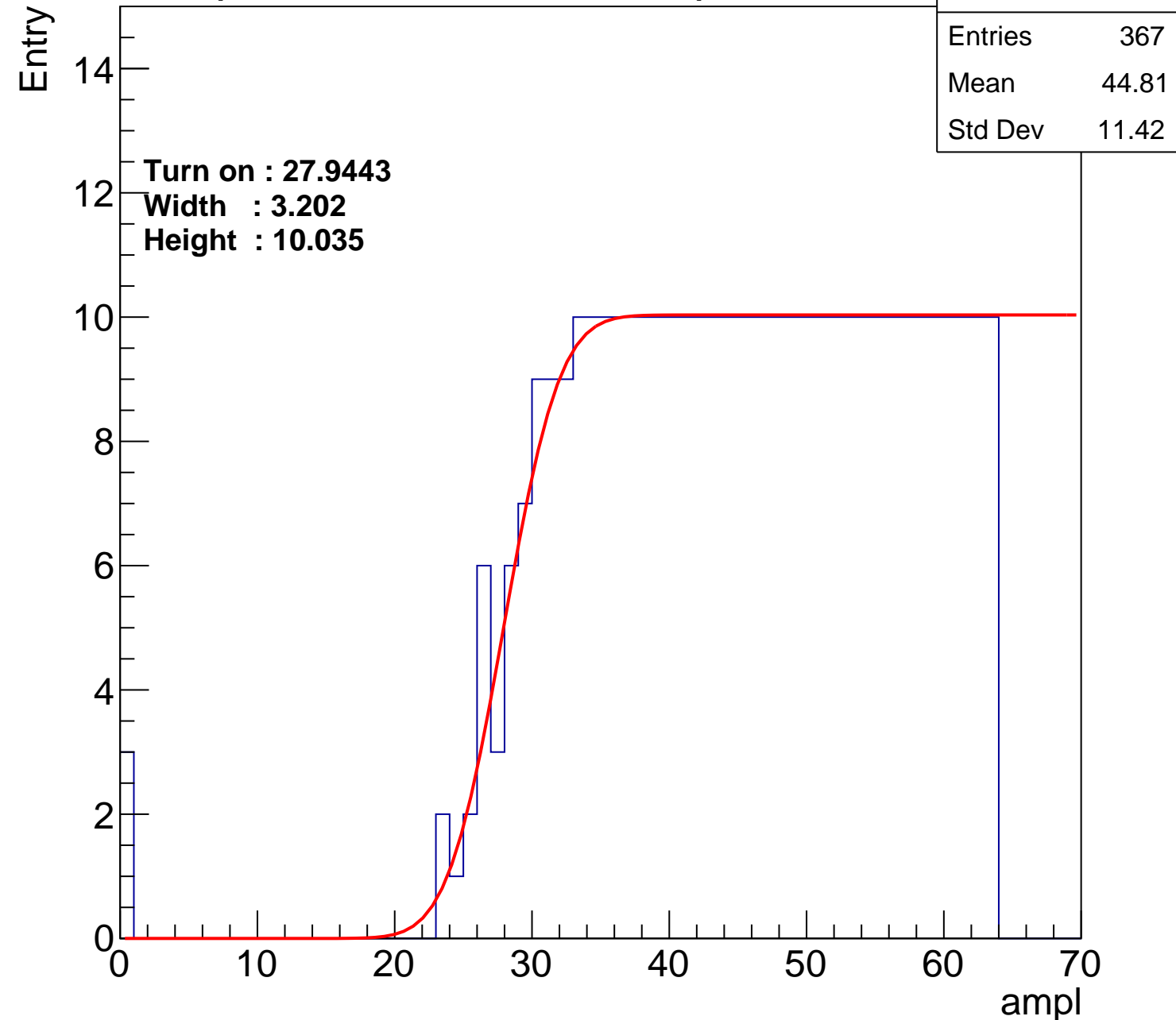
Width : 3.202

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch96

calib_packv5_042523_0143.root, FC#9, port A1

Entries	372
Mean	44.52
Std Dev	11.68

Turn on : 27.2181

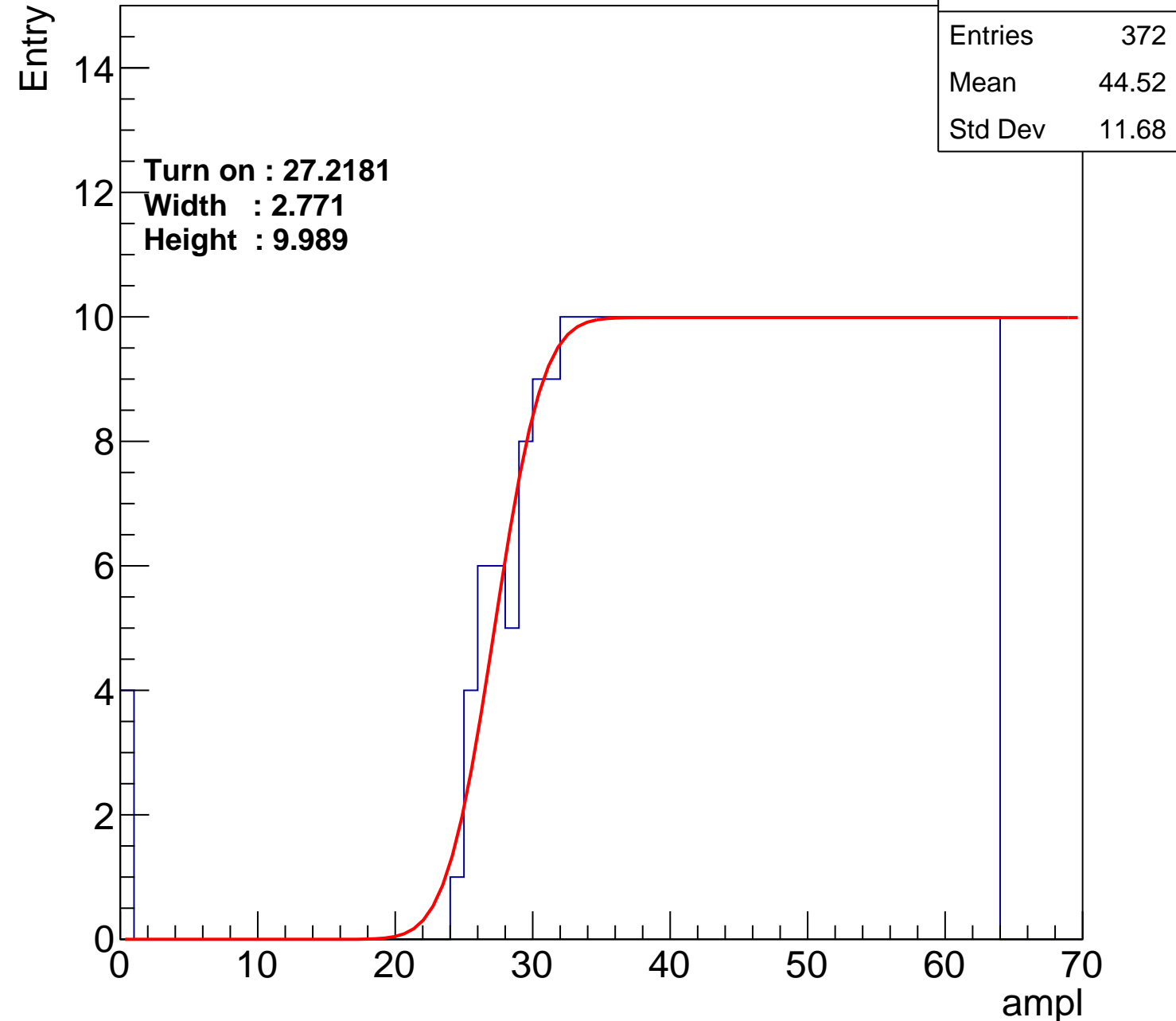
Width : 2.771

Height : 9.989

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch97

calib_packv5_042523_0143.root, FC#9, port A1

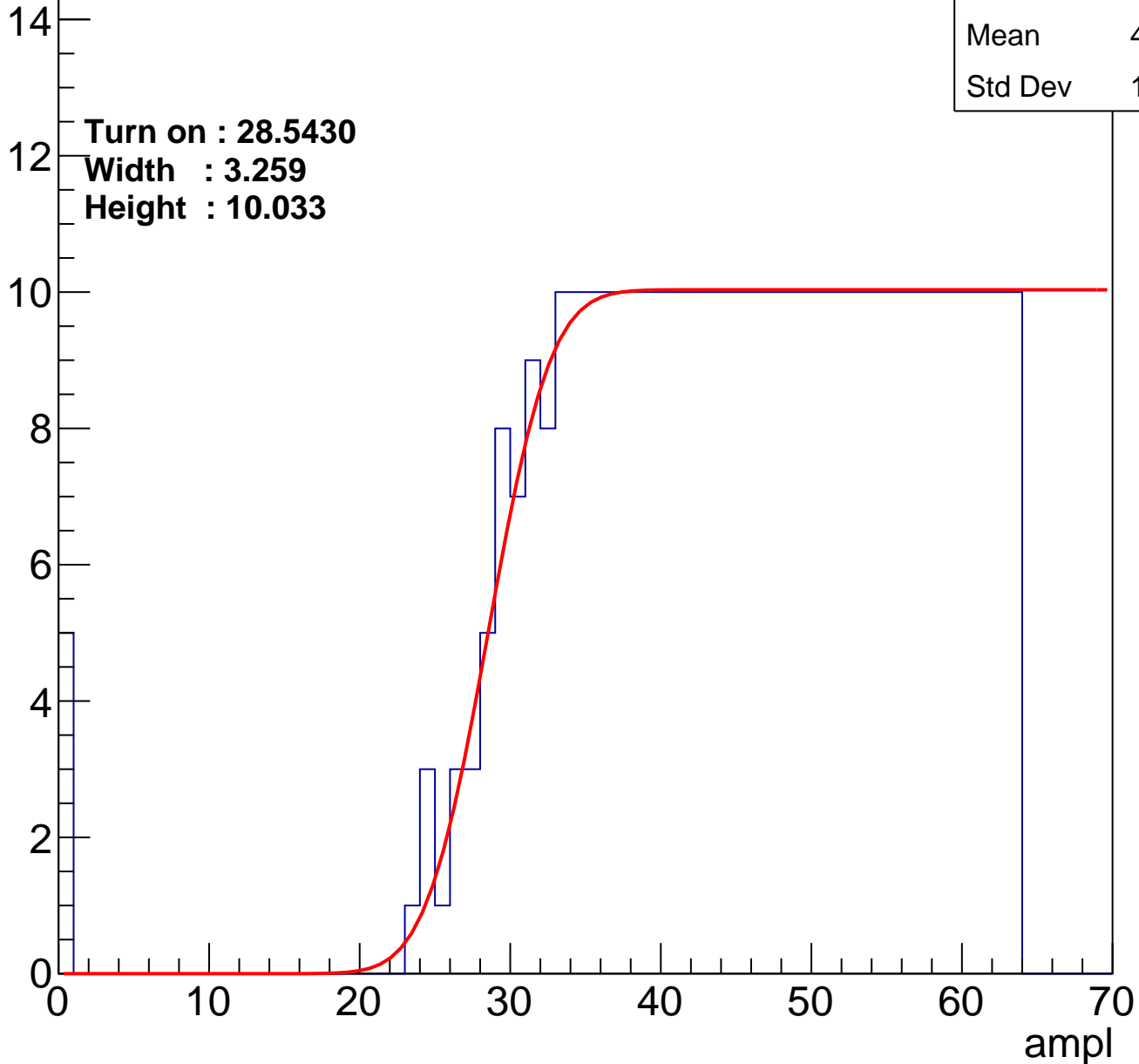
Entries	363
Mean	44.84
Std Dev	11.75

Turn on : 28.5430

Width : 3.259

Height : 10.033

Entry



B0L001S, U1-ch98

calib_packv5_042523_0143.root, FC#9, port A1

Entries	357
Mean	45.36
Std Dev	11

Turn on : 29.0354

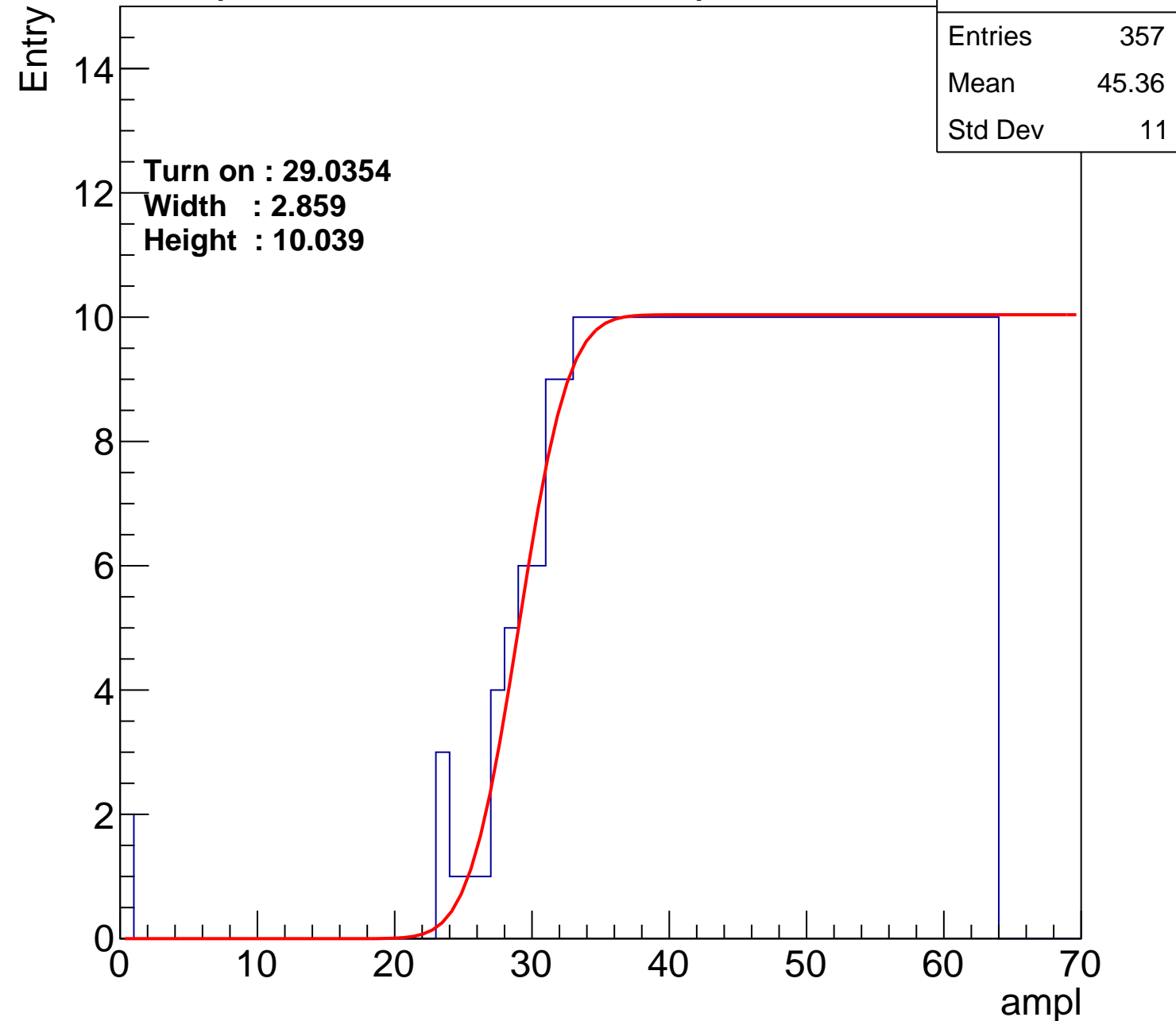
Width : 2.859

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch99

calib_packv5_042523_0143.root, FC#9, port A1

Entries	360
Mean	45.09
Std Dev	11.43

Turn on : 28.3421

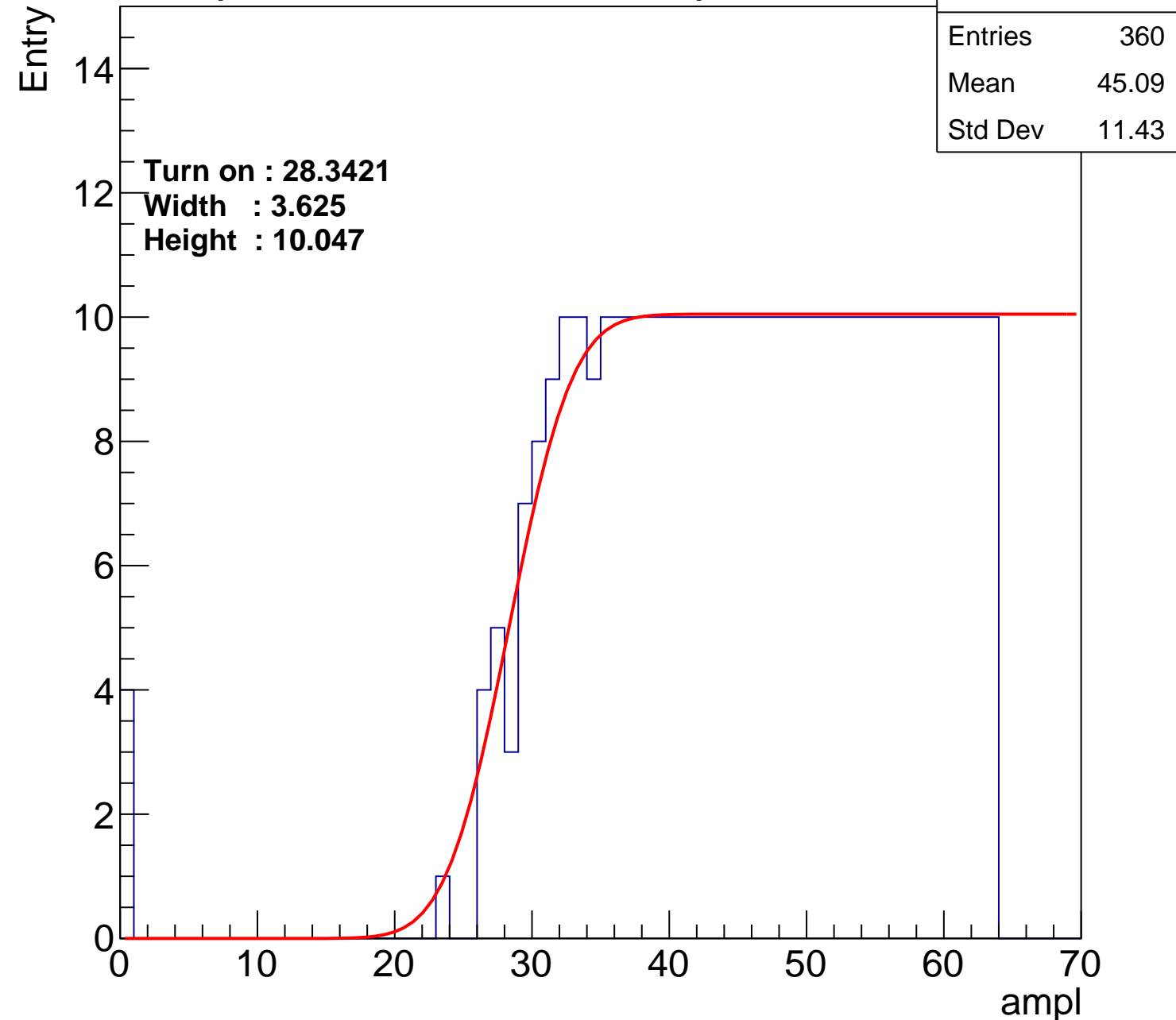
Width : 3.625

Height : 10.047

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch100

calib_packv5_042523_0143.root, FC#9, port A1

Entries	354
Mean	45.33
Std Dev	11.38

Turn on : 29.5300

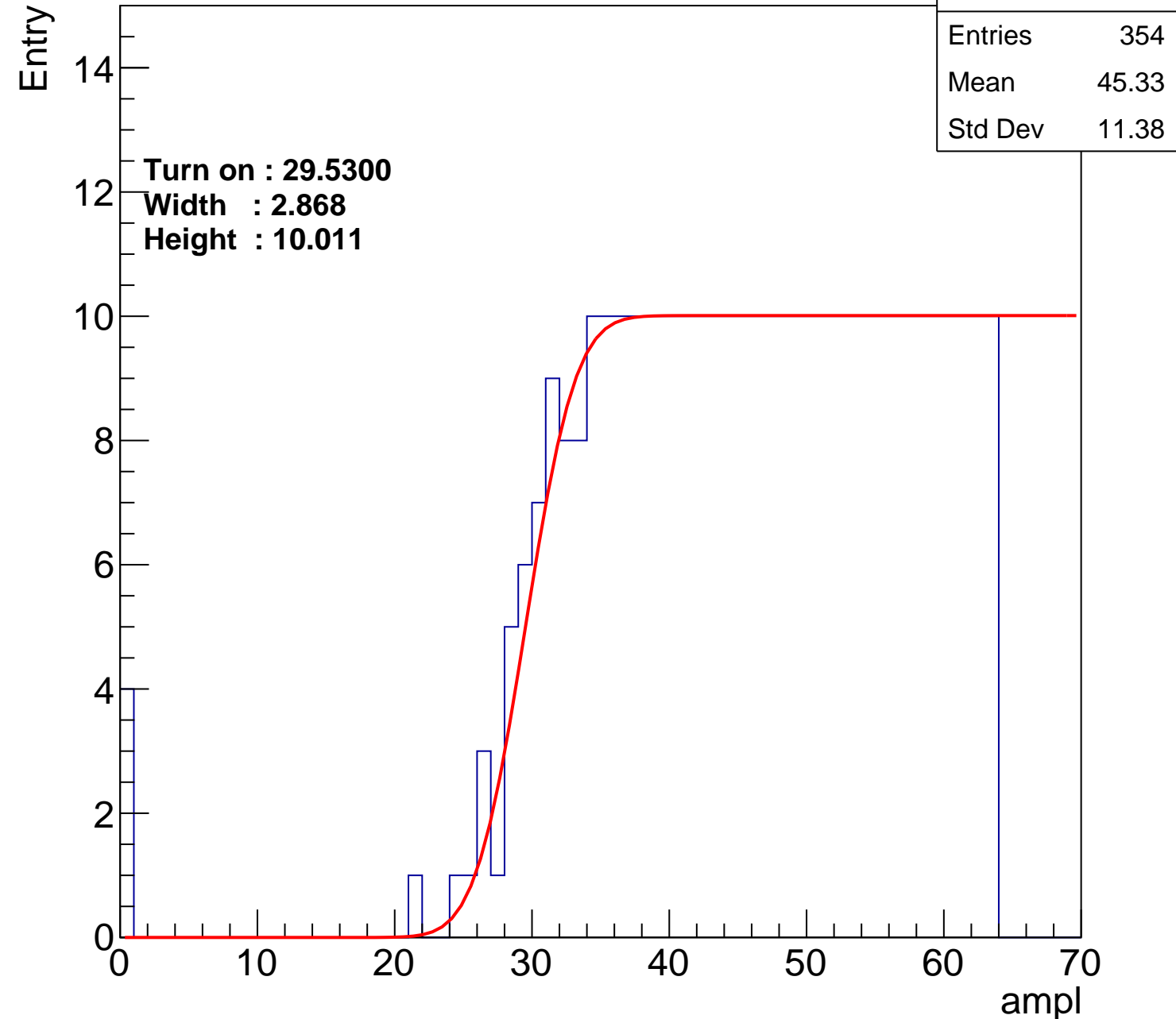
Width : 2.868

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch101

calib_packv5_042523_0143.root, FC#9, port A1

Entries	385
Mean	44.02
Std Dev	11.64

Turn on : 25.7886

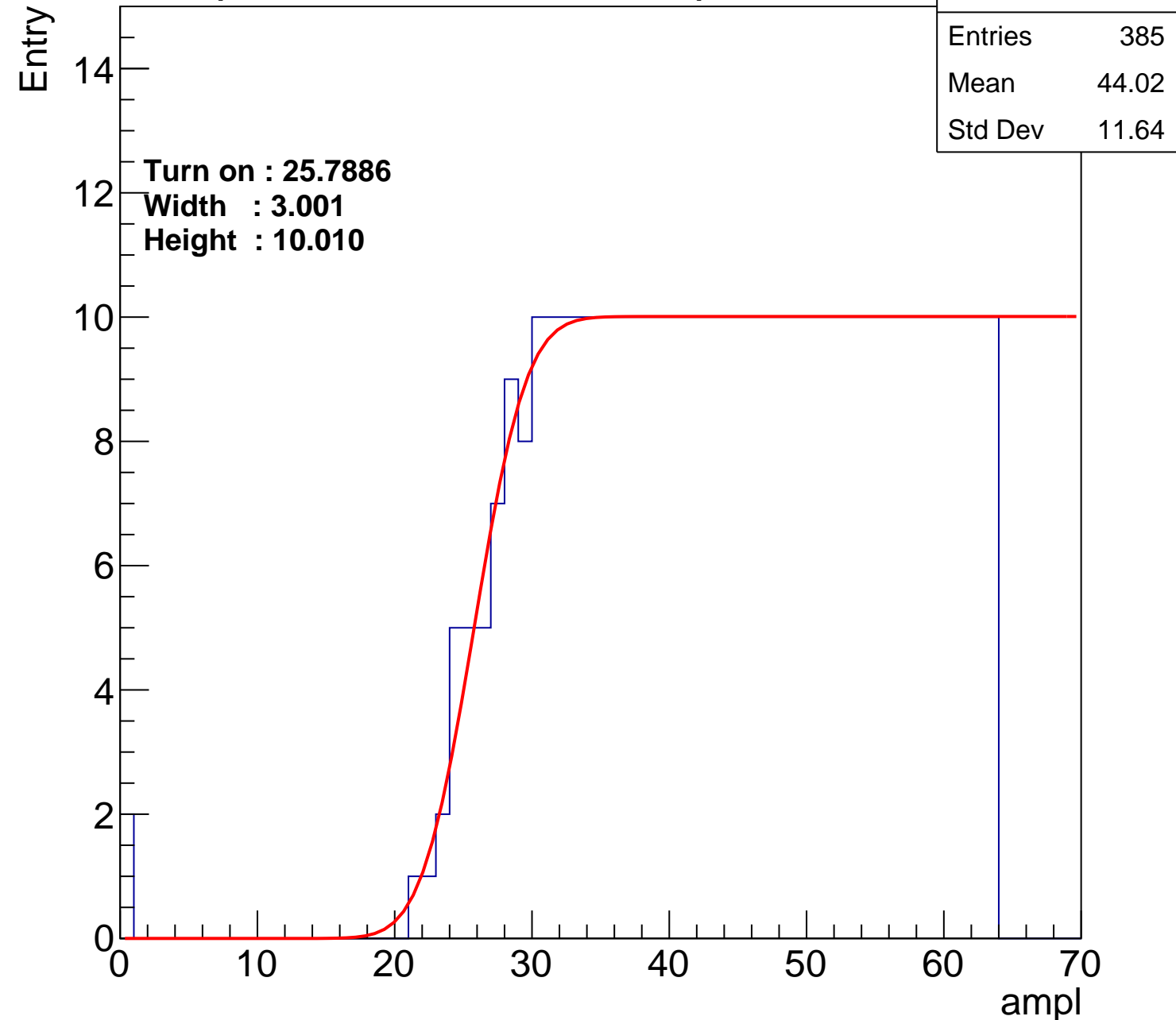
Width : 3.001

Height : 10.010

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch102

calib_packv5_042523_0143.root, FC#9, port A1

Entries	387
Mean	43.65
Std Dev	12.38

Turn on : 26.4493

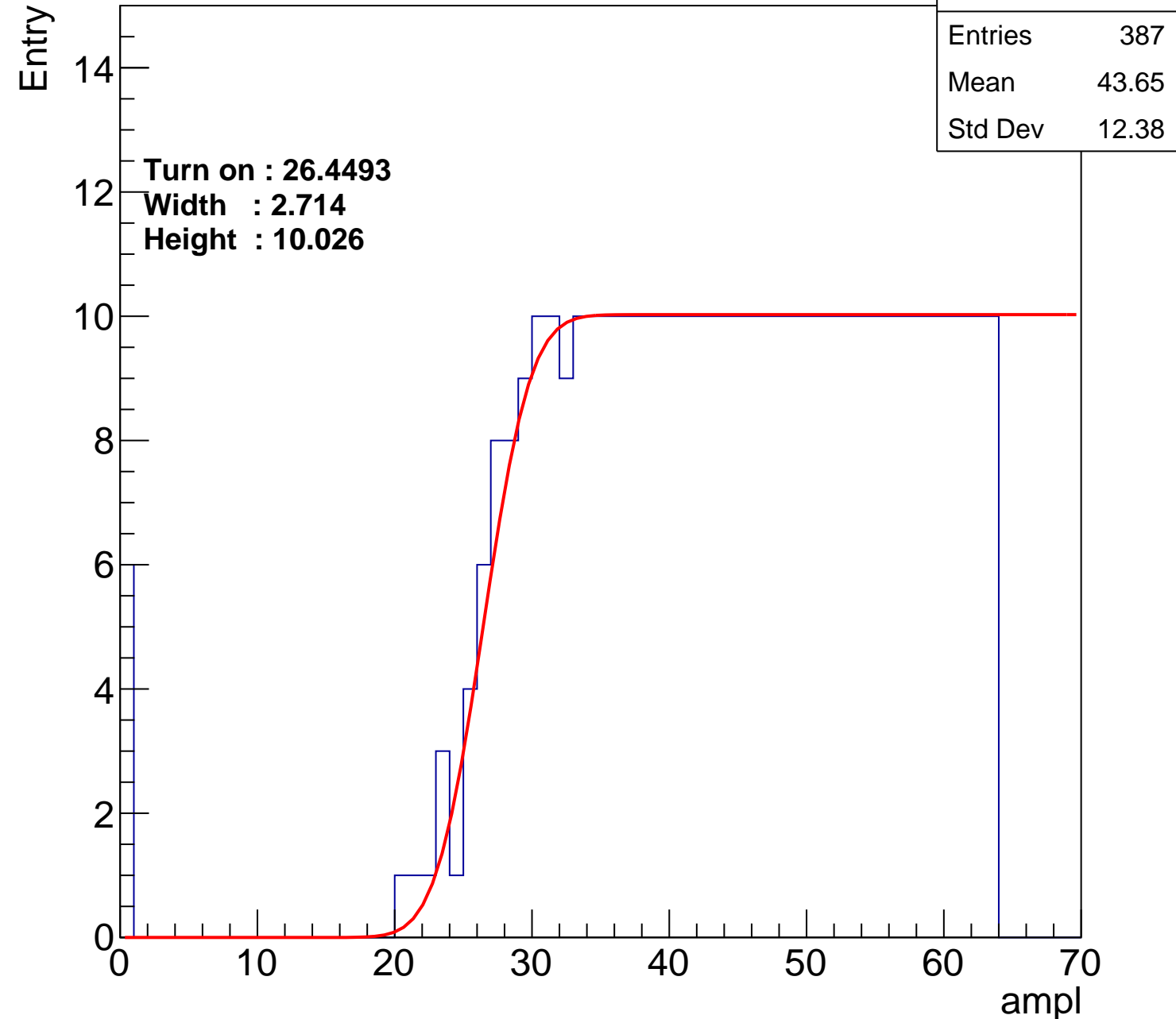
Width : 2.714

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch103

calib_packv5_042523_0143.root, FC#9, port A1

Entries	379
Mean	44.14
Std Dev	11.91

Turn on : 26.6416

Width : 3.937

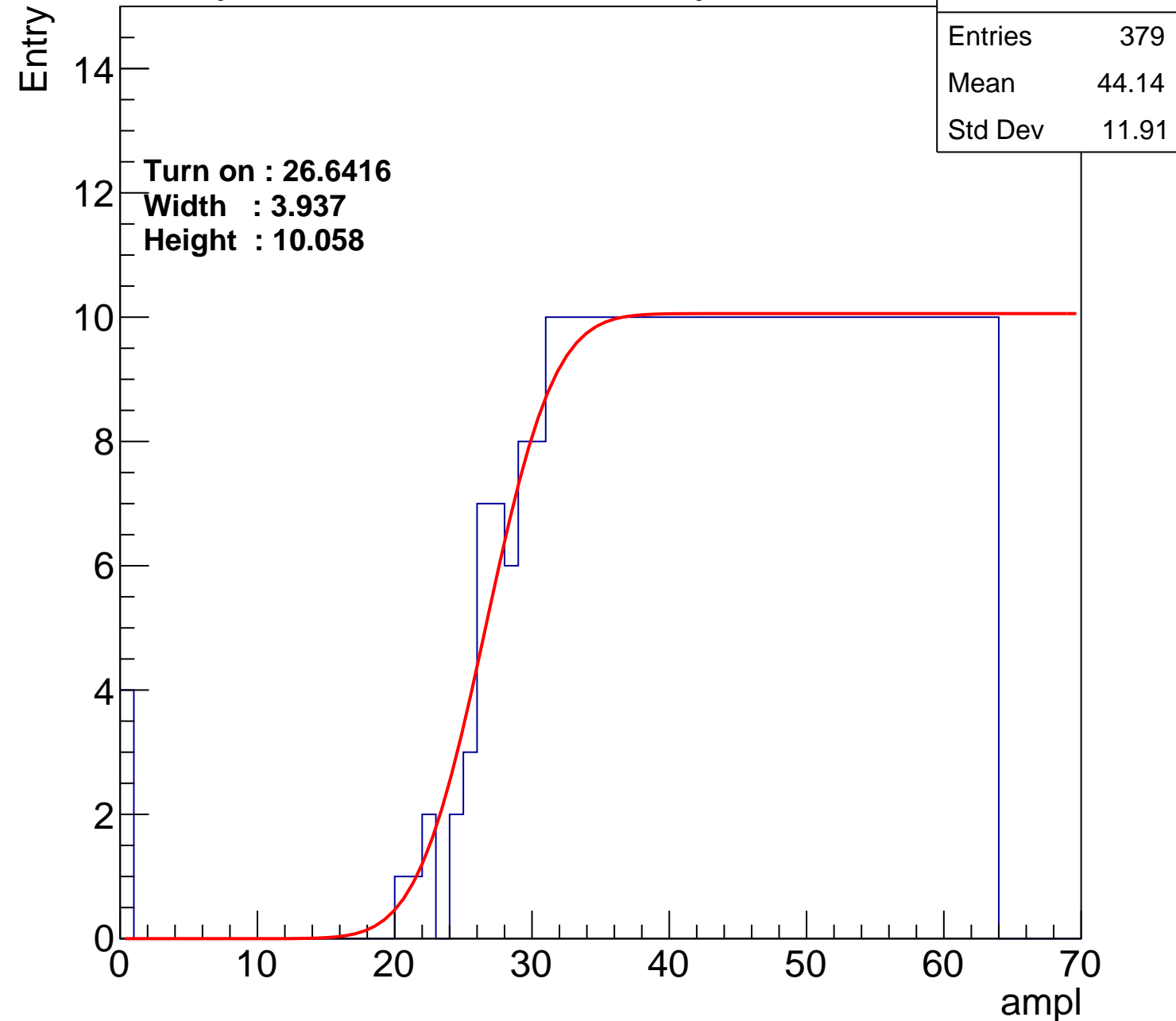
Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B0L001S, U1-ch104

calib_packv5_042523_0143.root, FC#9, port A1

Entries	373
Mean	44.51
Std Dev	11.56

Turn on : 26.9309

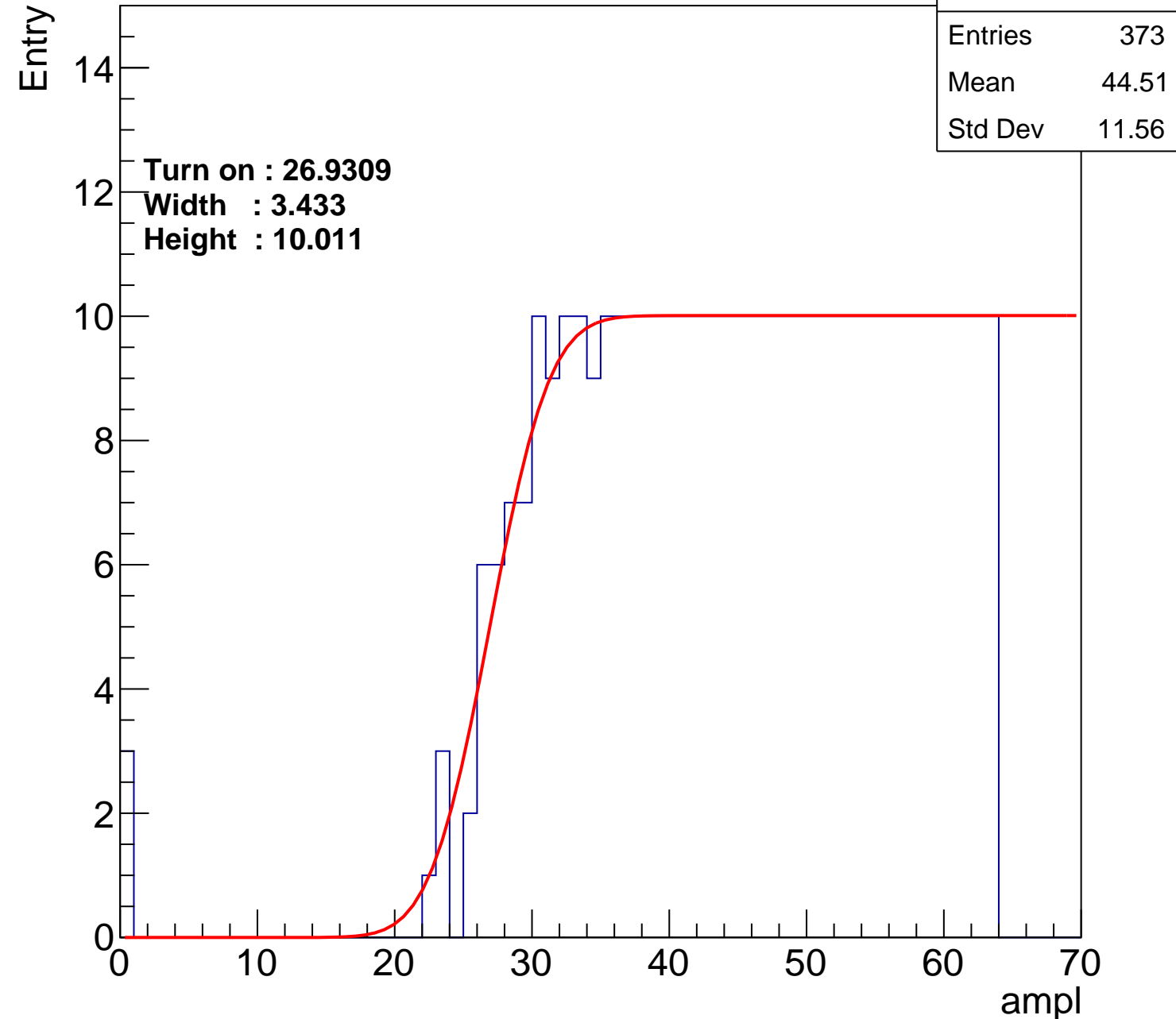
Width : 3.433

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch105

calib_packv5_042523_0143.root, FC#9, port A1

Entries	368
Mean	44.77
Std Dev	11.41

Turn on : 27.1009

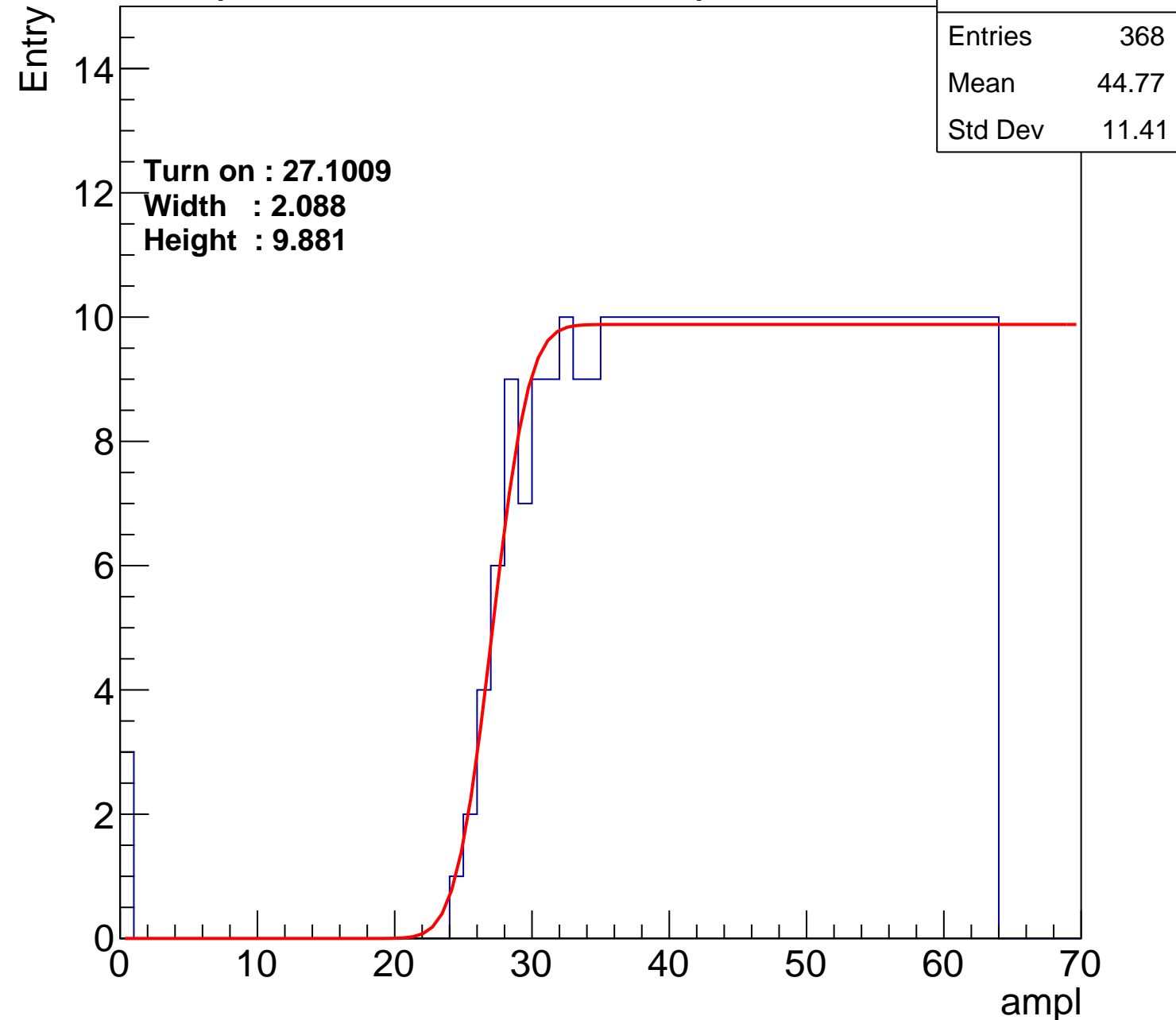
Width : 2.088

Height : 9.881

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch106

calib_packv5_042523_0143.root, FC#9, port A1

Entries	382
Mean	43.98
Std Dev	11.94

Turn on : 26.0952

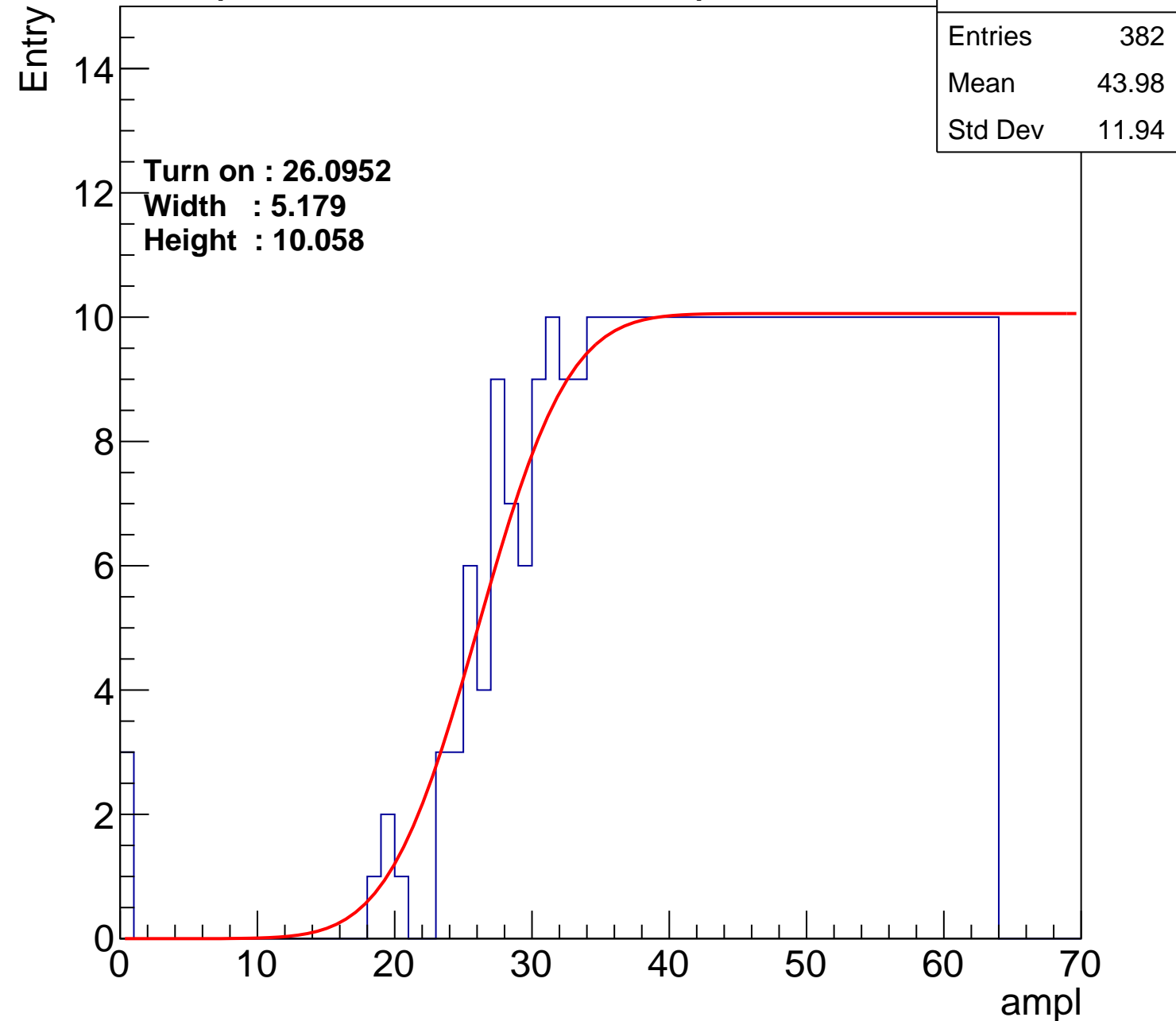
Width : 5.179

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch107

calib_packv5_042523_0143.root, FC#9, port A1

Entries	380
Mean	44.21
Std Dev	11.6

Turn on : 26.2477

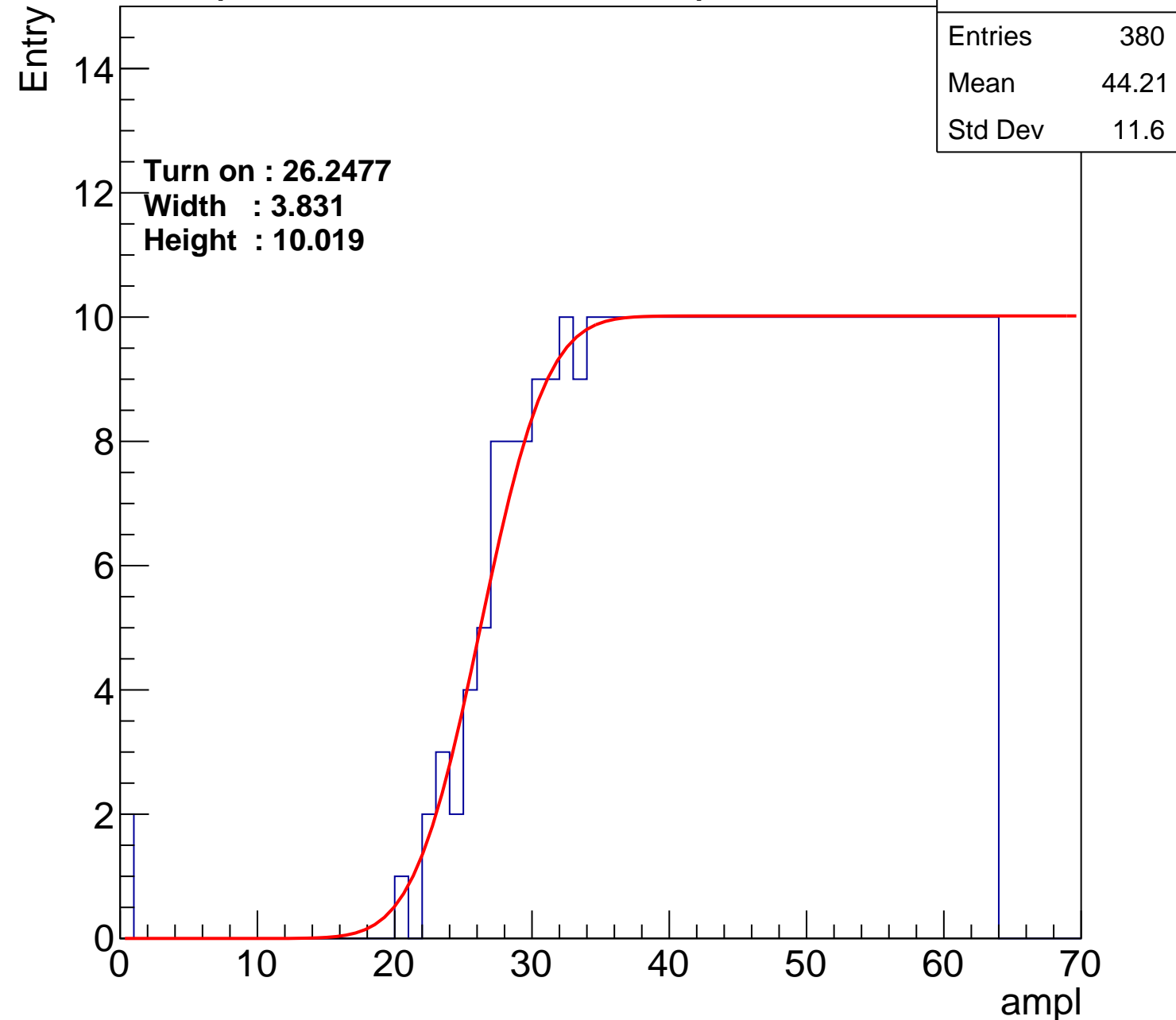
Width : 3.831

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch108

calib_packv5_042523_0143.root, FC#9, port A1

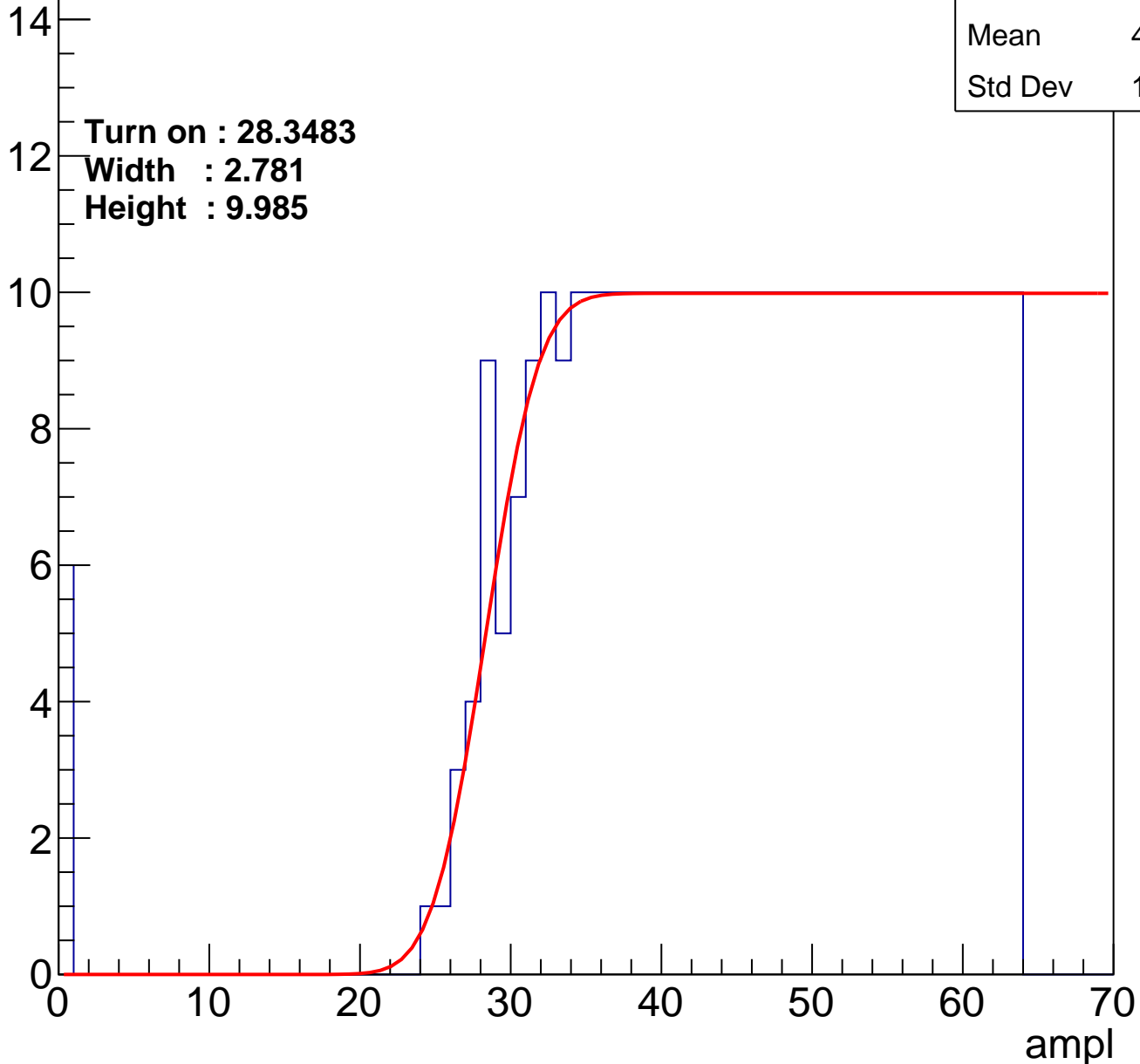
Entries	364
Mean	44.75
Std Dev	11.92

Turn on : 28.3483

Width : 2.781

Height : 9.985

Entry



B0L001S, U1-ch109

calib_packv5_042523_0143.root, FC#9, port A1

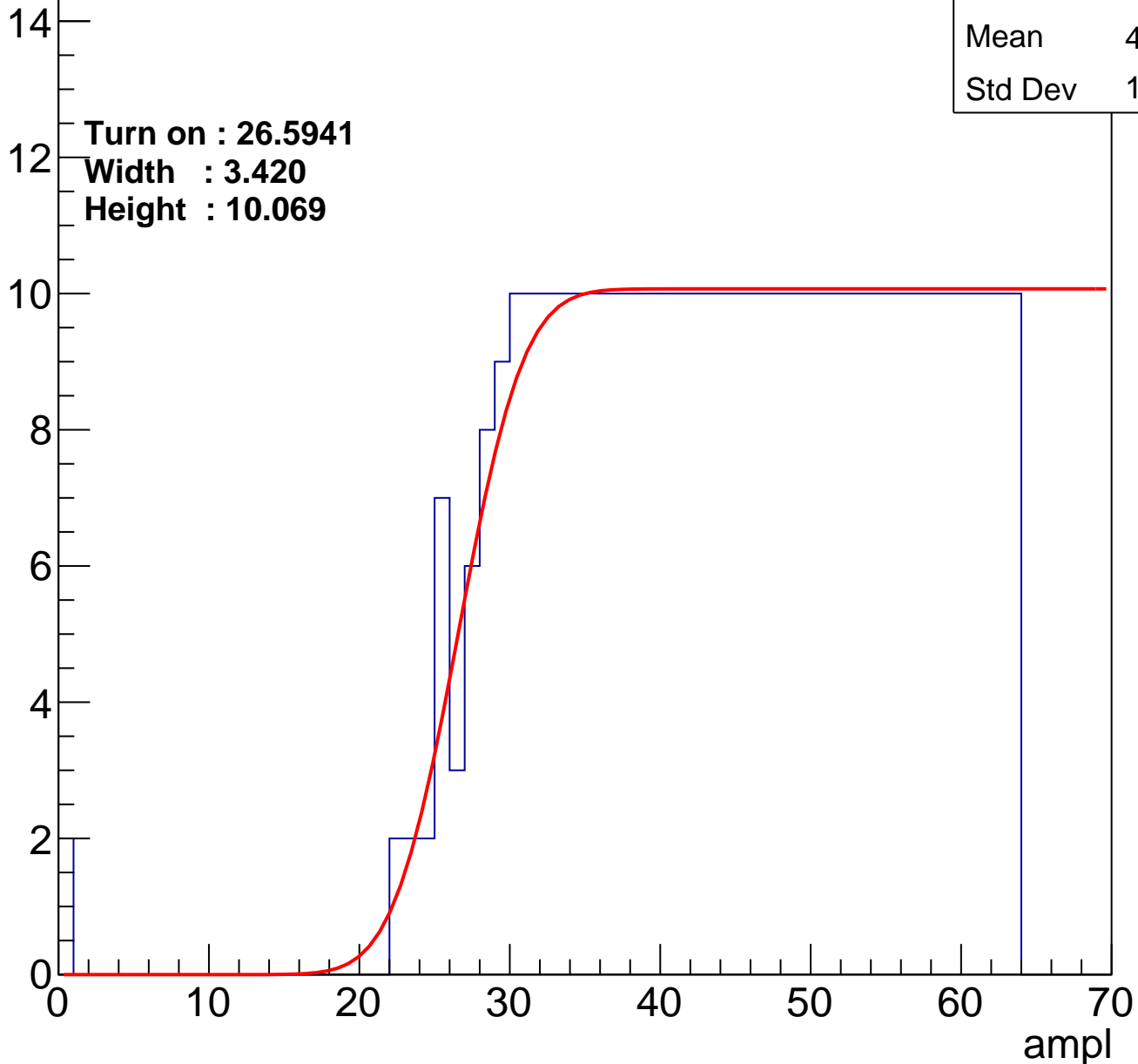
Entries	381
Mean	44.22
Std Dev	11.53

Turn on : 26.5941

Width : 3.420

Height : 10.069

Entry



B0L001S, U1-ch110

calib_packv5_042523_0143.root, FC#9, port A1

Entries	389
Mean	43.52
Std Dev	12.47

Turn on : 25.8322

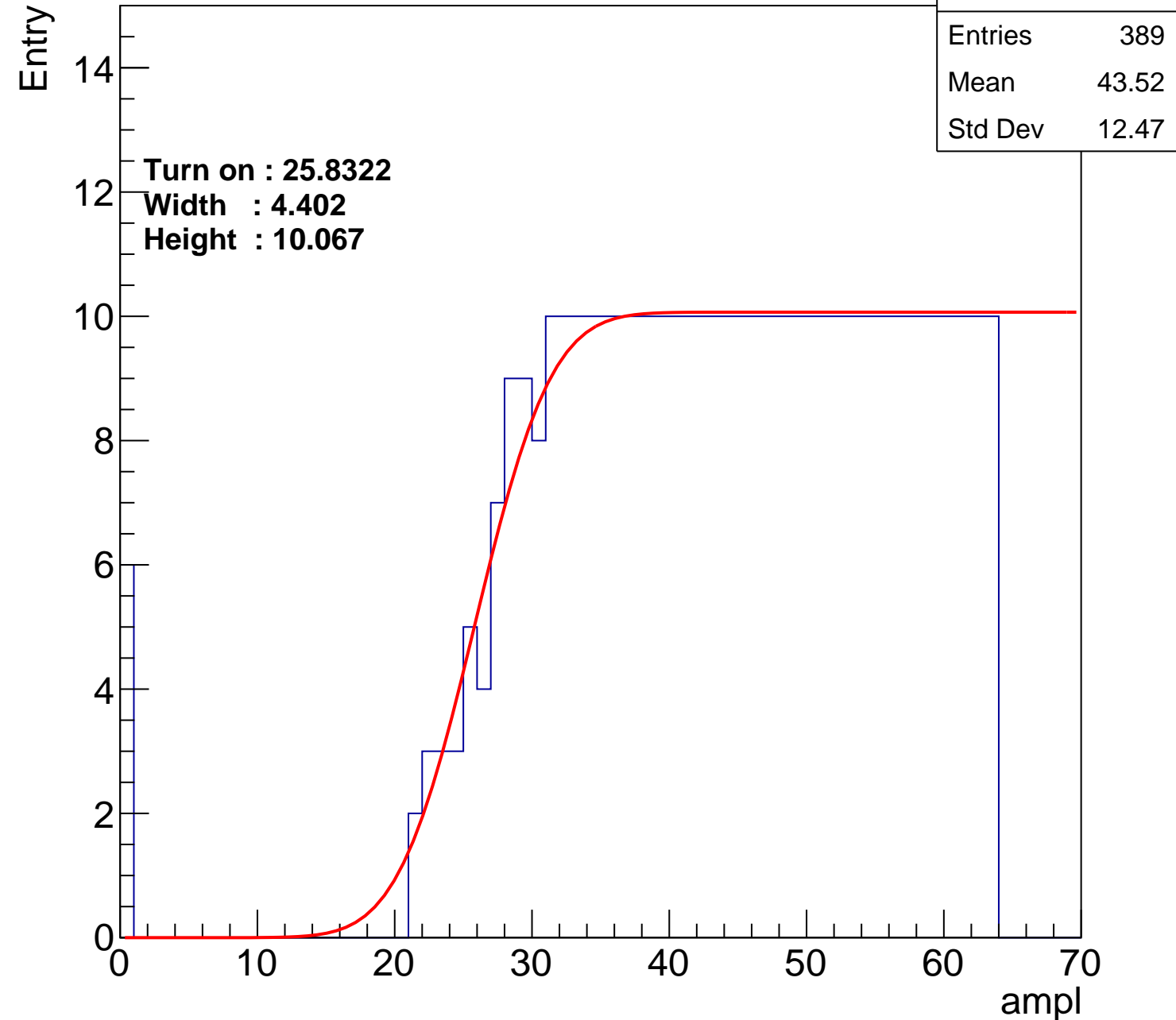
Width : 4.402

Height : 10.067

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch111

calib_packv5_042523_0143.root, FC#9, port A1

Entries	358
Mean	44.96
Std Dev	11.91

Turn on : 29.4757

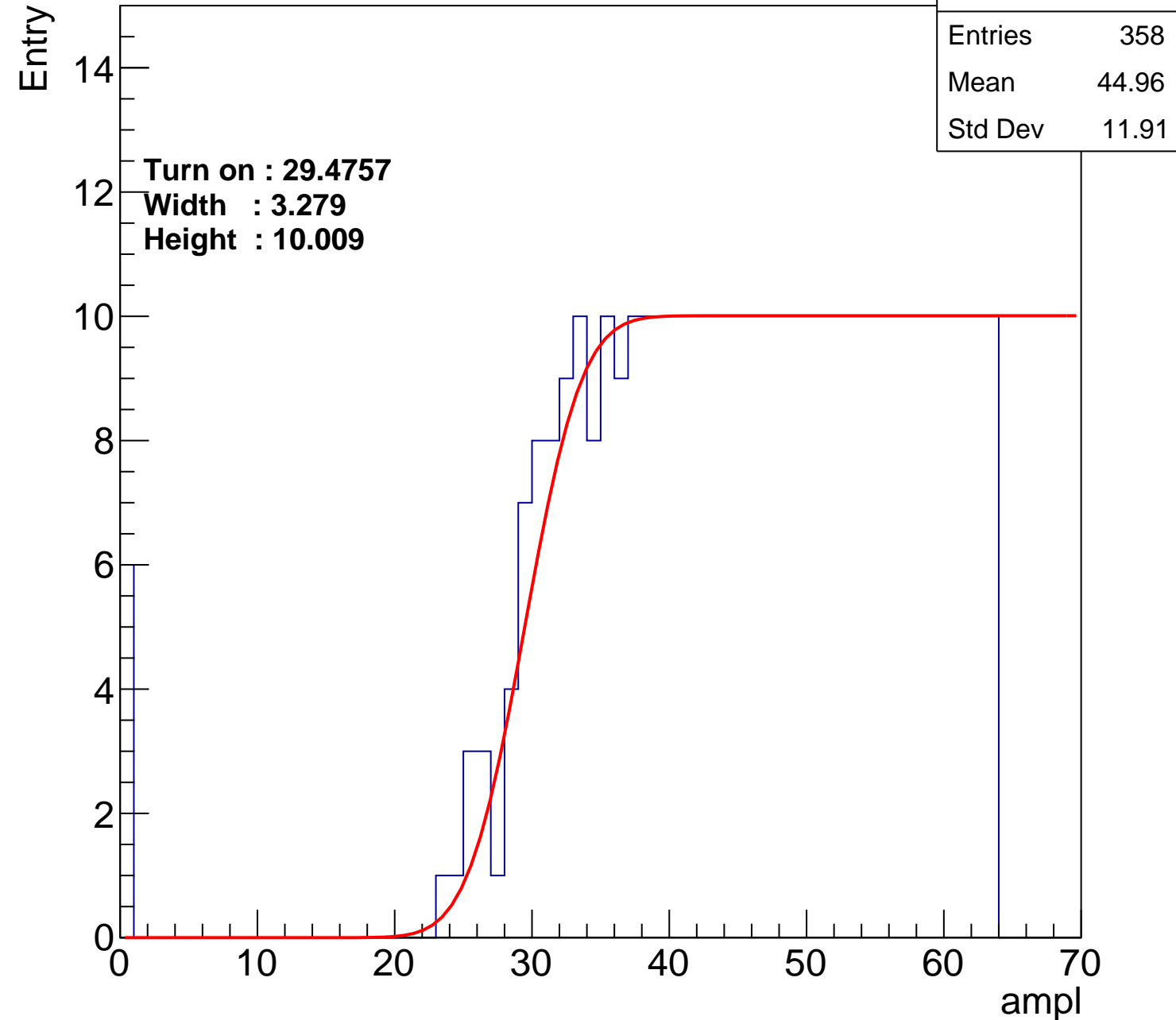
Width : 3.279

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch112

calib_packv5_042523_0143.root, FC#9, port A1

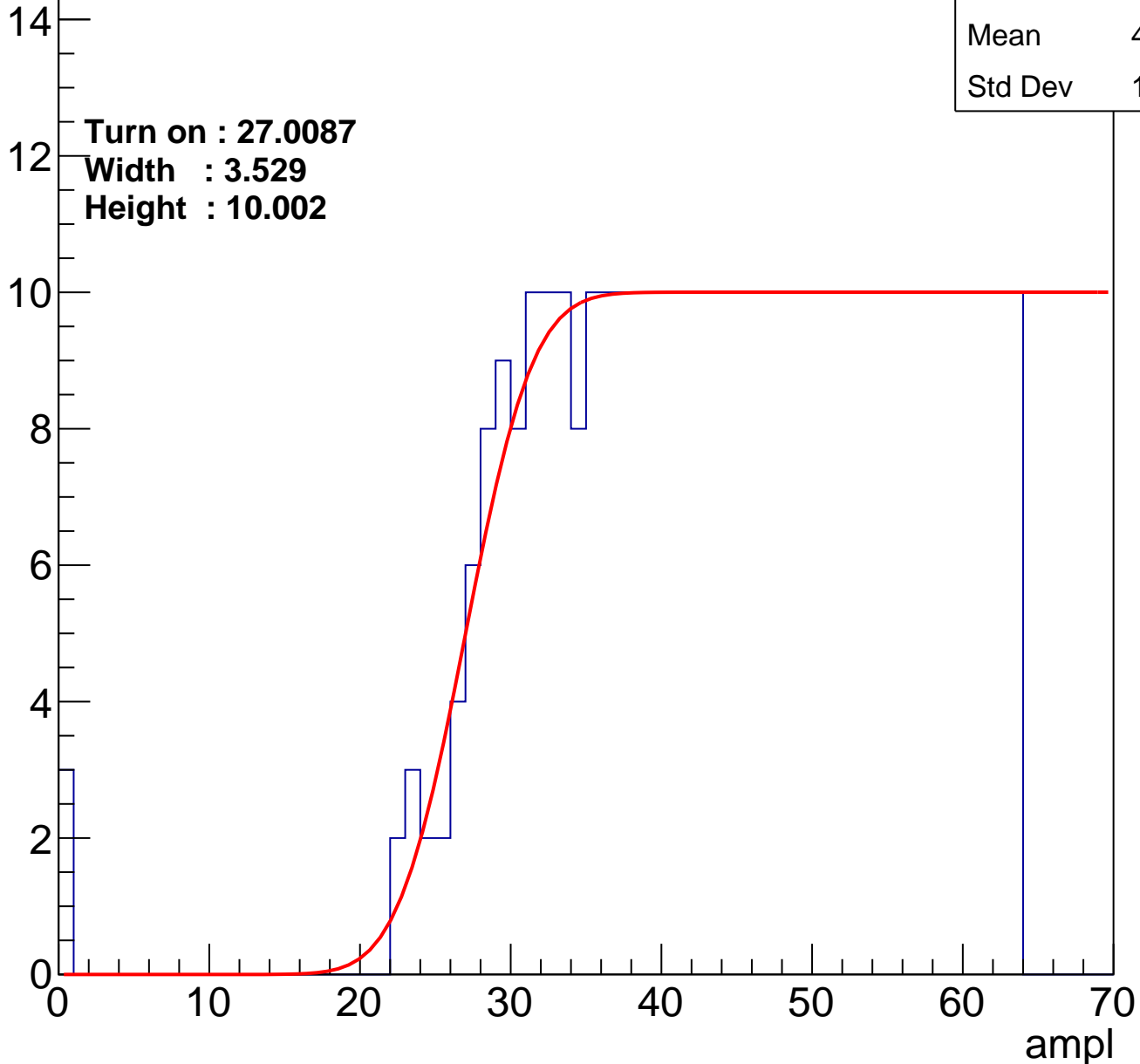
Entries	375
Mean	44.38
Std Dev	11.65

Turn on : 27.0087

Width : 3.529

Height : 10.002

Entry



B0L001S, U1-ch113

calib_packv5_042523_0143.root, FC#9, port A1

Entries	360
Mean	45.33
Std Dev	10.77

Turn on : 28.1798

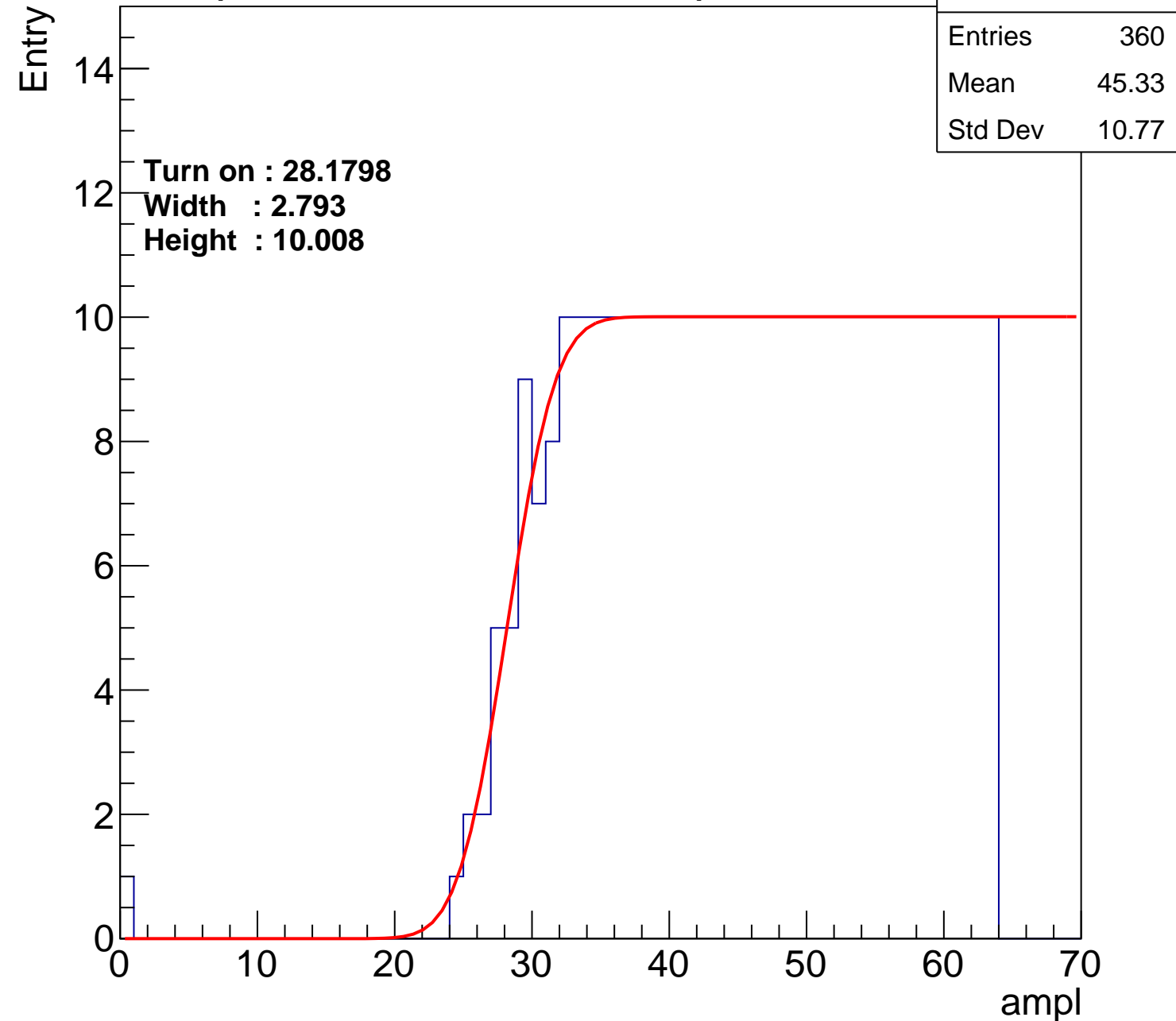
Width : 2.793

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch114

calib_packv5_042523_0143.root, FC#9, port A1

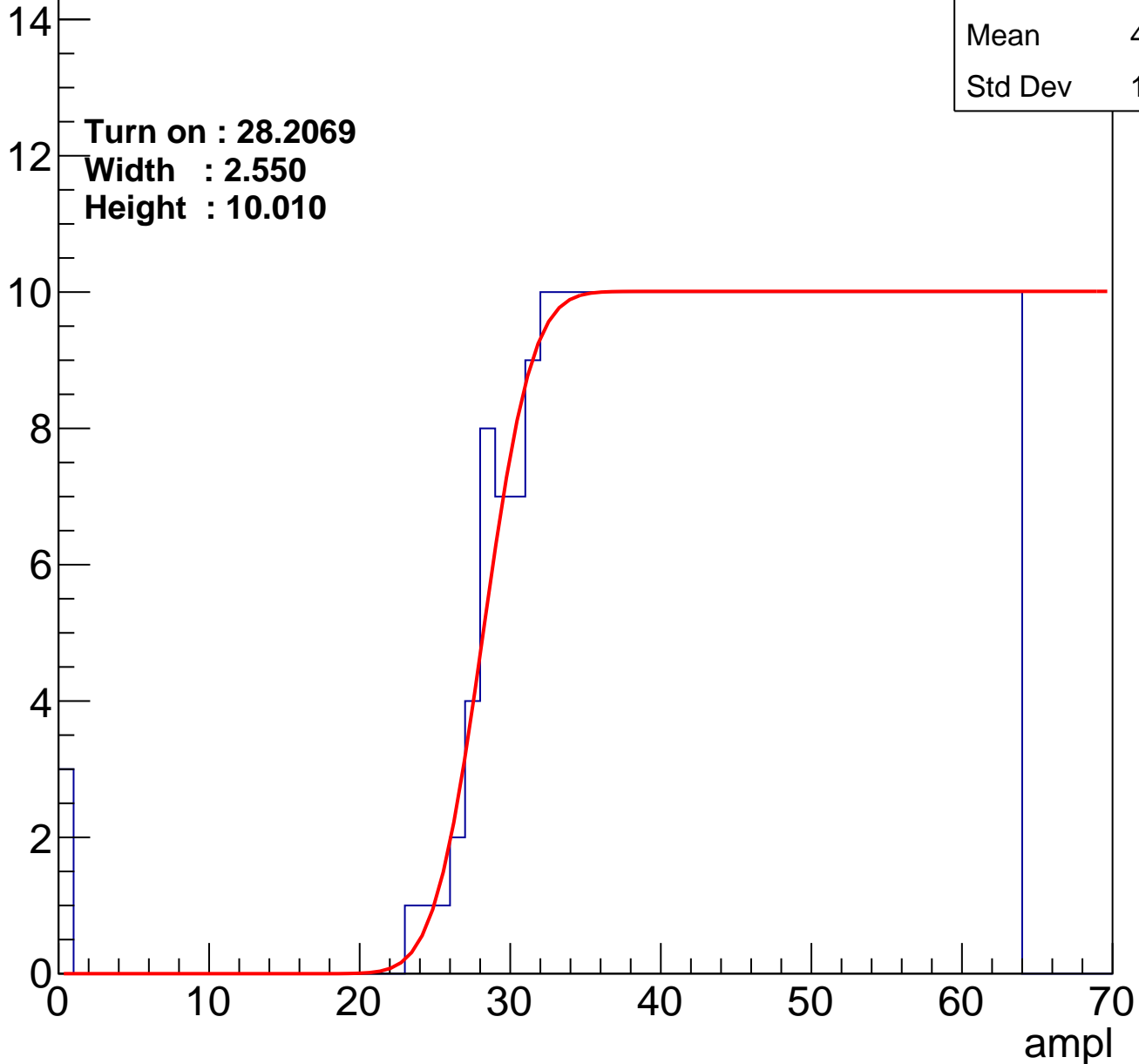
Entries	363
Mean	45.04
Std Dev	11.27

Turn on : 28.2069

Width : 2.550

Height : 10.010

Entry



B0L001S, U1-ch115

calib_packv5_042523_0143.root, FC#9, port A1

Entries	380
Mean	44.16
Std Dev	11.74

Turn on : 26.1205

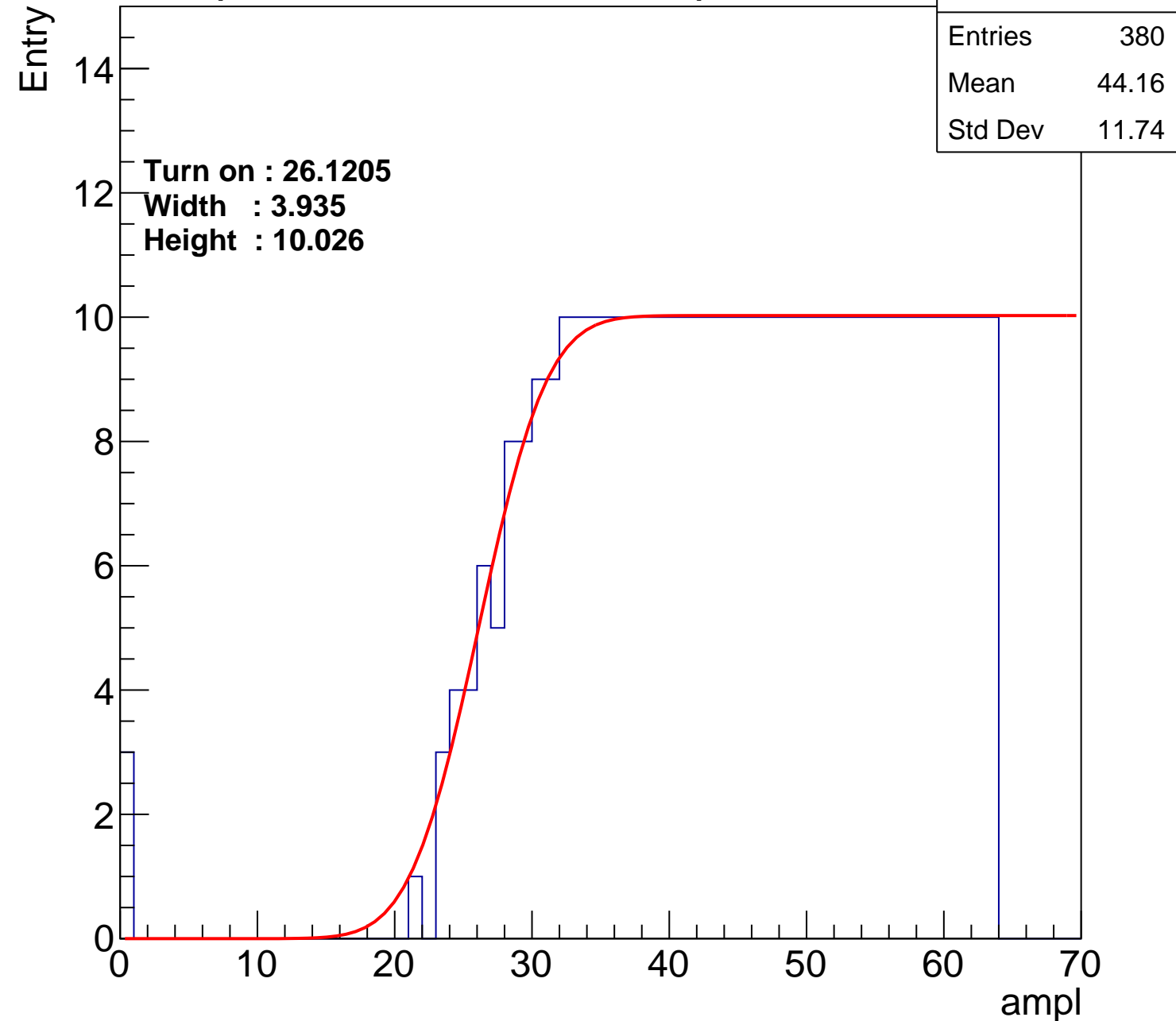
Width : 3.935

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch116

calib_packv5_042523_0143.root, FC#9, port A1

Entries	393
Mean	43.34
Std Dev	12.59

Turn on : 25.5573

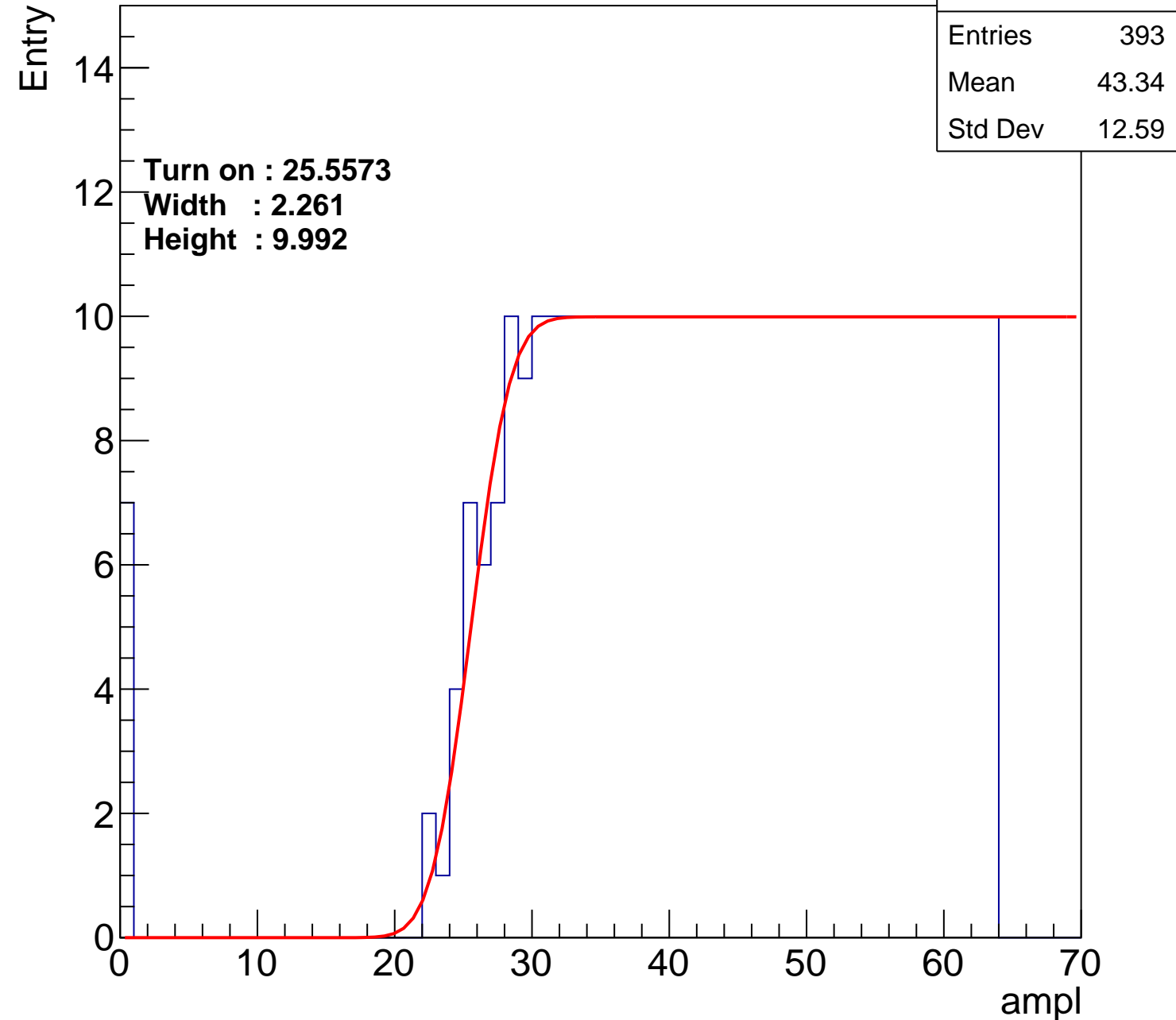
Width : 2.261

Height : 9.992

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch117

calib_packv5_042523_0143.root, FC#9, port A1

Entries	366
Mean	44.75
Std Dev	11.64

Turn on : 27.8272

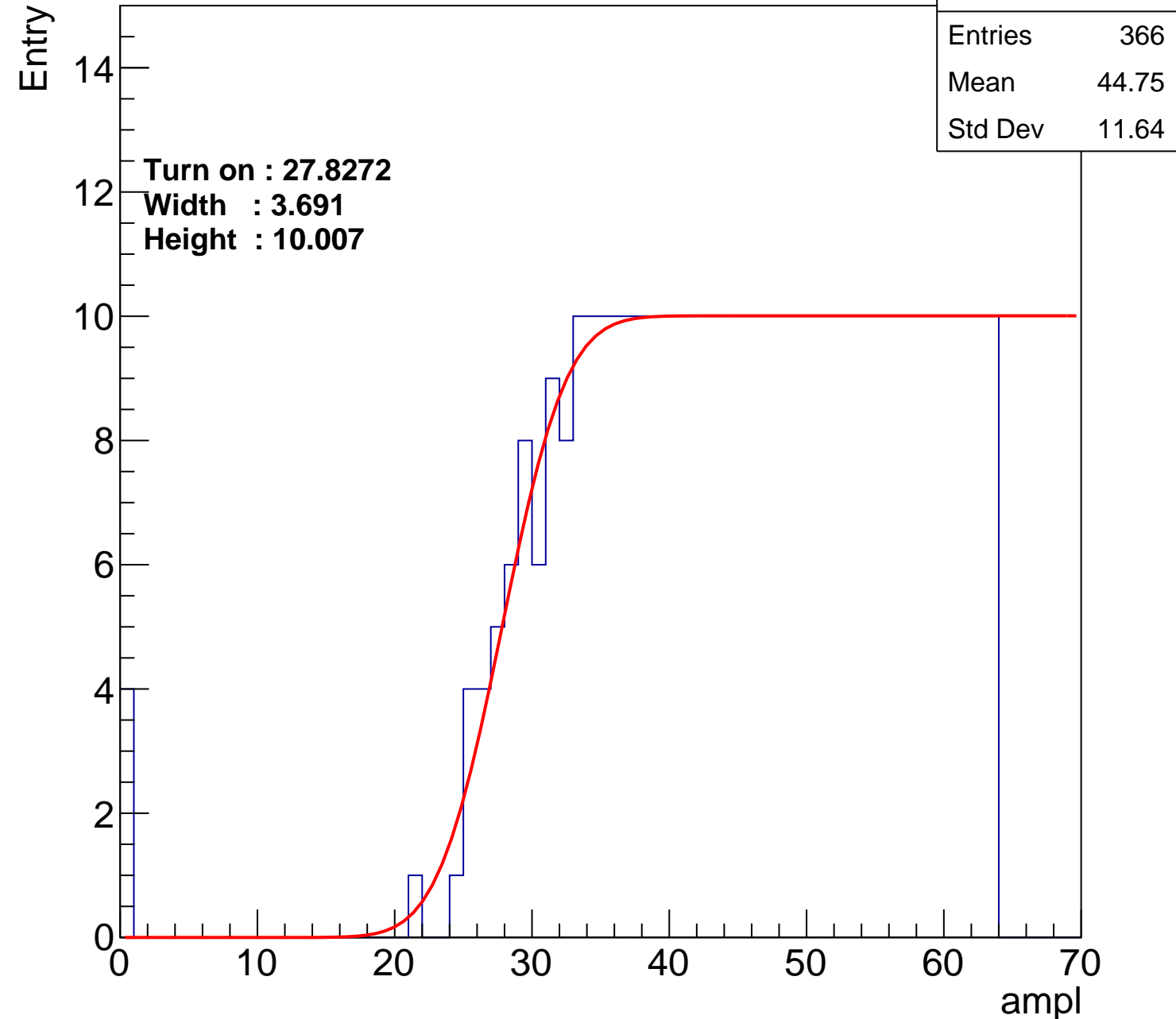
Width : 3.691

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch118

calib_packv5_042523_0143.root, FC#9, port A1

Entries	362
Mean	45.22
Std Dev	10.84

Turn on : 27.6230

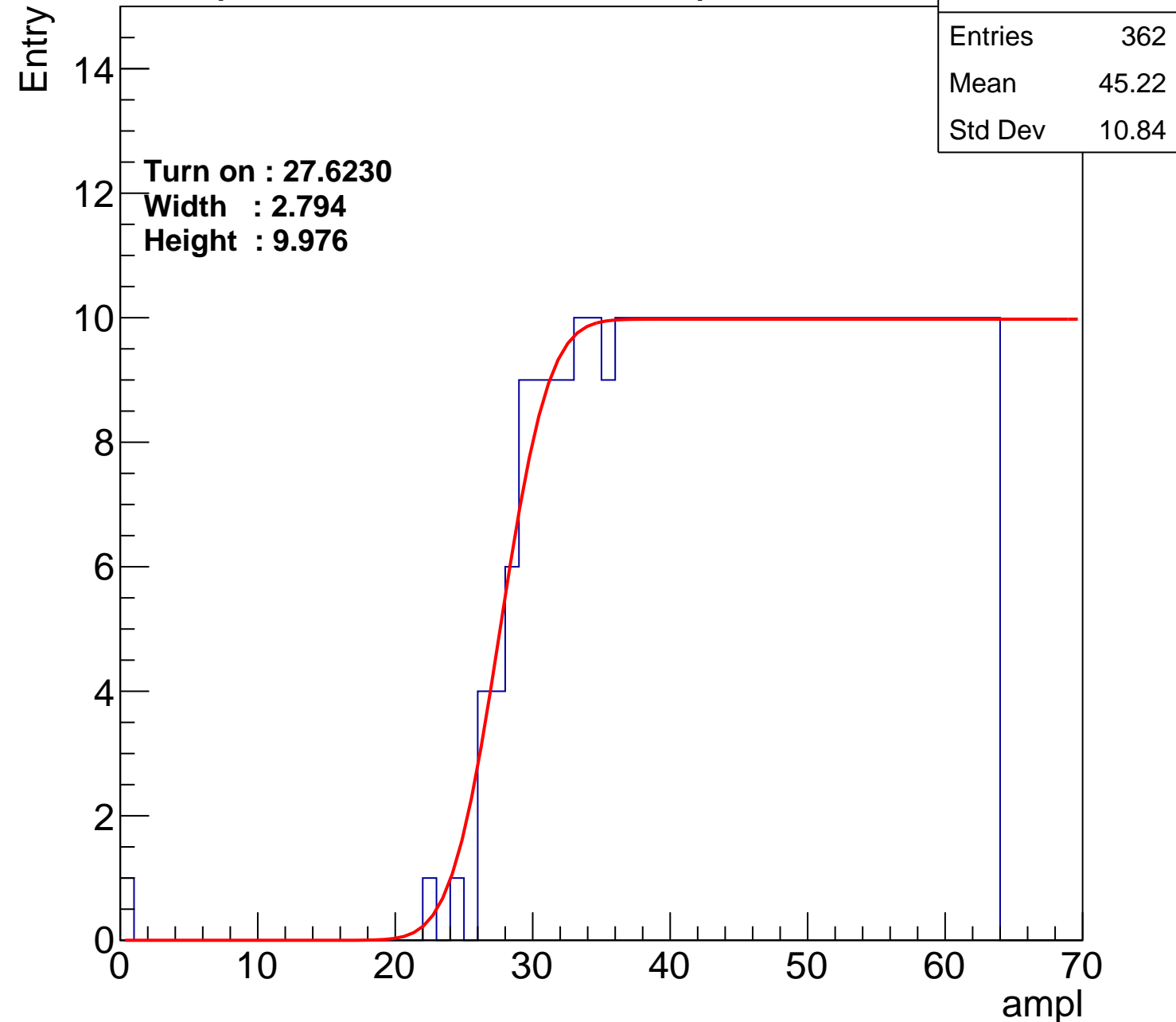
Width : 2.794

Height : 9.976

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch119

calib_packv5_042523_0143.root, FC#9, port A1

Entries	359
Mean	45.09
Std Dev	11.48

Turn on : 28.5982

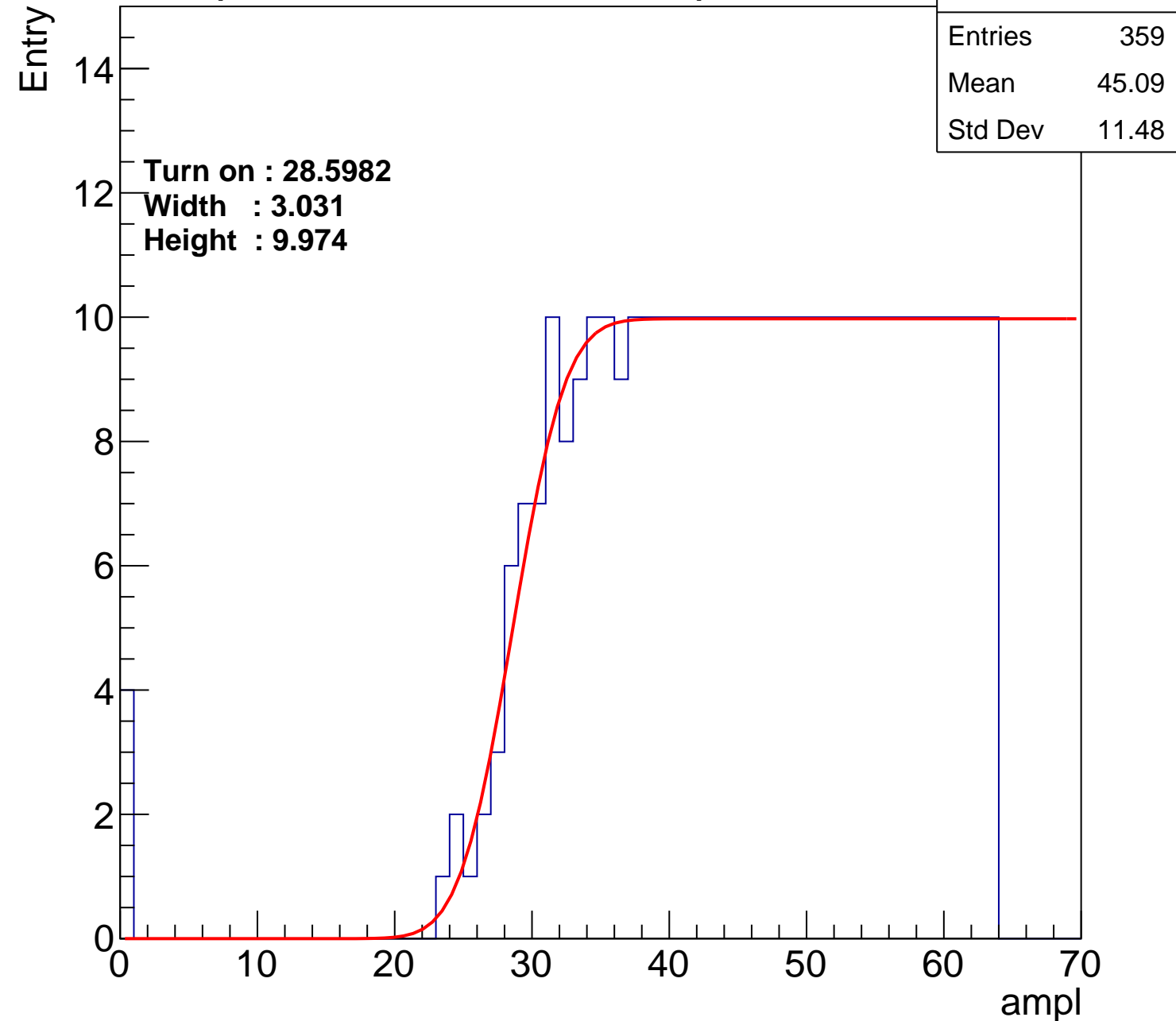
Width : 3.031

Height : 9.974

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch120

calib_packv5_042523_0143.root, FC#9, port A1

Entries	361
Mean	44.99
Std Dev	11.54

Turn on : 28.1833

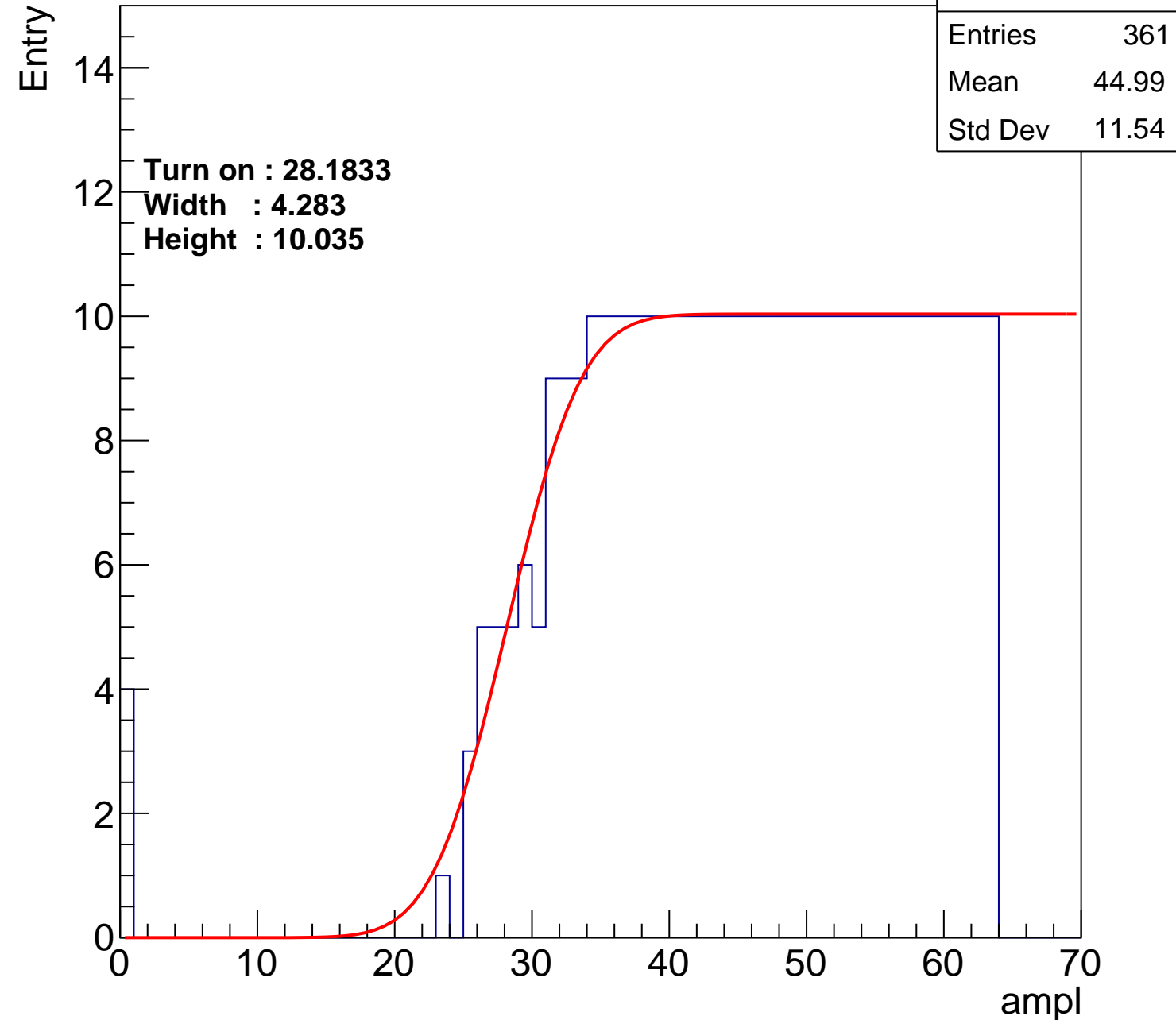
Width : 4.283

Height : 10.035

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch121

calib_packv5_042523_0143.root, FC#9, port A1

Entries	343
Mean	45.99
Std Dev	10.74

Turn on : 30.6002

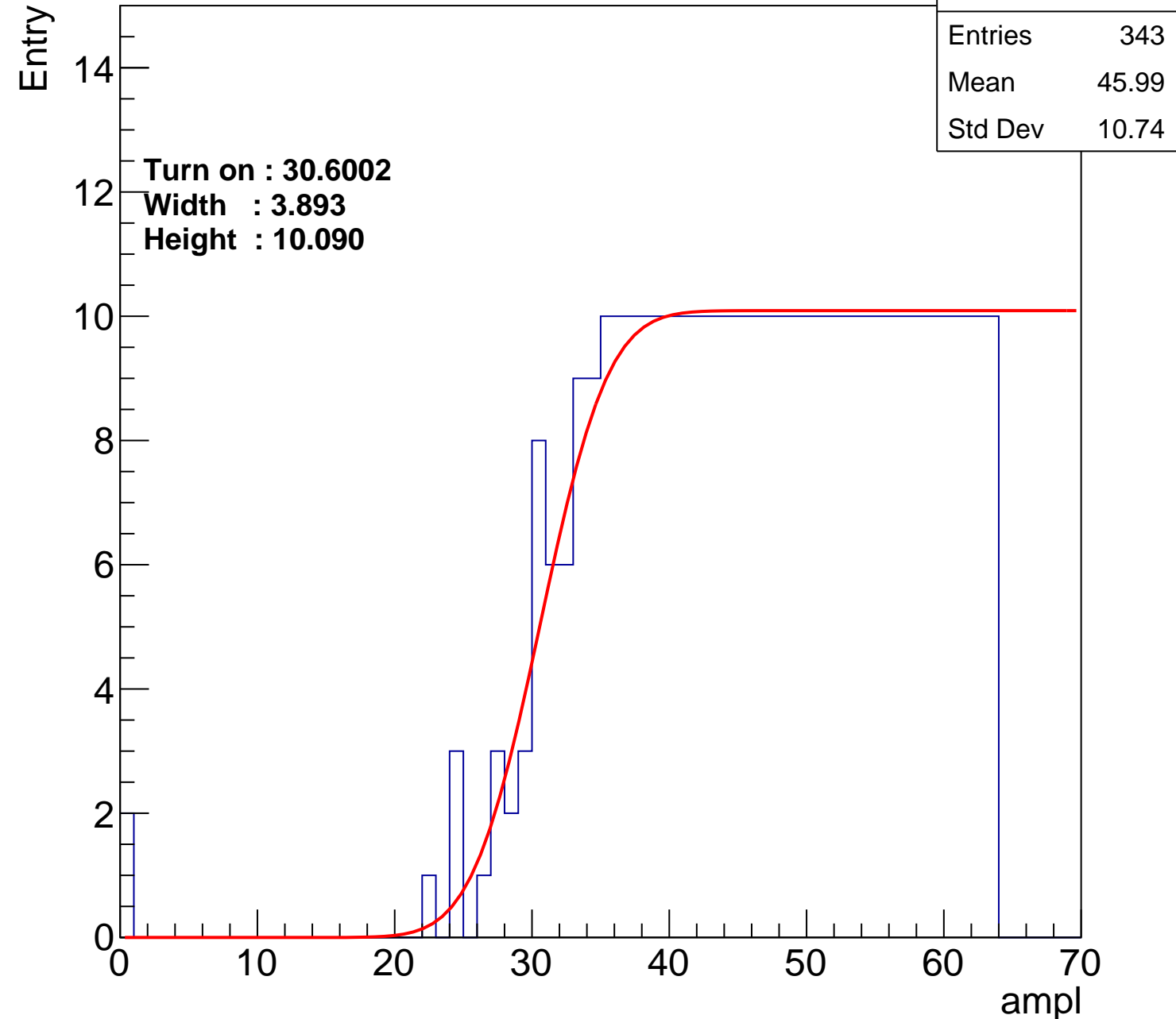
Width : 3.893

Height : 10.090

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch122

calib_packv5_042523_0143.root, FC#9, port A1

Entries	351
Mean	45.75
Std Dev	10.57

Turn on : 28.9920

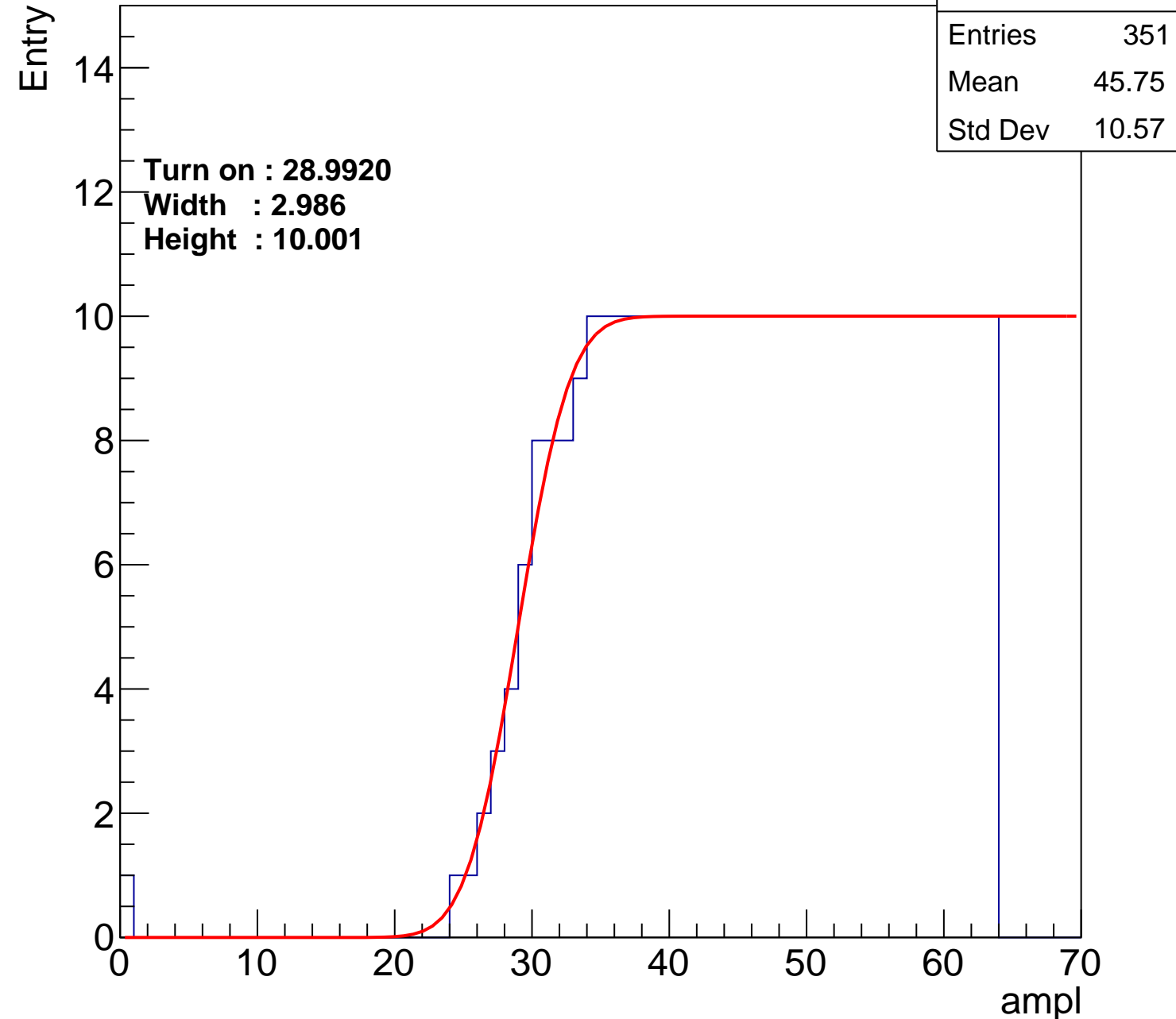
Width : 2.986

Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch123

calib_packv5_042523_0143.root, FC#9, port A1

Entries	376
Mean	44.47
Std Dev	11.41

Turn on : 26.9630

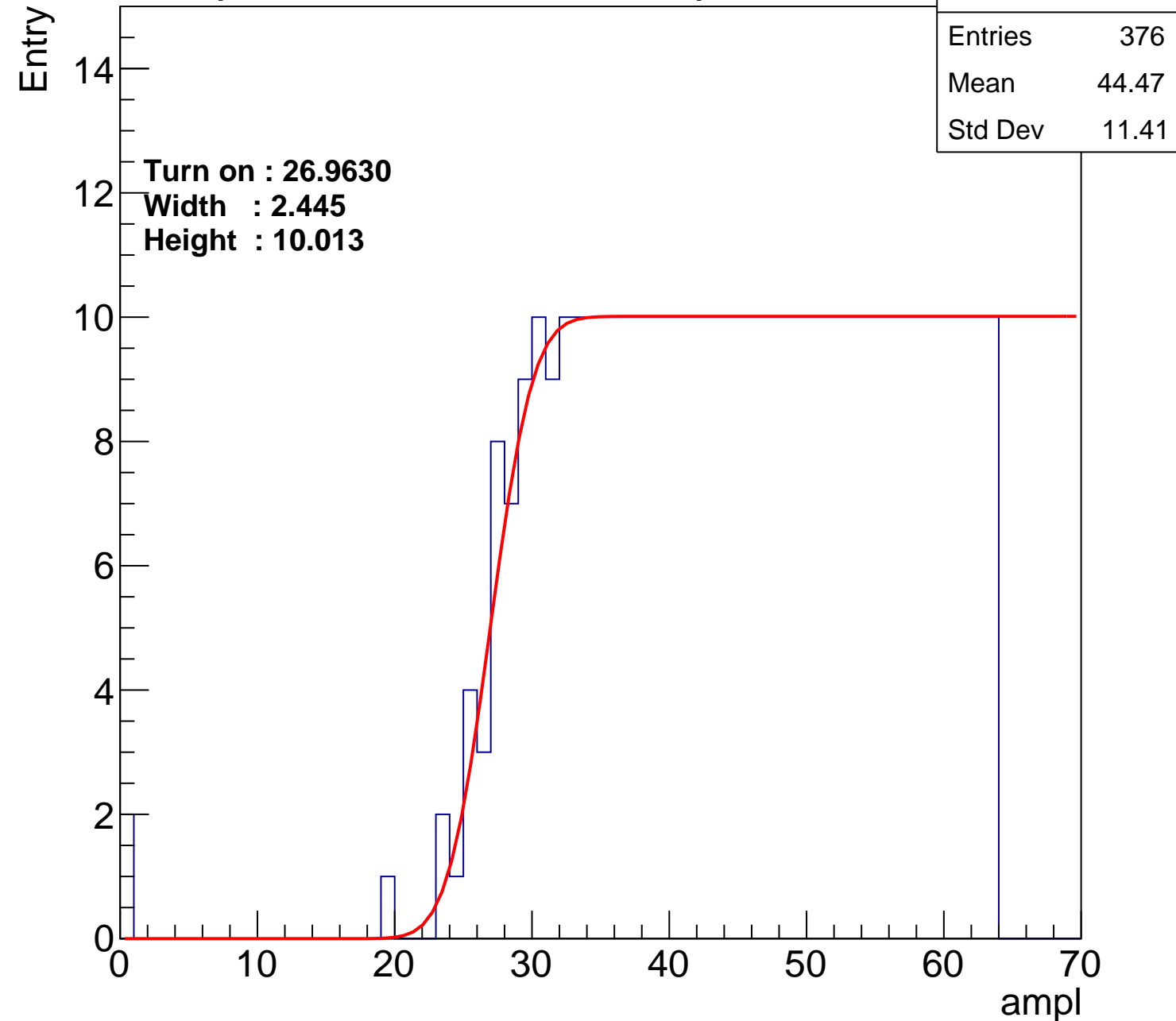
Width : 2.445

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch124

calib_packv5_042523_0143.root, FC#9, port A1

Entries	381
Mean	44.09
Std Dev	11.87

Turn on : 25.9365

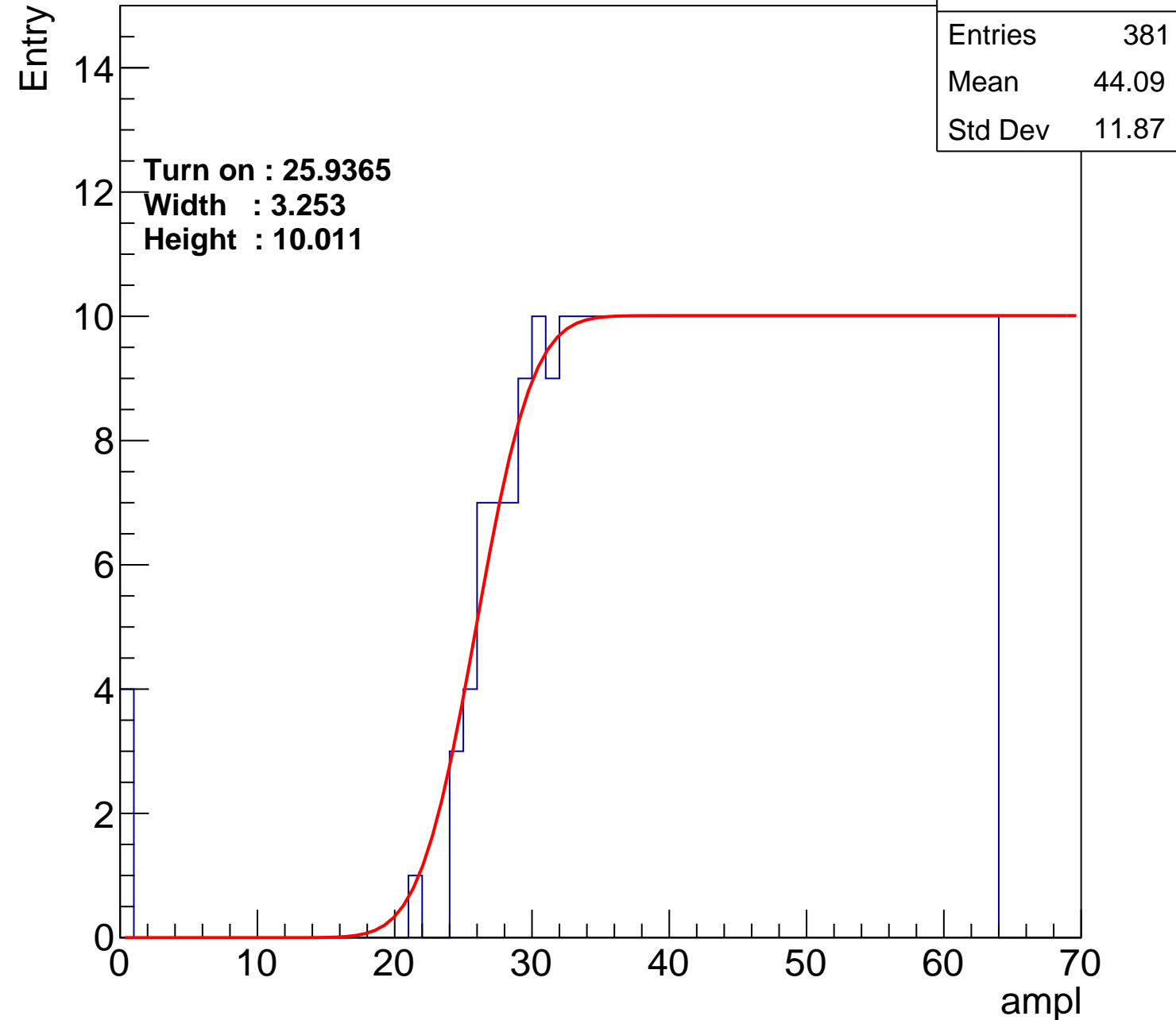
Width : 3.253

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch125

calib_packv5_042523_0143.root, FC#9, port A1

Entries	358
Mean	45.12
Std Dev	11.5

Turn on : 29.0757

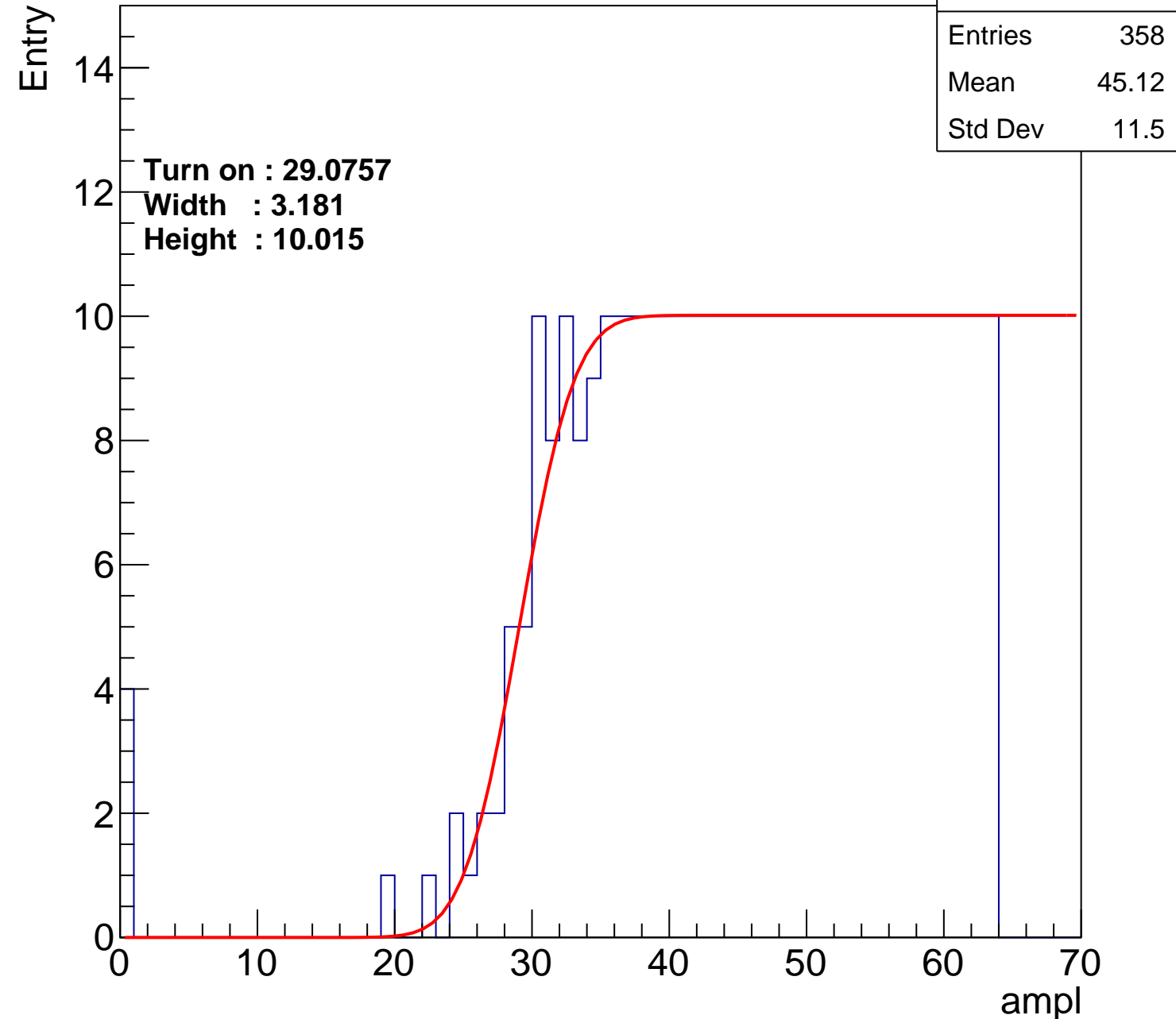
Width : 3.181

Height : 10.015

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch126

calib_packv5_042523_0143.root, FC#9, port A1

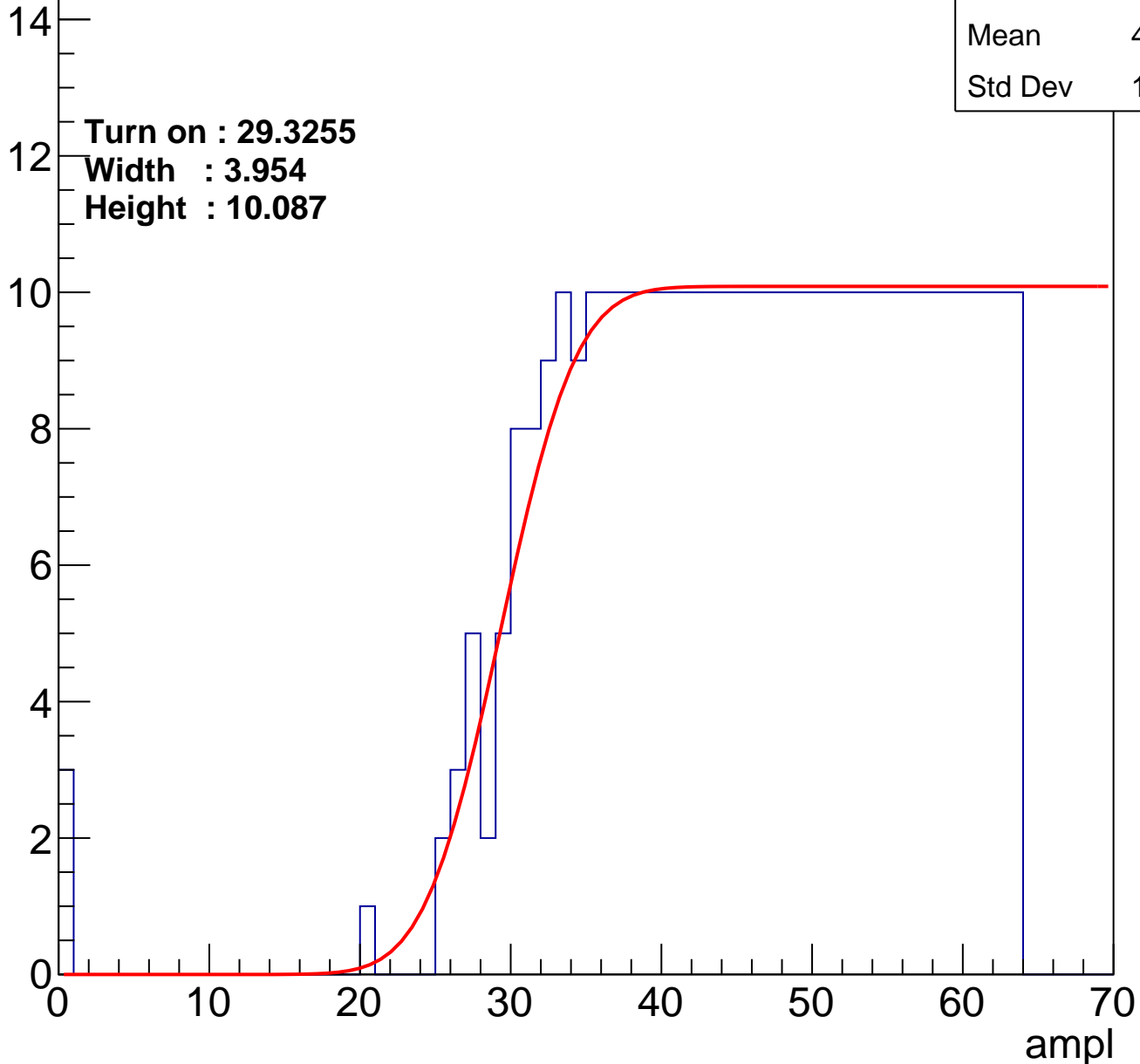
Entries	355
Mean	45.37
Std Dev	11.18

Turn on : 29.3255

Width : 3.954

Height : 10.087

Entry



B0L001S, U1-ch127

calib_packv5_042523_0143.root, FC#9, port A1

Entries	363
Mean	44.92
Std Dev	11.54

Turn on : 28.2908

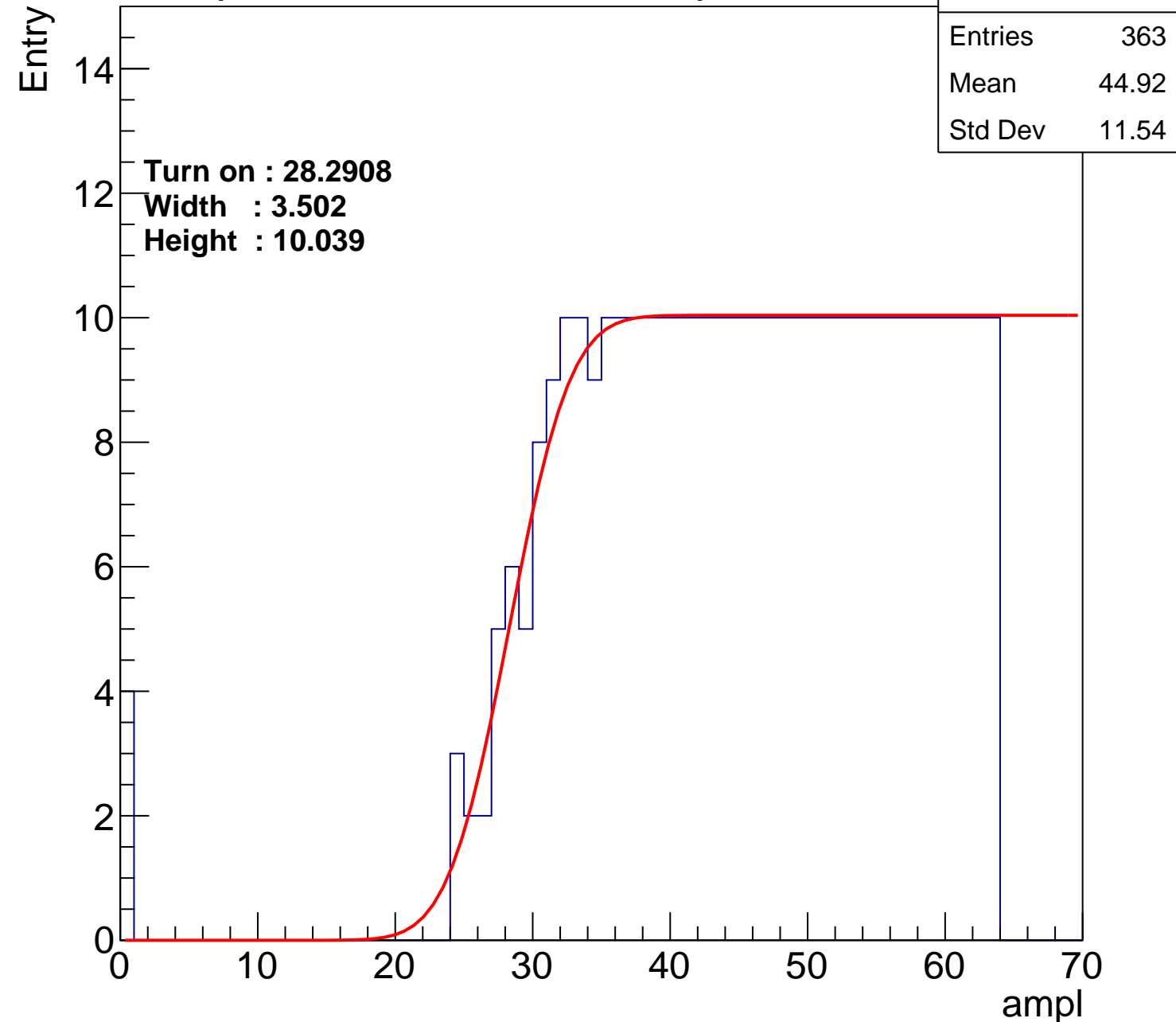
Width : 3.502

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B0L001S, U1-ch127

calib_packv5_042523_0143.root, FC#9, port A1

Entries	363
Mean	44.92
Std Dev	11.54

Turn on : 28.2908

Width : 3.502

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl

