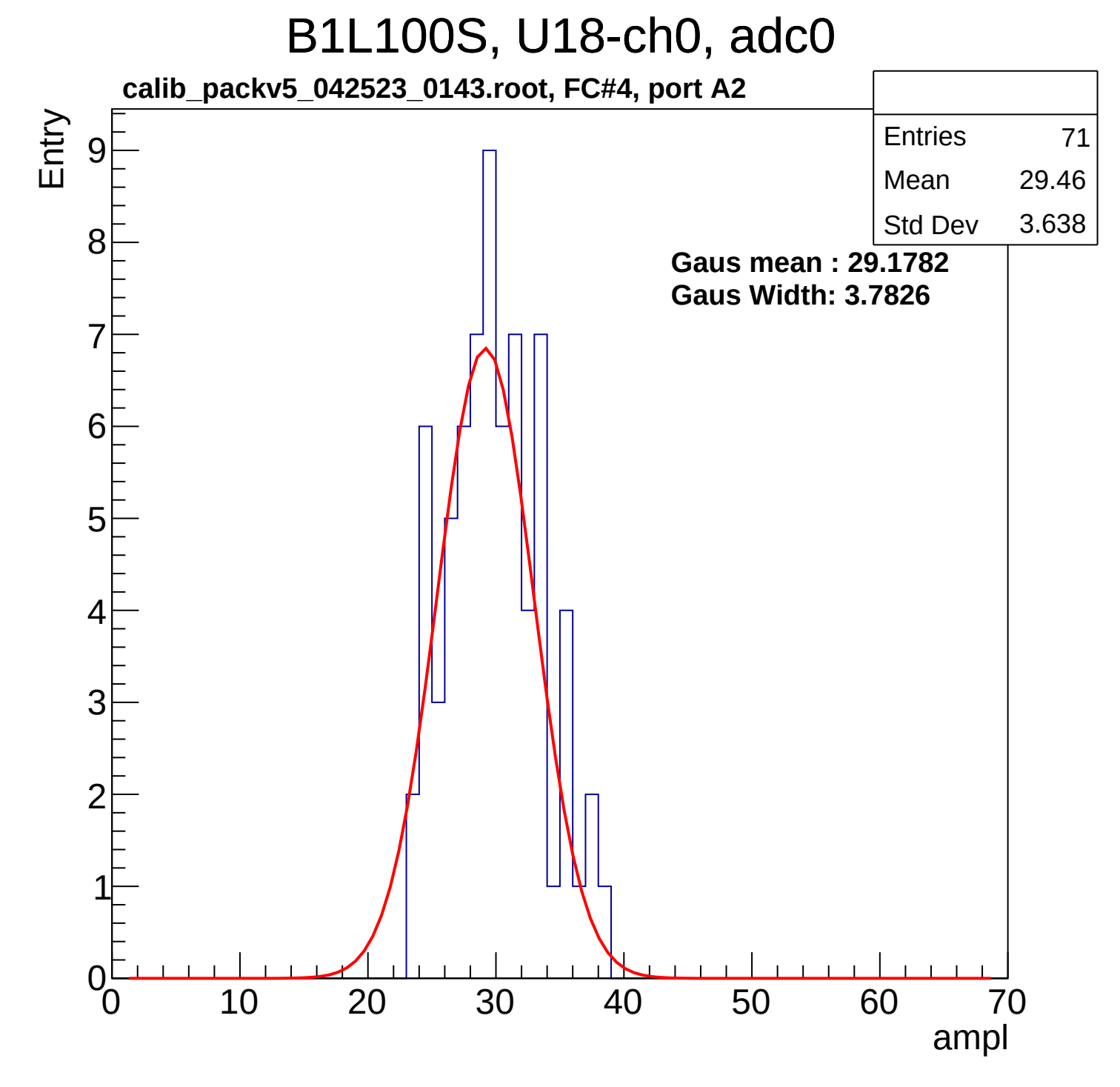
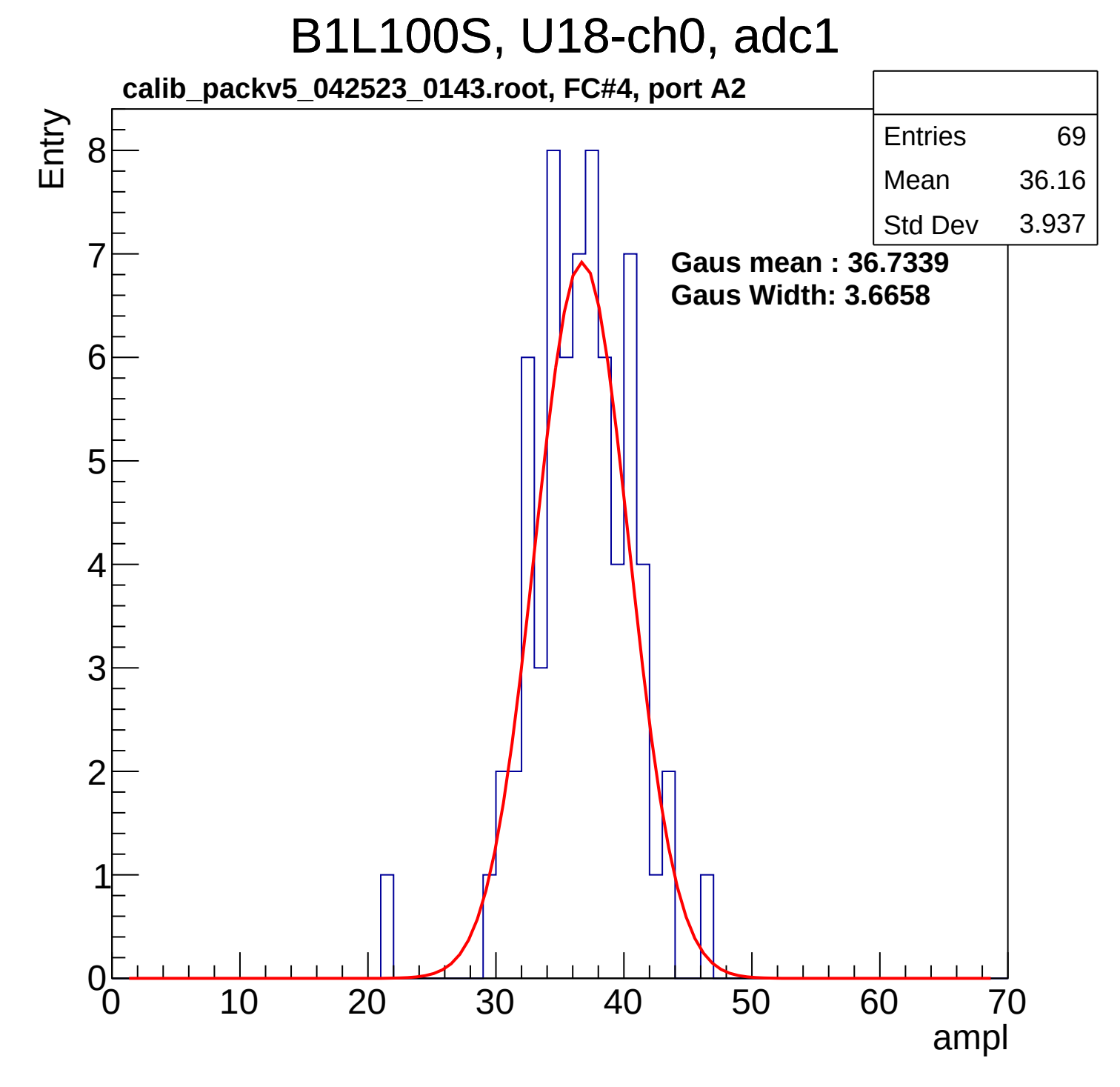
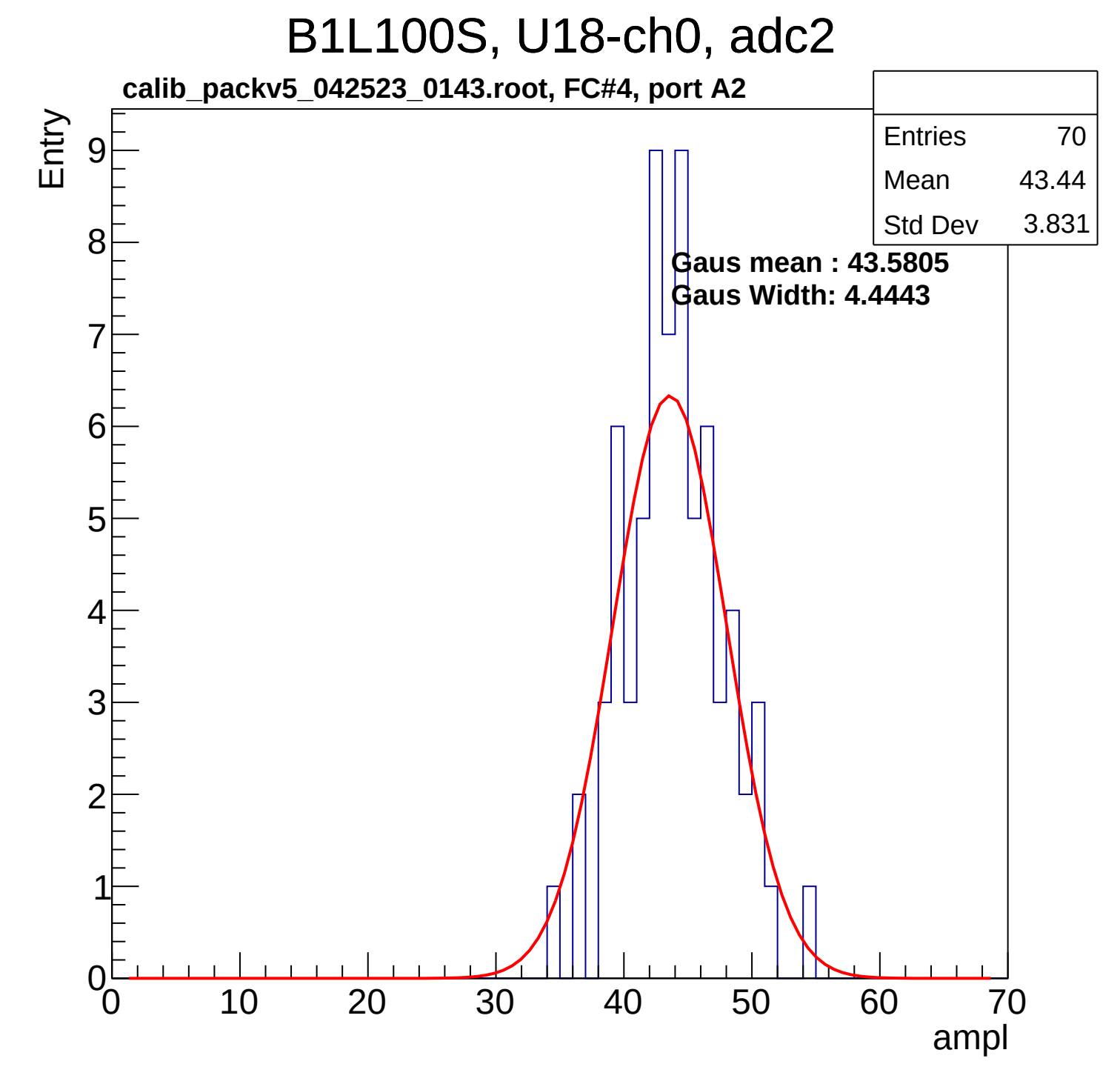
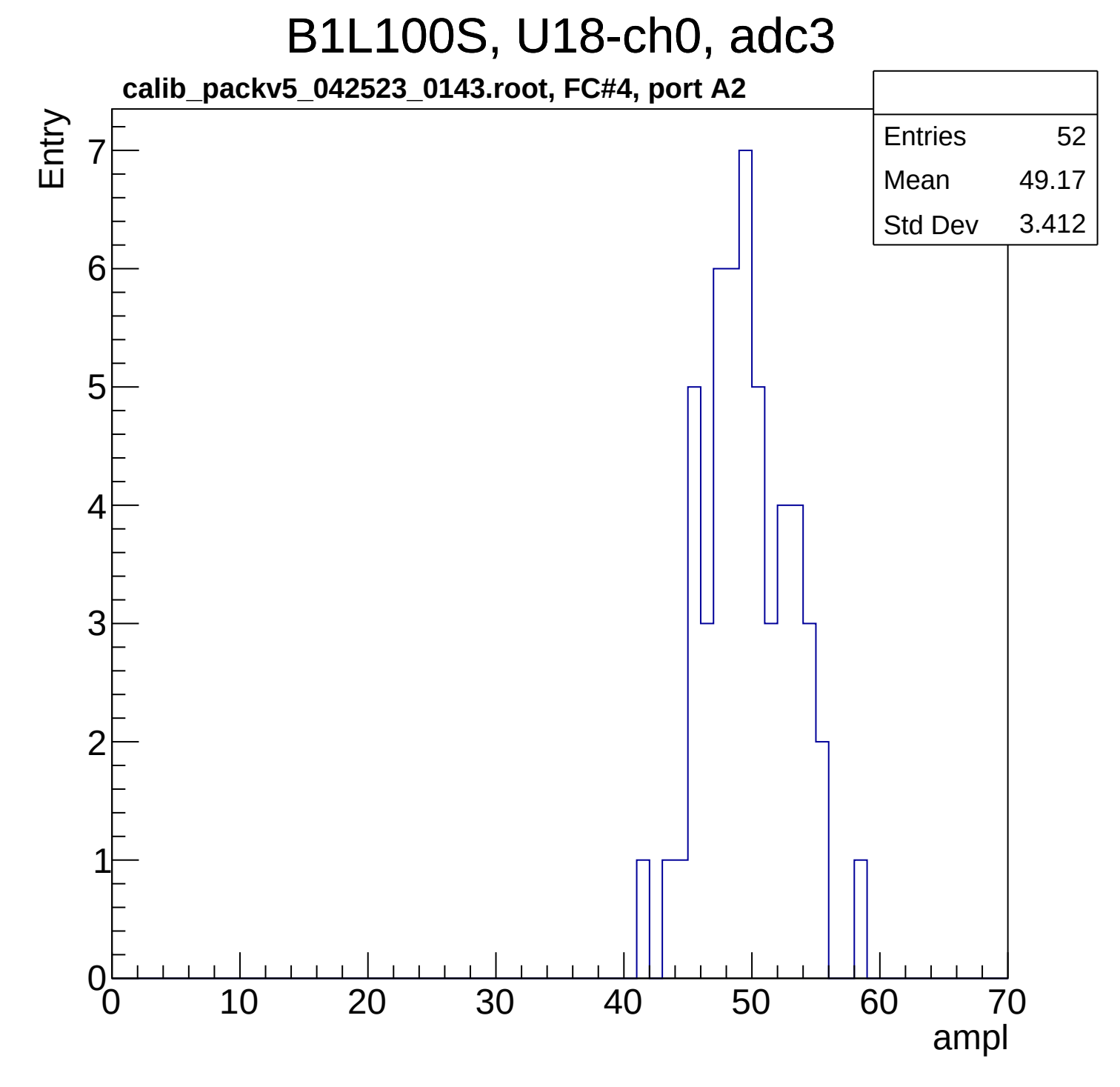
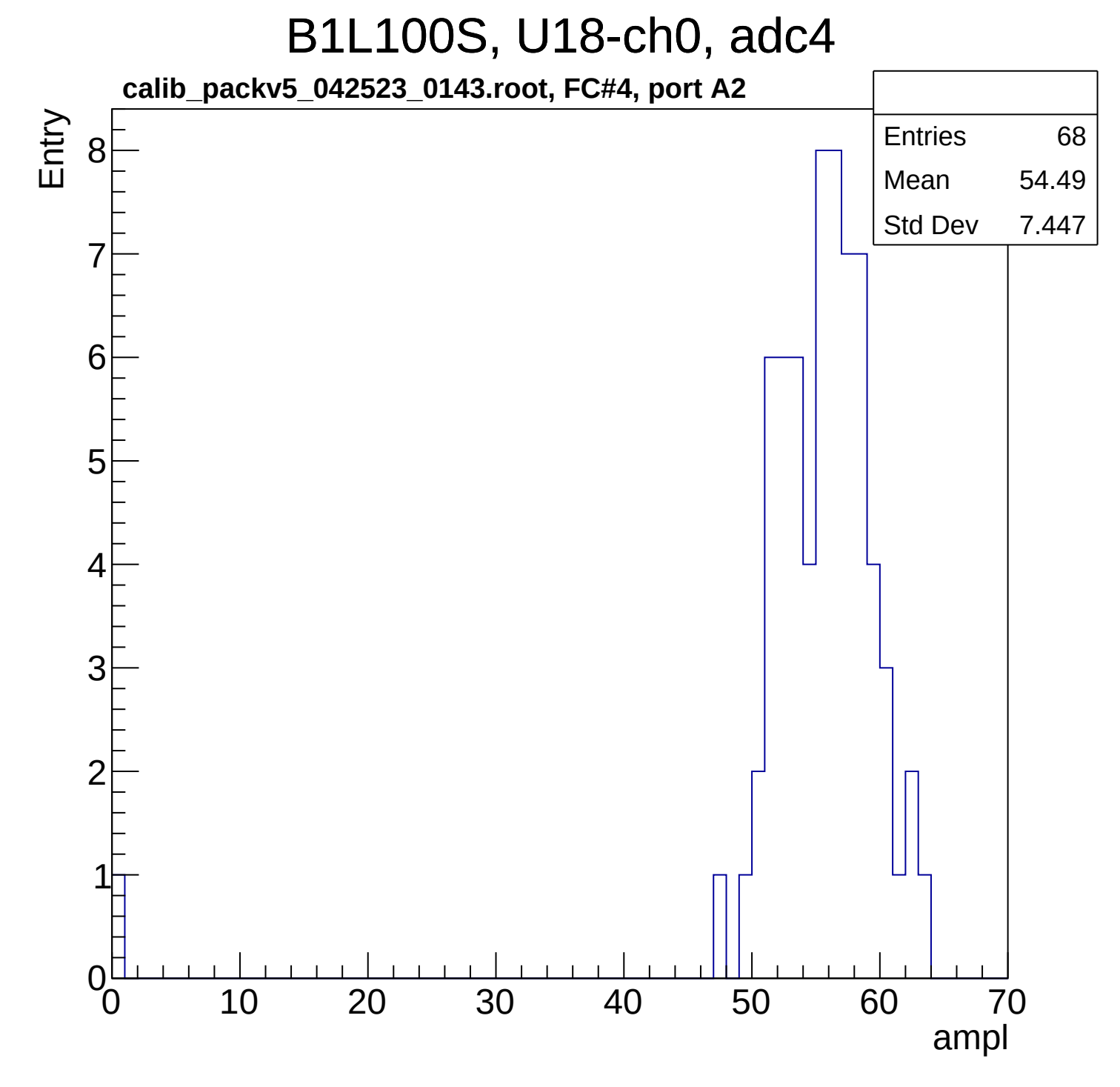
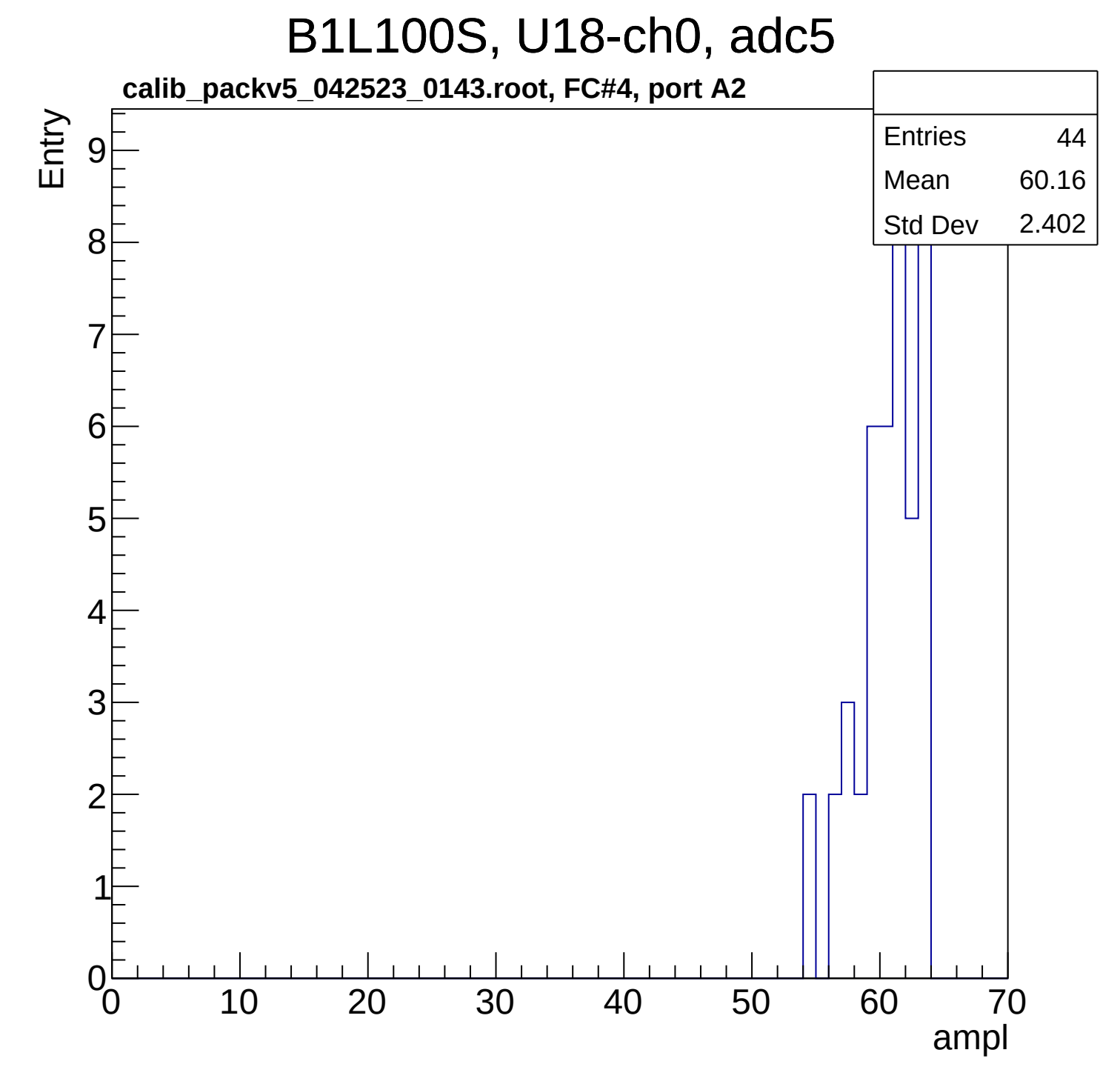

B1L100S, U18-ch0, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 29.46
Std Dev 3.638
Gaus mean : 29.1782
Gaus Width: 3.7826
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

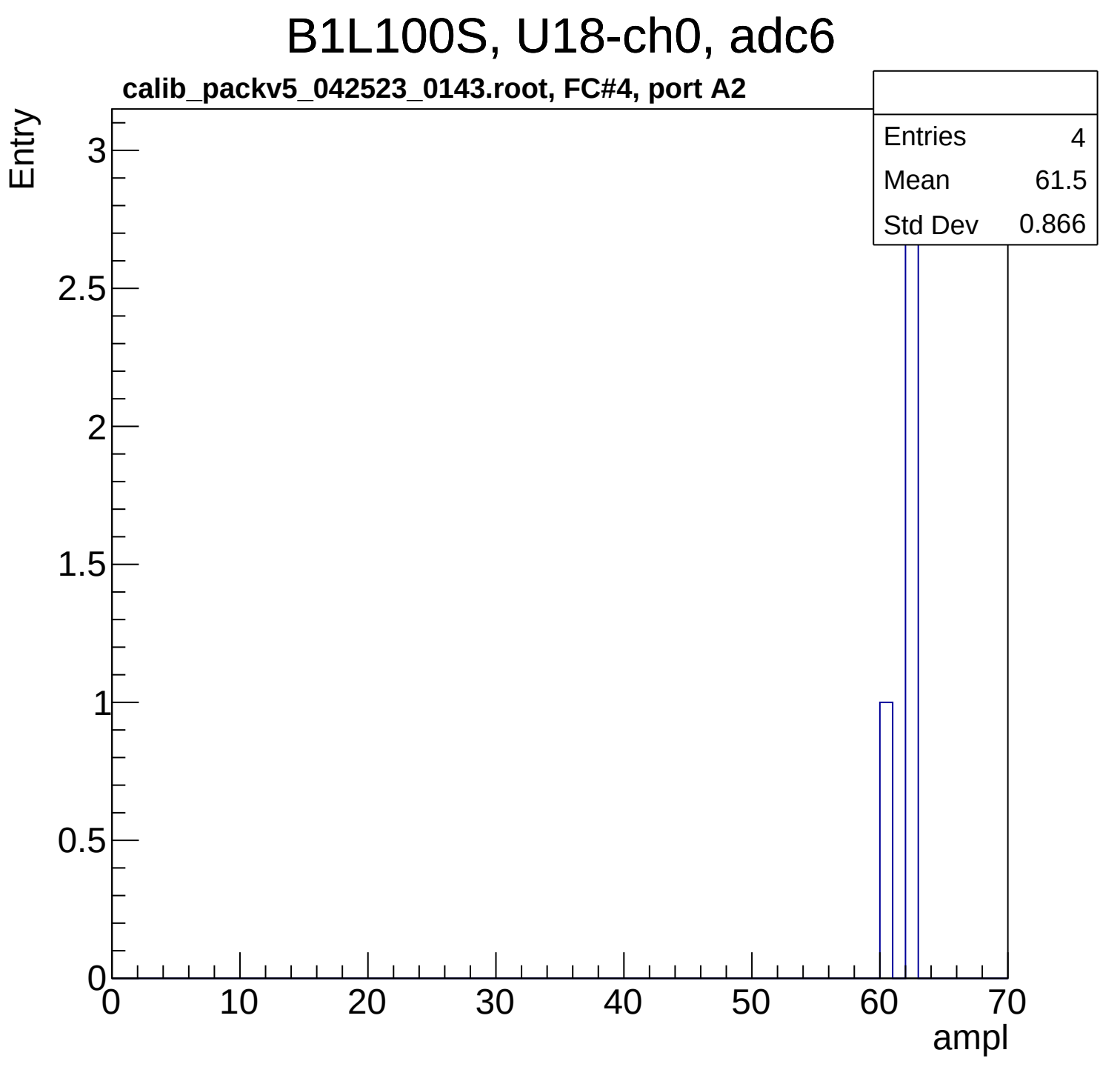

B1L100S, U18-ch0, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 36.16
Std Dev 3.937
Gaus mean : 36.7339
Gaus Width: 3.6658
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

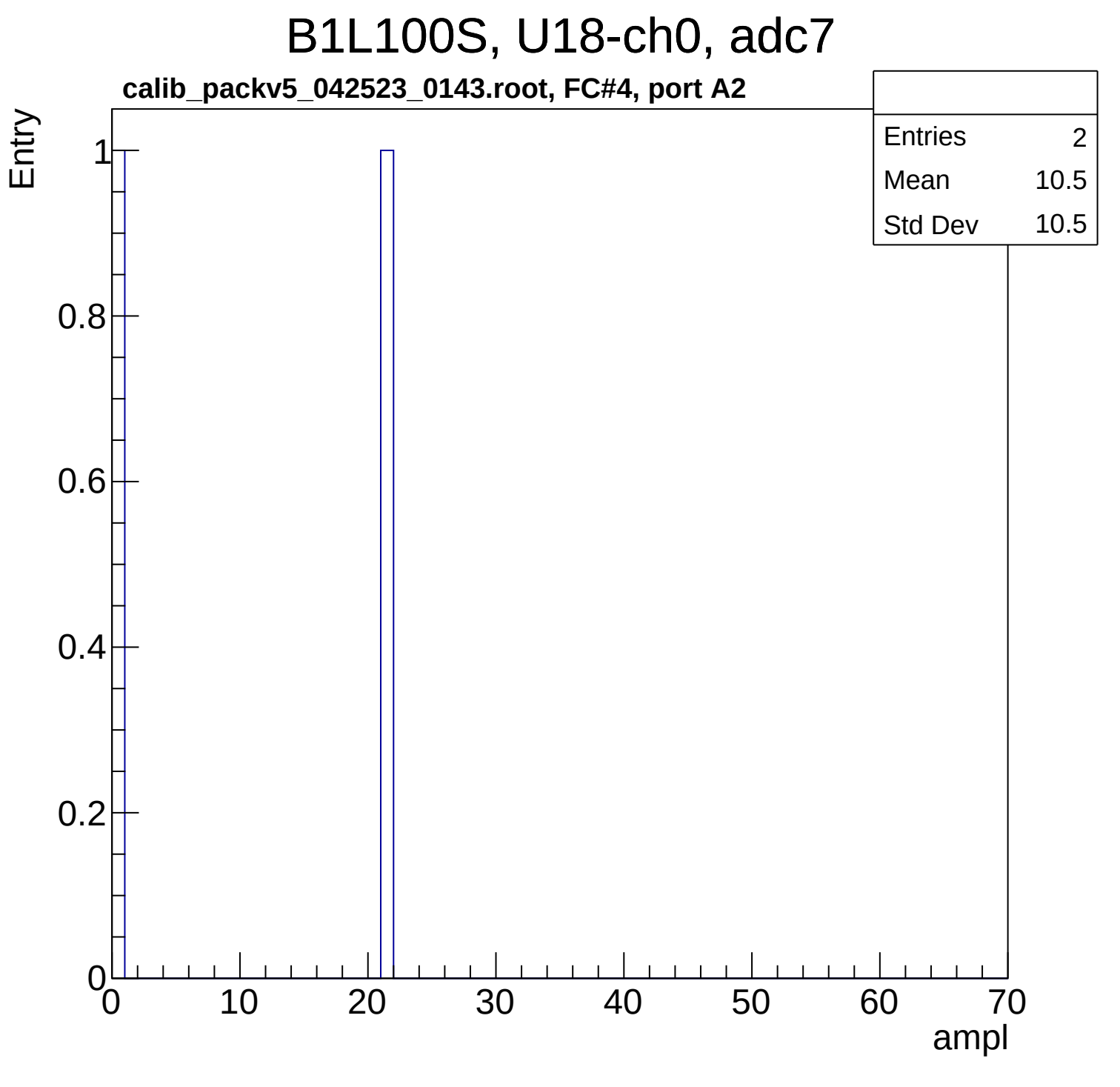

B1L100S, U18-ch0, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 43.44
Std Dev 3.831
Gaus mean : 43.5805
Gaus Width: 4.4443
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

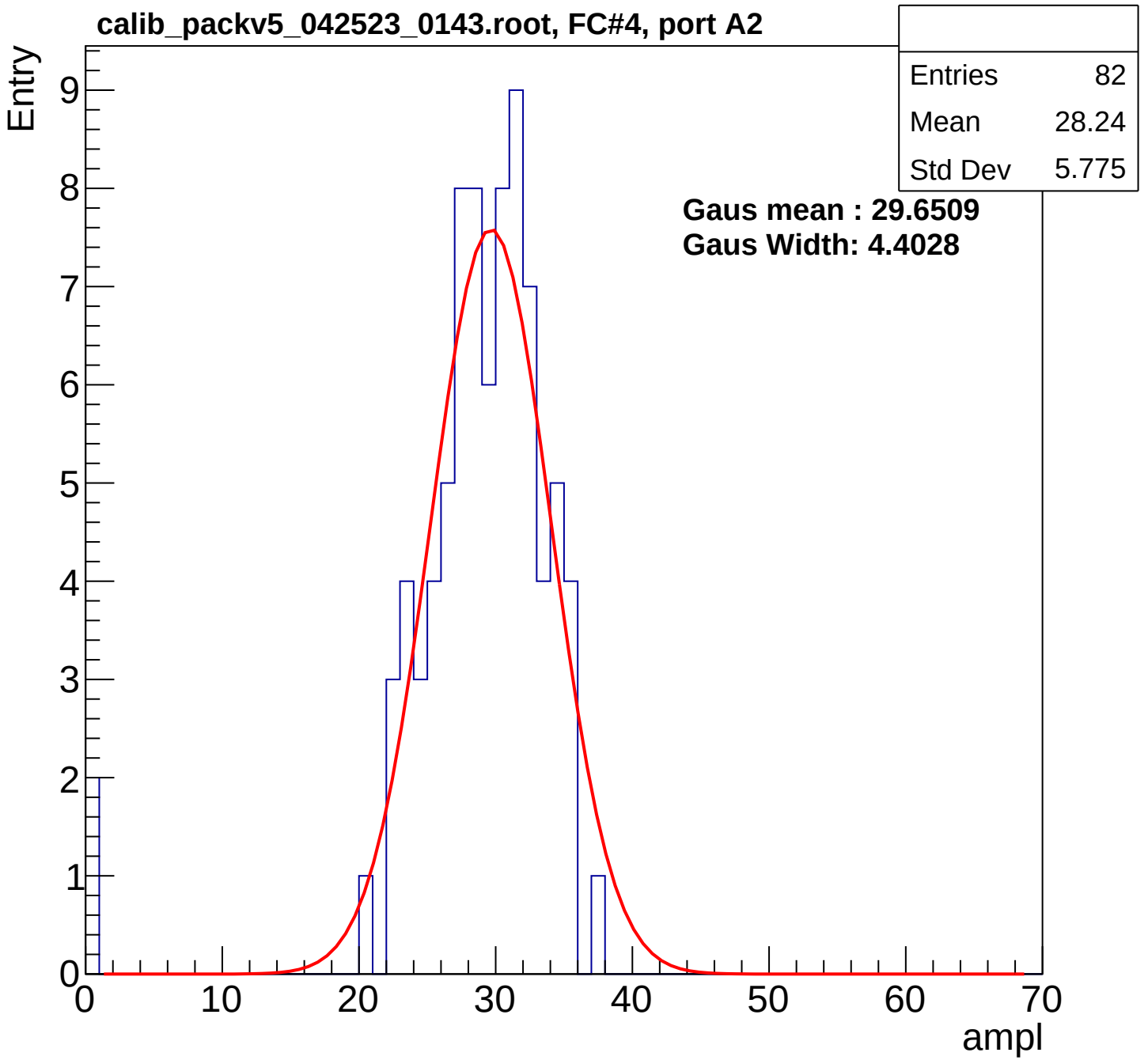

B1L100S, U18-ch0, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 49.17
Std Dev 3.412
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

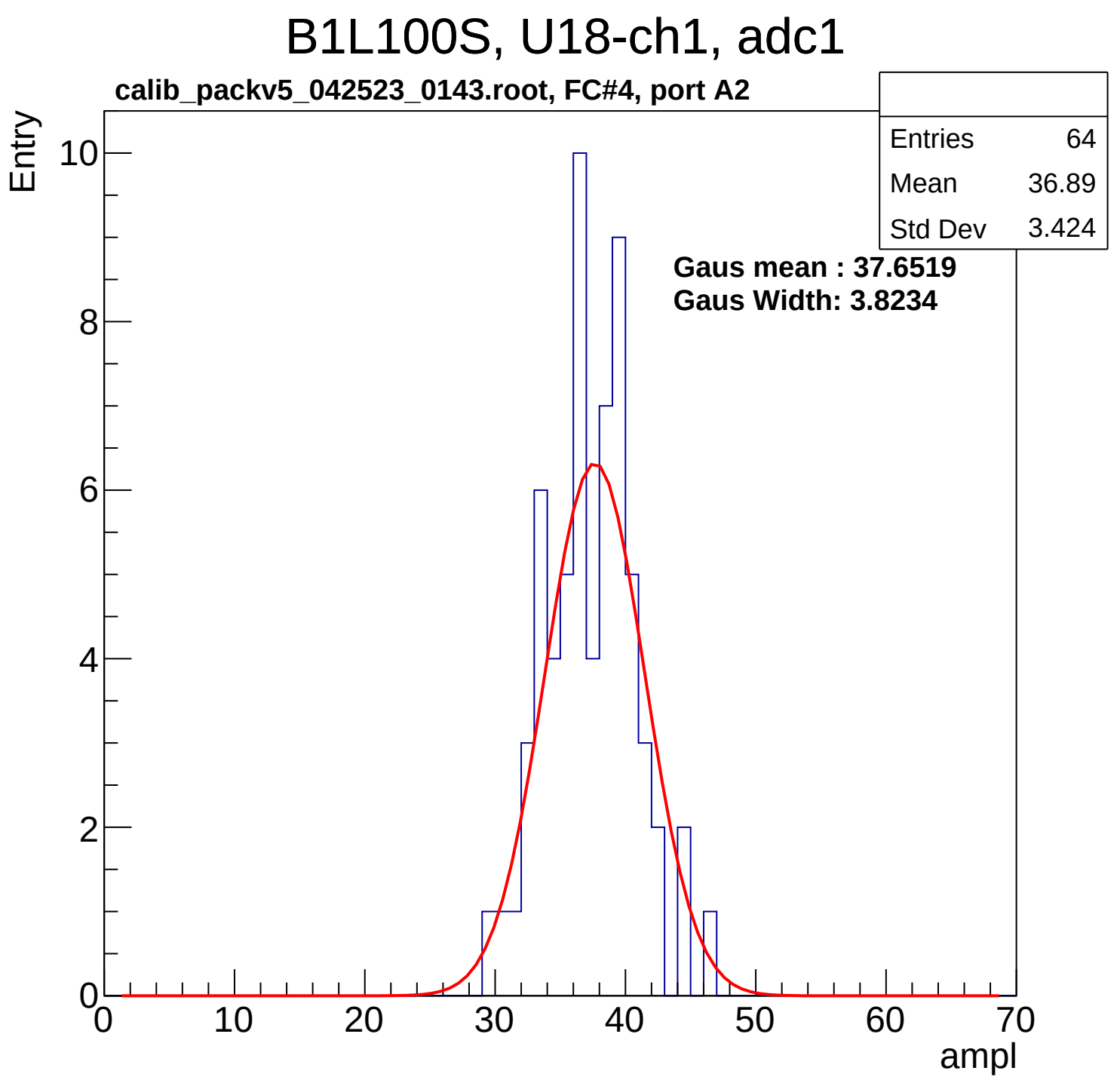

B1L100S, U18-ch0, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 54.49
Std Dev 7.447
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

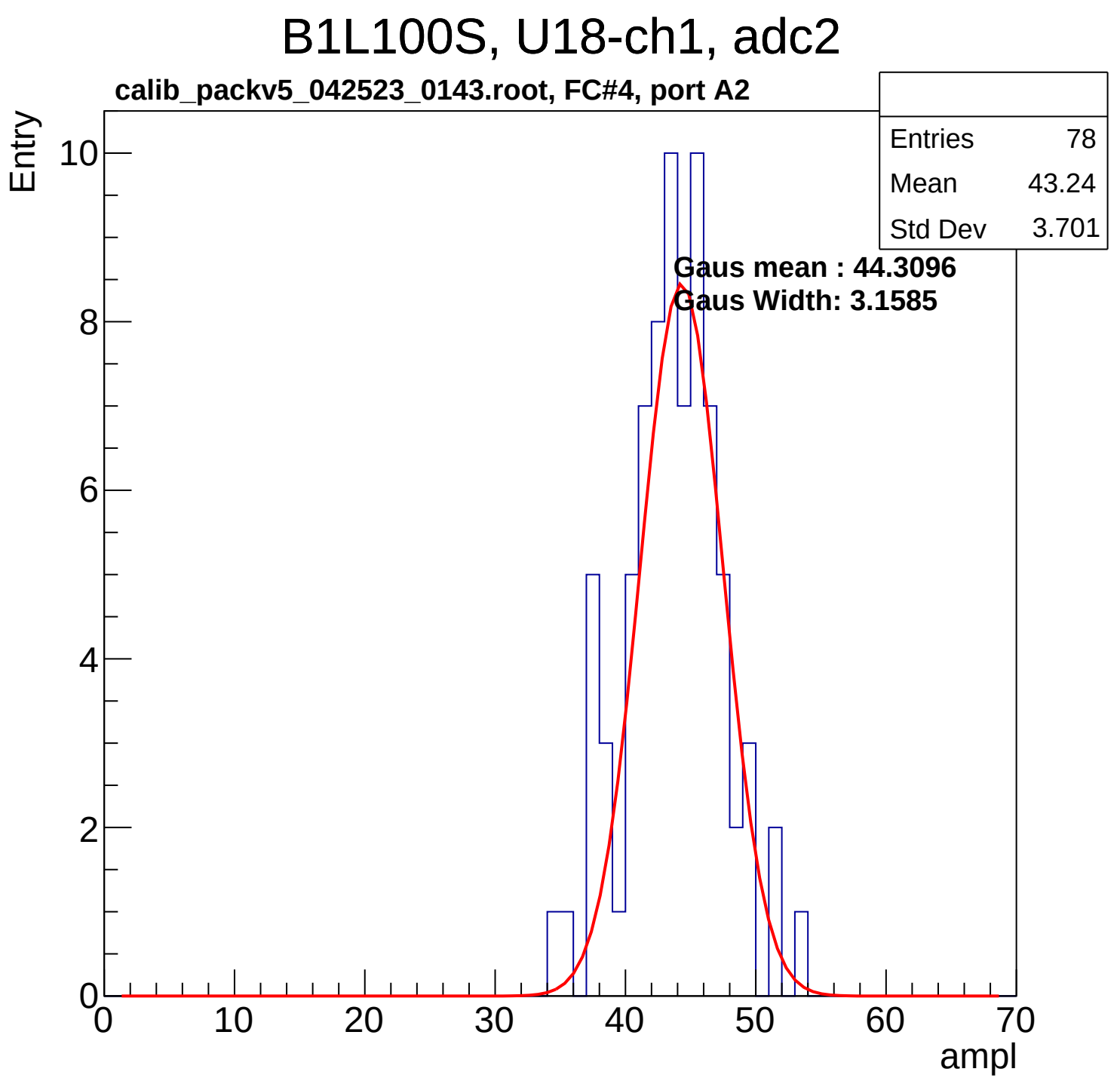

B1L100S, U18-ch0, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 44
Mean 60.16
Std Dev 2.402
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

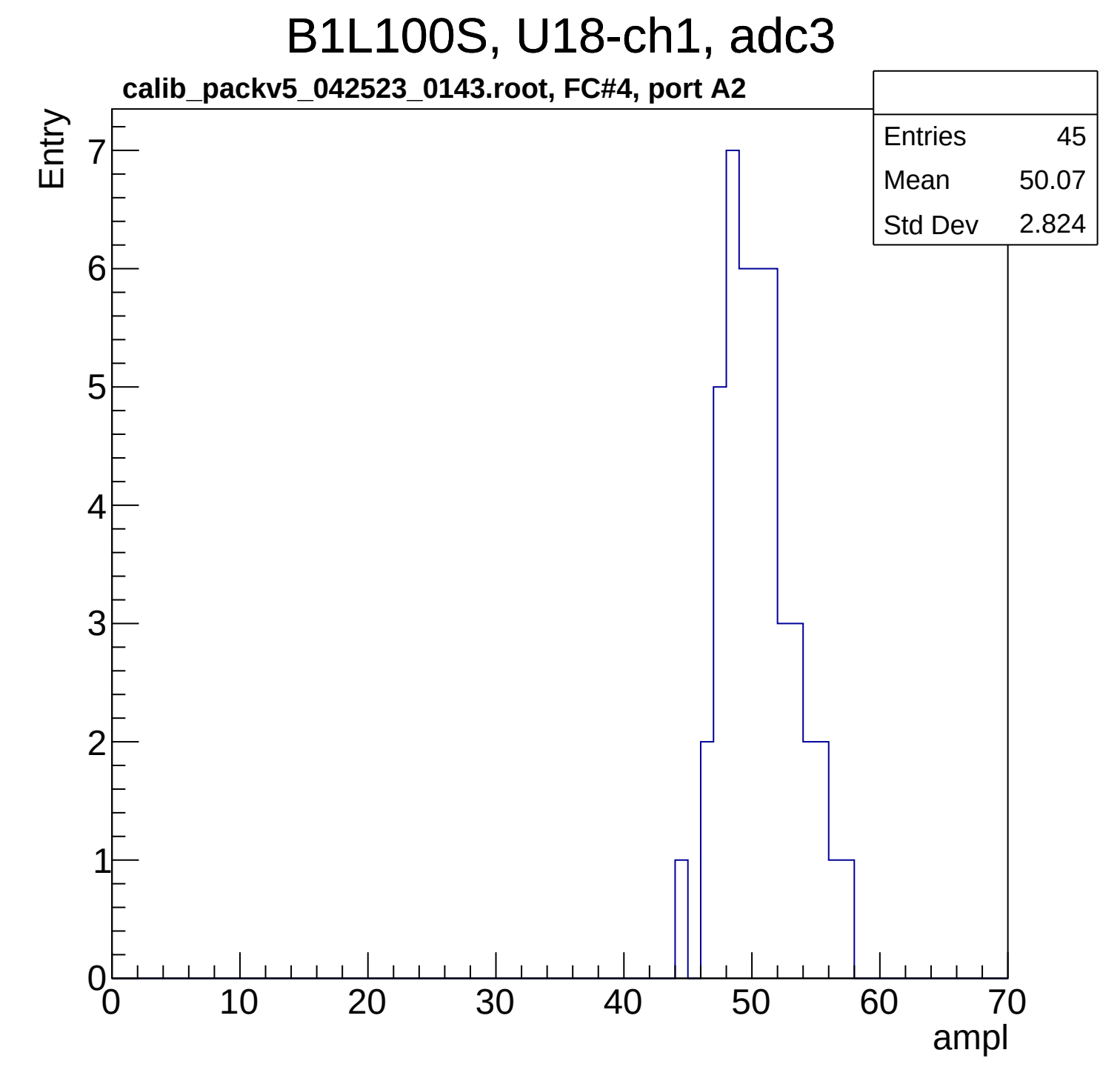

B1L100S, U18-ch0, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 61.5
Std Dev 0.866
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

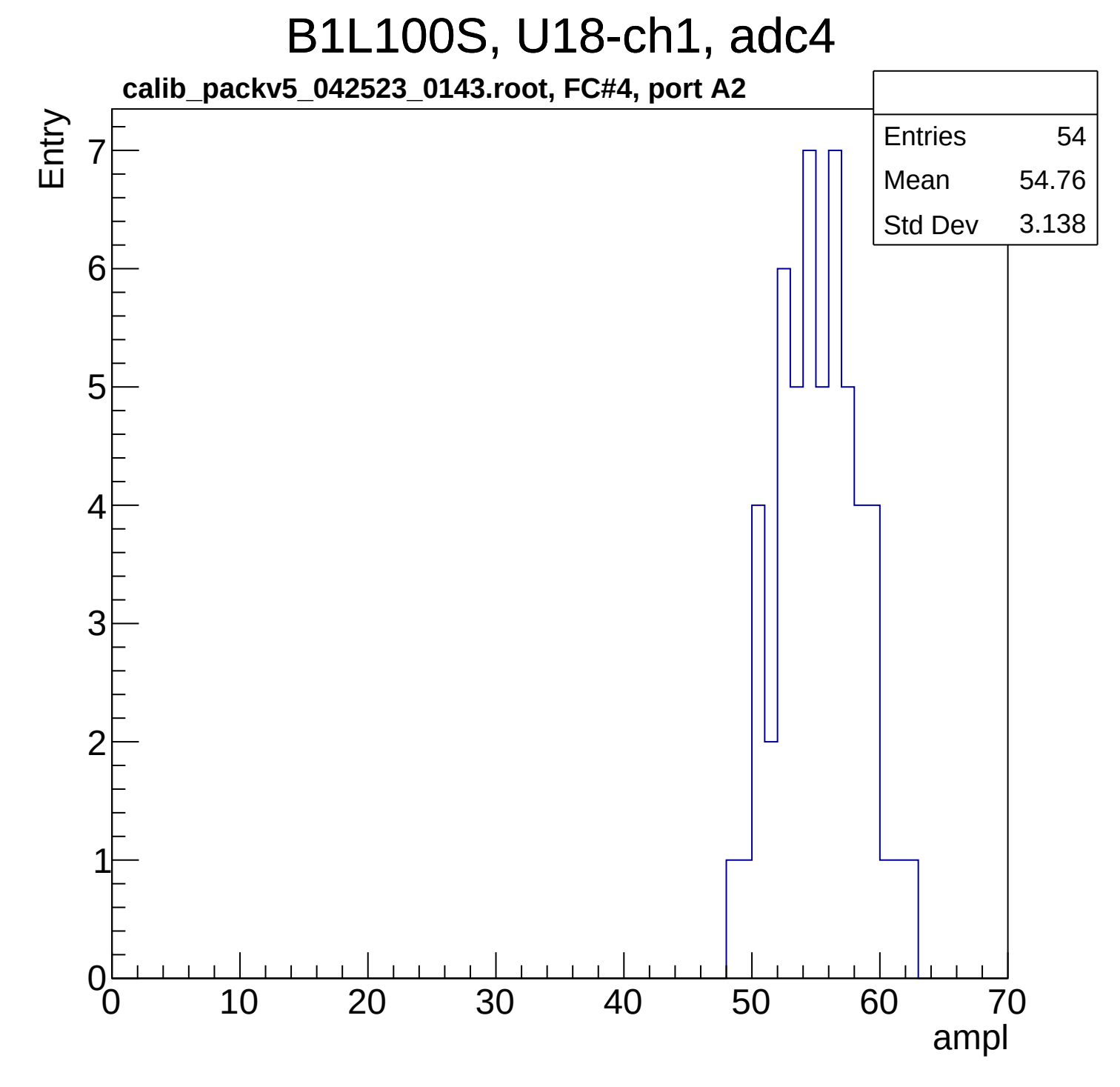

B1L100S, U18-ch0, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 10.5
Std Dev 10.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

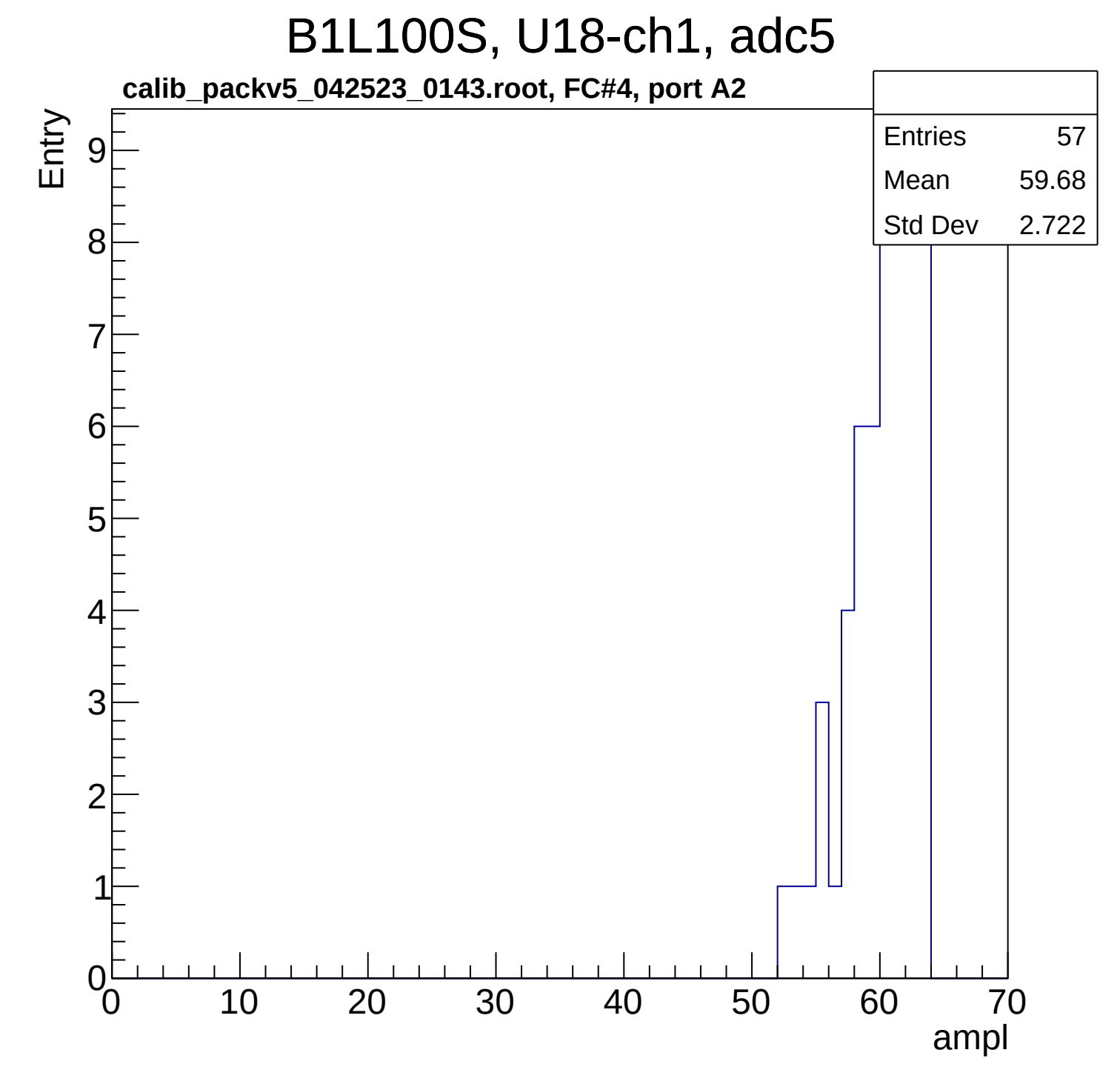

B1L100S, U18-ch1, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 28.24
Std Dev 5.775
Gaus mean : 29.6509
Gaus Width: 4.4028
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

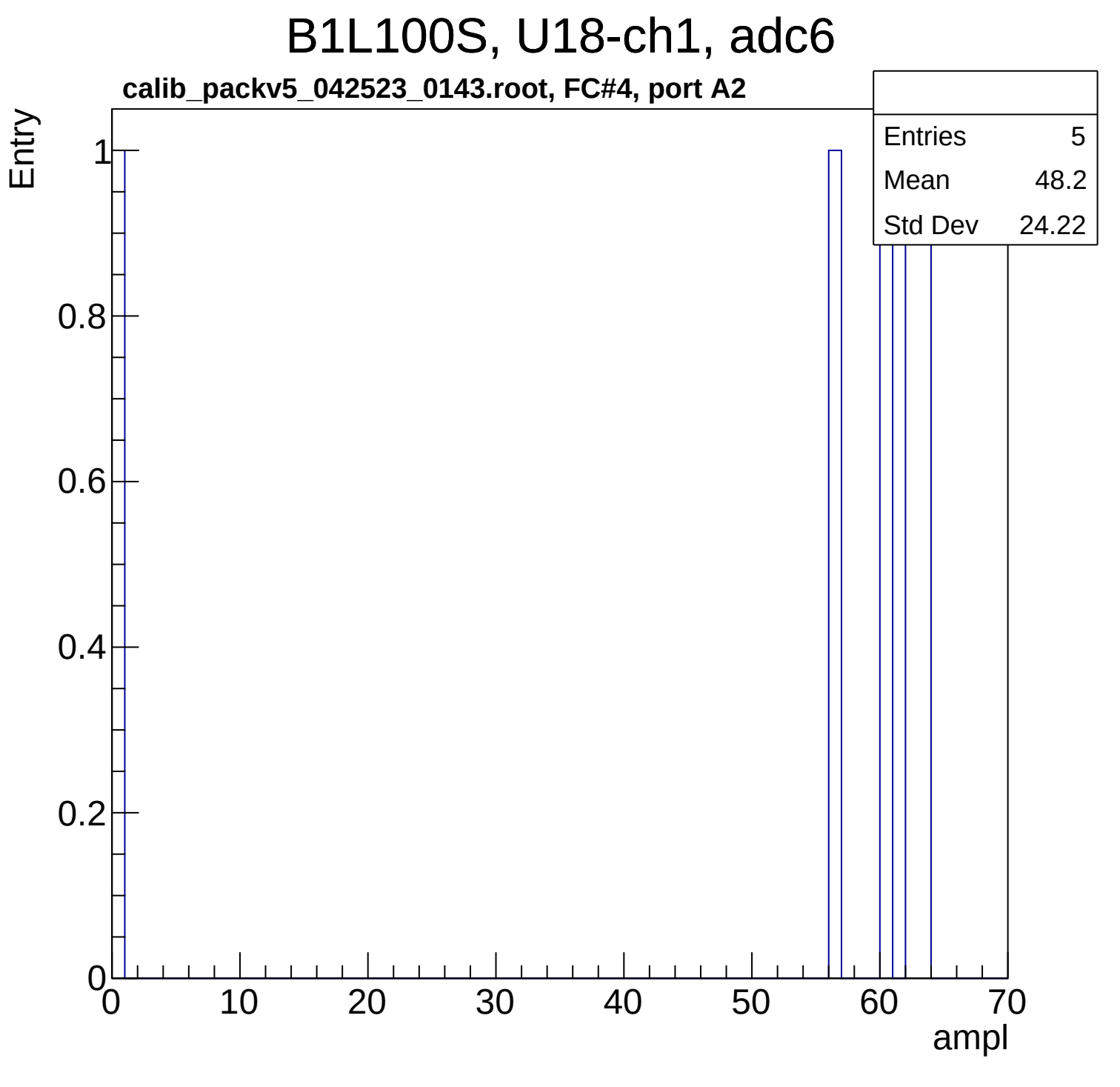

B1L100S, U18-ch1, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 36.89
Std Dev 3.424
Gaus mean : 37.6519
Gaus Width: 3.8234
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

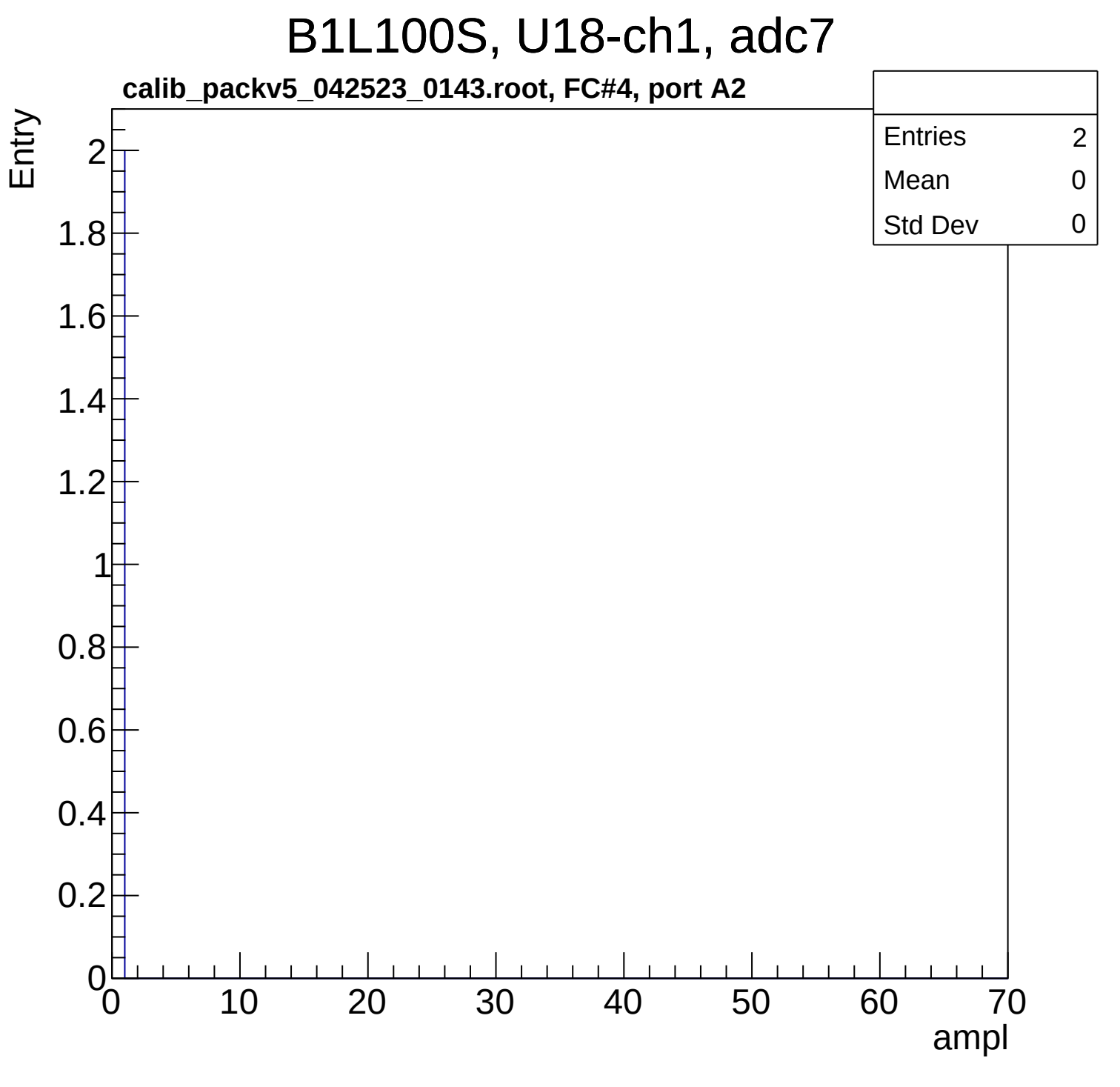

B1L100S, U18-ch1, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 43.24
Std Dev 3.701
Gaus mean : 44.3096
Gaus Width: 3.1585
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

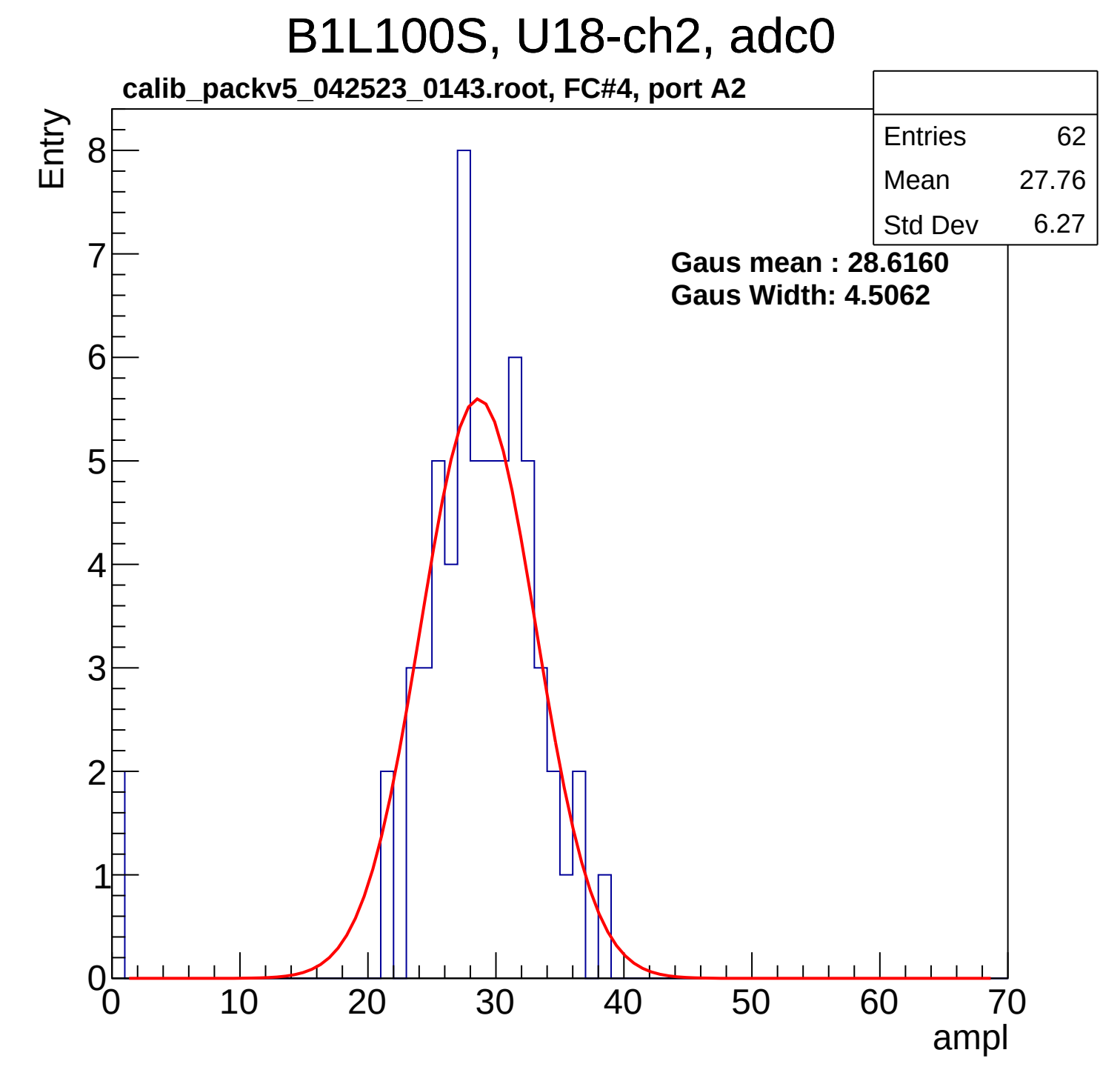

B1L100S, U18-ch1, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 45
Mean 50.07
Std Dev 2.824
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

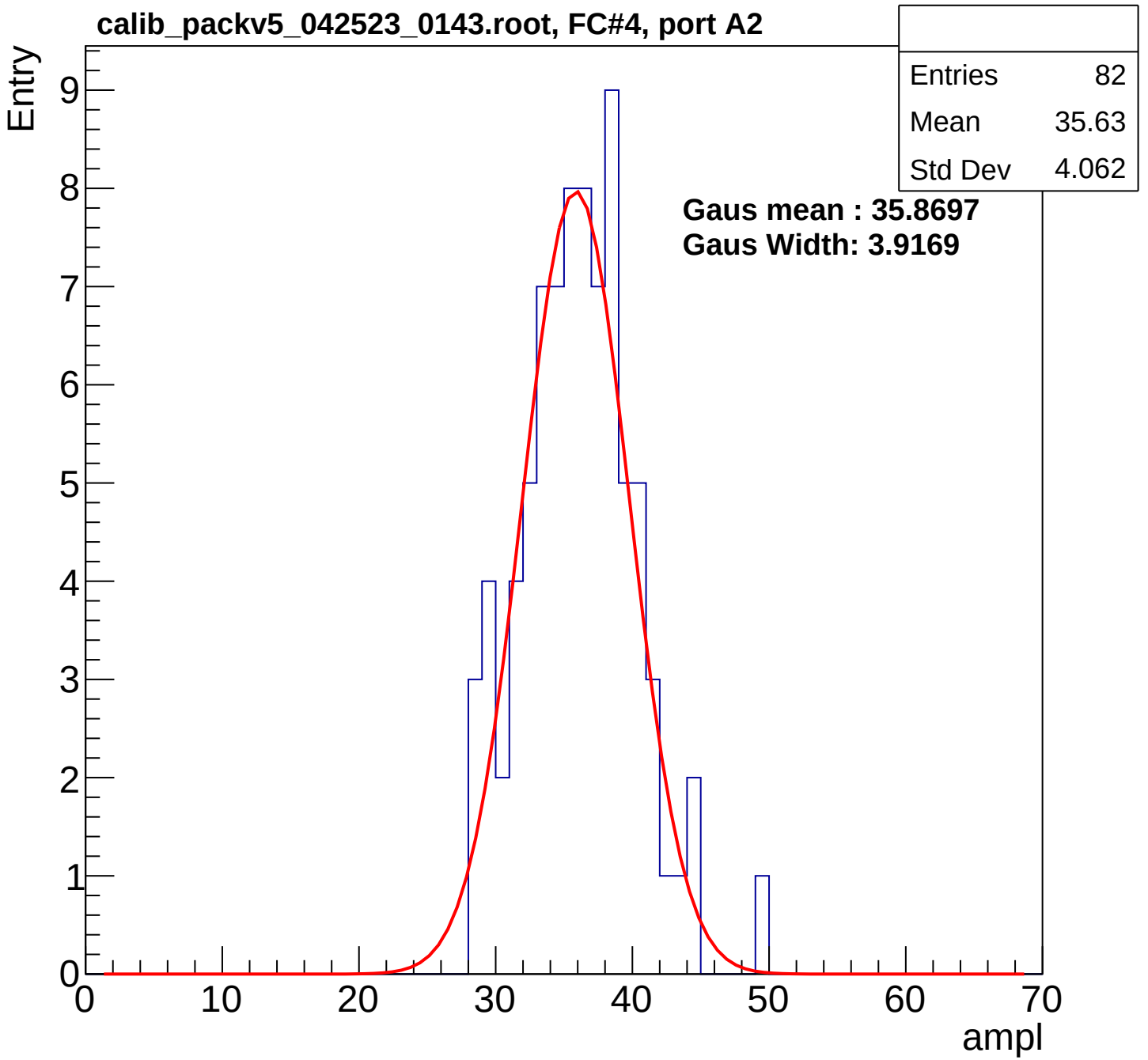

B1L100S, U18-ch1, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 54.76
Std Dev 3.138
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

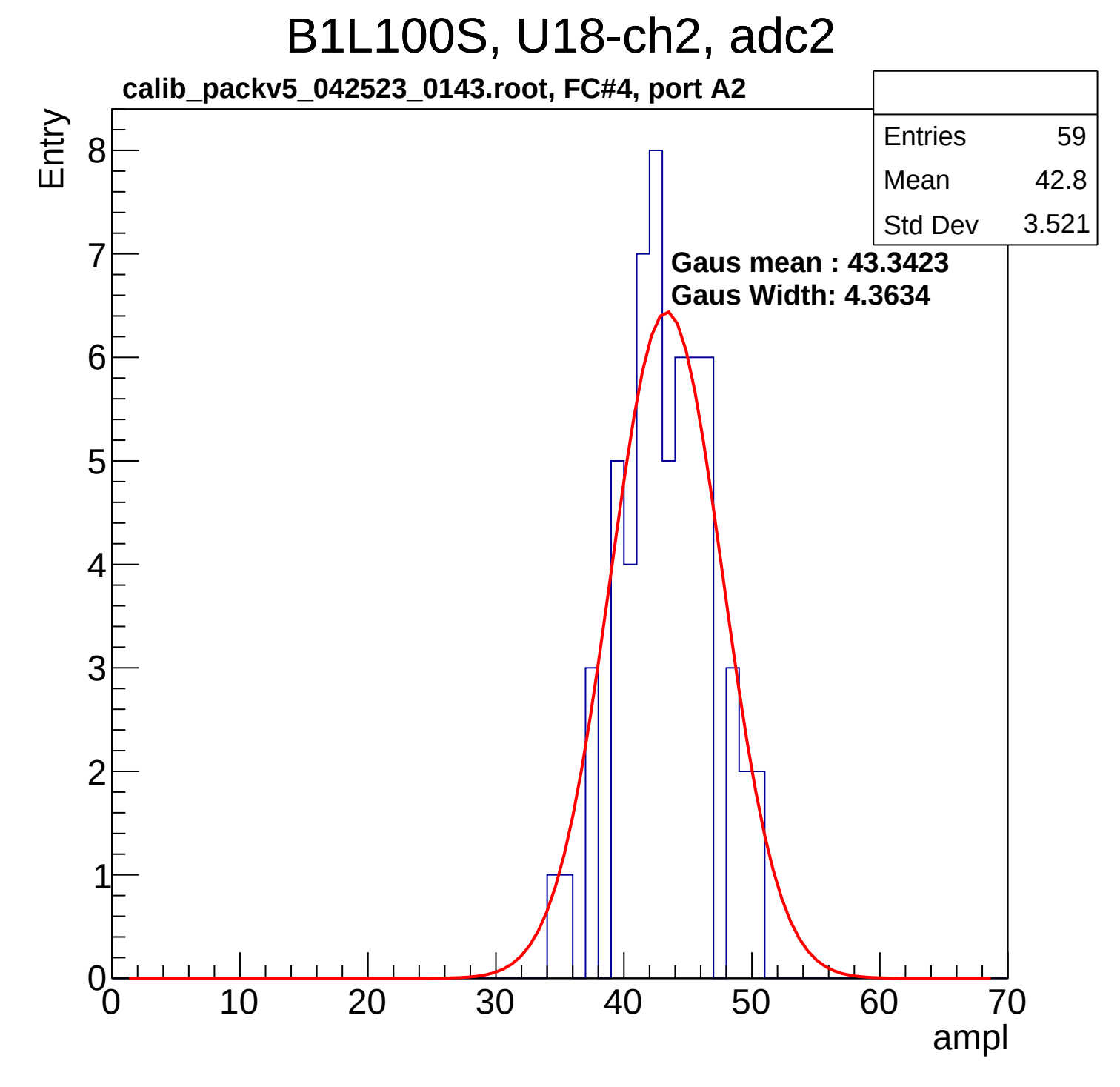

B1L100S, U18-ch1, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 59.68
Std Dev 2.722
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

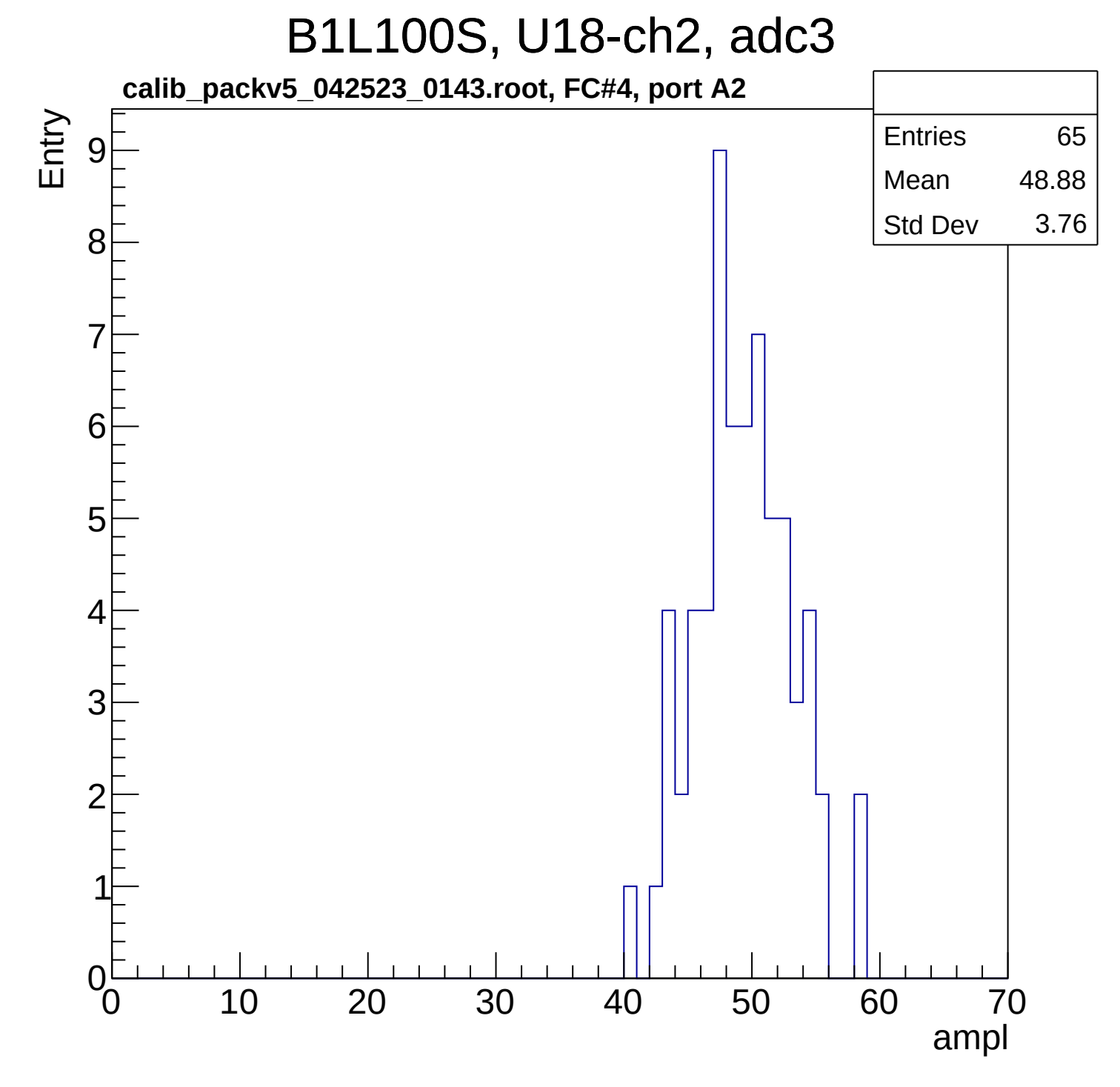

B1L100S, U18-ch1, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 5
Mean 48.2
Std Dev 24.22
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

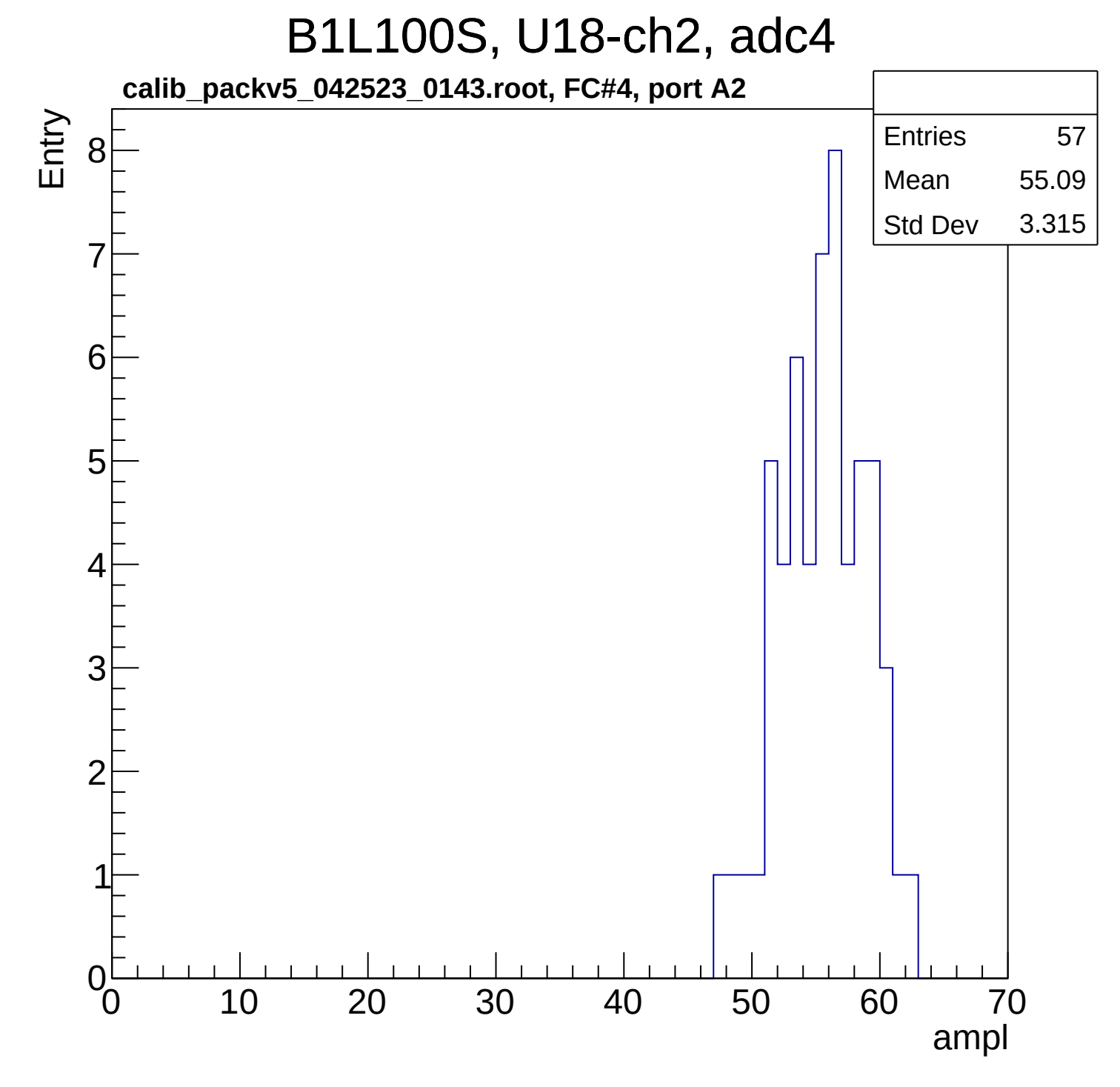

B1L100S, U18-ch1, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

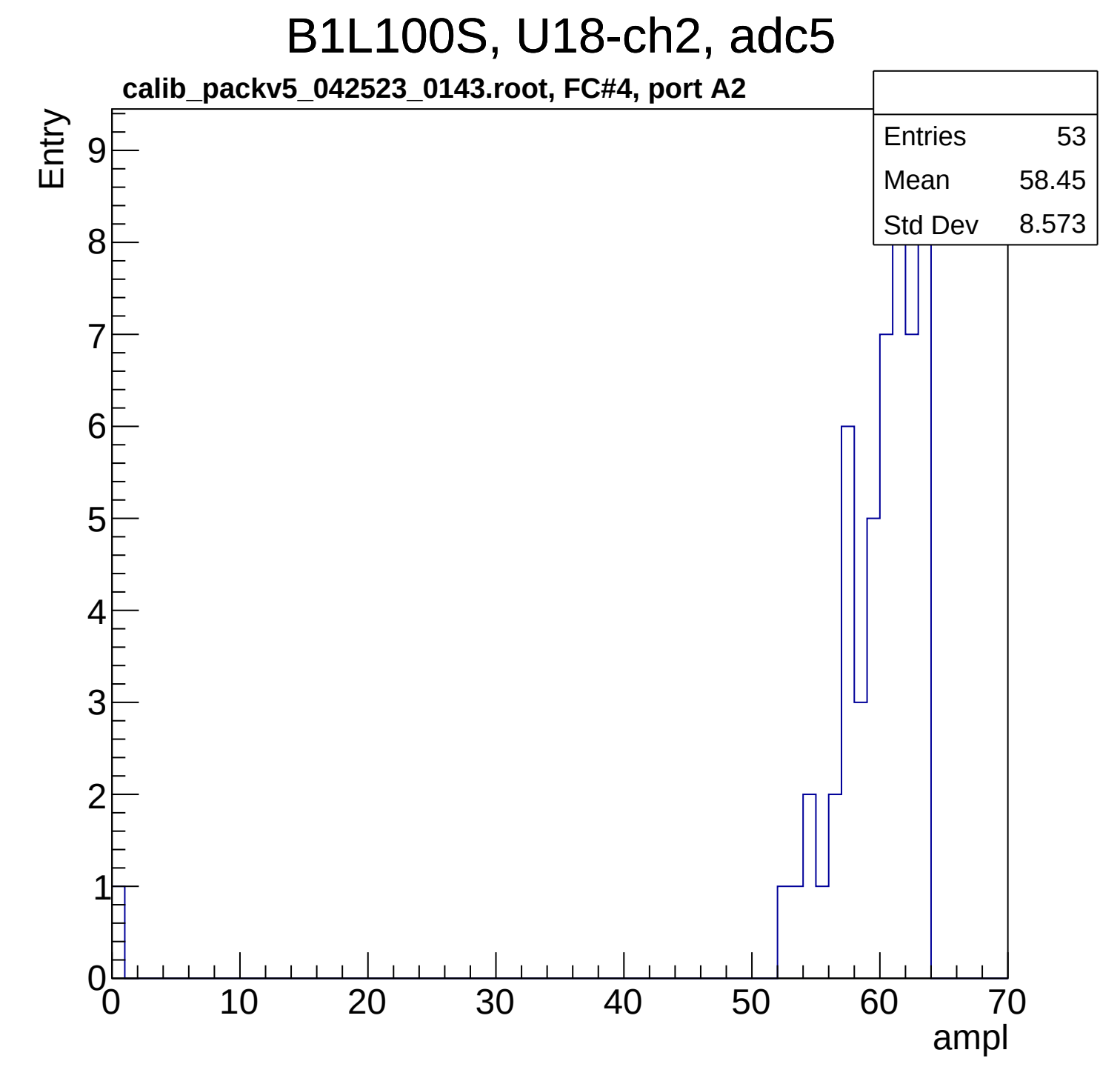

B1L100S, U18-ch2, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 27.76
Std Dev 6.27
Gaus mean : 28.6160
Gaus Width: 4.5062
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

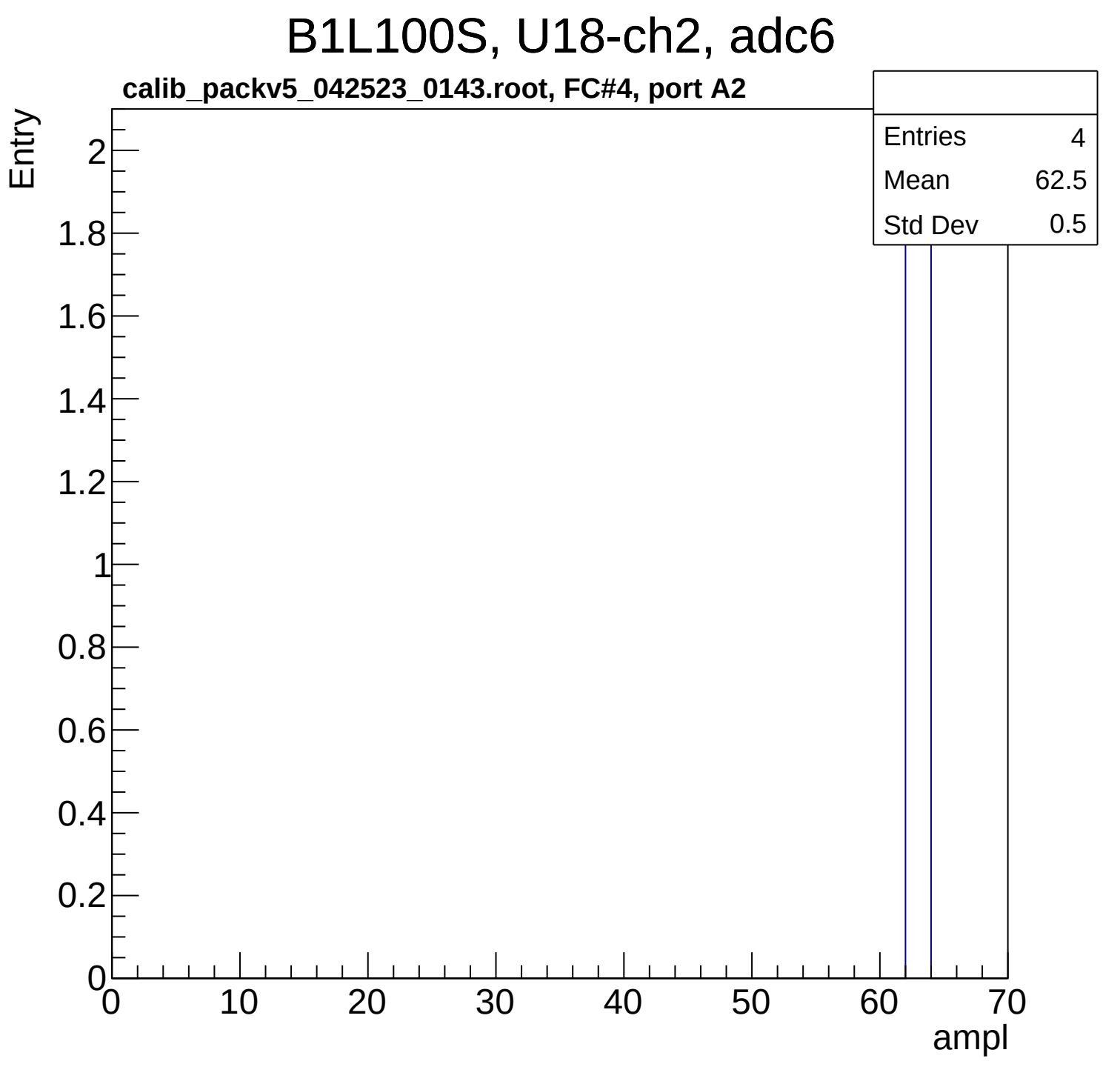

B1L100S, U18-ch2, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 35.63
Std Dev 4.062
Gaus mean : 35.8697
Gaus Width: 3.9169
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

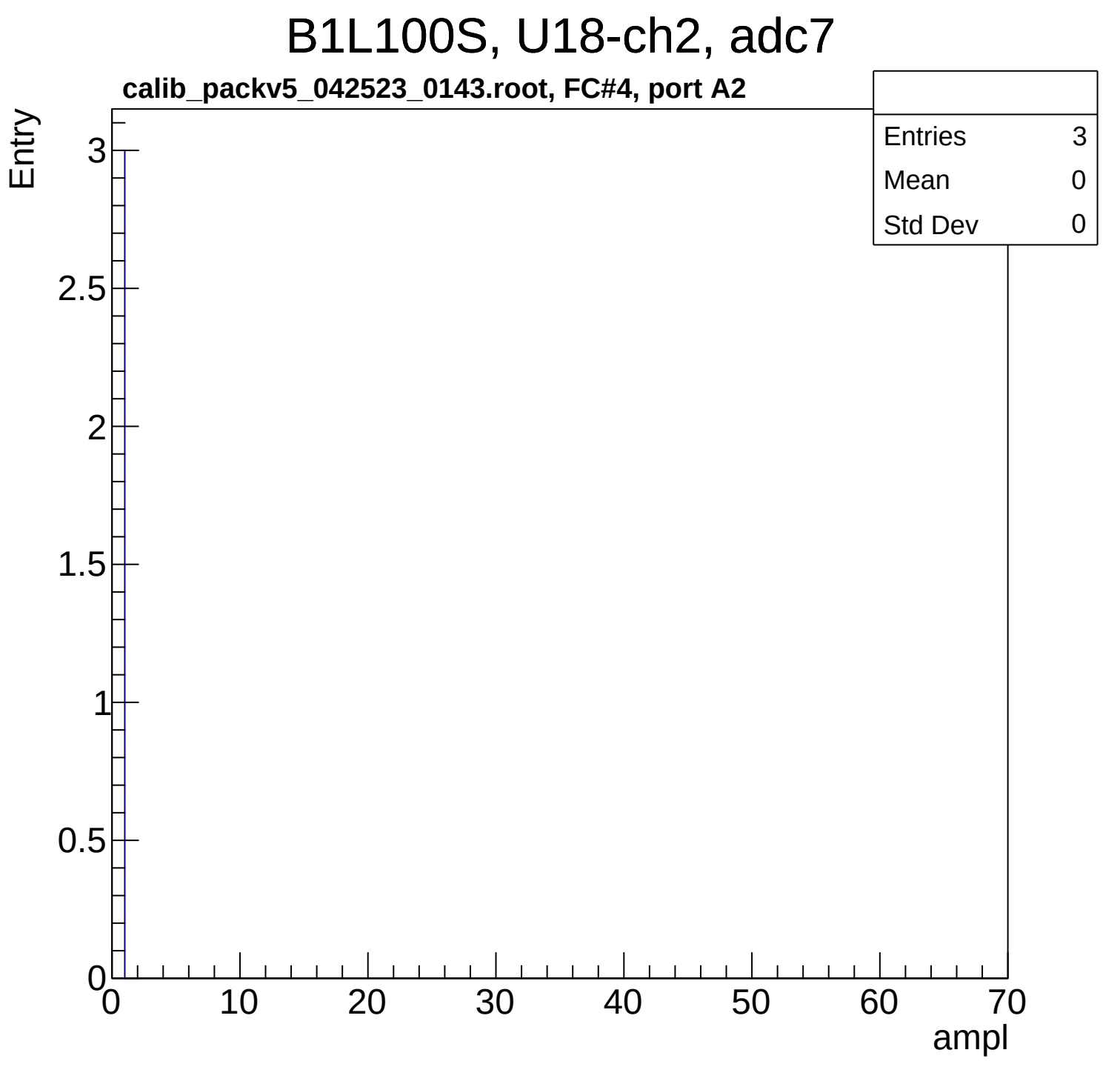

B1L100S, U18-ch2, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 42.8
Std Dev 3.521
Gaus mean : 43.3423
Gaus Width: 4.3634
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

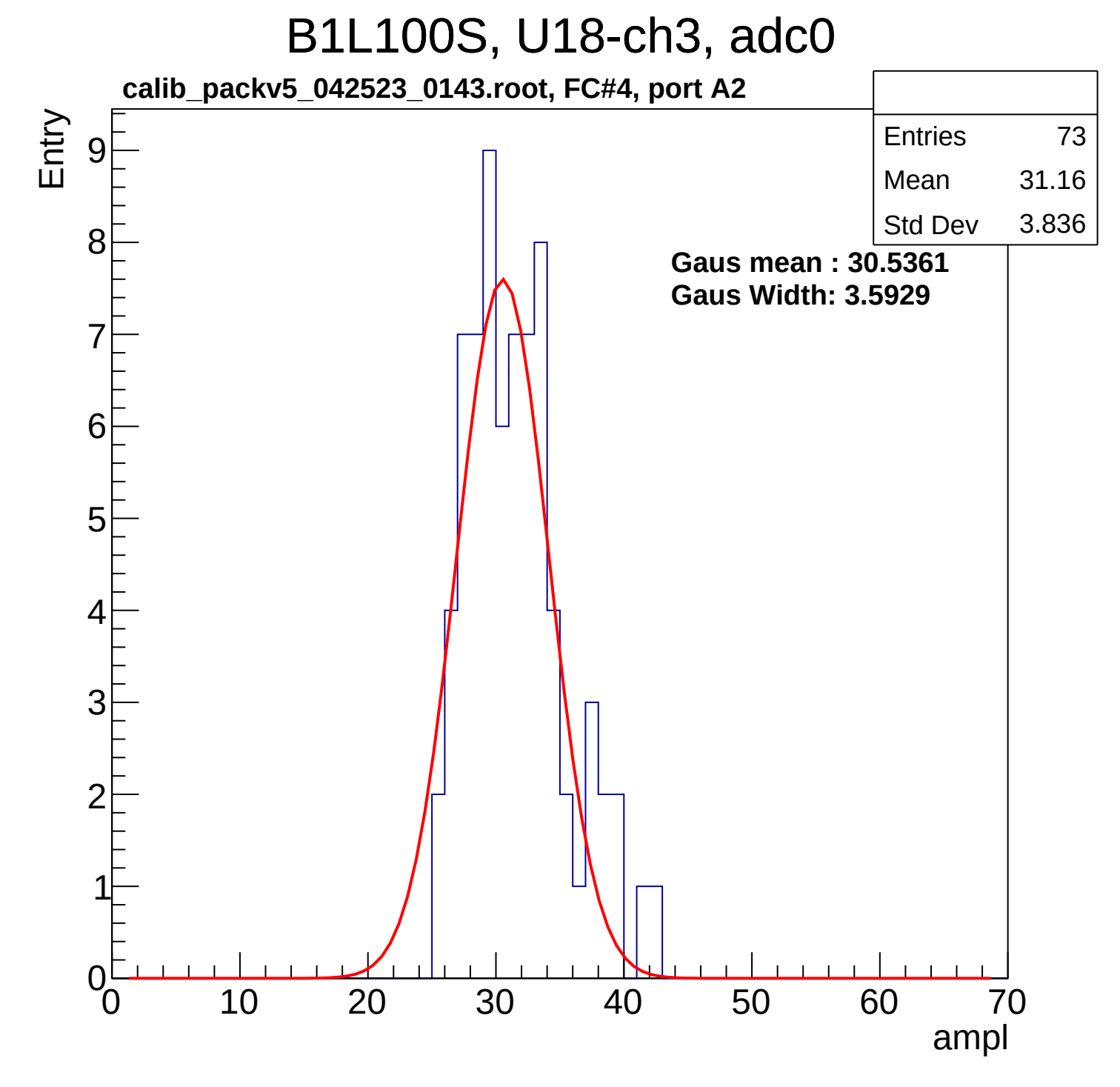

B1L100S, U18-ch2, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 48.88
Std Dev 3.76
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

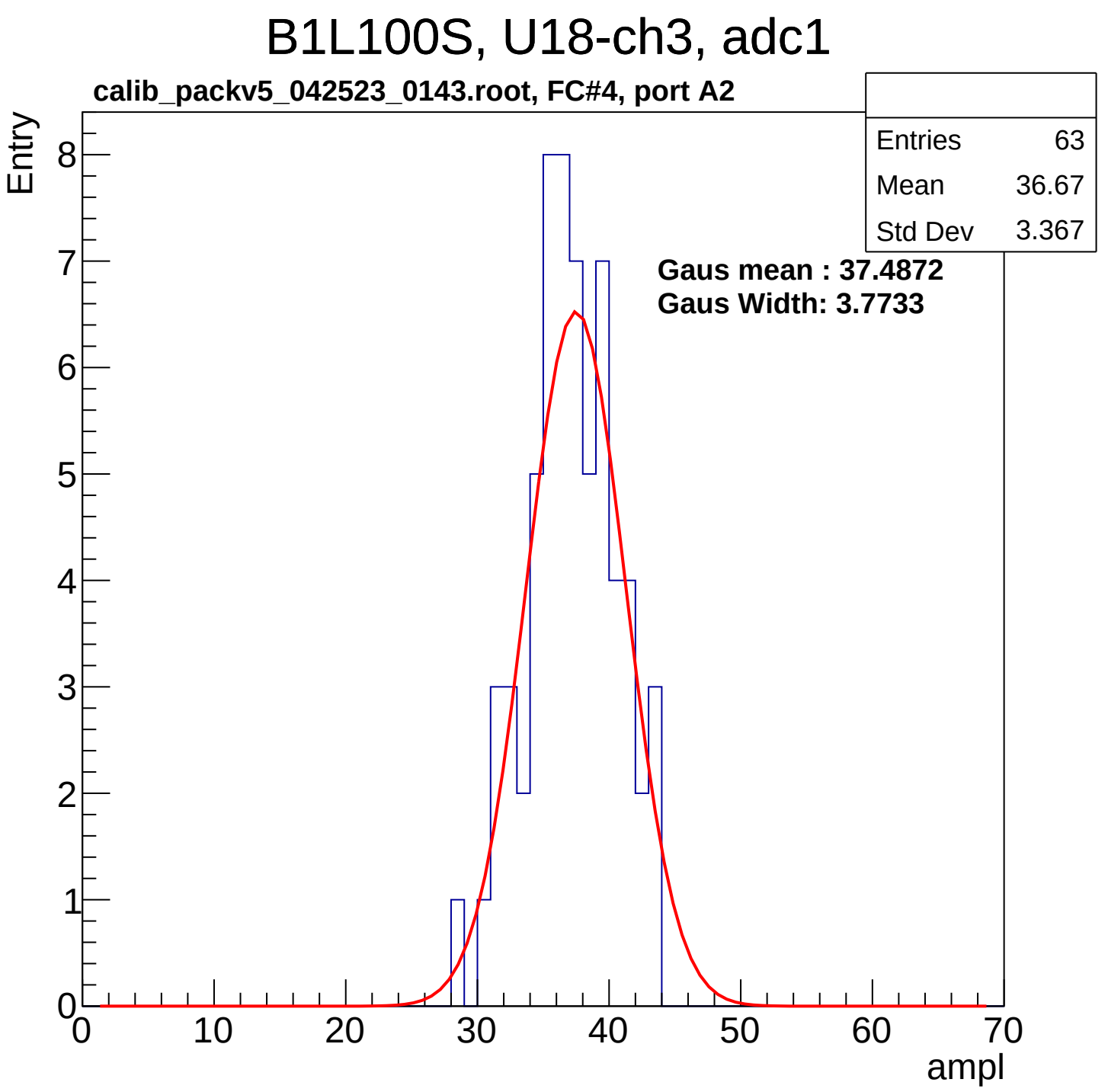

B1L100S, U18-ch2, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 55.09
Std Dev 3.315
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

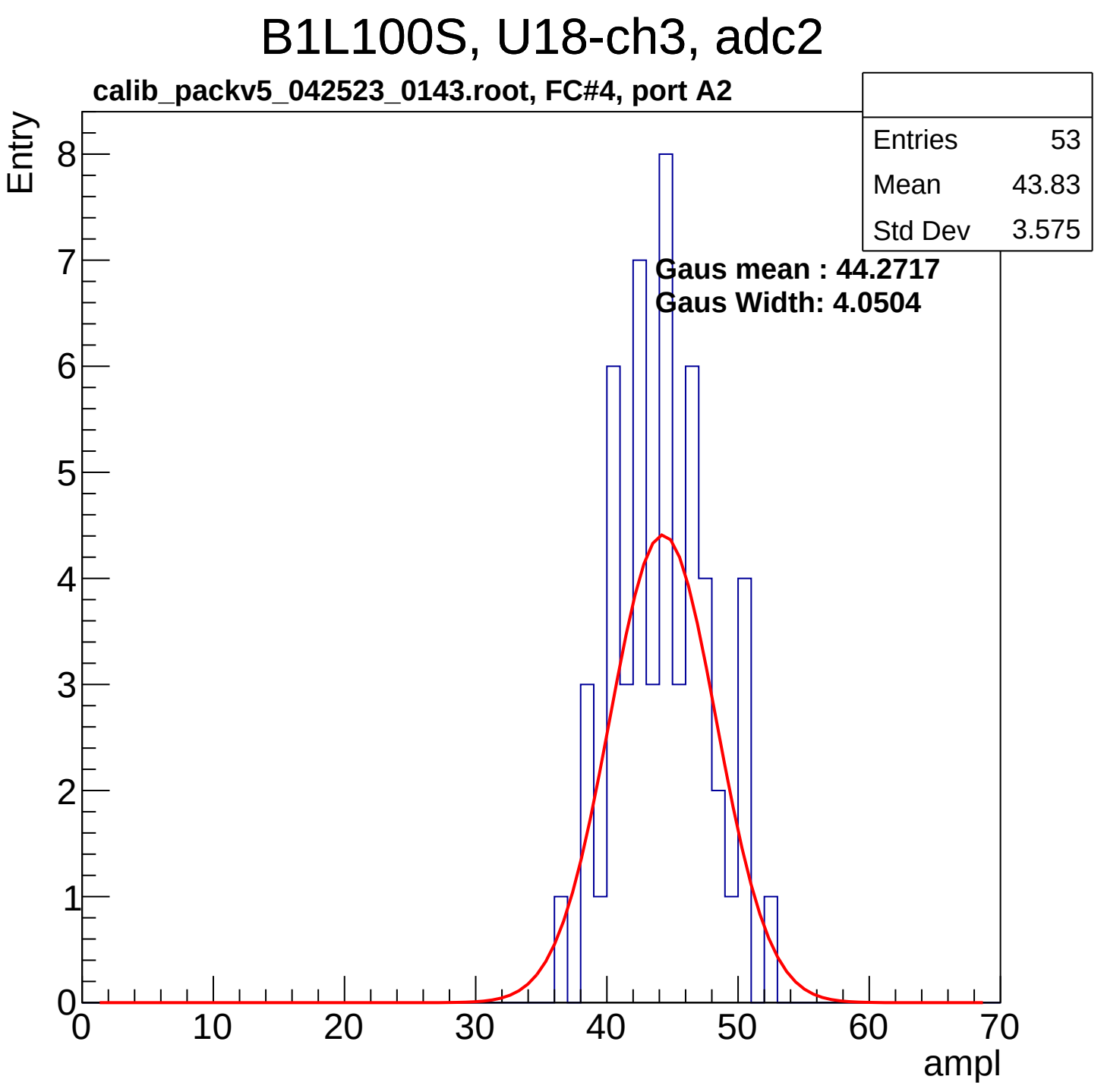

B1L100S, U18-ch2, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 58.45
Std Dev 8.573
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

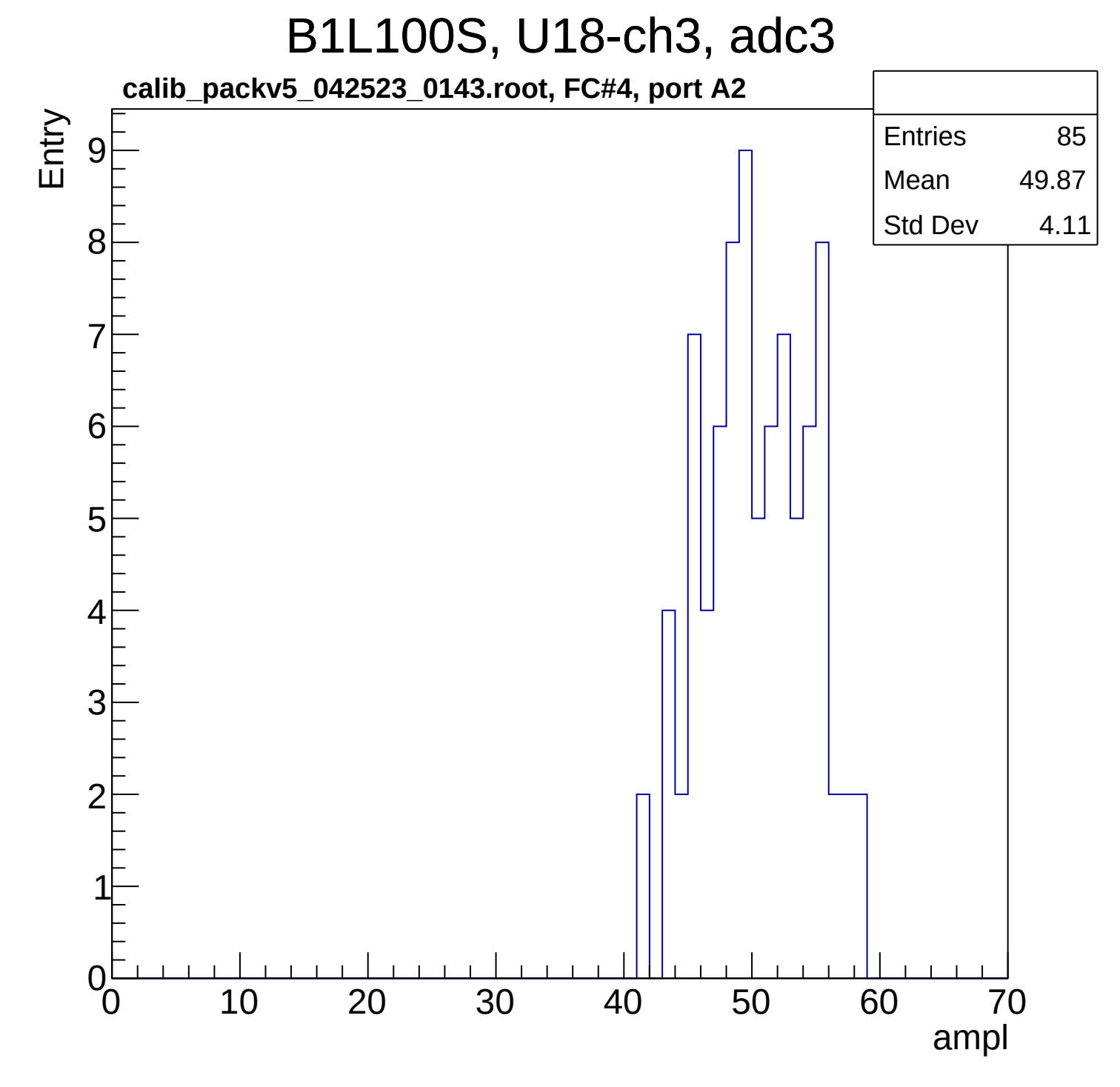

B1L100S, U18-ch2, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 62.5
Std Dev 0.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

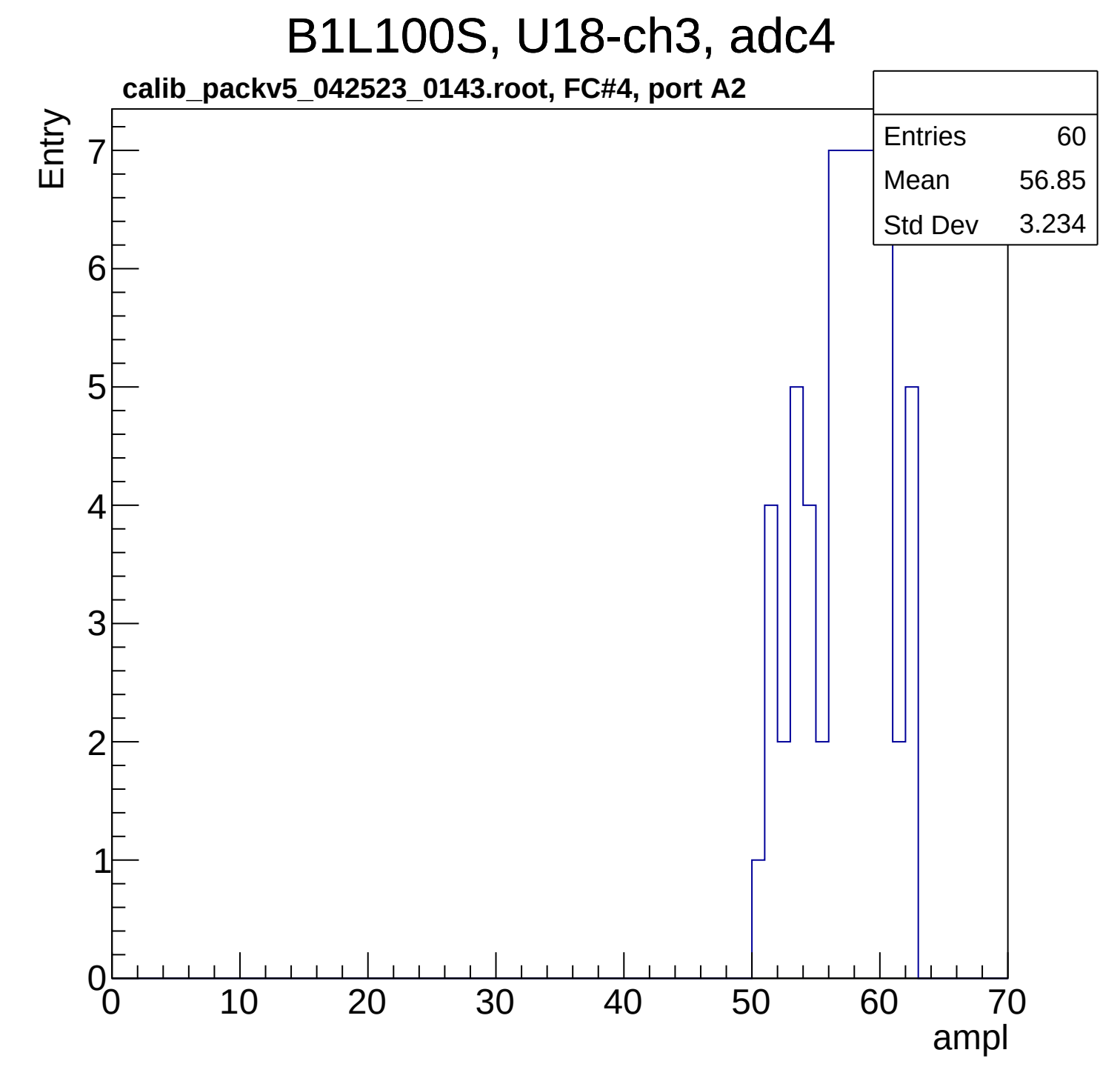

B1L100S, U18-ch2, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 0
Std Dev 0
Entry
3
2.5
2
1.5
1
0.5
0
0
10
20
30
40
50
60
70
ampl

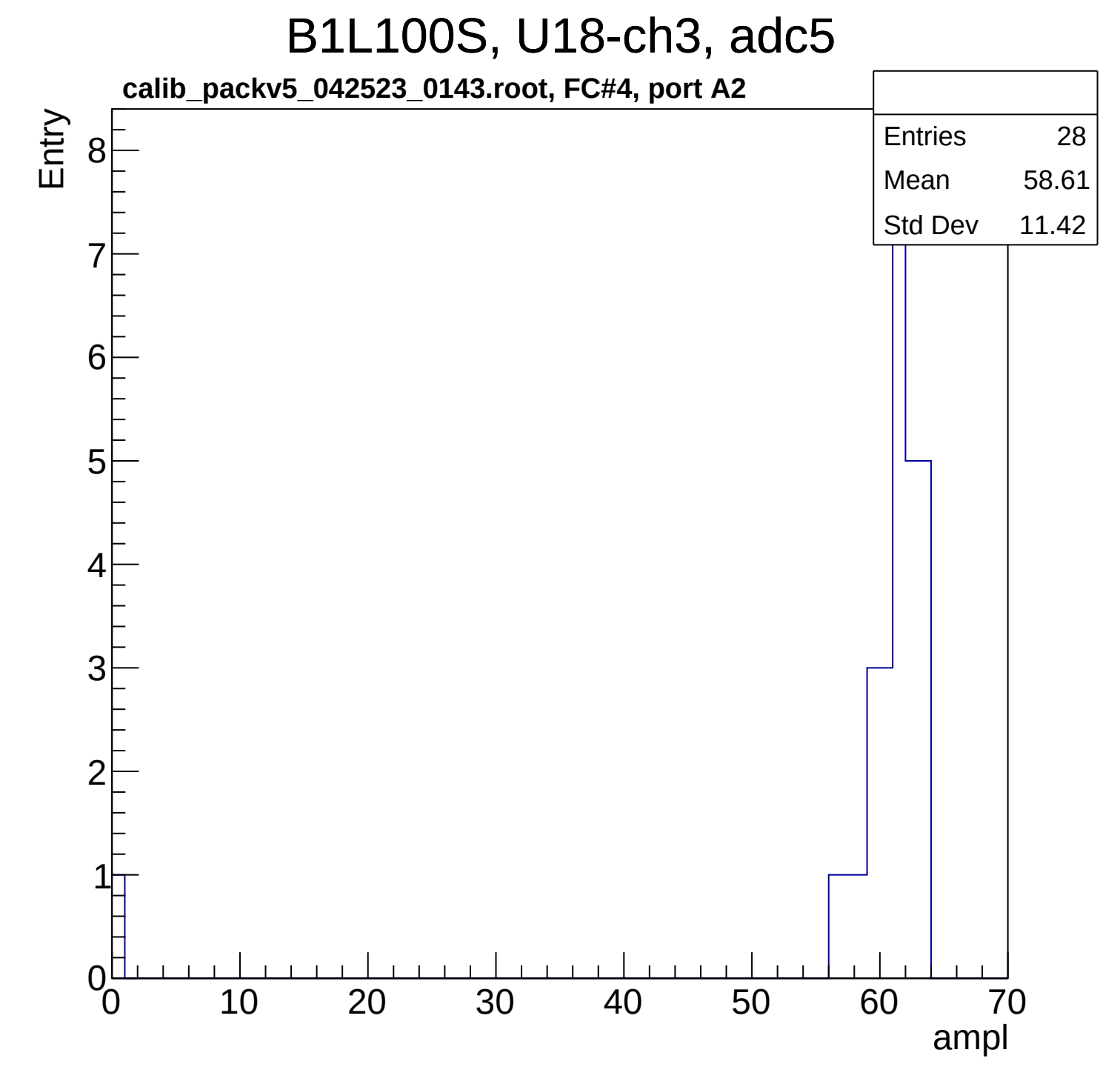

B1L100S, U18-ch3, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 31.16
Std Dev 3.836
Gaus mean : 30.5361
Gaus Width: 3.5929
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

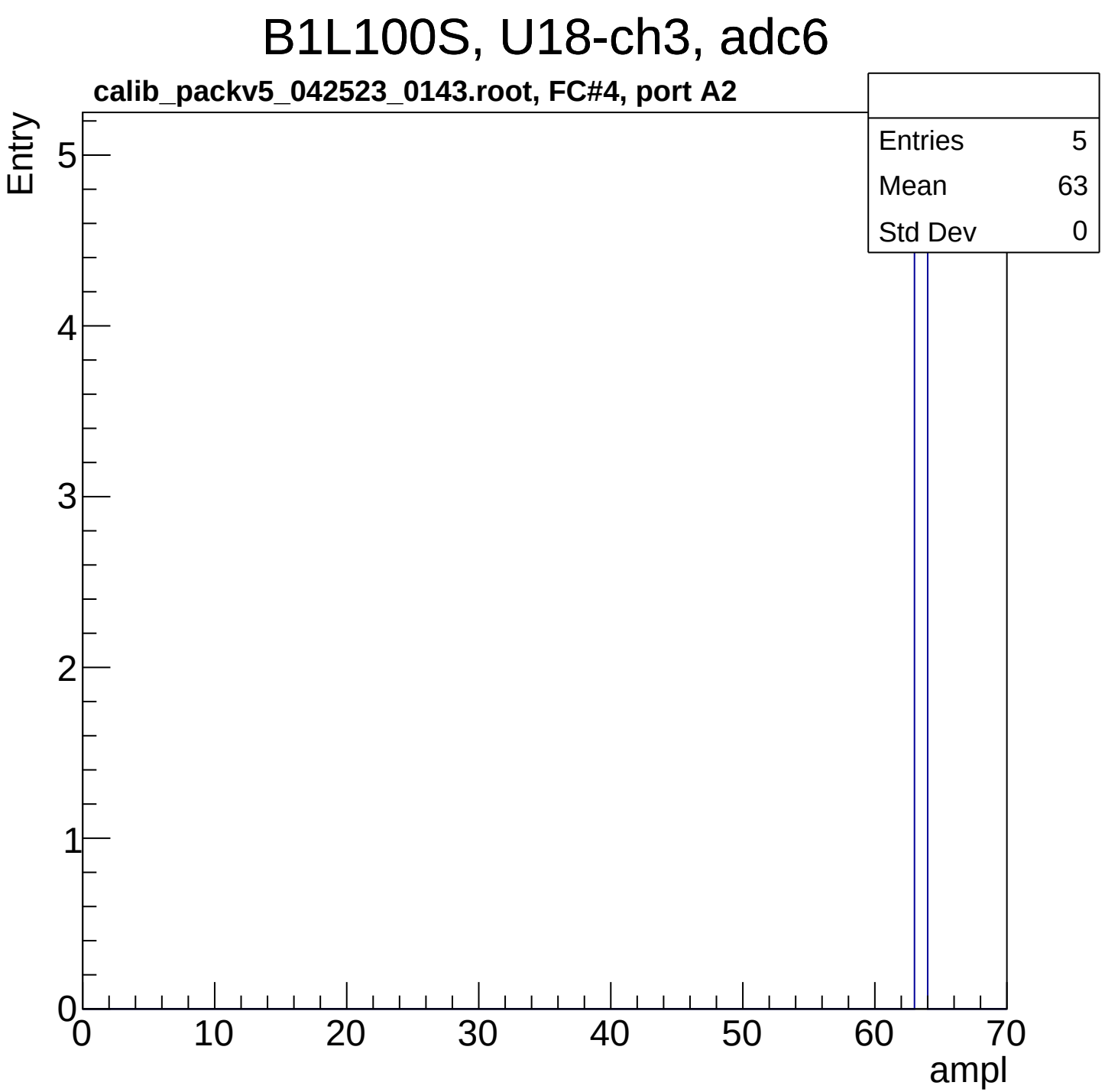

B1L100S, U18-ch3, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 36.67
Std Dev 3.367
Gaus mean : 37.4872
Gaus Width: 3.7733
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

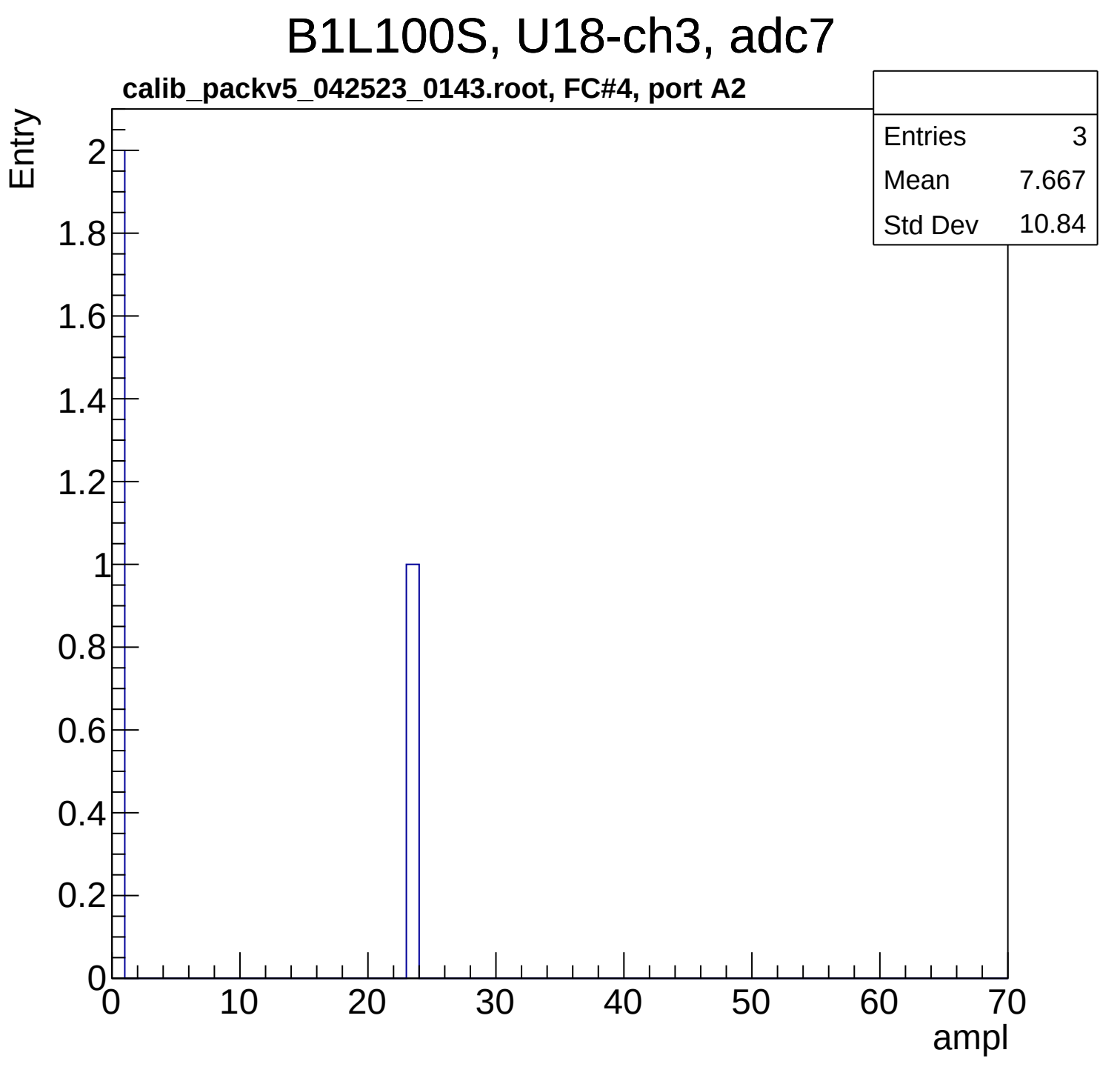

B1L100S, U18-ch3, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 43.83
Std Dev 3.575
Gaus mean : 44.2717
Gaus Width: 4.0504
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

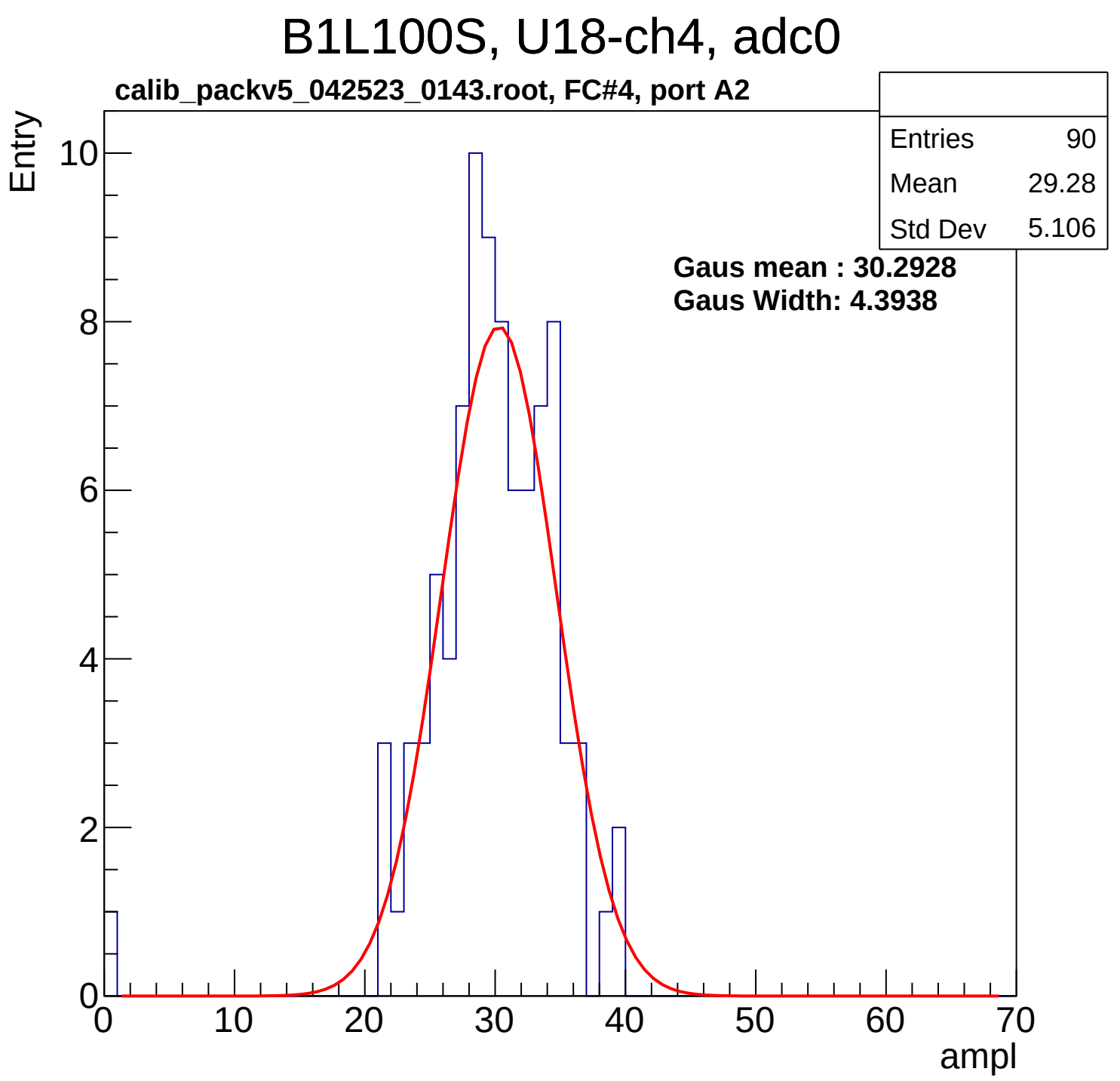

B1L100S, U18-ch3, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 85
Mean 49.87
Std Dev 4.11
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

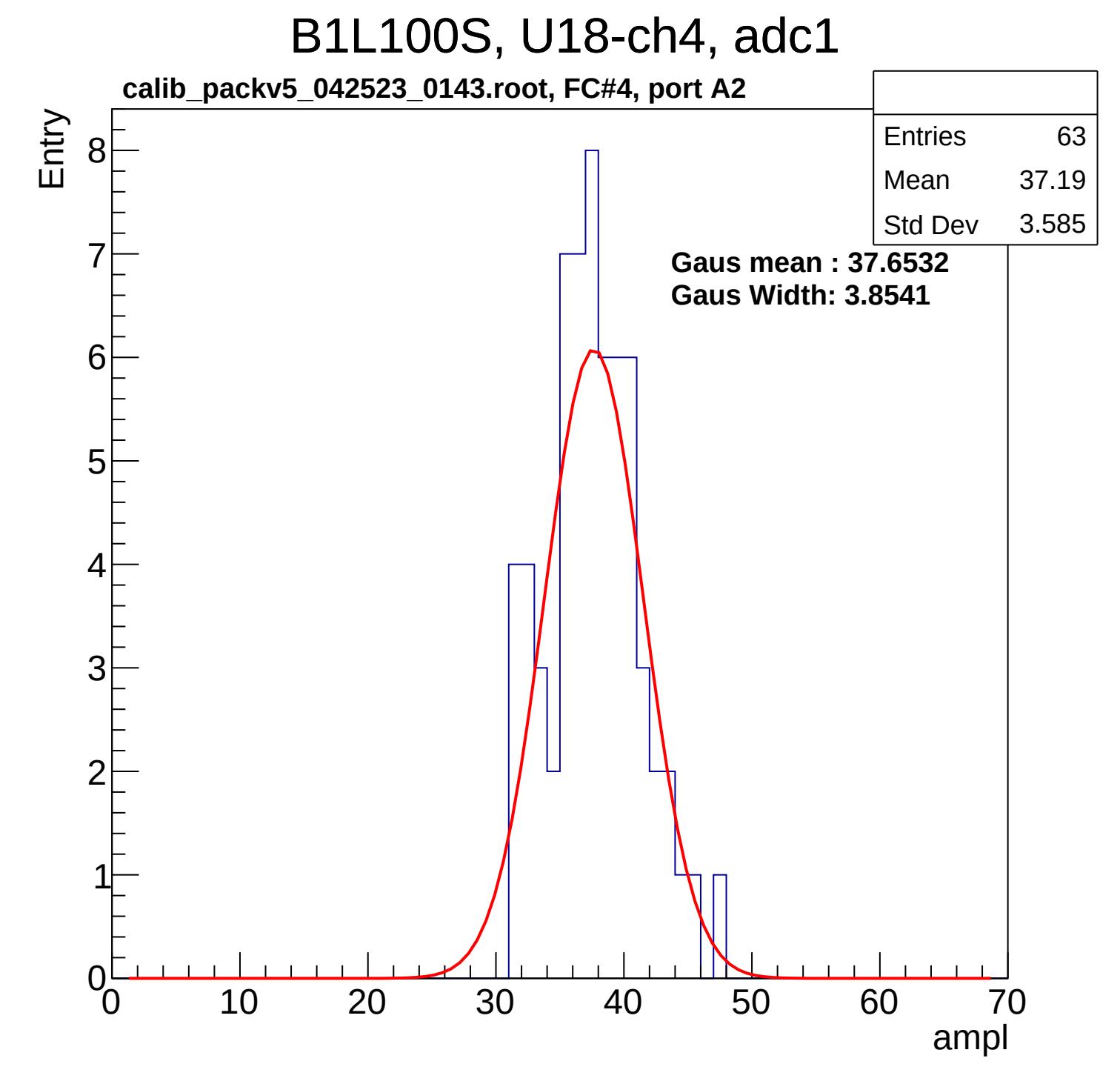

B1L100S, U18-ch3, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 56.85
Std Dev 3.234
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

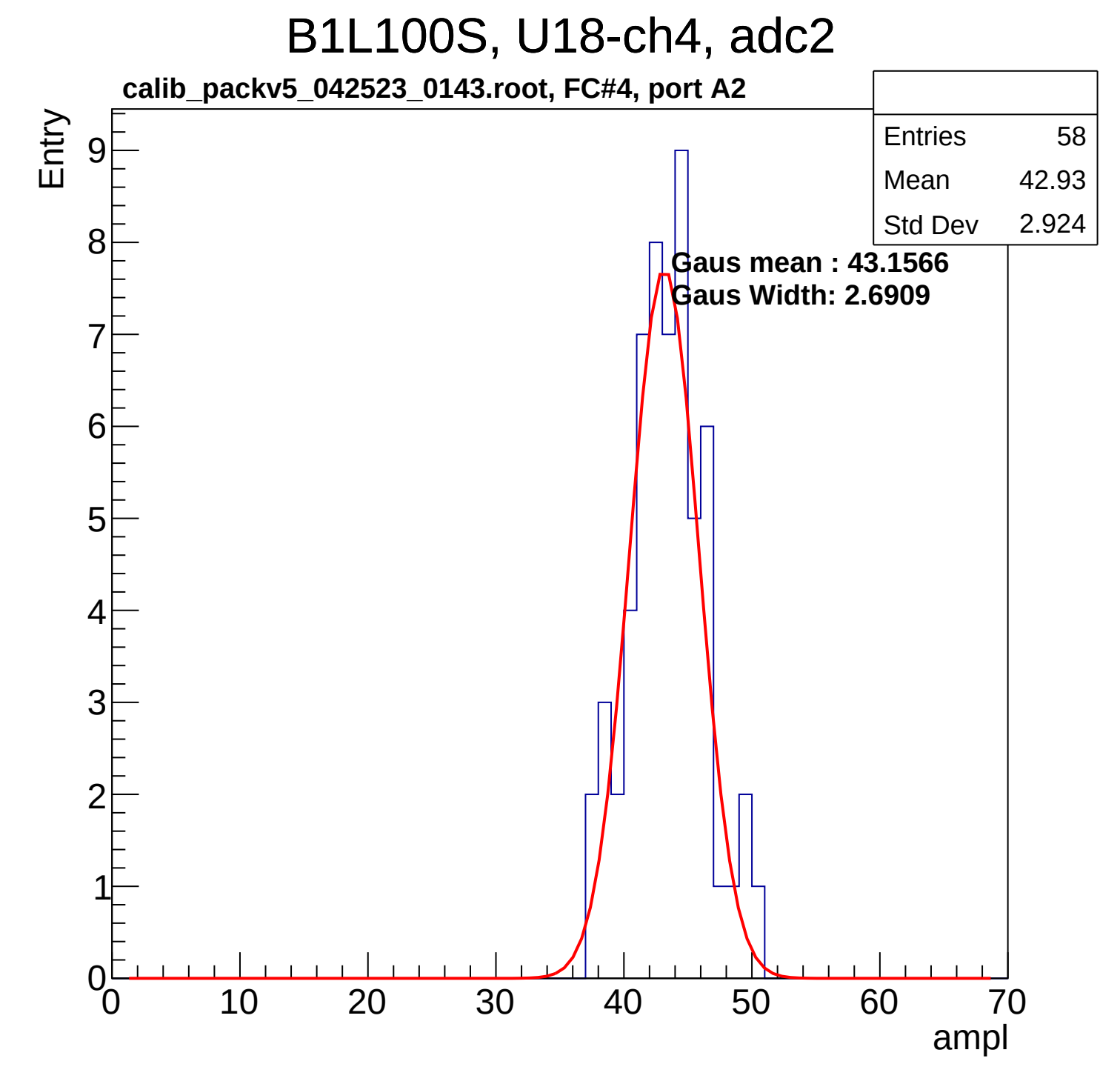

B1L100S, U18-ch3, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 28
Mean 58.61
Std Dev 11.42
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

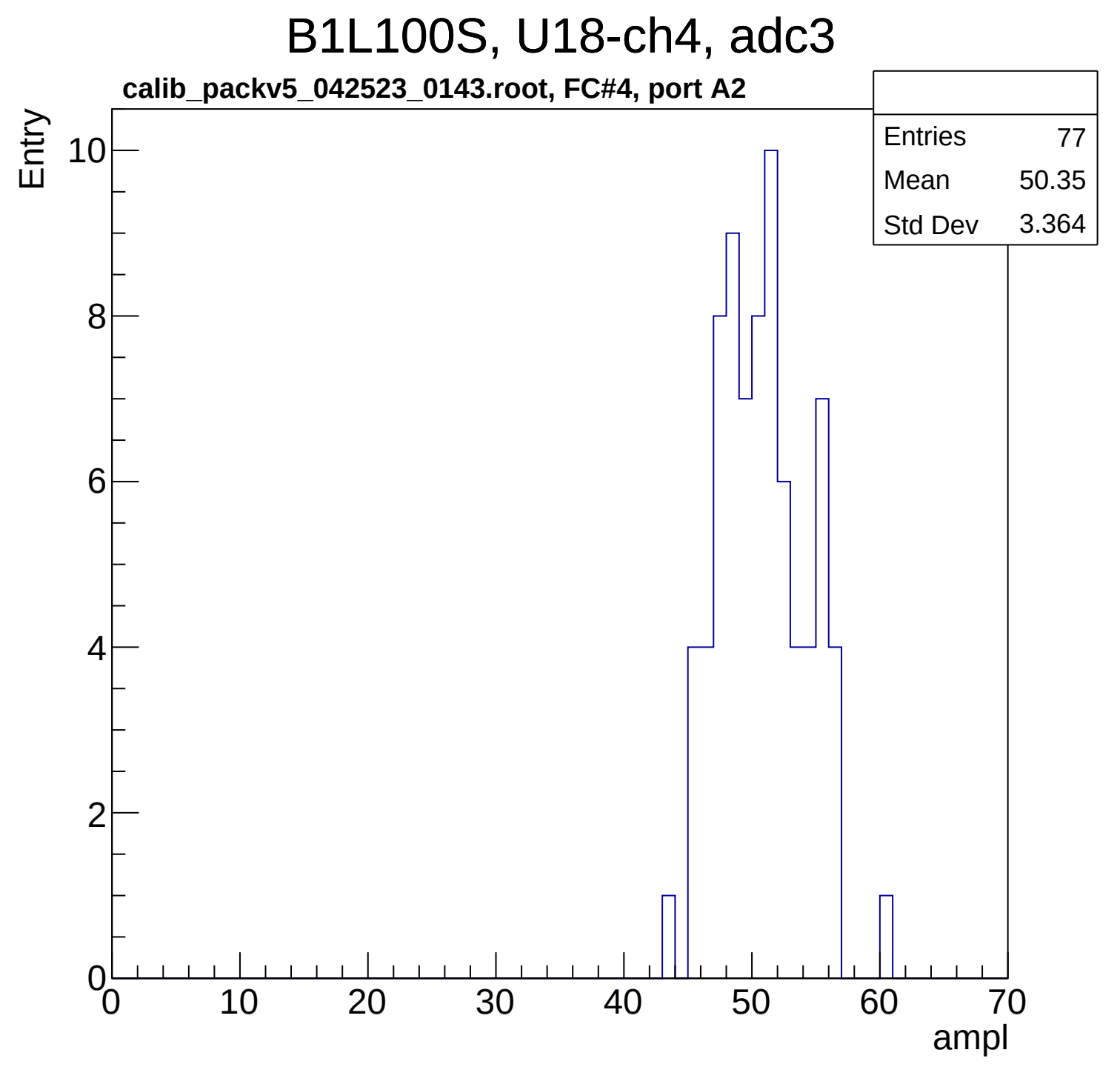

B1L100S, U18-ch3, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 5
Mean 63
Std Dev 0
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

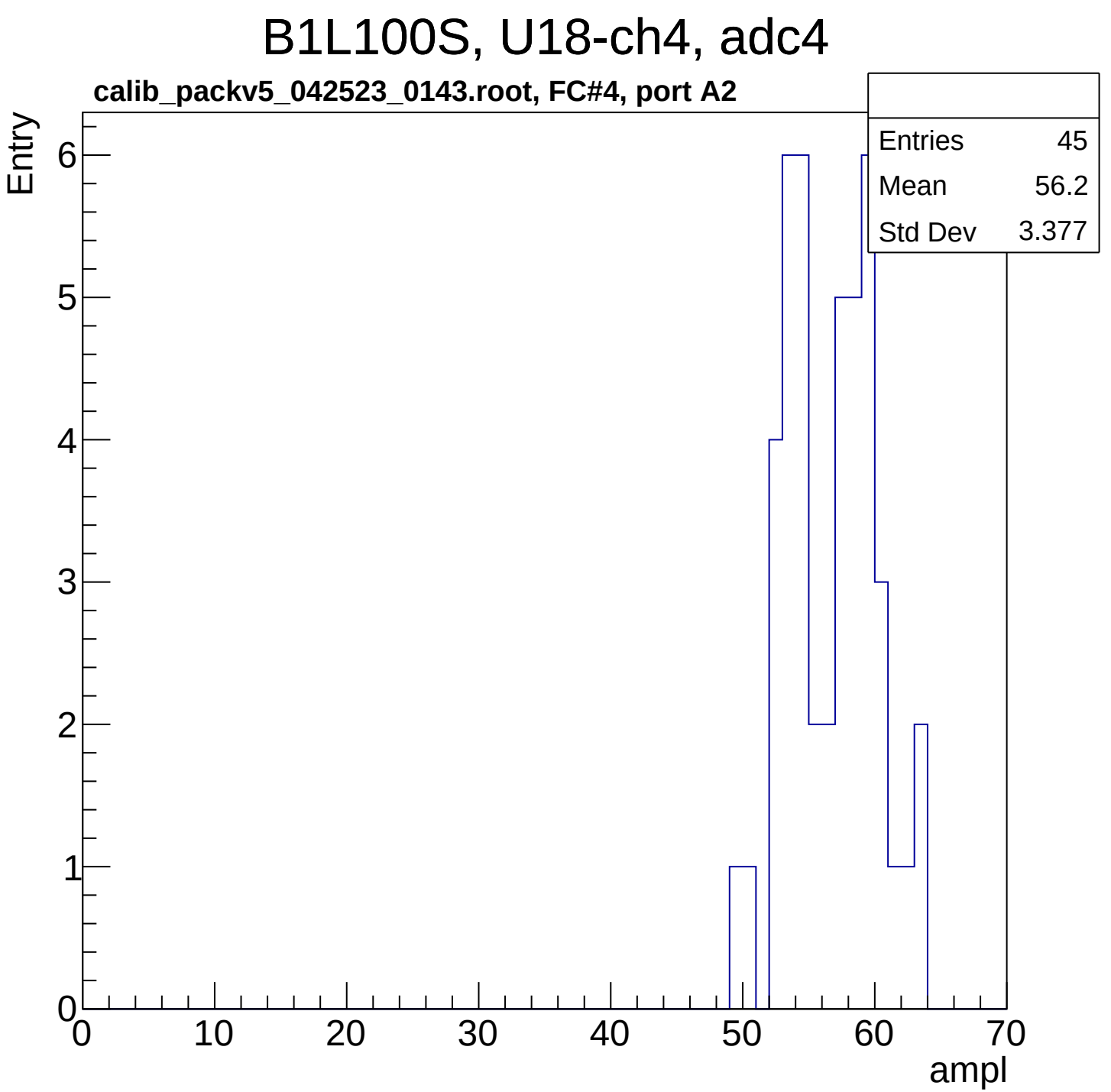

B1L100S, U18-ch3, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 7.667
Std Dev 10.84
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

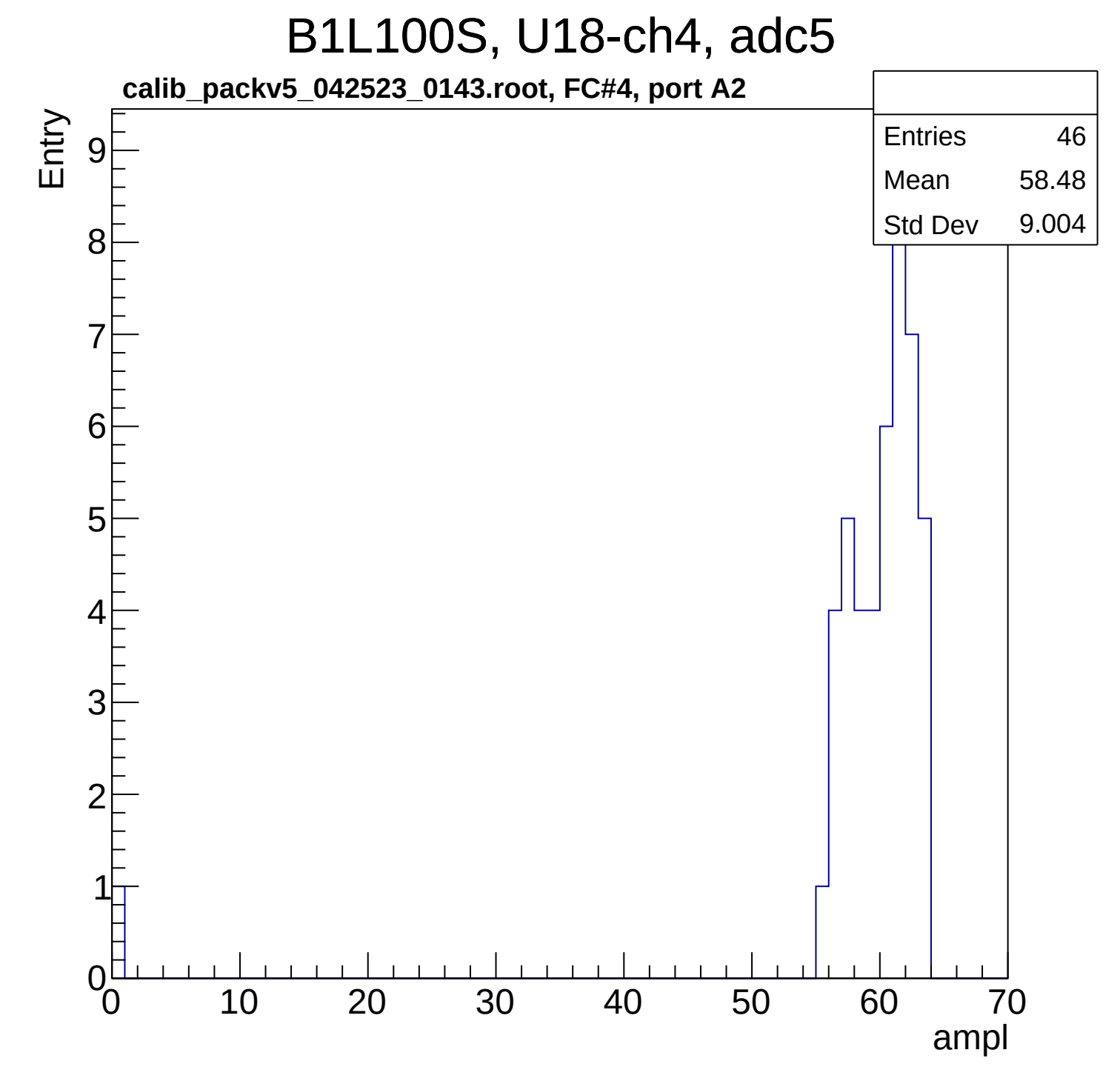

B1L100S, U18-ch4, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 90
Mean 29.28
Std Dev 5.106
Gaus mean : 30.2928
Gaus Width: 4.3938
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

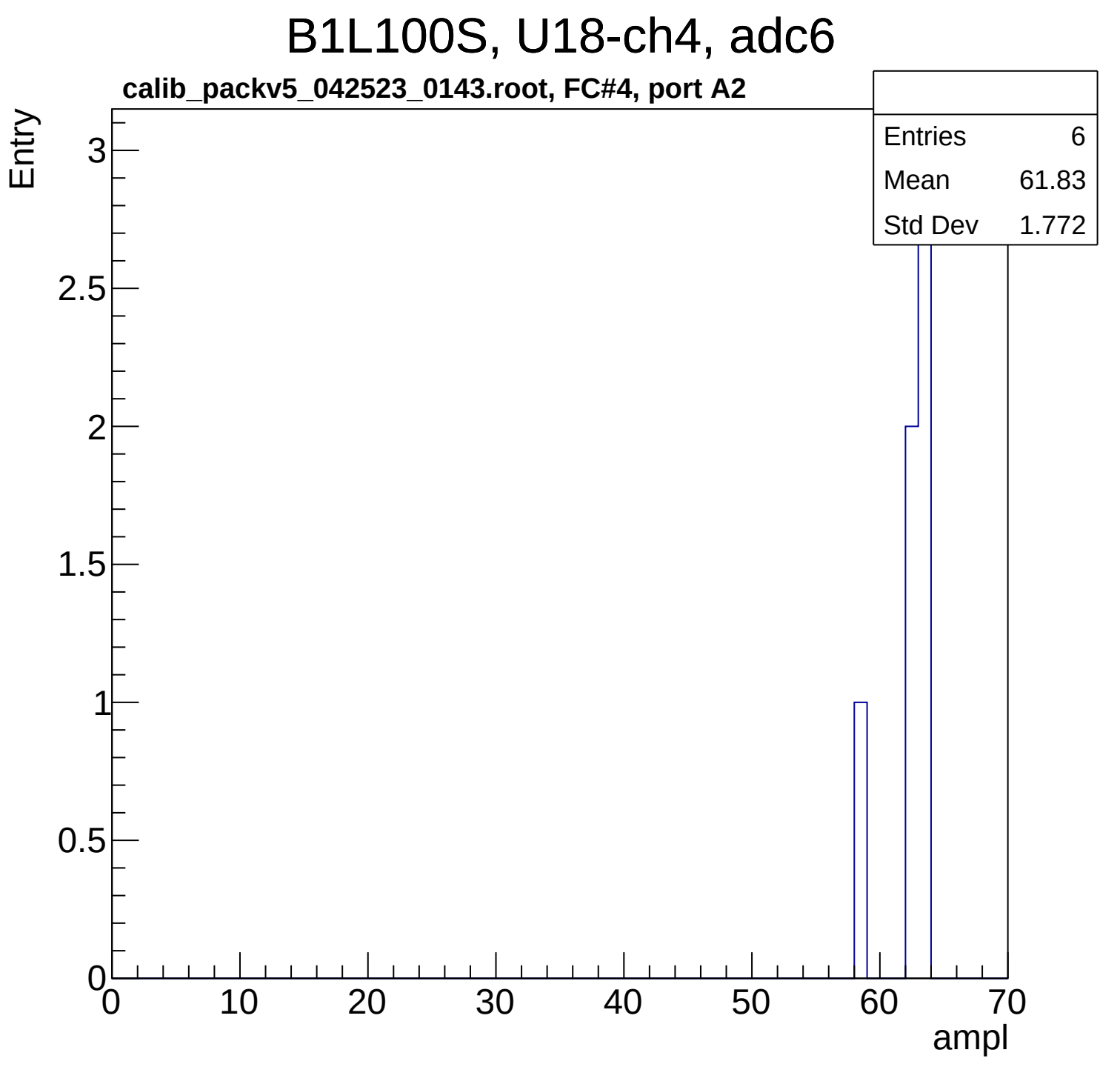

B1L100S, U18-ch4, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 37.19
Std Dev 3.585
Gaus mean : 37.6532
Gaus Width: 3.8541
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

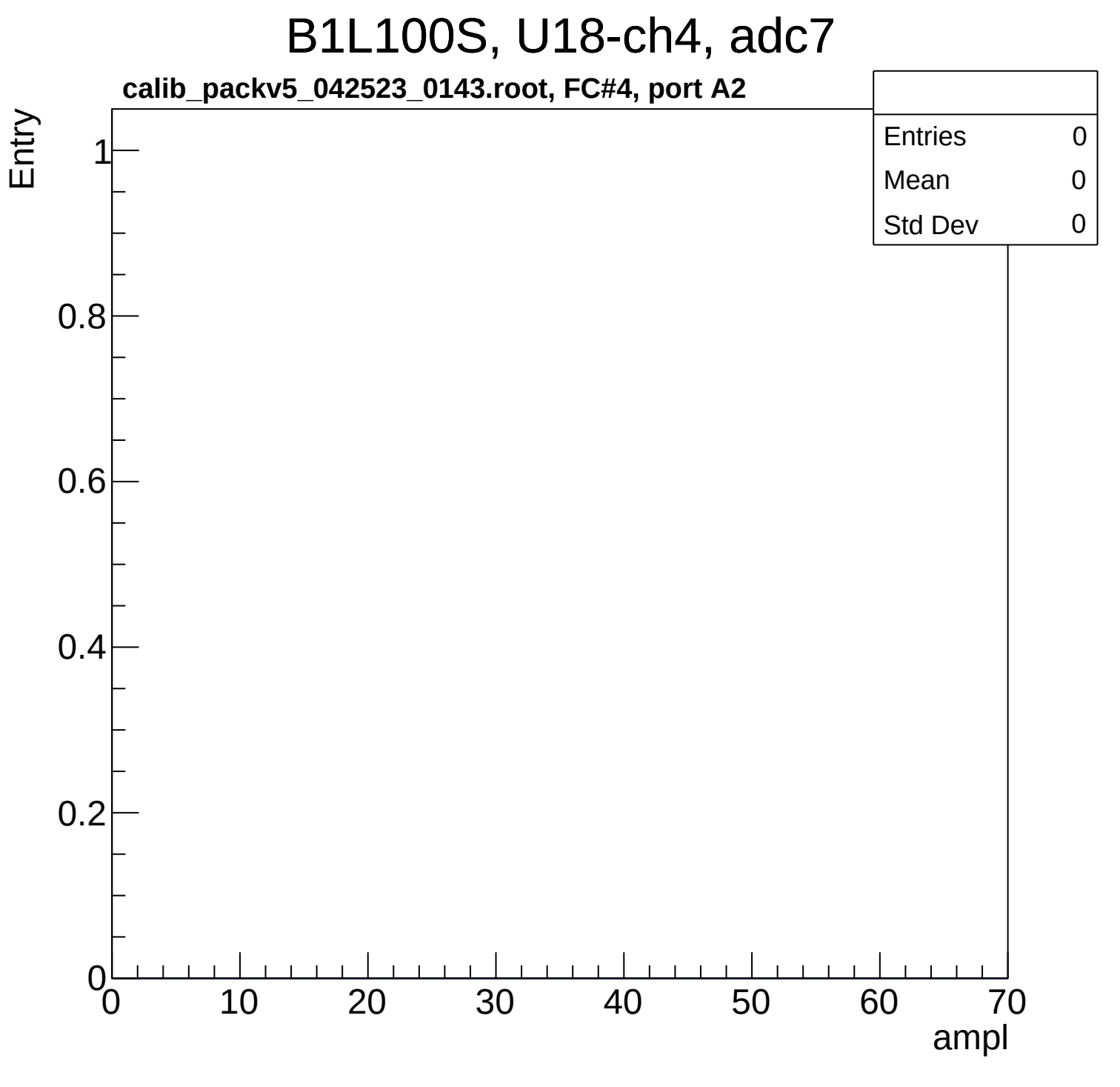

B1L100S, U18-ch4, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 42.93
Std Dev 2.924
Gaus mean : 43.1566
Gaus Width: 2.6909
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

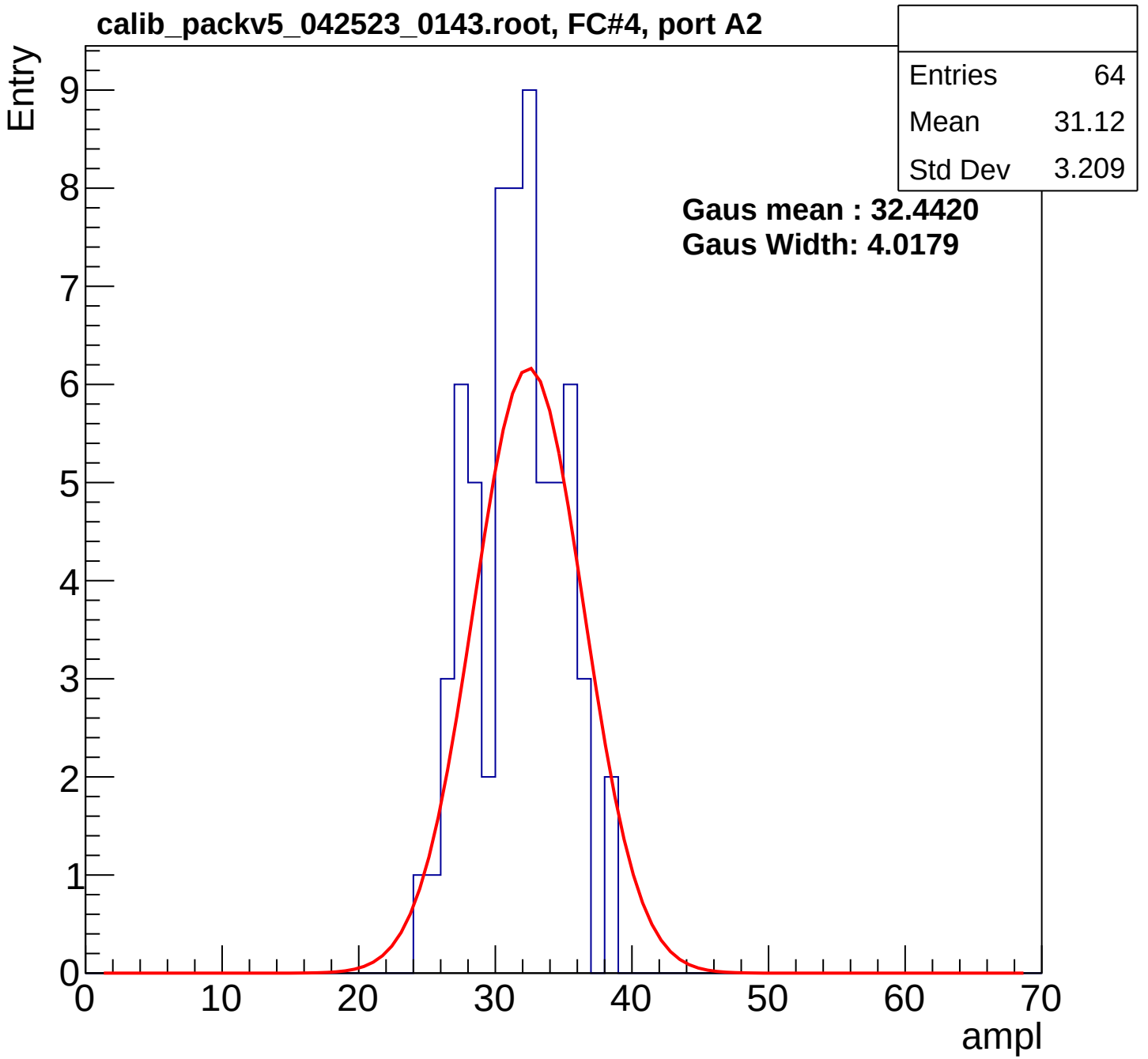

B1L100S, U18-ch4, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 50.35
Std Dev 3.364
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

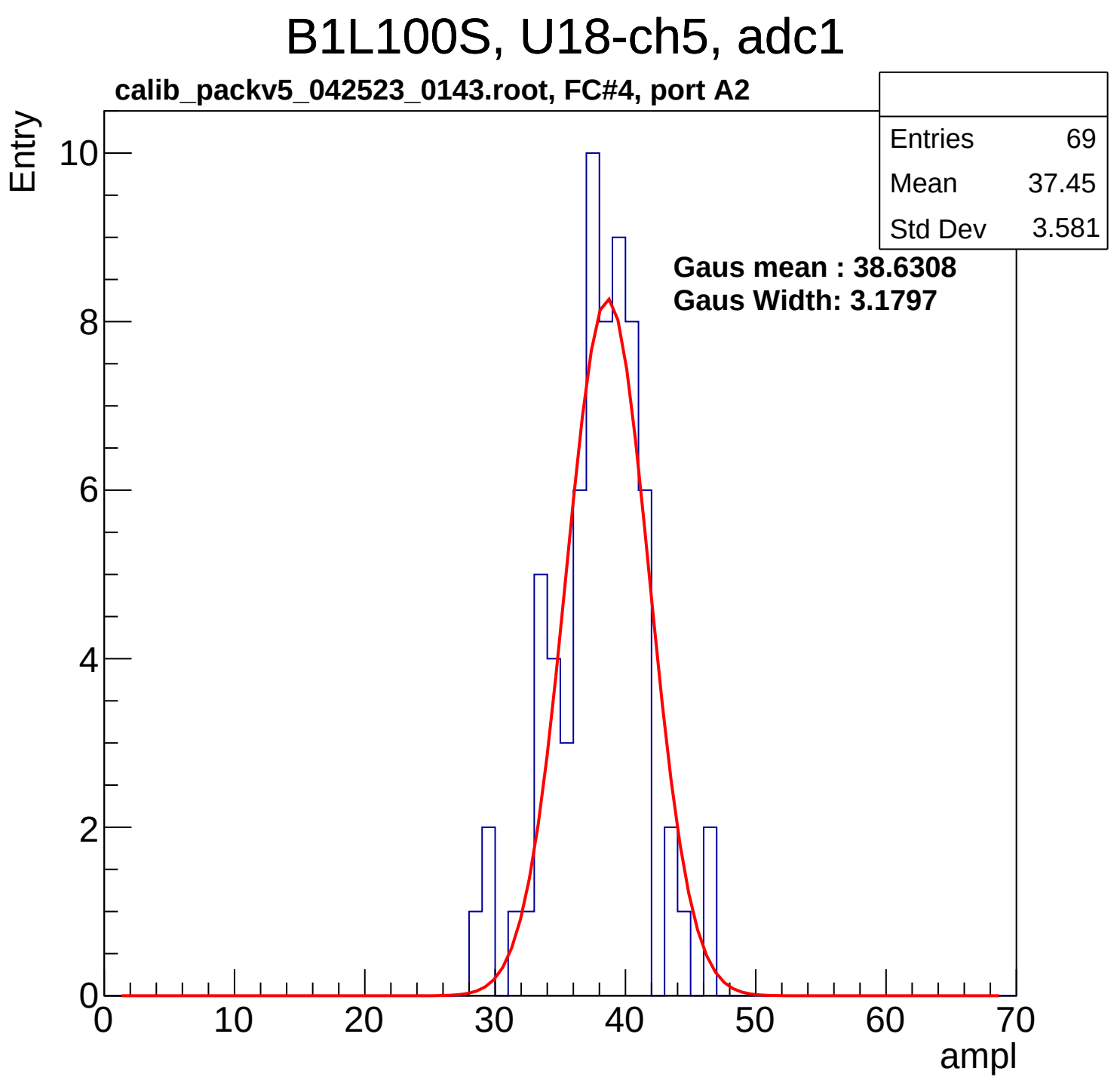

B1L100S, U18-ch4, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 45
Mean 56.2
Std Dev 3.377
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

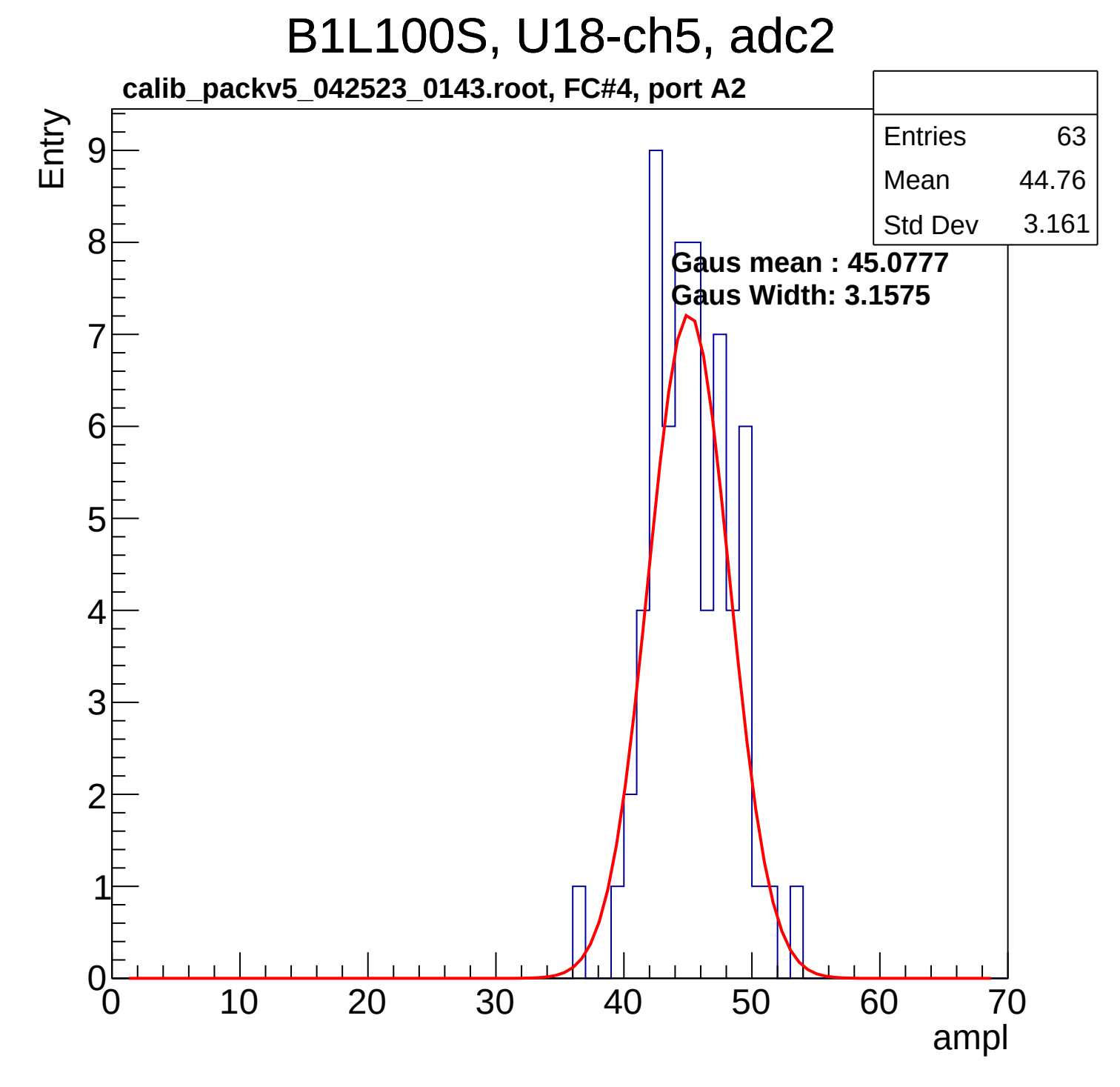

B1L100S, U18-ch4, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 58.48
Std Dev 9.004
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

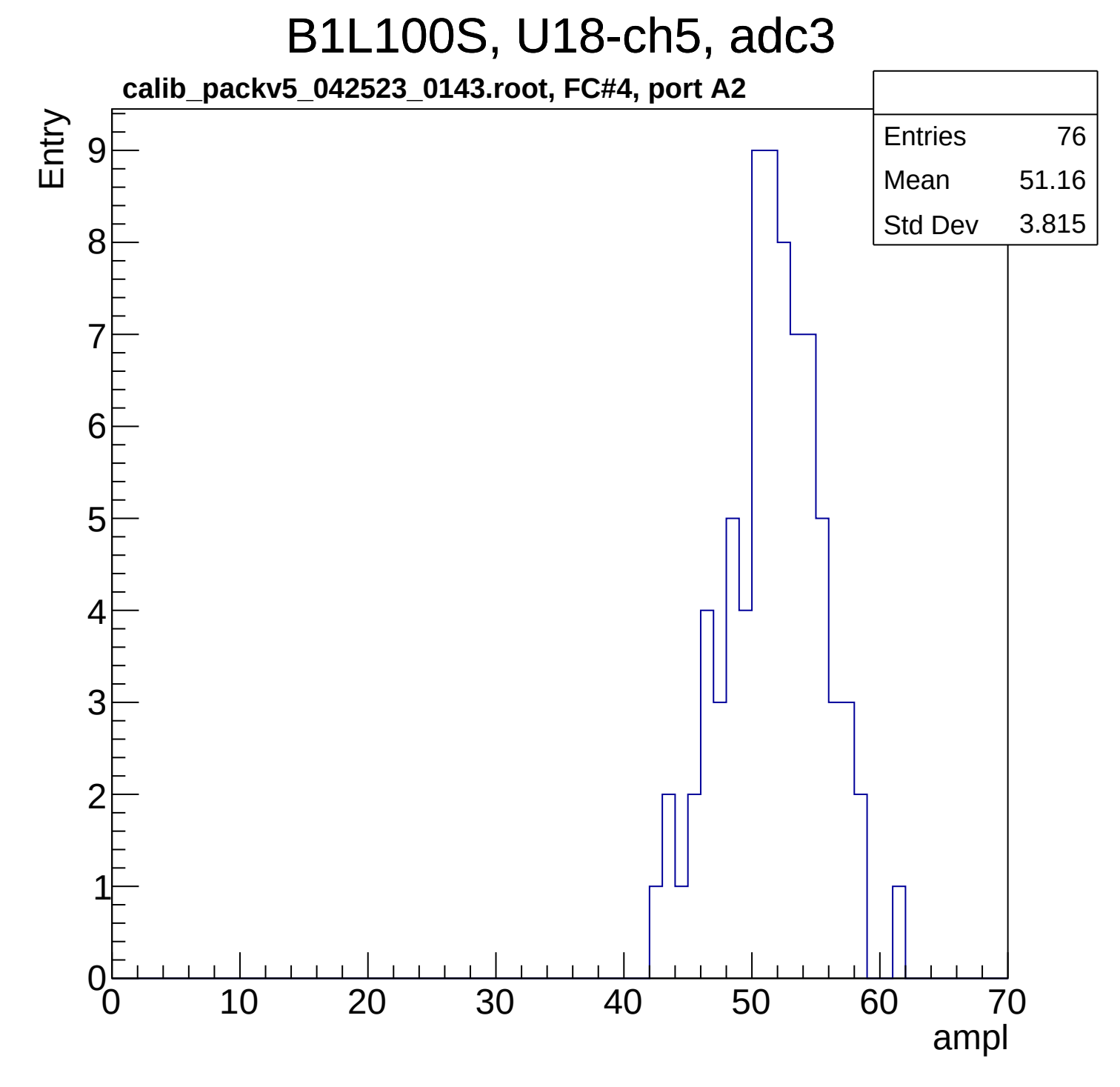

B1L100S, U18-ch4, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 61.83
Std Dev 1.772
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

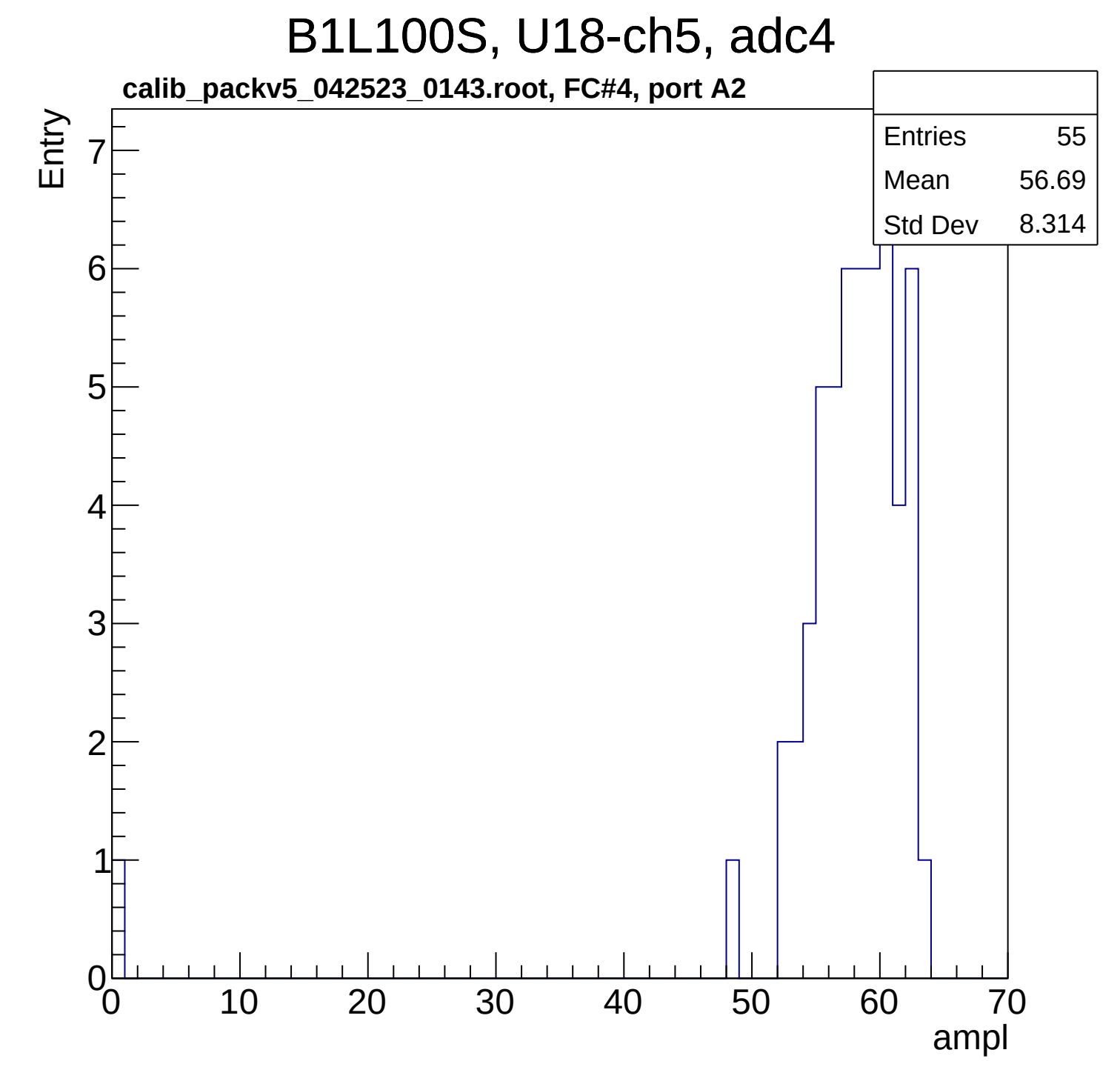

B1L100S, U18-ch4, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

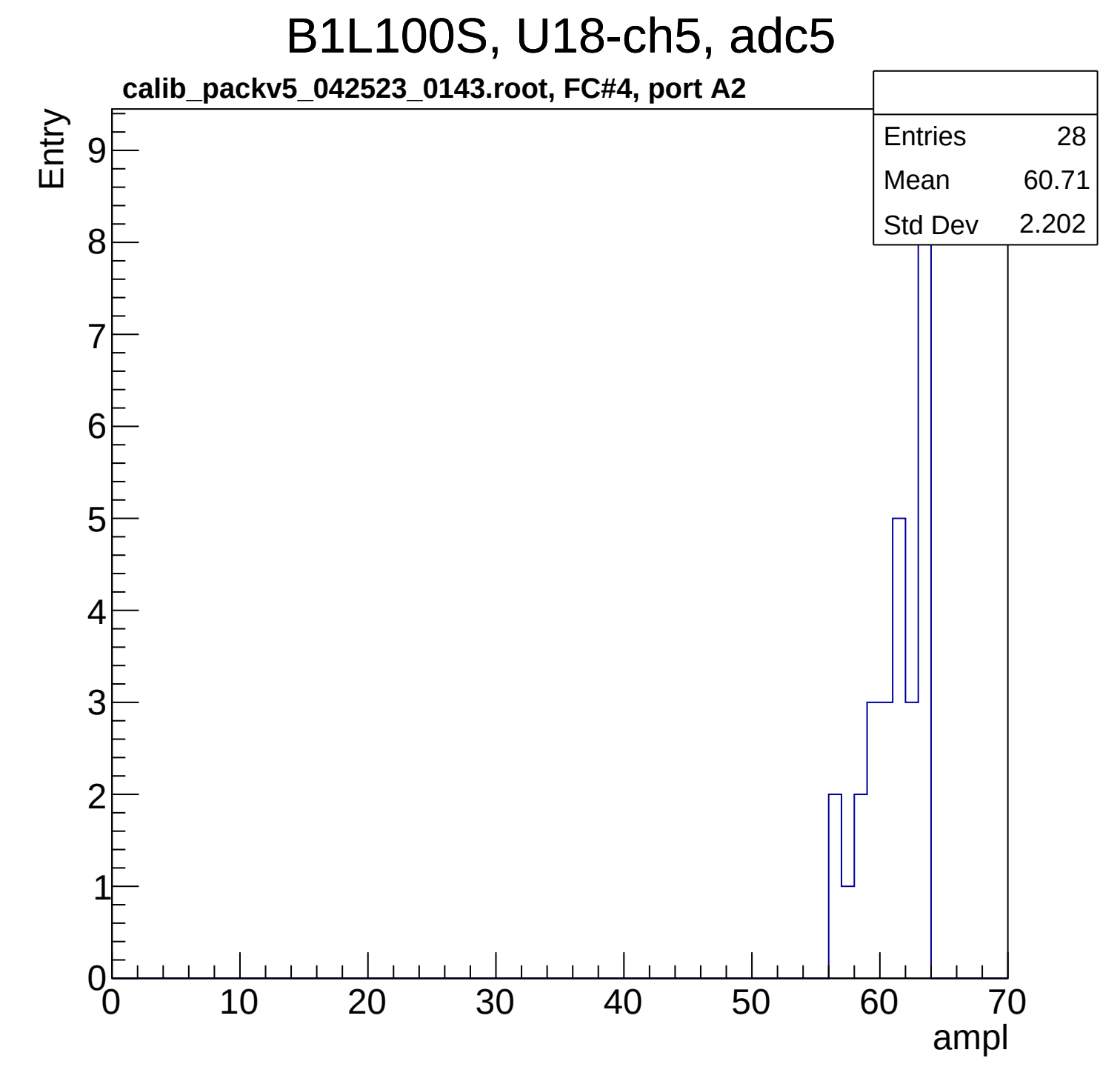

B1L100S, U18-ch5, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 31.12
Std Dev 3.209
Gaus mean : 32.4420
Gaus Width: 4.0179
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

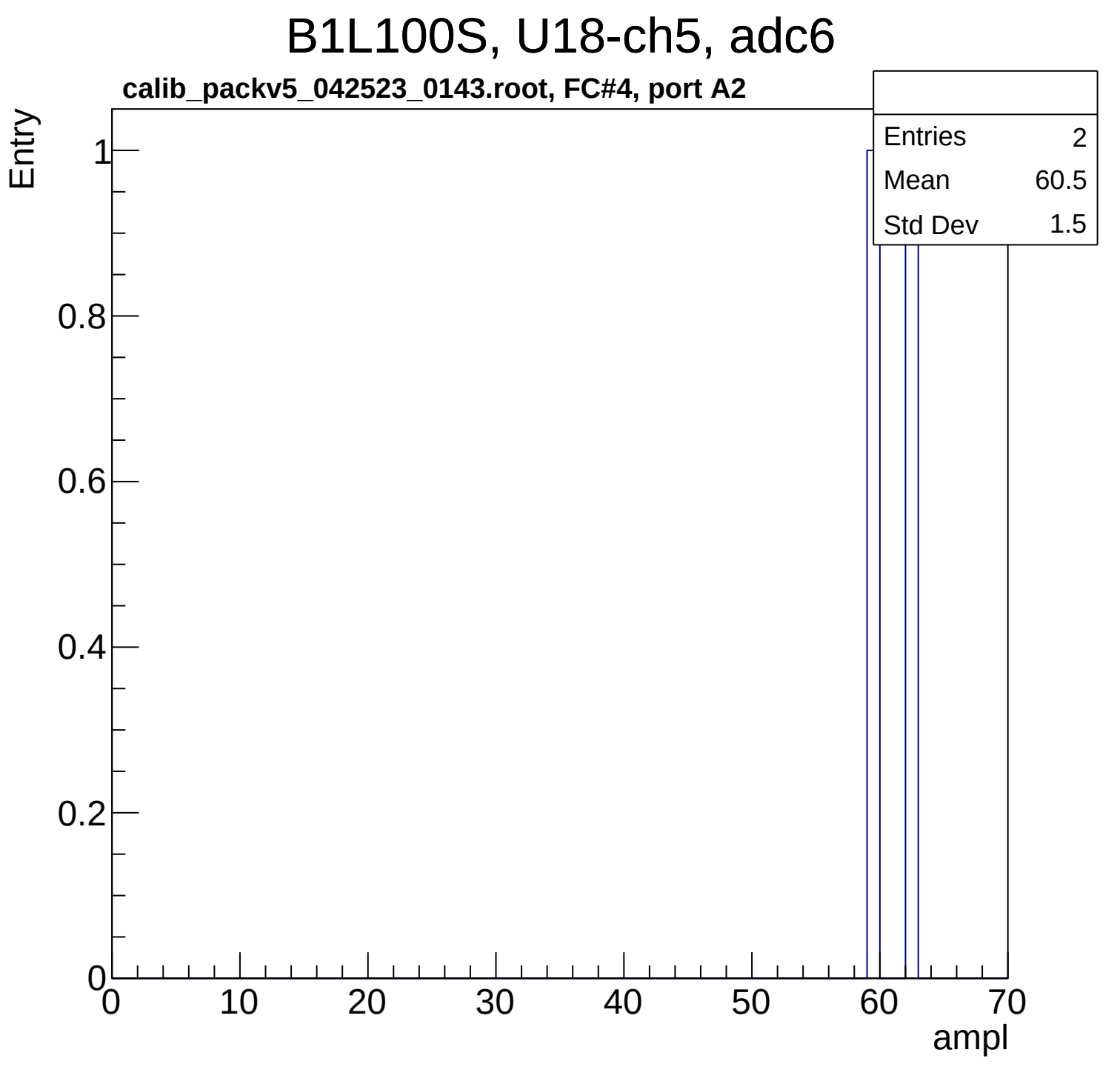

B1L100S, U18-ch5, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 37.45
Std Dev 3.581
Gaus mean : 38.6308
Gaus Width: 3.1797
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

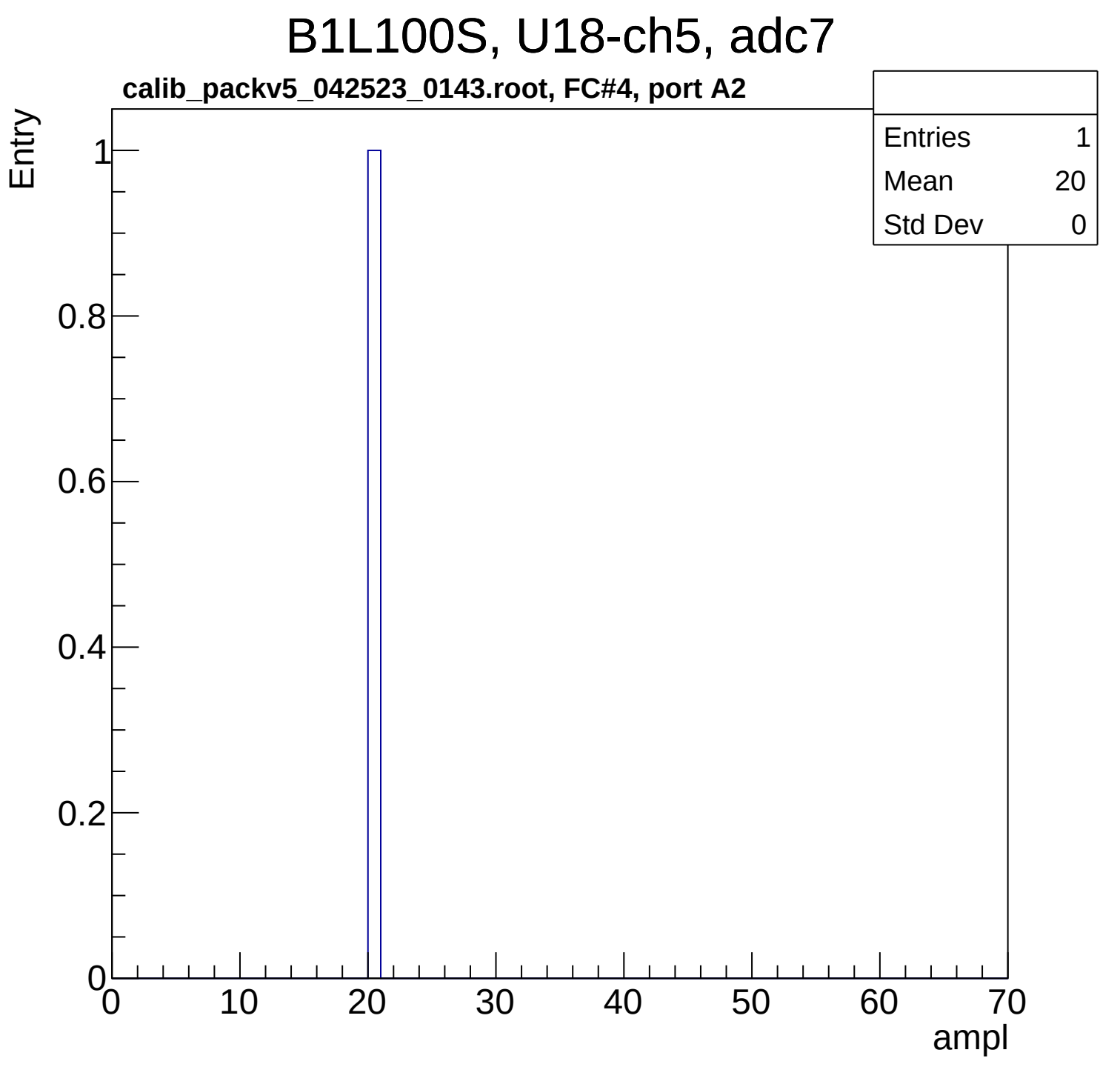

B1L100S, U18-ch5, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 44.76
Std Dev 3.161
Gaus mean : 45.0777
Gaus Width: 3.1575
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

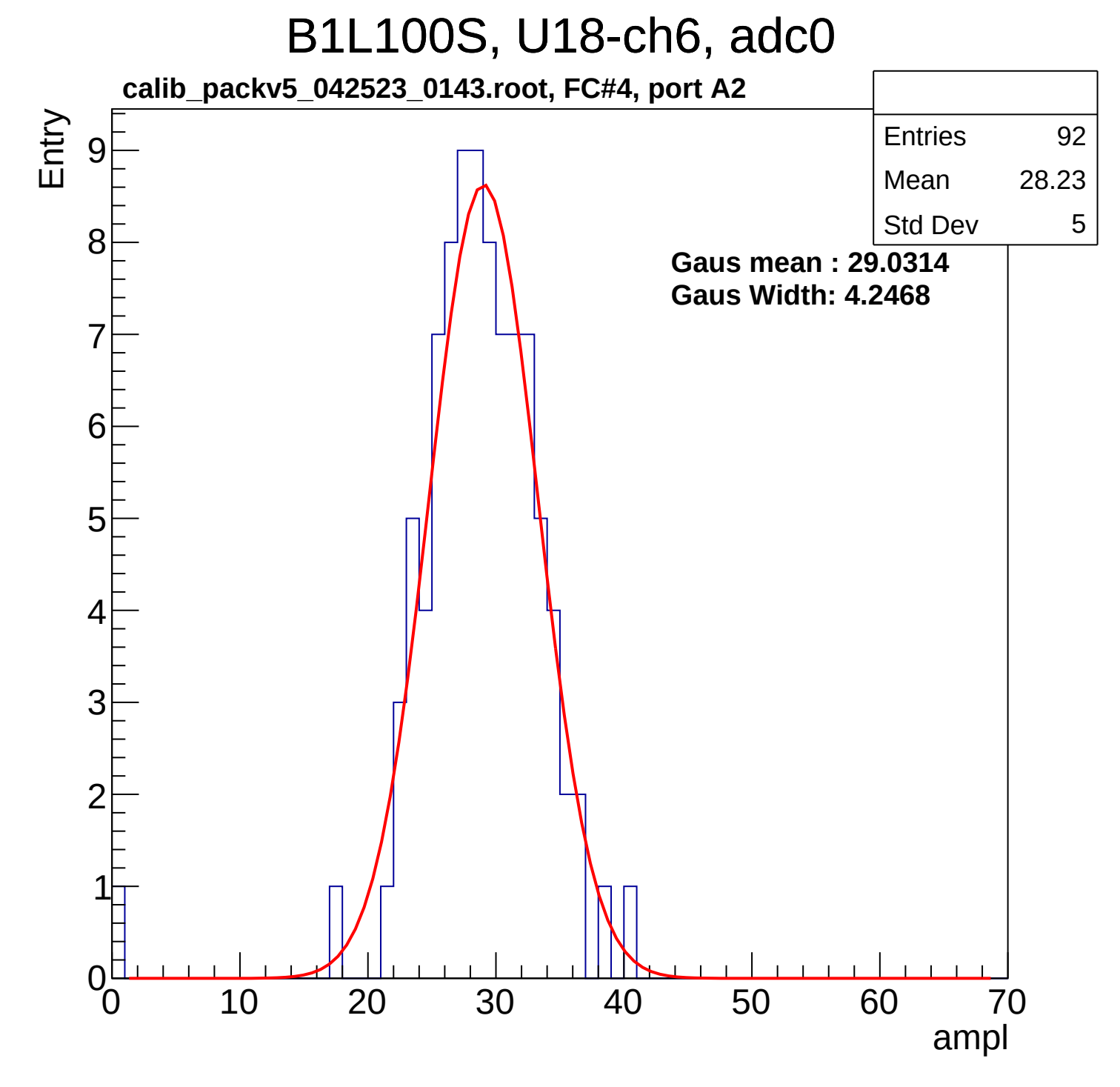

B1L100S, U18-ch5, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 51.16
Std Dev 3.815
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

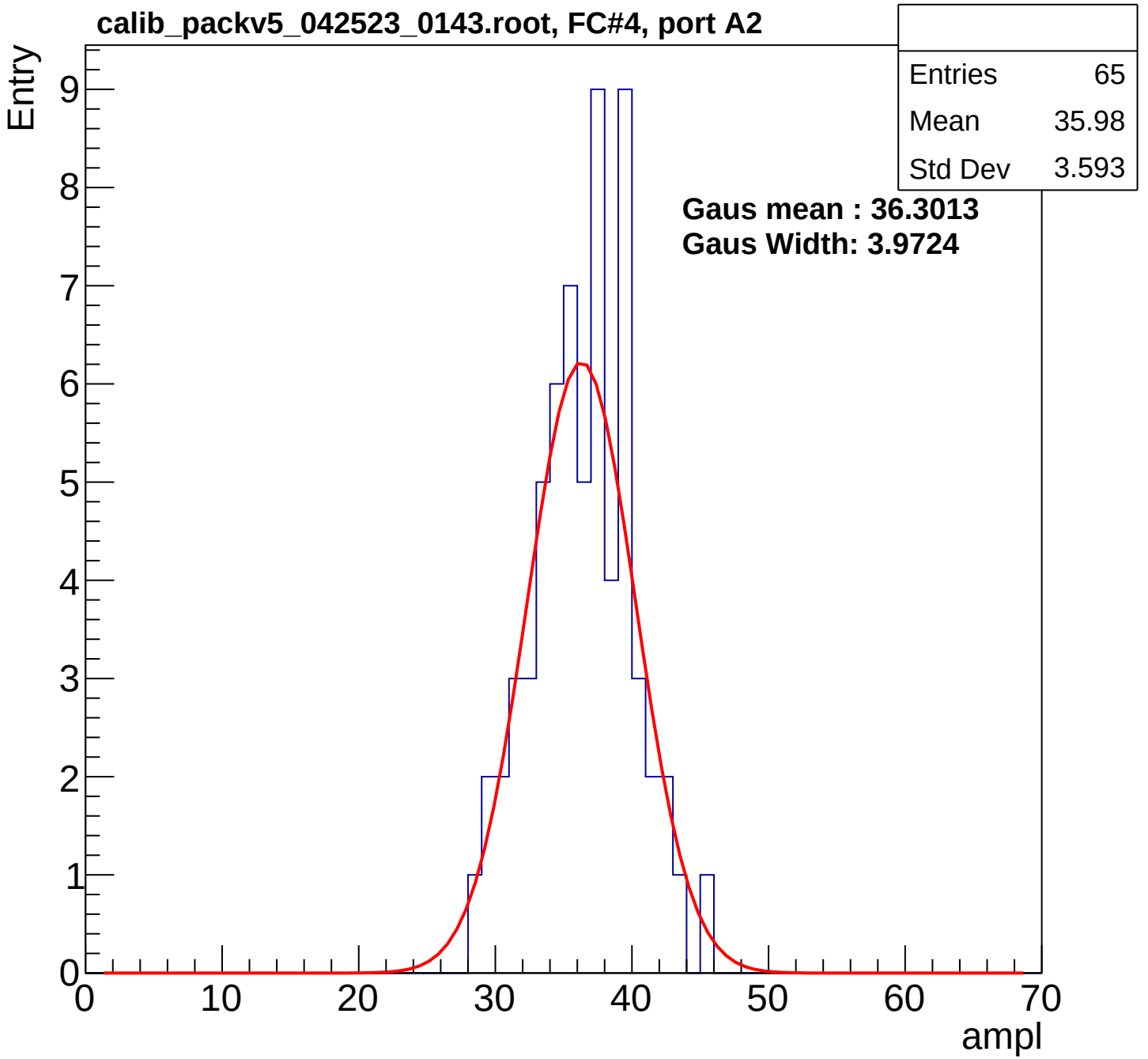

B1L100S, U18-ch5, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 56.69
Std Dev 8.314
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

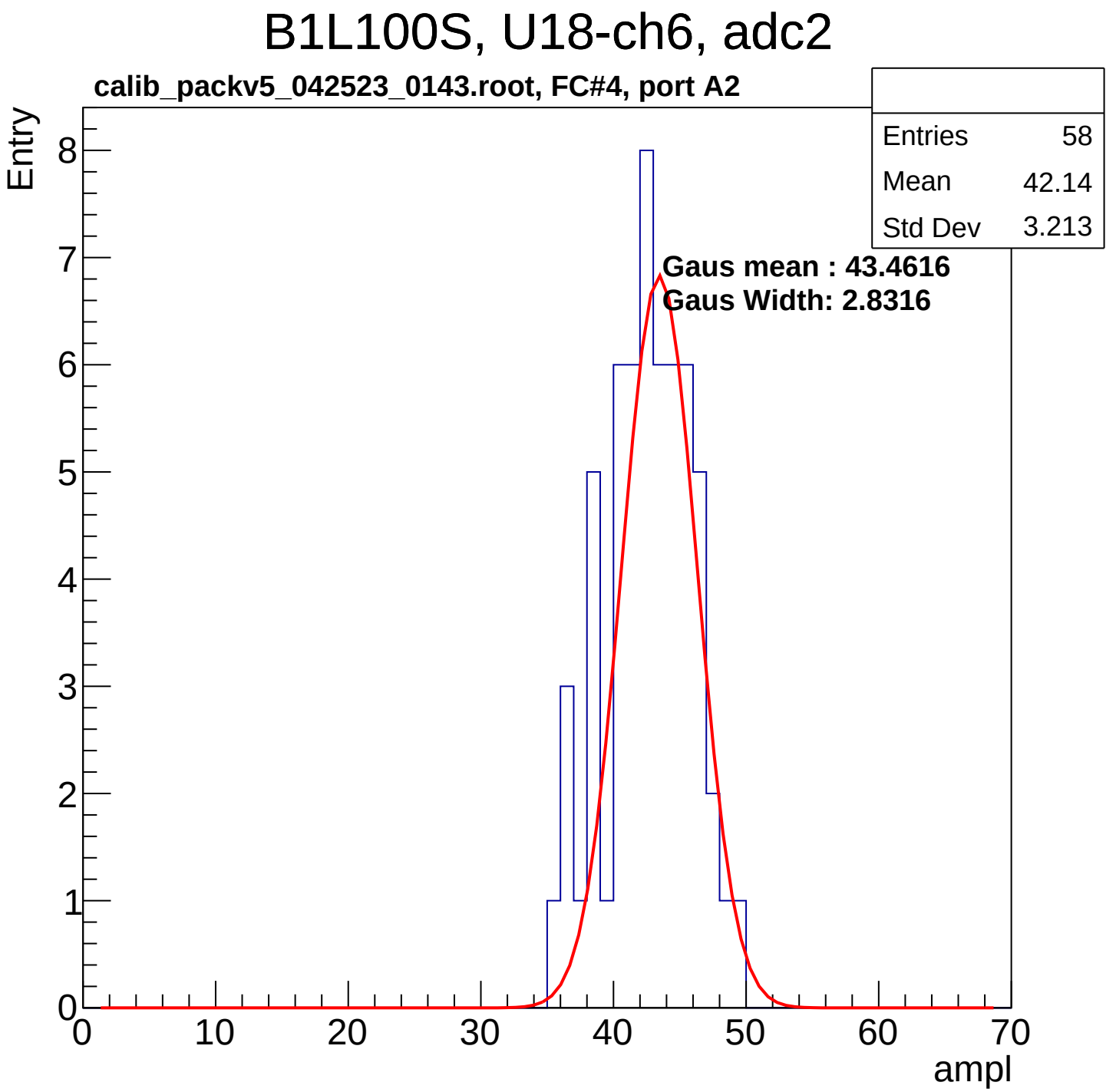

B1L100S, U18-ch5, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 28
Mean 60.71
Std Dev 2.202
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

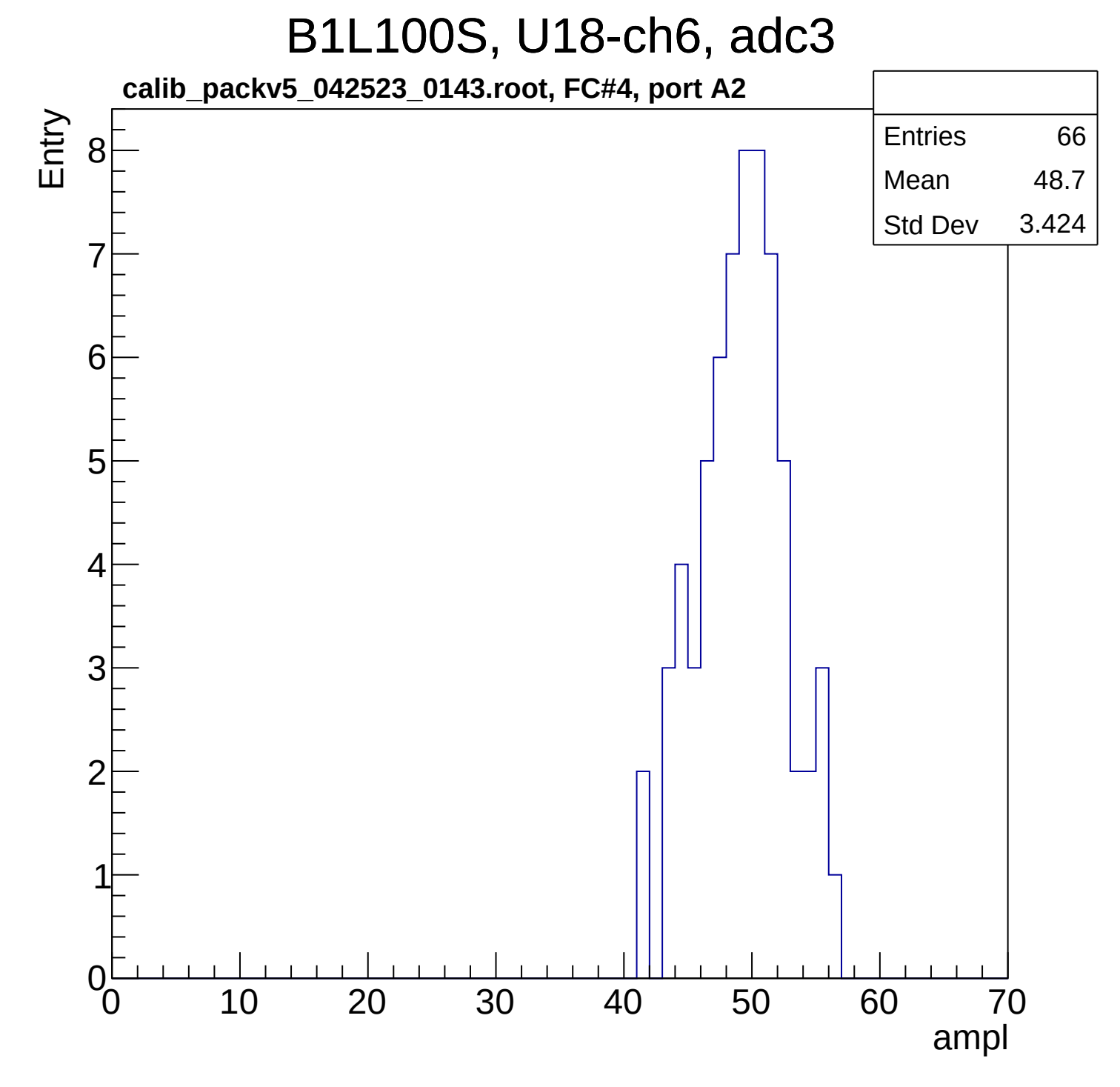

B1L100S, U18-ch5, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 60.5
Std Dev 1.5
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

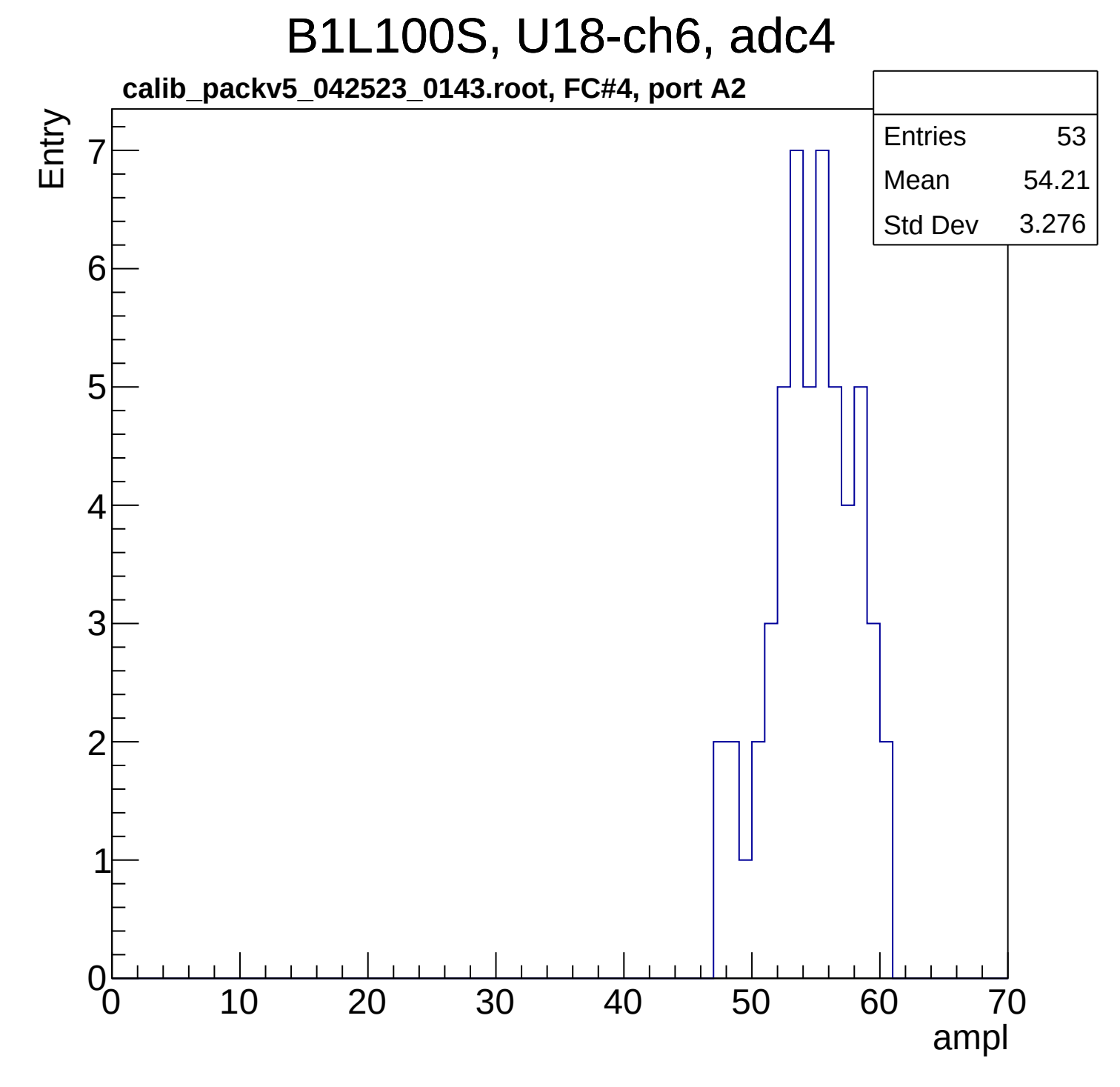

B1L100S, U18-ch5, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 20
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

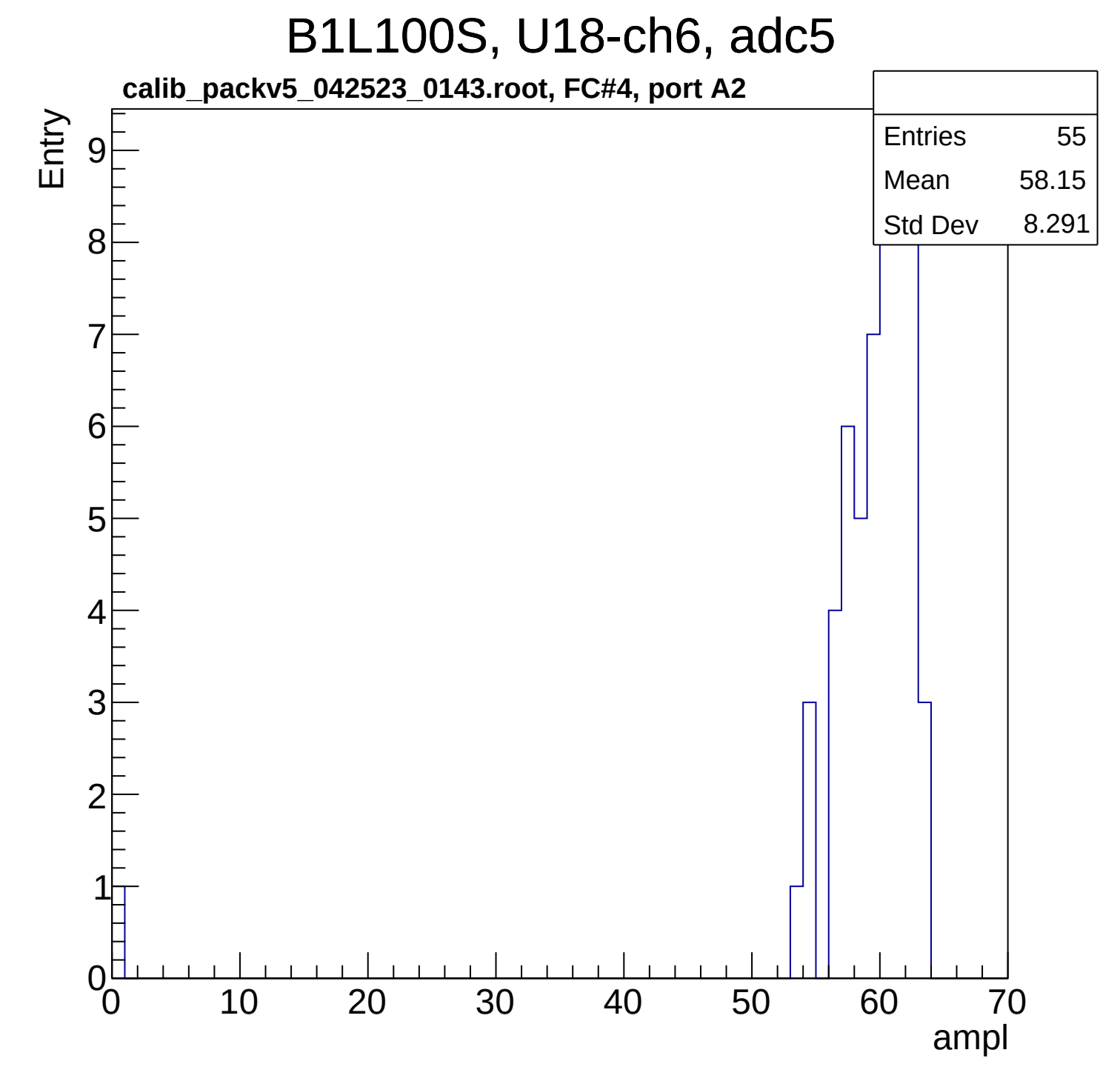

B1L100S, U18-ch6, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 92
Mean 28.23
Std Dev 5
Gaus mean : 29.0314
Gaus Width: 4.2468
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

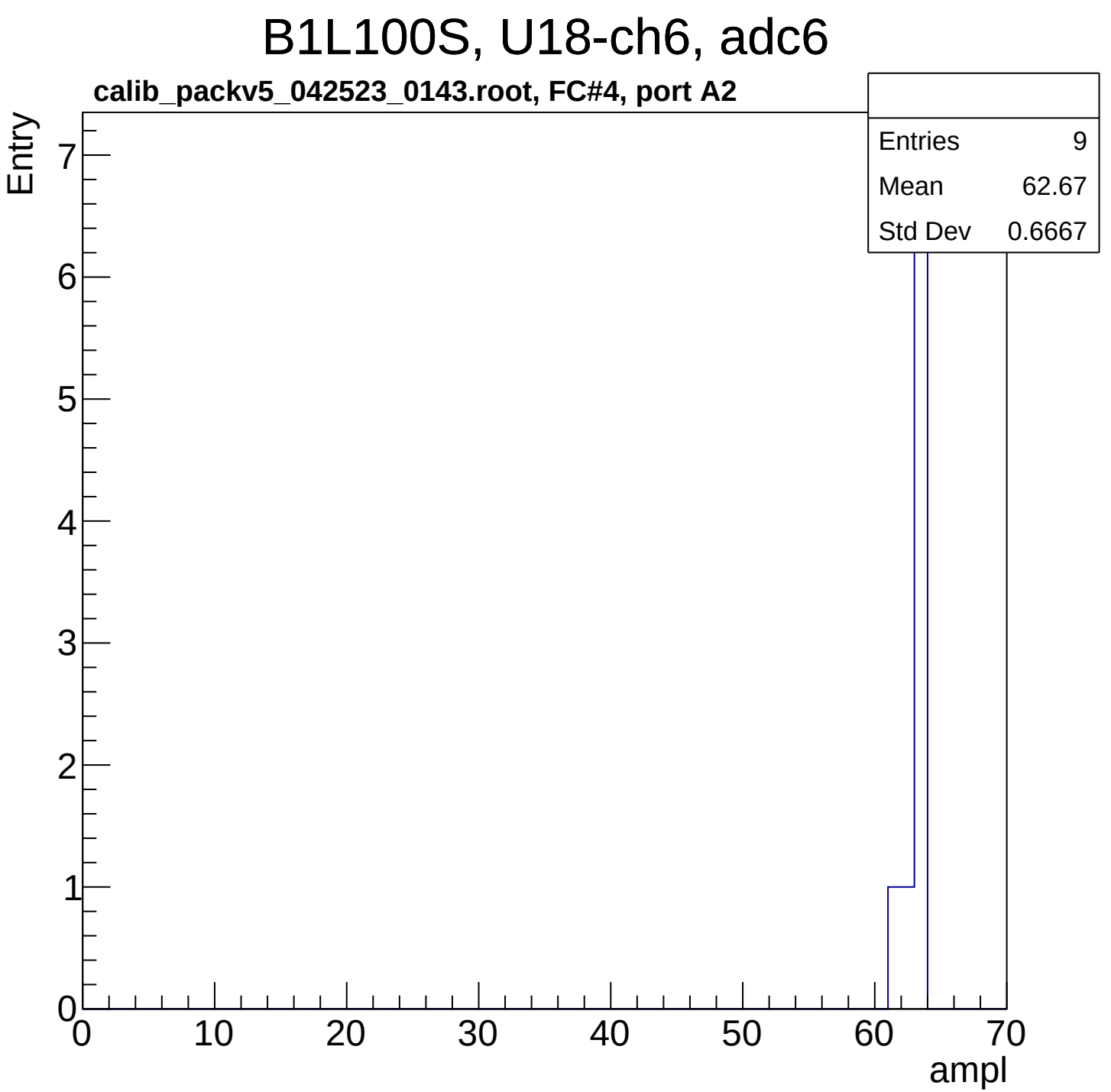

B1L100S, U18-ch6, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 35.98
Std Dev 3.593
Gaus mean : 36.3013
Gaus Width: 3.9724
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

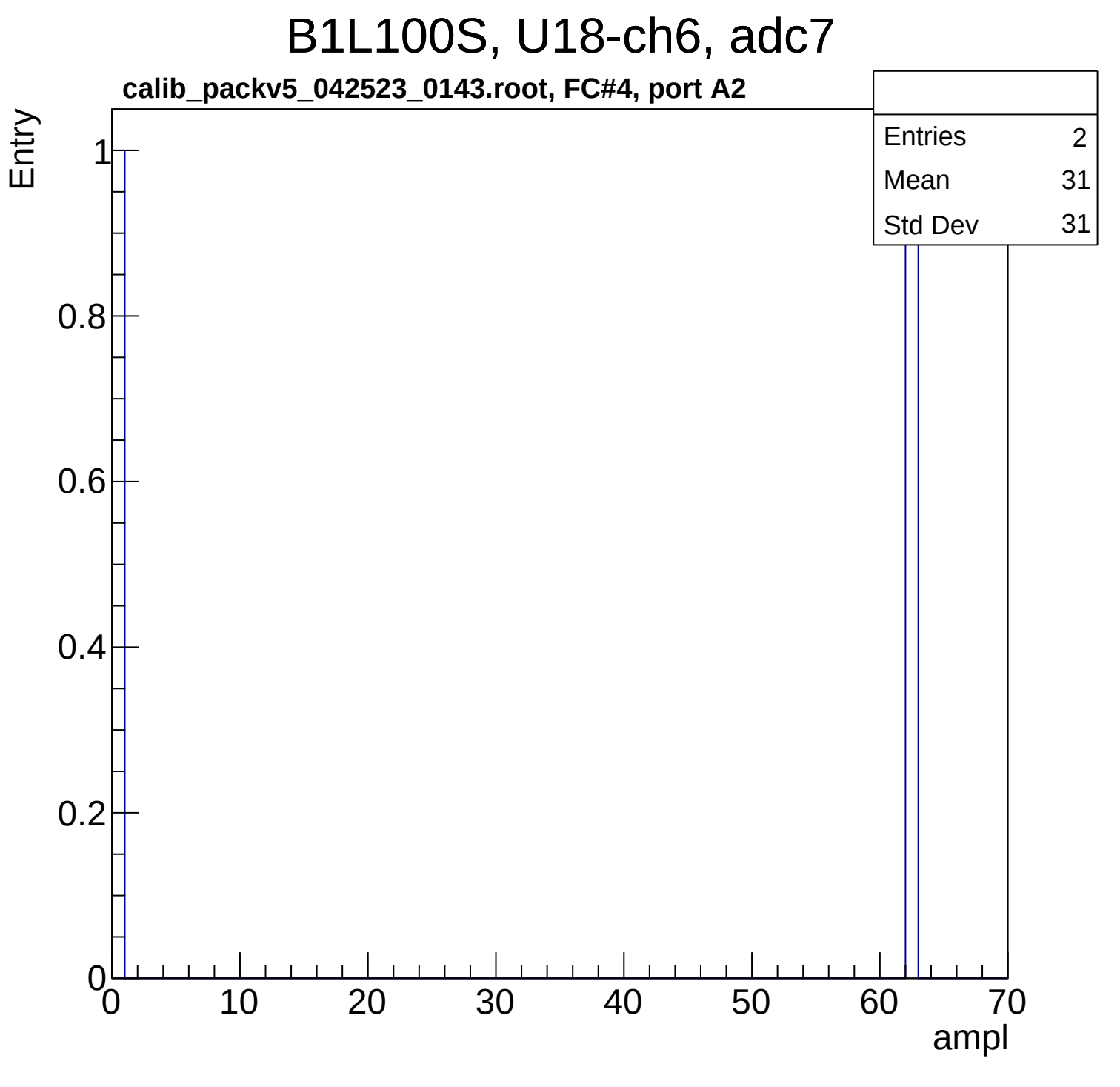

B1L100S, U18-ch6, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 42.14
Std Dev 3.213
Gaus mean : 43.4616
Gaus Width: 2.8316
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

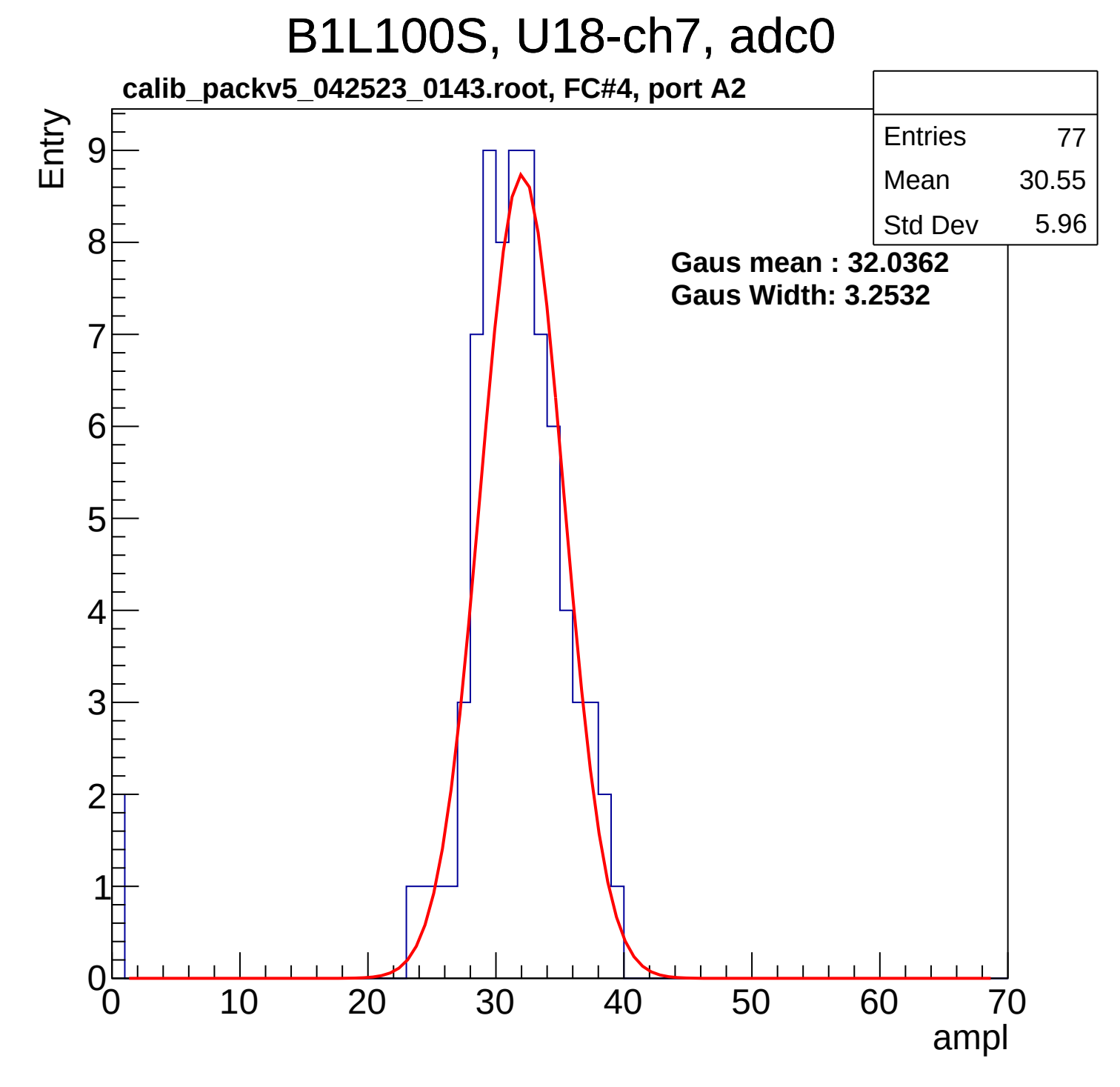

B1L100S, U18-ch6, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 48.7
Std Dev 3.424
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

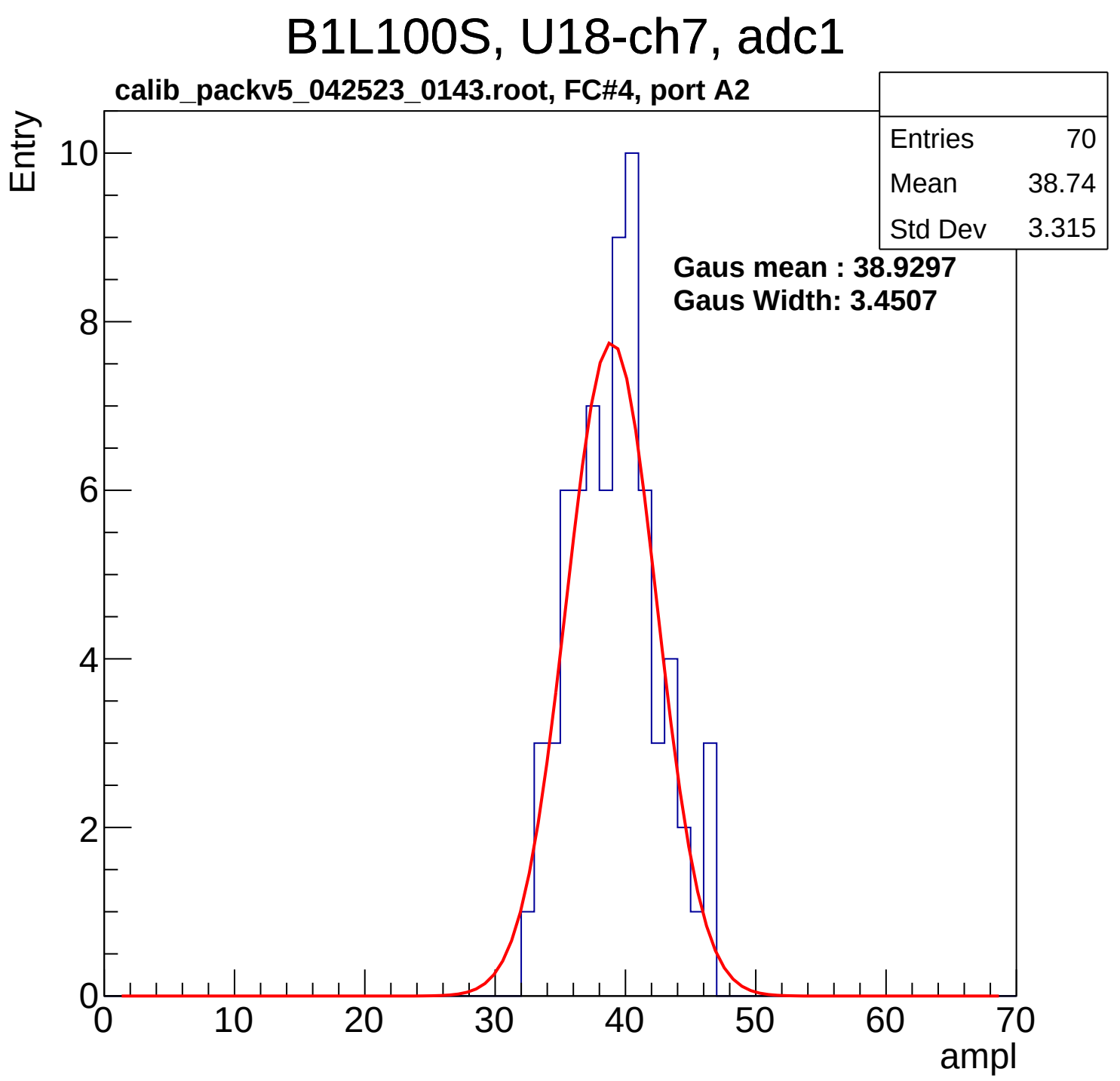

B1L100S, U18-ch6, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 54.21
Std Dev 3.276
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

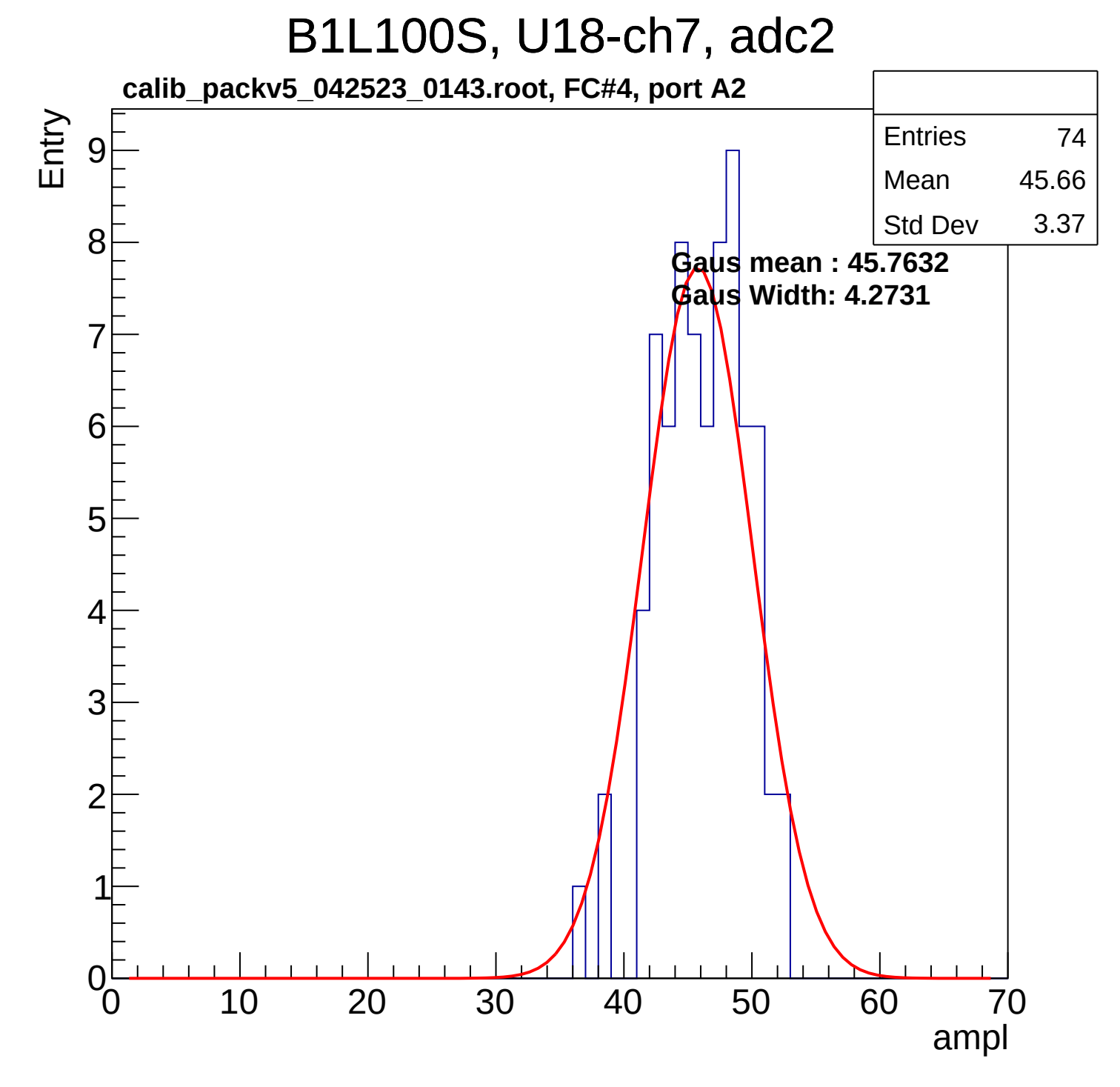

B1L100S, U18-ch6, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 58.15
Std Dev 8.291
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

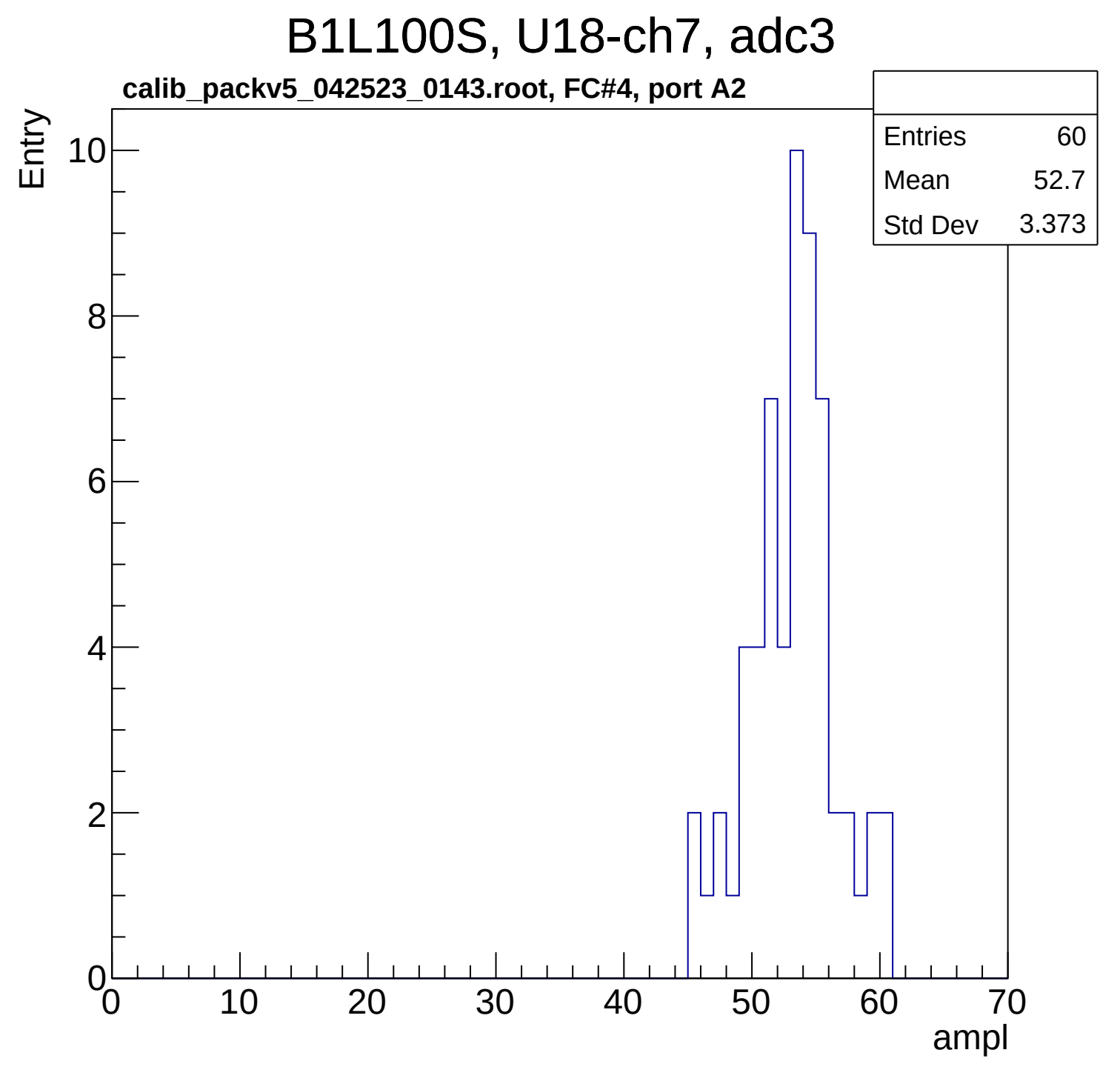

B1L100S, U18-ch6, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 62.67
Std Dev 0.6667
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

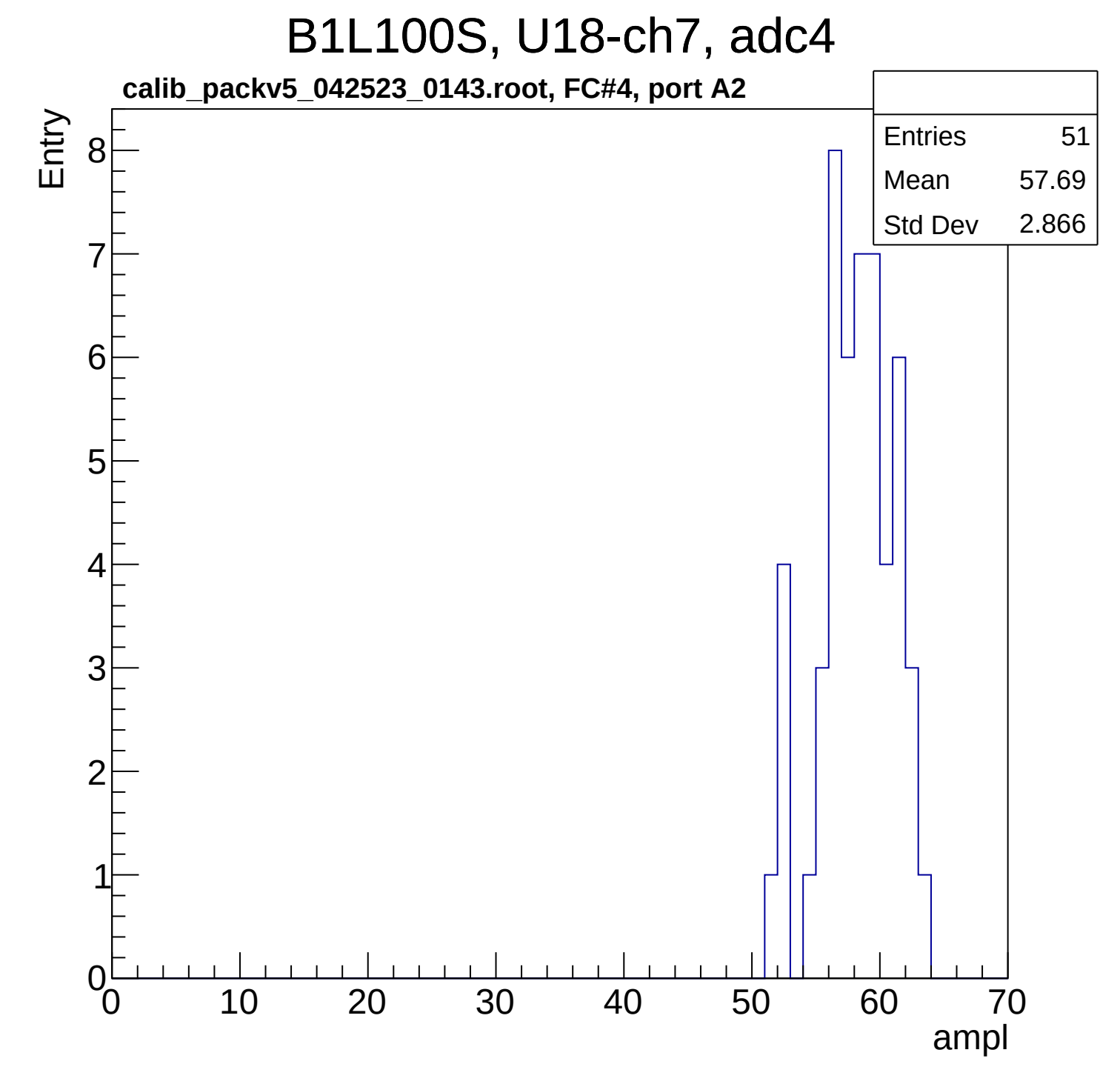

B1L100S, U18-ch6, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 31
Std Dev 31
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

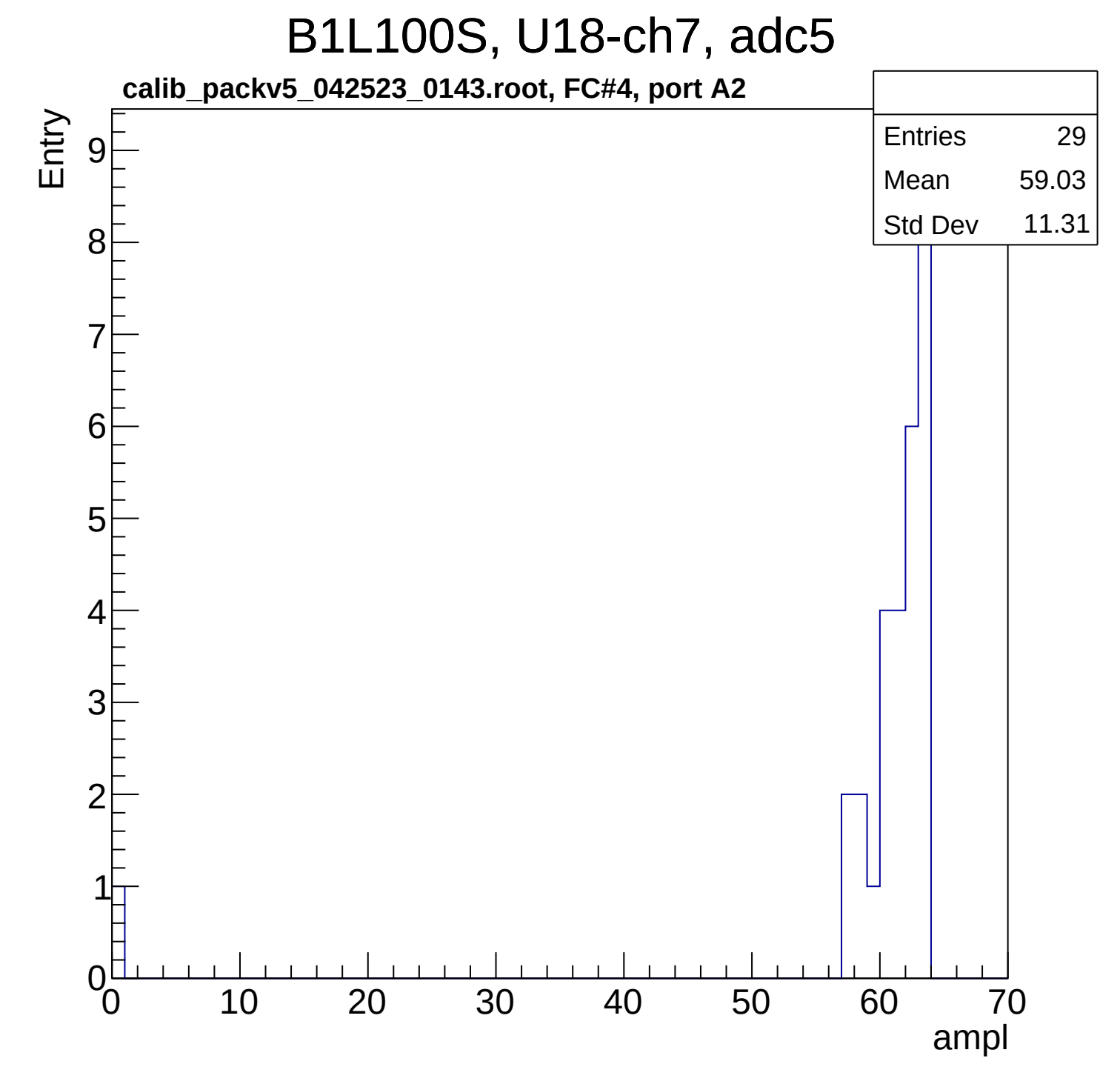

B1L100S, U18-ch7, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 30.55
Std Dev 5.96
Gaus mean : 32.0362
Gaus Width: 3.2532
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

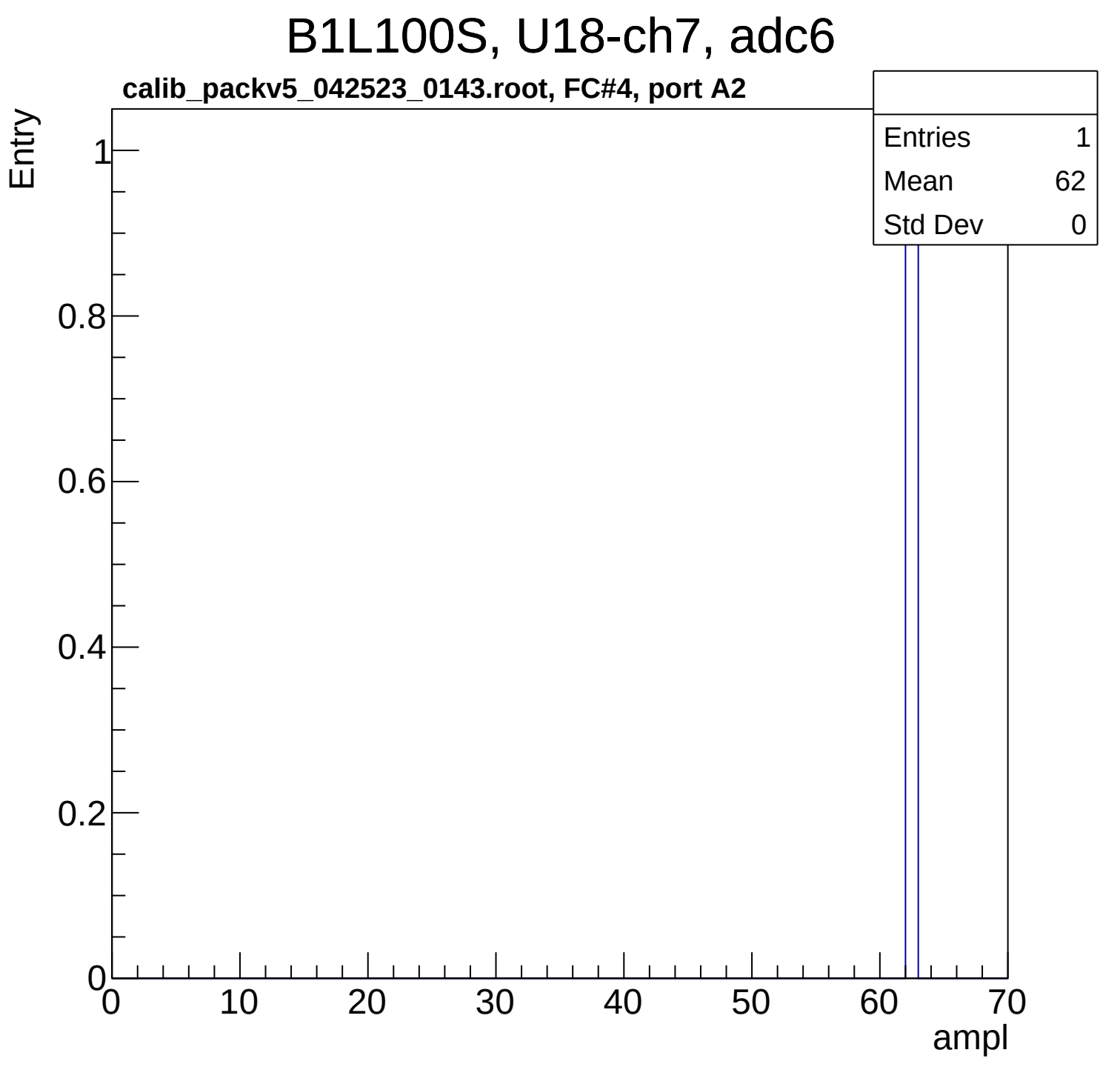

B1L100S, U18-ch7, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 38.74
Std Dev 3.315
Gaus mean : 38.9297
Gaus Width: 3.4507
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

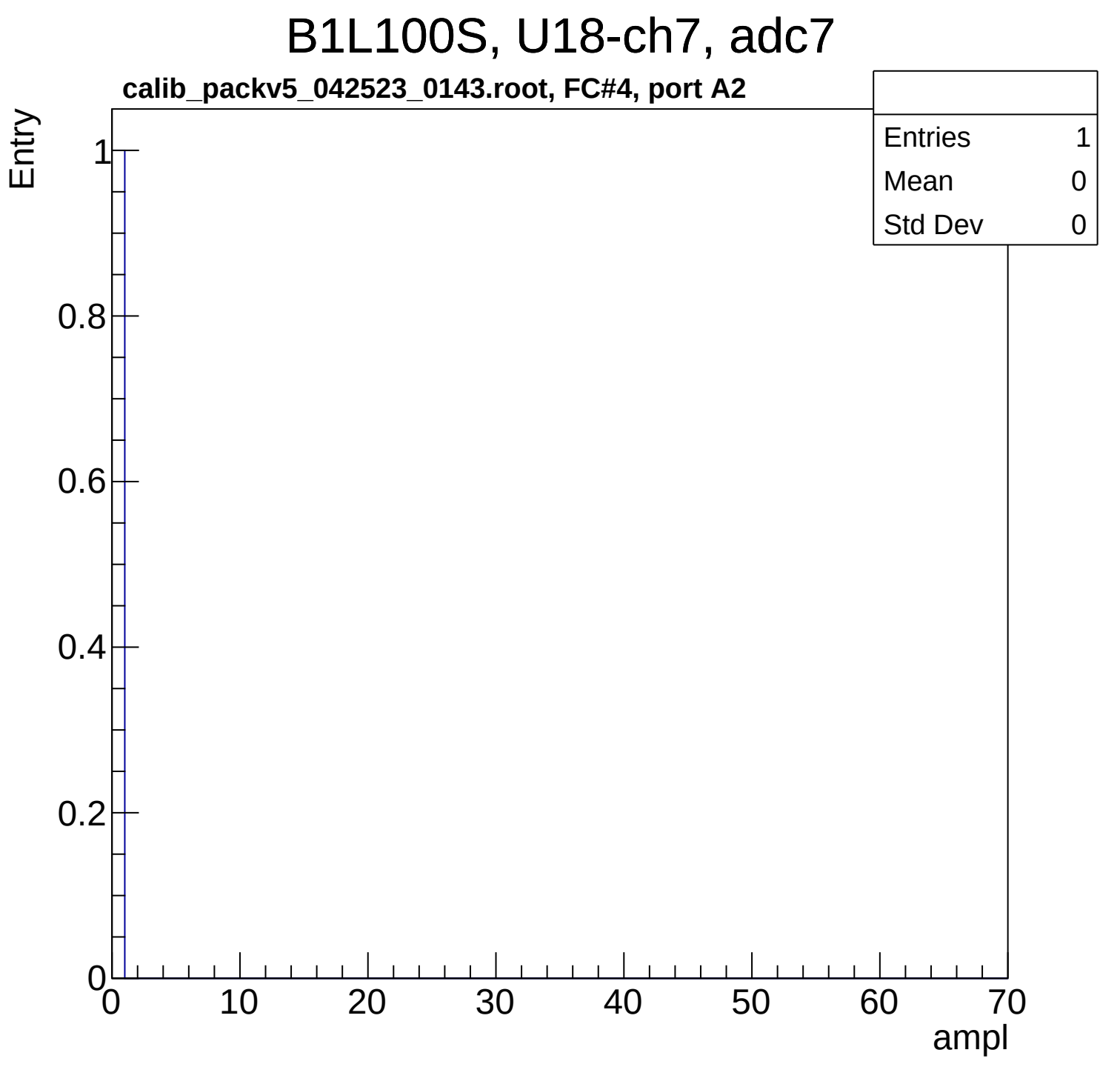

B1L100S, U18-ch7, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 45.66
Std Dev 3.37
Gaus mean : 45.7632
Gaus Width: 4.2731
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

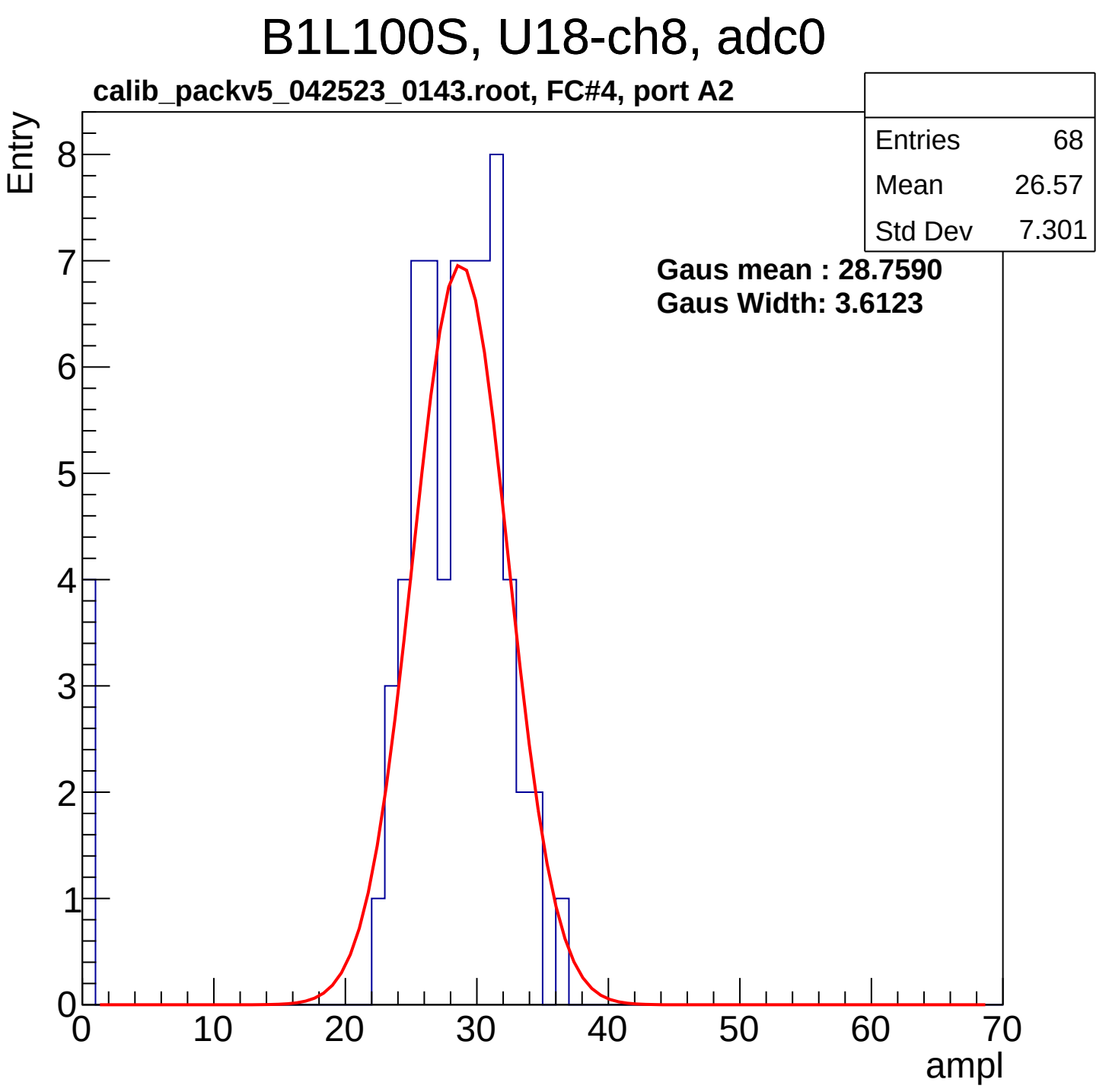

B1L100S, U18-ch7, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 52.7
Std Dev 3.373
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

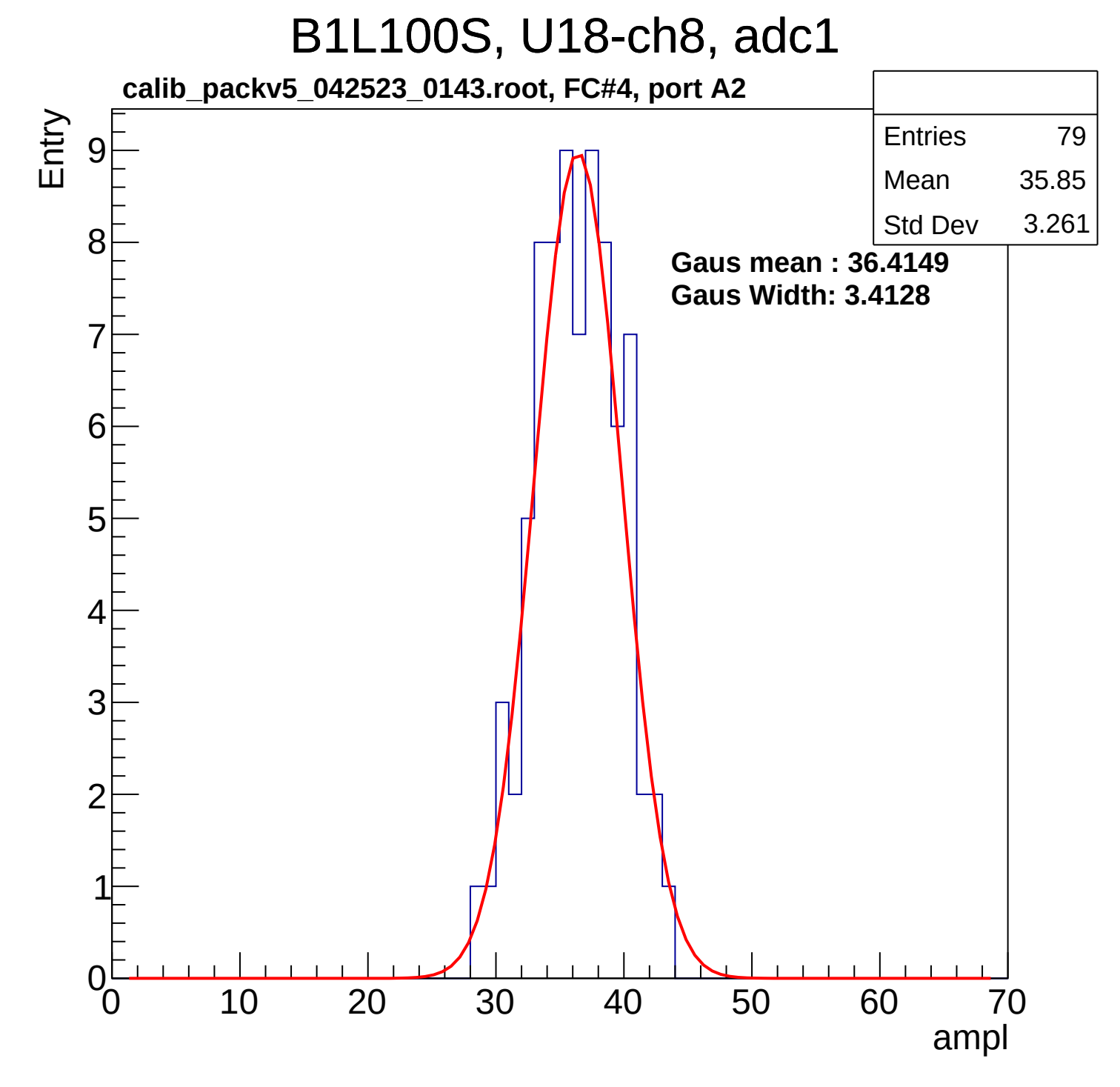

B1L100S, U18-ch7, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 57.69
Std Dev 2.866
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

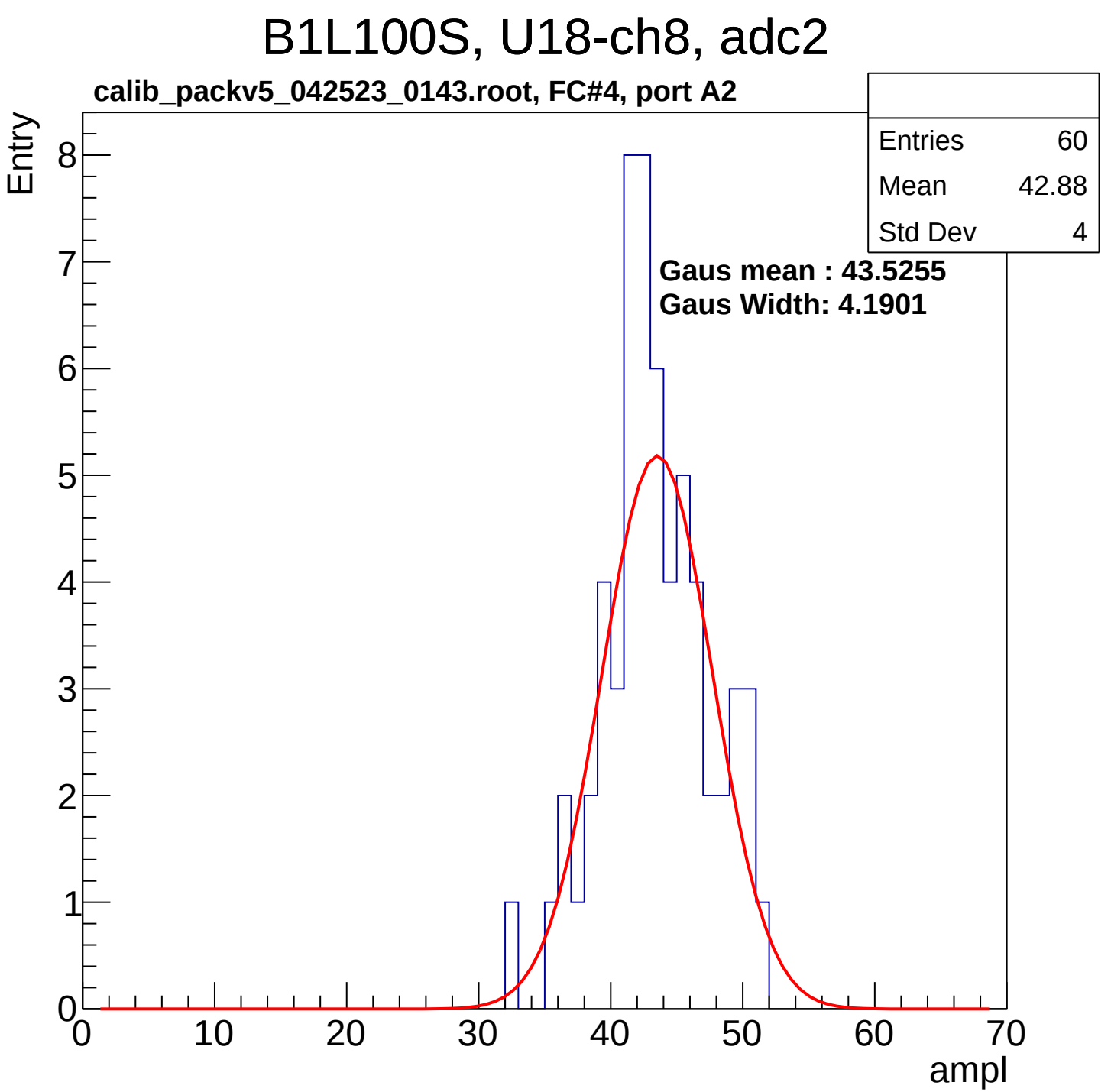

B1L100S, U18-ch7, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 29
Mean 59.03
Std Dev 11.31
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

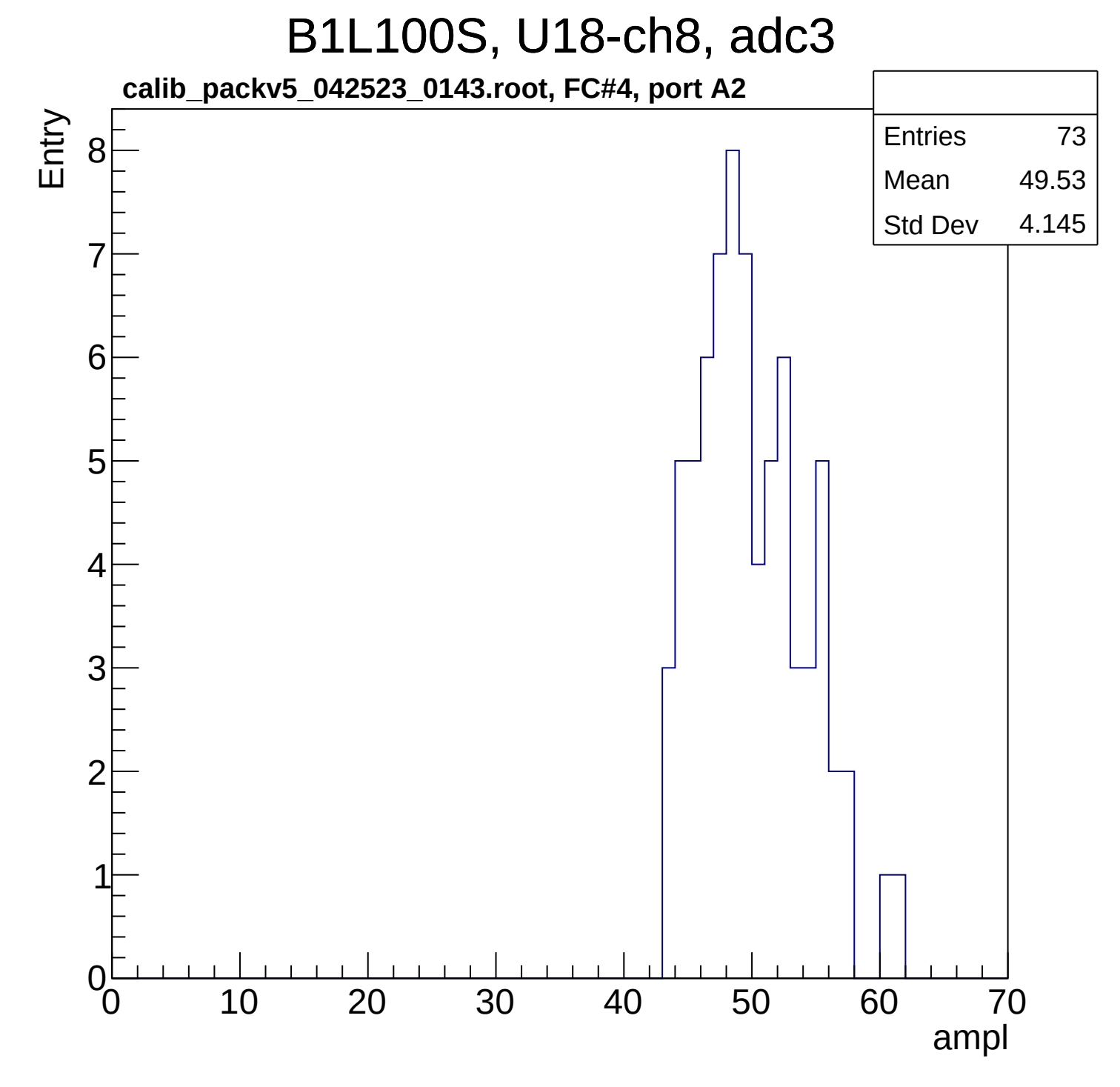

B1L100S, U18-ch7, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

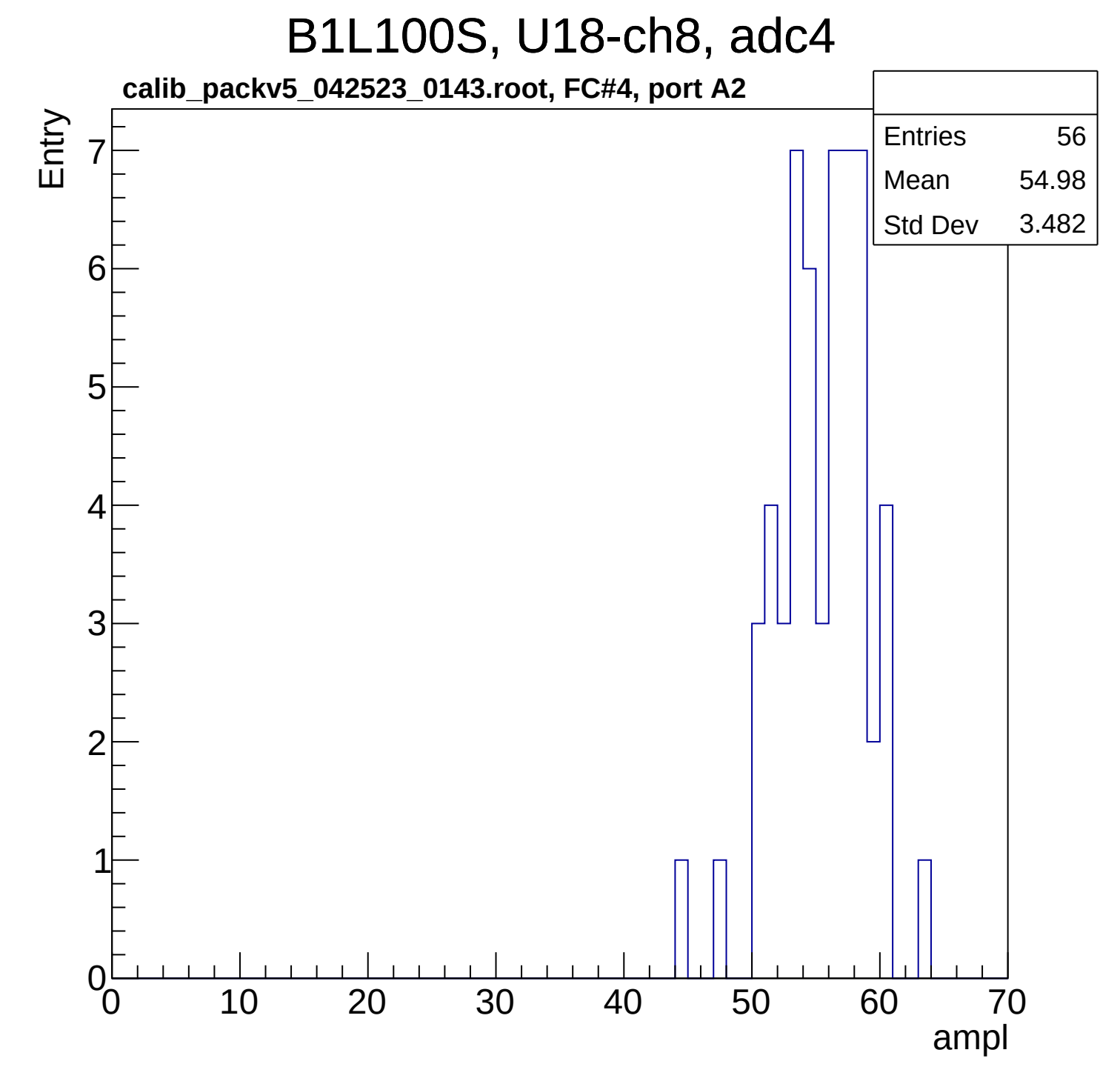

B1L100S, U18-ch7, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

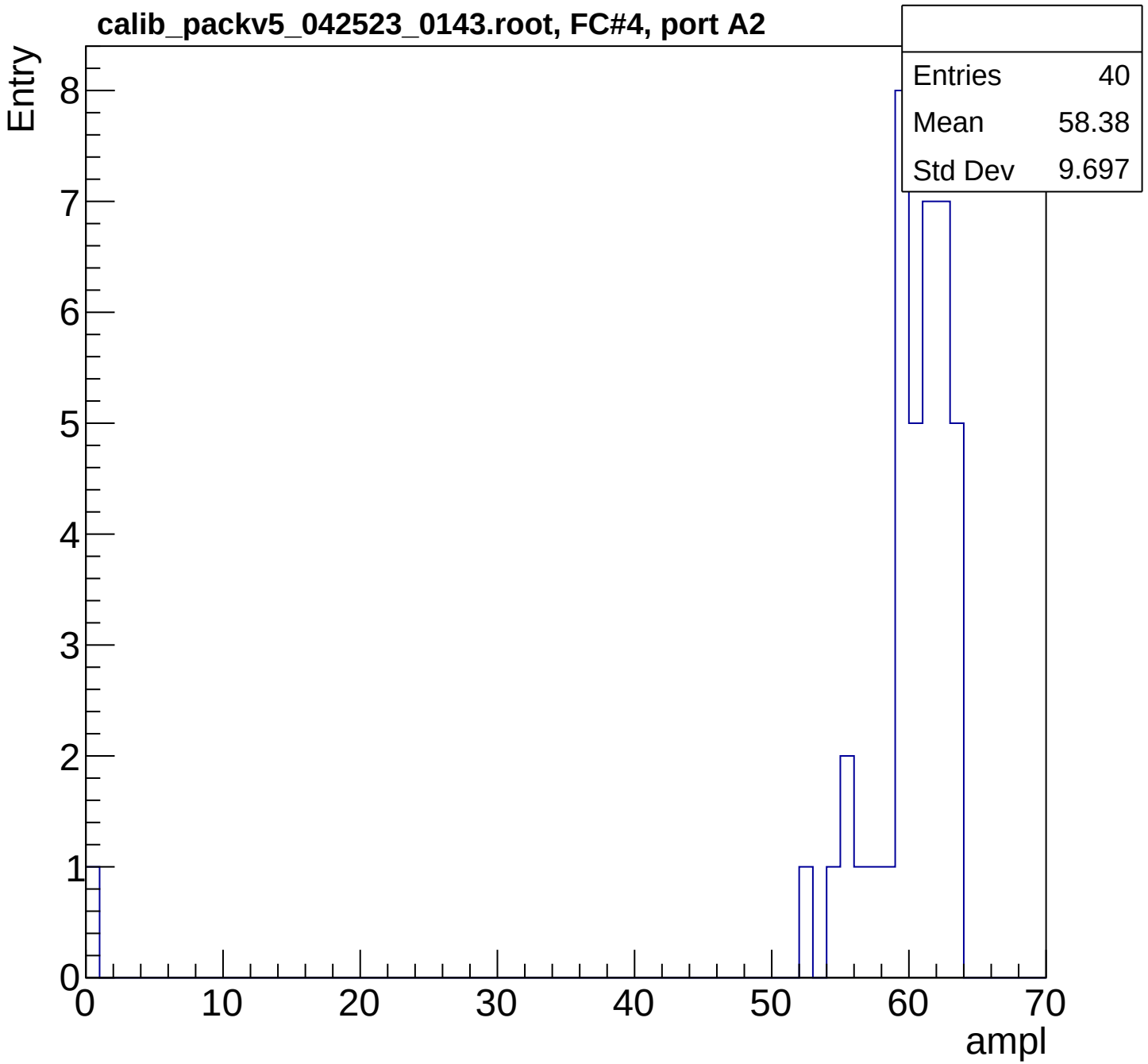

B1L100S, U18-ch8, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 26.57
Std Dev 7.301
Gaus mean : 28.7590
Gaus Width: 3.6123
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

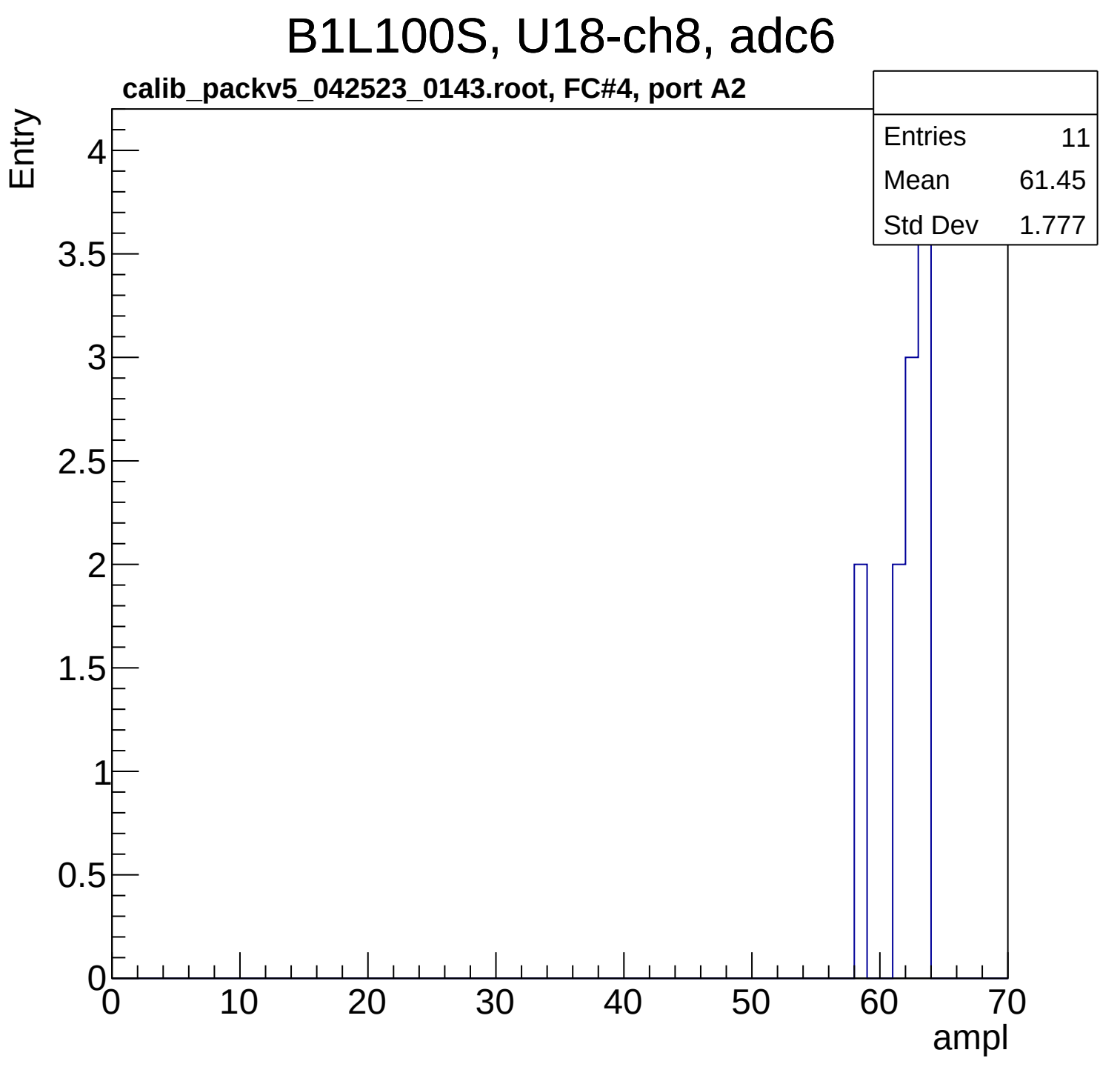

B1L100S, U18-ch8, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 35.85
Std Dev 3.261
Gaus mean : 36.4149
Gaus Width: 3.4128
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

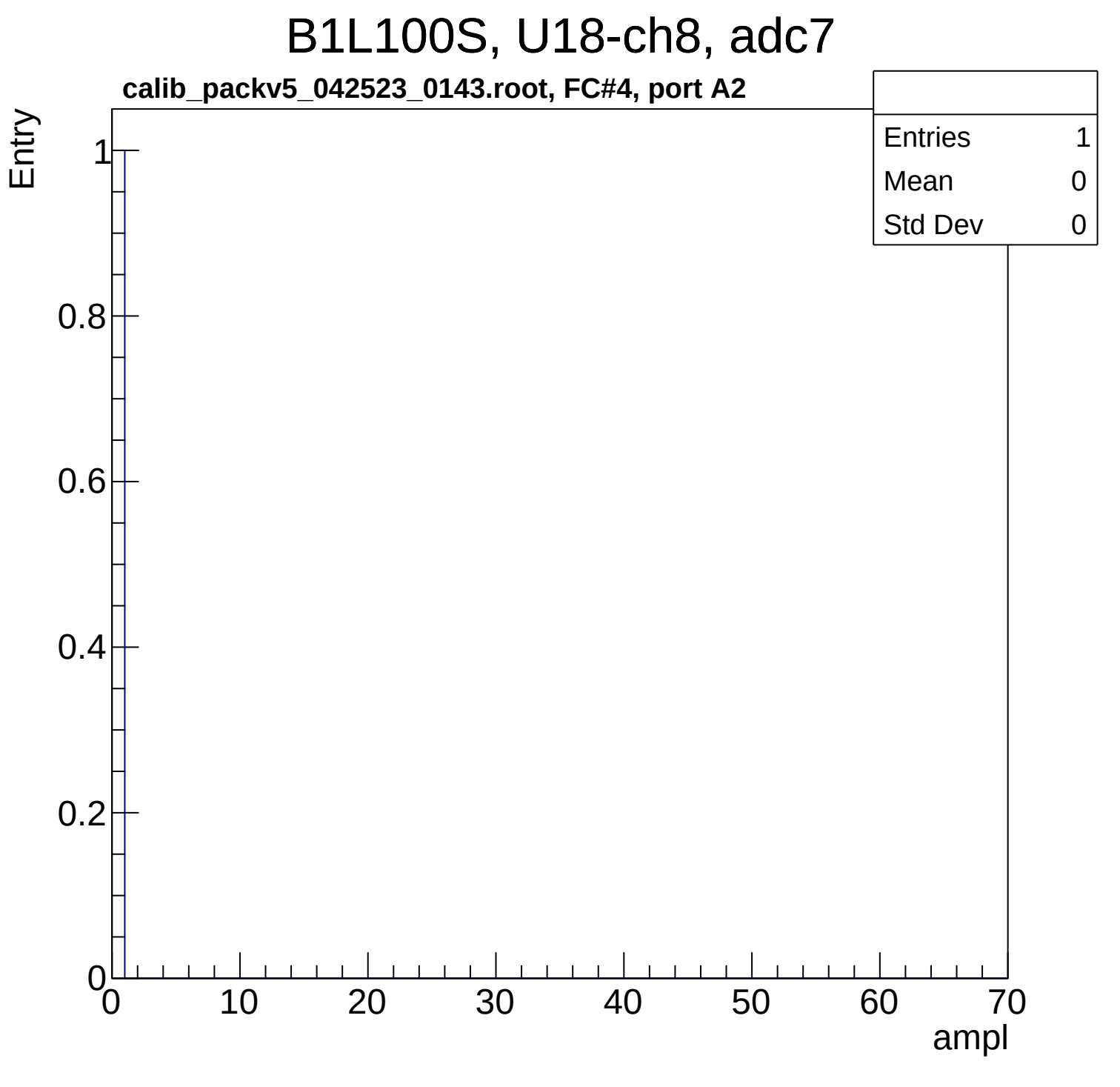

B1L100S, U18-ch8, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 42.88
Std Dev 4
Gaus mean : 43.5255
Gaus Width: 4.1901
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

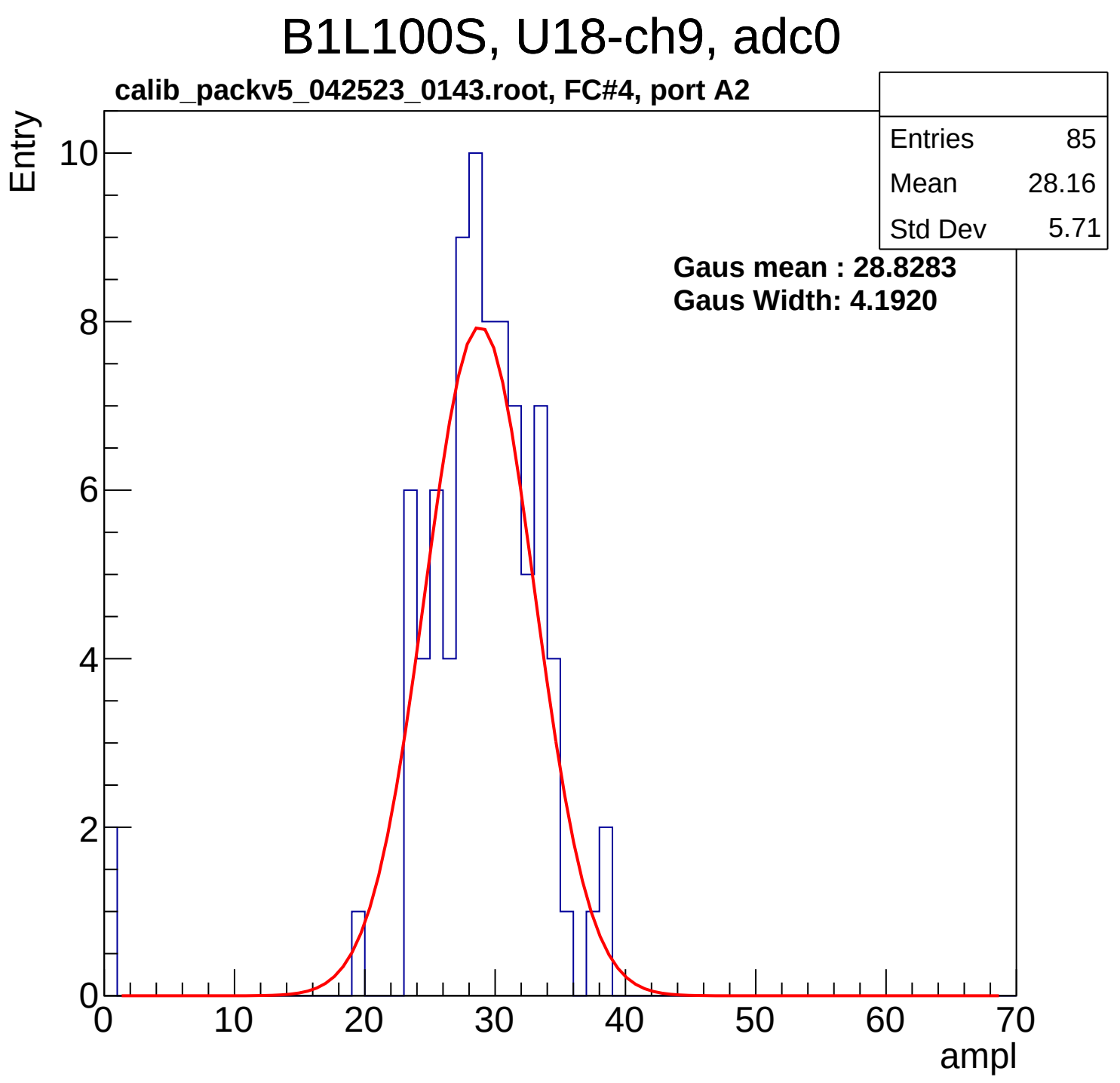

B1L100S, U18-ch8, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 49.53
Std Dev 4.145
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

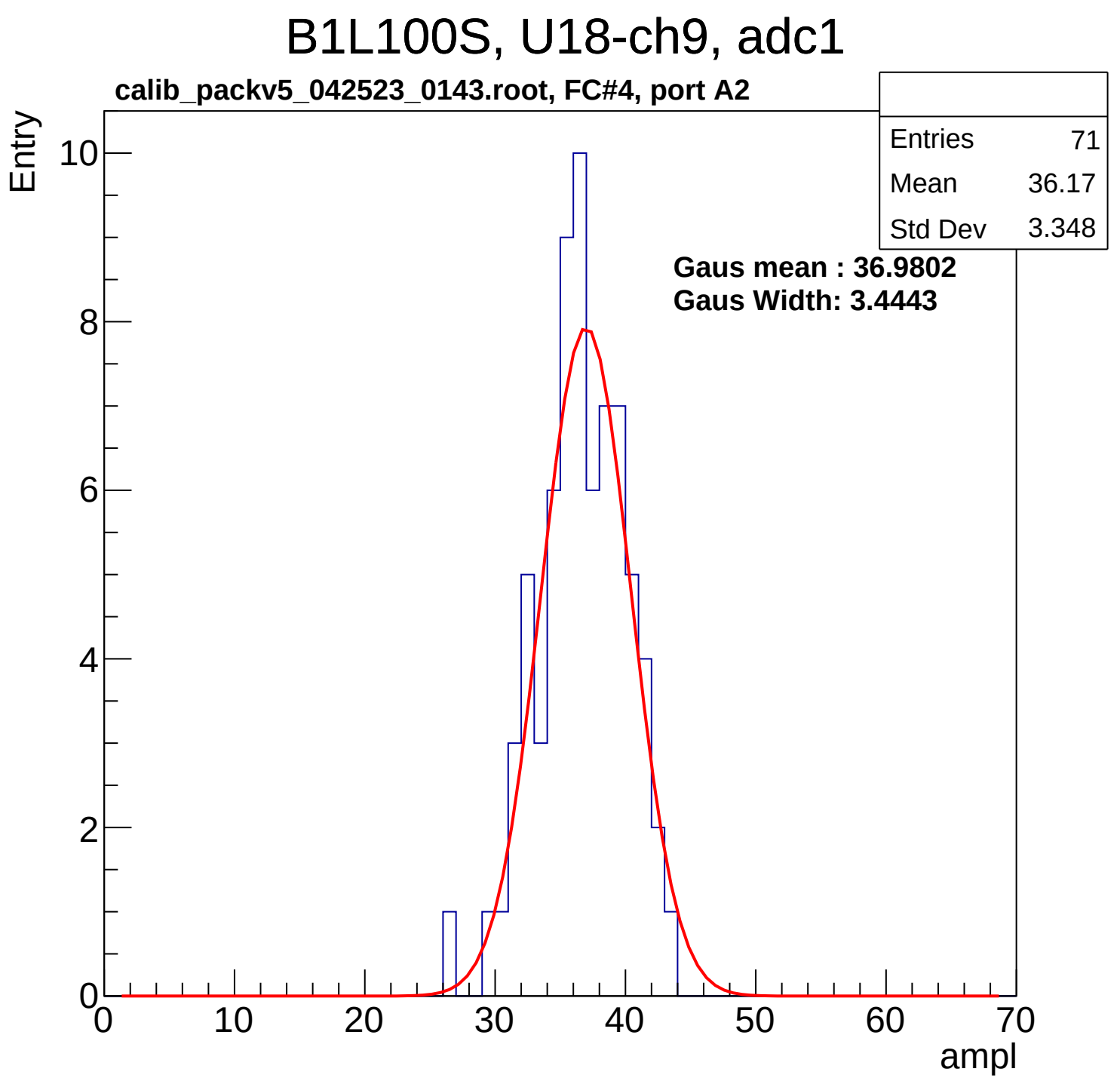

B1L100S, U18-ch8, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 54.98
Std Dev 3.482
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

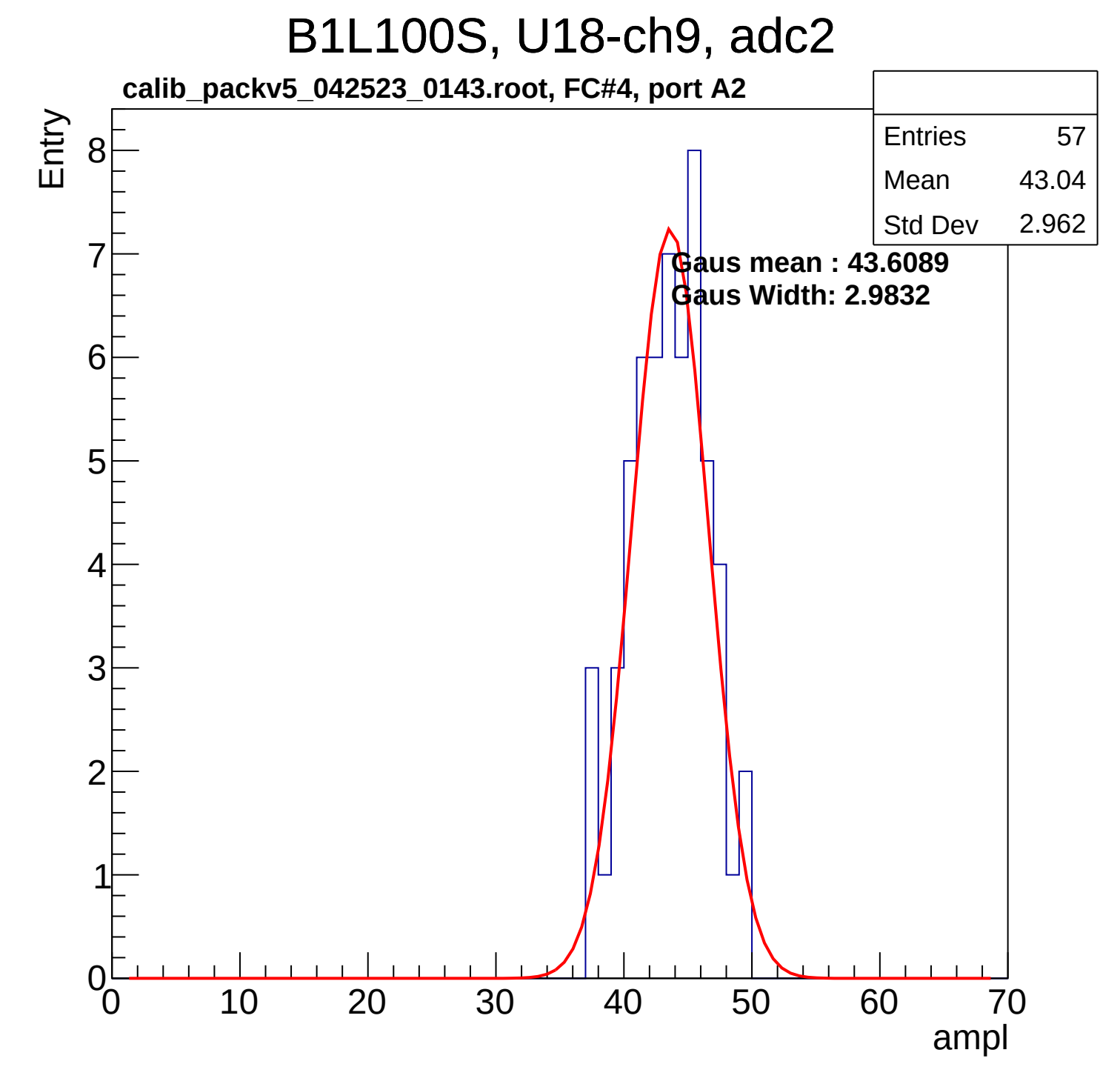

B1L100S, U18-ch8, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 40
Mean 58.38
Std Dev 9.697
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

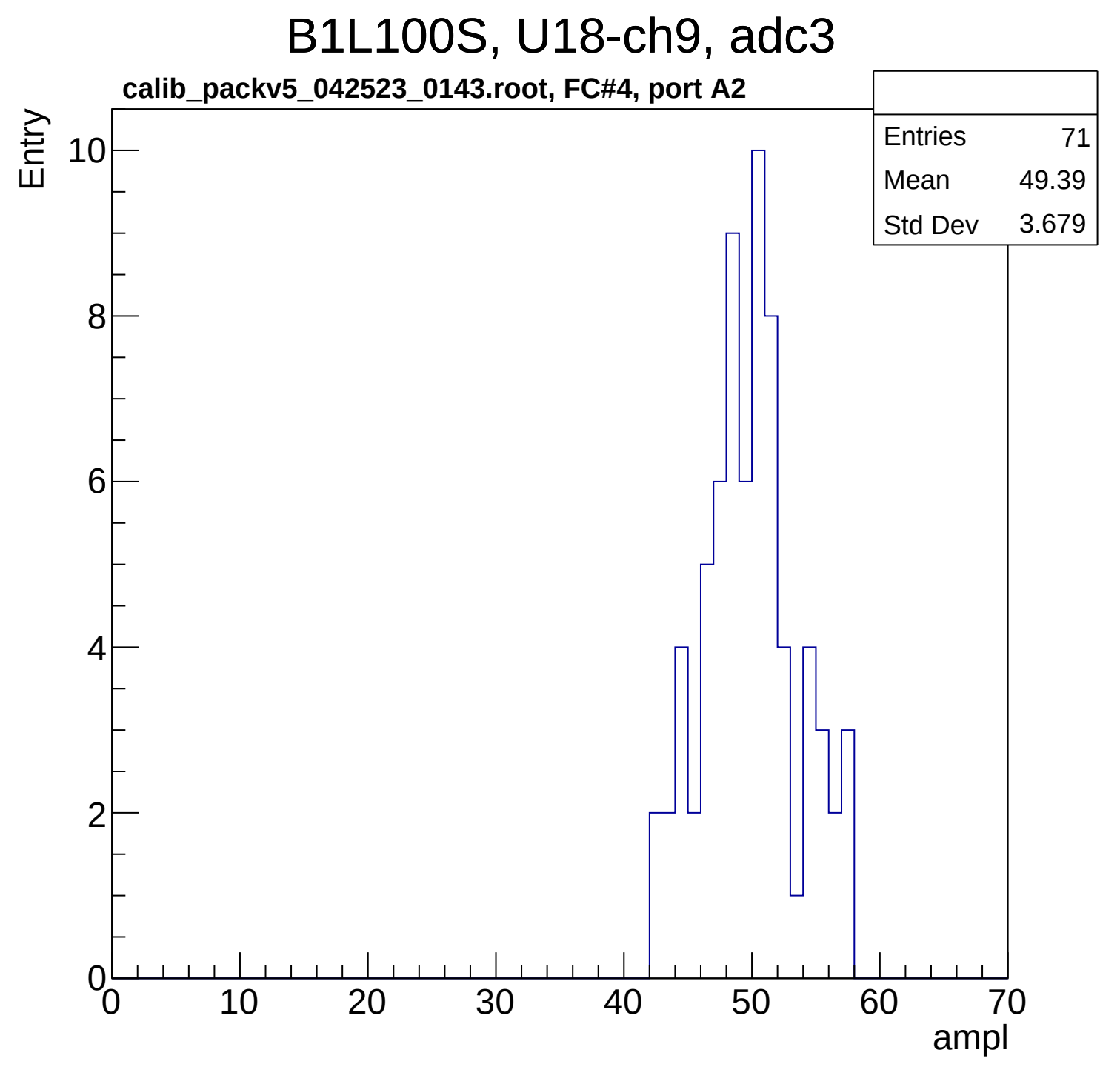

B1L100S, U18-ch8, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 61.45
Std Dev 1.777
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

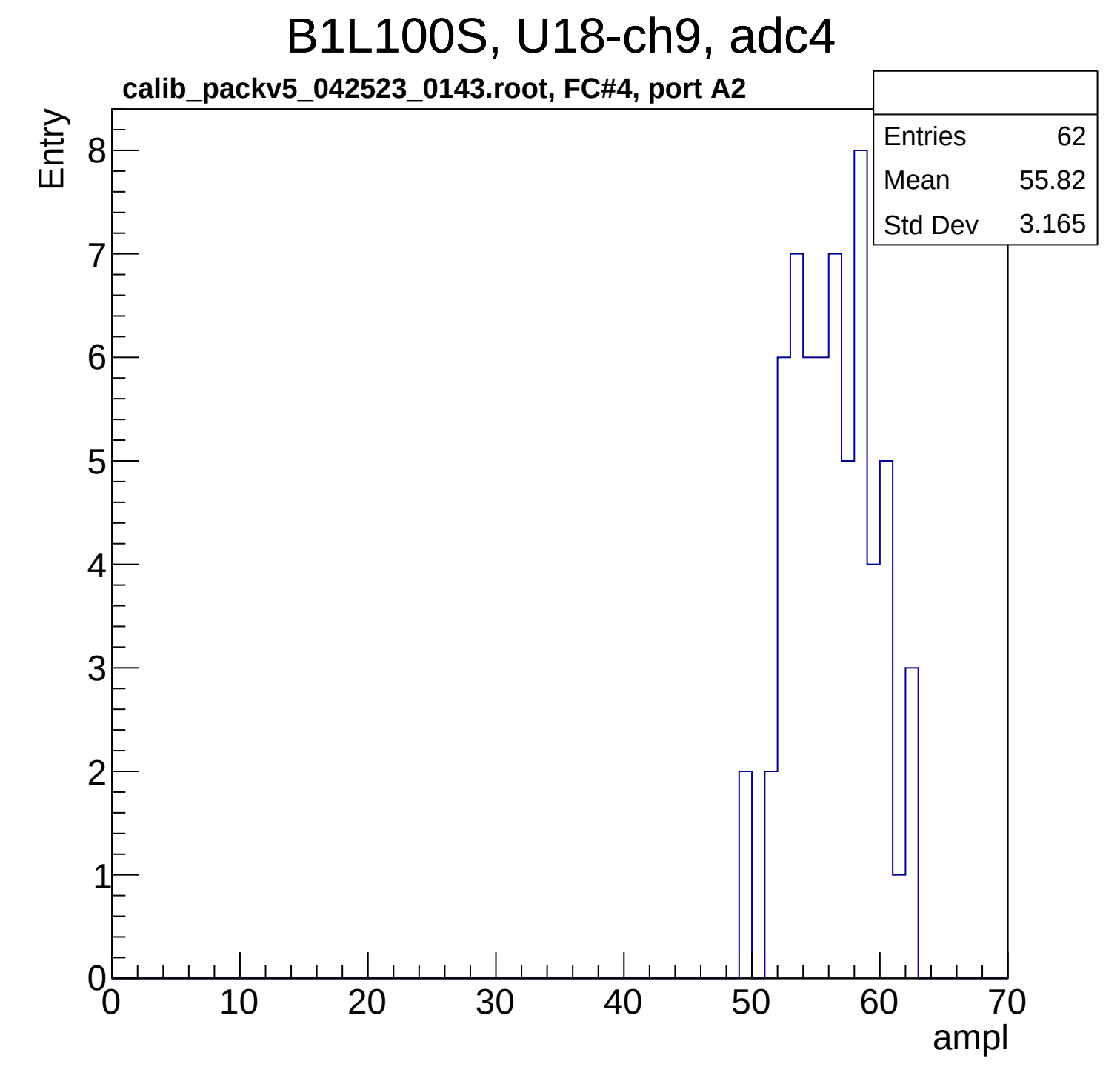

B1L100S, U18-ch8, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

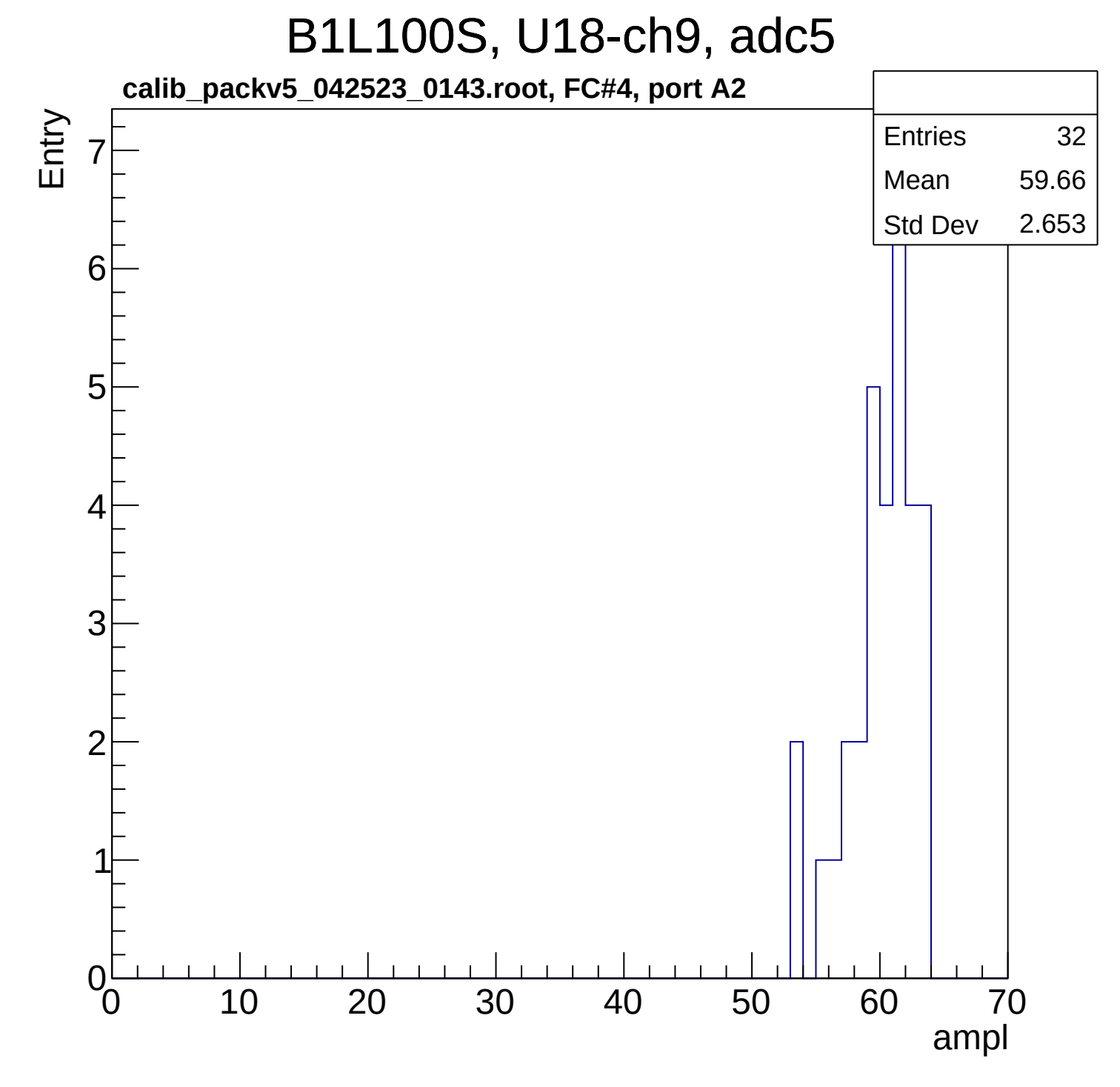

B1L100S, U18-ch9, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 85
Mean 28.16
Std Dev 5.71
Gaus mean : 28.8283
Gaus Width: 4.1920
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

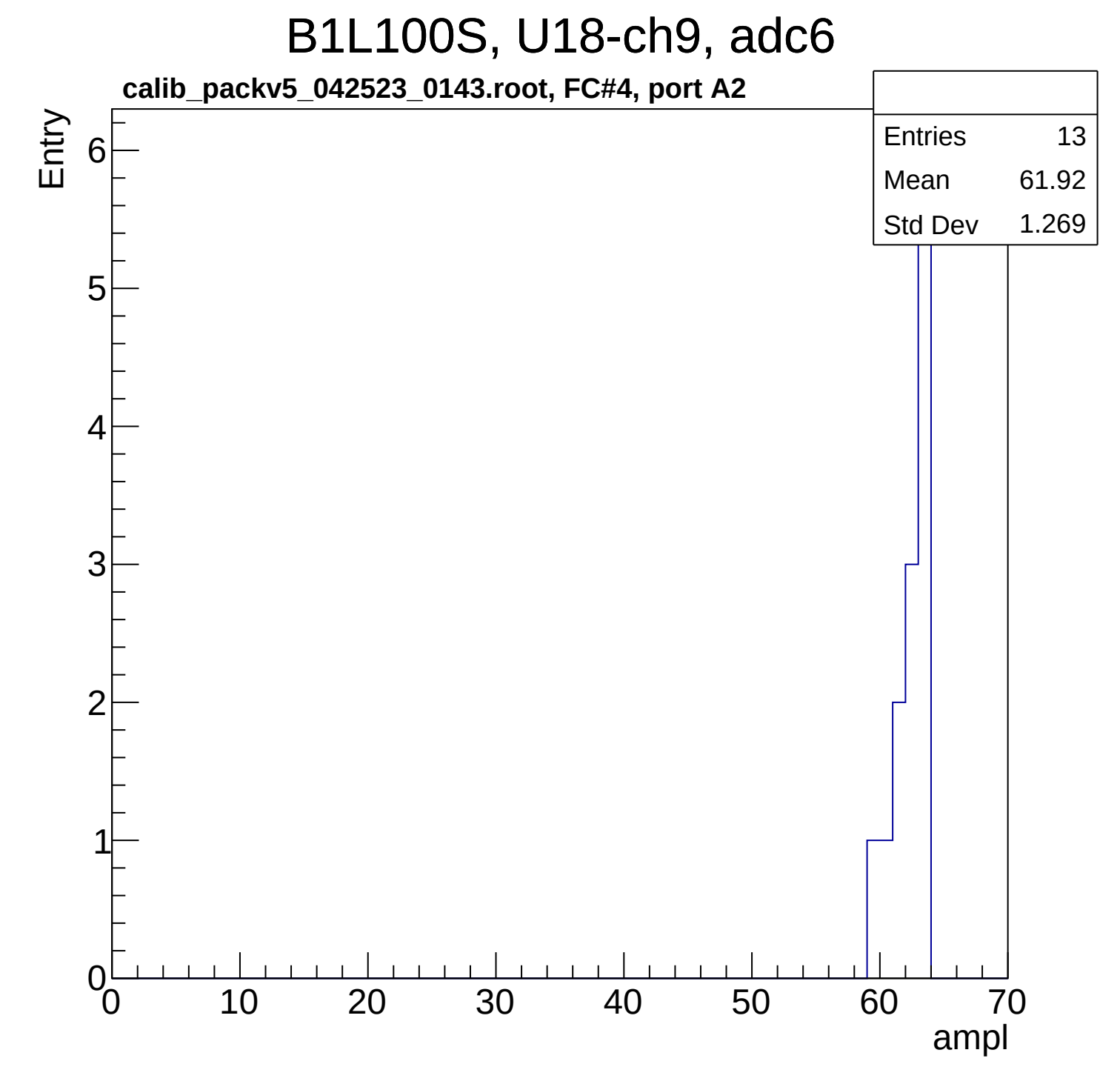

B1L100S, U18-ch9, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 36.17
Std Dev 3.348
Gaus mean : 36.9802
Gaus Width: 3.4443
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

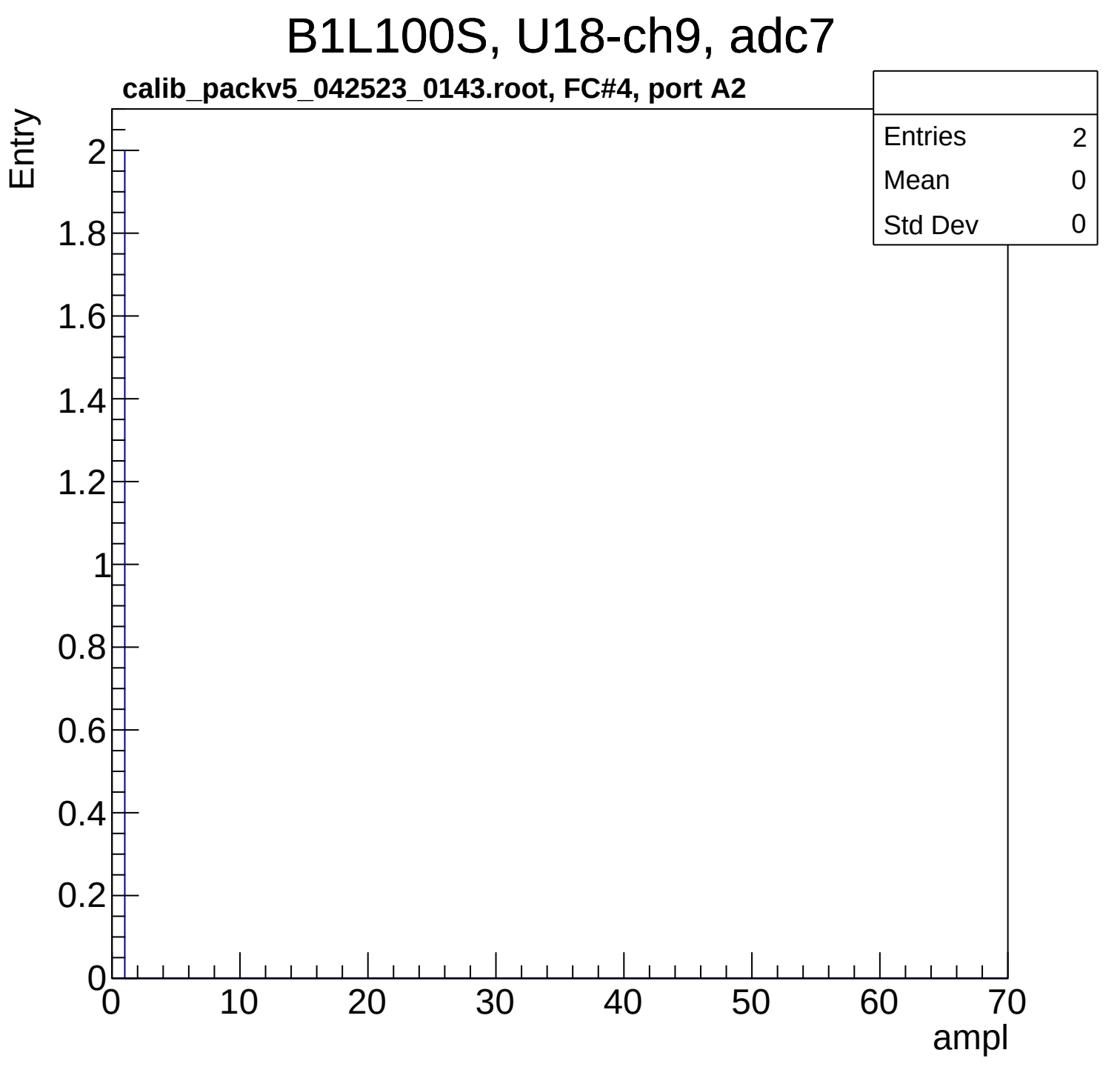

B1L100S, U18-ch9, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 43.04
Std Dev 2.962
Gaus mean : 43.6089
Gaus Width: 2.9832
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

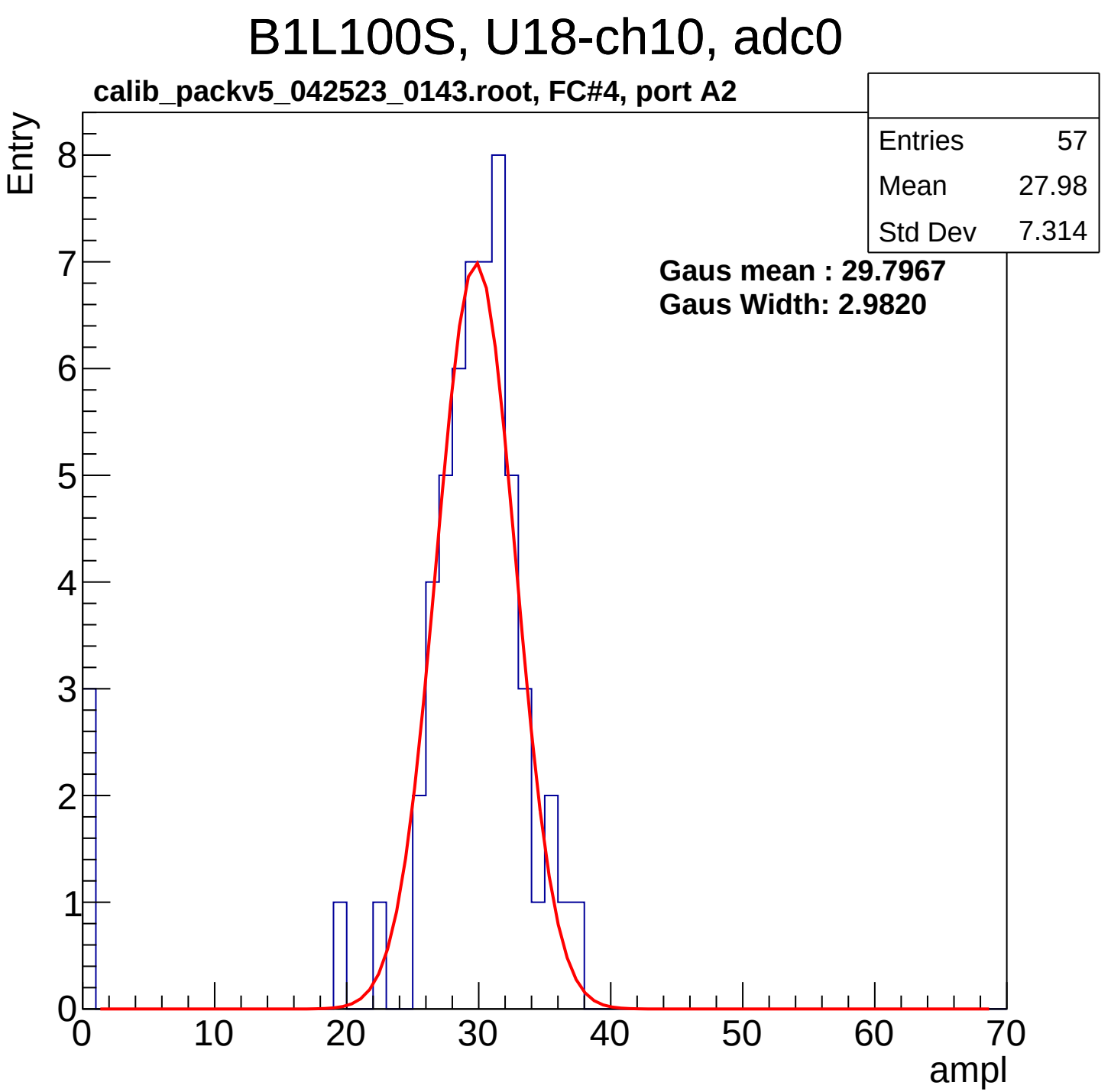

B1L100S, U18-ch9, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 49.39
Std Dev 3.679
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

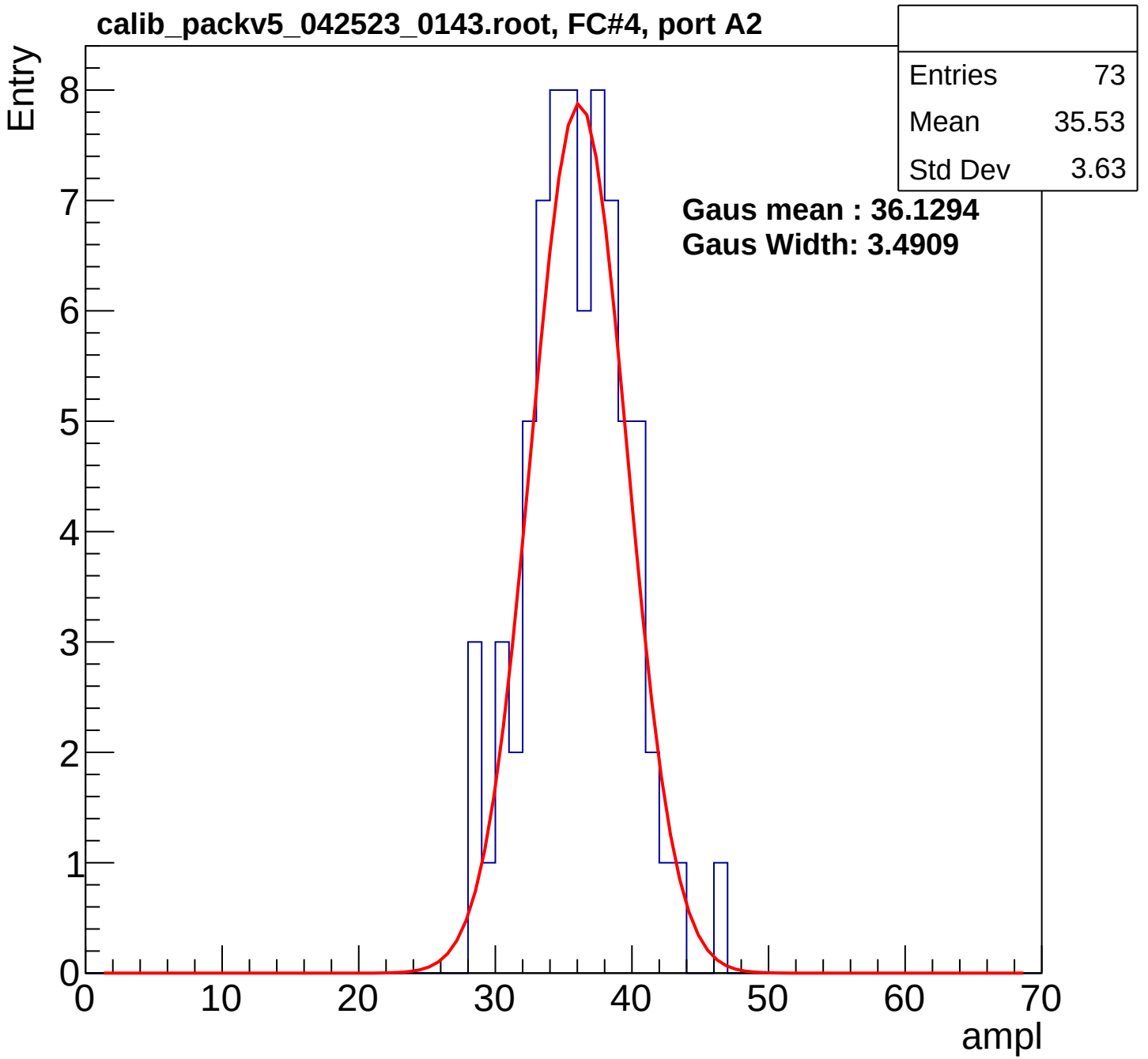

B1L100S, U18-ch9, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 55.82
Std Dev 3.165
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

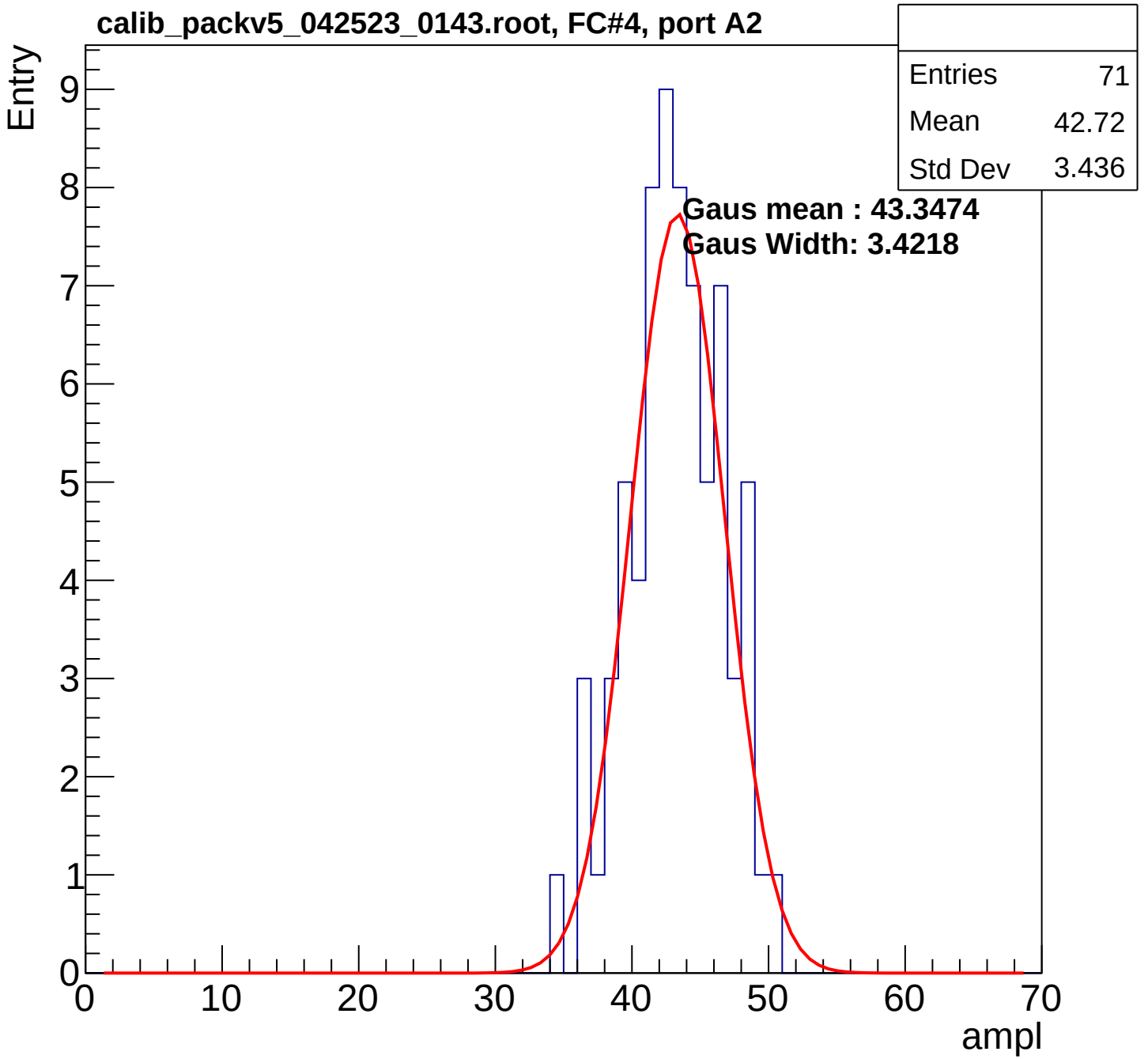

B1L100S, U18-ch9, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 32
Mean 59.66
Std Dev 2.653
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

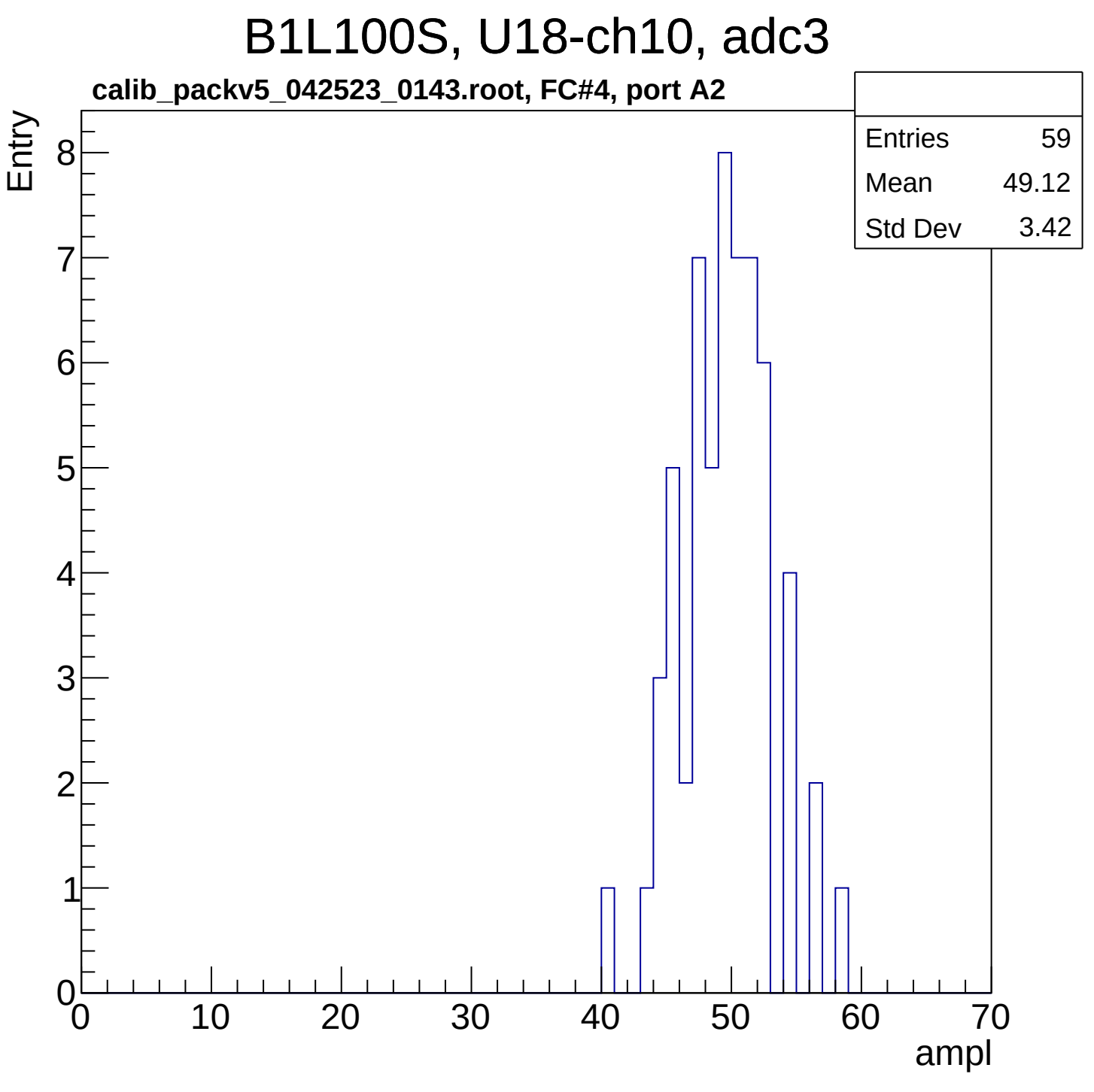

B1L100S, U18-ch9, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 13
Mean 61.92
Std Dev 1.269
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

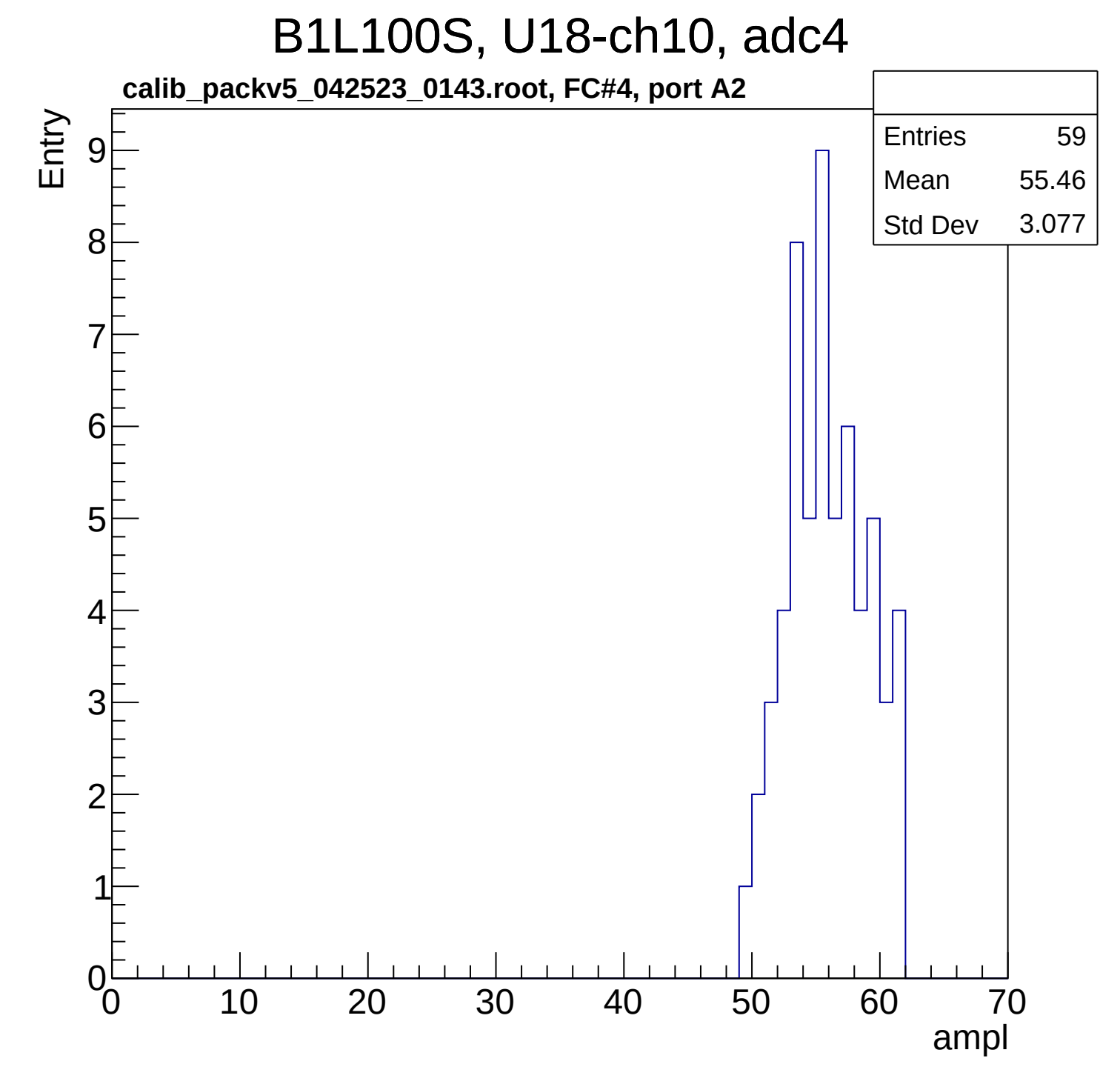

B1L100S, U18-ch9, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

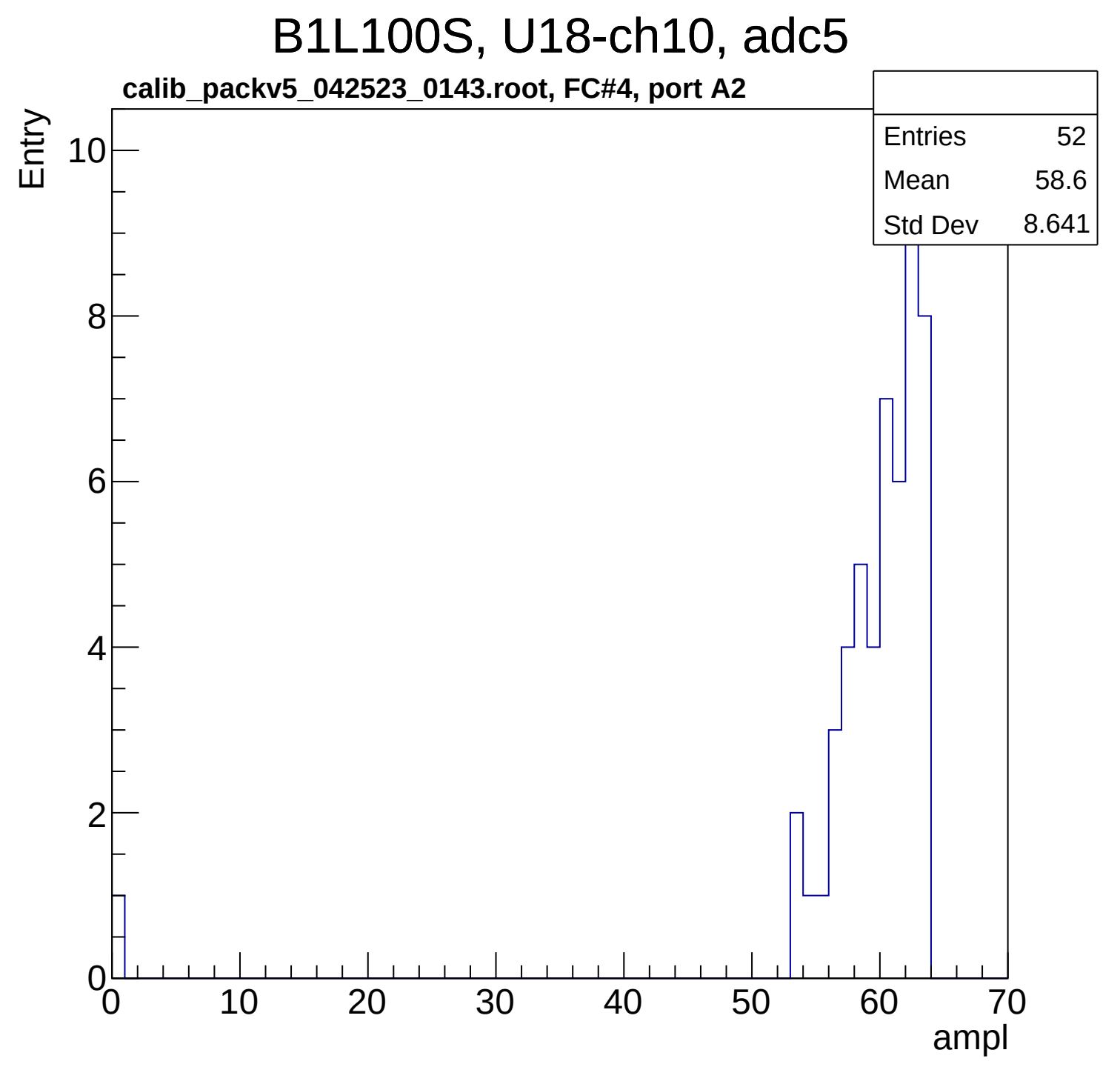

B1L100S, U18-ch10, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 27.98
Std Dev 7.314
Gaus mean : 29.7967
Gaus Width: 2.9820
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

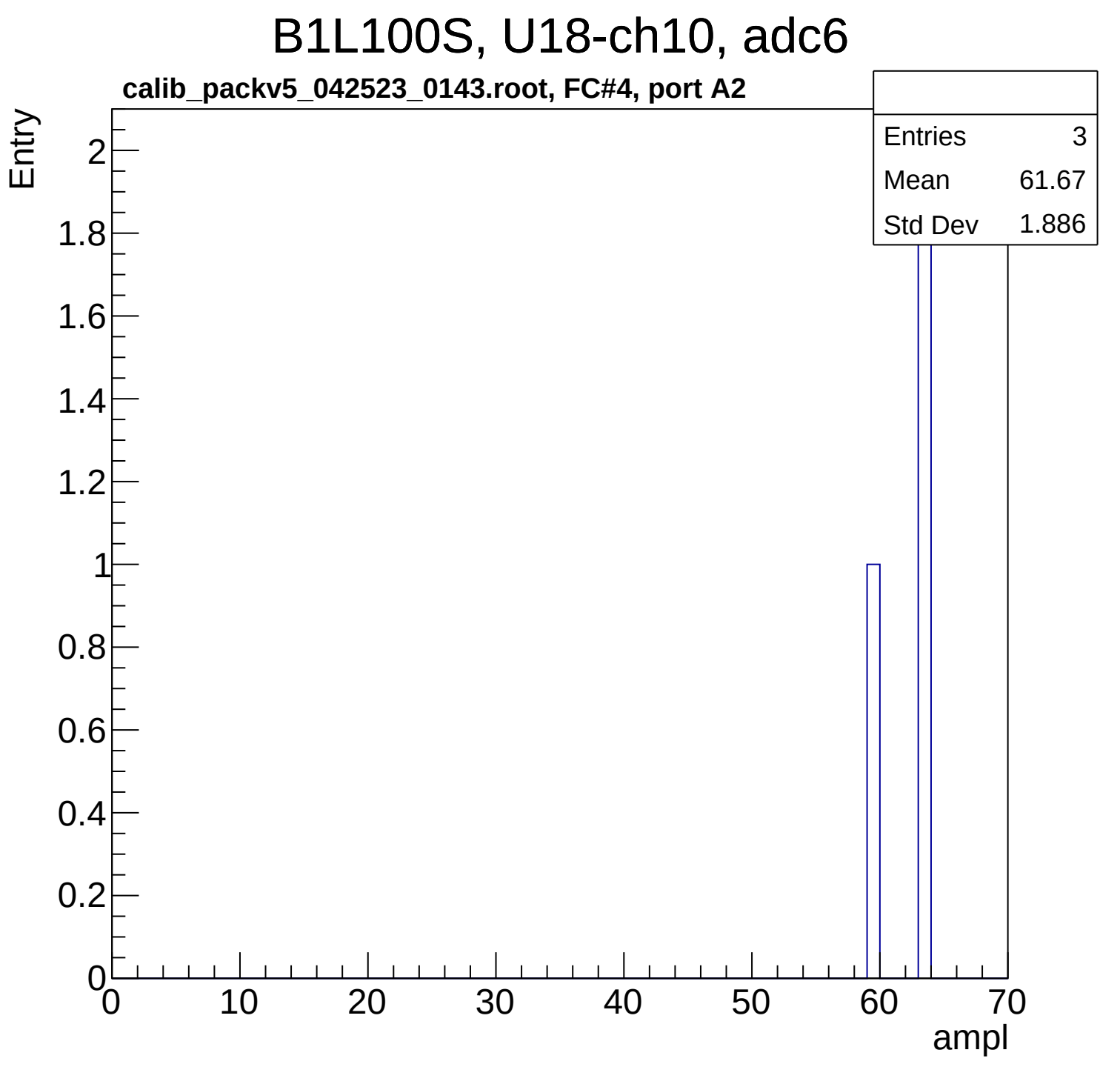

B1L100S, U18-ch10, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 35.53
Std Dev 3.63
Gaus mean : 36.1294
Gaus Width: 3.4909
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

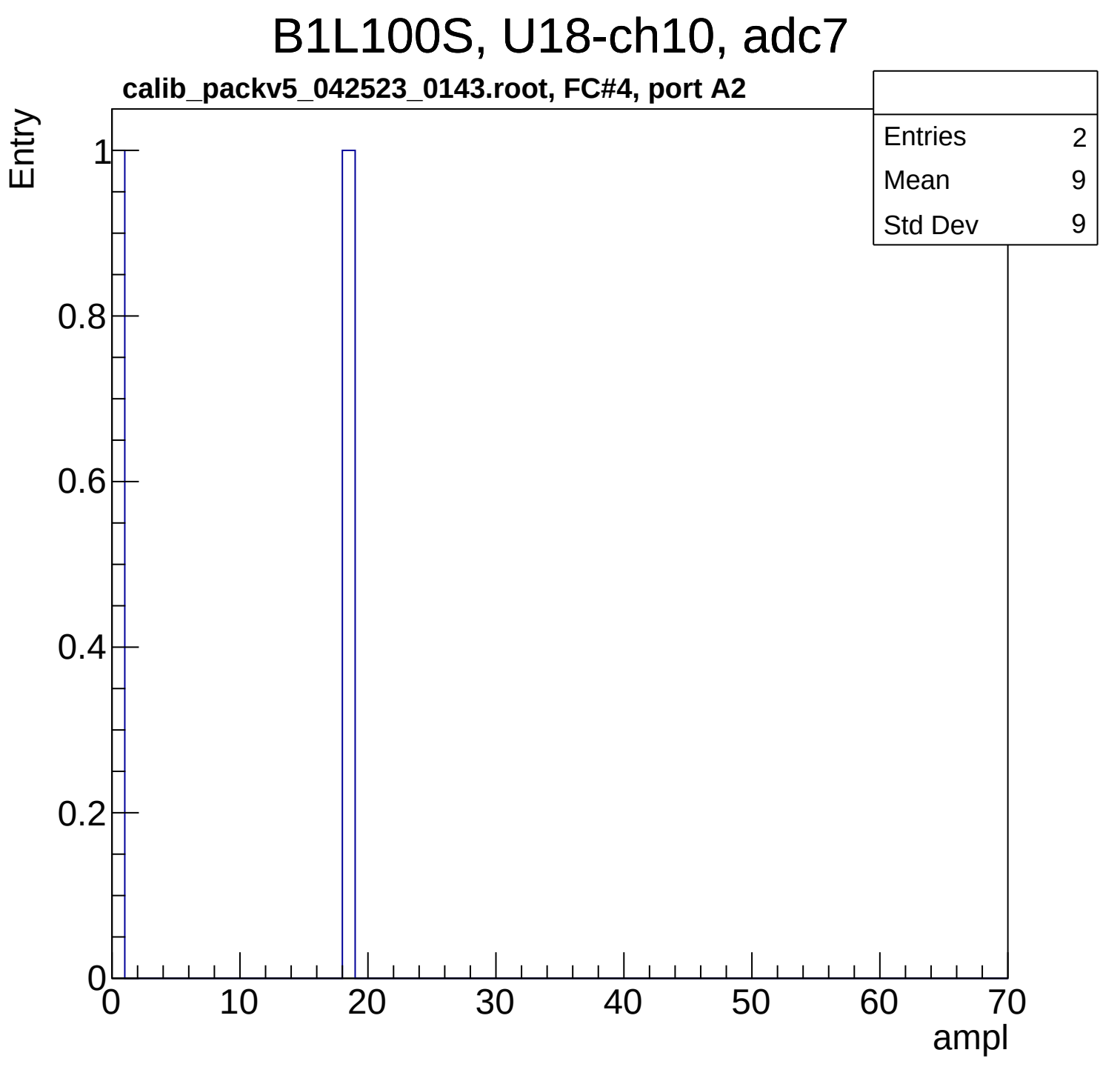

B1L100S, U18-ch10, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 42.72
Std Dev 3.436
Gaus mean : 43.3474
Gaus Width: 3.4218
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

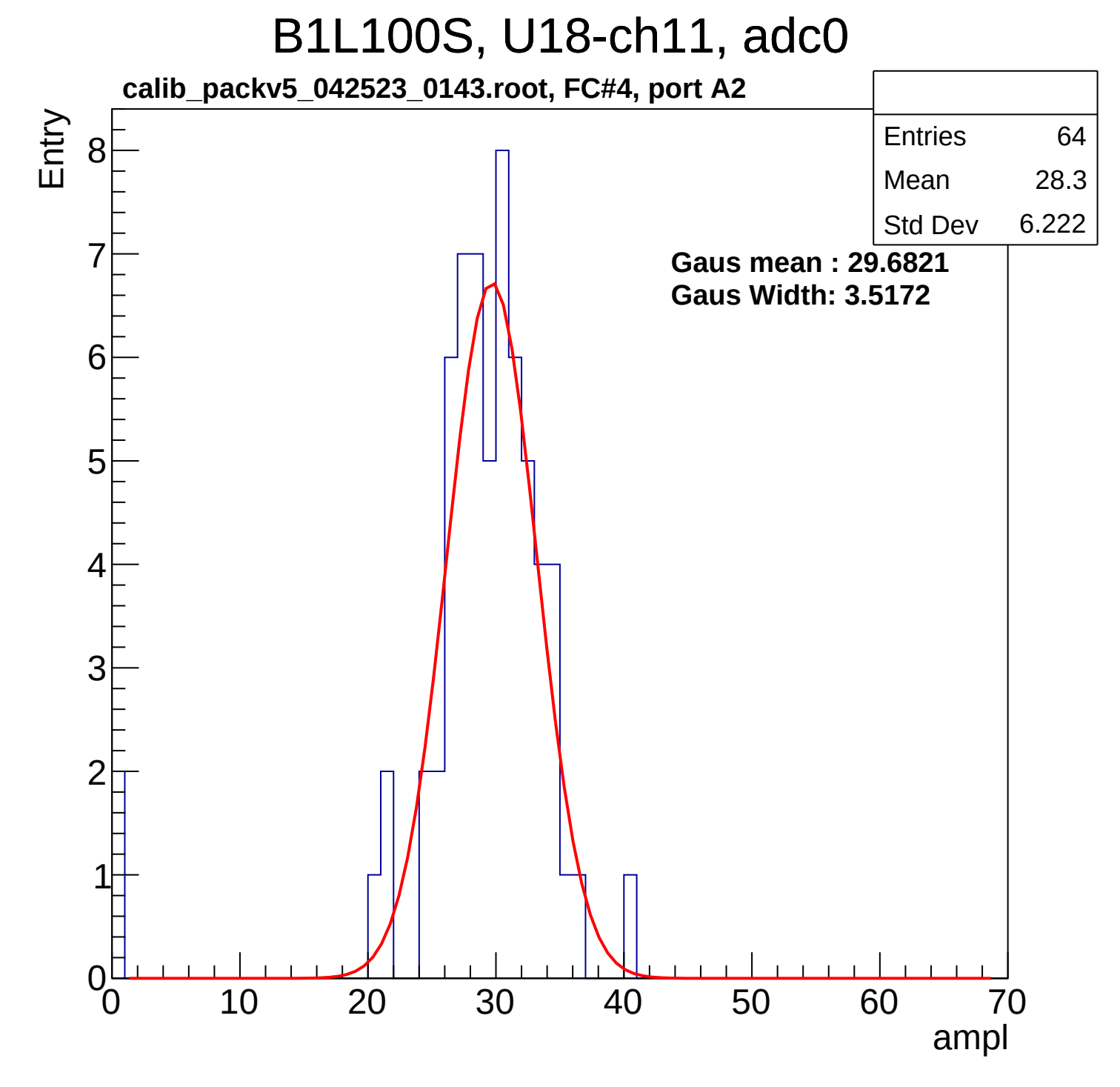

B1L100S, U18-ch10, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 49.12
Std Dev 3.42
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

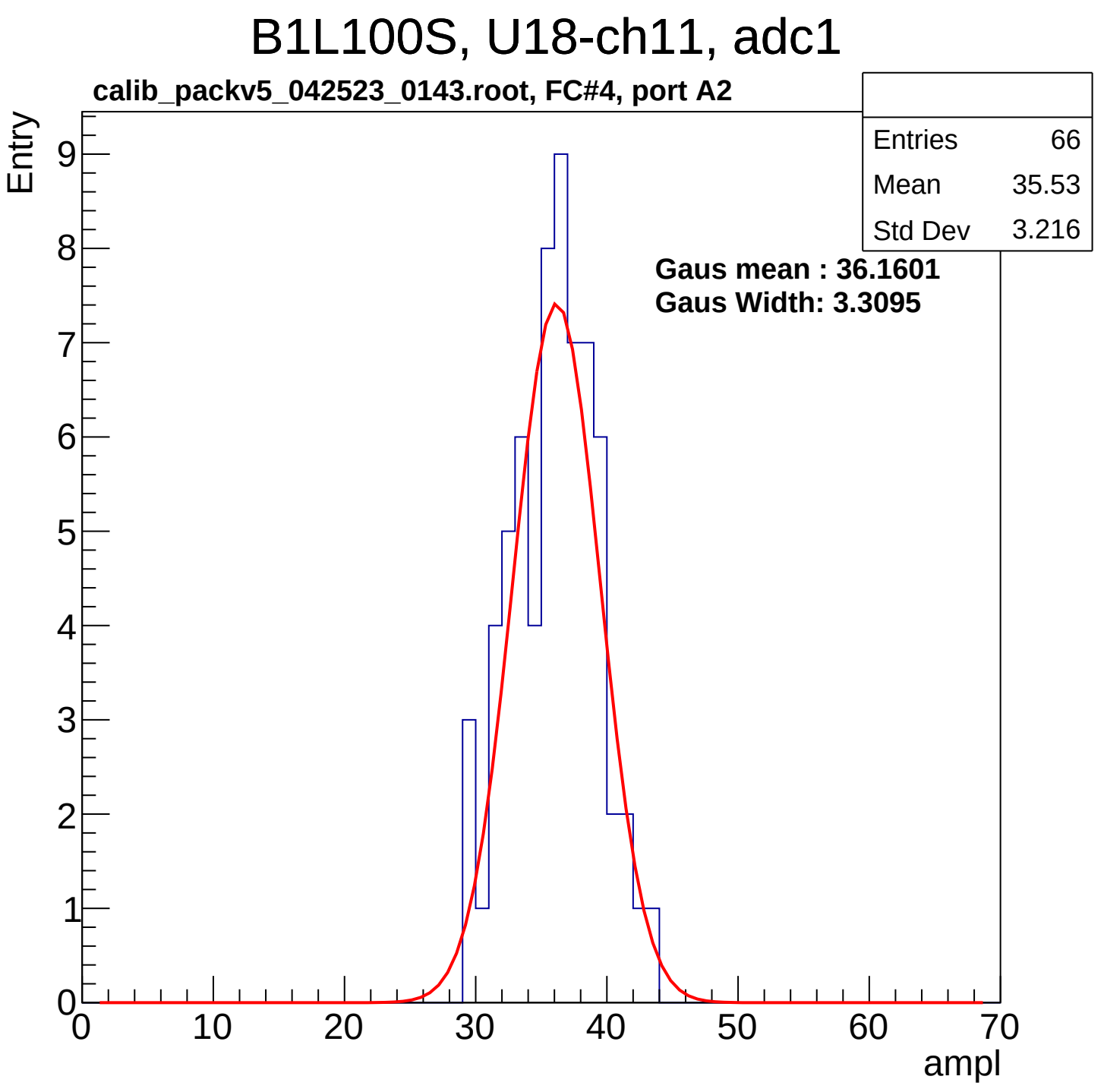

B1L100S, U18-ch10, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 55.46
Std Dev 3.077
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

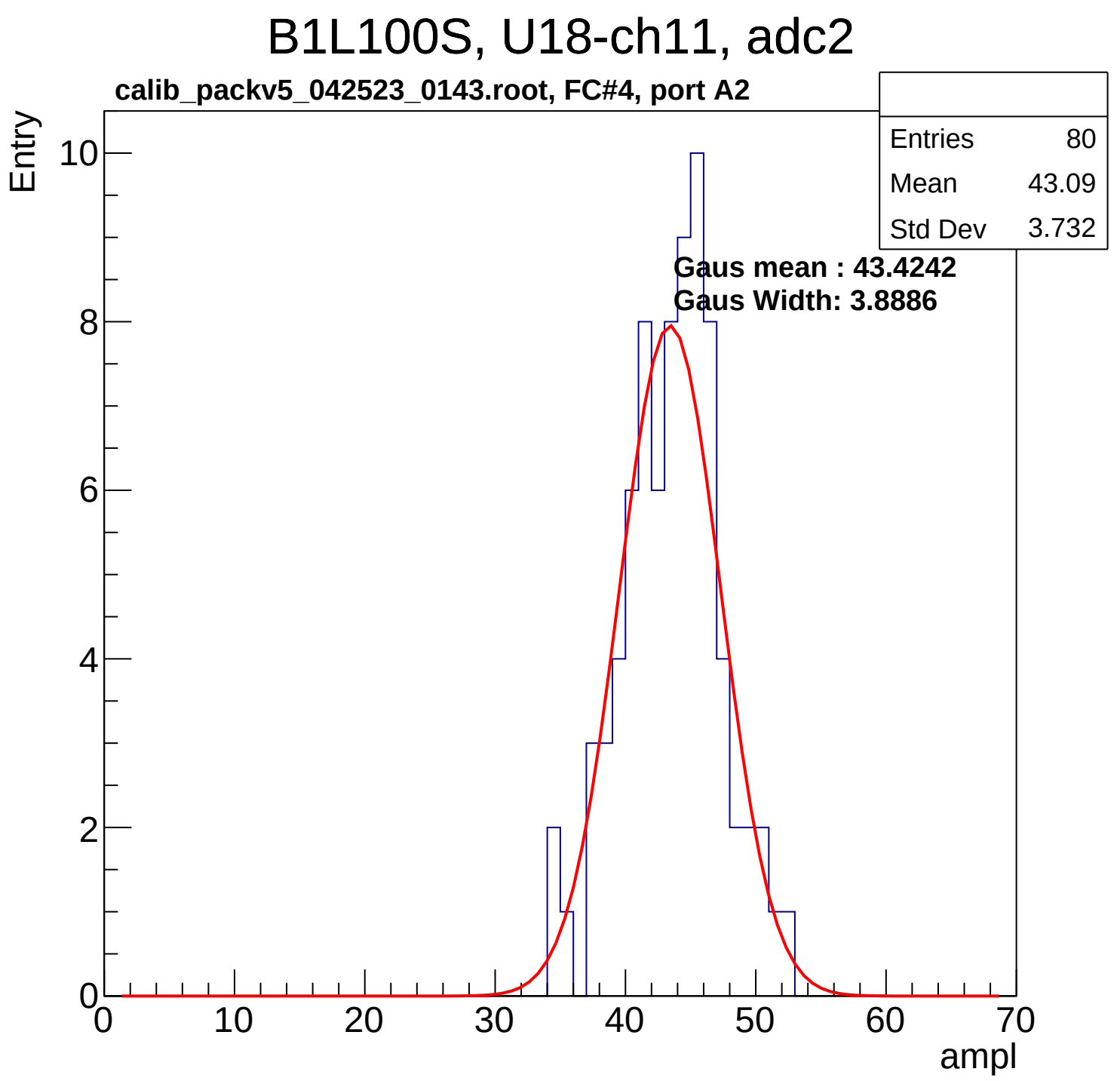

B1L100S, U18-ch10, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 58.6
Std Dev 8.641
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

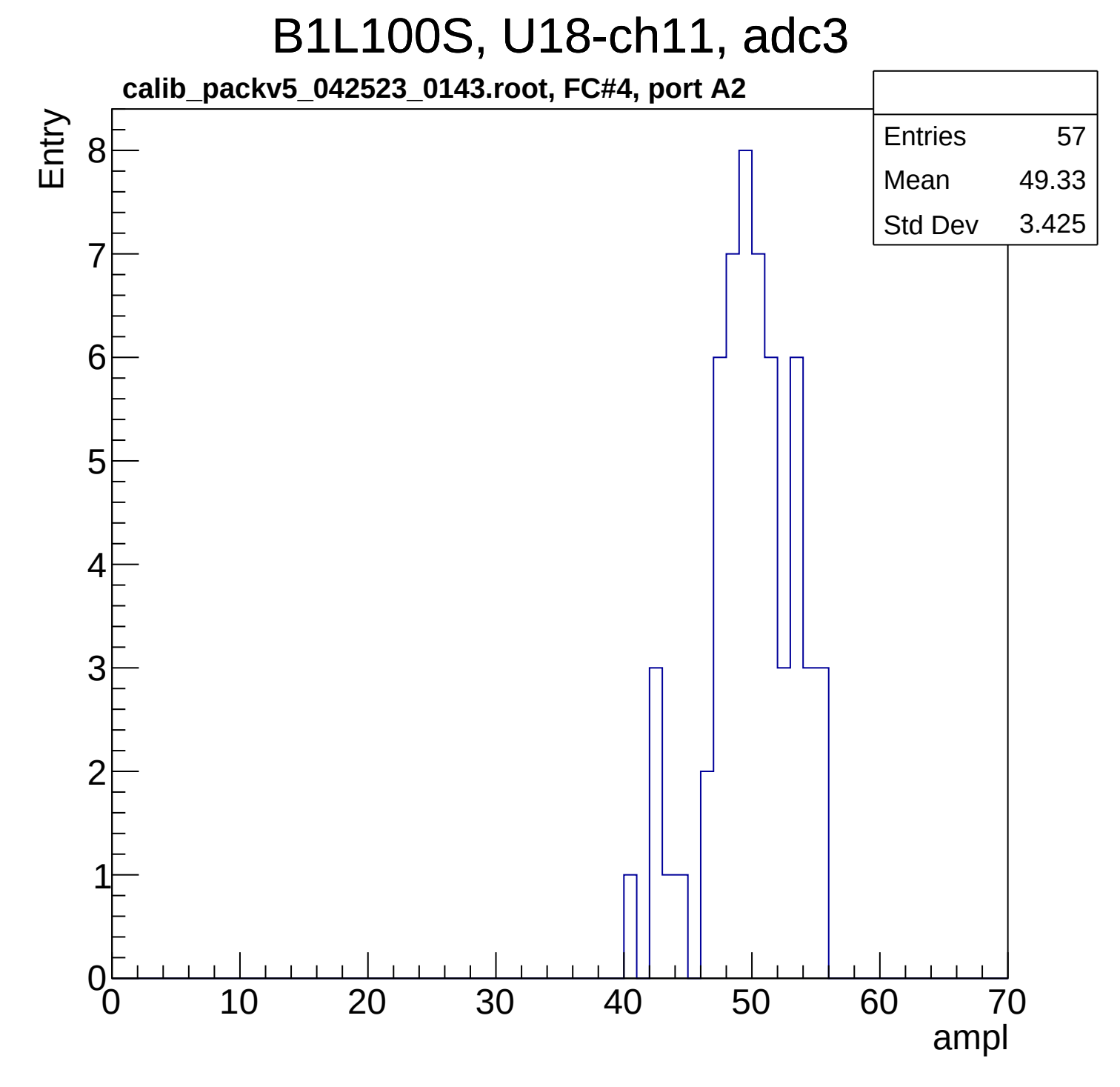

B1L100S, U18-ch10, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 61.67
Std Dev 1.886
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

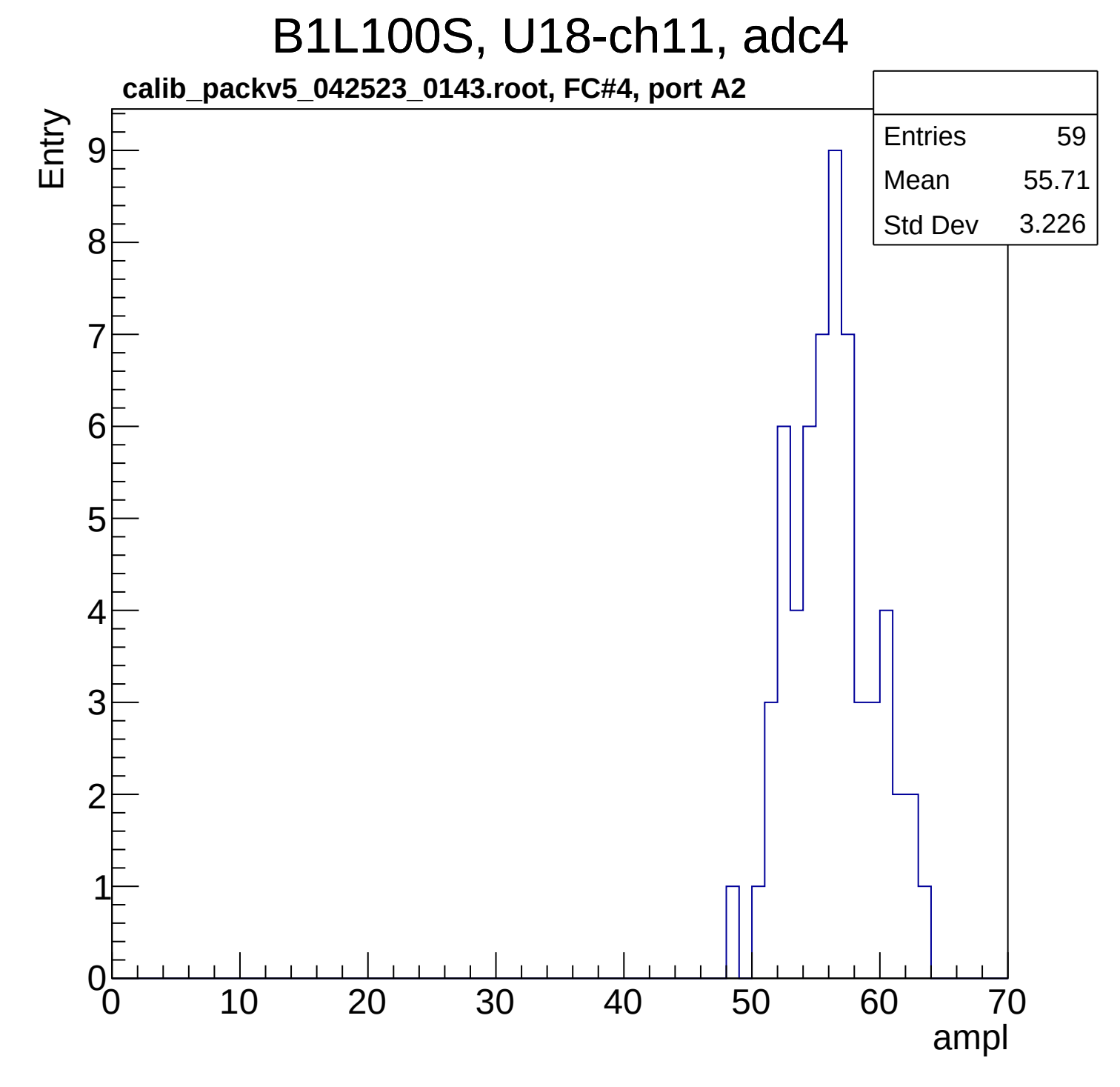

B1L100S, U18-ch10, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 9
Std Dev 9
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

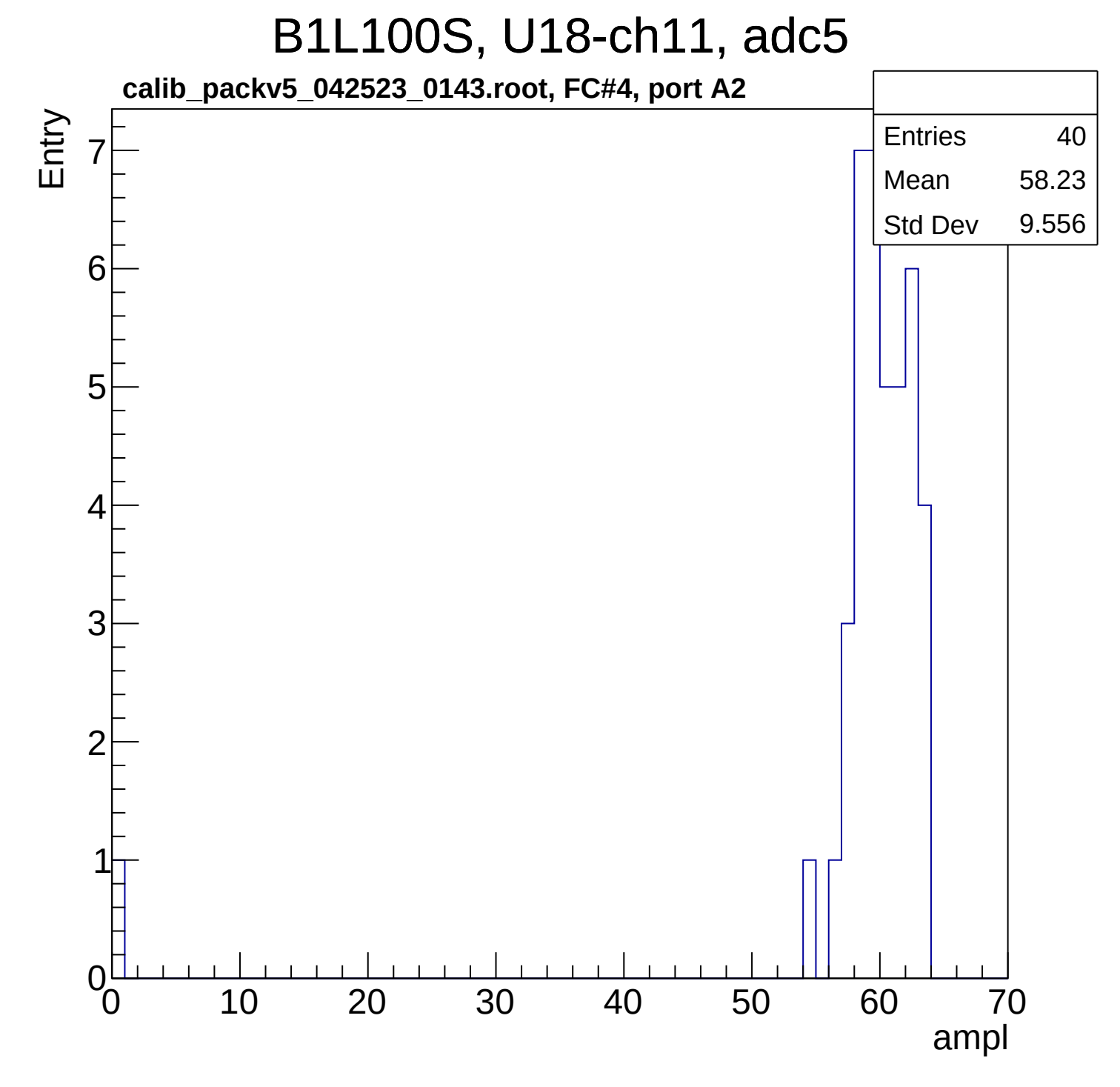

B1L100S, U18-ch11, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 28.3
Std Dev 6.222
Gaus mean : 29.6821
Gaus Width: 3.5172
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

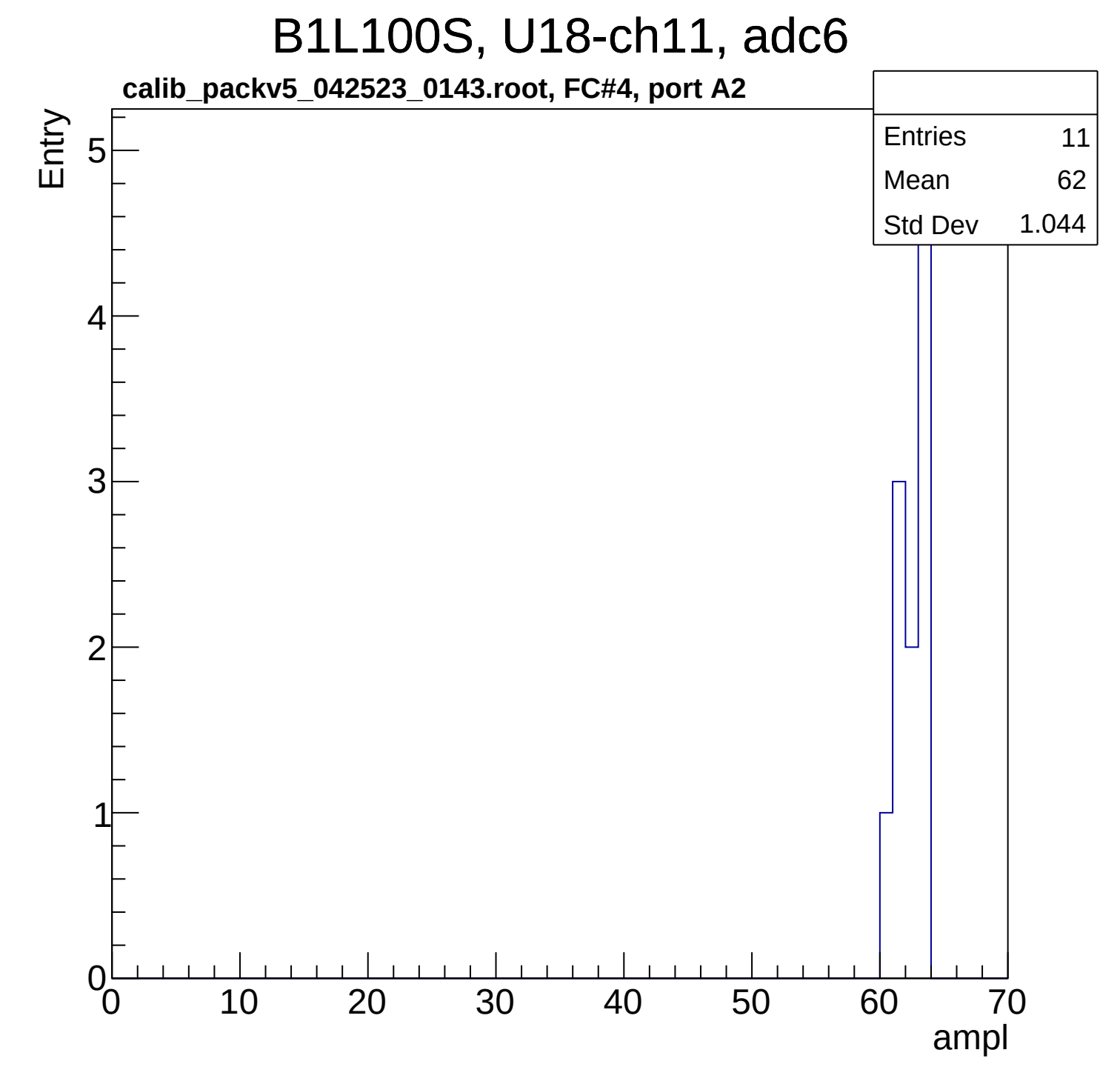

B1L100S, U18-ch11, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 35.53
Std Dev 3.216
Gaus mean : 36.1601
Gaus Width: 3.3095
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

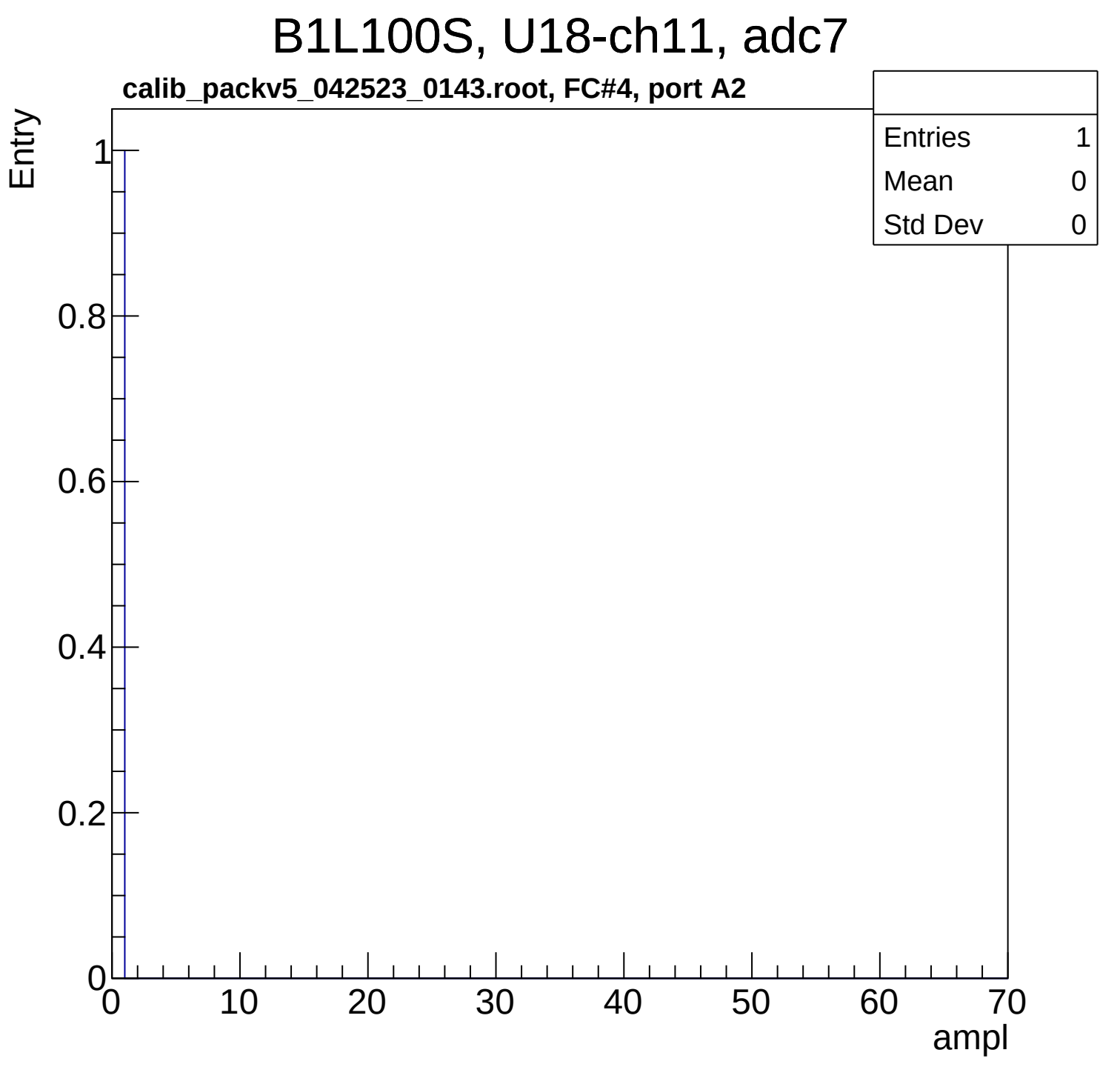

B1L100S, U18-ch11, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 43.09
Std Dev 3.732
Gaus mean : 43.4242
Gaus Width: 3.8886
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

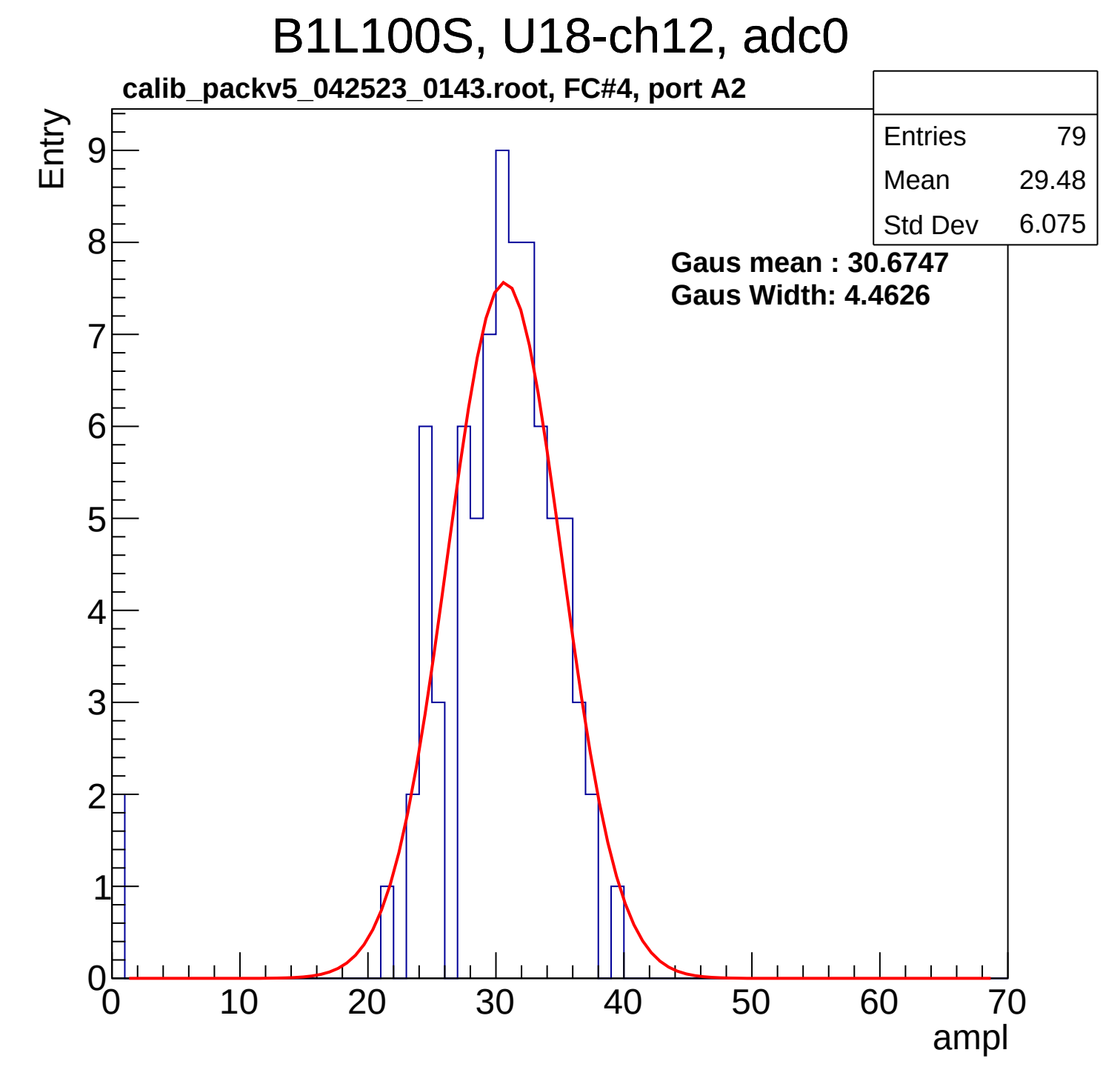

B1L100S, U18-ch11, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 49.33
Std Dev 3.425
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

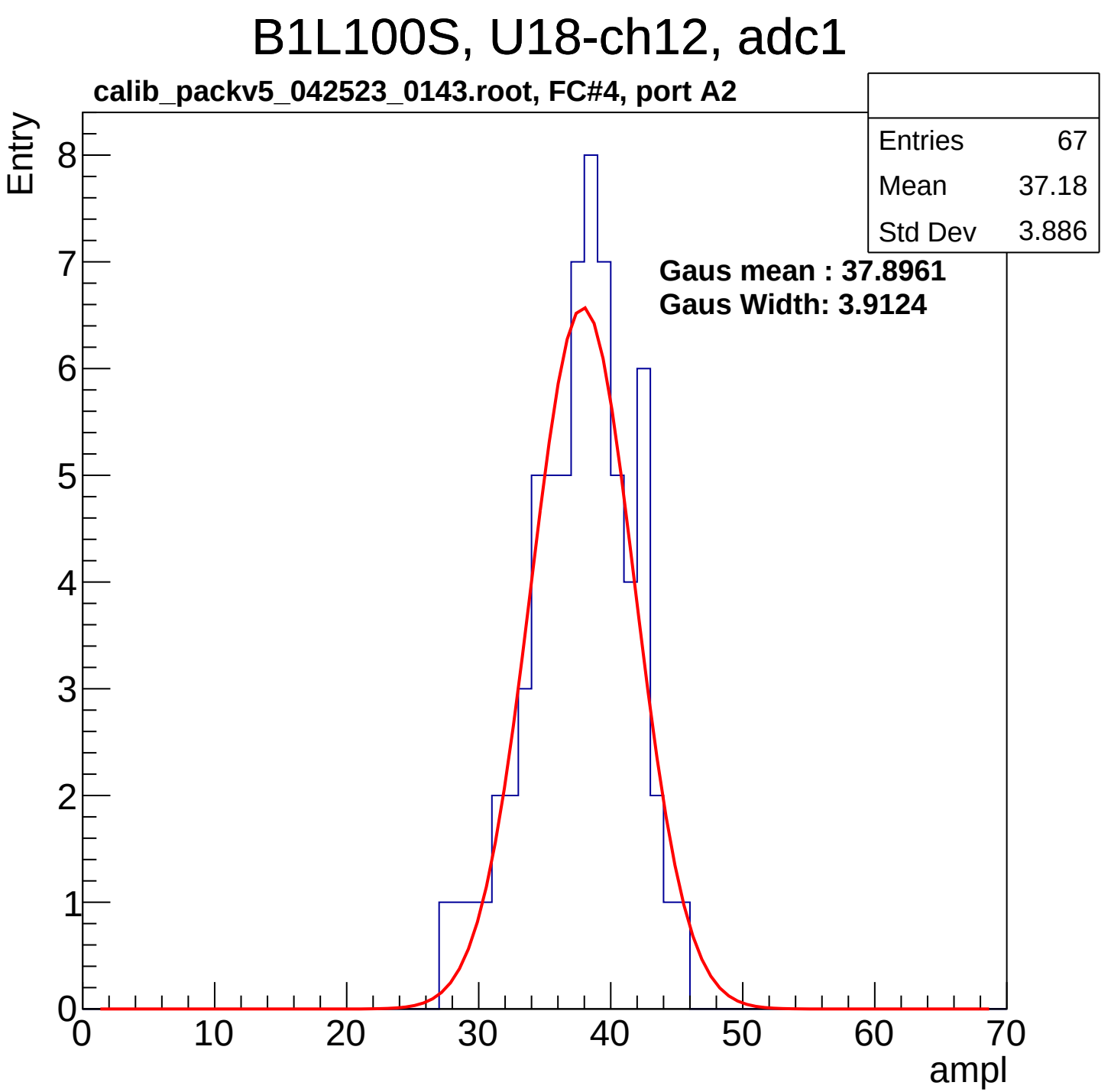

B1L100S, U18-ch11, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 55.71
Std Dev 3.226
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

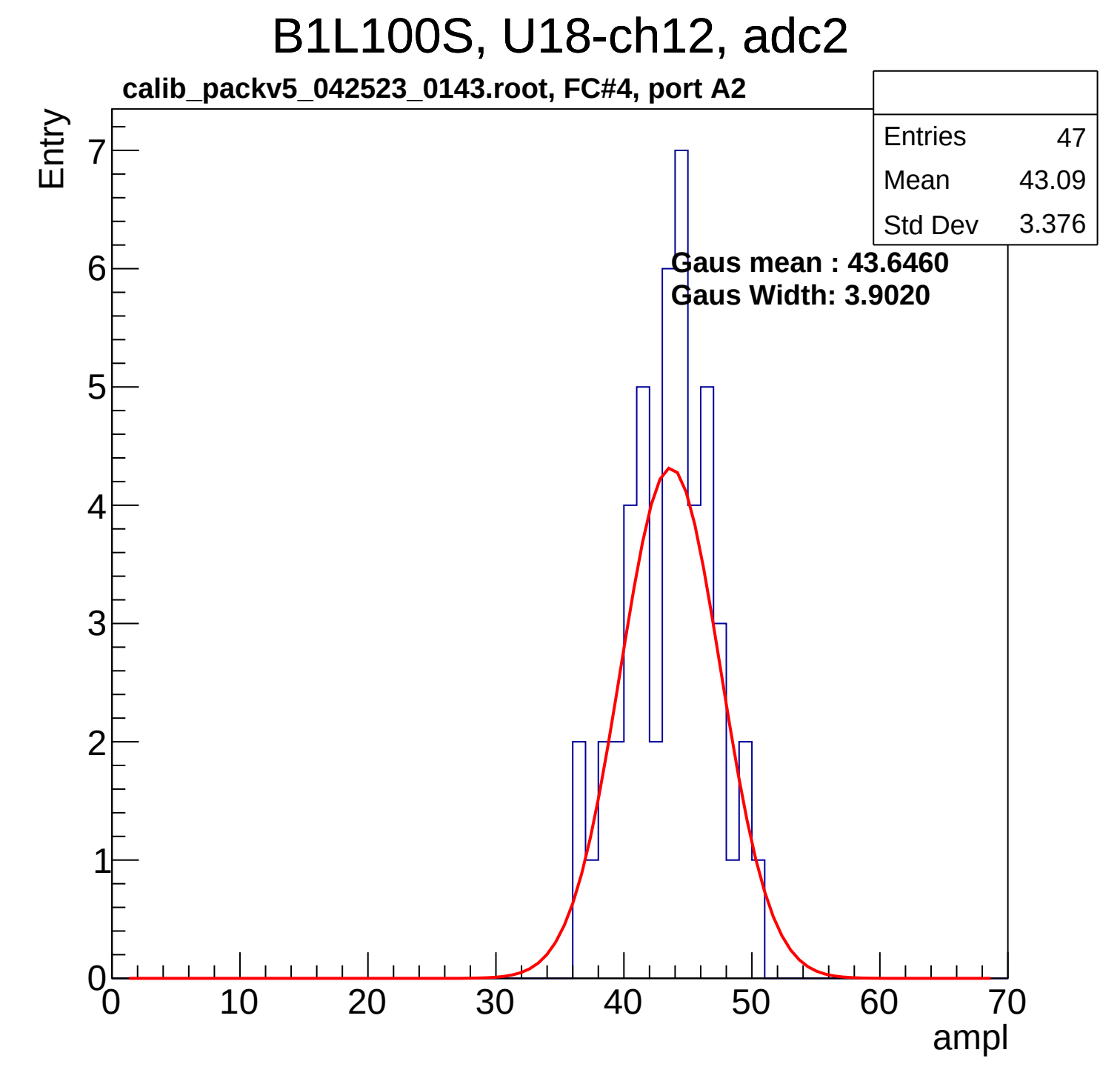

B1L100S, U18-ch11, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 40
Mean 58.23
Std Dev 9.556
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

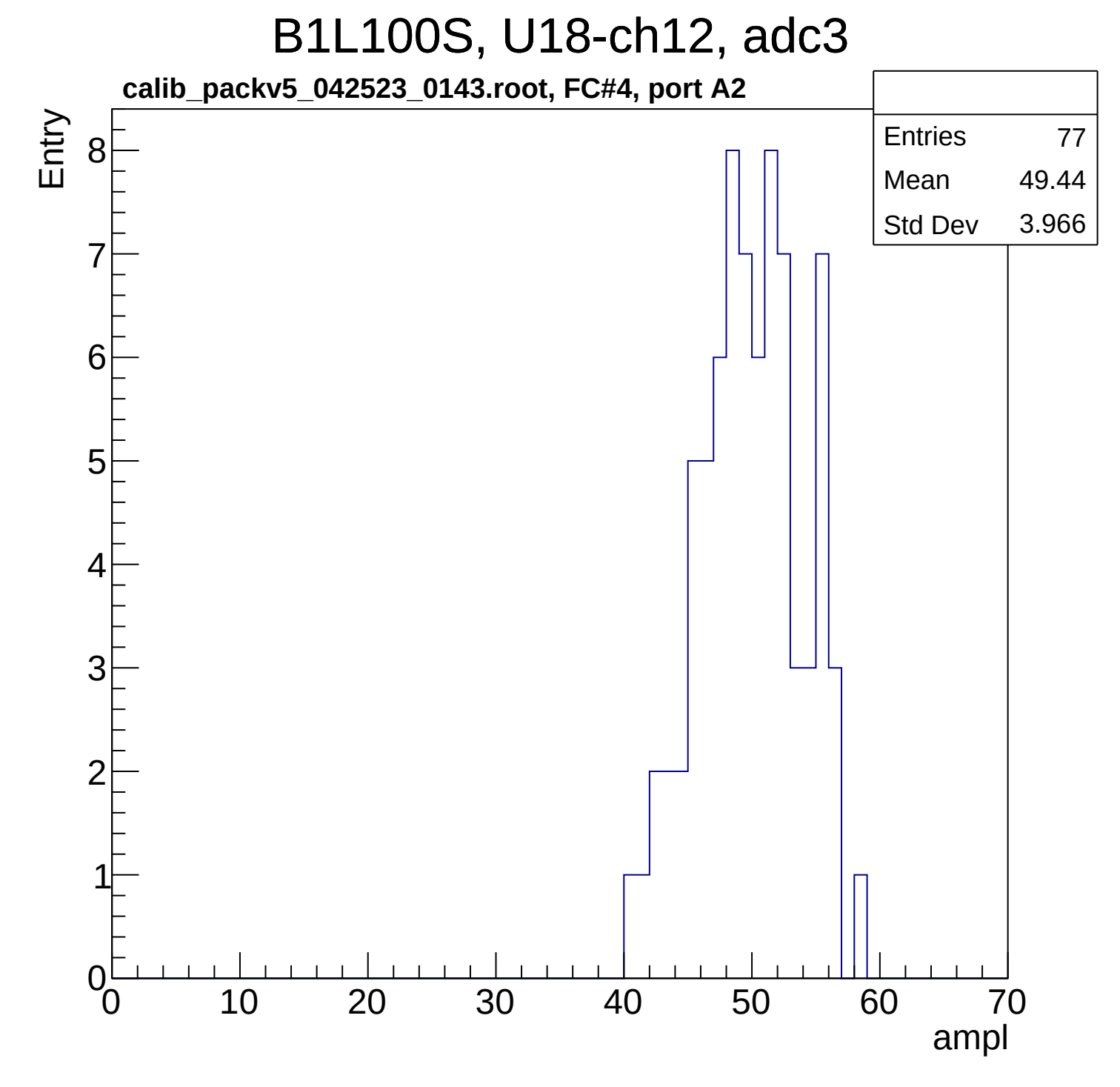

B1L100S, U18-ch11, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 62
Std Dev 1.044
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

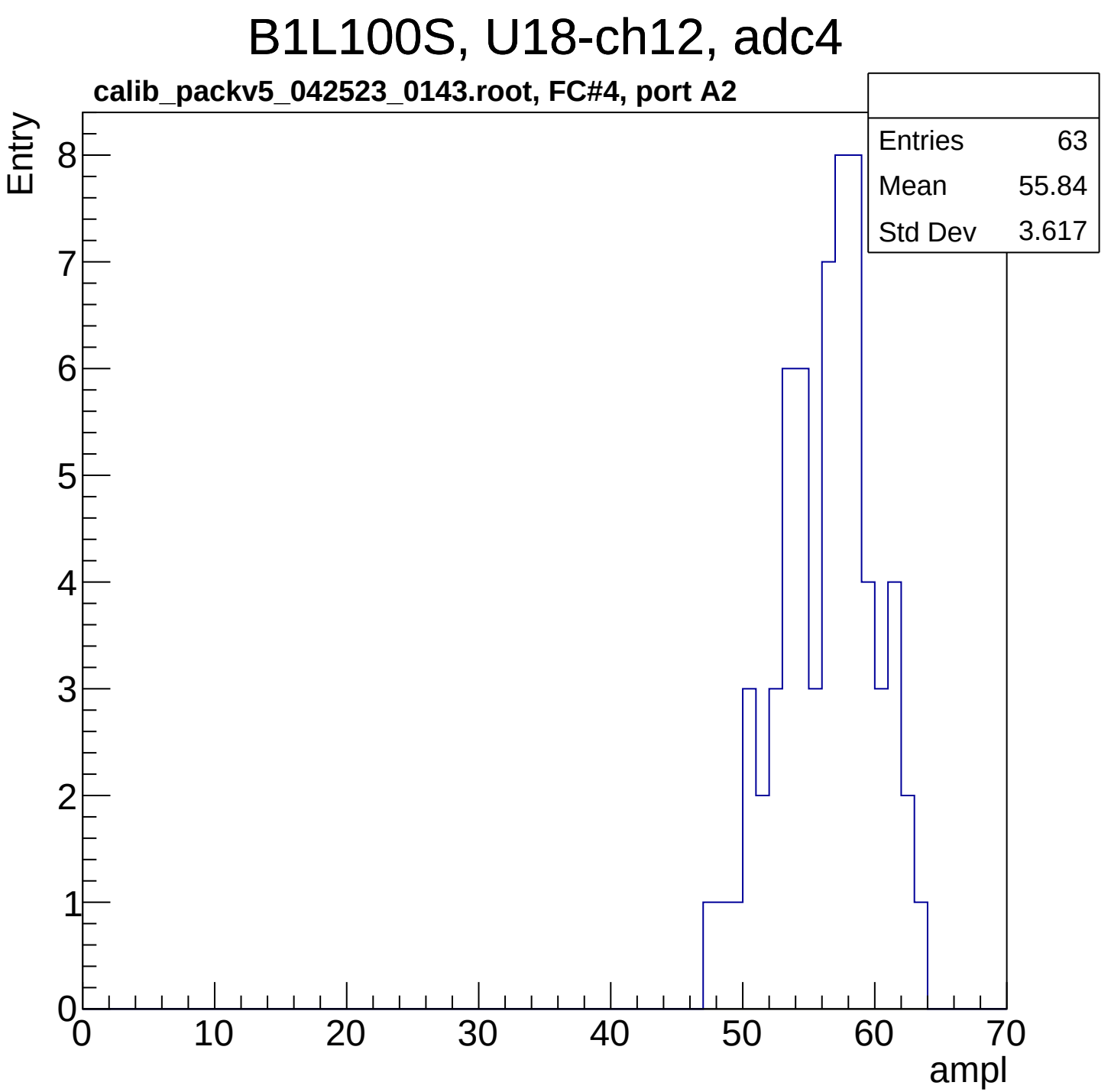

B1L100S, U18-ch11, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

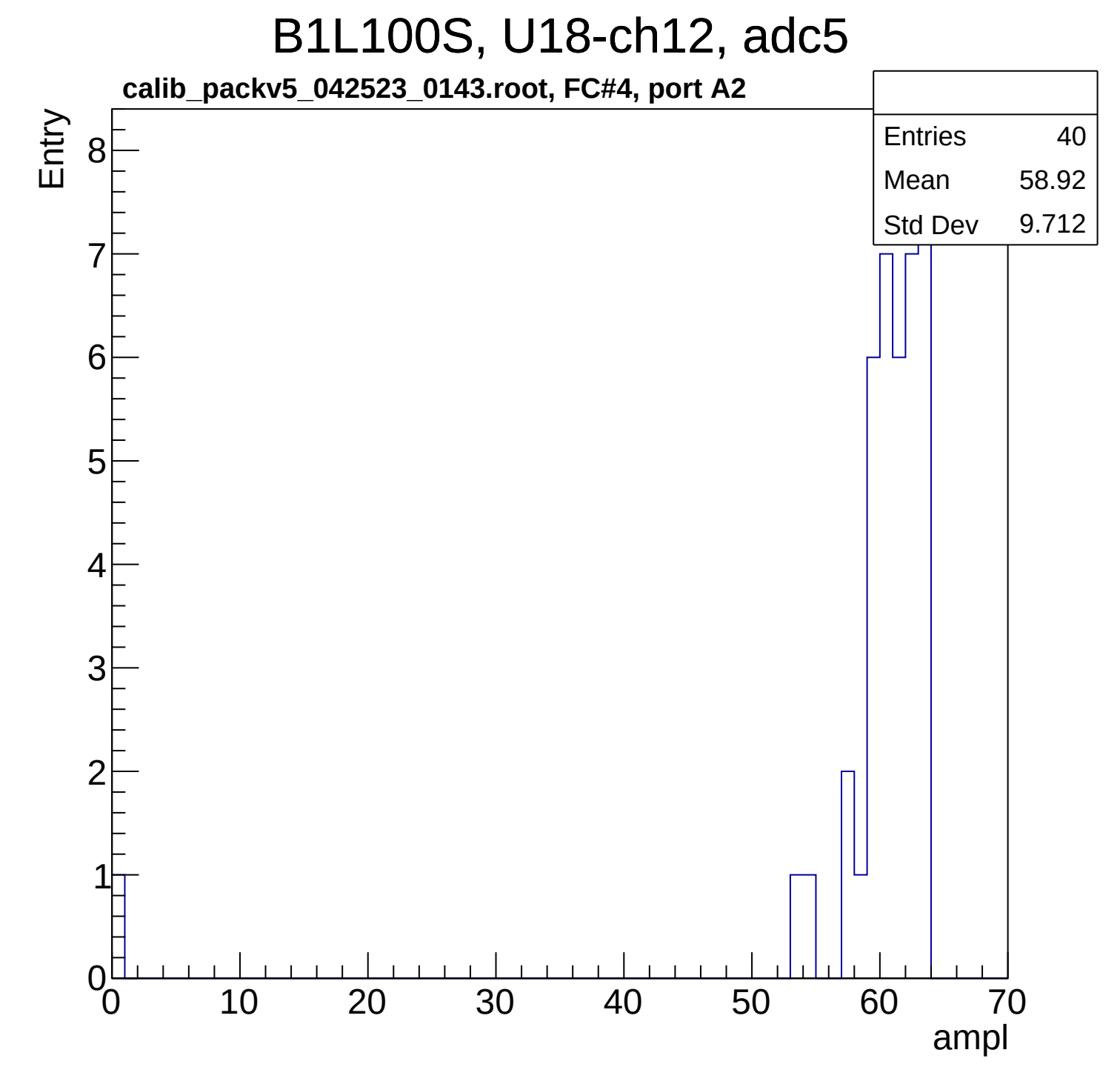

B1L100S, U18-ch12, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 29.48
Std Dev 6.075
Gaus mean : 30.6747
Gaus Width: 4.4626
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

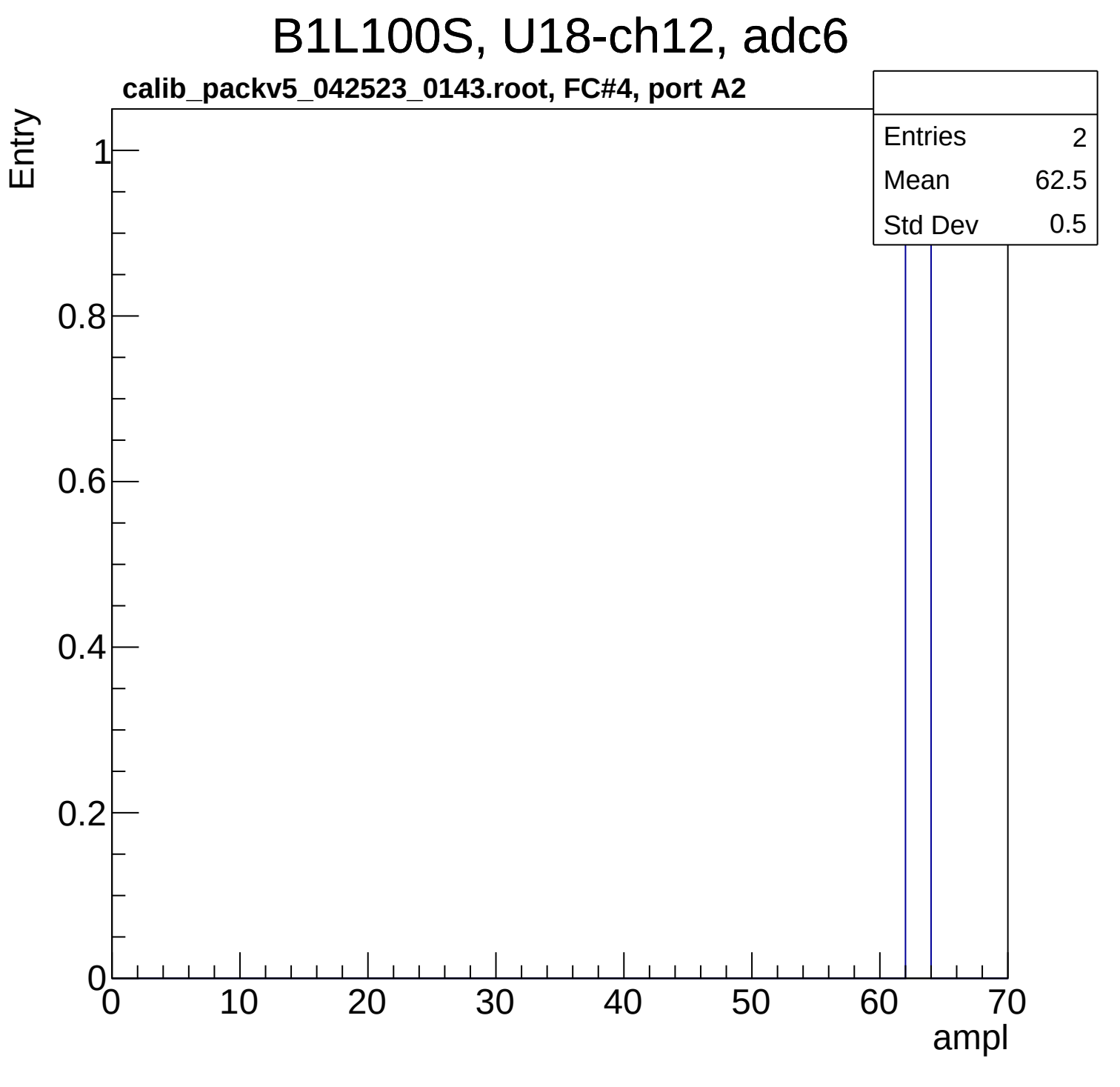

B1L100S, U18-ch12, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 37.18
Std Dev 3.886
Gaus mean : 37.8961
Gaus Width: 3.9124
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

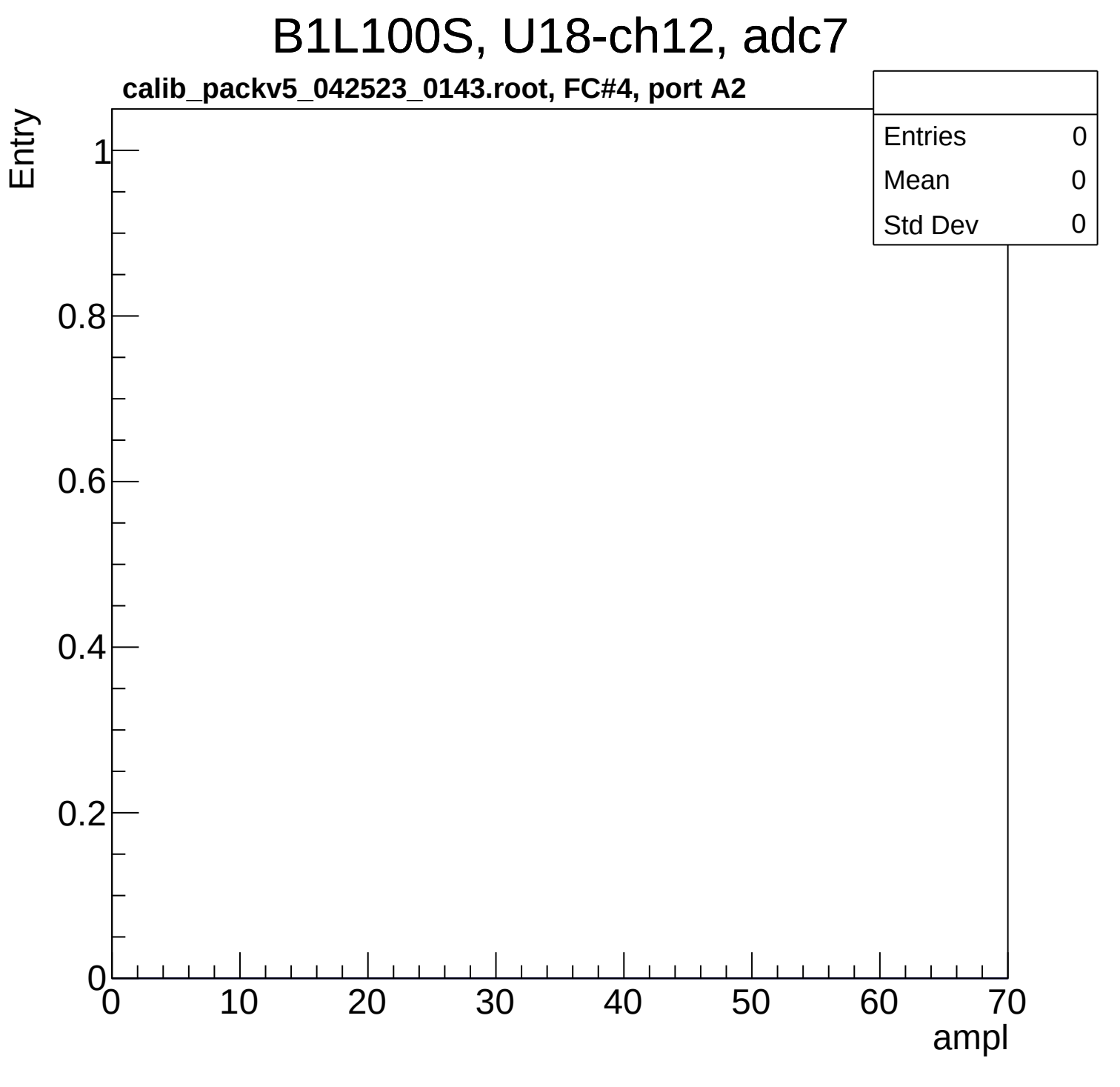

B1L100S, U18-ch12, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 43.09
Std Dev 3.376
Gaus mean : 43.6460
Gaus Width: 3.9020
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

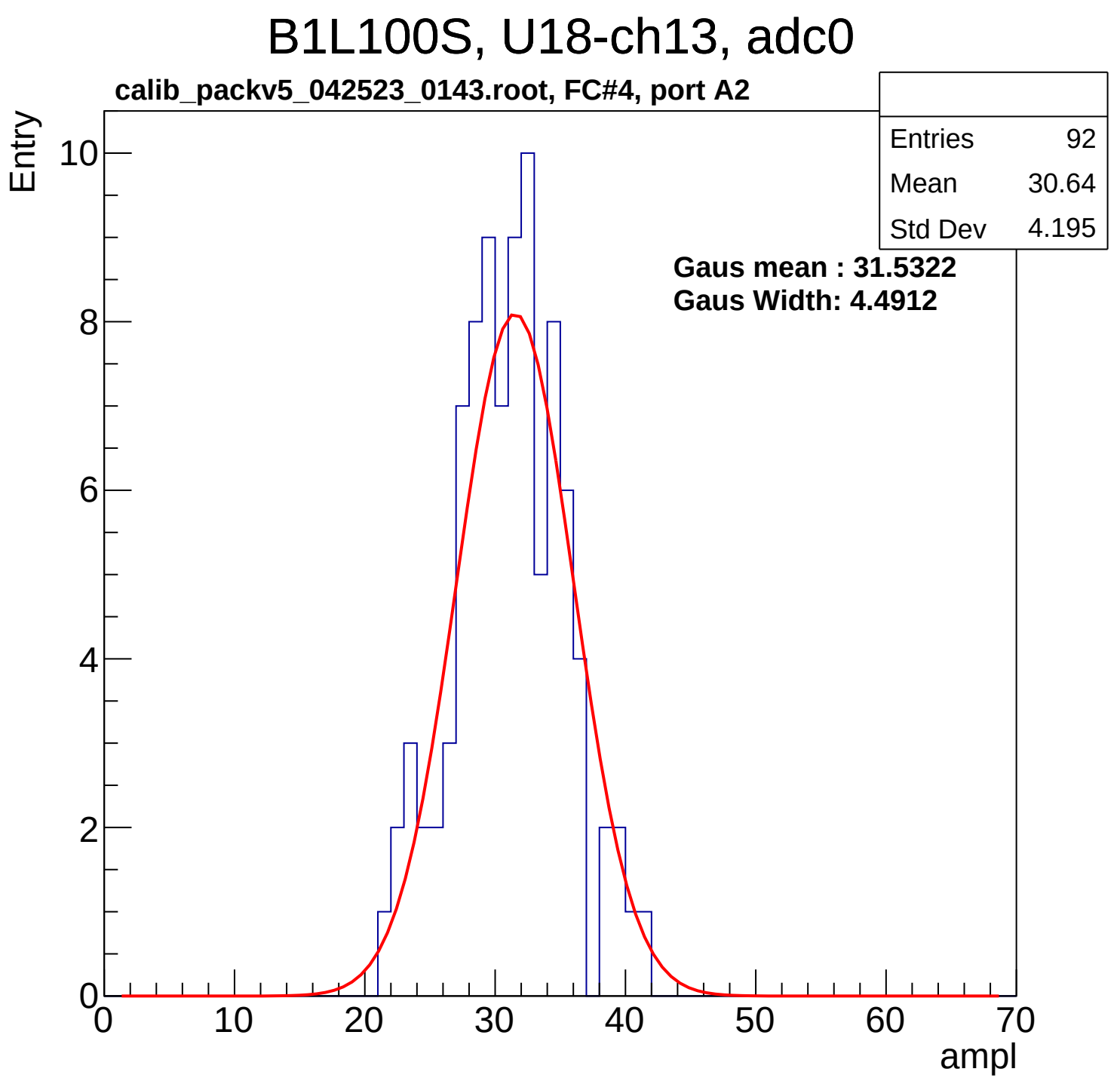

B1L100S, U18-ch12, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 49.44
Std Dev 3.966
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

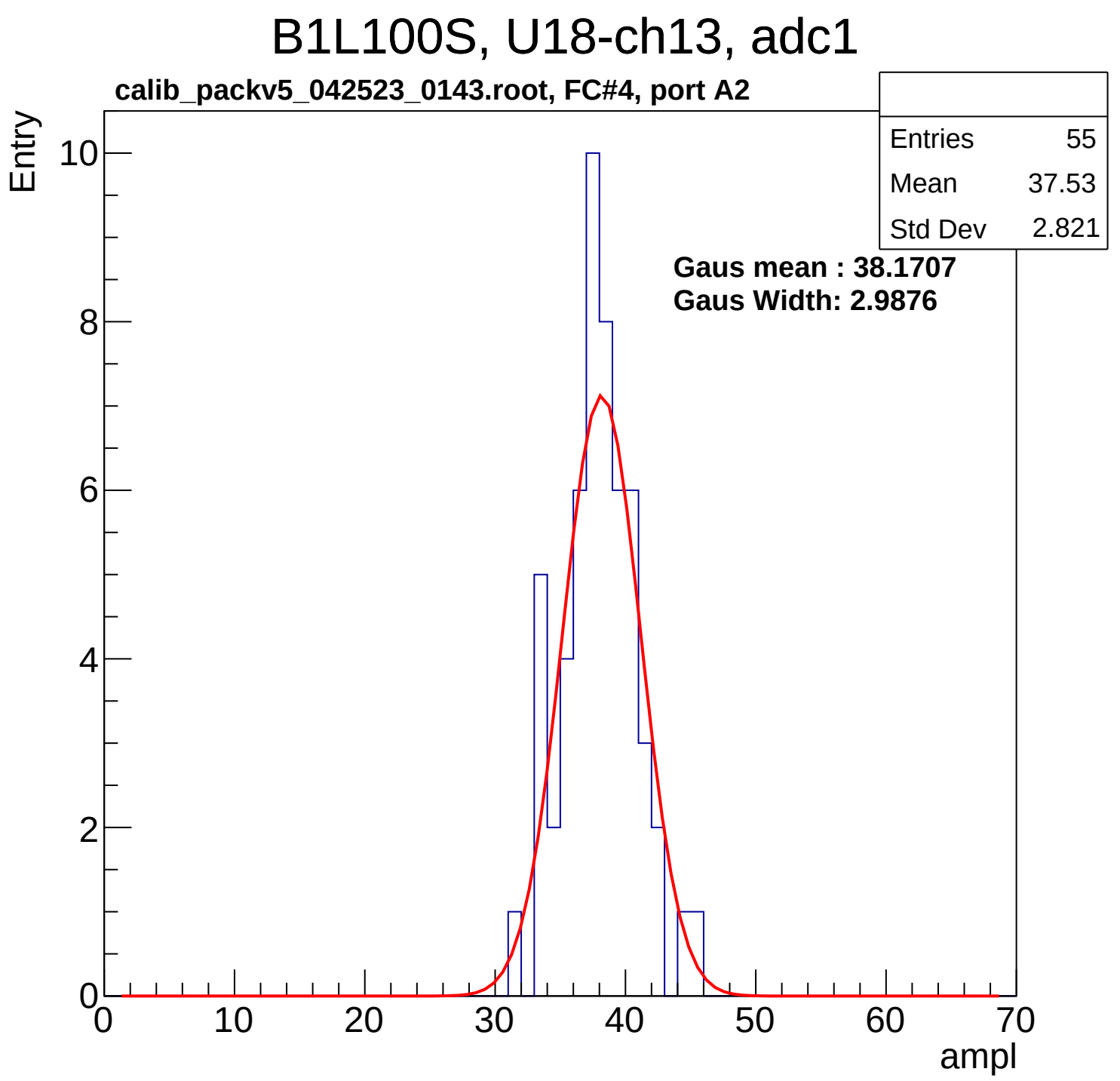

B1L100S, U18-ch12, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 55.84
Std Dev 3.617
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

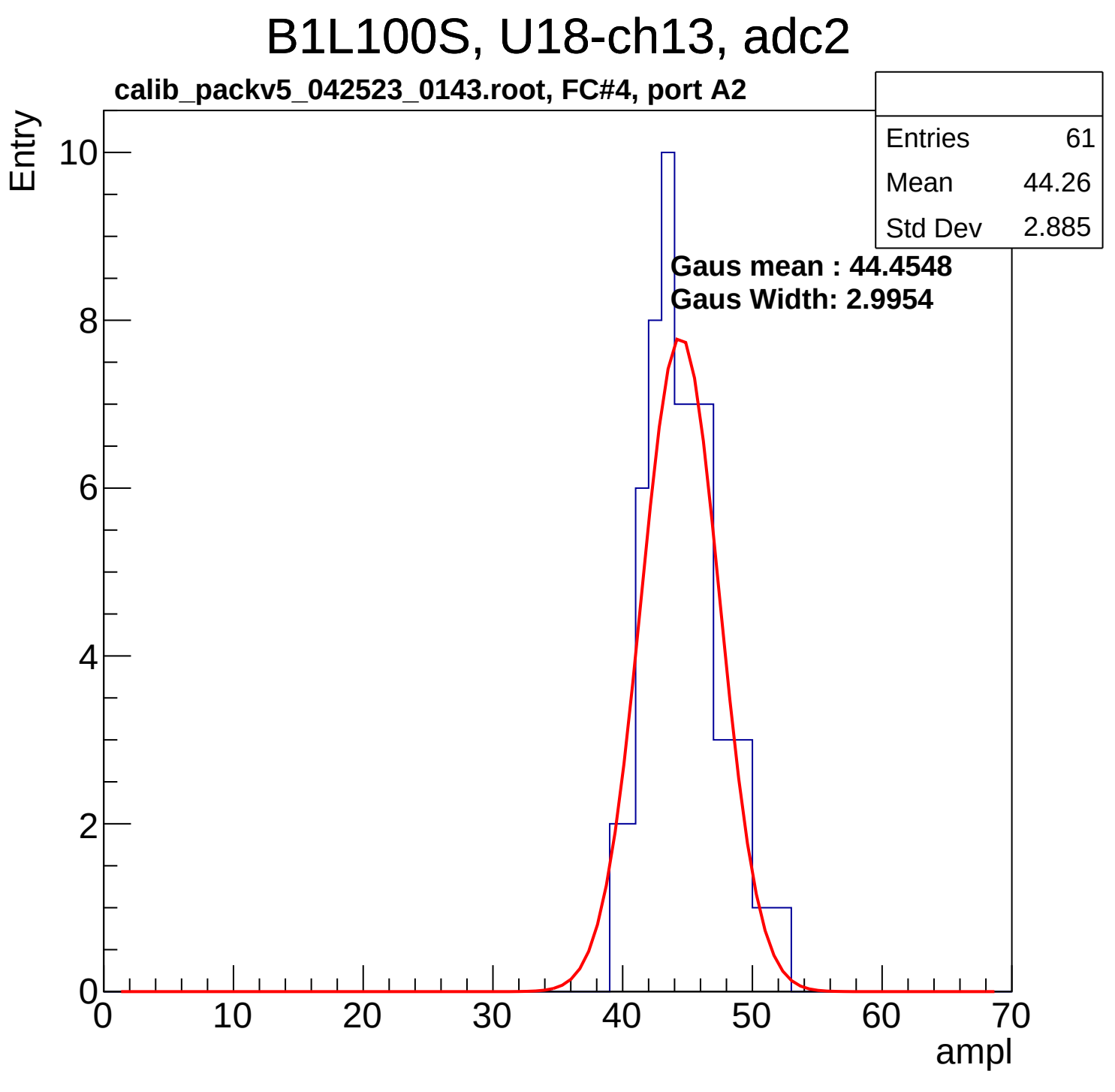

B1L100S, U18-ch12, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 40
Mean 58.92
Std Dev 9.712
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

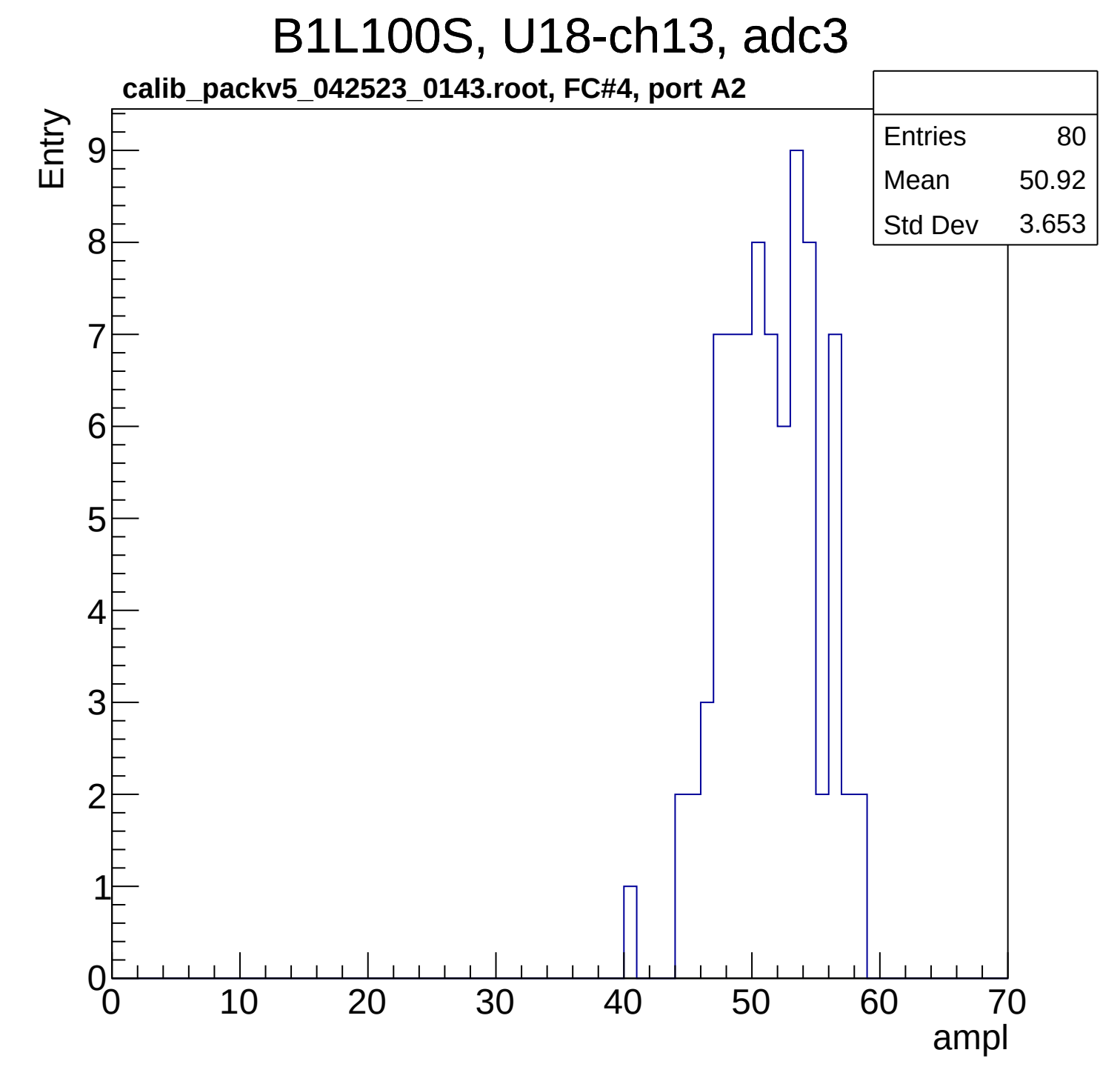

B1L100S, U18-ch12, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

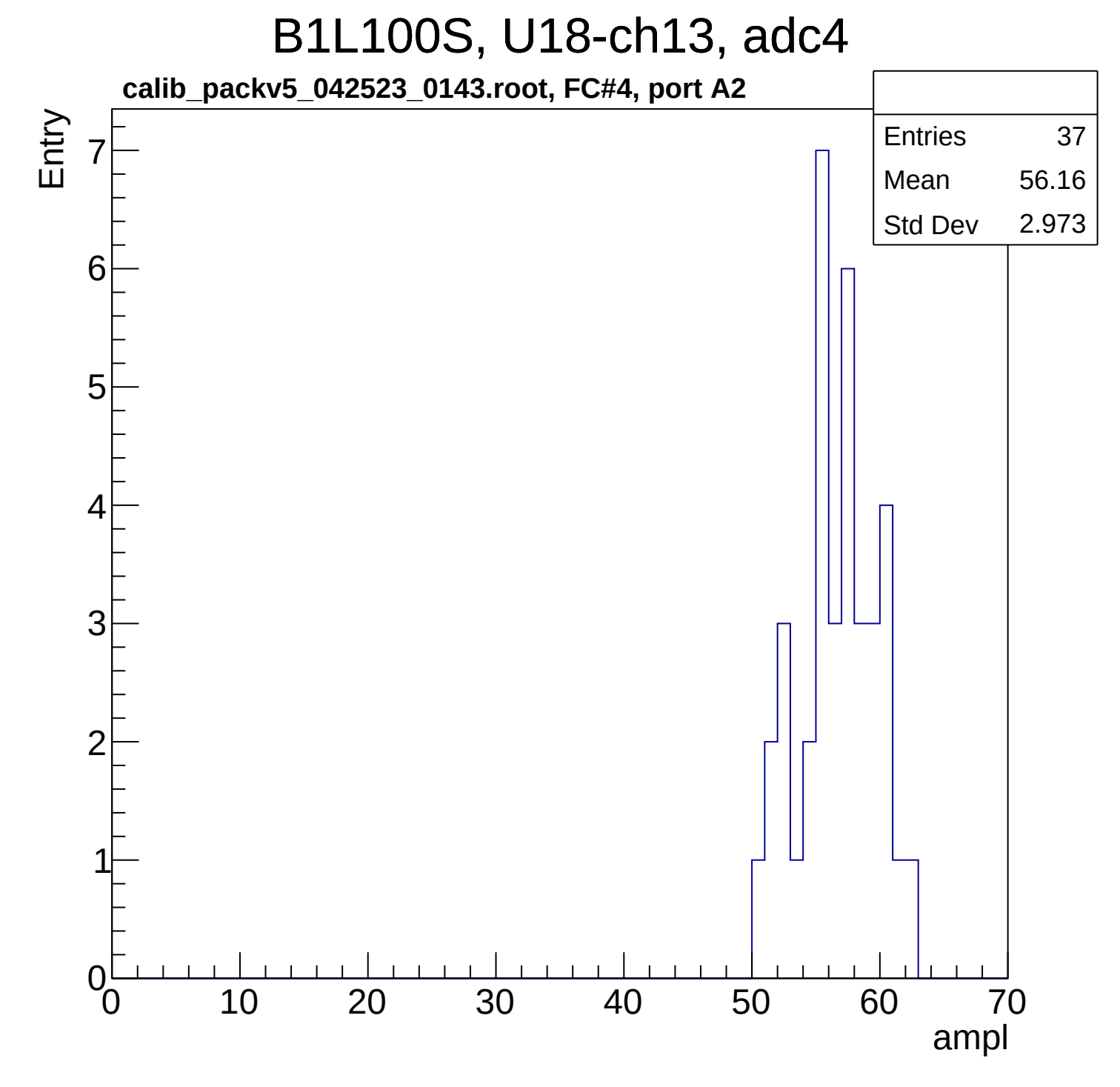

B1L100S, U18-ch12, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

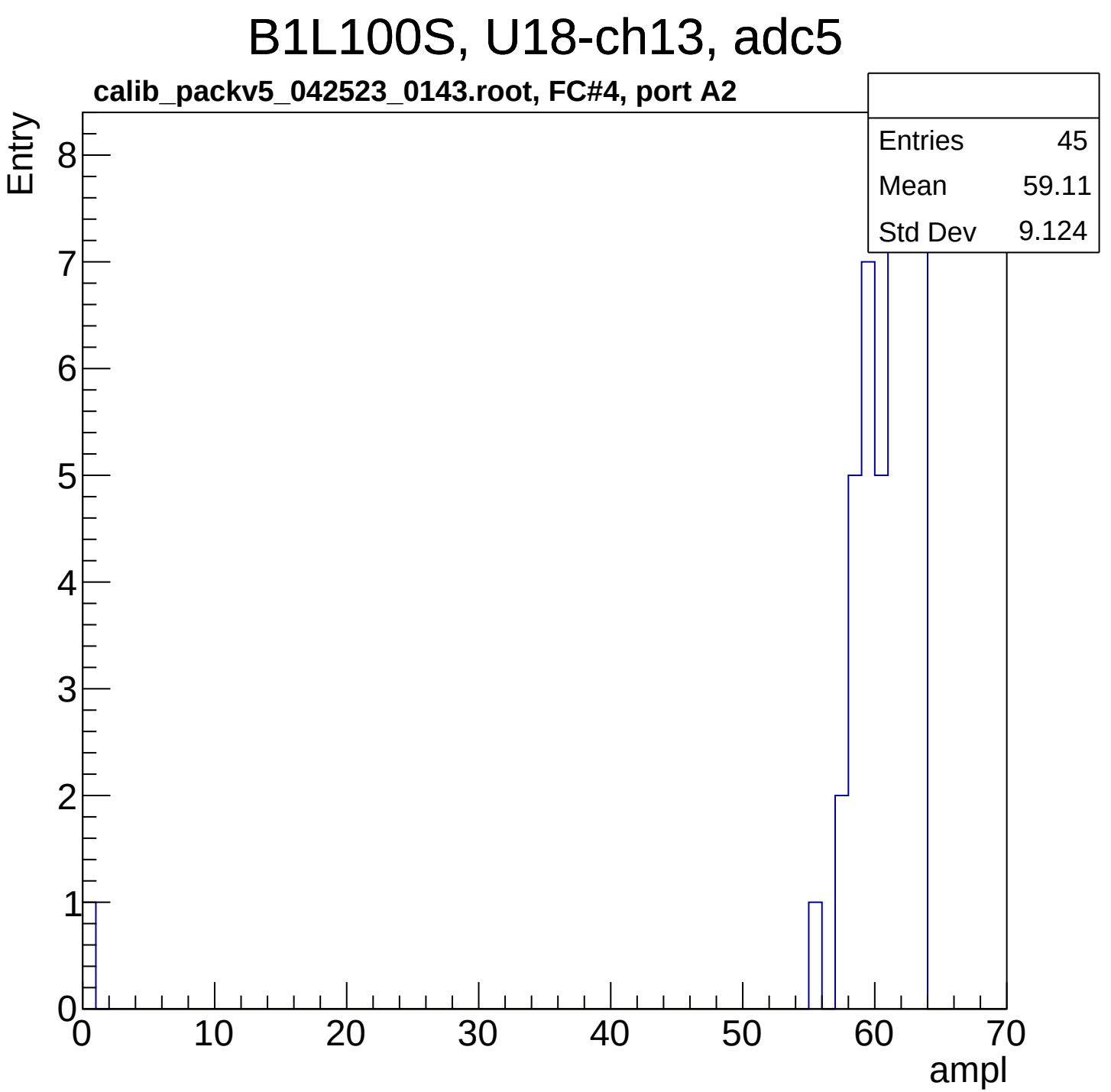

B1L100S, U18-ch13, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 92
Mean 30.64
Std Dev 4.195
Gaus mean : 31.5322
Gaus Width: 4.4912
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

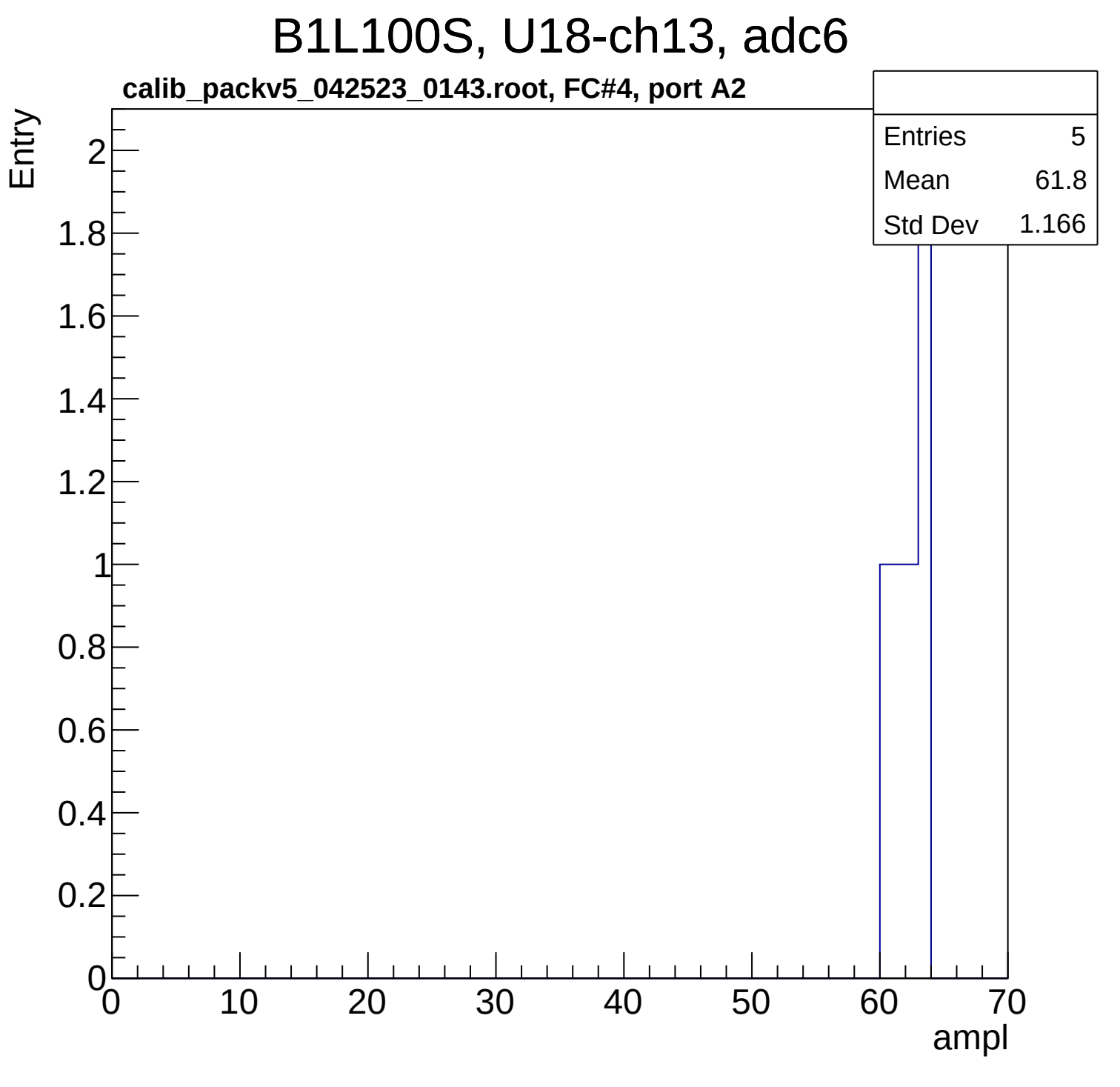

B1L100S, U18-ch13, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 37.53
Std Dev 2.821
Gaus mean : 38.1707
Gaus Width: 2.9876
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

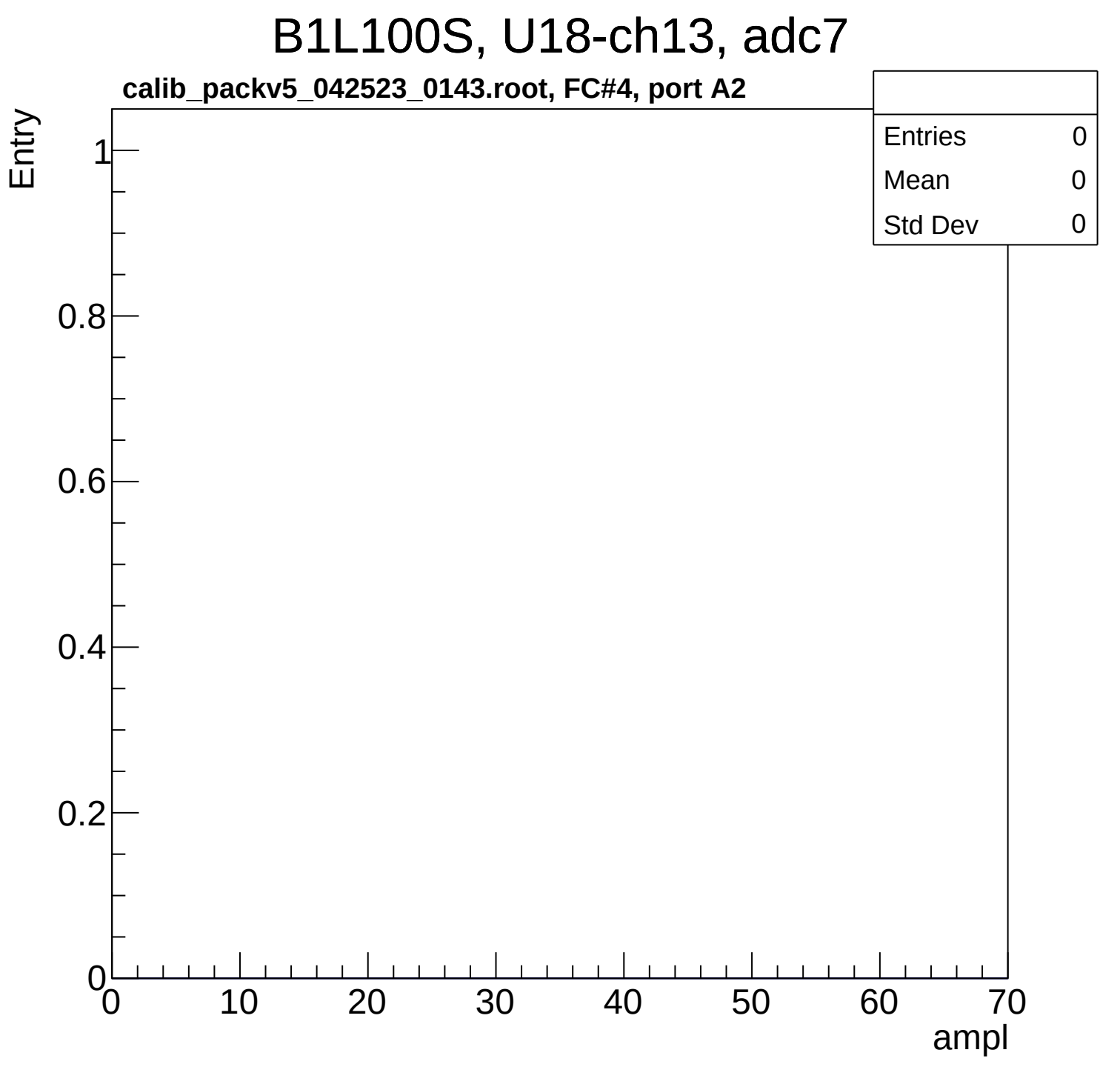

B1L100S, U18-ch13, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 44.26
Std Dev 2.885
Gaus mean : 44.4548
Gaus Width: 2.9954
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

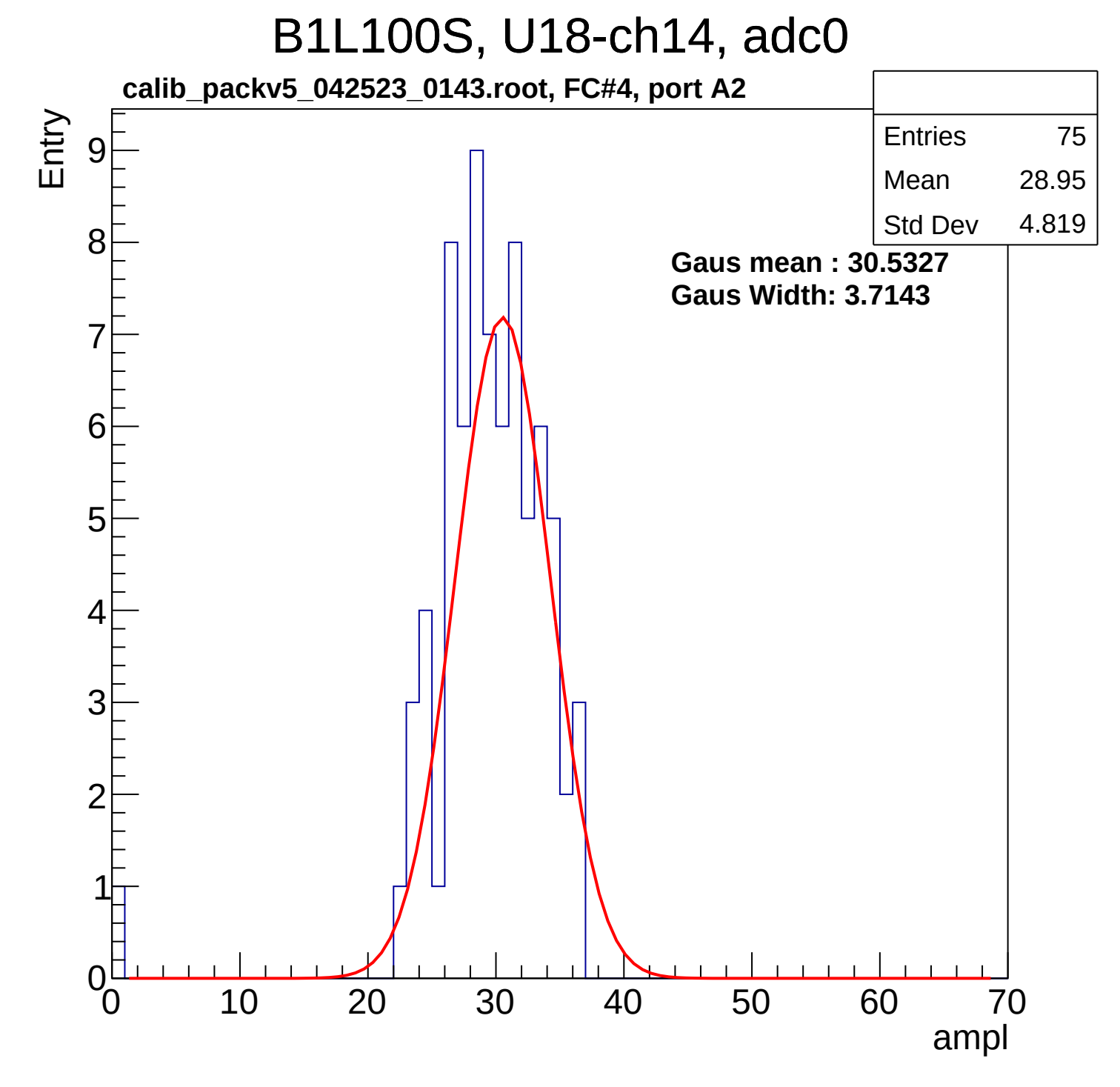

B1L100S, U18-ch13, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 50.92
Std Dev 3.653
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

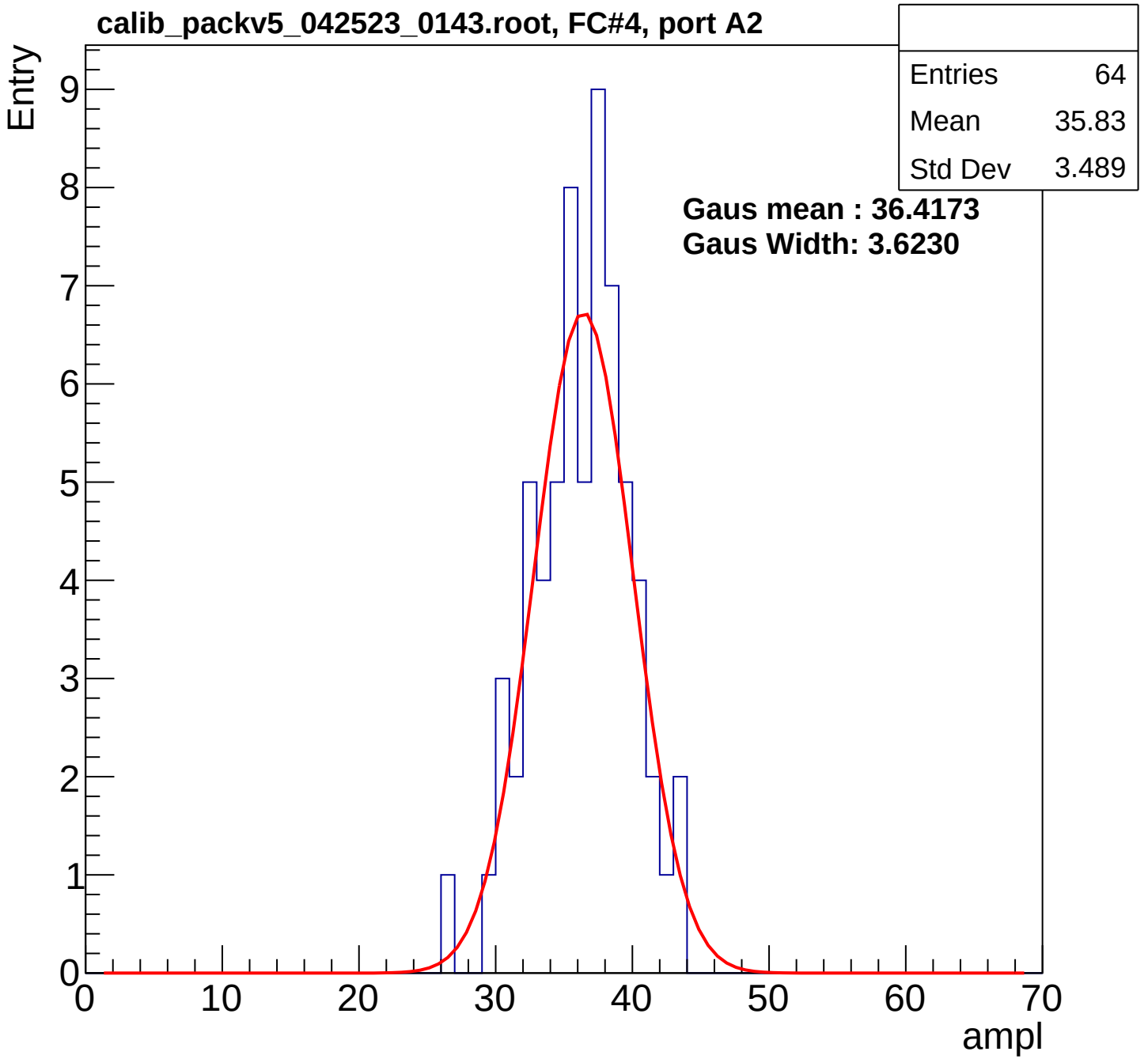

B1L100S, U18-ch13, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 37
Mean 56.16
Std Dev 2.973
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

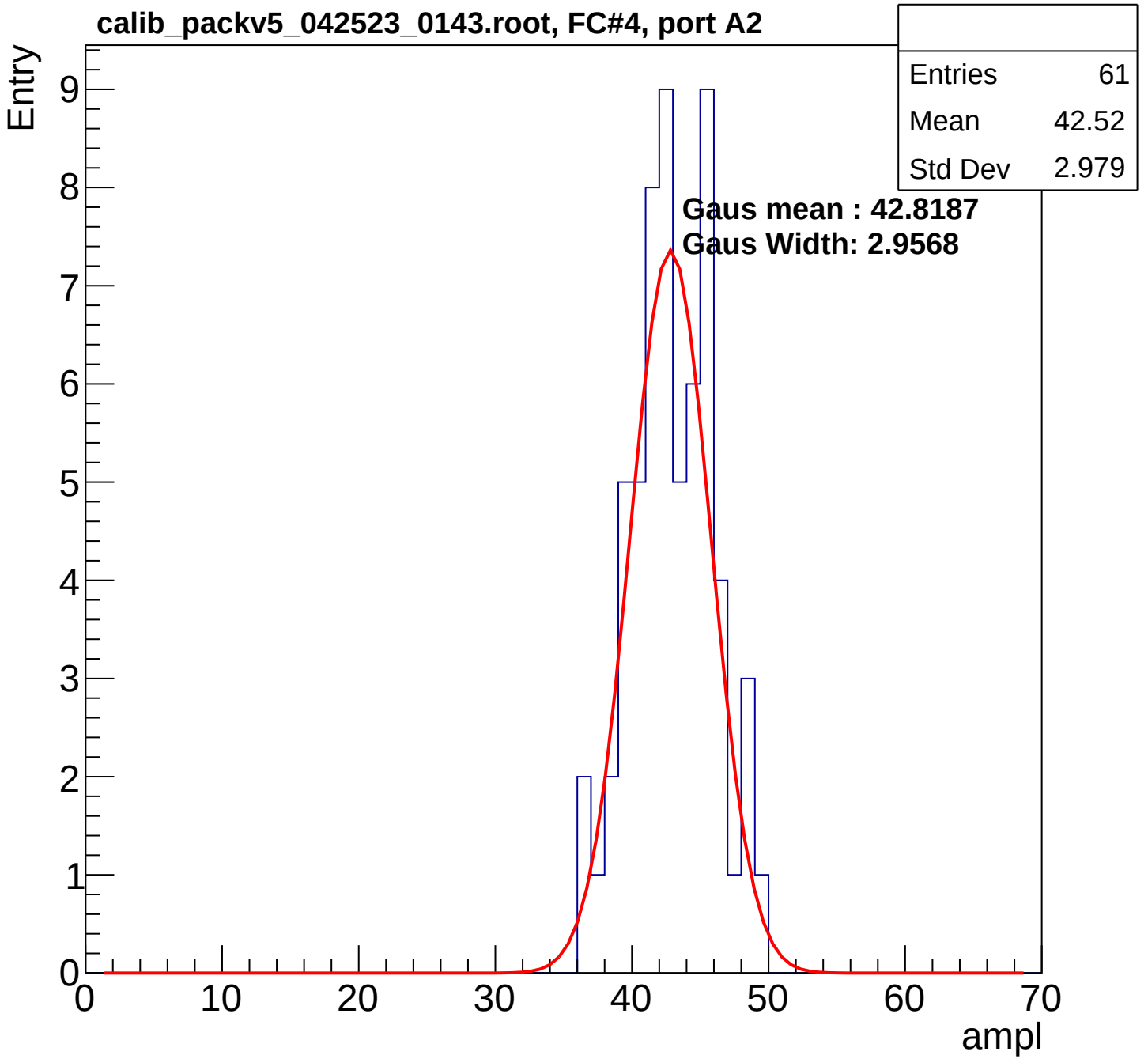

B1L100S, U18-ch13, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 45
Mean 59.11
Std Dev 9.124
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

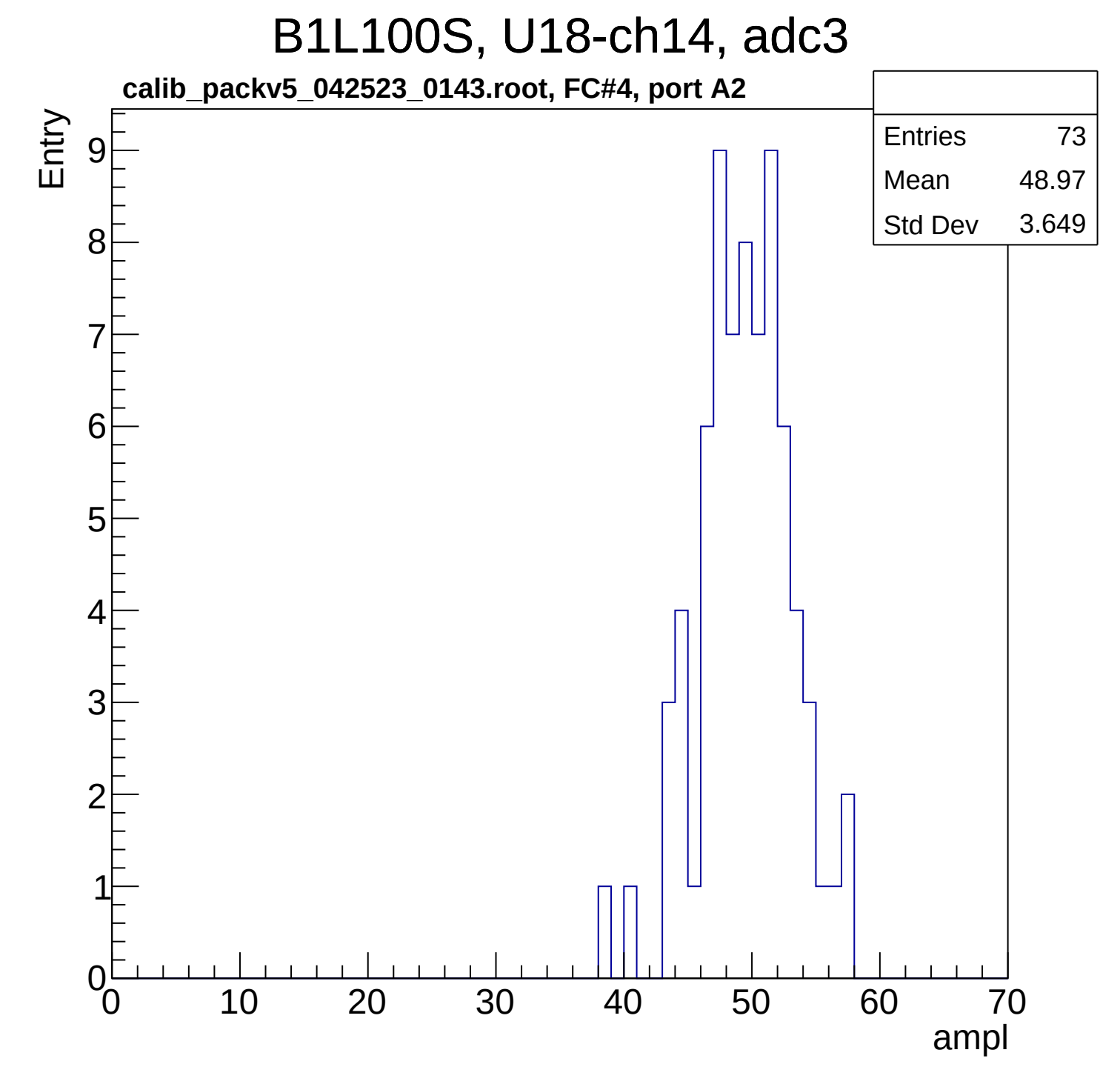

B1L100S, U18-ch13, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 5
Mean 61.8
Std Dev 1.166
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

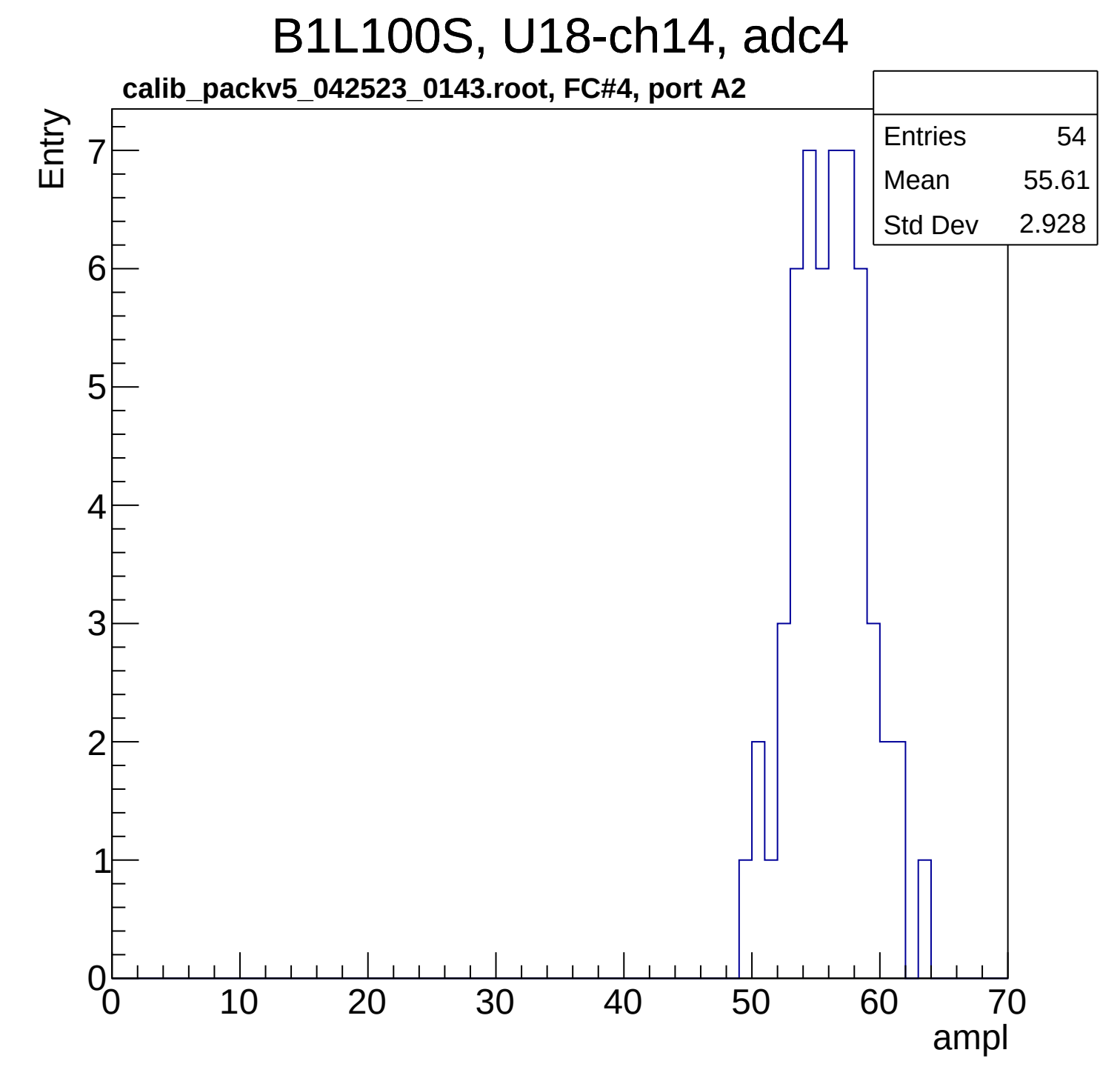

B1L100S, U18-ch13, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

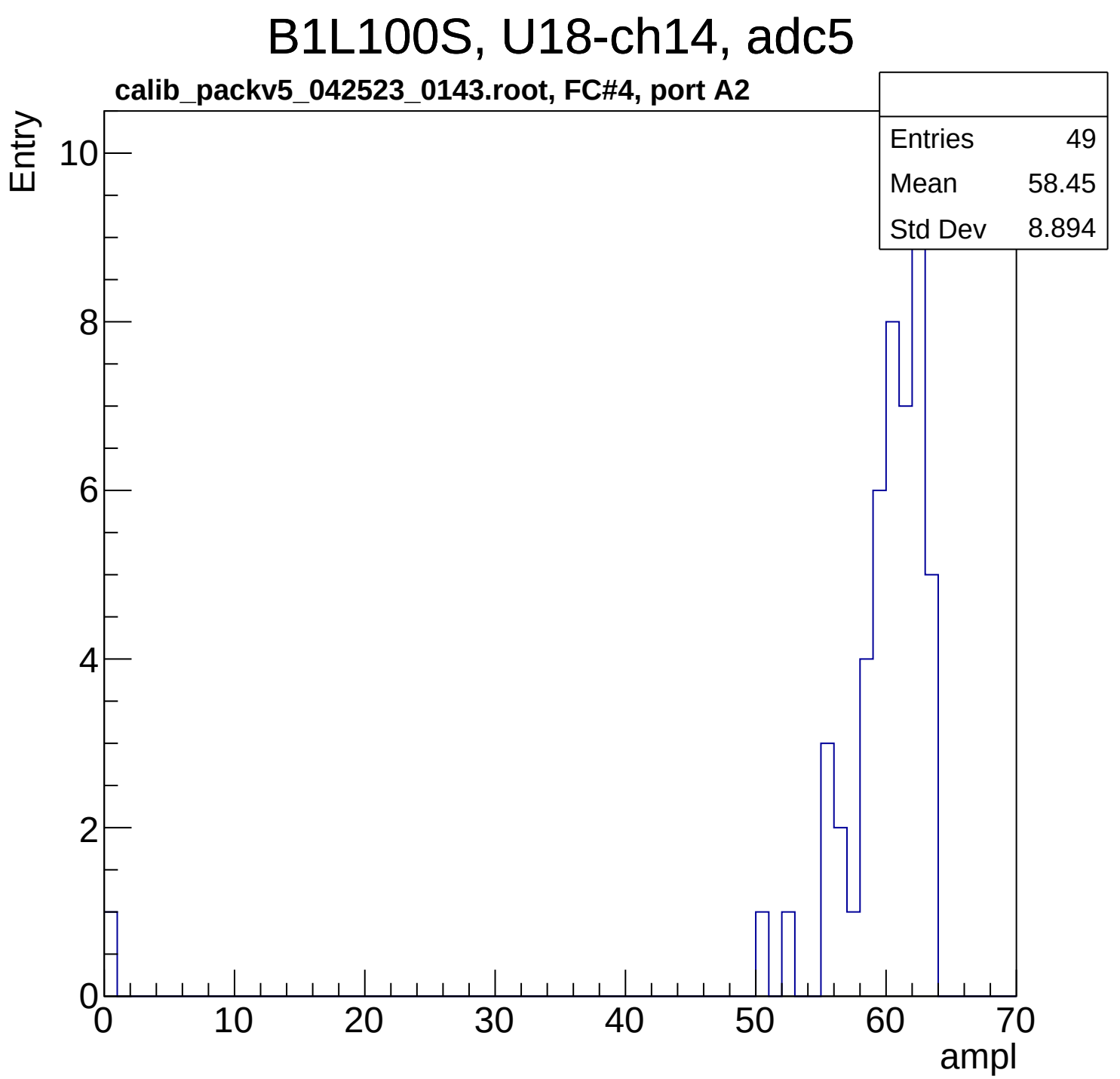

B1L100S, U18-ch14, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 28.95
Std Dev 4.819
Gaus mean : 30.5327
Gaus Width: 3.7143
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

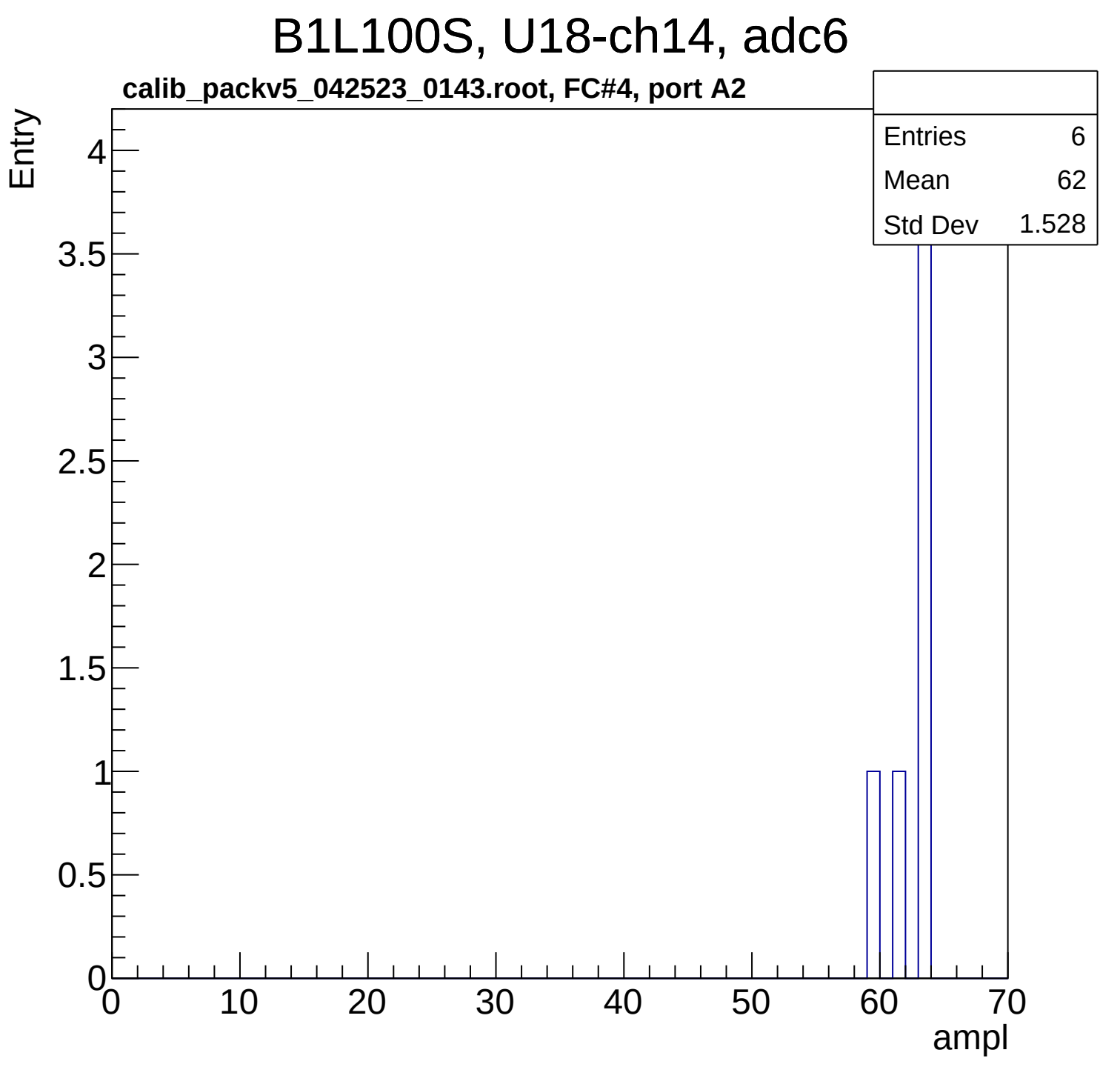

B1L100S, U18-ch14, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 35.83
Std Dev 3.489
Gaus mean : 36.4173
Gaus Width: 3.6230
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

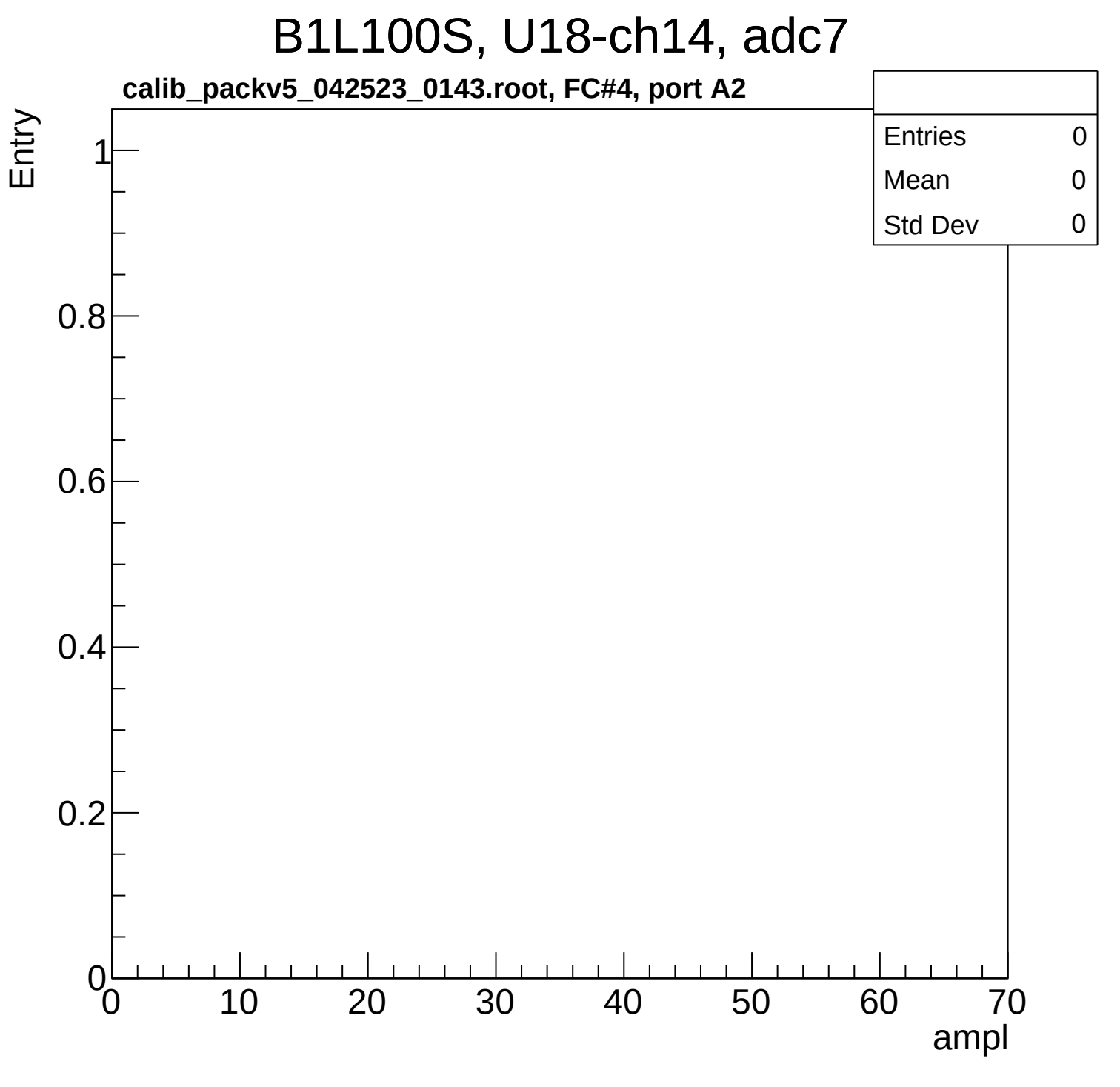

B1L100S, U18-ch14, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 42.52
Std Dev 2.979
Gaus mean : 42.8187
Gaus Width: 2.9568
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

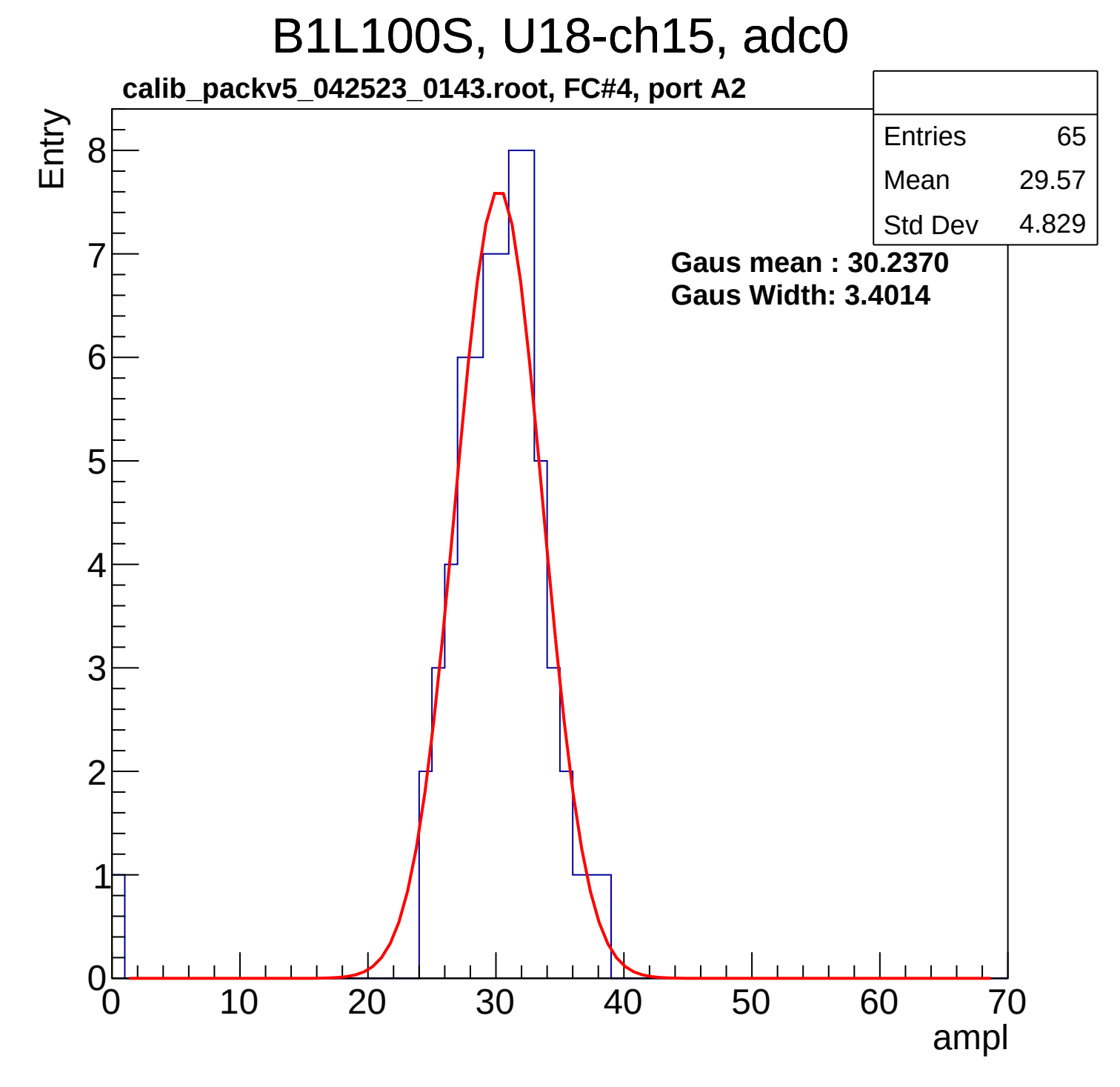

B1L100S, U18-ch14, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 48.97
Std Dev 3.649
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

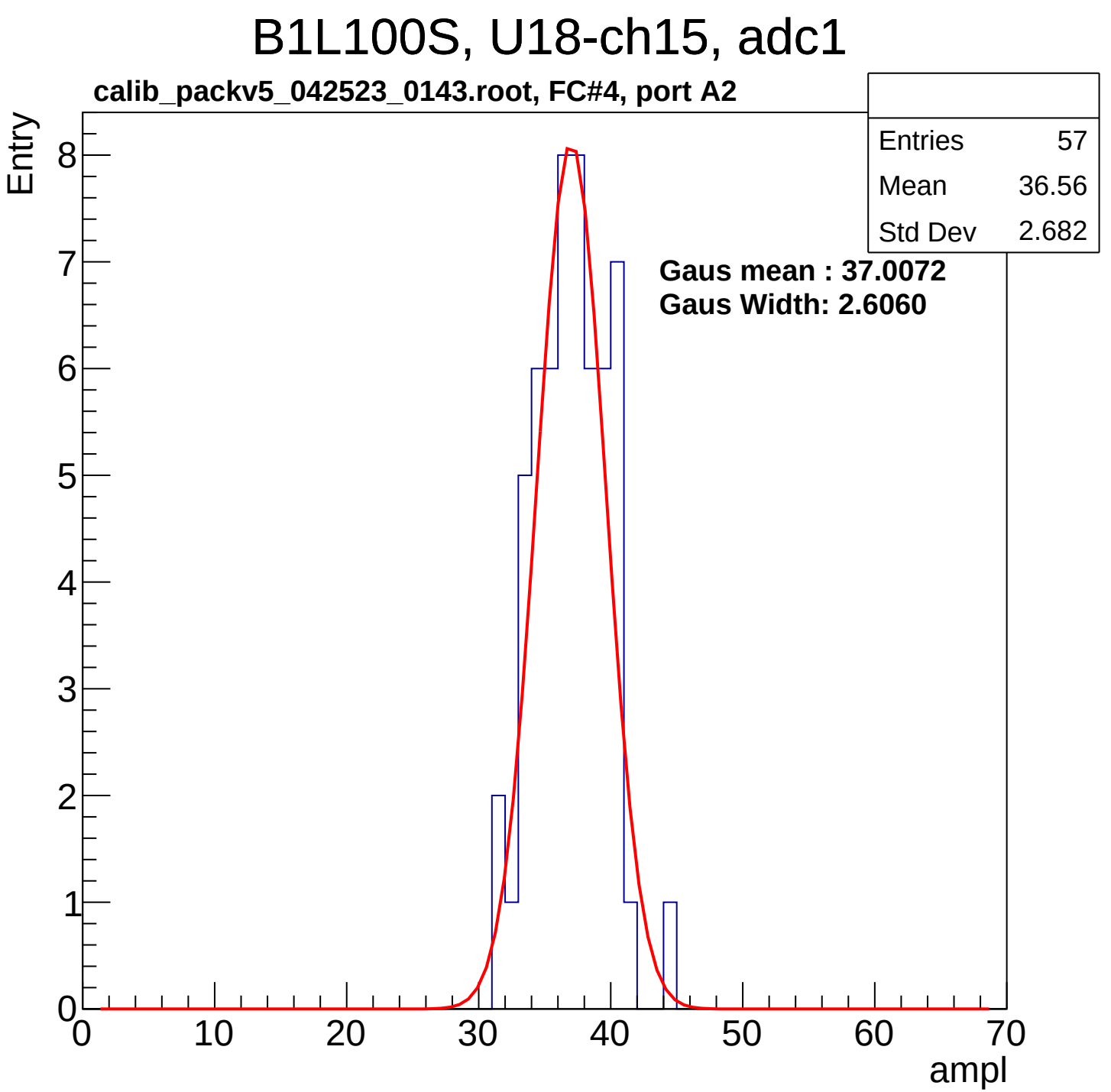

B1L100S, U18-ch14, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 55.61
Std Dev 2.928
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

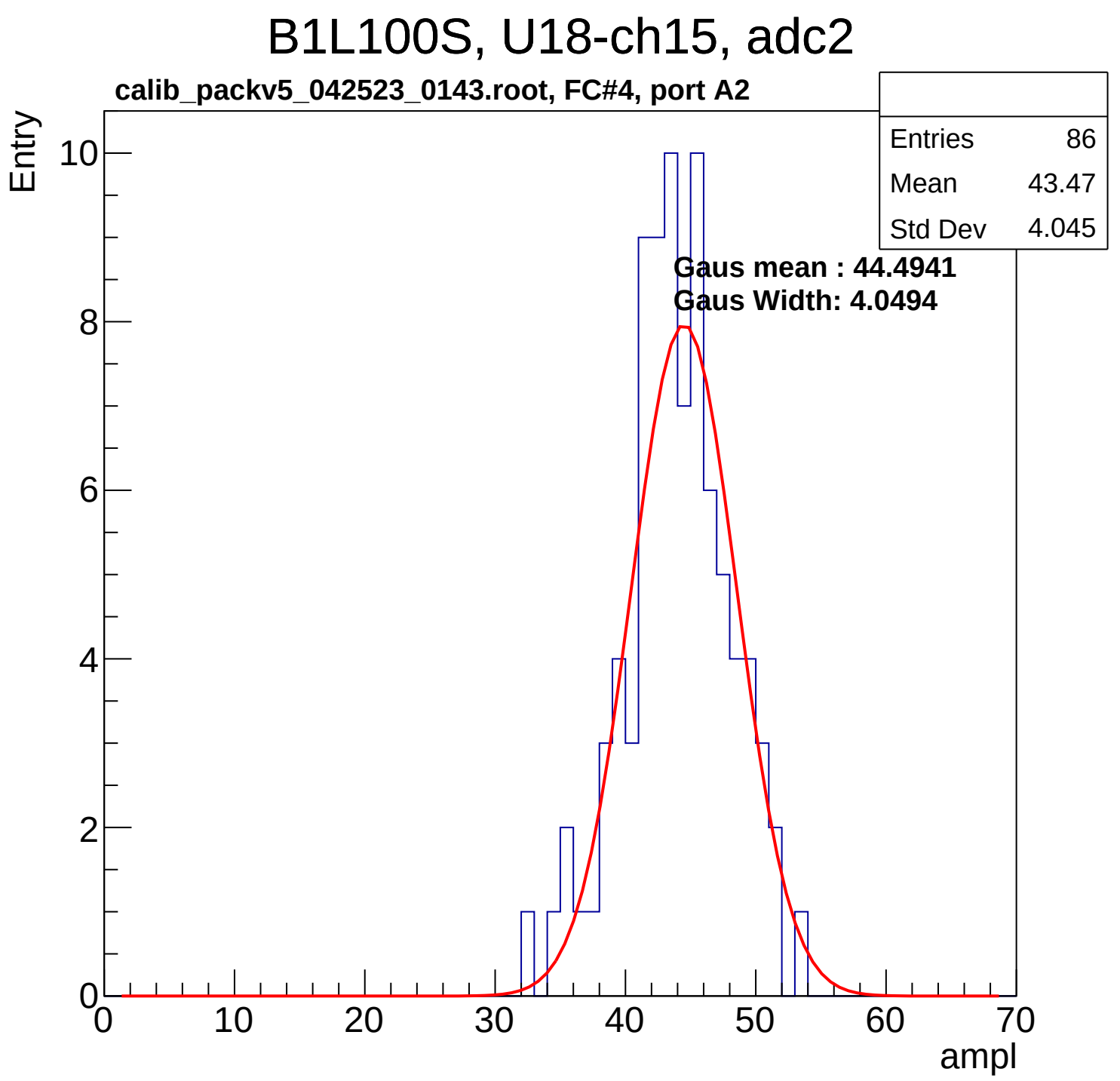

B1L100S, U18-ch14, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 58.45
Std Dev 8.894
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

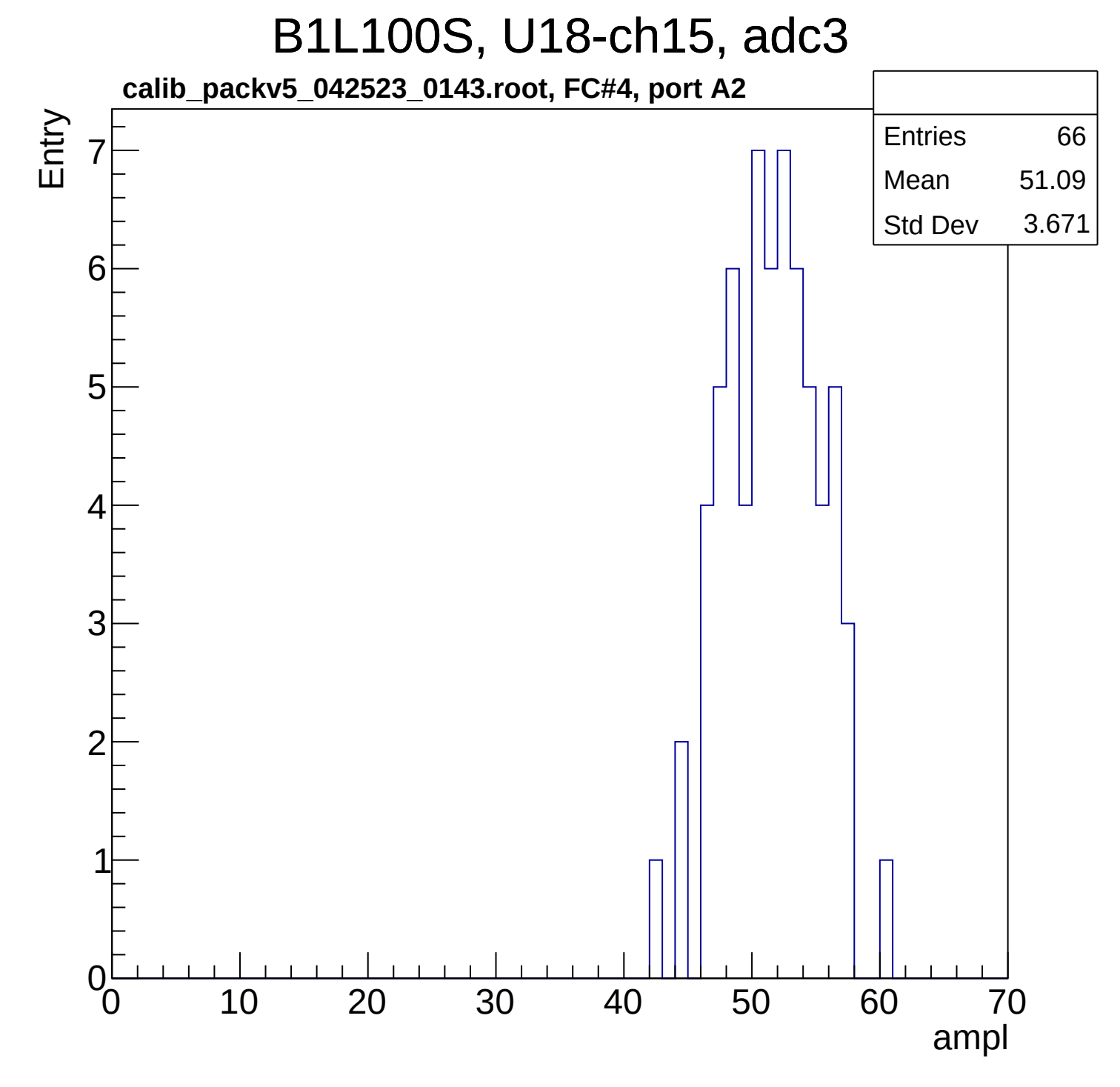

B1L100S, U18-ch14, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 62
Std Dev 1.528
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

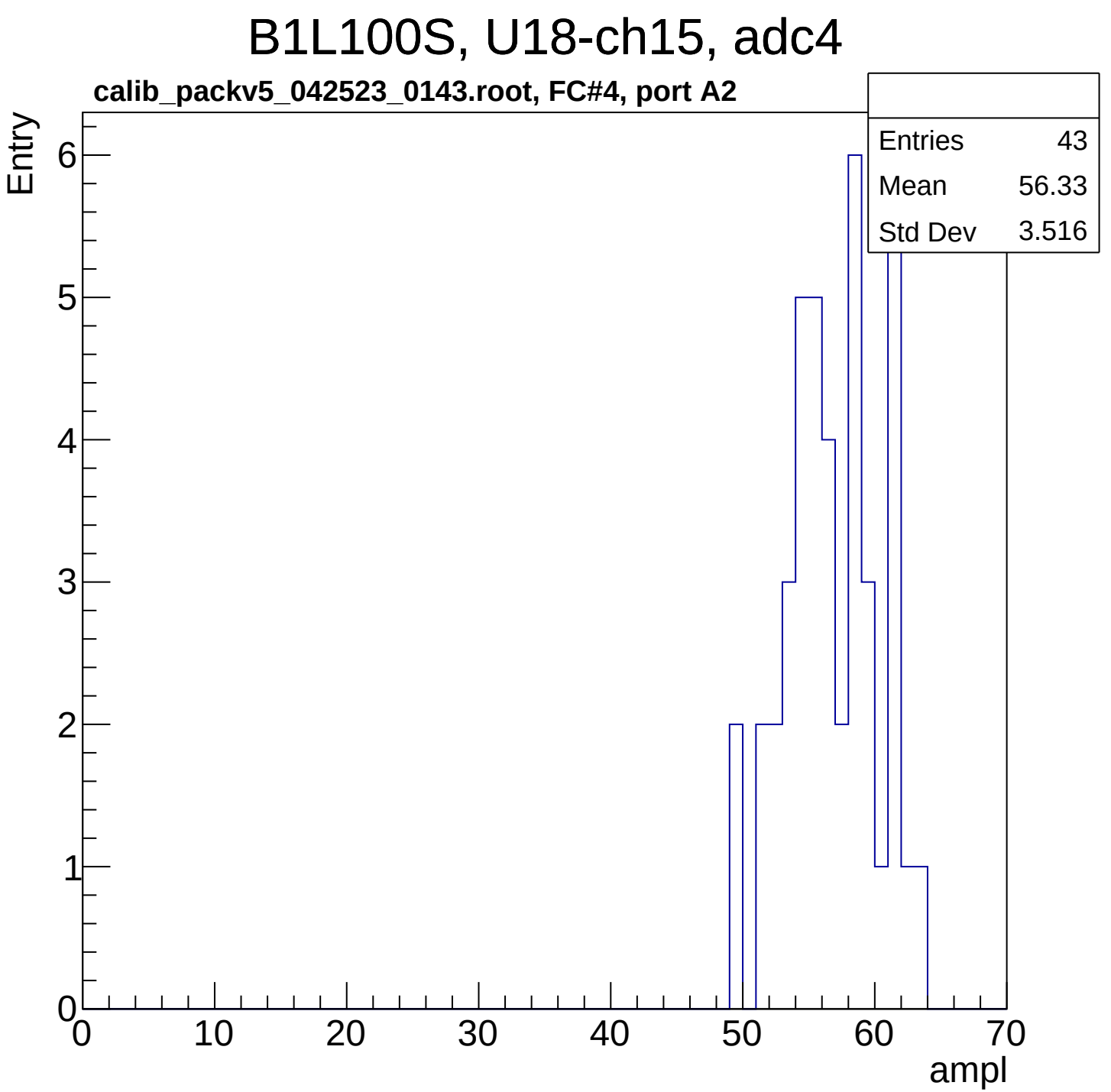

B1L100S, U18-ch14, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

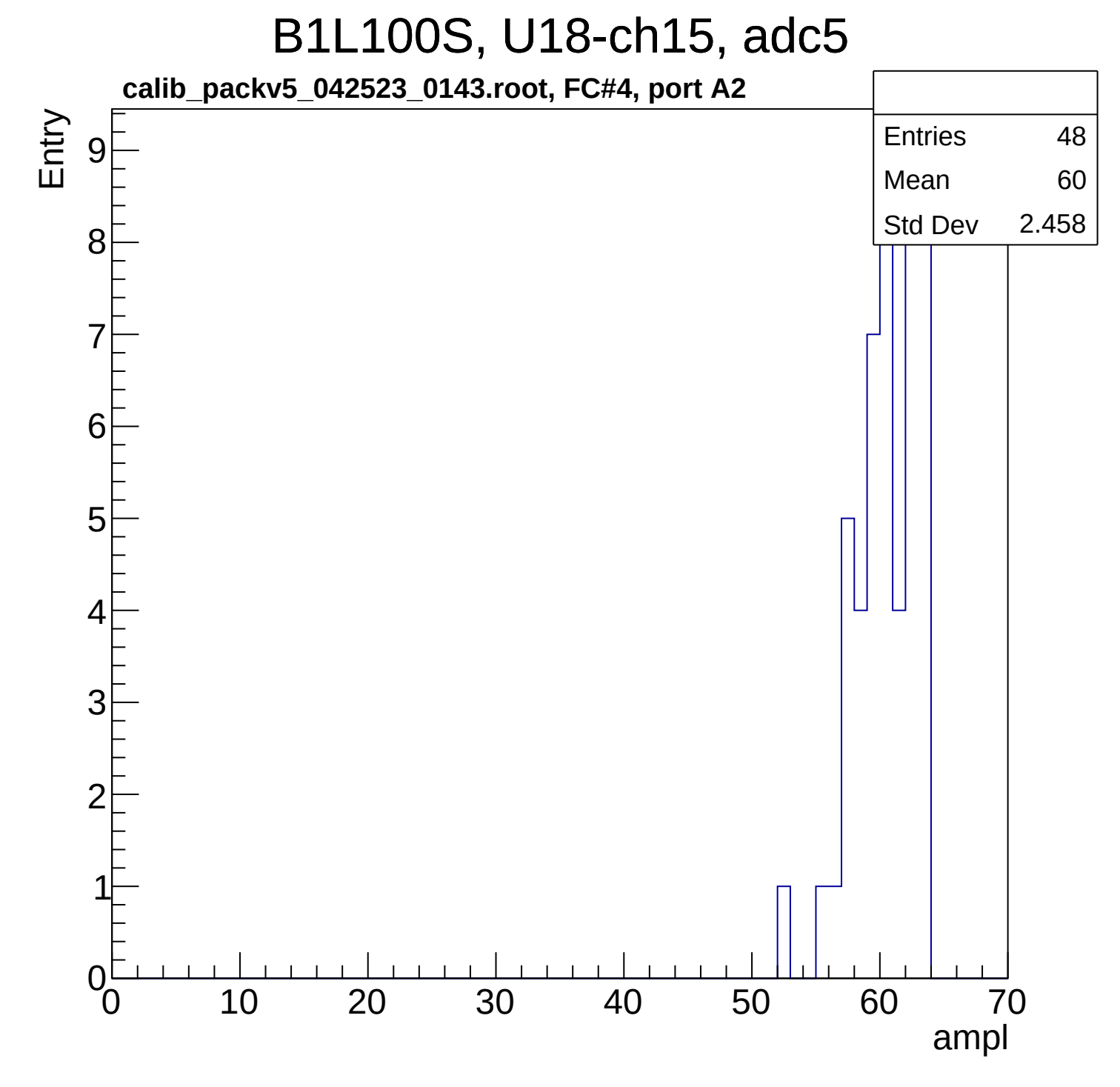

B1L100S, U18-ch15, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 29.57
Std Dev 4.829
Gaus mean : 30.2370
Gaus Width: 3.4014
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

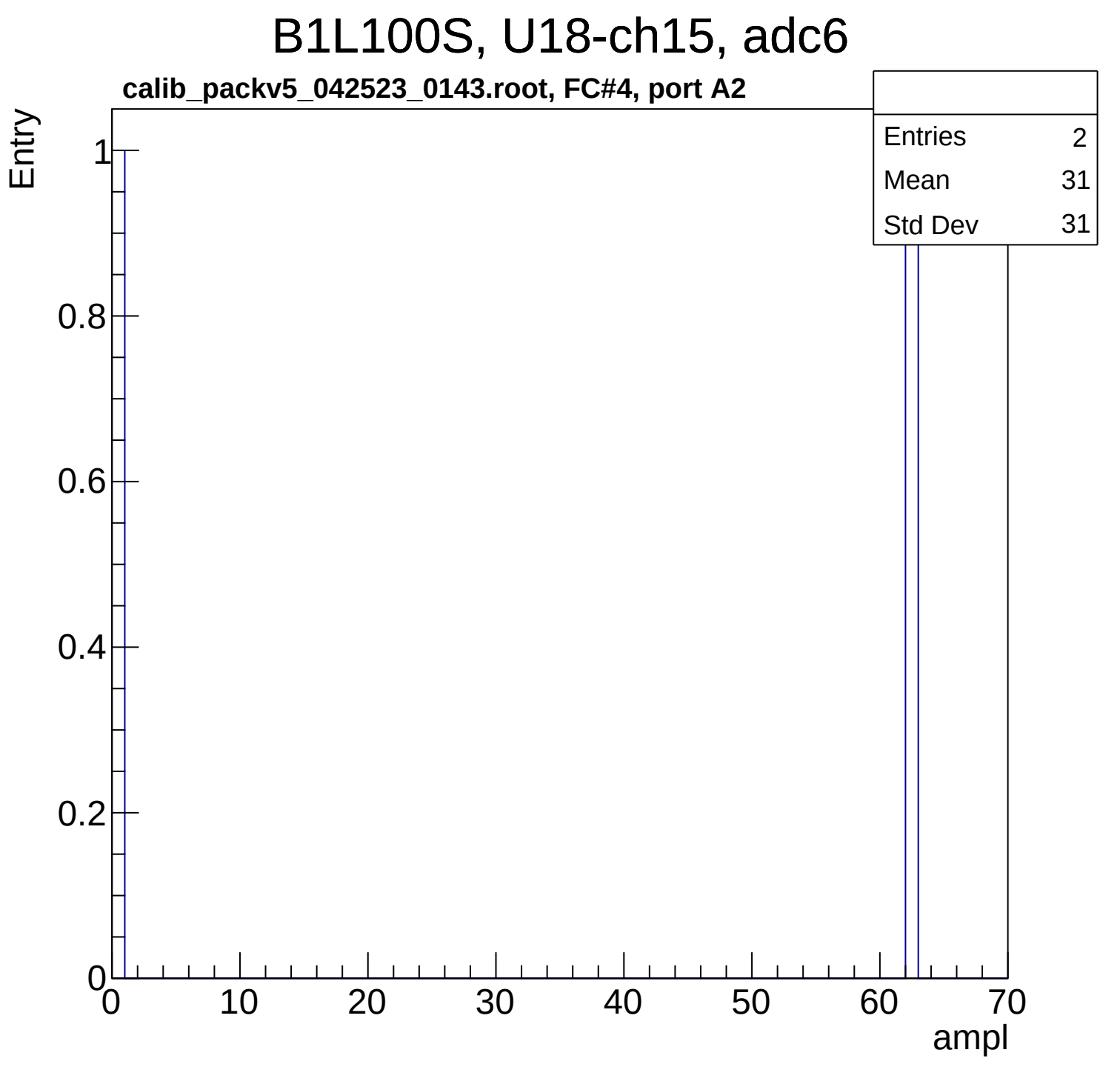

B1L100S, U18-ch15, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 36.56
Std Dev 2.682
Gaus mean : 37.0072
Gaus Width: 2.6060
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

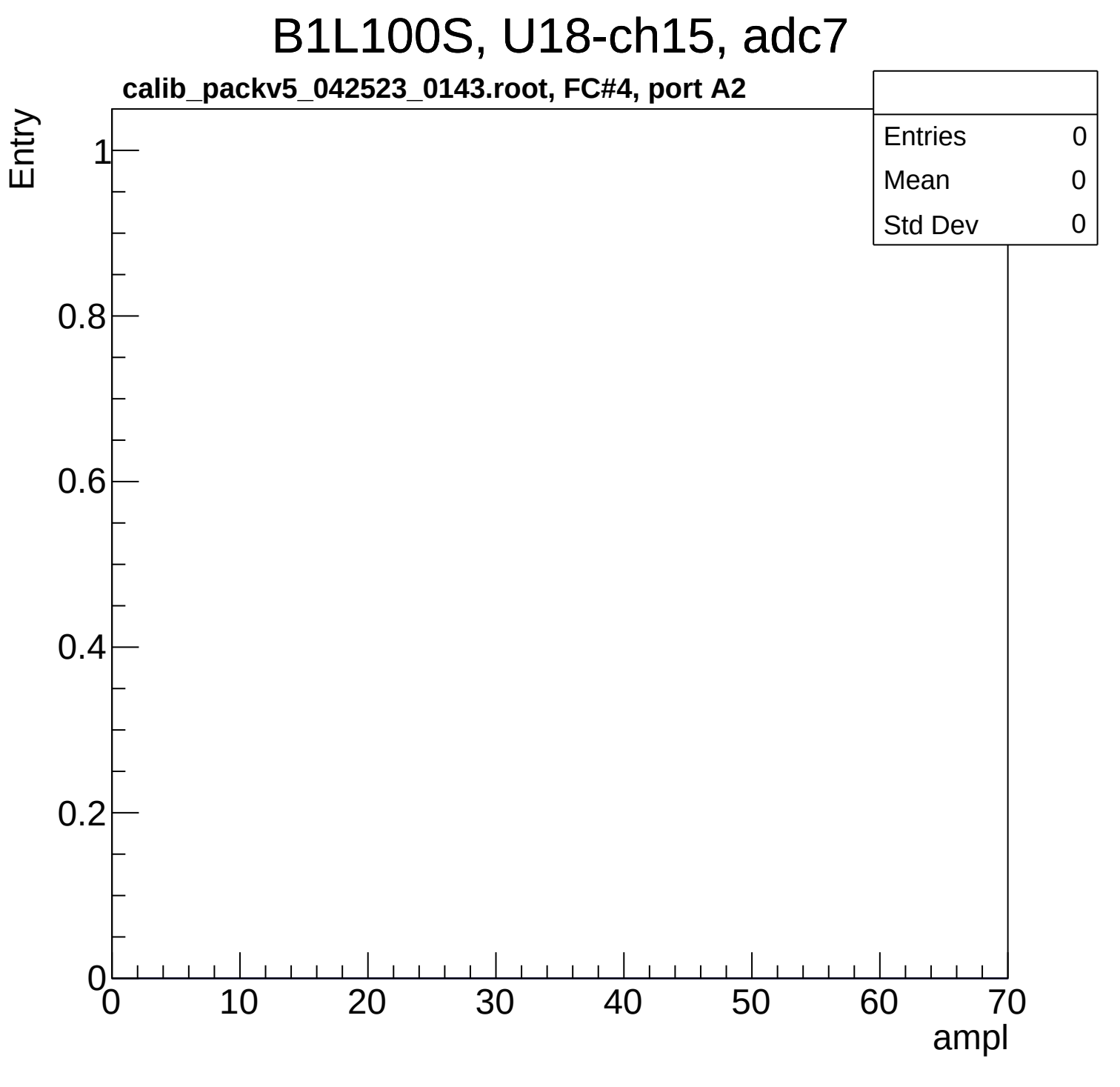

B1L100S, U18-ch15, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 86
Mean 43.47
Std Dev 4.045
Gaus mean : 44.4941
Gaus Width: 4.0494
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

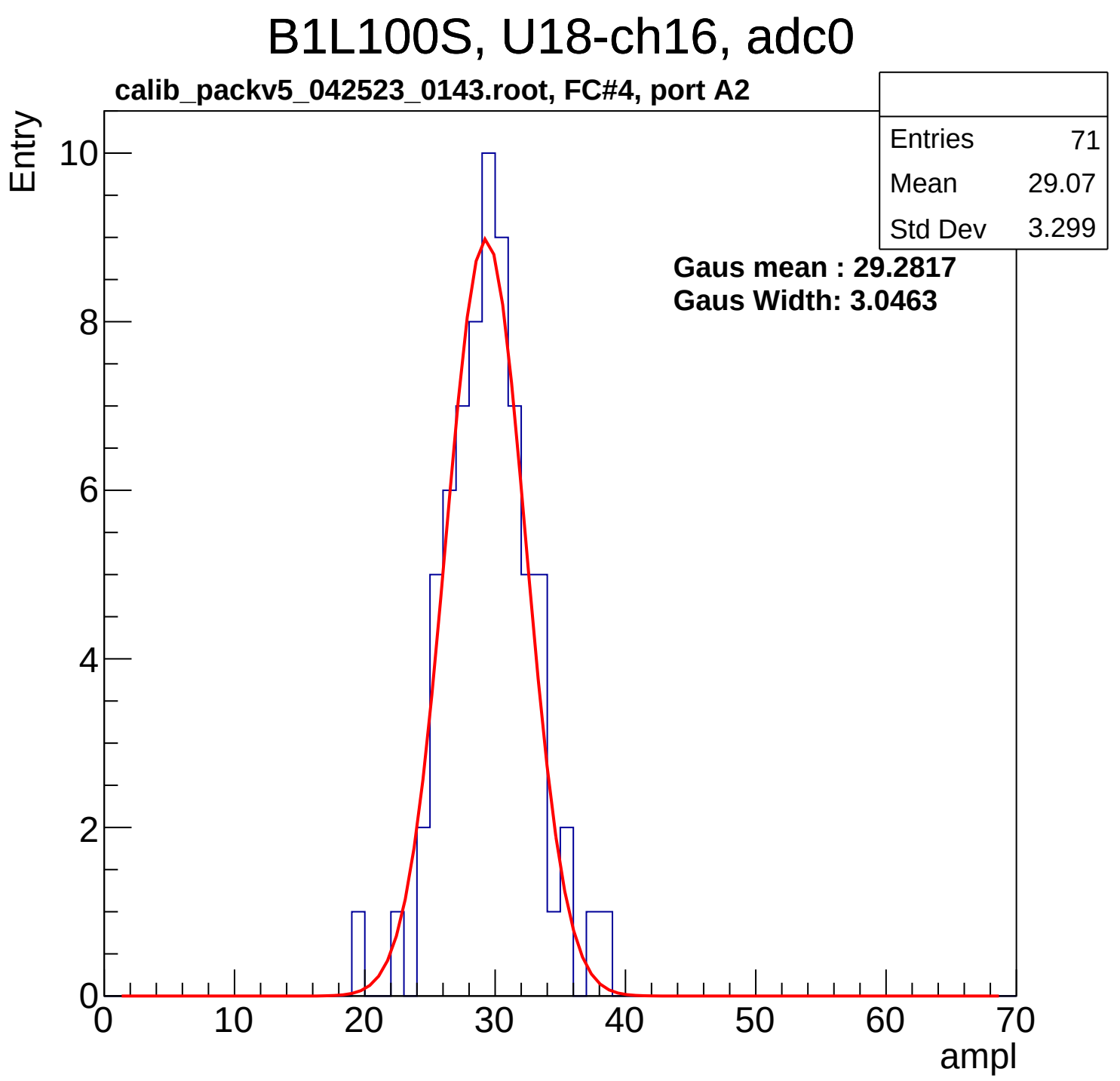

B1L100S, U18-ch15, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 51.09
Std Dev 3.671
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

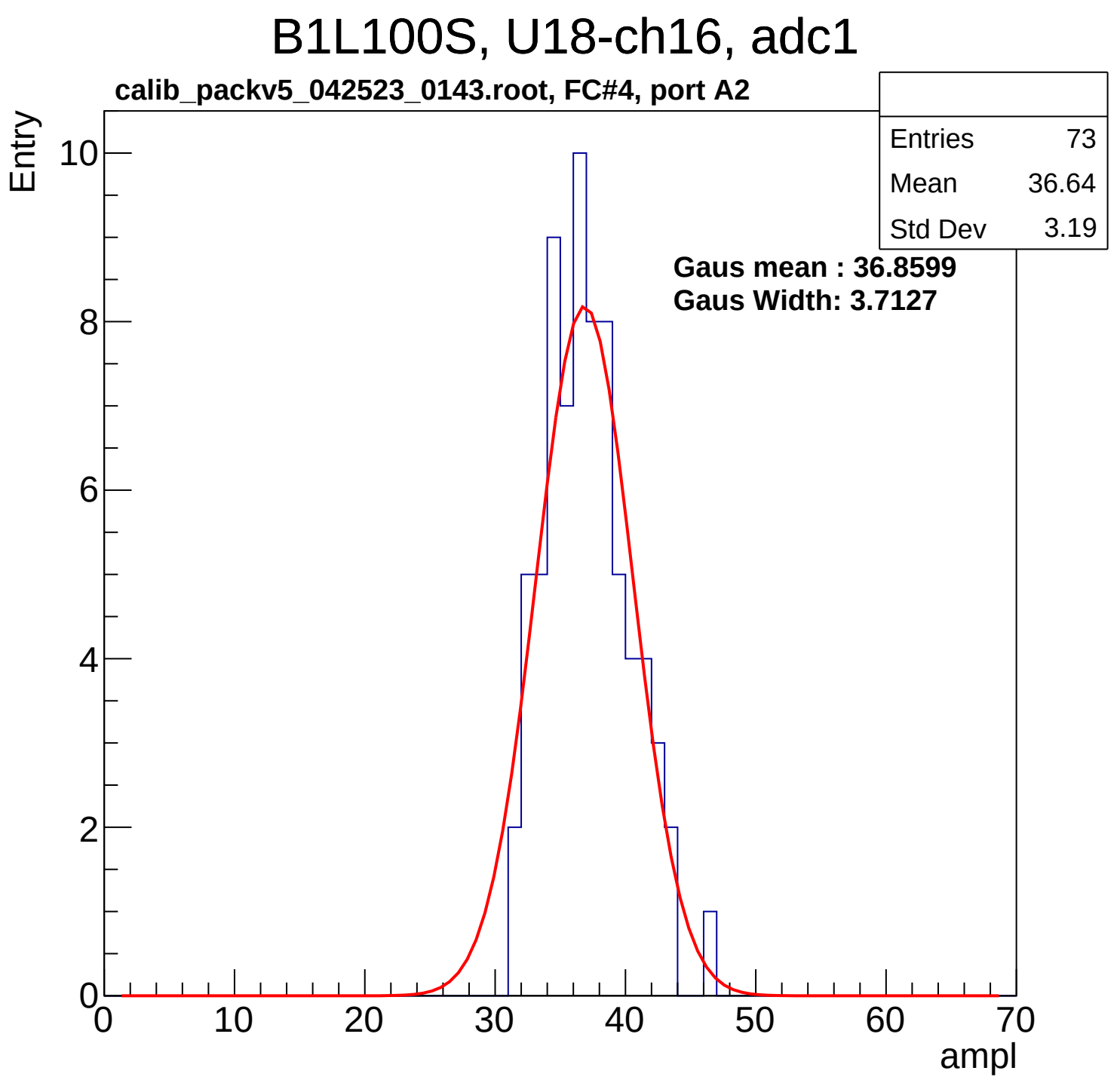

B1L100S, U18-ch15, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 56.33
Std Dev 3.516
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

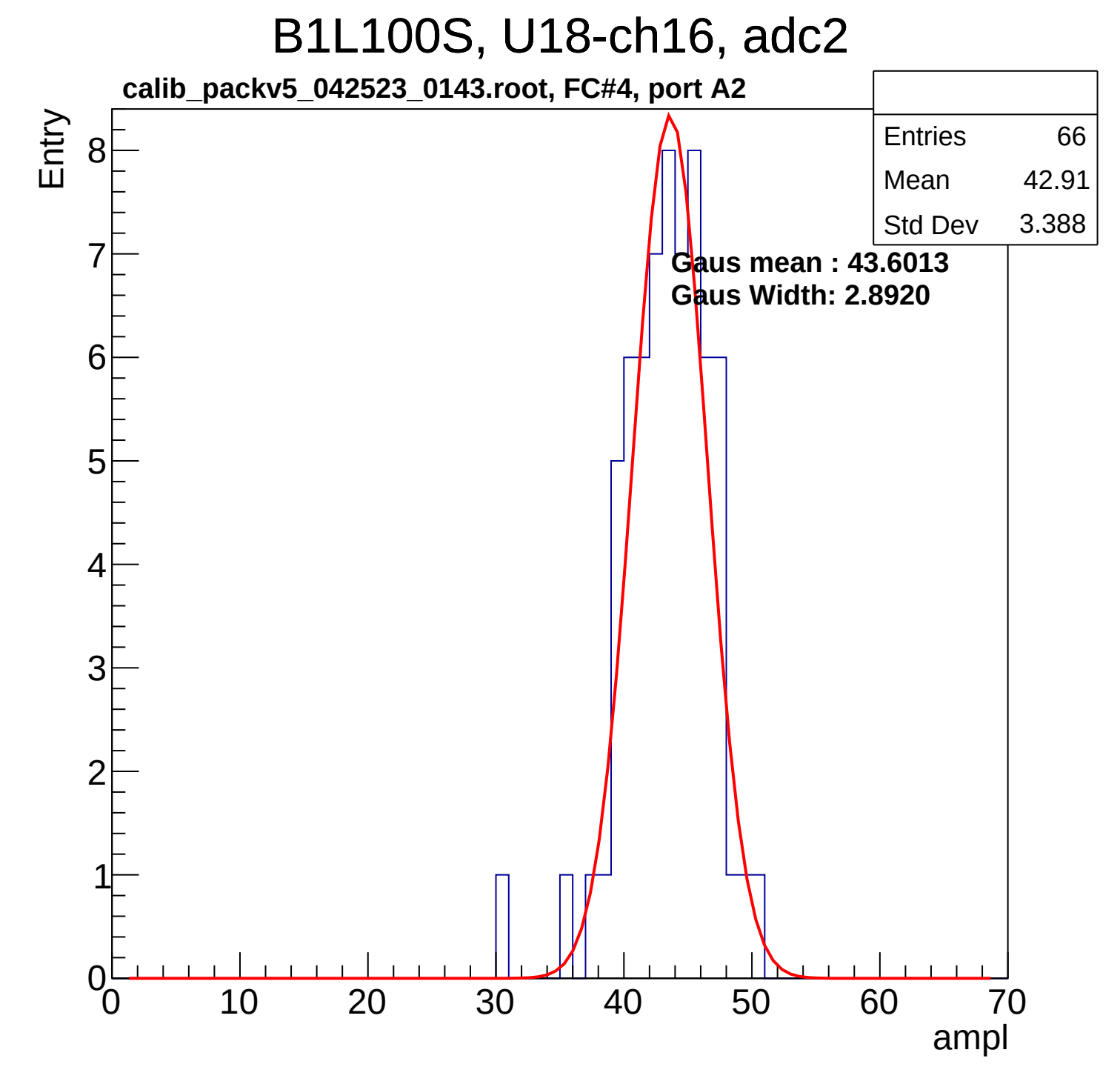

B1L100S, U18-ch15, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 60
Std Dev 2.458
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

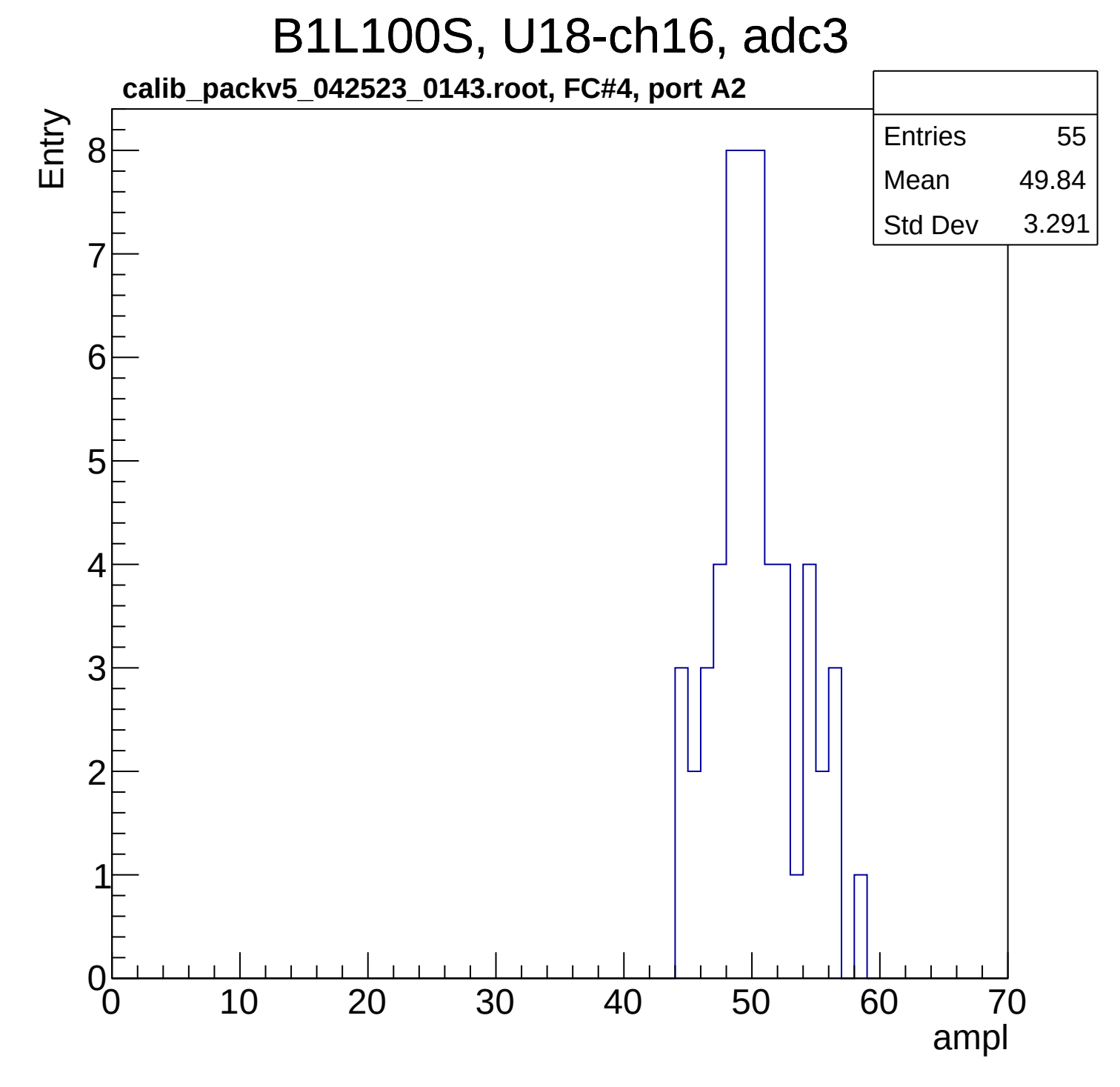

B1L100S, U18-ch15, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 31
Std Dev 31
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

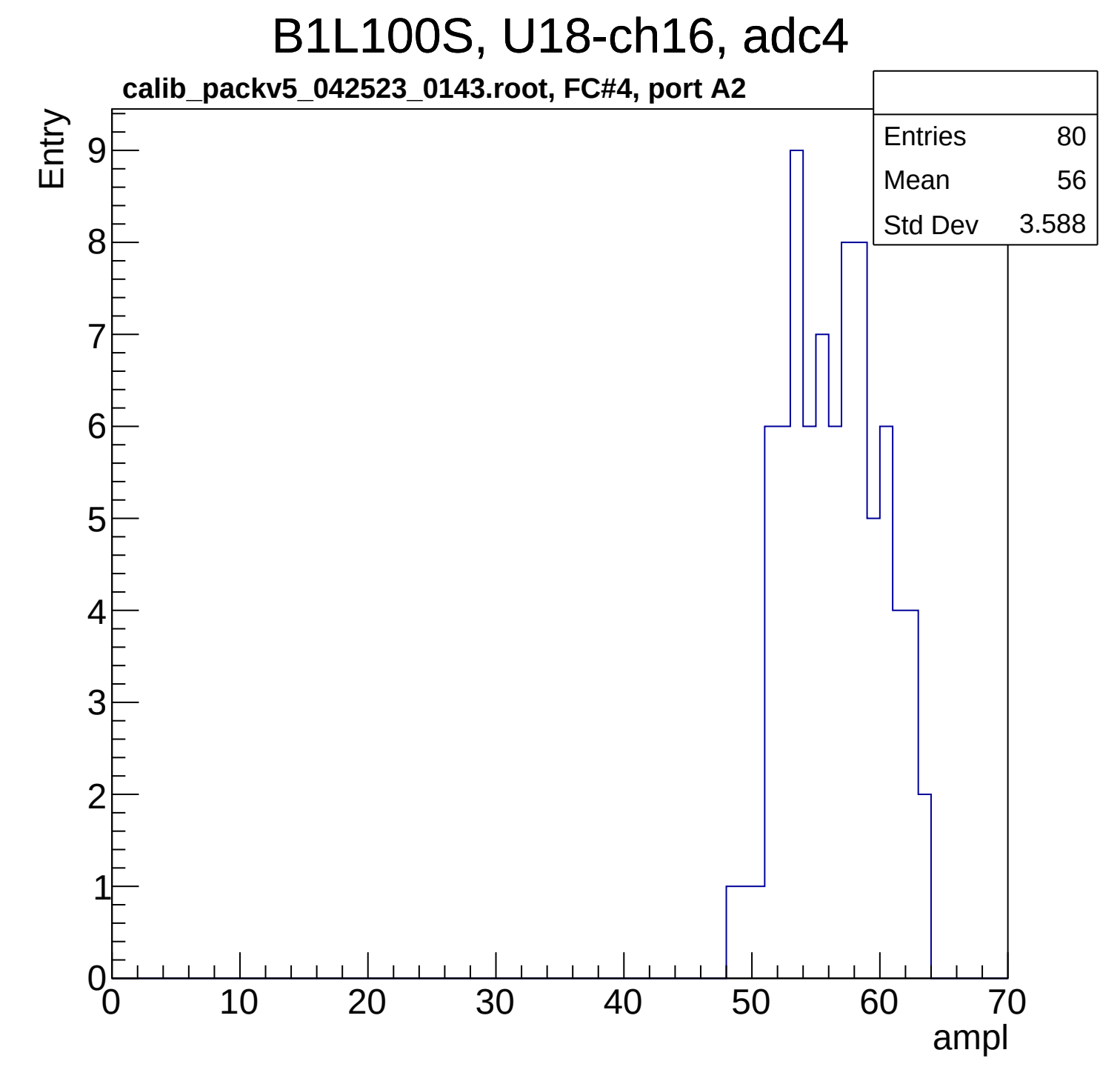

B1L100S, U18-ch15, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

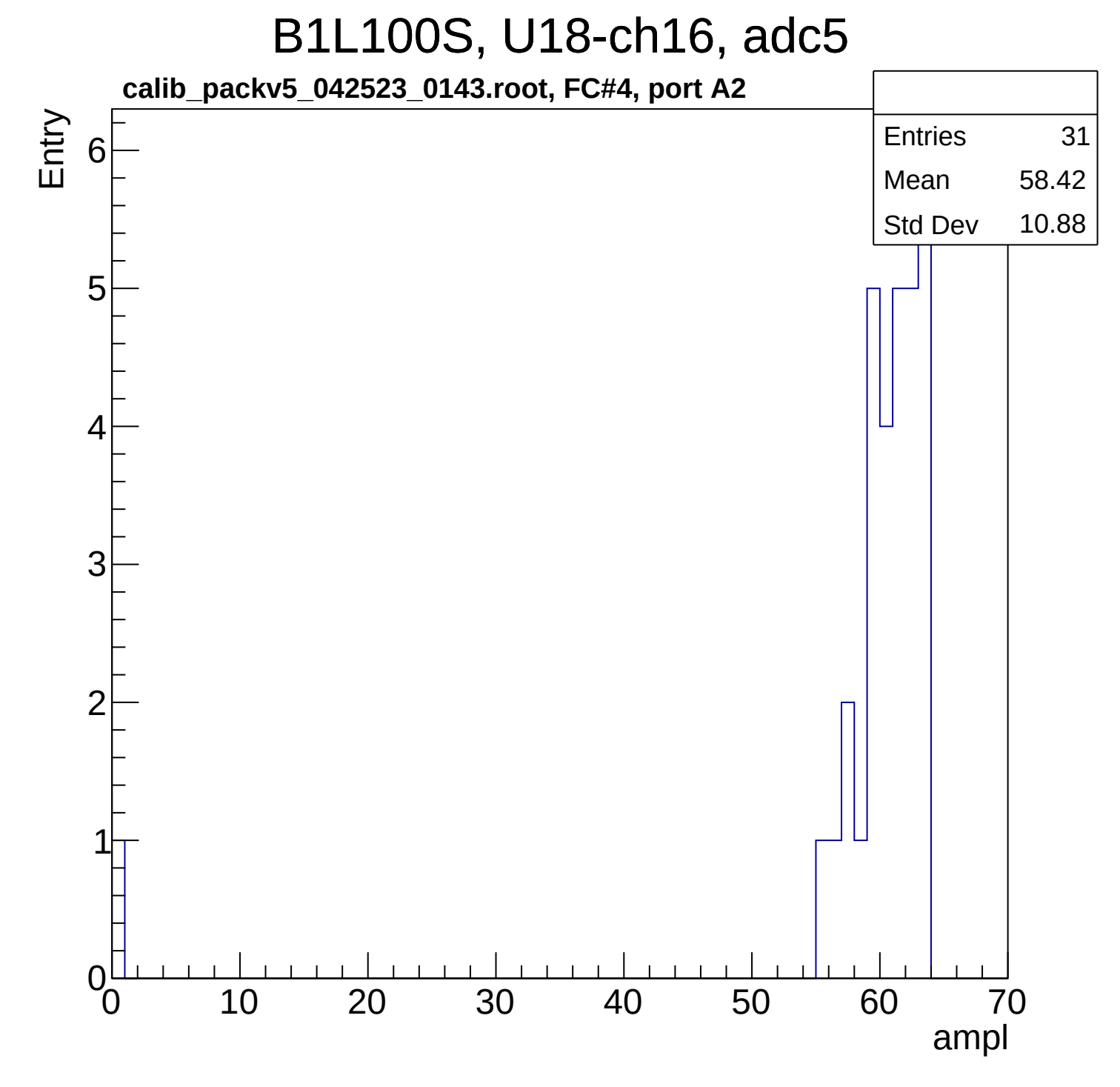

B1L100S, U18-ch16, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 29.07
Std Dev 3.299
Gaus mean : 29.2817
Gaus Width: 3.0463
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

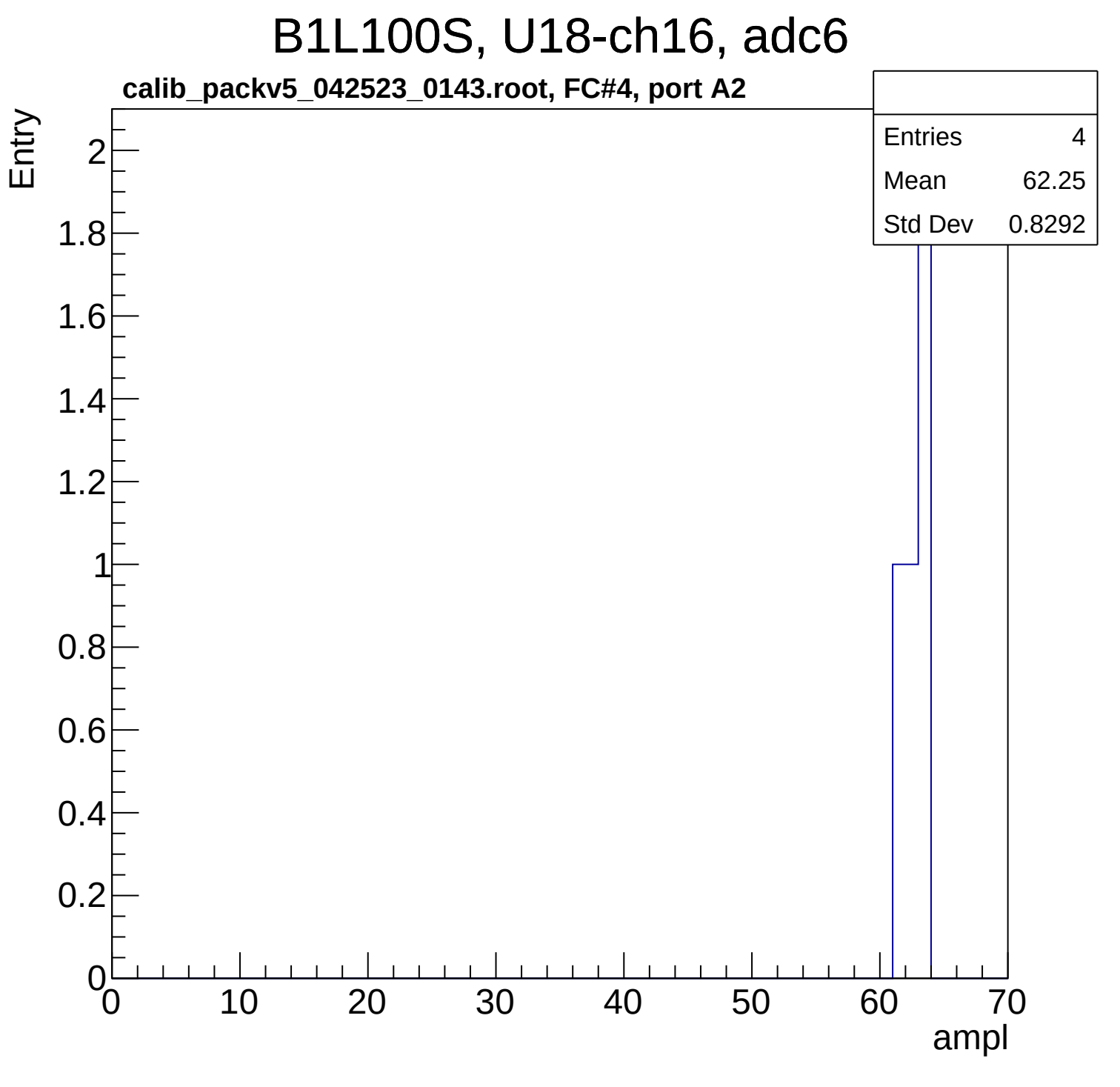

B1L100S, U18-ch16, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 36.64
Std Dev 3.19
Gaus mean : 36.8599
Gaus Width: 3.7127
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

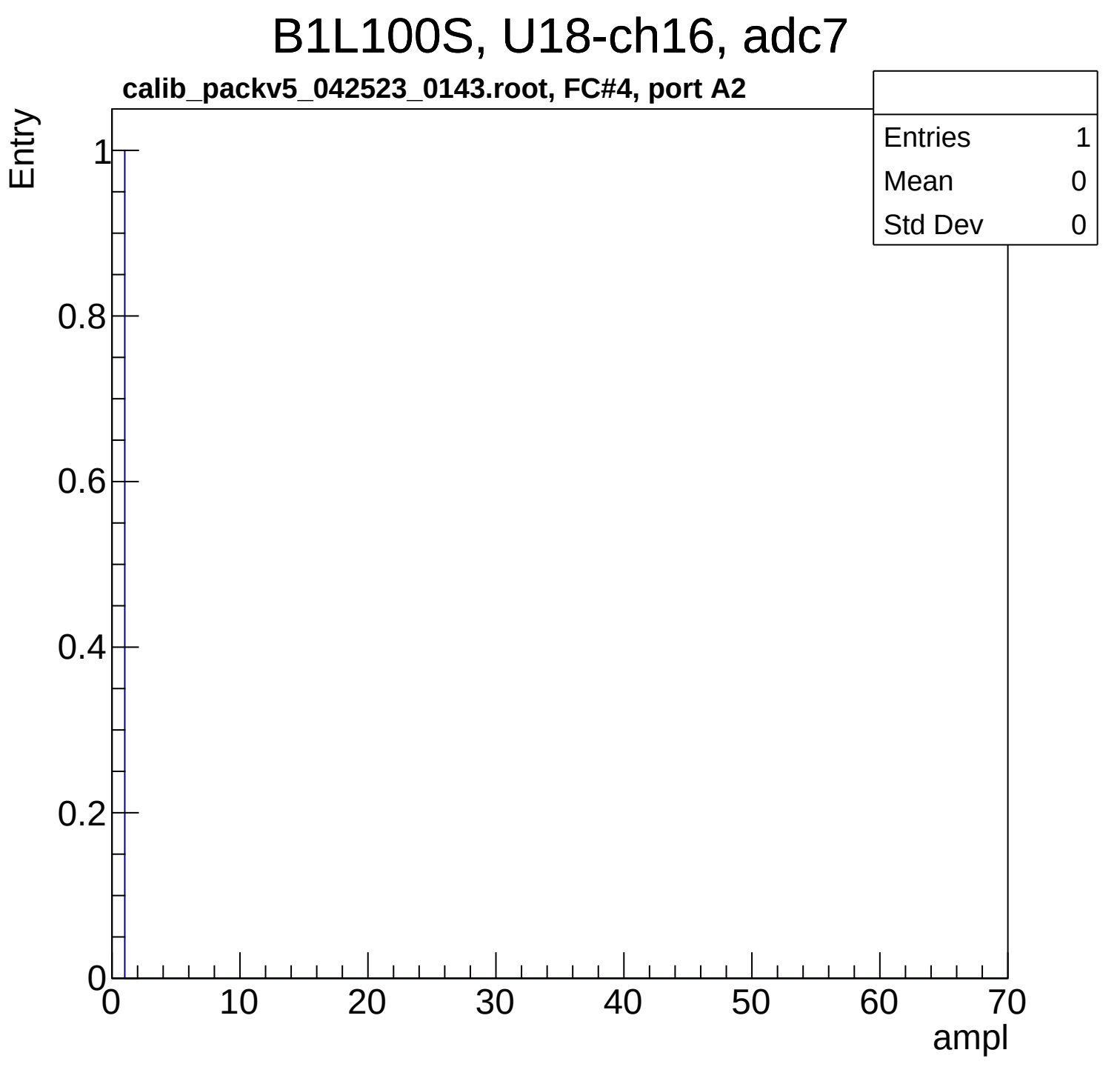

B1L100S, U18-ch16, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 42.91
Std Dev 3.388
Gaus mean : 43.6013
Gaus Width: 2.8920
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

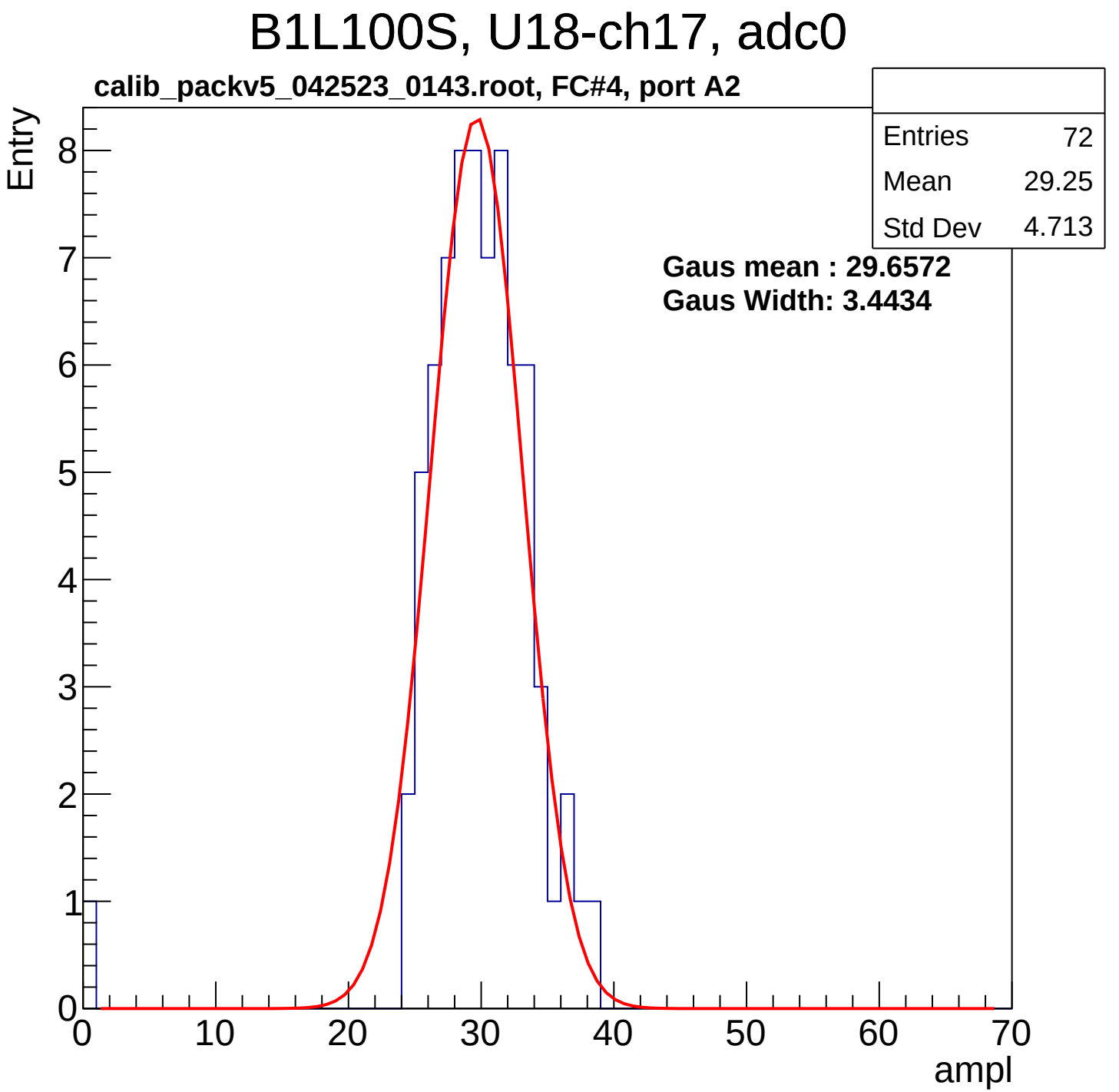

B1L100S, U18-ch16, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 49.84
Std Dev 3.291
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

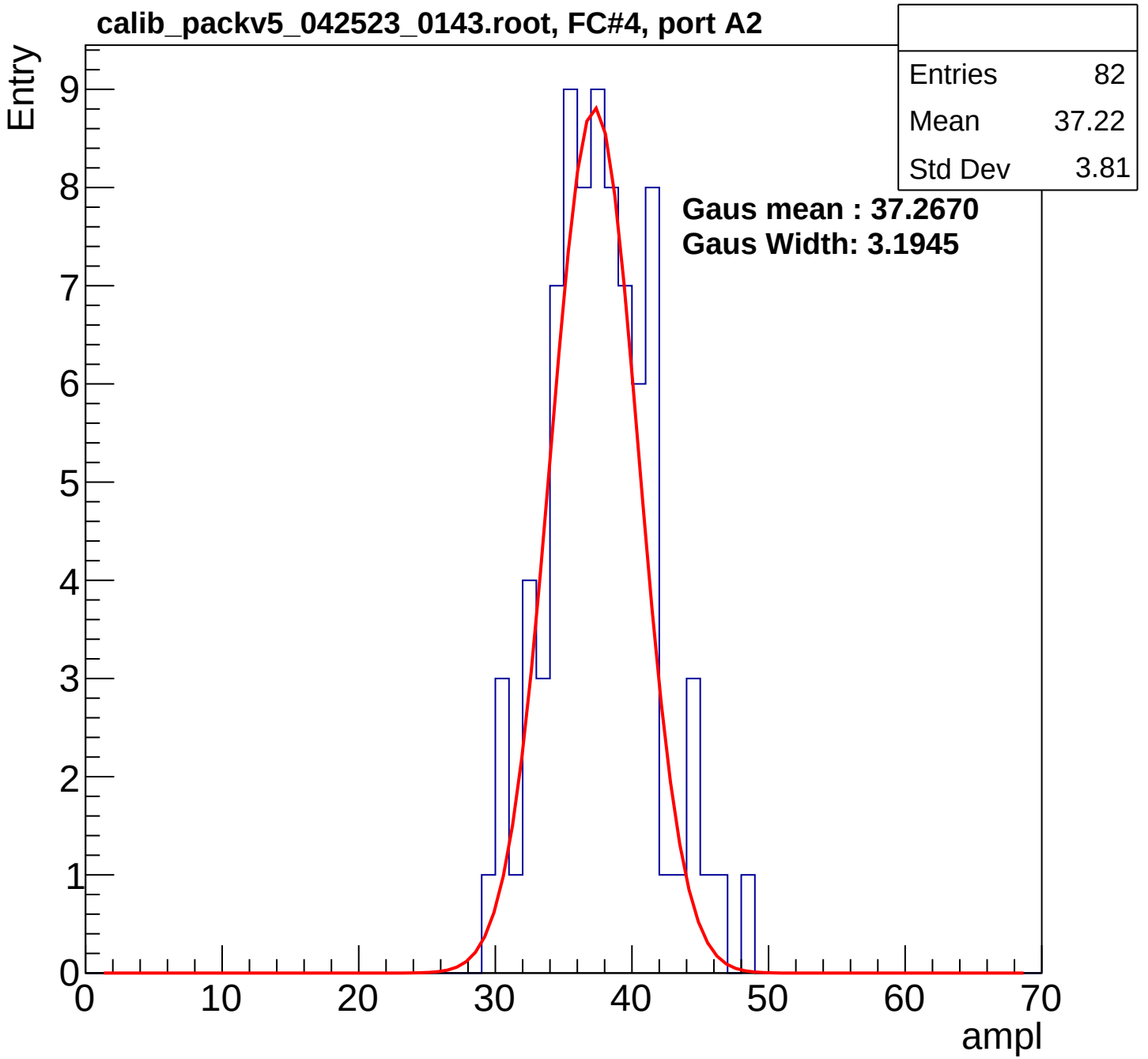

B1L100S, U18-ch16, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 56
Std Dev 3.588
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

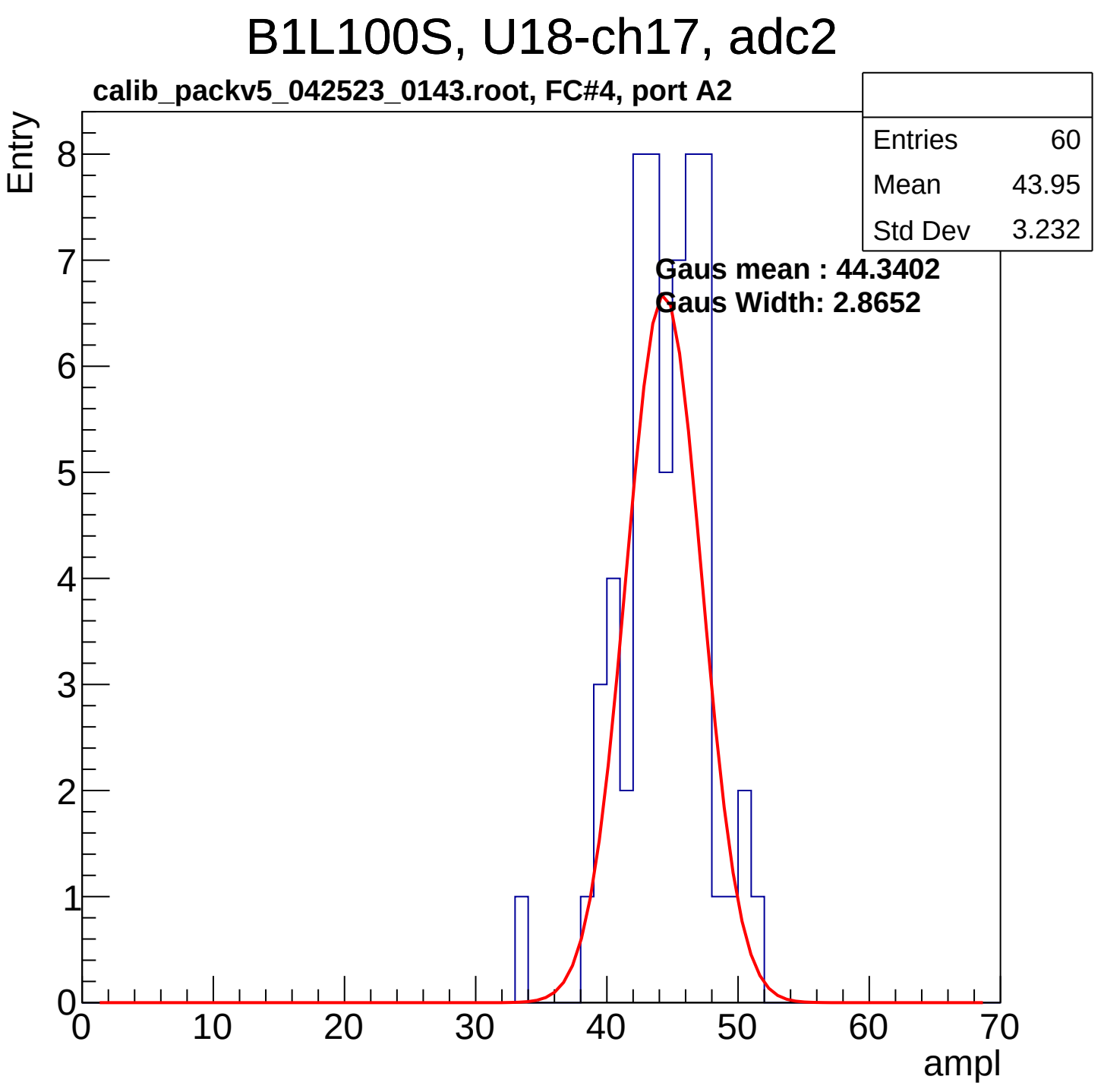

B1L100S, U18-ch16, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 31
Mean 58.42
Std Dev 10.88
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

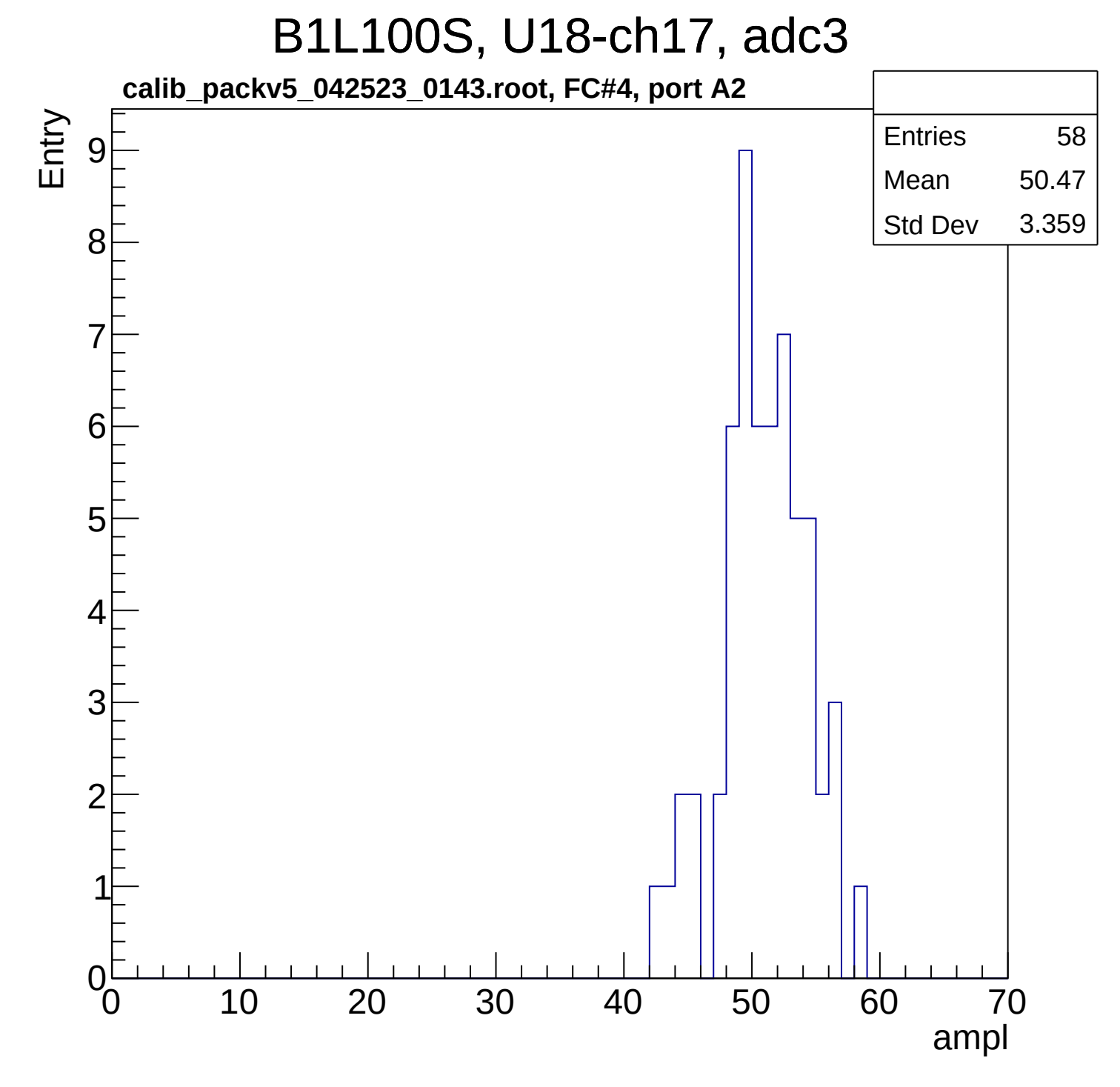

B1L100S, U18-ch16, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

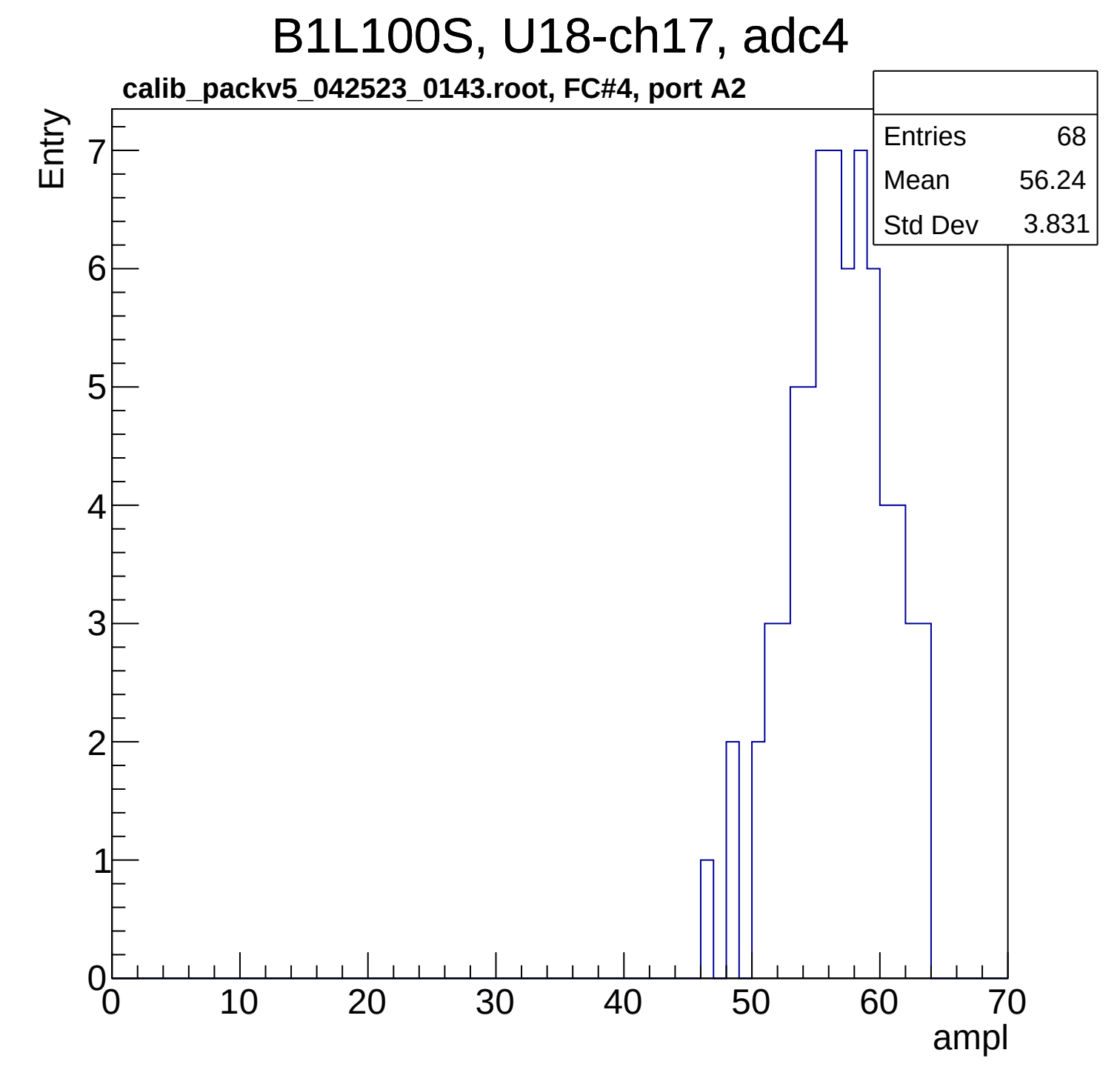

B1L100S, U18-ch16, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

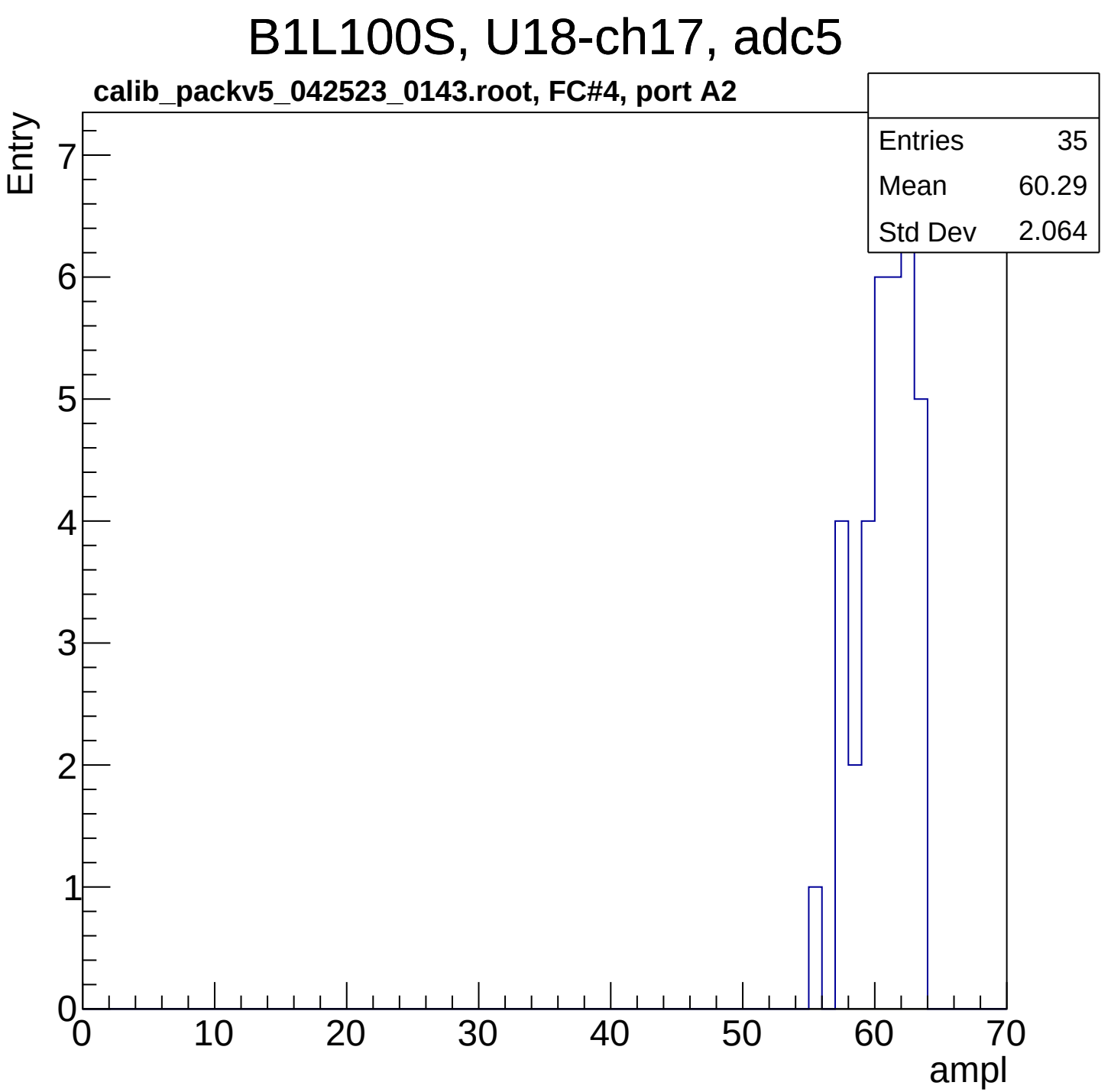

B1L100S, U18-ch17, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 29.25
Std Dev 4.713
Gaus mean : 29.6572
Gaus Width: 3.4434
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

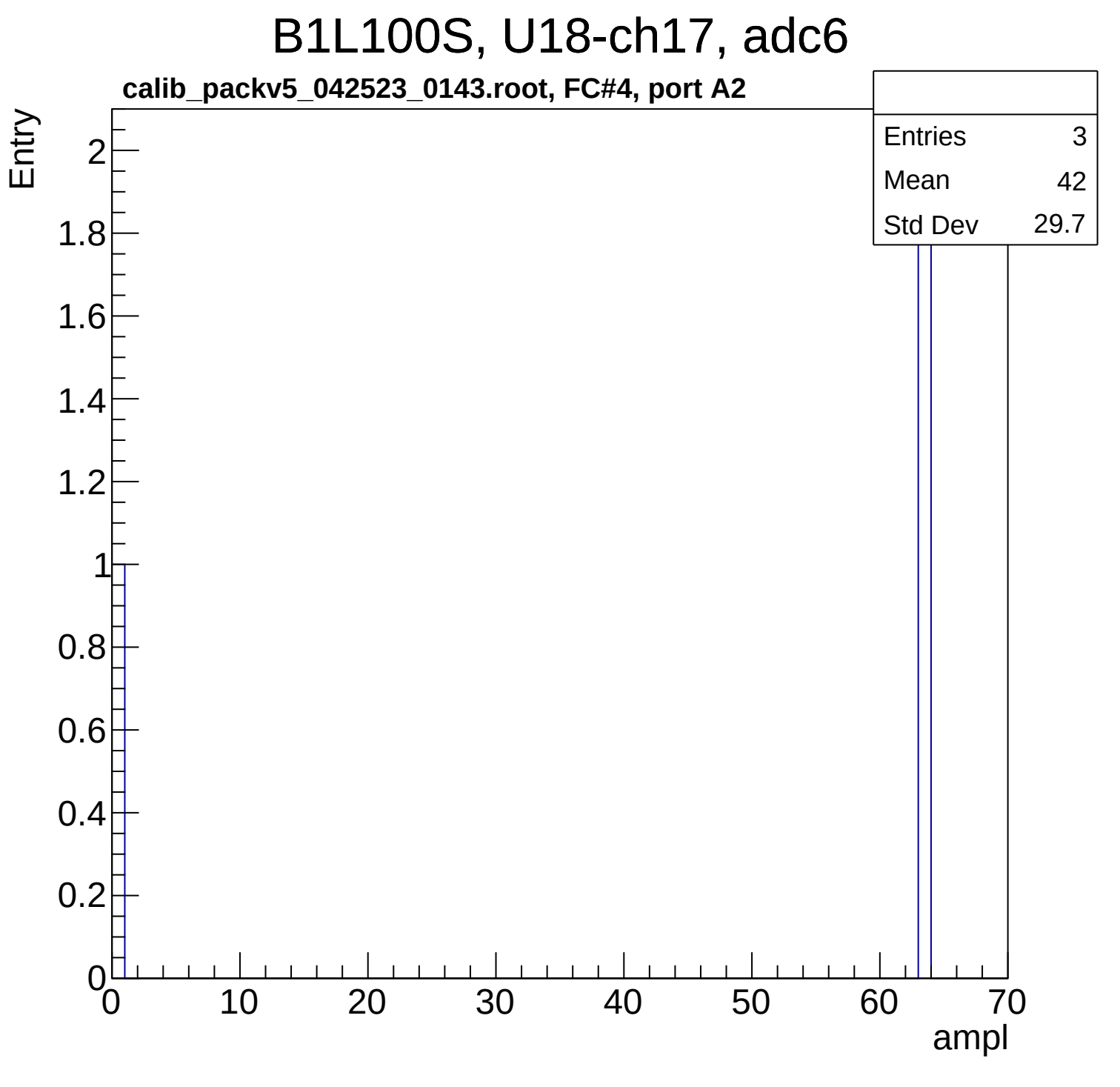

B1L100S, U18-ch17, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 37.22
Std Dev 3.81
Gaus mean : 37.2670
Gaus Width: 3.1945
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

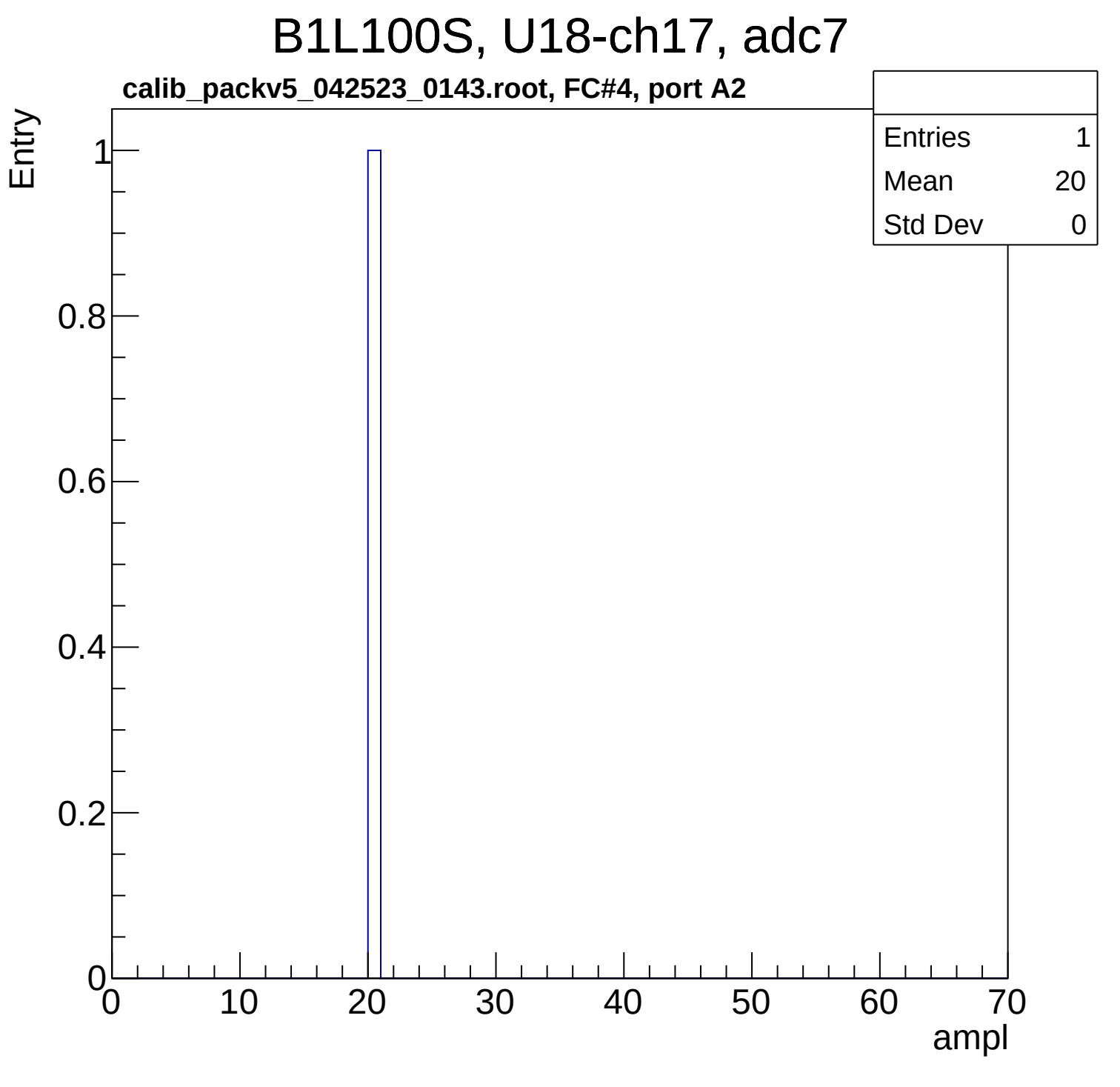

B1L100S, U18-ch17, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 43.95
Std Dev 3.232
Gaus mean : 44.3402
Gaus Width: 2.8652
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

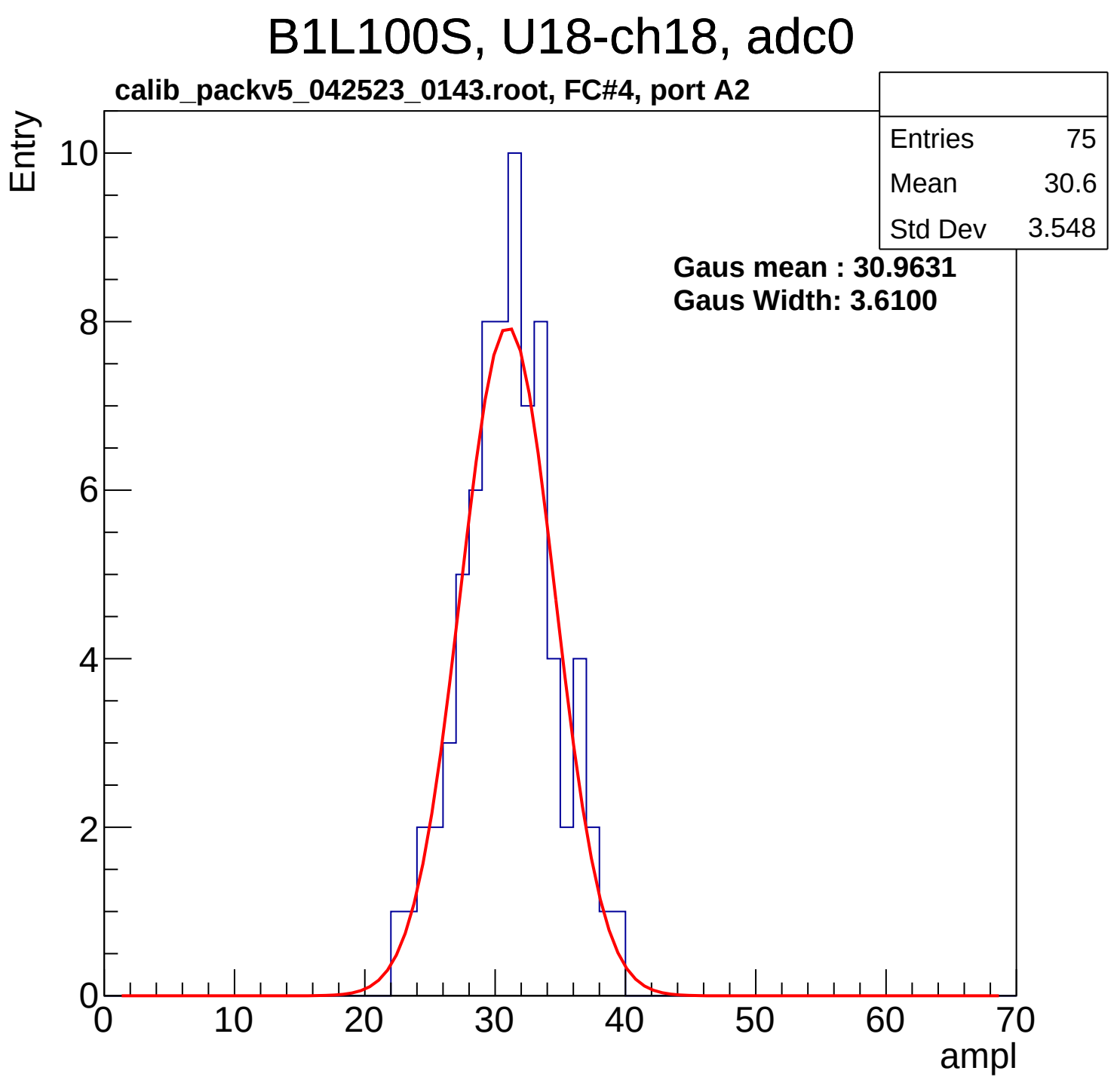

B1L100S, U18-ch17, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 50.47
Std Dev 3.359
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

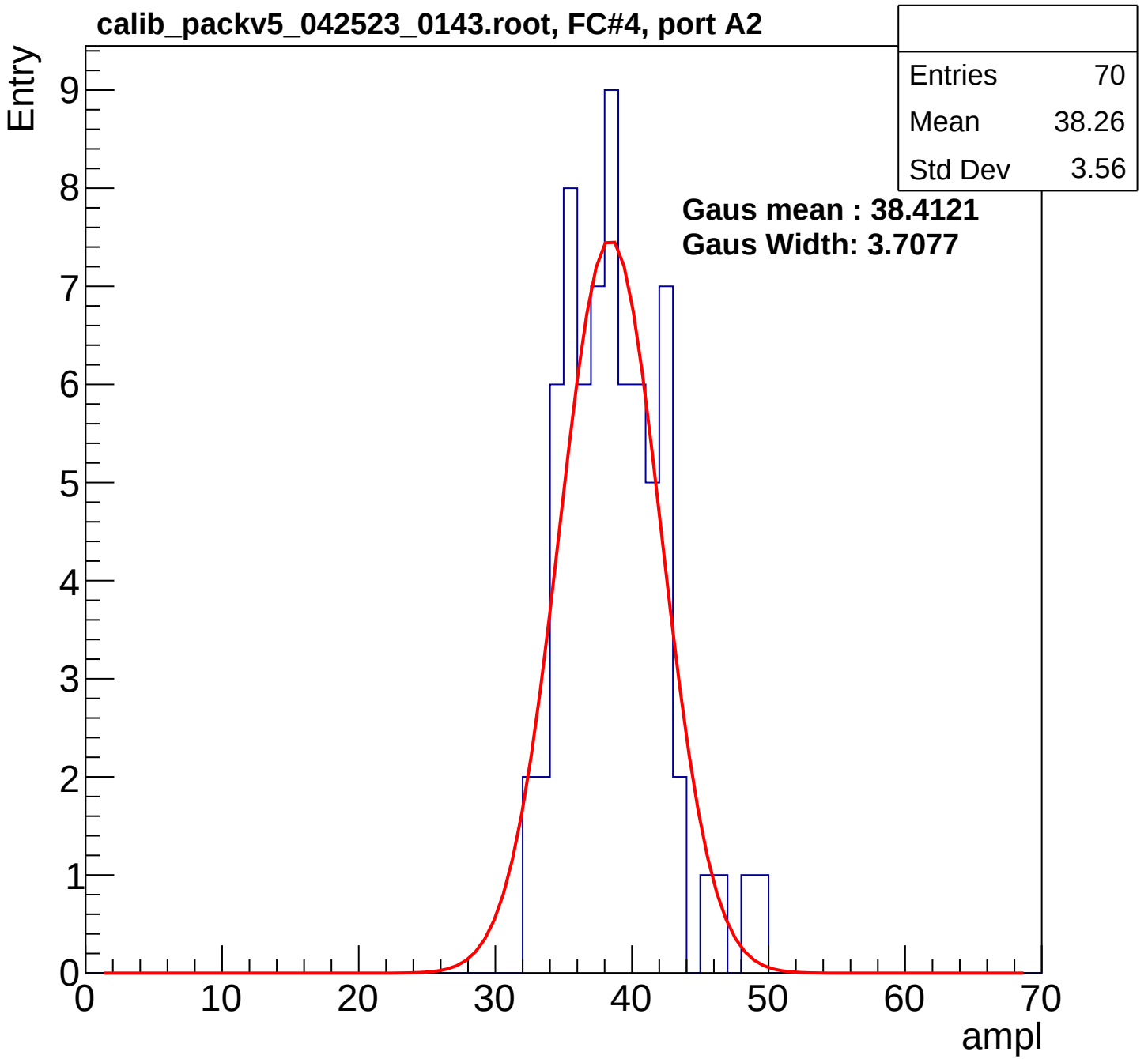

B1L100S, U18-ch17, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 56.24
Std Dev 3.831
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

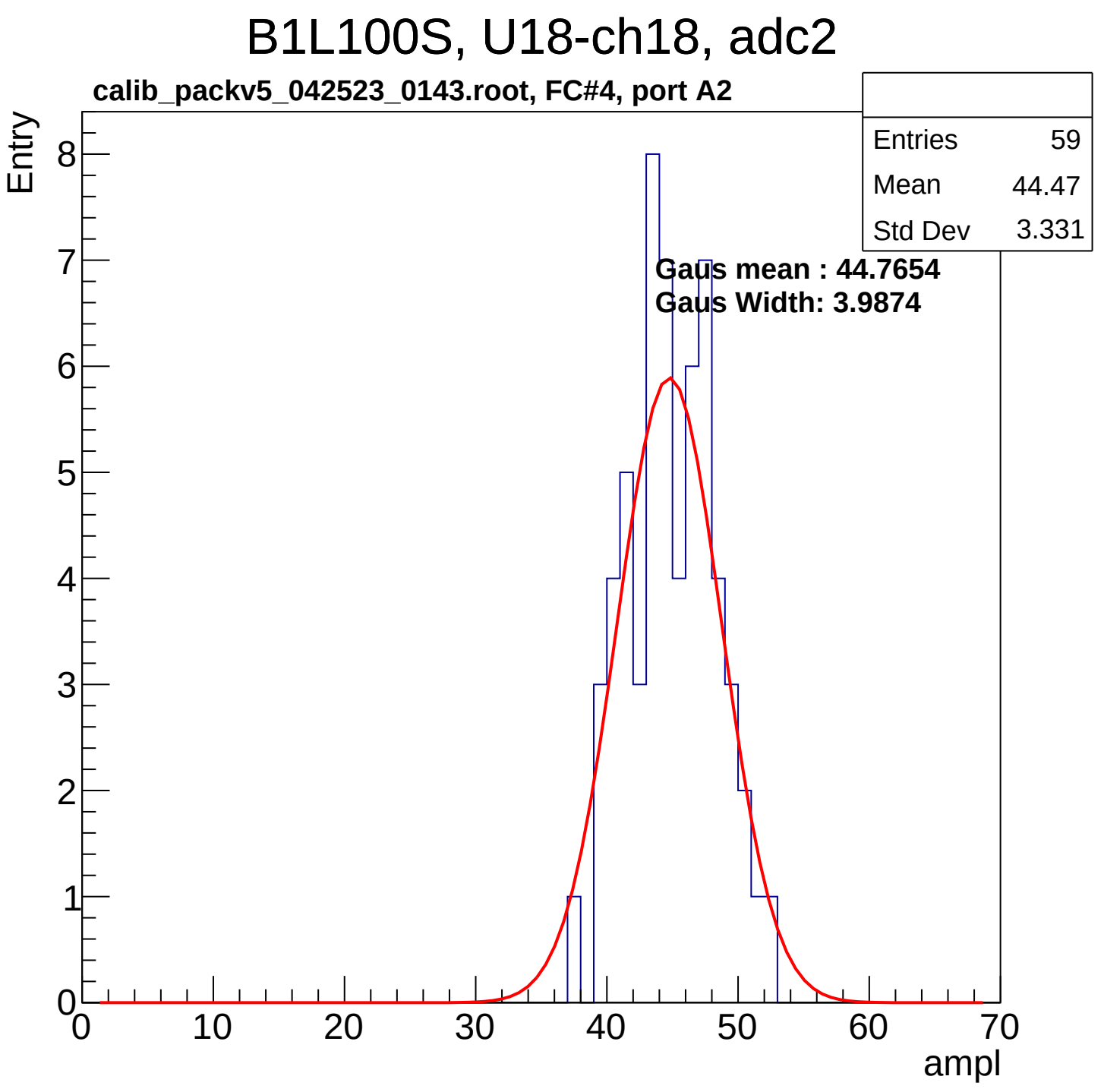

B1L100S, U18-ch17, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 35
Mean 60.29
Std Dev 2.064
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

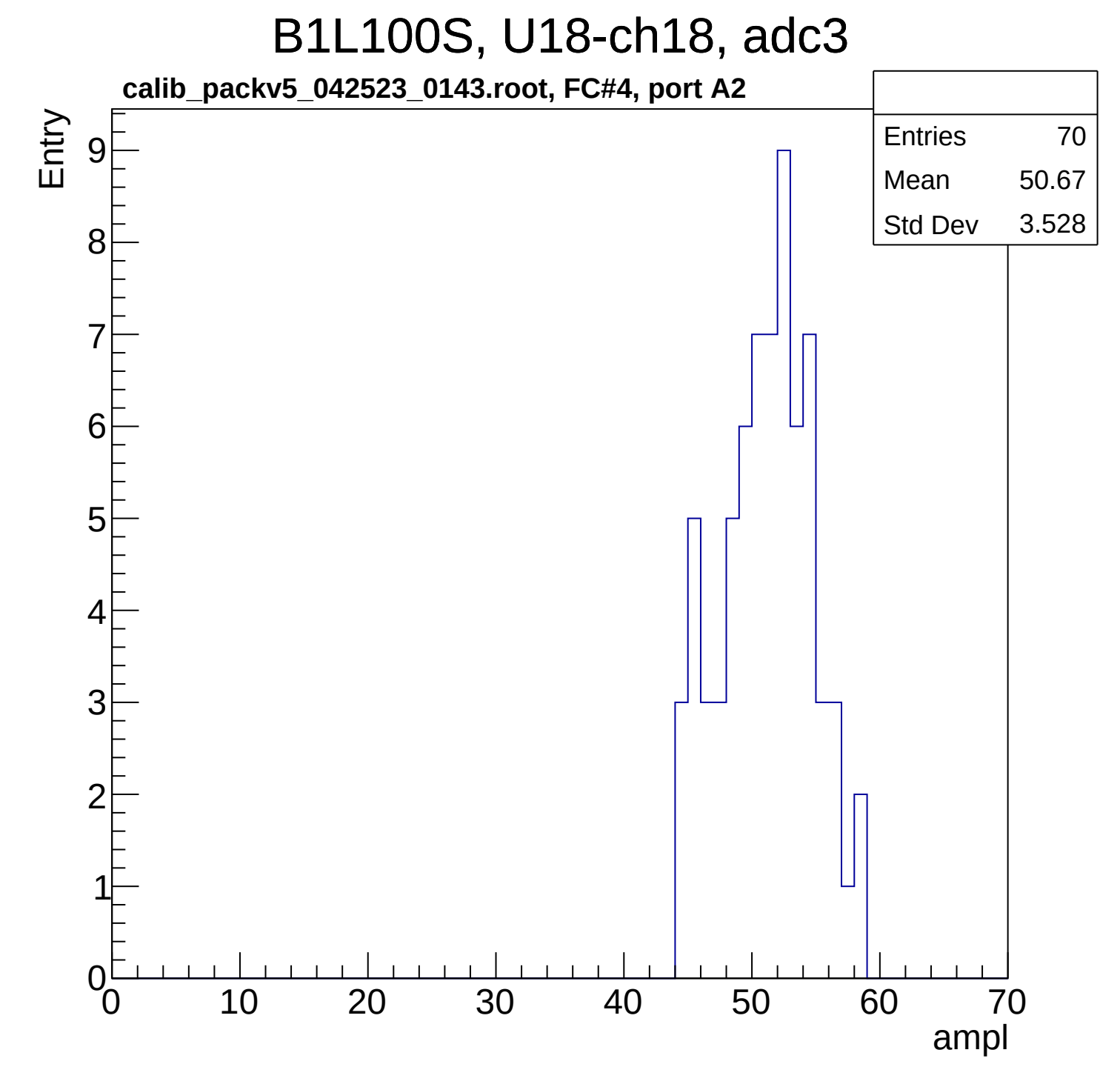

B1L100S, U18-ch17, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 42
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

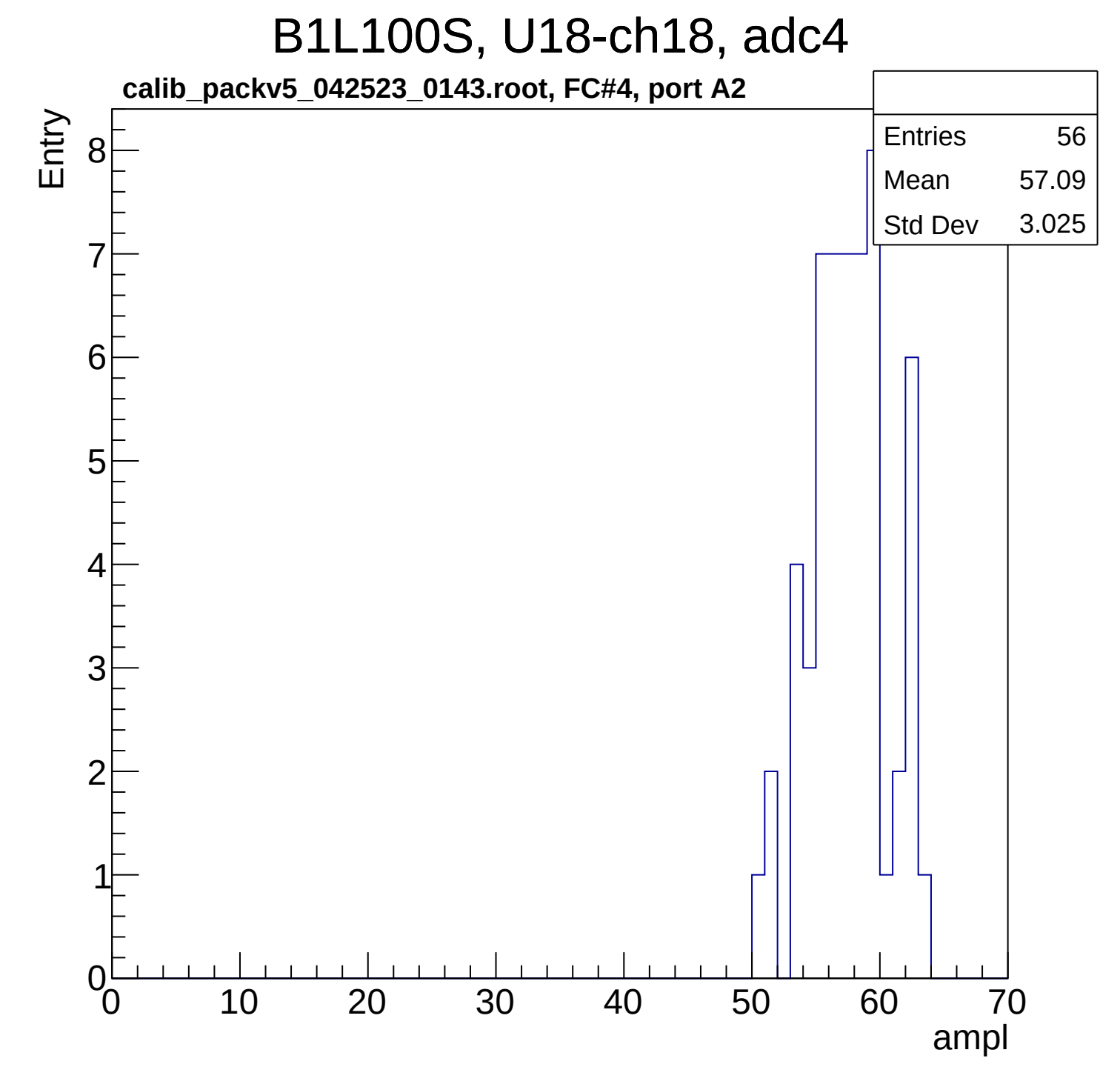

B1L100S, U18-ch17, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 20
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

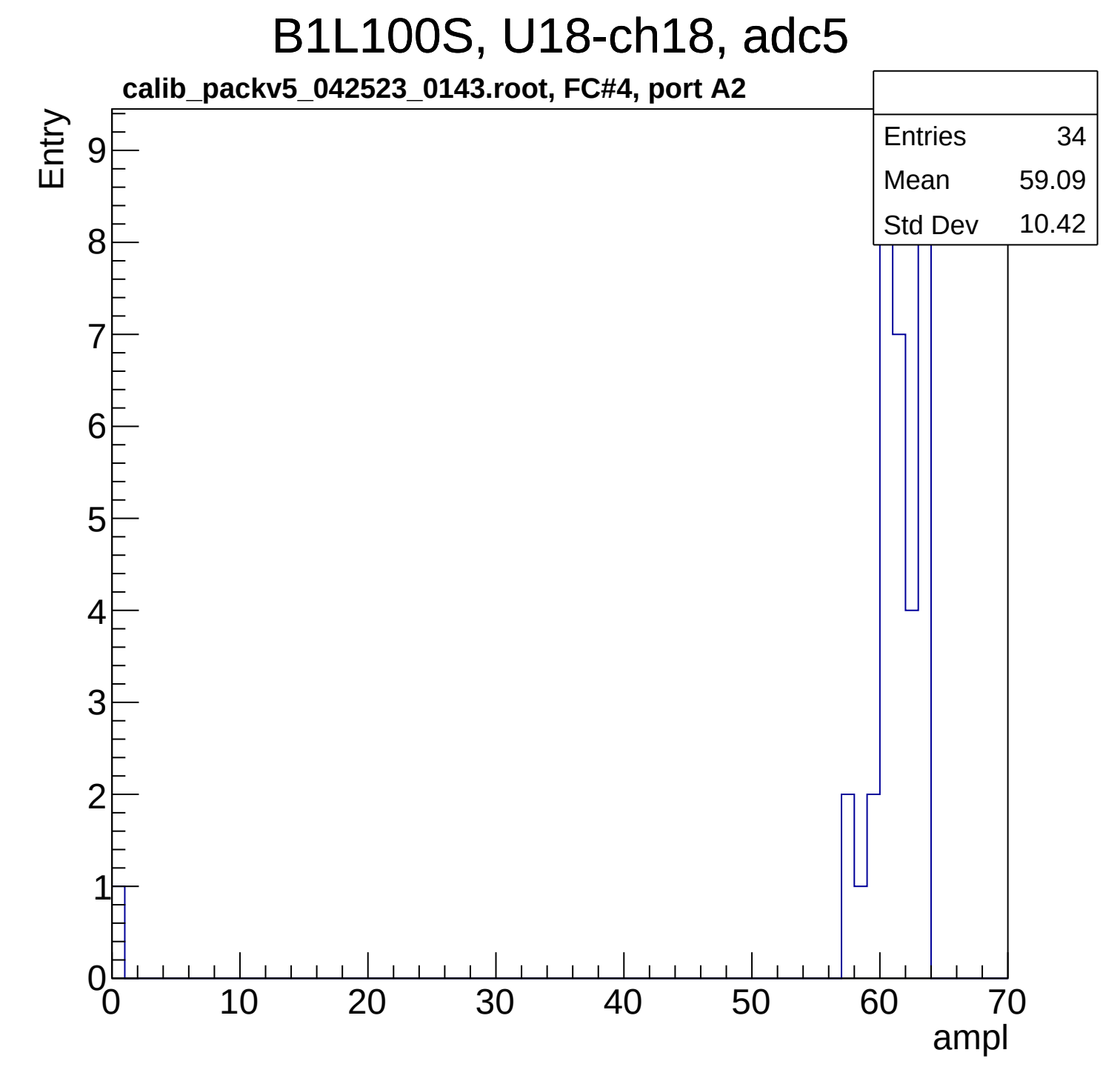

B1L100S, U18-ch18, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 30.6
Std Dev 3.548
Gaus mean : 30.9631
Gaus Width: 3.6100
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

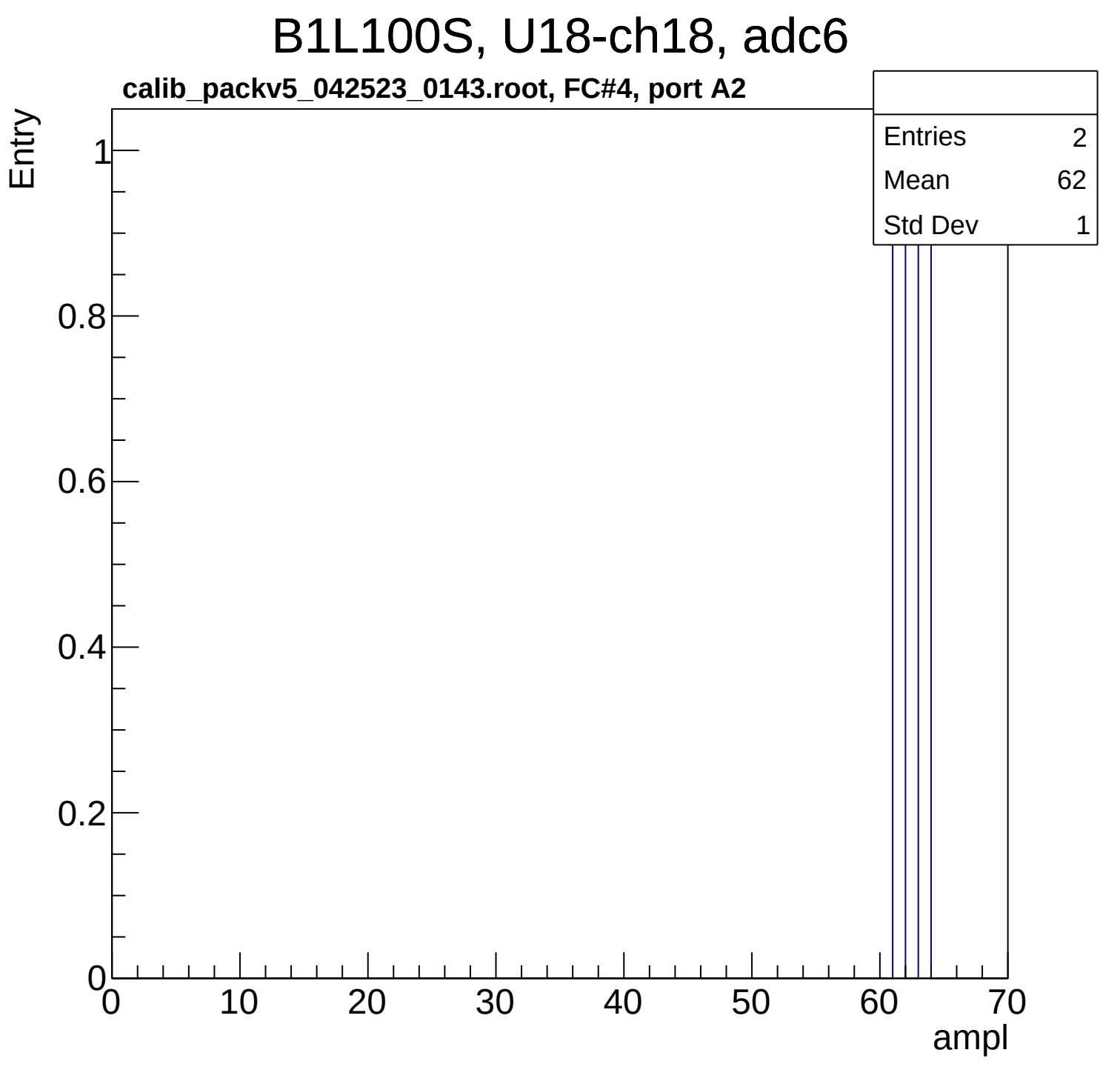

B1L100S, U18-ch18, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 38.26
Std Dev 3.56
Gaus mean : 38.4121
Gaus Width: 3.7077
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

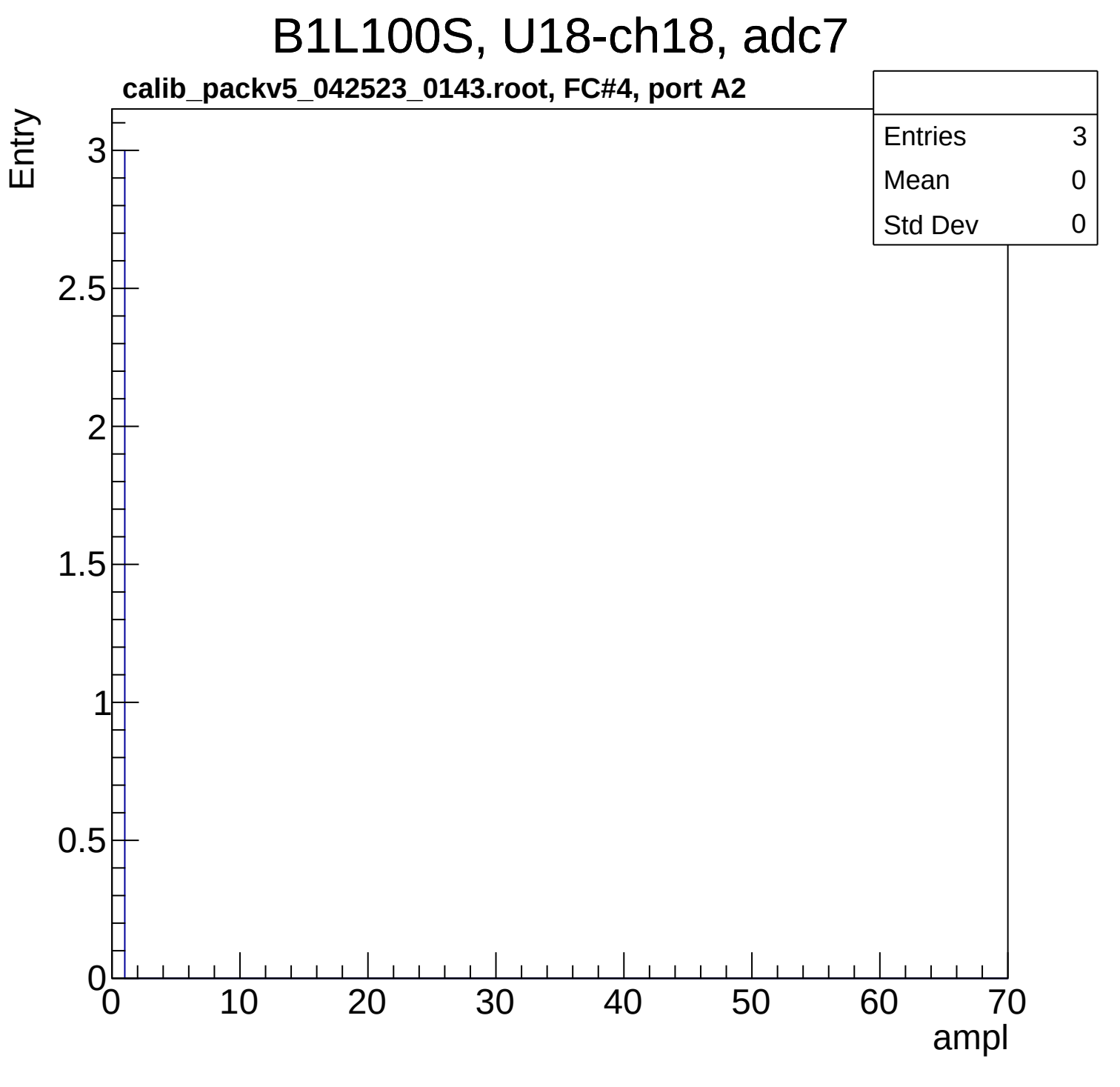

B1L100S, U18-ch18, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 44.47
Std Dev 3.331
Gaus mean : 44.7654
Gaus Width: 3.9874
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

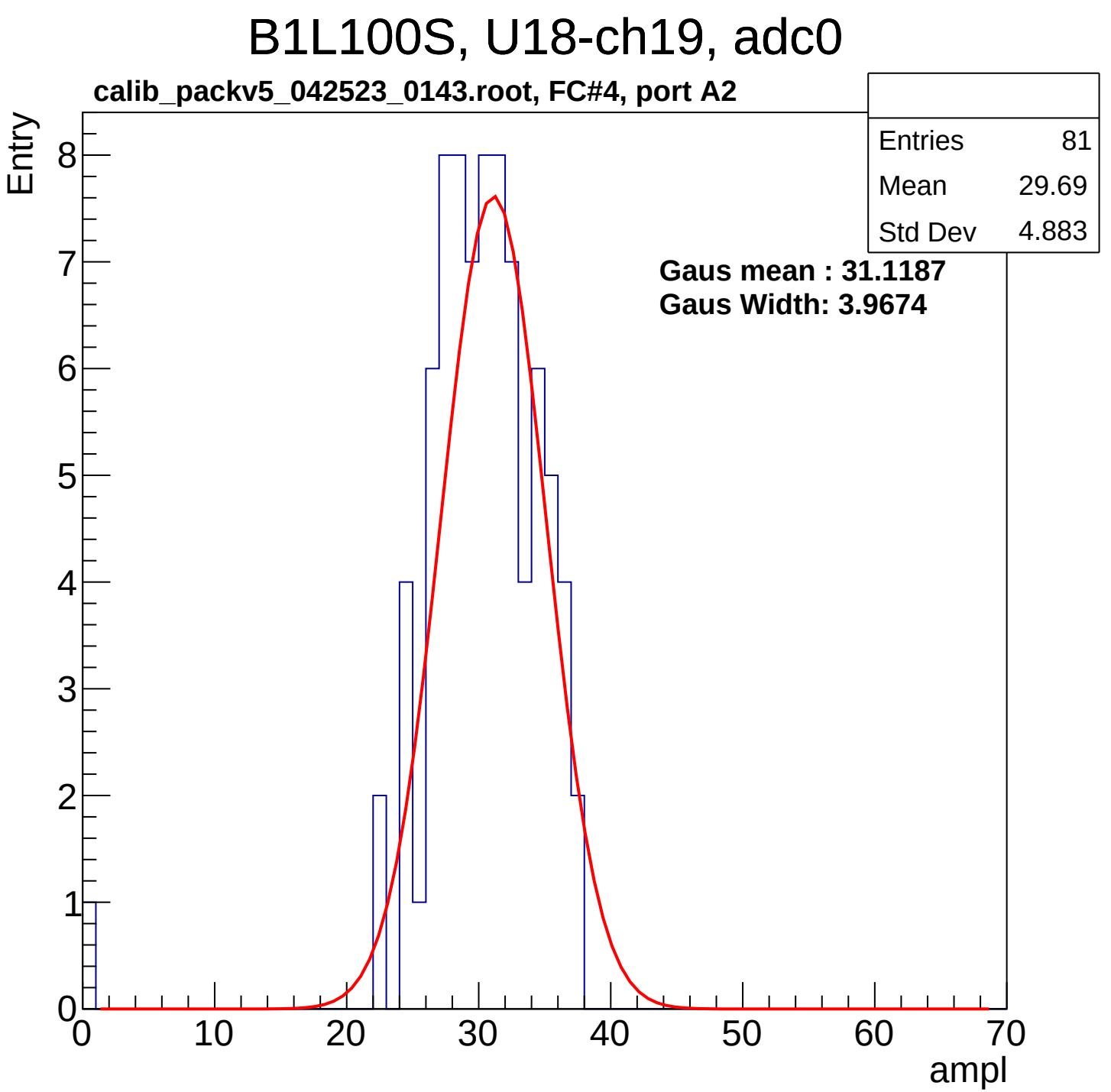

B1L100S, U18-ch18, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 50.67
Std Dev 3.528
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

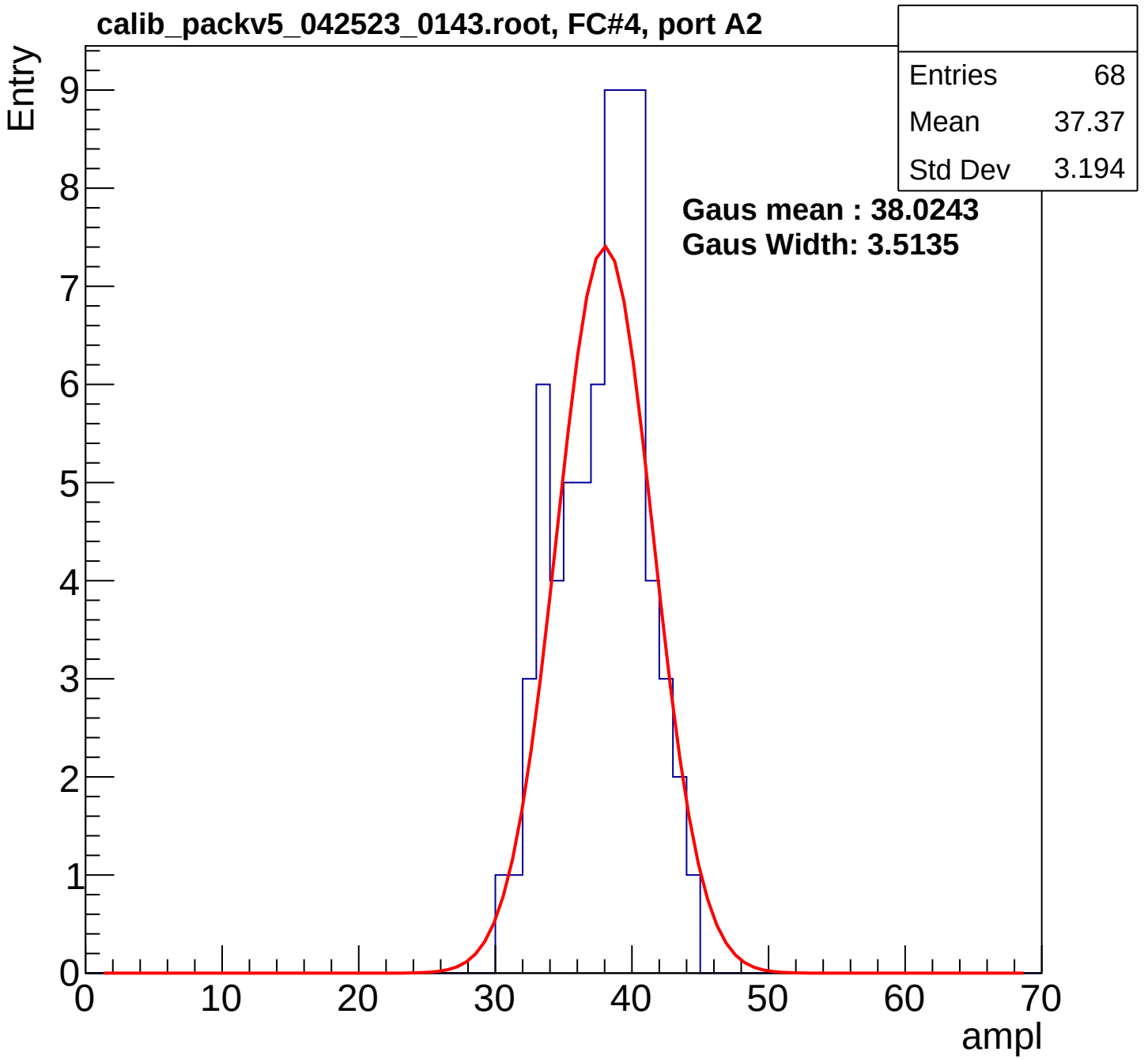

B1L100S, U18-ch18, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 57.09
Std Dev 3.025
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

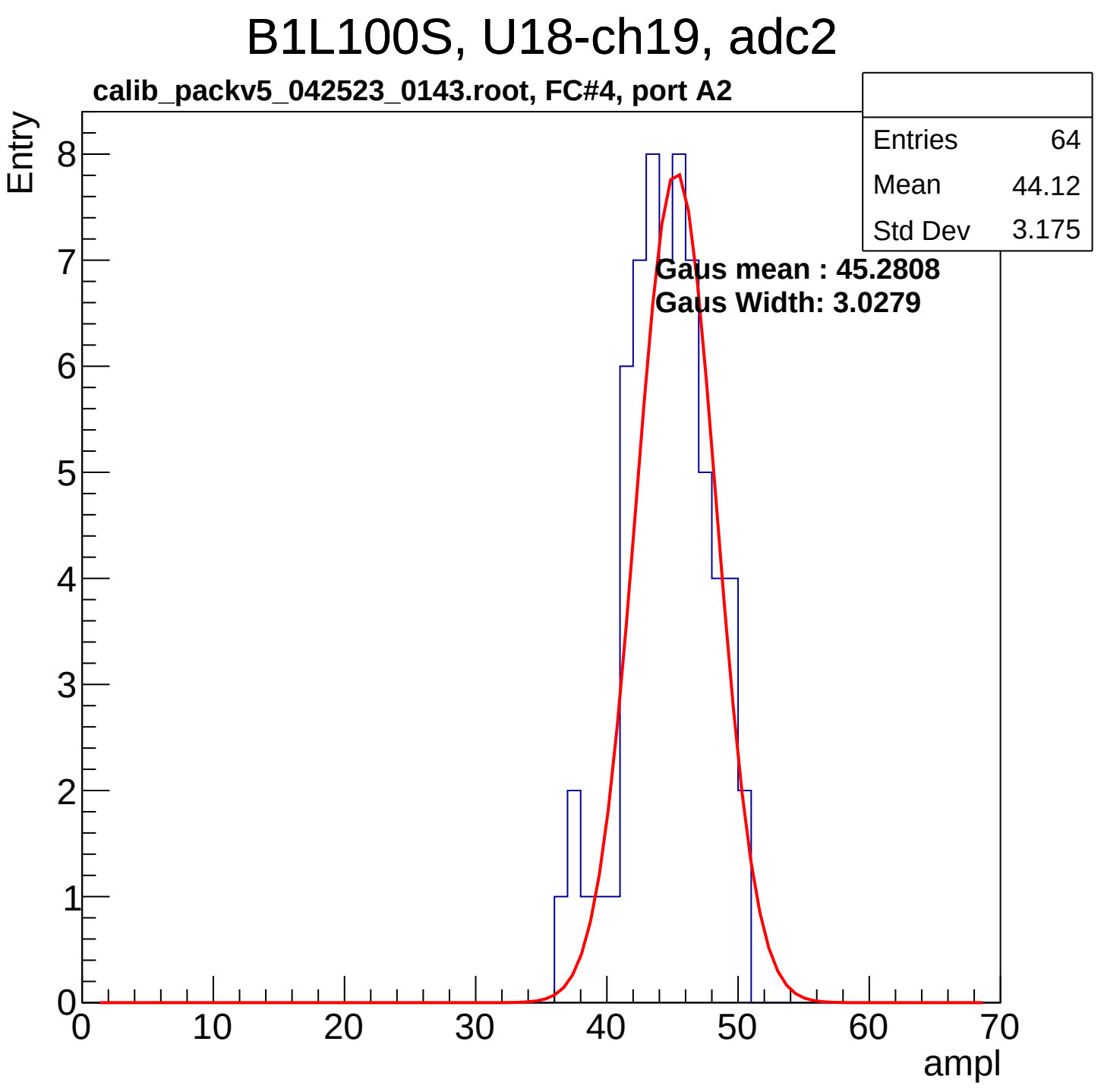

B1L100S, U18-ch18, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 34
Mean 59.09
Std Dev 10.42
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

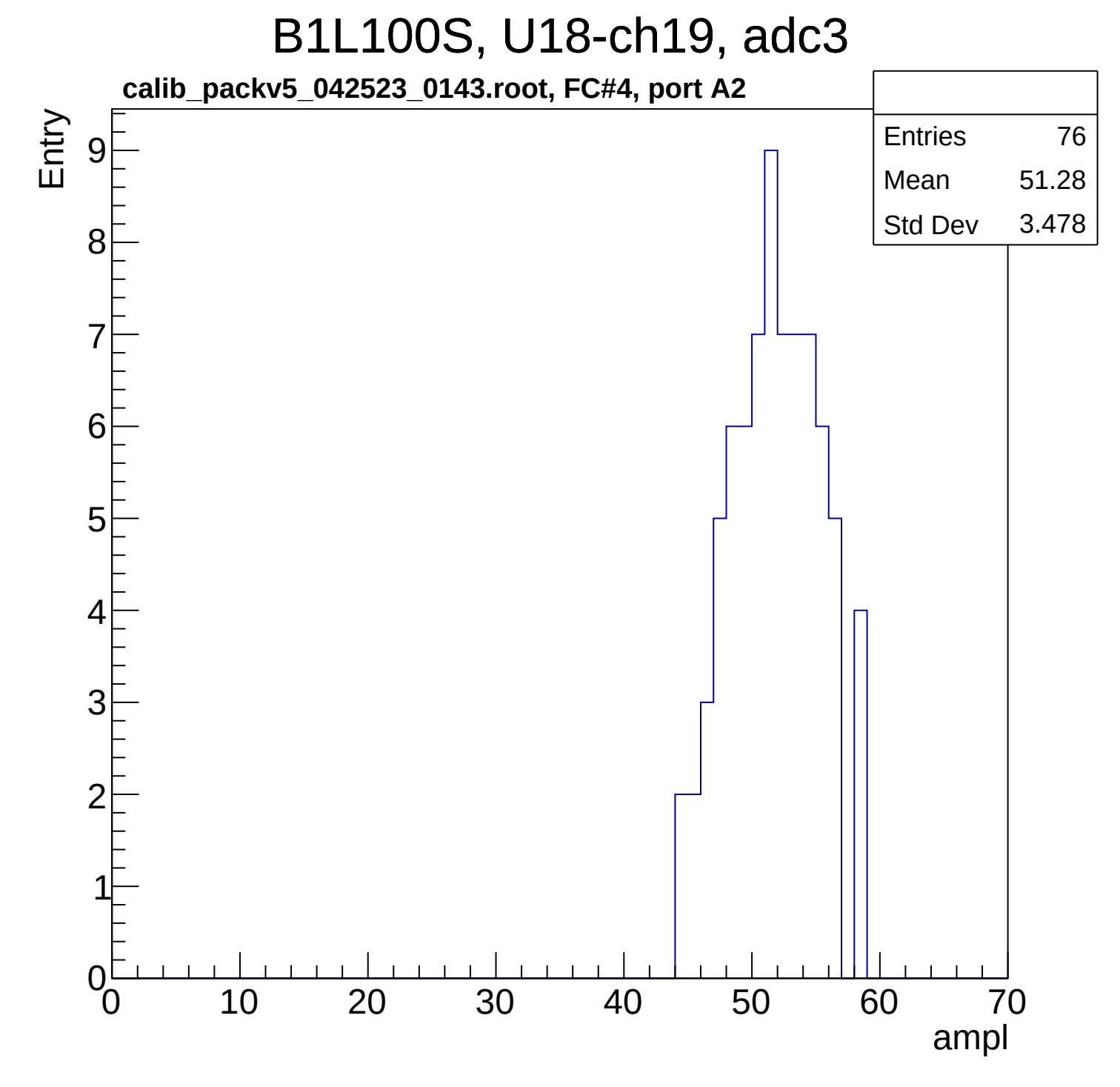

B1L100S, U18-ch18, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 62
Std Dev 1
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

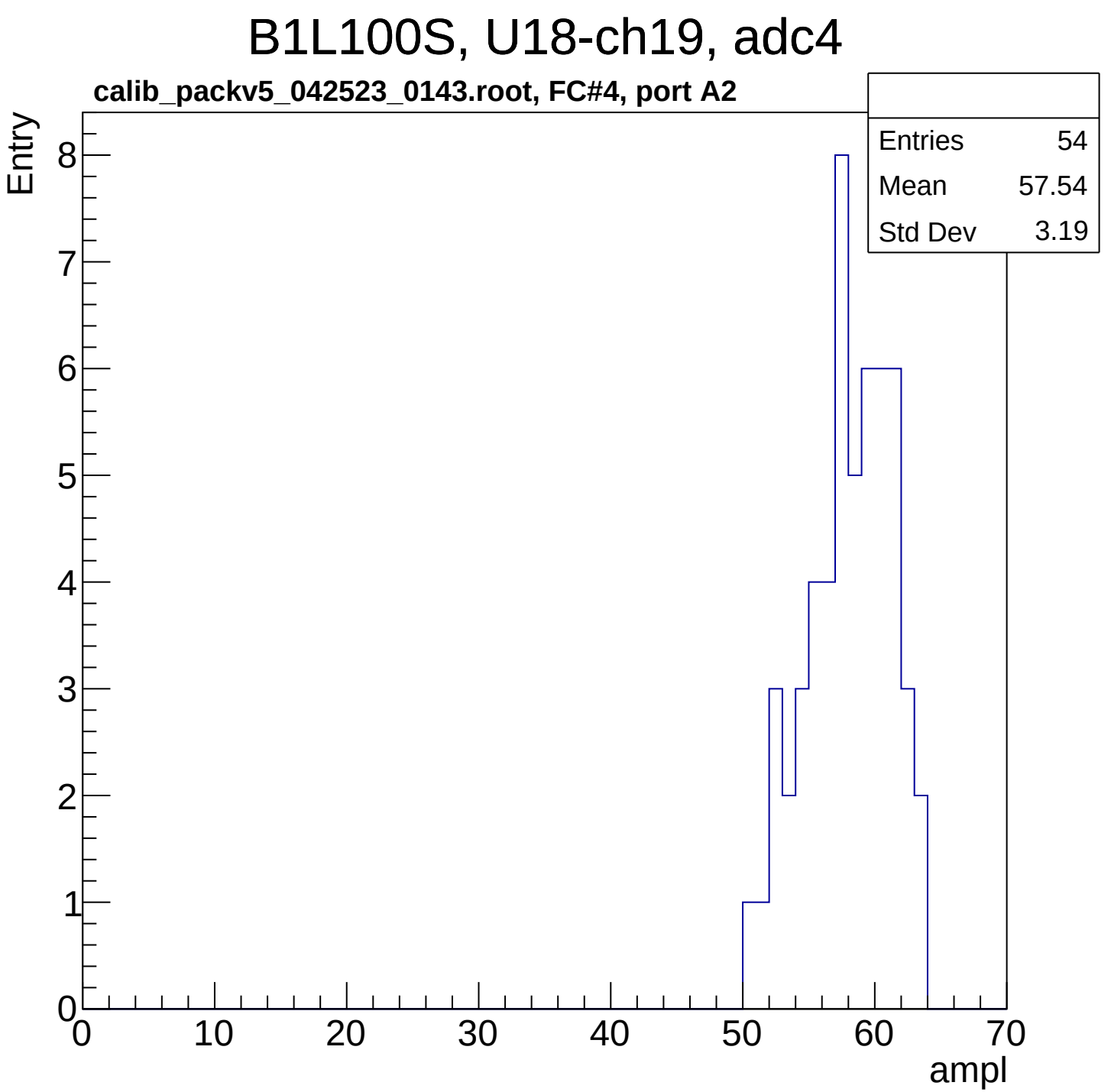

B1L100S, U18-ch18, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 0
Std Dev 0
Entry
3
2.5
2
1.5
1
0.5
0
0
10
20
30
40
50
60
70
ampl

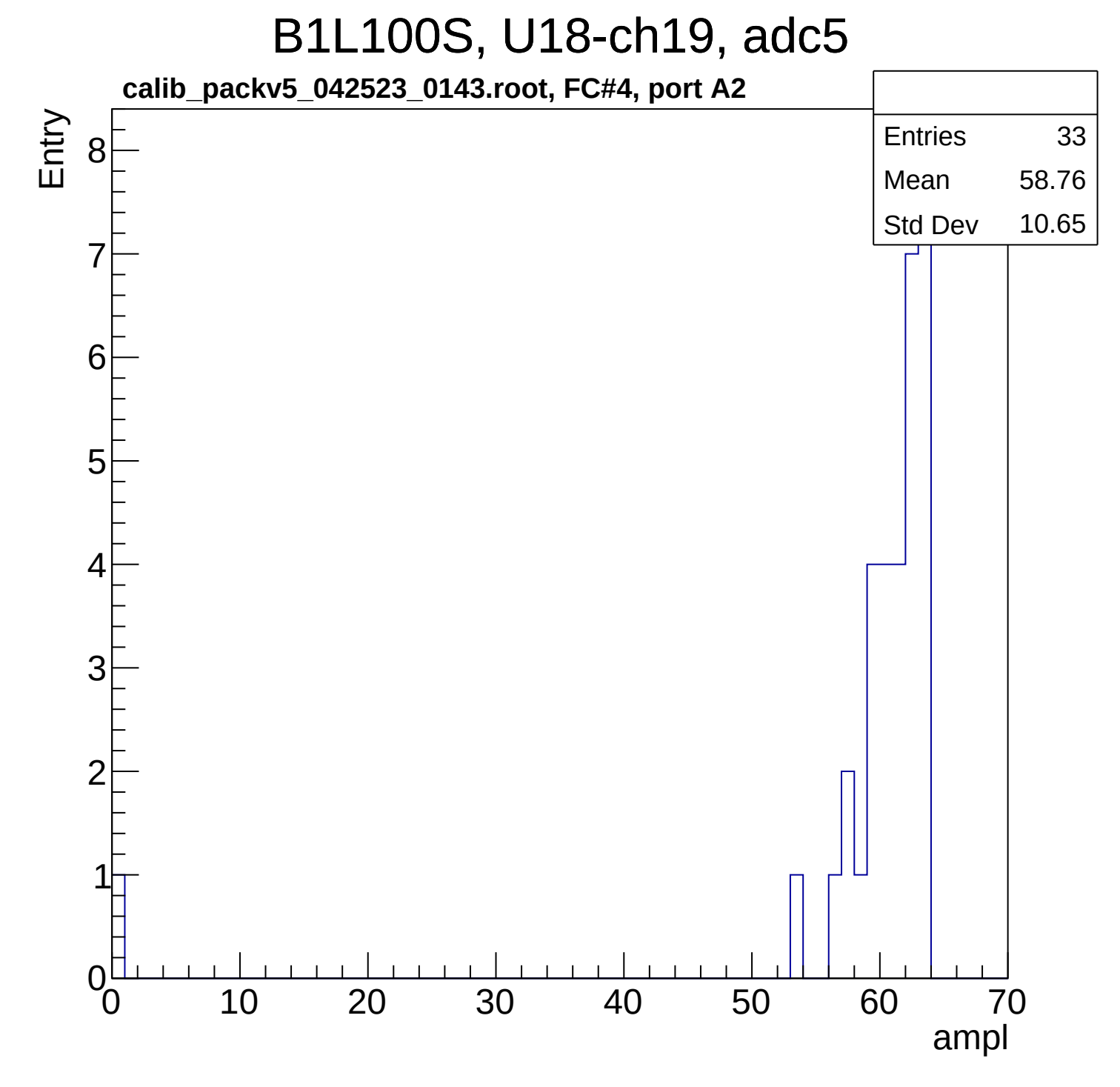

B1L100S, U18-ch19, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 29.69
Std Dev 4.883
Gaus mean : 31.1187
Gaus Width: 3.9674
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

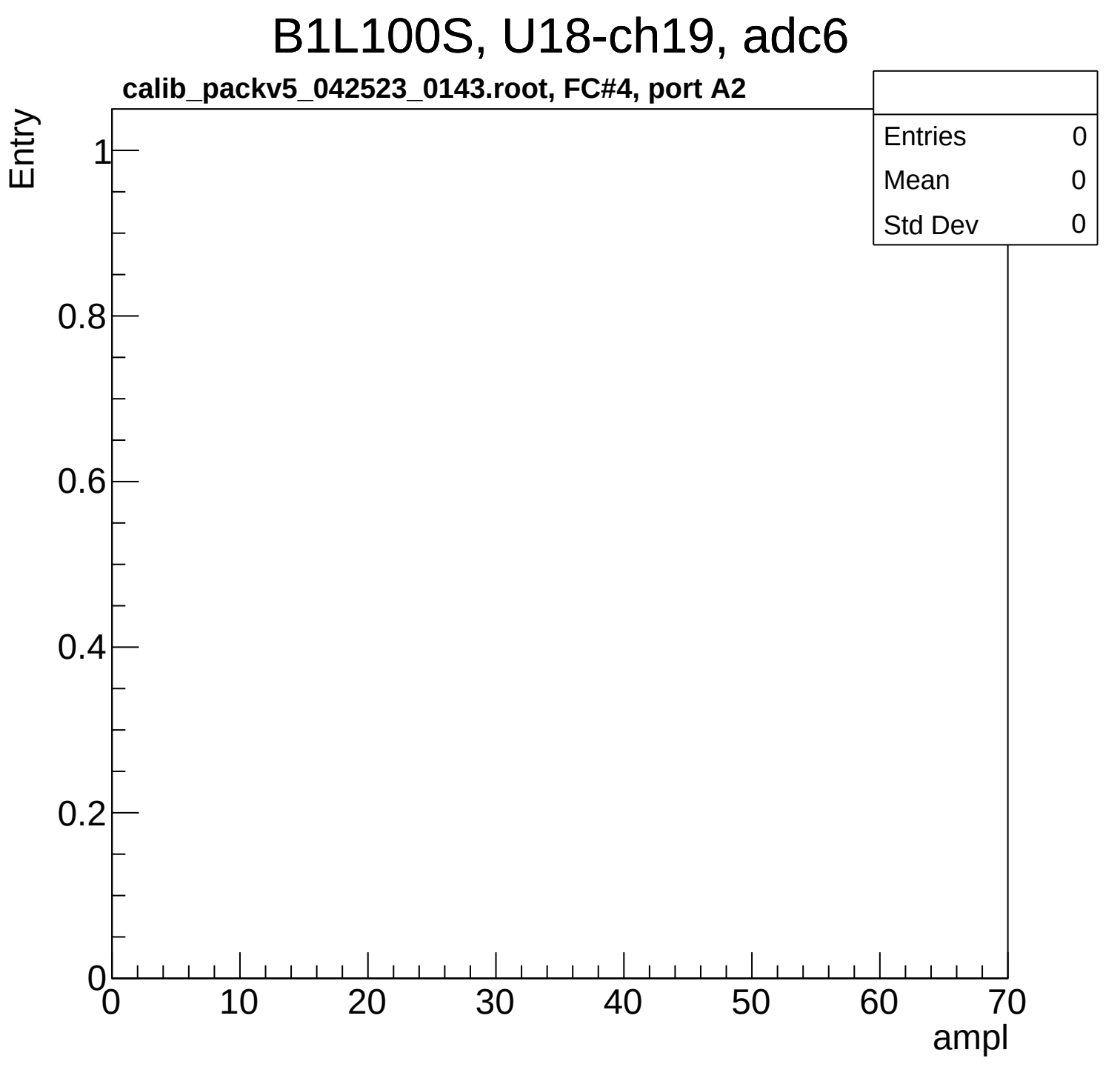

B1L100S, U18-ch19, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 37.37
Std Dev 3.194
Gaus mean : 38.0243
Gaus Width: 3.5135
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

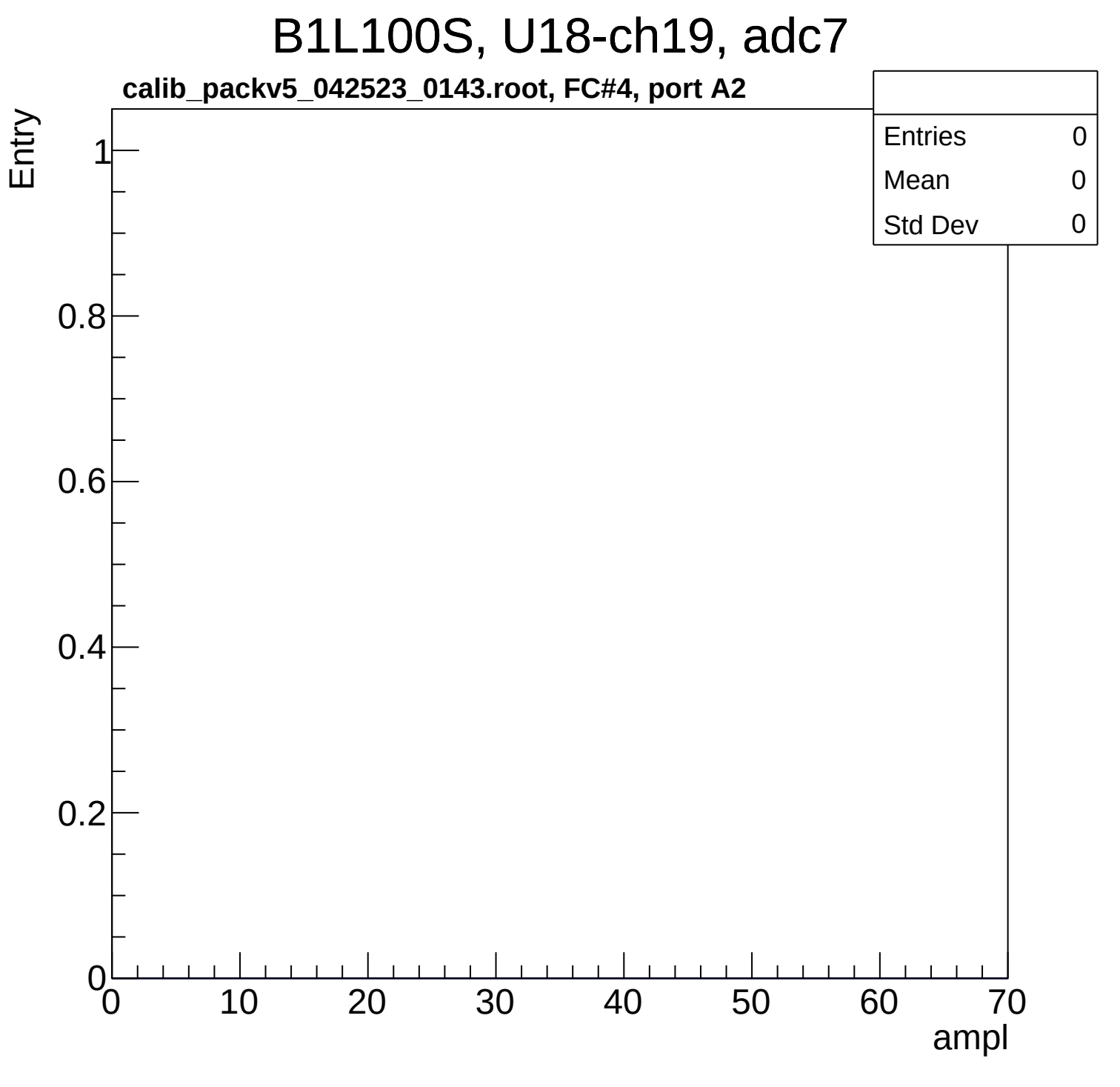

B1L100S, U18-ch19, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 44.12
Std Dev 3.175
Gaus mean : 45.2808
Gaus Width: 3.0279
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

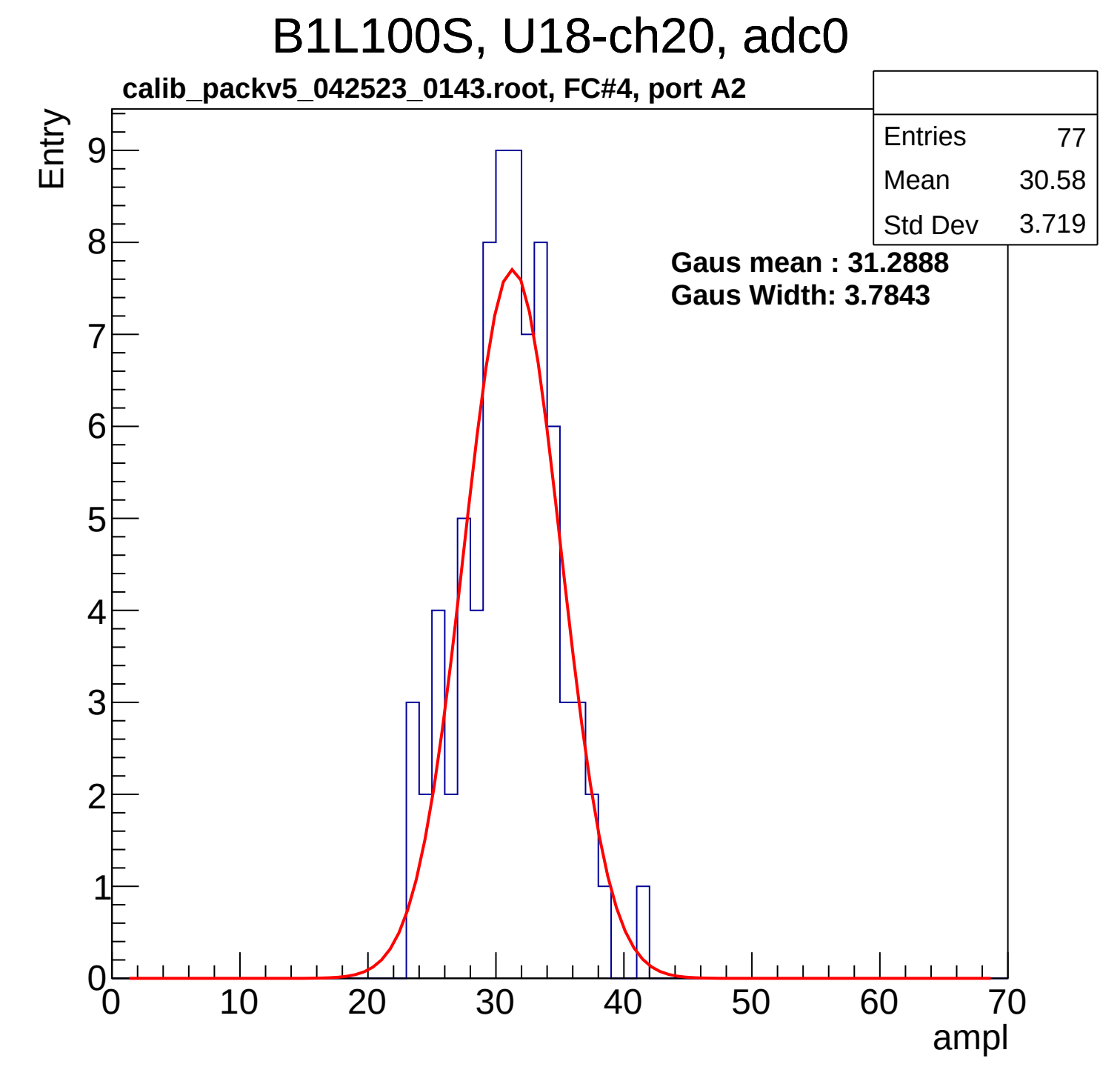

B1L100S, U18-ch19, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 51.28
Std Dev 3.478
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

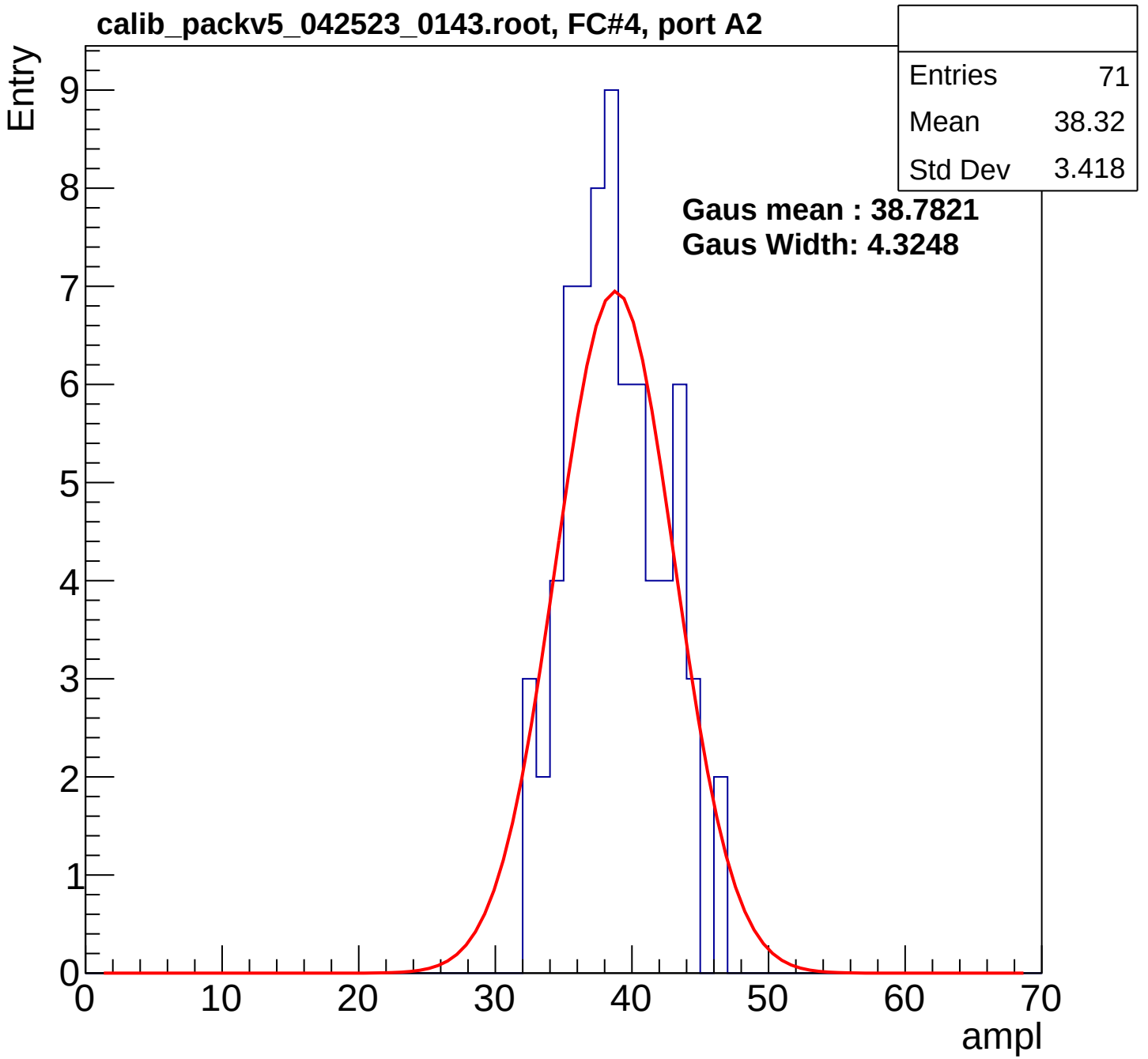

B1L100S, U18-ch19, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 57.54
Std Dev 3.19
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

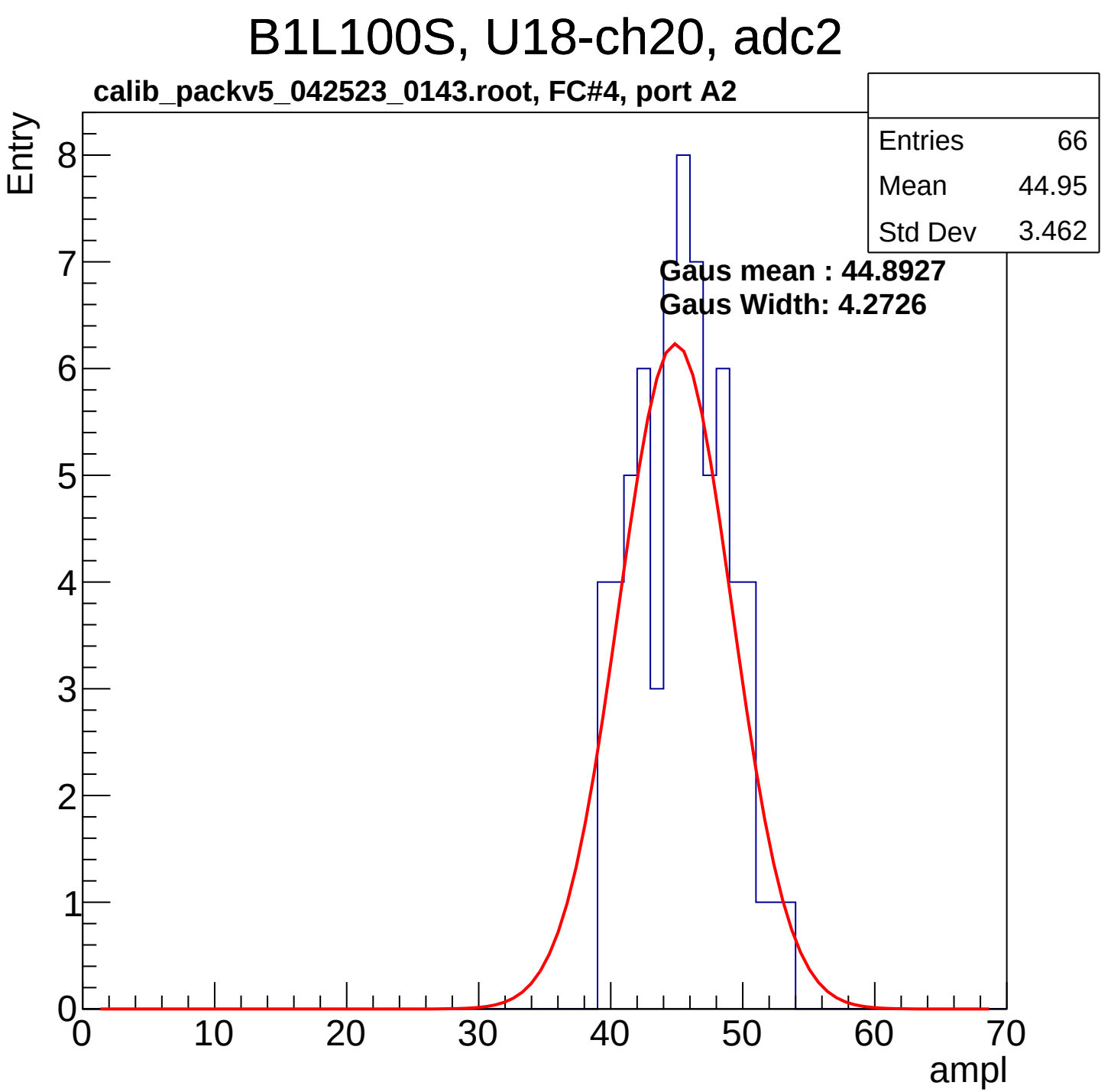

B1L100S, U18-ch19, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 33
Mean 58.76
Std Dev 10.65
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

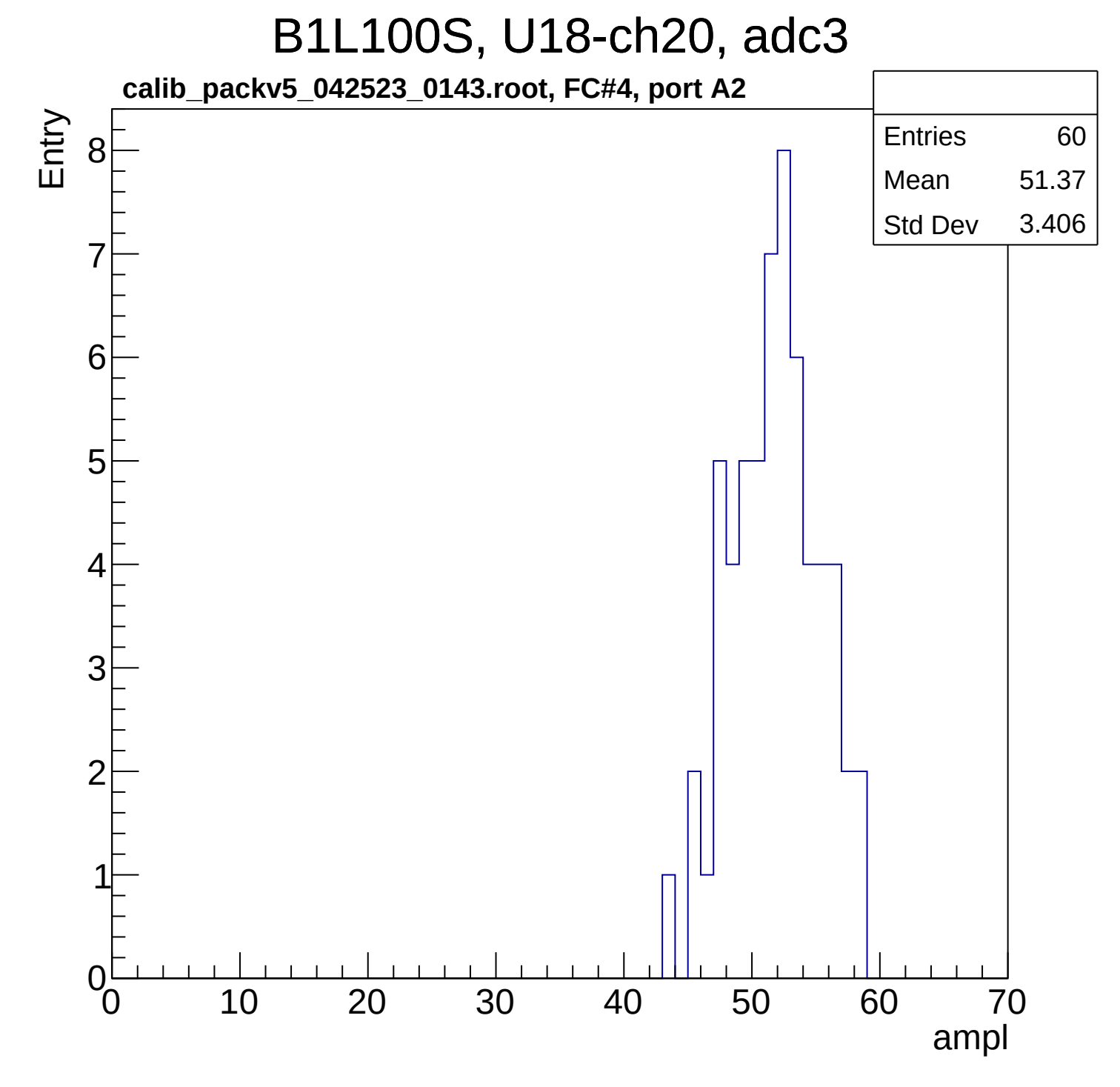

B1L100S, U18-ch19, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

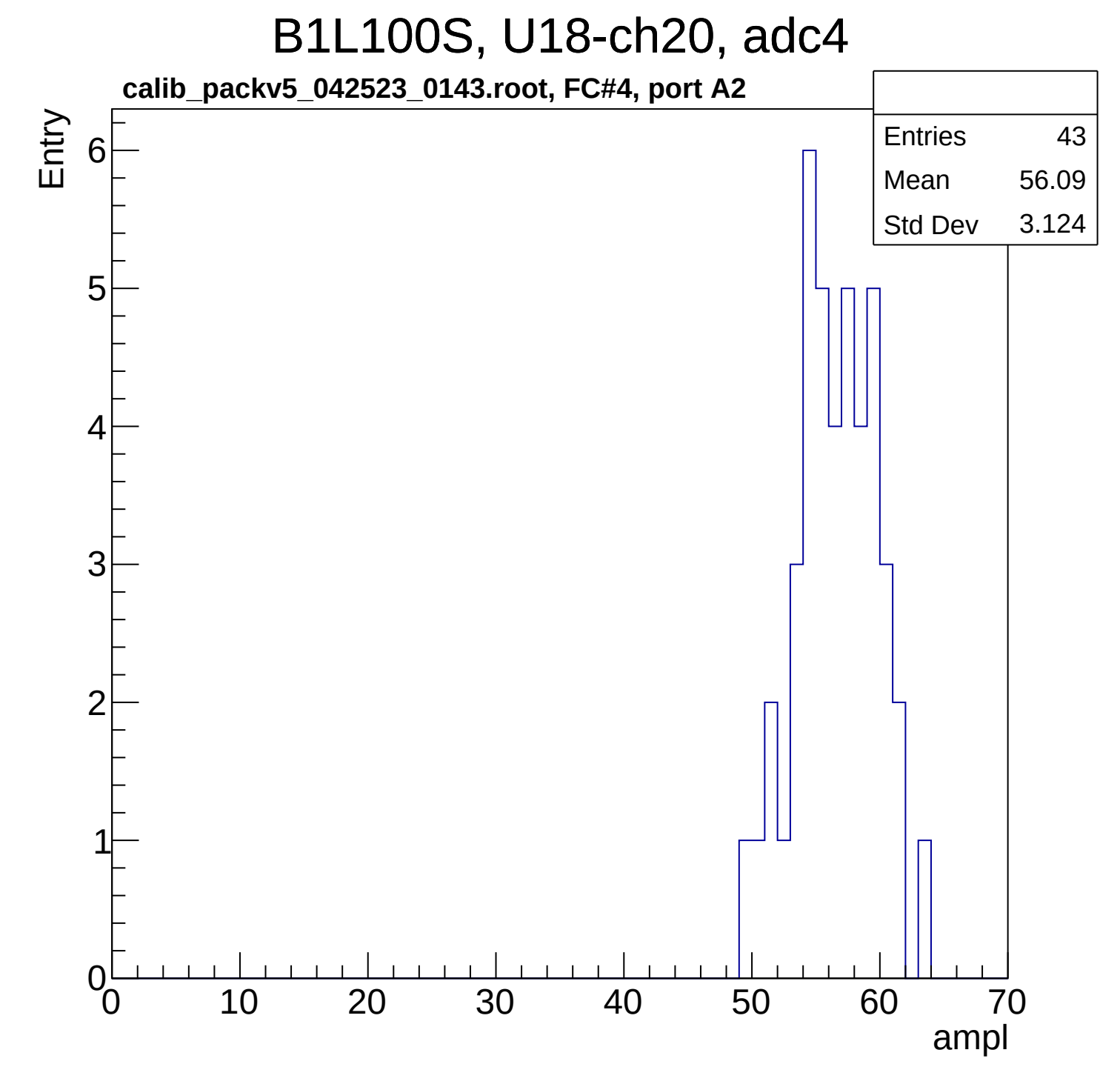

B1L100S, U18-ch19, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

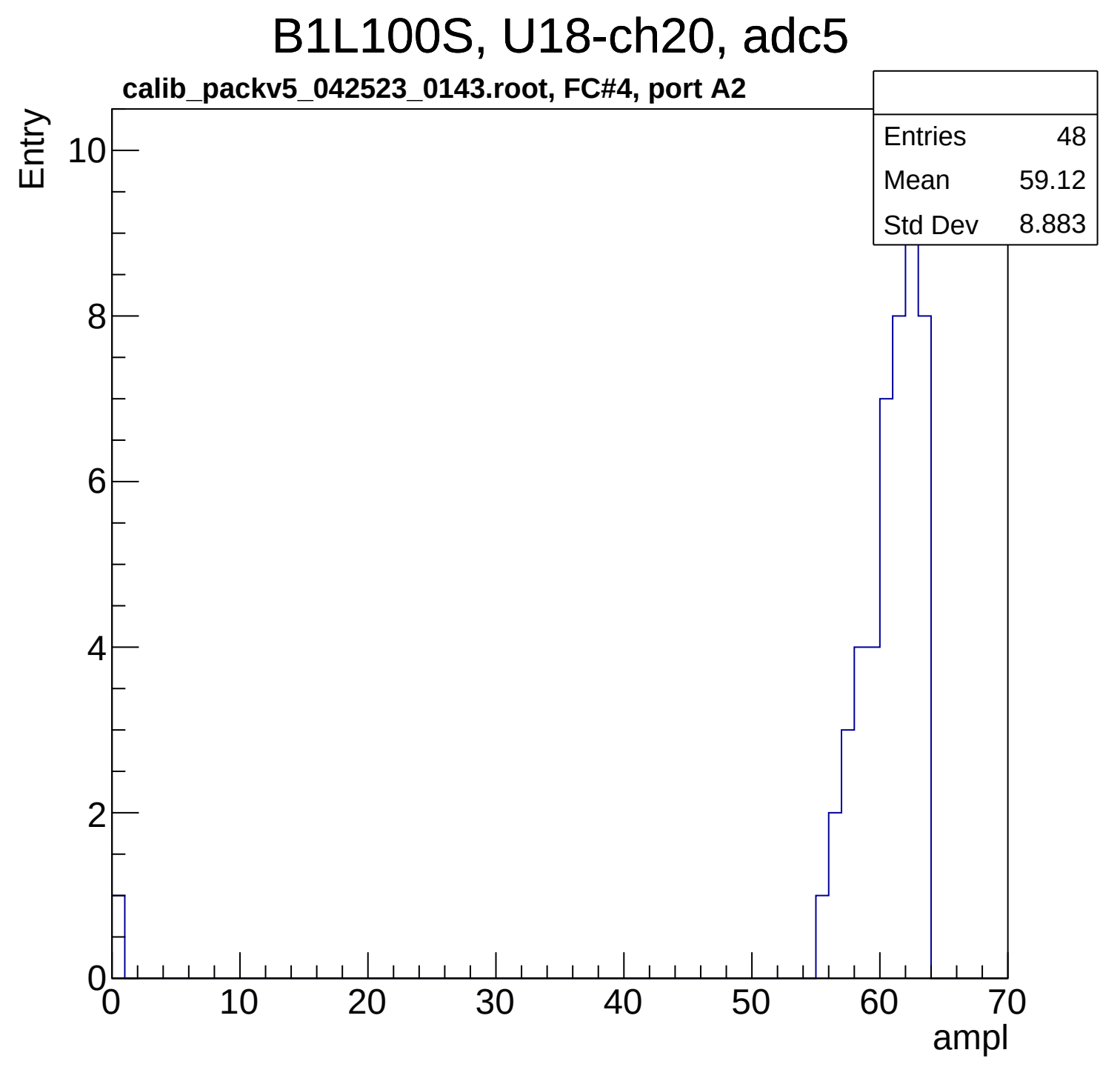

B1L100S, U18-ch20, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 30.58
Std Dev 3.719
Gaus mean : 31.2888
Gaus Width: 3.7843
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

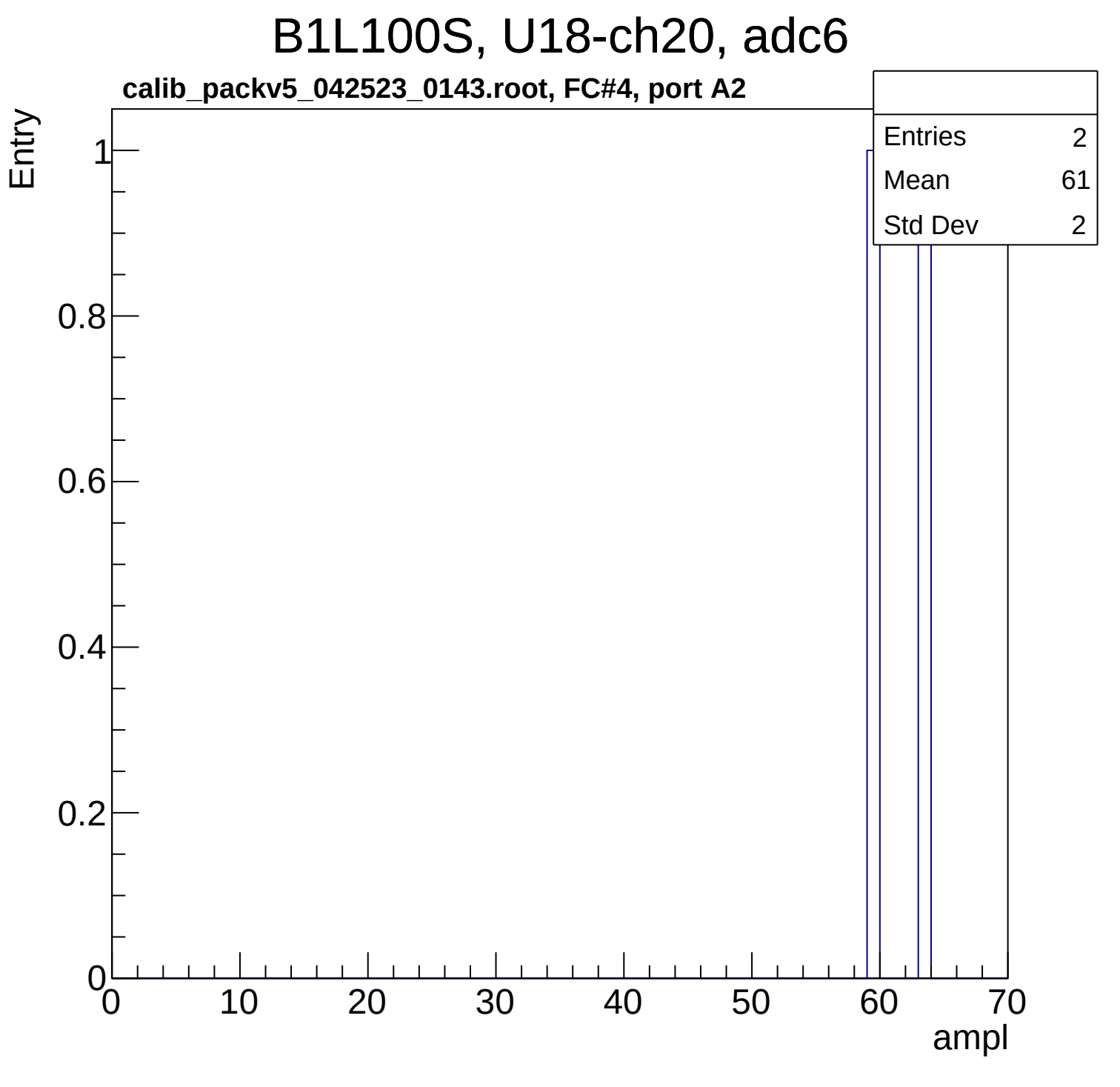

B1L100S, U18-ch20, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 38.32
Std Dev 3.418
Gaus mean : 38.7821
Gaus Width: 4.3248
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

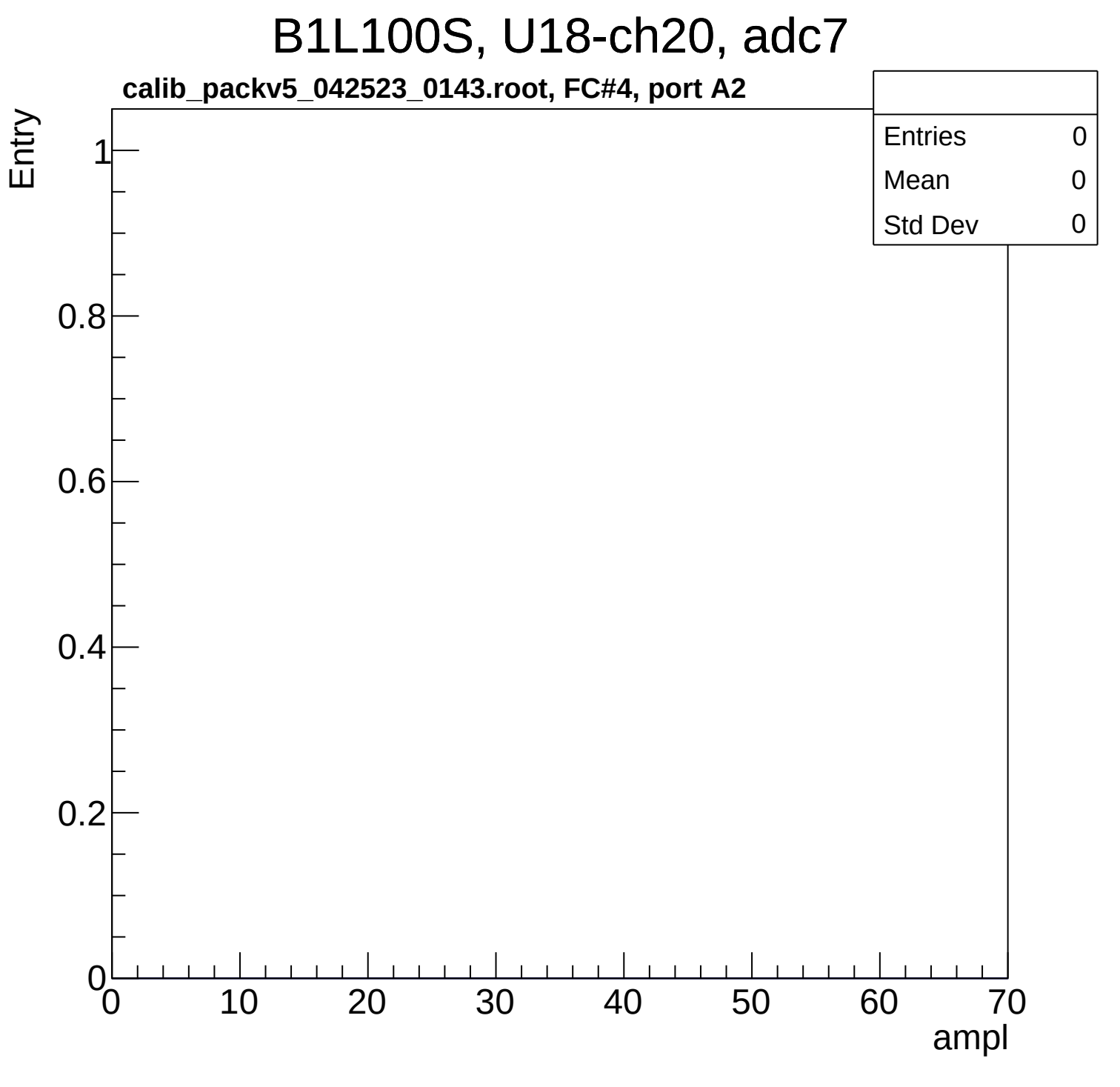

B1L100S, U18-ch20, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 44.95
Std Dev 3.462
Gaus mean : 44.8927
Gaus Width: 4.2726
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

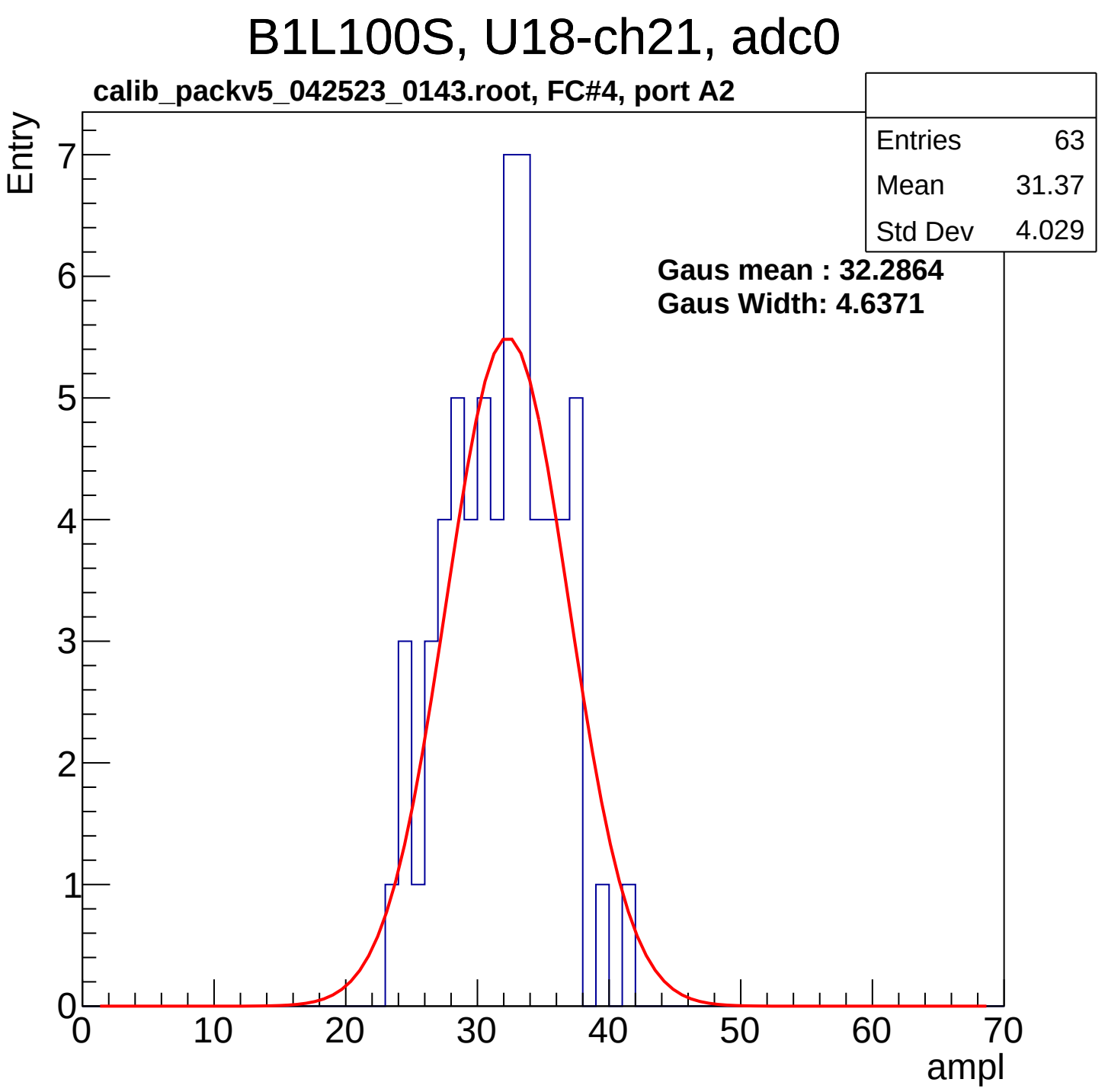

B1L100S, U18-ch20, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 51.37
Std Dev 3.406
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

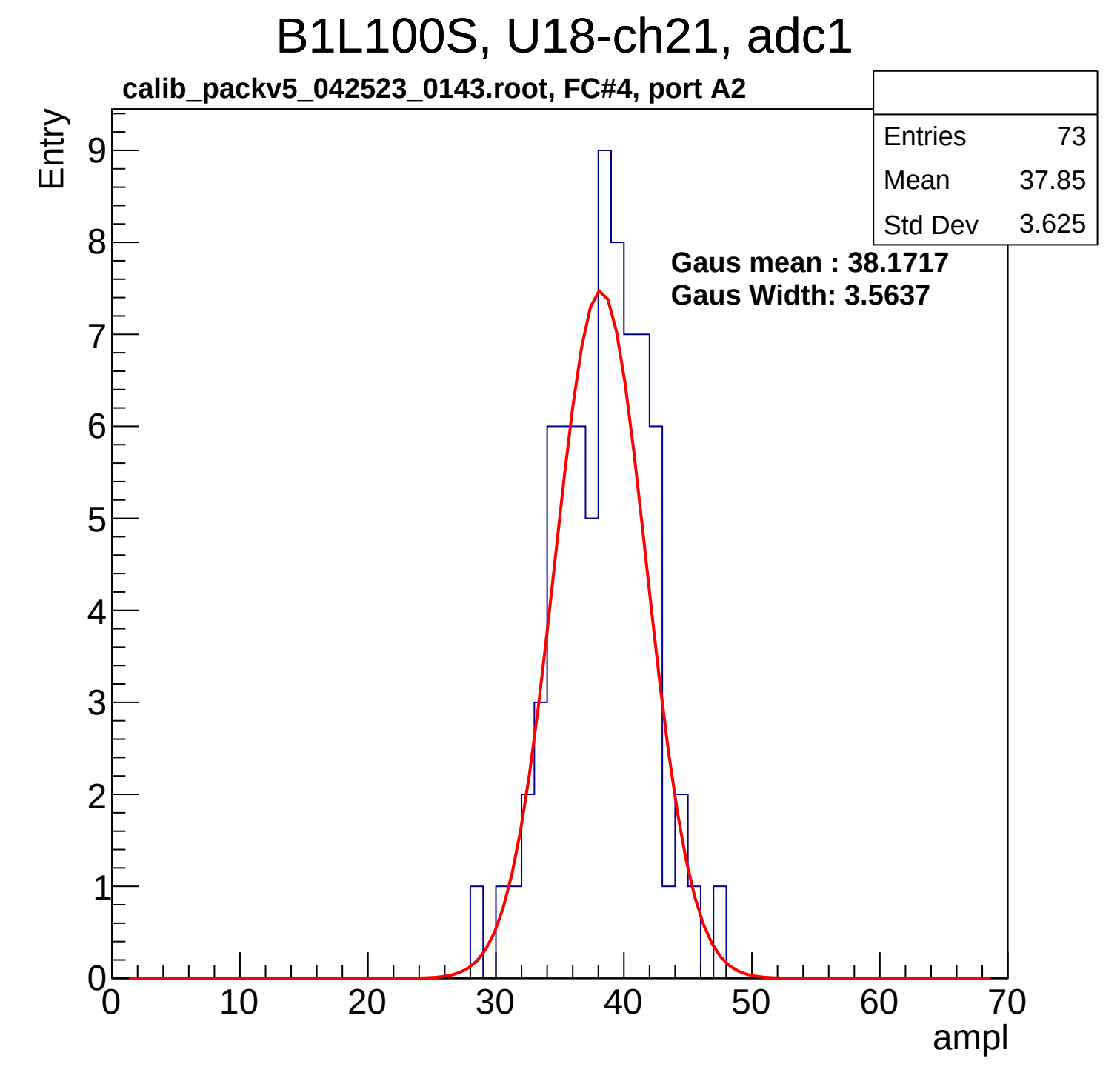

B1L100S, U18-ch20, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 56.09
Std Dev 3.124
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

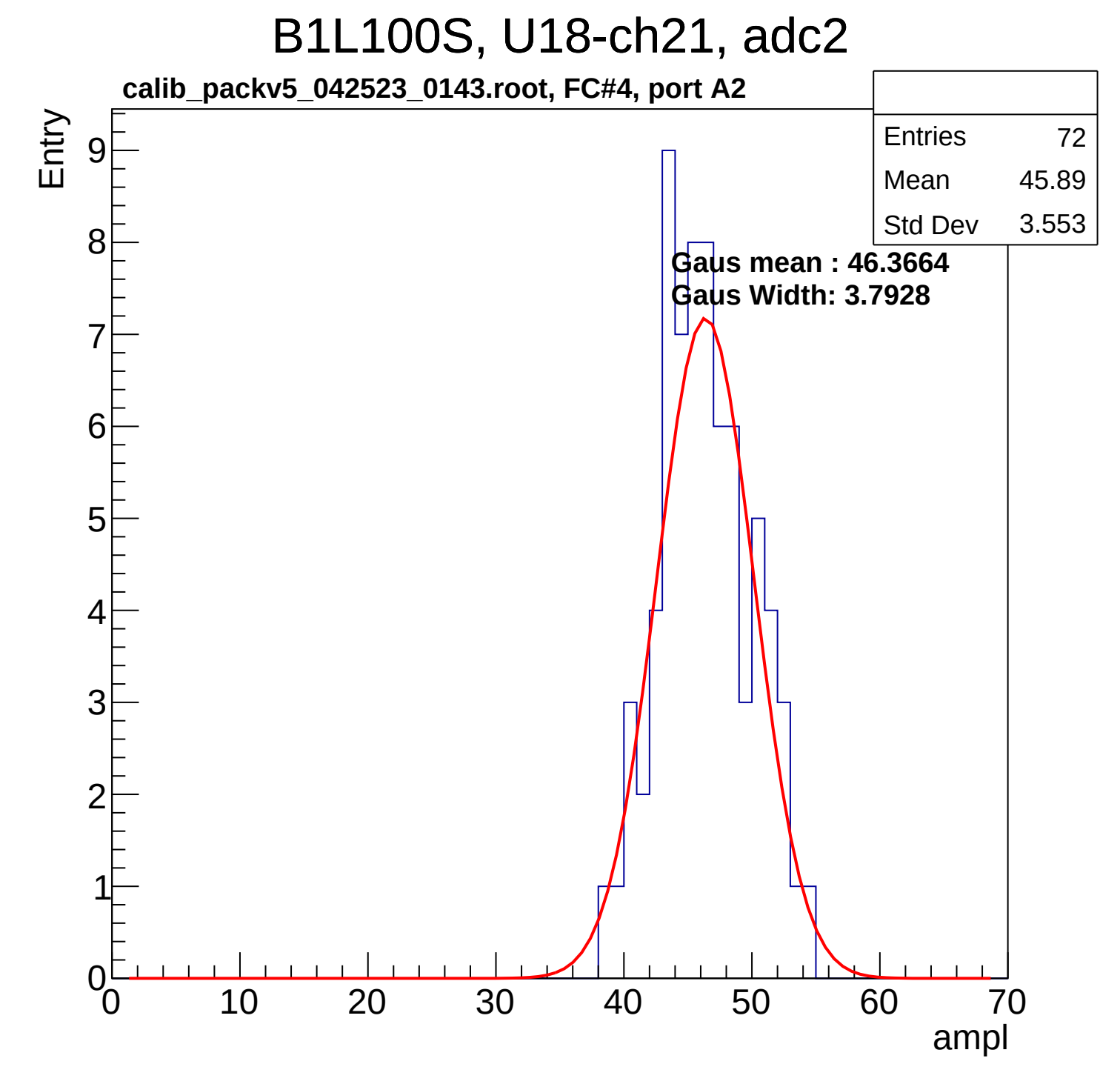

B1L100S, U18-ch20, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 59.12
Std Dev 8.883
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

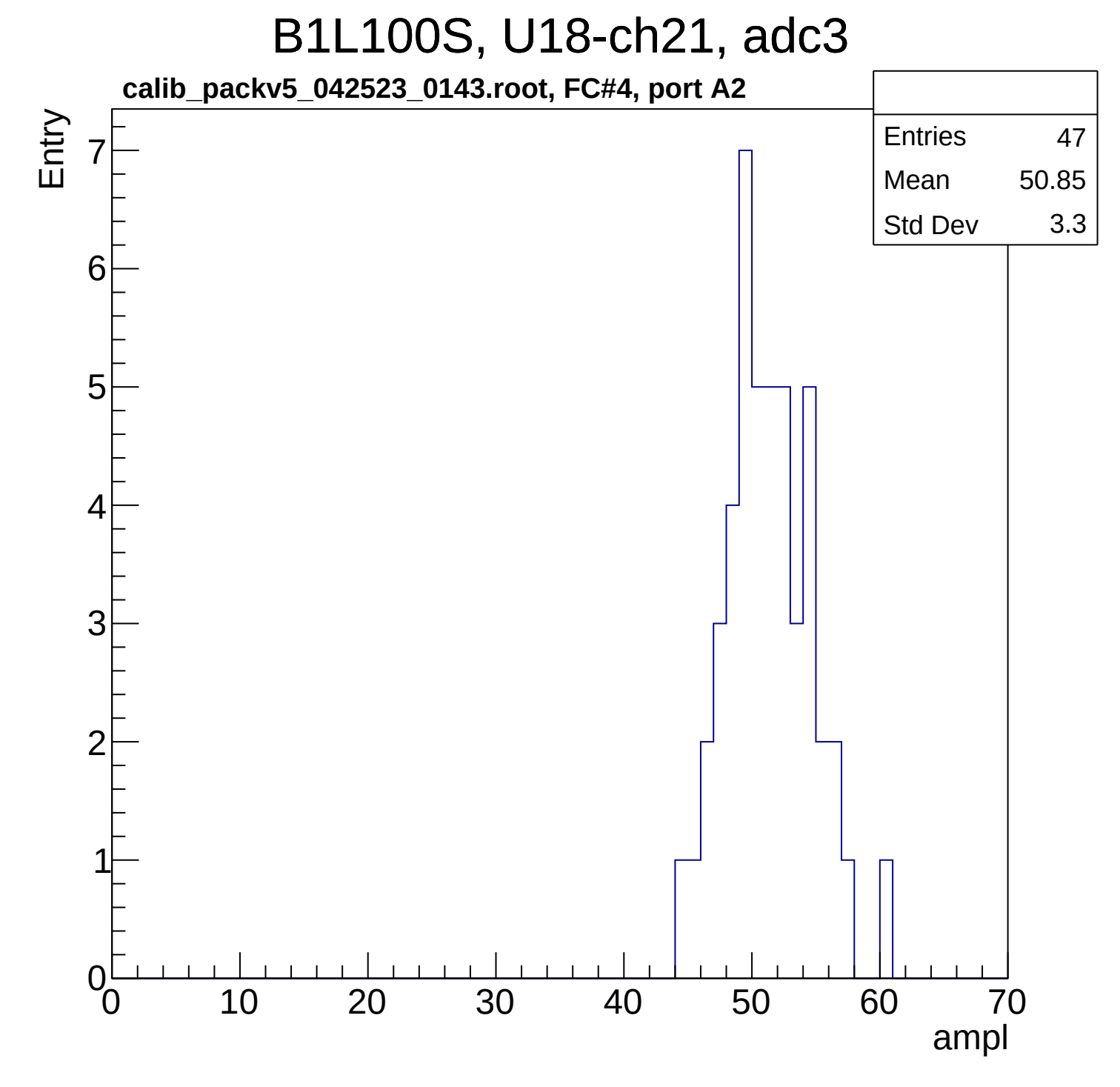

B1L100S, U18-ch20, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 61
Std Dev 2
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

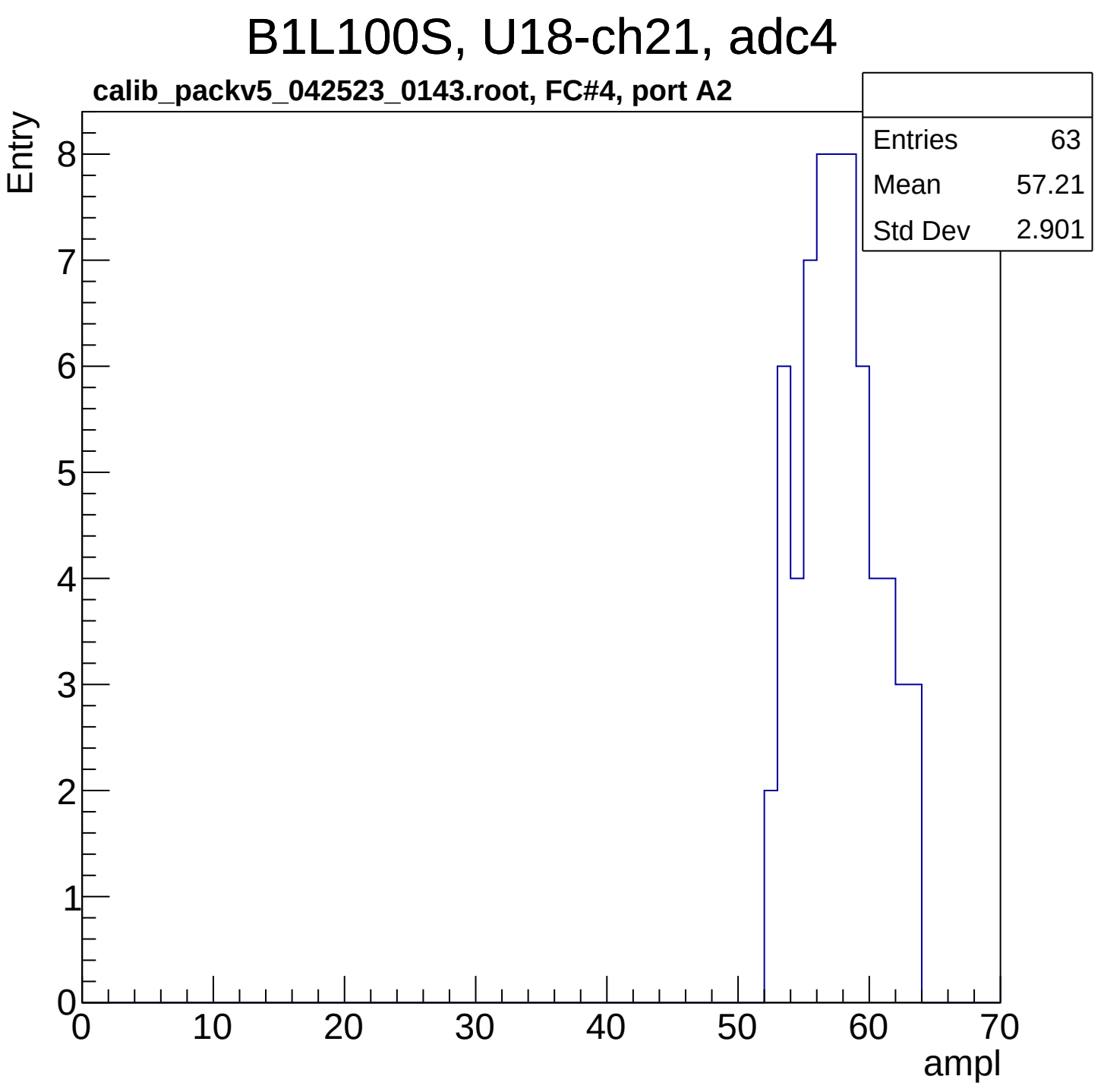

B1L100S, U18-ch20, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

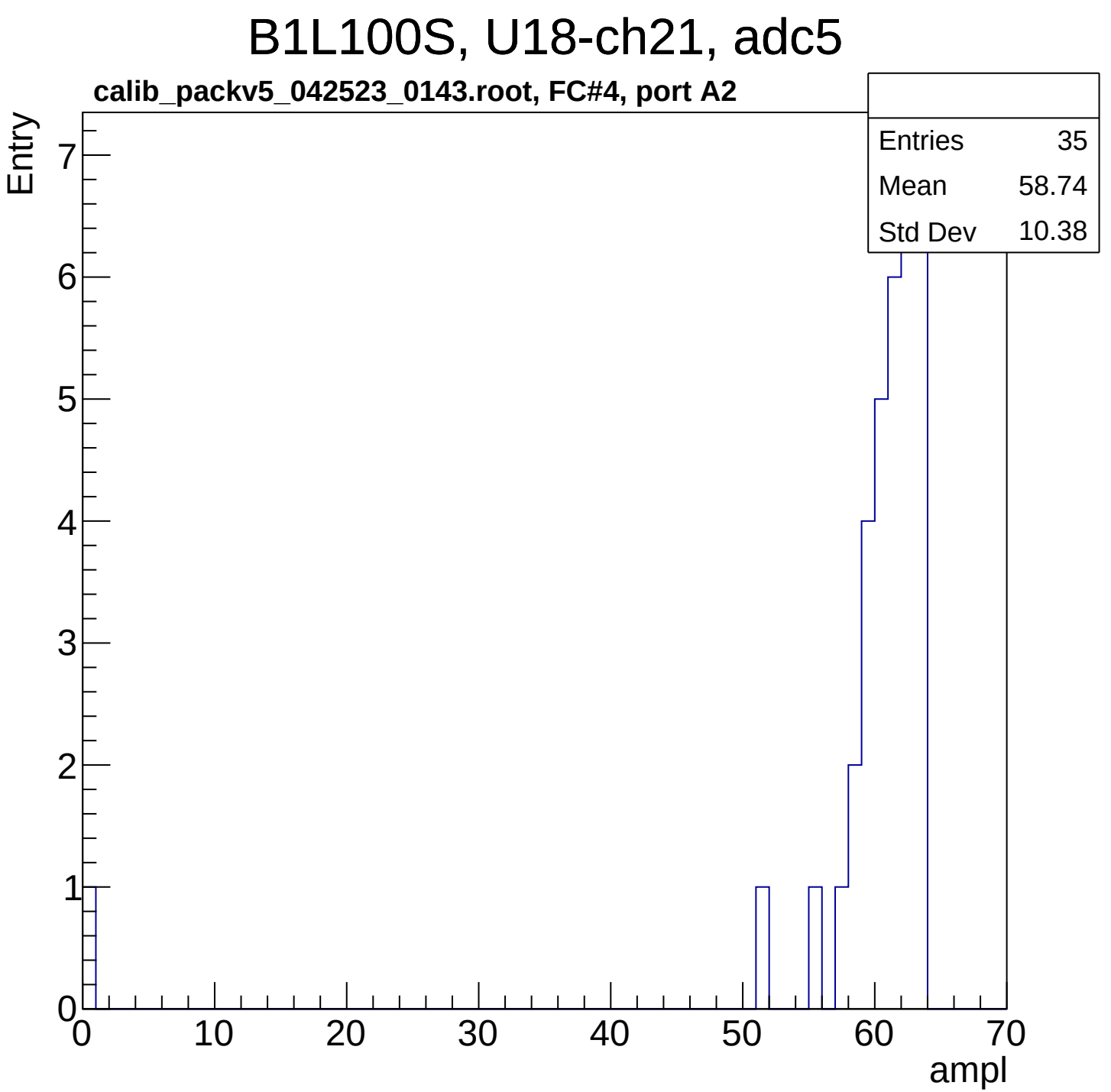

B1L100S, U18-ch21, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 31.37
Std Dev 4.029
Gaus mean : 32.2864
Gaus Width: 4.6371
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

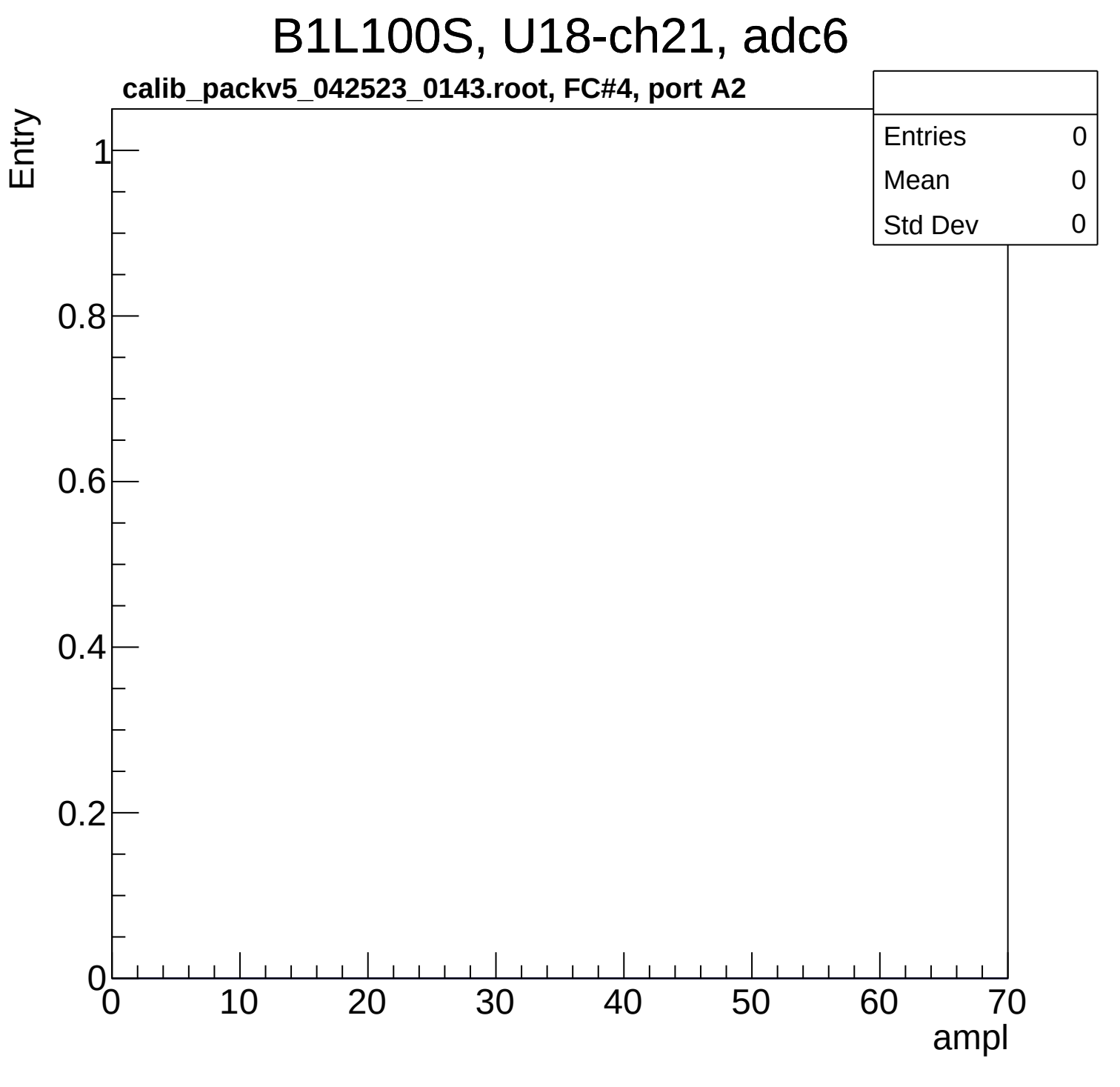

B1L100S, U18-ch21, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 37.85
Std Dev 3.625
Gaus mean : 38.1717
Gaus Width: 3.5637
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

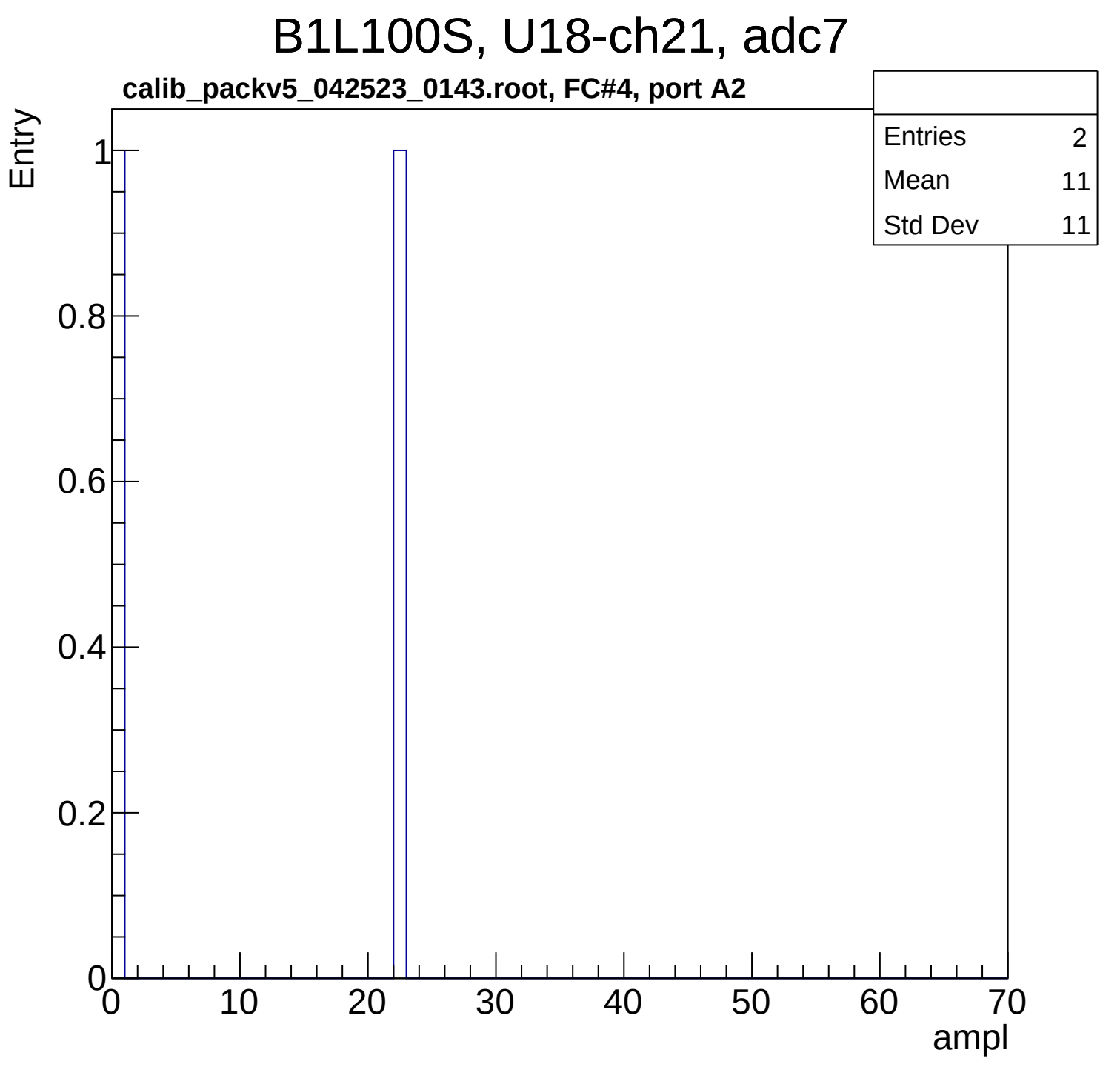

B1L100S, U18-ch21, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 45.89
Std Dev 3.553
Gaus mean : 46.3664
Gaus Width: 3.7928
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

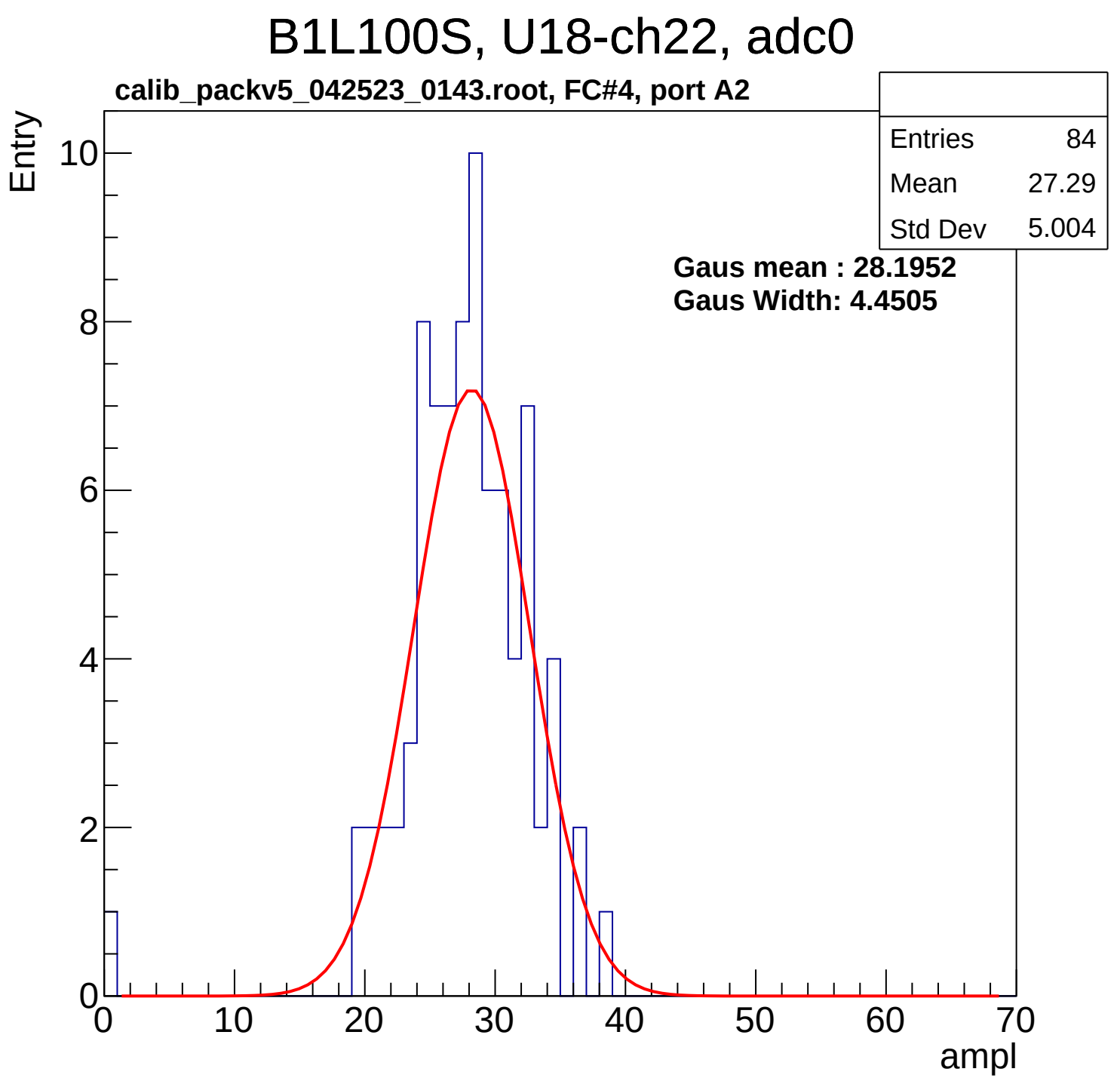

B1L100S, U18-ch21, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 50.85
Std Dev 3.3
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

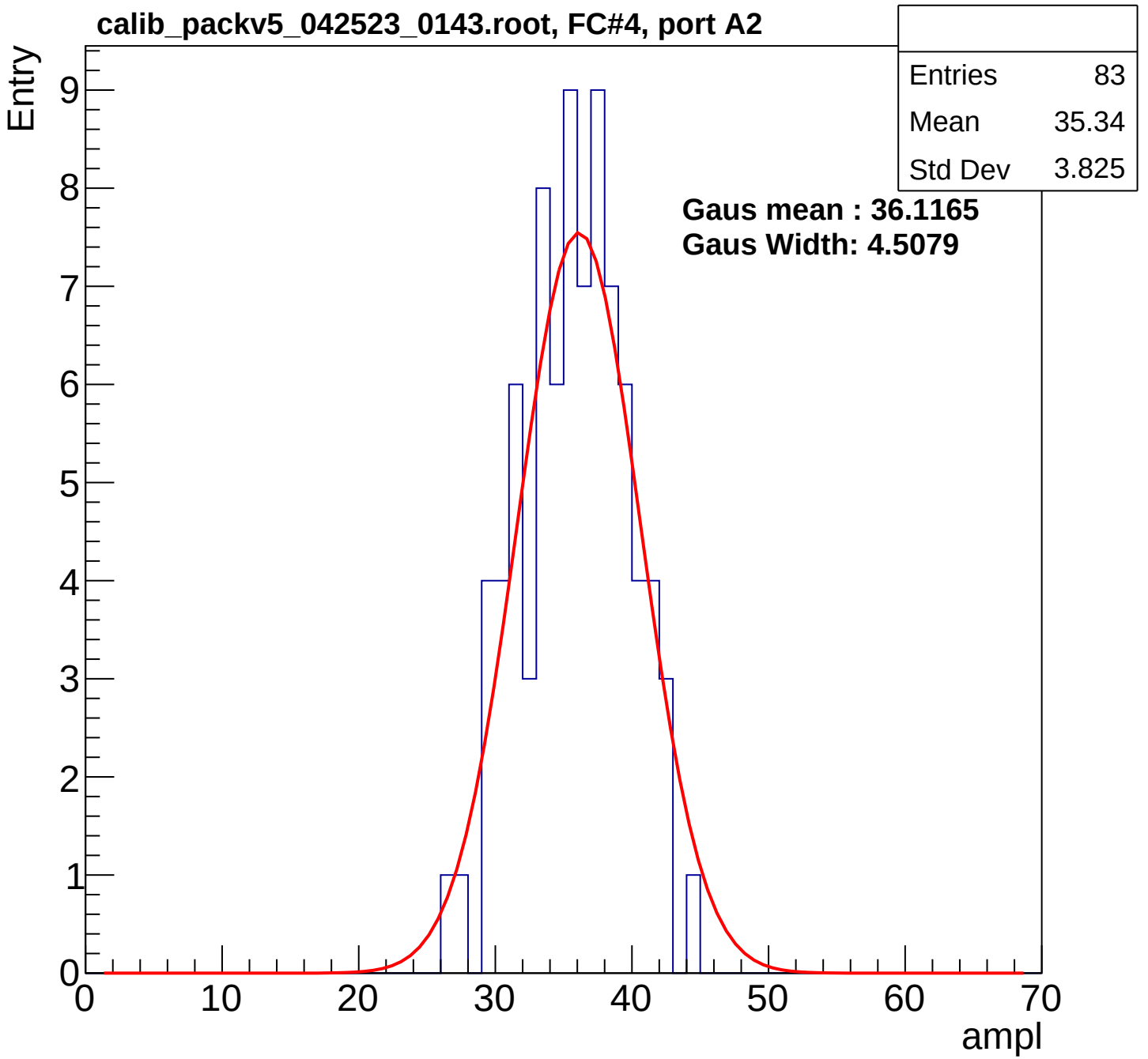

B1L100S, U18-ch21, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 57.21
Std Dev 2.901
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

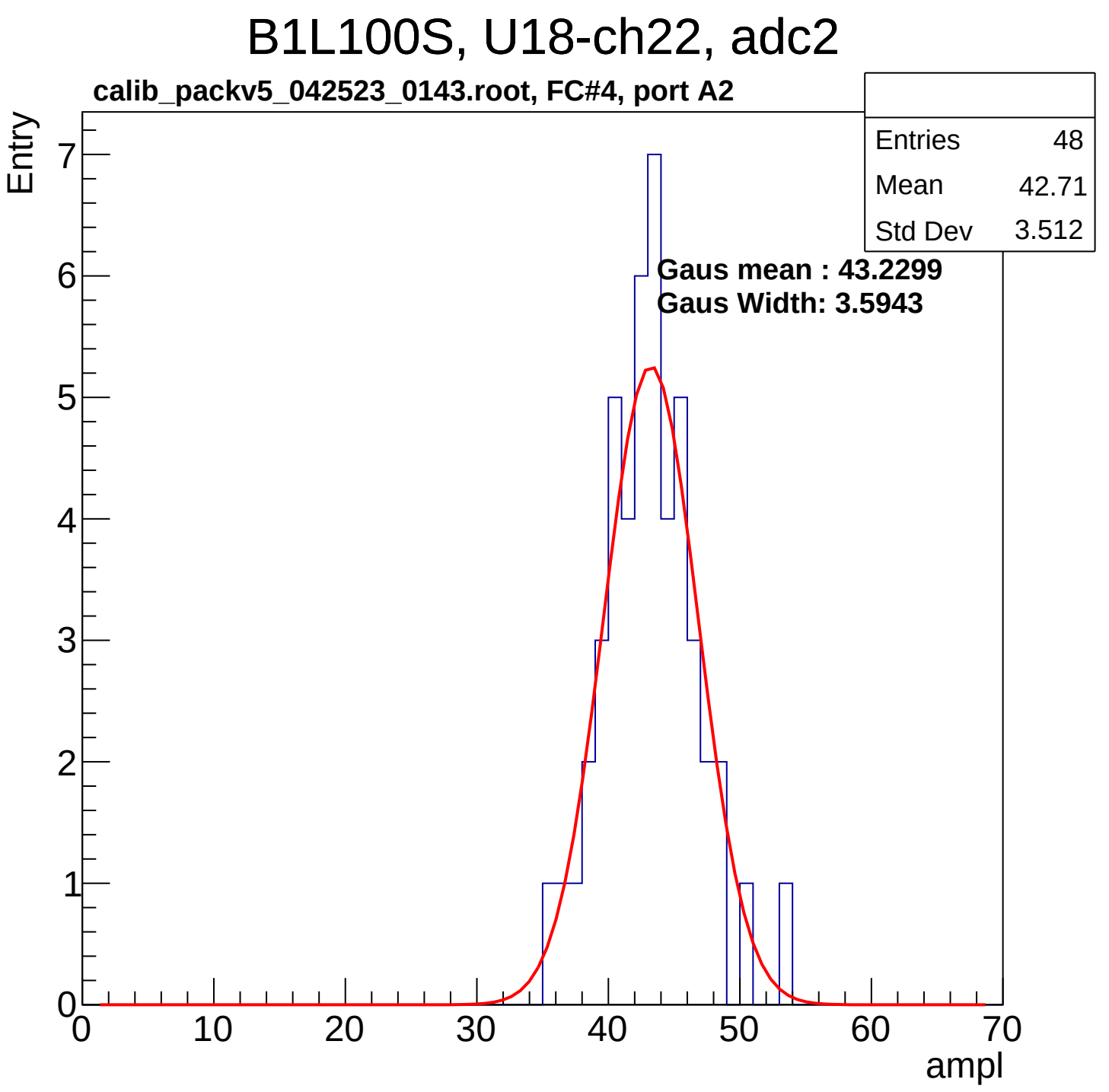

B1L100S, U18-ch21, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 35
Mean 58.74
Std Dev 10.38
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

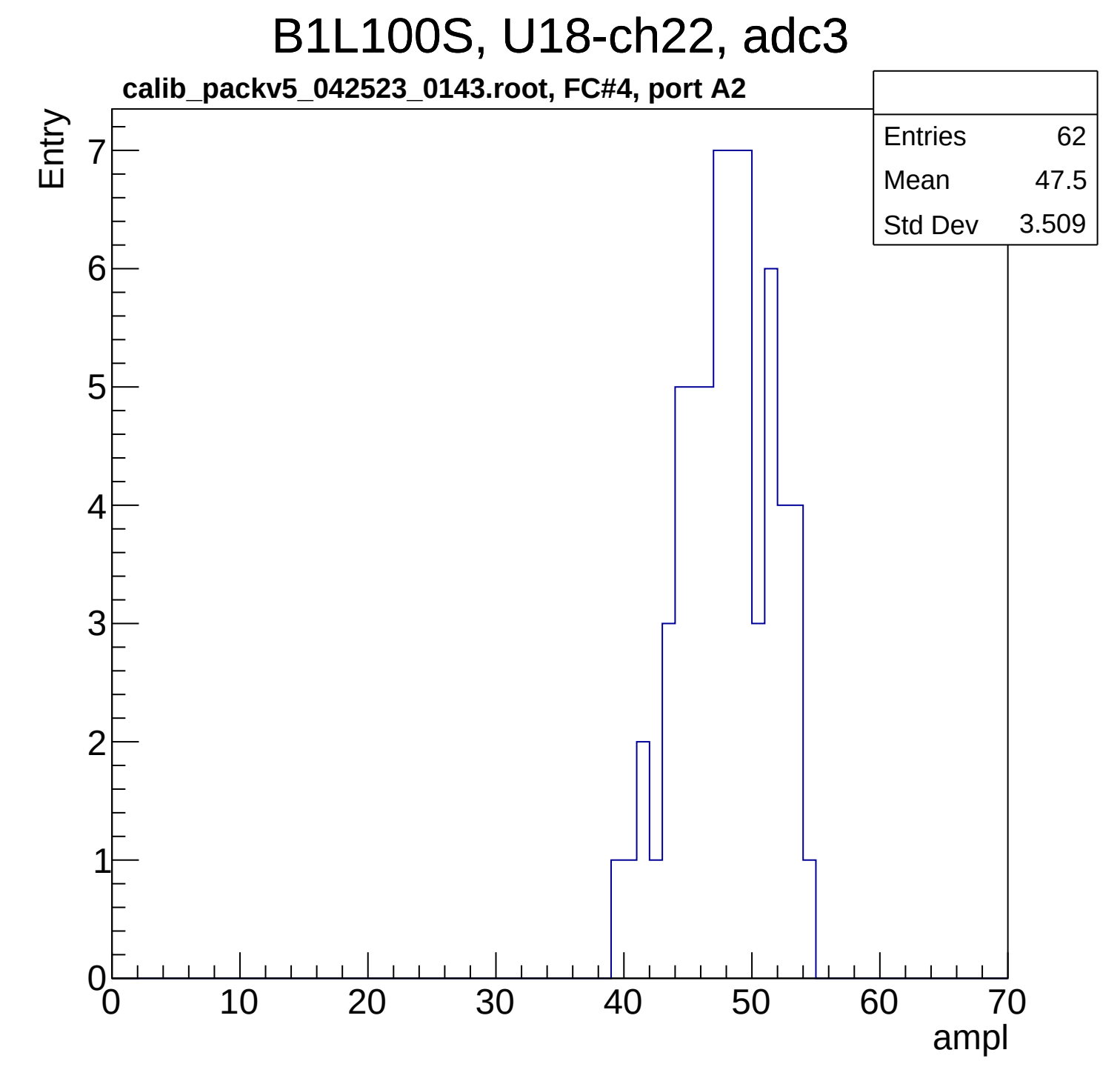

B1L100S, U18-ch21, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

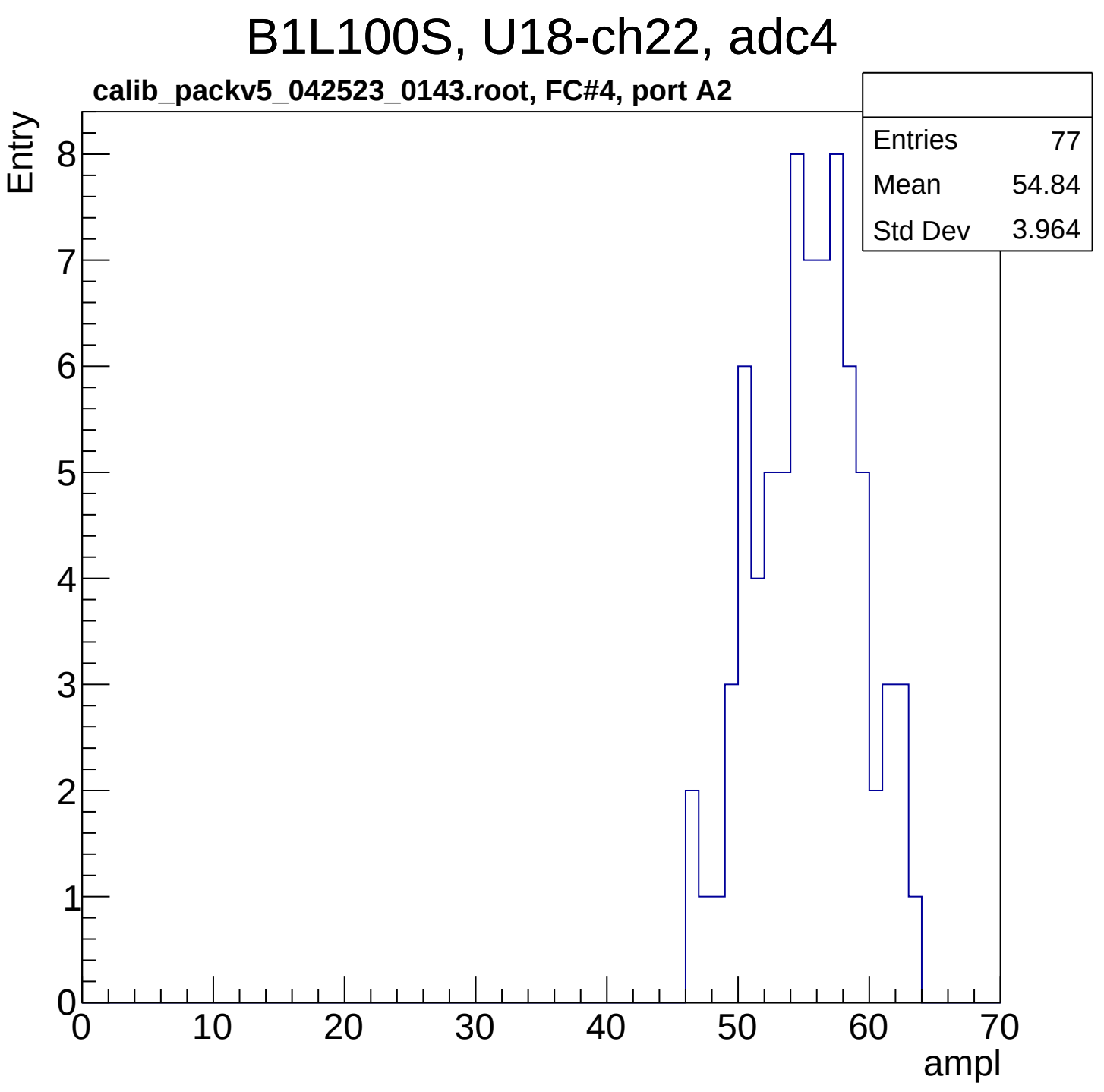

B1L100S, U18-ch21, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 11
Std Dev 11
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

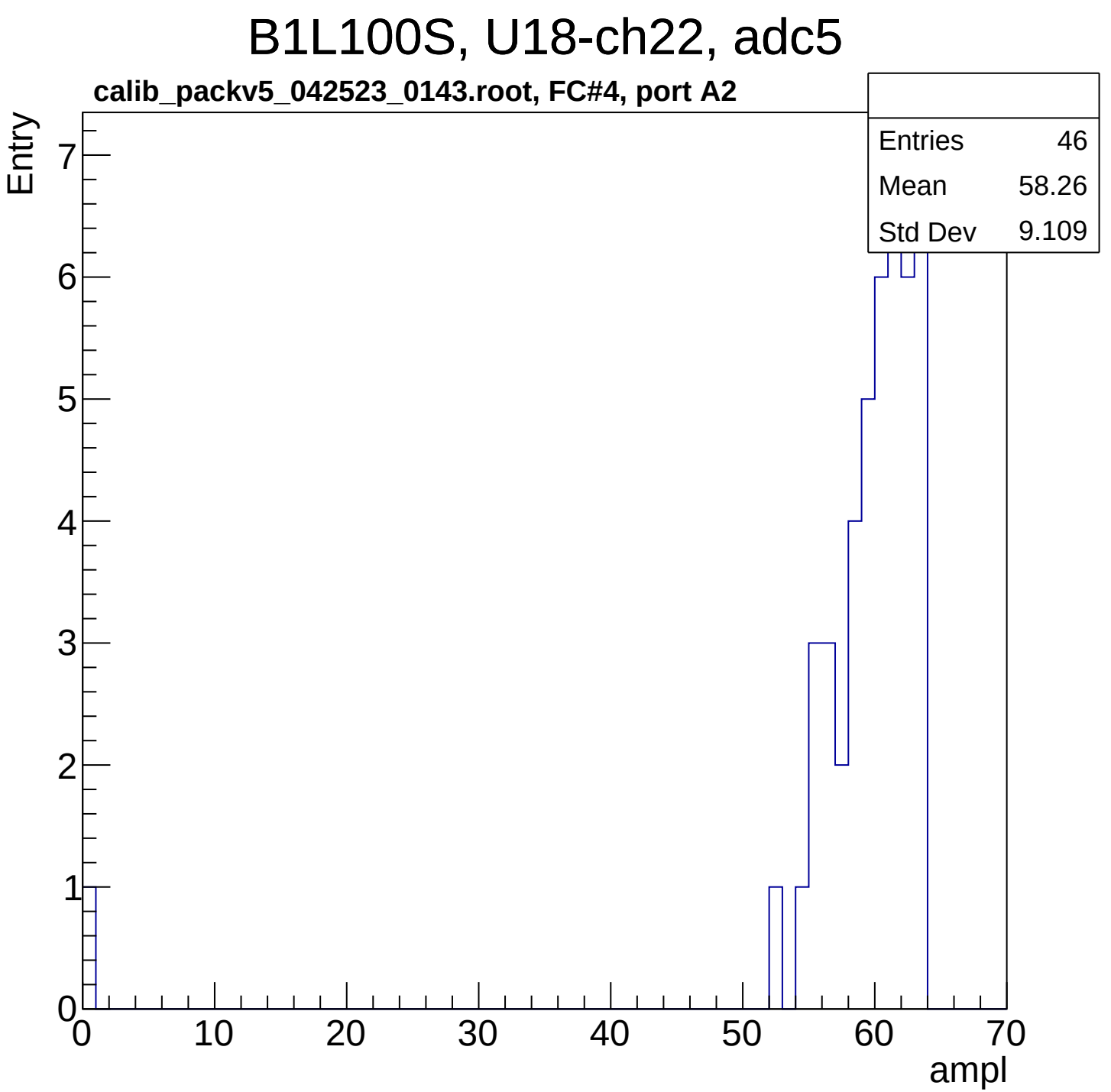

B1L100S, U18-ch22, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 84
Mean 27.29
Std Dev 5.004
Gaus mean : 28.1952
Gaus Width: 4.4505
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

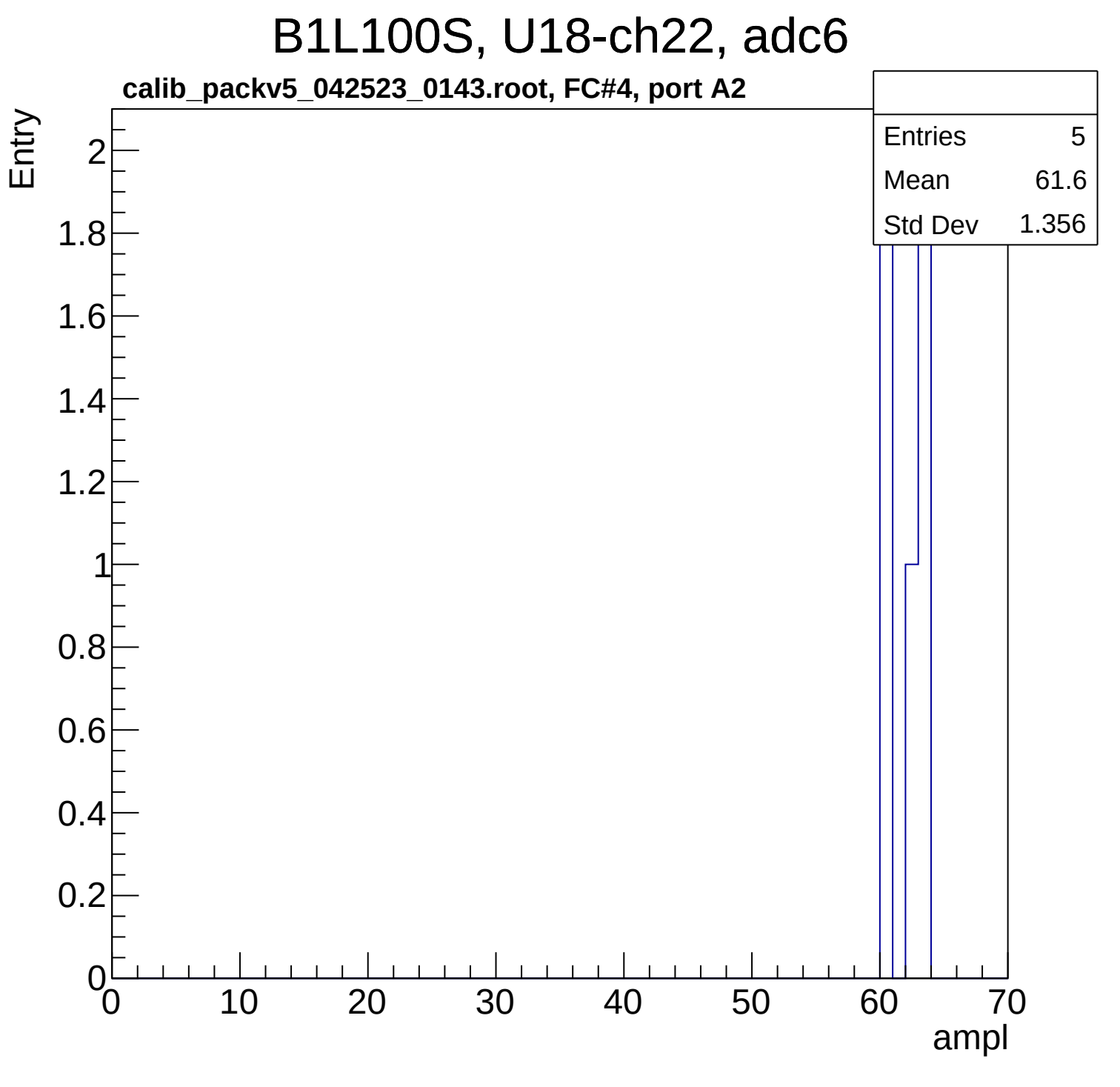

B1L100S, U18-ch22, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 83
Mean 35.34
Std Dev 3.825
Gaus mean : 36.1165
Gaus Width: 4.5079
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

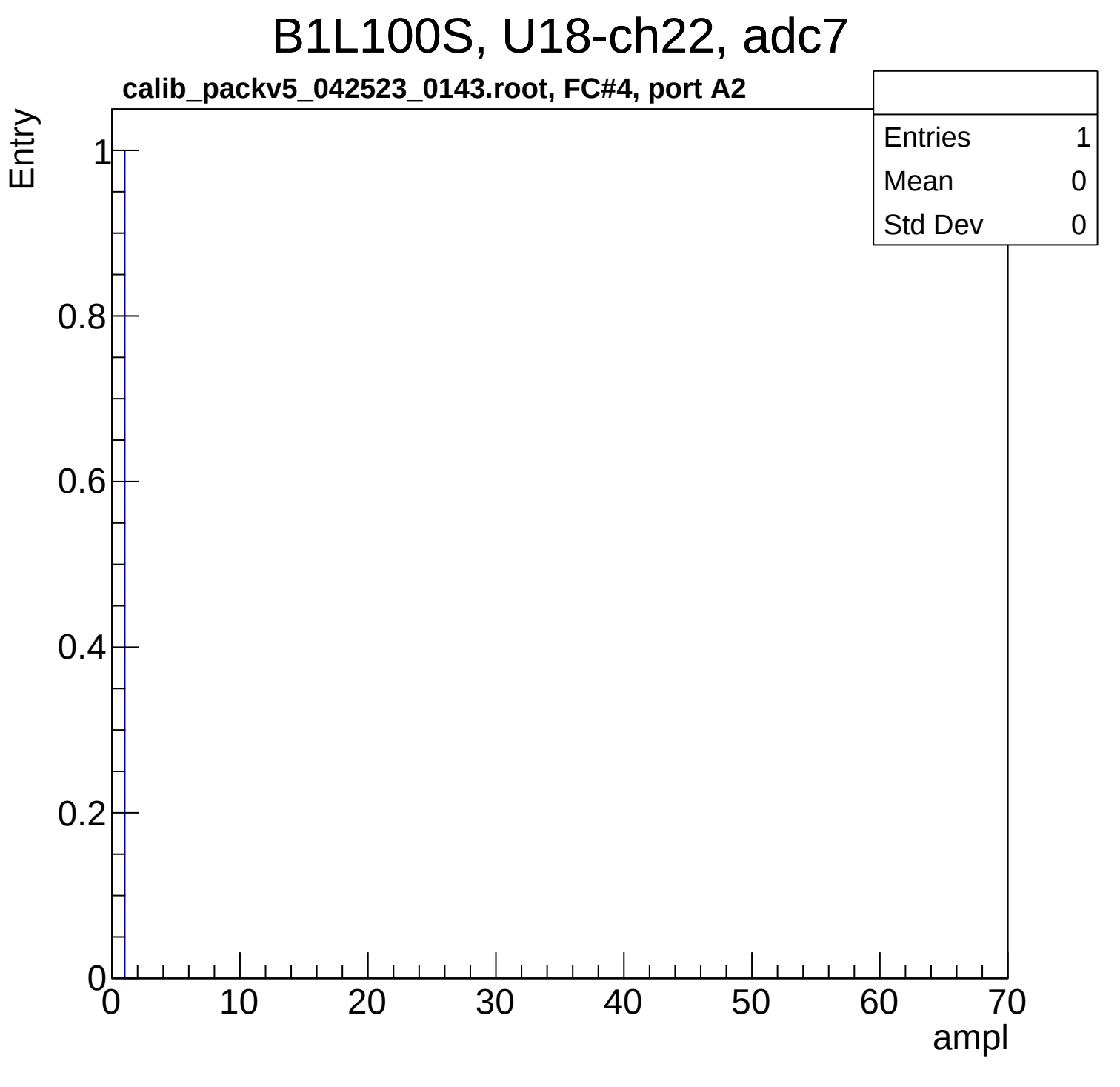

B1L100S, U18-ch22, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 42.71
Std Dev 3.512
Gaus mean : 43.2299
Gaus Width: 3.5943
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

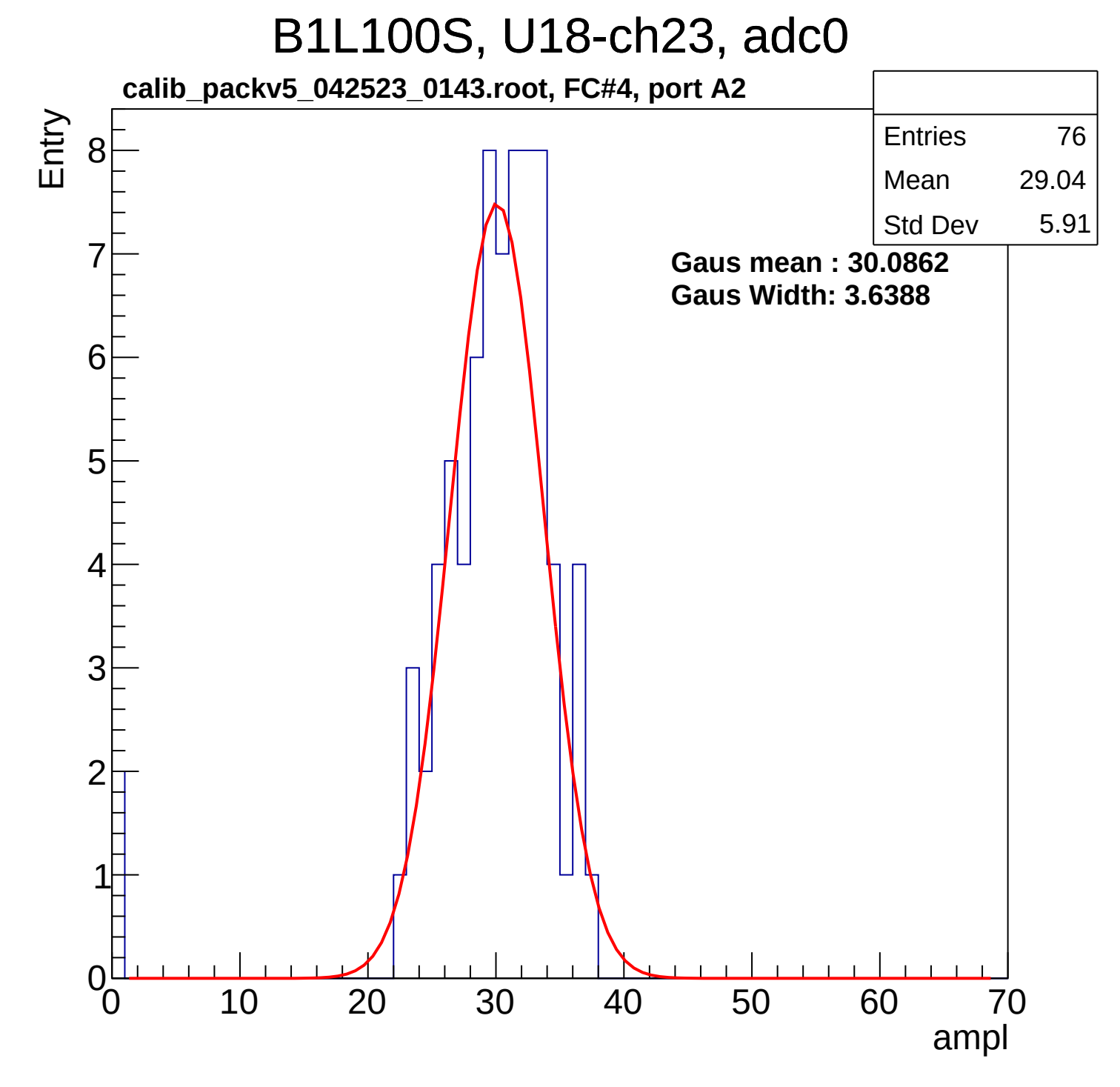

B1L100S, U18-ch22, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 47.5
Std Dev 3.509
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

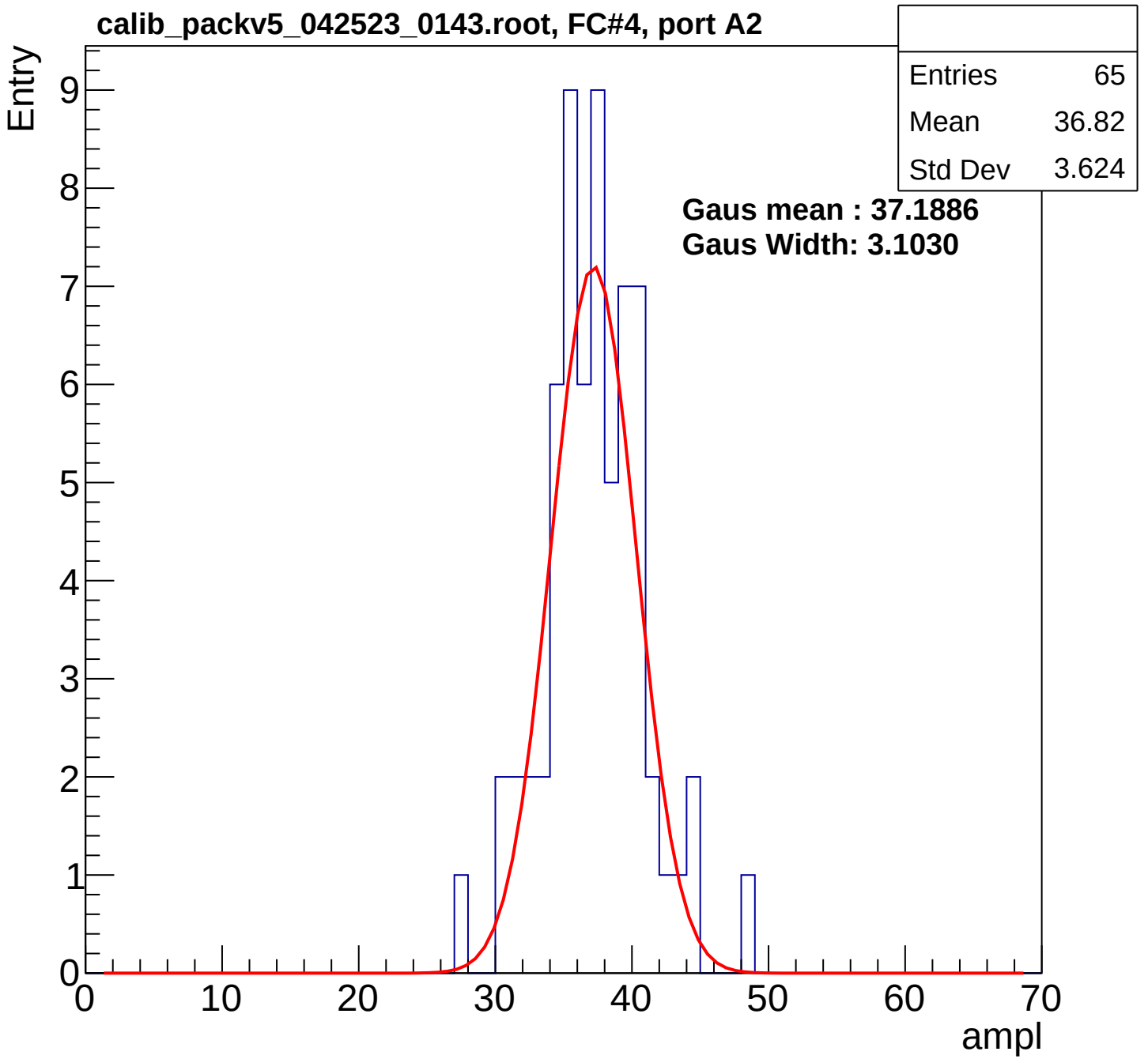

B1L100S, U18-ch22, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 54.84
Std Dev 3.964
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

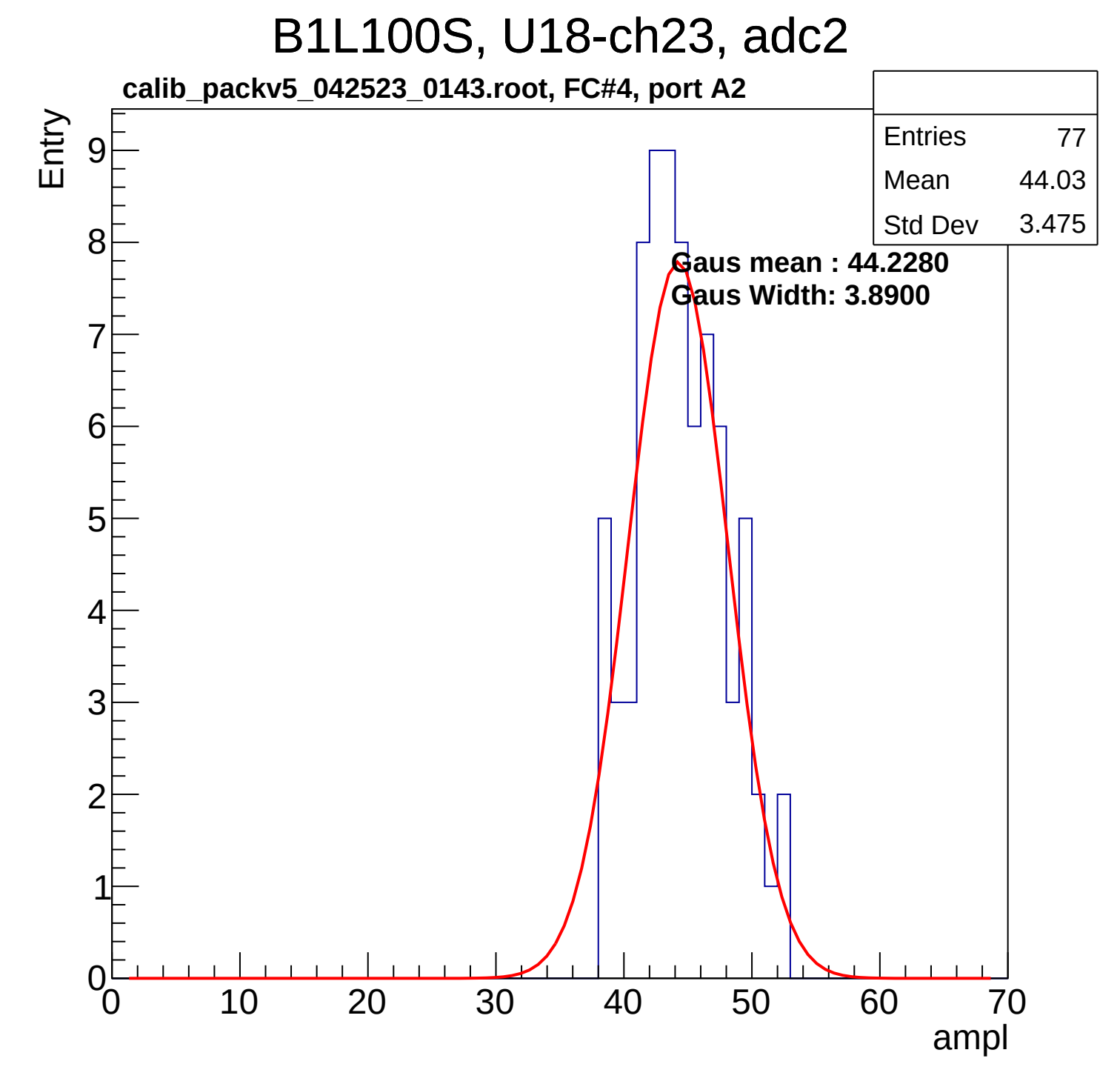

B1L100S, U18-ch22, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 58.26
Std Dev 9.109
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

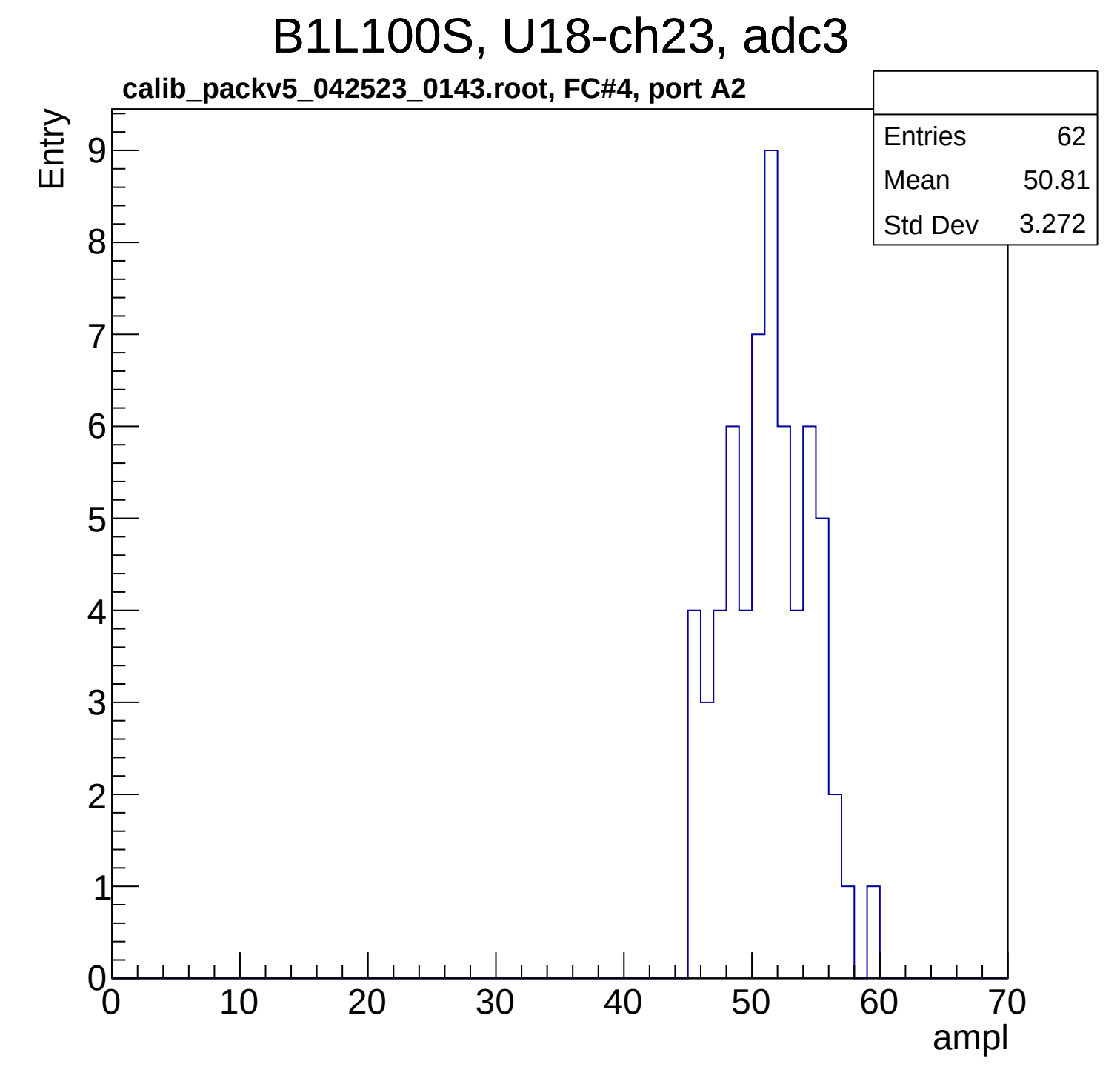

B1L100S, U18-ch22, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 5
Mean 61.6
Std Dev 1.356
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

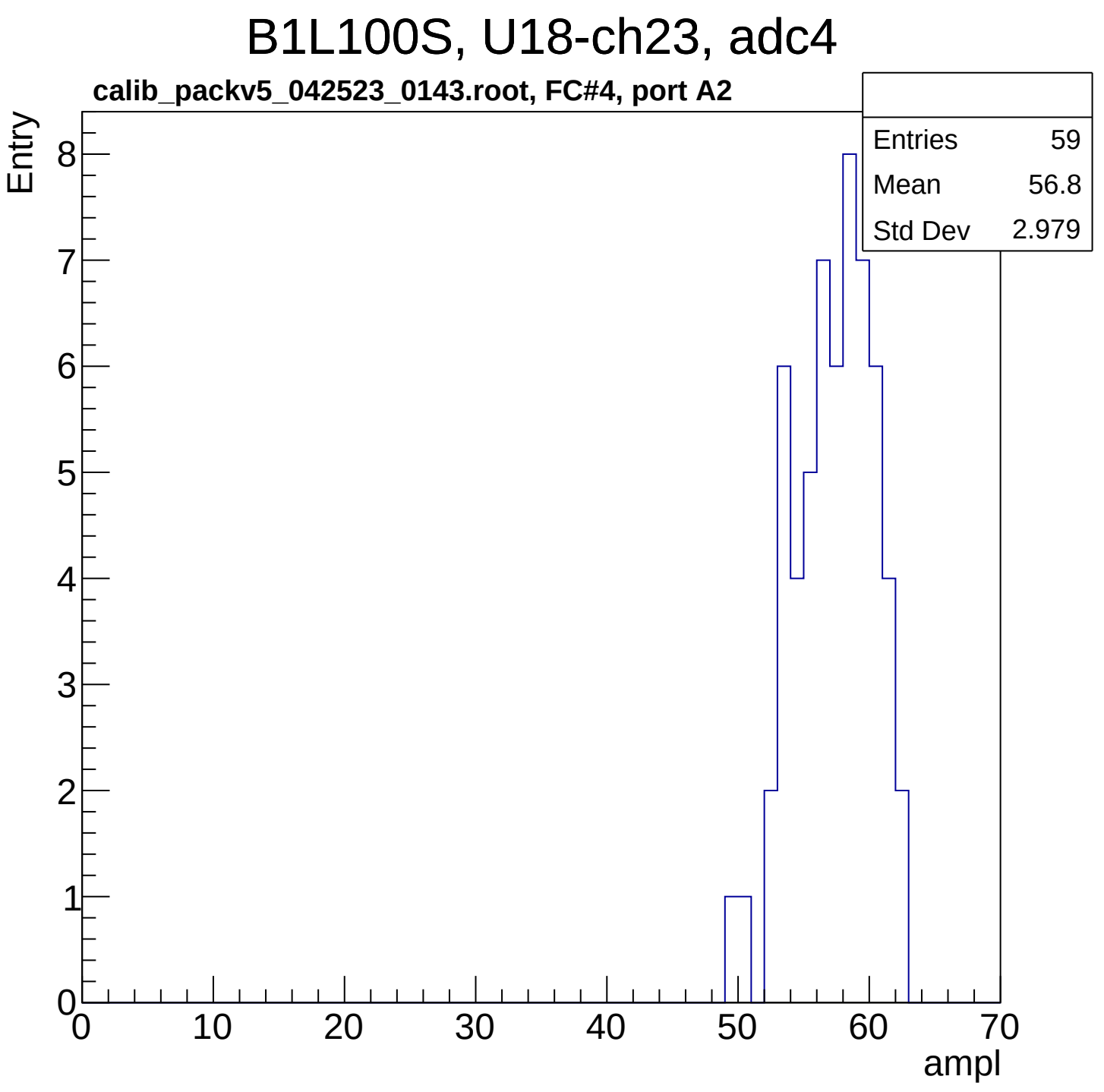

B1L100S, U18-ch22, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

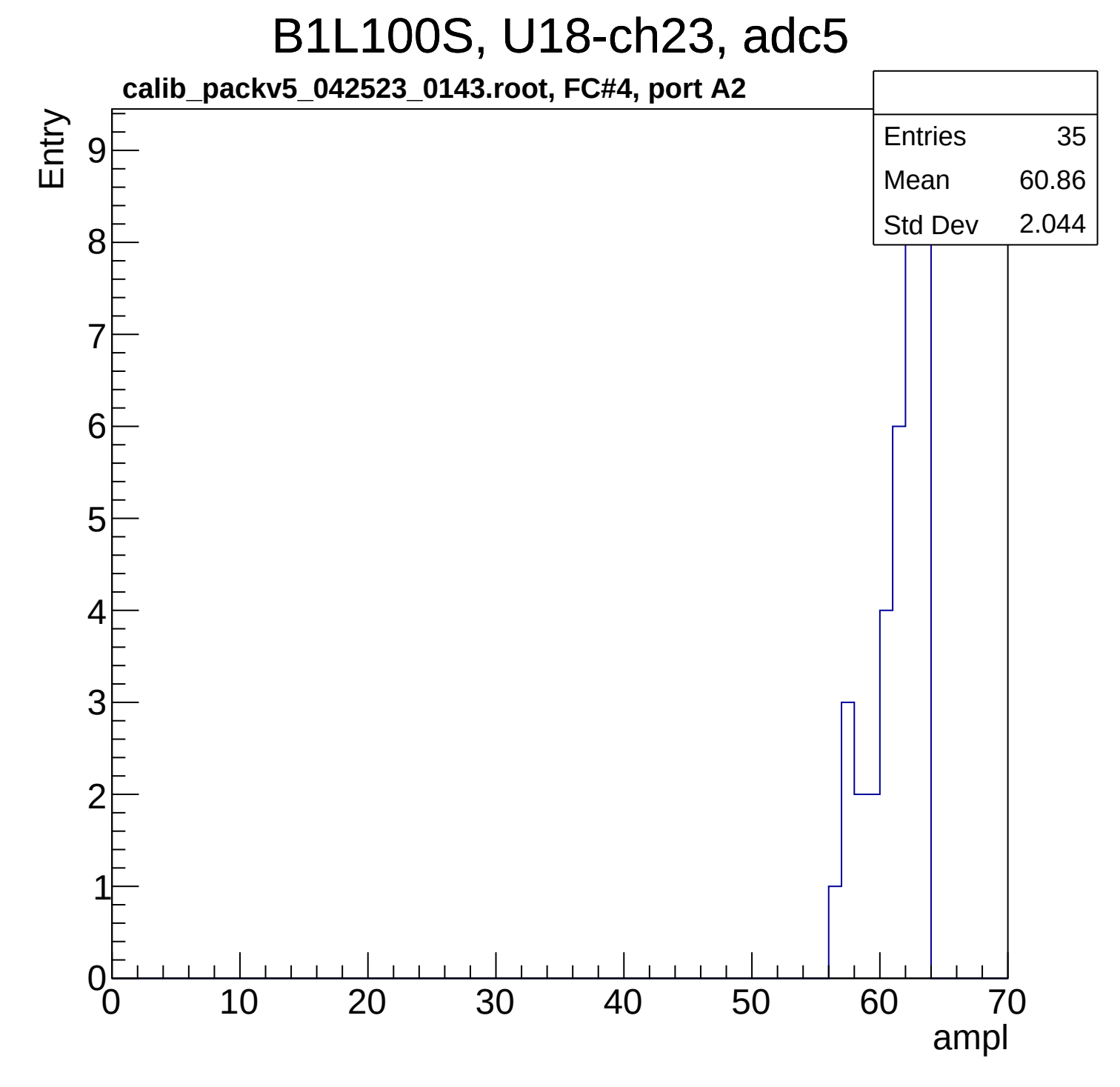

B1L100S, U18-ch23, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 29.04
Std Dev 5.91
Gaus mean : 30.0862
Gaus Width: 3.6388
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

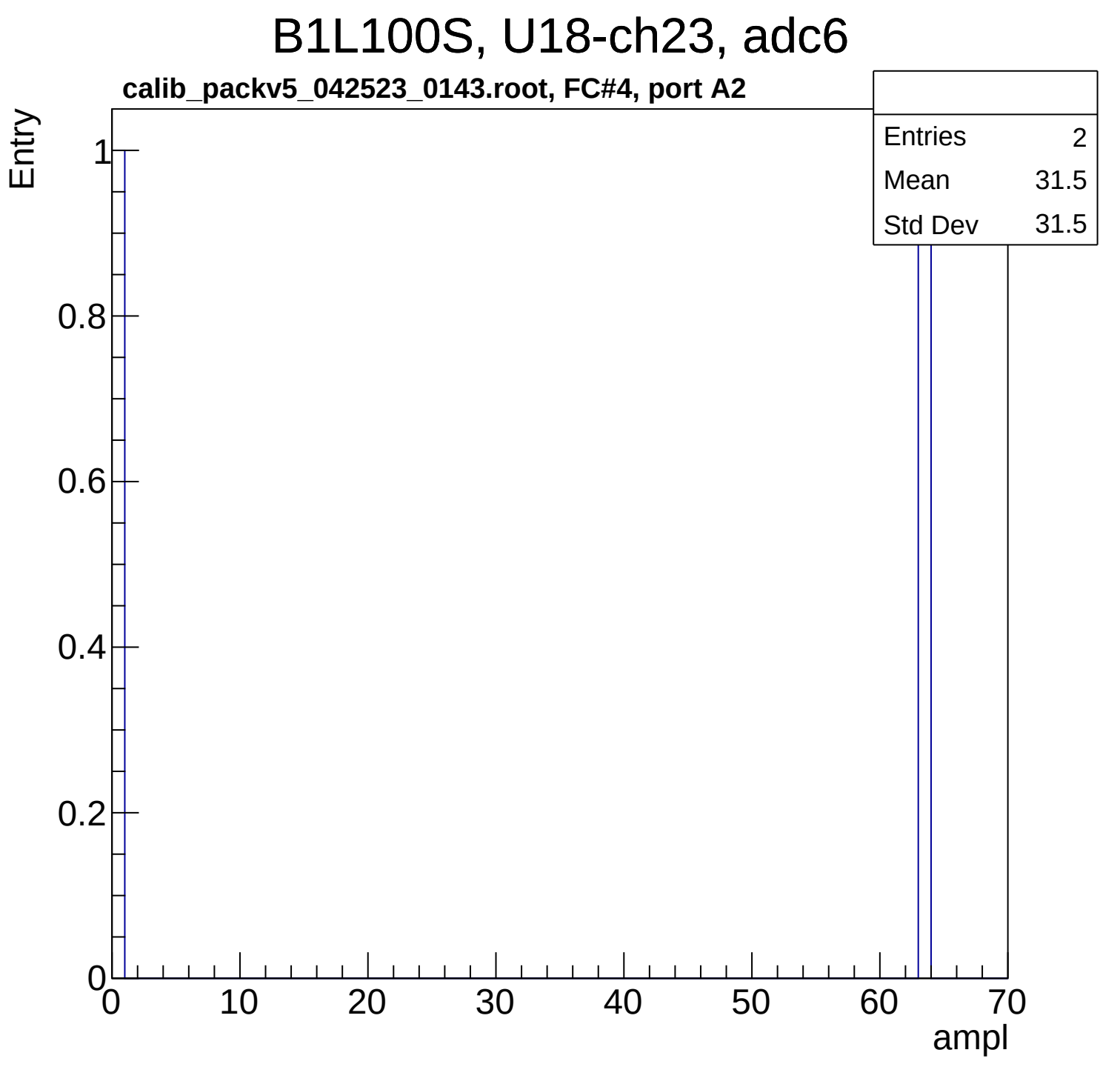

B1L100S, U18-ch23, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 36.82
Std Dev 3.624
Gaus mean : 37.1886
Gaus Width: 3.1030
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

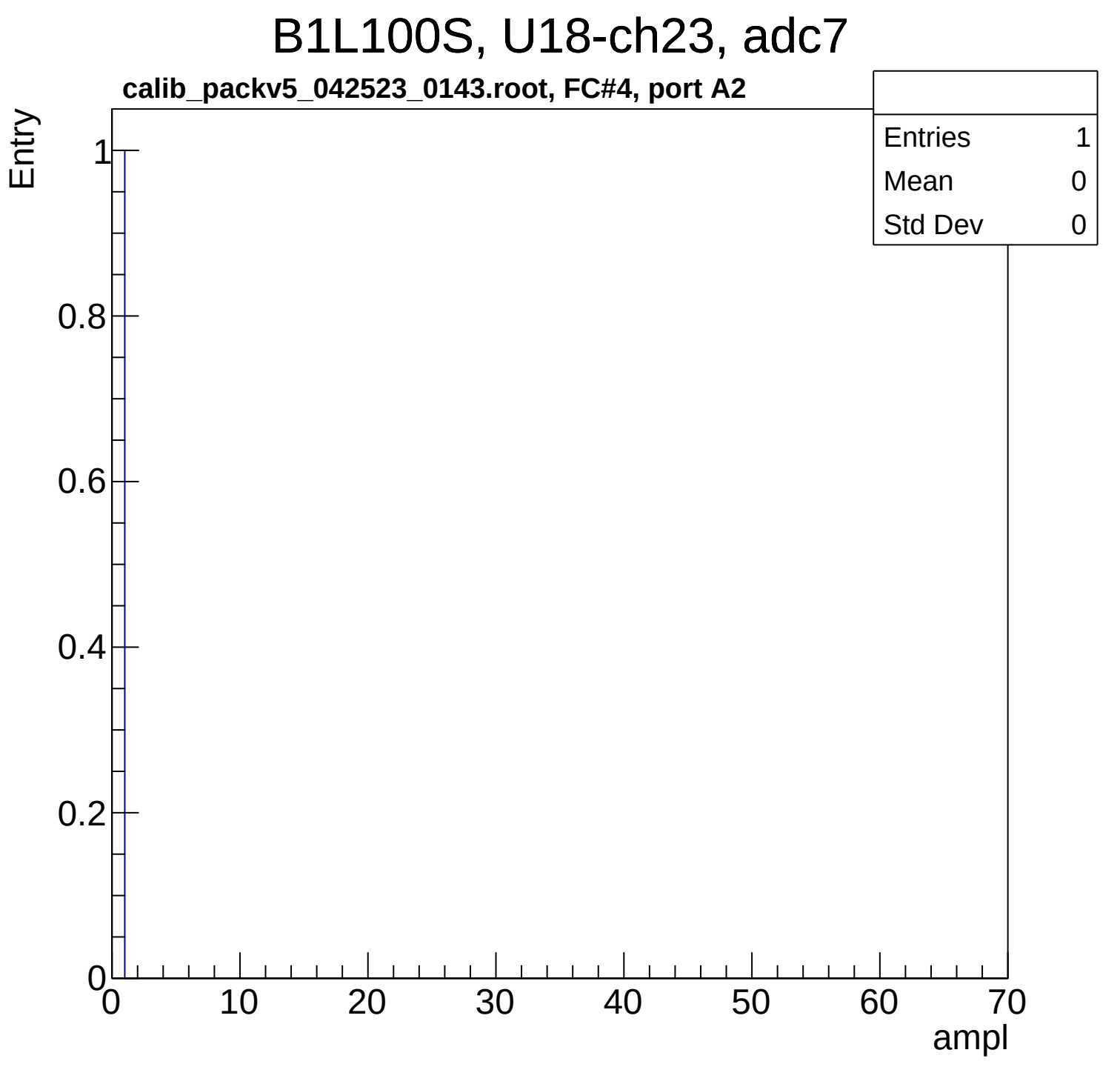

B1L100S, U18-ch23, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 44.03
Std Dev 3.475
Gaus mean : 44.2280
Gaus Width: 3.8900
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

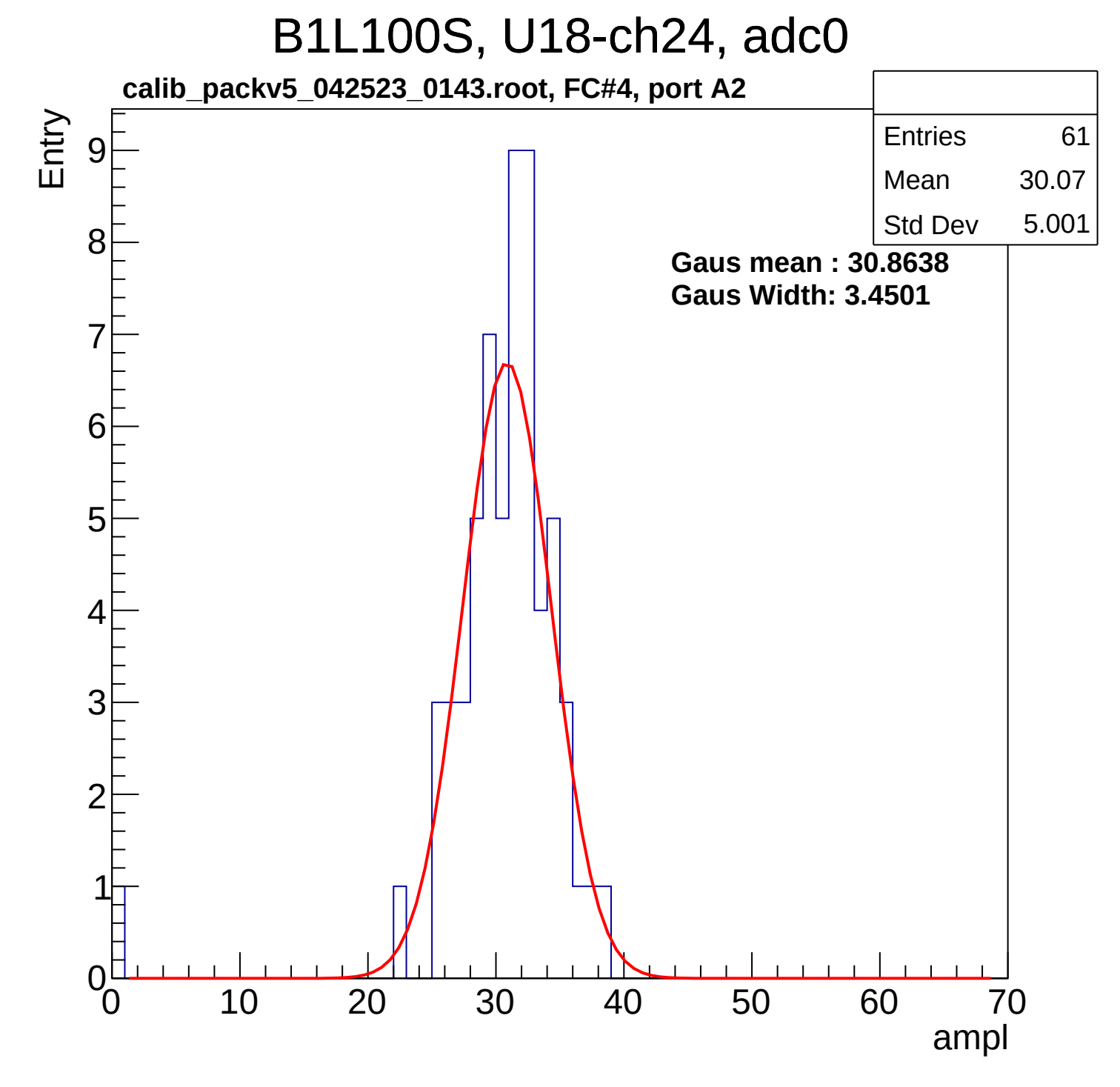

B1L100S, U18-ch23, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 50.81
Std Dev 3.272
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

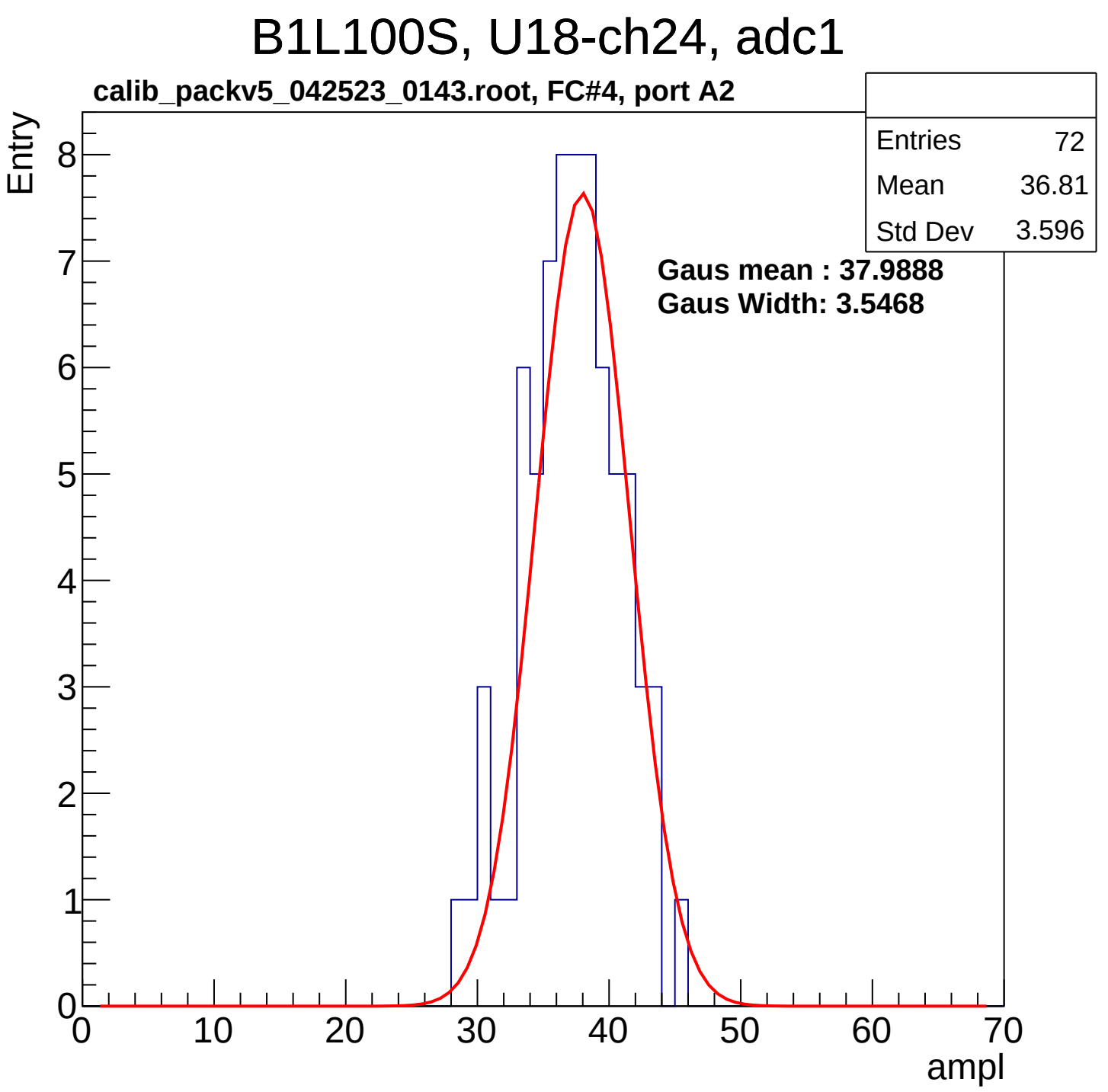

B1L100S, U18-ch23, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 56.8
Std Dev 2.979
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

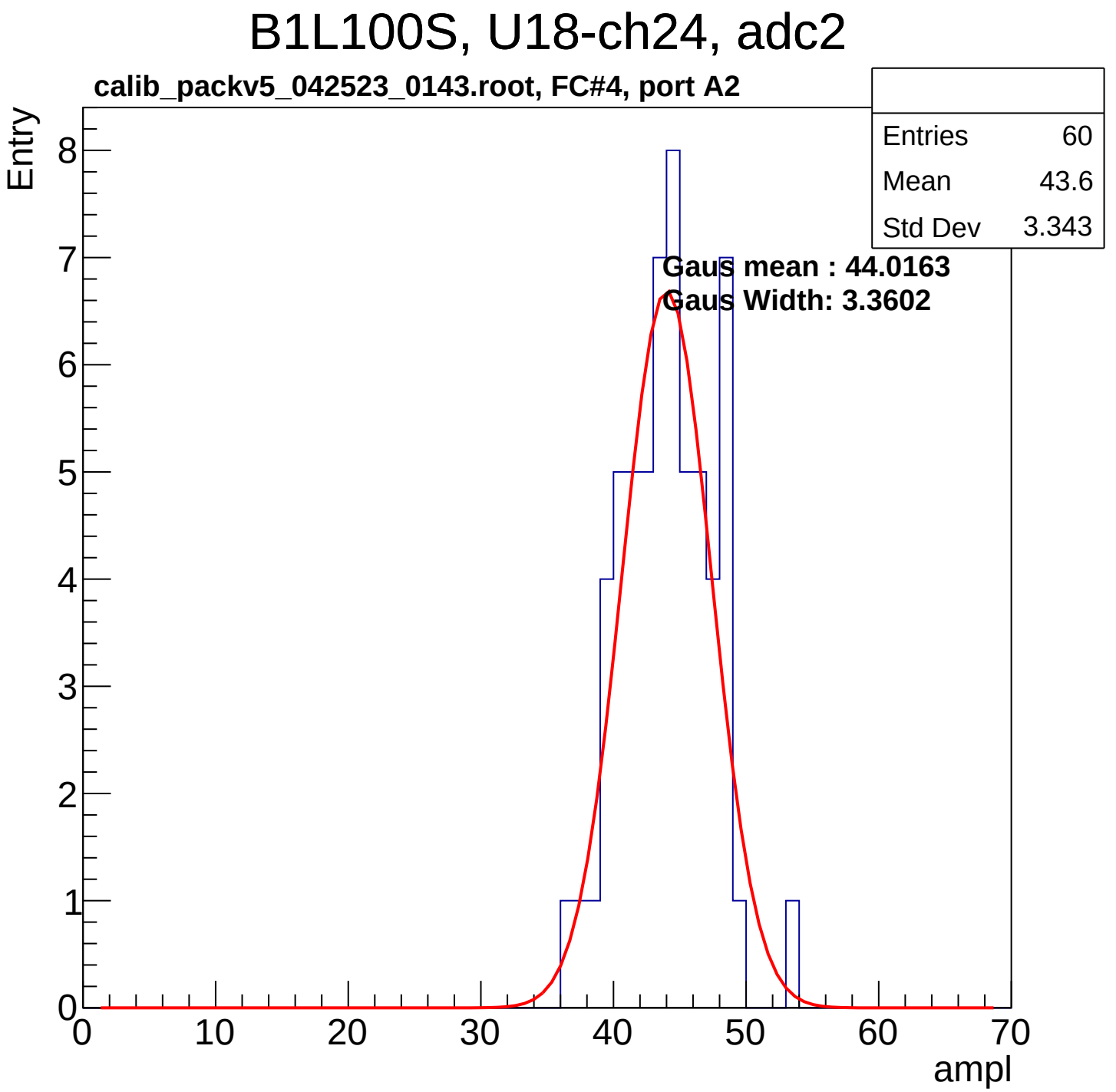

B1L100S, U18-ch23, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 35
Mean 60.86
Std Dev 2.044
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

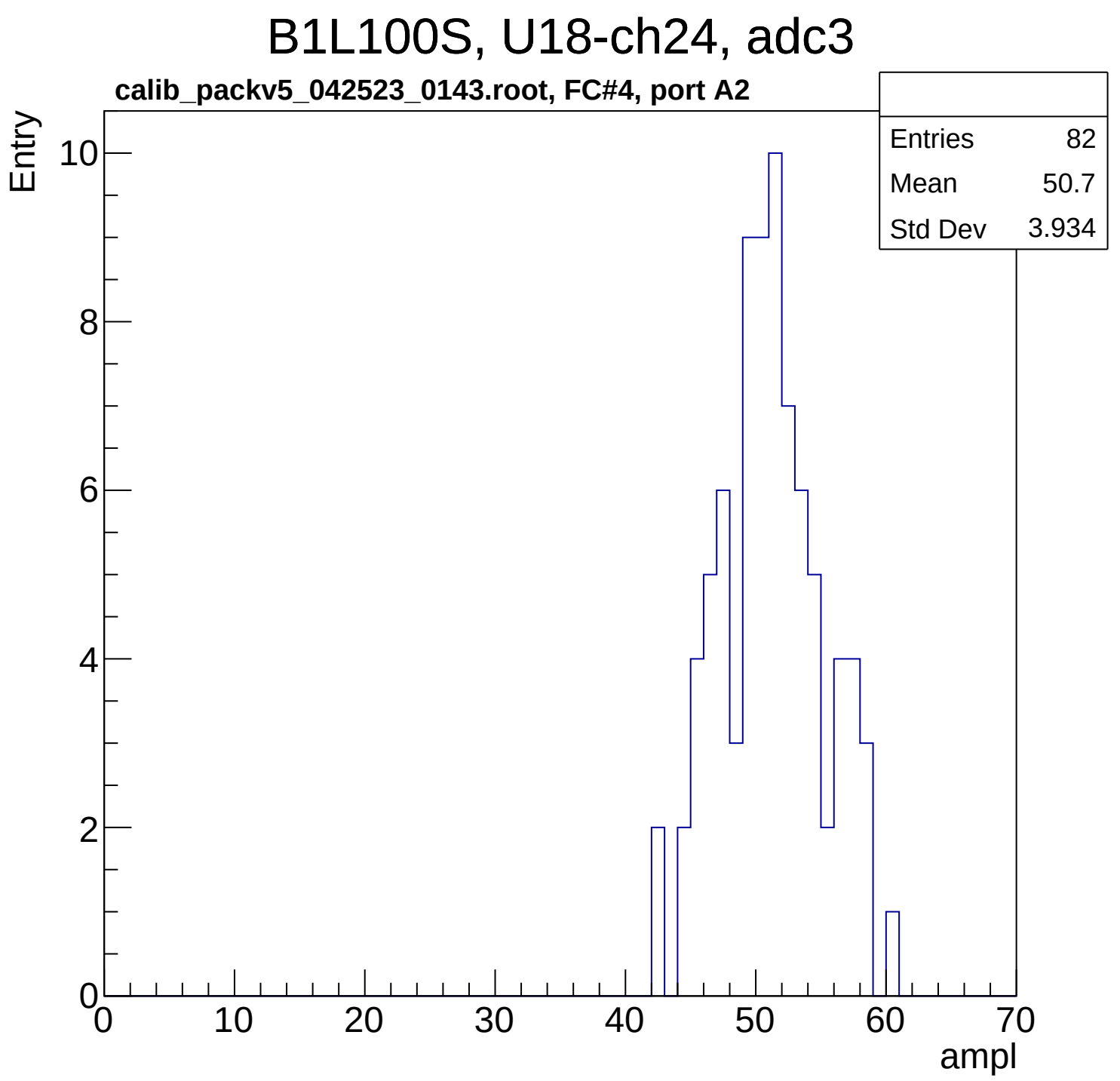

B1L100S, U18-ch23, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

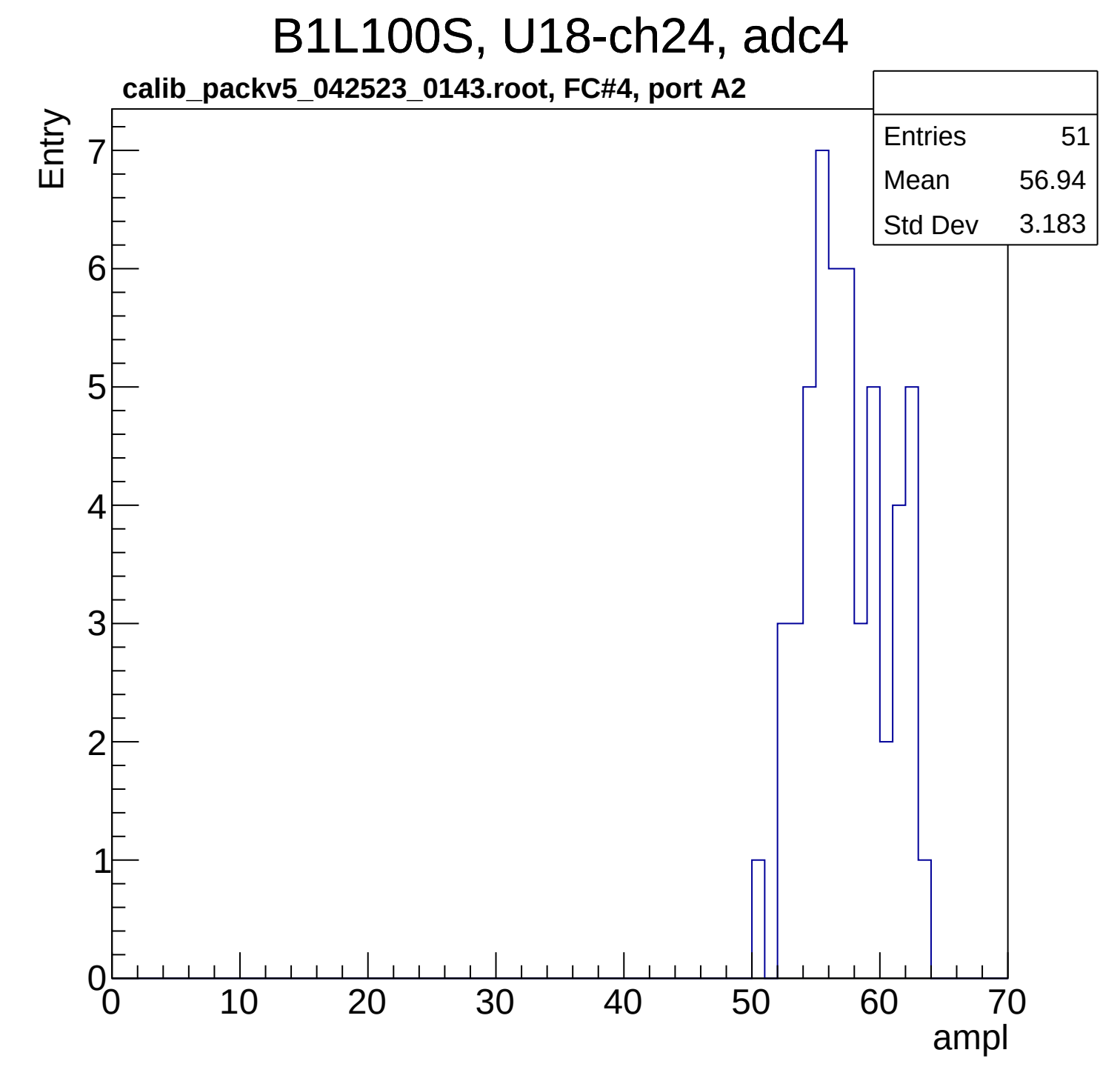

B1L100S, U18-ch23, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

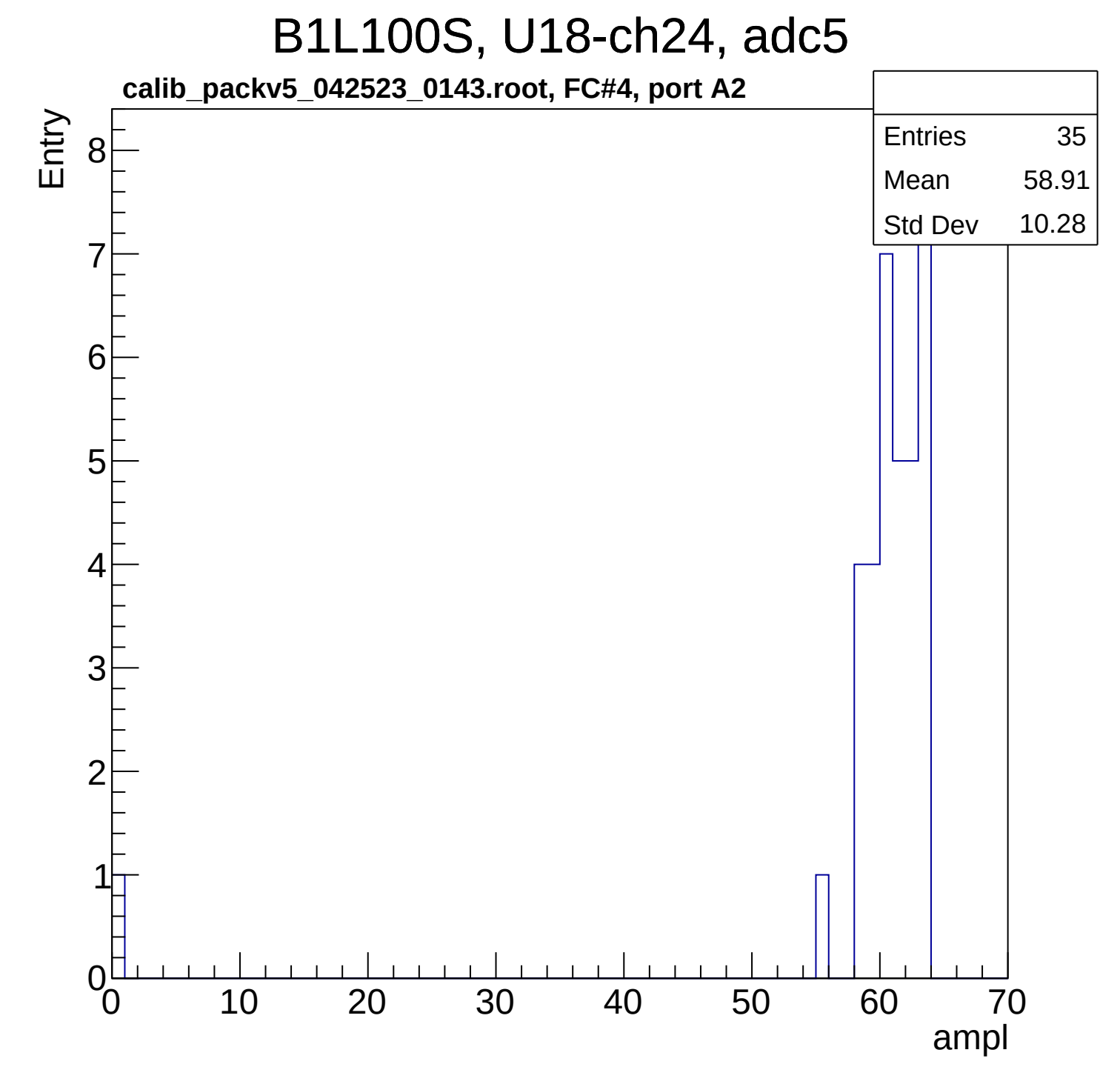

B1L100S, U18-ch24, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 30.07
Std Dev 5.001
Gaus mean : 30.8638
Gaus Width: 3.4501
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

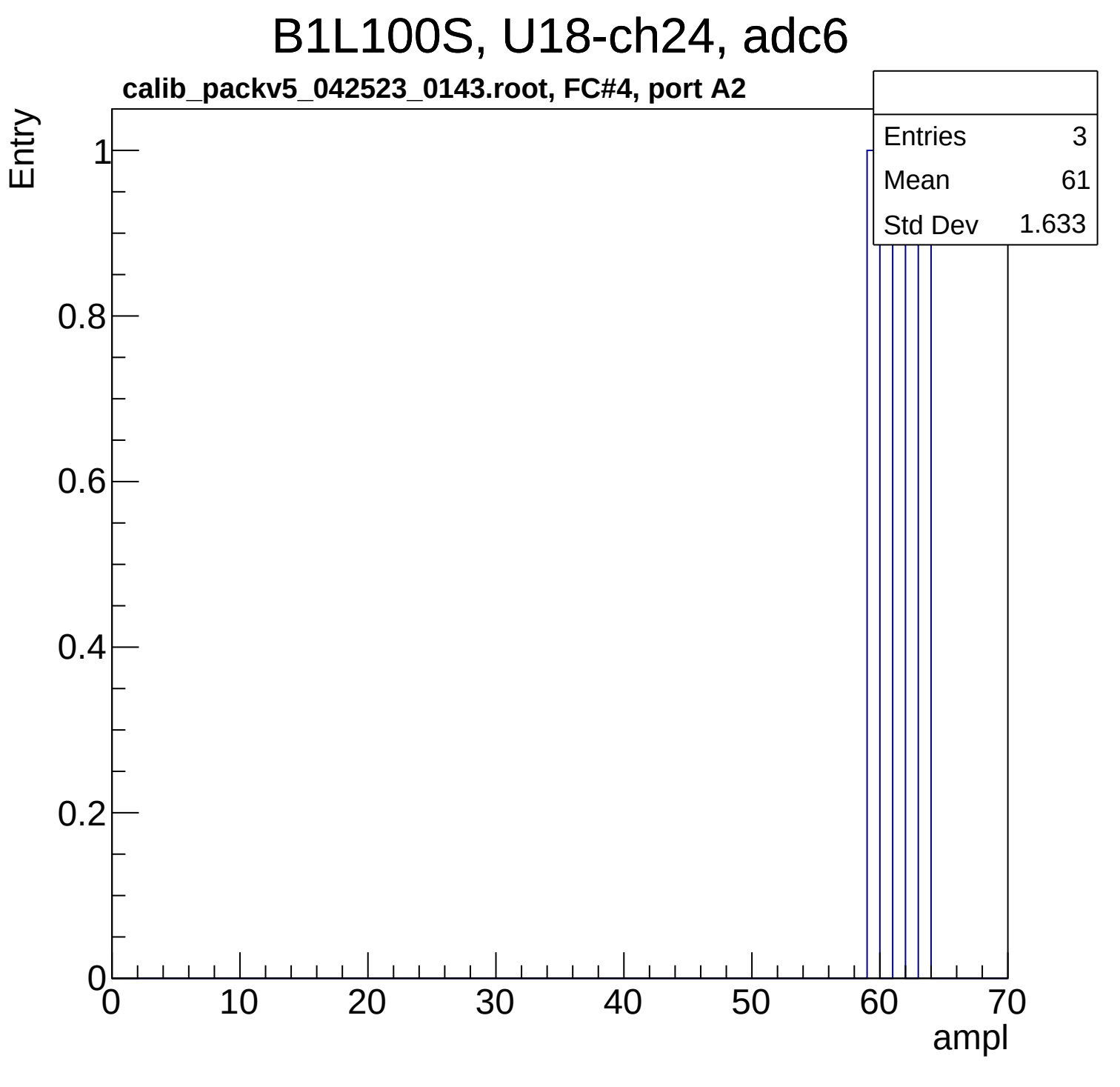

B1L100S, U18-ch24, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 36.81
Std Dev 3.596
Gaus mean : 37.9888
Gaus Width: 3.5468
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

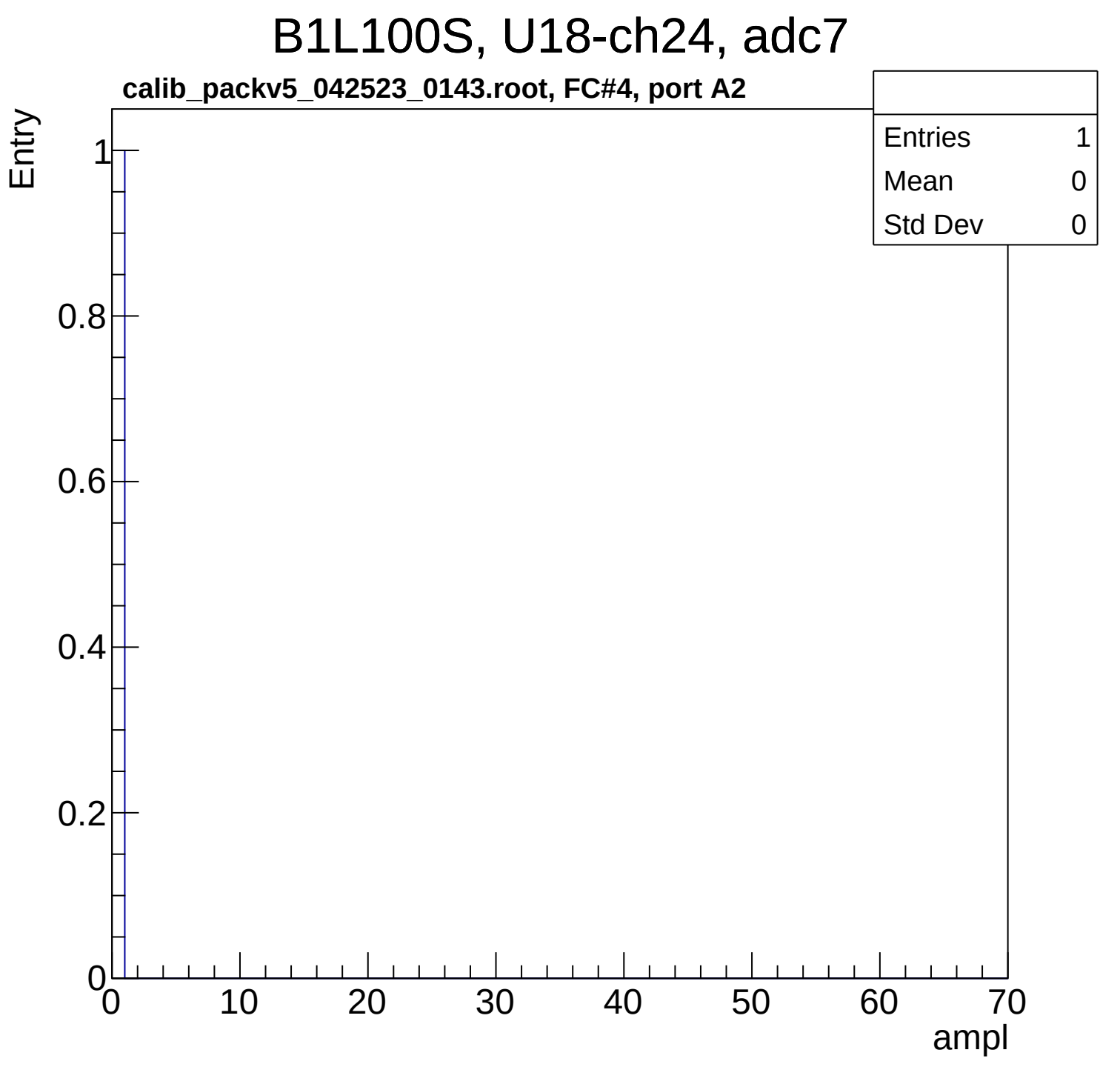

B1L100S, U18-ch24, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 43.6
Std Dev 3.343
Gaus mean : 44.0163
Gaus Width: 3.3602
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

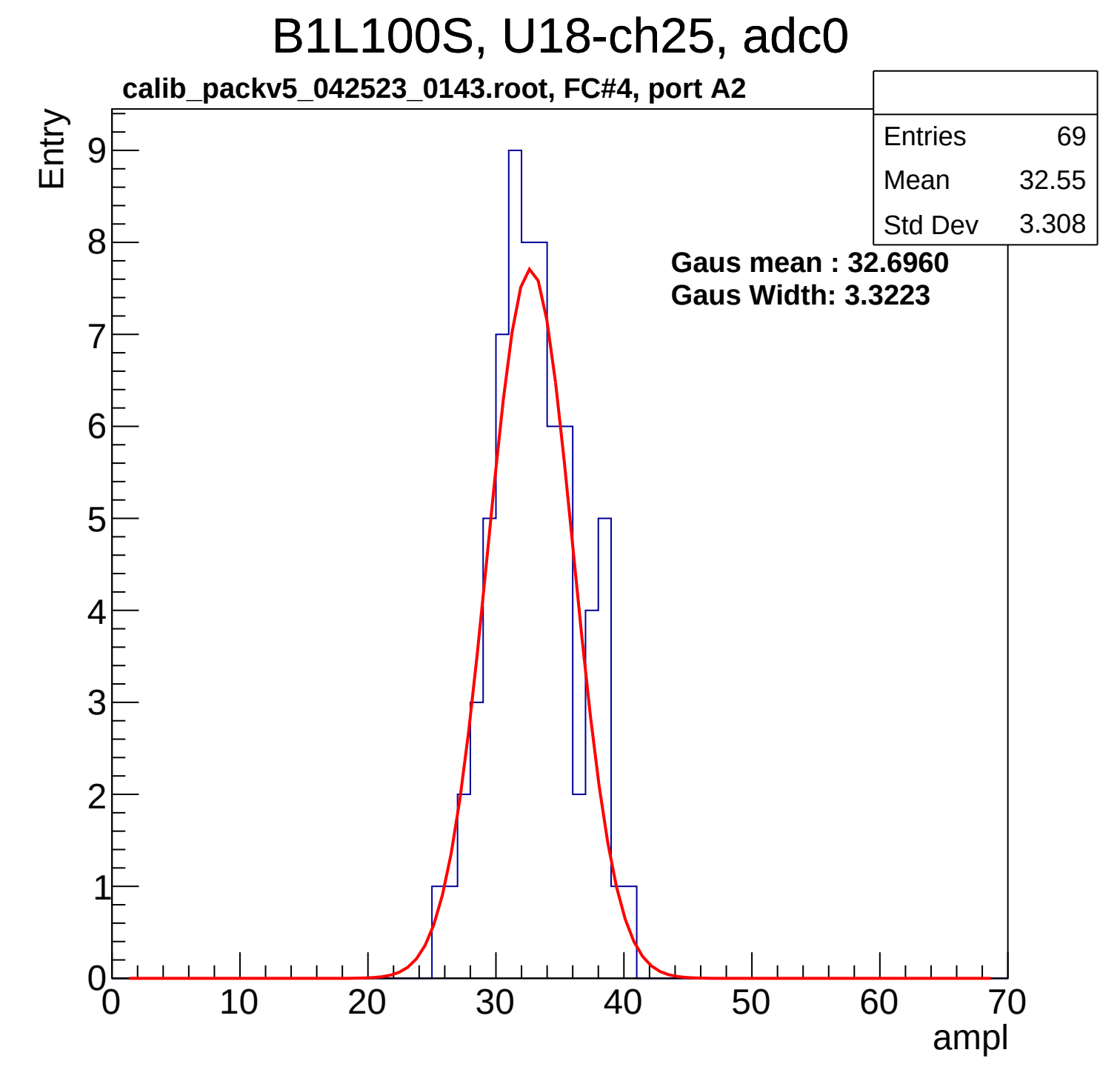

B1L100S, U18-ch24, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 50.7
Std Dev 3.934
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

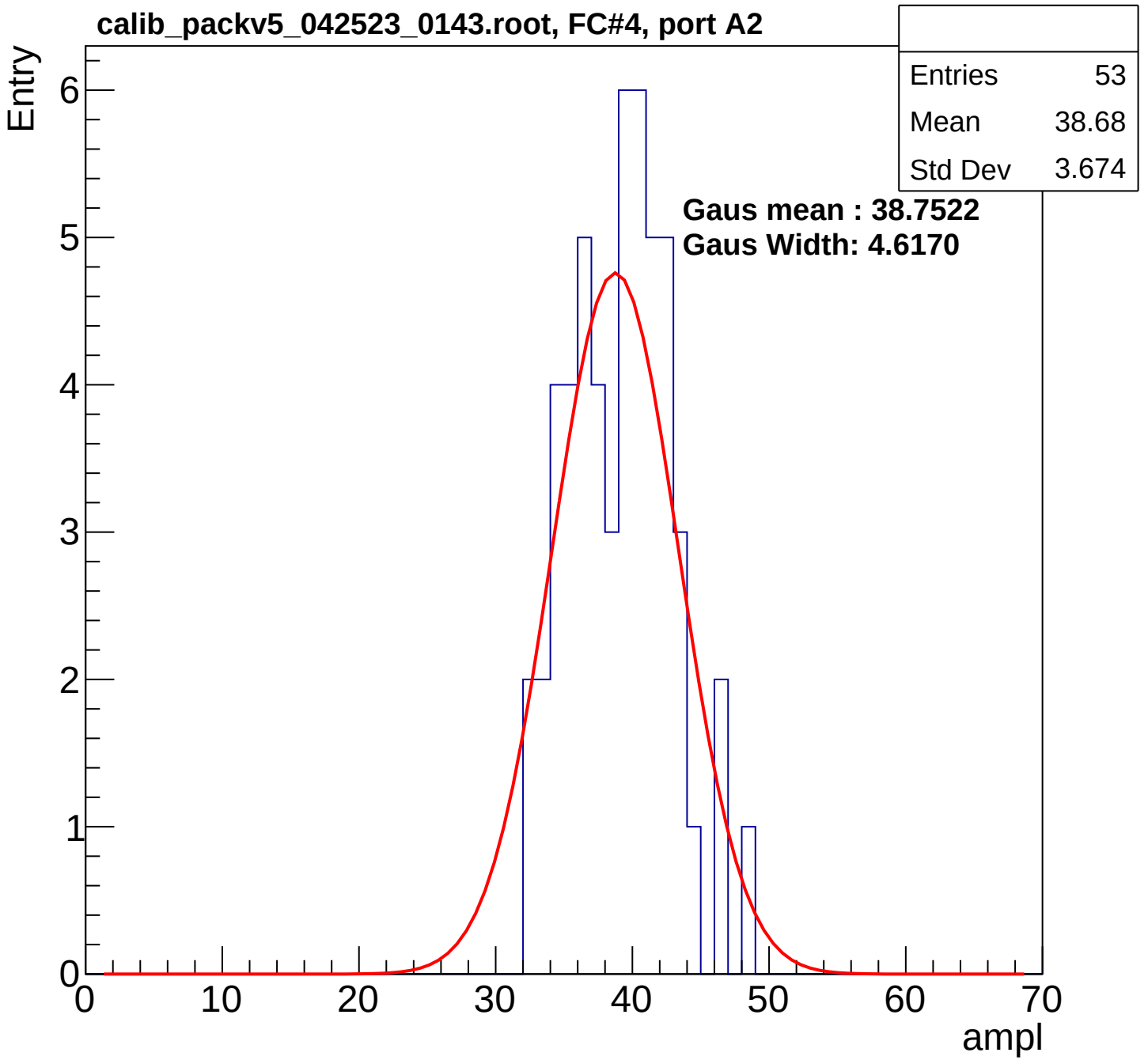

B1L100S, U18-ch24, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 56.94
Std Dev 3.183
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

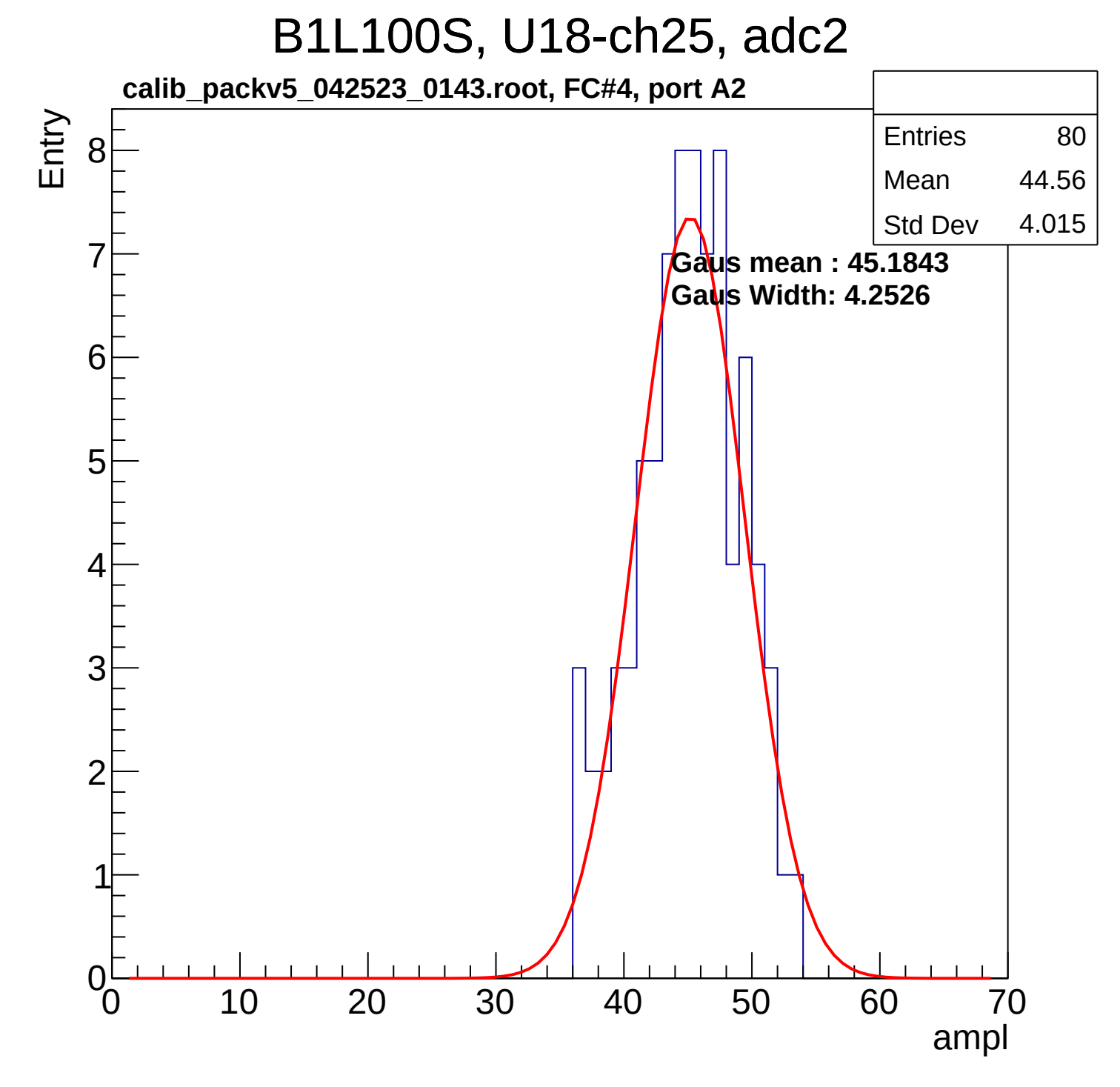

B1L100S, U18-ch24, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 35
Mean 58.91
Std Dev 10.28
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

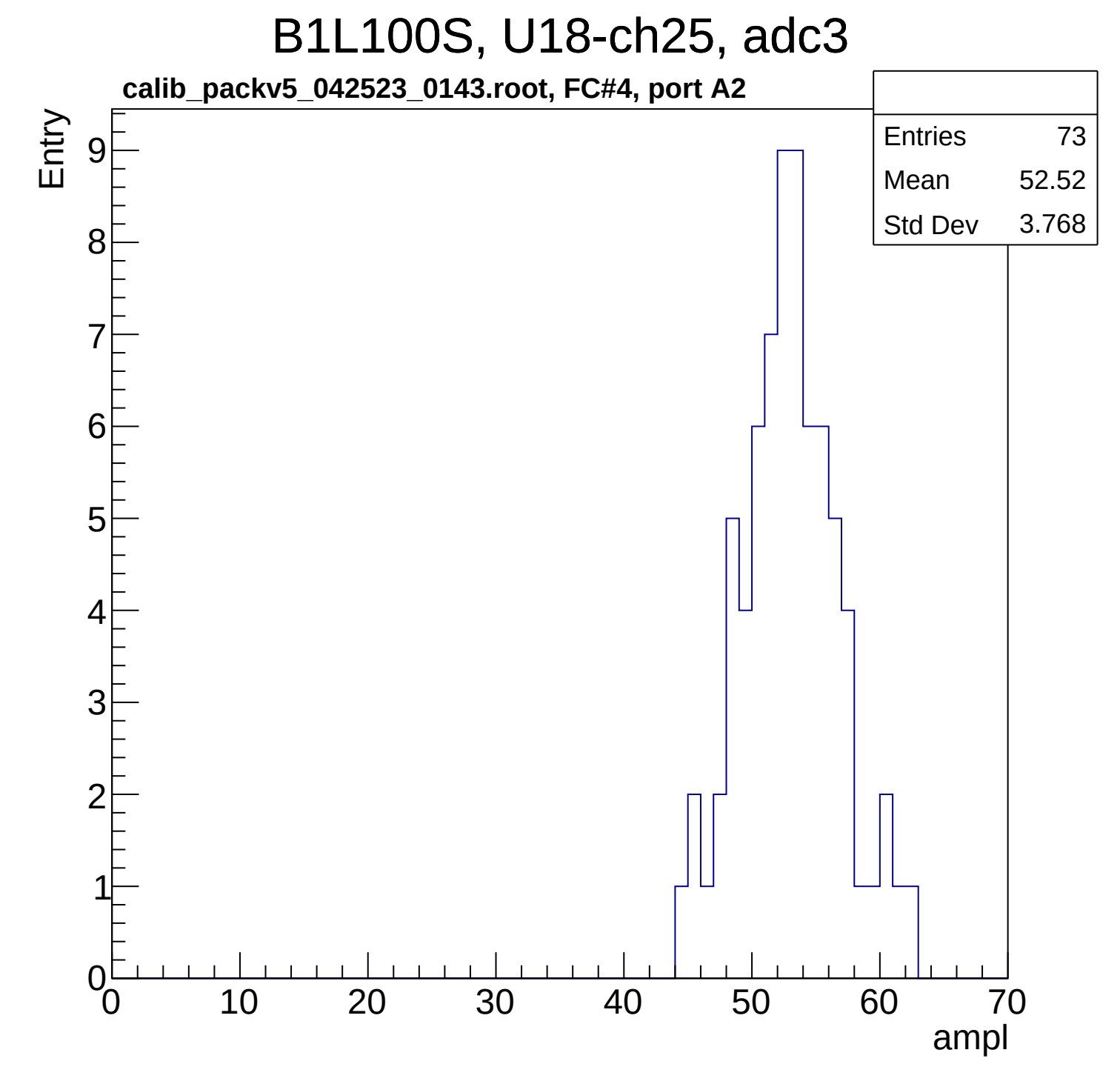

B1L100S, U18-ch24, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 61
Std Dev 1.633
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

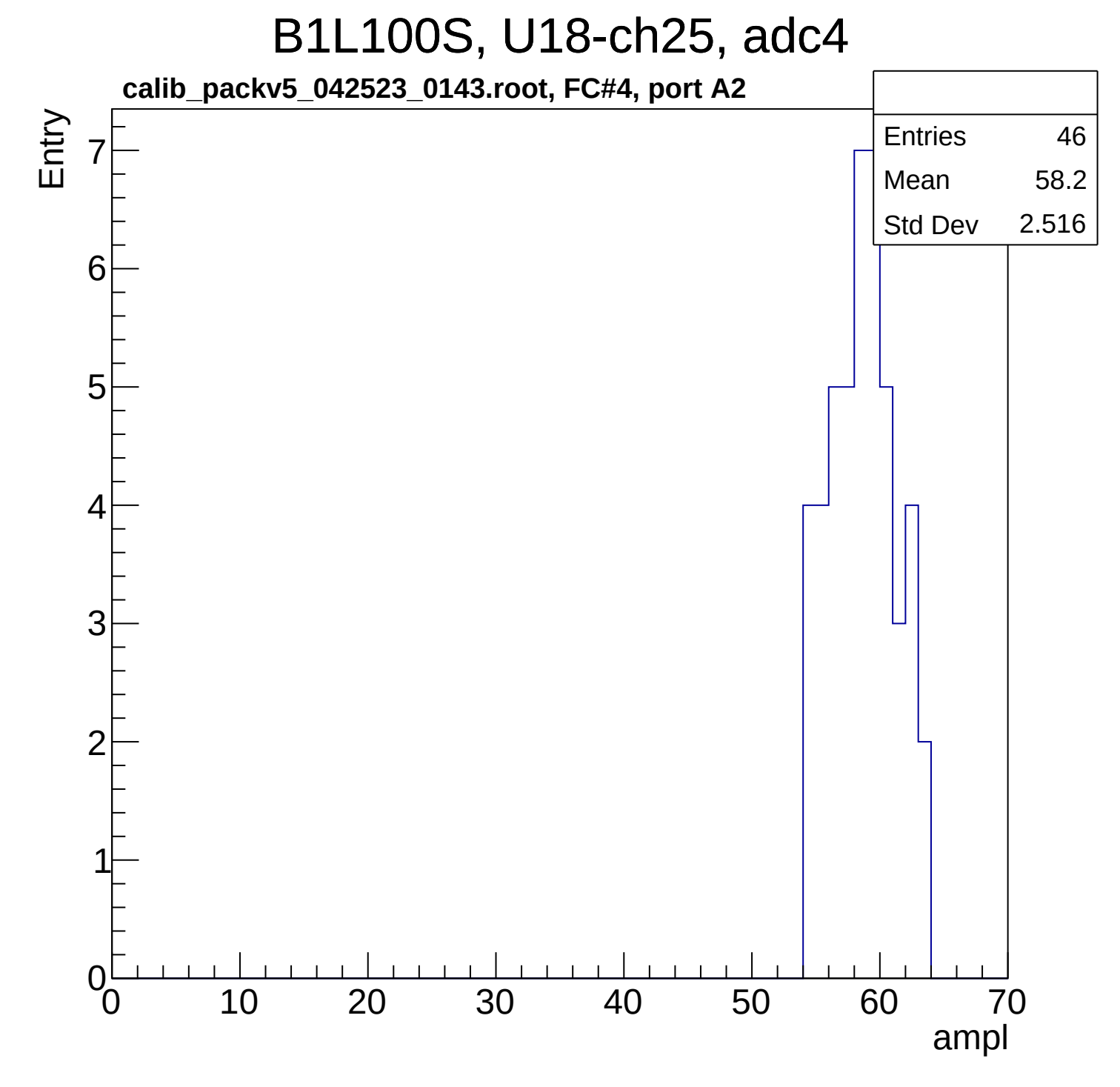

B1L100S, U18-ch24, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

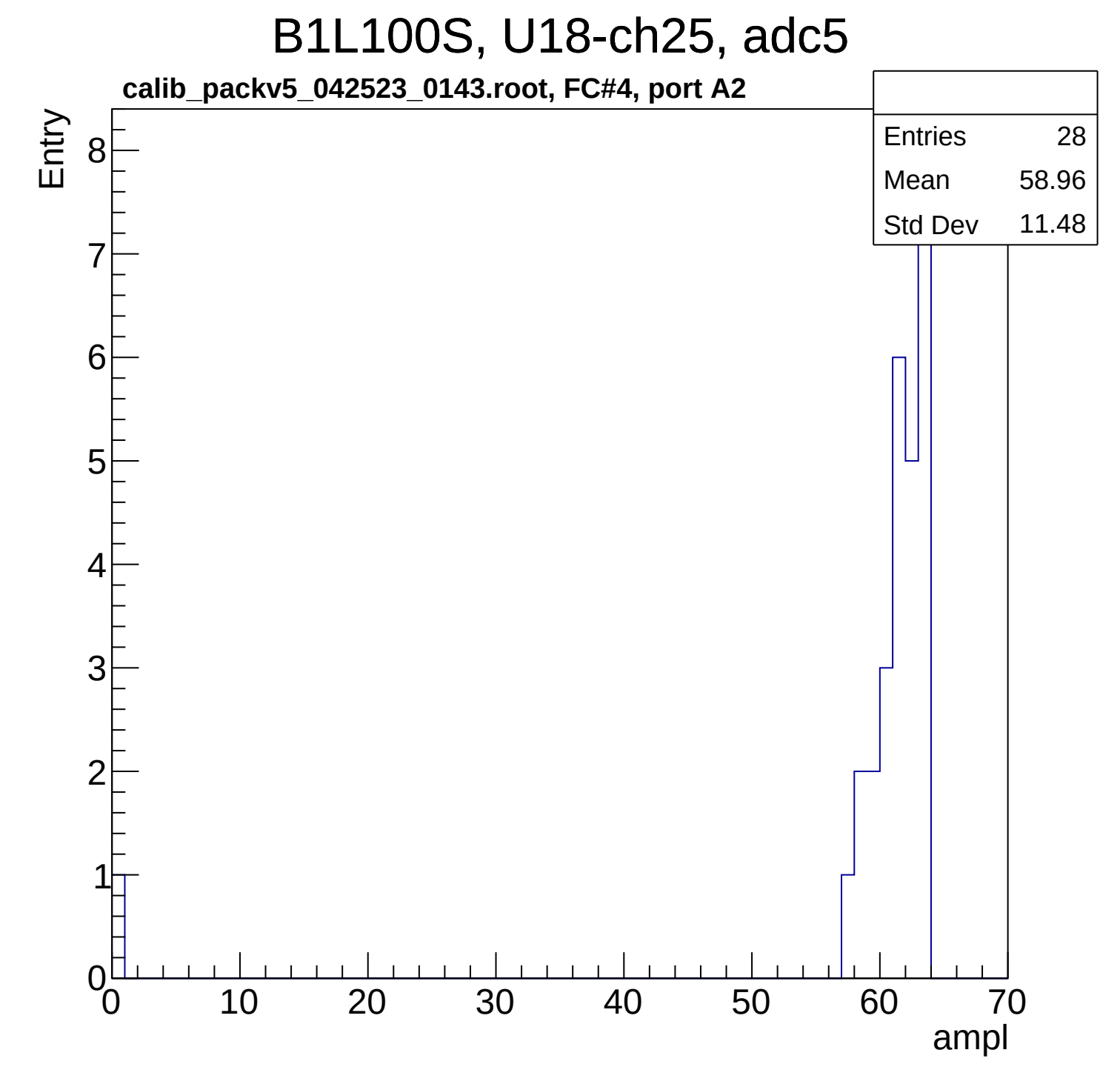

B1L100S, U18-ch25, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 32.55
Std Dev 3.308
Gaus mean : 32.6960
Gaus Width: 3.3223
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

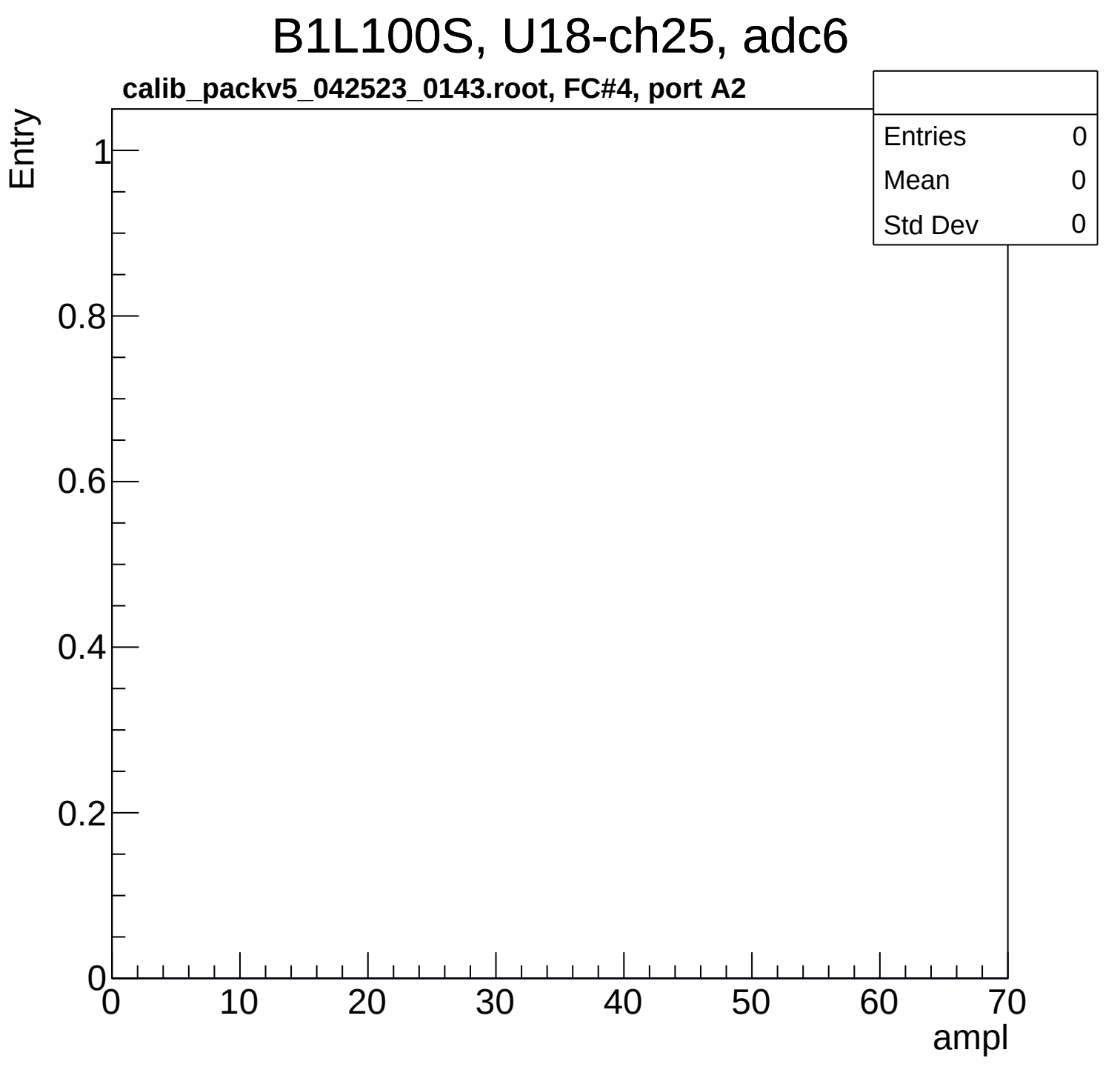

B1L100S, U18-ch25, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 38.68
Std Dev 3.674
Gaus mean : 38.7522
Gaus Width: 4.6170
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

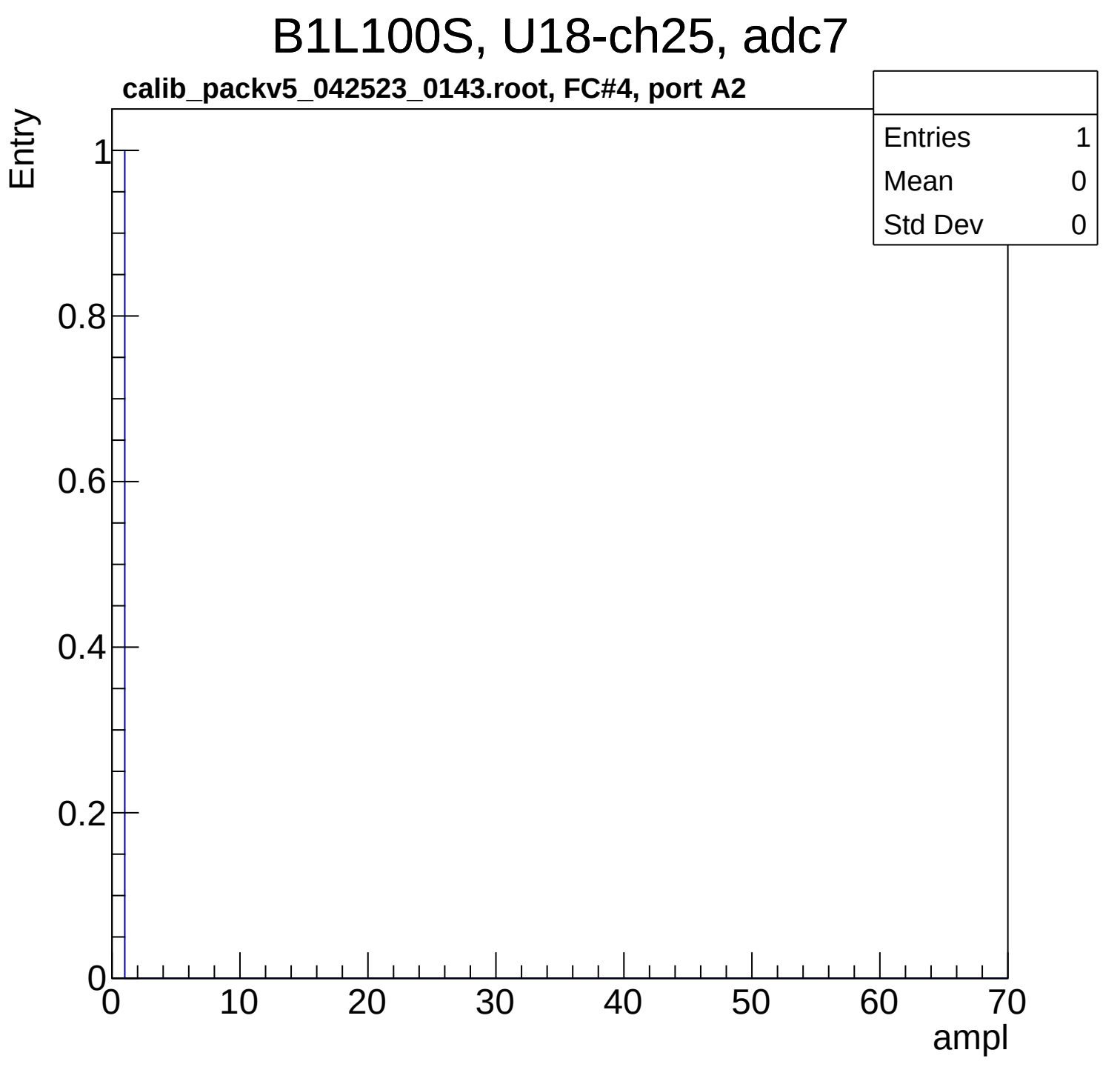

B1L100S, U18-ch25, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 44.56
Std Dev 4.015
Gaus mean : 45.1843
Gaus Width: 4.2526
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

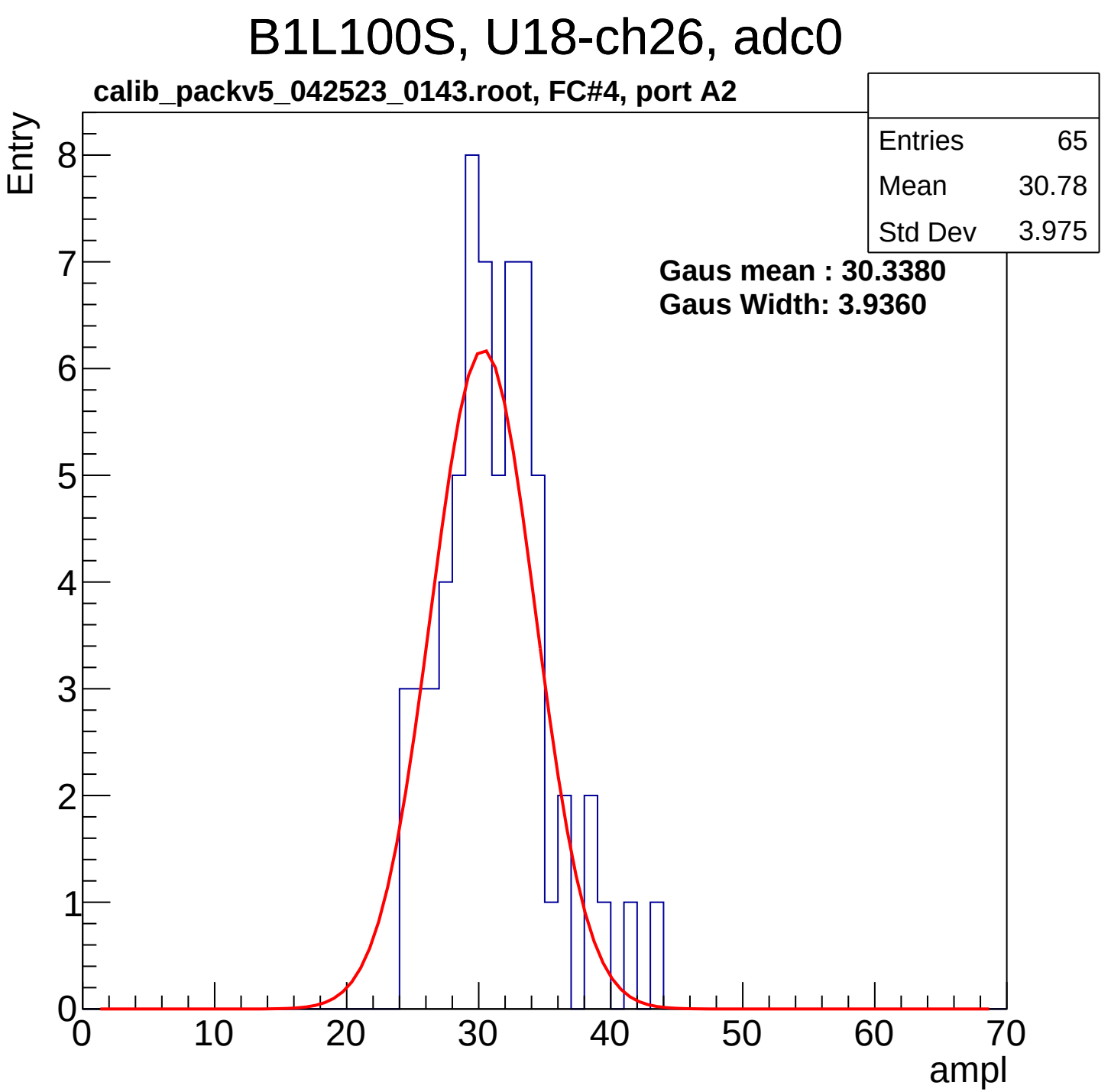

B1L100S, U18-ch25, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 52.52
Std Dev 3.768
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

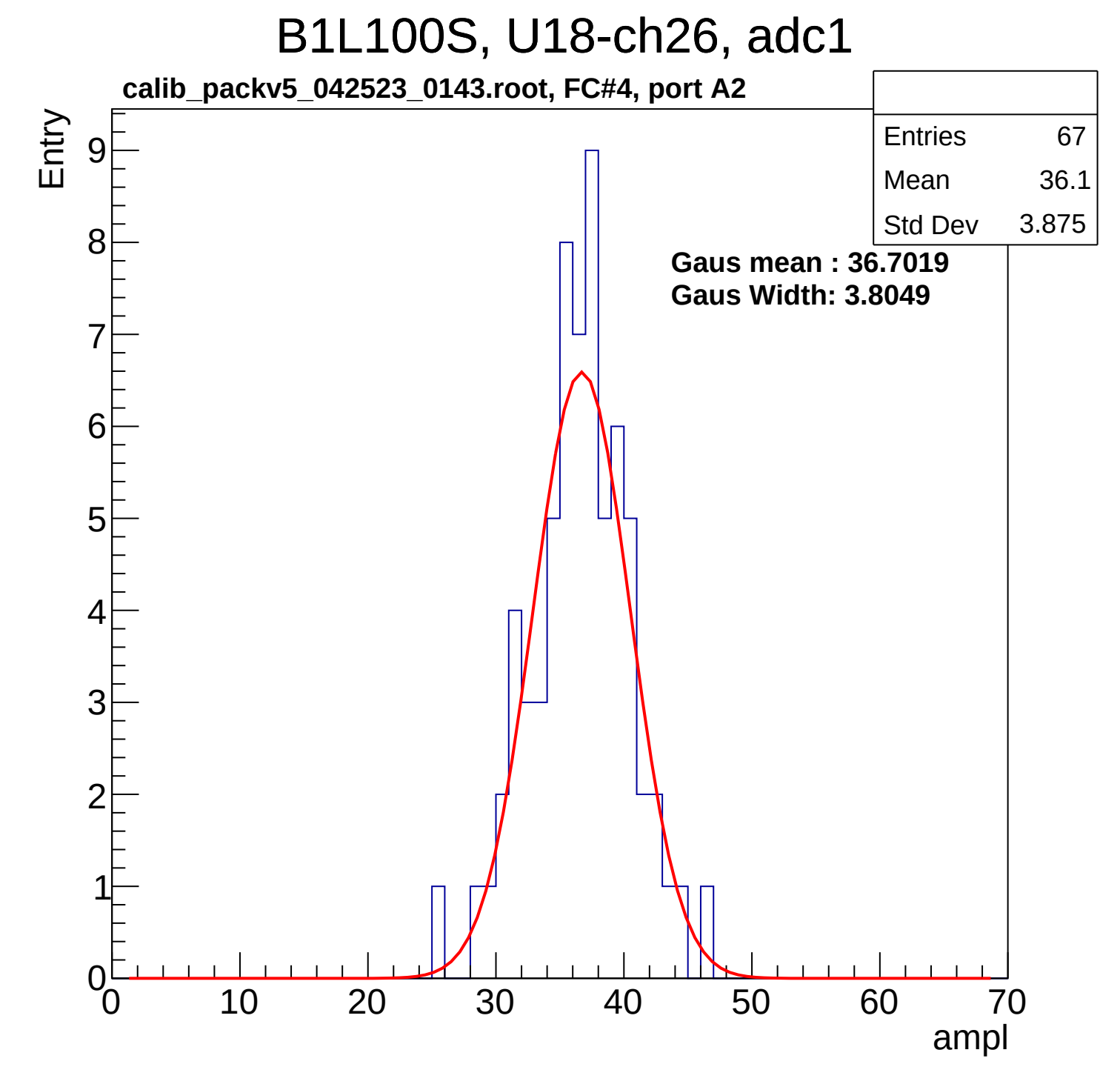

B1L100S, U18-ch25, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 58.2
Std Dev 2.516
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

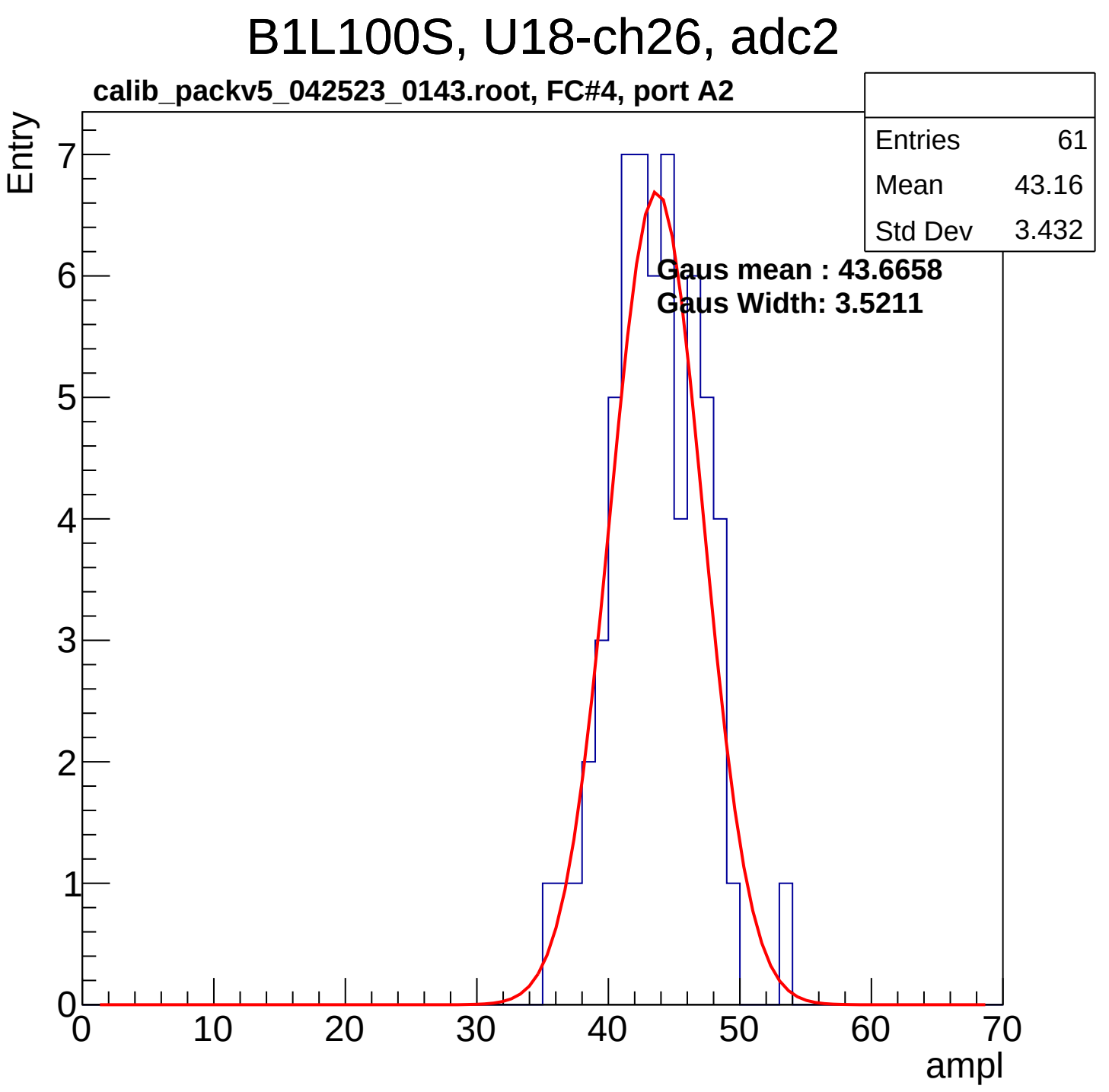

B1L100S, U18-ch25, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 28
Mean 58.96
Std Dev 11.48
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

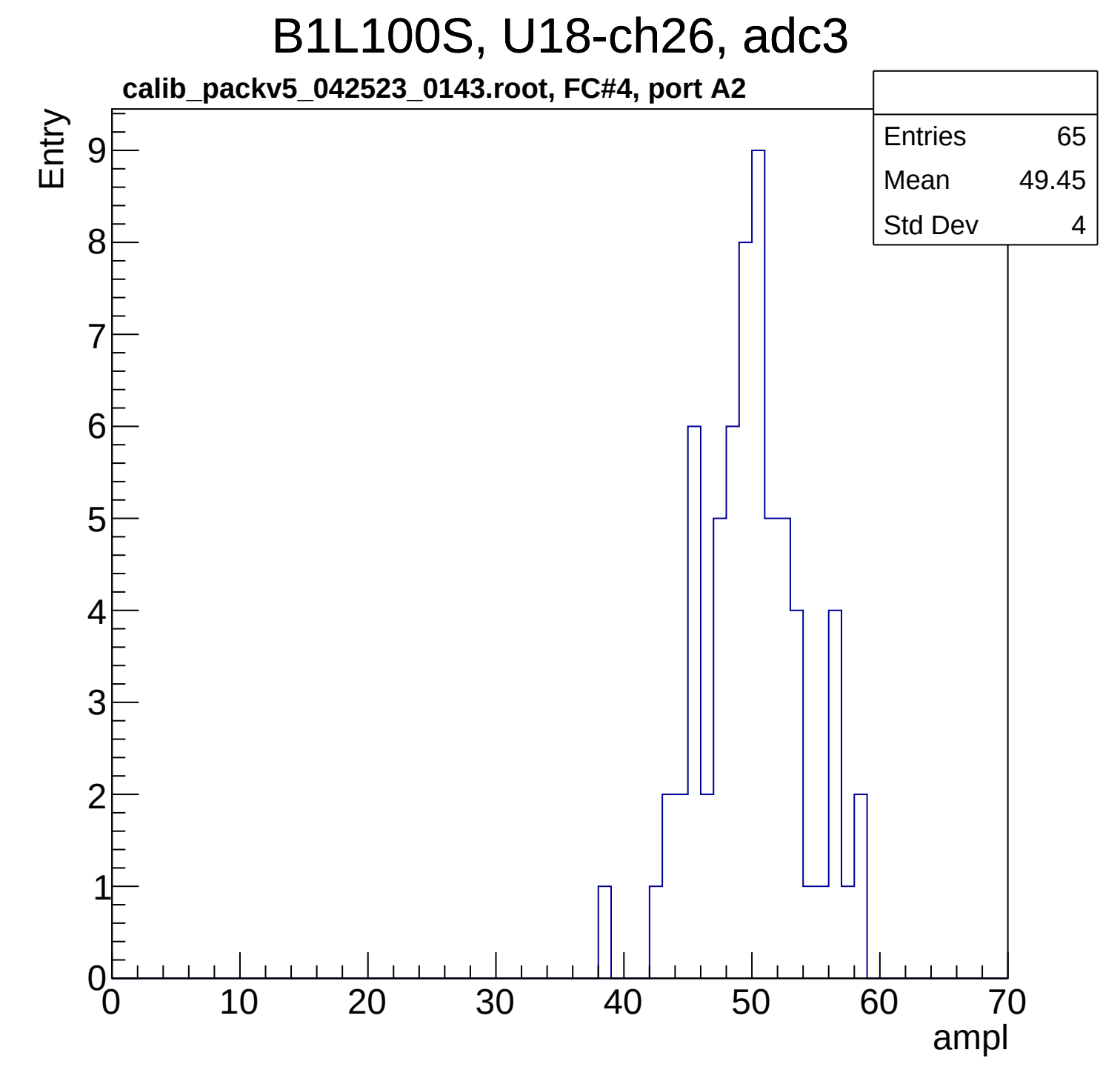

B1L100S, U18-ch25, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

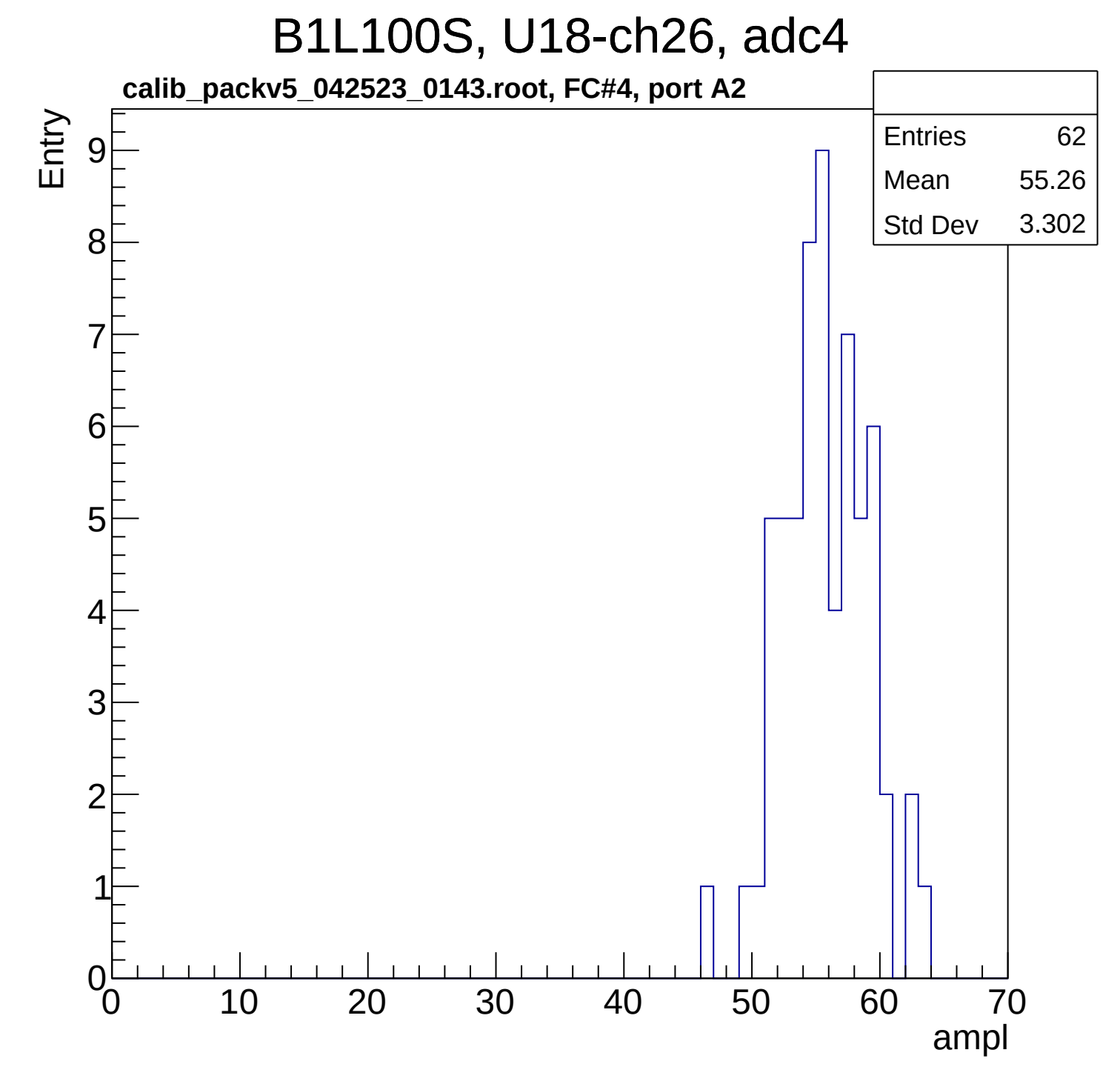

B1L100S, U18-ch25, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

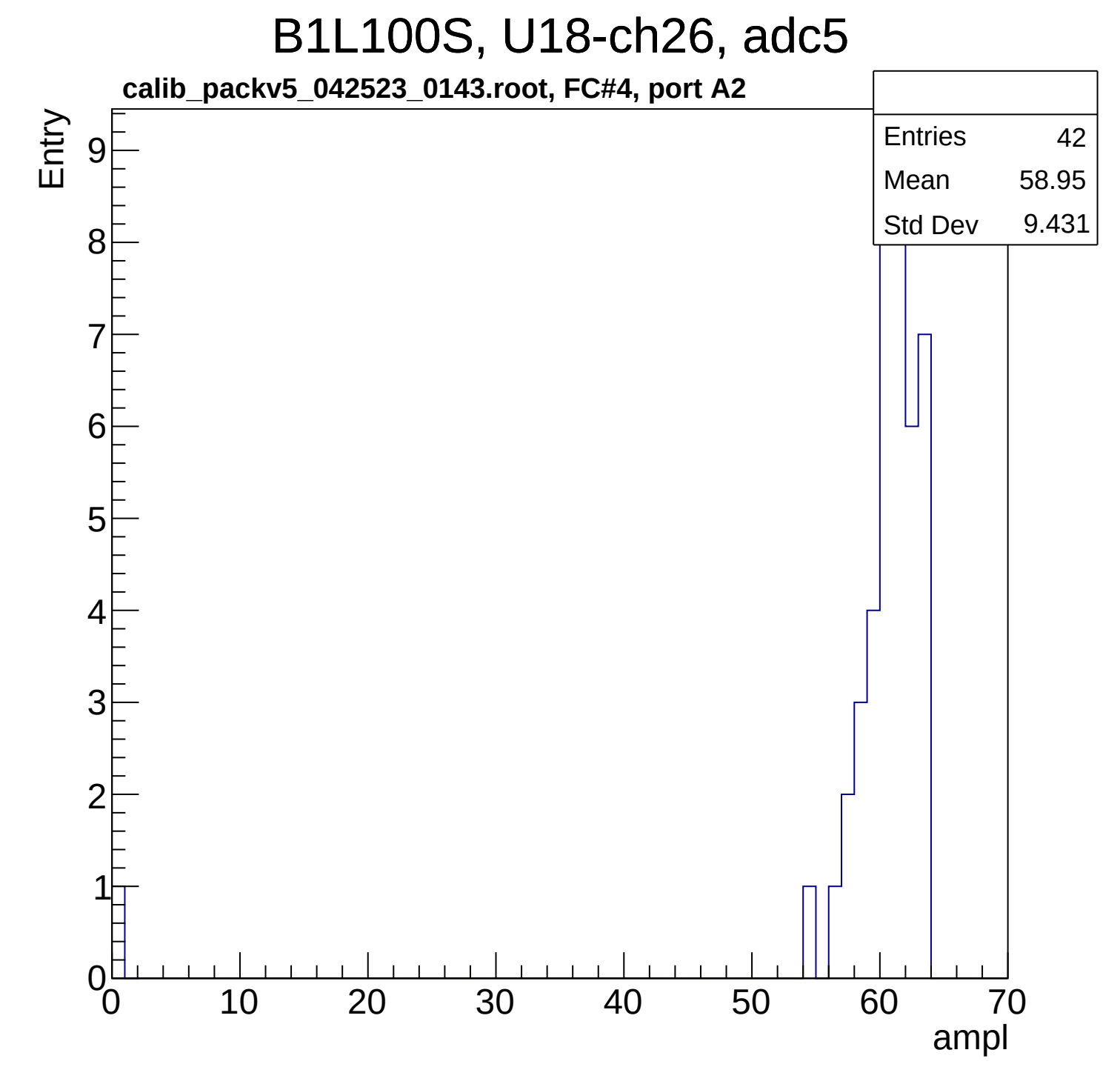

B1L100S, U18-ch26, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 30.78
Std Dev 3.975
Gaus mean : 30.3380
Gaus Width: 3.9360
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

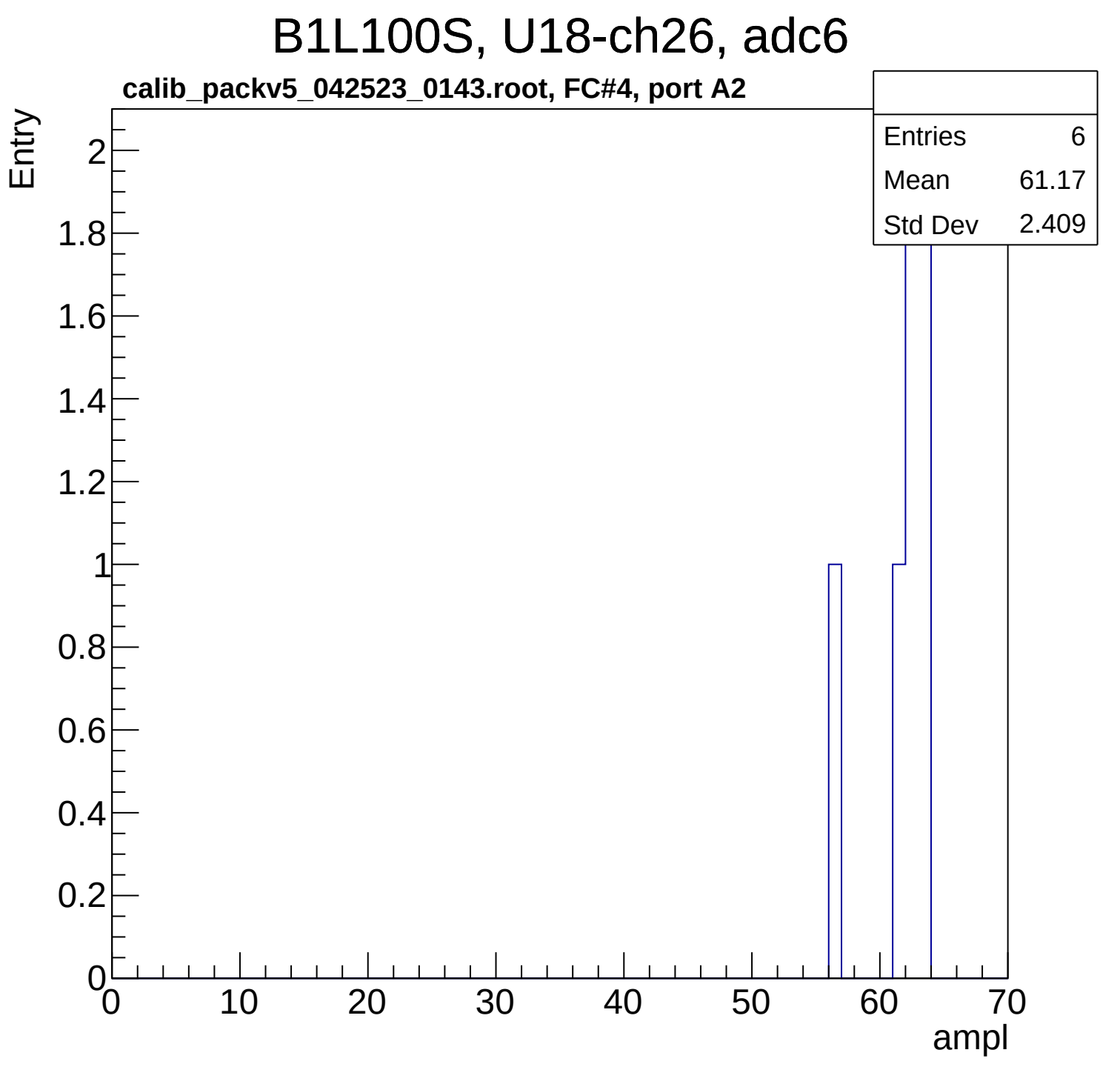

B1L100S, U18-ch26, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 36.1
Std Dev 3.875
Gaus mean : 36.7019
Gaus Width: 3.8049
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

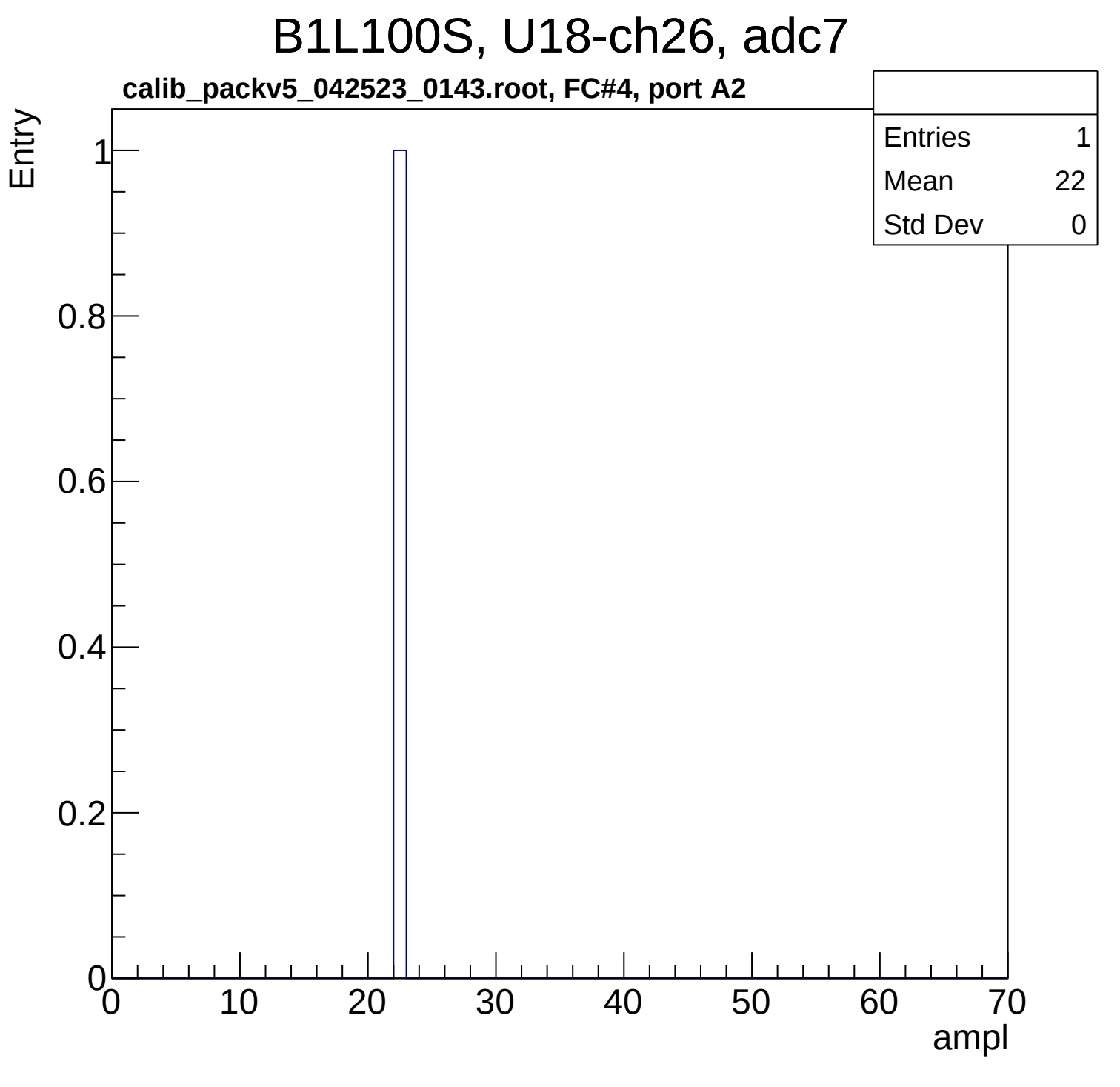

B1L100S, U18-ch26, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 43.16
Std Dev 3.432
Gaus mean : 43.6658
Gaus Width: 3.5211
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

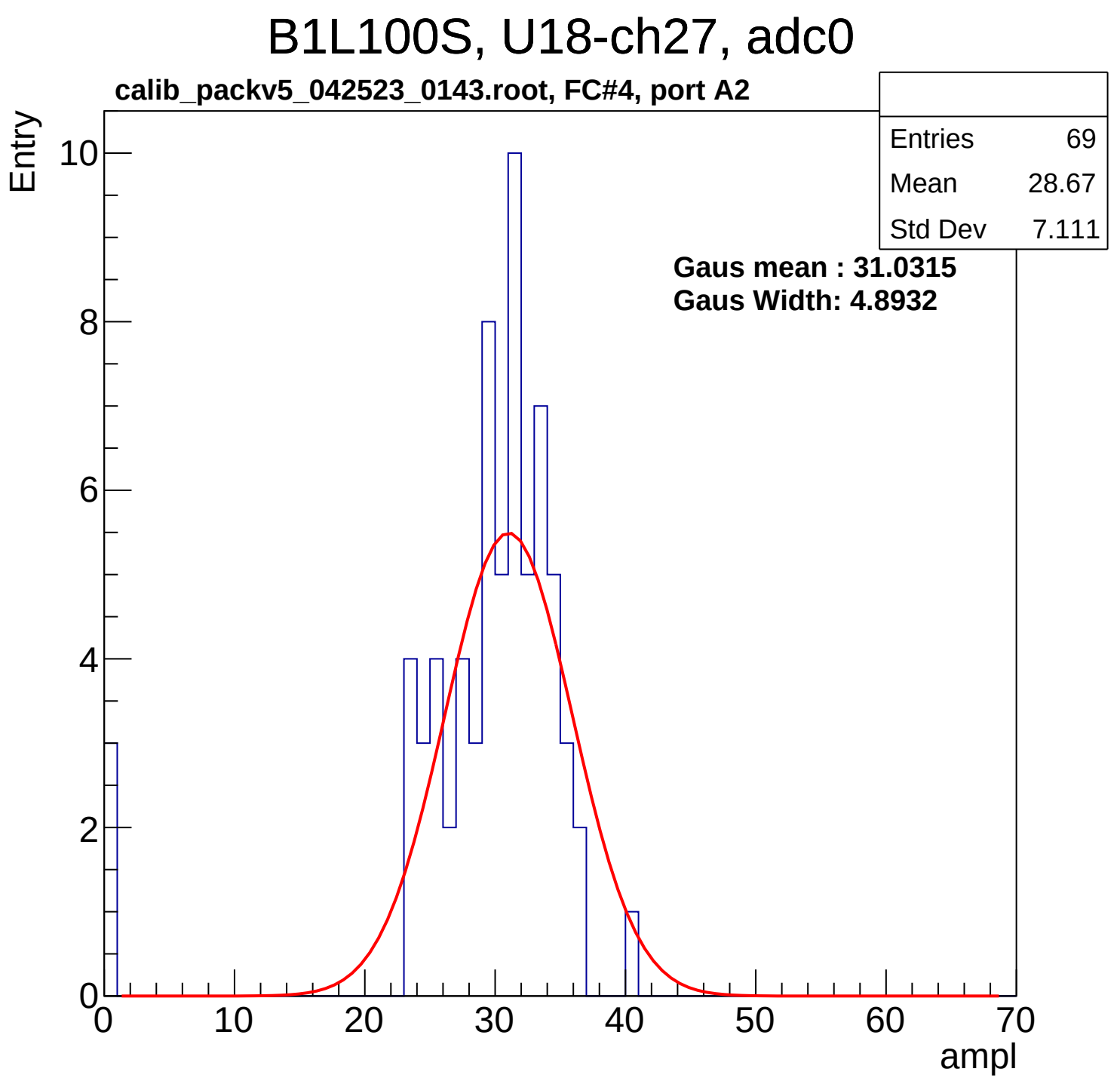

B1L100S, U18-ch26, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 49.45
Std Dev 4
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

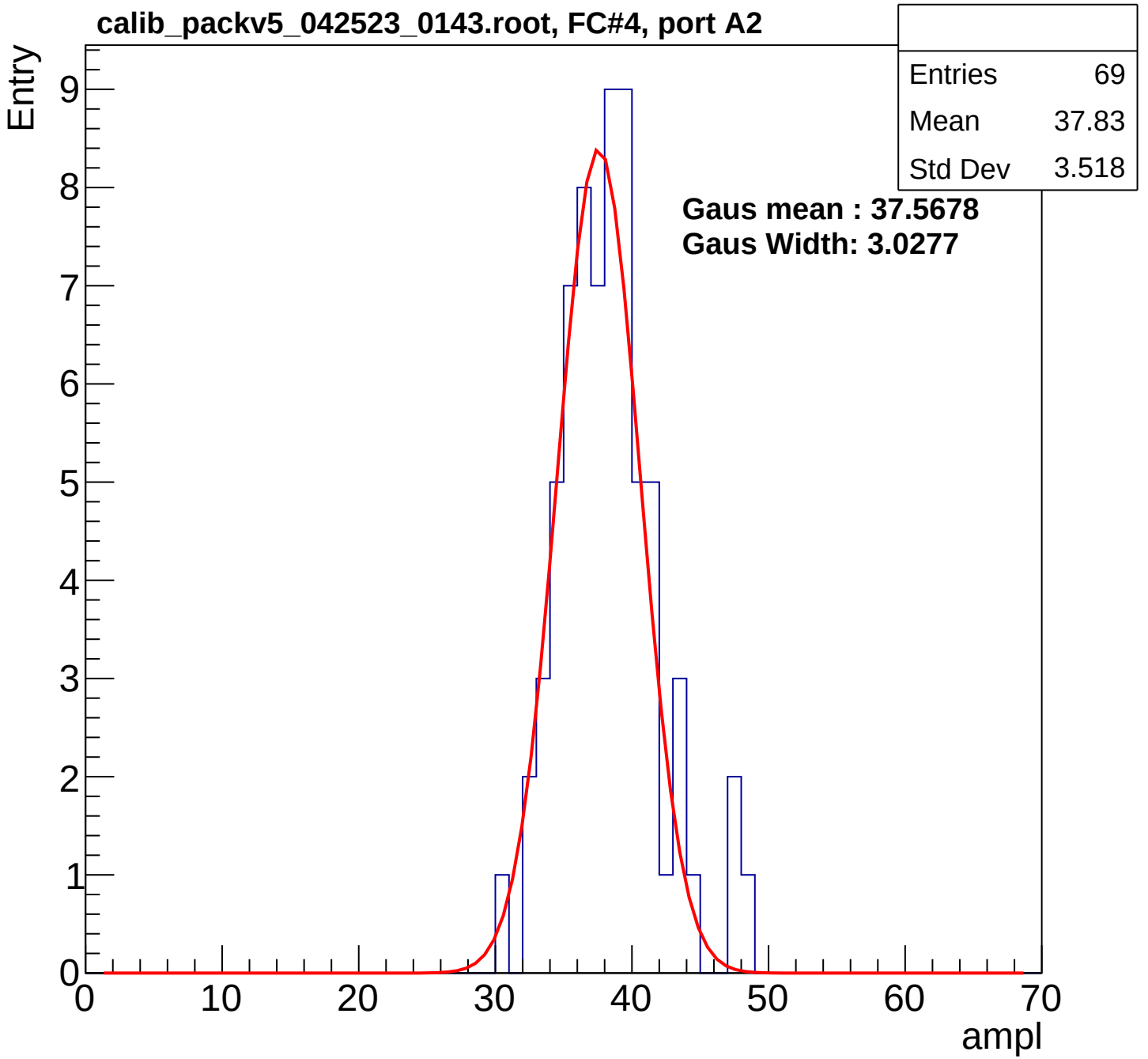

B1L100S, U18-ch26, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 55.26
Std Dev 3.302
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

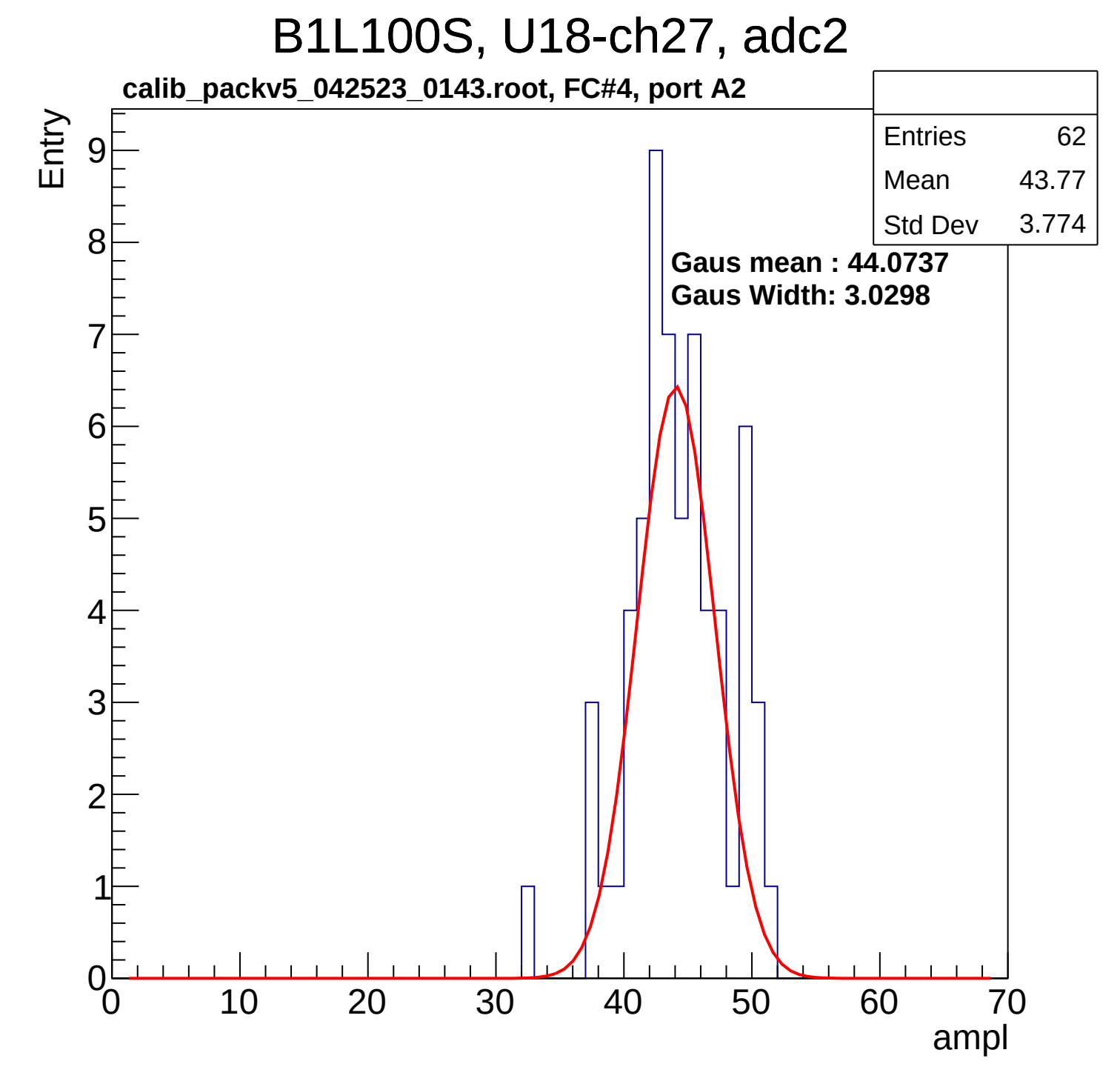

B1L100S, U18-ch26, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 42
Mean 58.95
Std Dev 9.431
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

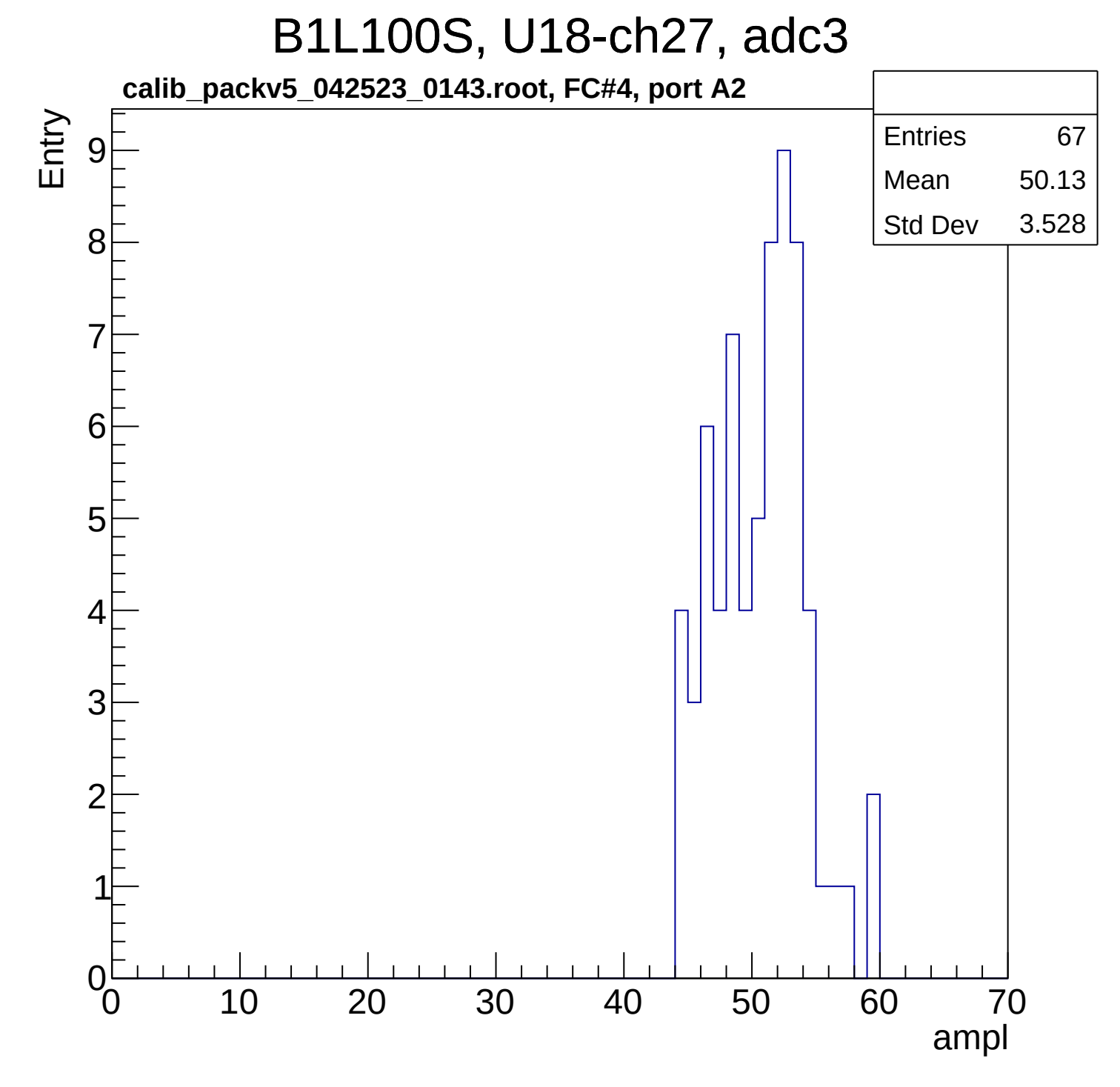

B1L100S, U18-ch26, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 61.17
Std Dev 2.409
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

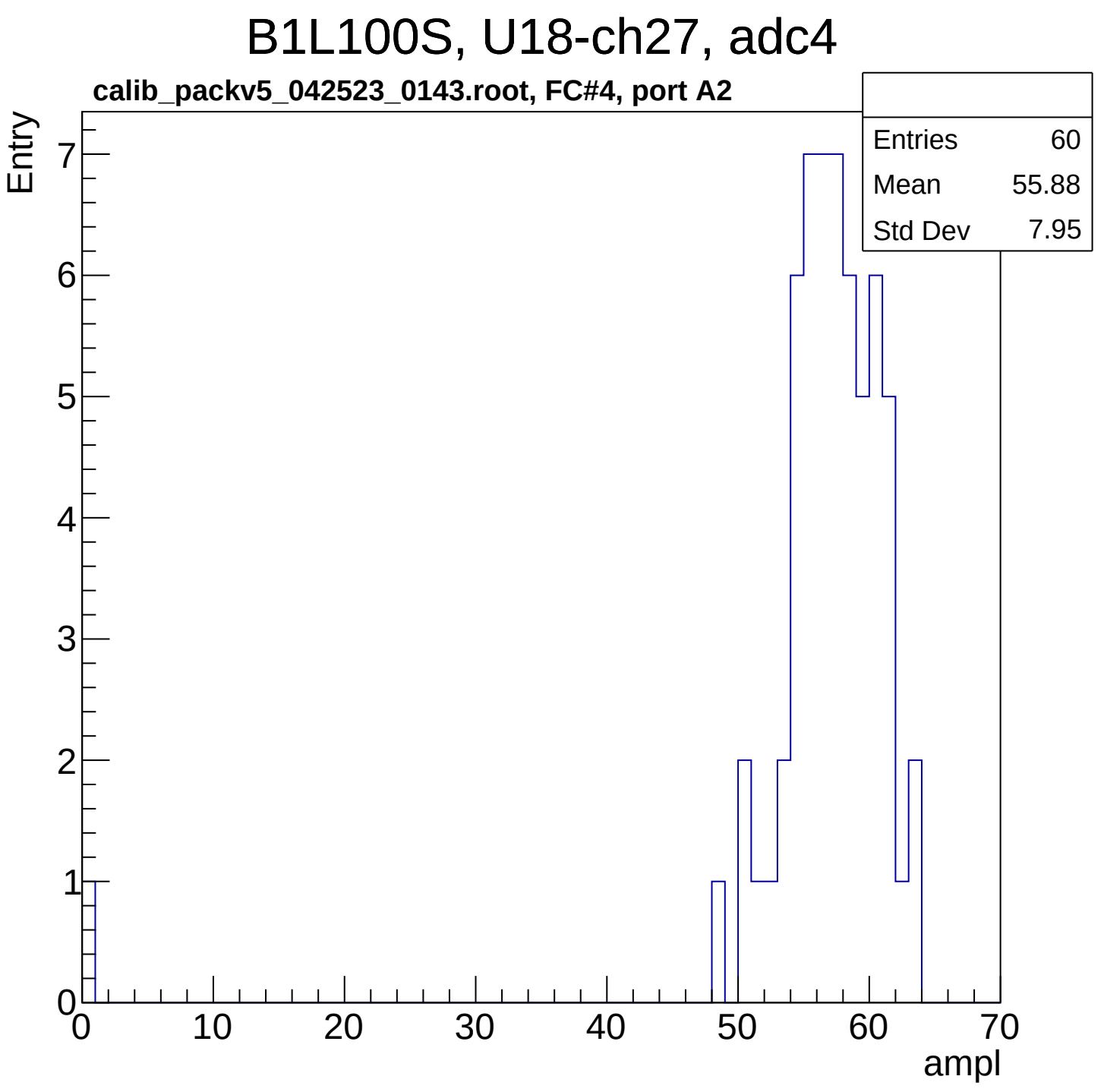

B1L100S, U18-ch26, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 22
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

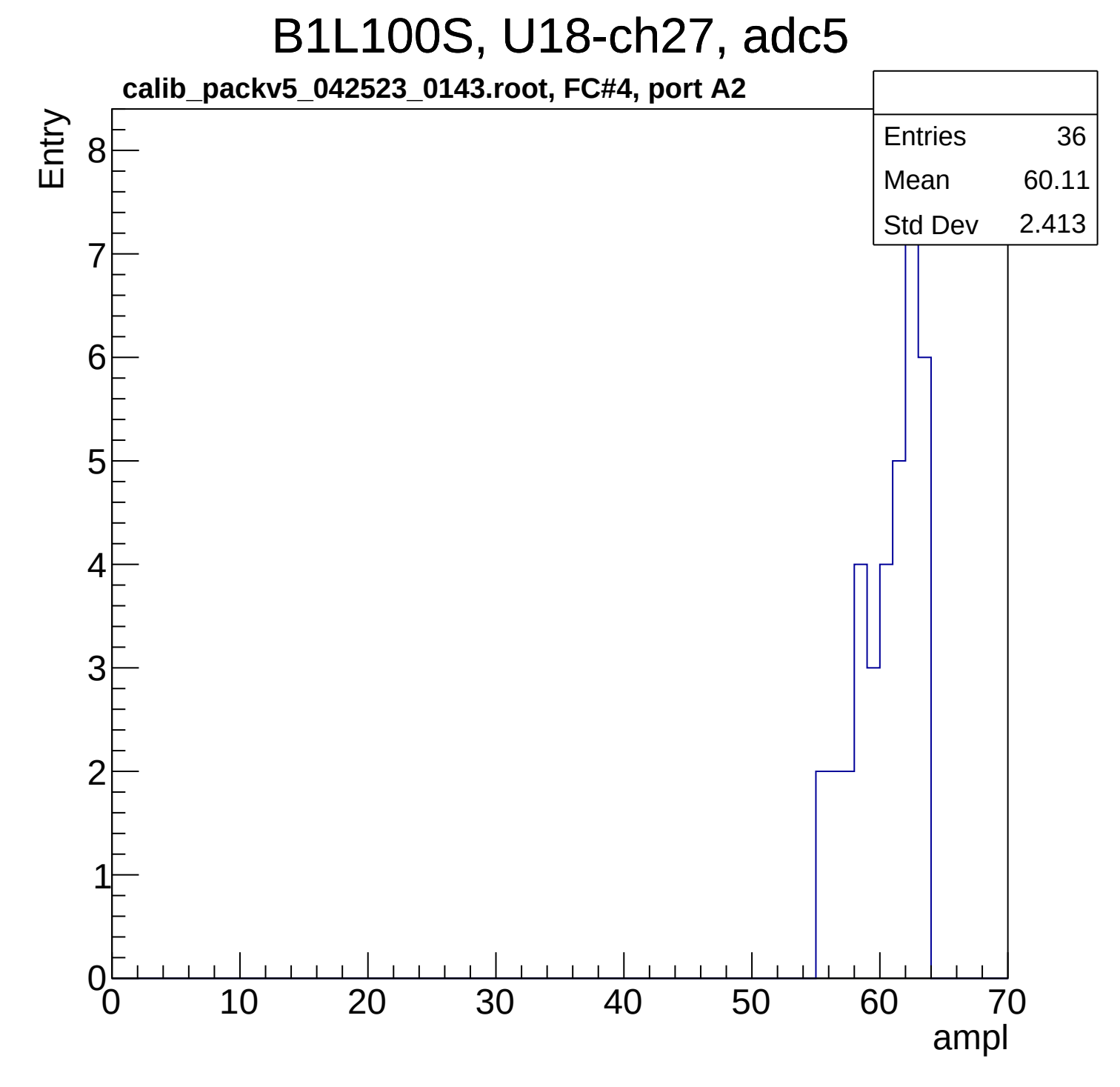

B1L100S, U18-ch27, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 28.67
Std Dev 7.111
Gaus mean : 31.0315
Gaus Width: 4.8932
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

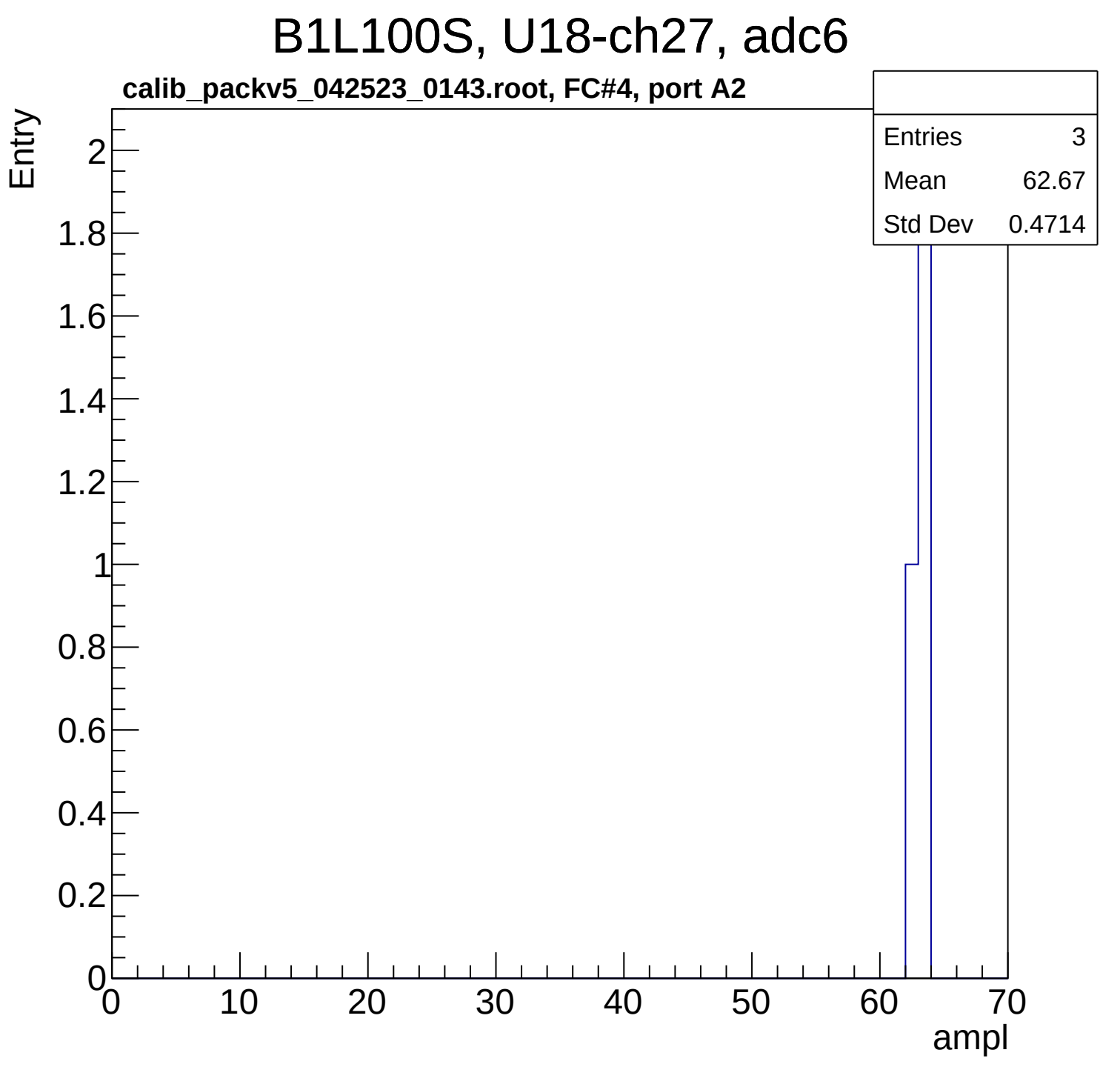

B1L100S, U18-ch27, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 37.83
Std Dev 3.518
Gaus mean : 37.5678
Gaus Width: 3.0277
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

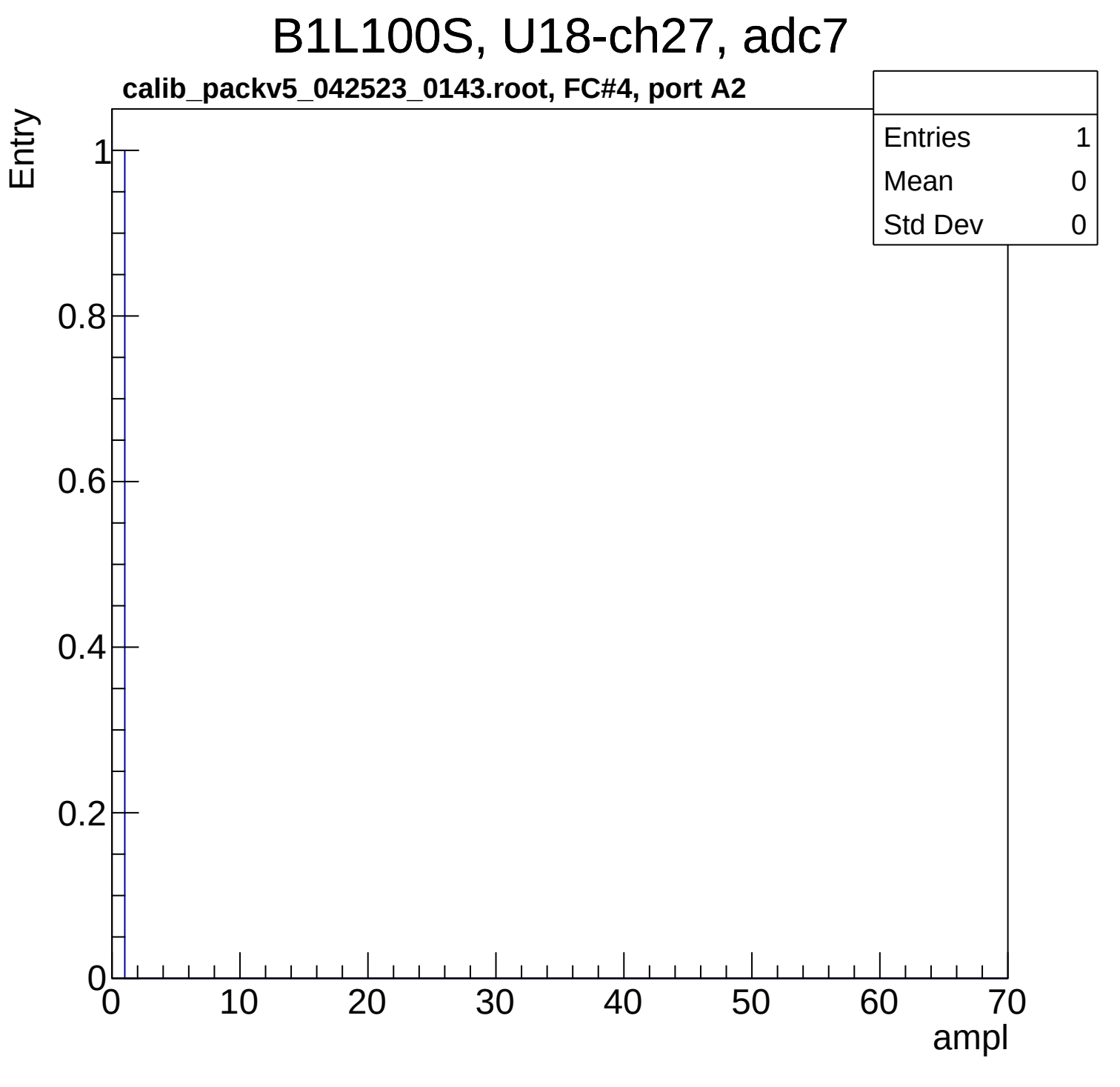

B1L100S, U18-ch27, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 43.77
Std Dev 3.774
Gaus mean : 44.0737
Gaus Width: 3.0298
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

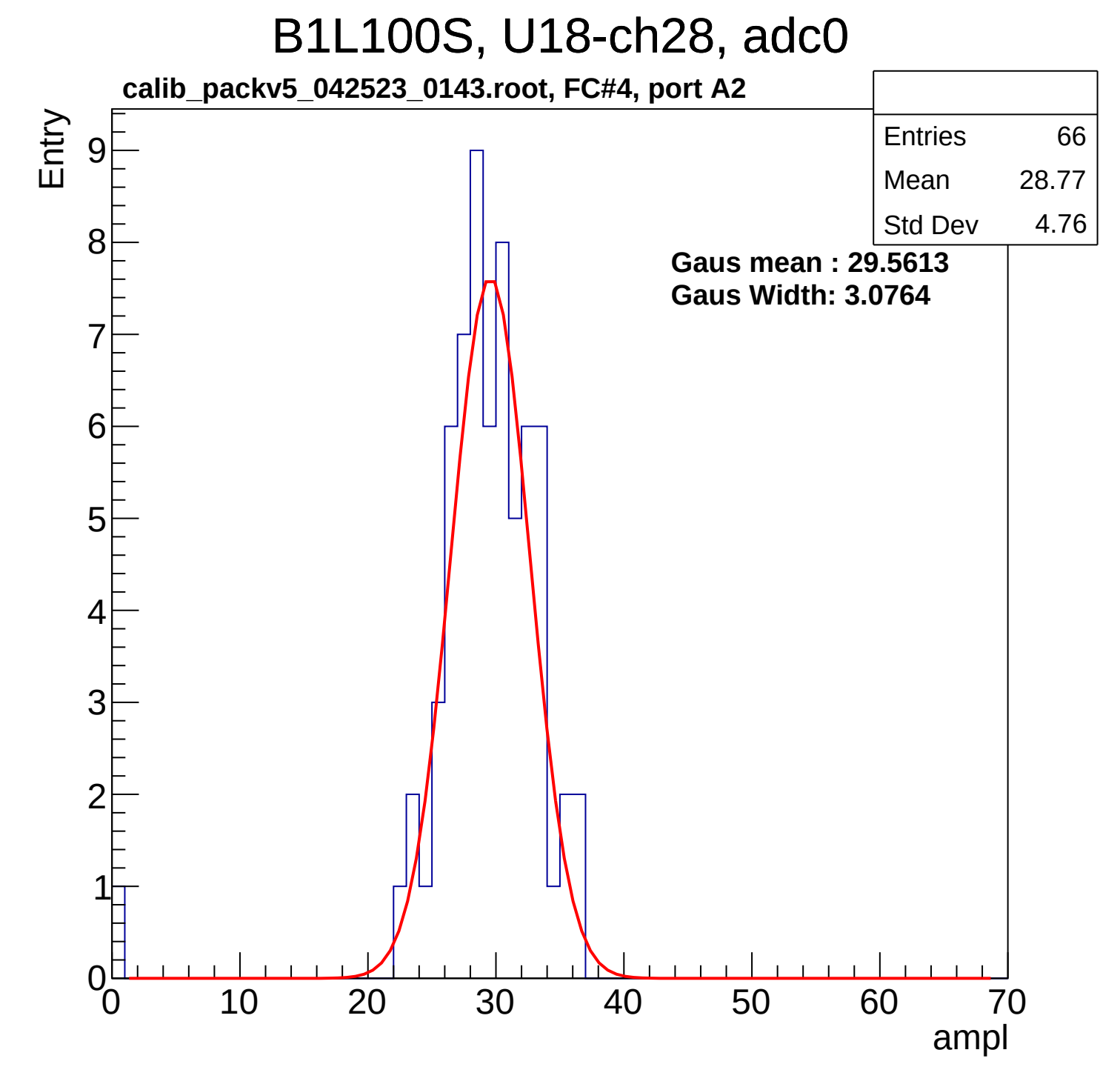

B1L100S, U18-ch27, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 50.13
Std Dev 3.528
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

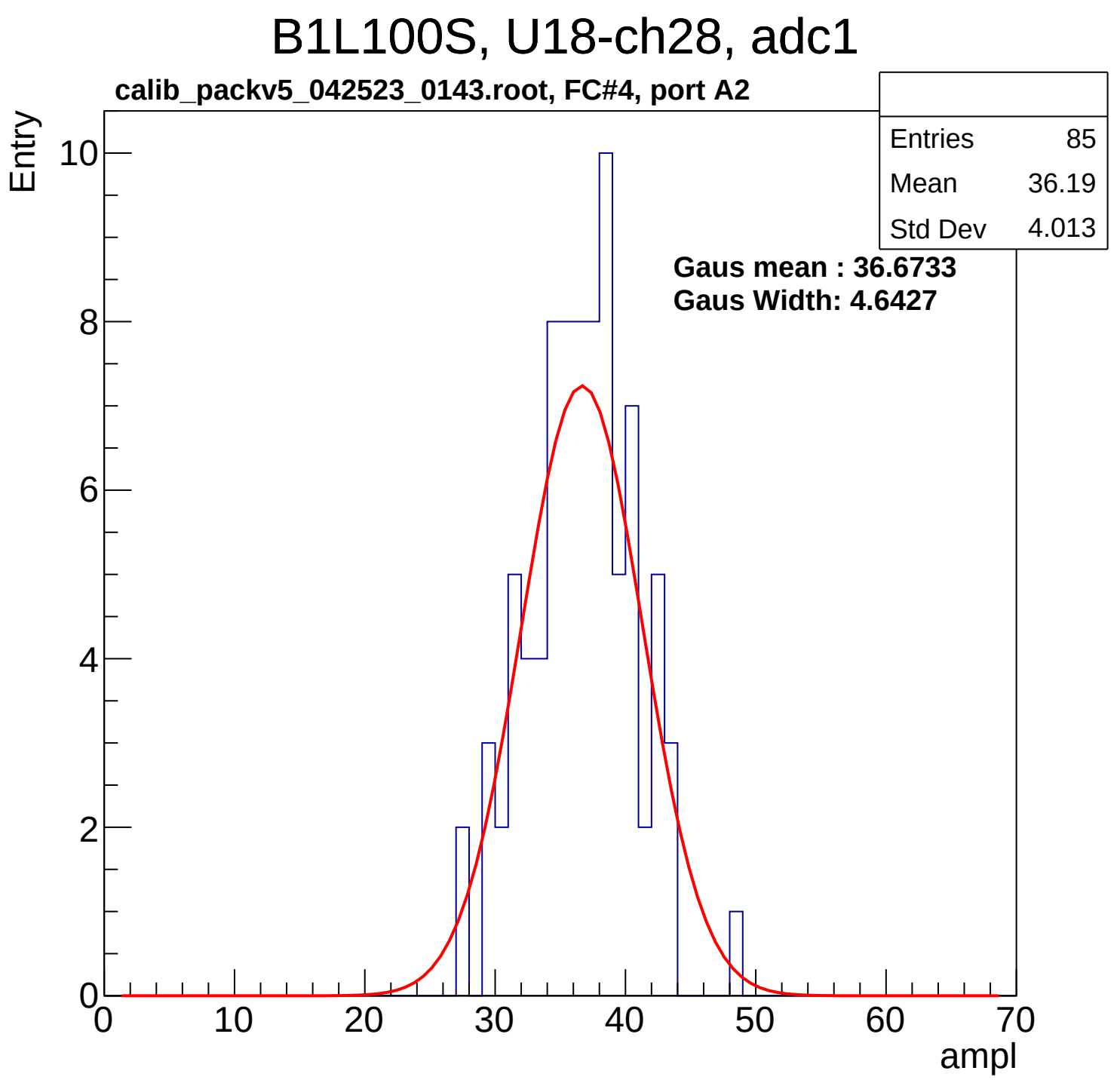

B1L100S, U18-ch27, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 55.88
Std Dev 7.95
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

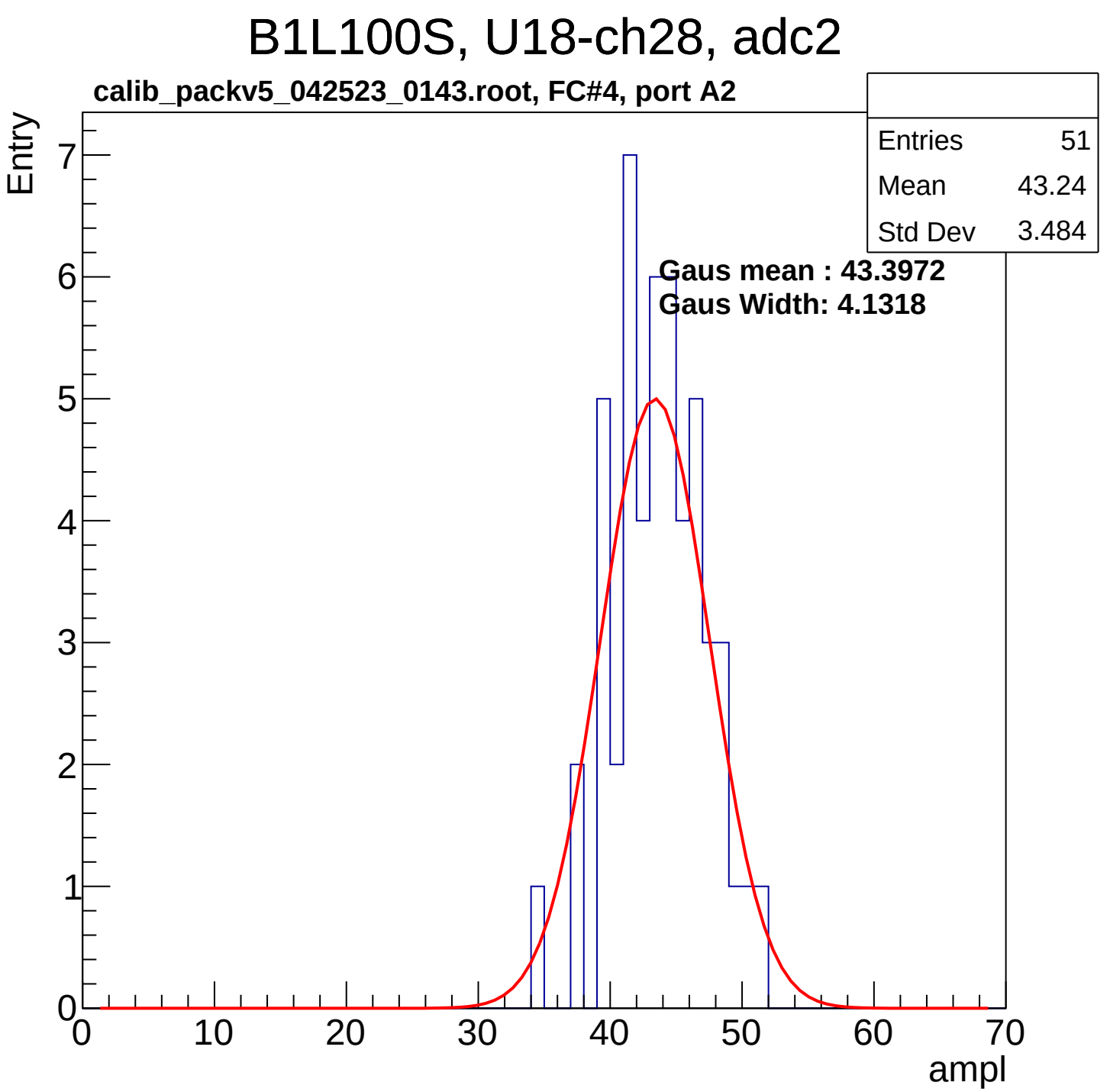

B1L100S, U18-ch27, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 36
Mean 60.11
Std Dev 2.413
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

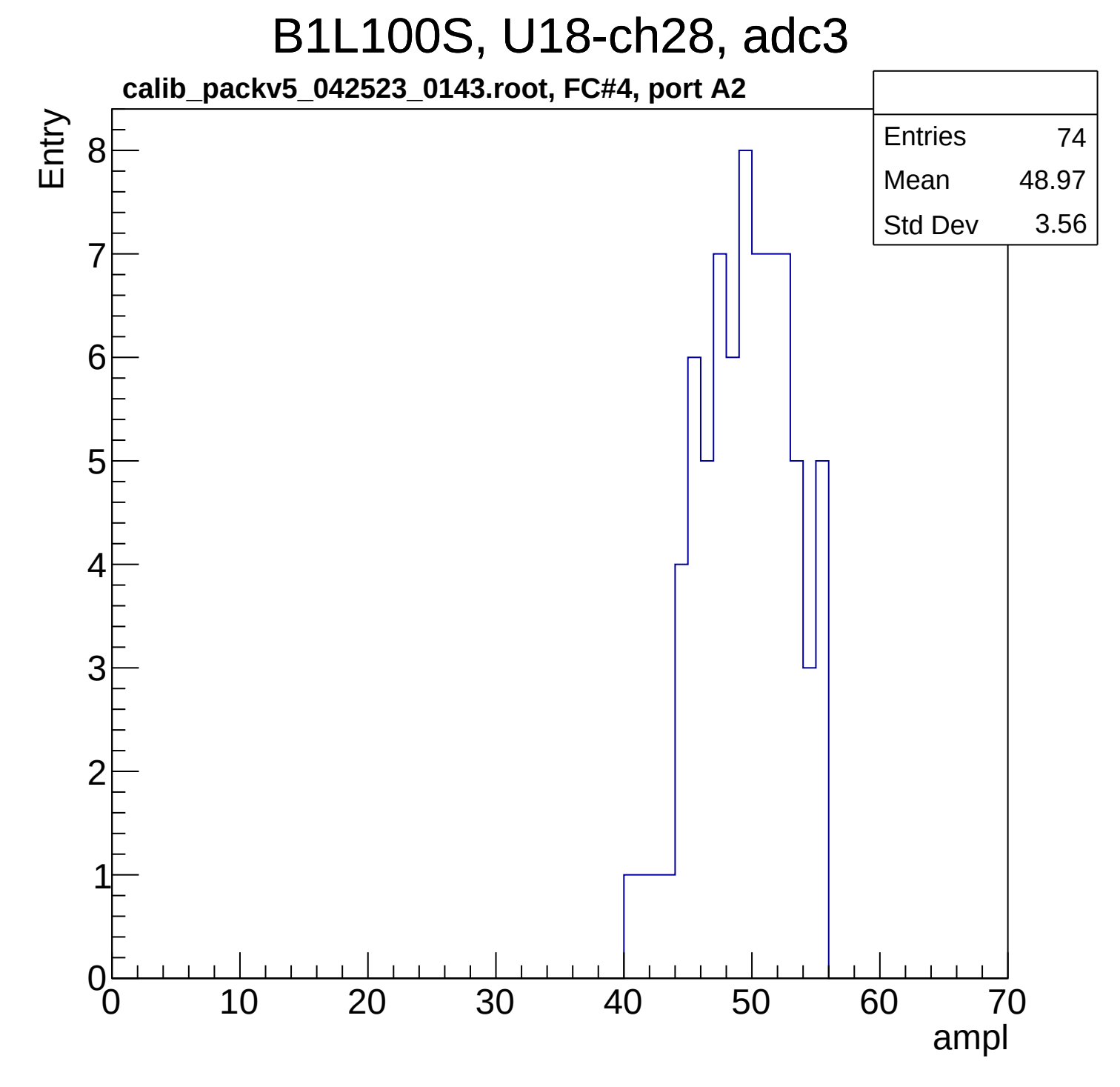

B1L100S, U18-ch27, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

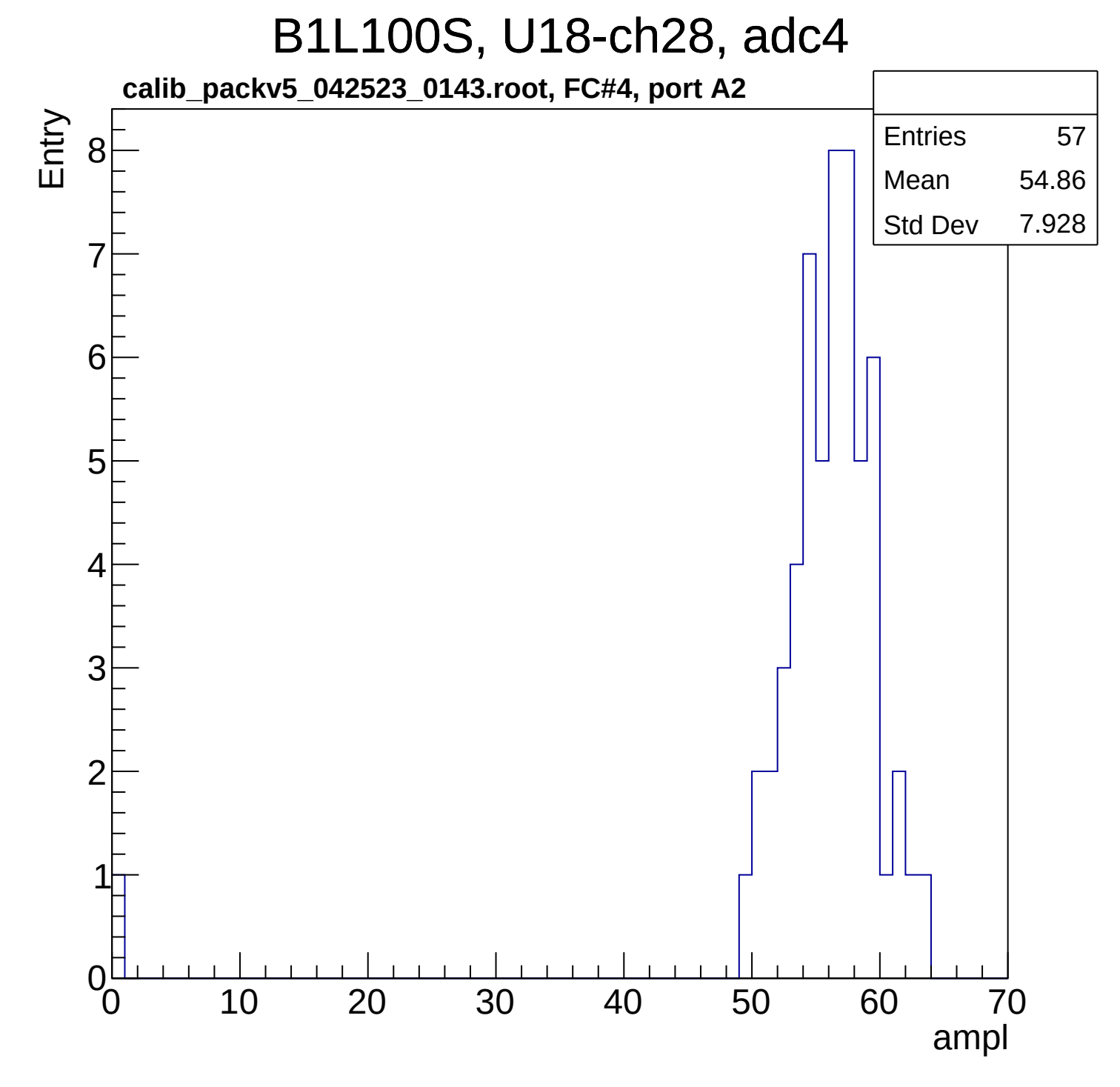

B1L100S, U18-ch27, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

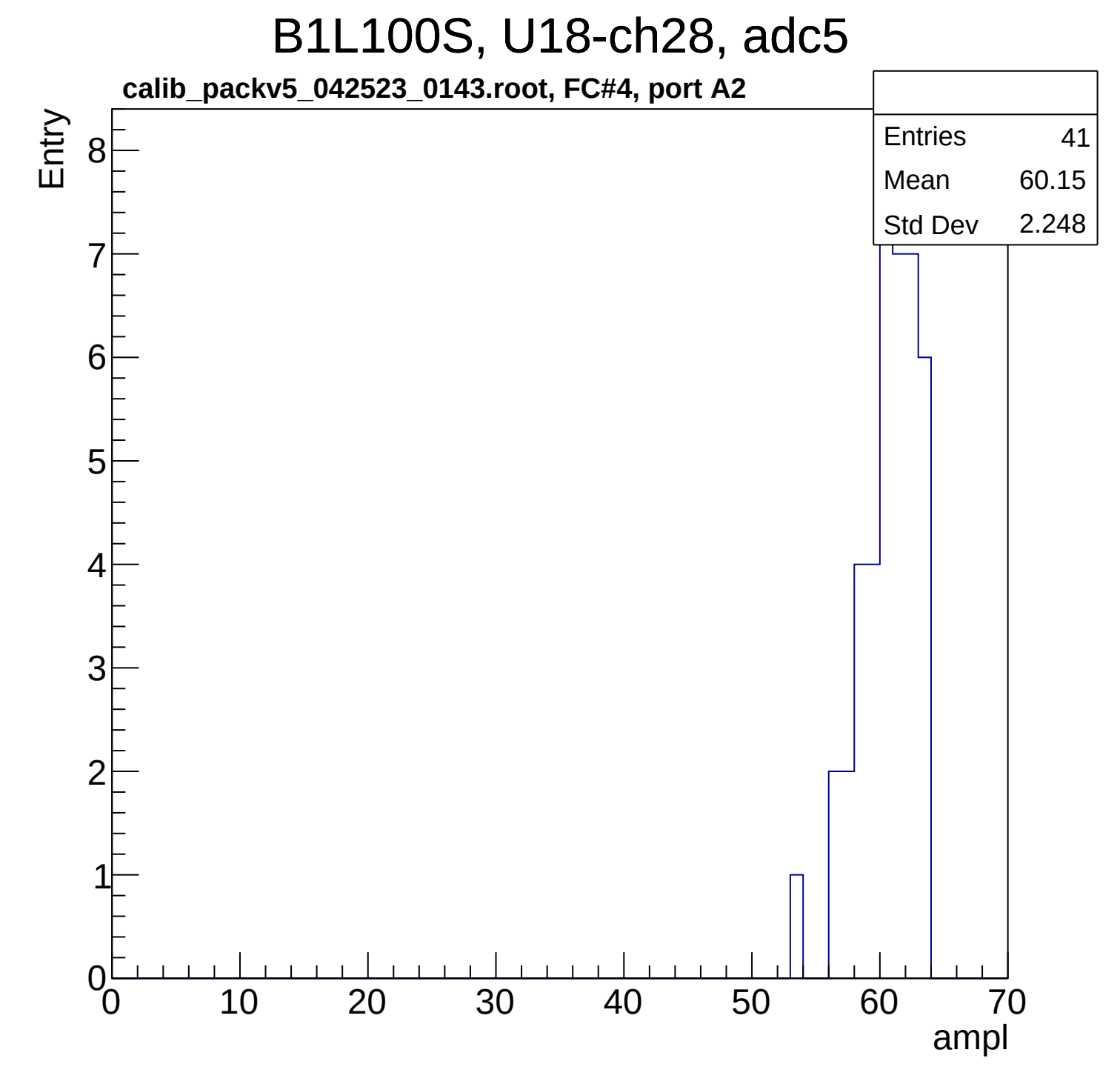

B1L100S, U18-ch28, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 28.77
Std Dev 4.76
Gaus mean : 29.5613
Gaus Width: 3.0764
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

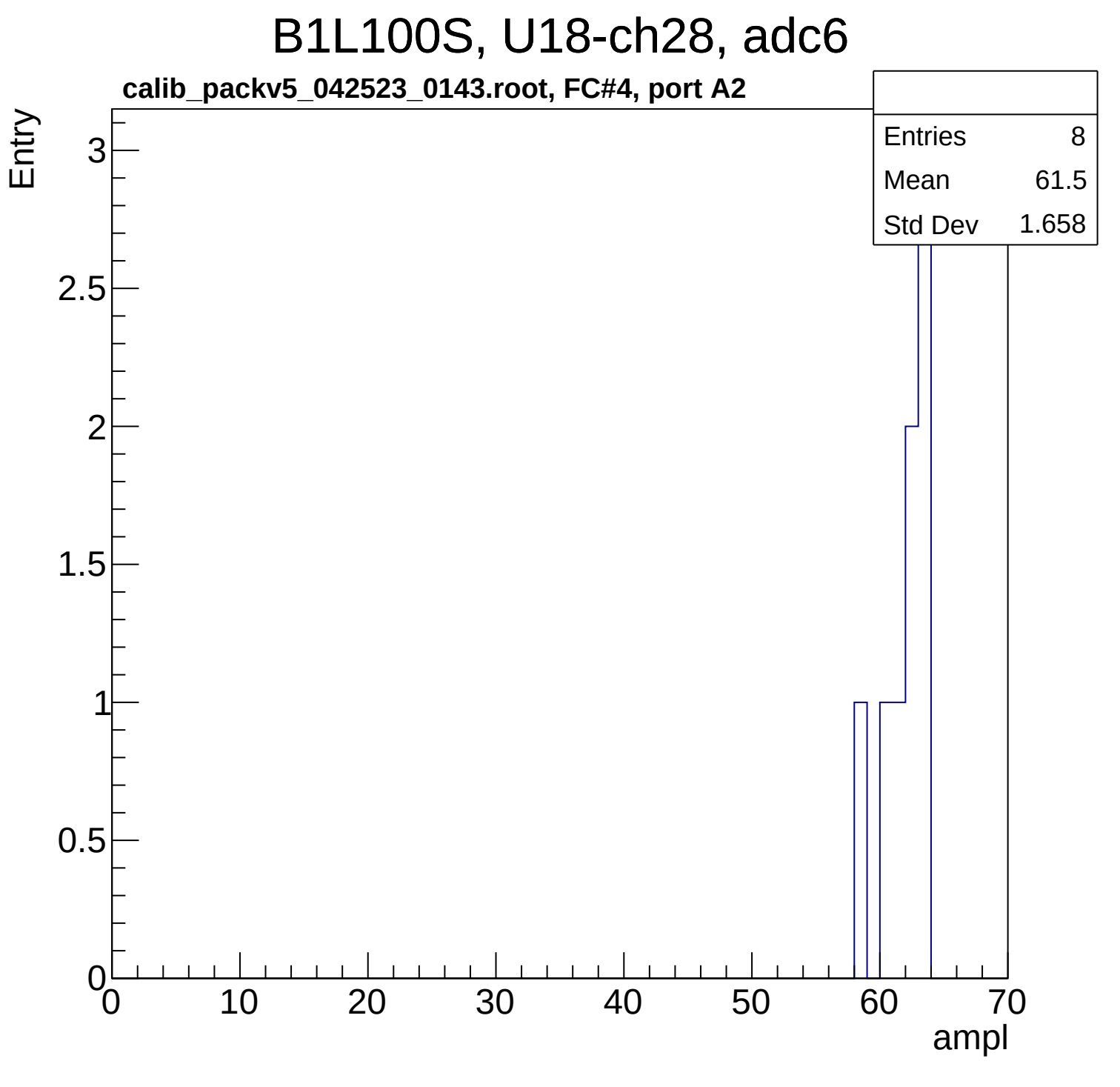

B1L100S, U18-ch28, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 85
Mean 36.19
Std Dev 4.013
Gaus mean : 36.6733
Gaus Width: 4.6427
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

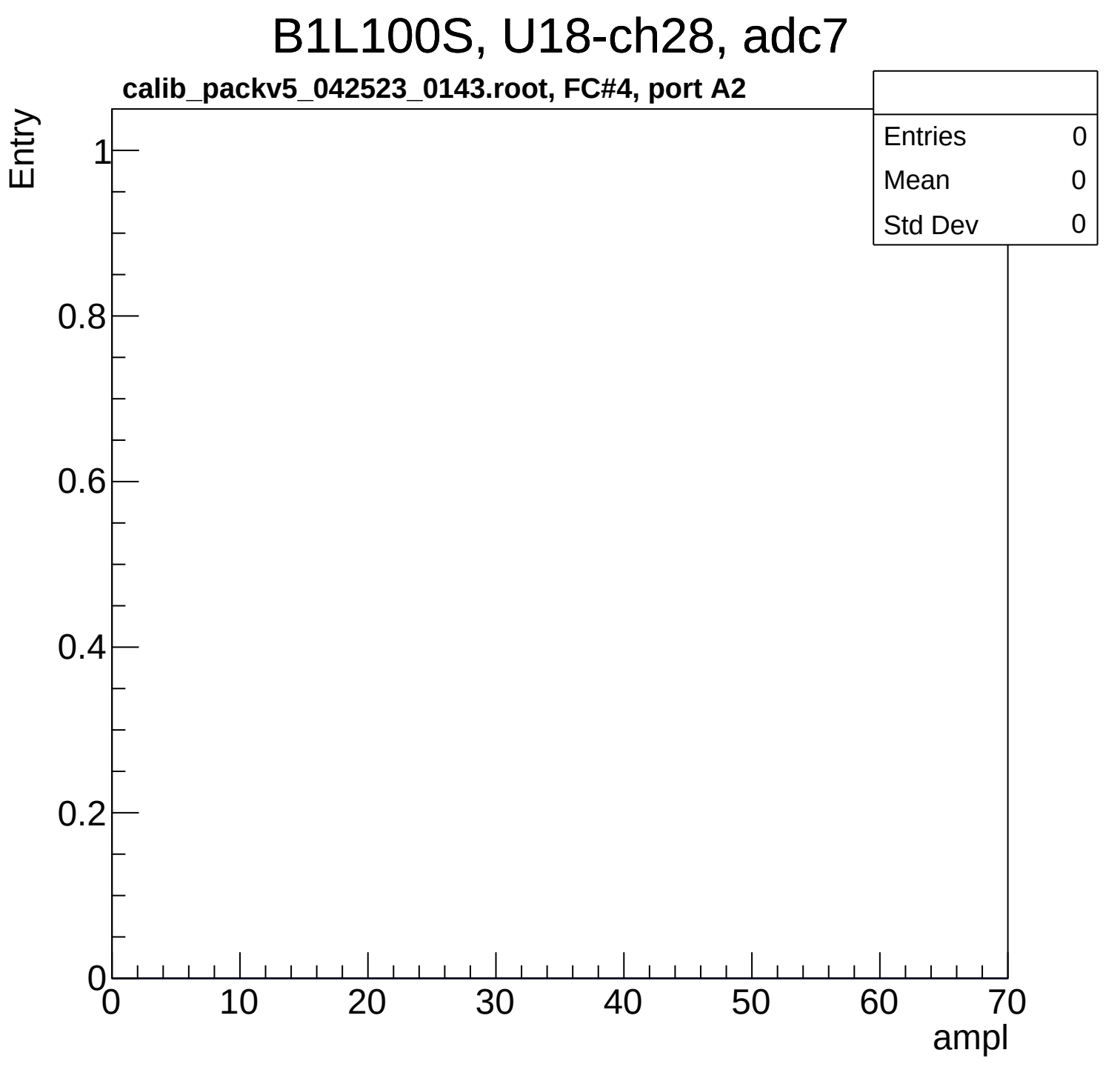

B1L100S, U18-ch28, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 43.24
Std Dev 3.484
Gaus mean : 43.3972
Gaus Width: 4.1318
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

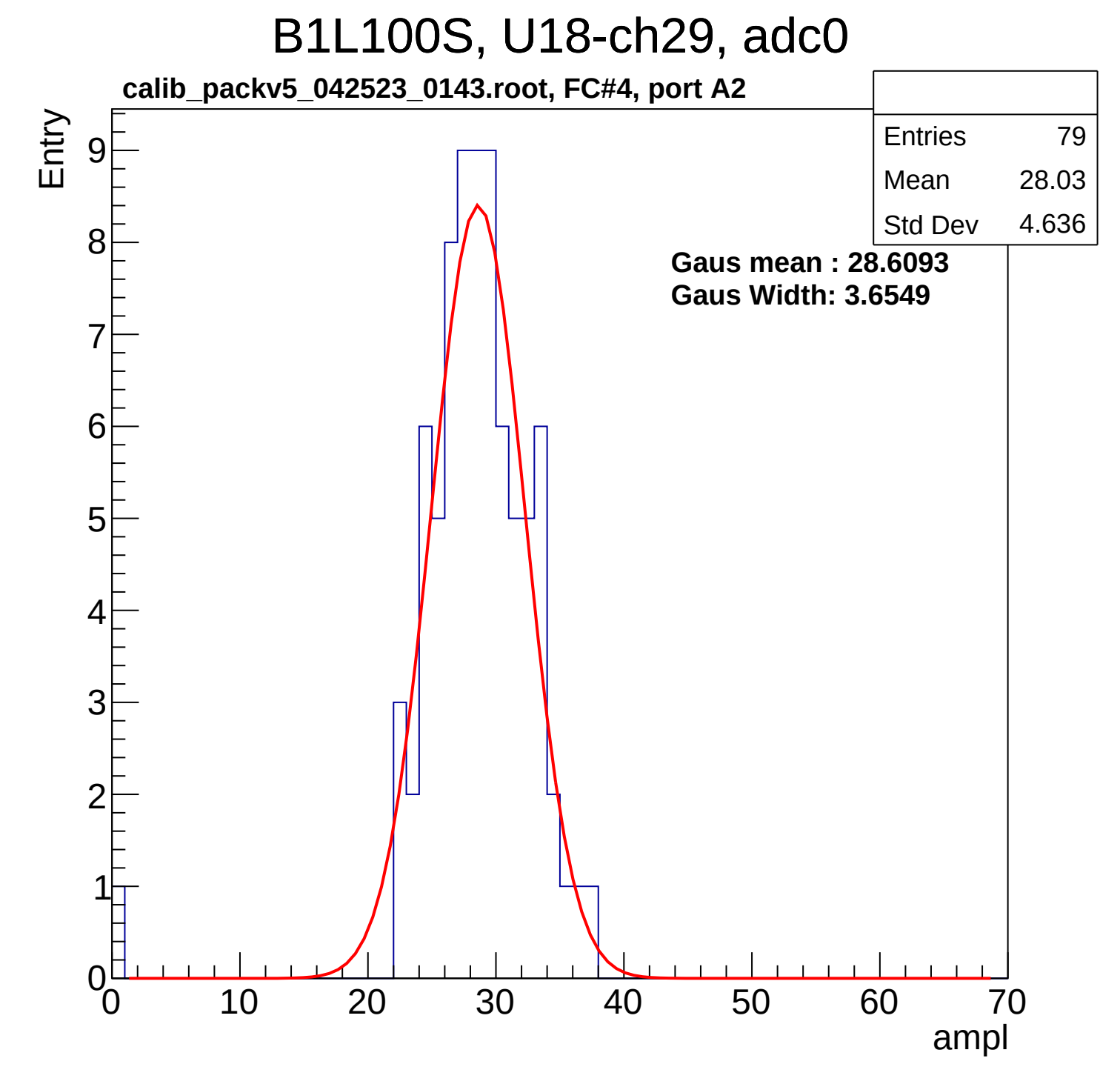

B1L100S, U18-ch28, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 48.97
Std Dev 3.56
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

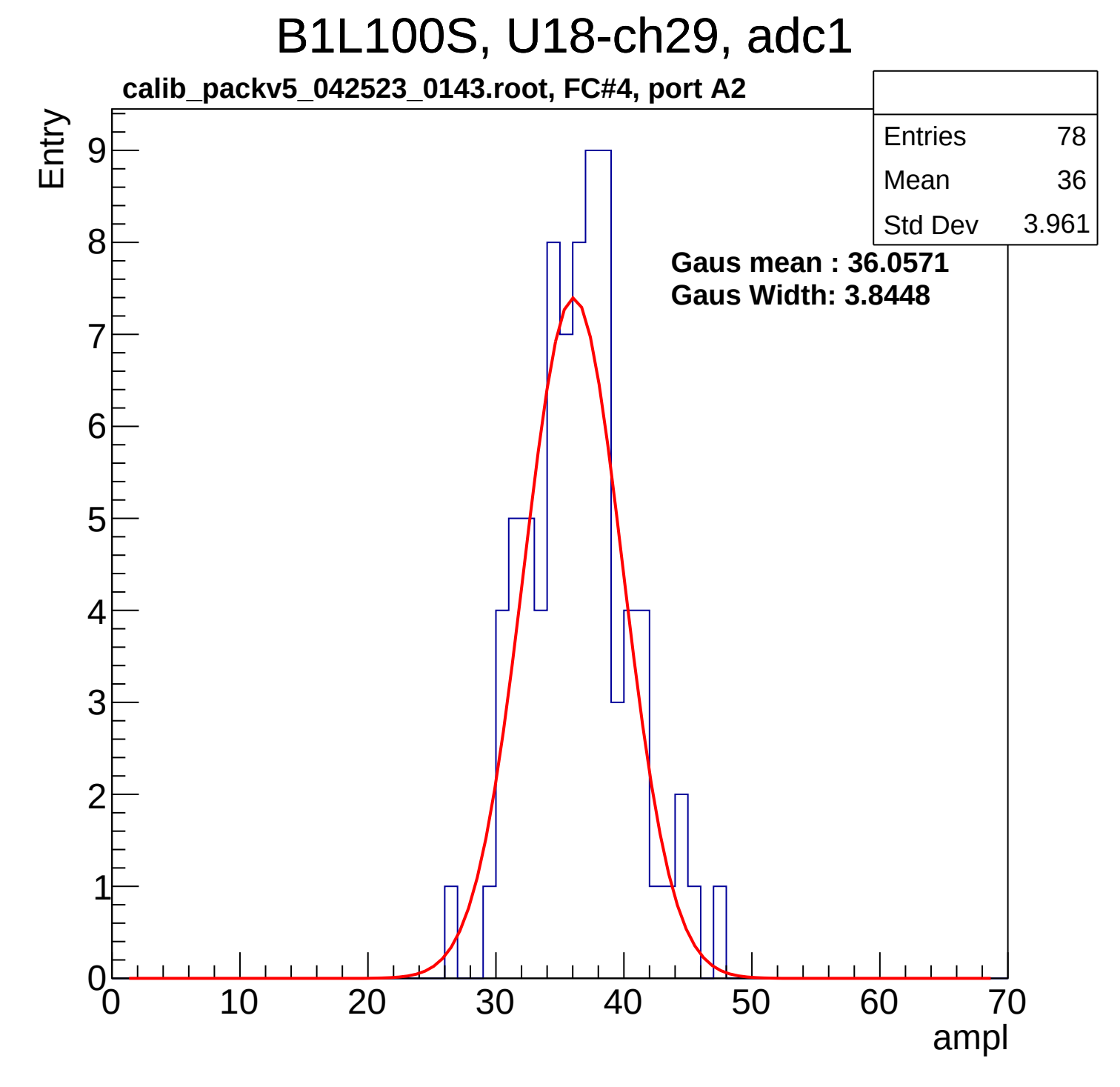

B1L100S, U18-ch28, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 54.86
Std Dev 7.928
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

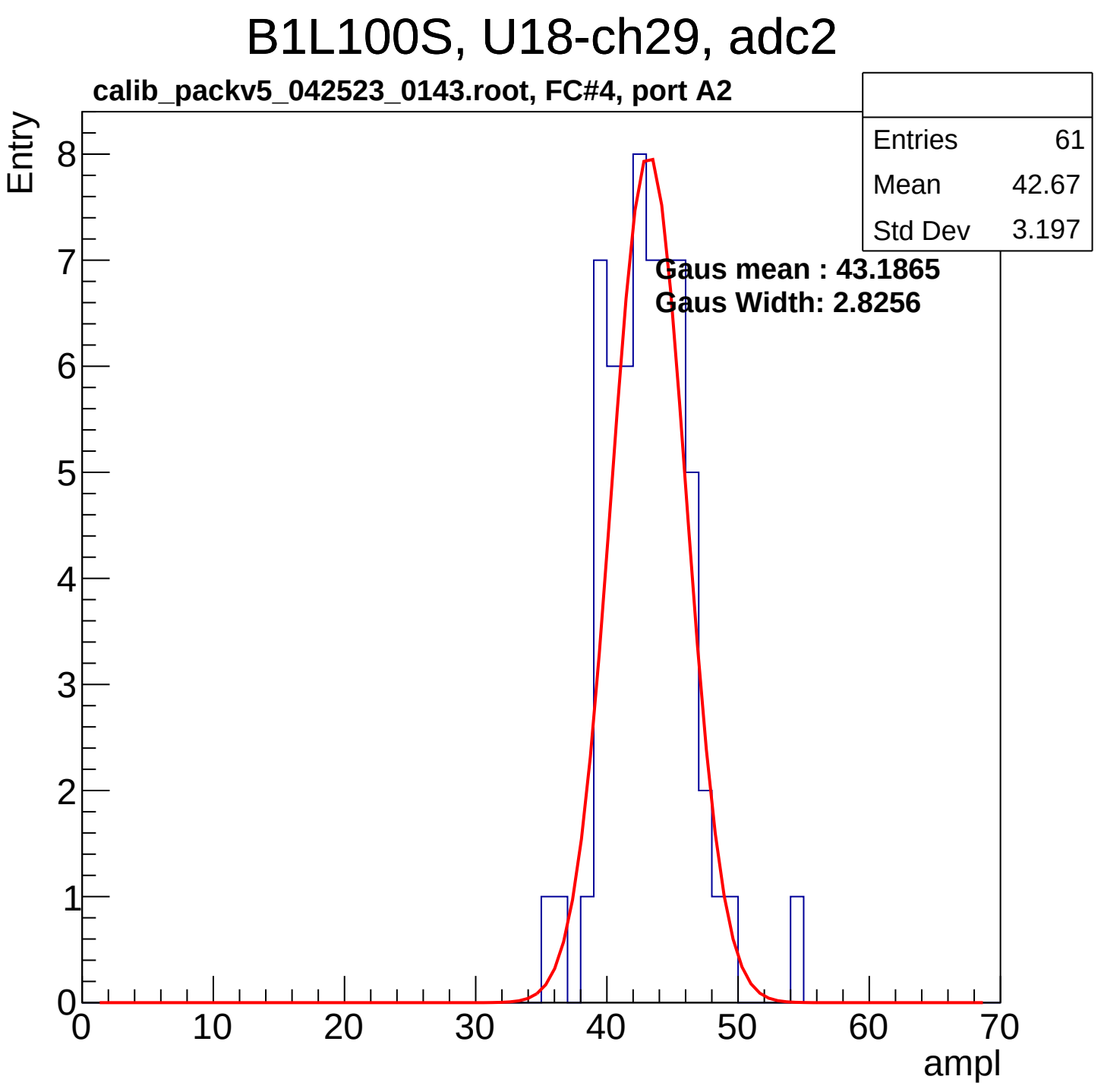

B1L100S, U18-ch28, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 41
Mean 60.15
Std Dev 2.248
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

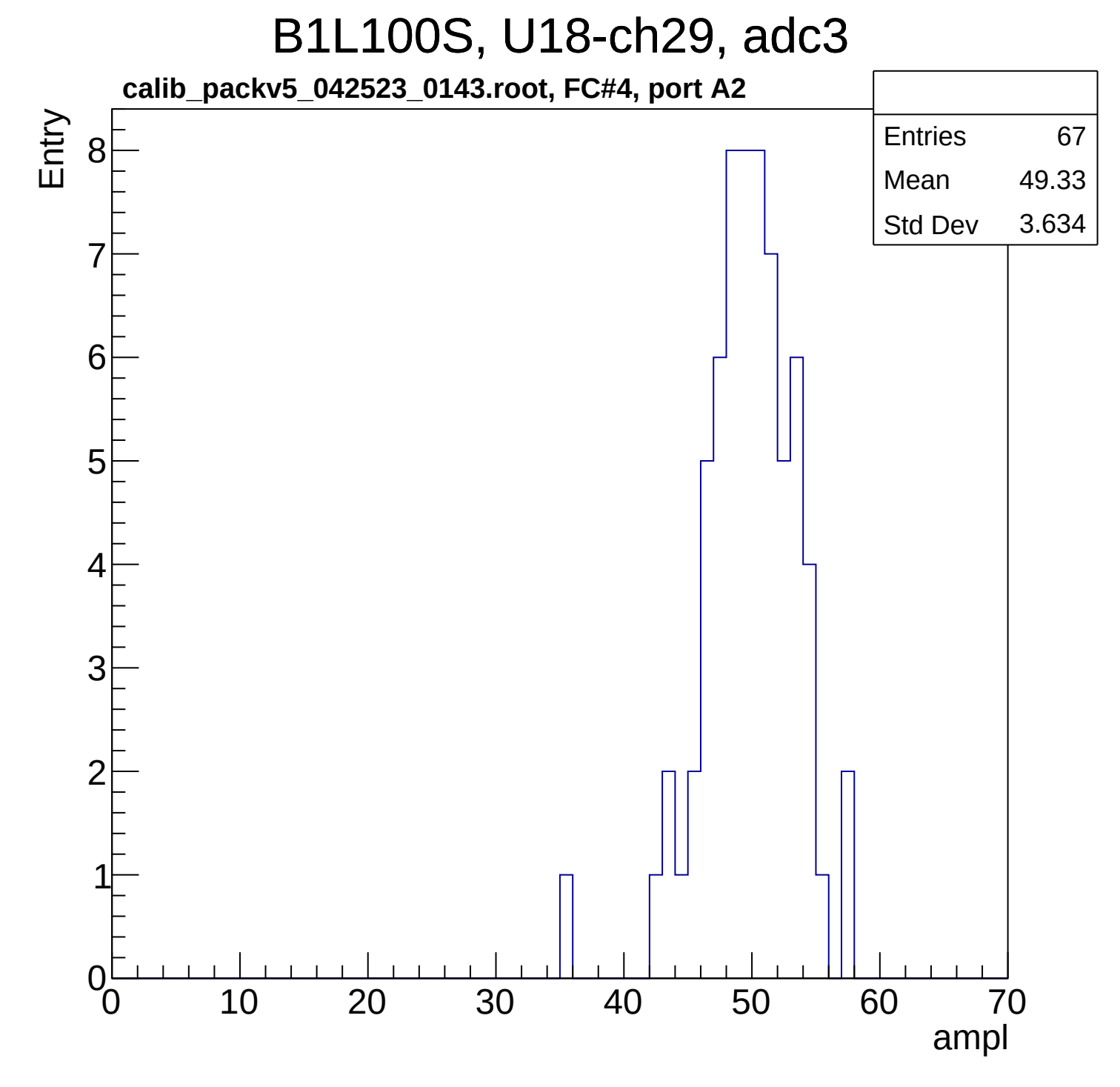

B1L100S, U18-ch28, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 8
Mean 61.5
Std Dev 1.658
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

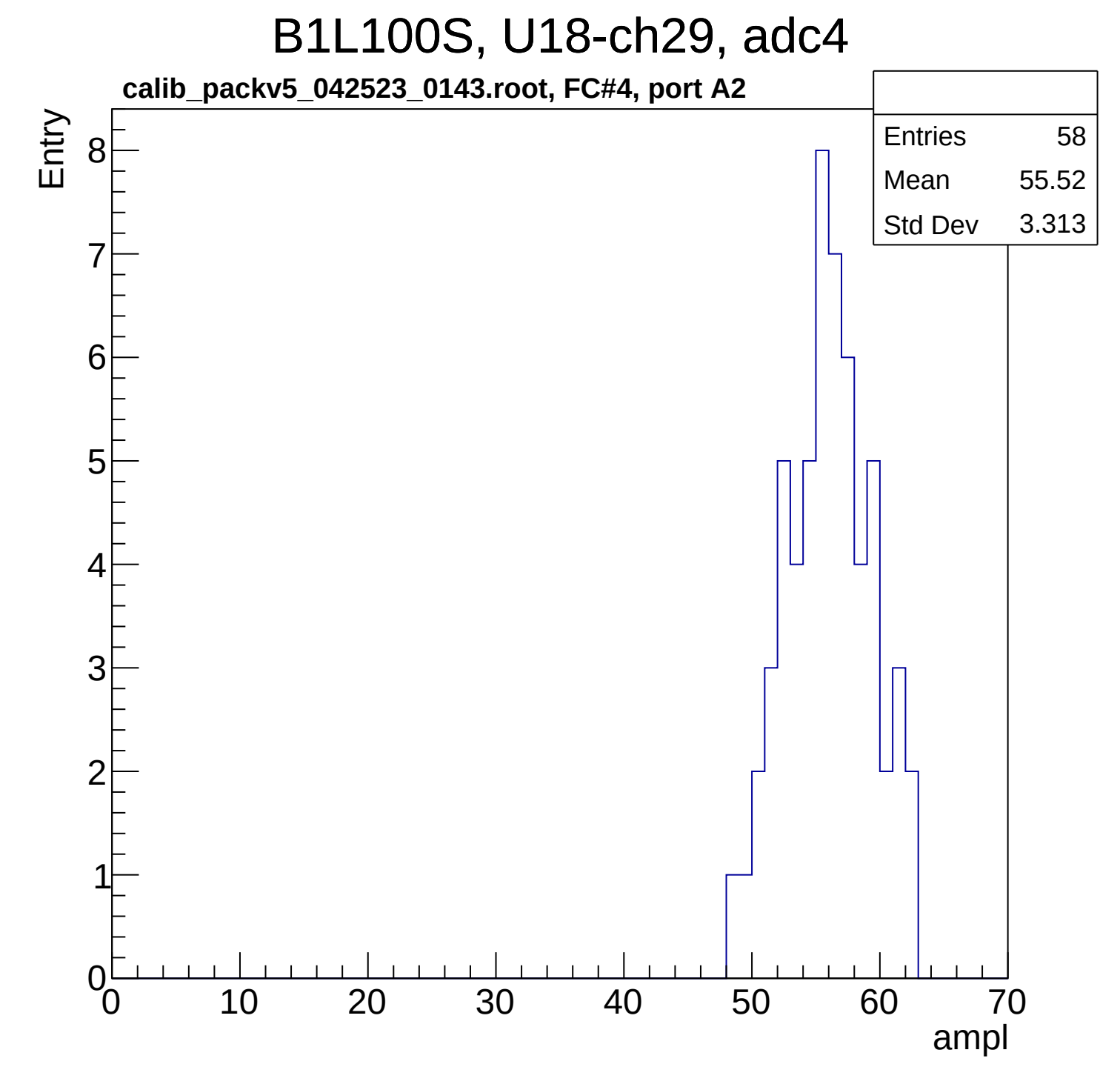

B1L100S, U18-ch28, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

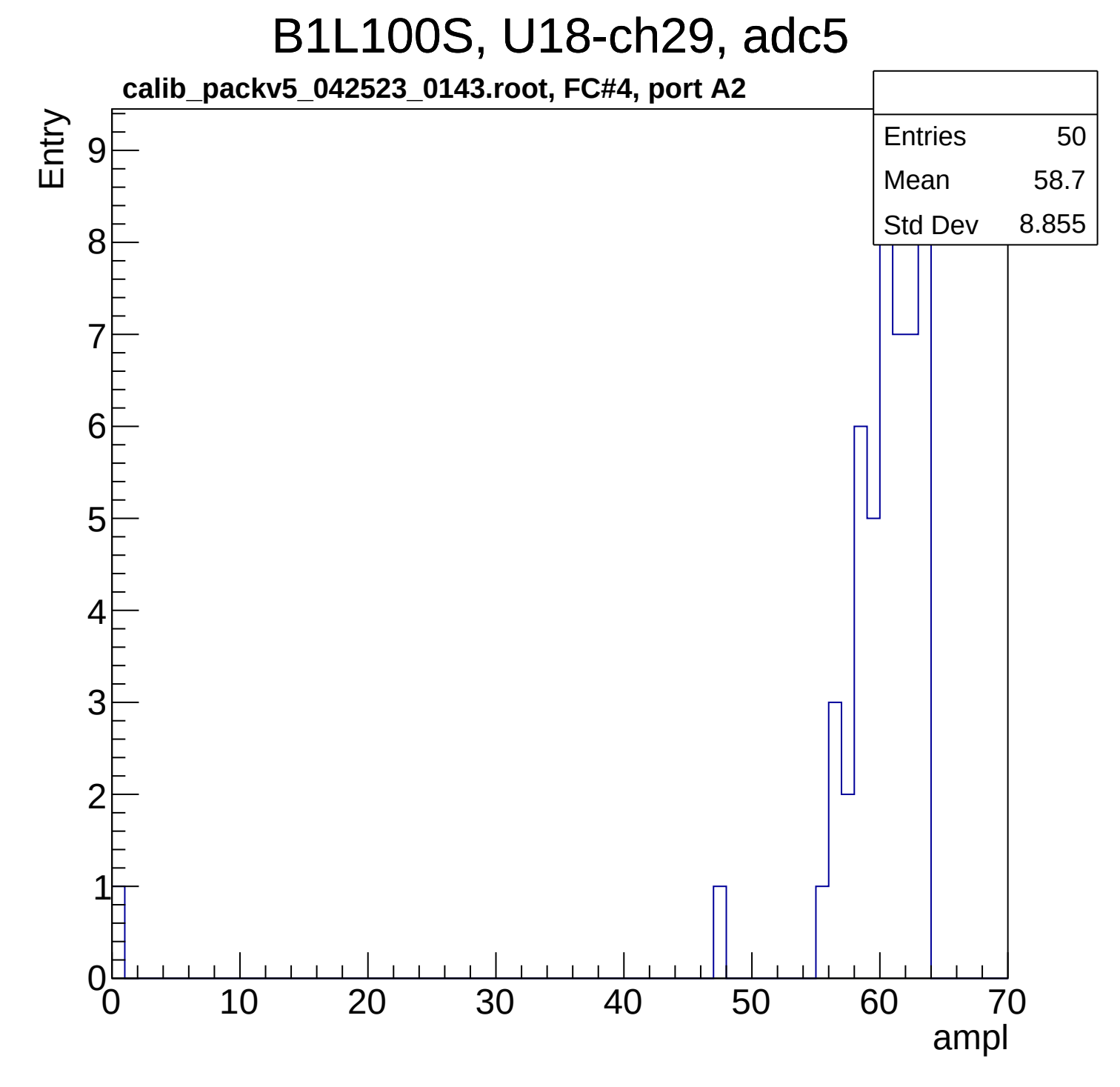

B1L100S, U18-ch29, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 28.03
Std Dev 4.636
Gaus mean : 28.6093
Gaus Width: 3.6549
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

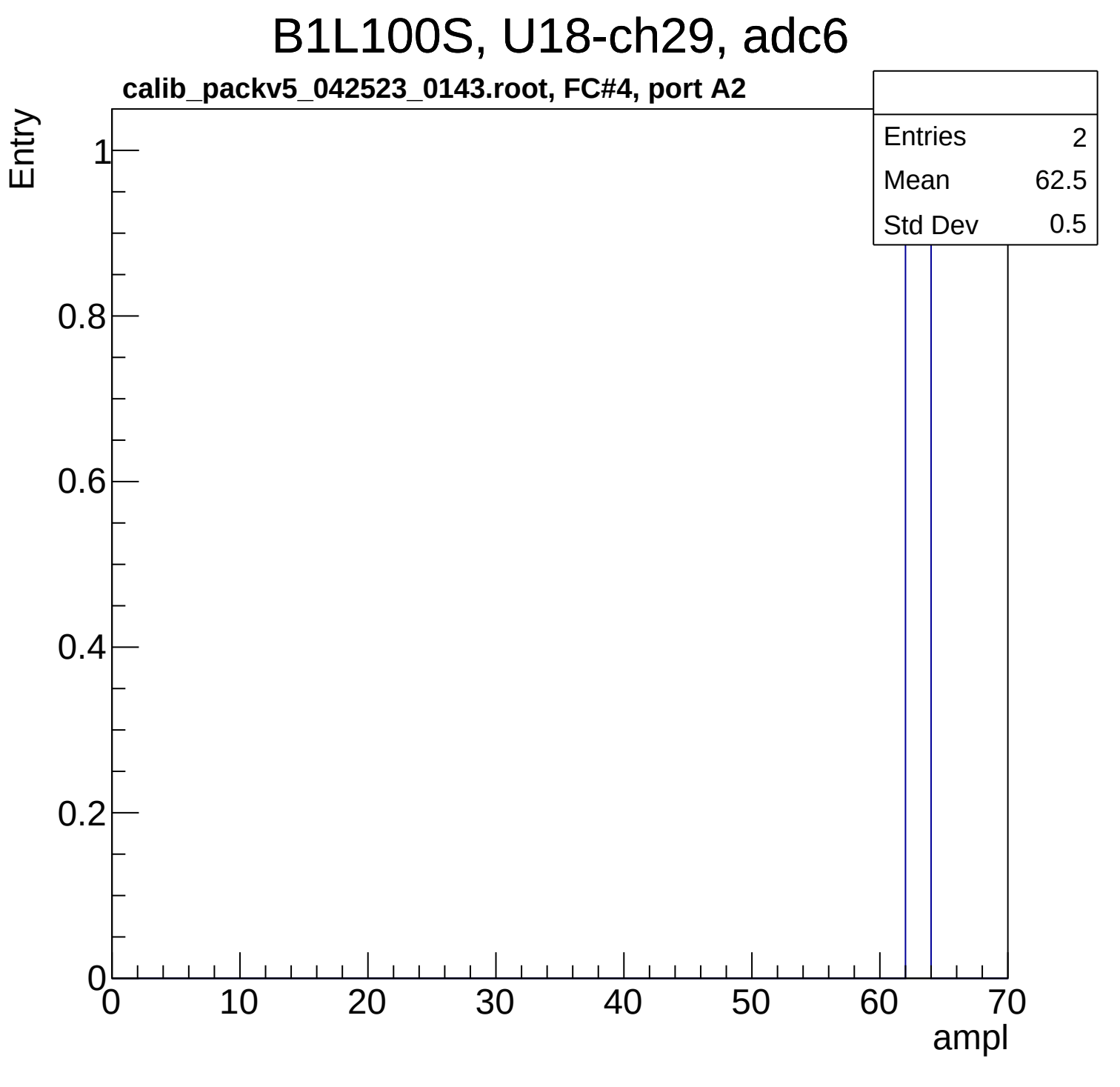

B1L100S, U18-ch29, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 36
Std Dev 3.961
Gaus mean : 36.0571
Gaus Width: 3.8448
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

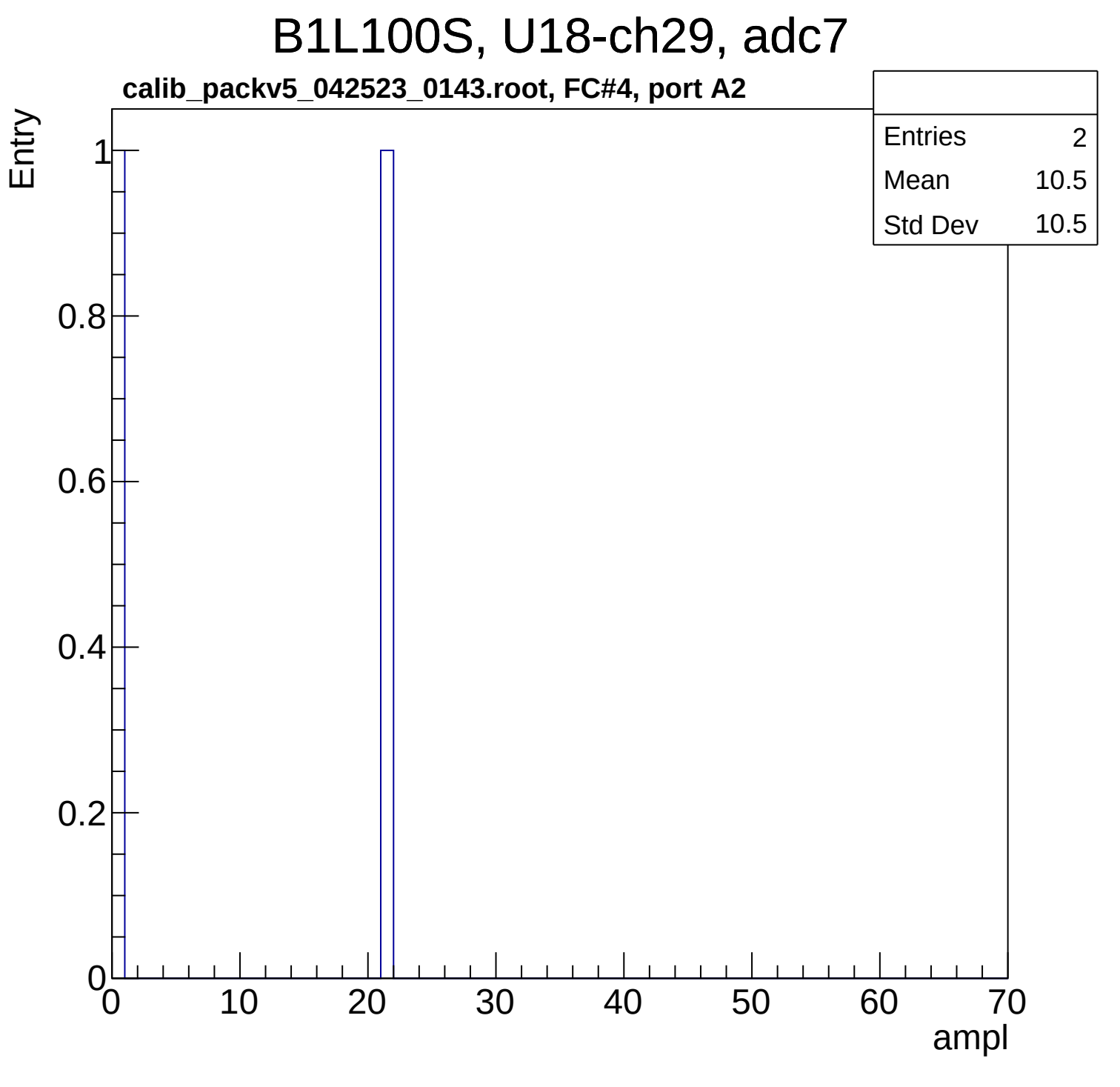

B1L100S, U18-ch29, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 42.67
Std Dev 3.197
Gaus mean : 43.1865
Gaus Width: 2.8256
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

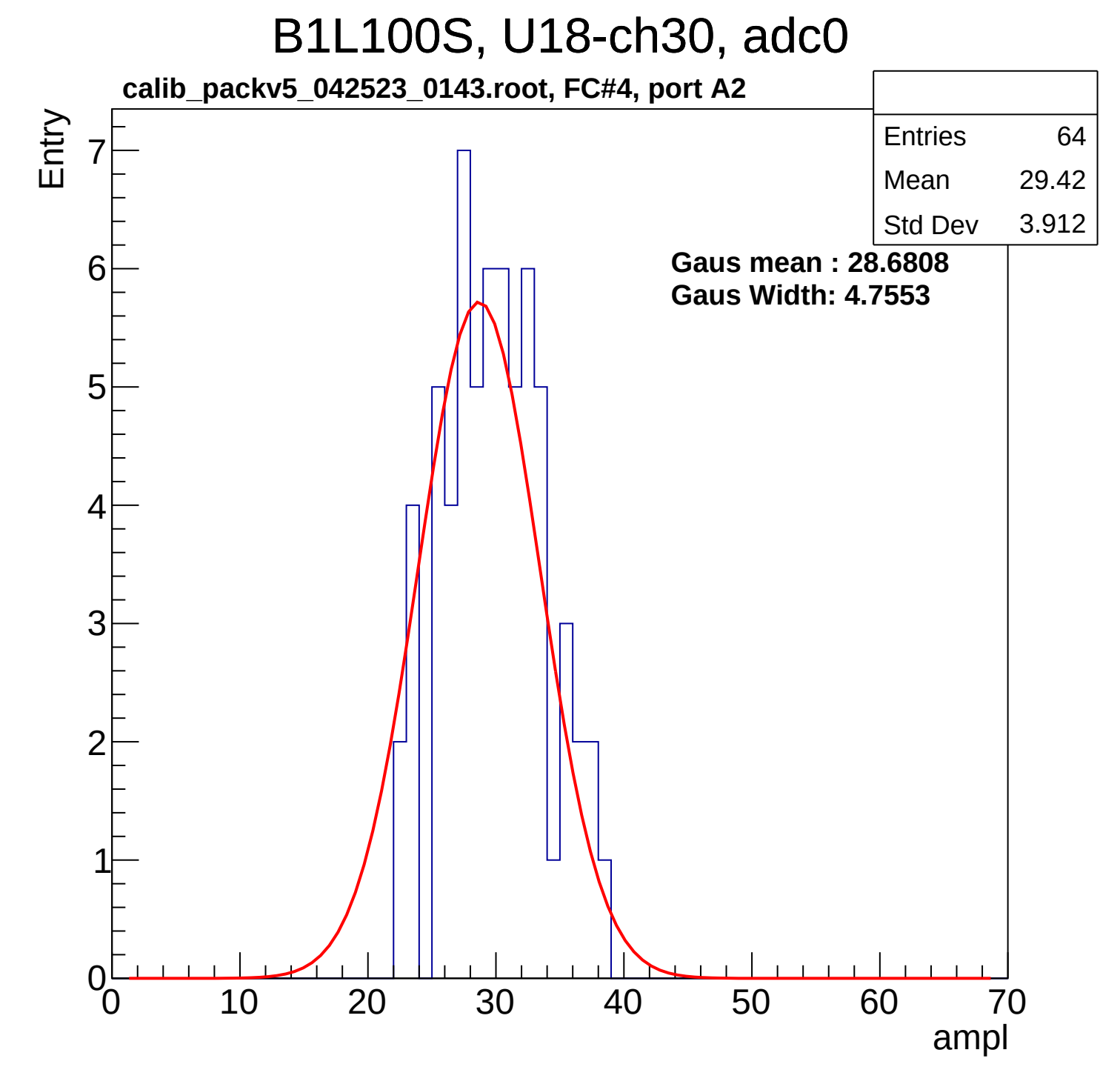

B1L100S, U18-ch29, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 49.33
Std Dev 3.634
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

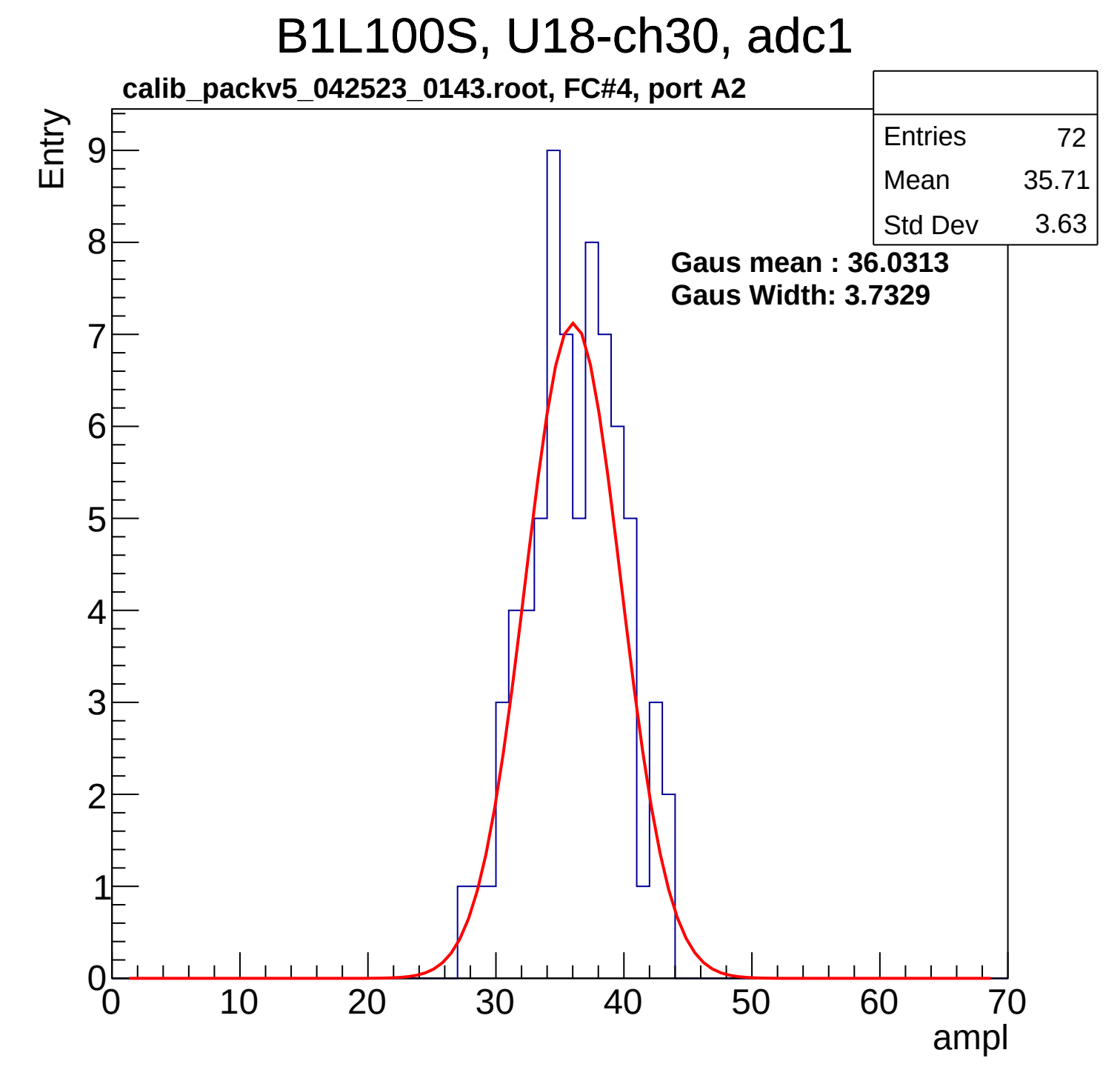

B1L100S, U18-ch29, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 55.52
Std Dev 3.313
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

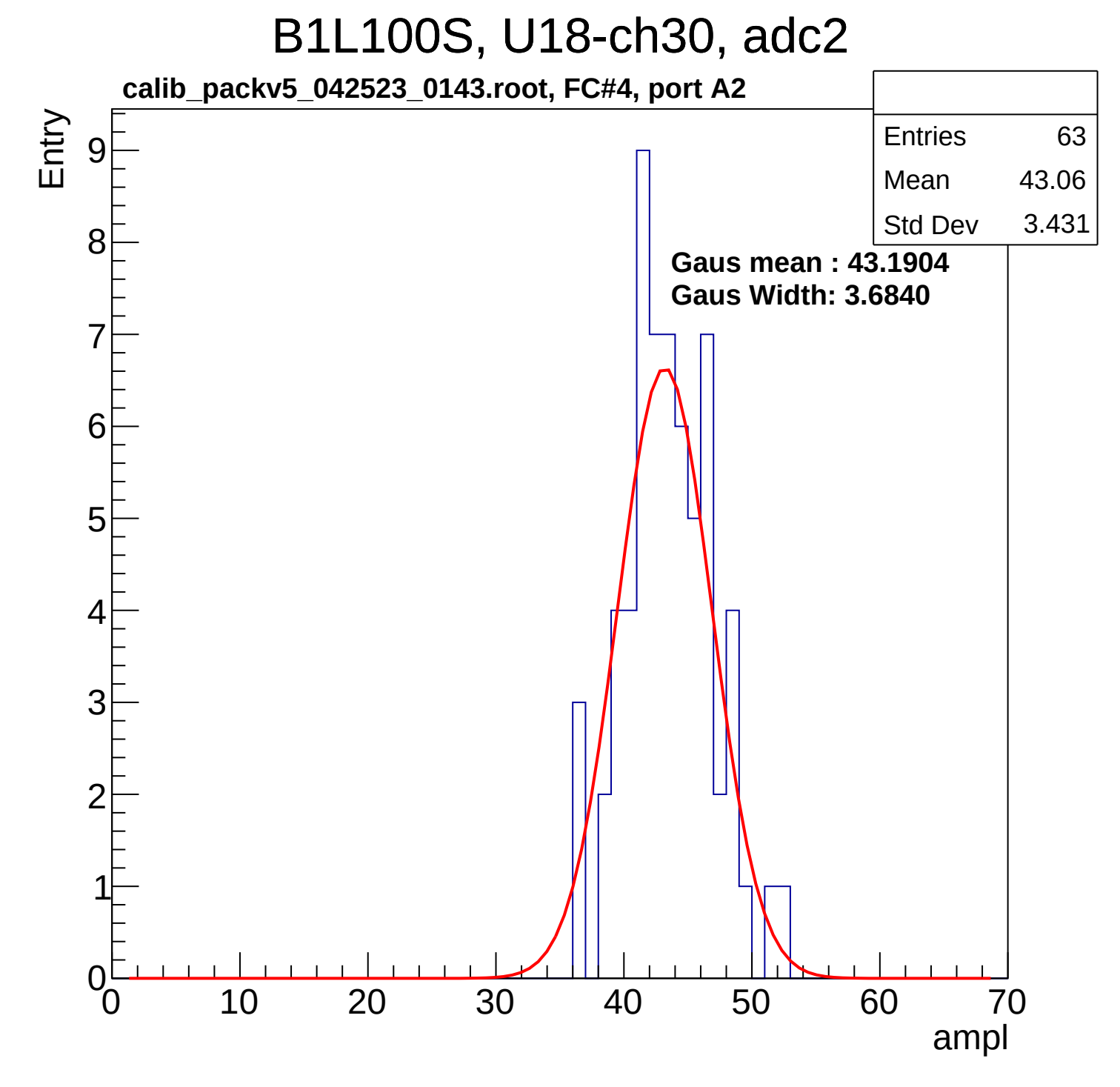

B1L100S, U18-ch29, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 58.7
Std Dev 8.855
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

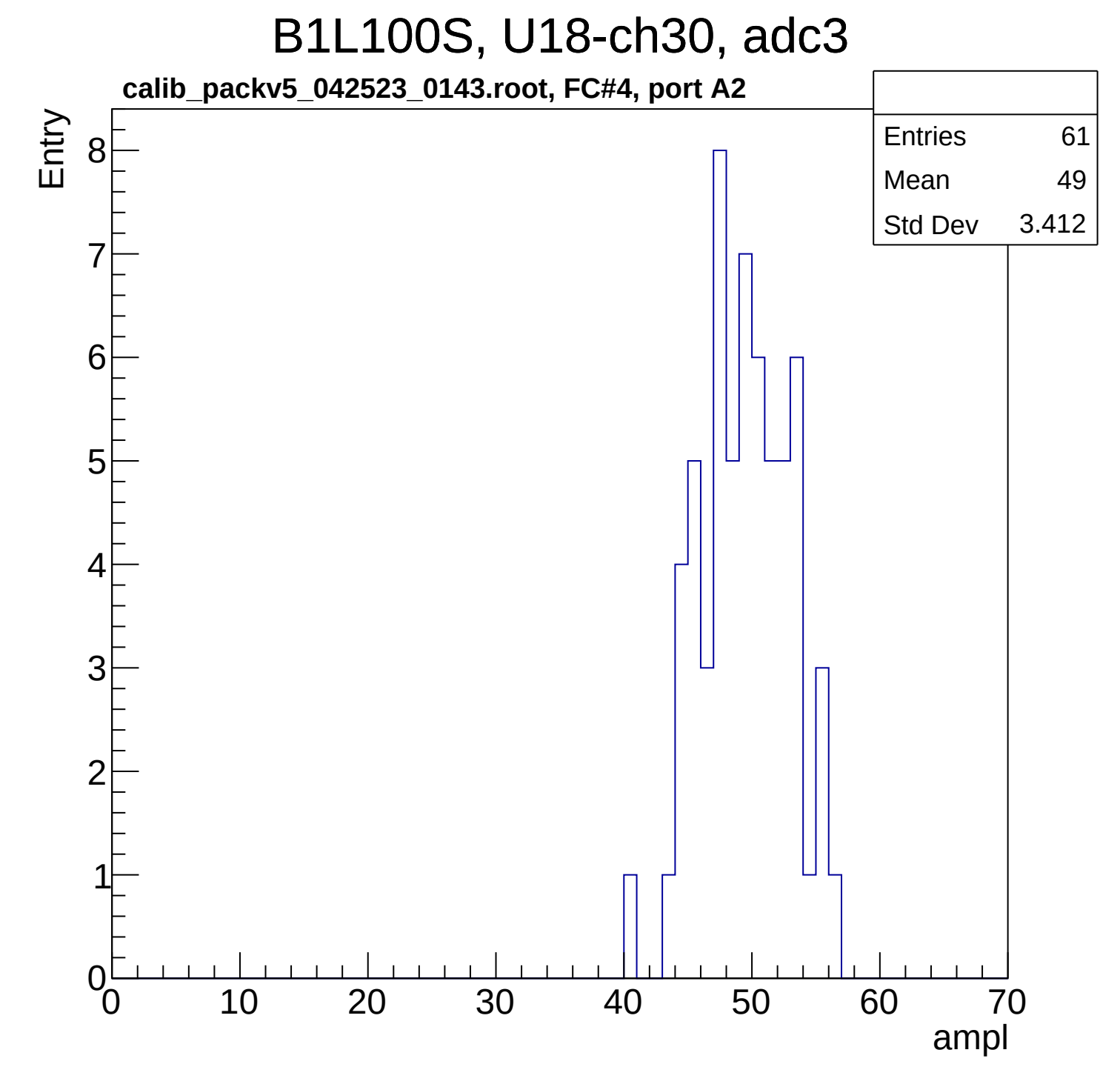

B1L100S, U18-ch29, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

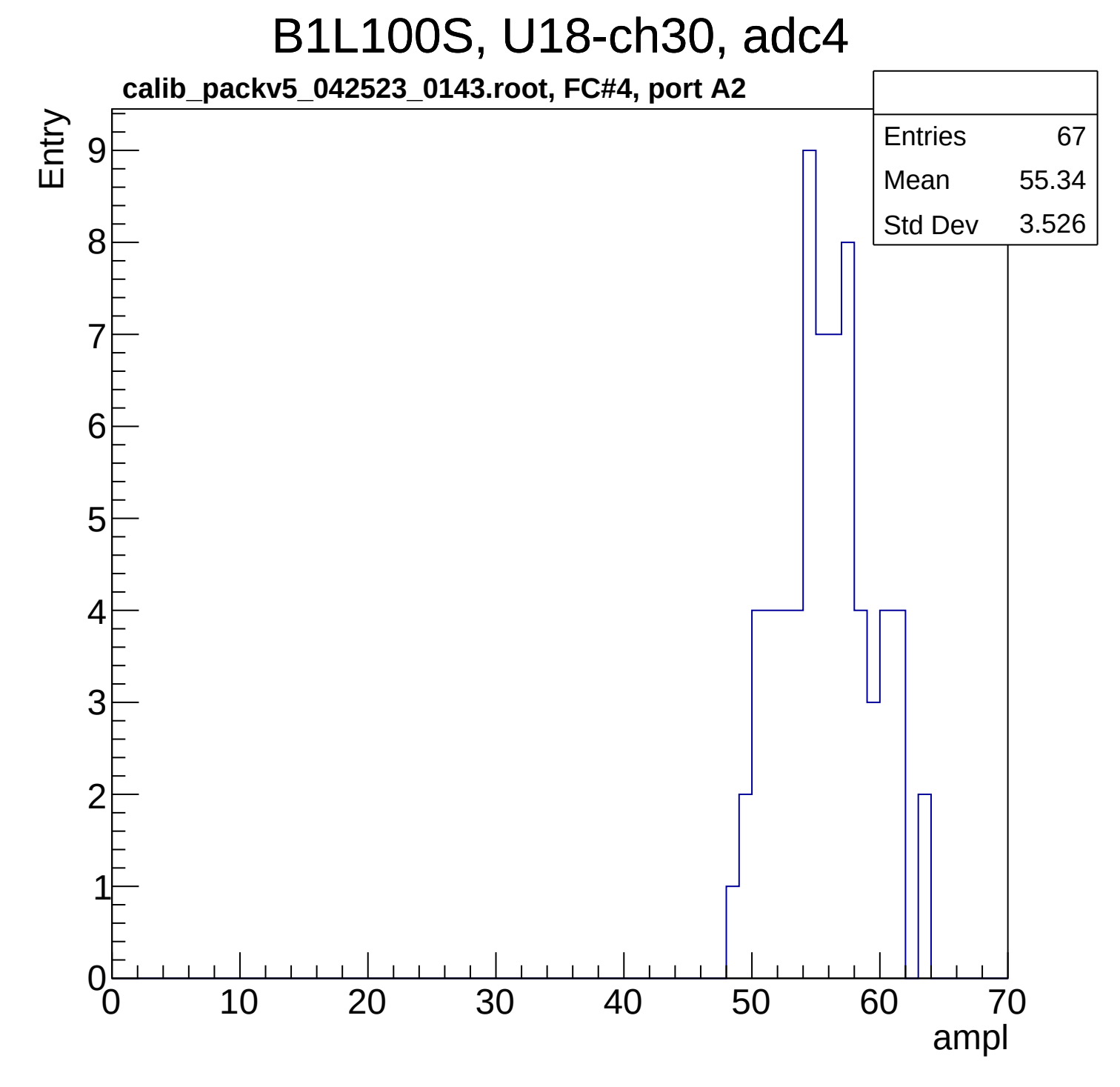

B1L100S, U18-ch29, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 10.5
Std Dev 10.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

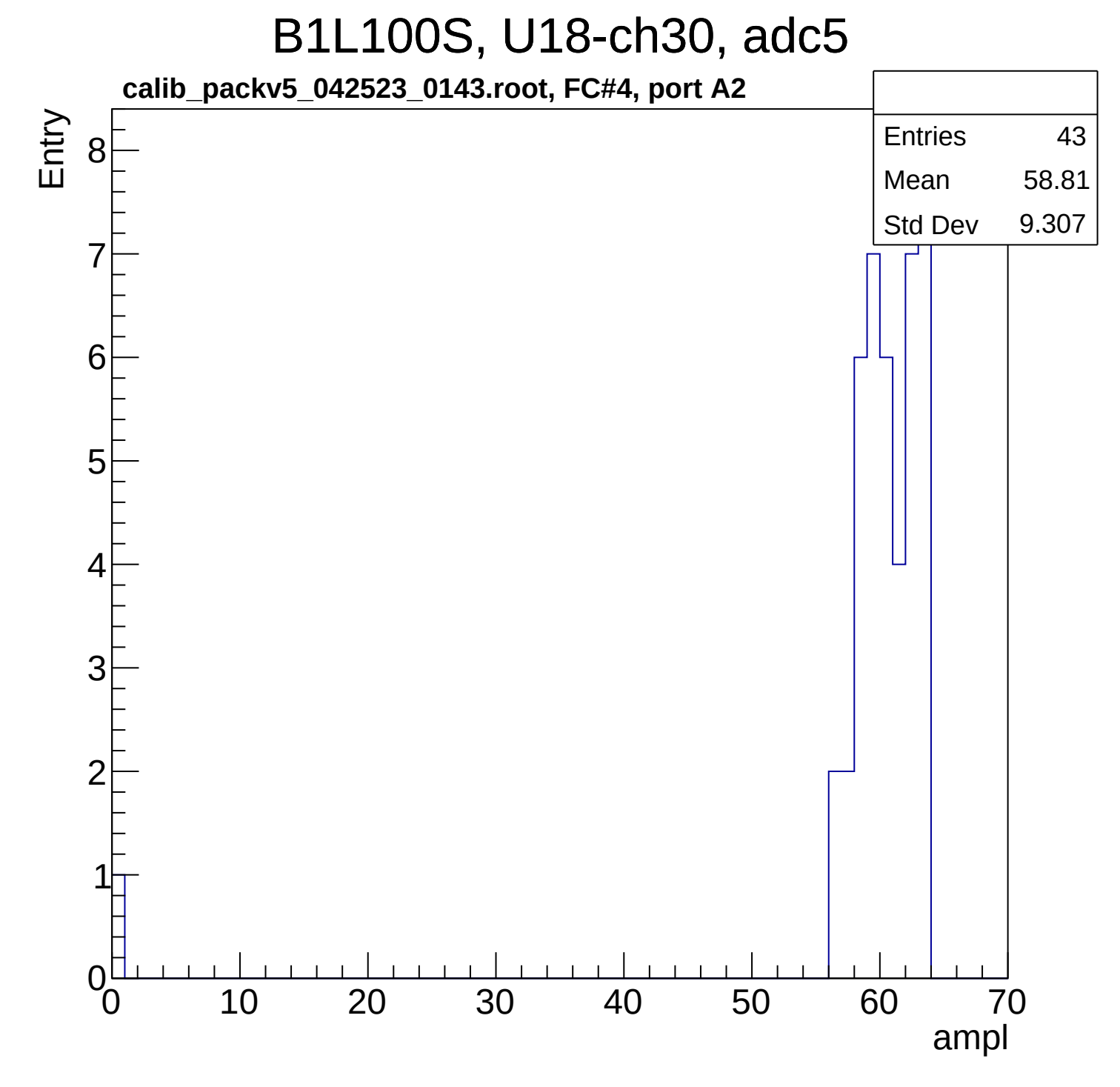

B1L100S, U18-ch30, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 29.42
Std Dev 3.912
Gaus mean : 28.6808
Gaus Width: 4.7553
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

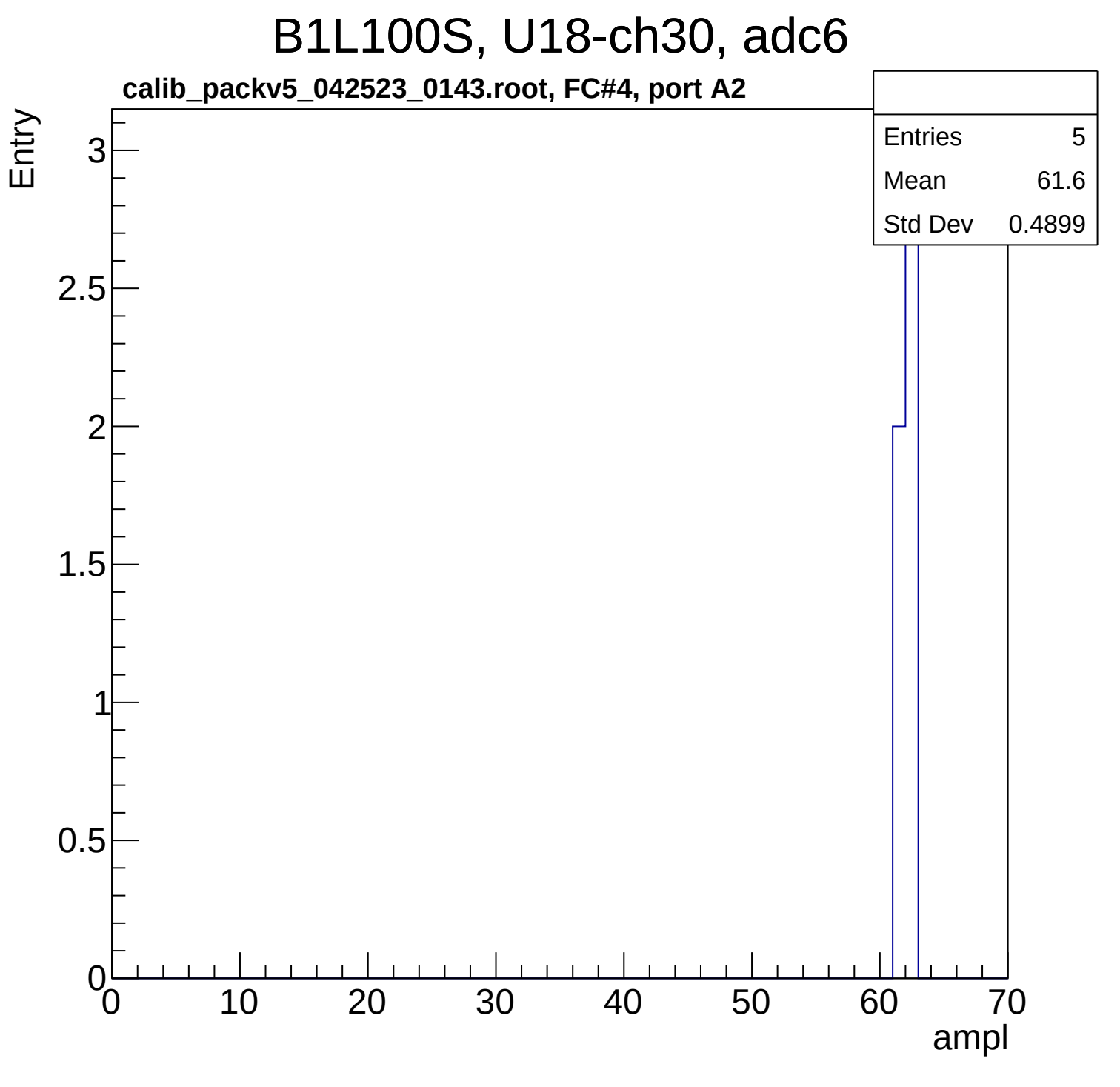

B1L100S, U18-ch30, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 35.71
Std Dev 3.63
Gaus mean : 36.0313
Gaus Width: 3.7329
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

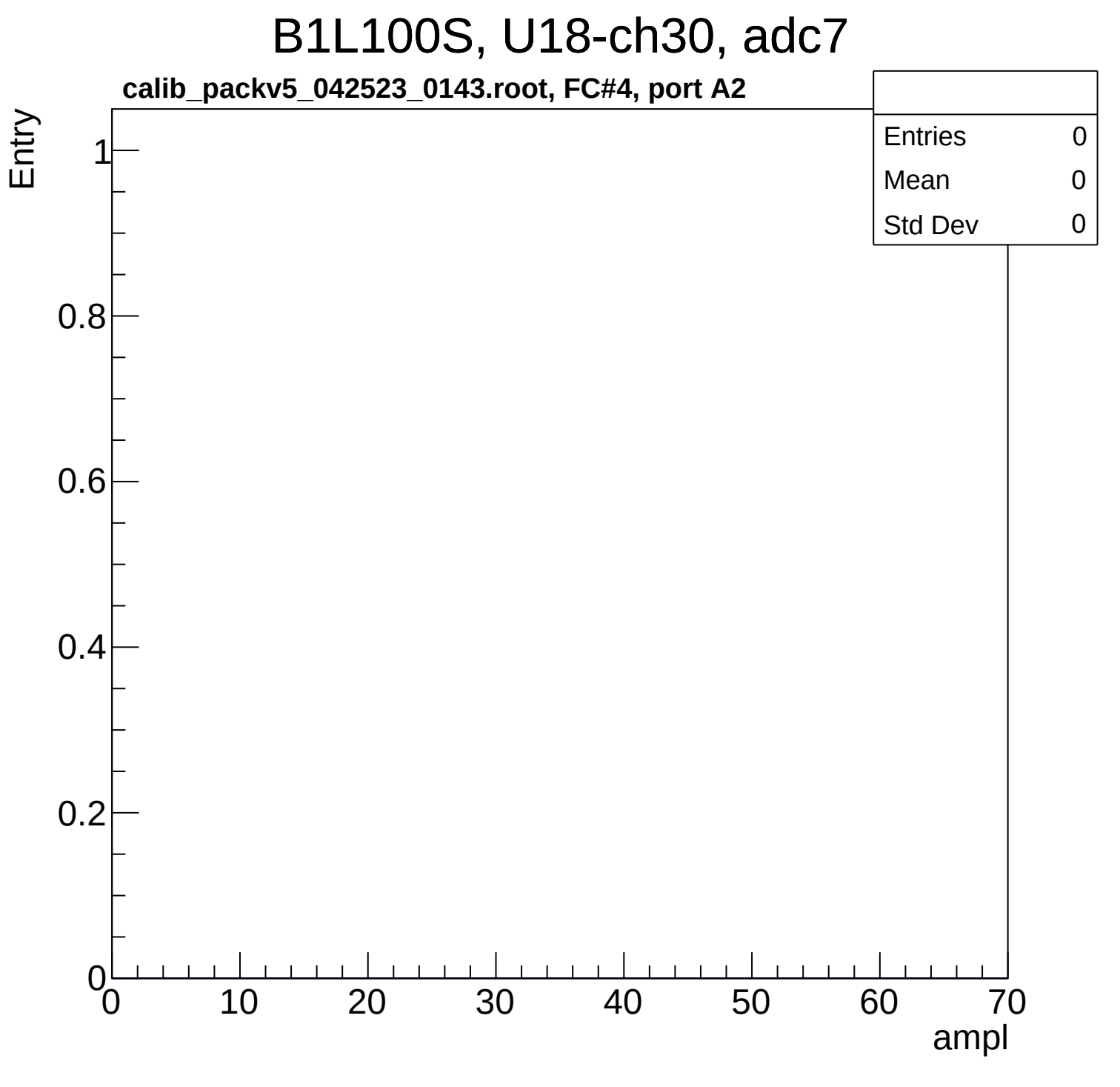

B1L100S, U18-ch30, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 43.06
Std Dev 3.431
Gaus mean : 43.1904
Gaus Width: 3.6840
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

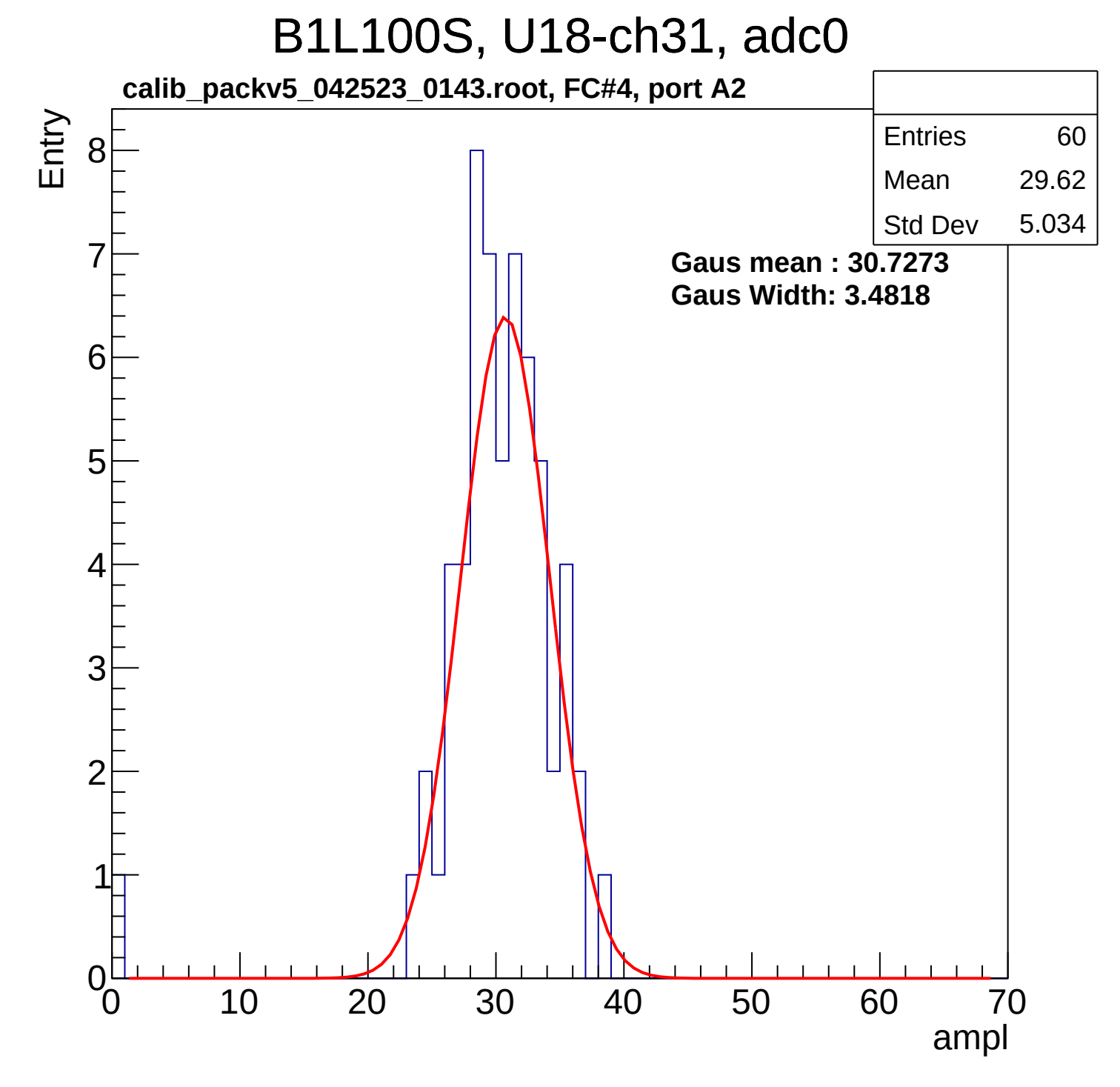

B1L100S, U18-ch30, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 49
Std Dev 3.412
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

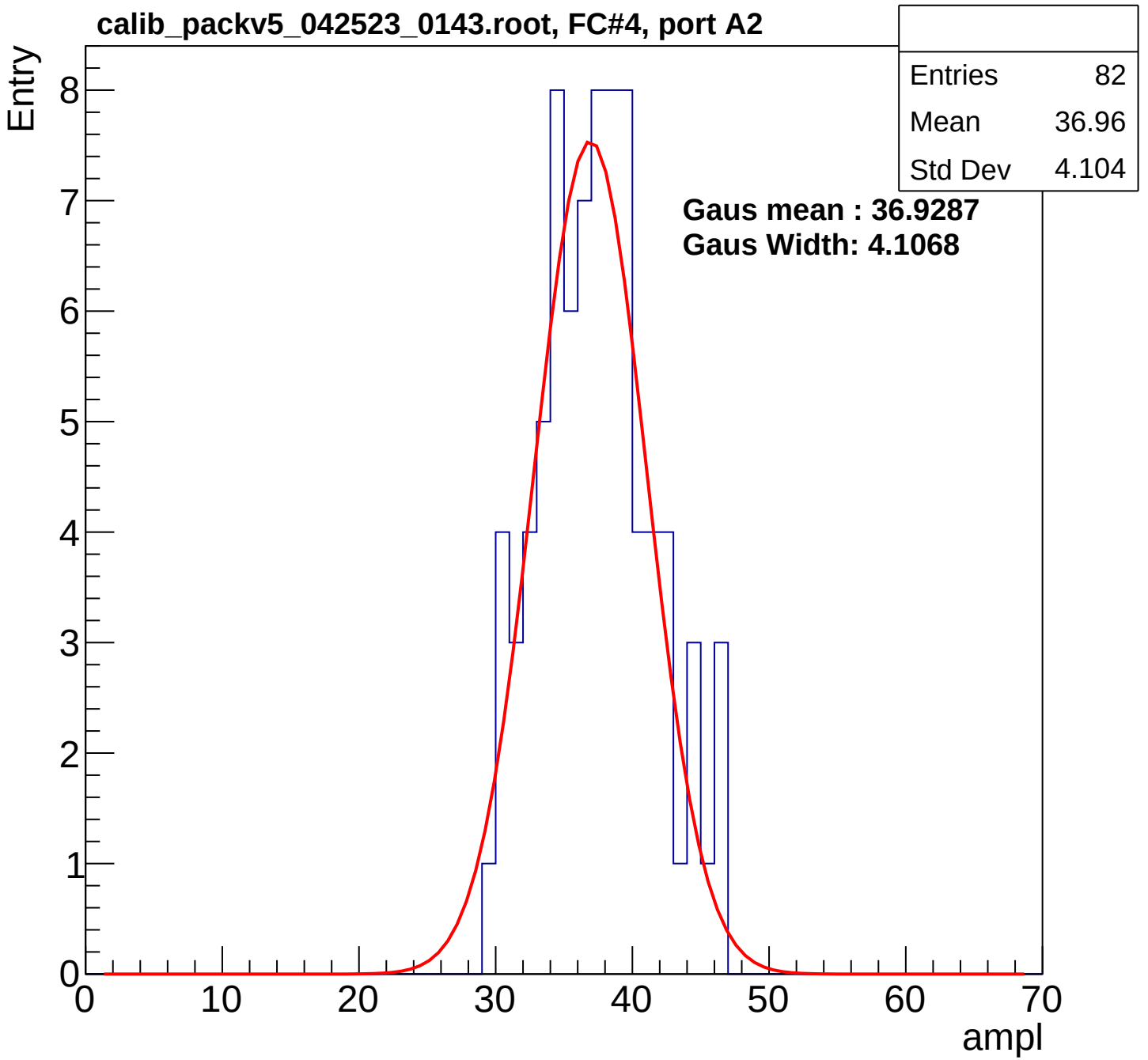

B1L100S, U18-ch30, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 55.34
Std Dev 3.526
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

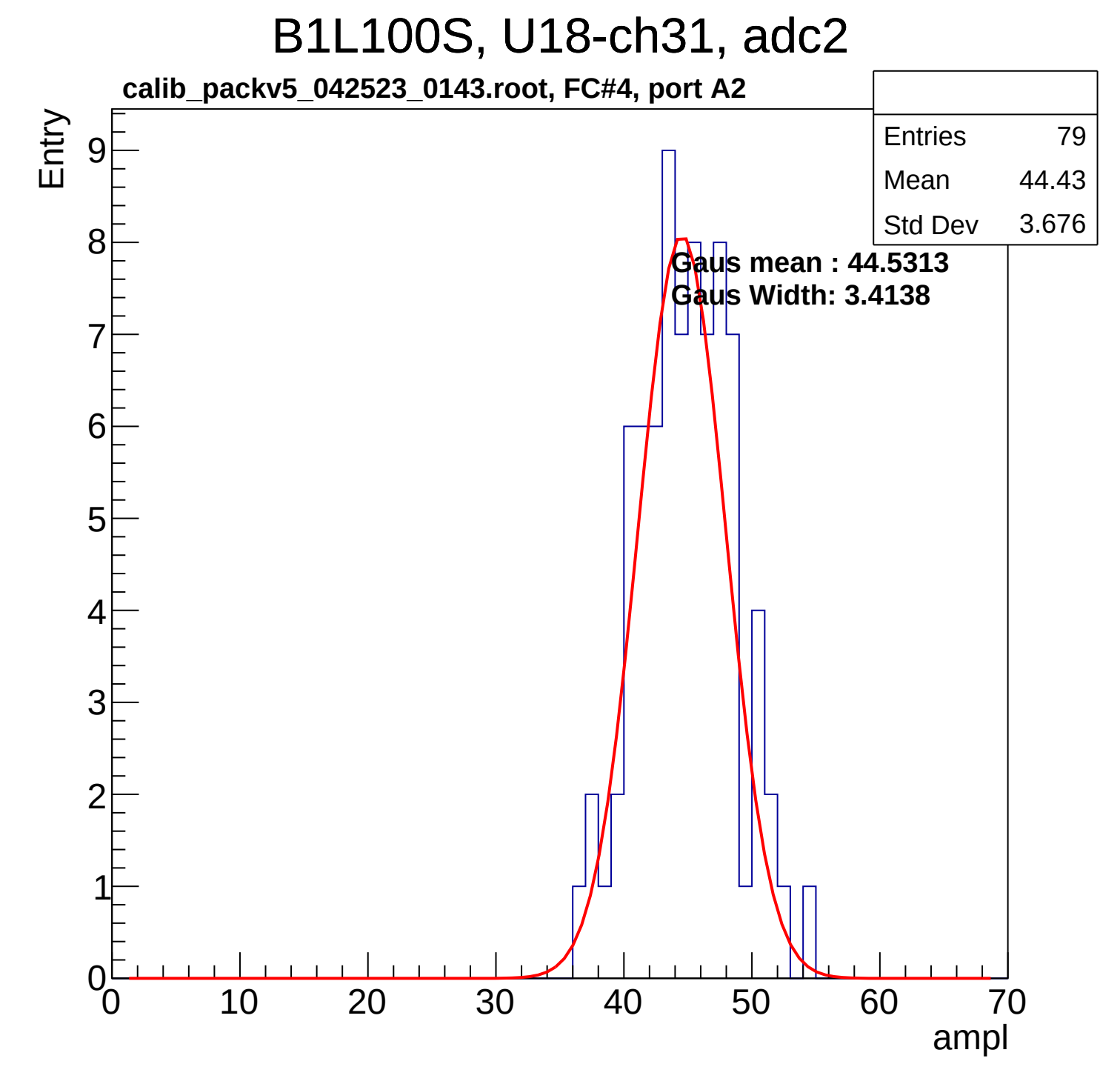

B1L100S, U18-ch30, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 58.81
Std Dev 9.307
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

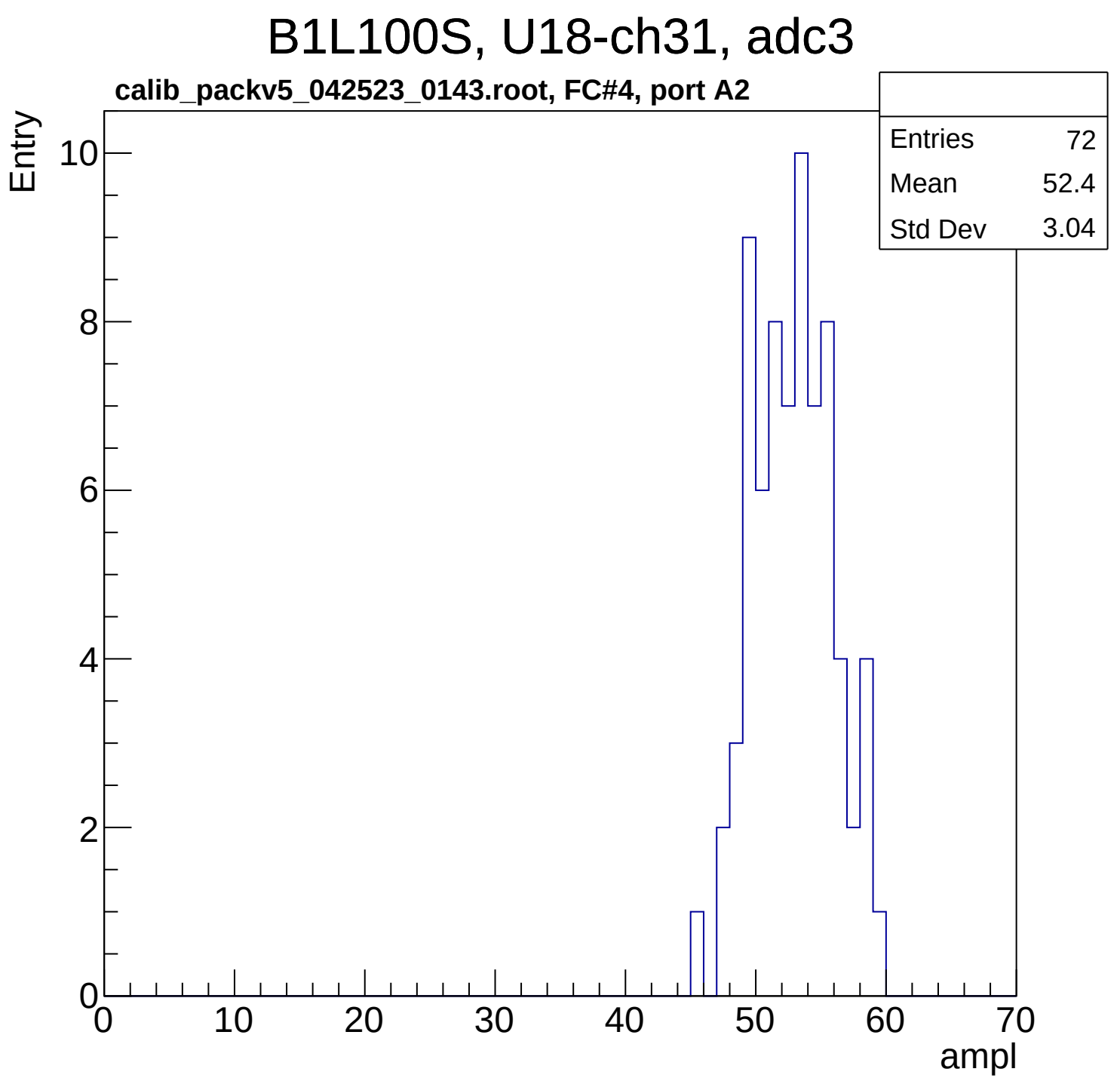

B1L100S, U18-ch30, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 5
Mean 61.6
Std Dev 0.4899
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

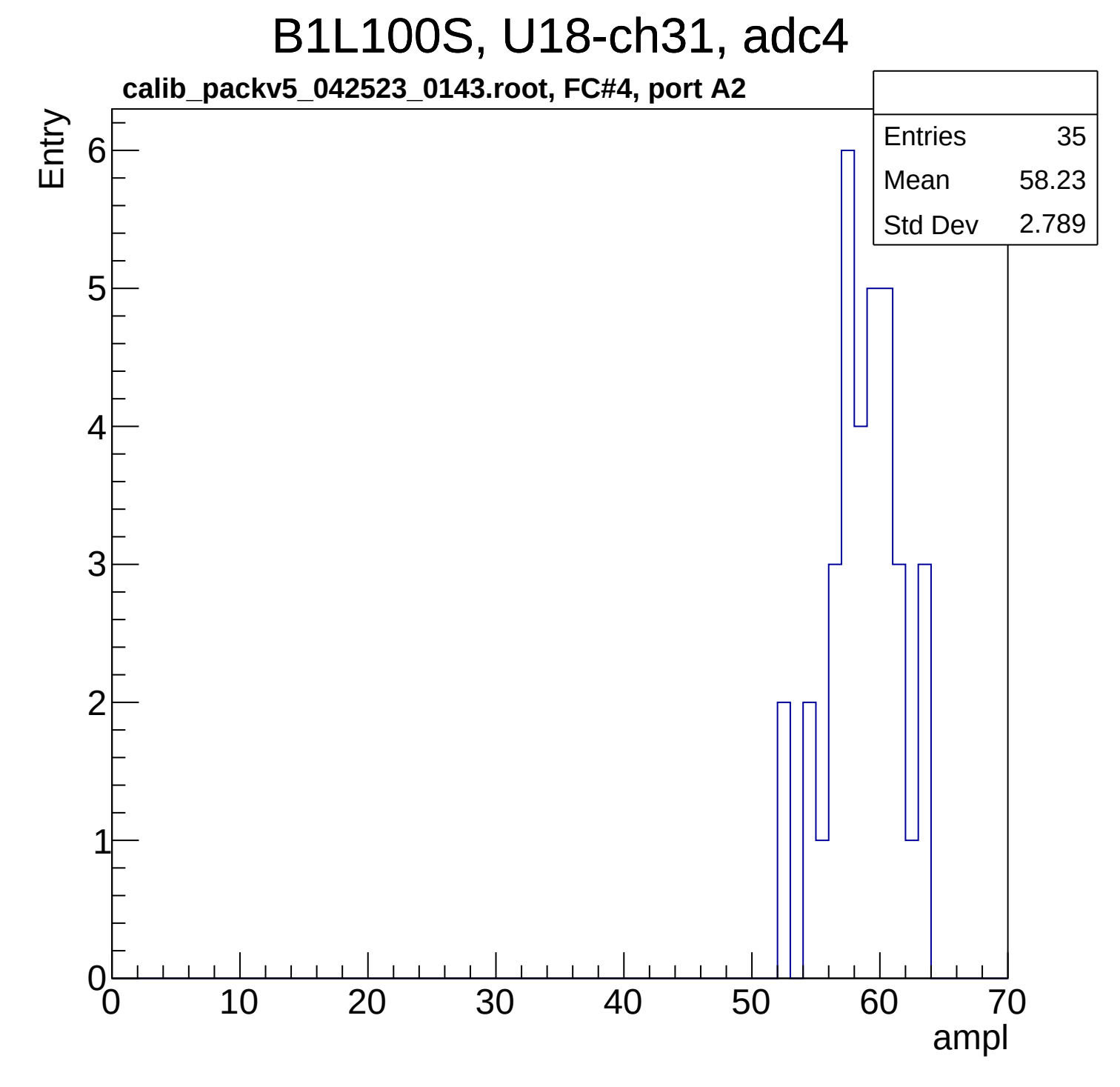

B1L100S, U18-ch30, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

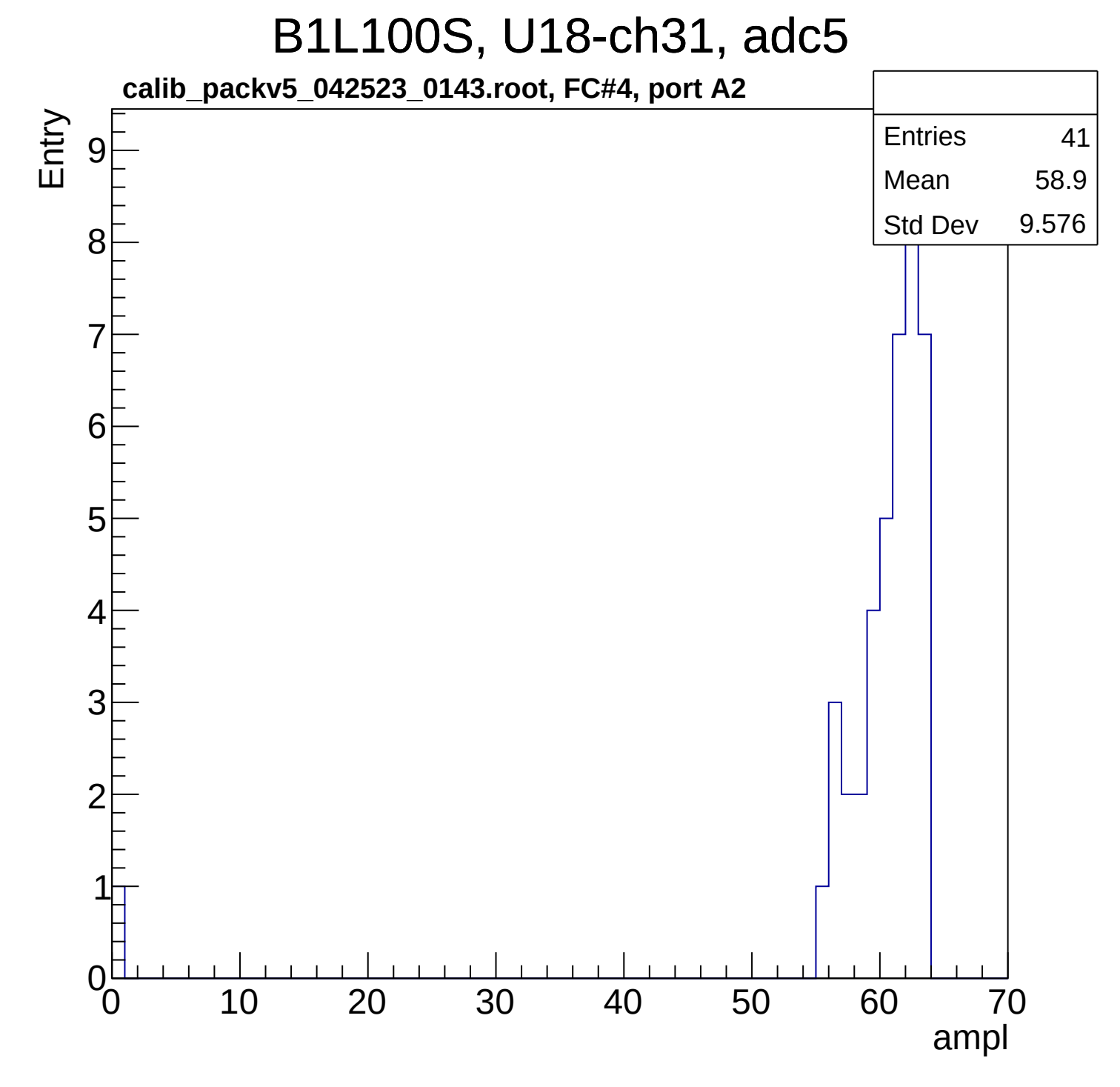

B1L100S, U18-ch31, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 29.62
Std Dev 5.034
Gaus mean : 30.7273
Gaus Width: 3.4818
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

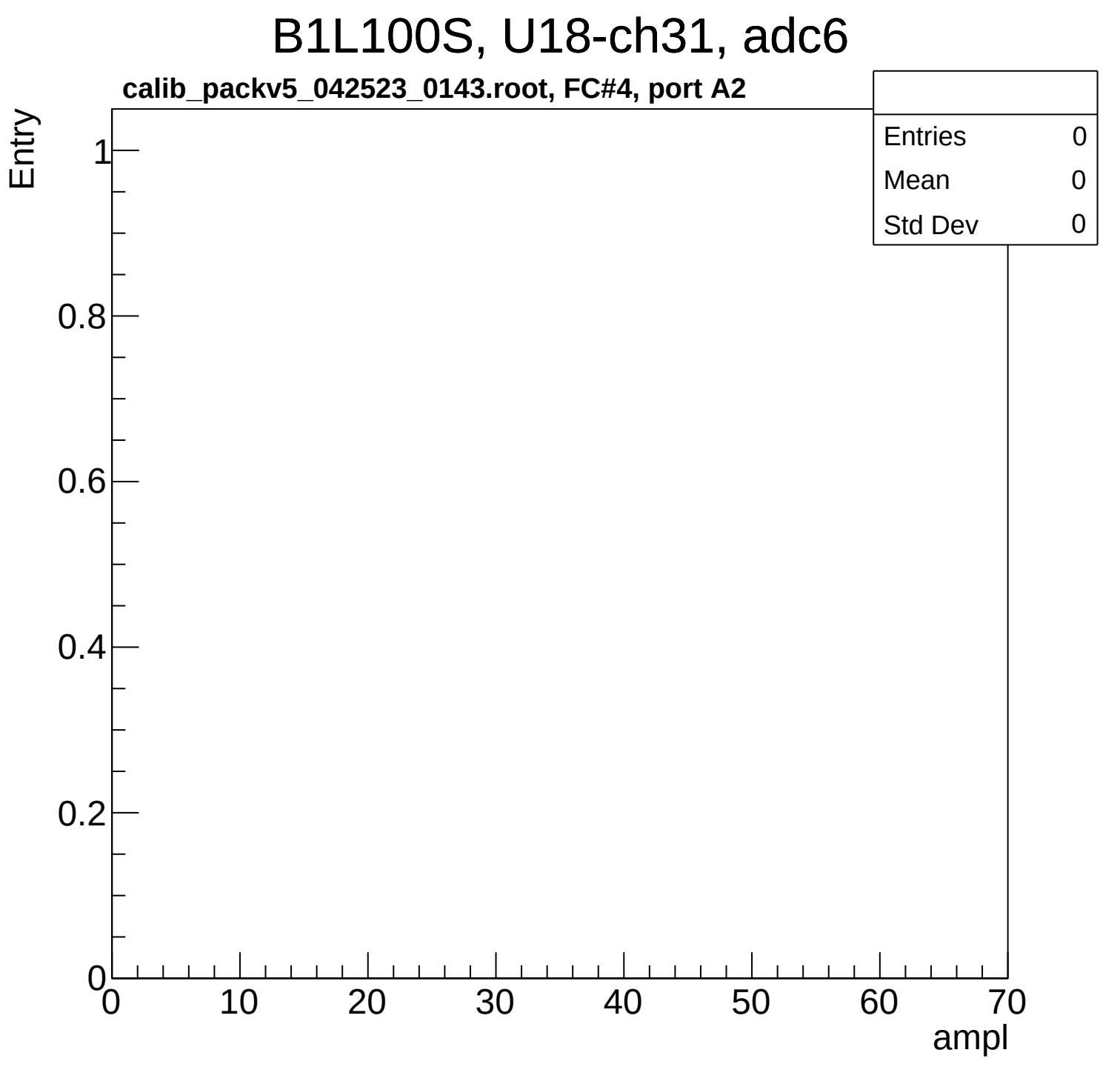

B1L100S, U18-ch31, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 36.96
Std Dev 4.104
Gaus mean : 36.9287
Gaus Width: 4.1068
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

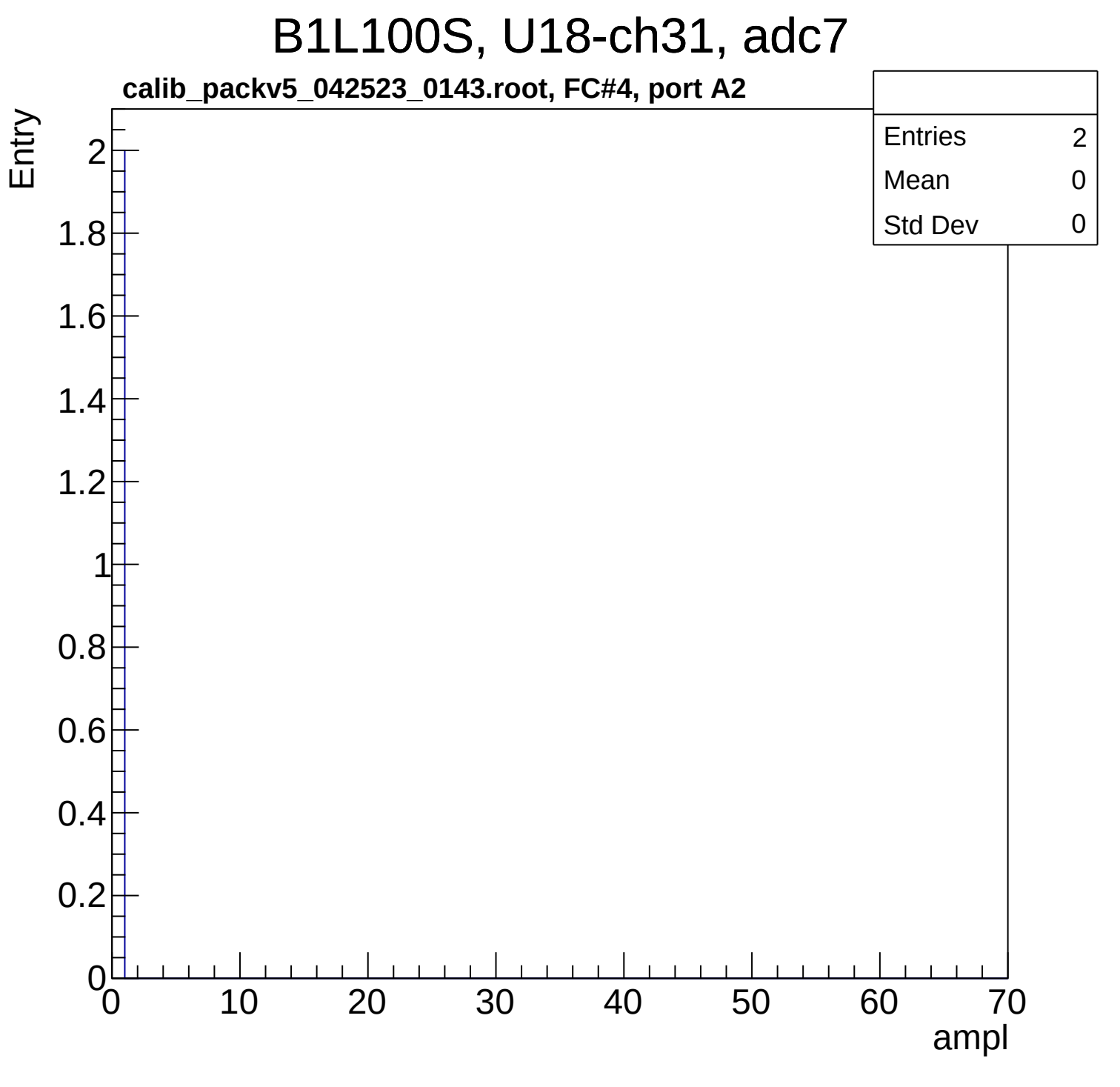

B1L100S, U18-ch31, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 44.43
Std Dev 3.676
Gaus mean : 44.5313
Gaus Width: 3.4138
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

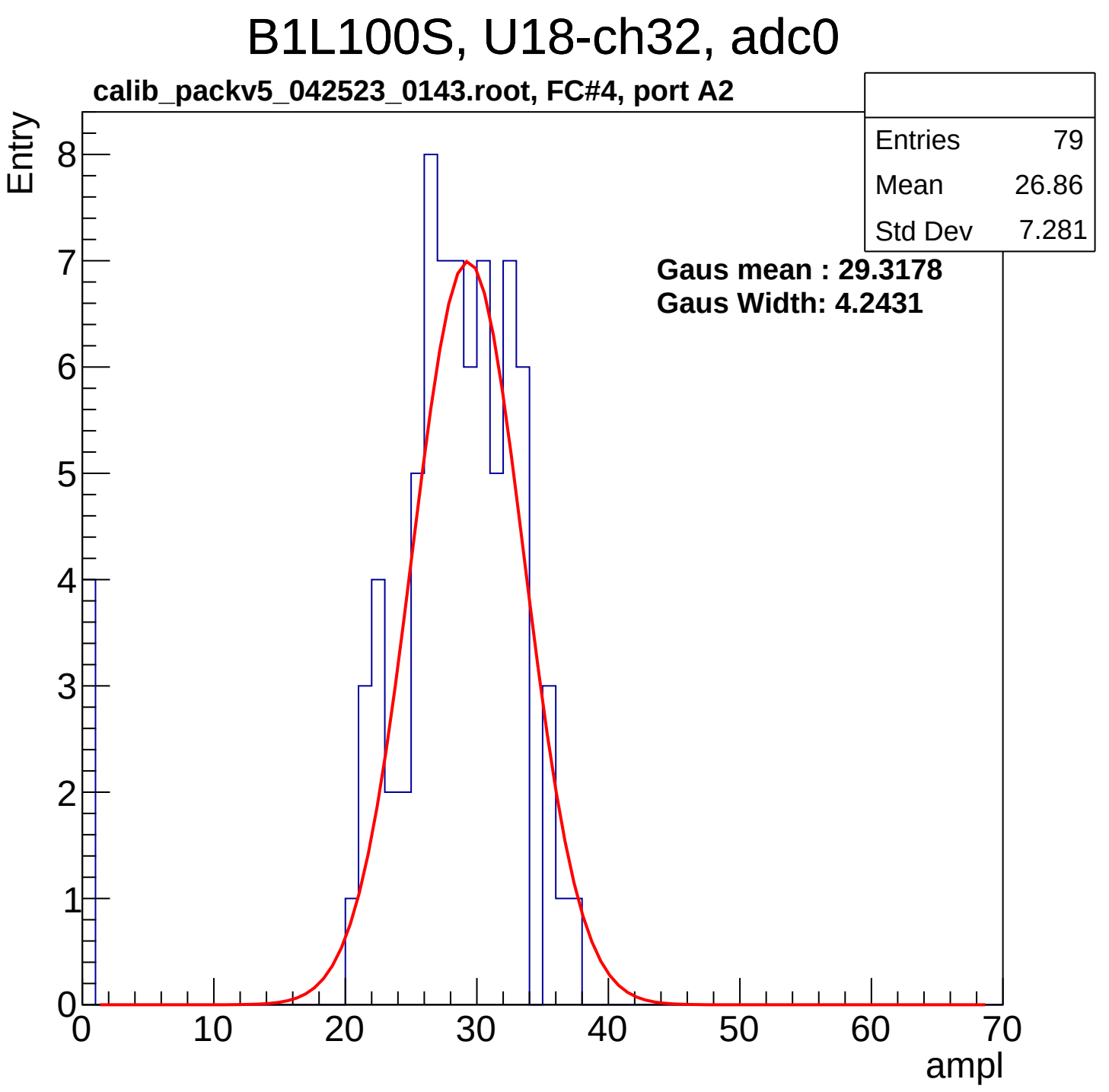

B1L100S, U18-ch31, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 52.4
Std Dev 3.04
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

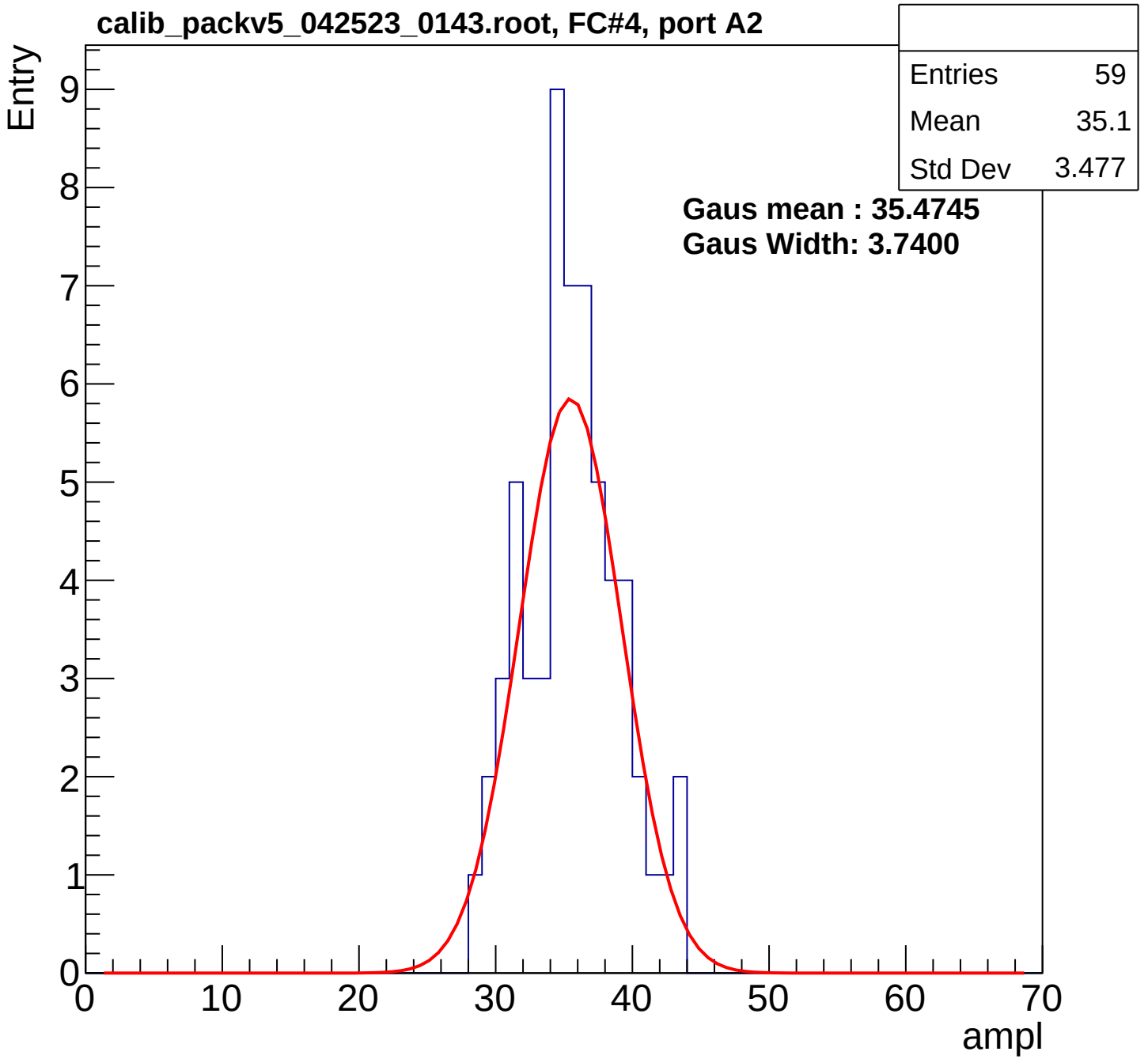

B1L100S, U18-ch31, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 35
Mean 58.23
Std Dev 2.789
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

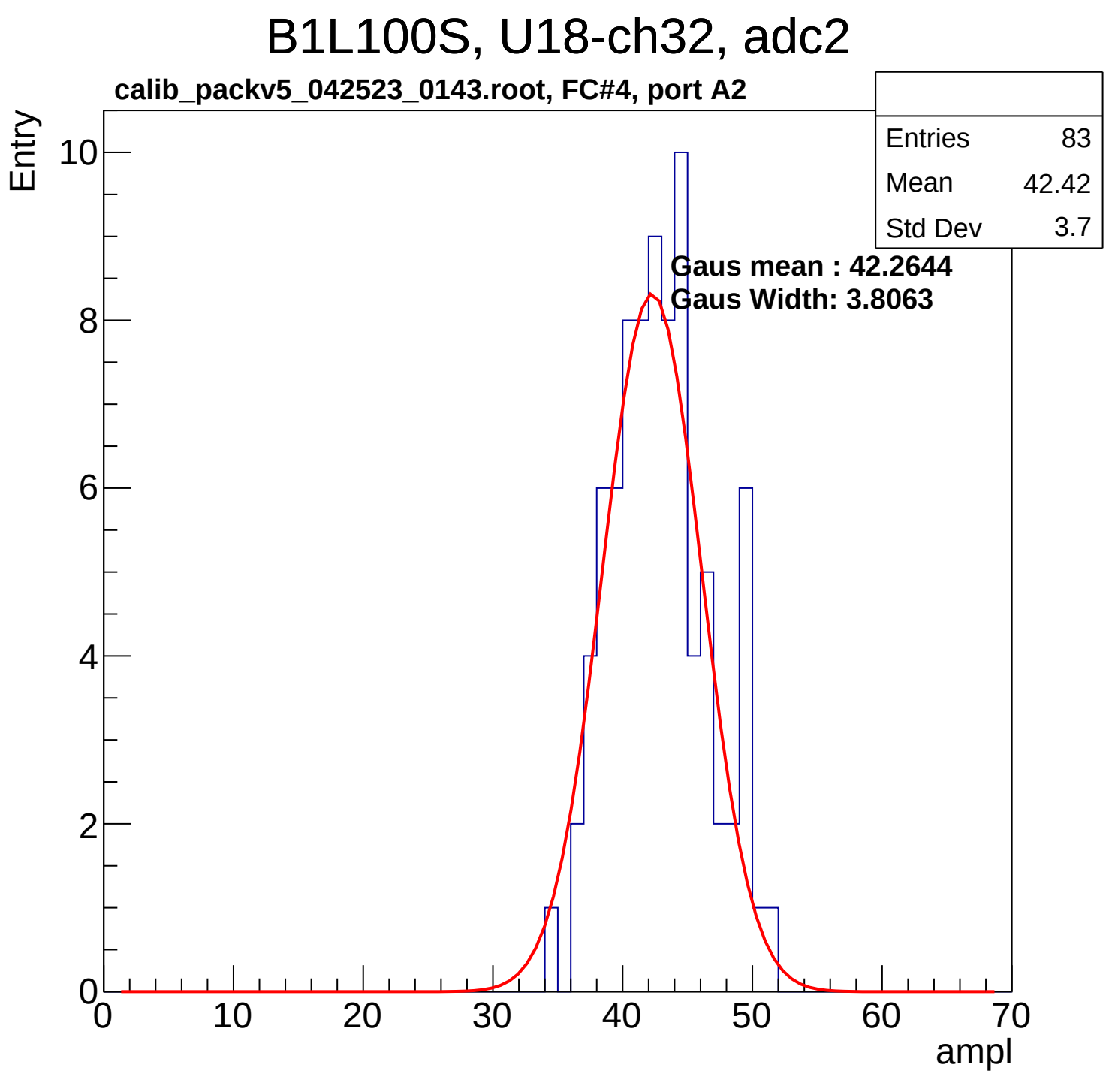

B1L100S, U18-ch31, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 41
Mean 58.9
Std Dev 9.576
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

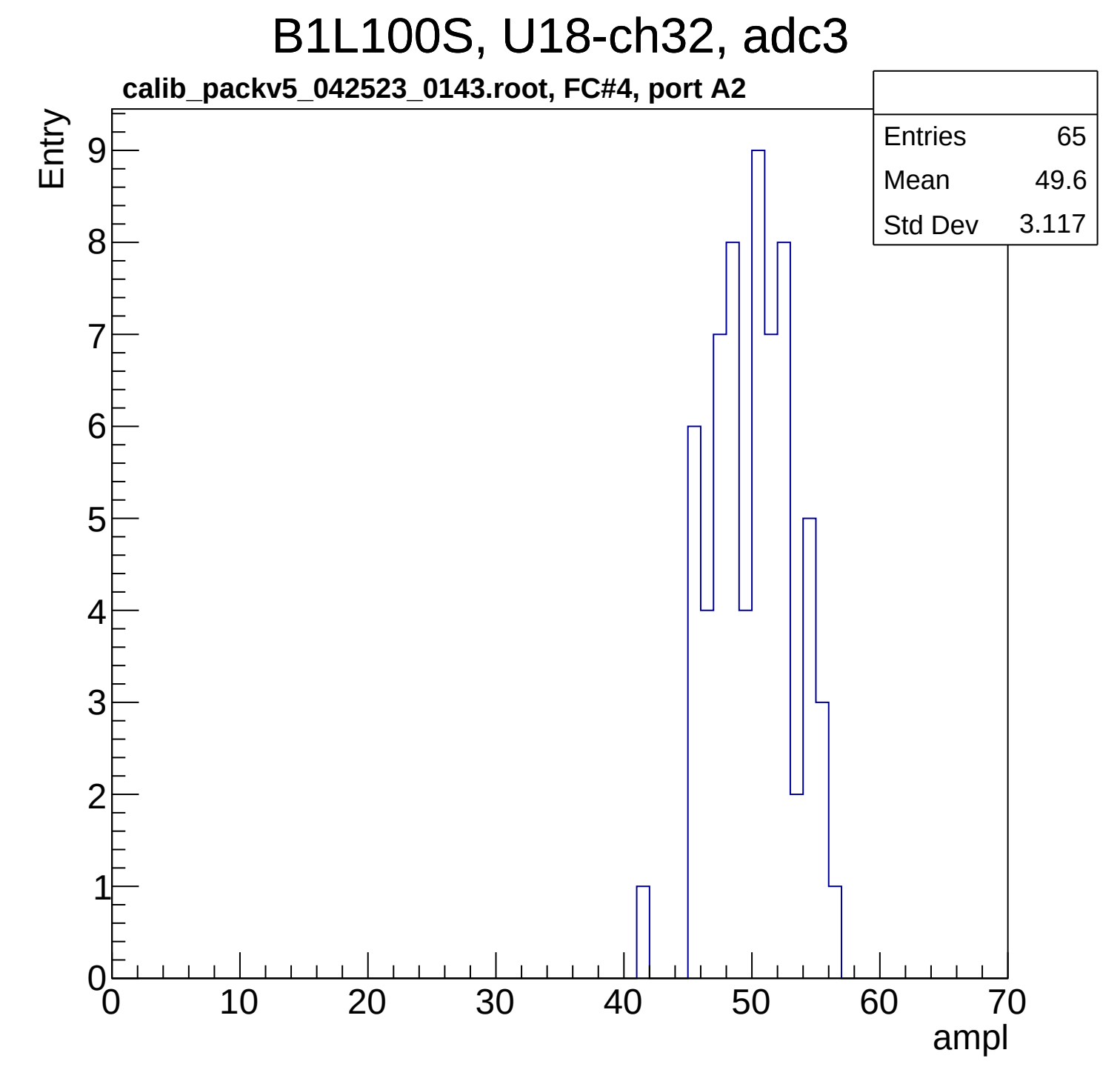

B1L100S, U18-ch31, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

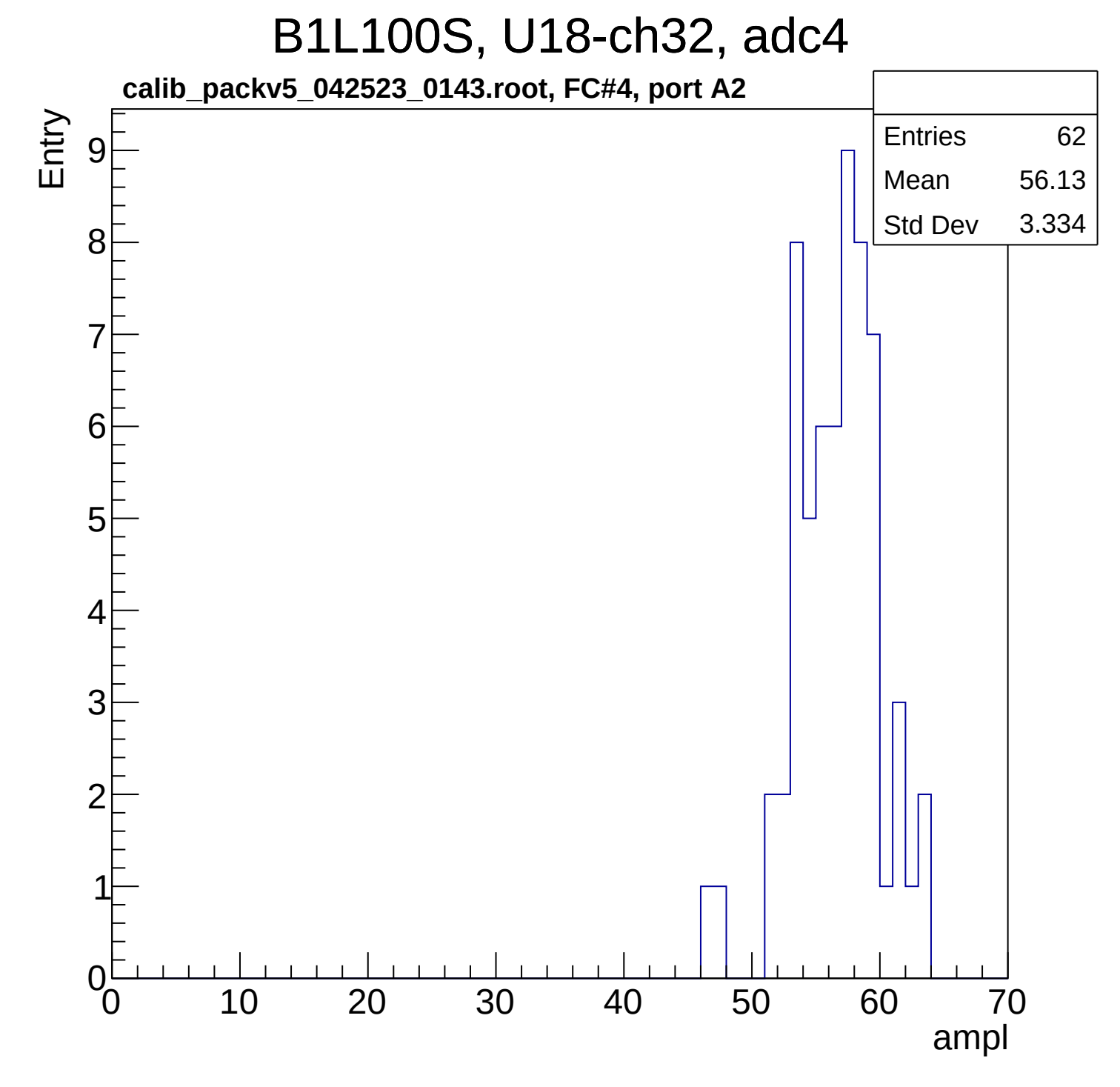

B1L100S, U18-ch31, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

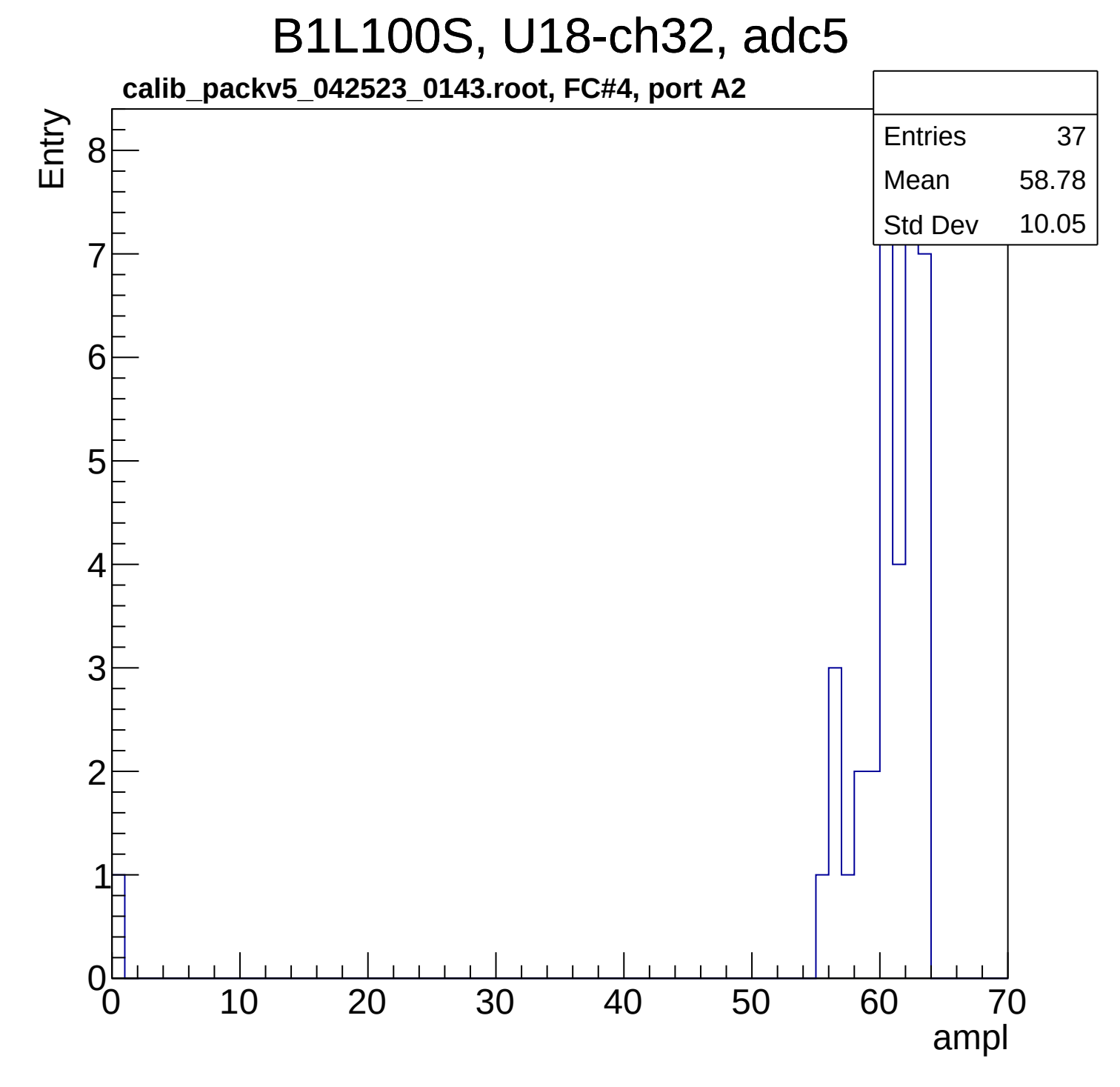

B1L100S, U18-ch32, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 26.86
Std Dev 7.281
Gaus mean : 29.3178
Gaus Width: 4.2431
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

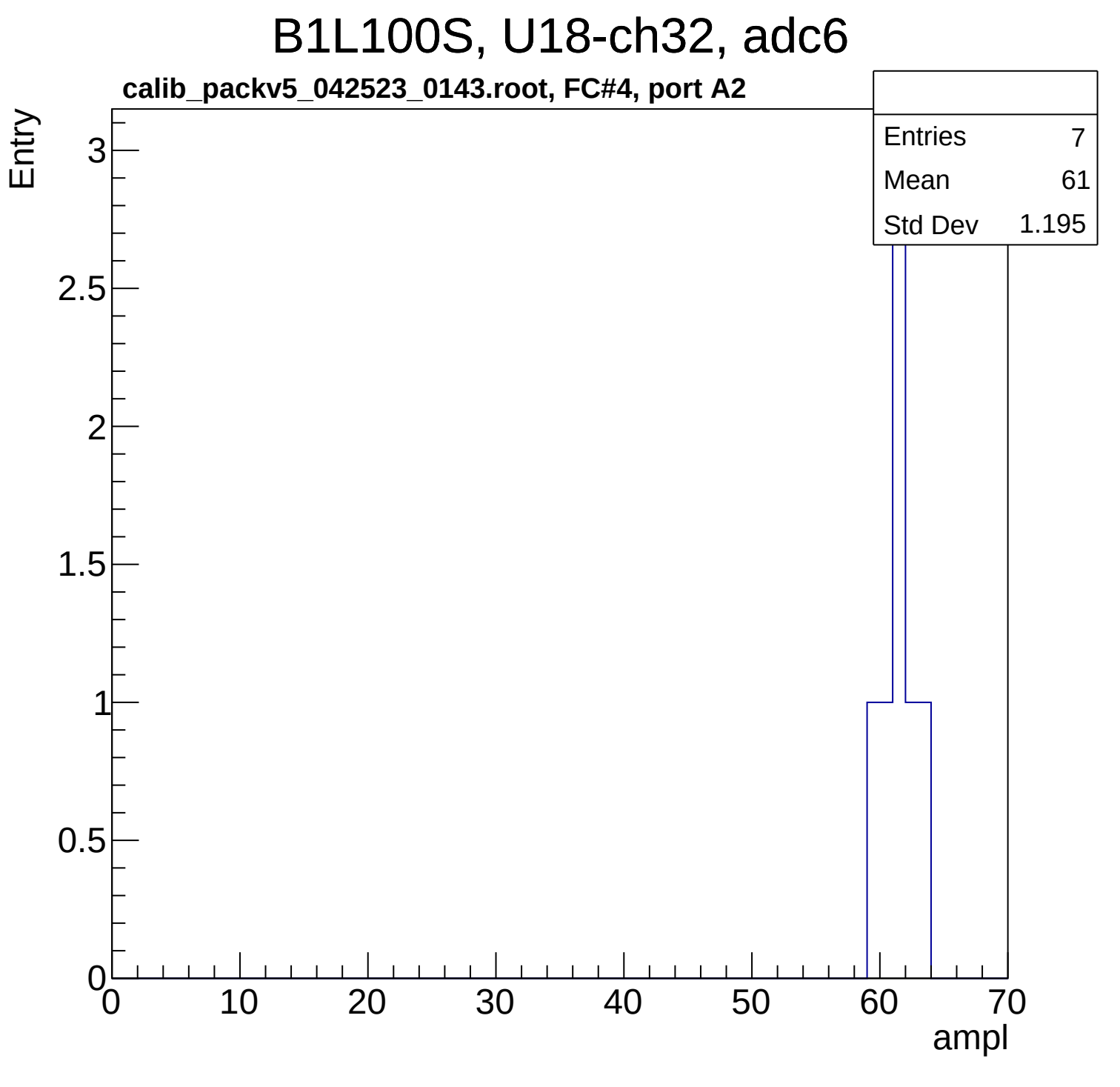

B1L100S, U18-ch32, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 35.1
Std Dev 3.477
Gaus mean : 35.4745
Gaus Width: 3.7400
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

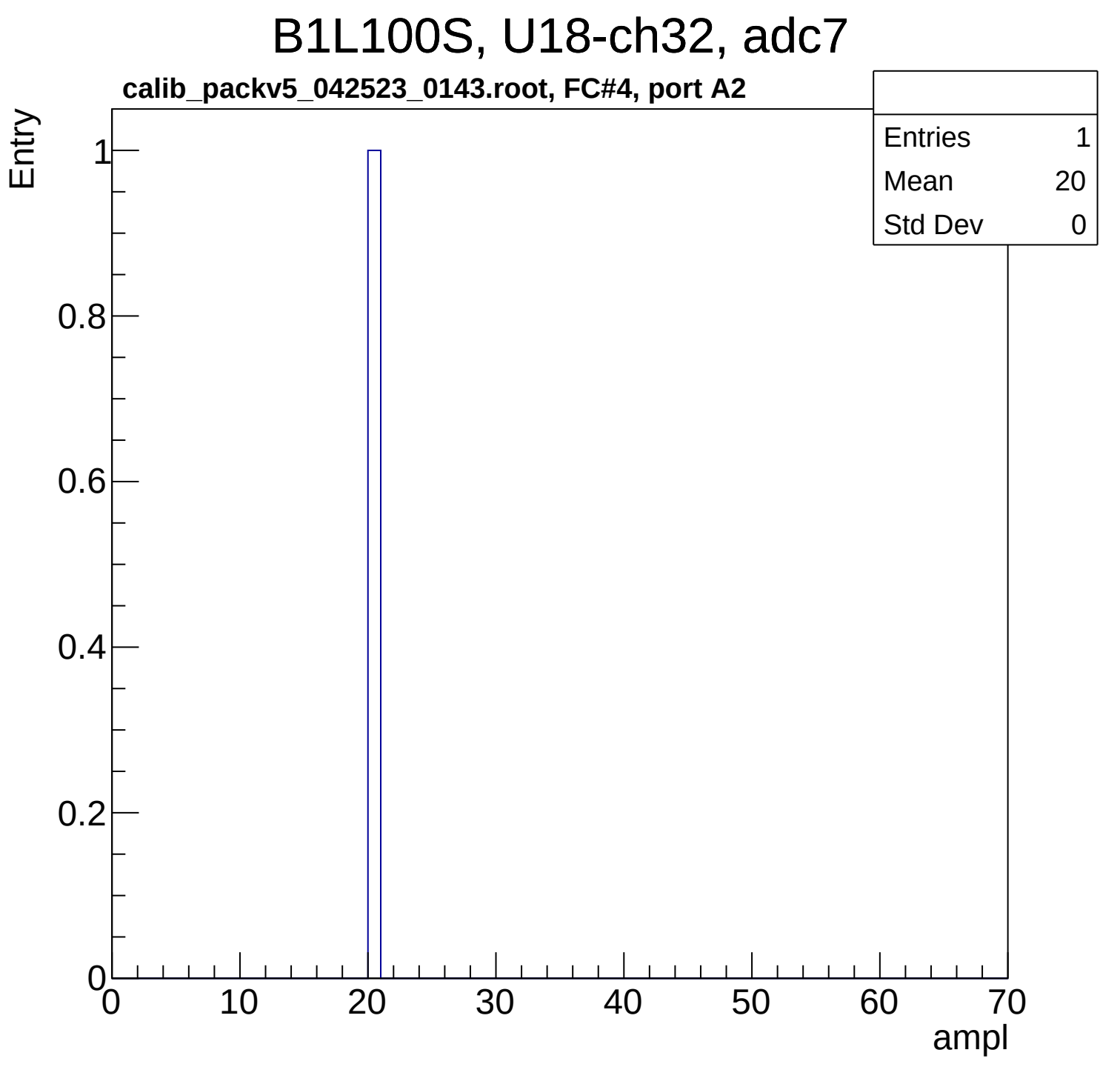

B1L100S, U18-ch32, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 83
Mean 42.42
Std Dev 3.7
Gaus mean : 42.2644
Gaus Width: 3.8063
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

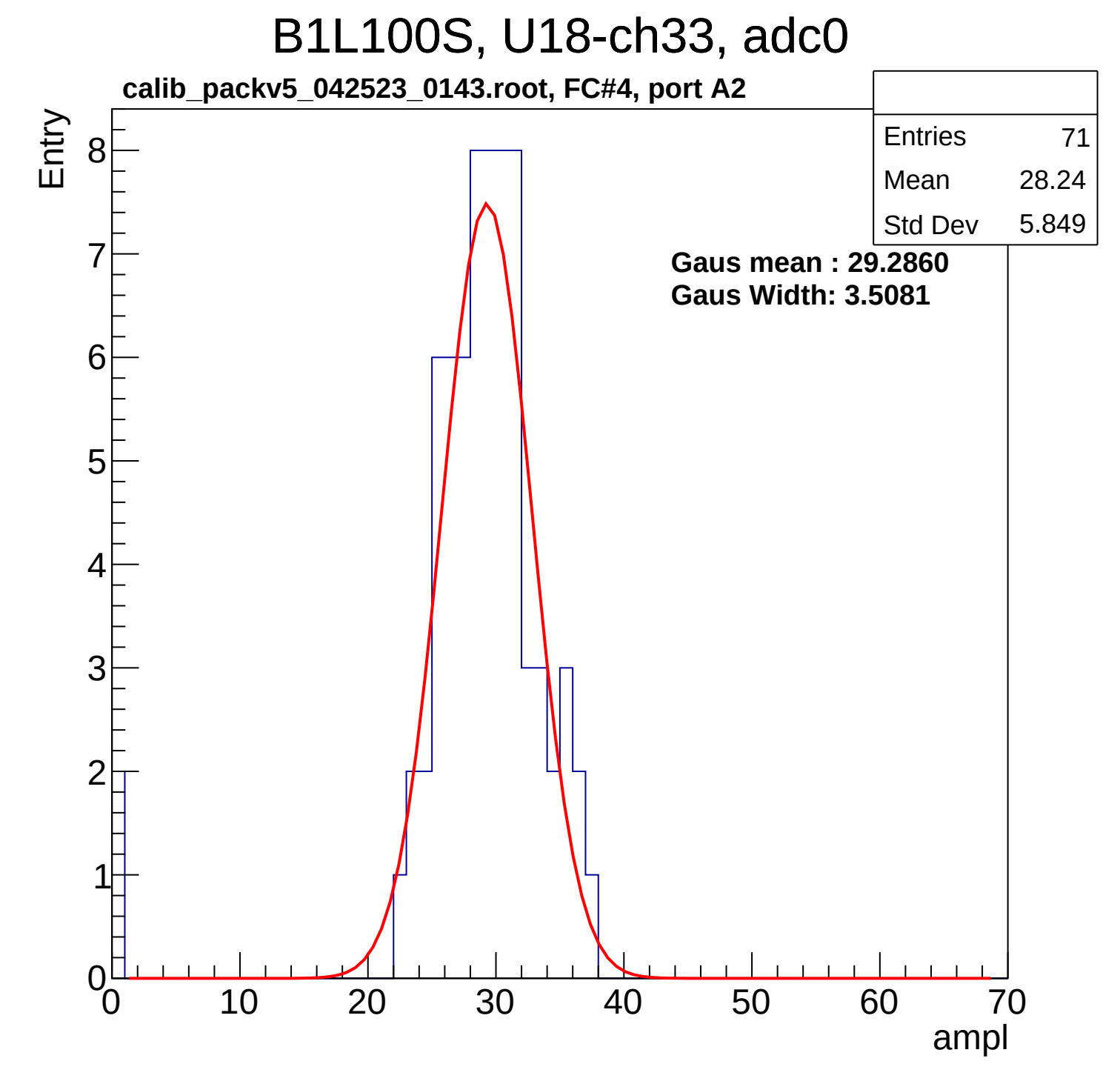

B1L100S, U18-ch32, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 49.6
Std Dev 3.117
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

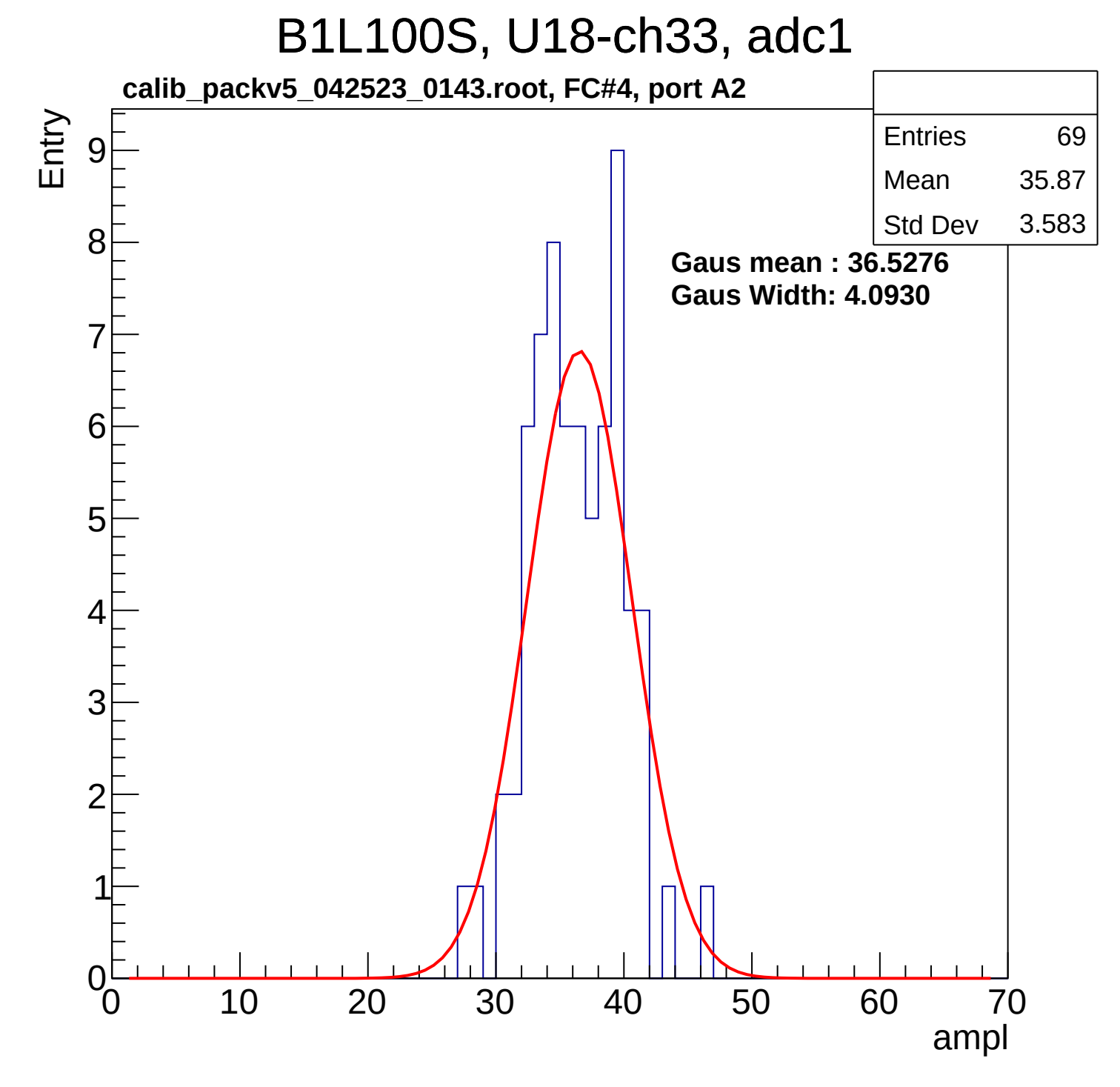

B1L100S, U18-ch32, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 56.13
Std Dev 3.334
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

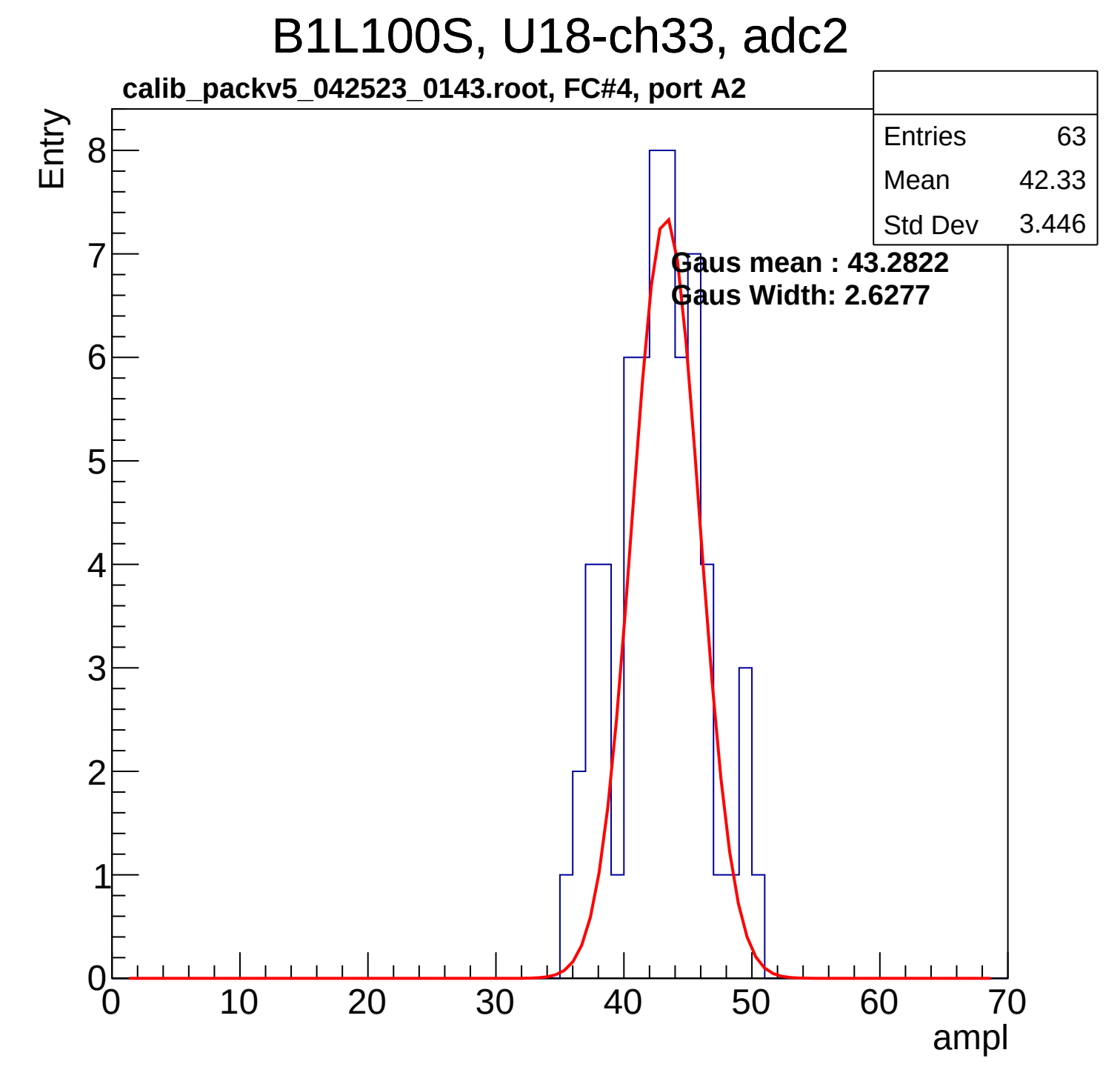

B1L100S, U18-ch32, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 37
Mean 58.78
Std Dev 10.05
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

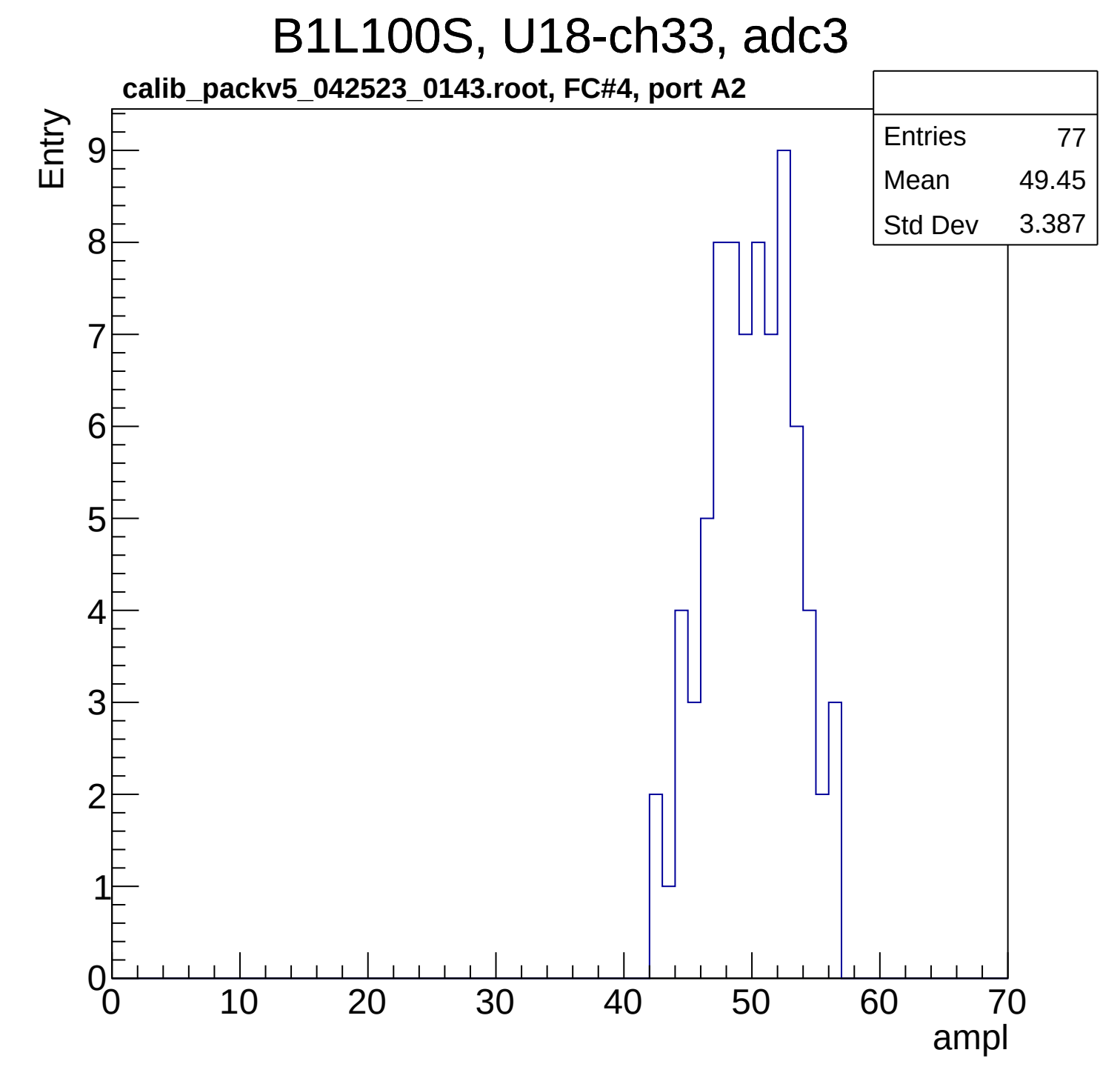

B1L100S, U18-ch32, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 61
Std Dev 1.195
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

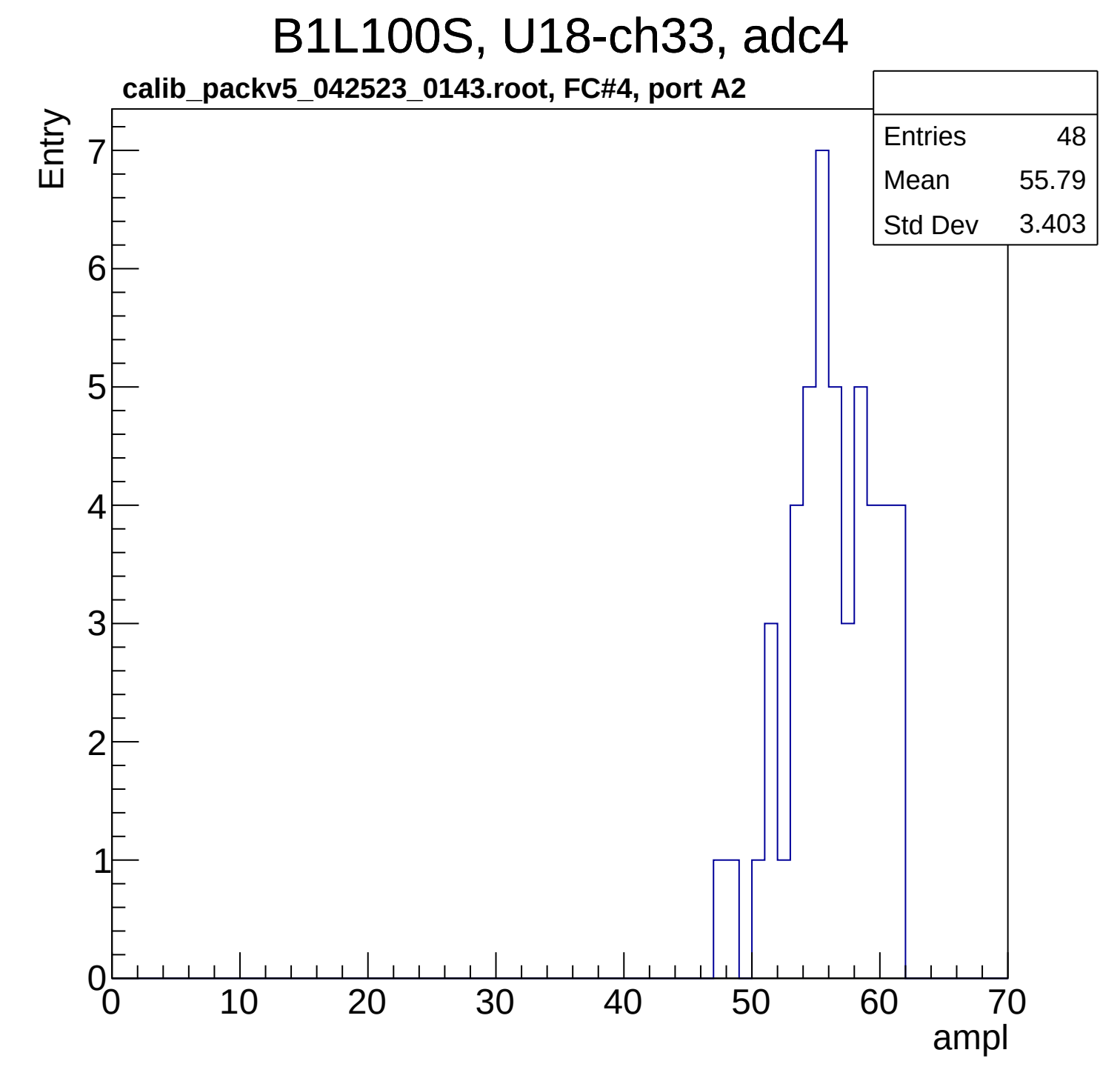

B1L100S, U18-ch32, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 20
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

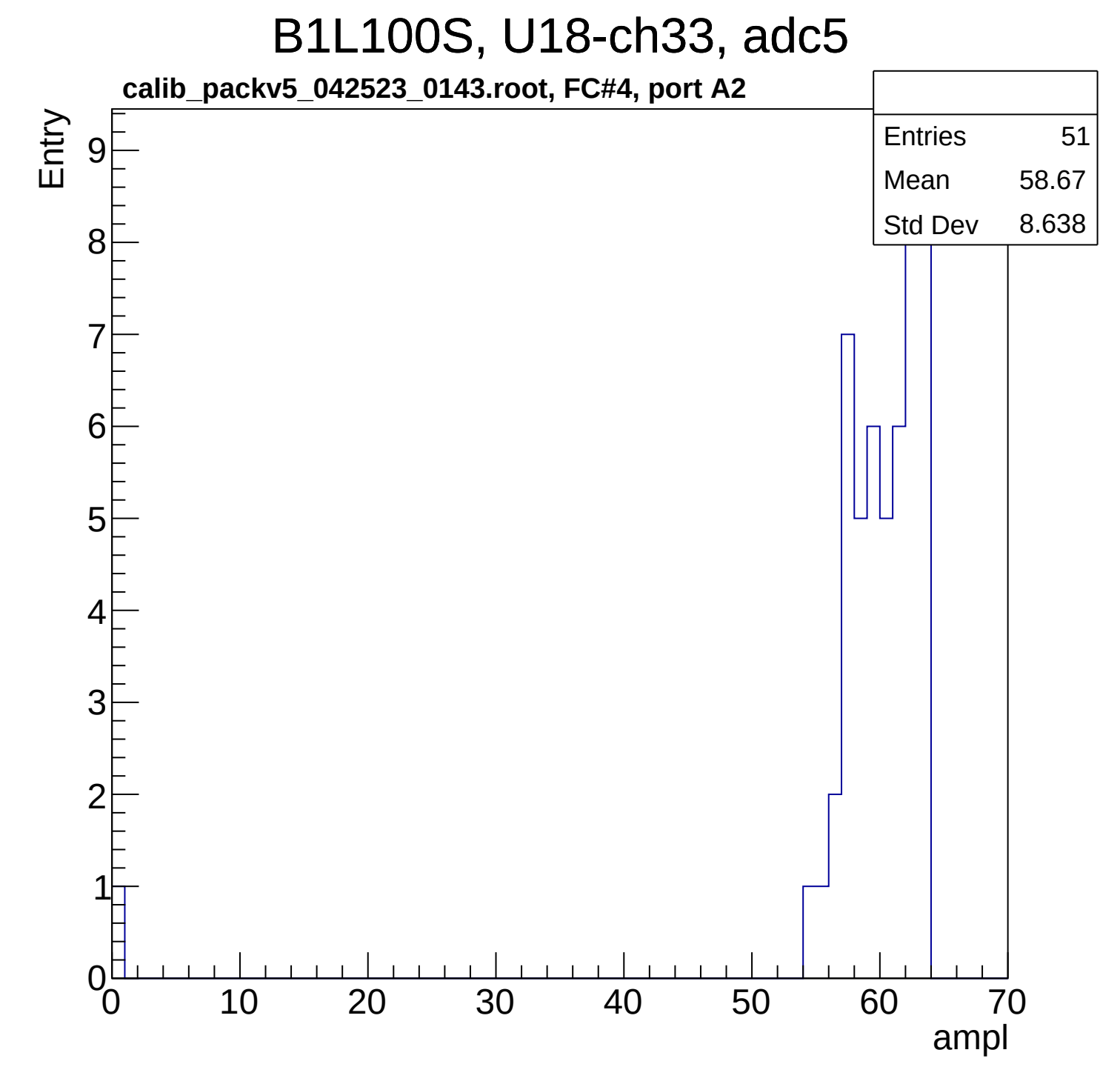

B1L100S, U18-ch33, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 28.24
Std Dev 5.849
Gaus mean : 29.2860
Gaus Width: 3.5081
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

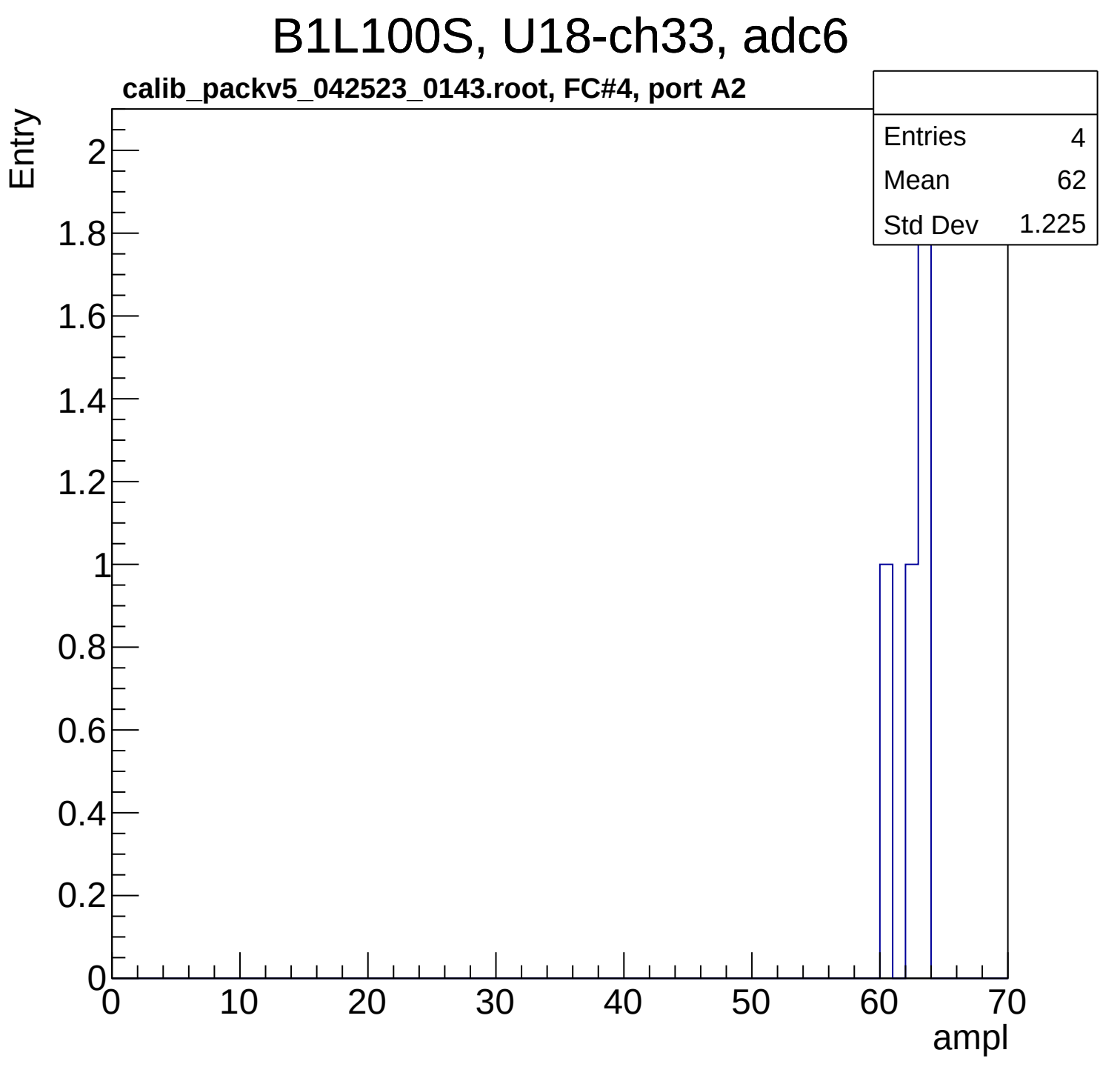

B1L100S, U18-ch33, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 35.87
Std Dev 3.583
Gaus mean : 36.5276
Gaus Width: 4.0930
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

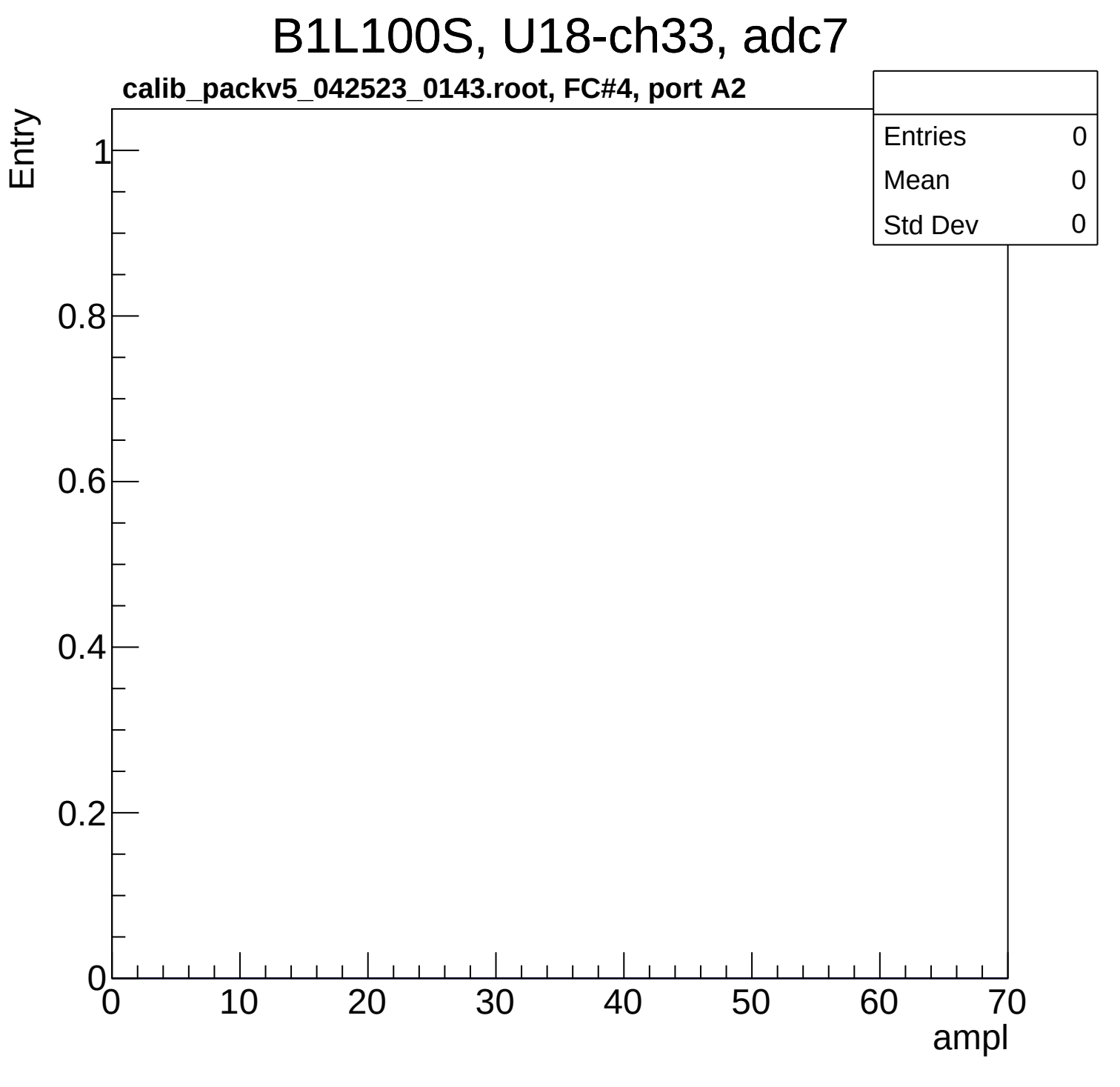

B1L100S, U18-ch33, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 42.33
Std Dev 3.446
Gaus mean : 43.2822
Gaus Width: 2.6277
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

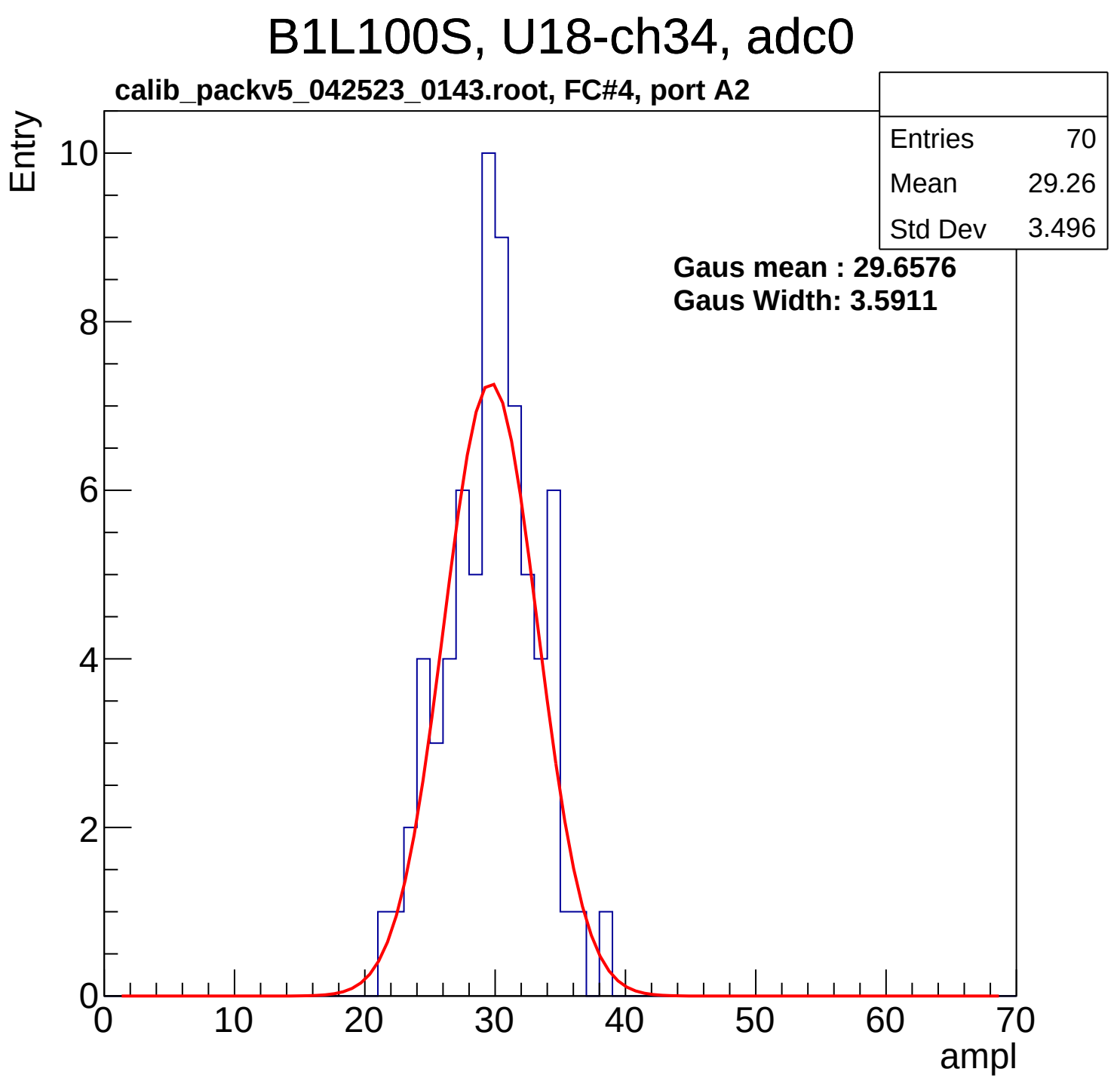

B1L100S, U18-ch33, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 49.45
Std Dev 3.387
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

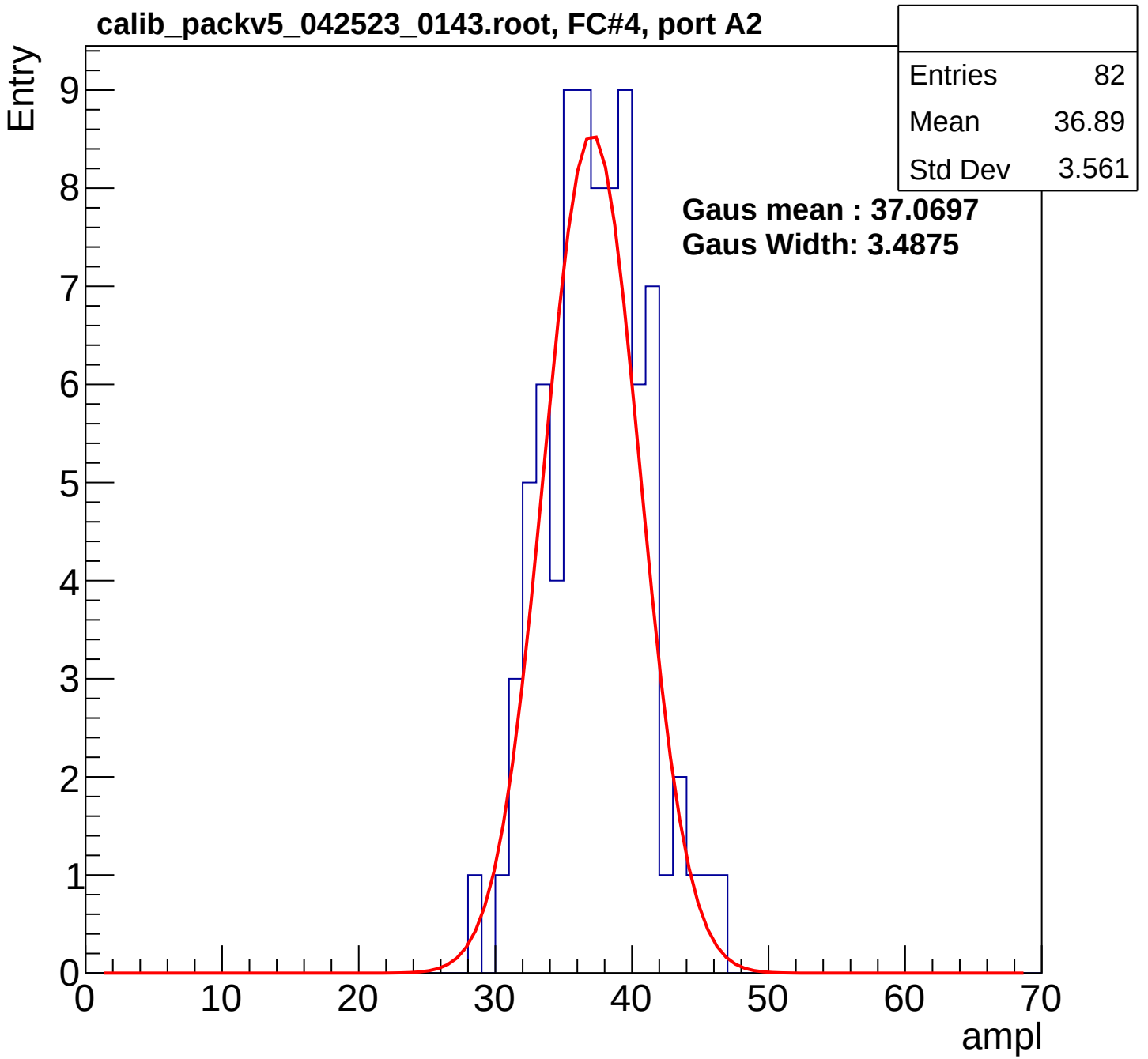

B1L100S, U18-ch33, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 55.79
Std Dev 3.403
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

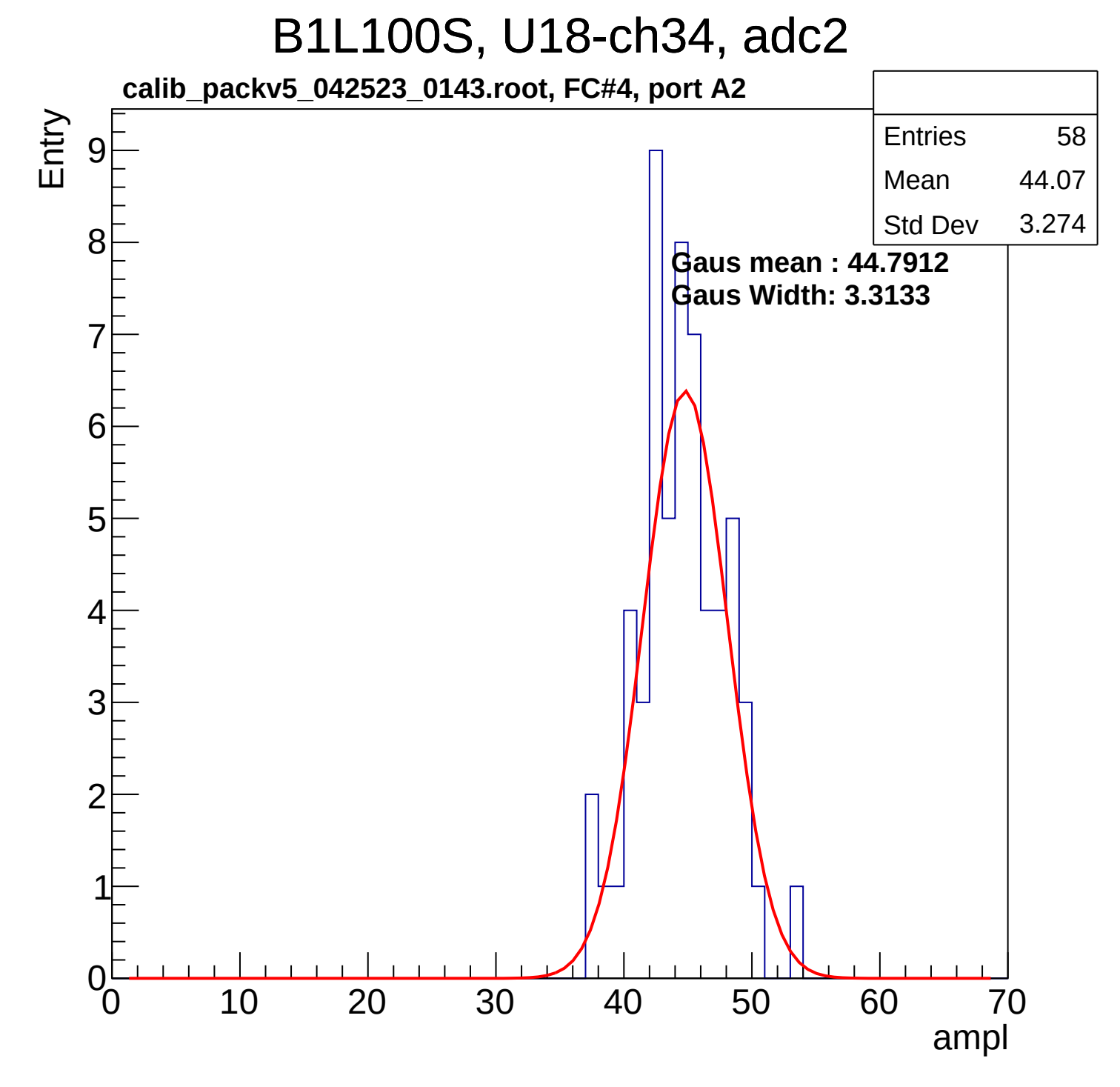

B1L100S, U18-ch33, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 58.67
Std Dev 8.638
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

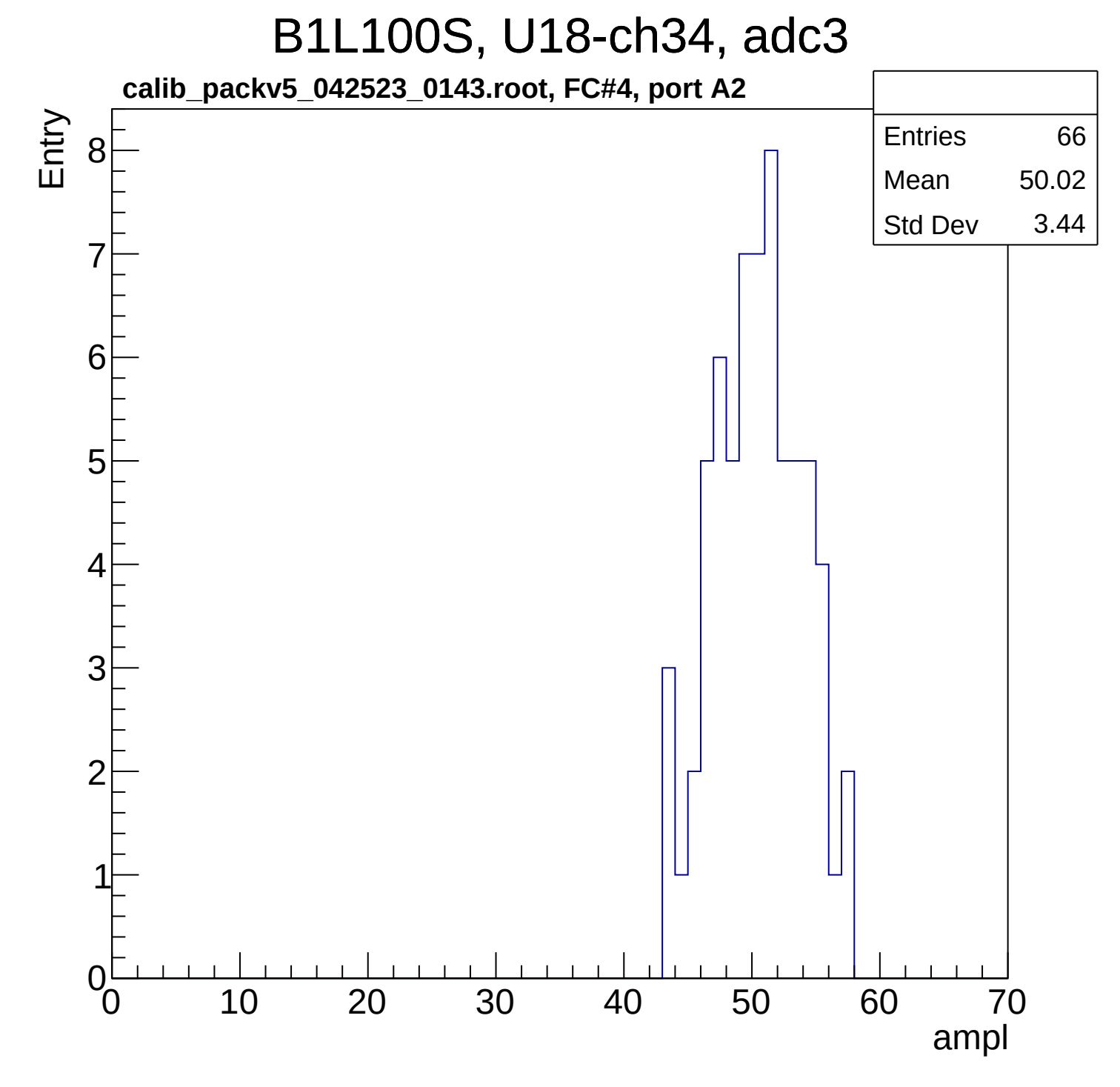

B1L100S, U18-ch33, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 62
Std Dev 1.225
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

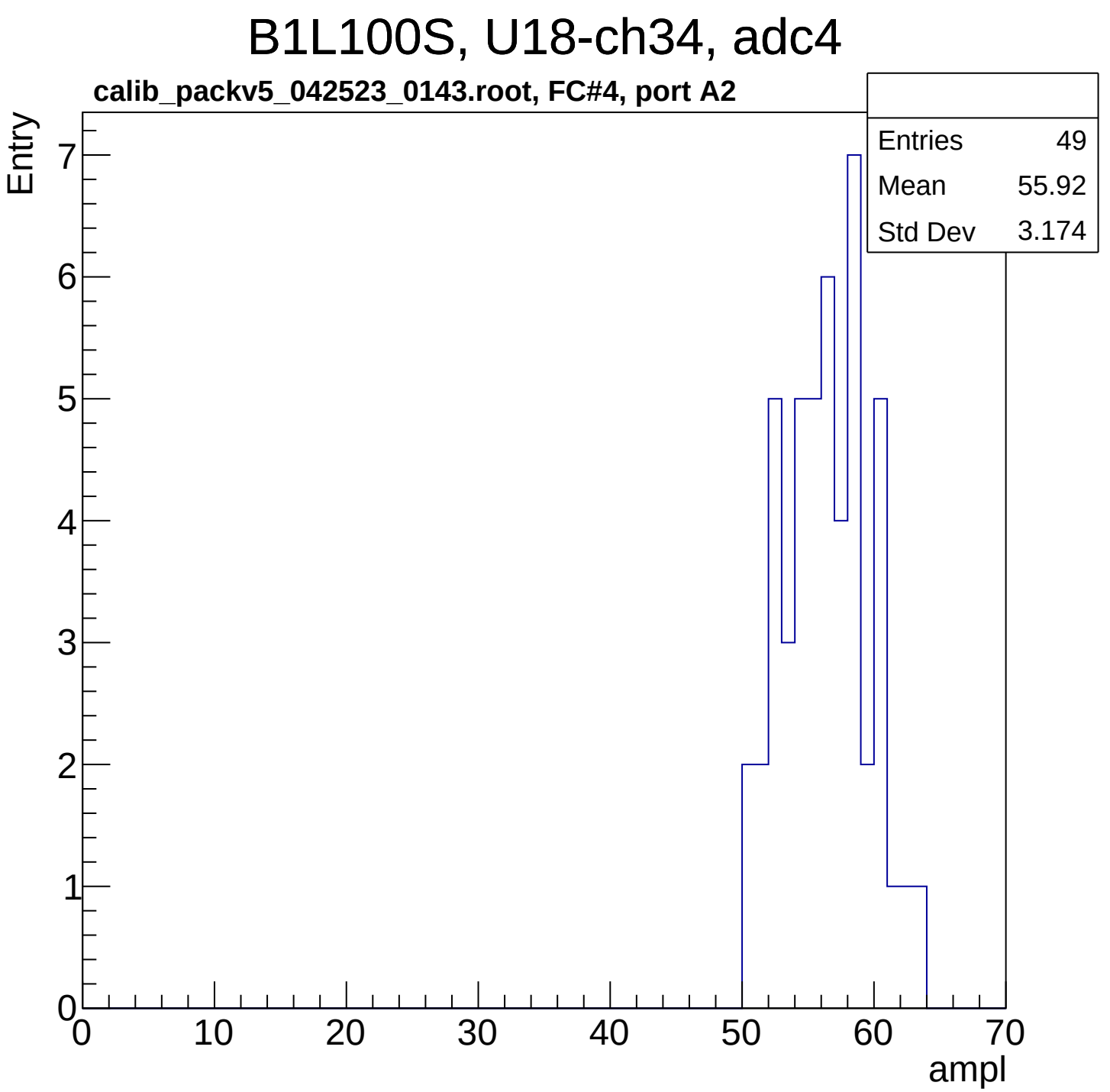

B1L100S, U18-ch33, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

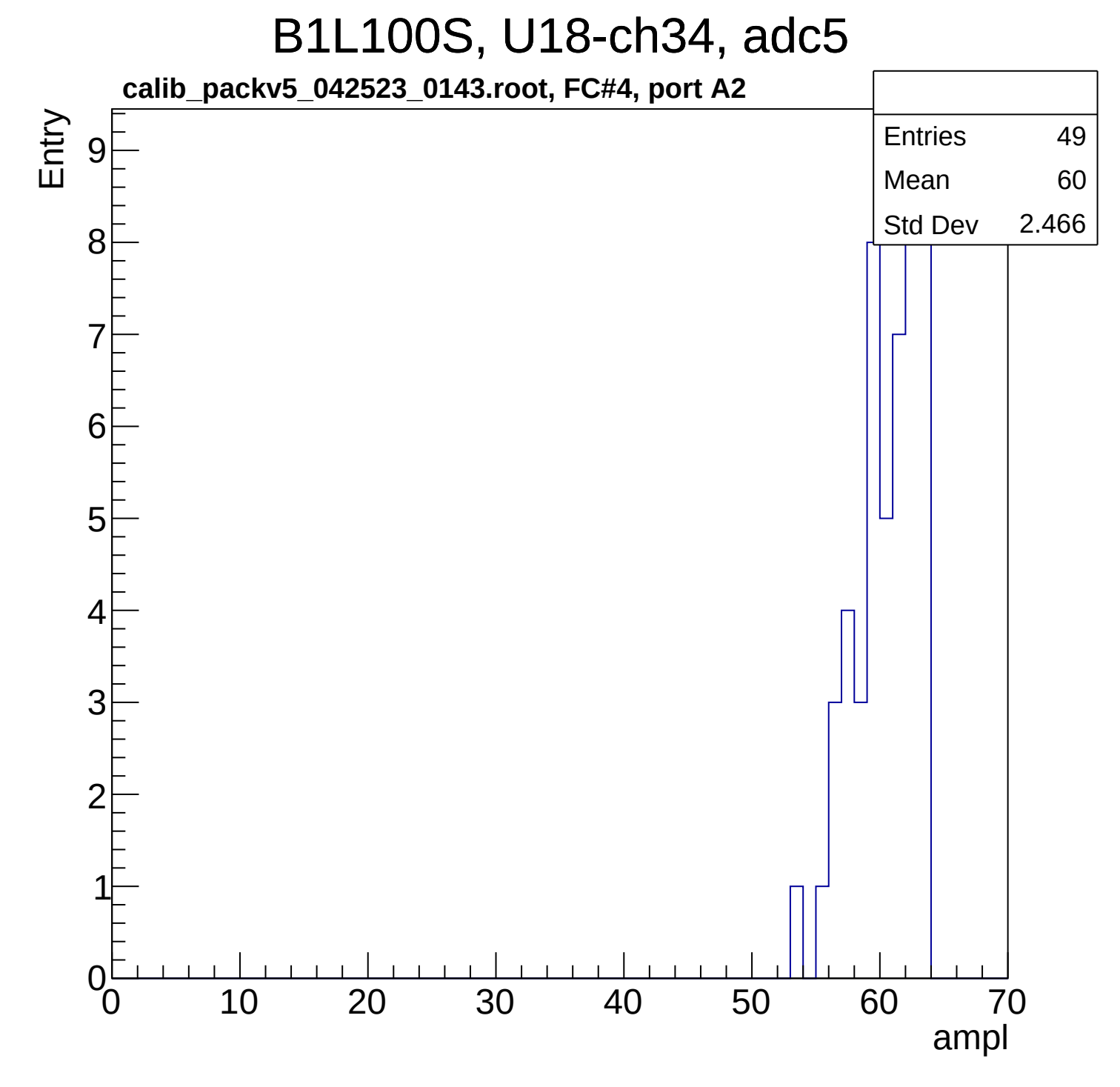

B1L100S, U18-ch34, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 29.26
Std Dev 3.496
Gaus mean : 29.6576
Gaus Width: 3.5911
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

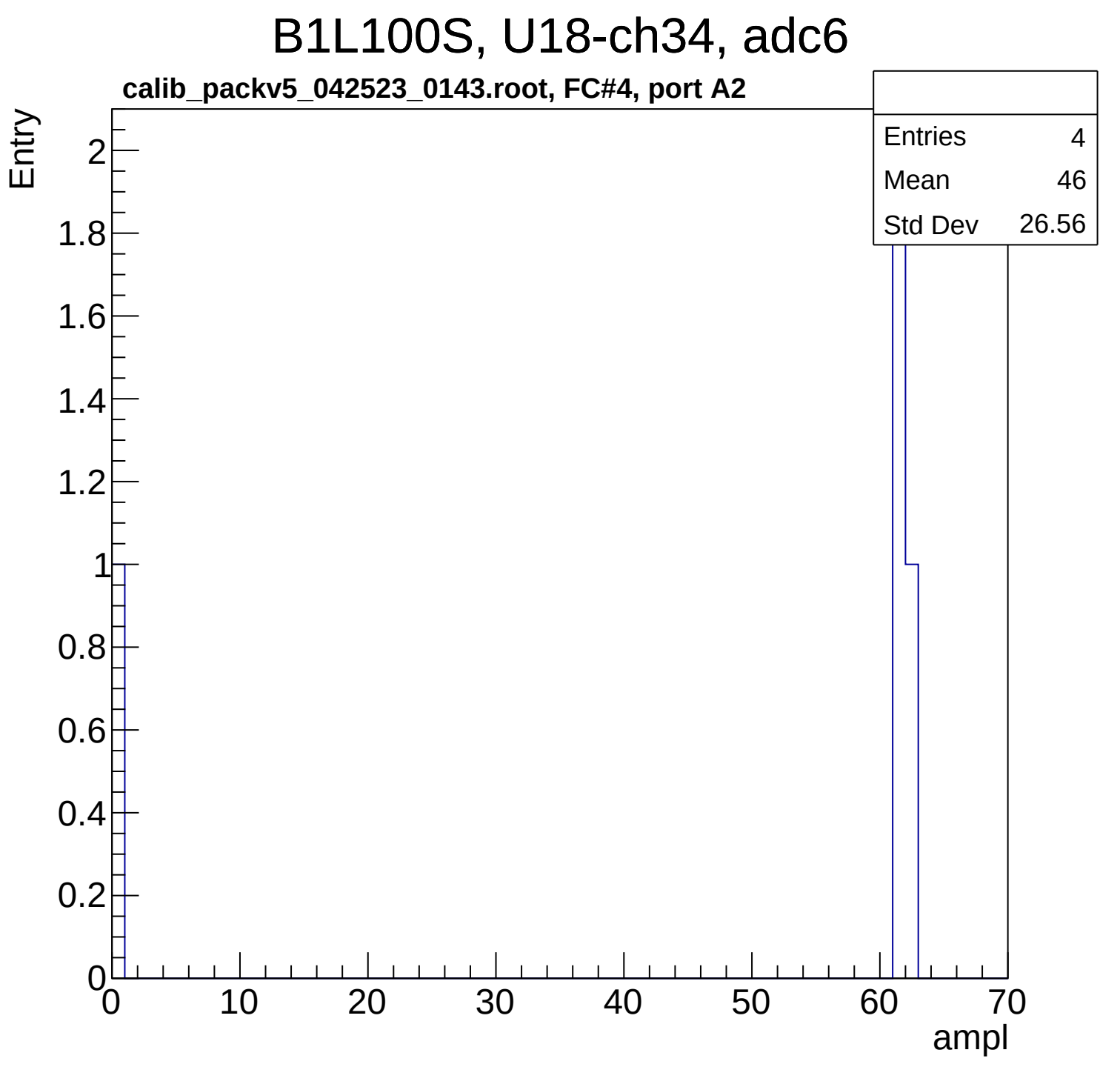

B1L100S, U18-ch34, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 36.89
Std Dev 3.561
Gaus mean : 37.0697
Gaus Width: 3.4875
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

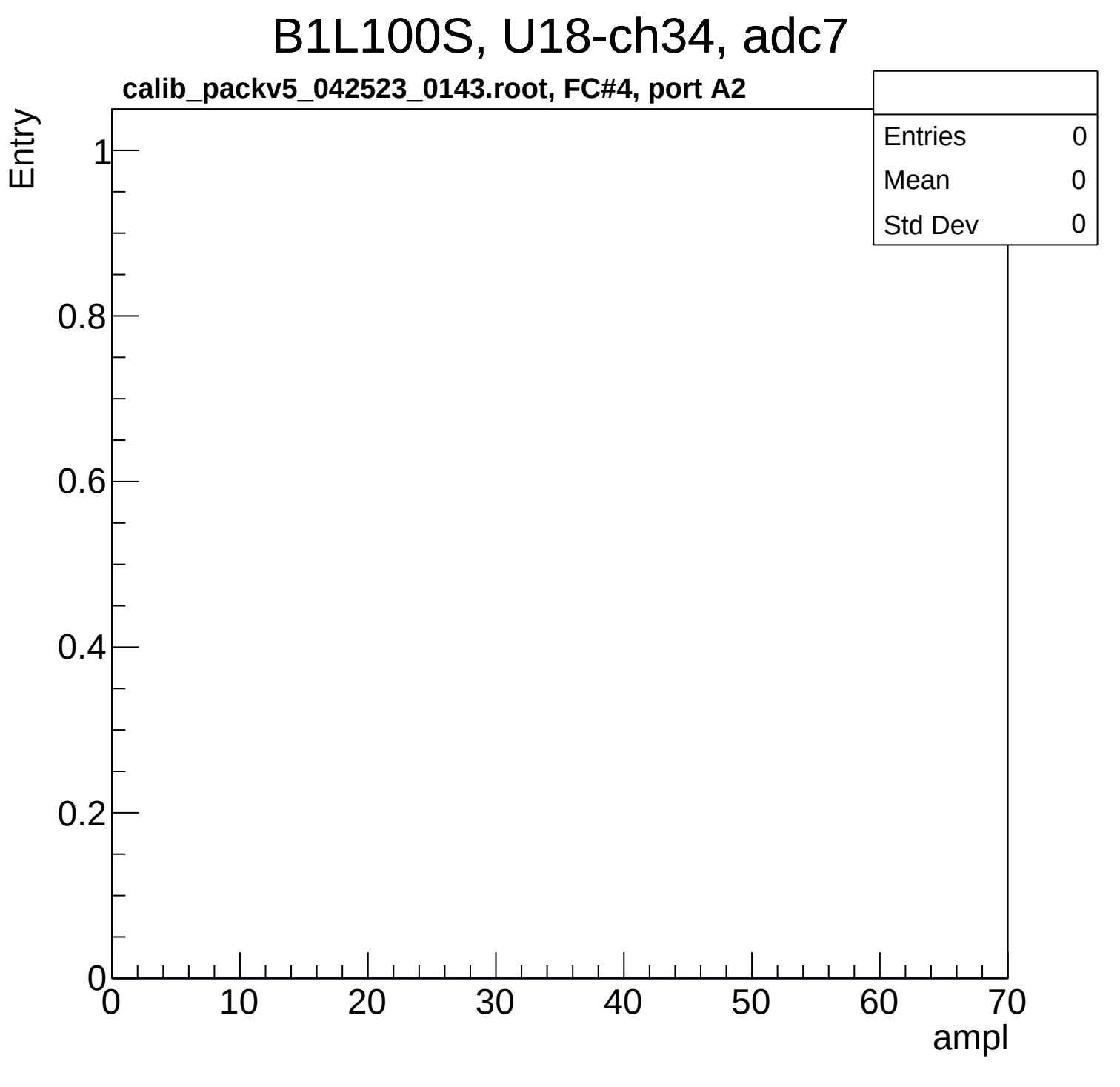

B1L100S, U18-ch34, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 44.07
Std Dev 3.274
Gaus mean : 44.7912
Gaus Width: 3.3133
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

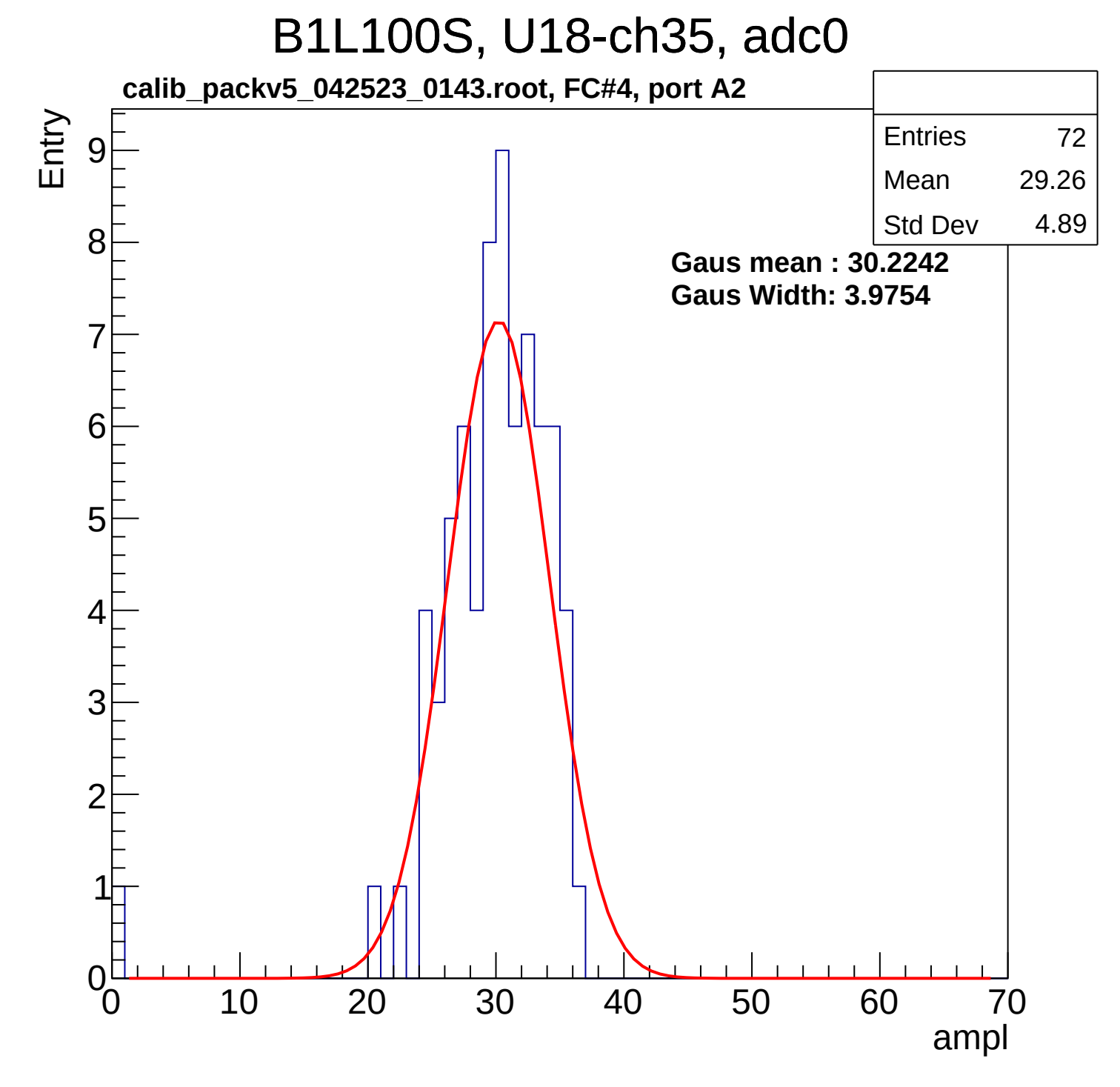

B1L100S, U18-ch34, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 50.02
Std Dev 3.44
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

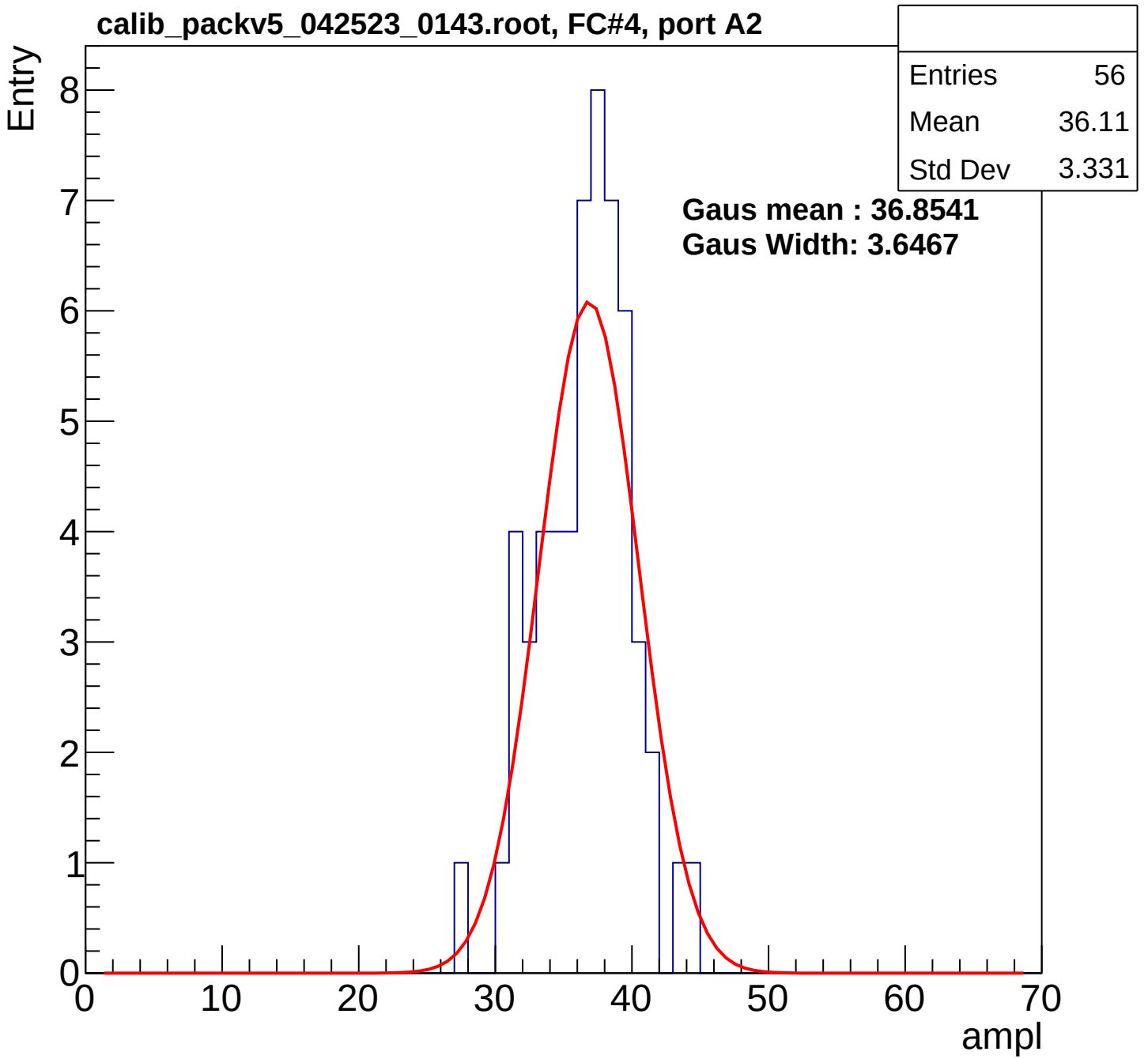

B1L100S, U18-ch34, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 55.92
Std Dev 3.174
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

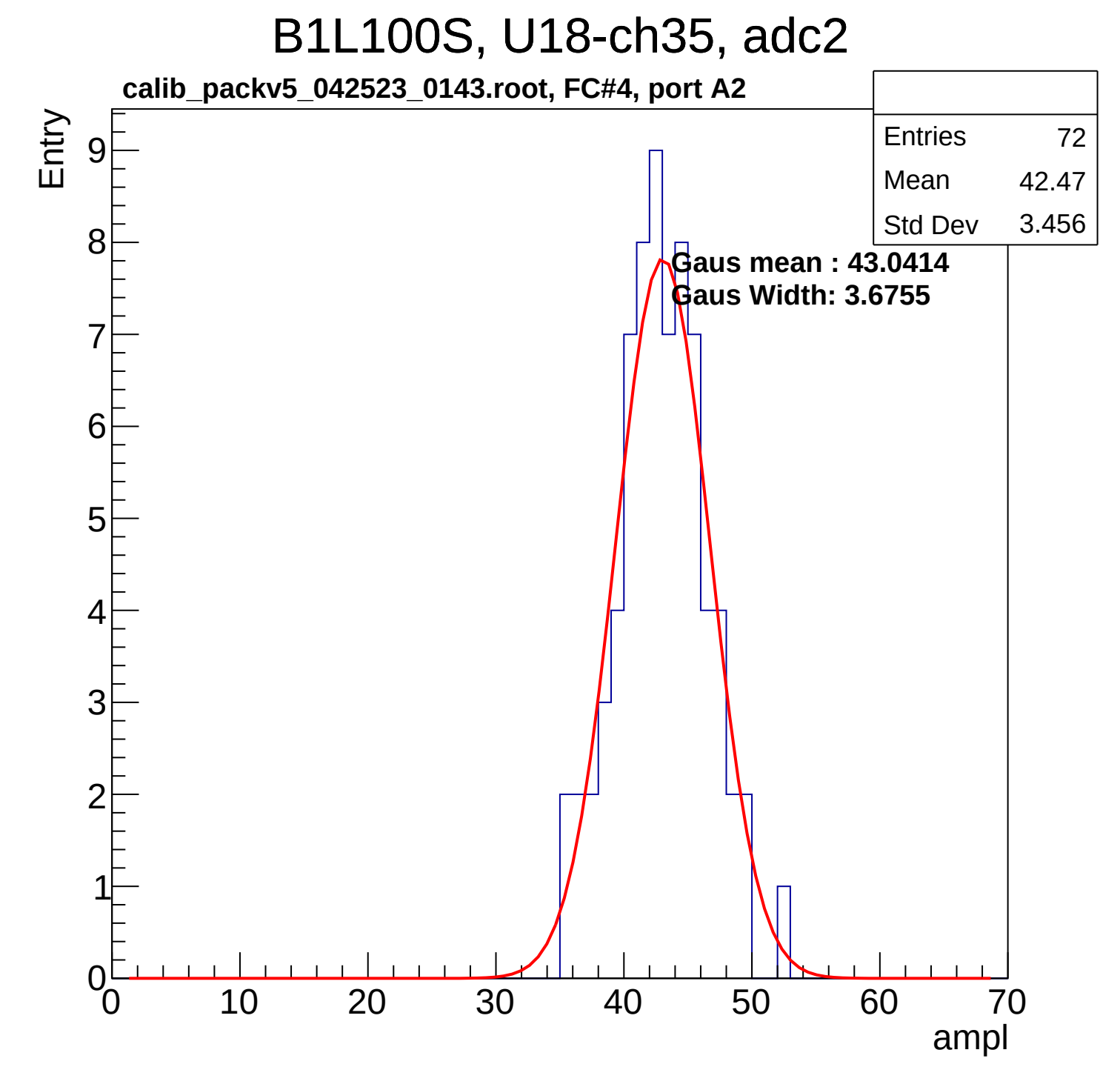

B1L100S, U18-ch34, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 60
Std Dev 2.466
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

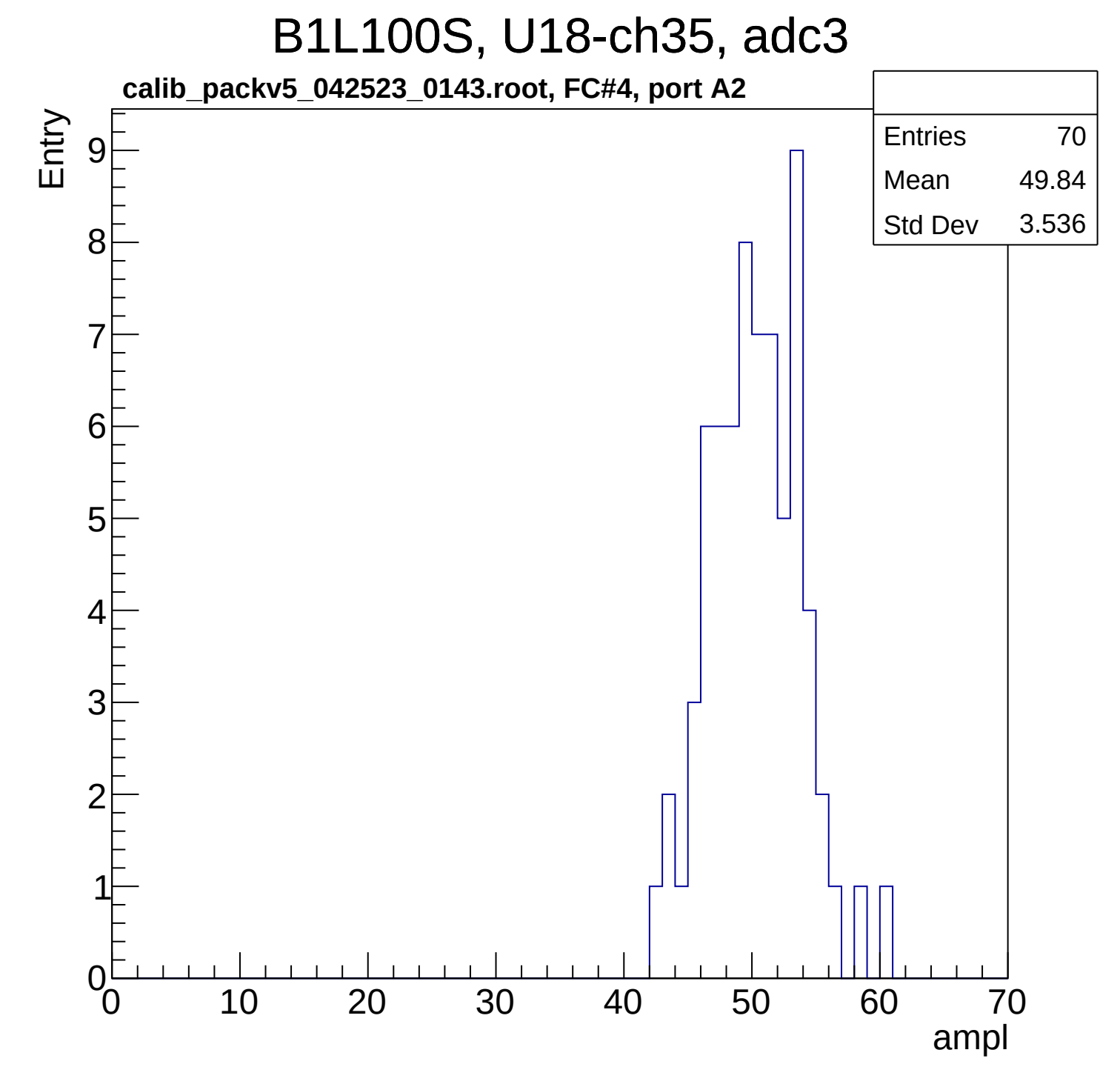

B1L100S, U18-ch34, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 46
Std Dev 26.56
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

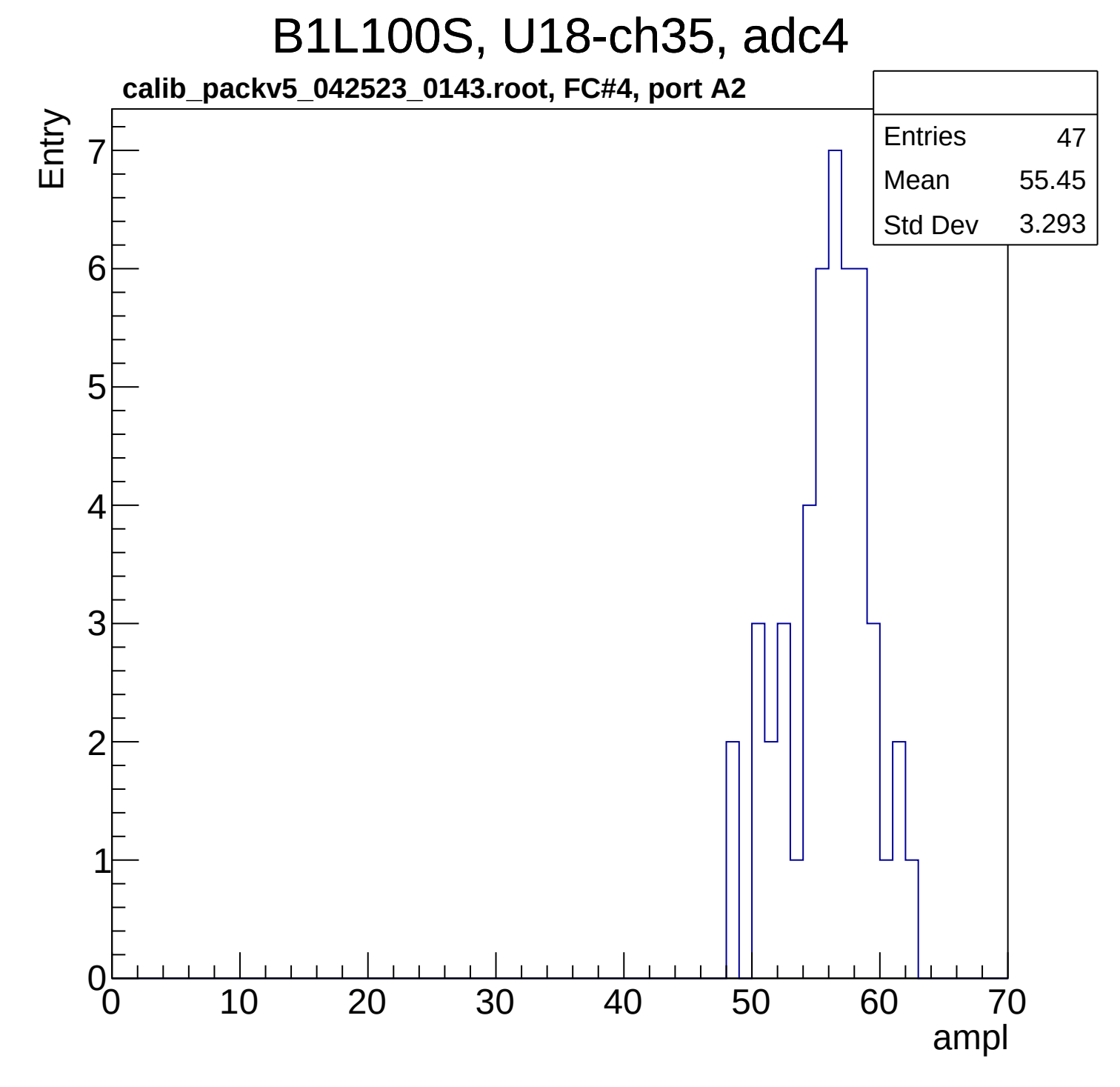

B1L100S, U18-ch34, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

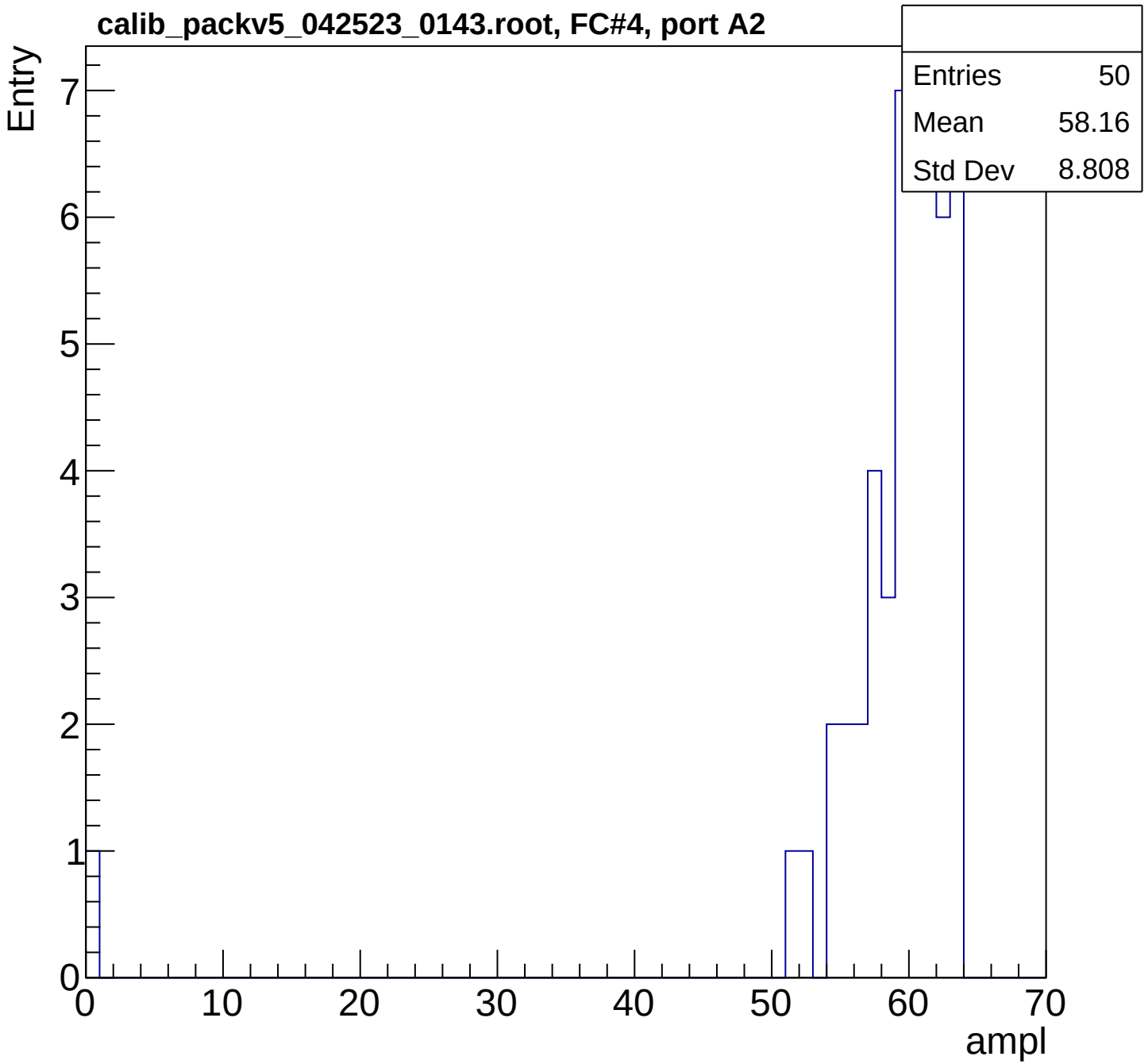

B1L100S, U18-ch35, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 29.26
Std Dev 4.89
Gaus mean : 30.2242
Gaus Width: 3.9754
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

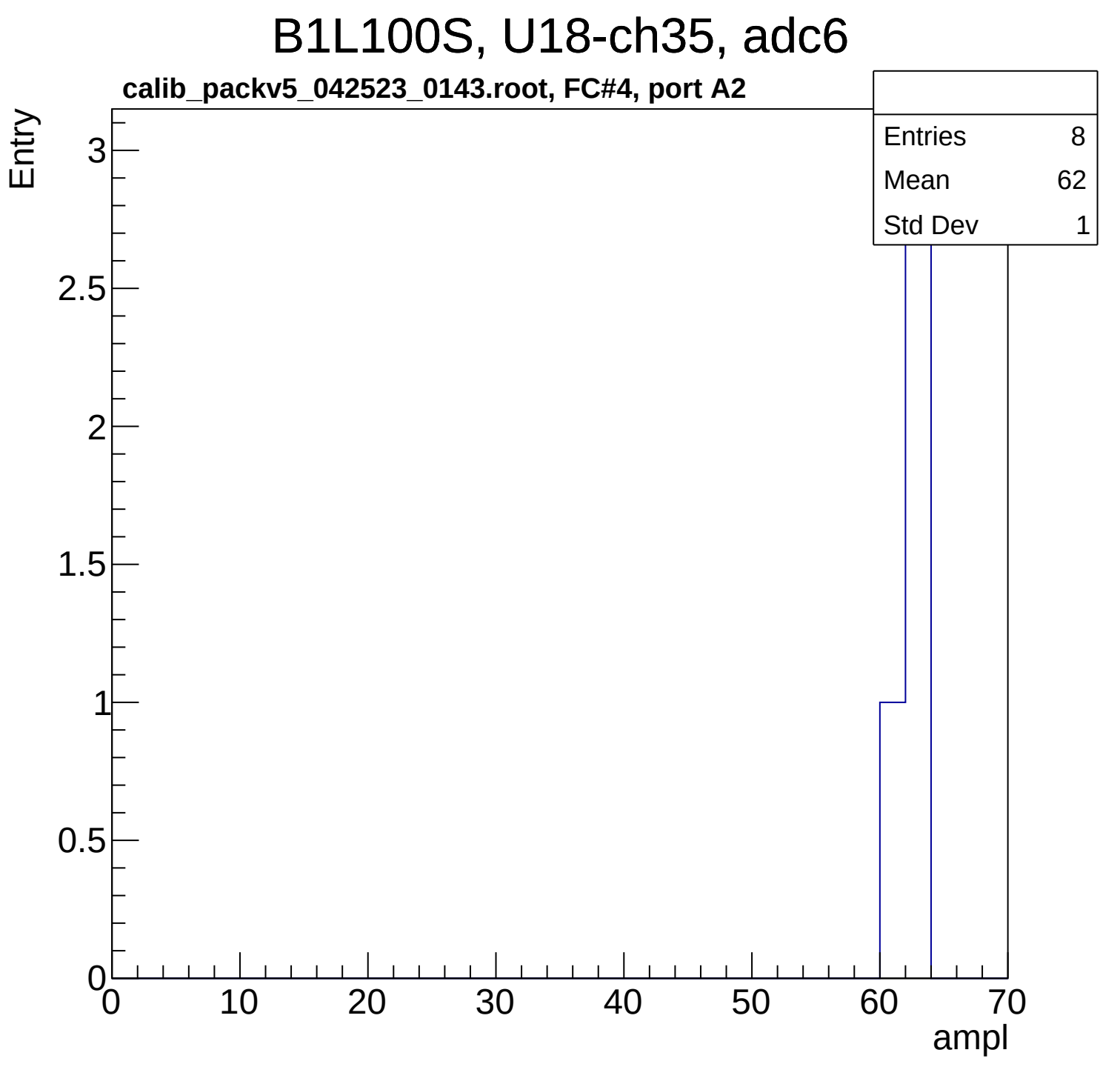

B1L100S, U18-ch35, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 36.11
Std Dev 3.331
Gaus mean : 36.8541
Gaus Width: 3.6467
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

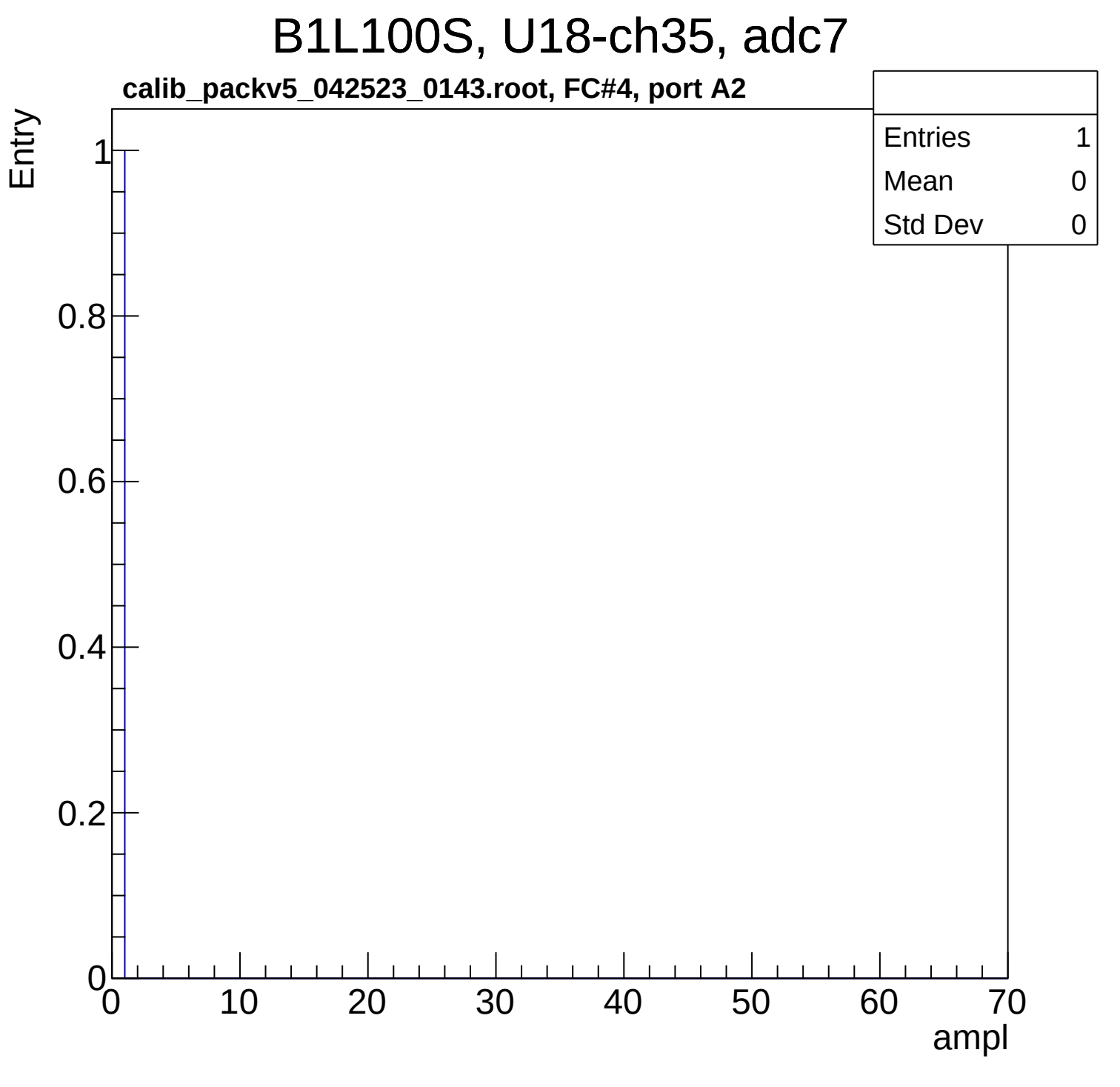

B1L100S, U18-ch35, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 42.47
Std Dev 3.456
Gaus mean : 43.0414
Gaus Width: 3.6755
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

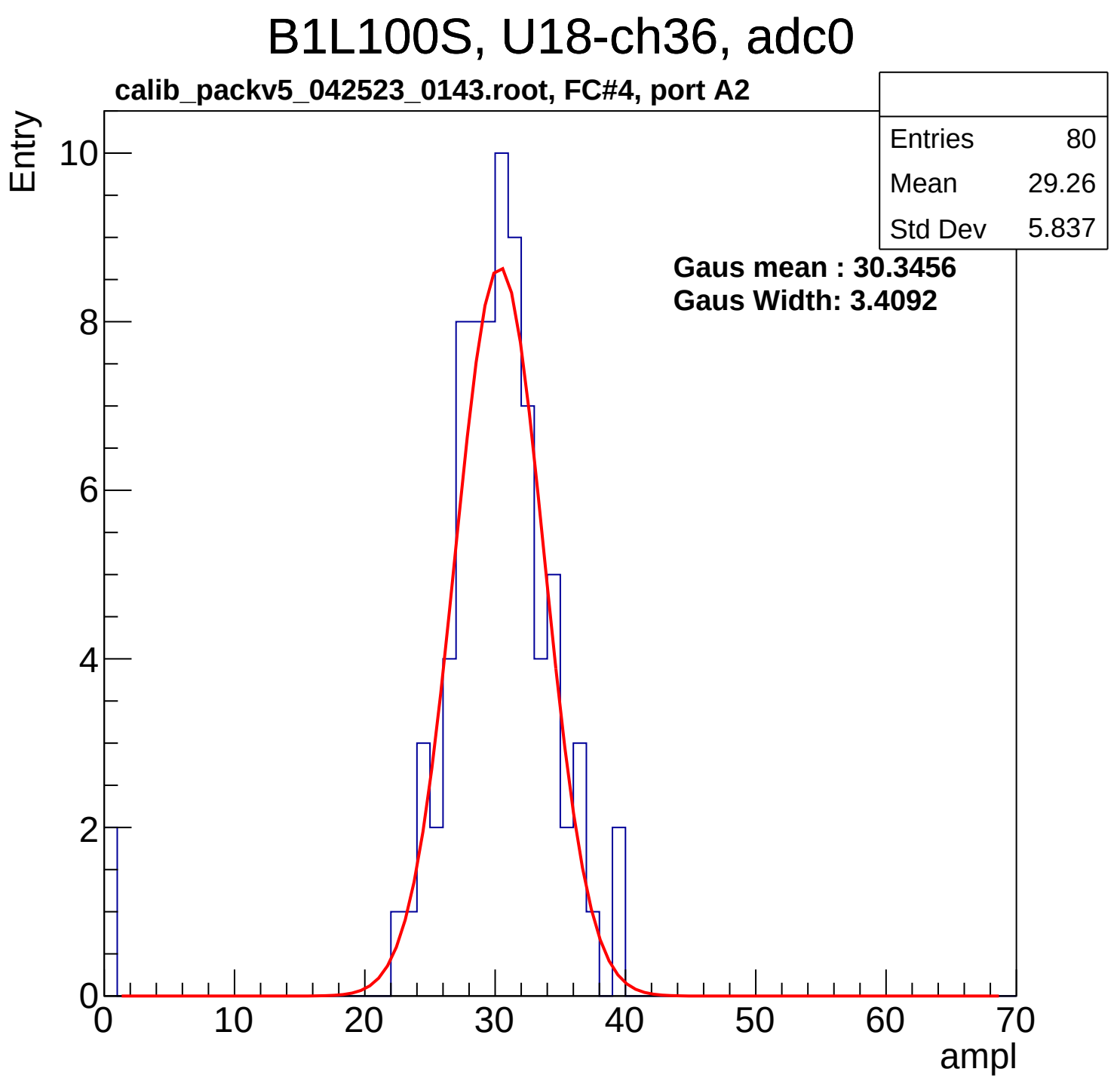

B1L100S, U18-ch35, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 49.84
Std Dev 3.536
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

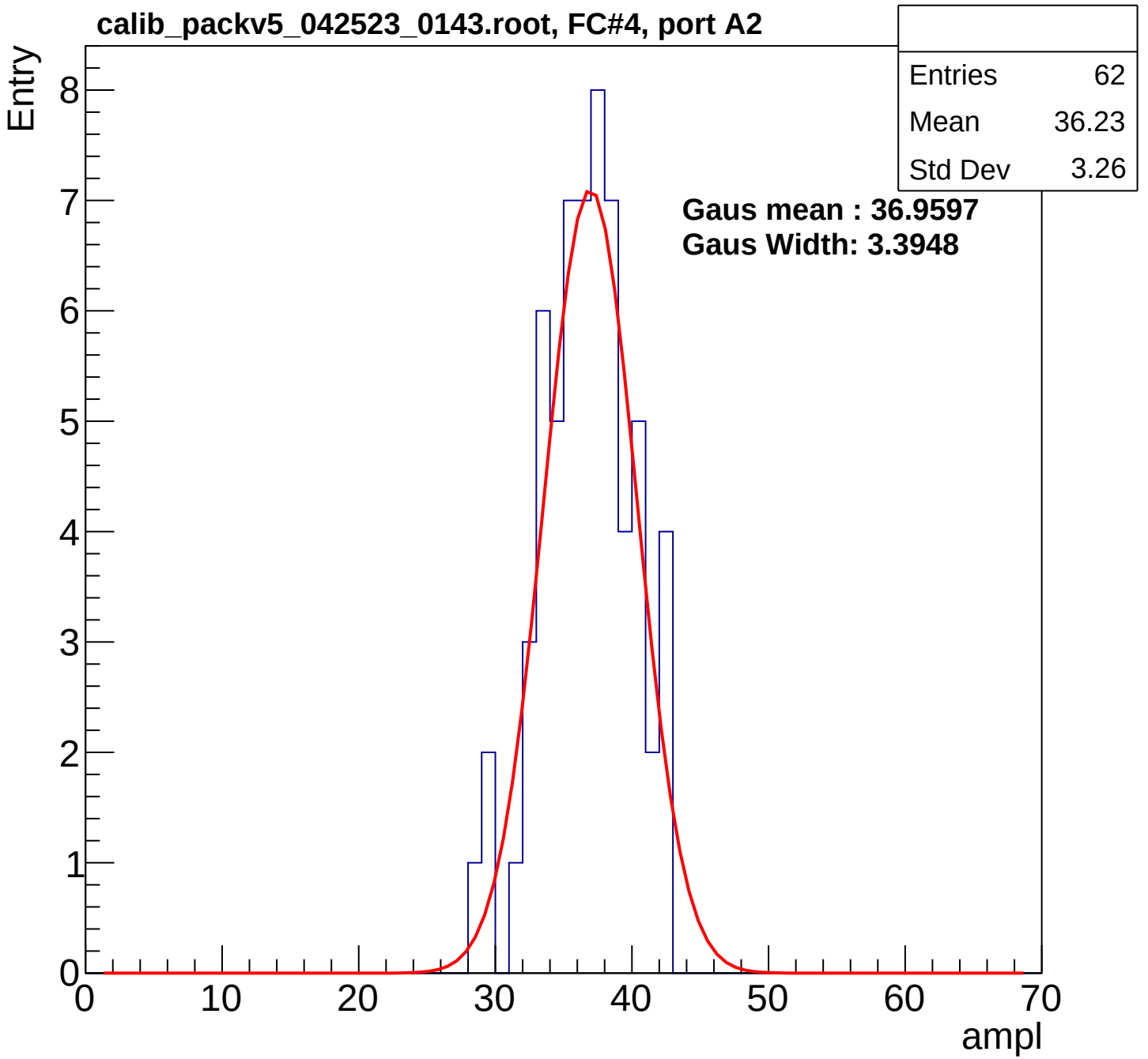

B1L100S, U18-ch35, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 55.45
Std Dev 3.293
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

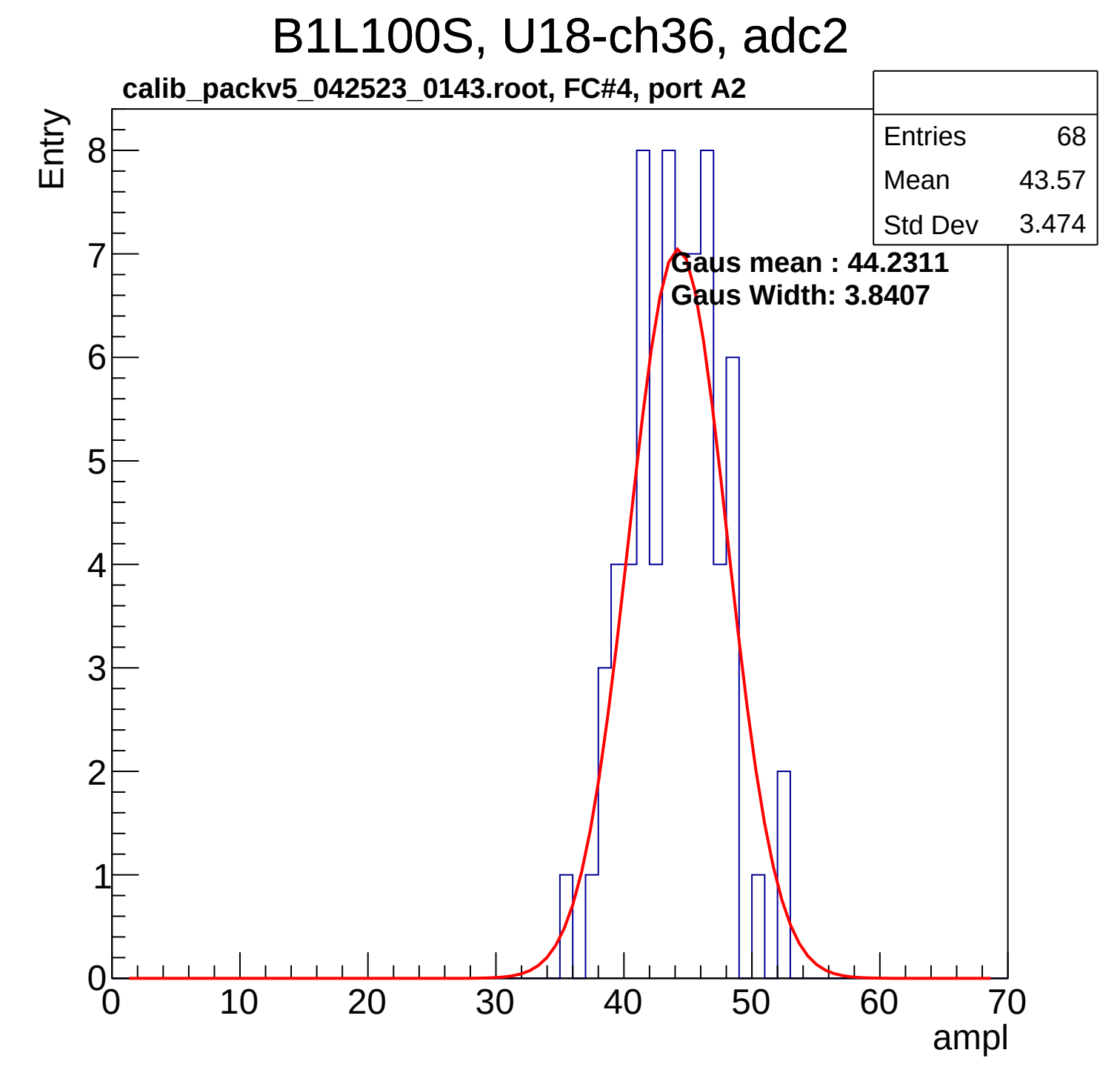

B1L100S, U18-ch35, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 58.16
Std Dev 8.808
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

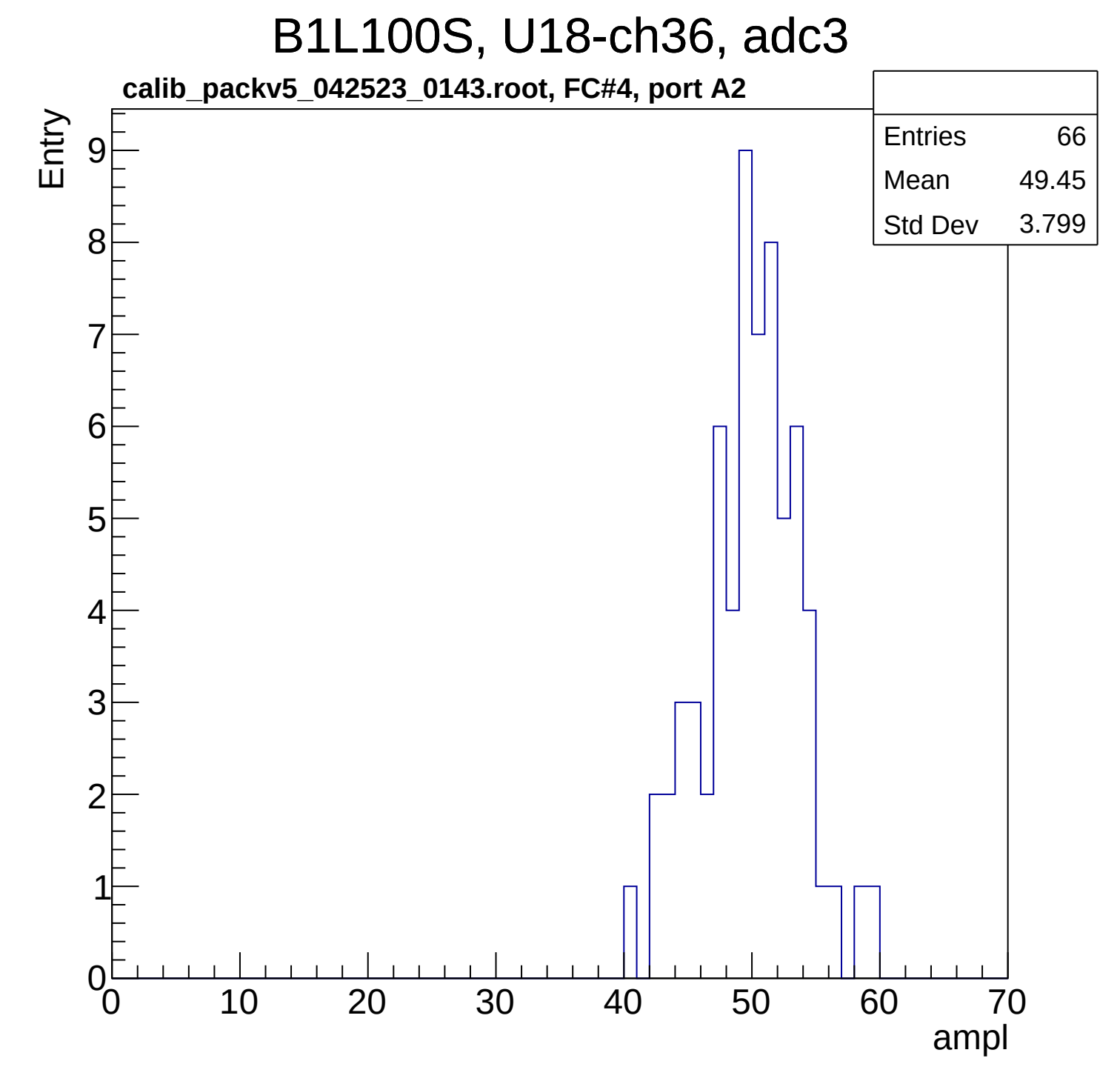

B1L100S, U18-ch35, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 8
Mean 62
Std Dev 1
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

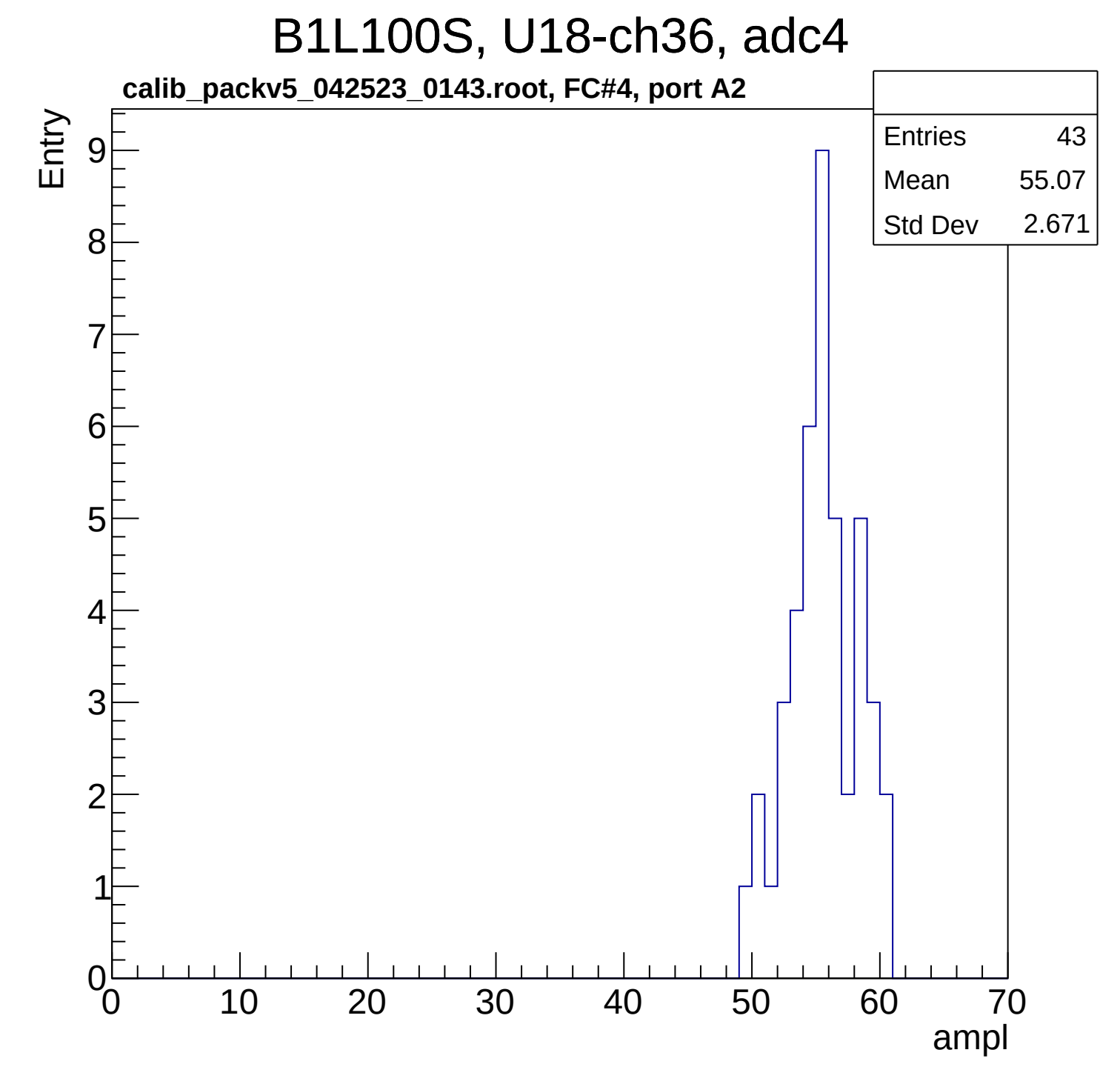

B1L100S, U18-ch35, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

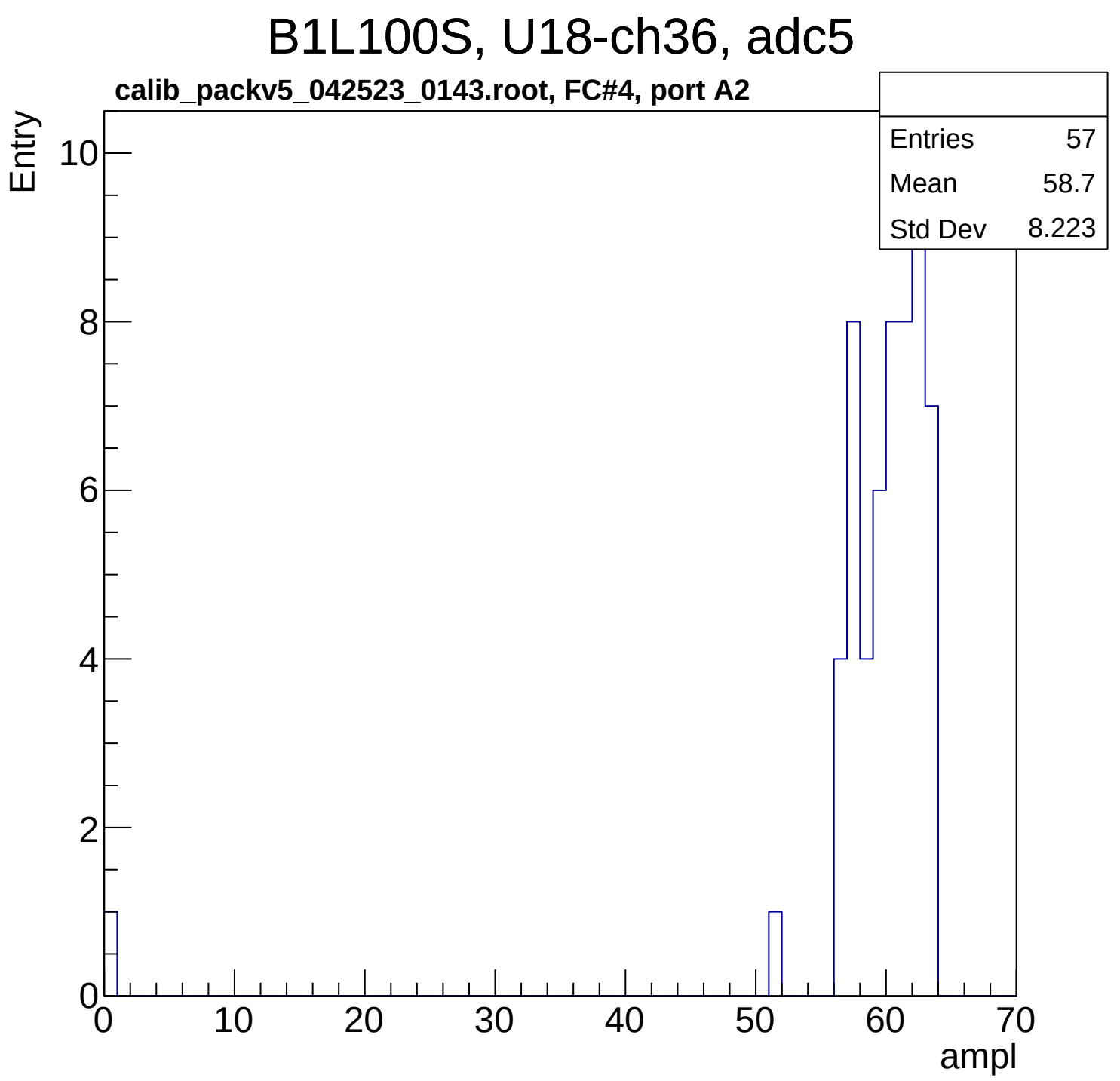

B1L100S, U18-ch36, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 29.26
Std Dev 5.837
Gaus mean : 30.3456
Gaus Width: 3.4092
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

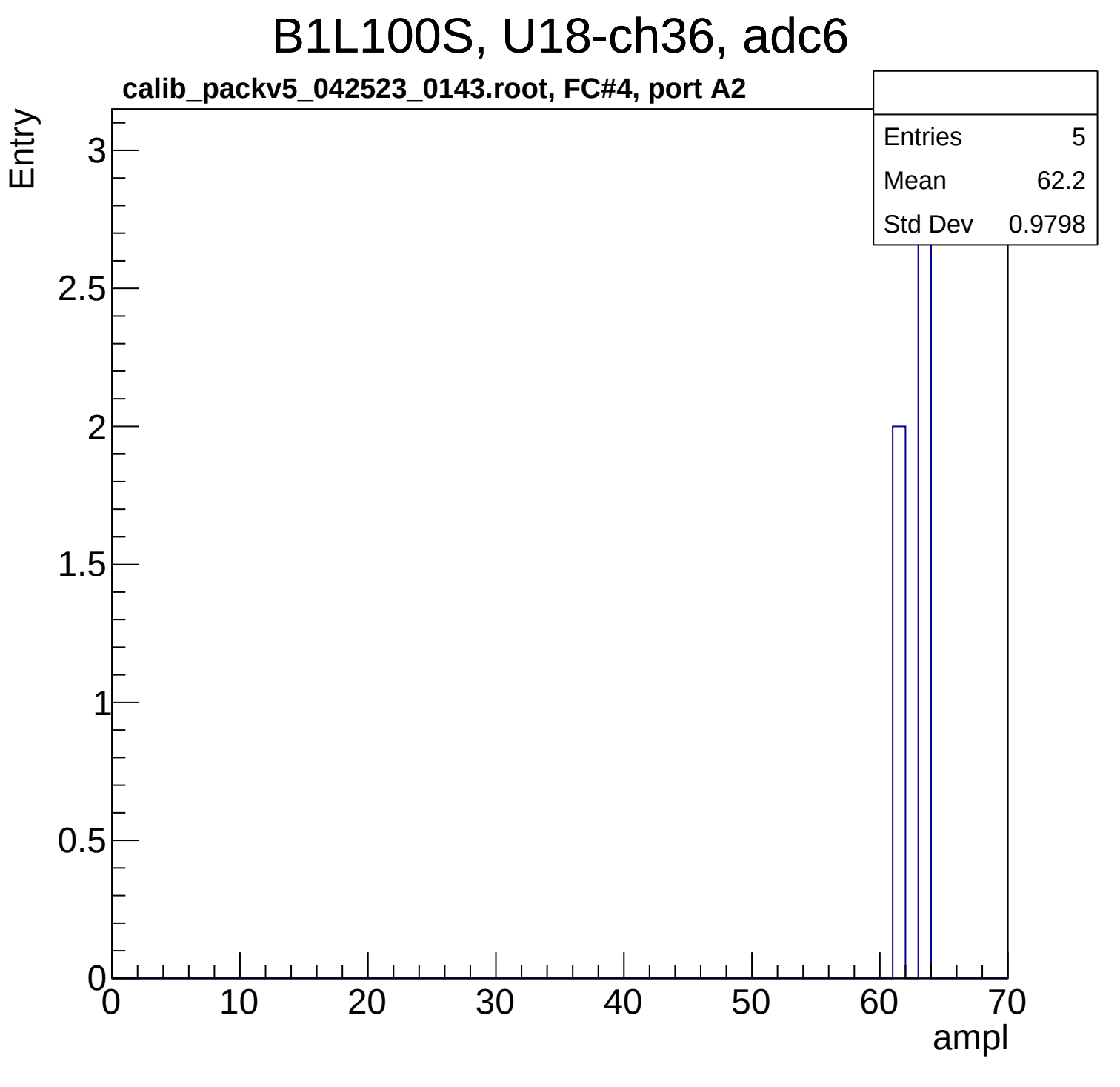

B1L100S, U18-ch36, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 36.23
Std Dev 3.26
Gaus mean : 36.9597
Gaus Width: 3.3948
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

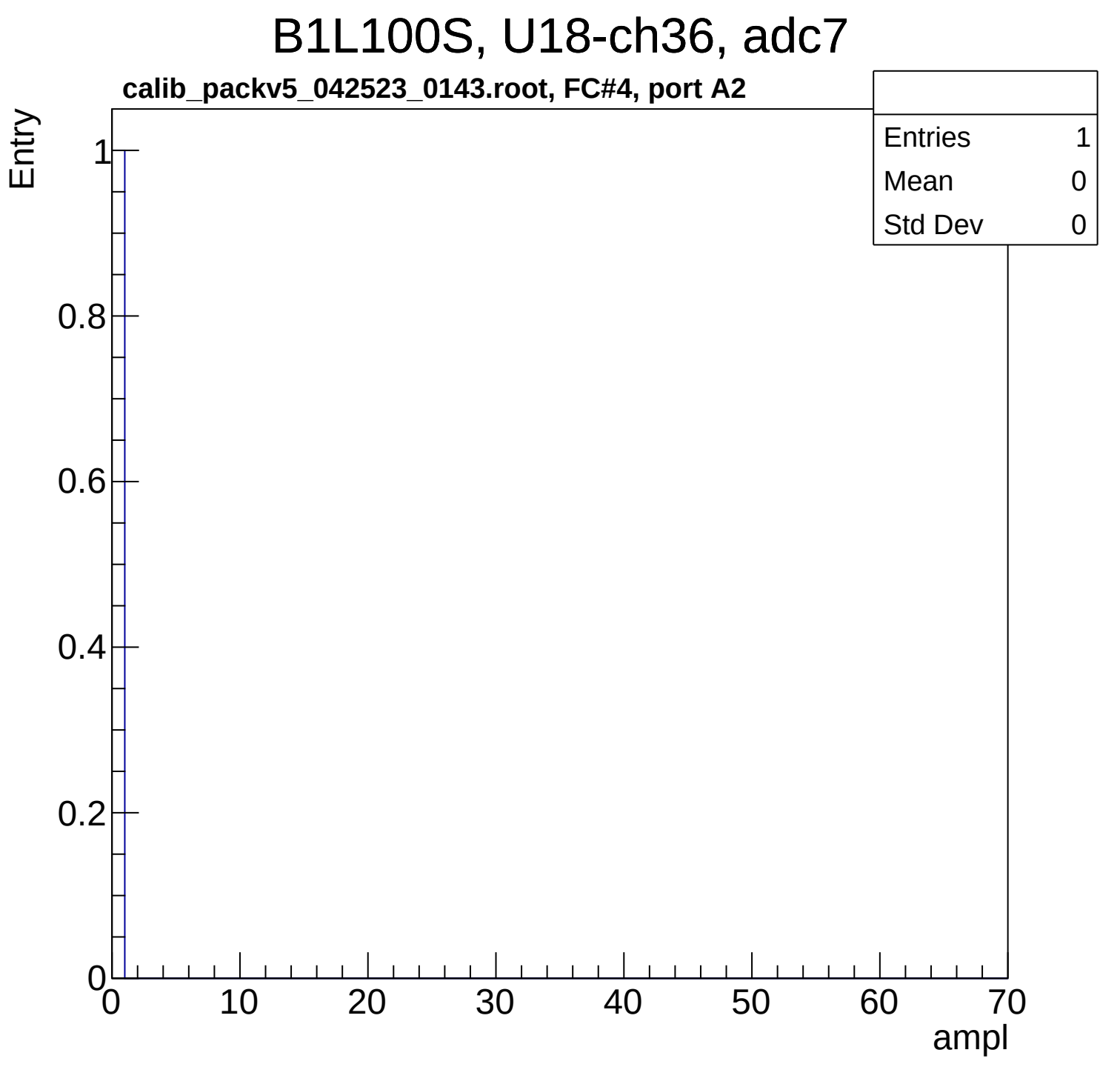

B1L100S, U18-ch36, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 43.57
Std Dev 3.474
Gaus mean : 44.2311
Gaus Width: 3.8407
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

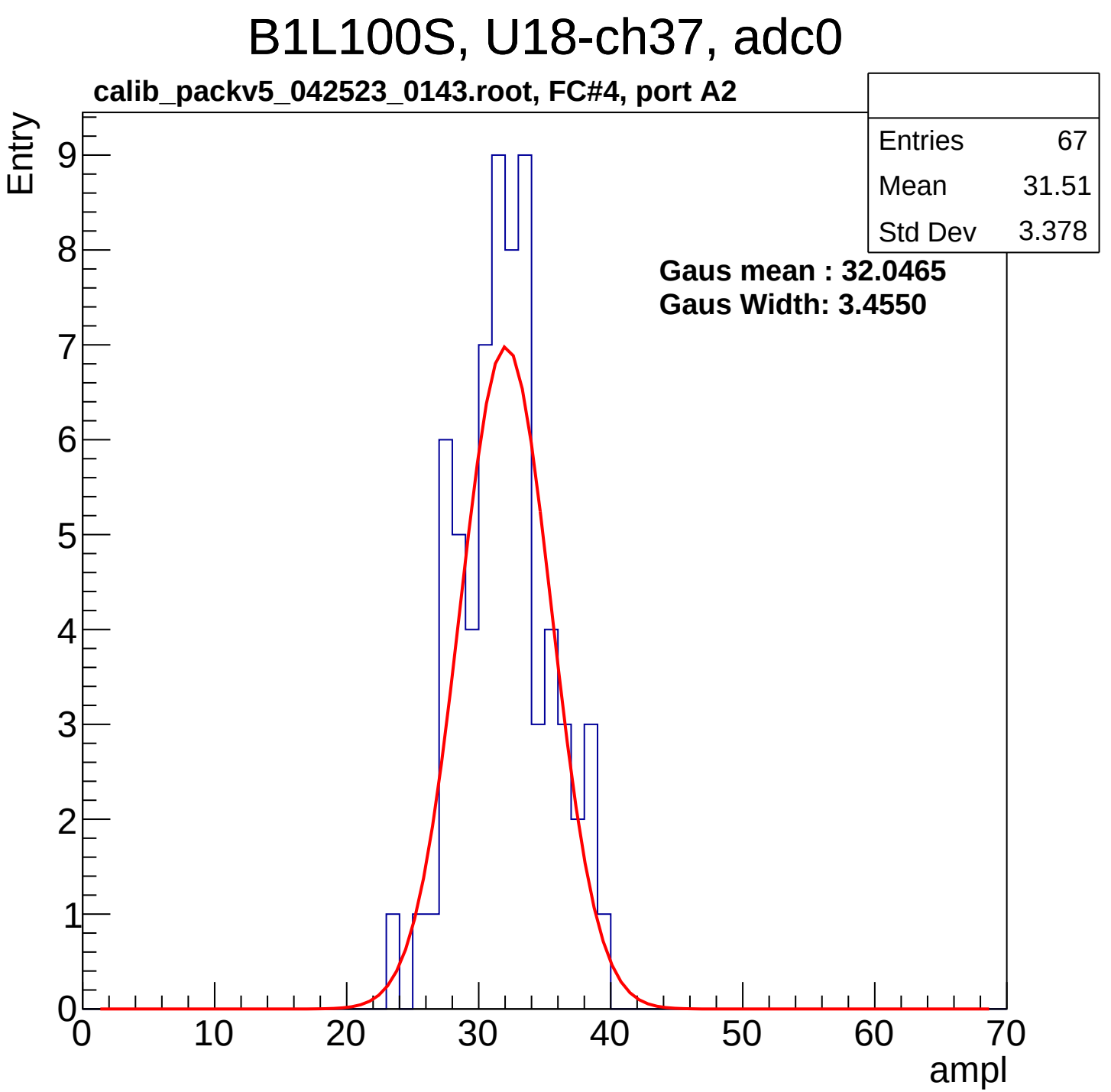

B1L100S, U18-ch36, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 49.45
Std Dev 3.799
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

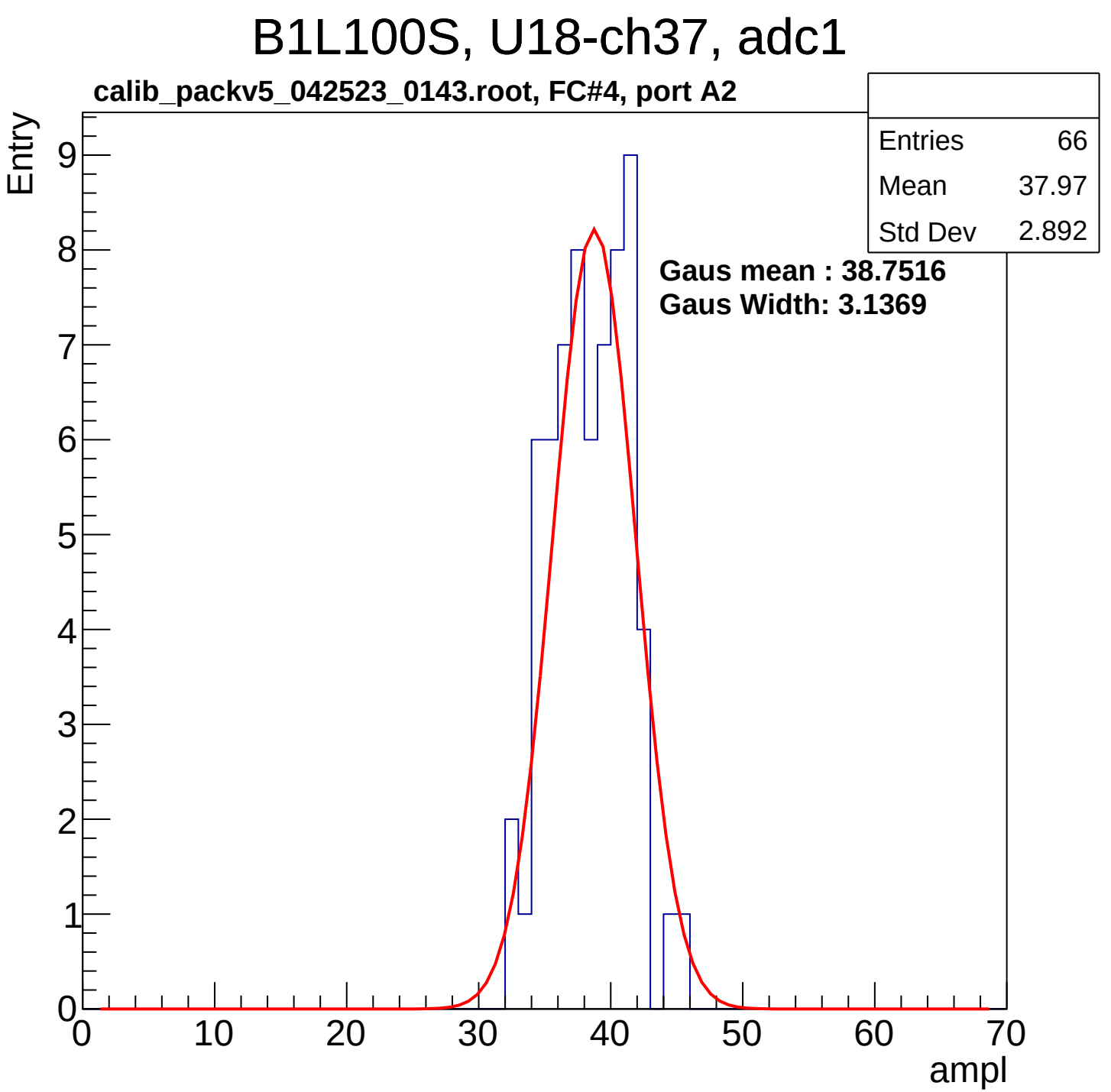

B1L100S, U18-ch36, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 55.07
Std Dev 2.671
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

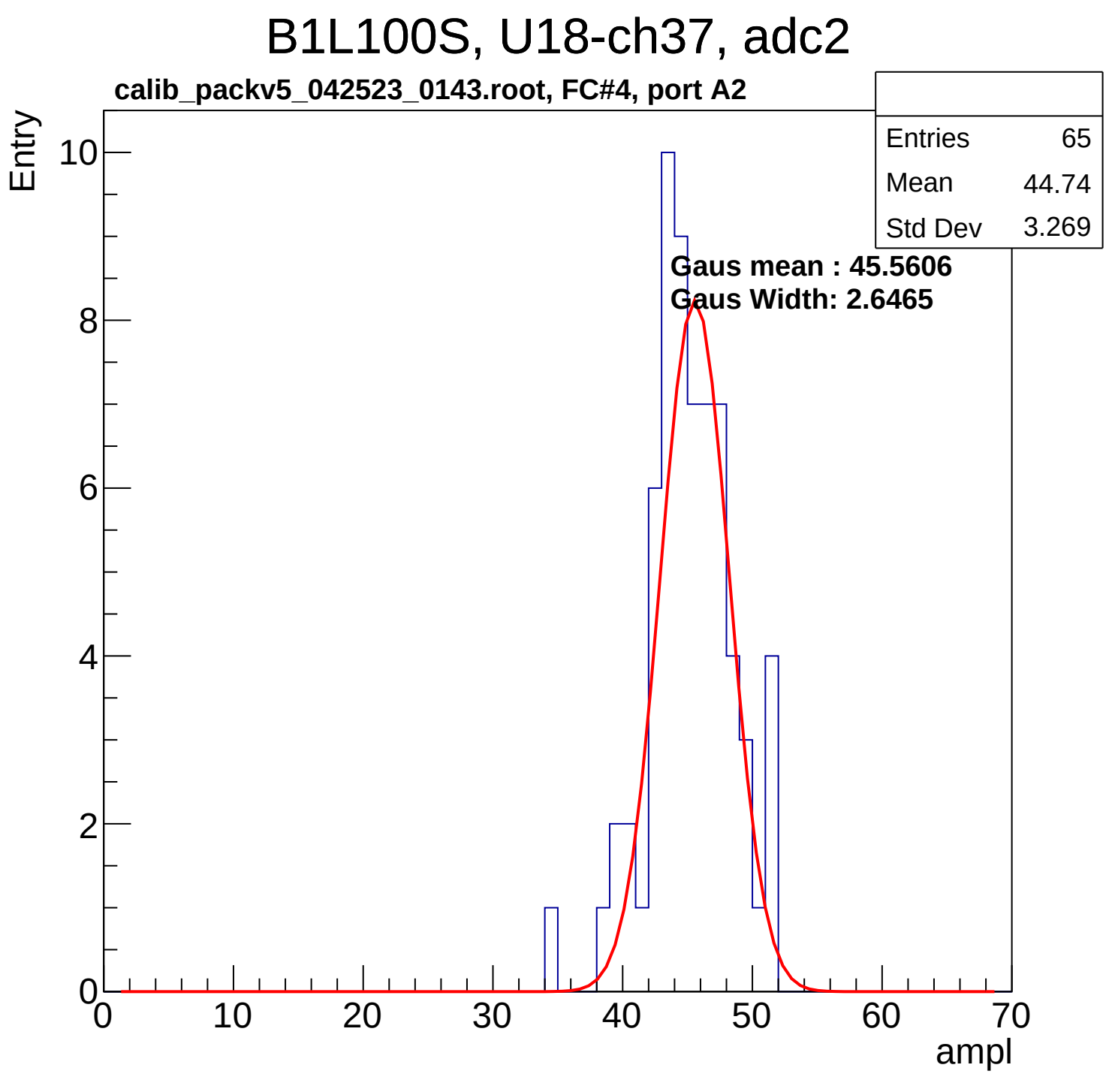

B1L100S, U18-ch36, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 58.7
Std Dev 8.223
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

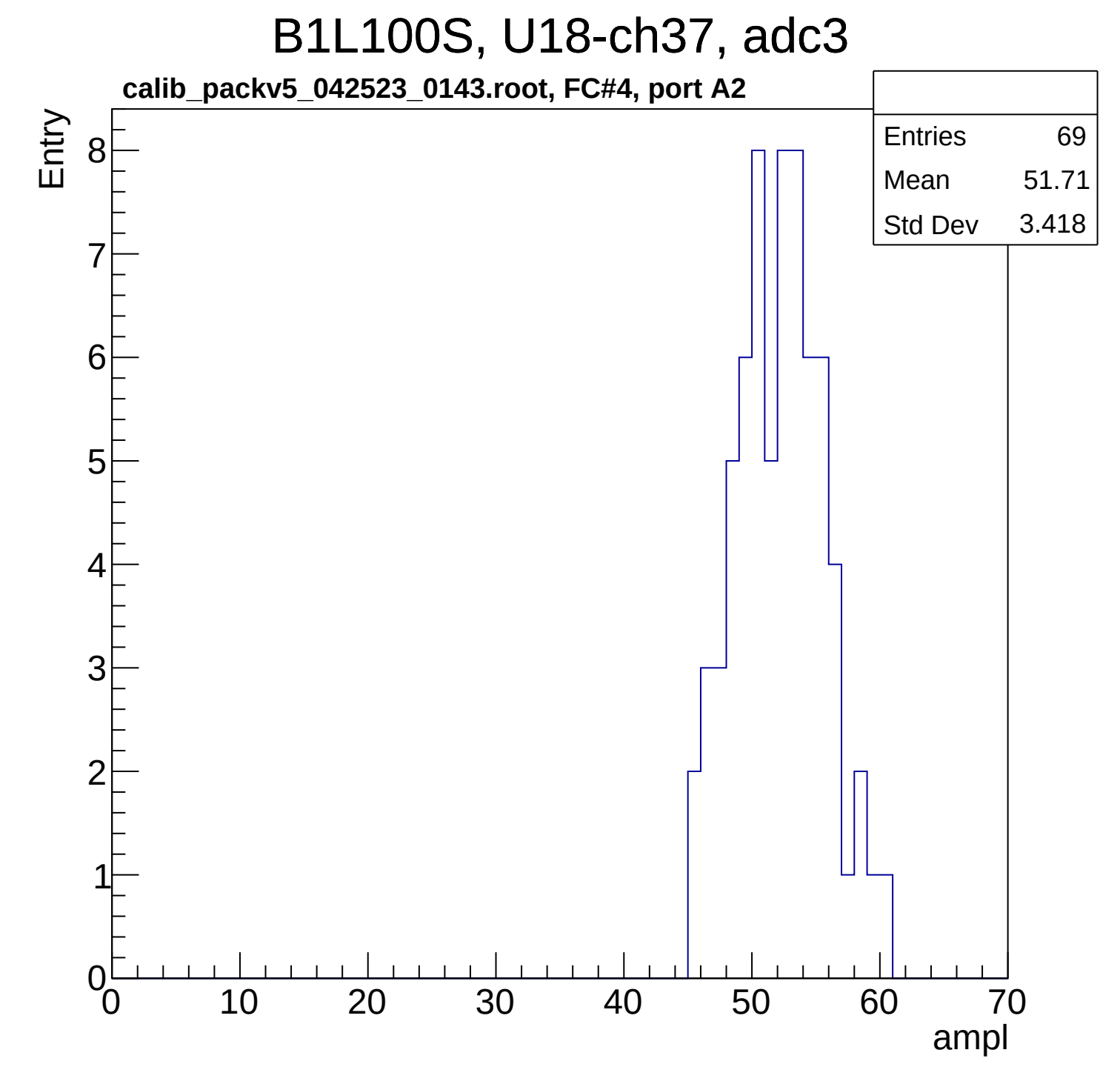

B1L100S, U18-ch36, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 5
Mean 62.2
Std Dev 0.9798
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

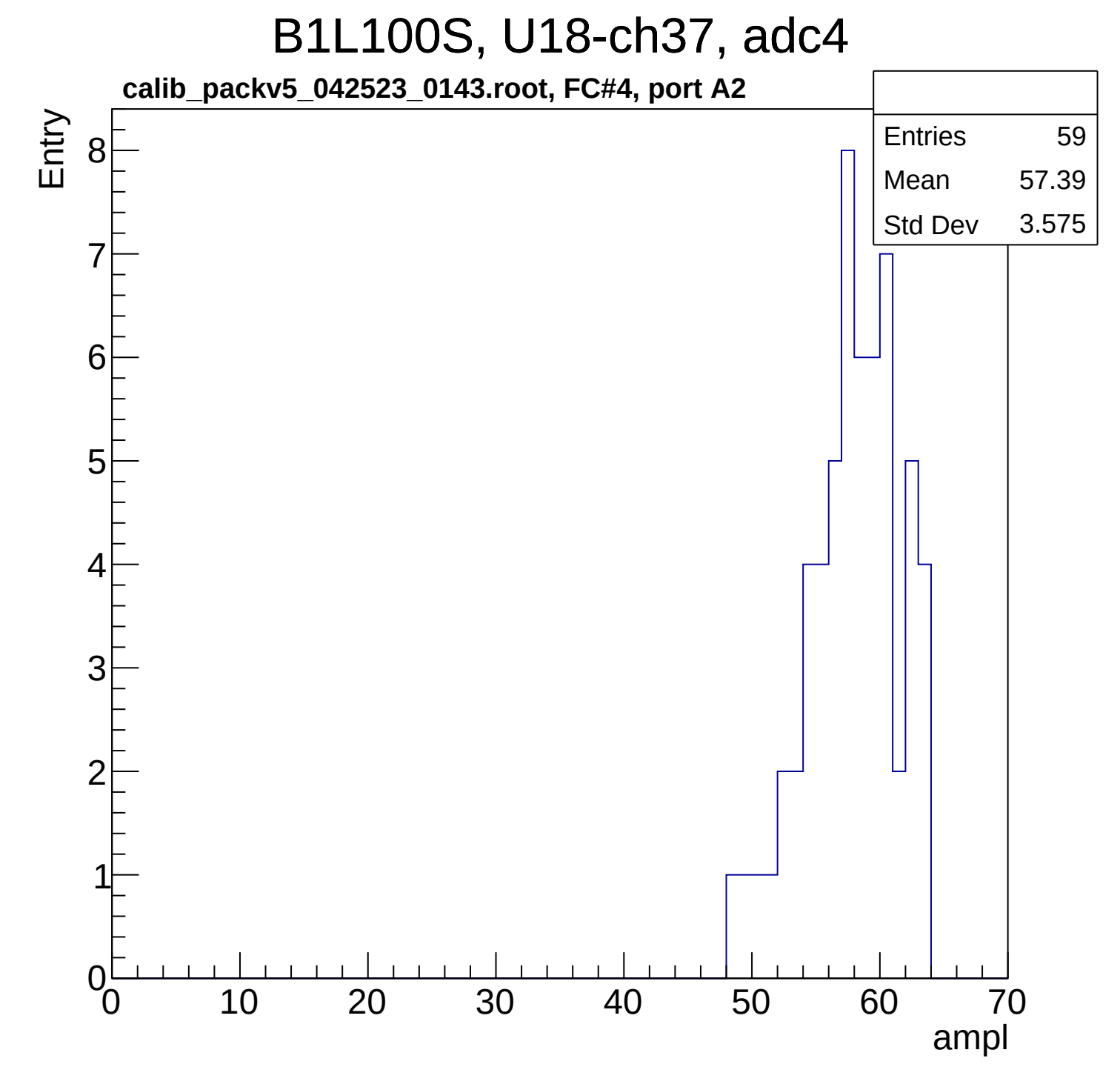

B1L100S, U18-ch36, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

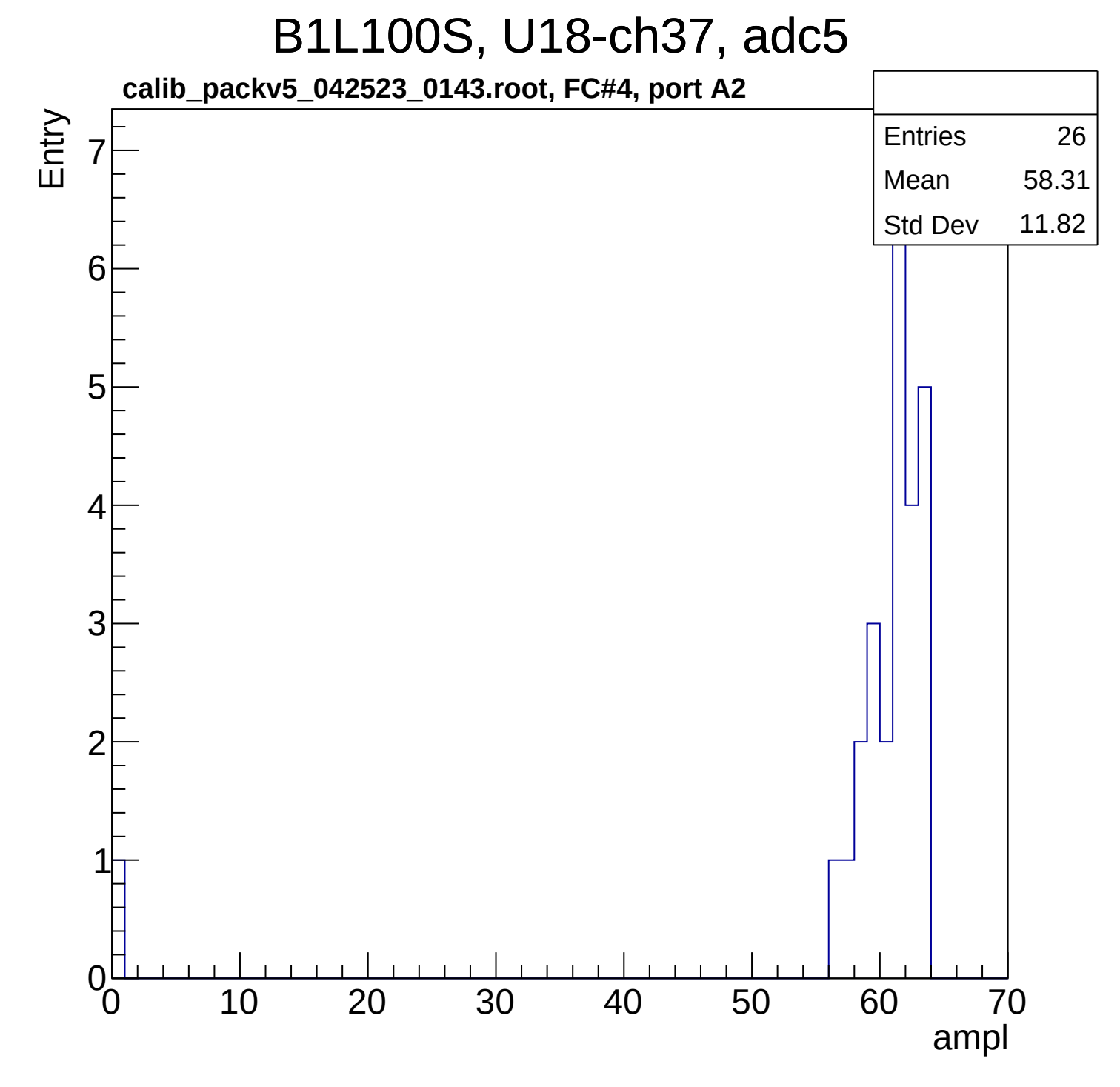

B1L100S, U18-ch37, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 31.51
Std Dev 3.378
Gaus mean : 32.0465
Gaus Width: 3.4550
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

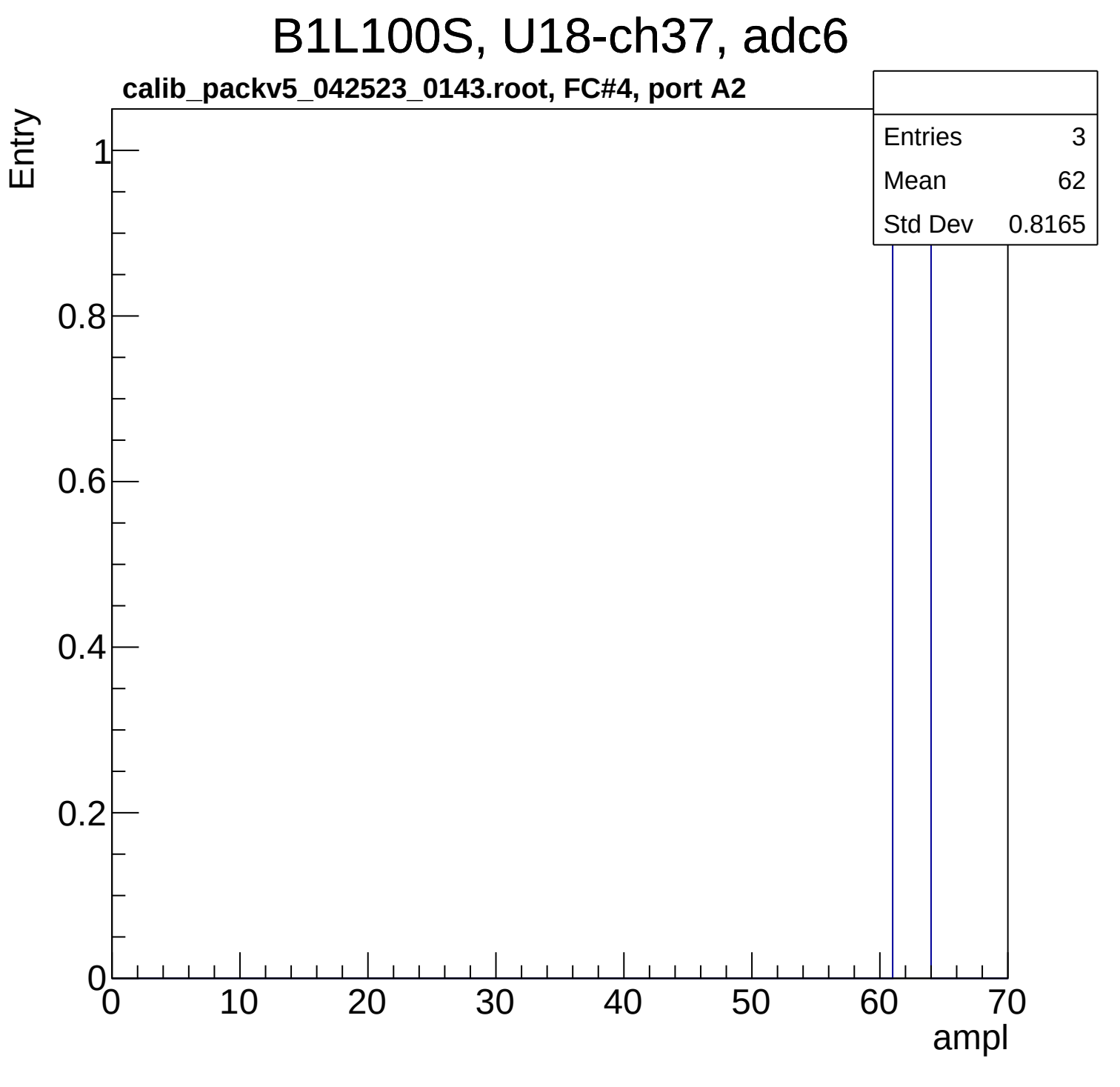

B1L100S, U18-ch37, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 37.97
Std Dev 2.892
Gaus mean : 38.7516
Gaus Width: 3.1369
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

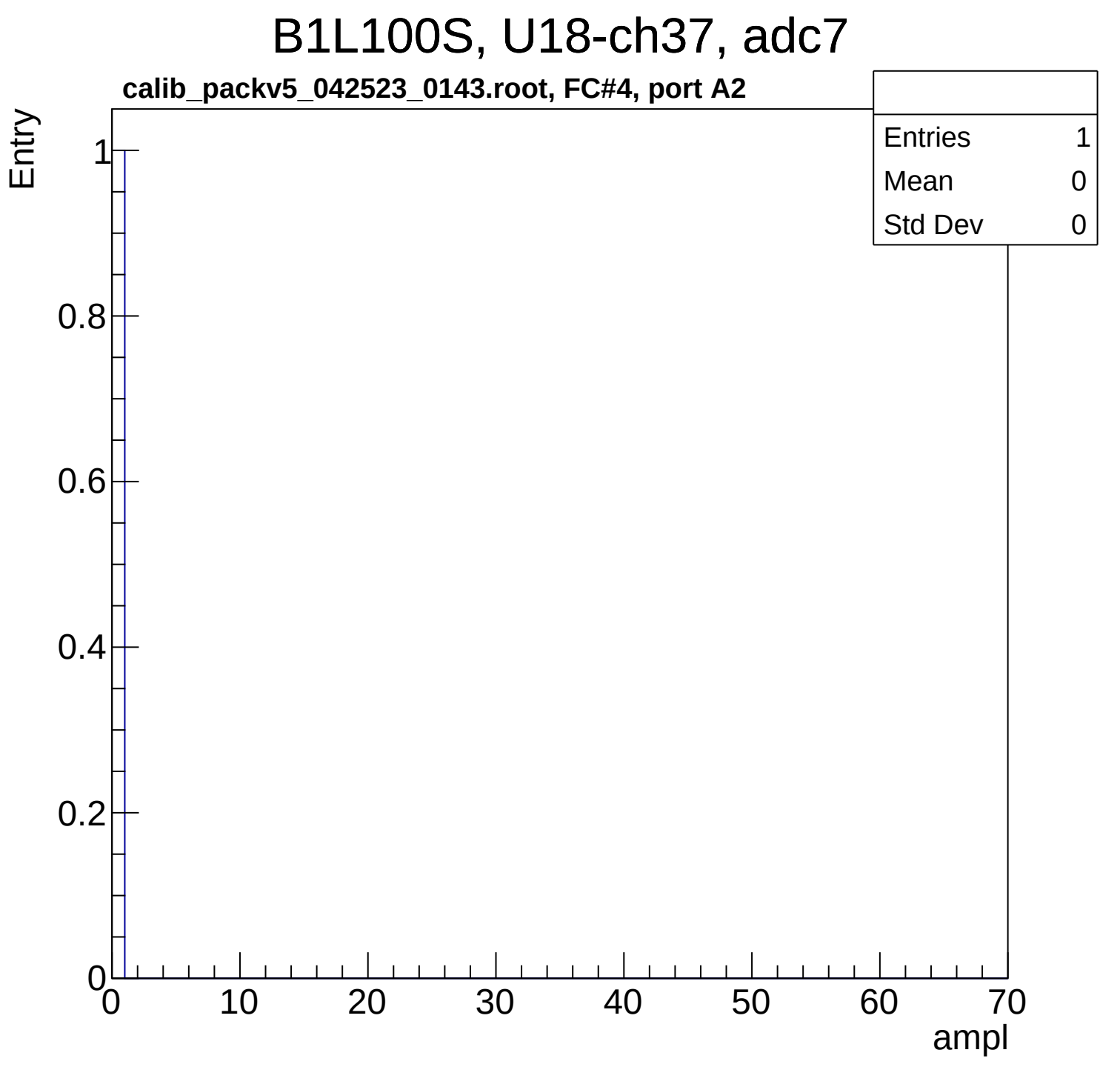

B1L100S, U18-ch37, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 44.74
Std Dev 3.269
Gaus mean : 45.5606
Gaus Width: 2.6465
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

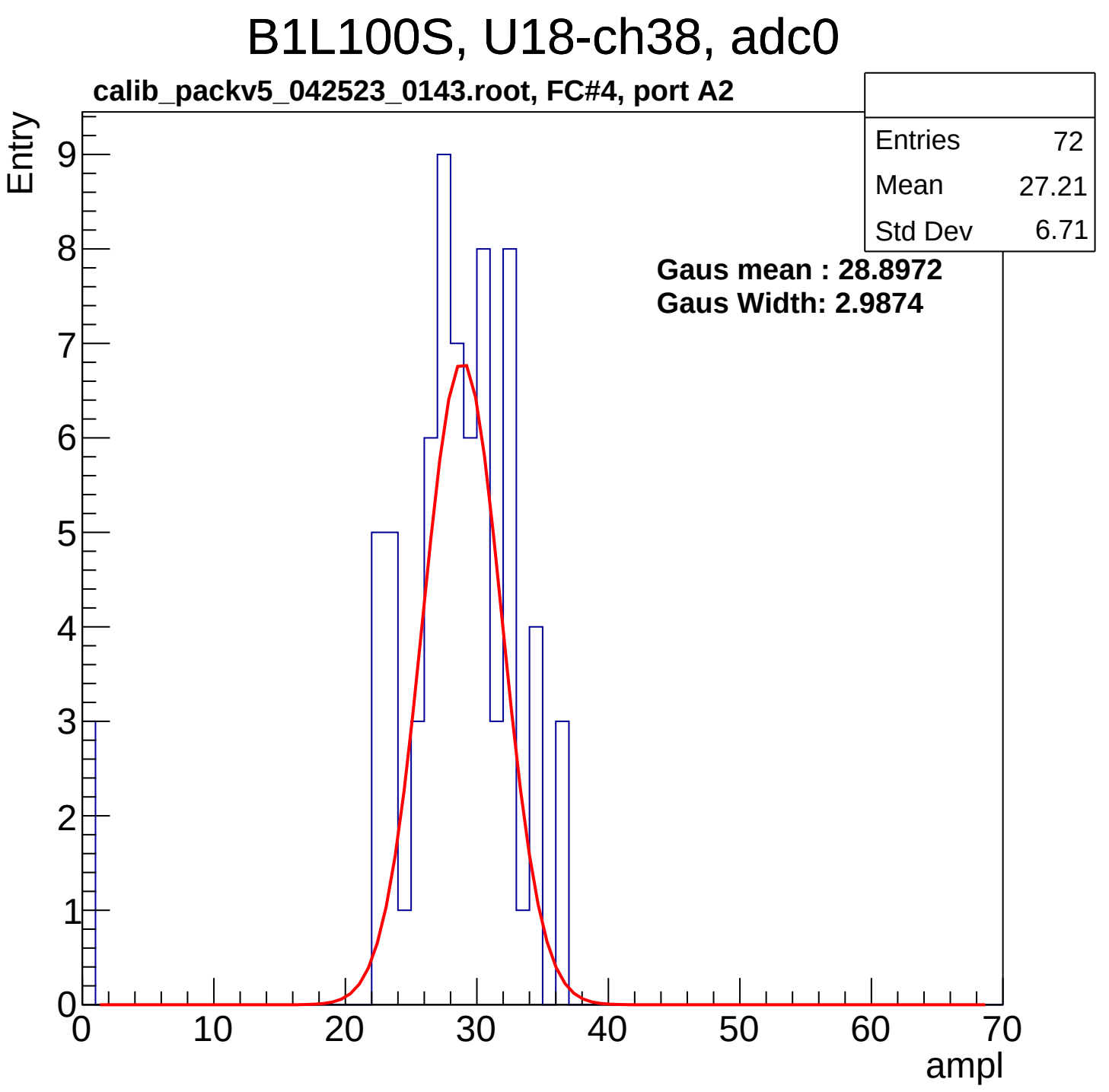

B1L100S, U18-ch37, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 51.71
Std Dev 3.418
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

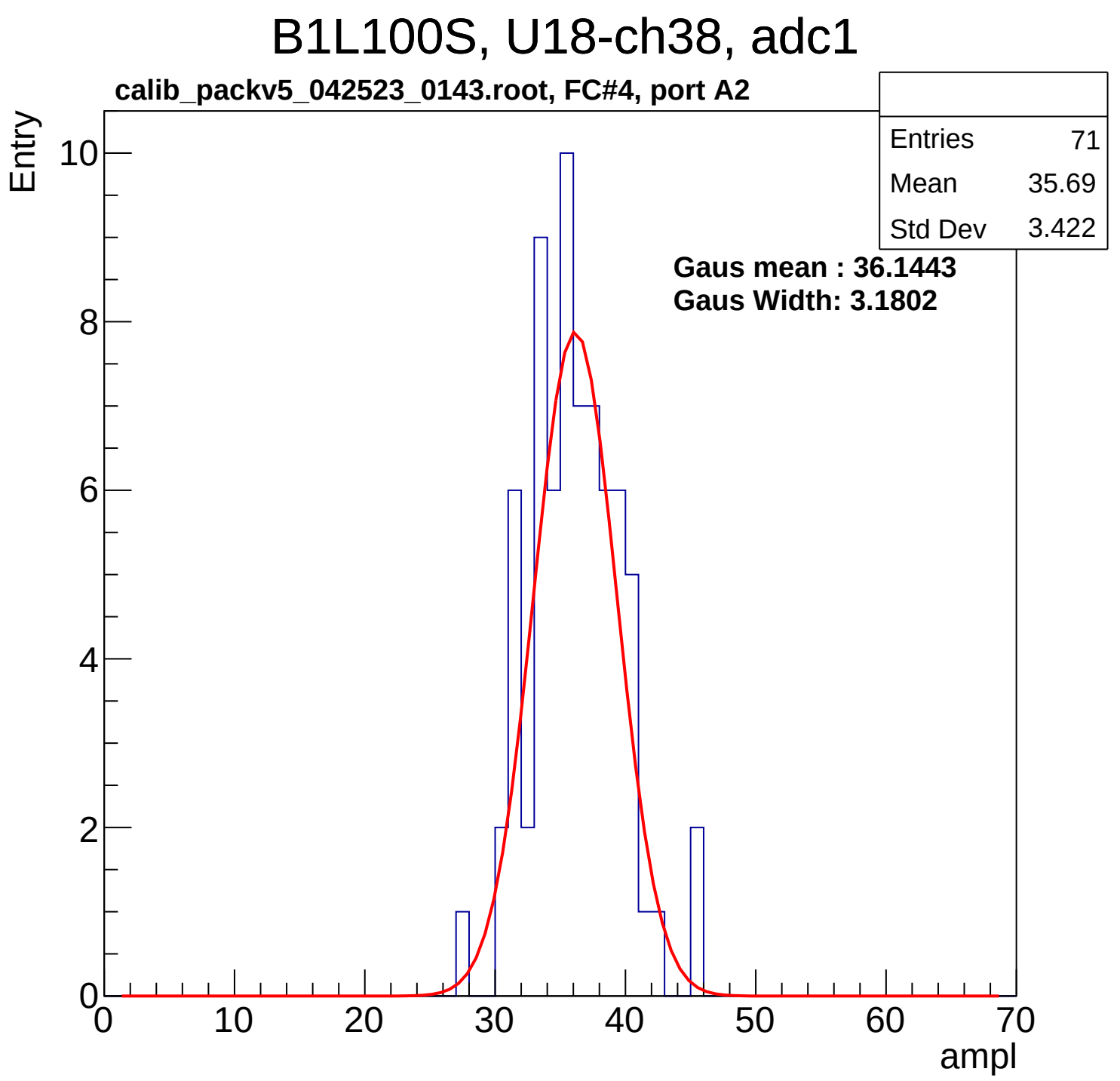

B1L100S, U18-ch37, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 57.39
Std Dev 3.575
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

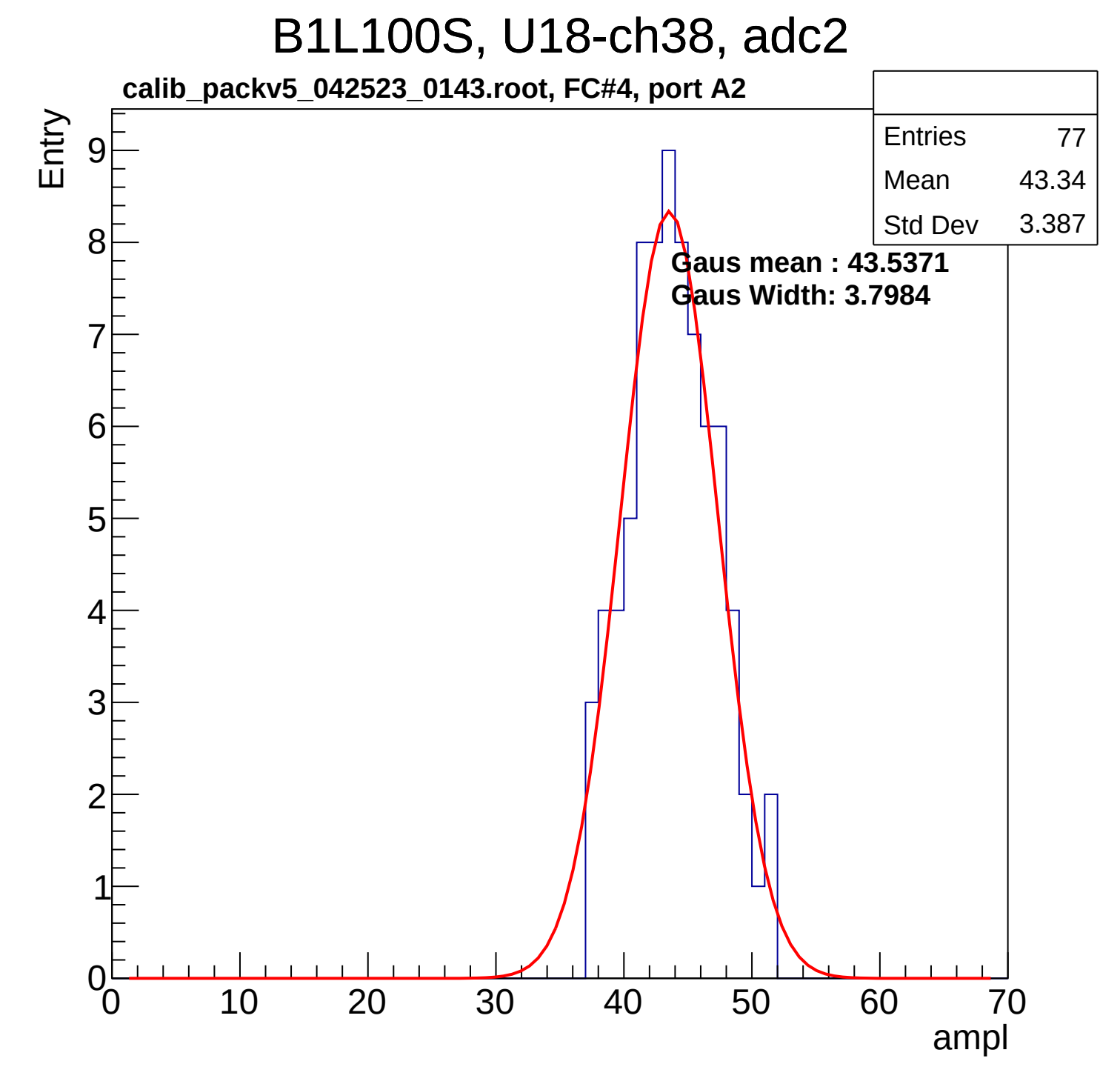

B1L100S, U18-ch37, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 26
Mean 58.31
Std Dev 11.82
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

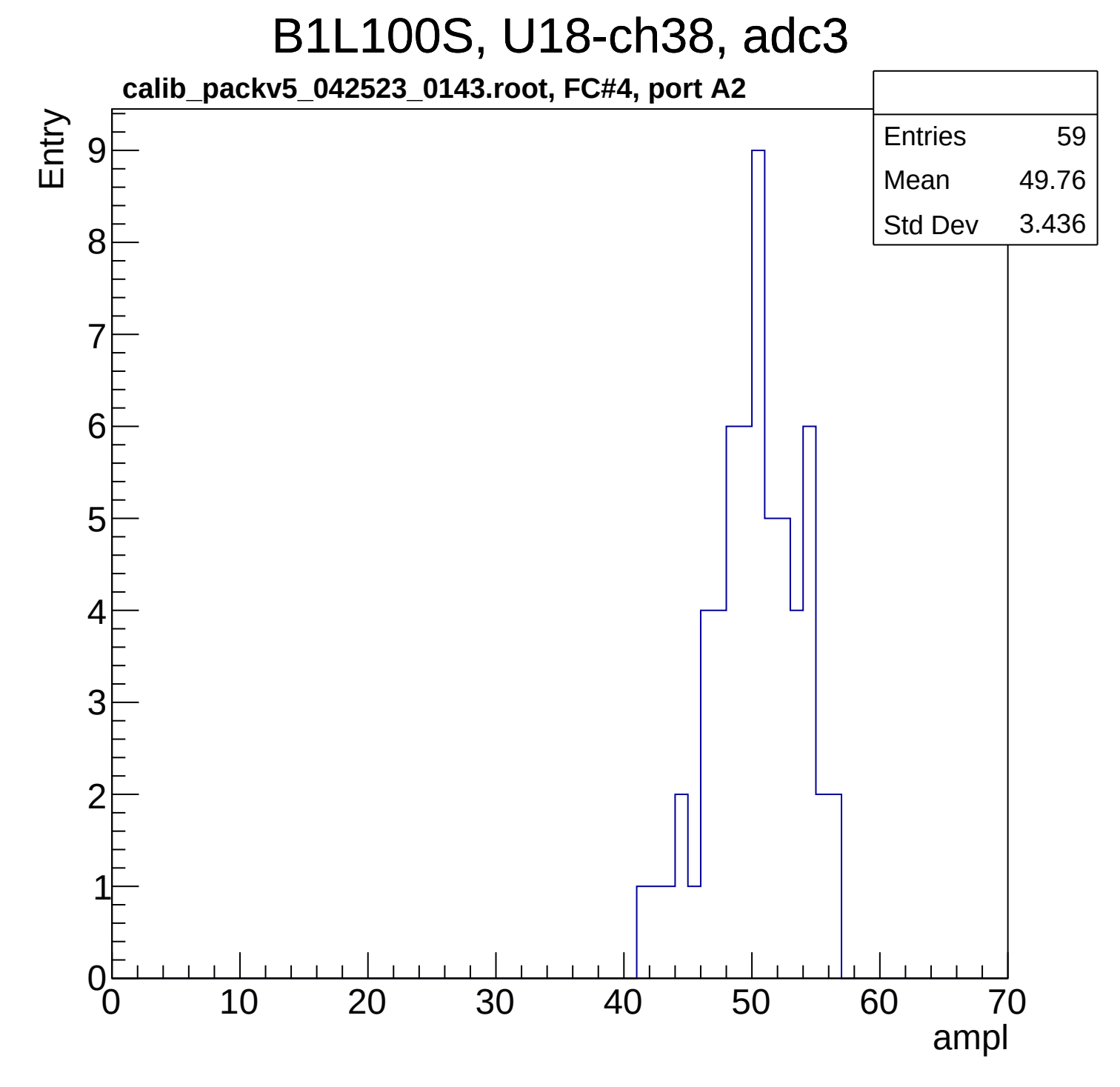

B1L100S, U18-ch37, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 62
Std Dev 0.8165
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

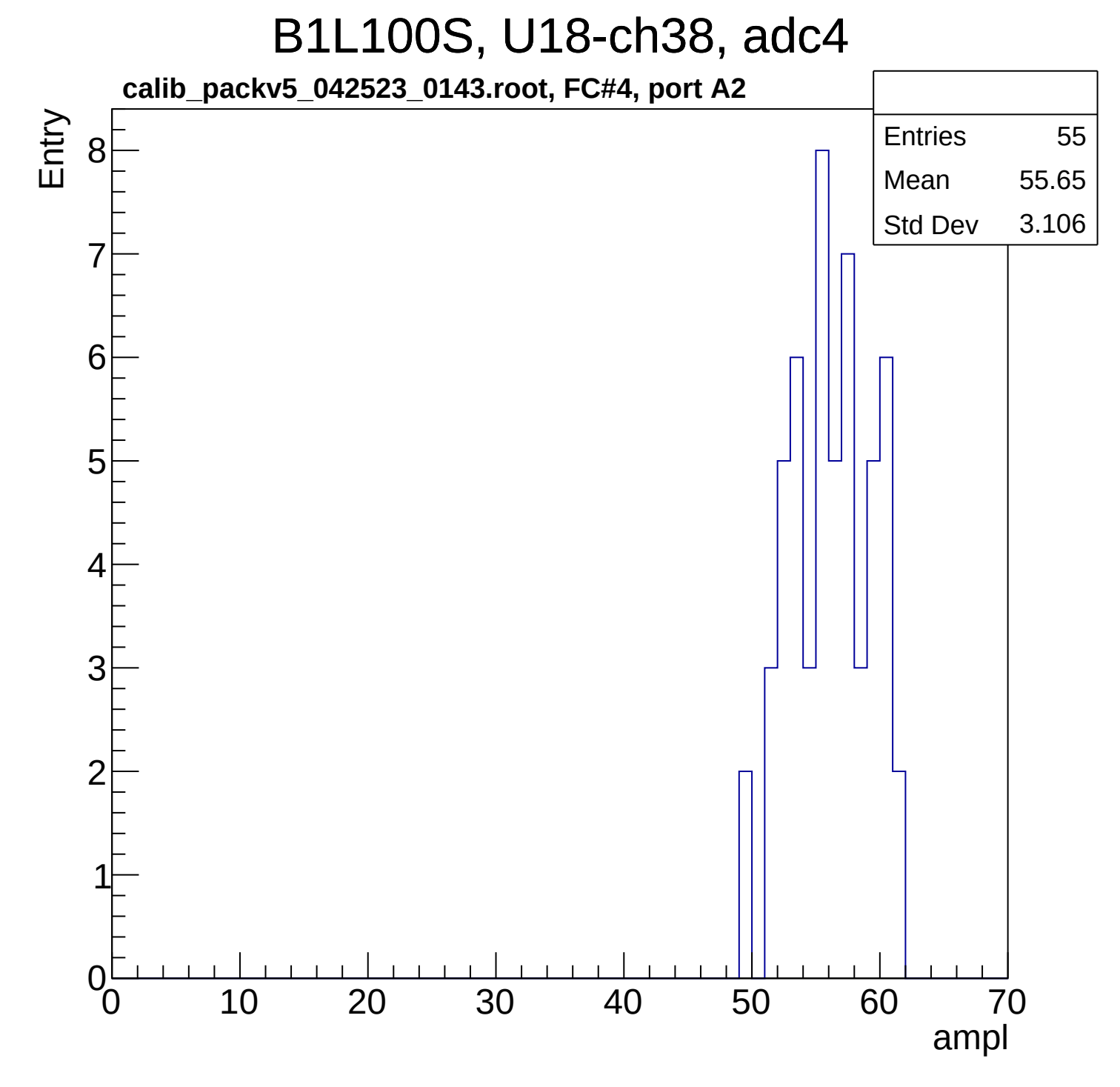

B1L100S, U18-ch37, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

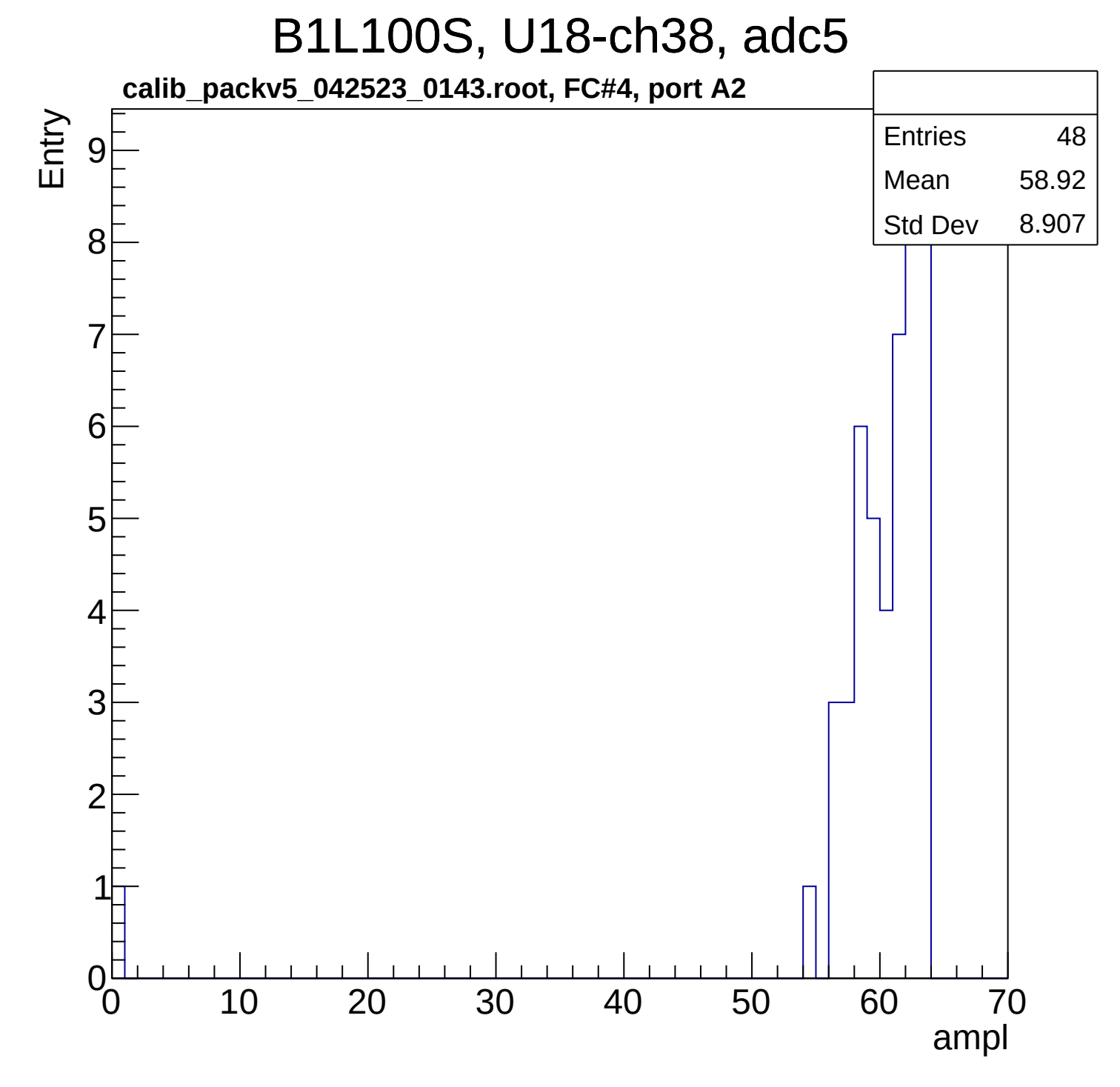

B1L100S, U18-ch38, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 27.21
Std Dev 6.71
Gaus mean : 28.8972
Gaus Width: 2.9874
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

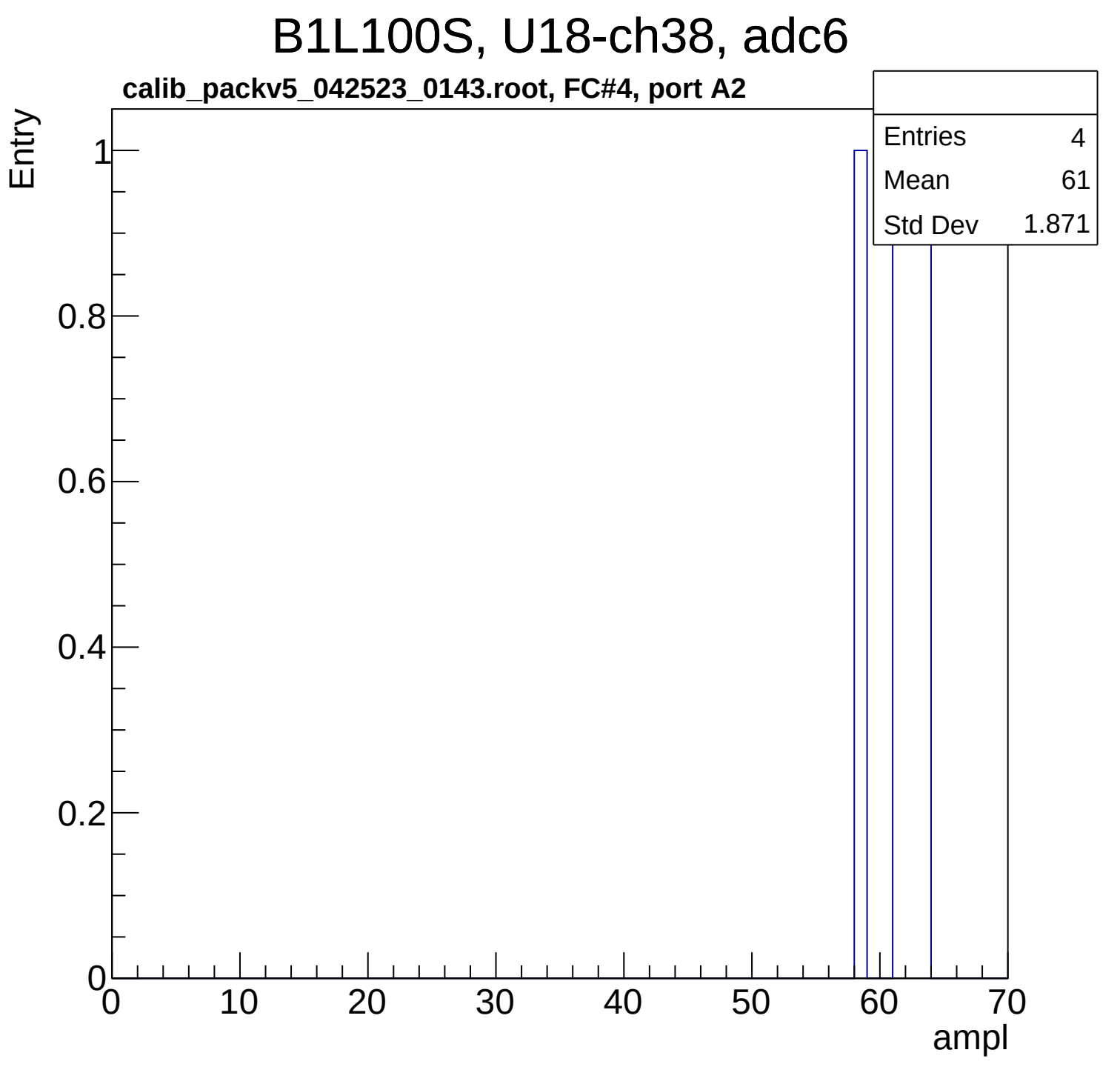

B1L100S, U18-ch38, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 35.69
Std Dev 3.422
Gaus mean : 36.1443
Gaus Width: 3.1802
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

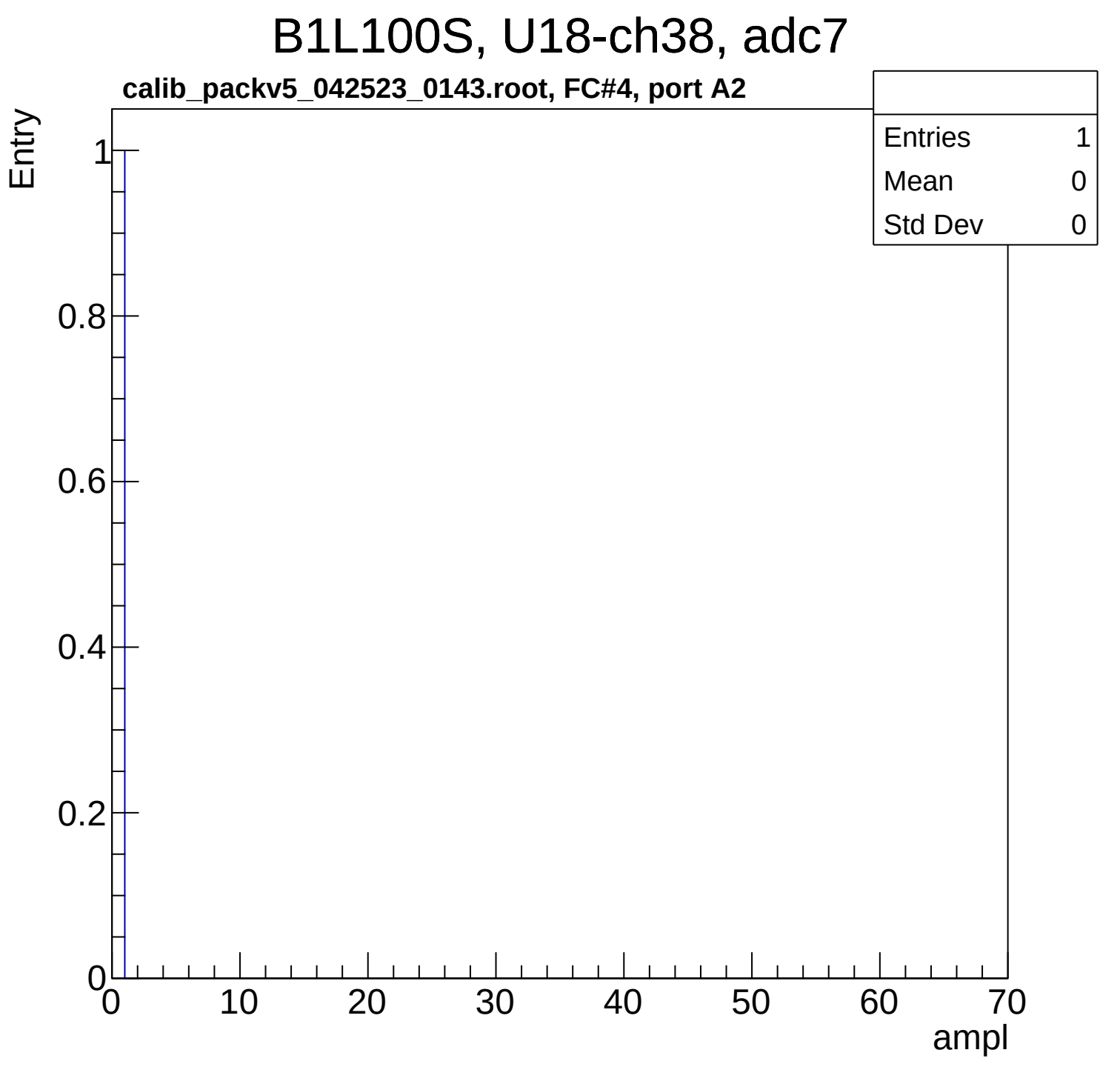

B1L100S, U18-ch38, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 43.34
Std Dev 3.387
Gaus mean : 43.5371
Gaus Width: 3.7984
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

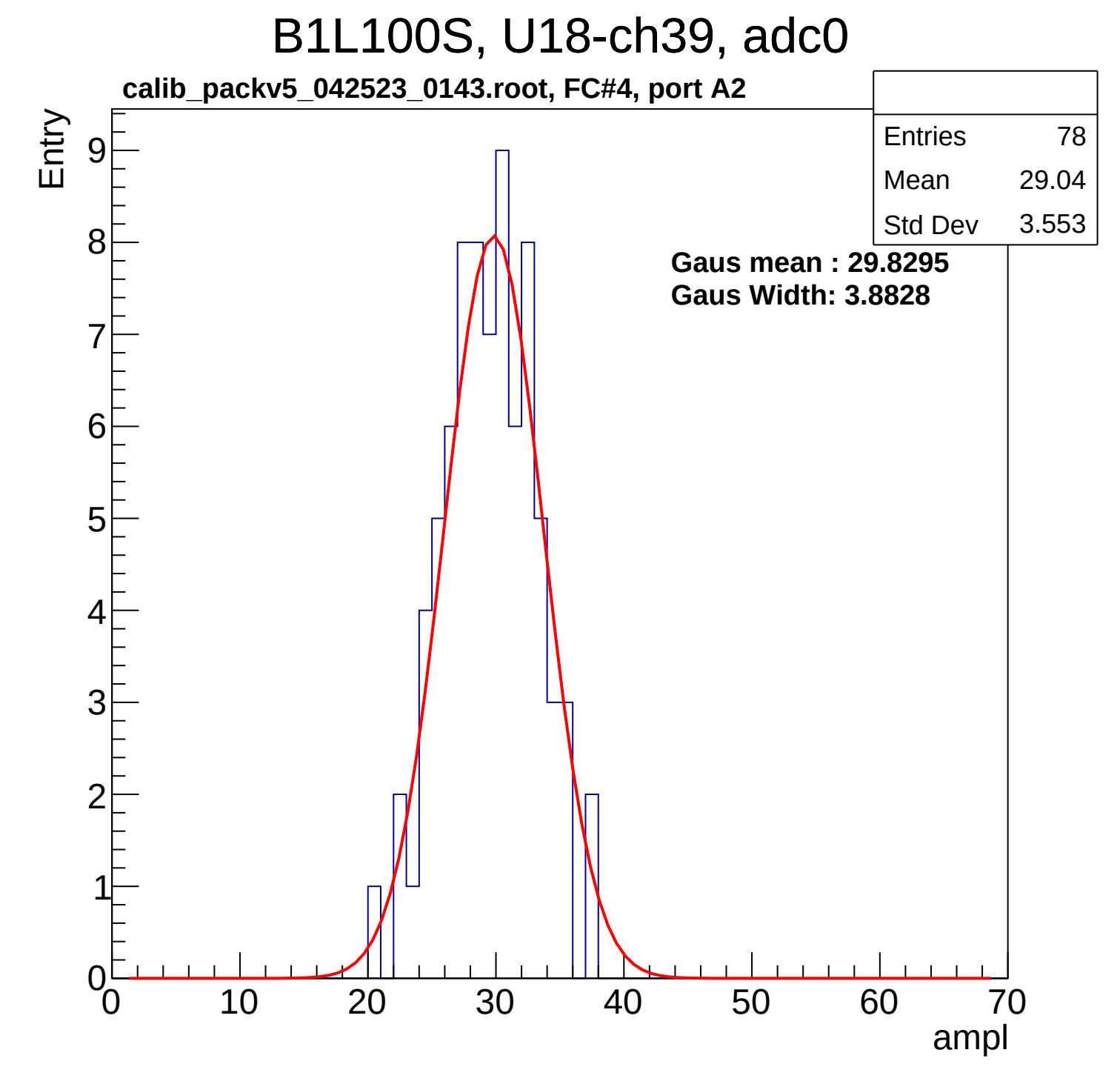

B1L100S, U18-ch38, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 49.76
Std Dev 3.436
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

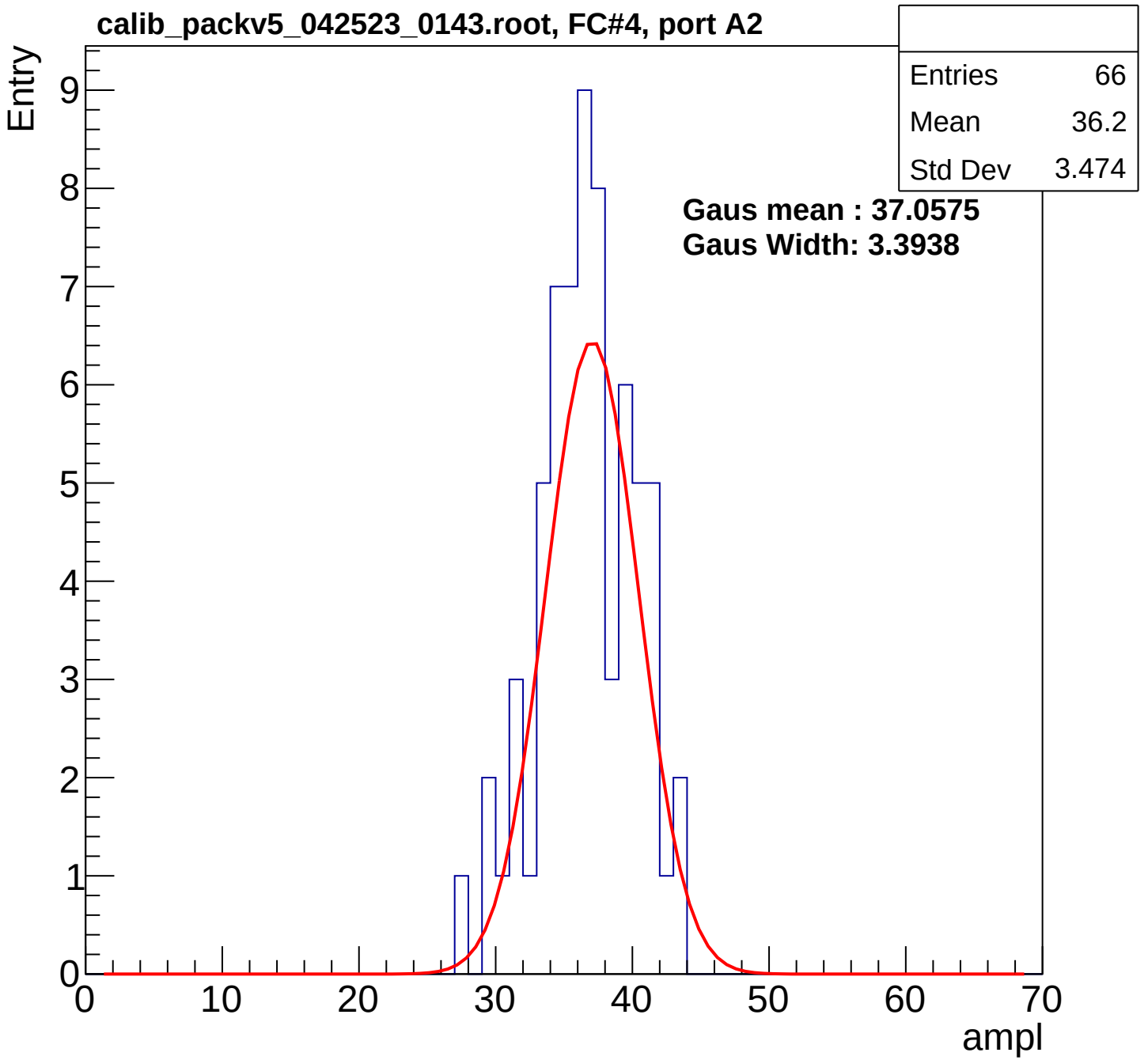

B1L100S, U18-ch38, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 55.65
Std Dev 3.106
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

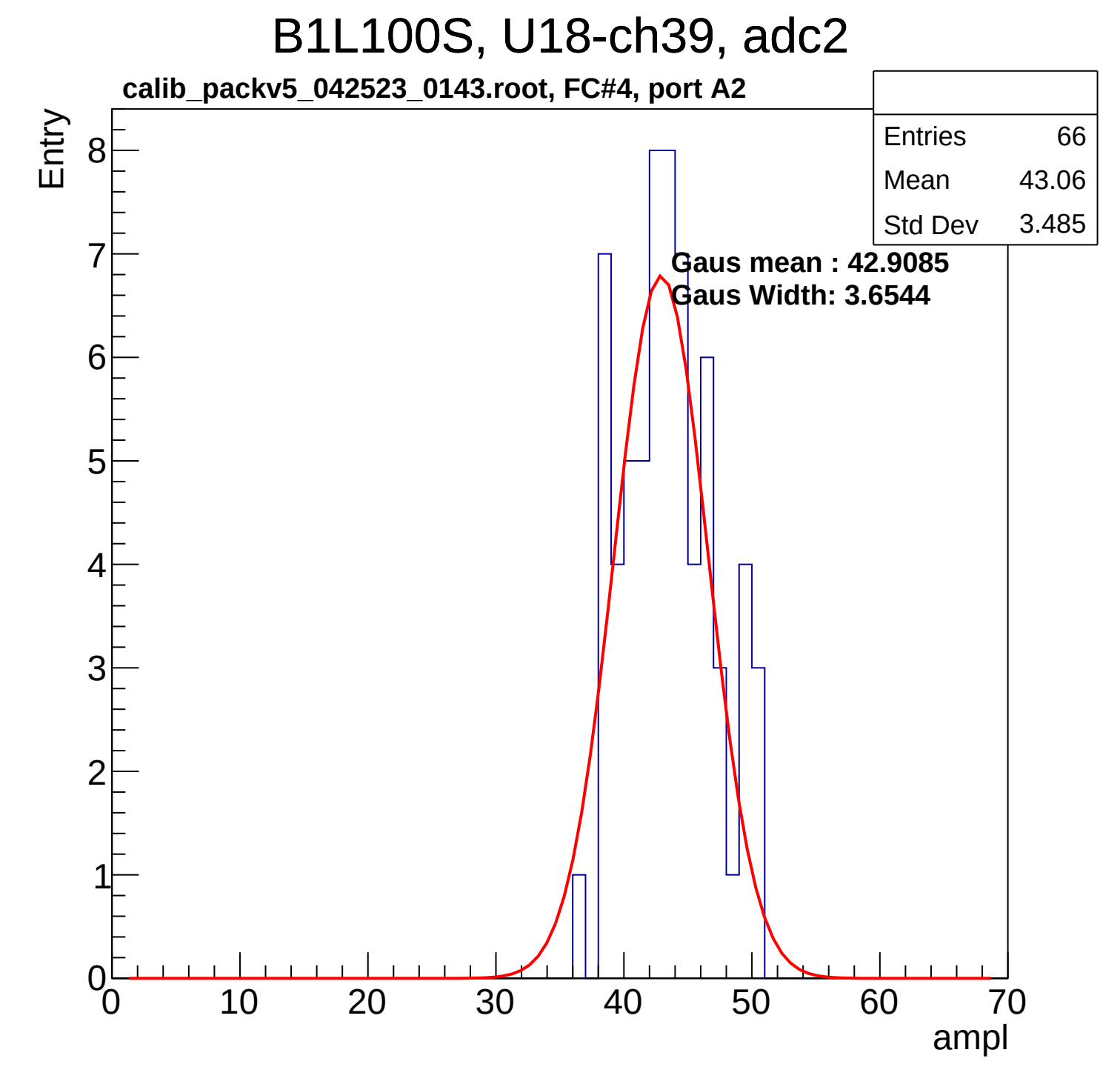

B1L100S, U18-ch38, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 58.92
Std Dev 8.907
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

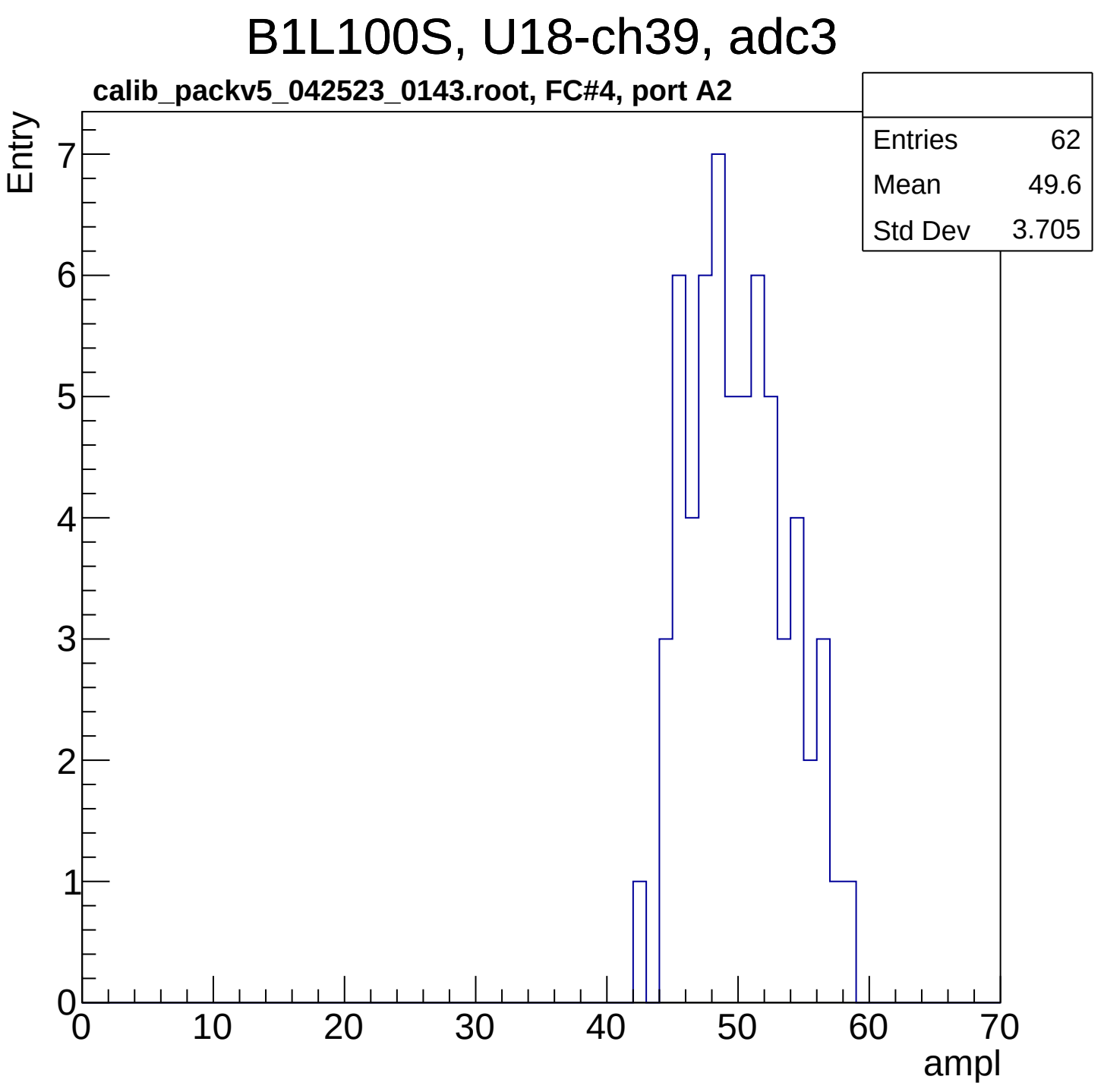

B1L100S, U18-ch38, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 61
Std Dev 1.871
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

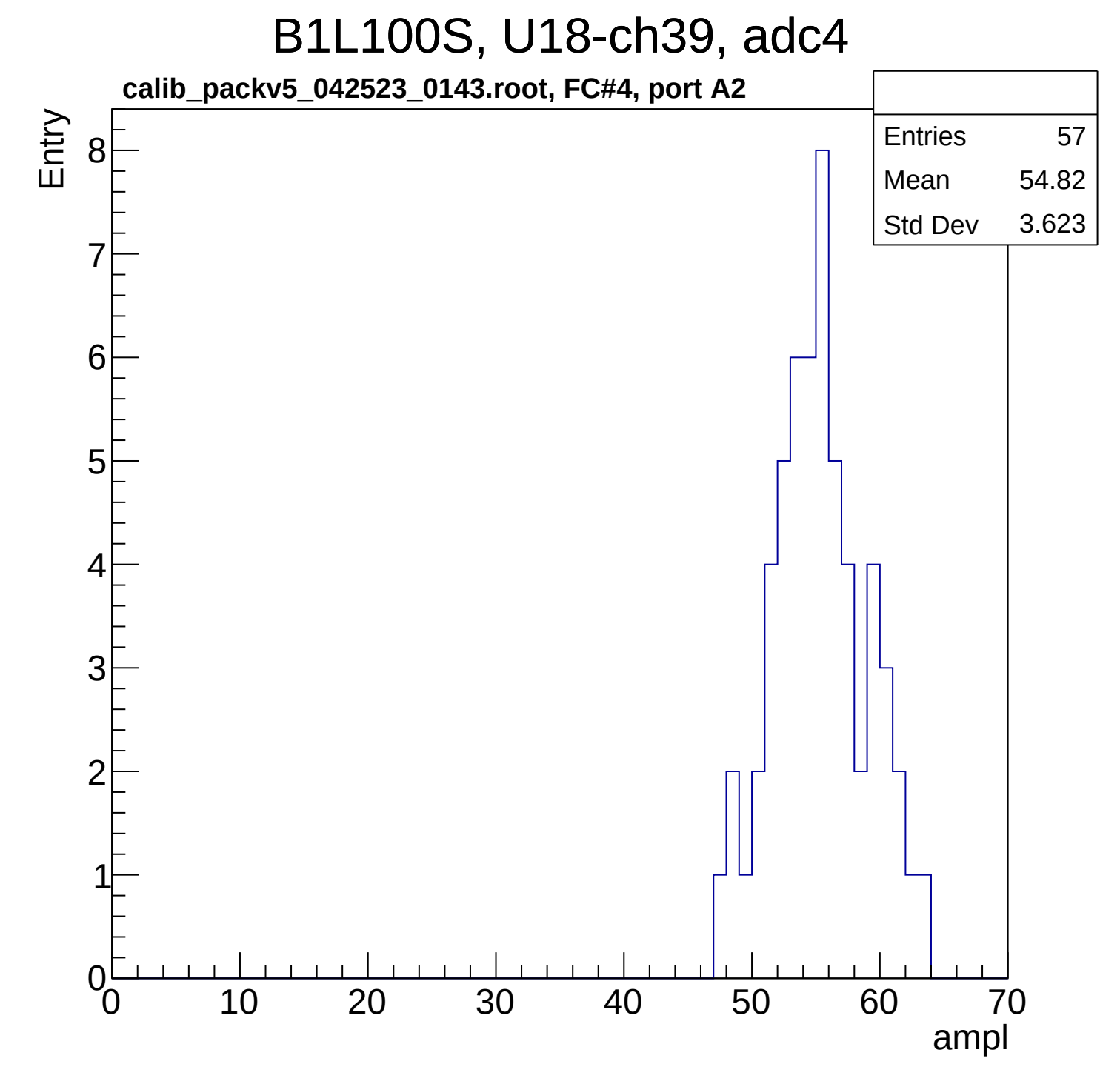

B1L100S, U18-ch38, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

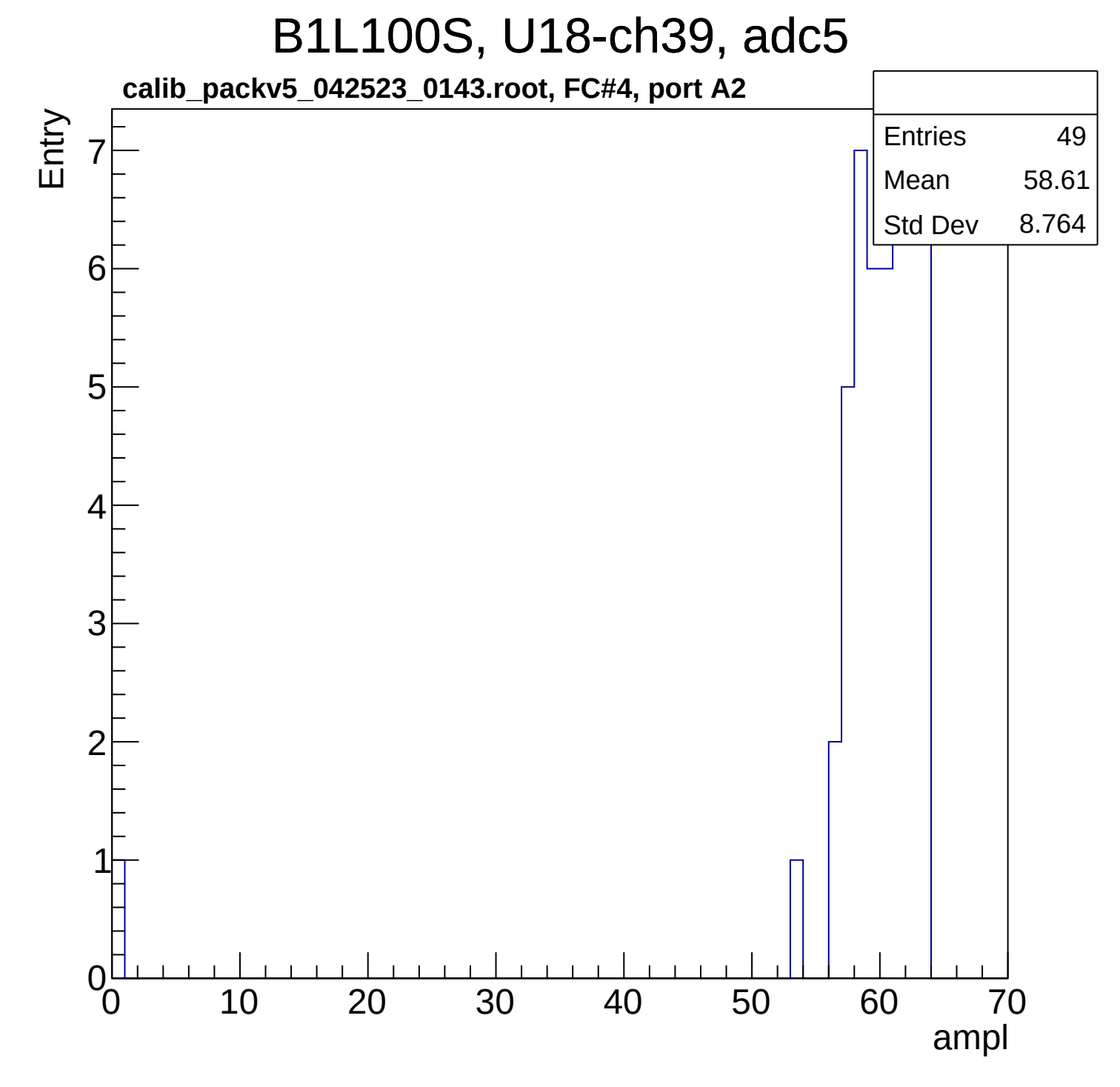

B1L100S, U18-ch39, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 29.04
Std Dev 3.553
Gaus mean : 29.8295
Gaus Width: 3.8828
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

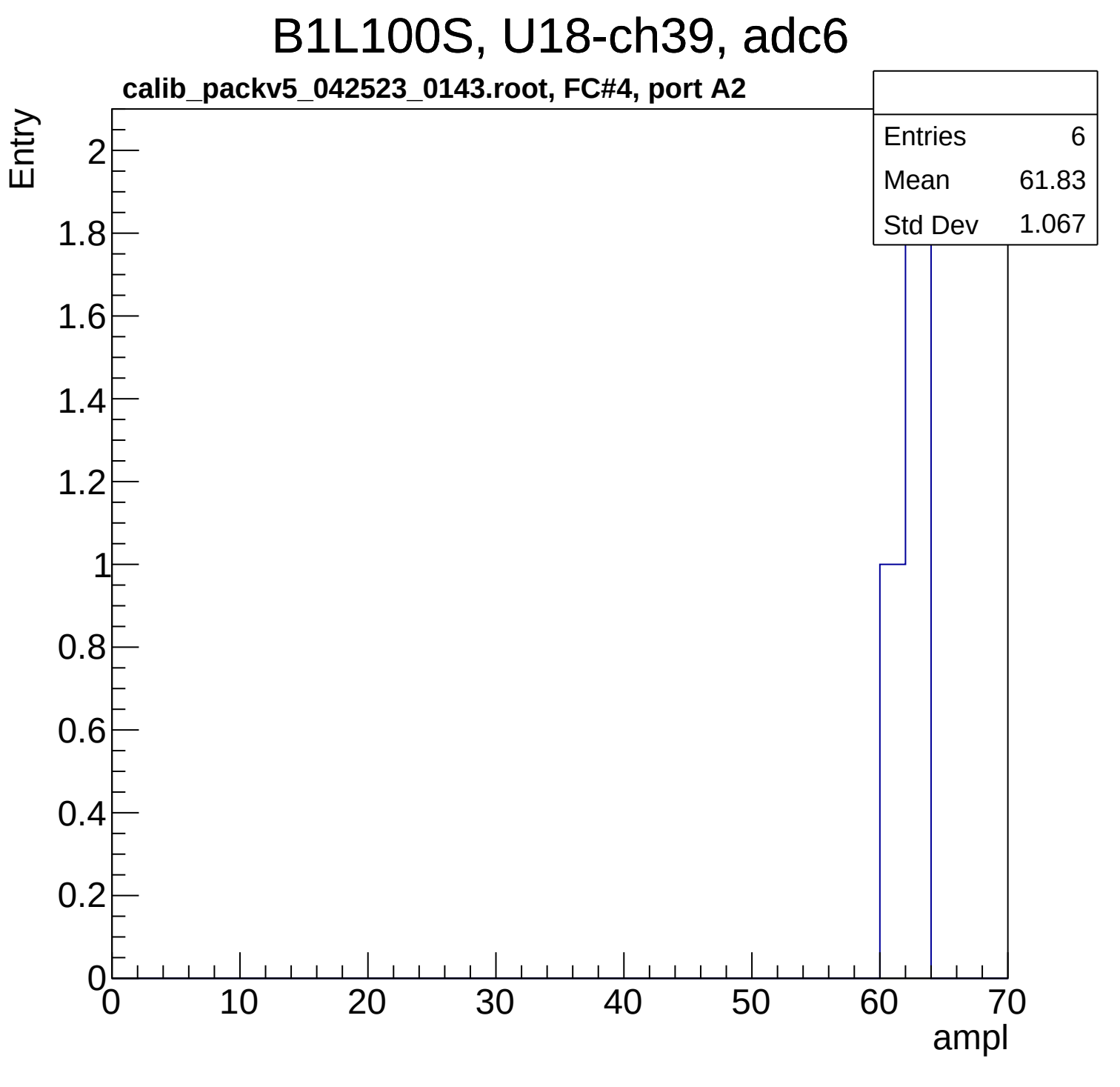

B1L100S, U18-ch39, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 36.2
Std Dev 3.474
Gaus mean : 37.0575
Gaus Width: 3.3938
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

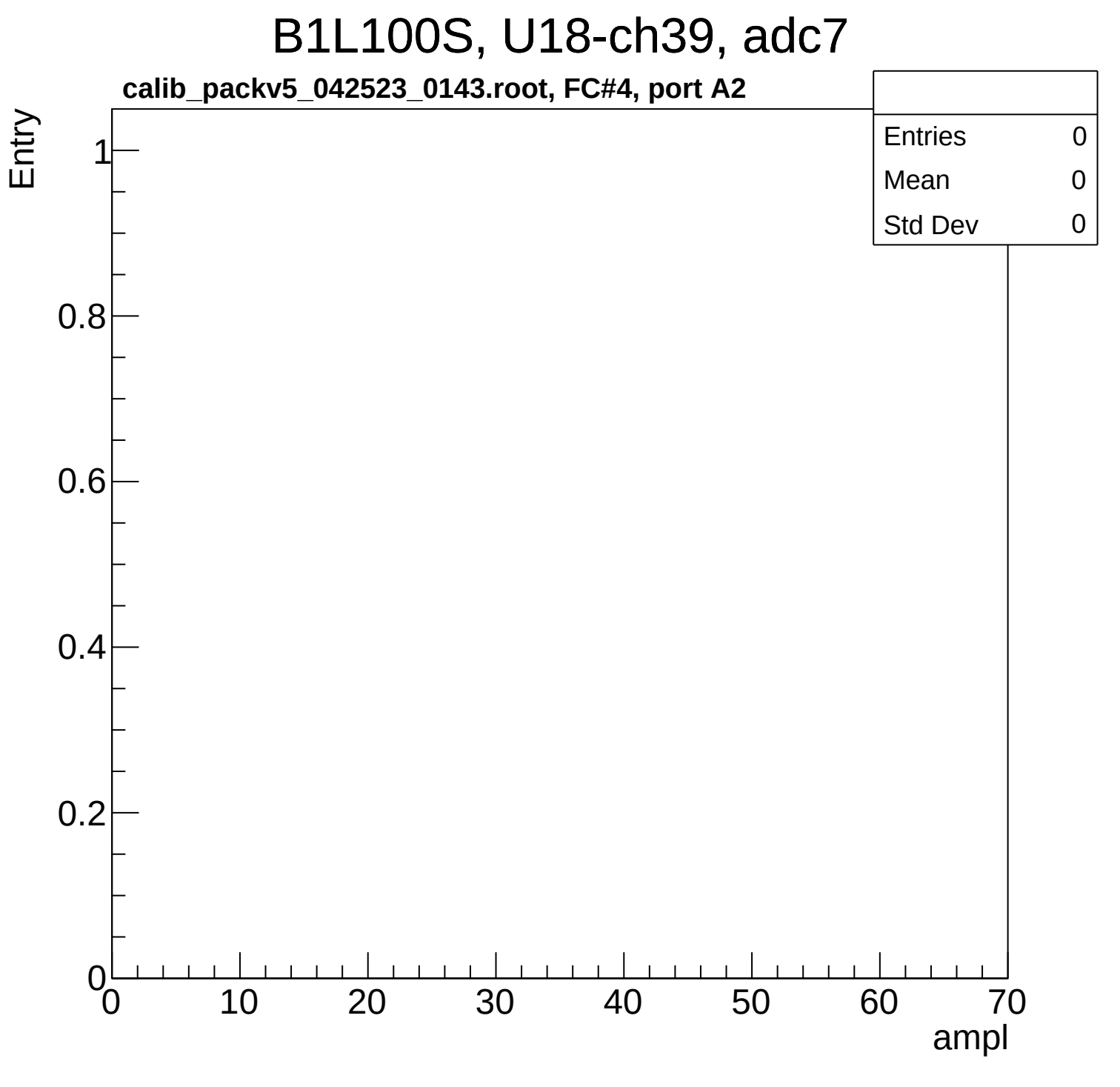

B1L100S, U18-ch39, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 43.06
Std Dev 3.485
Gaus mean : 42.9085
Gaus Width: 3.6544
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

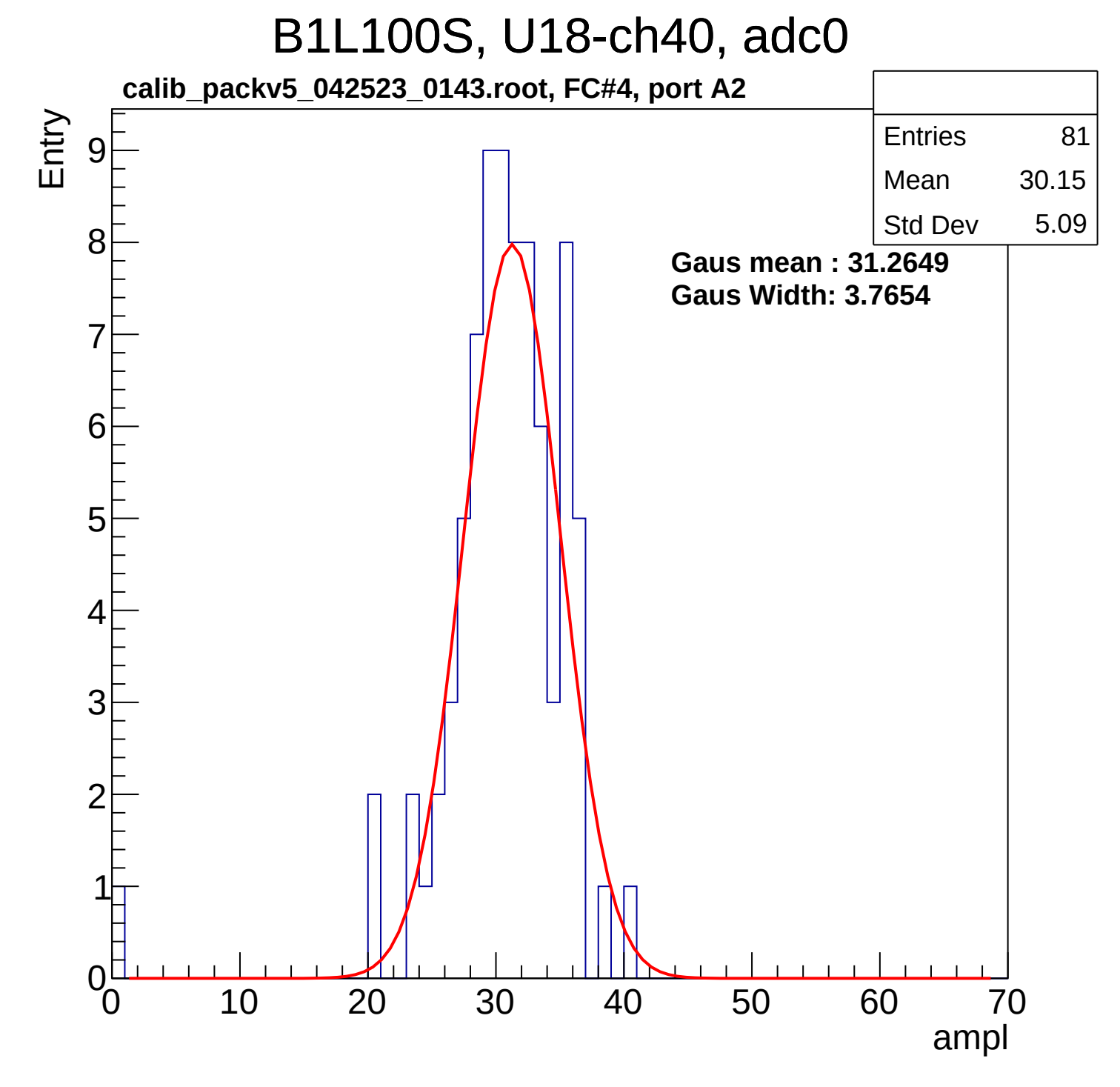

B1L100S, U18-ch39, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 49.6
Std Dev 3.705
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

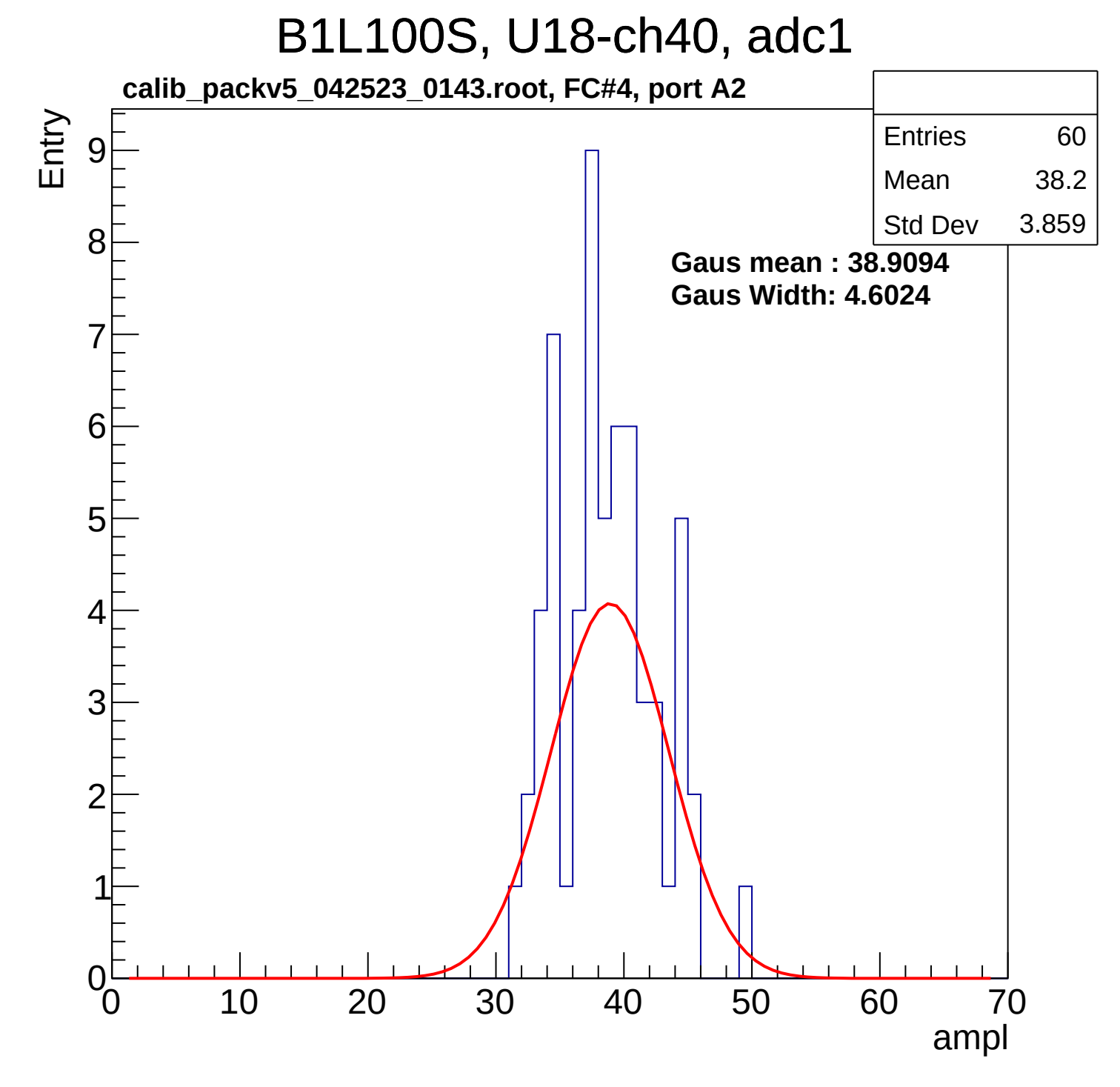

B1L100S, U18-ch39, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 54.82
Std Dev 3.623
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

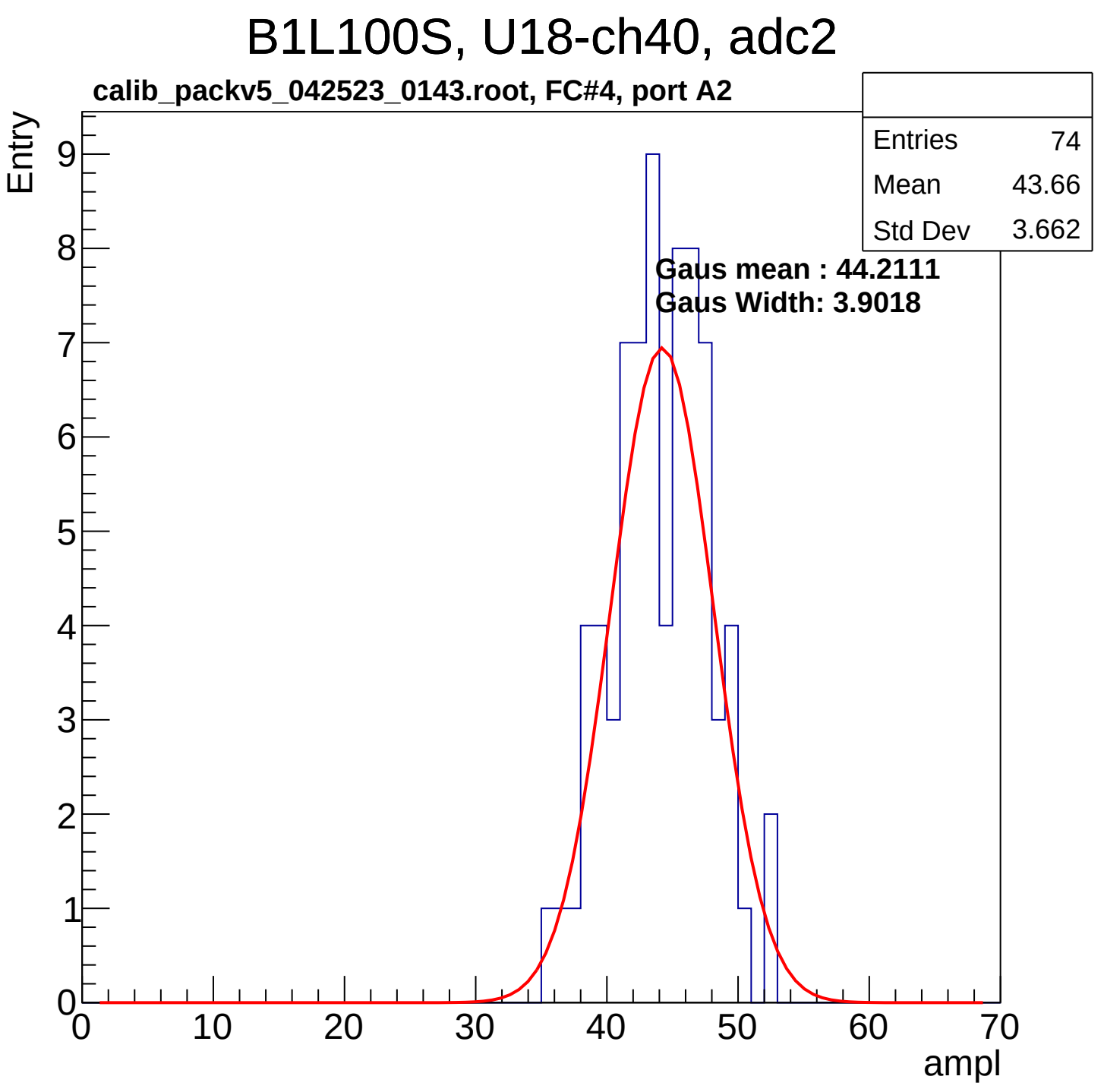

B1L100S, U18-ch39, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 58.61
Std Dev 8.764
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

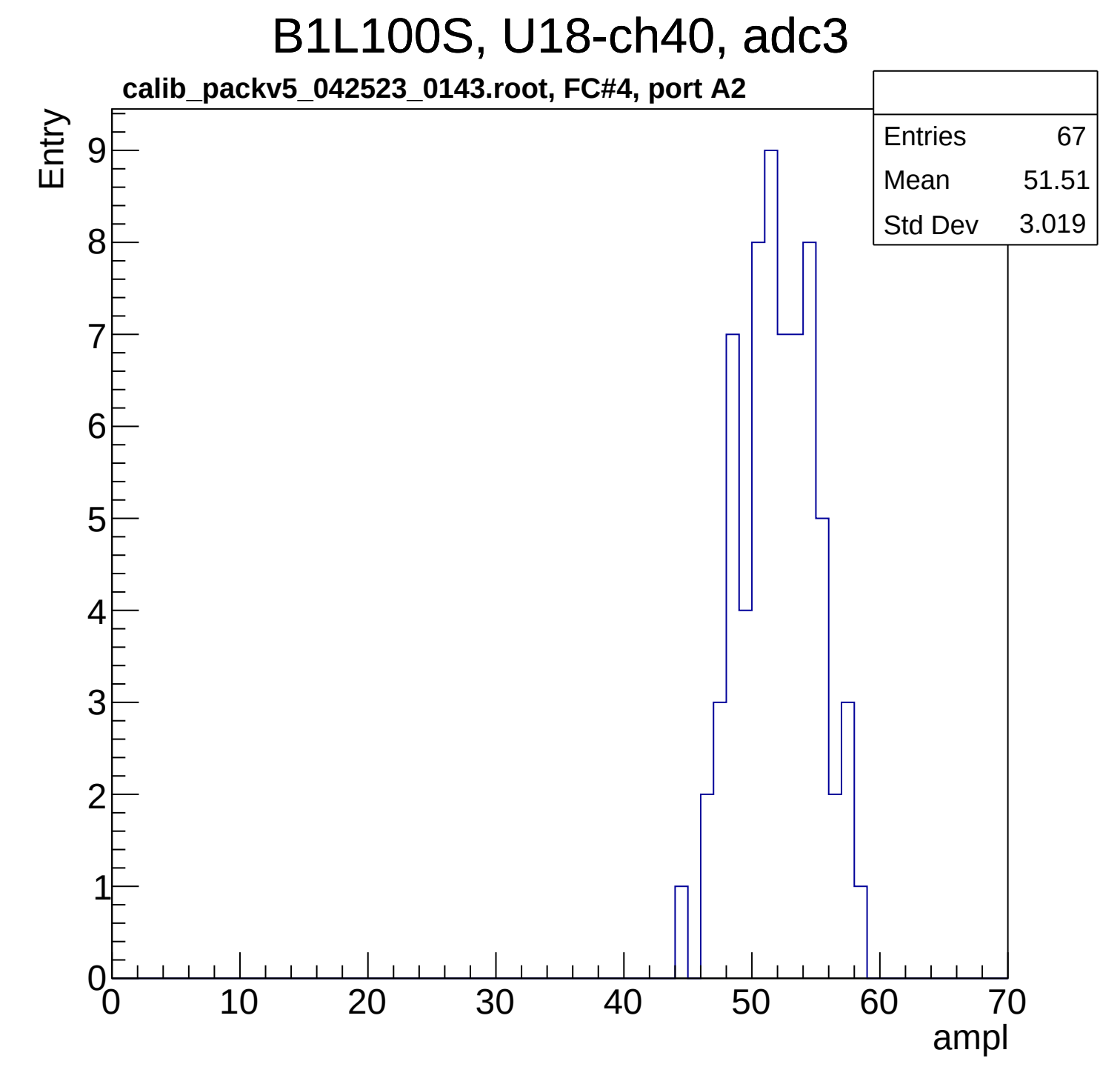

B1L100S, U18-ch39, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 61.83
Std Dev 1.067
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

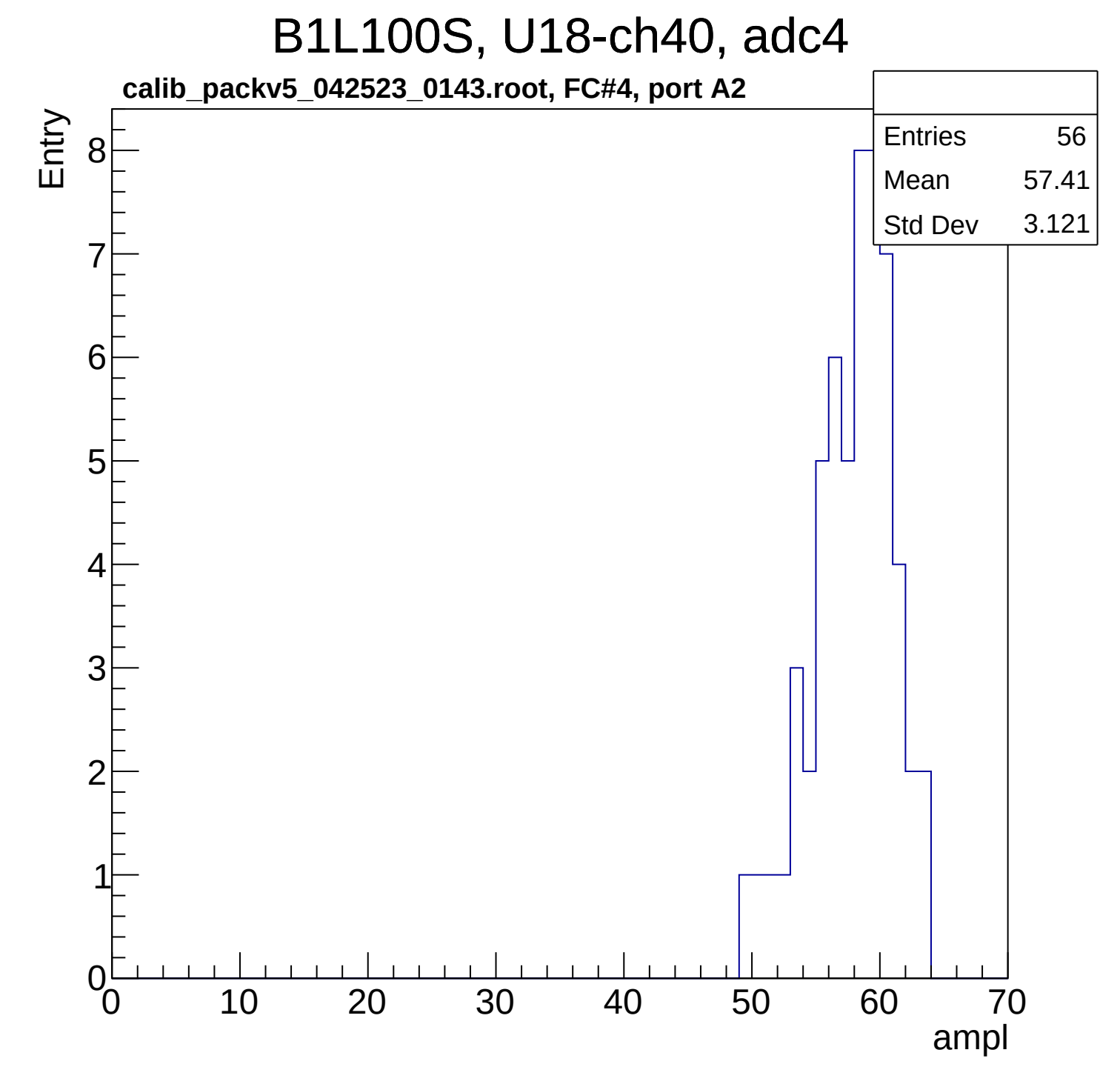

B1L100S, U18-ch39, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

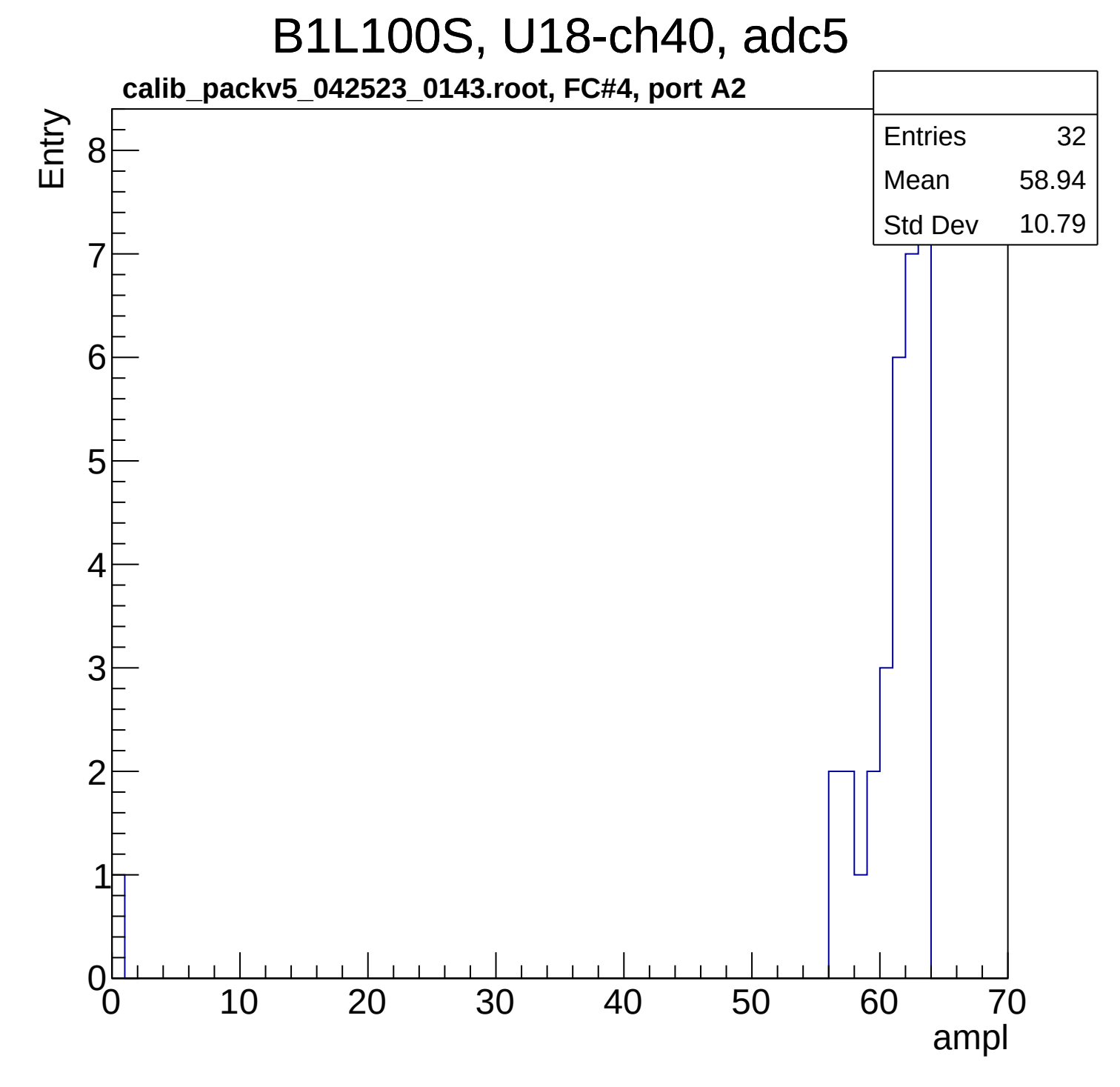

B1L100S, U18-ch40, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 30.15
Std Dev 5.09
Gaus mean : 31.2649
Gaus Width: 3.7654
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

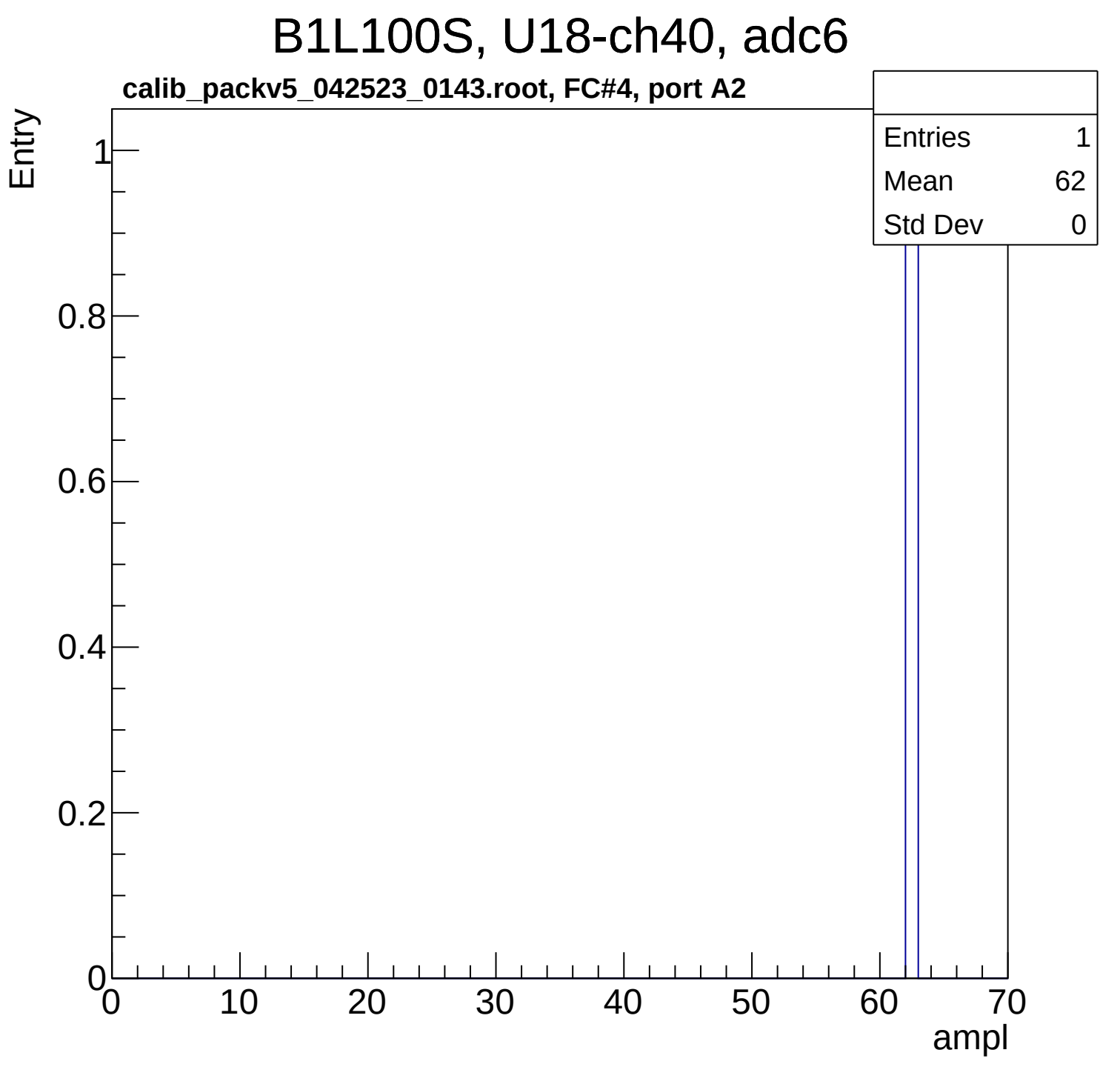

B1L100S, U18-ch40, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 38.2
Std Dev 3.859
Gaus mean : 38.9094
Gaus Width: 4.6024
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

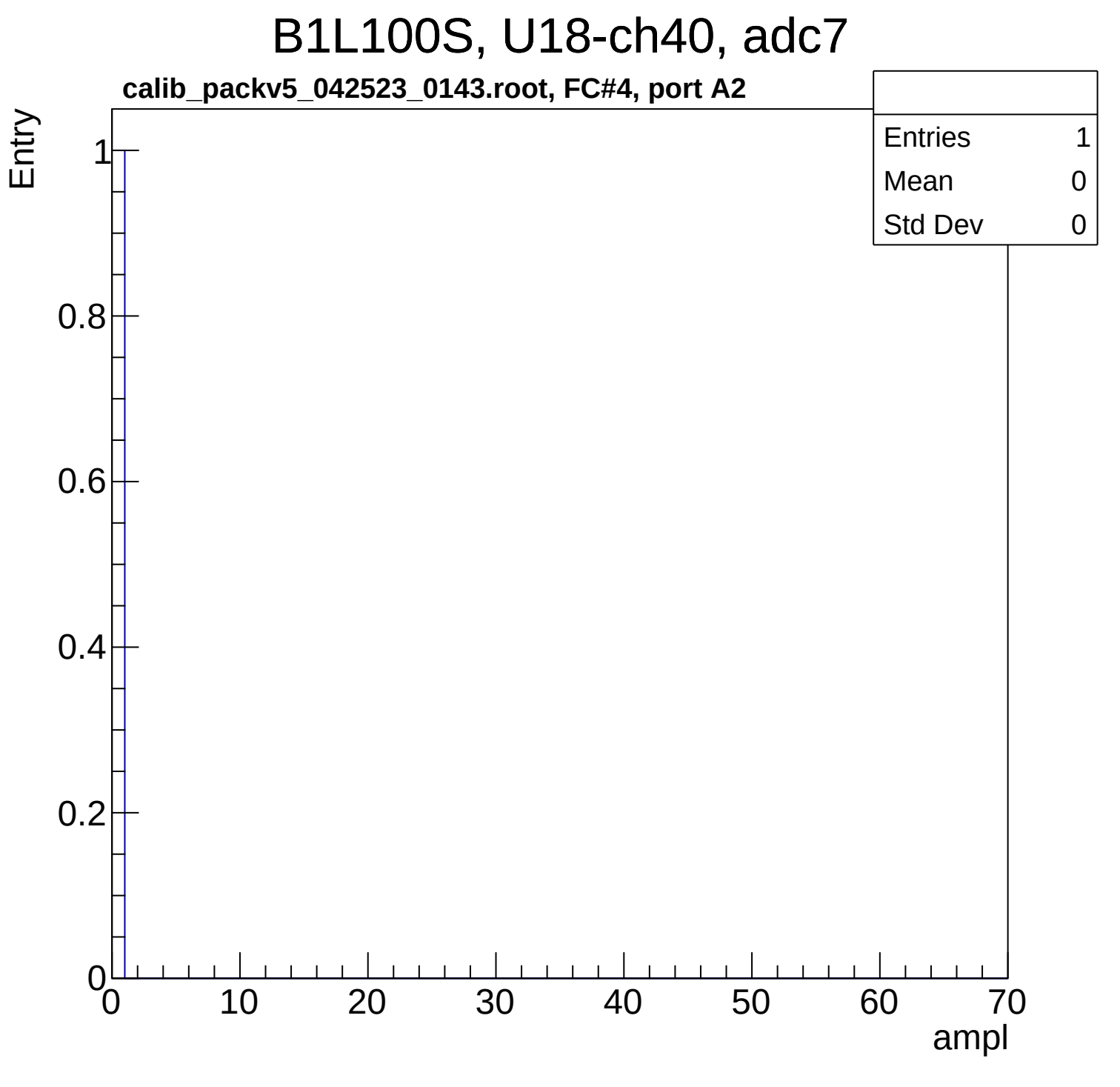

B1L100S, U18-ch40, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 43.66
Std Dev 3.662
Gaus mean : 44.2111
Gaus Width: 3.9018
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

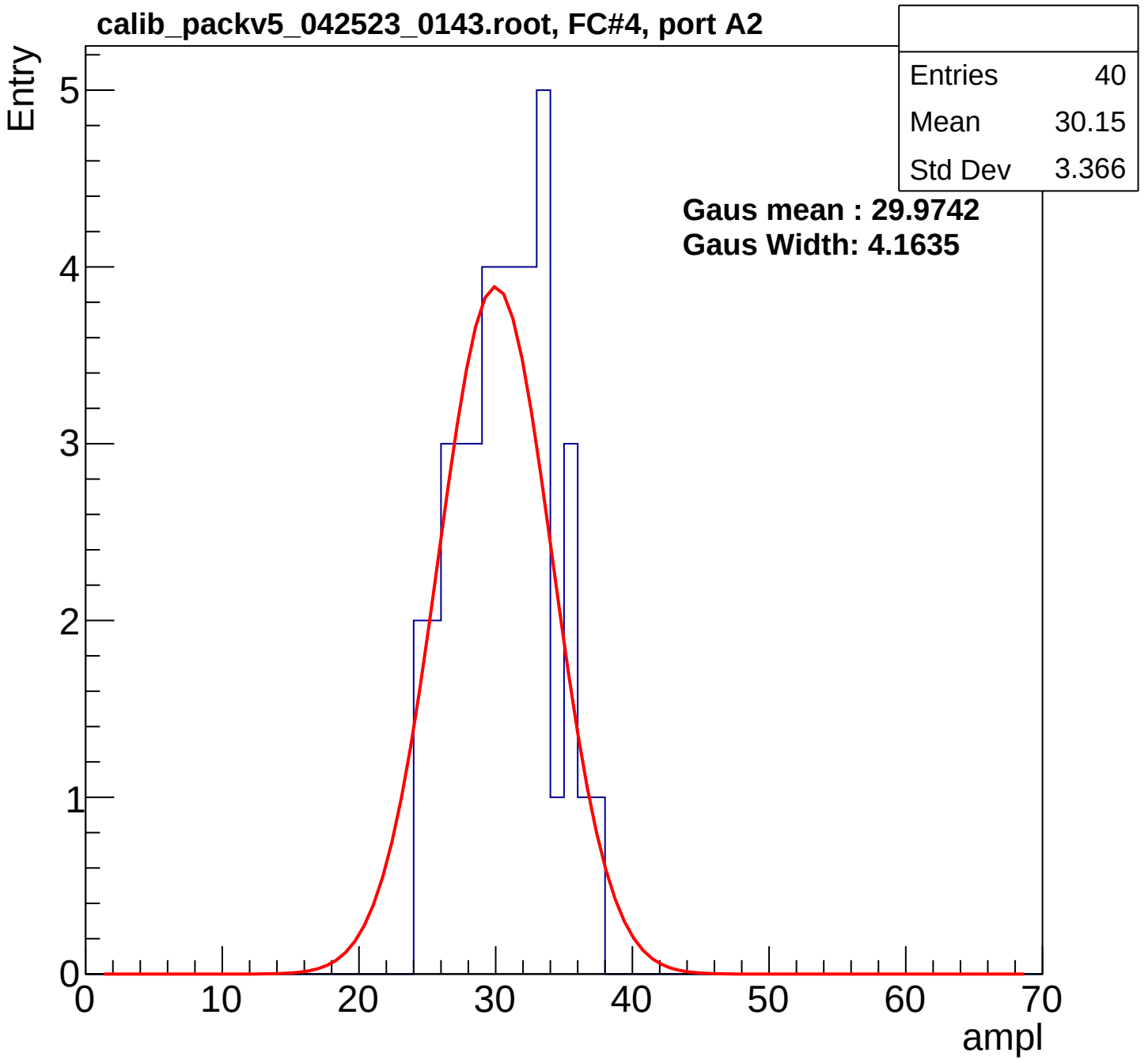

B1L100S, U18-ch40, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 51.51
Std Dev 3.019
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

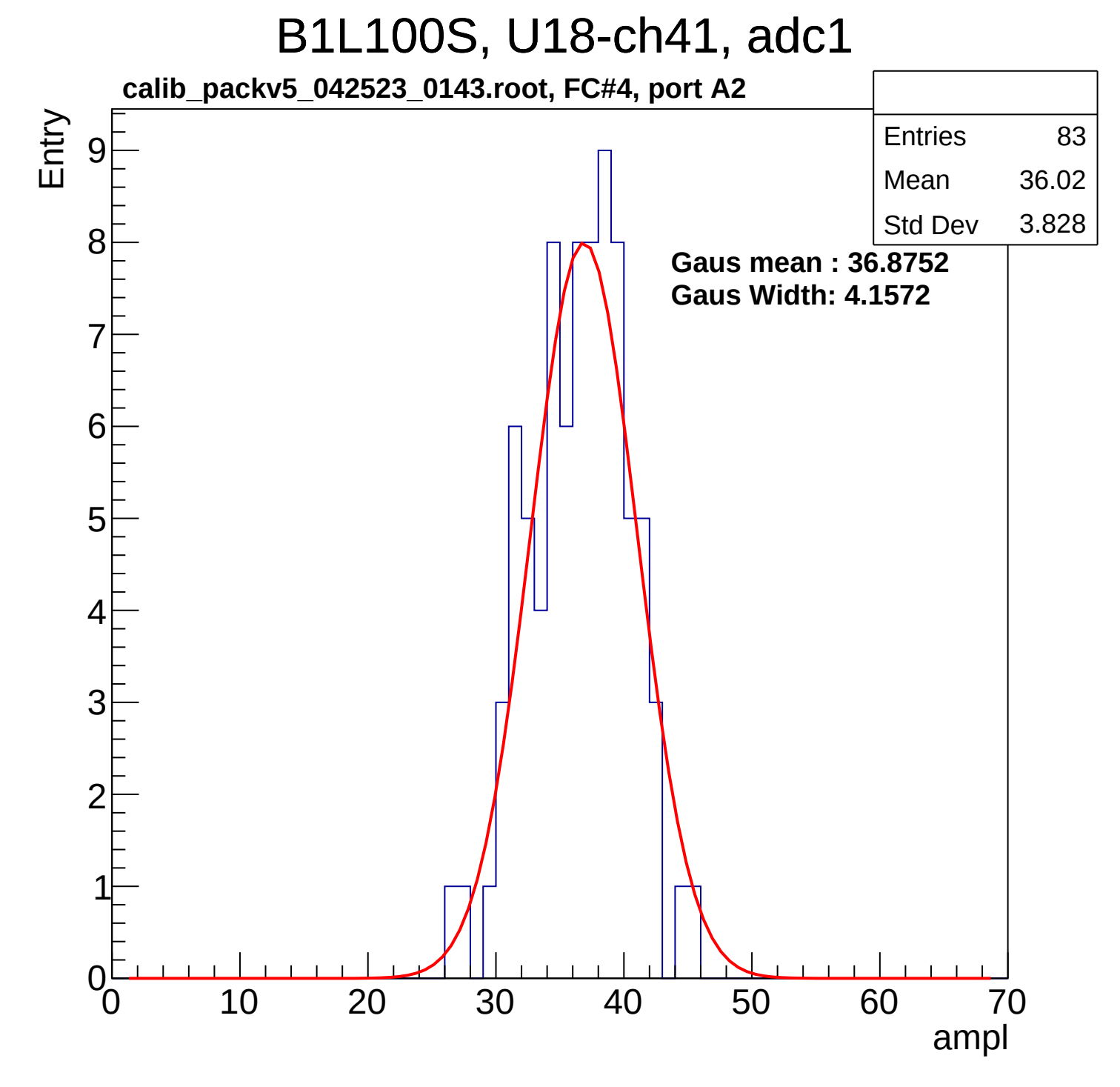

B1L100S, U18-ch40, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 57.41
Std Dev 3.121
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

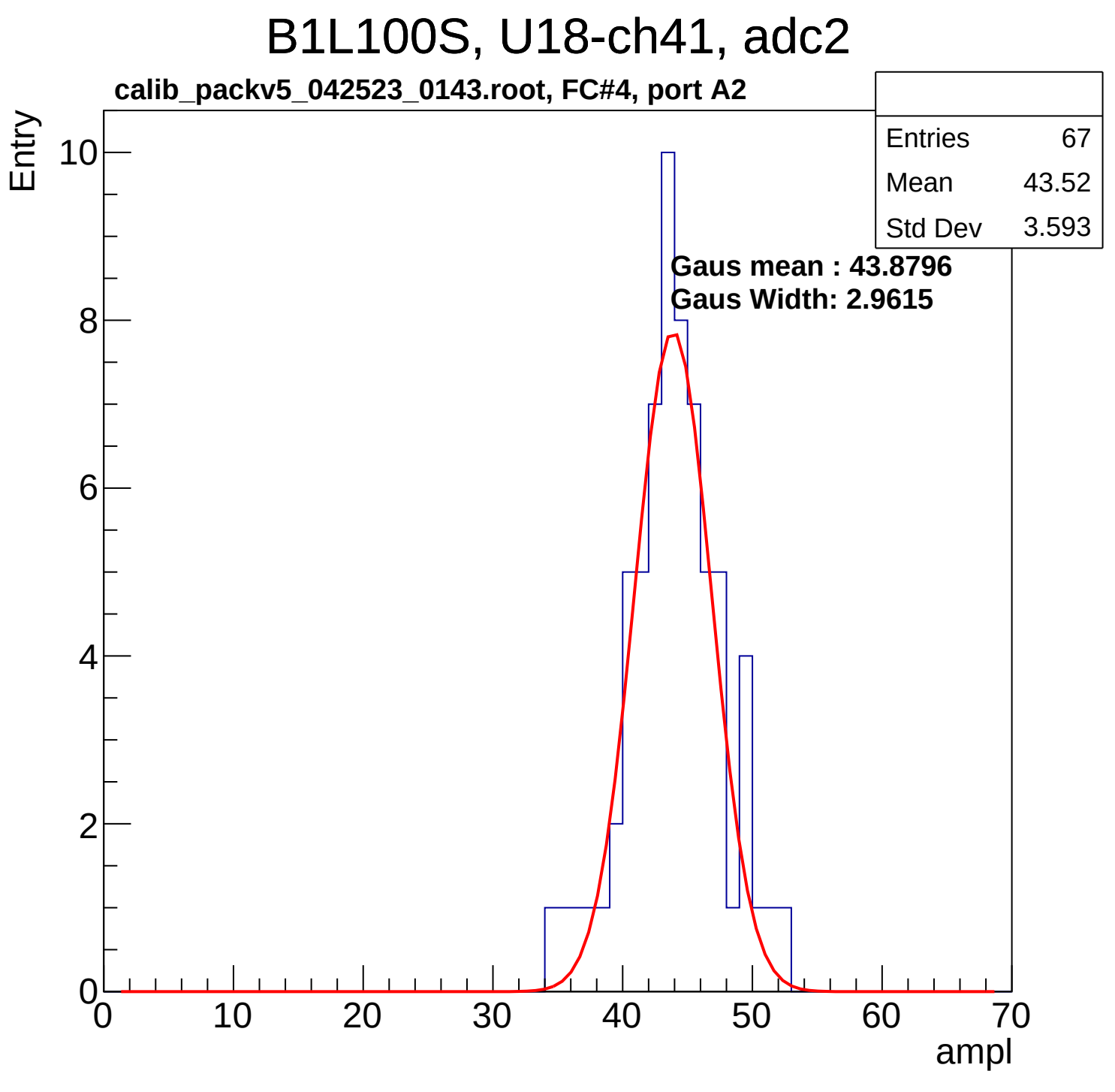

B1L100S, U18-ch40, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 32
Mean 58.94
Std Dev 10.79
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

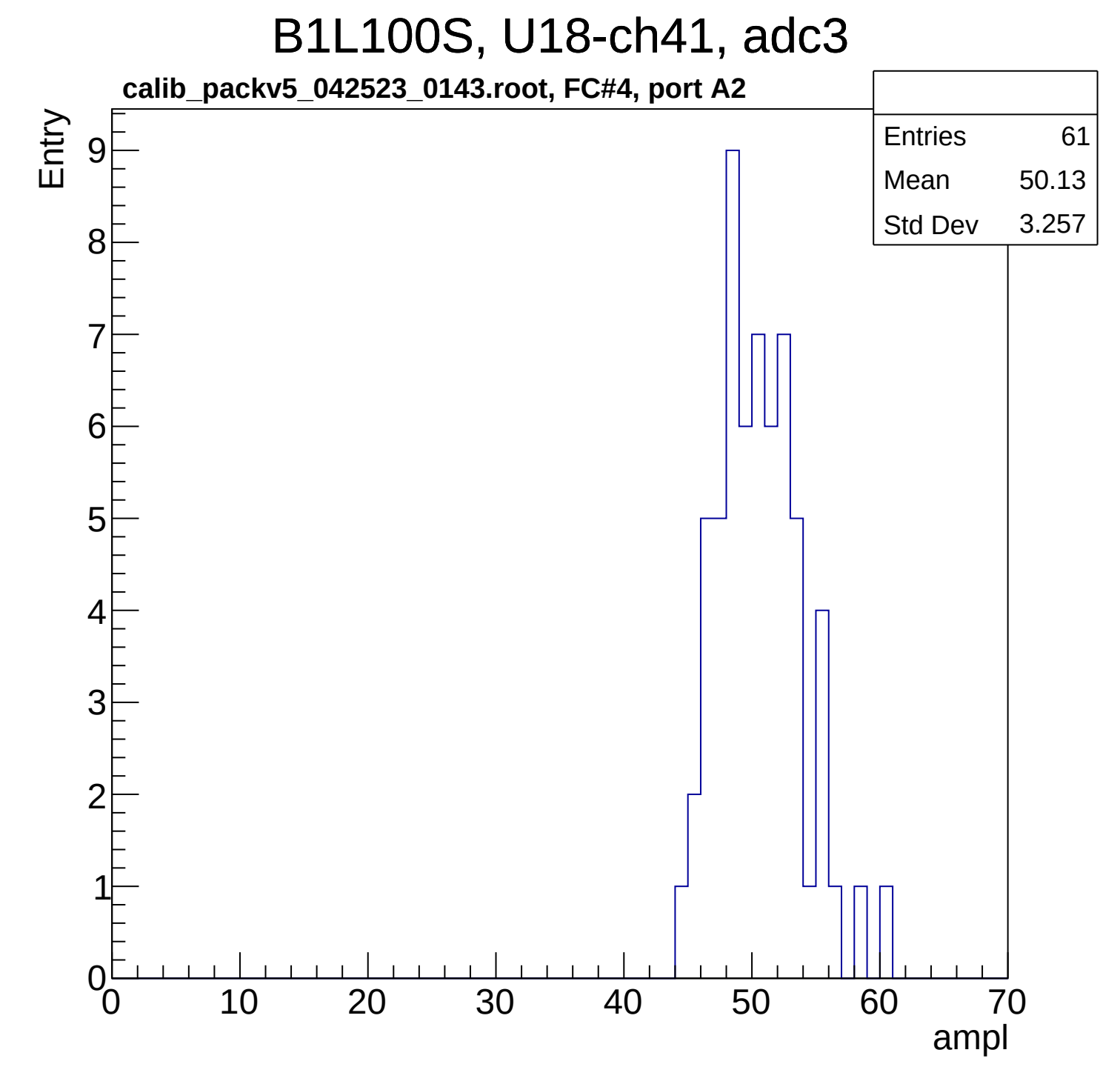

B1L100S, U18-ch40, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

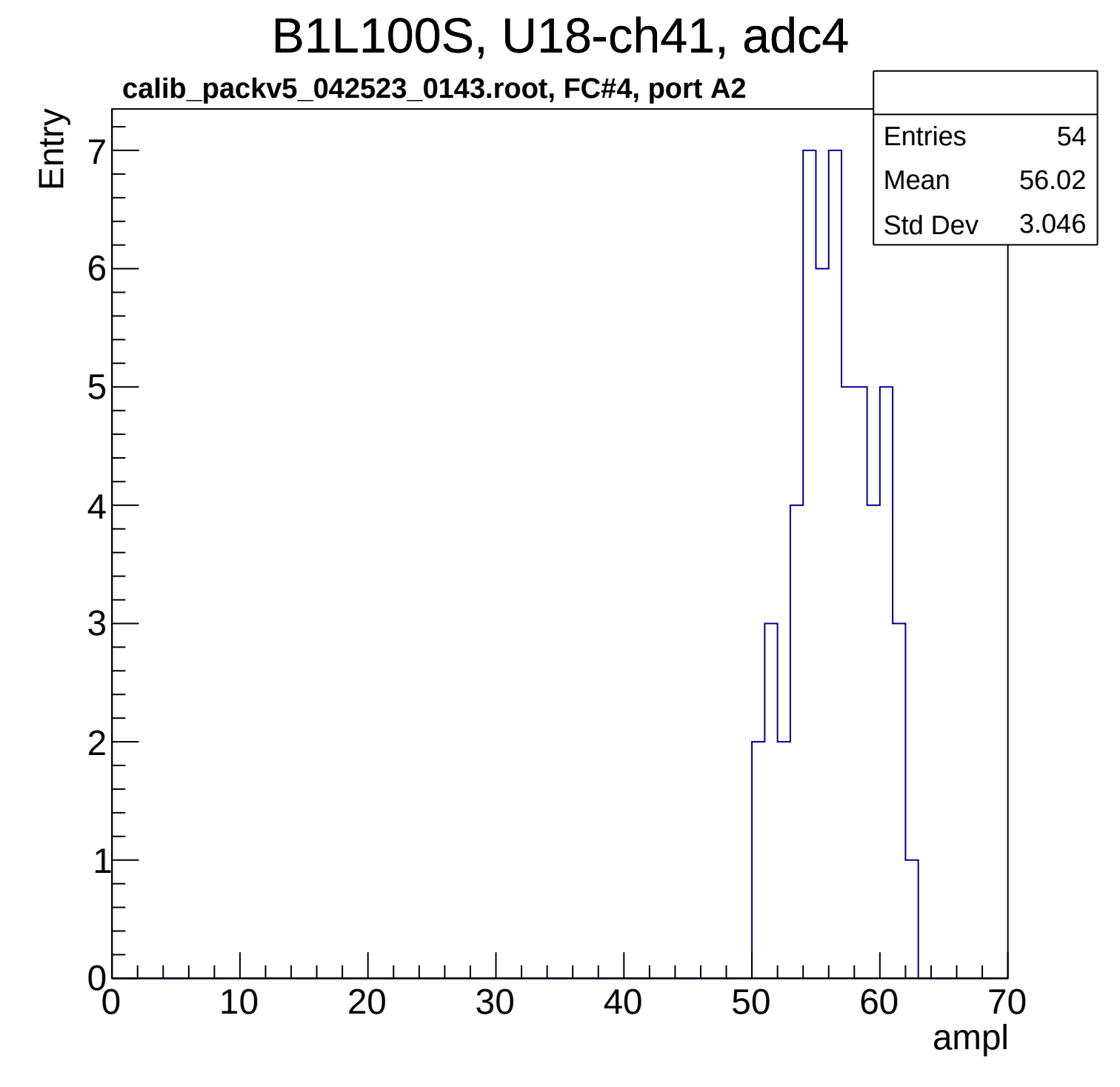

B1L100S, U18-ch40, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

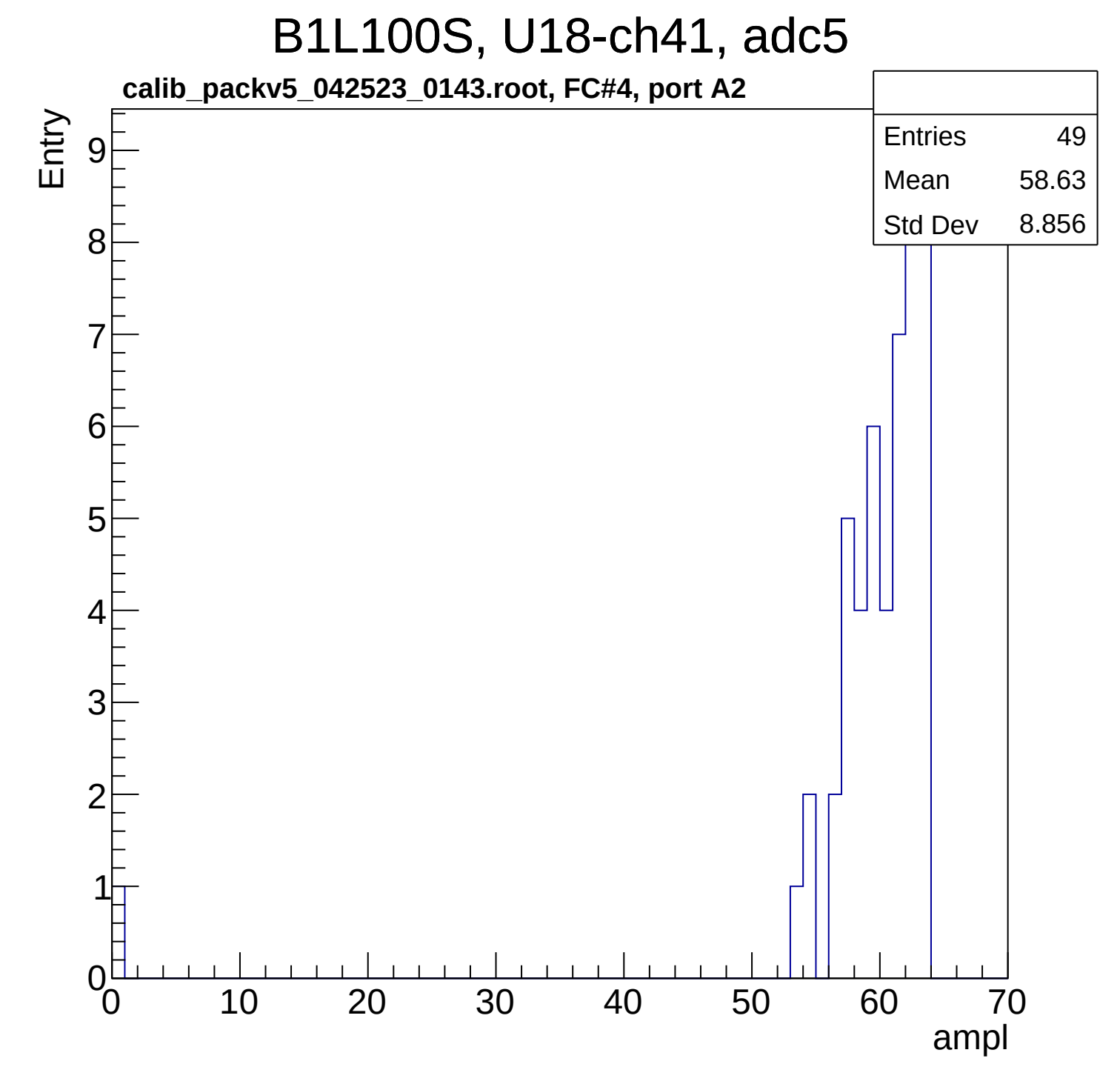

B1L100S, U18-ch41, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 40
Mean 30.15
Std Dev 3.366
Gaus mean : 29.9742
Gaus Width: 4.1635
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

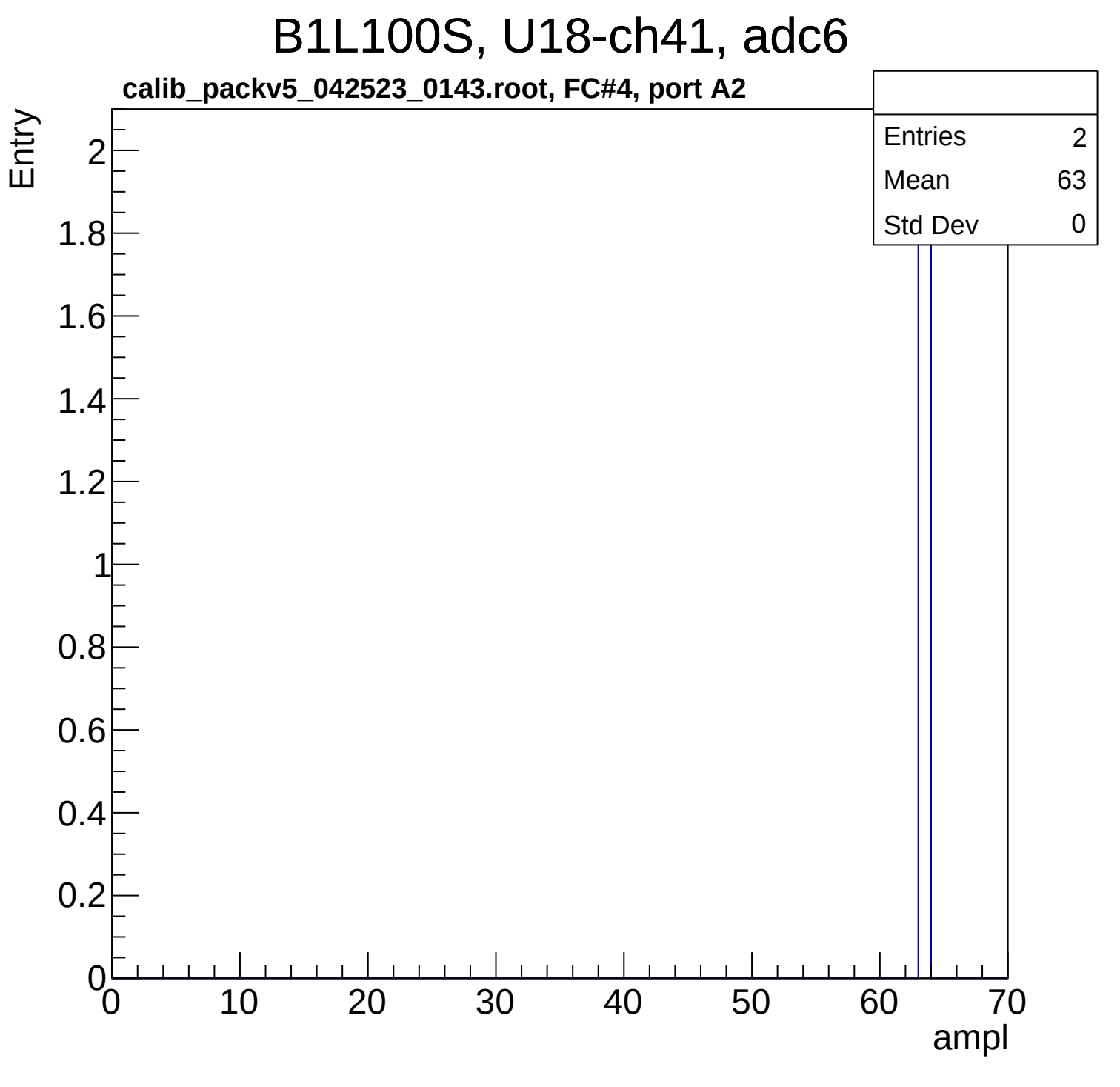

B1L100S, U18-ch41, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 83
Mean 36.02
Std Dev 3.828
Gaus mean : 36.8752
Gaus Width: 4.1572
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

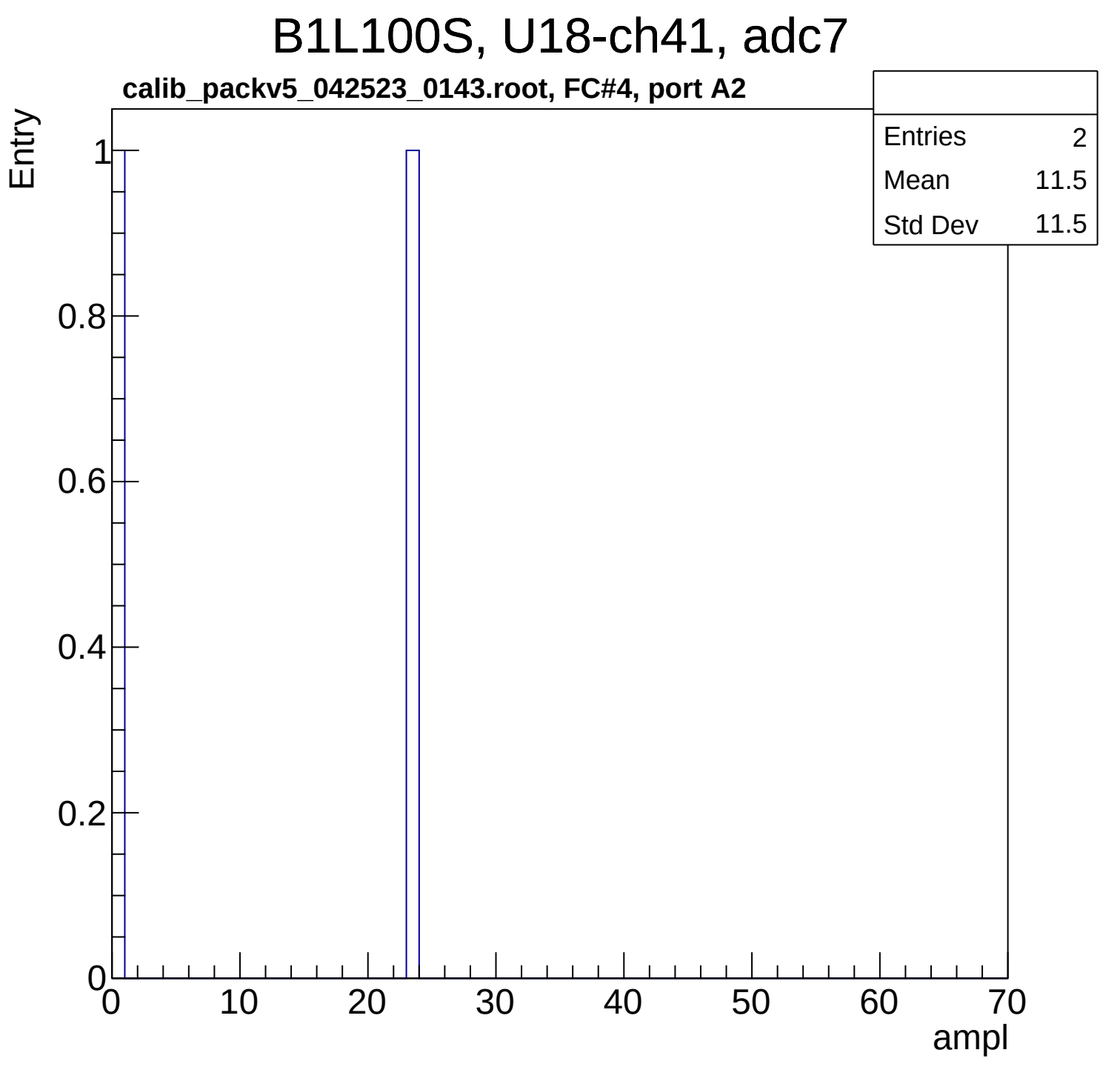

B1L100S, U18-ch41, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 43.52
Std Dev 3.593
Gaus mean : 43.8796
Gaus Width: 2.9615
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

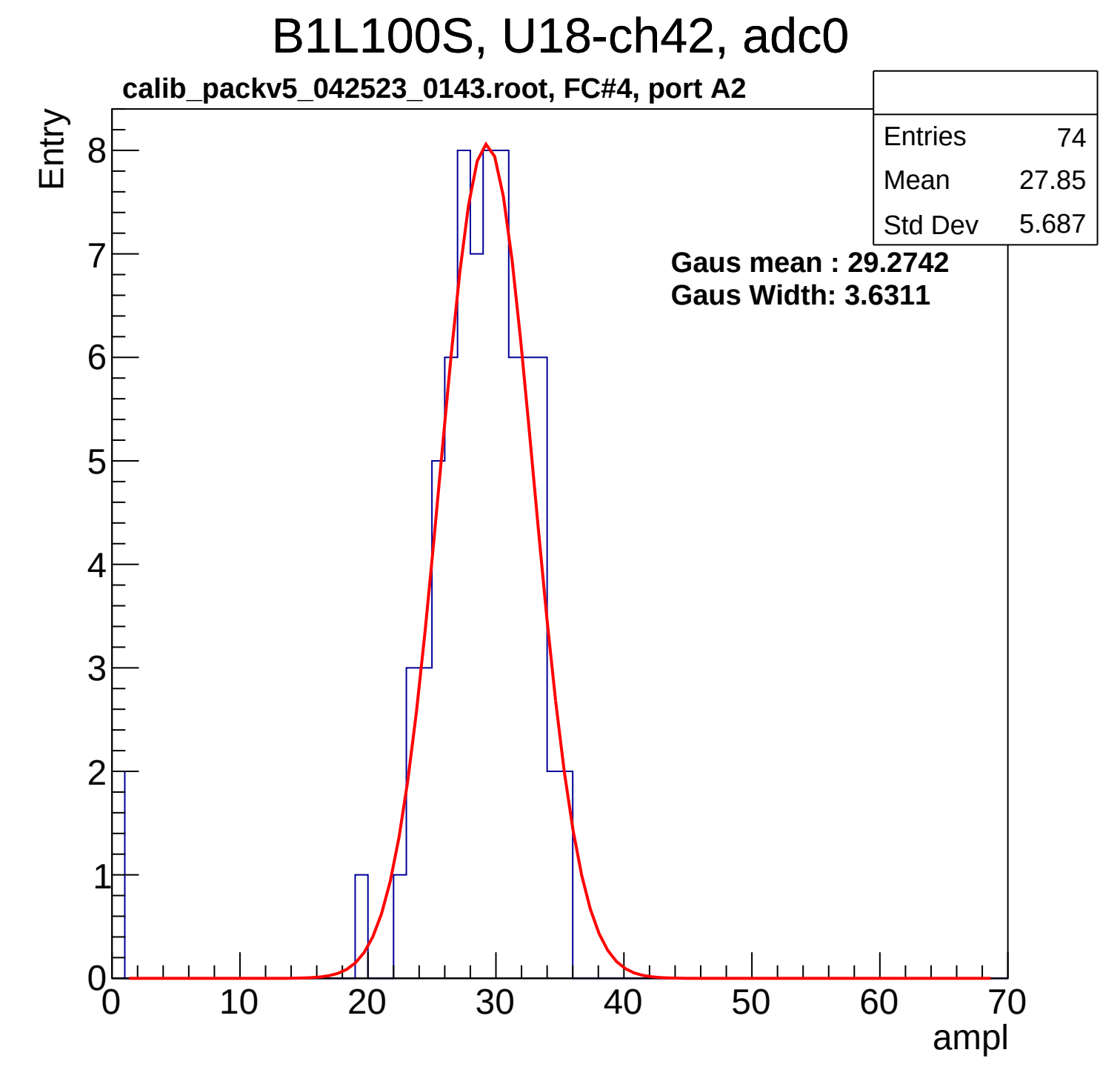

B1L100S, U18-ch41, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 50.13
Std Dev 3.257
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

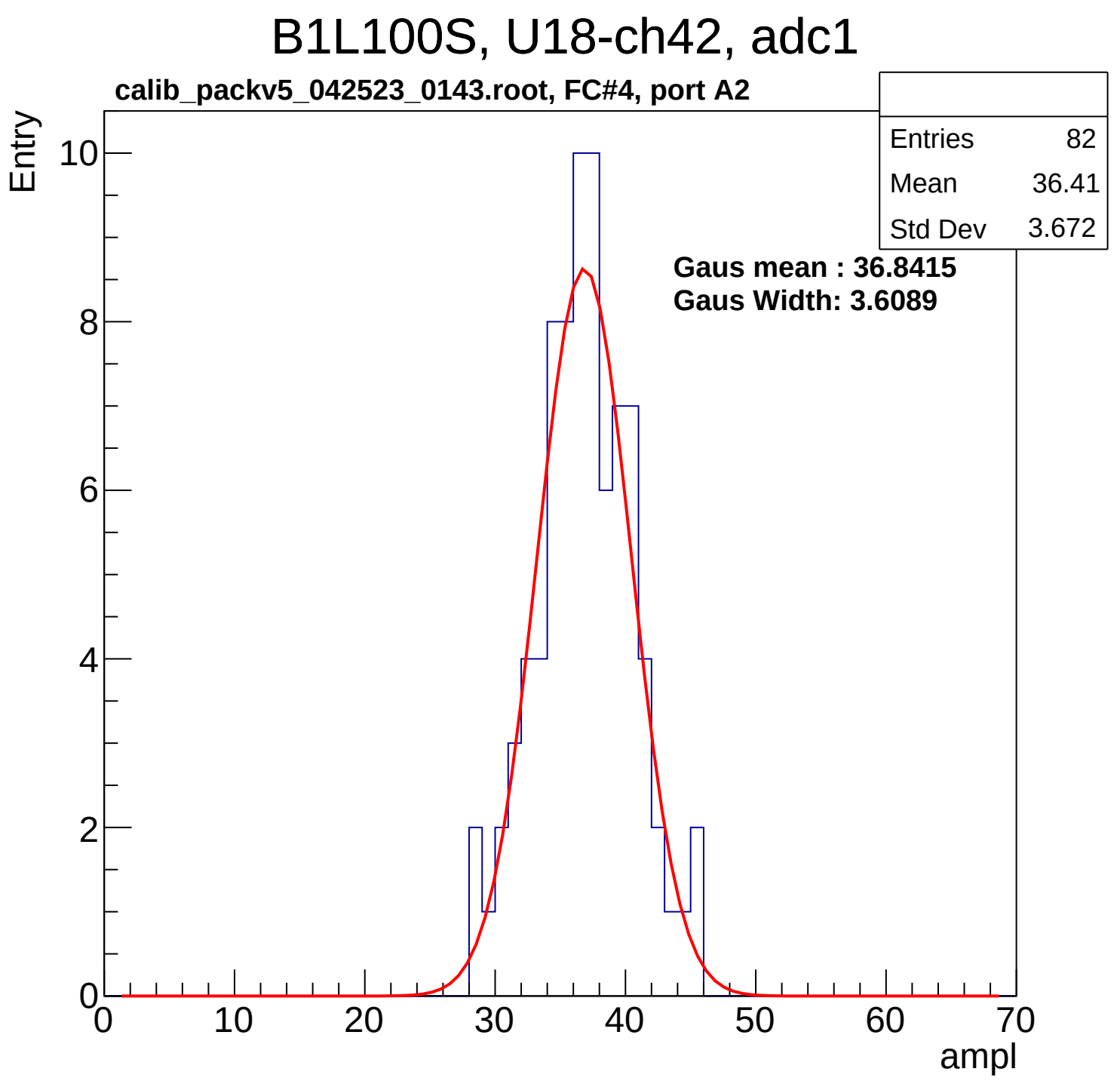

B1L100S, U18-ch41, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 56.02
Std Dev 3.046
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

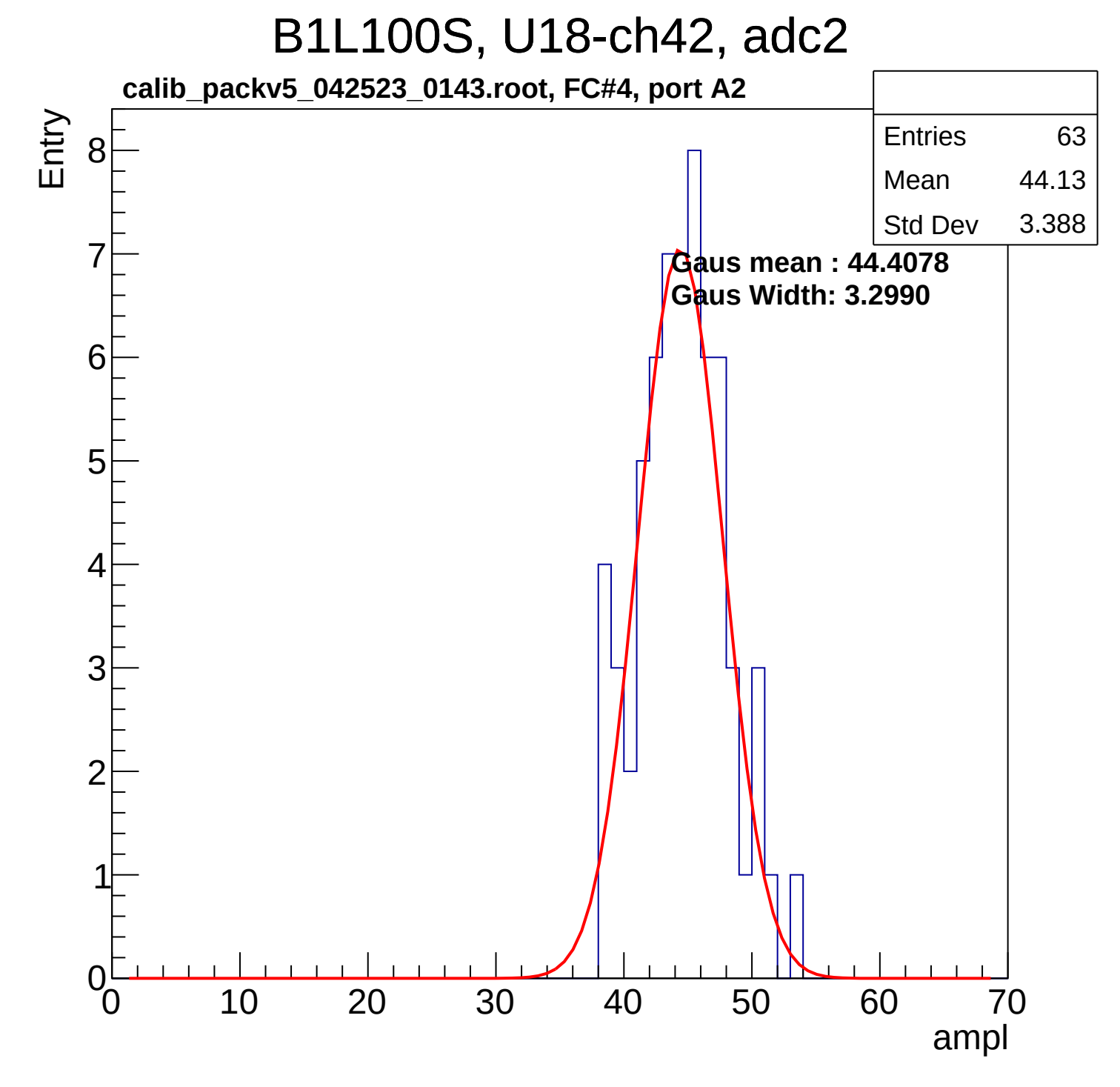

B1L100S, U18-ch41, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 58.63
Std Dev 8.856
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

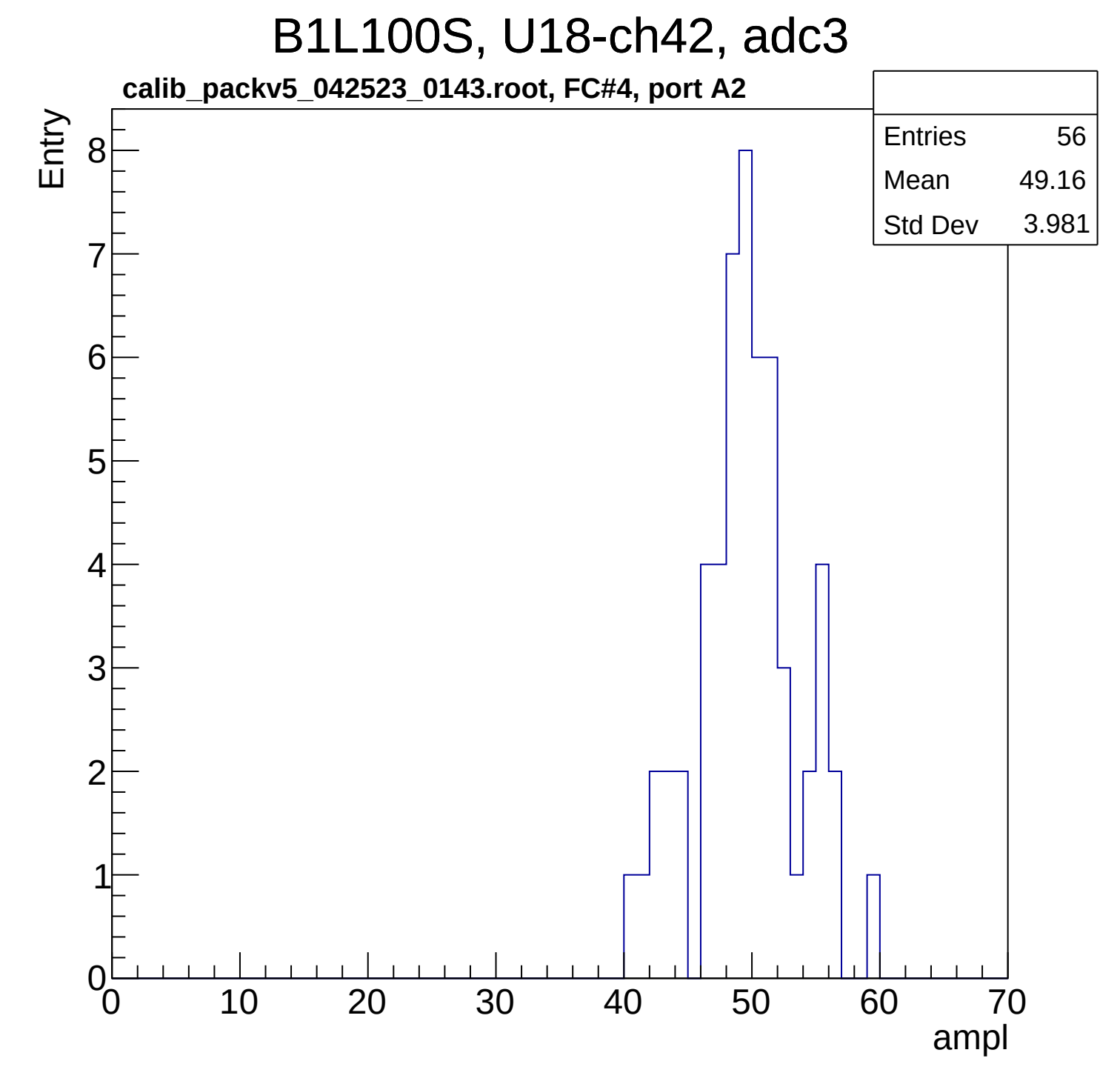

B1L100S, U18-ch41, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

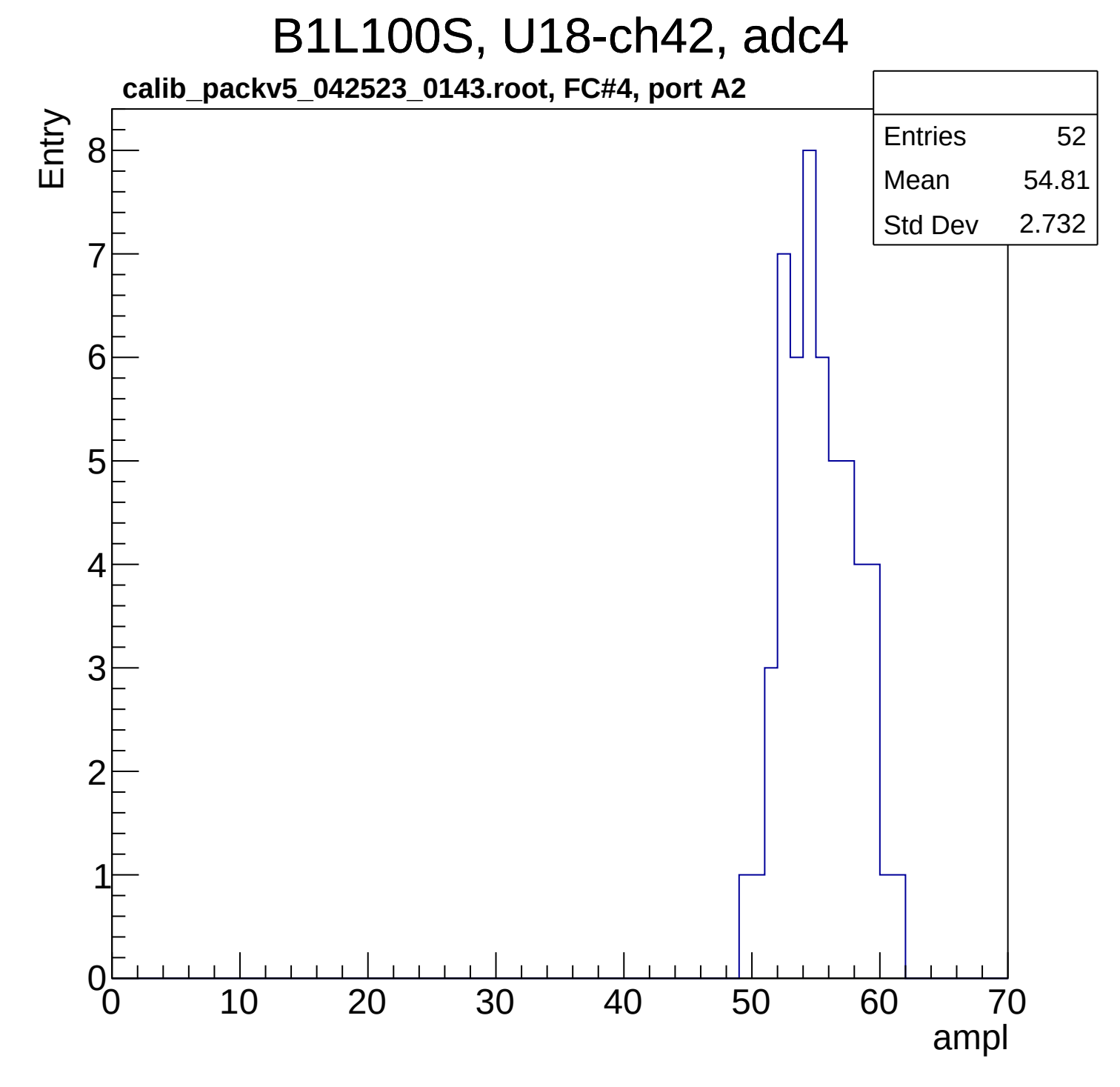

B1L100S, U18-ch41, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 11.5
Std Dev 11.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

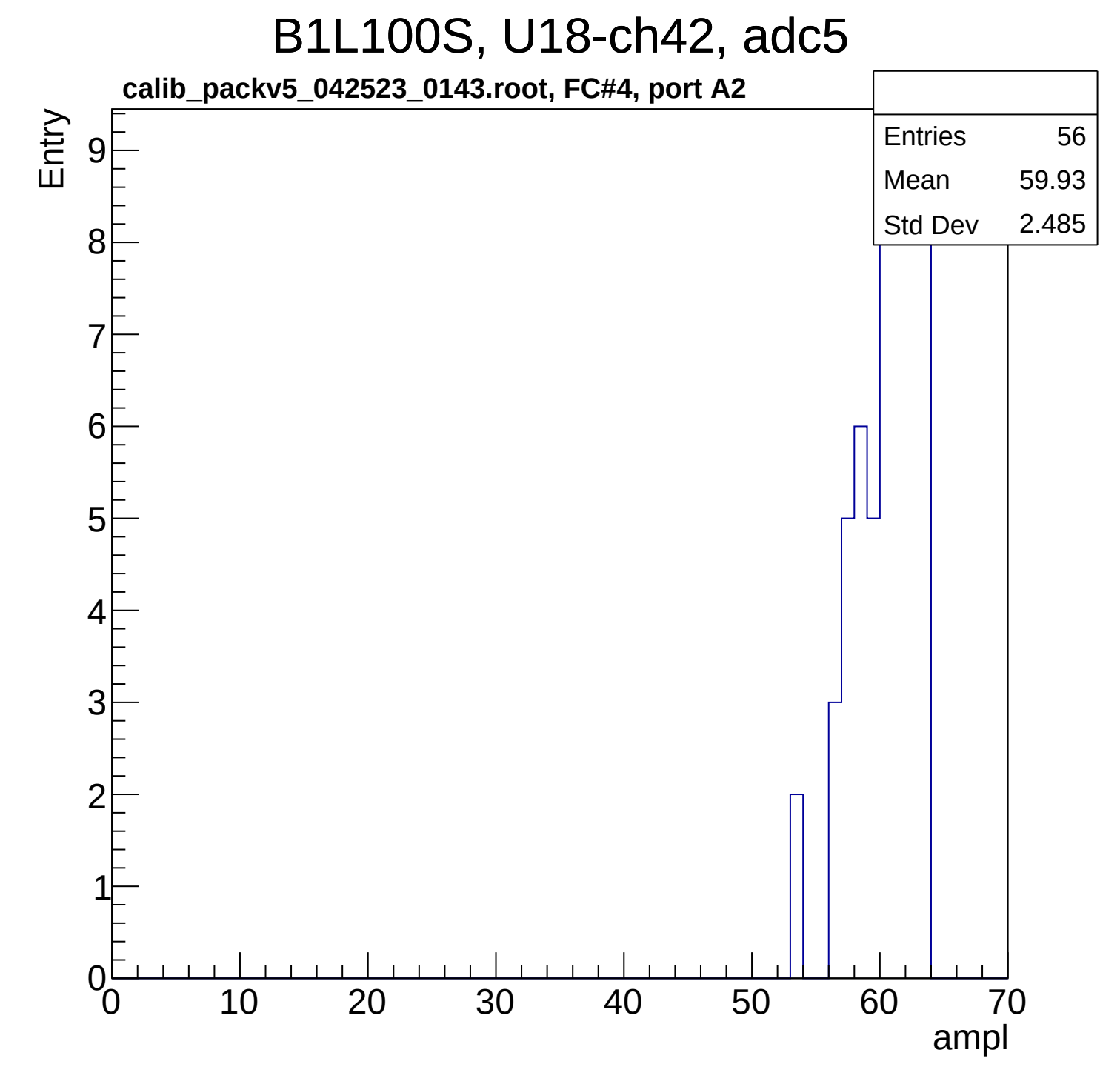

B1L100S, U18-ch42, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 27.85
Std Dev 5.687
Gaus mean : 29.2742
Gaus Width: 3.6311
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

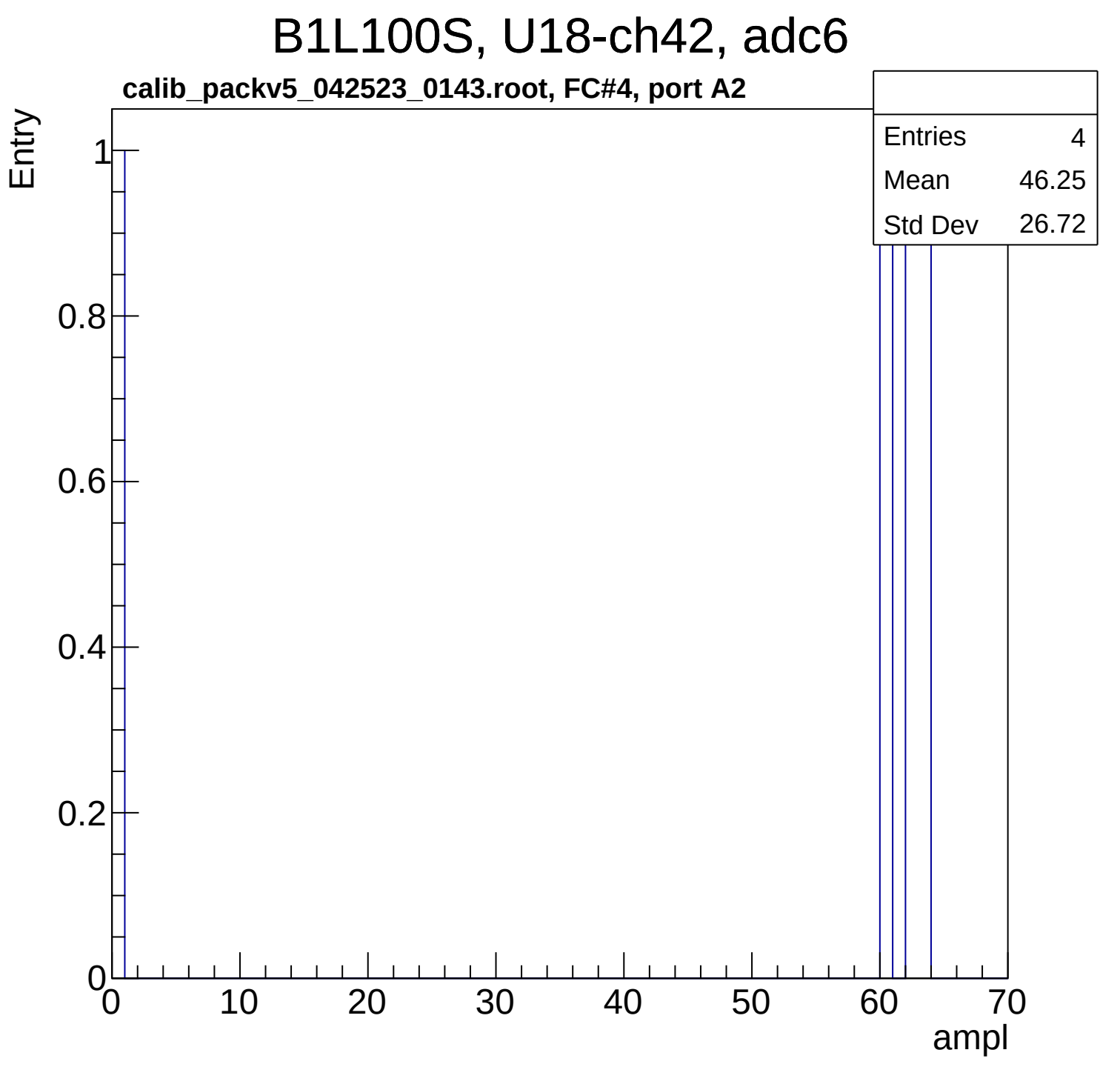

B1L100S, U18-ch42, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 36.41
Std Dev 3.672
Gaus mean : 36.8415
Gaus Width: 3.6089
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

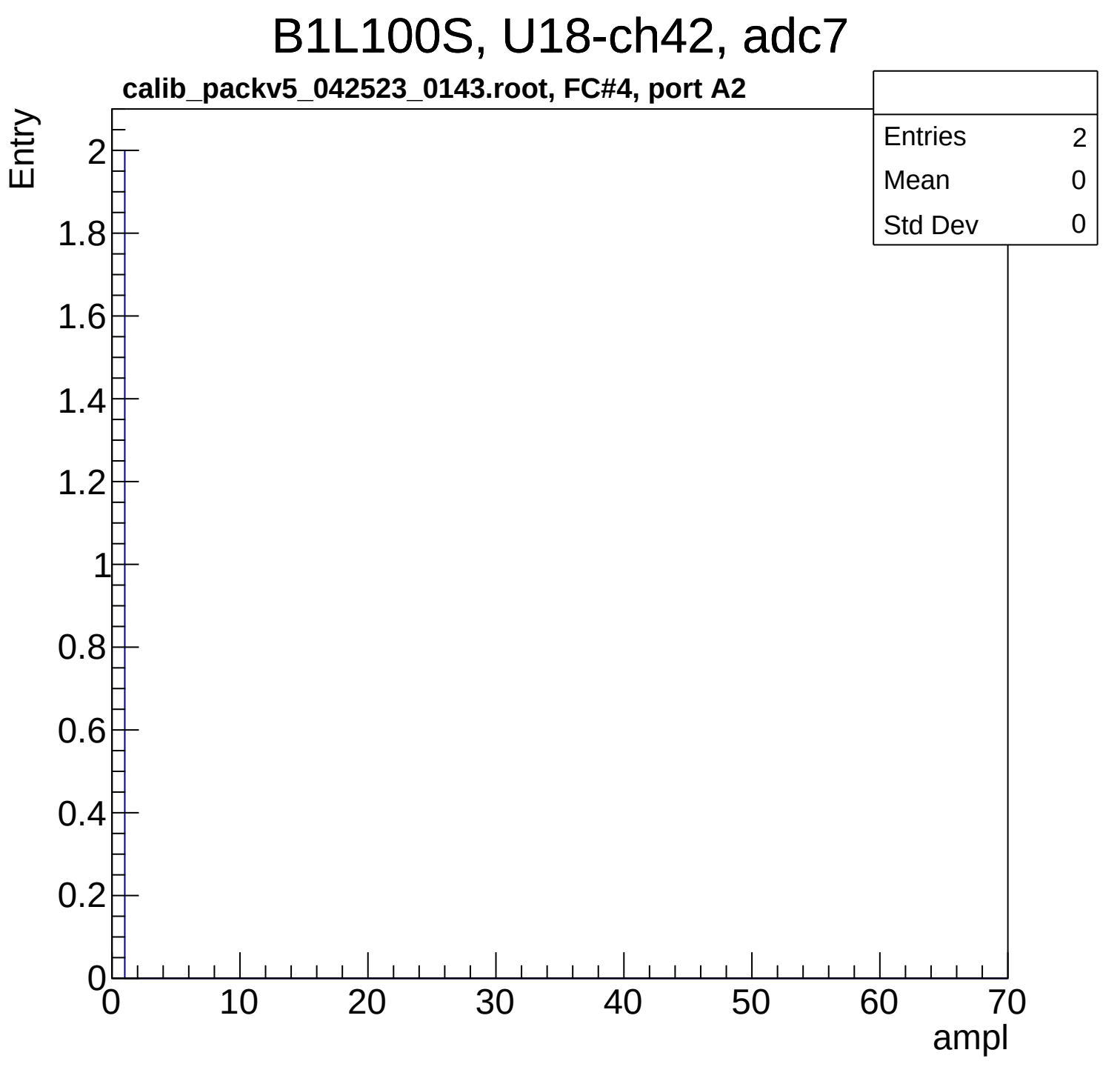

B1L100S, U18-ch42, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 44.13
Std Dev 3.388
Gaus mean : 44.4078
Gaus Width: 3.2990
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

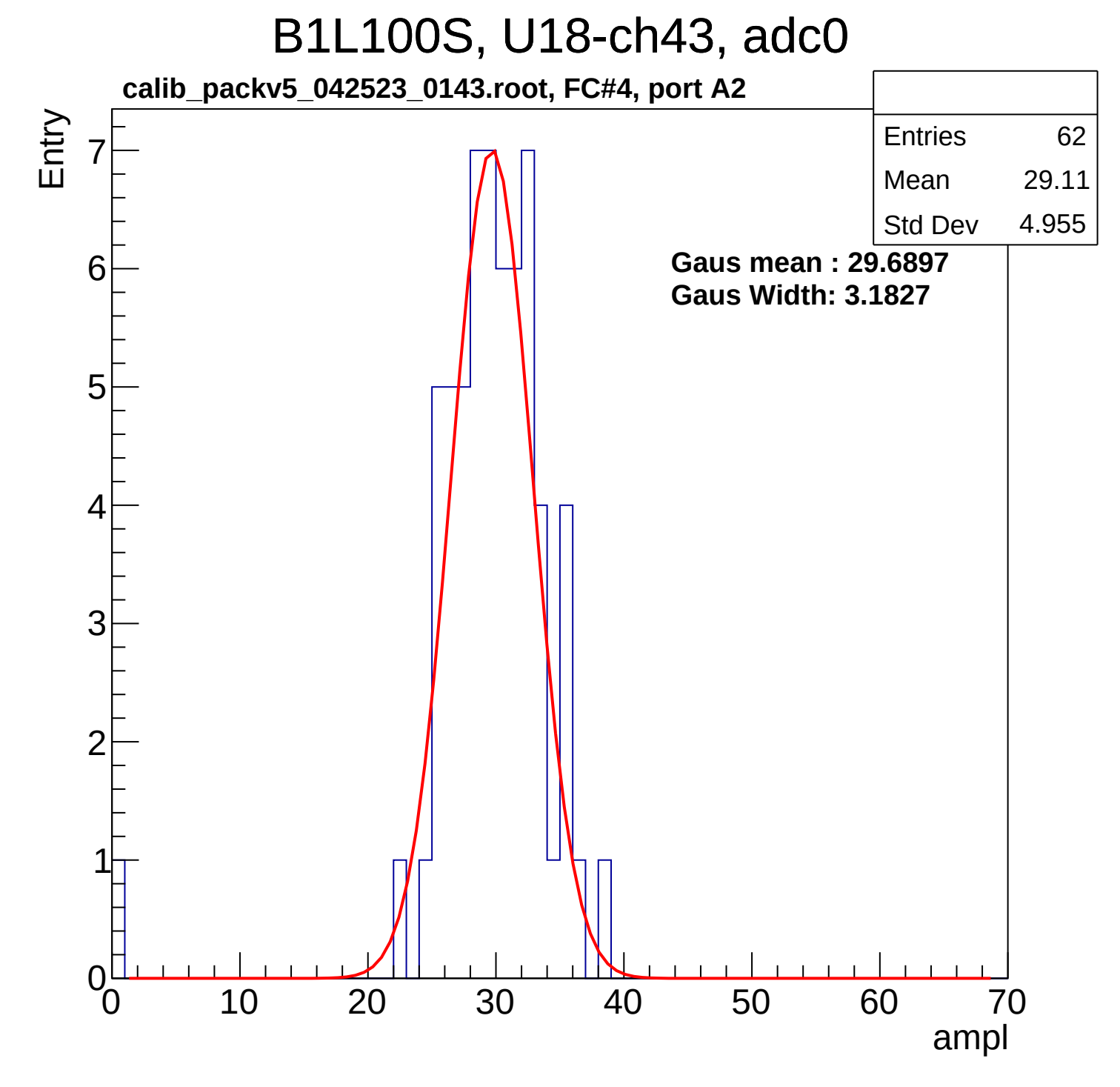

B1L100S, U18-ch42, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 49.16
Std Dev 3.981
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

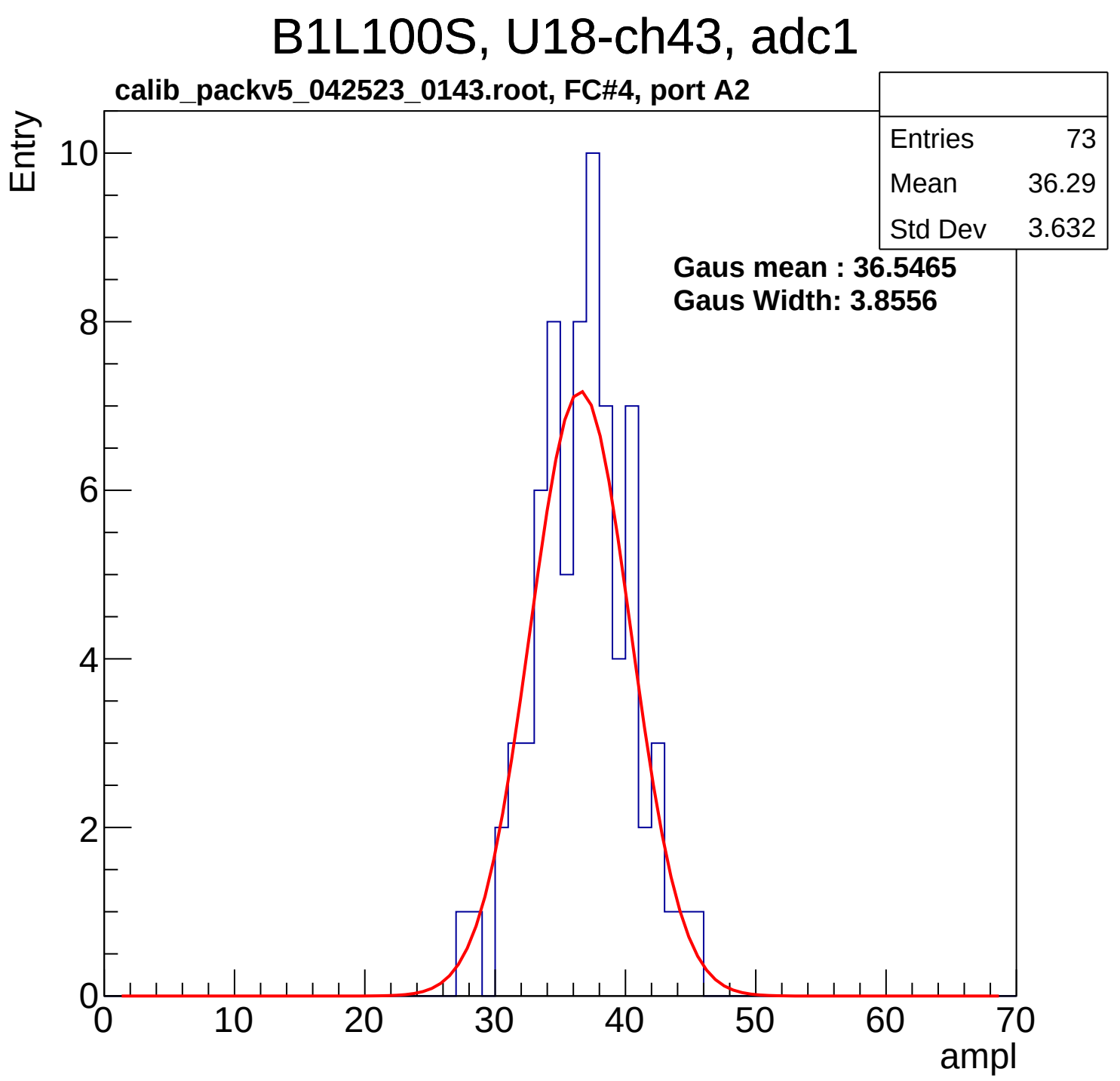

B1L100S, U18-ch42, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 54.81
Std Dev 2.732
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

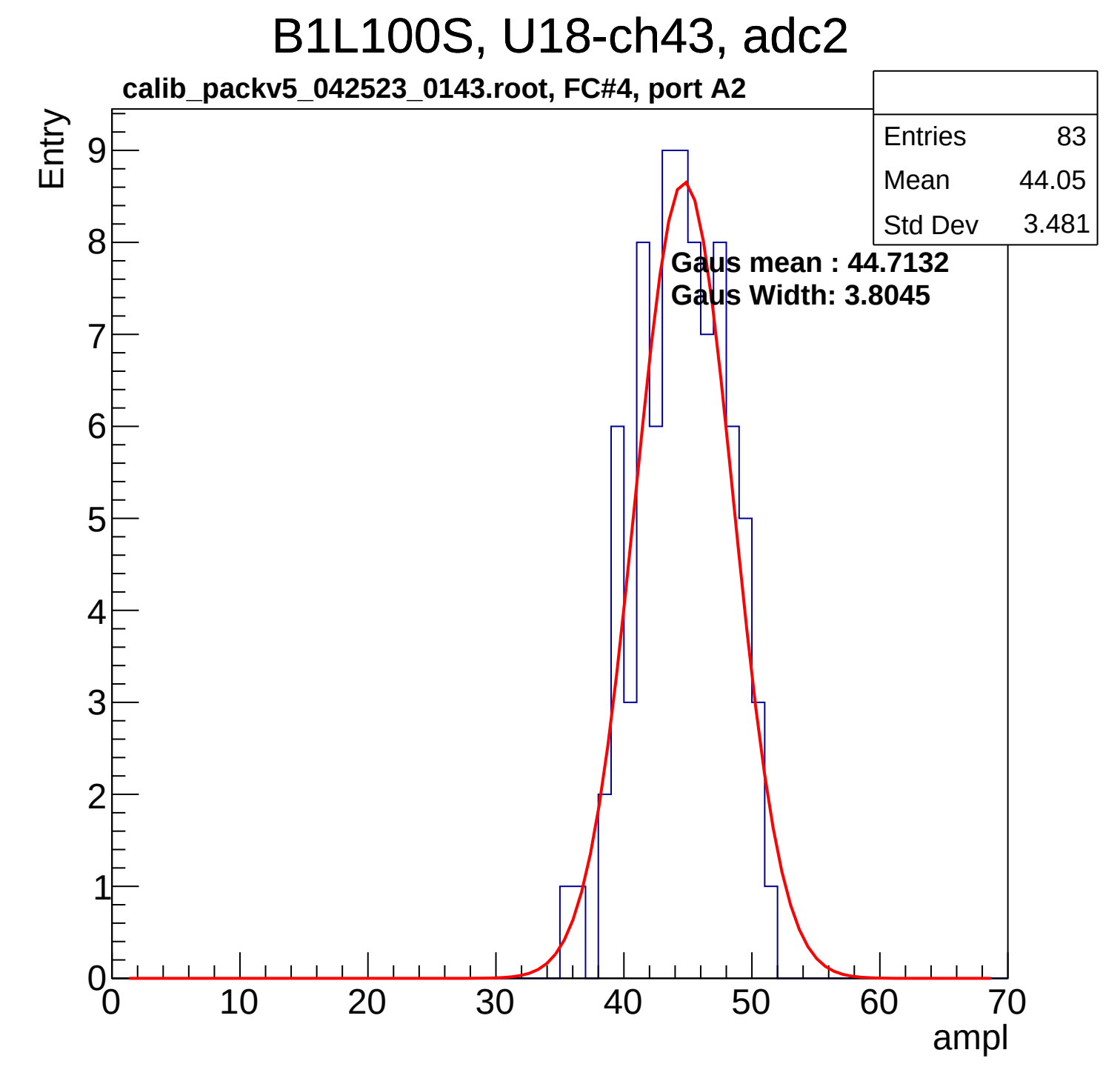

B1L100S, U18-ch42, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 59.93
Std Dev 2.485
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

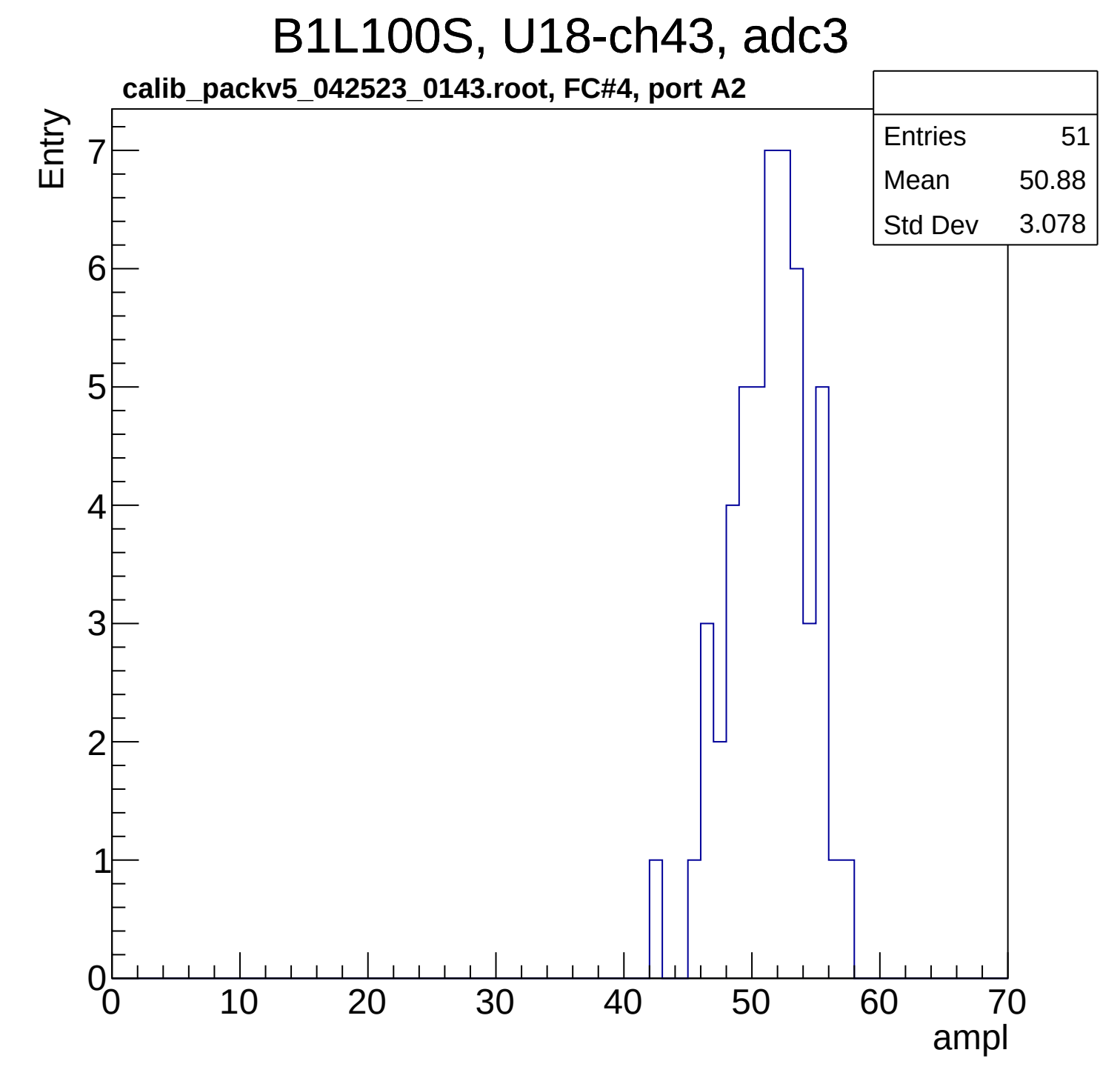

B1L100S, U18-ch42, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 46.25
Std Dev 26.72
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

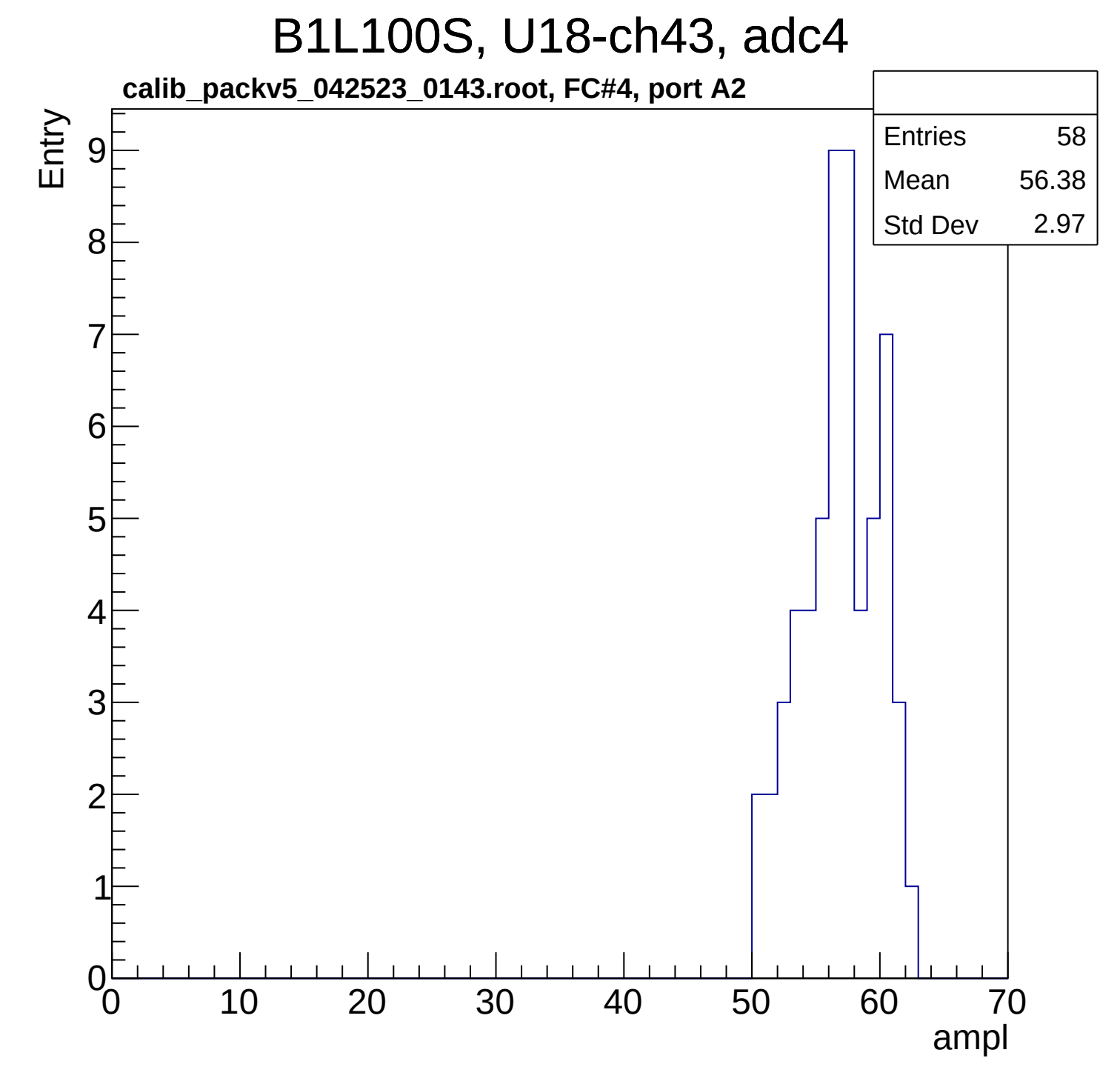

B1L100S, U18-ch42, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

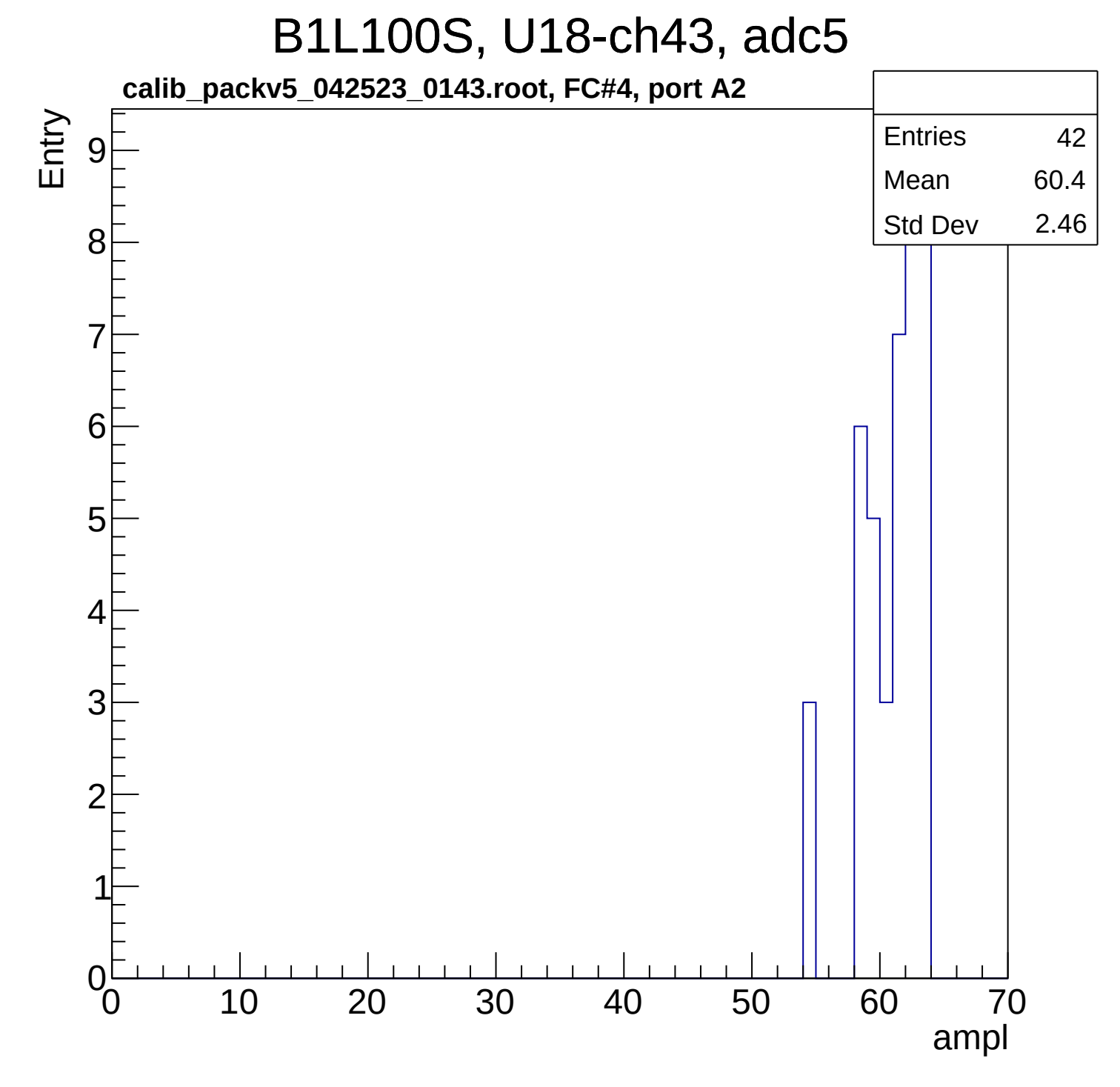

B1L100S, U18-ch43, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 29.11
Std Dev 4.955
Gaus mean : 29.6897
Gaus Width: 3.1827
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

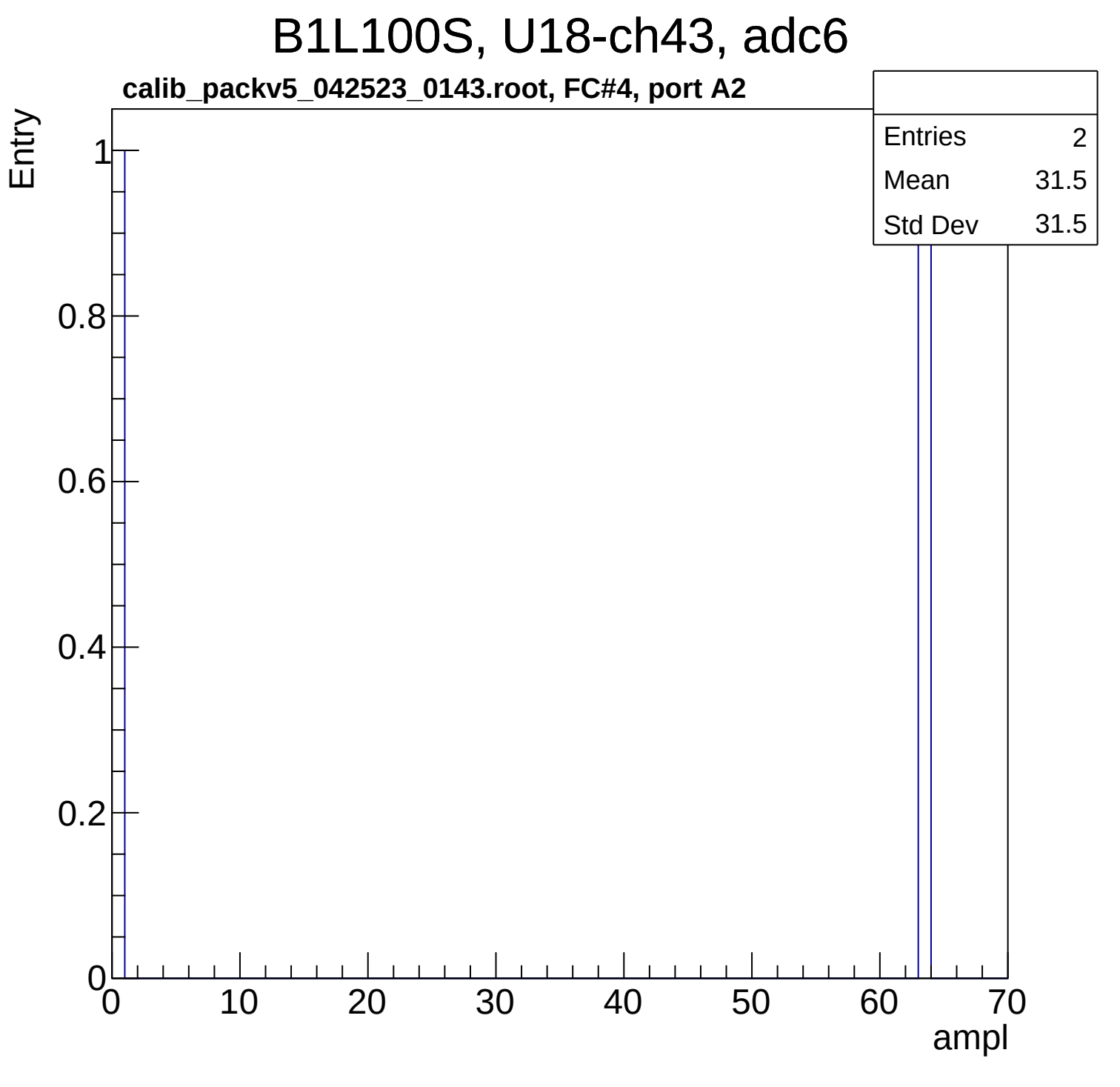

B1L100S, U18-ch43, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 36.29
Std Dev 3.632
Gaus mean : 36.5465
Gaus Width: 3.8556
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

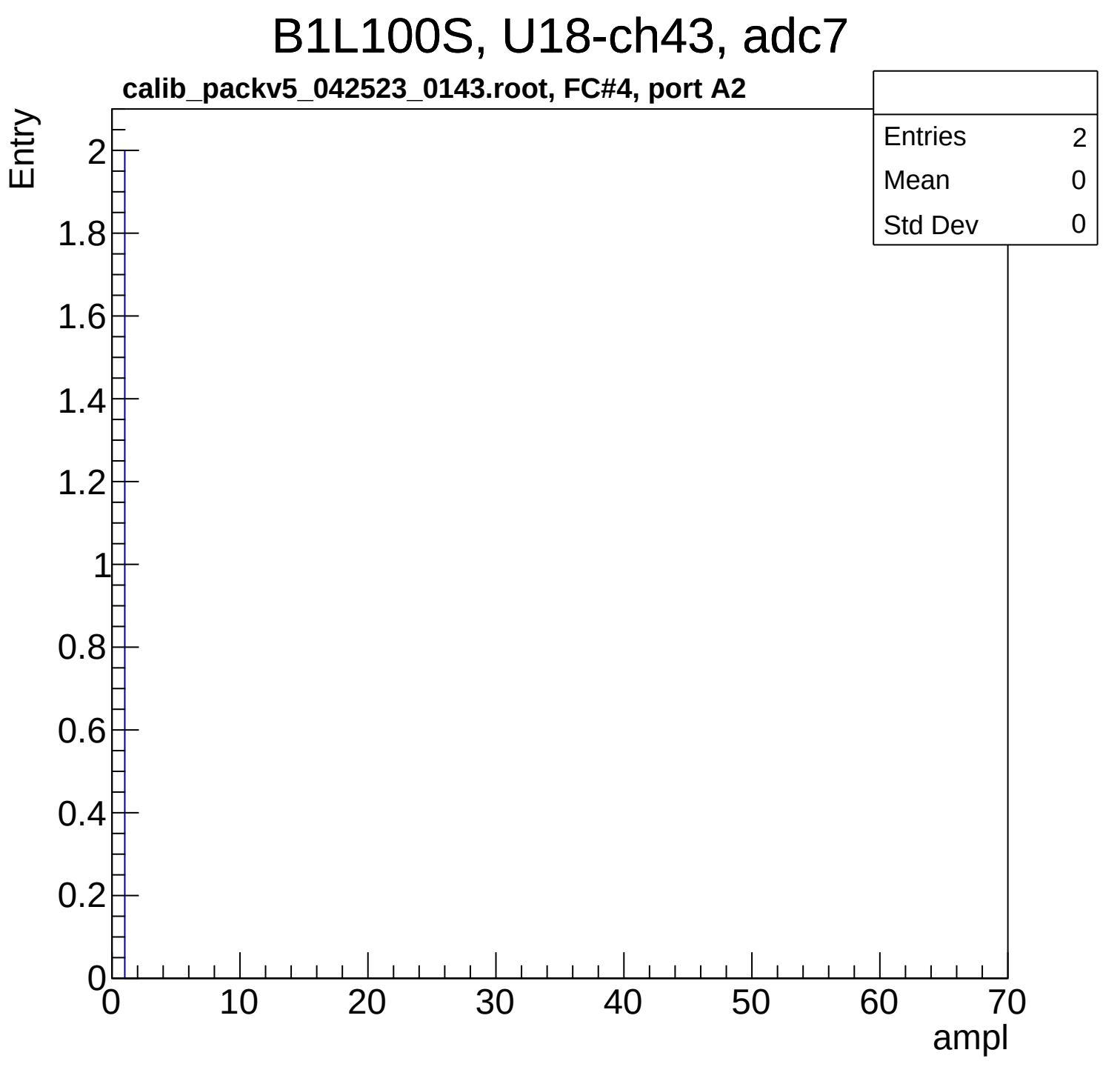

B1L100S, U18-ch43, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 83
Mean 44.05
Std Dev 3.481
Gaus mean : 44.7132
Gaus Width: 3.8045
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

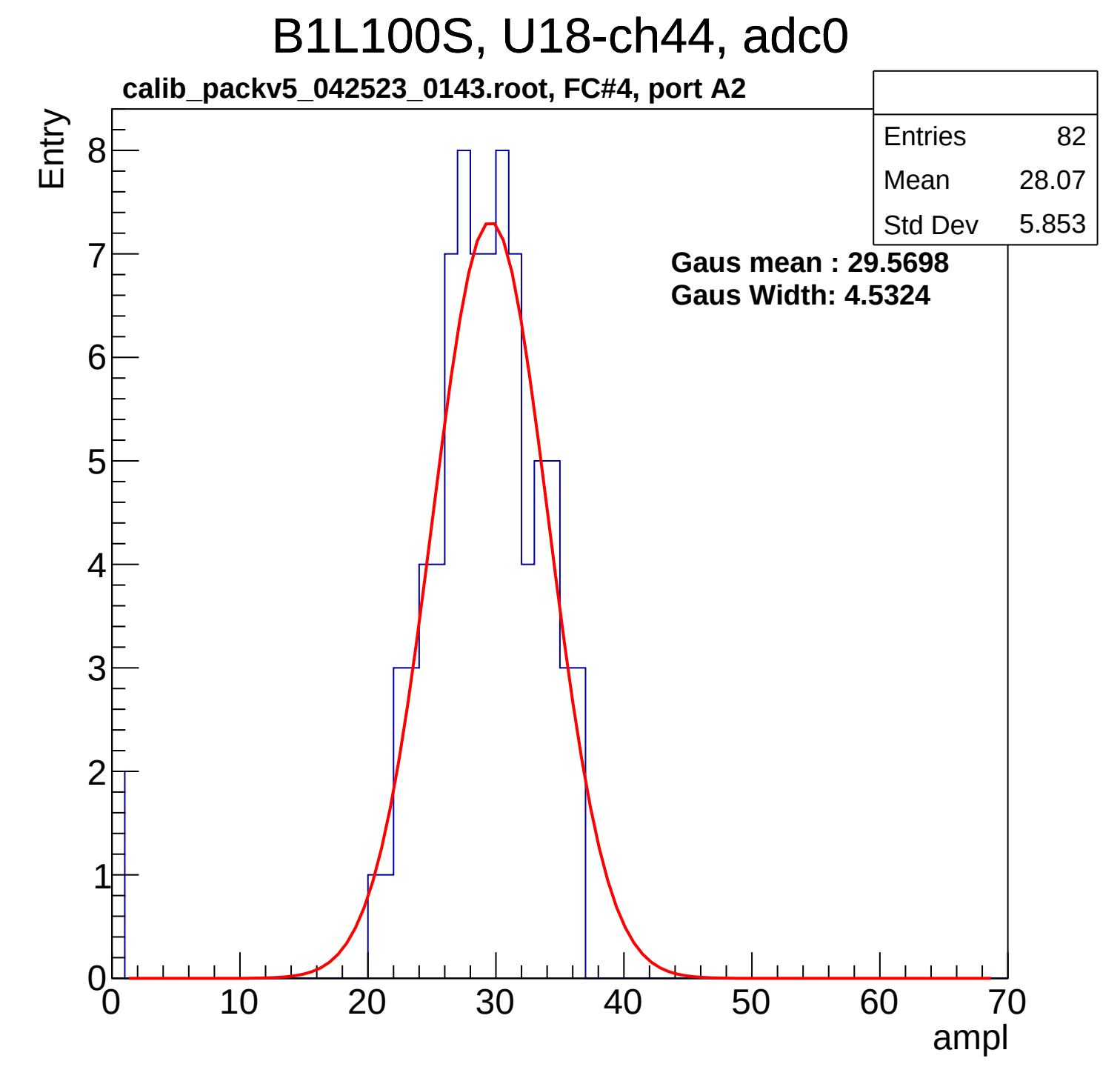

B1L100S, U18-ch43, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 50.88
Std Dev 3.078
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

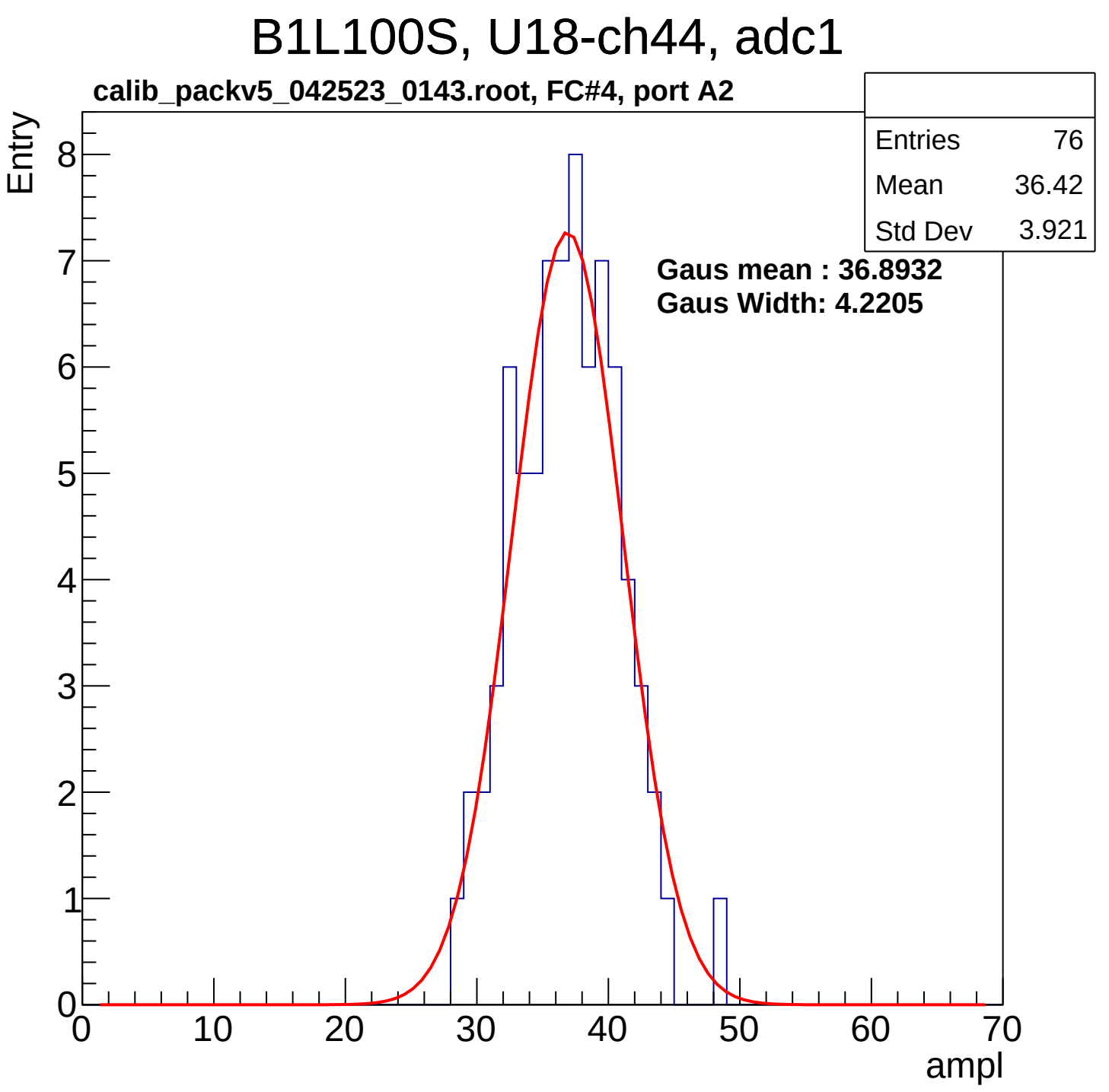

B1L100S, U18-ch43, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 56.38
Std Dev 2.97
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

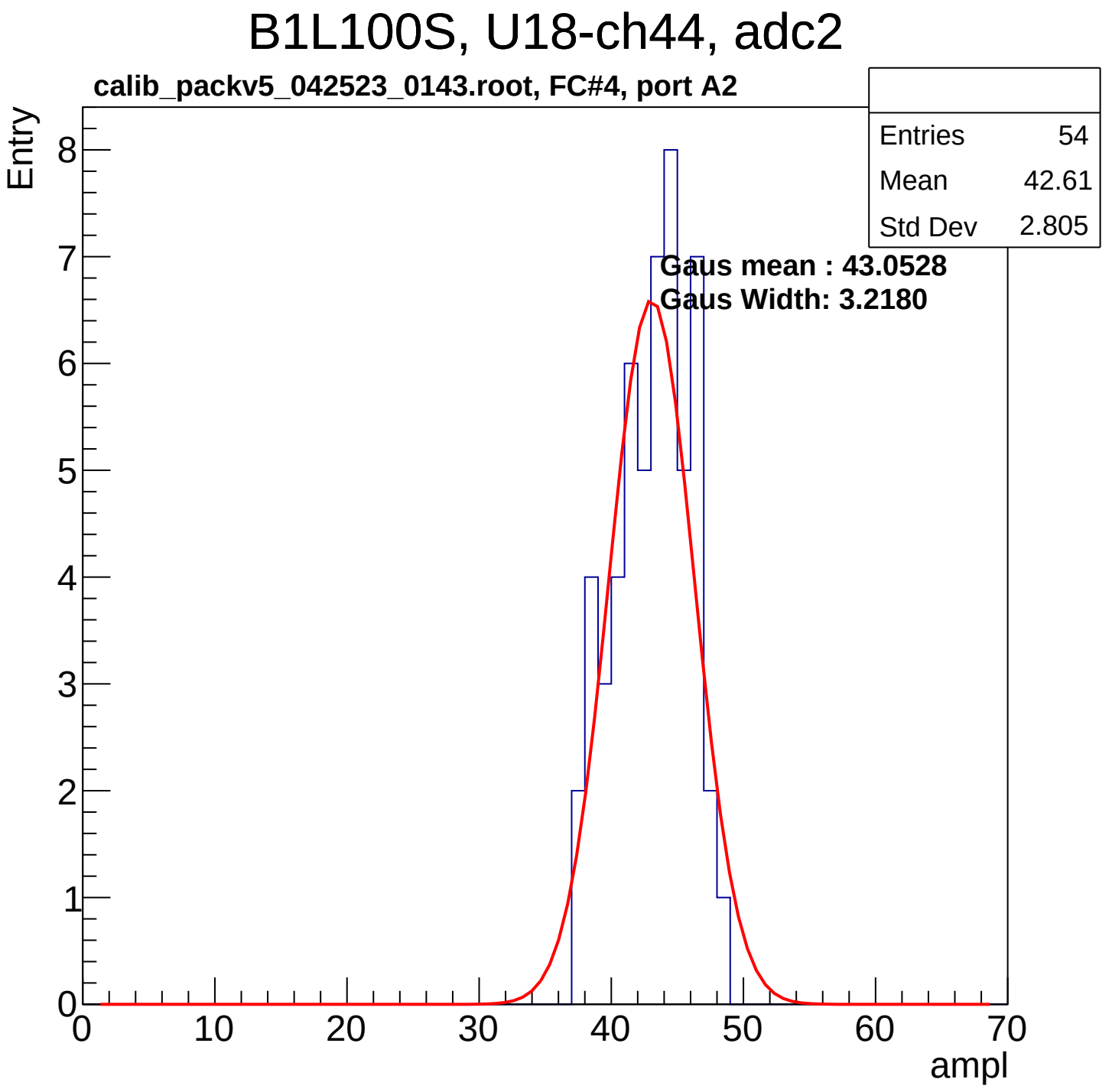

B1L100S, U18-ch43, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 42
Mean 60.4
Std Dev 2.46
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

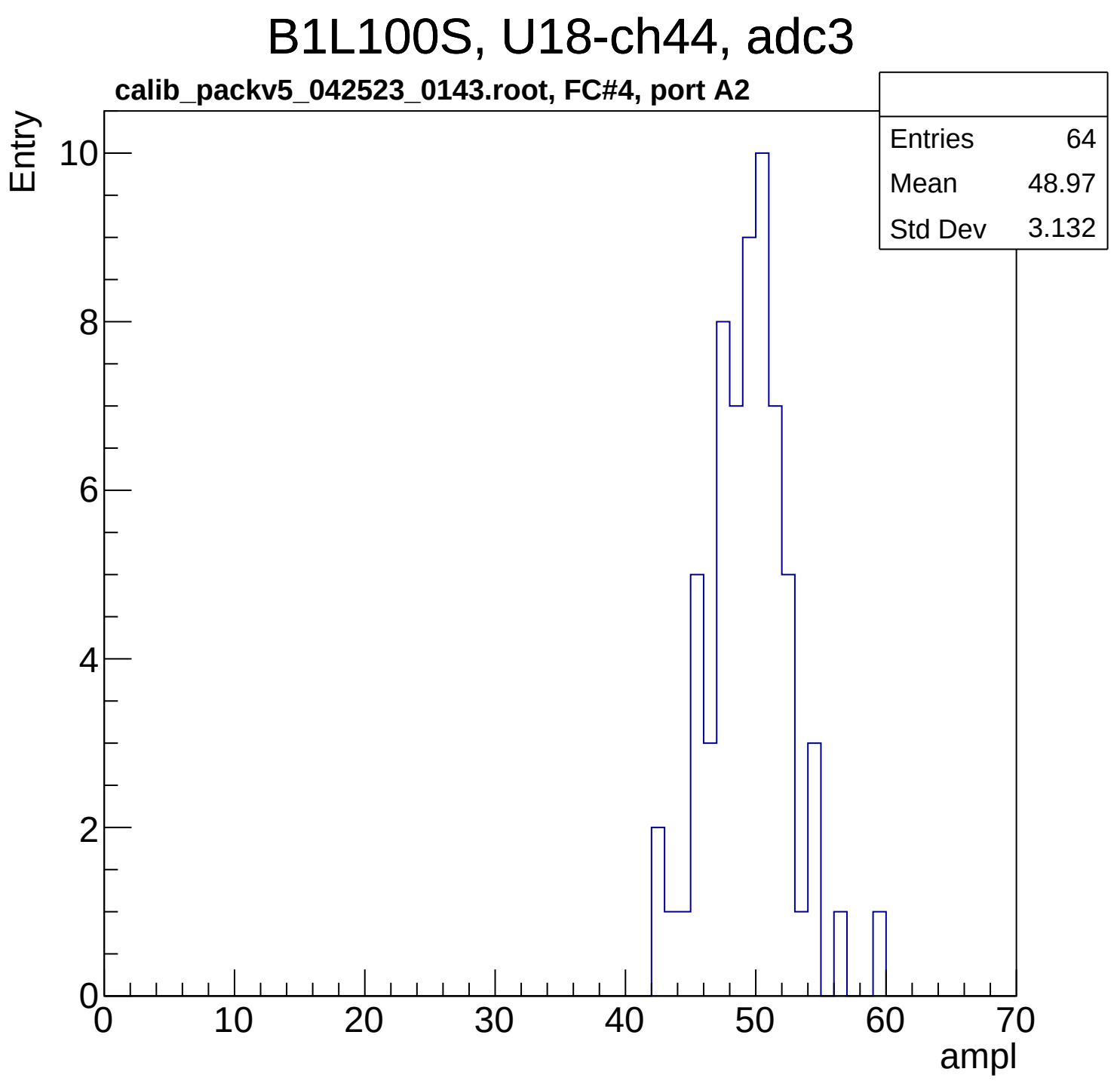

B1L100S, U18-ch43, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

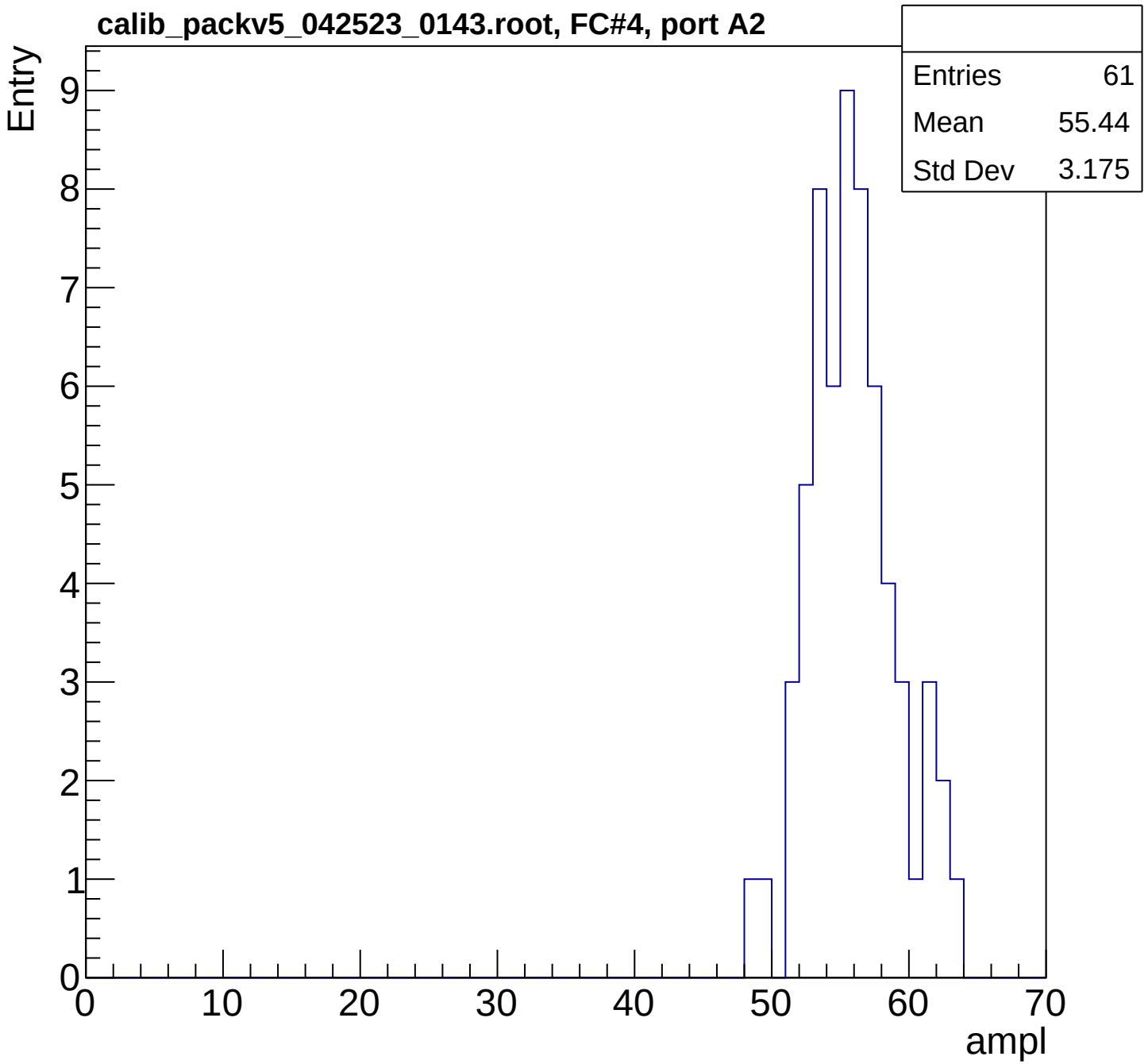

B1L100S, U18-ch43, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

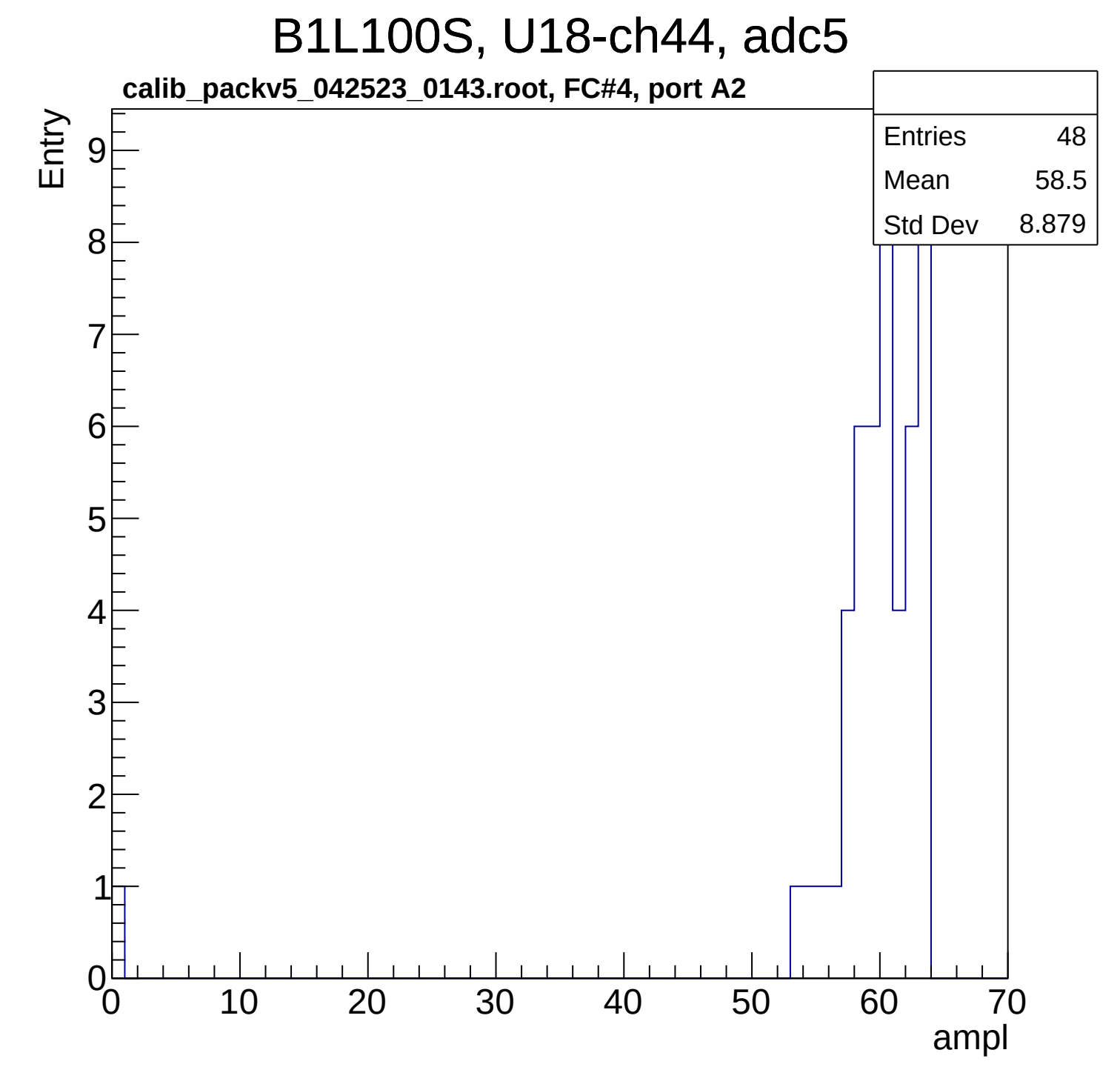

B1L100S, U18-ch44, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 28.07
Std Dev 5.853
Gaus mean : 29.5698
Gaus Width: 4.5324
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

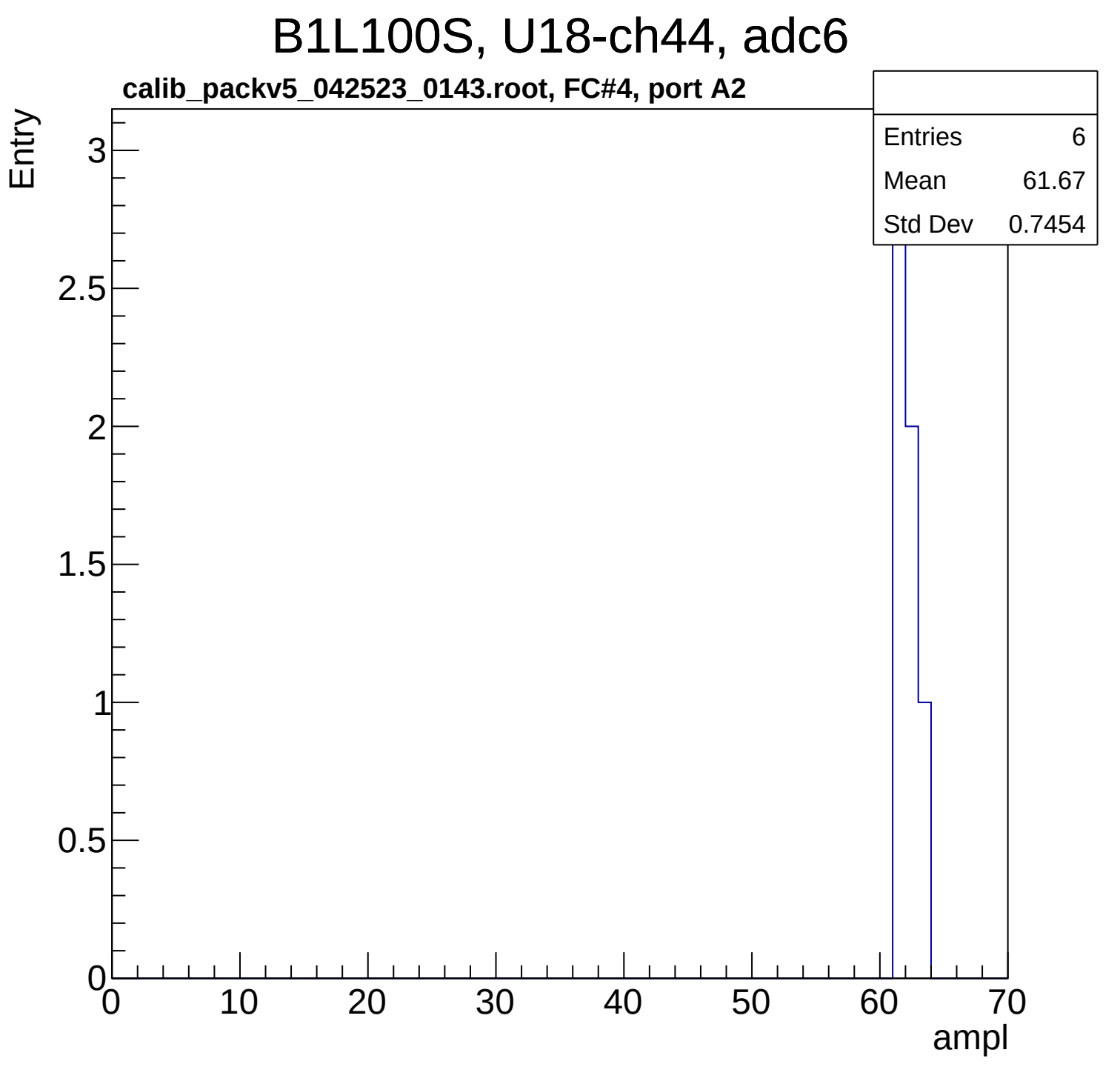

B1L100S, U18-ch44, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 36.42
Std Dev 3.921
Gaus mean : 36.8932
Gaus Width: 4.2205
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

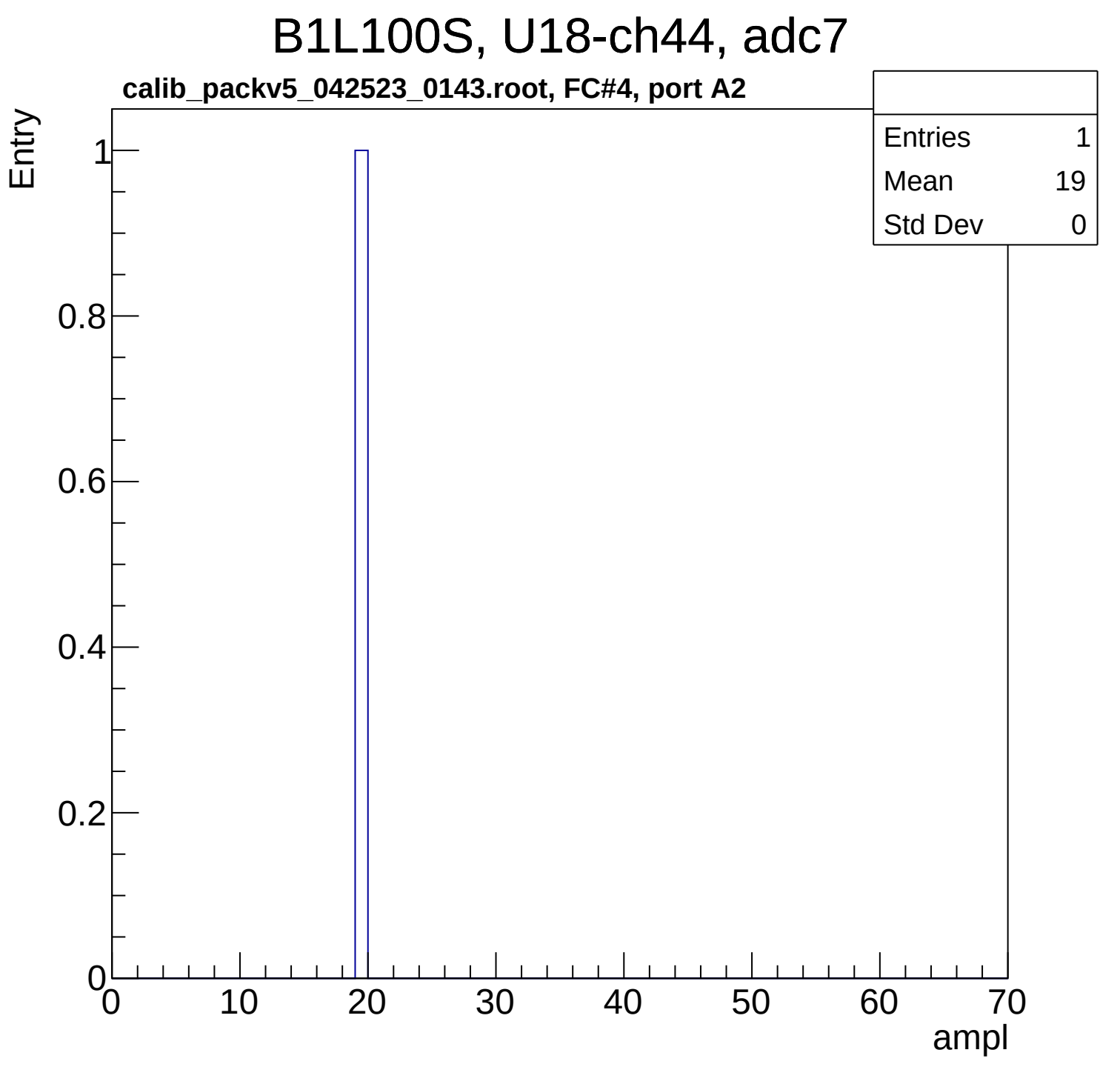

B1L100S, U18-ch44, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 42.61
Std Dev 2.805
Gaus mean : 43.0528
Gaus Width: 3.2180
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

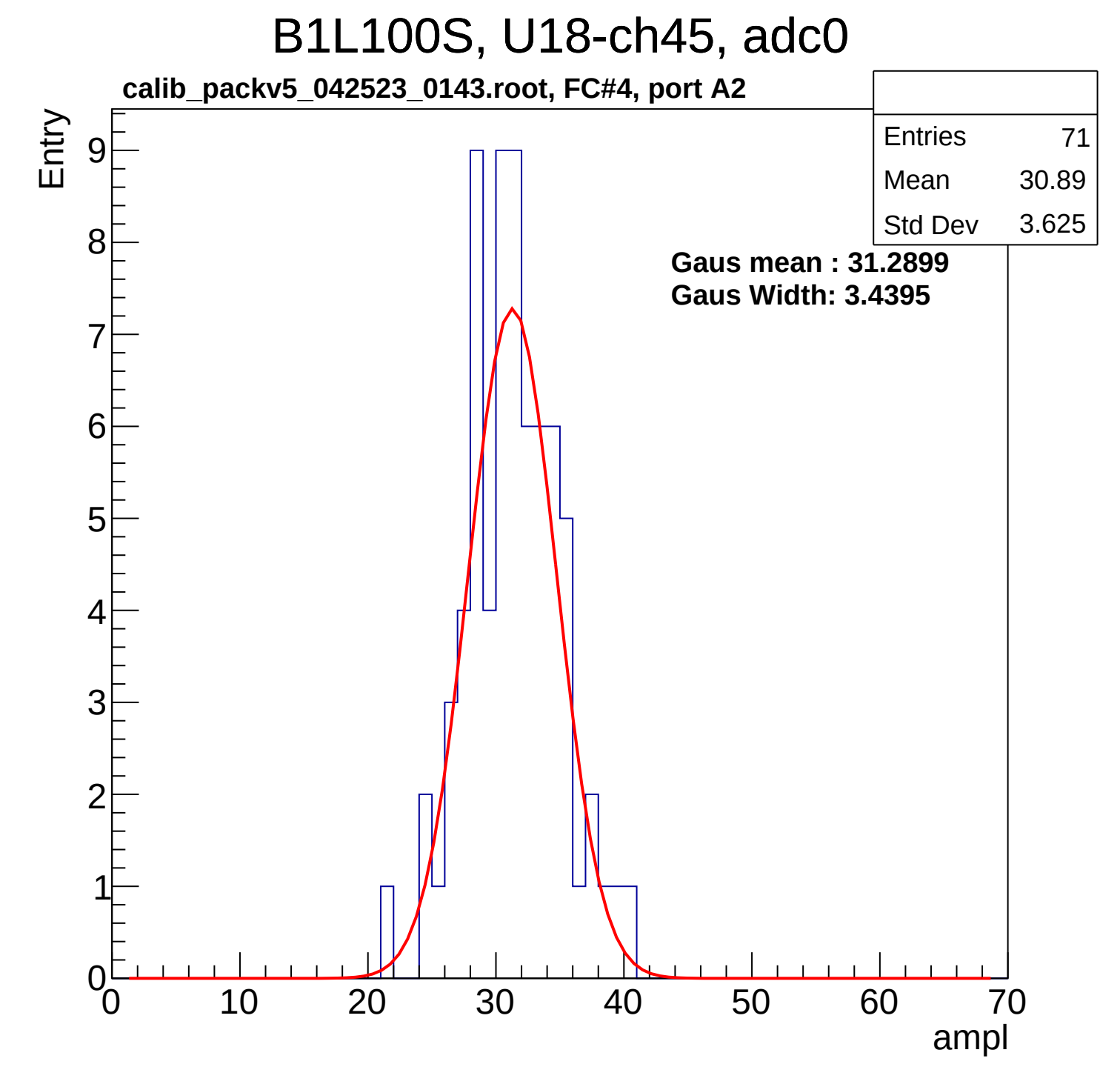

B1L100S, U18-ch44, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 48.97
Std Dev 3.132
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

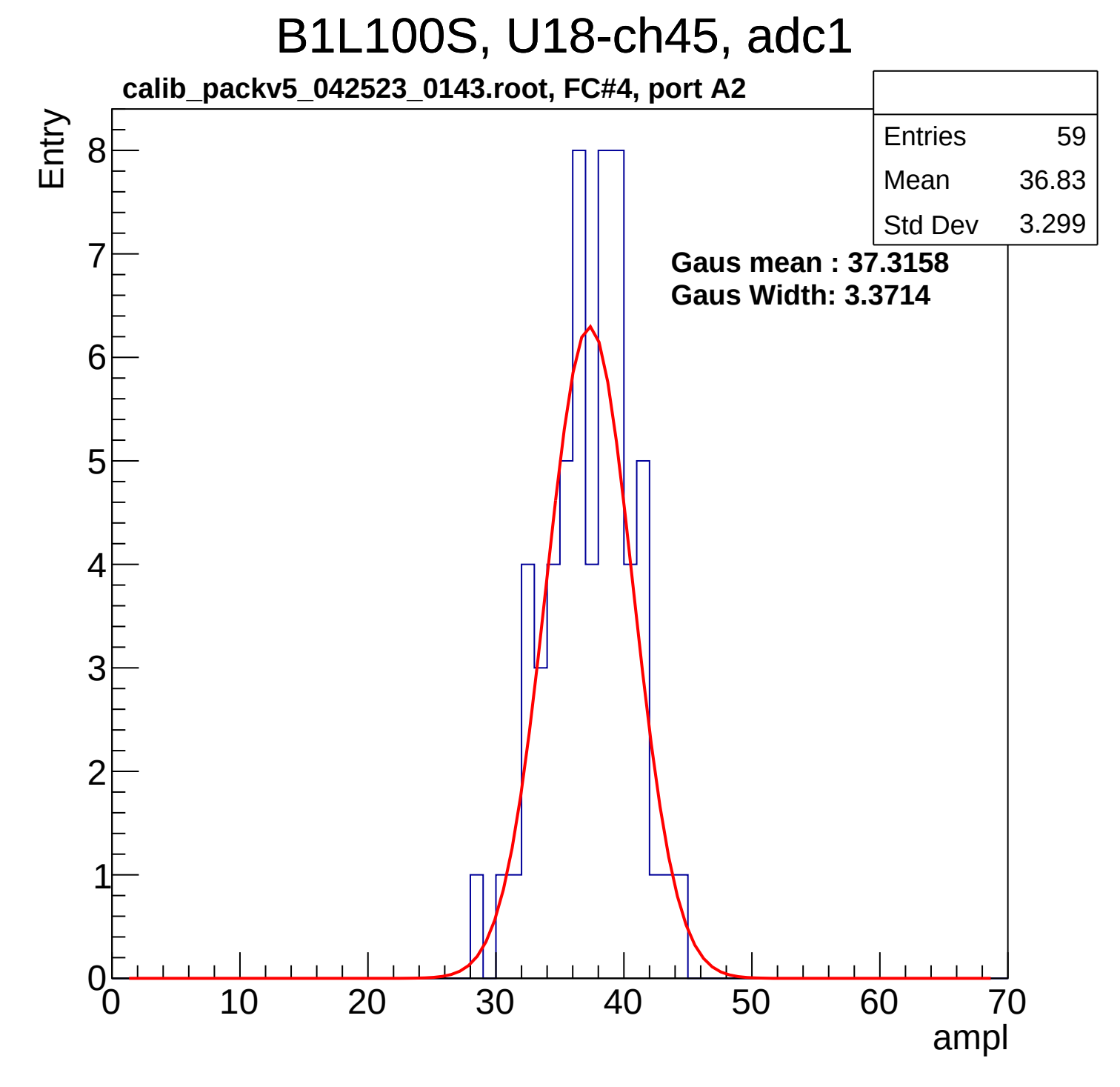

B1L100S, U18-ch44, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 55.44
Std Dev 3.175
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

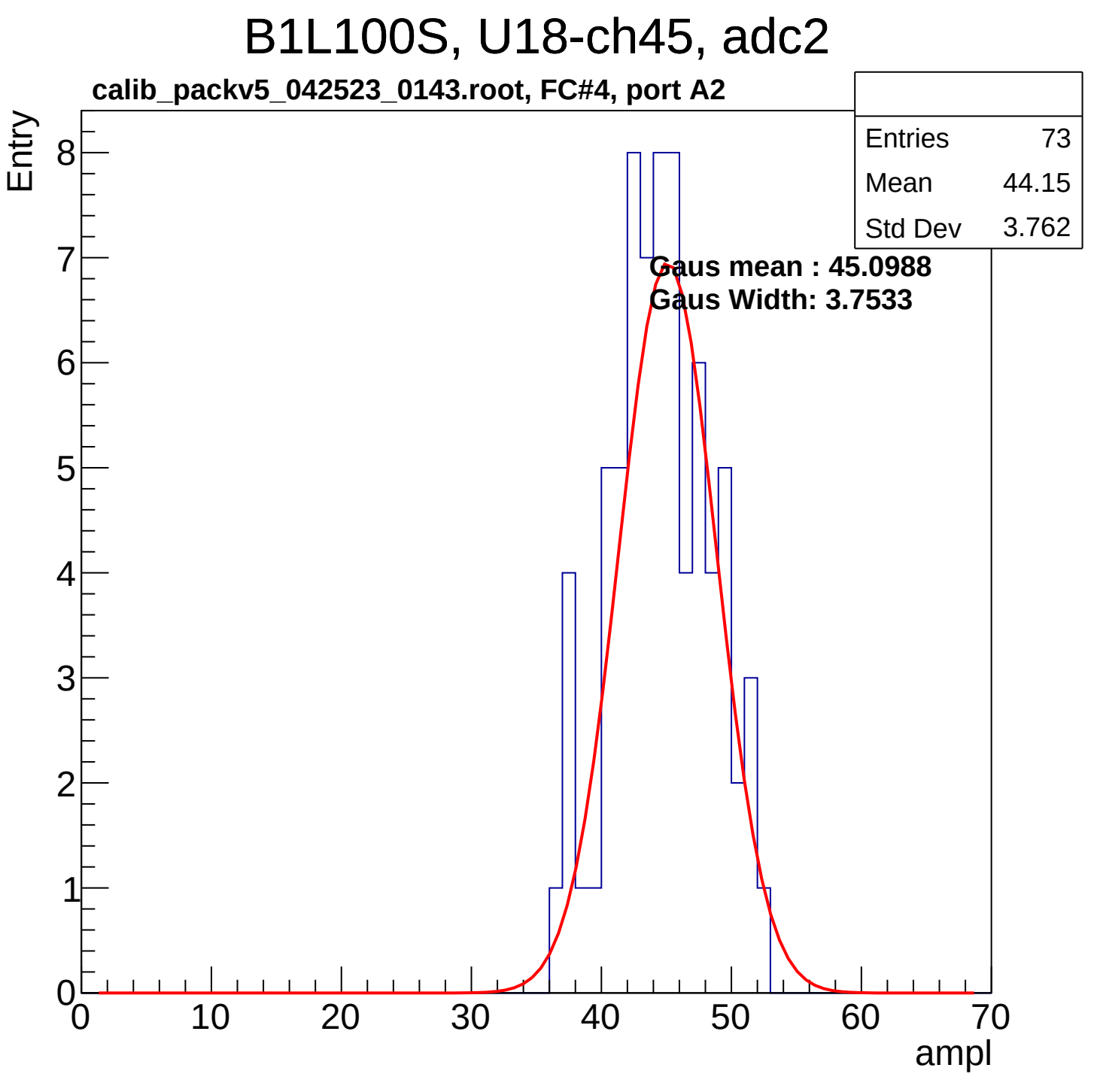

B1L100S, U18-ch44, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 58.5
Std Dev 8.879
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

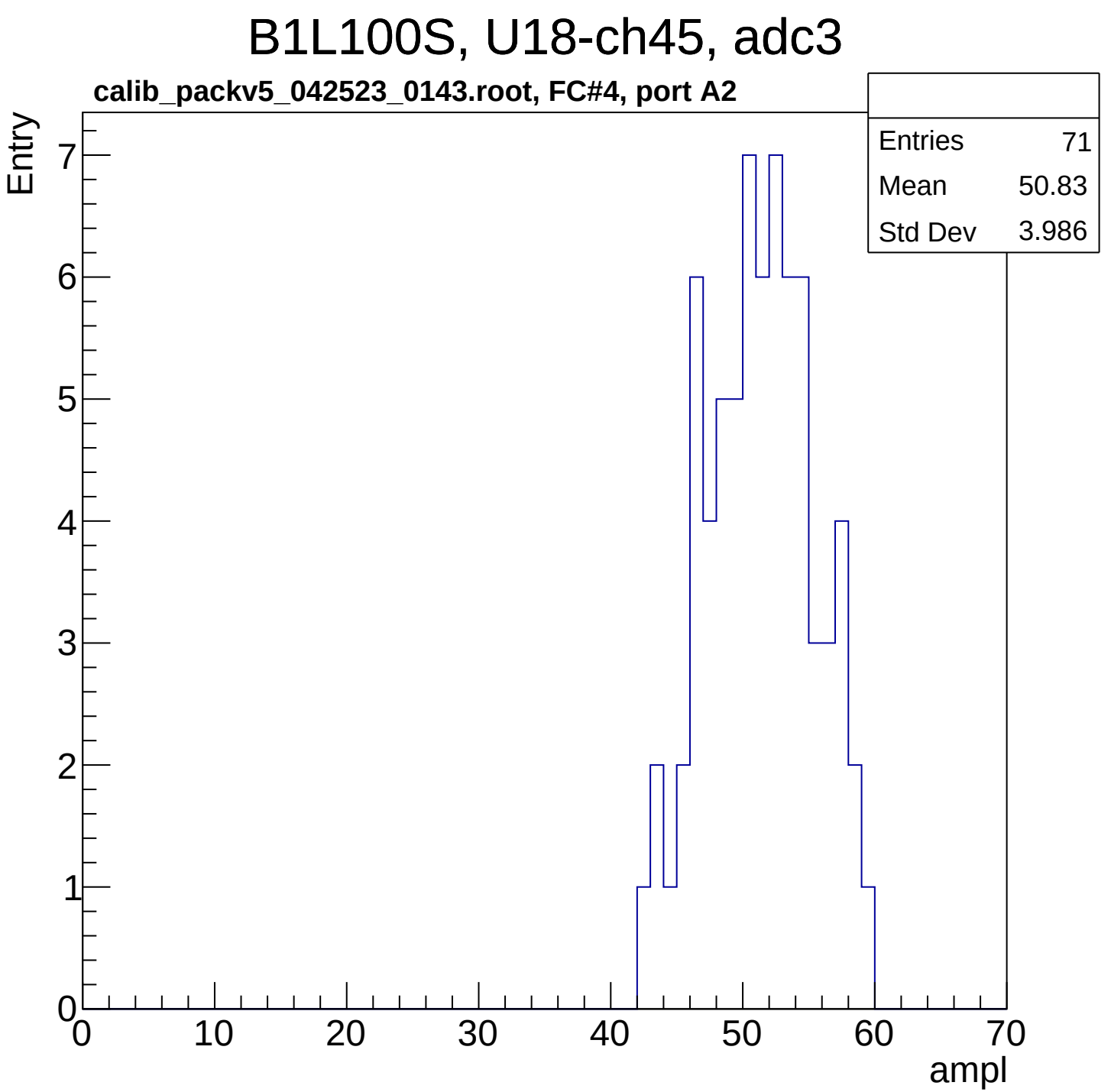

B1L100S, U18-ch44, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 61.67
Std Dev 0.7454
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

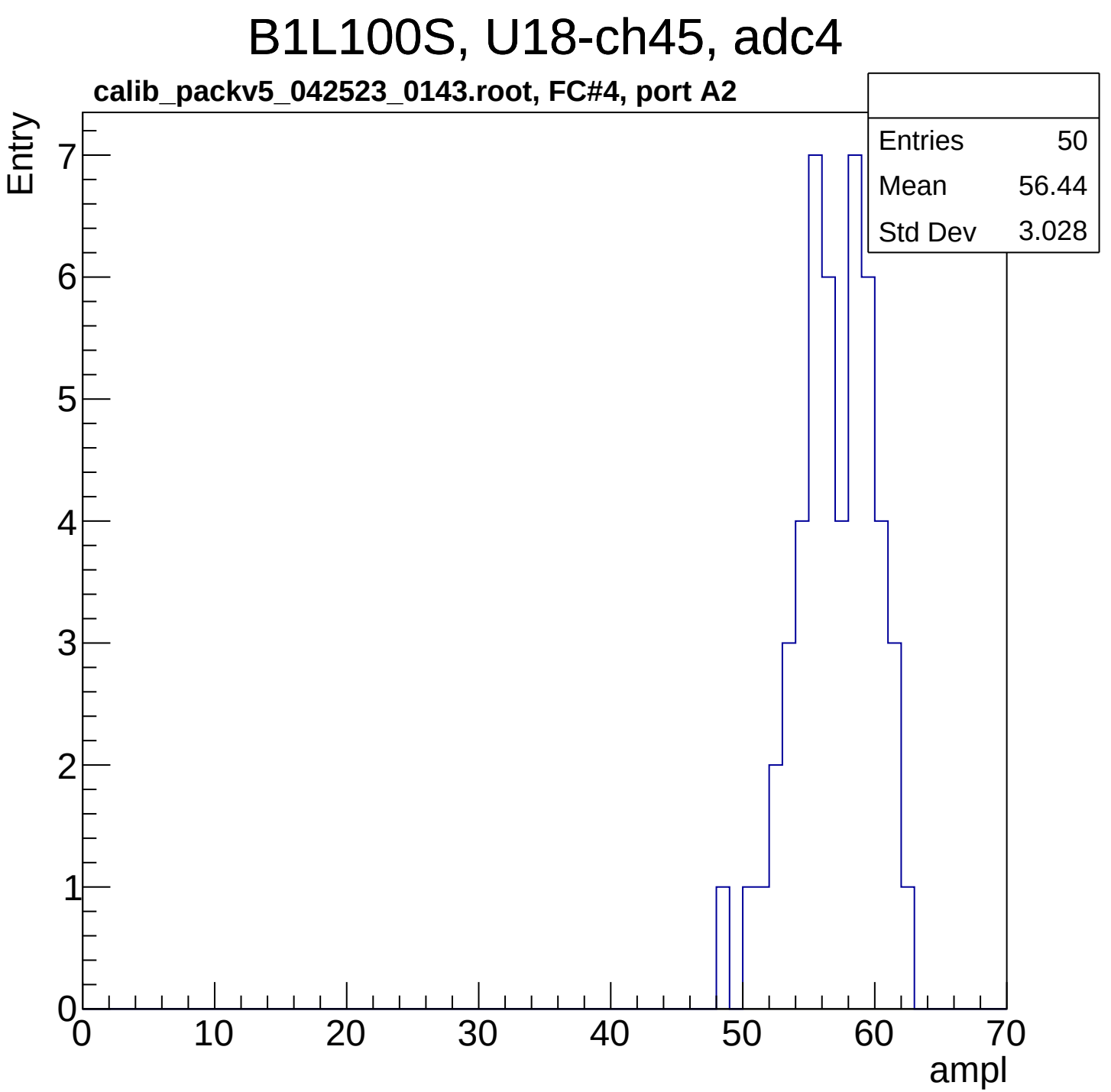

B1L100S, U18-ch44, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 19
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

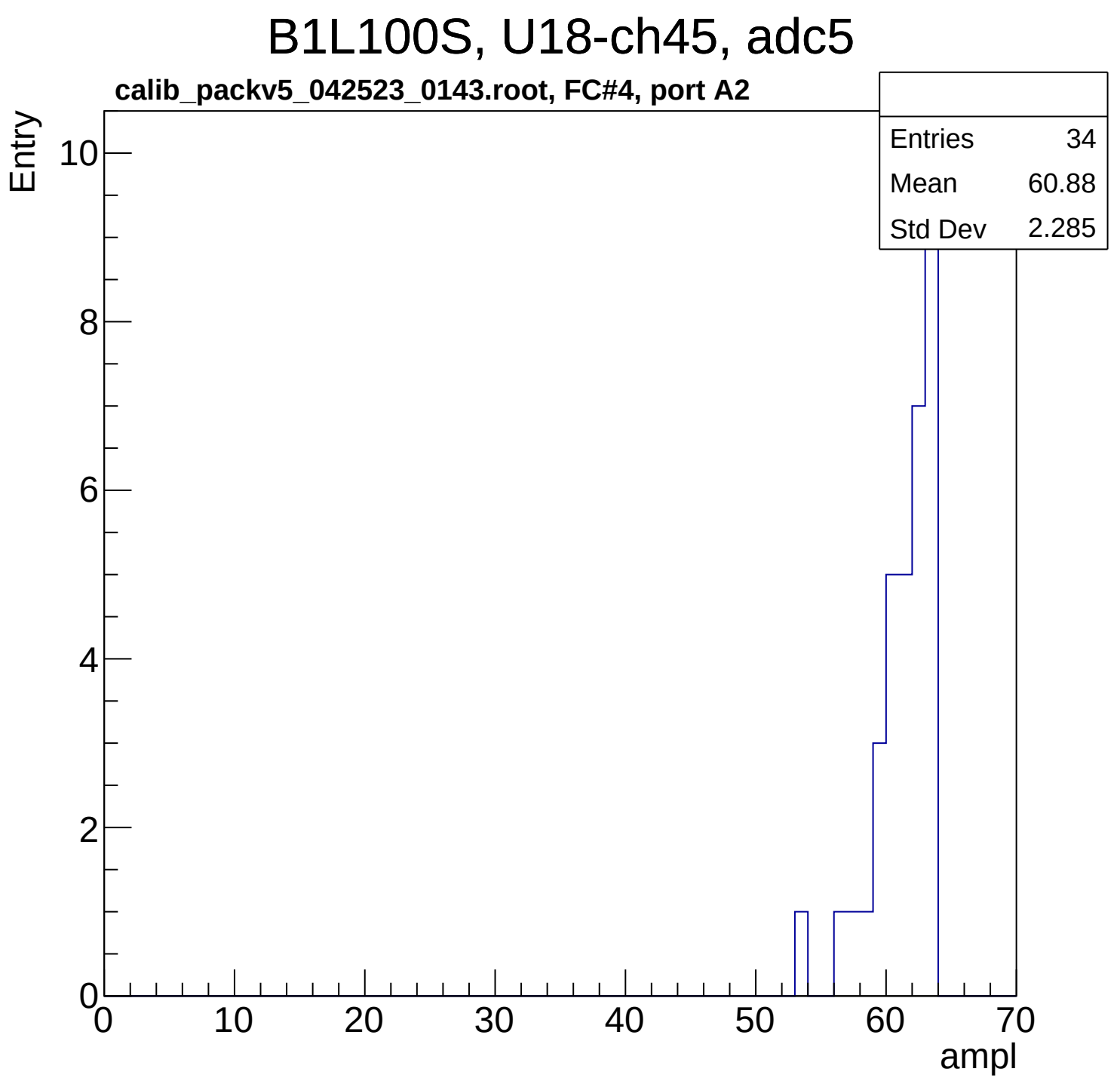

B1L100S, U18-ch45, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 30.89
Std Dev 3.625
Gaus mean : 31.2899
Gaus Width: 3.4395
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

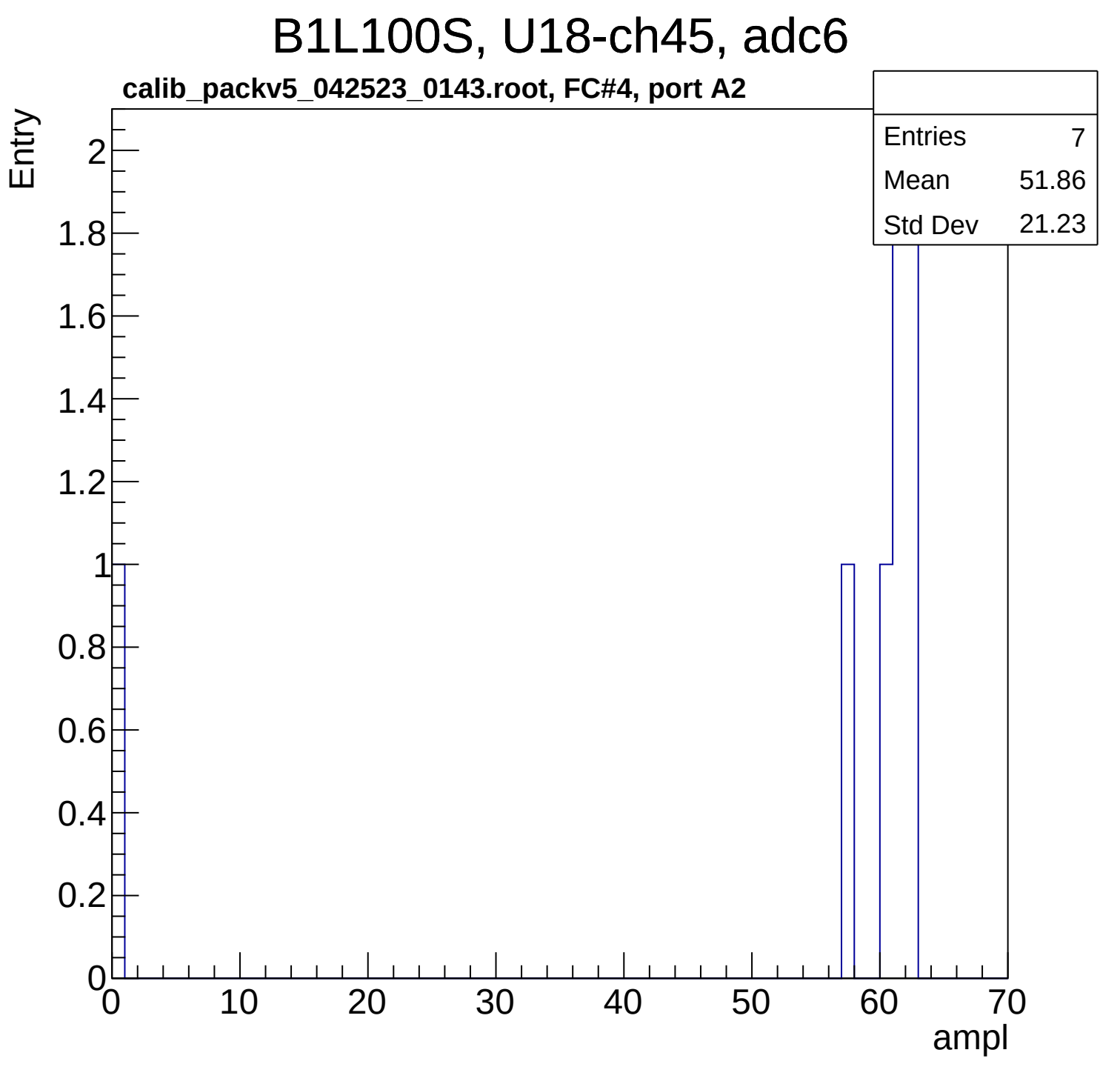

B1L100S, U18-ch45, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 36.83
Std Dev 3.299
Gaus mean : 37.3158
Gaus Width: 3.3714
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

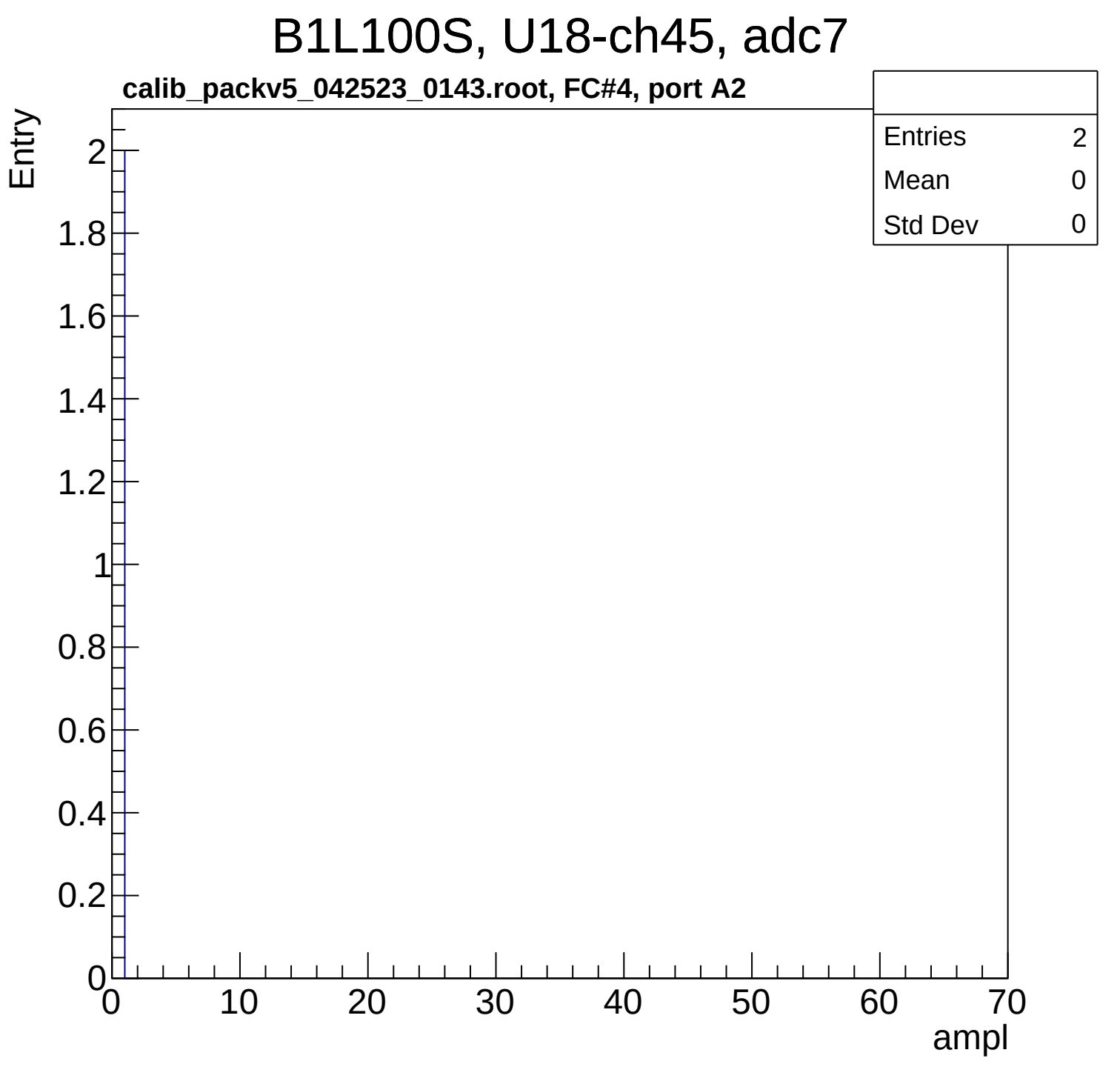

B1L100S, U18-ch45, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 44.15
Std Dev 3.762
Gaus mean : 45.0988
Gaus Width: 3.7533
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

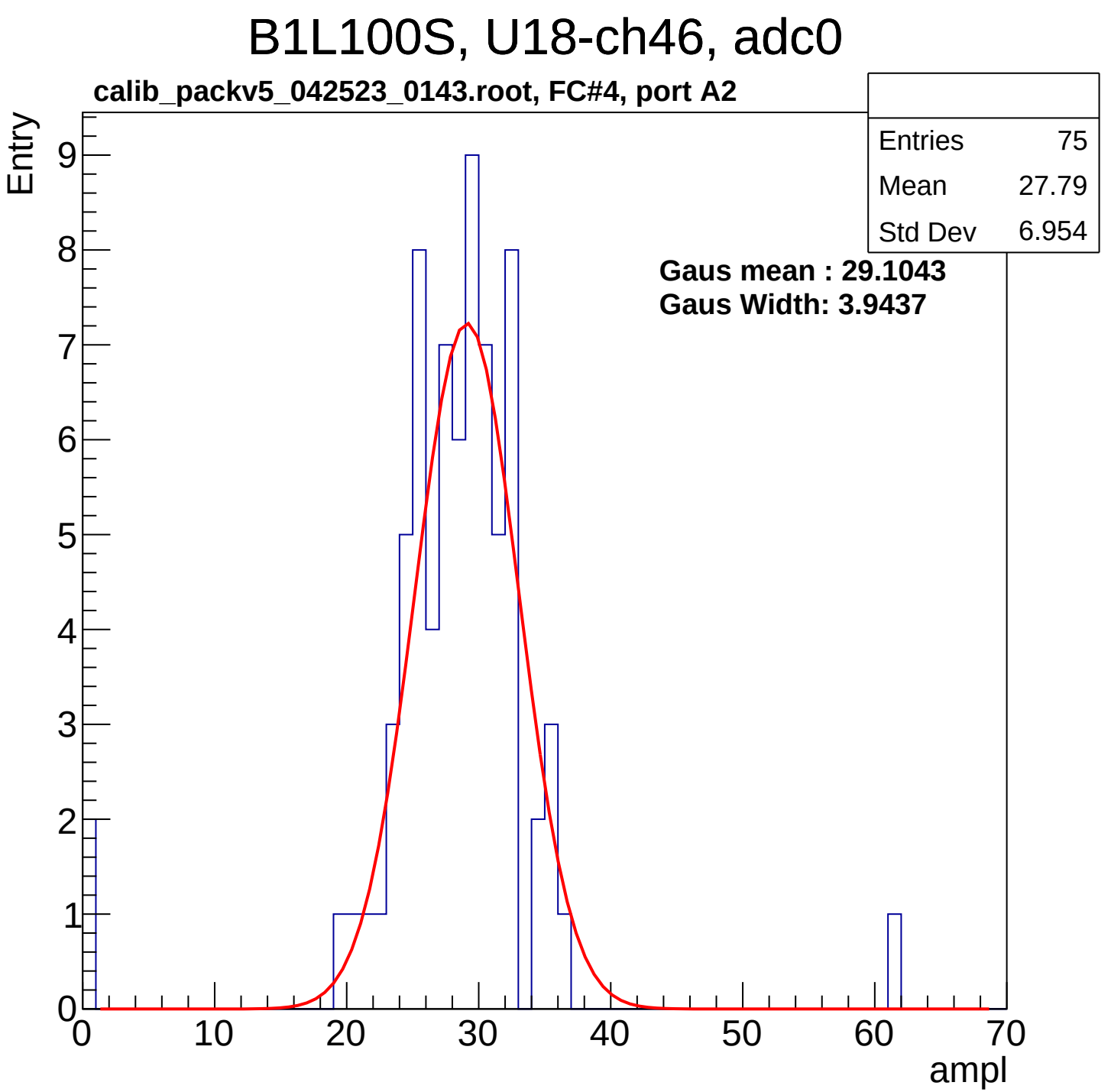

B1L100S, U18-ch45, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 50.83
Std Dev 3.986
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

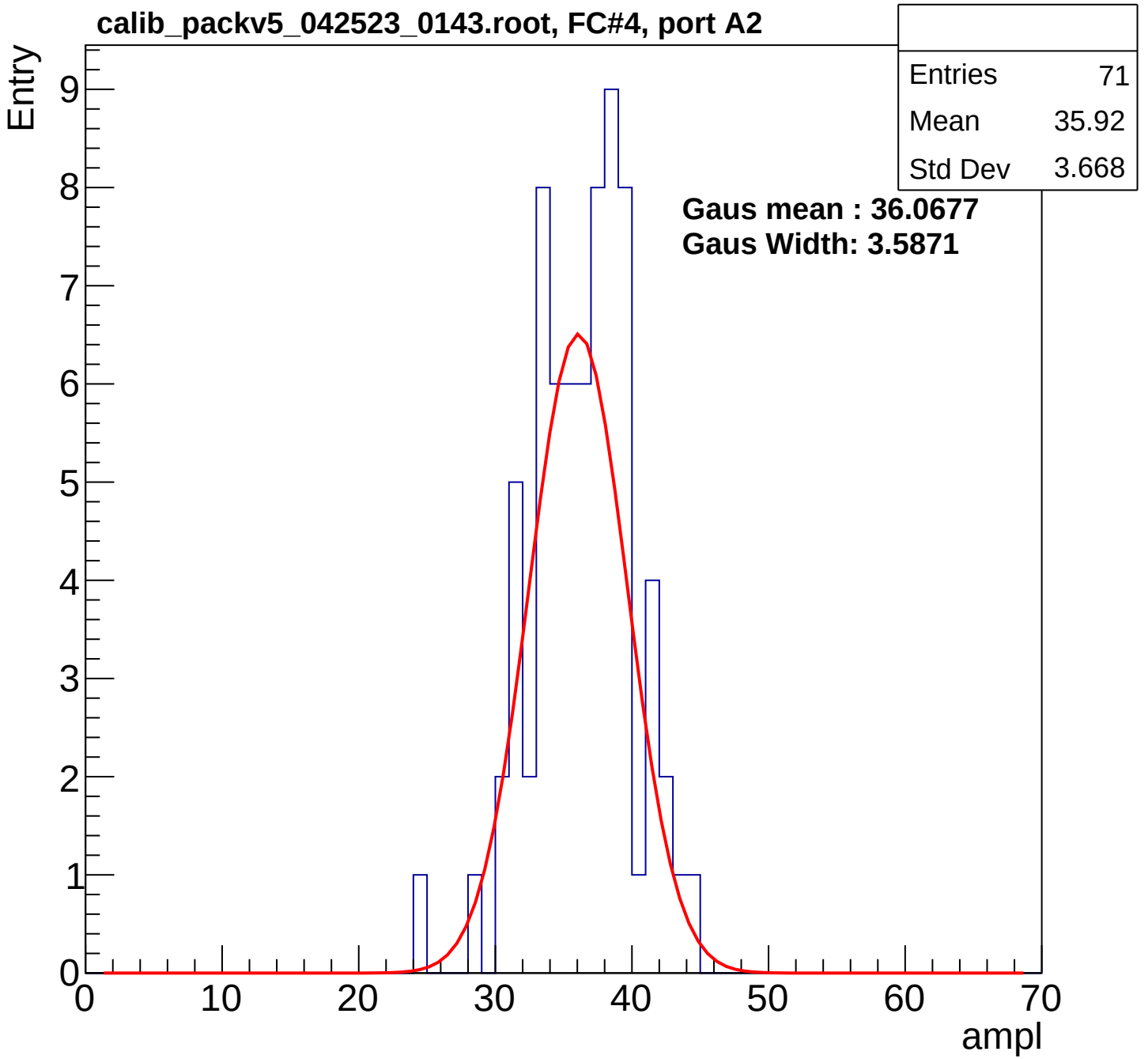

B1L100S, U18-ch45, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 56.44
Std Dev 3.028
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

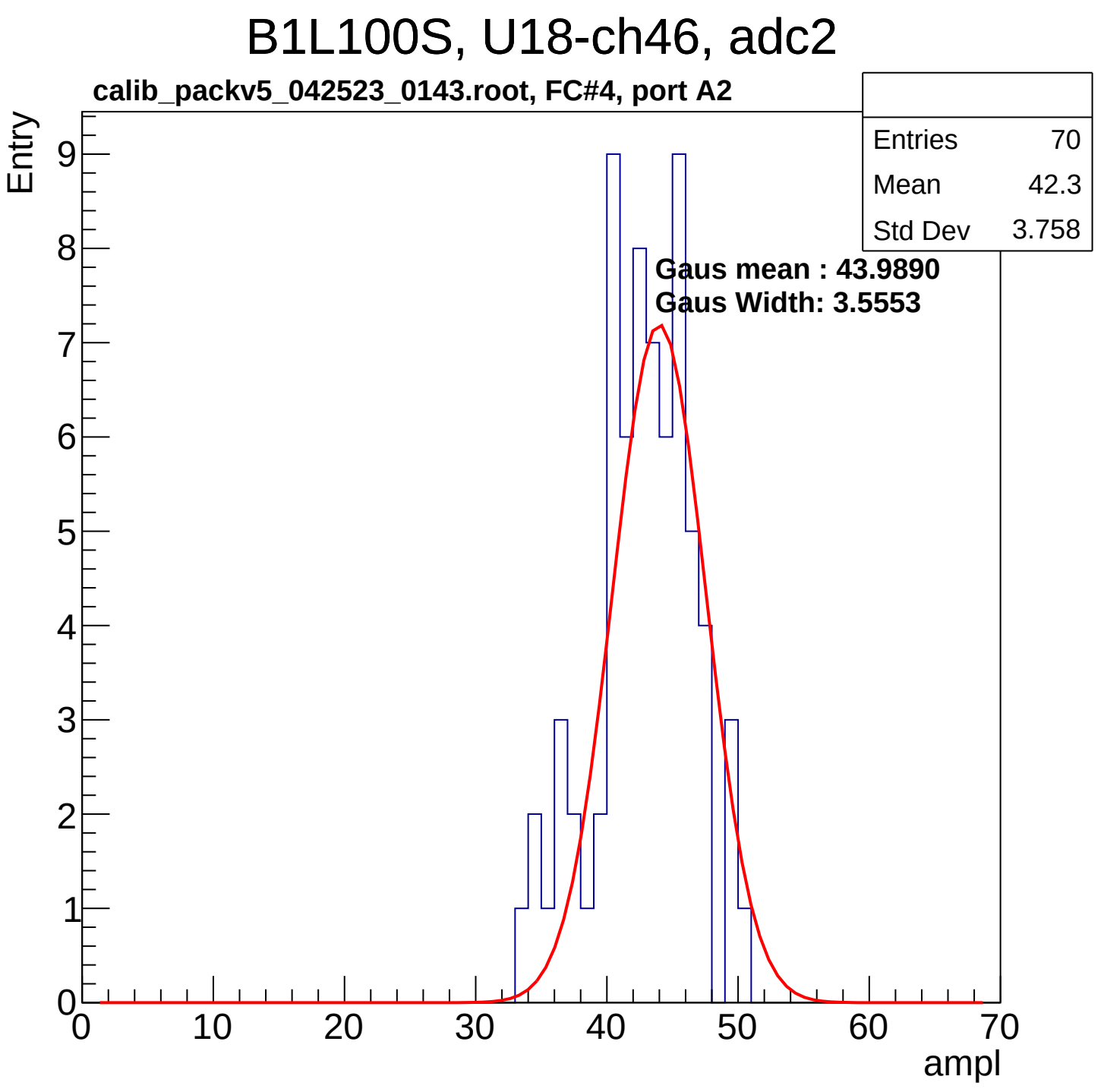

B1L100S, U18-ch45, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 34
Mean 60.88
Std Dev 2.285
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

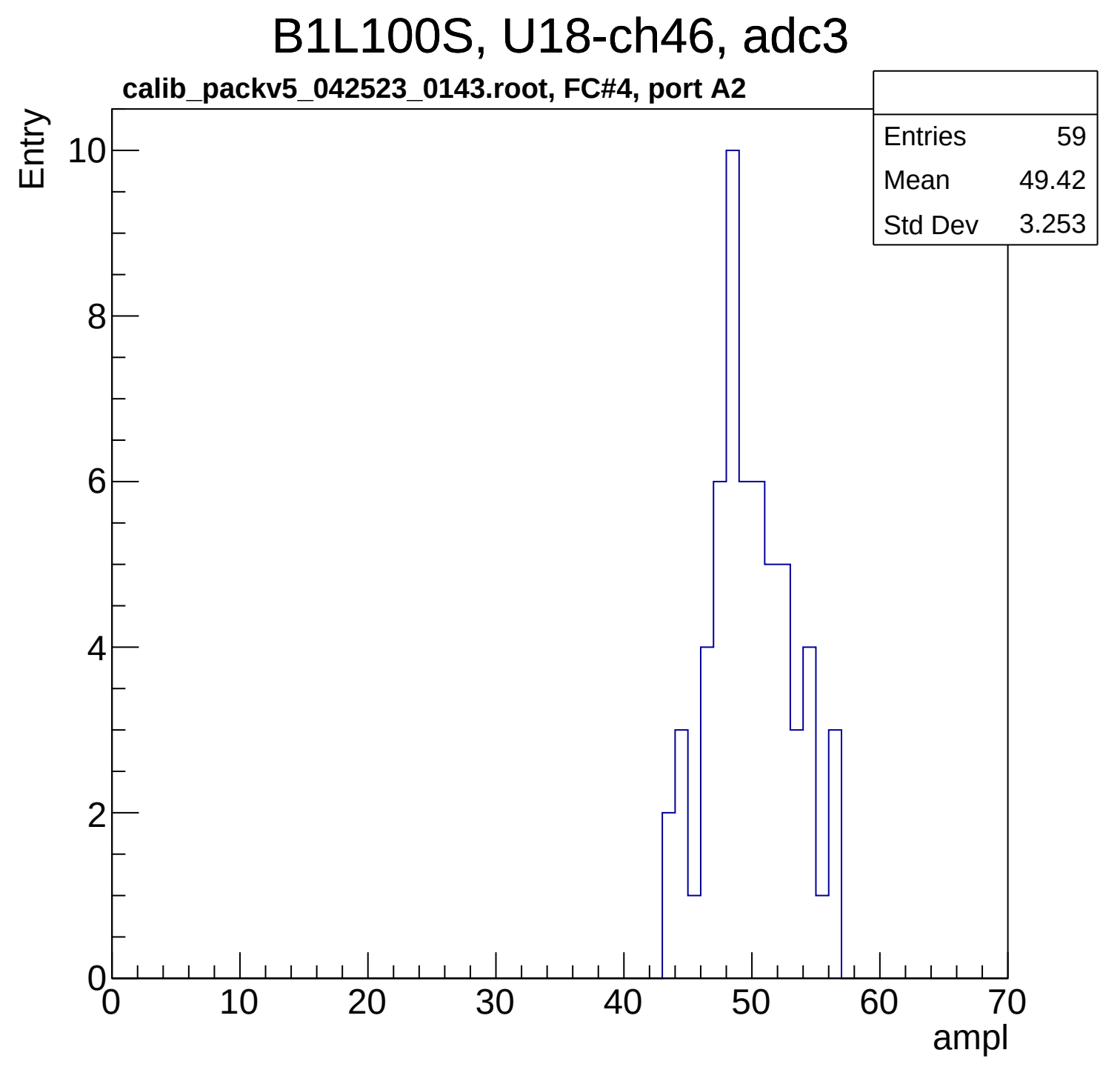

B1L100S, U18-ch45, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 51.86
Std Dev 21.23
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

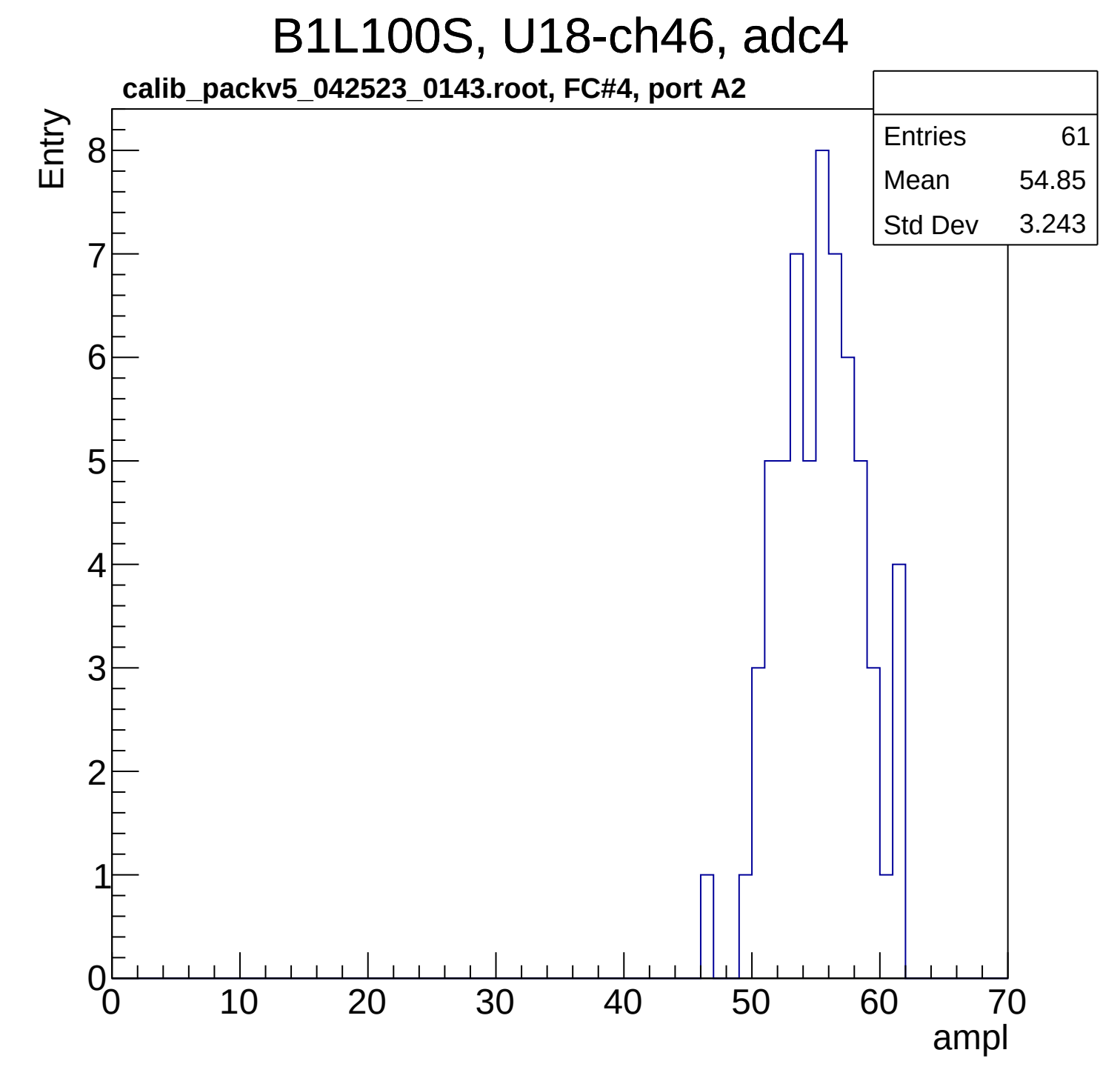

B1L100S, U18-ch45, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

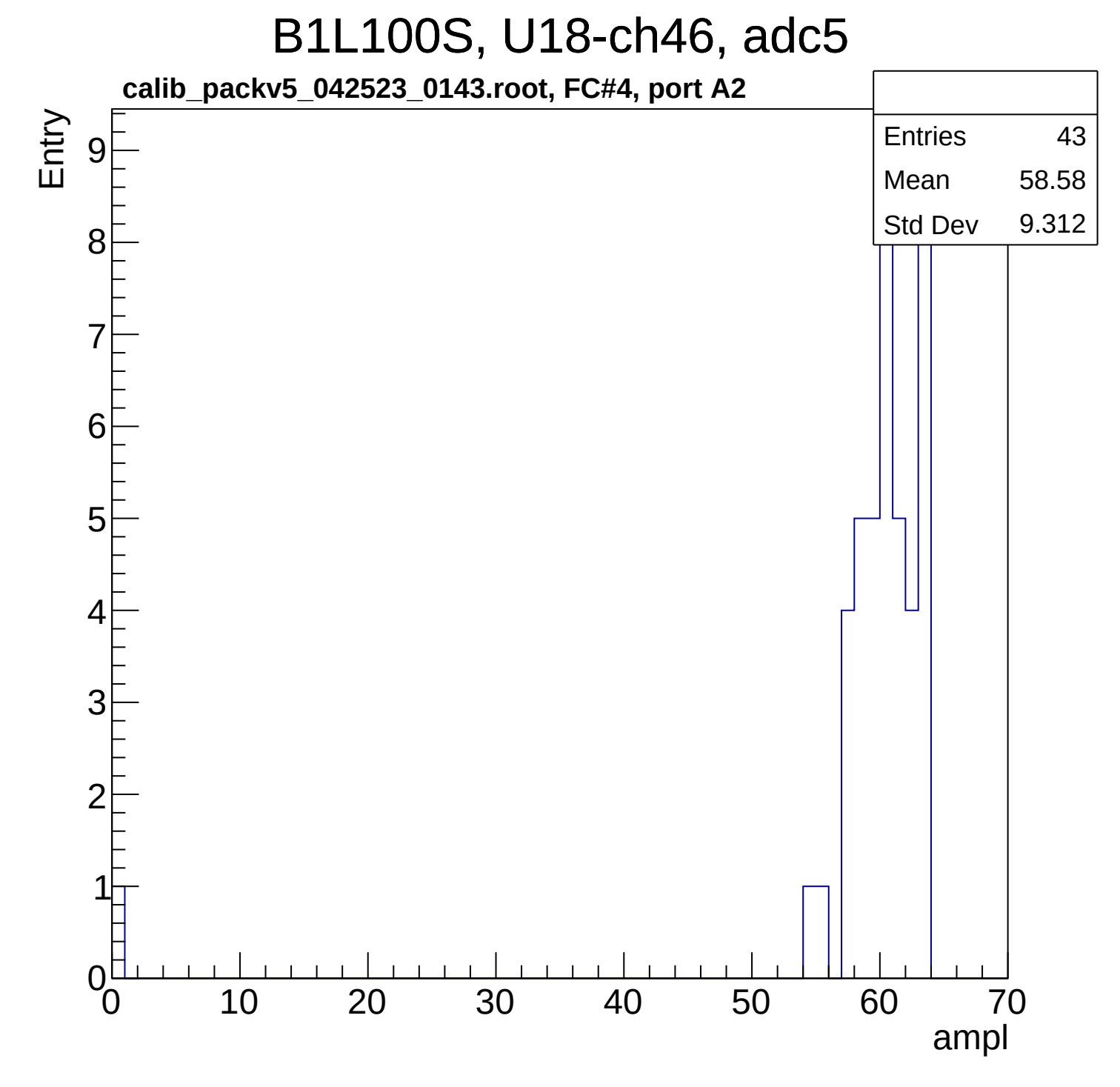

B1L100S, U18-ch46, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 27.79
Std Dev 6.954
Gaus mean : 29.1043
Gaus Width: 3.9437
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

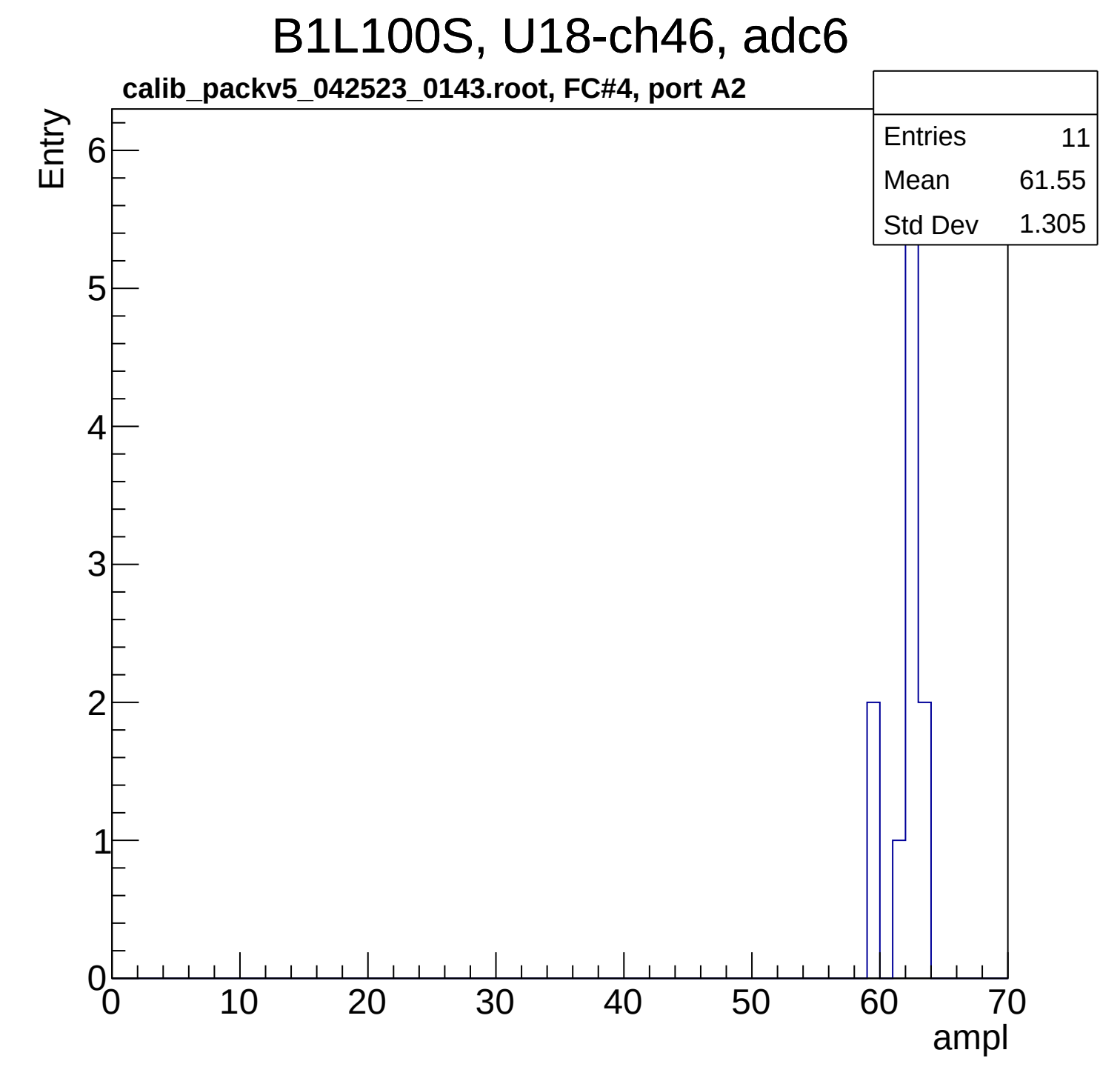

B1L100S, U18-ch46, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 35.92
Std Dev 3.668
Gaus mean : 36.0677
Gaus Width: 3.5871
Entry
ampl
0
10
20
30
40
50
60
70
1
2
3
4
5
6
7
8
9

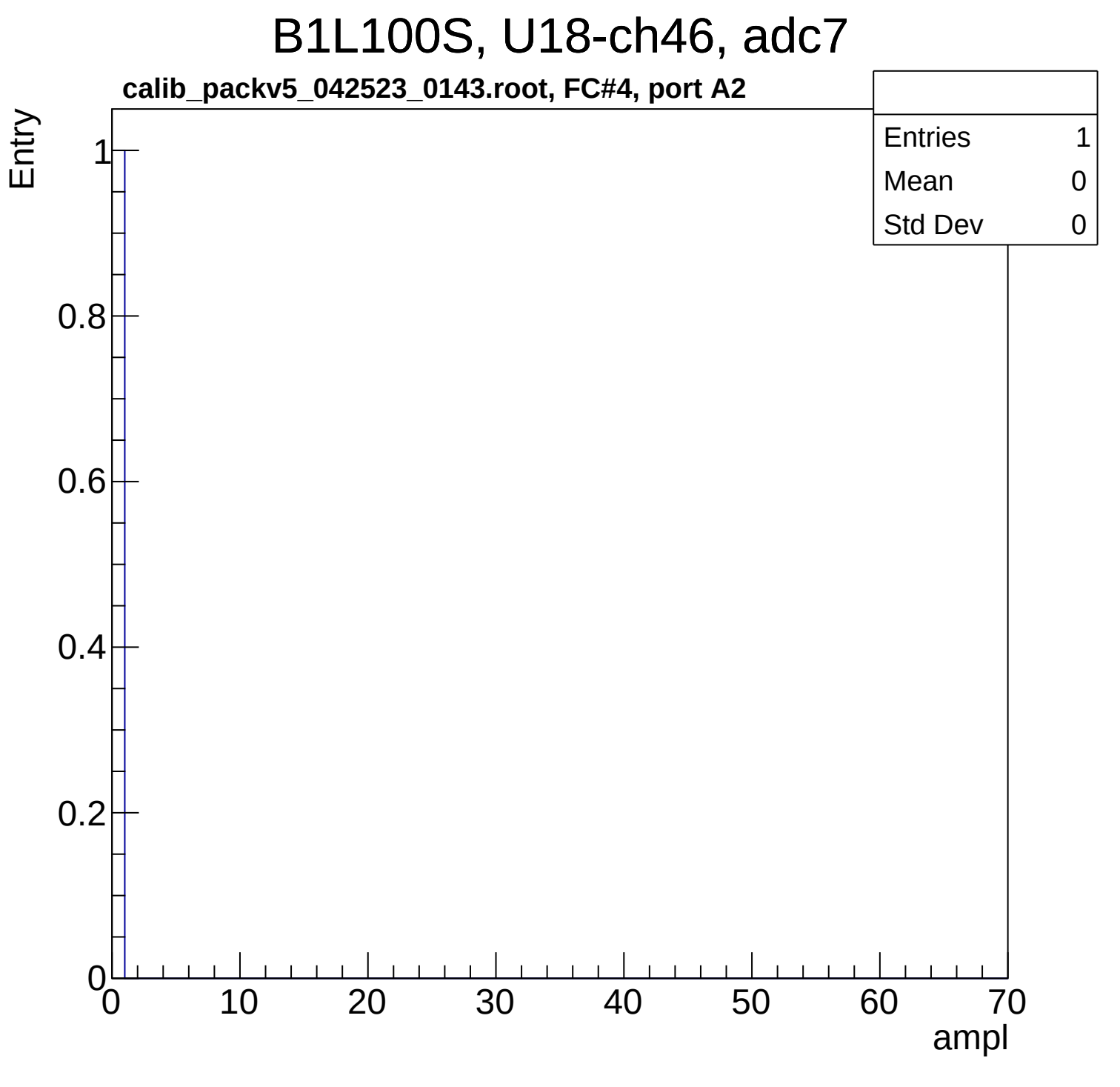

B1L100S, U18-ch46, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 42.3
Std Dev 3.758
Gaus mean : 43.9890
Gaus Width: 3.5553
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

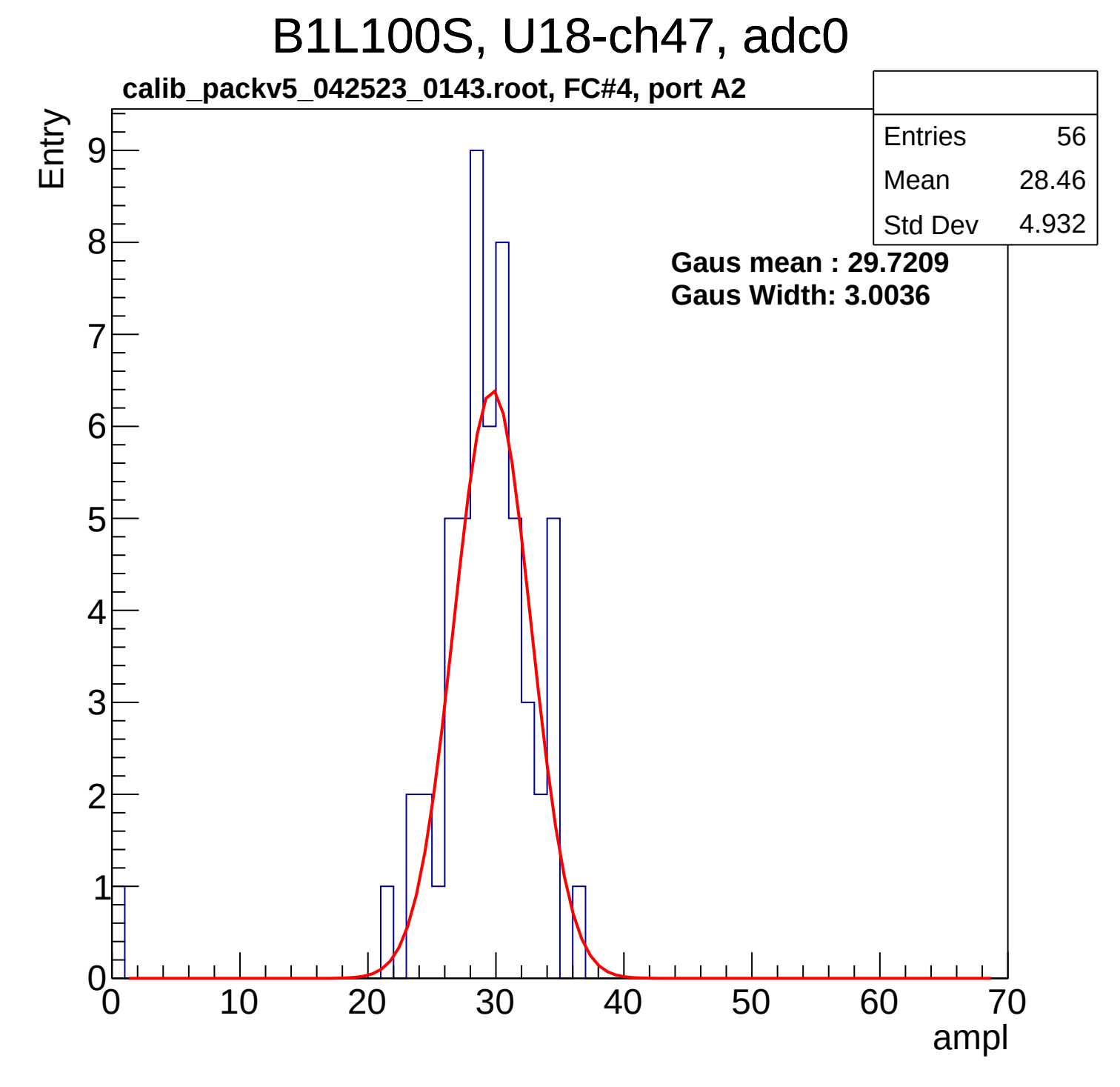

B1L100S, U18-ch46, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 49.42
Std Dev 3.253
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

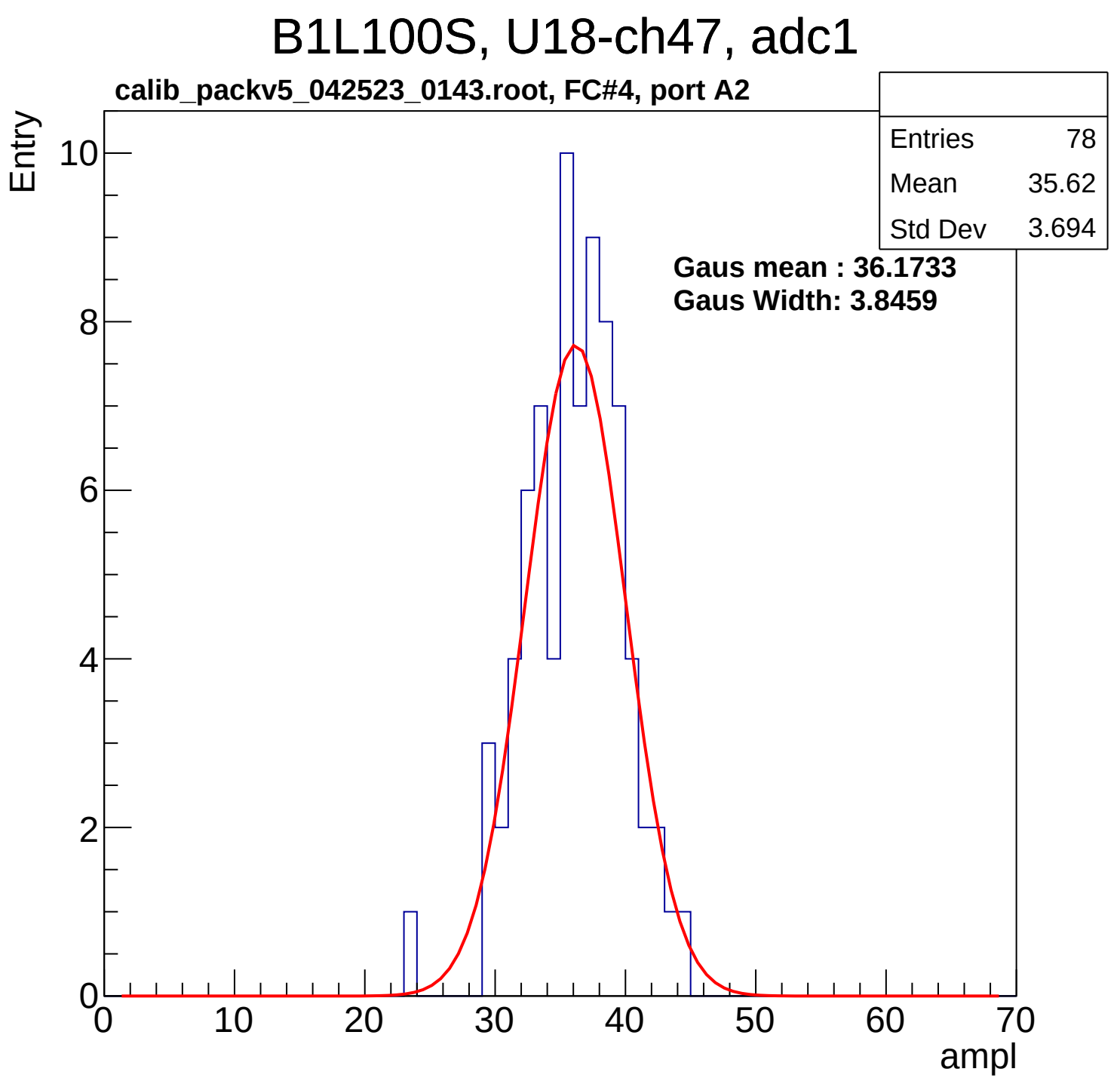

B1L100S, U18-ch46, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 54.85
Std Dev 3.243
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

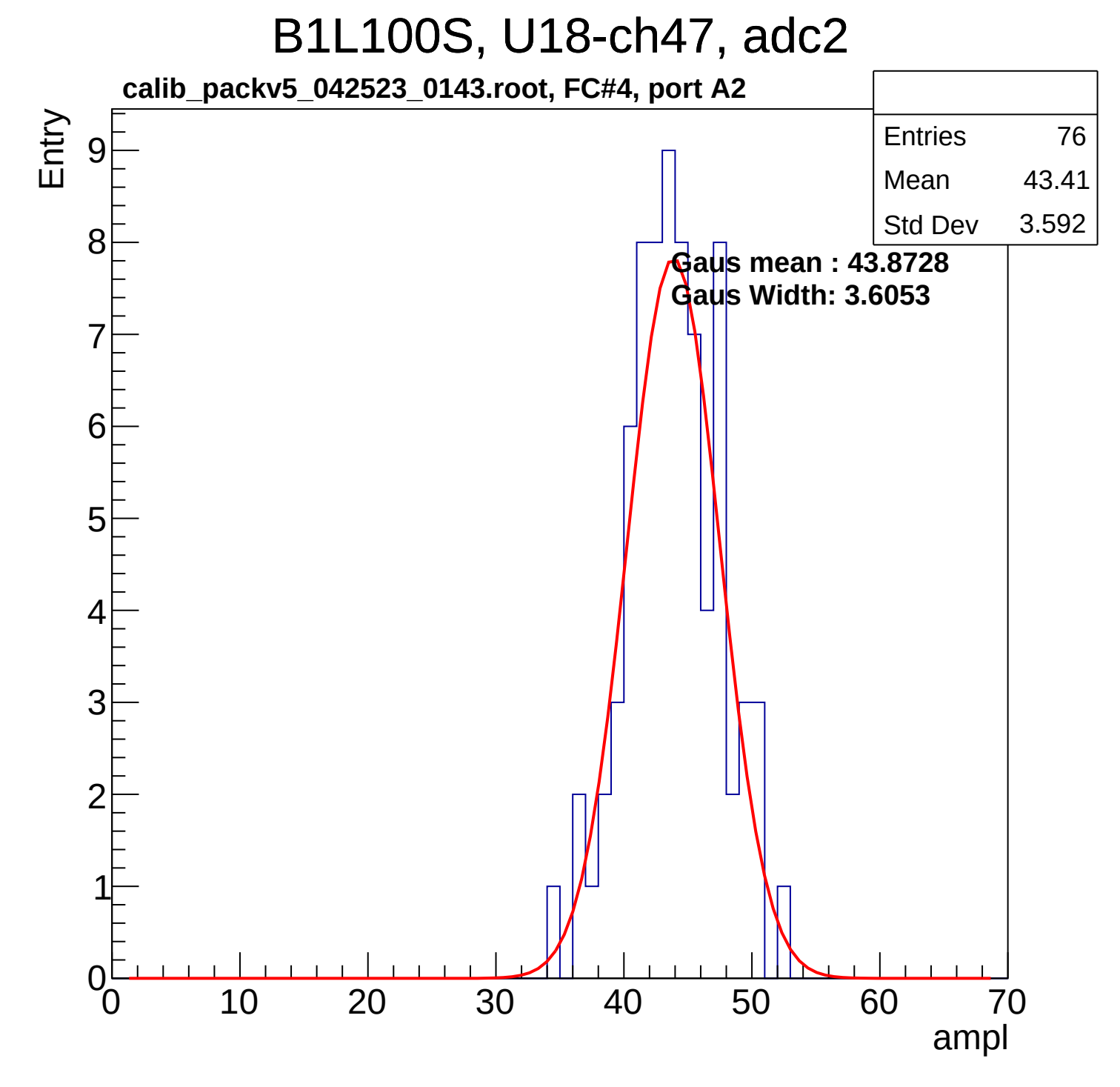

B1L100S, U18-ch46, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 58.58
Std Dev 9.312
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

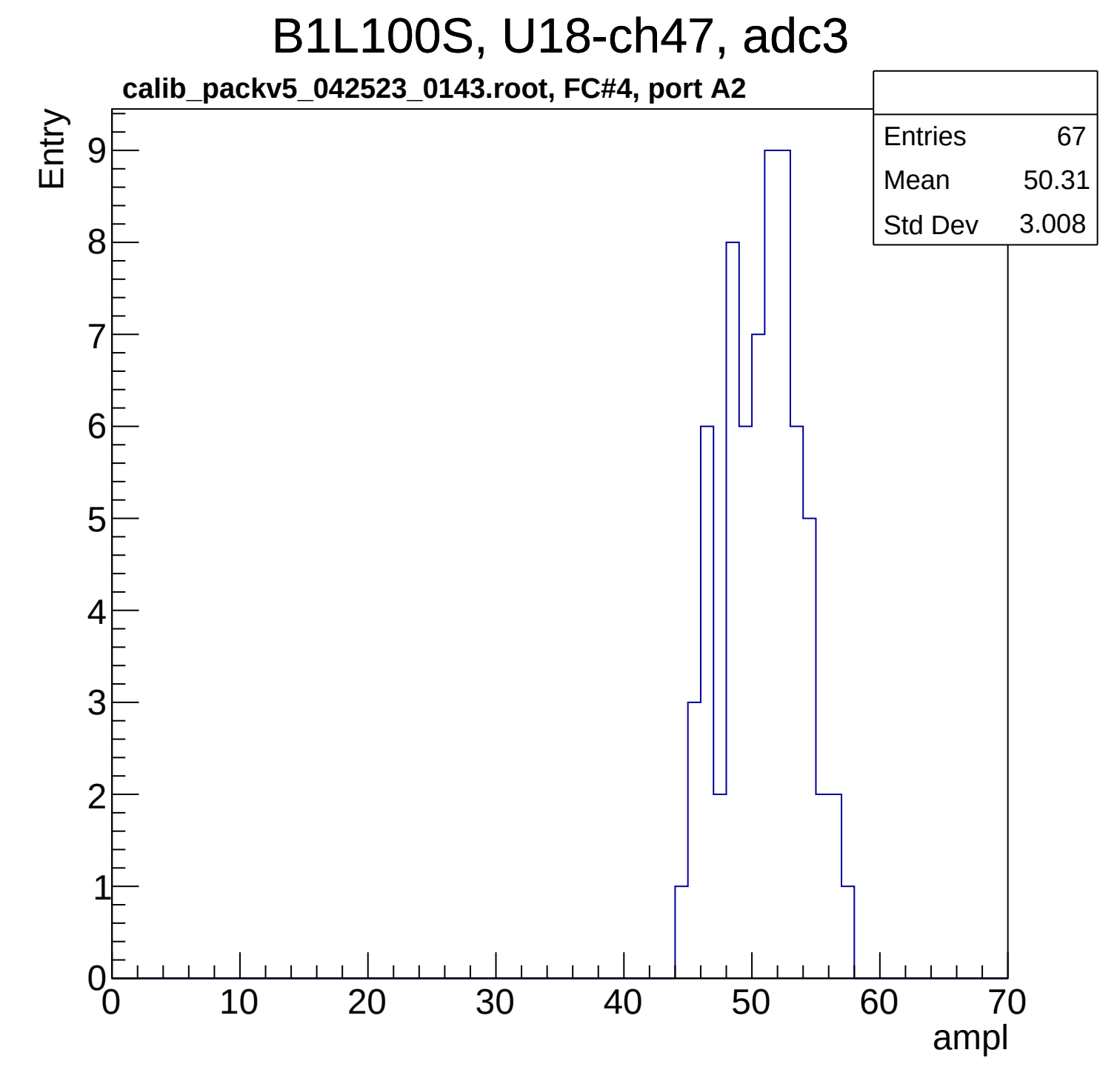

B1L100S, U18-ch46, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 61.55
Std Dev 1.305
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

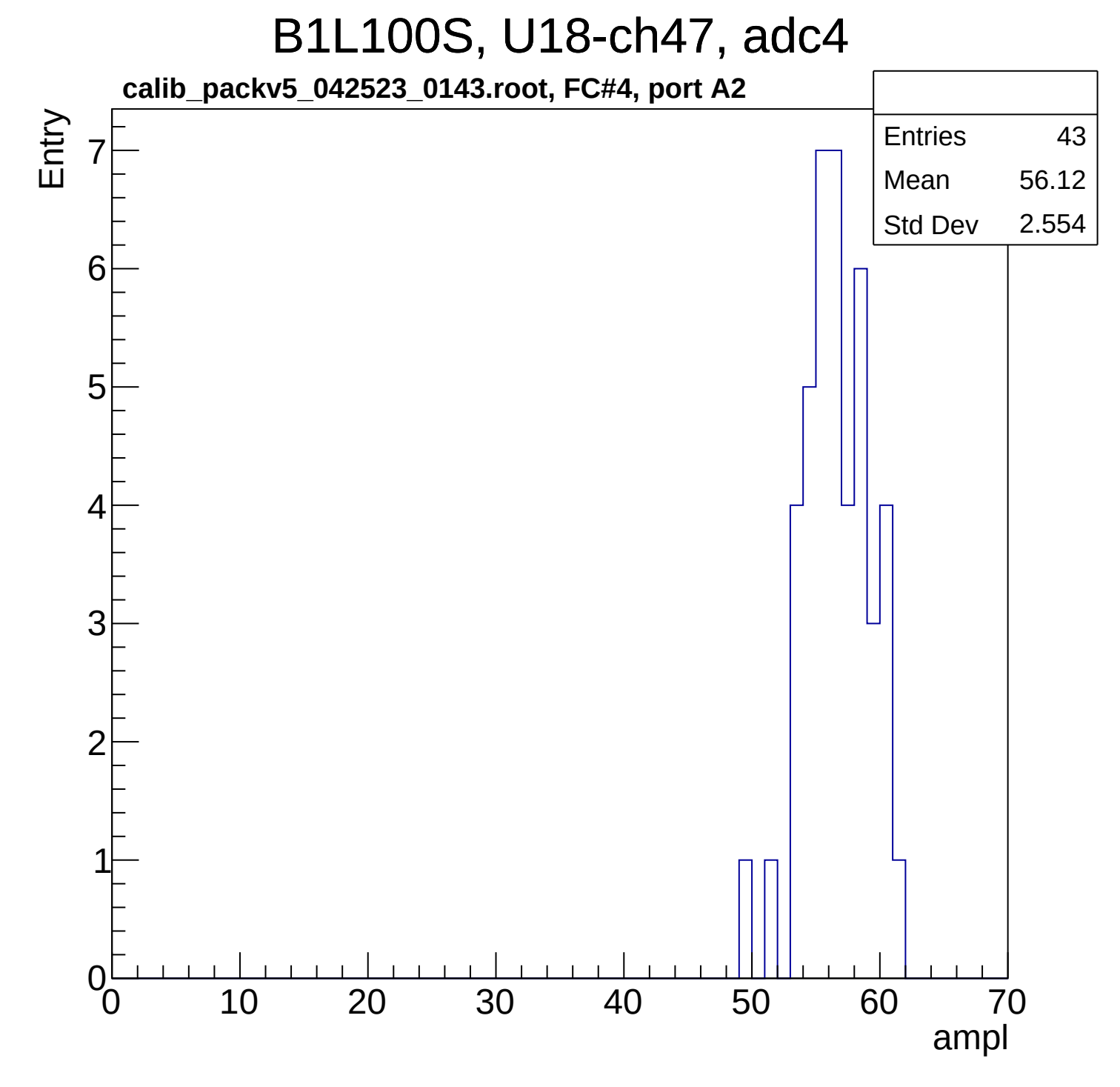

B1L100S, U18-ch46, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

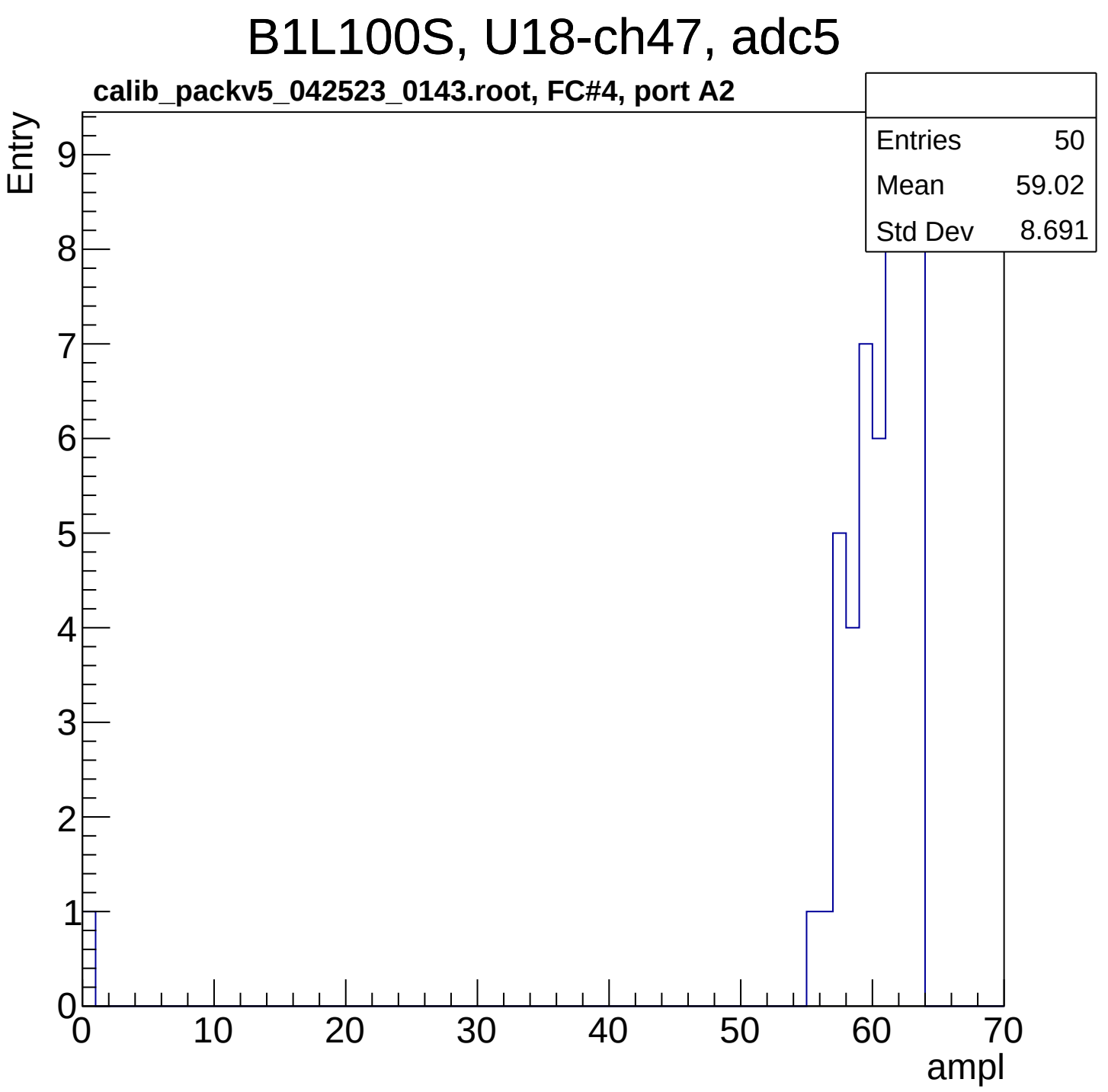

B1L100S, U18-ch47, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 28.46
Std Dev 4.932
Gaus mean : 29.7209
Gaus Width: 3.0036
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

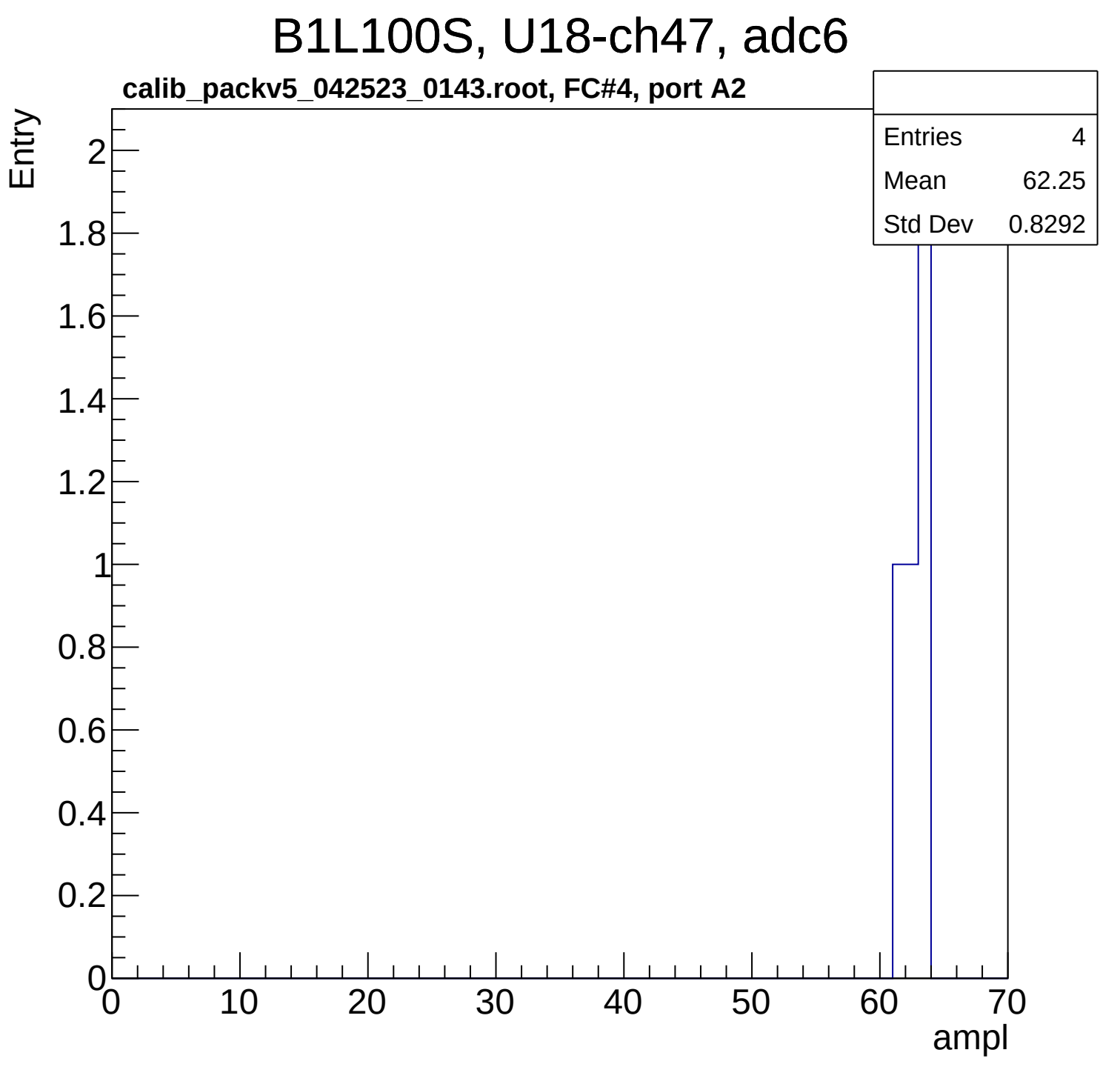

B1L100S, U18-ch47, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 35.62
Std Dev 3.694
Gaus mean : 36.1733
Gaus Width: 3.8459
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

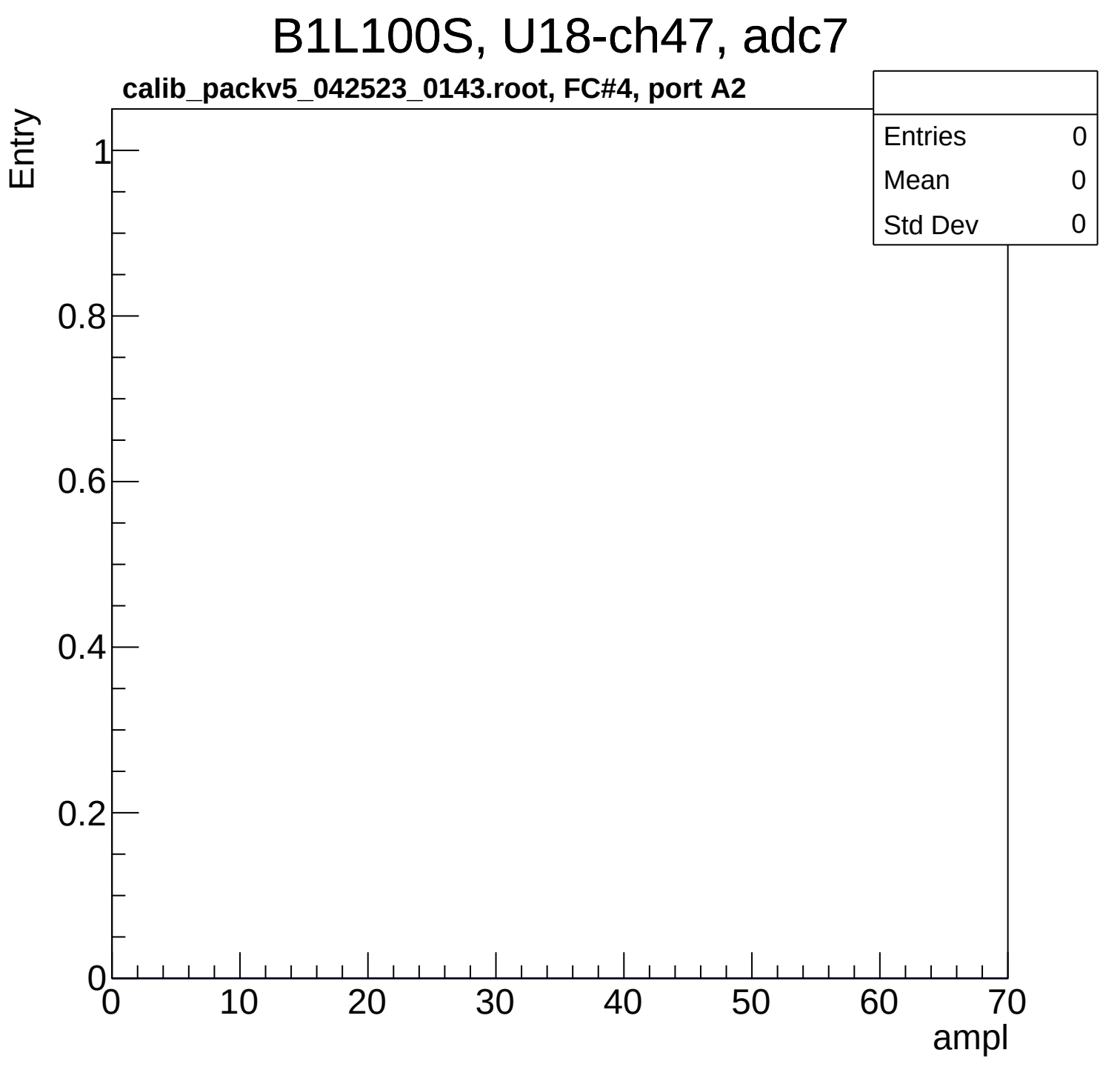

B1L100S, U18-ch47, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 43.41
Std Dev 3.592
Gaus mean : 43.8728
Gaus Width: 3.6053
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

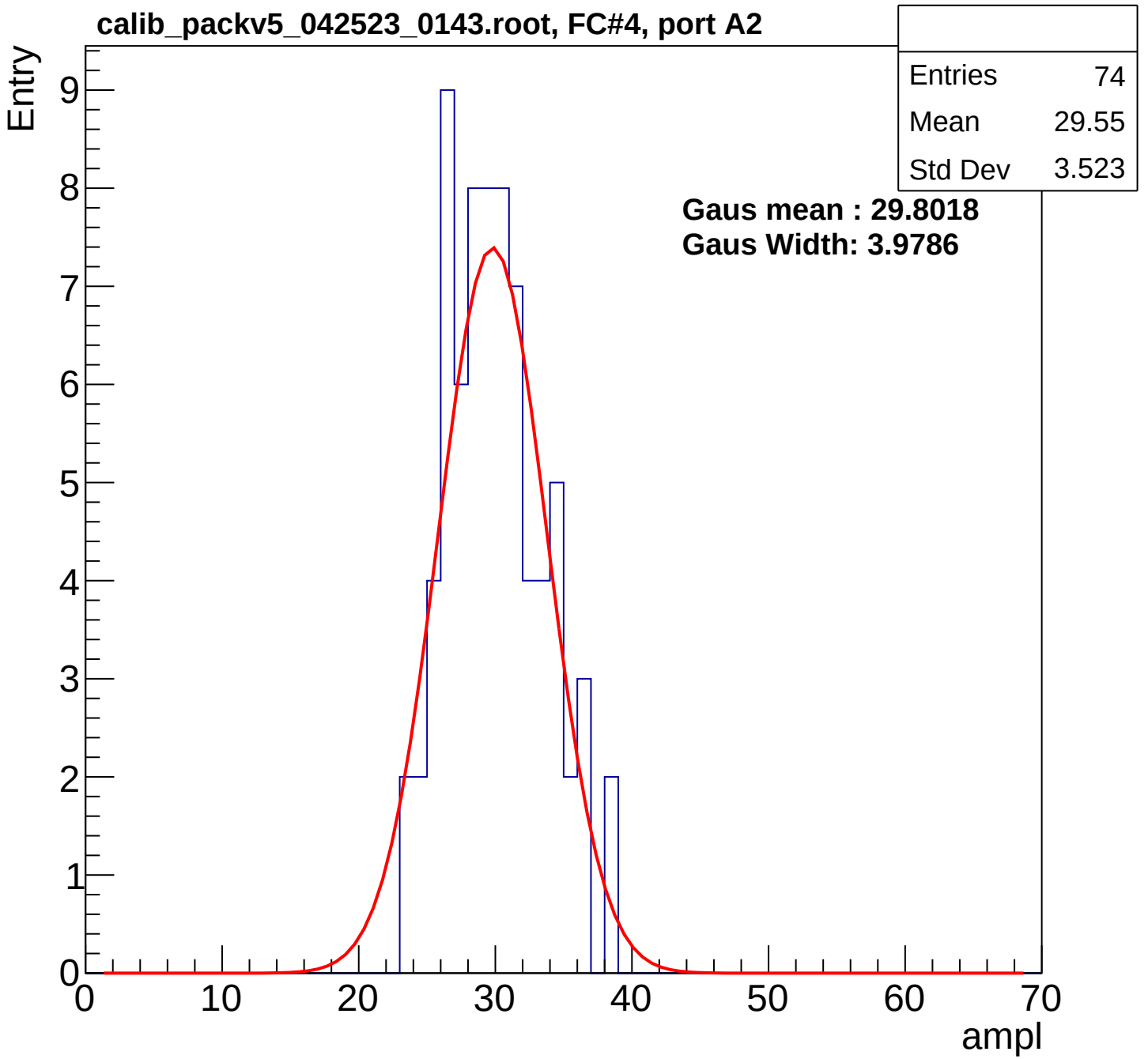

B1L100S, U18-ch47, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 50.31
Std Dev 3.008
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

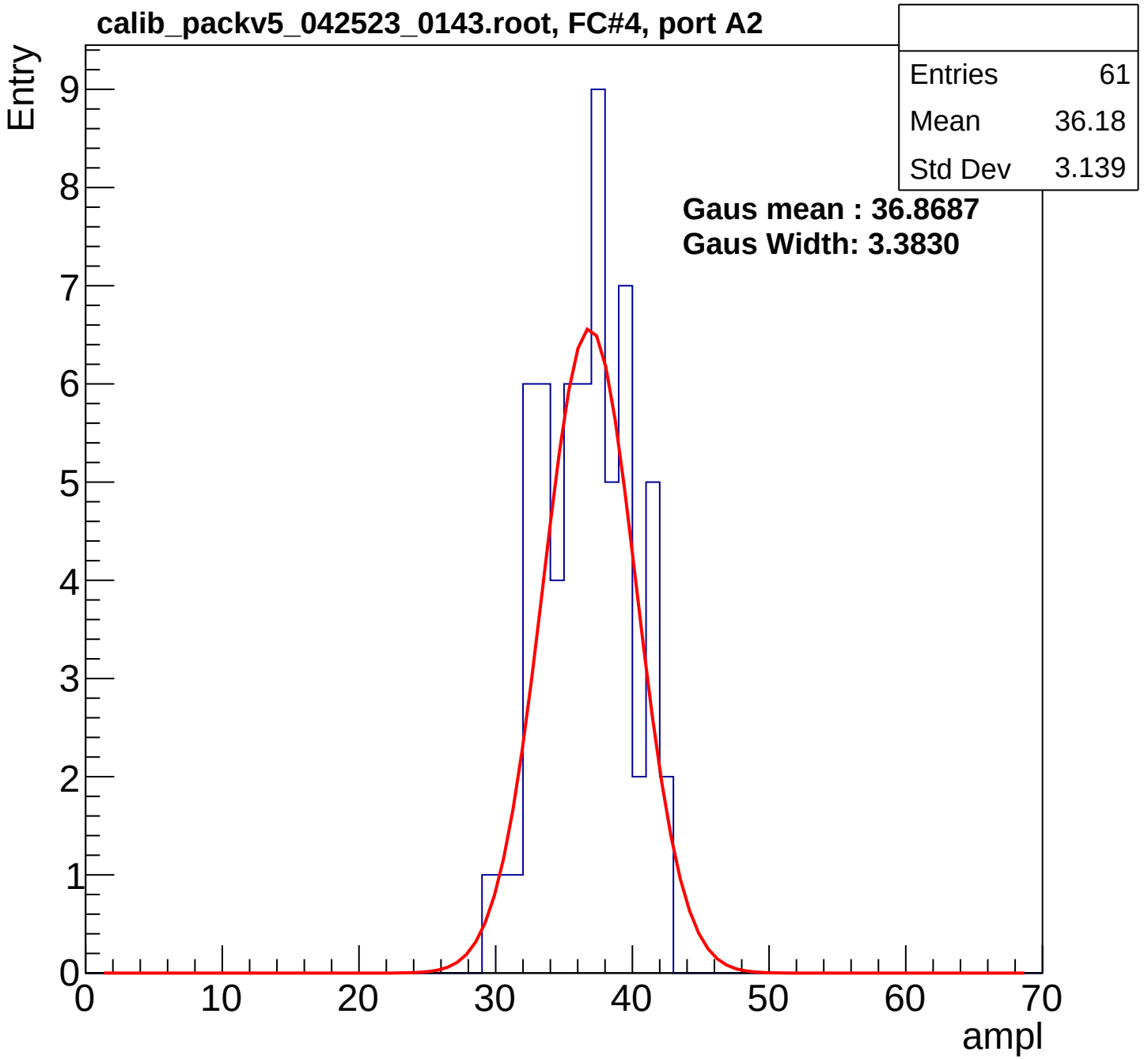

B1L100S, U18-ch47, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 56.12
Std Dev 2.554
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

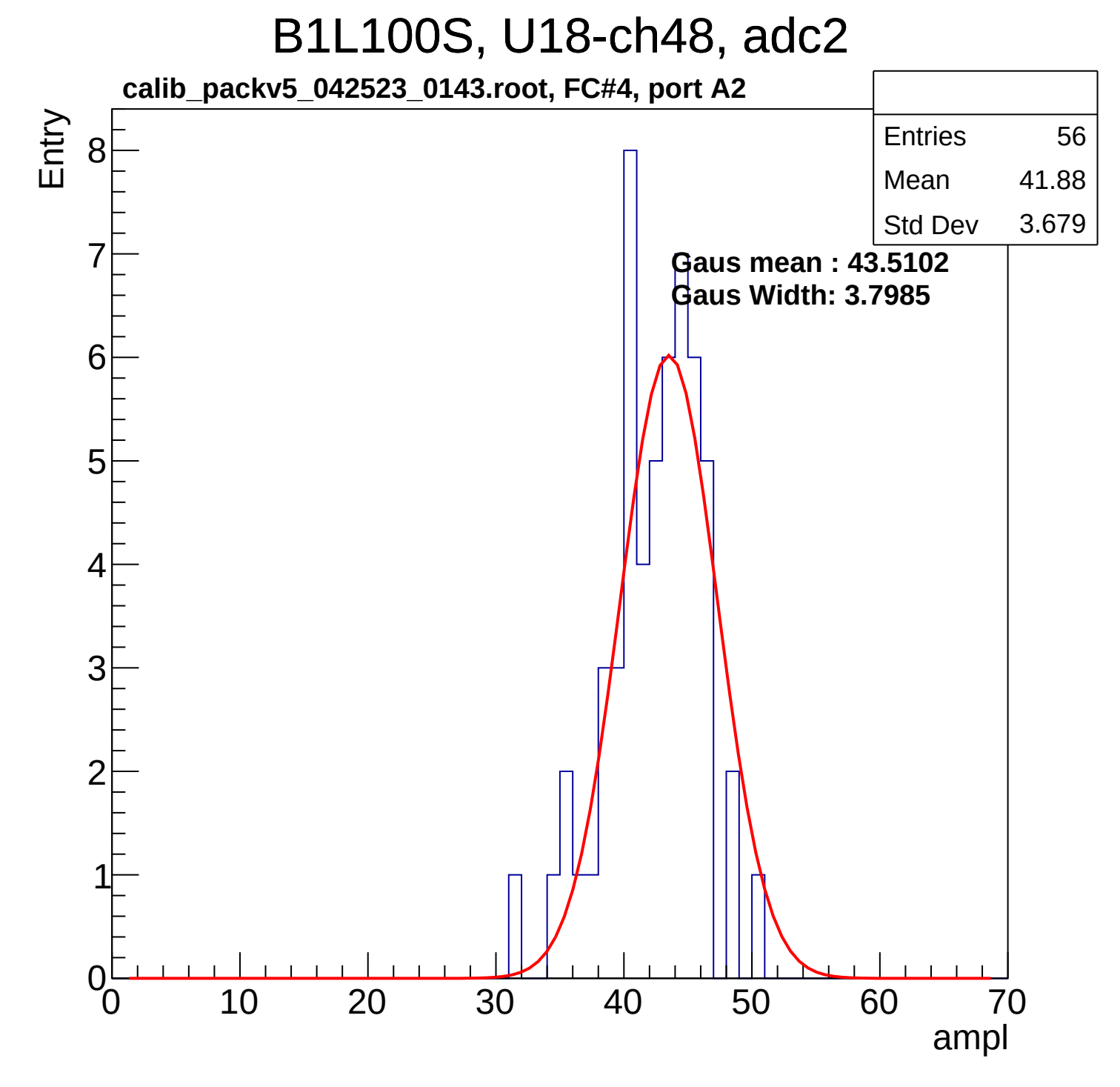

B1L100S, U18-ch47, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 59.02
Std Dev 8.691
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

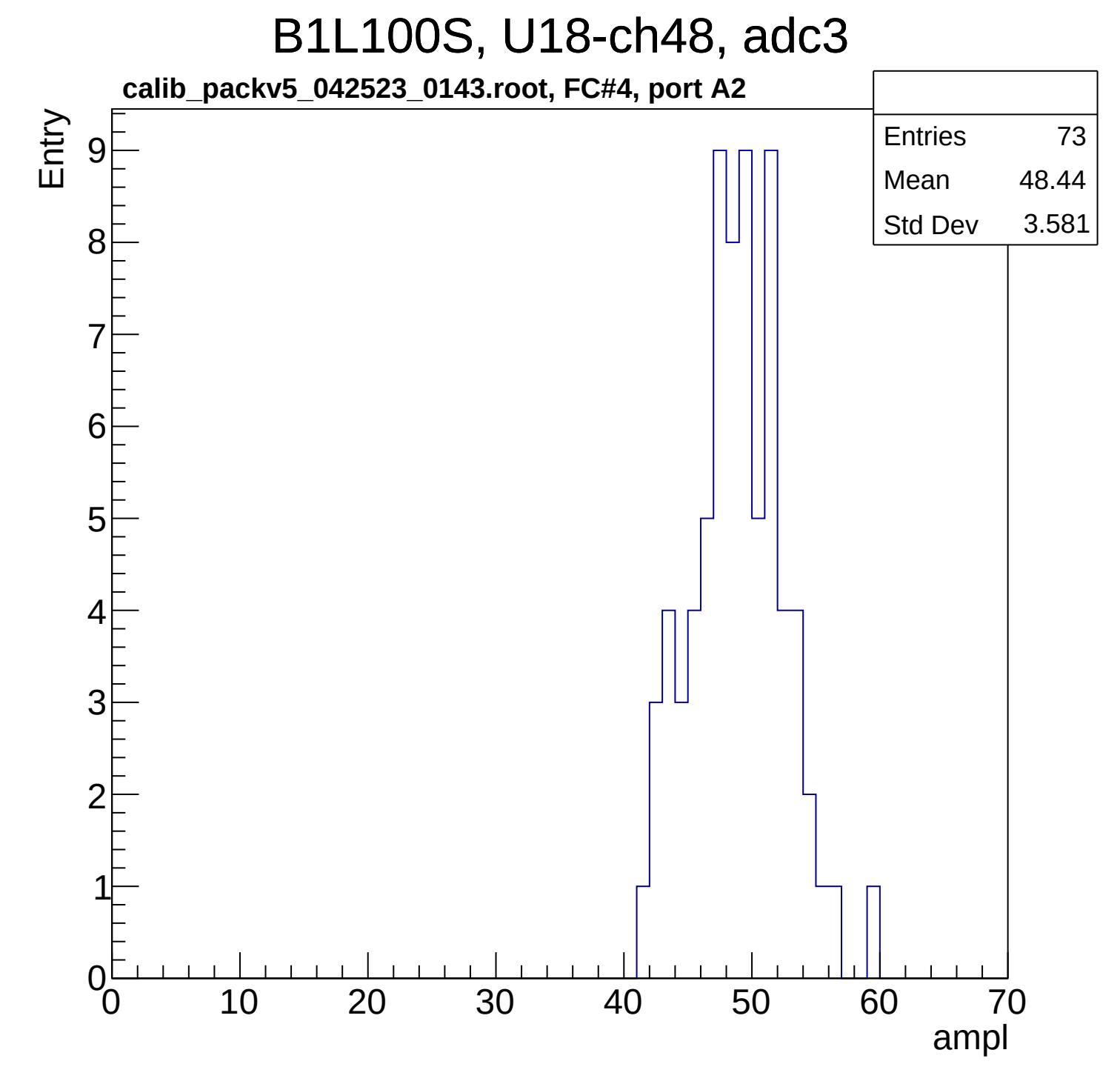

B1L100S, U18-ch47, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 62.25
Std Dev 0.8292
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

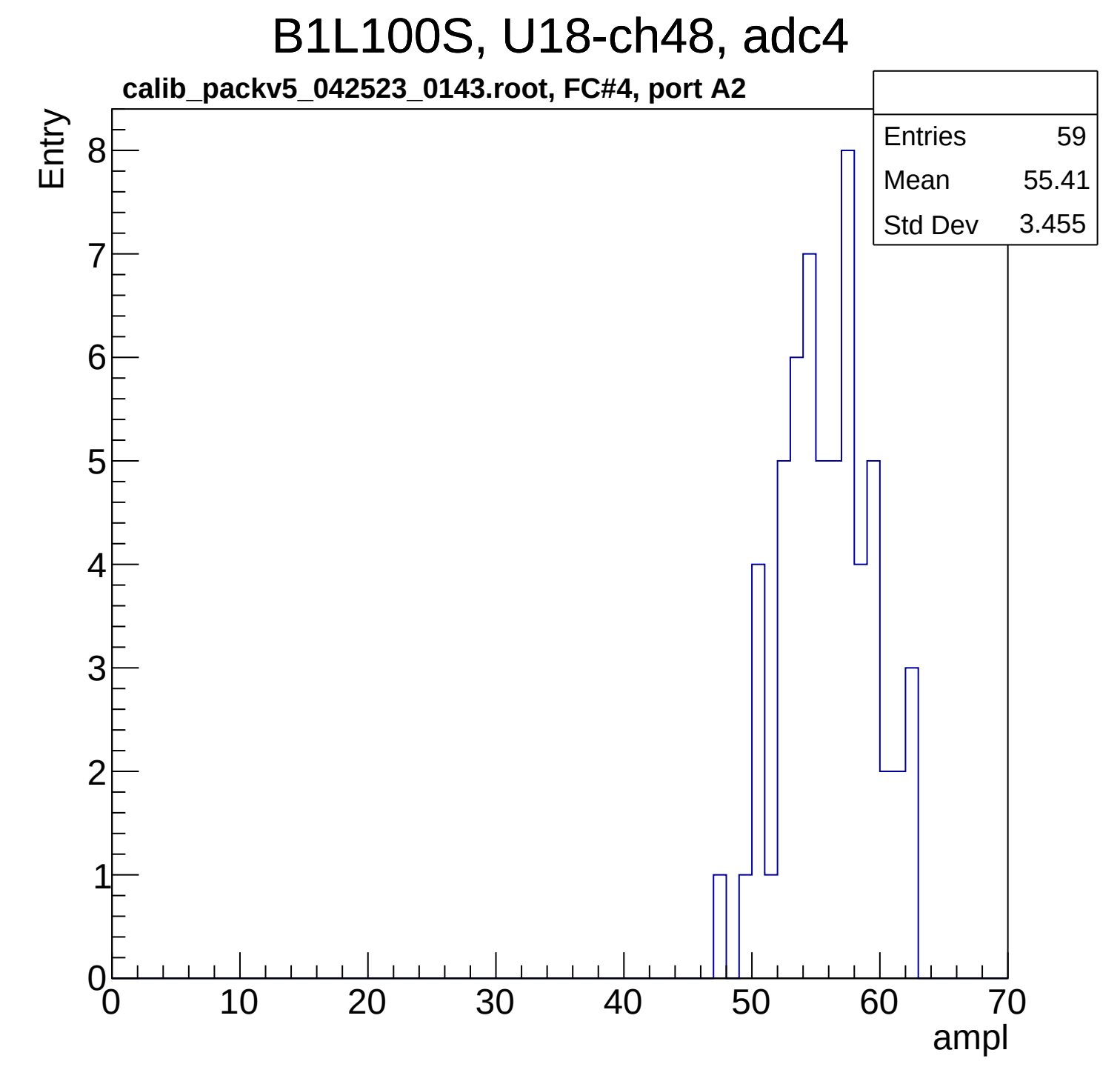

B1L100S, U18-ch47, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

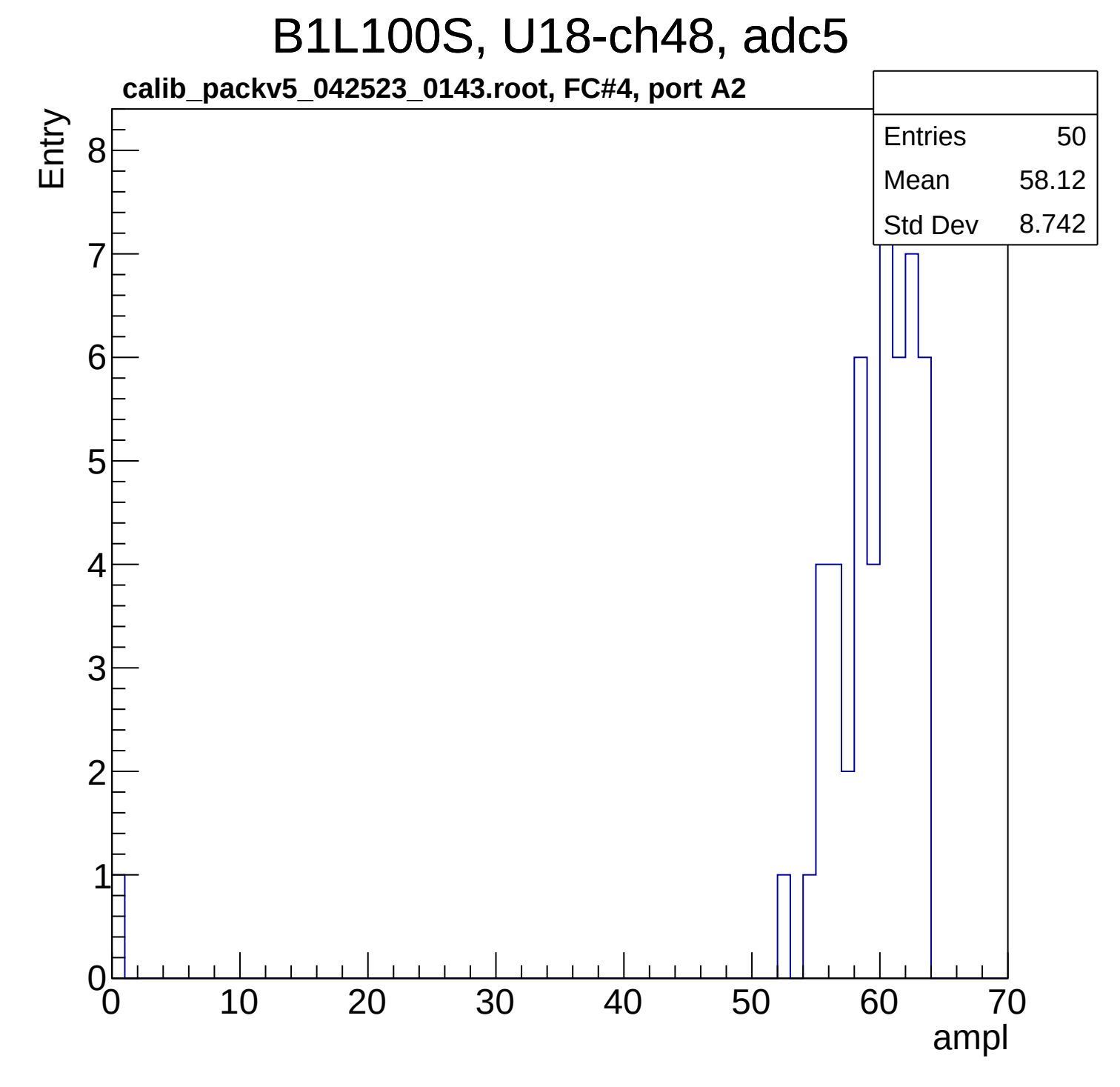

B1L100S, U18-ch48, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 29.55
Std Dev 3.523
Gaus mean : 29.8018
Gaus Width: 3.9786
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

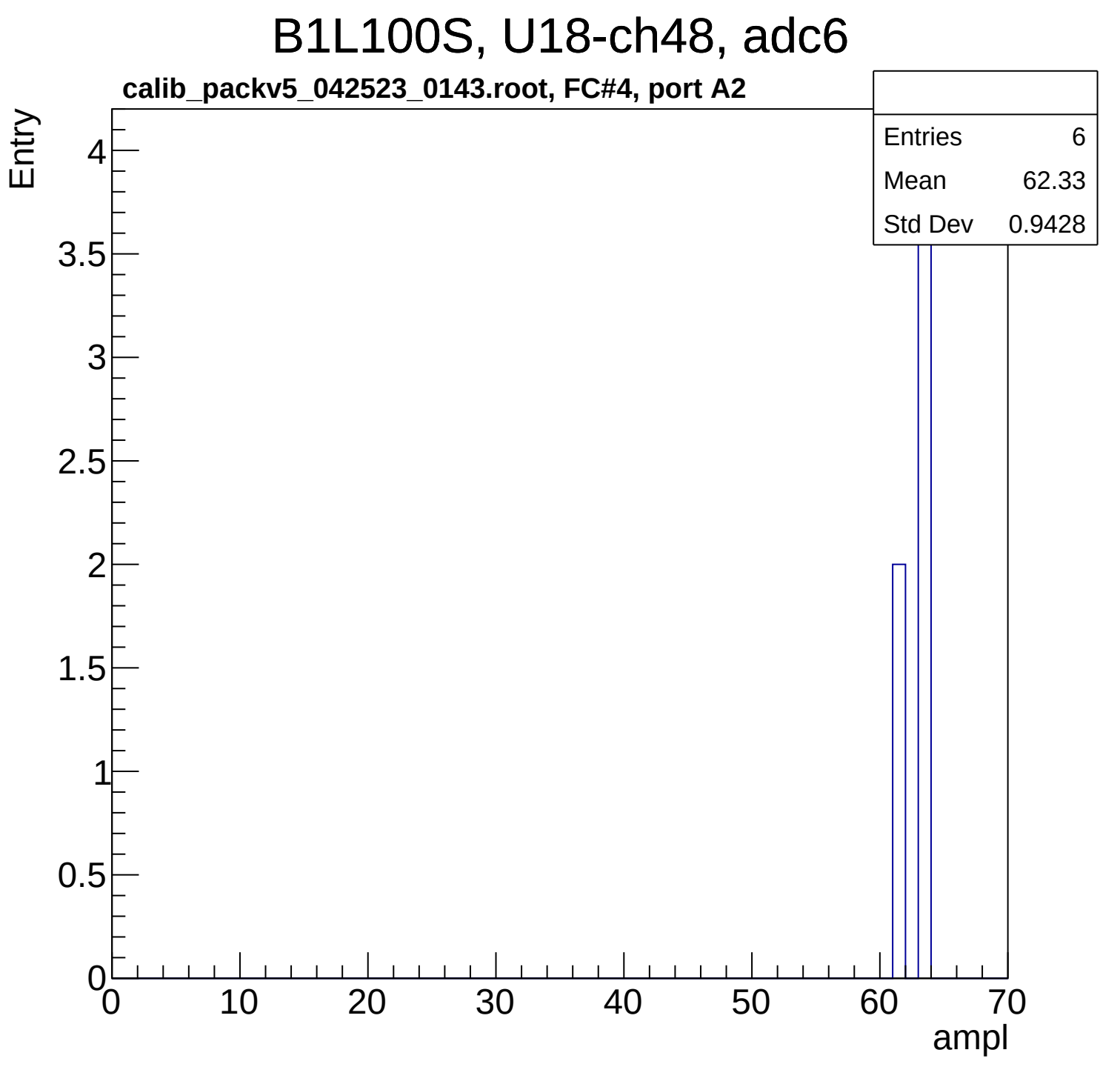

B1L100S, U18-ch48, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 36.18
Std Dev 3.139
Gaus mean : 36.8687
Gaus Width: 3.3830
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

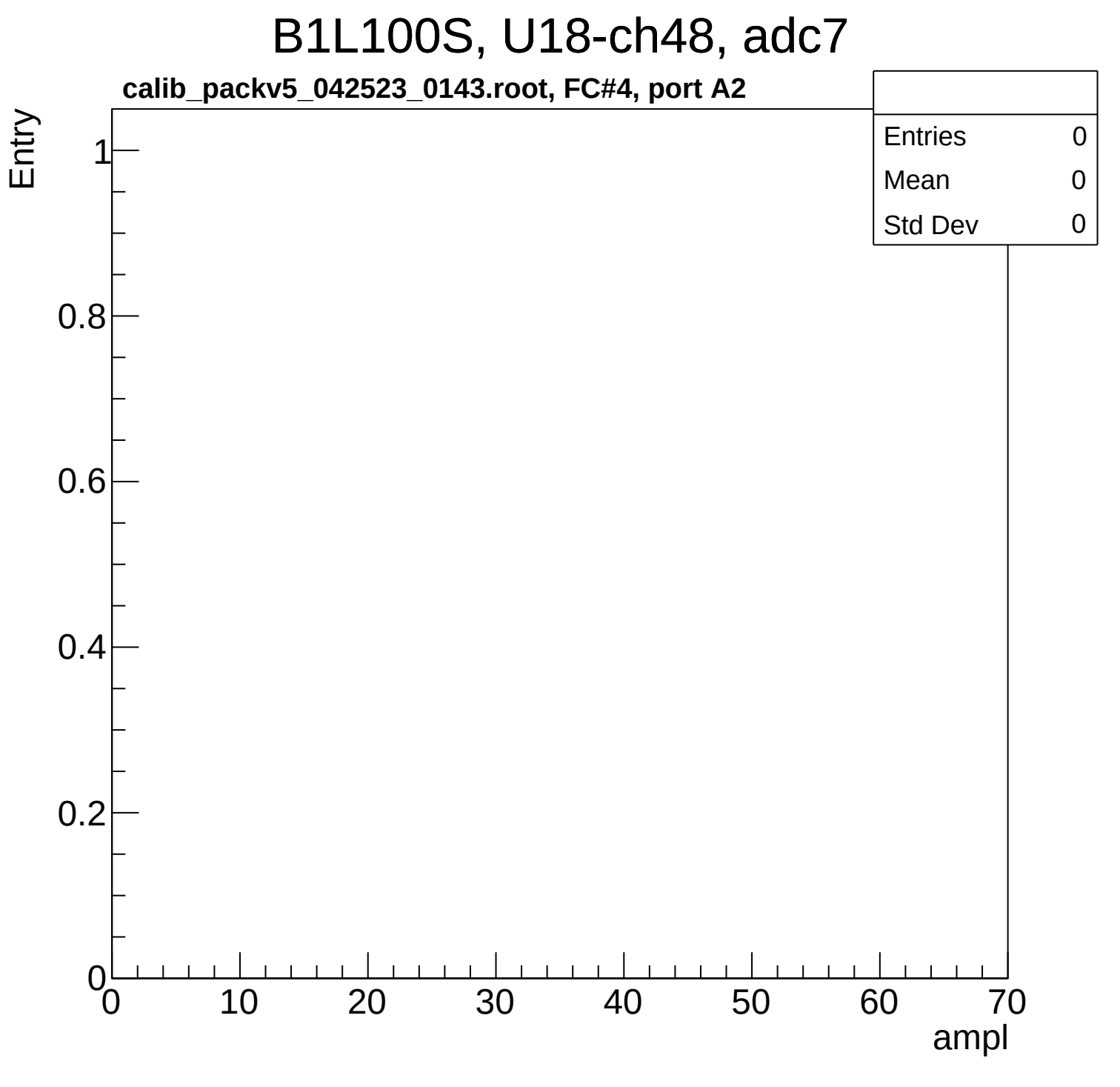

B1L100S, U18-ch48, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 41.88
Std Dev 3.679
Gaus mean : 43.5102
Gaus Width: 3.7985
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

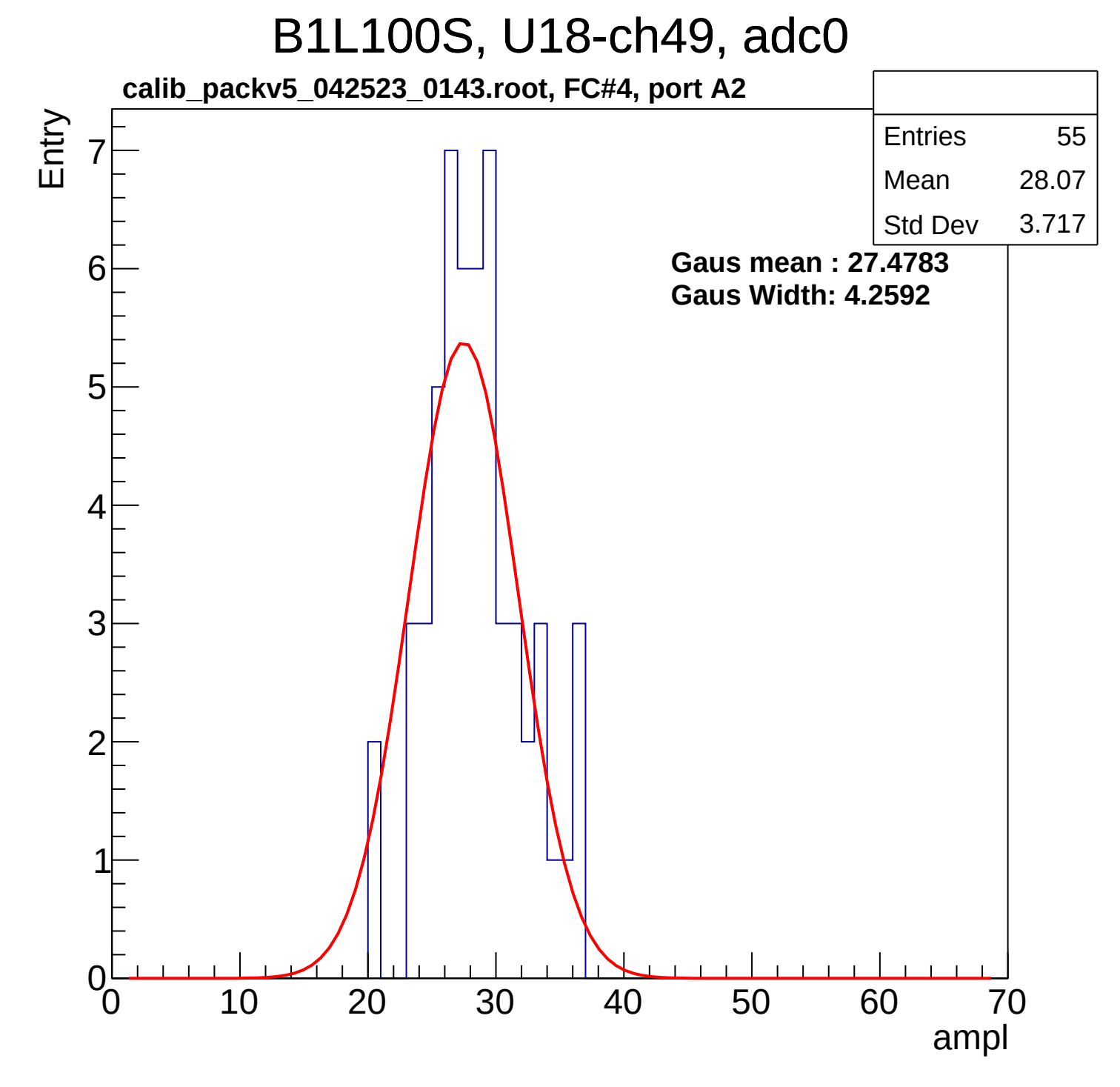

B1L100S, U18-ch48, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 48.44
Std Dev 3.581
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

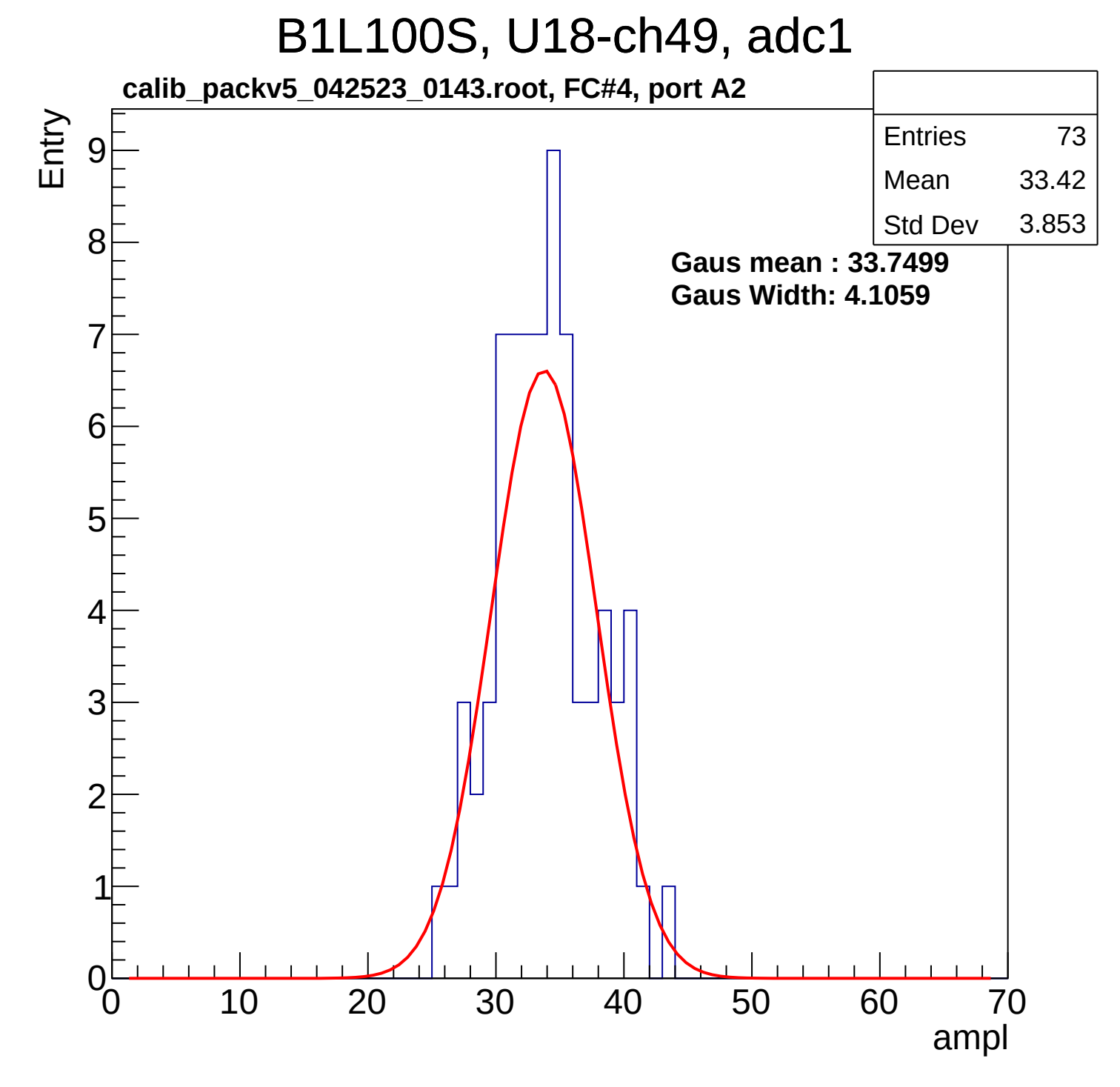

B1L100S, U18-ch48, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 55.41
Std Dev 3.455
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

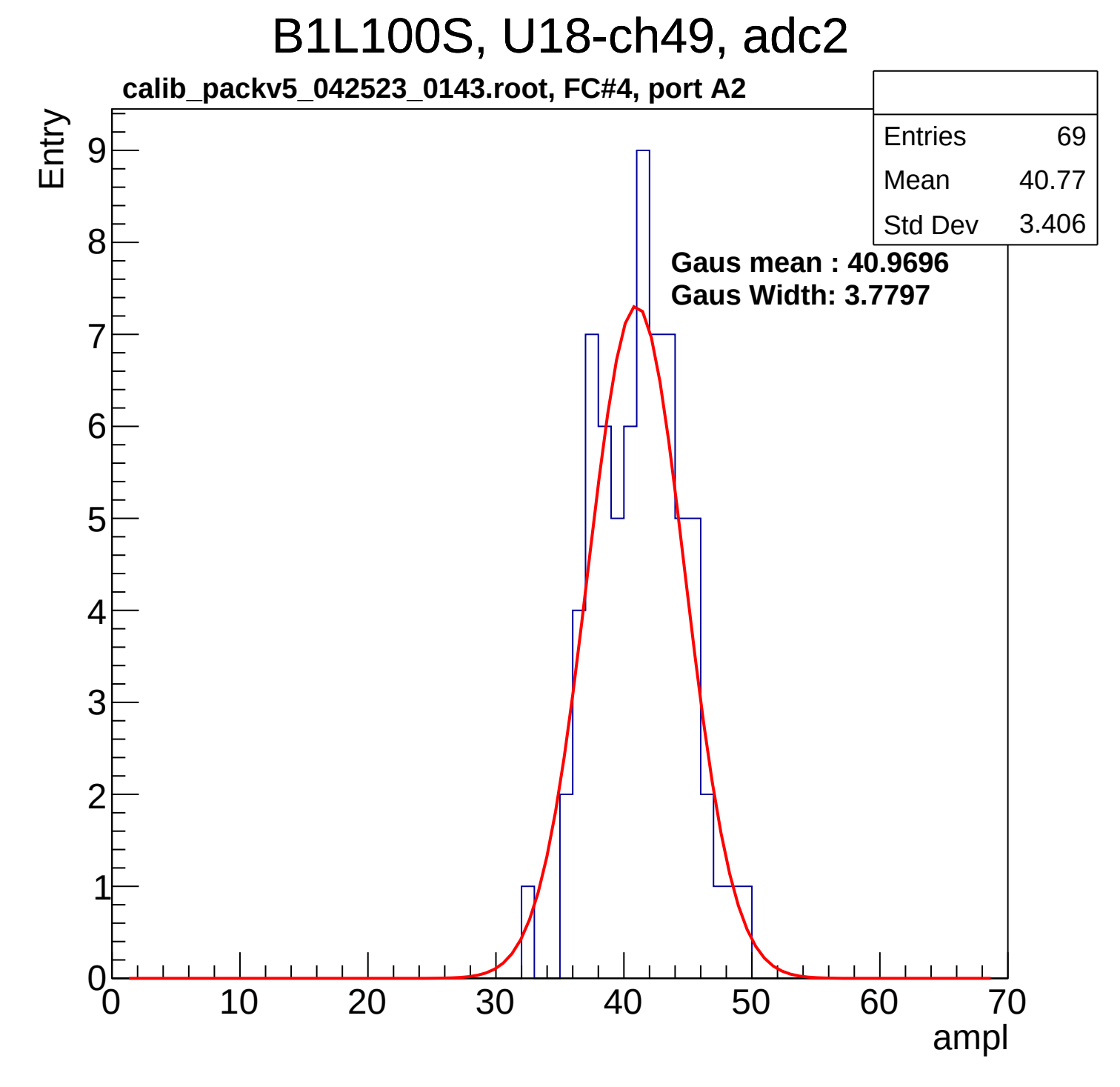

B1L100S, U18-ch48, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 58.12
Std Dev 8.742
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

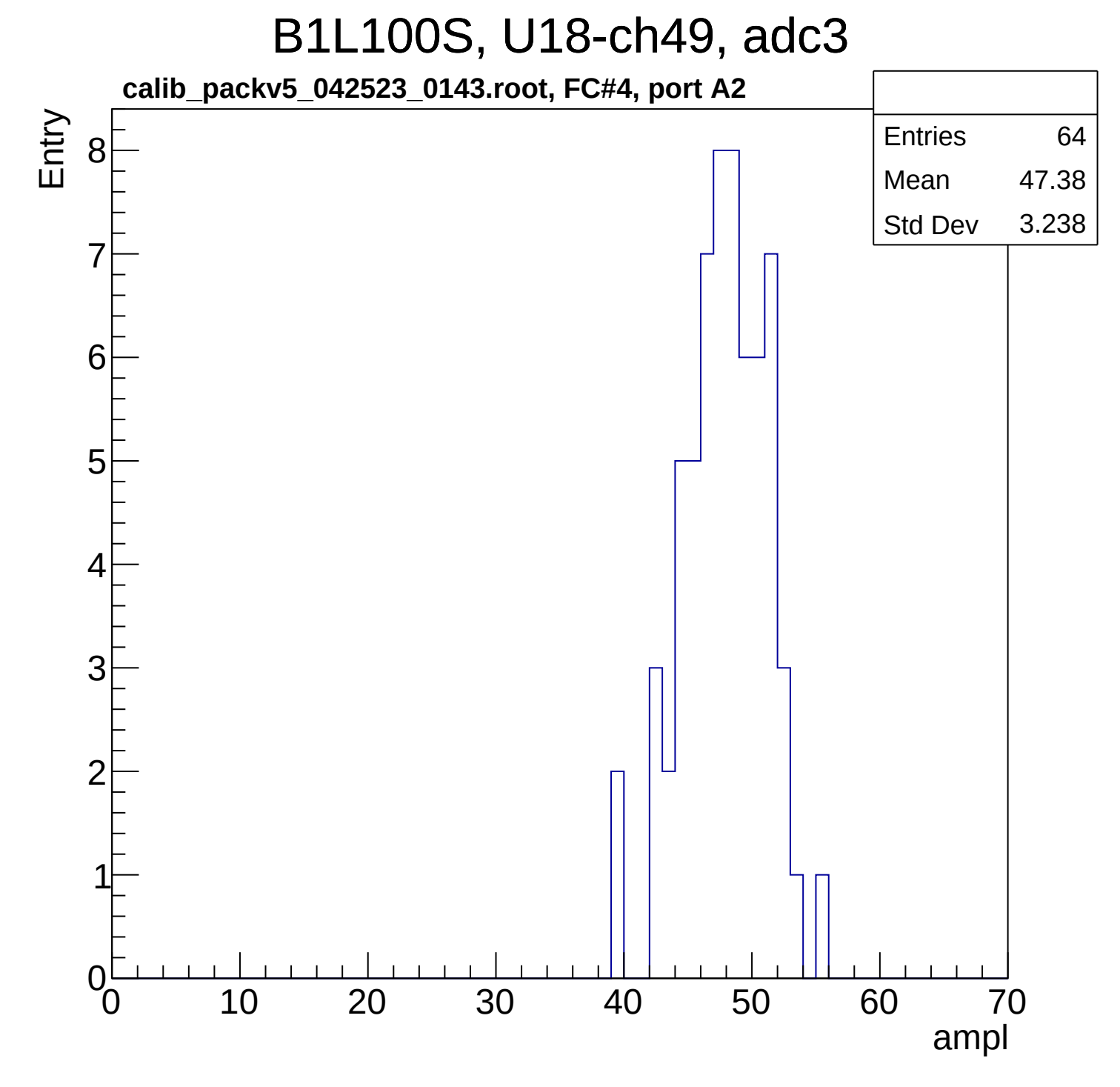

B1L100S, U18-ch48, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 62.33
Std Dev 0.9428
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

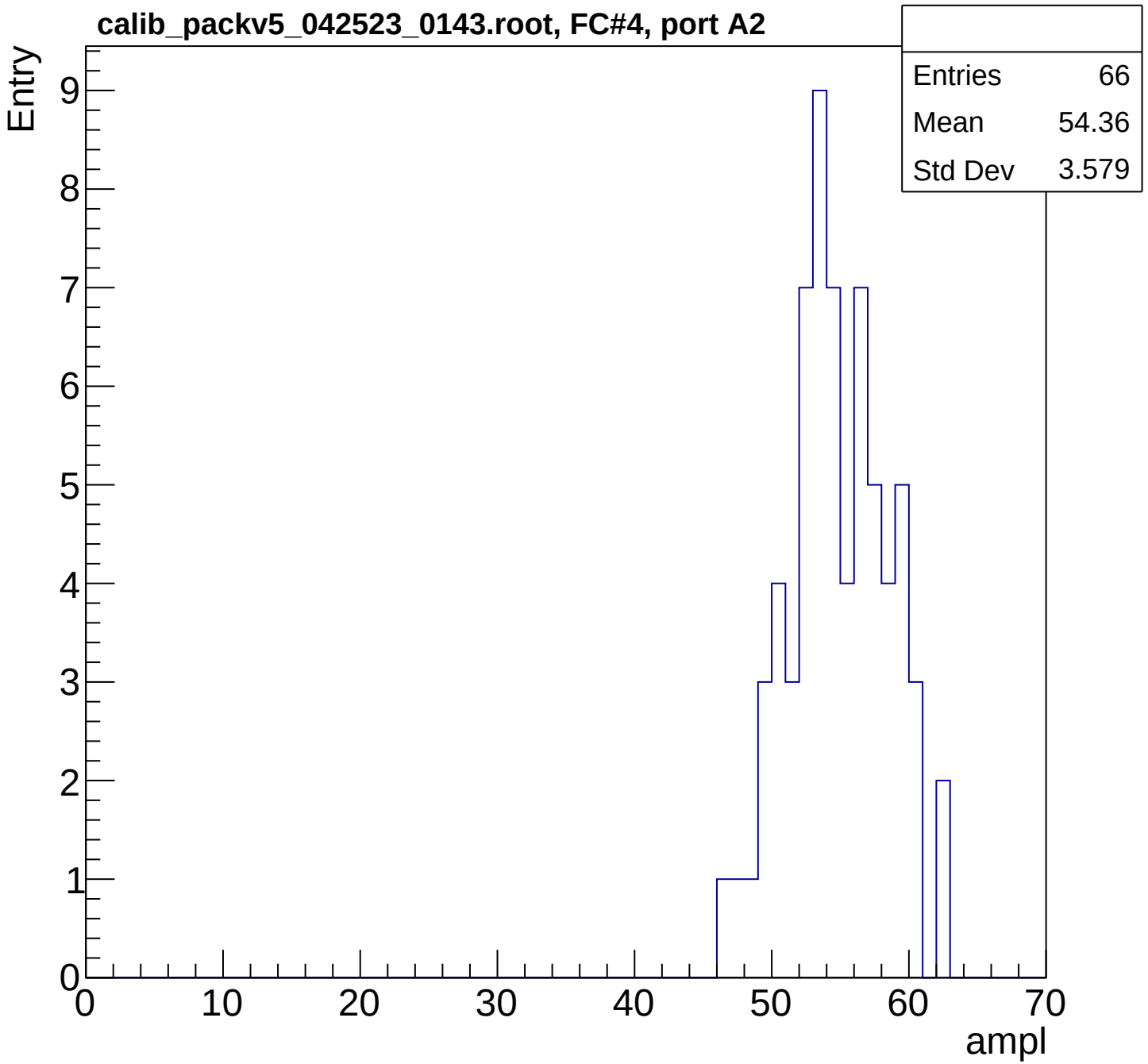

B1L100S, U18-ch48, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

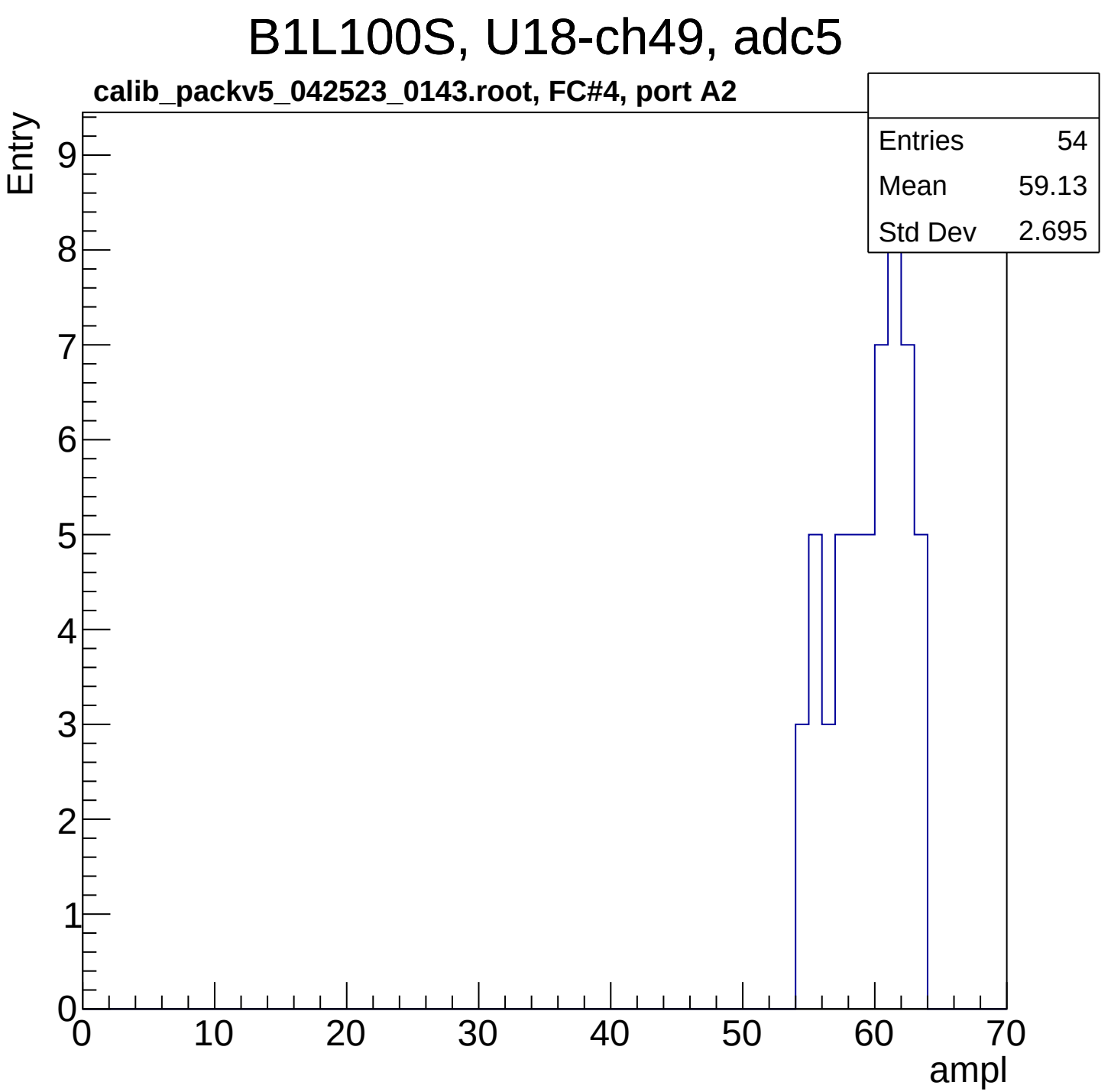

B1L100S, U18-ch49, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 28.07
Std Dev 3.717
Gaus mean : 27.4783
Gaus Width: 4.2592
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

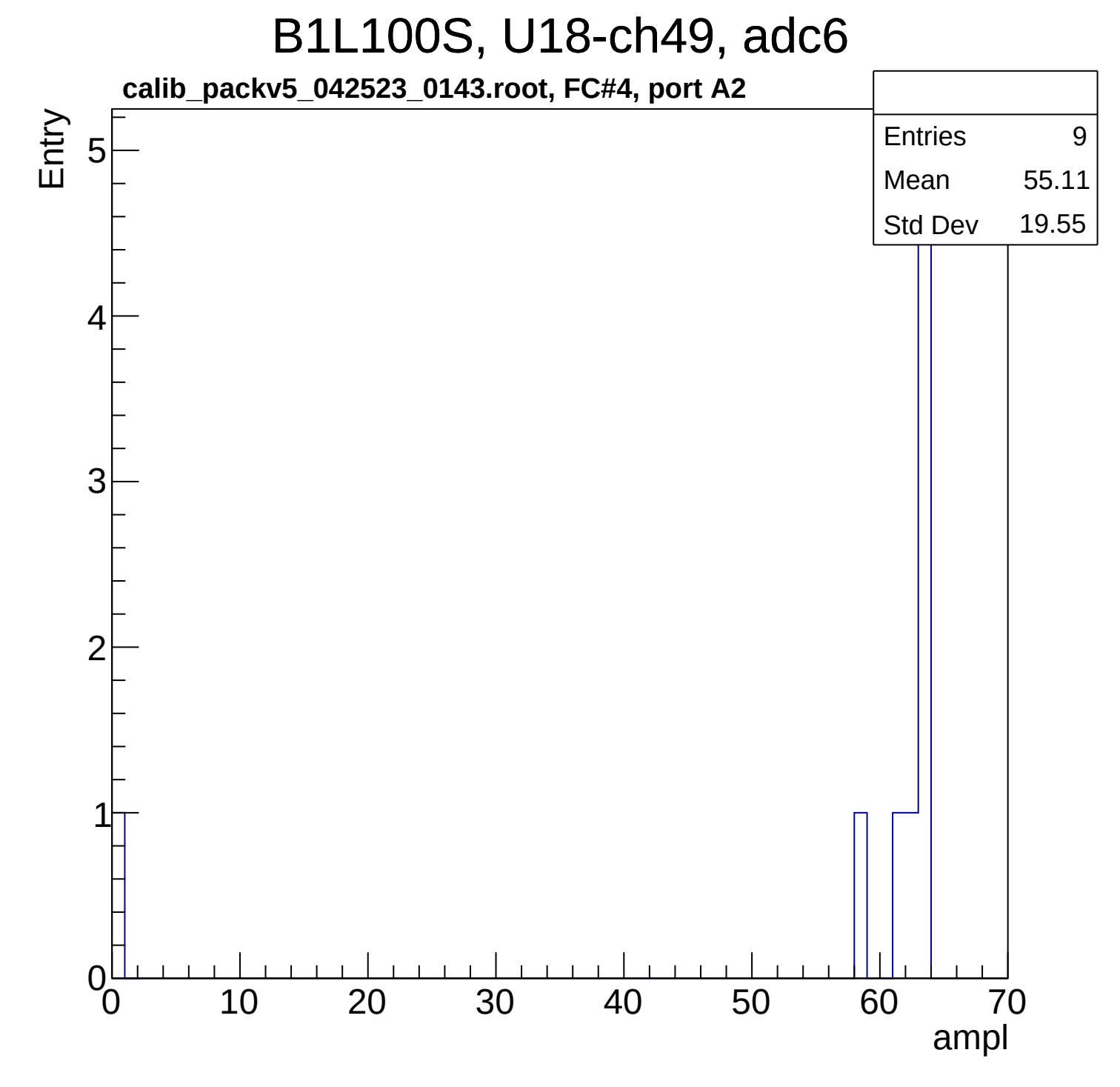

B1L100S, U18-ch49, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 33.42
Std Dev 3.853
Gaus mean : 33.7499
Gaus Width: 4.1059
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

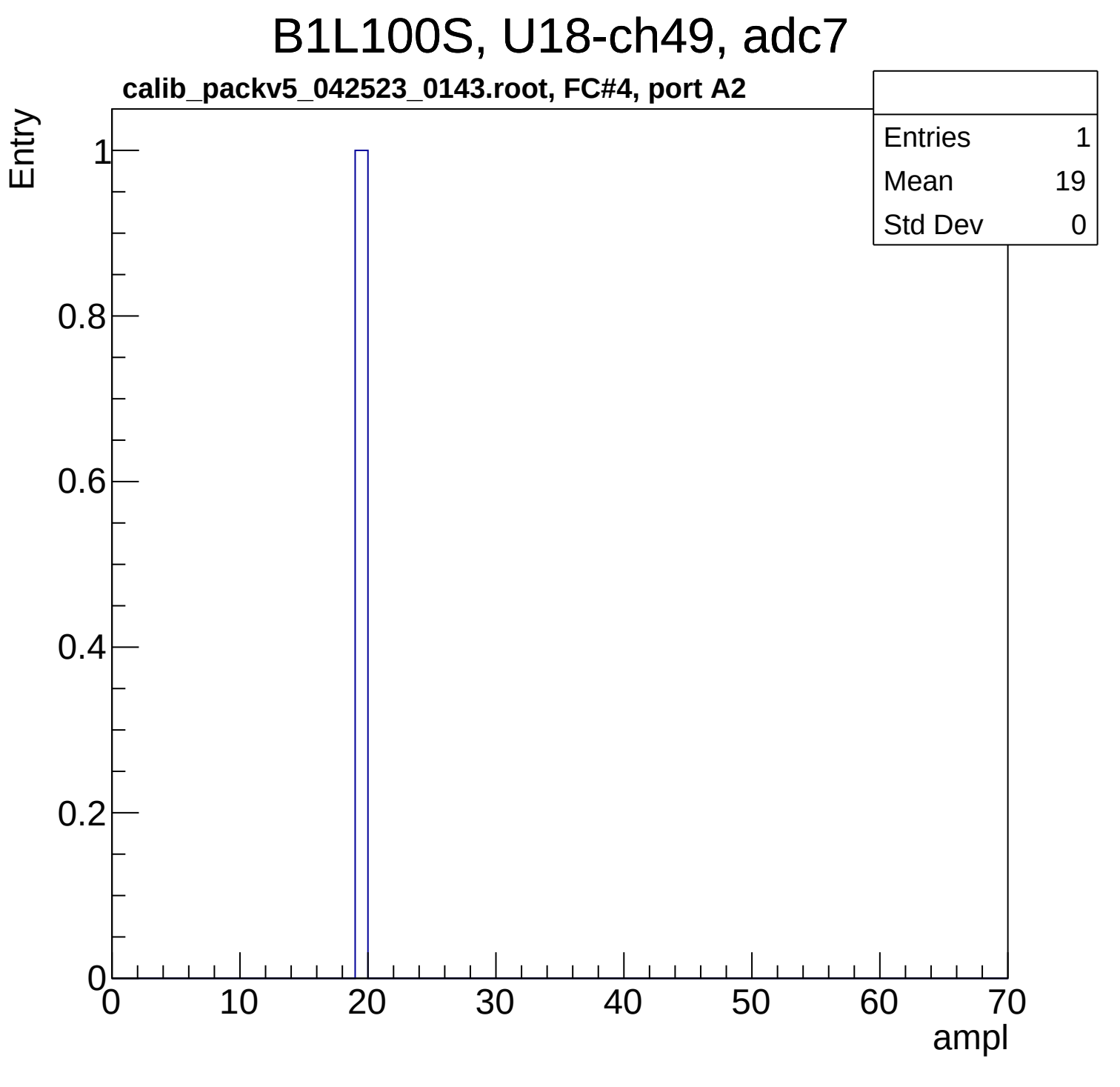

B1L100S, U18-ch49, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 40.77
Std Dev 3.406
Gaus mean : 40.9696
Gaus Width: 3.7797
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

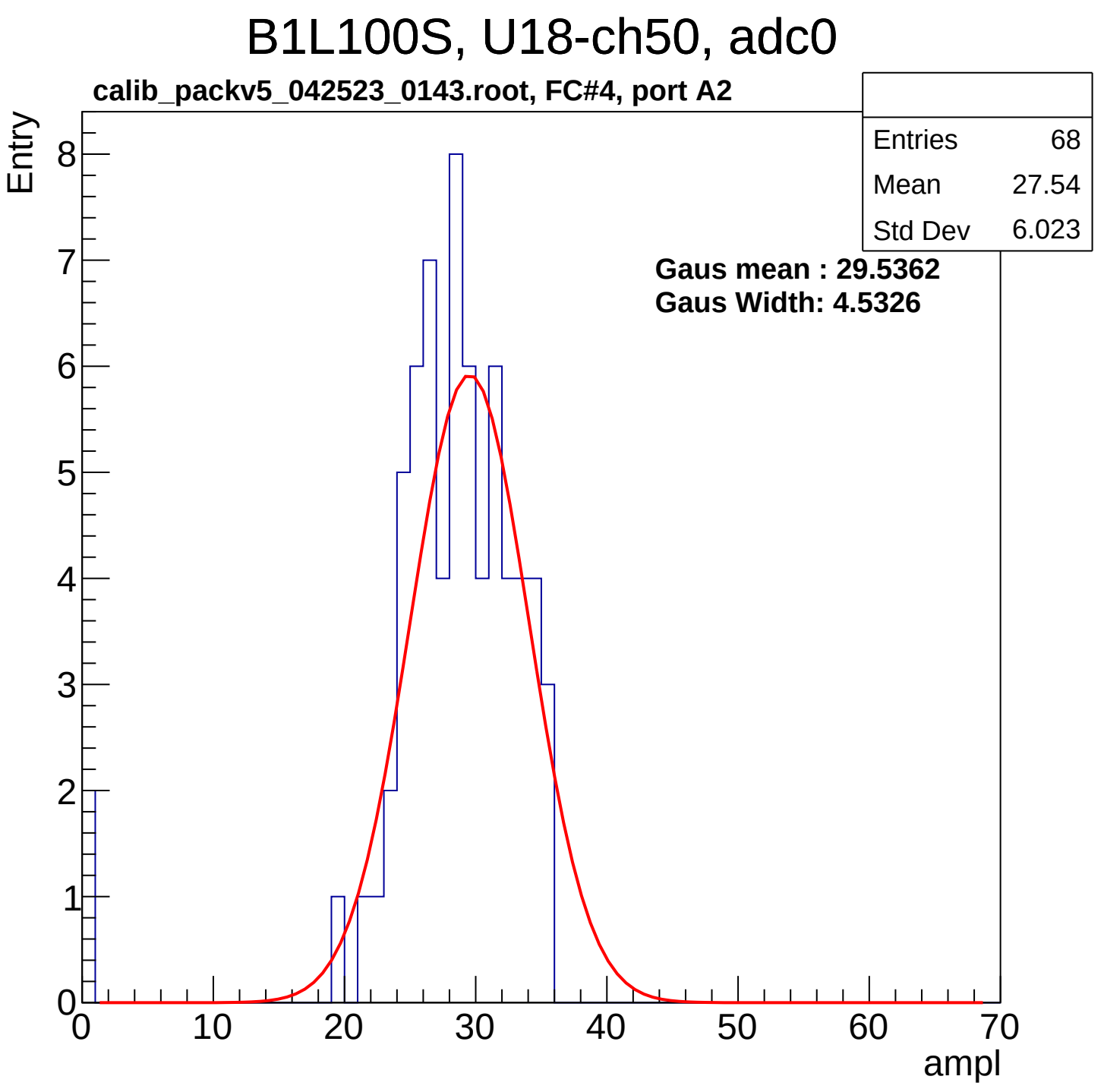

B1L100S, U18-ch49, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 47.38
Std Dev 3.238
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

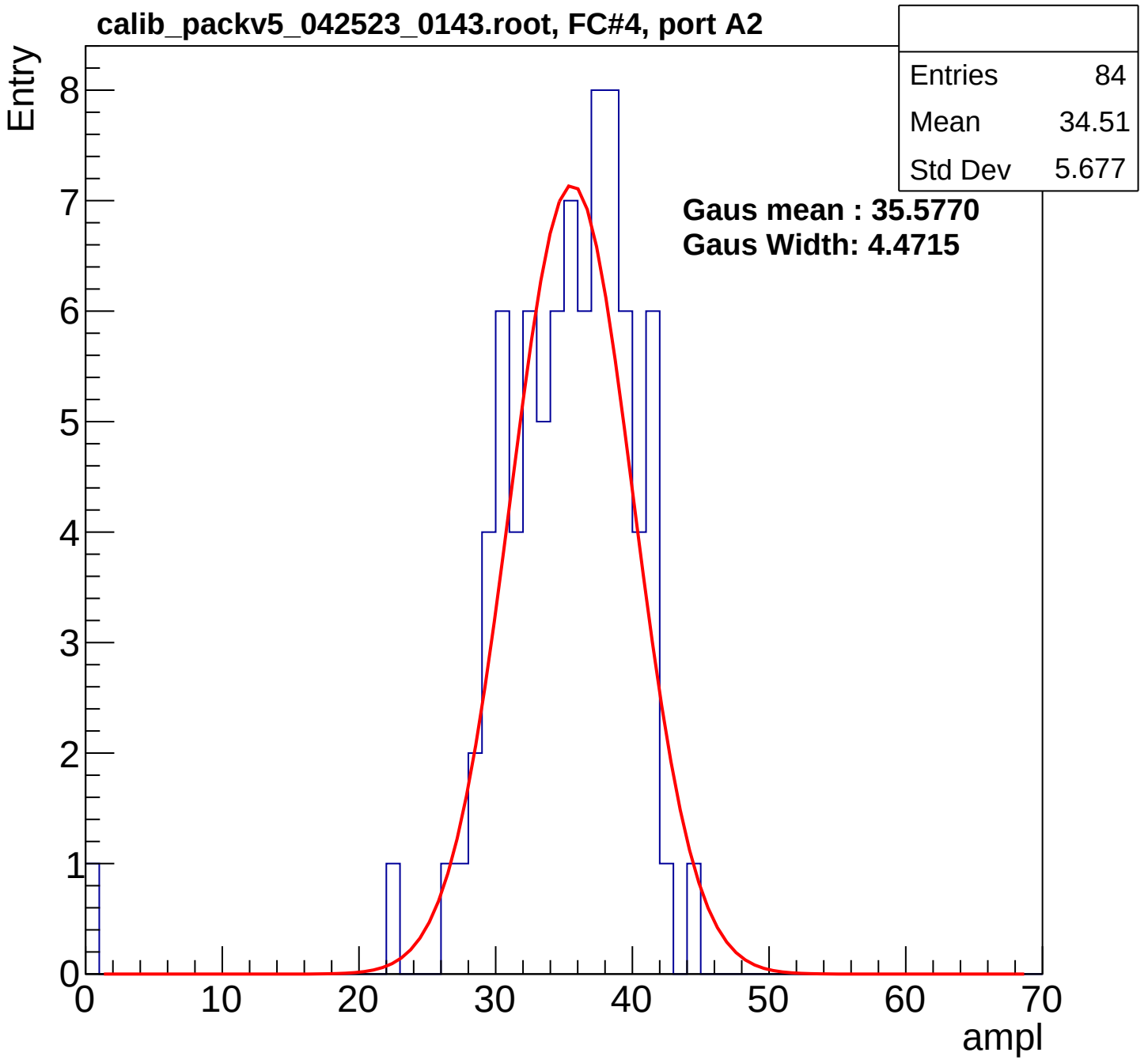

B1L100S, U18-ch49, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 54.36
Std Dev 3.579
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

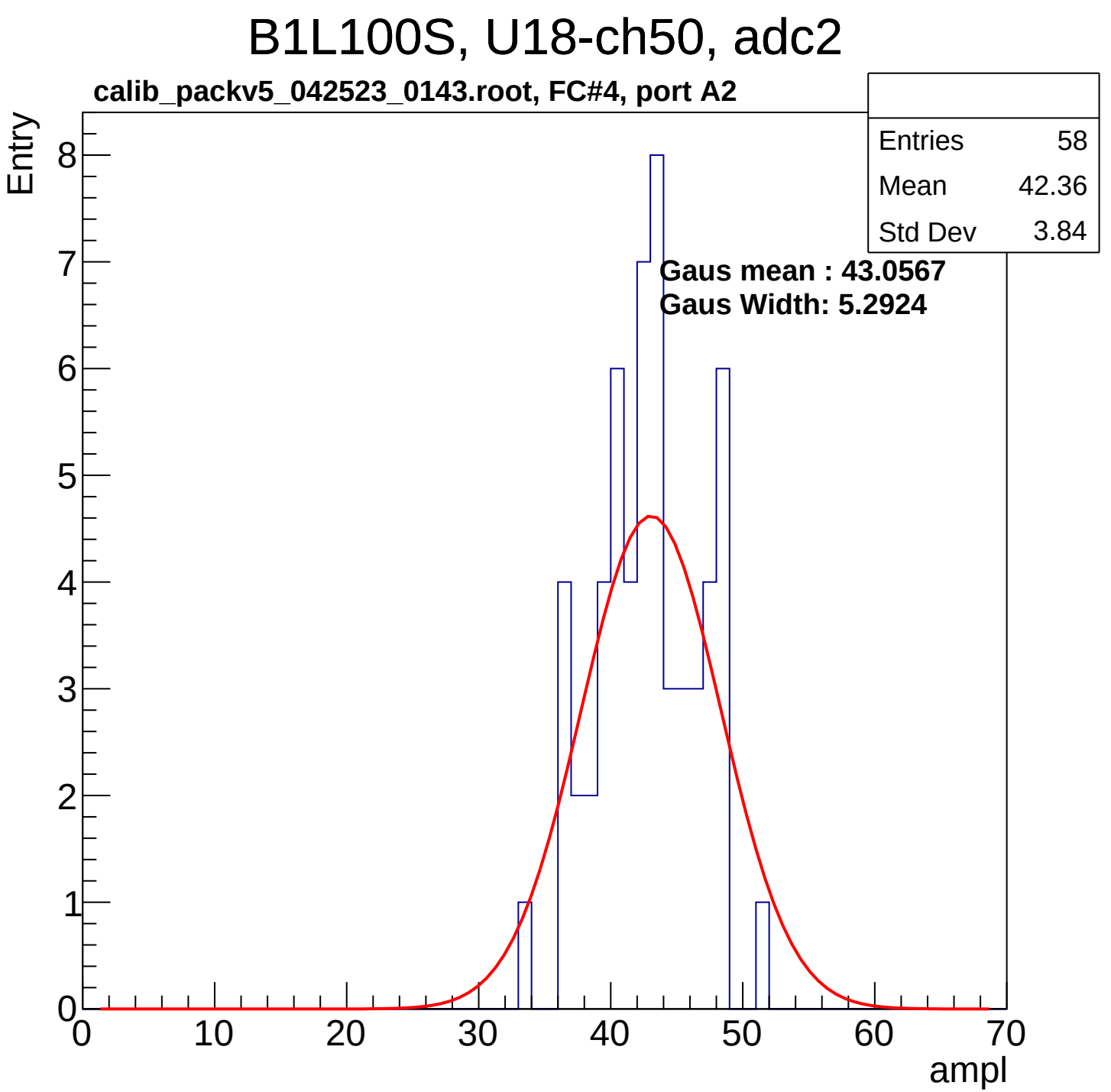

B1L100S, U18-ch49, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 59.13
Std Dev 2.695
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

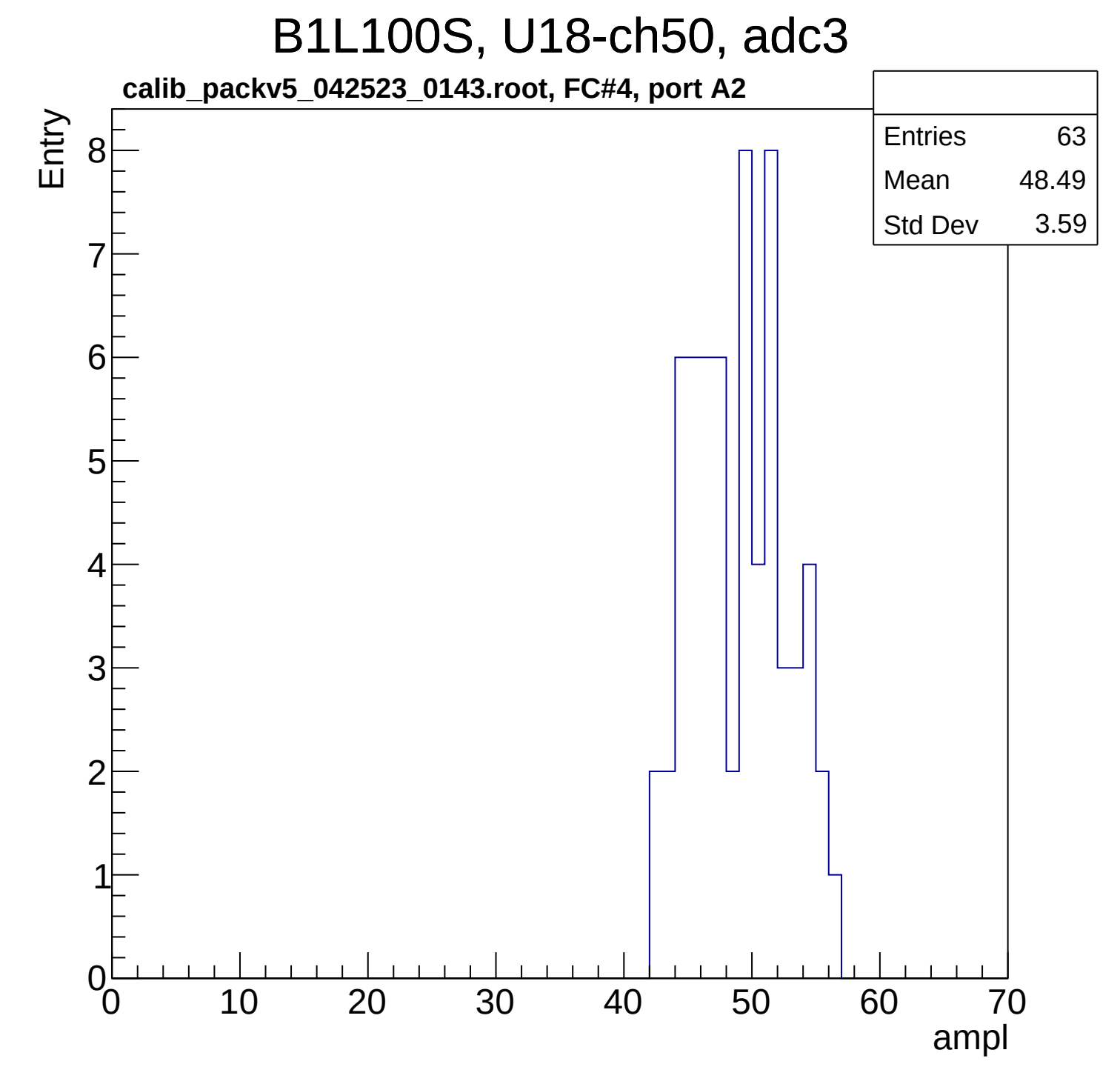

B1L100S, U18-ch49, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 55.11
Std Dev 19.55
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

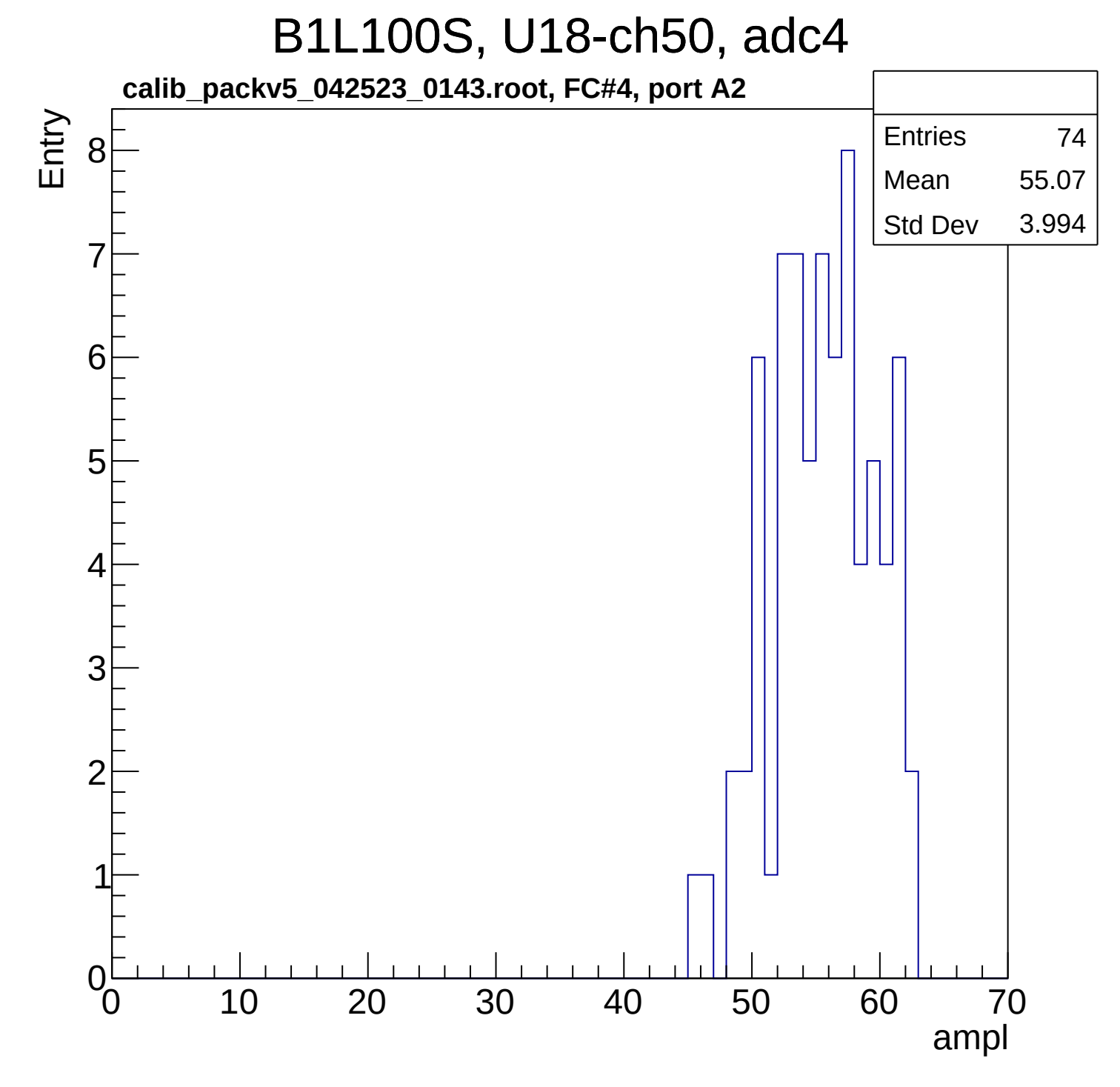

B1L100S, U18-ch49, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 19
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

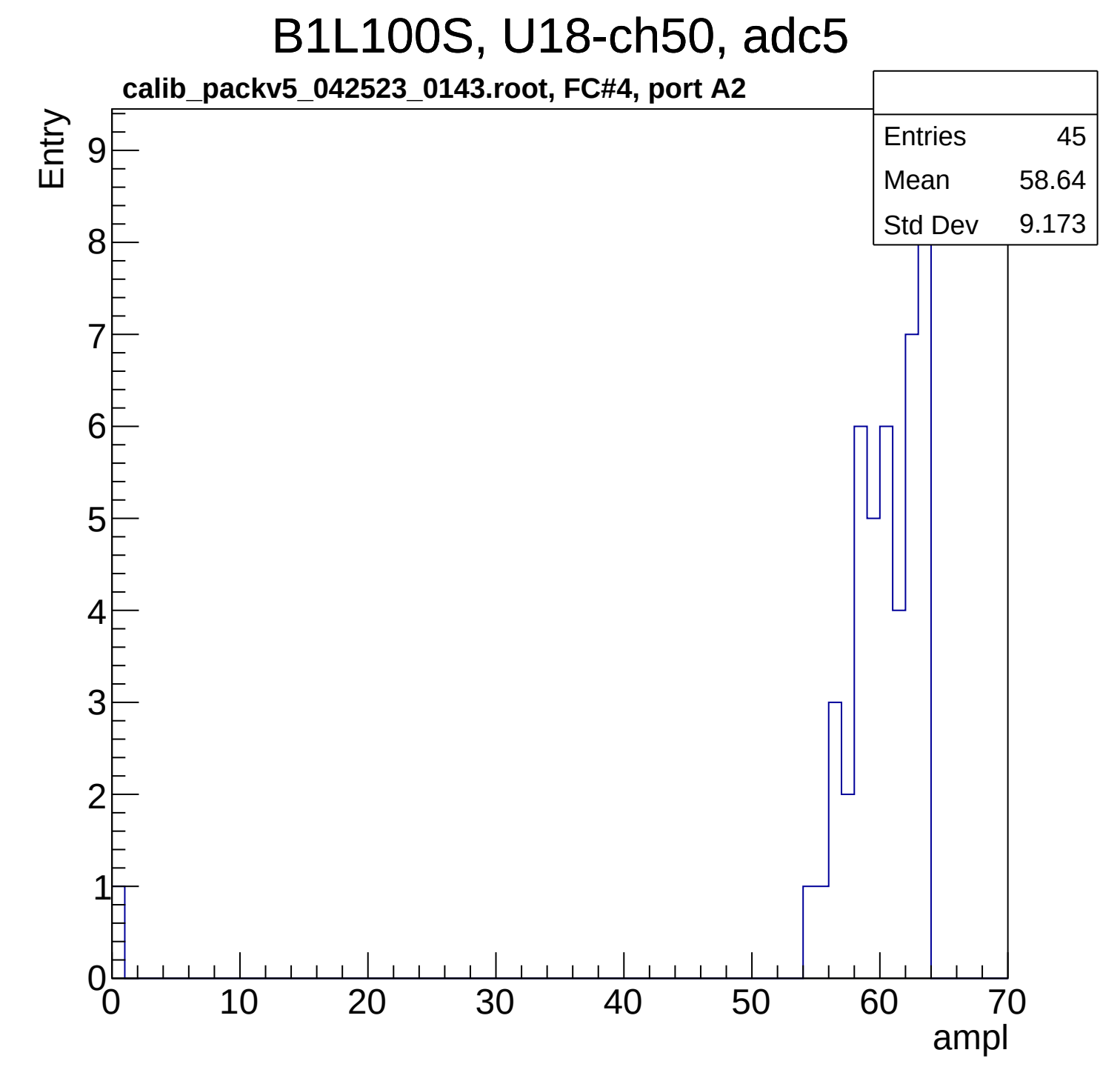

B1L100S, U18-ch50, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 27.54
Std Dev 6.023
Gaus mean : 29.5362
Gaus Width: 4.5326
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

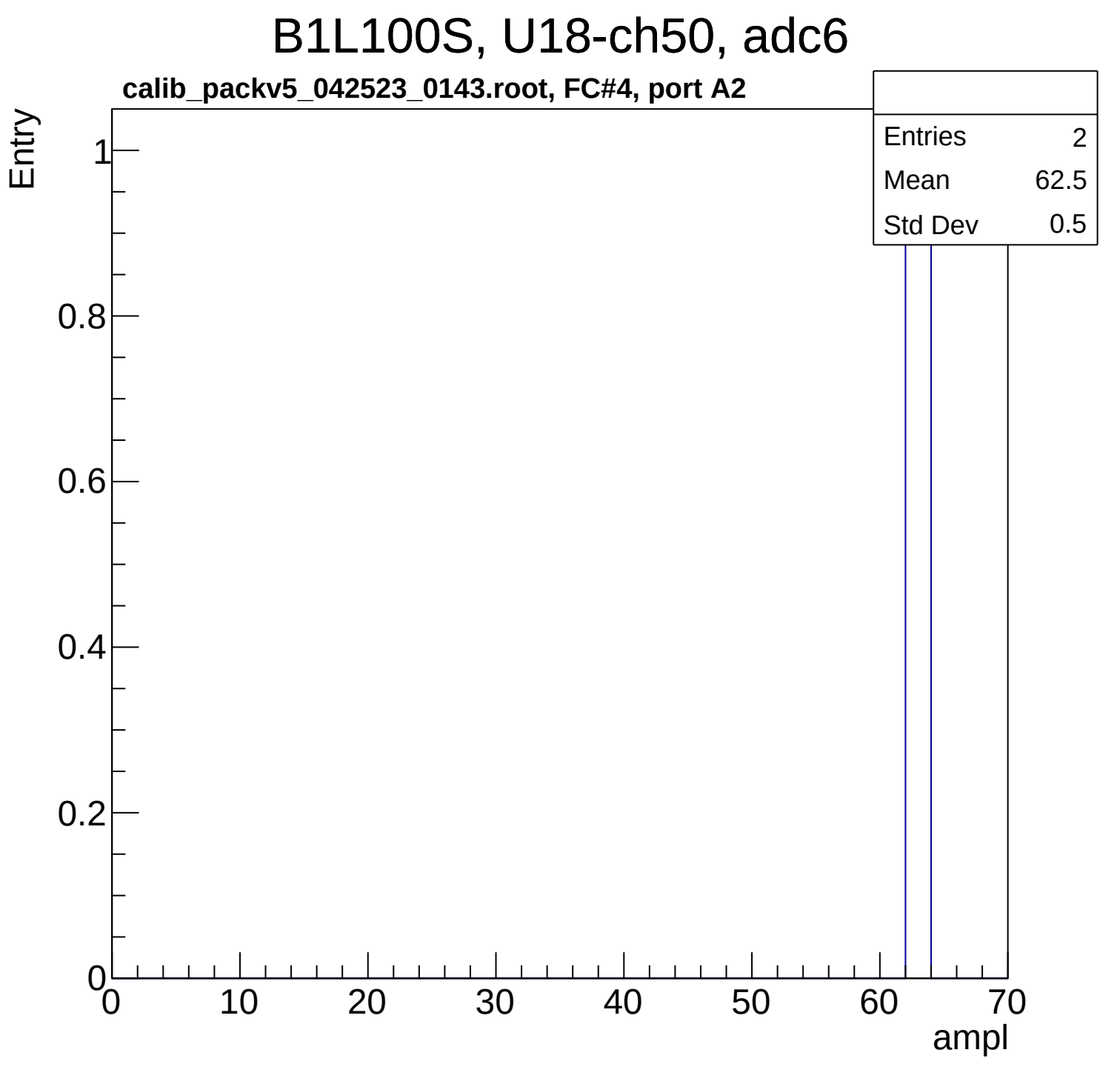

B1L100S, U18-ch50, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 84
Mean 34.51
Std Dev 5.677
Gaus mean : 35.5770
Gaus Width: 4.4715
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

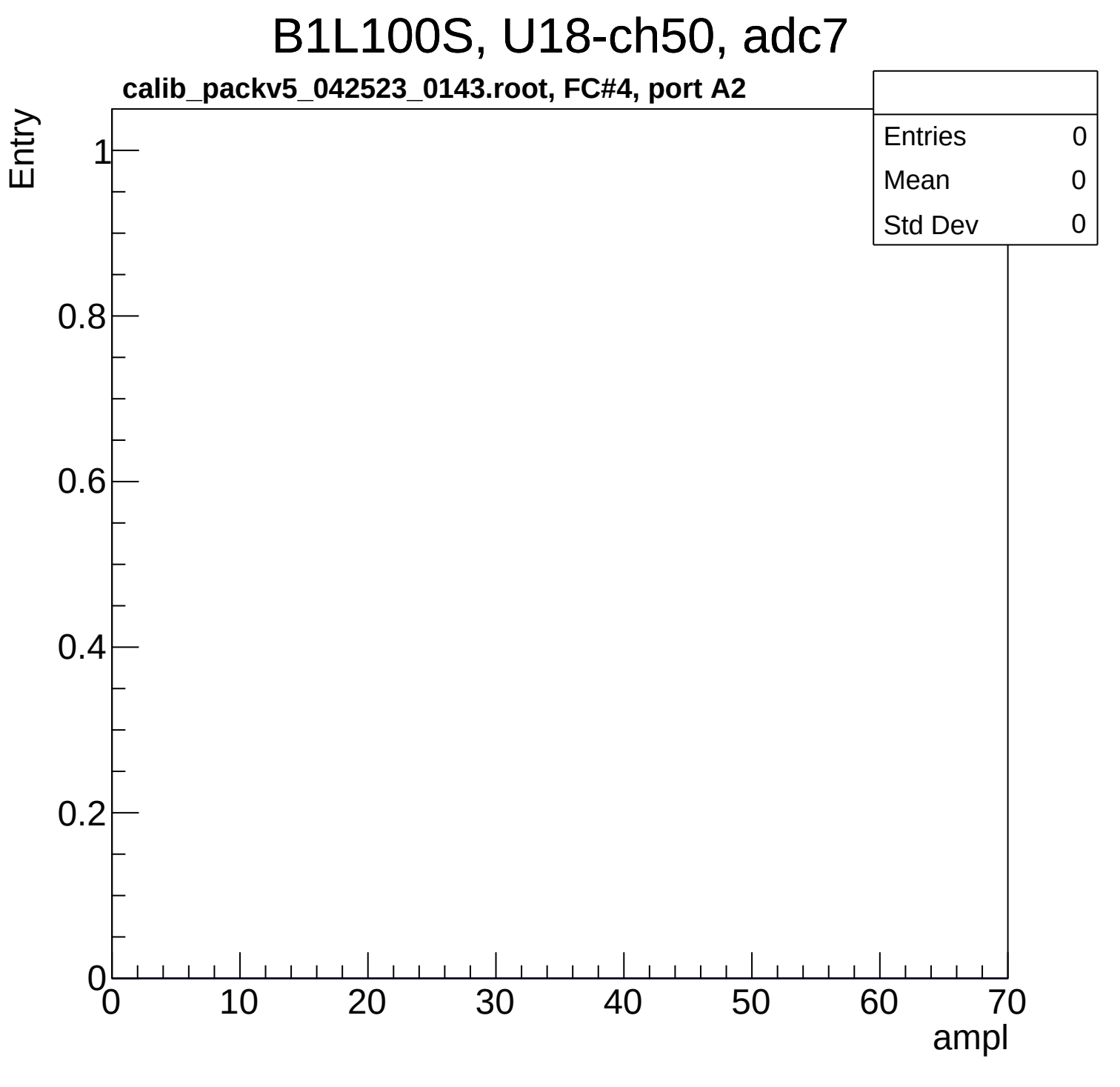

B1L100S, U18-ch50, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 42.36
Std Dev 3.84
Gaus mean : 43.0567
Gaus Width: 5.2924
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

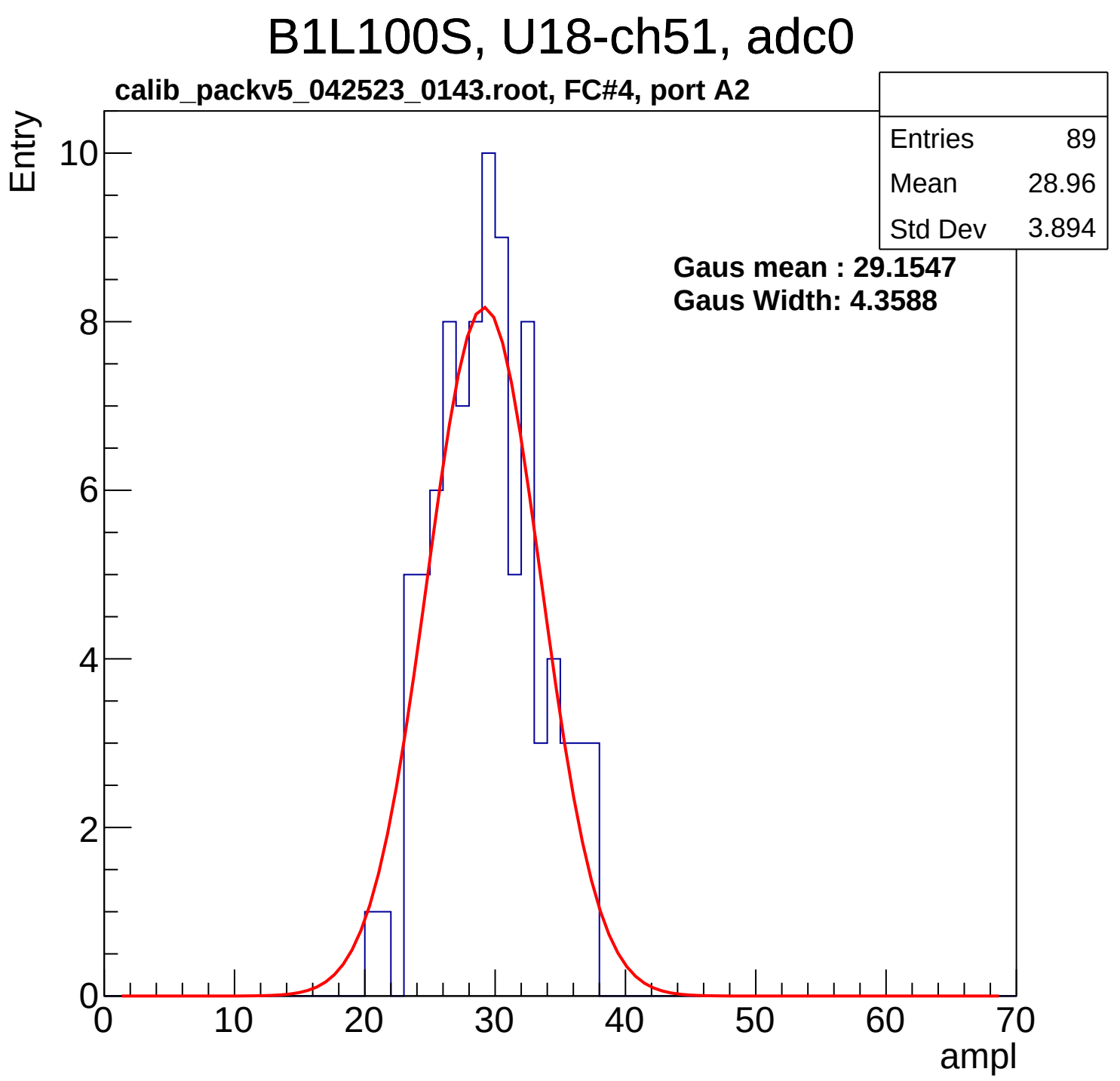

B1L100S, U18-ch50, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 48.49
Std Dev 3.59
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

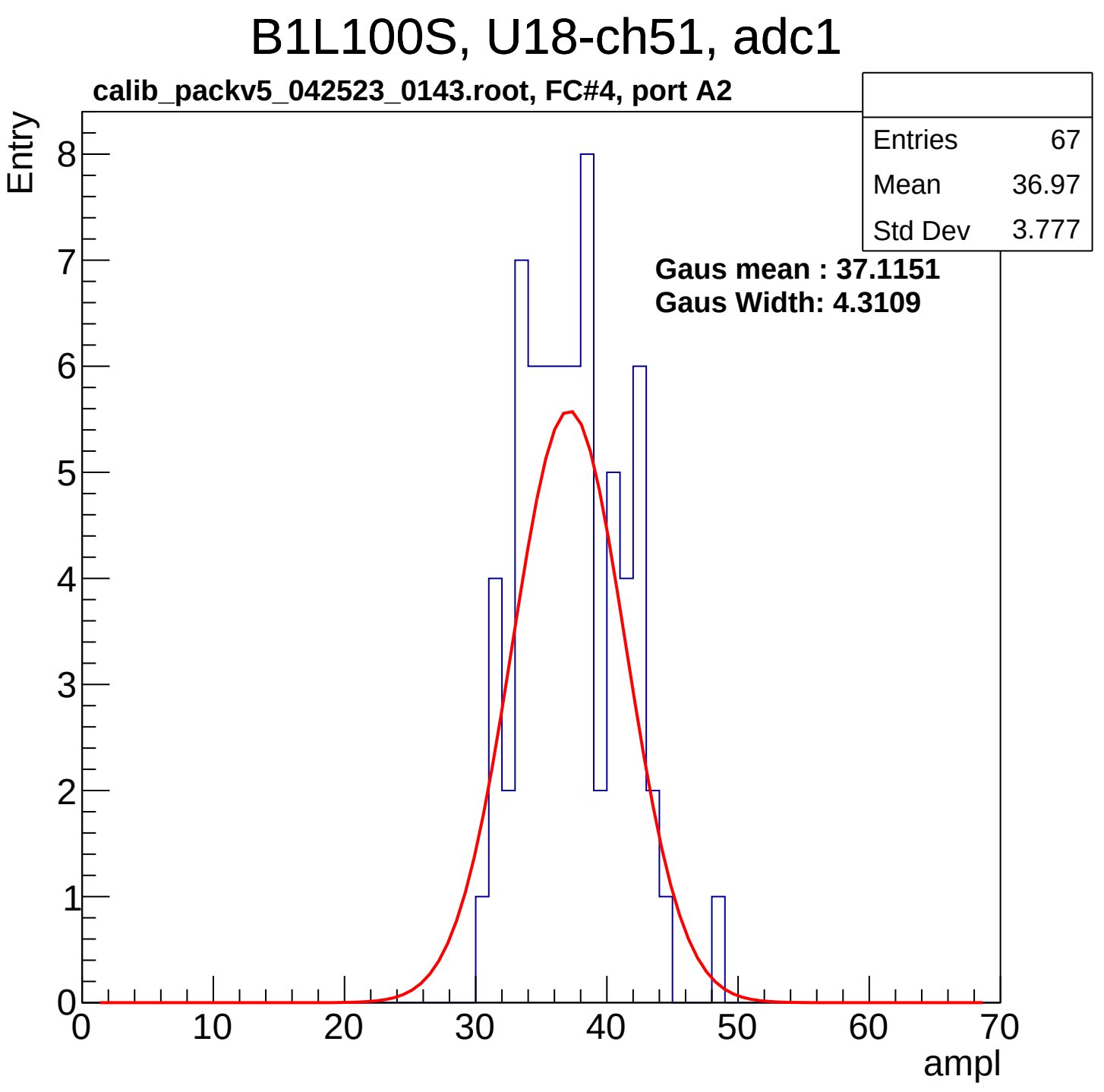

B1L100S, U18-ch50, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 55.07
Std Dev 3.994
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

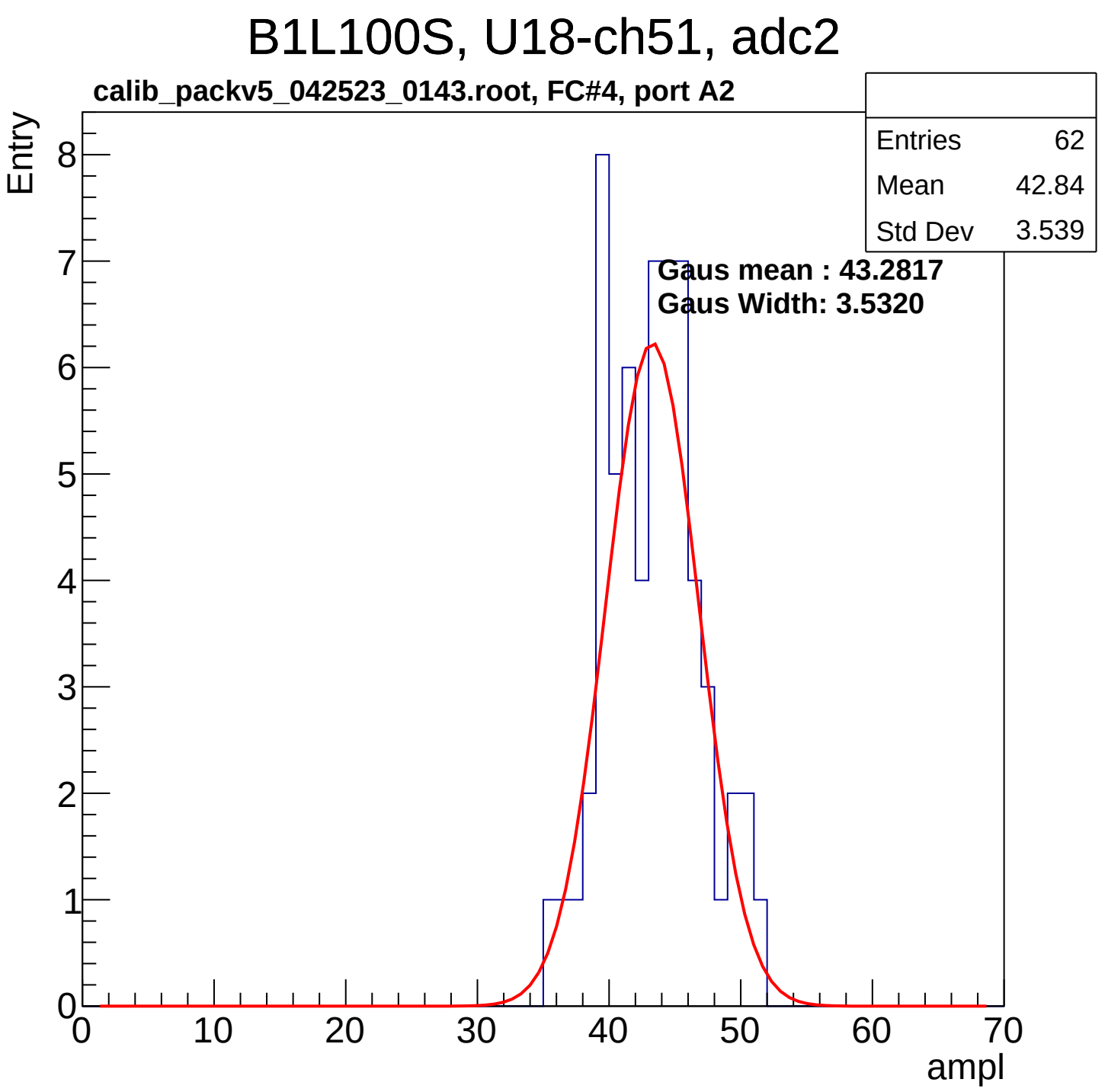

B1L100S, U18-ch50, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 45
Mean 58.64
Std Dev 9.173
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

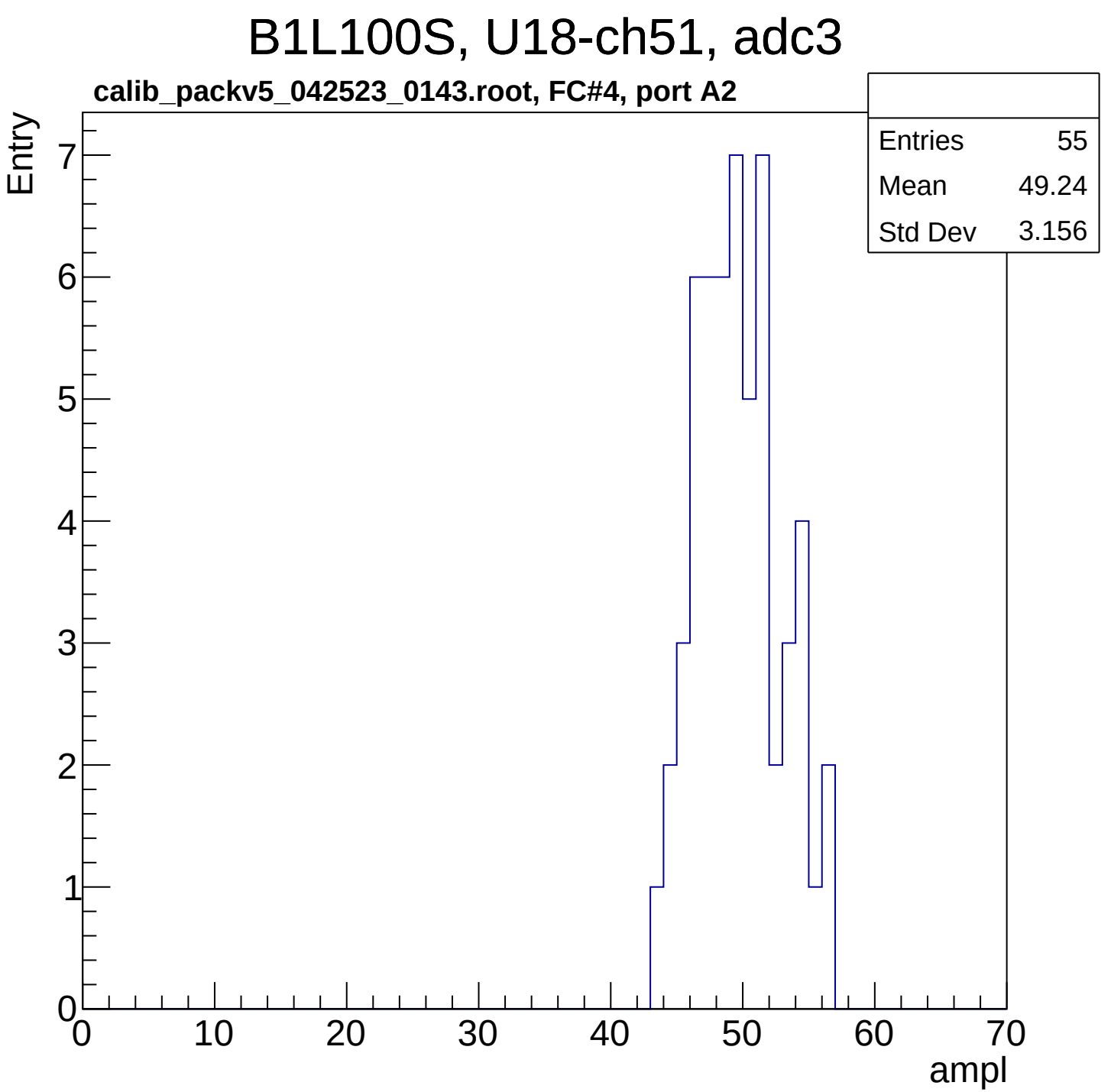

B1L100S, U18-ch50, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

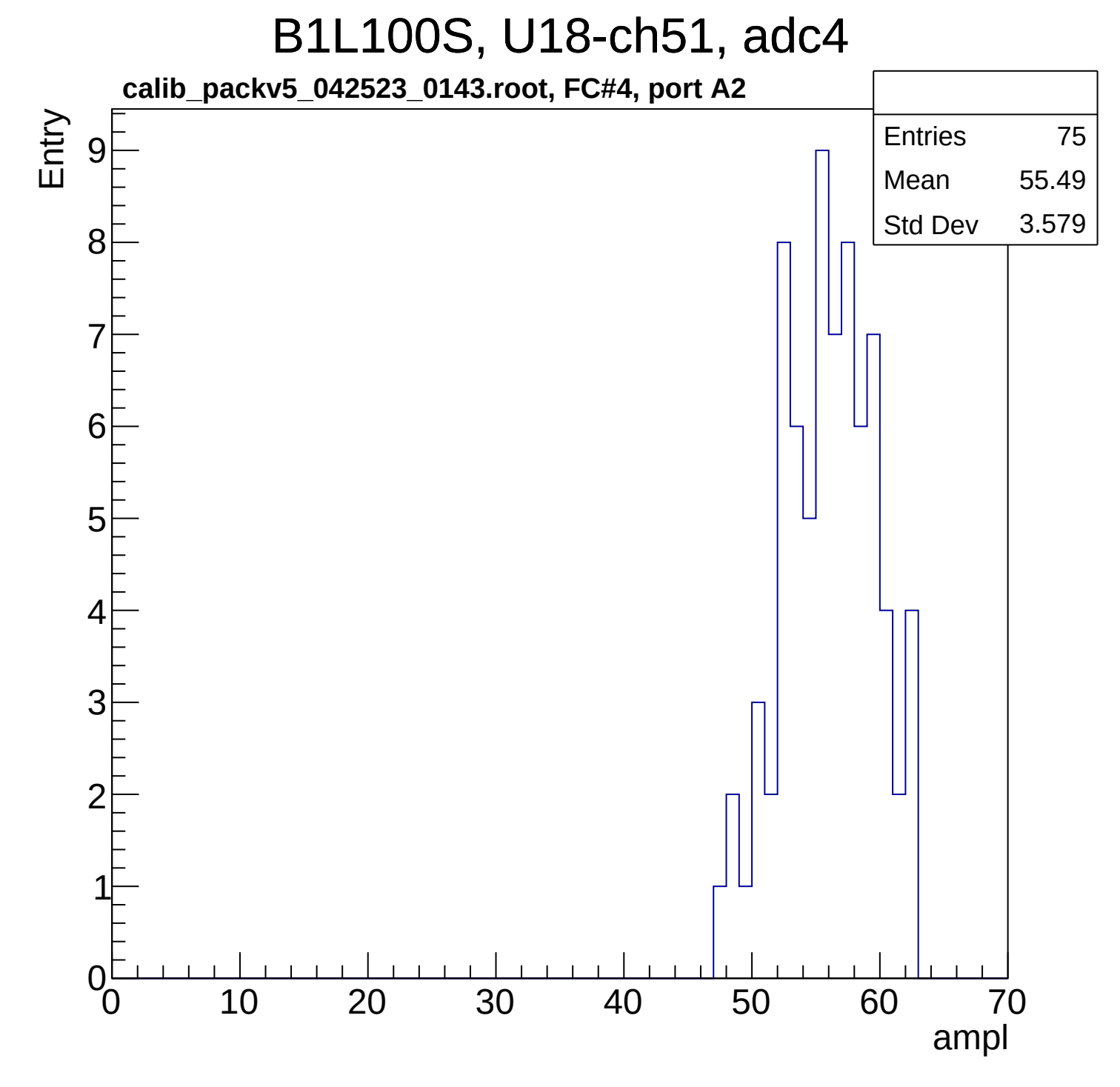

B1L100S, U18-ch50, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

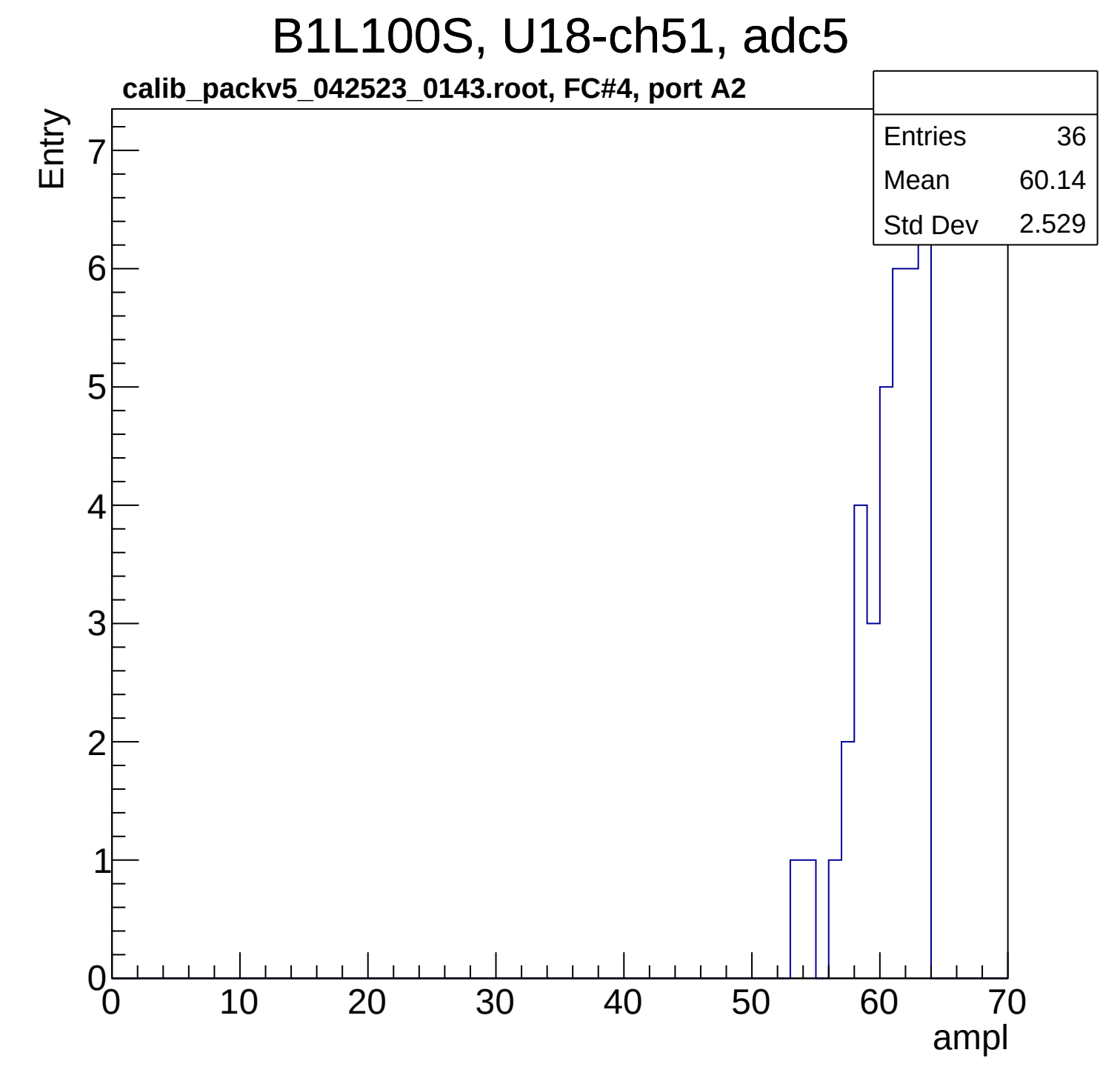

B1L100S, U18-ch51, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 89
Mean 28.96
Std Dev 3.894
Gaus mean : 29.1547
Gaus Width: 4.3588
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

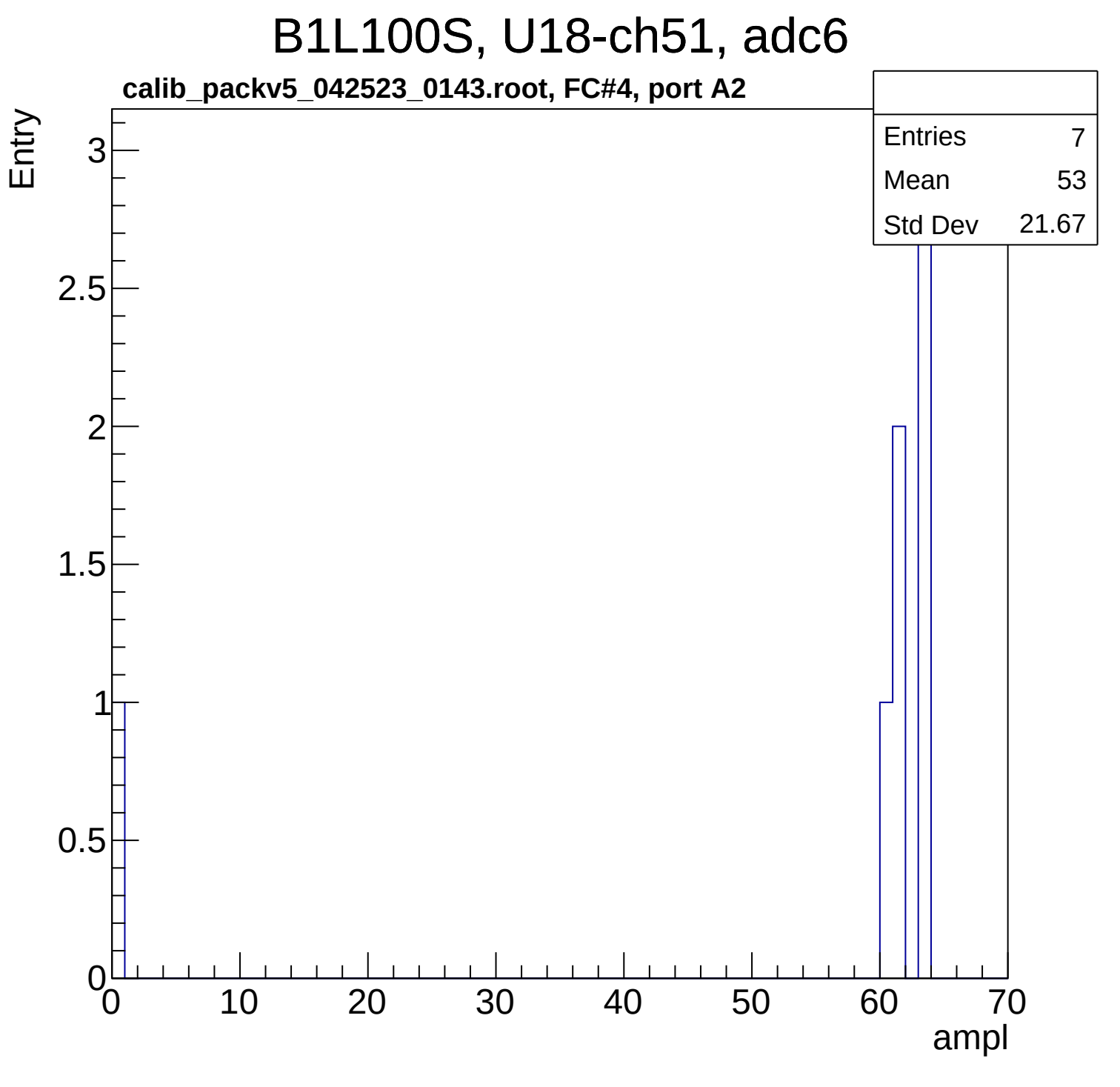

B1L100S, U18-ch51, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 36.97
Std Dev 3.777
Gaus mean : 37.1151
Gaus Width: 4.3109
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

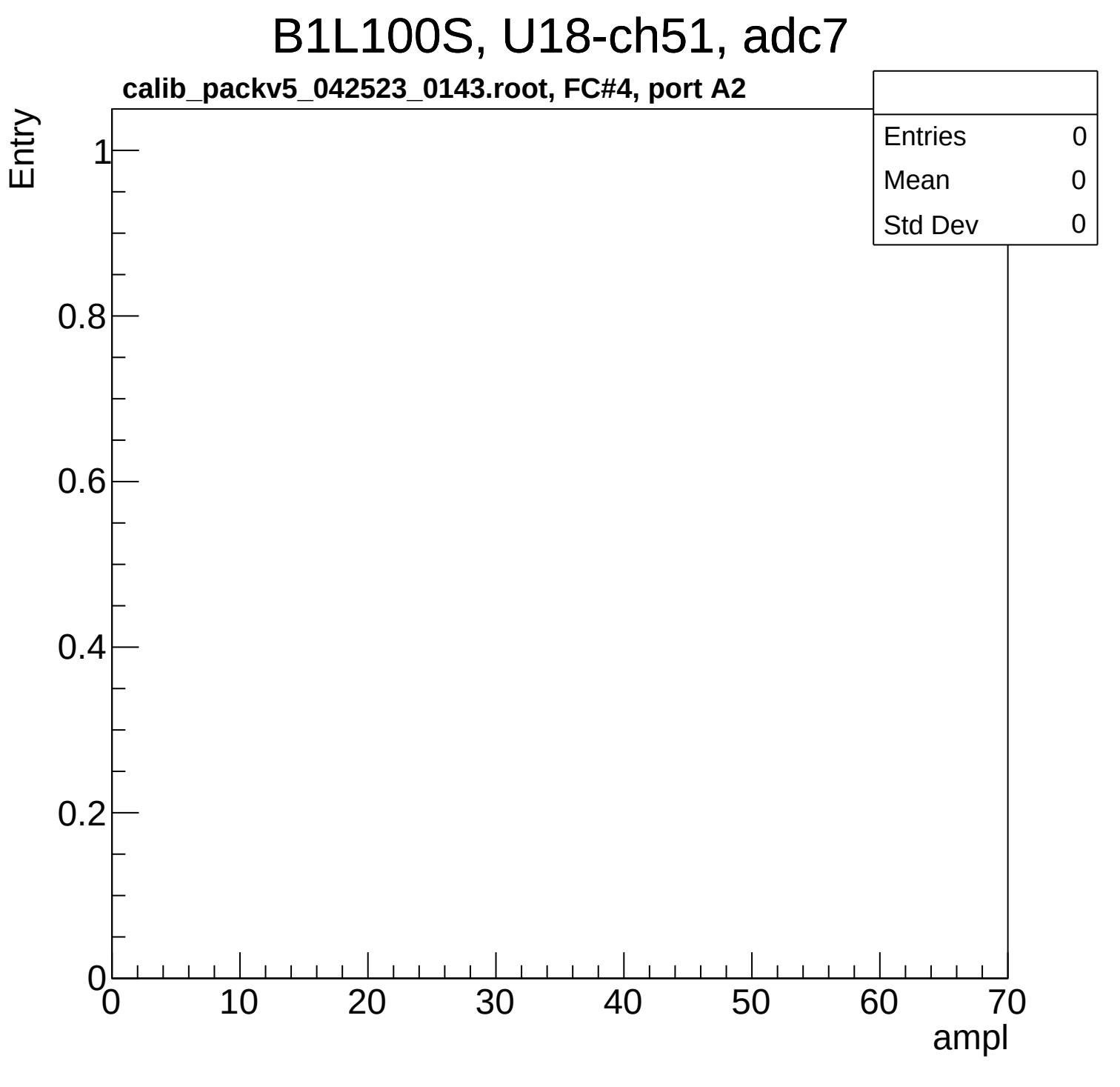

B1L100S, U18-ch51, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 42.84
Std Dev 3.539
Gaus mean : 43.2817
Gaus Width: 3.5320
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

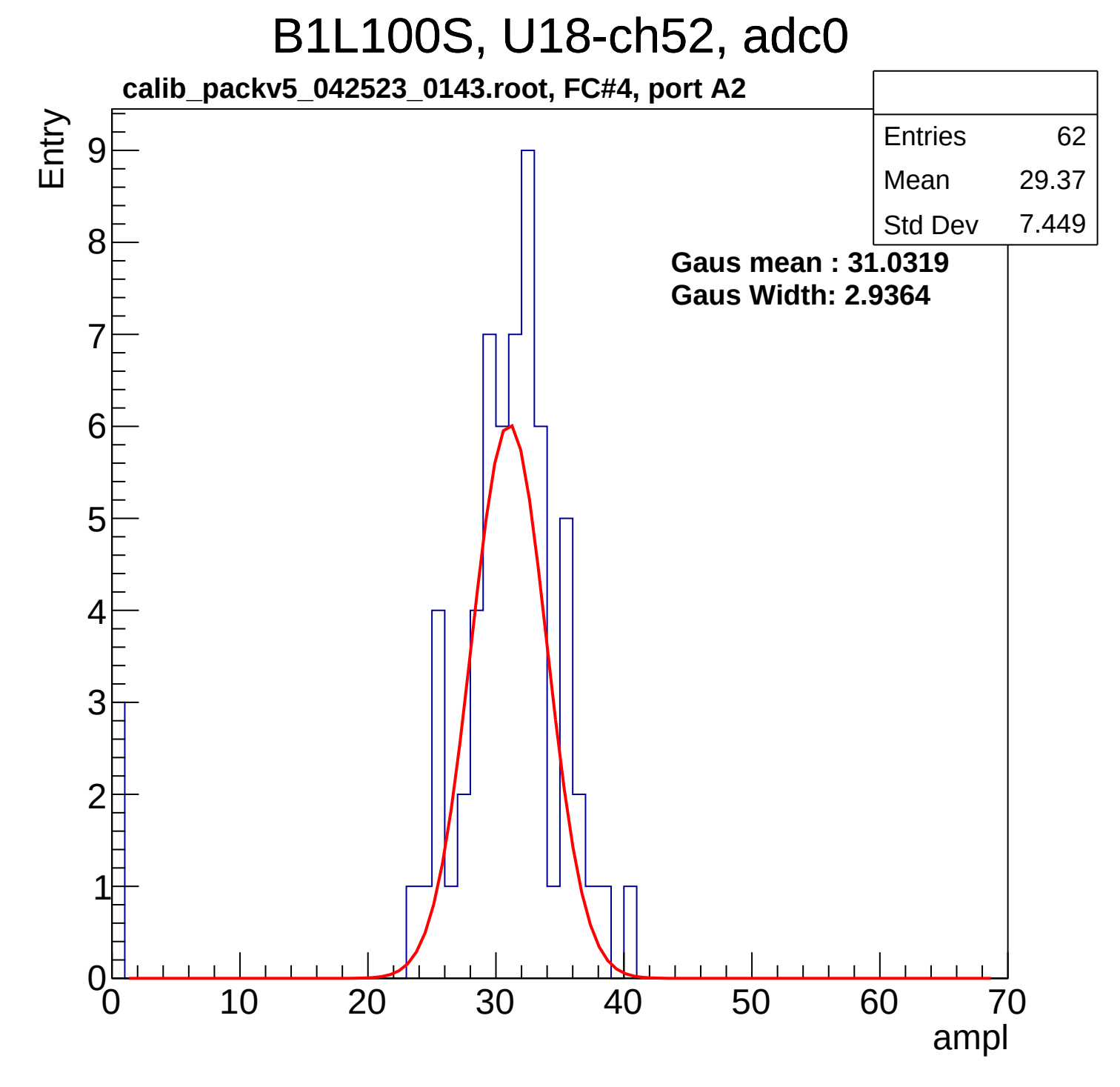

B1L100S, U18-ch51, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 49.24
Std Dev 3.156
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

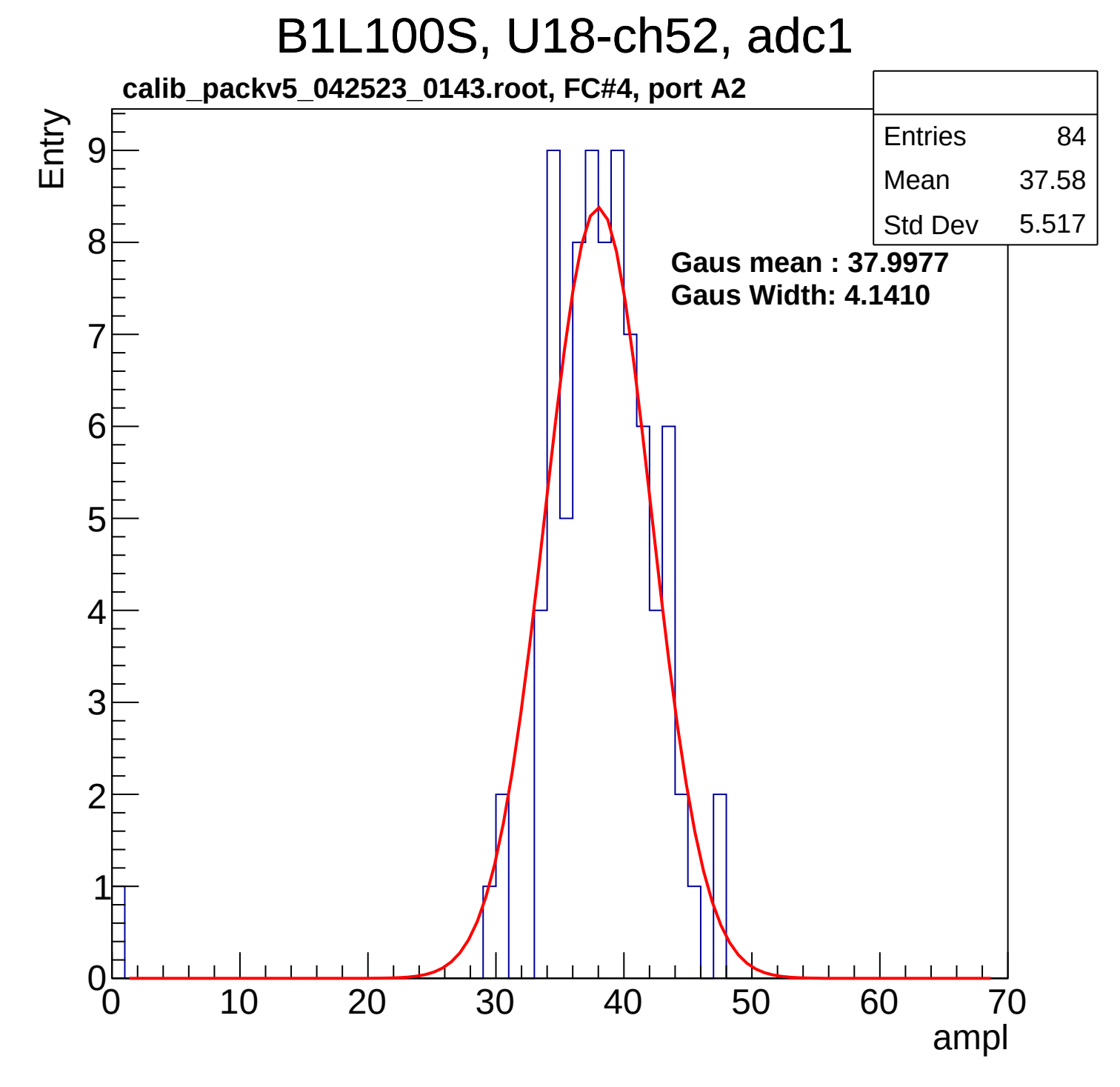

B1L100S, U18-ch51, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 55.49
Std Dev 3.579
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

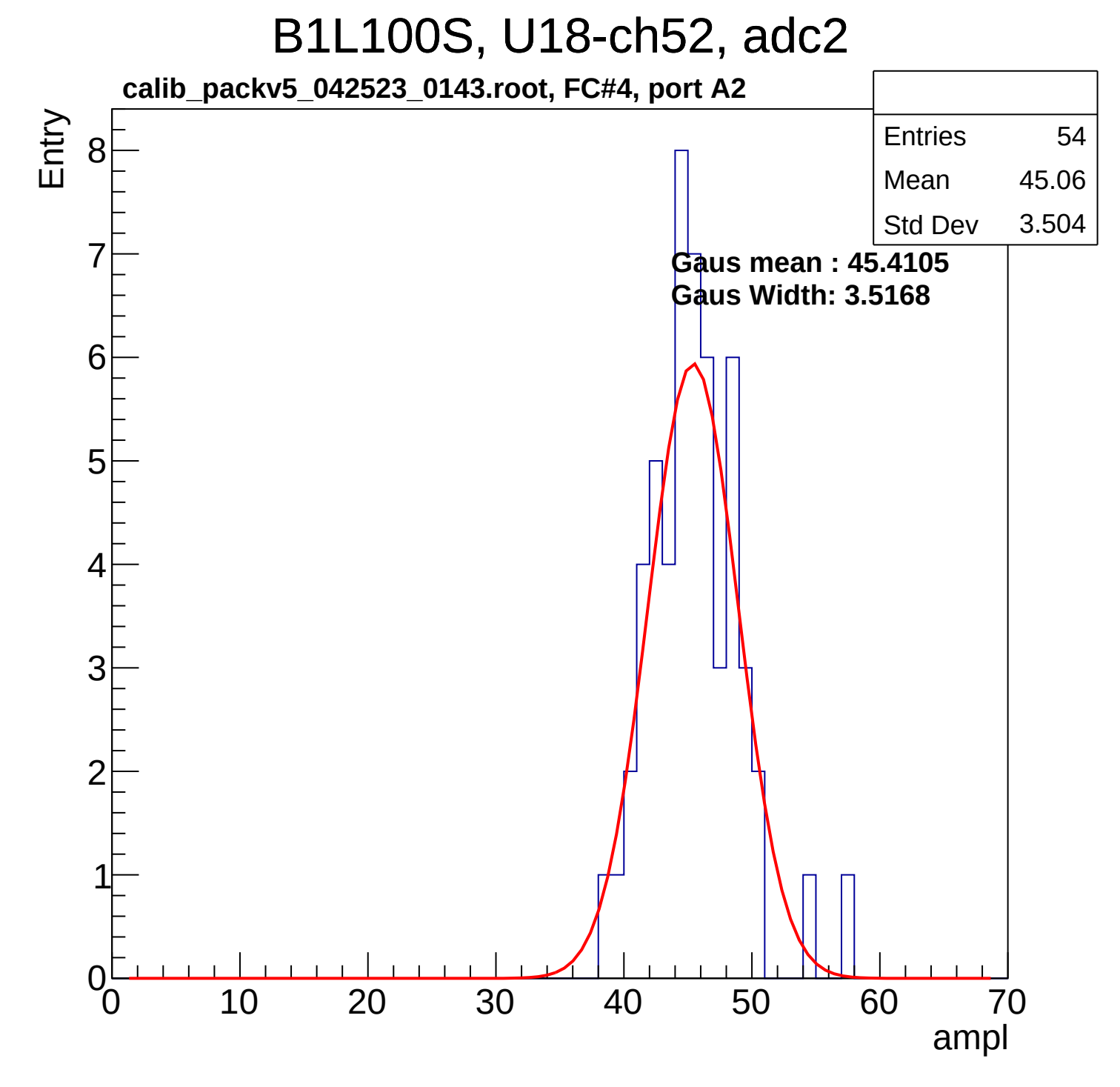

B1L100S, U18-ch51, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 36
Mean 60.14
Std Dev 2.529
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

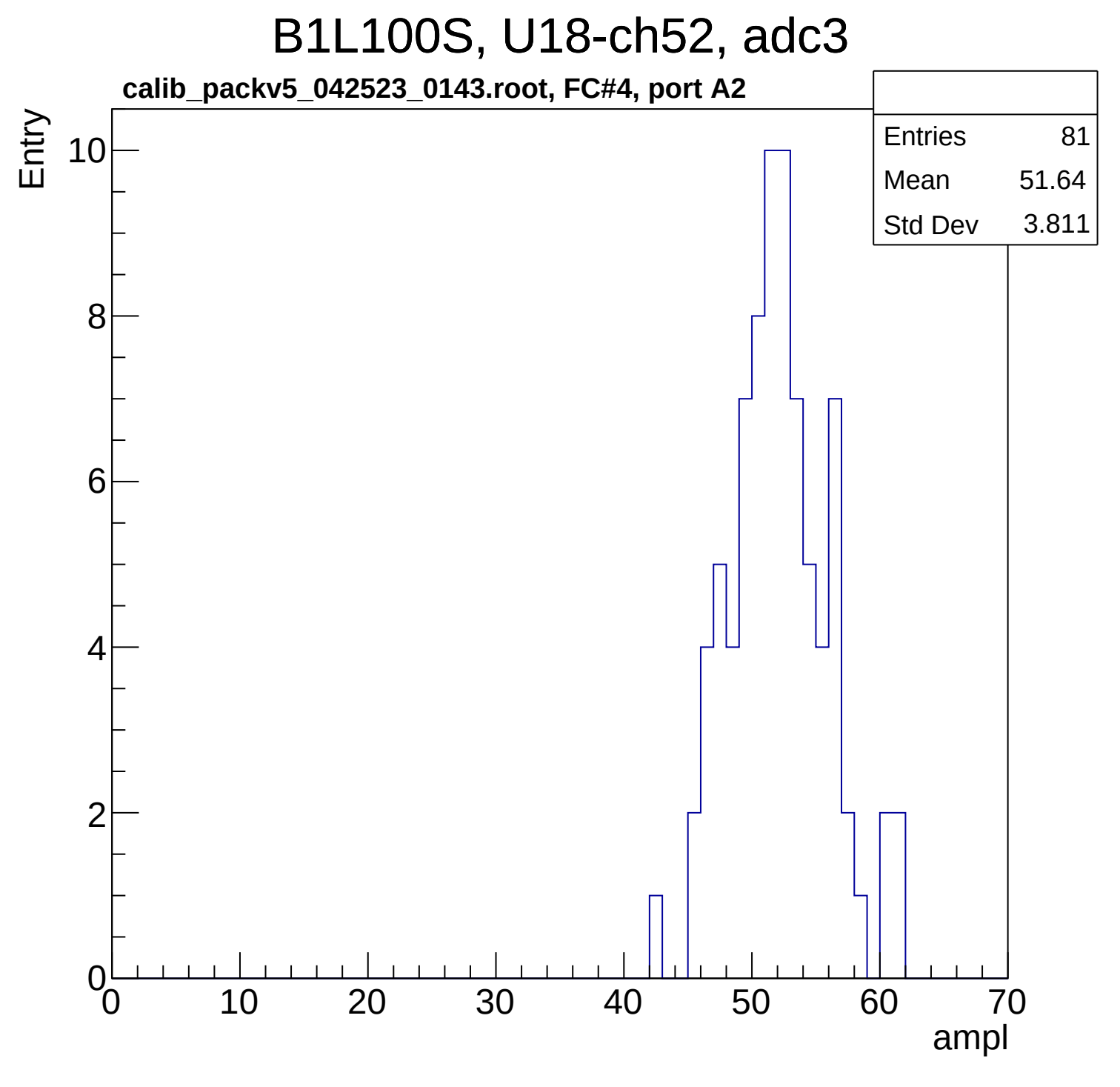

B1L100S, U18-ch51, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 53
Std Dev 21.67
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

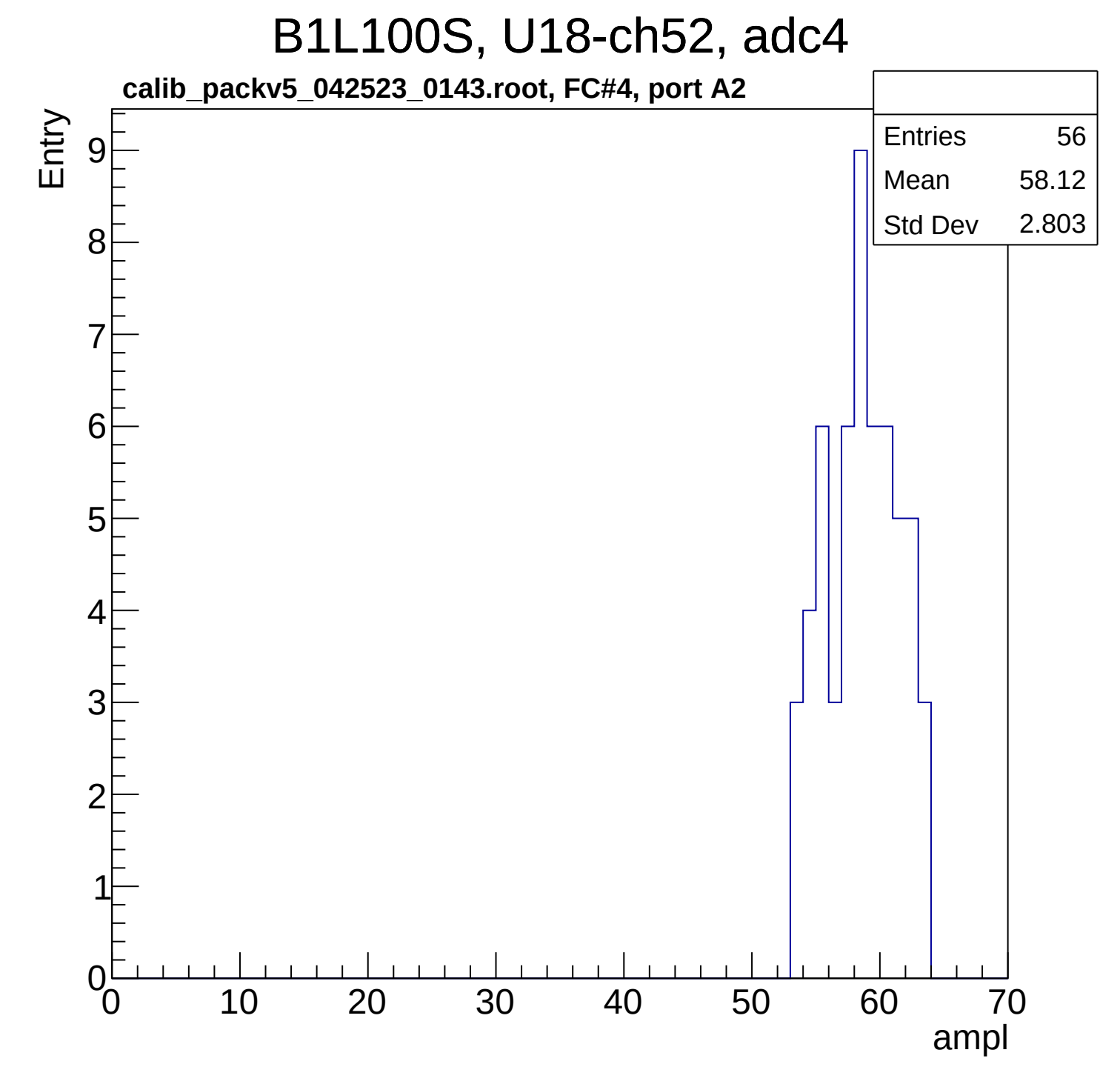

B1L100S, U18-ch51, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

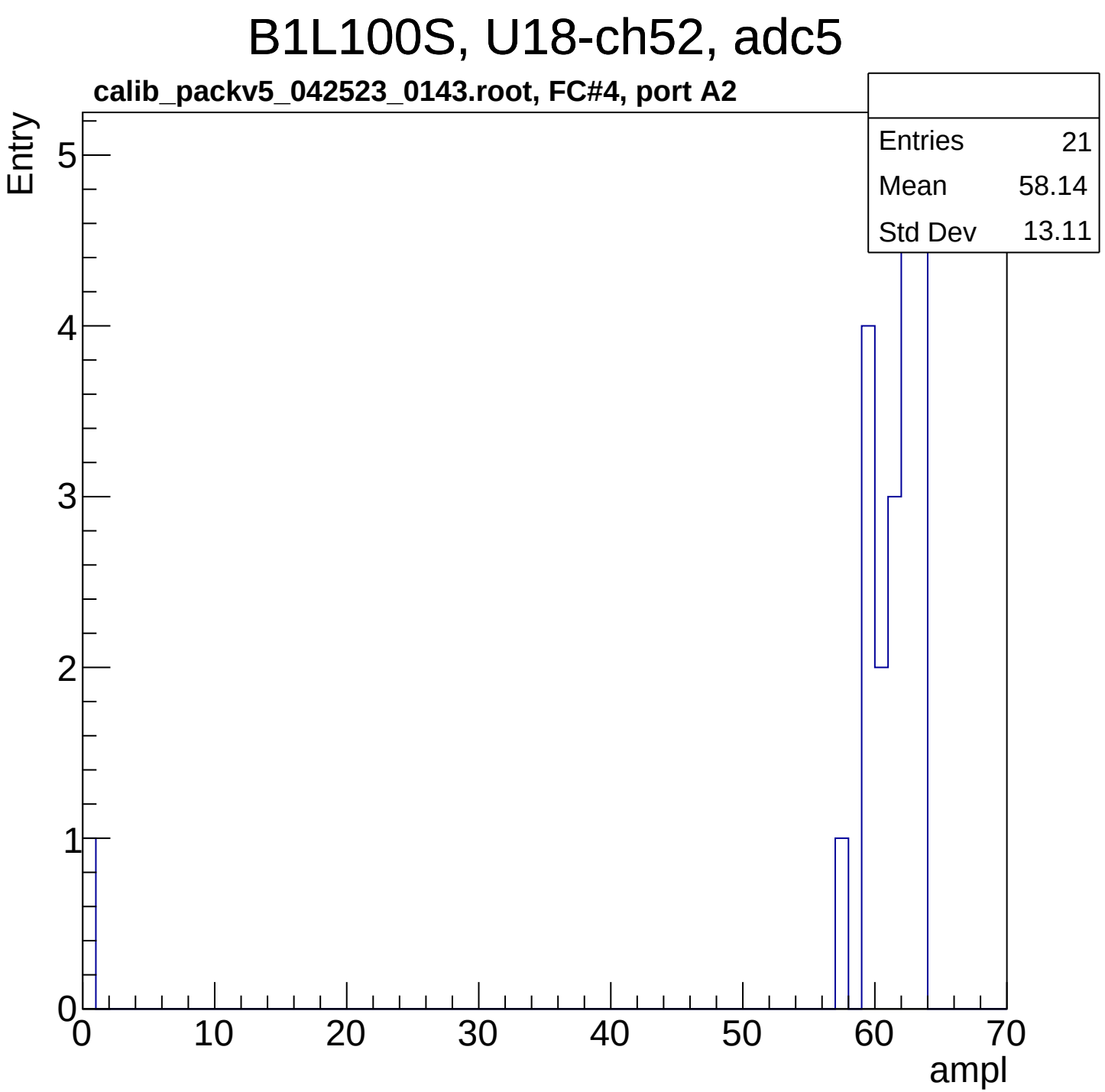

B1L100S, U18-ch52, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 29.37
Std Dev 7.449
Gaus mean : 31.0319
Gaus Width: 2.9364
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

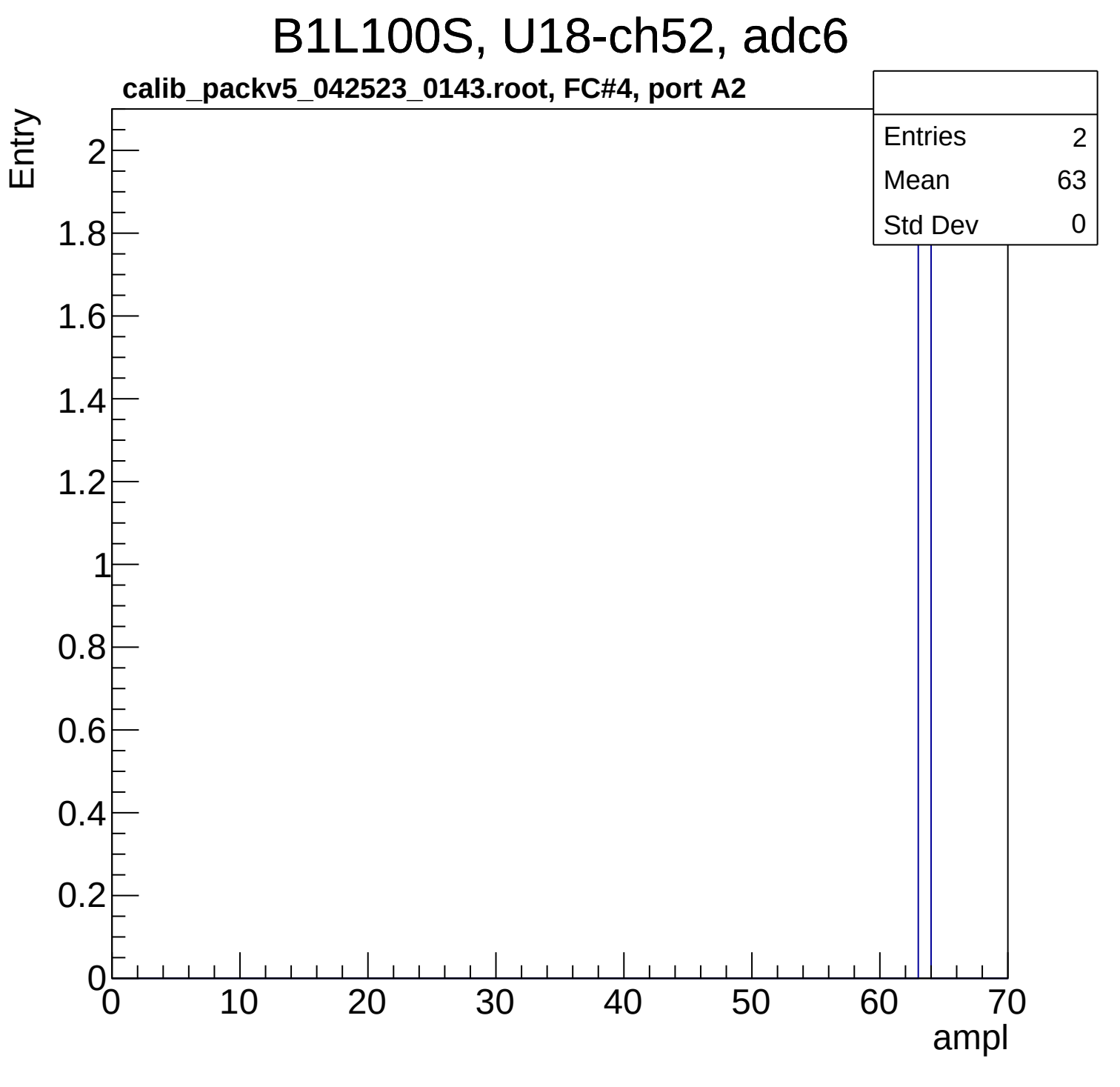

B1L100S, U18-ch52, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 84
Mean 37.58
Std Dev 5.517
Gaus mean : 37.9977
Gaus Width: 4.1410
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

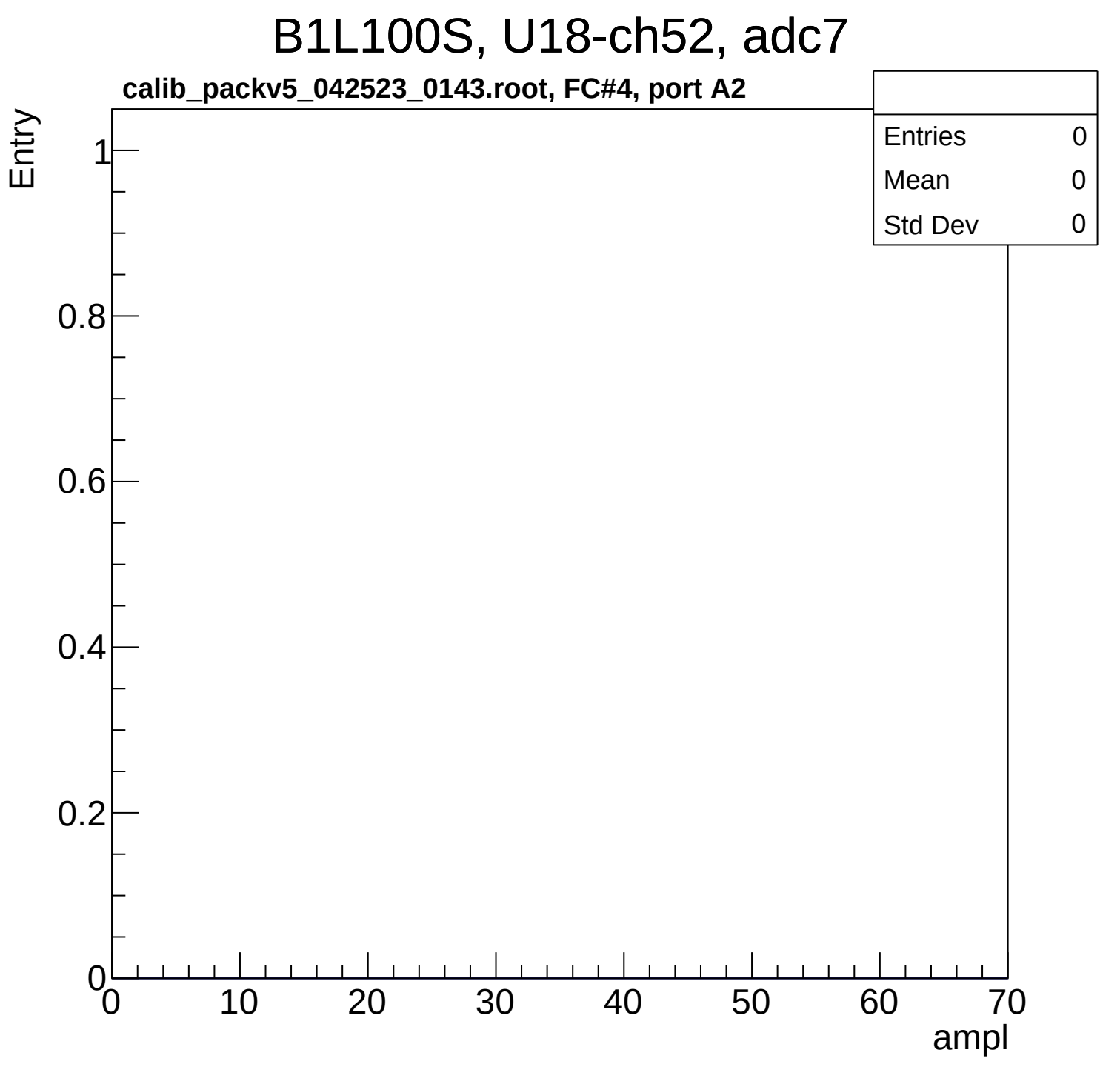

B1L100S, U18-ch52, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 45.06
Std Dev 3.504
Gaus mean : 45.4105
Gaus Width: 3.5168
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

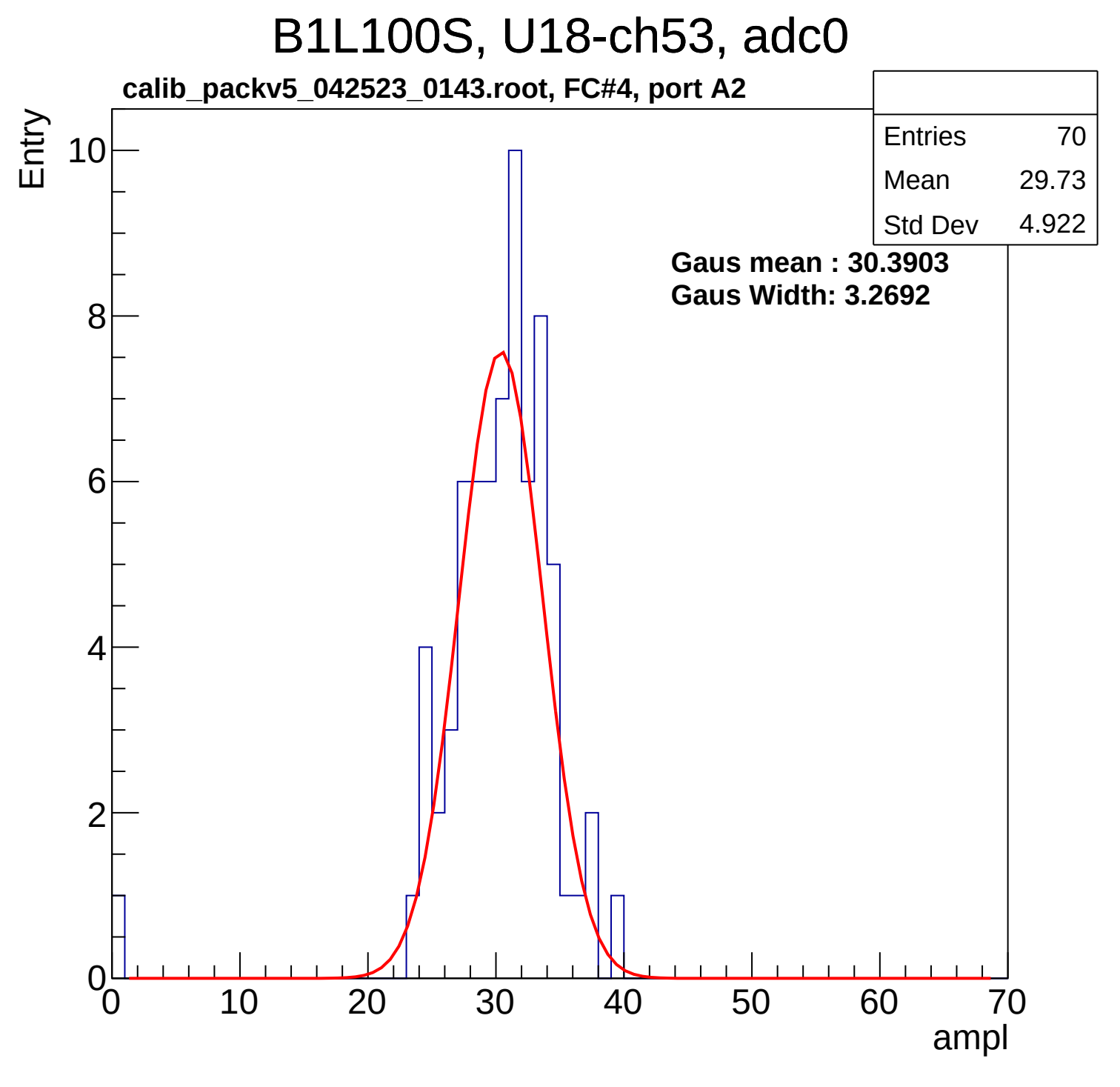

B1L100S, U18-ch52, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 51.64
Std Dev 3.811
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

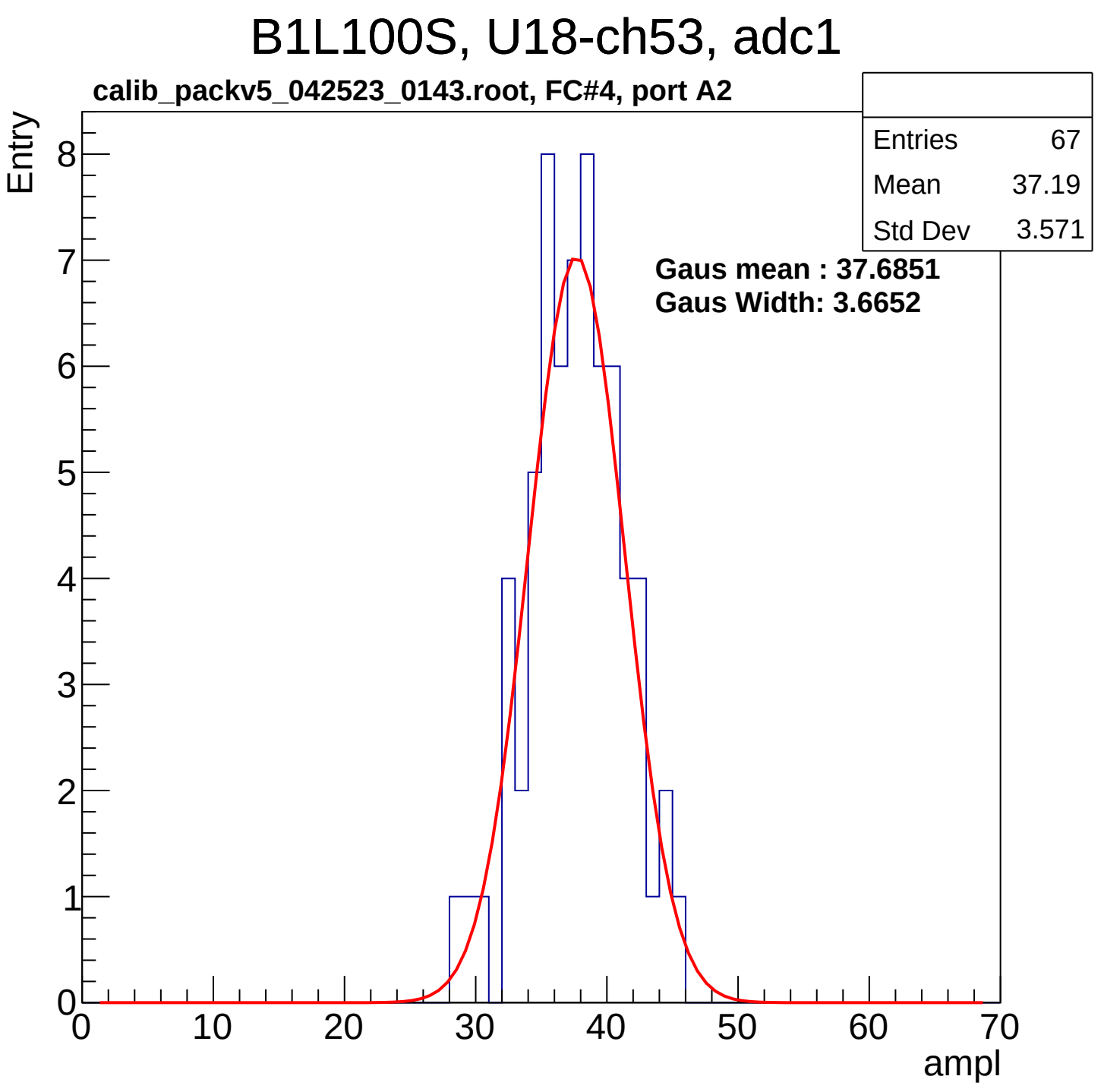

B1L100S, U18-ch52, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 58.12
Std Dev 2.803
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

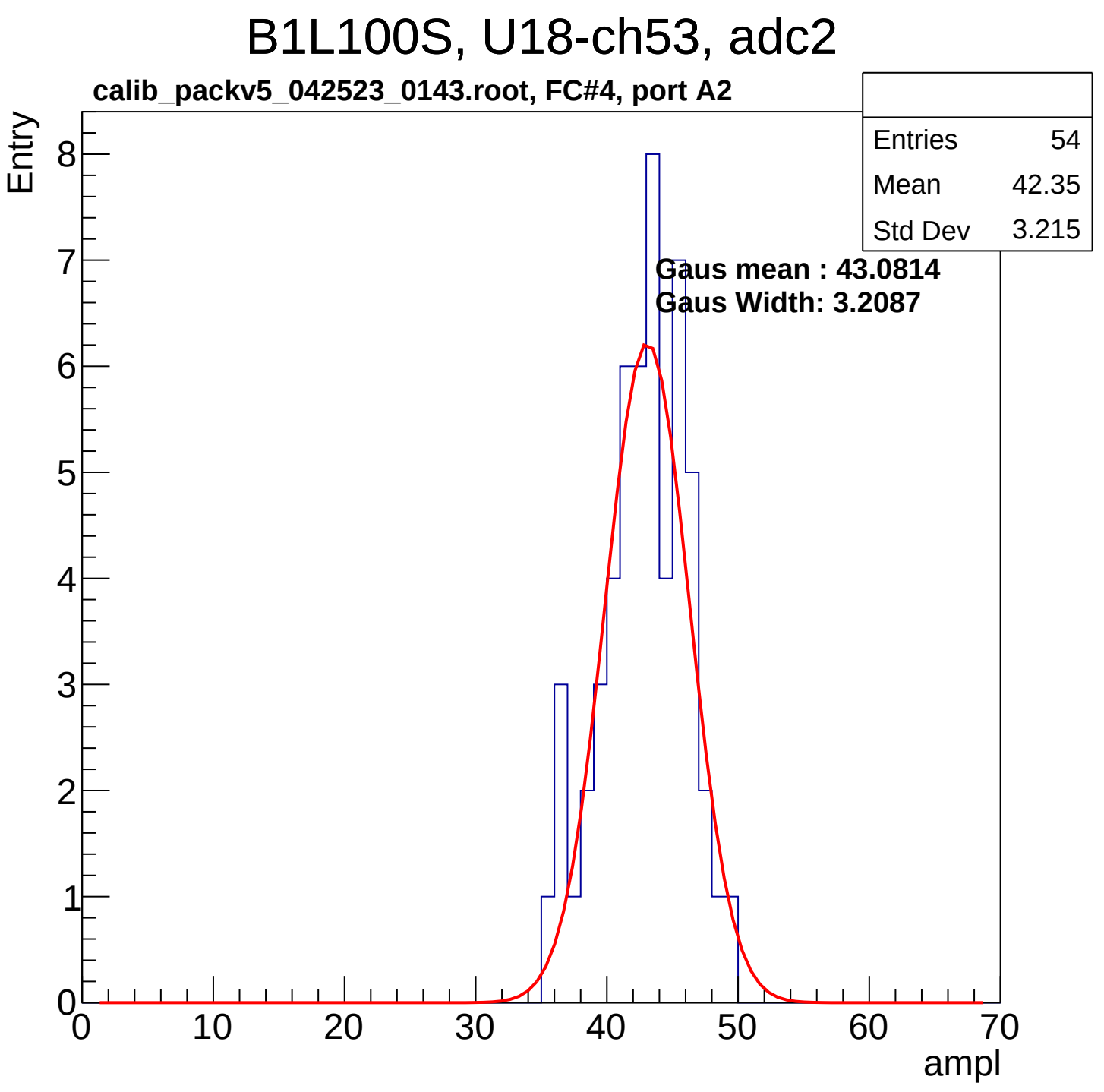

B1L100S, U18-ch52, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 21
Mean 58.14
Std Dev 13.11
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

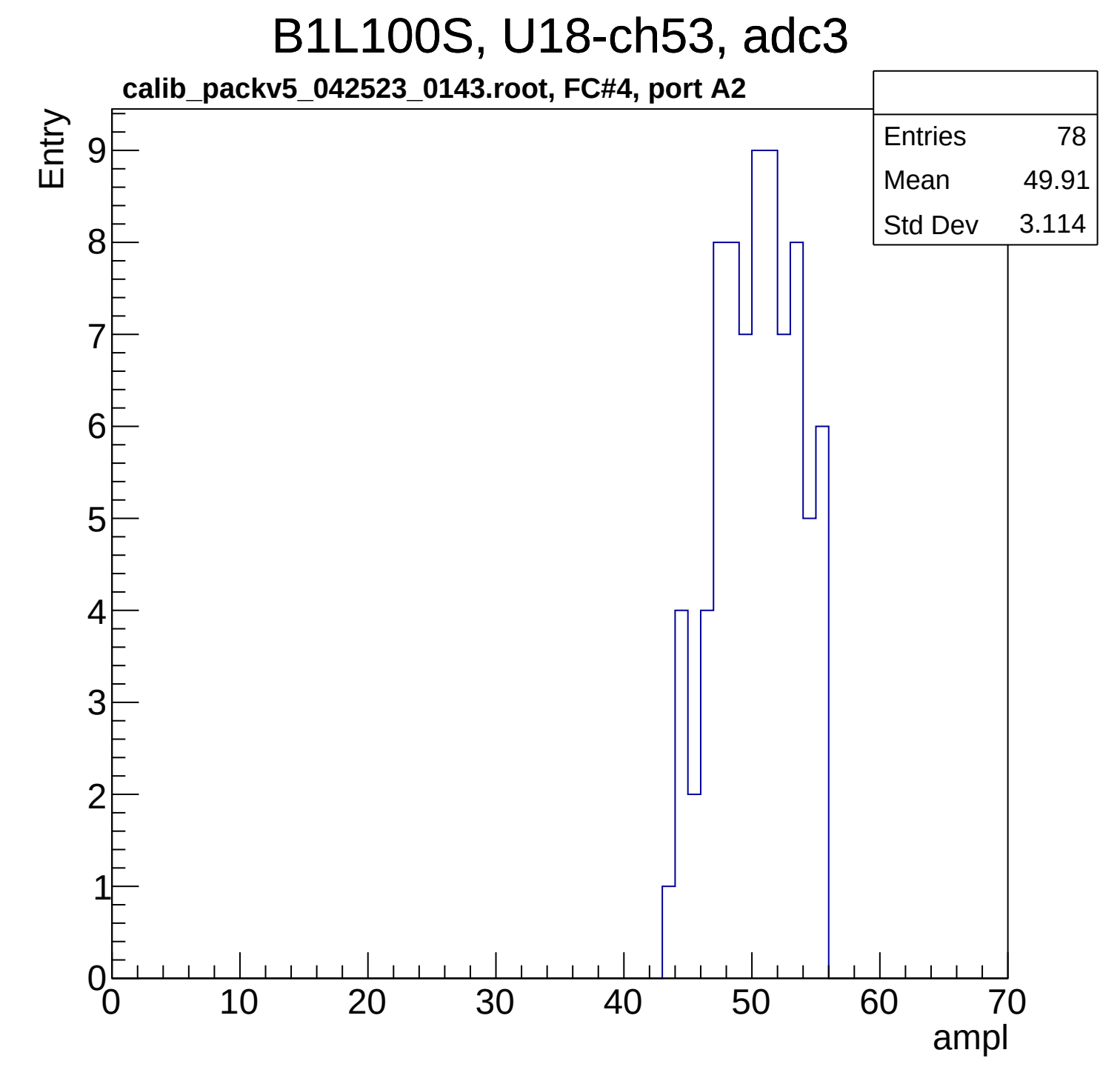

B1L100S, U18-ch52, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

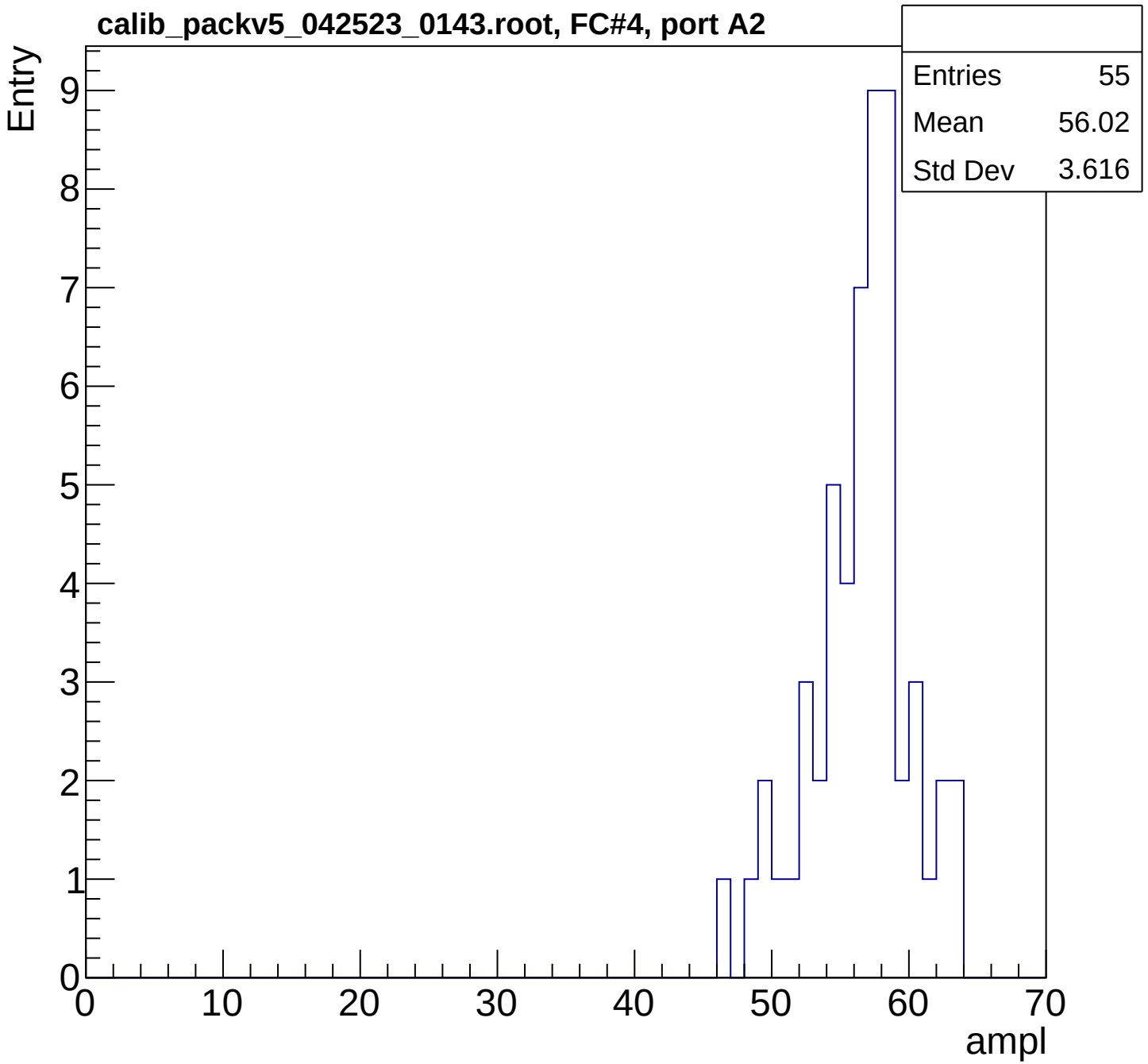

B1L100S, U18-ch52, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

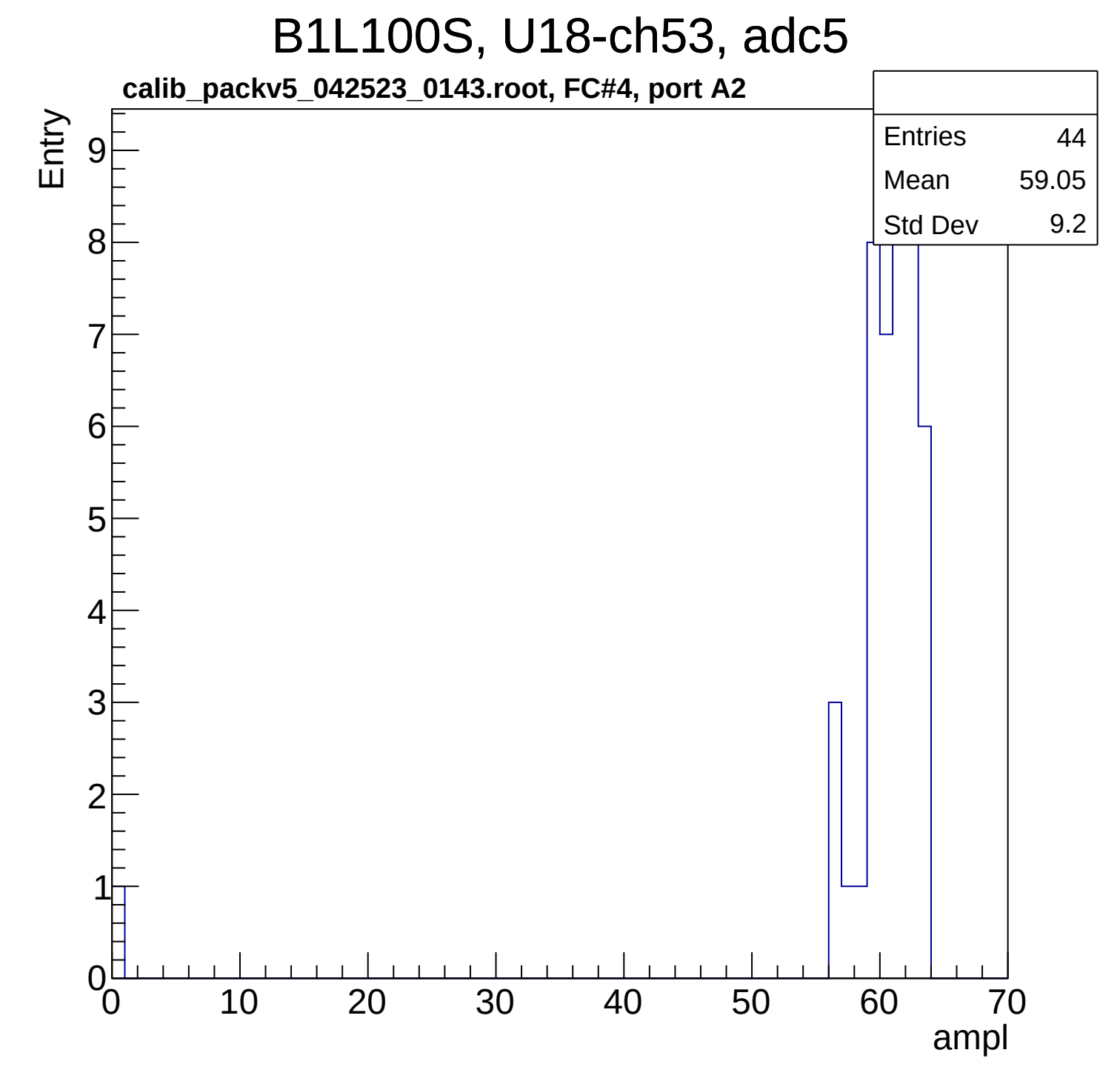

B1L100S, U18-ch53, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 29.73
Std Dev 4.922
Gaus mean : 30.3903
Gaus Width: 3.2692
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

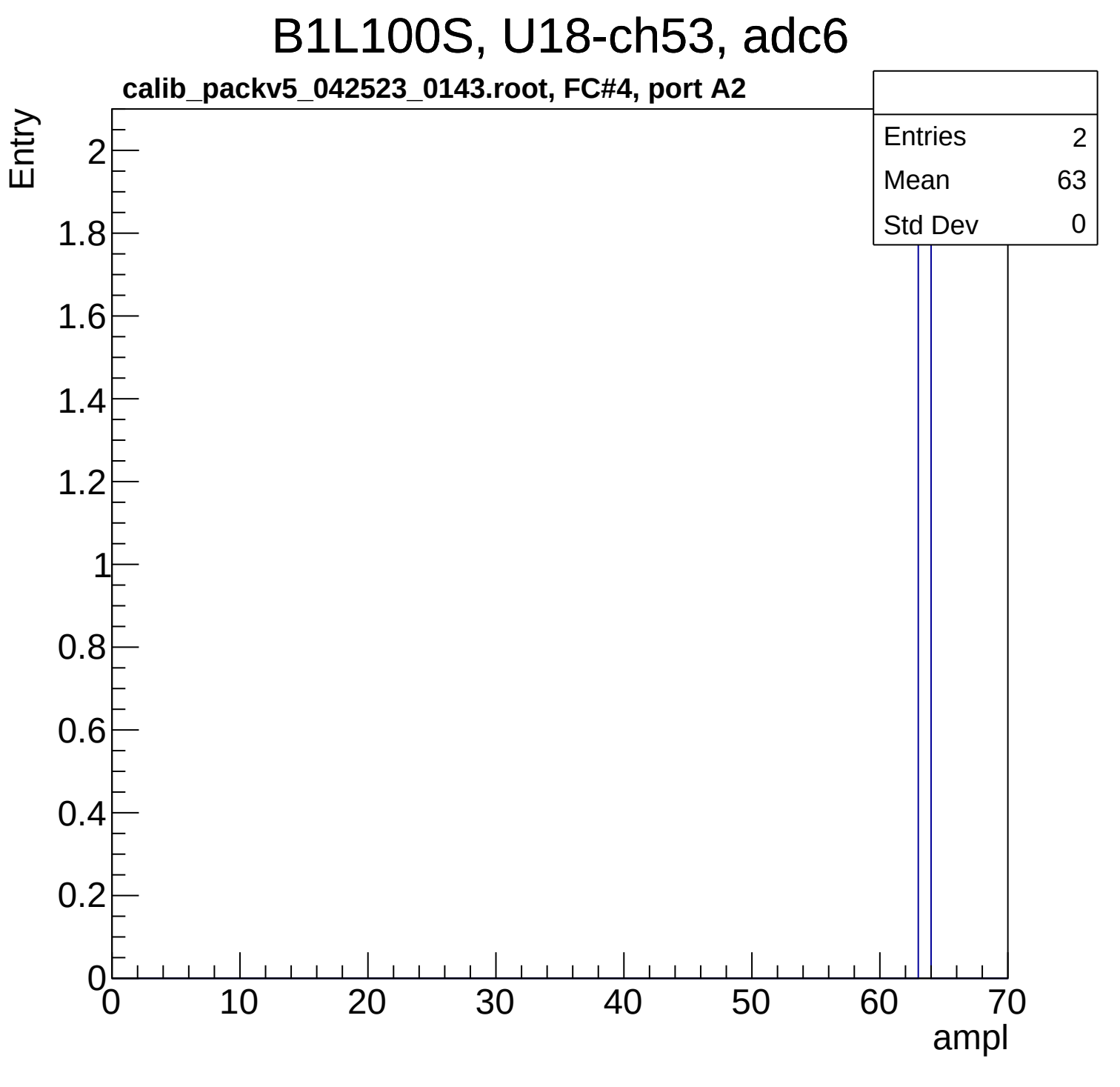

B1L100S, U18-ch53, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 37.19
Std Dev 3.571
Gaus mean : 37.6851
Gaus Width: 3.6652
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

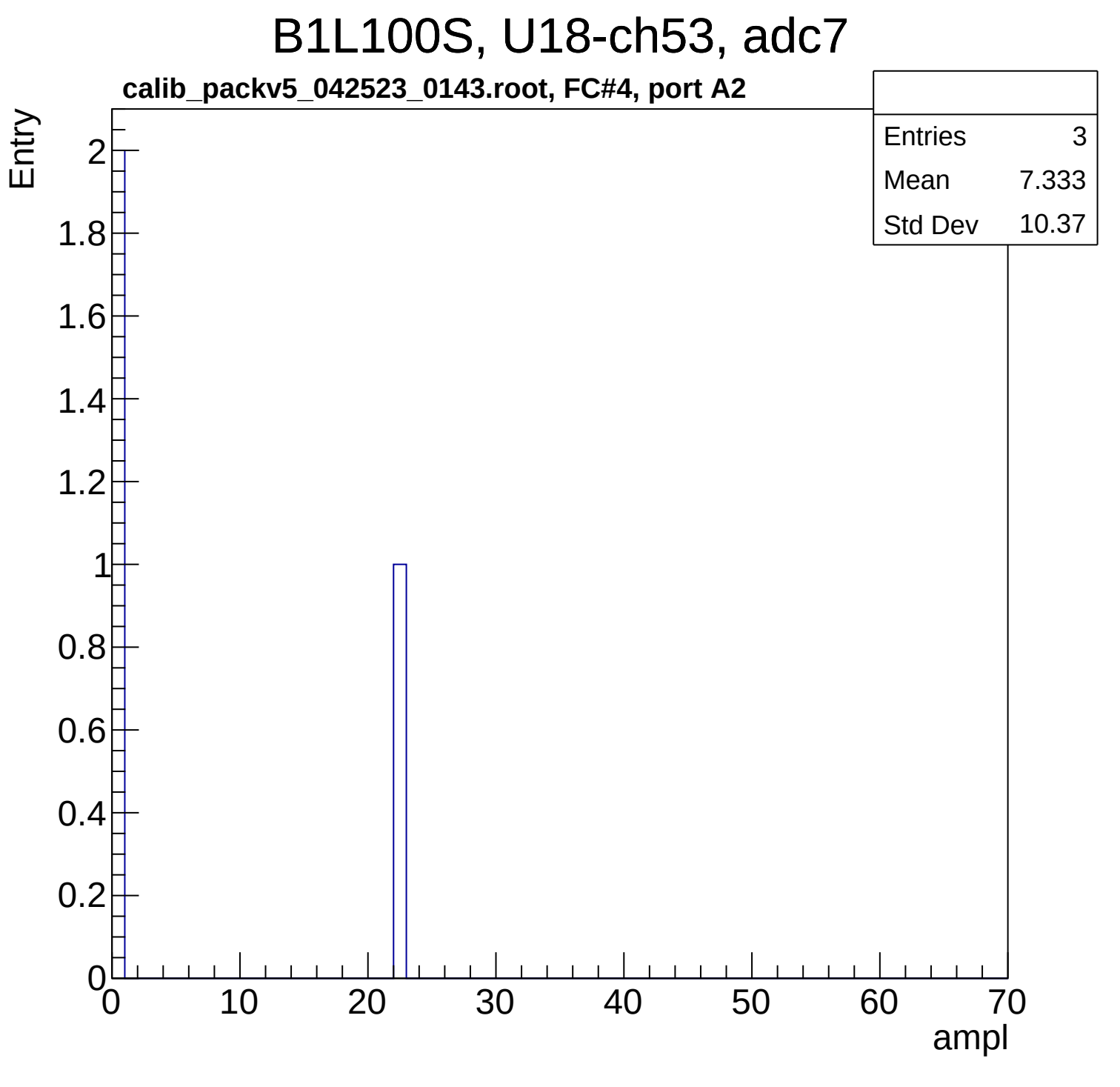

B1L100S, U18-ch53, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 42.35
Std Dev 3.215
Gaus mean : 43.0814
Gaus Width: 3.2087
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

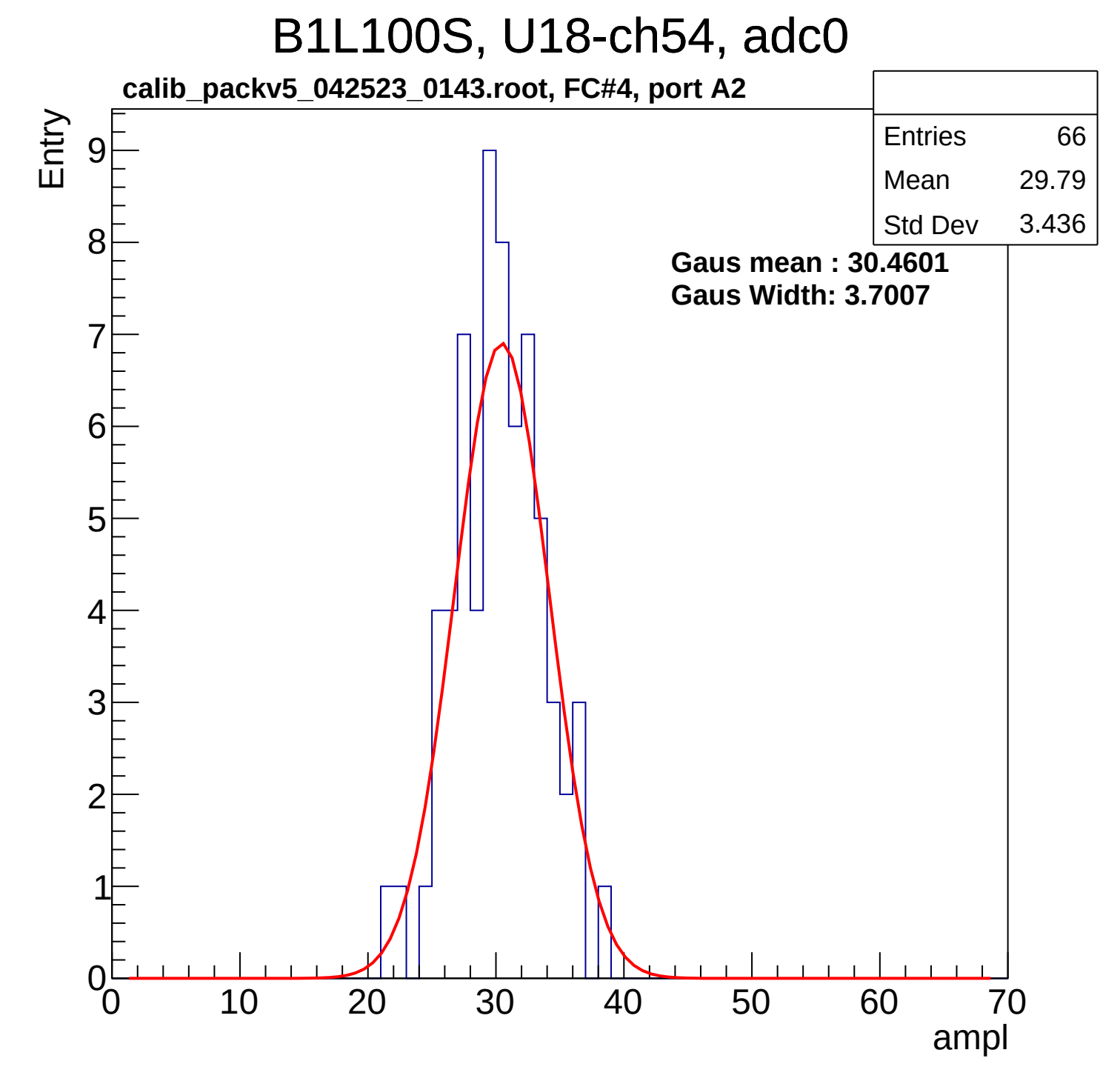

B1L100S, U18-ch53, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 49.91
Std Dev 3.114
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

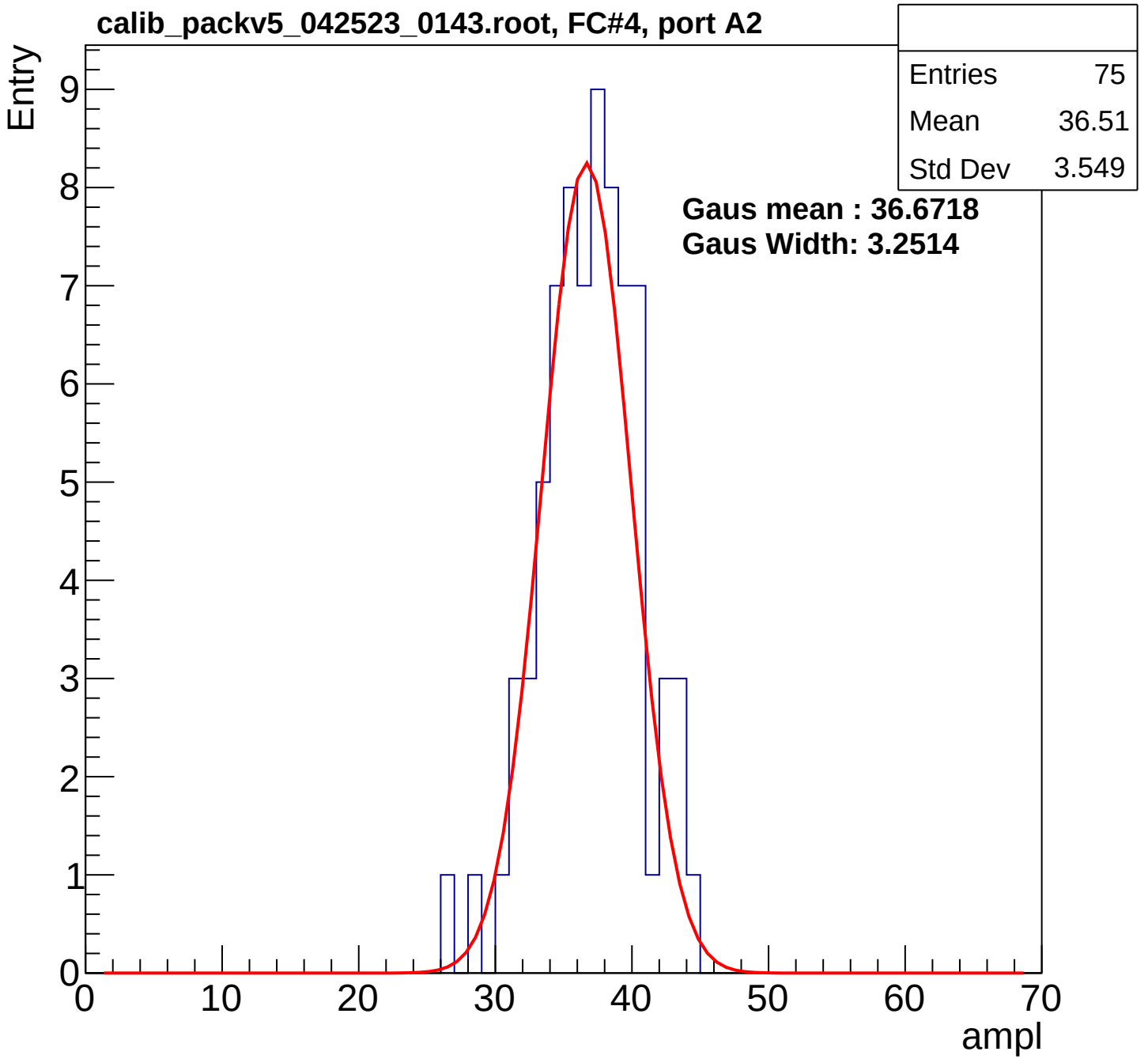

B1L100S, U18-ch53, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 56.02
Std Dev 3.616
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

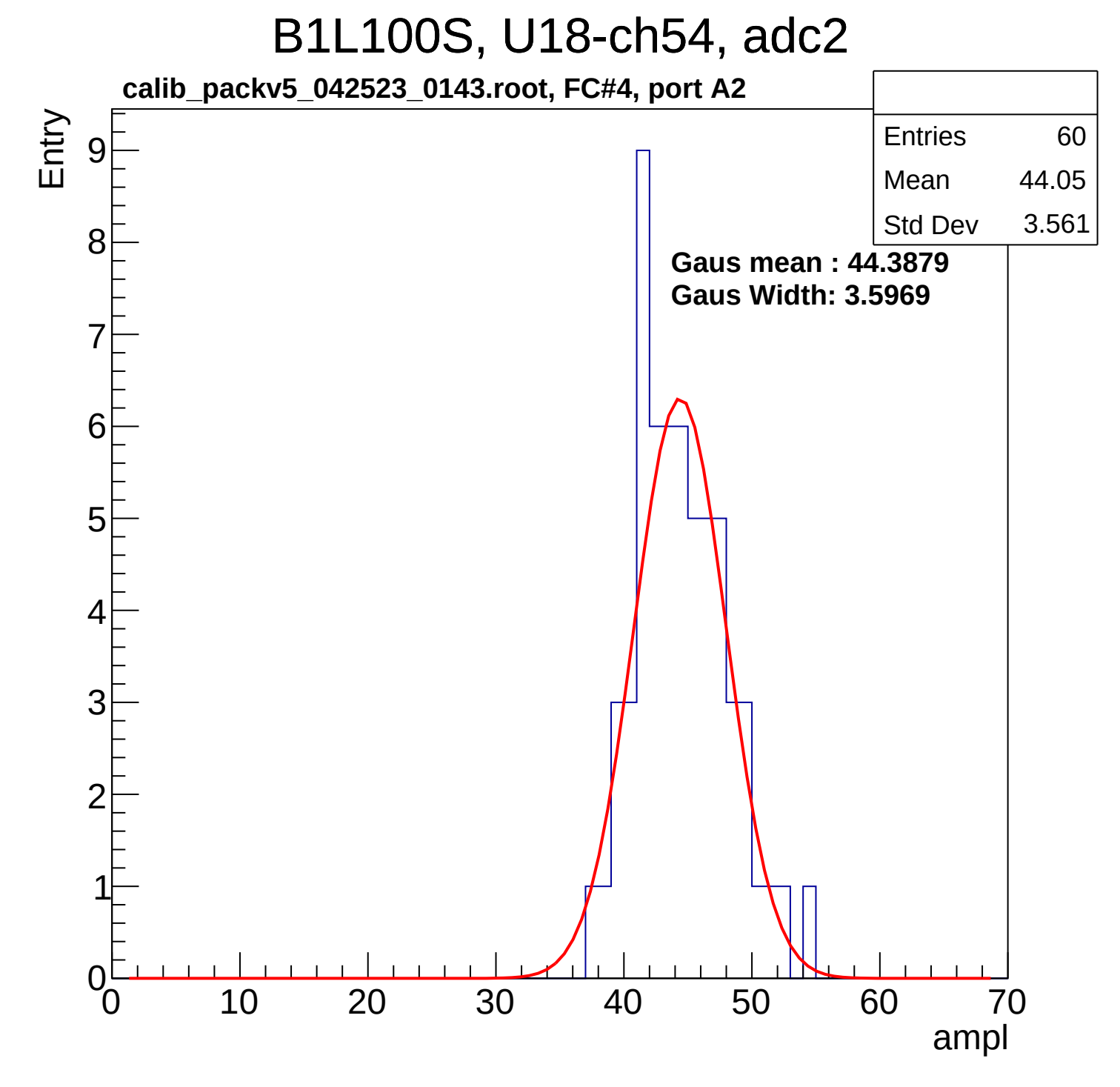

B1L100S, U18-ch53, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 44
Mean 59.05
Std Dev 9.2
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

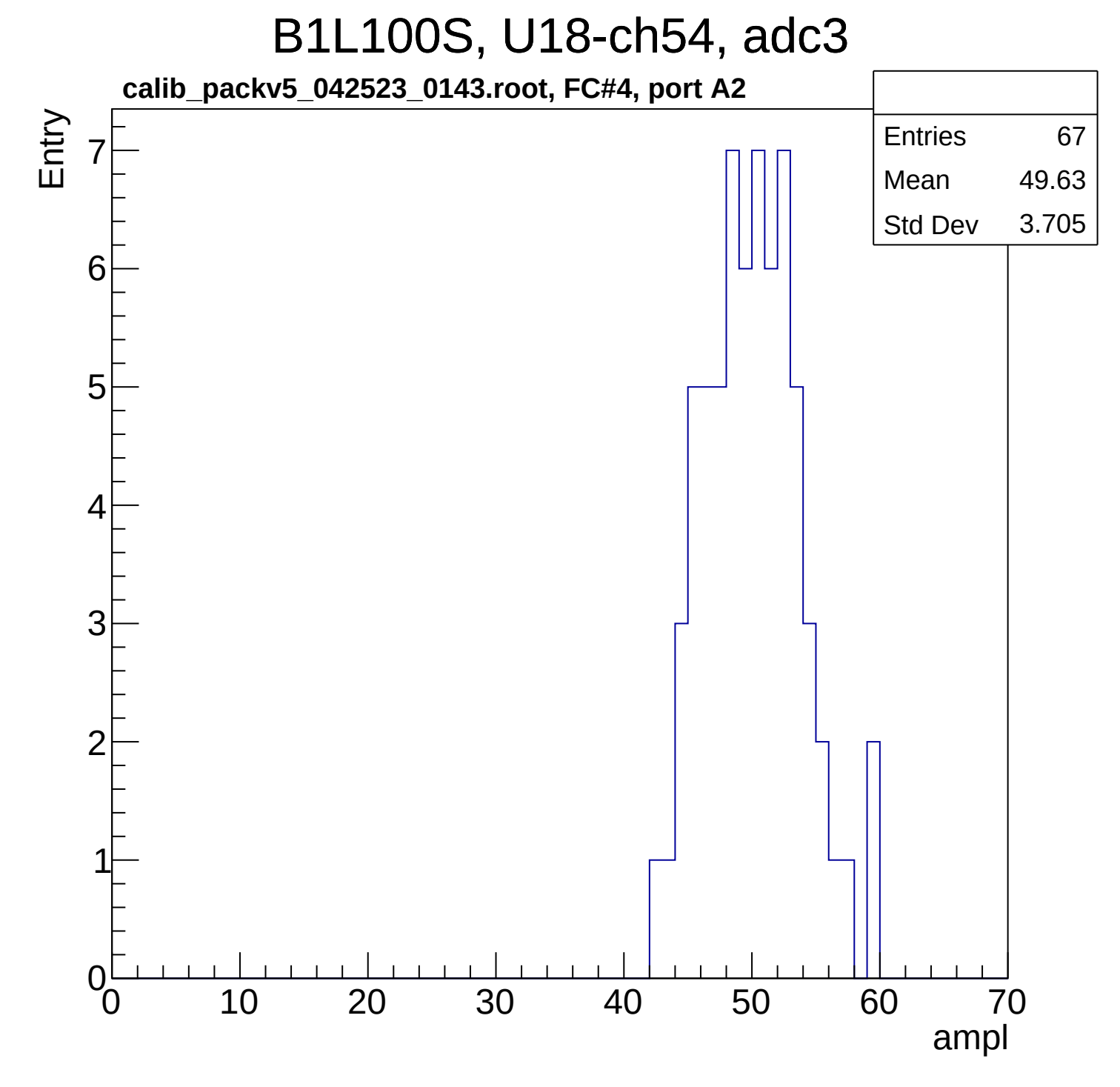

B1L100S, U18-ch53, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

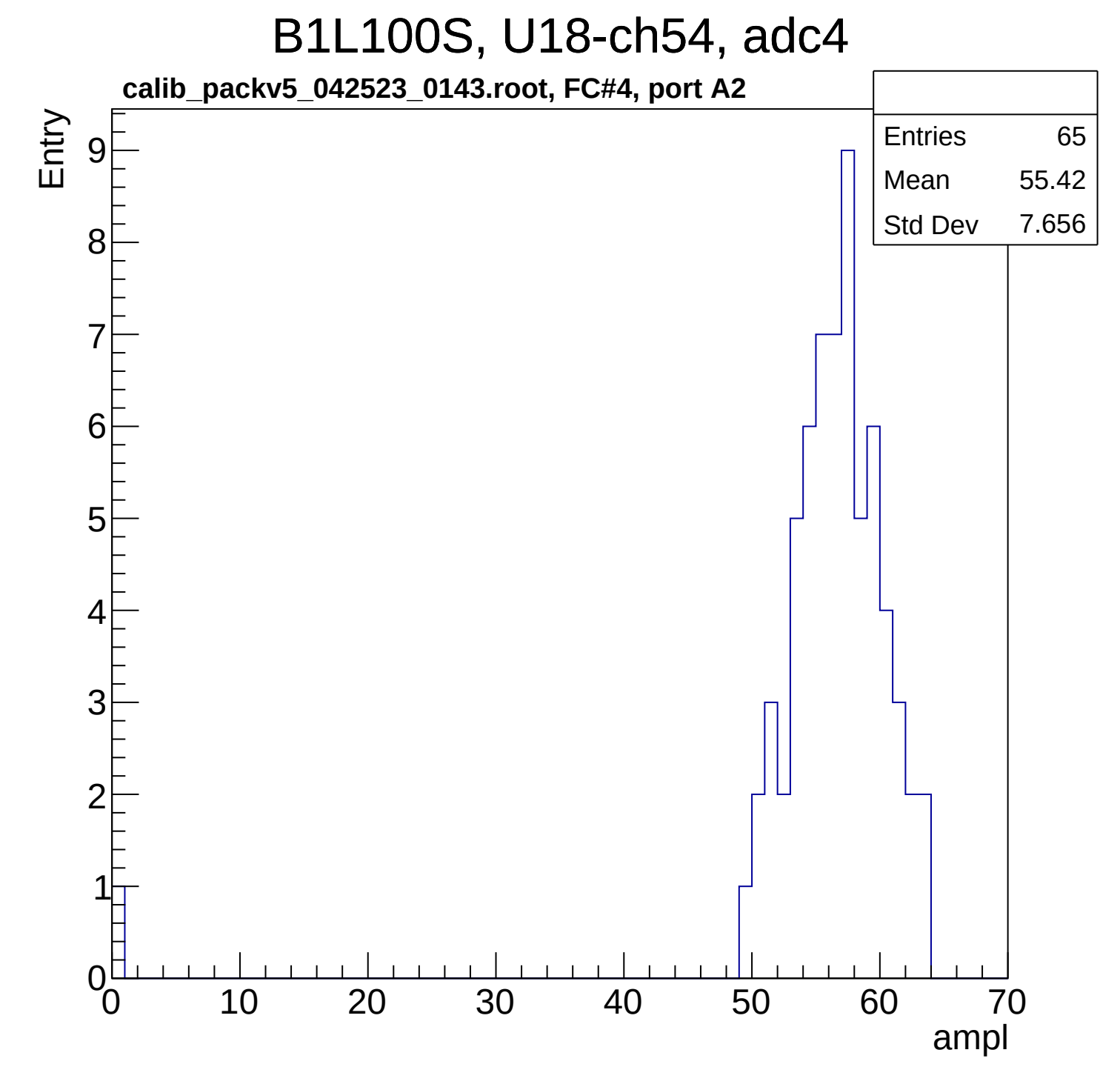

B1L100S, U18-ch53, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 7.333
Std Dev 10.37
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

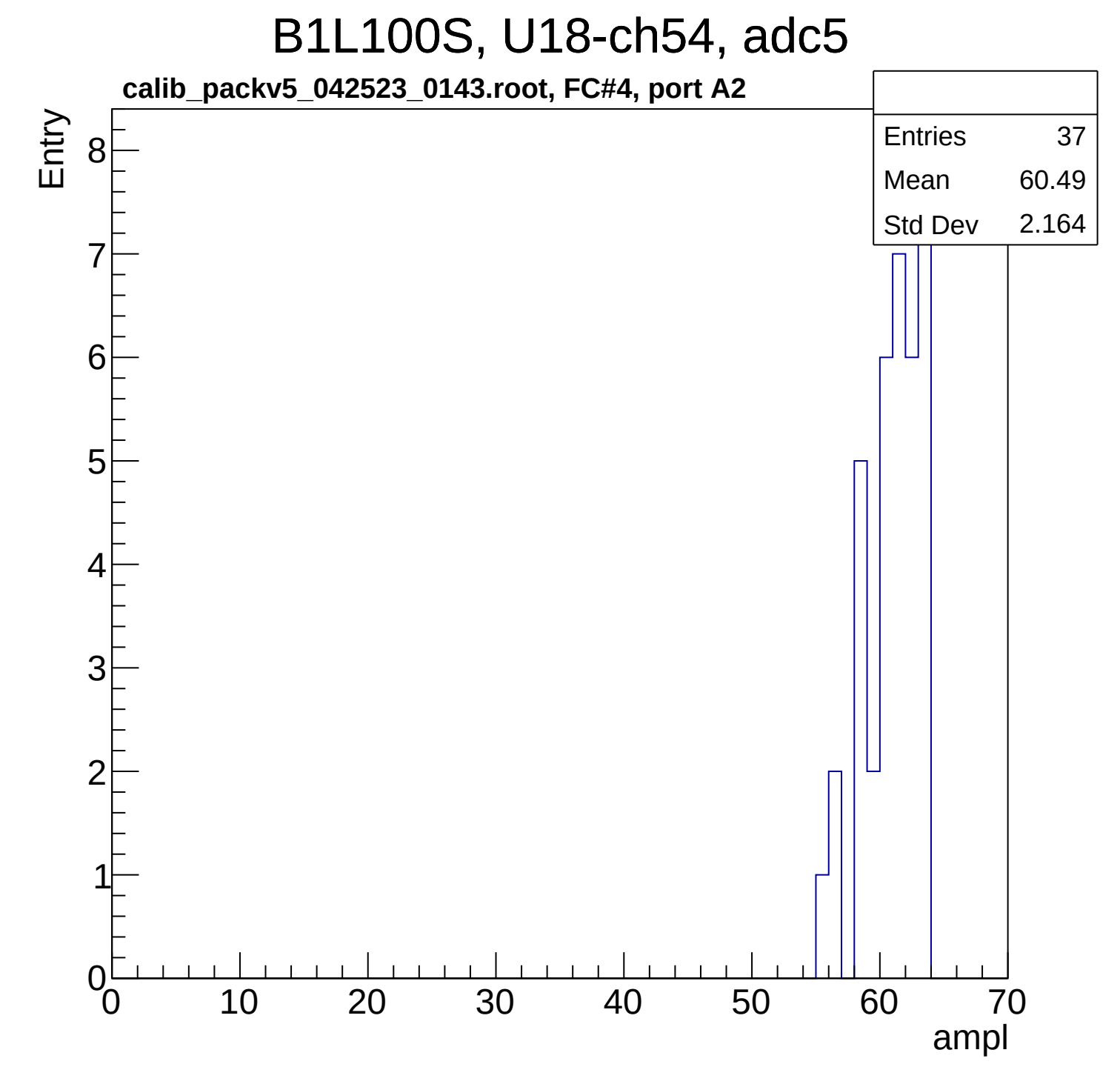

B1L100S, U18-ch54, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 29.79
Std Dev 3.436
Gaus mean : 30.4601
Gaus Width: 3.7007
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

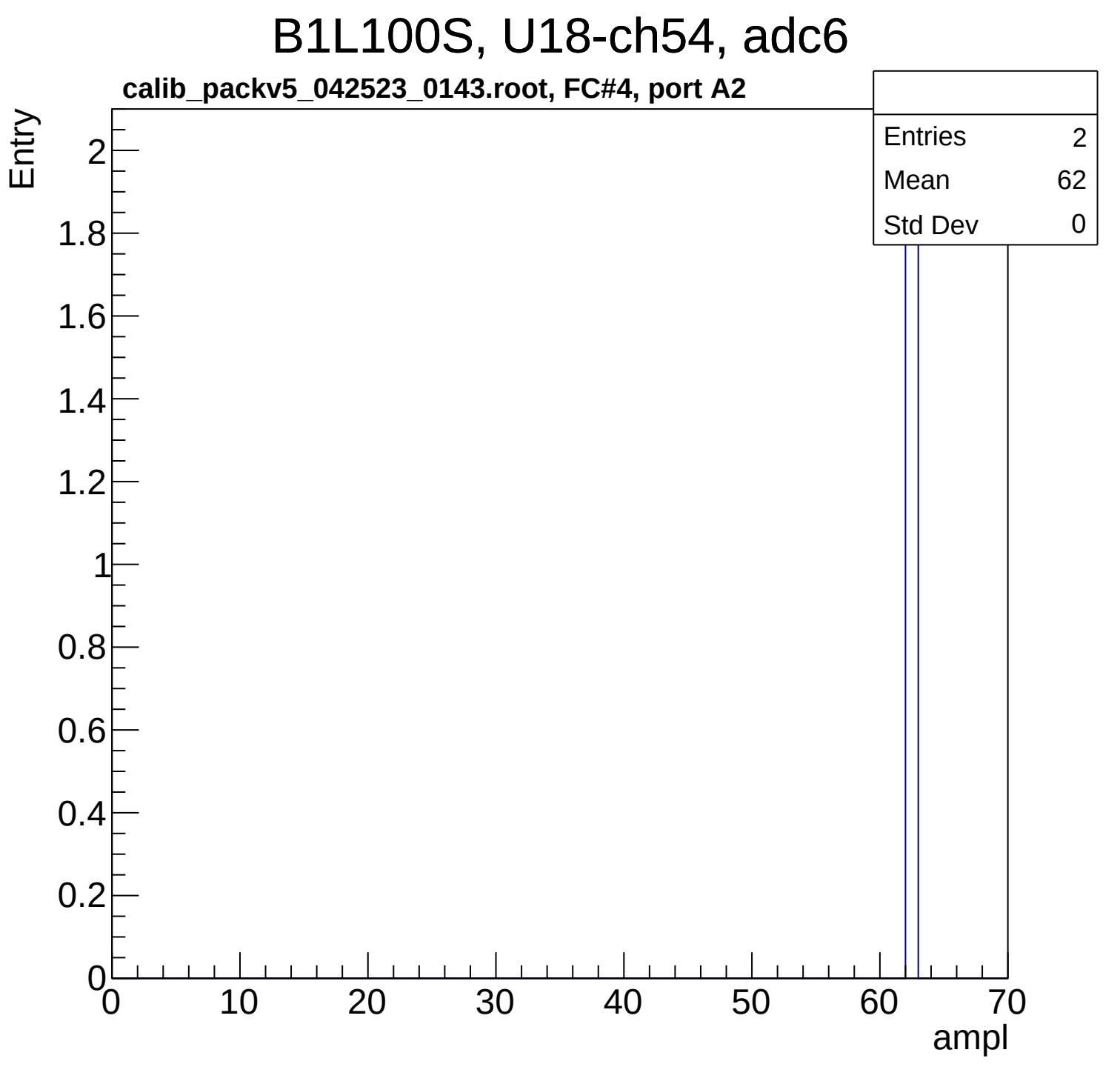

B1L100S, U18-ch54, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 36.51
Std Dev 3.549
Gaus mean : 36.6718
Gaus Width: 3.2514
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

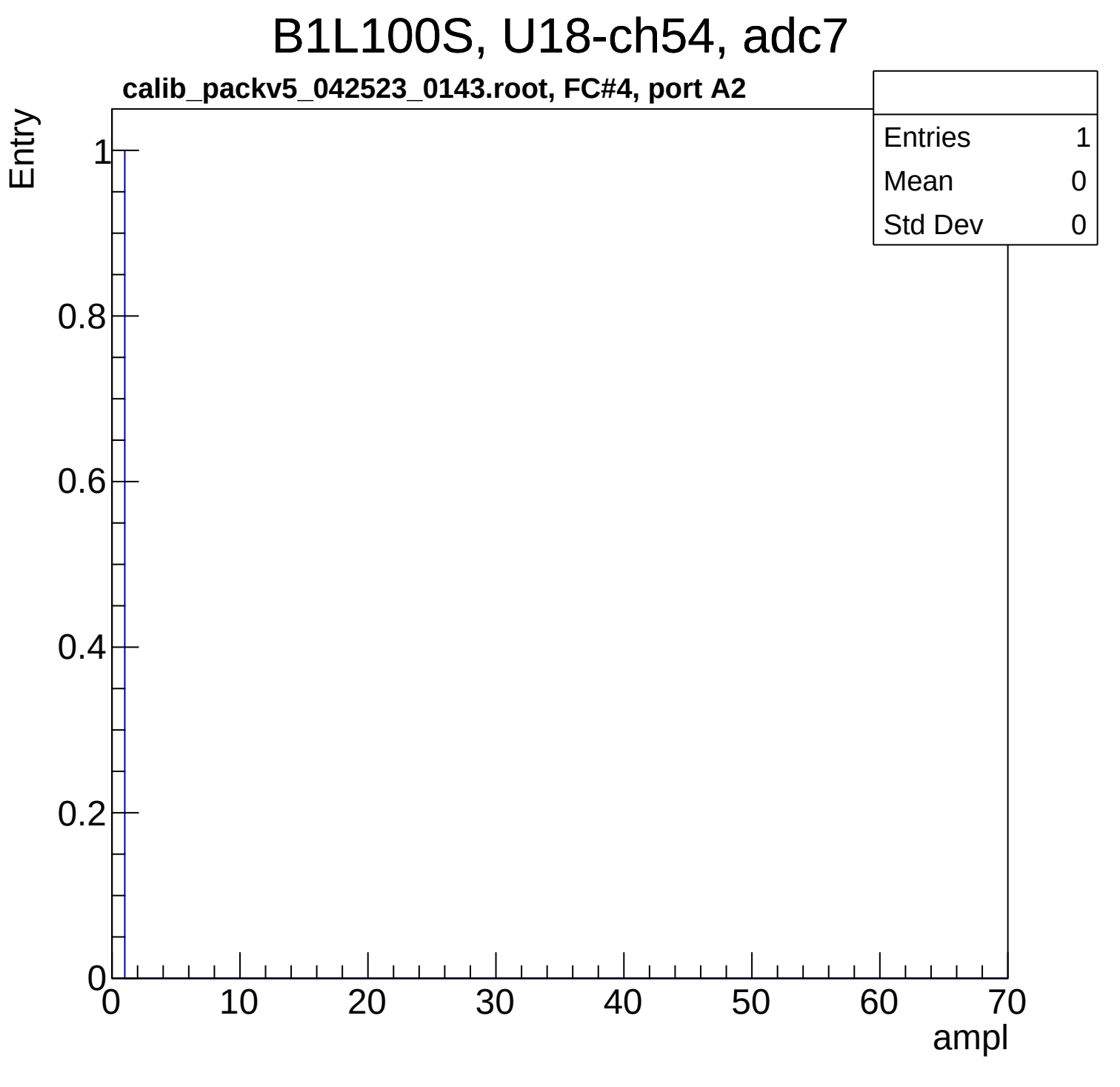

B1L100S, U18-ch54, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 44.05
Std Dev 3.561
Gaus mean : 44.3879
Gaus Width: 3.5969
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

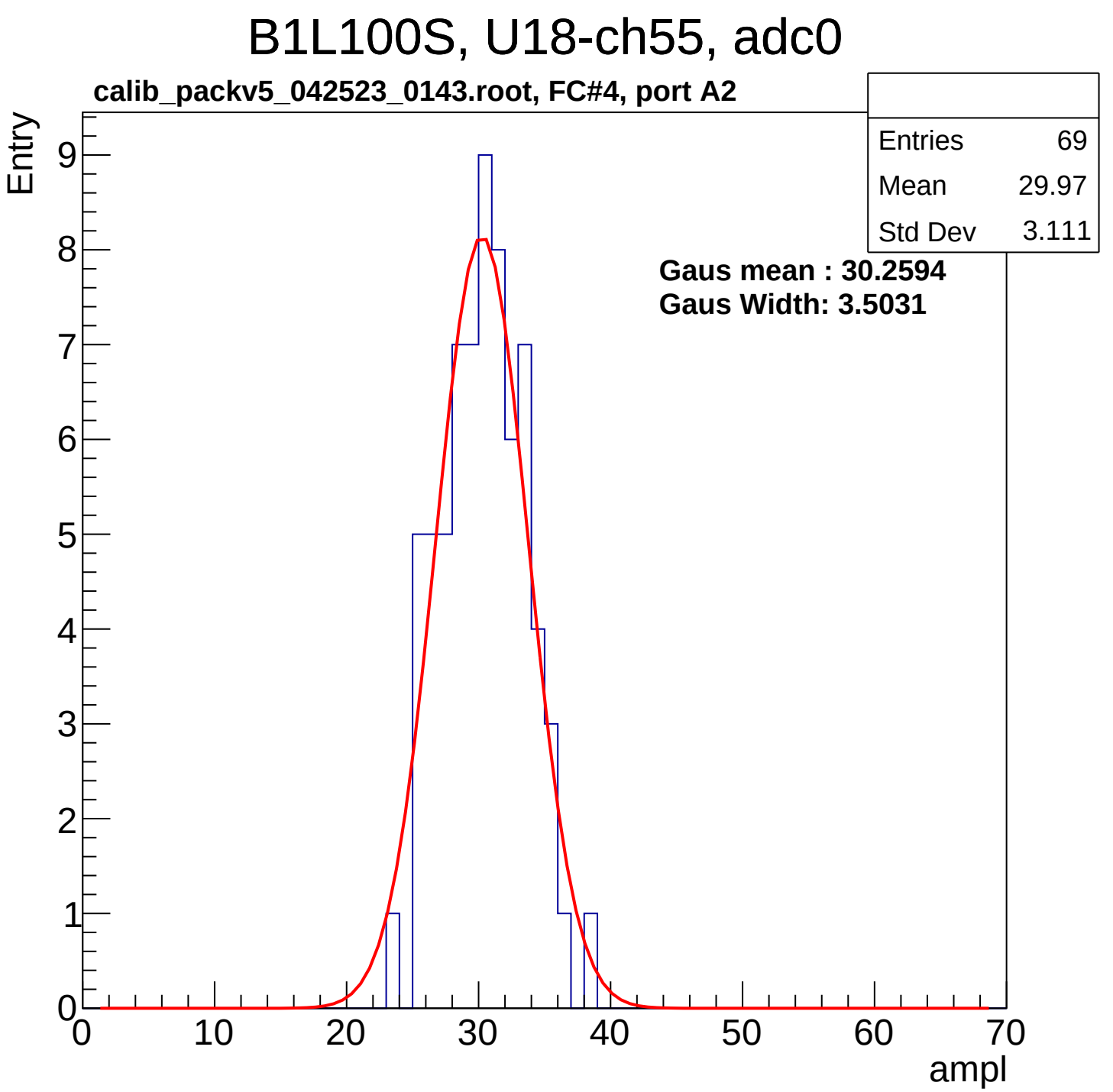

B1L100S, U18-ch54, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 49.63
Std Dev 3.705
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

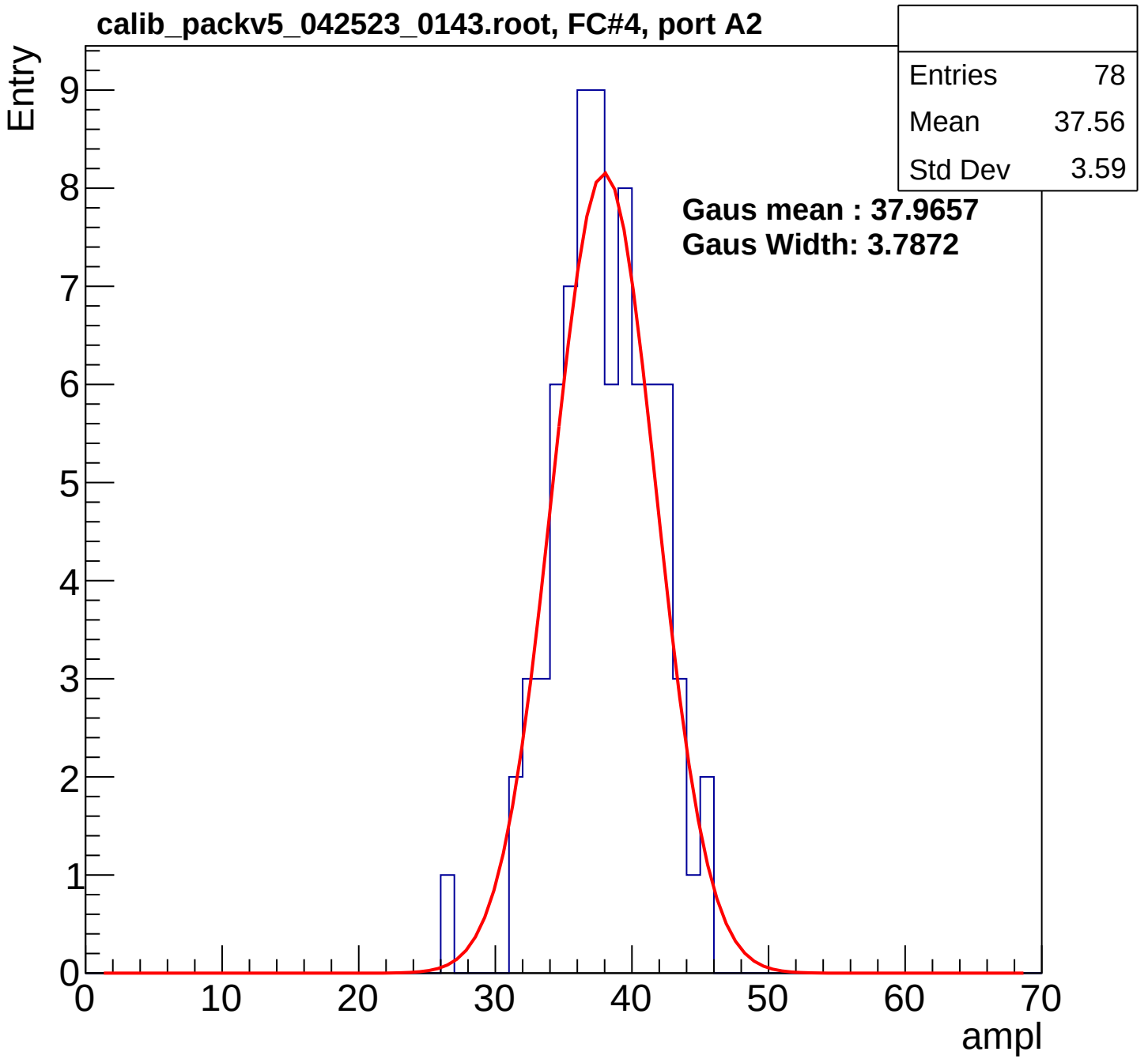

B1L100S, U18-ch54, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 55.42
Std Dev 7.656
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

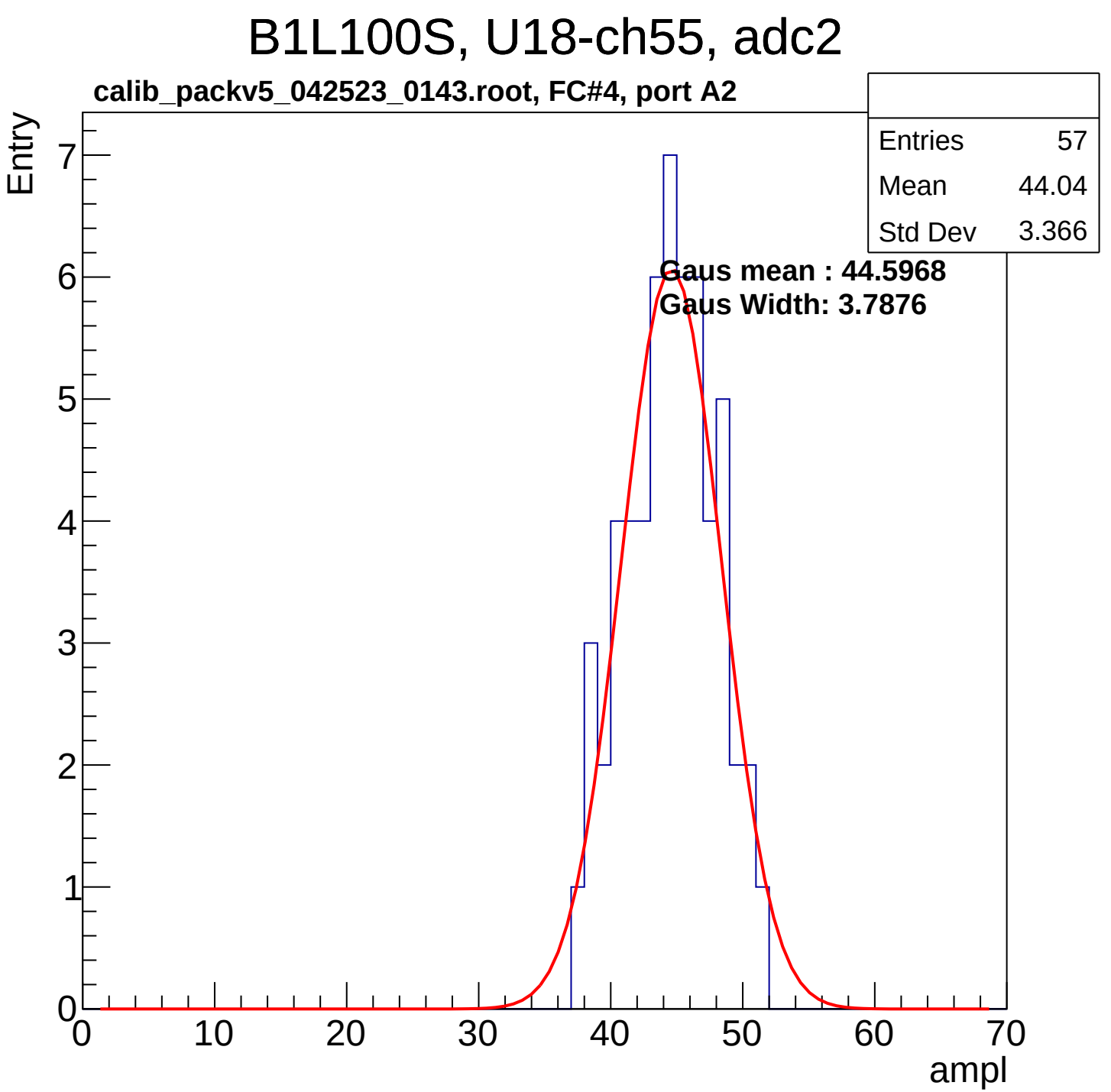

B1L100S, U18-ch54, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 37
Mean 60.49
Std Dev 2.164
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

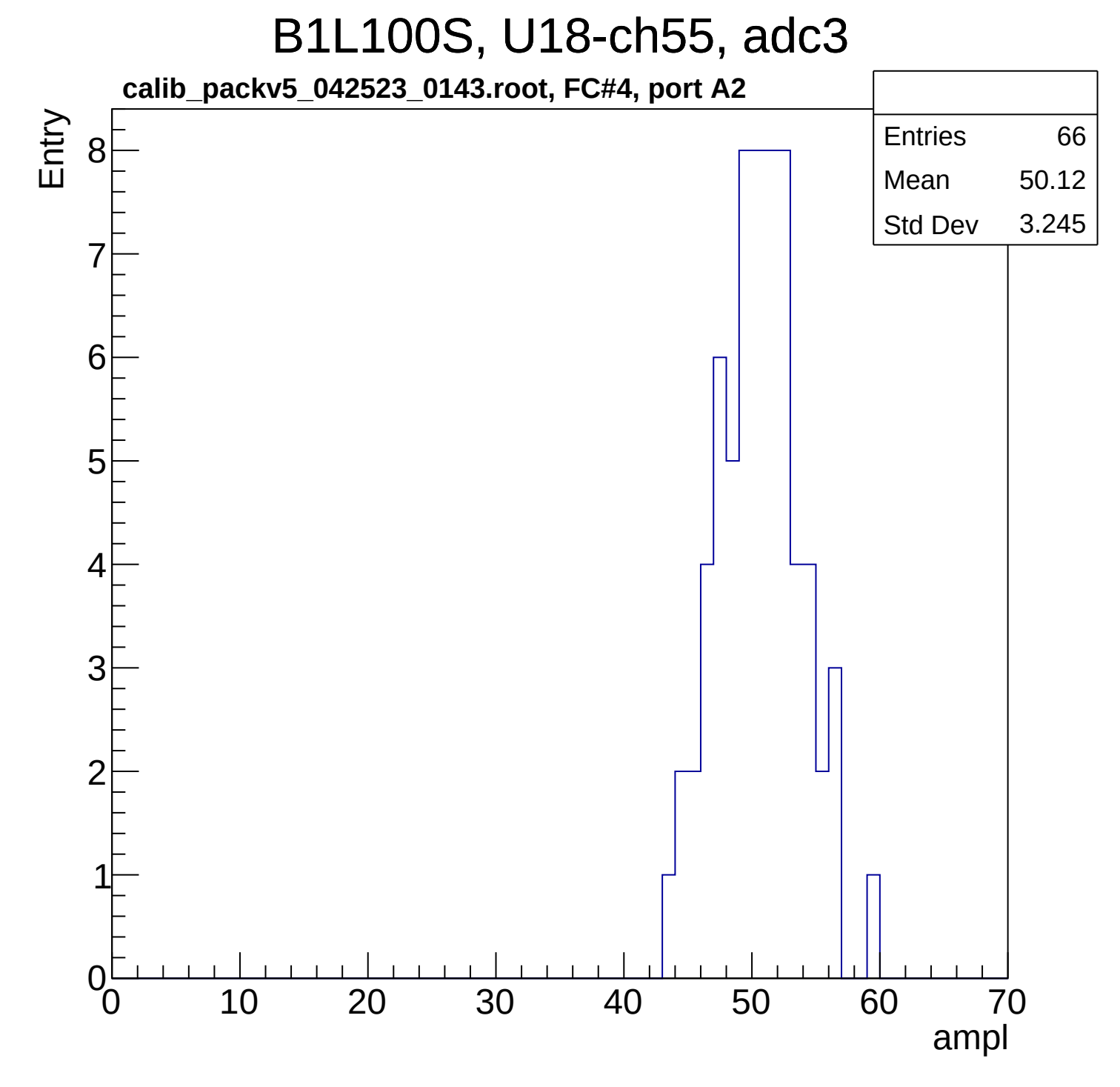

B1L100S, U18-ch54, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 62
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

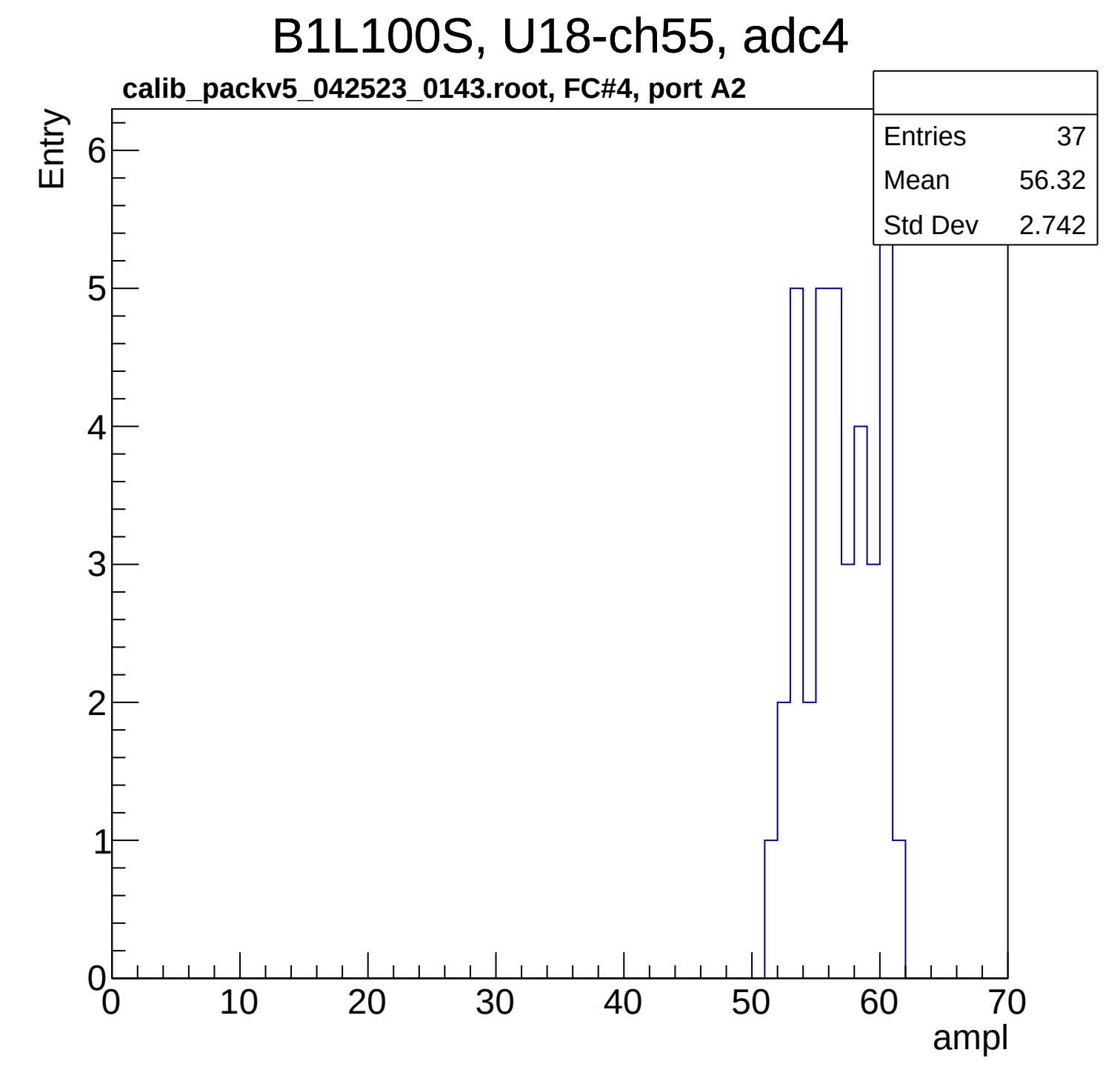

B1L100S, U18-ch54, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

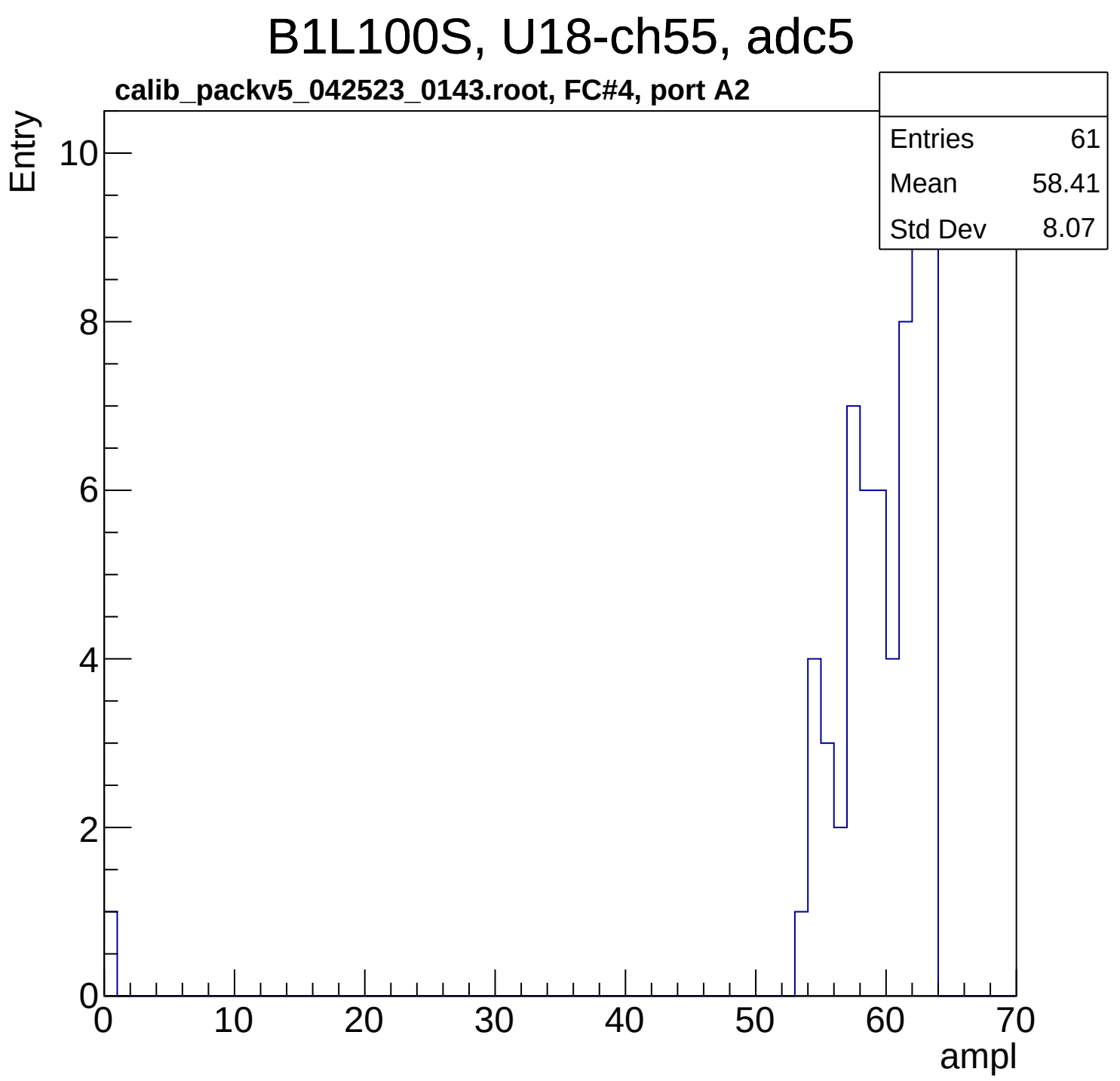

B1L100S, U18-ch55, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 29.97
Std Dev 3.111
Gaus mean : 30.2594
Gaus Width: 3.5031
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

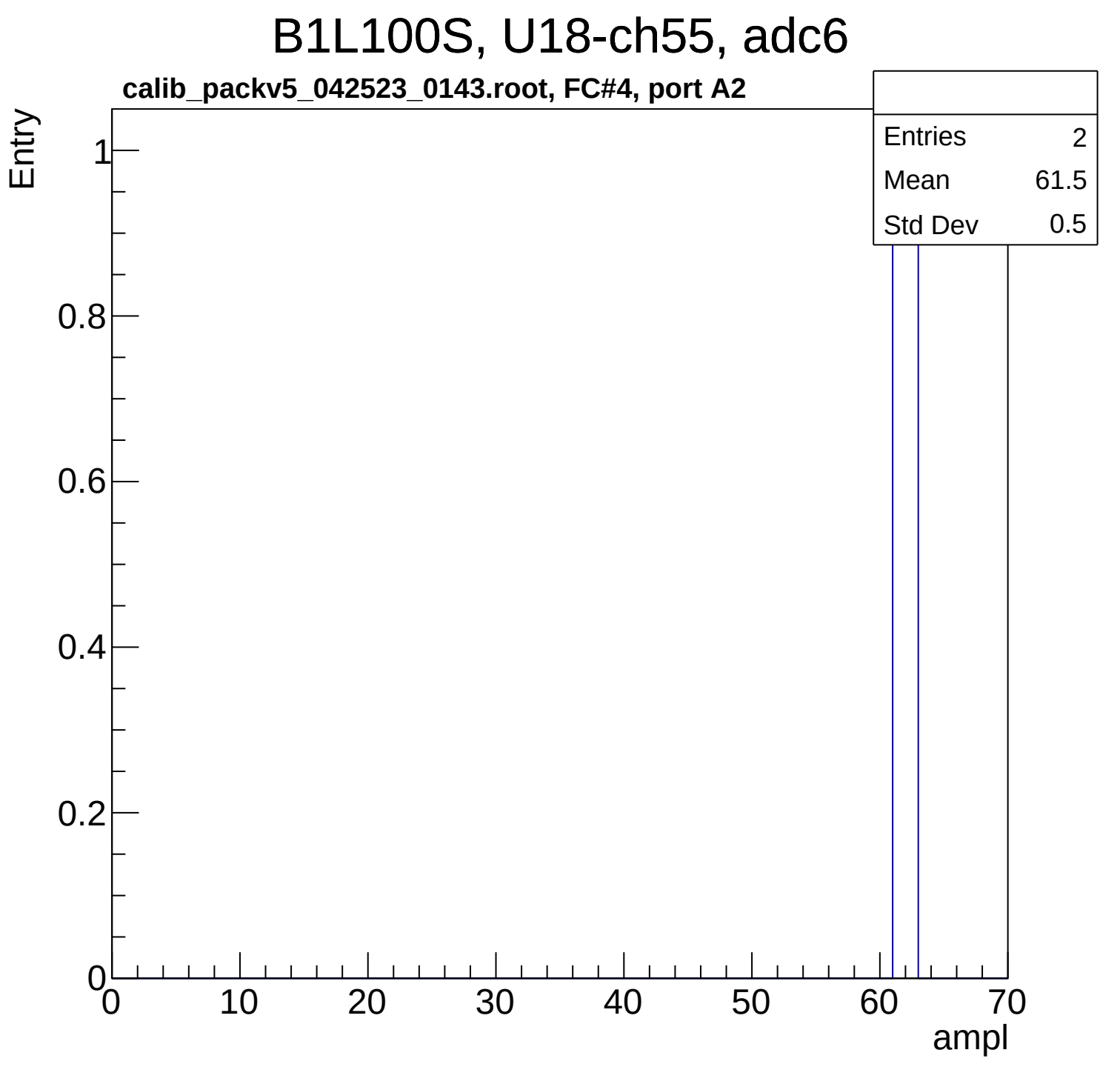

B1L100S, U18-ch55, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 37.56
Std Dev 3.59
Gaus mean : 37.9657
Gaus Width: 3.7872
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

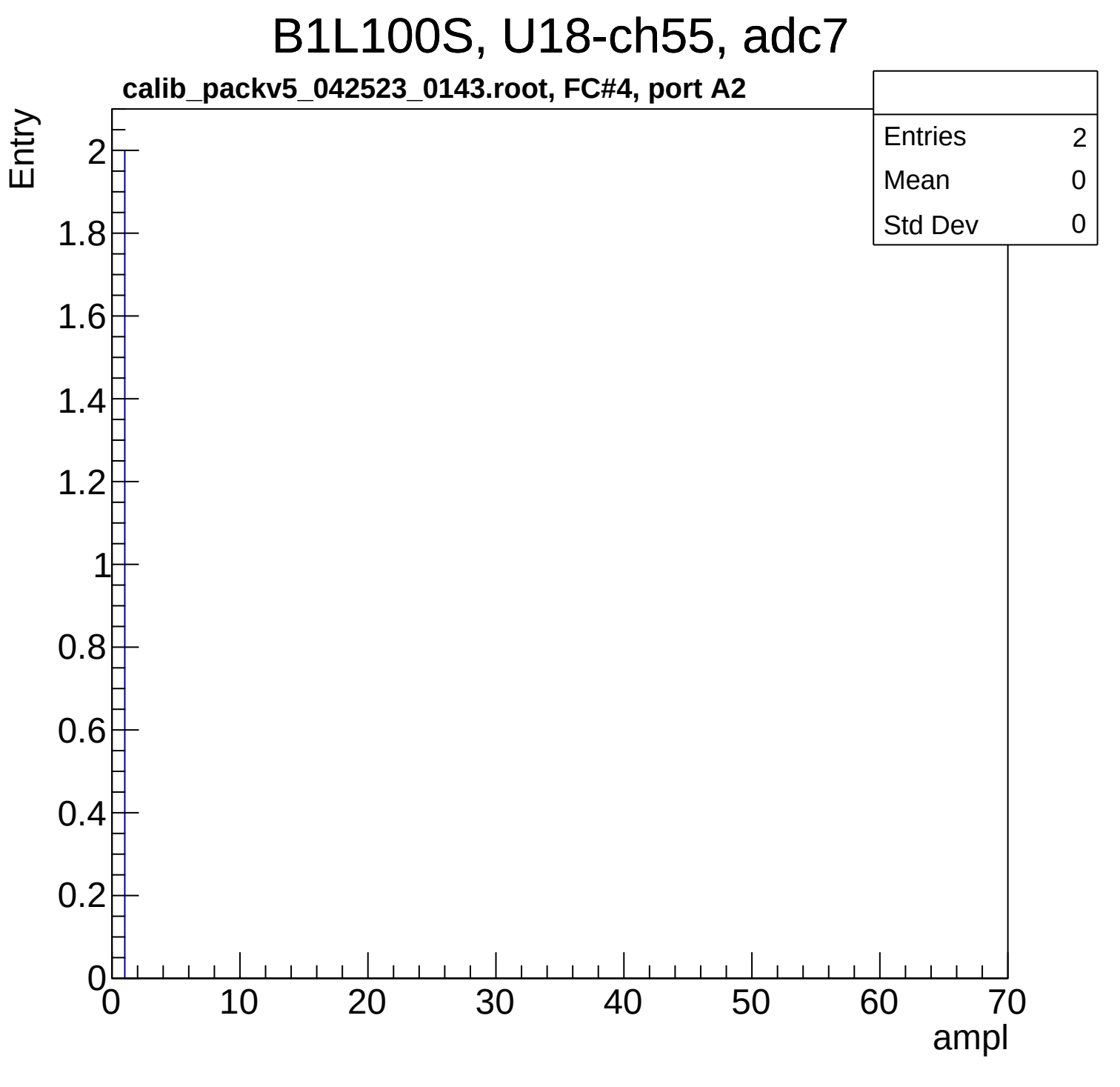

B1L100S, U18-ch55, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 44.04
Std Dev 3.366
Gaus mean : 44.5968
Gaus Width: 3.7876
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

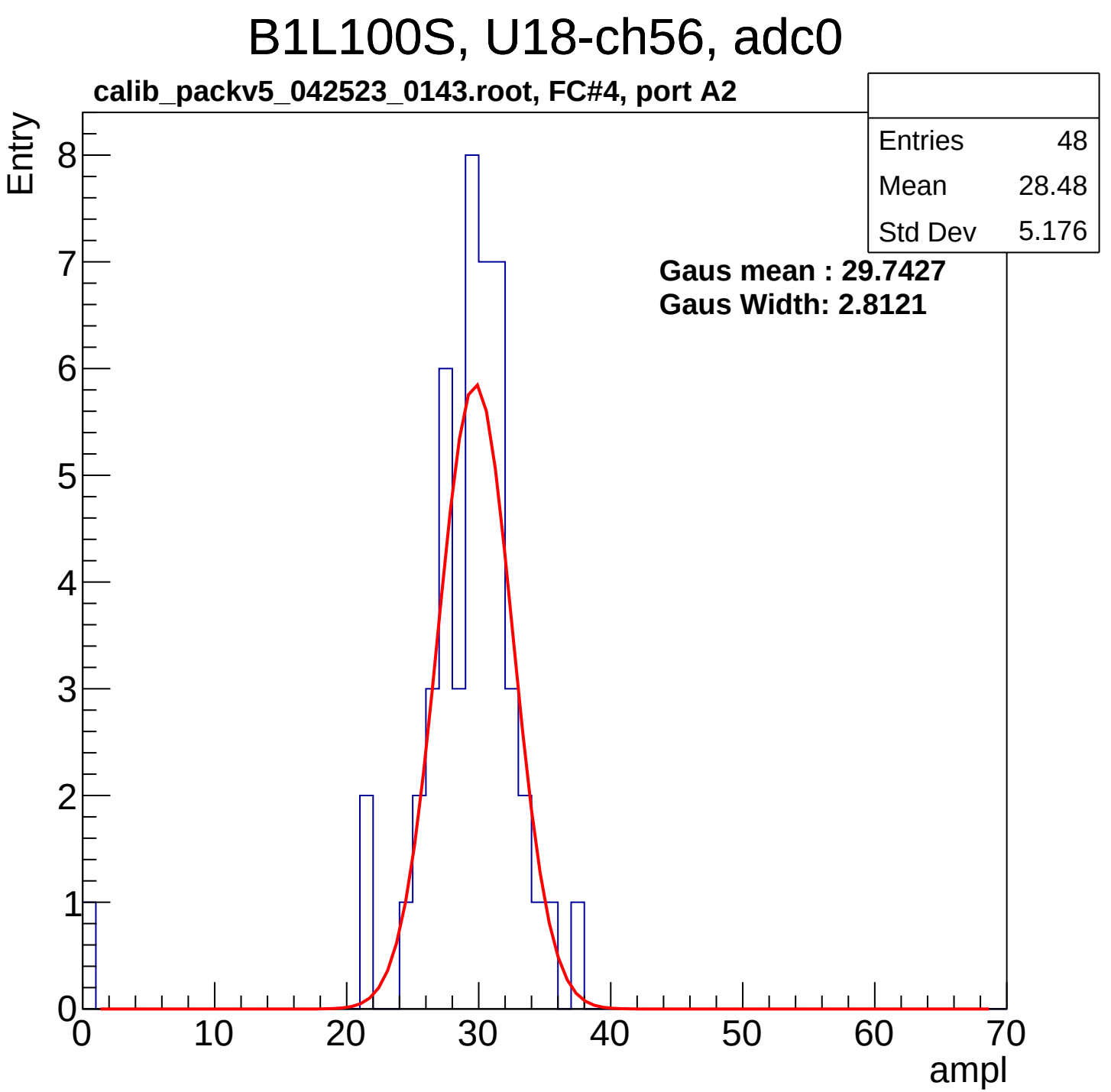

B1L100S, U18-ch55, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 50.12
Std Dev 3.245
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

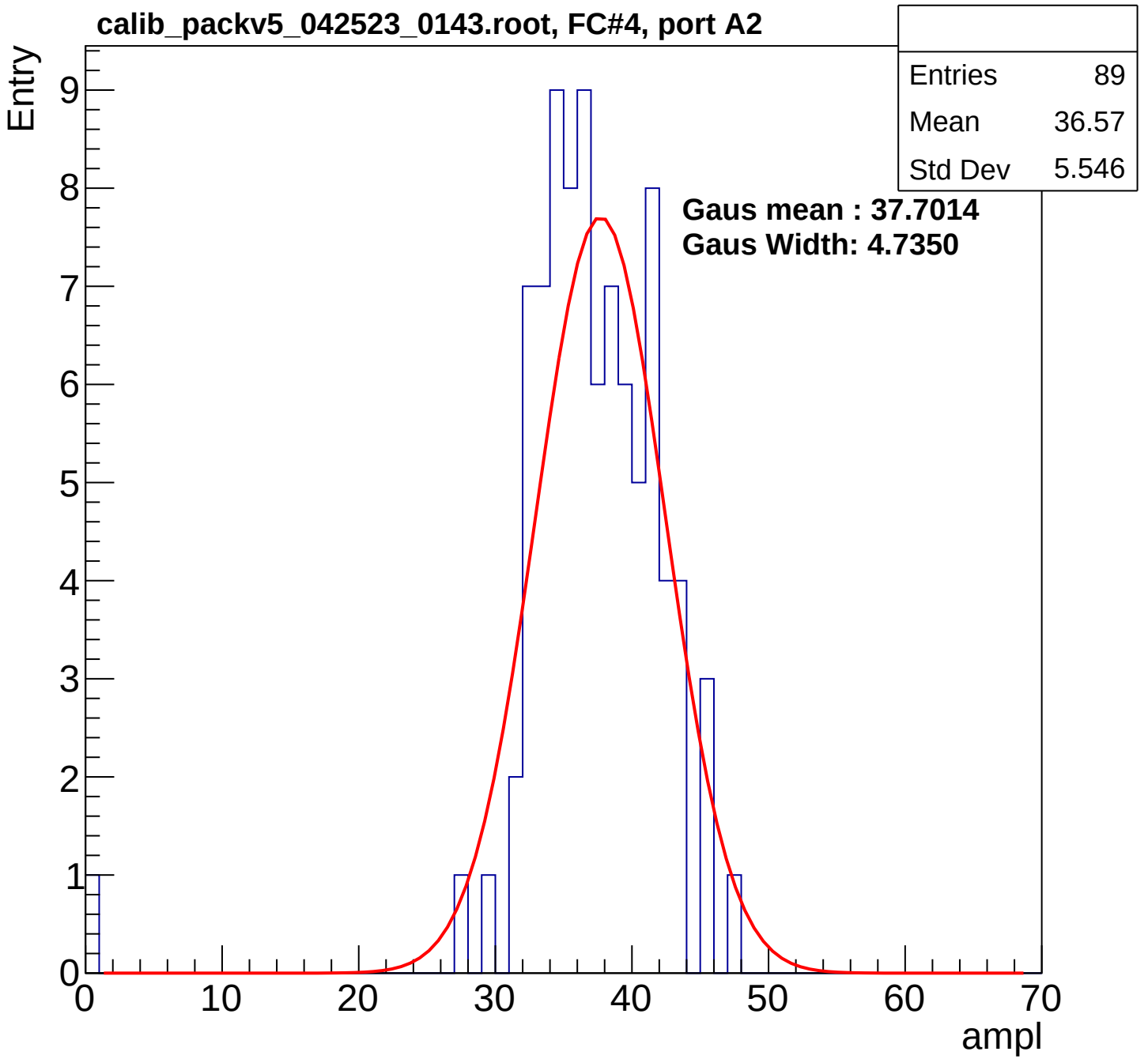

B1L100S, U18-ch55, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 37
Mean 56.32
Std Dev 2.742
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

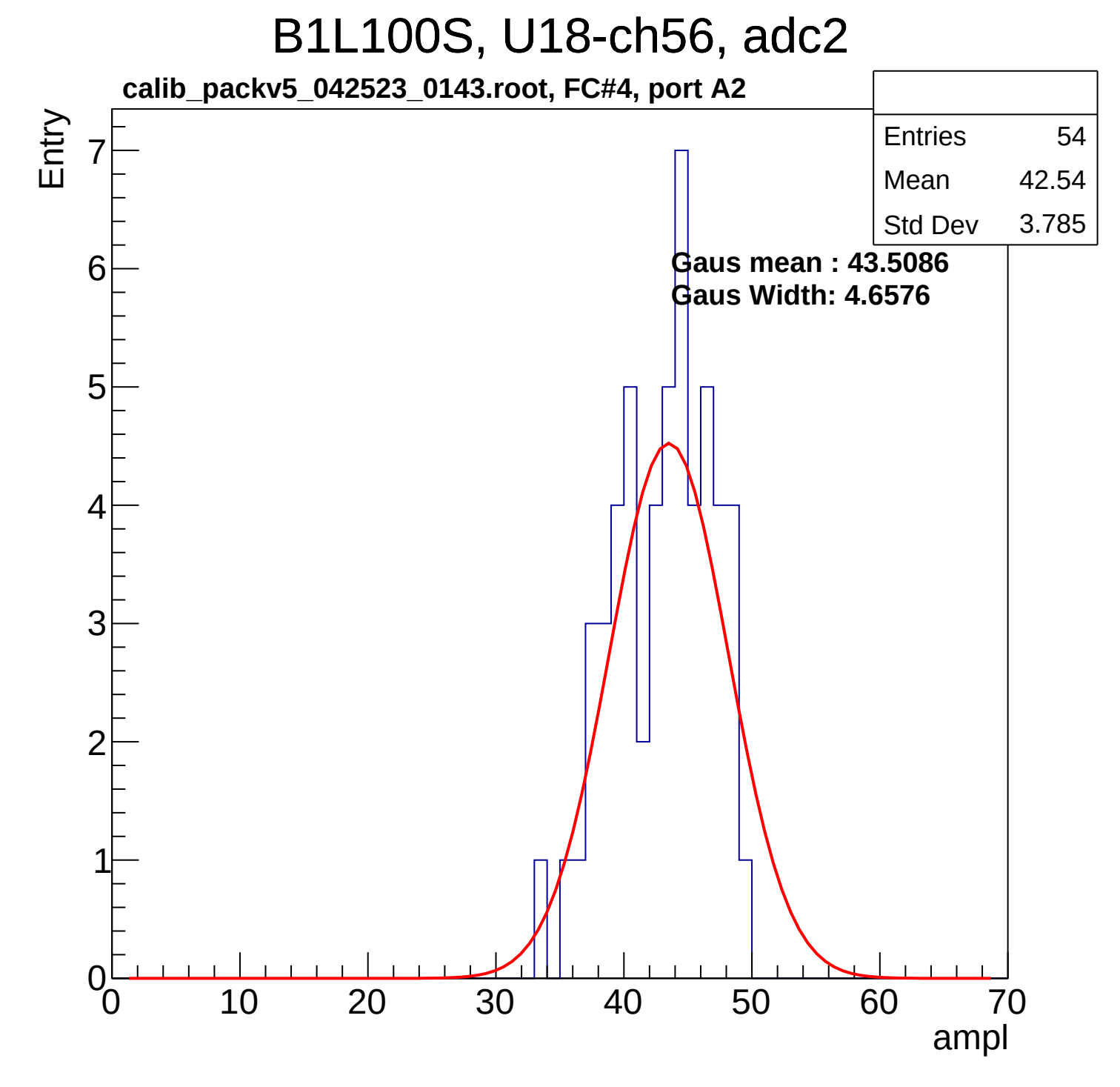

B1L100S, U18-ch55, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 58.41
Std Dev 8.07
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

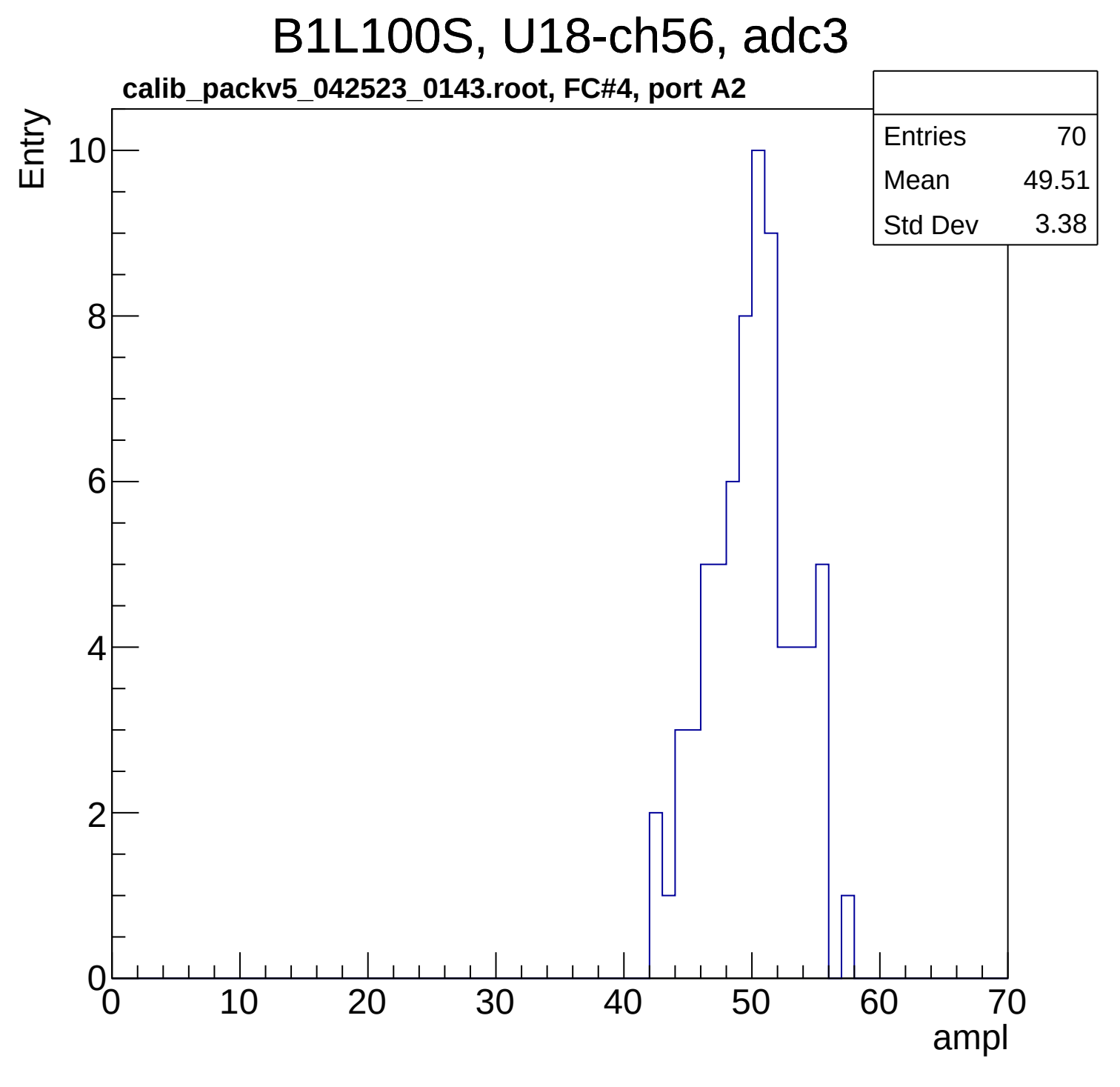

B1L100S, U18-ch55, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 61.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

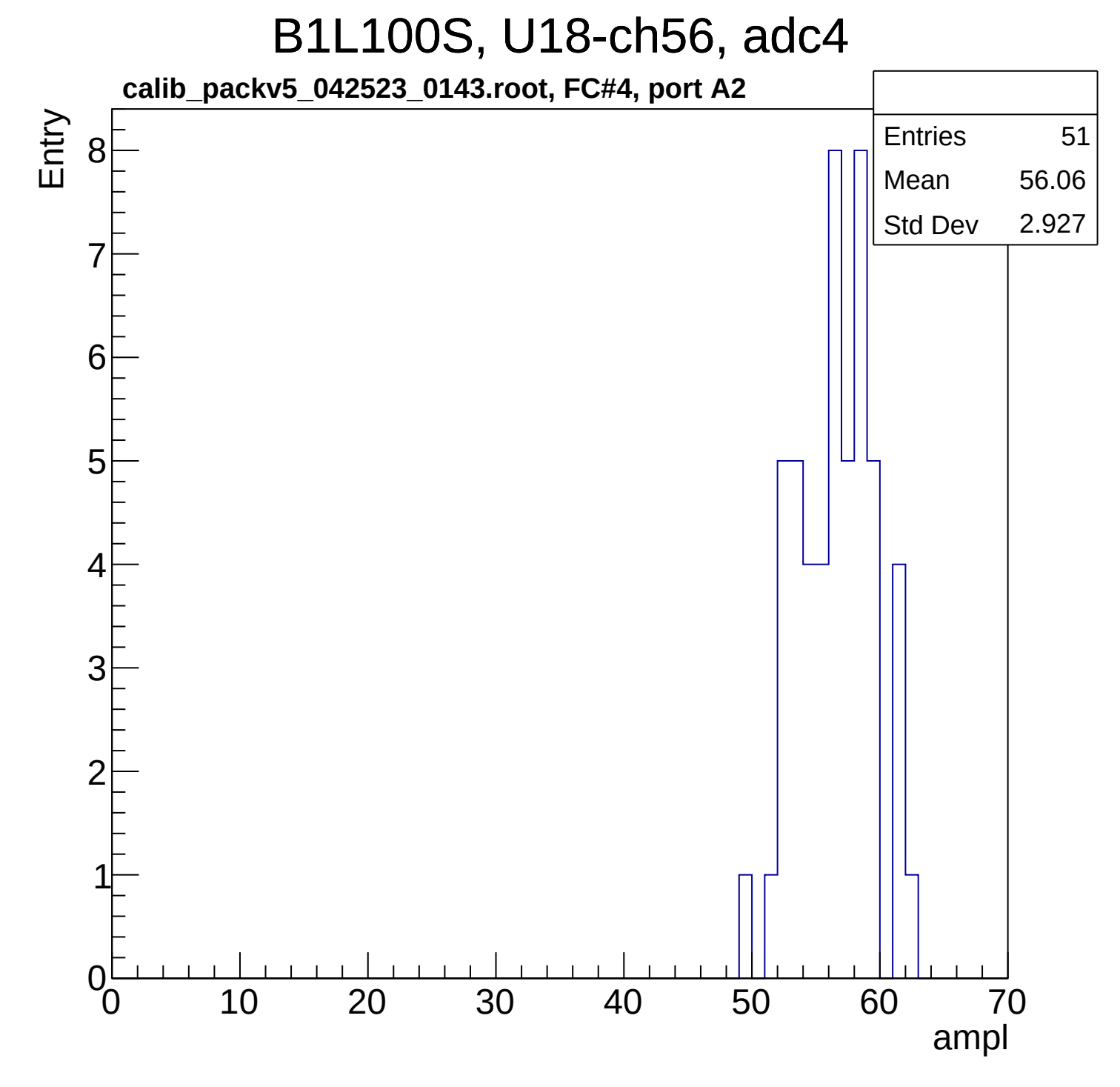

B1L100S, U18-ch55, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

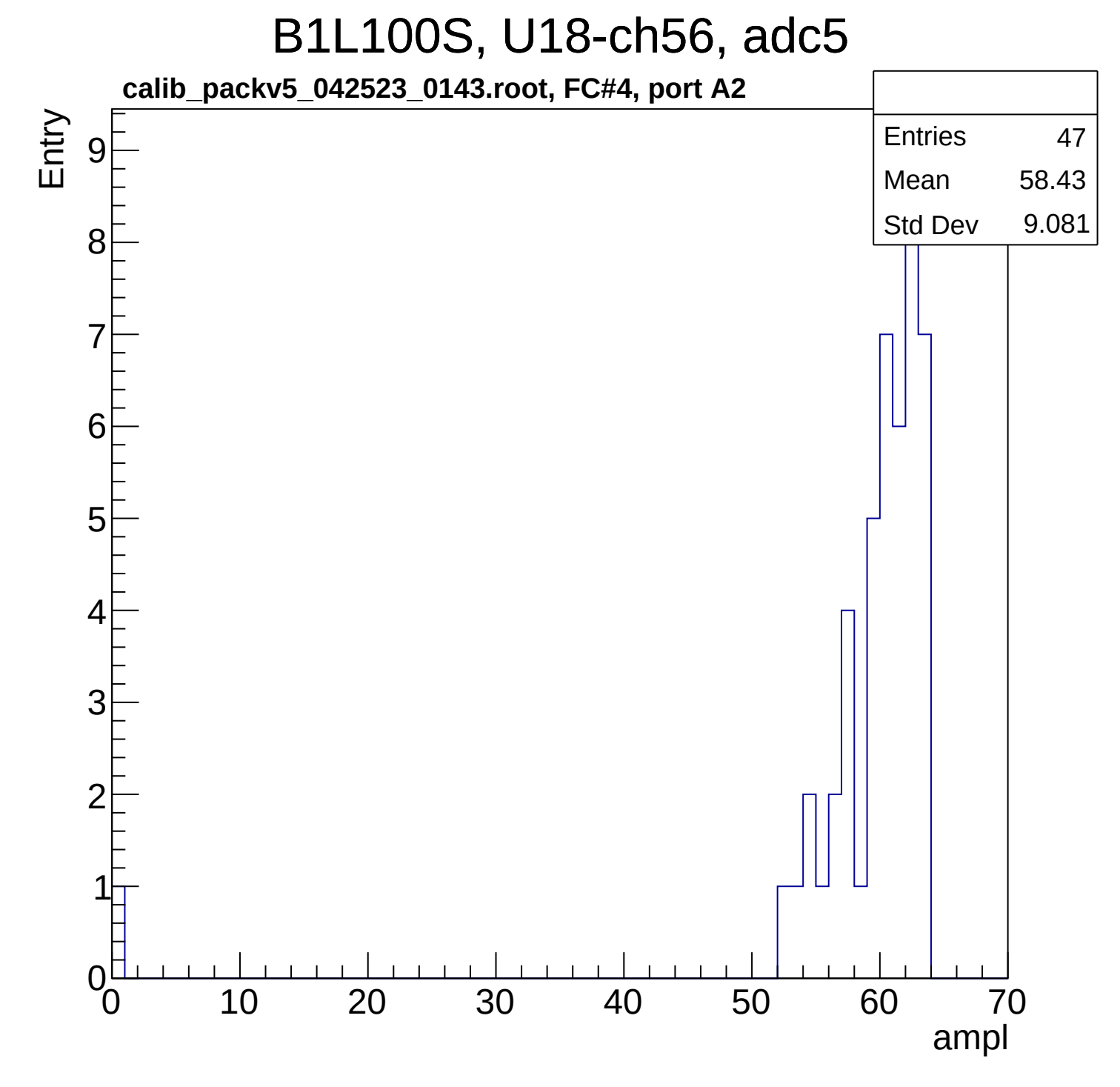

B1L100S, U18-ch56, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 28.48
Std Dev 5.176
Gaus mean : 29.7427
Gaus Width: 2.8121
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

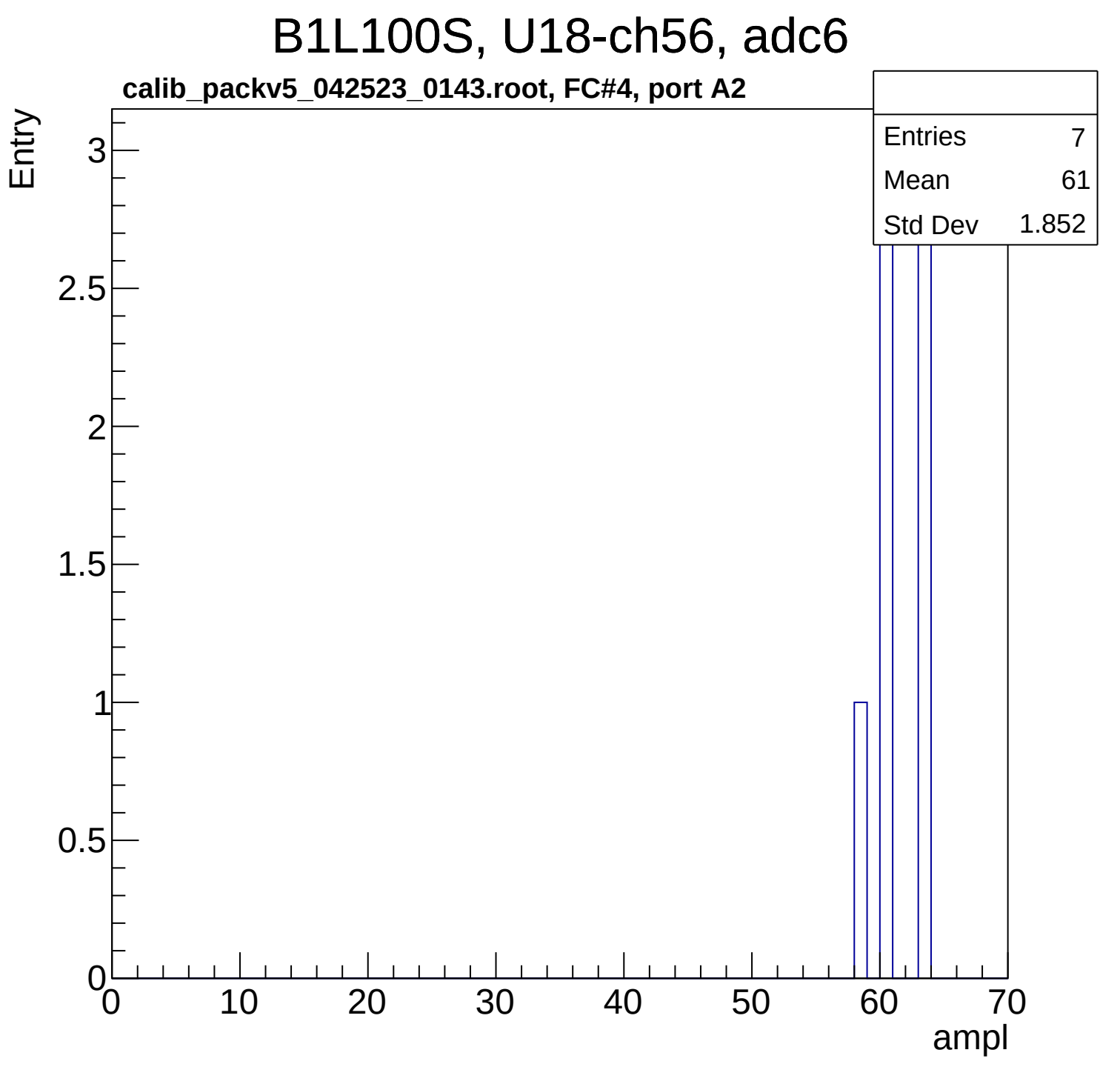

B1L100S, U18-ch56, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 89
Mean 36.57
Std Dev 5.546
Gaus mean : 37.7014
Gaus Width: 4.7350
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

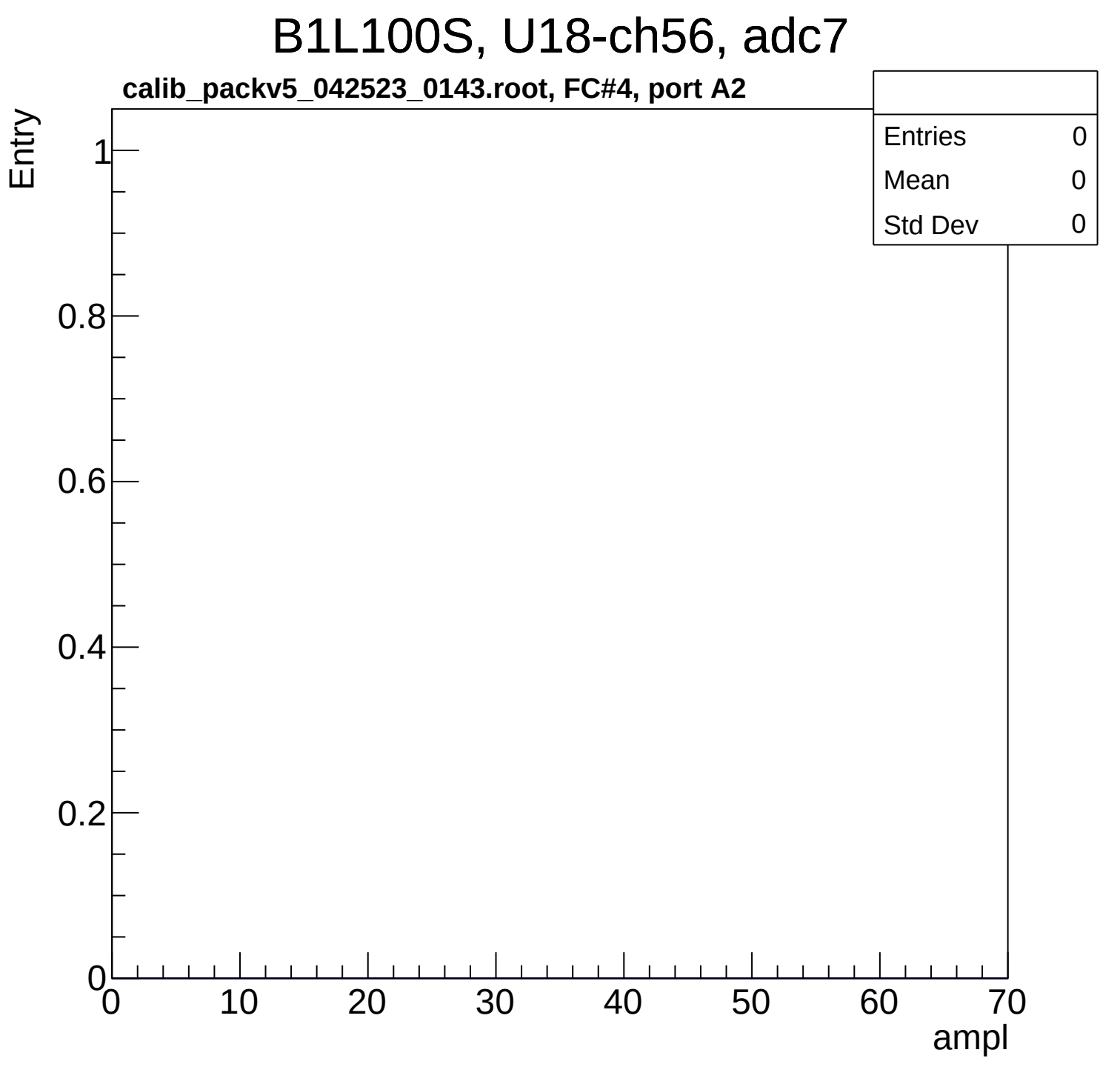

B1L100S, U18-ch56, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 42.54
Std Dev 3.785
Gaus mean : 43.5086
Gaus Width: 4.6576
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

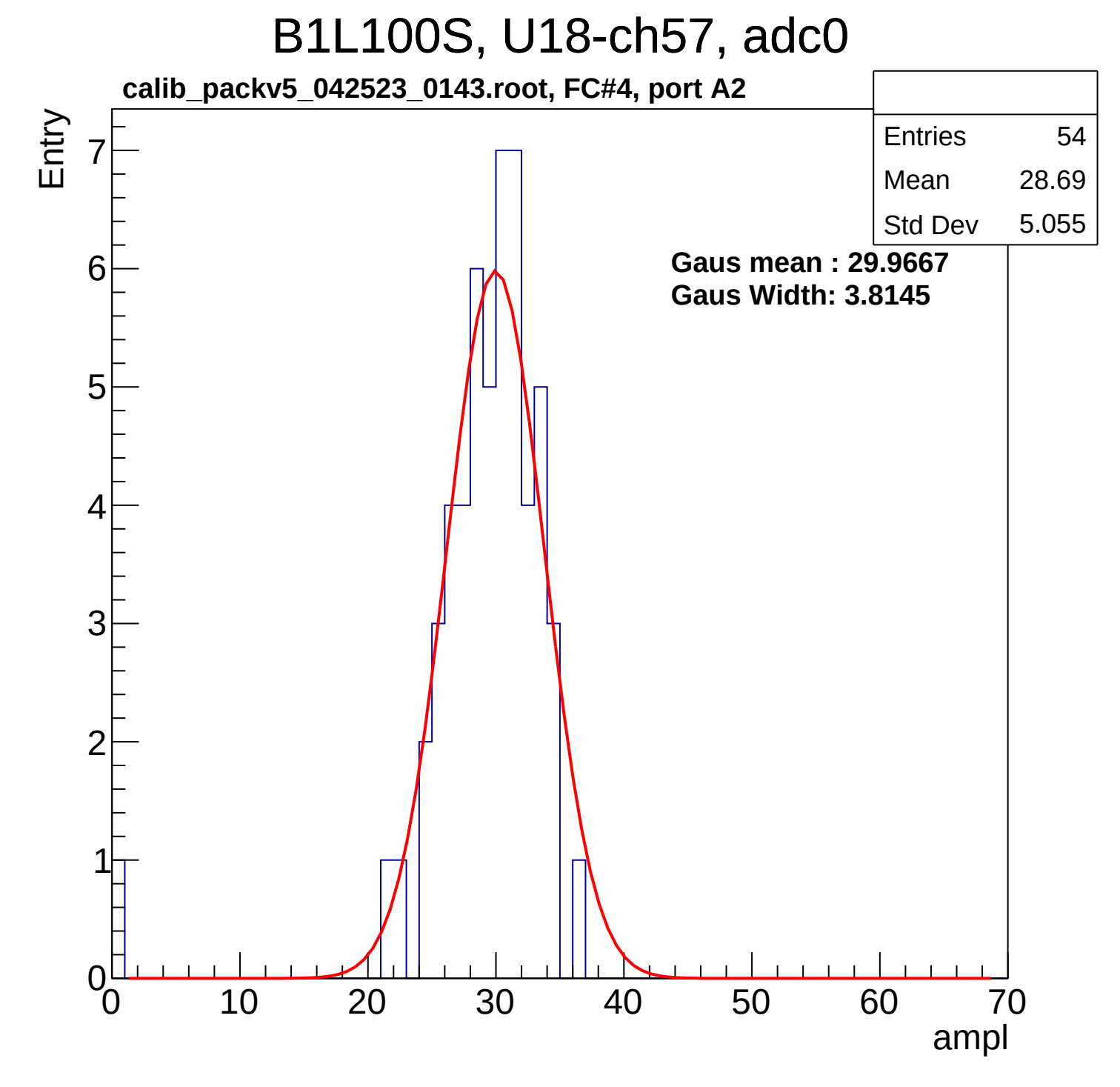

B1L100S, U18-ch56, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 49.51
Std Dev 3.38
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

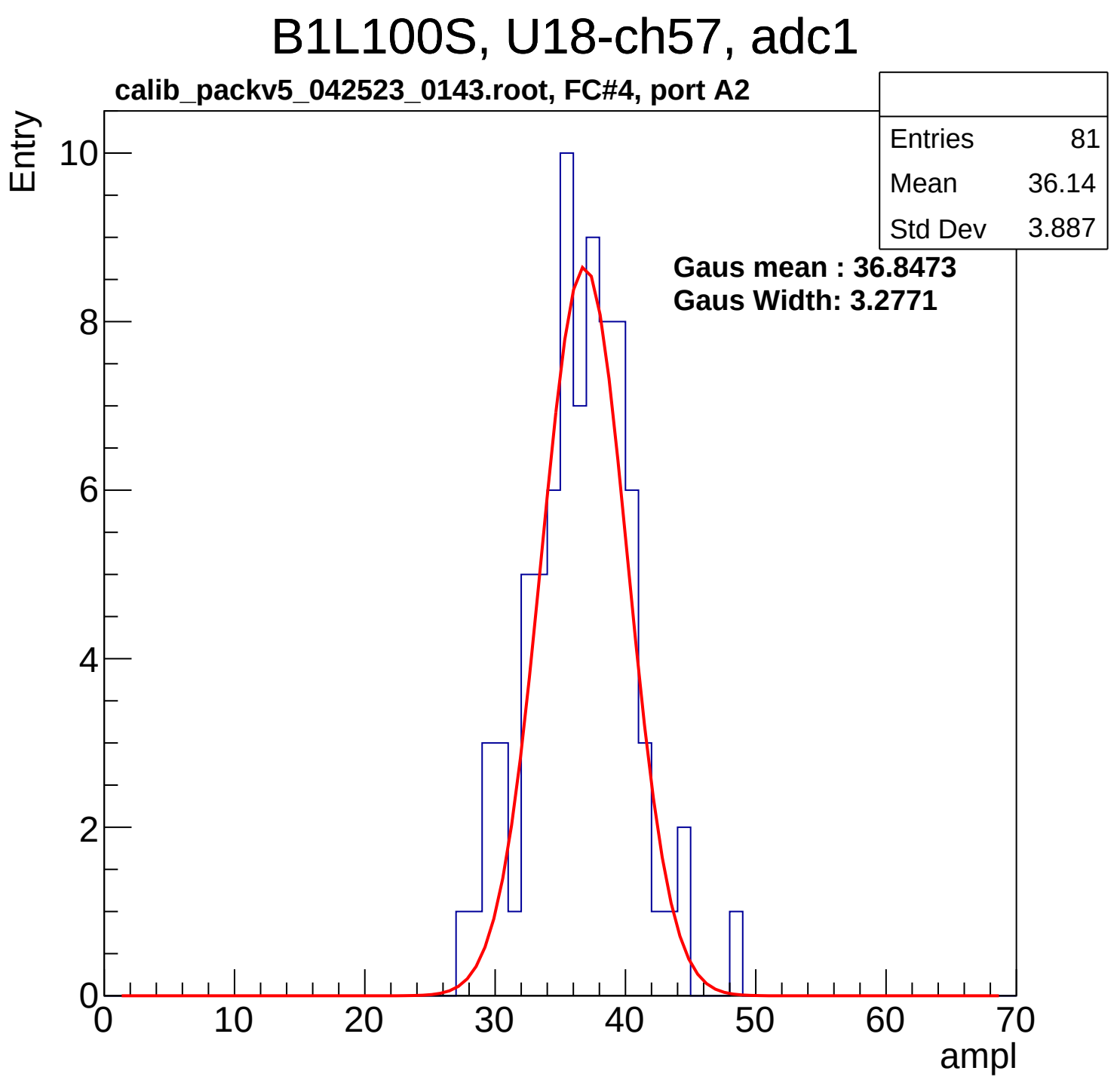

B1L100S, U18-ch56, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 56.06
Std Dev 2.927
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

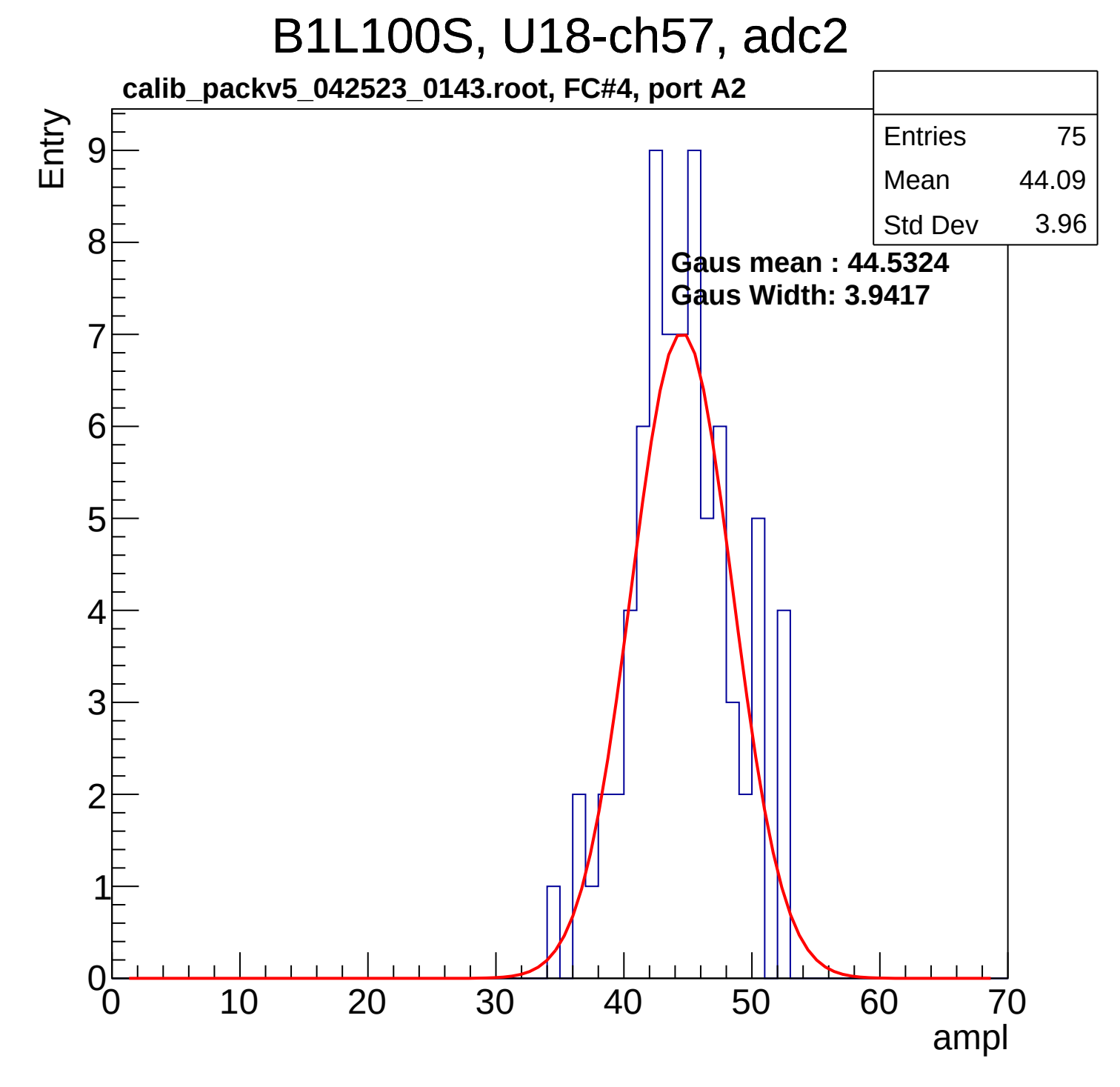

B1L100S, U18-ch56, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 58.43
Std Dev 9.081
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

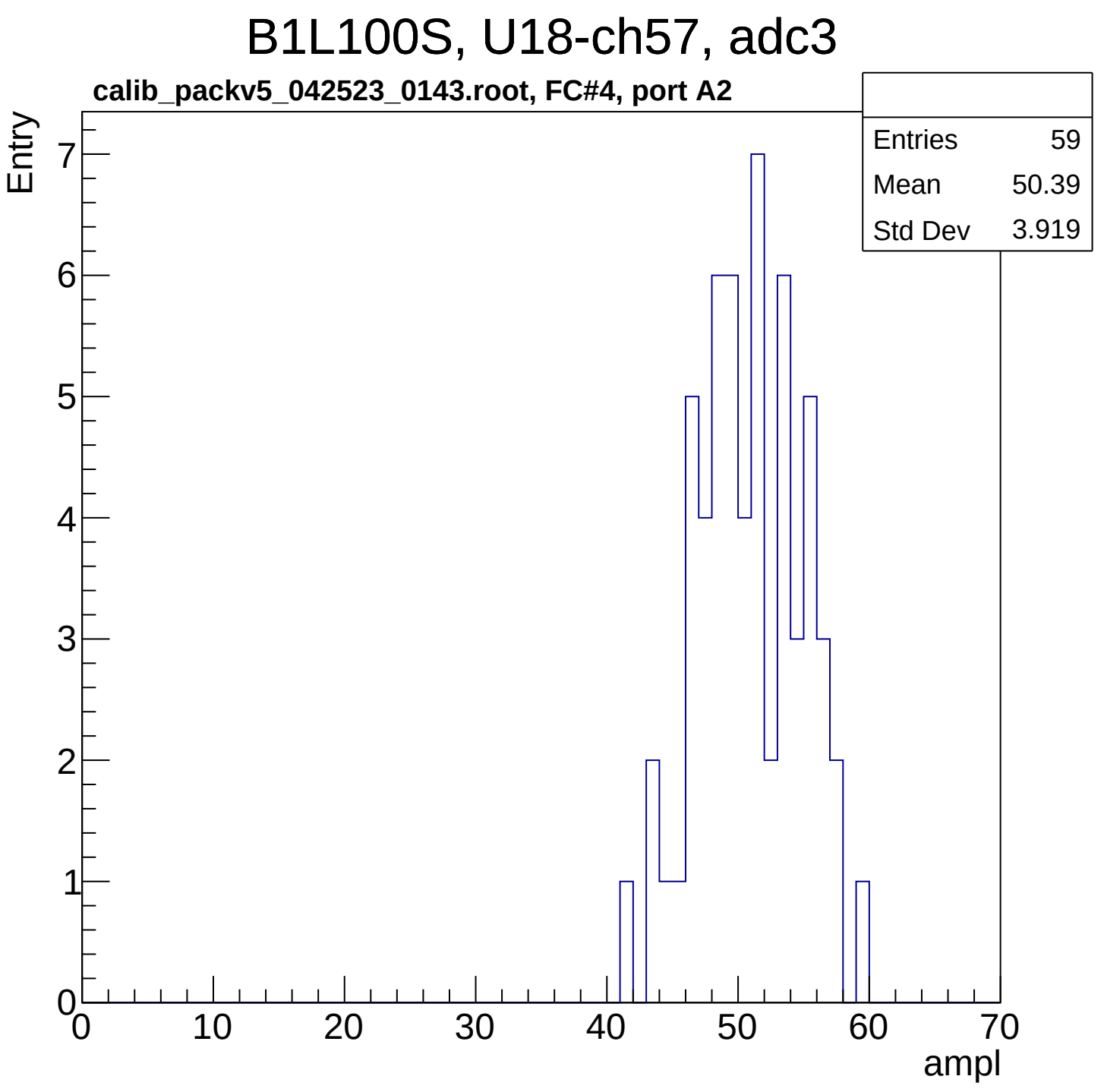

B1L100S, U18-ch56, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 61
Std Dev 1.852
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

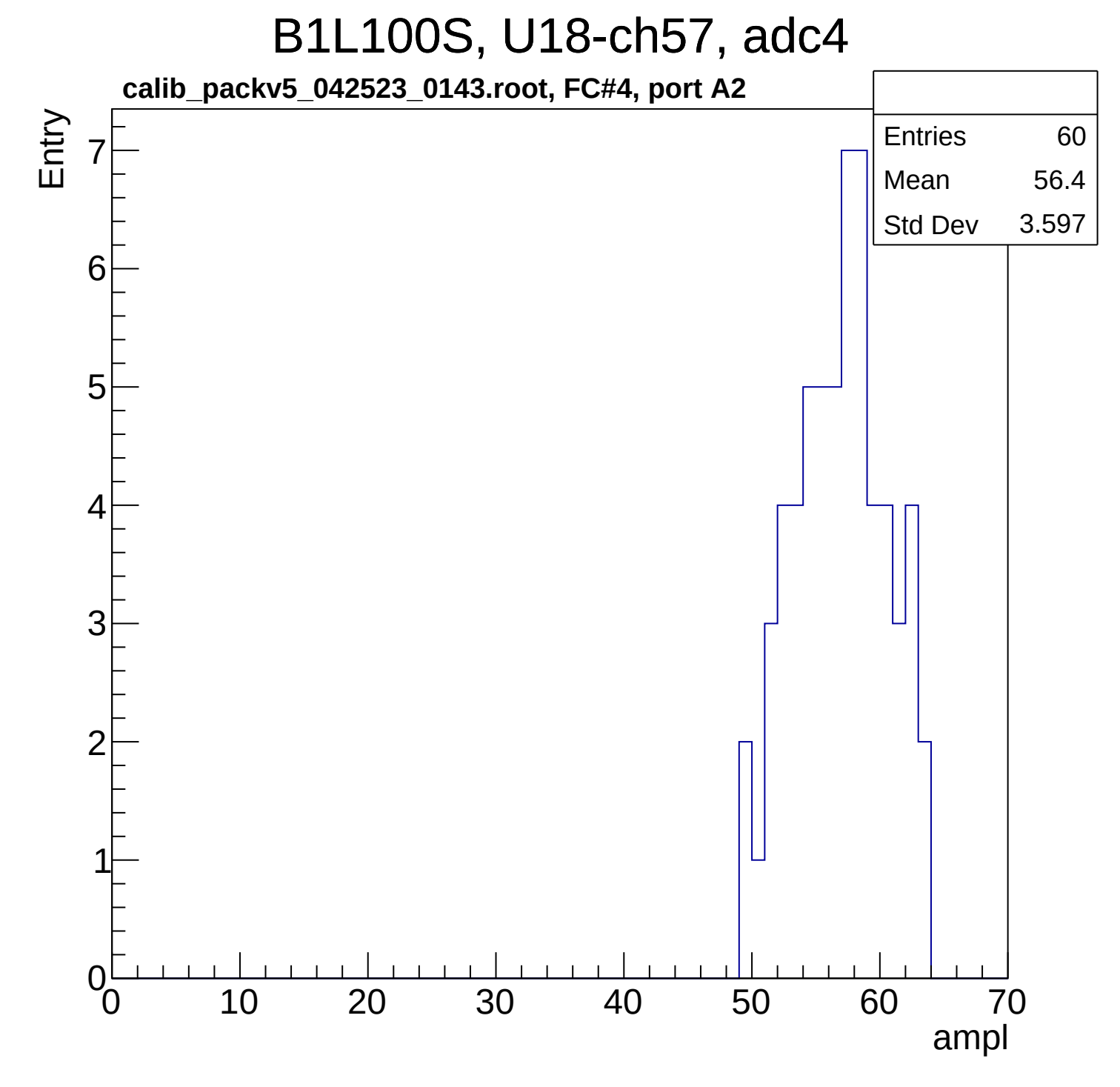

B1L100S, U18-ch56, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

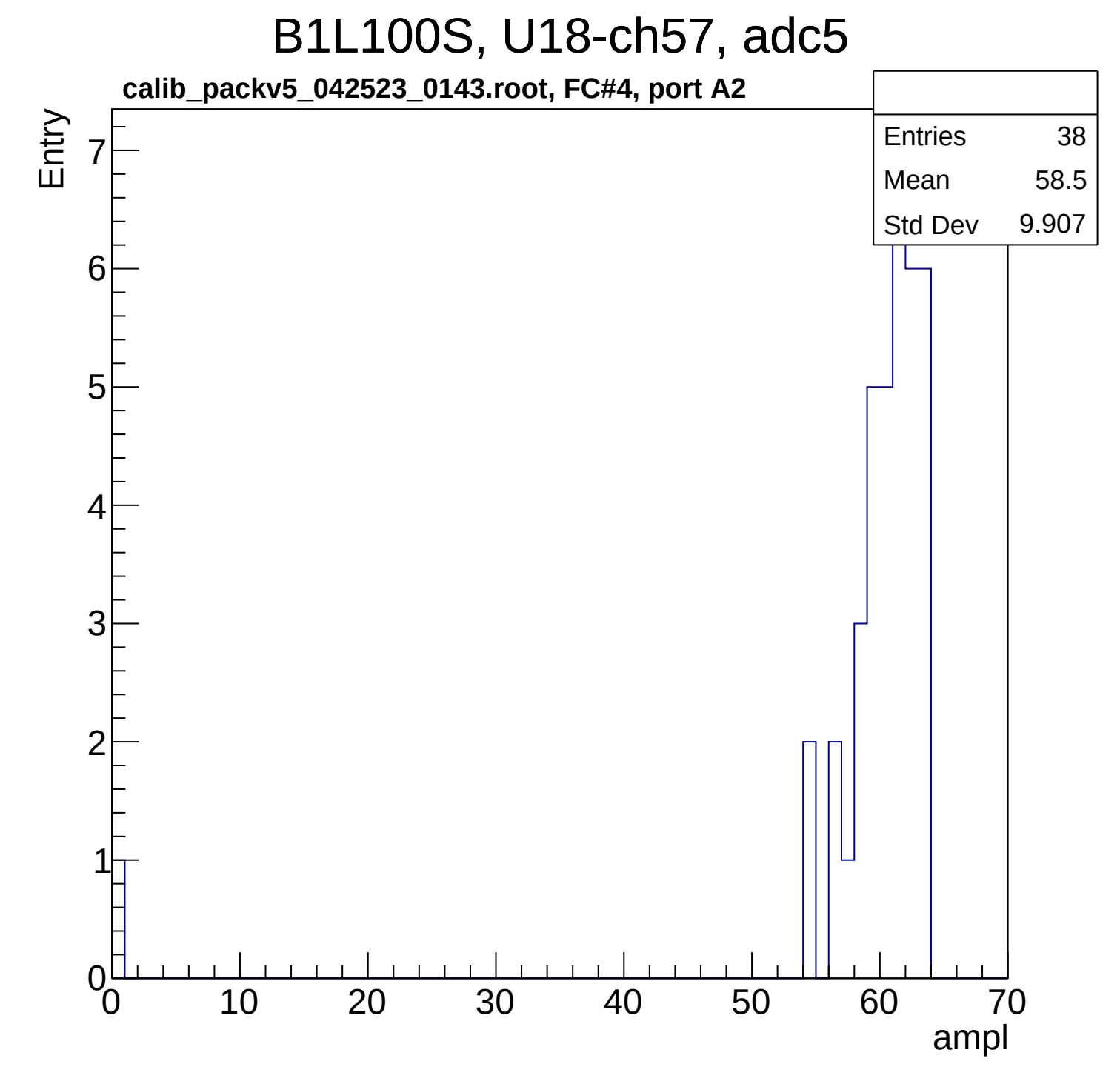

B1L100S, U18-ch57, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 28.69
Std Dev 5.055
Gaus mean : 29.9667
Gaus Width: 3.8145
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

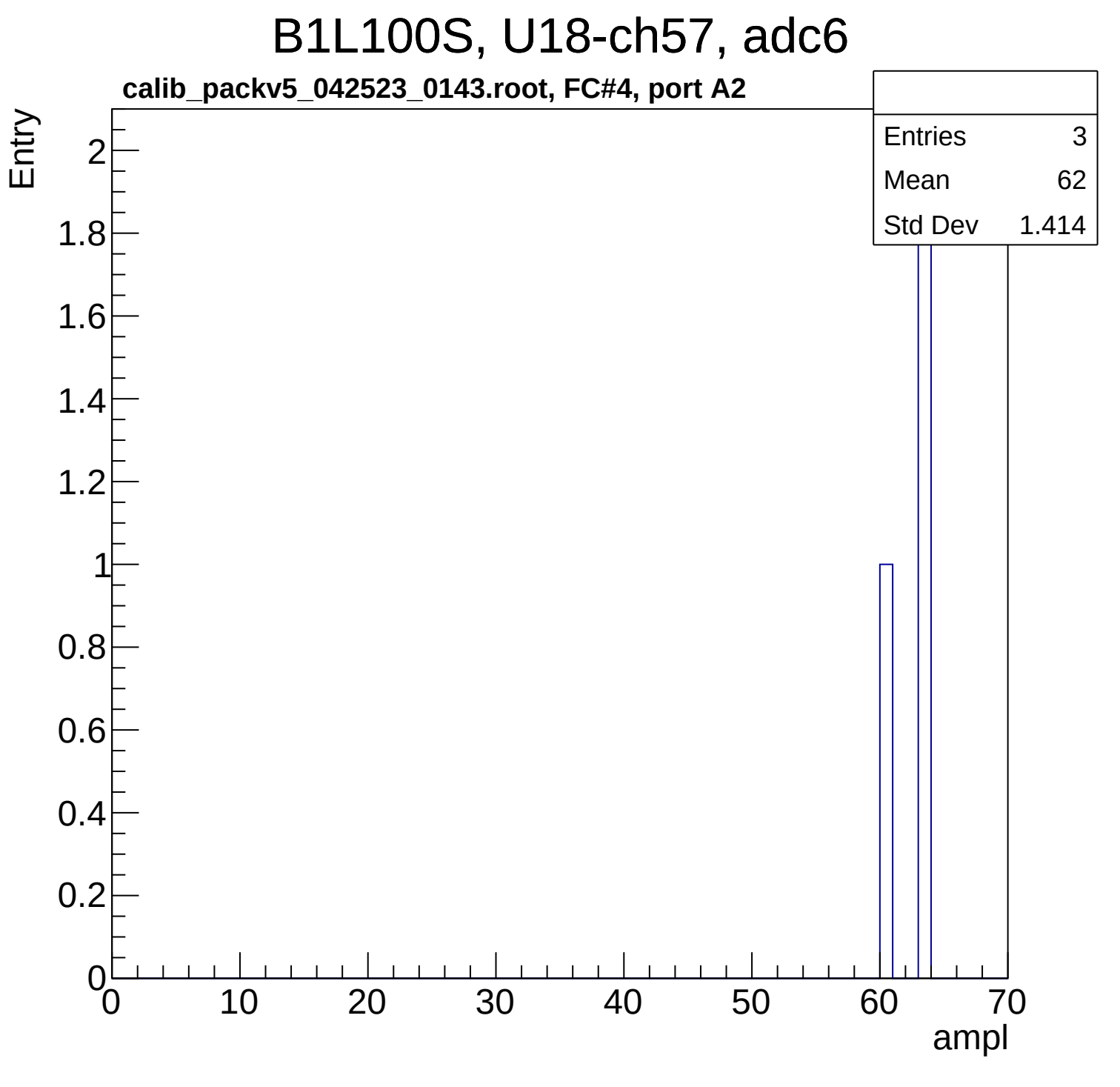

B1L100S, U18-ch57, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 36.14
Std Dev 3.887
Gaus mean : 36.8473
Gaus Width: 3.2771
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

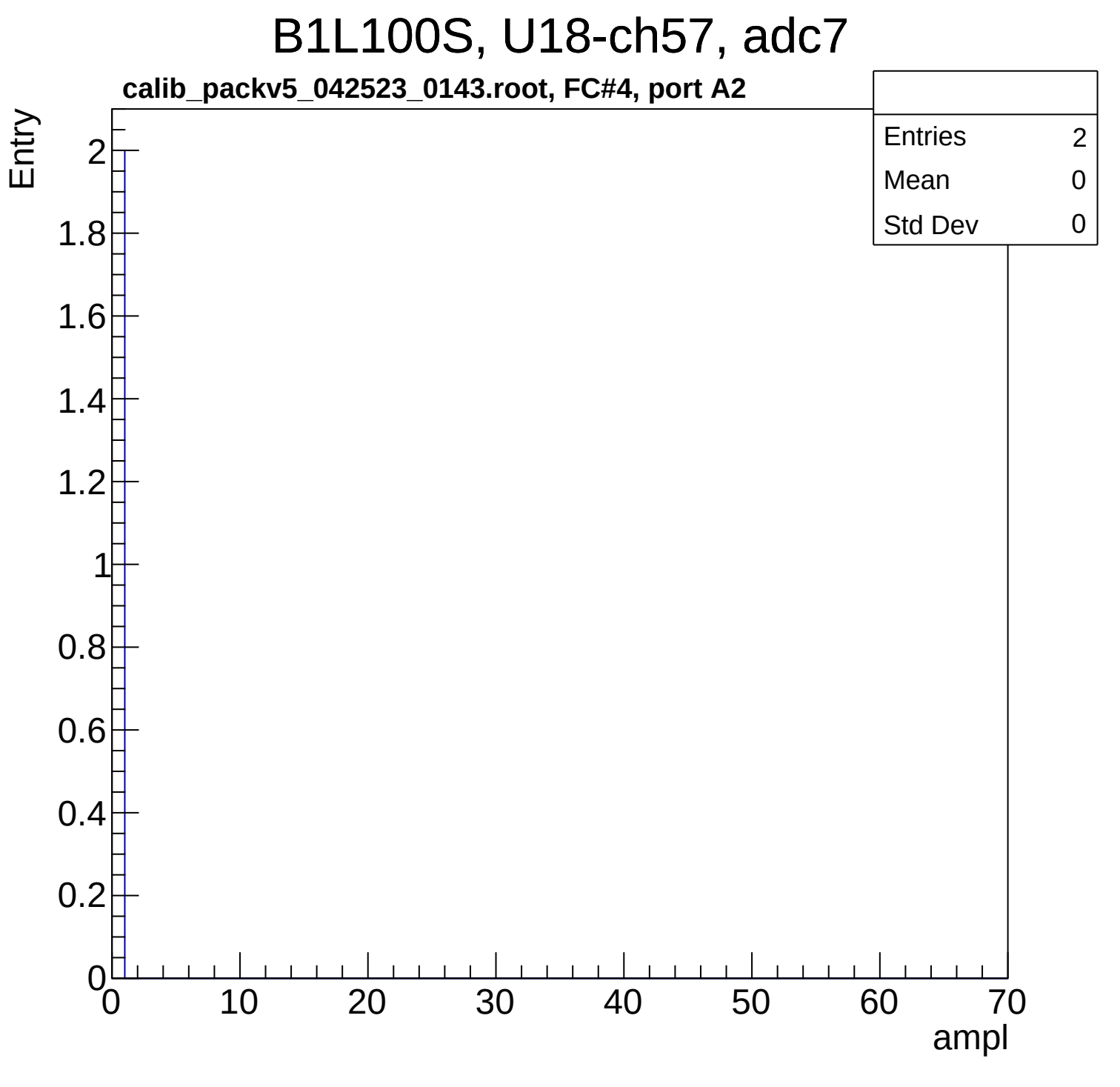

B1L100S, U18-ch57, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 44.09
Std Dev 3.96
Gaus mean : 44.5324
Gaus Width: 3.9417
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

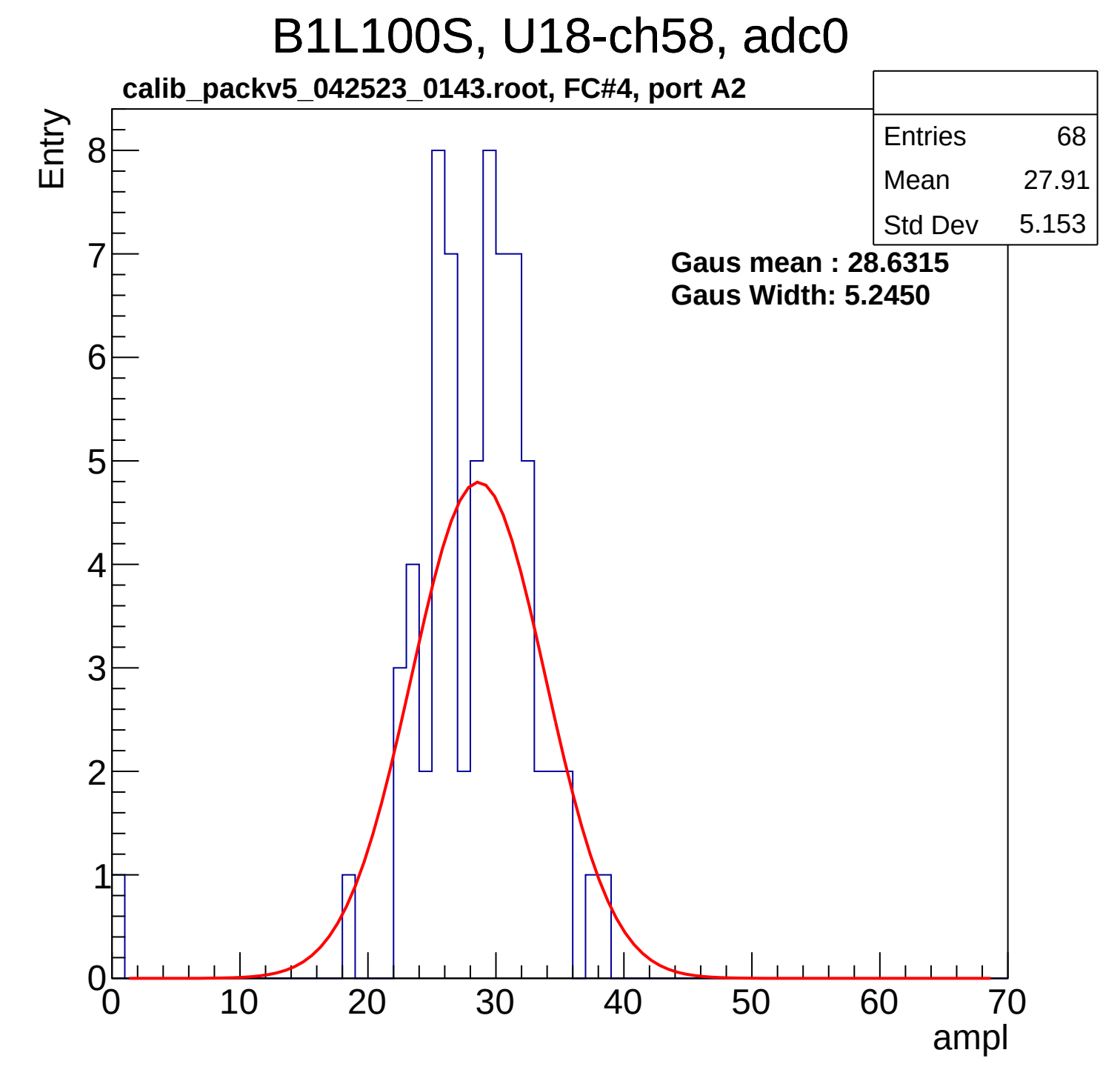

B1L100S, U18-ch57, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 50.39
Std Dev 3.919
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

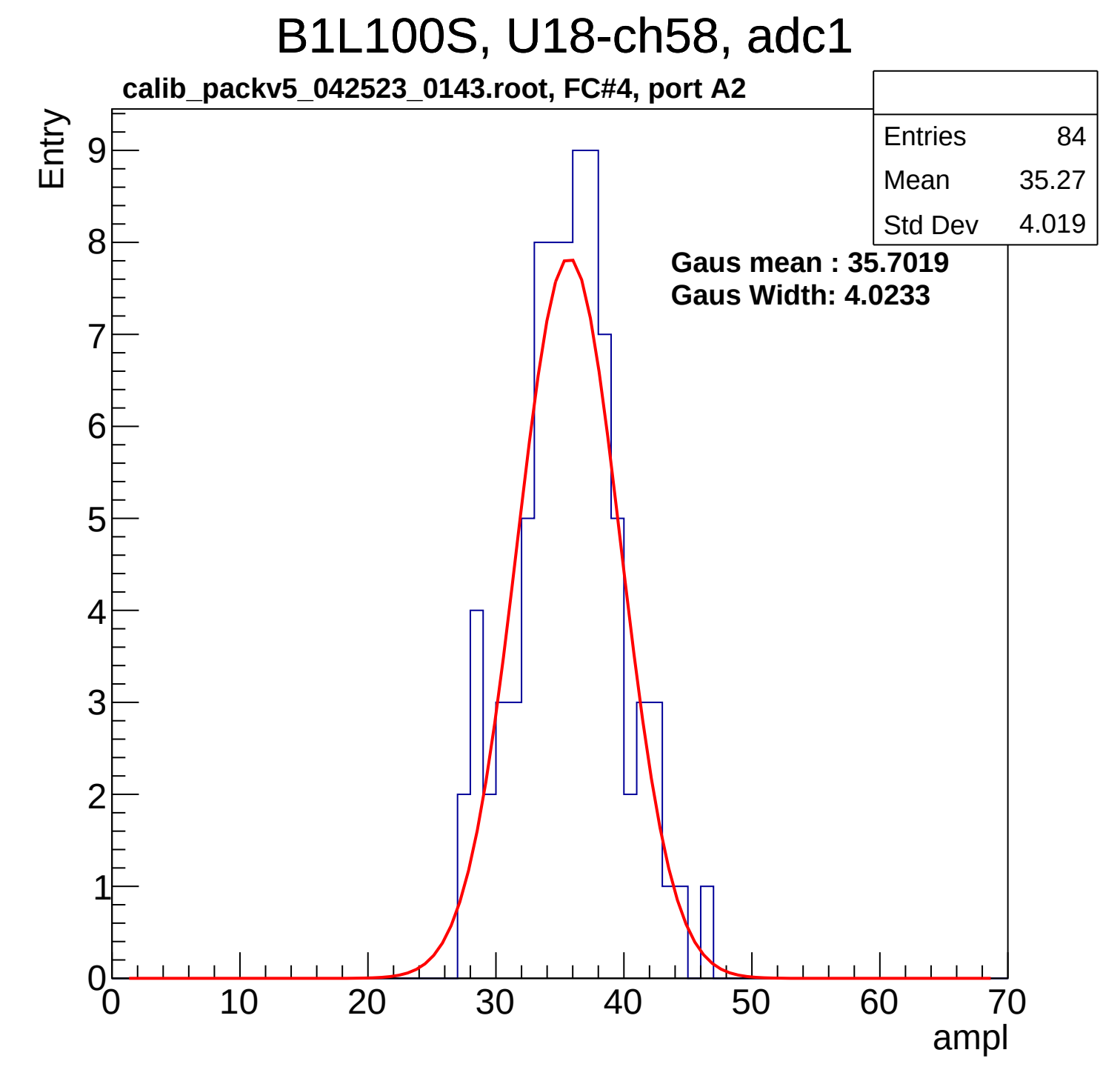

B1L100S, U18-ch57, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 56.4
Std Dev 3.597
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

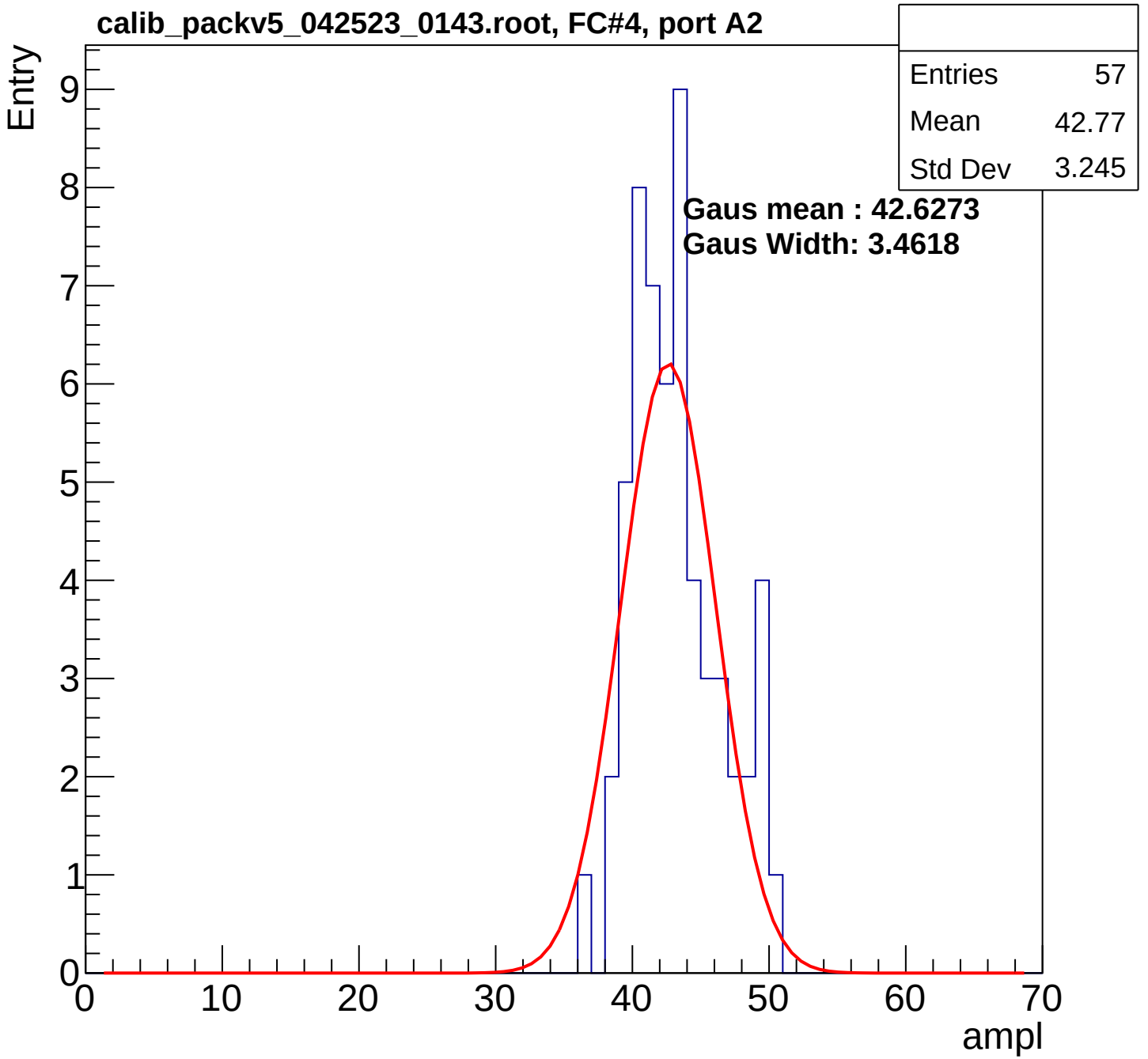

B1L100S, U18-ch57, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 38
Mean 58.5
Std Dev 9.907
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

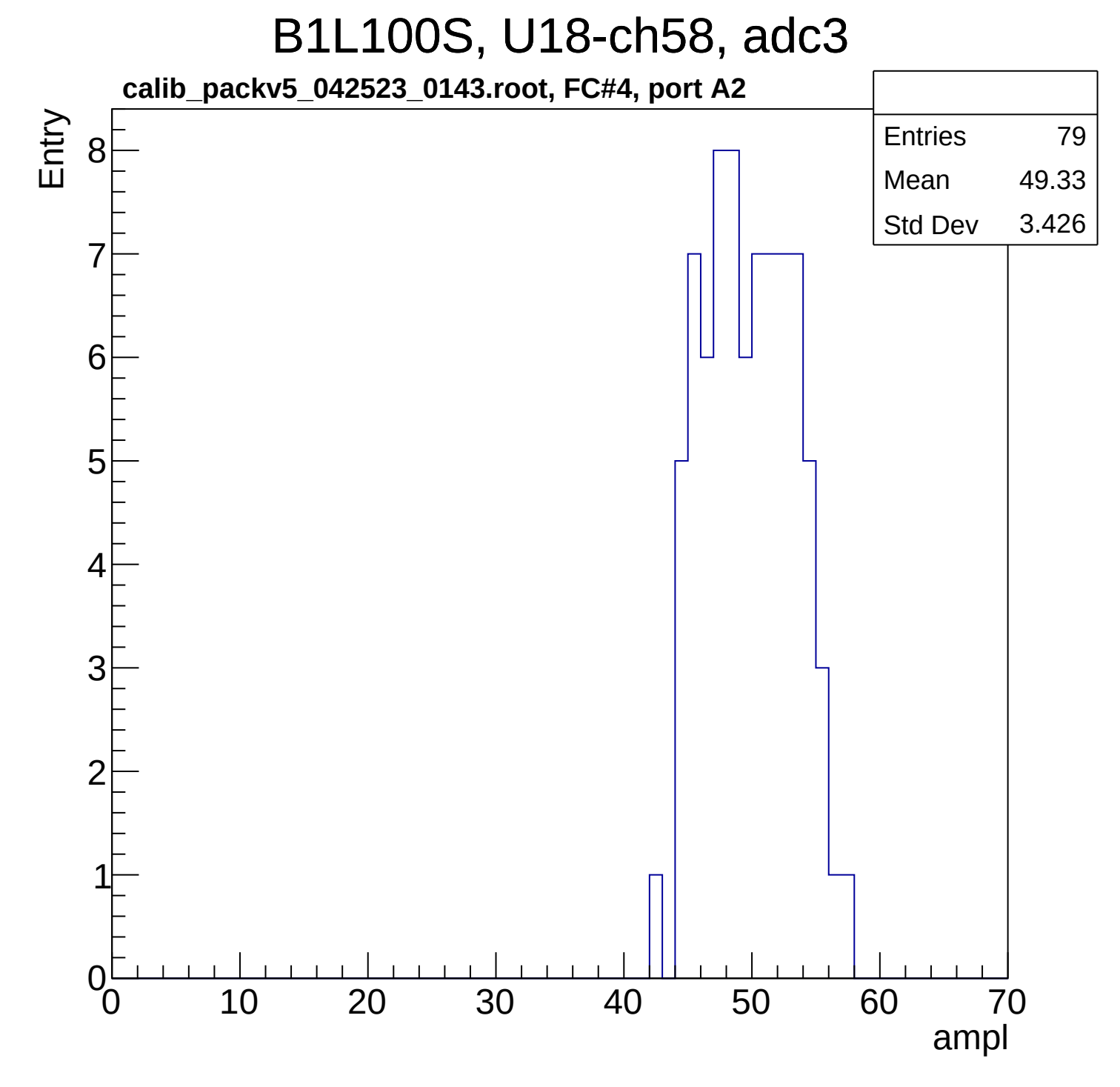

B1L100S, U18-ch57, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 62
Std Dev 1.414
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

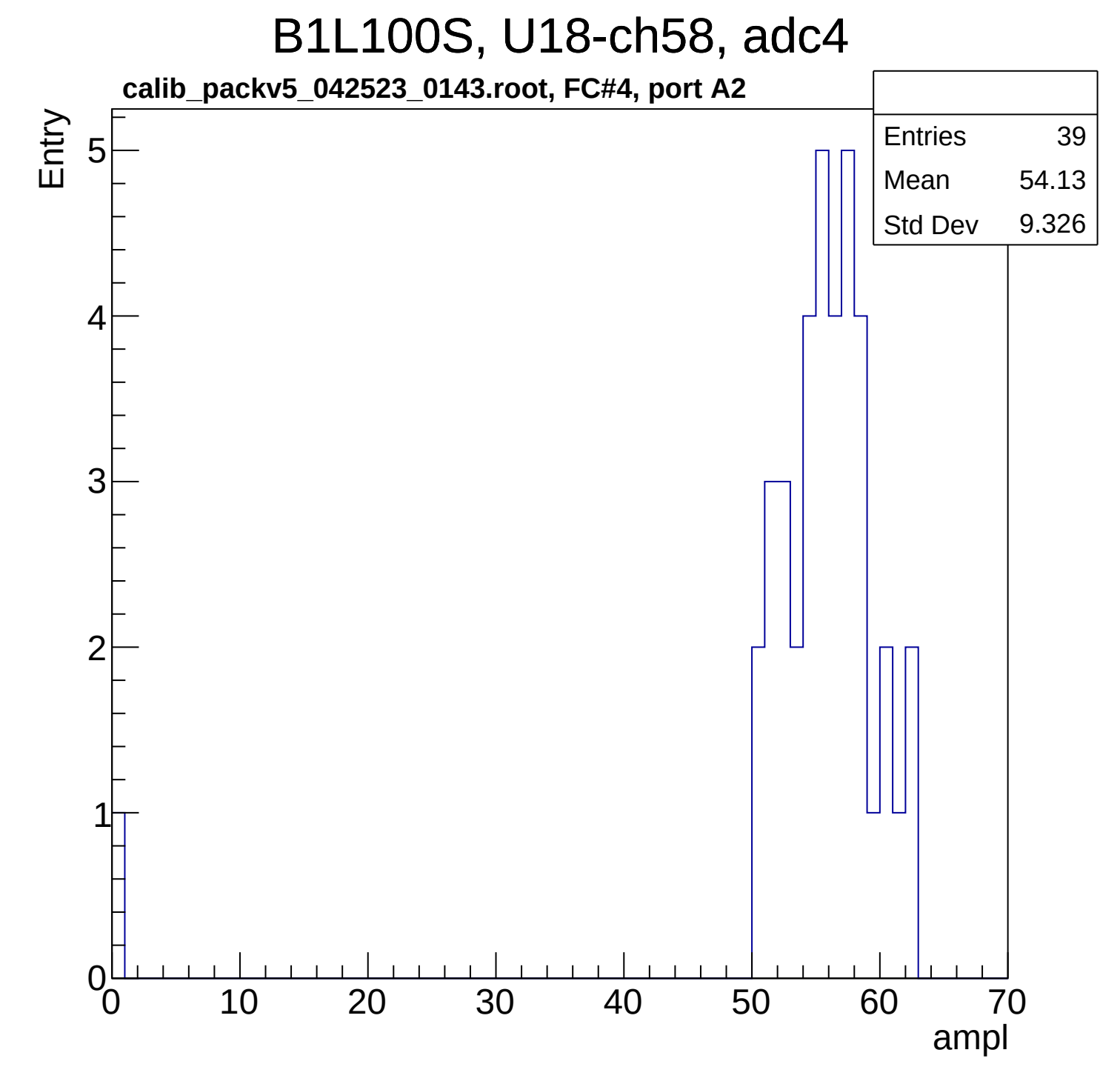

B1L100S, U18-ch57, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

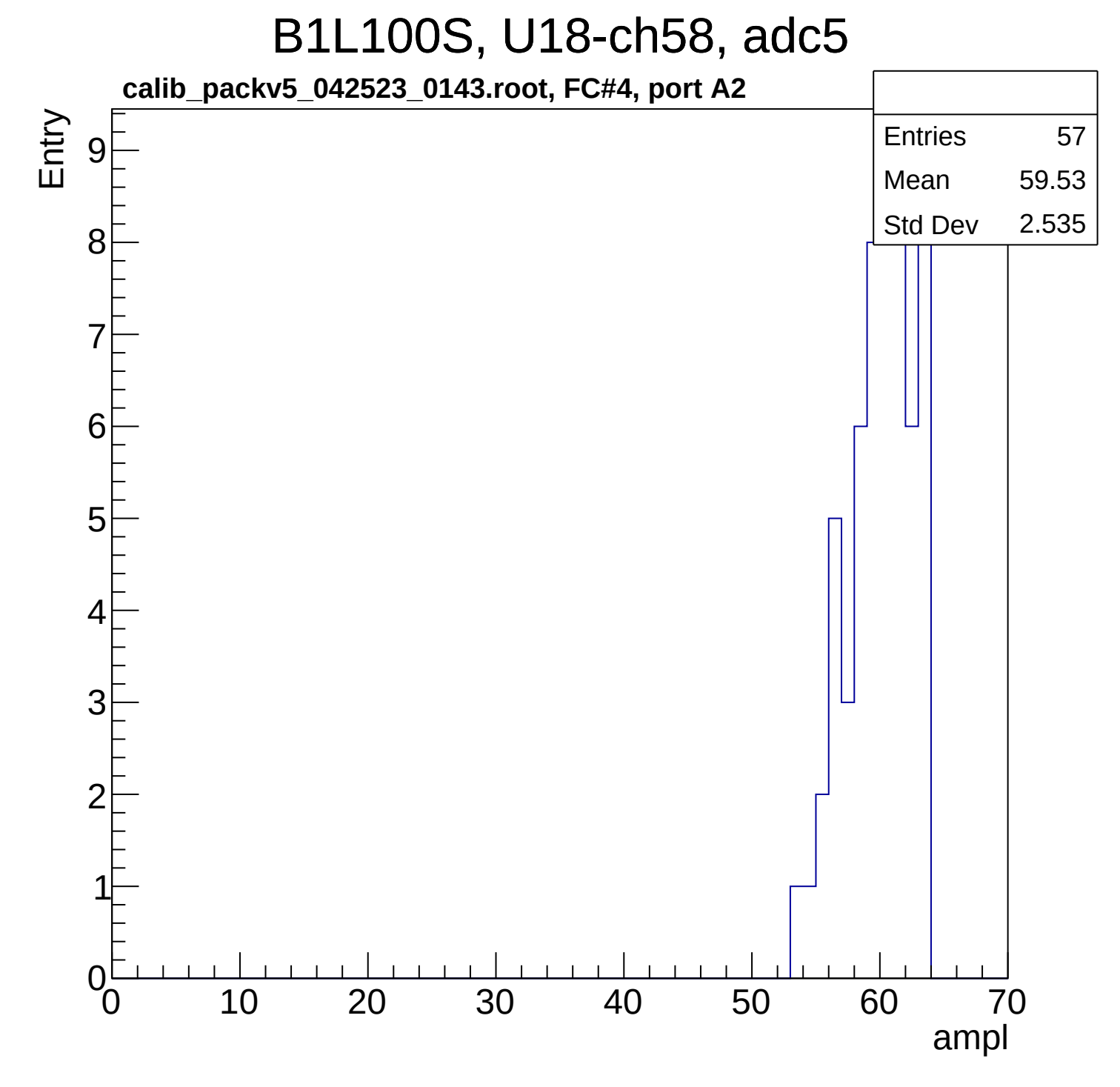

B1L100S, U18-ch58, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 27.91
Std Dev 5.153
Gaus mean : 28.6315
Gaus Width: 5.2450
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

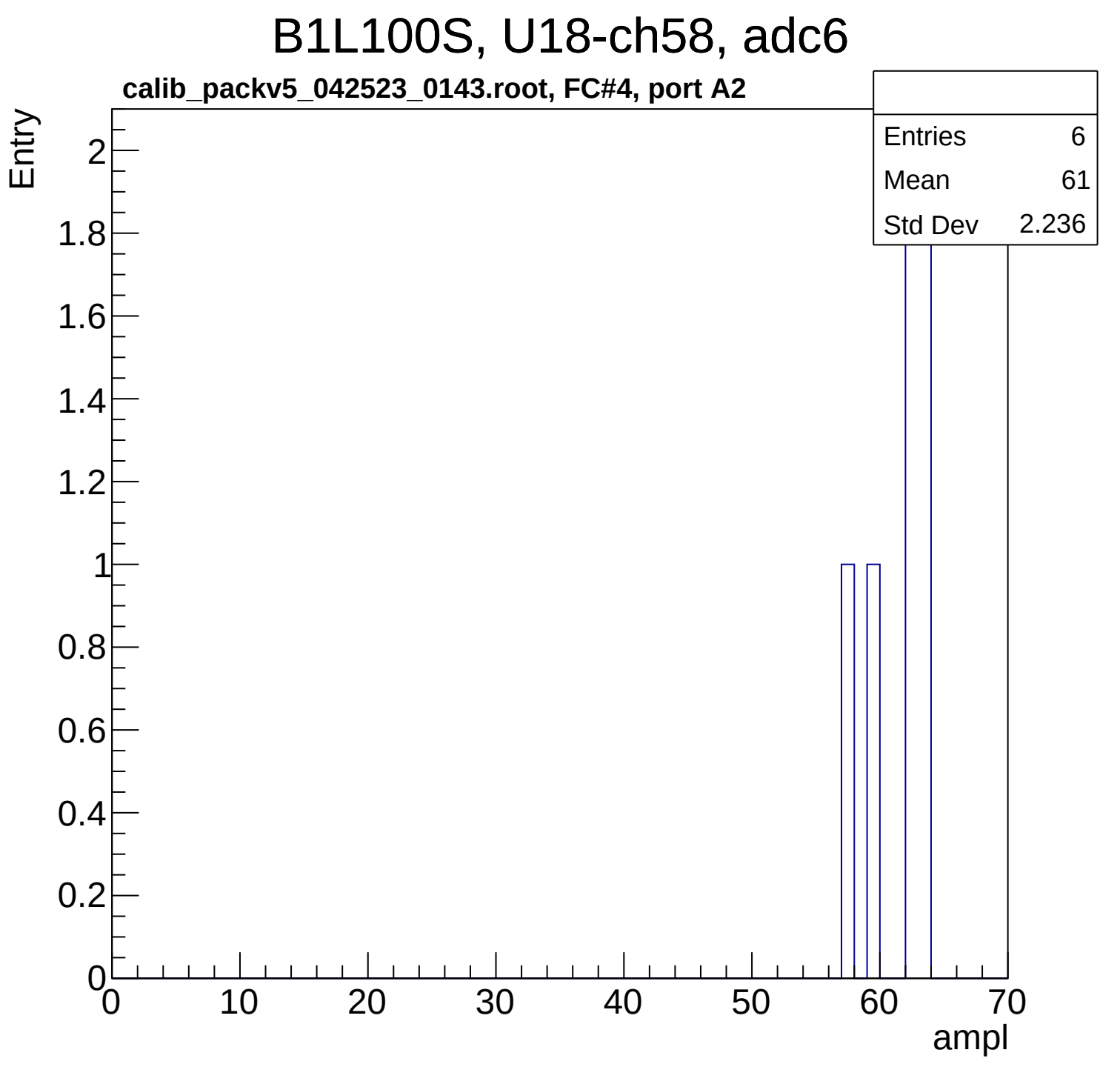

B1L100S, U18-ch58, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 84
Mean 35.27
Std Dev 4.019
Gaus mean : 35.7019
Gaus Width: 4.0233
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

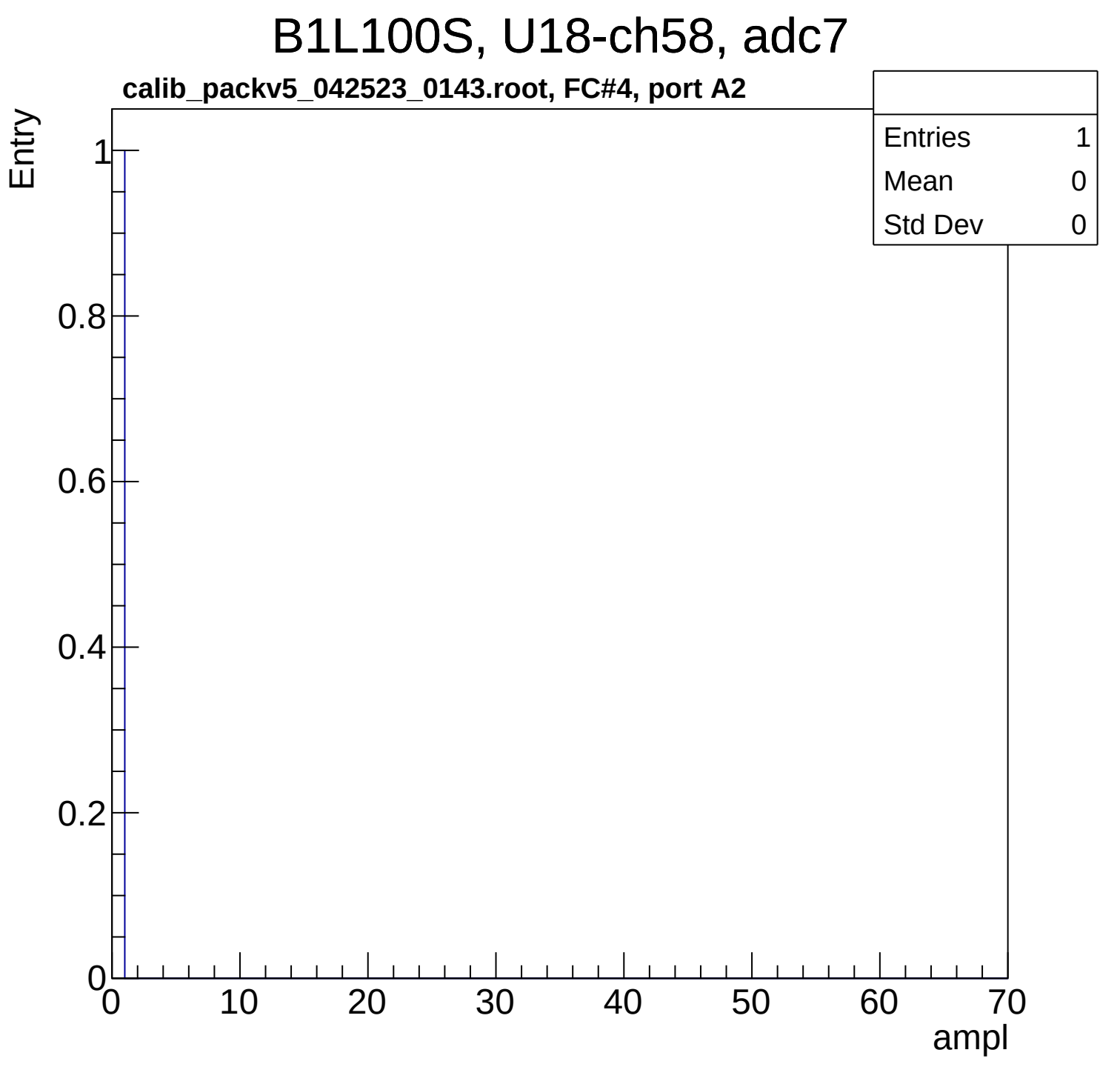

B1L100S, U18-ch58, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 42.77
Std Dev 3.245
Gaus mean : 42.6273
Gaus Width: 3.4618
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

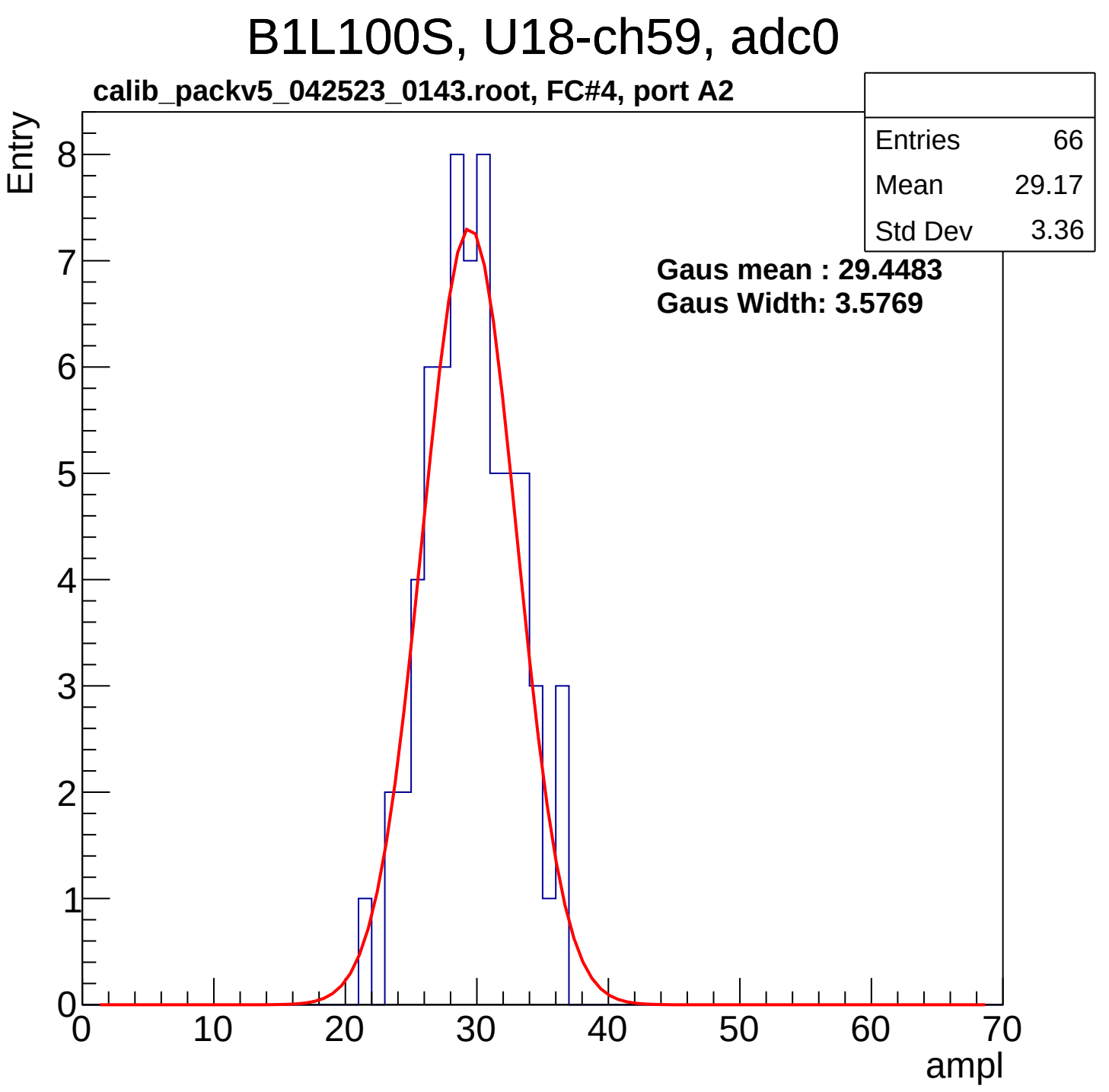

B1L100S, U18-ch58, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 49.33
Std Dev 3.426
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

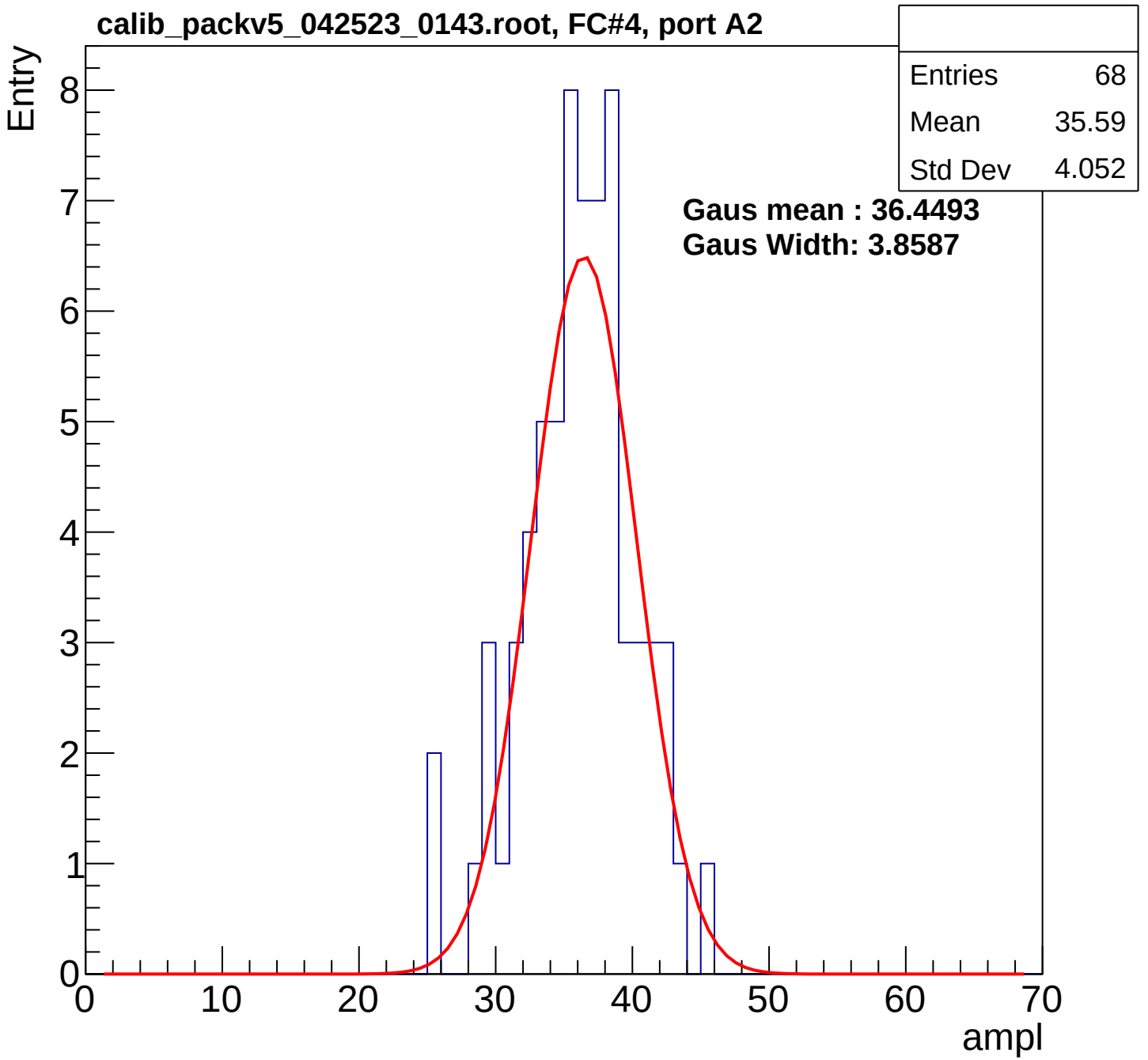

B1L100S, U18-ch58, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 39
Mean 54.13
Std Dev 9.326
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

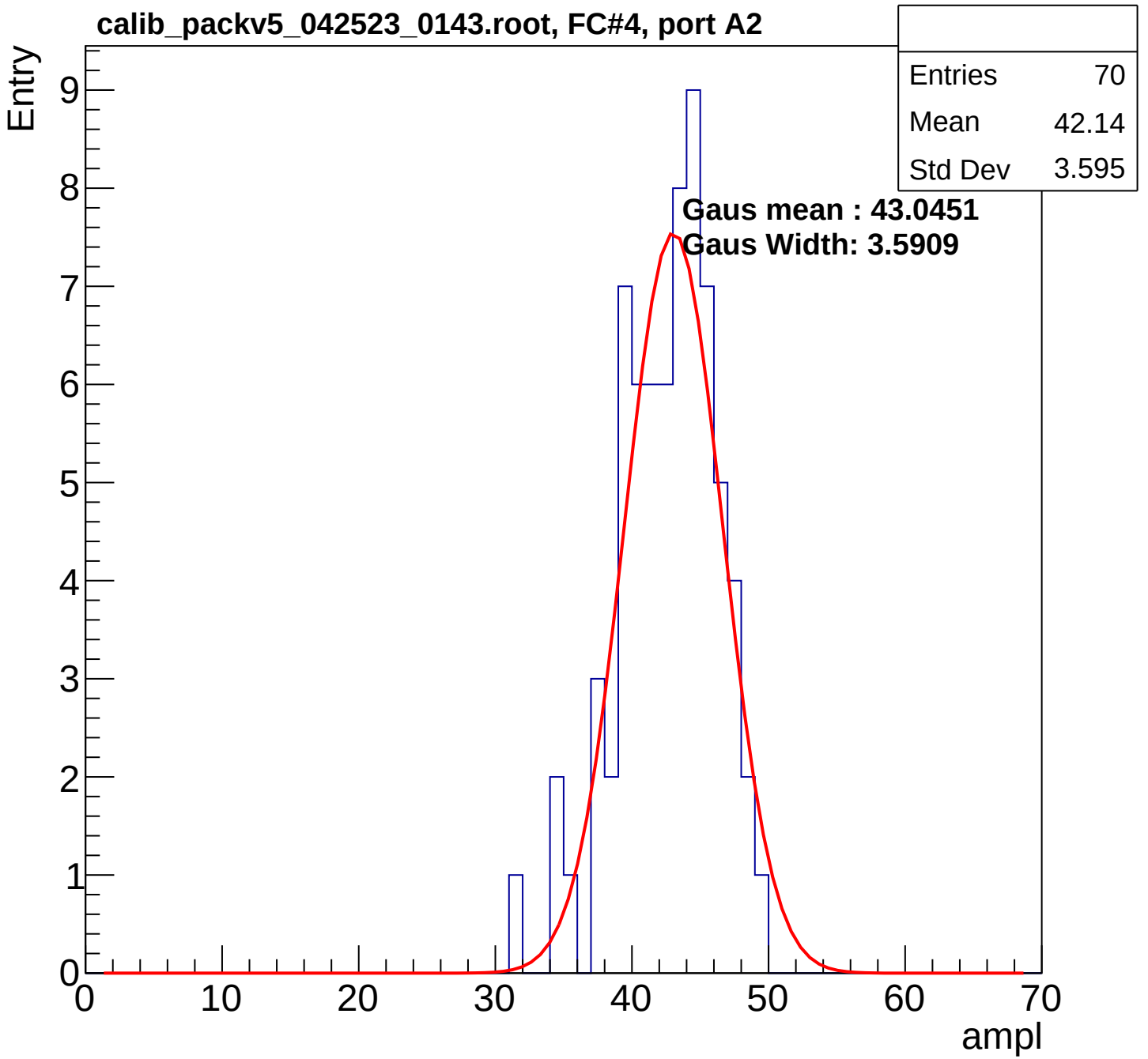

B1L100S, U18-ch58, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 59.53
Std Dev 2.535
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

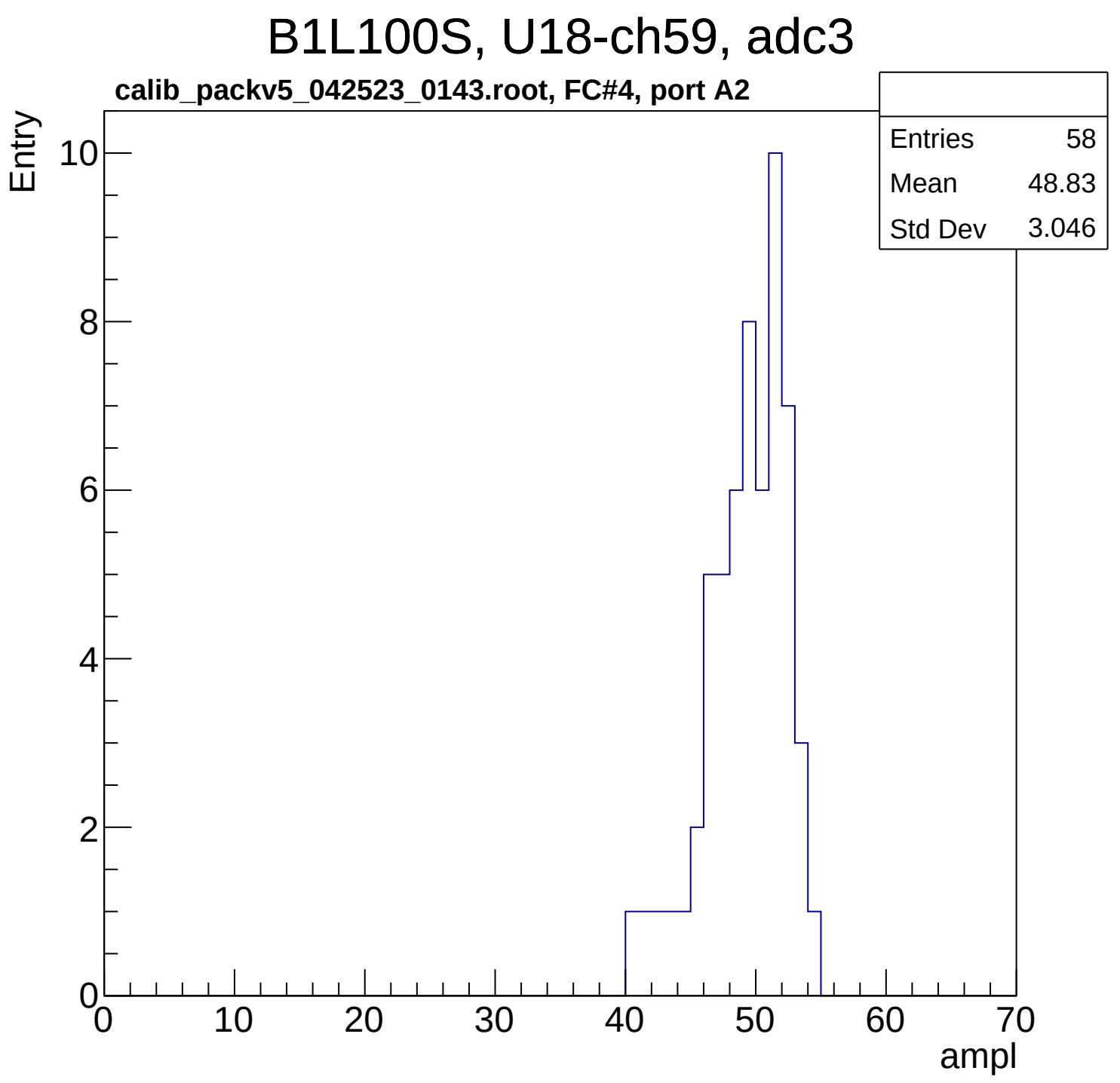

B1L100S, U18-ch58, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 61
Std Dev 2.236
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

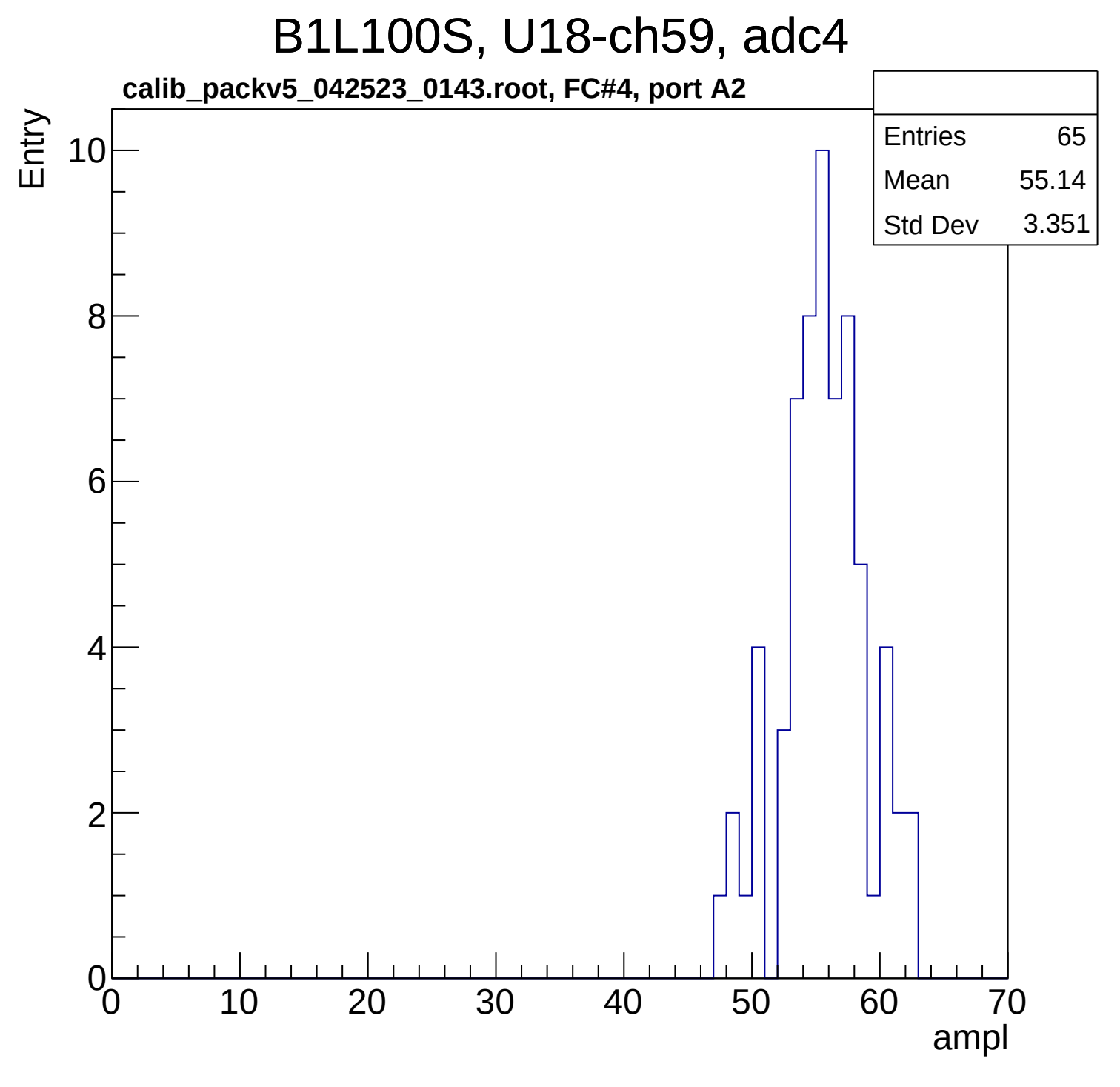

B1L100S, U18-ch58, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

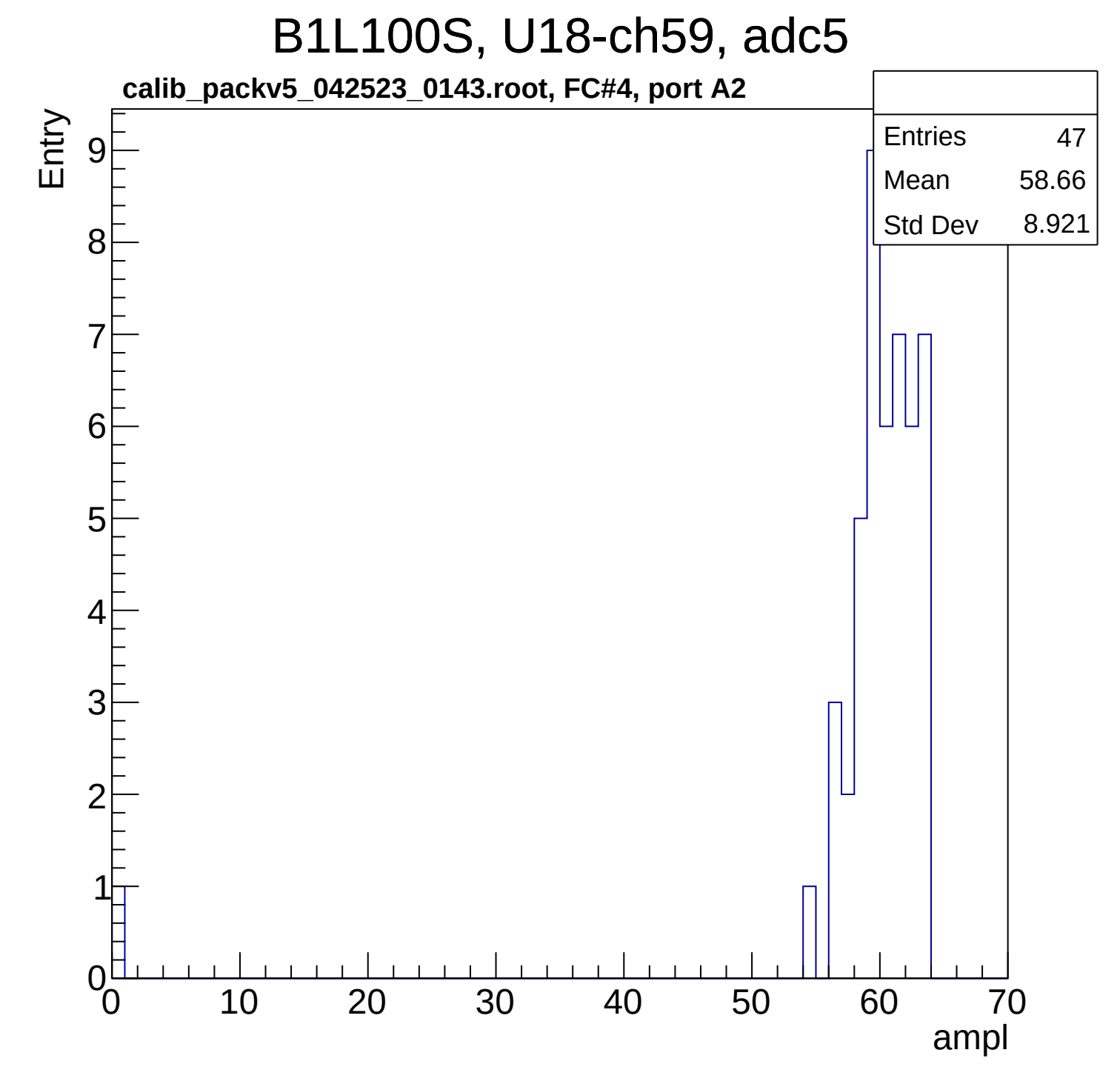

B1L100S, U18-ch59, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 29.17
Std Dev 3.36
Gaus mean : 29.4483
Gaus Width: 3.5769
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

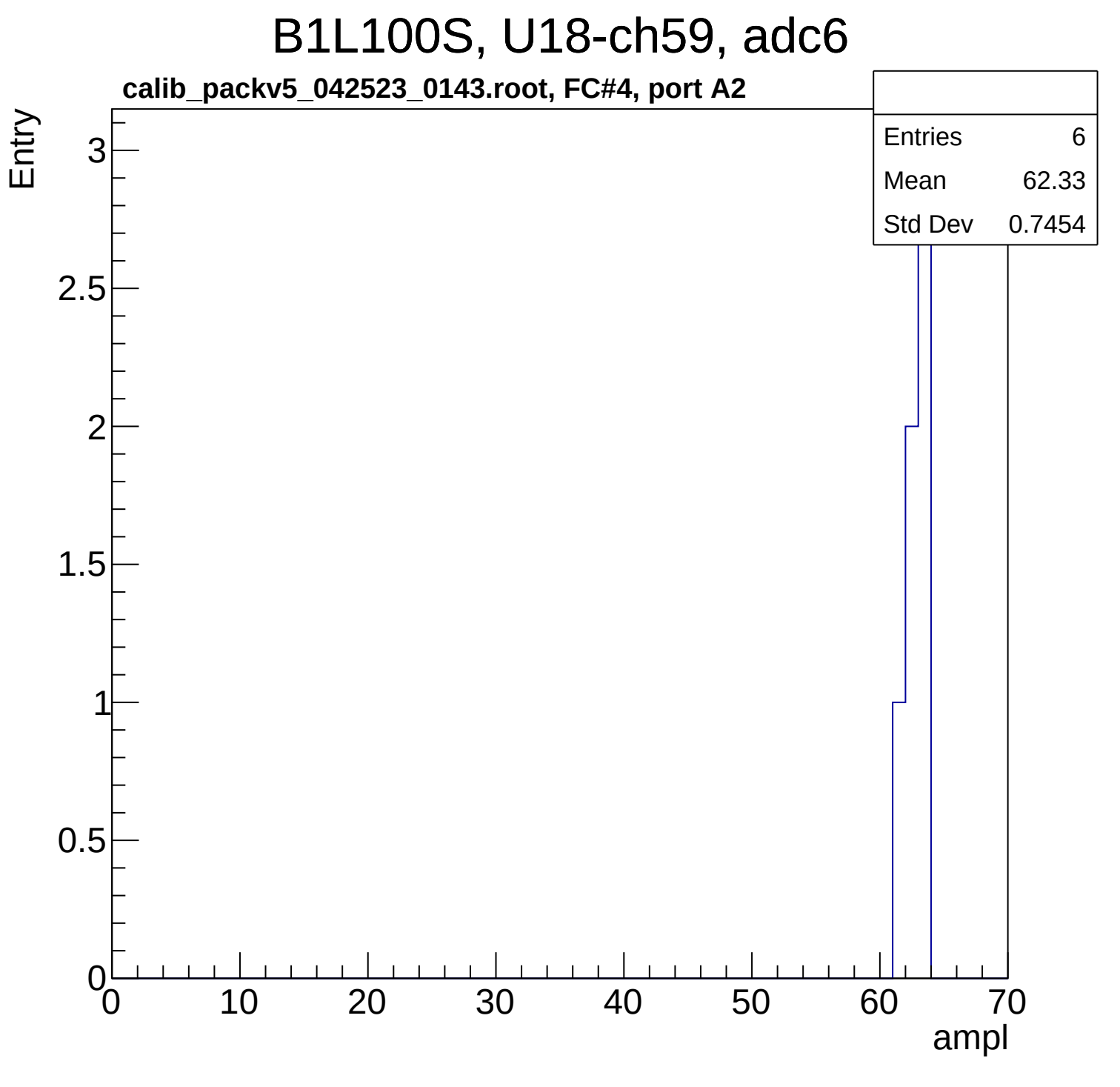

B1L100S, U18-ch59, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 35.59
Std Dev 4.052
Gaus mean : 36.4493
Gaus Width: 3.8587
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

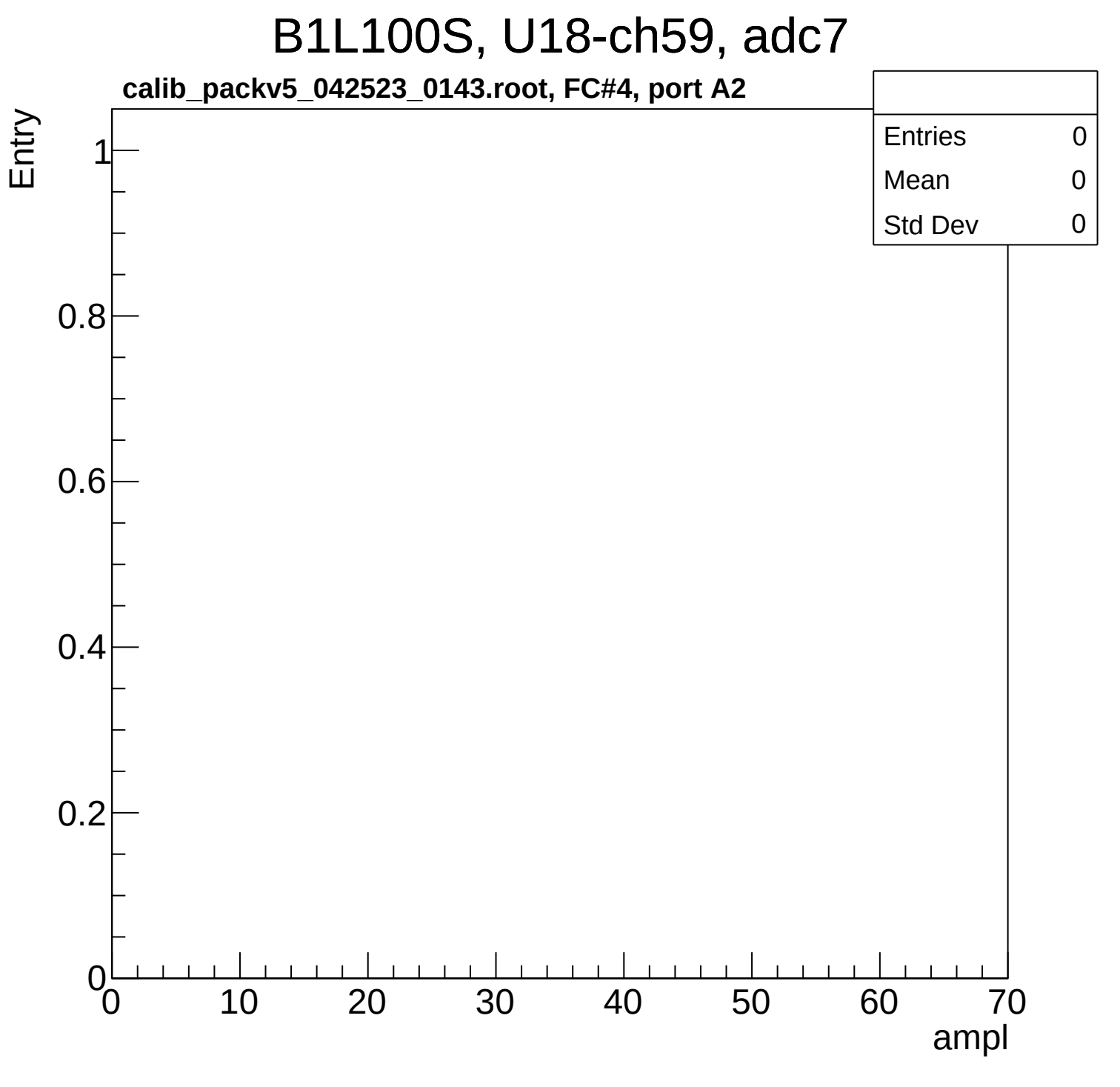

B1L100S, U18-ch59, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 42.14
Std Dev 3.595
Gaus mean : 43.0451
Gaus Width: 3.5909
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

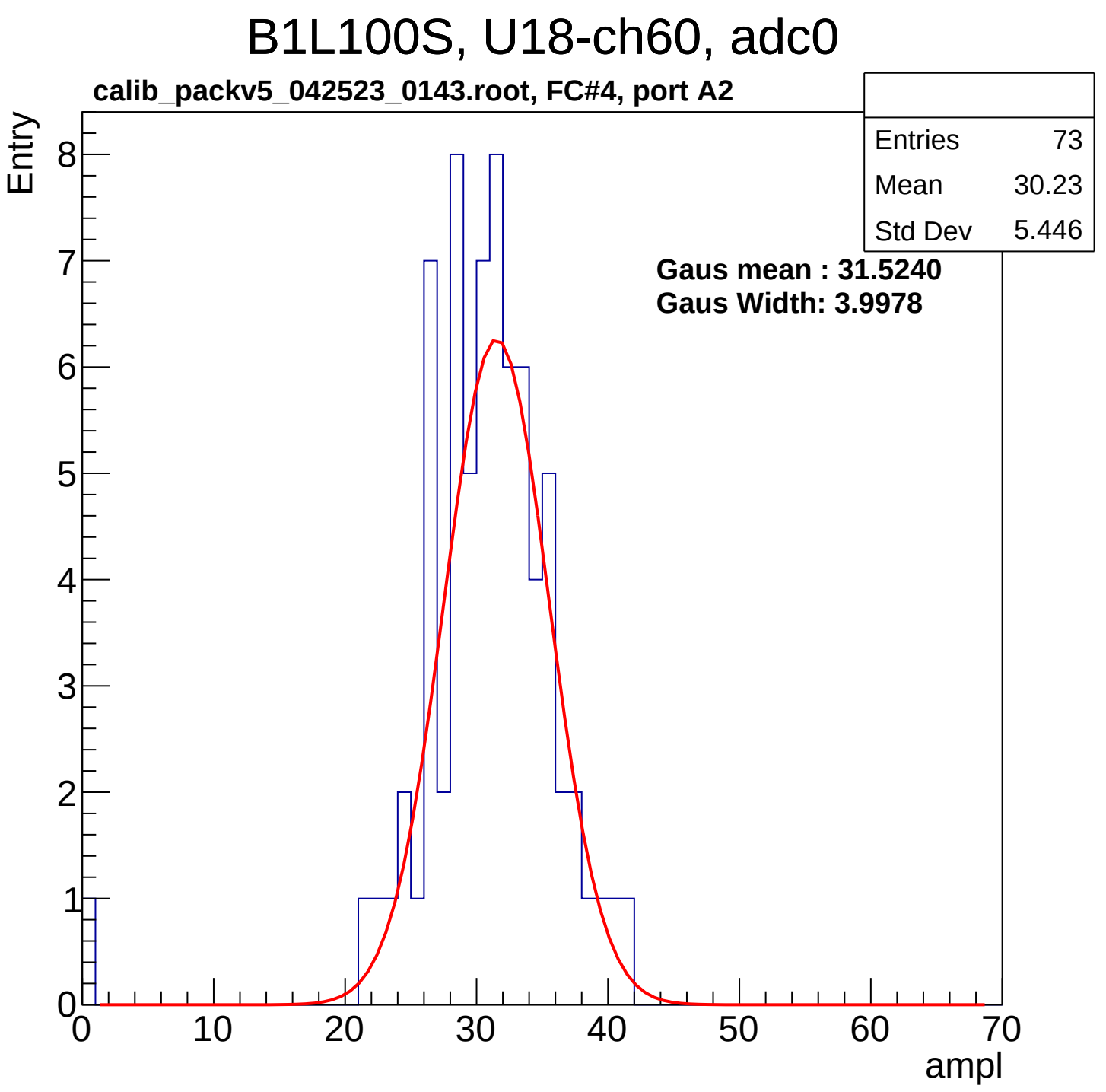

B1L100S, U18-ch59, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 48.83
Std Dev 3.046
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

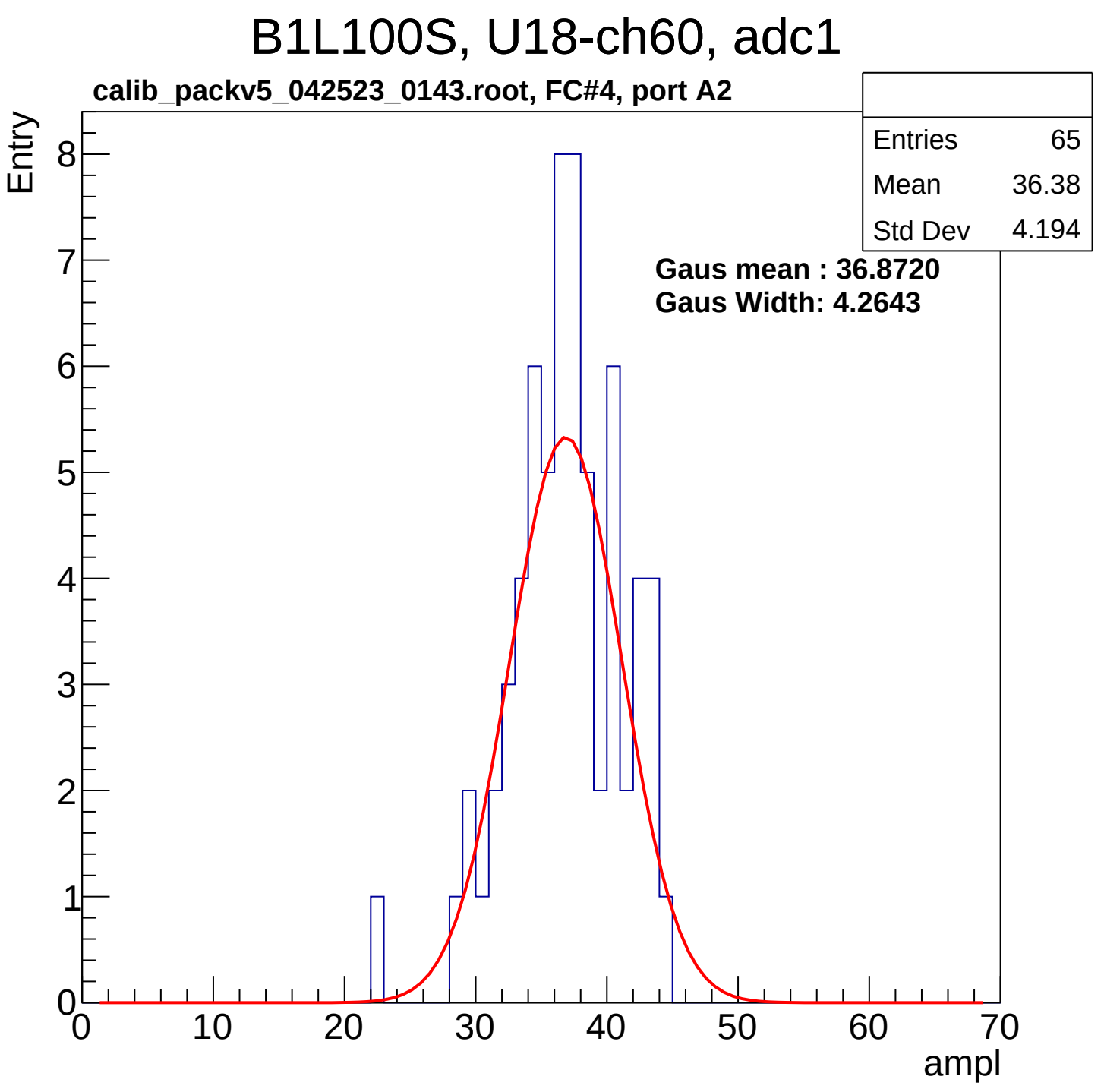

B1L100S, U18-ch59, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 55.14
Std Dev 3.351
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

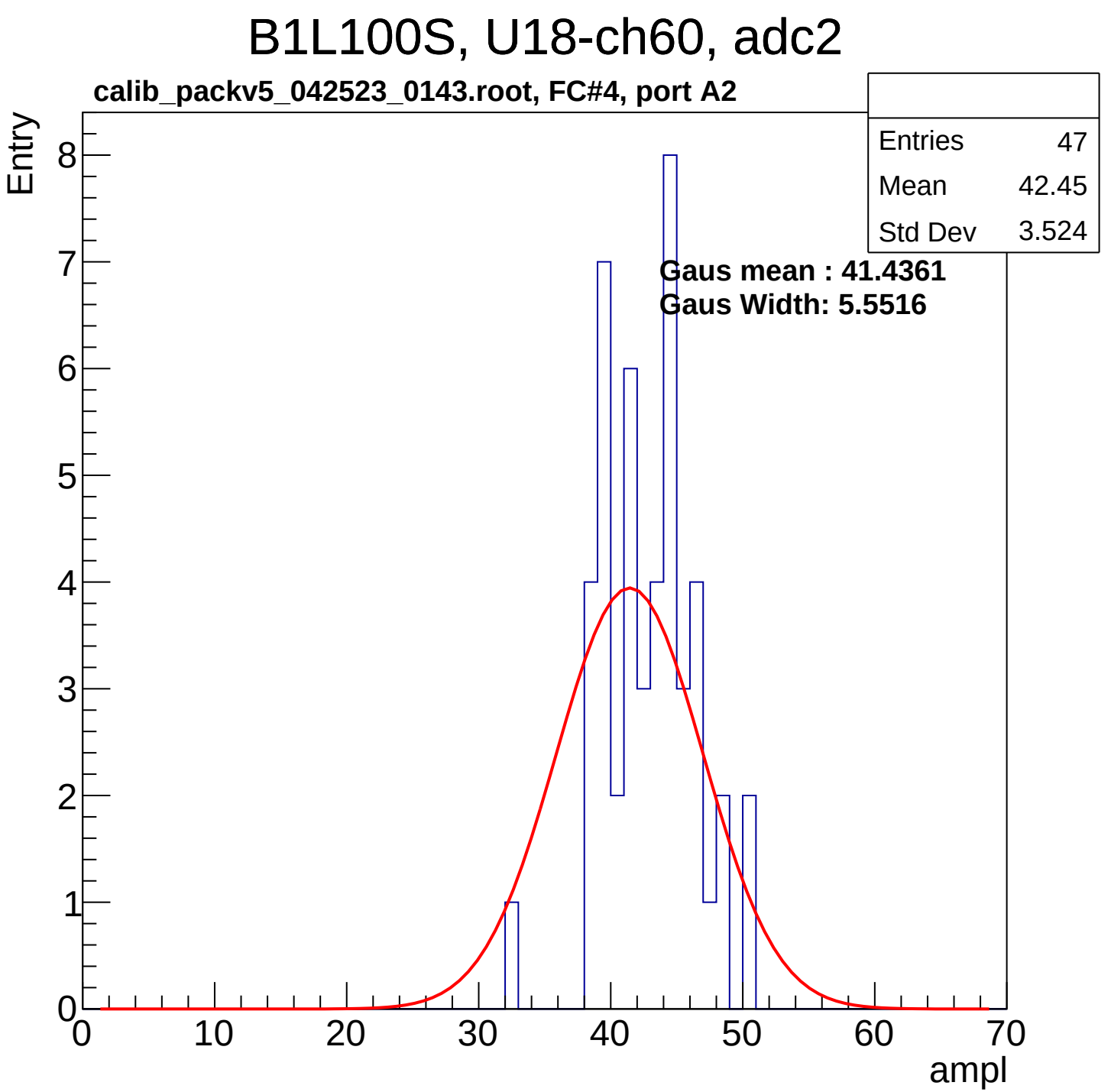

B1L100S, U18-ch59, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 58.66
Std Dev 8.921
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

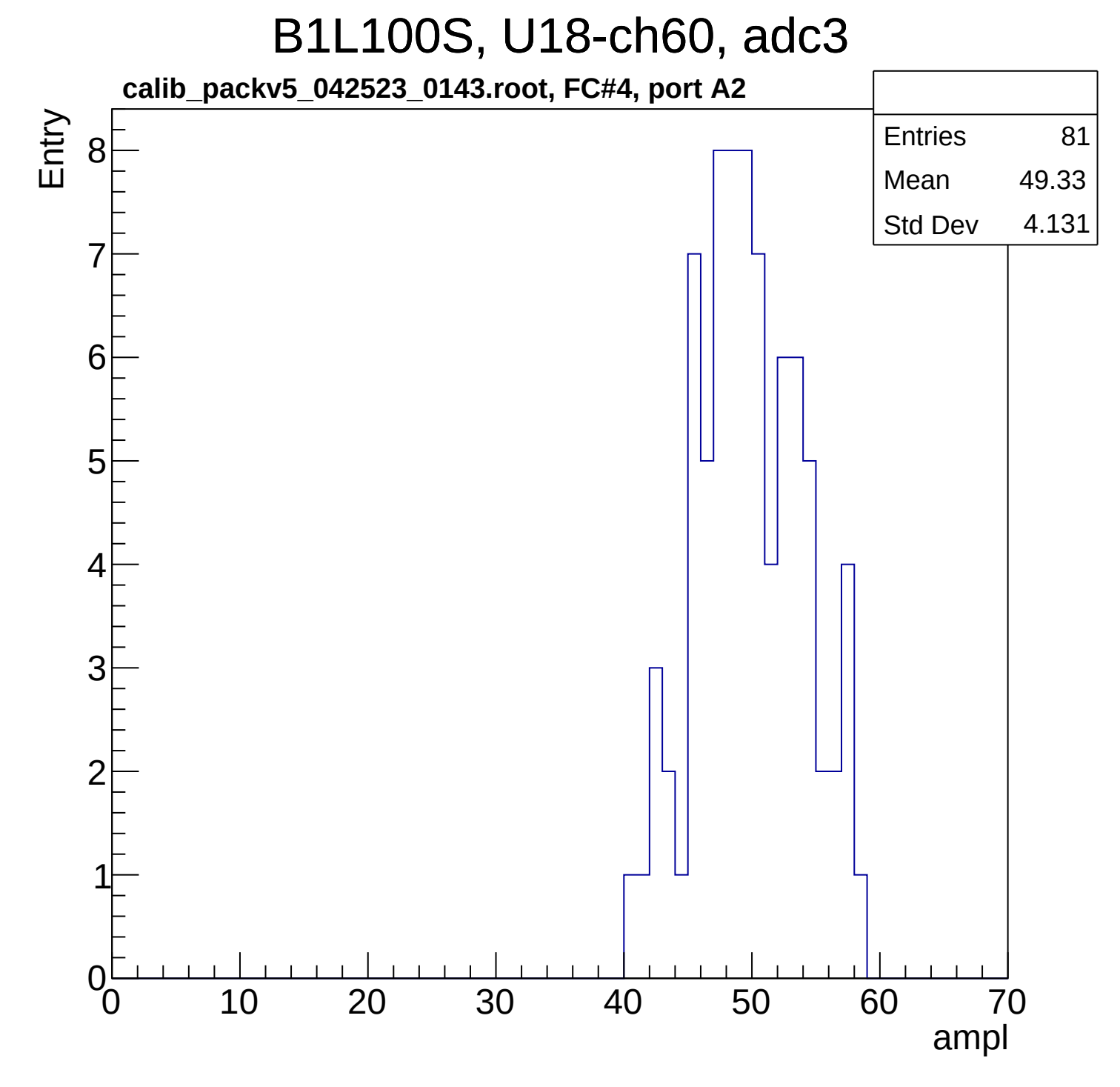

B1L100S, U18-ch59, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 62.33
Std Dev 0.7454
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

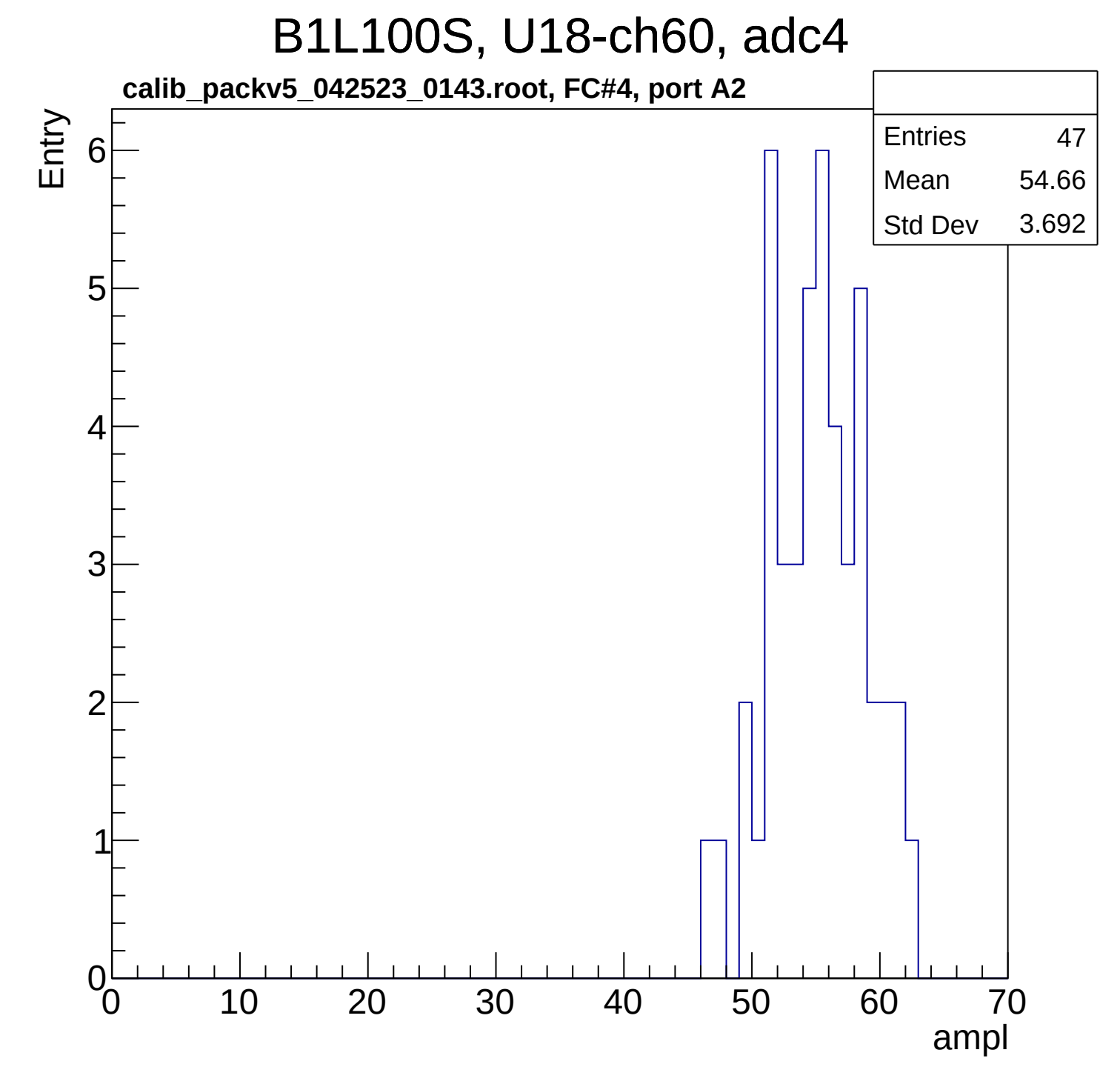

B1L100S, U18-ch59, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

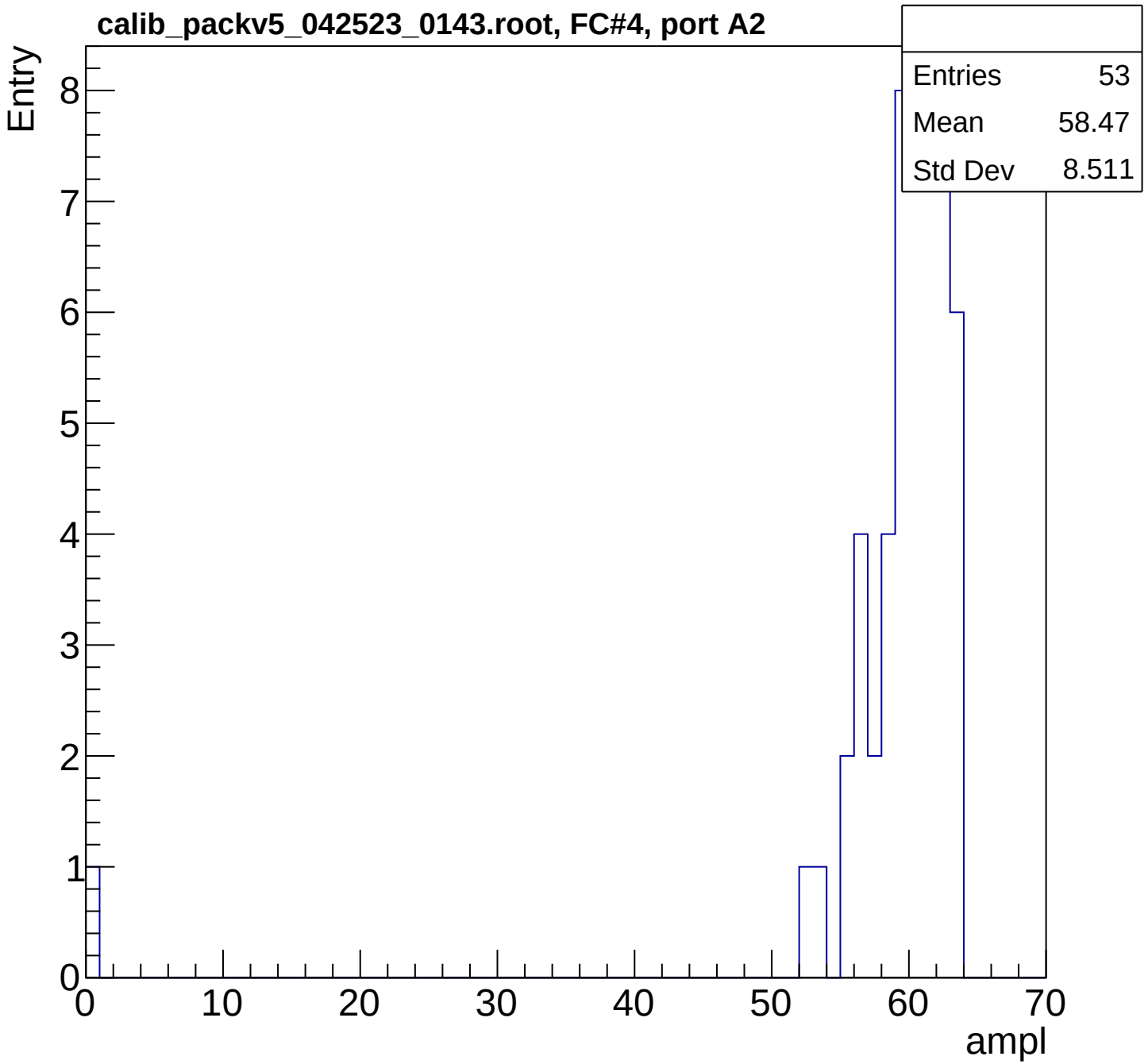

B1L100S, U18-ch60, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 30.23
Std Dev 5.446
Gaus mean : 31.5240
Gaus Width: 3.9978
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

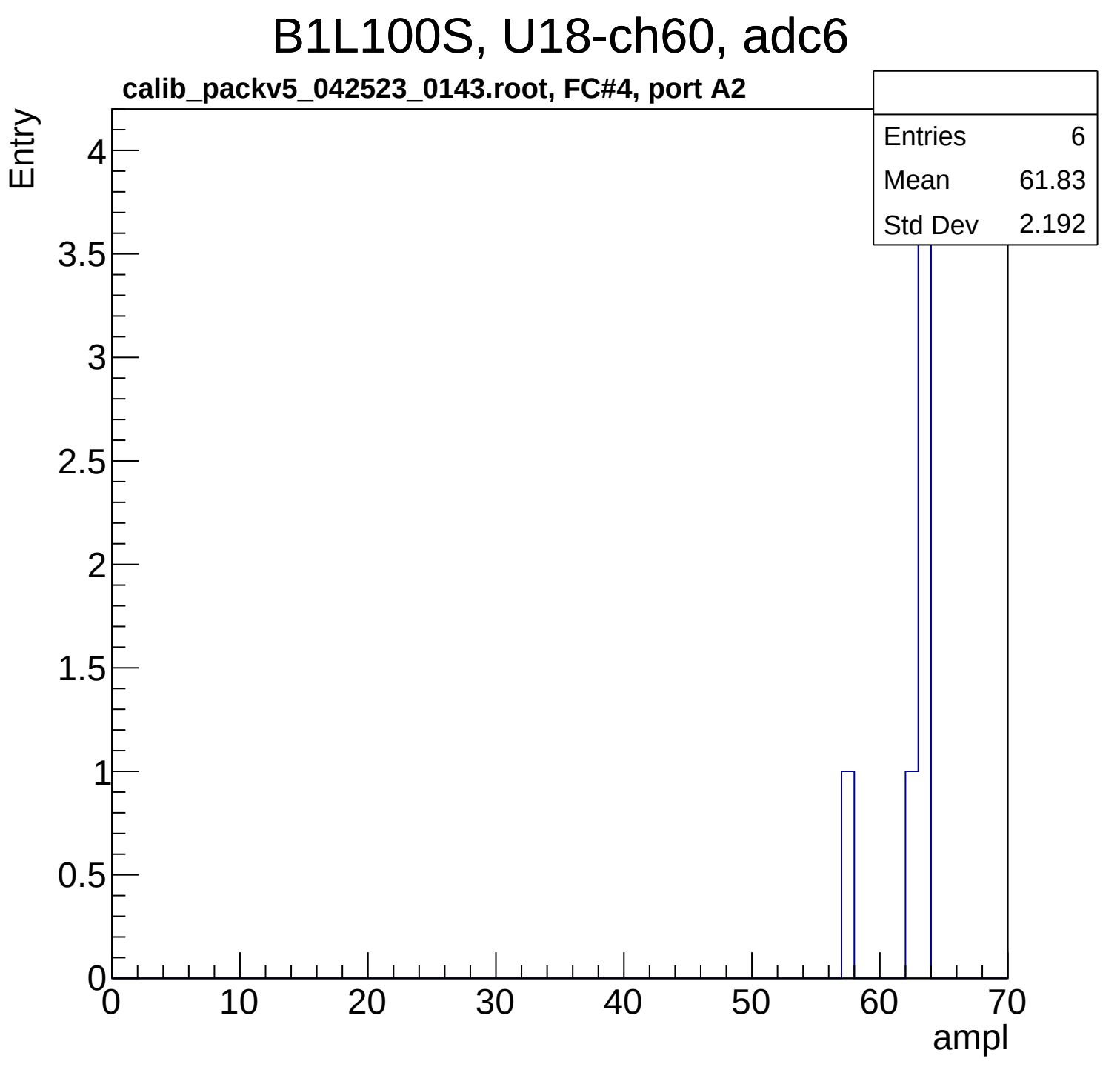

B1L100S, U18-ch60, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 36.38
Std Dev 4.194
Gaus mean : 36.8720
Gaus Width: 4.2643
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

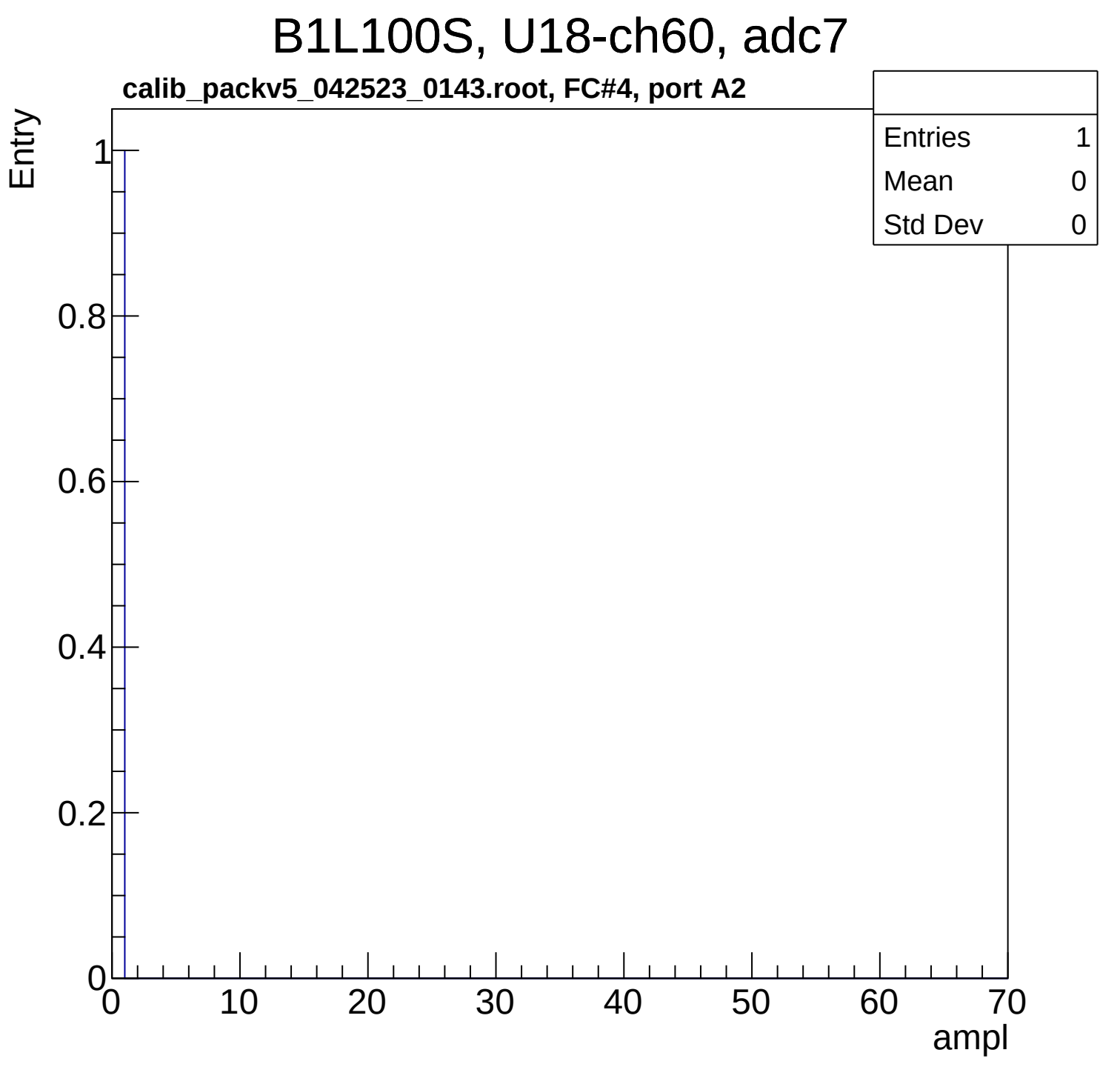

B1L100S, U18-ch60, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 42.45
Std Dev 3.524
Gaus mean : 41.4361
Gaus Width: 5.5516
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

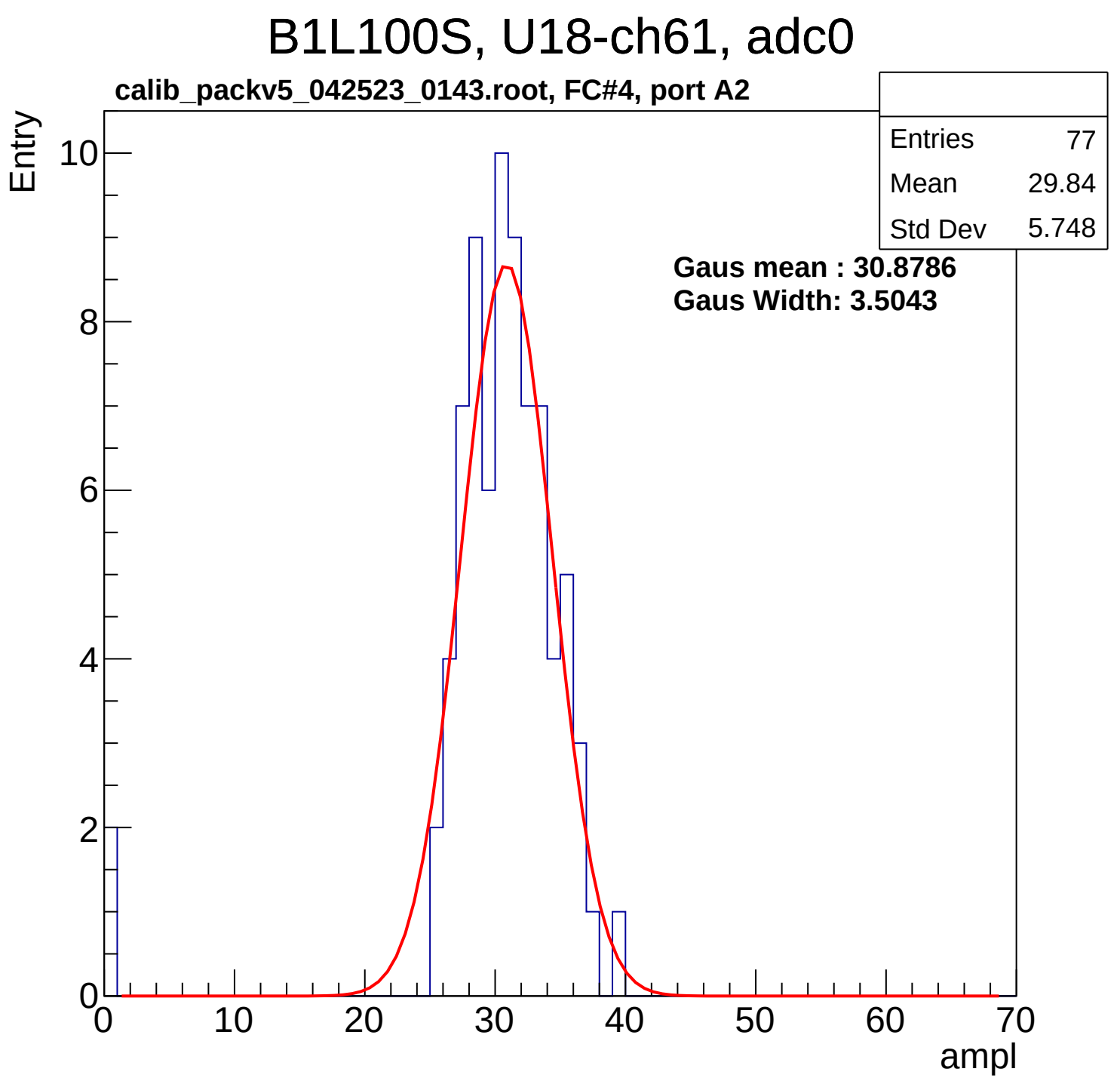

B1L100S, U18-ch60, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 49.33
Std Dev 4.131
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

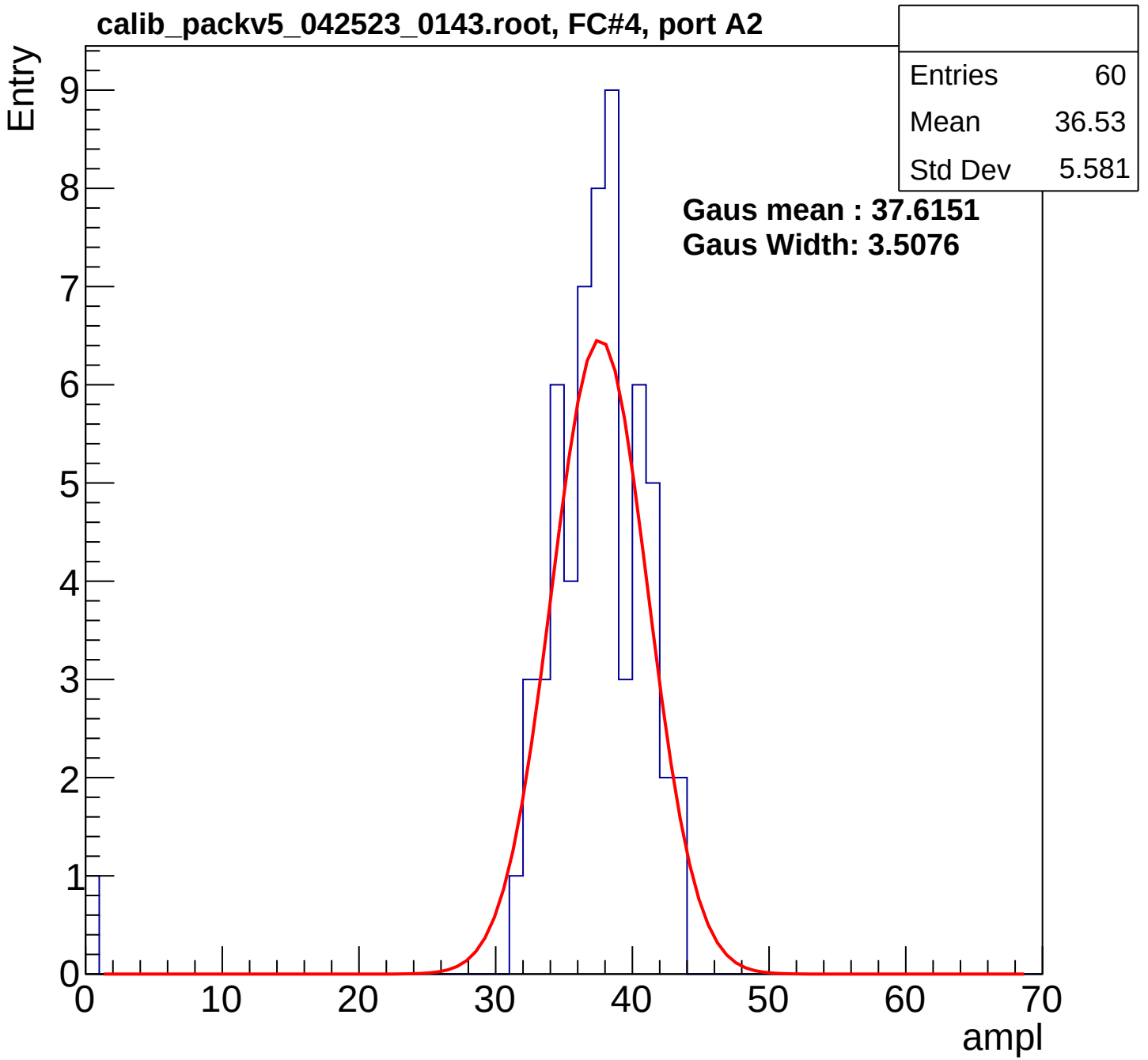

B1L100S, U18-ch60, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 54.66
Std Dev 3.692
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

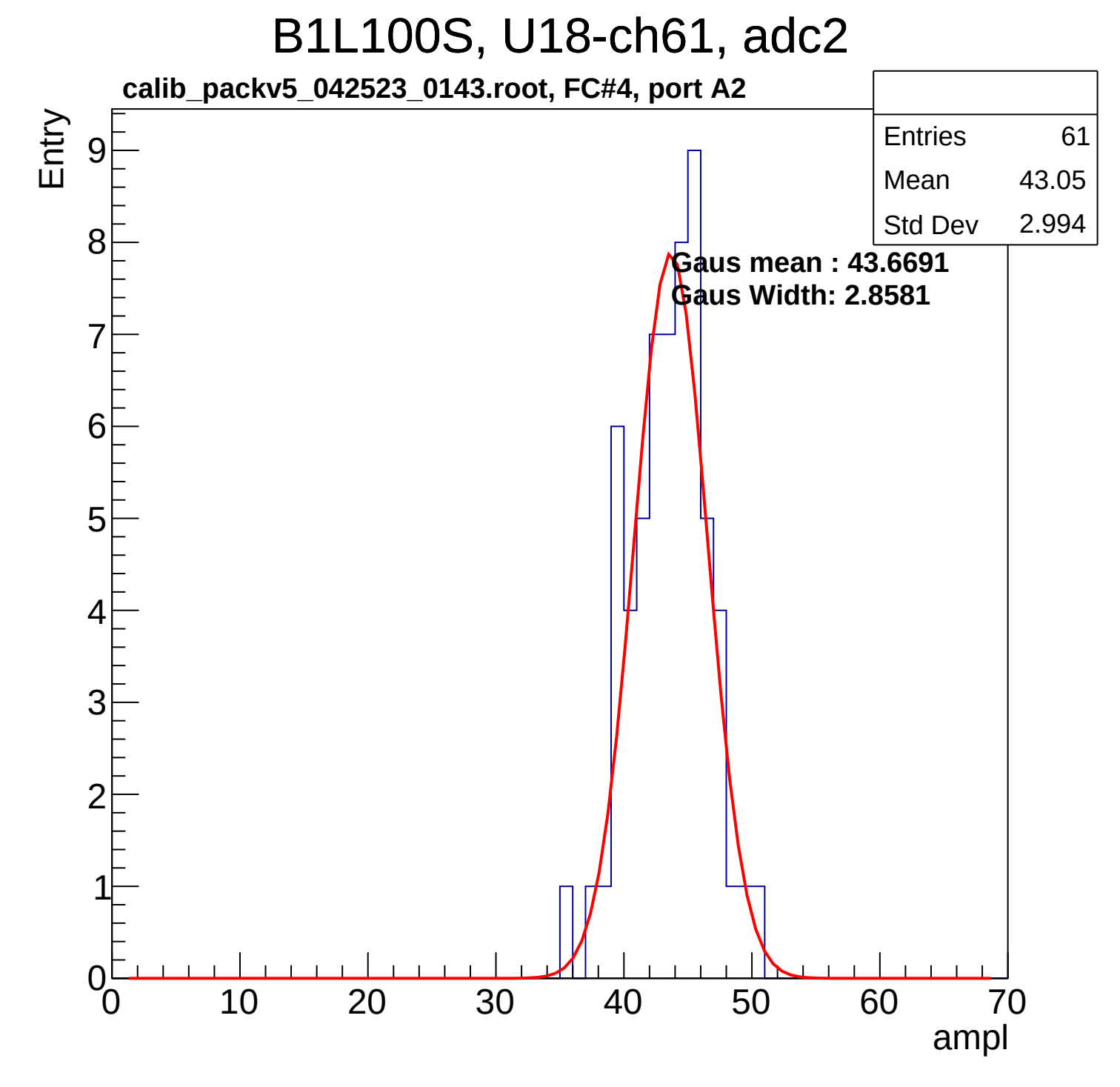

B1L100S, U18-ch60, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 58.47
Std Dev 8.511
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

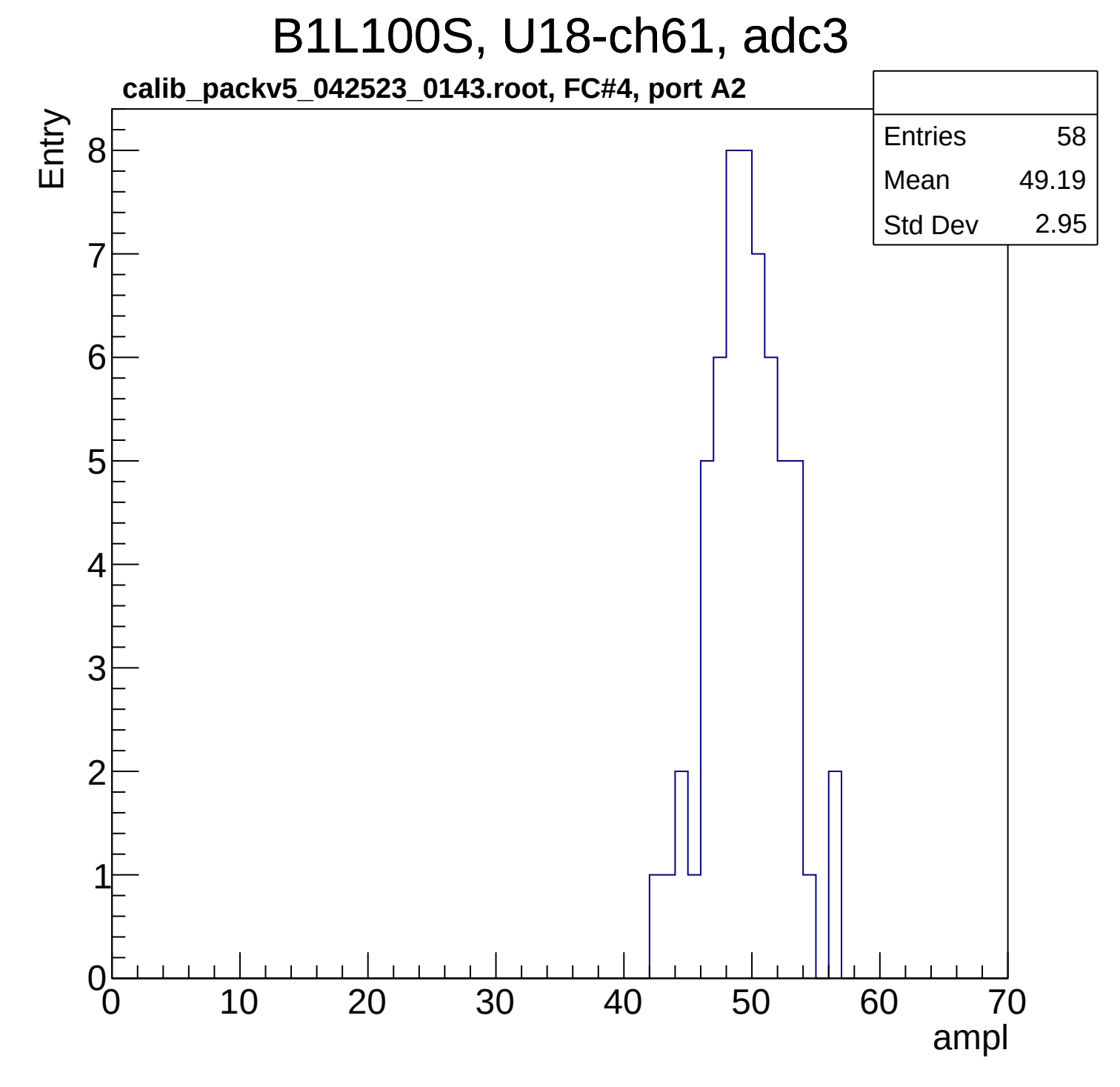

B1L100S, U18-ch60, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 61.83
Std Dev 2.192
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

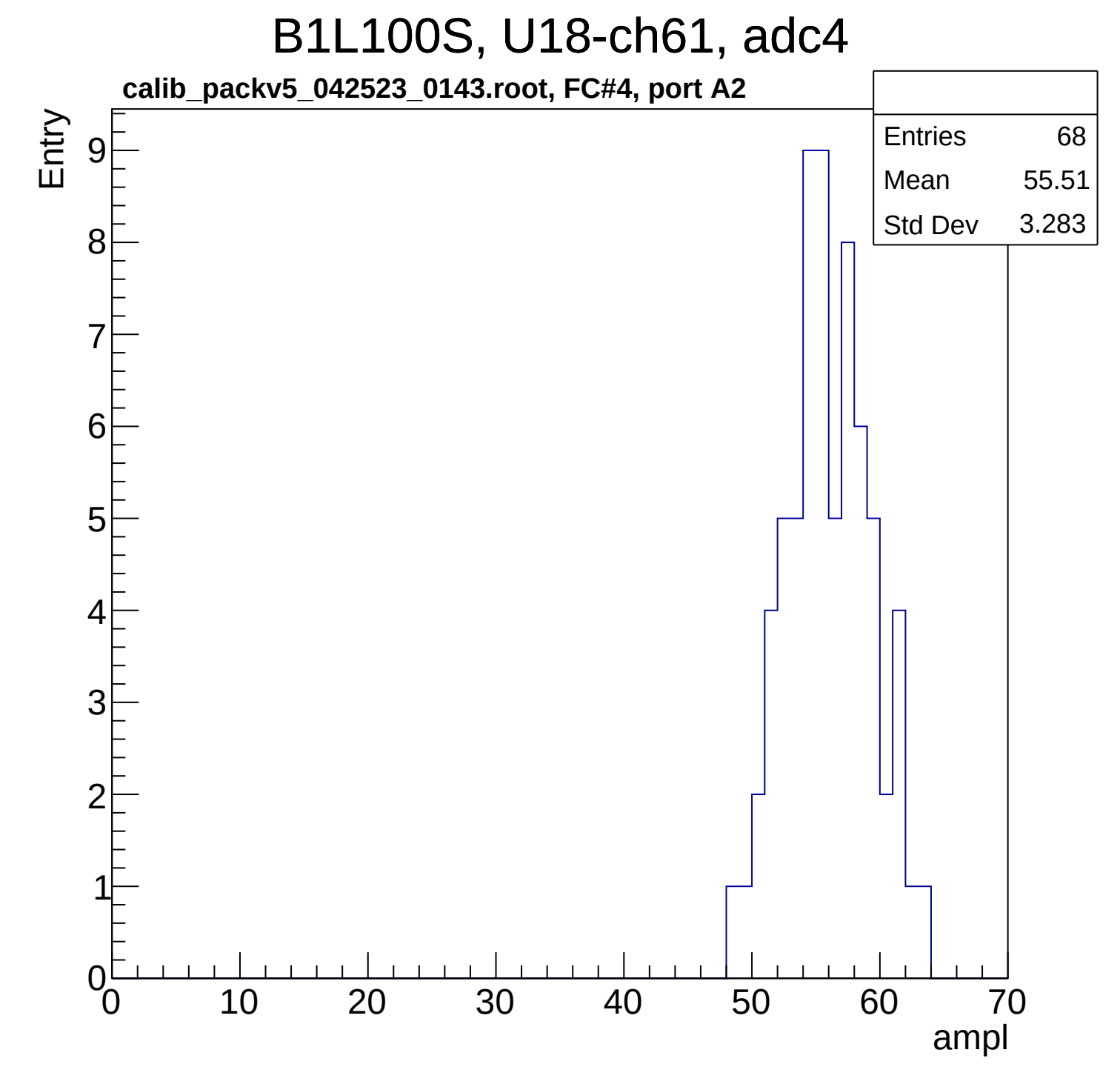

B1L100S, U18-ch60, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

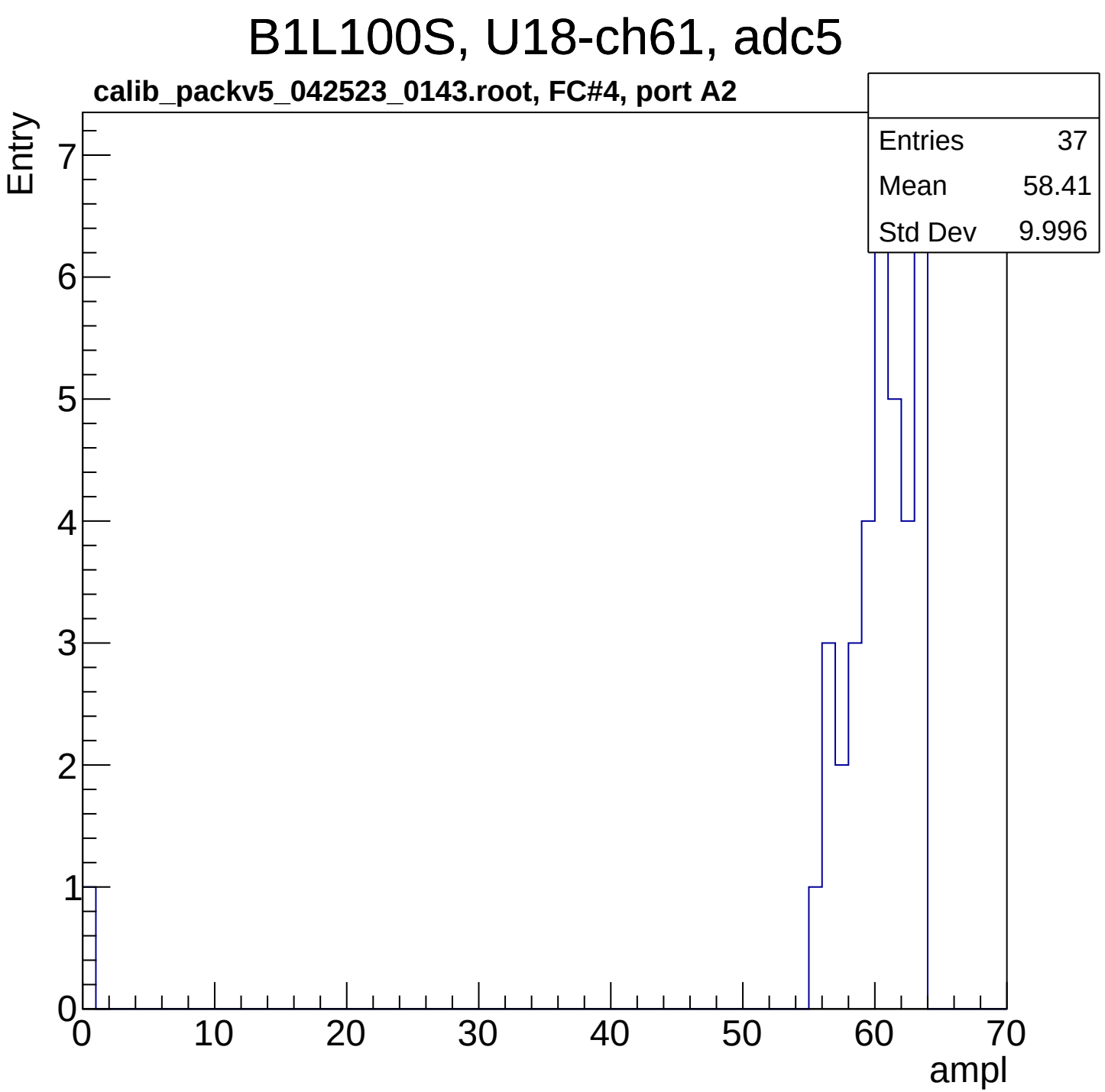

B1L100S, U18-ch61, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 29.84
Std Dev 5.748
Gaus mean : 30.8786
Gaus Width: 3.5043
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

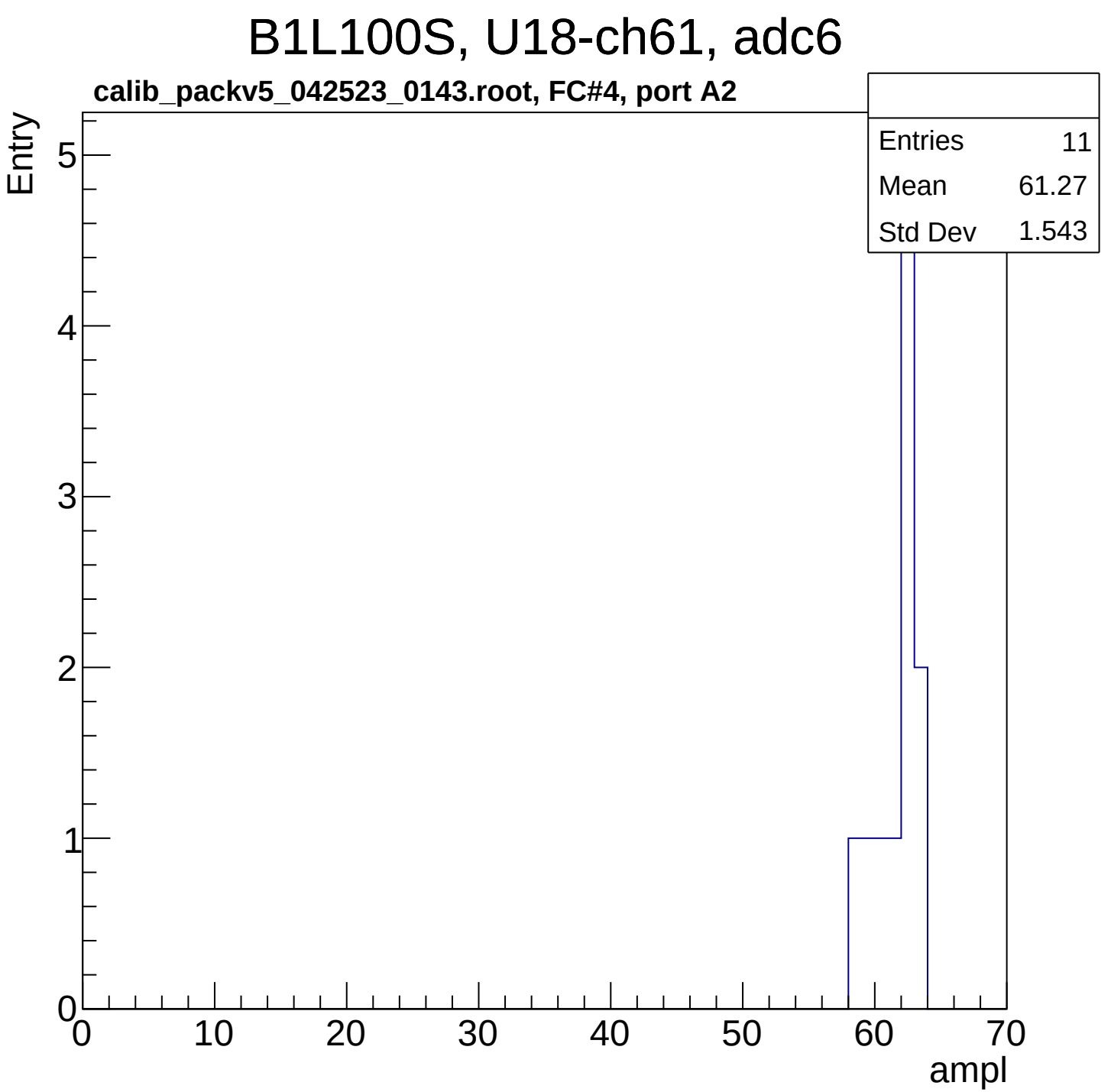

B1L100S, U18-ch61, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 36.53
Std Dev 5.581
Gaus mean : 37.6151
Gaus Width: 3.5076
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

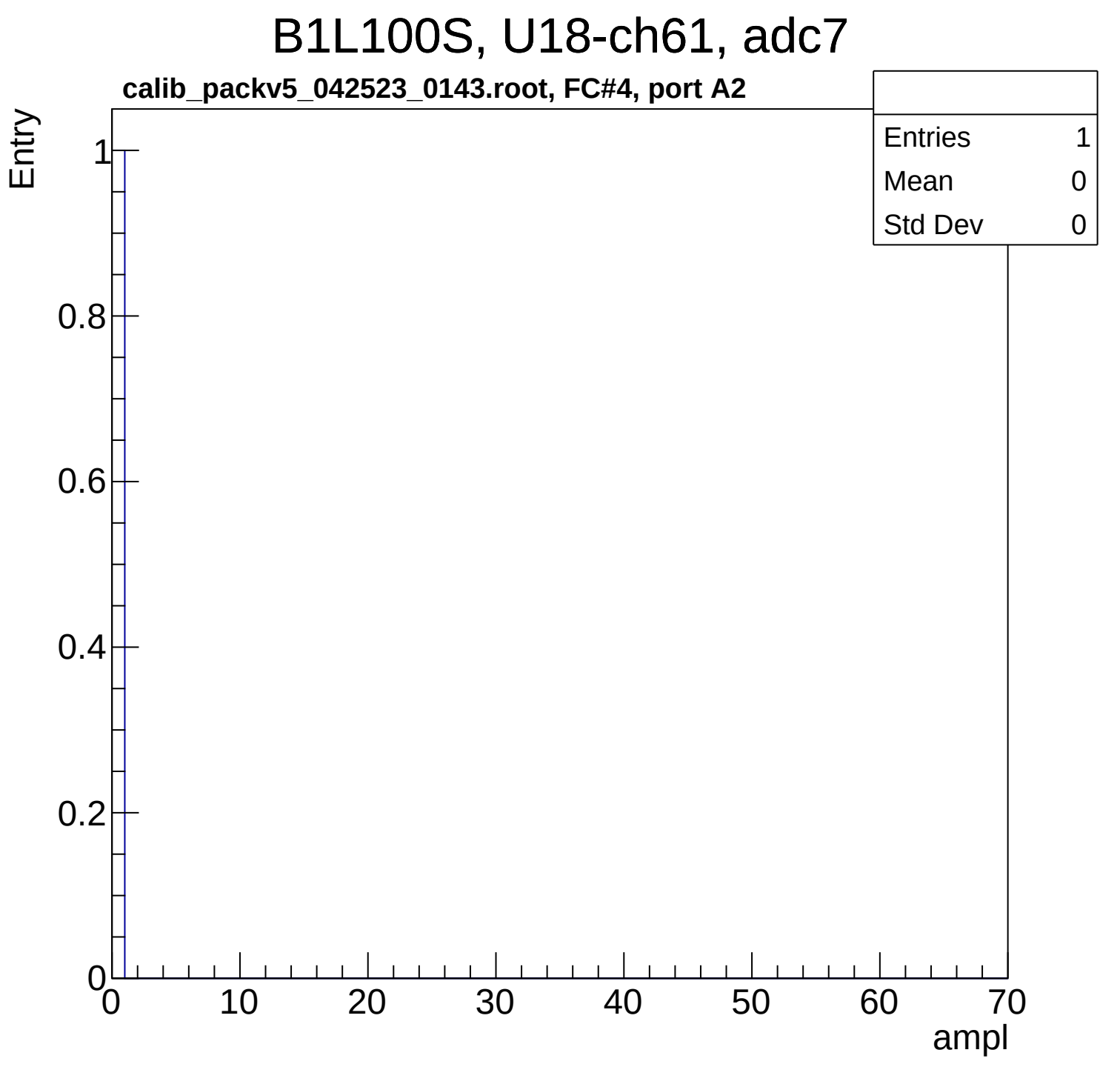

B1L100S, U18-ch61, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 43.05
Std Dev 2.994
Gaus mean : 43.6691
Gaus Width: 2.8581
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

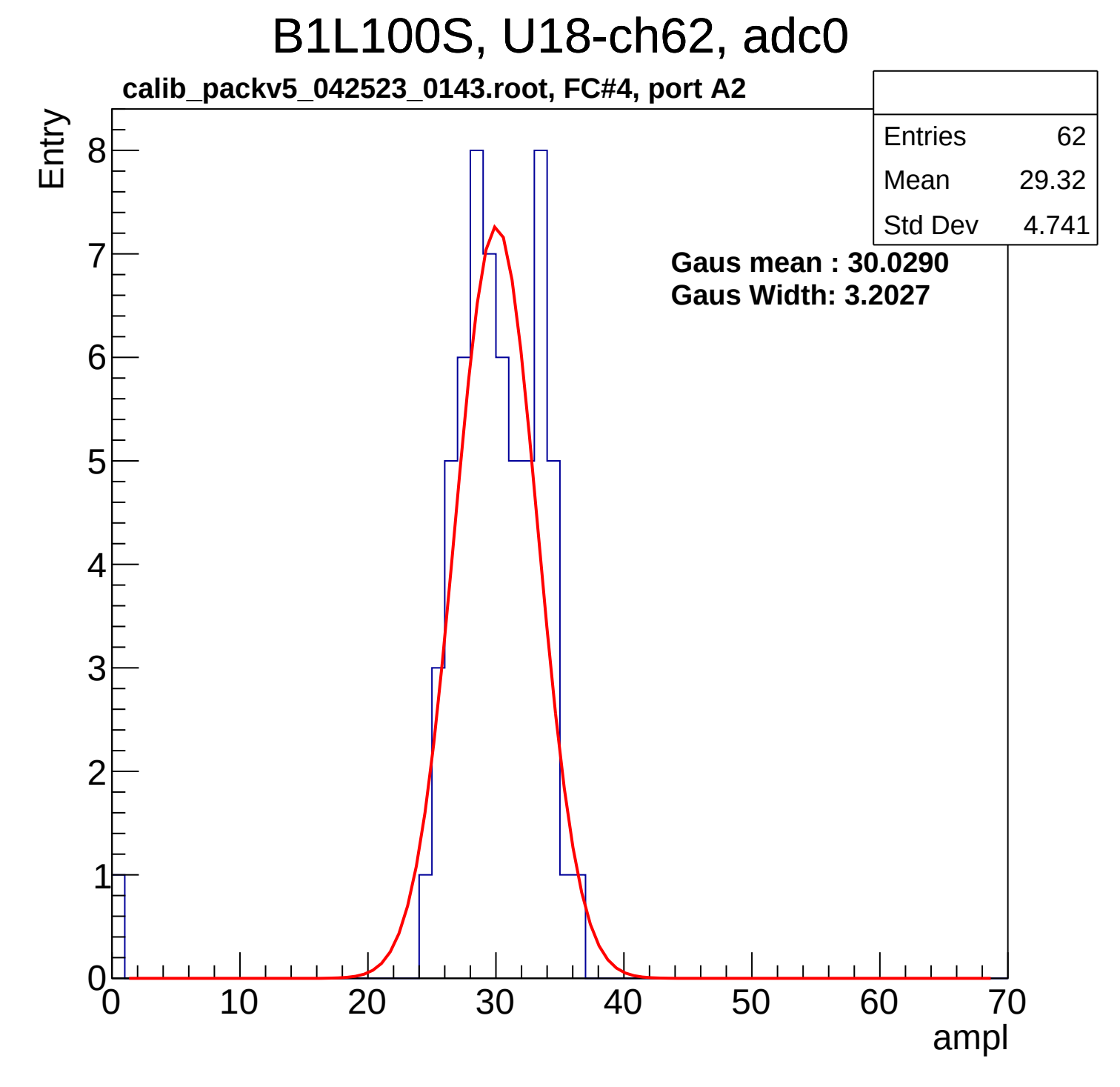

B1L100S, U18-ch61, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 49.19
Std Dev 2.95
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

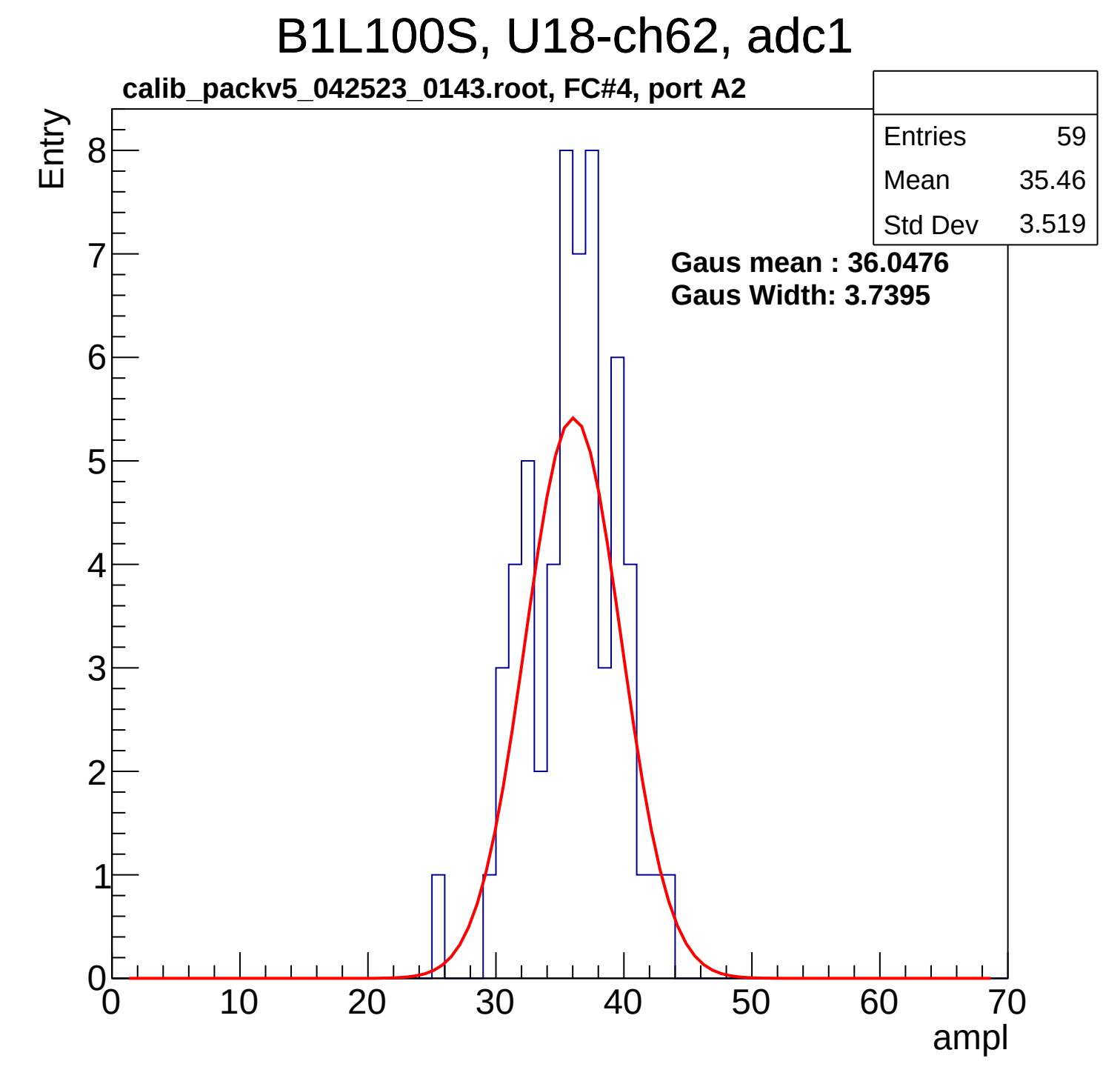

B1L100S, U18-ch61, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 55.51
Std Dev 3.283
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

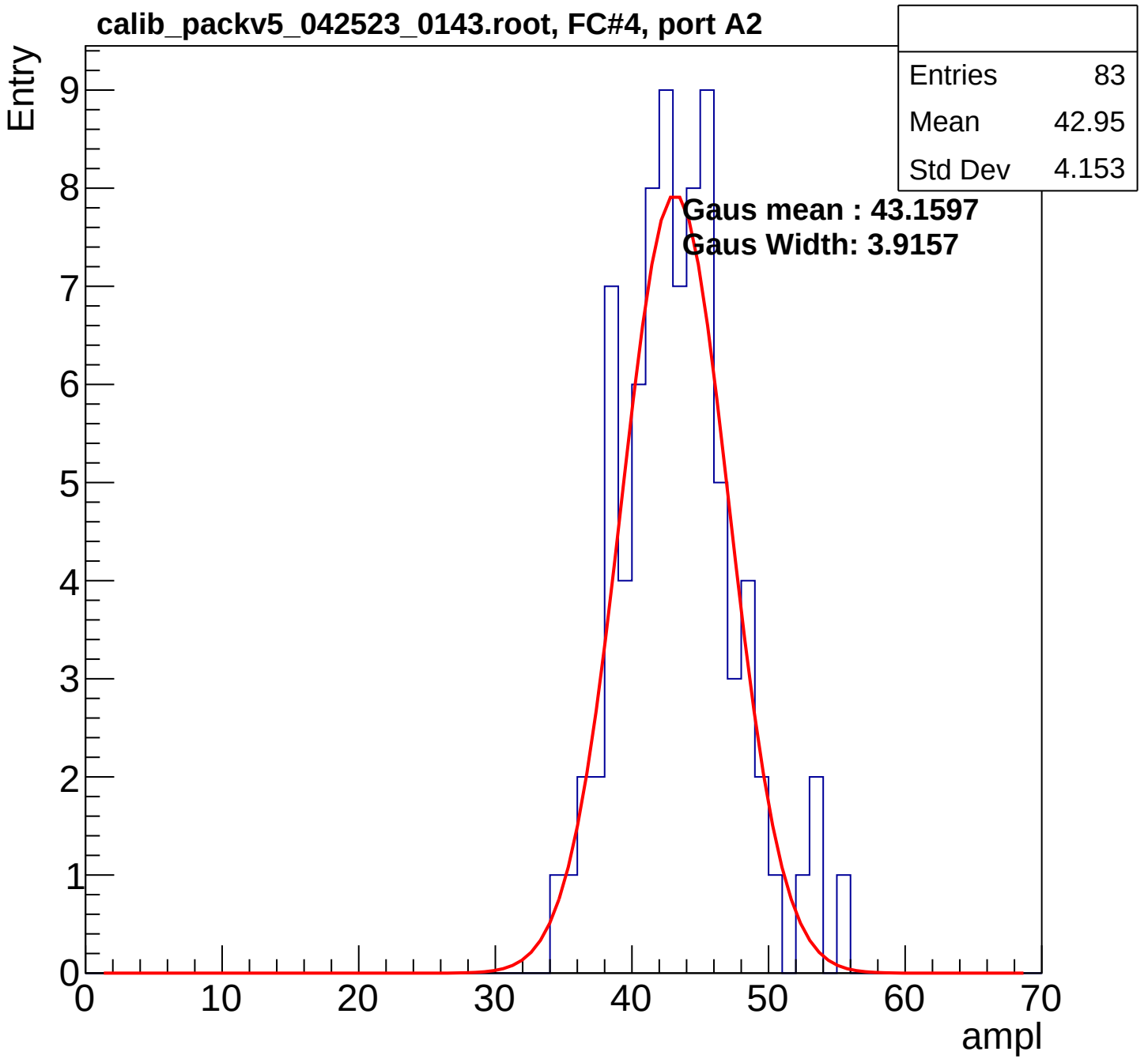

B1L100S, U18-ch61, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 37
Mean 58.41
Std Dev 9.996
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

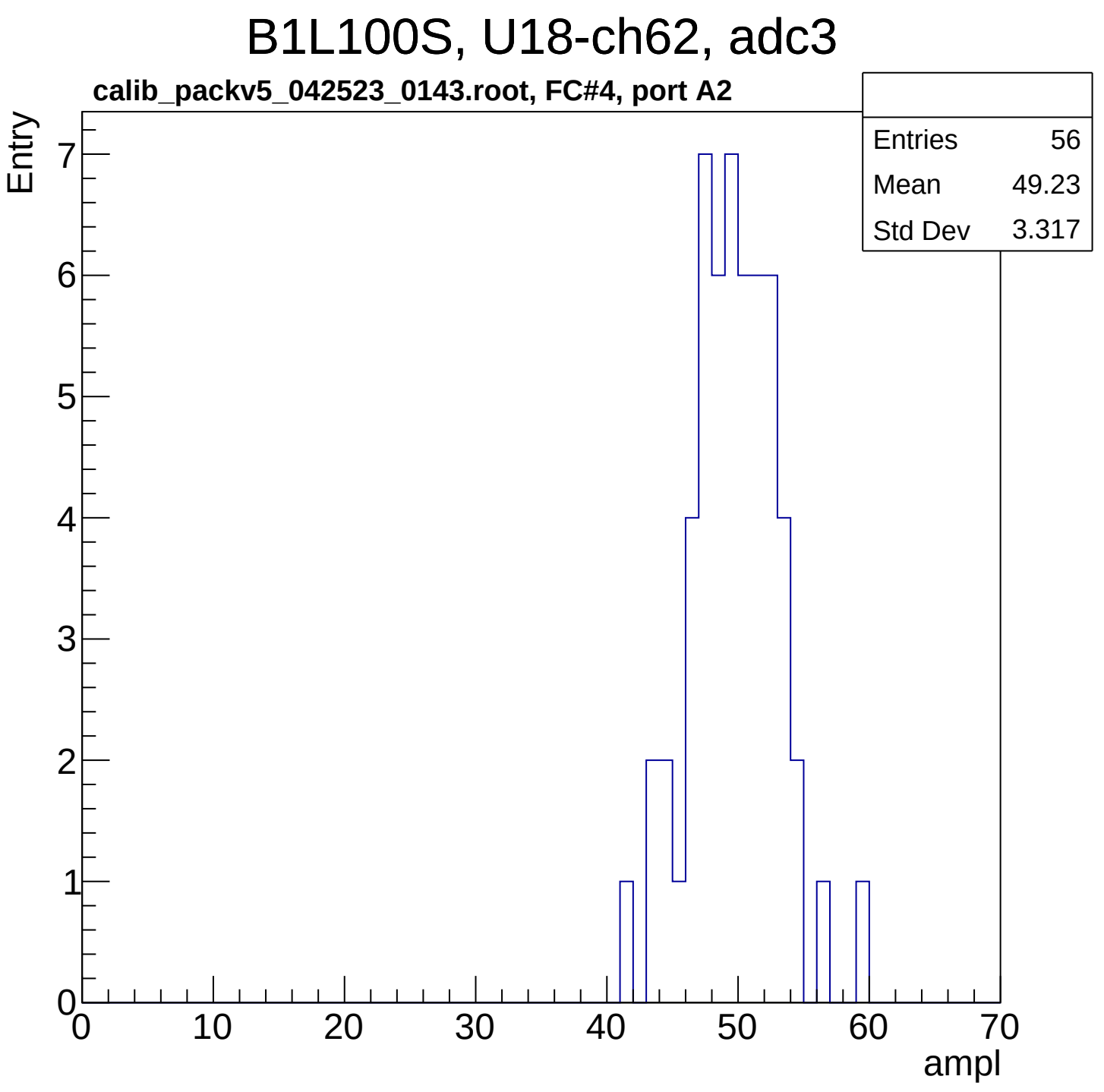

B1L100S, U18-ch61, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 61.27
Std Dev 1.543
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

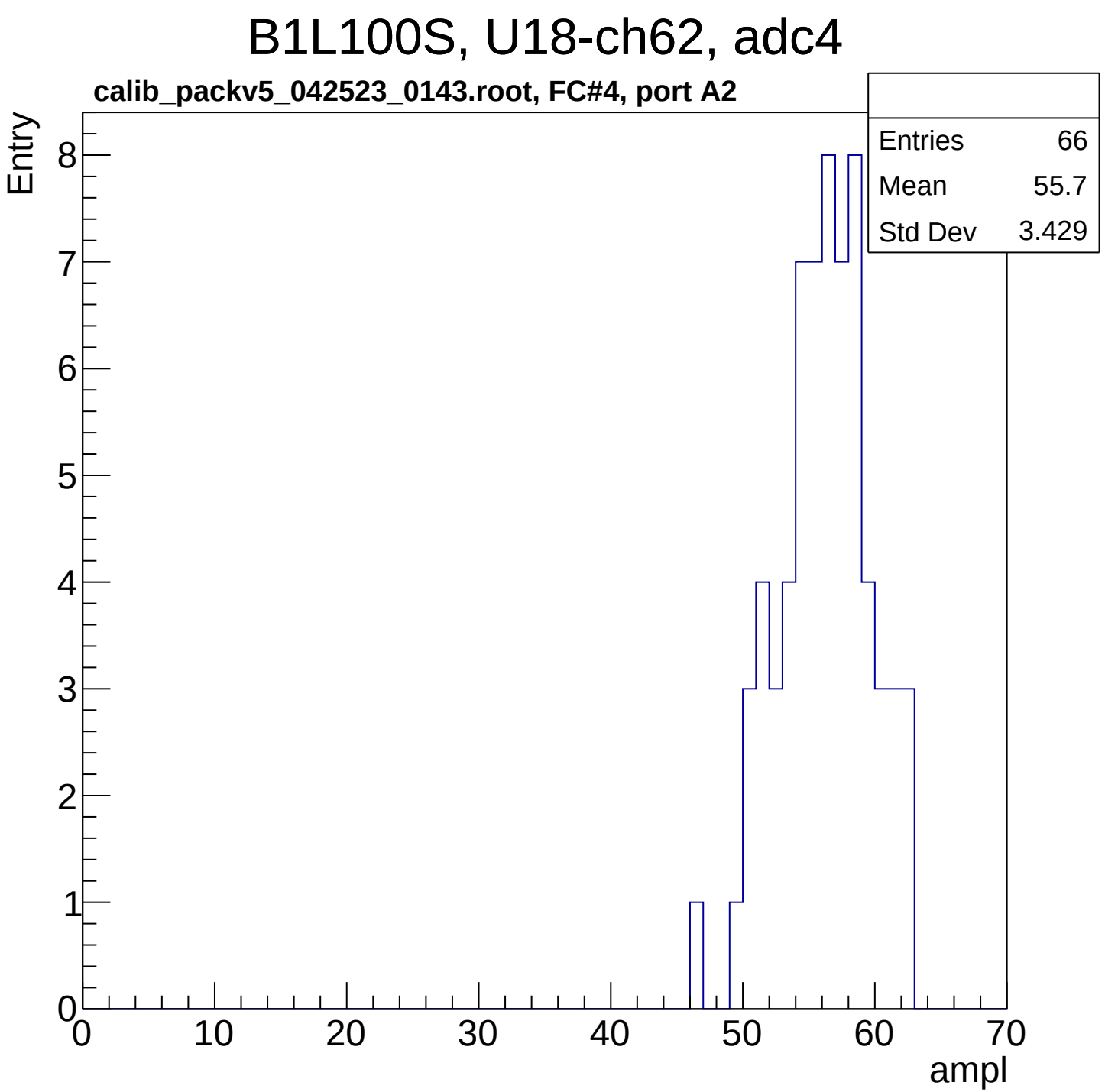

B1L100S, U18-ch61, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

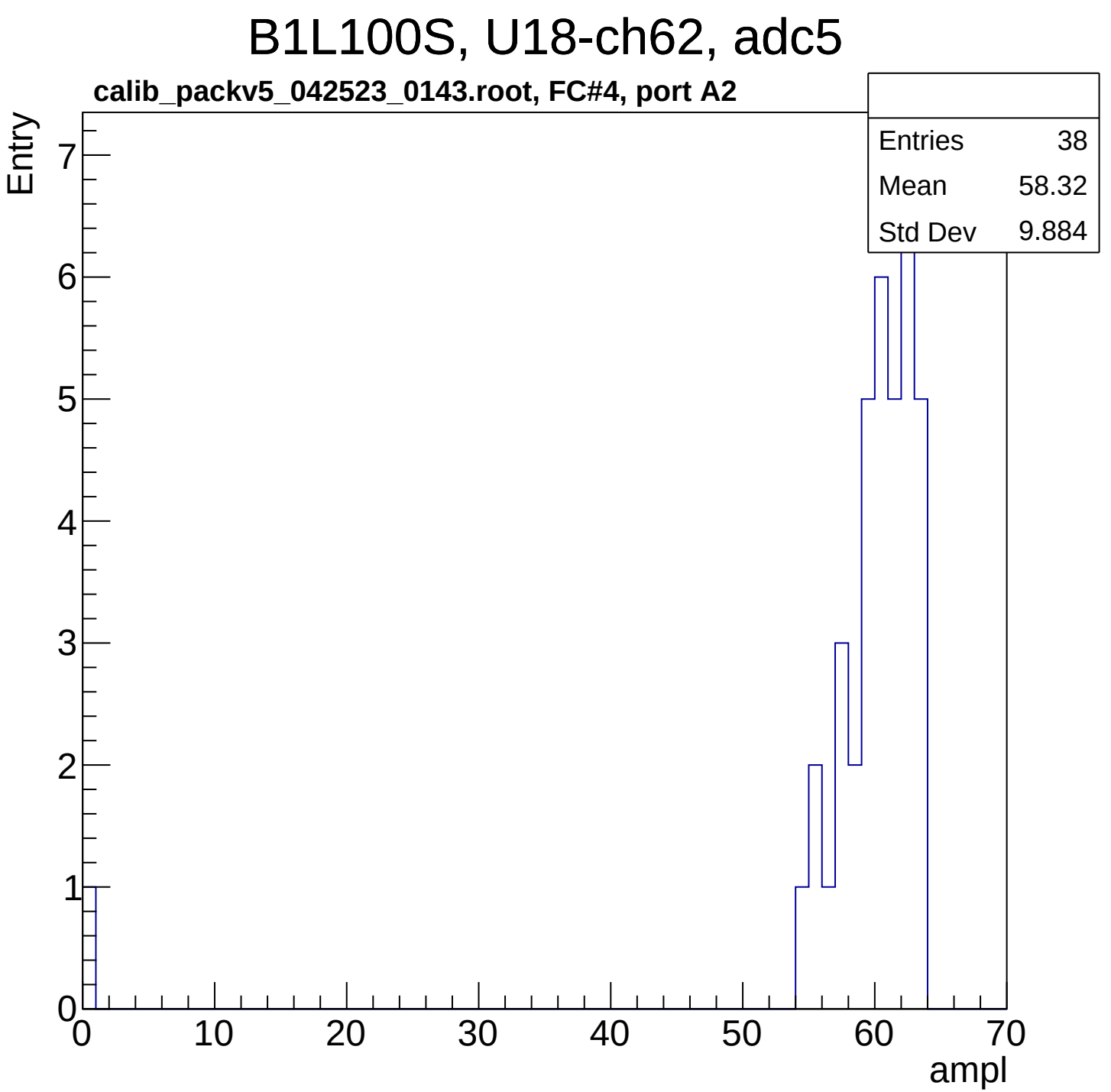

B1L100S, U18-ch62, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 29.32
Std Dev 4.741
Gaus mean : 30.0290
Gaus Width: 3.2027
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

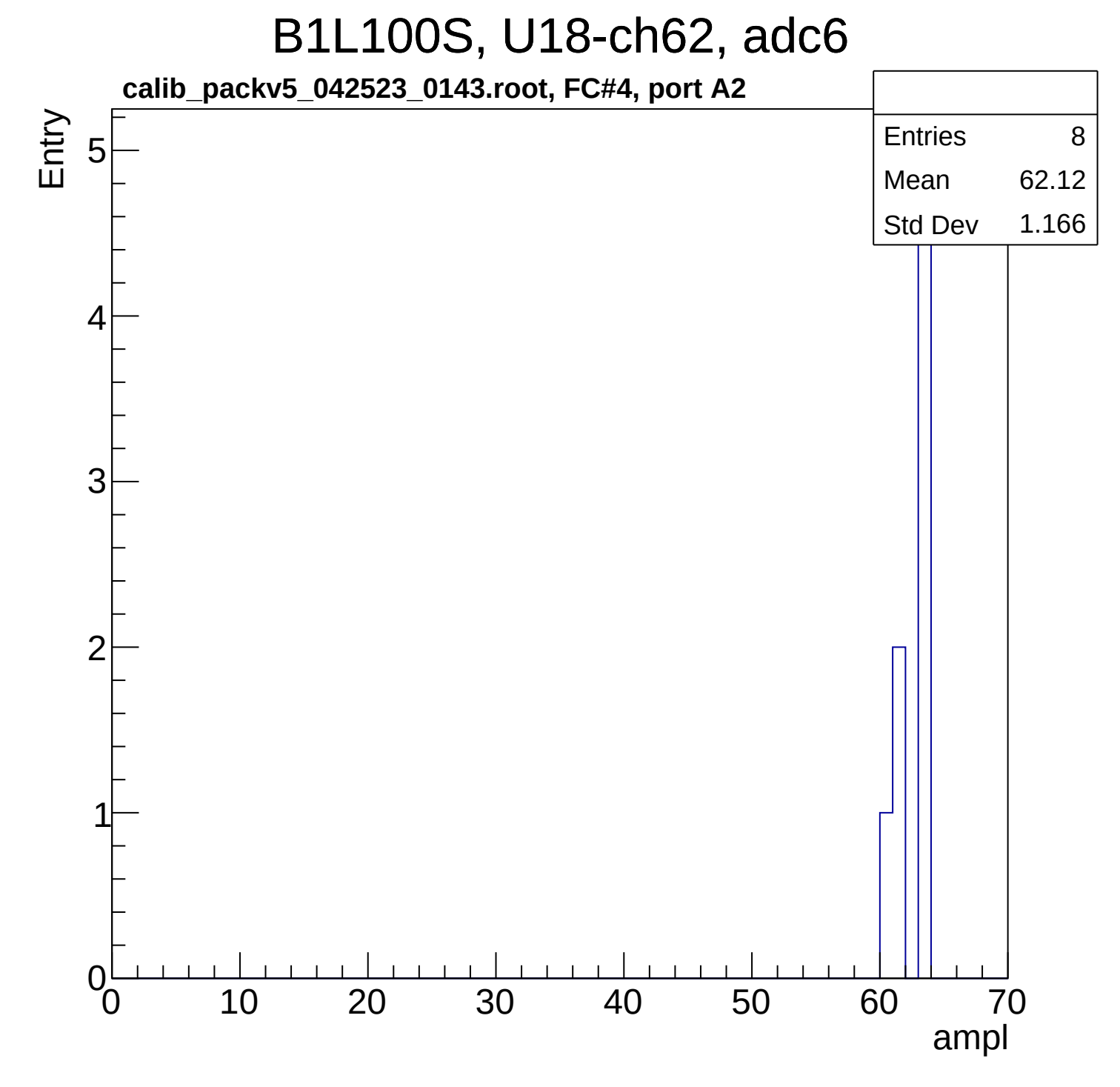

B1L100S, U18-ch62, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 35.46
Std Dev 3.519
Gaus mean : 36.0476
Gaus Width: 3.7395
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

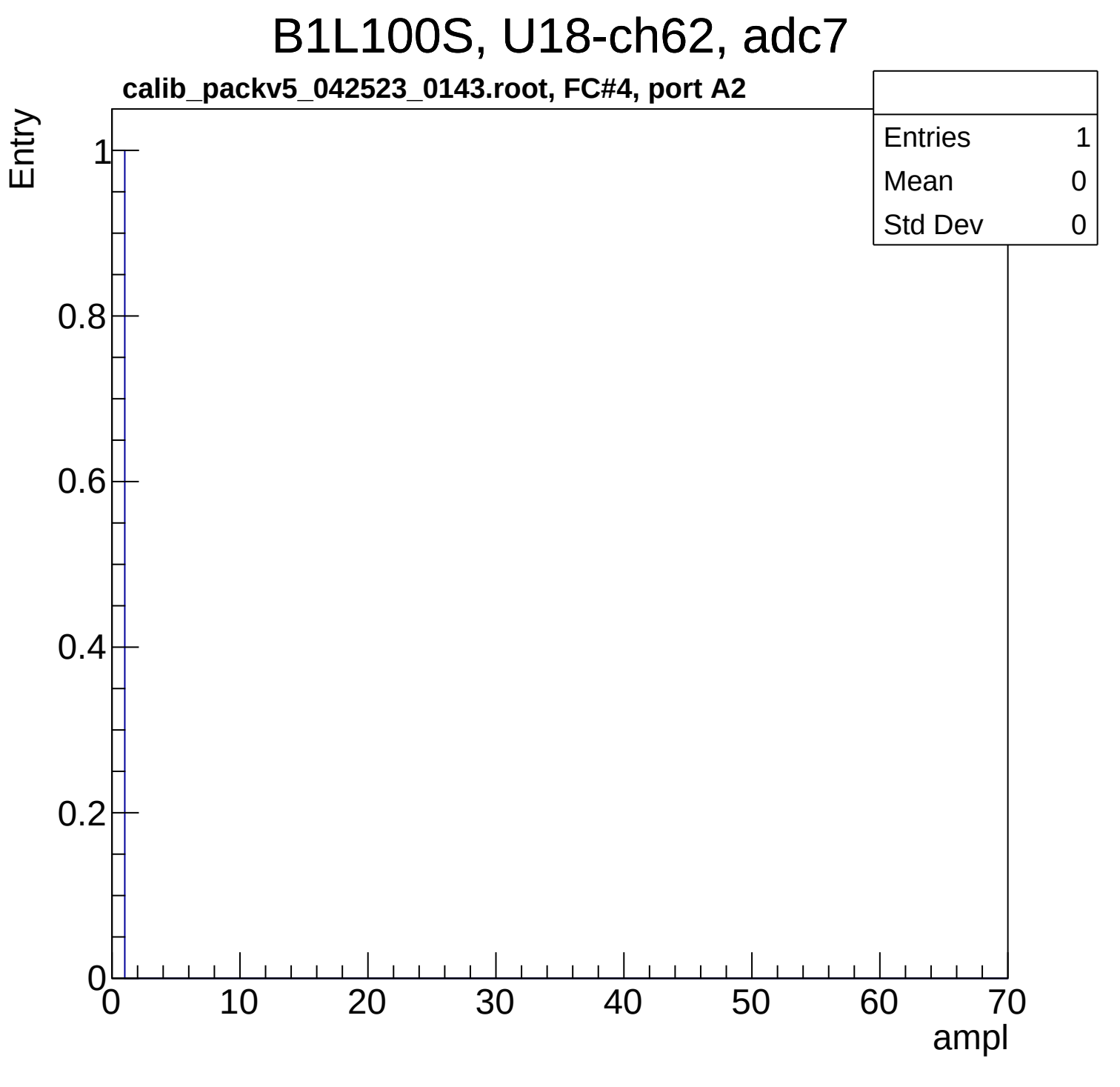

B1L100S, U18-ch62, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 83
Mean 42.95
Std Dev 4.153
Gaus mean : 43.1597
Gaus Width: 3.9157
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

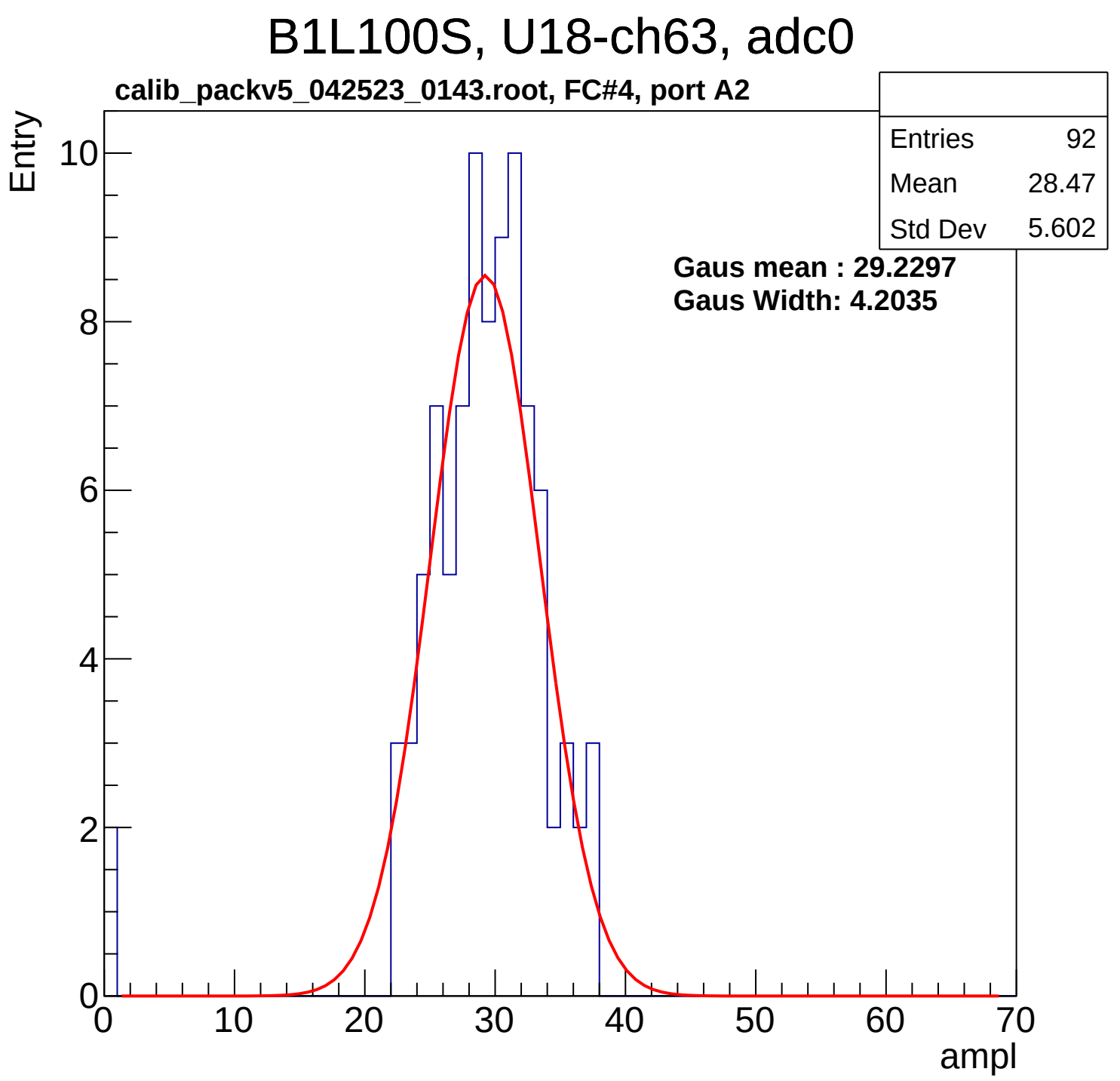

B1L100S, U18-ch62, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 49.23
Std Dev 3.317
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

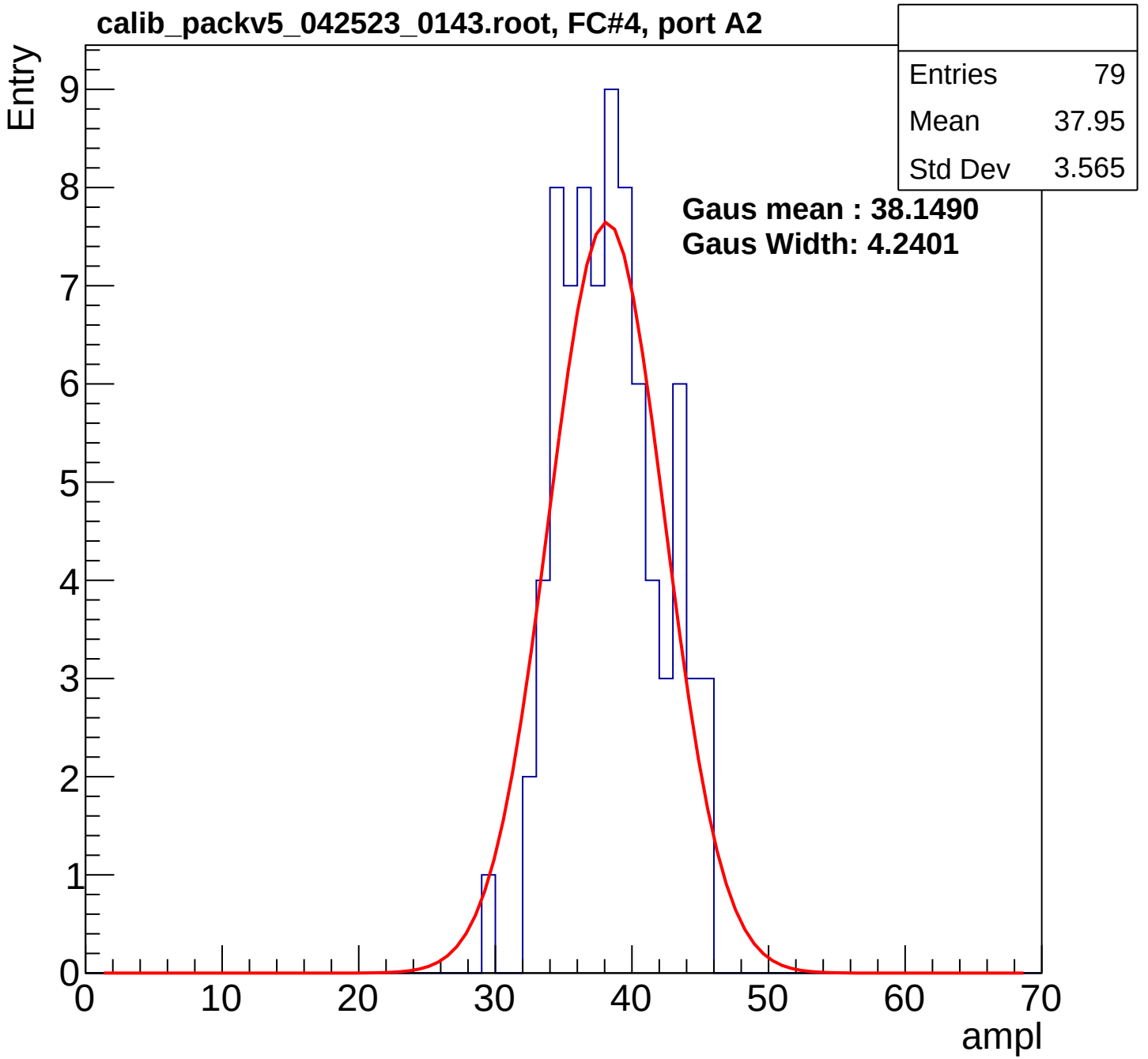

B1L100S, U18-ch62, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 55.7
Std Dev 3.429
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

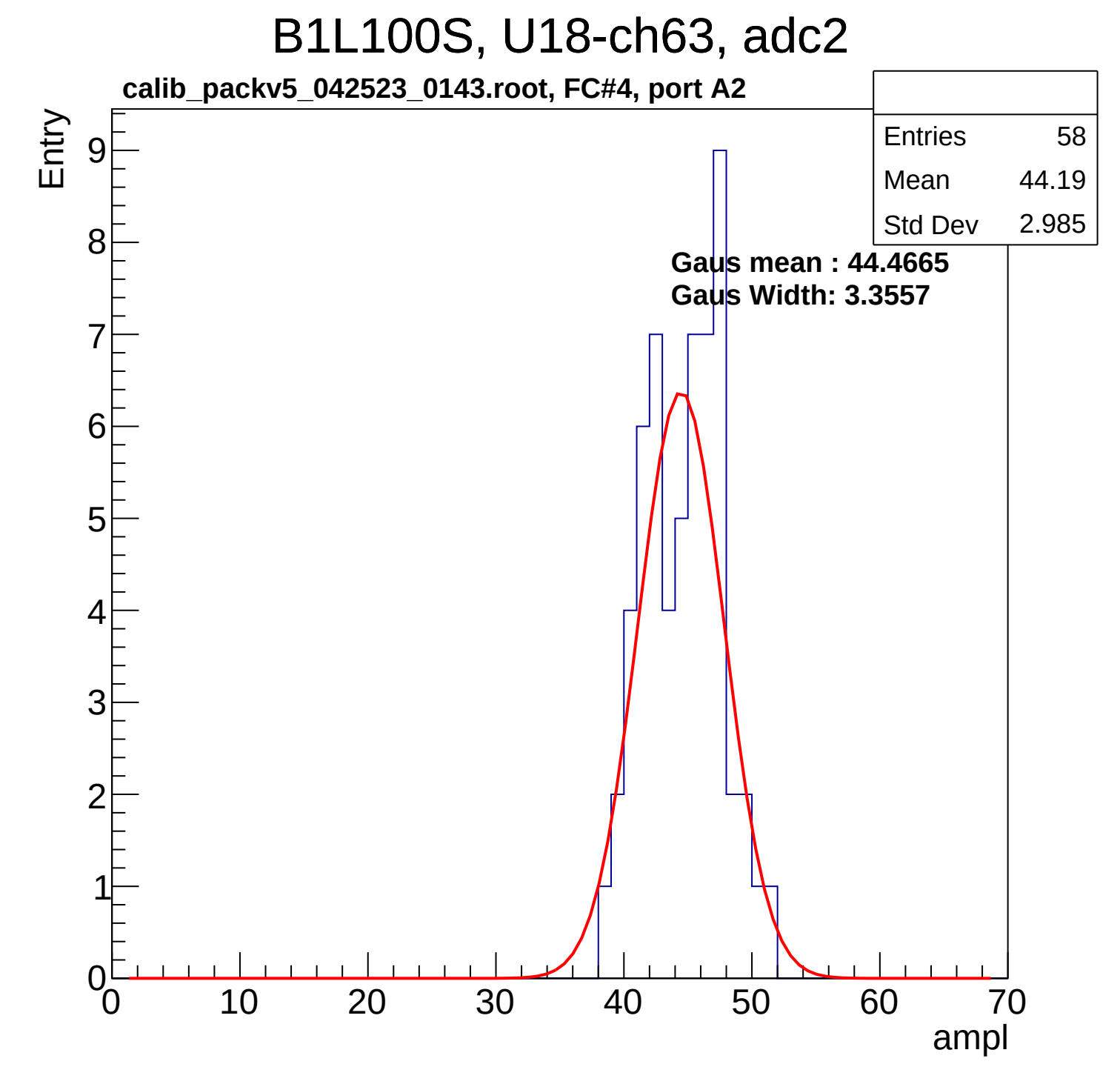

B1L100S, U18-ch62, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 38
Mean 58.32
Std Dev 9.884
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

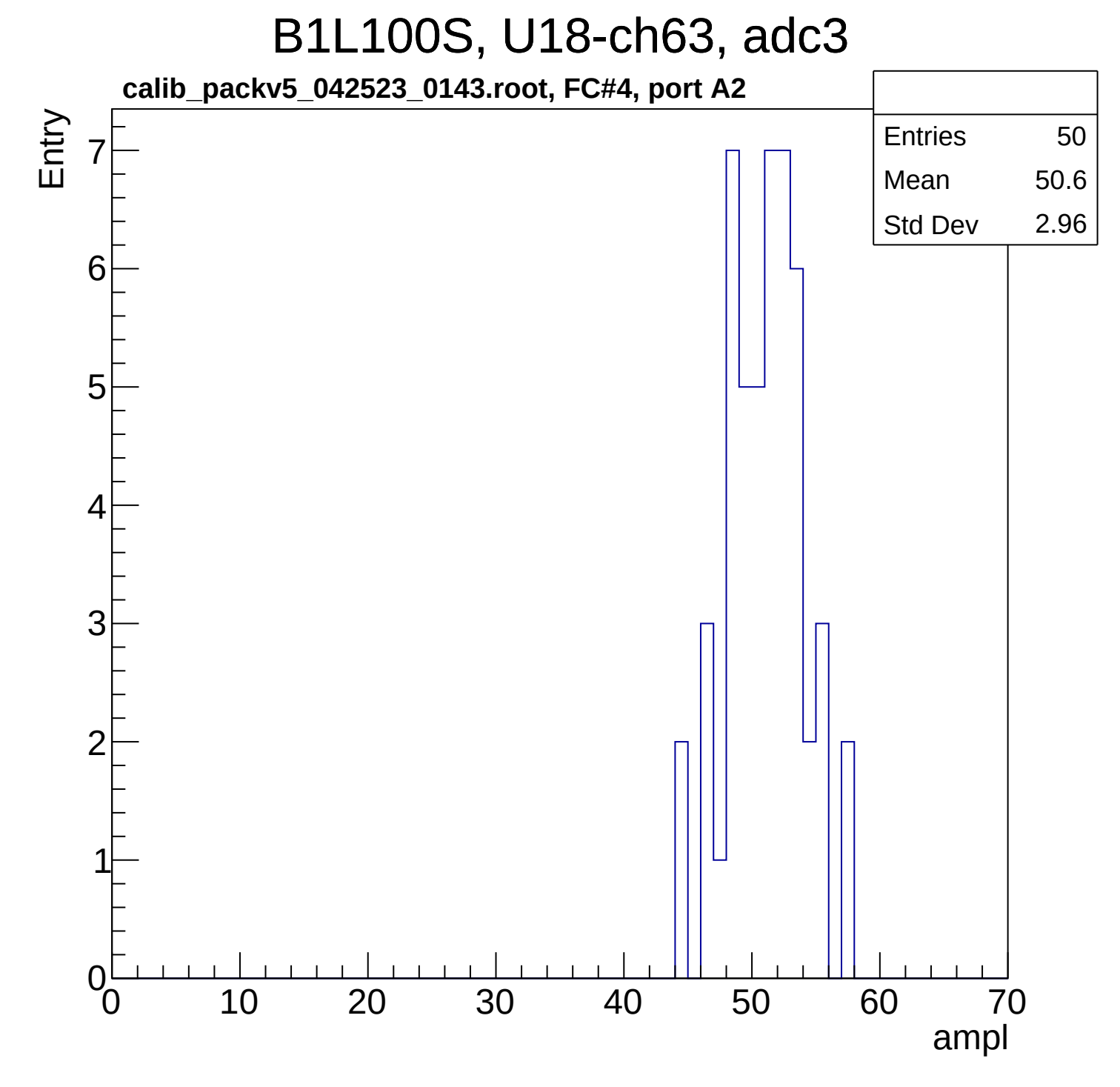

B1L100S, U18-ch62, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 8
Mean 62.12
Std Dev 1.166
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

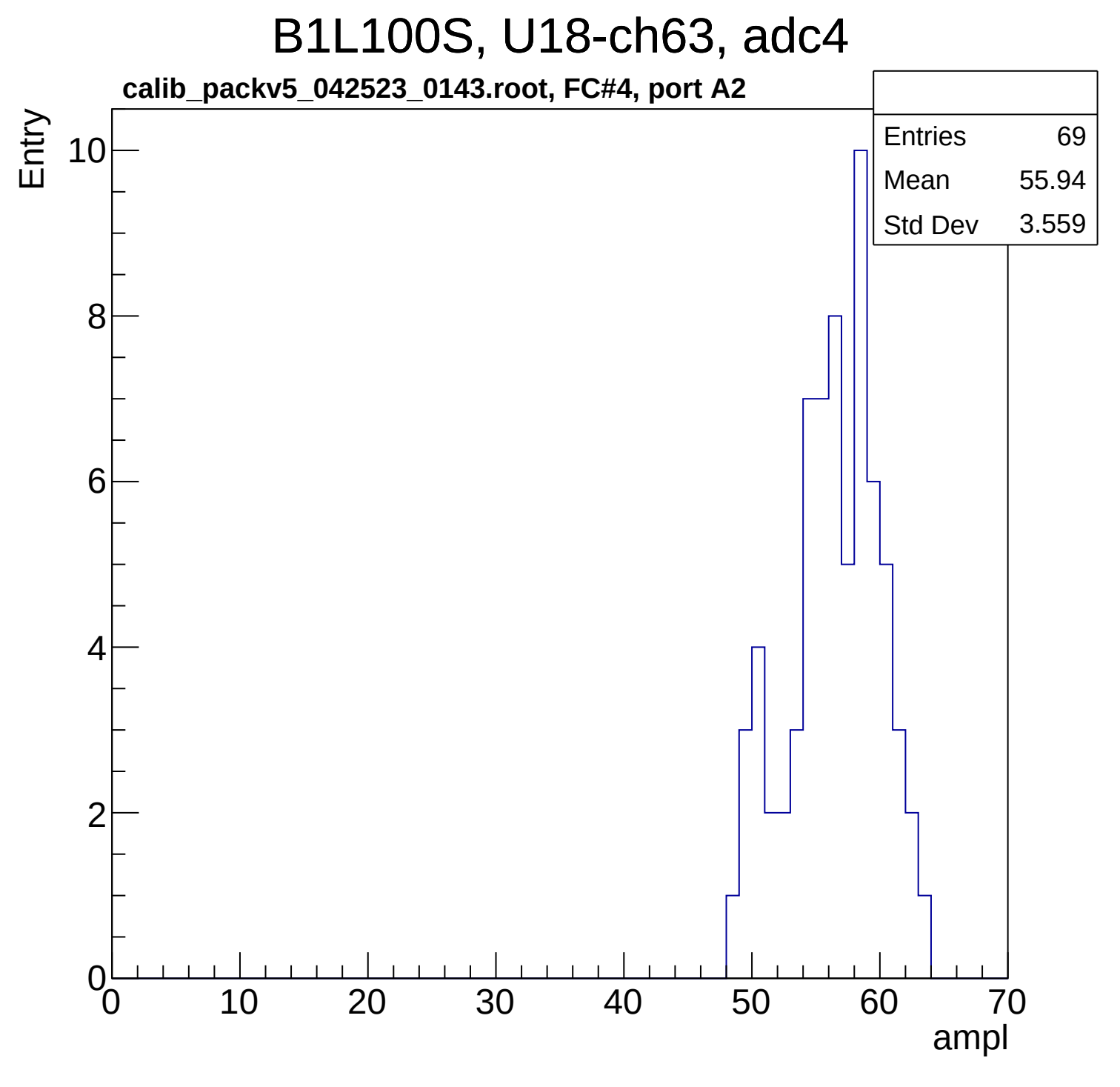

B1L100S, U18-ch62, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

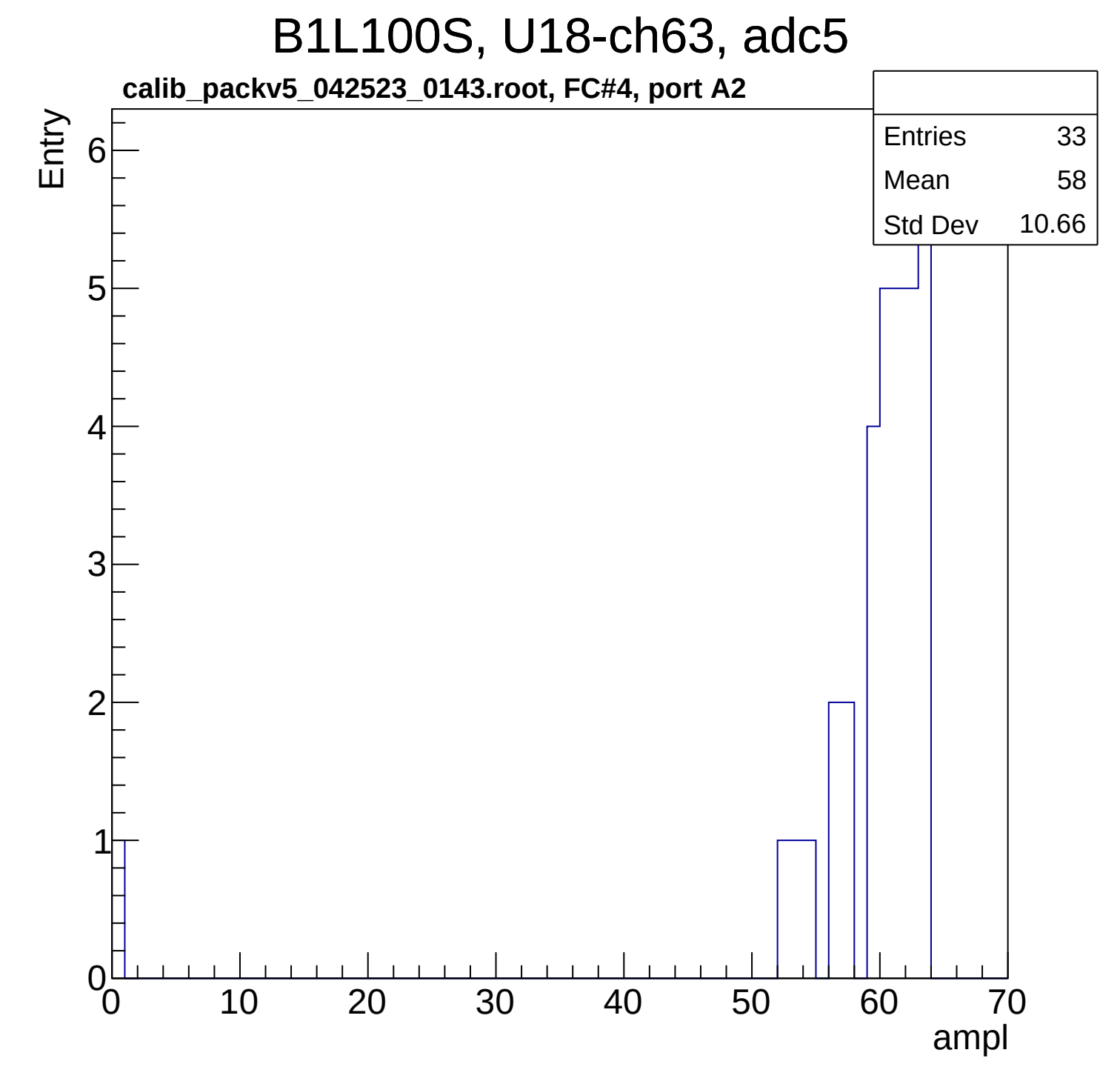

B1L100S, U18-ch63, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 92
Mean 28.47
Std Dev 5.602
Gaus mean : 29.2297
Gaus Width: 4.2035
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

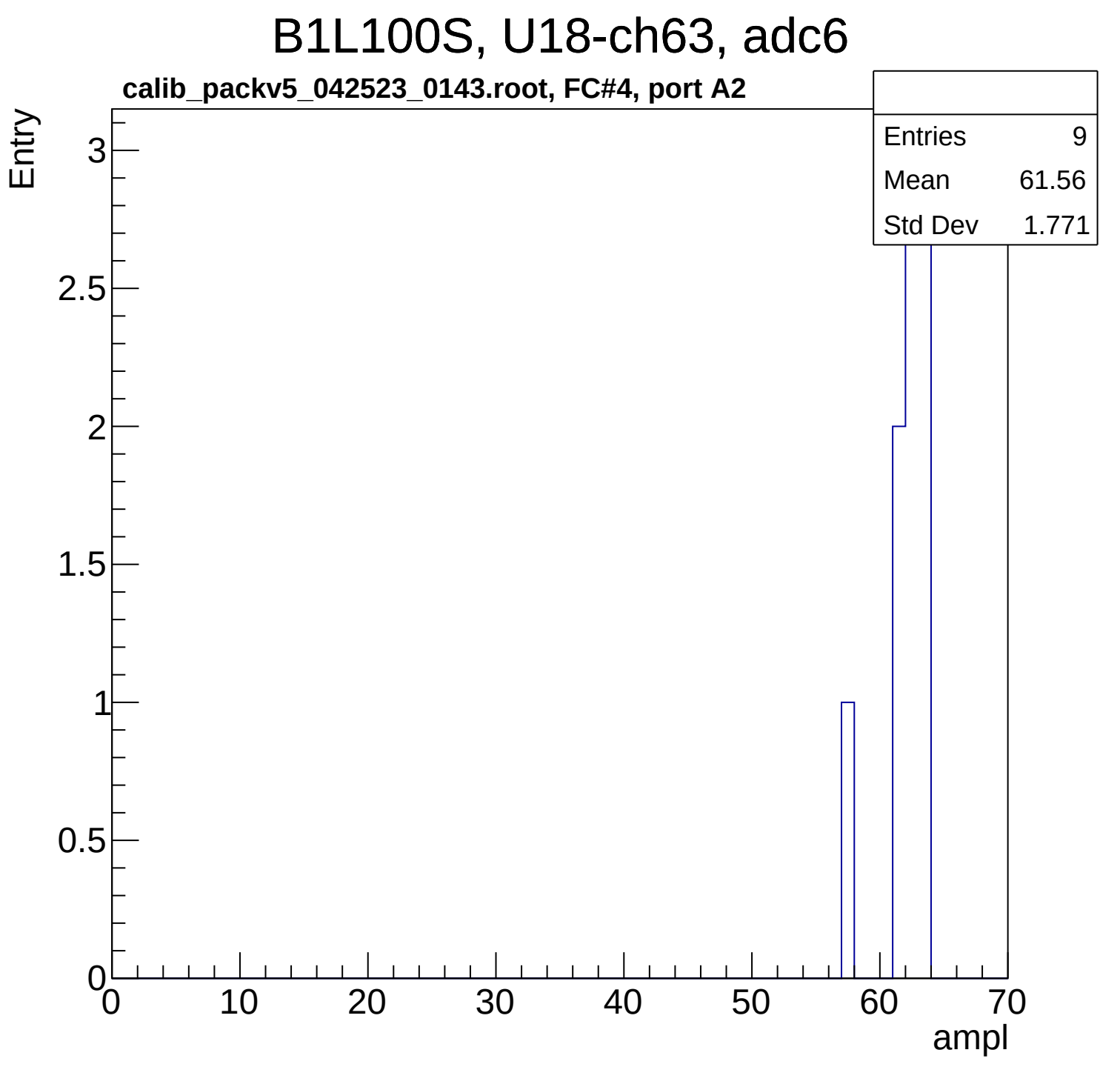

B1L100S, U18-ch63, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 37.95
Std Dev 3.565
Gaus mean : 38.1490
Gaus Width: 4.2401
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

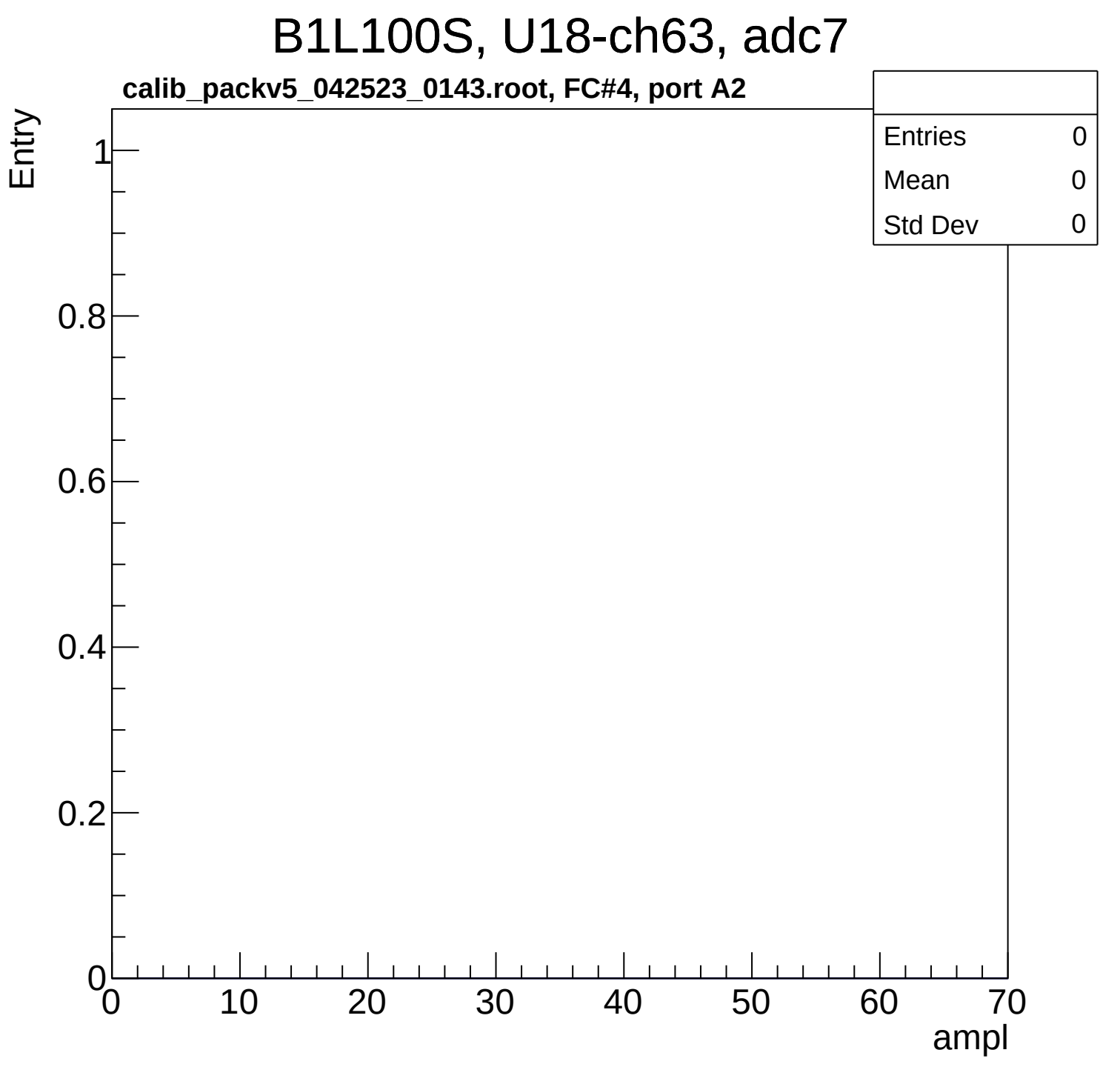

B1L100S, U18-ch63, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 44.19
Std Dev 2.985
Gaus mean : 44.4665
Gaus Width: 3.3557
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

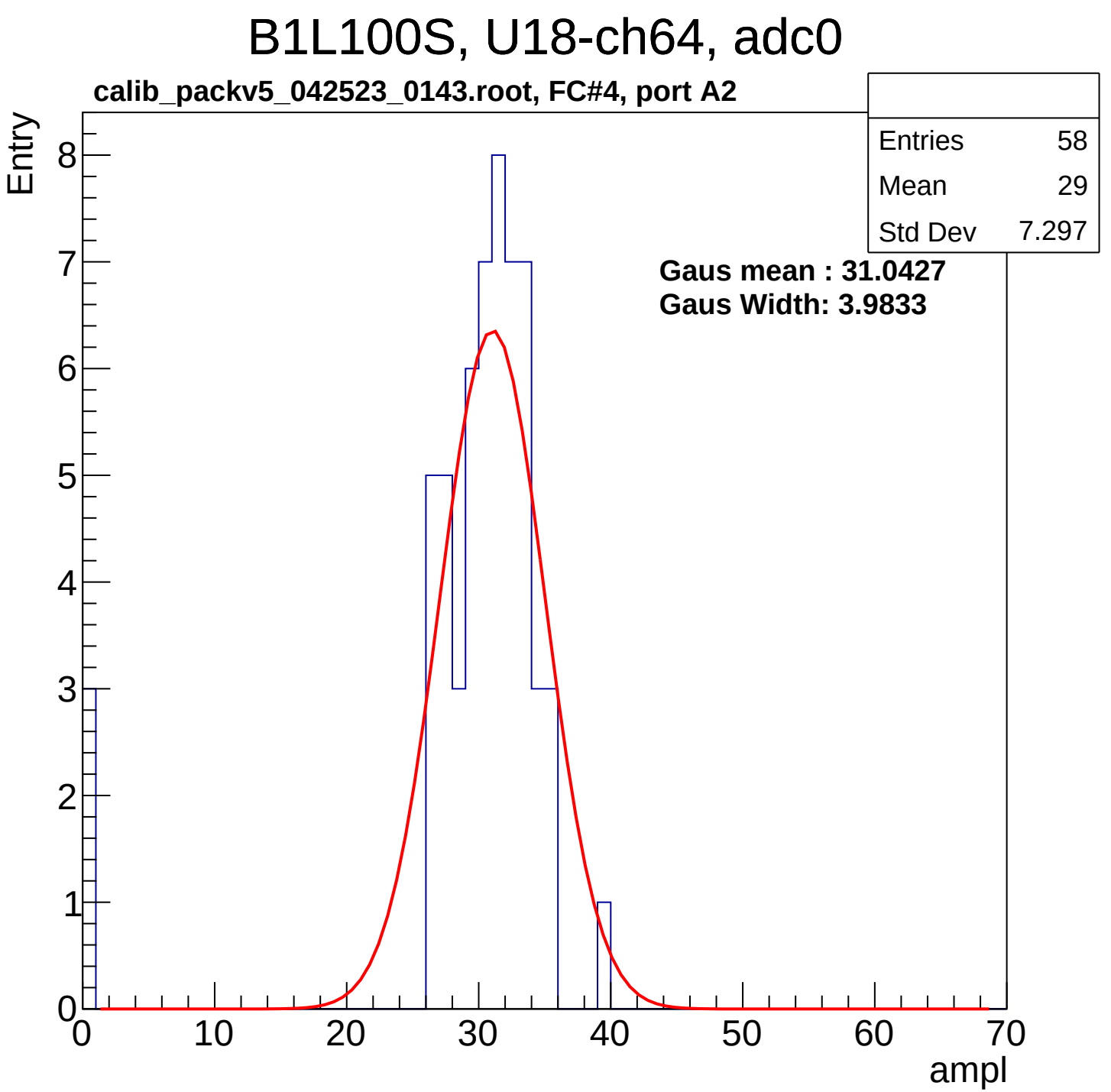

B1L100S, U18-ch63, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 50.6
Std Dev 2.96
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

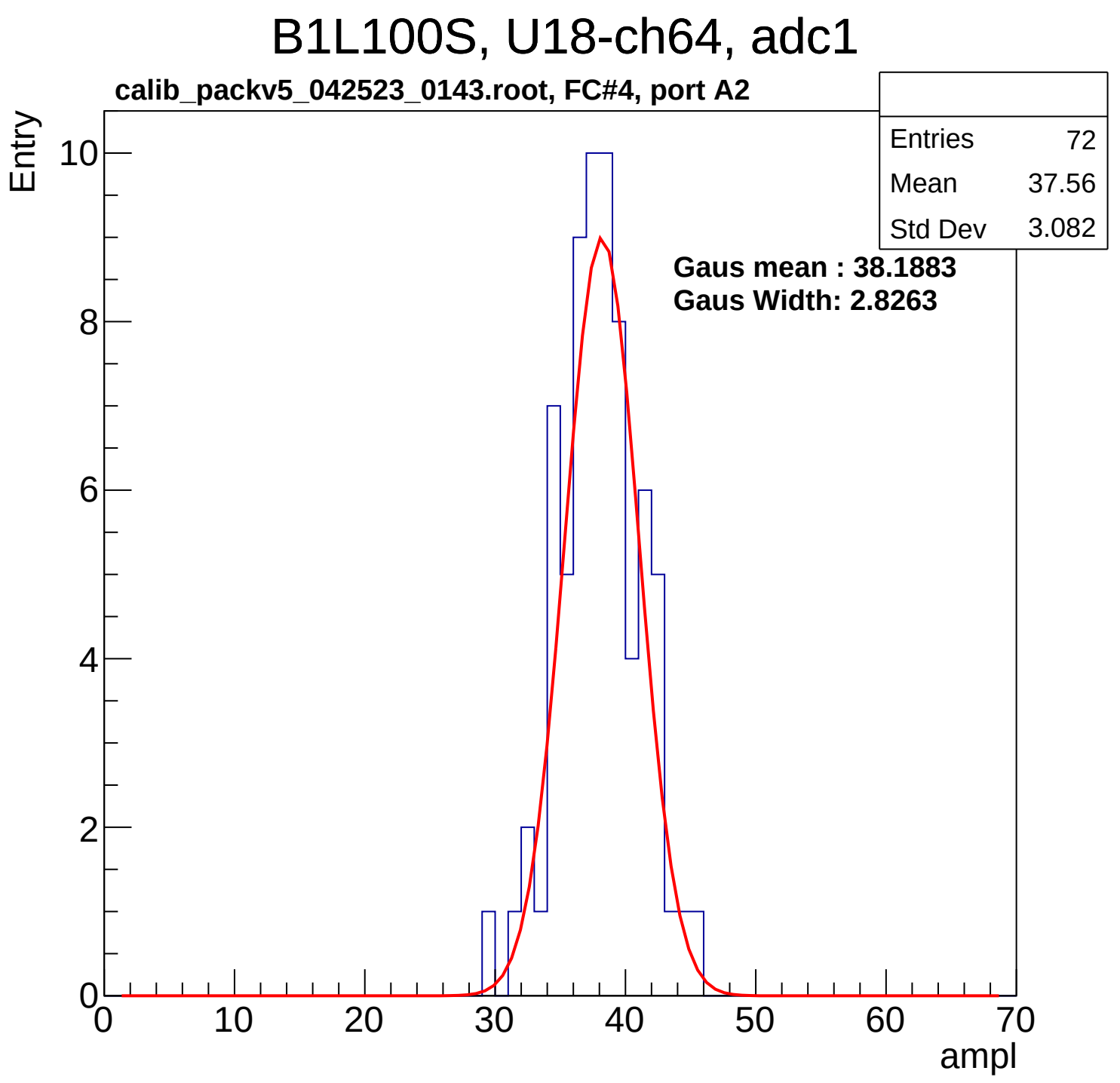

B1L100S, U18-ch63, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 55.94
Std Dev 3.559
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

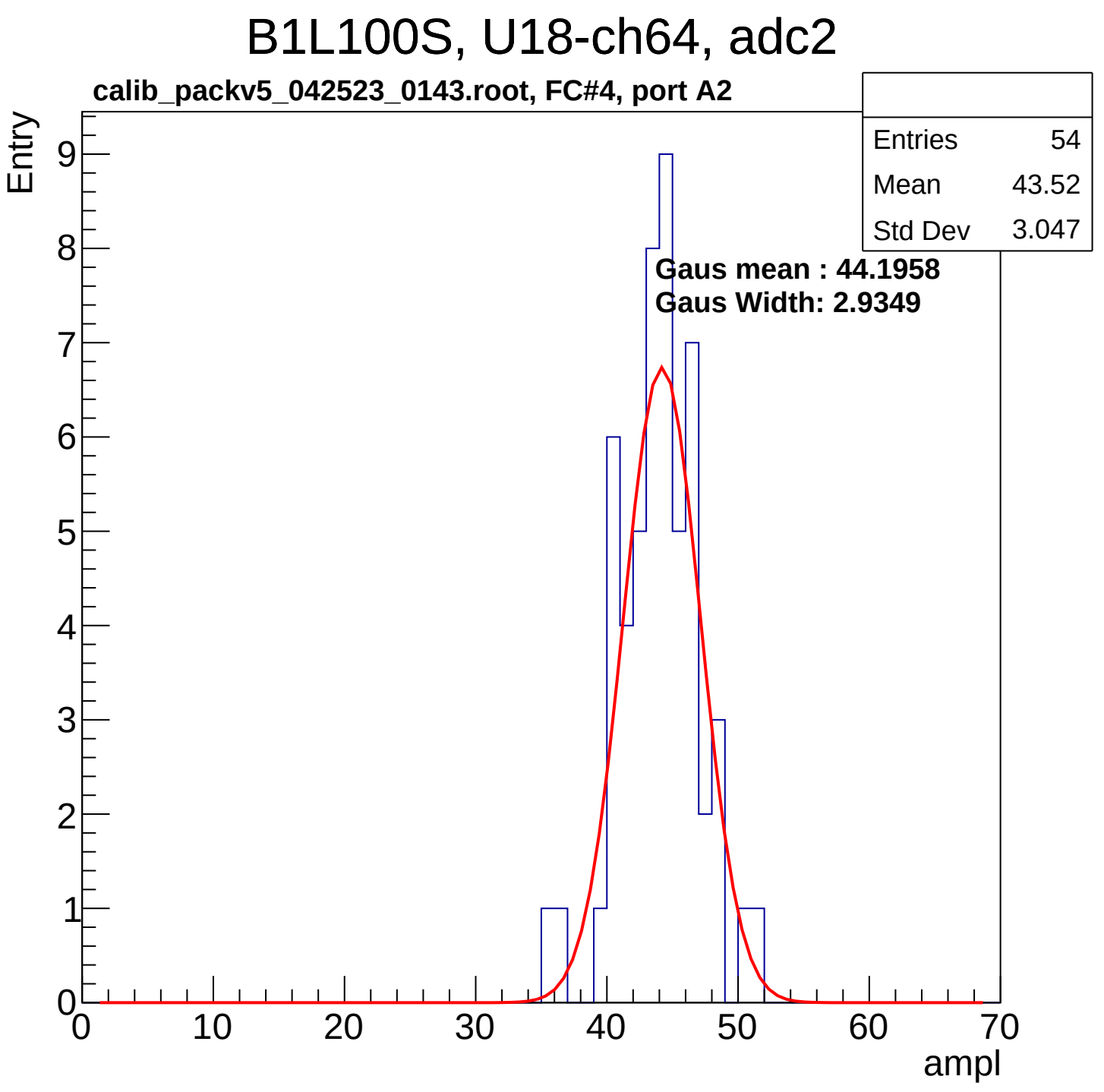

B1L100S, U18-ch63, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 33
Mean 58
Std Dev 10.66
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

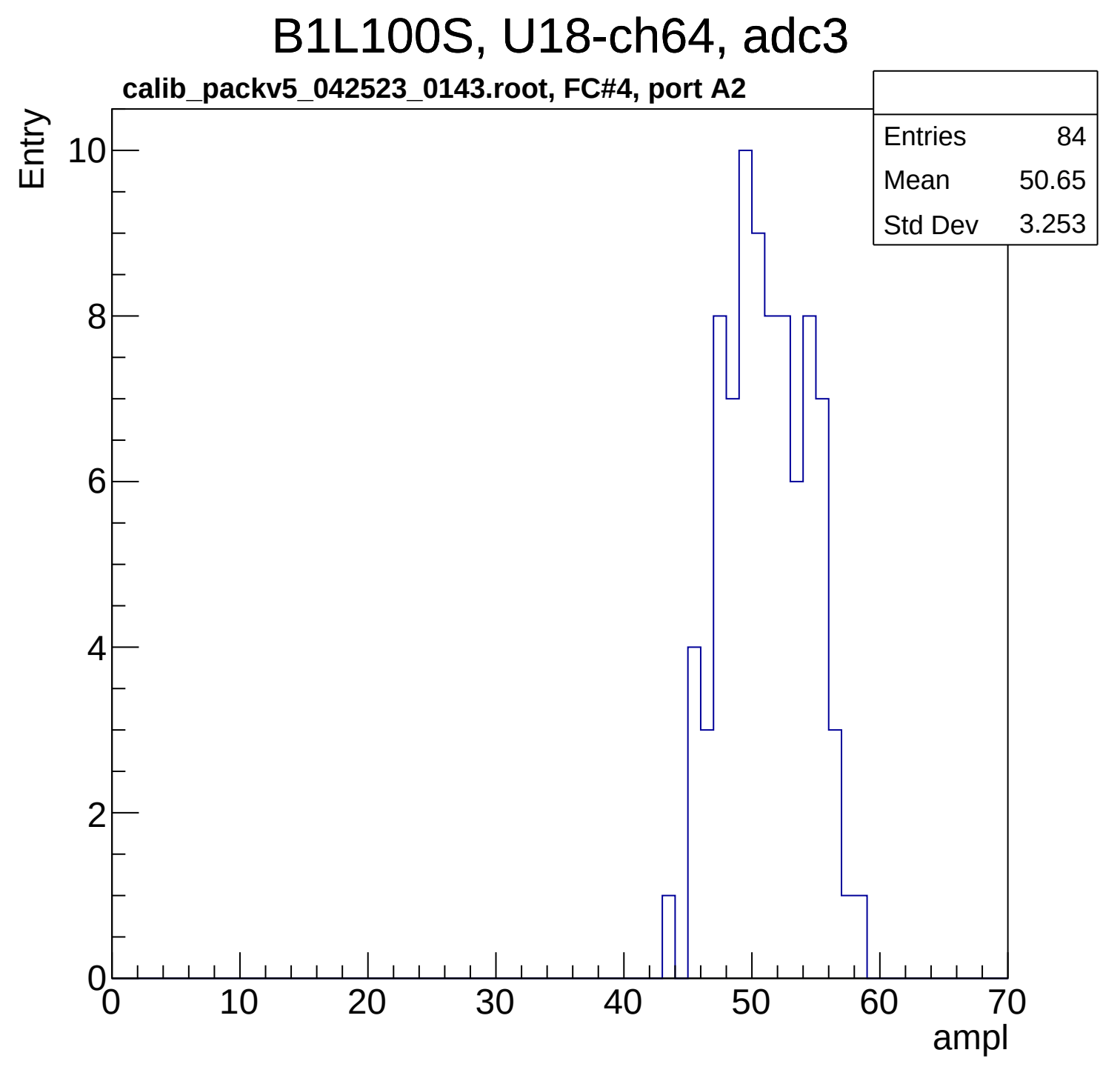

B1L100S, U18-ch63, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 61.56
Std Dev 1.771
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

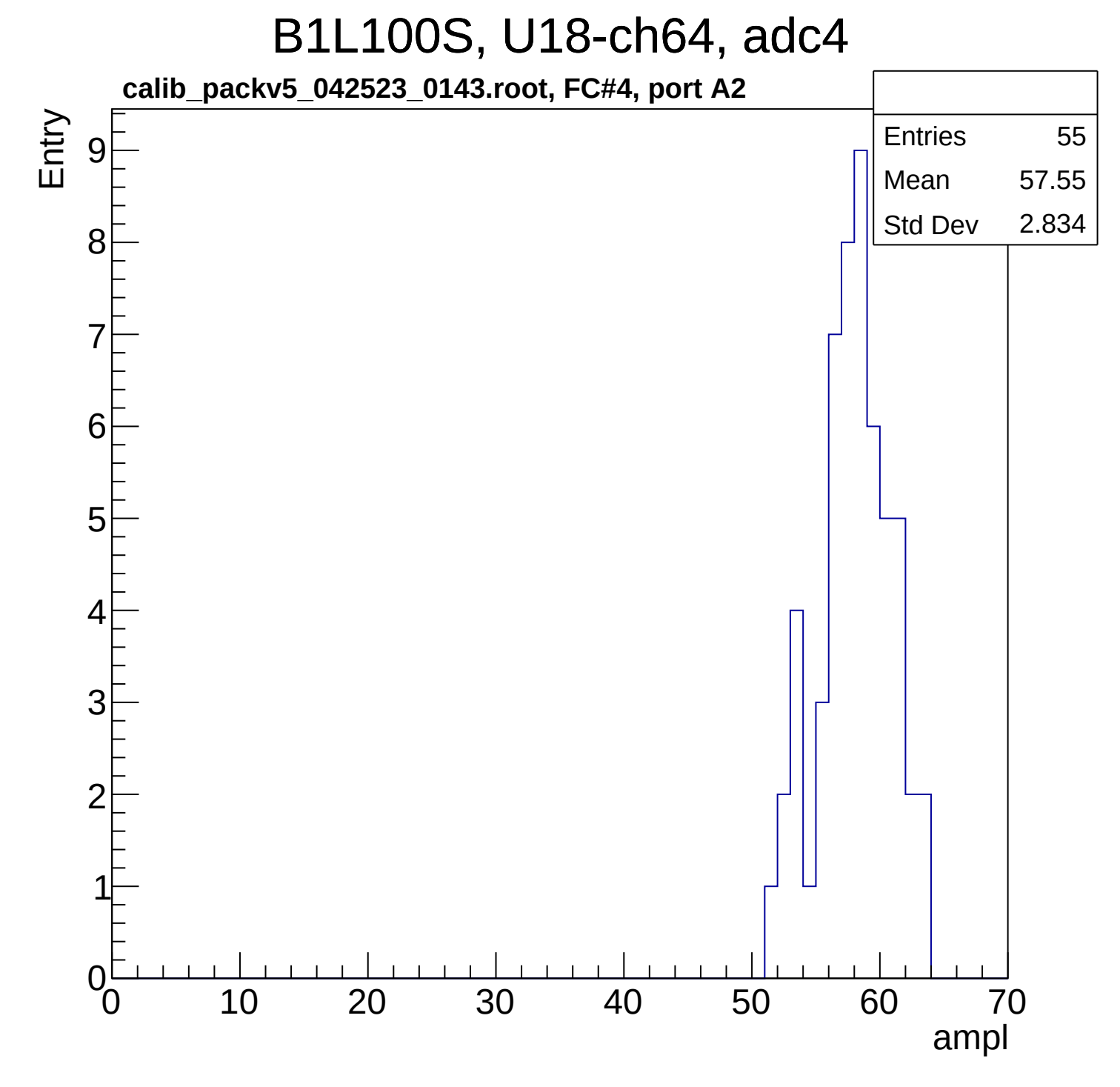

B1L100S, U18-ch63, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

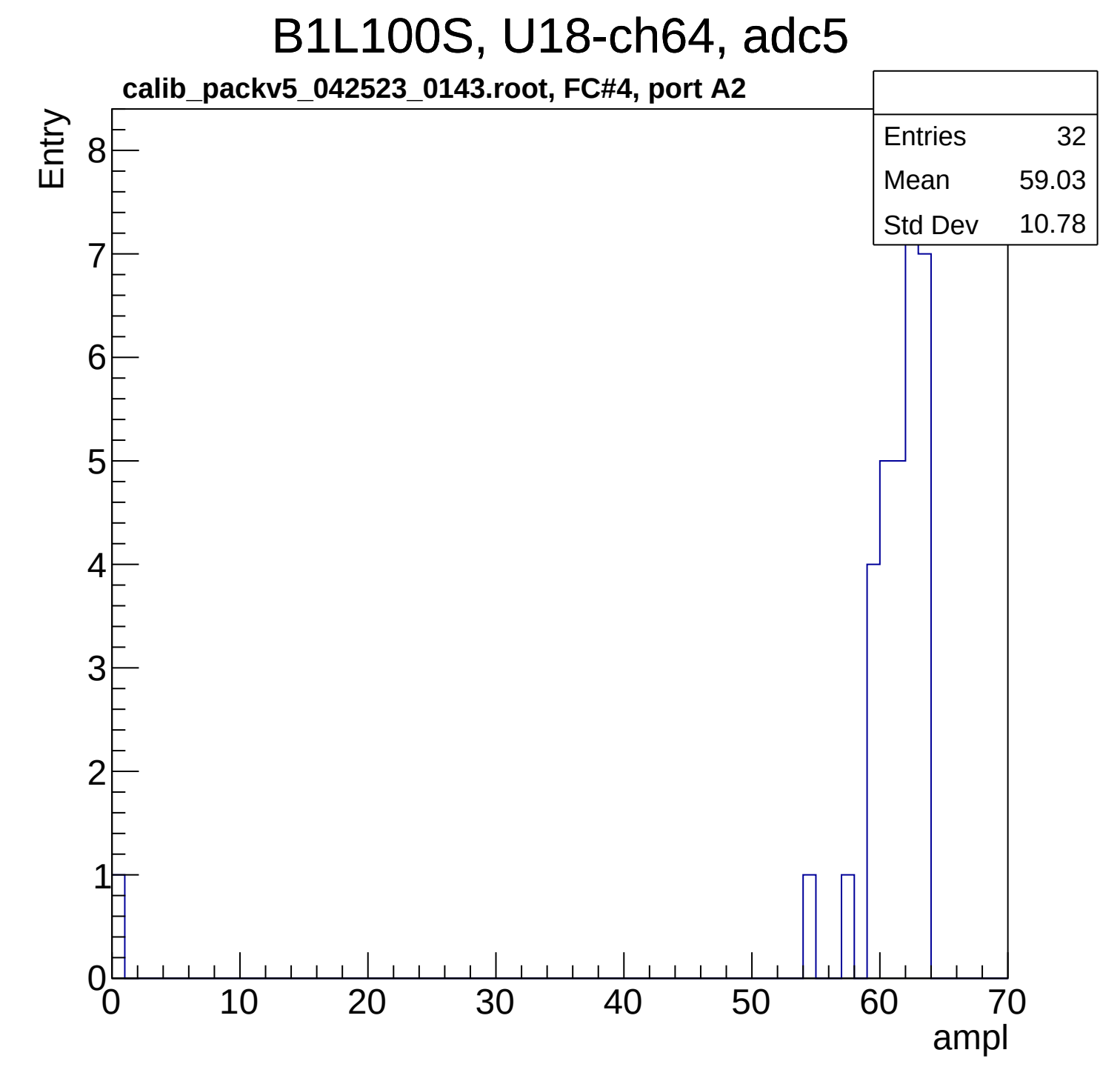

B1L100S, U18-ch64, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 29
Std Dev 7.297
Gaus mean : 31.0427
Gaus Width: 3.9833
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

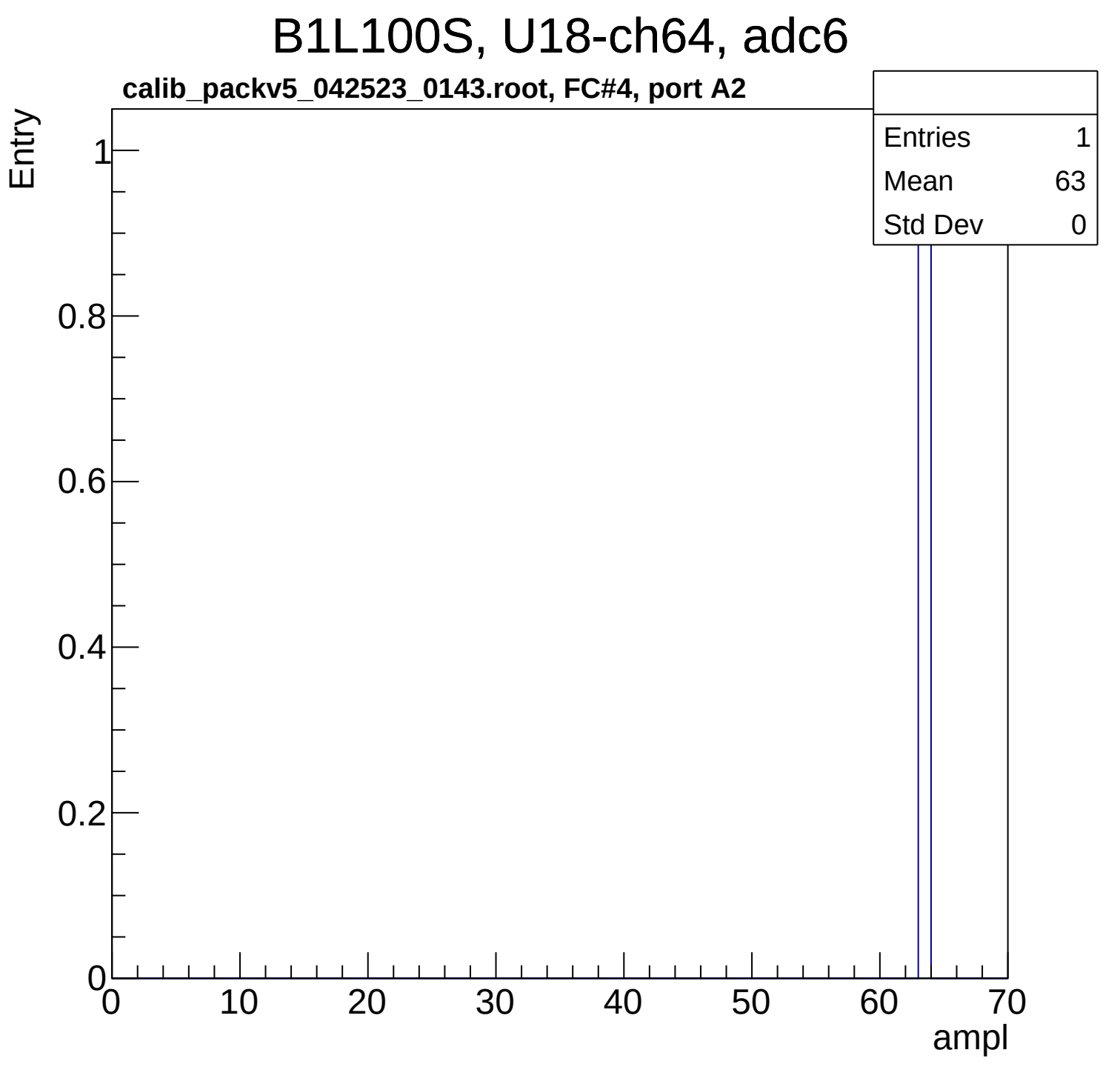

B1L100S, U18-ch64, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 37.56
Std Dev 3.082
Gaus mean : 38.1883
Gaus Width: 2.8263
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

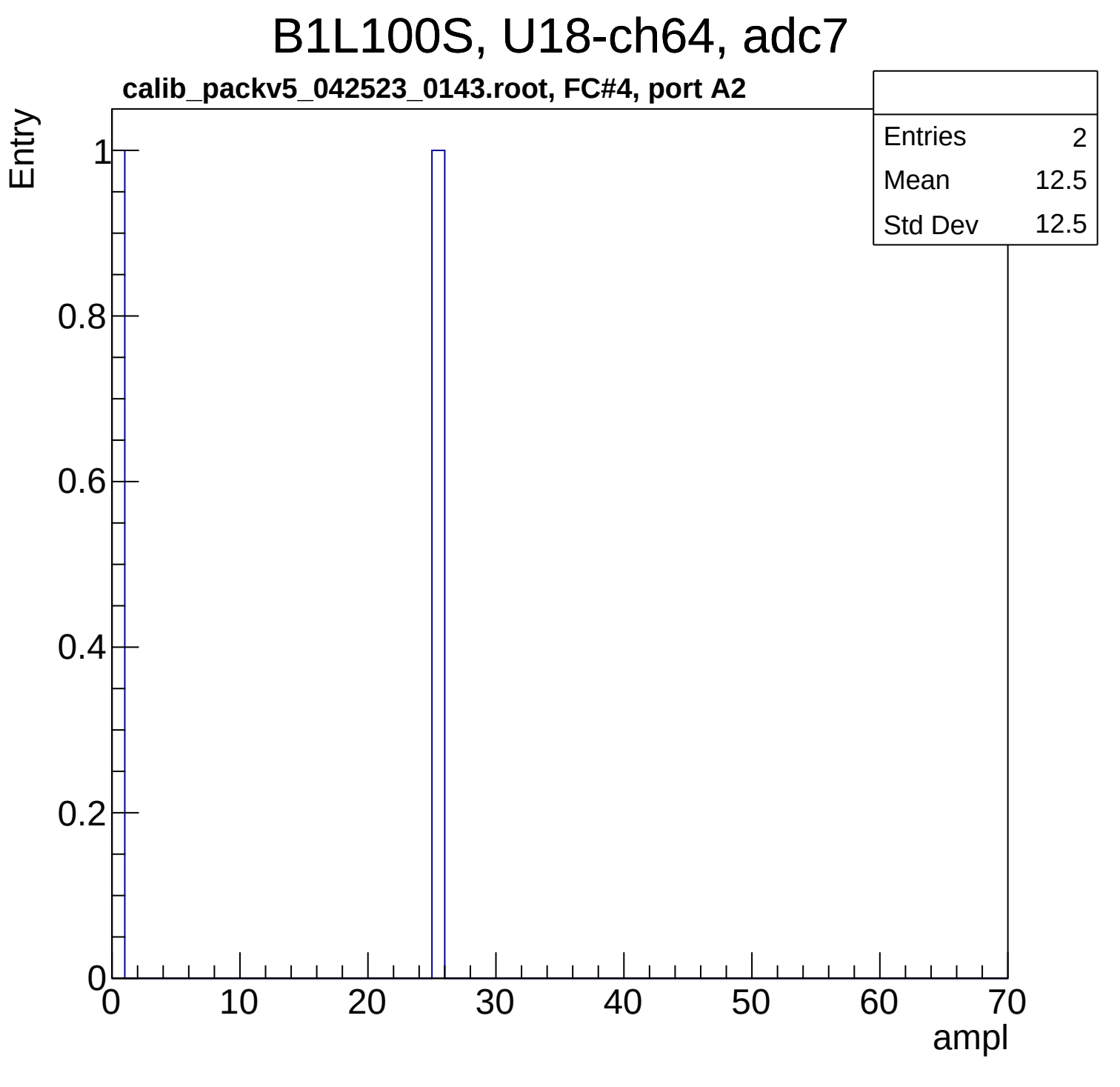

B1L100S, U18-ch64, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 43.52
Std Dev 3.047
Gaus mean : 44.1958
Gaus Width: 2.9349
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

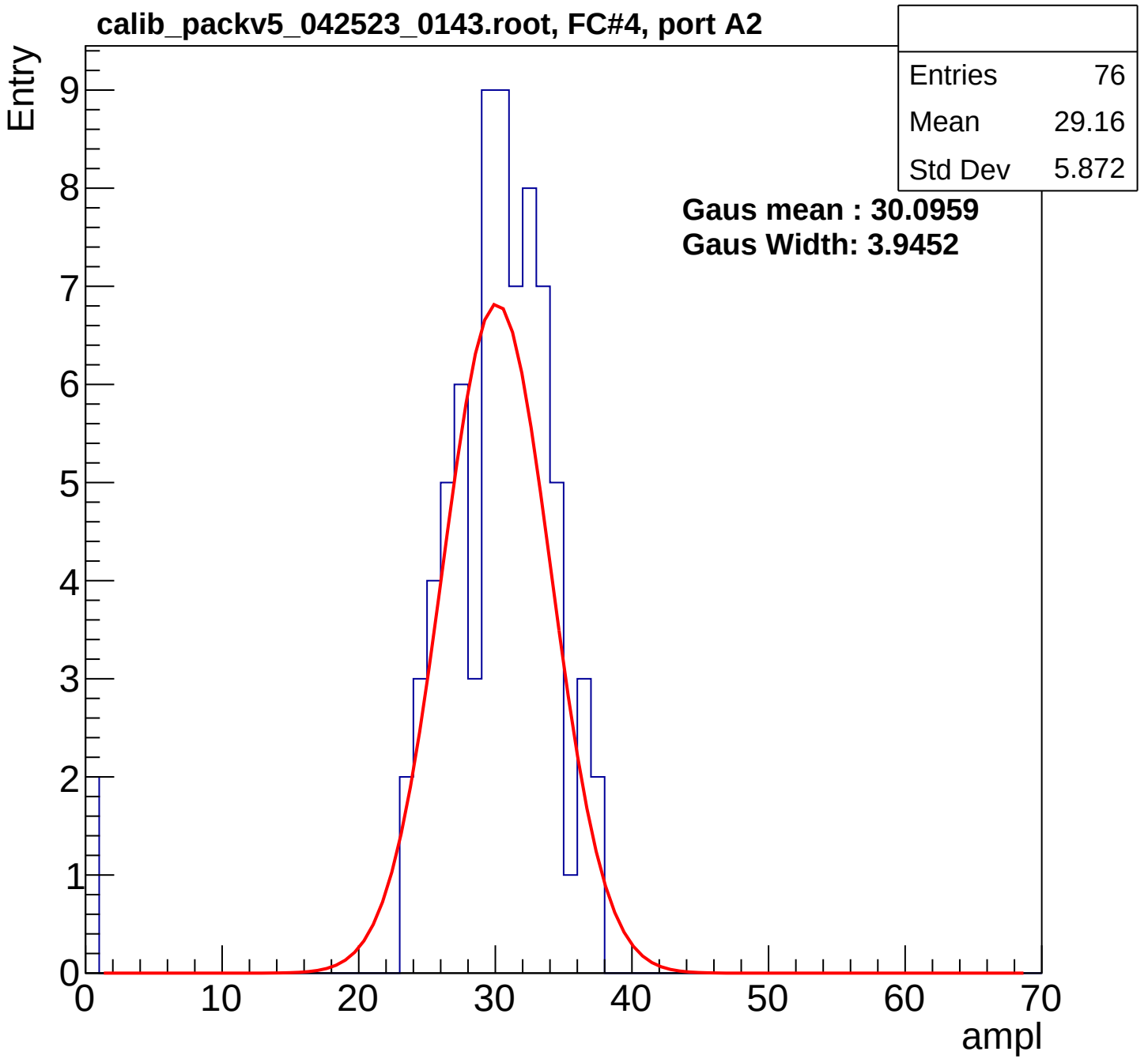

B1L100S, U18-ch64, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 84
Mean 50.65
Std Dev 3.253
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

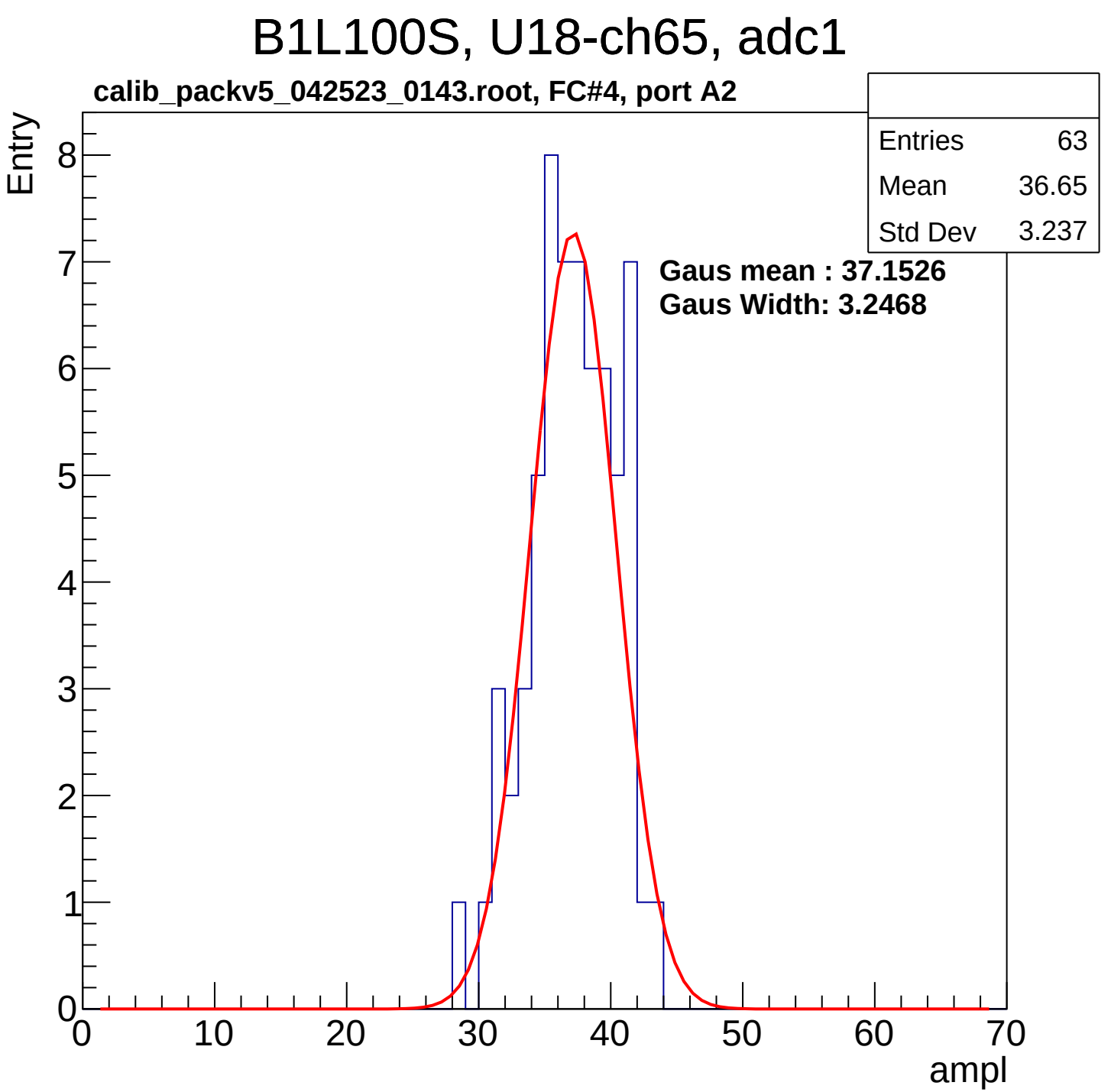

B1L100S, U18-ch64, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 57.55
Std Dev 2.834
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

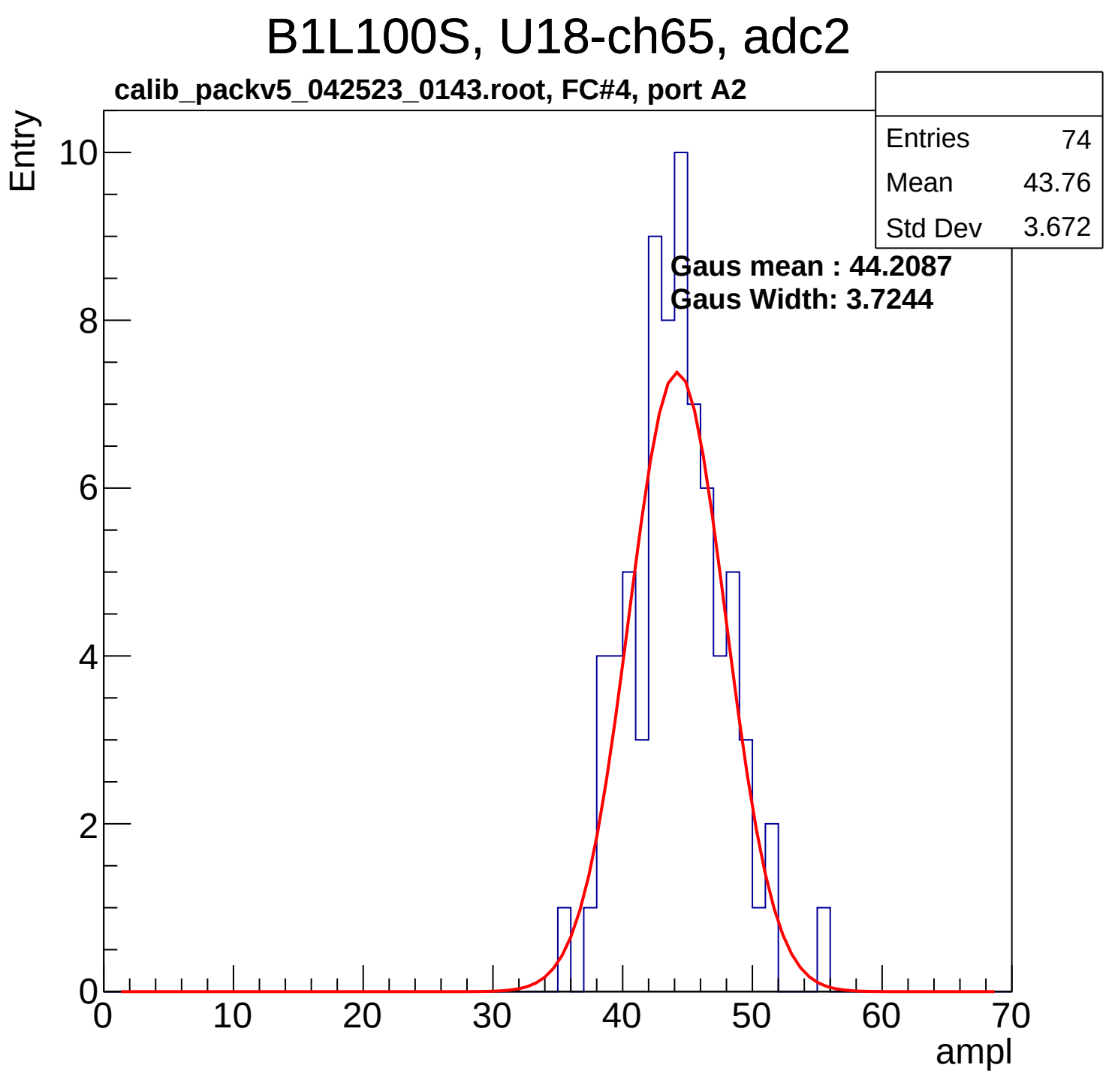

B1L100S, U18-ch64, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 32
Mean 59.03
Std Dev 10.78
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

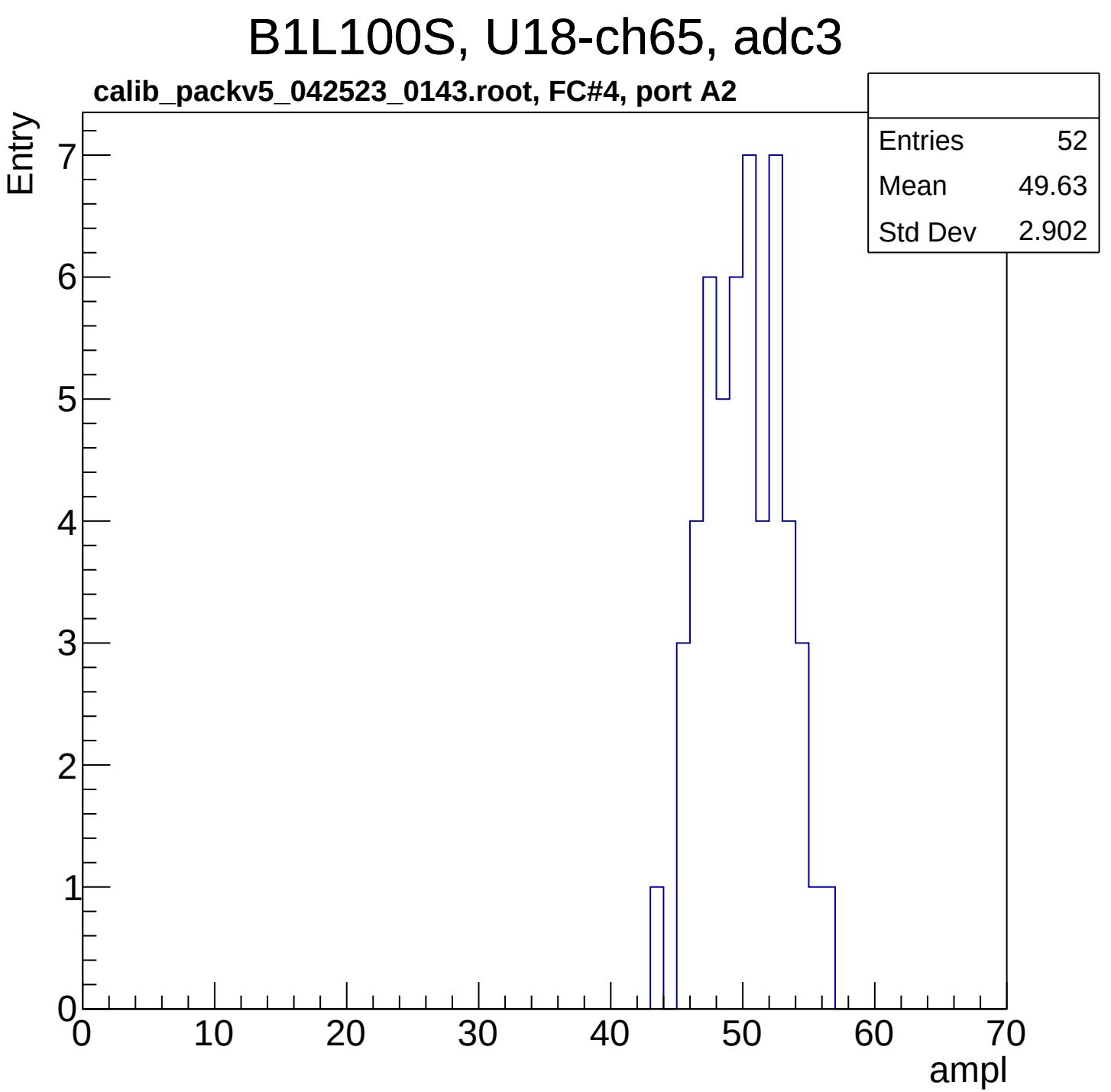

B1L100S, U18-ch64, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

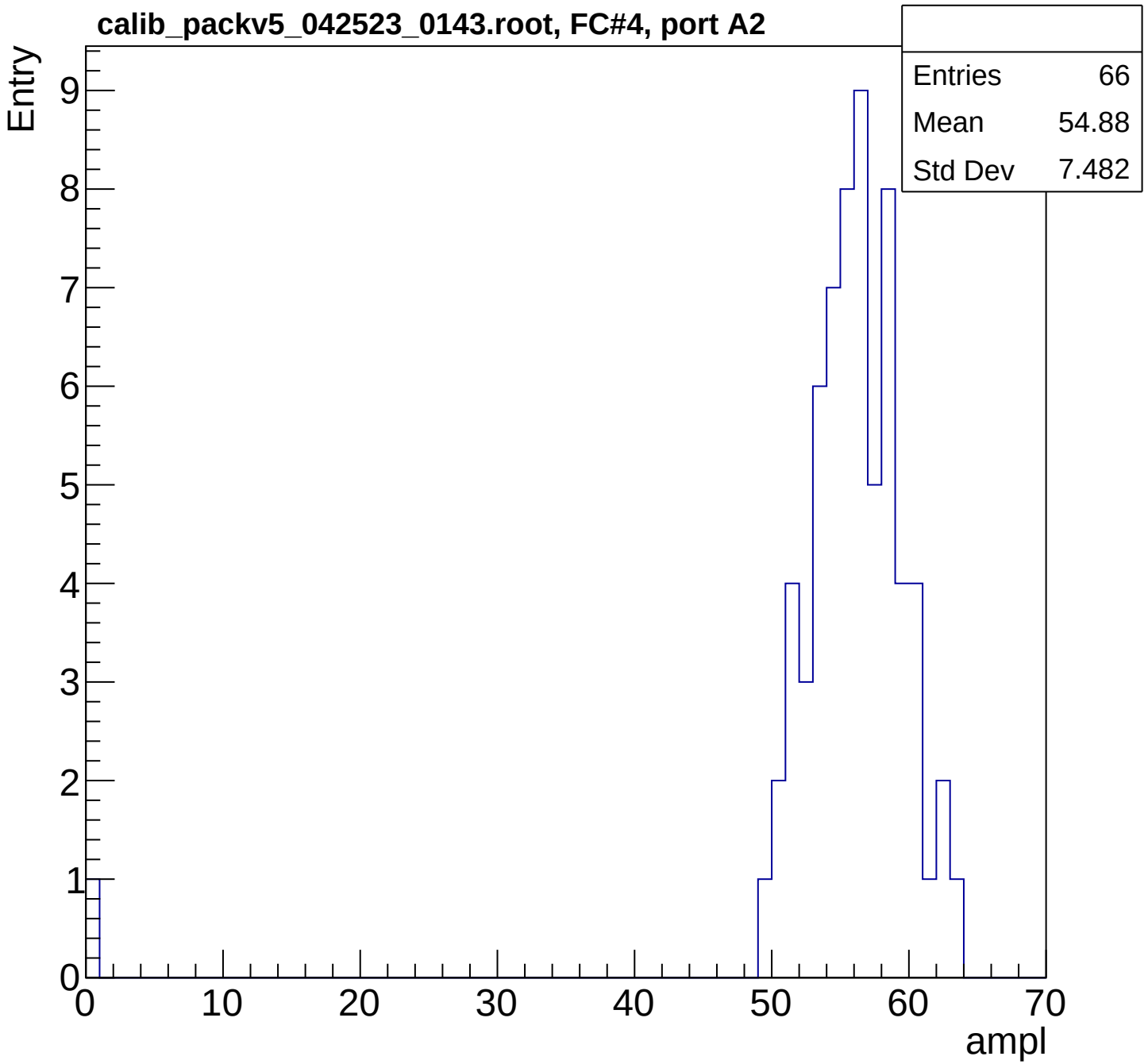

B1L100S, U18-ch64, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 12.5
Std Dev 12.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

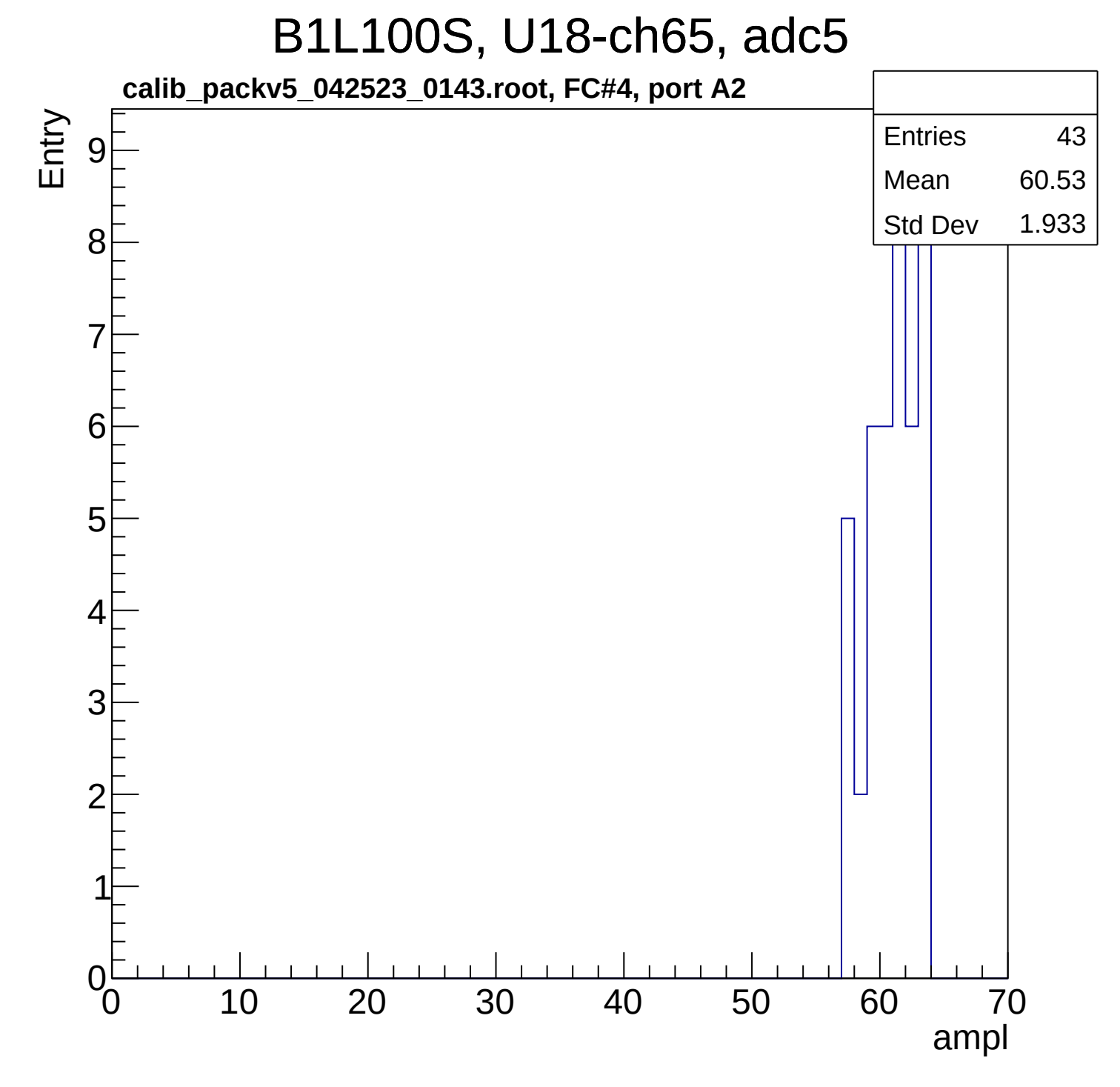

B1L100S, U18-ch65, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 29.16
Std Dev 5.872
Gaus mean : 30.0959
Gaus Width: 3.9452
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

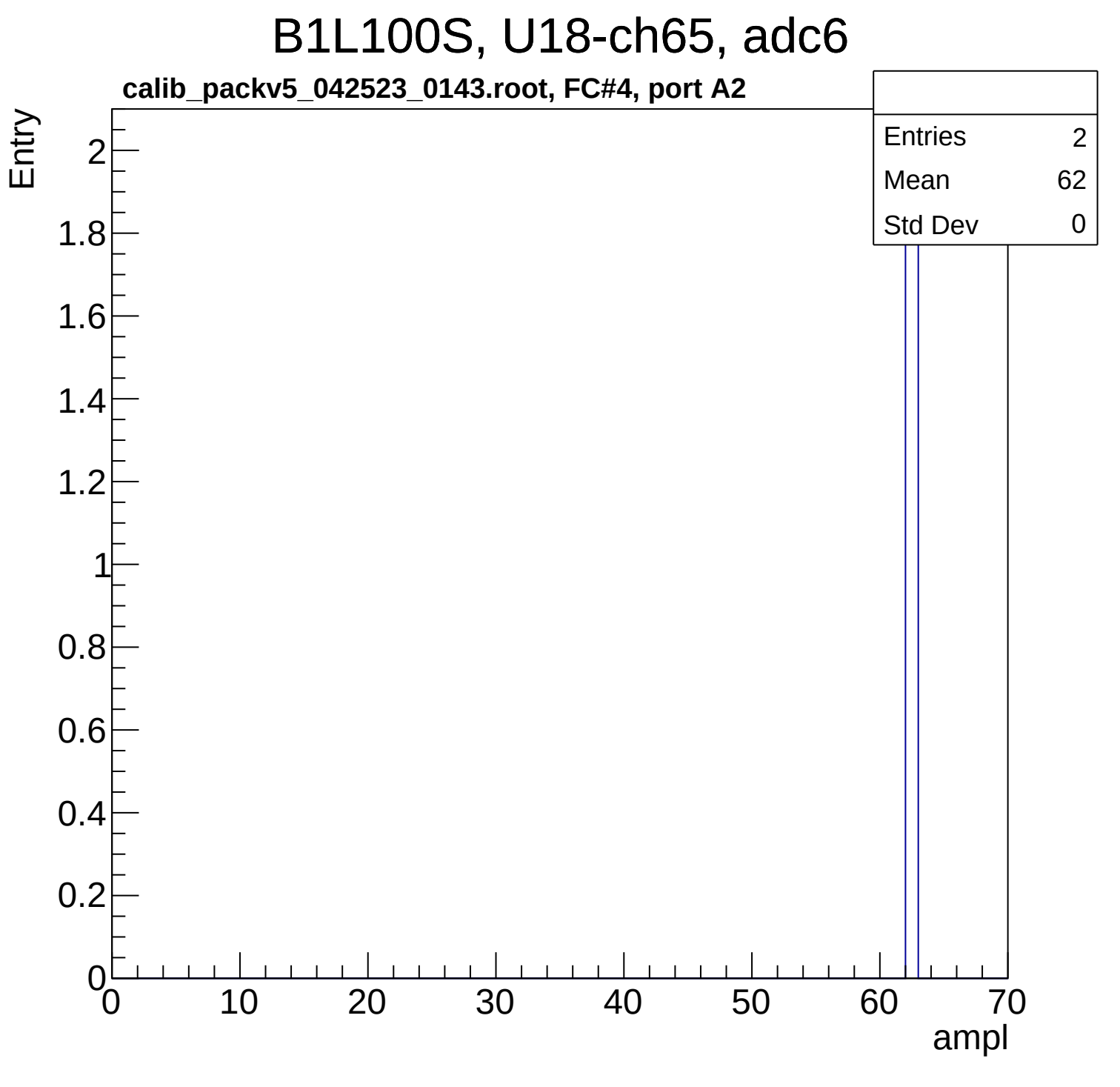

B1L100S, U18-ch65, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 36.65
Std Dev 3.237
Gaus mean : 37.1526
Gaus Width: 3.2468
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

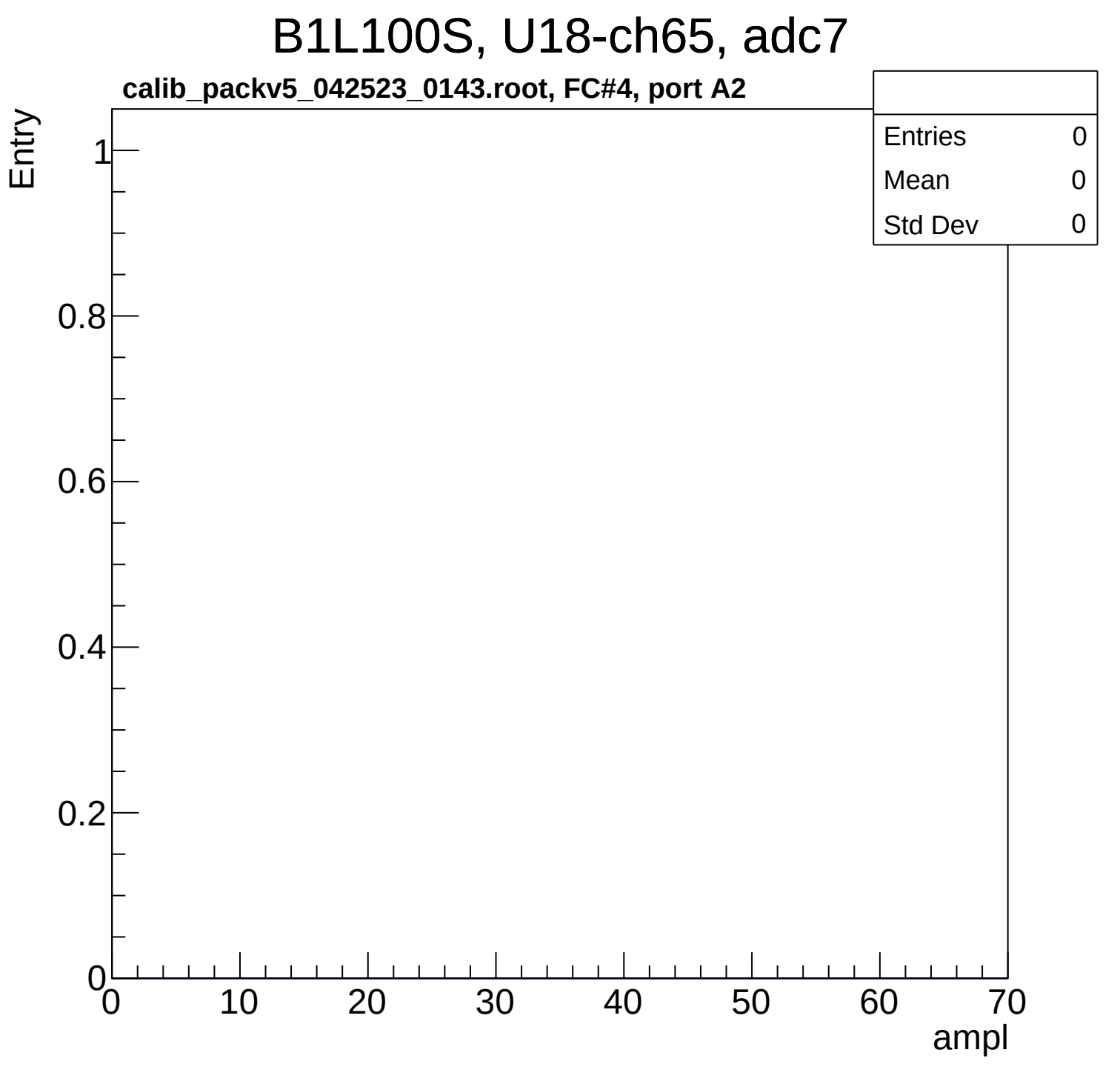

B1L100S, U18-ch65, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 43.76
Std Dev 3.672
Gaus mean : 44.2087
Gaus Width: 3.7244
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

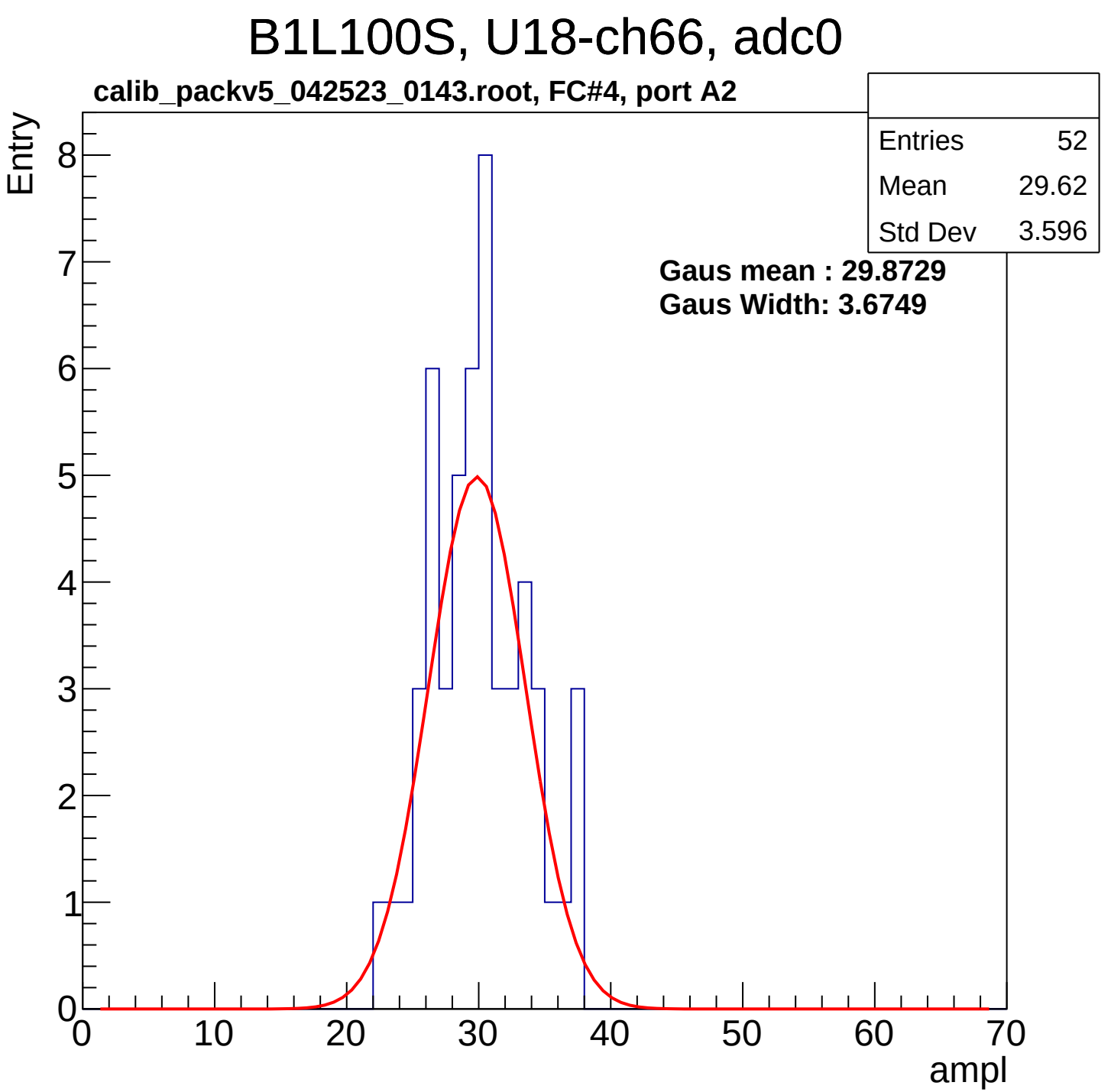

B1L100S, U18-ch65, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 49.63
Std Dev 2.902
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

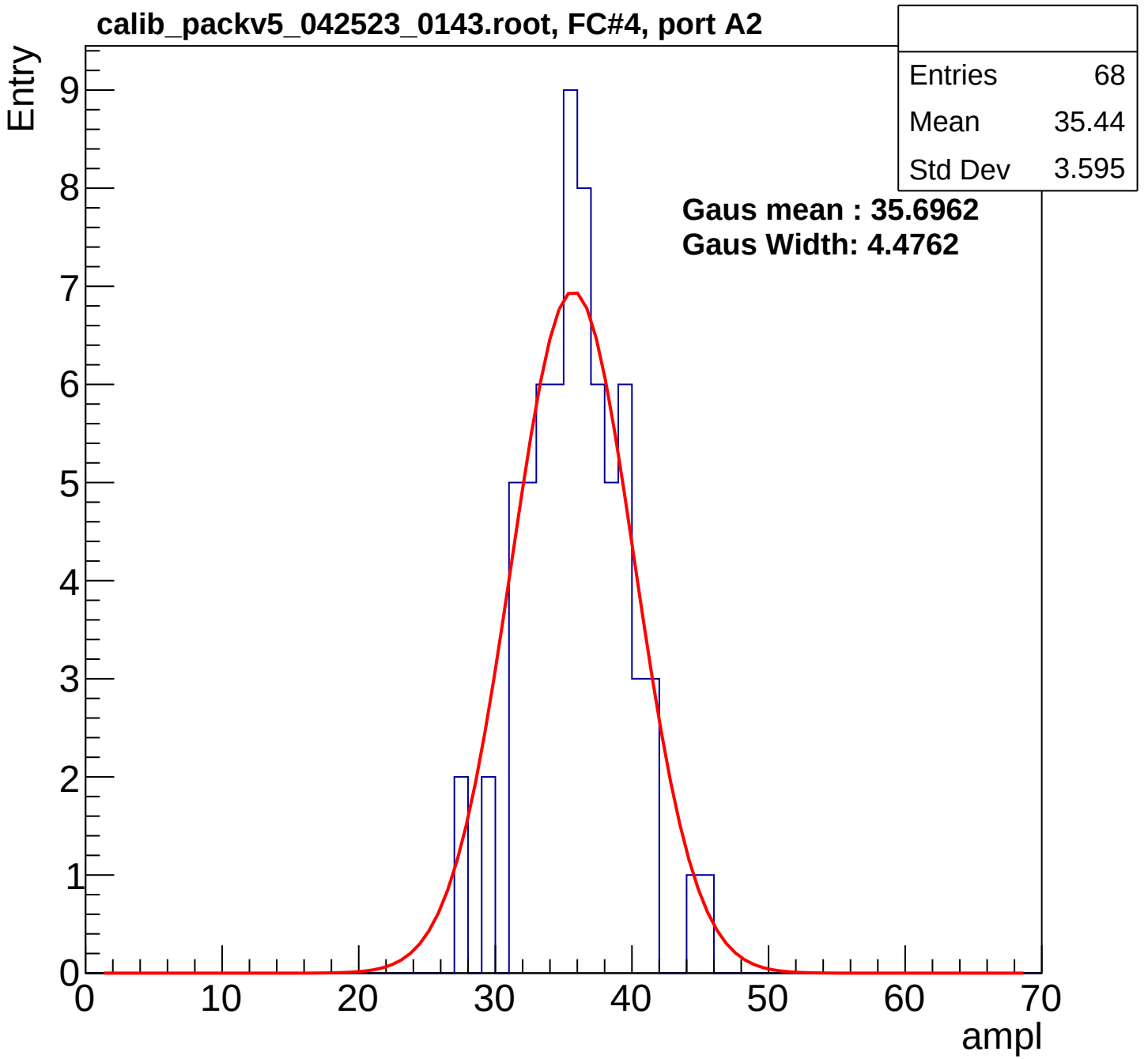

B1L100S, U18-ch65, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 54.88
Std Dev 7.482
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

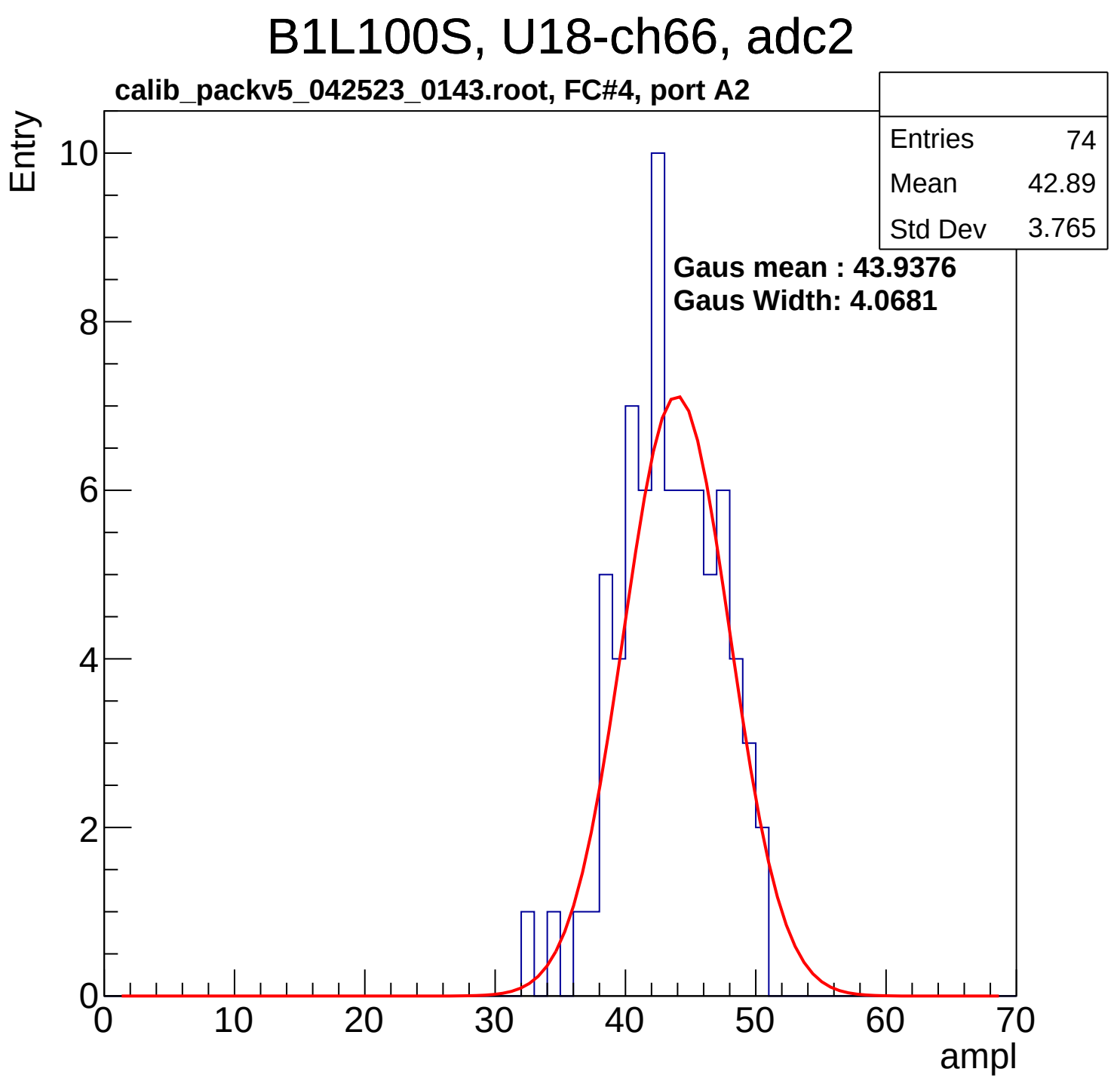

B1L100S, U18-ch65, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 60.53
Std Dev 1.933
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

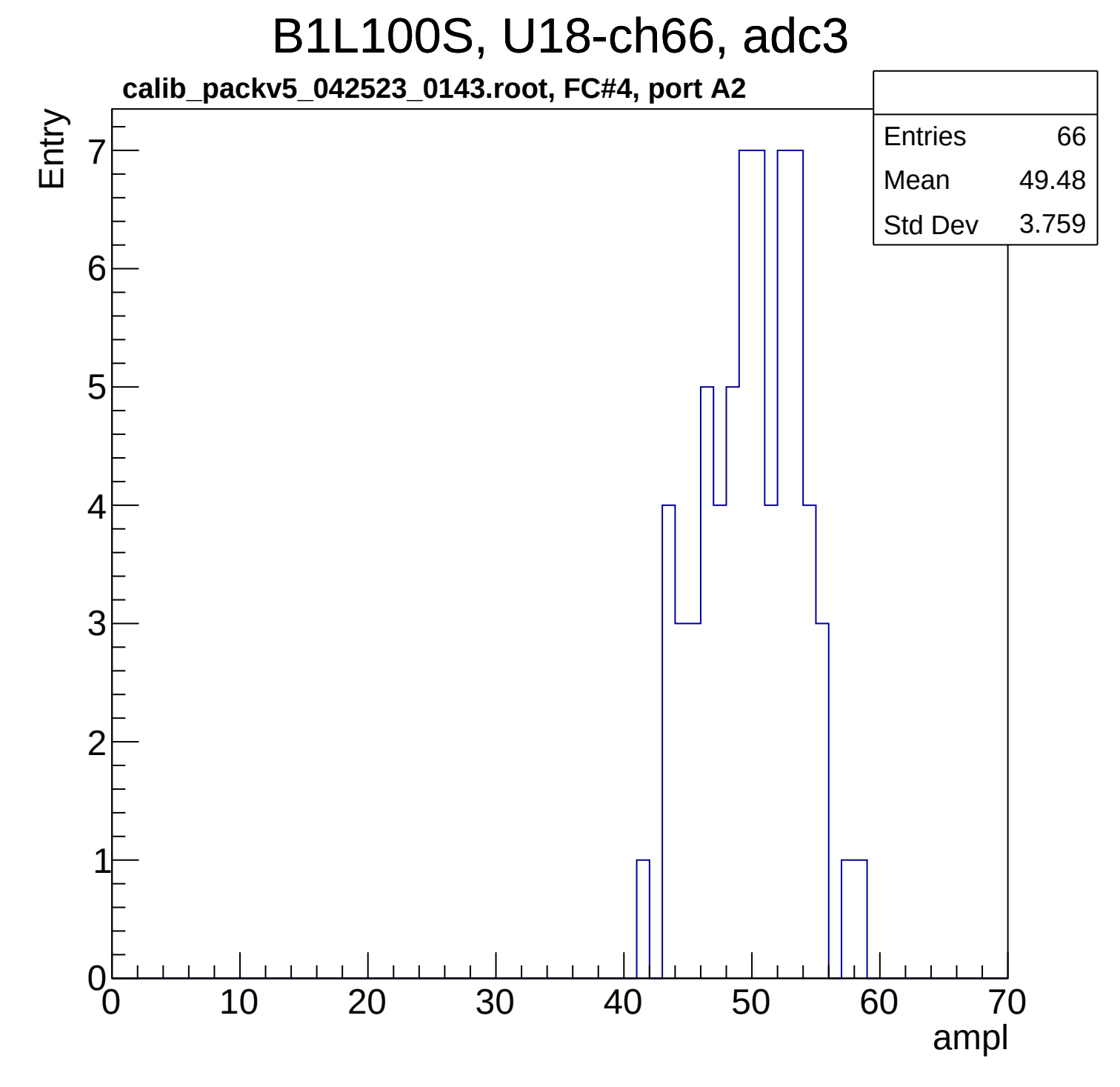

B1L100S, U18-ch65, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 62
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

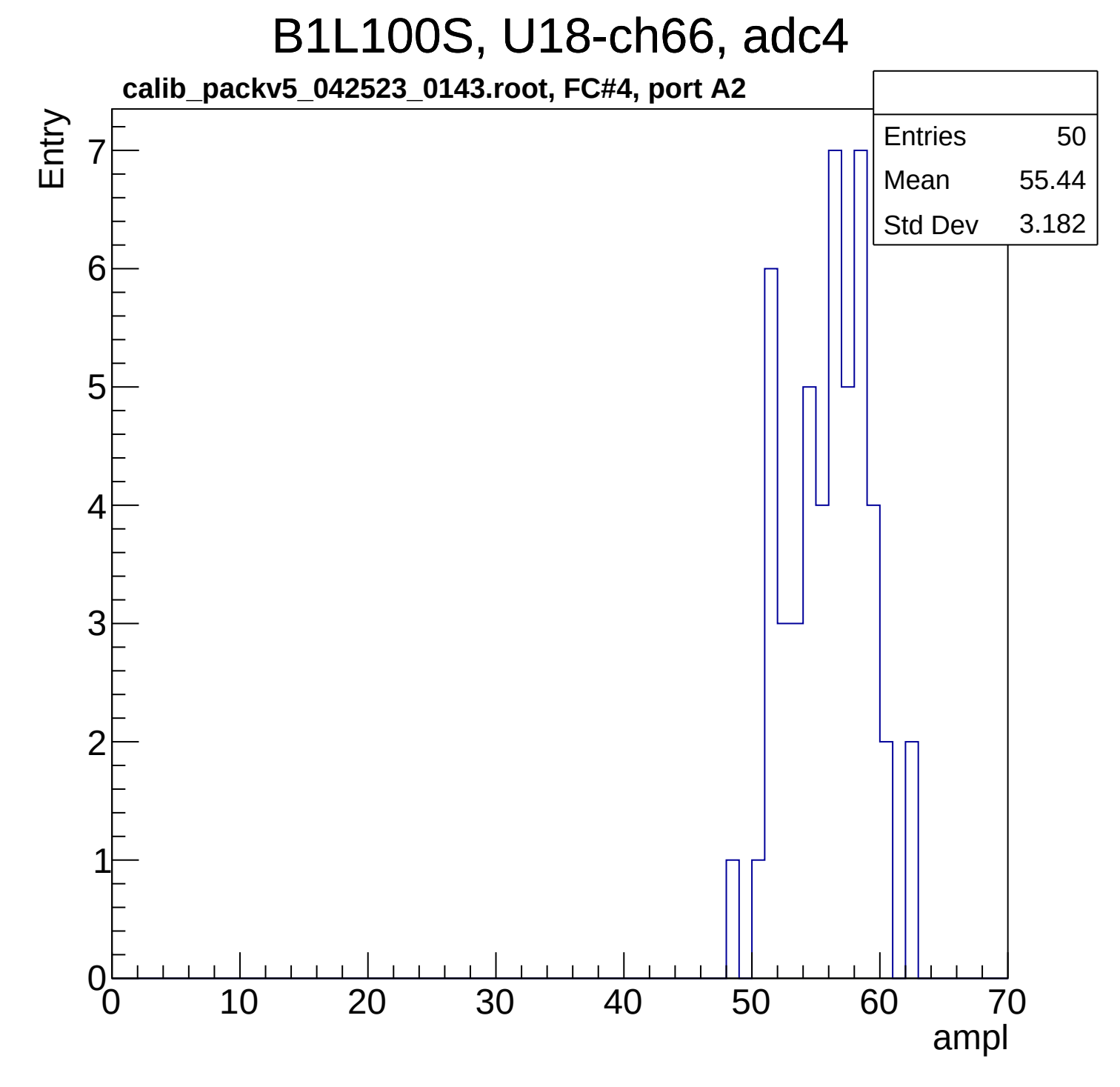

B1L100S, U18-ch65, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

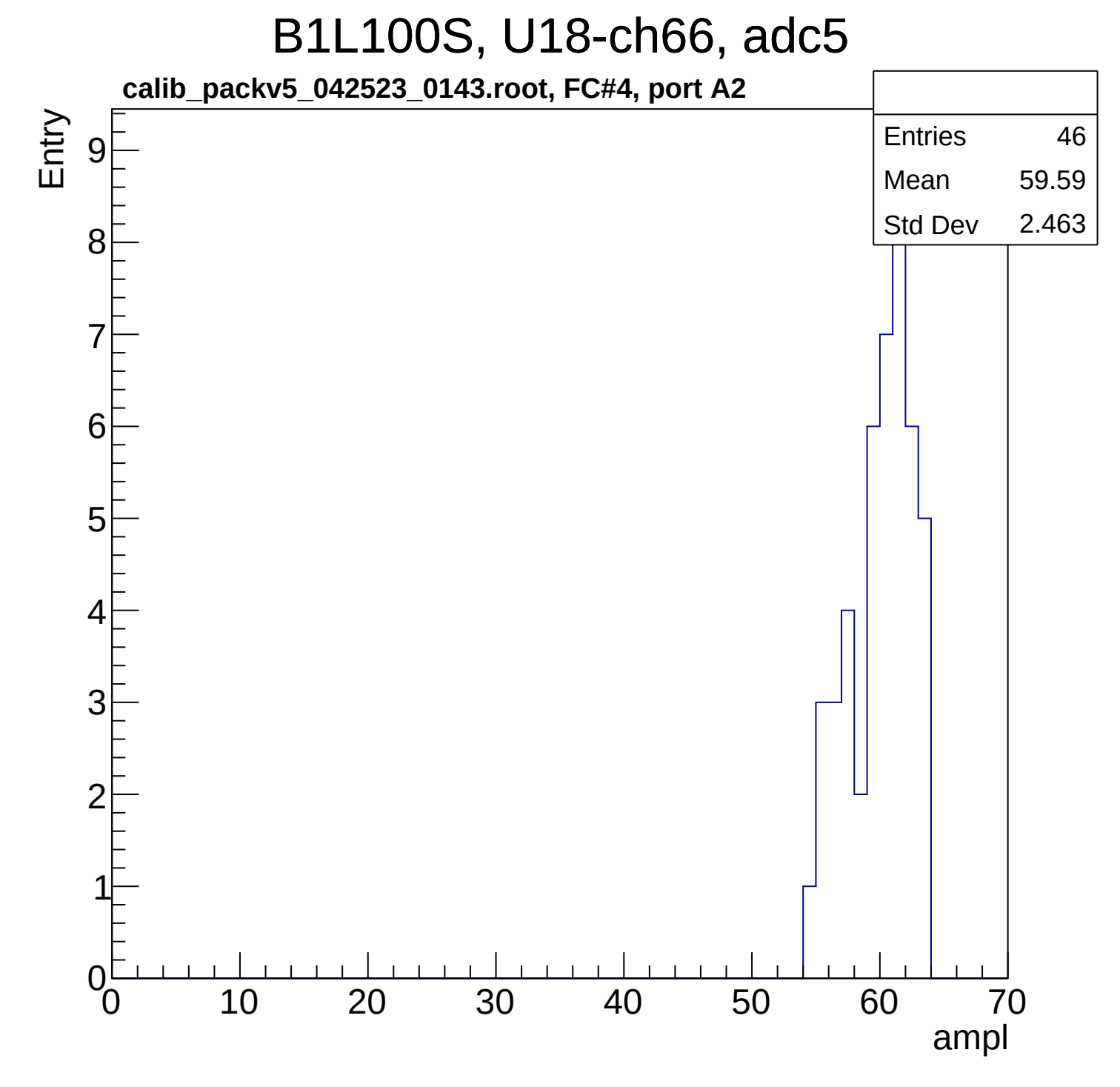

B1L100S, U18-ch66, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 29.62
Std Dev 3.596
Gaus mean : 29.8729
Gaus Width: 3.6749
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

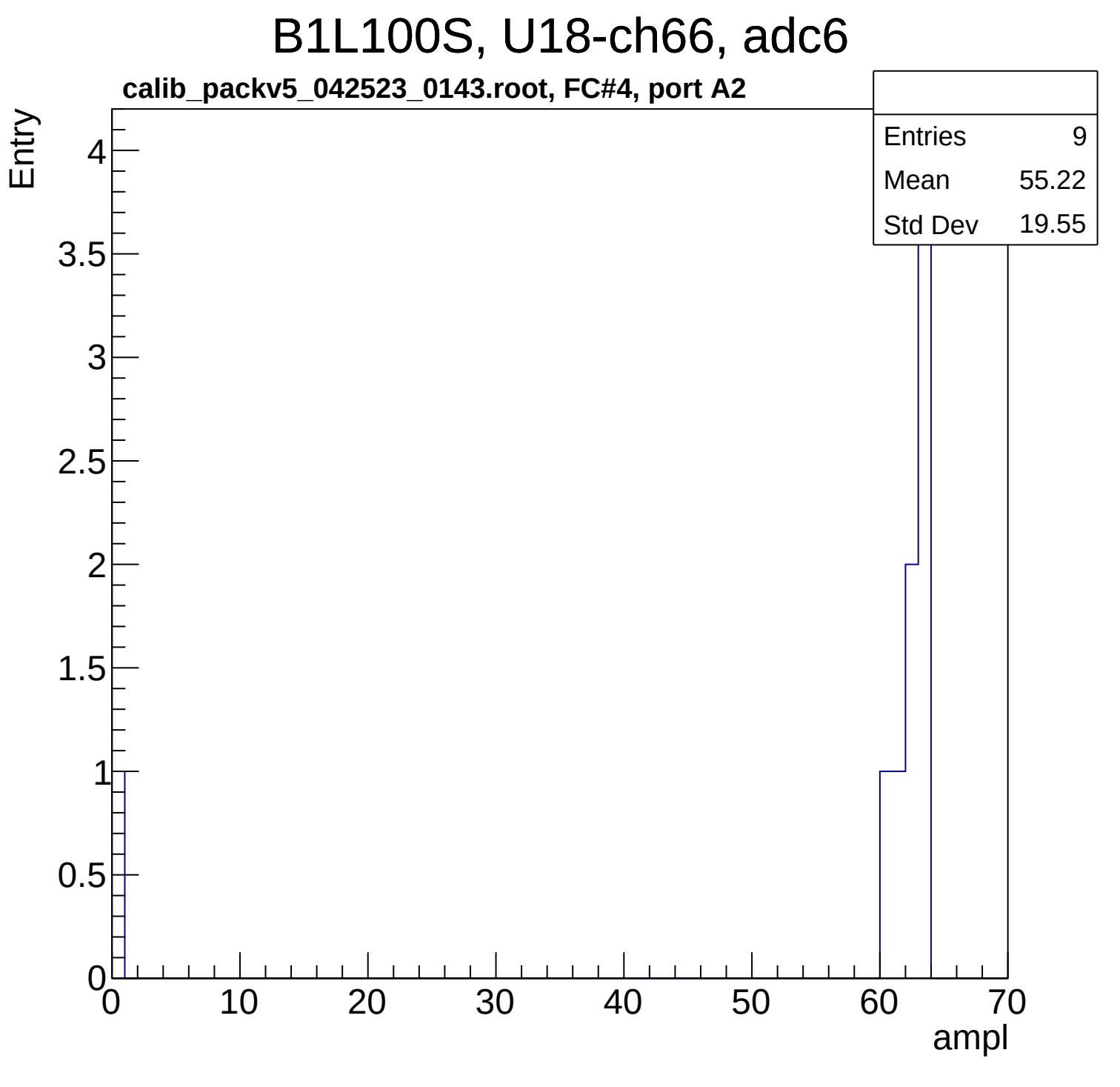

B1L100S, U18-ch66, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 35.44
Std Dev 3.595
Gaus mean : 35.6962
Gaus Width: 4.4762
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

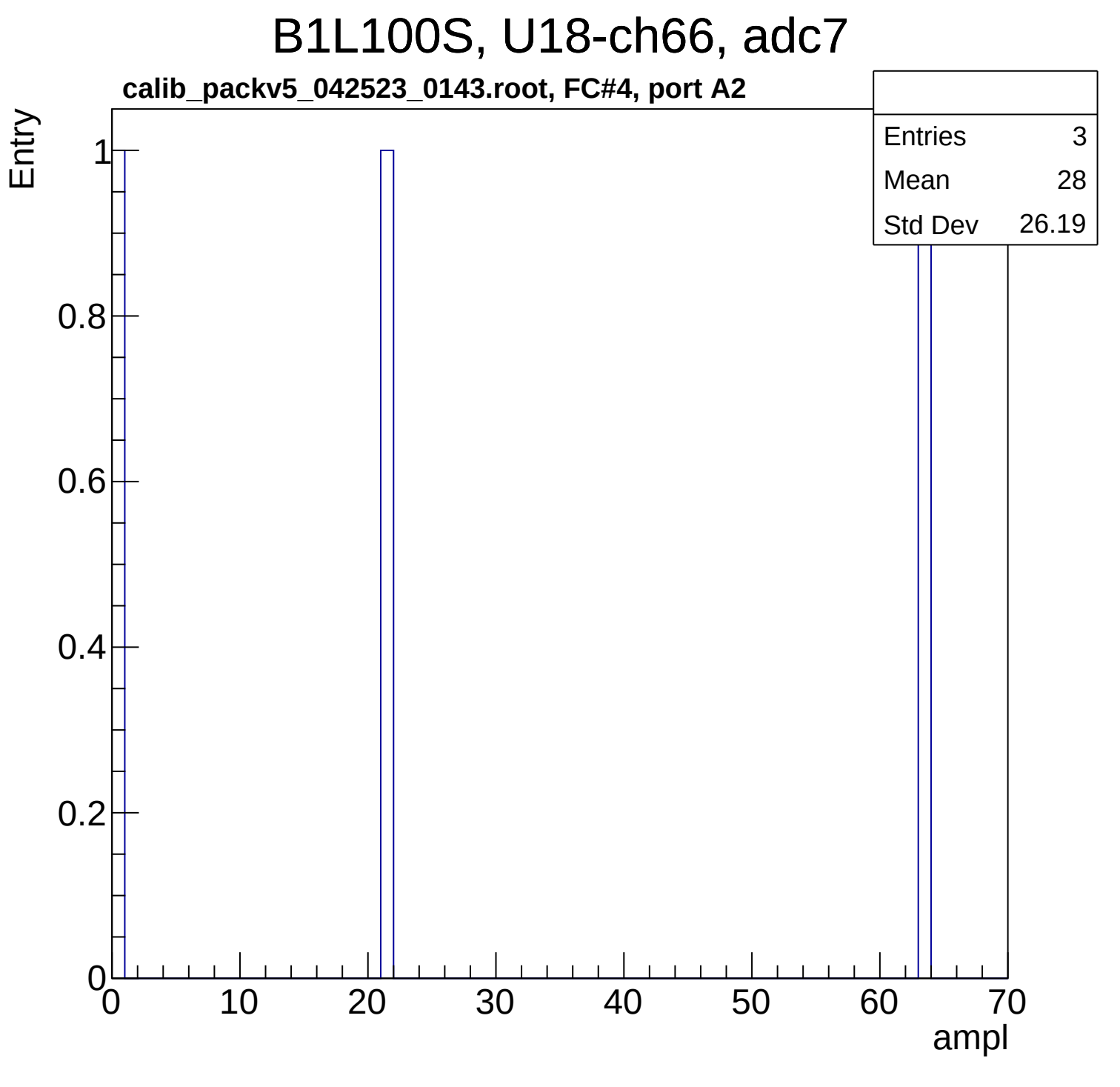

B1L100S, U18-ch66, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 42.89
Std Dev 3.765
Gaus mean : 43.9376
Gaus Width: 4.0681
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

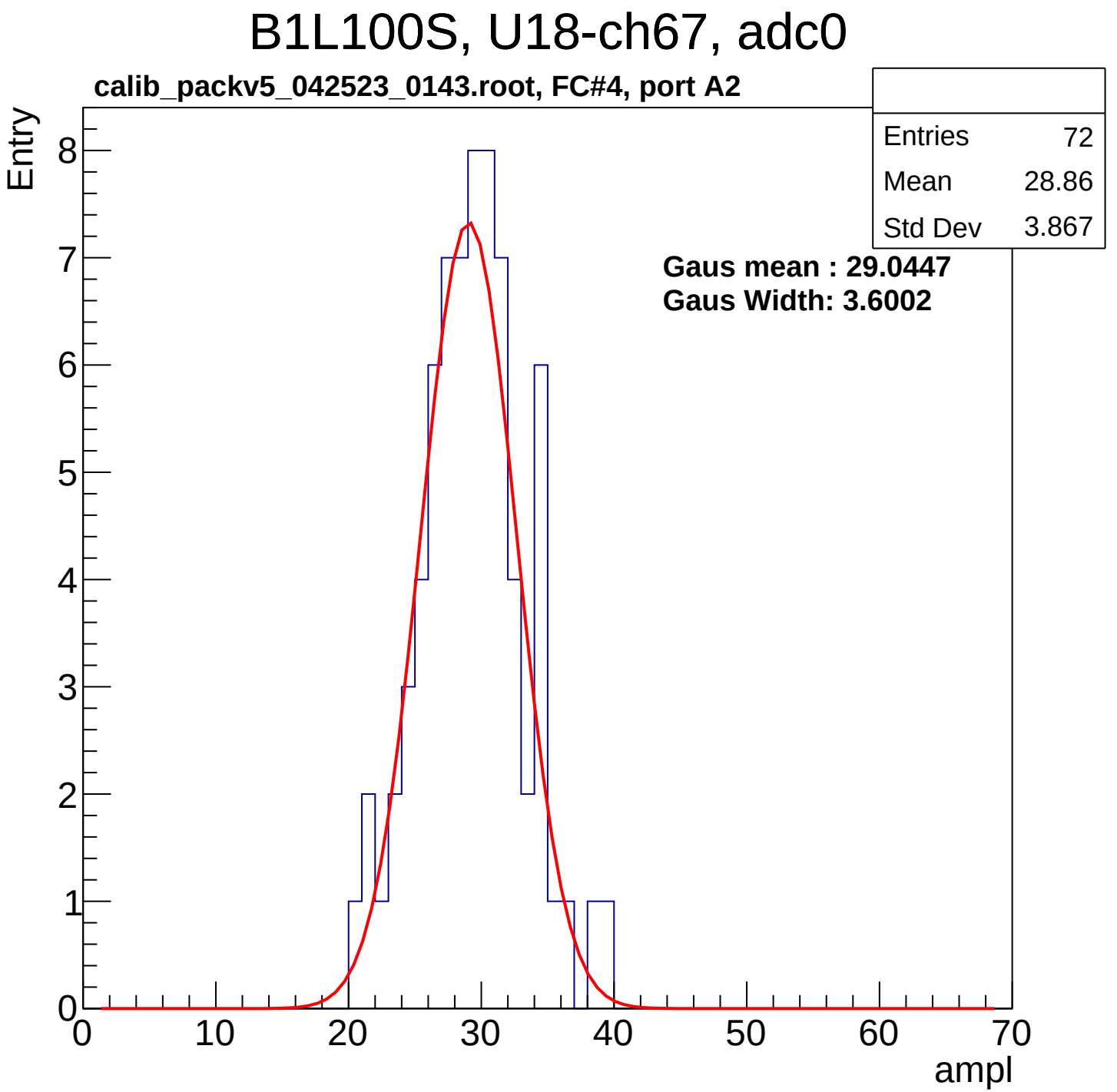

B1L100S, U18-ch66, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 49.48
Std Dev 3.759
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

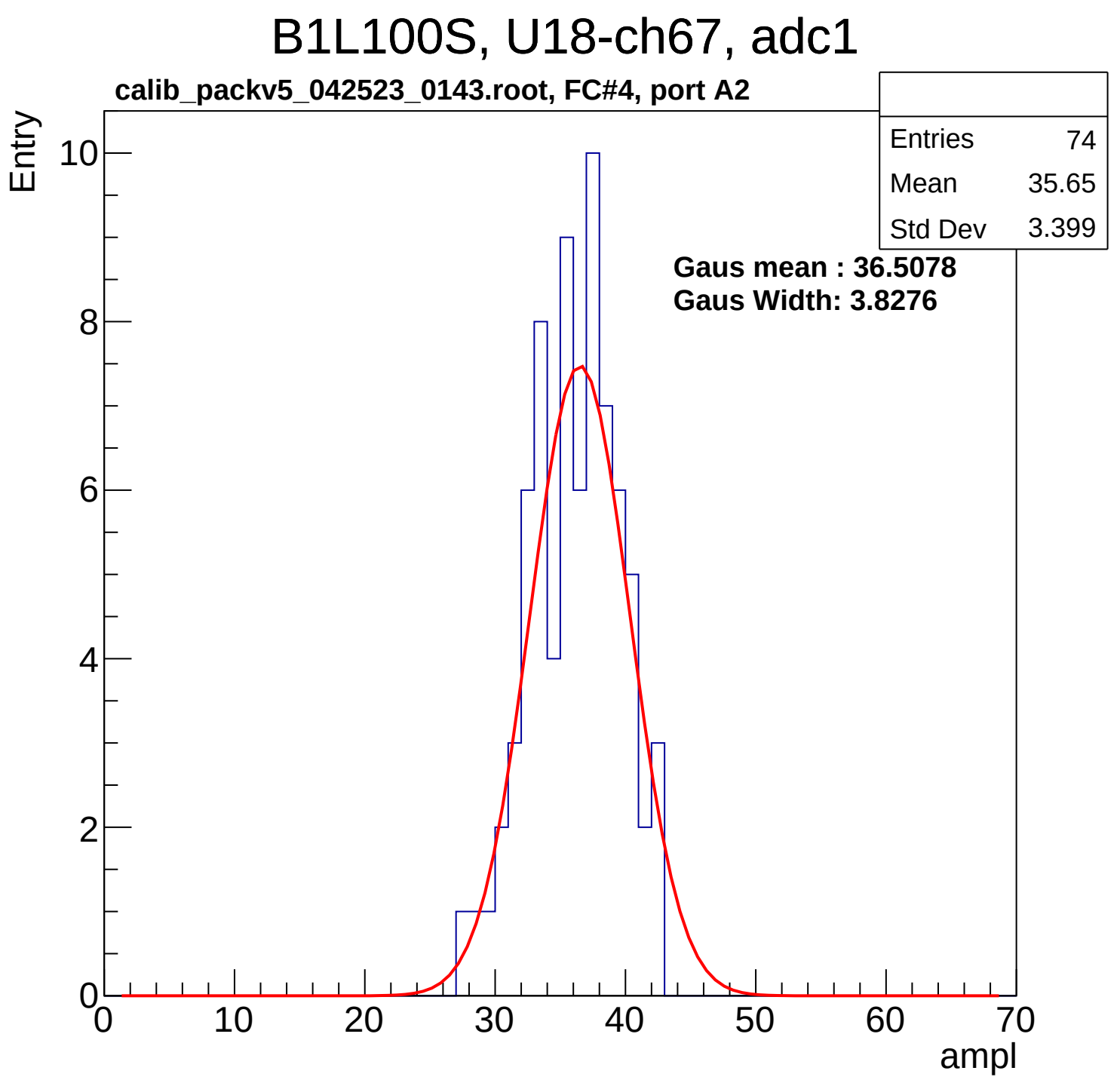

B1L100S, U18-ch66, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 55.44
Std Dev 3.182
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

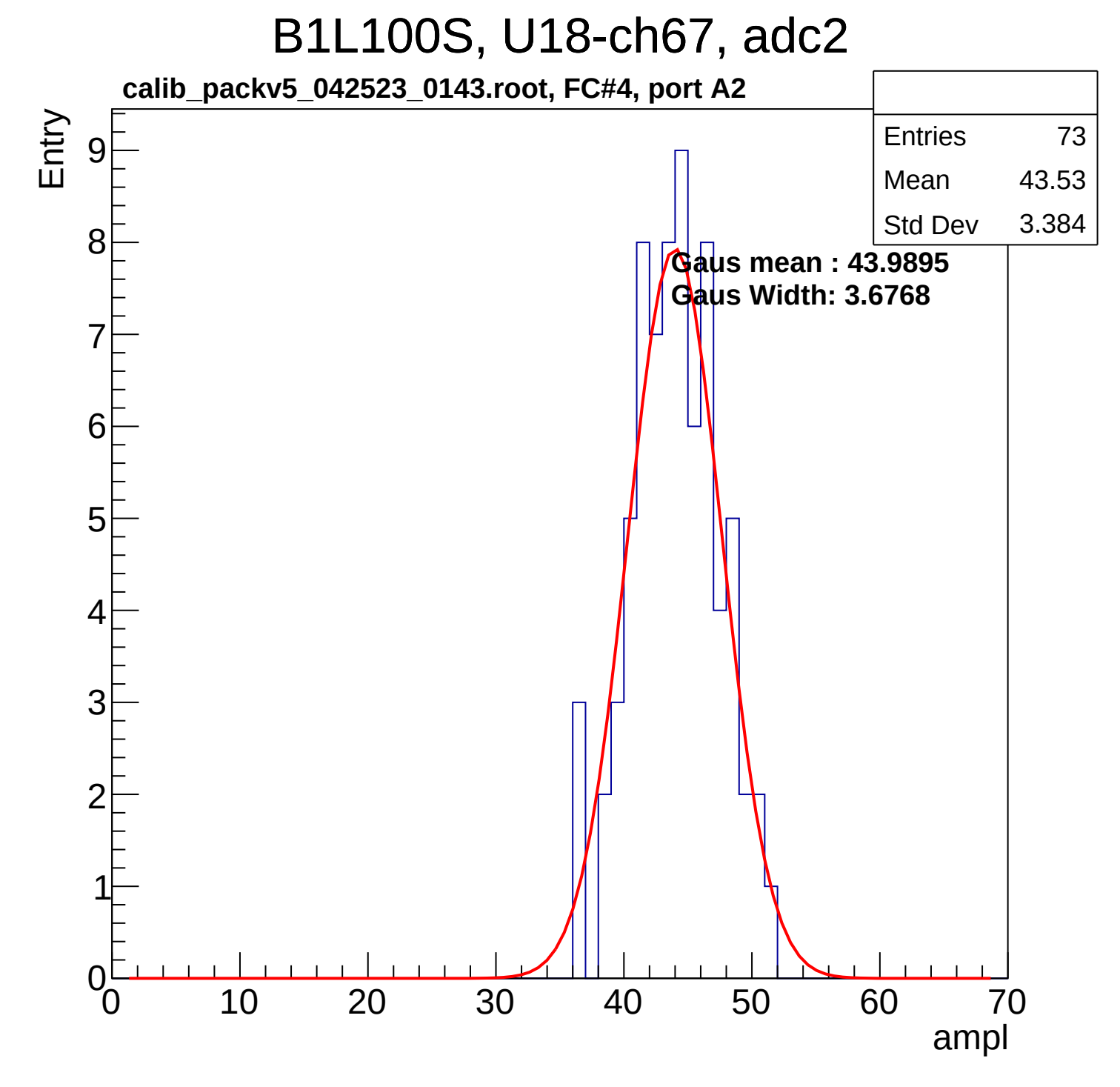

B1L100S, U18-ch66, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 59.59
Std Dev 2.463
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

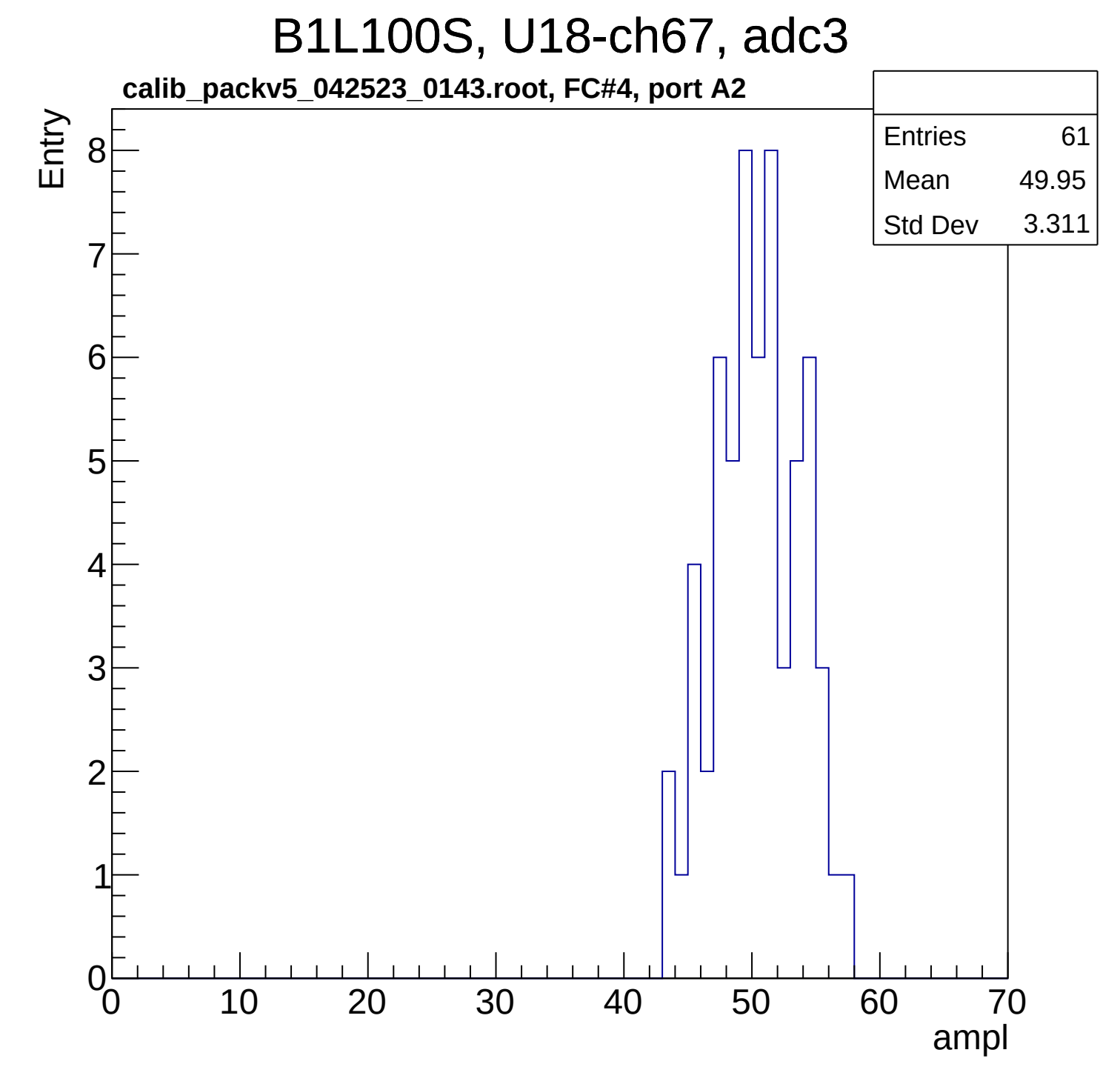

B1L100S, U18-ch66, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 55.22
Std Dev 19.55
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

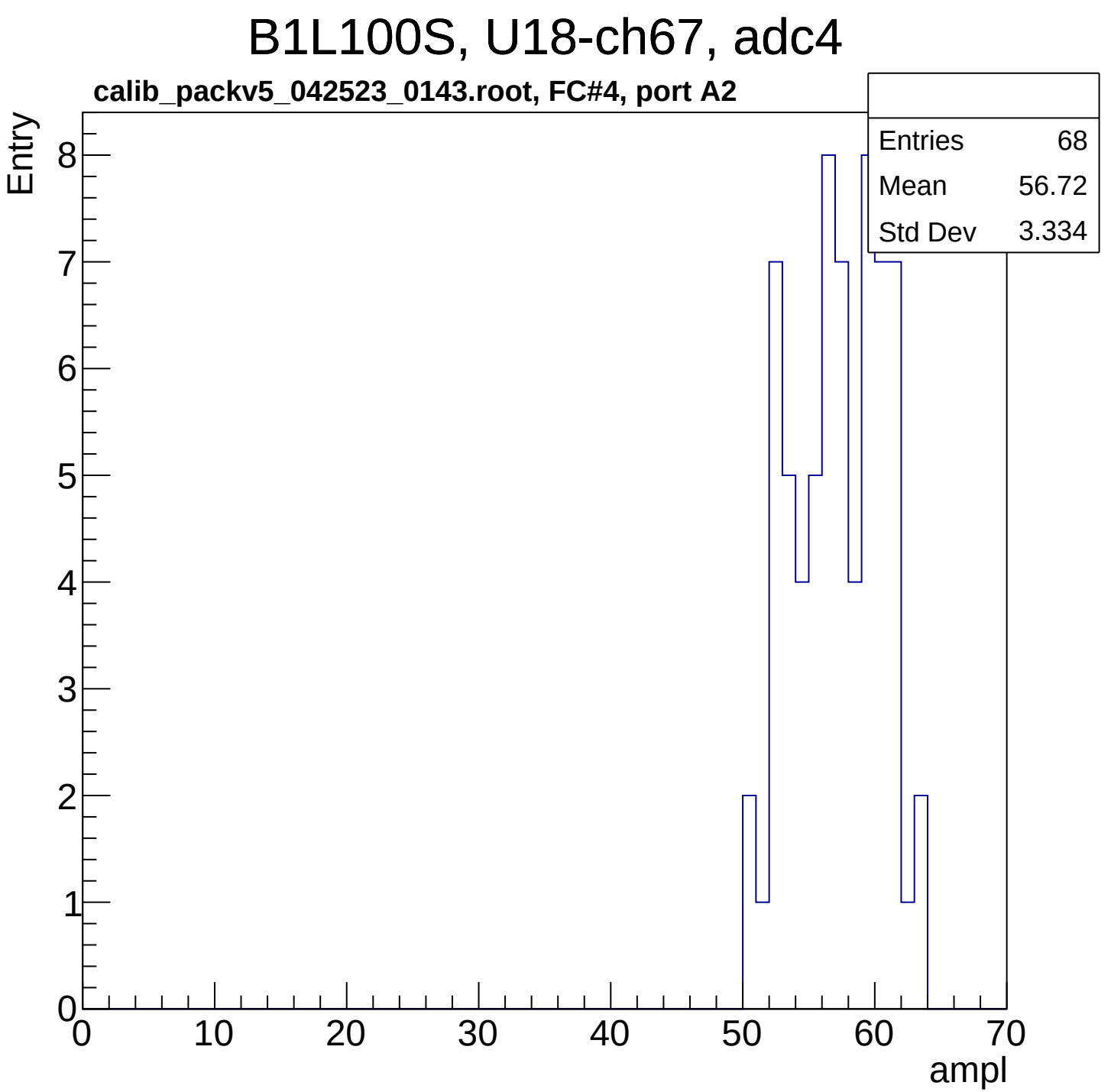

B1L100S, U18-ch66, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 28
Std Dev 26.19
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

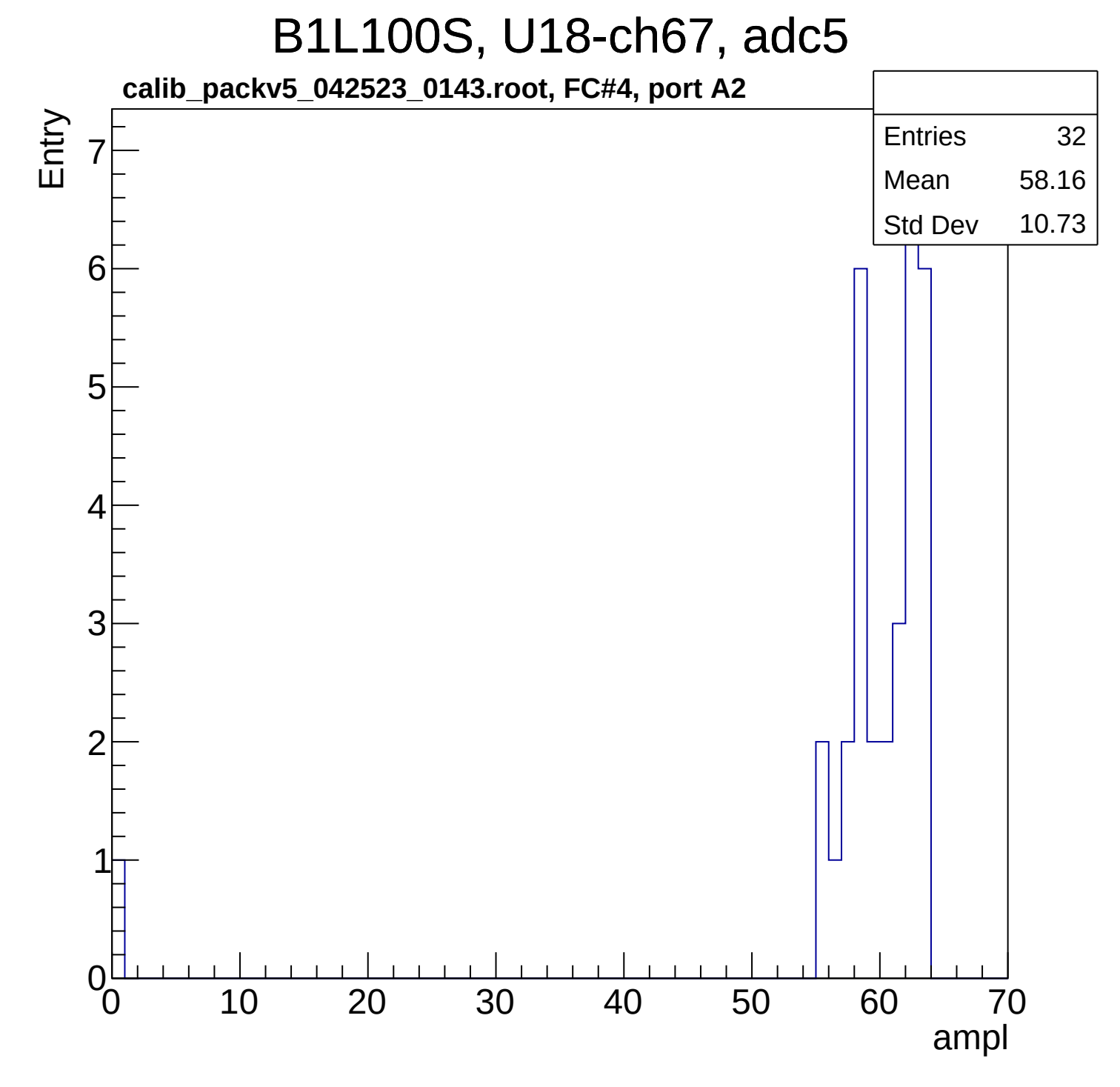

B1L100S, U18-ch67, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 28.86
Std Dev 3.867
Gaus mean : 29.0447
Gaus Width: 3.6002
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

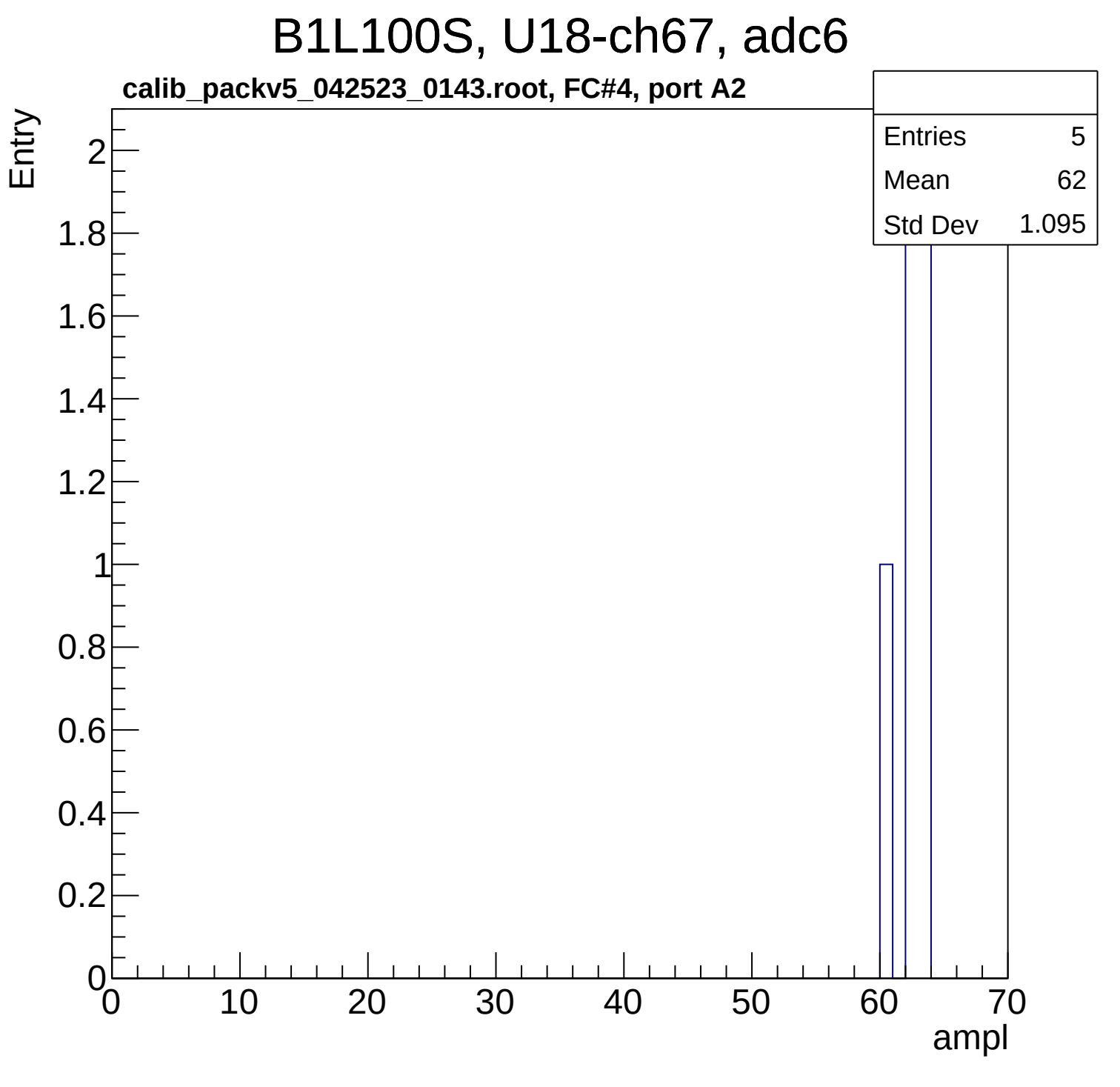

B1L100S, U18-ch67, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 35.65
Std Dev 3.399
Gaus mean : 36.5078
Gaus Width: 3.8276
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

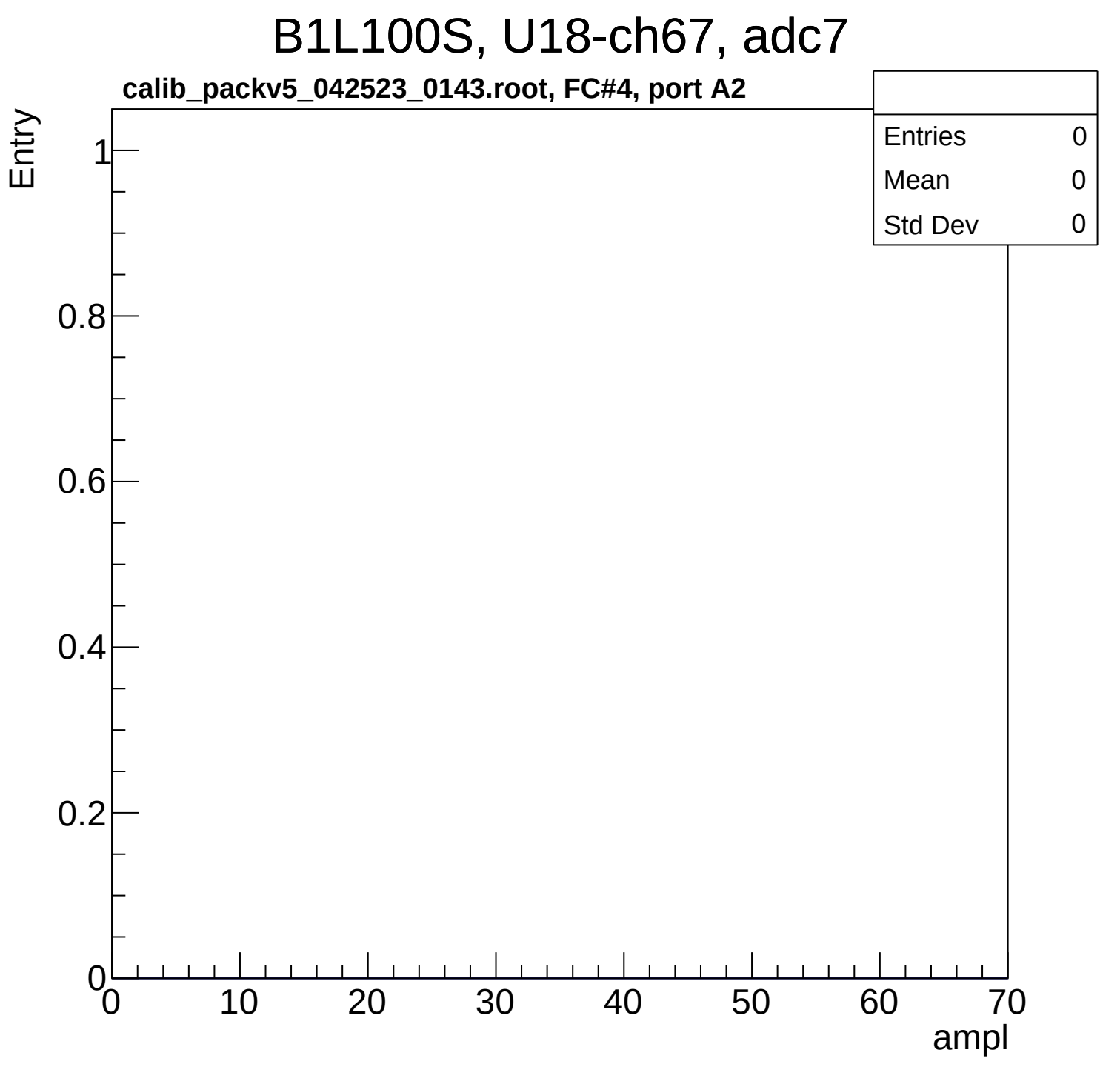

B1L100S, U18-ch67, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 43.53
Std Dev 3.384
Gaus mean : 43.9895
Gaus Width: 3.6768
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

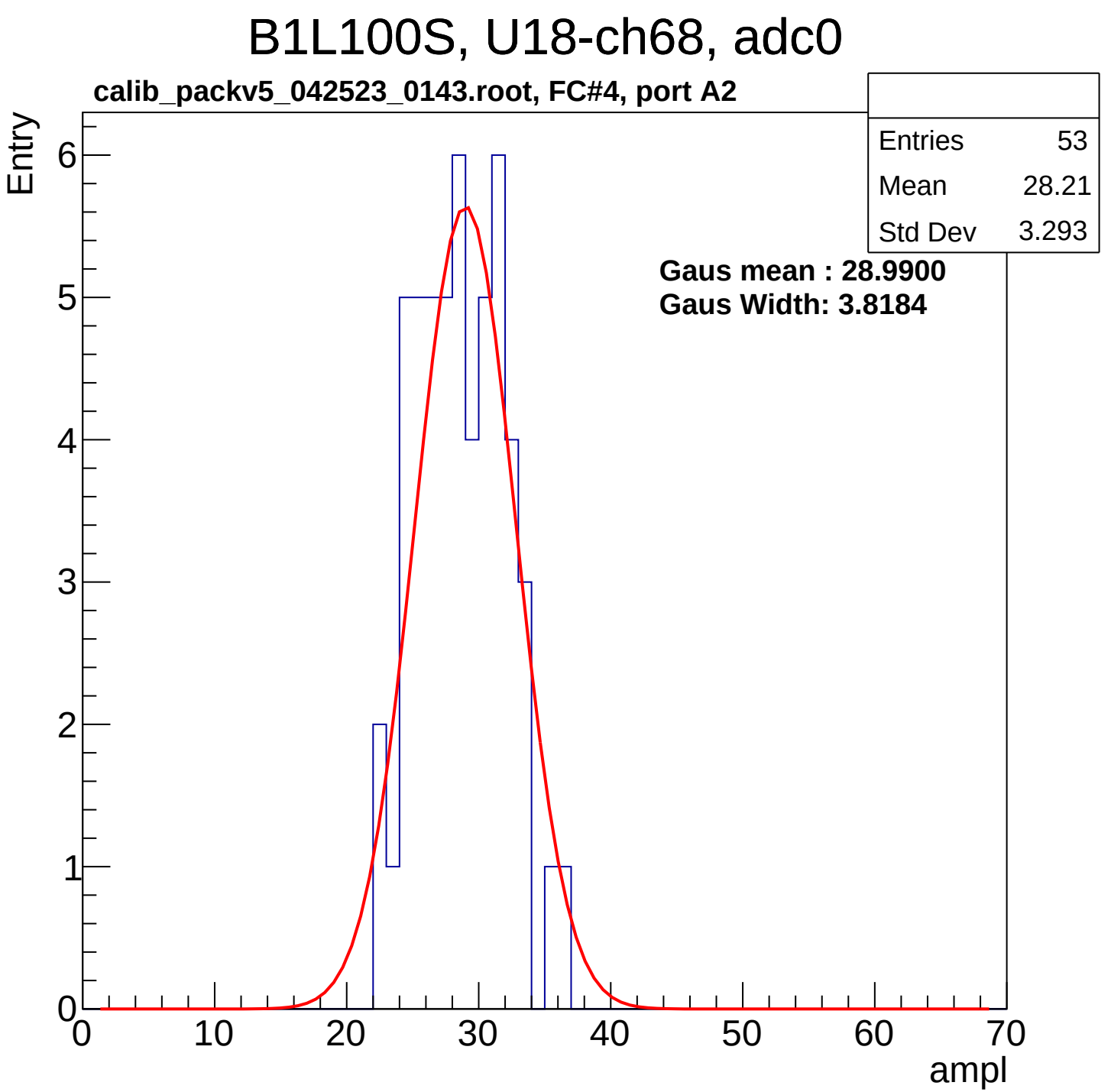

B1L100S, U18-ch67, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 49.95
Std Dev 3.311
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

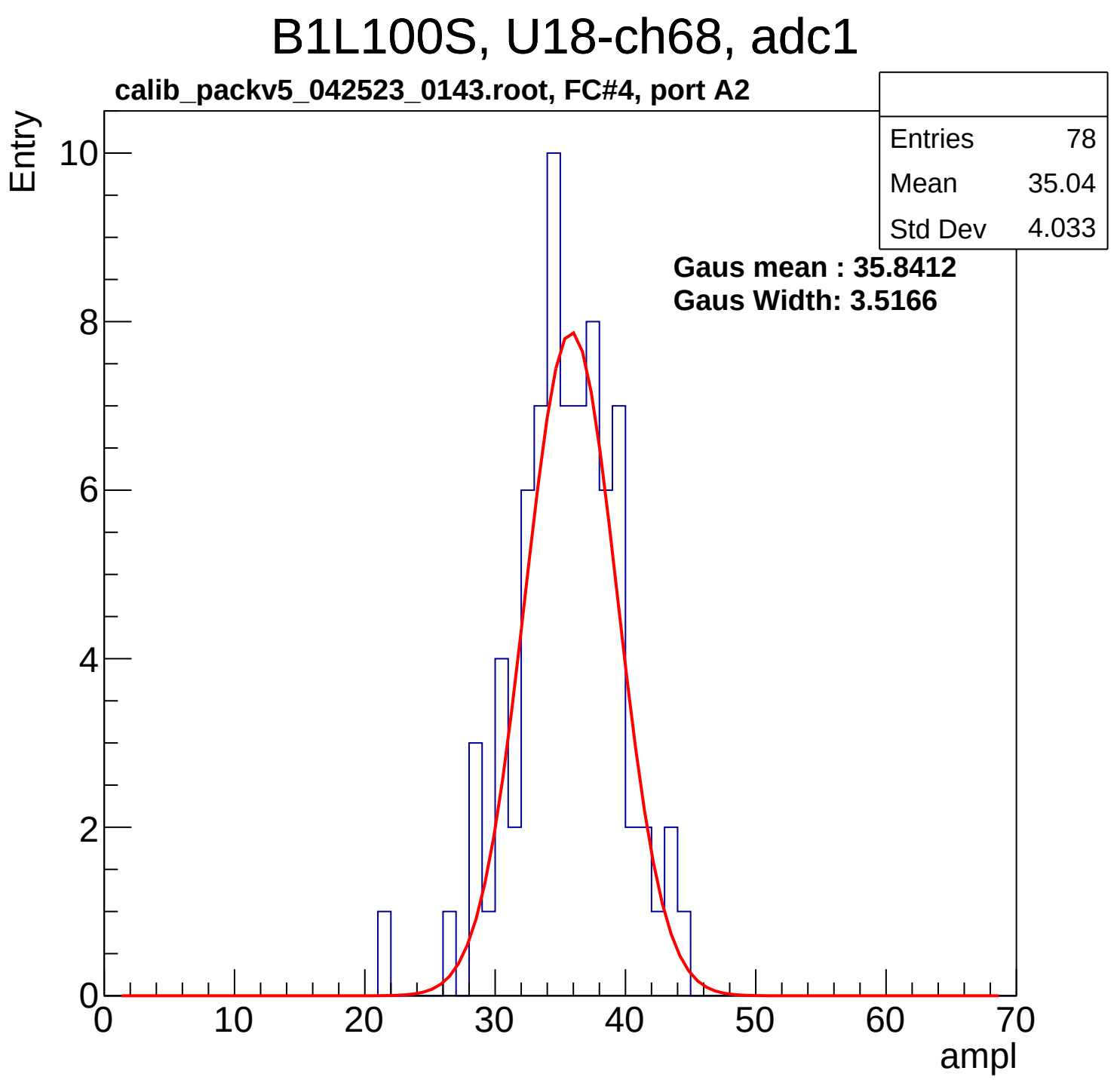

B1L100S, U18-ch67, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 56.72
Std Dev 3.334
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

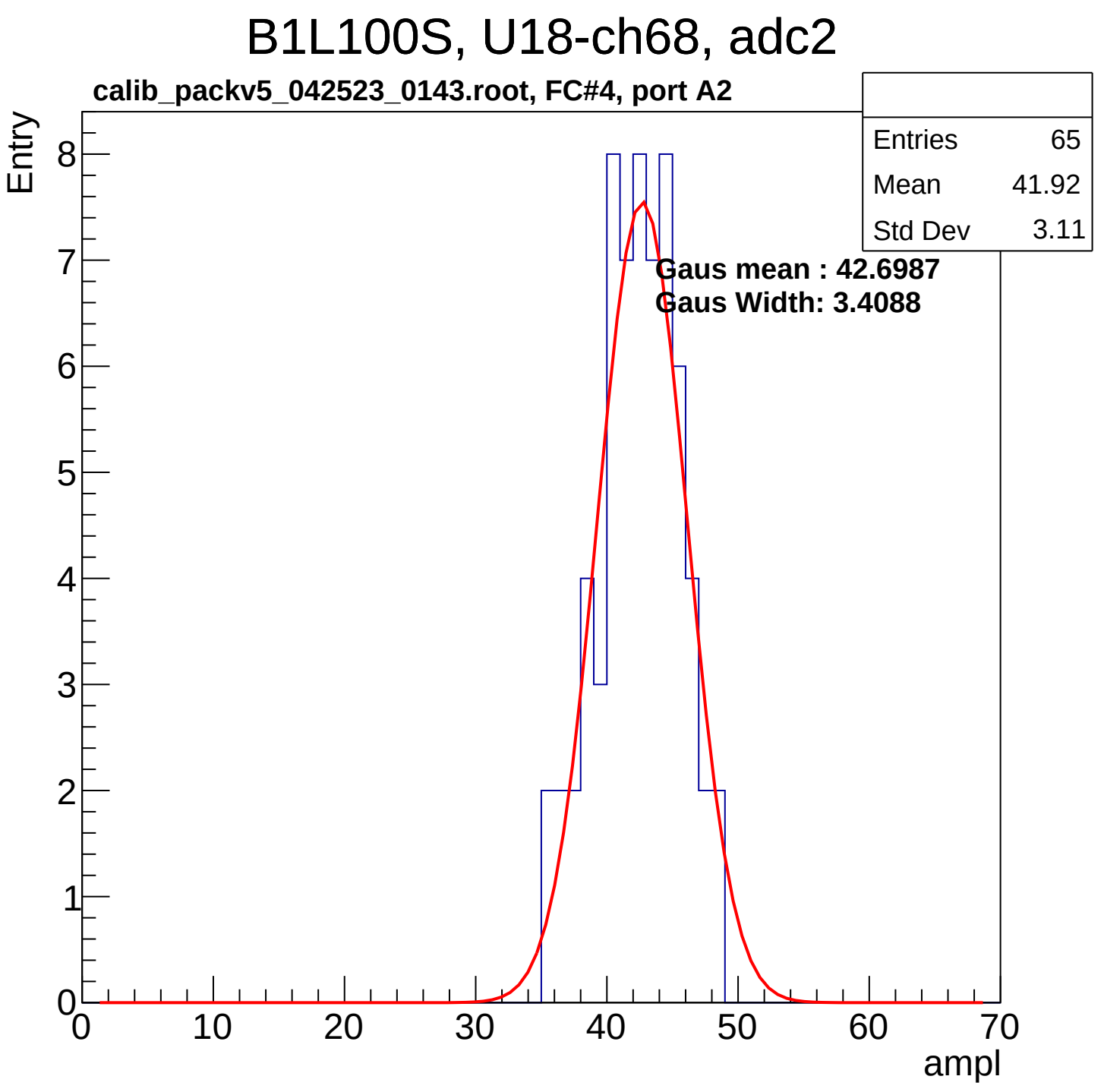

B1L100S, U18-ch67, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 32
Mean 58.16
Std Dev 10.73
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

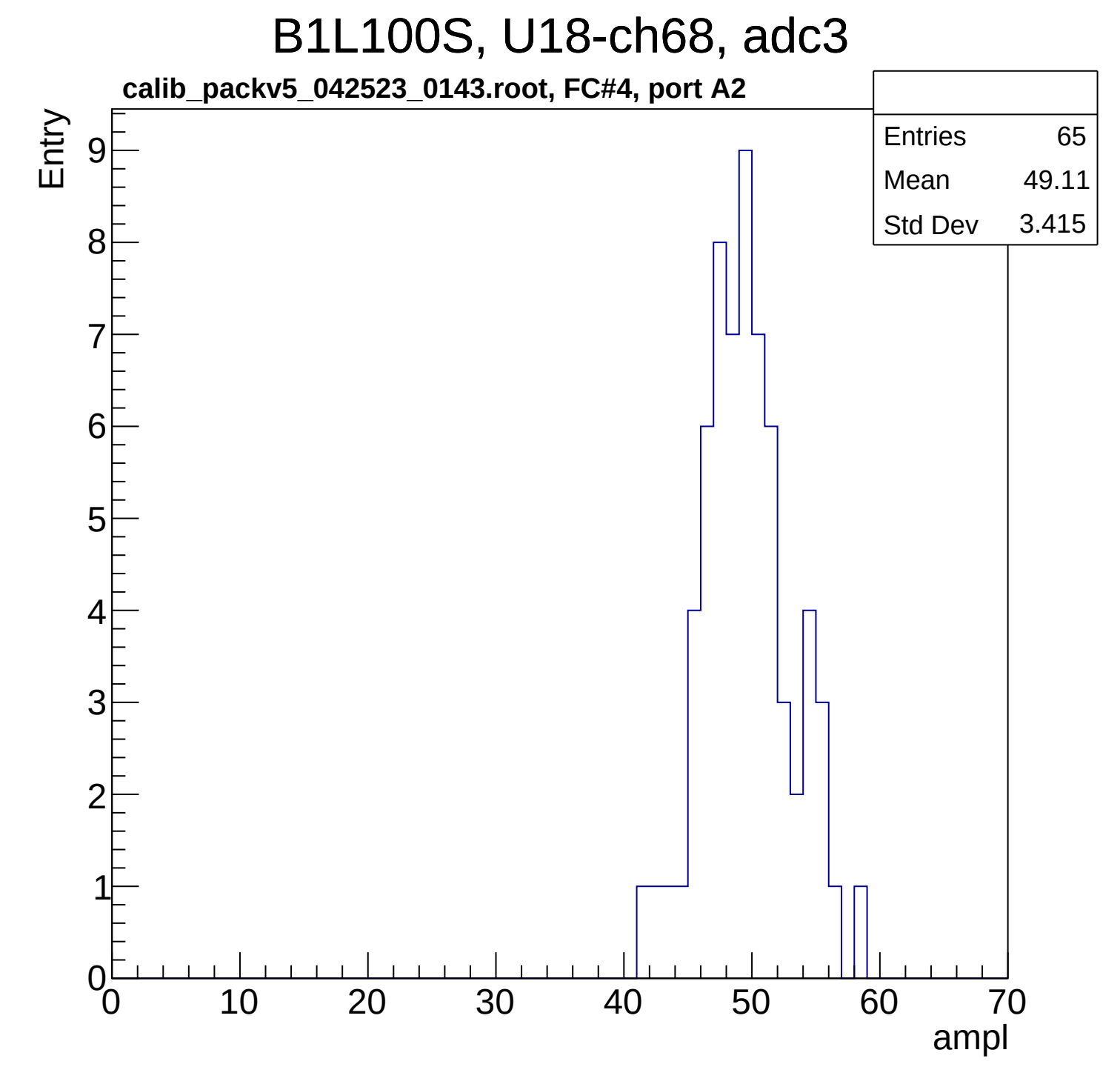

B1L100S, U18-ch67, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 5
Mean 62
Std Dev 1.095
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

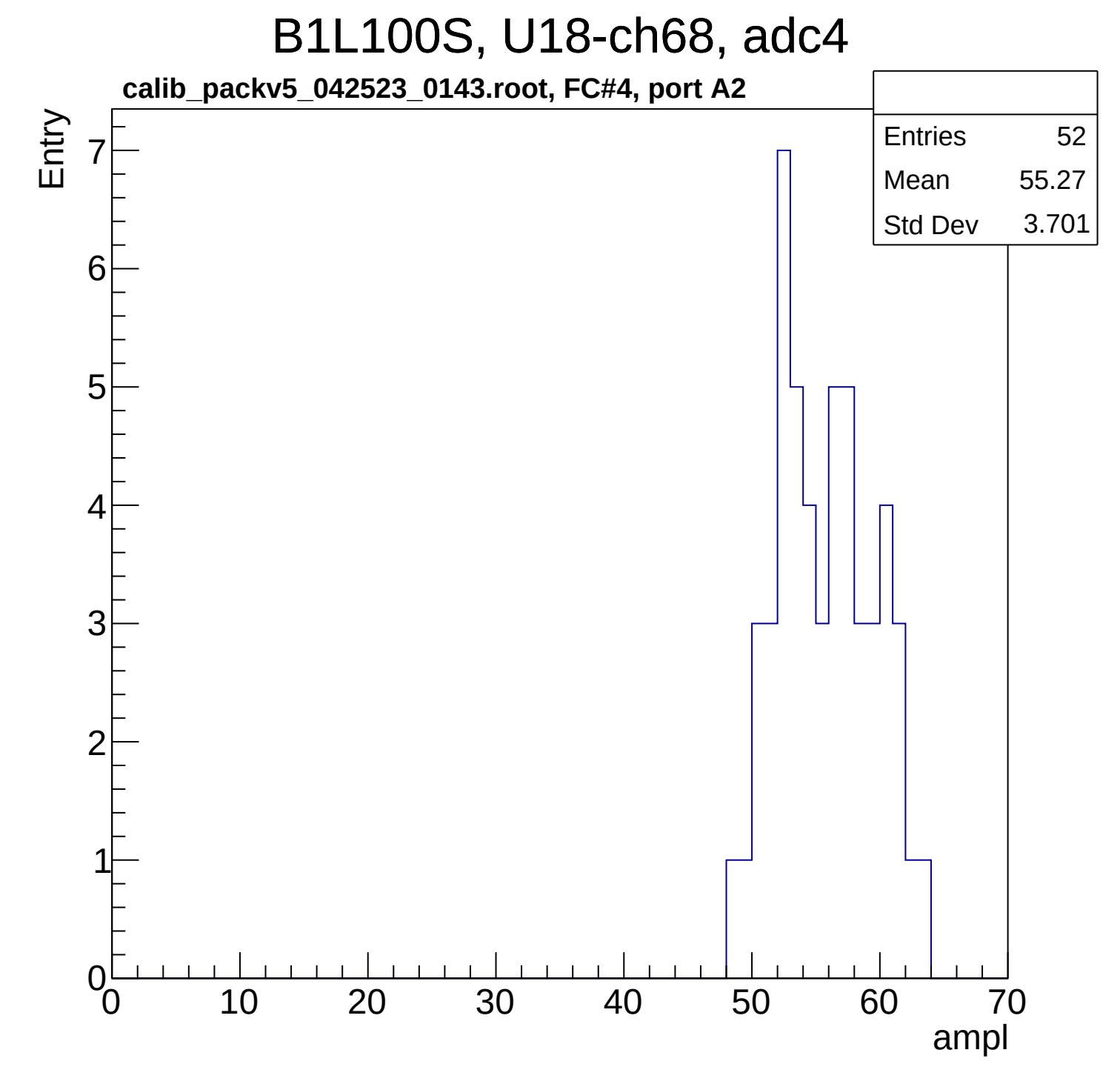

B1L100S, U18-ch67, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

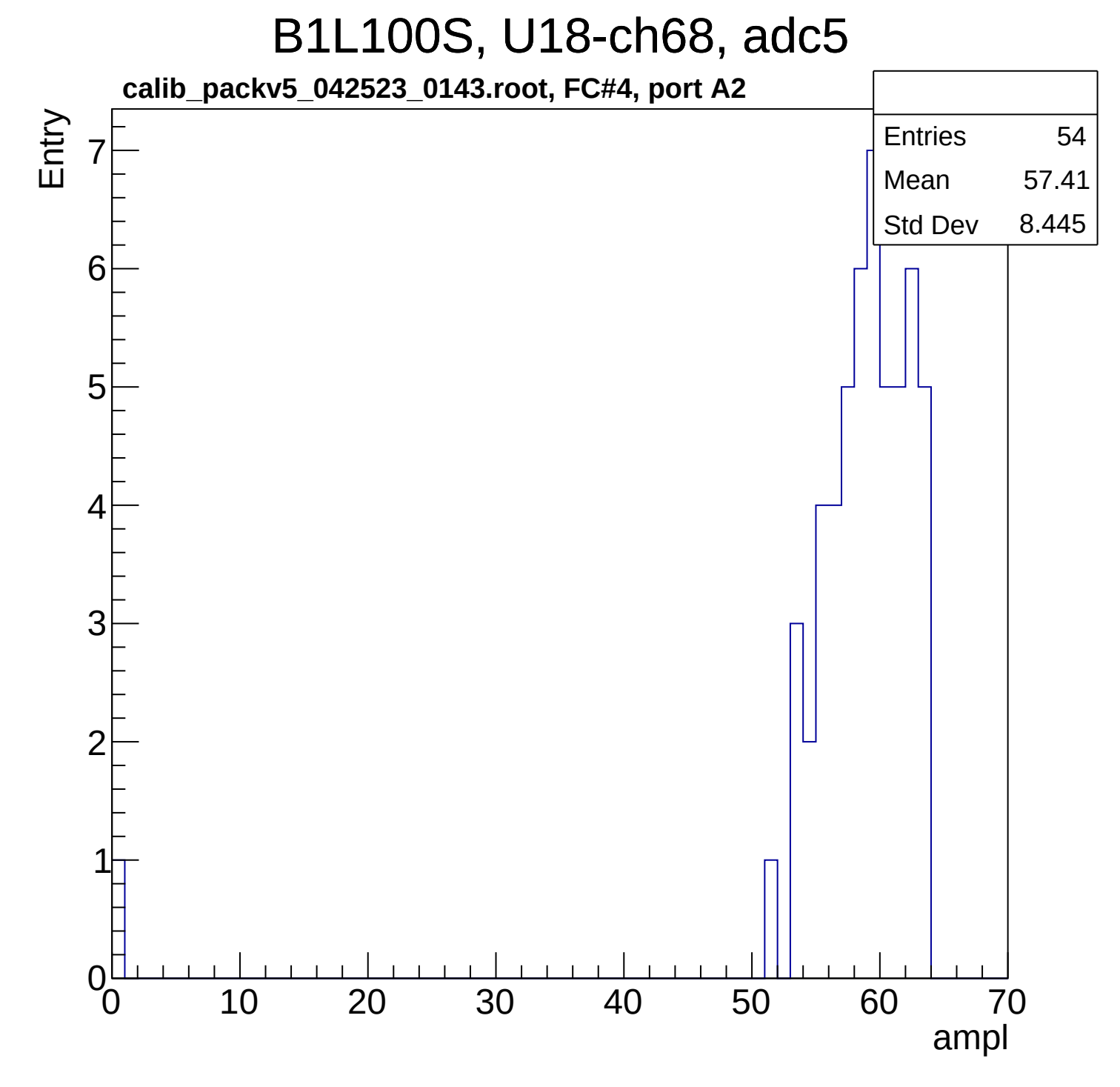

B1L100S, U18-ch68, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 28.21
Std Dev 3.293
Gaus mean : 28.9900
Gaus Width: 3.8184
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

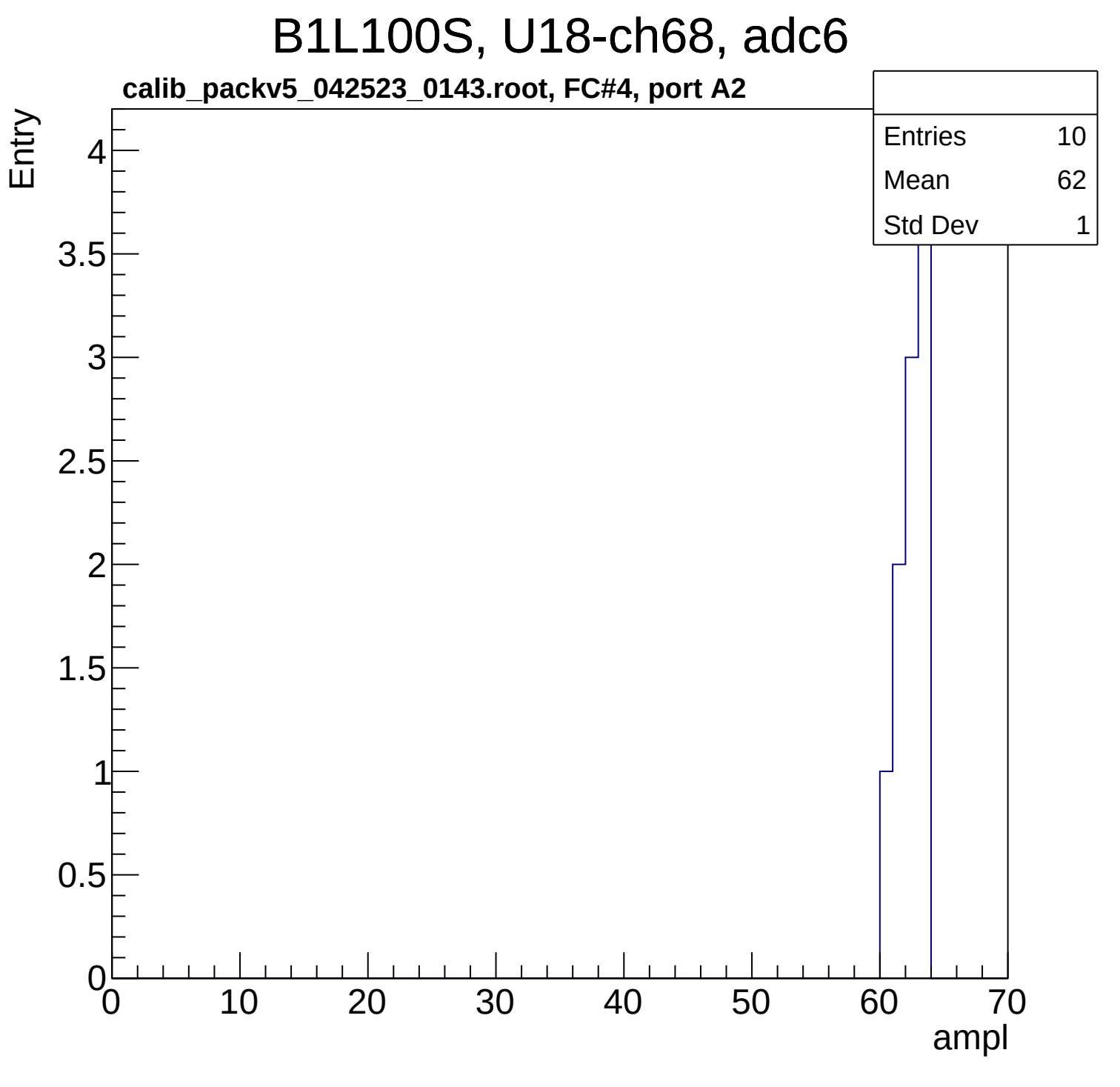

B1L100S, U18-ch68, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 35.04
Std Dev 4.033
Gaus mean : 35.8412
Gaus Width: 3.5166
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

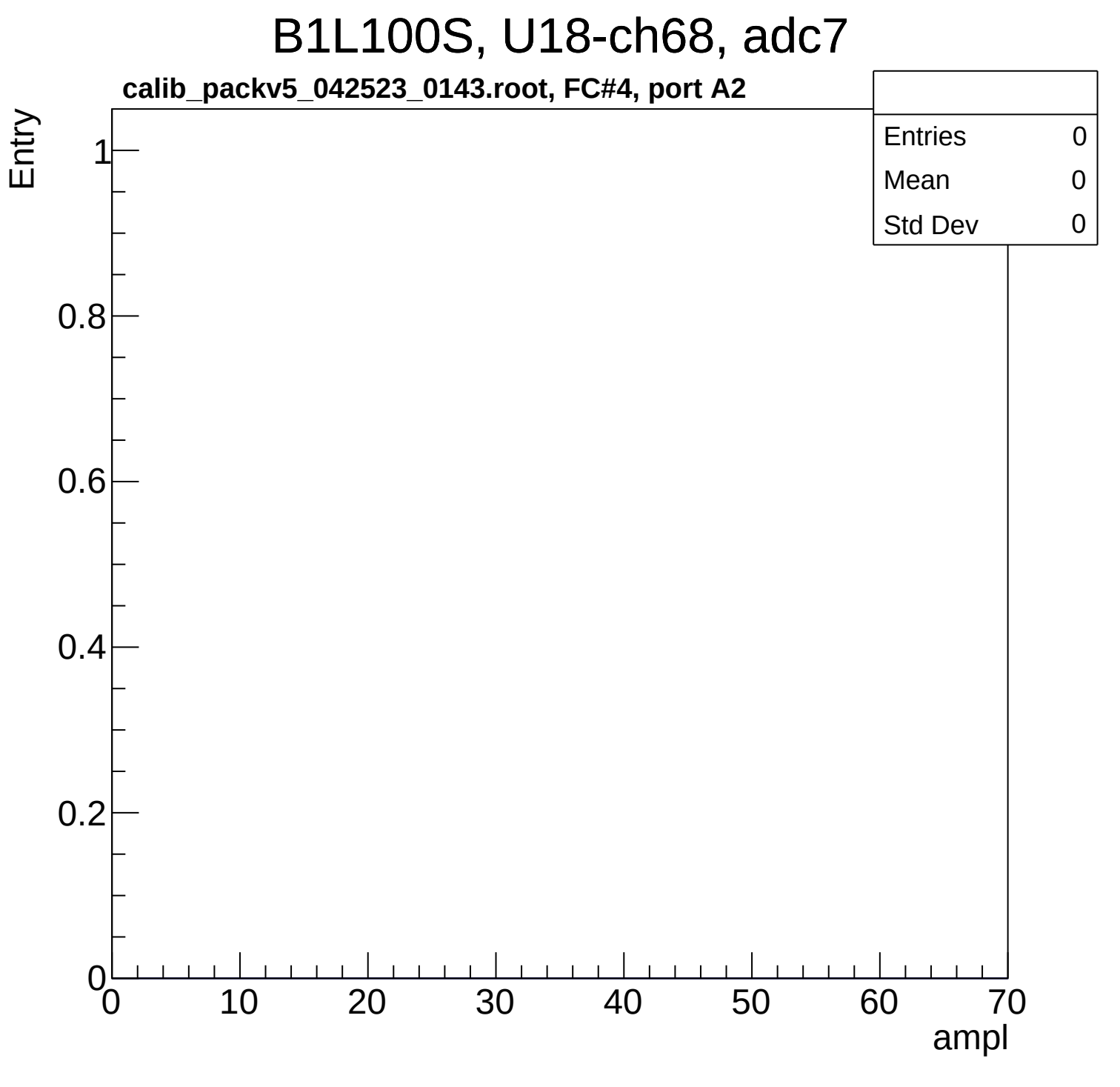

B1L100S, U18-ch68, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 41.92
Std Dev 3.11
Gaus mean : 42.6987
Gaus Width: 3.4088
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

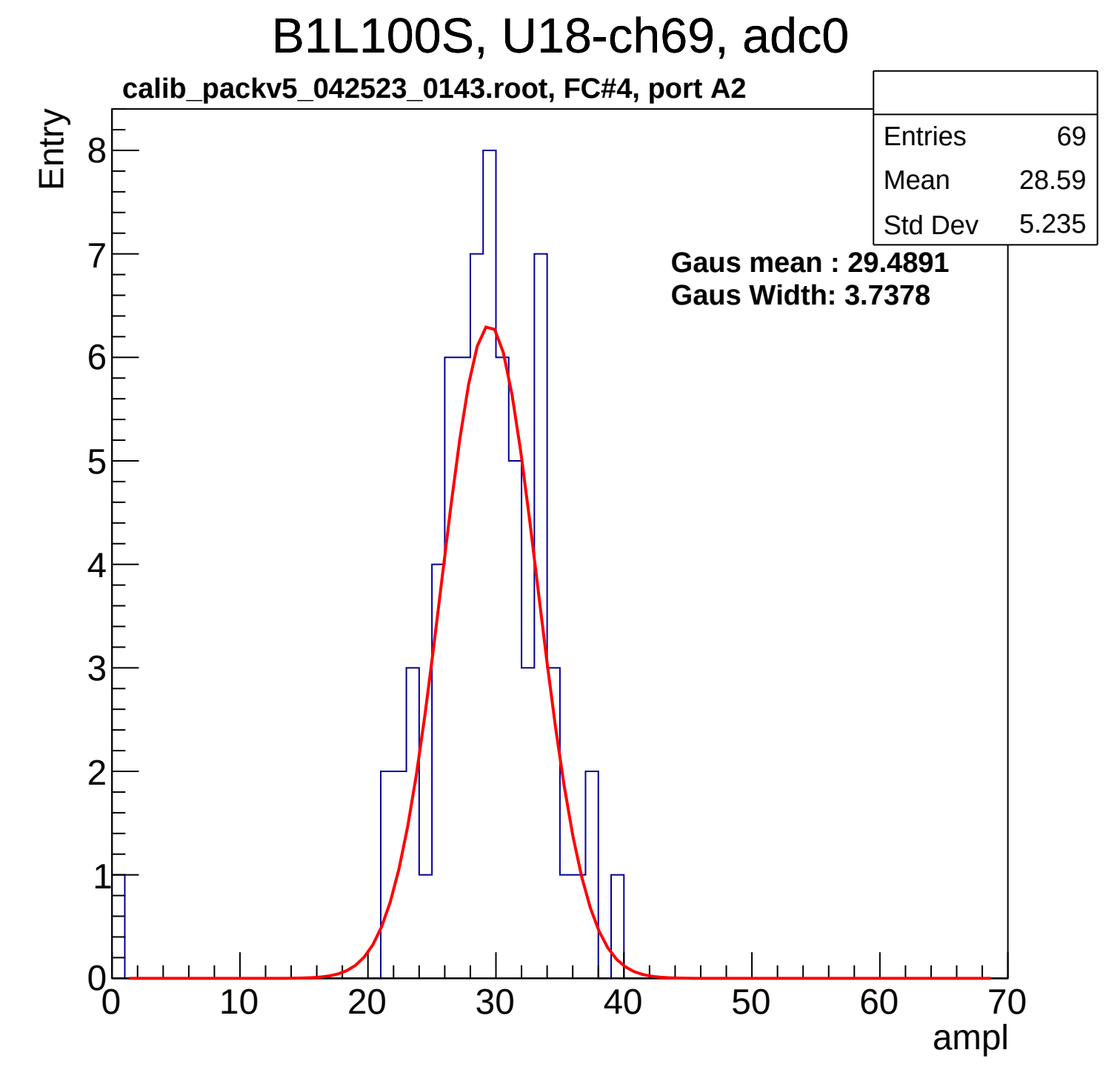

B1L100S, U18-ch68, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 49.11
Std Dev 3.415
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

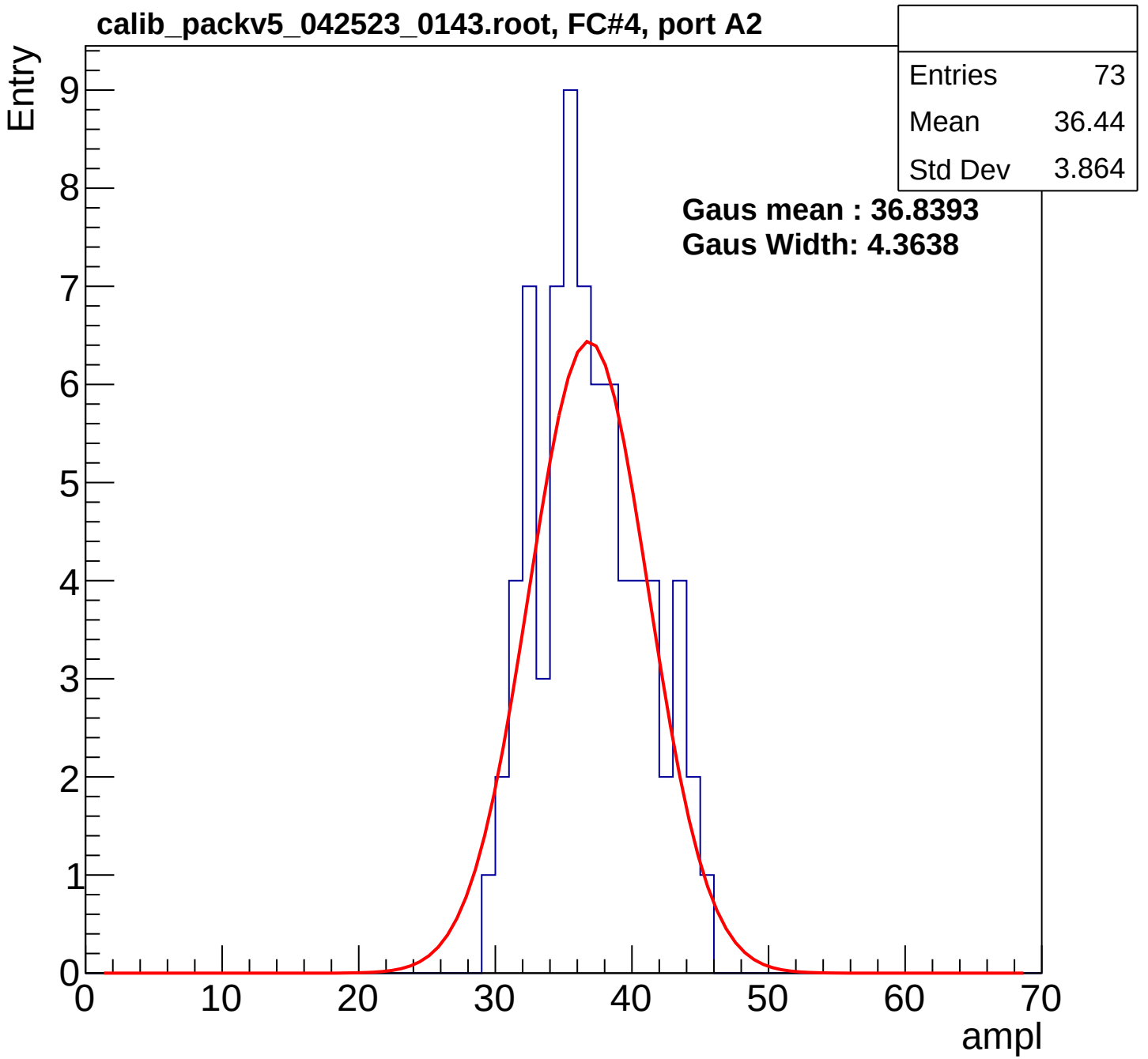

B1L100S, U18-ch68, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 55.27
Std Dev 3.701
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

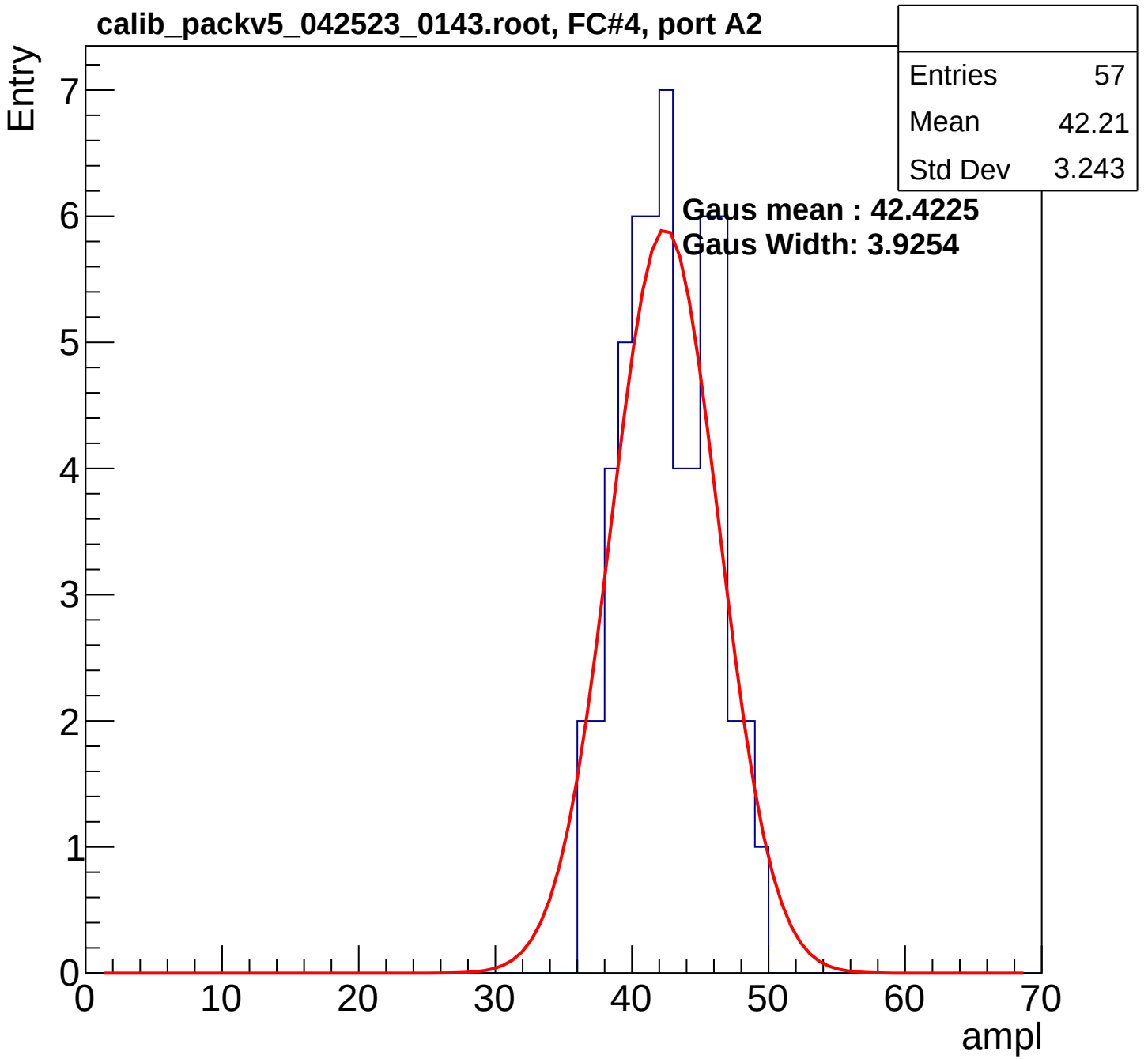

B1L100S, U18-ch68, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 57.41
Std Dev 8.445
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

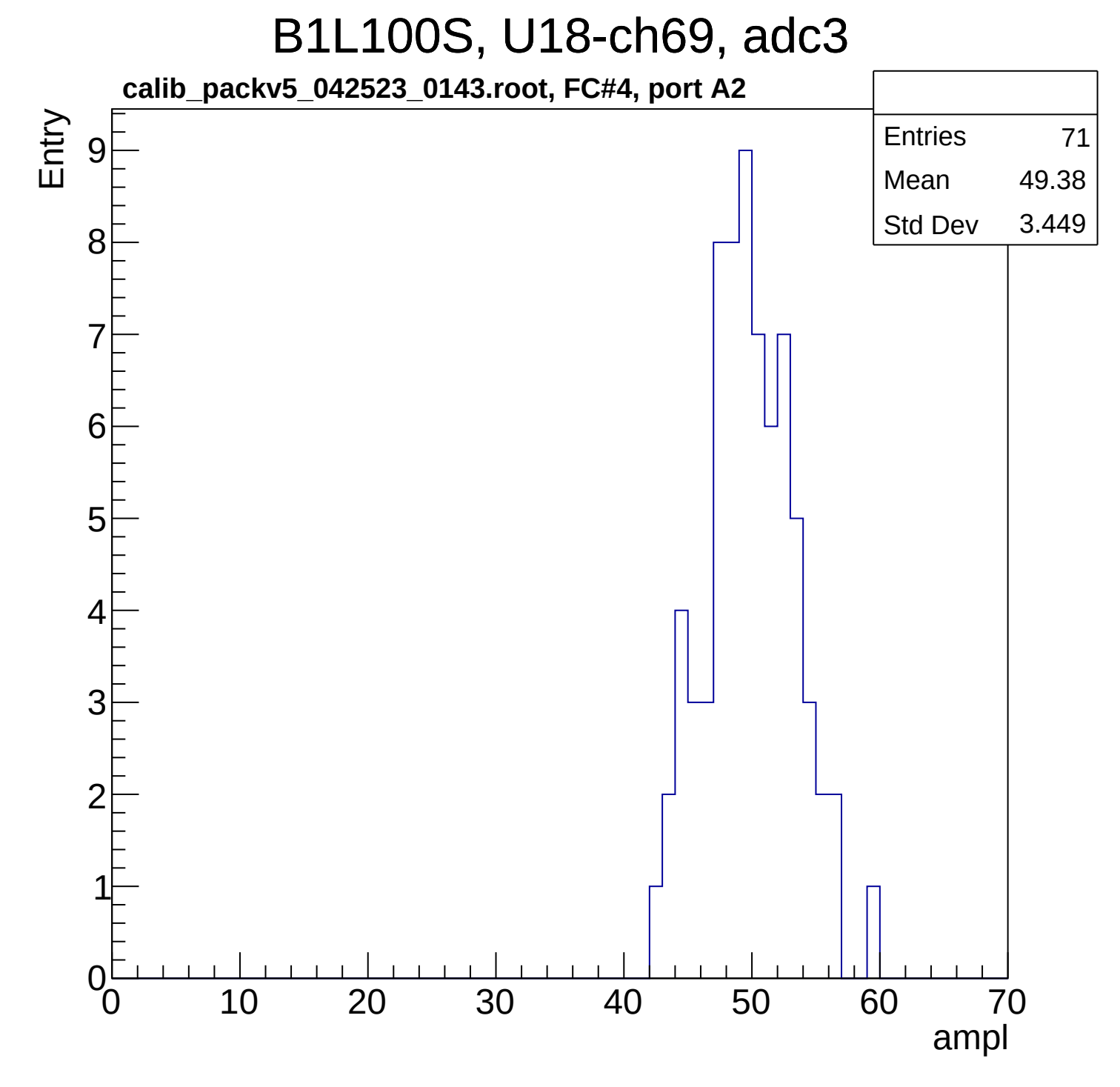

B1L100S, U18-ch68, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 62
Std Dev 1
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

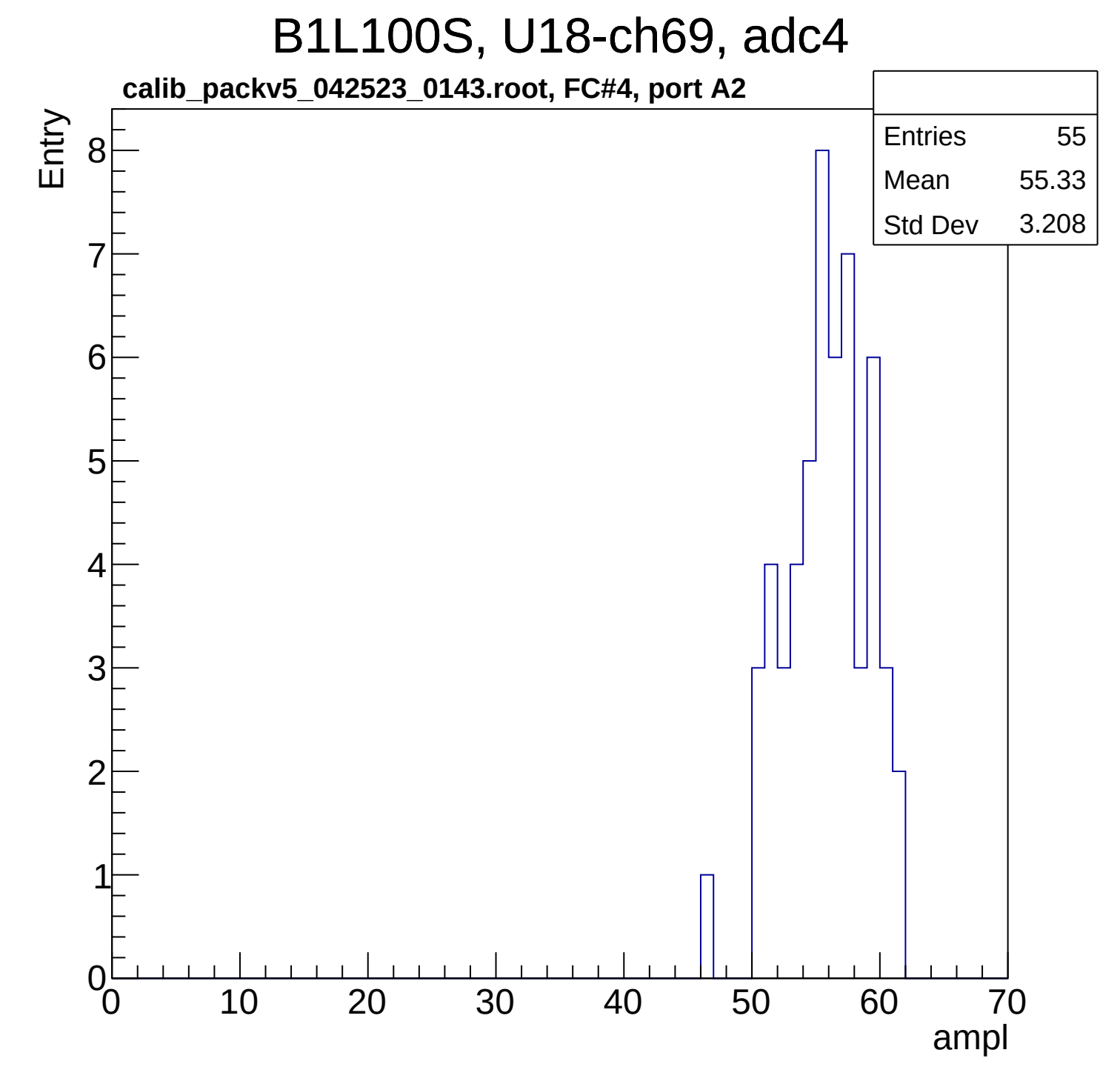

B1L100S, U18-ch68, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

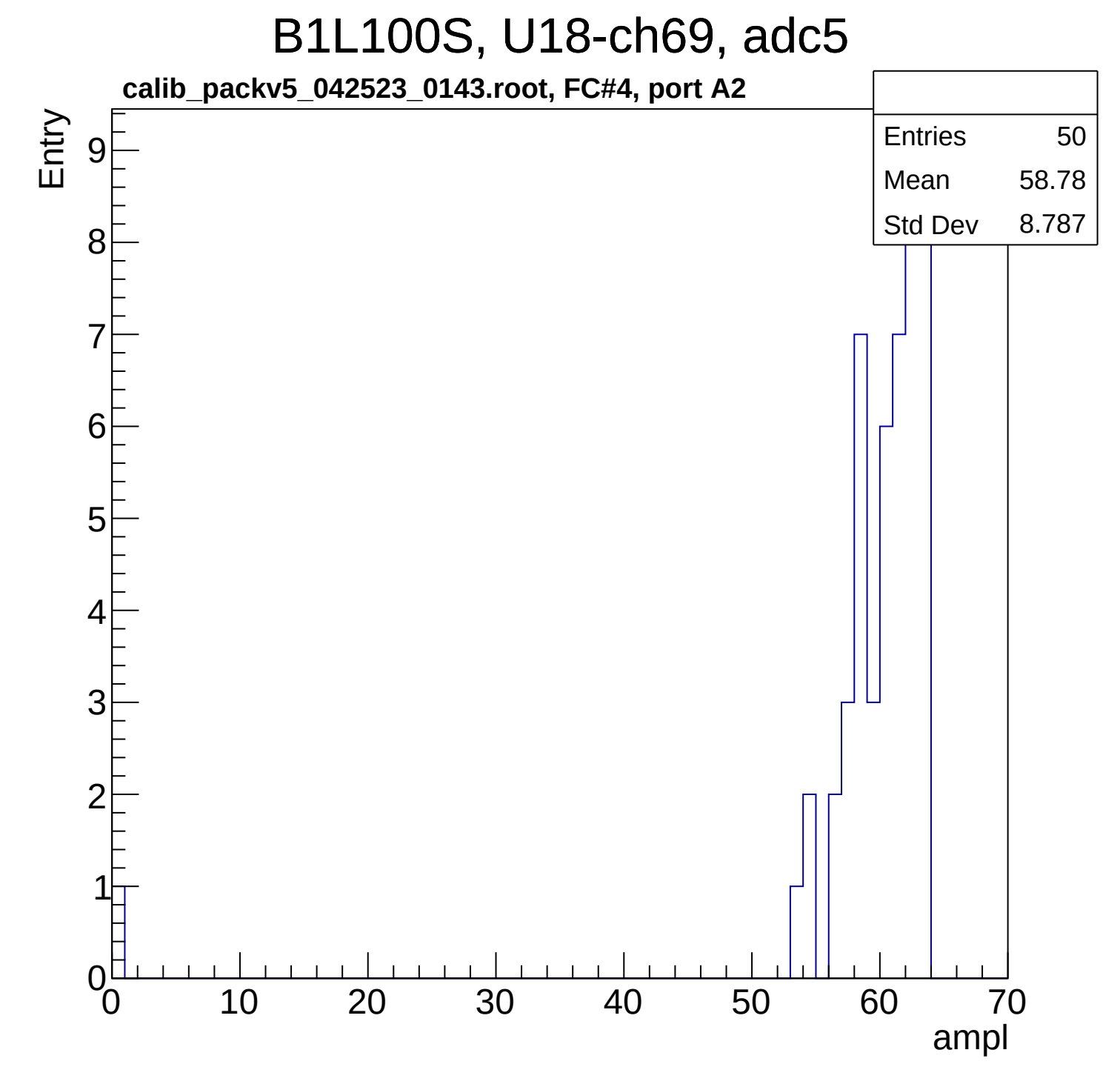

B1L100S, U18-ch69, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 28.59
Std Dev 5.235
Gaus mean : 29.4891
Gaus Width: 3.7378
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

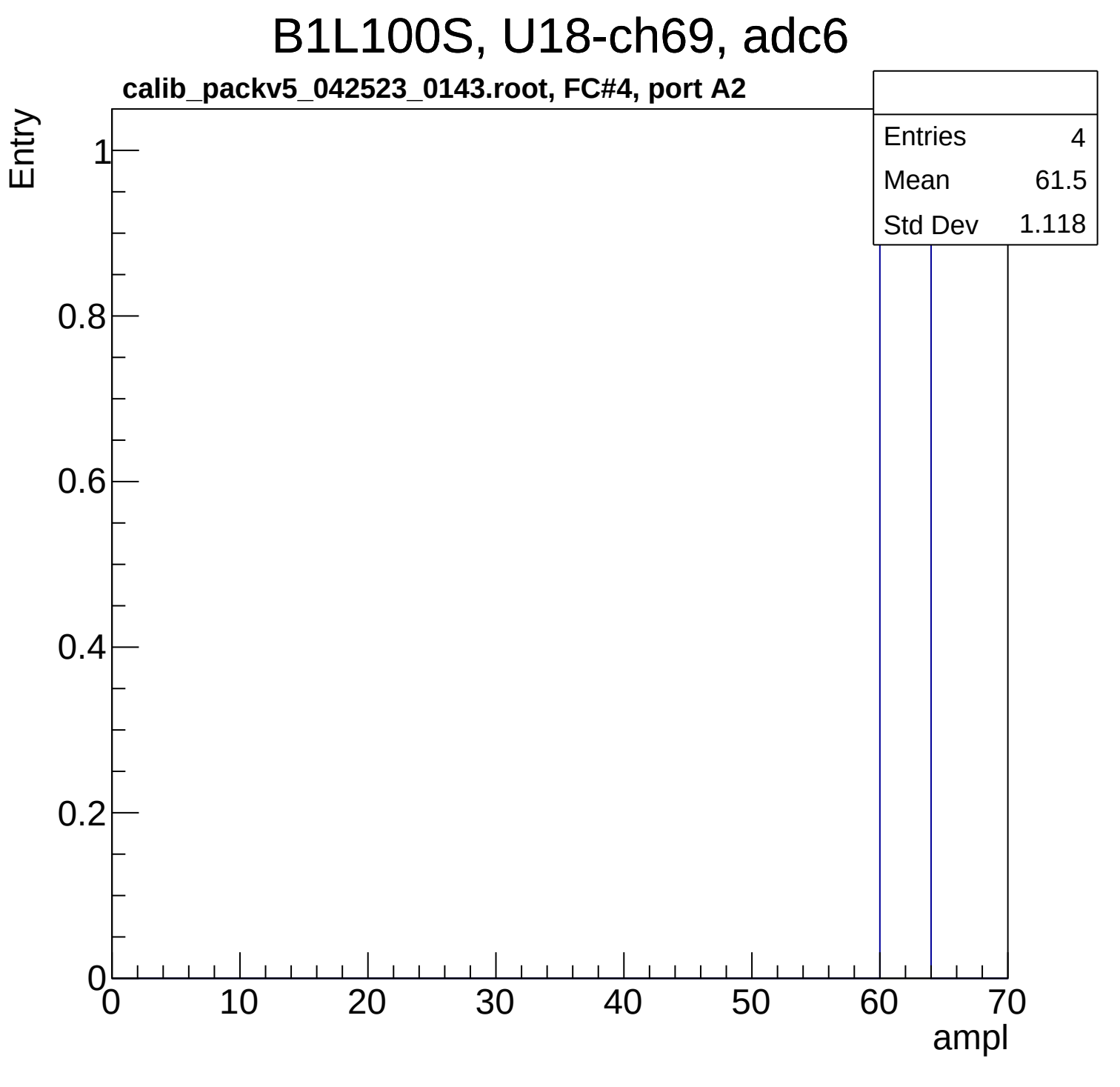

B1L100S, U18-ch69, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 36.44
Std Dev 3.864
Gaus mean : 36.8393
Gaus Width: 4.3638
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

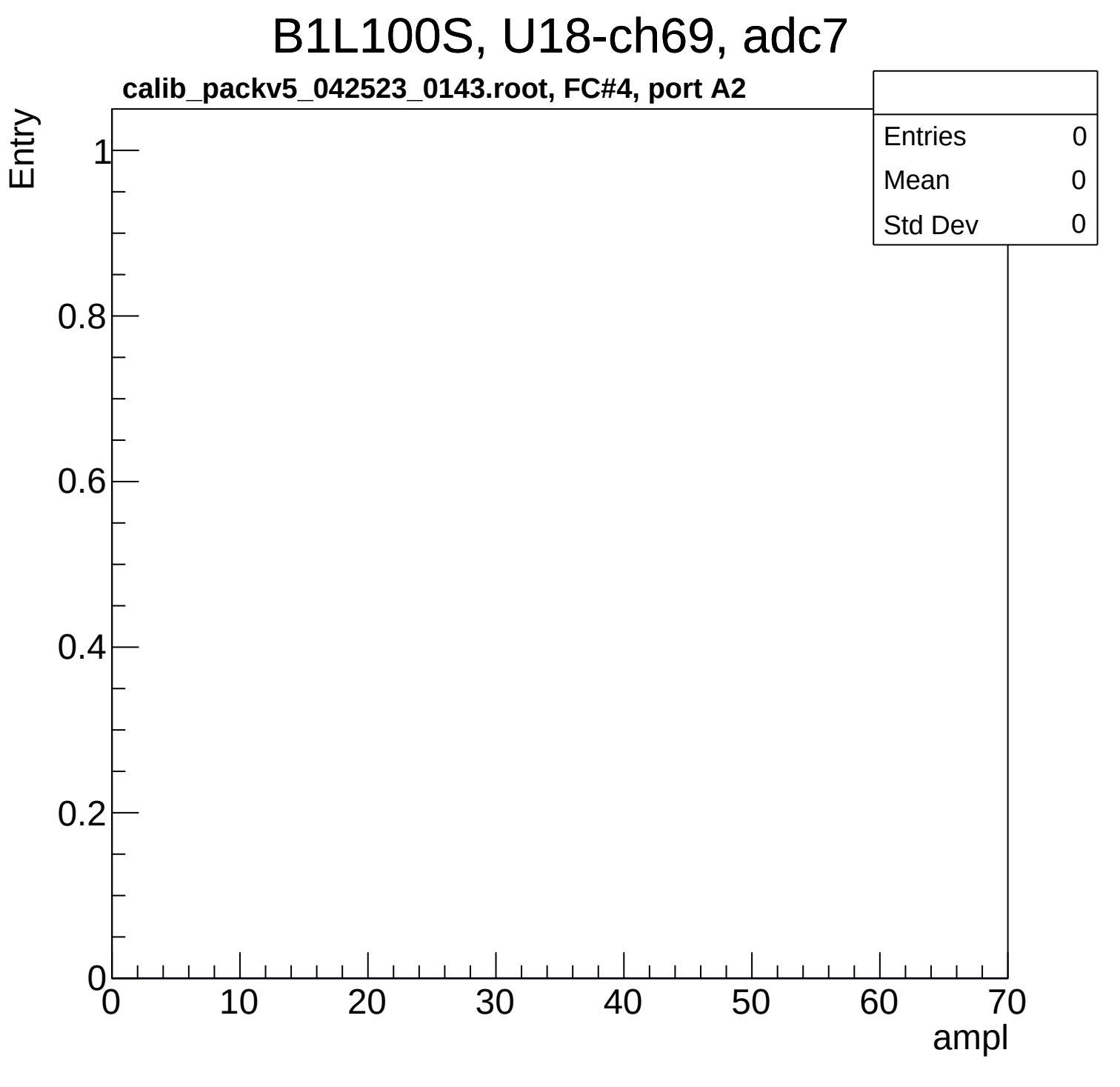

B1L100S, U18-ch69, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 42.21
Std Dev 3.243
Gaus mean : 42.4225
Gaus Width: 3.9254
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

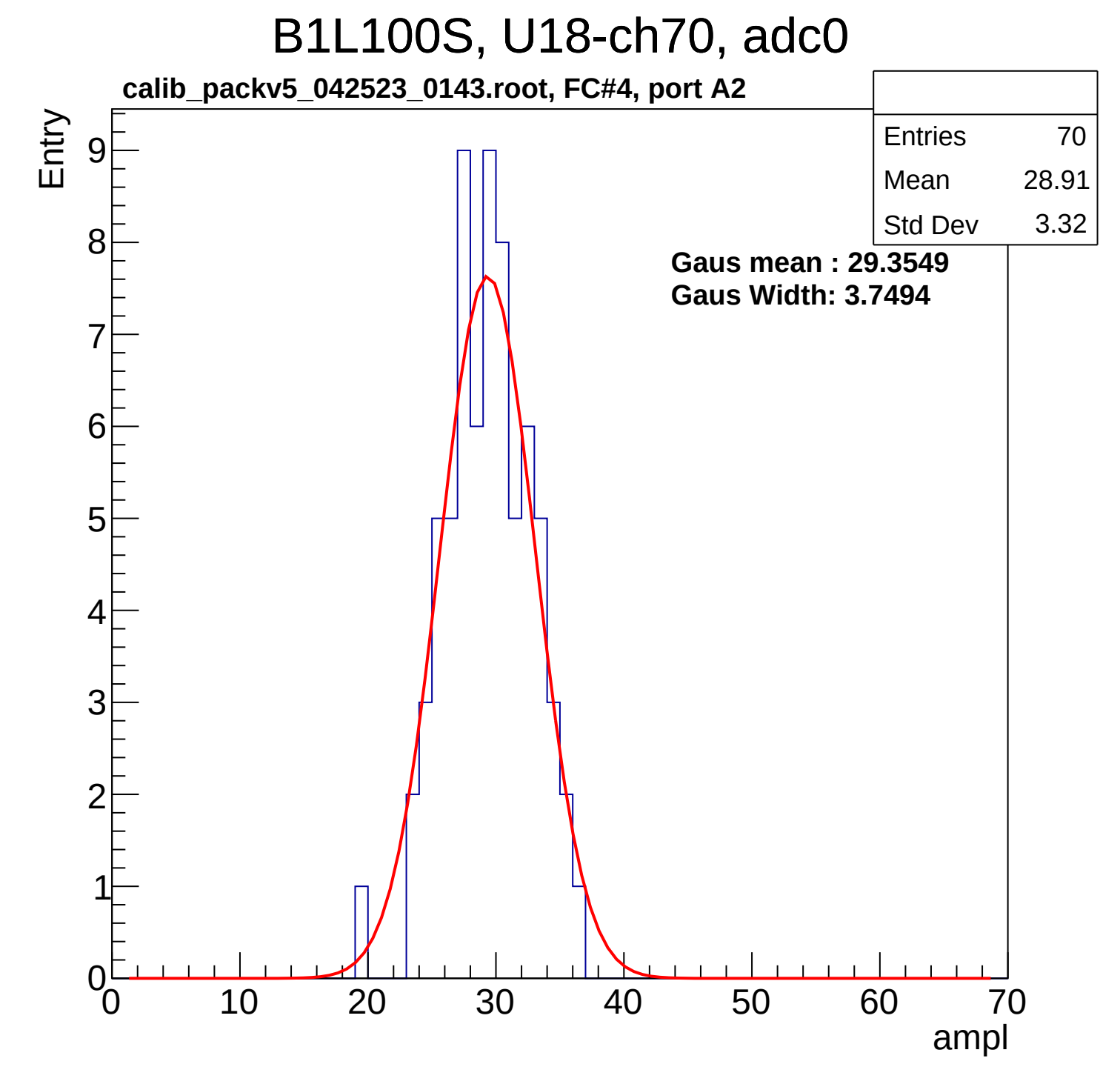

B1L100S, U18-ch69, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 49.38
Std Dev 3.449
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

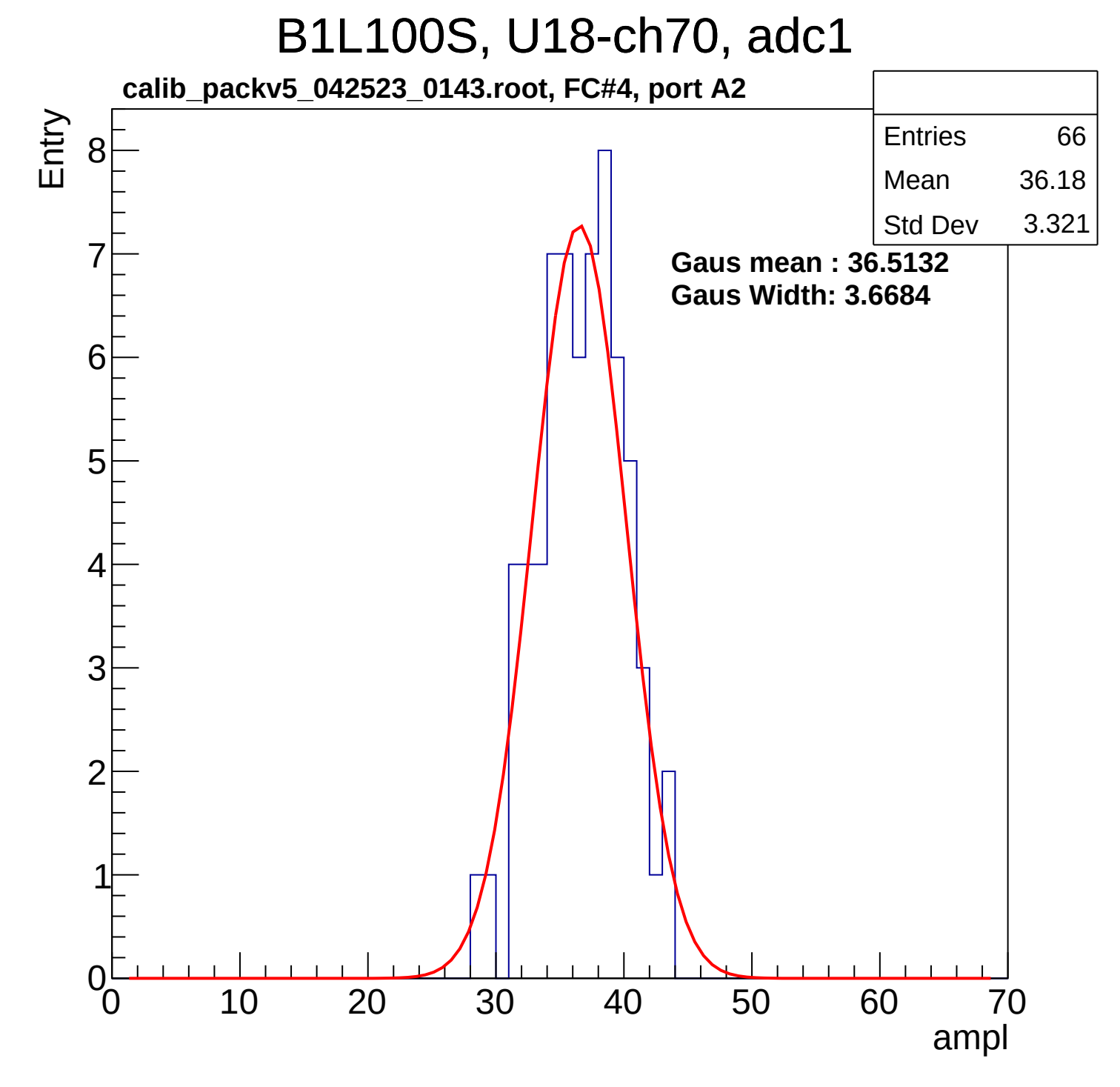

B1L100S, U18-ch69, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 55.33
Std Dev 3.208
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

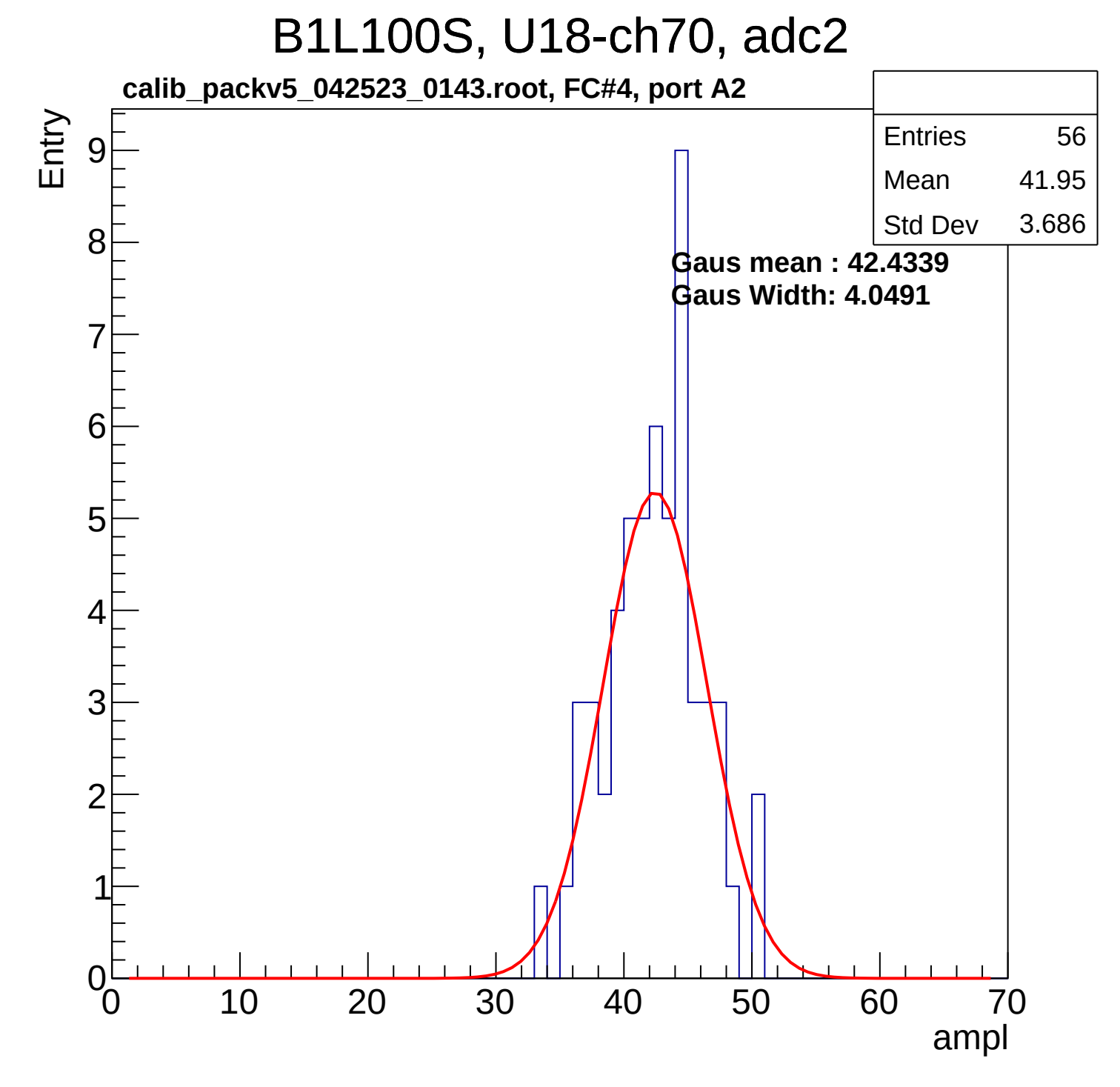

B1L100S, U18-ch69, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 58.78
Std Dev 8.787
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

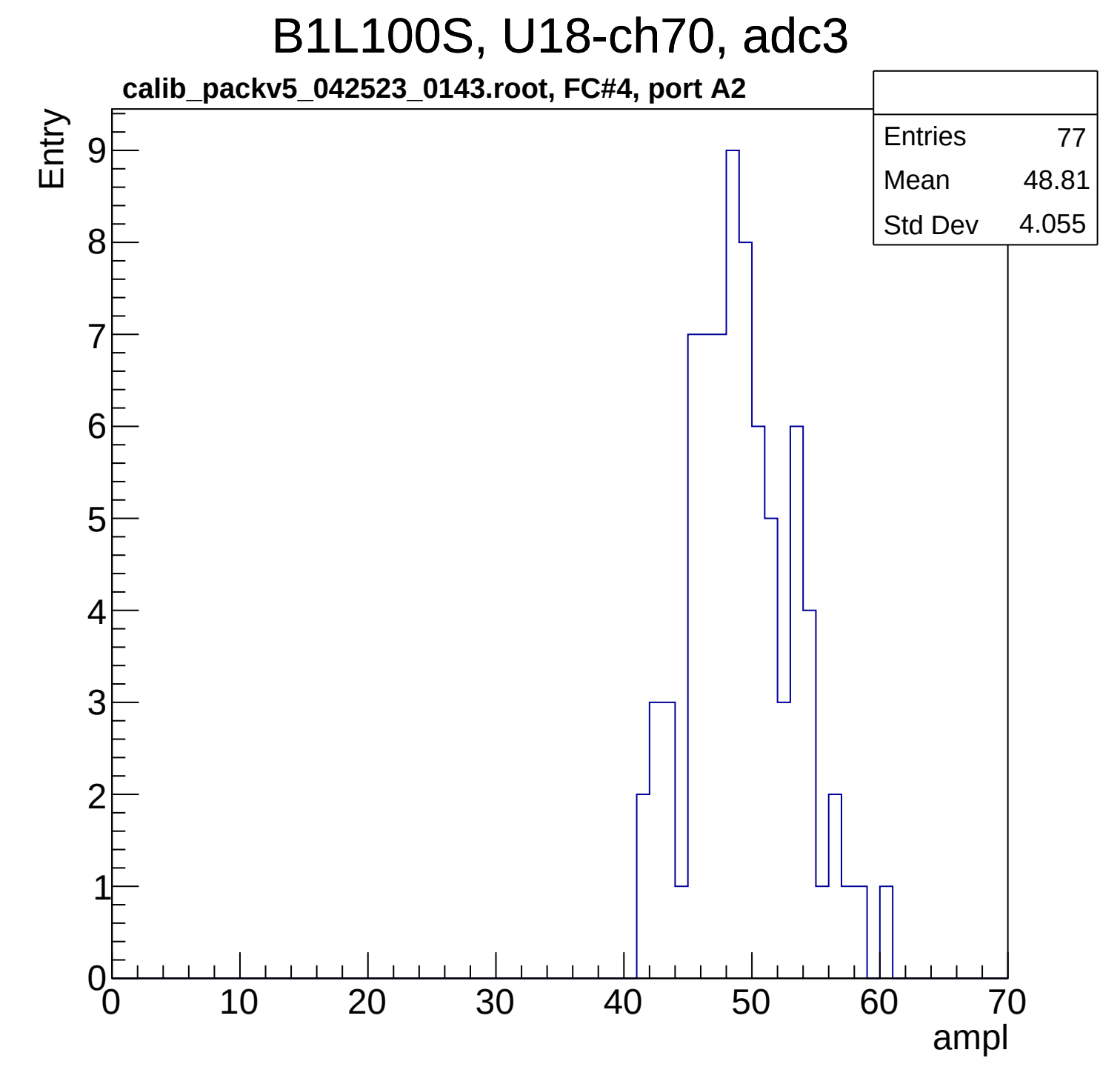

B1L100S, U18-ch69, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 61.5
Std Dev 1.118
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

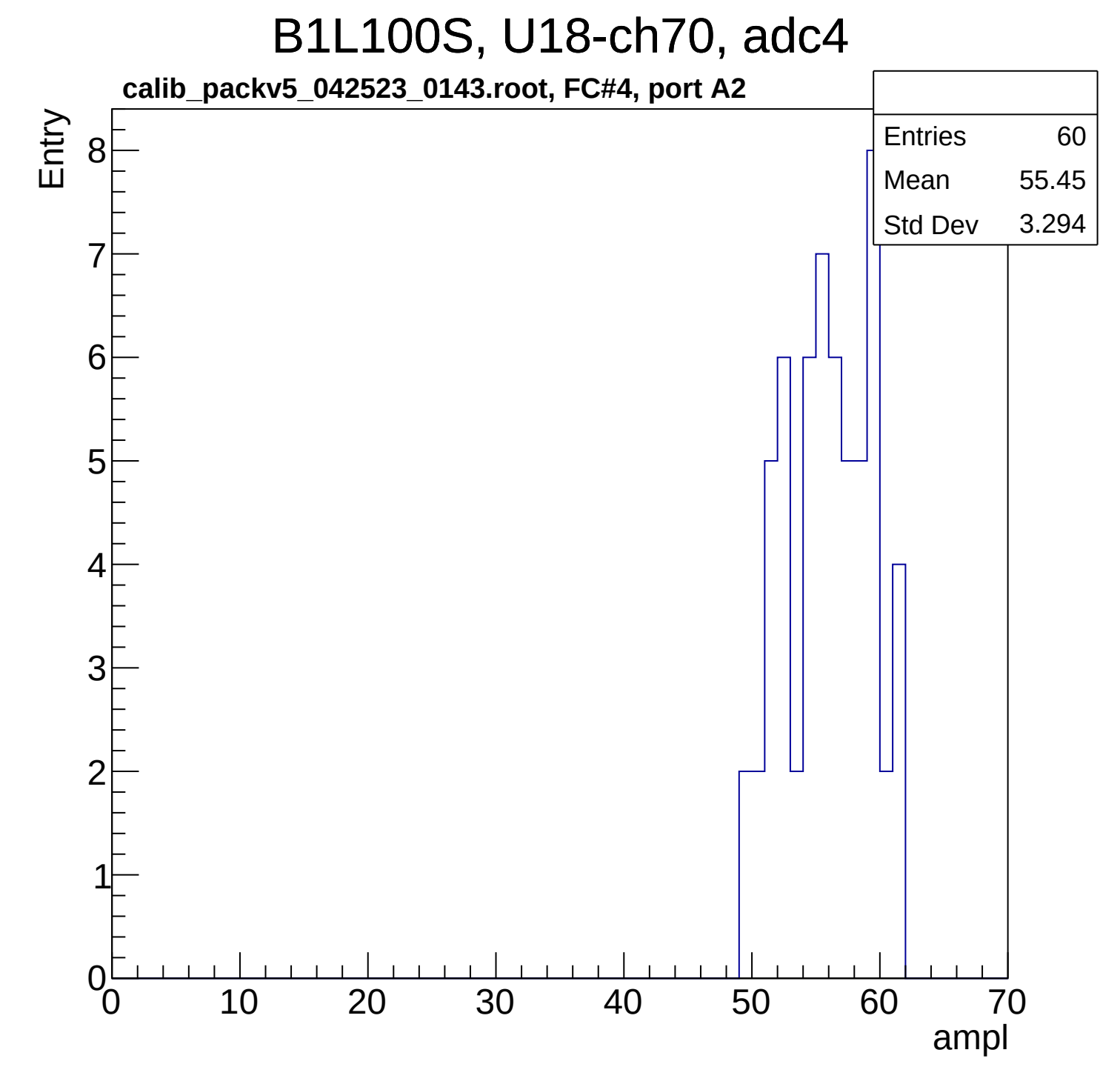

B1L100S, U18-ch69, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

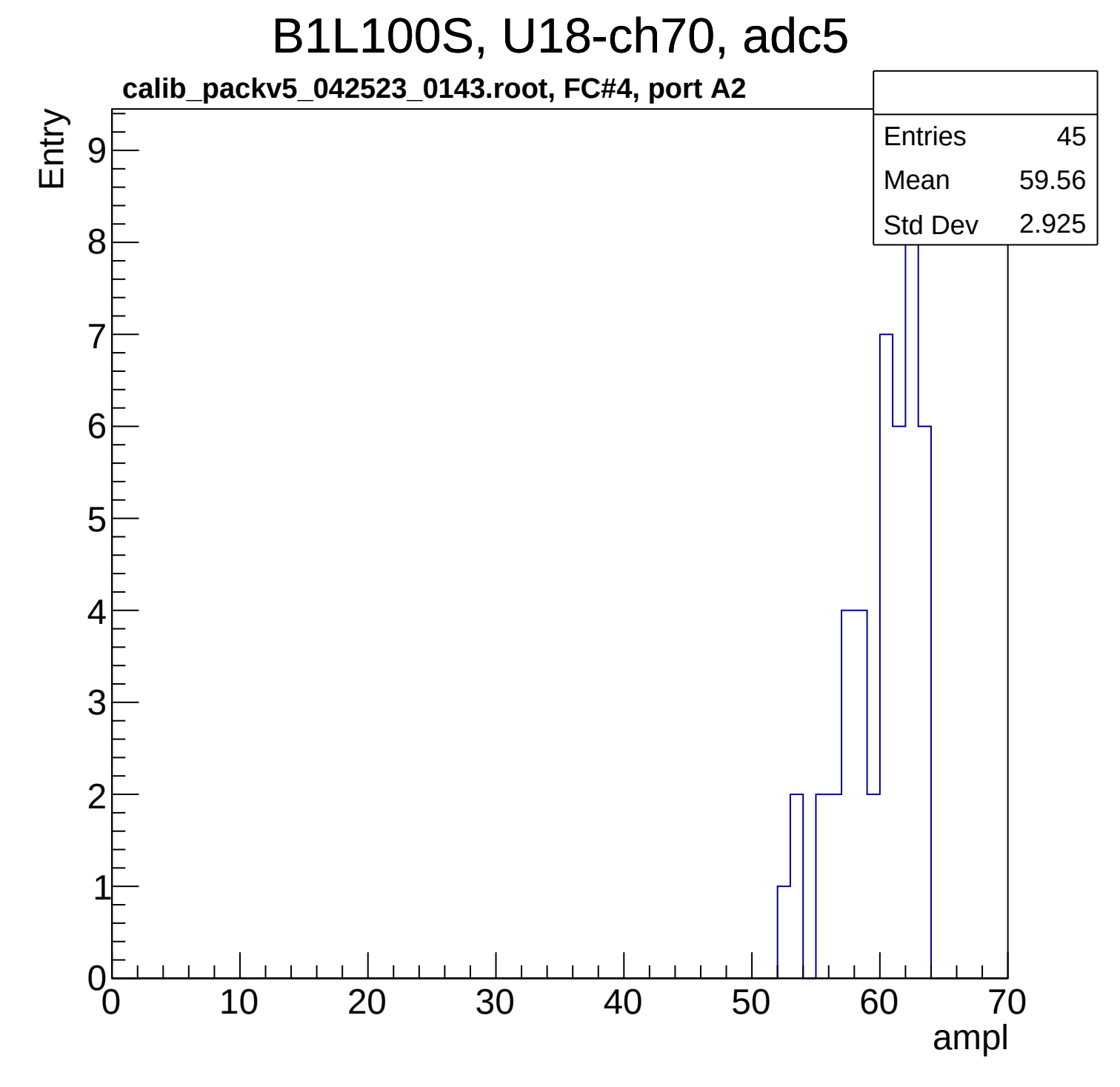

B1L100S, U18-ch70, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 28.91
Std Dev 3.32
Gaus mean : 29.3549
Gaus Width: 3.7494
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

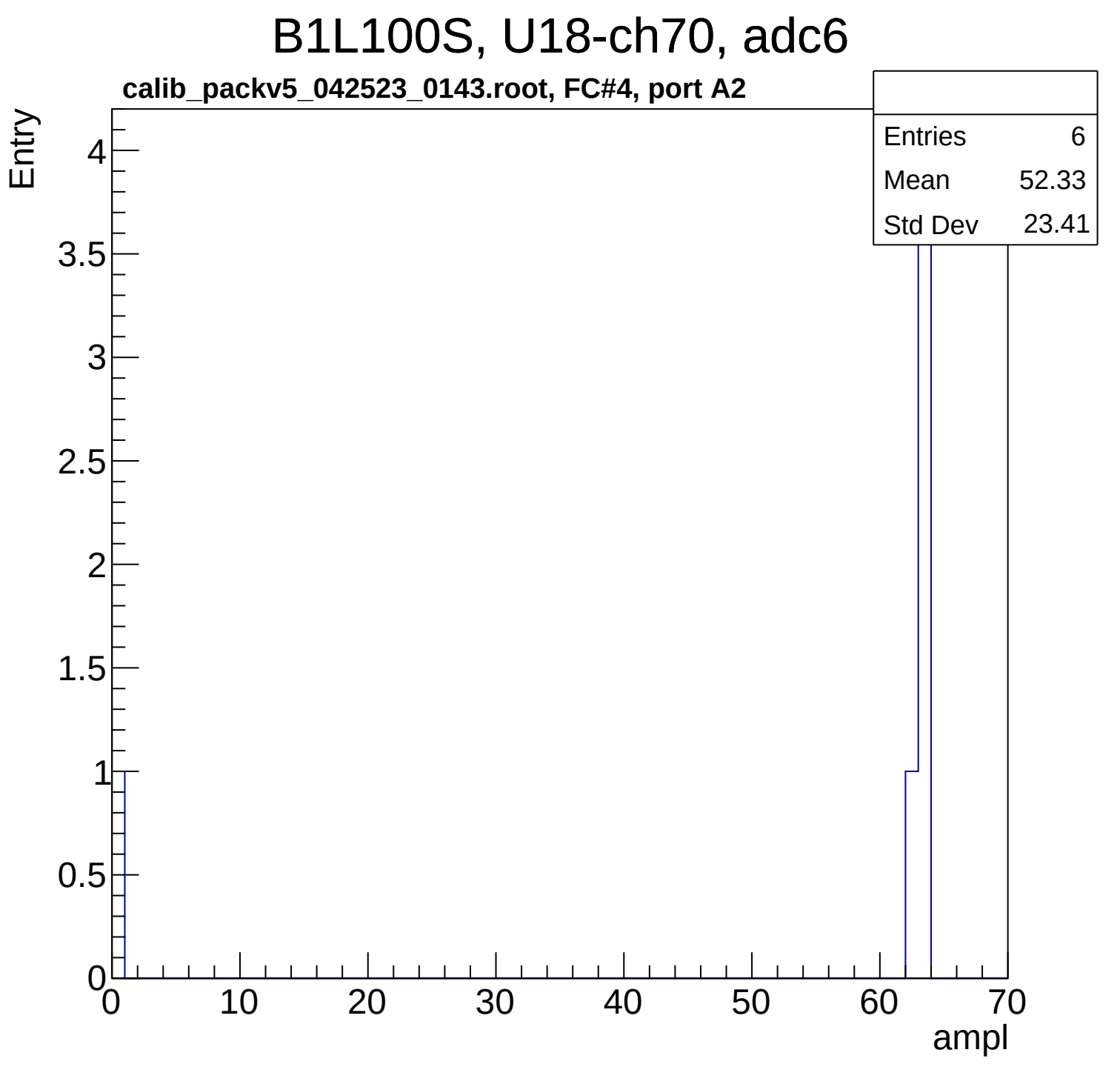

B1L100S, U18-ch70, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 36.18
Std Dev 3.321
Gaus mean : 36.5132
Gaus Width: 3.6684
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

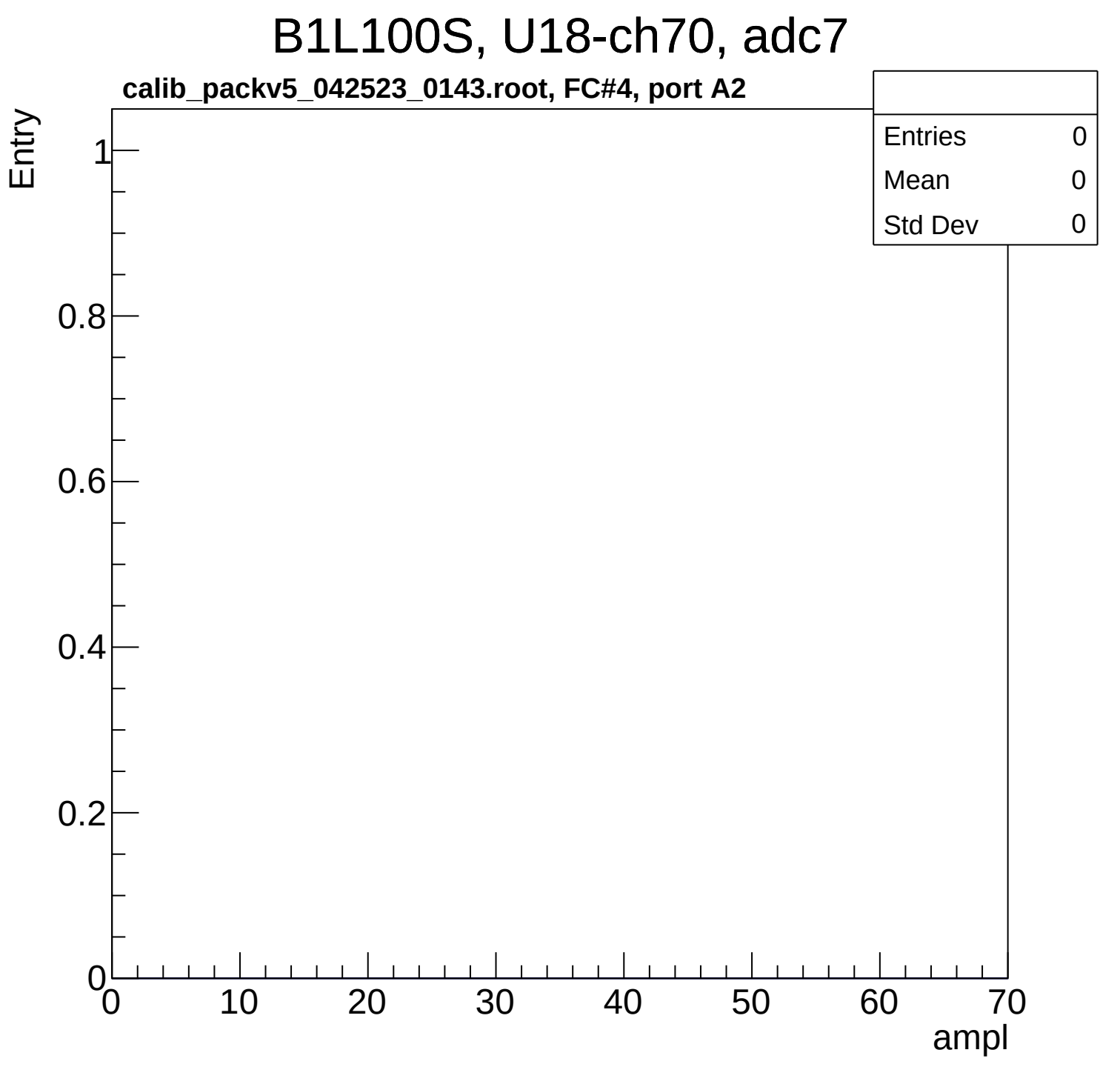

B1L100S, U18-ch70, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 41.95
Std Dev 3.686
Gaus mean : 42.4339
Gaus Width: 4.0491
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

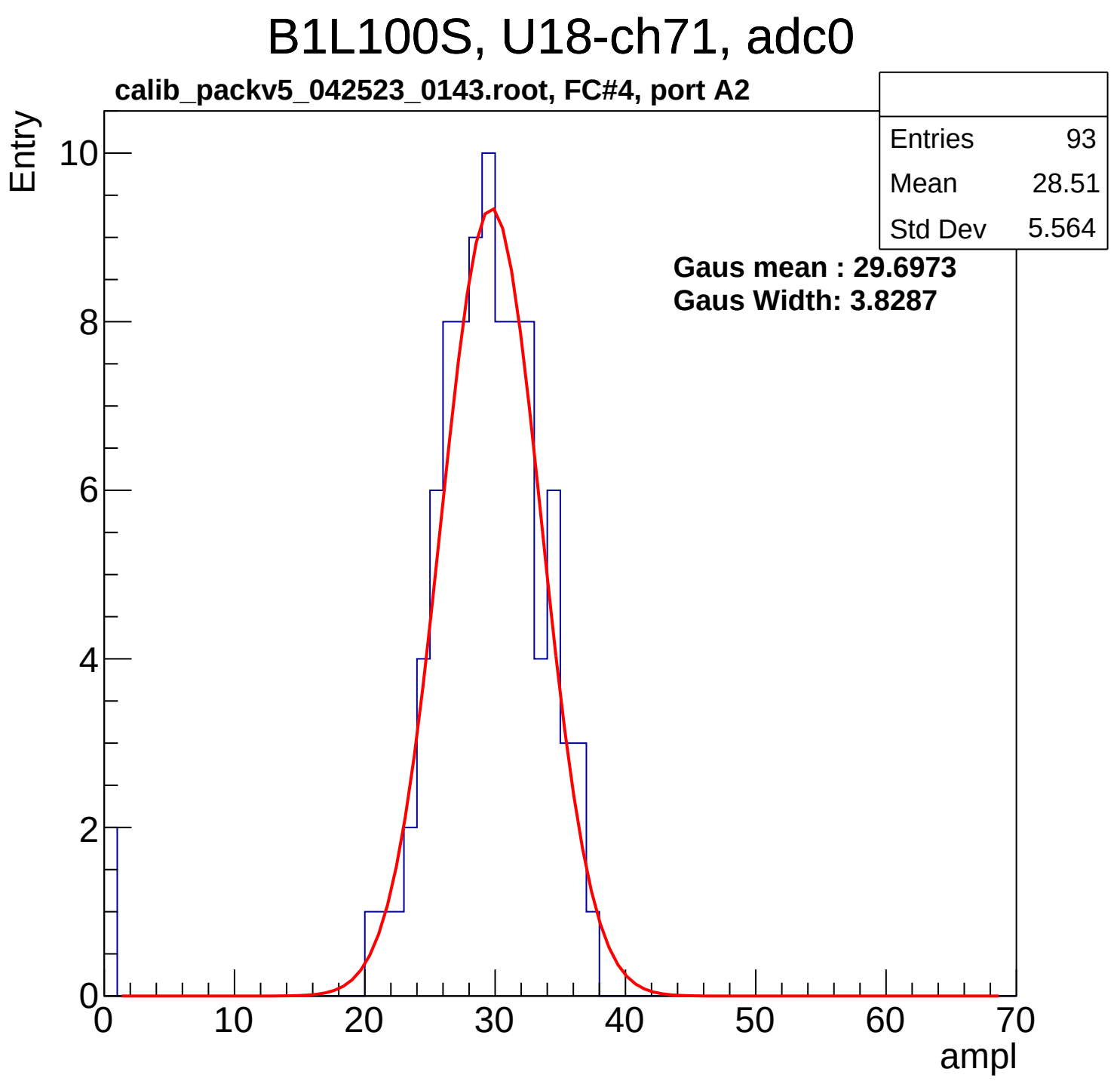

B1L100S, U18-ch70, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 48.81
Std Dev 4.055
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

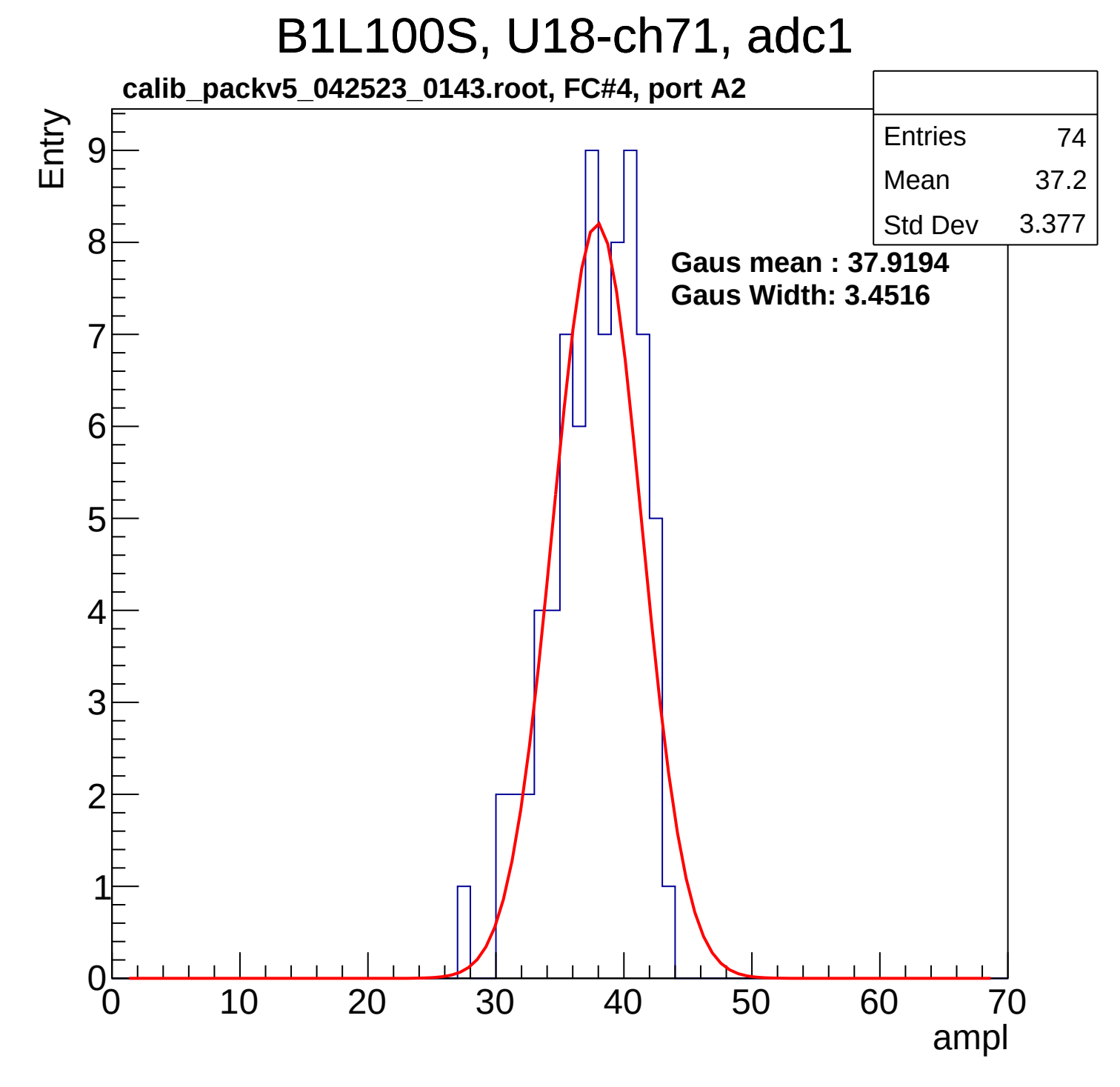

B1L100S, U18-ch70, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 55.45
Std Dev 3.294
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

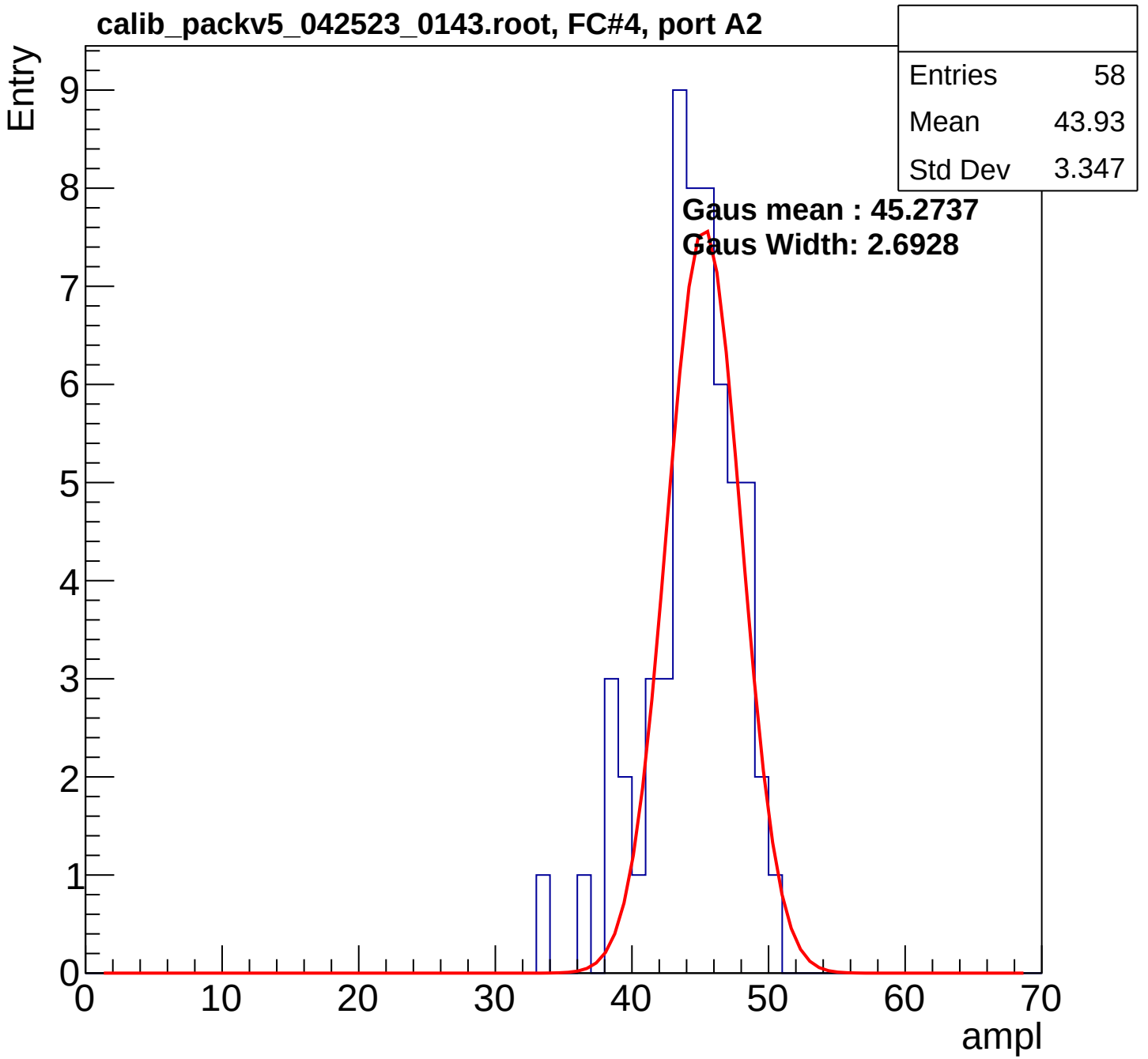

B1L100S, U18-ch70, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 45
Mean 59.56
Std Dev 2.925
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

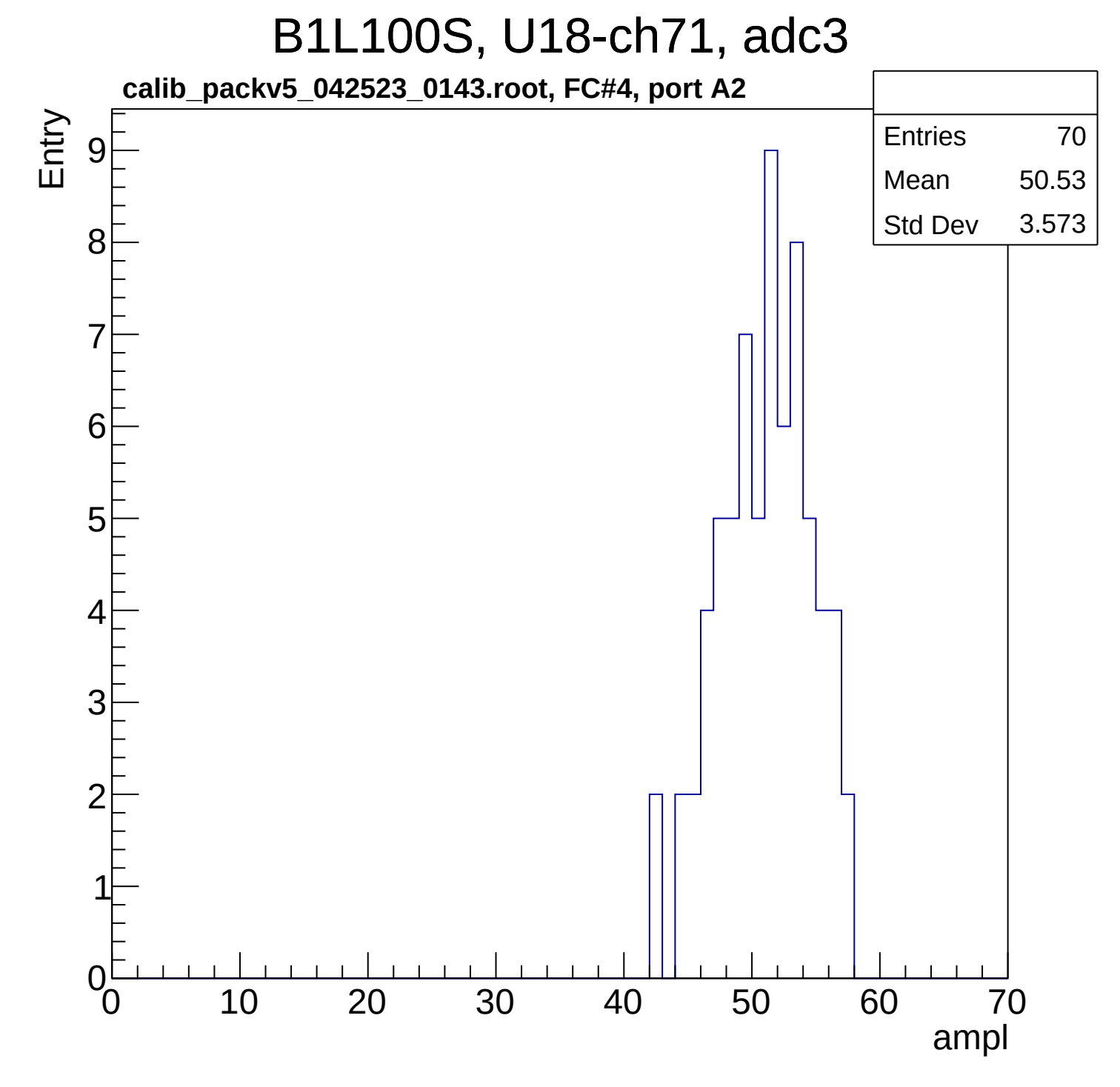

B1L100S, U18-ch70, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 52.33
Std Dev 23.41
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

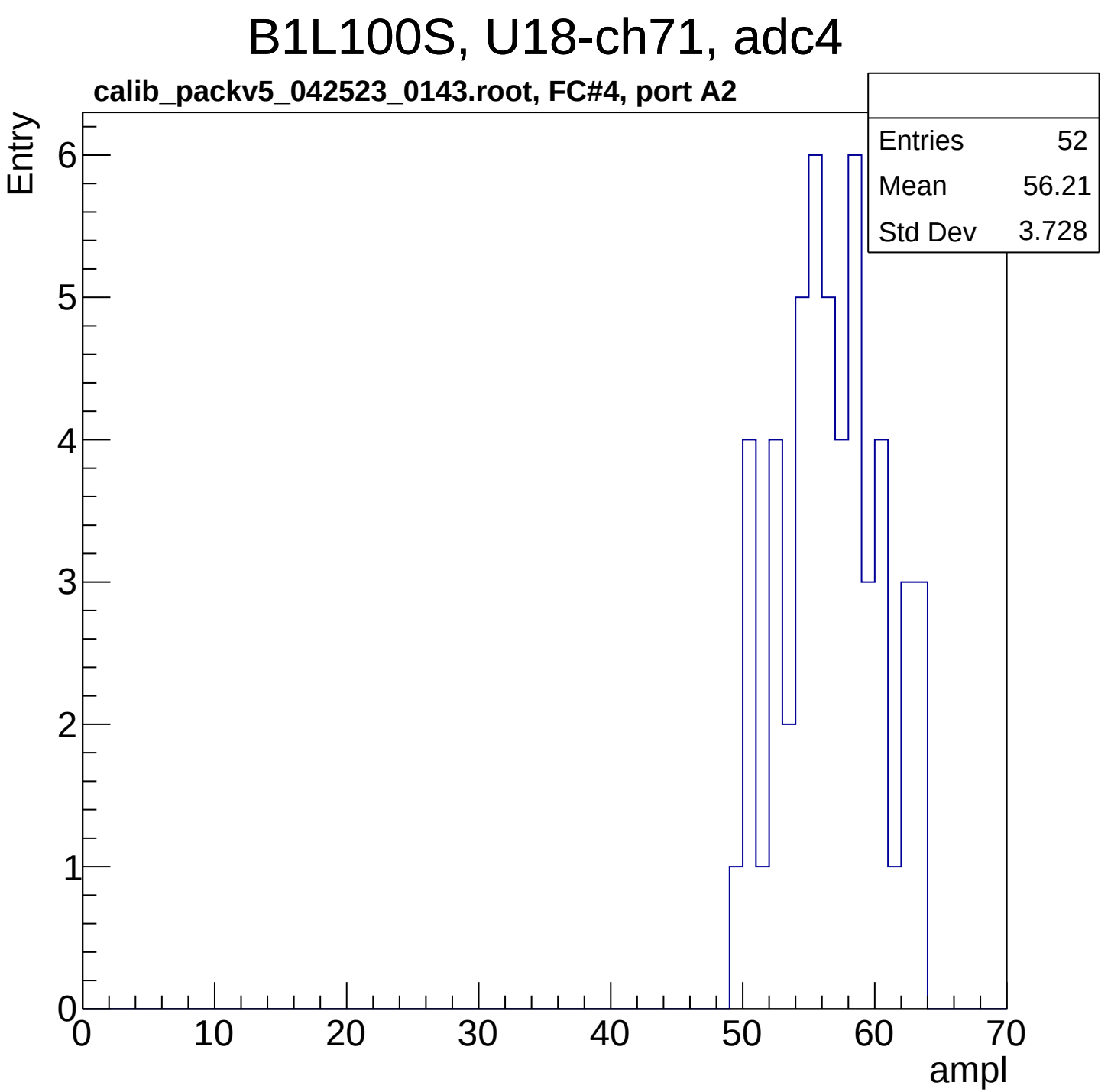

B1L100S, U18-ch70, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

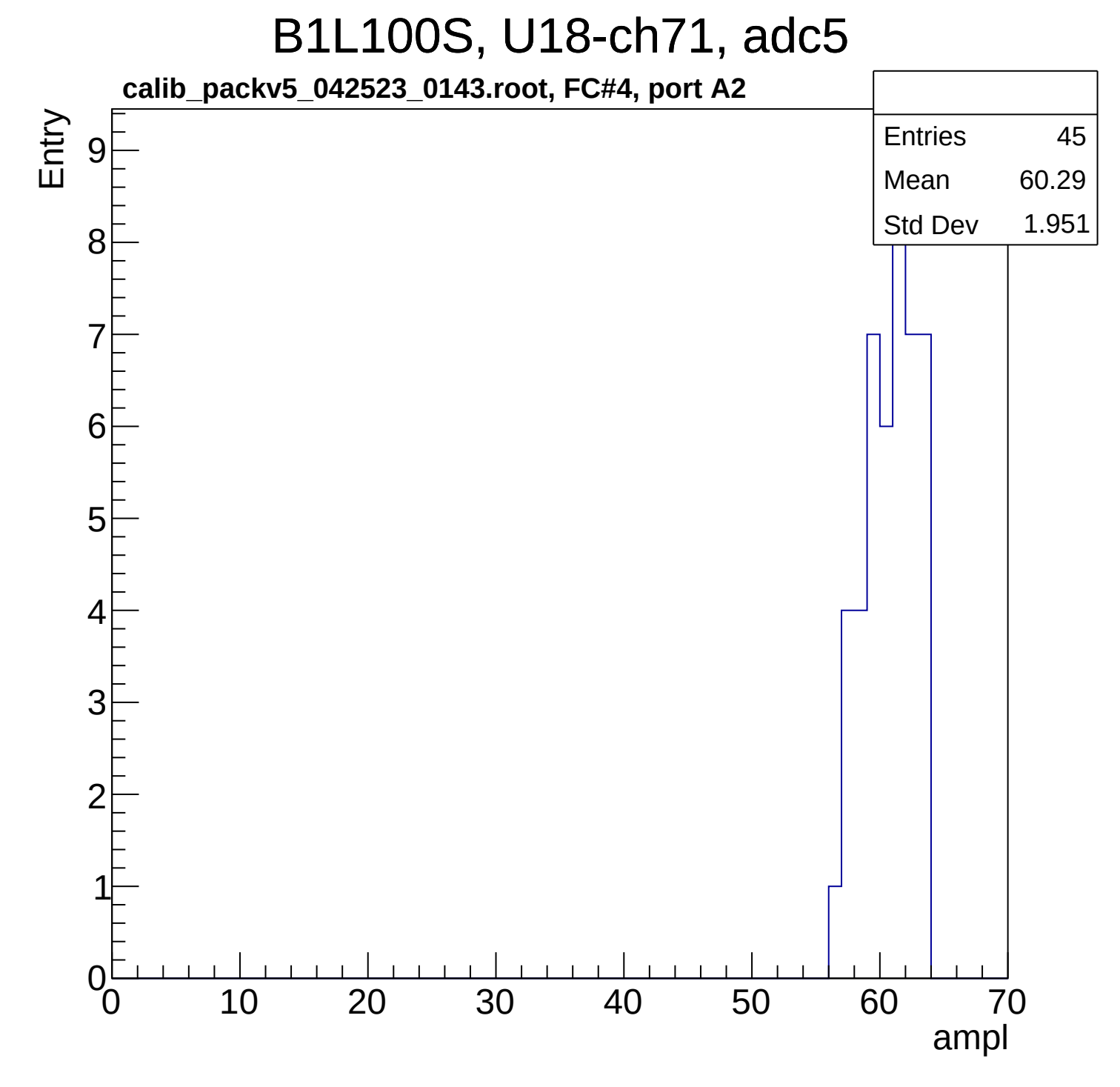

B1L100S, U18-ch71, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 93
Mean 28.51
Std Dev 5.564
Gaus mean : 29.6973
Gaus Width: 3.8287
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

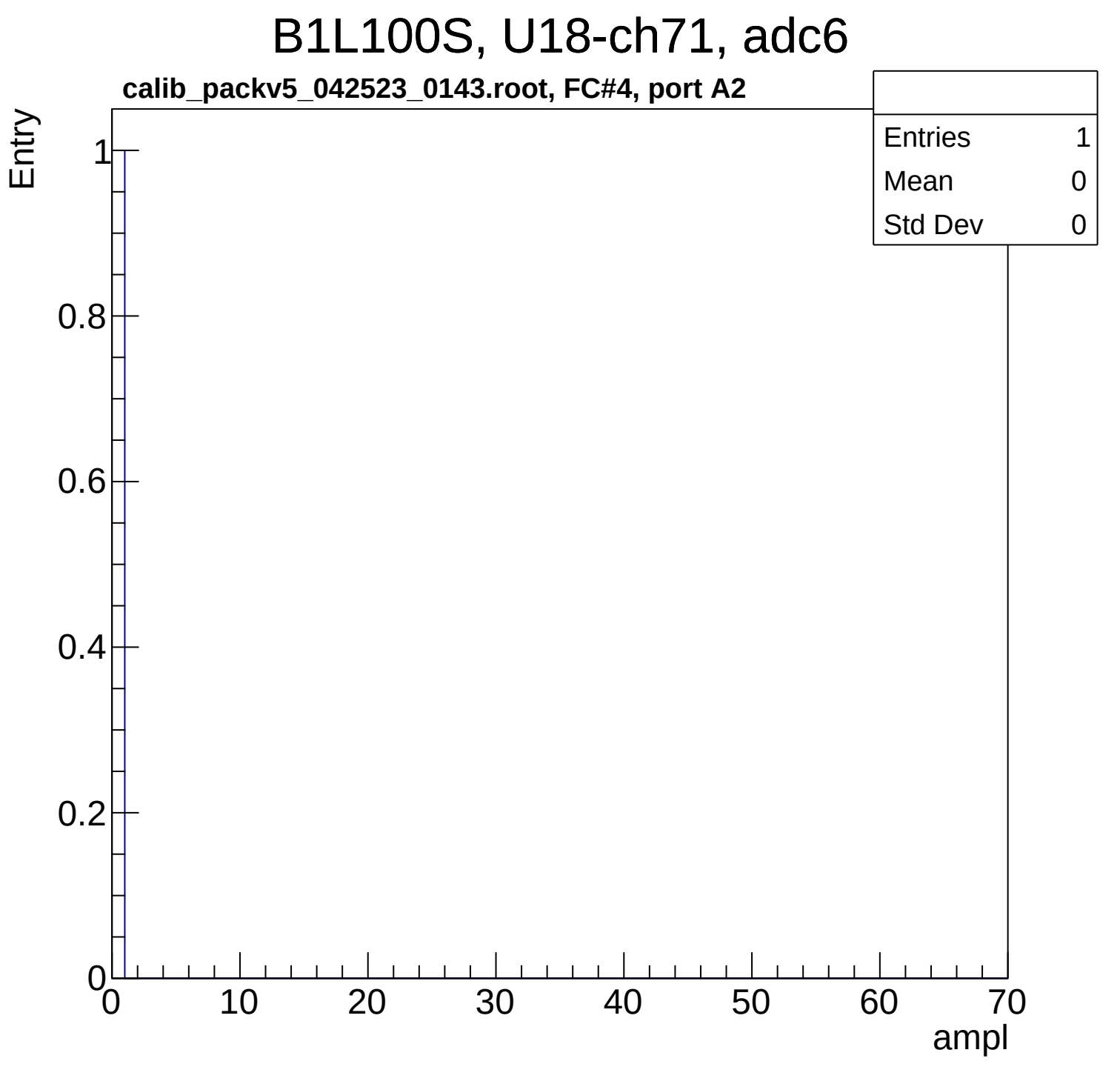

B1L100S, U18-ch71, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 37.2
Std Dev 3.377
Gaus mean : 37.9194
Gaus Width: 3.4516
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

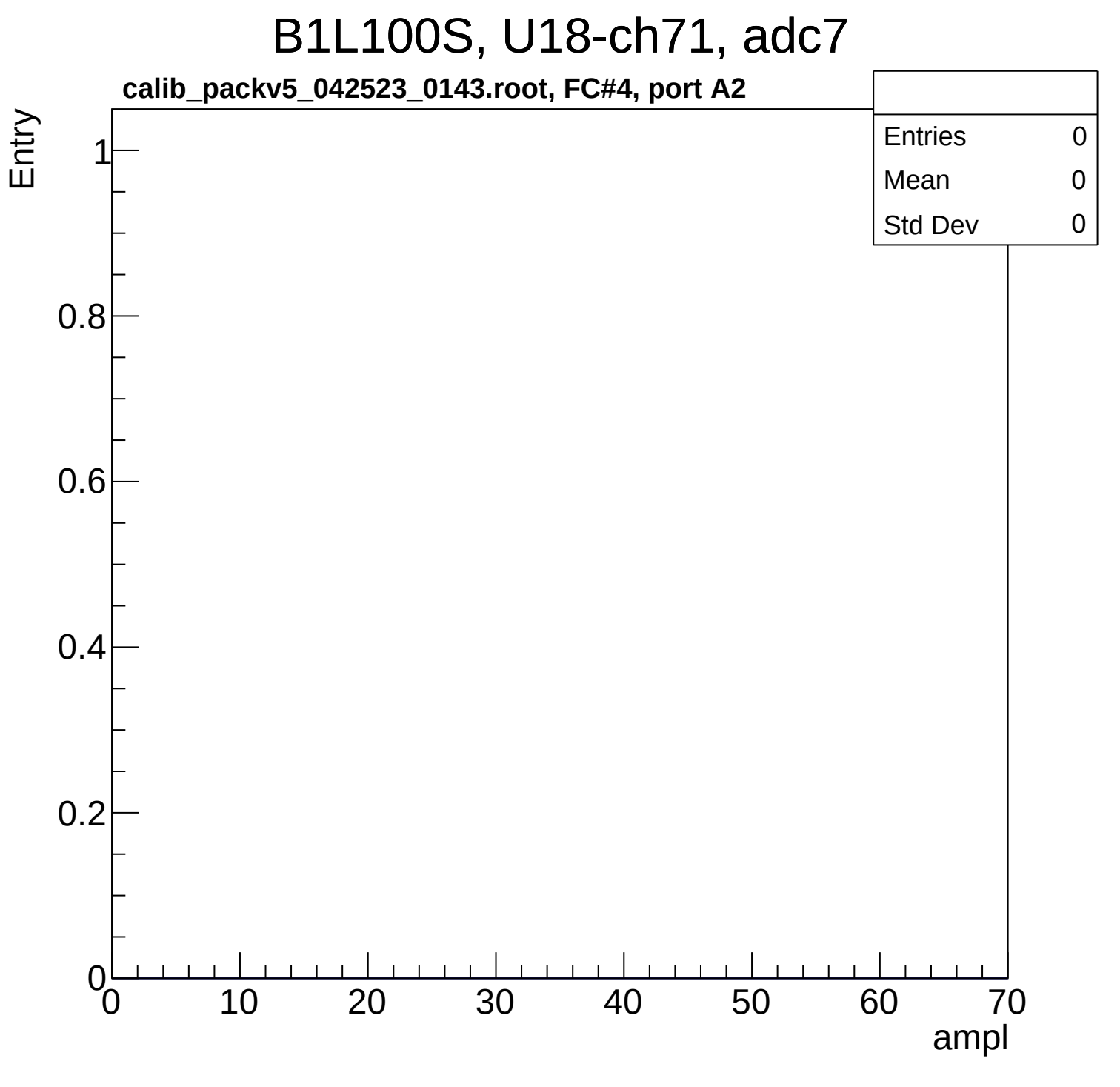

B1L100S, U18-ch71, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 43.93
Std Dev 3.347
Gaus mean : 45.2737
Gaus Width: 2.6928
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

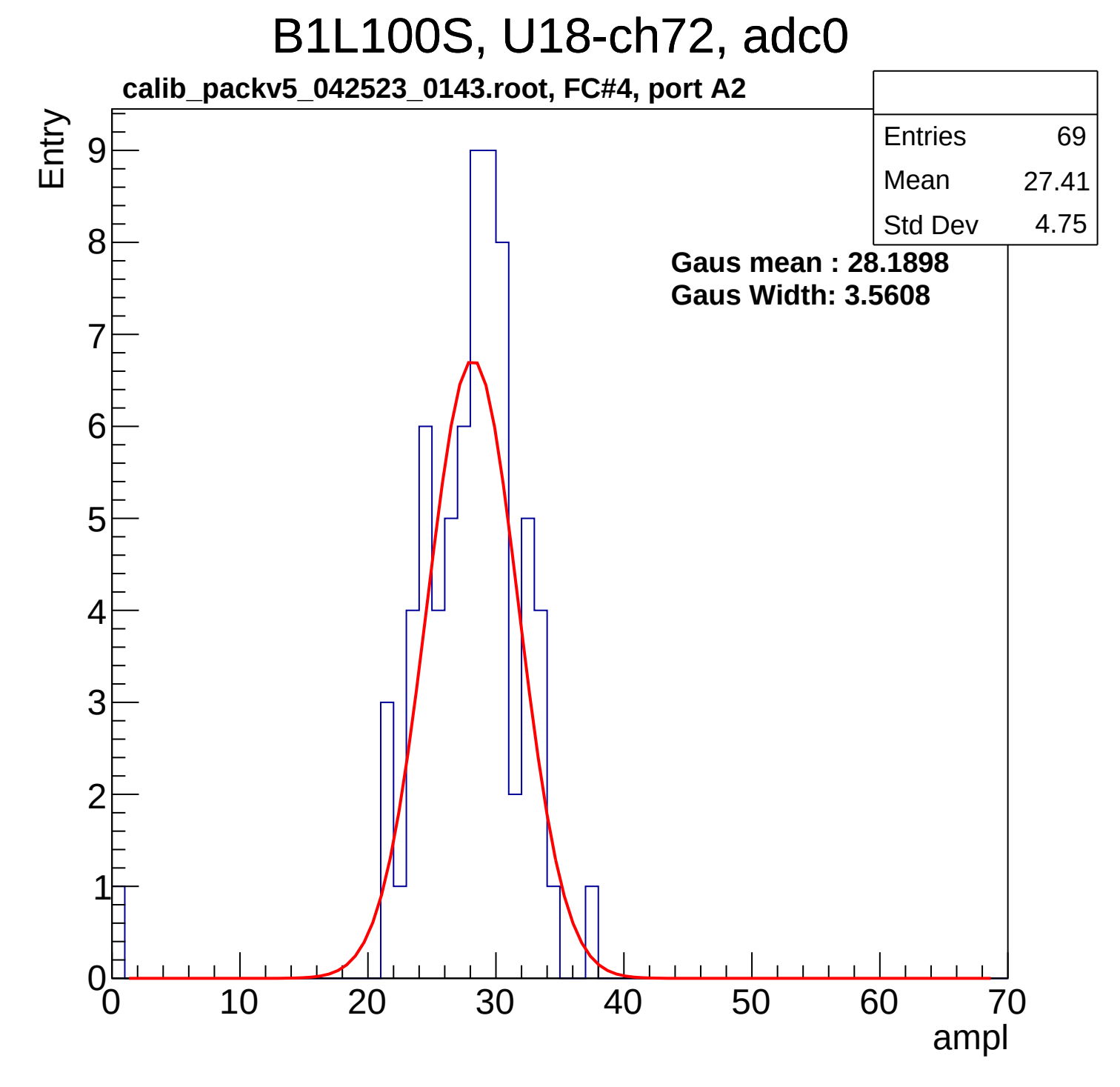

B1L100S, U18-ch71, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 50.53
Std Dev 3.573
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

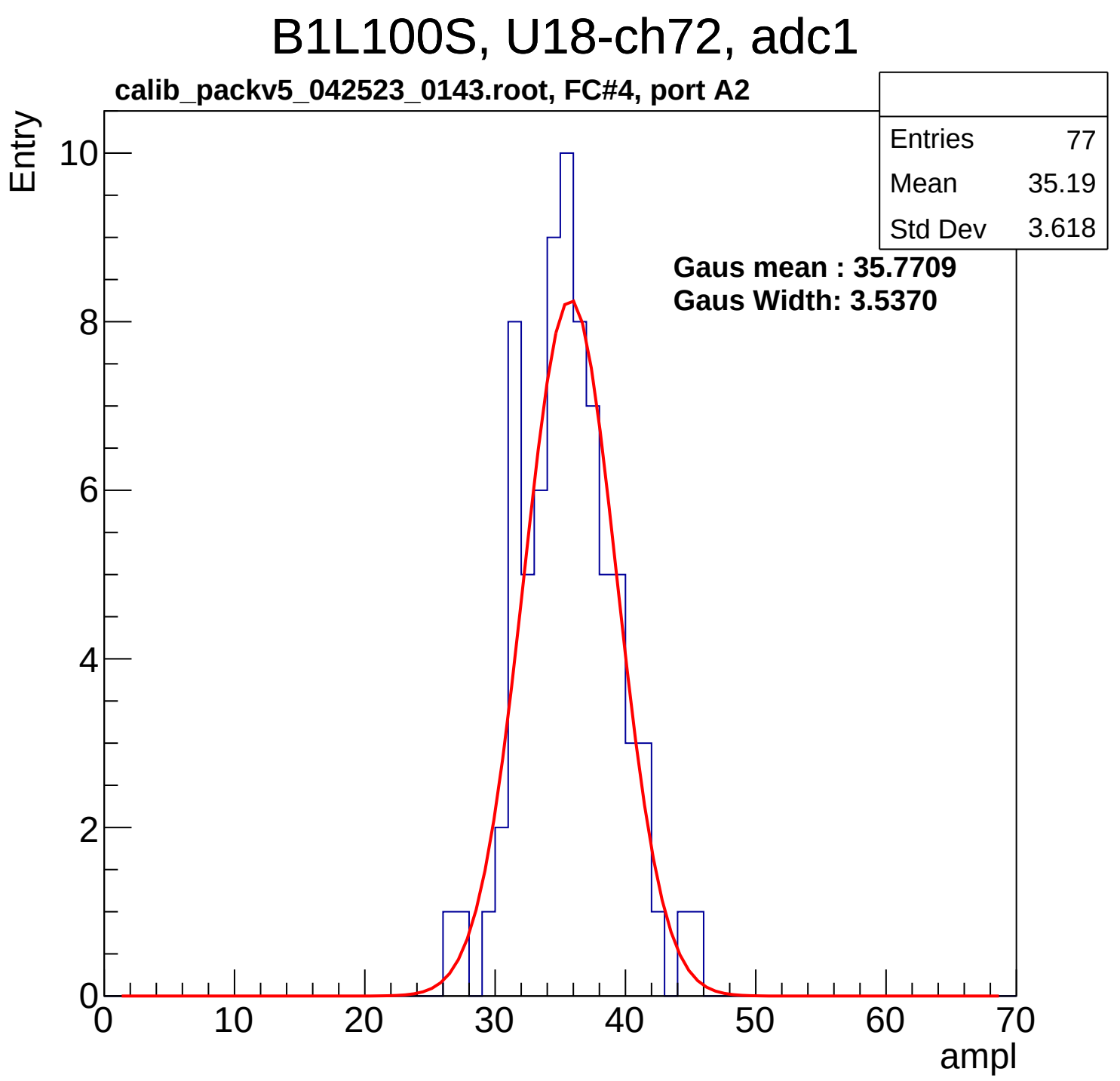

B1L100S, U18-ch71, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 56.21
Std Dev 3.728
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

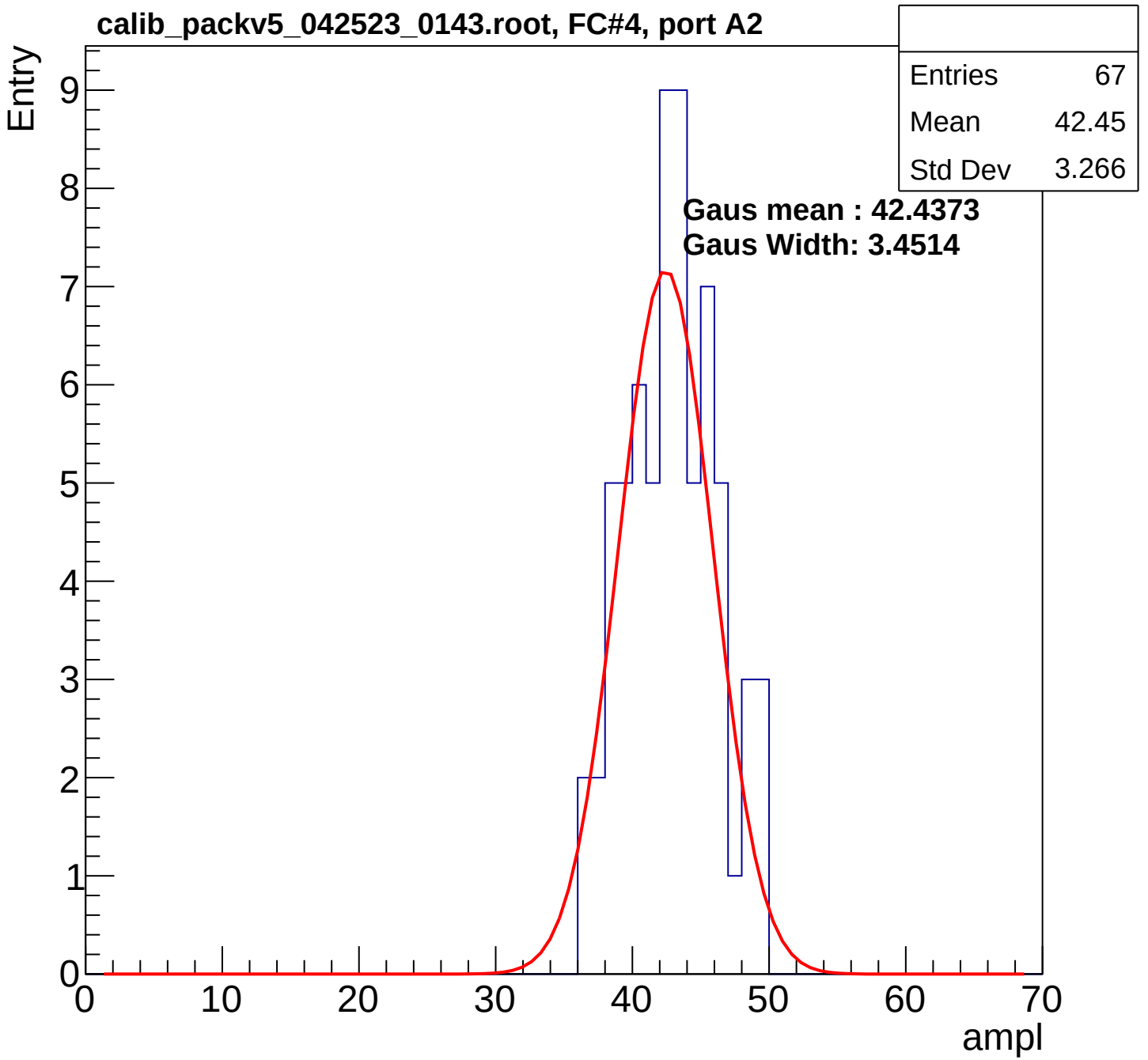

B1L100S, U18-ch71, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 45
Mean 60.29
Std Dev 1.951
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

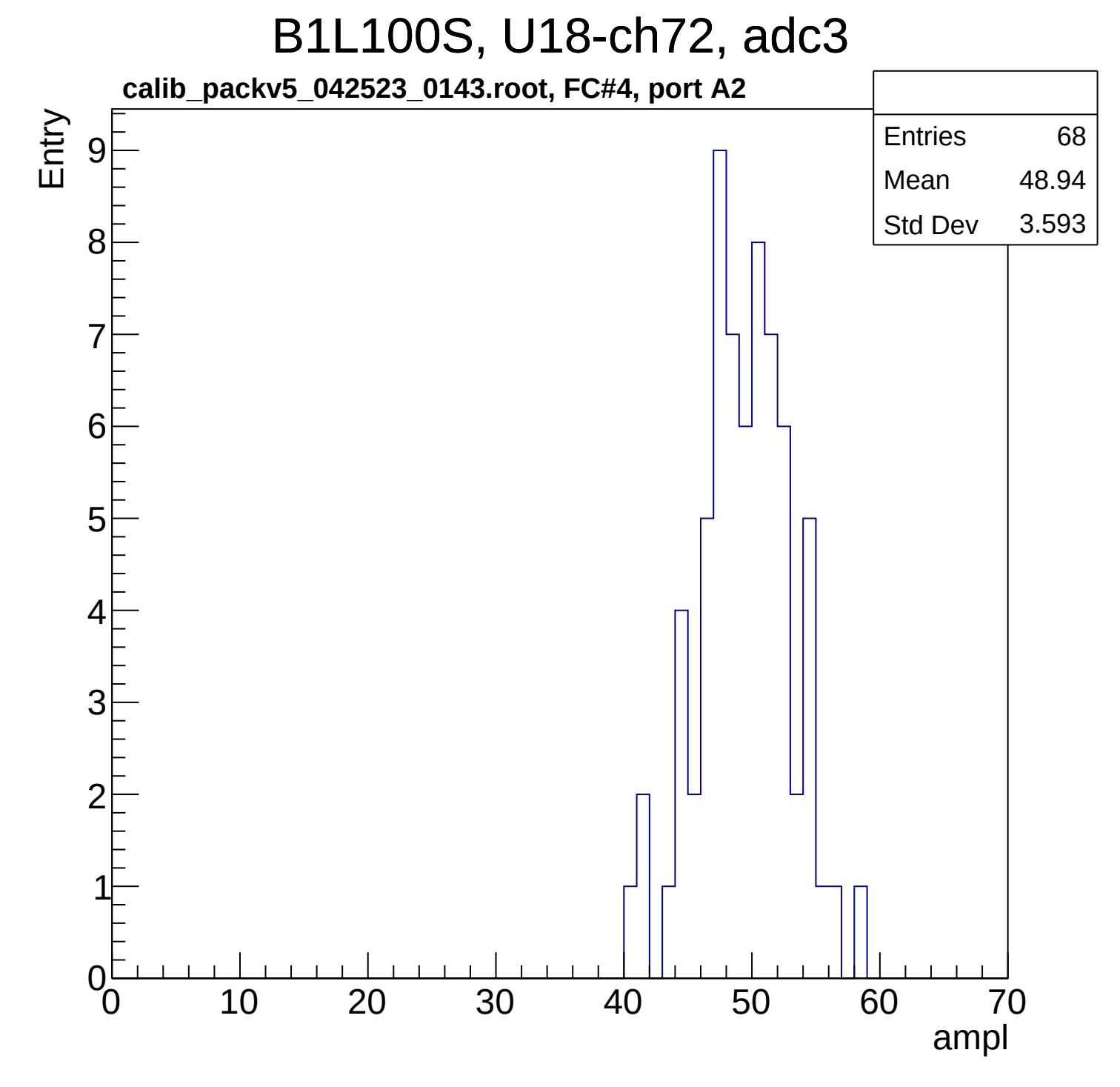

B1L100S, U18-ch71, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

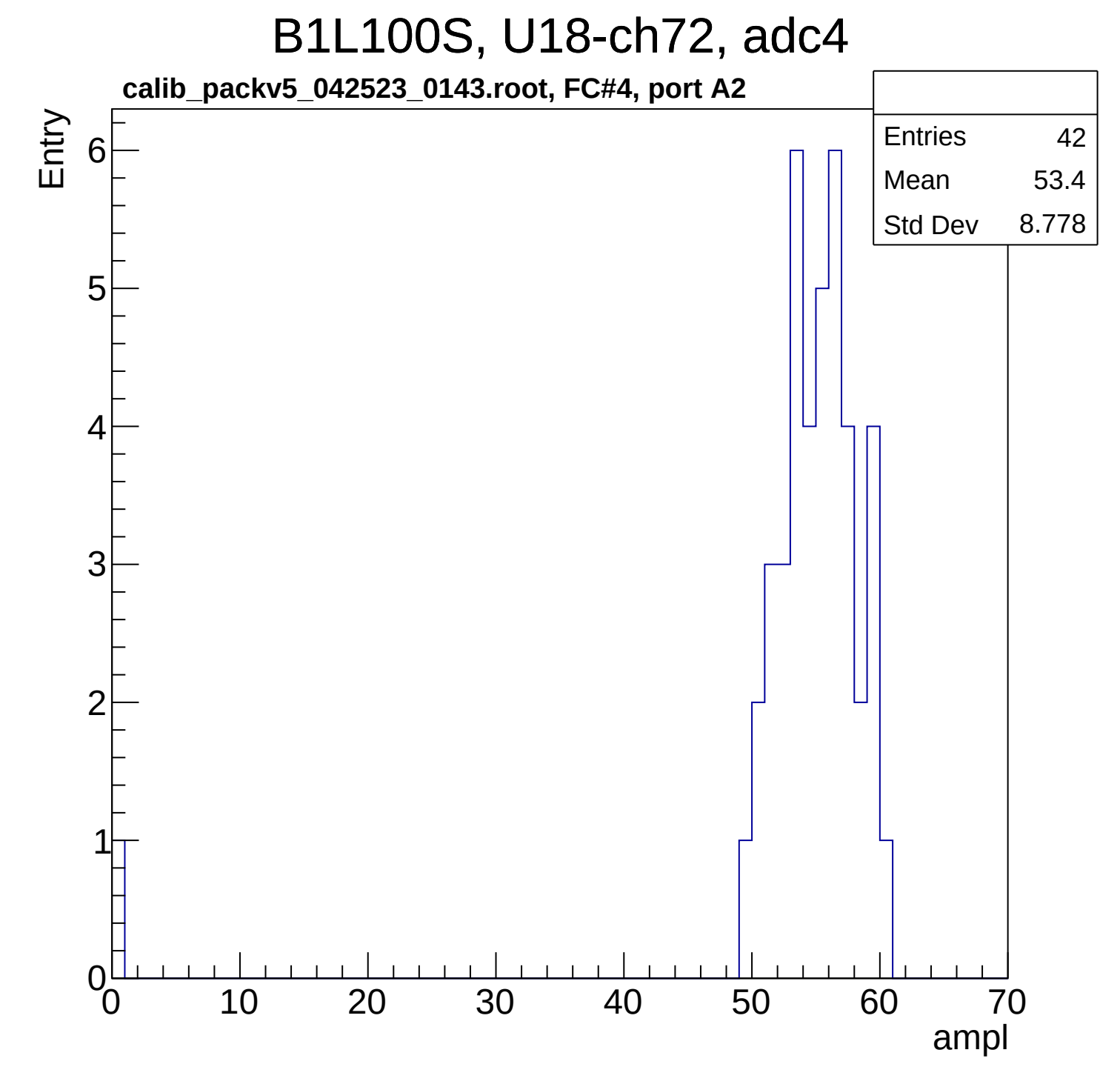

B1L100S, U18-ch71, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

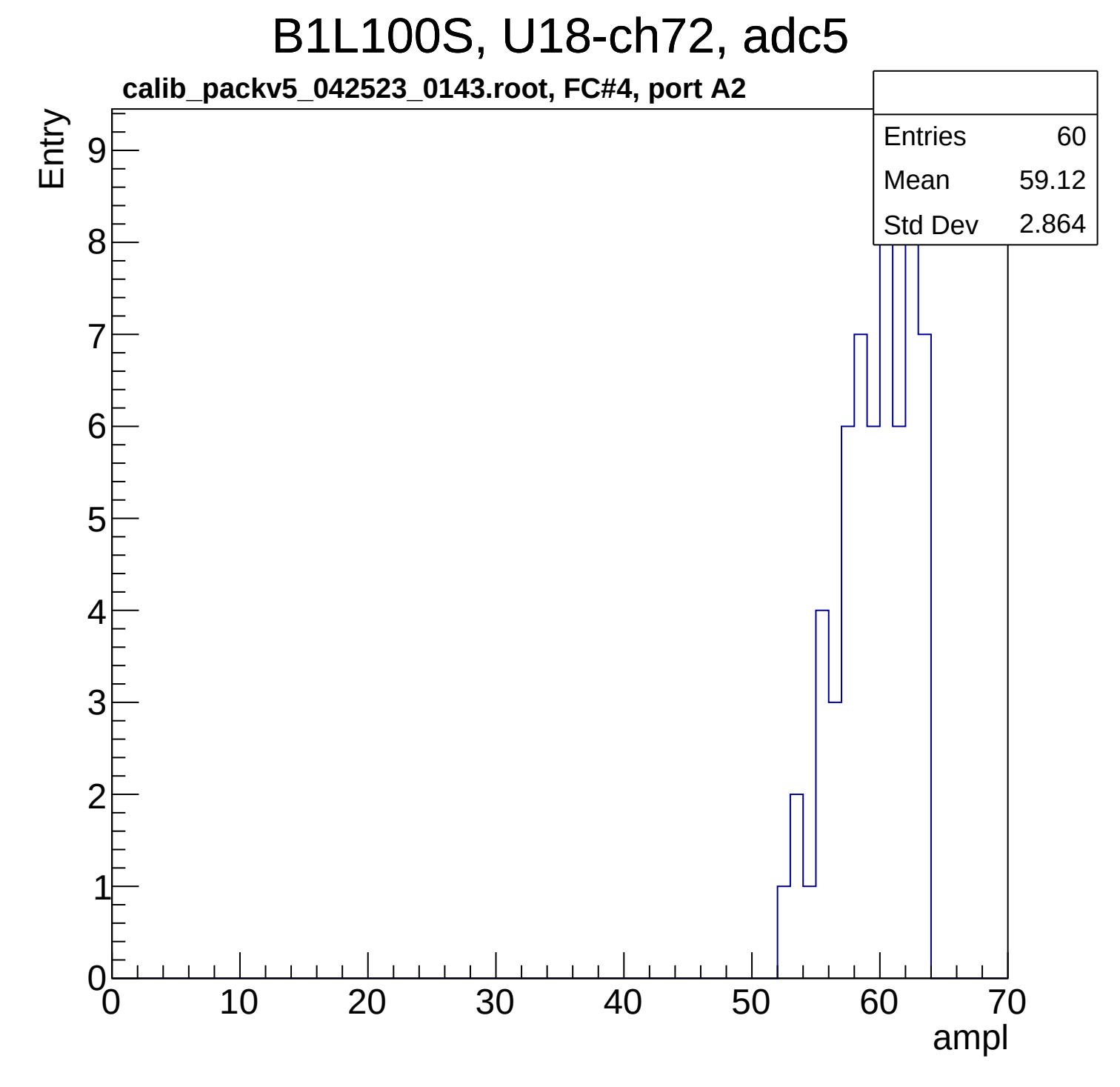

B1L100S, U18-ch72, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 27.41
Std Dev 4.75
Gaus mean : 28.1898
Gaus Width: 3.5608
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

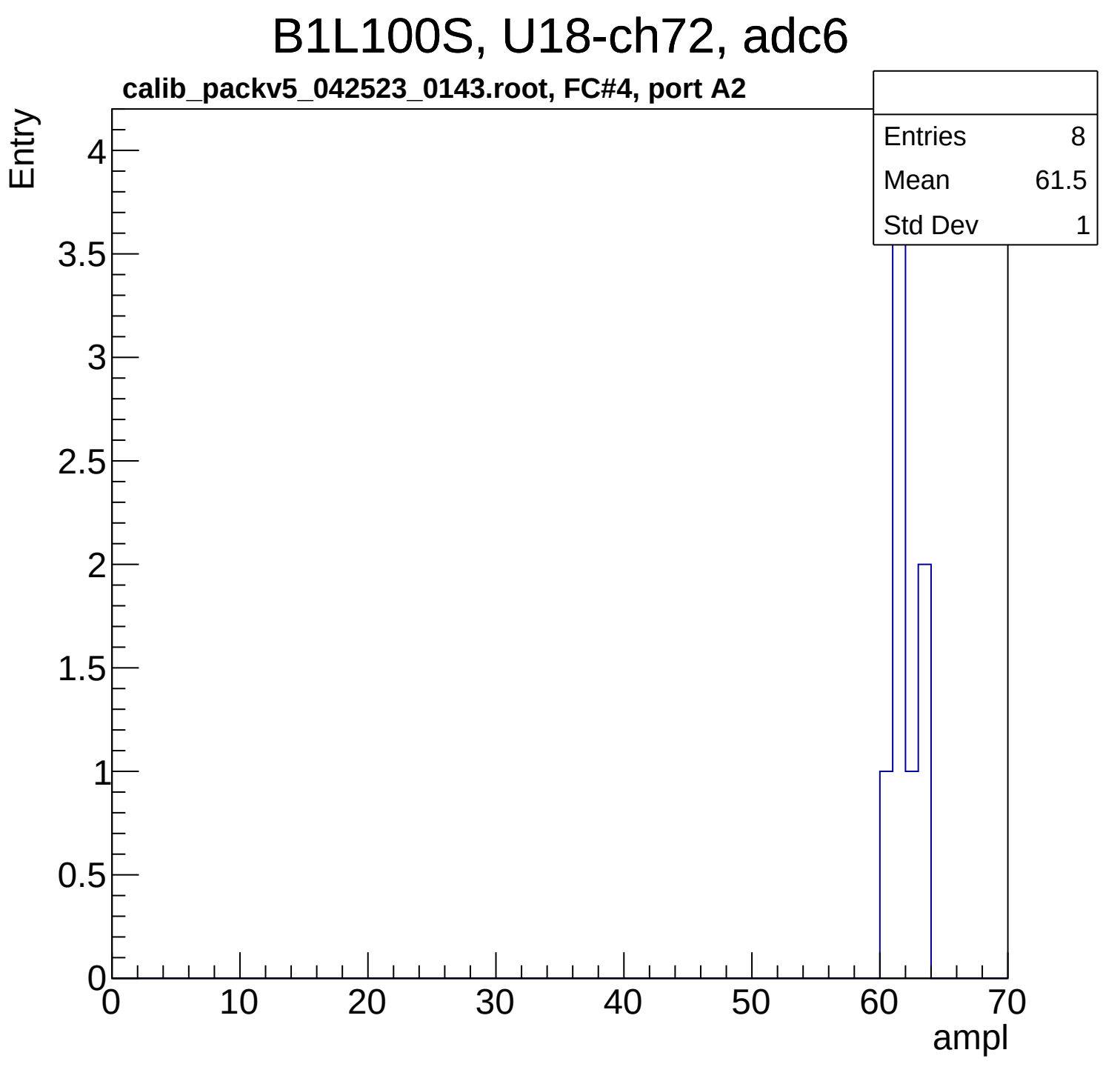

B1L100S, U18-ch72, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 35.19
Std Dev 3.618
Gaus mean : 35.7709
Gaus Width: 3.5370
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

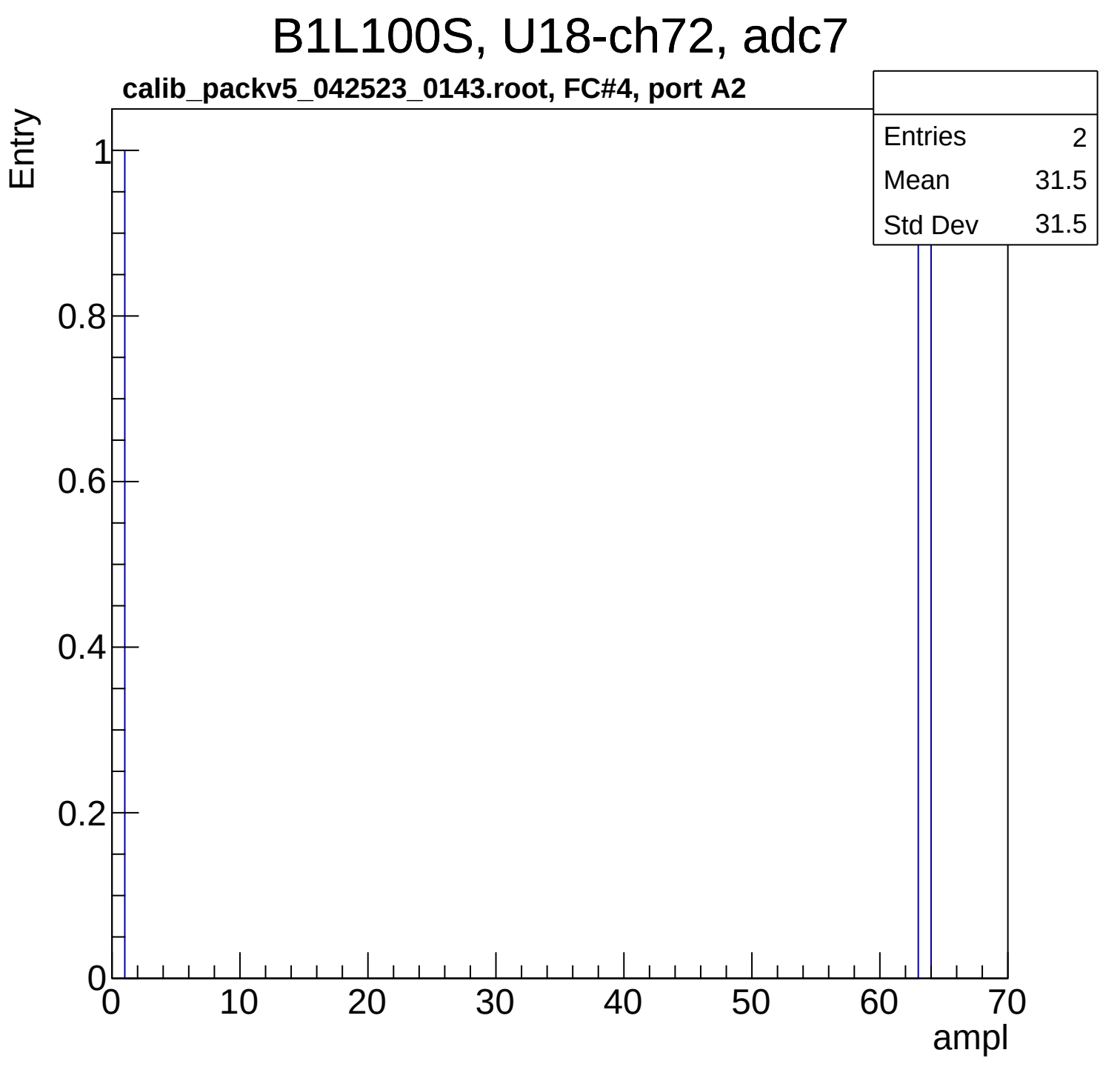

B1L100S, U18-ch72, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 42.45
Std Dev 3.266
Gaus mean : 42.4373
Gaus Width: 3.4514
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

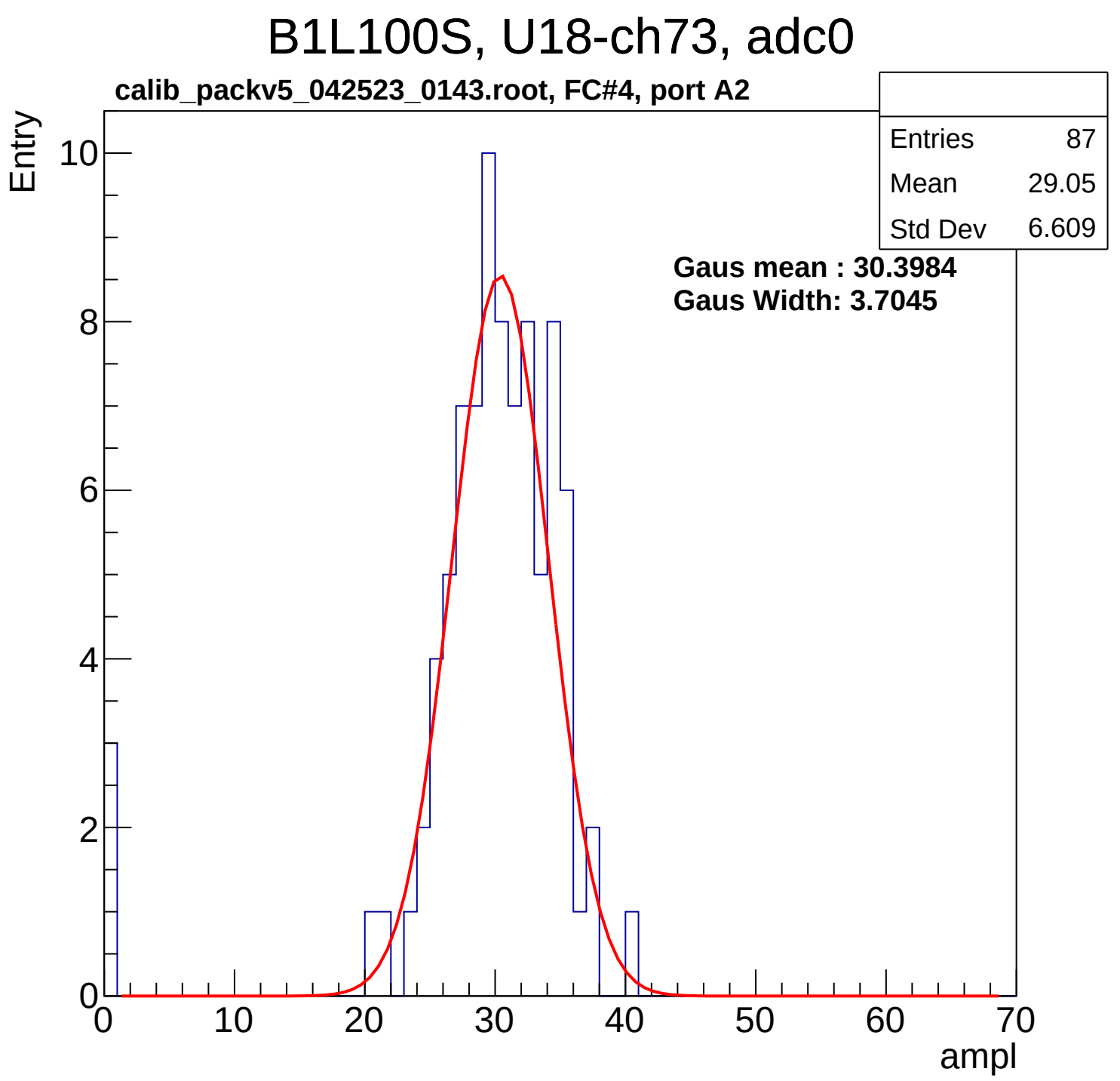

B1L100S, U18-ch72, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 48.94
Std Dev 3.593
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

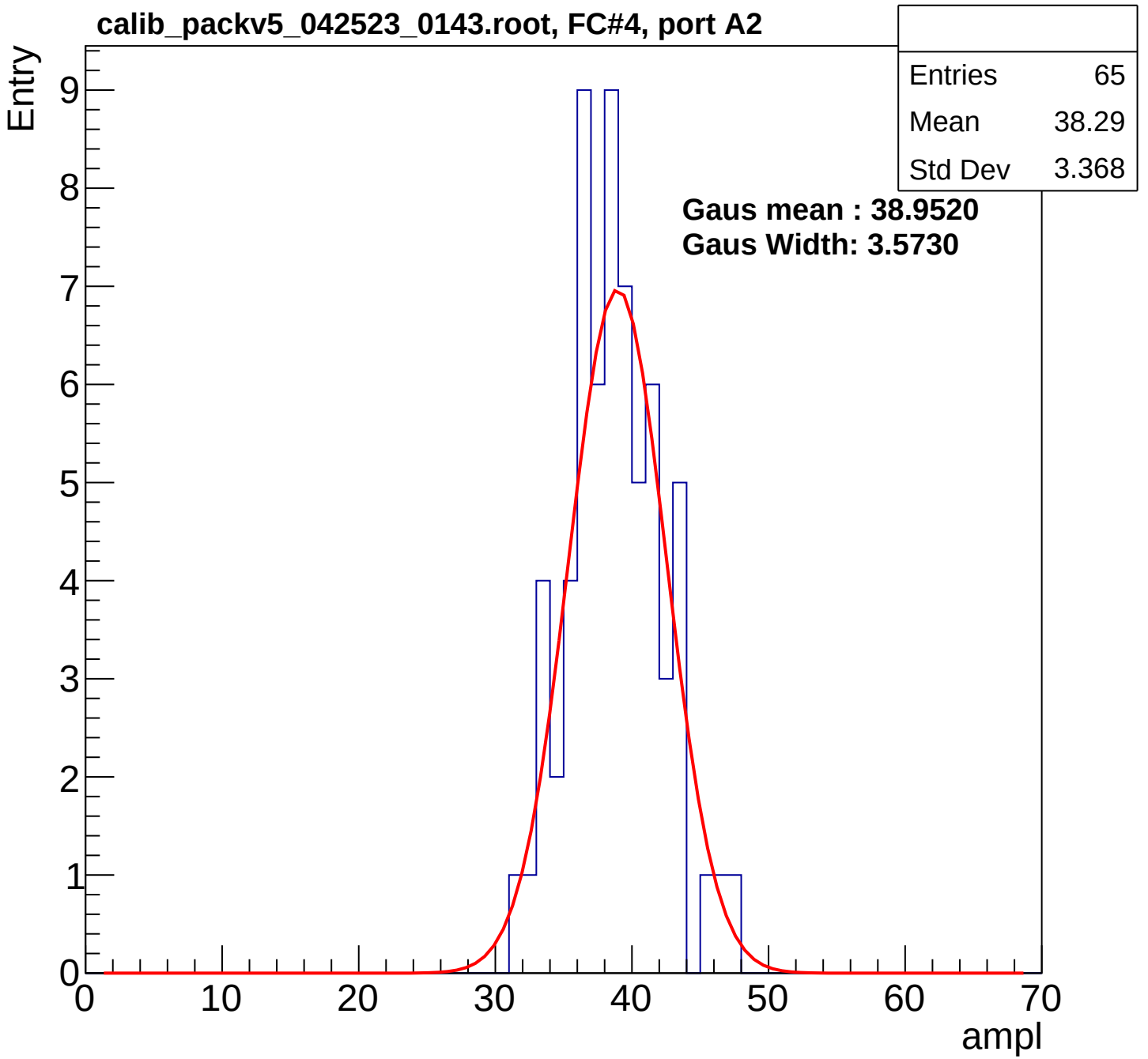

B1L100S, U18-ch72, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 42
Mean 53.4
Std Dev 8.778
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

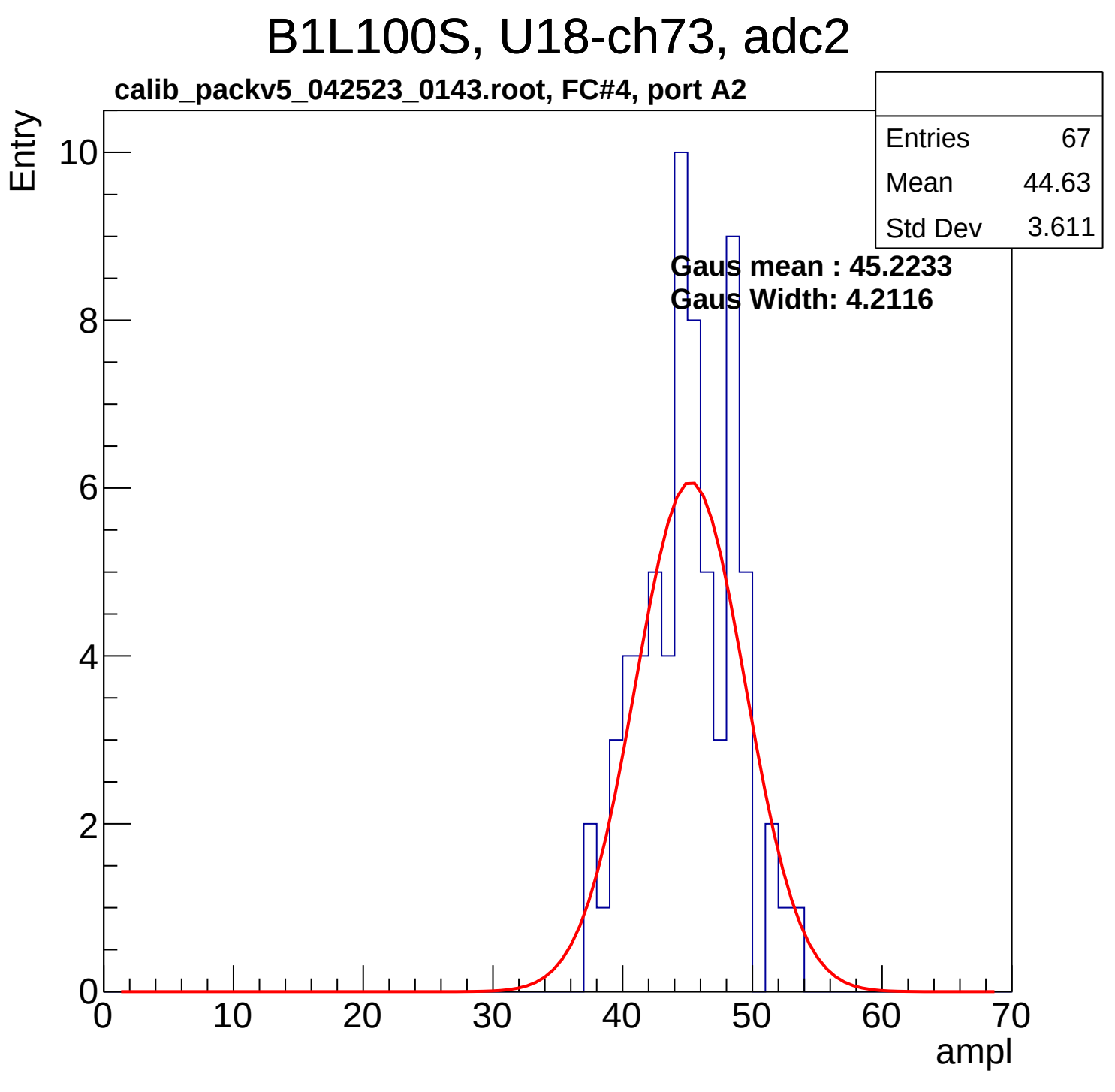

B1L100S, U18-ch72, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 59.12
Std Dev 2.864
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

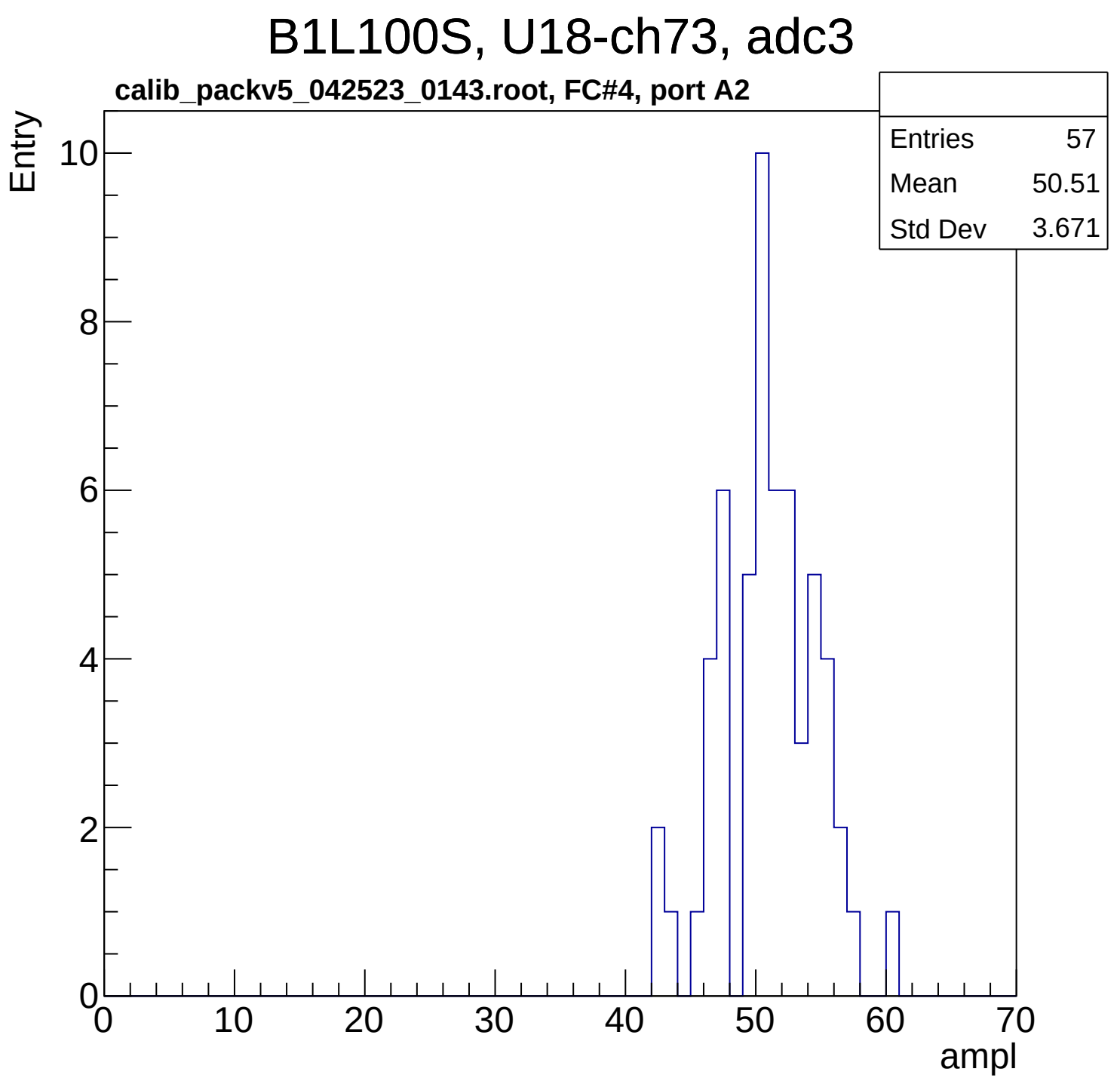

B1L100S, U18-ch72, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 8
Mean 61.5
Std Dev 1
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

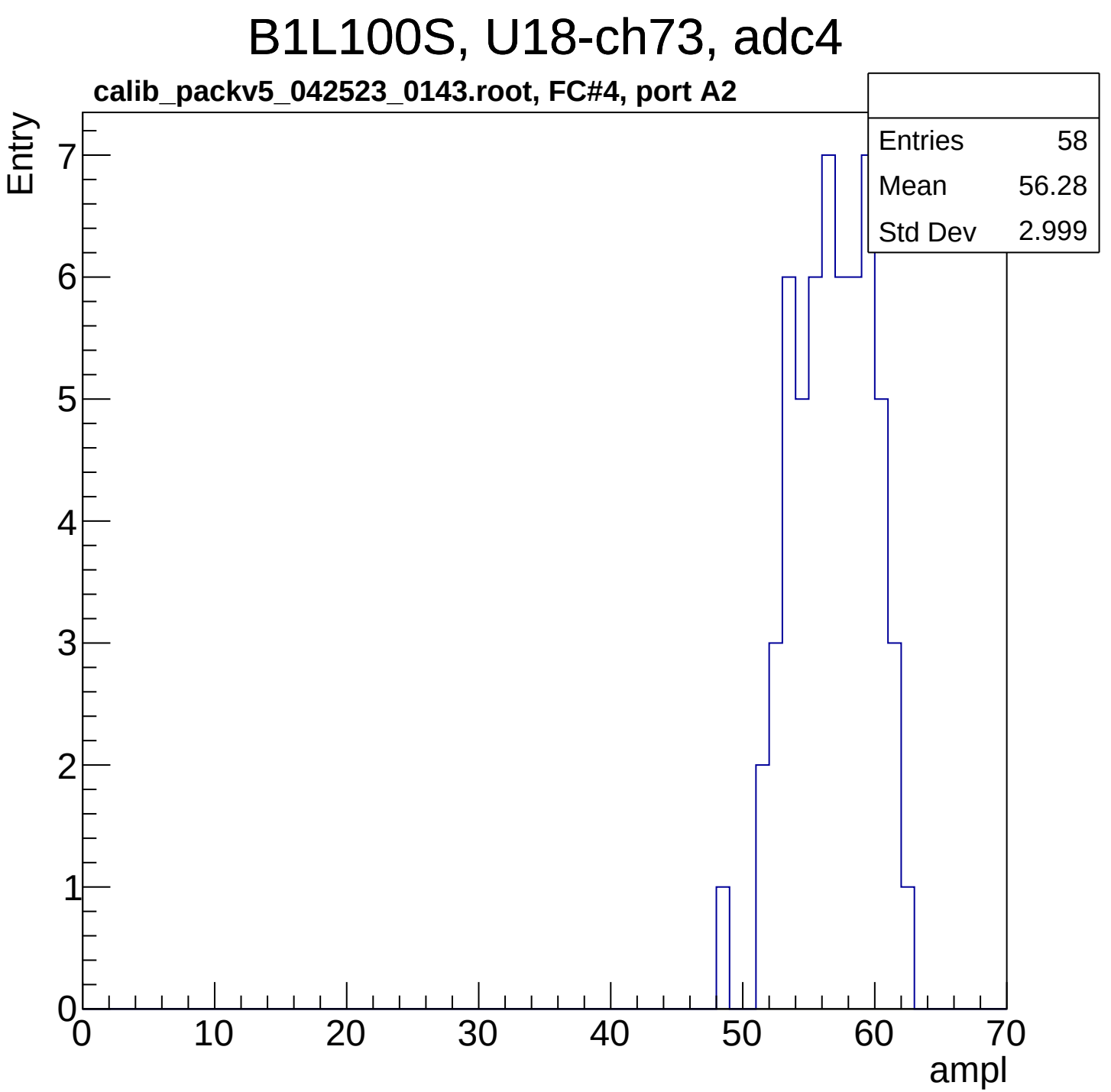

B1L100S, U18-ch72, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

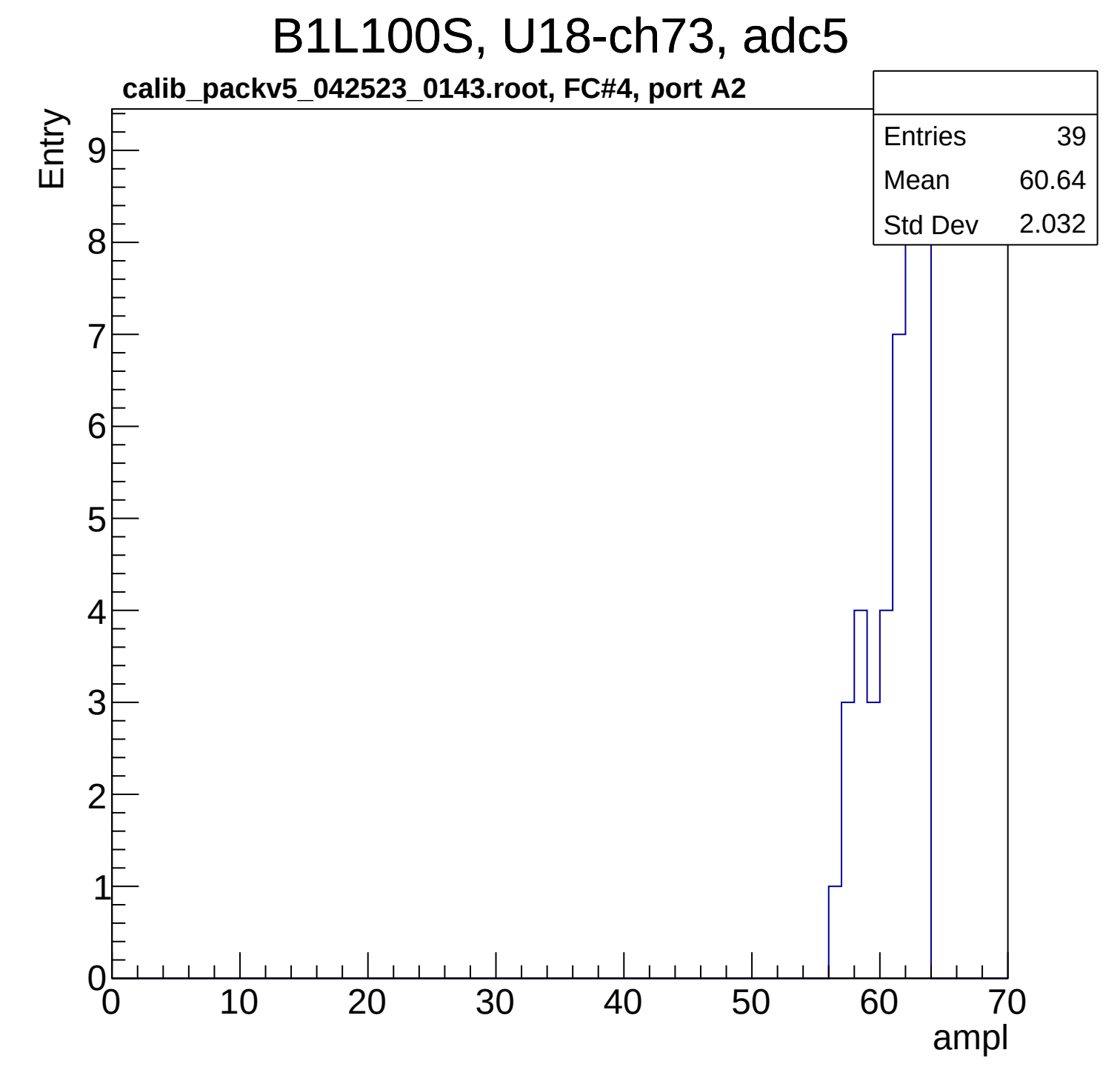

B1L100S, U18-ch73, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 87
Mean 29.05
Std Dev 6.609
Gaus mean : 30.3984
Gaus Width: 3.7045
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

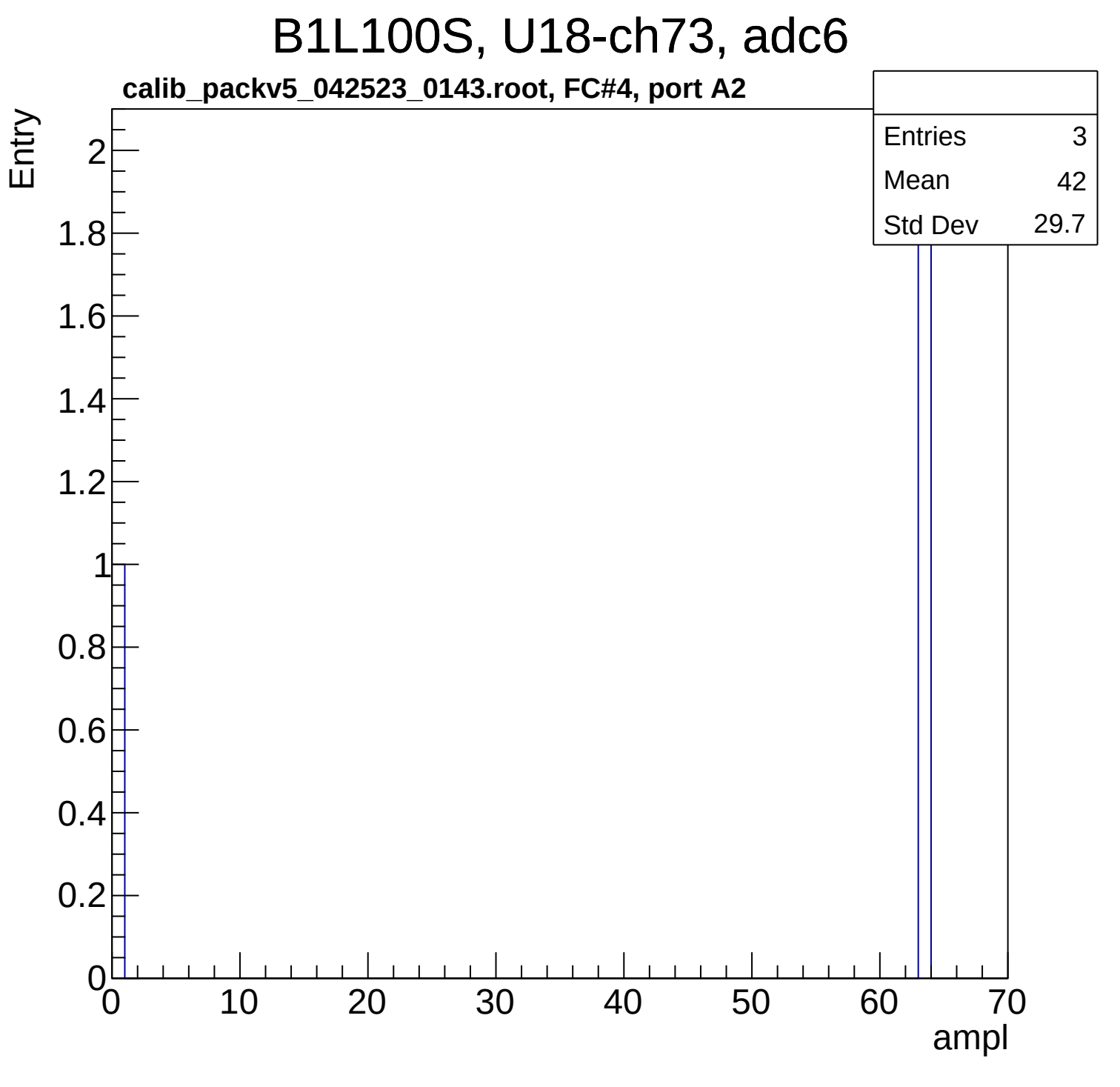

B1L100S, U18-ch73, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 38.29
Std Dev 3.368
Gaus mean : 38.9520
Gaus Width: 3.5730
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

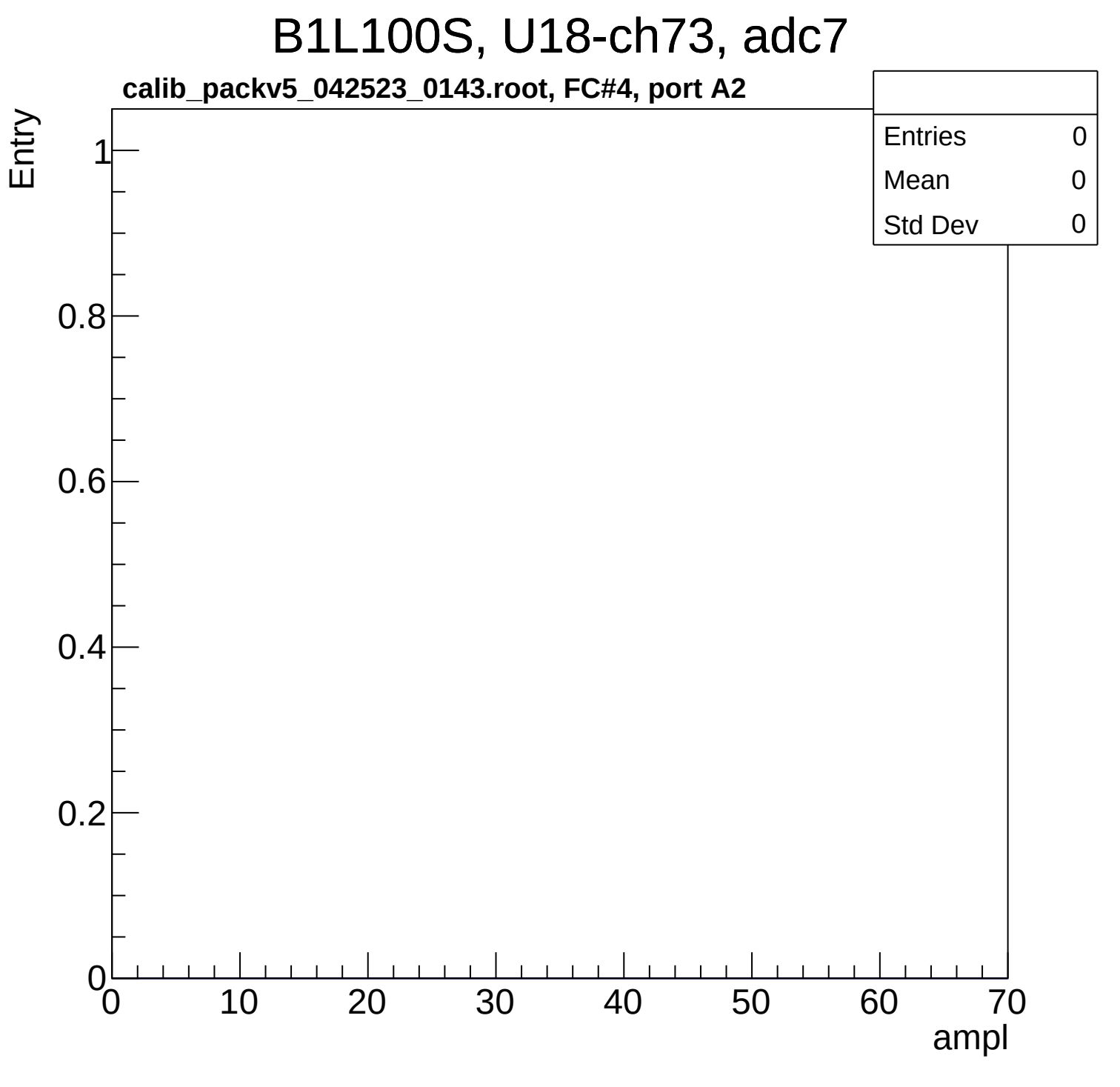

B1L100S, U18-ch73, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 44.63
Std Dev 3.611
Gaus mean : 45.2233
Gaus Width: 4.2116
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

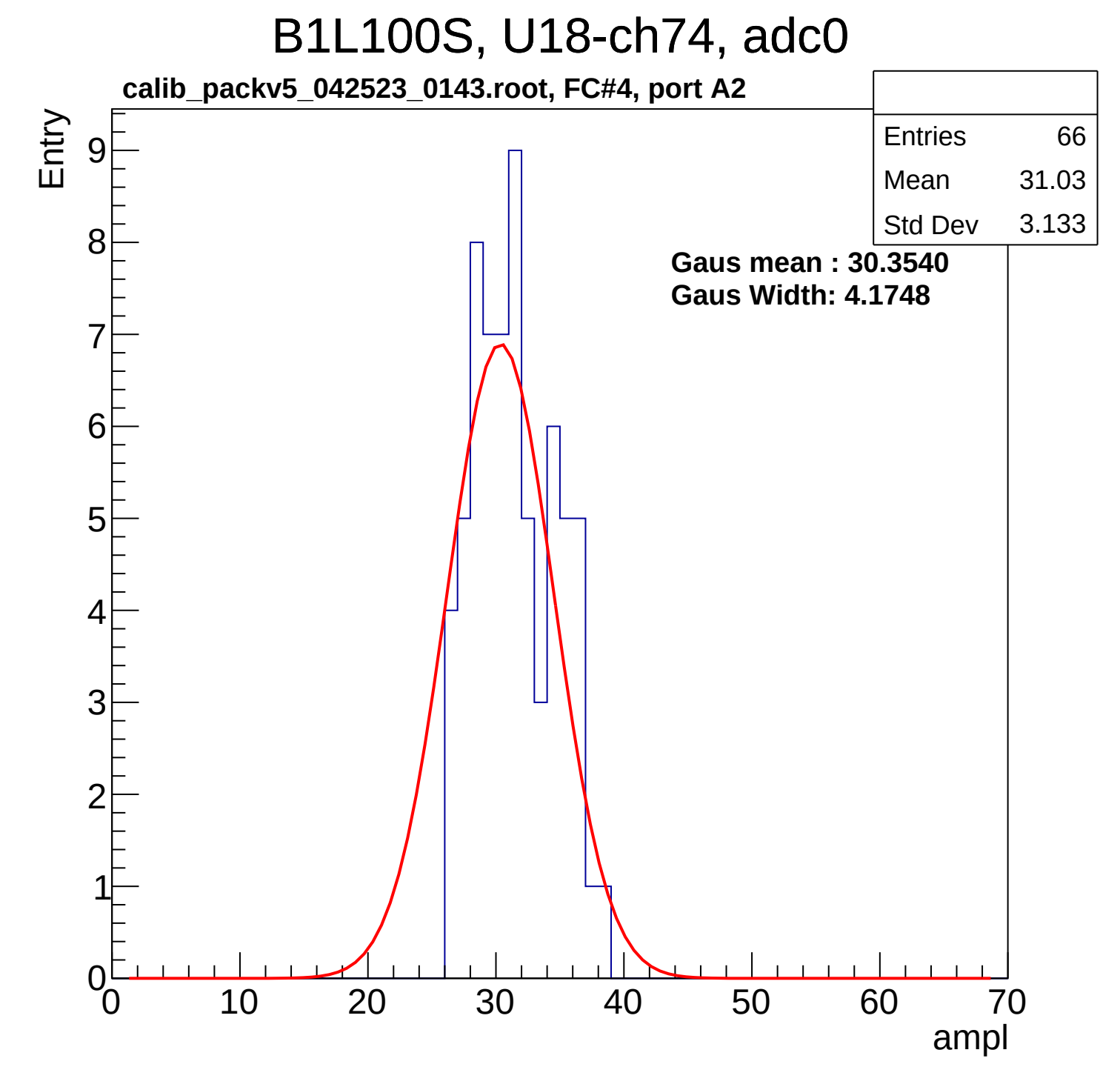

B1L100S, U18-ch73, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 50.51
Std Dev 3.671
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

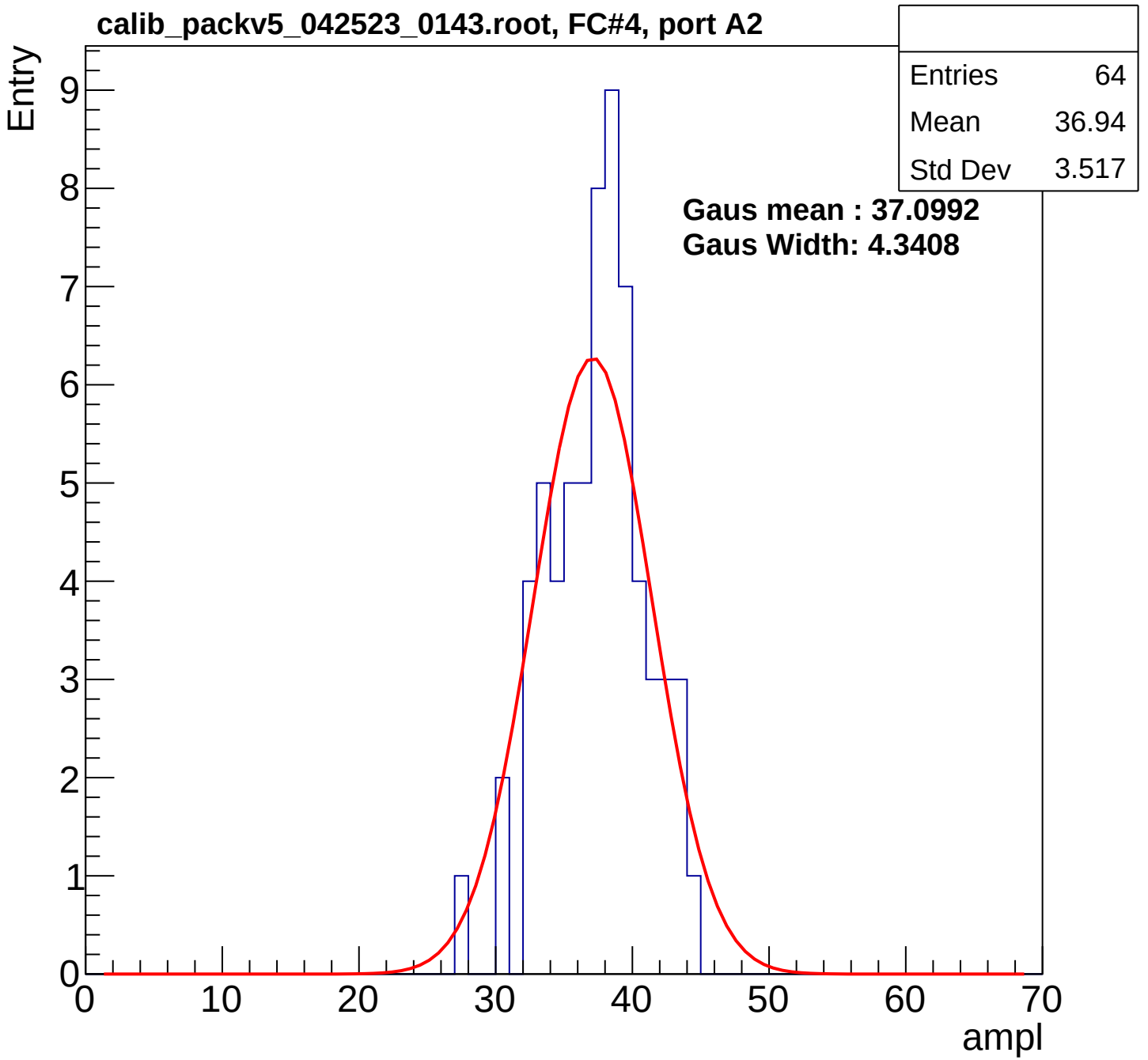

B1L100S, U18-ch73, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 56.28
Std Dev 2.999
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

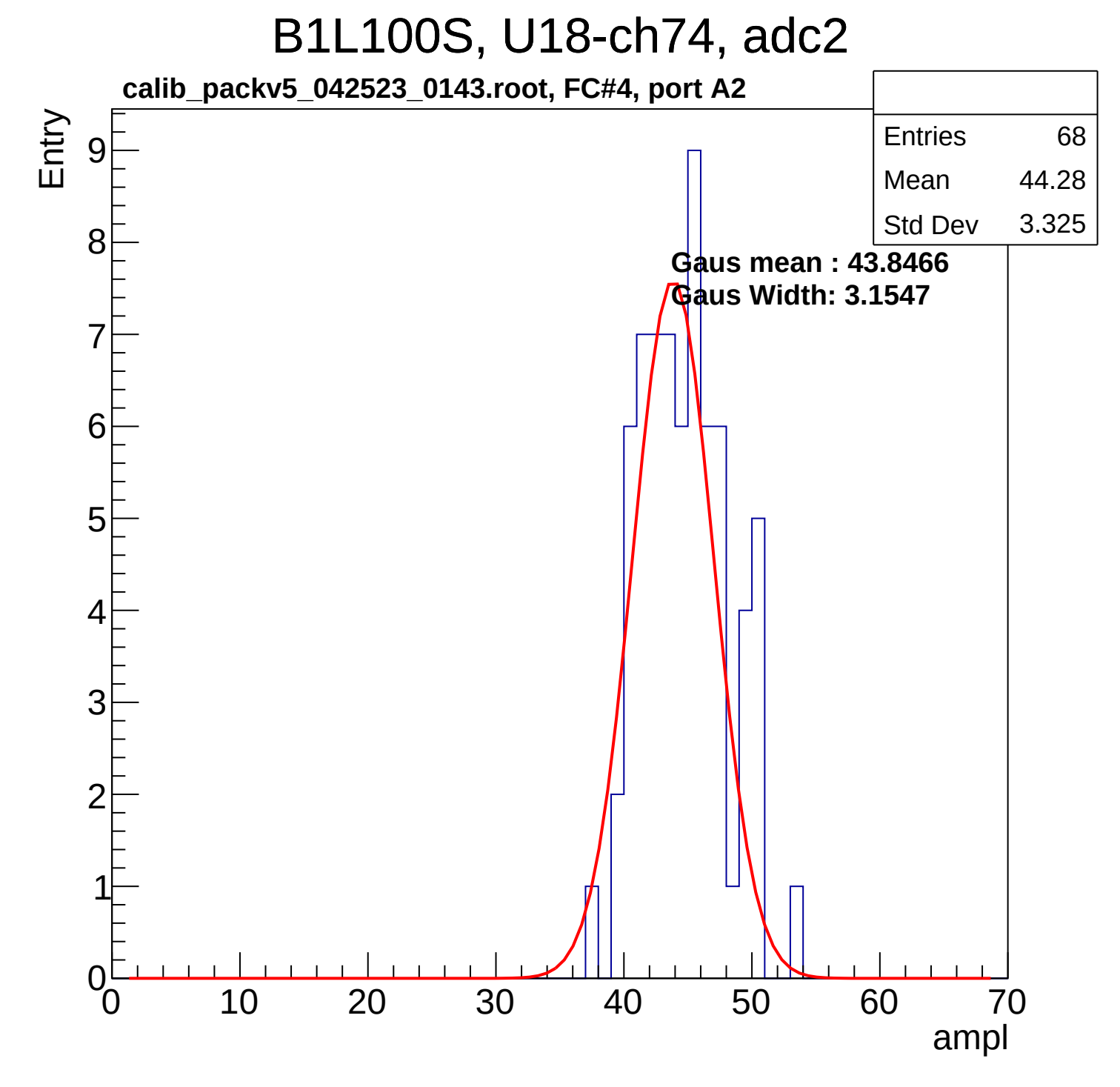

B1L100S, U18-ch73, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 39
Mean 60.64
Std Dev 2.032
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

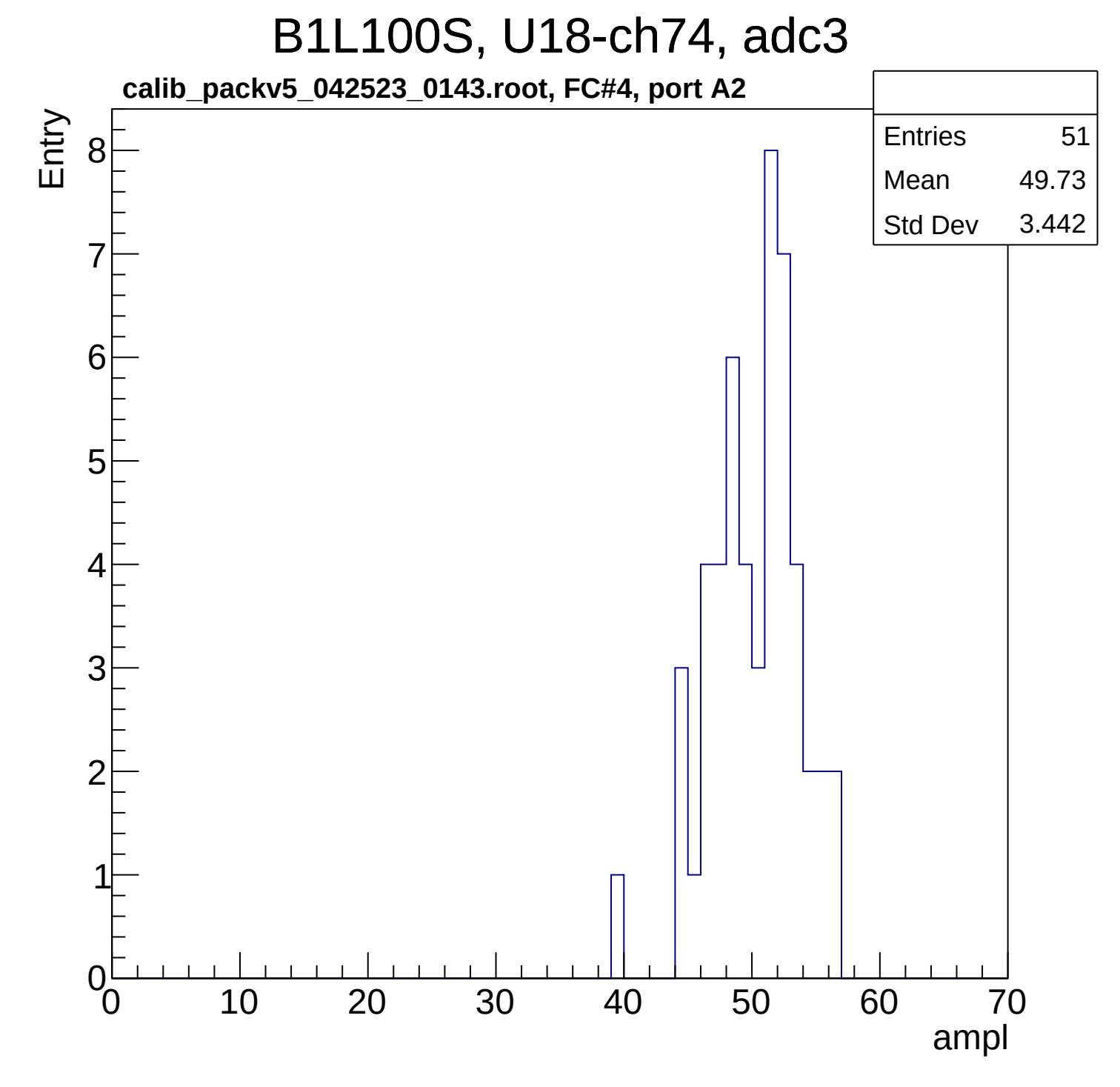

B1L100S, U18-ch73, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 42
Std Dev 29.7
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

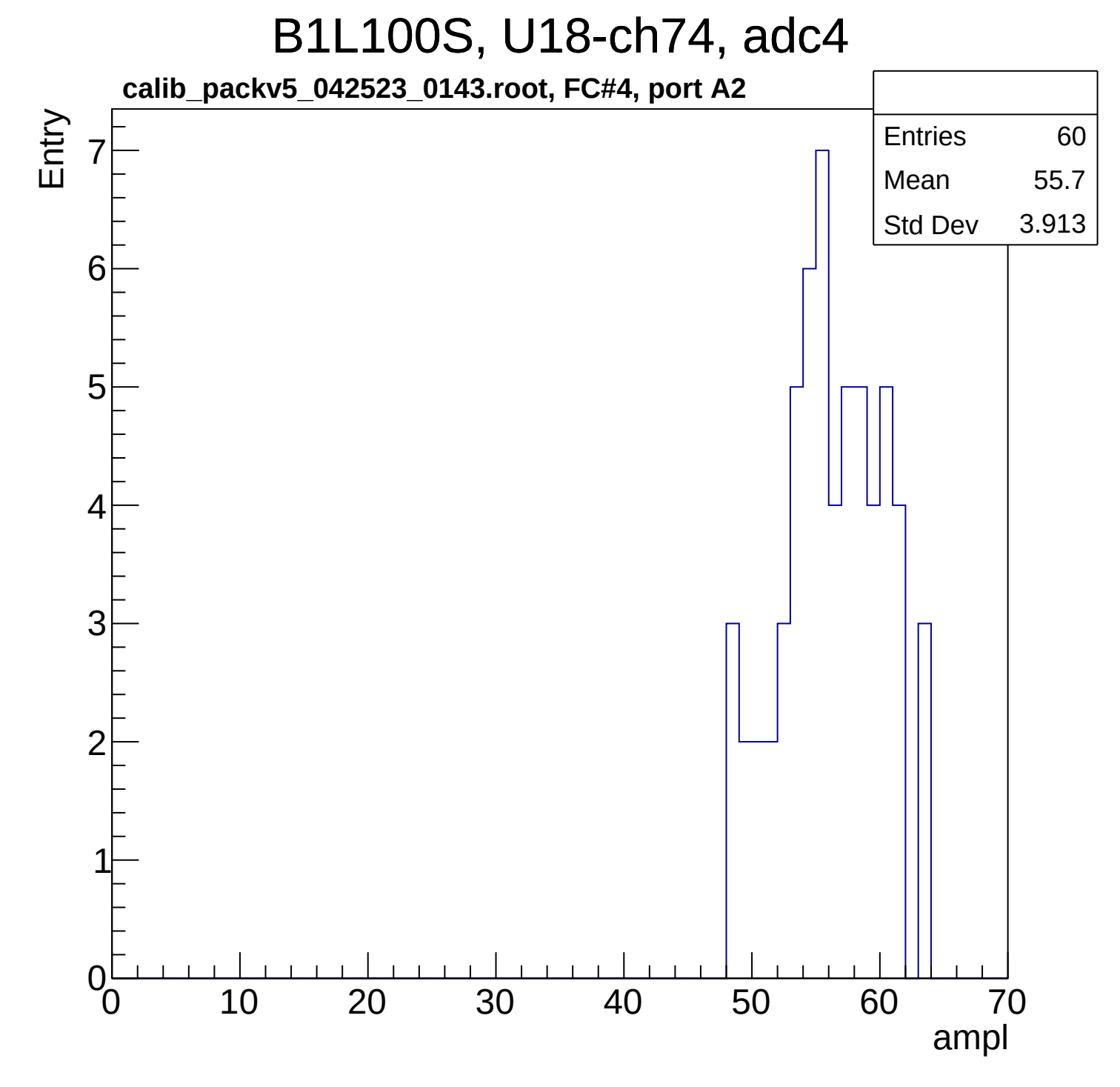

B1L100S, U18-ch73, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

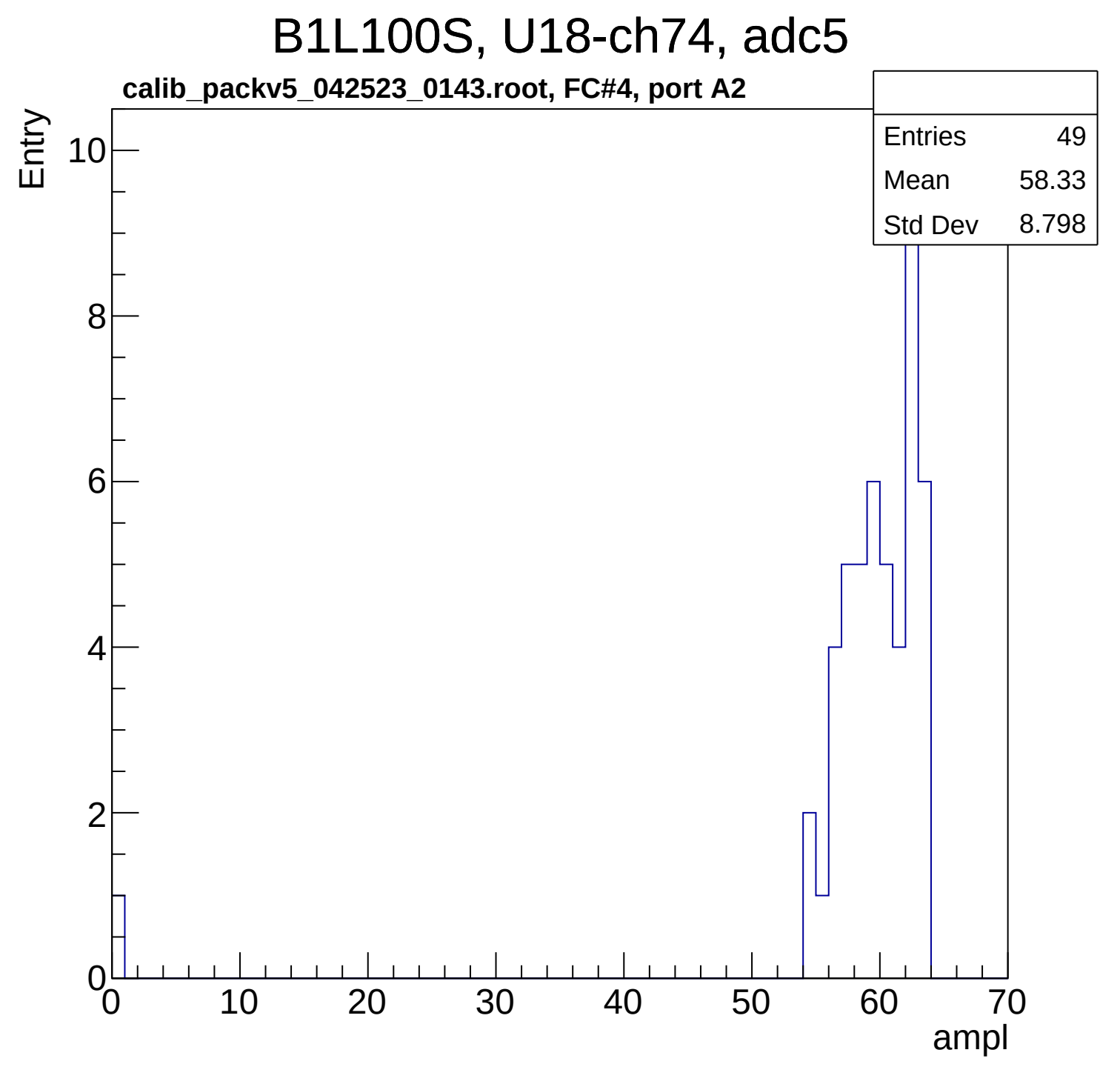

B1L100S, U18-ch74, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 31.03
Std Dev 3.133
Gaus mean : 30.3540
Gaus Width: 4.1748
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

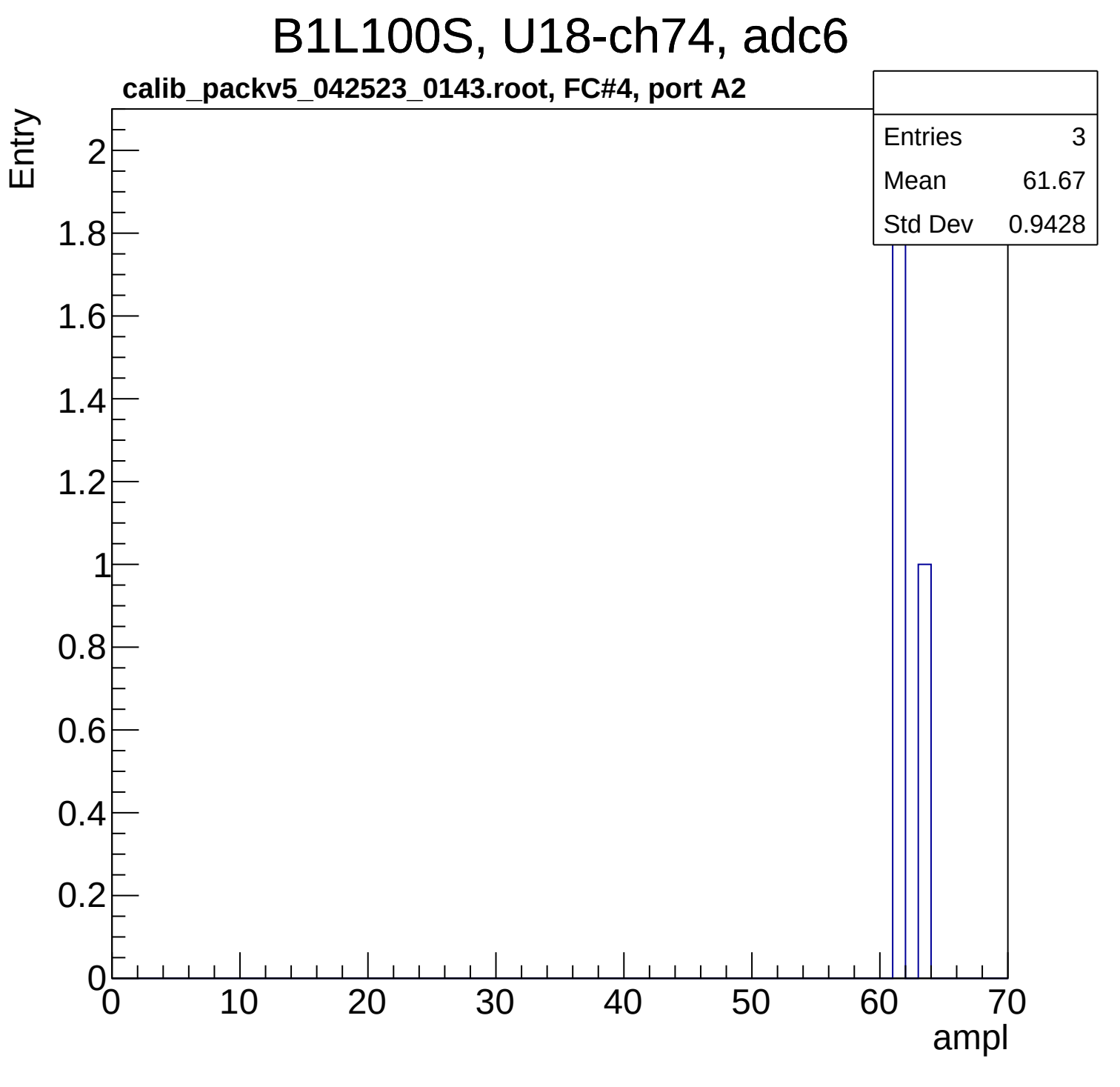

B1L100S, U18-ch74, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 36.94
Std Dev 3.517
Gaus mean : 37.0992
Gaus Width: 4.3408
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

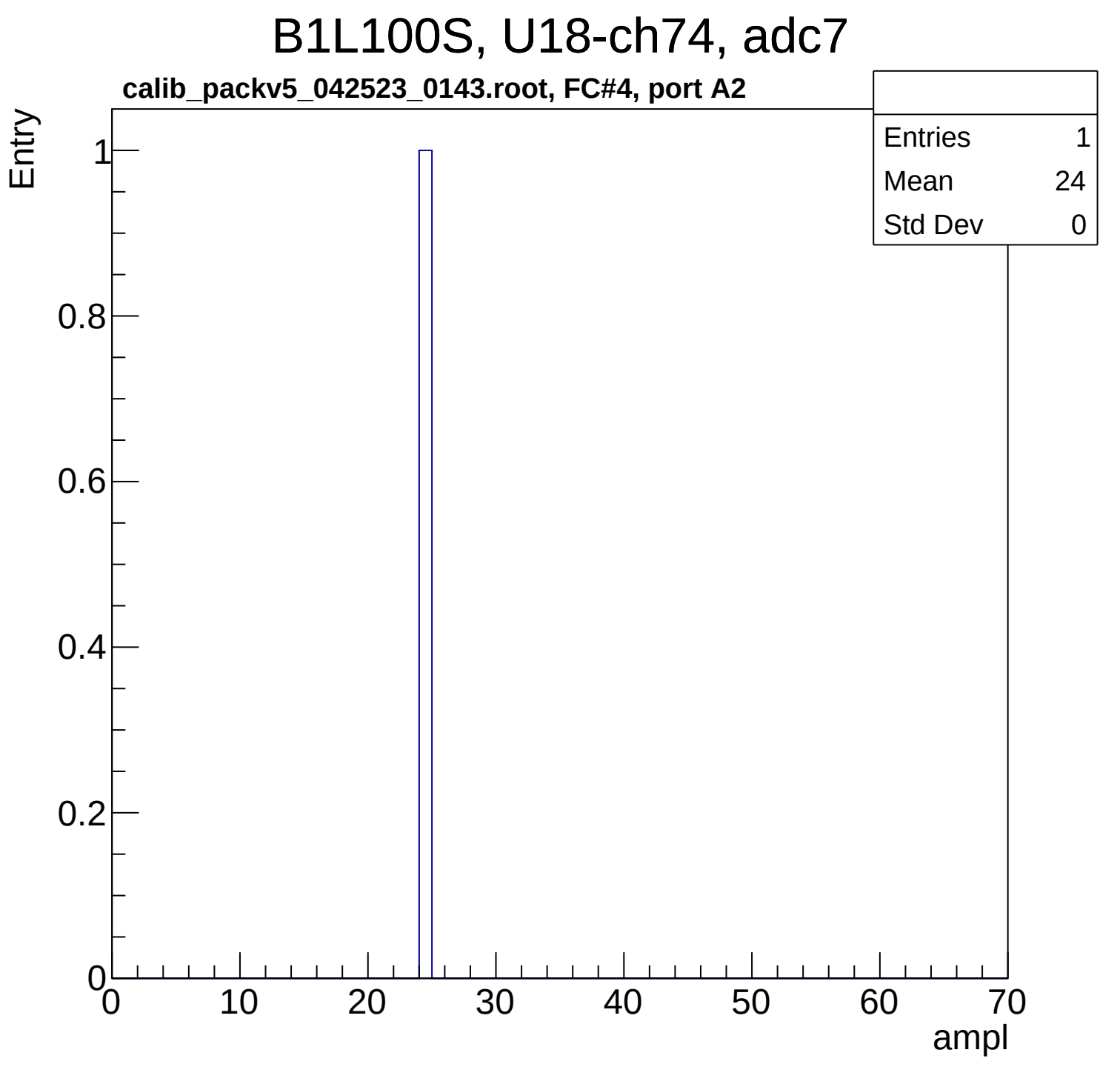

B1L100S, U18-ch74, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 44.28
Std Dev 3.325
Gaus mean : 43.8466
Gaus Width: 3.1547
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

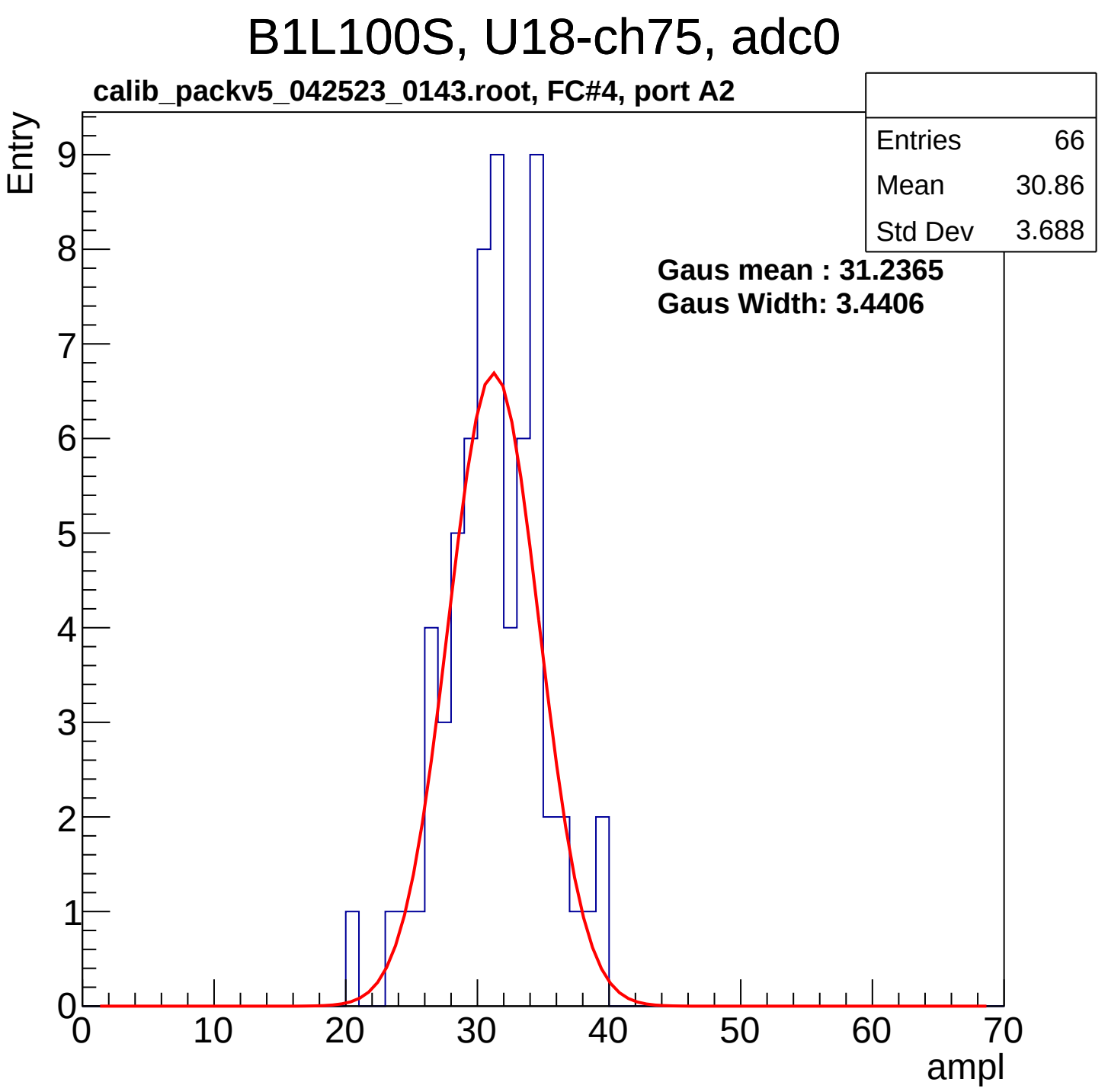

B1L100S, U18-ch74, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 49.73
Std Dev 3.442
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

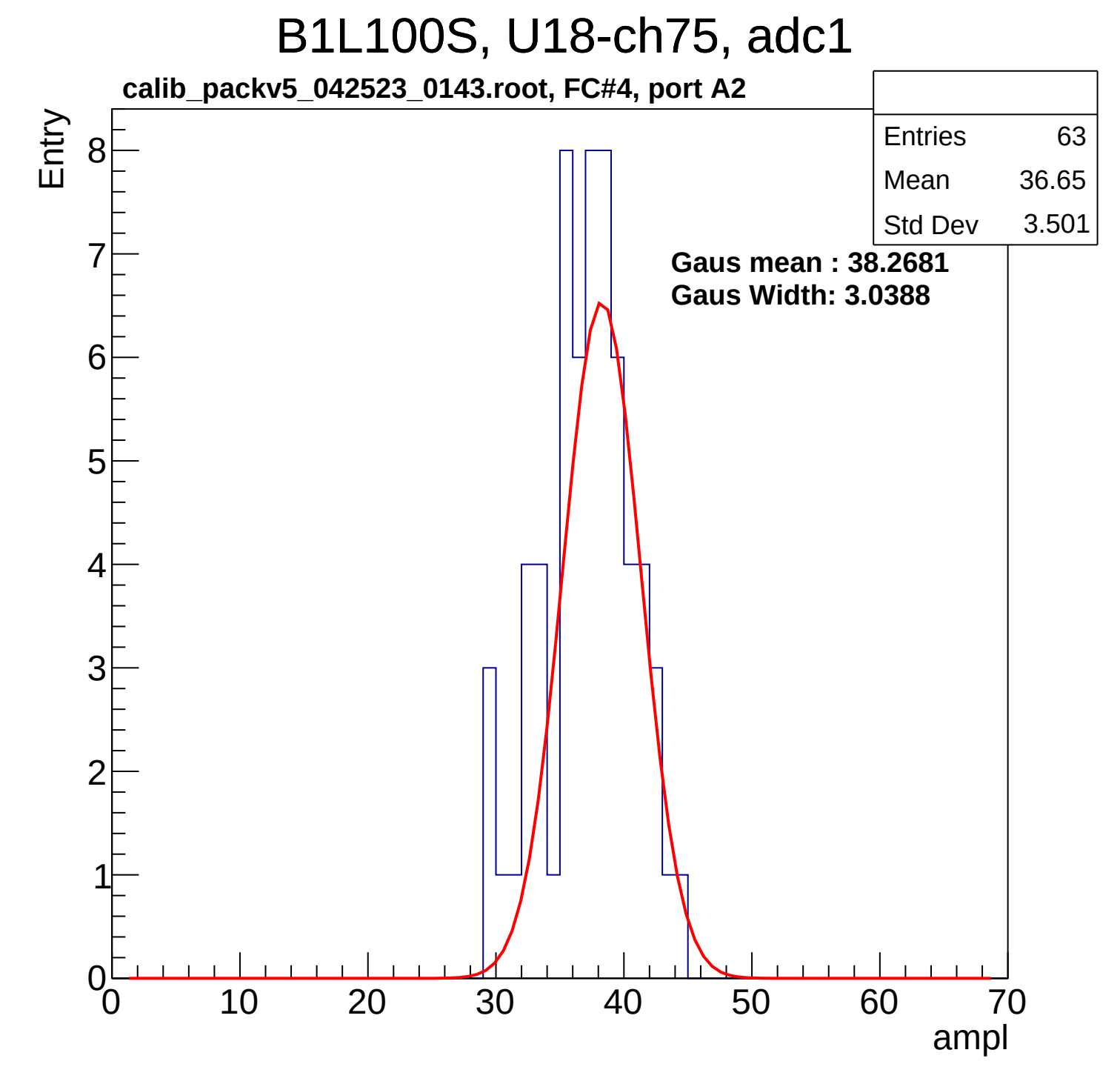

B1L100S, U18-ch74, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 55.7
Std Dev 3.913
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

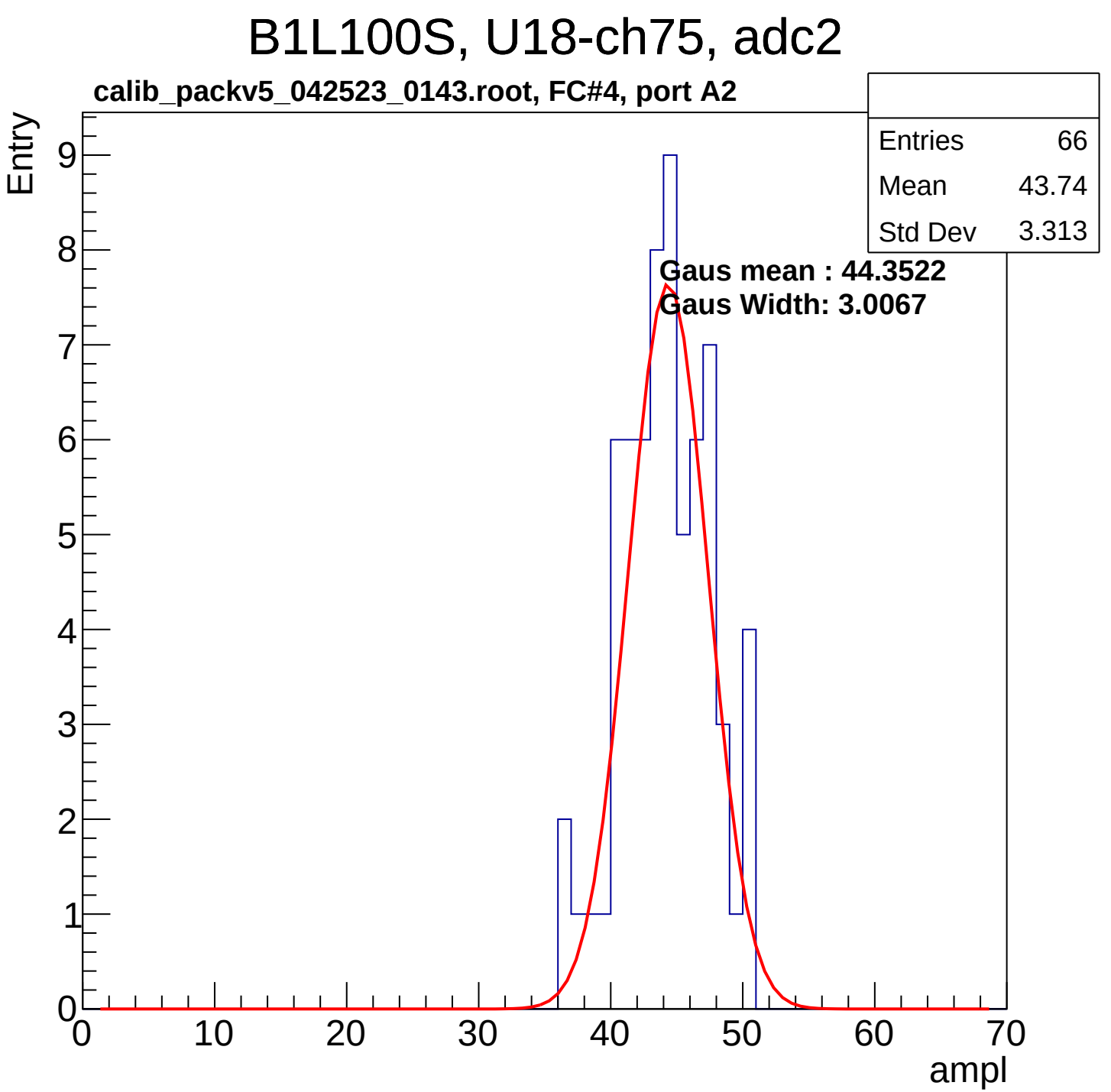

B1L100S, U18-ch74, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 58.33
Std Dev 8.798
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

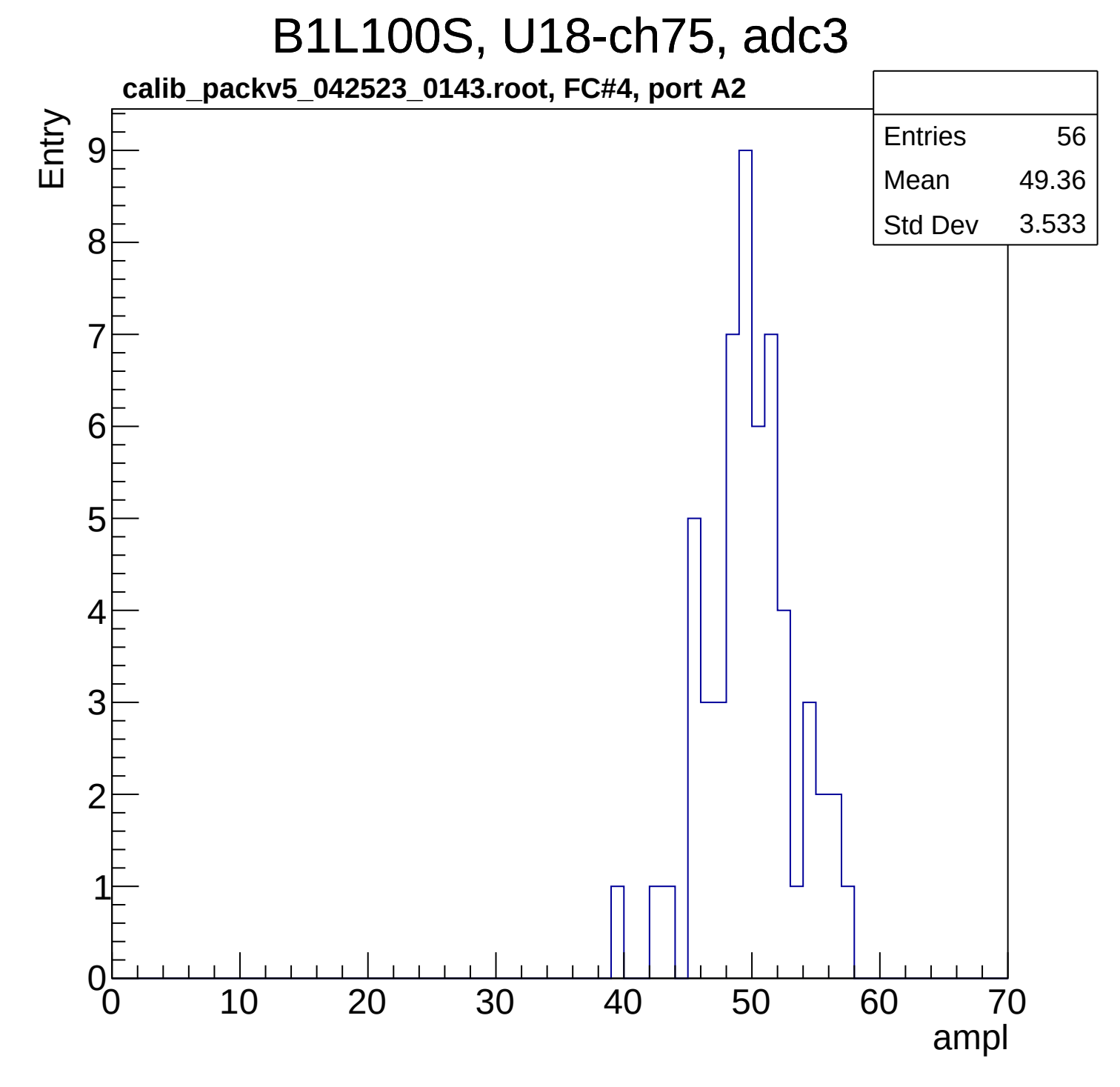

B1L100S, U18-ch74, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 61.67
Std Dev 0.9428
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

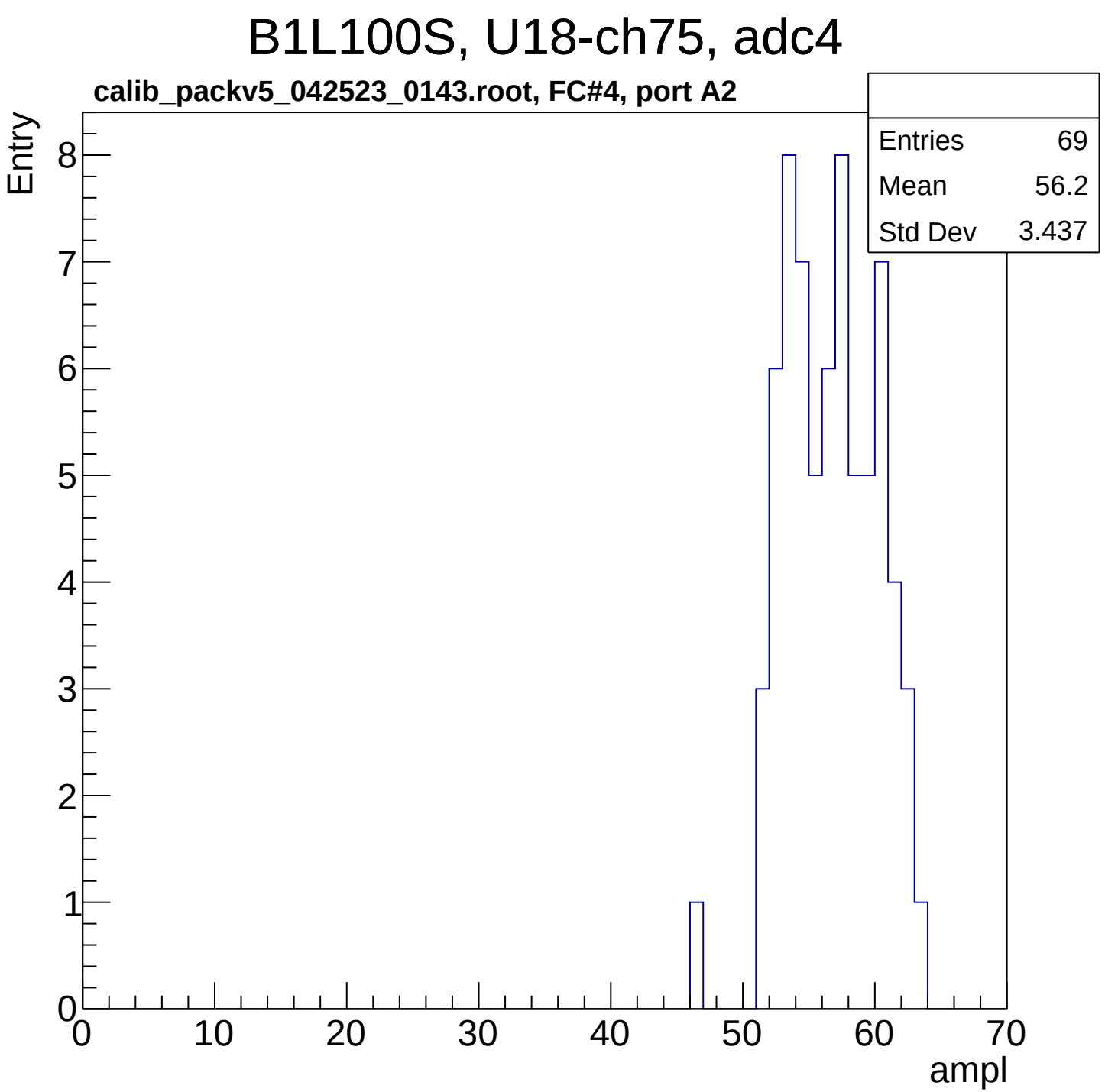

B1L100S, U18-ch74, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 24
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

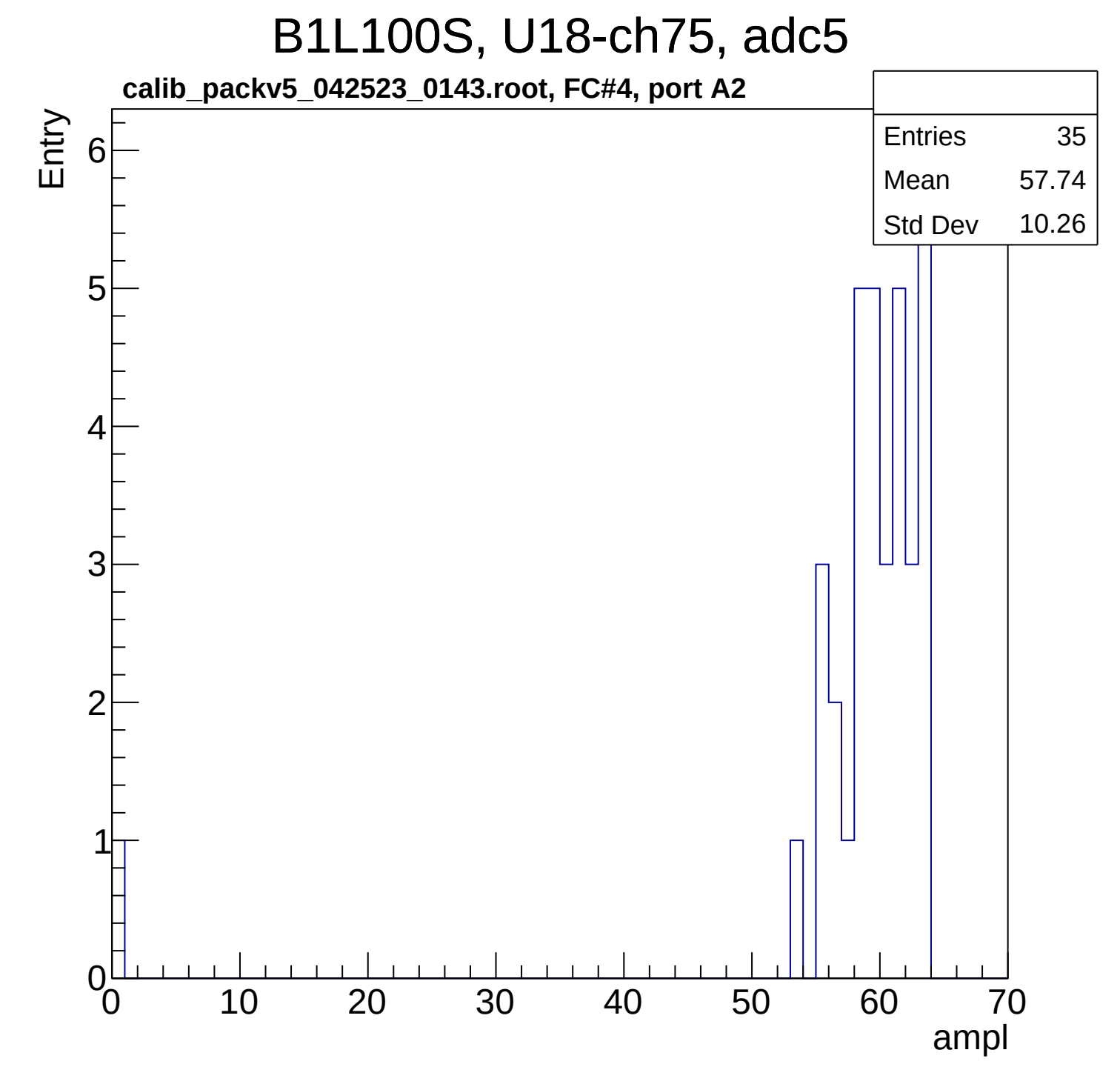

B1L100S, U18-ch75, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 30.86
Std Dev 3.688
Gaus mean : 31.2365
Gaus Width: 3.4406
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

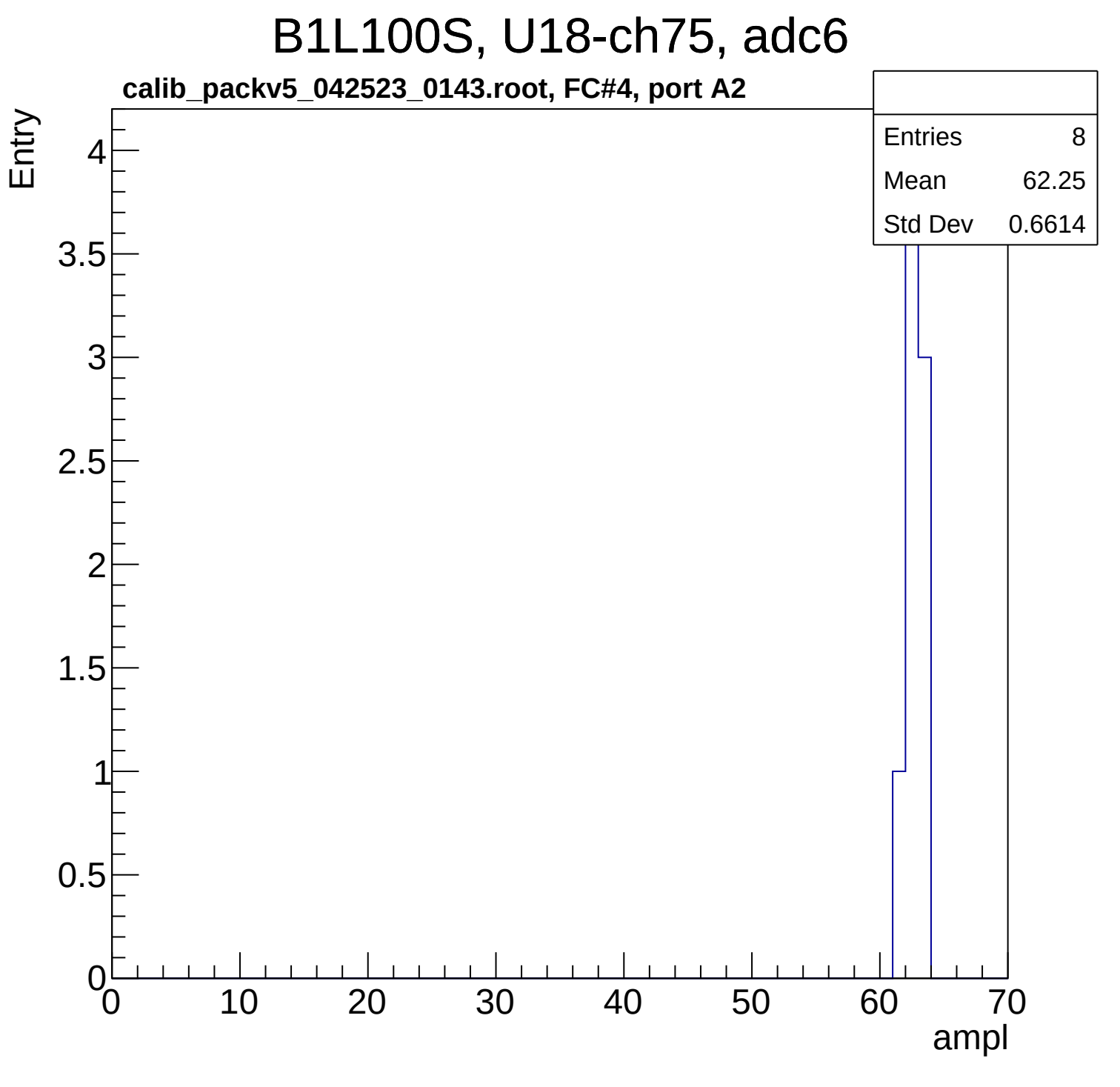

B1L100S, U18-ch75, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 36.65
Std Dev 3.501
Gaus mean : 38.2681
Gaus Width: 3.0388
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

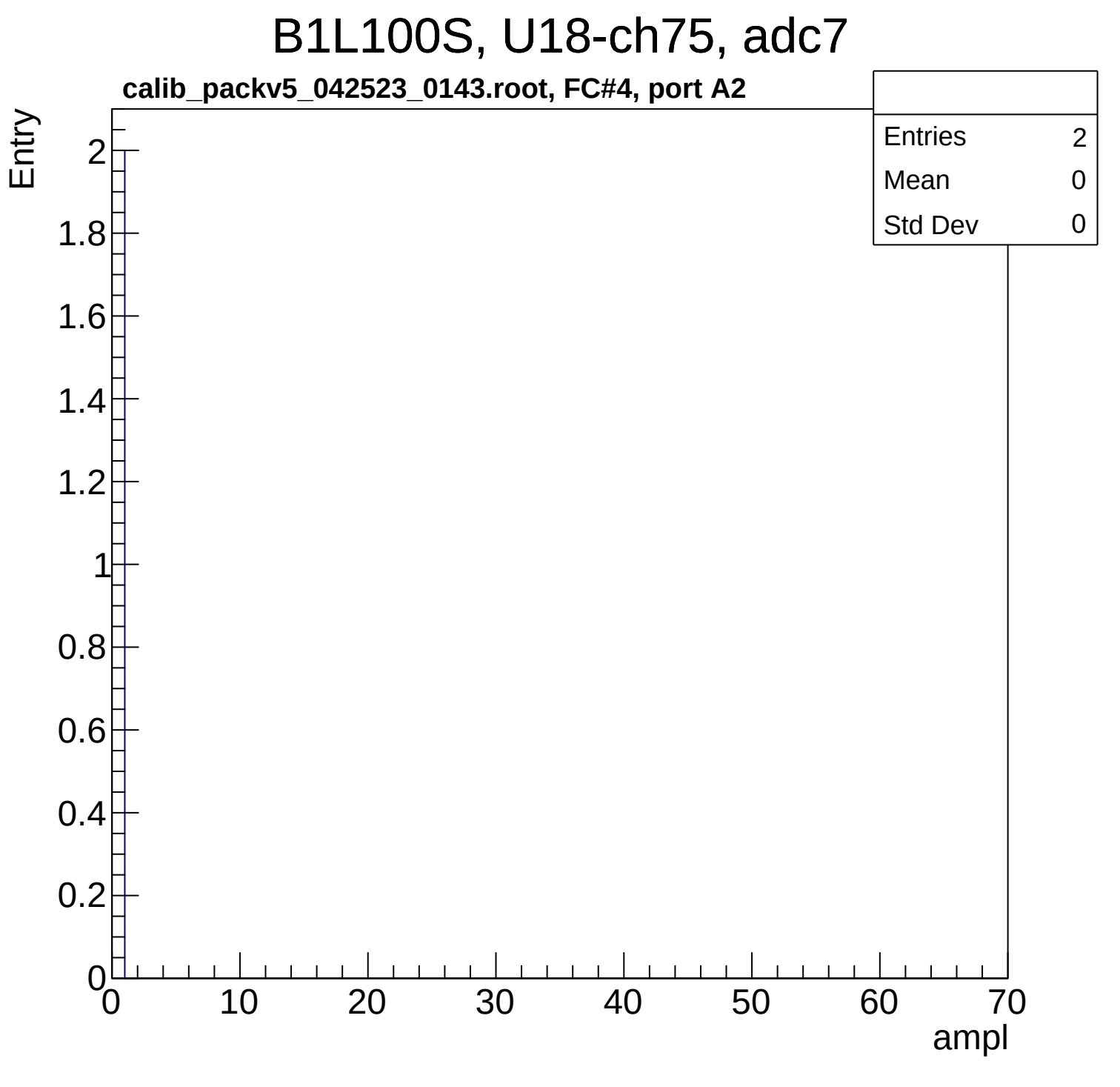

B1L100S, U18-ch75, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 43.74
Std Dev 3.313
Gaus mean : 44.3522
Gaus Width: 3.0067
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

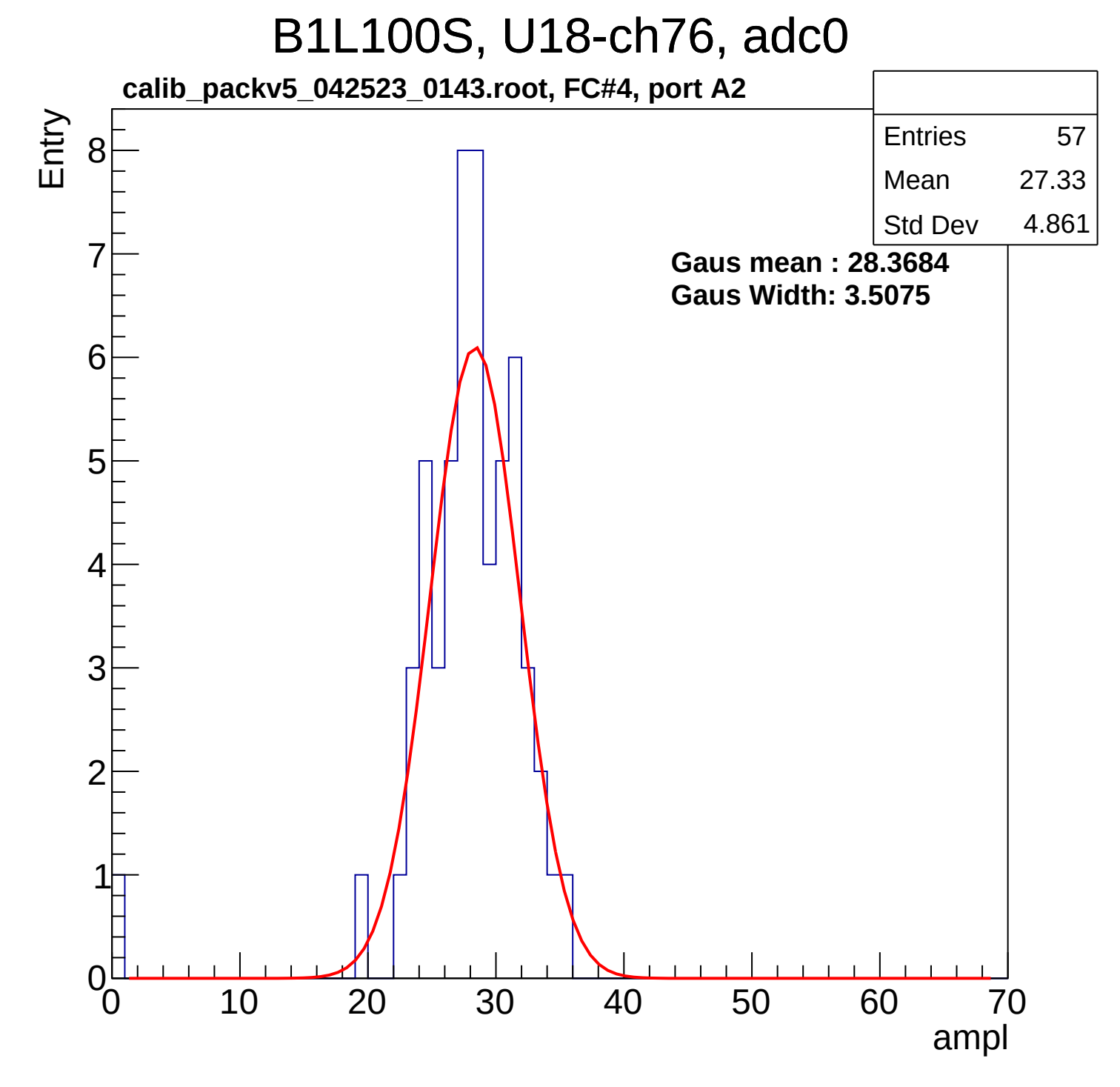

B1L100S, U18-ch75, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 49.36
Std Dev 3.533
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

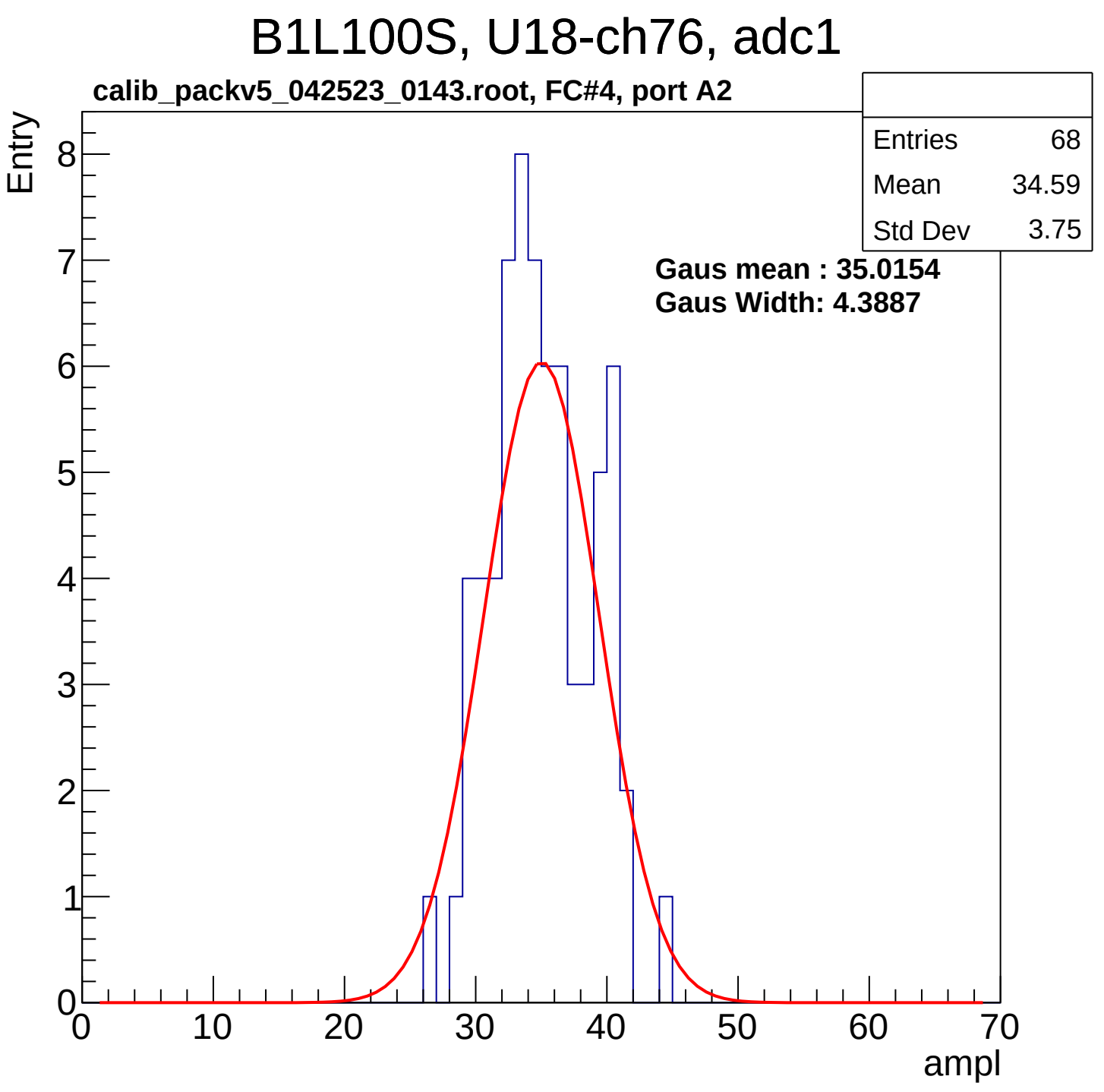

B1L100S, U18-ch75, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 56.2
Std Dev 3.437
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

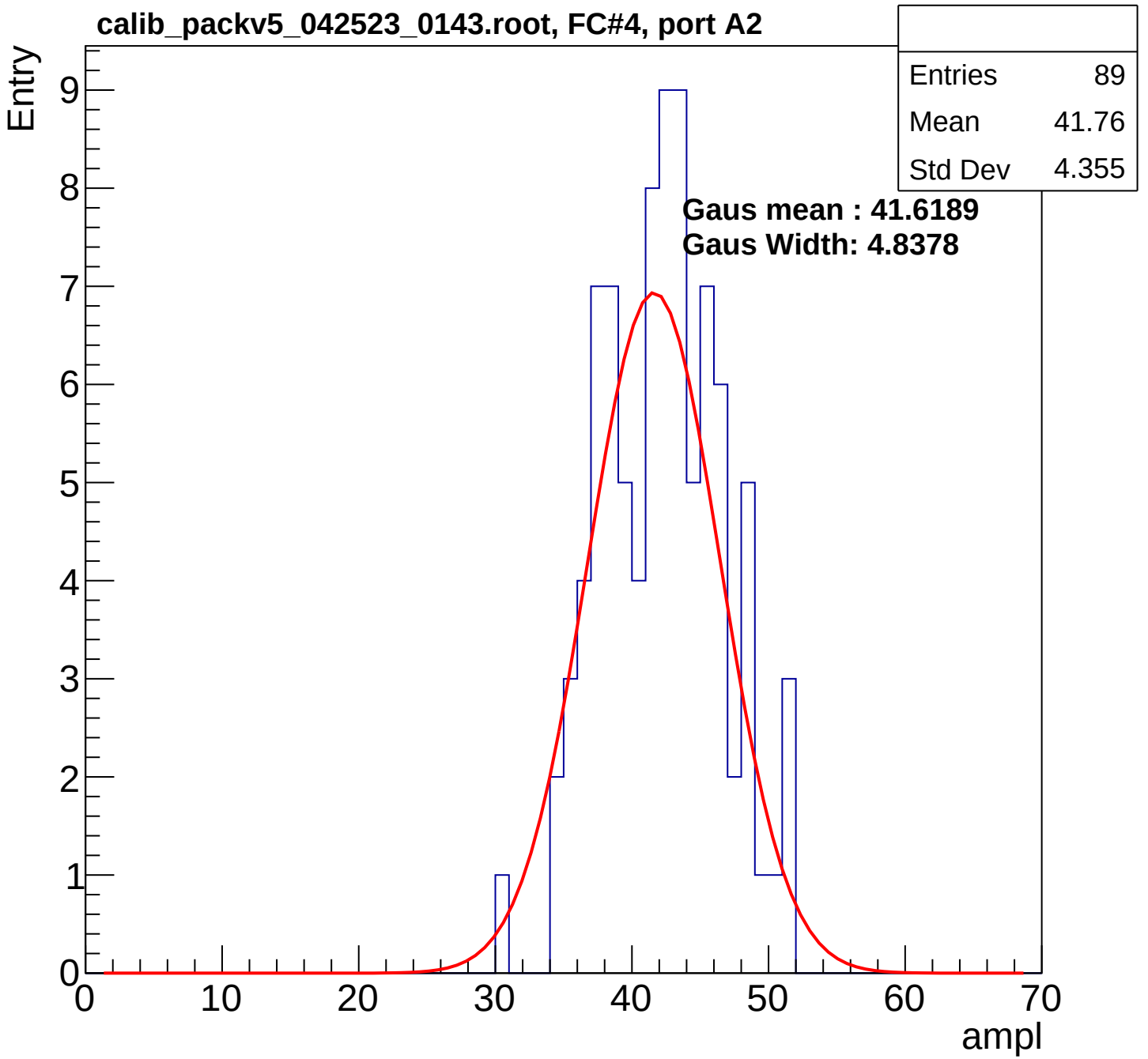

B1L100S, U18-ch75, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 35
Mean 57.74
Std Dev 10.26
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

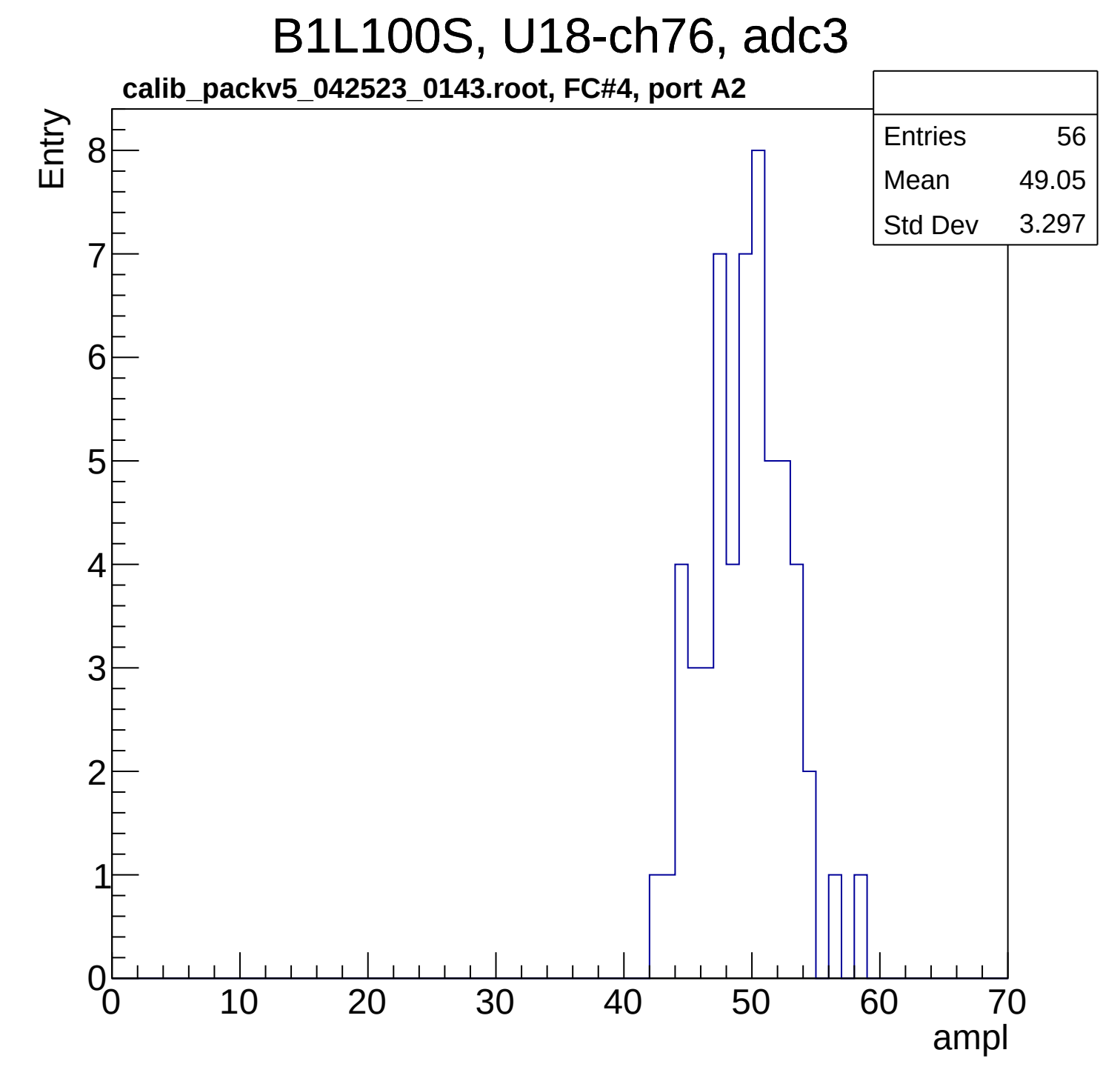

B1L100S, U18-ch75, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 8
Mean 62.25
Std Dev 0.6614
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

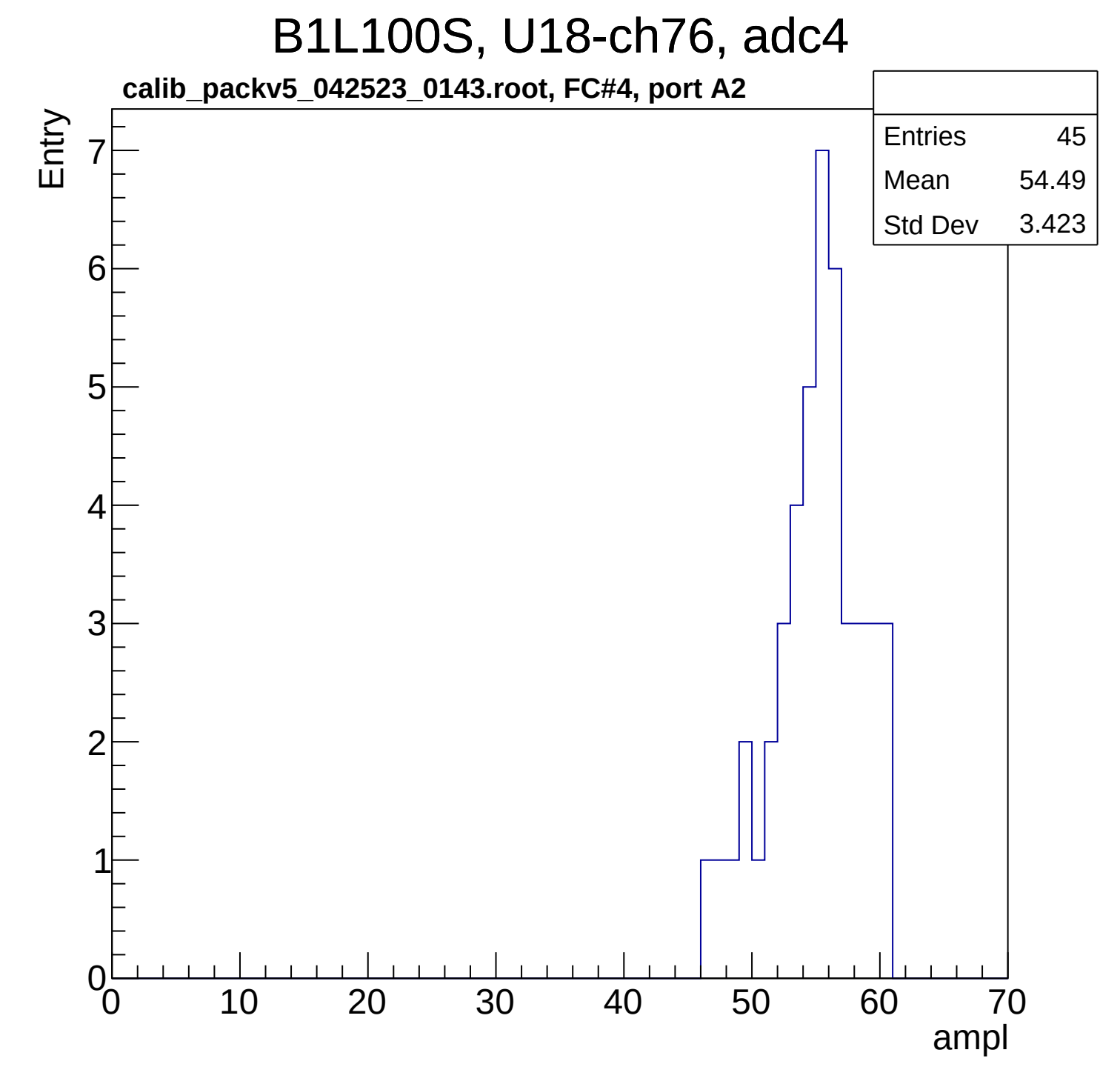

B1L100S, U18-ch75, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

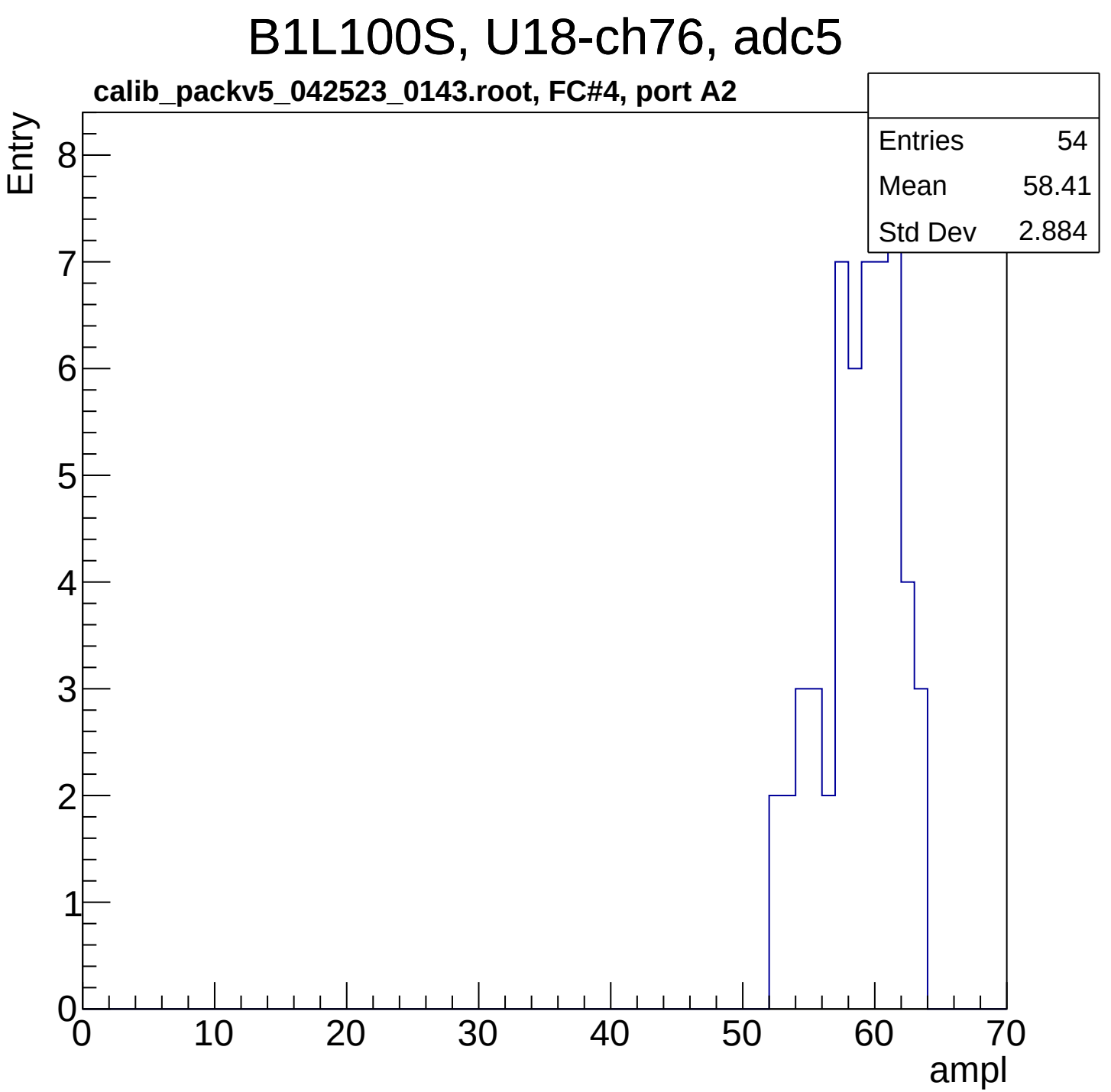

B1L100S, U18-ch76, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 27.33
Std Dev 4.861
Gaus mean : 28.3684
Gaus Width: 3.5075
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

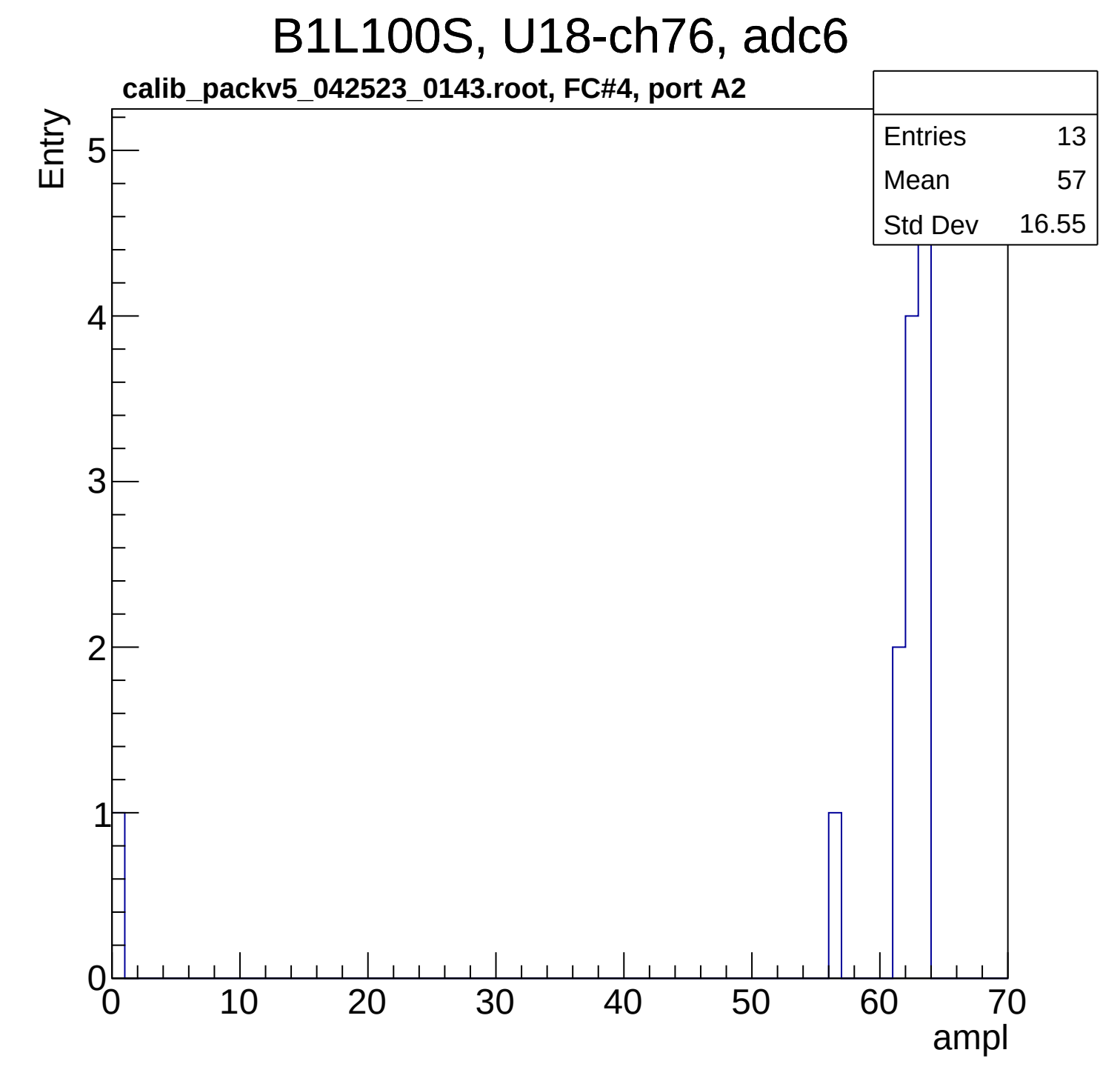

B1L100S, U18-ch76, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 34.59
Std Dev 3.75
Gaus mean : 35.0154
Gaus Width: 4.3887
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

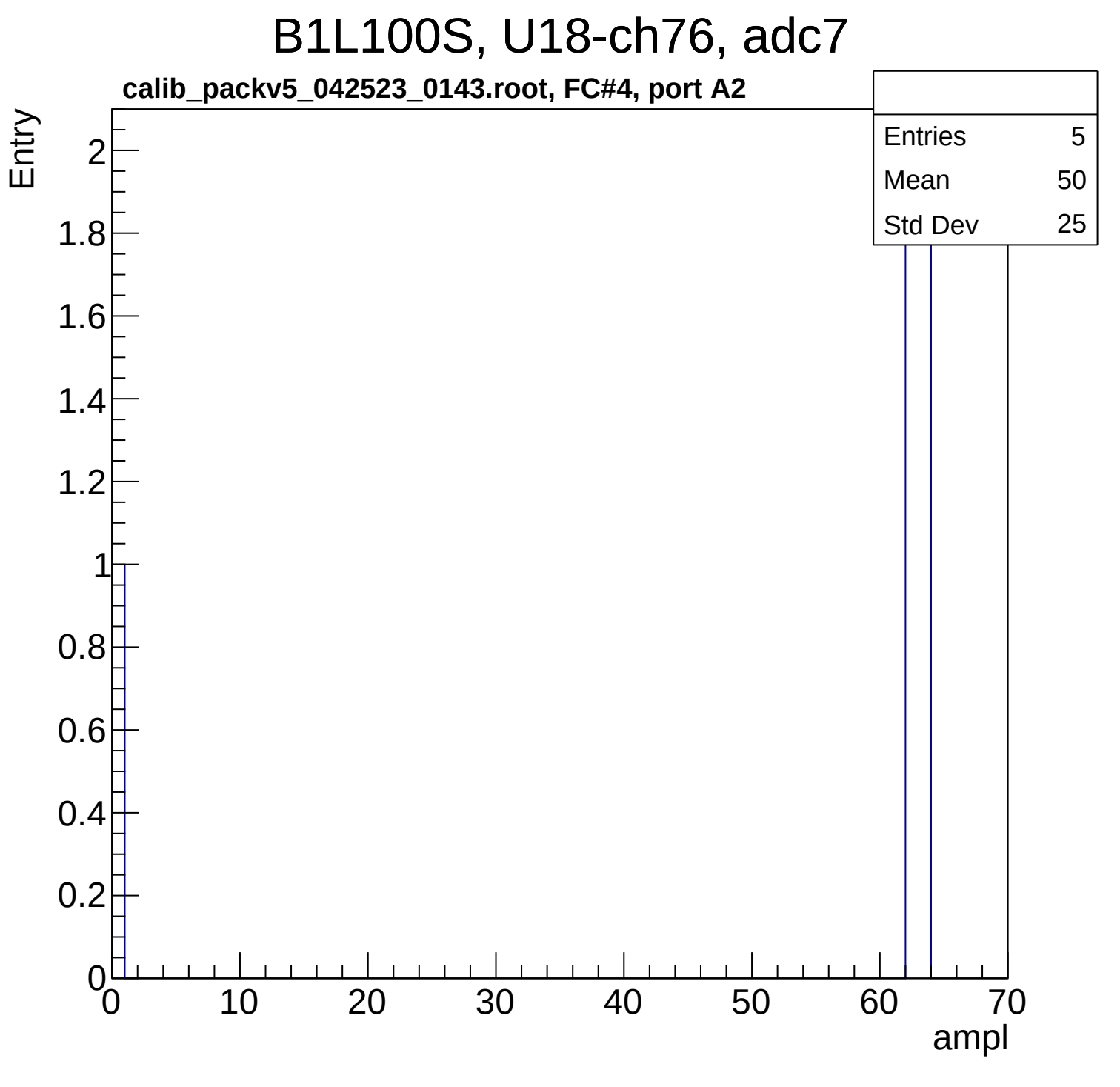

B1L100S, U18-ch76, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 89
Mean 41.76
Std Dev 4.355
Gaus mean : 41.6189
Gaus Width: 4.8378
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

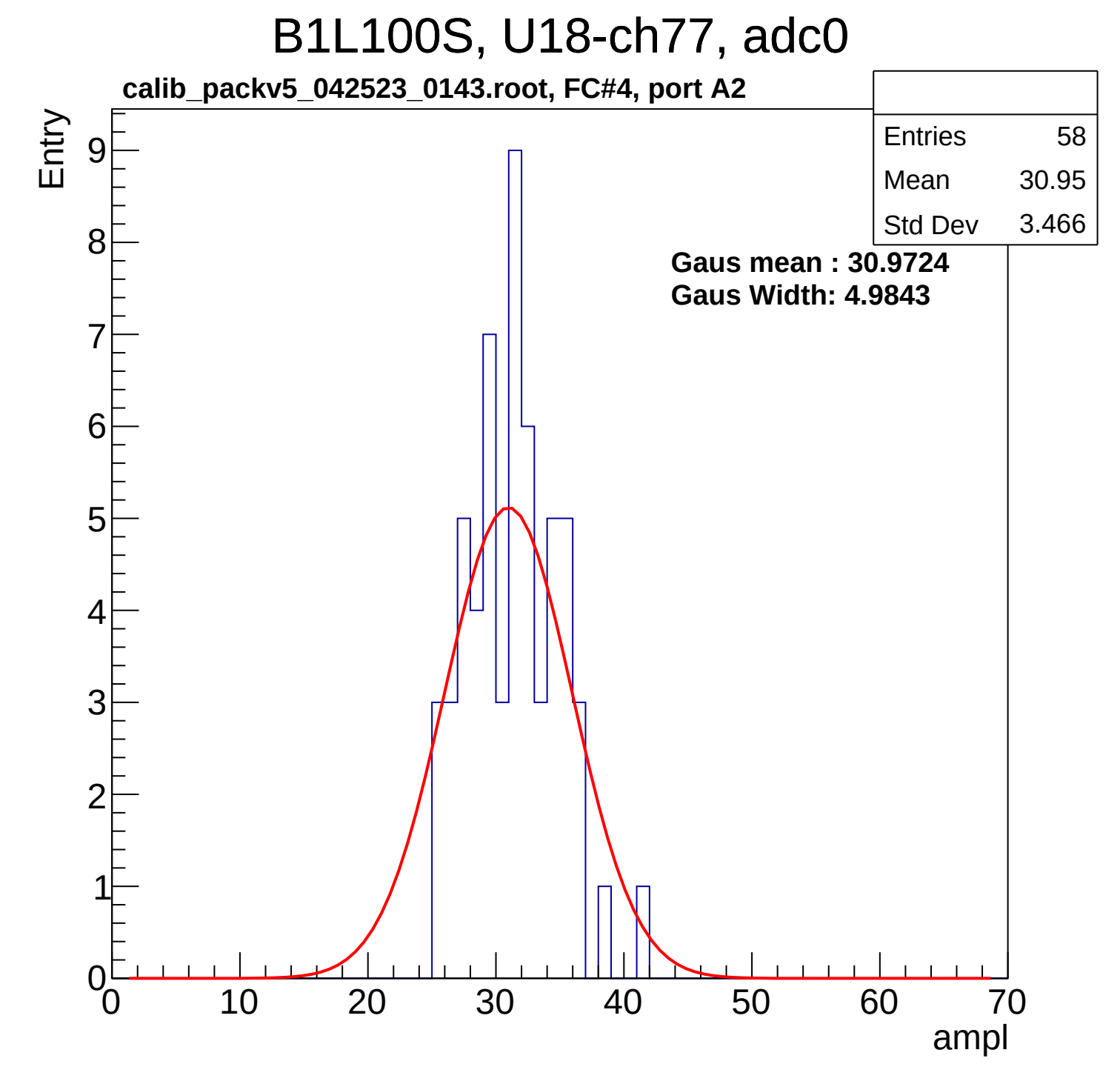

B1L100S, U18-ch76, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 49.05
Std Dev 3.297
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

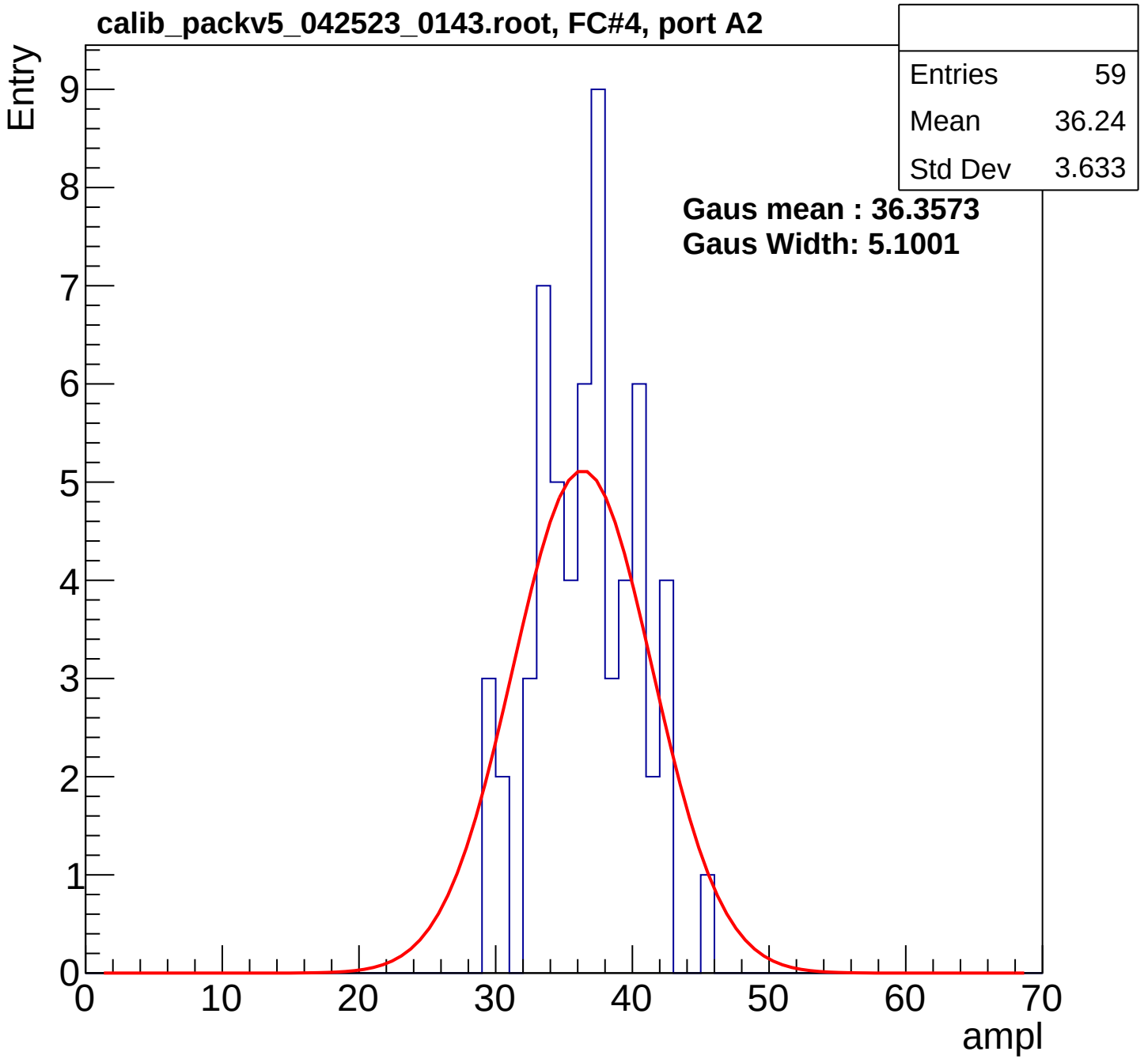

B1L100S, U18-ch76, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 45
Mean 54.49
Std Dev 3.423
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

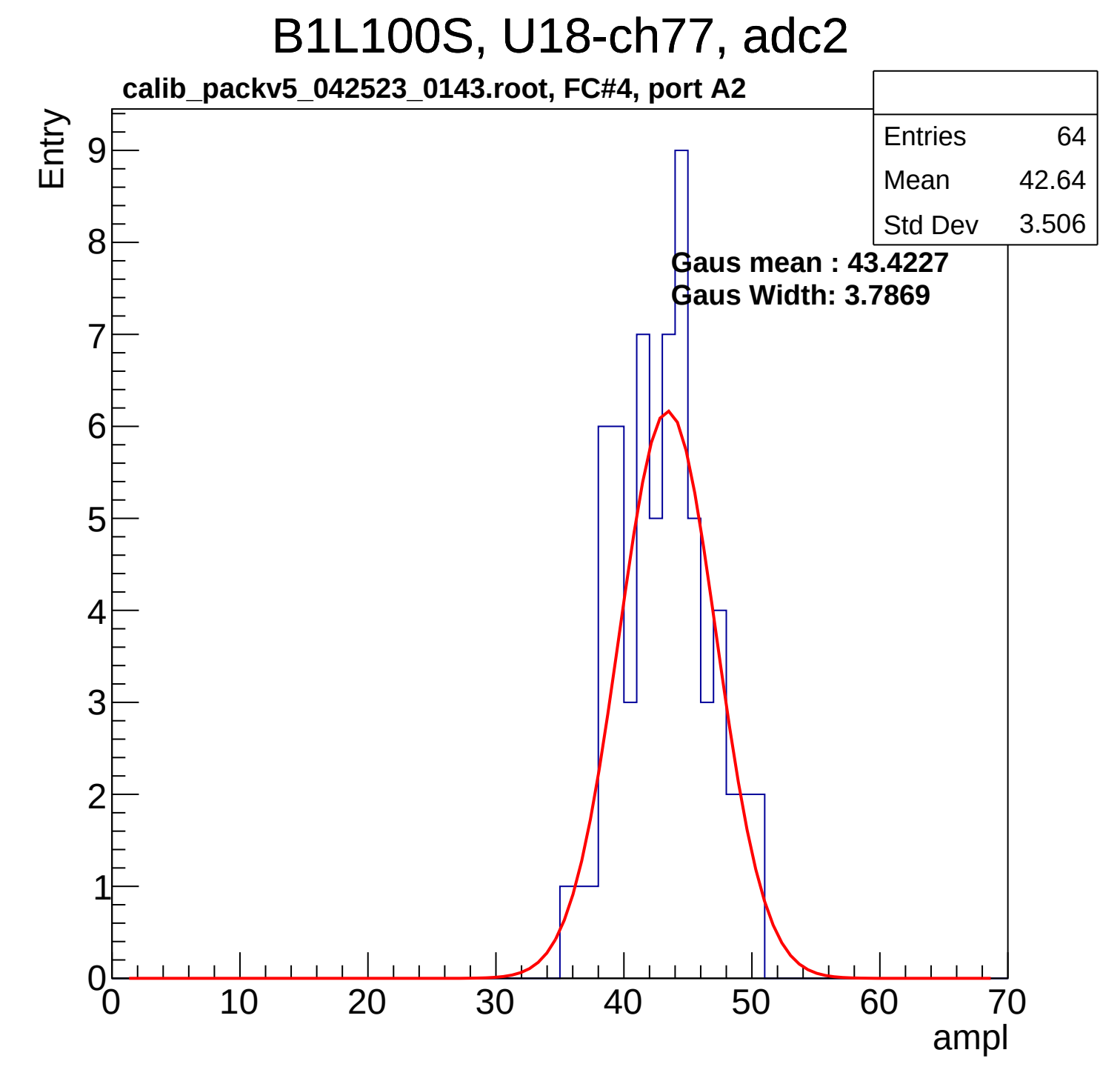

B1L100S, U18-ch76, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 58.41
Std Dev 2.884
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

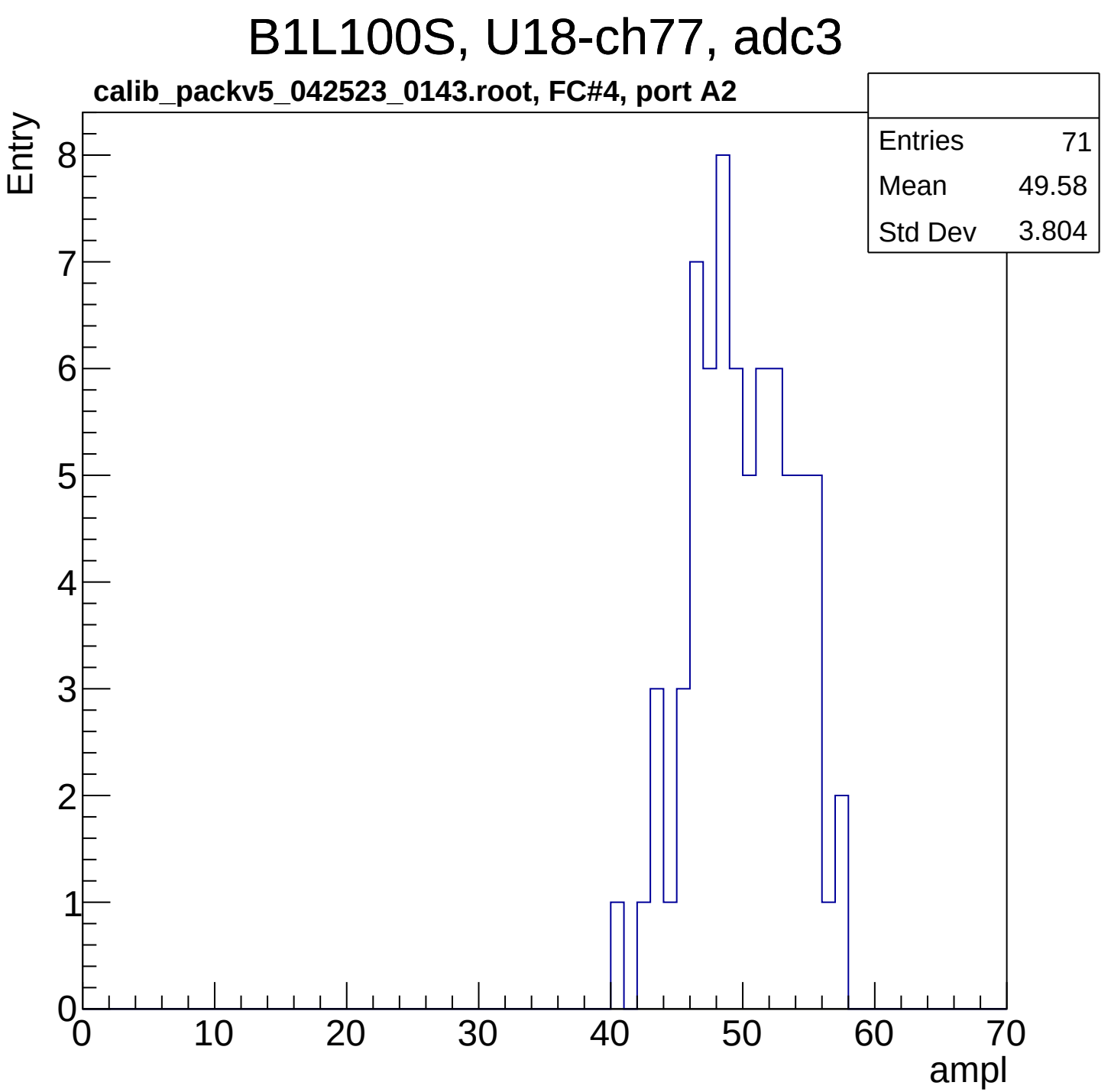

B1L100S, U18-ch76, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 13
Mean 57
Std Dev 16.55
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

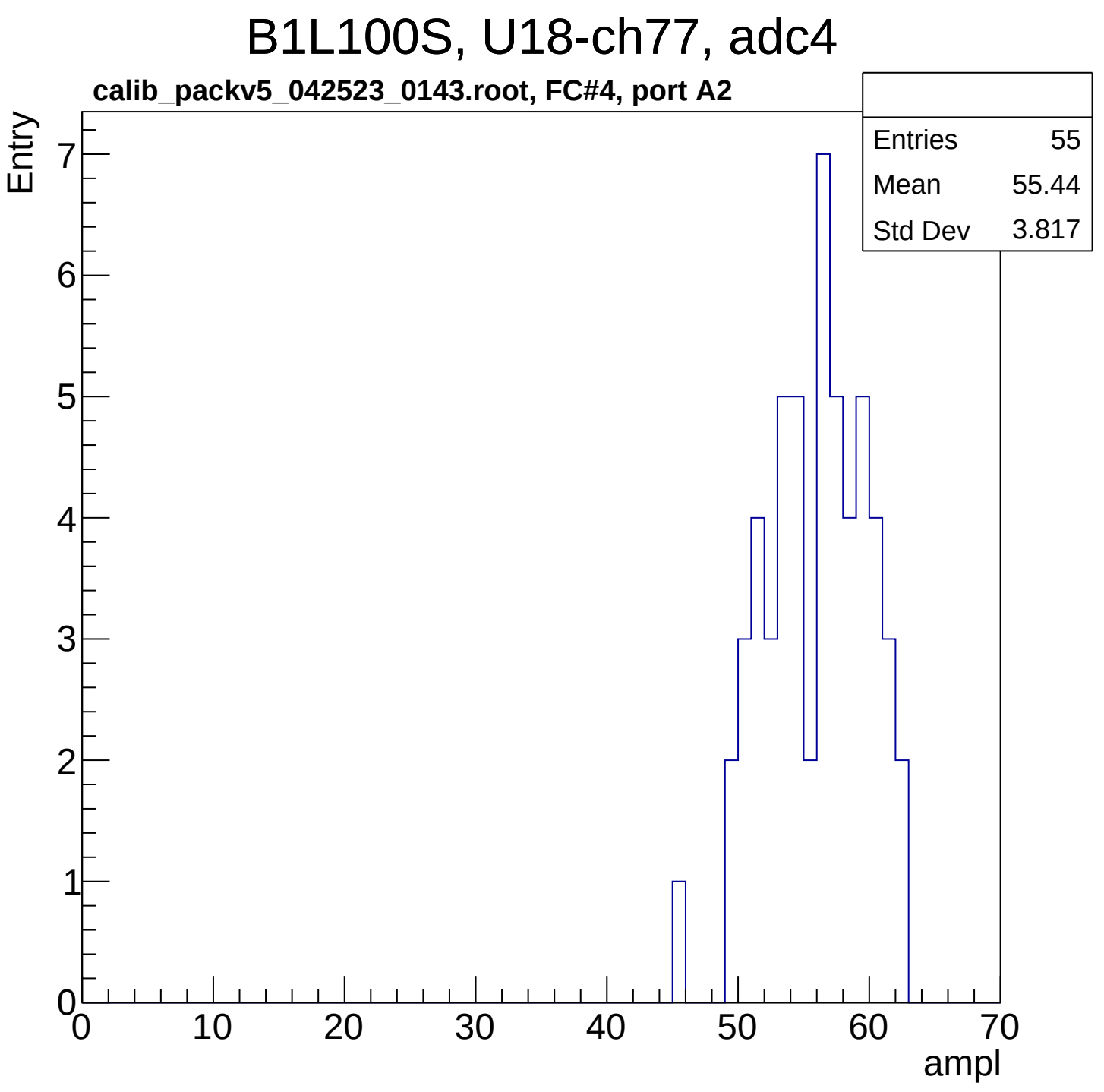

B1L100S, U18-ch76, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 5
Mean 50
Std Dev 25
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

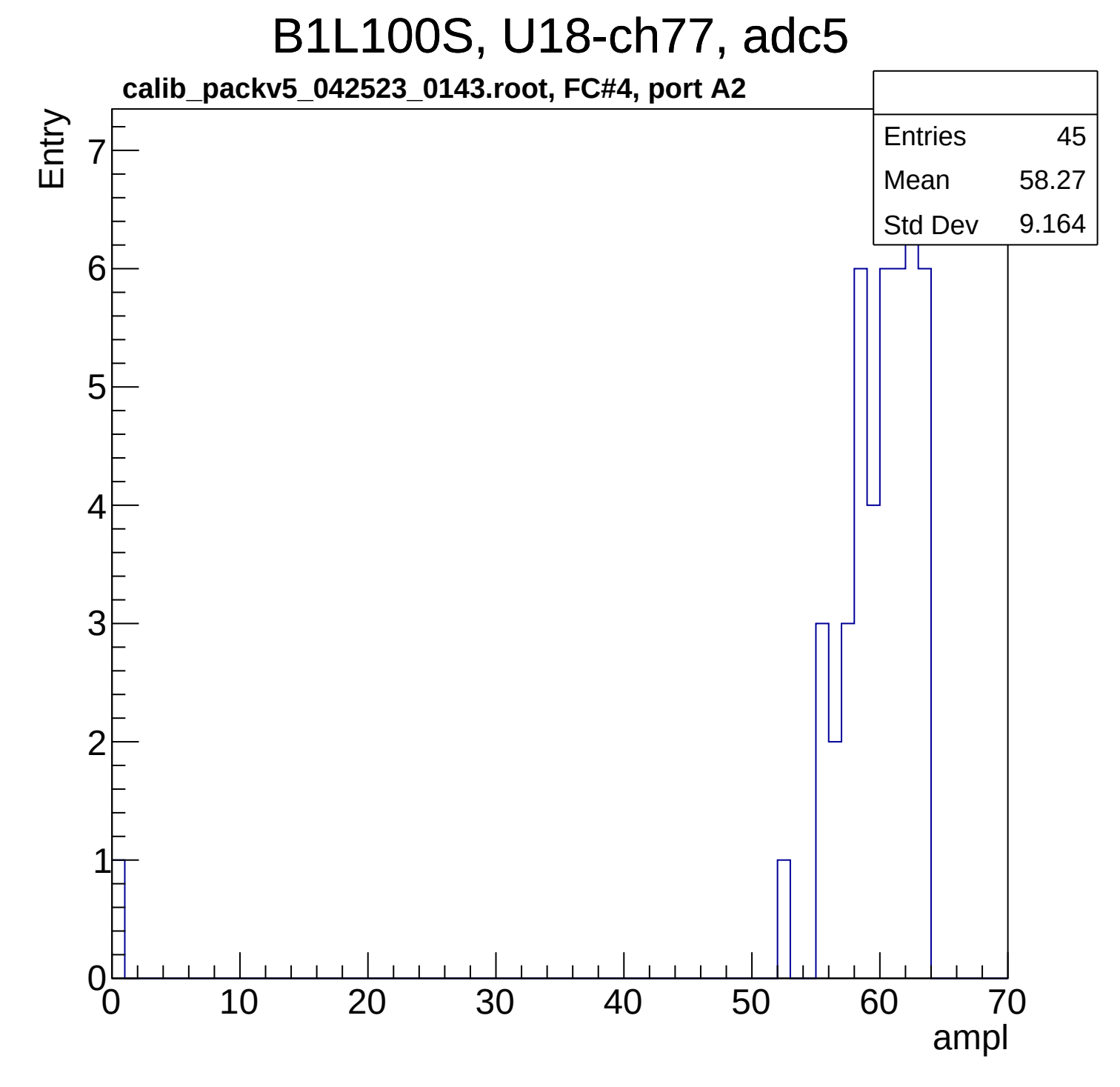

B1L100S, U18-ch77, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 30.95
Std Dev 3.466
Gaus mean : 30.9724
Gaus Width: 4.9843
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

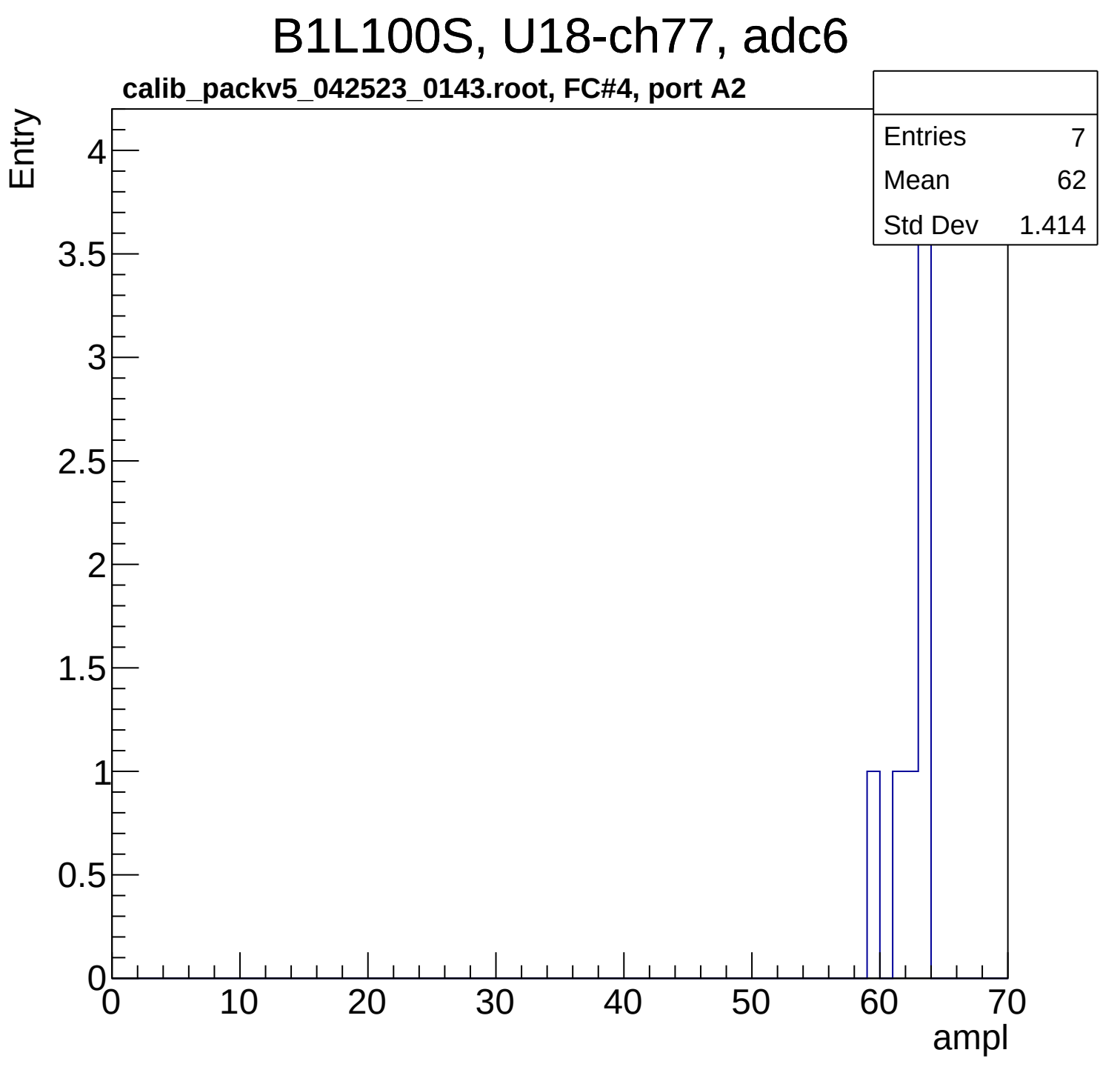

B1L100S, U18-ch77, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 36.24
Std Dev 3.633
Gaus mean : 36.3573
Gaus Width: 5.1001
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

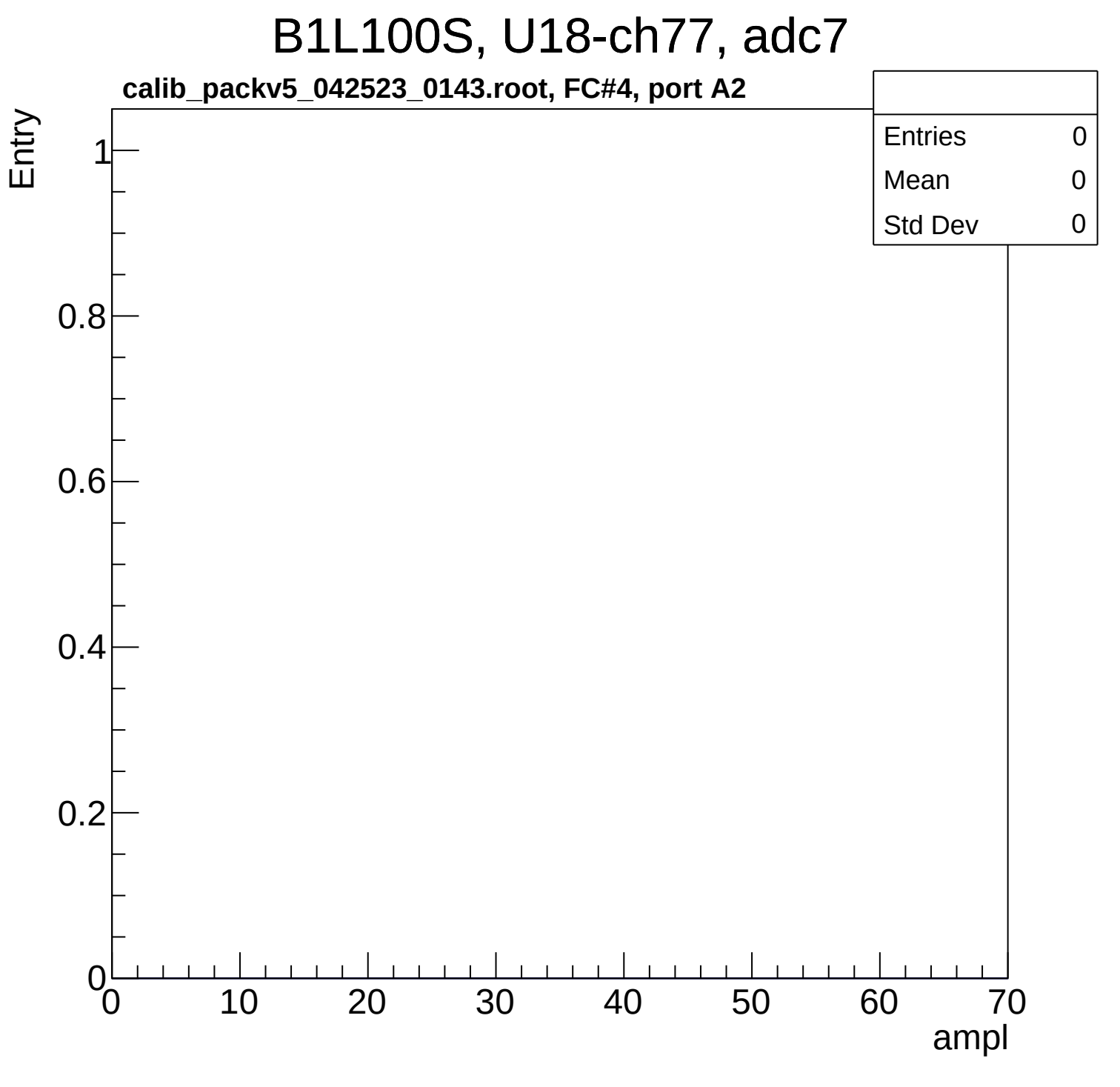

B1L100S, U18-ch77, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 42.64
Std Dev 3.506
Gaus mean : 43.4227
Gaus Width: 3.7869
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

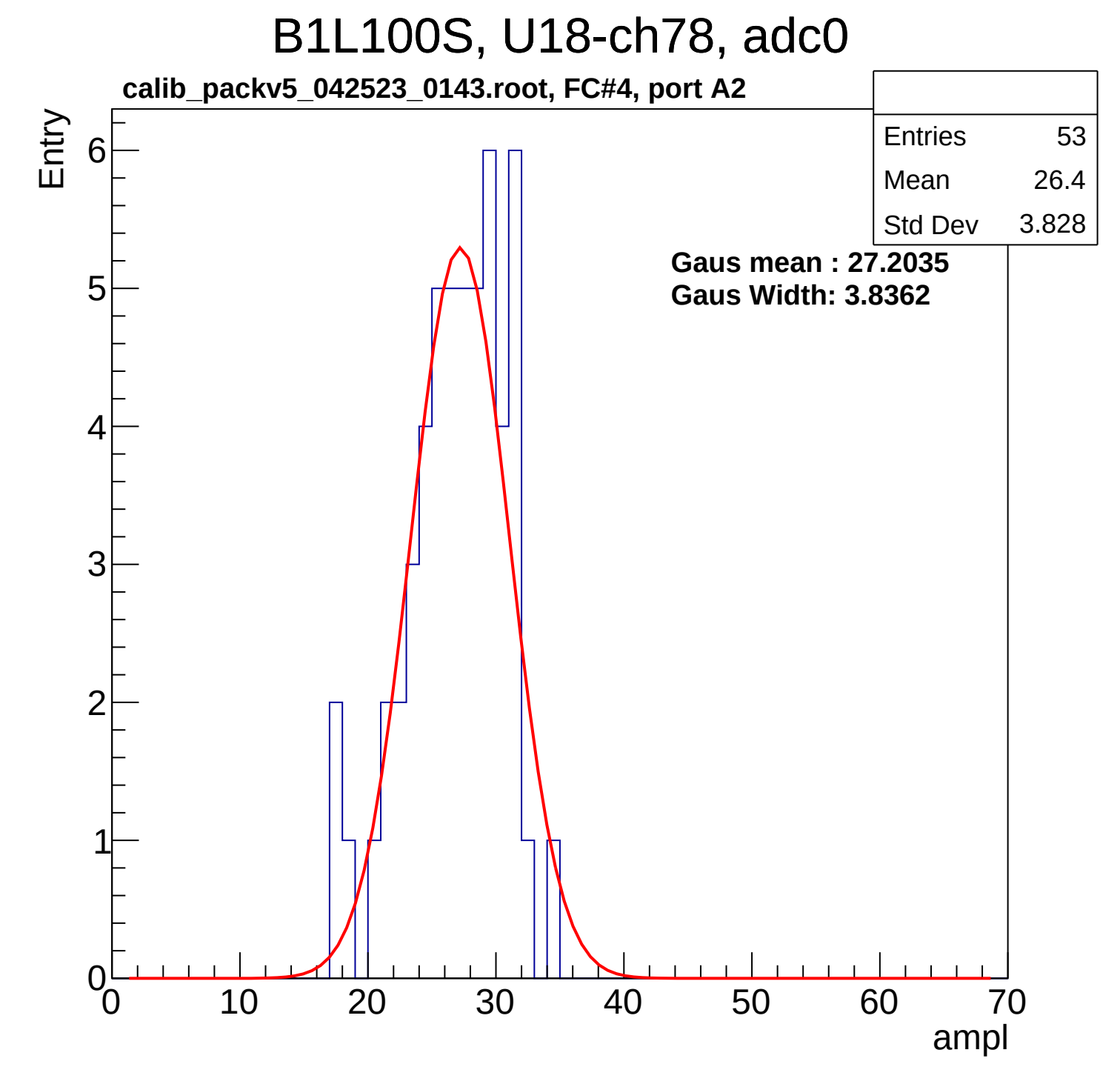

B1L100S, U18-ch77, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 49.58
Std Dev 3.804
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

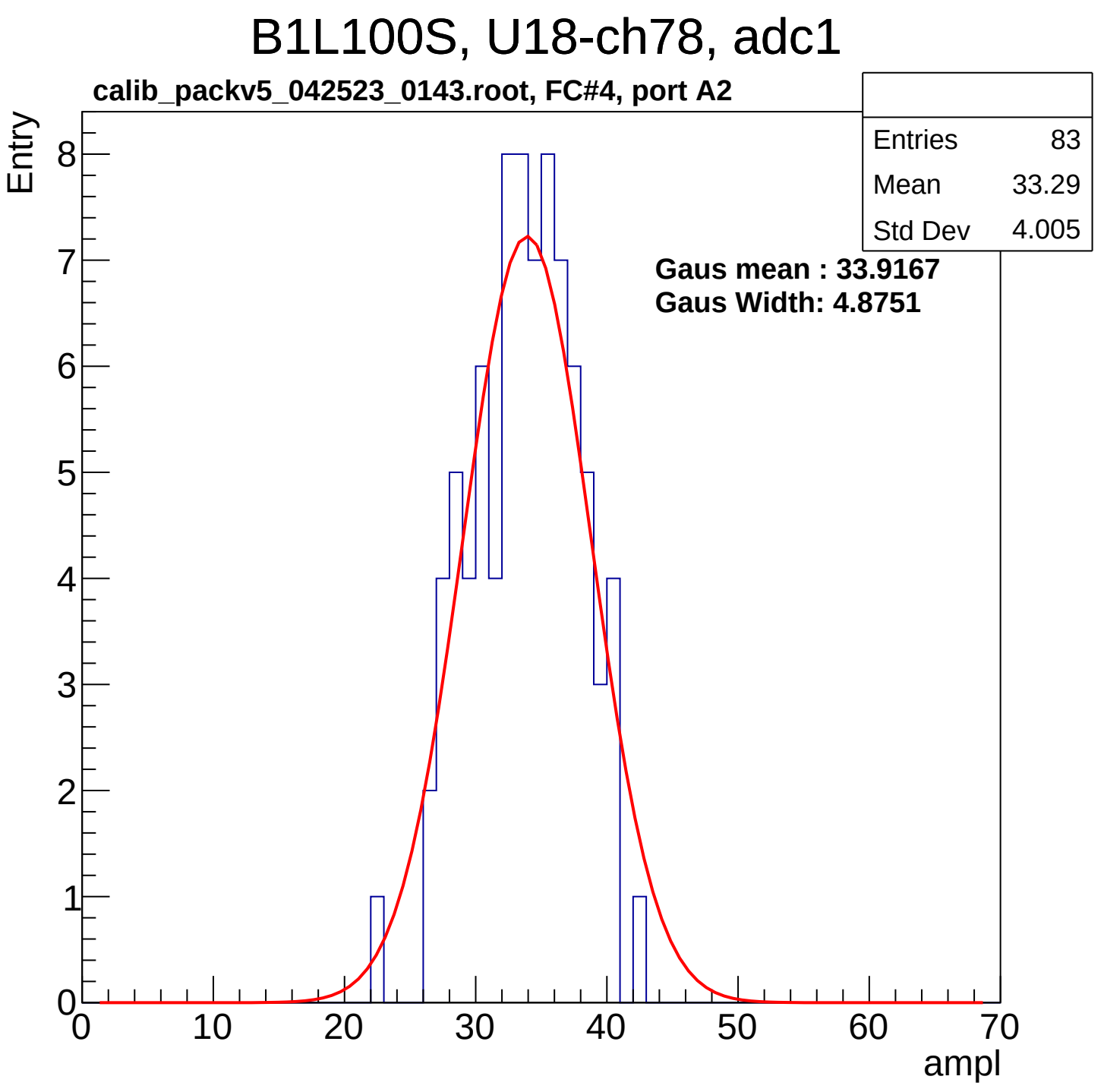

B1L100S, U18-ch77, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 55.44
Std Dev 3.817
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

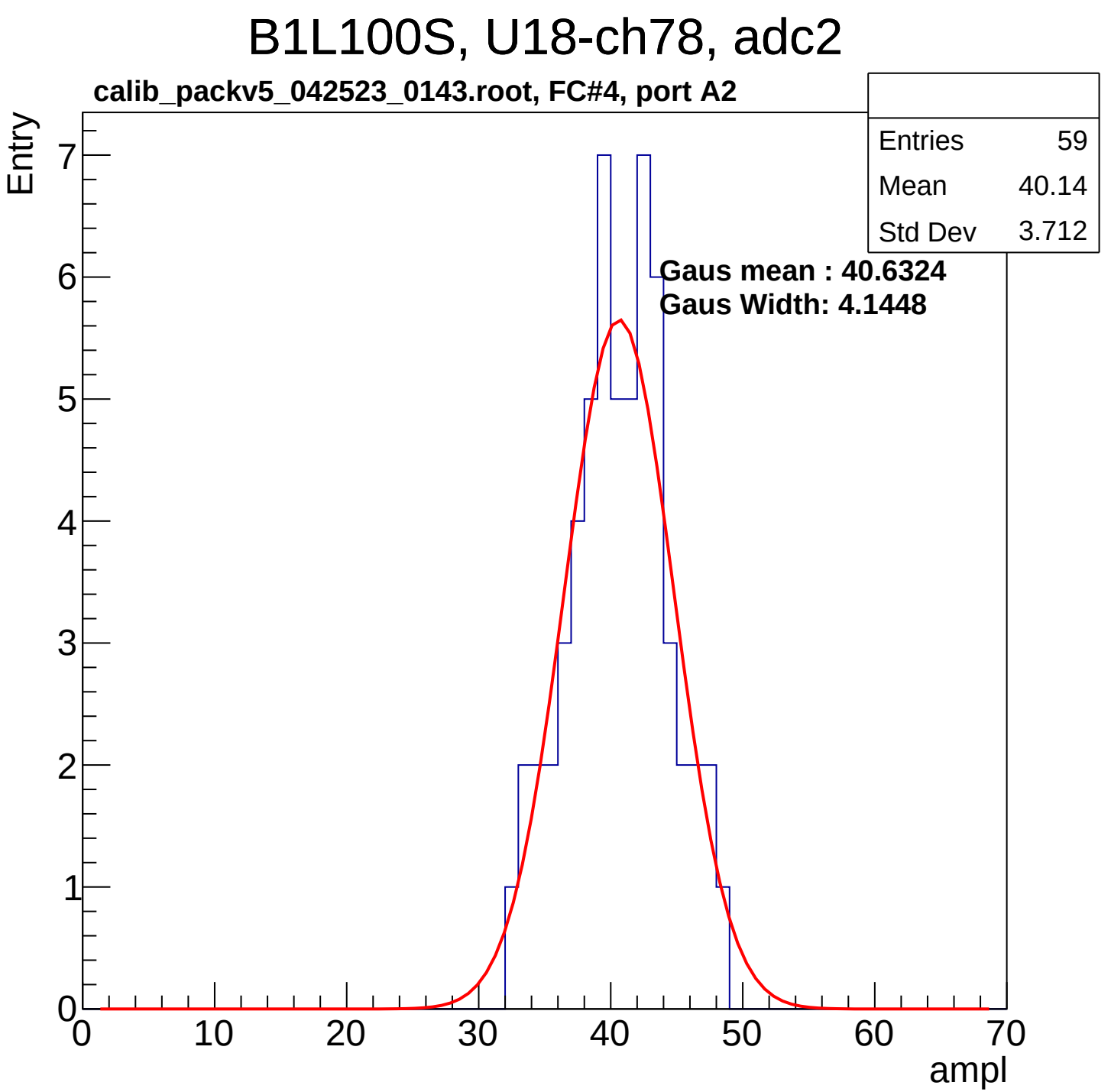

B1L100S, U18-ch77, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 45
Mean 58.27
Std Dev 9.164
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

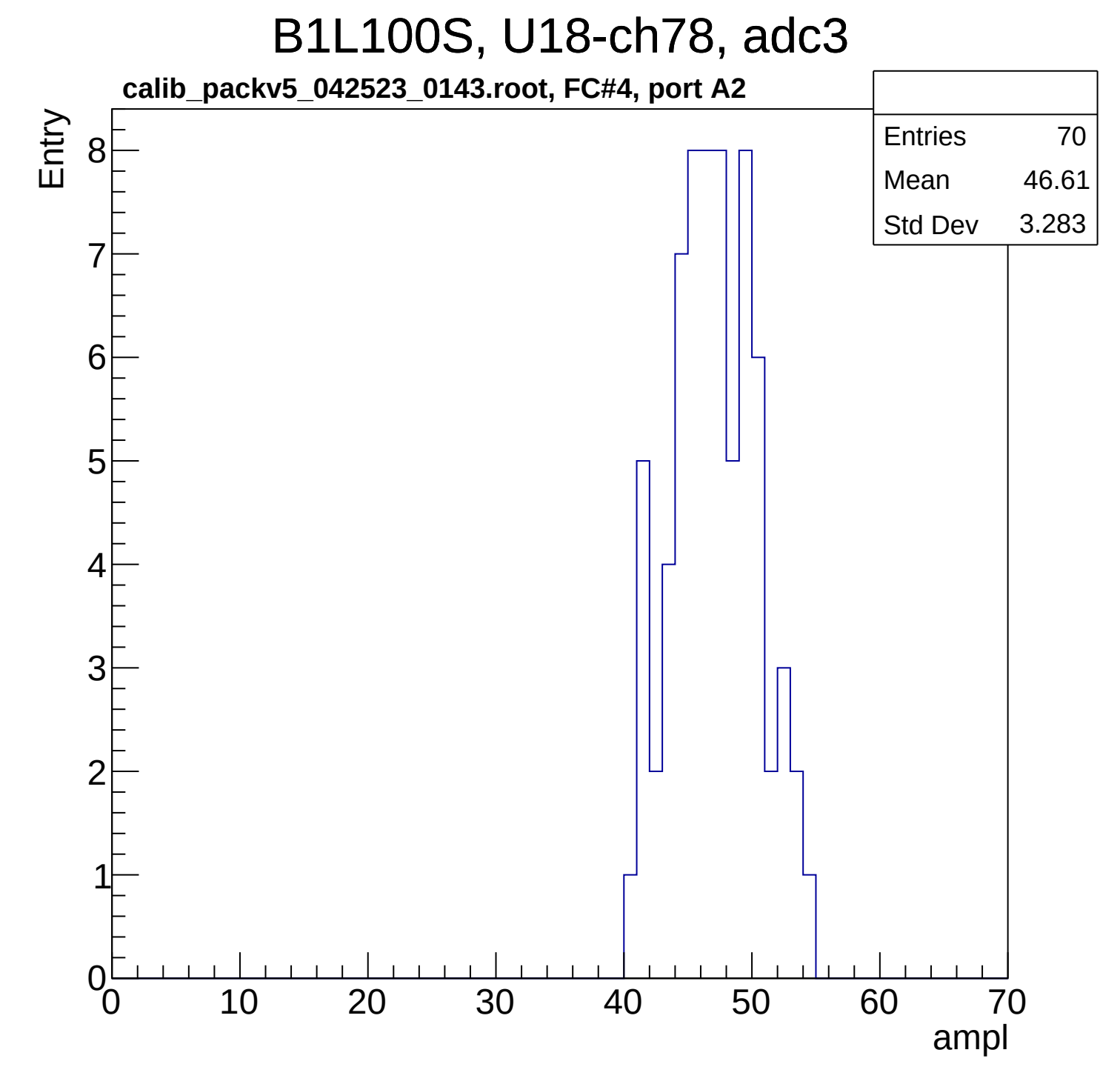

B1L100S, U18-ch77, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 62
Std Dev 1.414
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

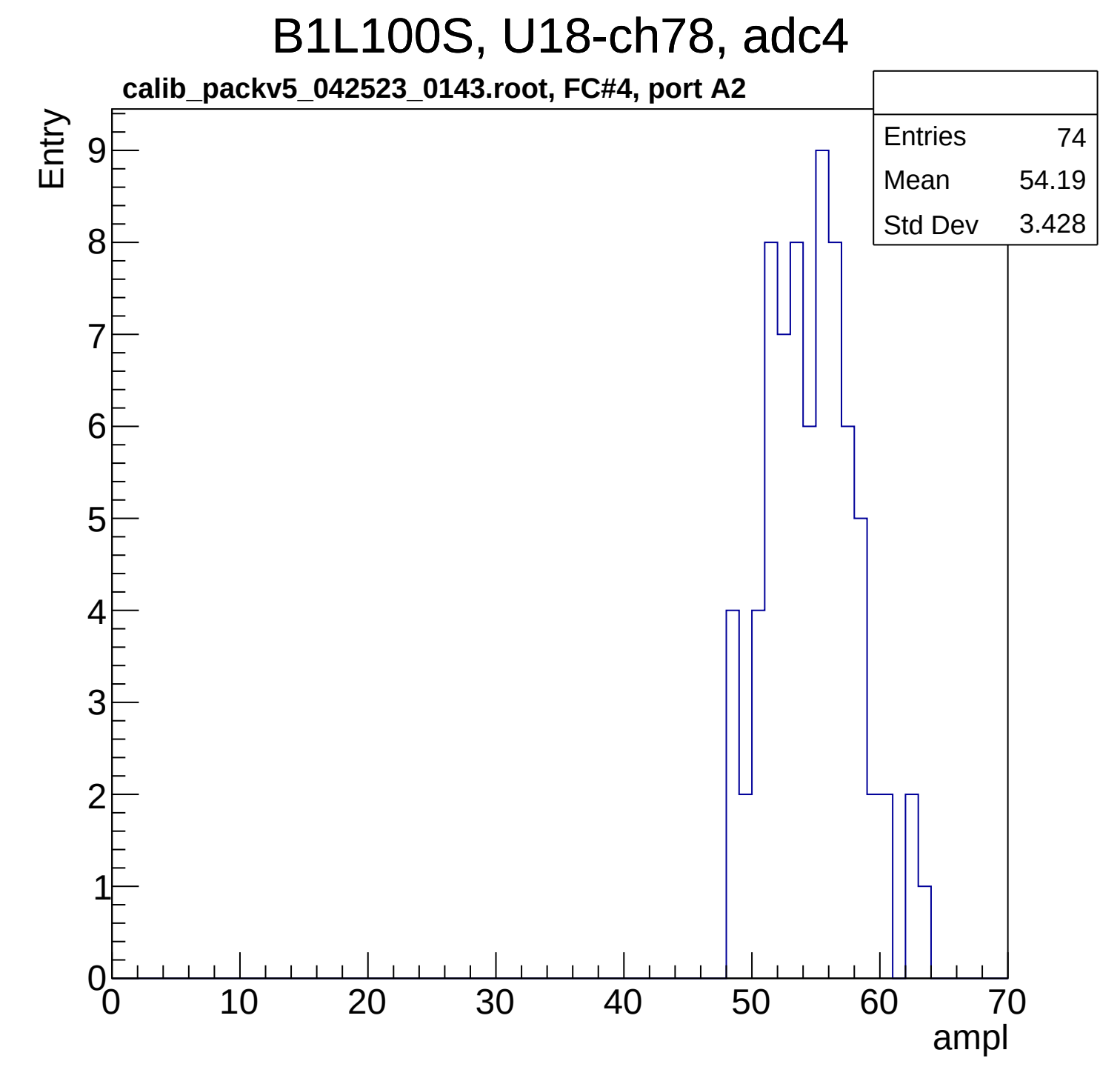

B1L100S, U18-ch77, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

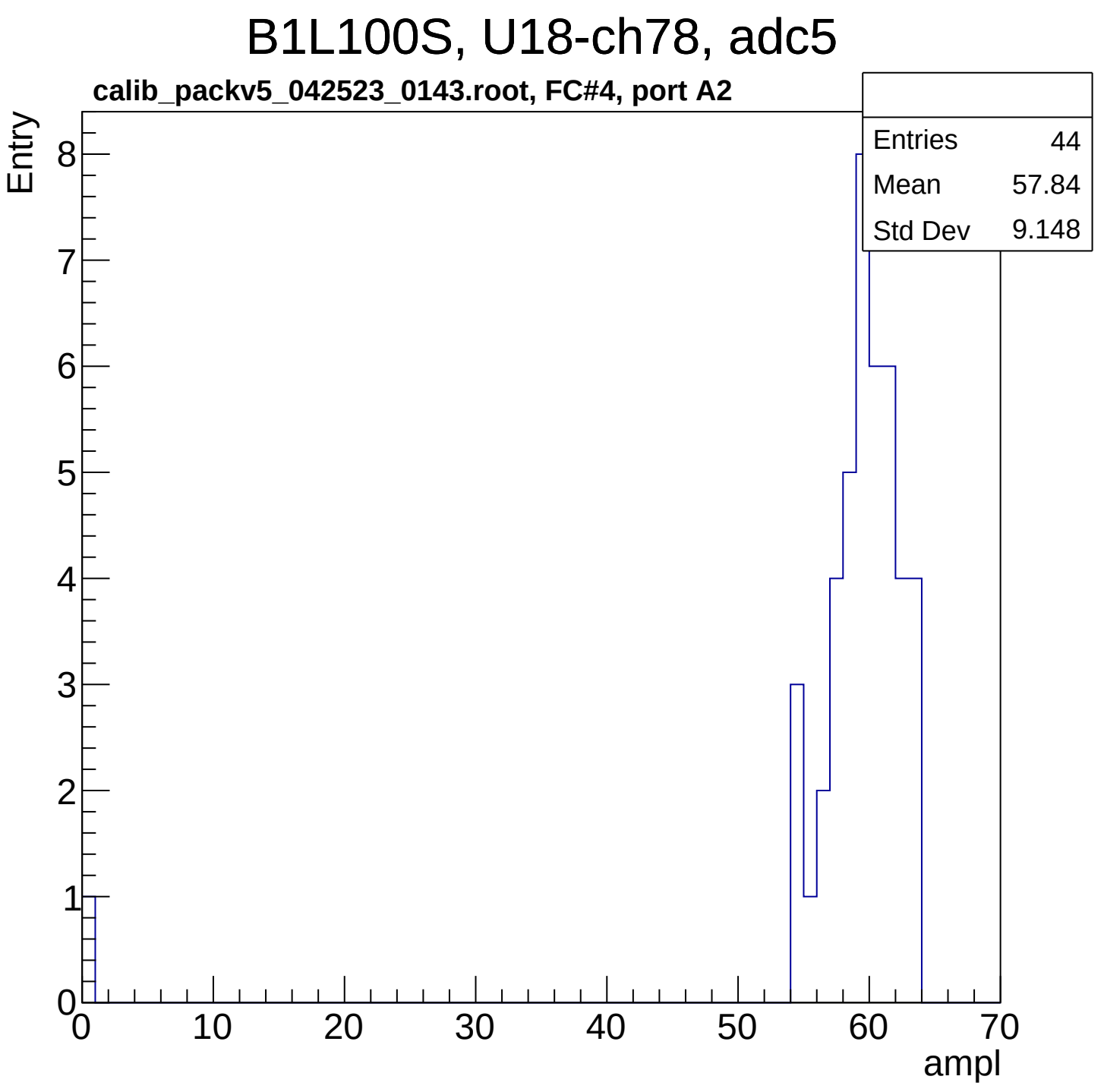

B1L100S, U18-ch78, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 26.4
Std Dev 3.828
Gaus mean : 27.2035
Gaus Width: 3.8362
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

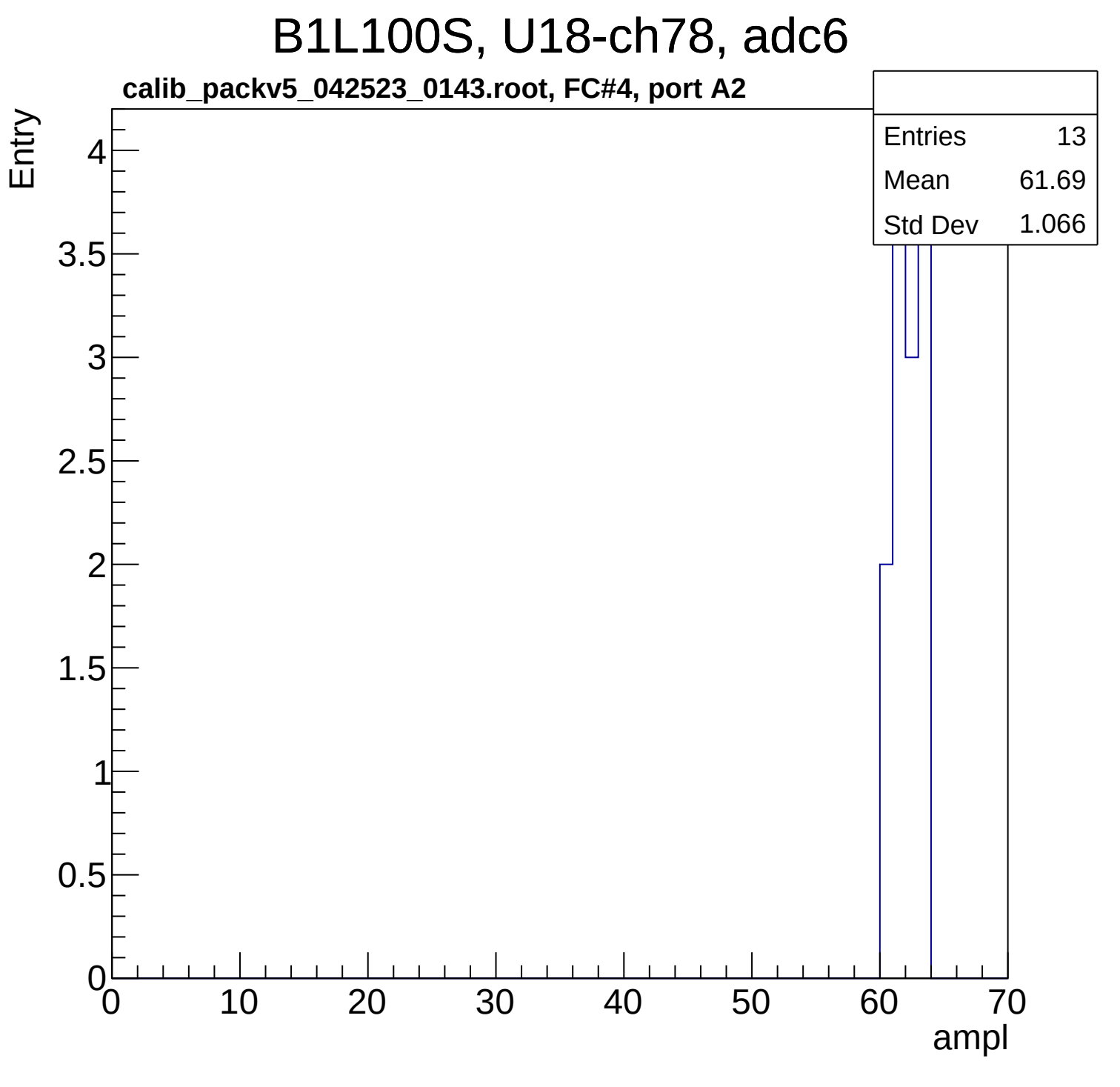

B1L100S, U18-ch78, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 83
Mean 33.29
Std Dev 4.005
Gaus mean : 33.9167
Gaus Width: 4.8751
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

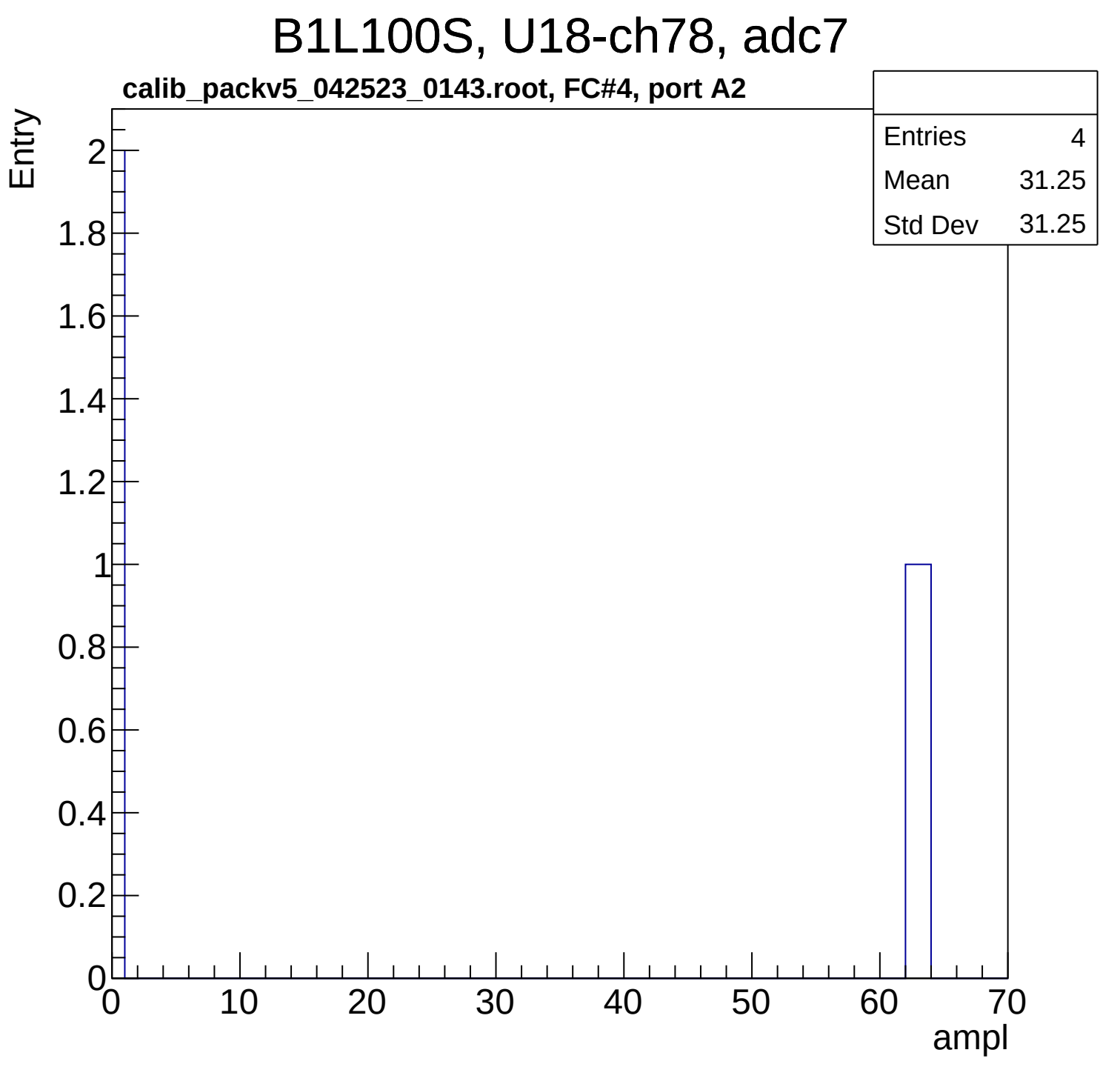

B1L100S, U18-ch78, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 40.14
Std Dev 3.712
Gaus mean : 40.6324
Gaus Width: 4.1448
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

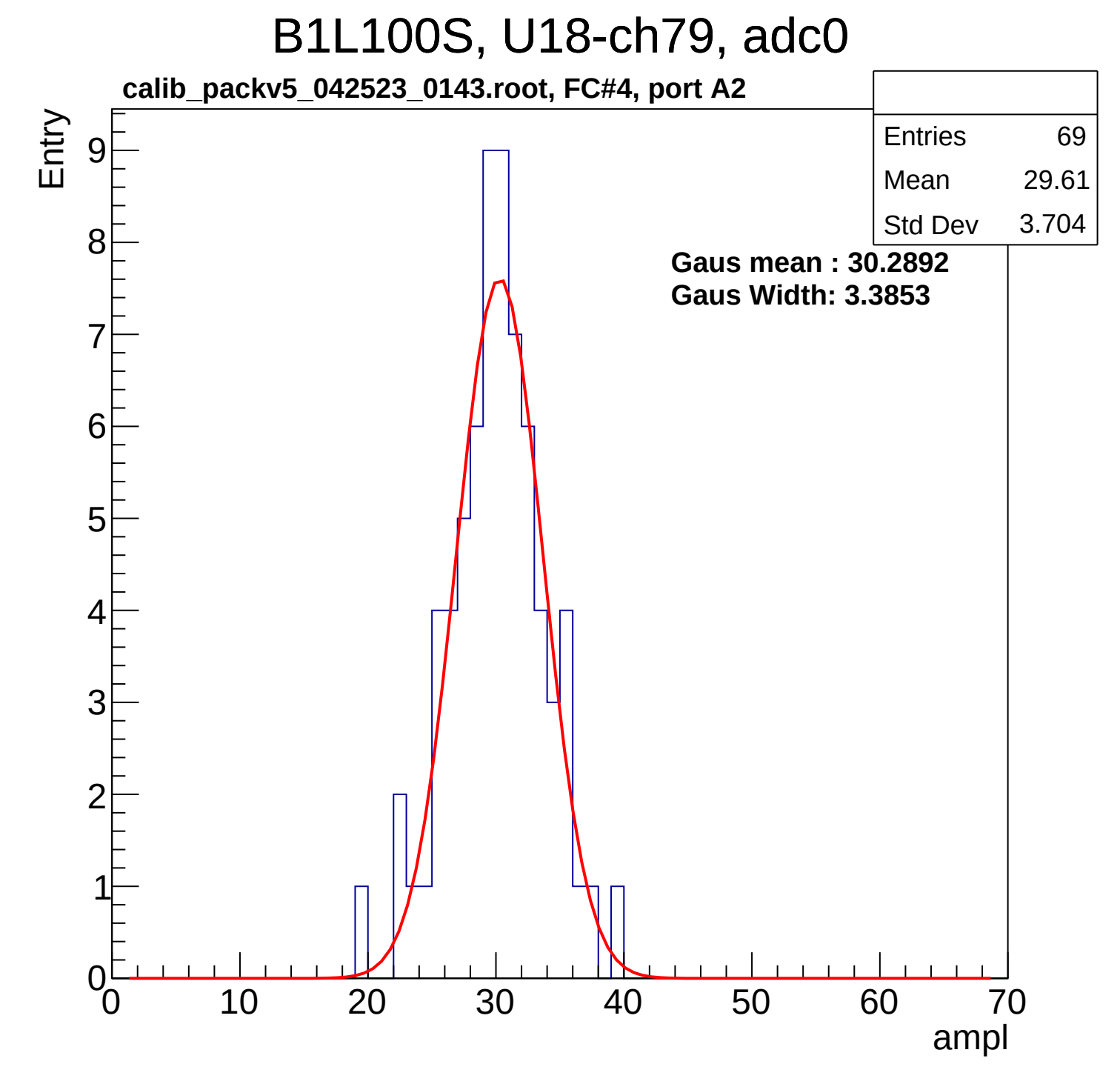

B1L100S, U18-ch78, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 46.61
Std Dev 3.283
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

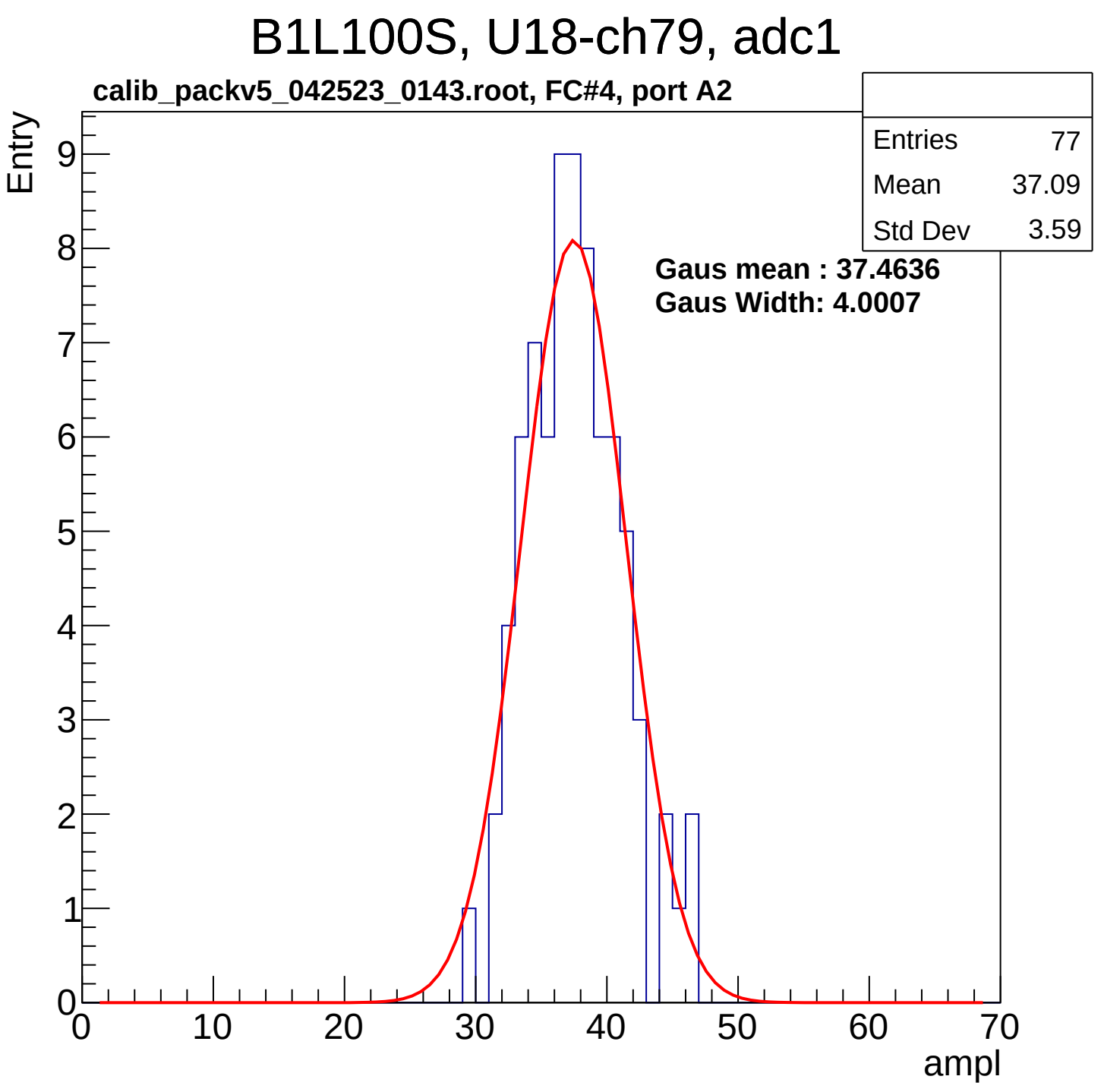

B1L100S, U18-ch78, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 54.19
Std Dev 3.428
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

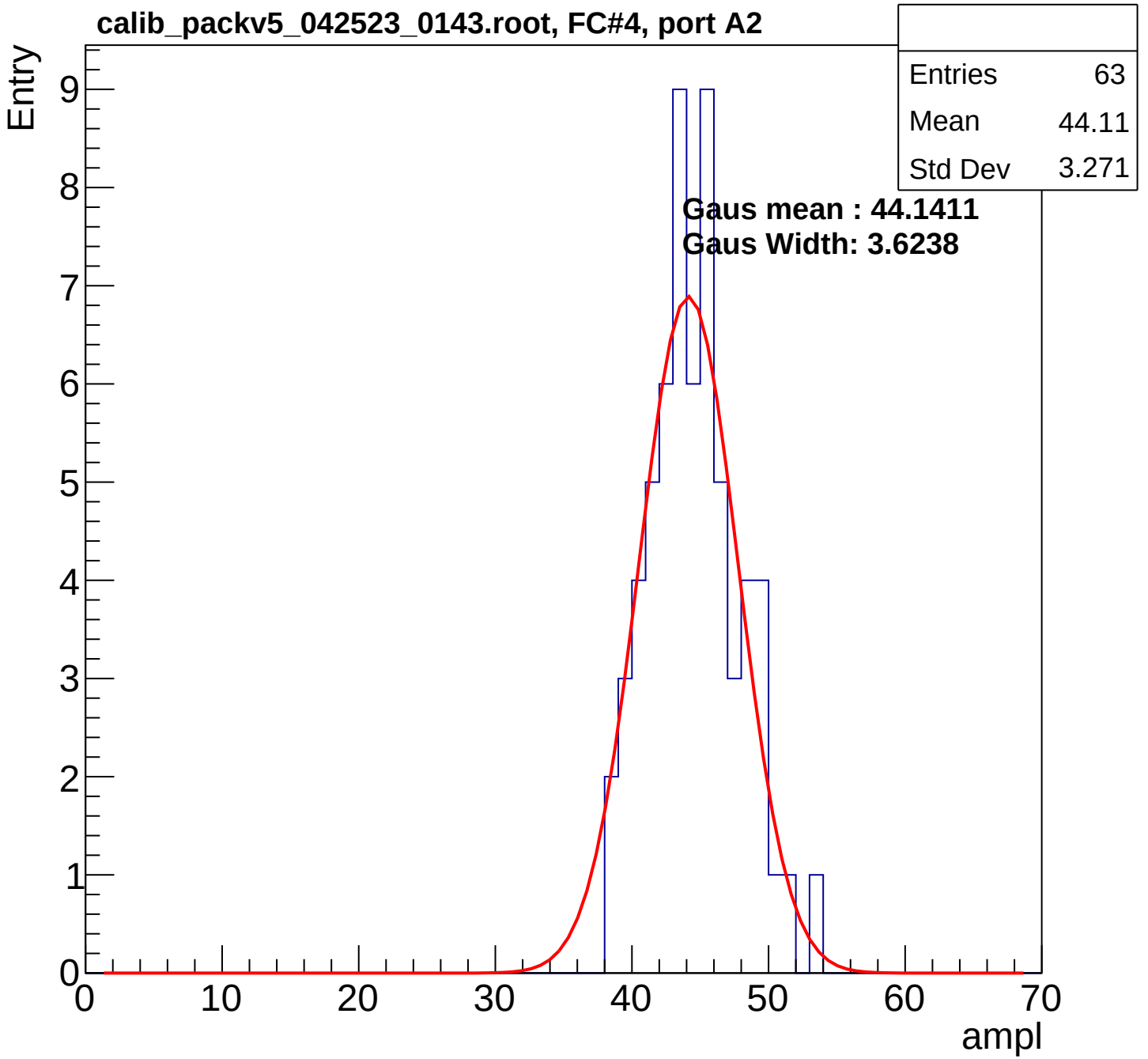

B1L100S, U18-ch78, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 44
Mean 57.84
Std Dev 9.148
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

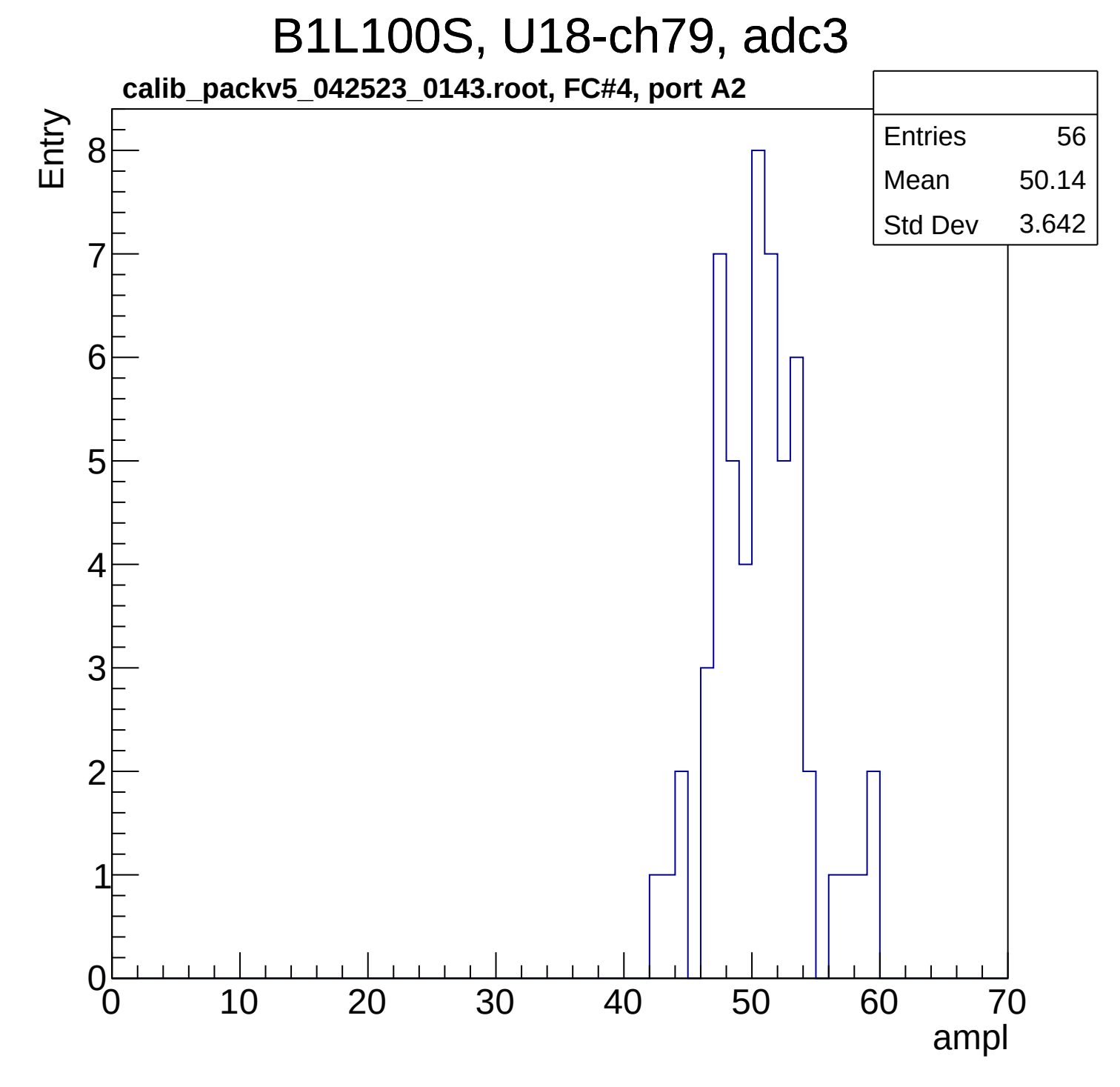

B1L100S, U18-ch78, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 13
Mean 61.69
Std Dev 1.066
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

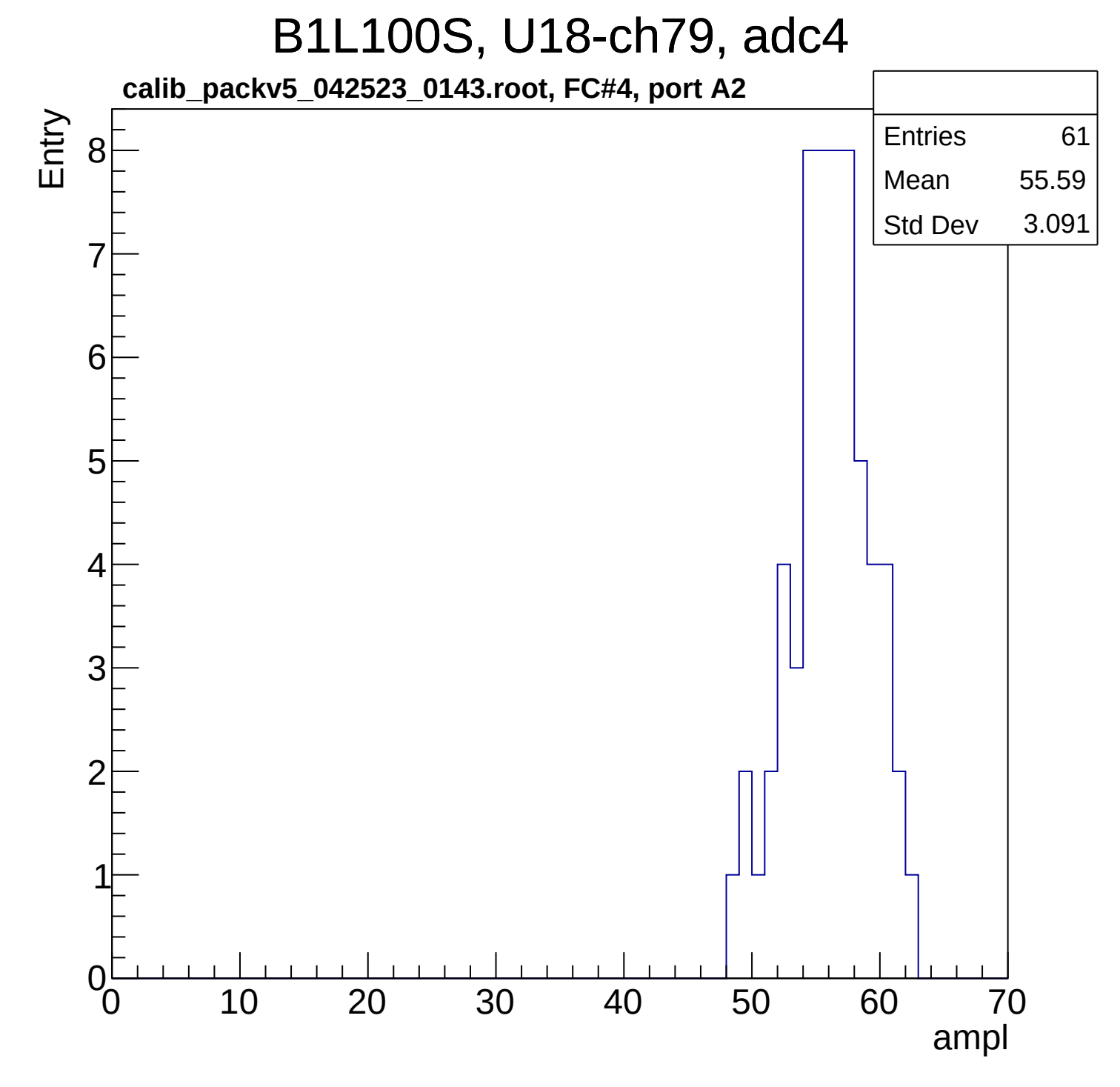

B1L100S, U18-ch78, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 4
Mean 31.25
Std Dev 31.25
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

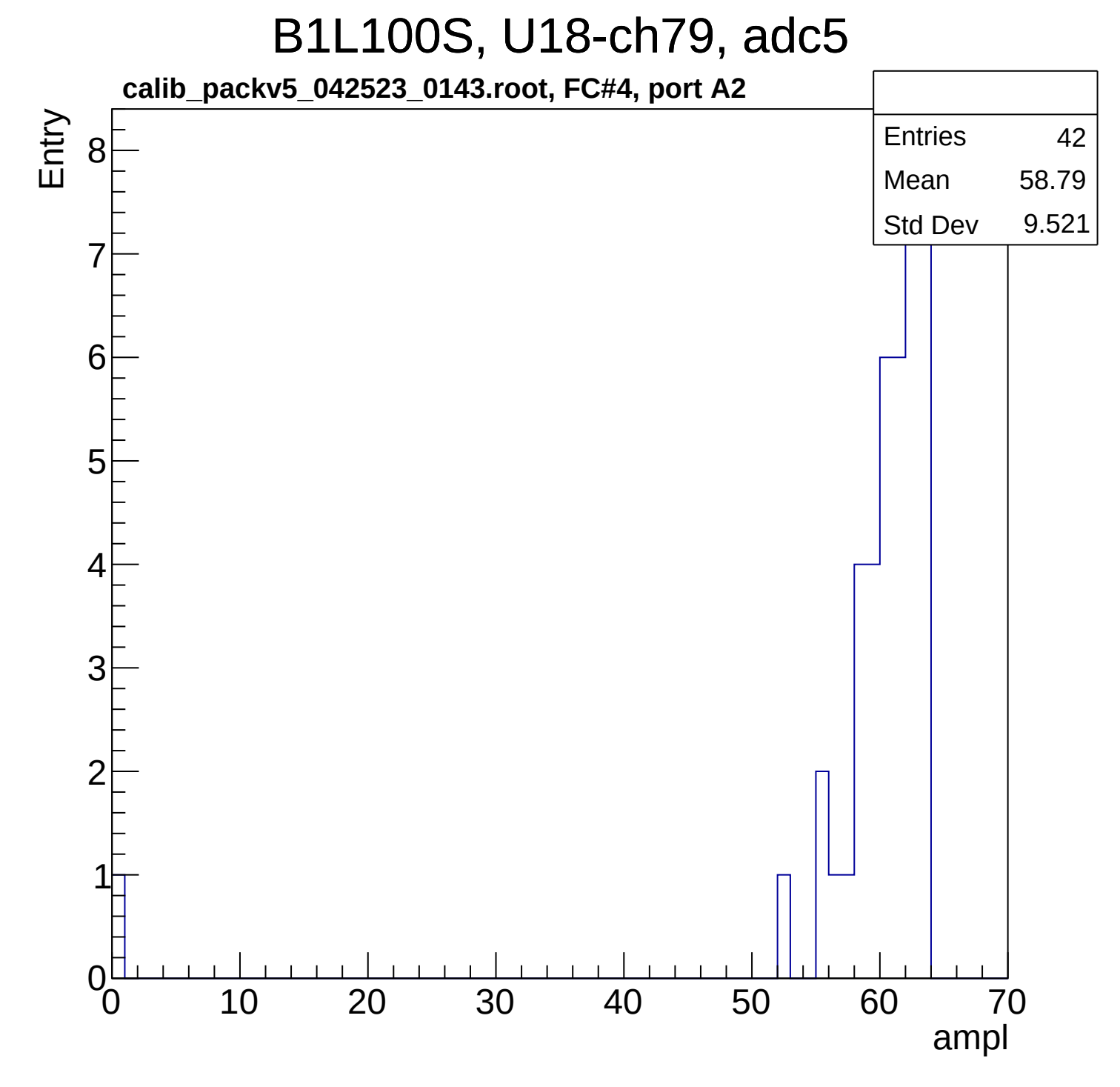

B1L100S, U18-ch79, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 29.61
Std Dev 3.704
Gaus mean : 30.2892
Gaus Width: 3.3853
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

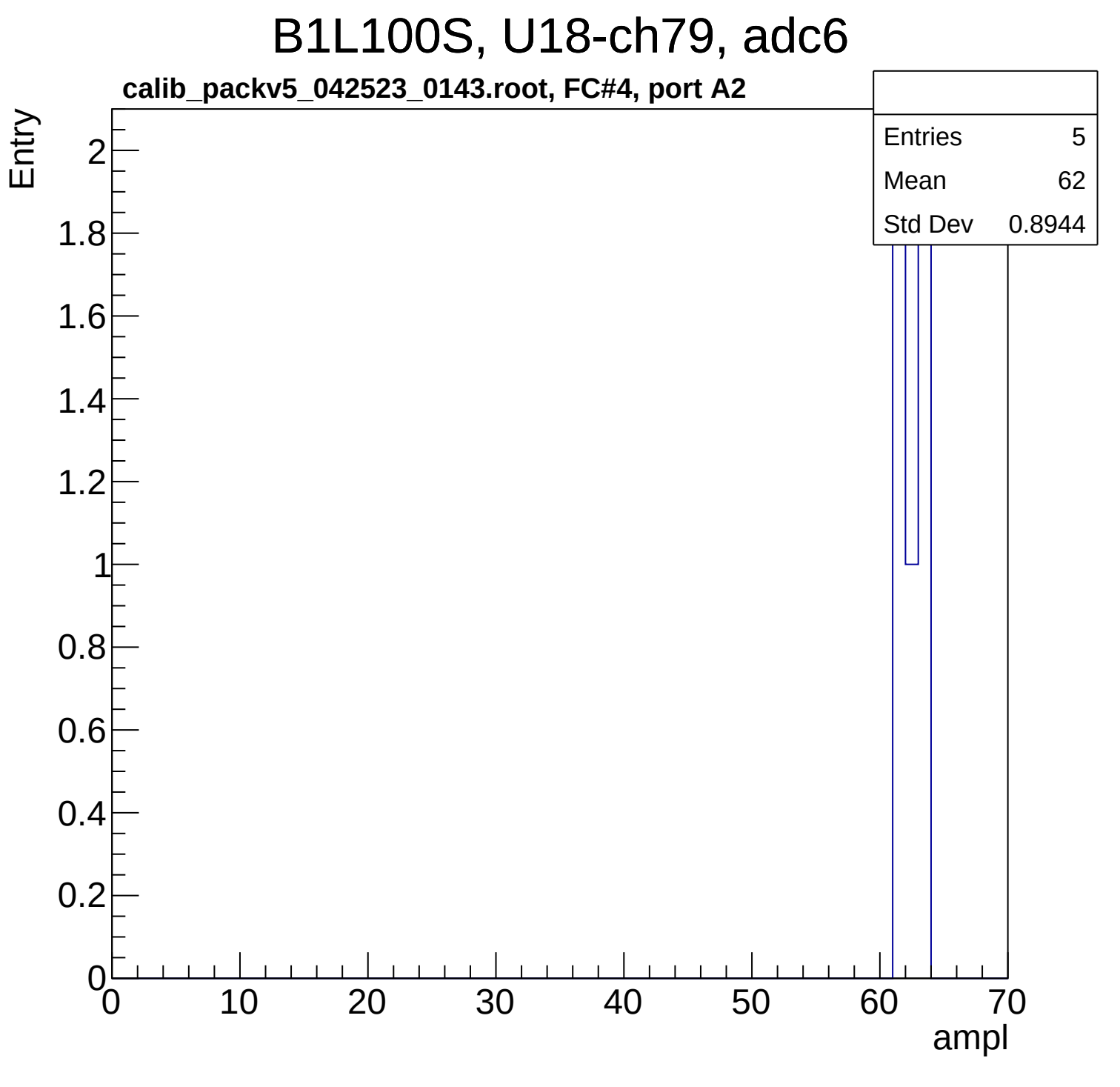

B1L100S, U18-ch79, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 37.09
Std Dev 3.59
Gaus mean : 37.4636
Gaus Width: 4.0007
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

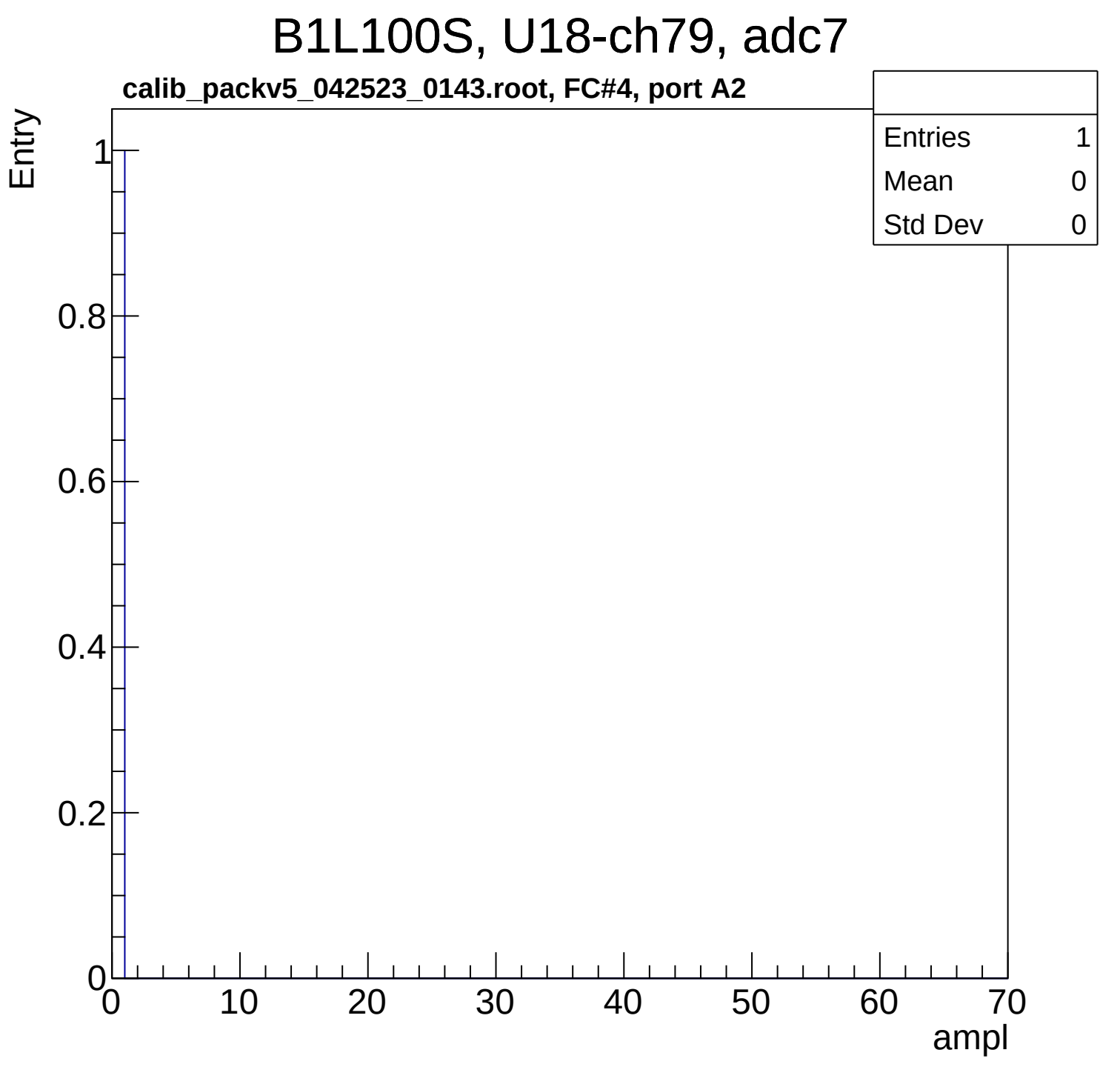

B1L100S, U18-ch79, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 44.11
Std Dev 3.271
Gaus mean : 44.1411
Gaus Width: 3.6238
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

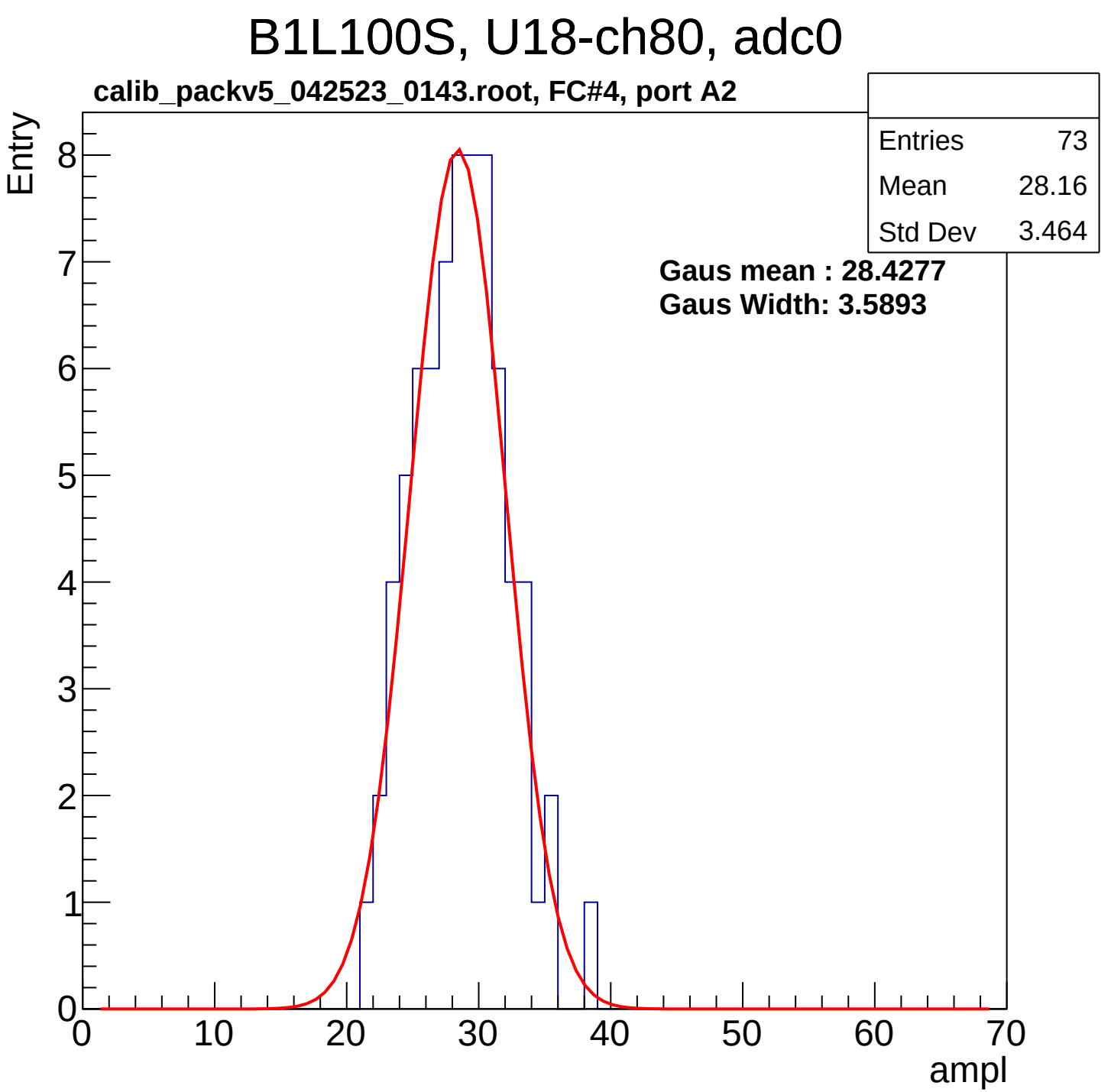

B1L100S, U18-ch79, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 50.14
Std Dev 3.642
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

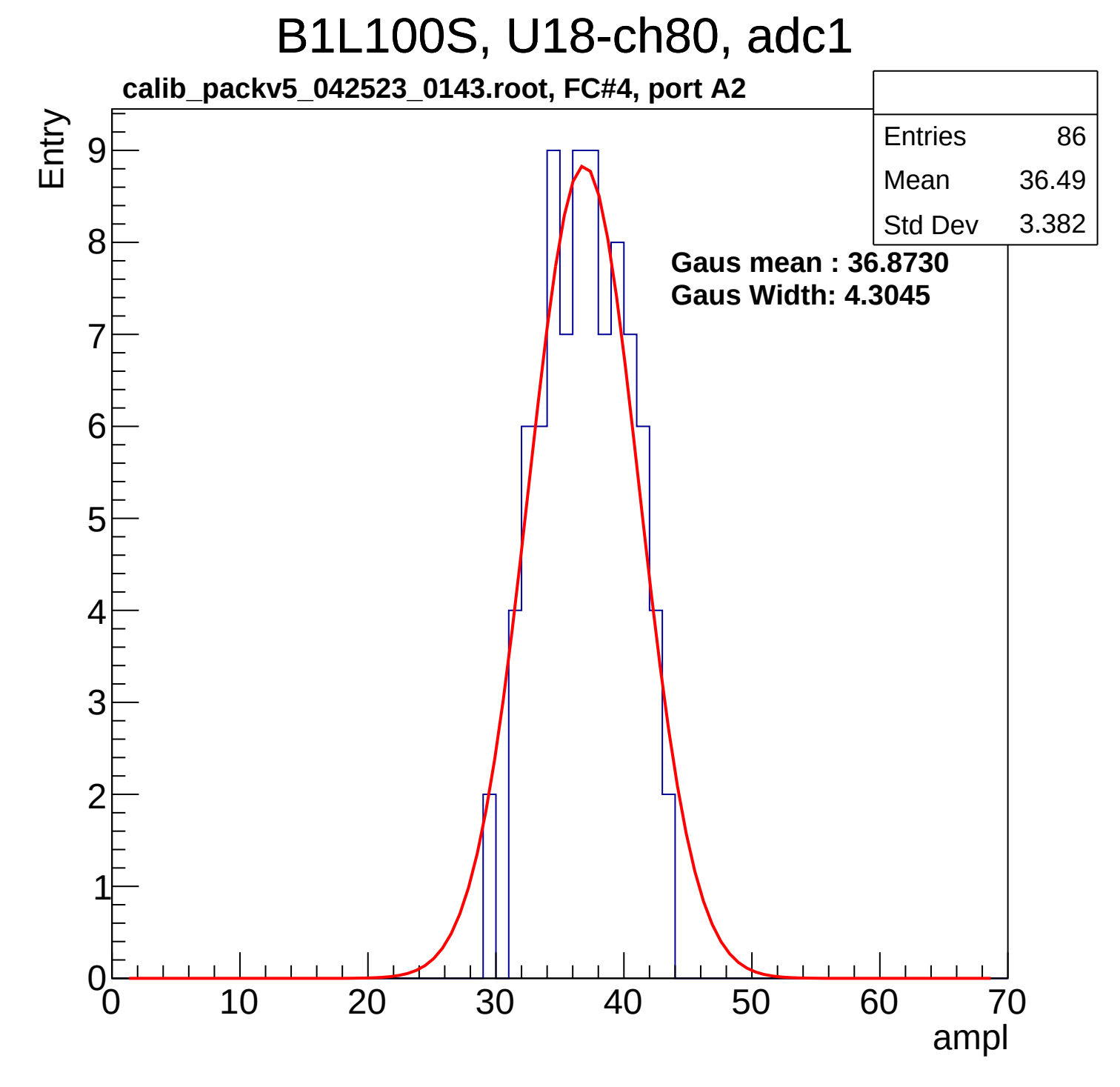

B1L100S, U18-ch79, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 55.59
Std Dev 3.091
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

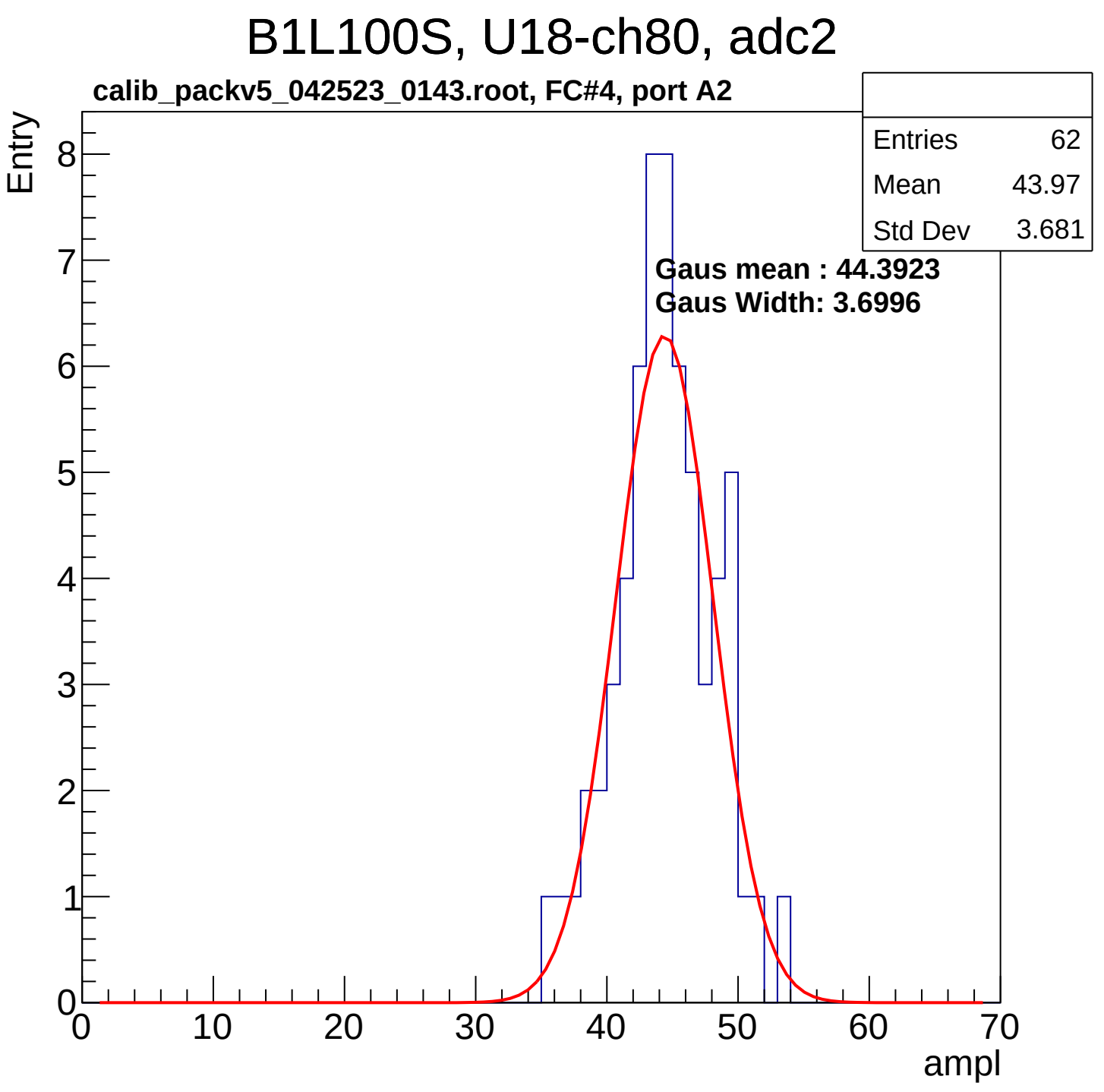

B1L100S, U18-ch79, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 42
Mean 58.79
Std Dev 9.521
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

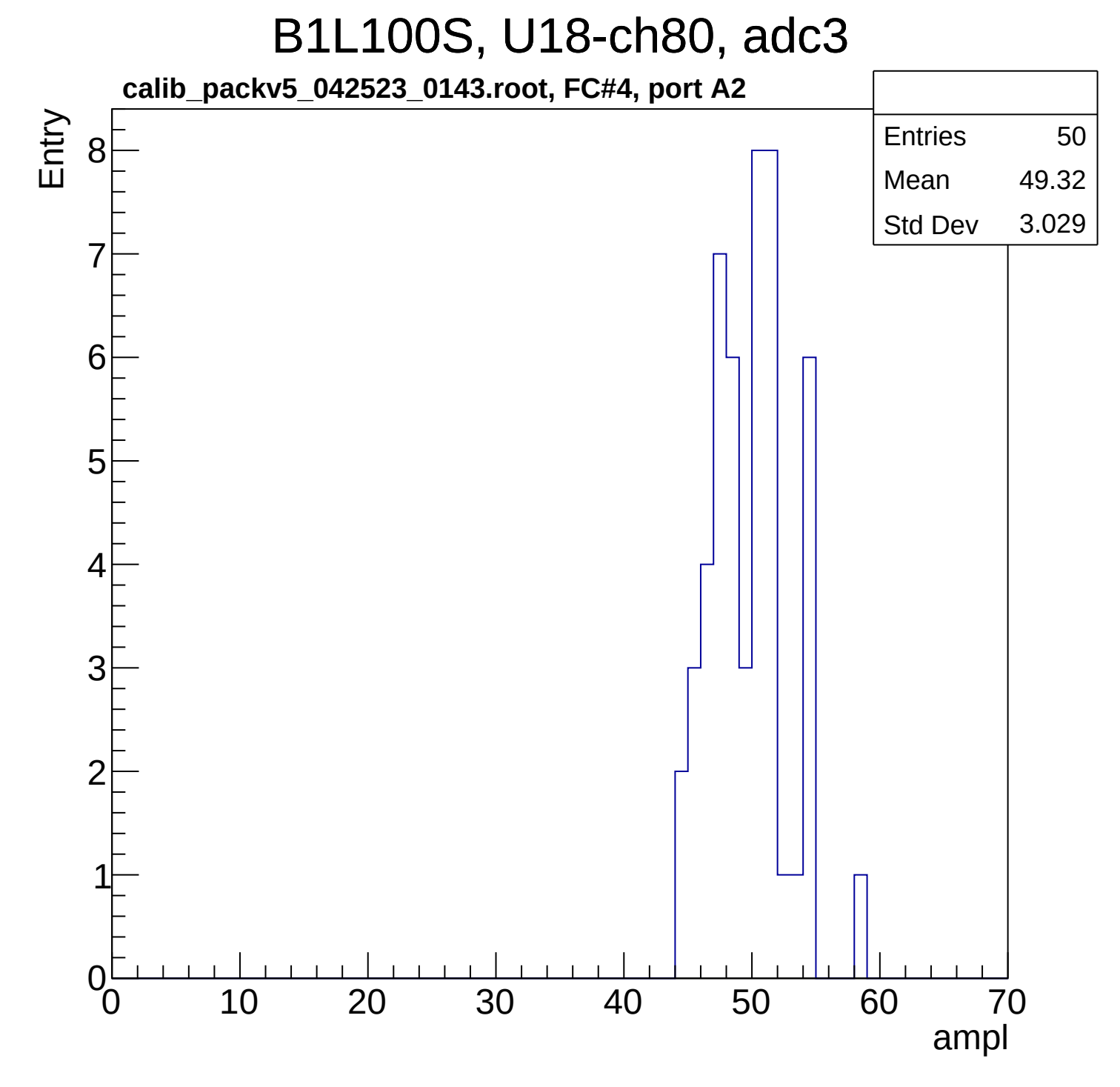

B1L100S, U18-ch79, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 5
Mean 62
Std Dev 0.8944
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

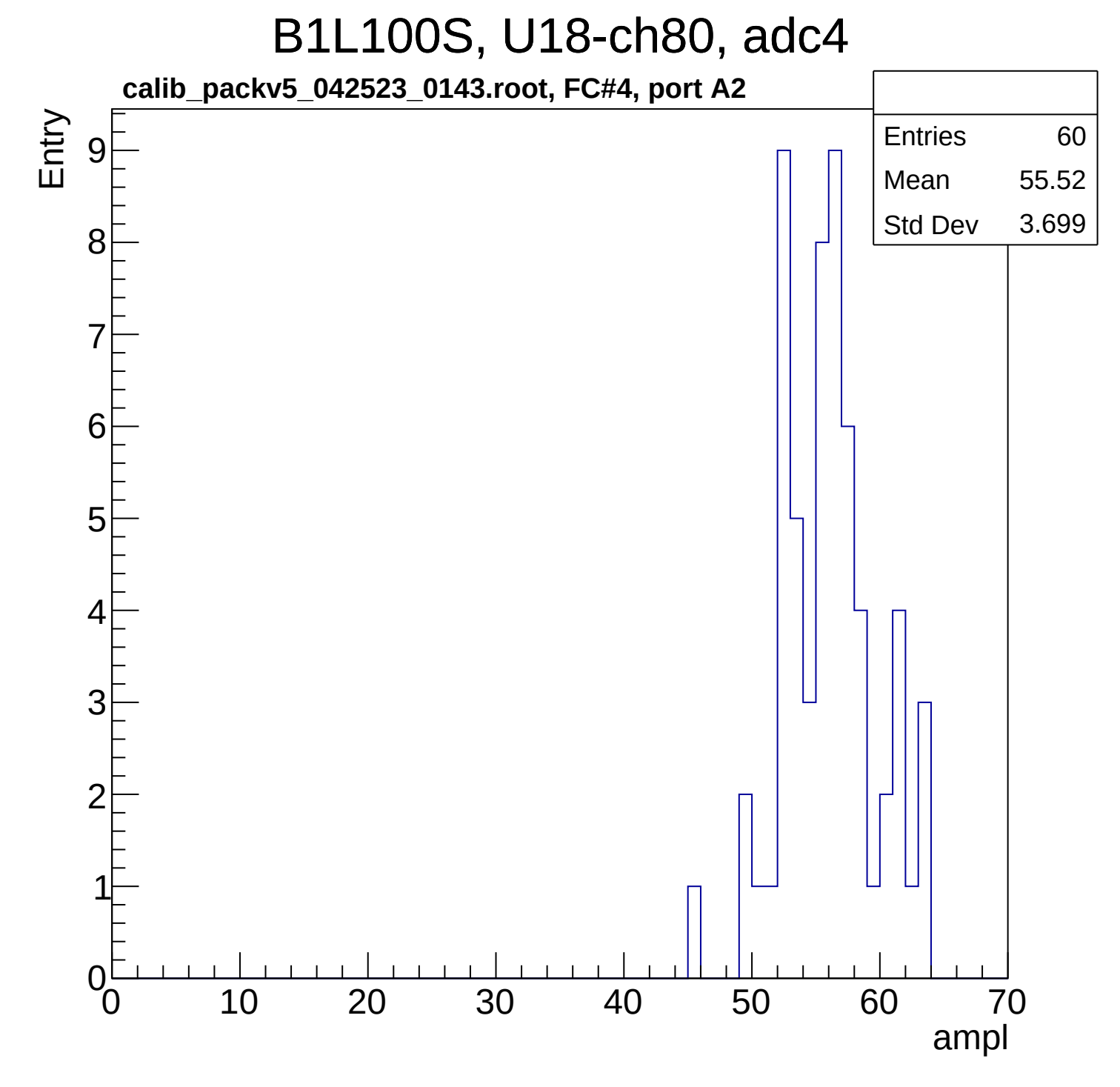

B1L100S, U18-ch79, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

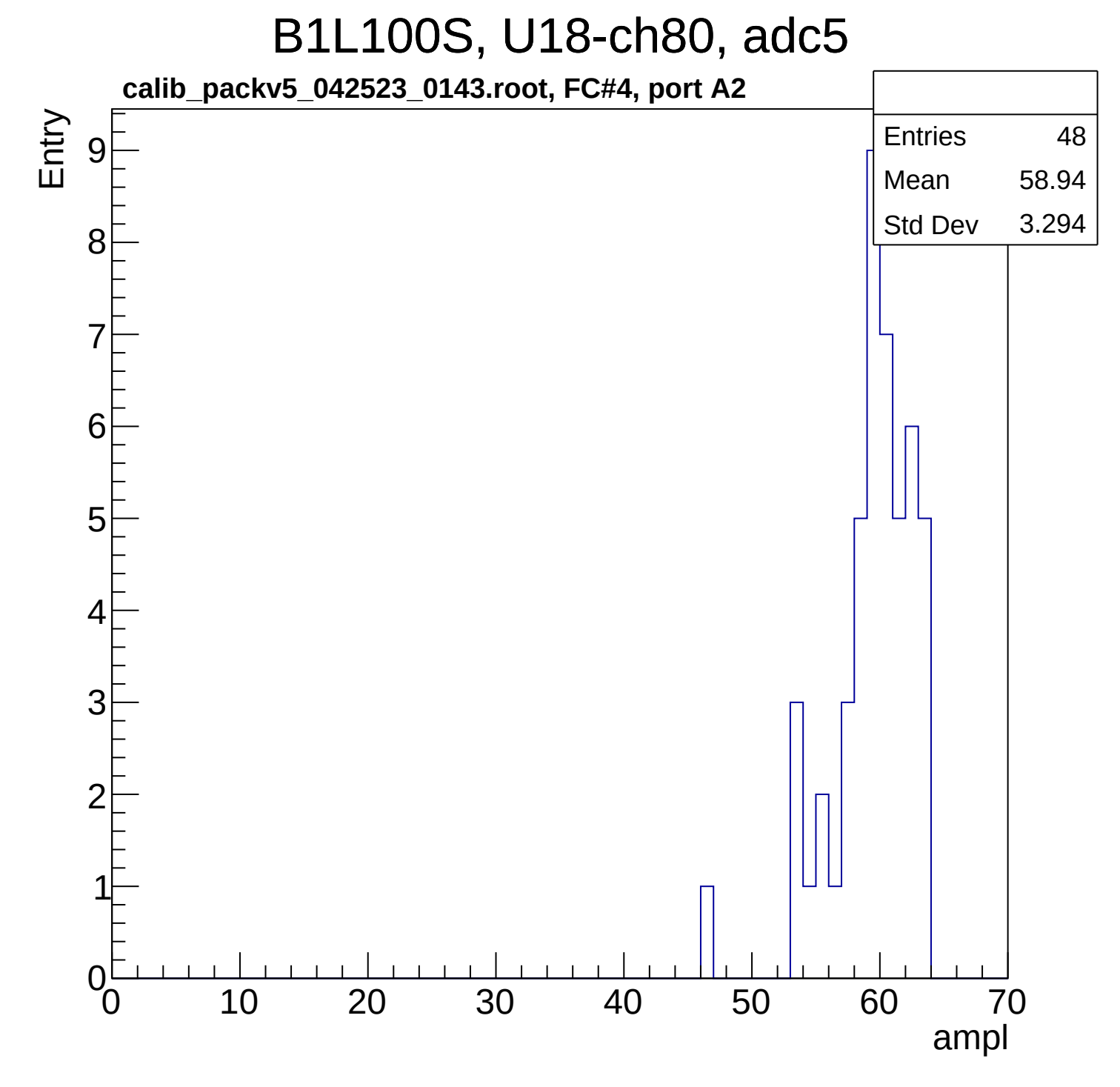

B1L100S, U18-ch80, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 28.16
Std Dev 3.464
Gaus mean : 28.4277
Gaus Width: 3.5893
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

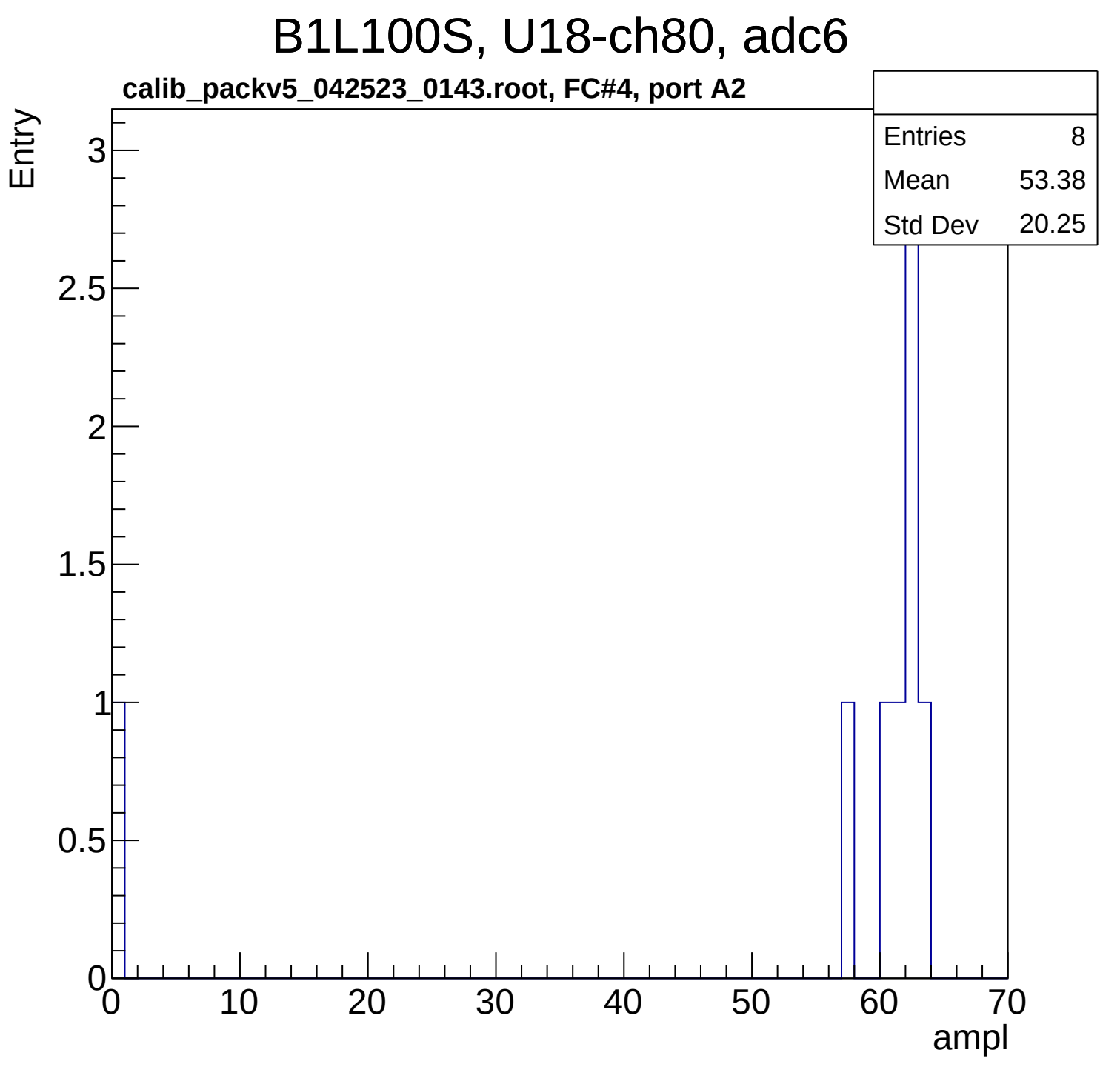

B1L100S, U18-ch80, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 86
Mean 36.49
Std Dev 3.382
Gaus mean : 36.8730
Gaus Width: 4.3045
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

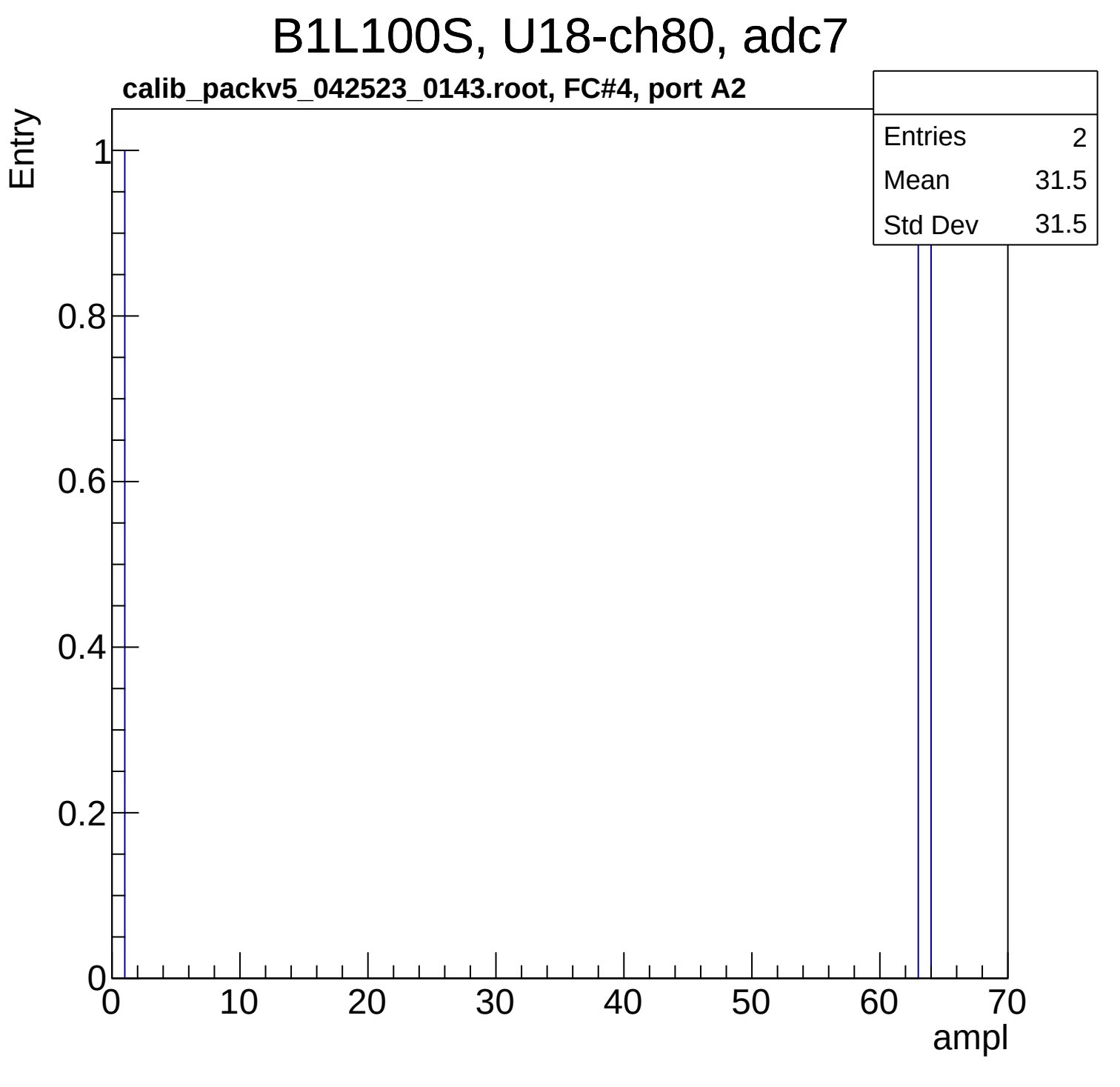

B1L100S, U18-ch80, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 43.97
Std Dev 3.681
Gaus mean : 44.3923
Gaus Width: 3.6996
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

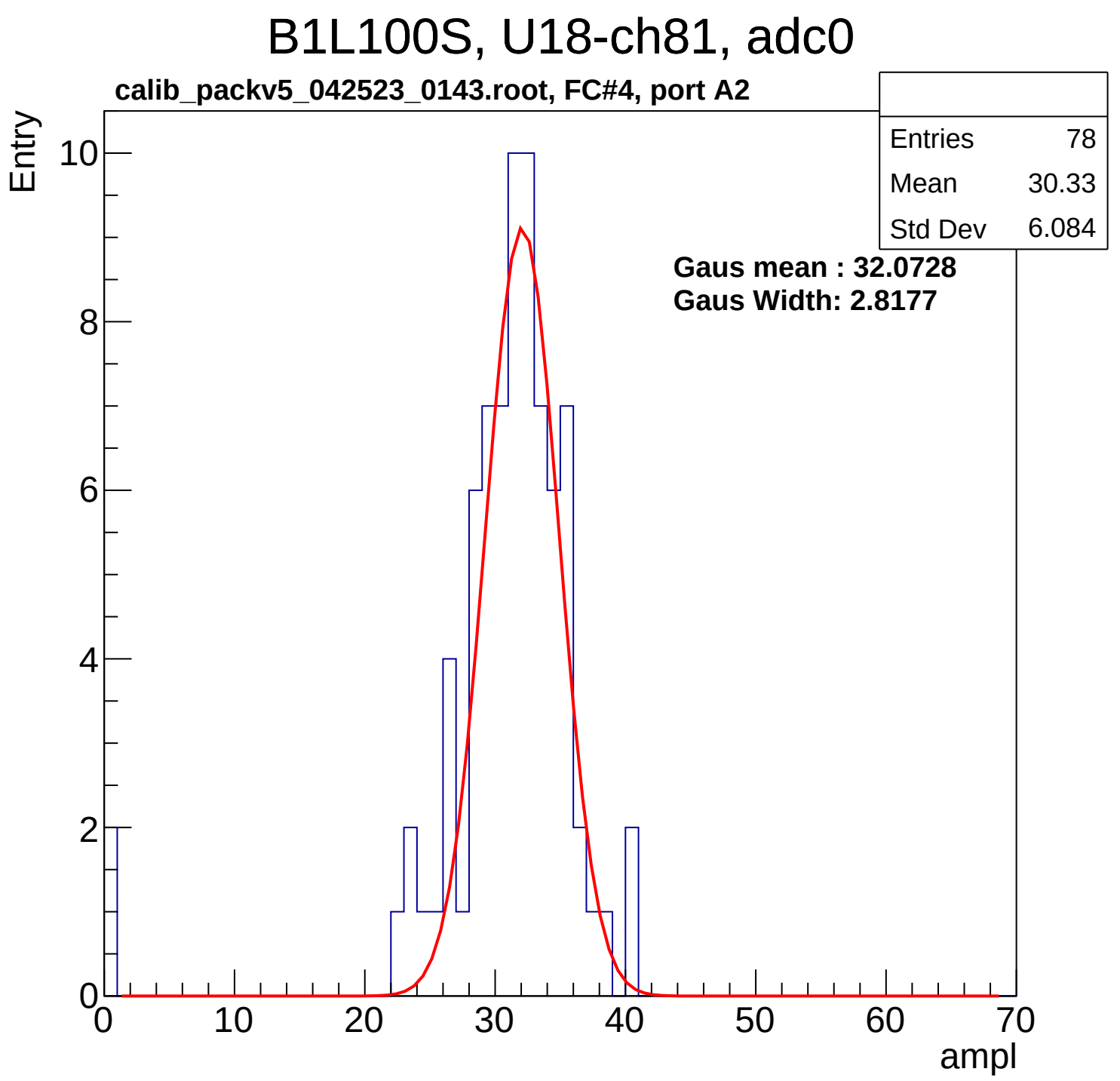

B1L100S, U18-ch80, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 49.32
Std Dev 3.029
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

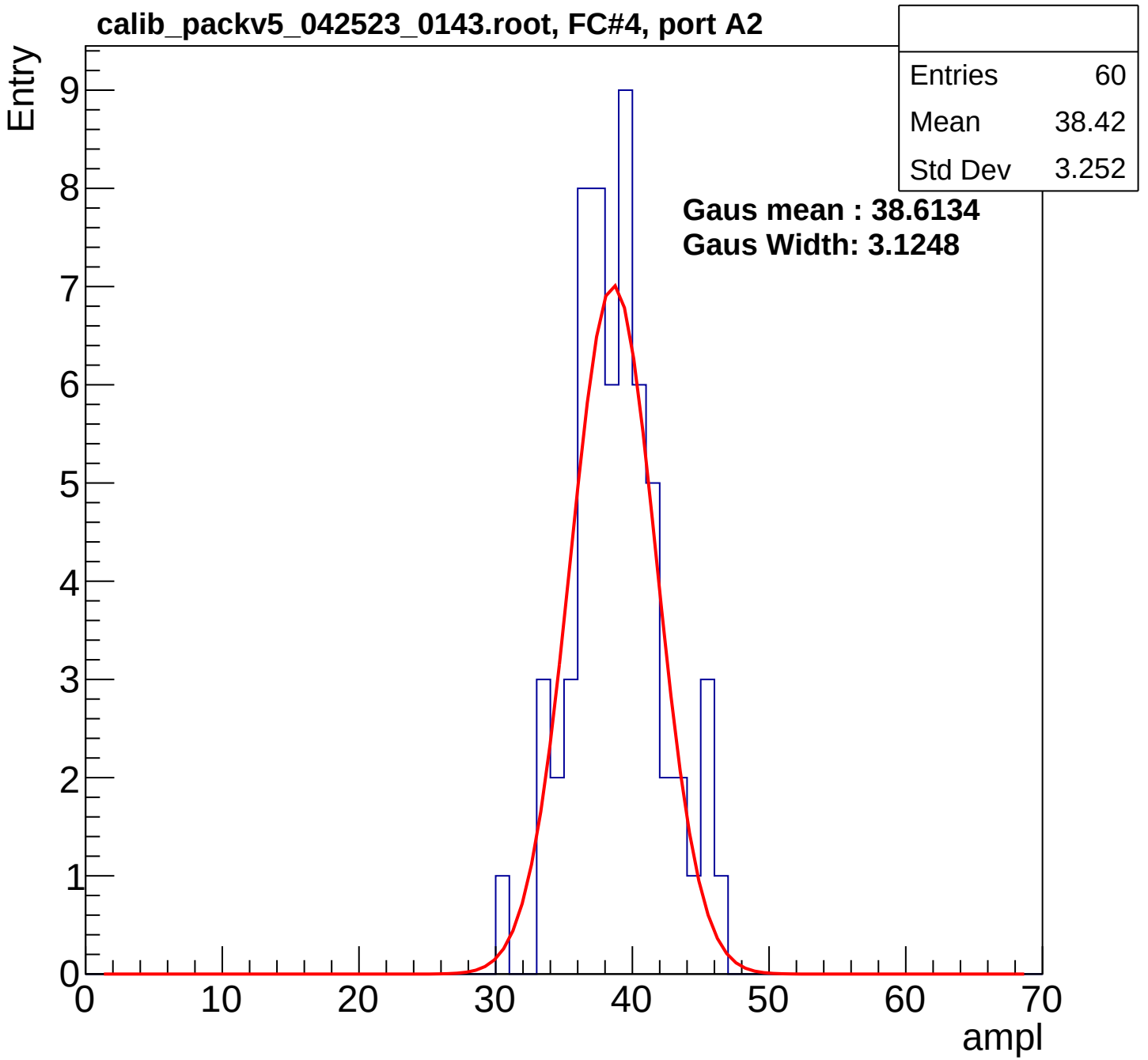

B1L100S, U18-ch80, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 55.52
Std Dev 3.699
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

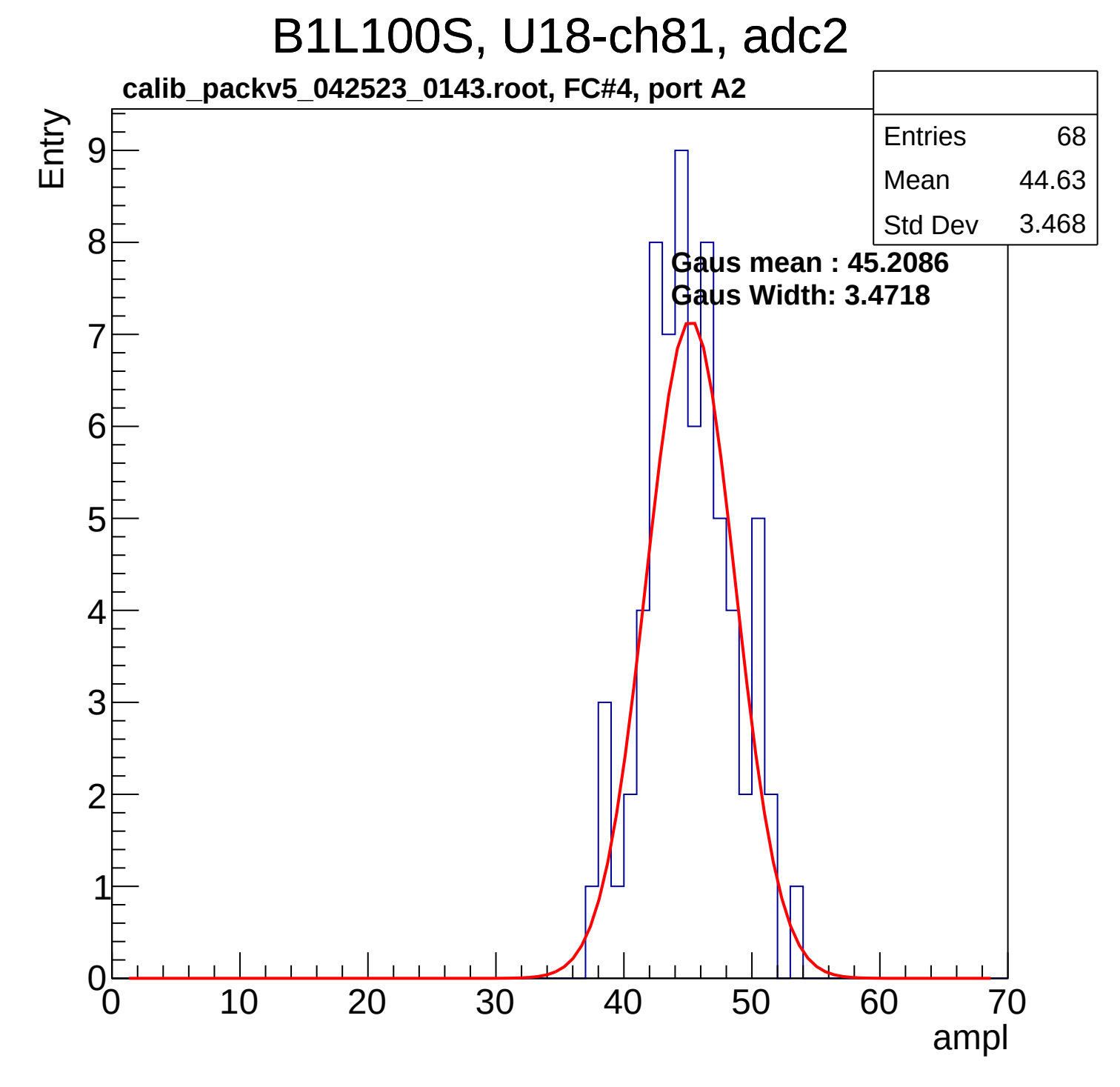

B1L100S, U18-ch80, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 58.94
Std Dev 3.294
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

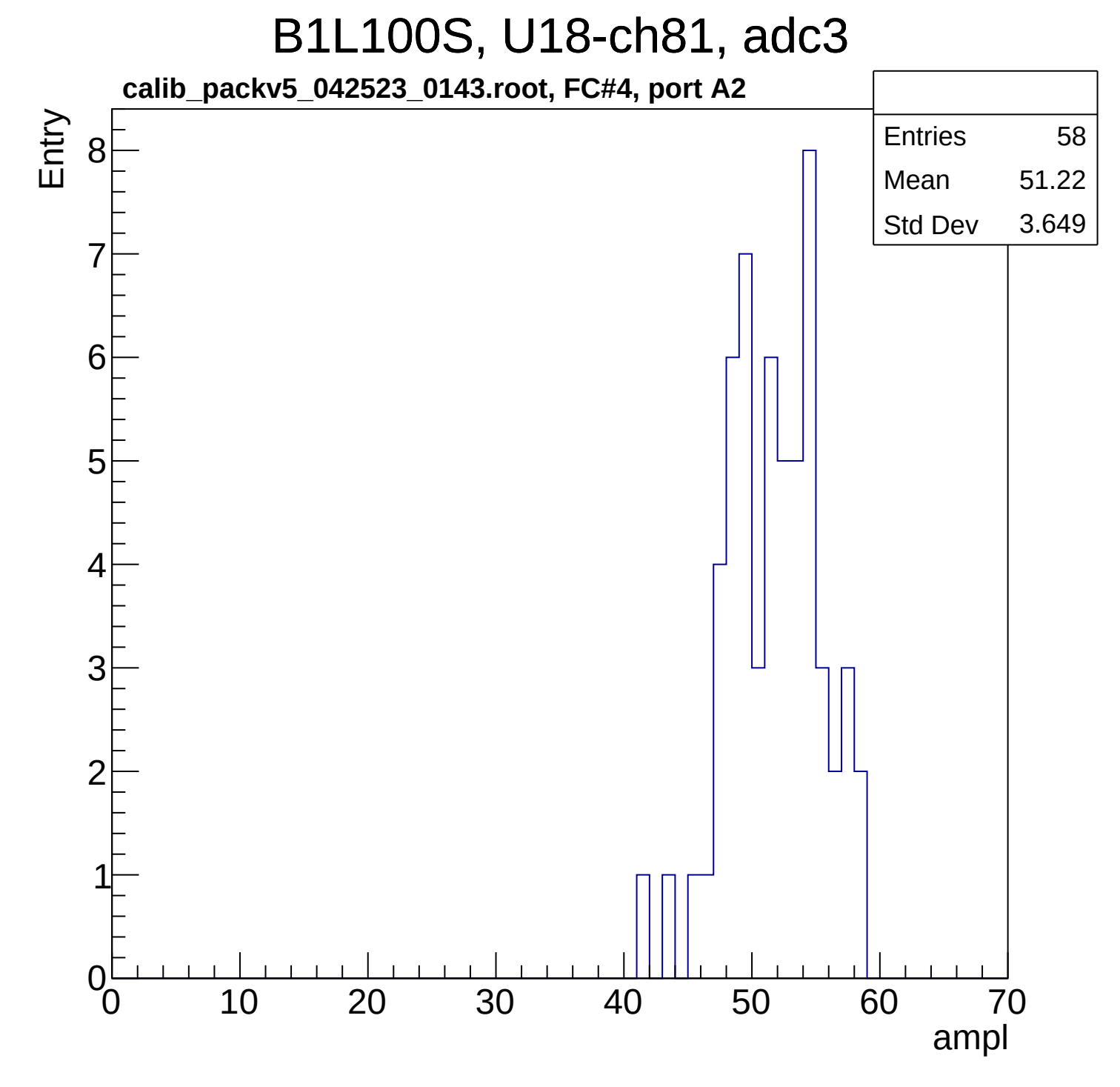

B1L100S, U18-ch80, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 8
Mean 53.38
Std Dev 20.25
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

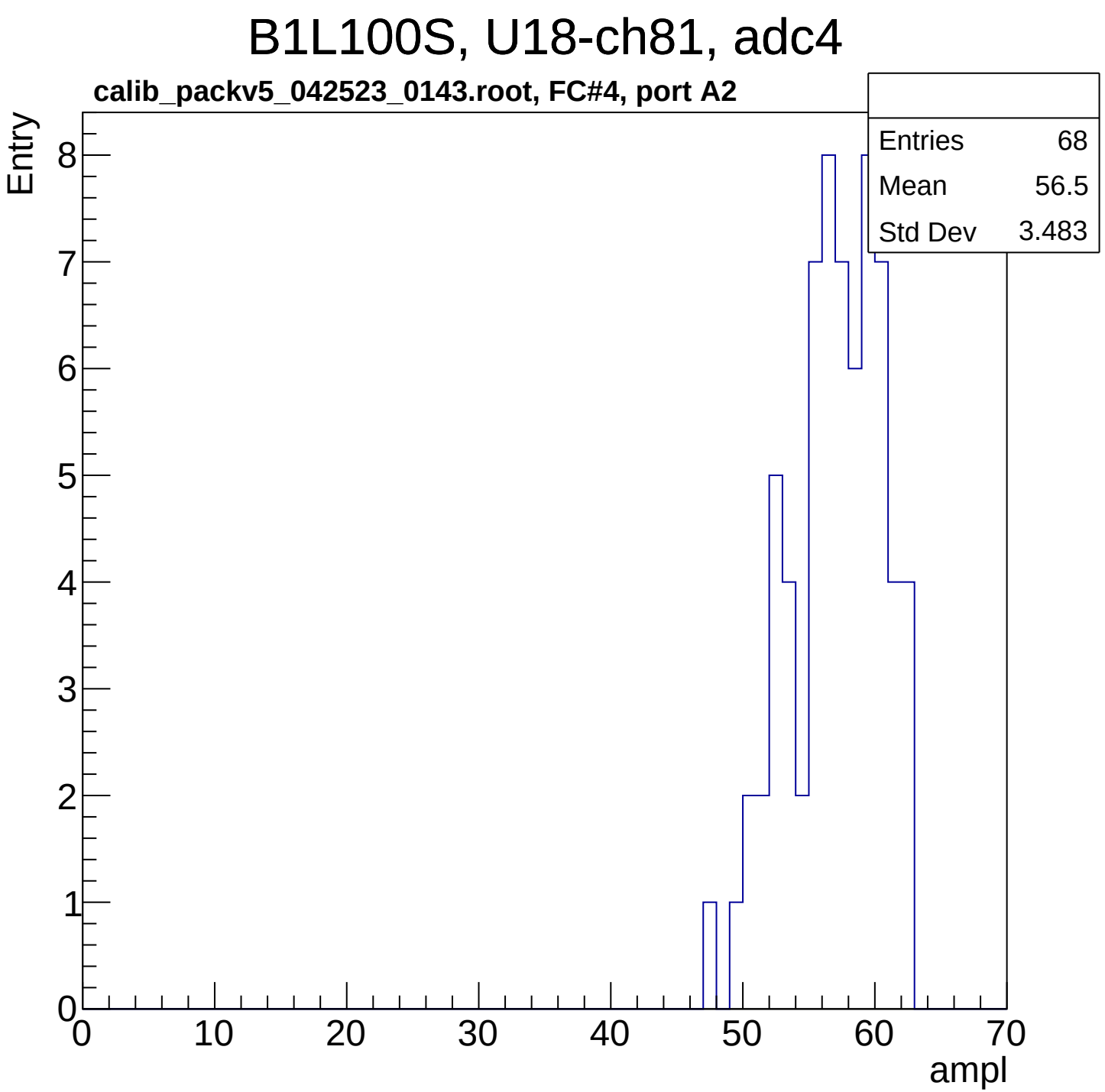

B1L100S, U18-ch80, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

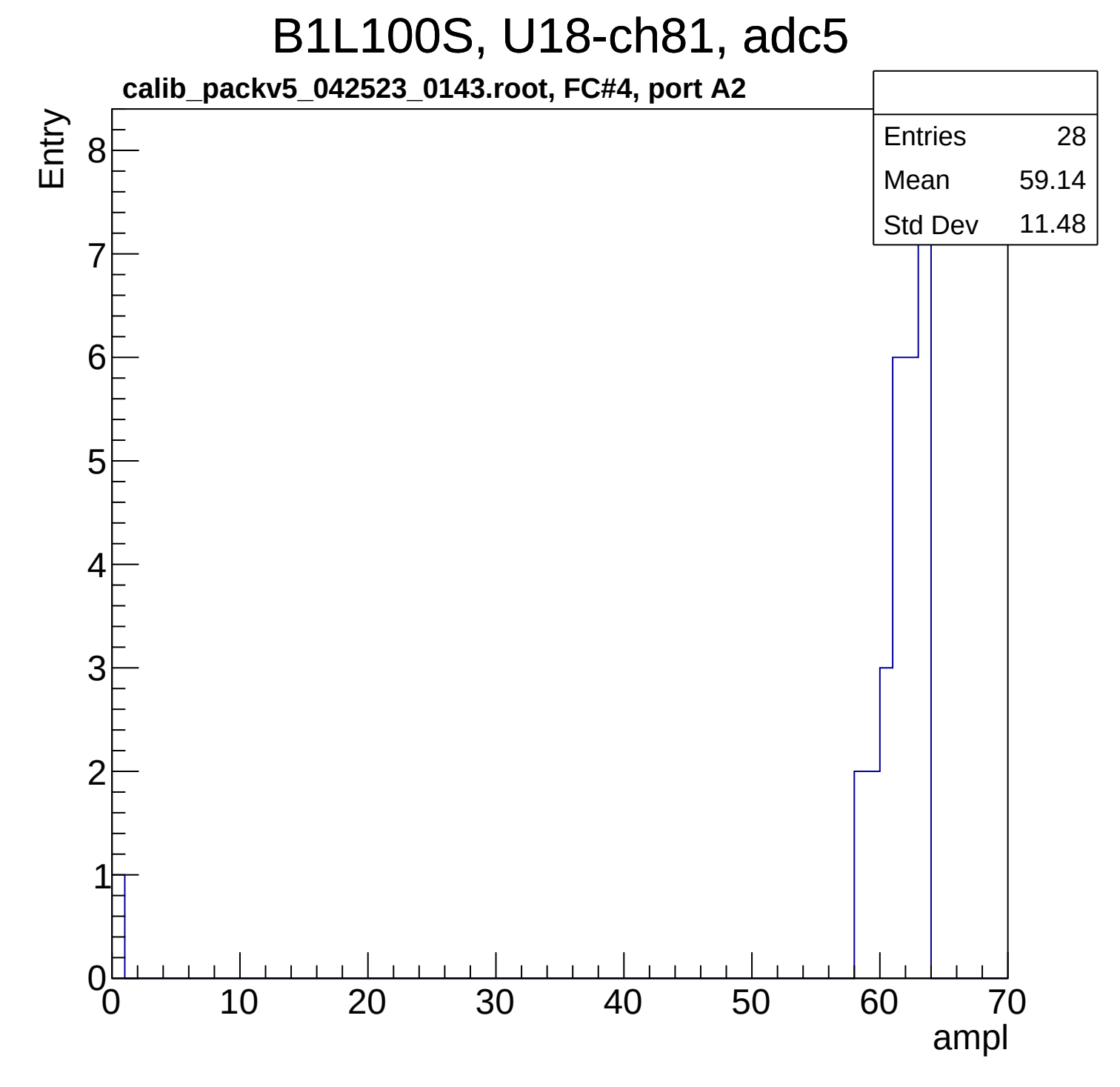

B1L100S, U18-ch81, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 30.33
Std Dev 6.084
Gaus mean : 32.0728
Gaus Width: 2.8177
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

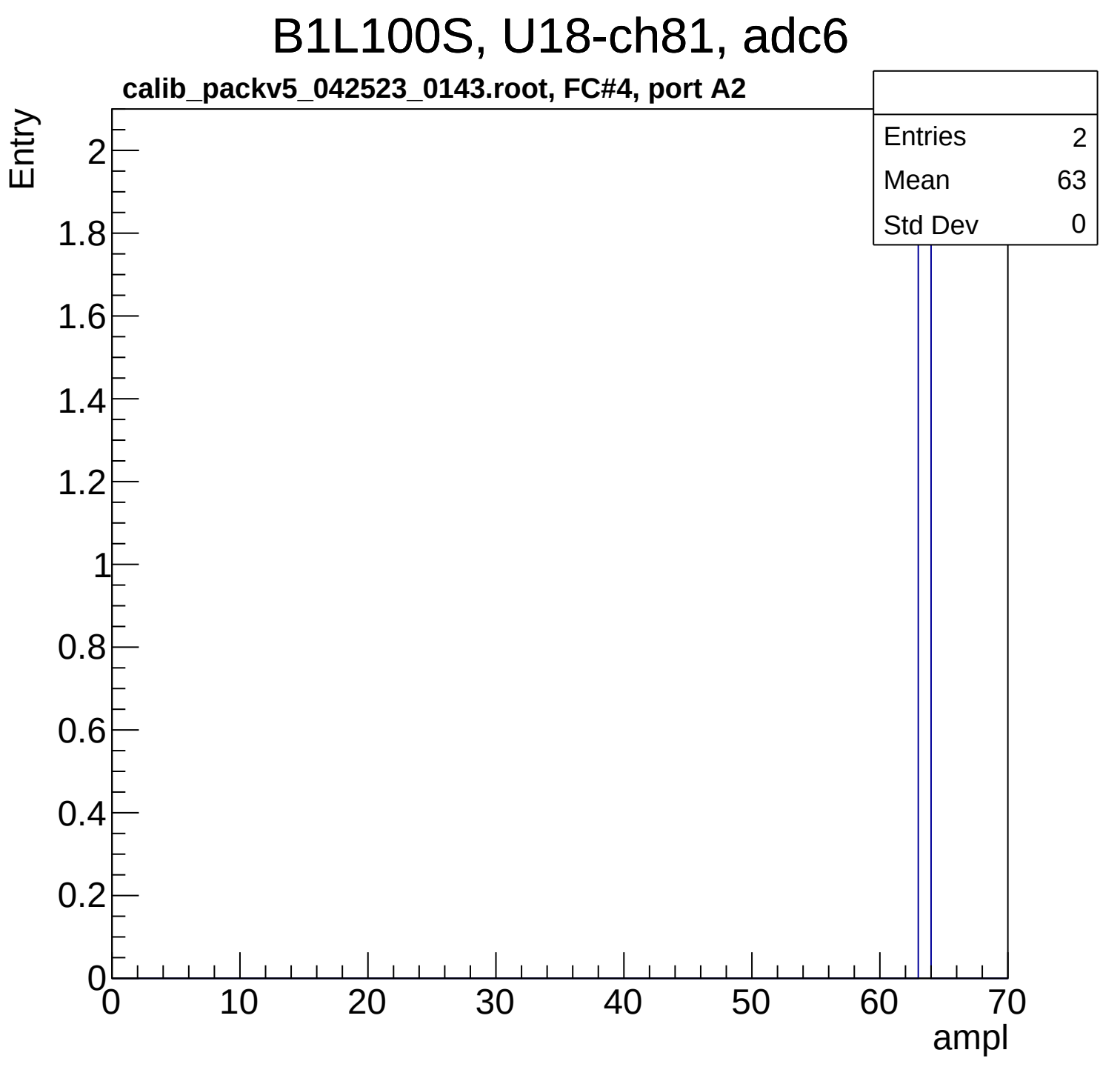

B1L100S, U18-ch81, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 38.42
Std Dev 3.252
Gaus mean : 38.6134
Gaus Width: 3.1248
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

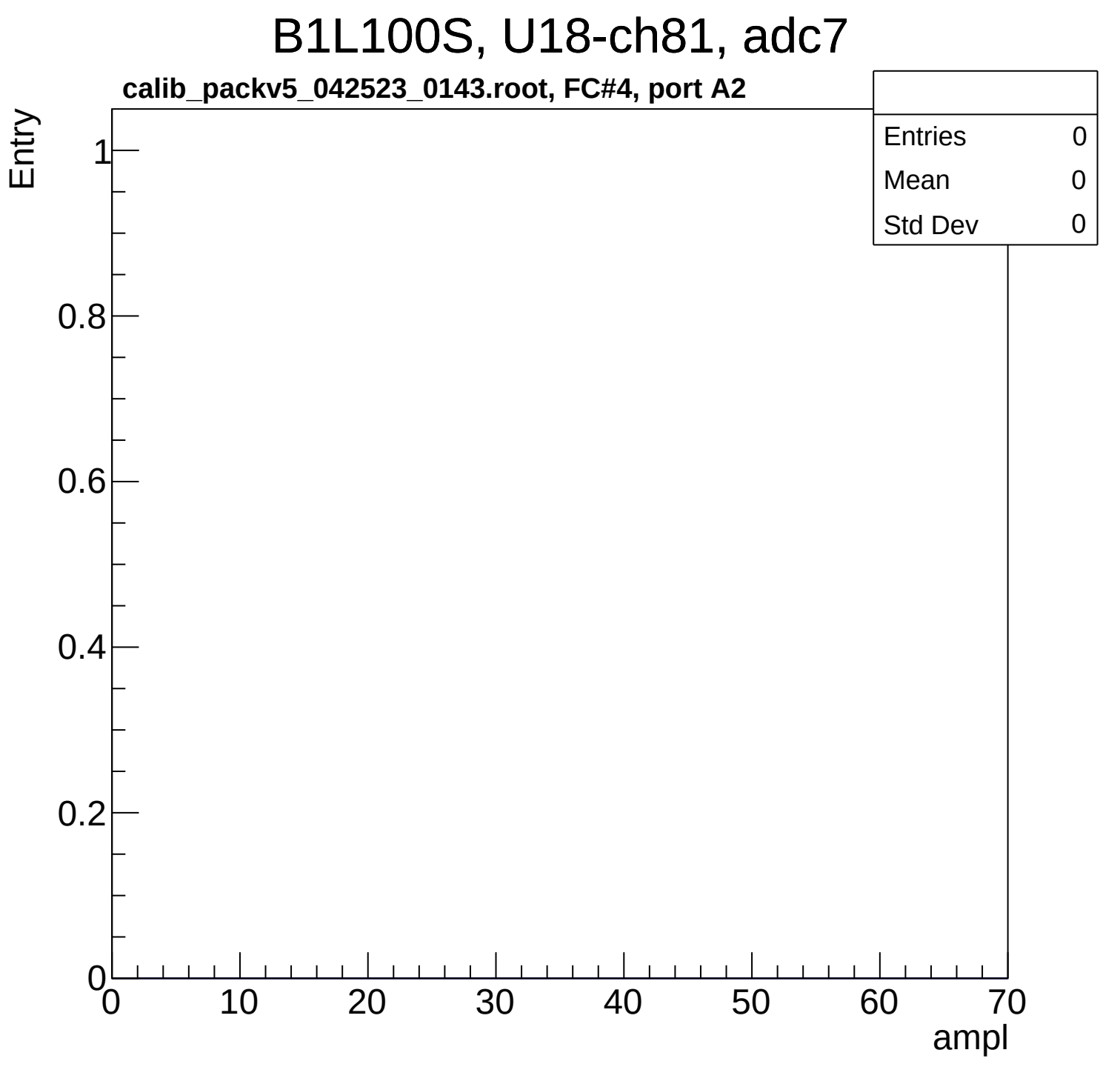

B1L100S, U18-ch81, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 44.63
Std Dev 3.468
Gaus mean : 45.2086
Gaus Width: 3.4718
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

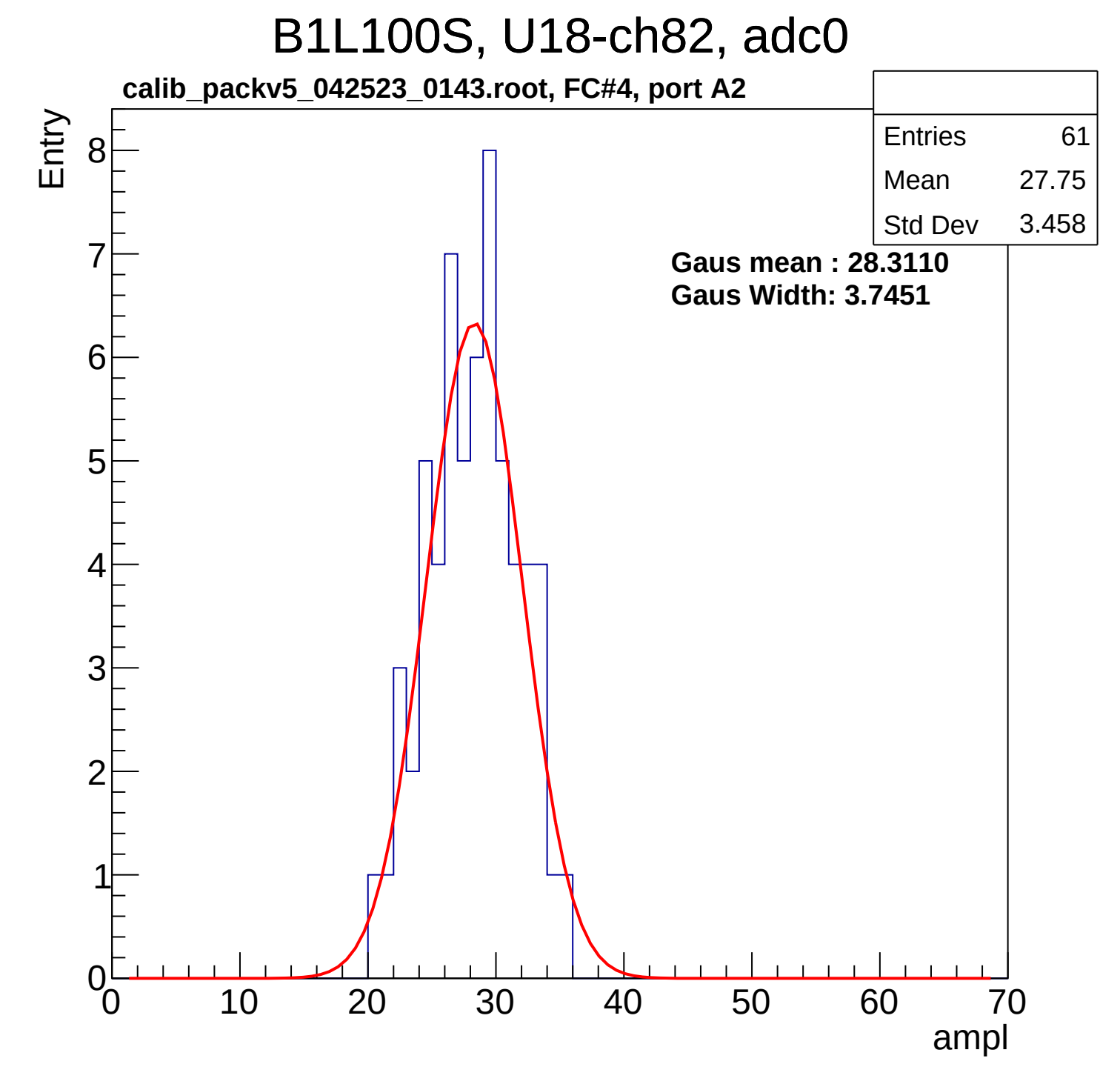

B1L100S, U18-ch81, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 51.22
Std Dev 3.649
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

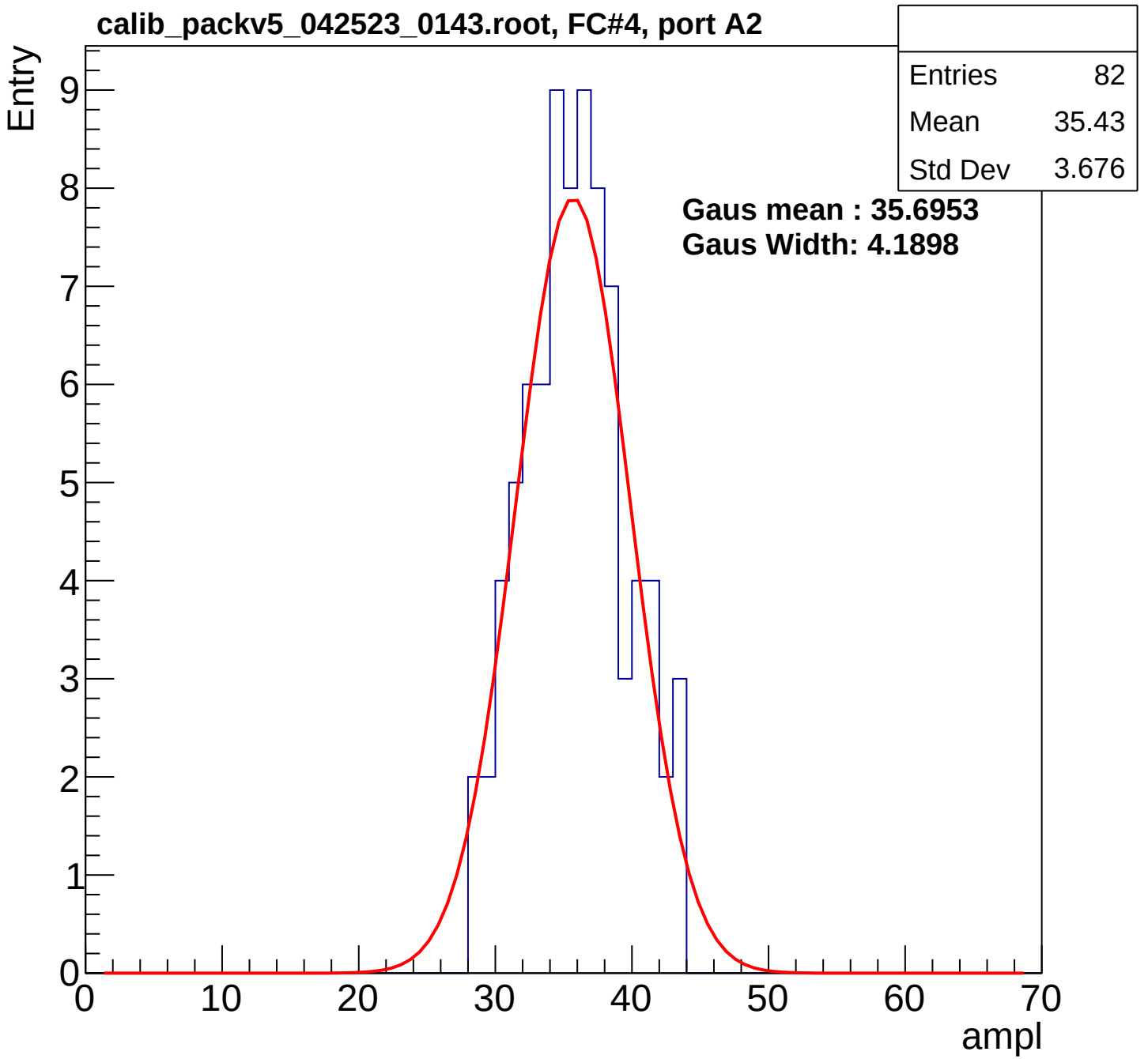

B1L100S, U18-ch81, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 56.5
Std Dev 3.483
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

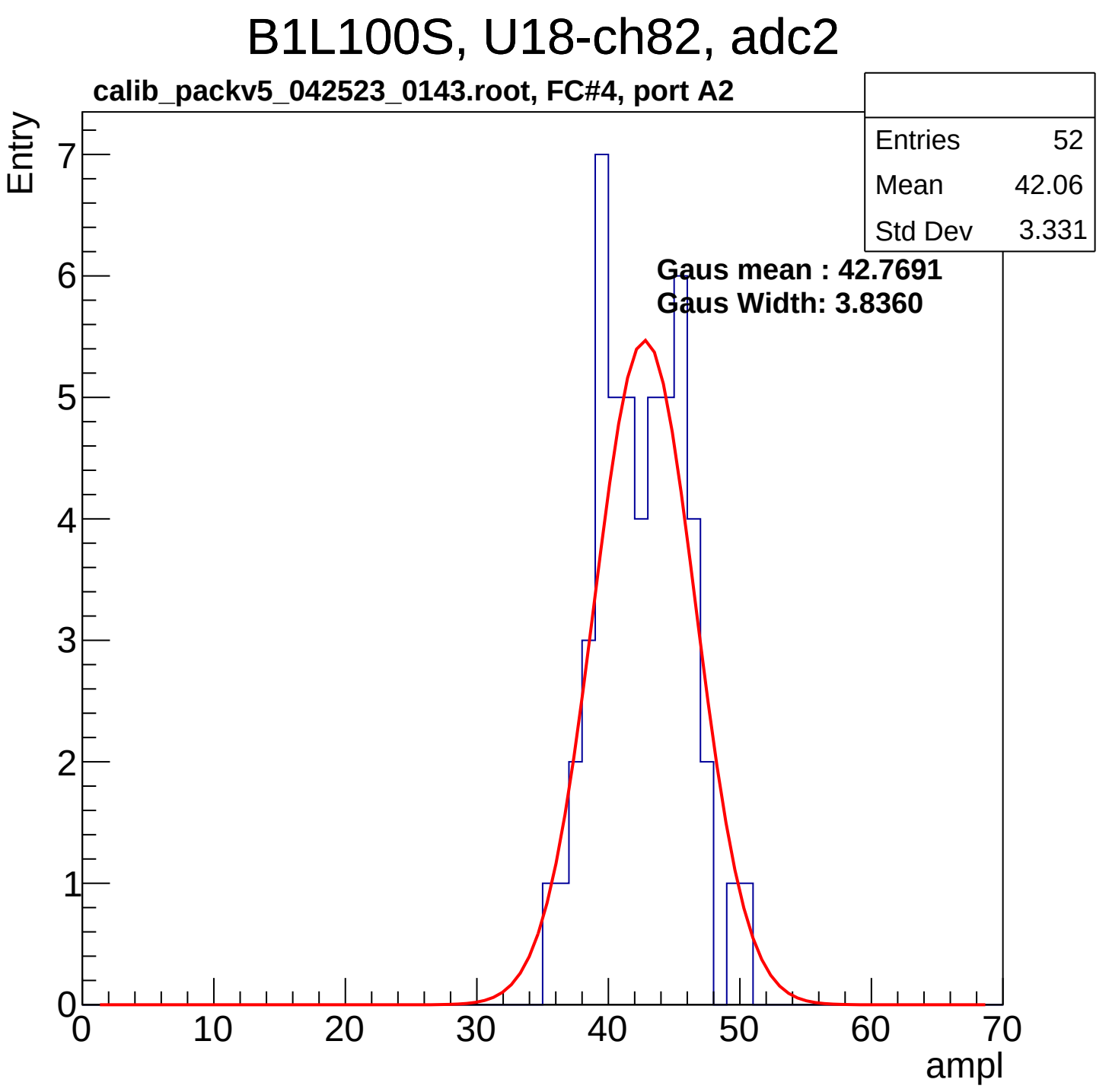

B1L100S, U18-ch81, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 28
Mean 59.14
Std Dev 11.48
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

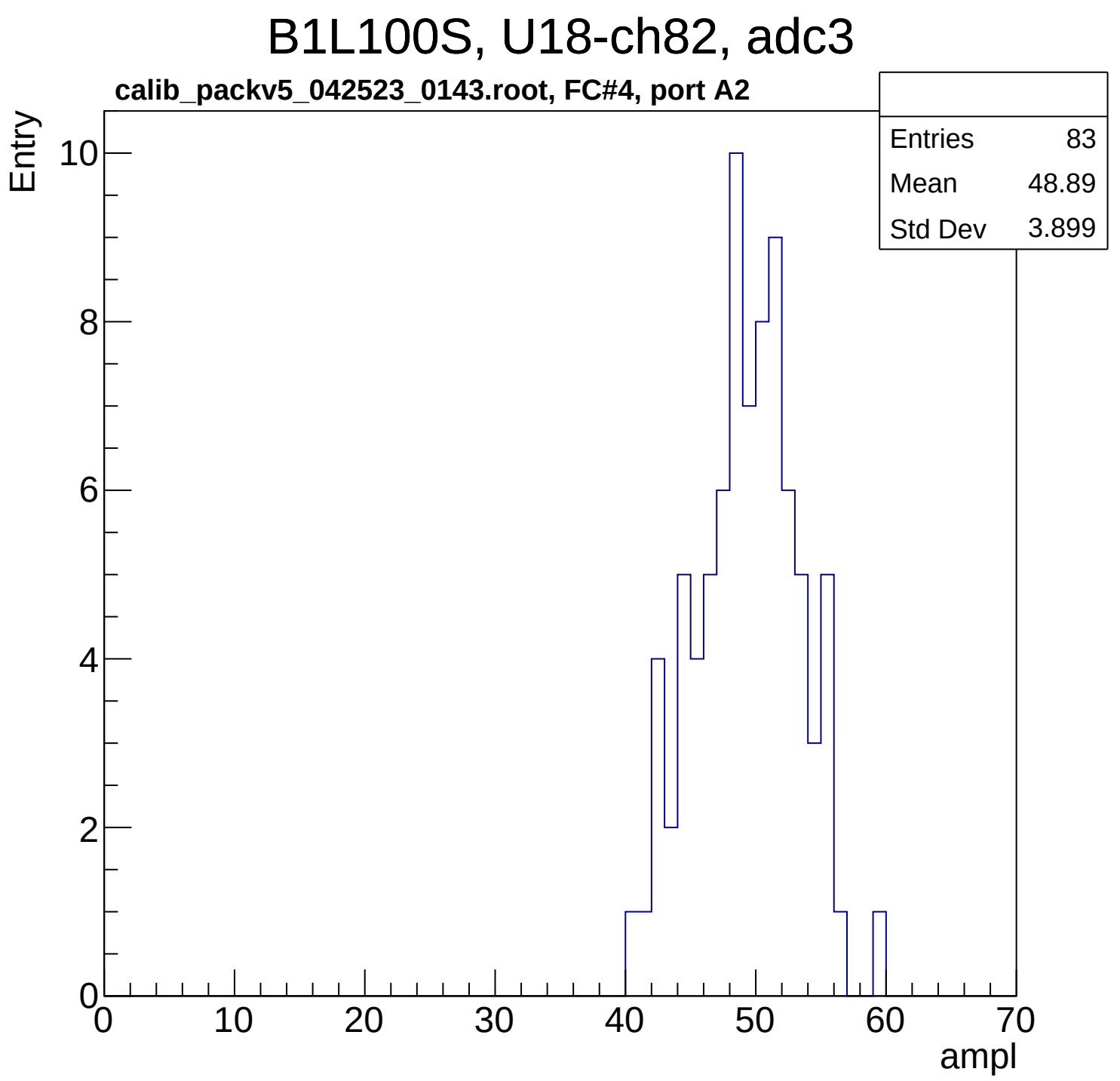

B1L100S, U18-ch81, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

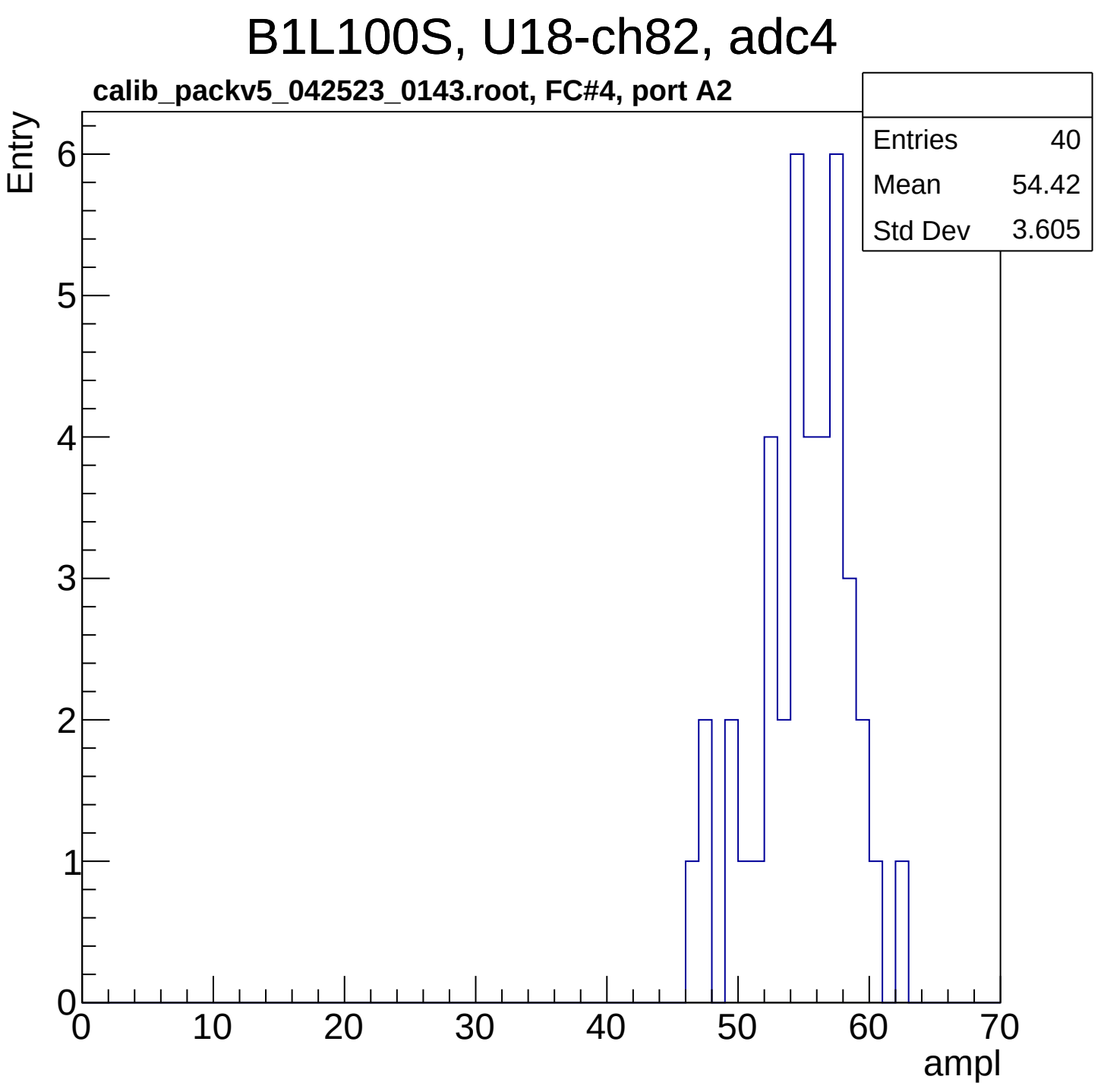

B1L100S, U18-ch81, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

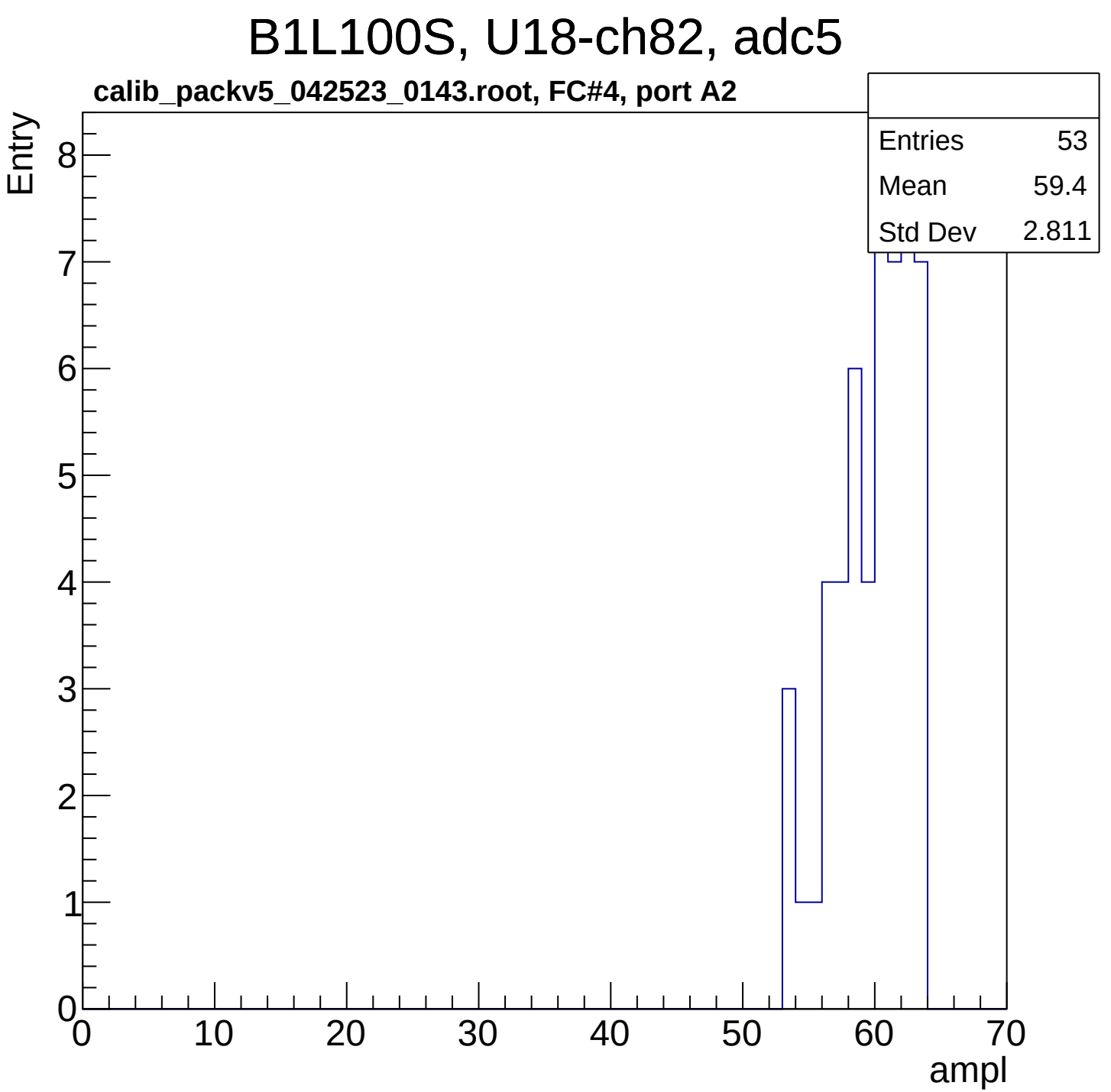

B1L100S, U18-ch82, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 27.75
Std Dev 3.458
Gaus mean : 28.3110
Gaus Width: 3.7451
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

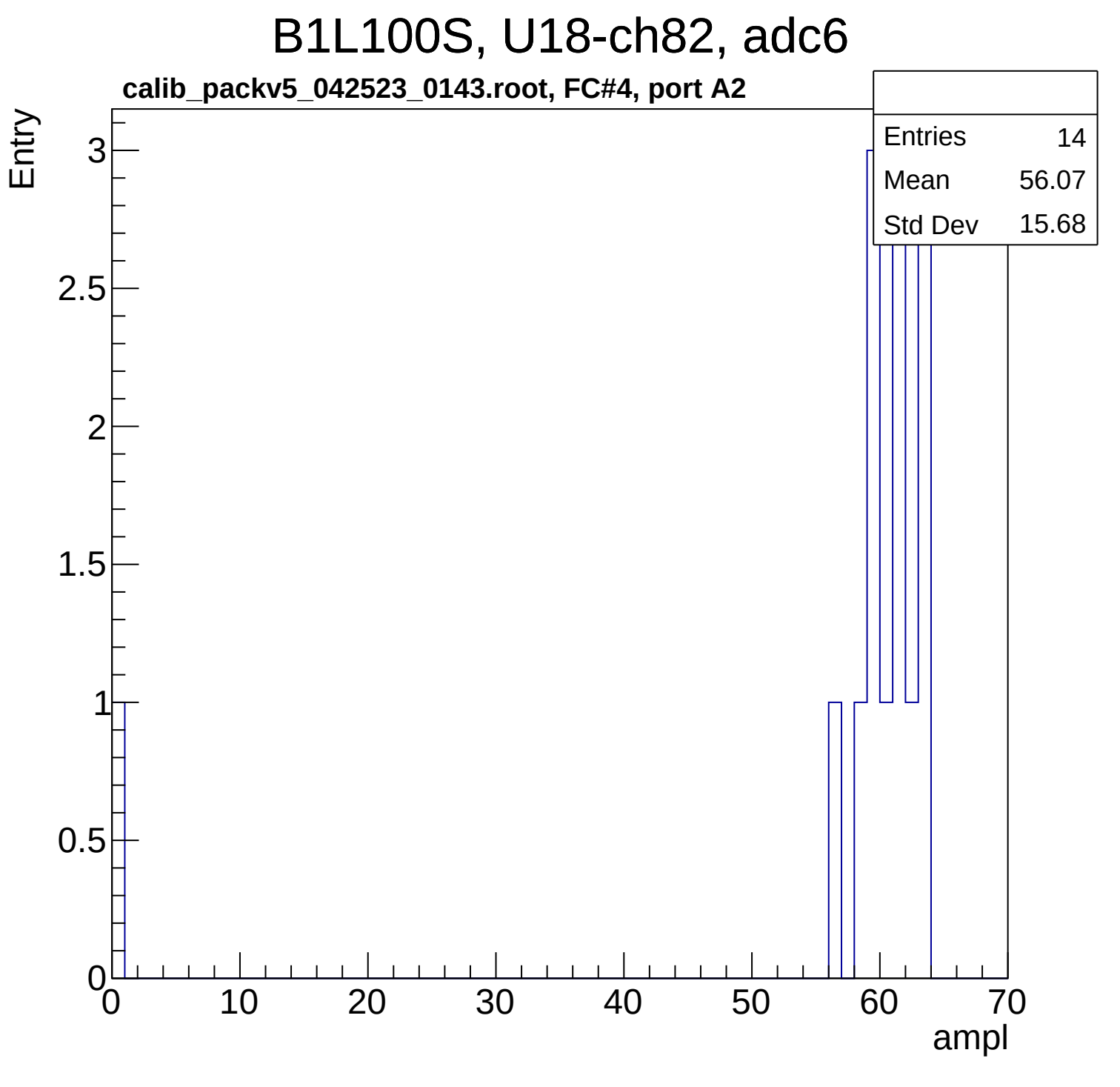

B1L100S, U18-ch82, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 35.43
Std Dev 3.676
Gaus mean : 35.6953
Gaus Width: 4.1898
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

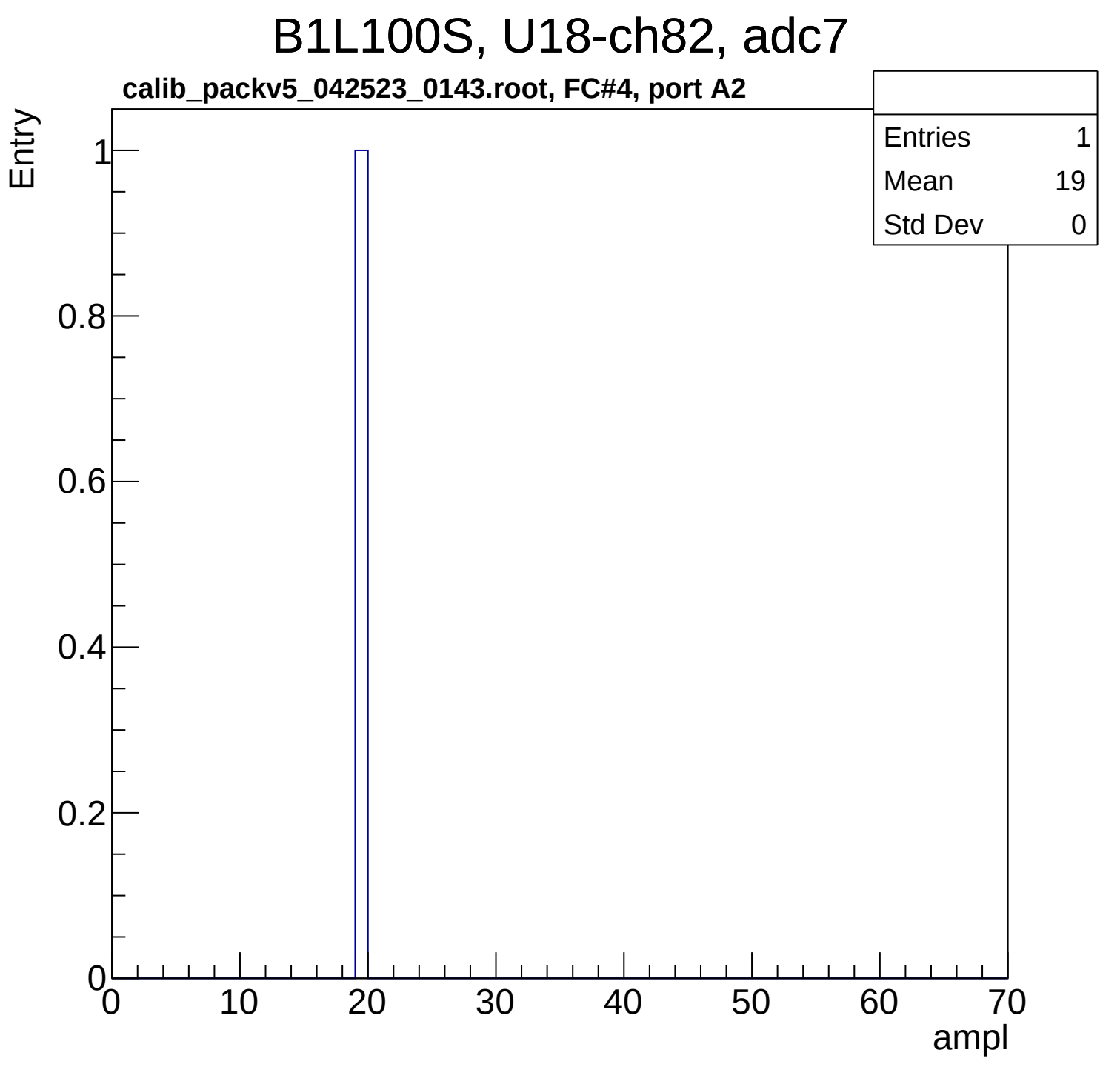

B1L100S, U18-ch82, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 42.06
Std Dev 3.331
Gaus mean : 42.7691
Gaus Width: 3.8360
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

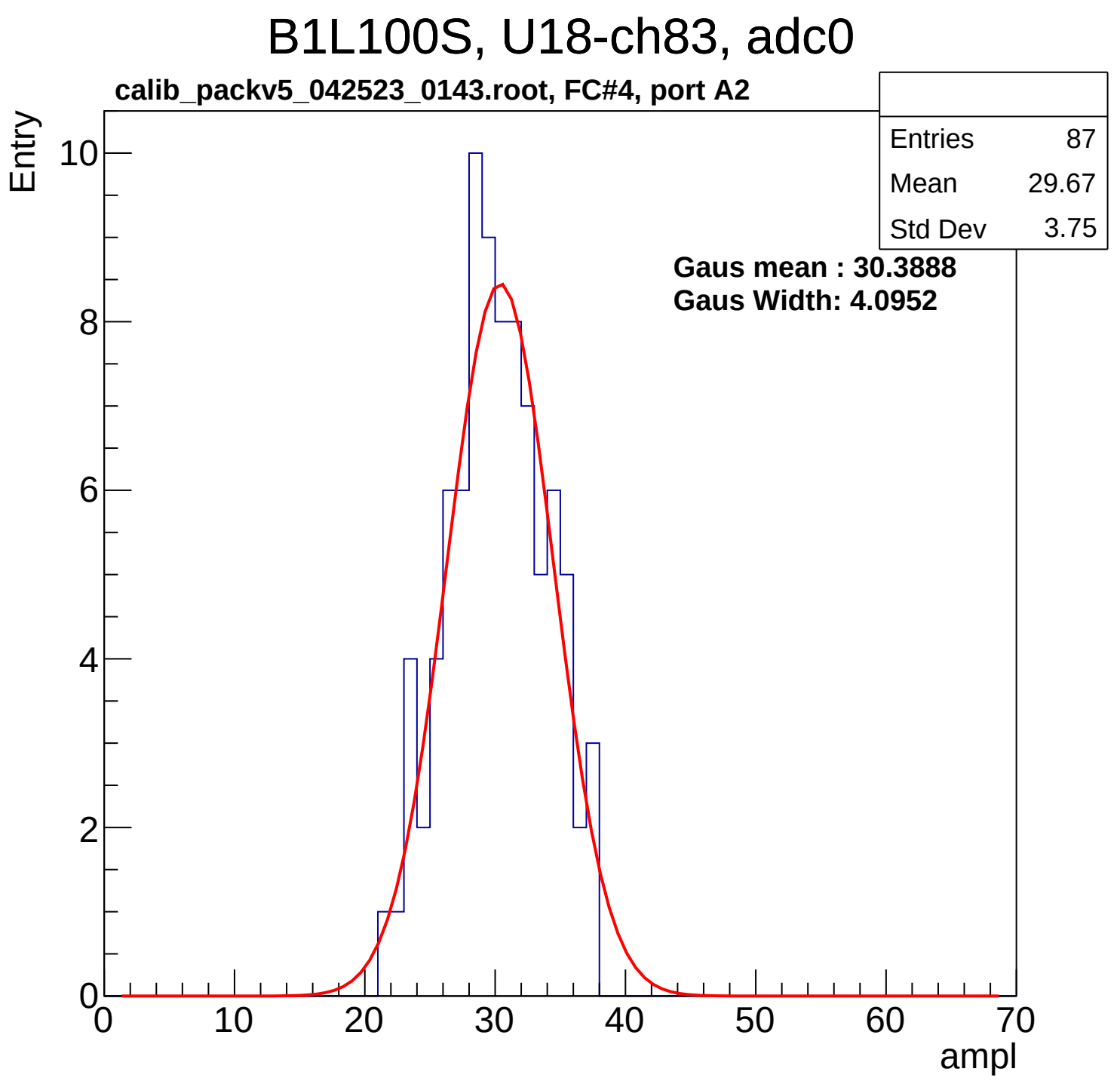

B1L100S, U18-ch82, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 83
Mean 48.89
Std Dev 3.899
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

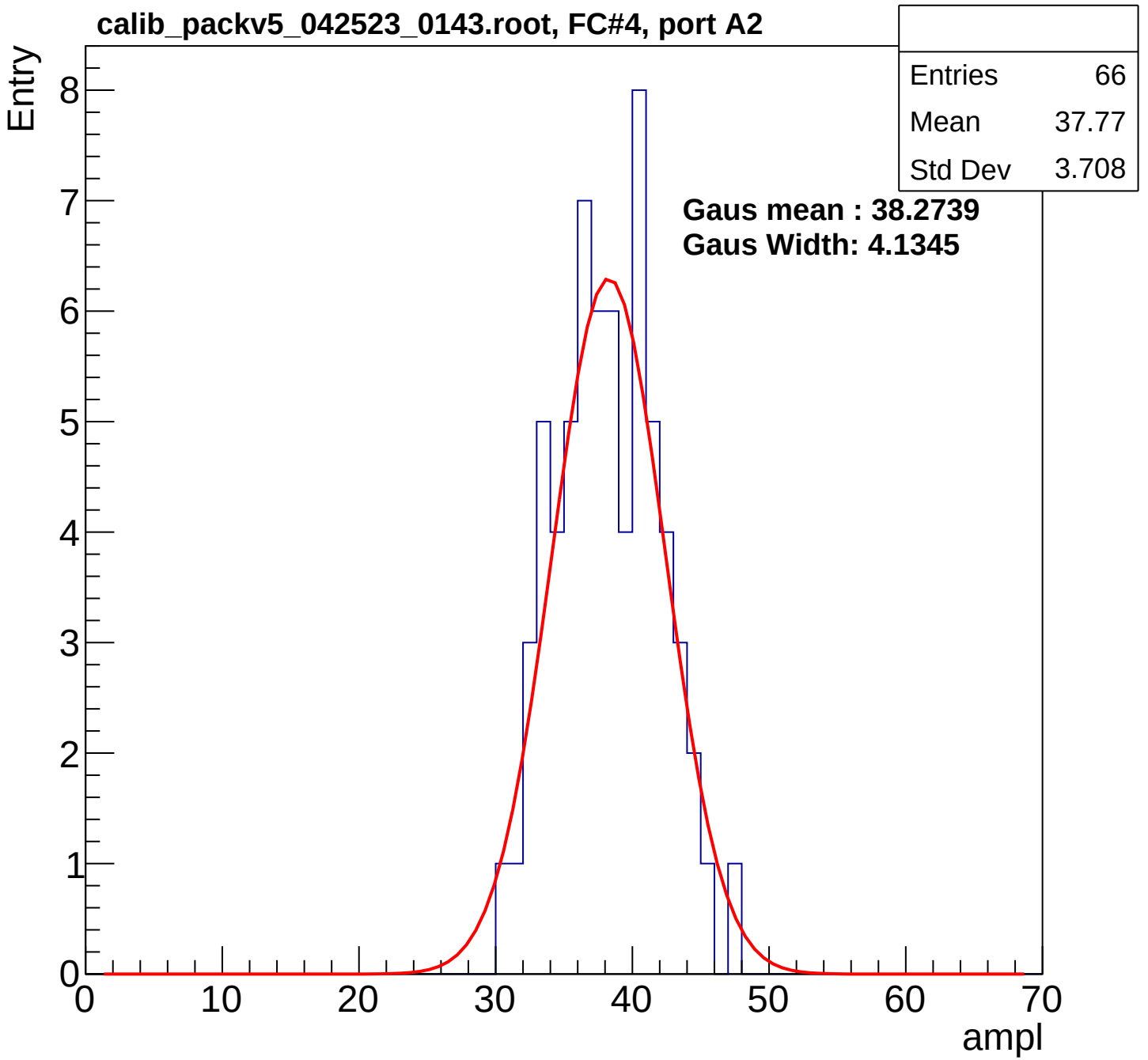

B1L100S, U18-ch82, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 40
Mean 54.42
Std Dev 3.605
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

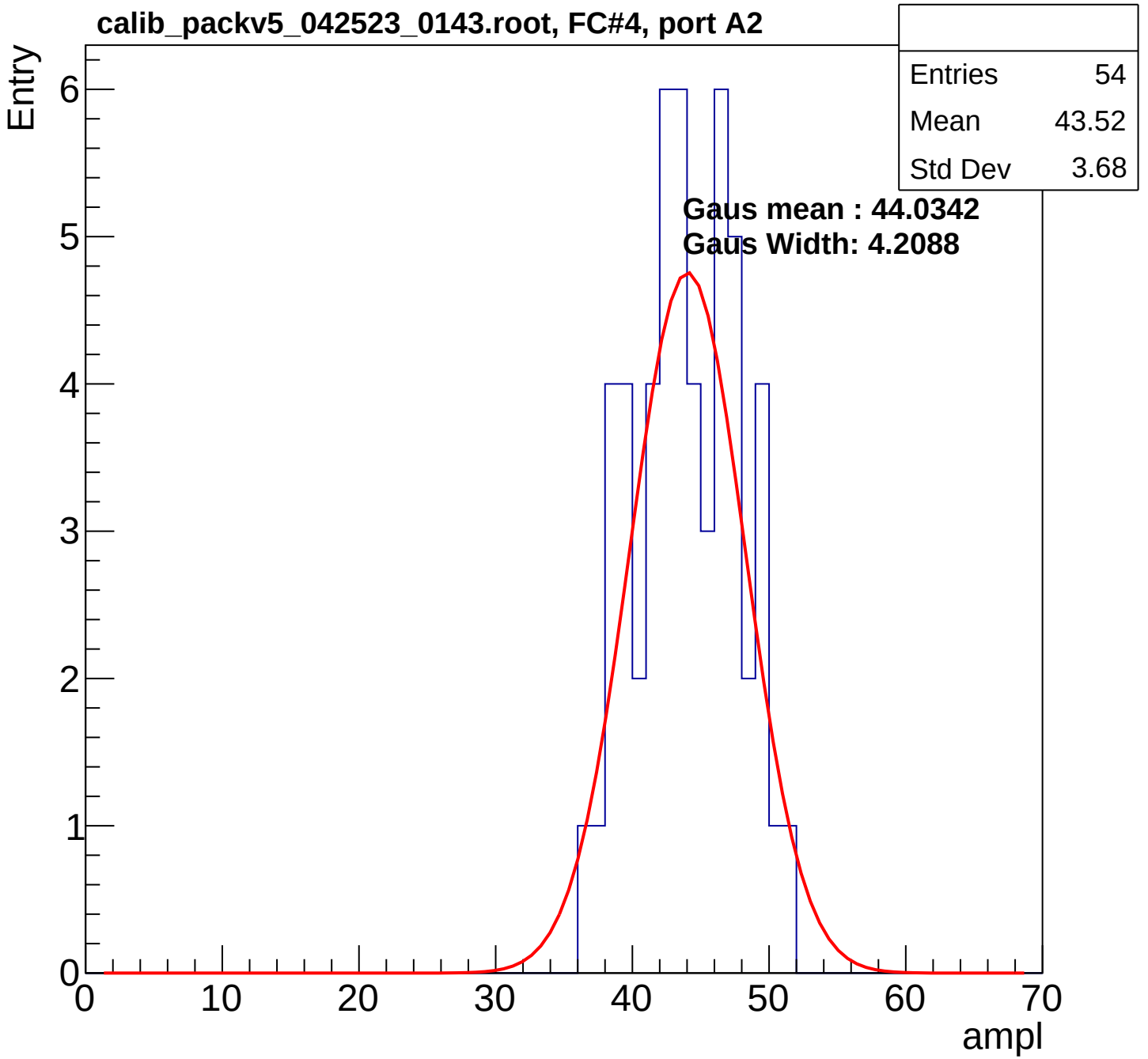

B1L100S, U18-ch82, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 59.4
Std Dev 2.811
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

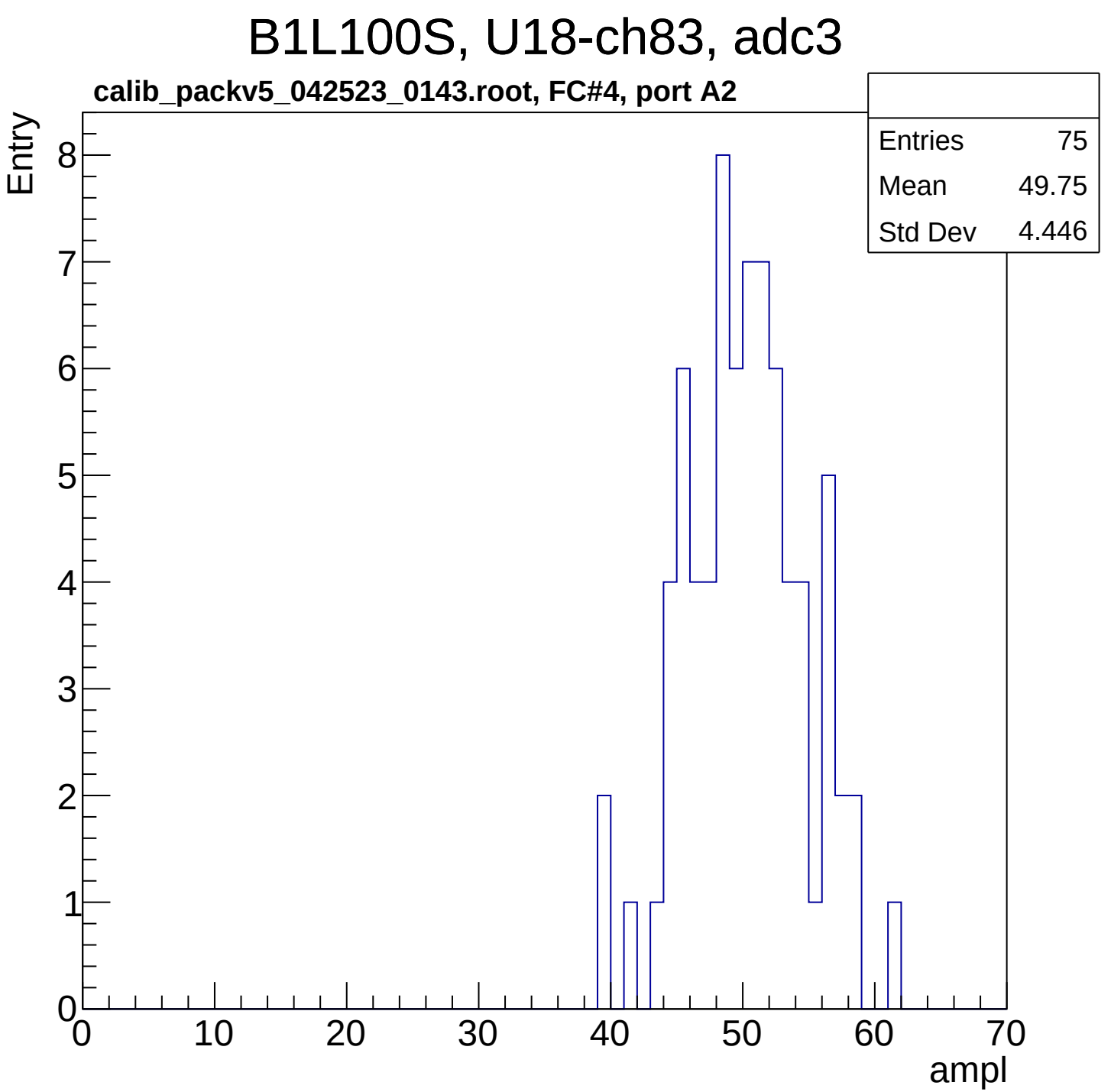

B1L100S, U18-ch82, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 14
Mean 56.07
Std Dev 15.68
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

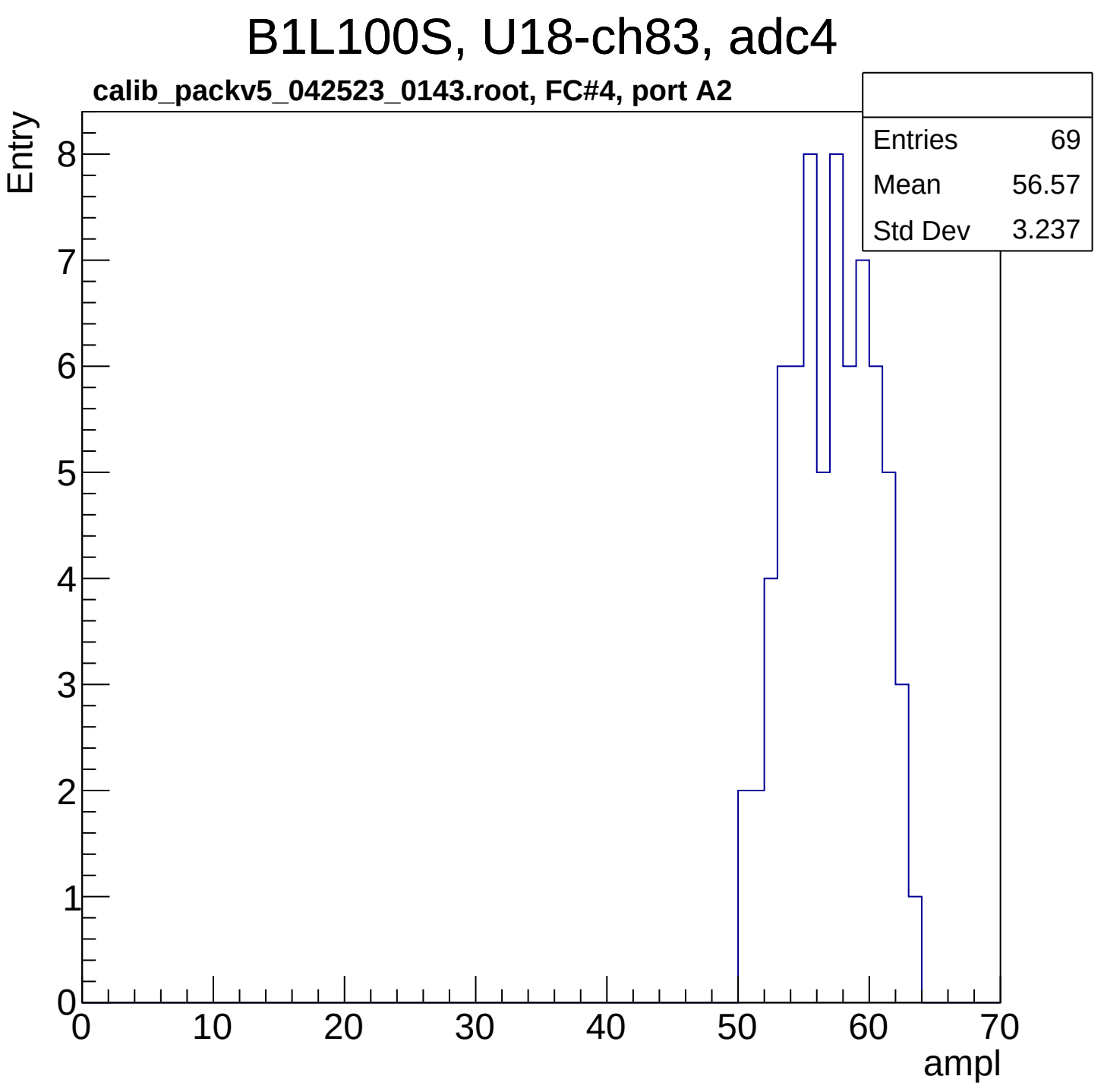

B1L100S, U18-ch82, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 19
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

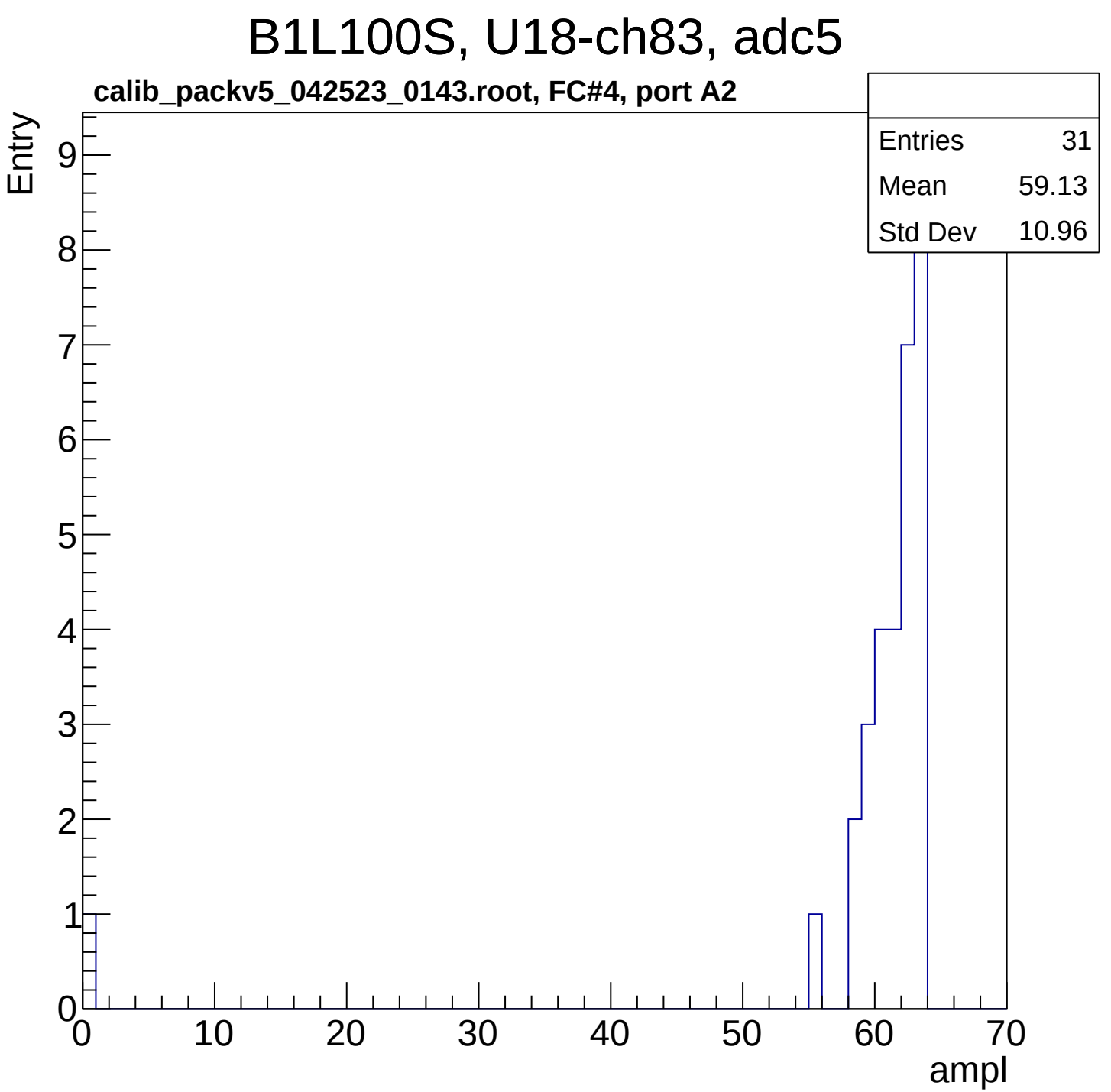

B1L100S, U18-ch83, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 87
Mean 29.67
Std Dev 3.75
Gaus mean : 30.3888
Gaus Width: 4.0952
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

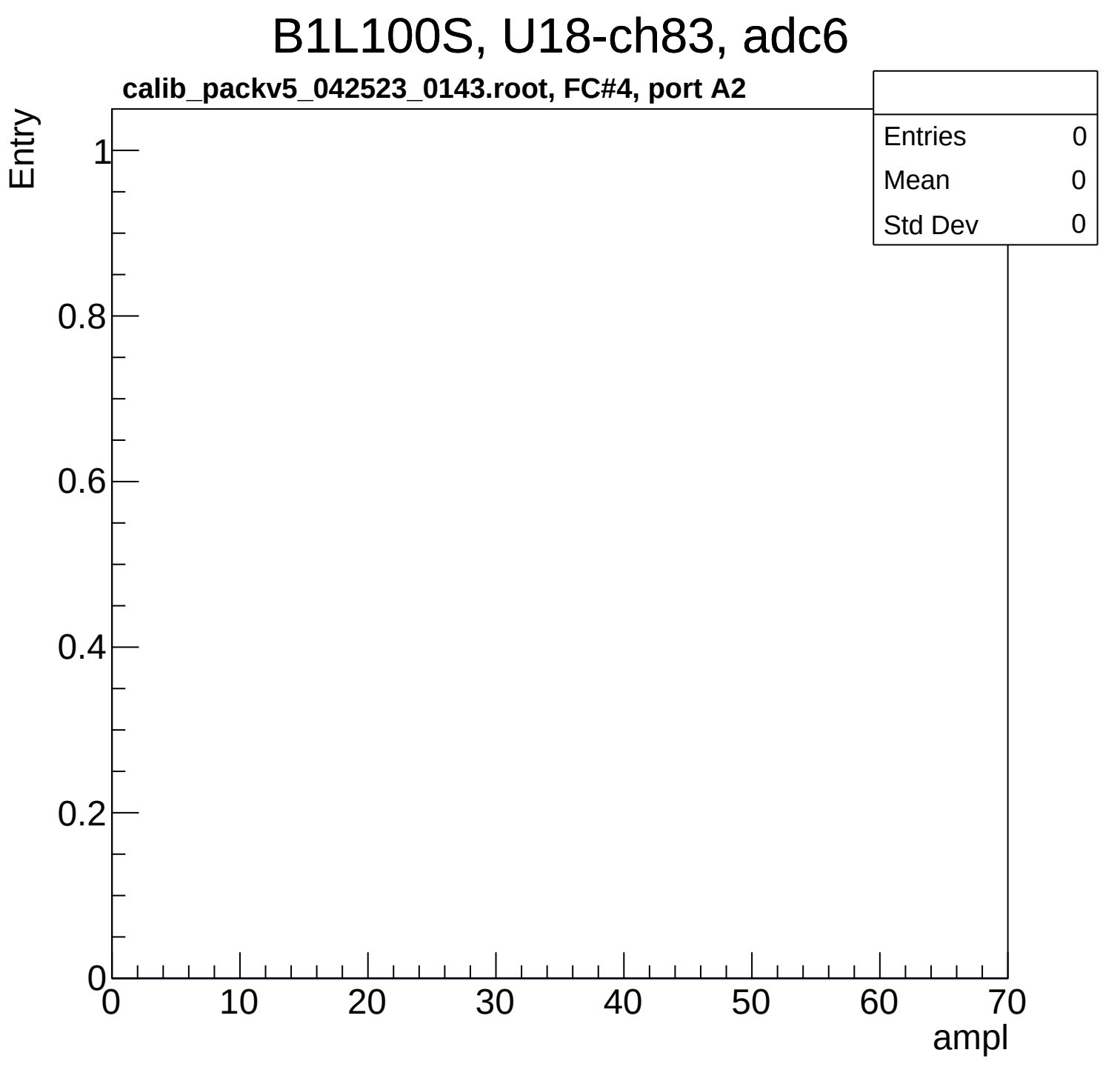

B1L100S, U18-ch83, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 37.77
Std Dev 3.708
Gaus mean : 38.2739
Gaus Width: 4.1345
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

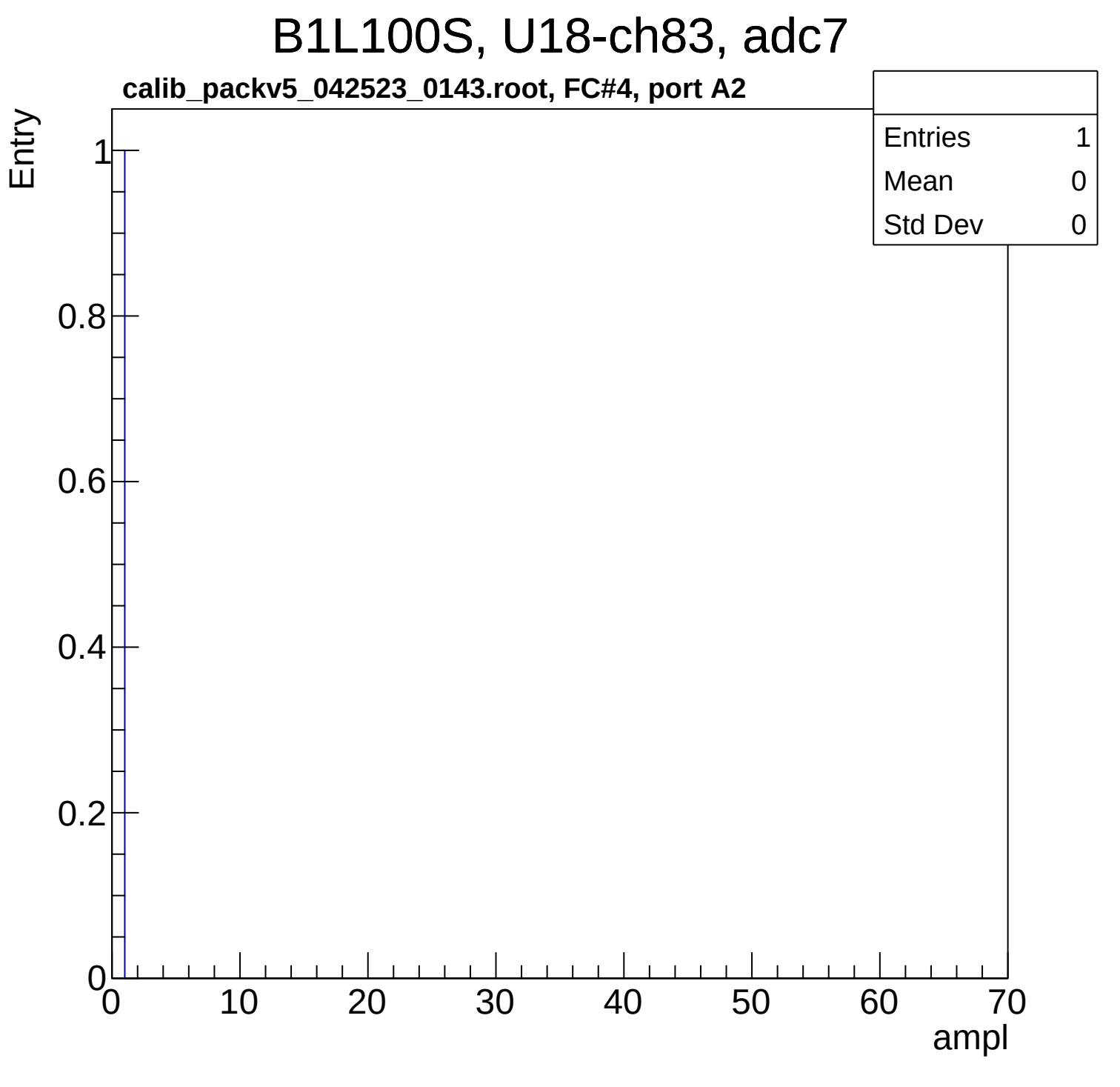

B1L100S, U18-ch83, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 43.52
Std Dev 3.68
Gaus mean : 44.0342
Gaus Width: 4.2088
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

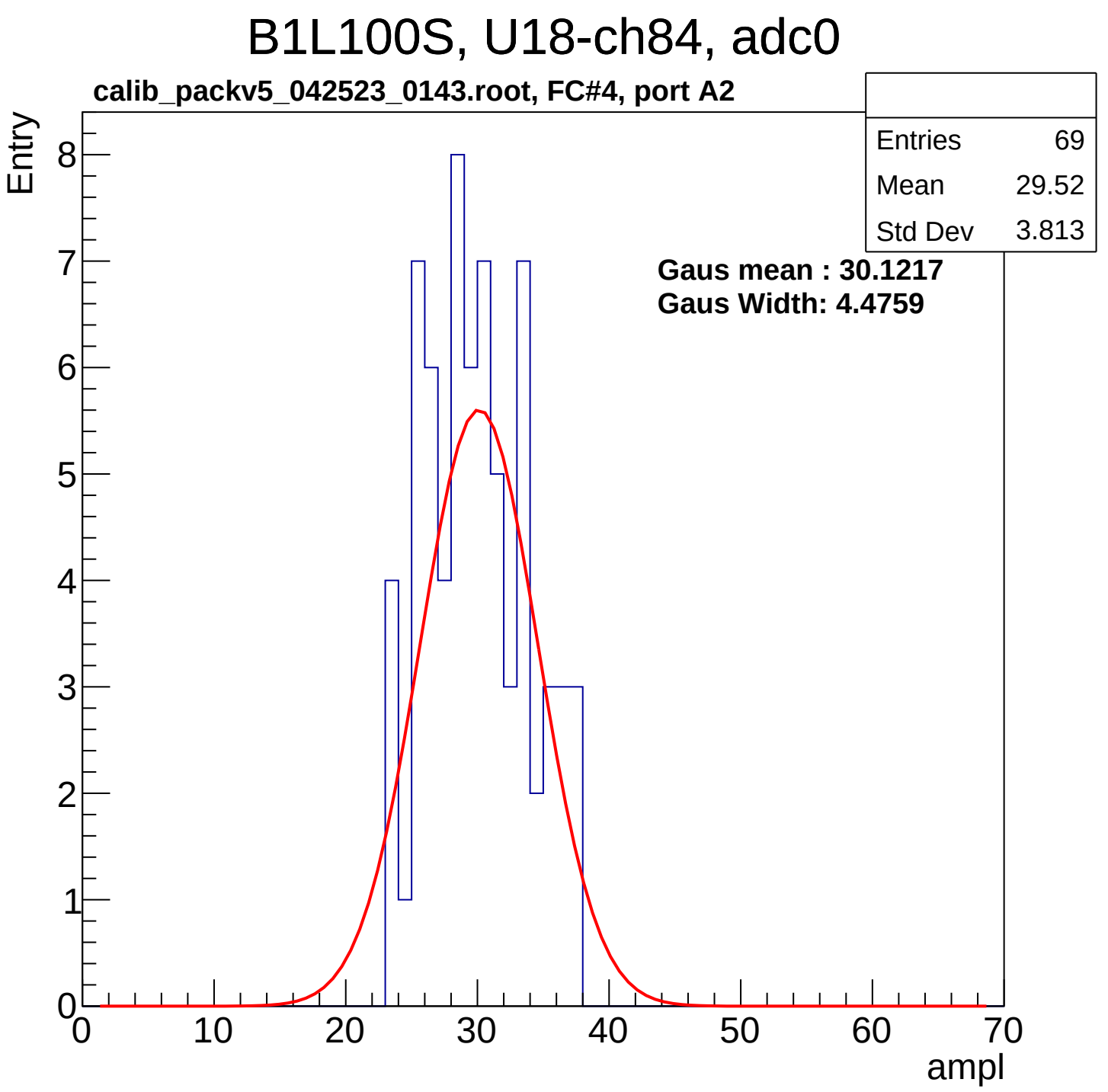

B1L100S, U18-ch83, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 49.75
Std Dev 4.446
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

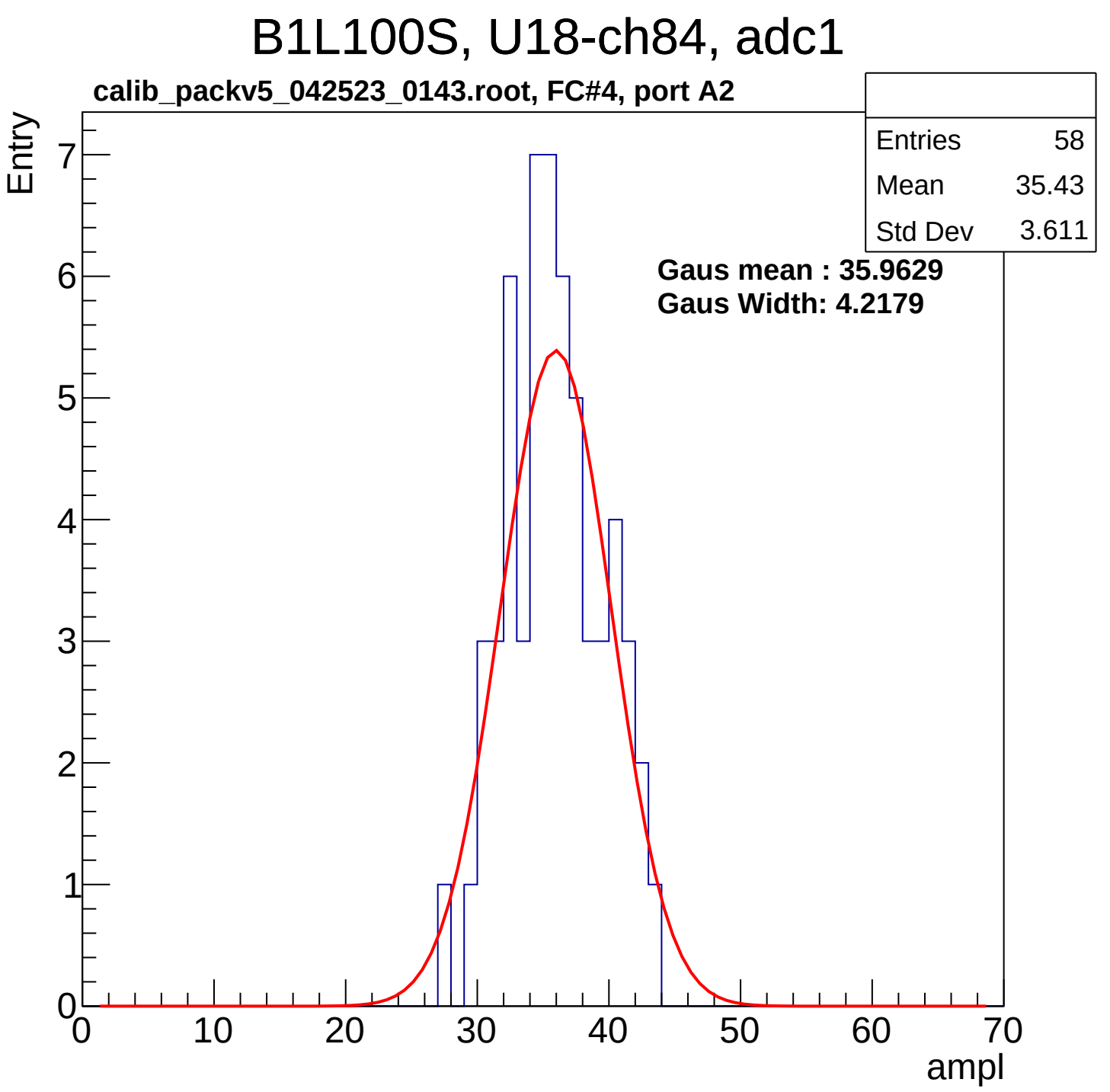

B1L100S, U18-ch83, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 56.57
Std Dev 3.237
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

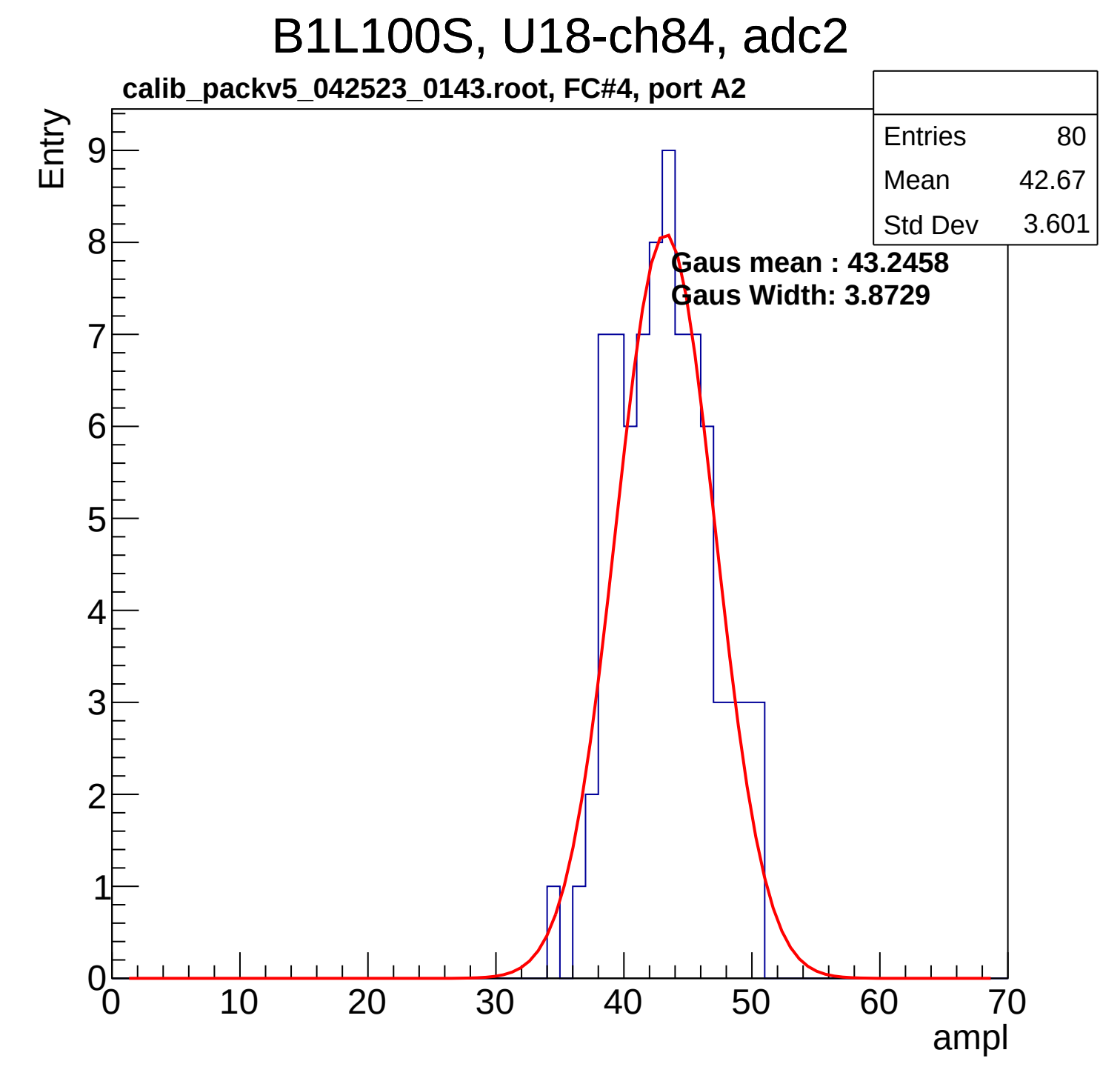

B1L100S, U18-ch83, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 31
Mean 59.13
Std Dev 10.96
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

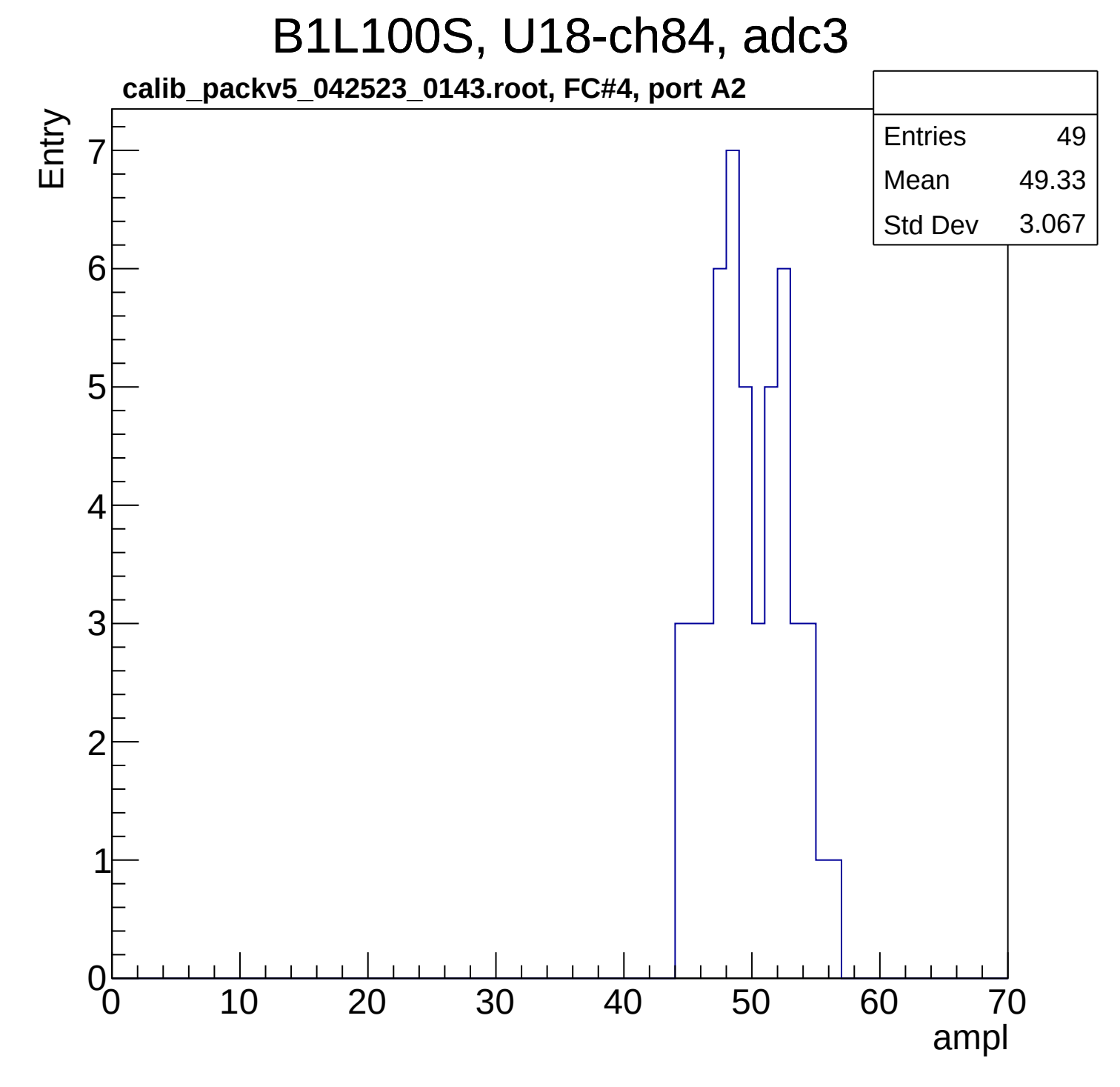

B1L100S, U18-ch83, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

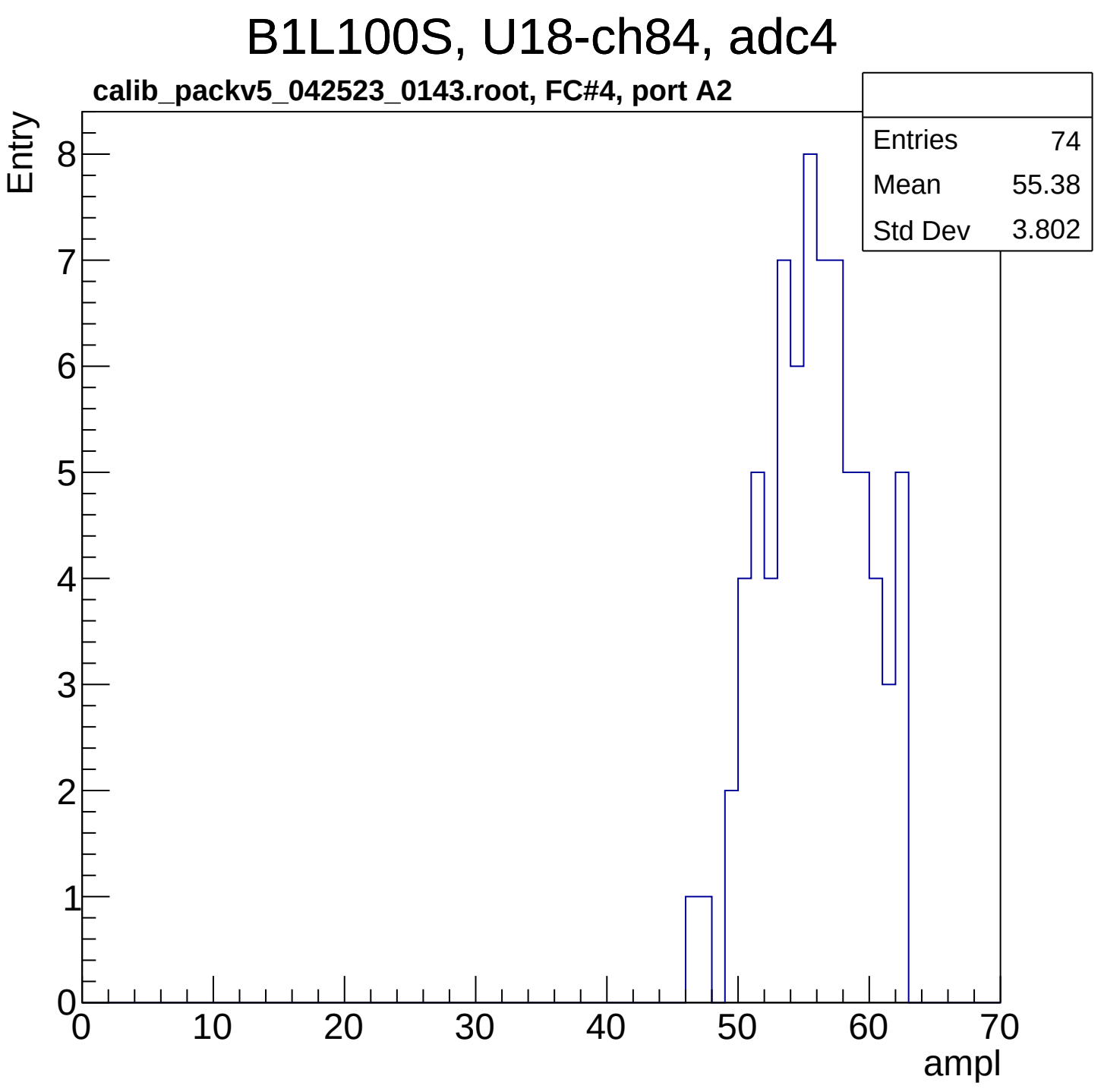

B1L100S, U18-ch83, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

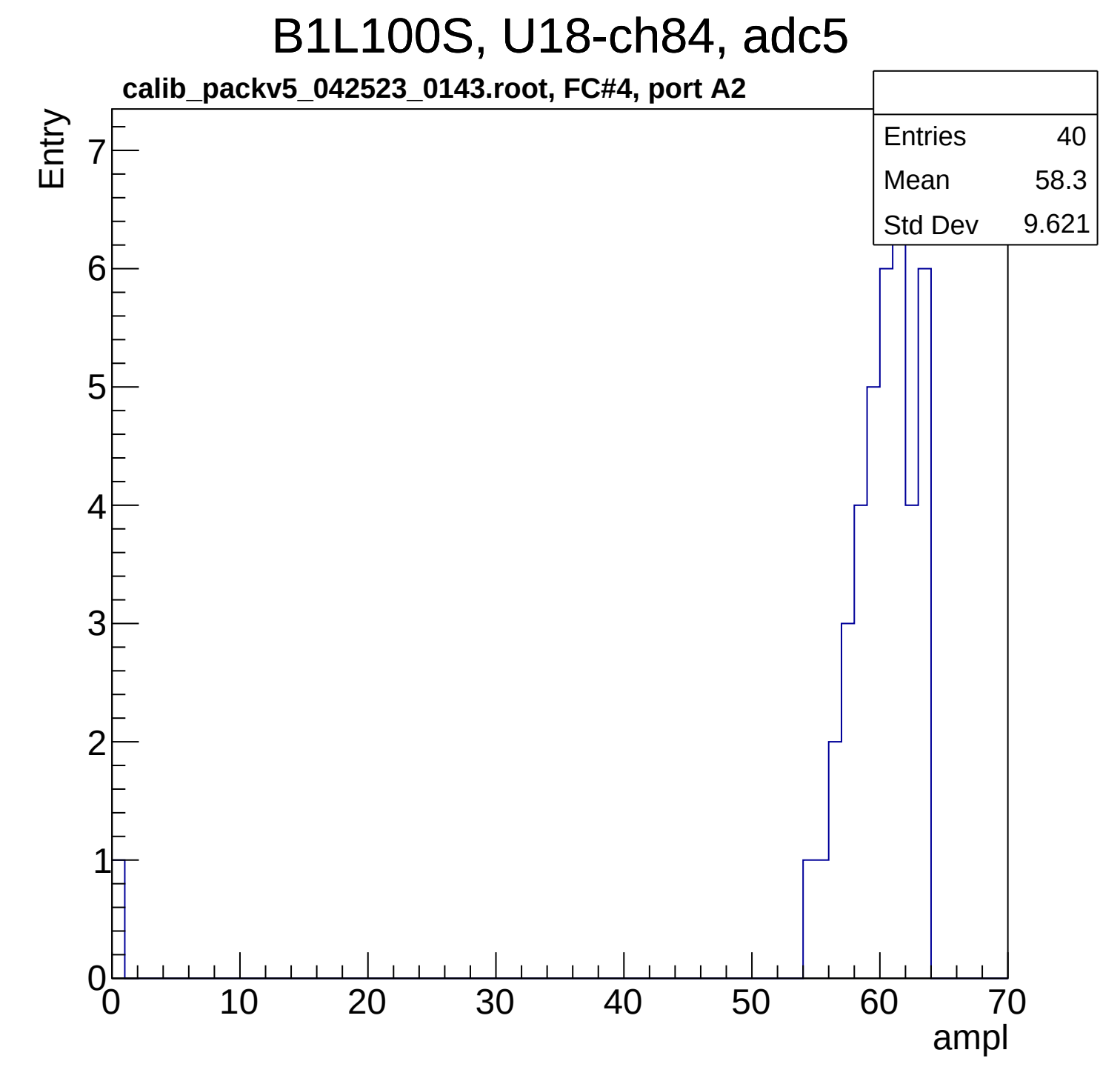

B1L100S, U18-ch84, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 29.52
Std Dev 3.813
Gaus mean : 30.1217
Gaus Width: 4.4759
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

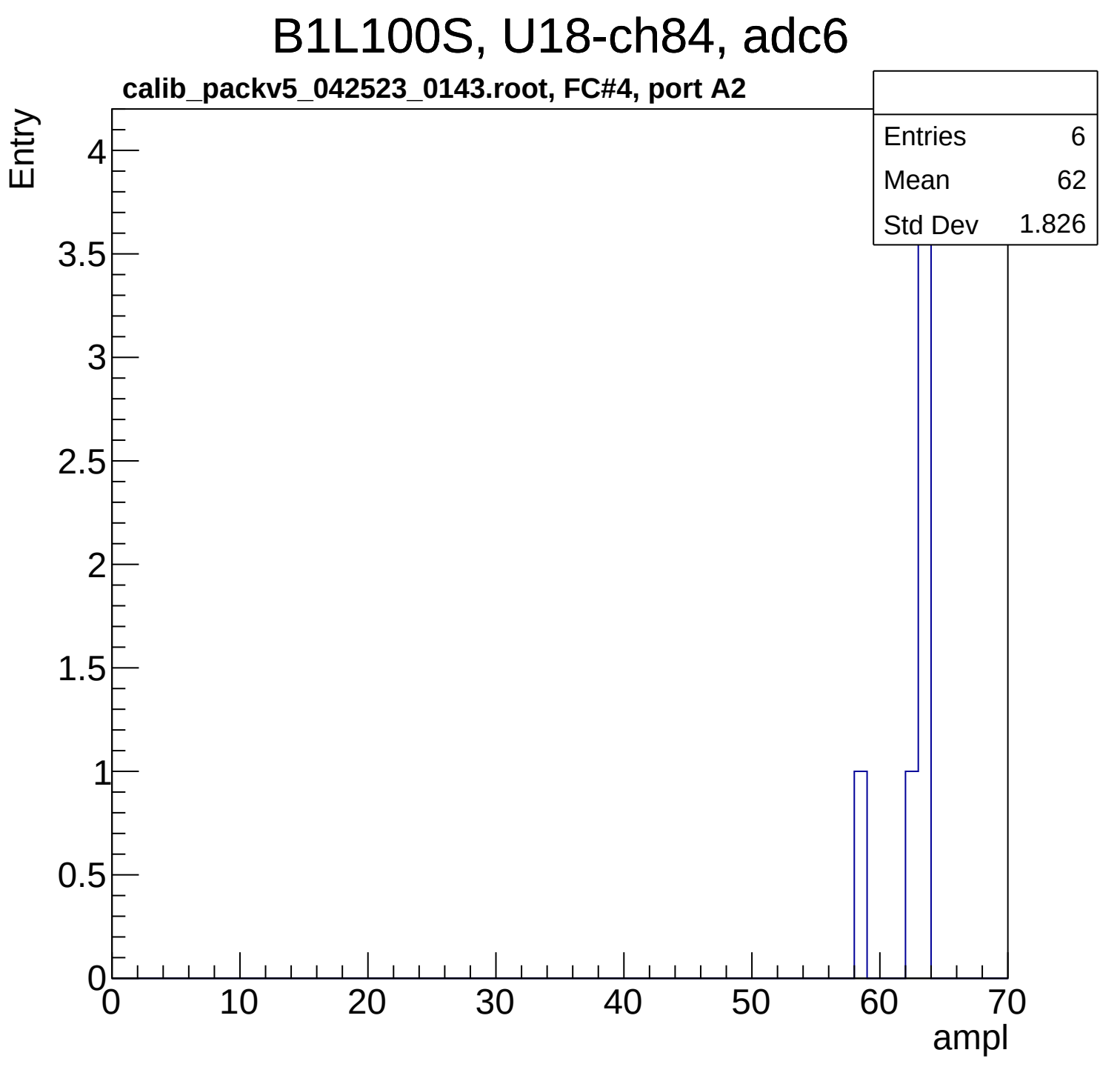

B1L100S, U18-ch84, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 35.43
Std Dev 3.611
Gaus mean : 35.9629
Gaus Width: 4.2179
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

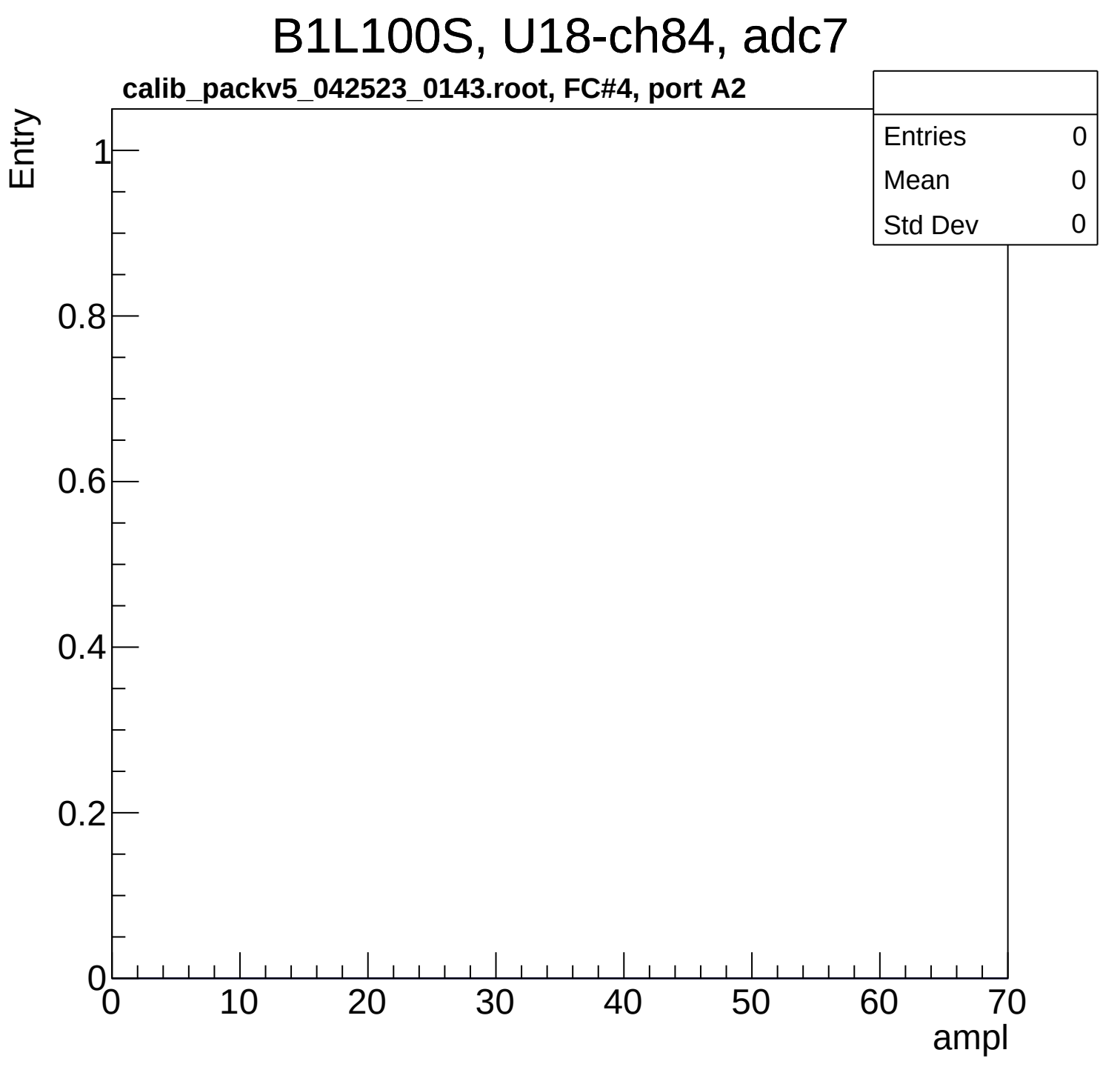

B1L100S, U18-ch84, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 42.67
Std Dev 3.601
Gaus mean : 43.2458
Gaus Width: 3.8729
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

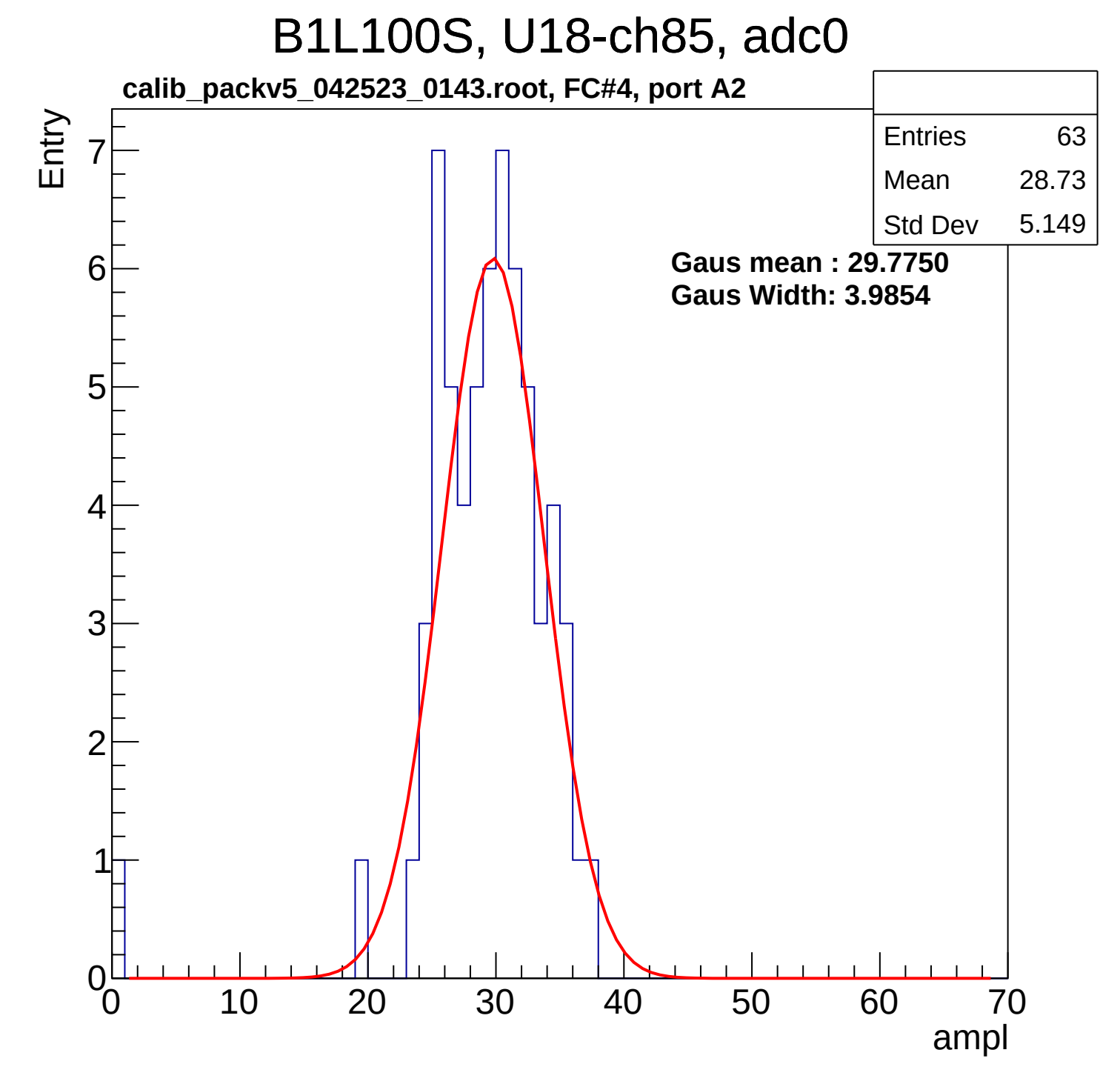

B1L100S, U18-ch84, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 49.33
Std Dev 3.067
Entry
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70
ampl

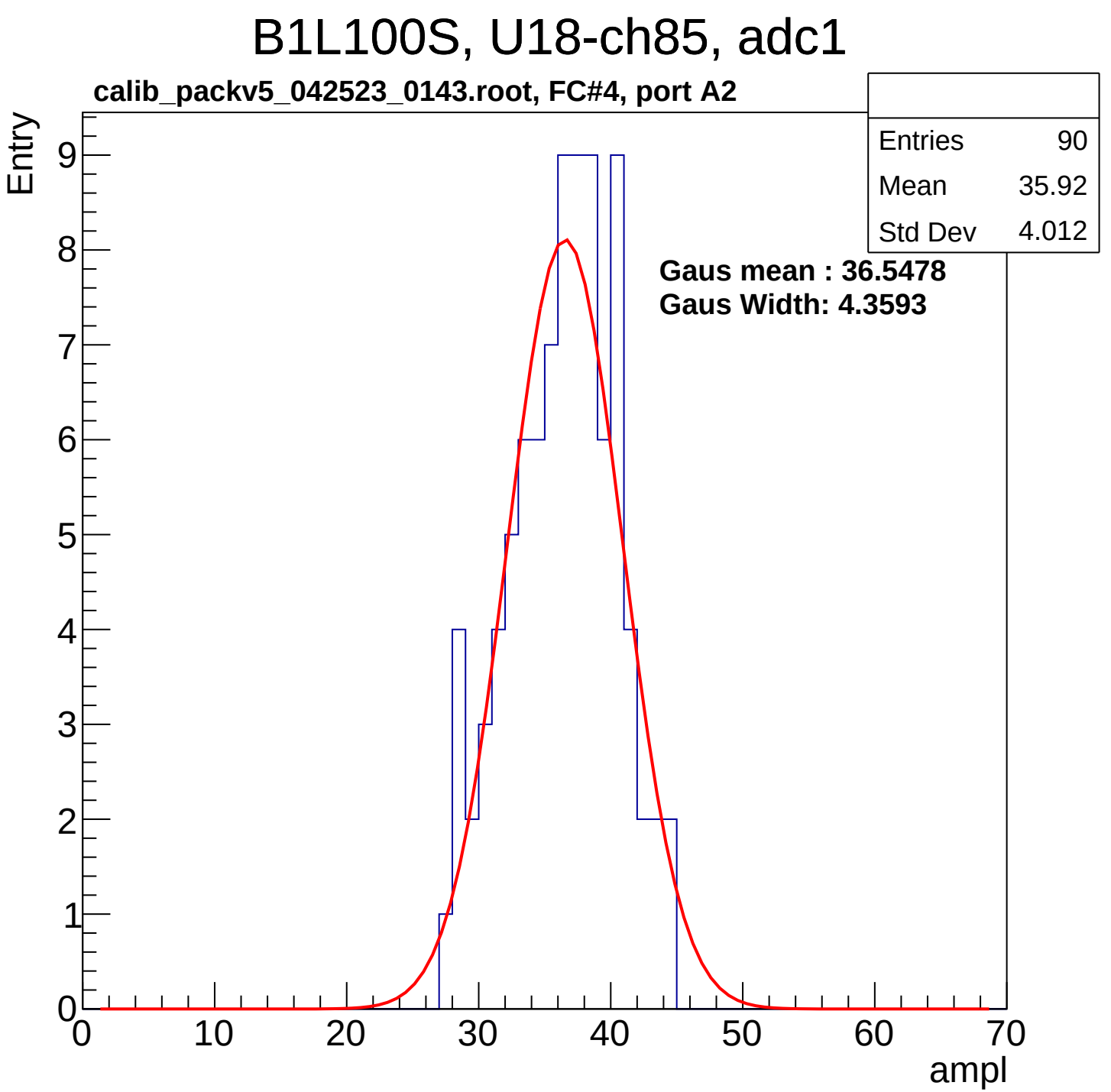

B1L100S, U18-ch84, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 55.38
Std Dev 3.802
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

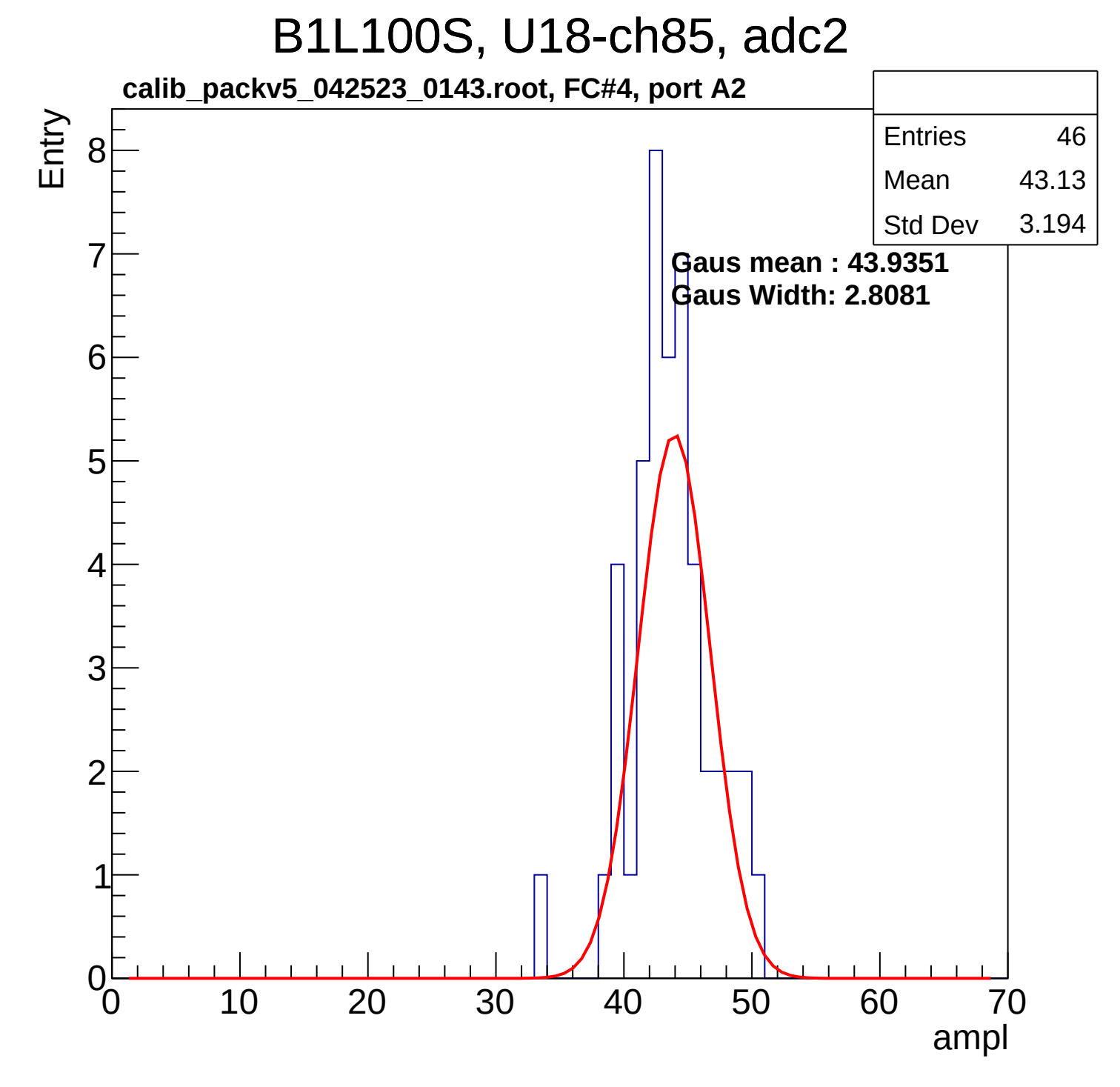

B1L100S, U18-ch84, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 40
Mean 58.3
Std Dev 9.621
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

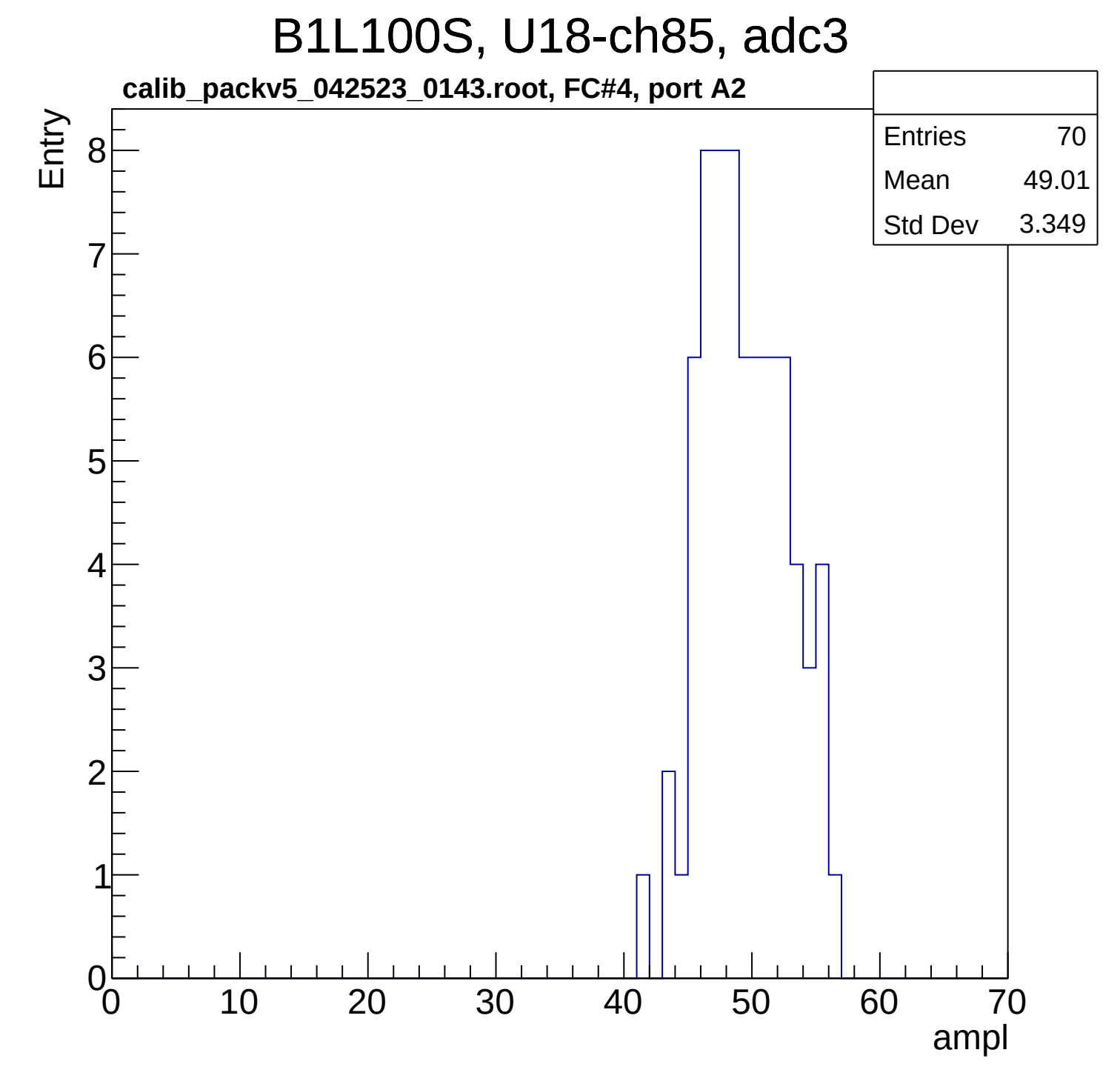

B1L100S, U18-ch84, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 62
Std Dev 1.826
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

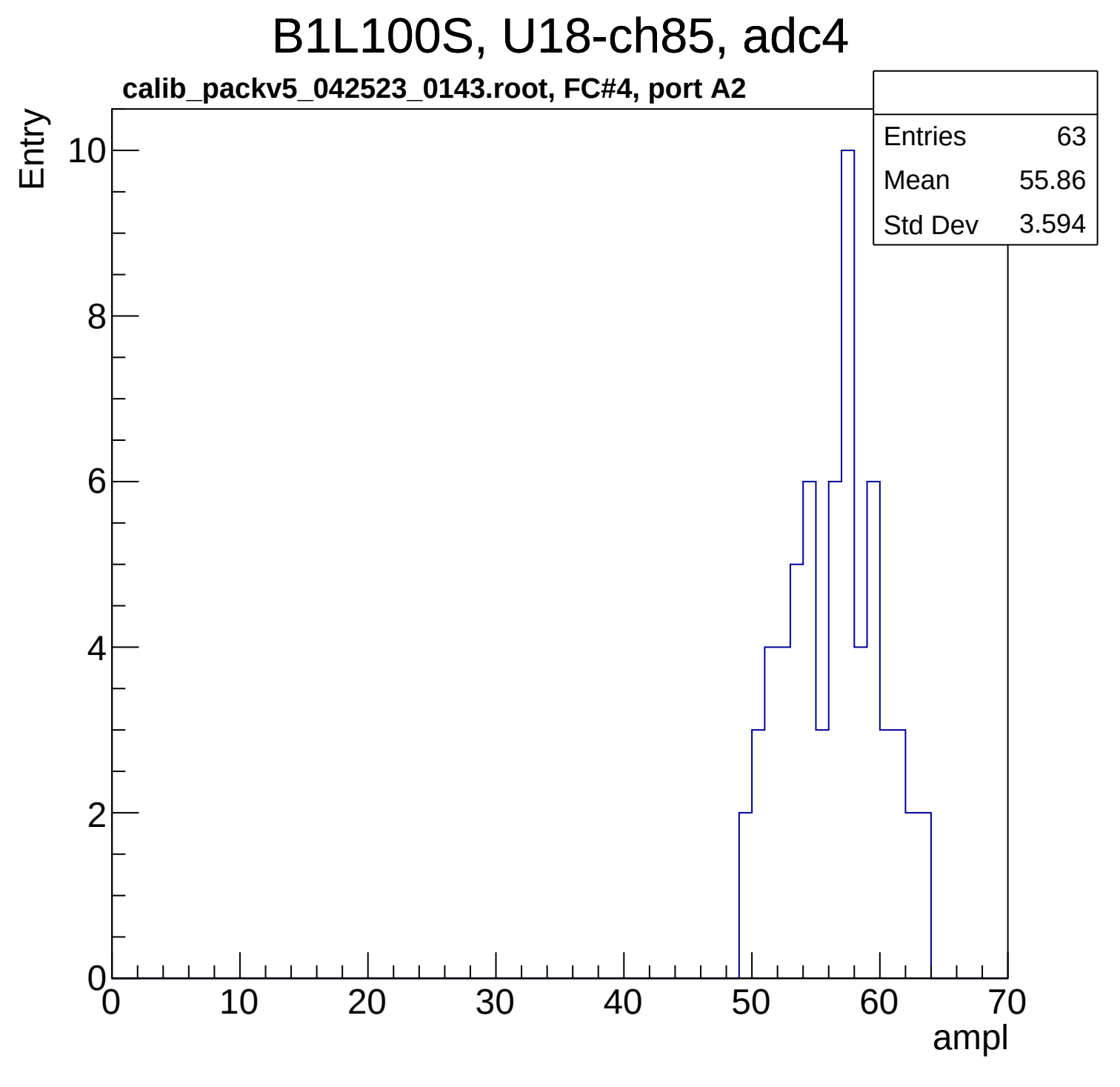

B1L100S, U18-ch84, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

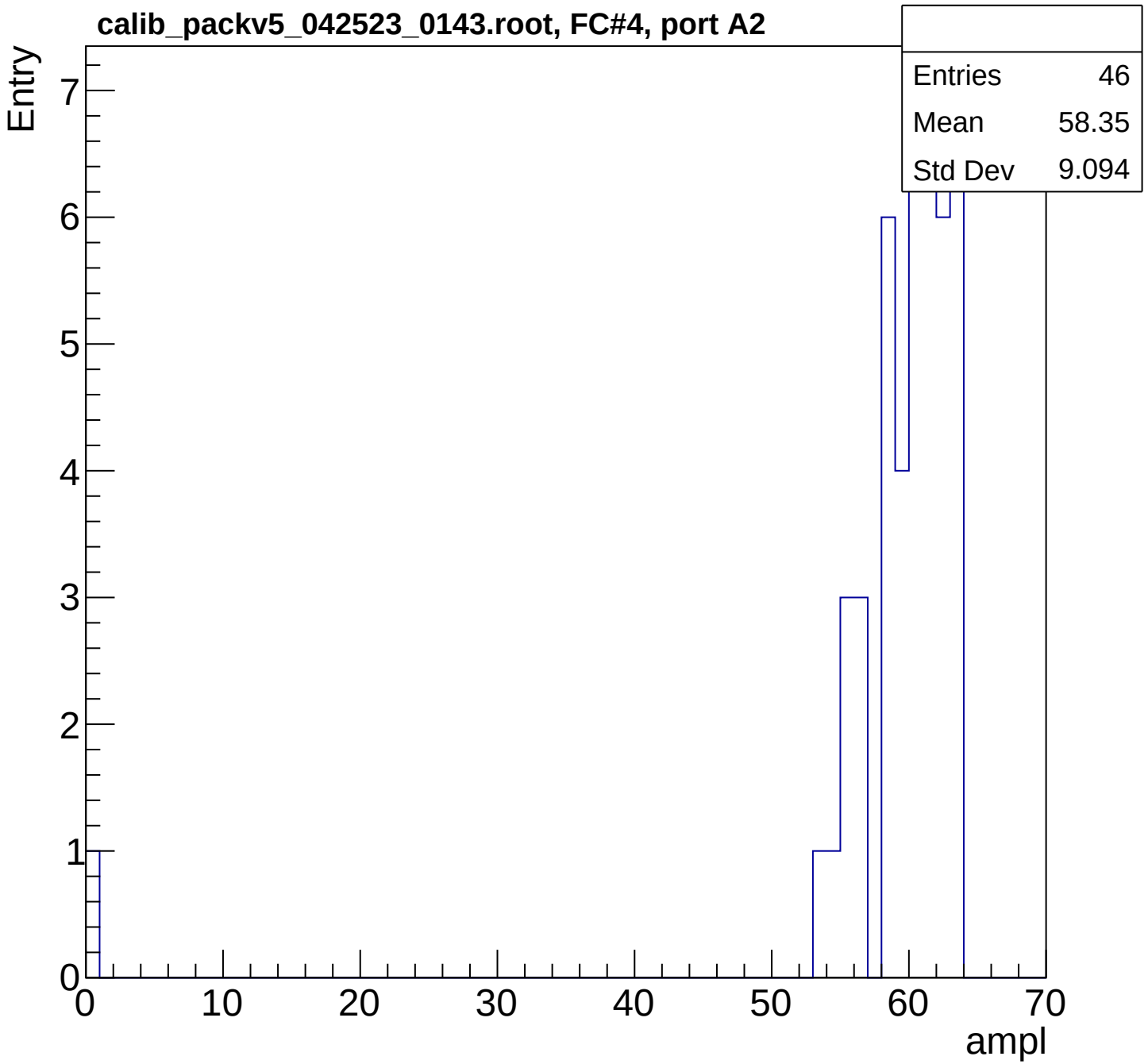

B1L100S, U18-ch85, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 28.73
Std Dev 5.149
Gaus mean : 29.7750
Gaus Width: 3.9854
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

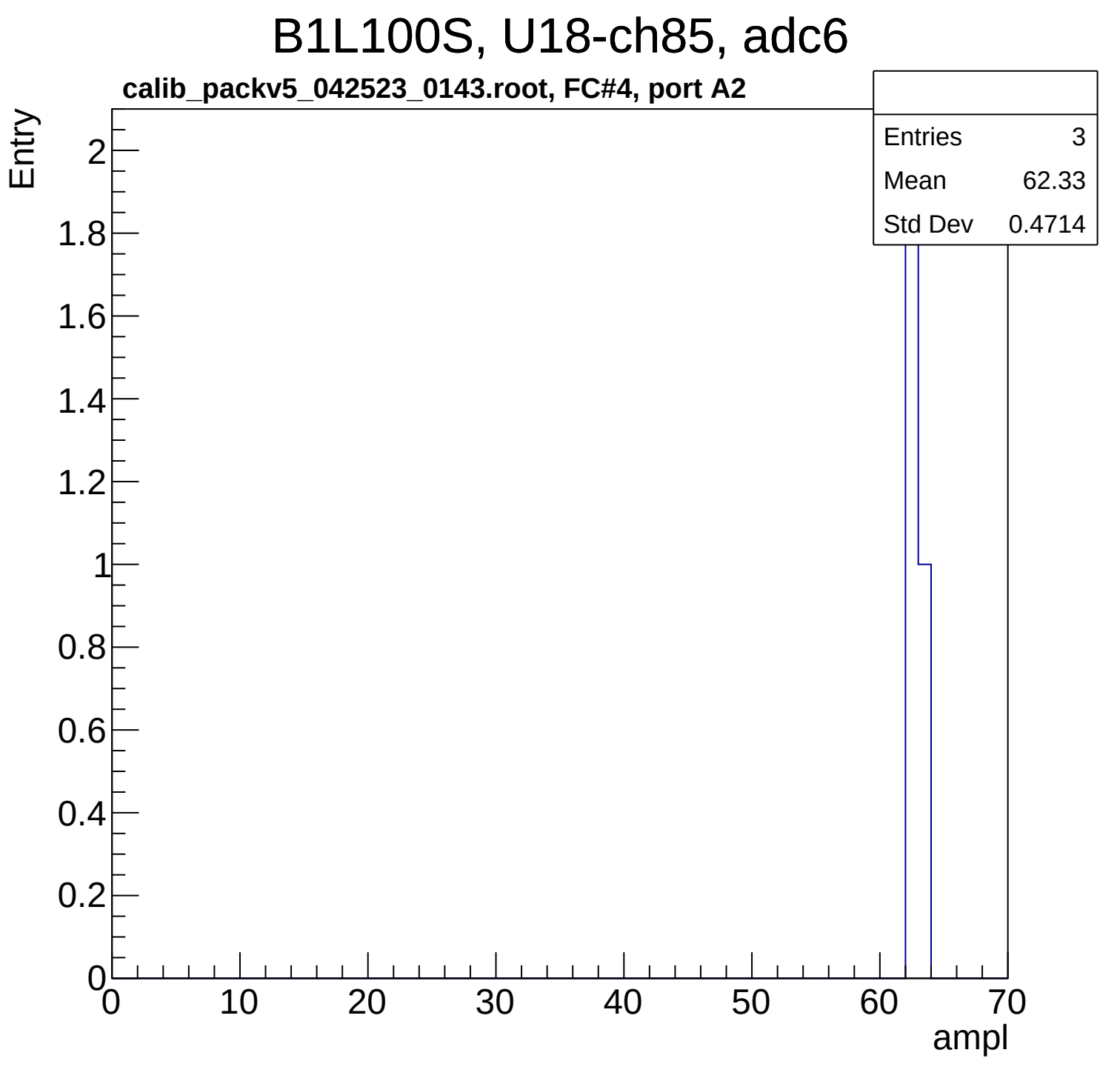

B1L100S, U18-ch85, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 90
Mean 35.92
Std Dev 4.012
Gaus mean : 36.5478
Gaus Width: 4.3593
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

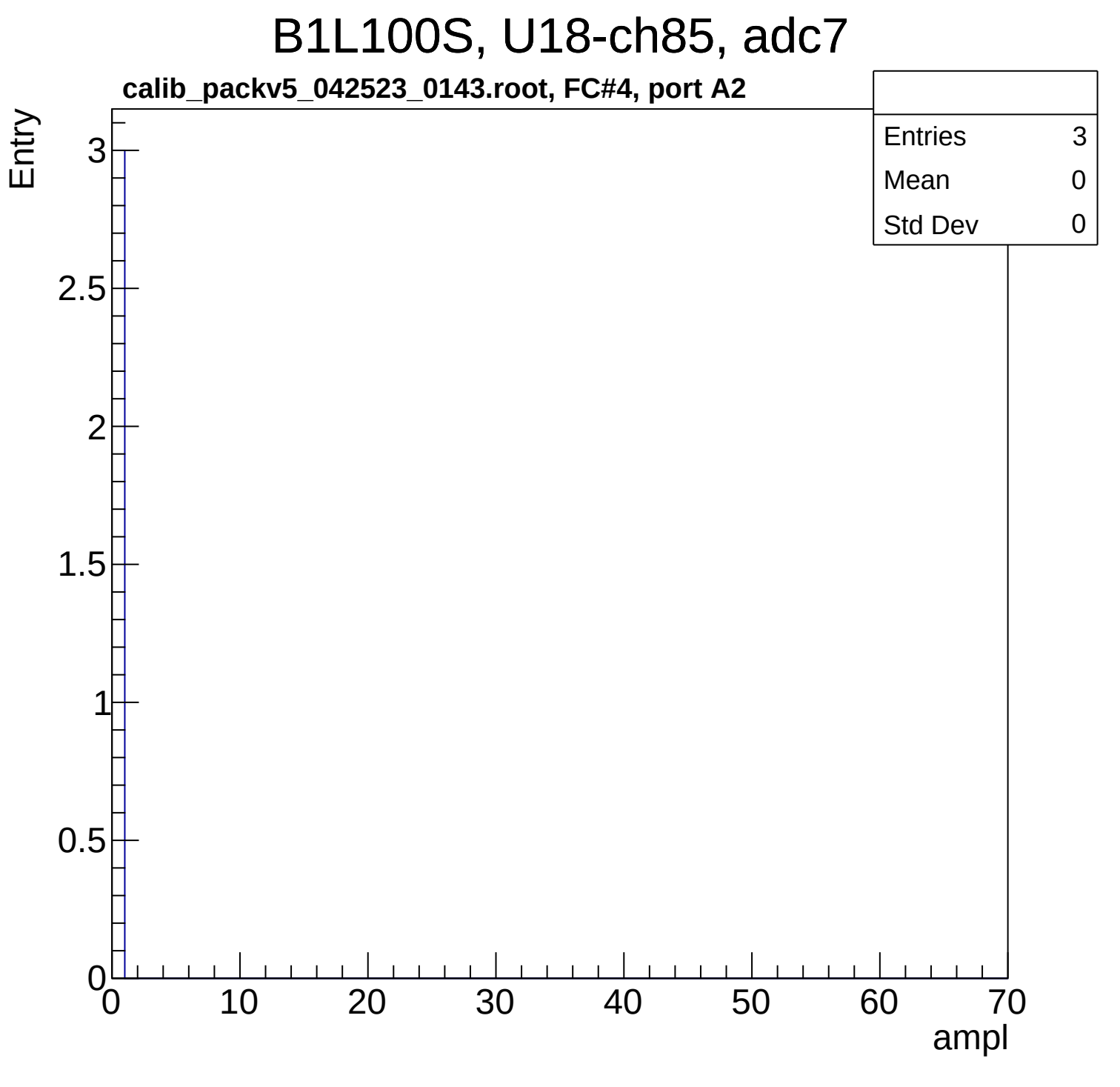

B1L100S, U18-ch85, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 43.13
Std Dev 3.194
Gaus mean : 43.9351
Gaus Width: 2.8081
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

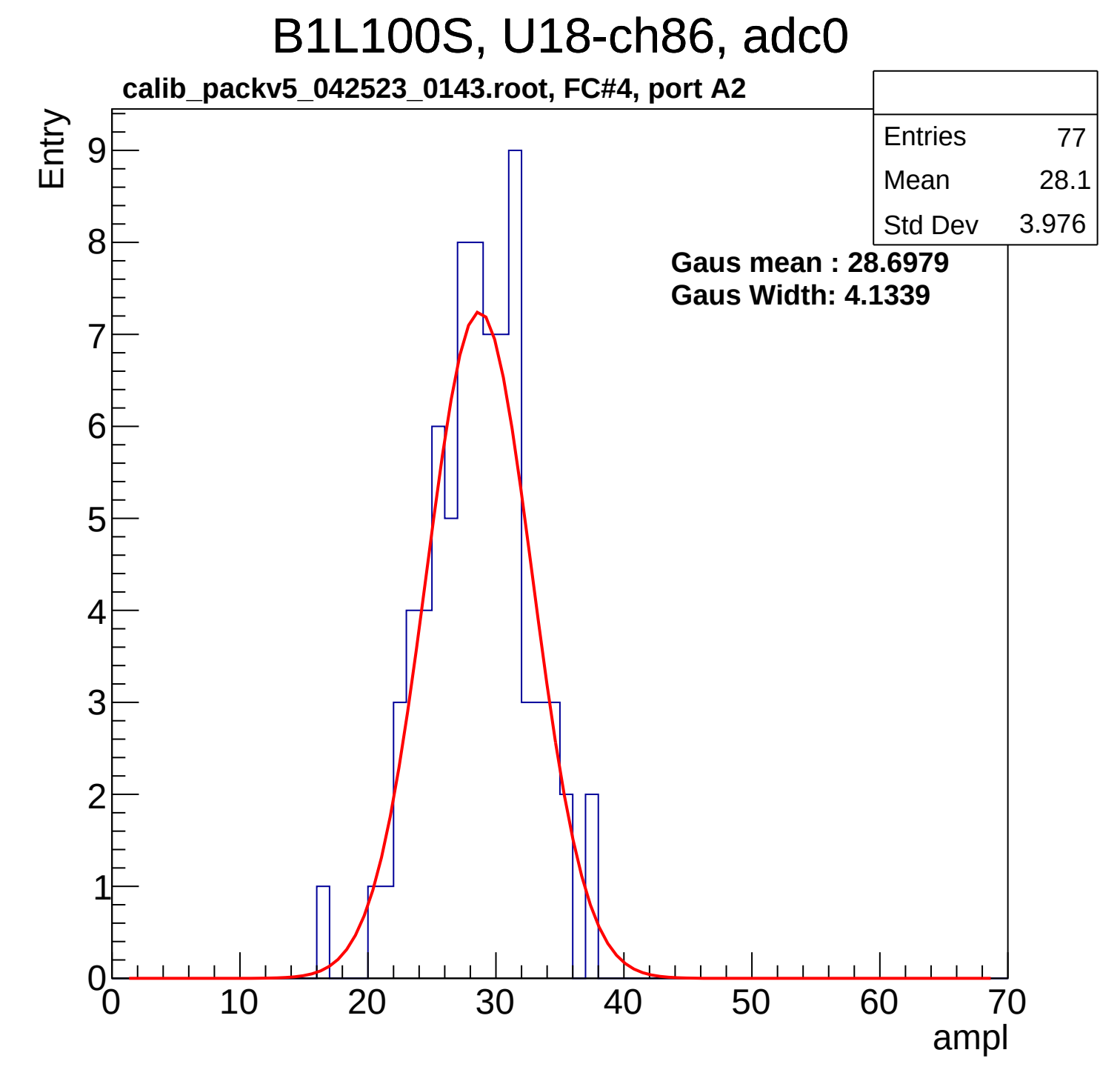

B1L100S, U18-ch85, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 49.01
Std Dev 3.349
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

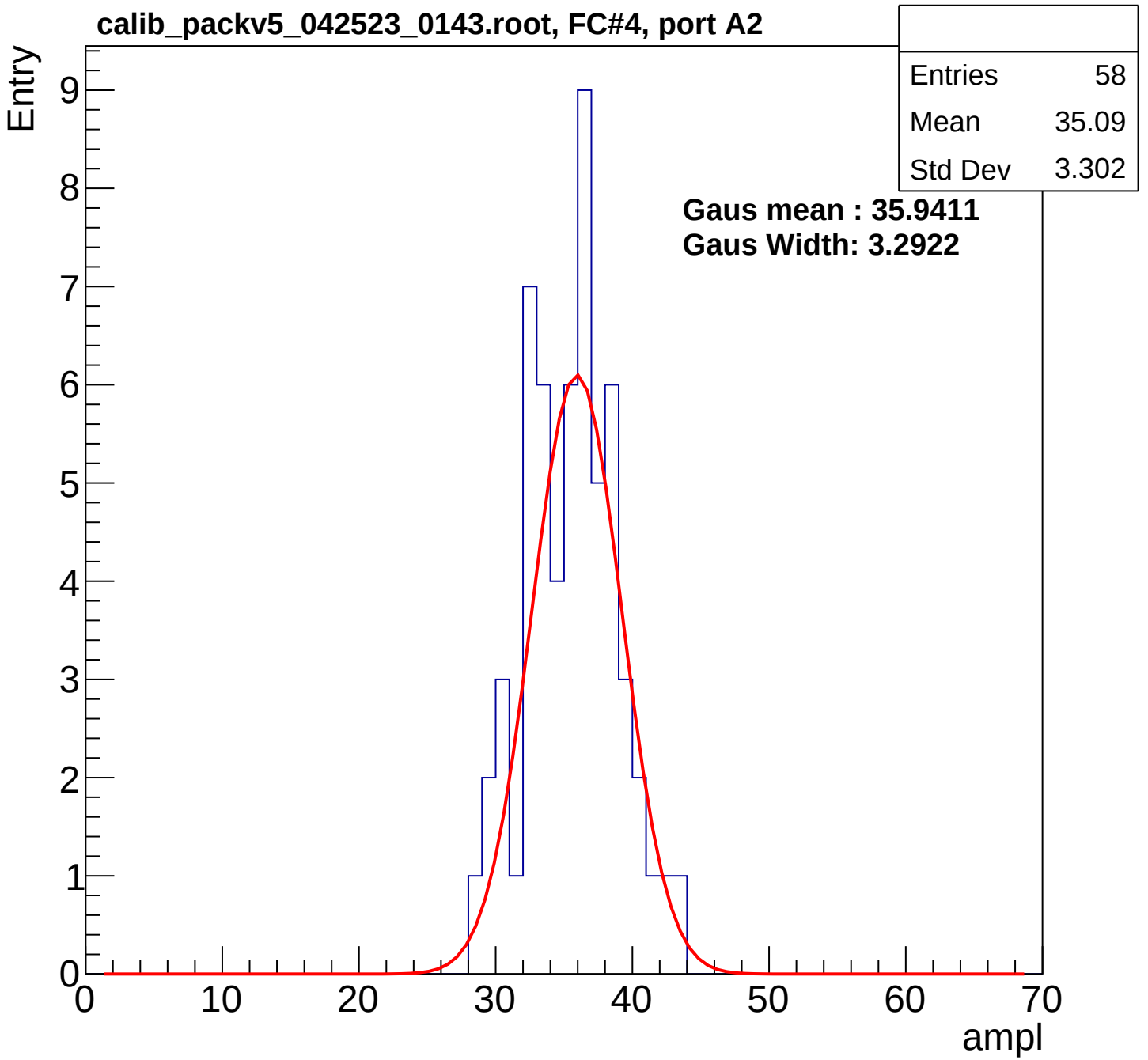

B1L100S, U18-ch85, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 55.86
Std Dev 3.594
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

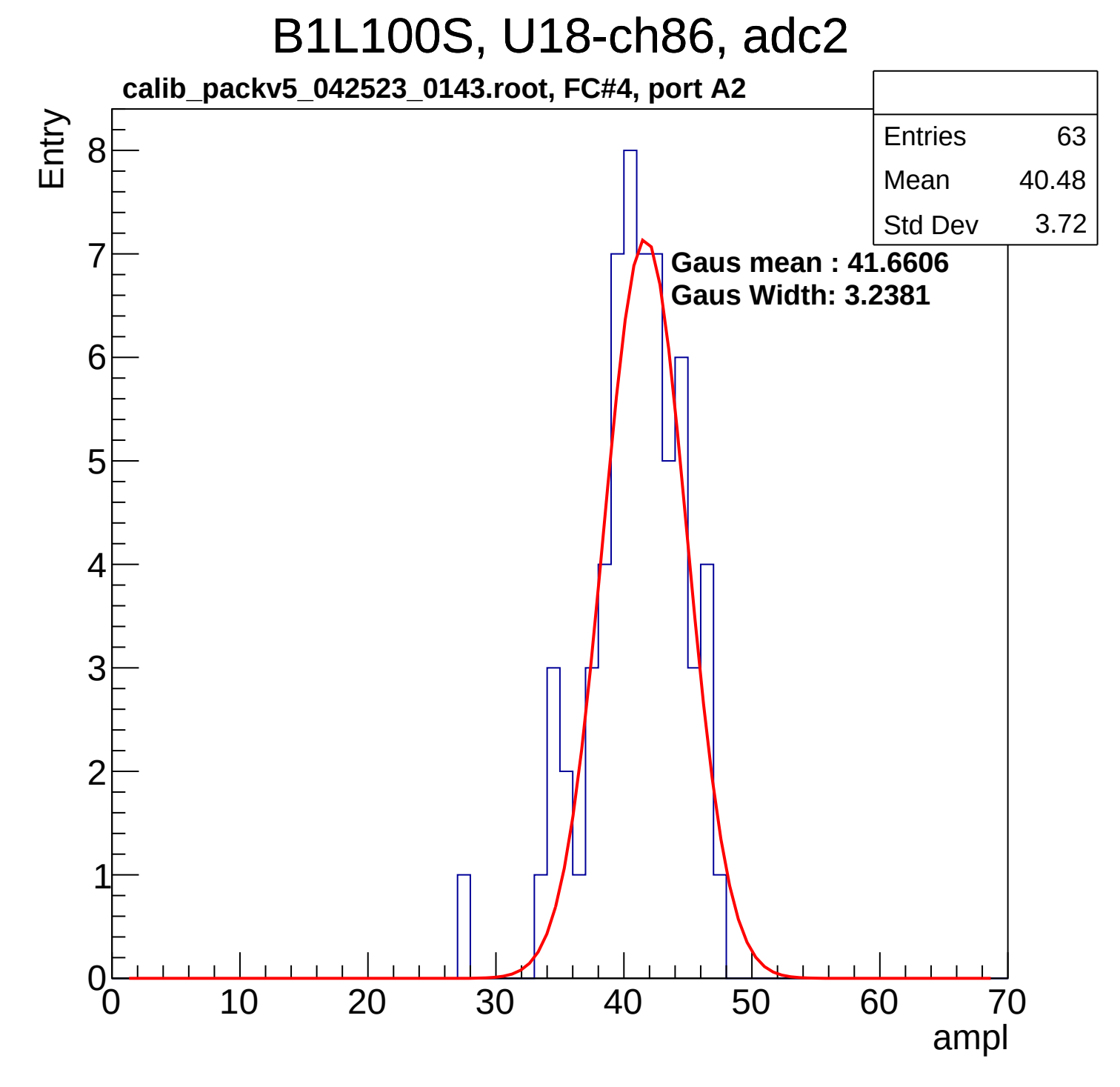

B1L100S, U18-ch85, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 58.35
Std Dev 9.094
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

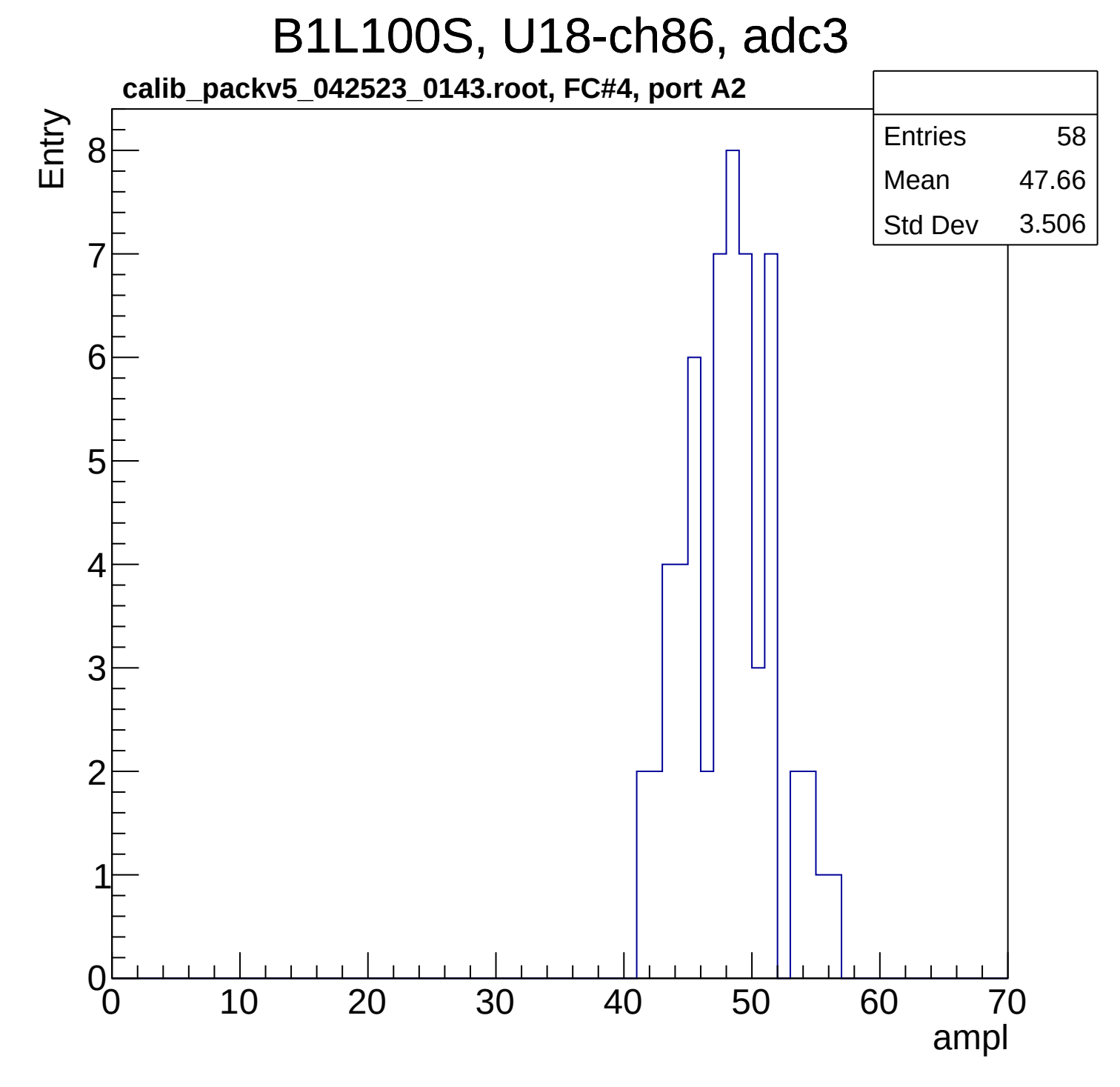

B1L100S, U18-ch85, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

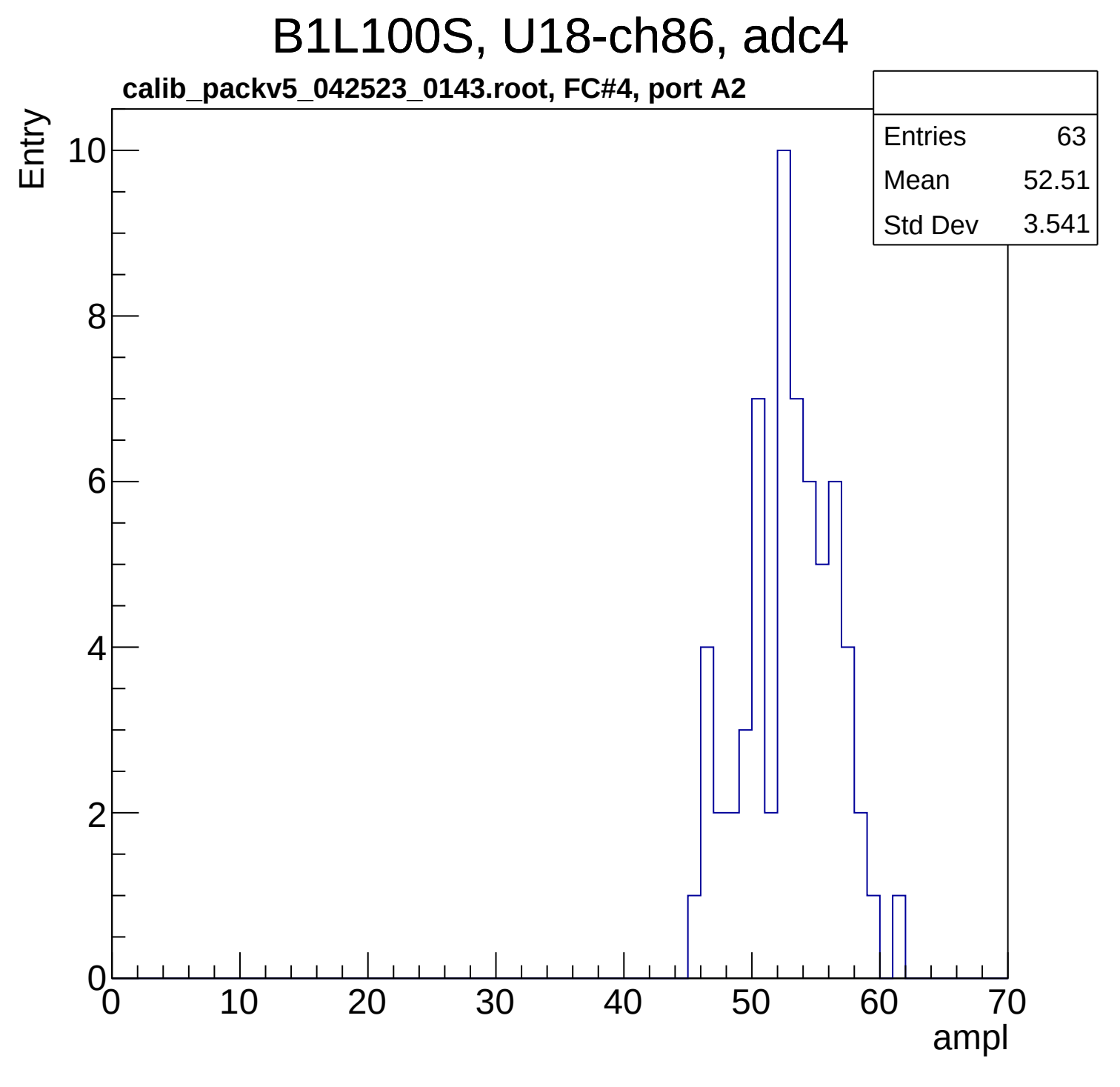

B1L100S, U18-ch85, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 0
Std Dev 0
Entry
3
2.5
2
1.5
1
0.5
0
0
10
20
30
40
50
60
70
ampl

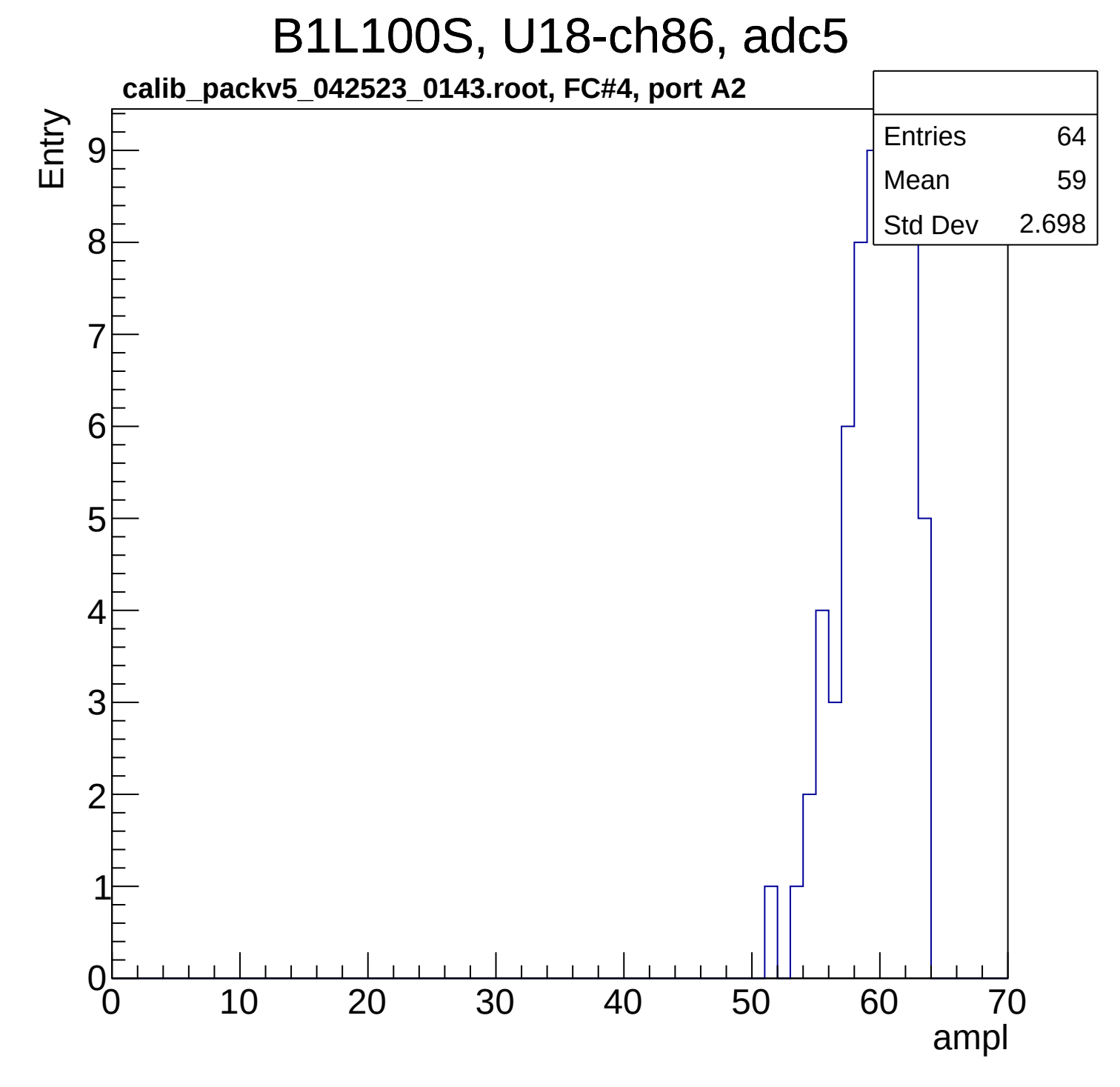

B1L100S, U18-ch86, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 28.1
Std Dev 3.976
Gaus mean : 28.6979
Gaus Width: 4.1339
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

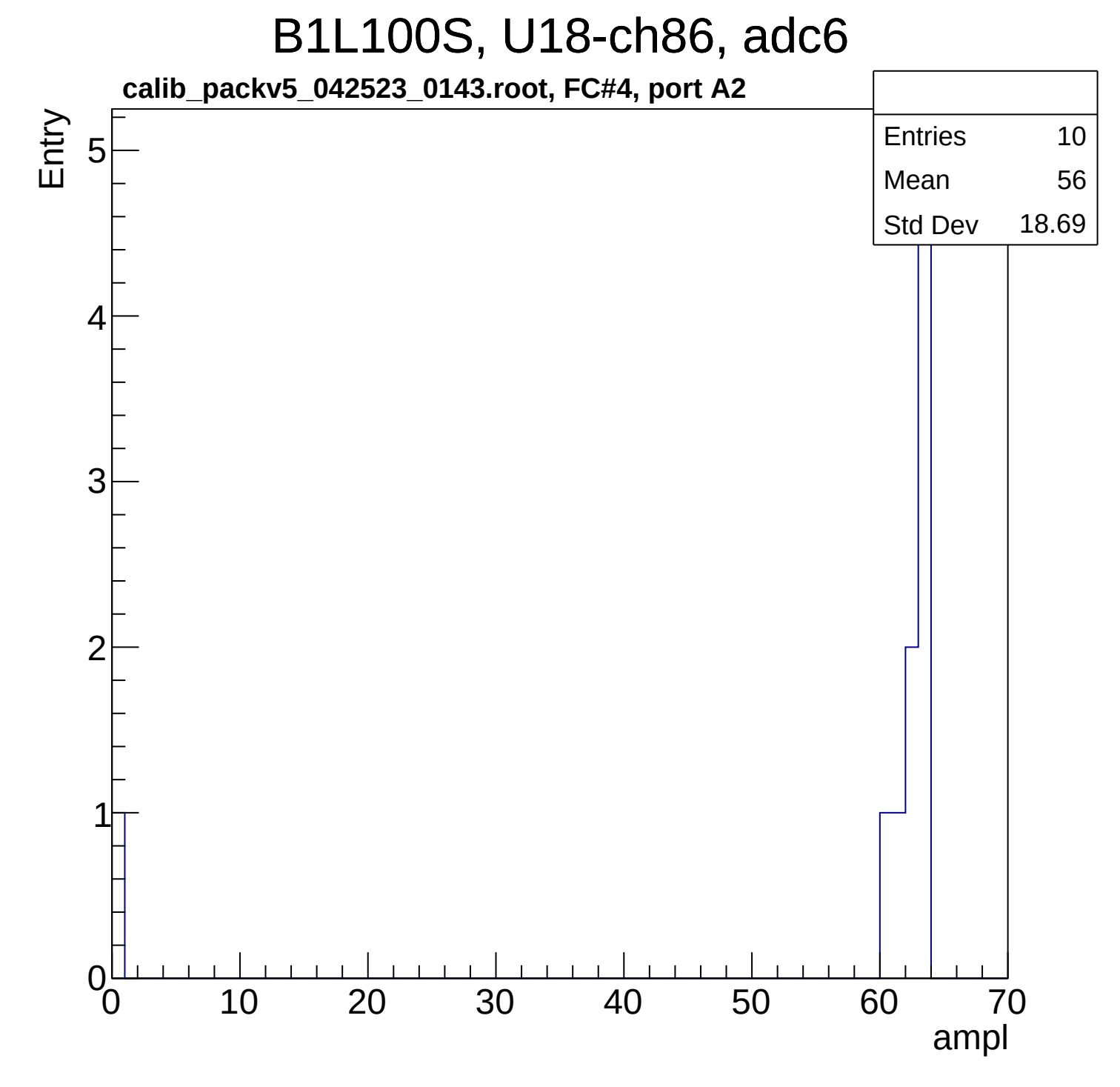

B1L100S, U18-ch86, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 35.09
Std Dev 3.302
Gaus mean : 35.9411
Gaus Width: 3.2922
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

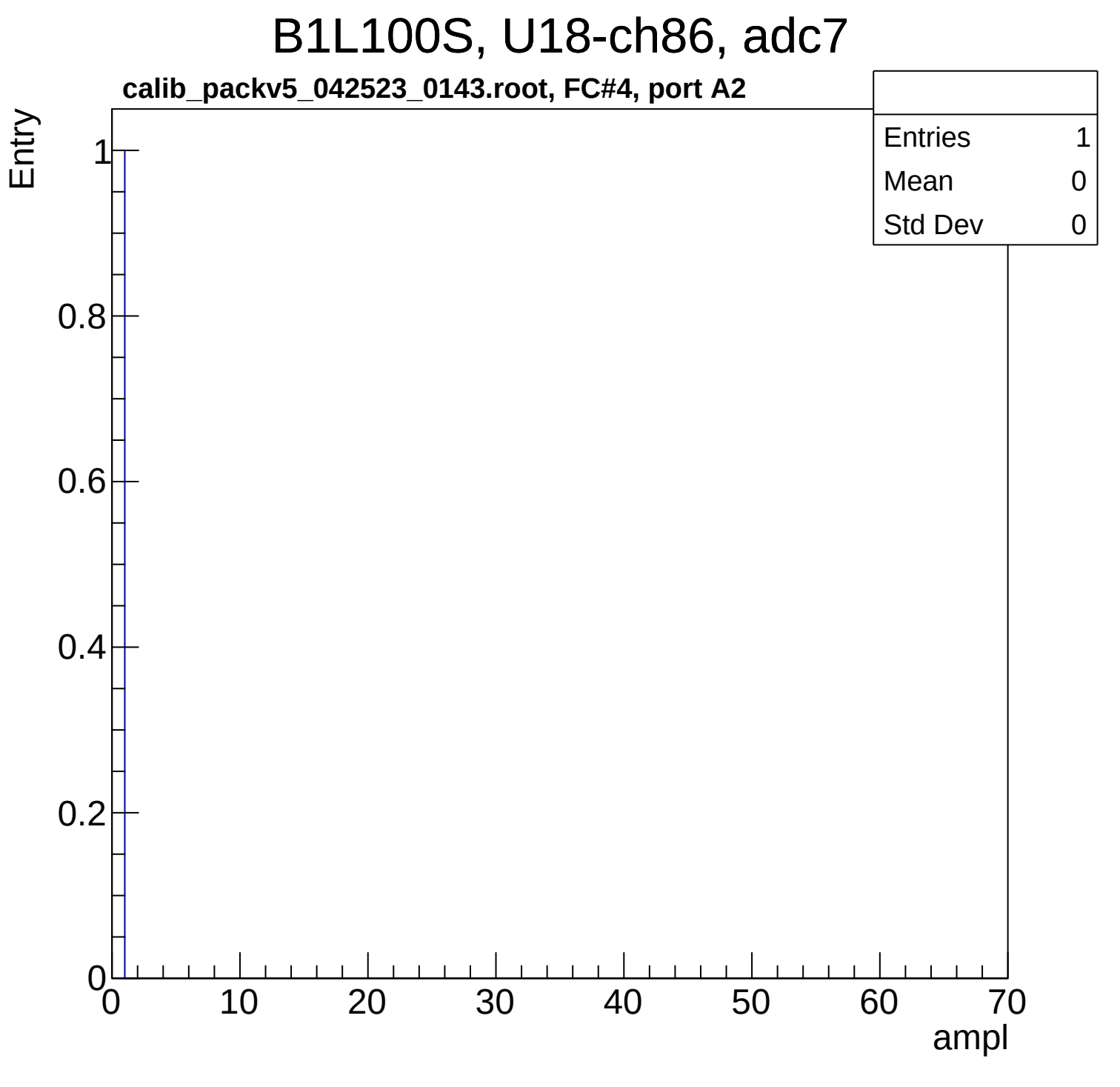

B1L100S, U18-ch86, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 40.48
Std Dev 3.72
Gaus mean : 41.6606
Gaus Width: 3.2381
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

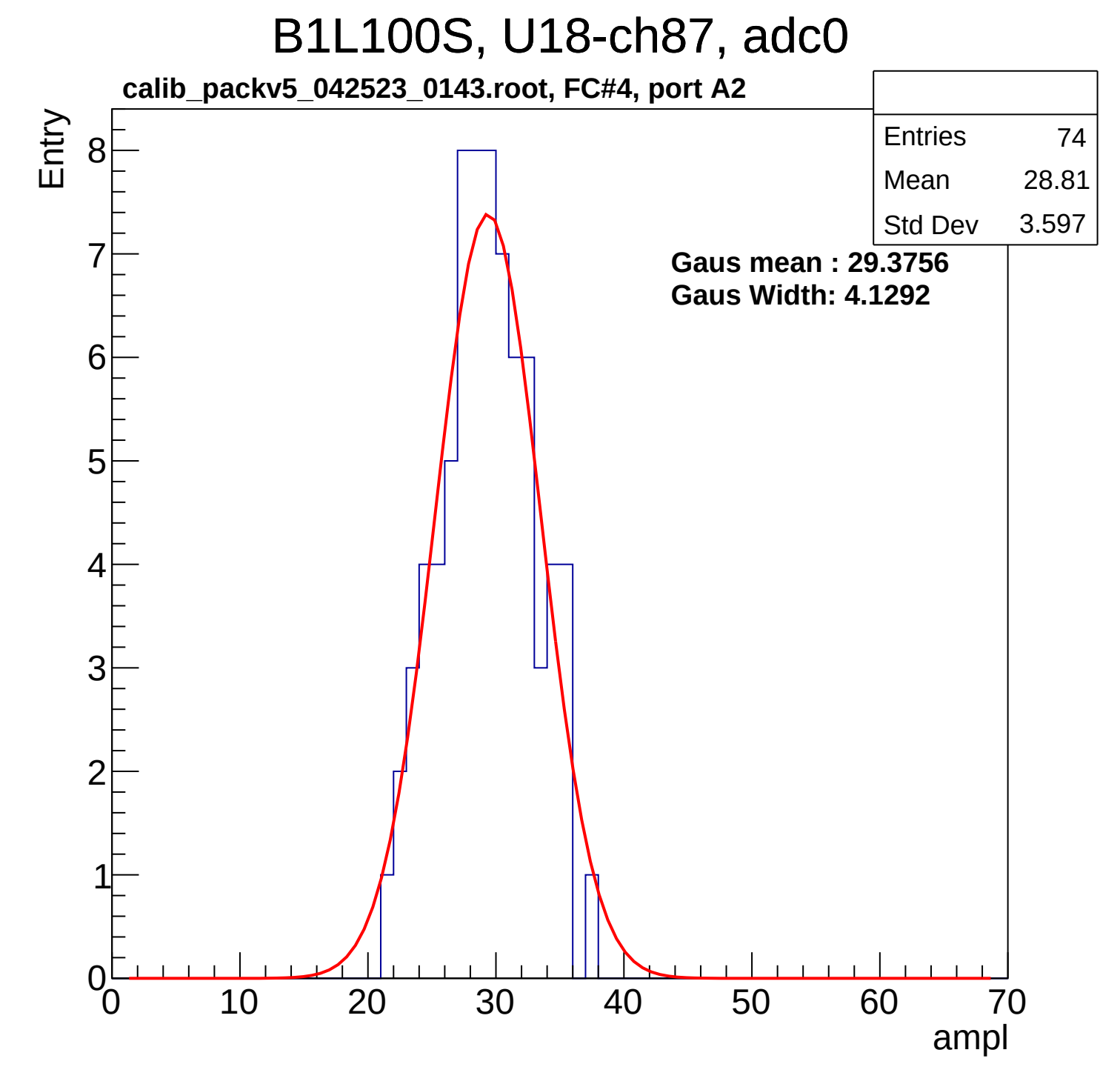

B1L100S, U18-ch86, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 47.66
Std Dev 3.506
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

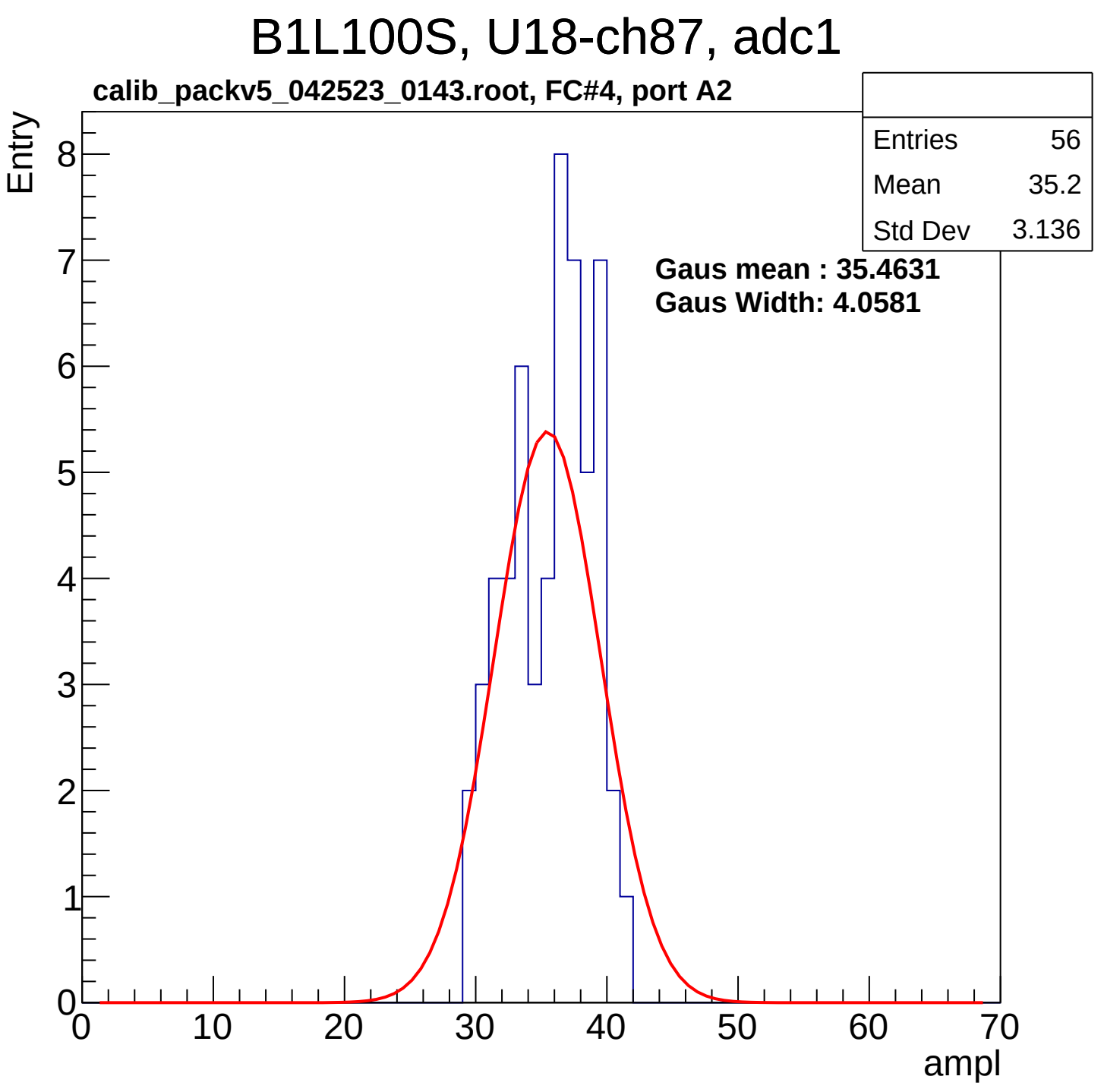

B1L100S, U18-ch86, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 52.51
Std Dev 3.541
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

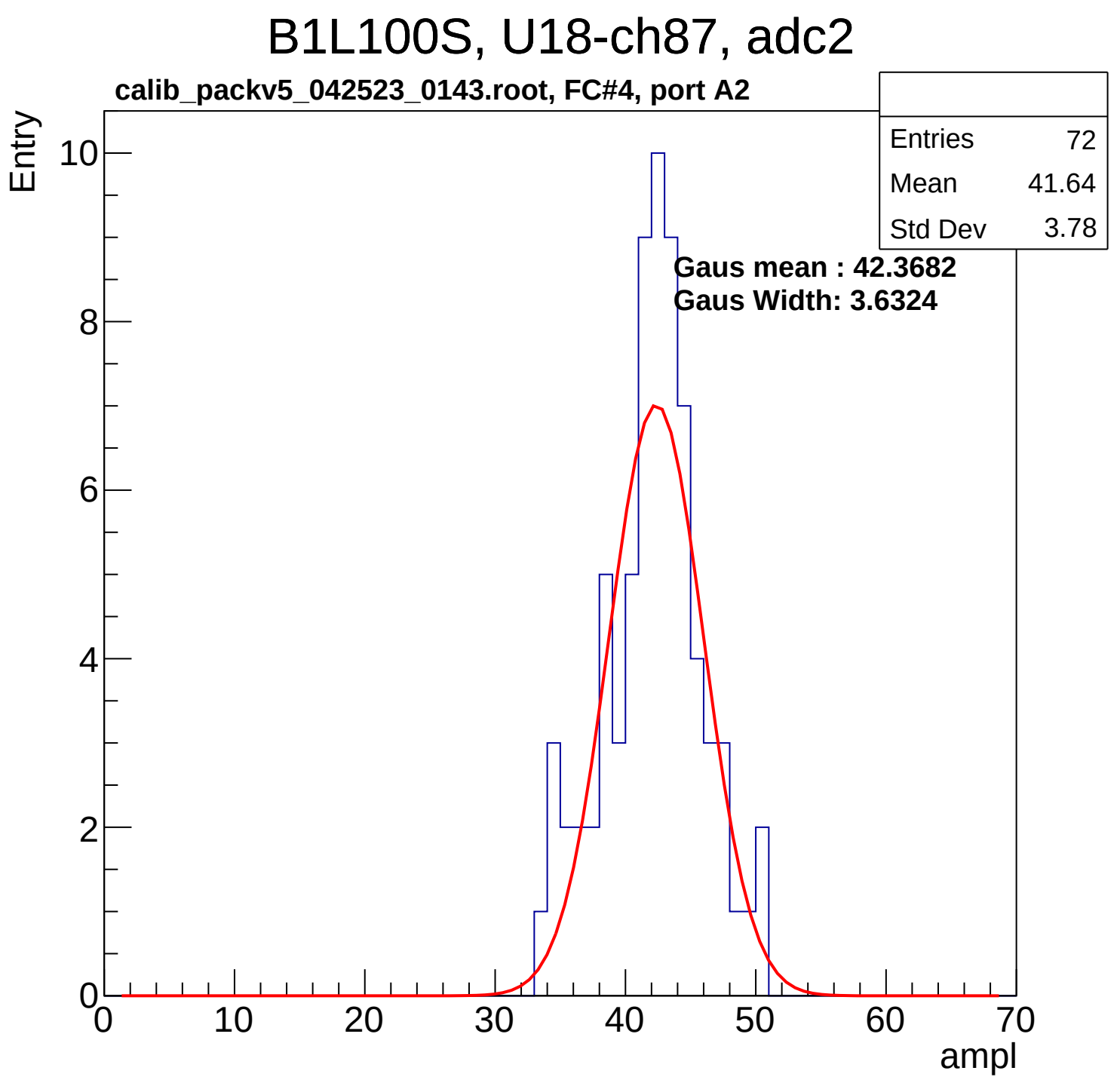

B1L100S, U18-ch86, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 59
Std Dev 2.698
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

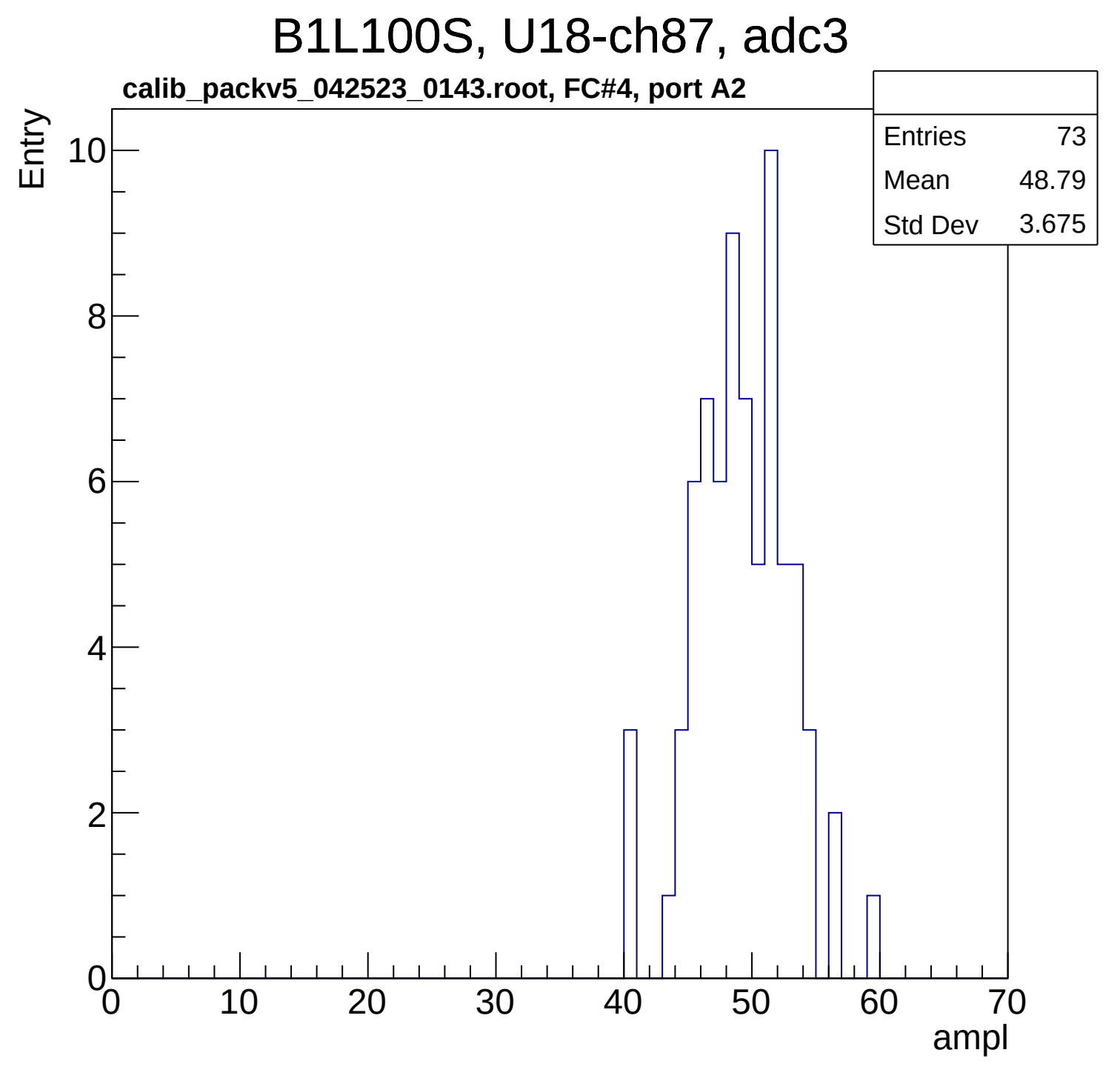

B1L100S, U18-ch86, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 56
Std Dev 18.69
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

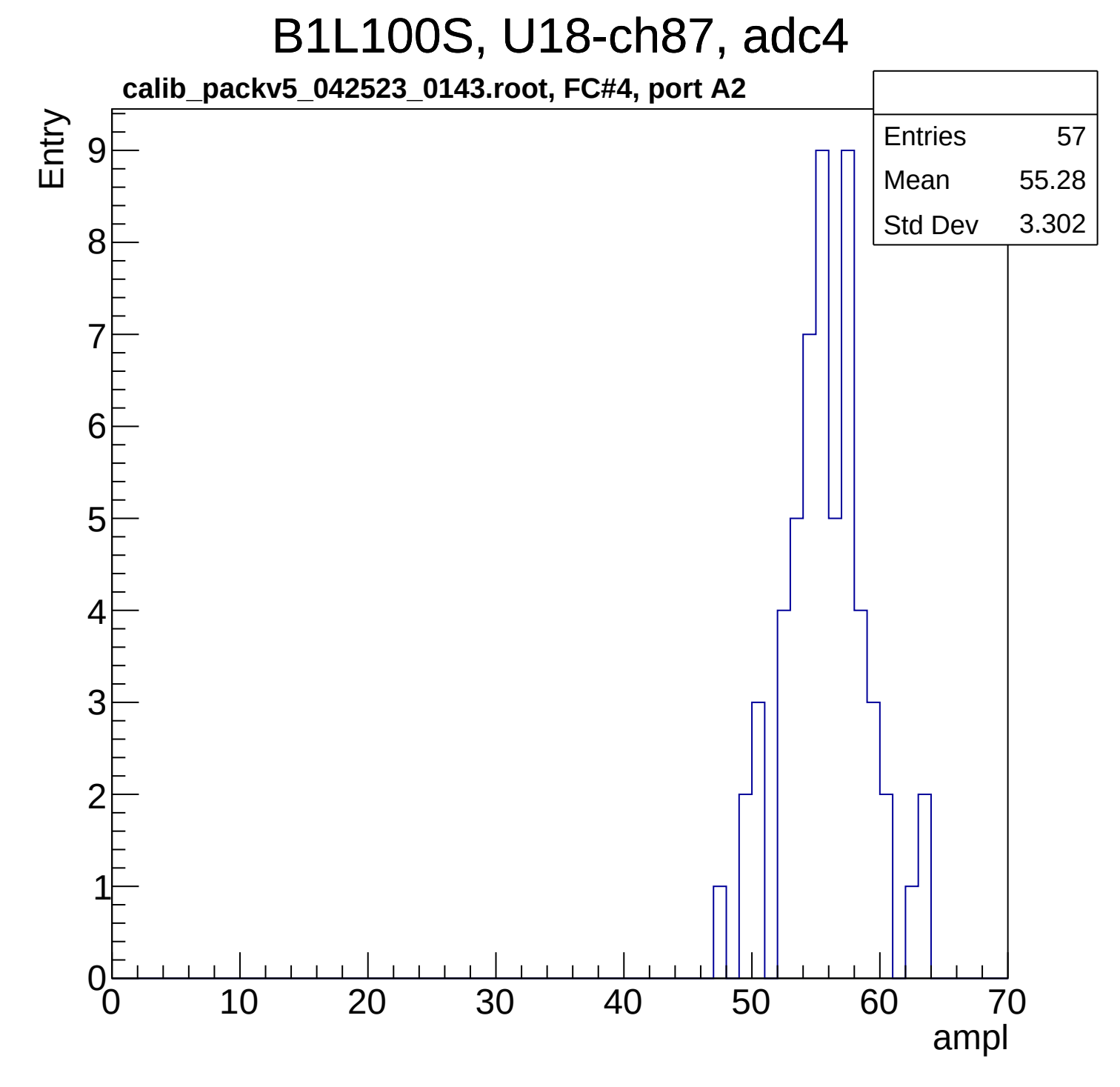

B1L100S, U18-ch86, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

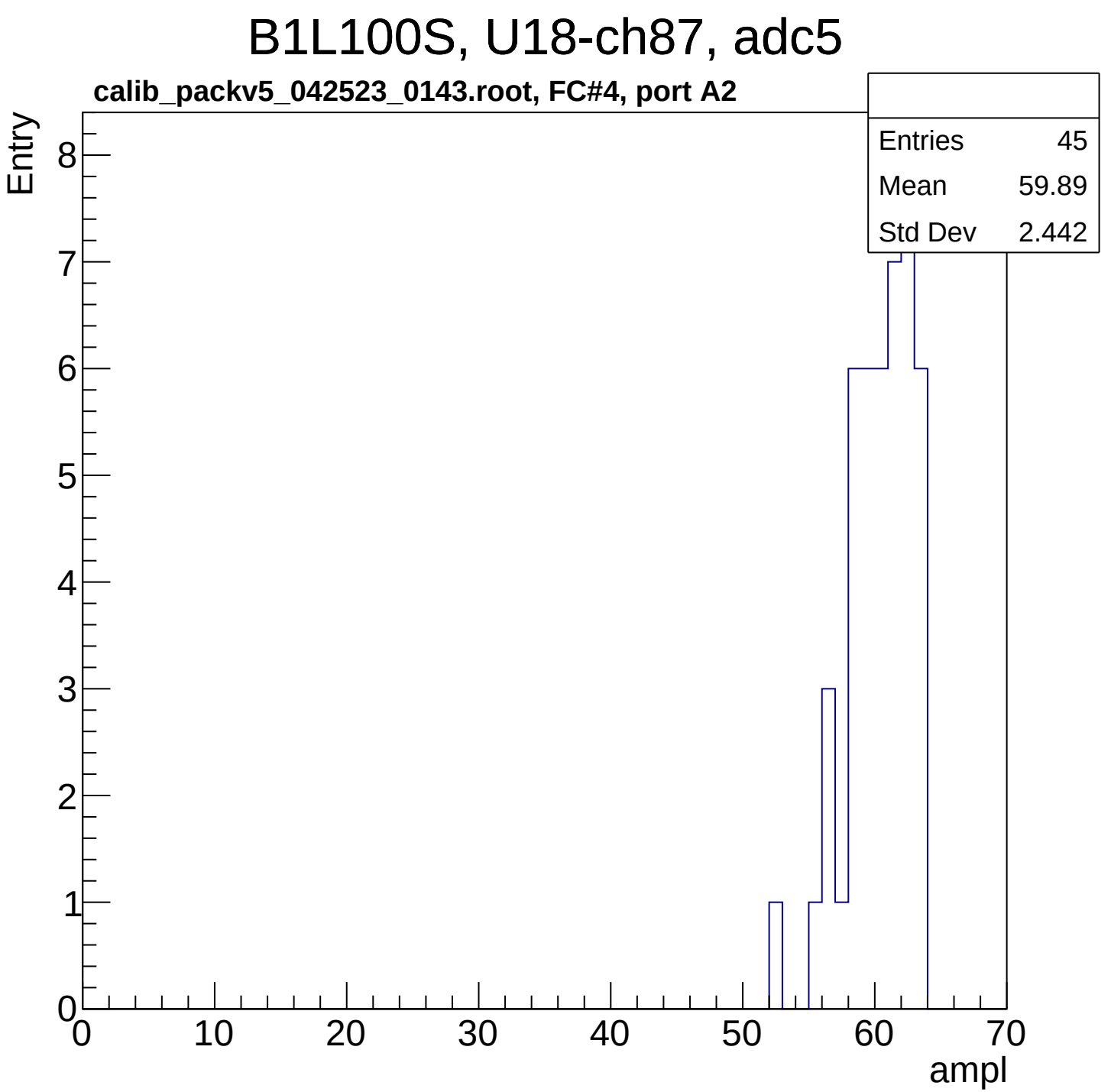

B1L100S, U18-ch87, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 28.81
Std Dev 3.597
Gaus mean : 29.3756
Gaus Width: 4.1292
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

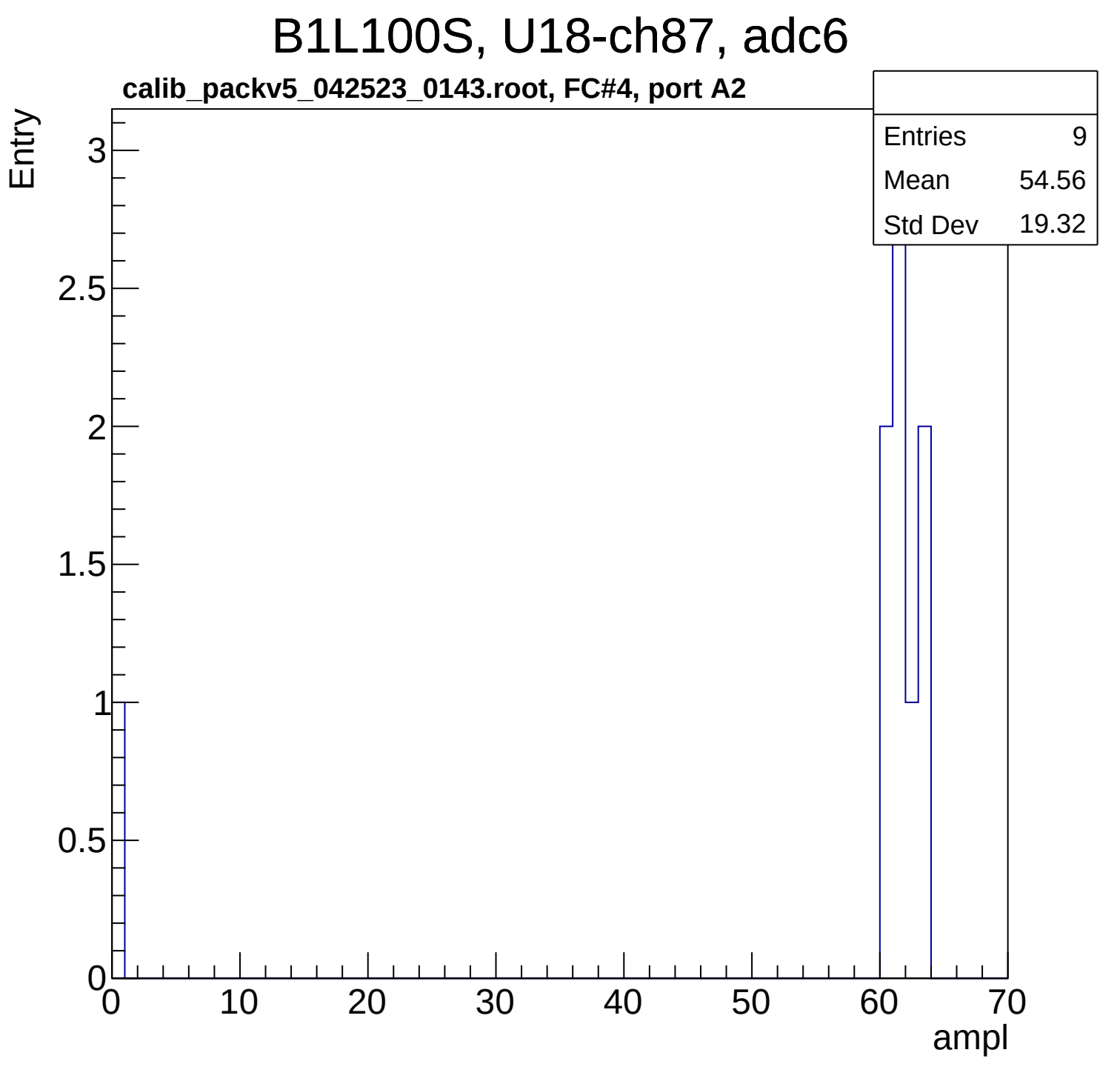

B1L100S, U18-ch87, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 35.2
Std Dev 3.136
Gaus mean : 35.4631
Gaus Width: 4.0581
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

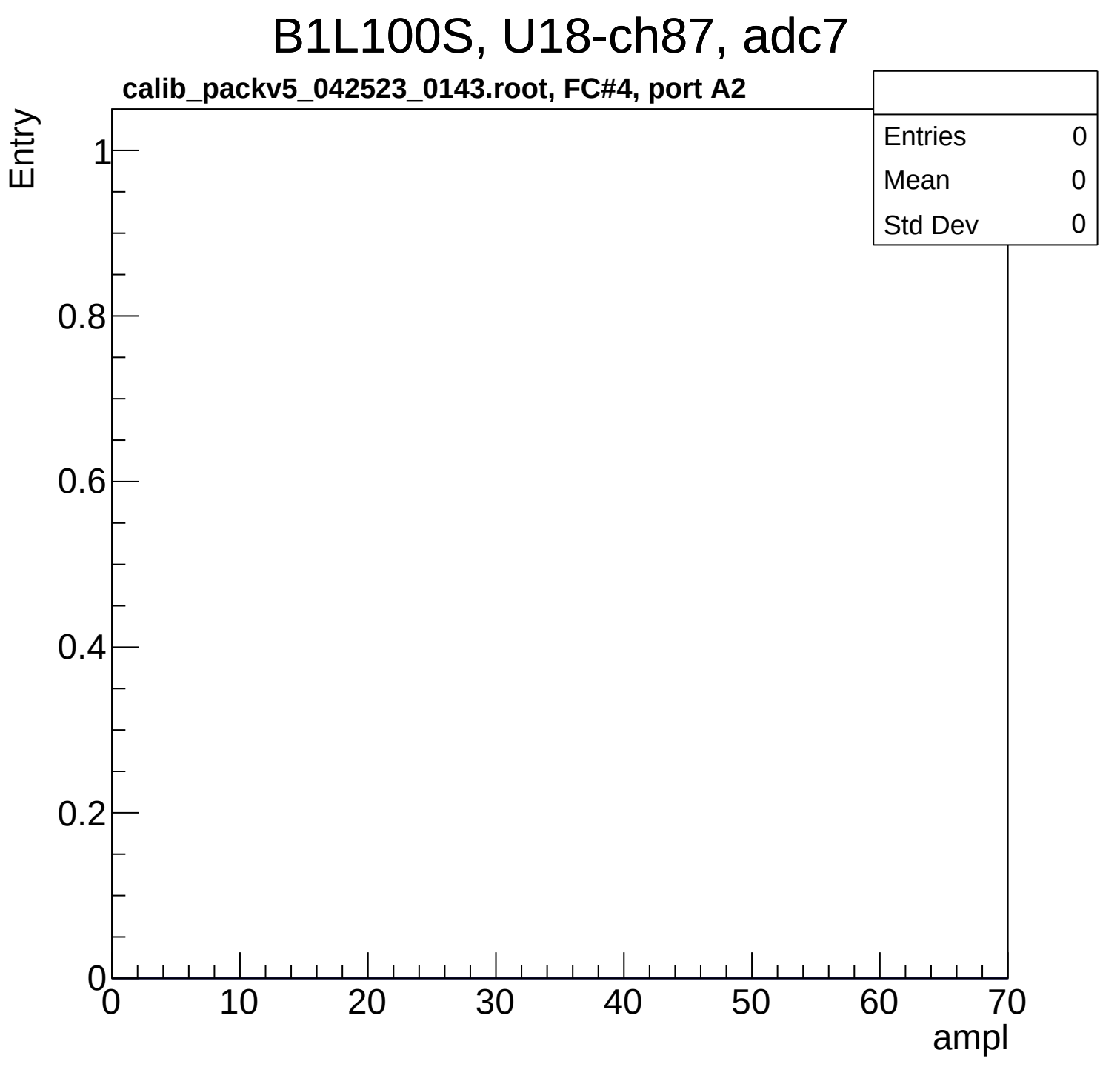

B1L100S, U18-ch87, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 41.64
Std Dev 3.78
Gaus mean : 42.3682
Gaus Width: 3.6324
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

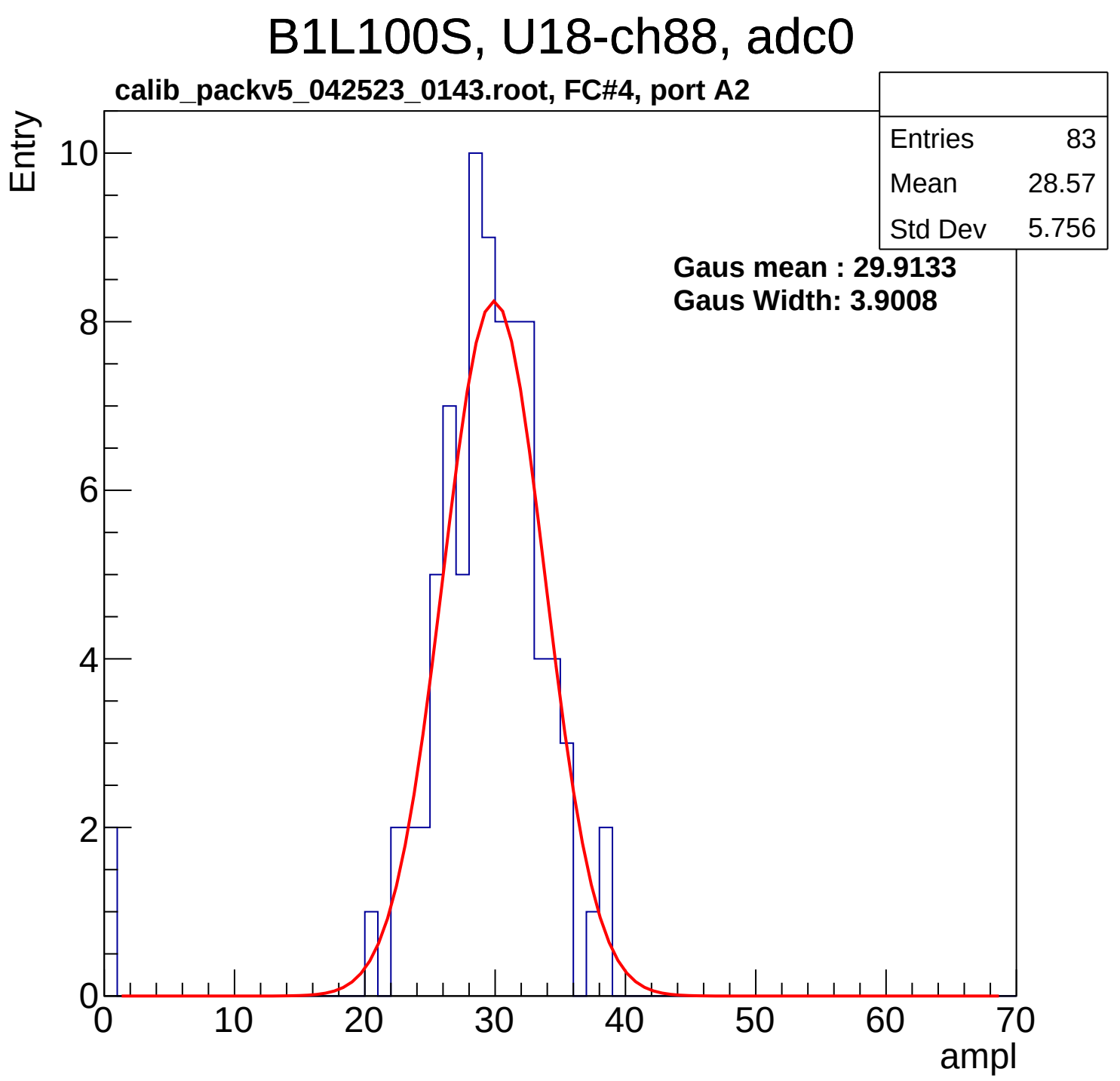

B1L100S, U18-ch87, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 48.79
Std Dev 3.675
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

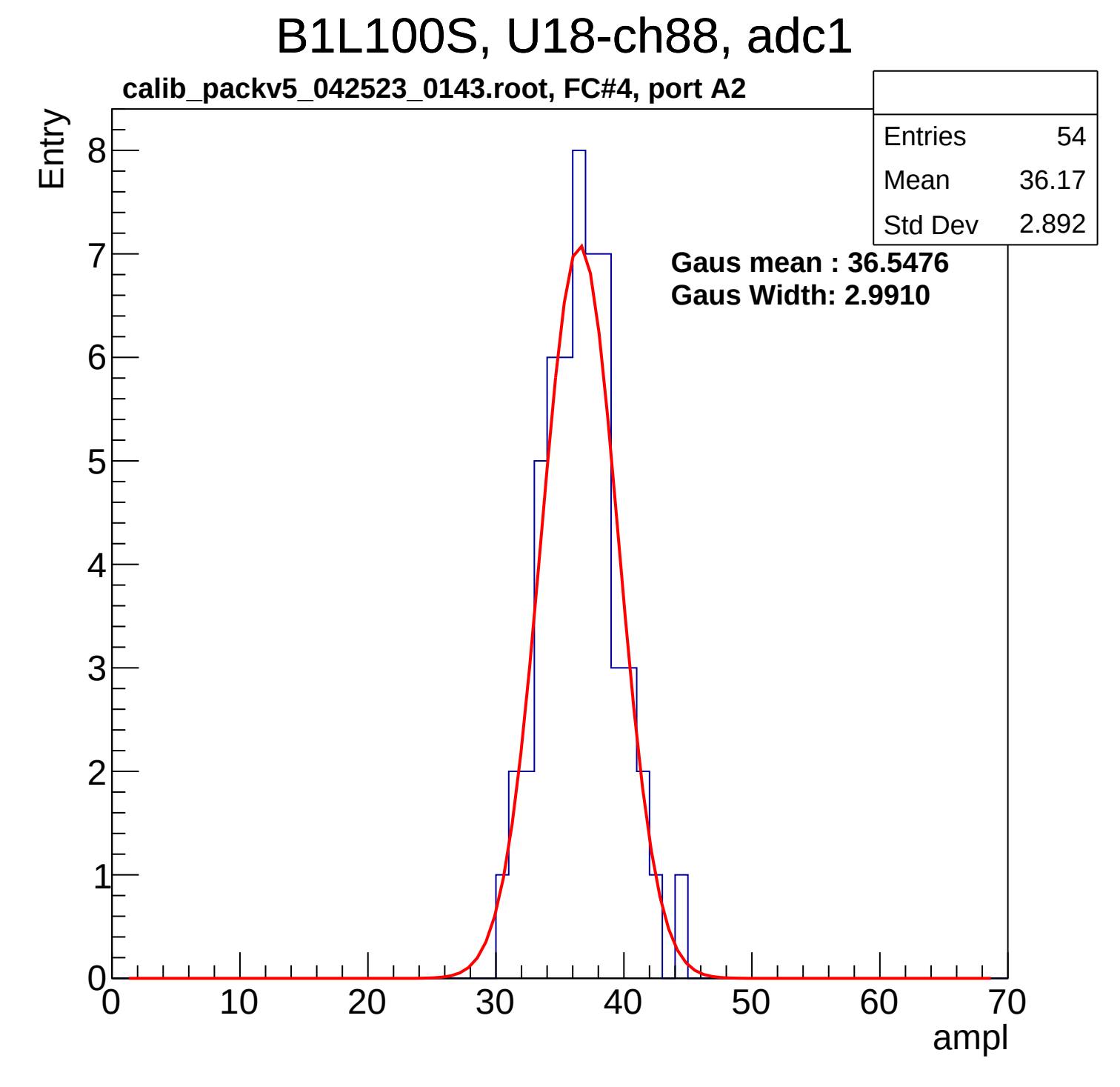

B1L100S, U18-ch87, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 55.28
Std Dev 3.302
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

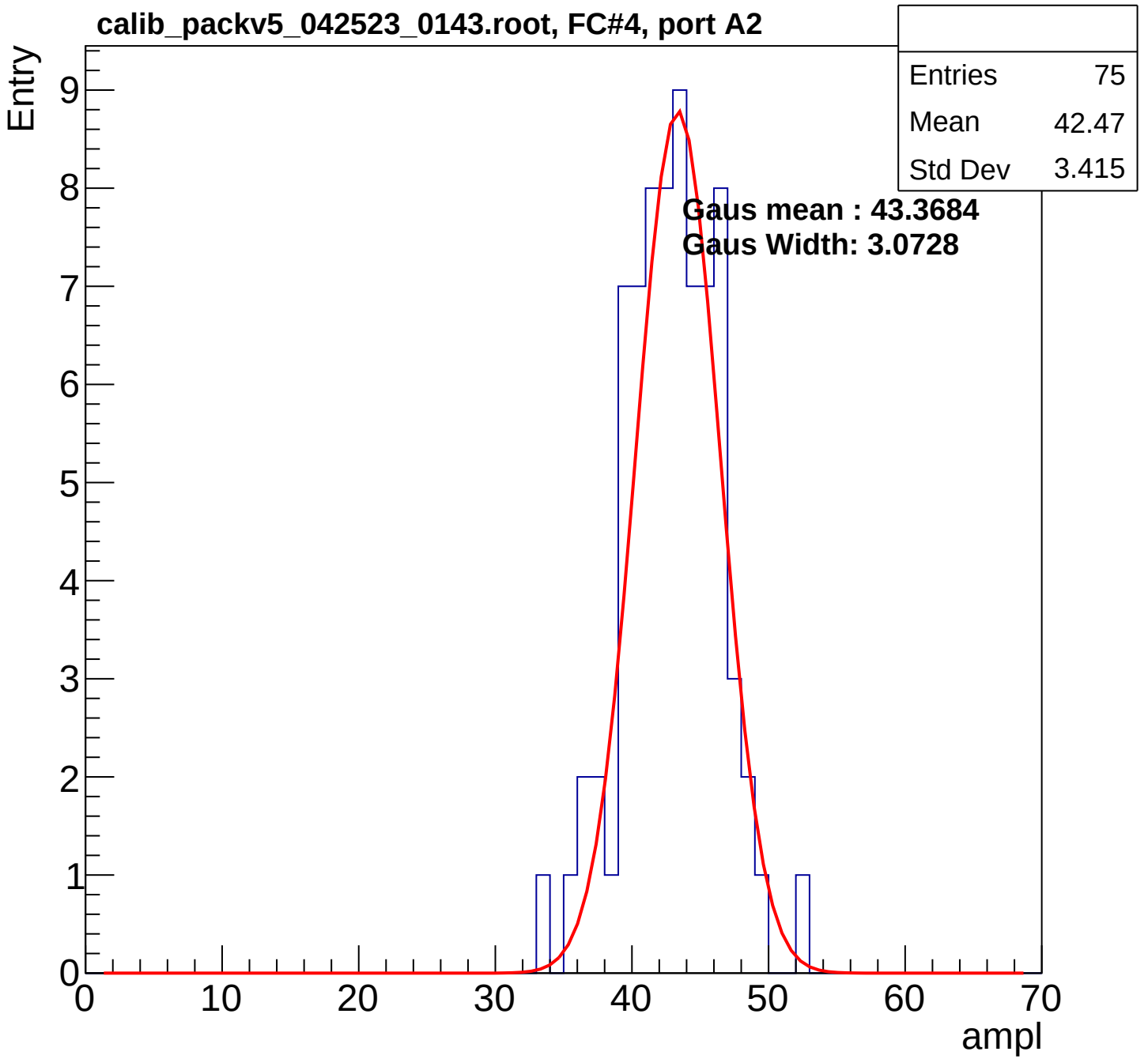

B1L100S, U18-ch87, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 45
Mean 59.89
Std Dev 2.442
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

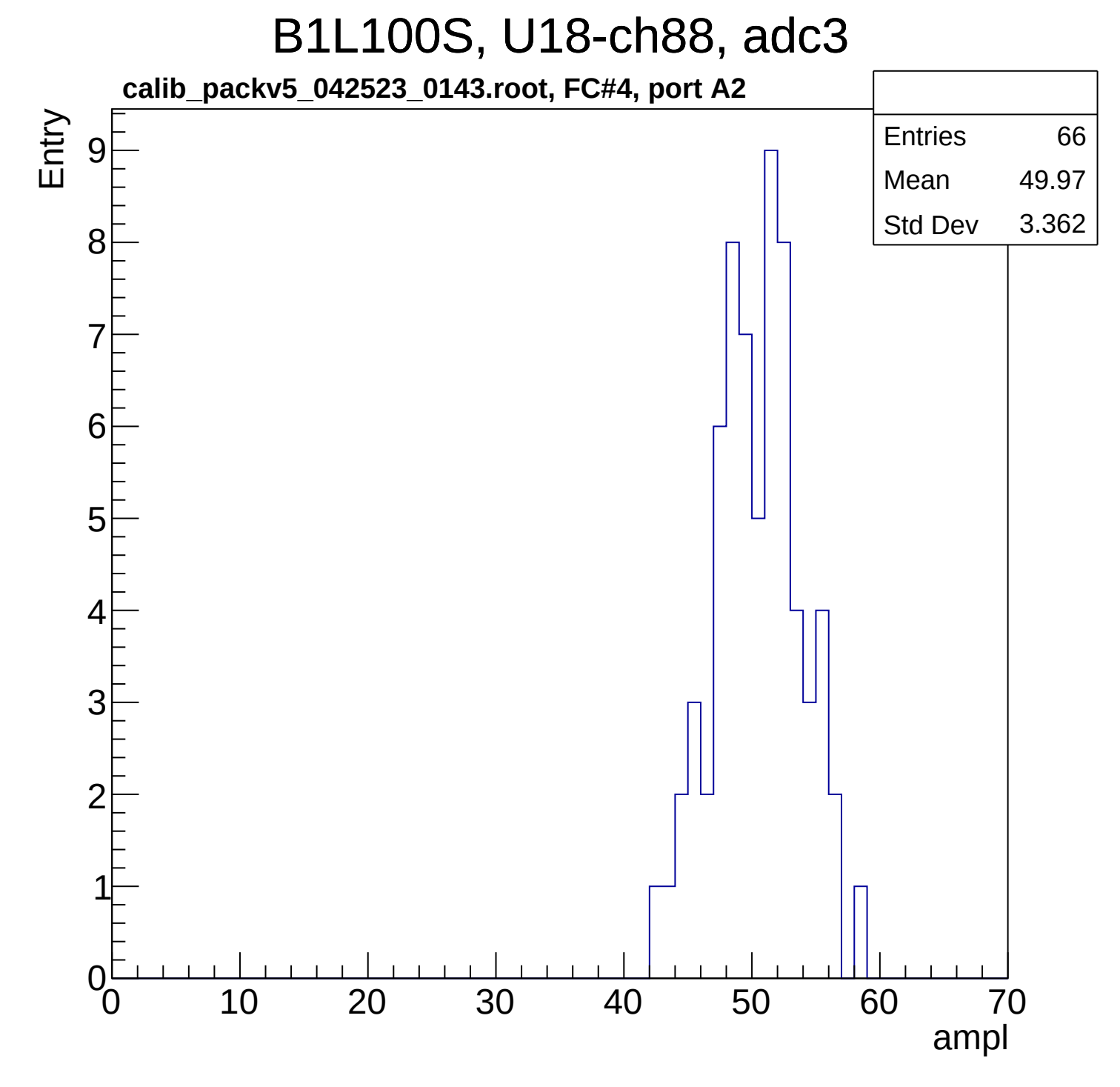

B1L100S, U18-ch87, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 54.56
Std Dev 19.32
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

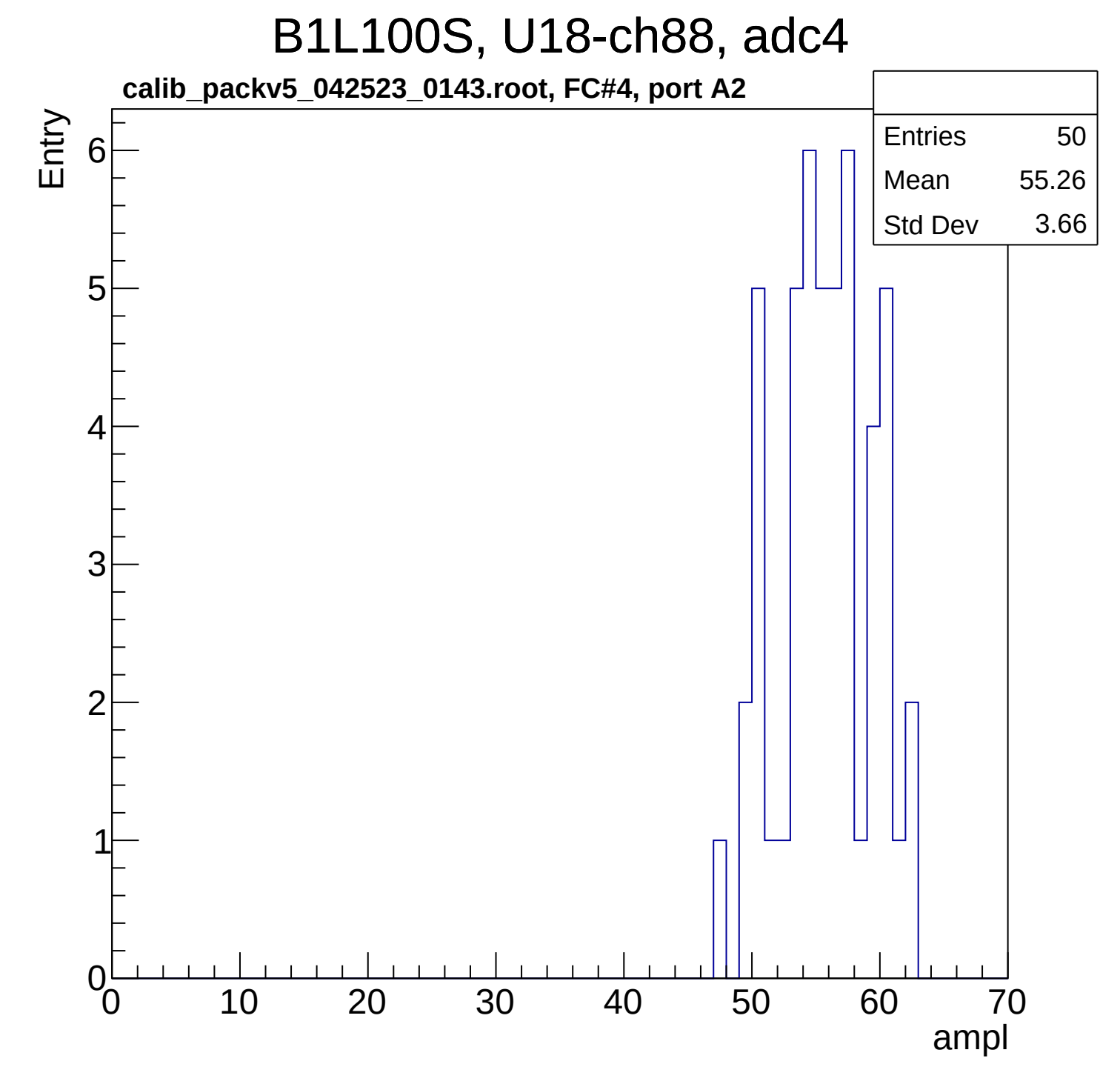

B1L100S, U18-ch87, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

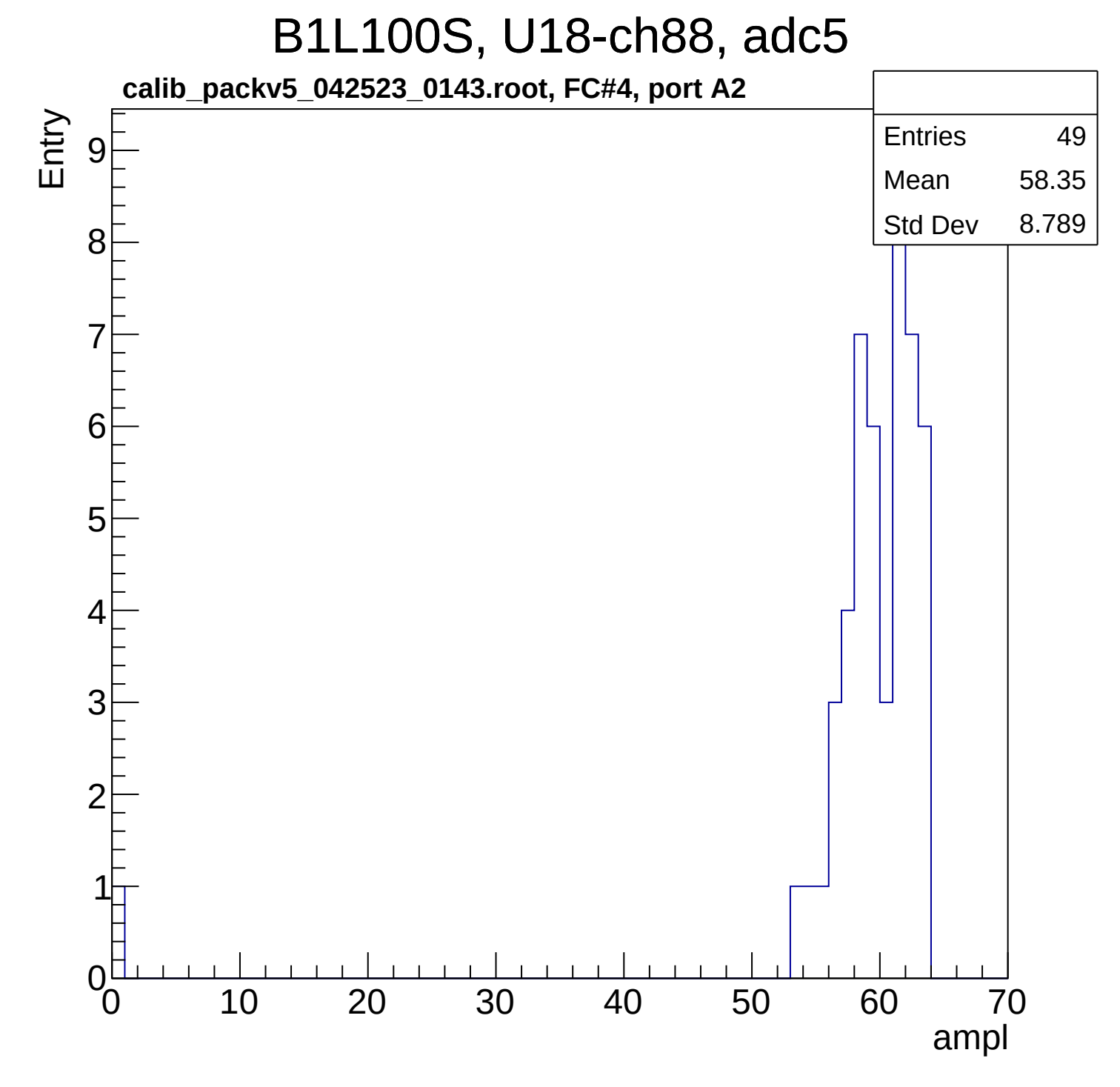

B1L100S, U18-ch88, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 83
Mean 28.57
Std Dev 5.756
Gaus mean : 29.9133
Gaus Width: 3.9008
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

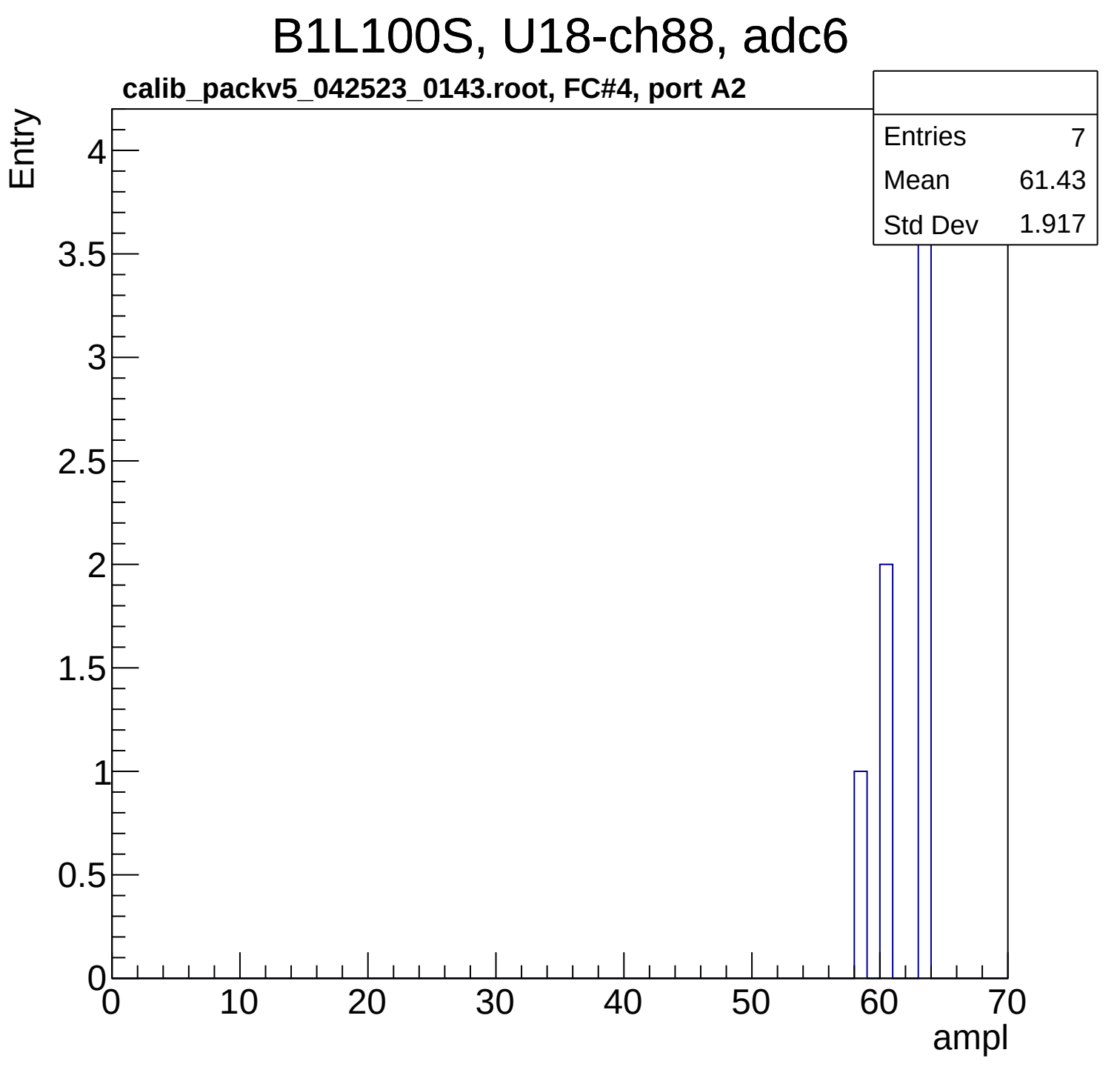

B1L100S, U18-ch88, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 36.17
Std Dev 2.892
Gaus mean : 36.5476
Gaus Width: 2.9910
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

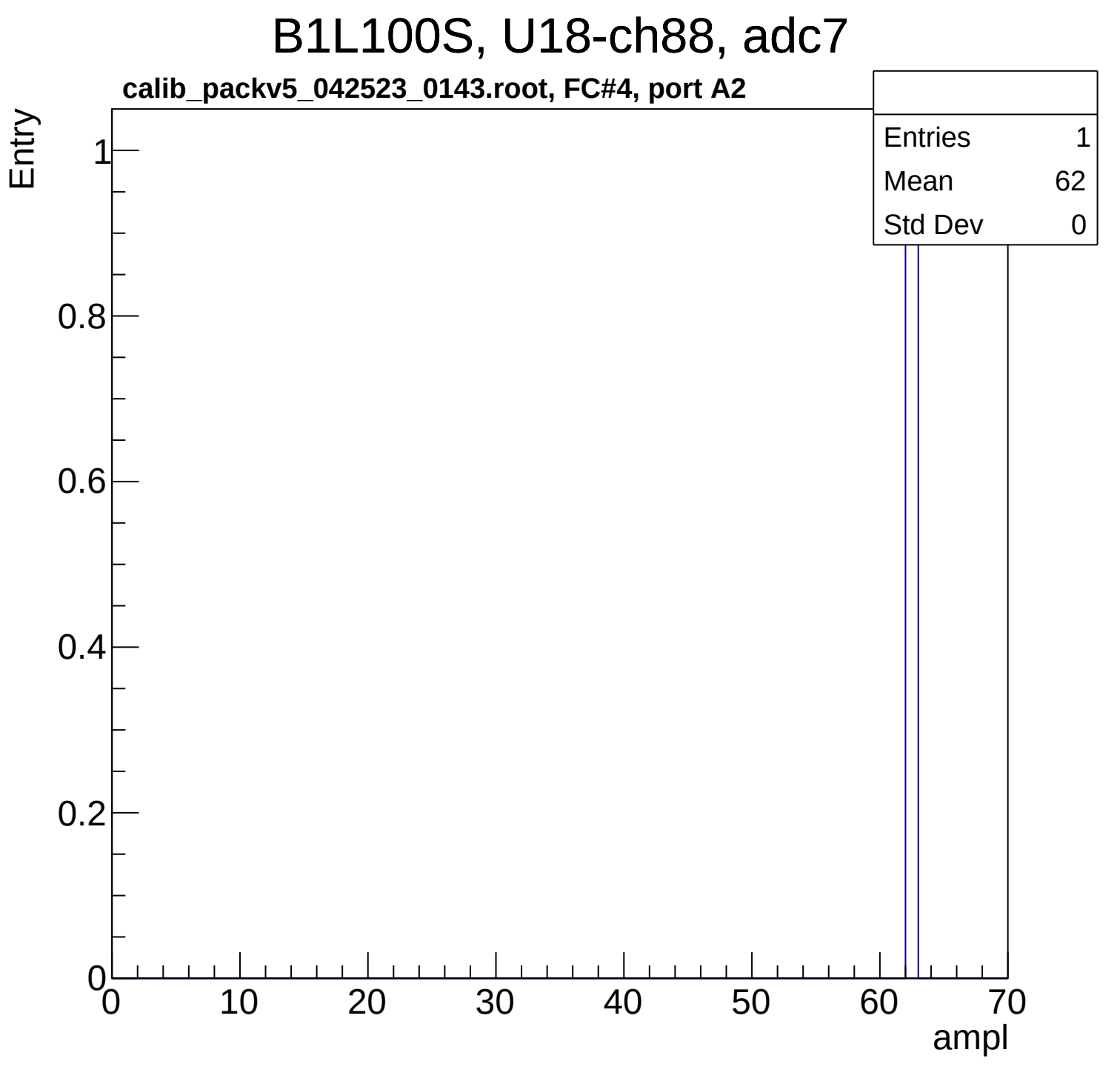

B1L100S, U18-ch88, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 42.47
Std Dev 3.415
Gaus mean : 43.3684
Gaus Width: 3.0728
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

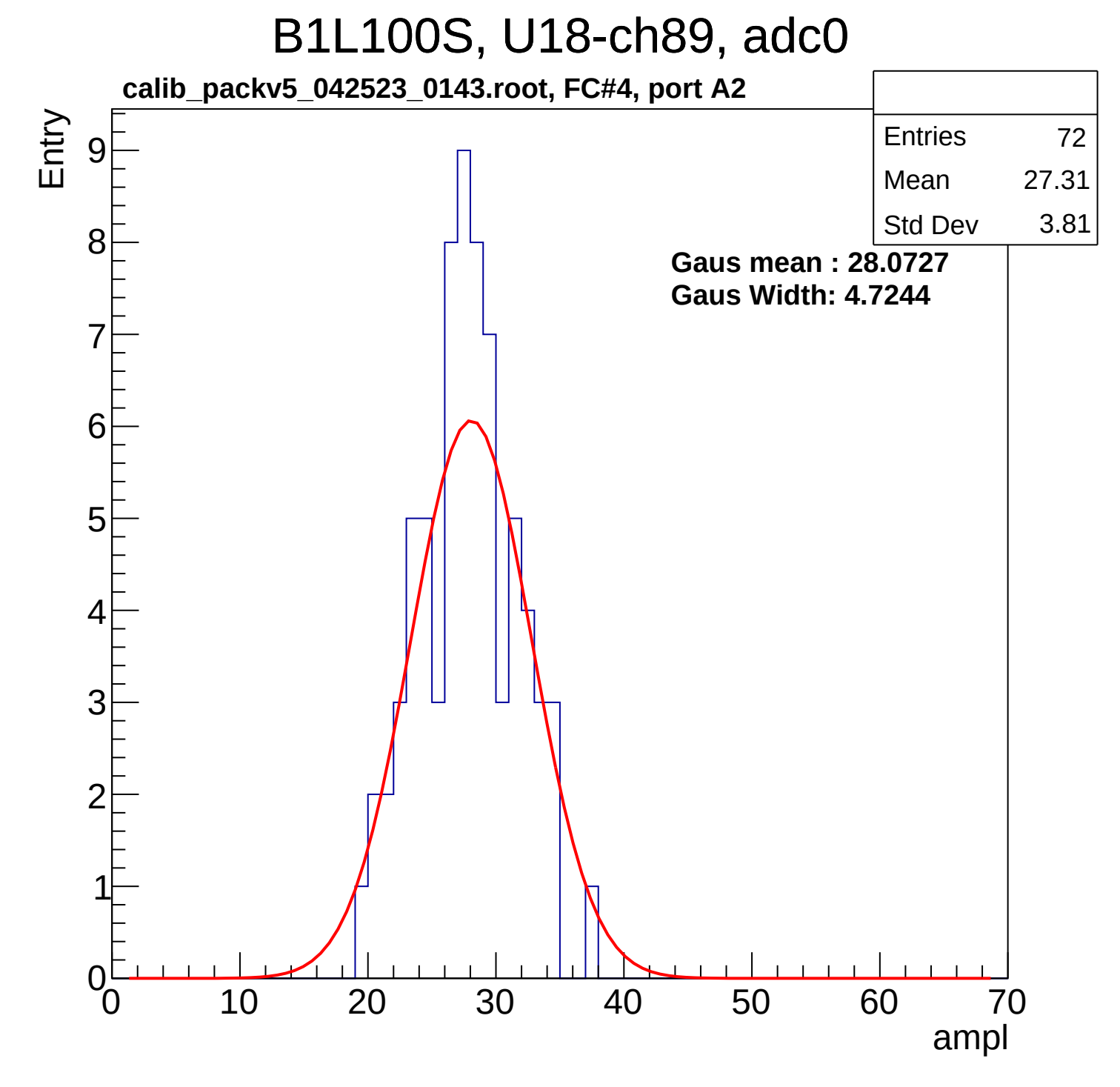

B1L100S, U18-ch88, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 49.97
Std Dev 3.362
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

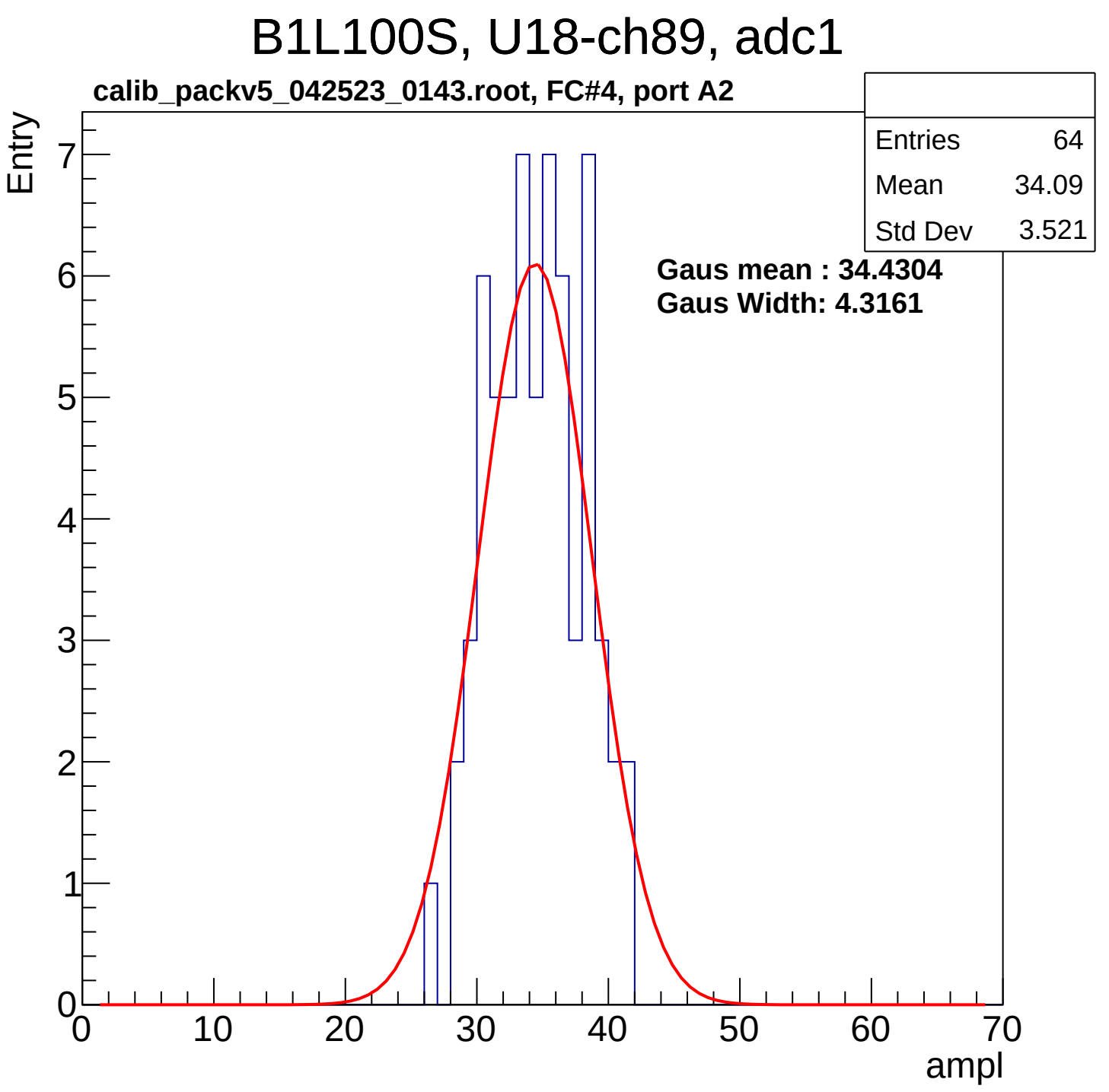

B1L100S, U18-ch88, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 55.26
Std Dev 3.66
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

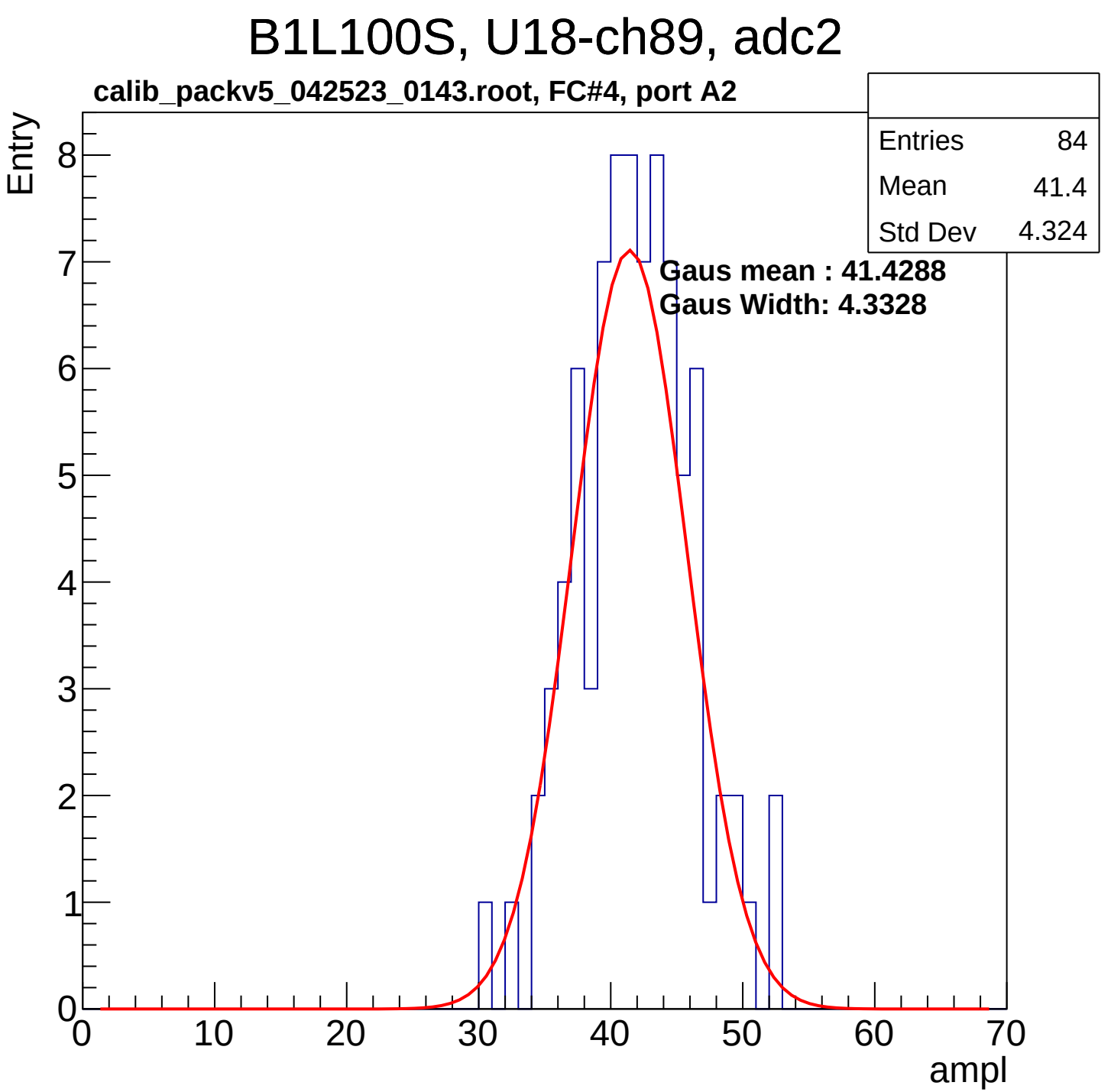

B1L100S, U18-ch88, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 58.35
Std Dev 8.789
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

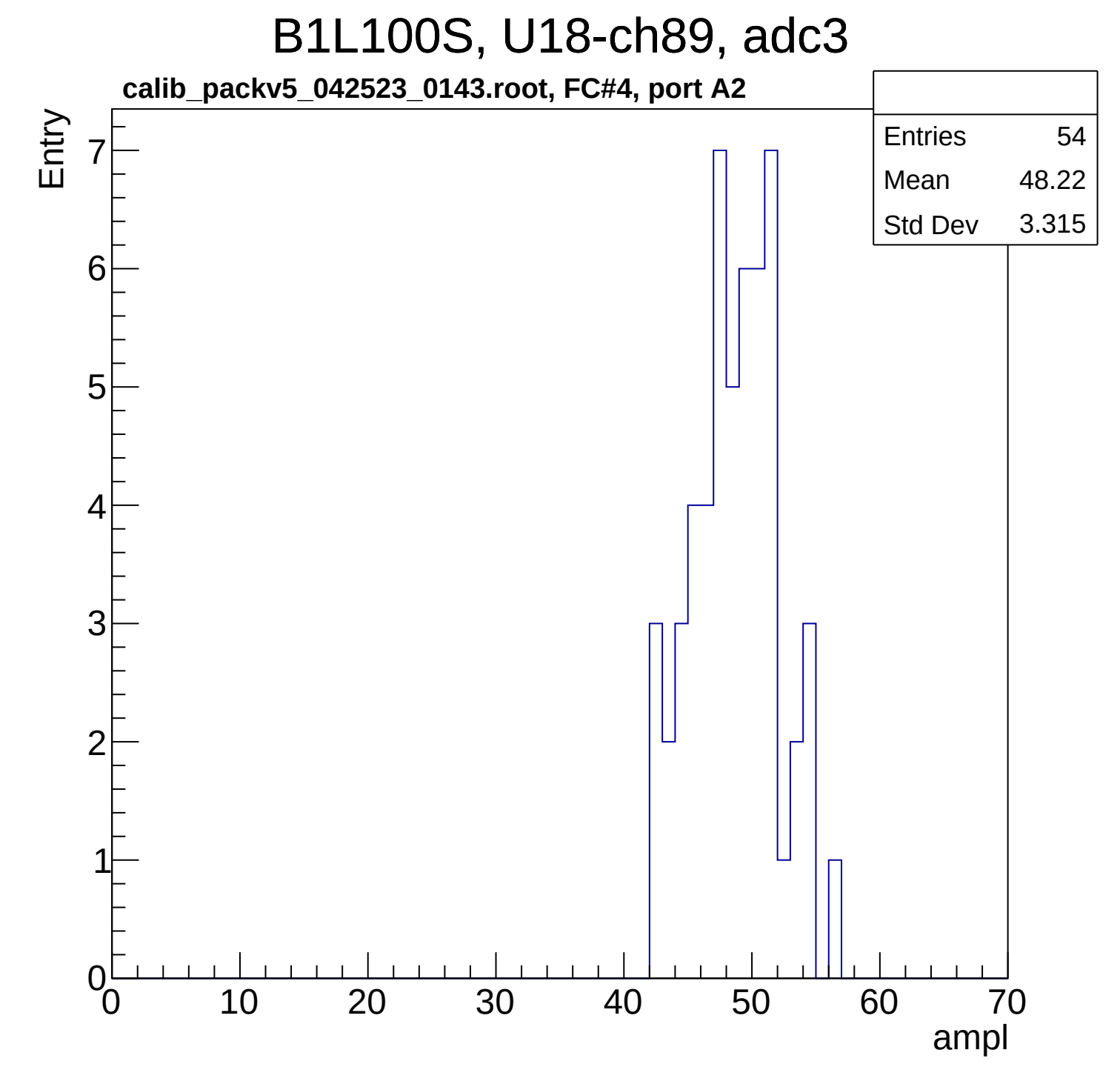

B1L100S, U18-ch88, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 61.43
Std Dev 1.917
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

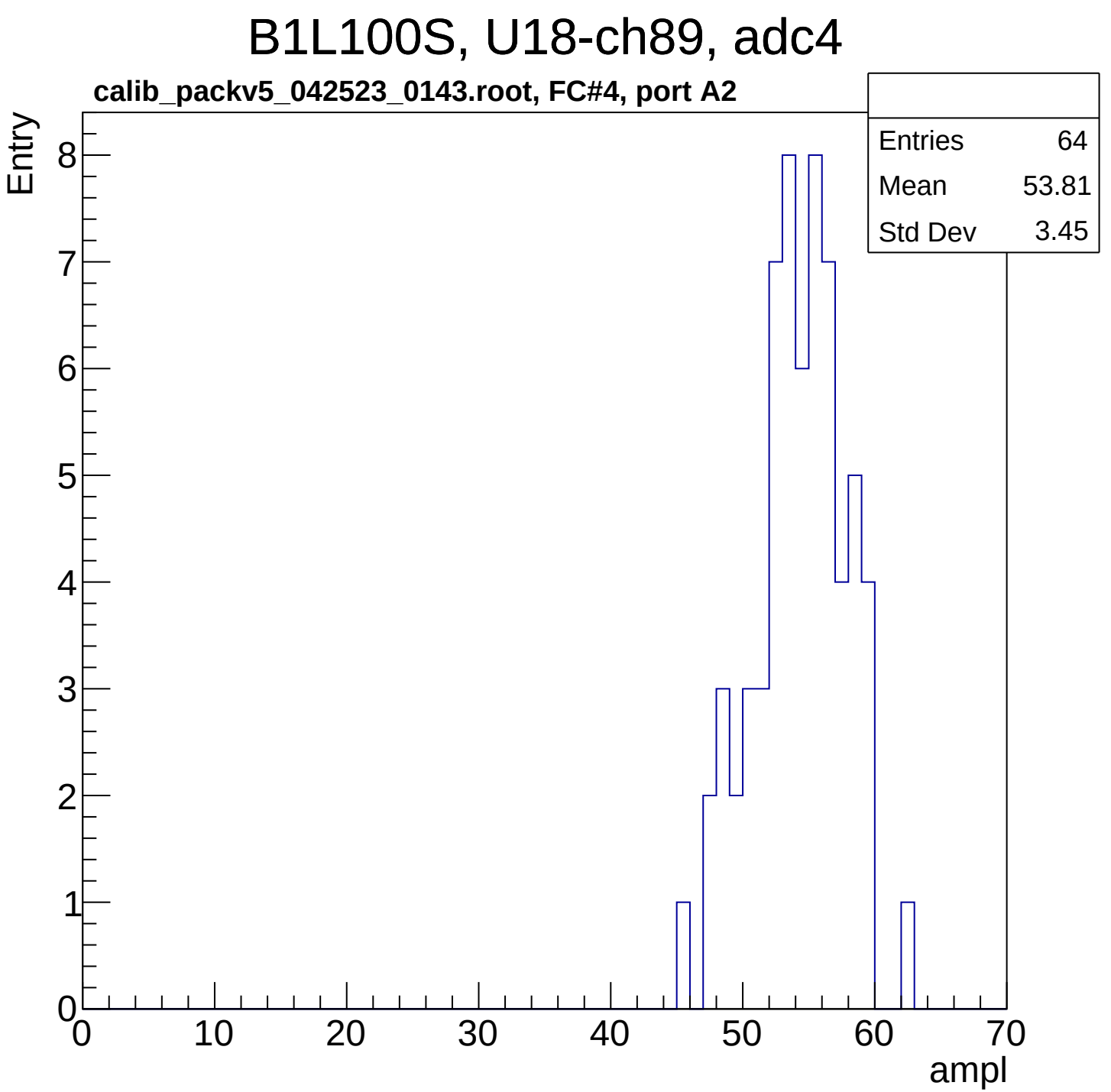

B1L100S, U18-ch88, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

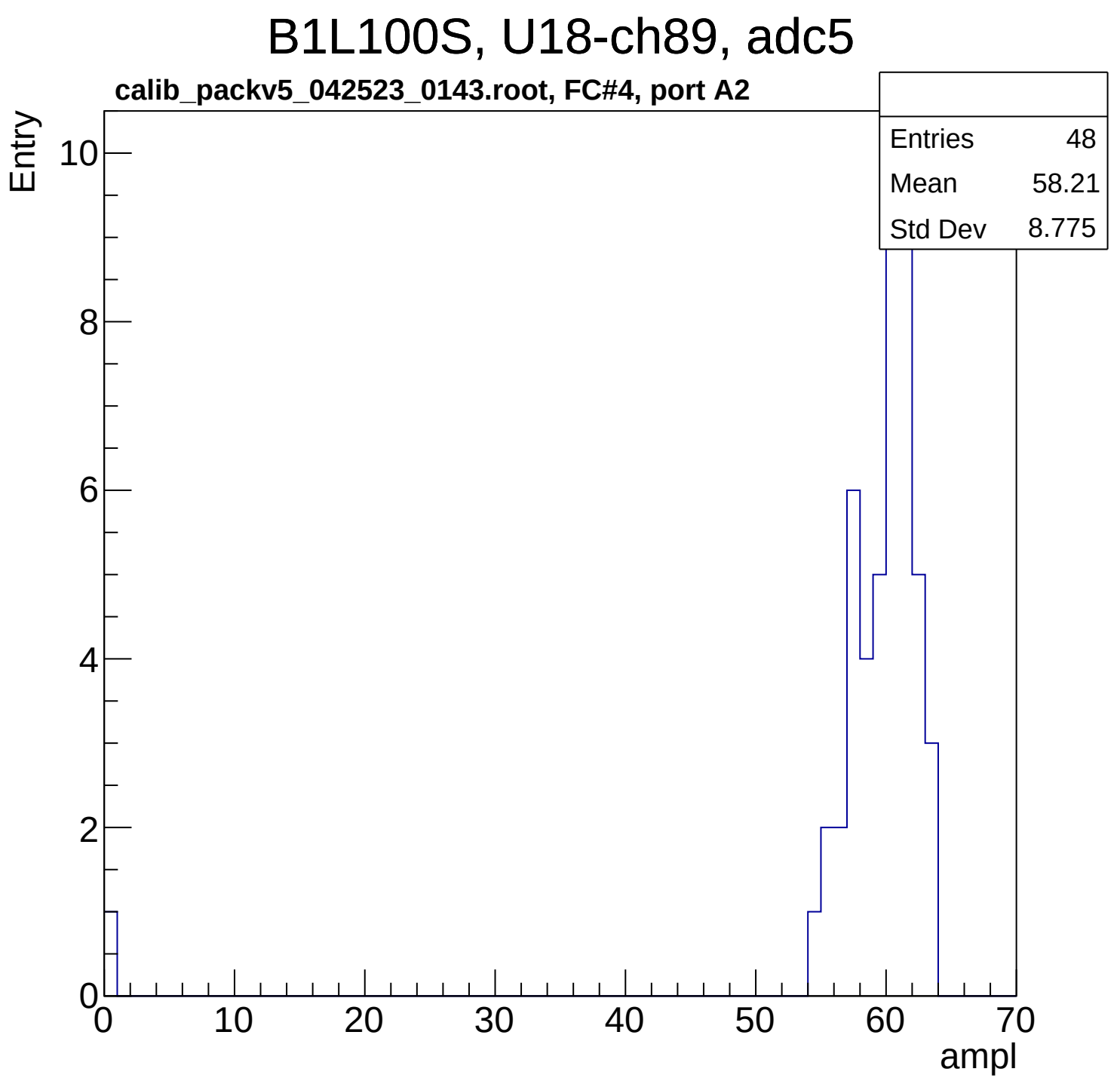

B1L100S, U18-ch89, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 27.31
Std Dev 3.81
Gaus mean : 28.0727
Gaus Width: 4.7244
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

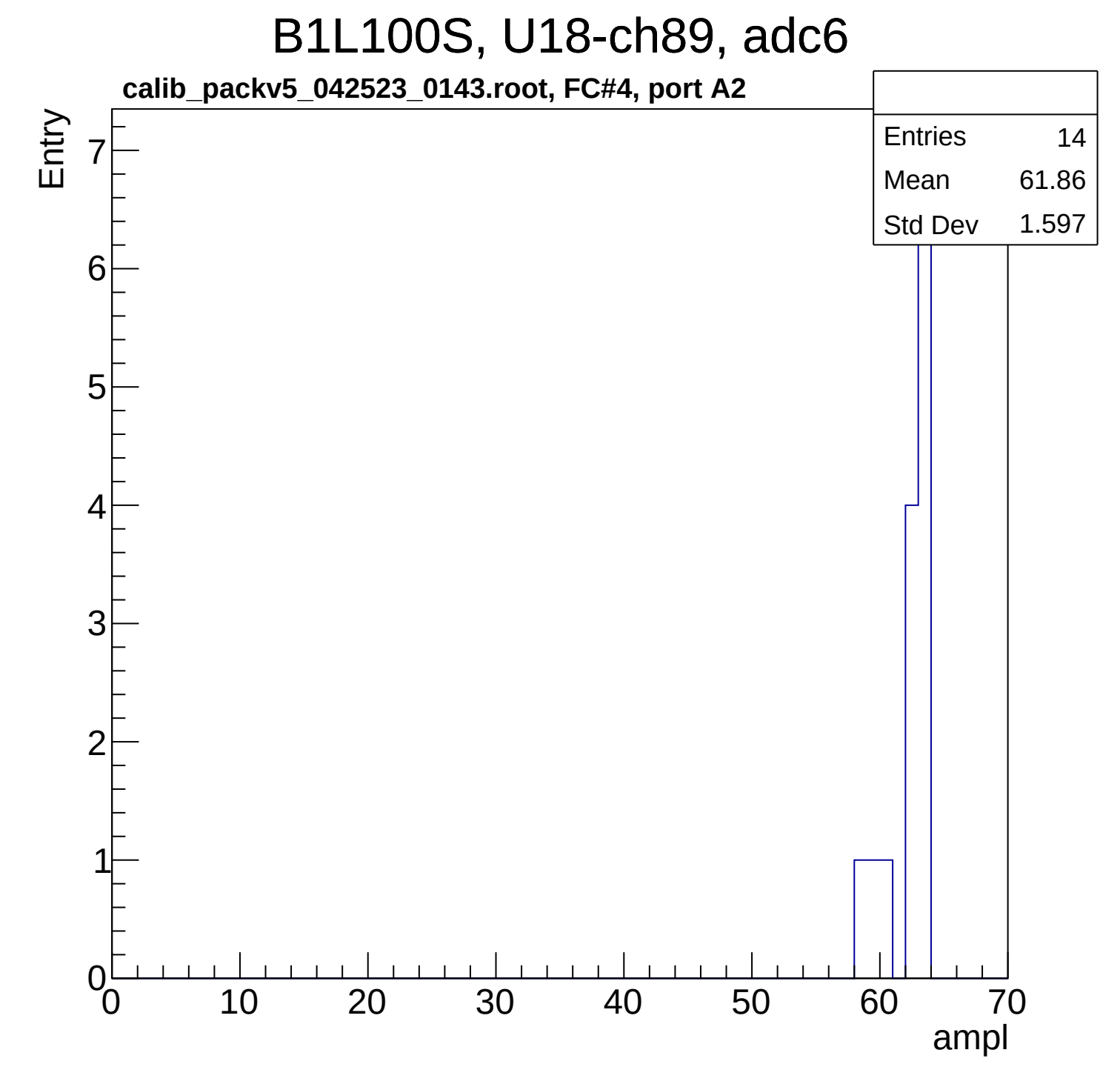

B1L100S, U18-ch89, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 34.09
Std Dev 3.521
Gaus mean : 34.4304
Gaus Width: 4.3161
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

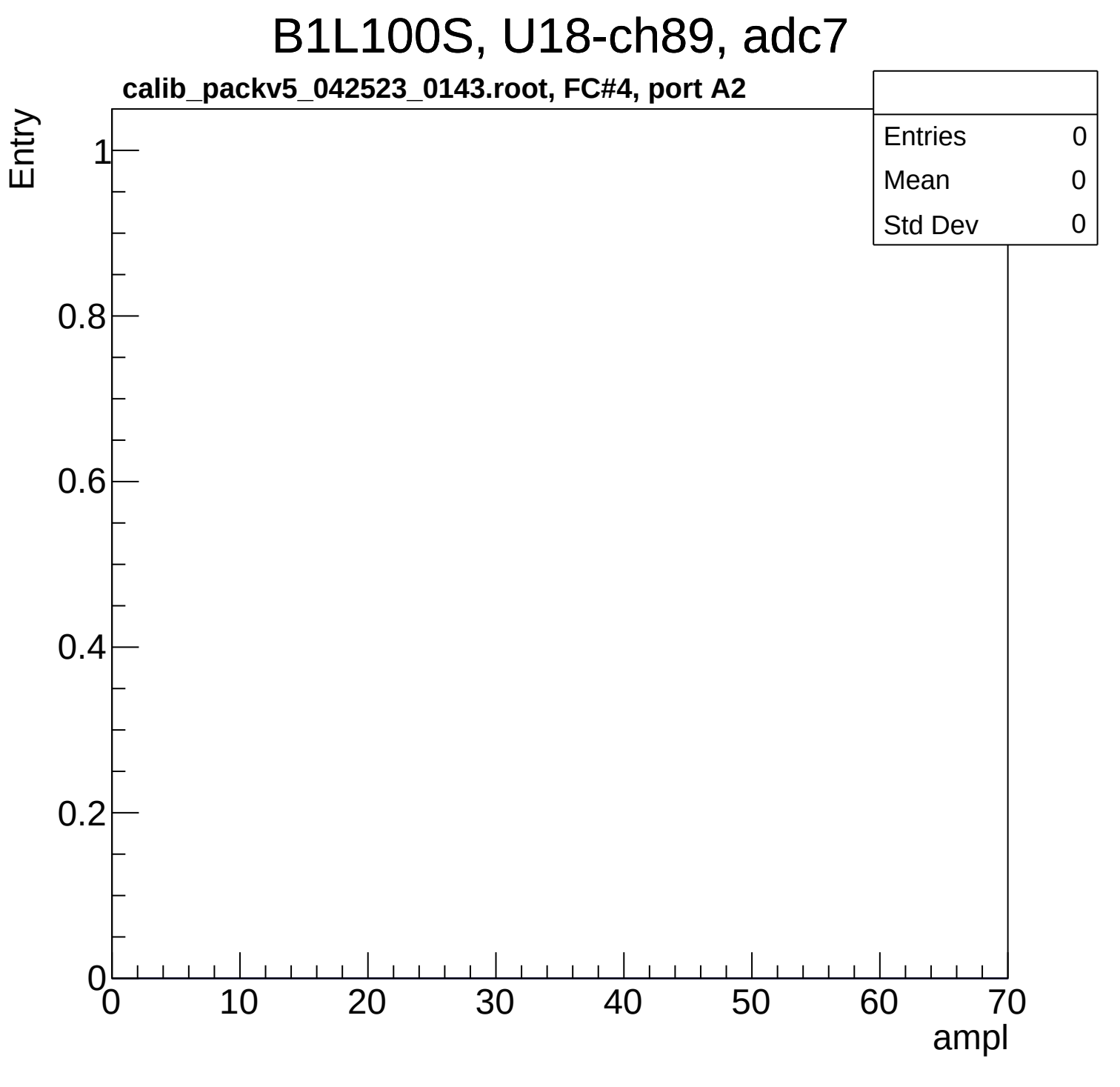

B1L100S, U18-ch89, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 84
Mean 41.4
Std Dev 4.324
Gaus mean : 41.4288
Gaus Width: 4.3328
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

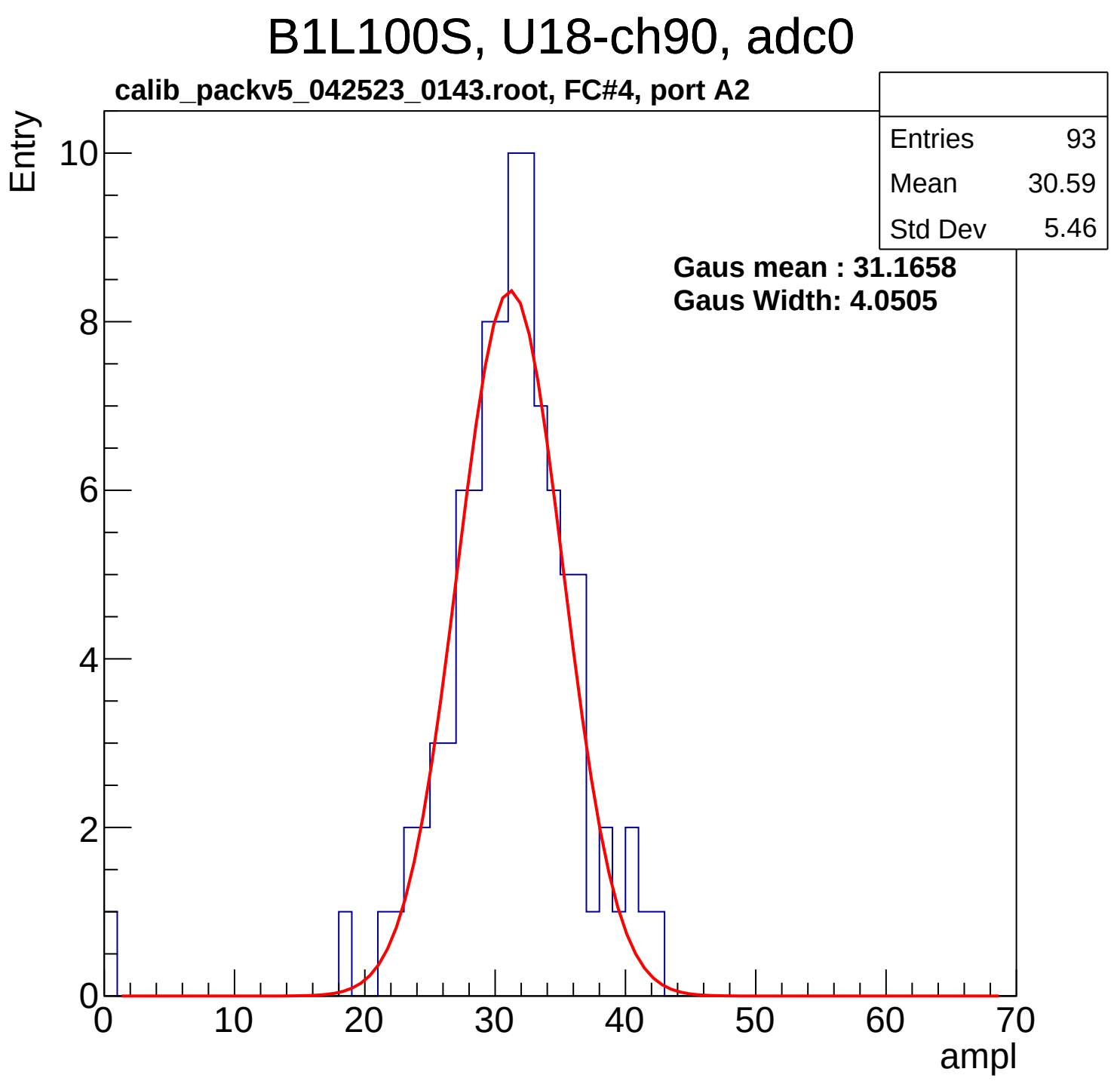

B1L100S, U18-ch89, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 48.22
Std Dev 3.315
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

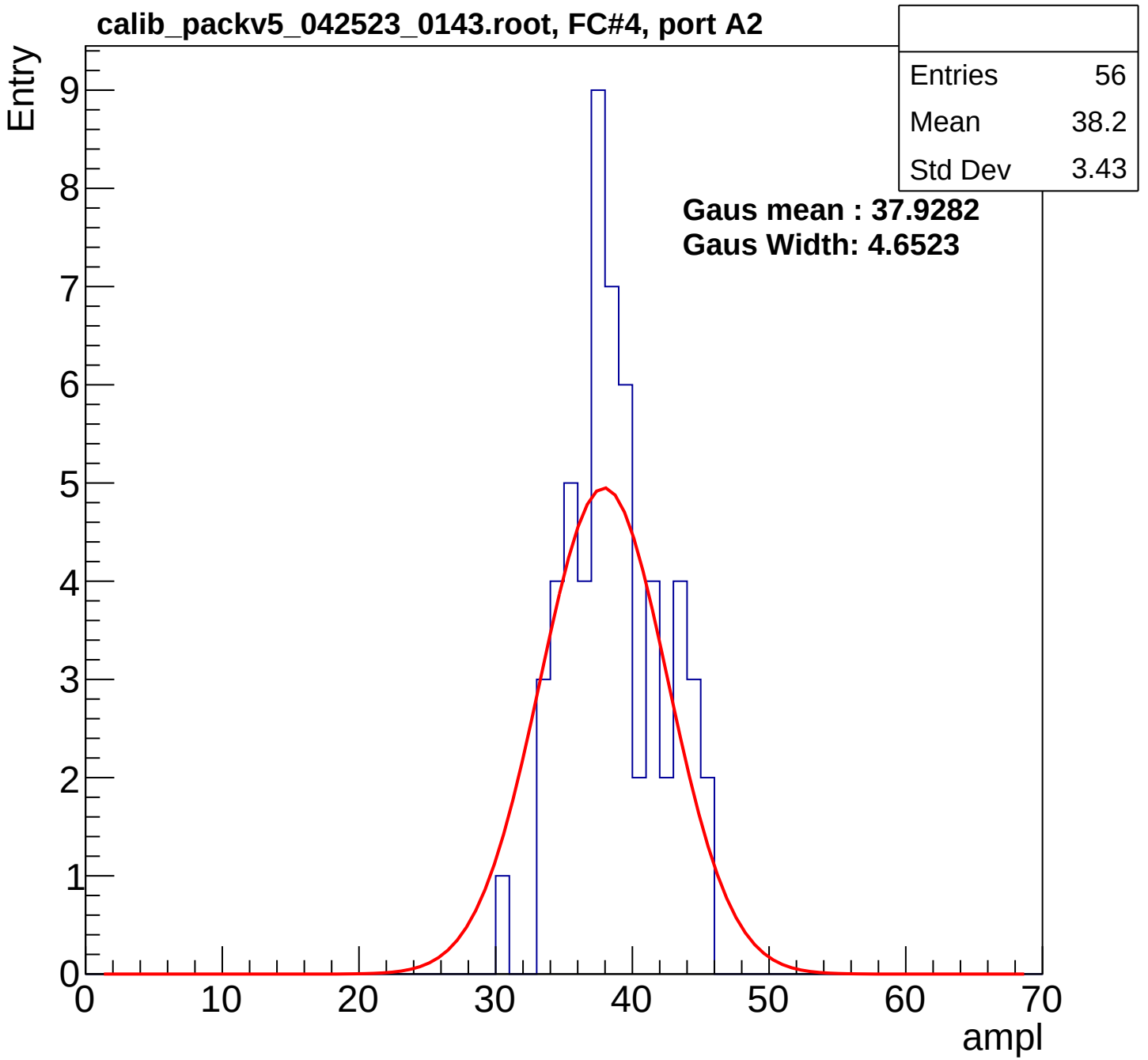

B1L100S, U18-ch89, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 53.81
Std Dev 3.45
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

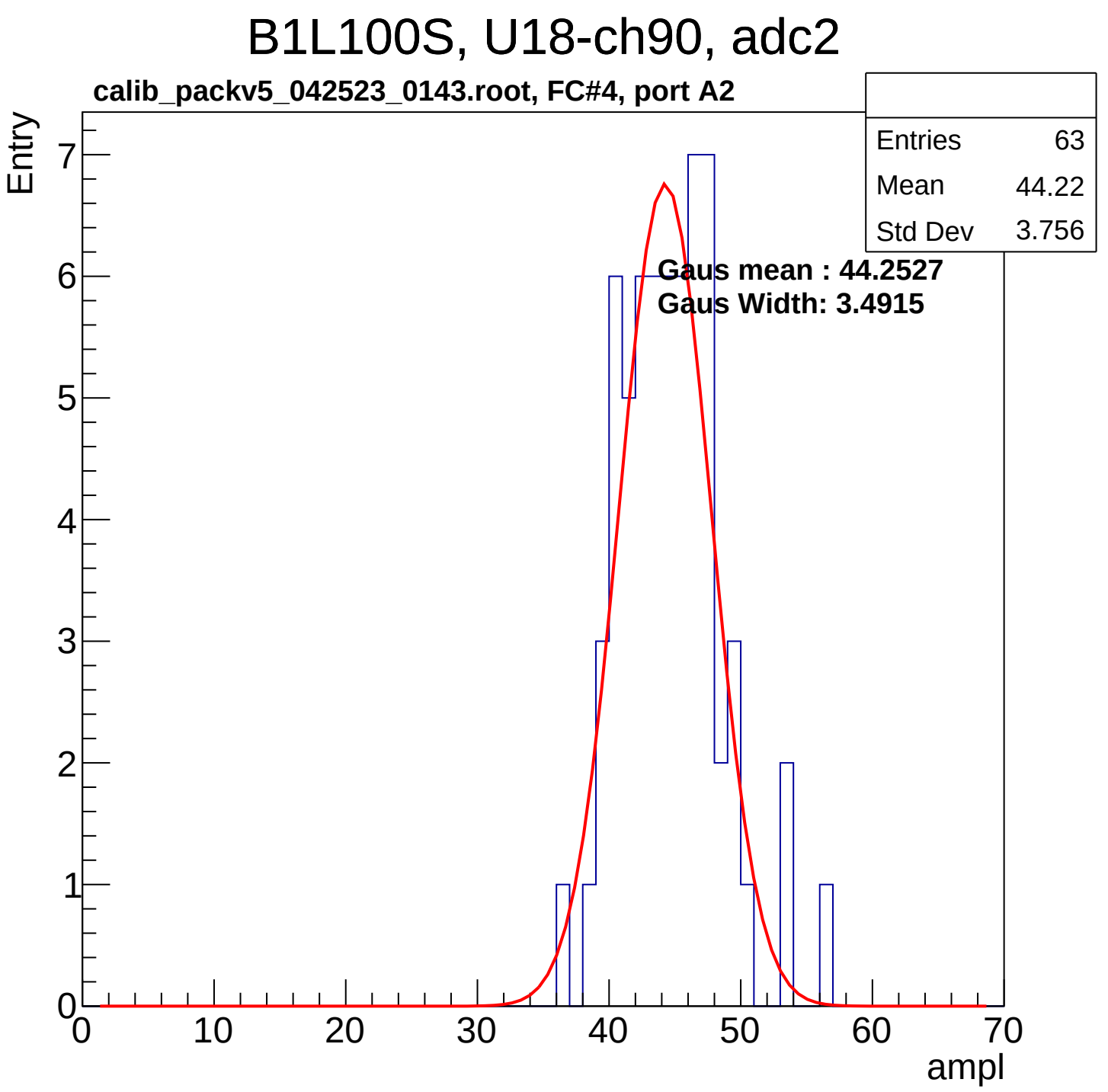

B1L100S, U18-ch89, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 58.21
Std Dev 8.775
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

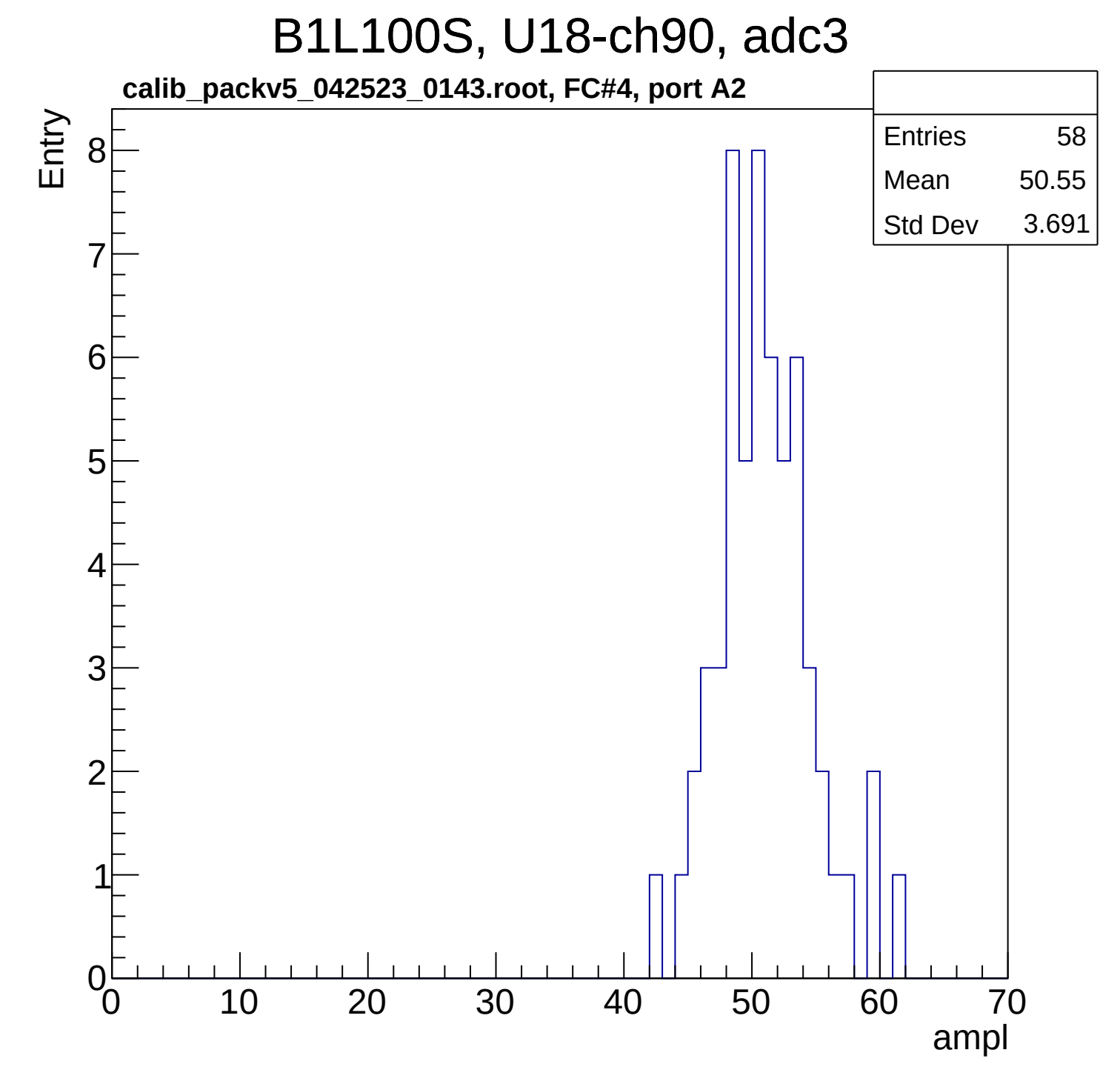

B1L100S, U18-ch89, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 14
Mean 61.86
Std Dev 1.597
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

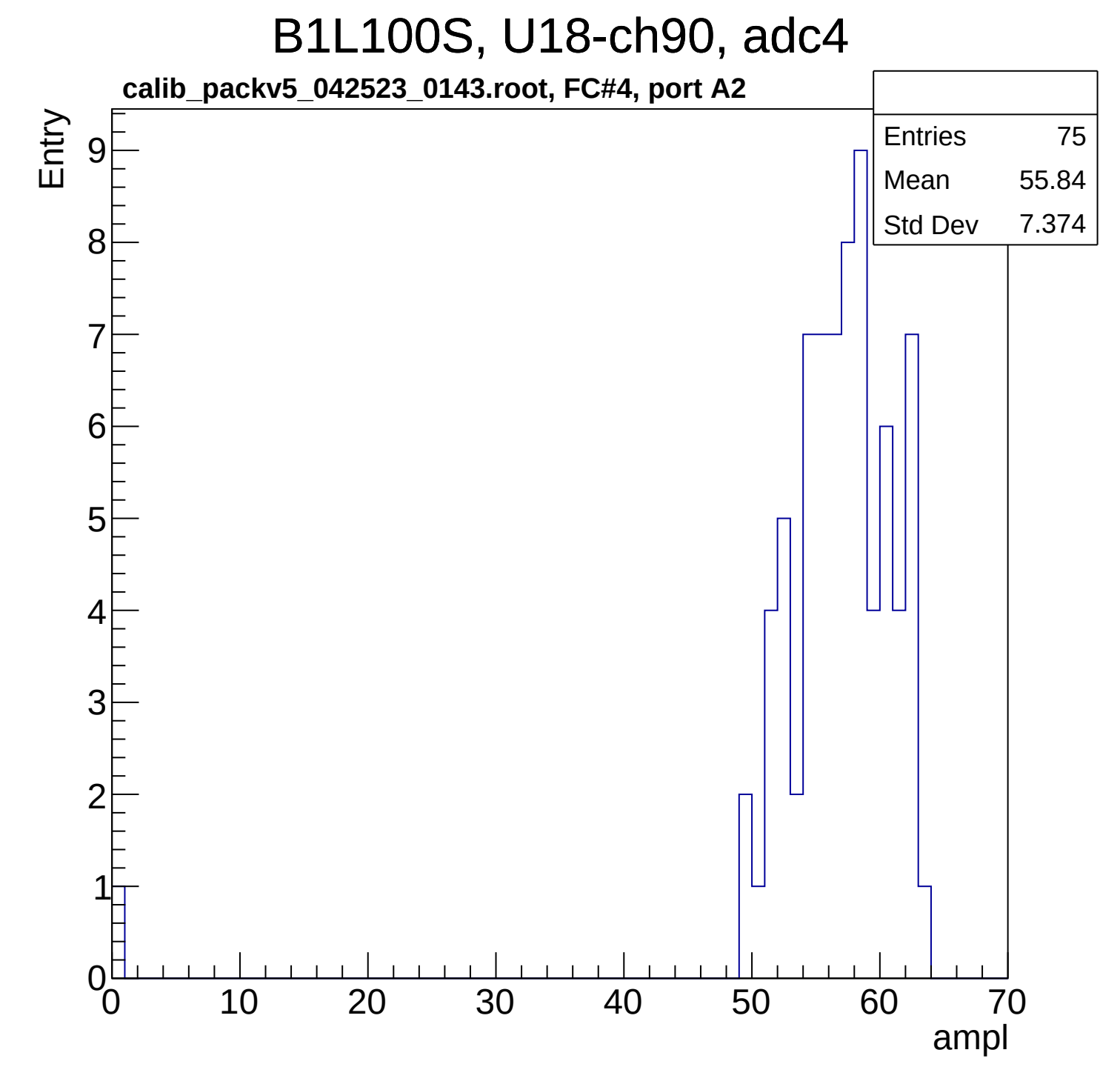

B1L100S, U18-ch89, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

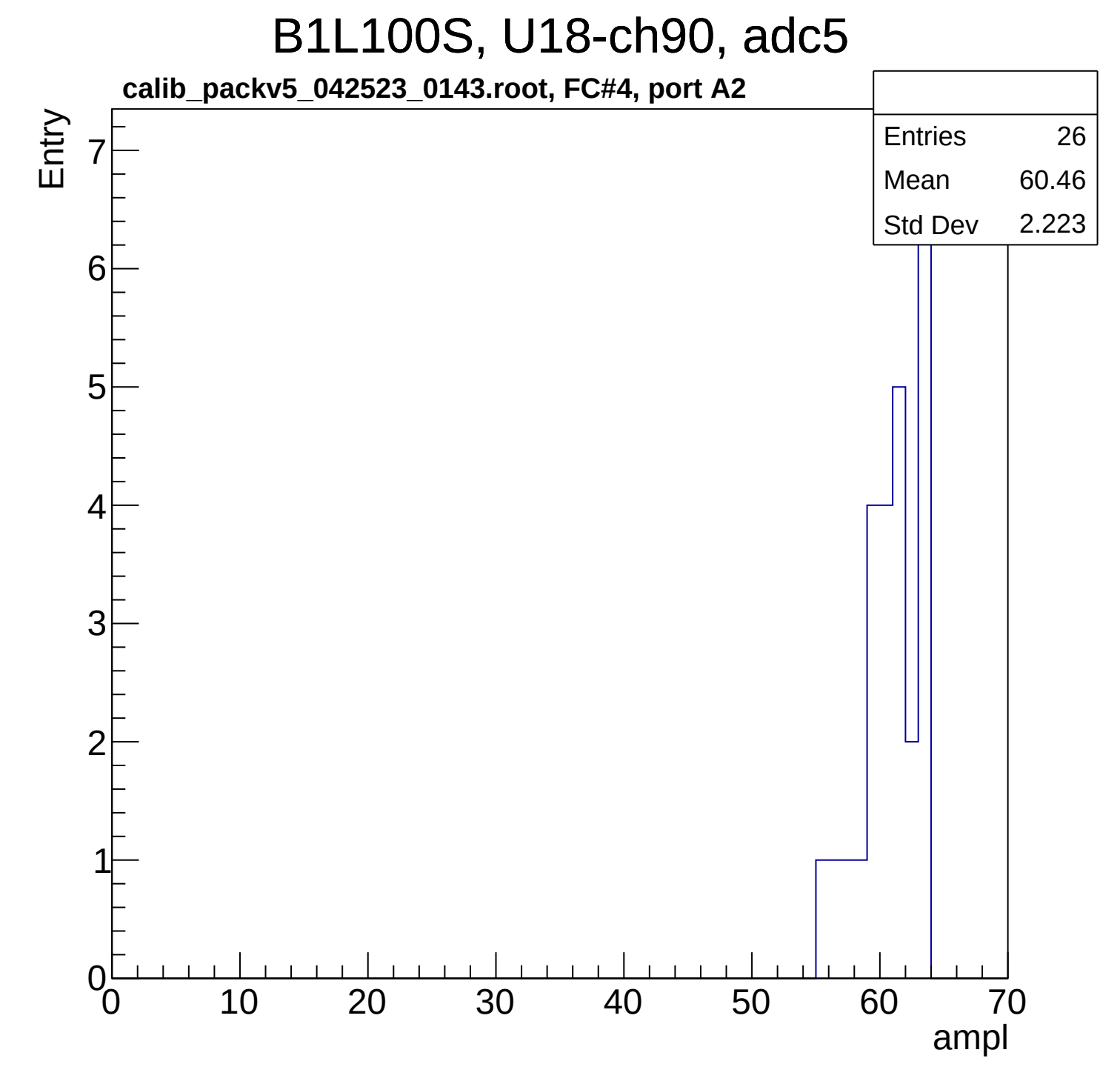

B1L100S, U18-ch90, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 93
Mean 30.59
Std Dev 5.46
Gaus mean : 31.1658
Gaus Width: 4.0505
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

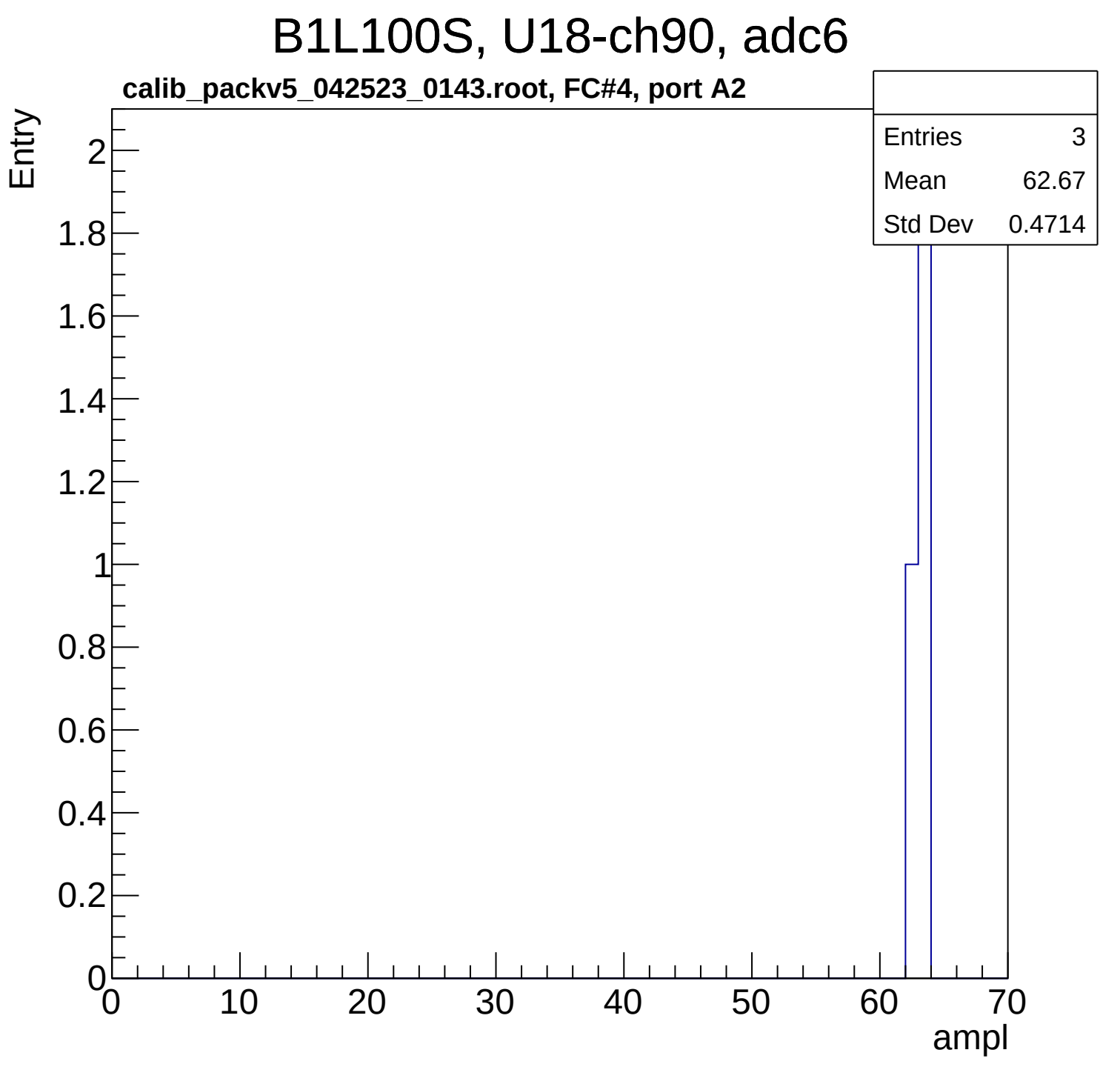

B1L100S, U18-ch90, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 38.2
Std Dev 3.43
Gaus mean : 37.9282
Gaus Width: 4.6523
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

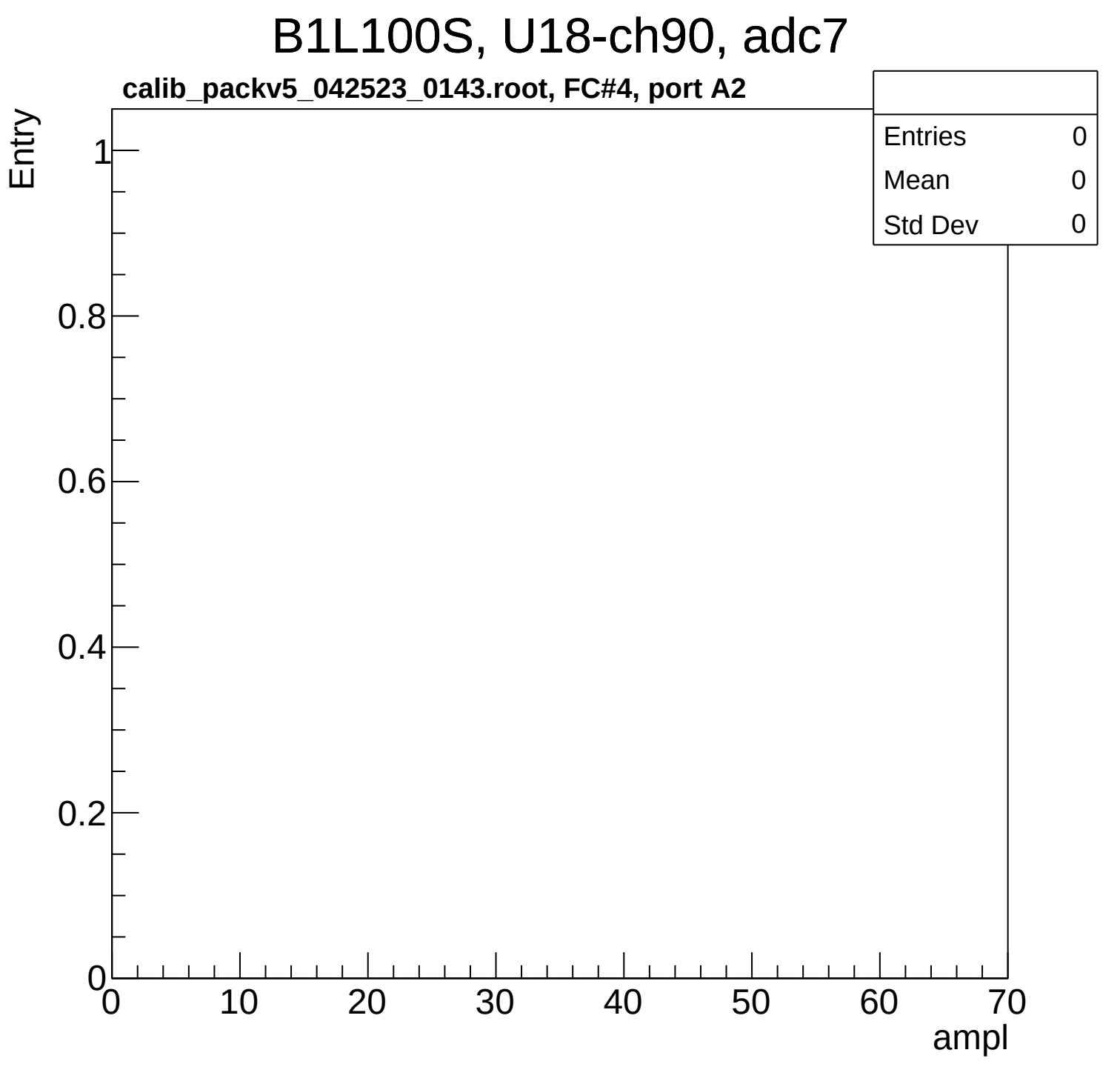

B1L100S, U18-ch90, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 44.22
Std Dev 3.756
Gaus mean : 44.2527
Gaus Width: 3.4915
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

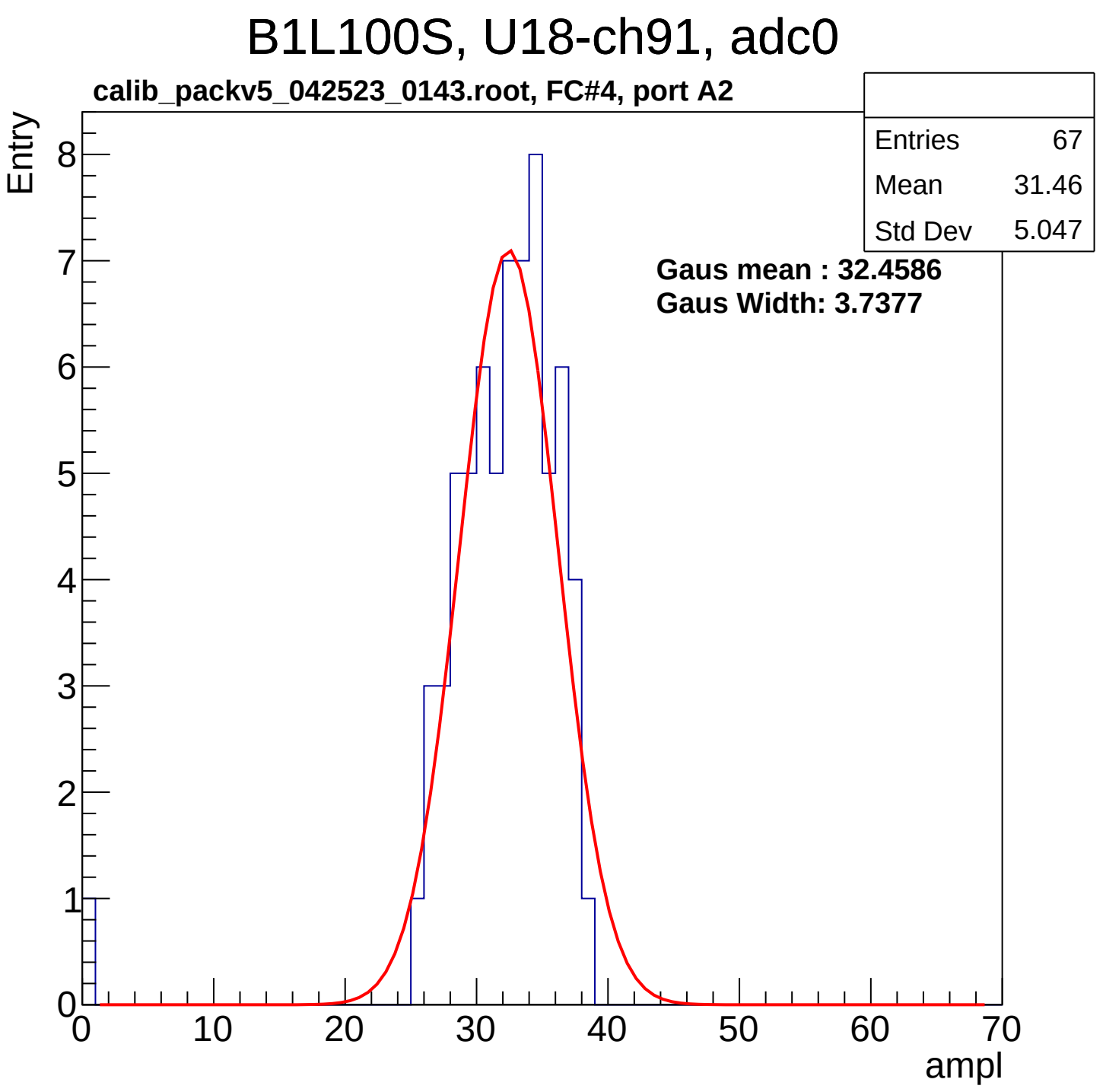

B1L100S, U18-ch90, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 50.55
Std Dev 3.691
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

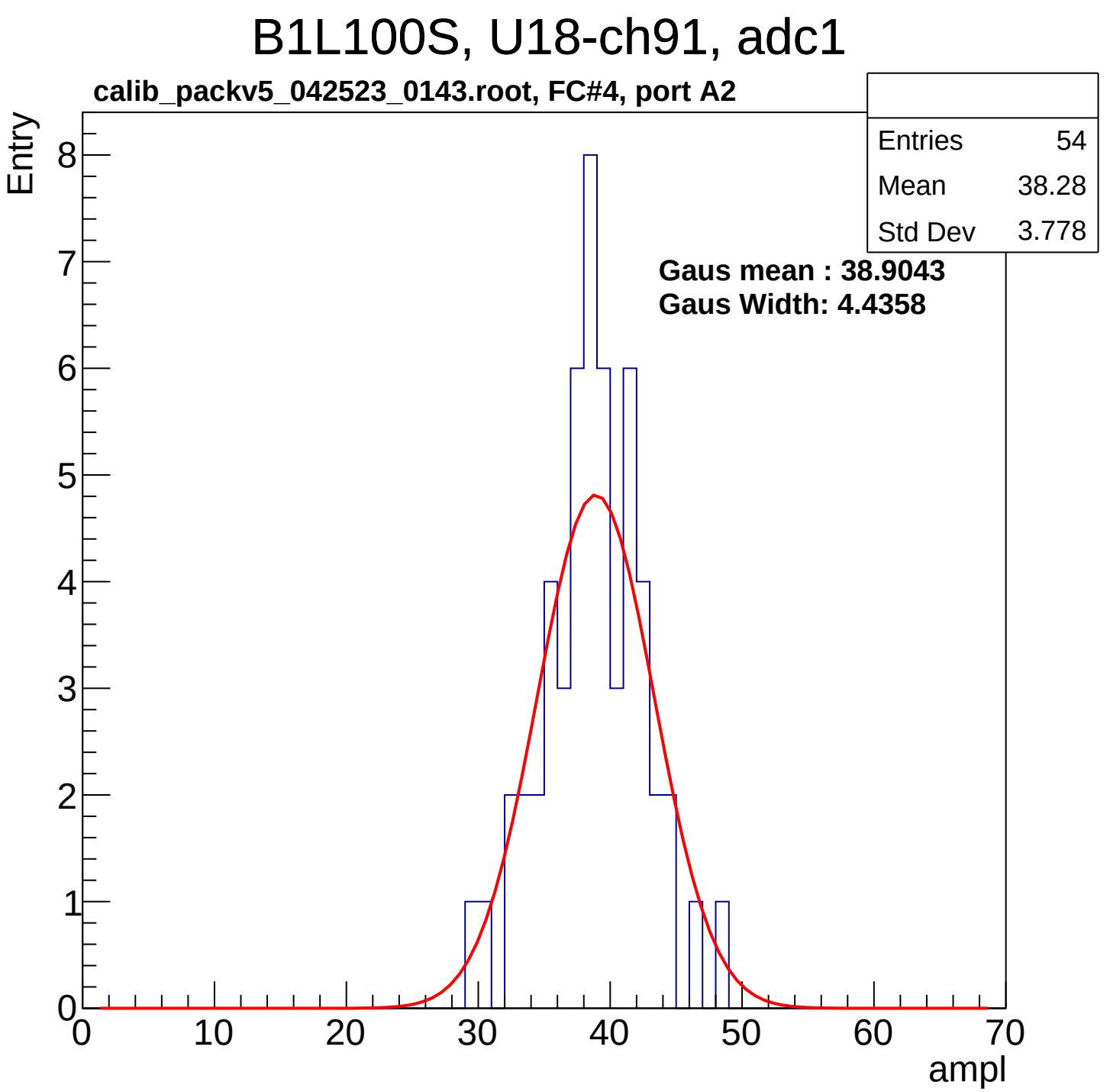

B1L100S, U18-ch90, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 55.84
Std Dev 7.374
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

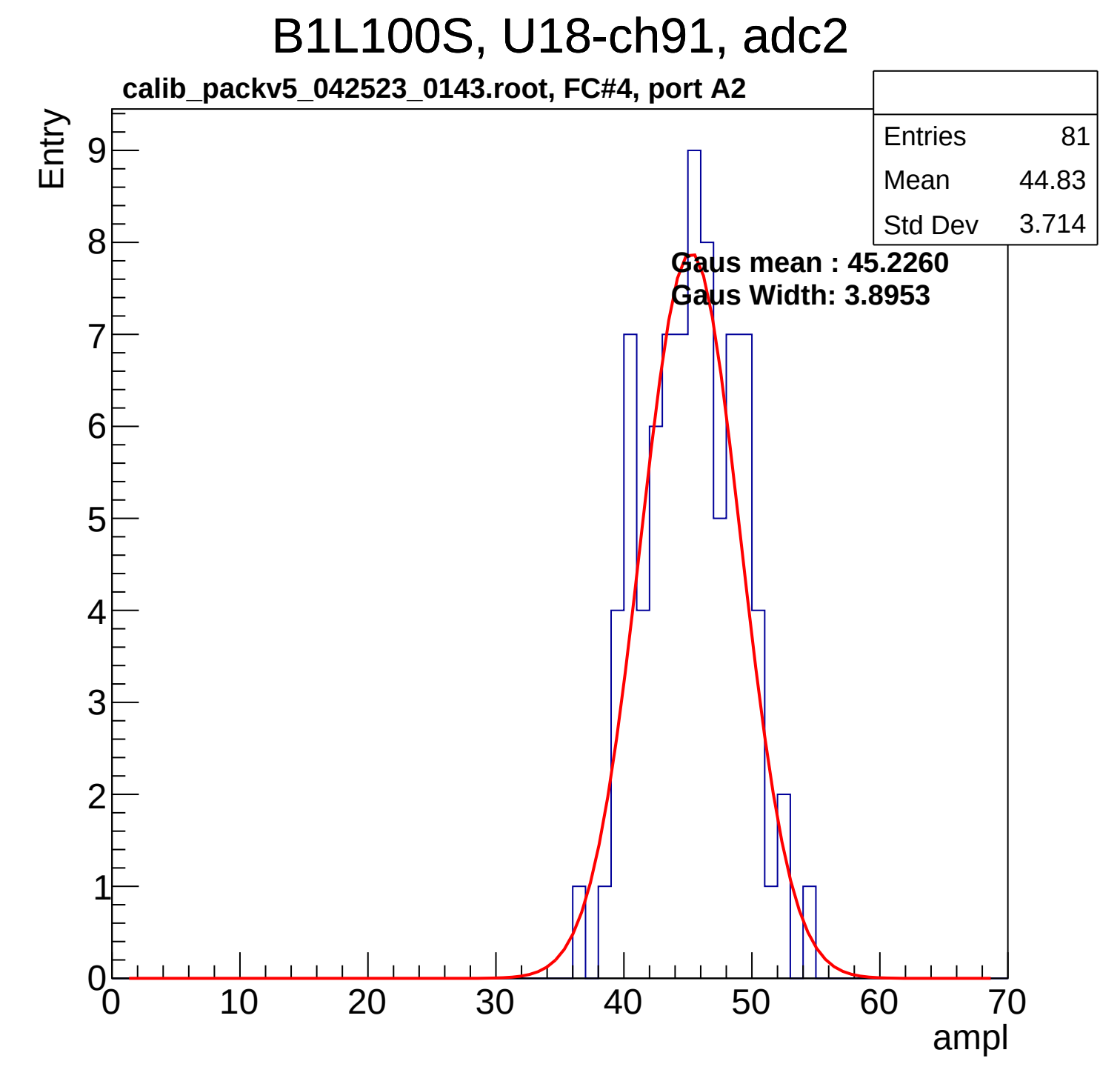

B1L100S, U18-ch90, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 26
Mean 60.46
Std Dev 2.223
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

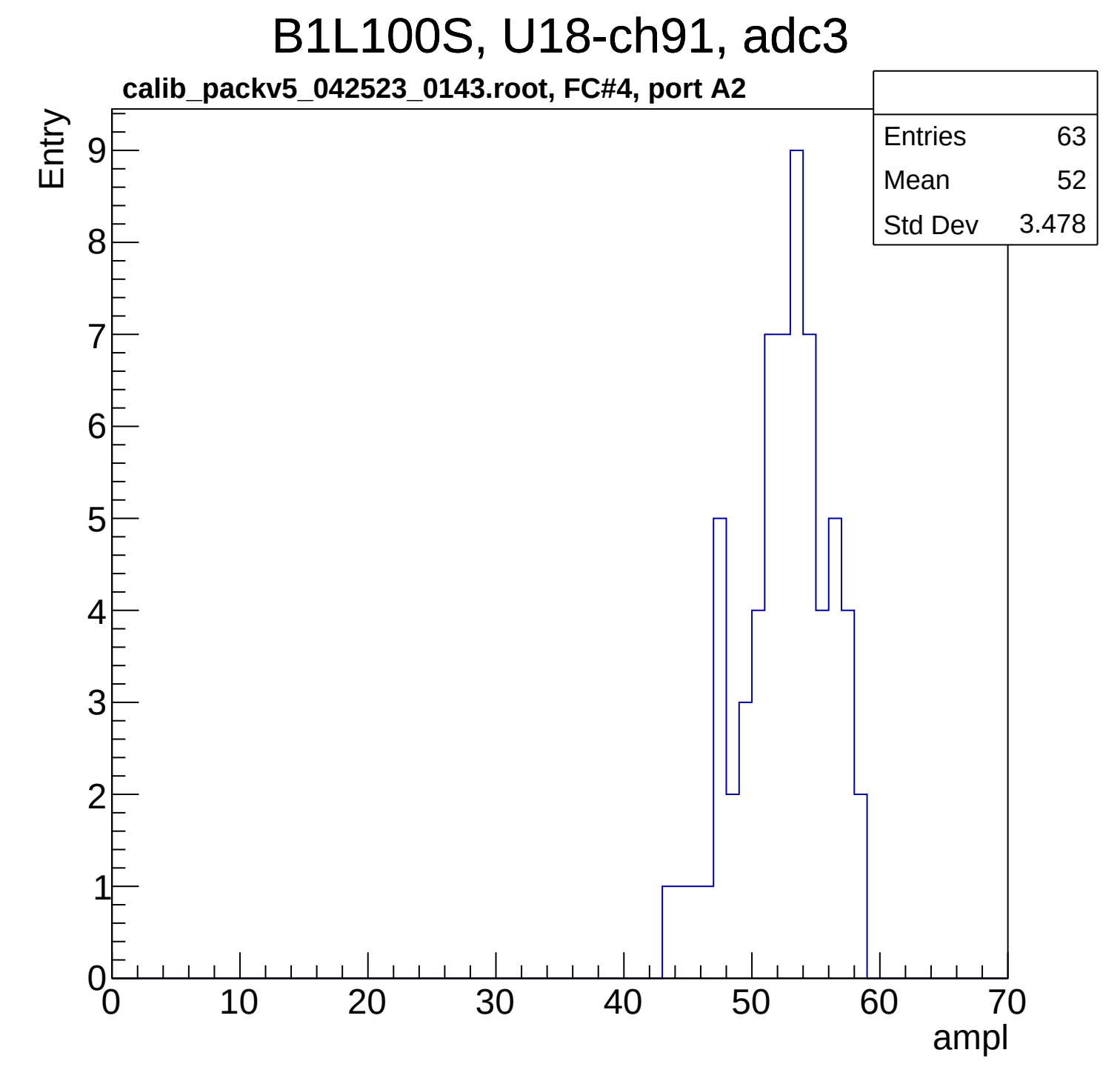

B1L100S, U18-ch90, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

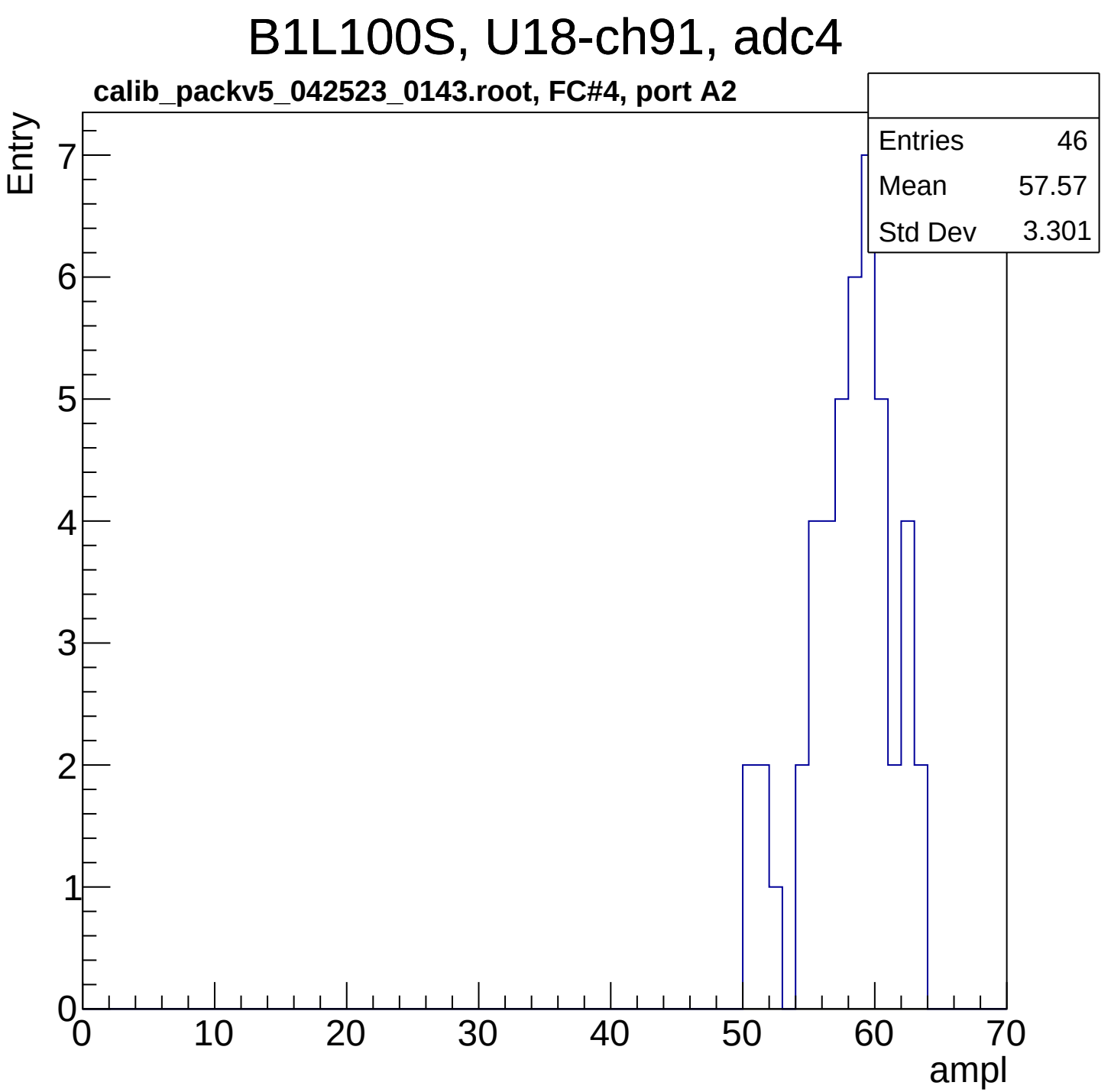

B1L100S, U18-ch90, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

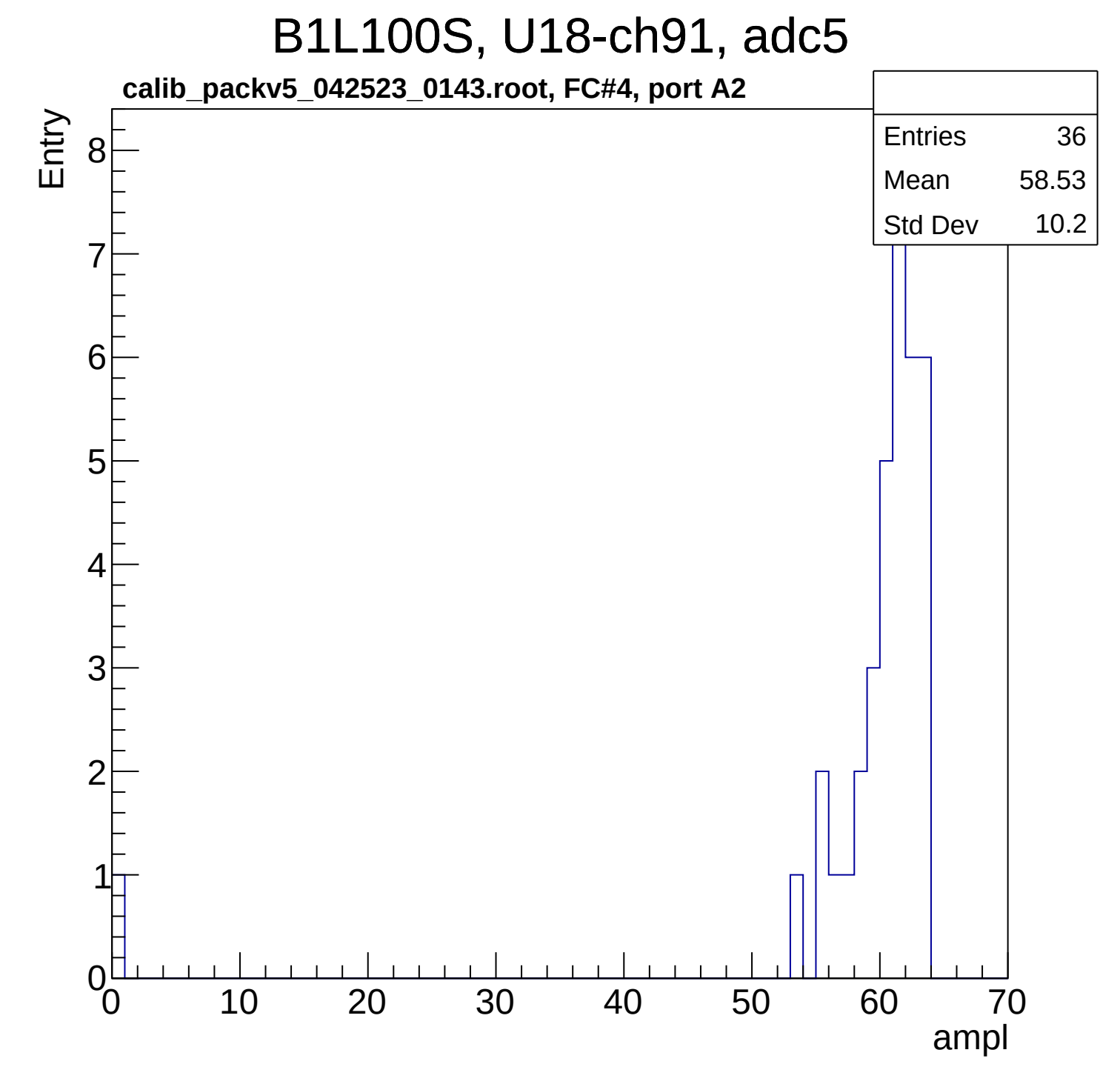

B1L100S, U18-ch91, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 31.46
Std Dev 5.047
Gaus mean : 32.4586
Gaus Width: 3.7377
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

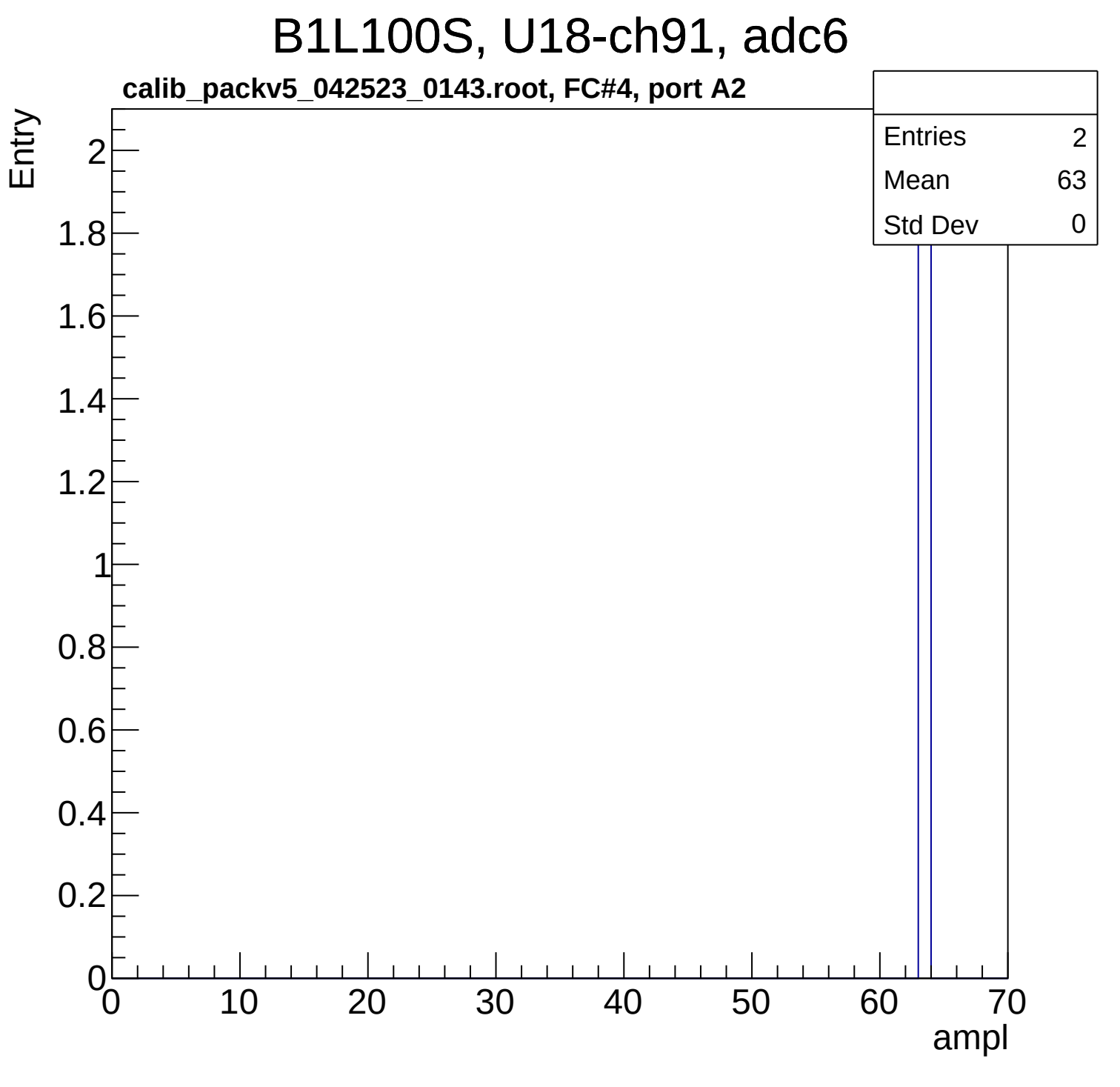

B1L100S, U18-ch91, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 38.28
Std Dev 3.778
Gaus mean : 38.9043
Gaus Width: 4.4358
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

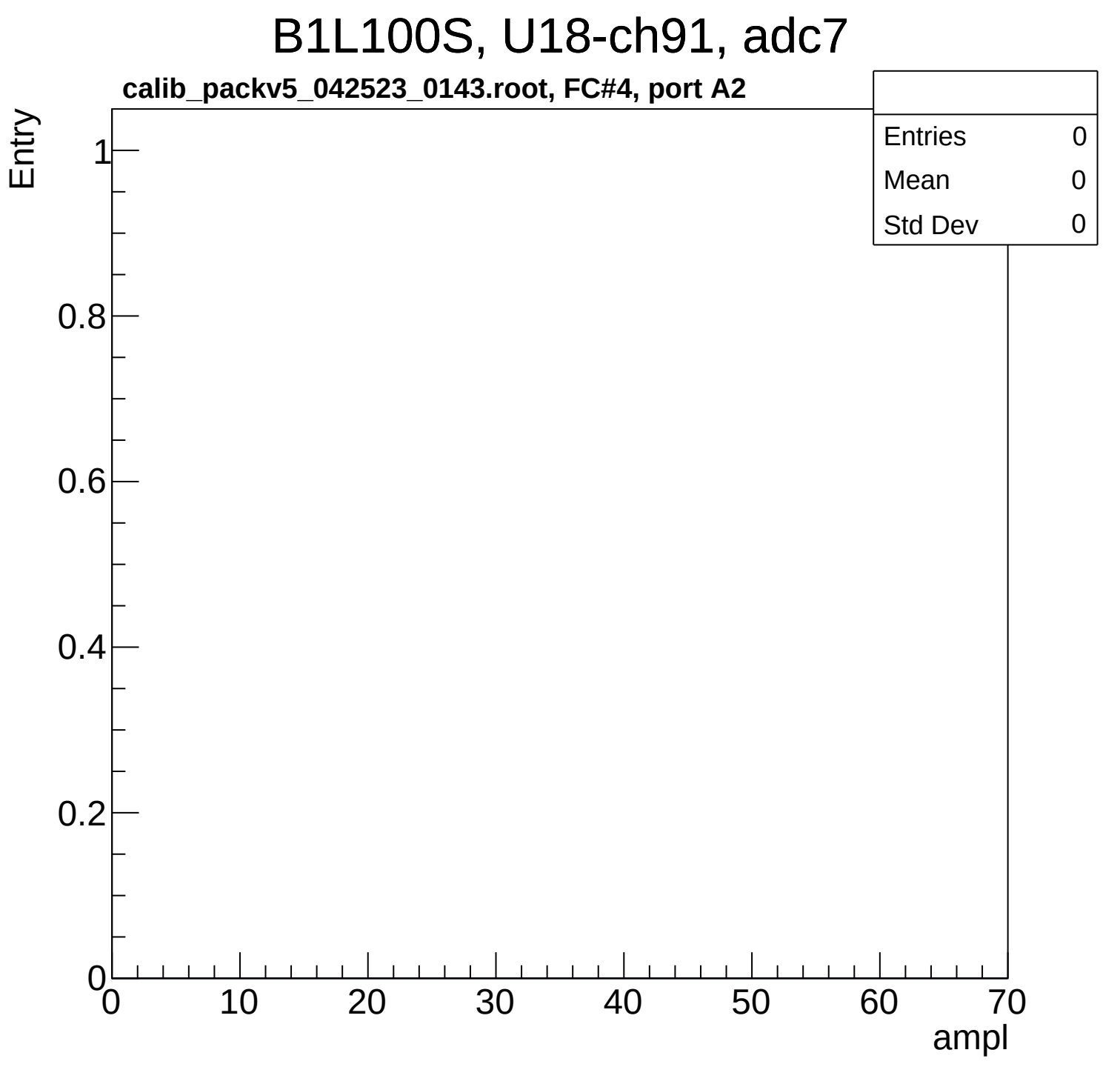

B1L100S, U18-ch91, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 44.83
Std Dev 3.714
Gaus mean : 45.2260
Gaus Width: 3.8953
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

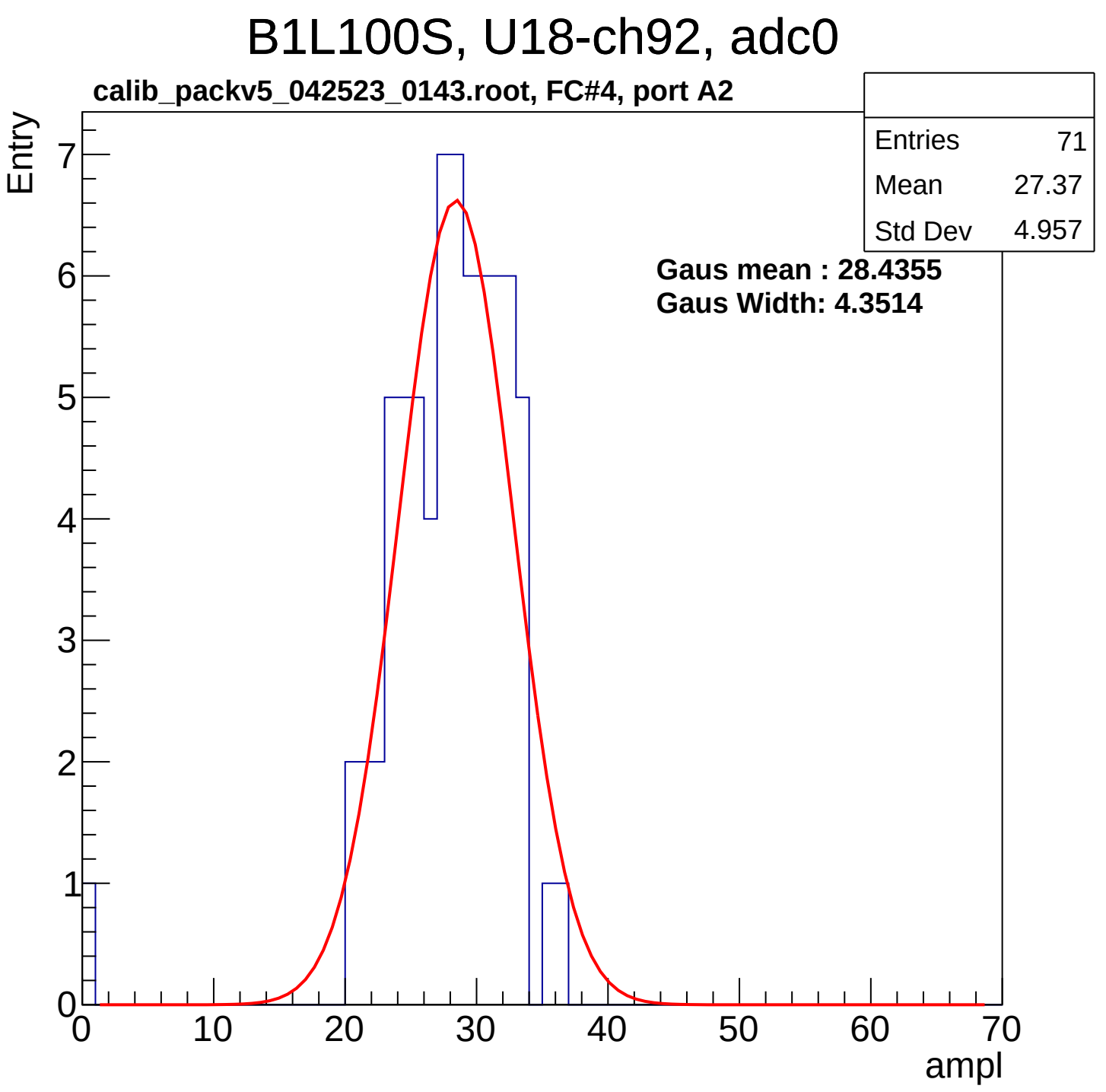

B1L100S, U18-ch91, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 52
Std Dev 3.478
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

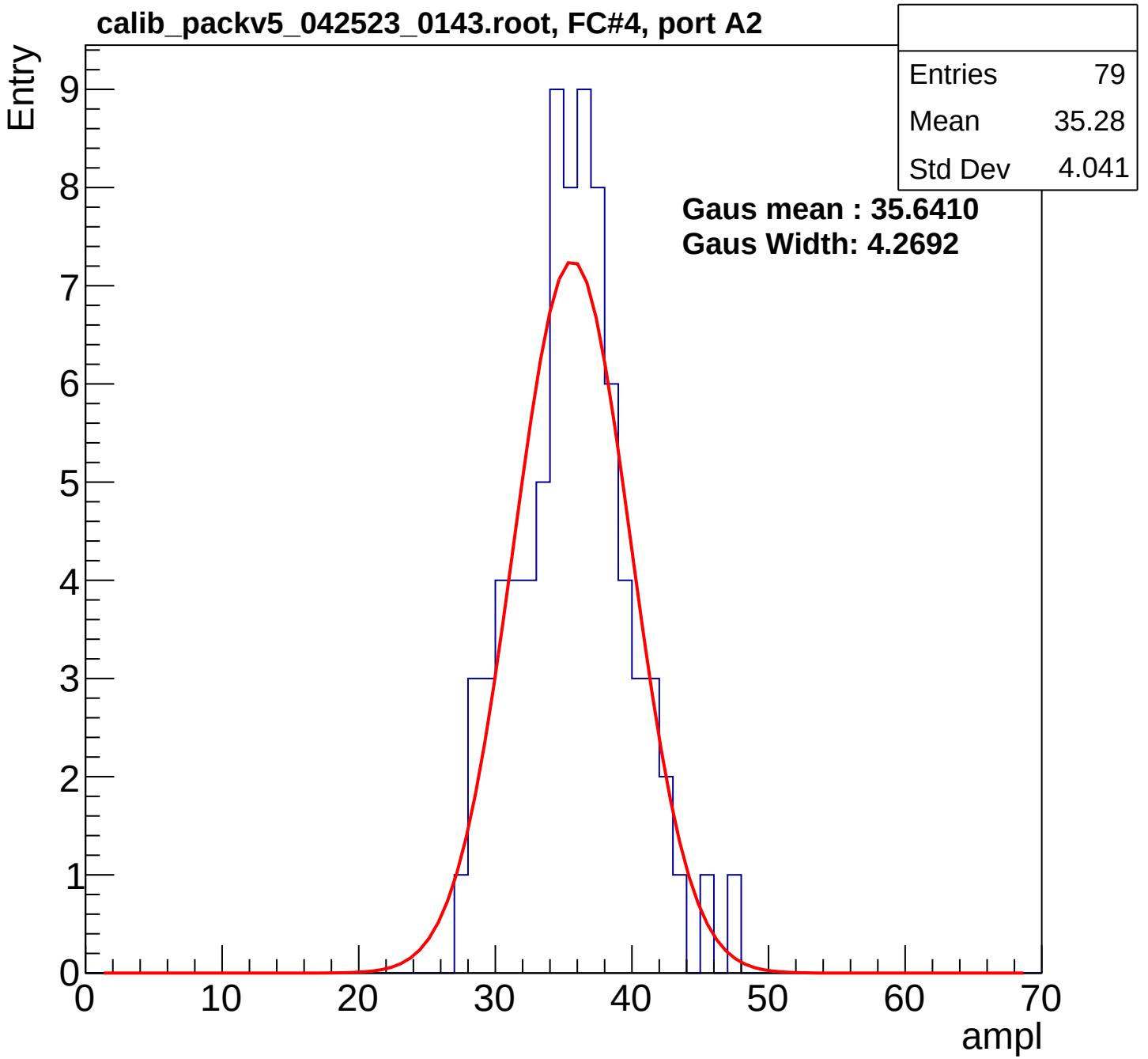

B1L100S, U18-ch91, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 57.57
Std Dev 3.301
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

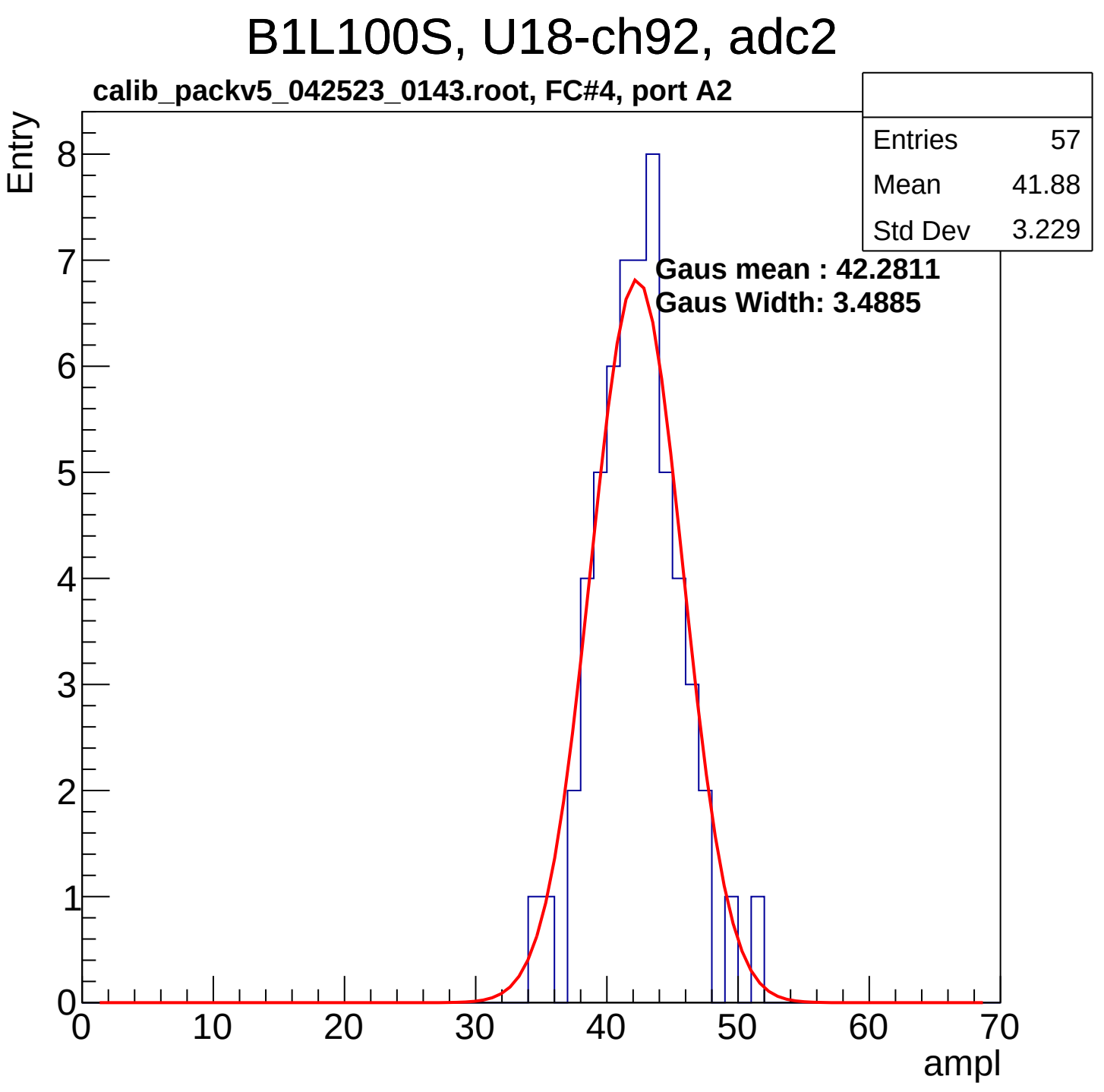

B1L100S, U18-ch91, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 36
Mean 58.53
Std Dev 10.2
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

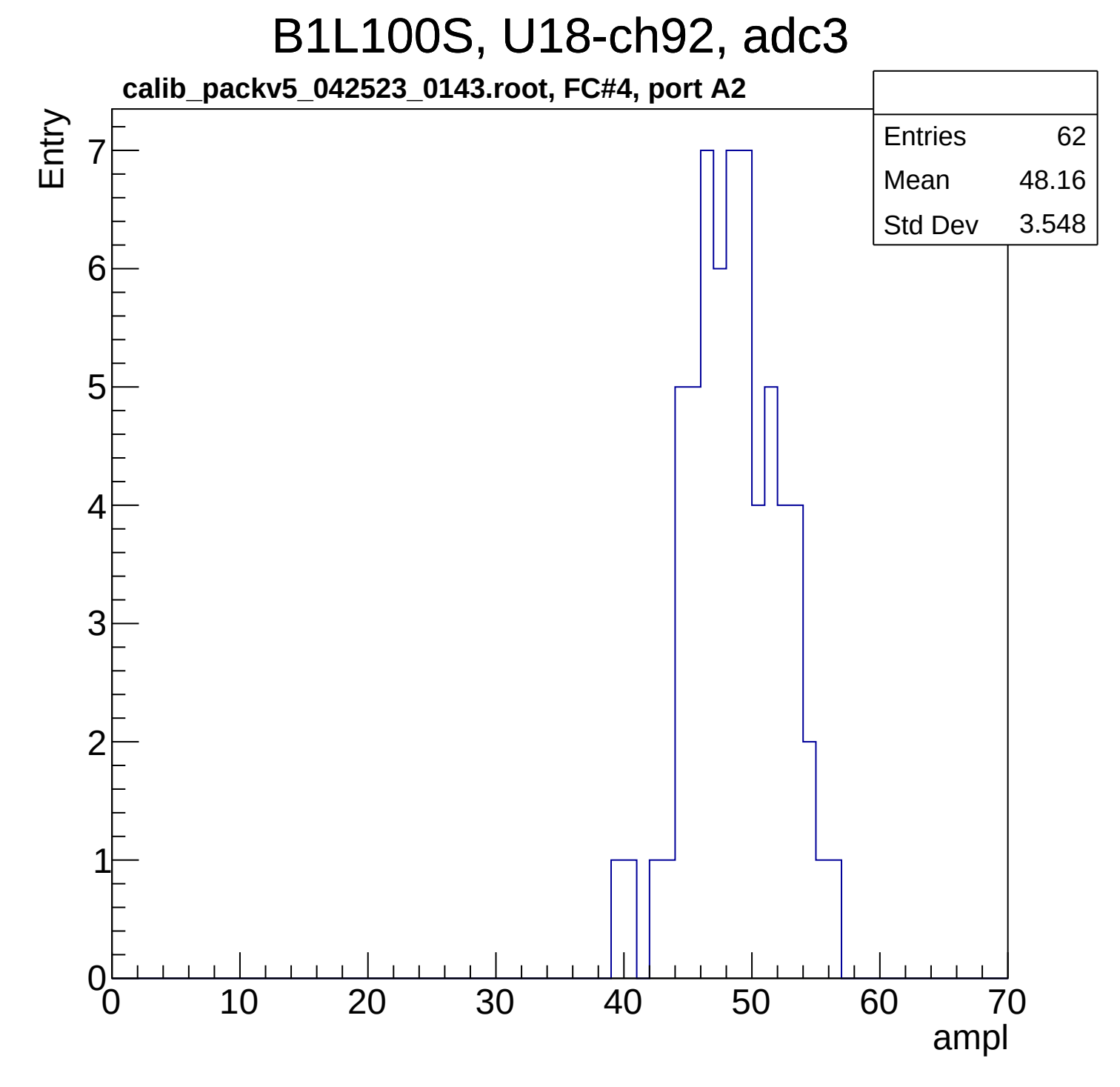

B1L100S, U18-ch91, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

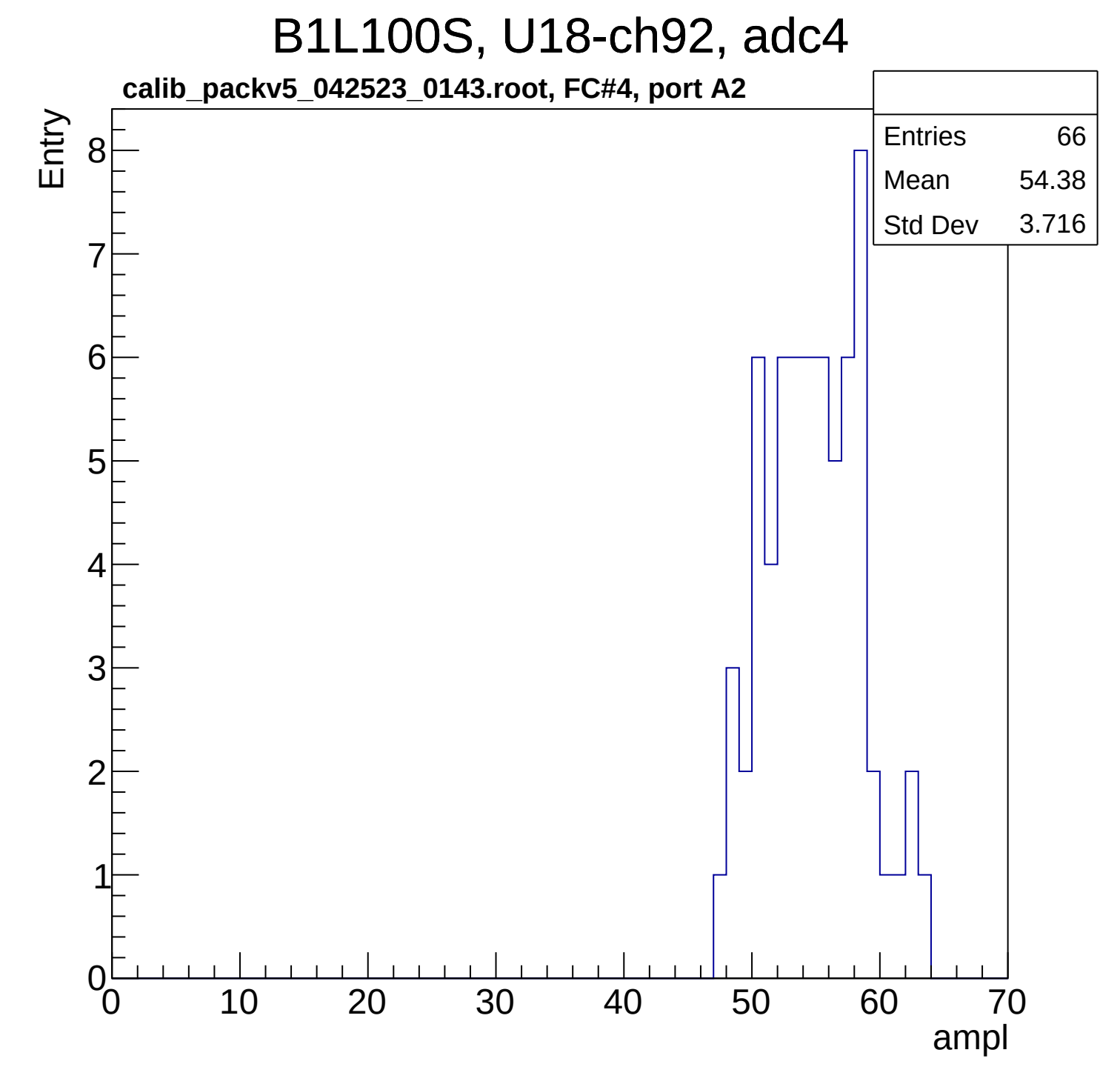

B1L100S, U18-ch91, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

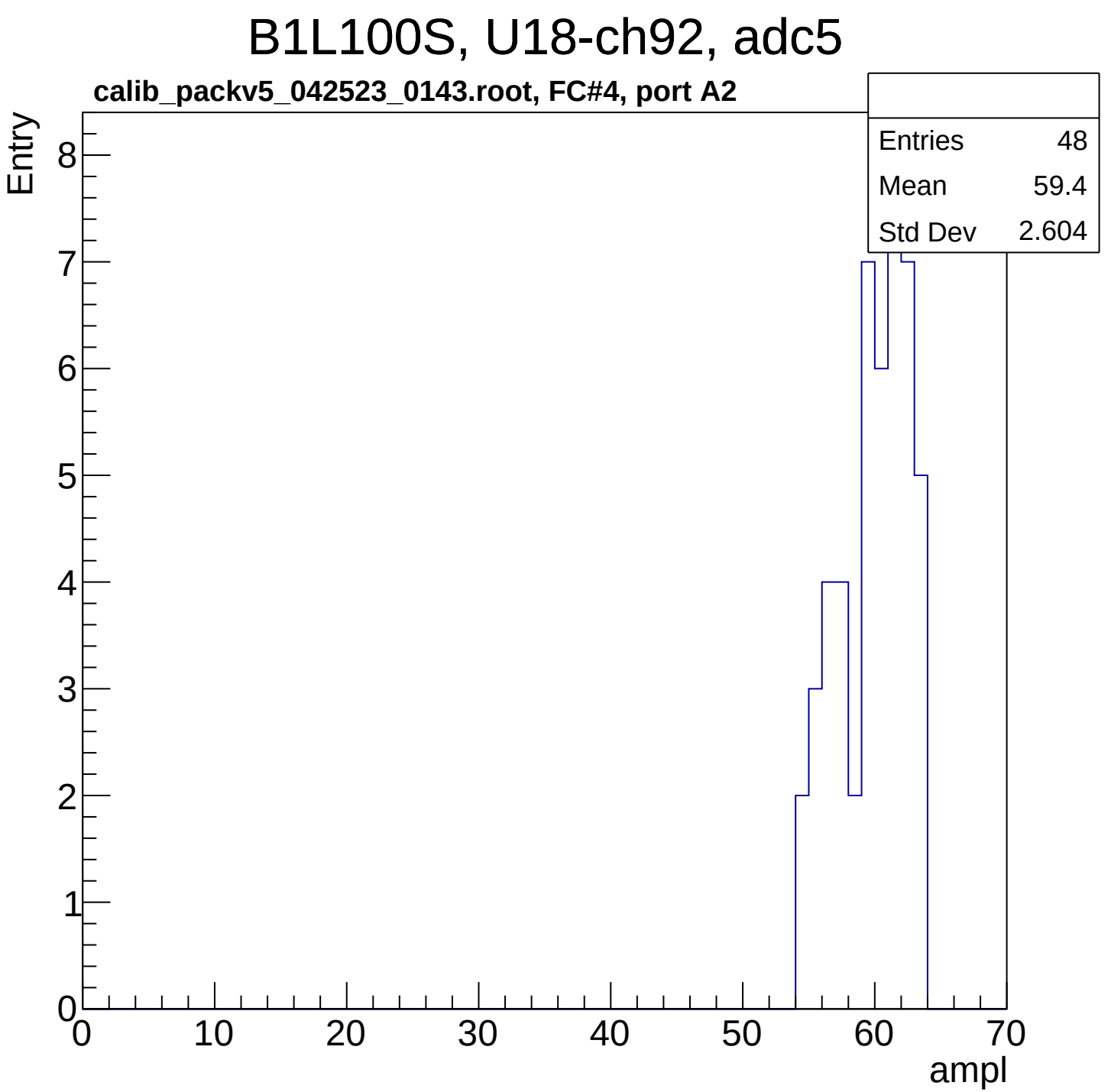

B1L100S, U18-ch92, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 27.37
Std Dev 4.957
Gaus mean : 28.4355
Gaus Width: 4.3514
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

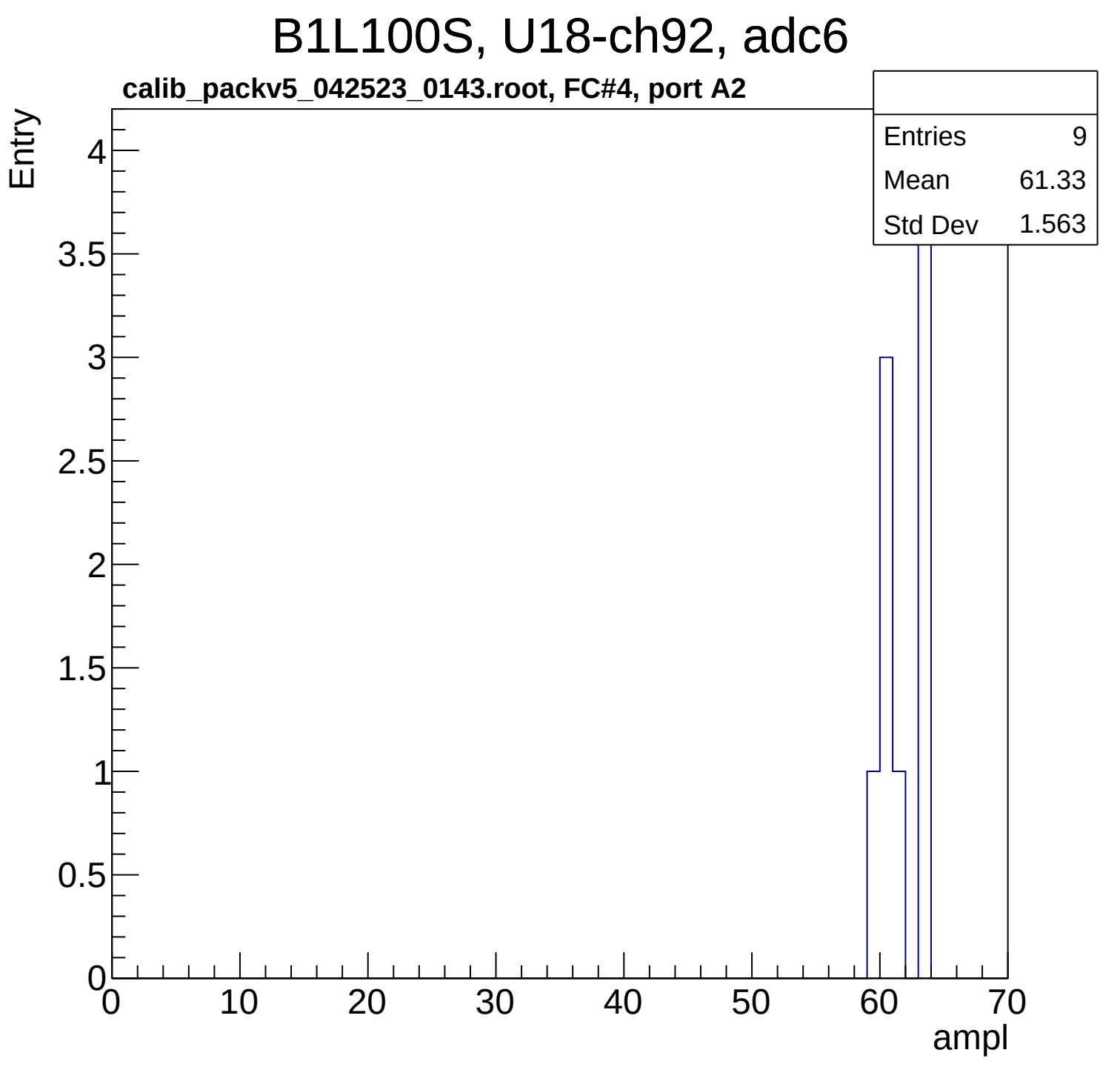

B1L100S, U18-ch92, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 35.28
Std Dev 4.041
Gaus mean : 35.6410
Gaus Width: 4.2692
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

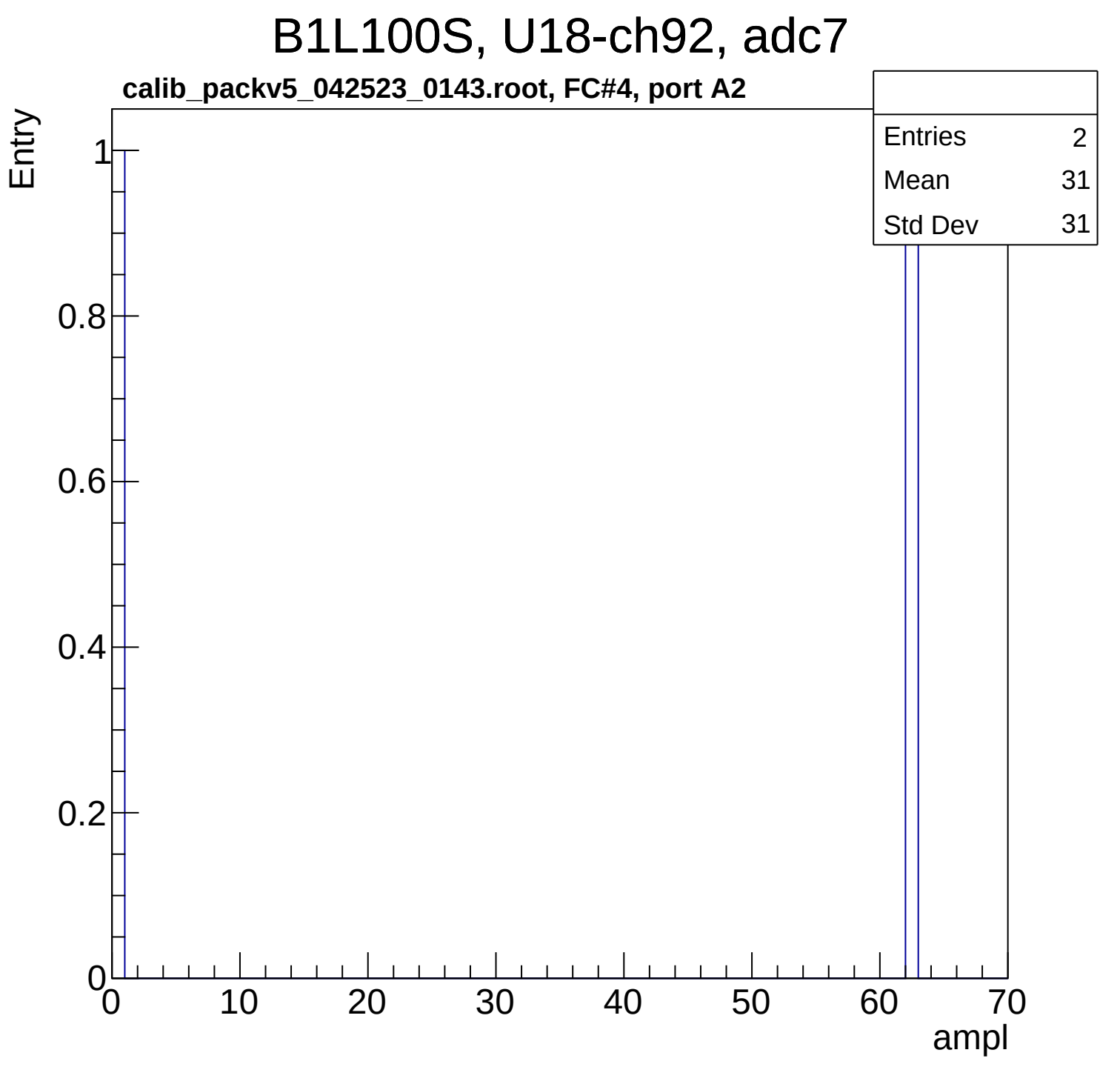

B1L100S, U18-ch92, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 41.88
Std Dev 3.229
Gaus mean : 42.2811
Gaus Width: 3.4885
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

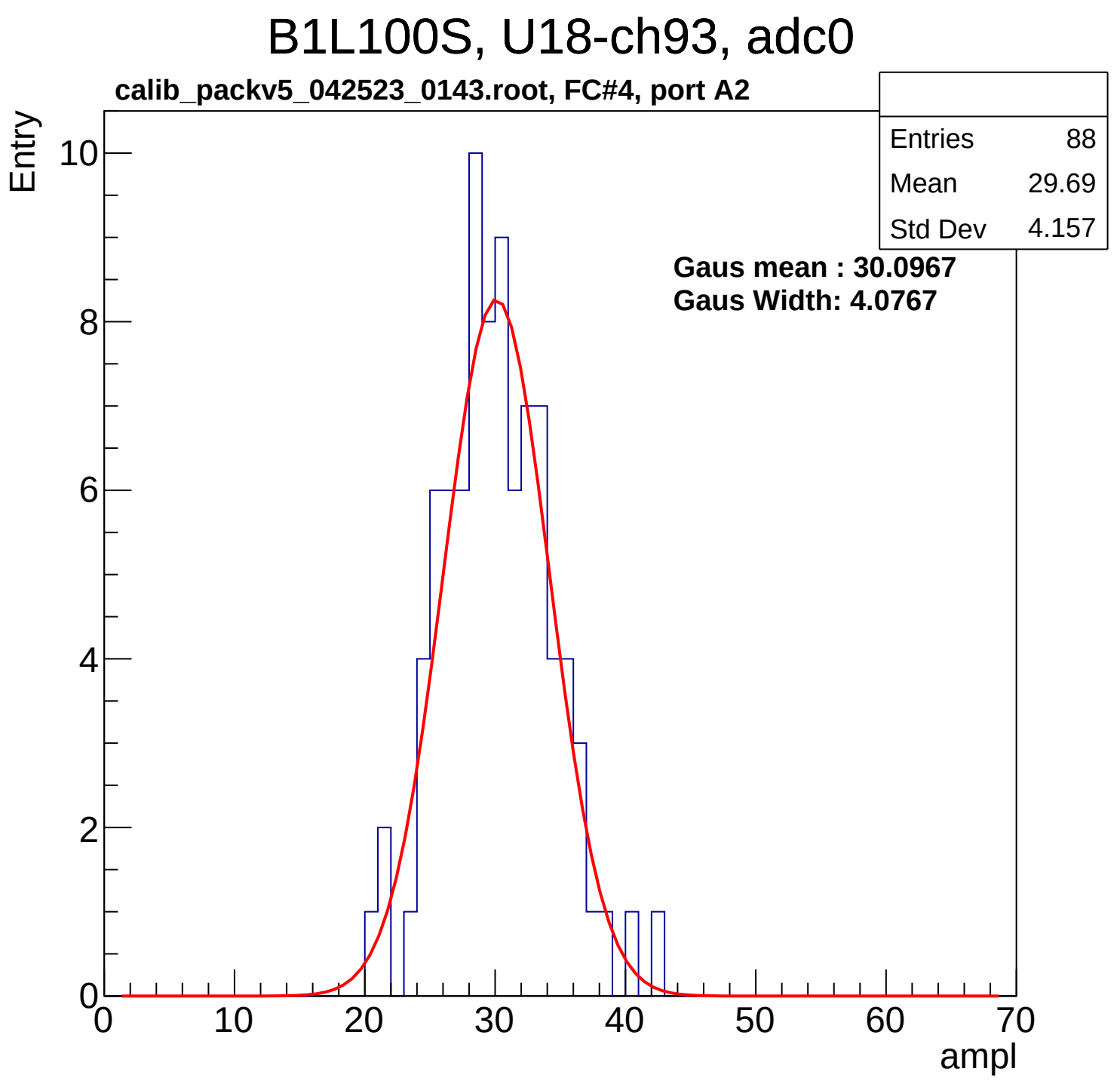

B1L100S, U18-ch92, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 48.16
Std Dev 3.548
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

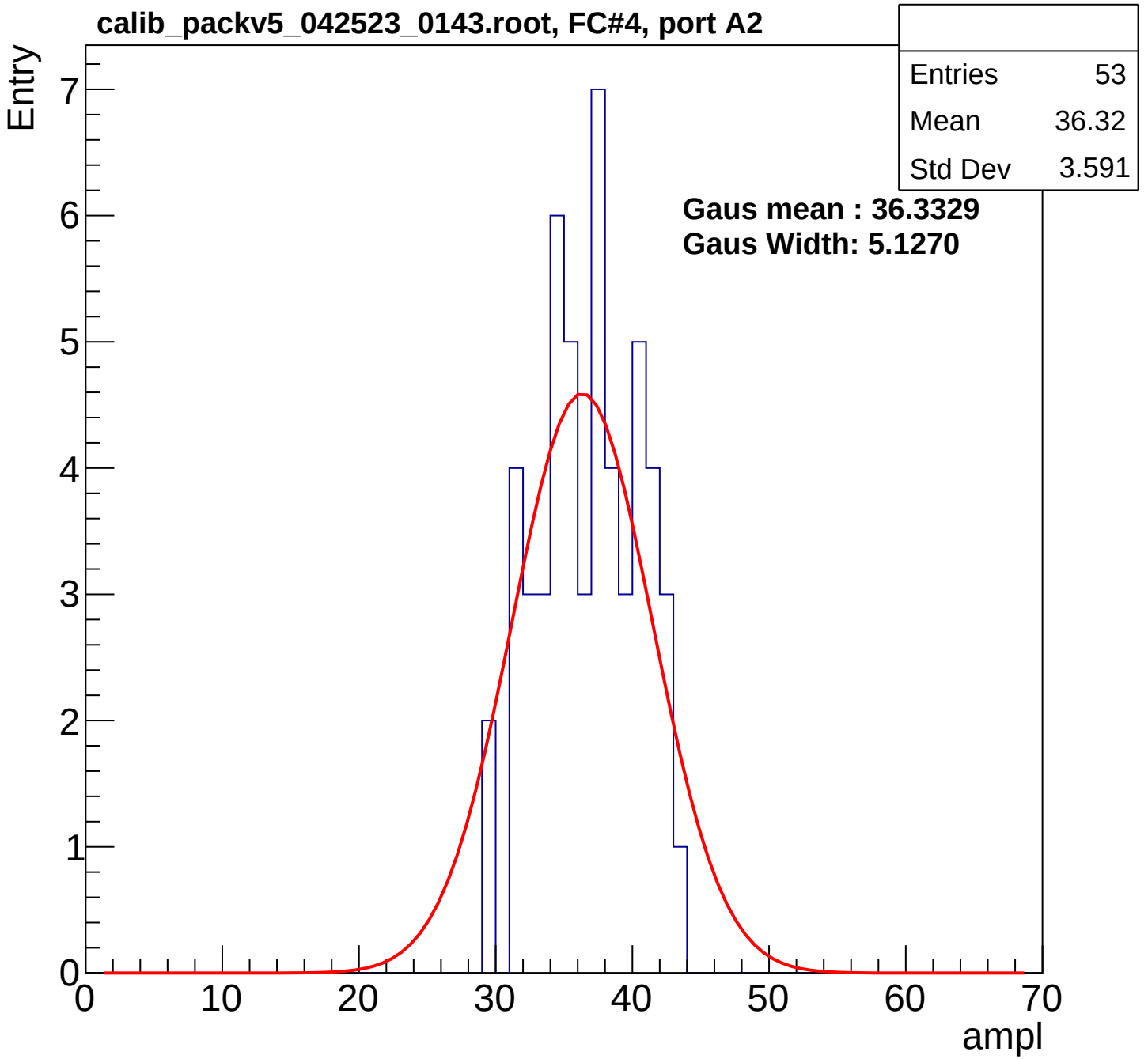

B1L100S, U18-ch92, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 54.38
Std Dev 3.716
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

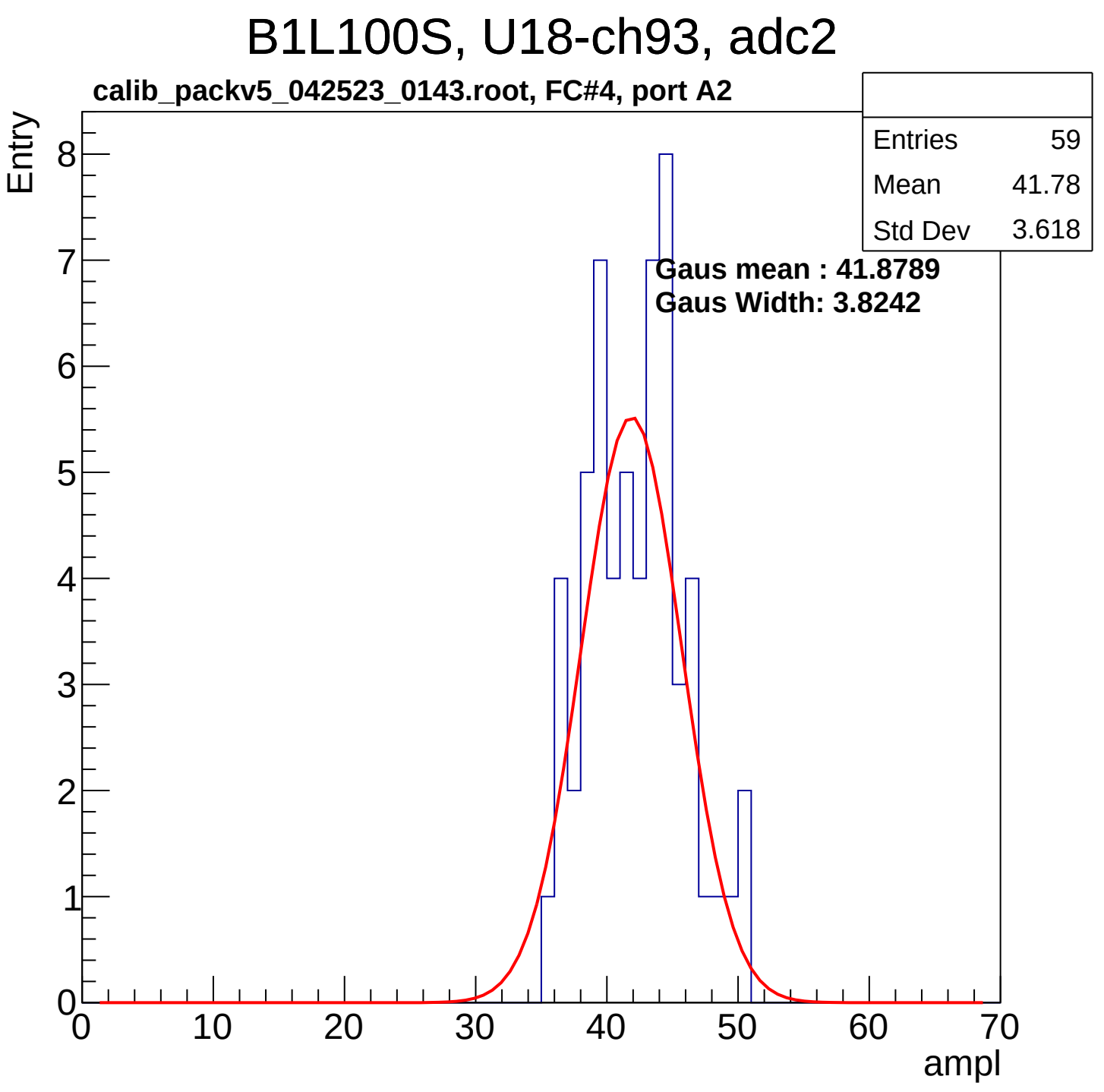

B1L100S, U18-ch92, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 59.4
Std Dev 2.604
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

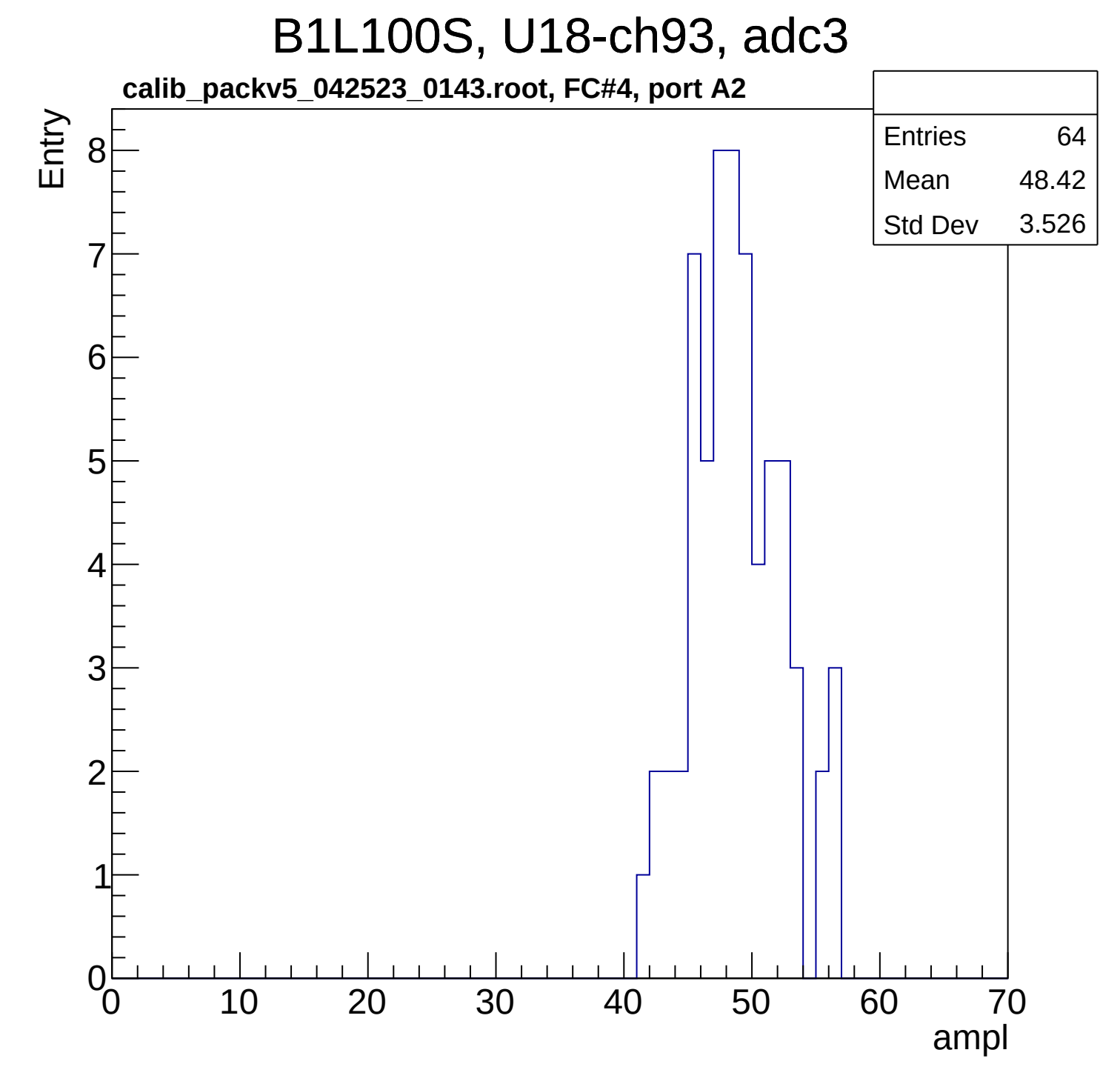

B1L100S, U18-ch92, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 61.33
Std Dev 1.563
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

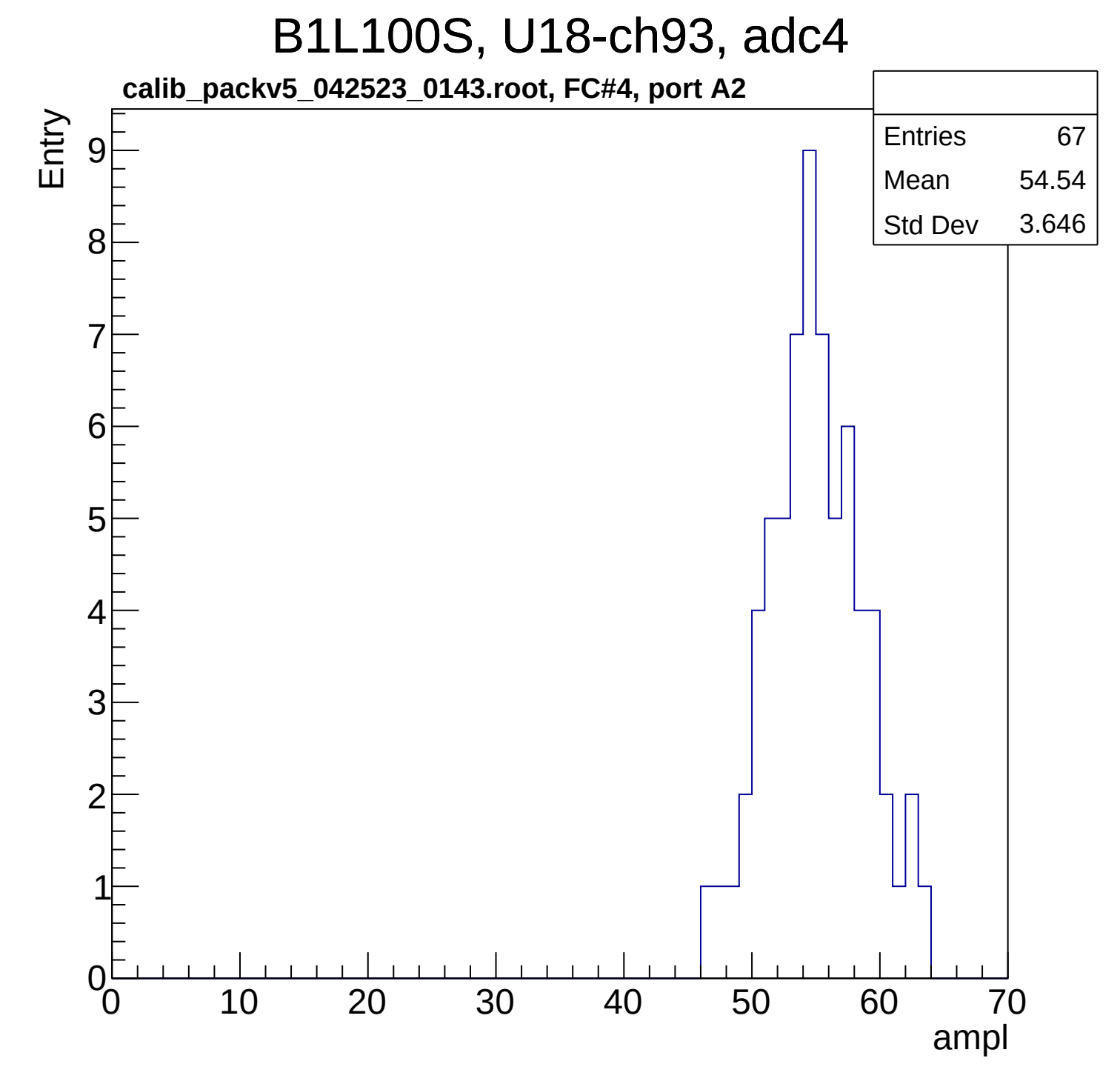

B1L100S, U18-ch92, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 31
Std Dev 31
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

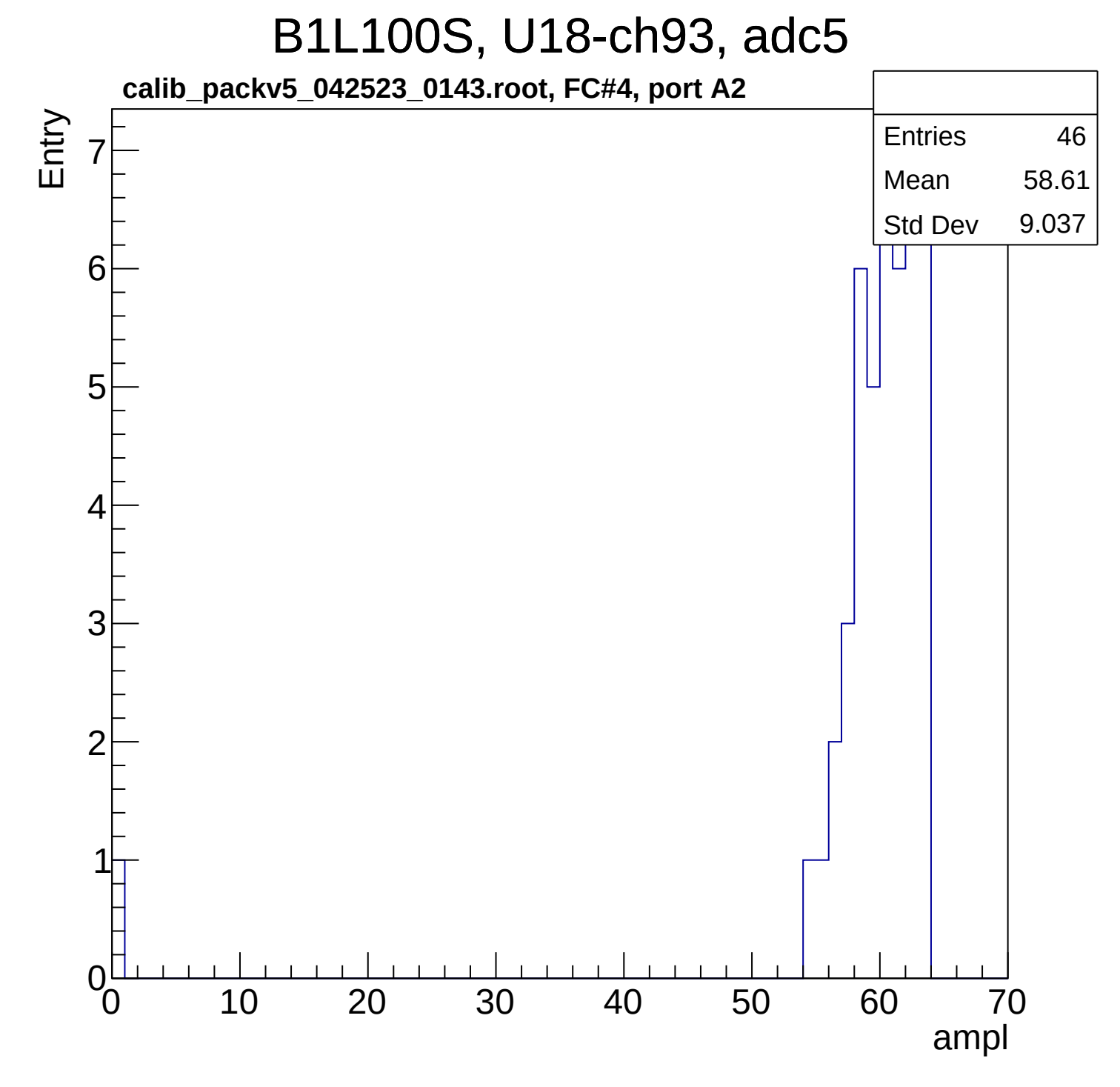

B1L100S, U18-ch93, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 88
Mean 29.69
Std Dev 4.157
Gaus mean : 30.0967
Gaus Width: 4.0767
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

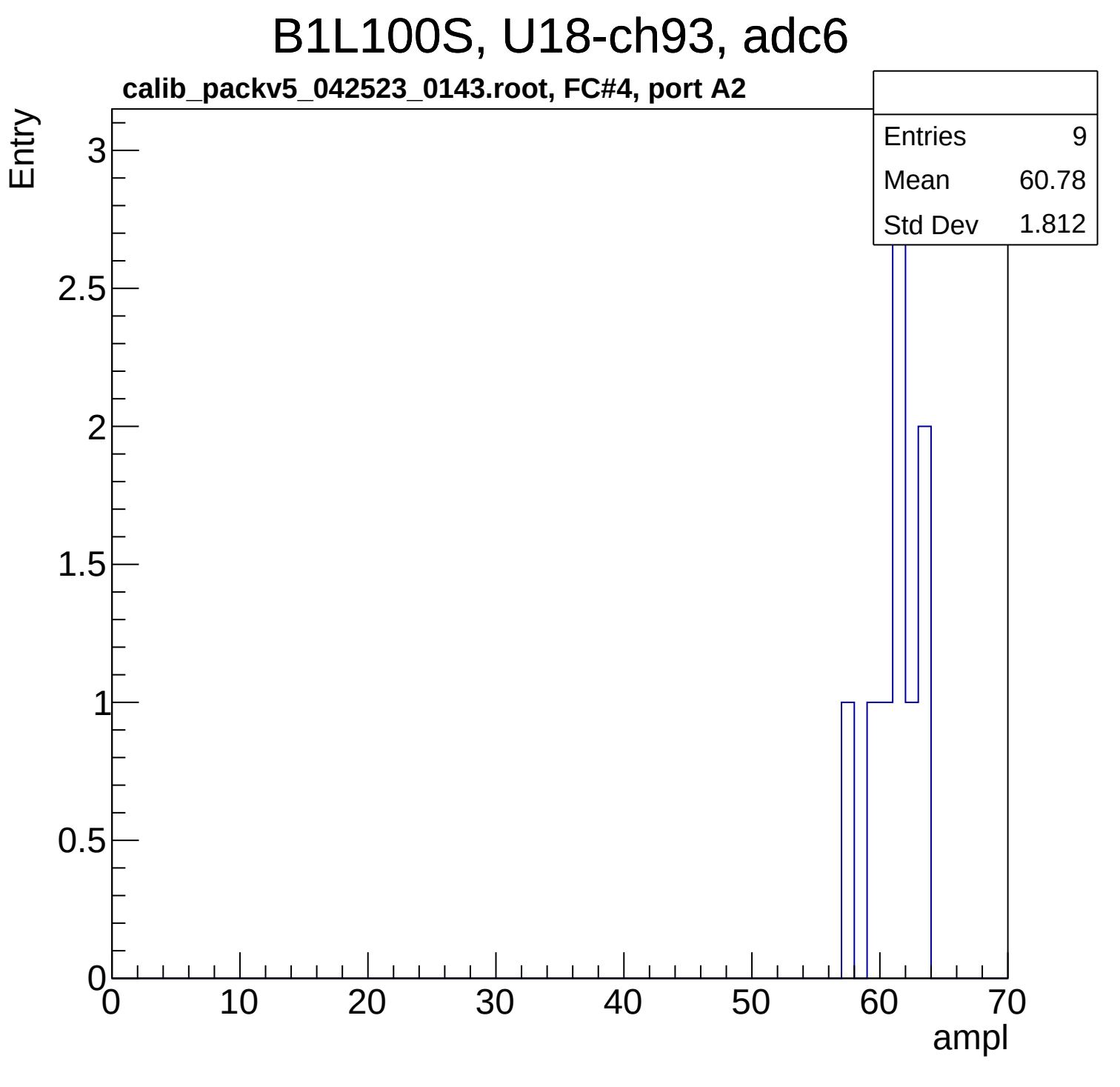

B1L100S, U18-ch93, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 36.32
Std Dev 3.591
Gaus mean : 36.3329
Gaus Width: 5.1270
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

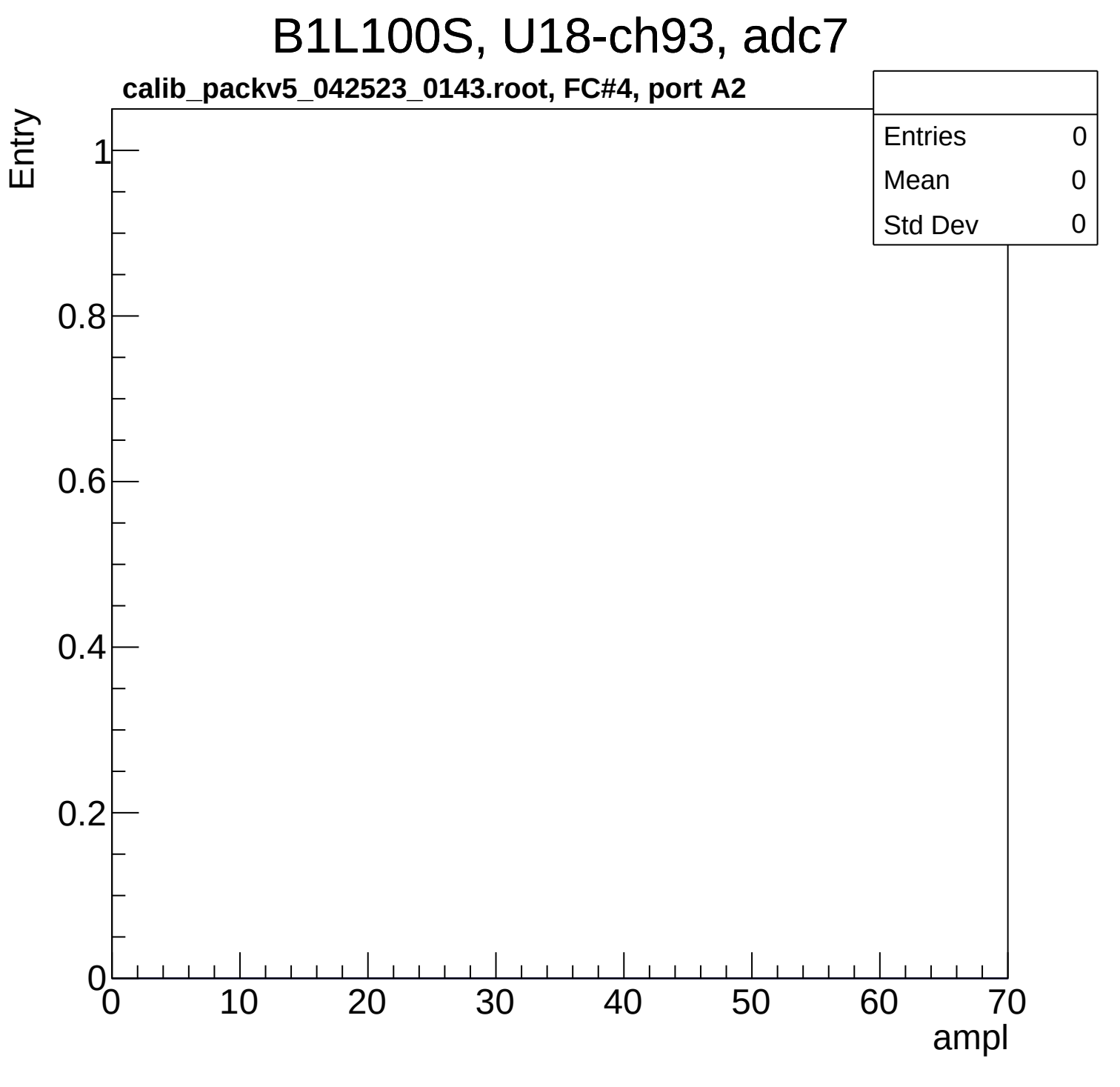

B1L100S, U18-ch93, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 41.78
Std Dev 3.618
Gaus mean : 41.8789
Gaus Width: 3.8242
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

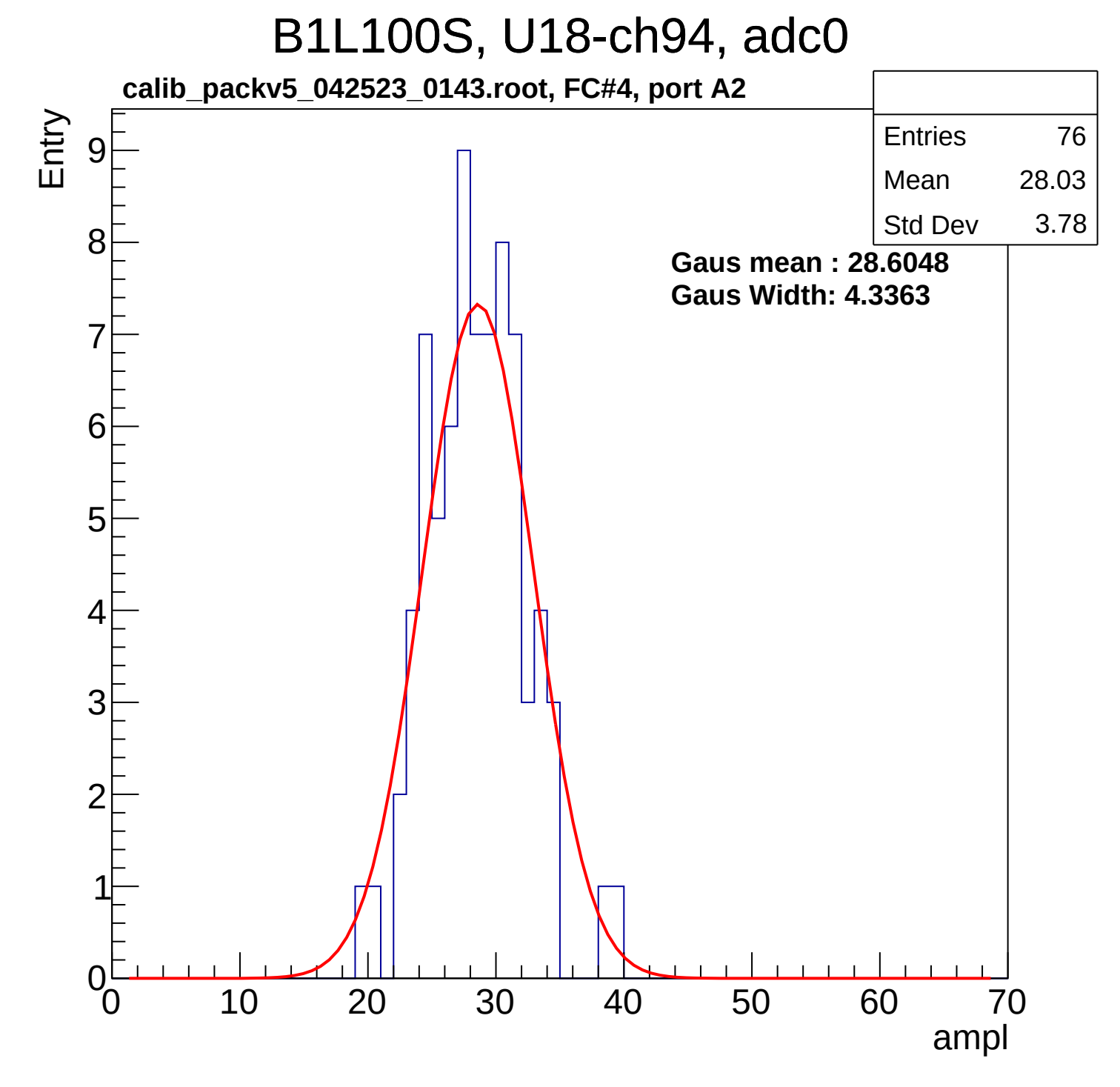

B1L100S, U18-ch93, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 48.42
Std Dev 3.526
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

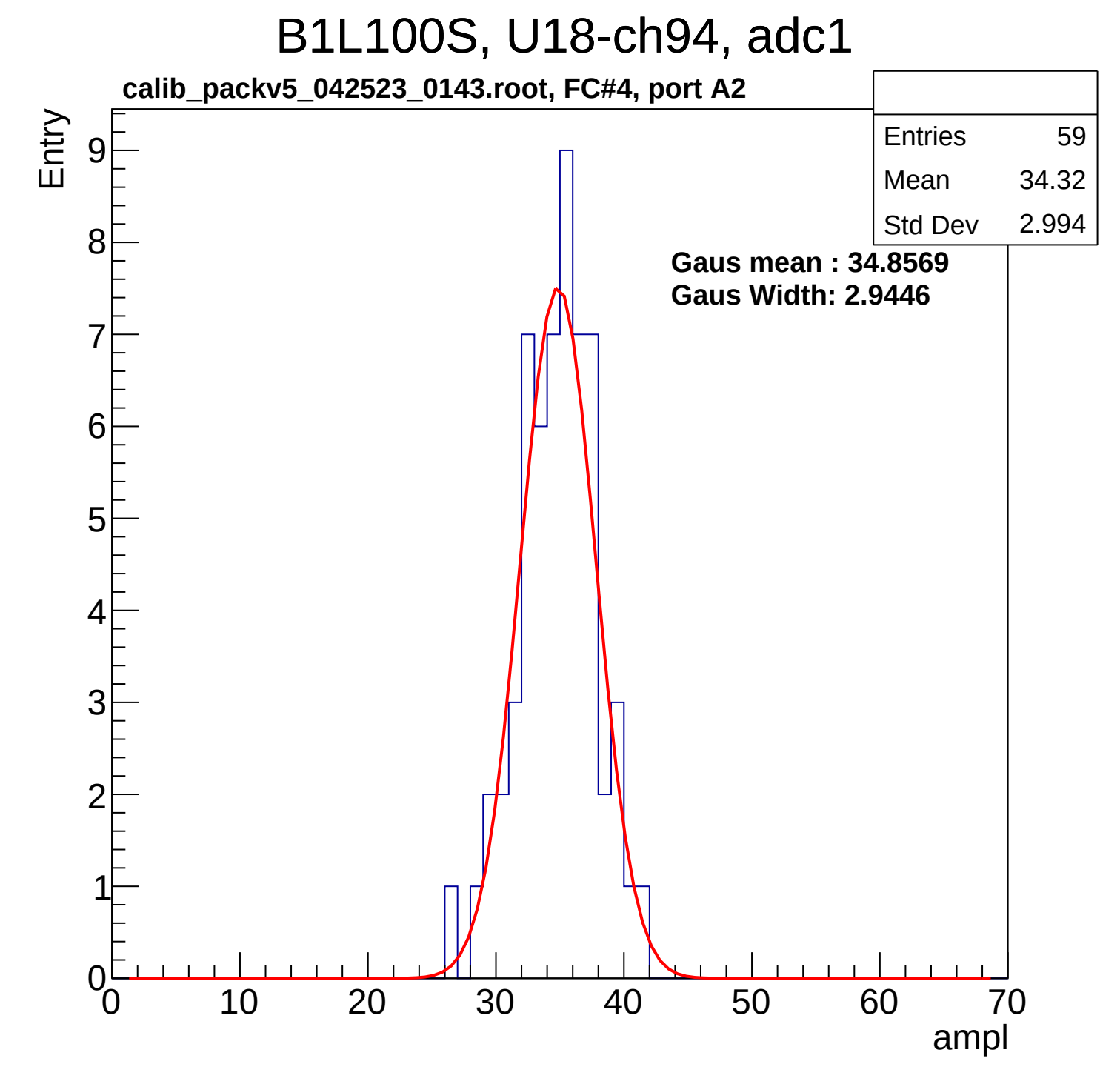

B1L100S, U18-ch93, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 54.54
Std Dev 3.646
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

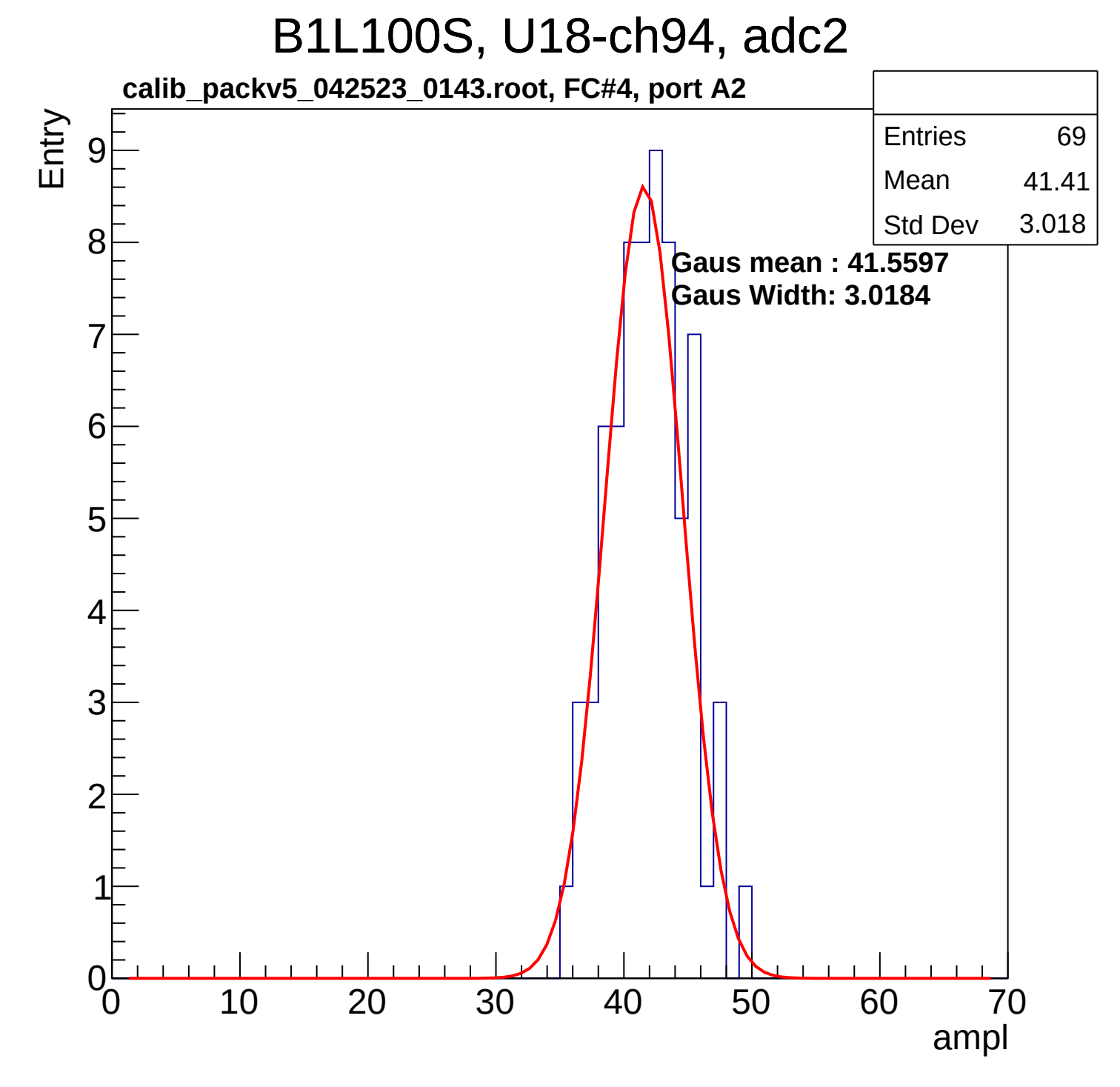

B1L100S, U18-ch93, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 58.61
Std Dev 9.037
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

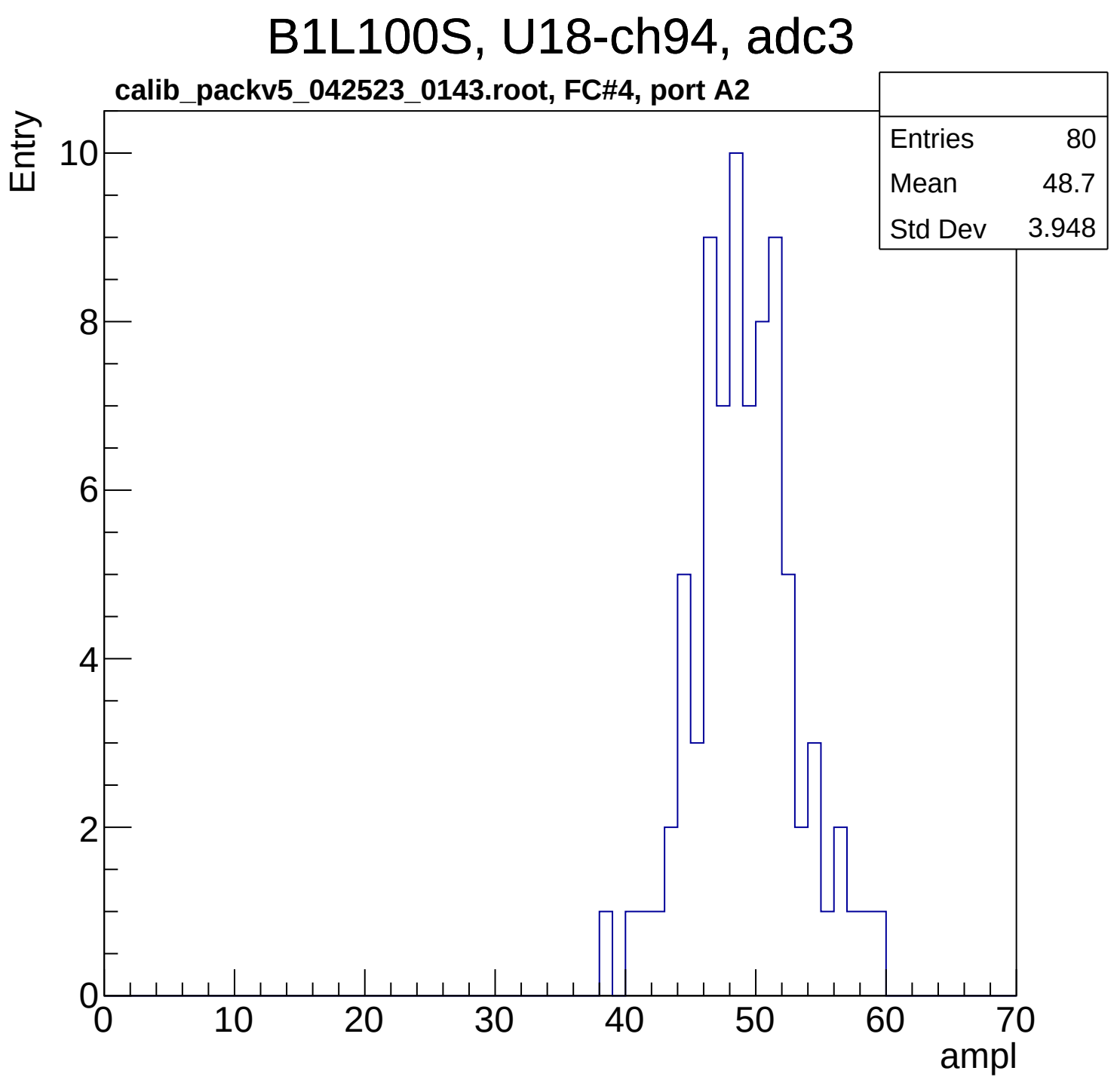

B1L100S, U18-ch93, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 60.78
Std Dev 1.812
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

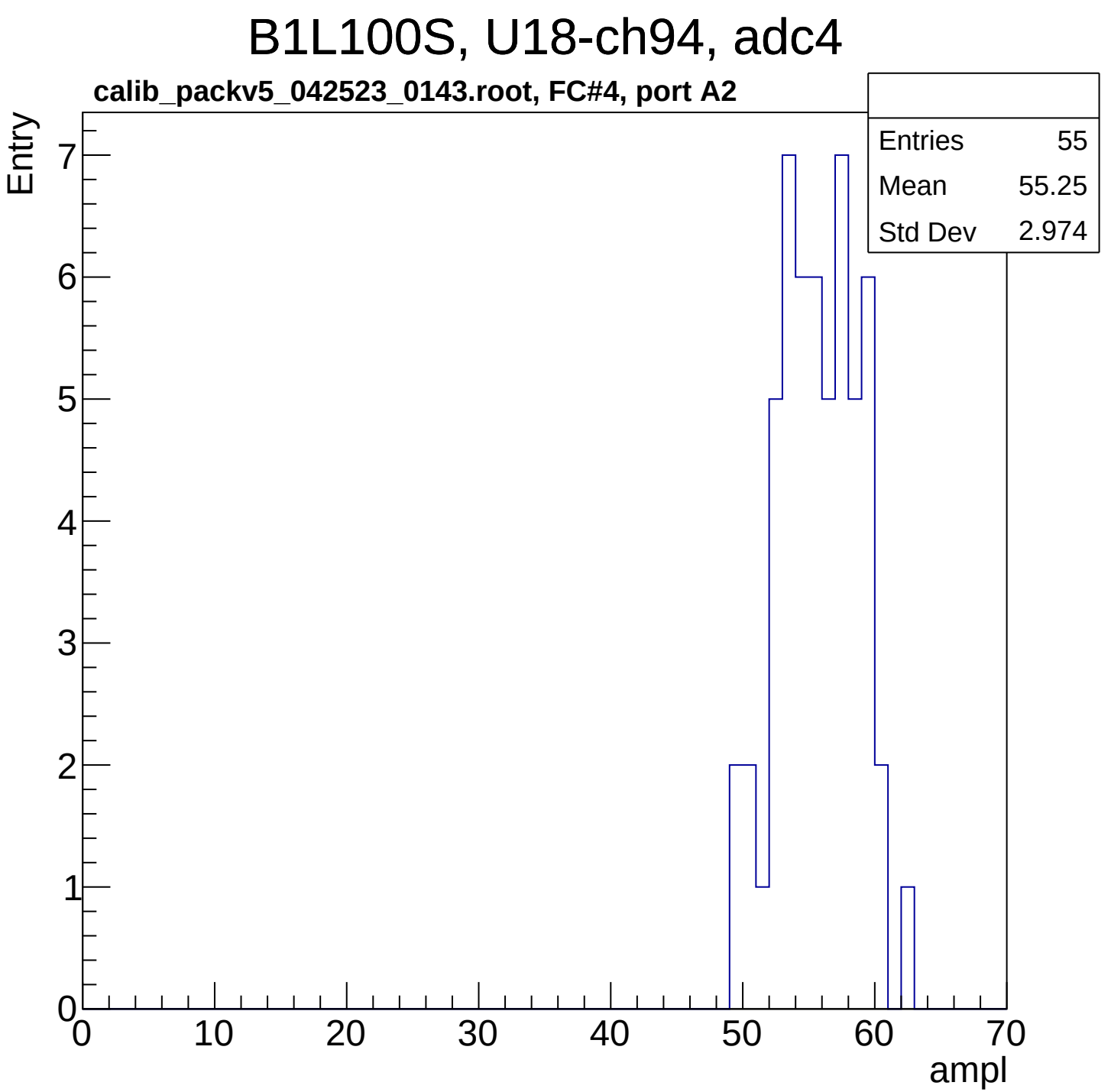

B1L100S, U18-ch93, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

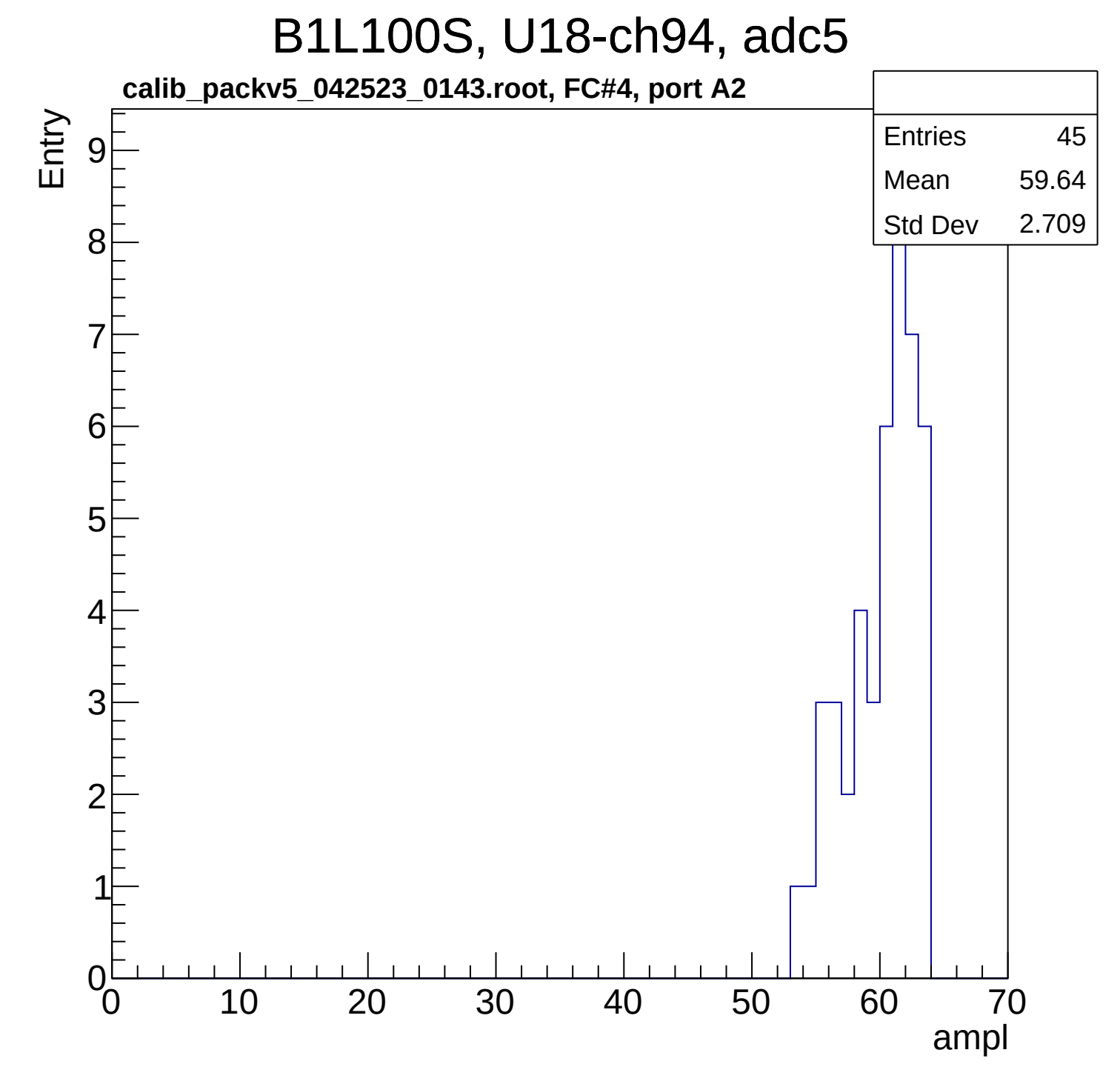

B1L100S, U18-ch94, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 28.03
Std Dev 3.78
Gaus mean : 28.6048
Gaus Width: 4.3363
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

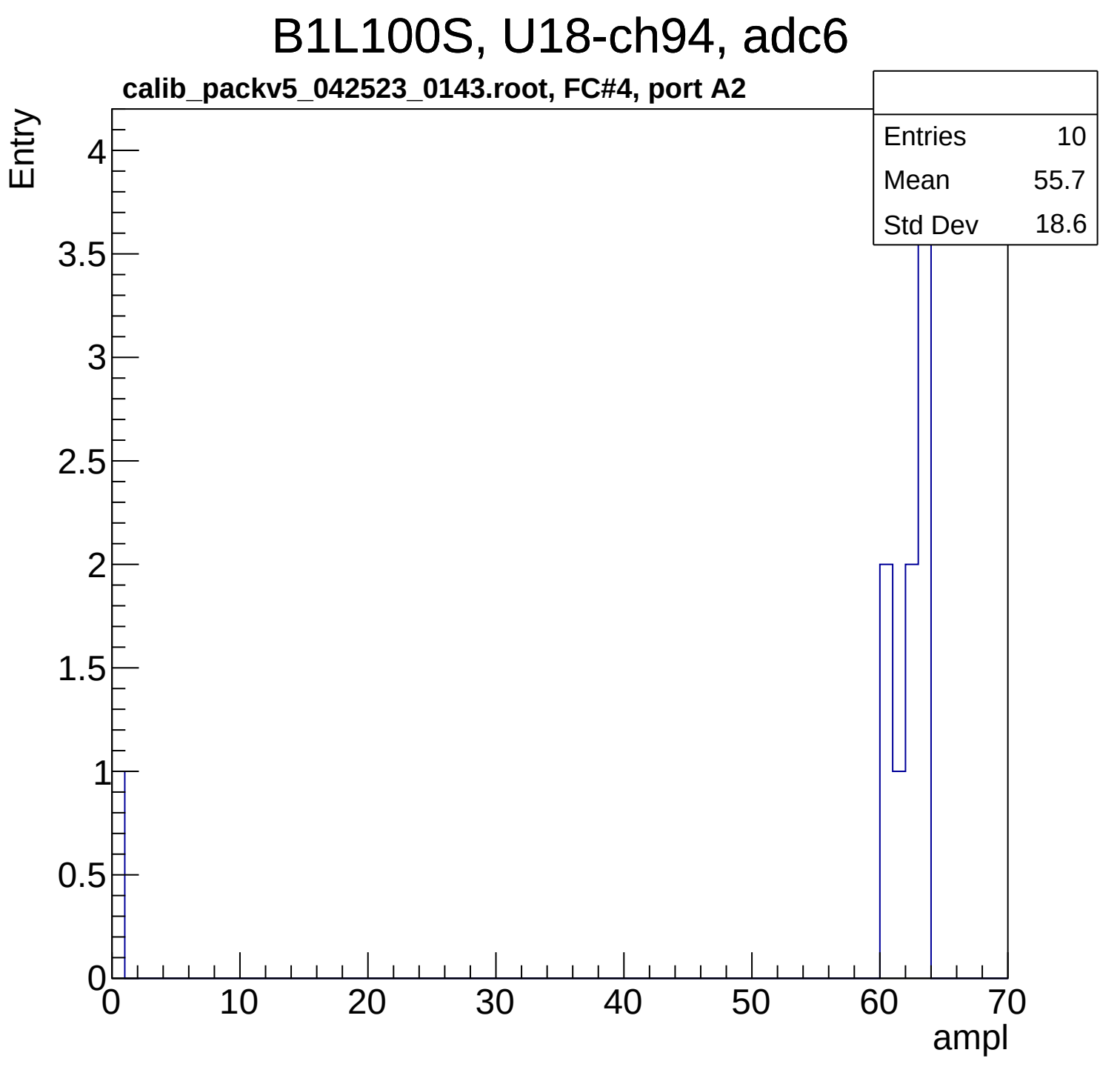

B1L100S, U18-ch94, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 34.32
Std Dev 2.994
Gaus mean : 34.8569
Gaus Width: 2.9446
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

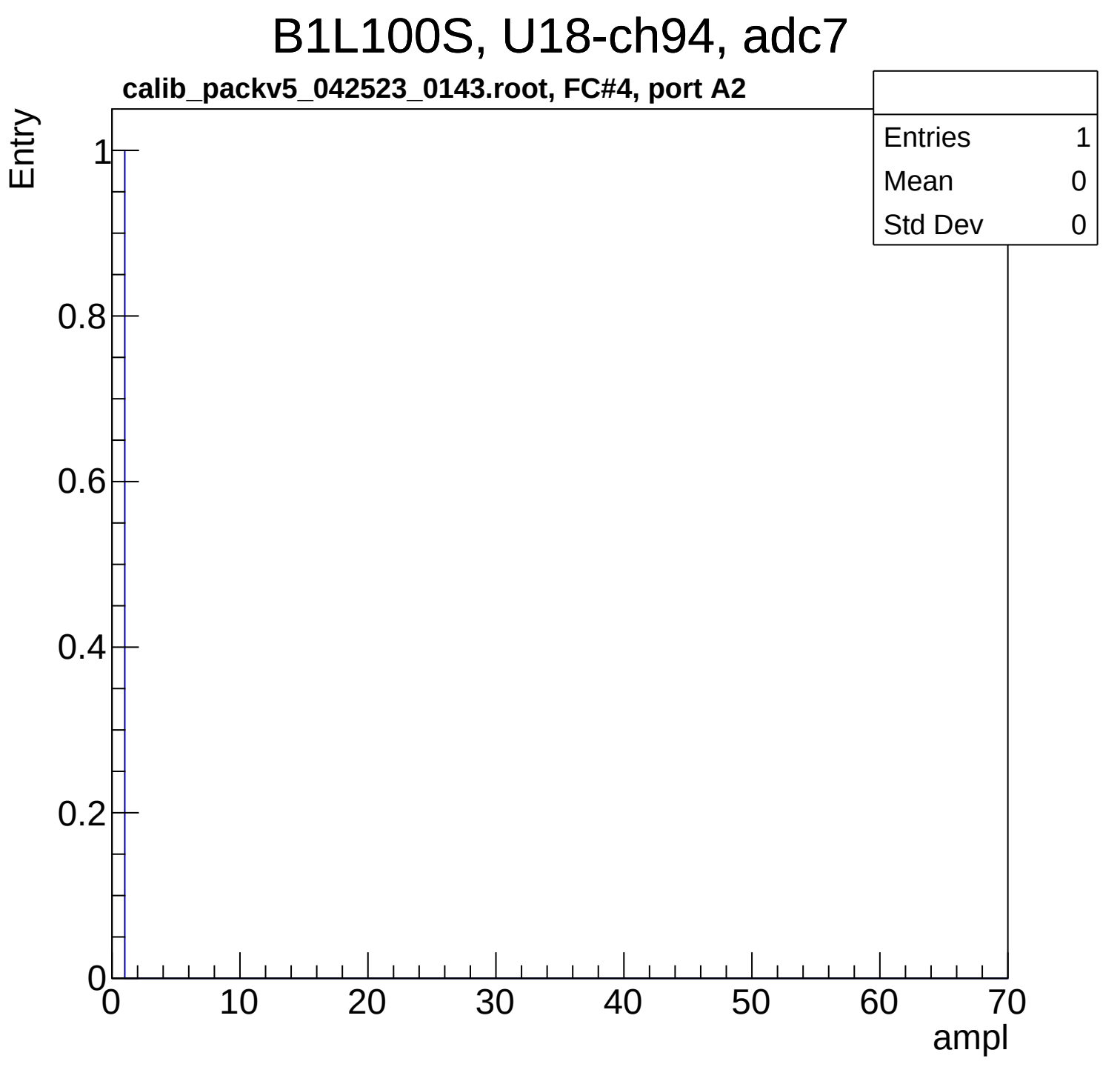

B1L100S, U18-ch94, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 41.41
Std Dev 3.018
Gaus mean : 41.5597
Gaus Width: 3.0184
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

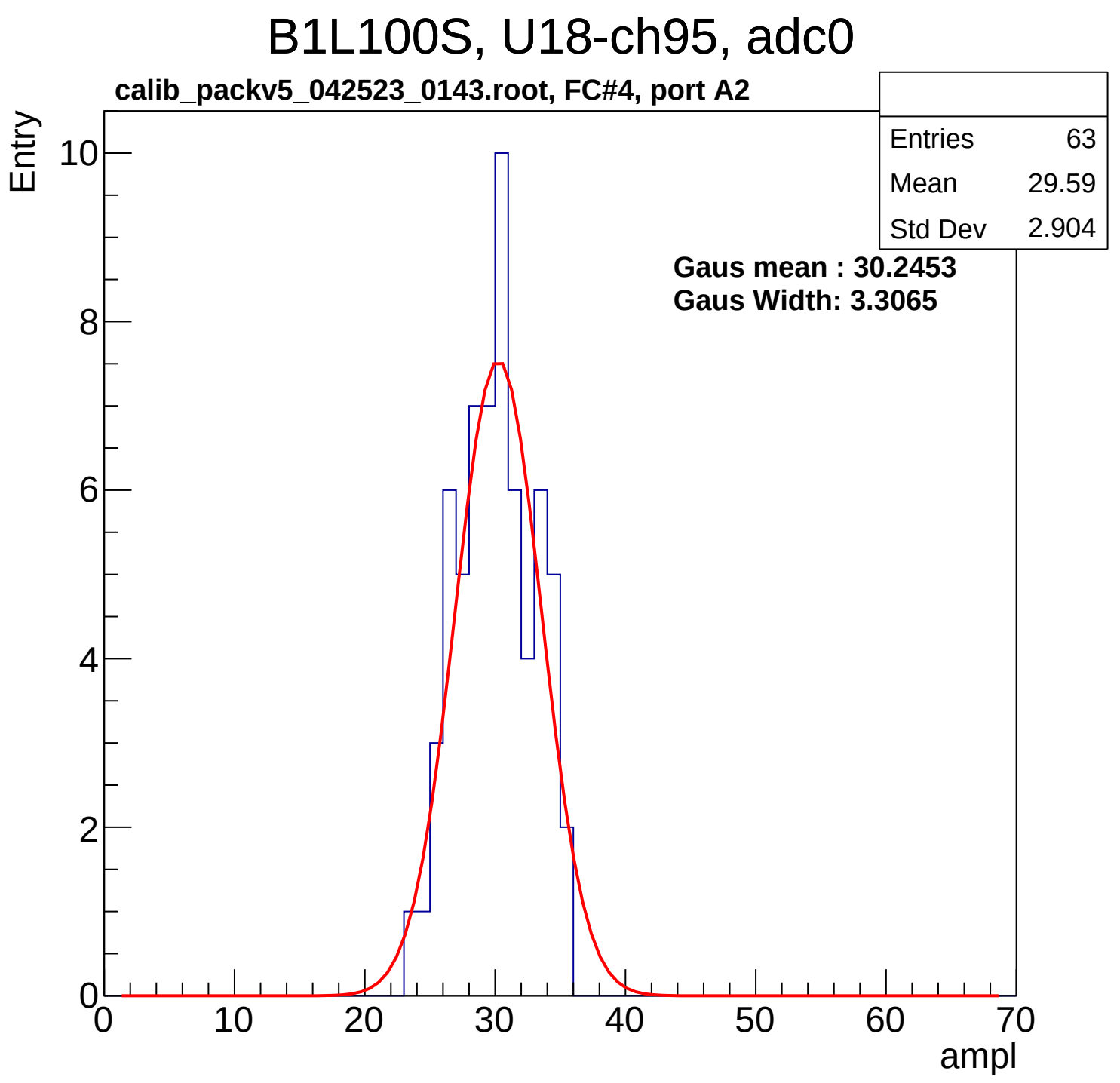

B1L100S, U18-ch94, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 48.7
Std Dev 3.948
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

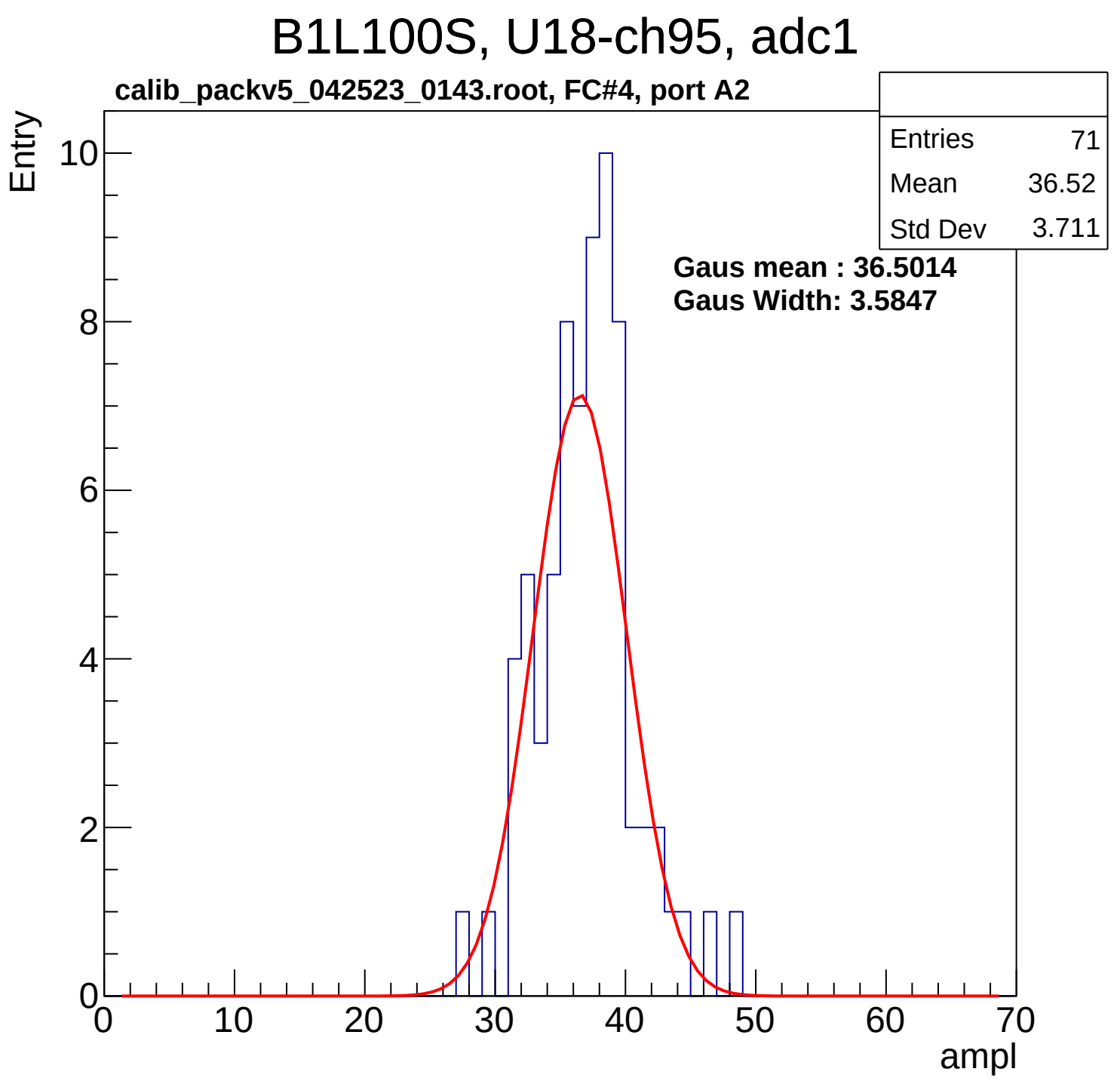

B1L100S, U18-ch94, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 55.25
Std Dev 2.974
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

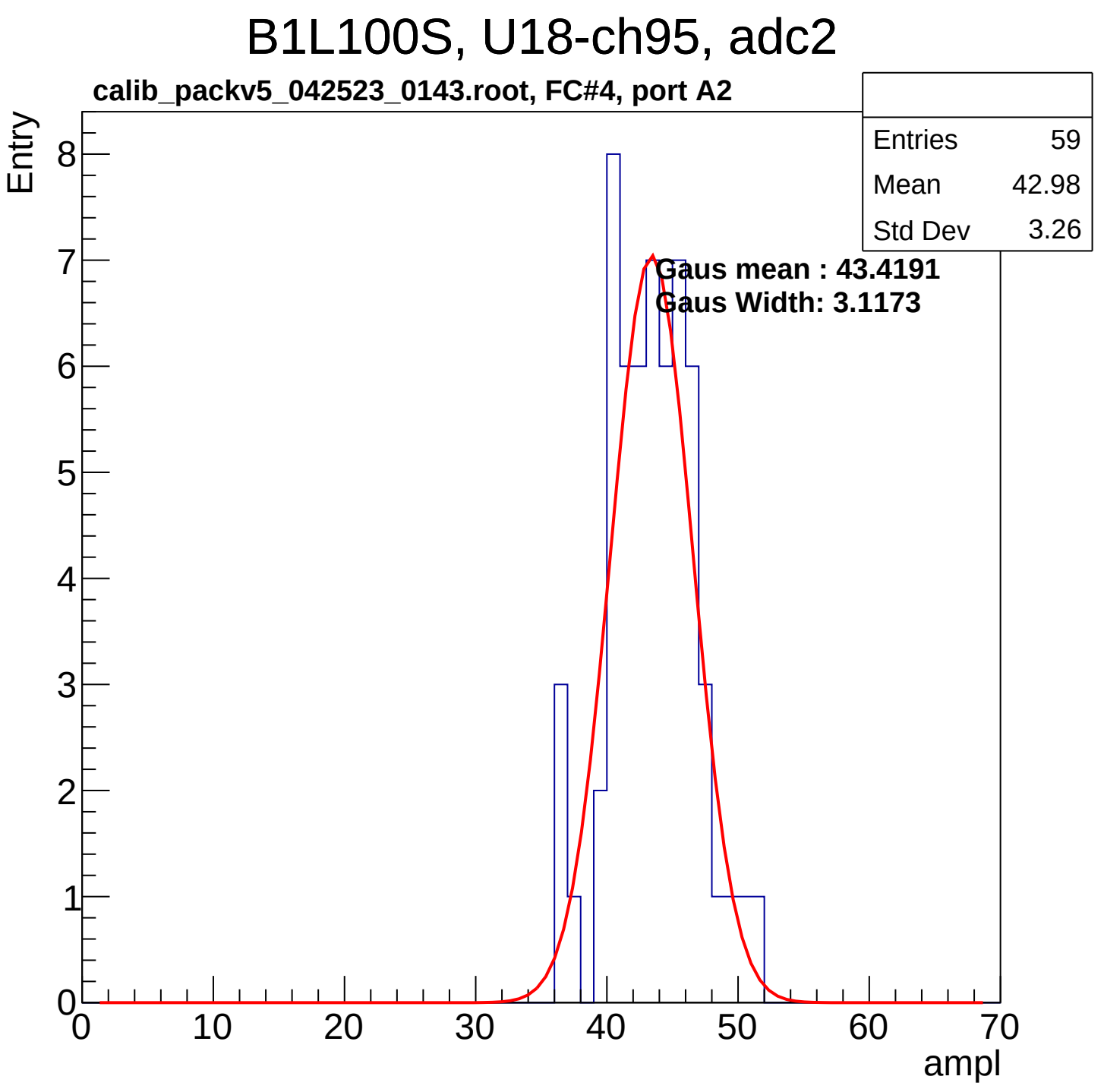

B1L100S, U18-ch94, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 45
Mean 59.64
Std Dev 2.709
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

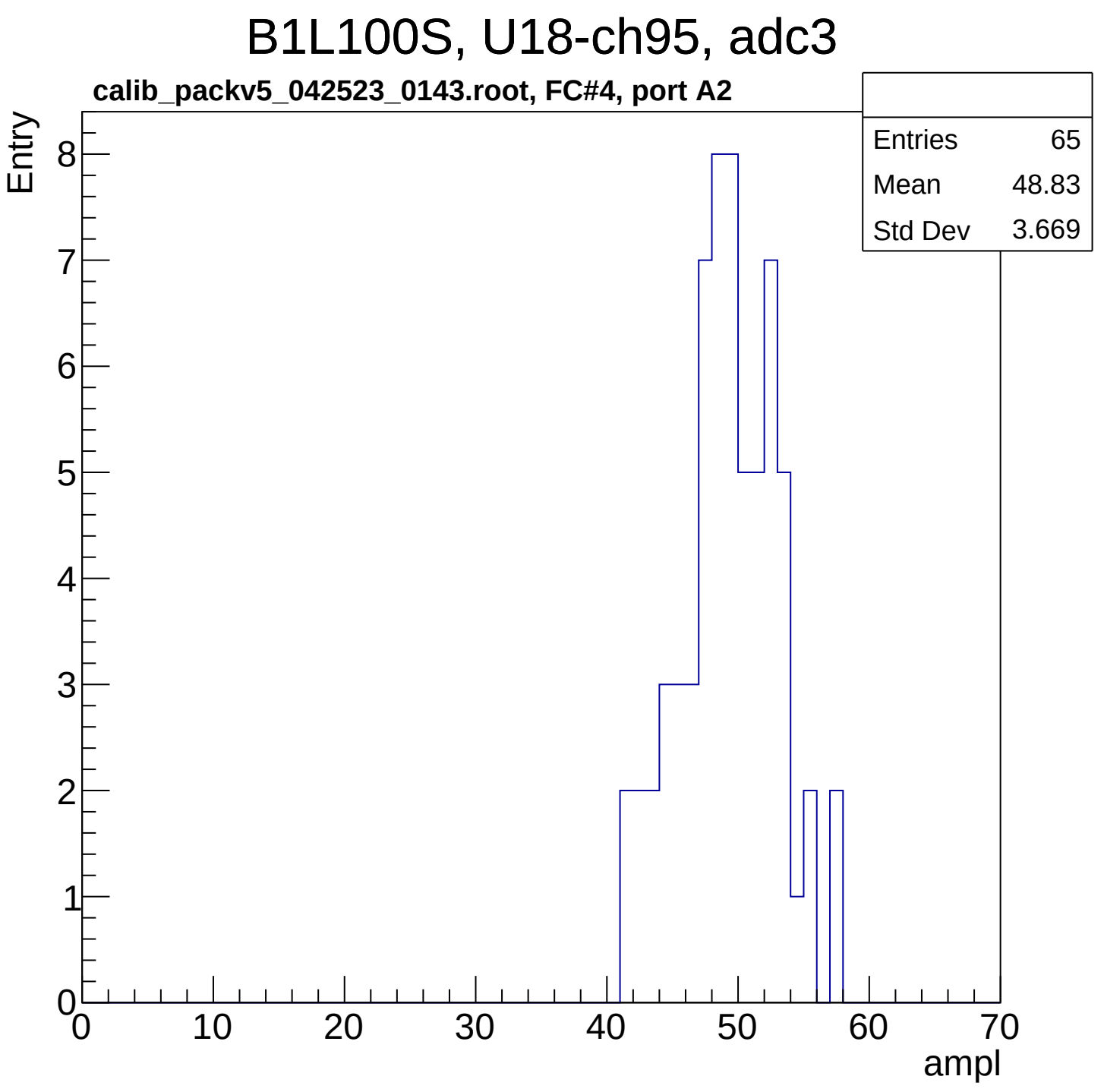

B1L100S, U18-ch94, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 55.7
Std Dev 18.6
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

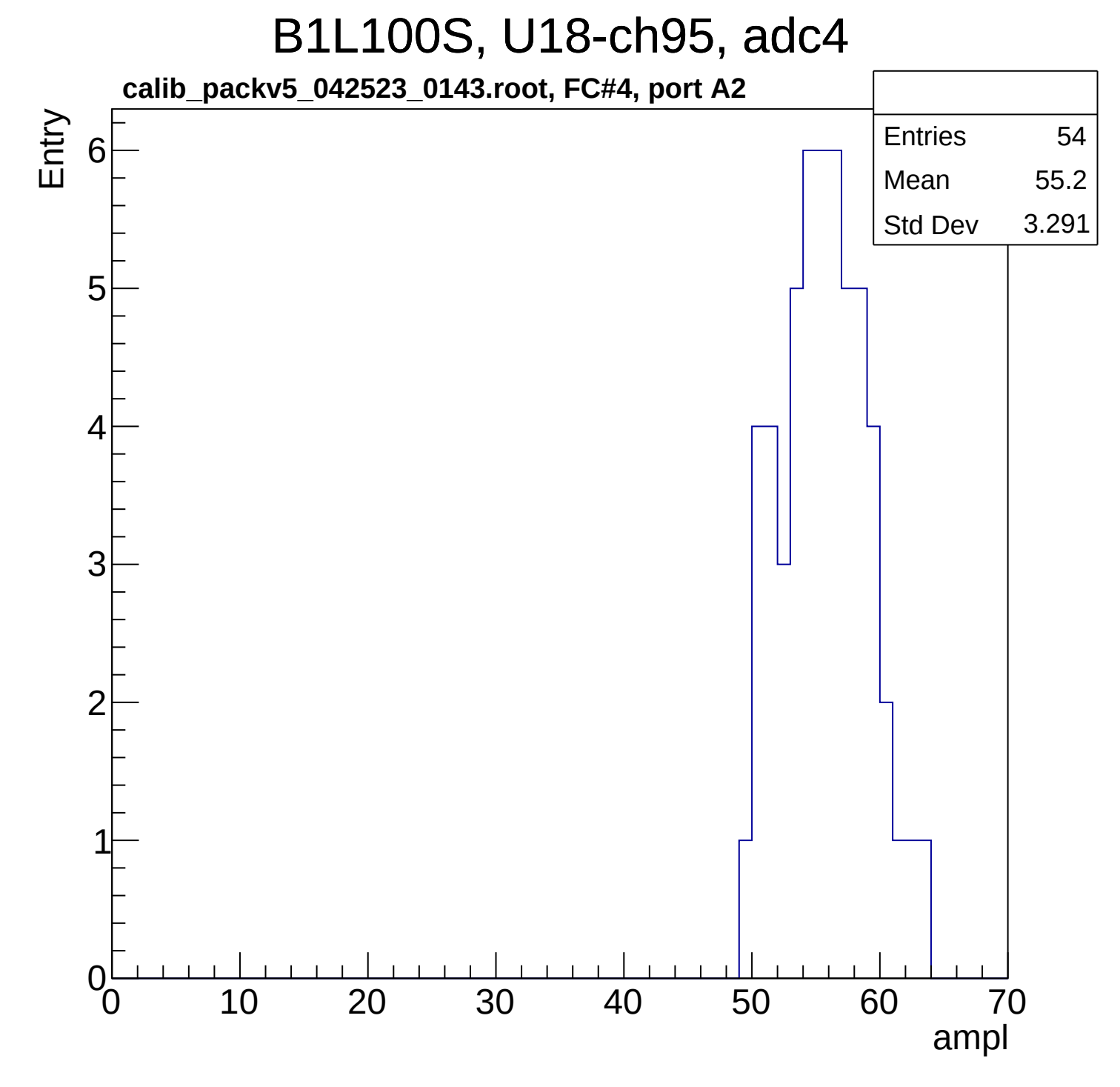

B1L100S, U18-ch94, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

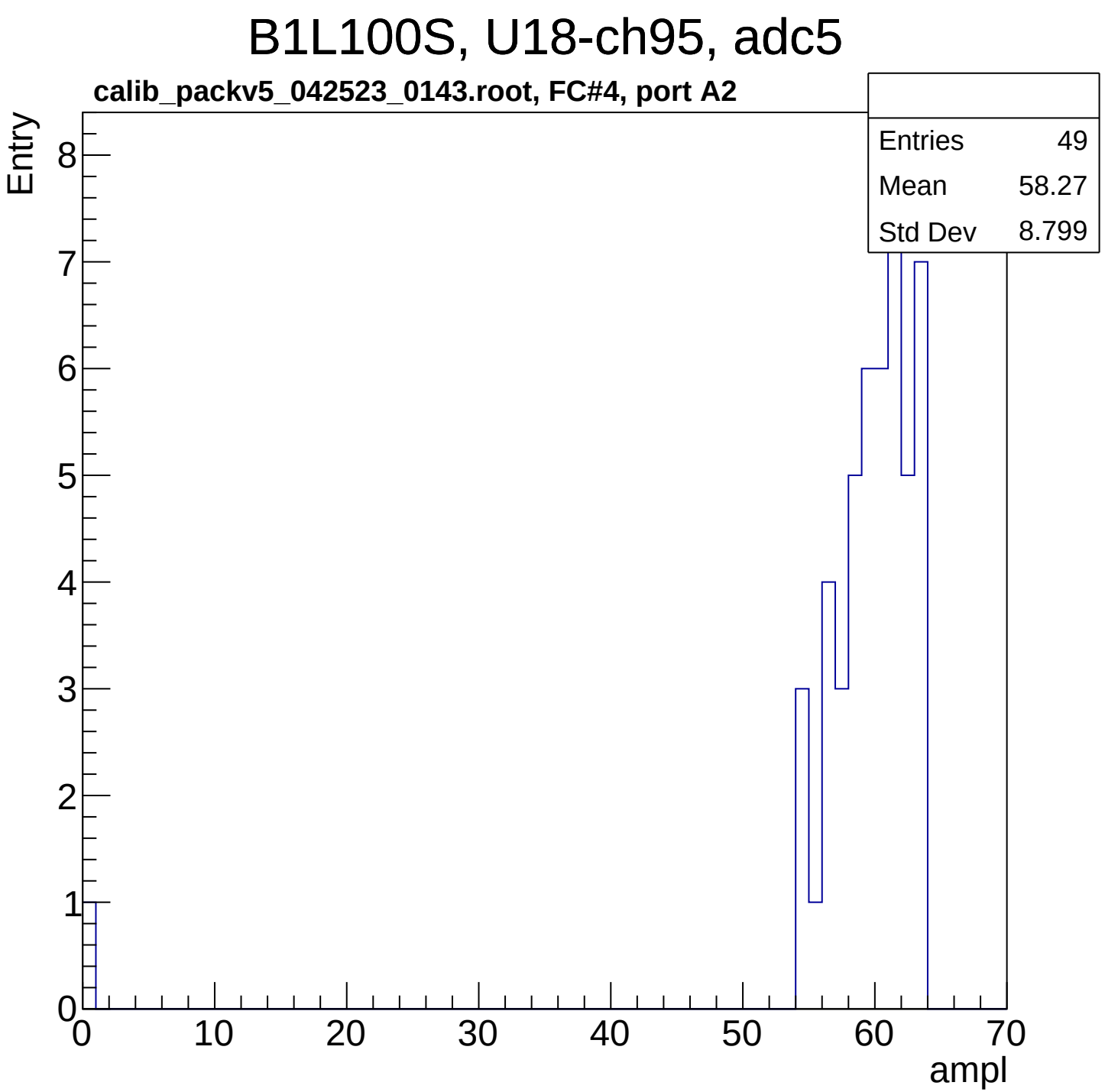

B1L100S, U18-ch95, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 29.59
Std Dev 2.904
Gaus mean : 30.2453
Gaus Width: 3.3065
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

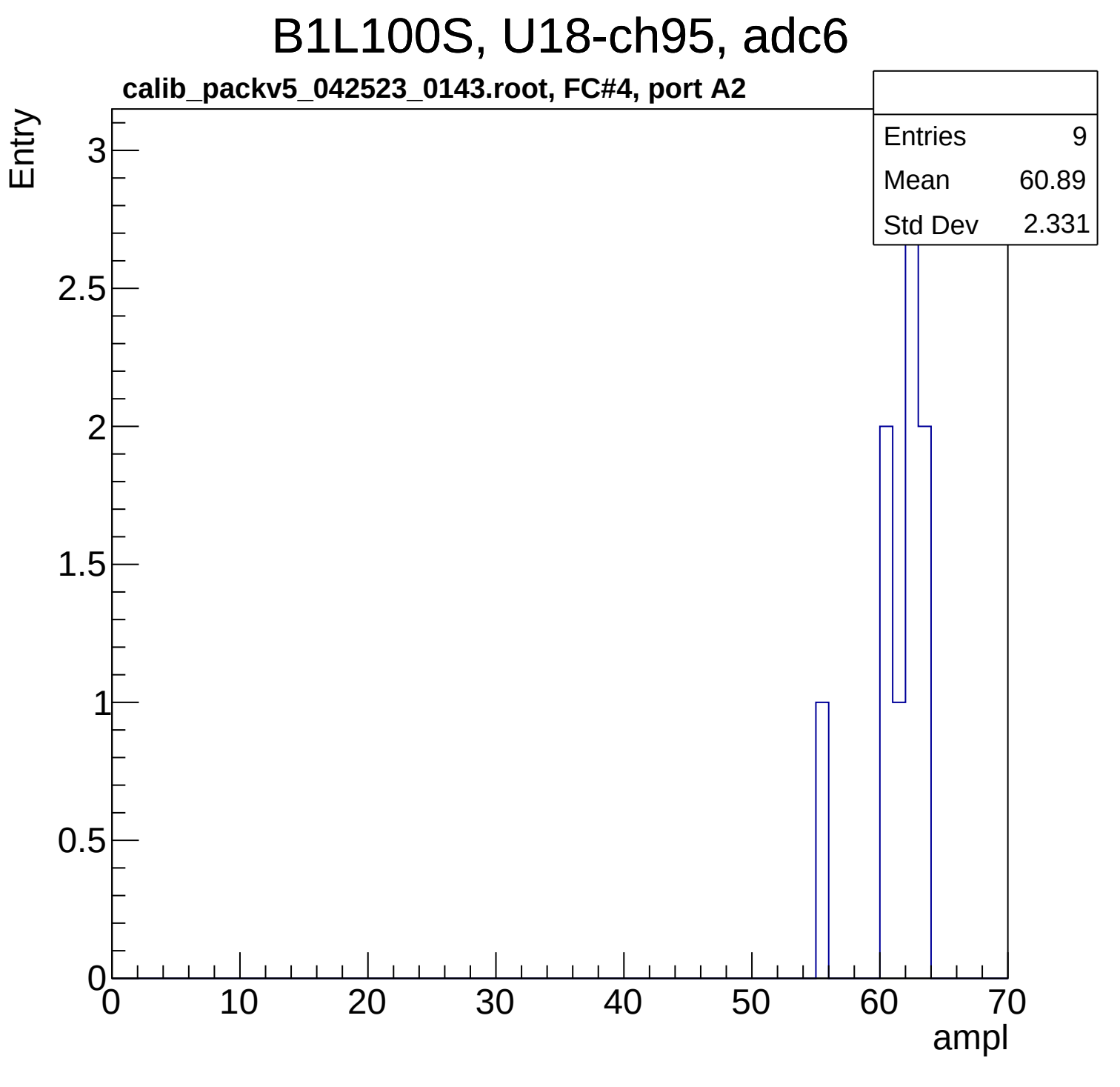

B1L100S, U18-ch95, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 36.52
Std Dev 3.711
Gaus mean : 36.5014
Gaus Width: 3.5847
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

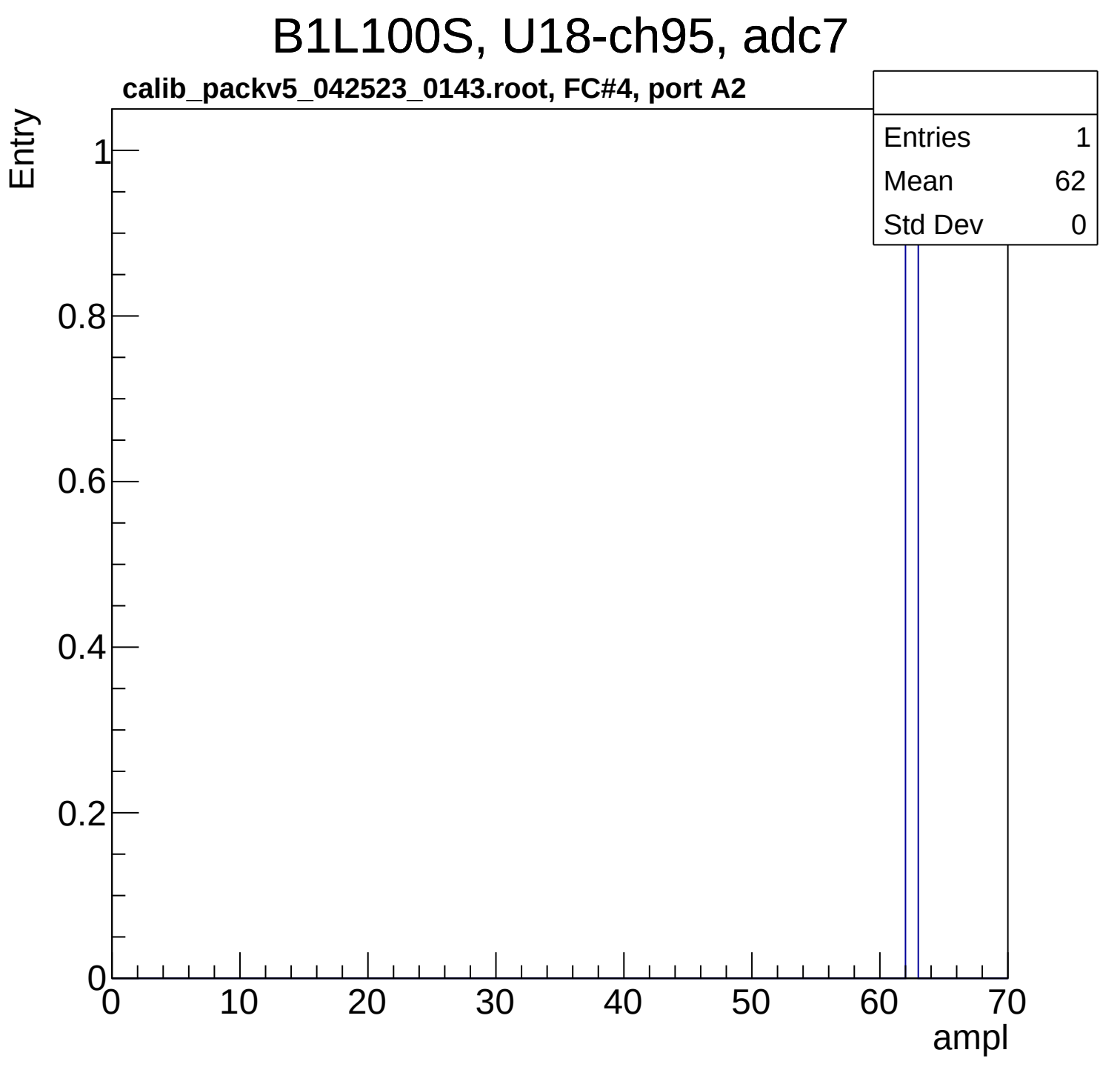

B1L100S, U18-ch95, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 42.98
Std Dev 3.26
Gaus mean : 43.4191
Gaus Width: 3.1173
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

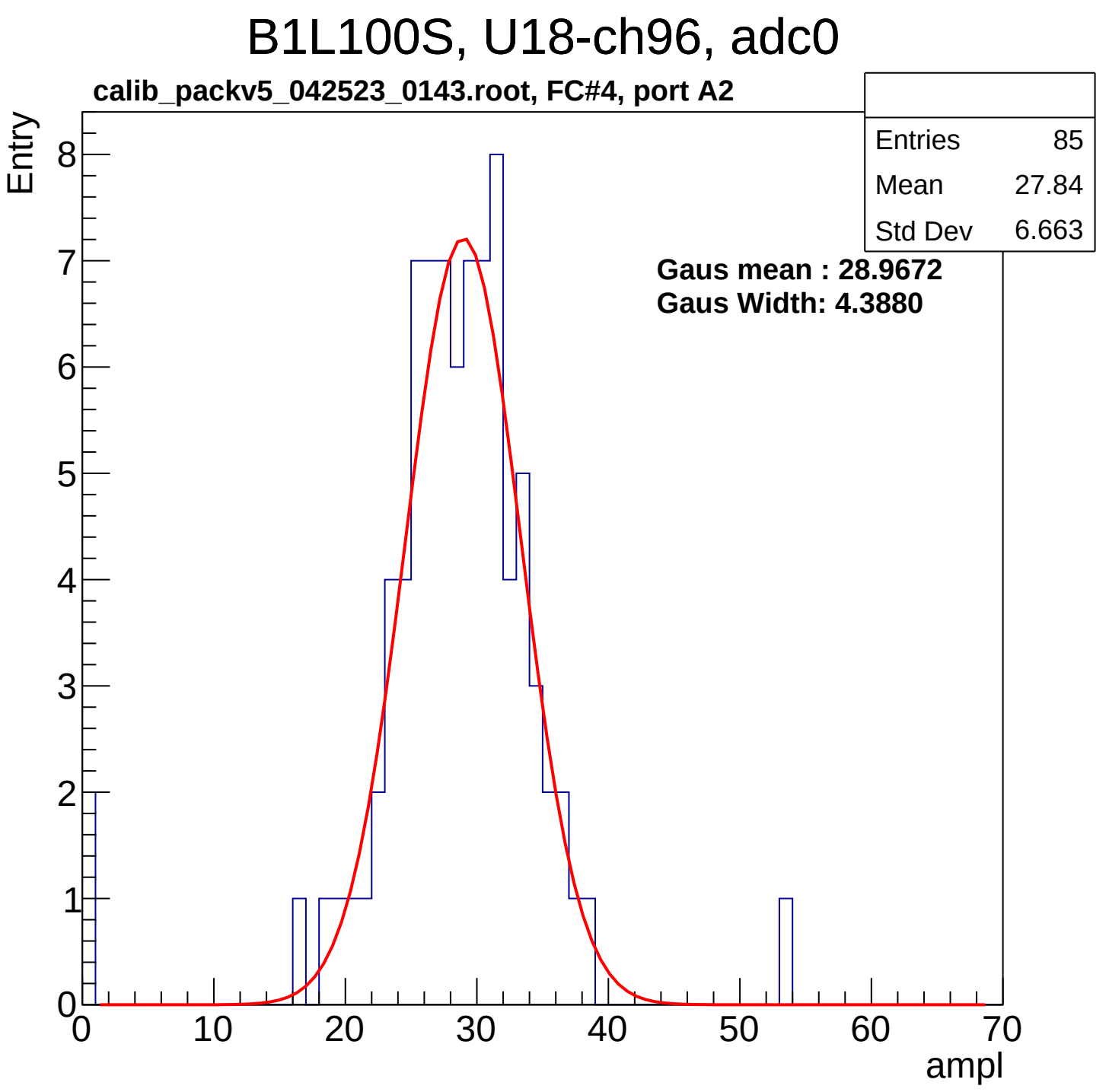

B1L100S, U18-ch95, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 48.83
Std Dev 3.669
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

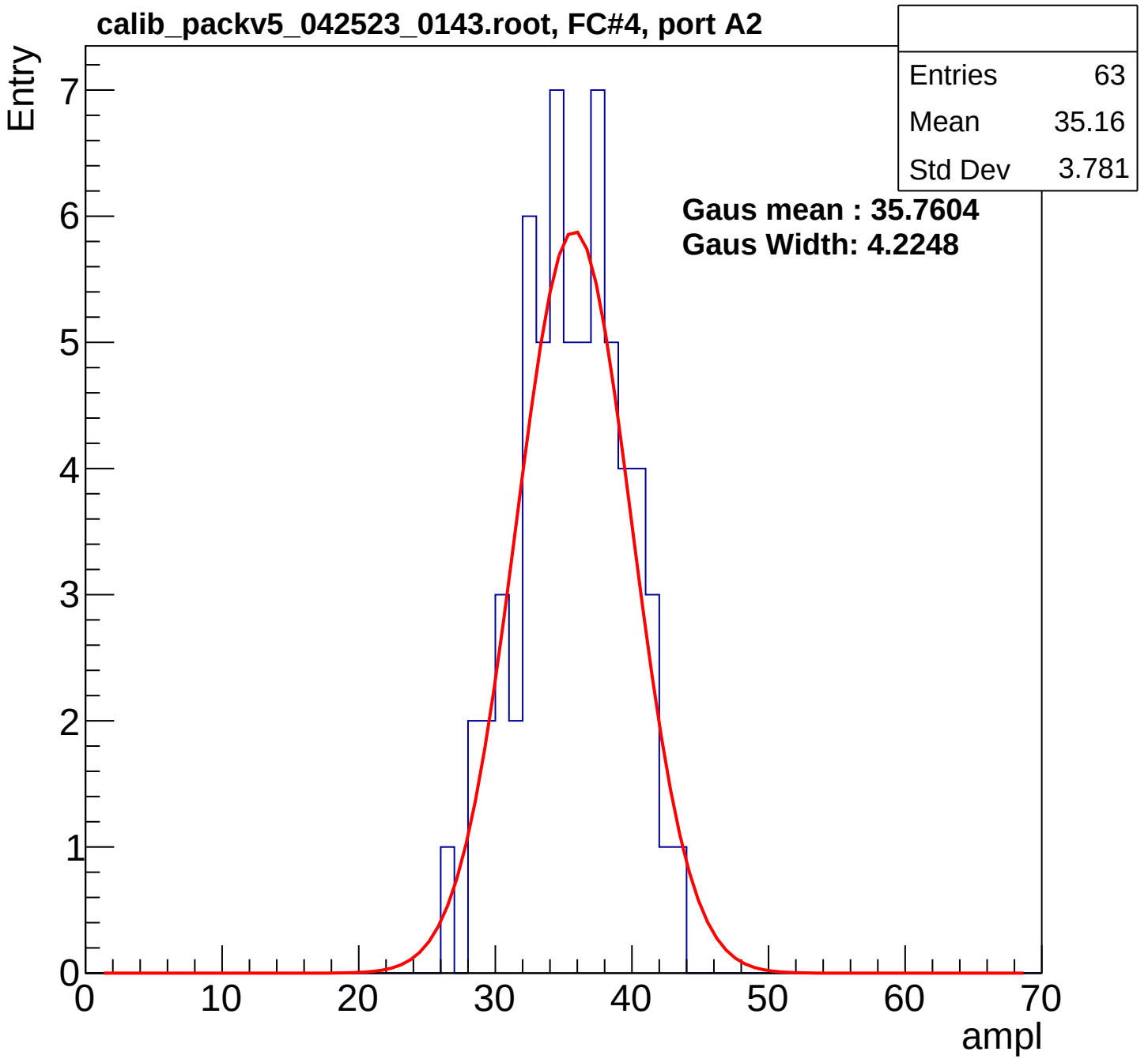

B1L100S, U18-ch95, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 55.2
Std Dev 3.291
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

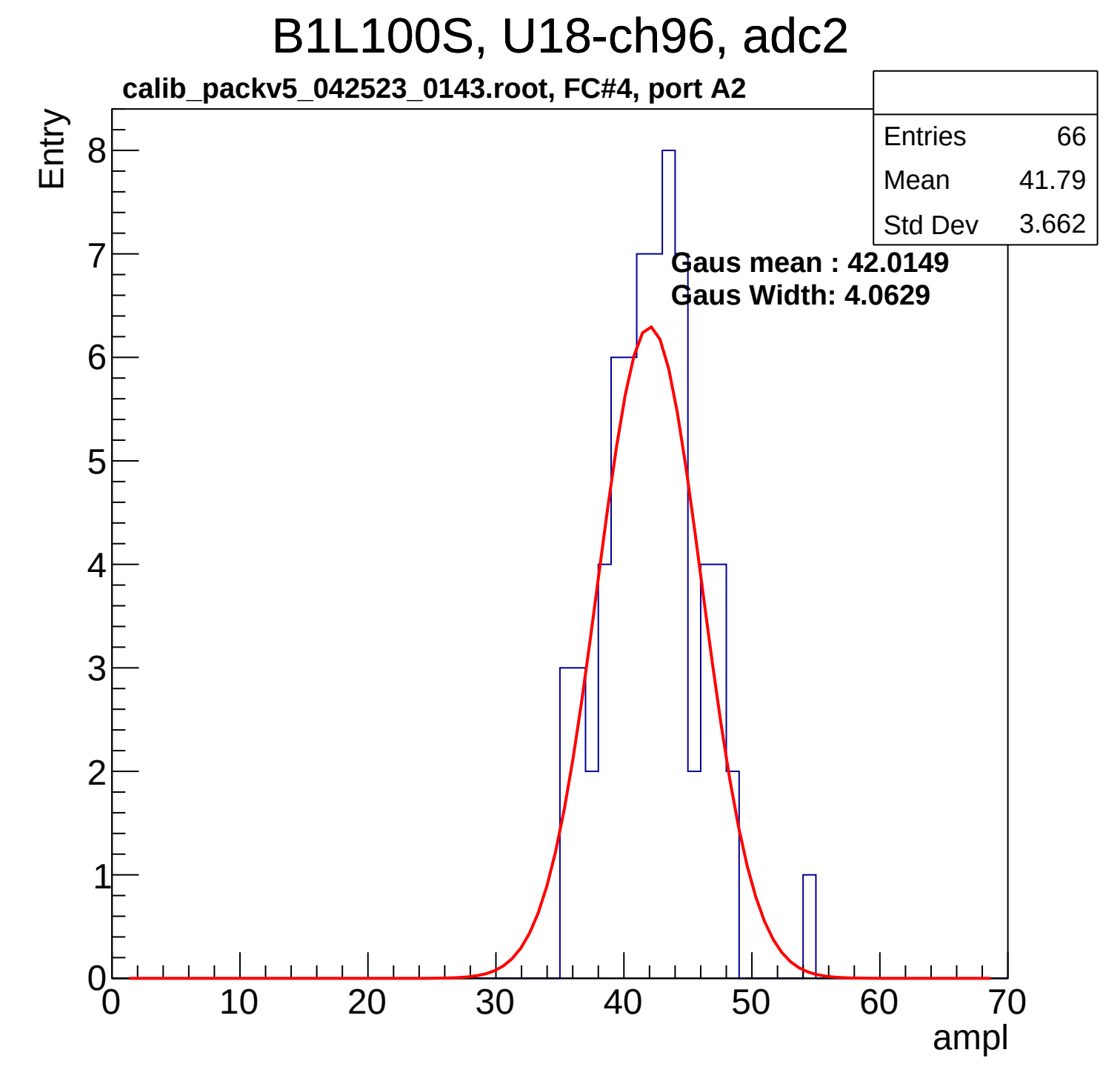

B1L100S, U18-ch95, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 58.27
Std Dev 8.799
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

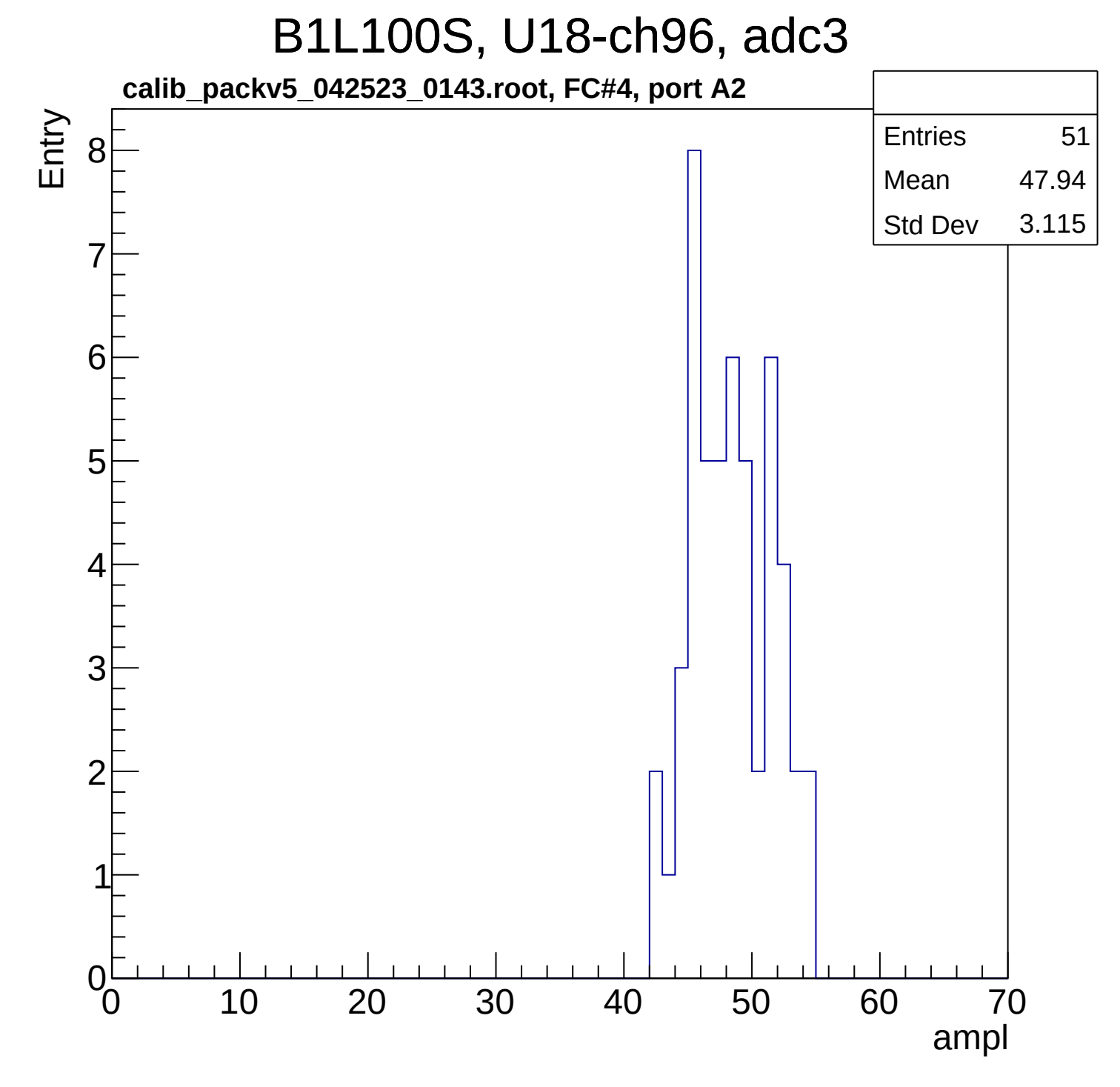

B1L100S, U18-ch95, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 60.89
Std Dev 2.331
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

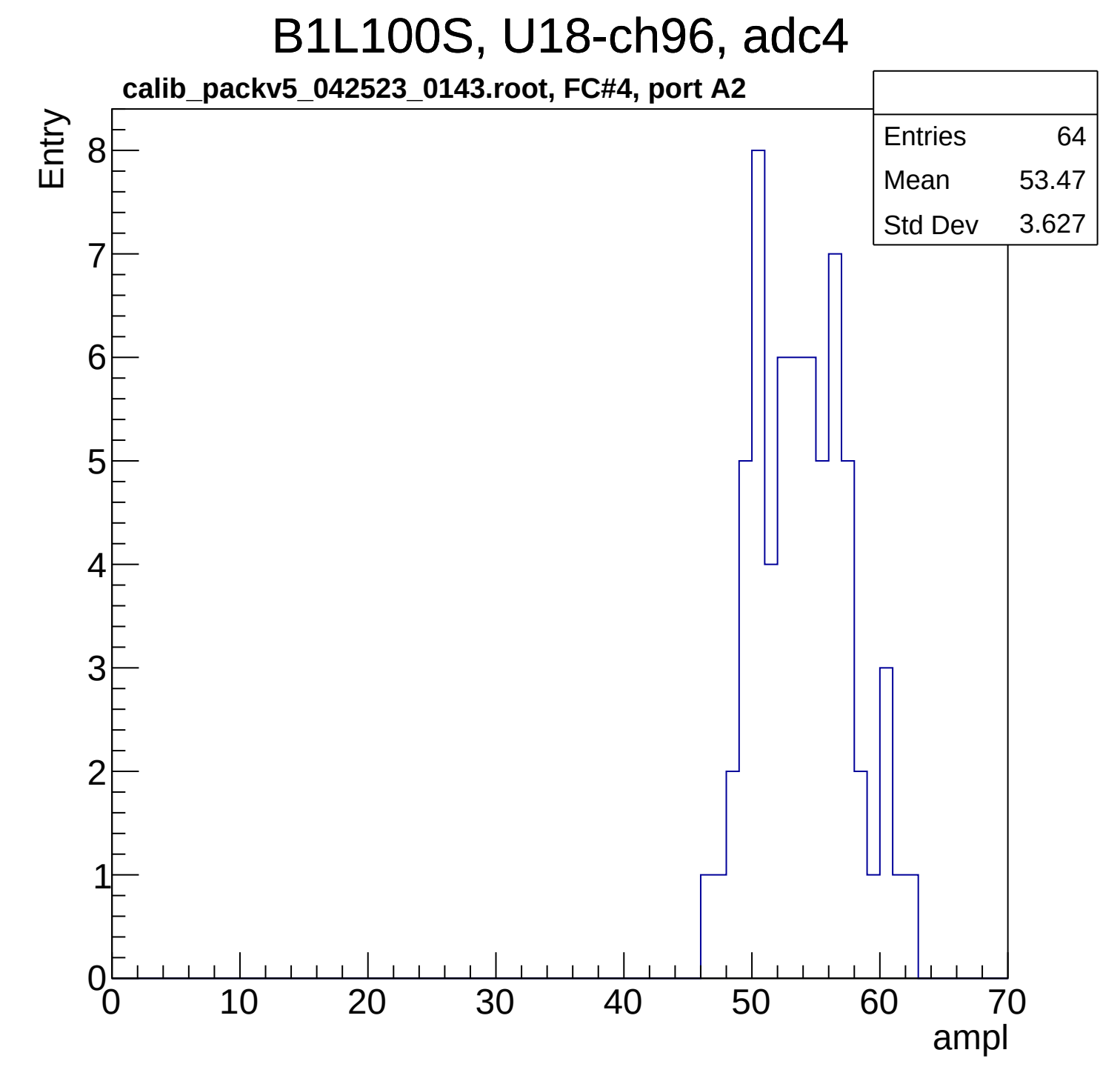

B1L100S, U18-ch95, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 62
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

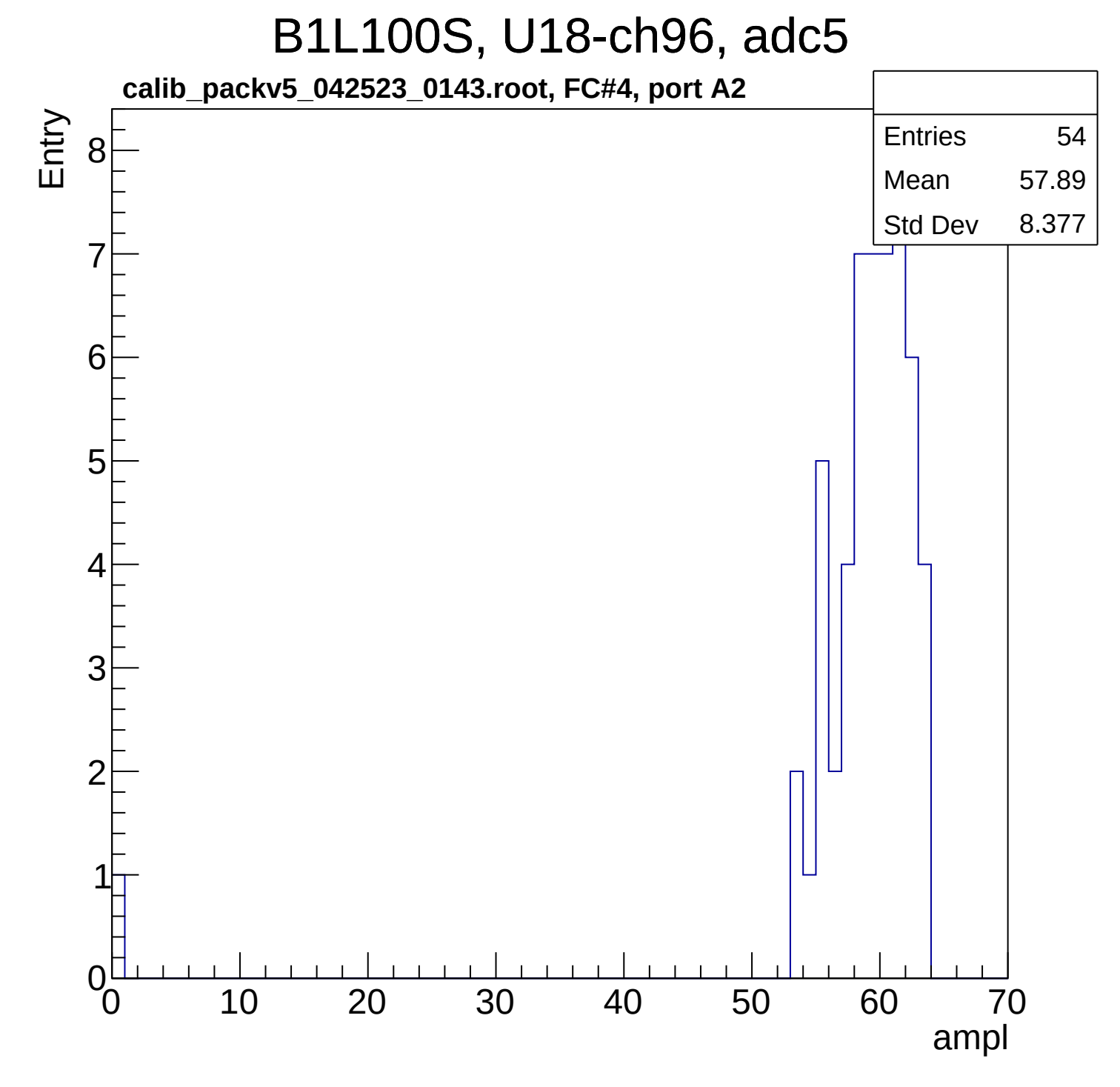

B1L100S, U18-ch96, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 85
Mean 27.84
Std Dev 6.663
Gaus mean : 28.9672
Gaus Width: 4.3880
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

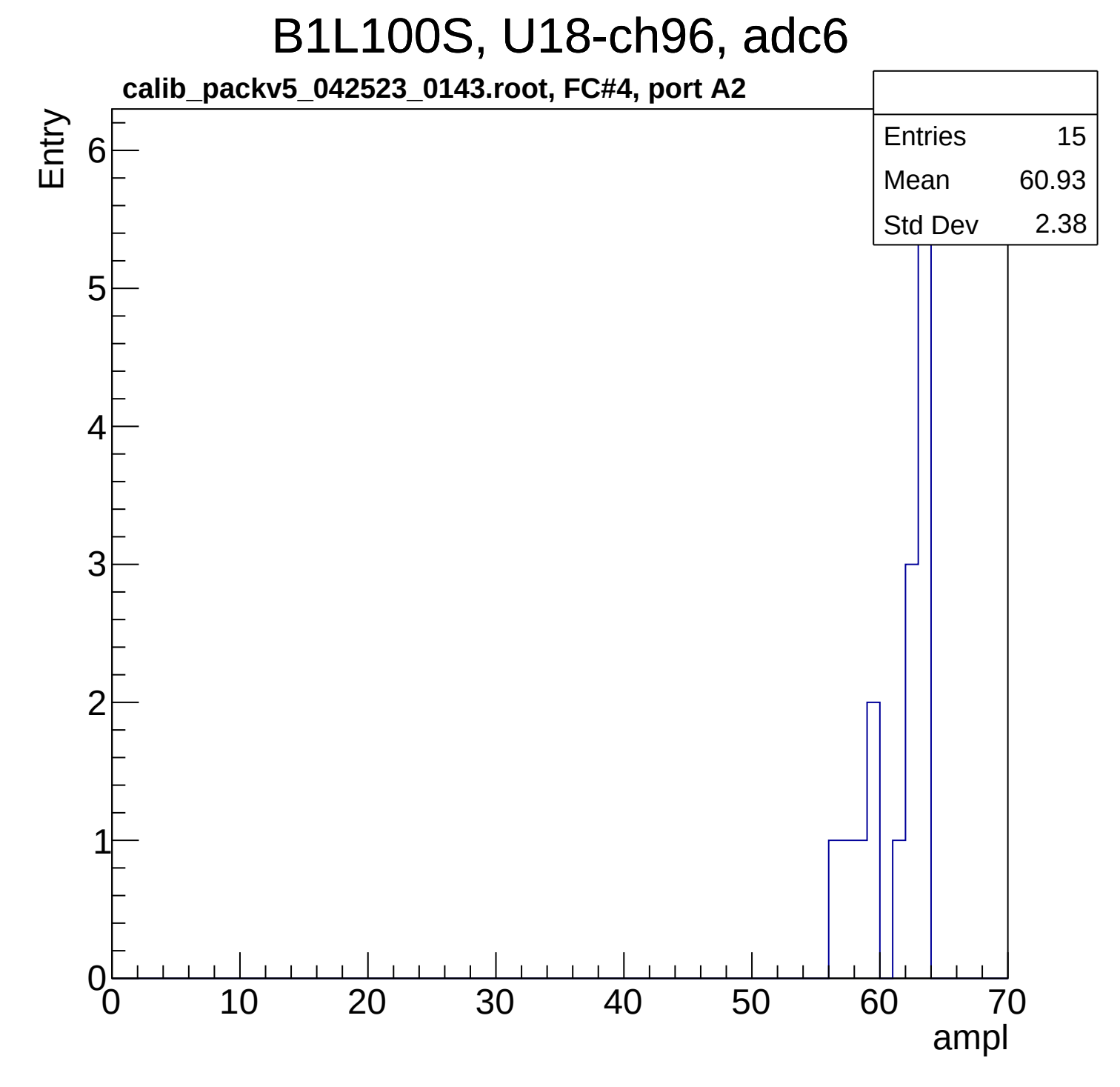

B1L100S, U18-ch96, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 35.16
Std Dev 3.781
Gaus mean : 35.7604
Gaus Width: 4.2248
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

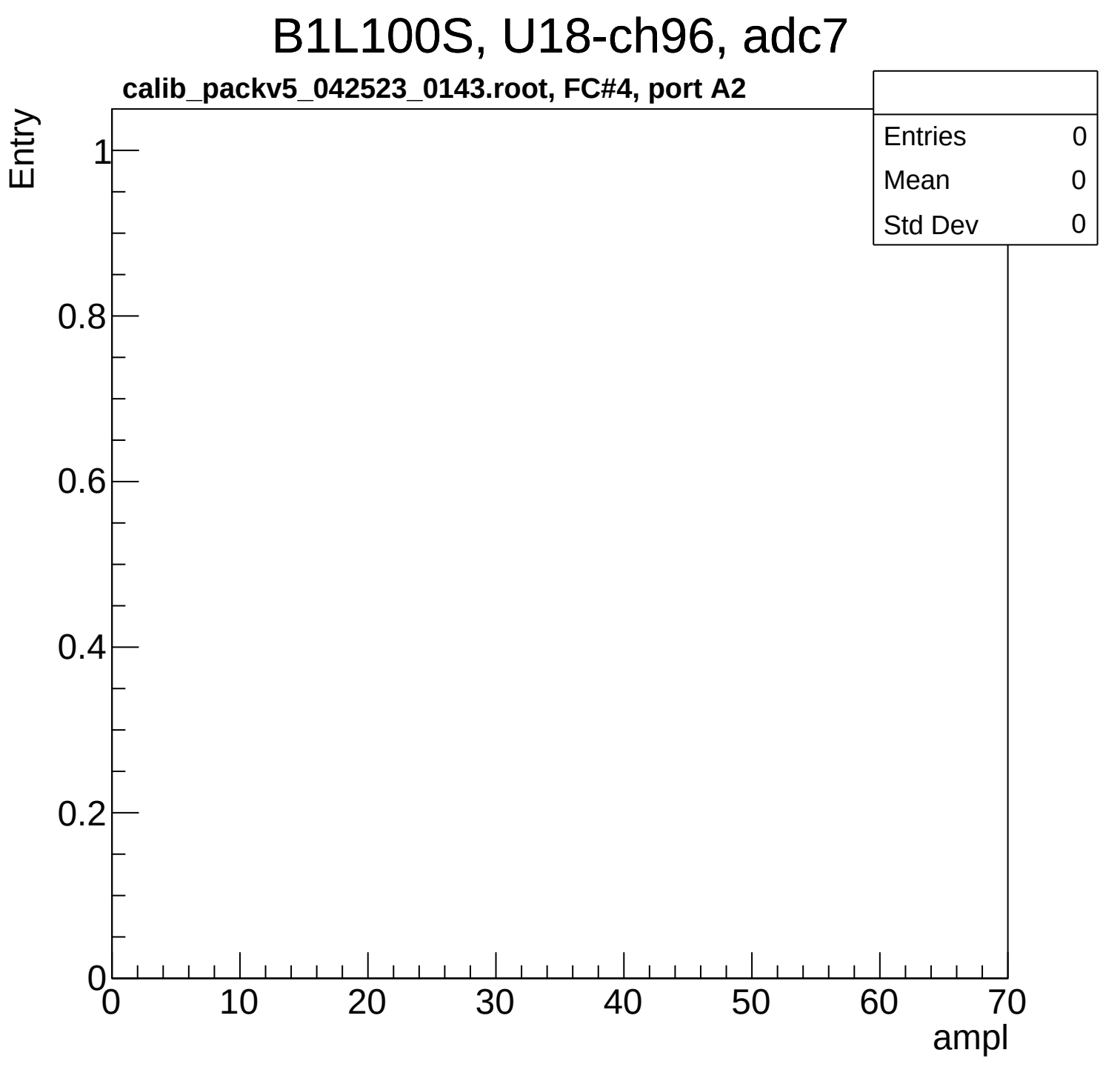

B1L100S, U18-ch96, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 41.79
Std Dev 3.662
Gaus mean : 42.0149
Gaus Width: 4.0629
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

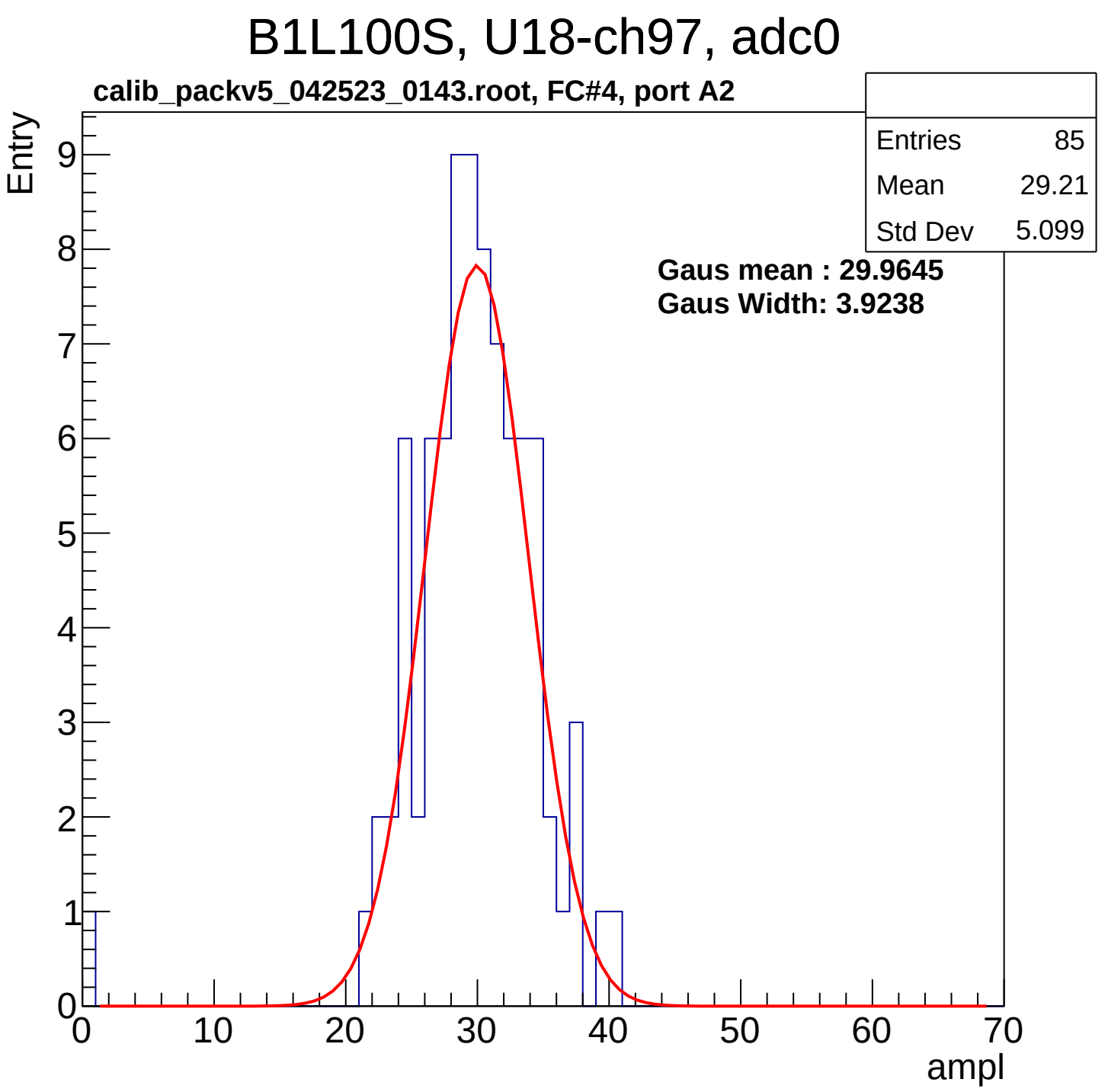

B1L100S, U18-ch96, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 47.94
Std Dev 3.115
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

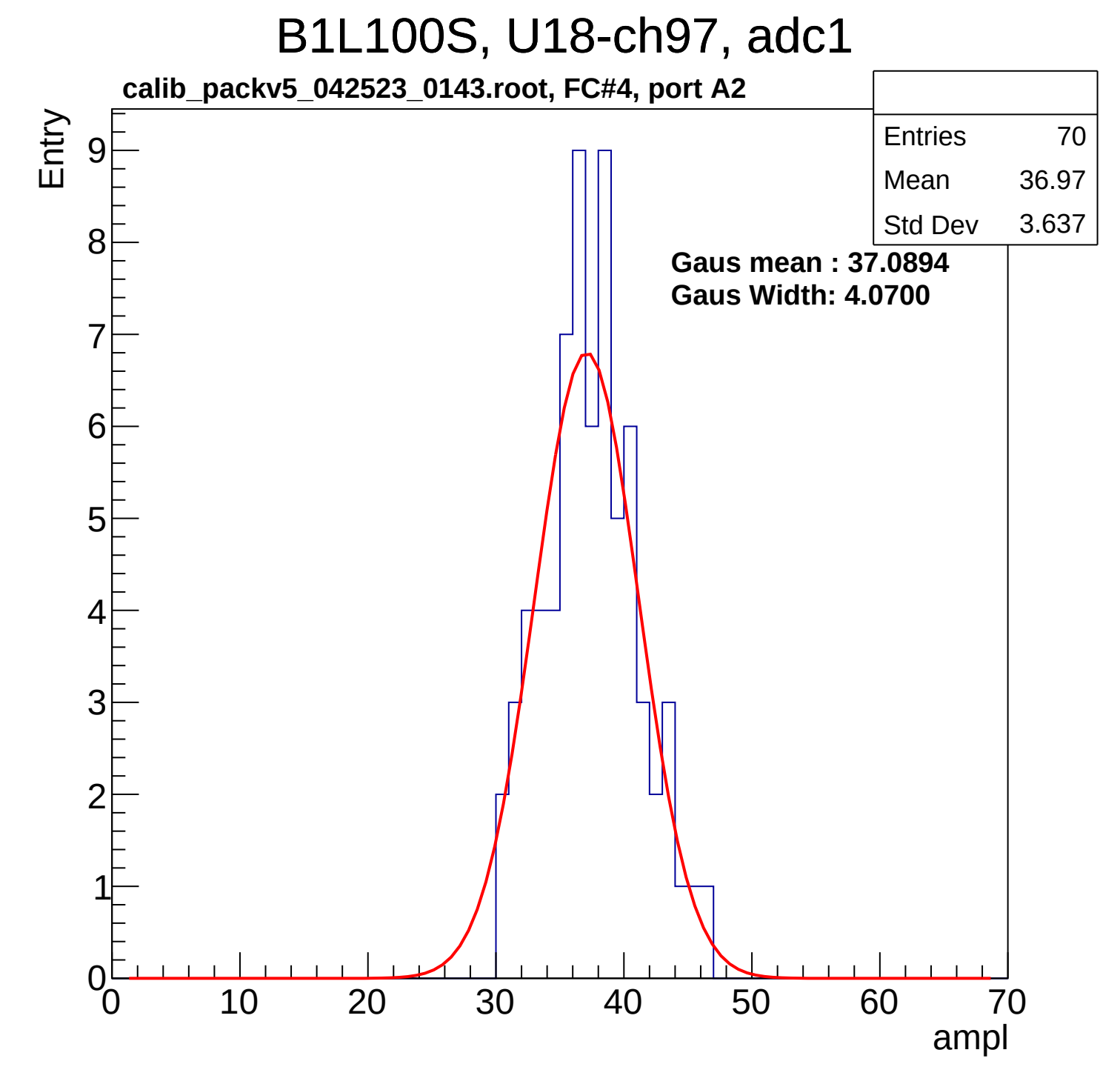

B1L100S, U18-ch96, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 53.47
Std Dev 3.627
Entry
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70
ampl

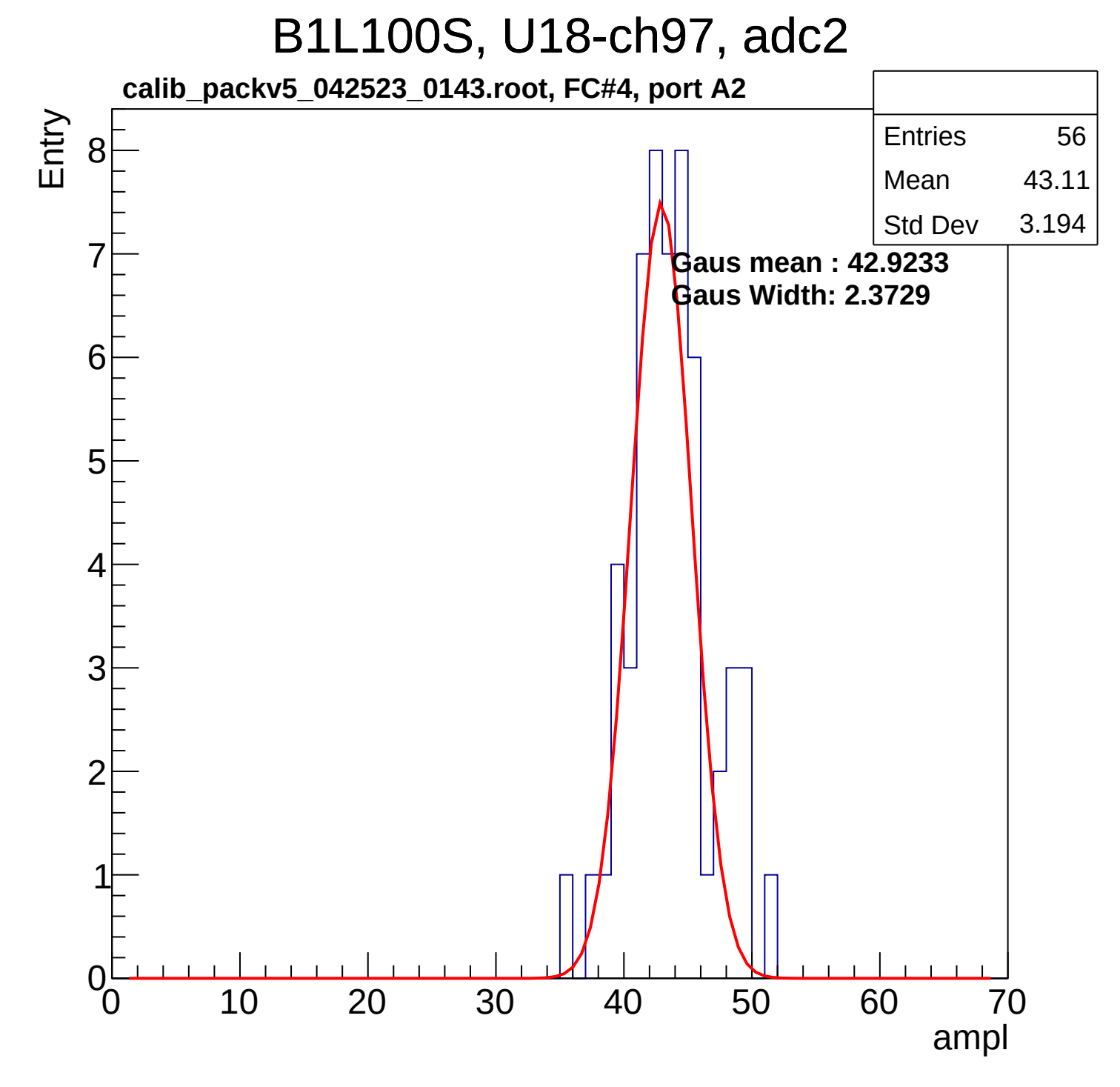

B1L100S, U18-ch96, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 57.89
Std Dev 8.377
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

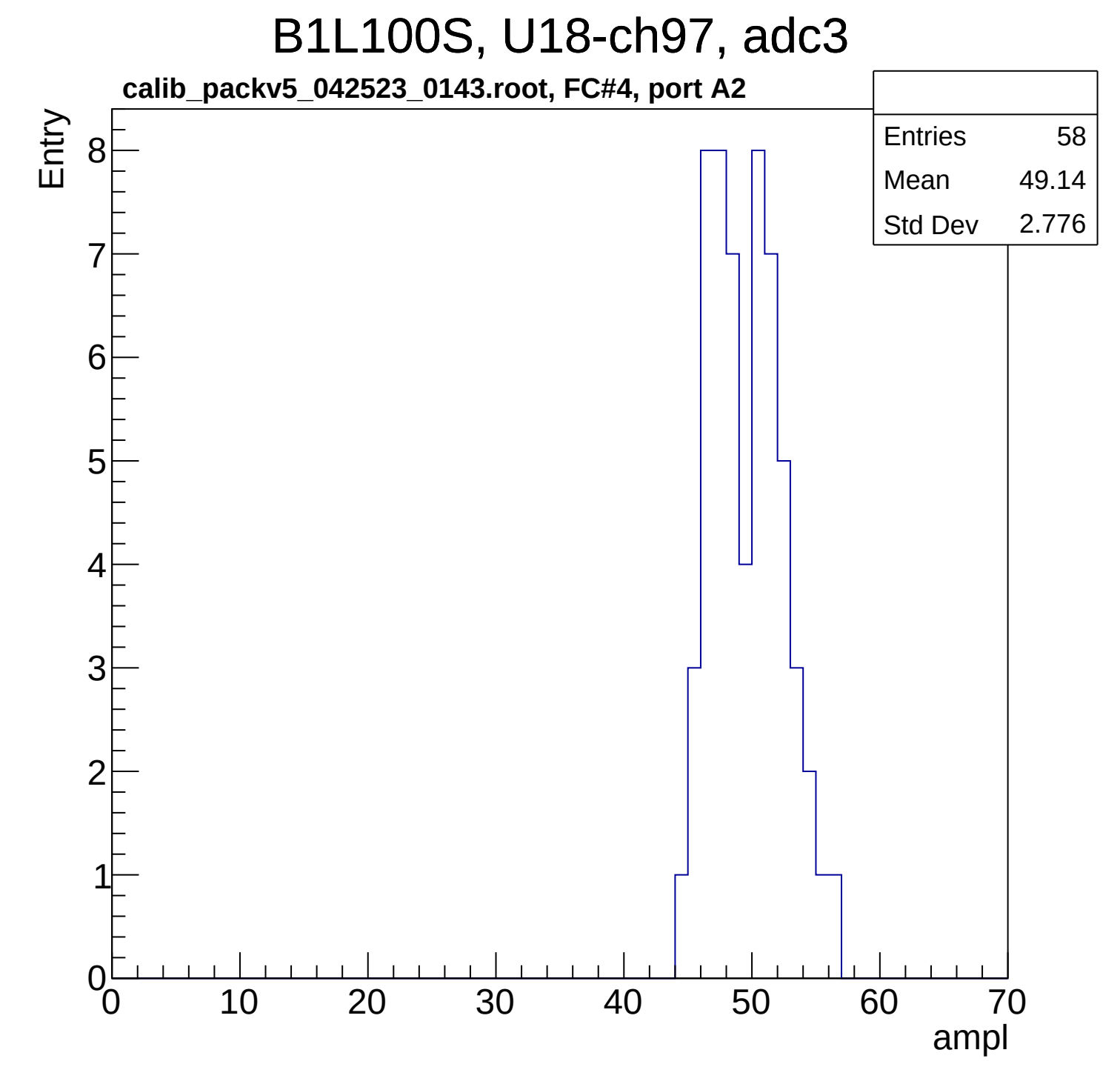

B1L100S, U18-ch96, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 15
Mean 60.93
Std Dev 2.38
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

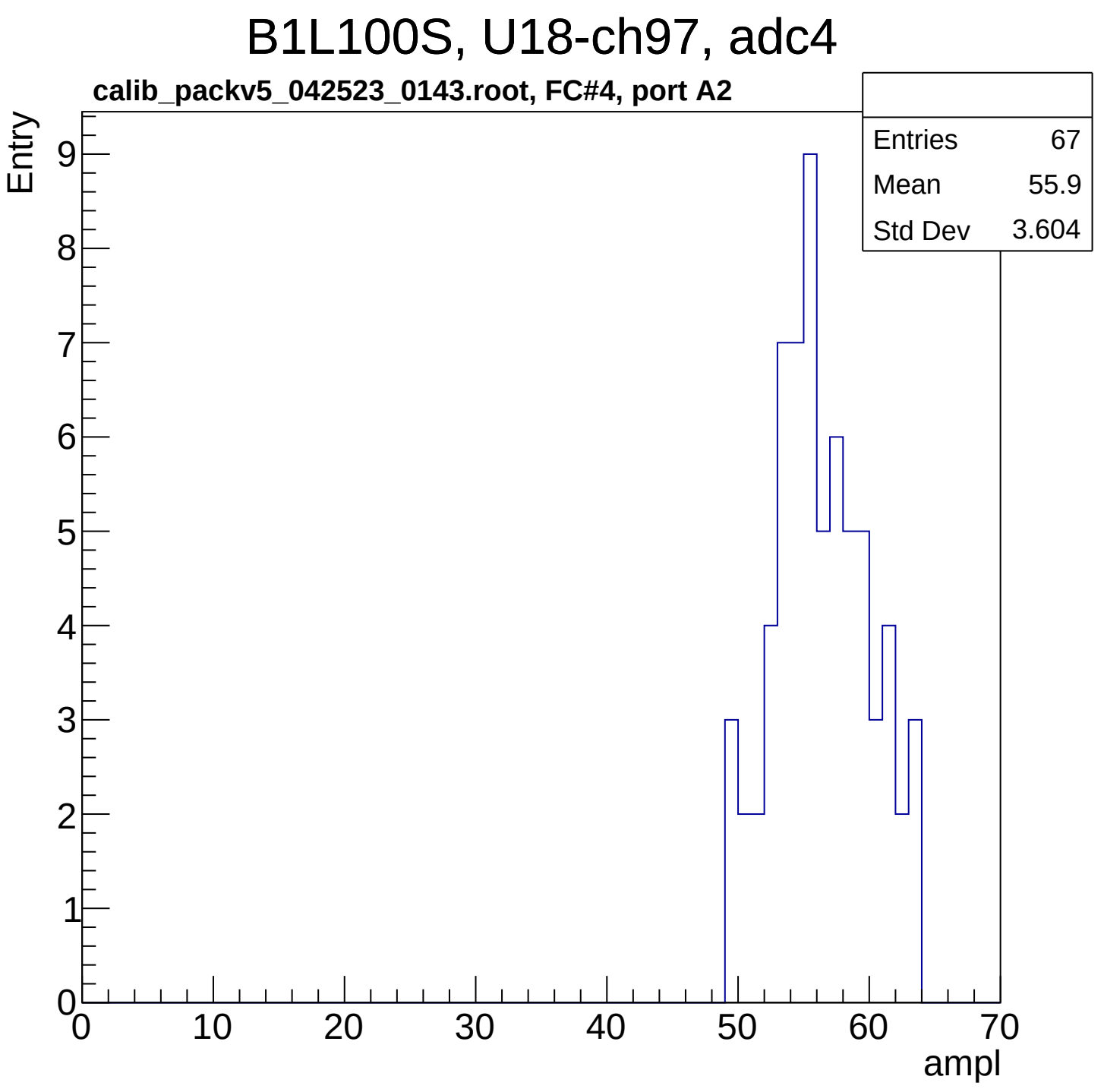

B1L100S, U18-ch96, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

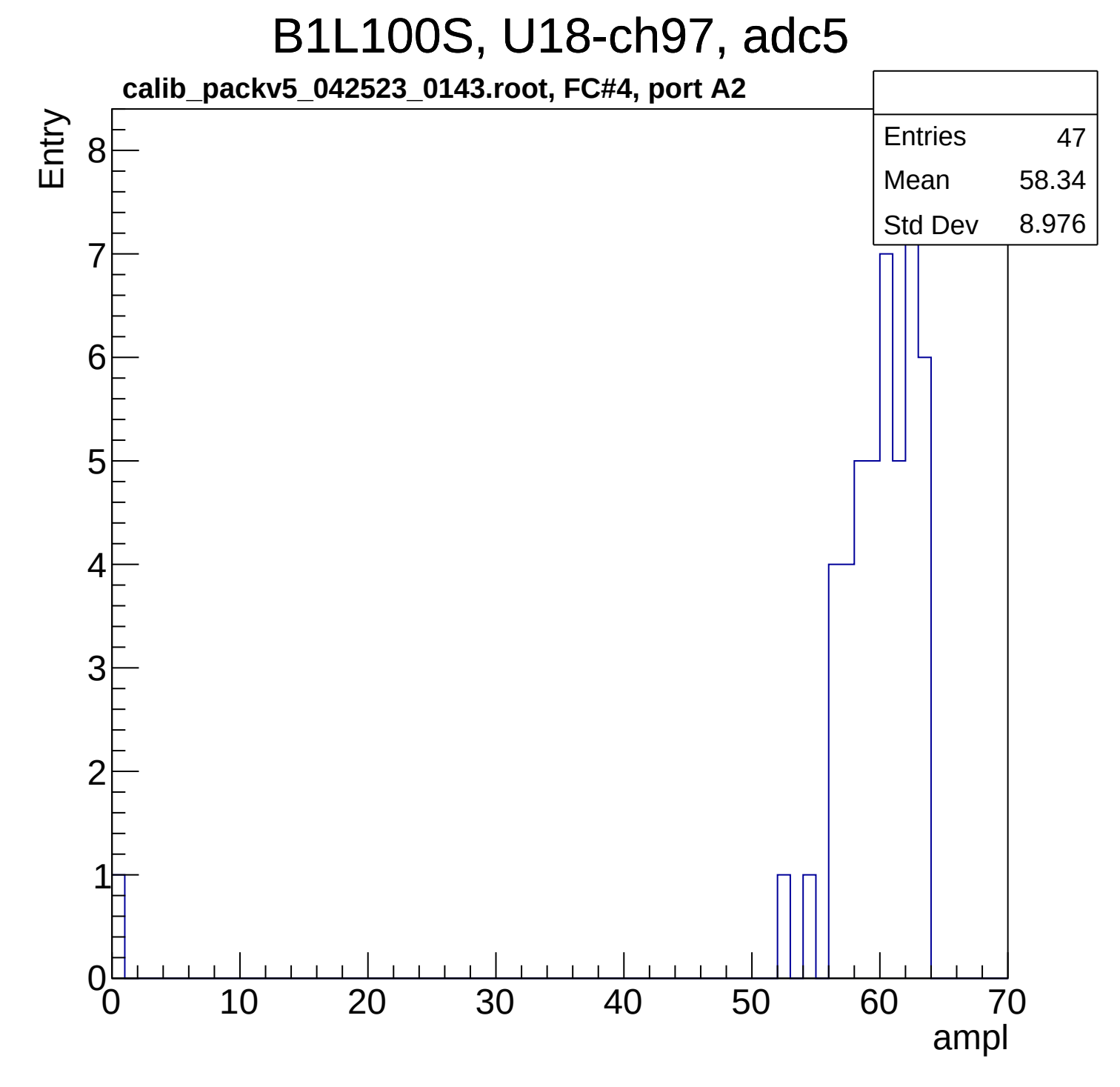

B1L100S, U18-ch97, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 85
Mean 29.21
Std Dev 5.099
Gaus mean : 29.9645
Gaus Width: 3.9238
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

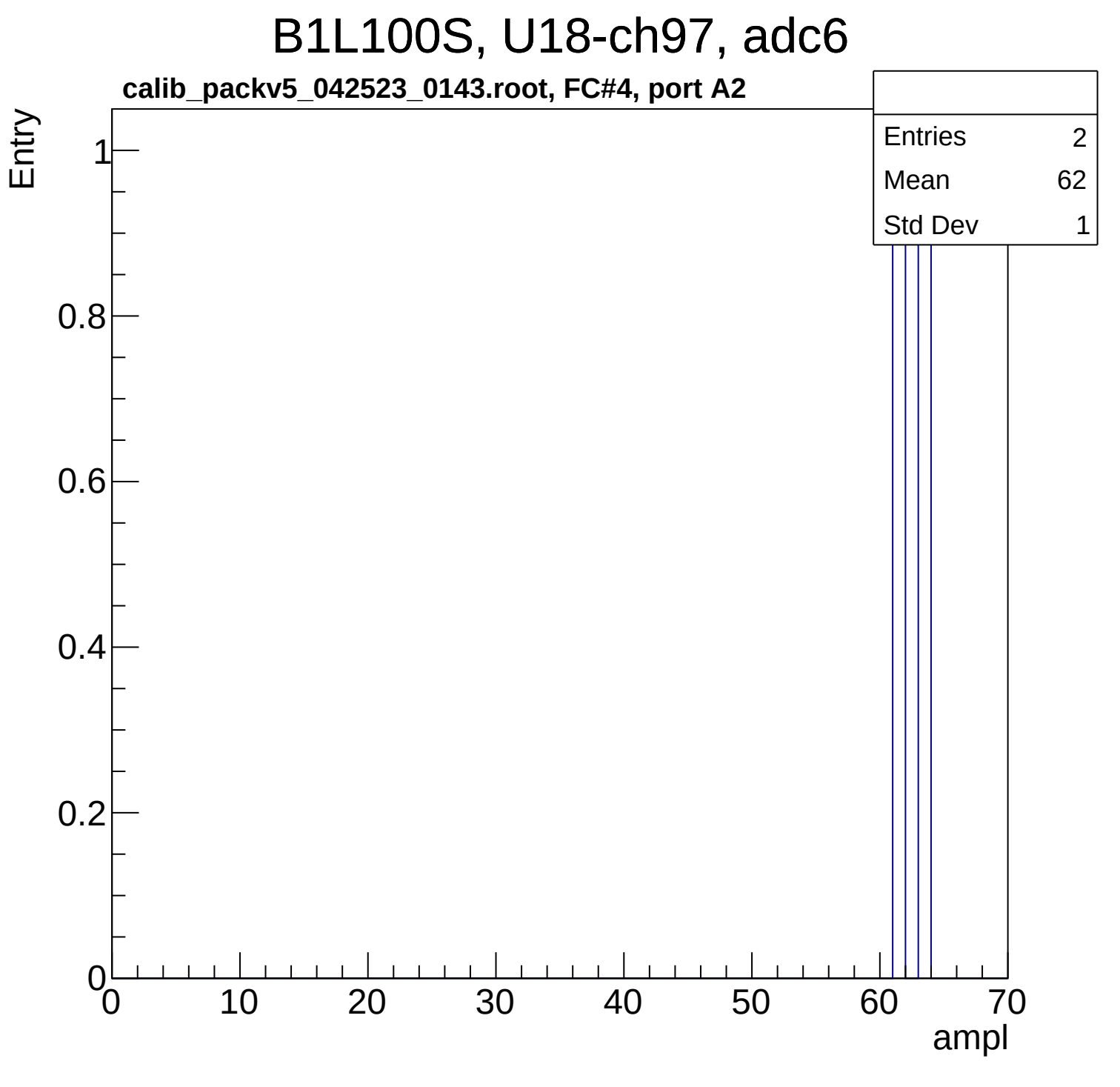

B1L100S, U18-ch97, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 36.97
Std Dev 3.637
Gaus mean : 37.0894
Gaus Width: 4.0700
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

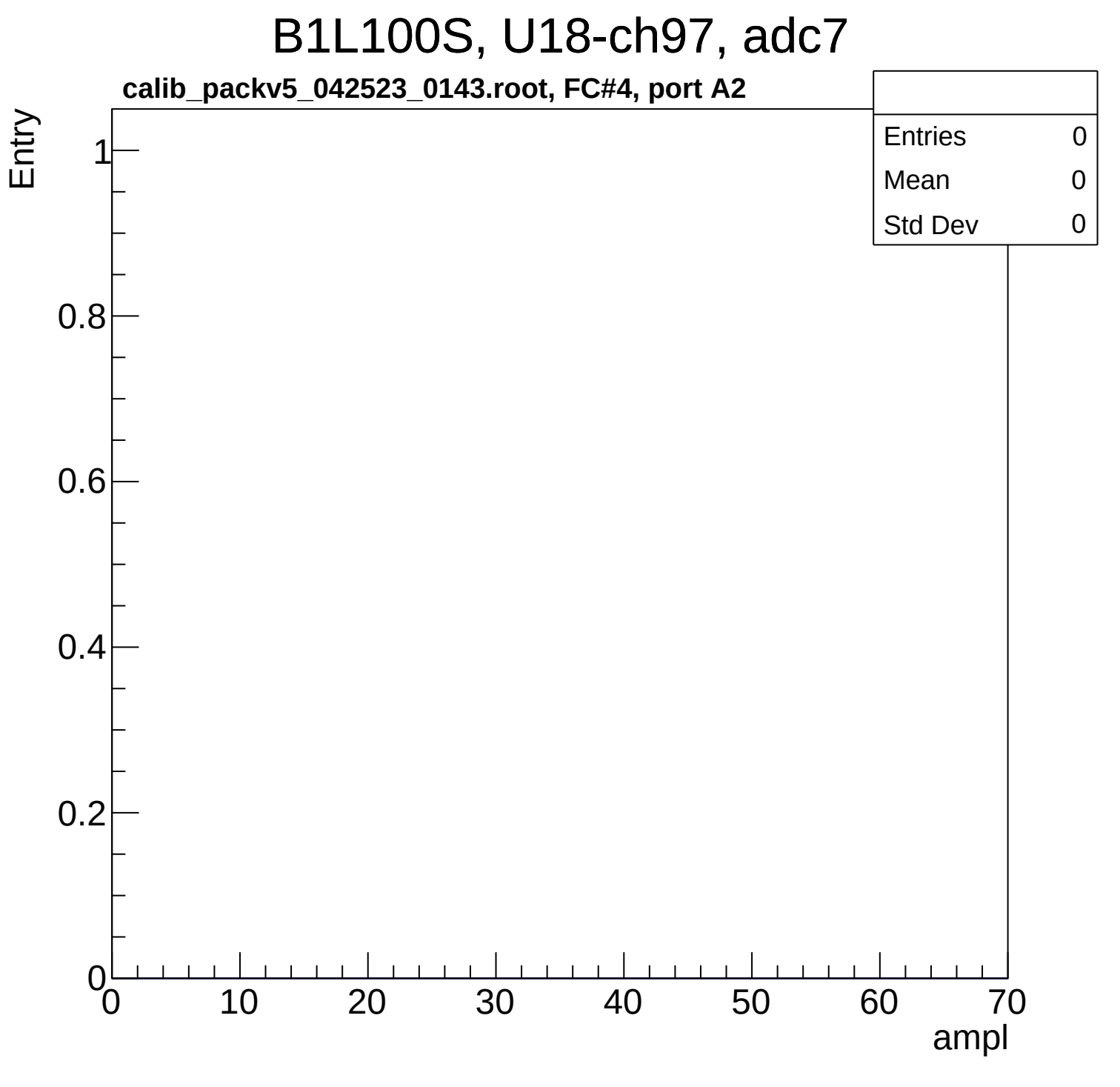

B1L100S, U18-ch97, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 43.11
Std Dev 3.194
Gaus mean : 42.9233
Gaus Width: 2.3729
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

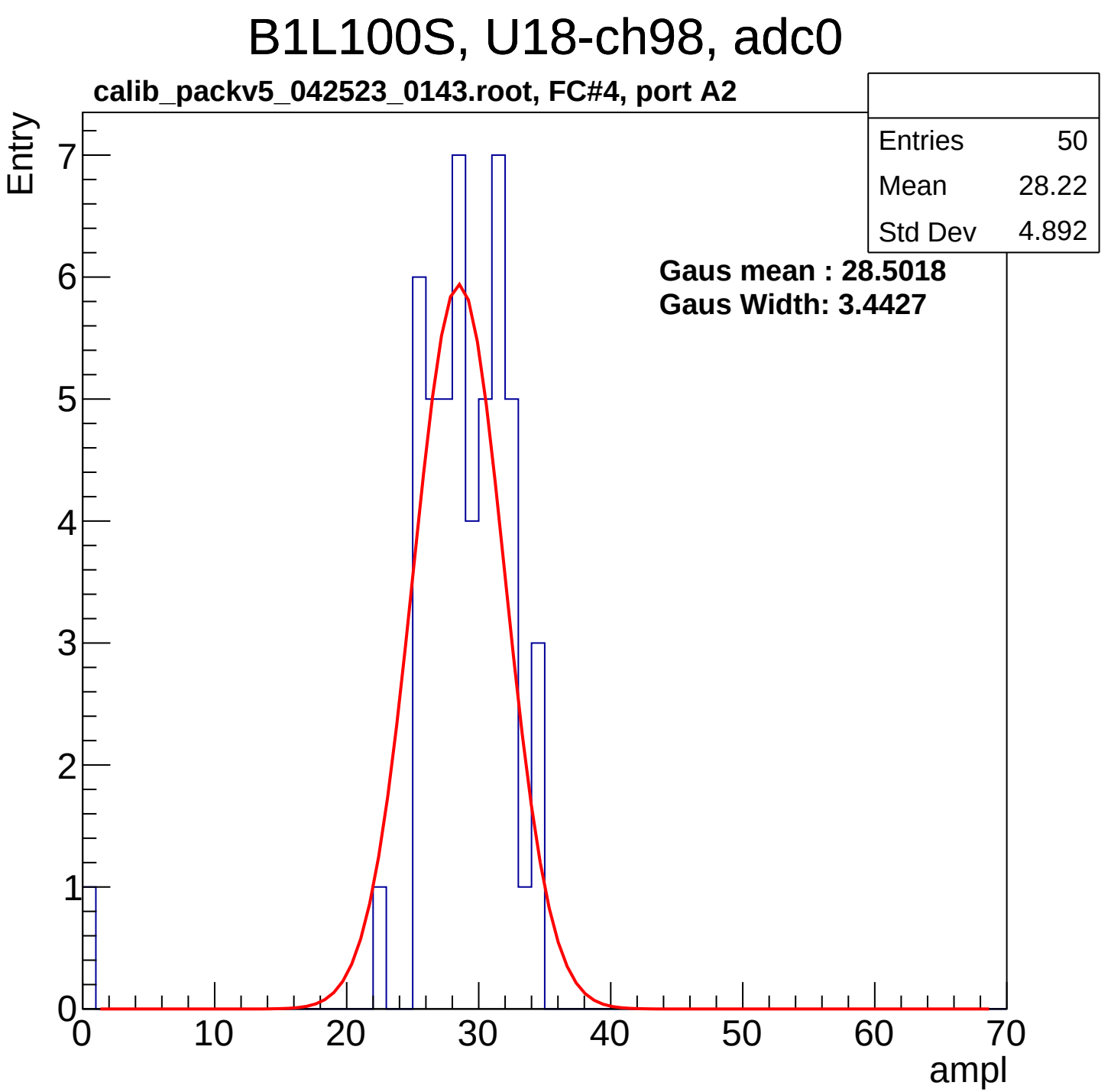

B1L100S, U18-ch97, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 49.14
Std Dev 2.776
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

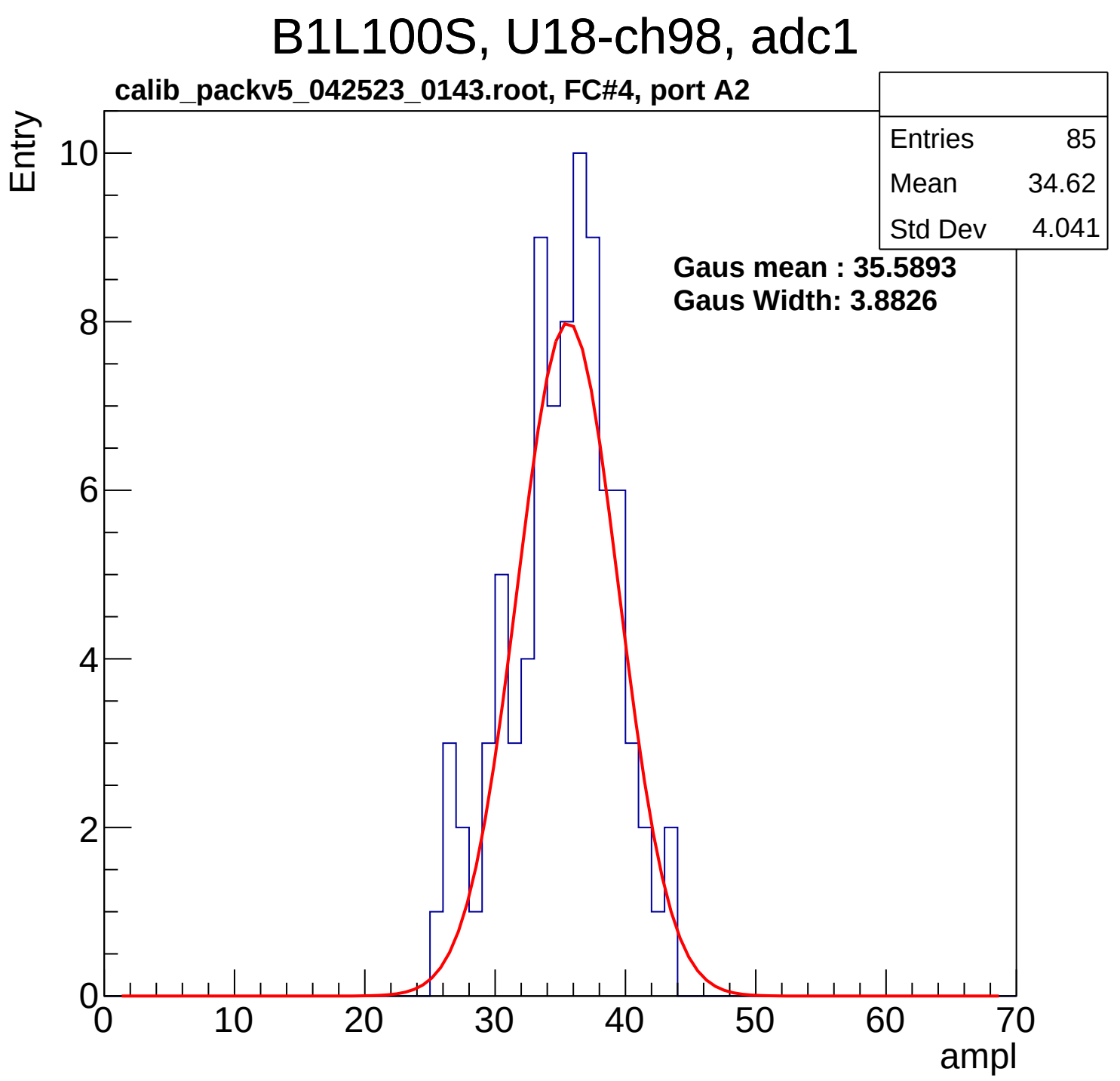

B1L100S, U18-ch97, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 55.9
Std Dev 3.604
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

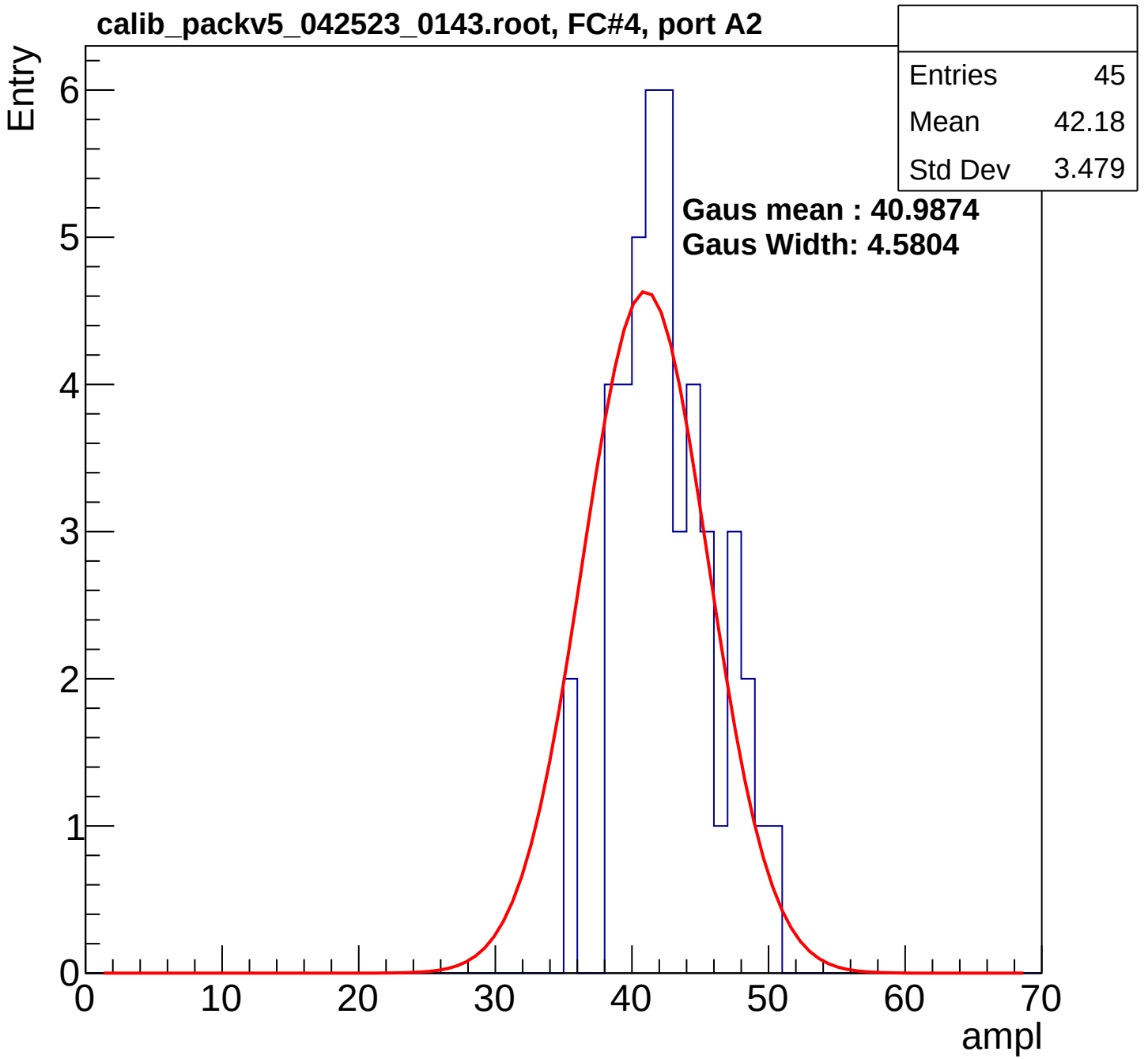

B1L100S, U18-ch97, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 58.34
Std Dev 8.976
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

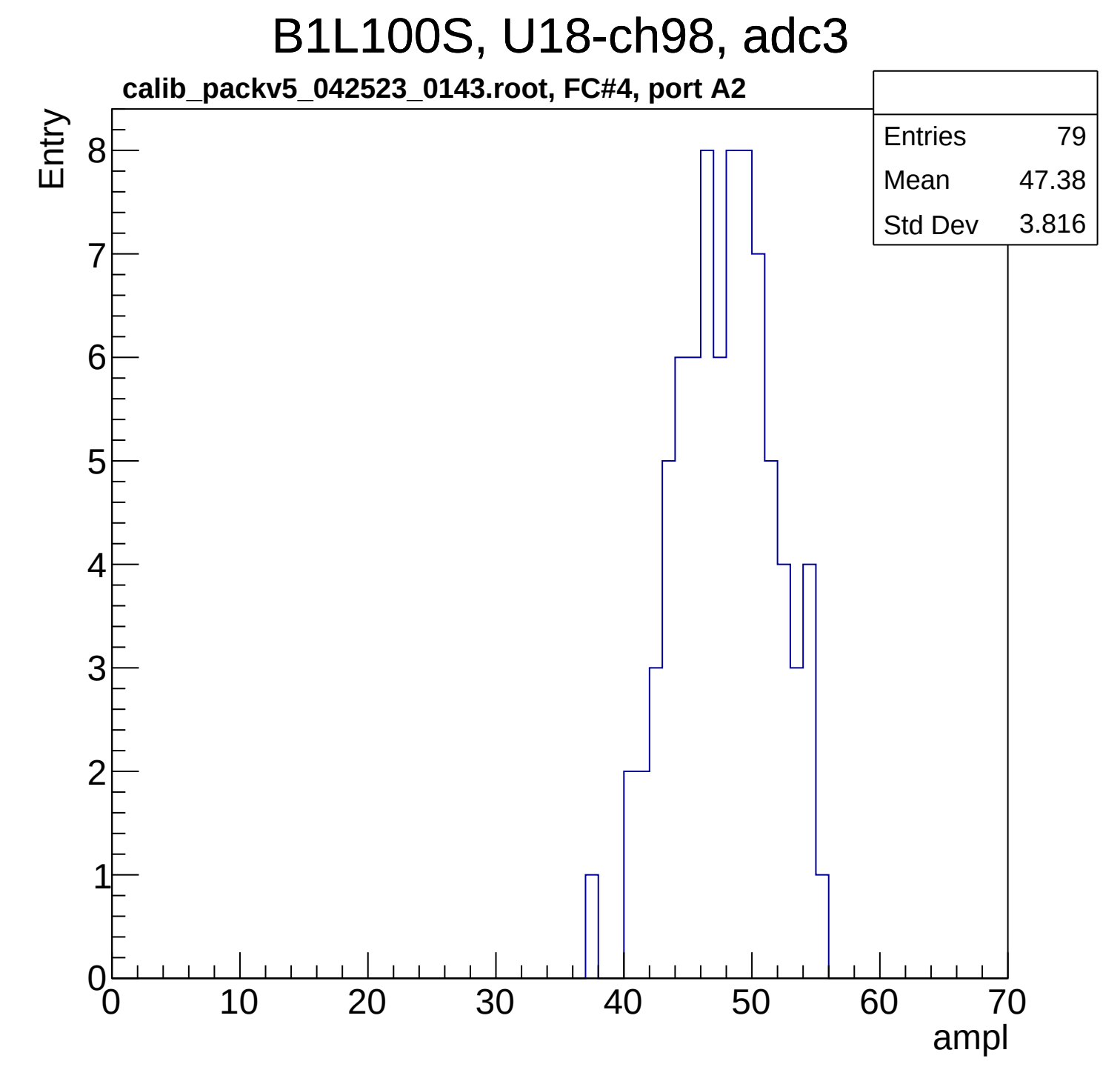

B1L100S, U18-ch97, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 62
Std Dev 1
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

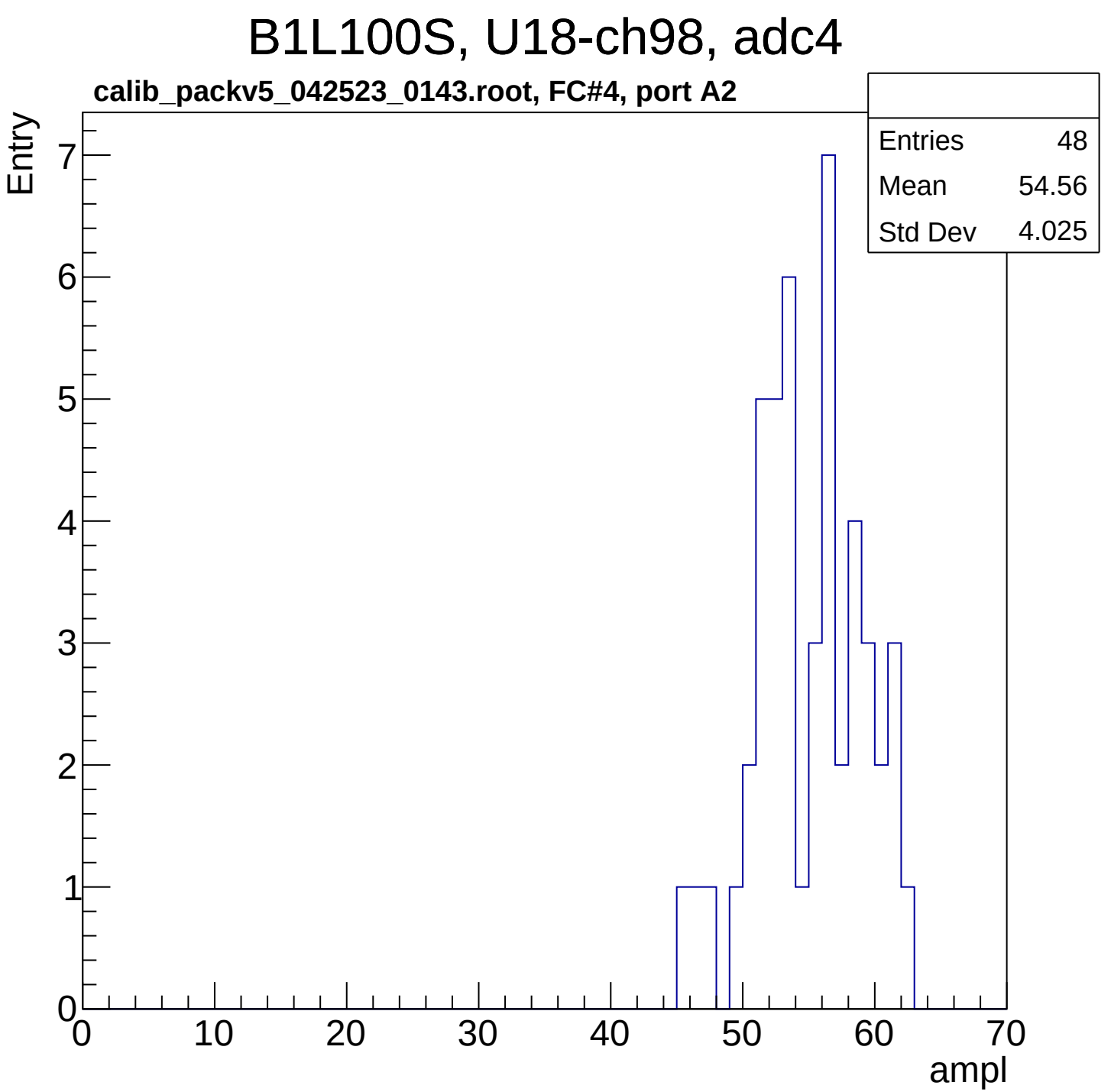

B1L100S, U18-ch97, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

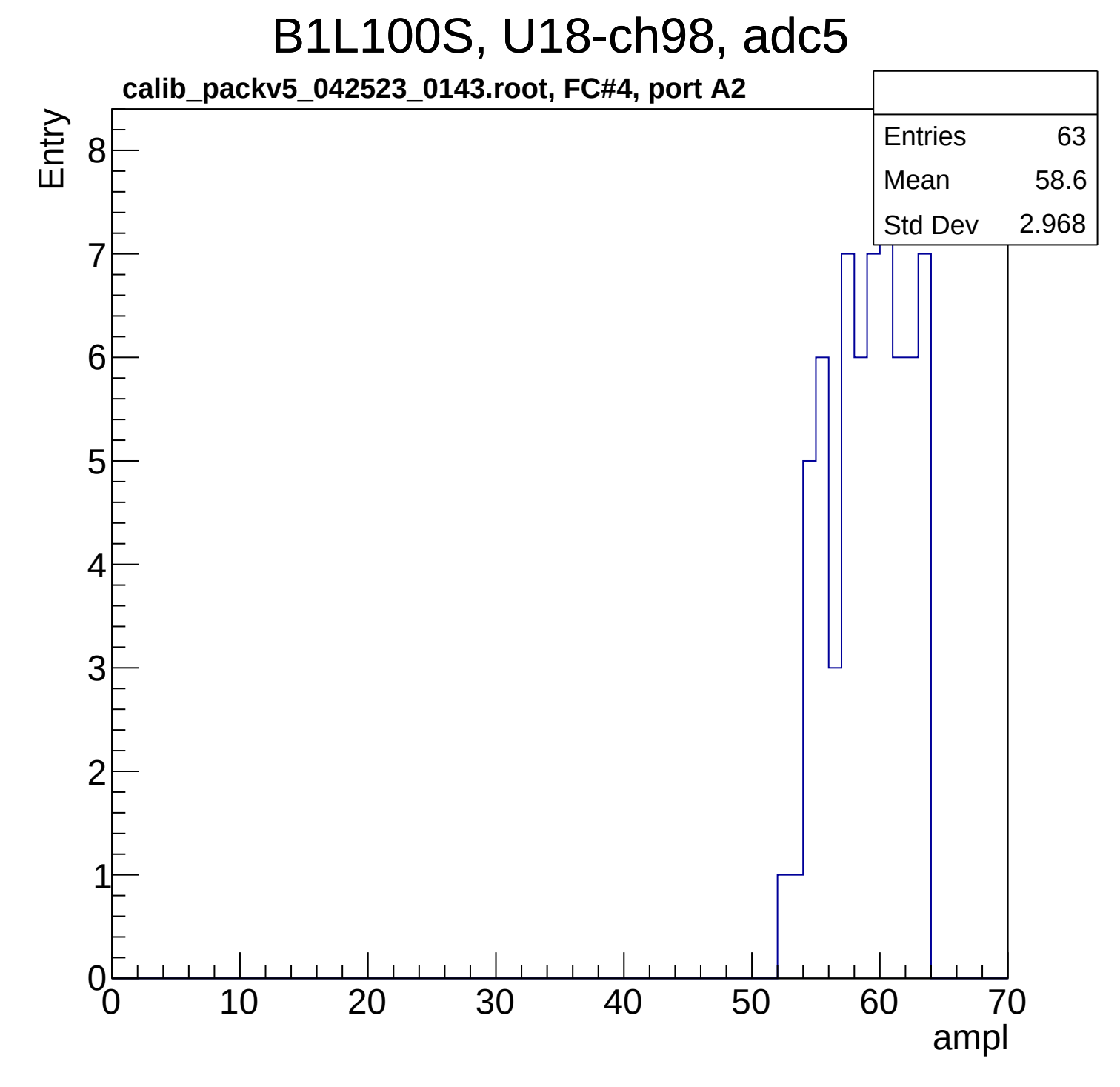

B1L100S, U18-ch98, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 28.22
Std Dev 4.892
Gaus mean : 28.5018
Gaus Width: 3.4427
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

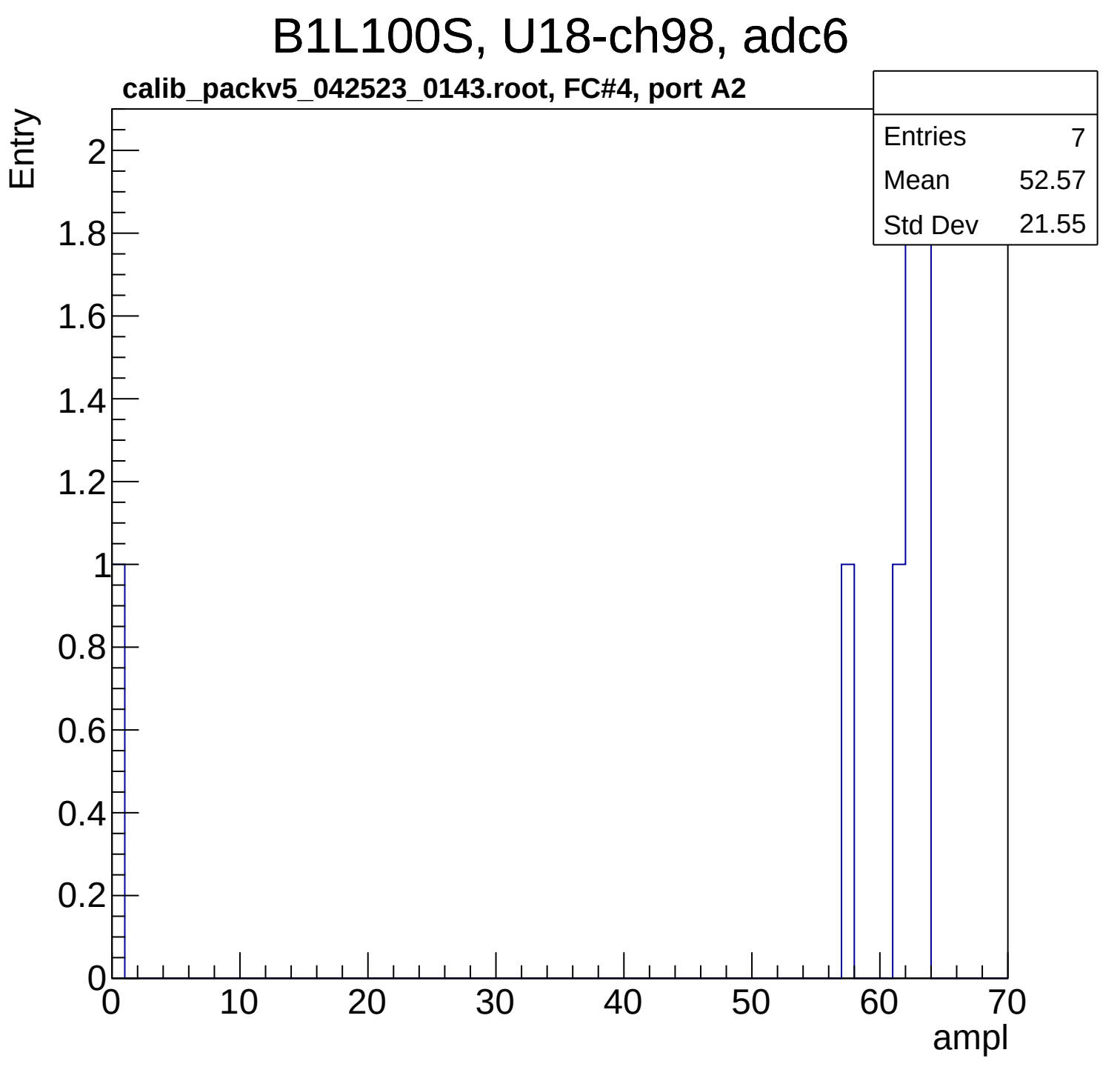

B1L100S, U18-ch98, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 85
Mean 34.62
Std Dev 4.041
Gaus mean : 35.5893
Gaus Width: 3.8826
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

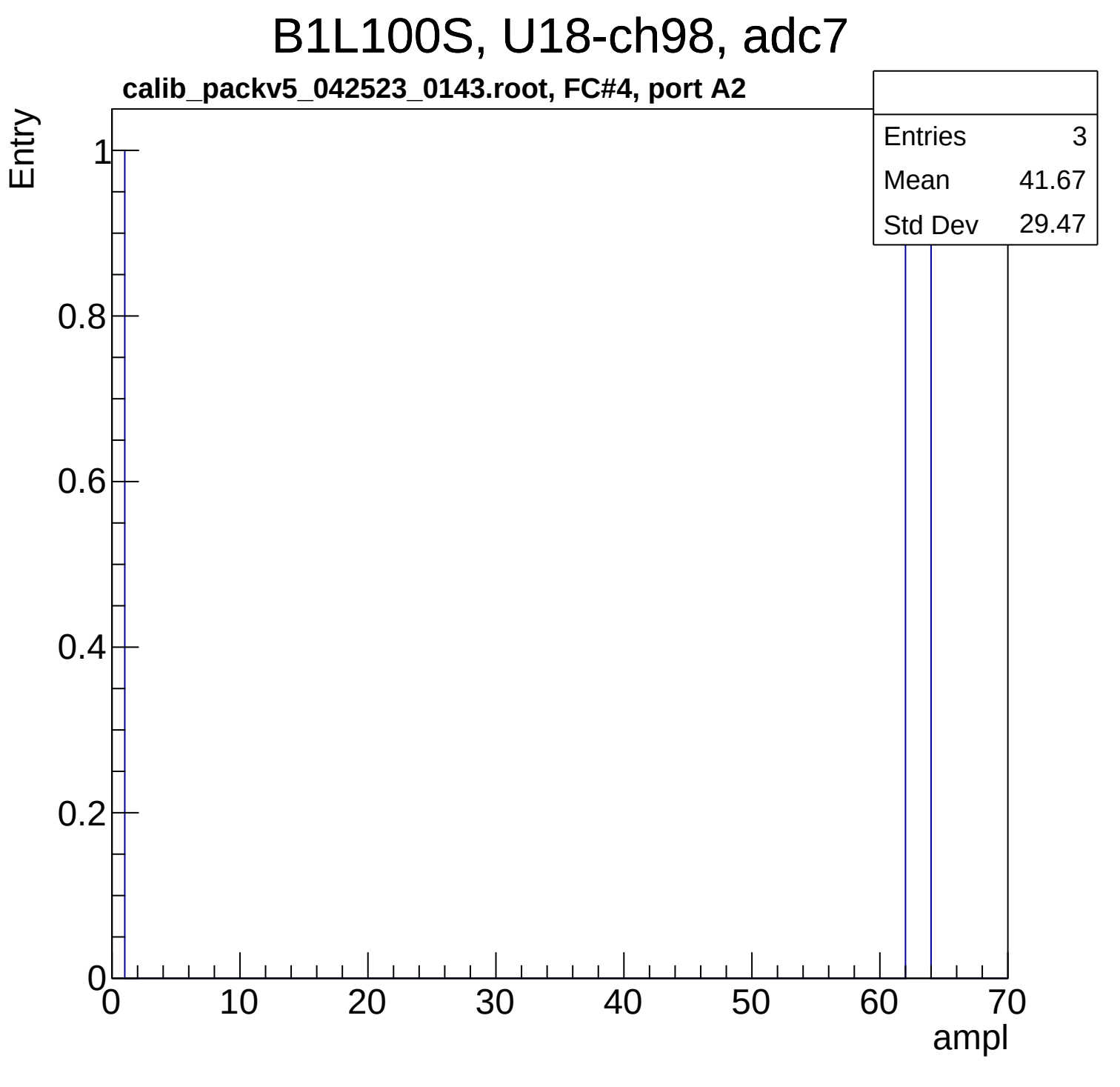

B1L100S, U18-ch98, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 45
Mean 42.18
Std Dev 3.479
Gaus mean : 40.9874
Gaus Width: 4.5804
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

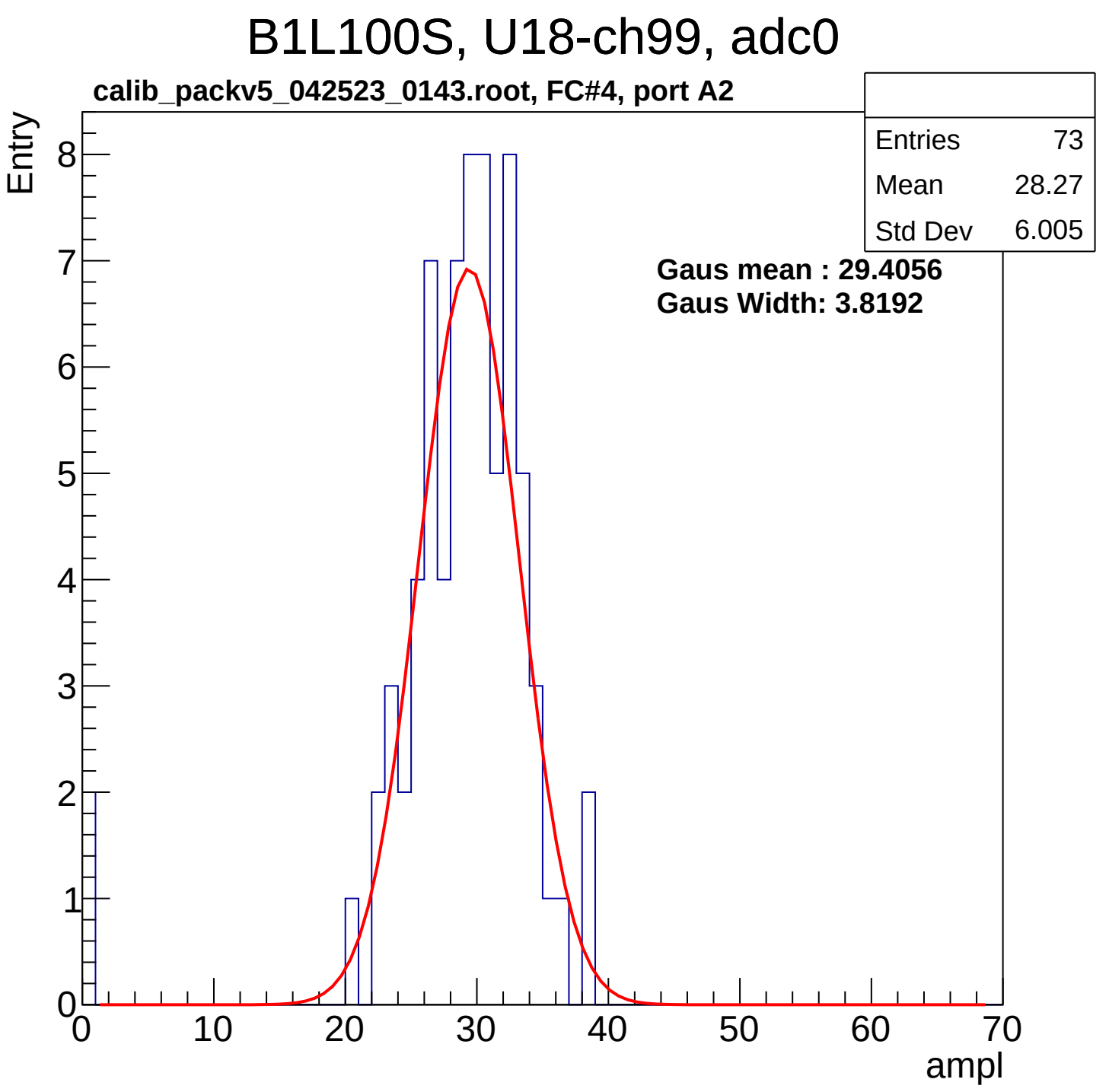

B1L100S, U18-ch98, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 47.38
Std Dev 3.816
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

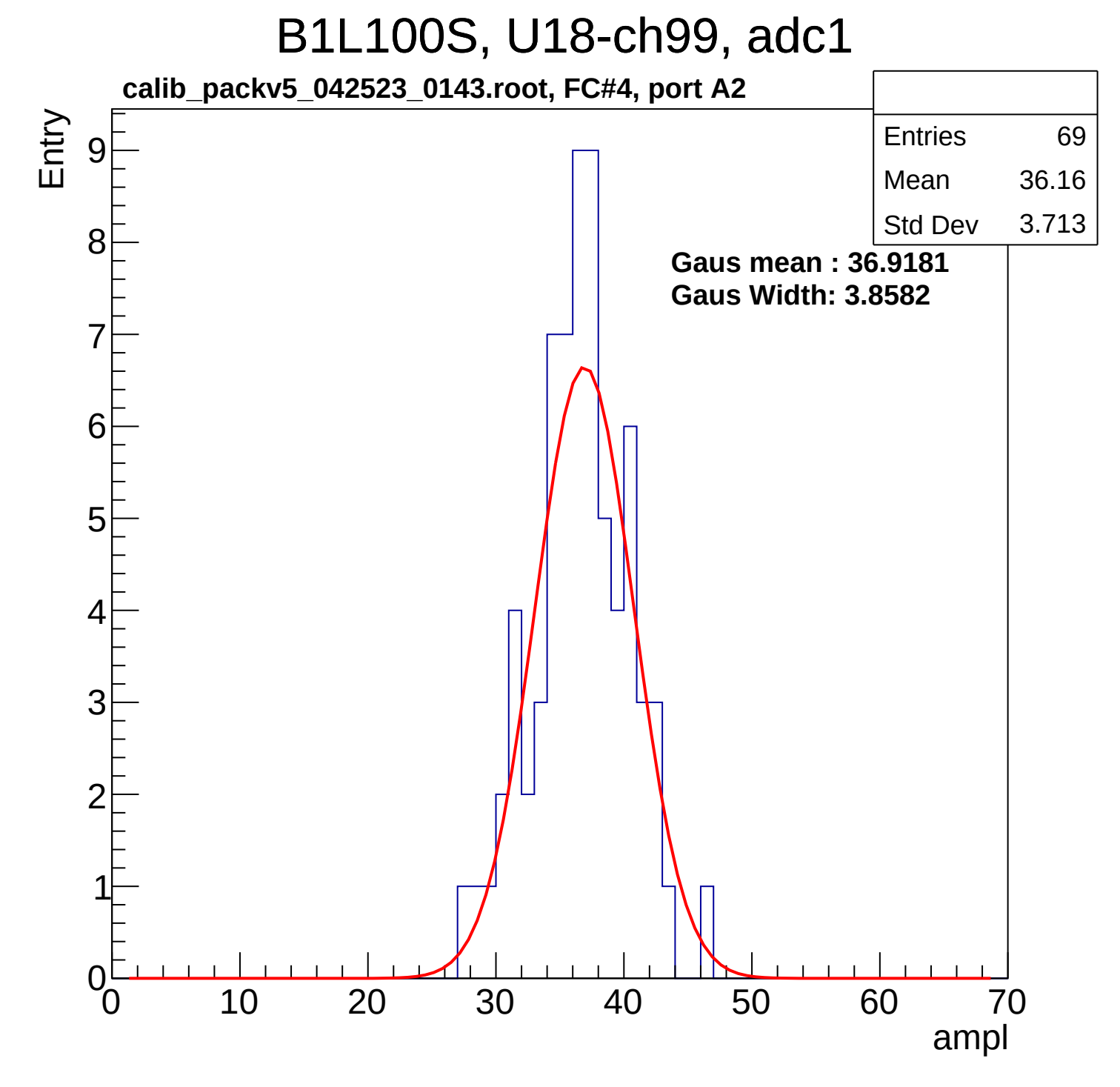

B1L100S, U18-ch98, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 54.56
Std Dev 4.025
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

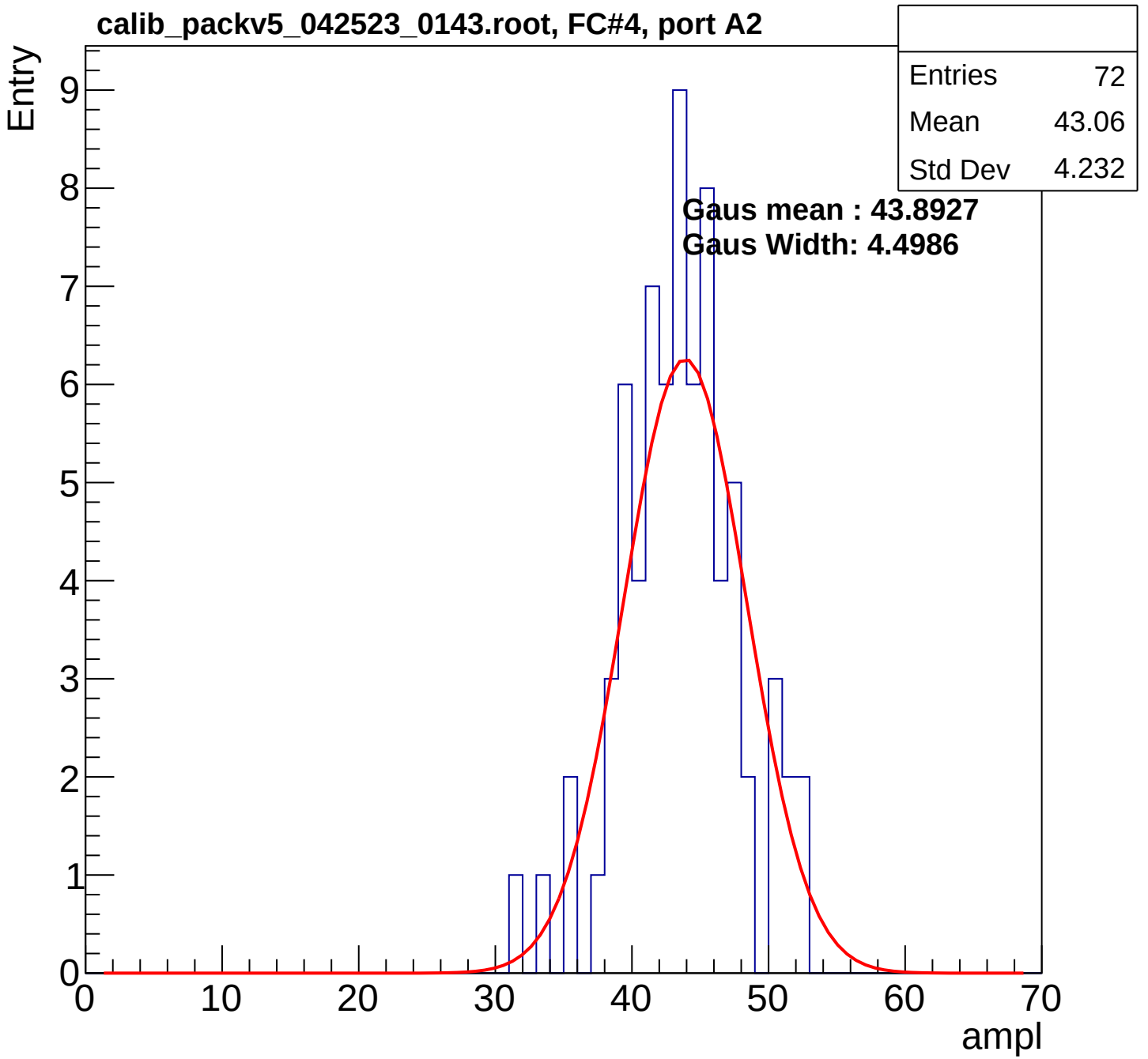

B1L100S, U18-ch98, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 58.6
Std Dev 2.968
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

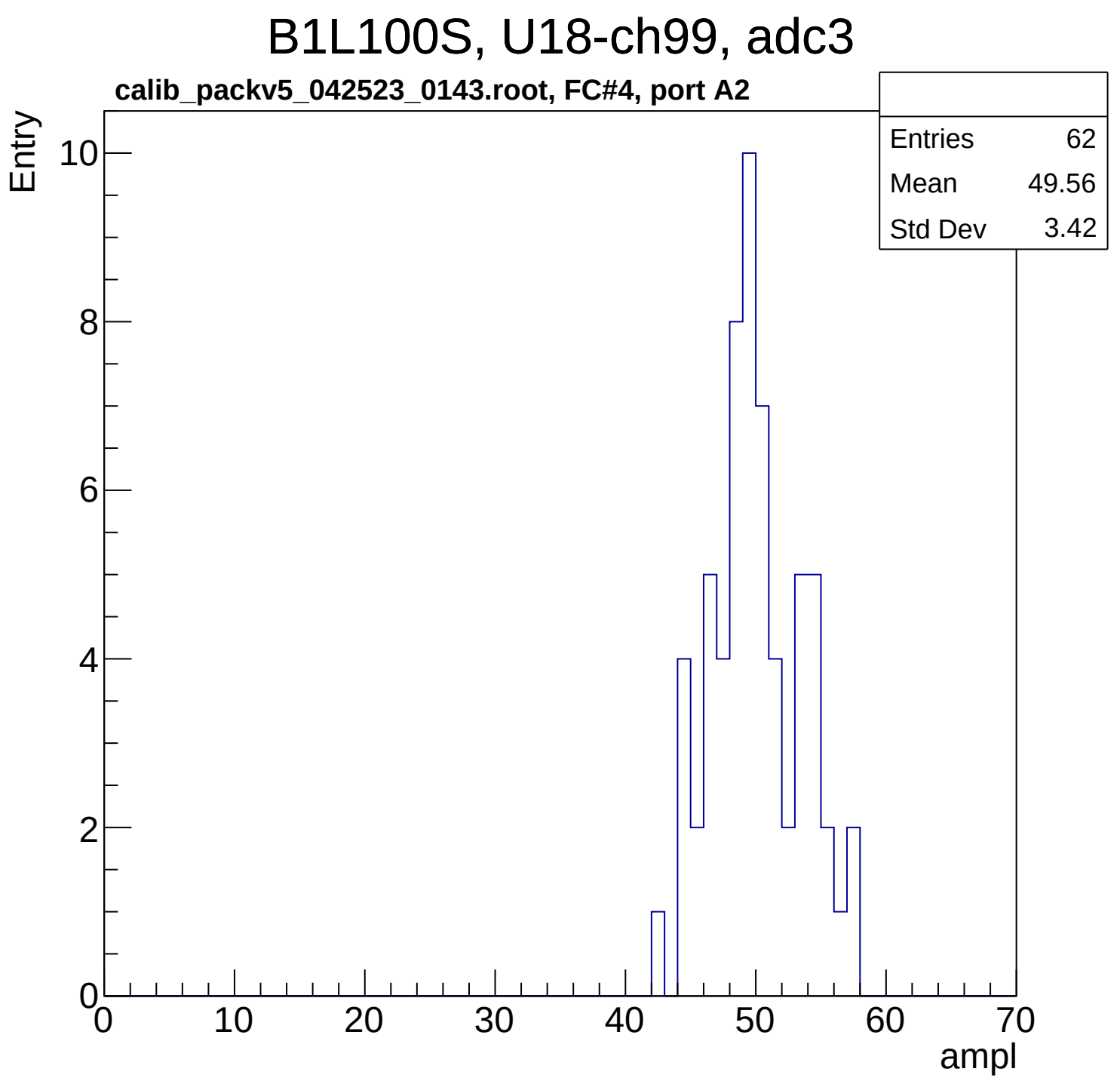

B1L100S, U18-ch98, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 52.57
Std Dev 21.55
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

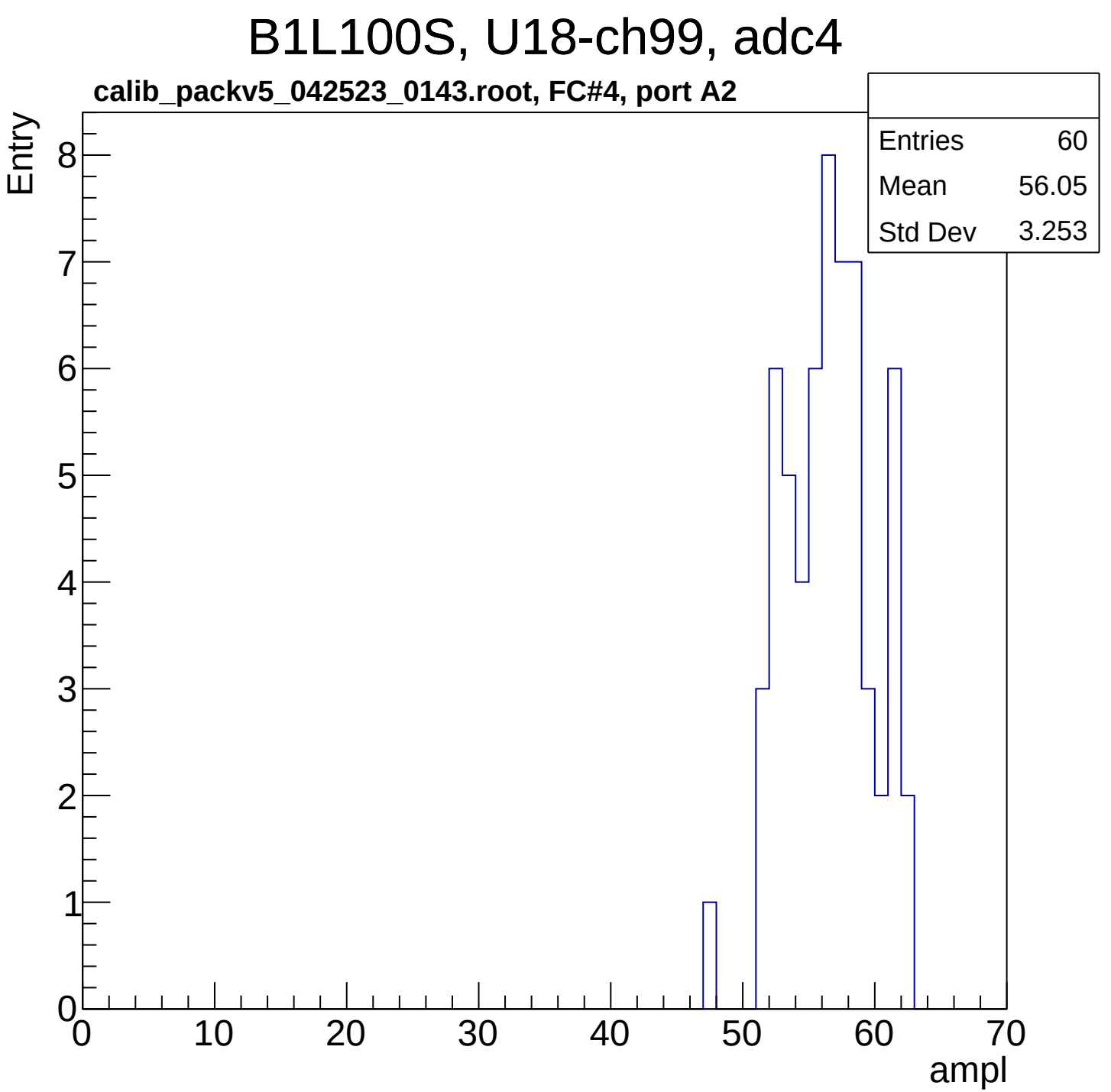

B1L100S, U18-ch98, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 41.67
Std Dev 29.47
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

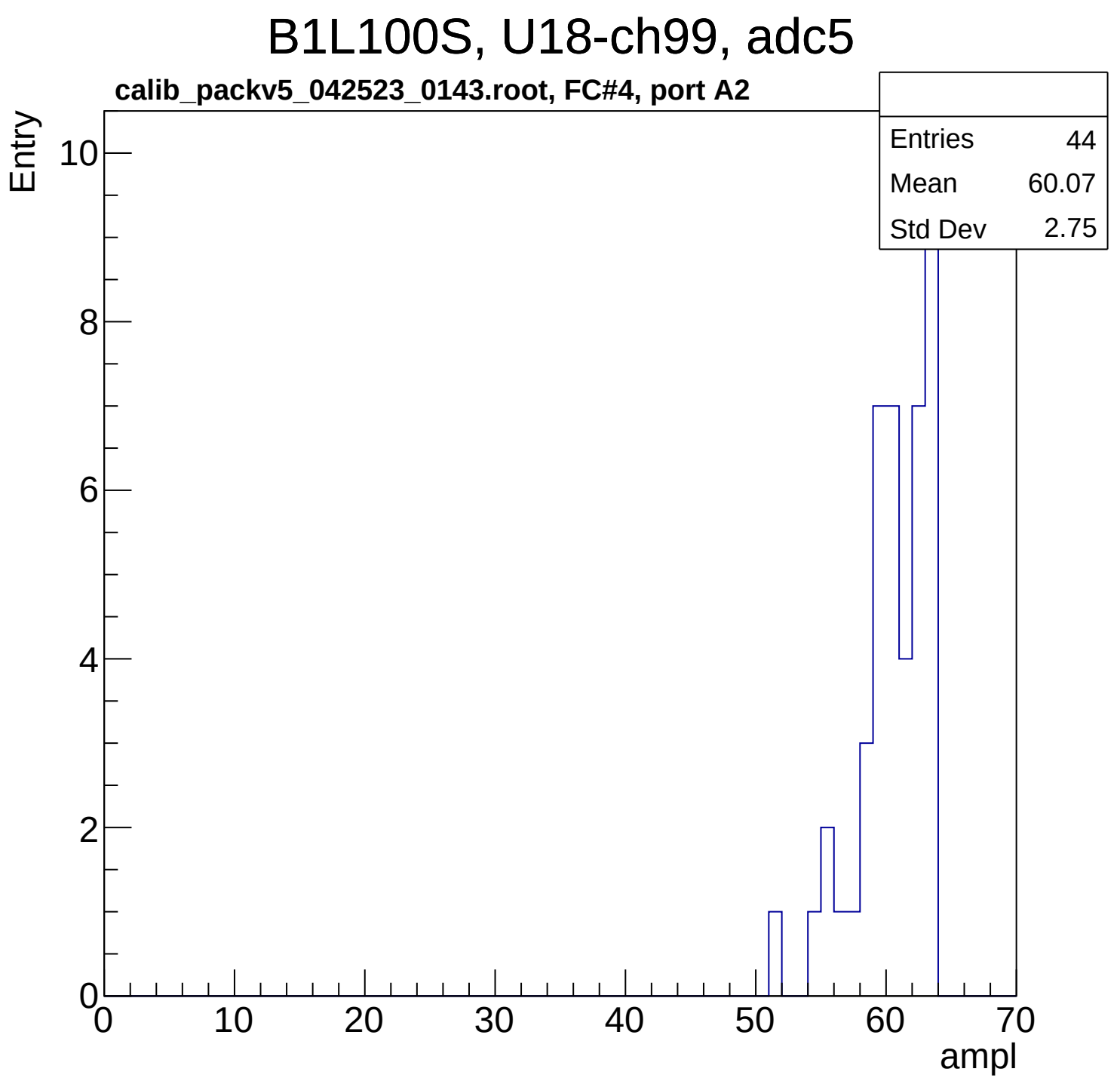

B1L100S, U18-ch99, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 28.27
Std Dev 6.005
Gaus mean : 29.4056
Gaus Width: 3.8192
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

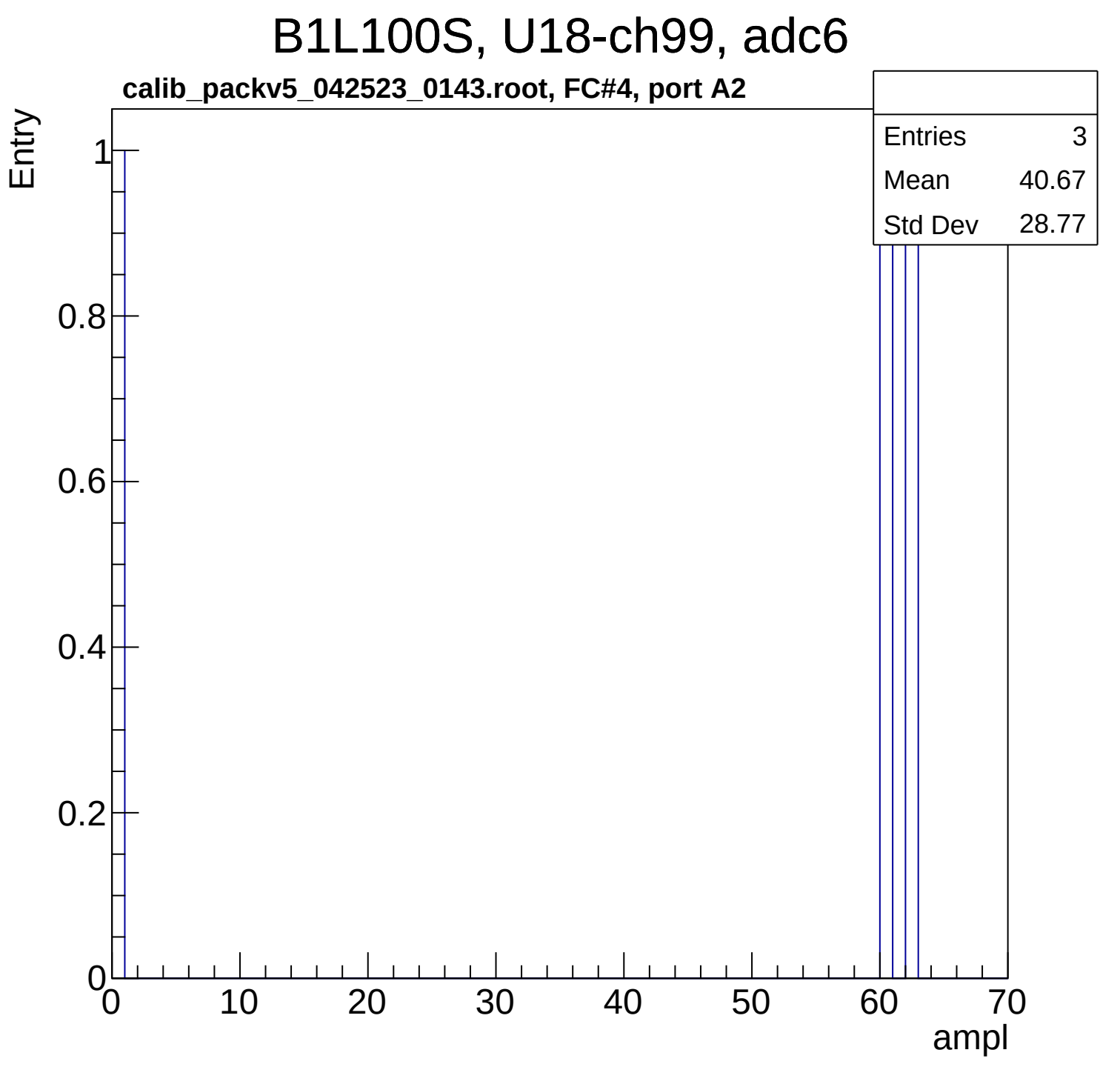

B1L100S, U18-ch99, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 36.16
Std Dev 3.713
Gaus mean : 36.9181
Gaus Width: 3.8582
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

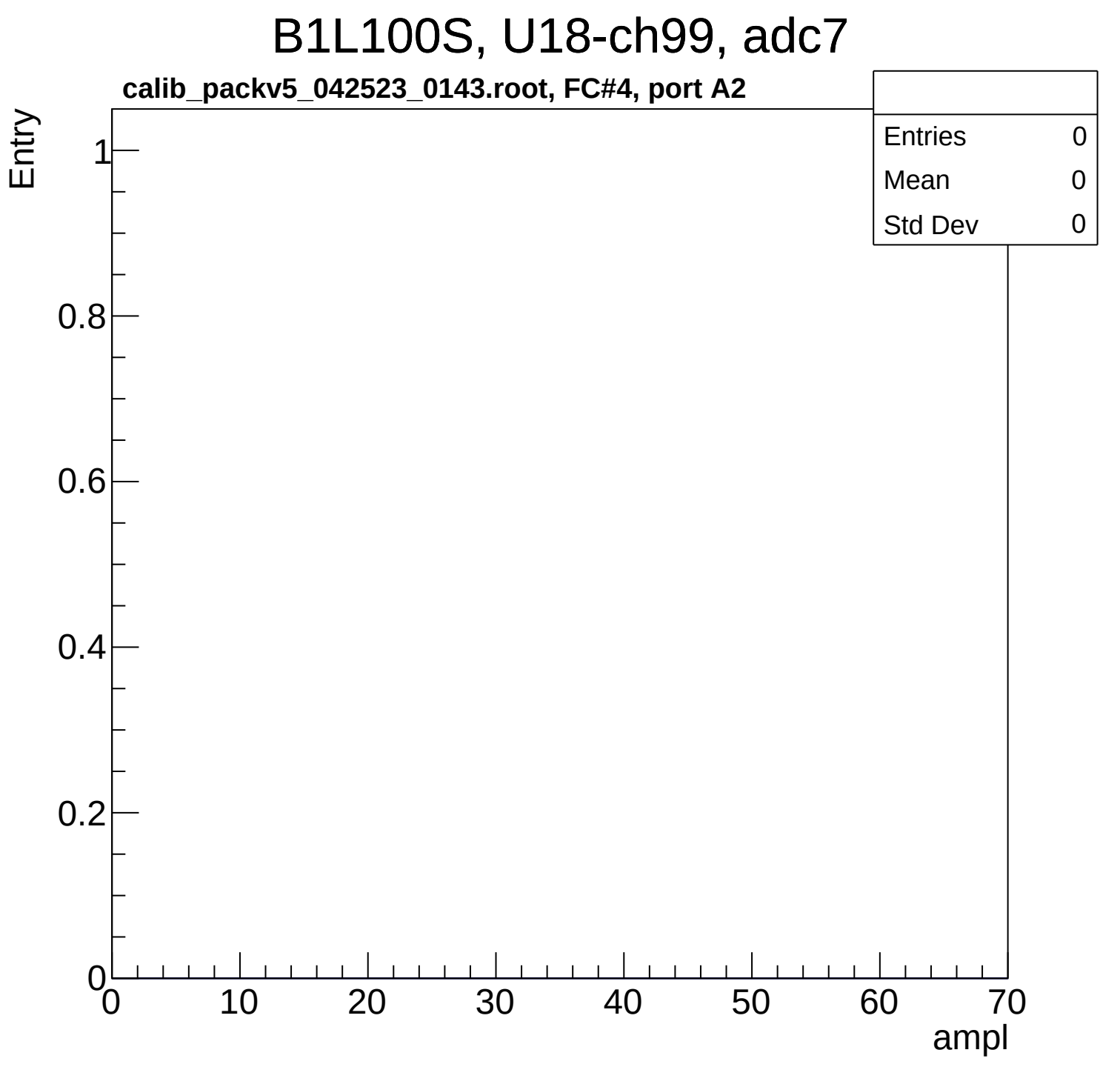

B1L100S, U18-ch99, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 43.06
Std Dev 4.232
Gaus mean : 43.8927
Gaus Width: 4.4986
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

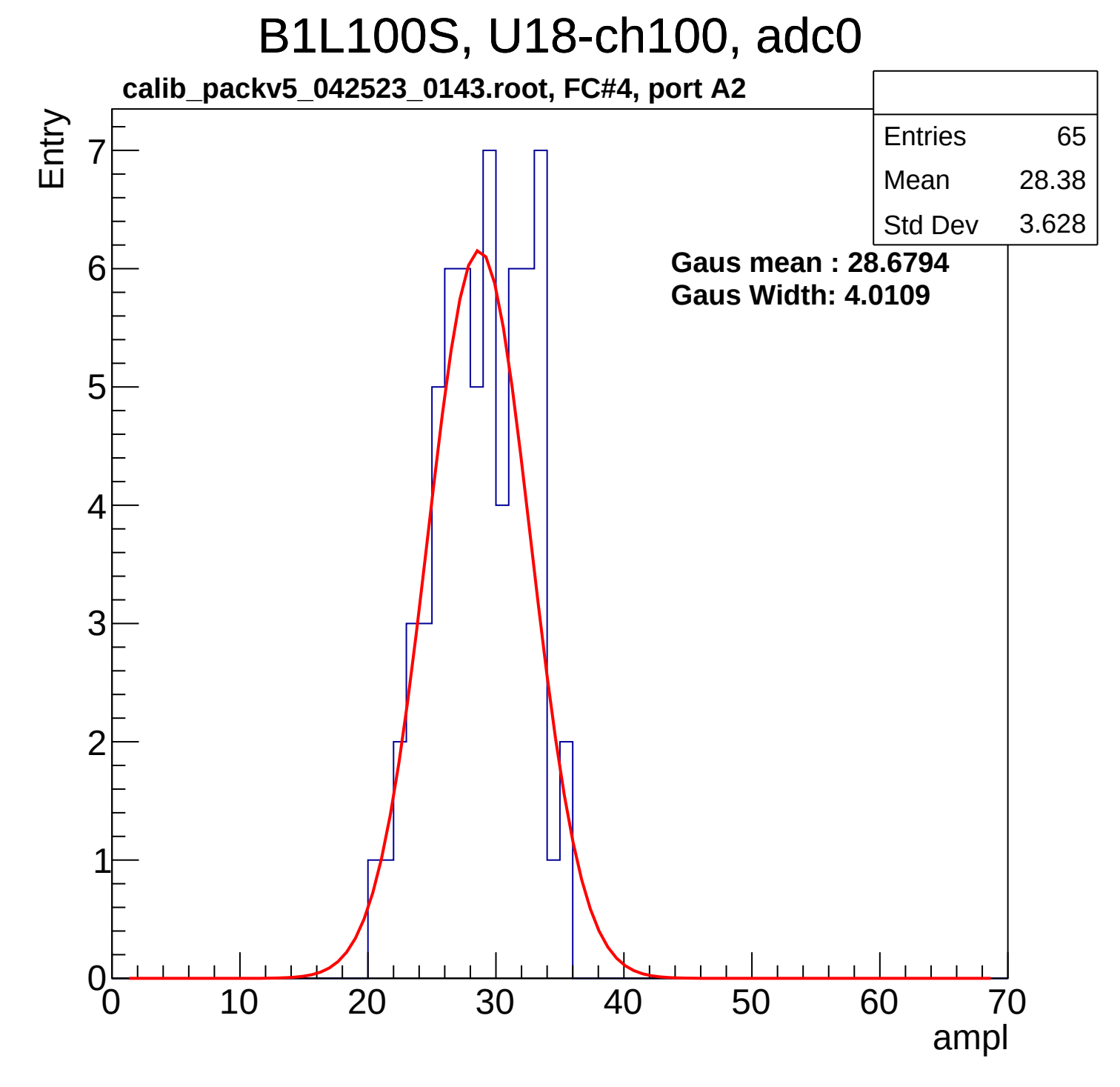

B1L100S, U18-ch99, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 49.56
Std Dev 3.42
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

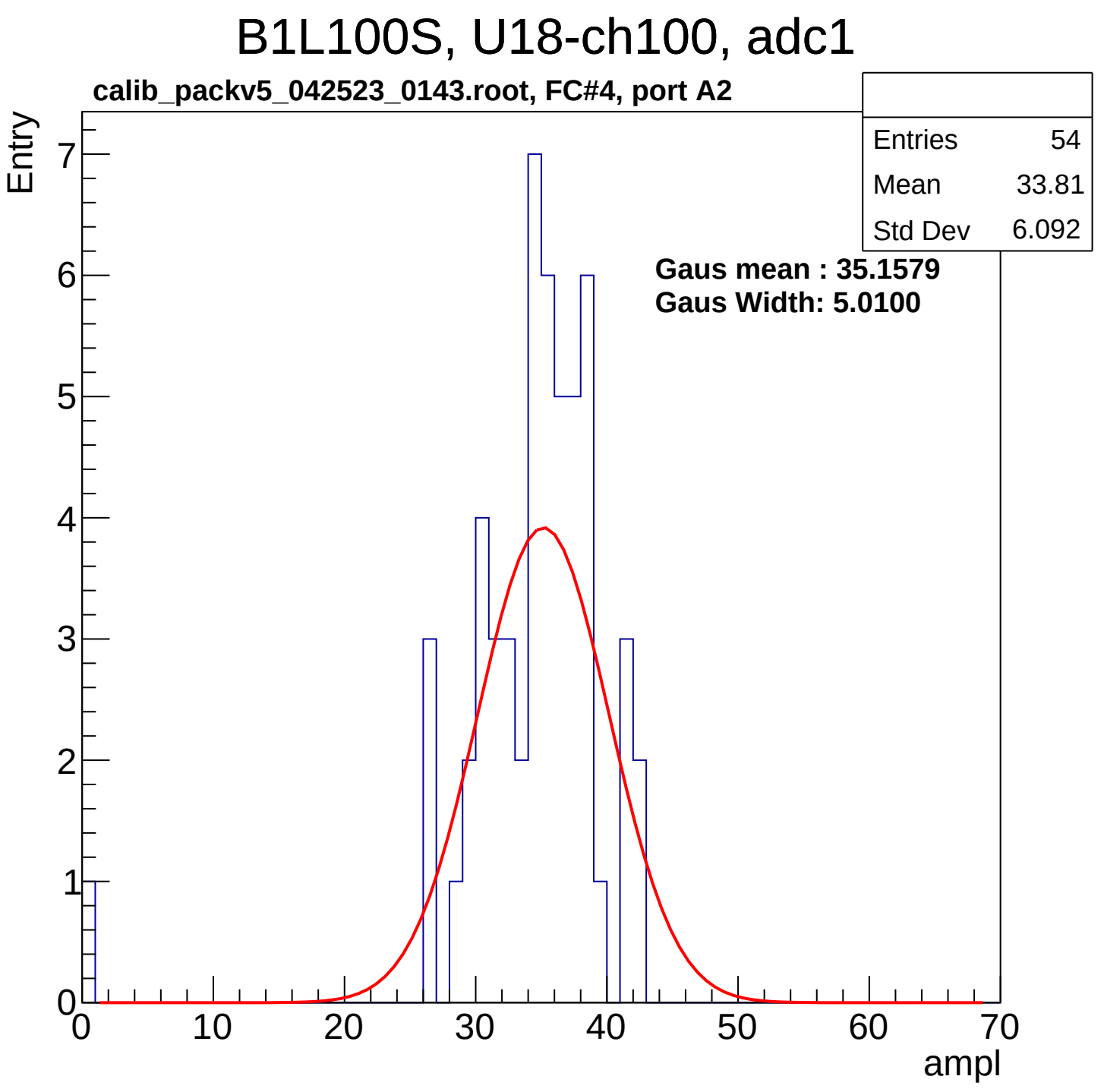

B1L100S, U18-ch99, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 56.05
Std Dev 3.253
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

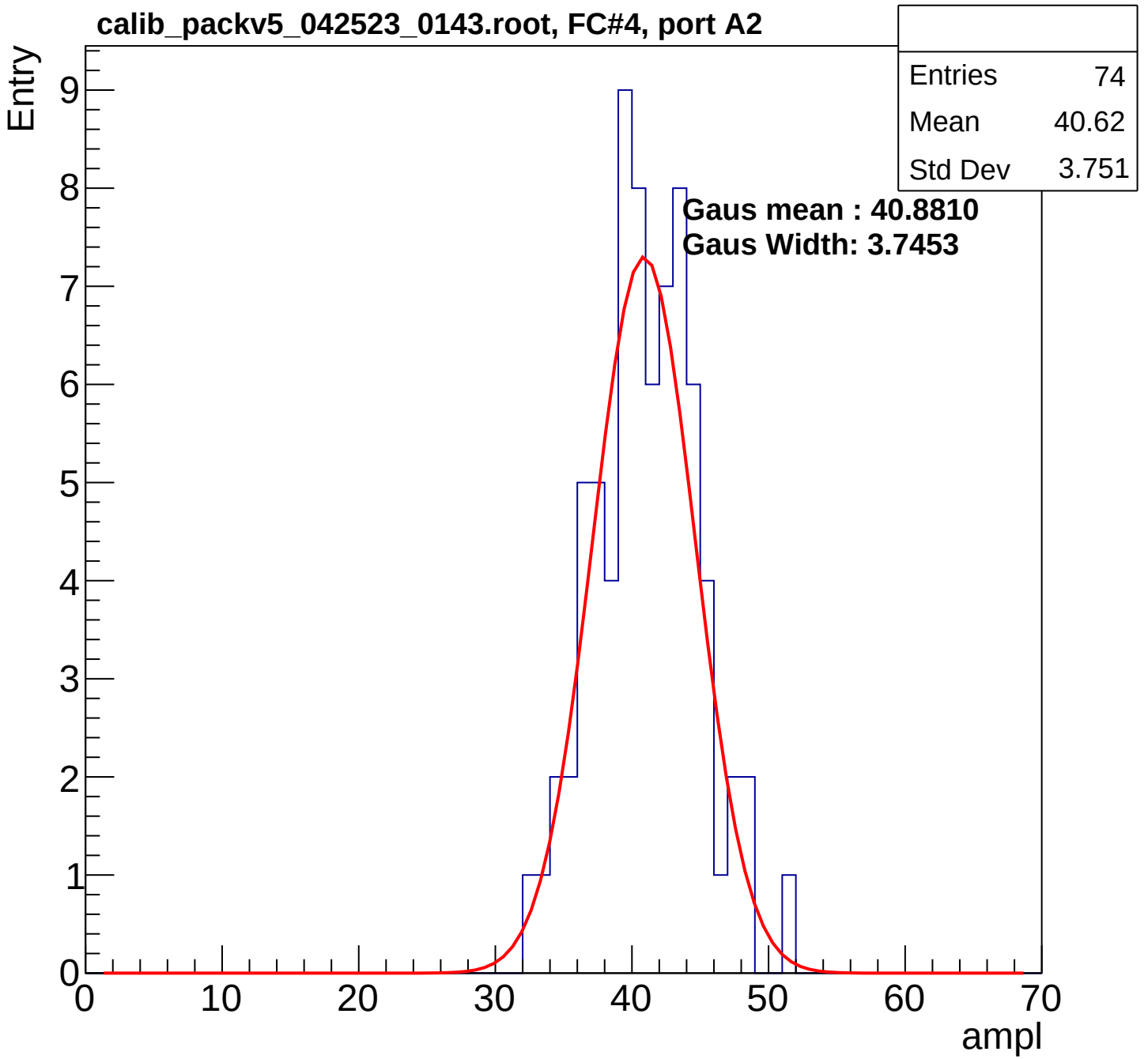

B1L100S, U18-ch99, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 44
Mean 60.07
Std Dev 2.75
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

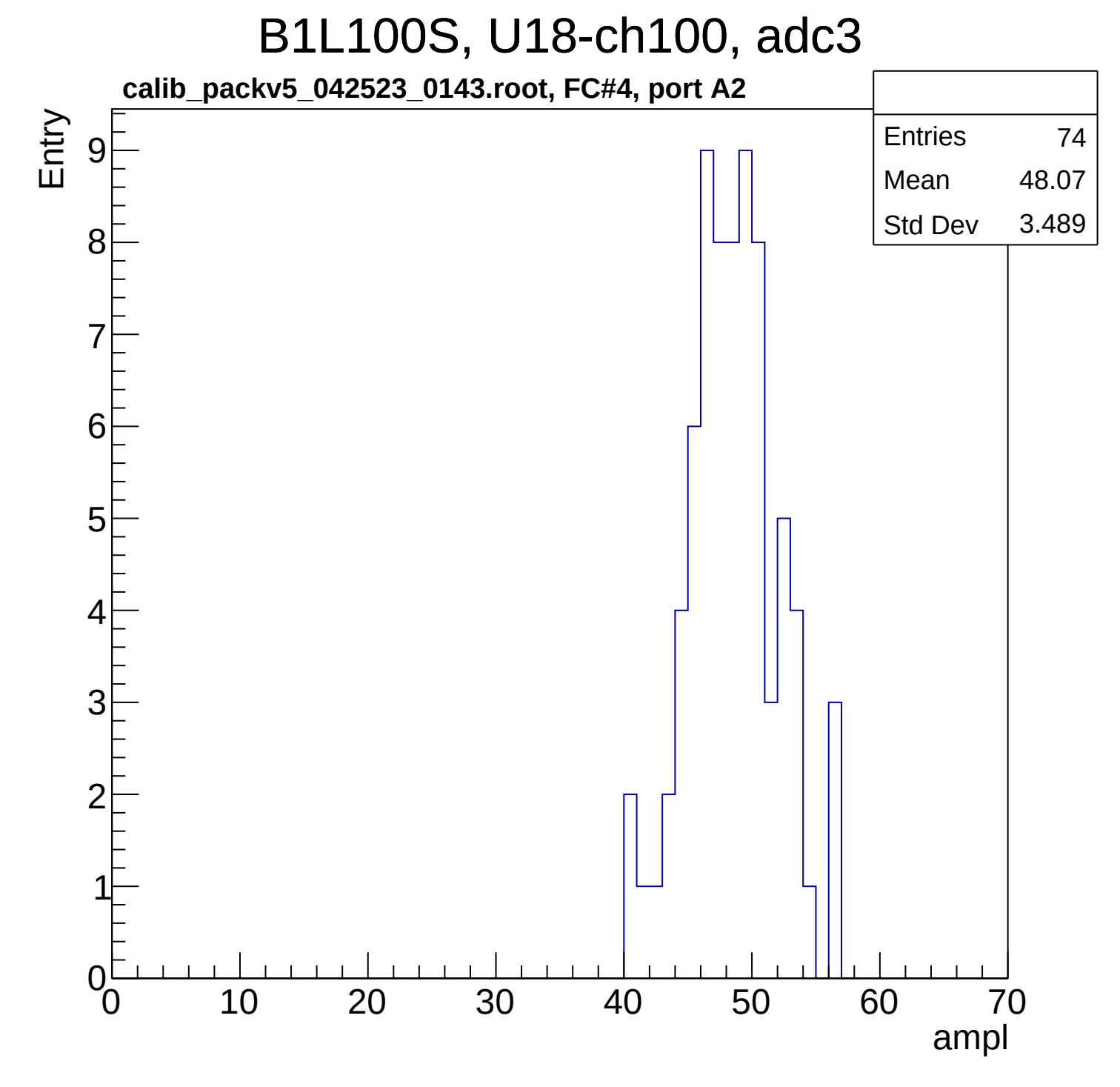

B1L100S, U18-ch99, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 40.67
Std Dev 28.77
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

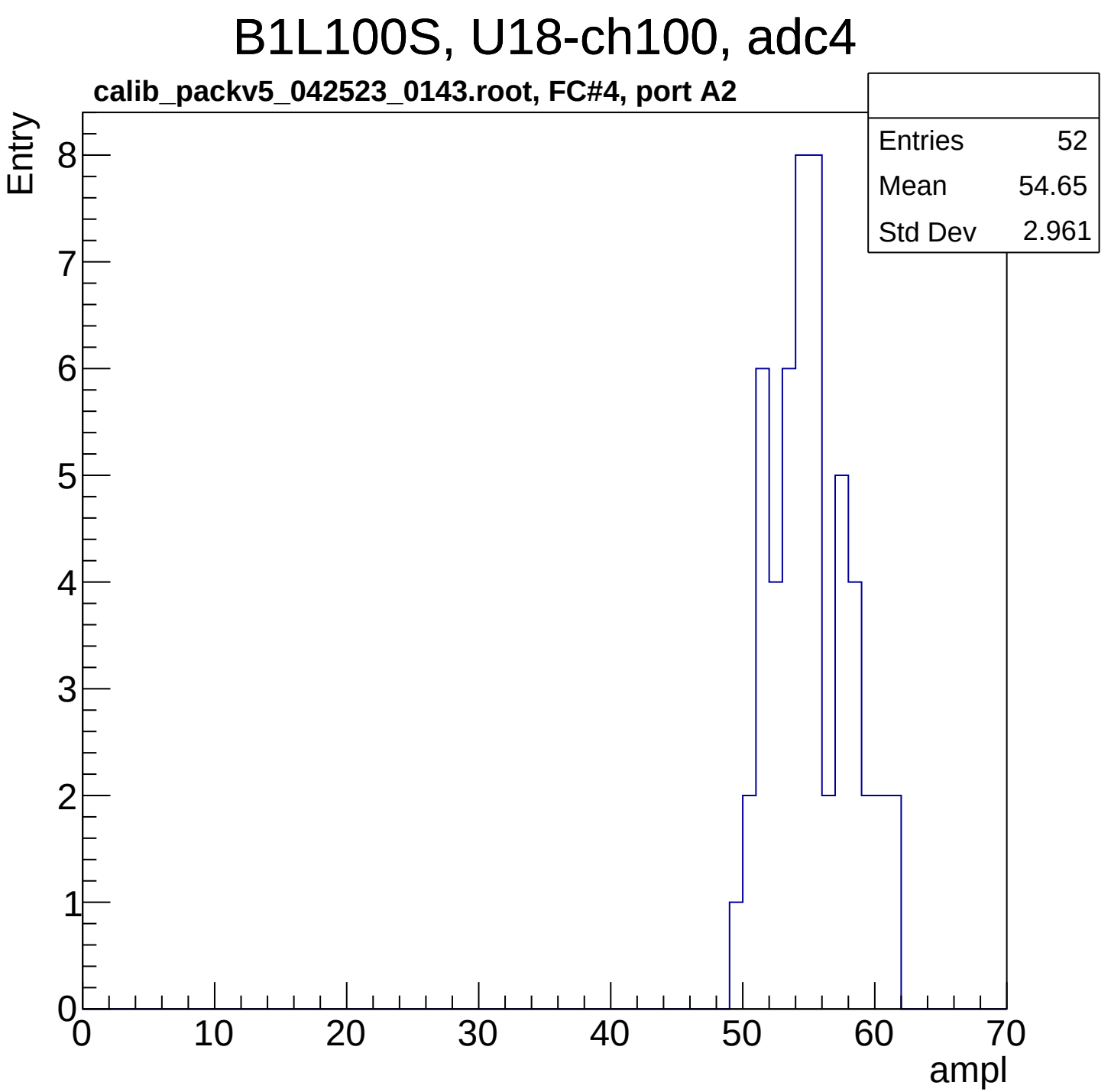

B1L100S, U18-ch99, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

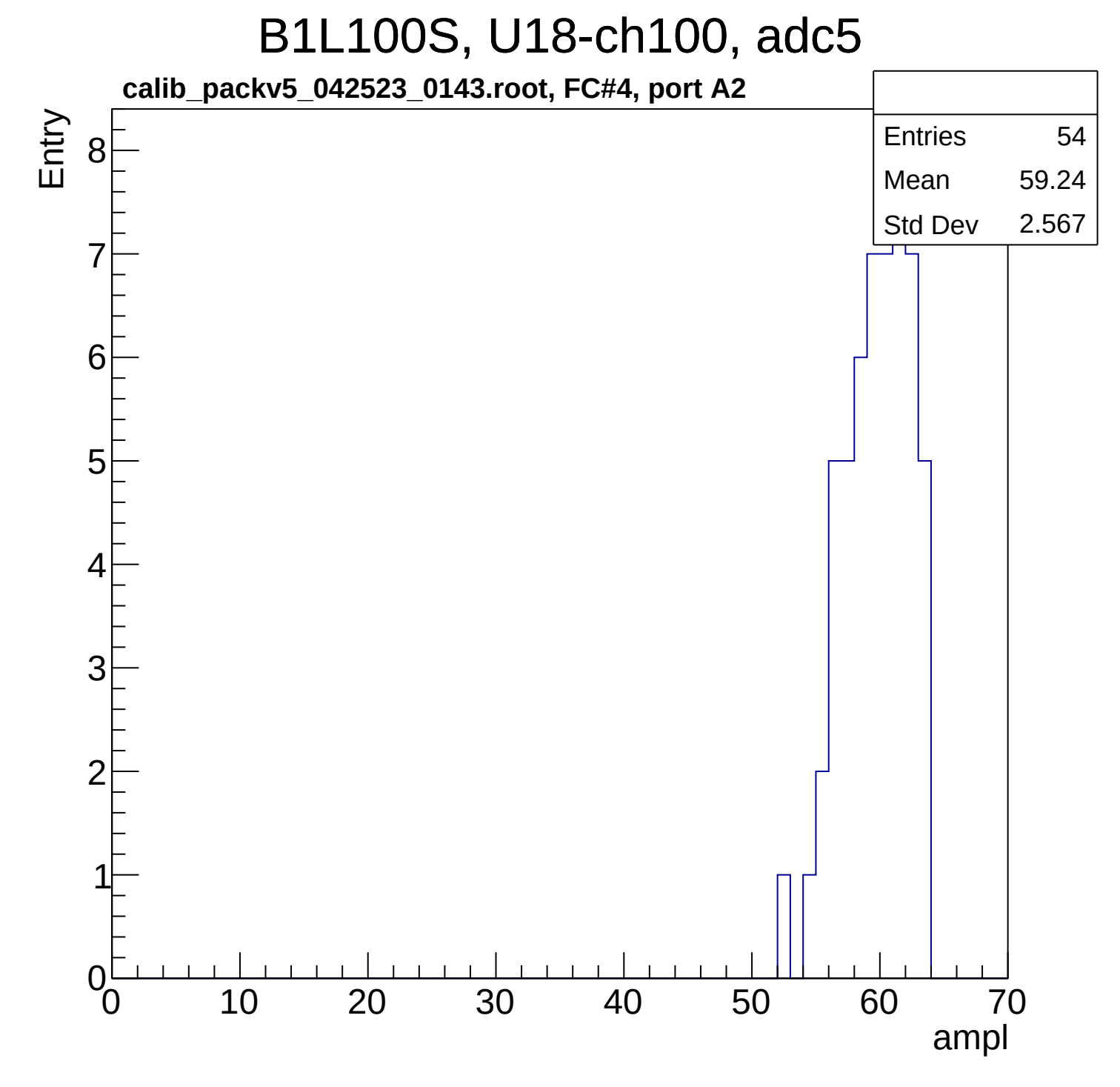

B1L100S, U18-ch100, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 28.38
Std Dev 3.628
Gaus mean : 28.6794
Gaus Width: 4.0109
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

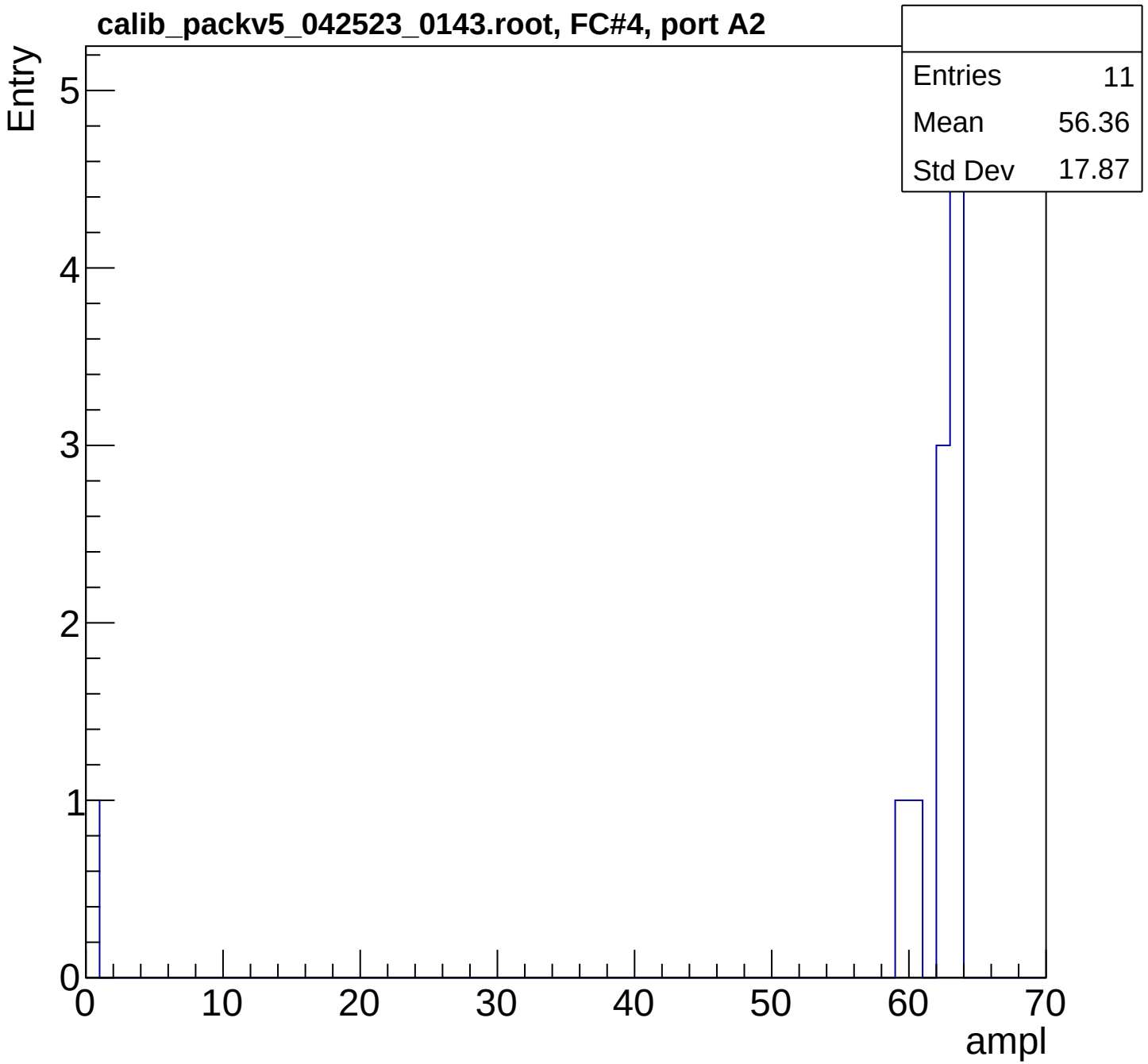

B1L100S, U18-ch100, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 33.81
Std Dev 6.092
Gaus mean : 35.1579
Gaus Width: 5.0100
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

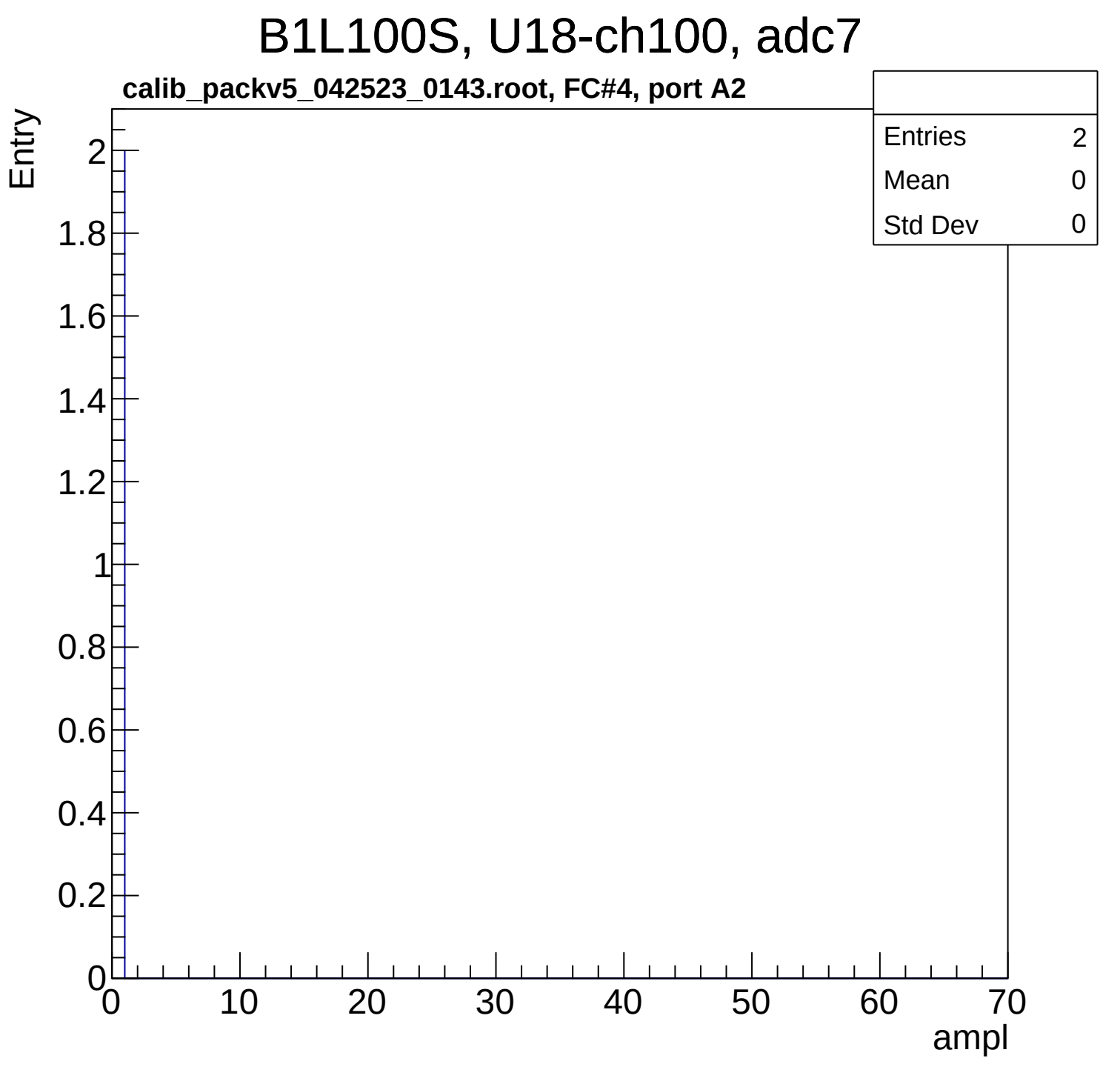

B1L100S, U18-ch100, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 40.62
Std Dev 3.751
Gaus mean : 40.8810
Gaus Width: 3.7453
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

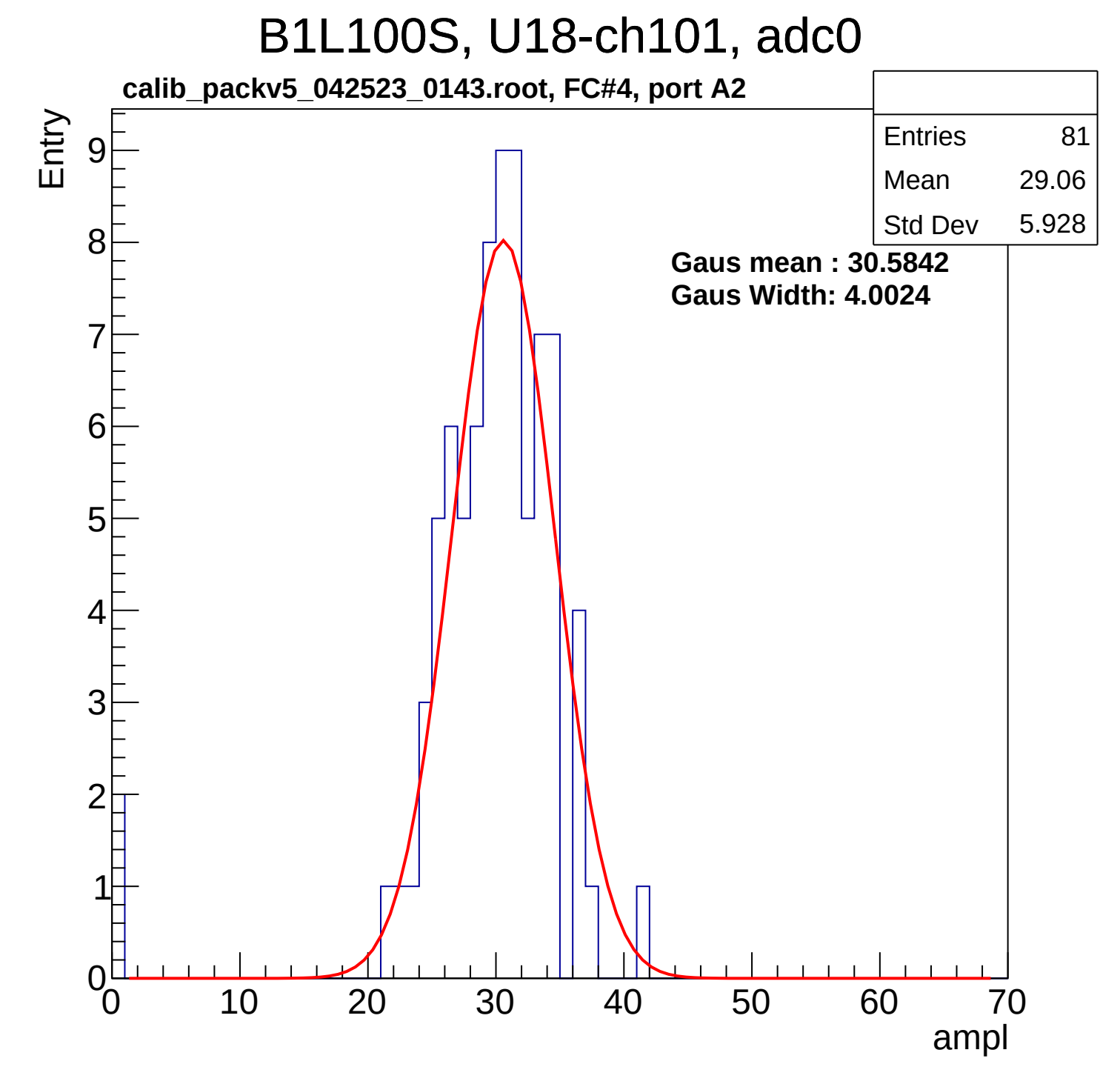

B1L100S, U18-ch100, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 48.07
Std Dev 3.489
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

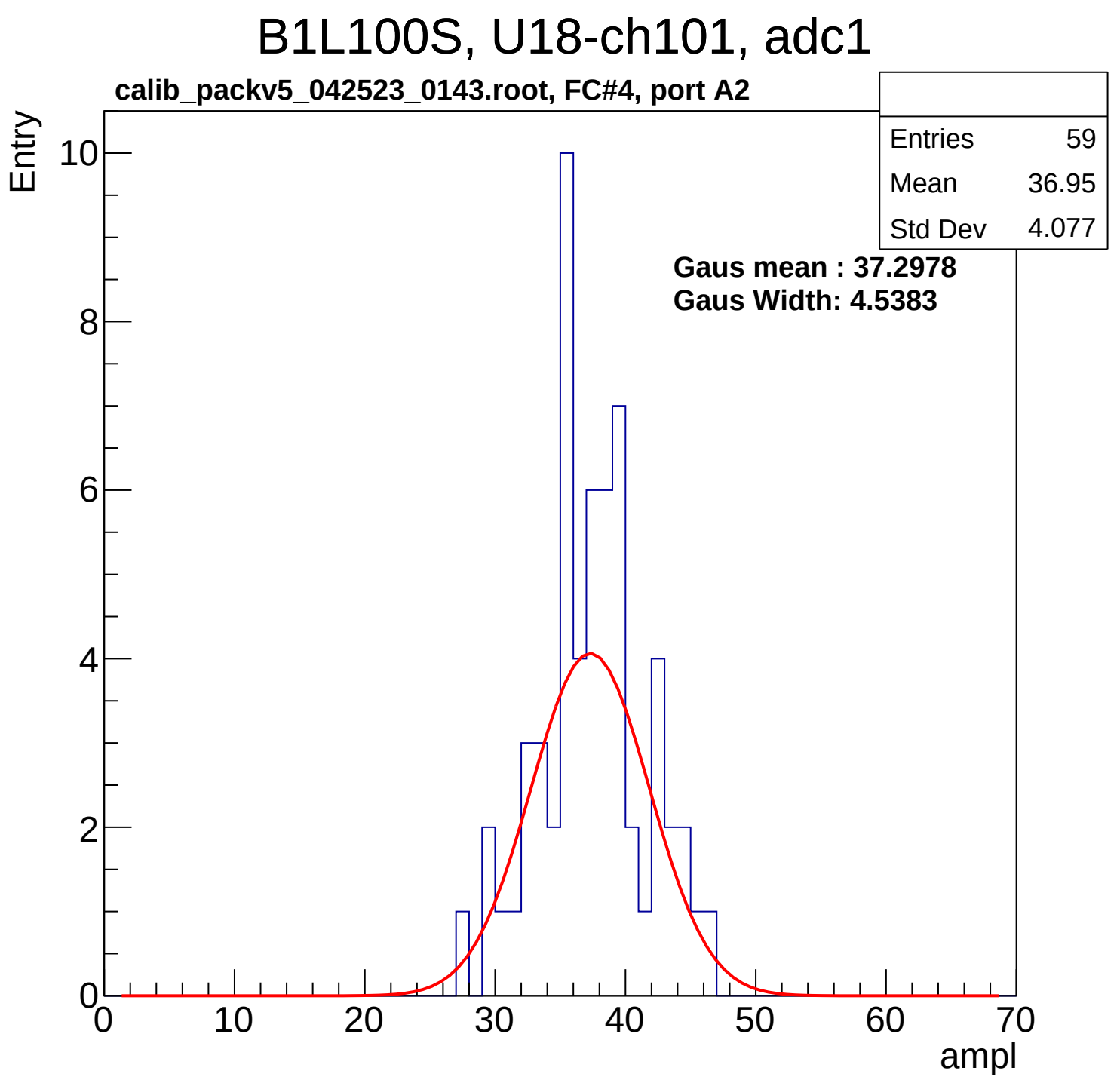

B1L100S, U18-ch100, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 54.65
Std Dev 2.961
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

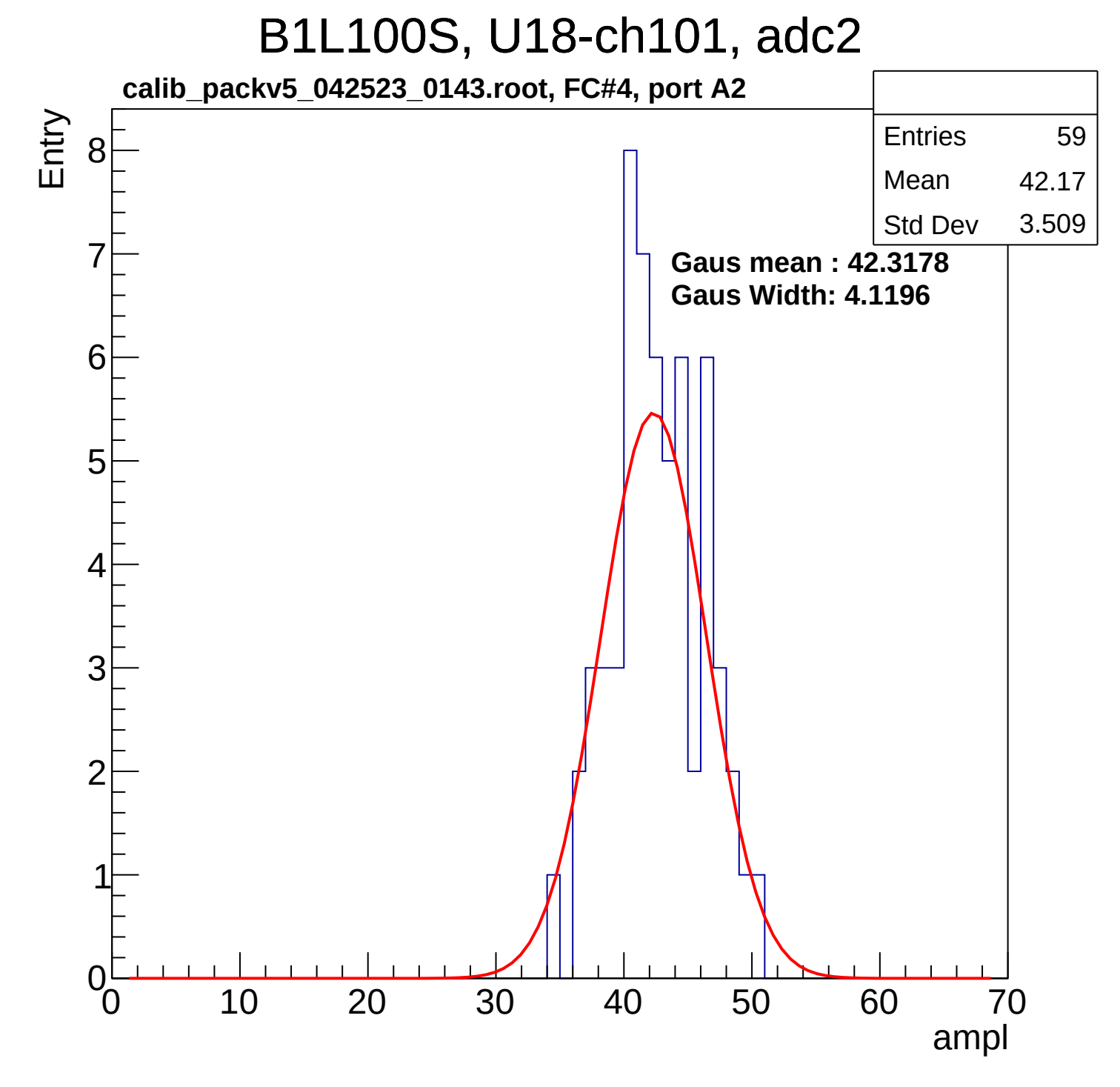

B1L100S, U18-ch100, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 59.24
Std Dev 2.567
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

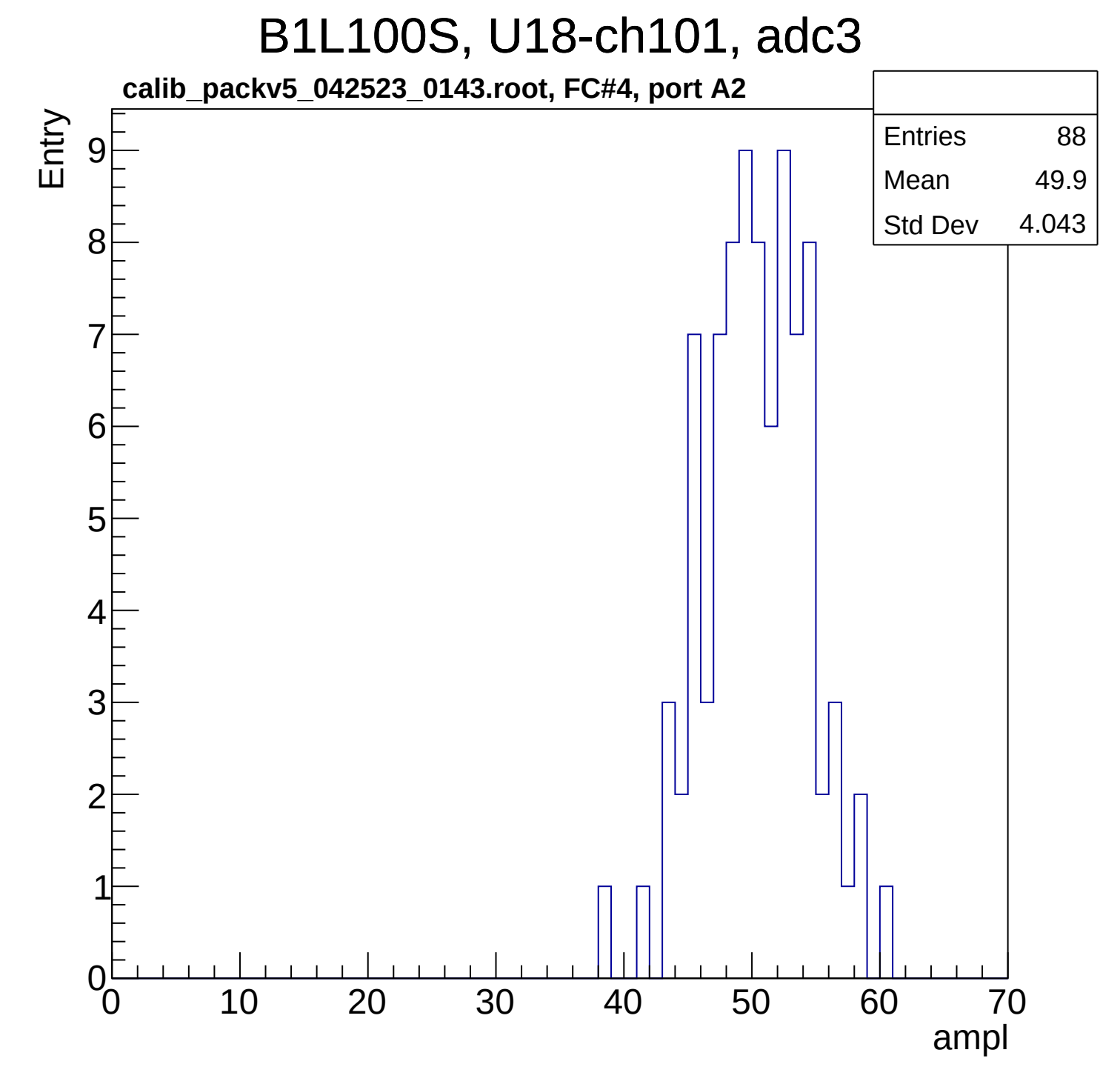

B1L100S, U18-ch100, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 56.36
Std Dev 17.87
Entry
ampl
0
1
2
3
4
5
0
10
20
30
40
50
60
70

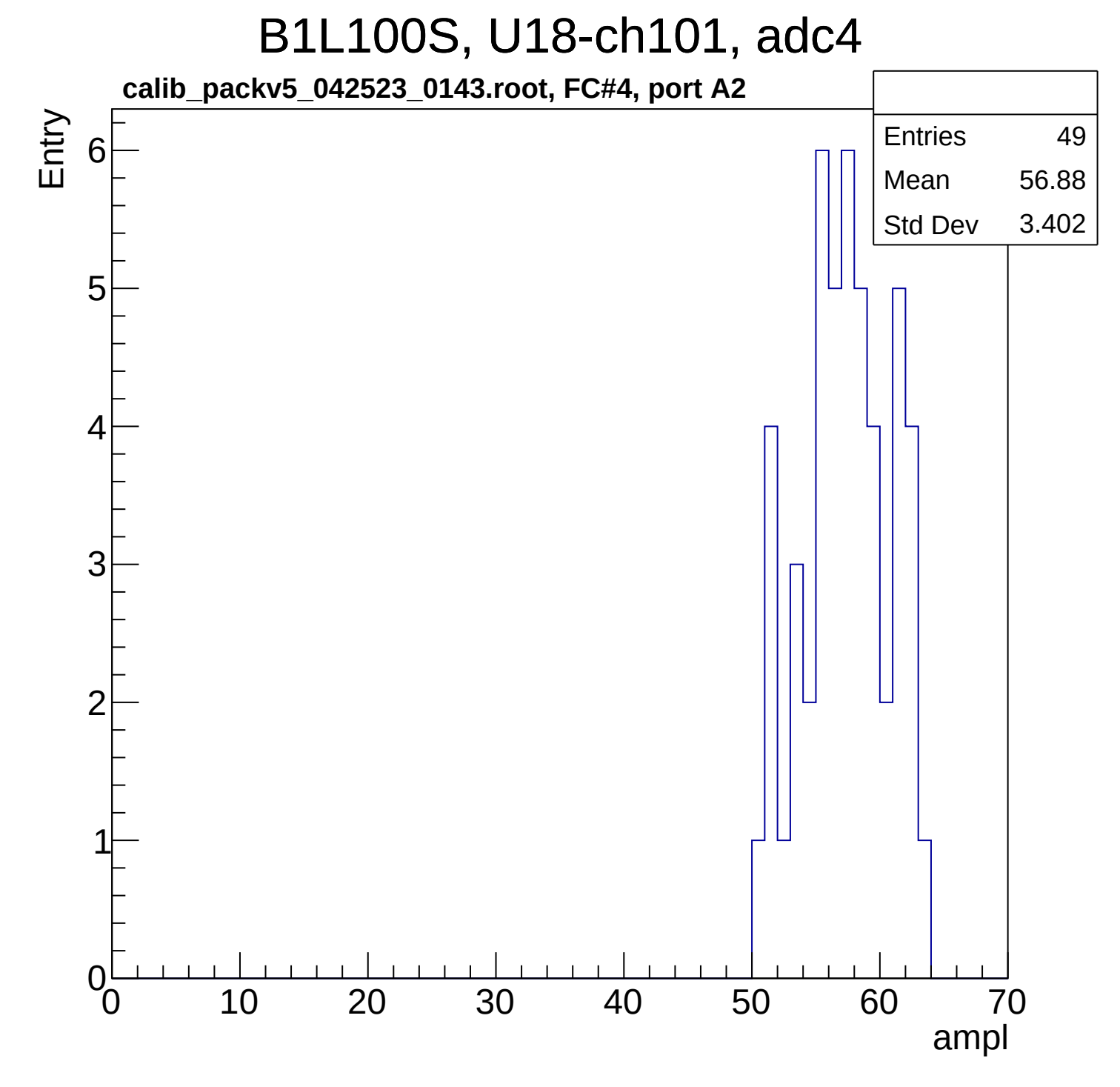

B1L100S, U18-ch100, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

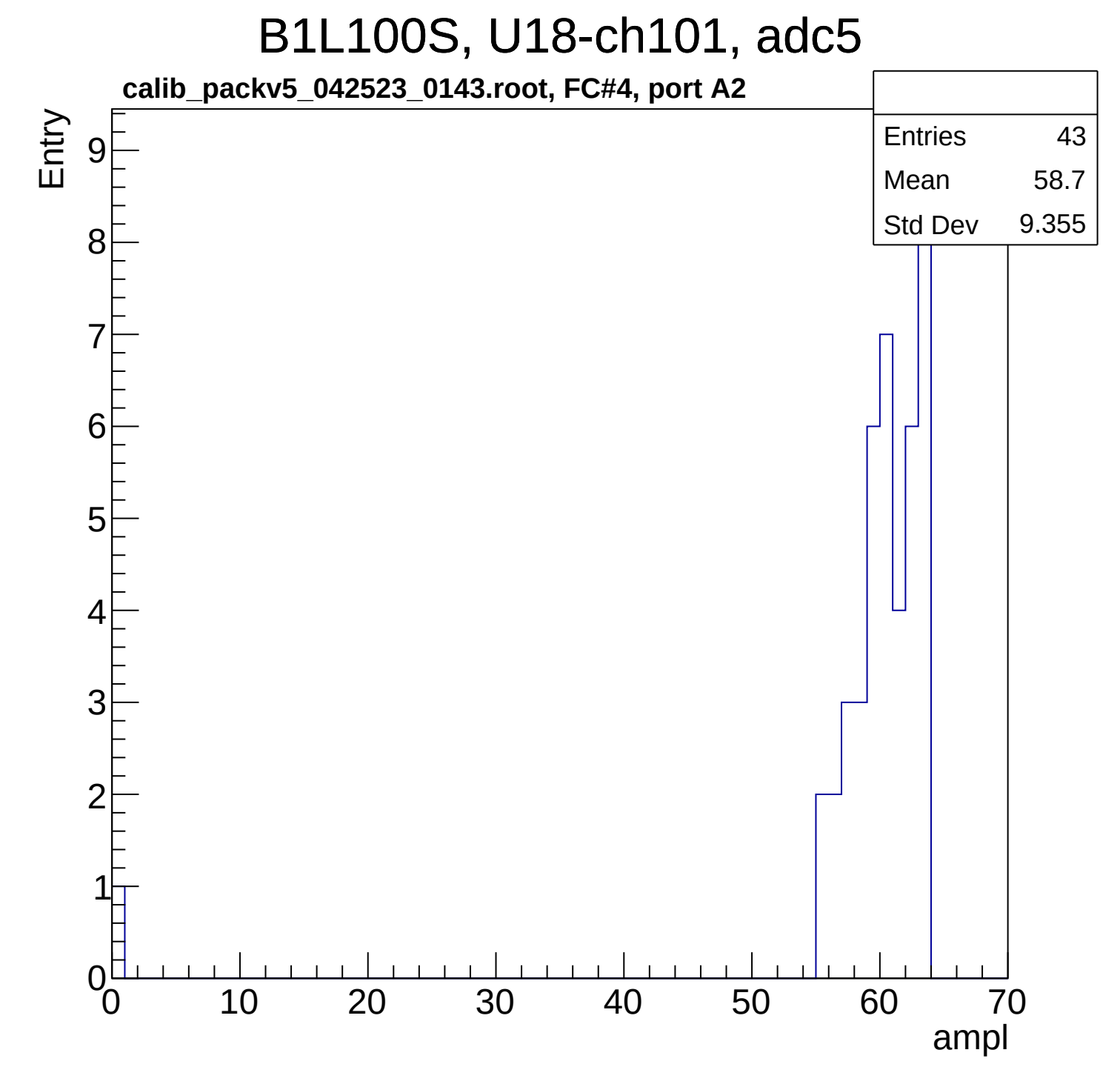

B1L100S, U18-ch101, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 29.06
Std Dev 5.928
Gaus mean : 30.5842
Gaus Width: 4.0024
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

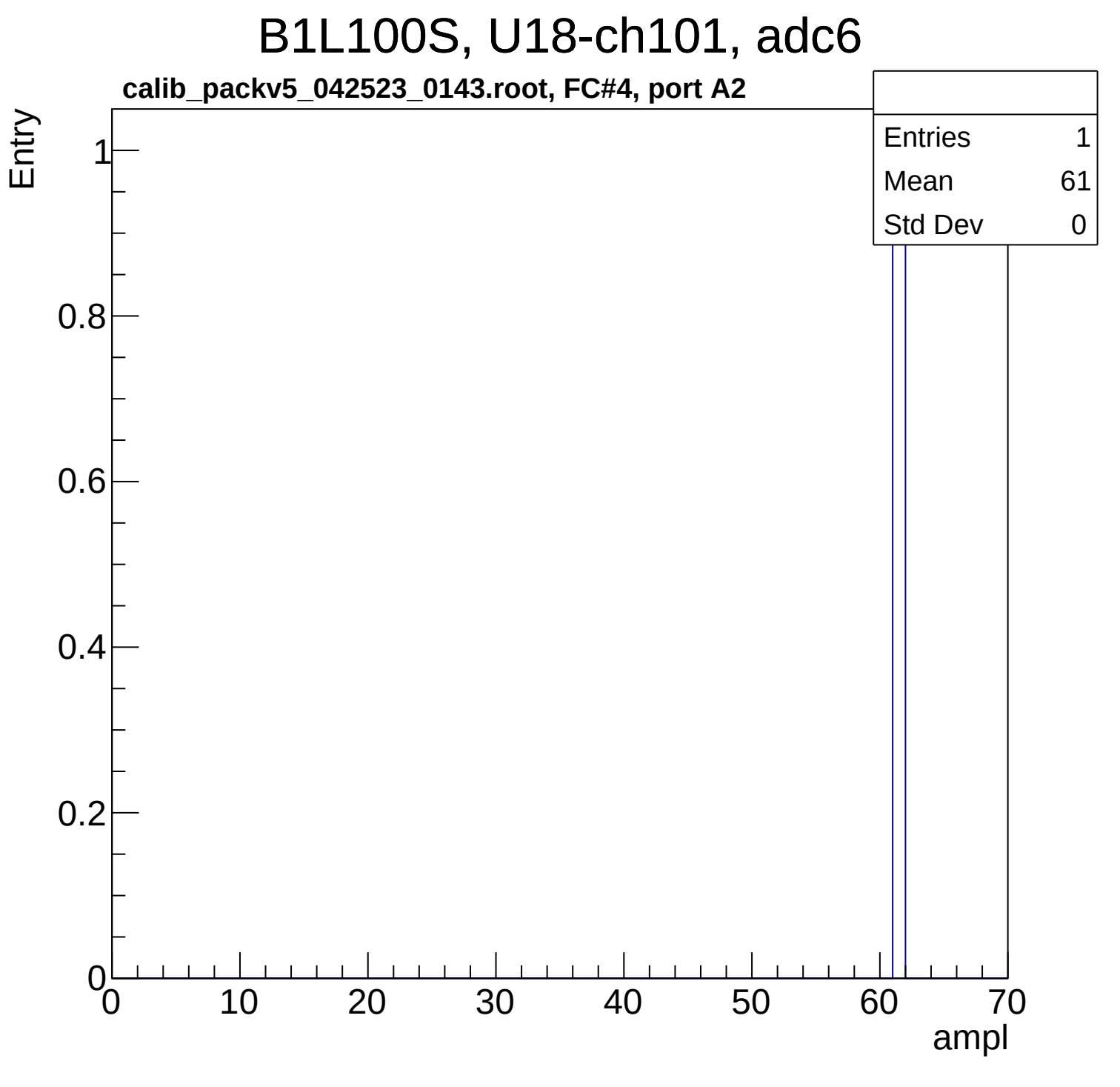

B1L100S, U18-ch101, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 36.95
Std Dev 4.077
Gaus mean : 37.2978
Gaus Width: 4.5383
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

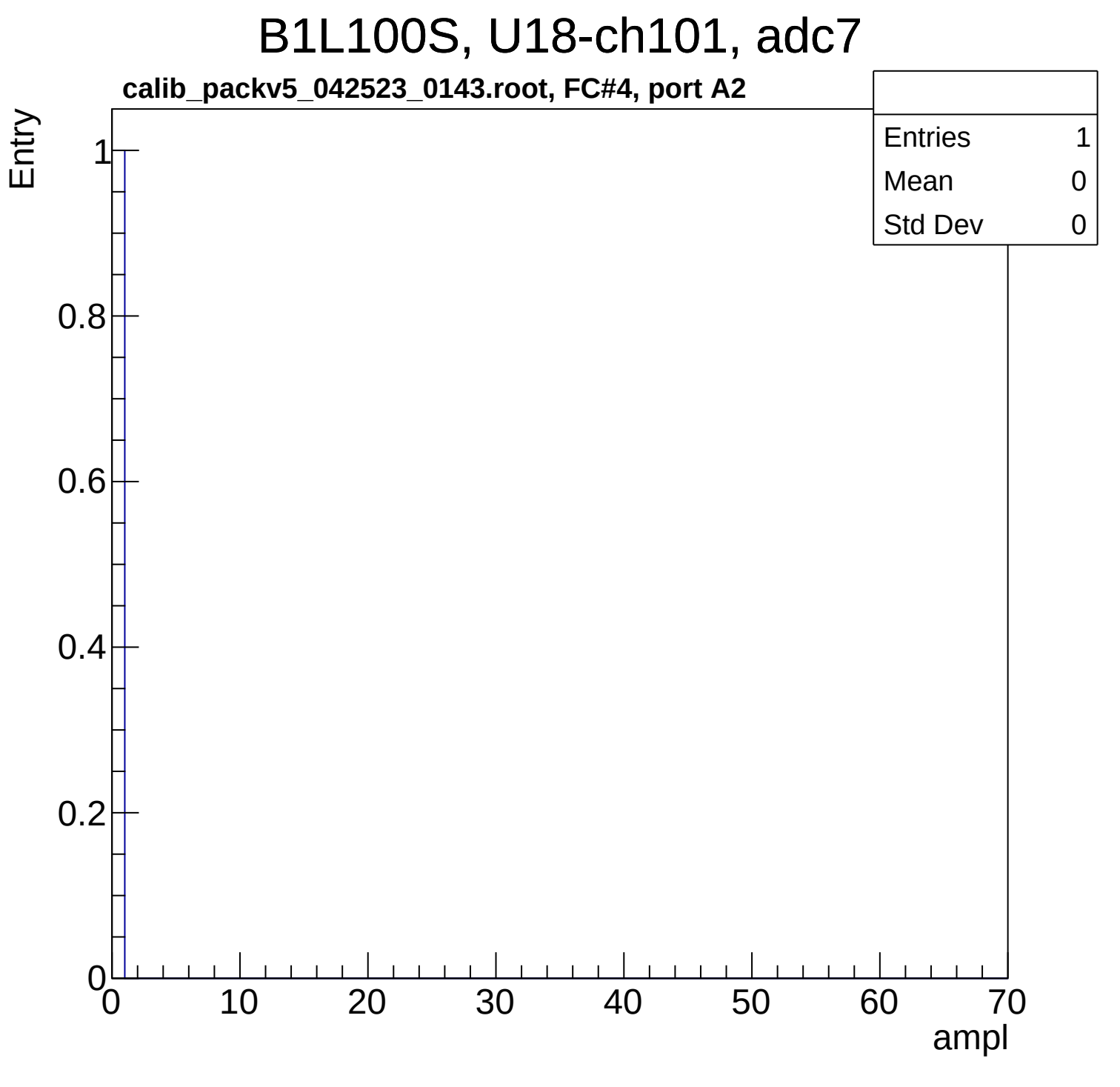

B1L100S, U18-ch101, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 42.17
Std Dev 3.509
Gaus mean : 42.3178
Gaus Width: 4.1196
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

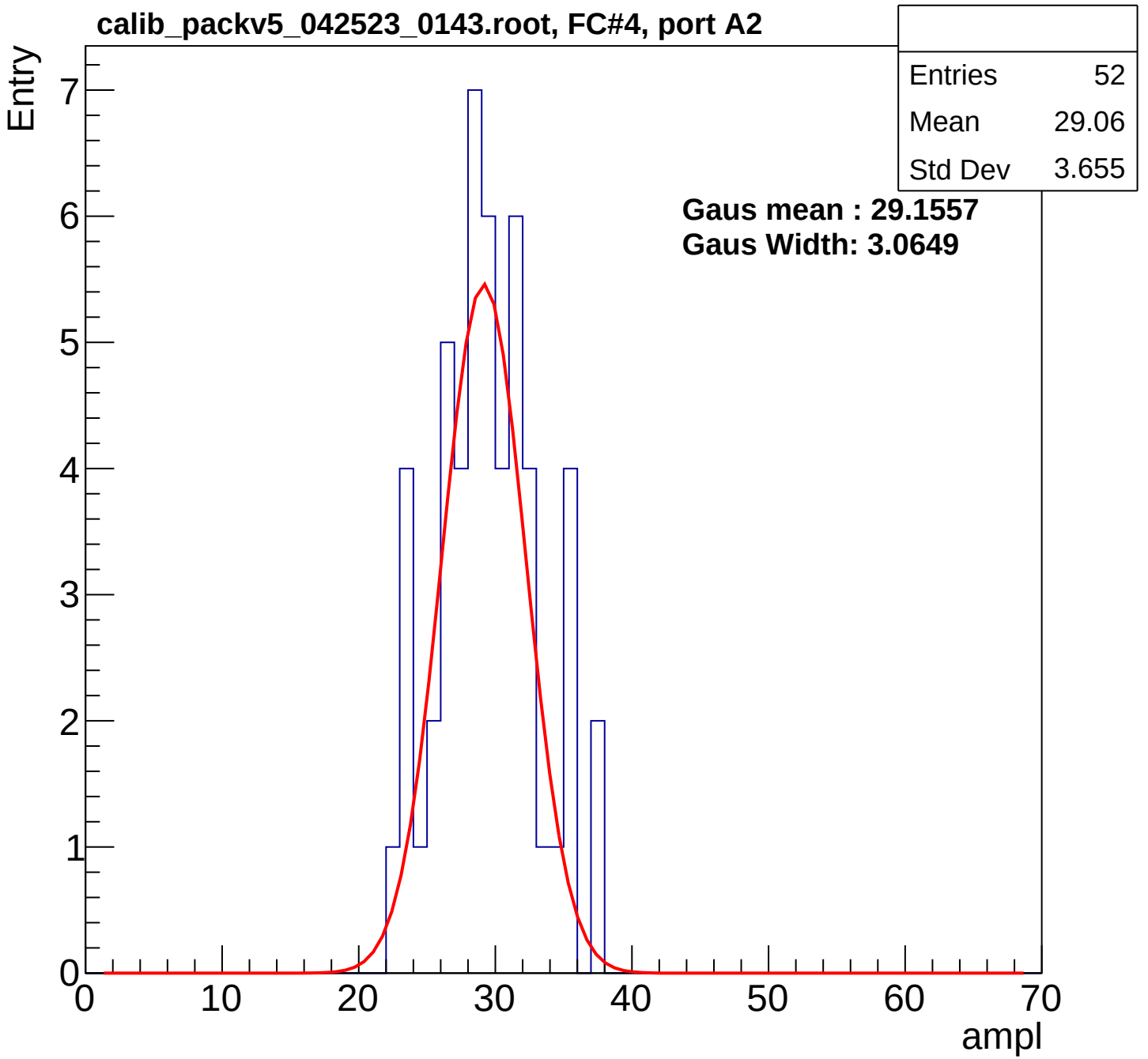

B1L100S, U18-ch101, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 88
Mean 49.9
Std Dev 4.043
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

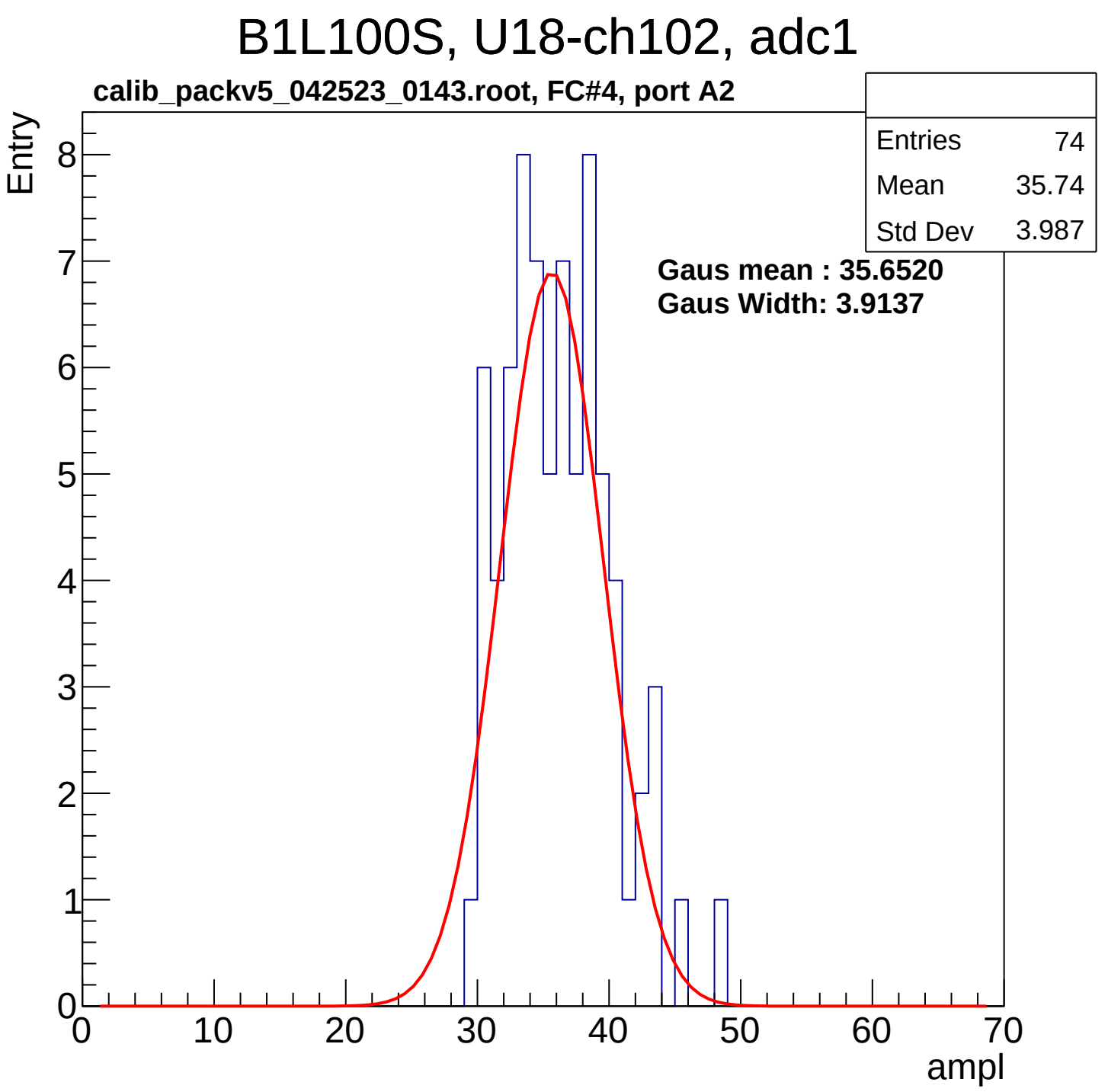

B1L100S, U18-ch101, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 56.88
Std Dev 3.402
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

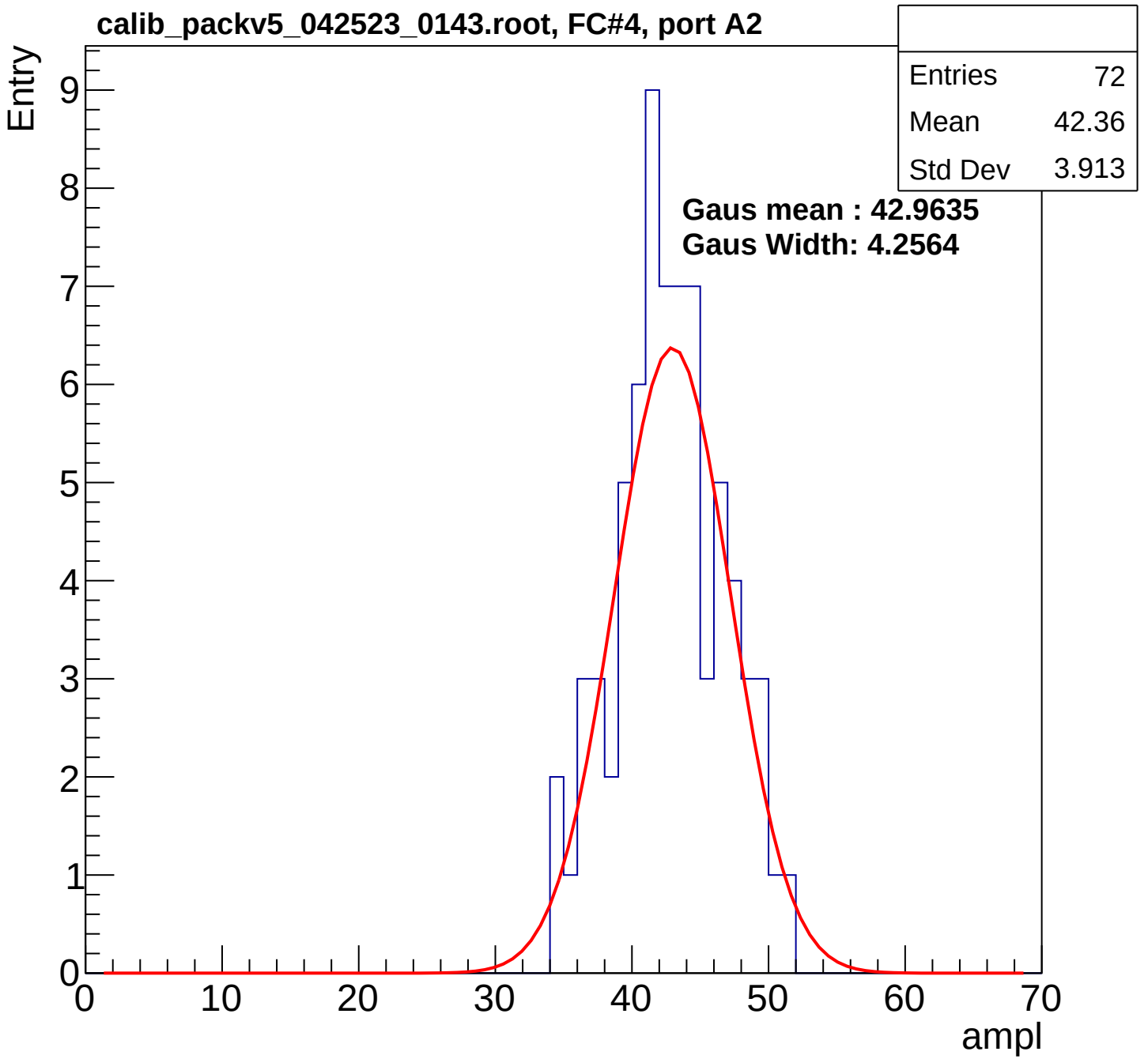

B1L100S, U18-ch101, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 58.7
Std Dev 9.355
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

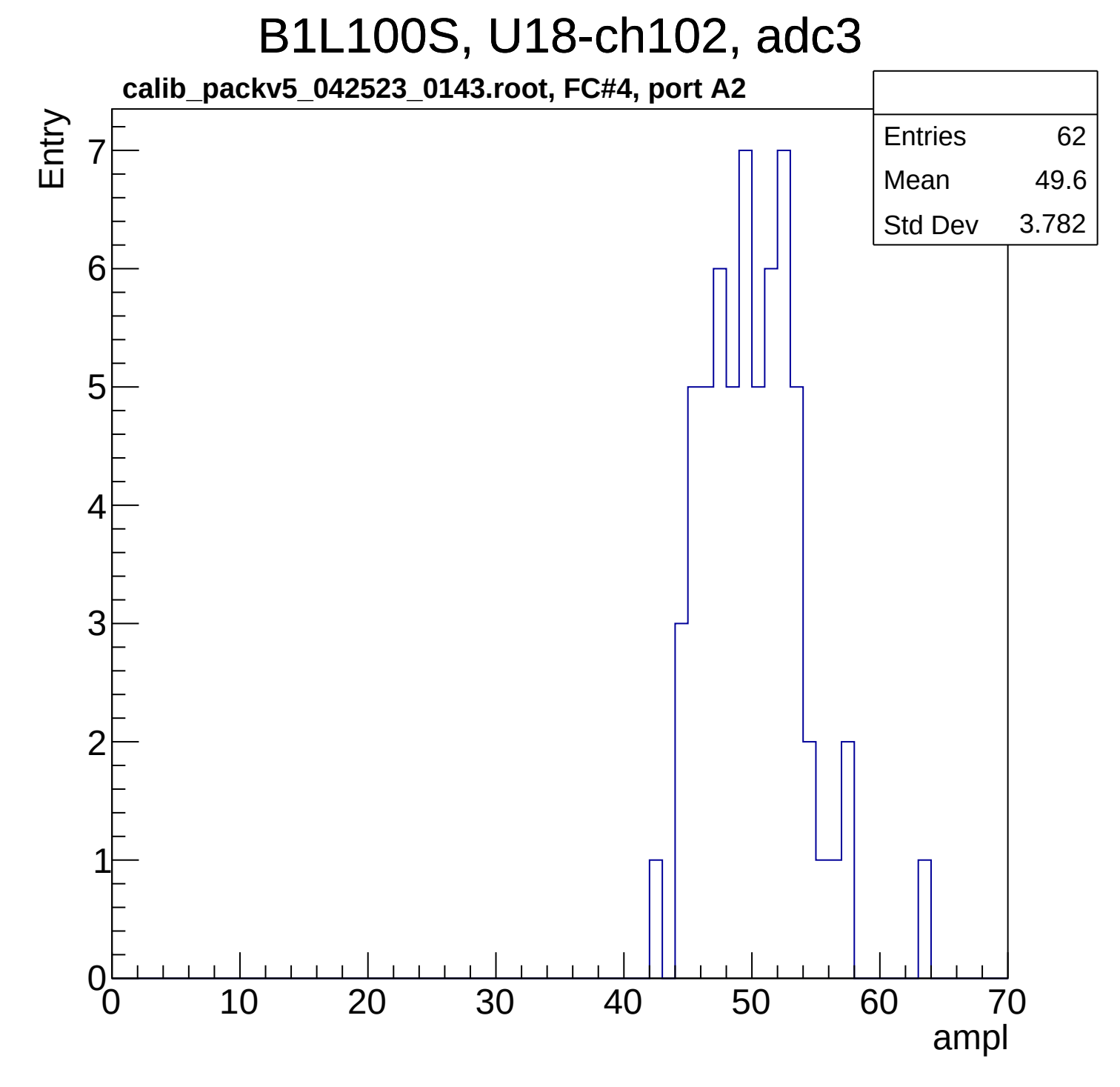

B1L100S, U18-ch101, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 61
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

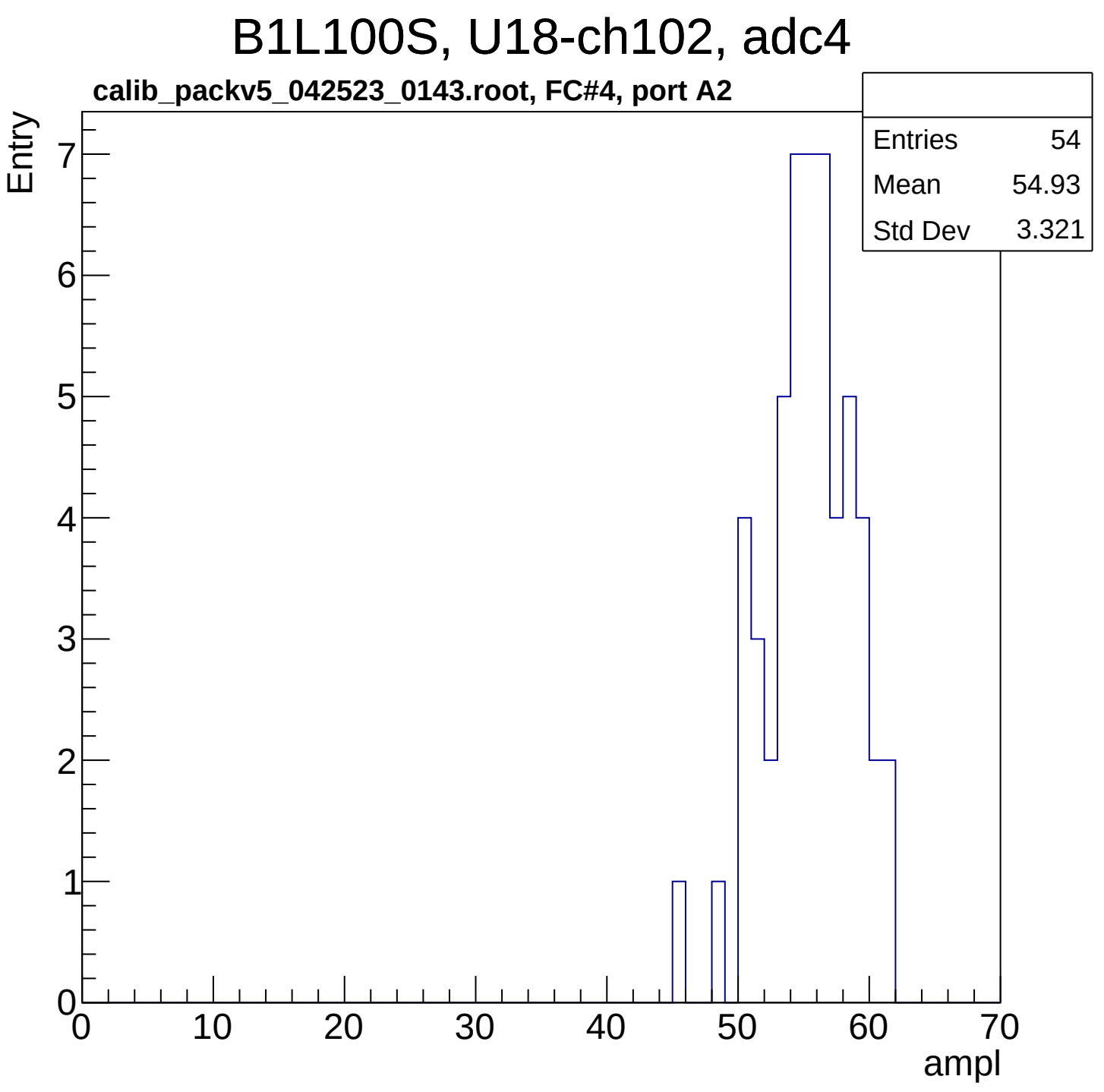

B1L100S, U18-ch101, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

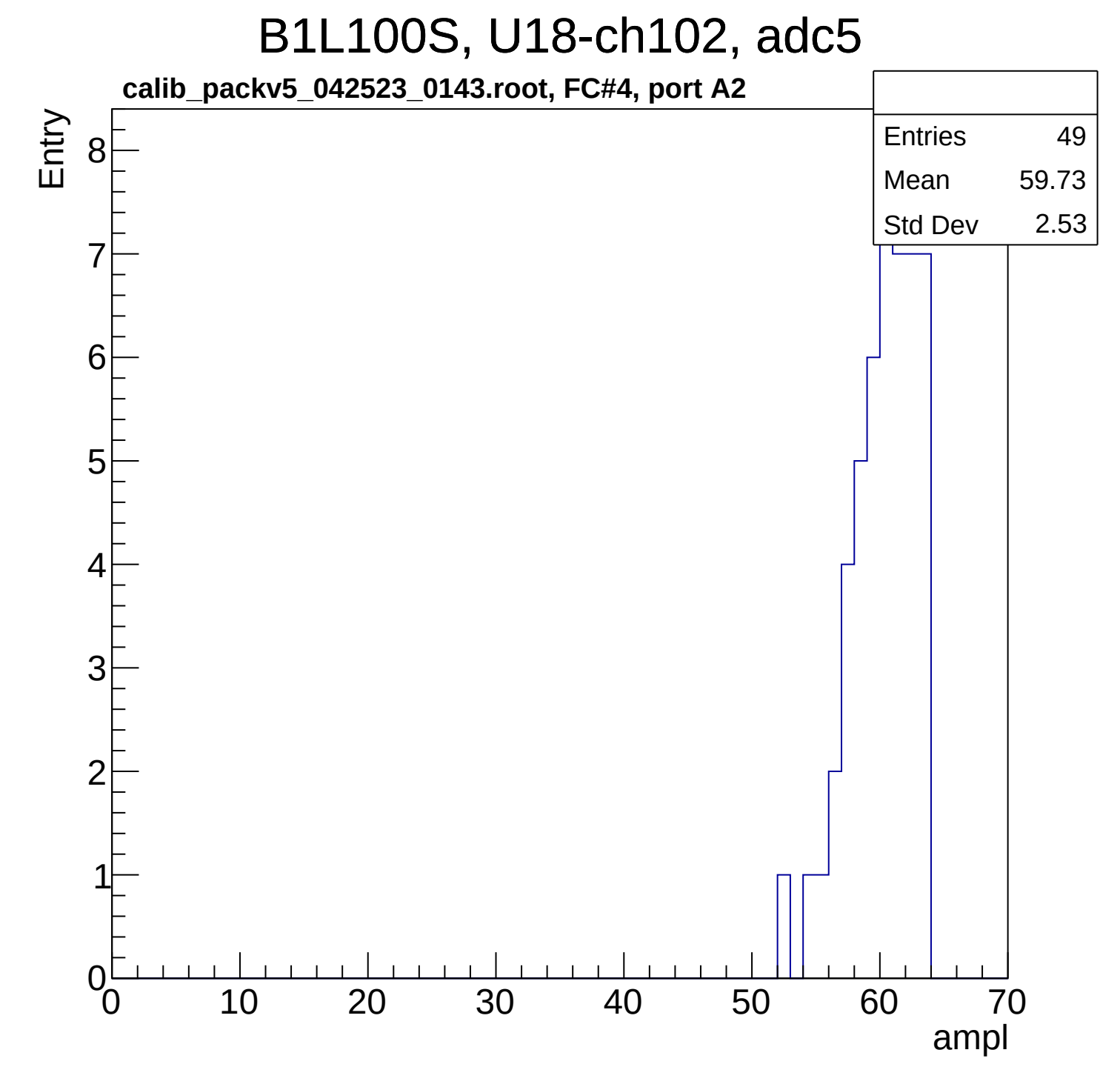

B1L100S, U18-ch102, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 29.06
Std Dev 3.655
Gaus mean : 29.1557
Gaus Width: 3.0649
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

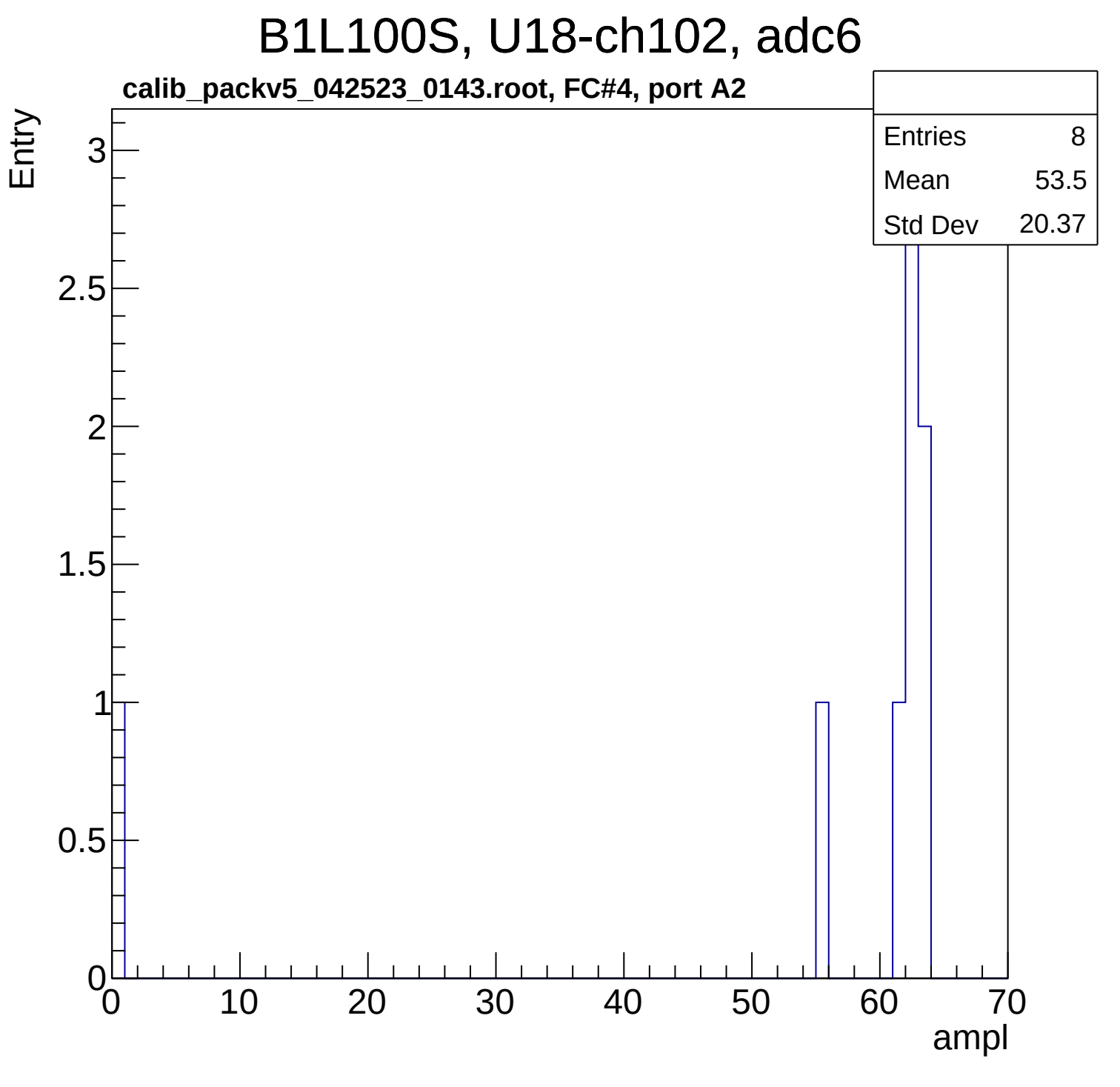

B1L100S, U18-ch102, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 35.74
Std Dev 3.987
Gaus mean : 35.6520
Gaus Width: 3.9137
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

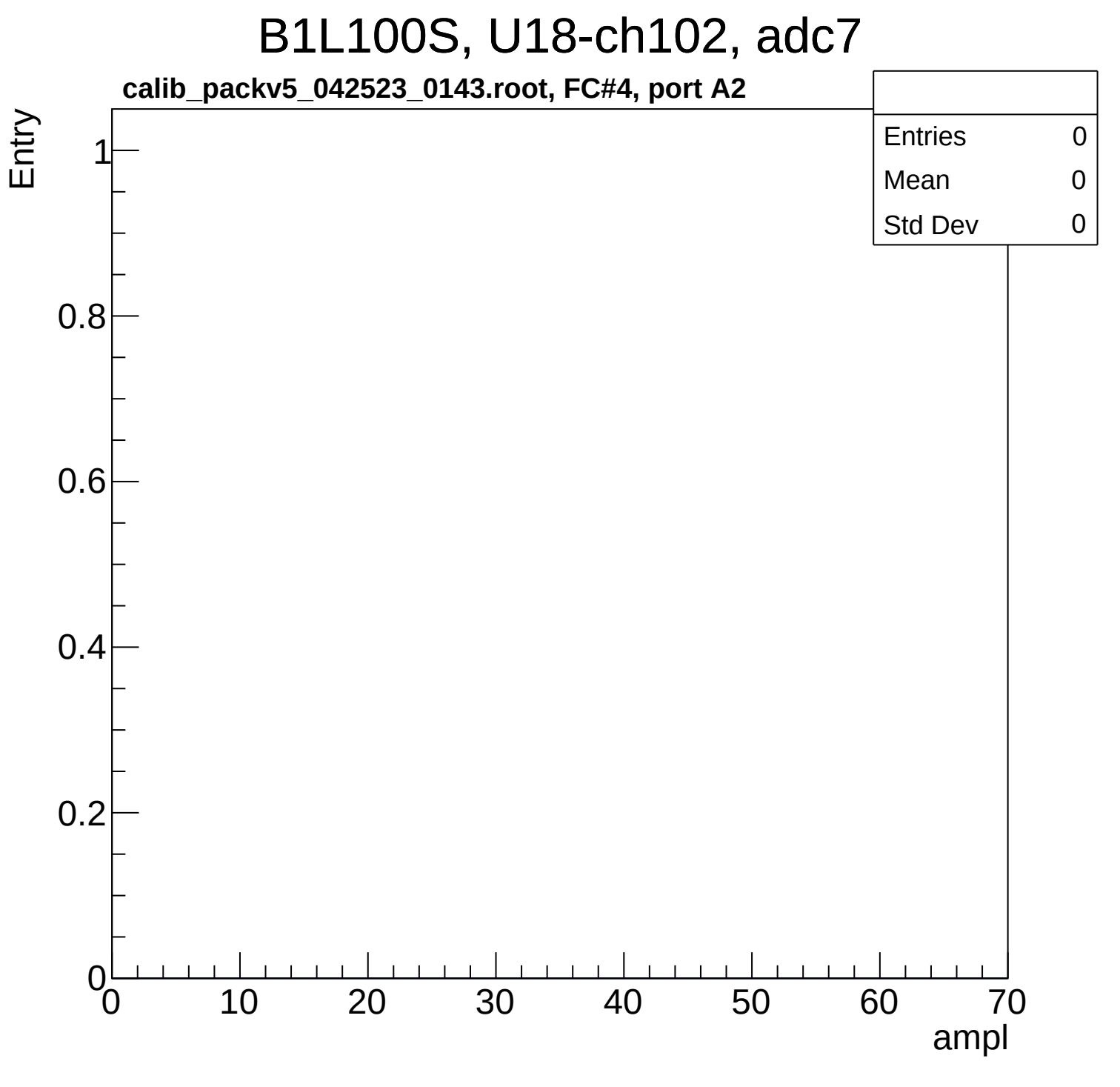

B1L100S, U18-ch102, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 42.36
Std Dev 3.913
Gaus mean : 42.9635
Gaus Width: 4.2564
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

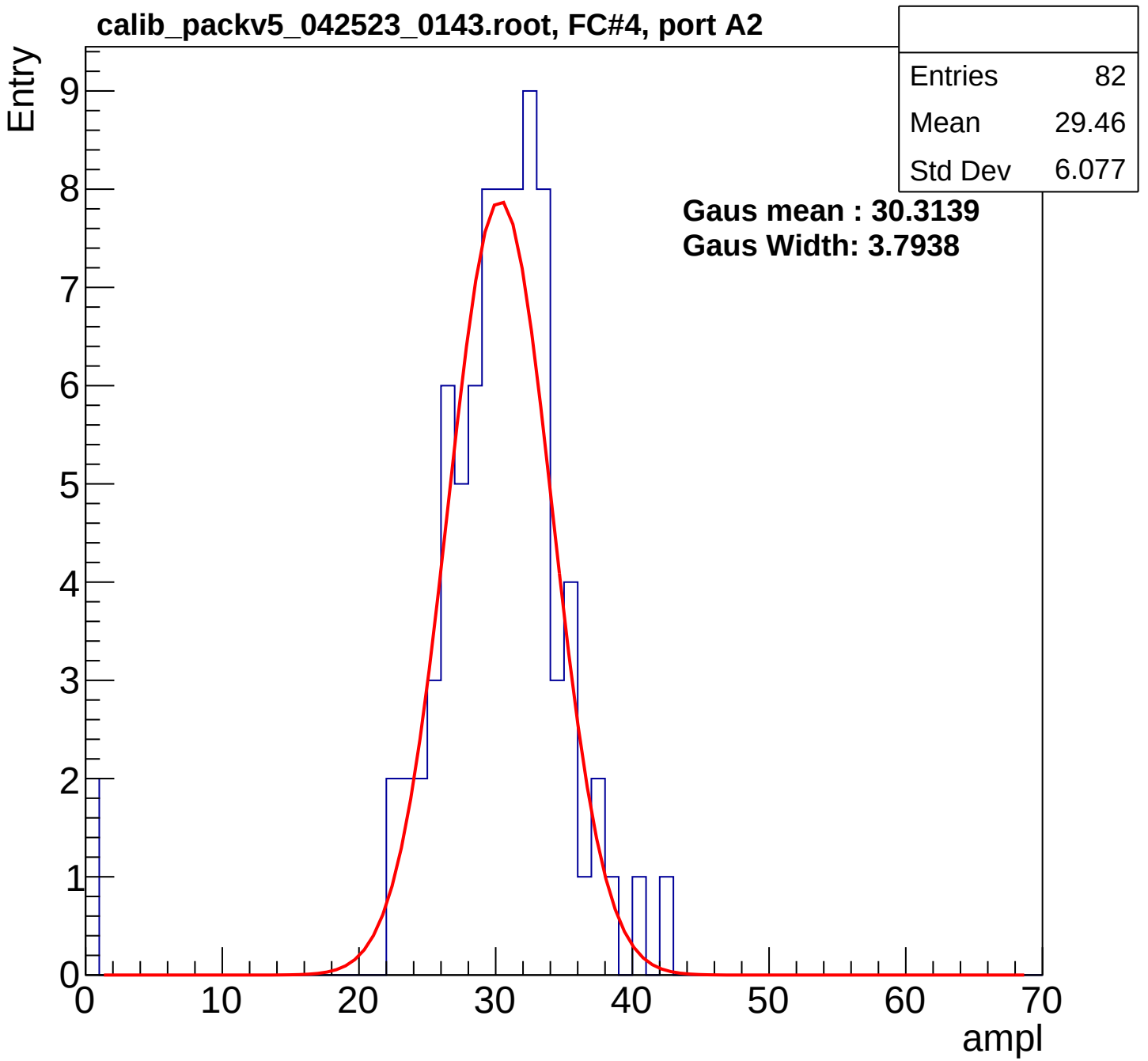

B1L100S, U18-ch102, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 49.6
Std Dev 3.782
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

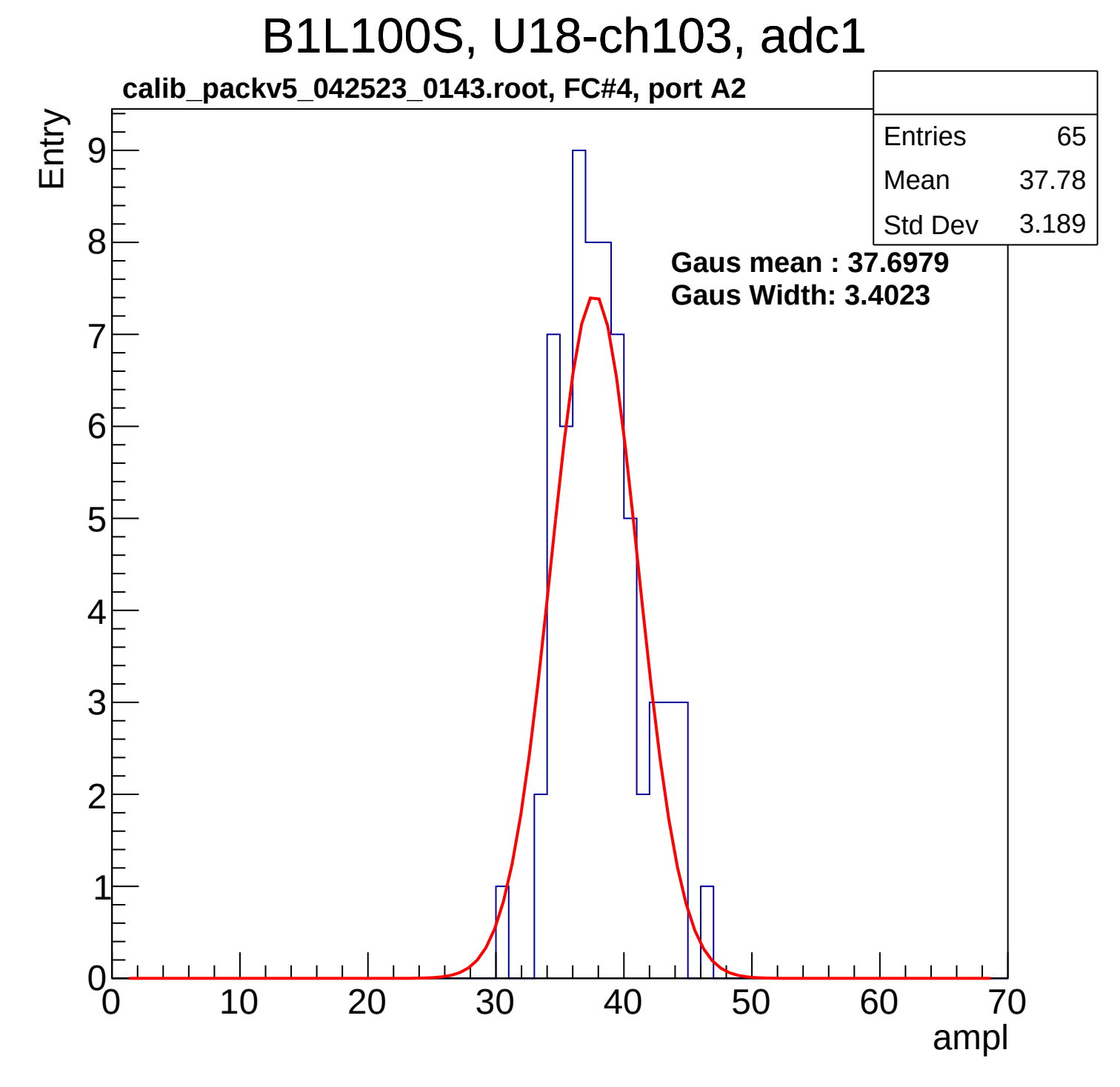

B1L100S, U18-ch102, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 54.93
Std Dev 3.321
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

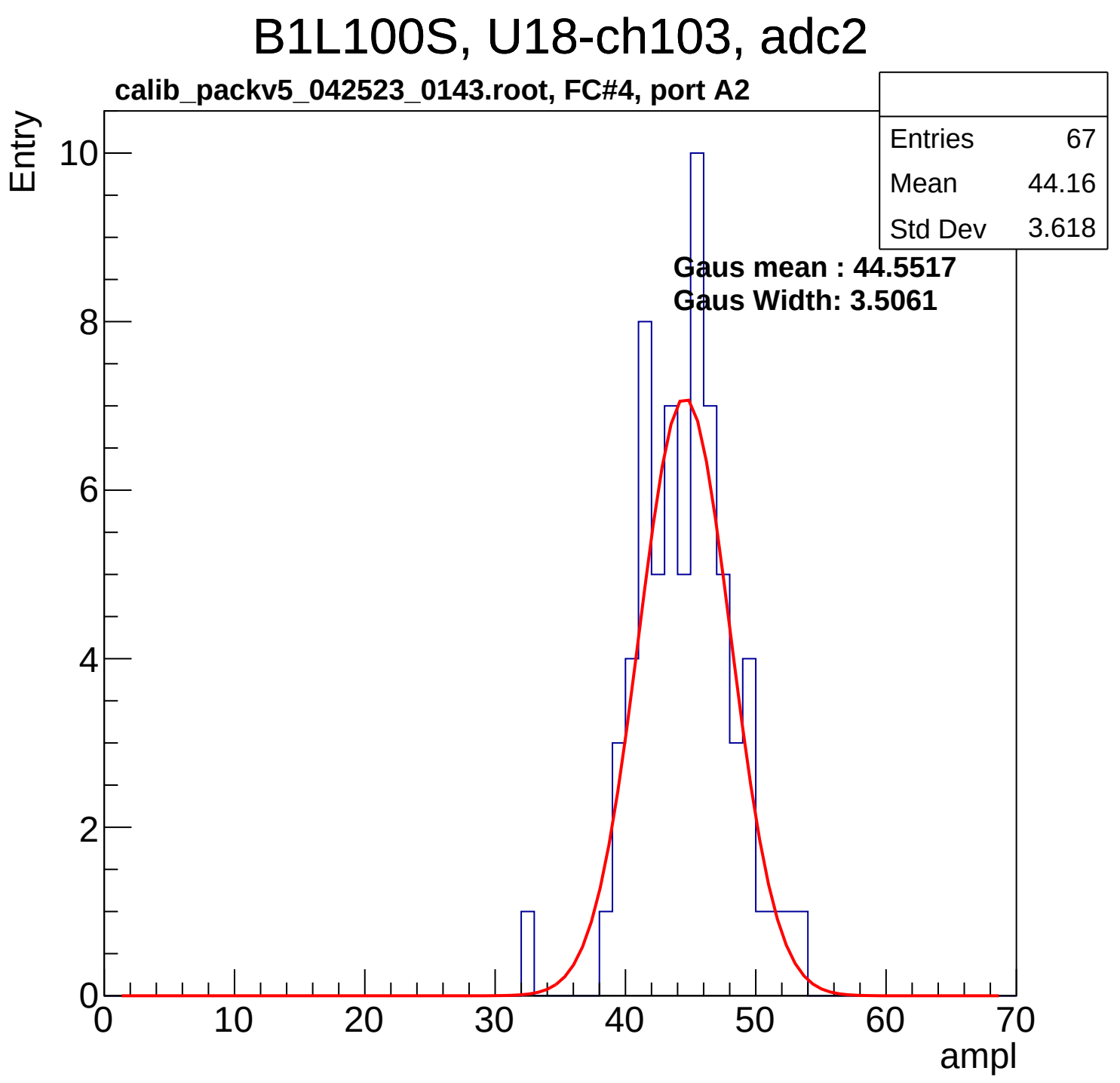

B1L100S, U18-ch102, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 59.73
Std Dev 2.53
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

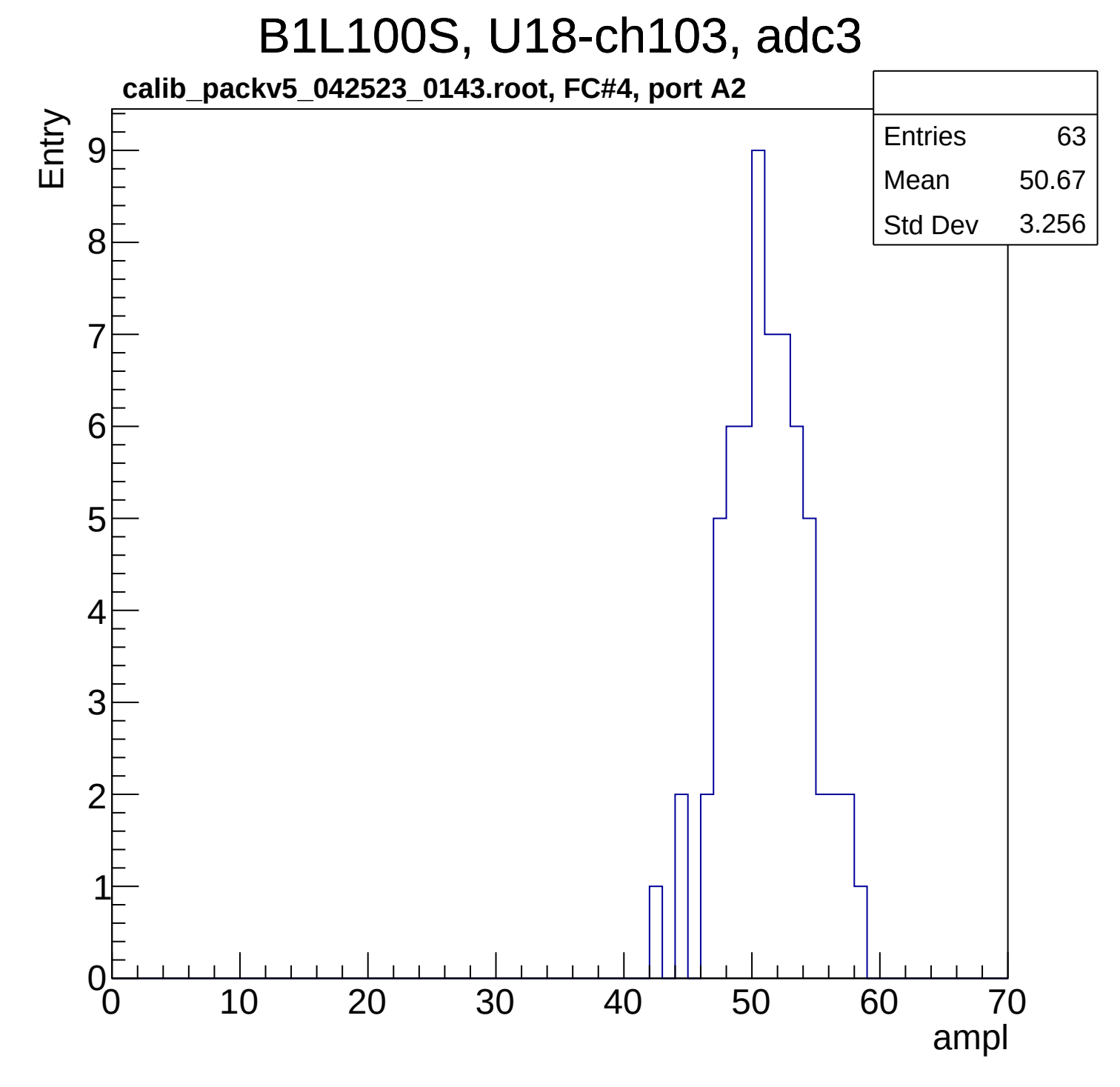

B1L100S, U18-ch102, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 8
Mean 53.5
Std Dev 20.37
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

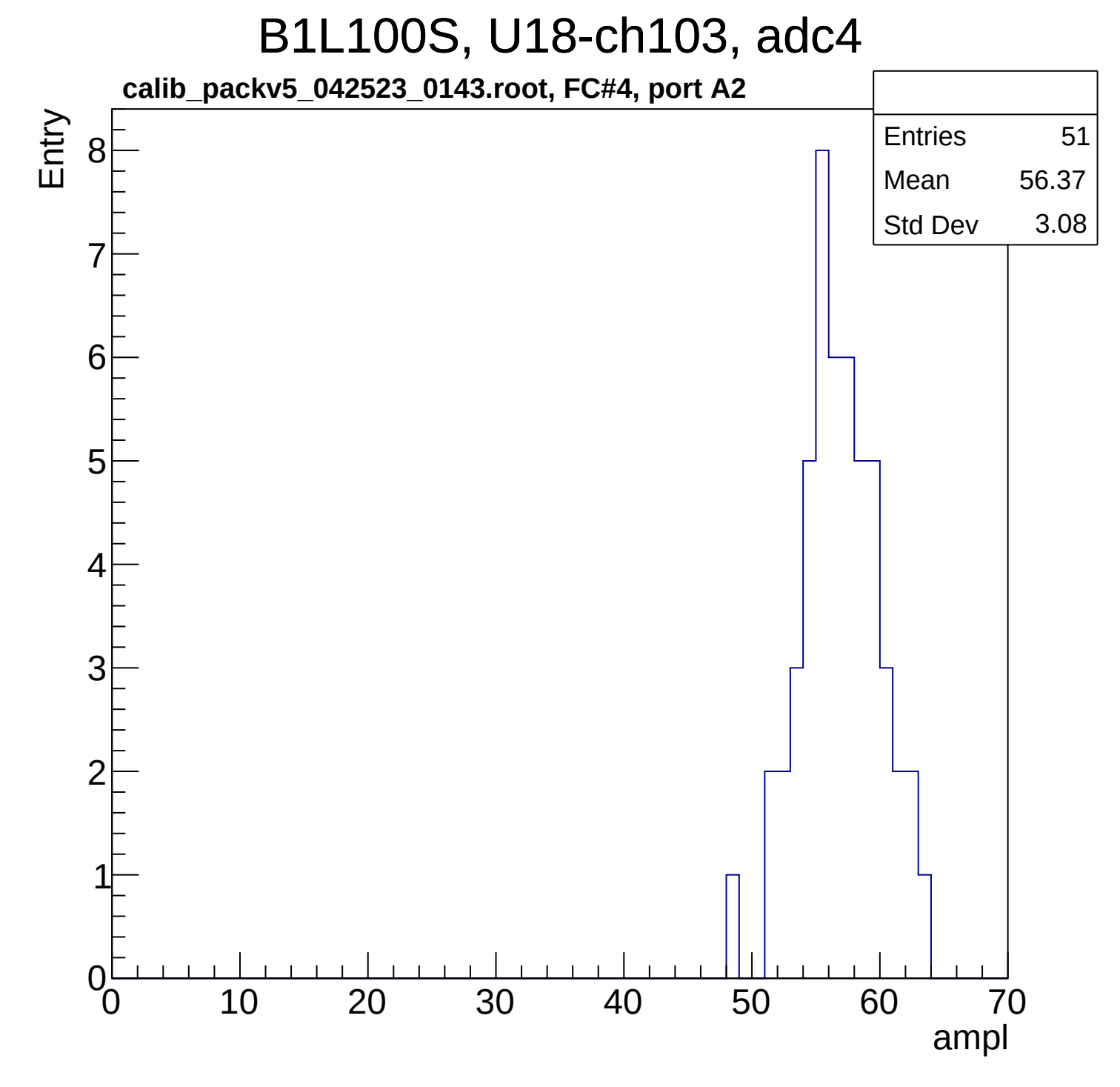

B1L100S, U18-ch102, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

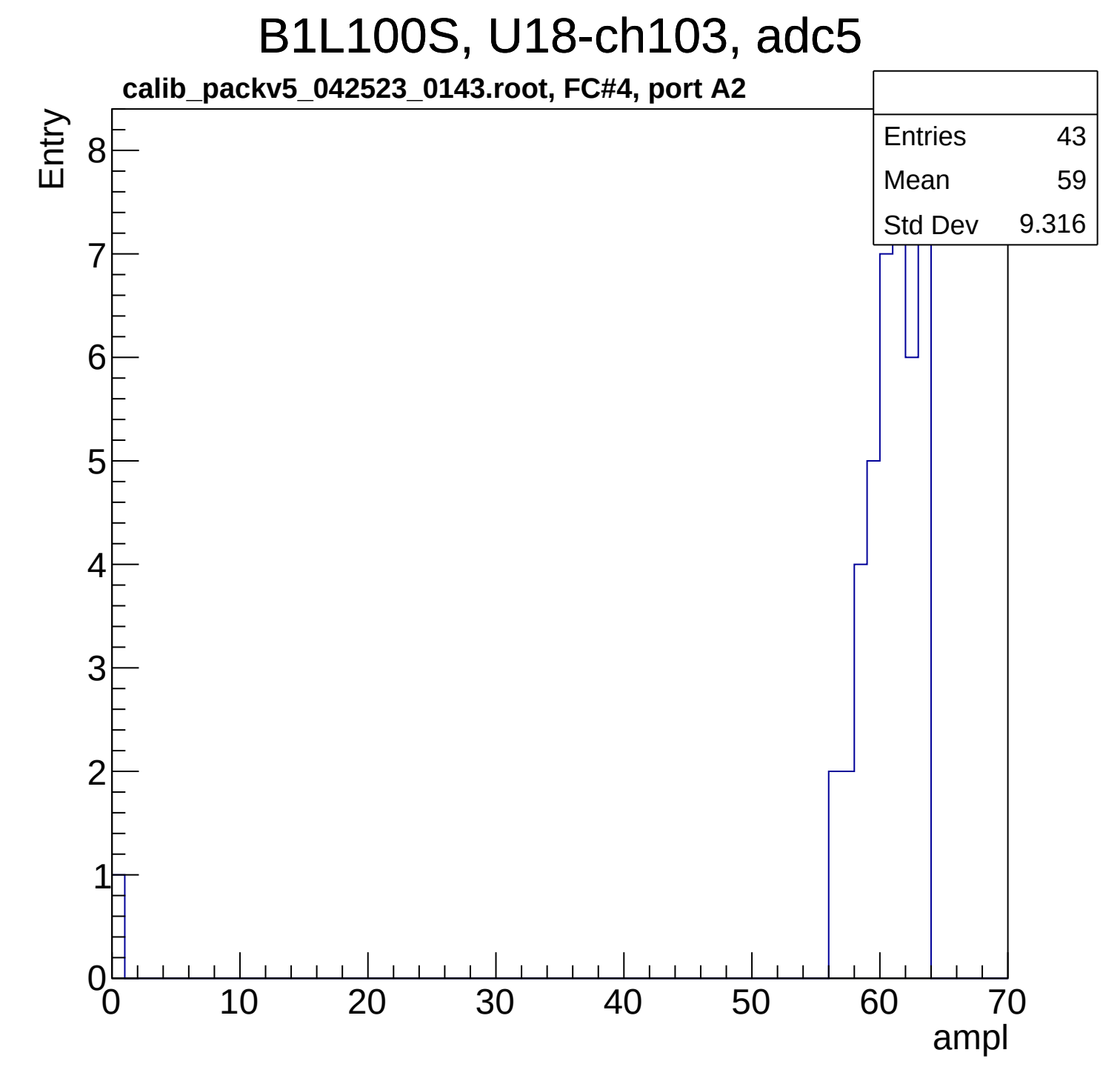

B1L100S, U18-ch103, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 29.46
Std Dev 6.077
Gaus mean : 30.3139
Gaus Width: 3.7938
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

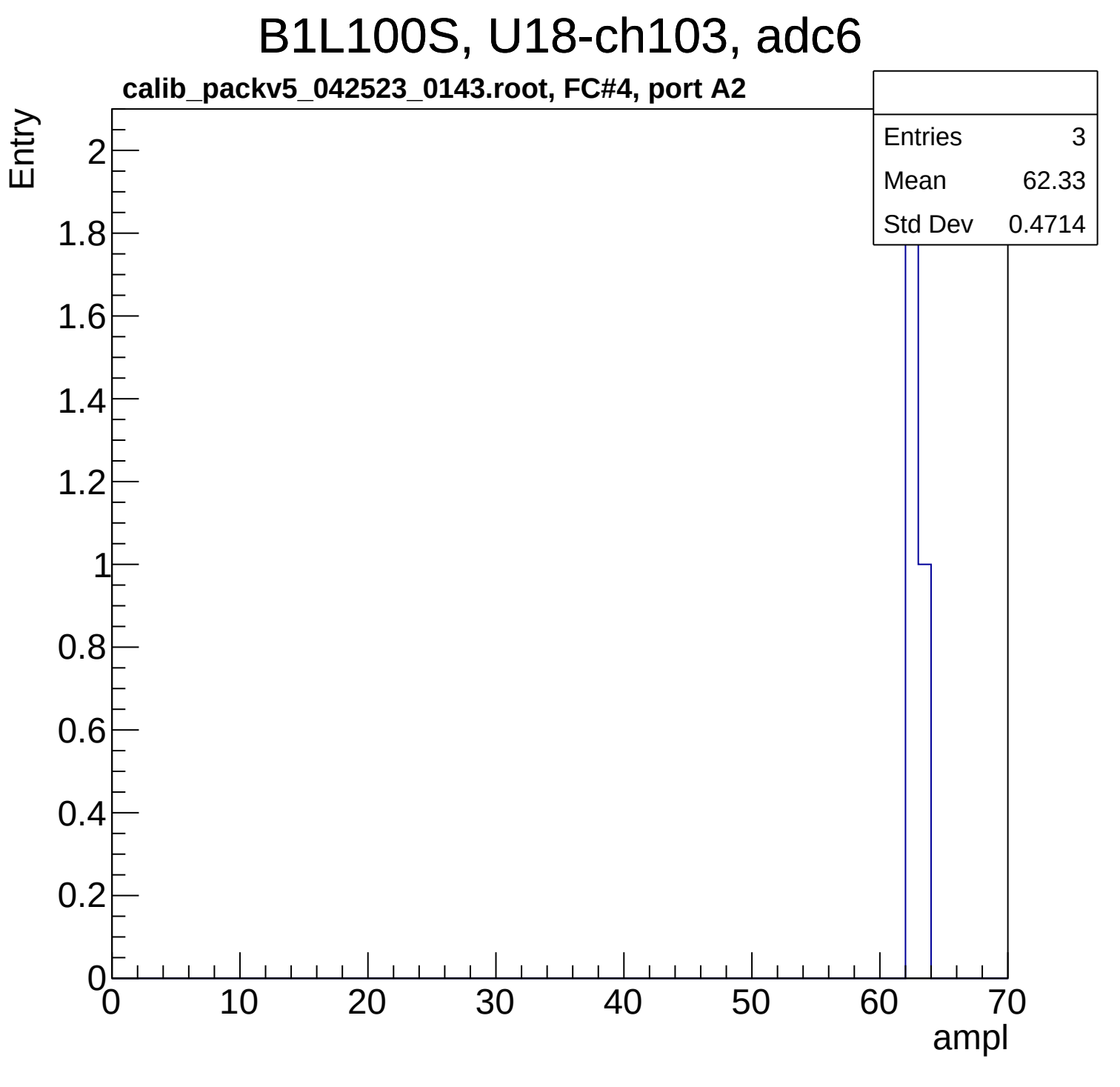

B1L100S, U18-ch103, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 37.78
Std Dev 3.189
Gaus mean : 37.6979
Gaus Width: 3.4023
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

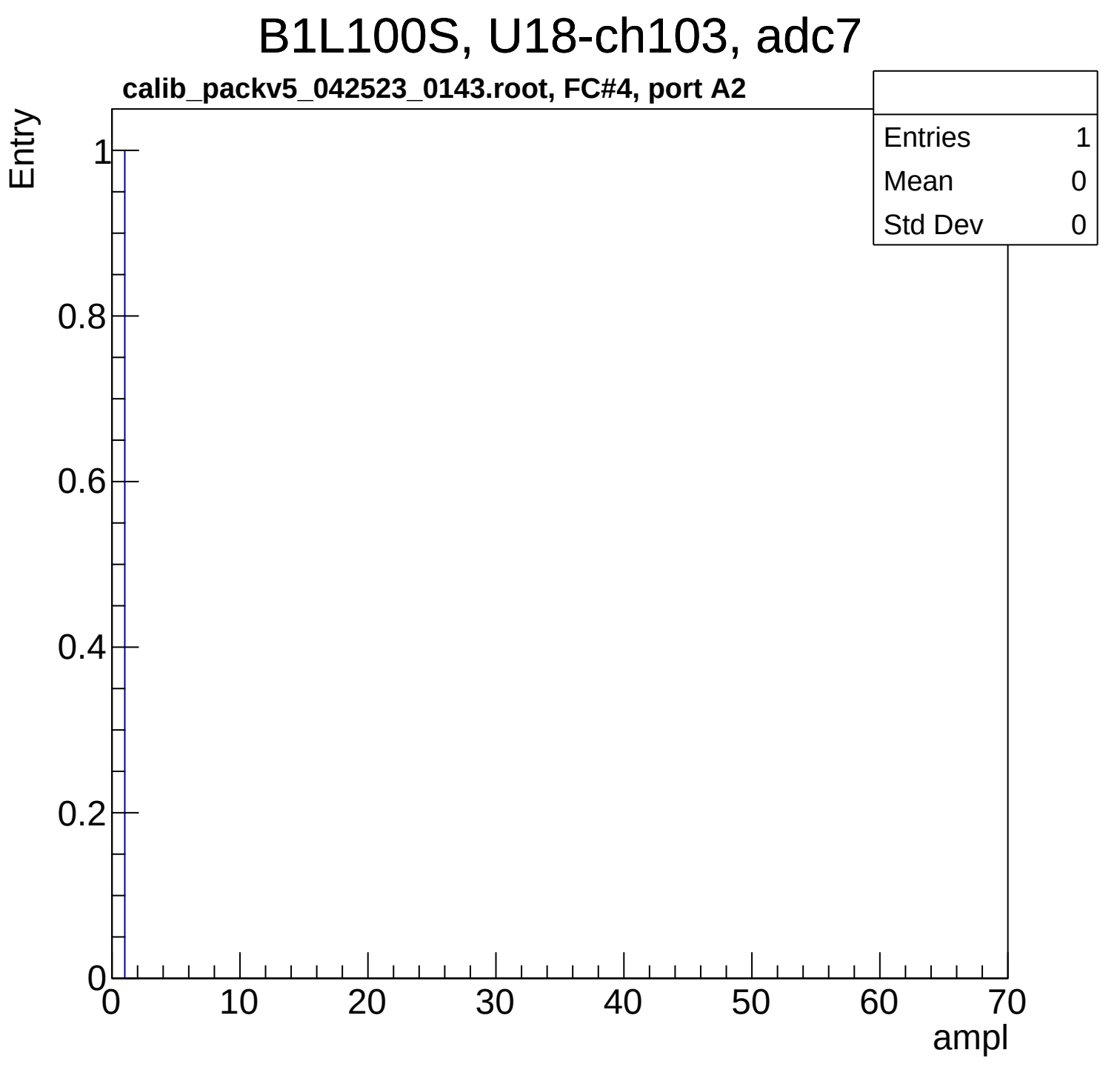

B1L100S, U18-ch103, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 44.16
Std Dev 3.618
Gaus mean : 44.5517
Gaus Width: 3.5061
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

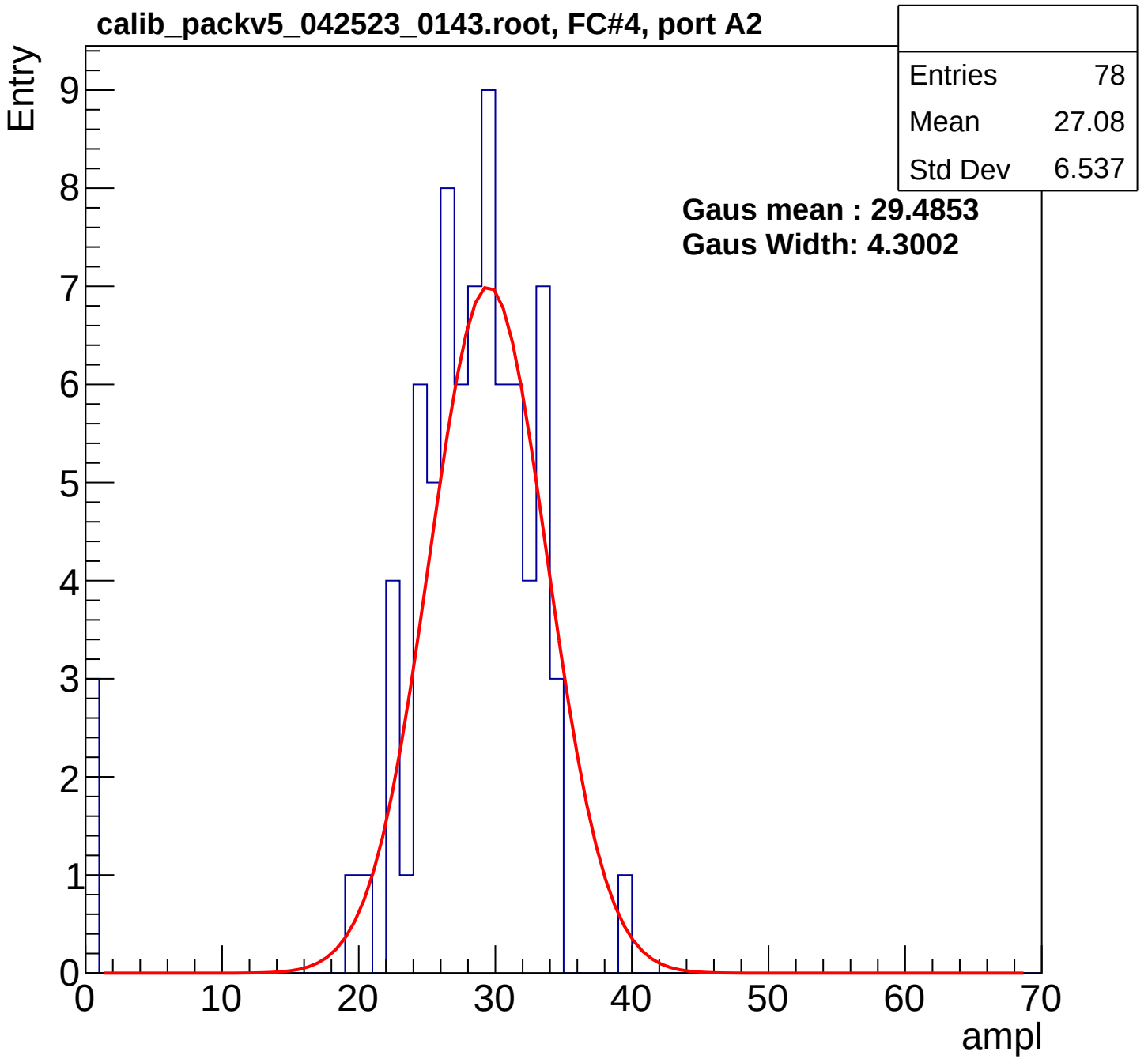

B1L100S, U18-ch103, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 50.67
Std Dev 3.256
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

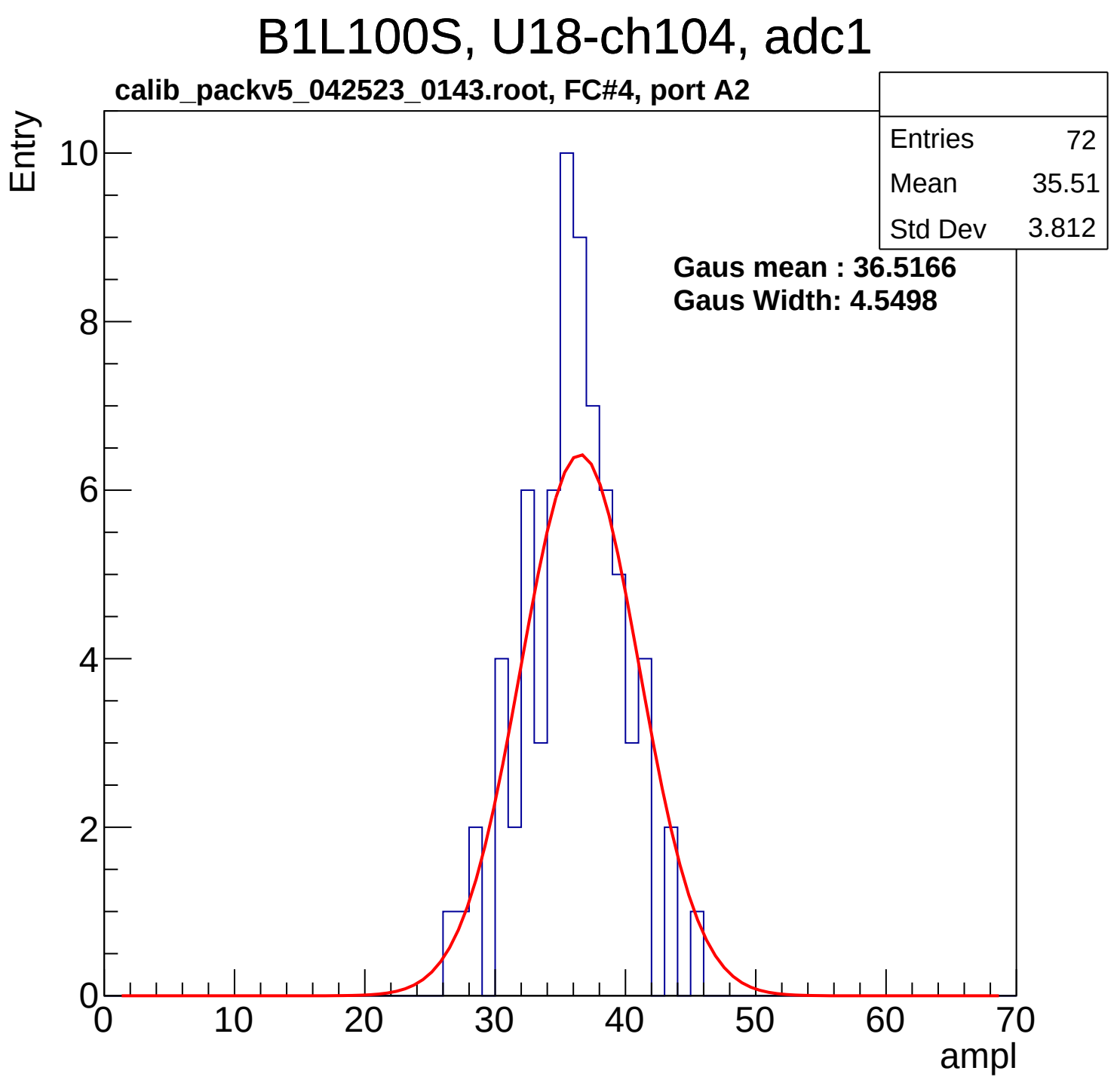

B1L100S, U18-ch103, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 56.37
Std Dev 3.08
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

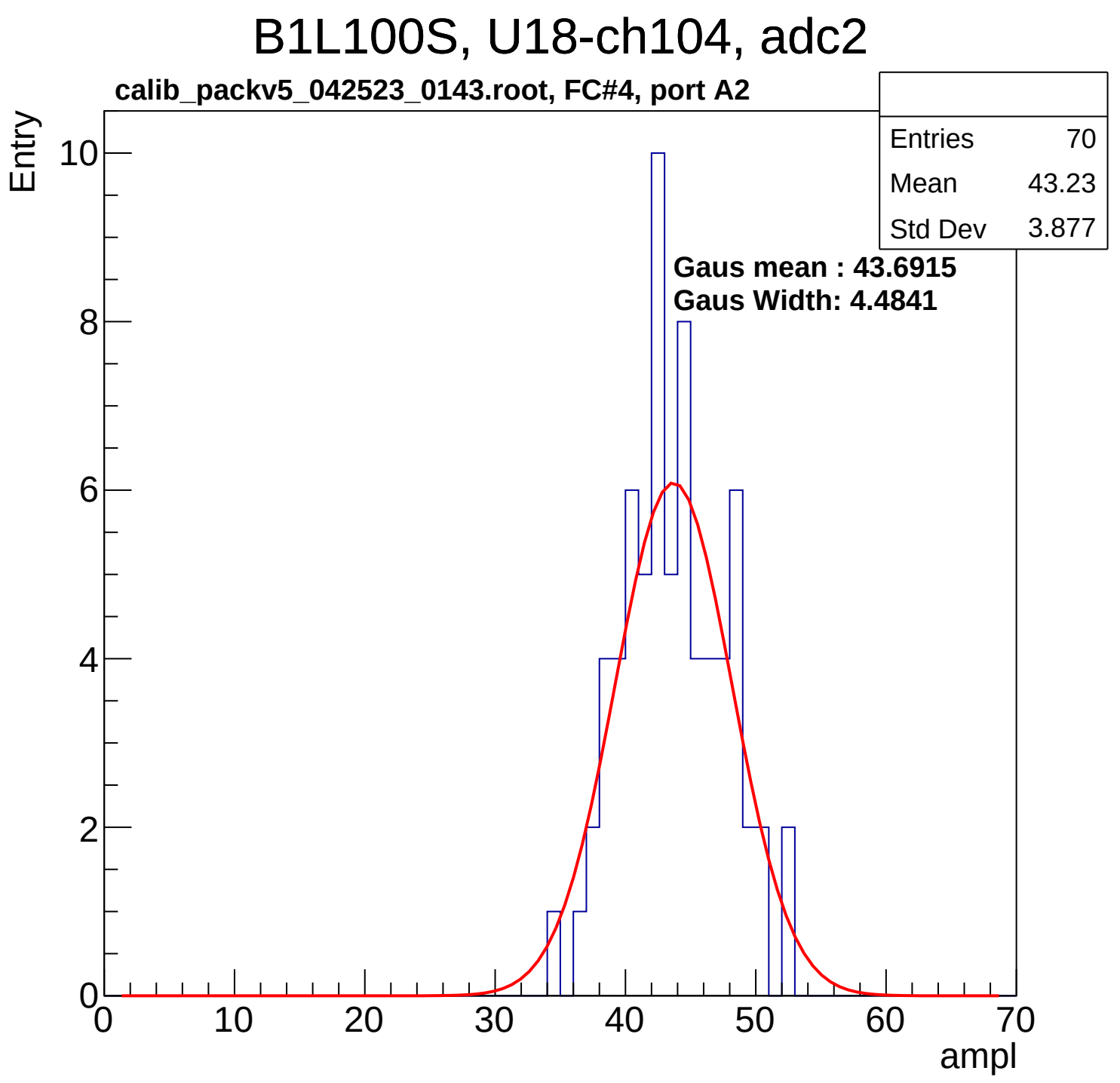

B1L100S, U18-ch103, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 59
Std Dev 9.316
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

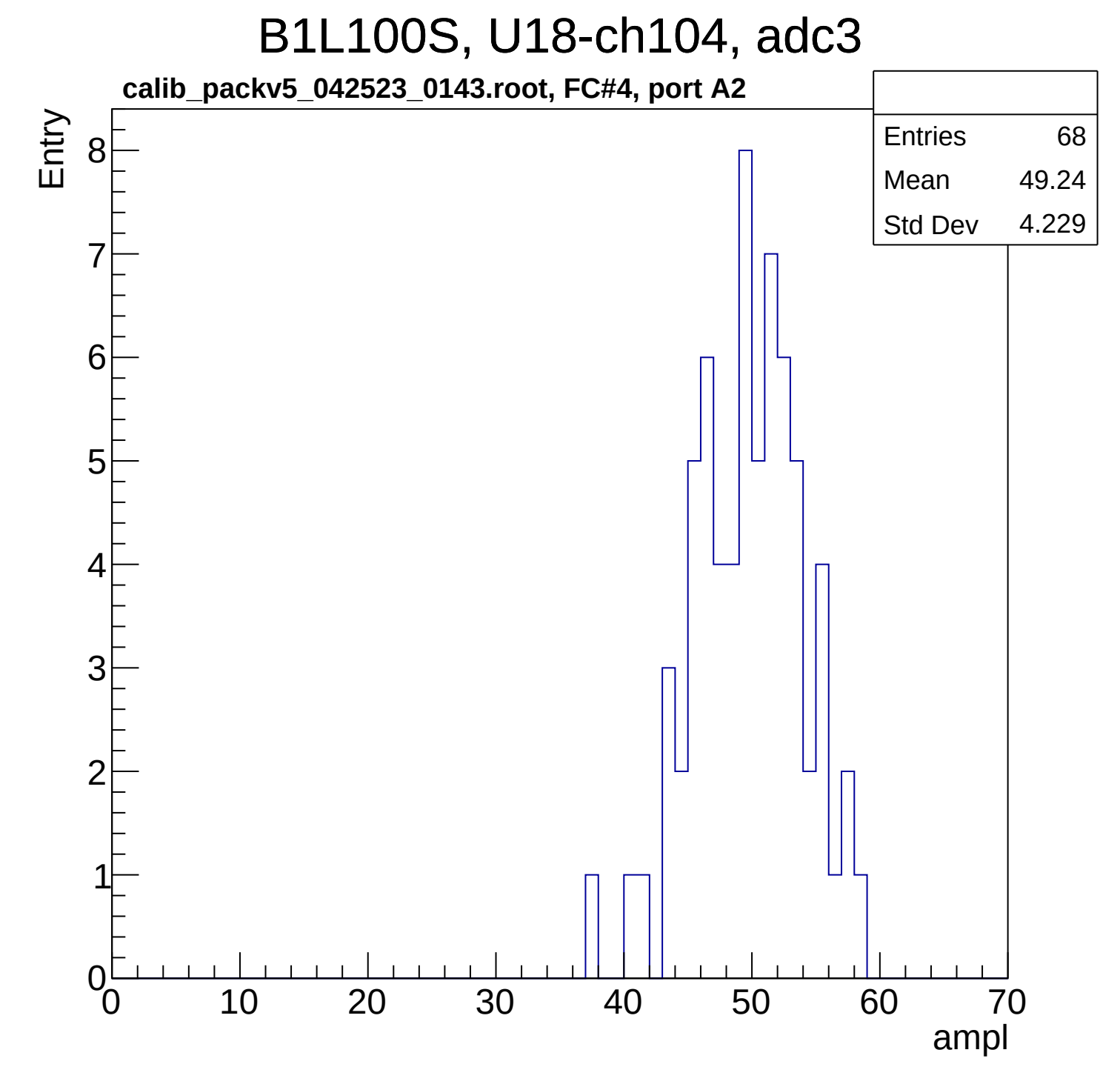

B1L100S, U18-ch103, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

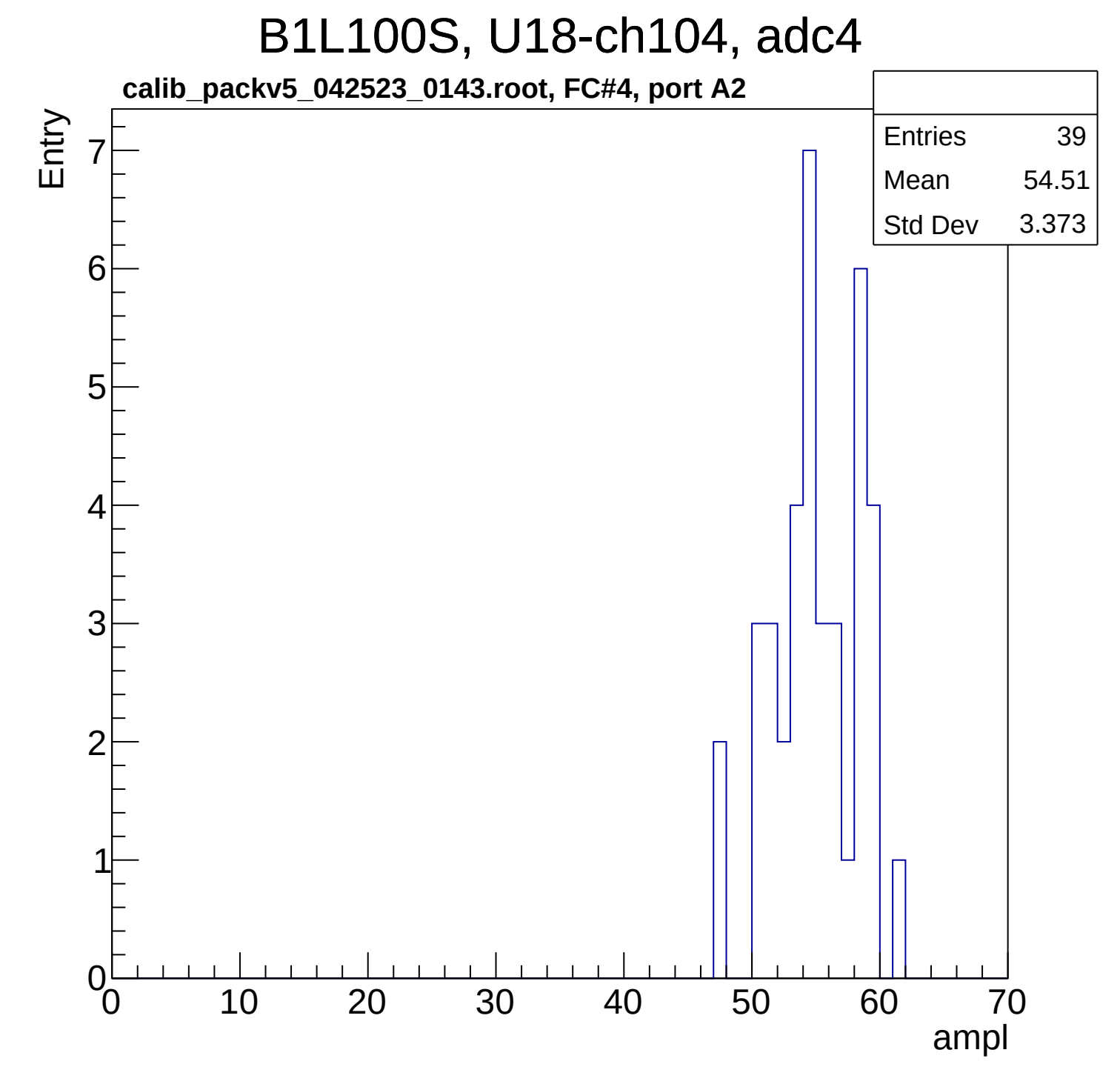

B1L100S, U18-ch103, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

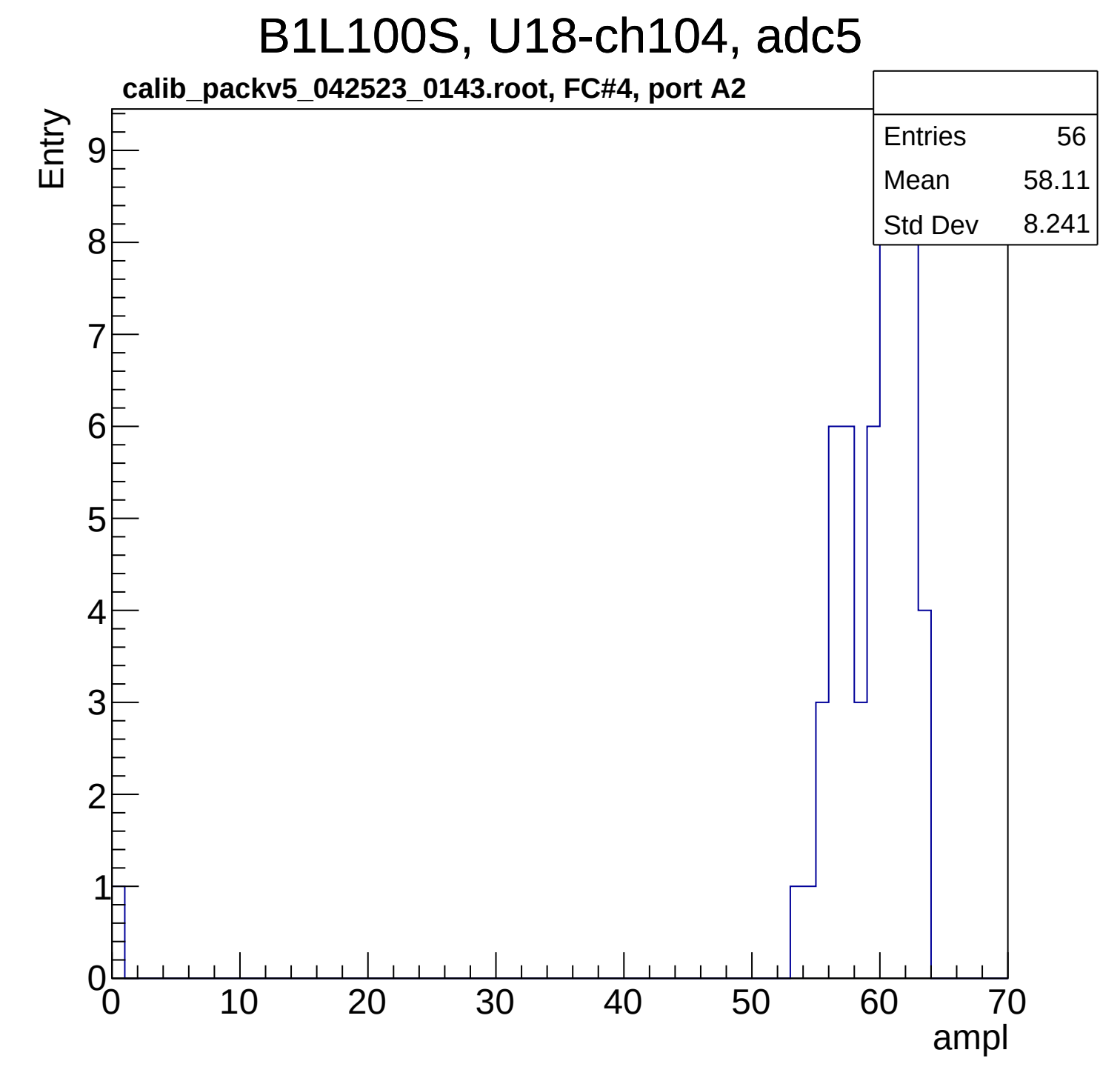

B1L100S, U18-ch104, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 27.08
Std Dev 6.537
Gaus mean : 29.4853
Gaus Width: 4.3002
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

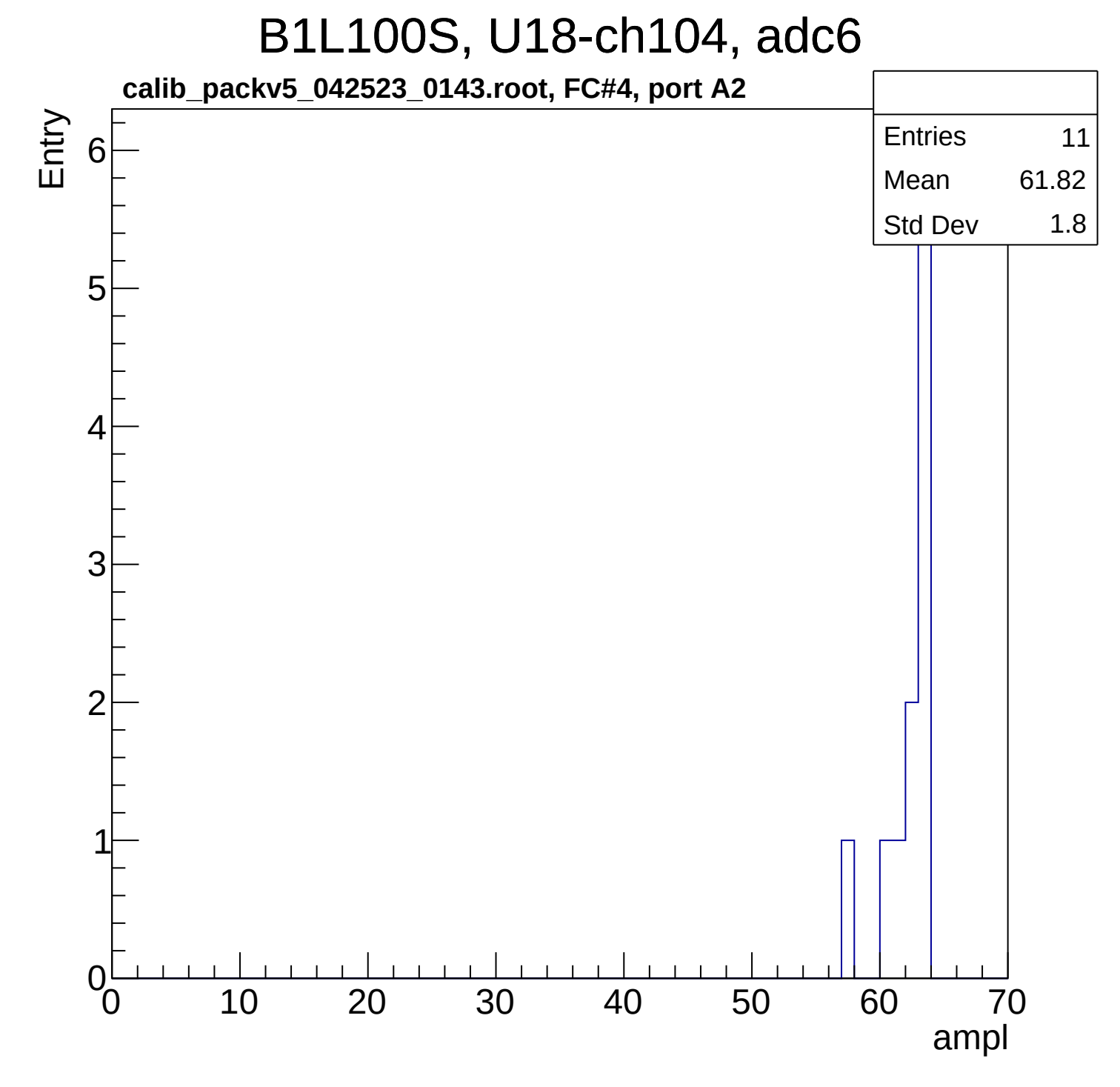

B1L100S, U18-ch104, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 35.51
Std Dev 3.812
Gaus mean : 36.5166
Gaus Width: 4.5498
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

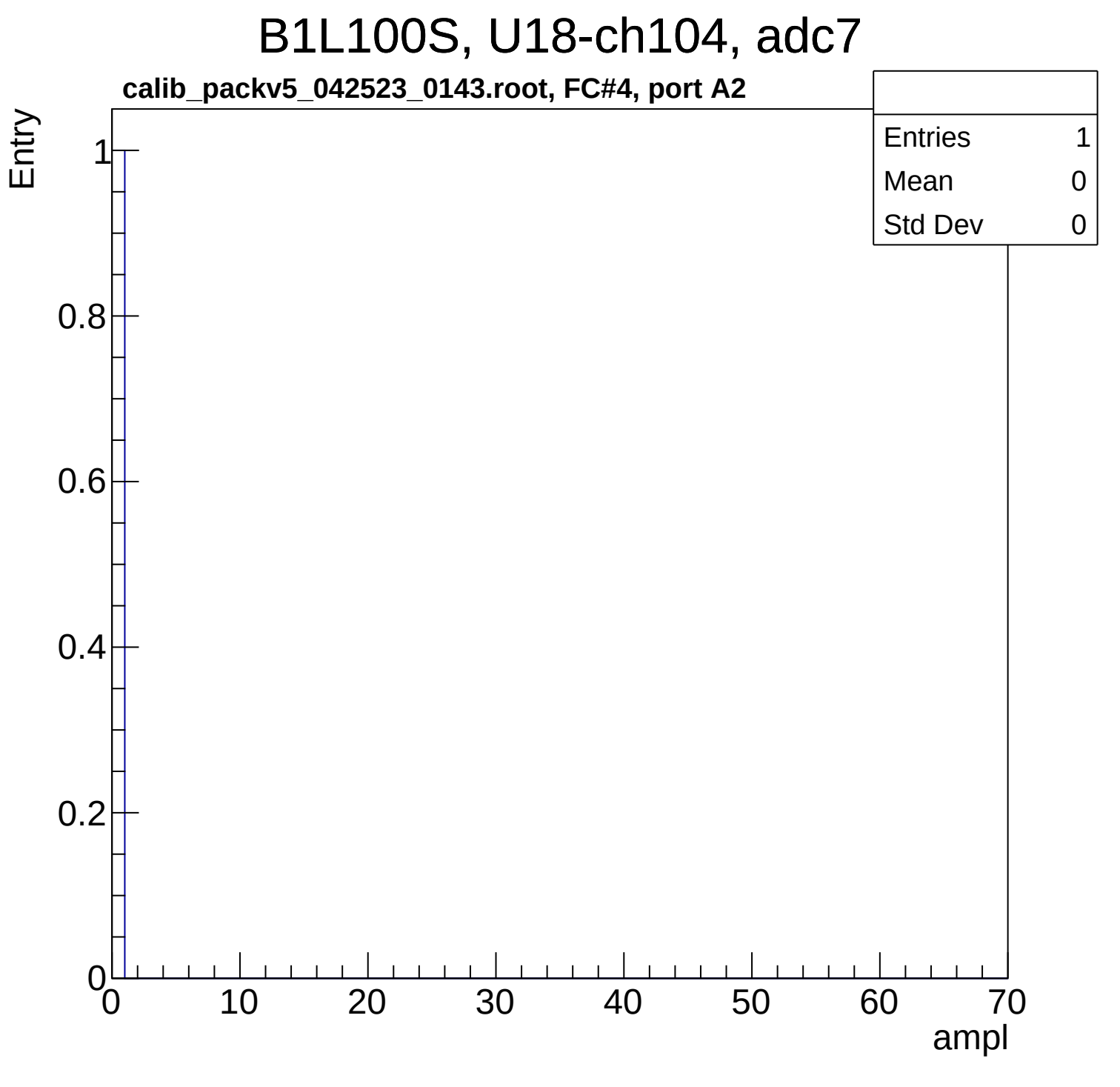

B1L100S, U18-ch104, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 43.23
Std Dev 3.877
Gaus mean : 43.6915
Gaus Width: 4.4841
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

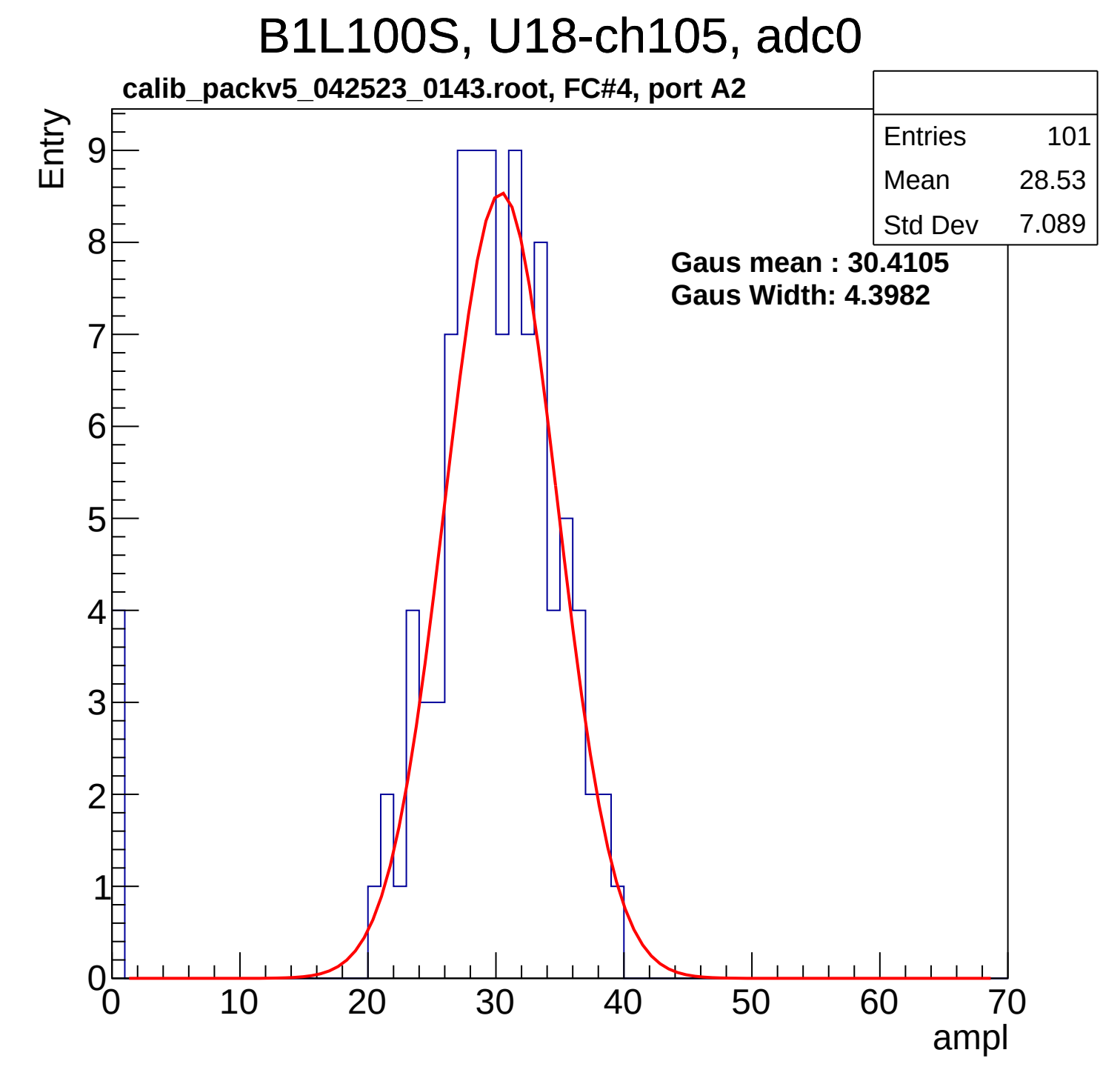

B1L100S, U18-ch104, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 49.24
Std Dev 4.229
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

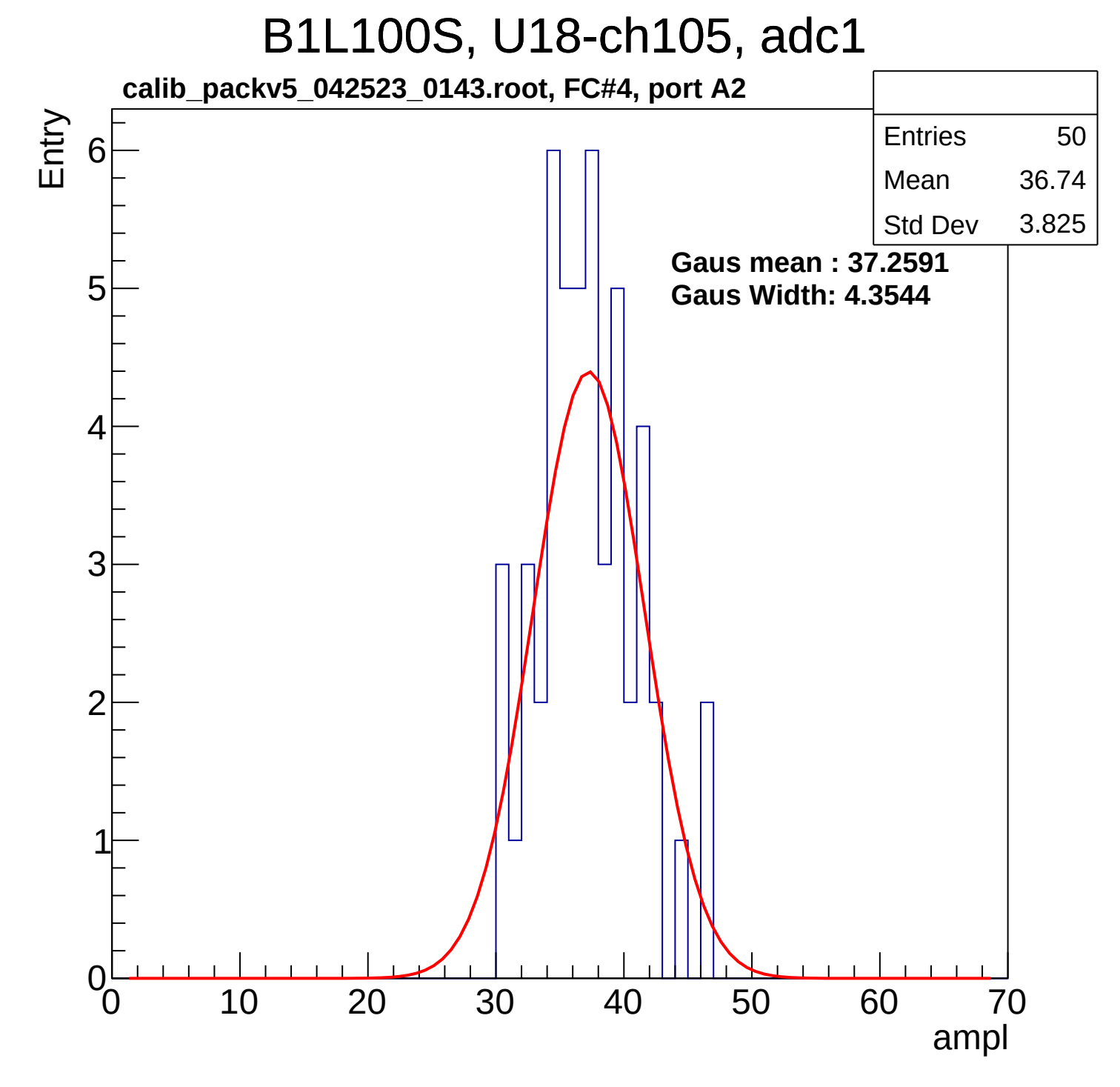

B1L100S, U18-ch104, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 39
Mean 54.51
Std Dev 3.373
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

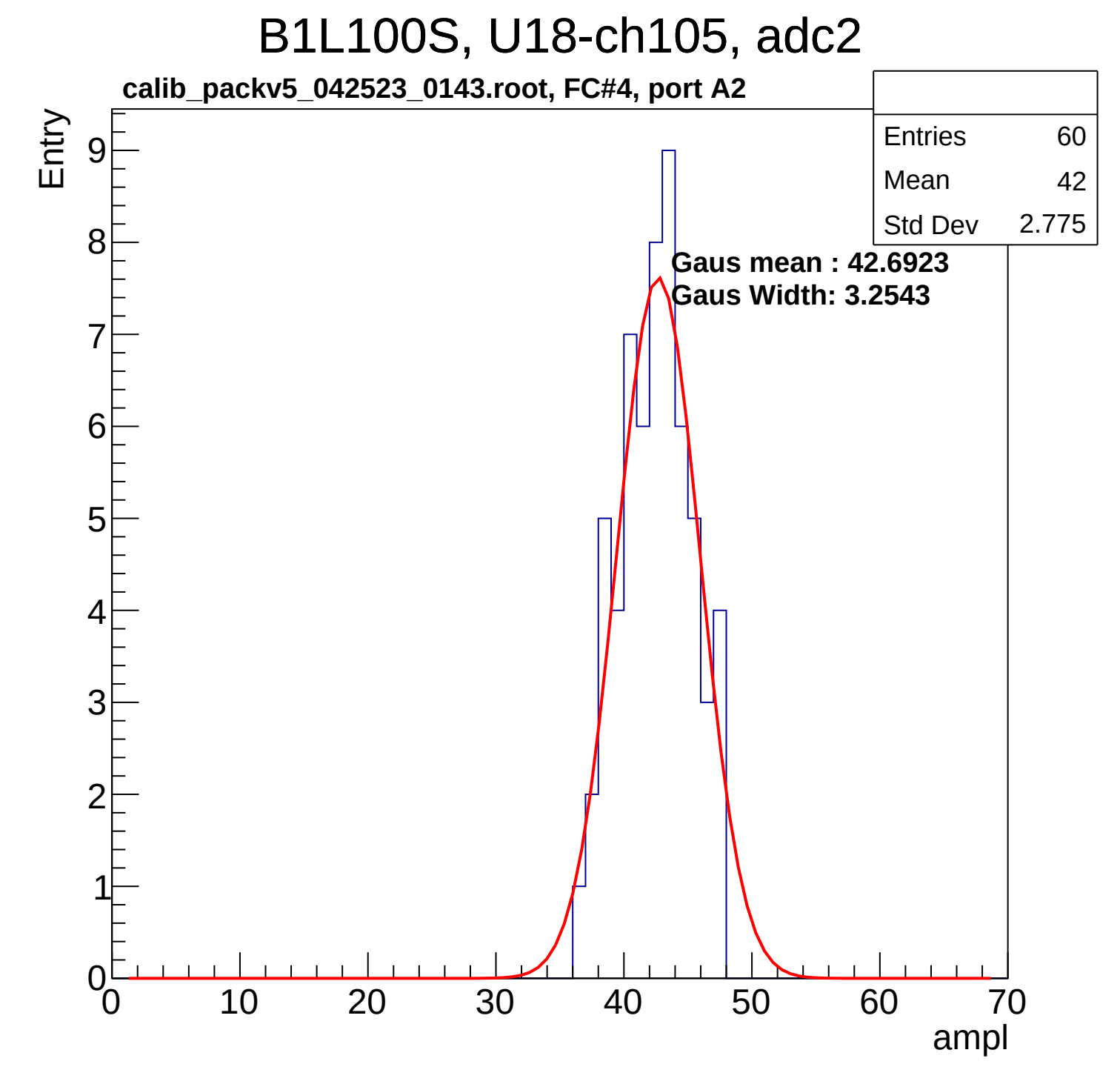

B1L100S, U18-ch104, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 58.11
Std Dev 8.241
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

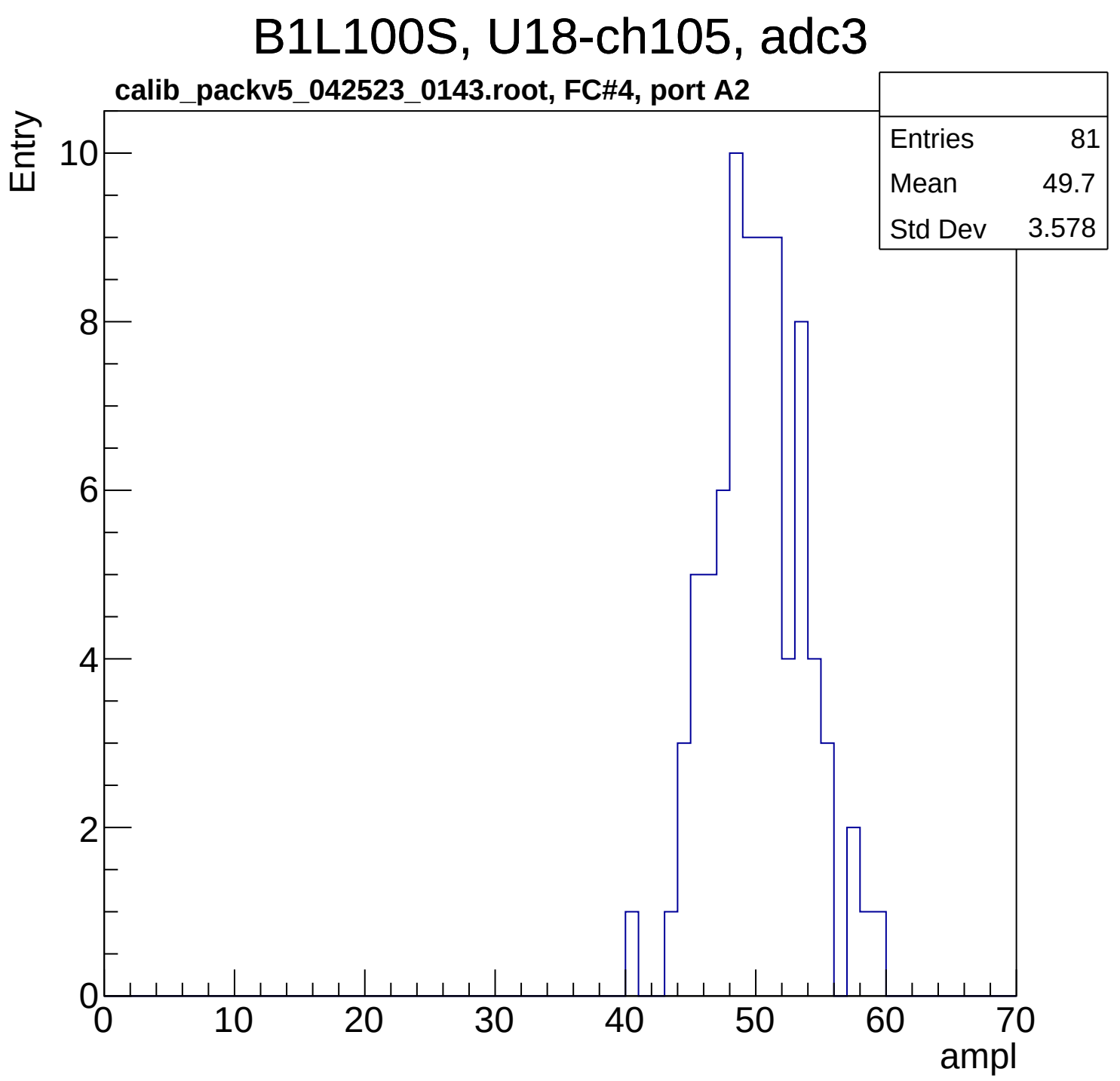

B1L100S, U18-ch104, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 11
Mean 61.82
Std Dev 1.8
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

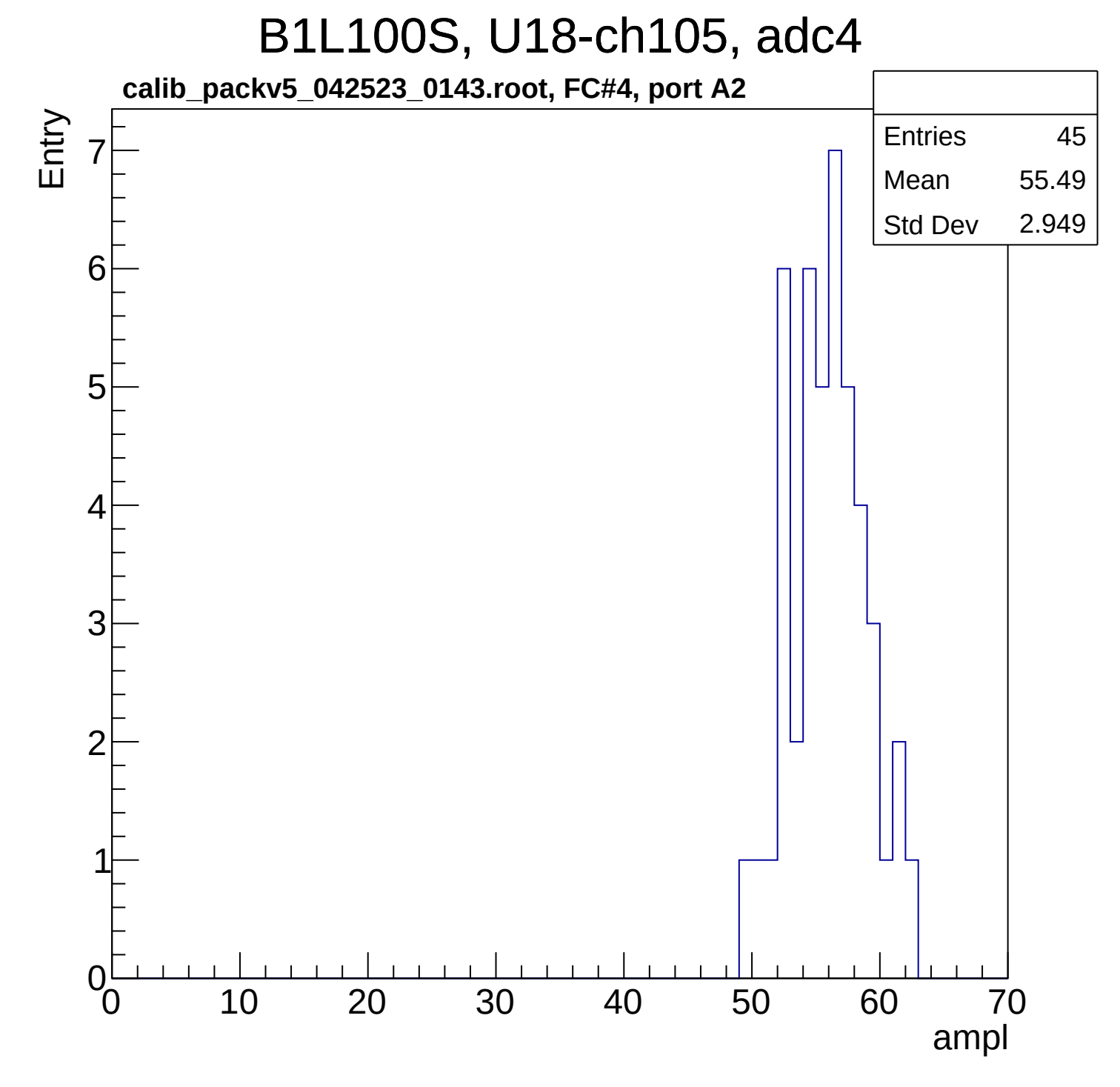

B1L100S, U18-ch104, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

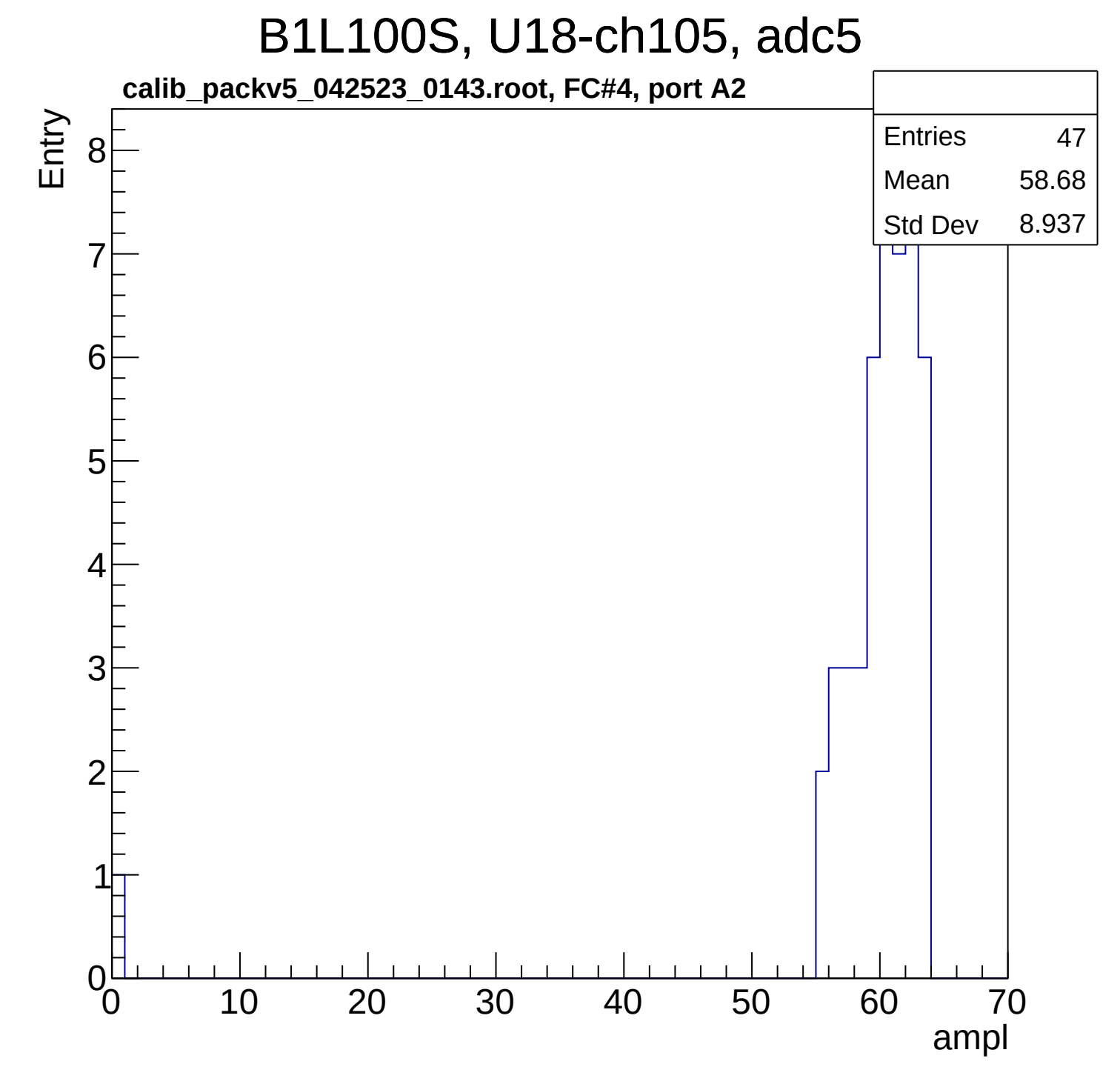

B1L100S, U18-ch105, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 101
Mean 28.53
Std Dev 7.089
Gaus mean : 30.4105
Gaus Width: 4.3982
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

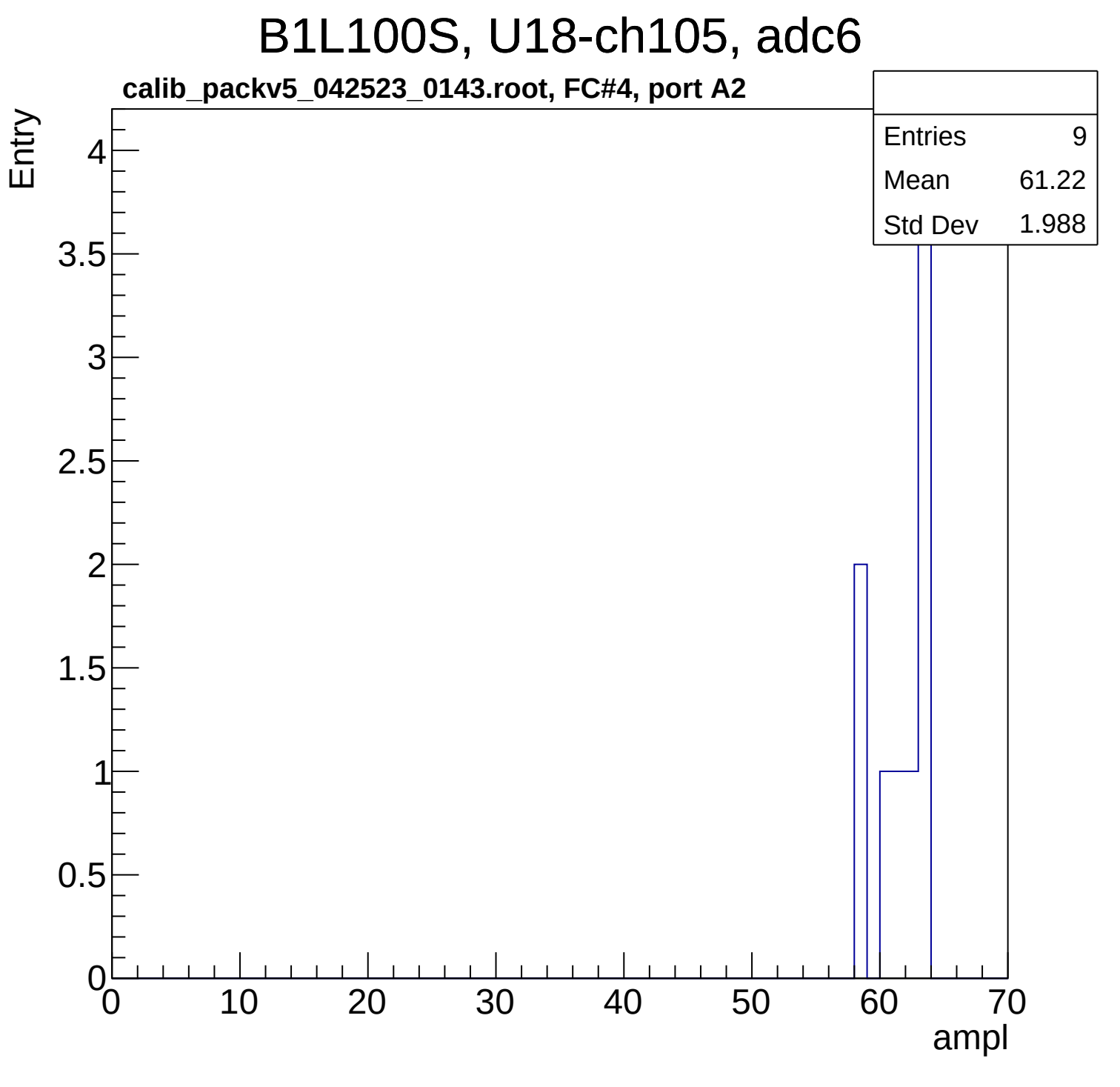

B1L100S, U18-ch105, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 36.74
Std Dev 3.825
Gaus mean : 37.2591
Gaus Width: 4.3544
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

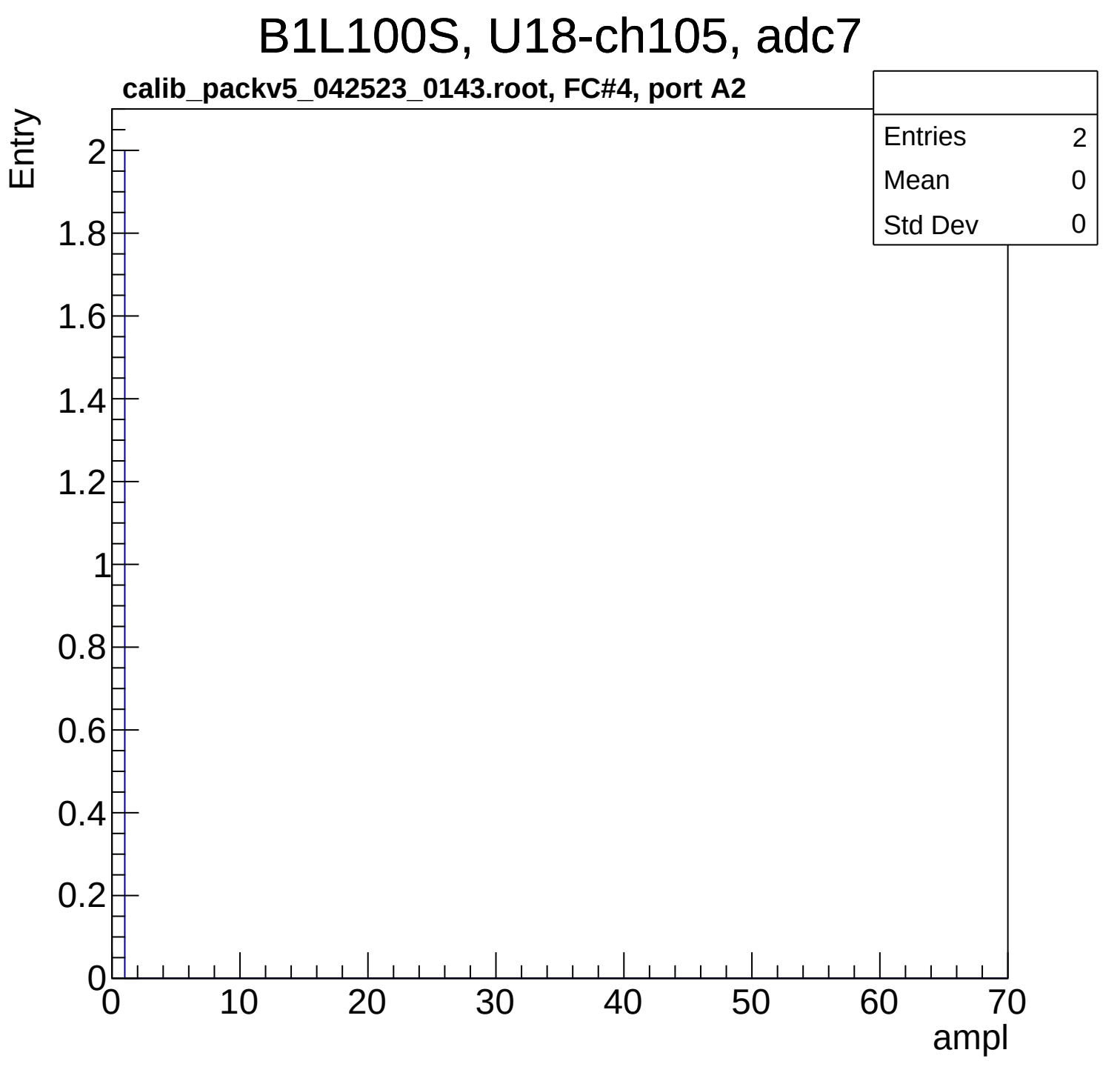

B1L100S, U18-ch105, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 42
Std Dev 2.775
Gaus mean : 42.6923
Gaus Width: 3.2543
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

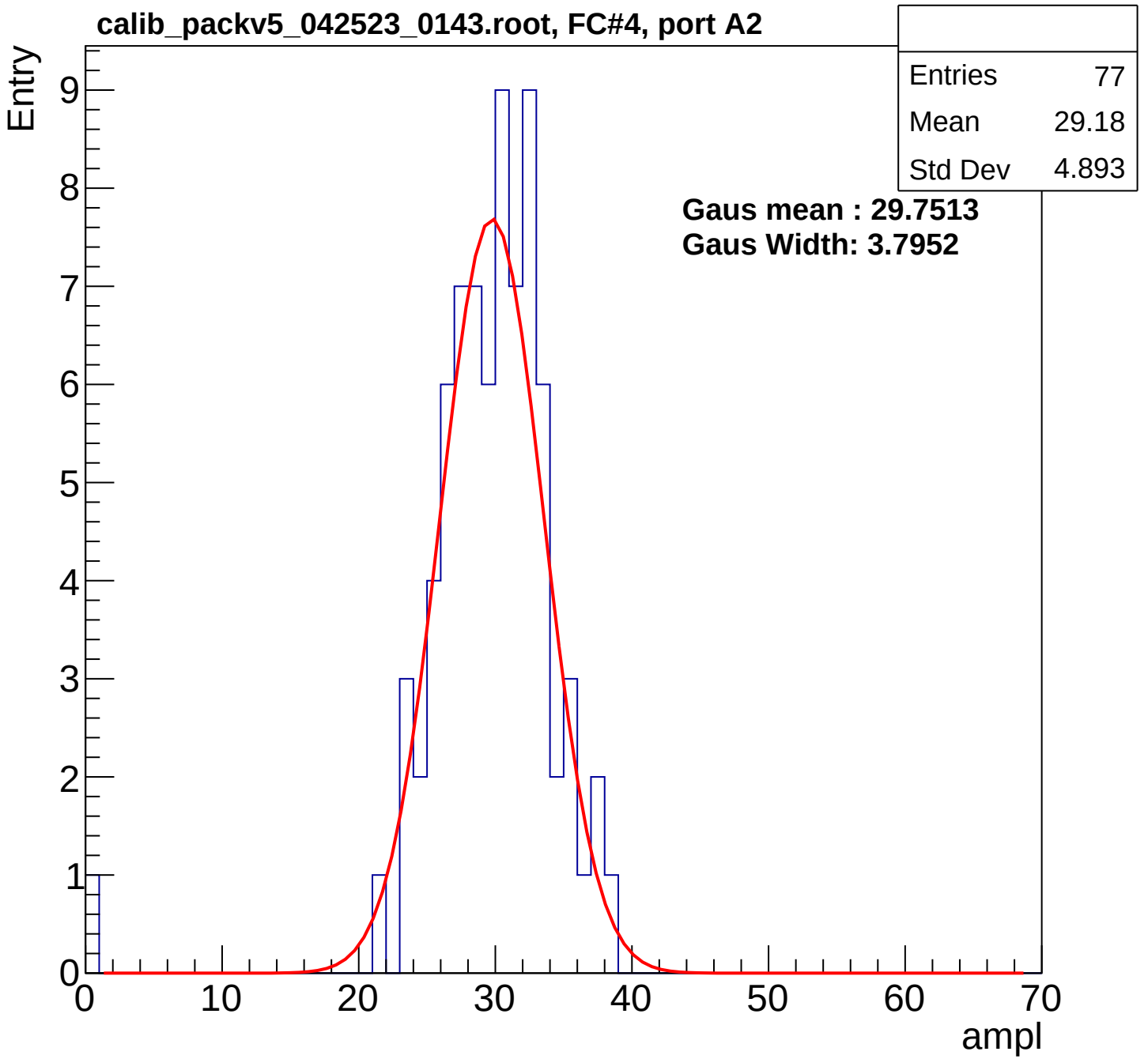

B1L100S, U18-ch105, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 49.7
Std Dev 3.578
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

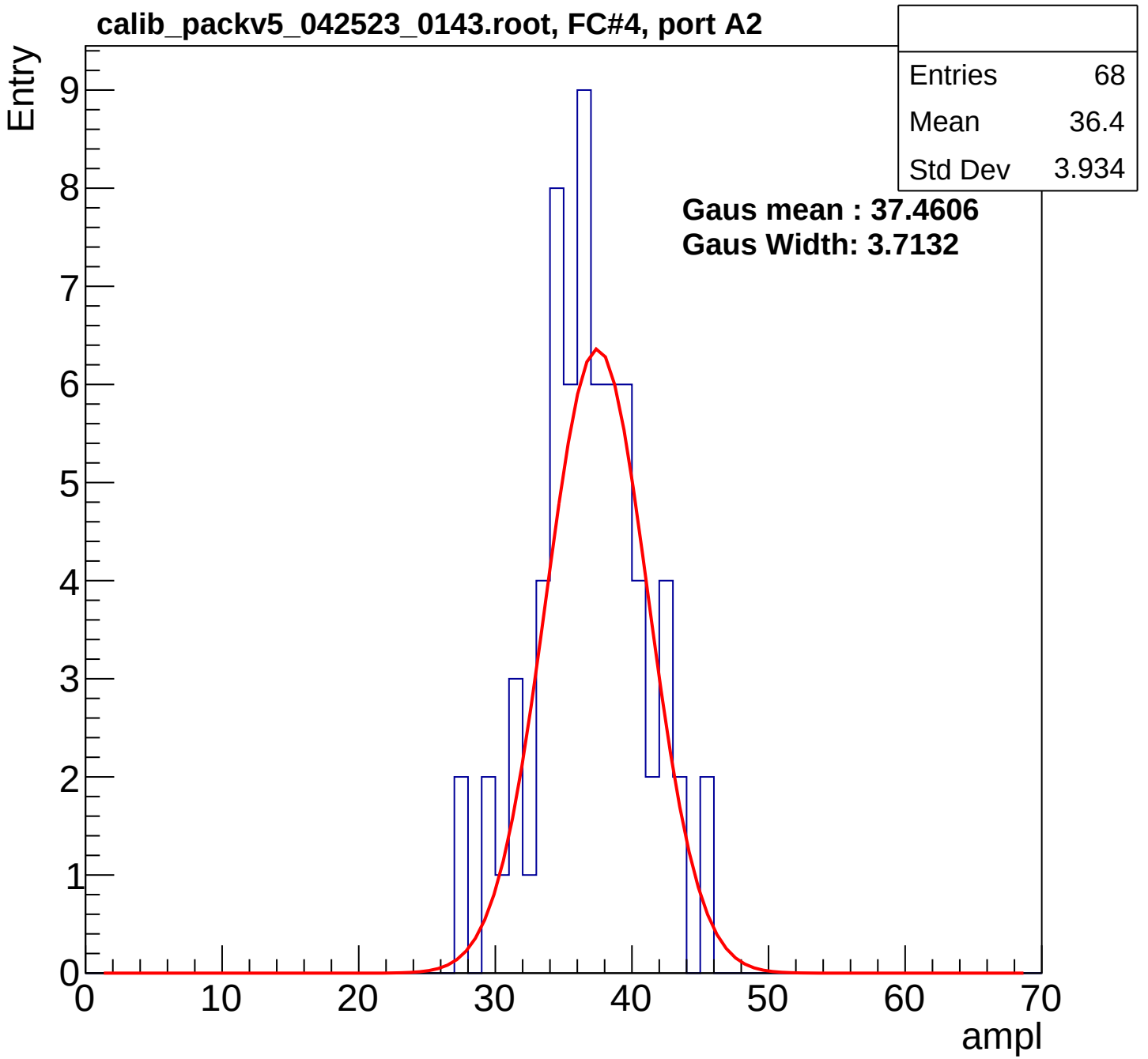

B1L100S, U18-ch105, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 45
Mean 55.49
Std Dev 2.949
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

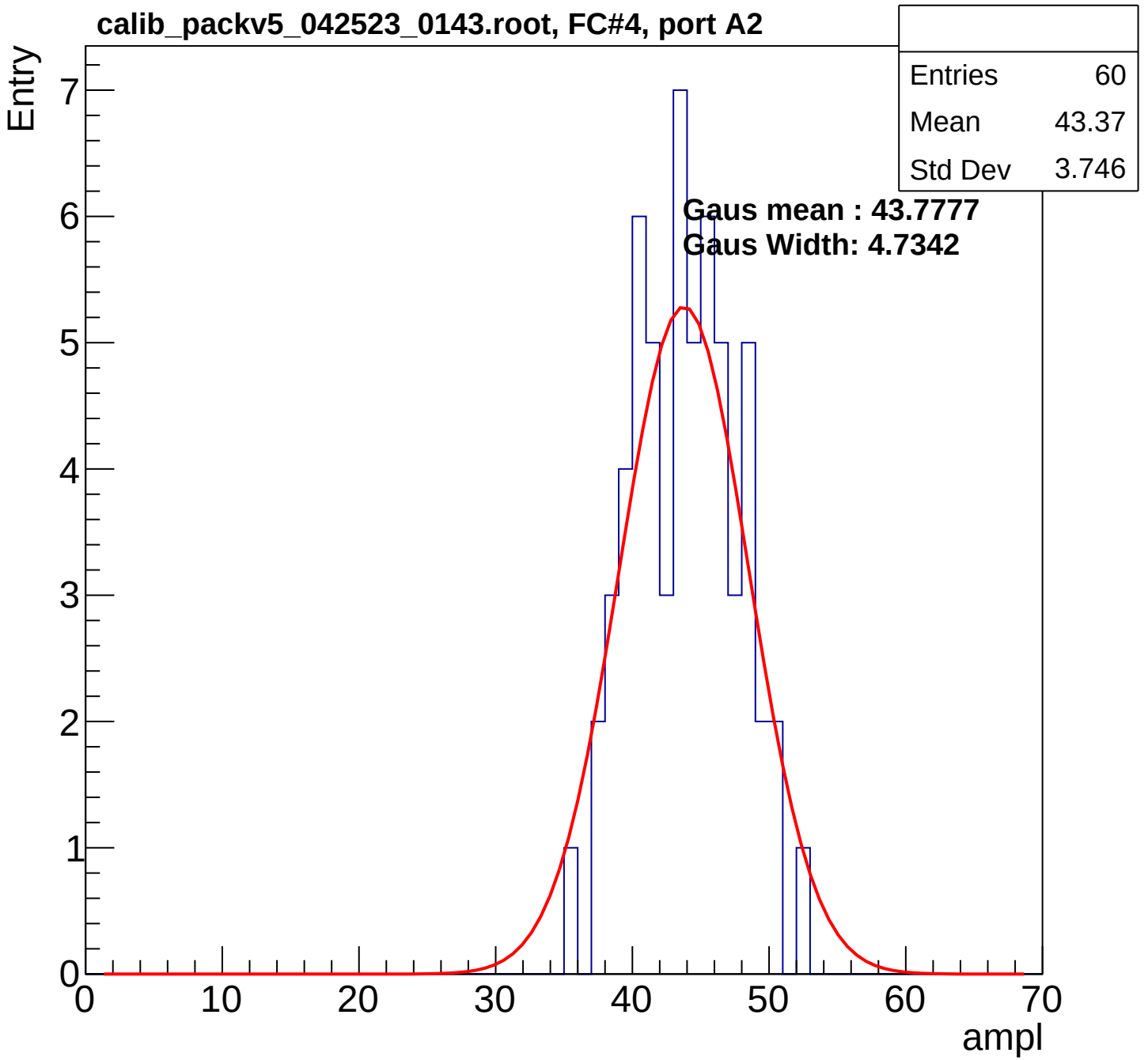

B1L100S, U18-ch105, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 58.68
Std Dev 8.937
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

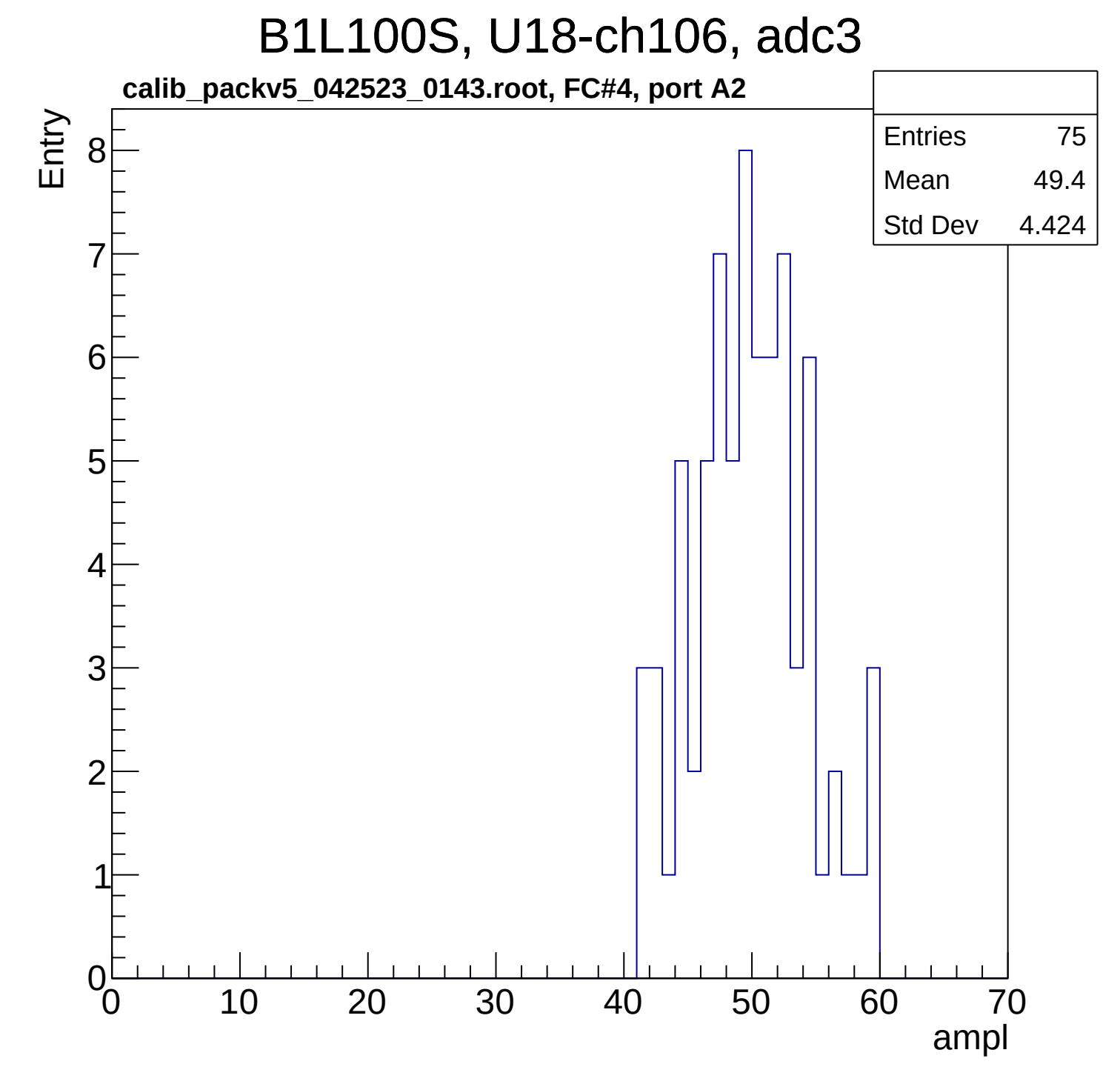

B1L100S, U18-ch105, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 61.22
Std Dev 1.988
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

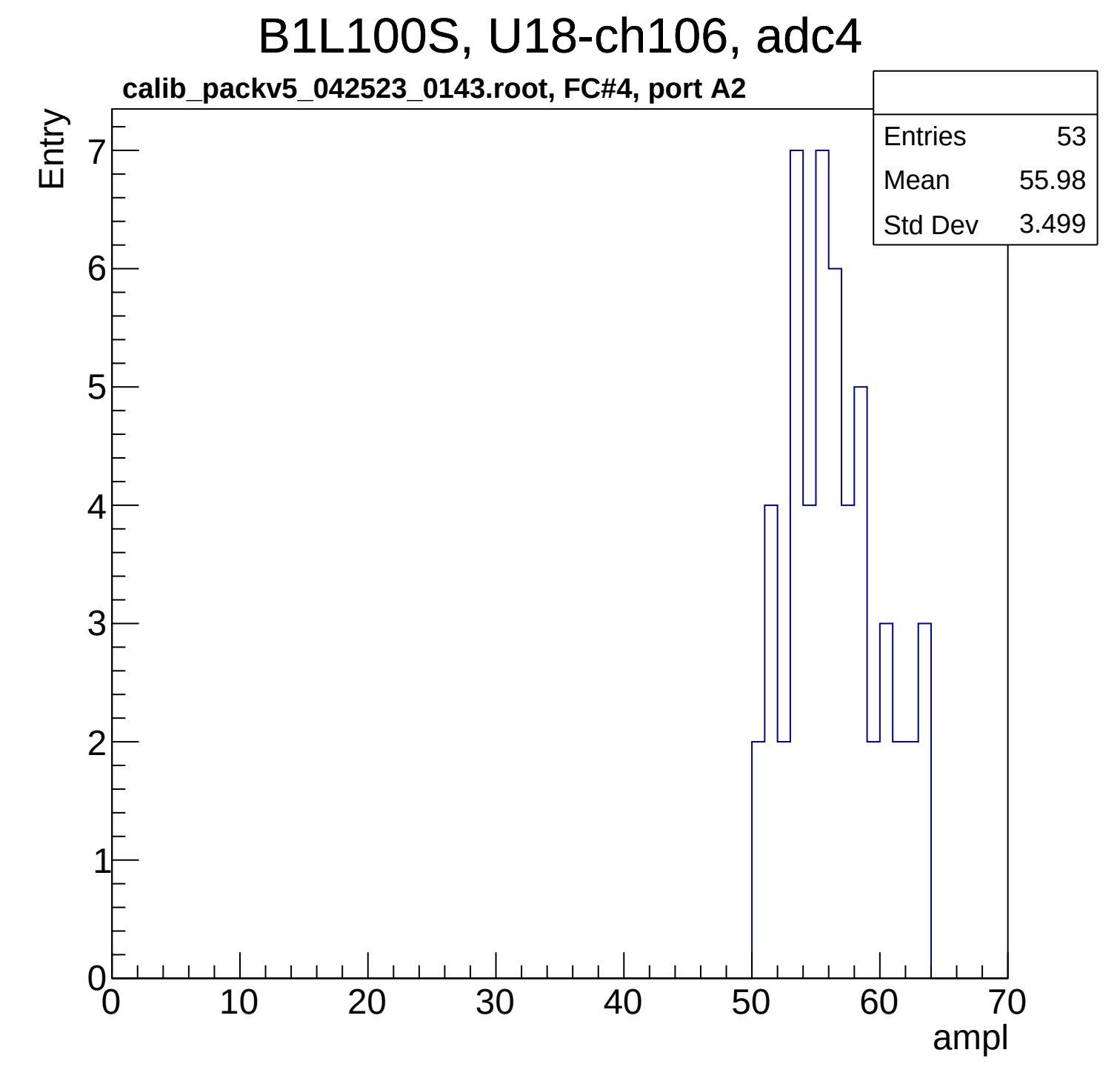

B1L100S, U18-ch105, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

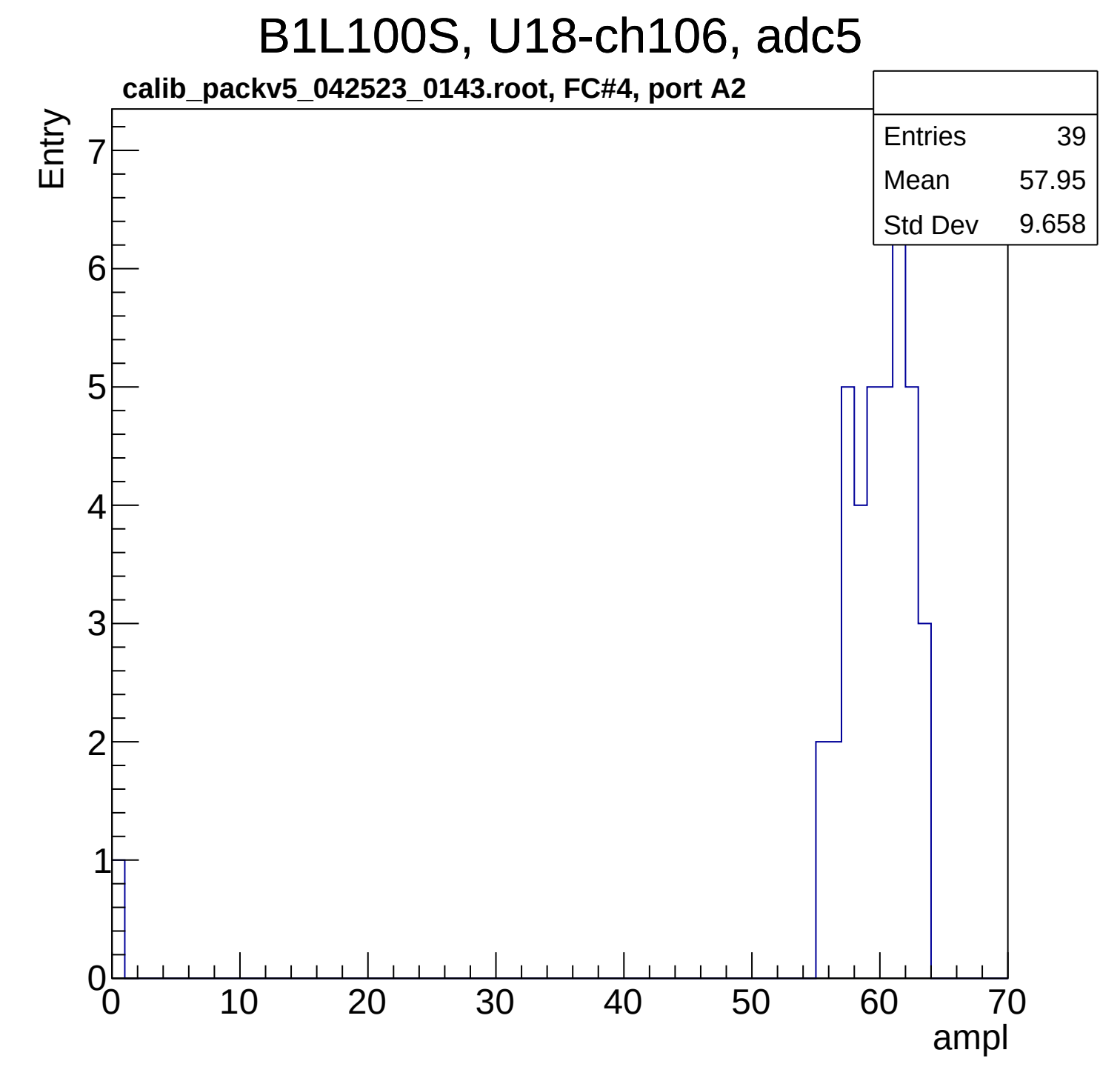

B1L100S, U18-ch106, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 77
Mean 29.18
Std Dev 4.893
Gaus mean : 29.7513
Gaus Width: 3.7952
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

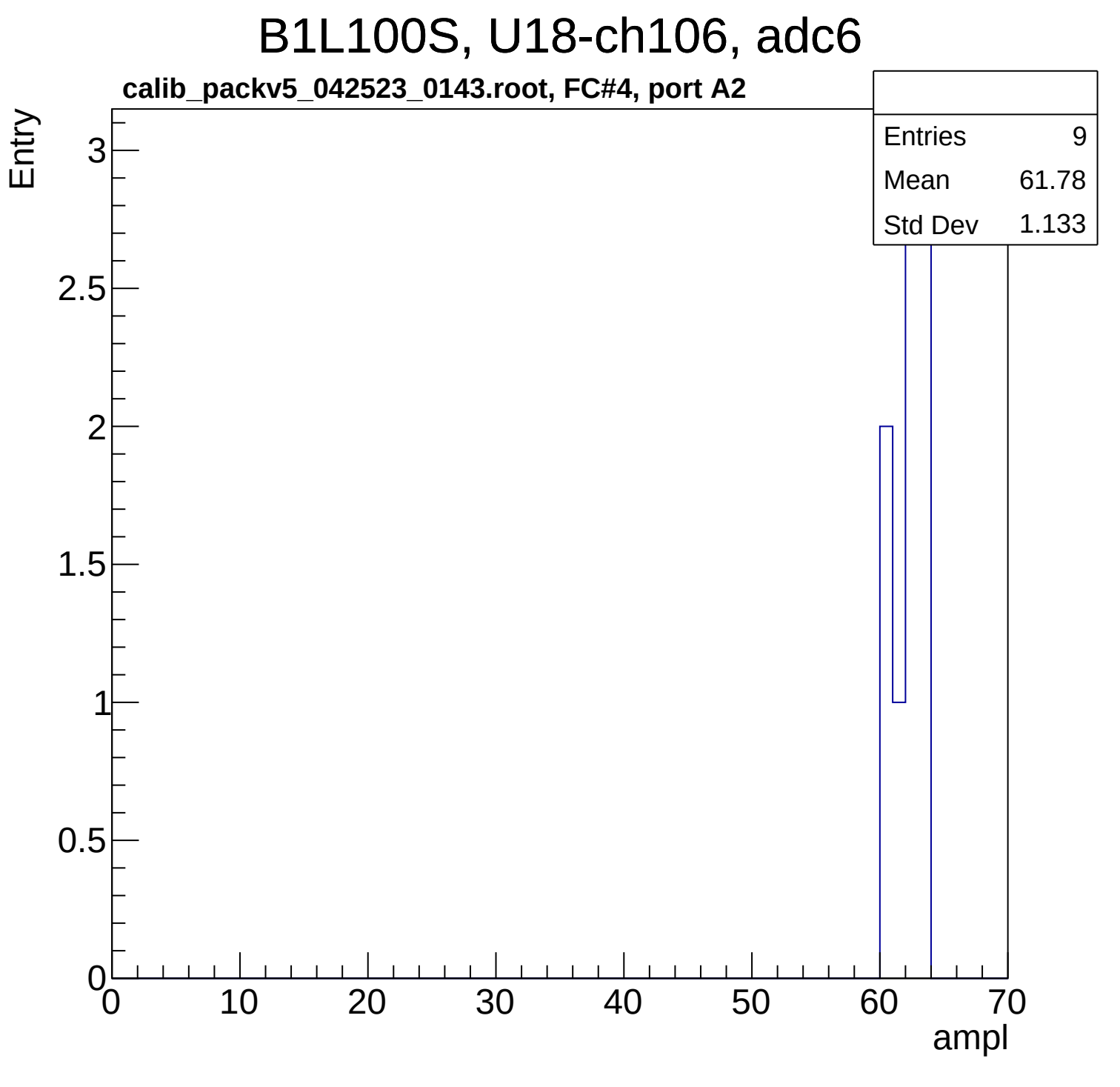

B1L100S, U18-ch106, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 36.4
Std Dev 3.934
Gaus mean : 37.4606
Gaus Width: 3.7132
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

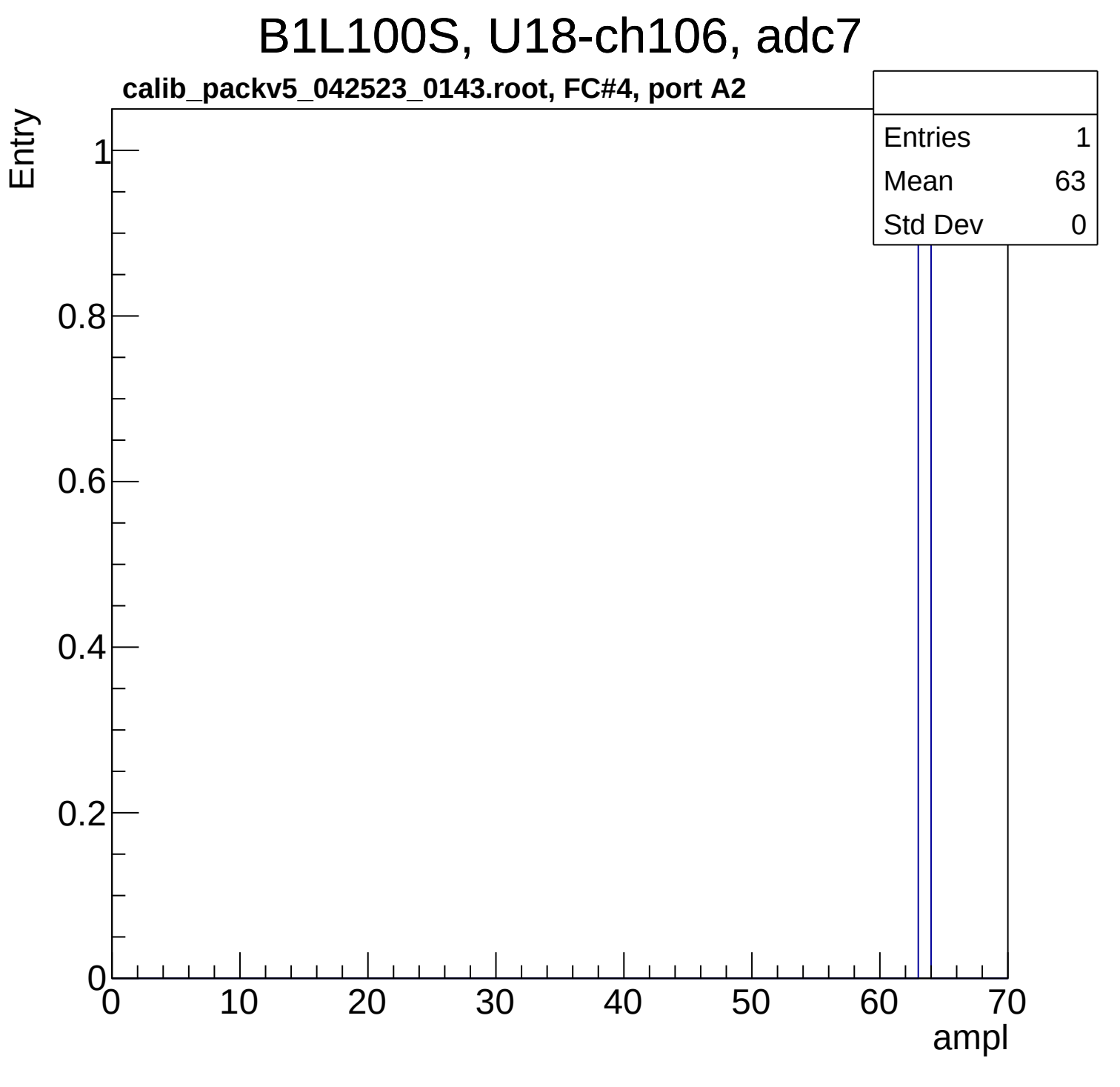

B1L100S, U18-ch106, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 43.37
Std Dev 3.746
Gaus mean : 43.7777
Gaus Width: 4.7342
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

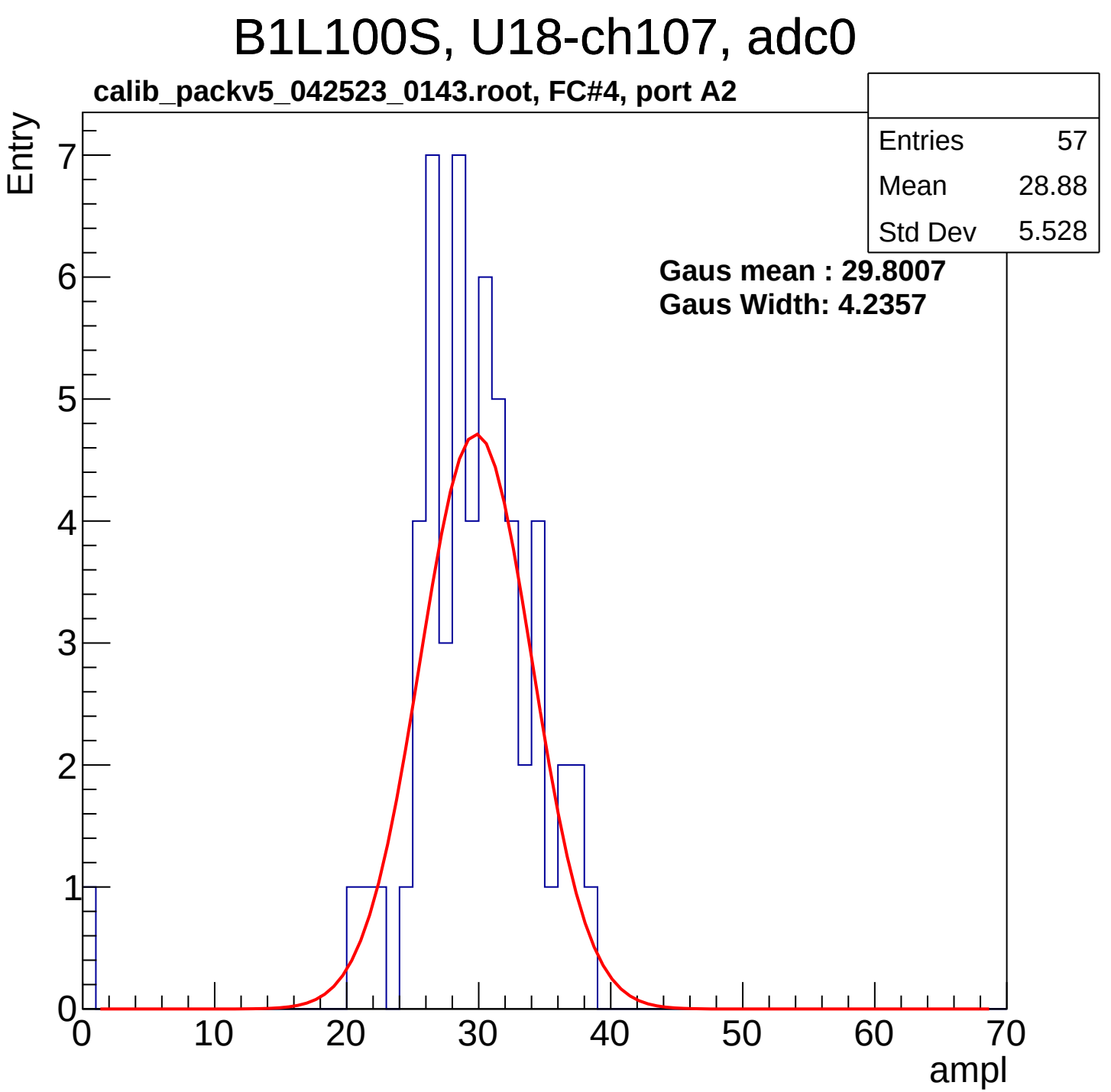

B1L100S, U18-ch106, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 49.4
Std Dev 4.424
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

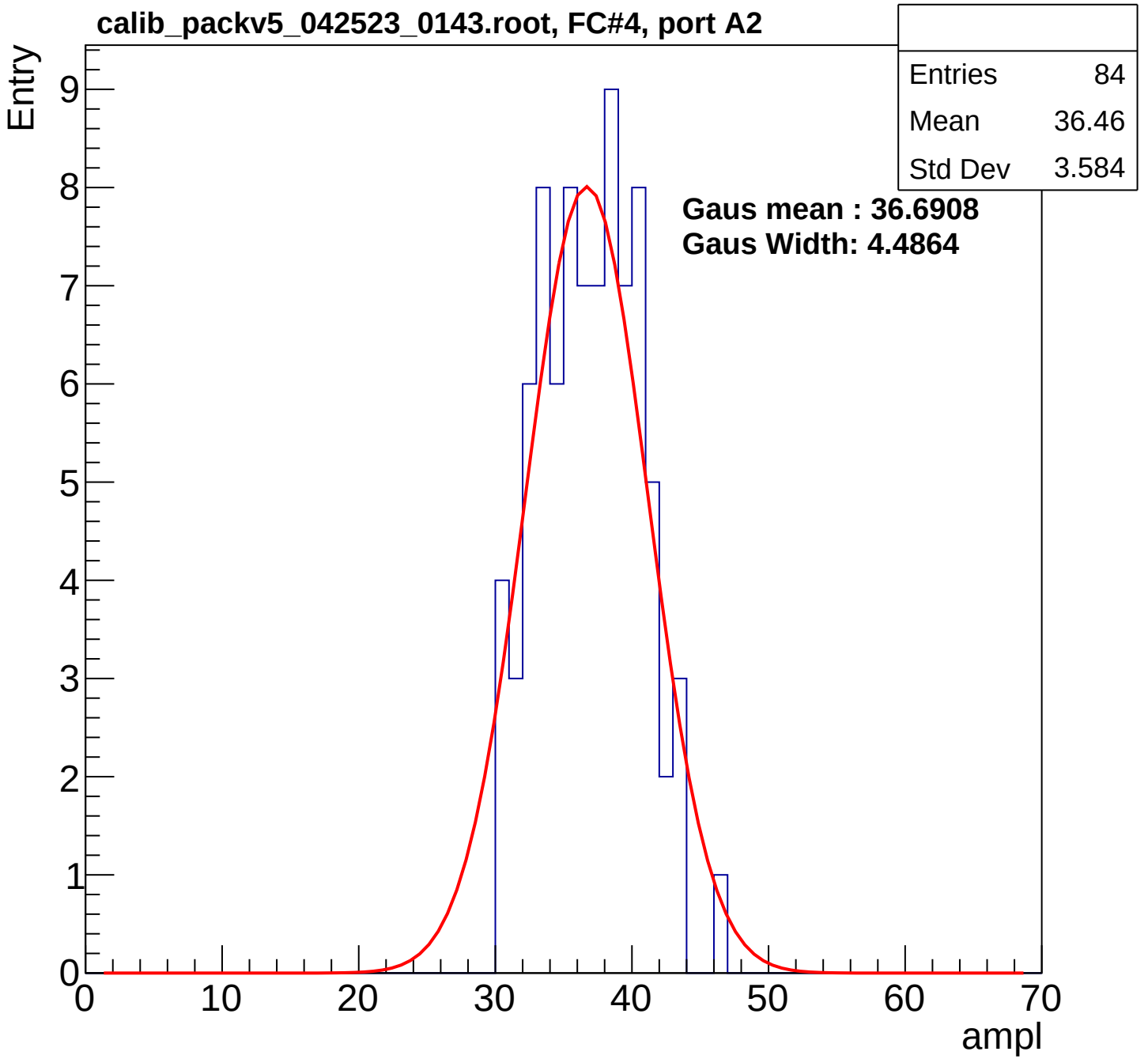

B1L100S, U18-ch106, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 55.98
Std Dev 3.499
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

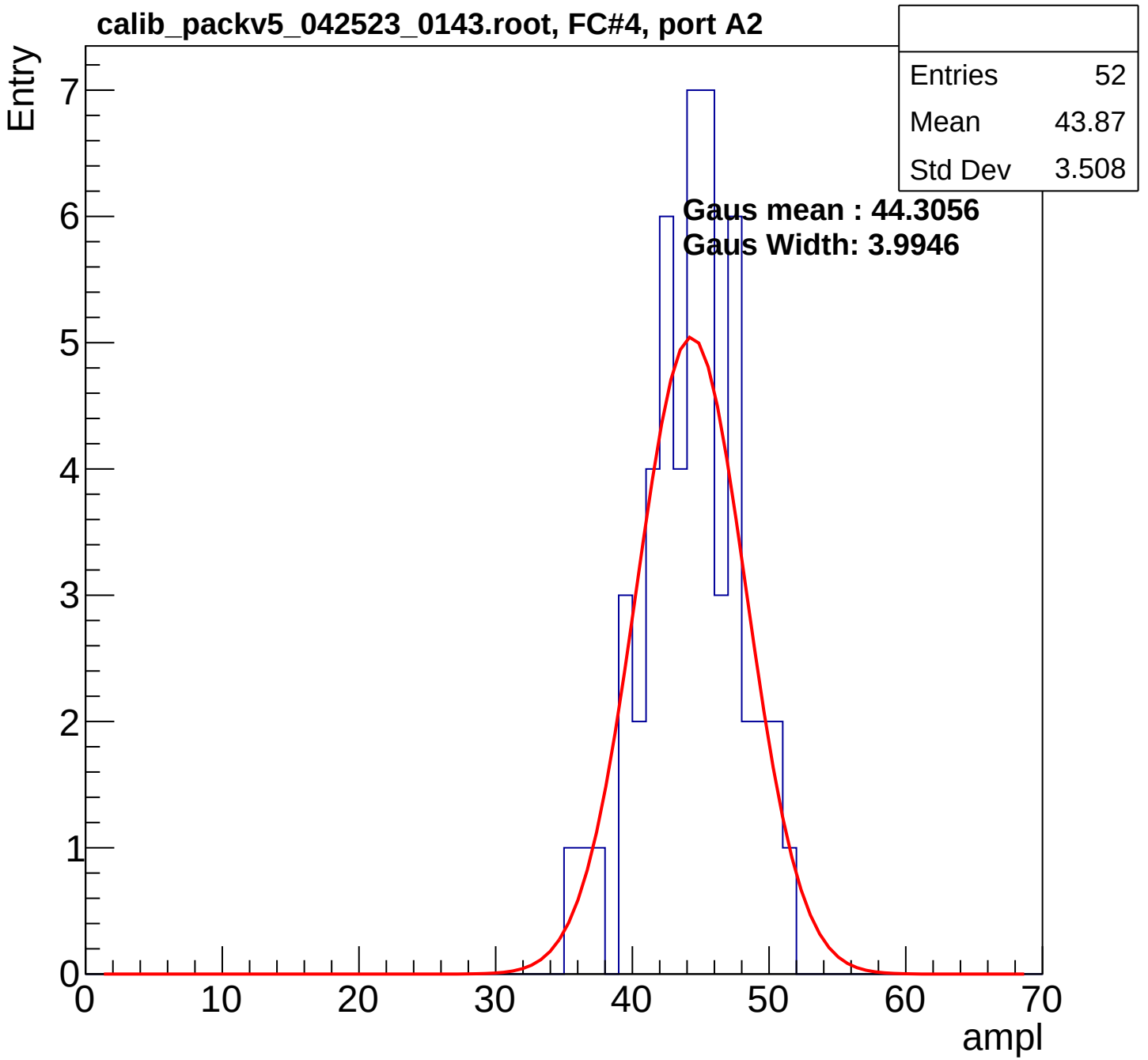

B1L100S, U18-ch106, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 39
Mean 57.95
Std Dev 9.658
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

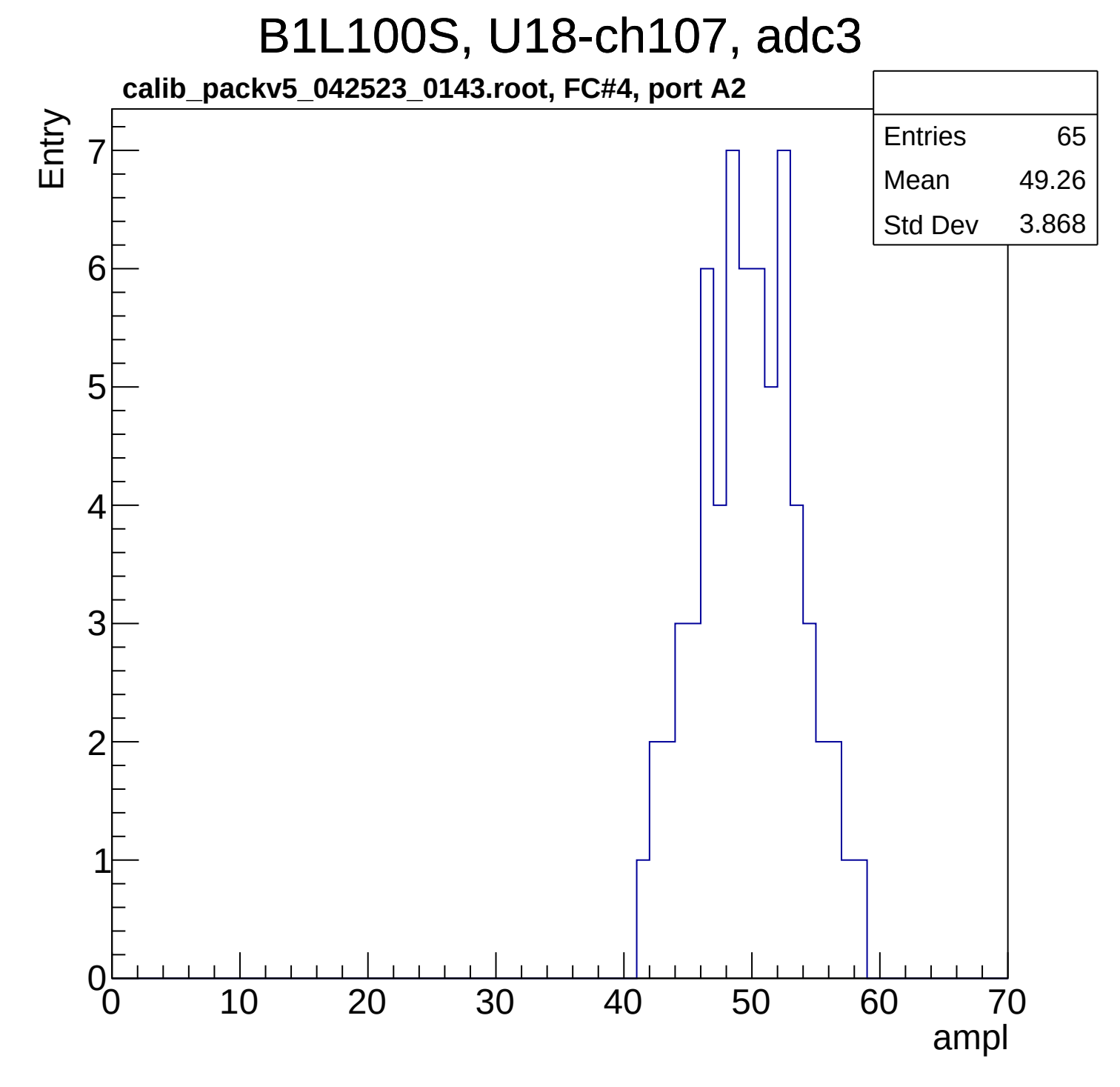

B1L100S, U18-ch106, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 61.78
Std Dev 1.133
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

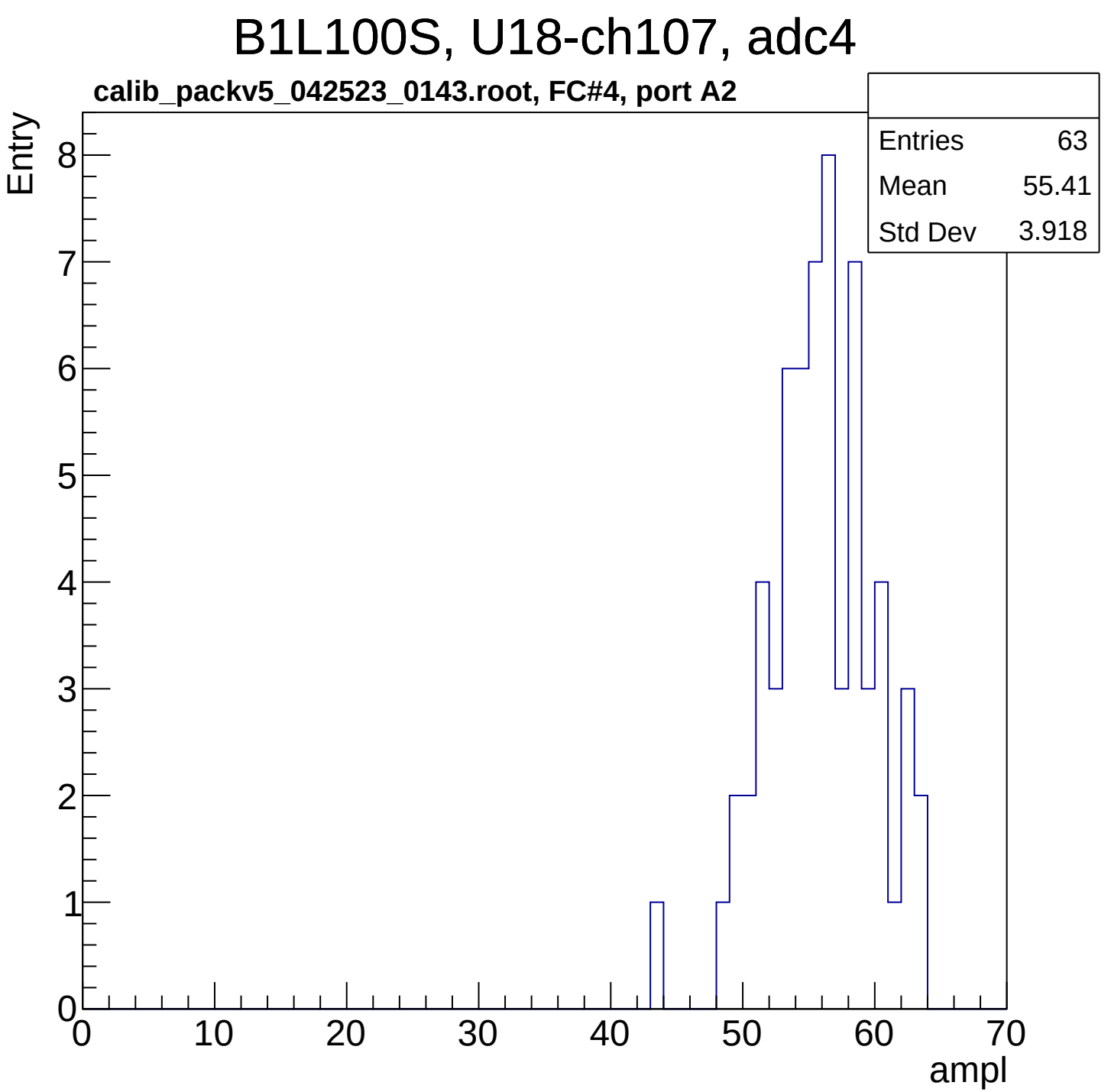

B1L100S, U18-ch106, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

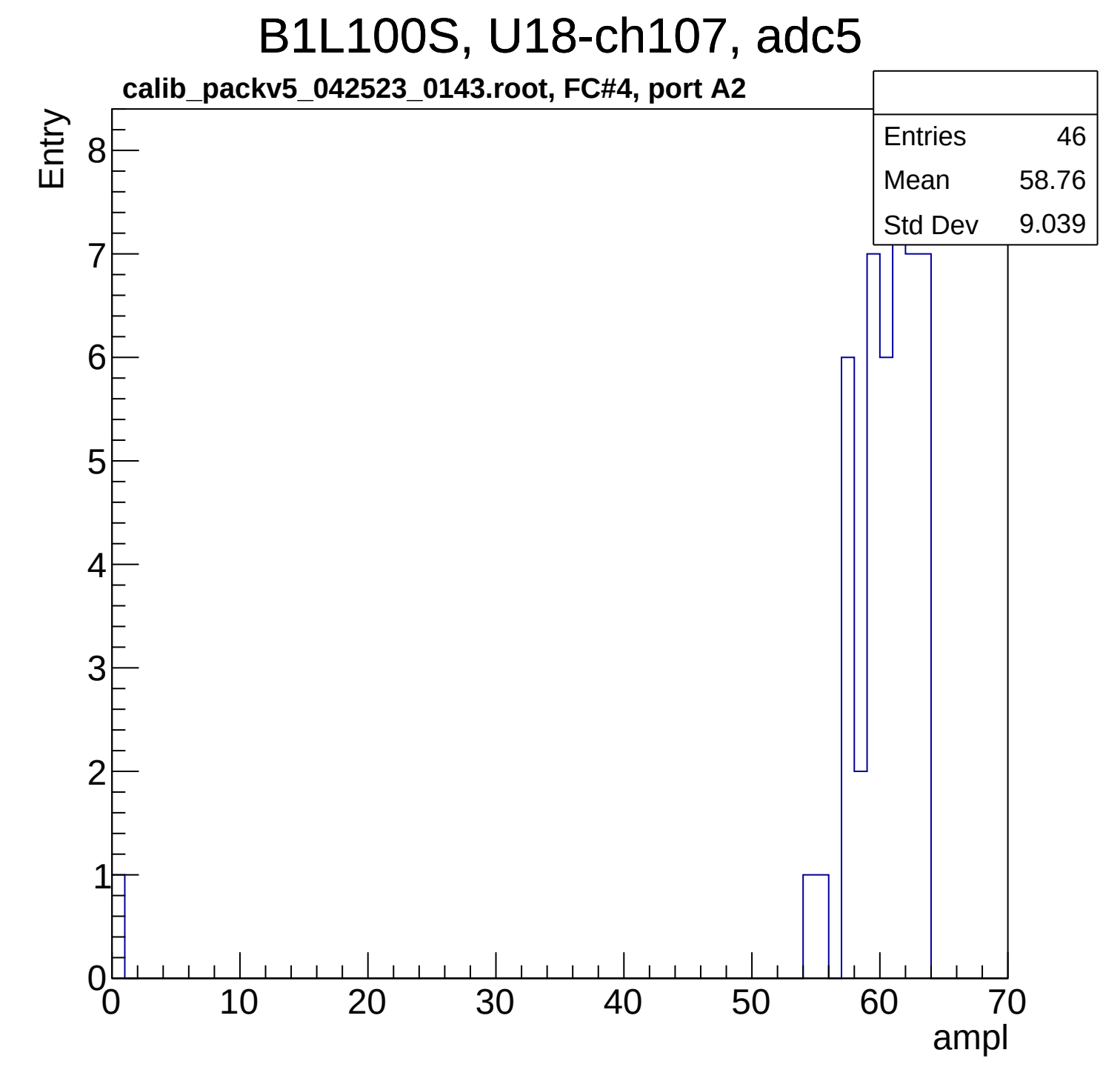

B1L100S, U18-ch107, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 28.88
Std Dev 5.528
Gaus mean : 29.8007
Gaus Width: 4.2357
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

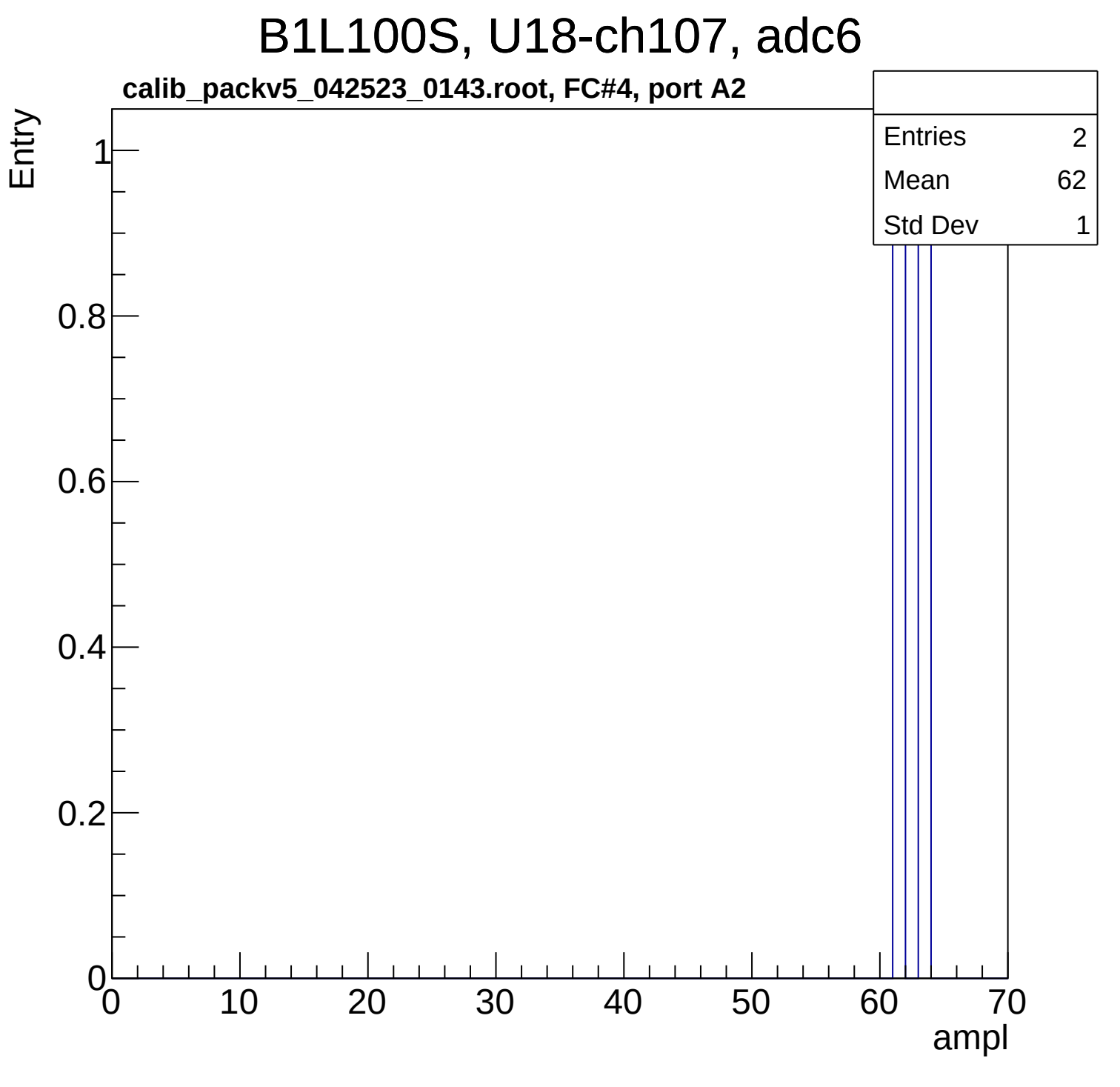

B1L100S, U18-ch107, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 84
Mean 36.46
Std Dev 3.584
Gaus mean : 36.6908
Gaus Width: 4.4864
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

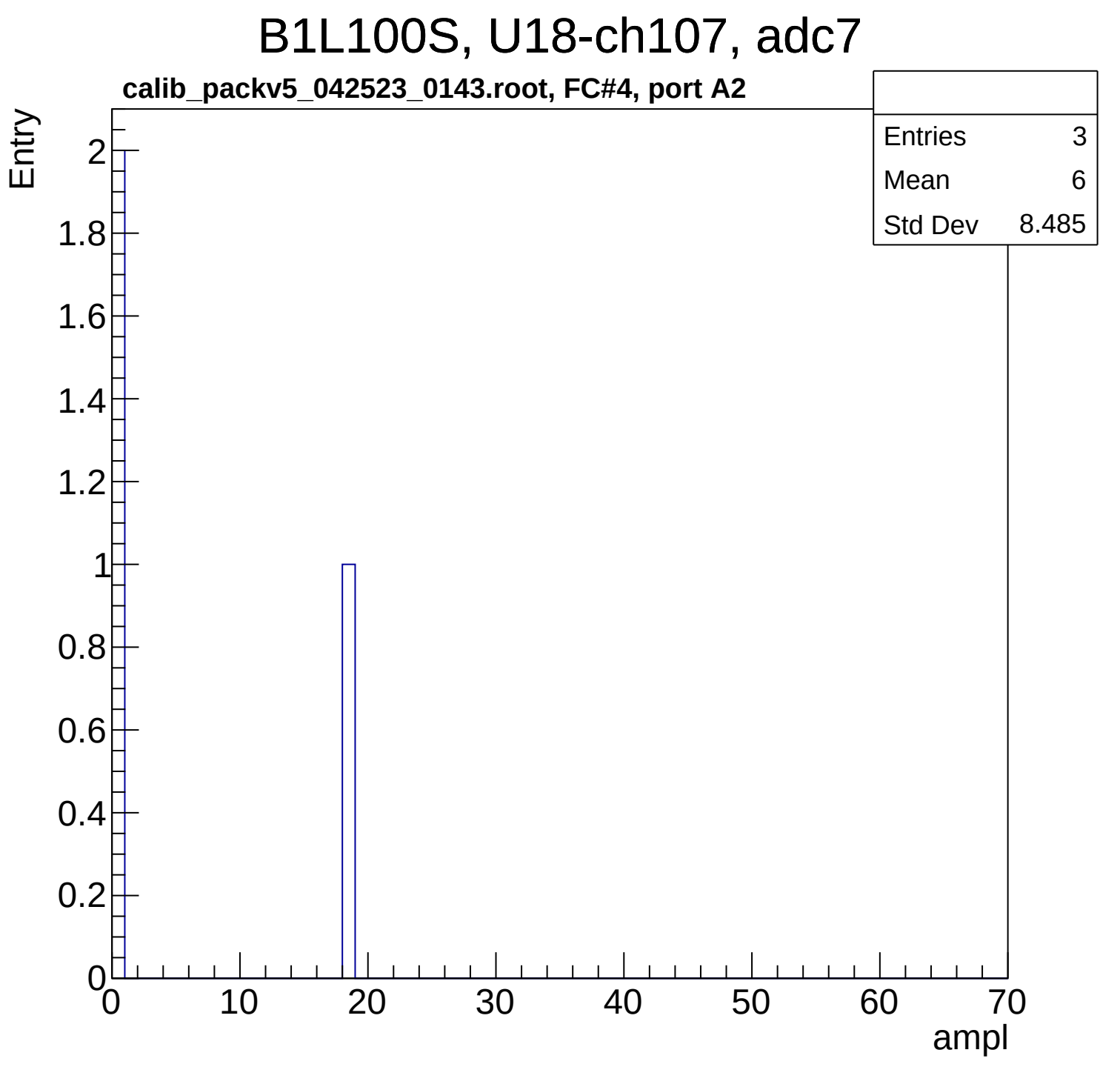

B1L100S, U18-ch107, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 43.87
Std Dev 3.508
Gaus mean : 44.3056
Gaus Width: 3.9946
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

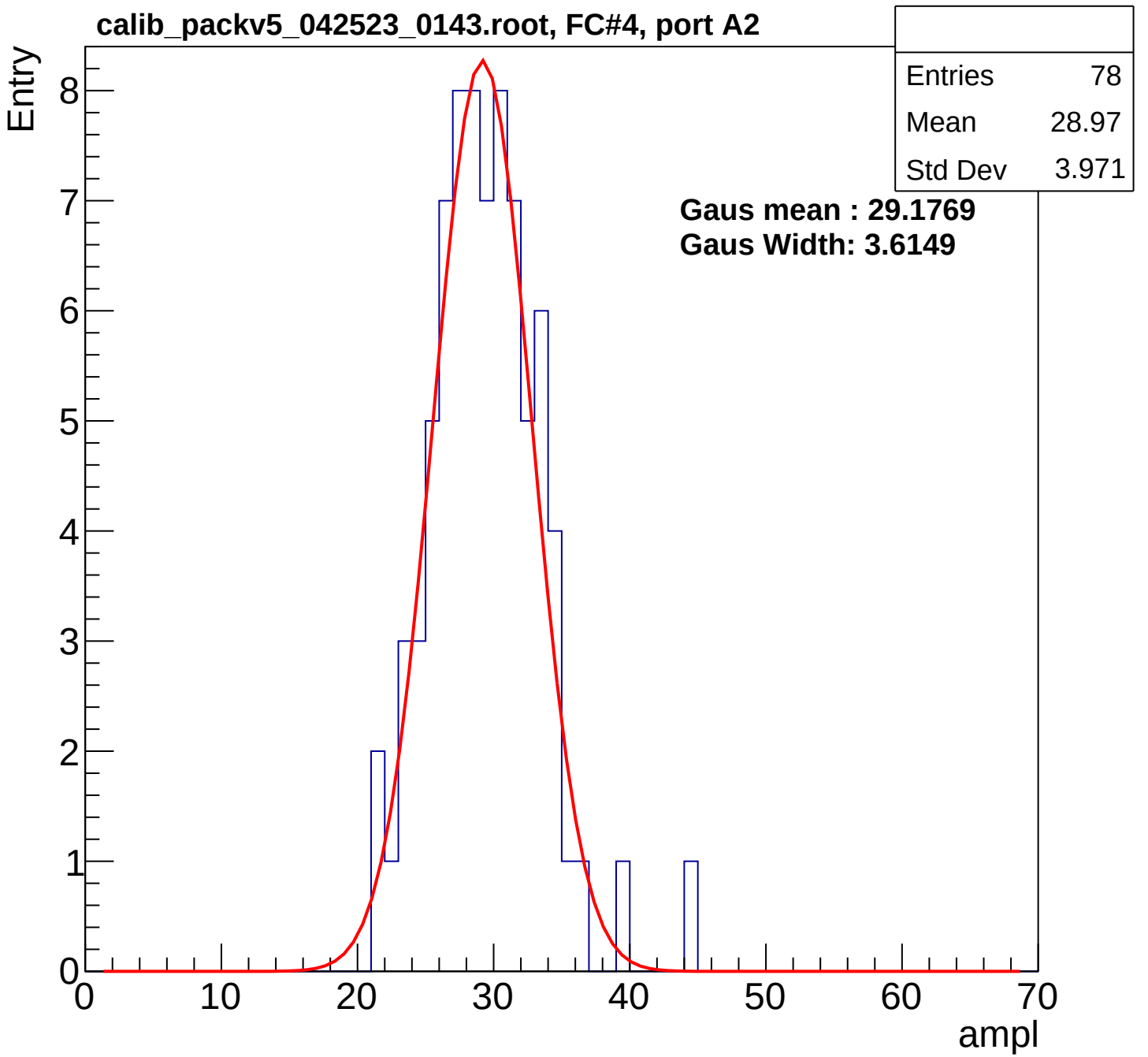

B1L100S, U18-ch107, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 49.26
Std Dev 3.868
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

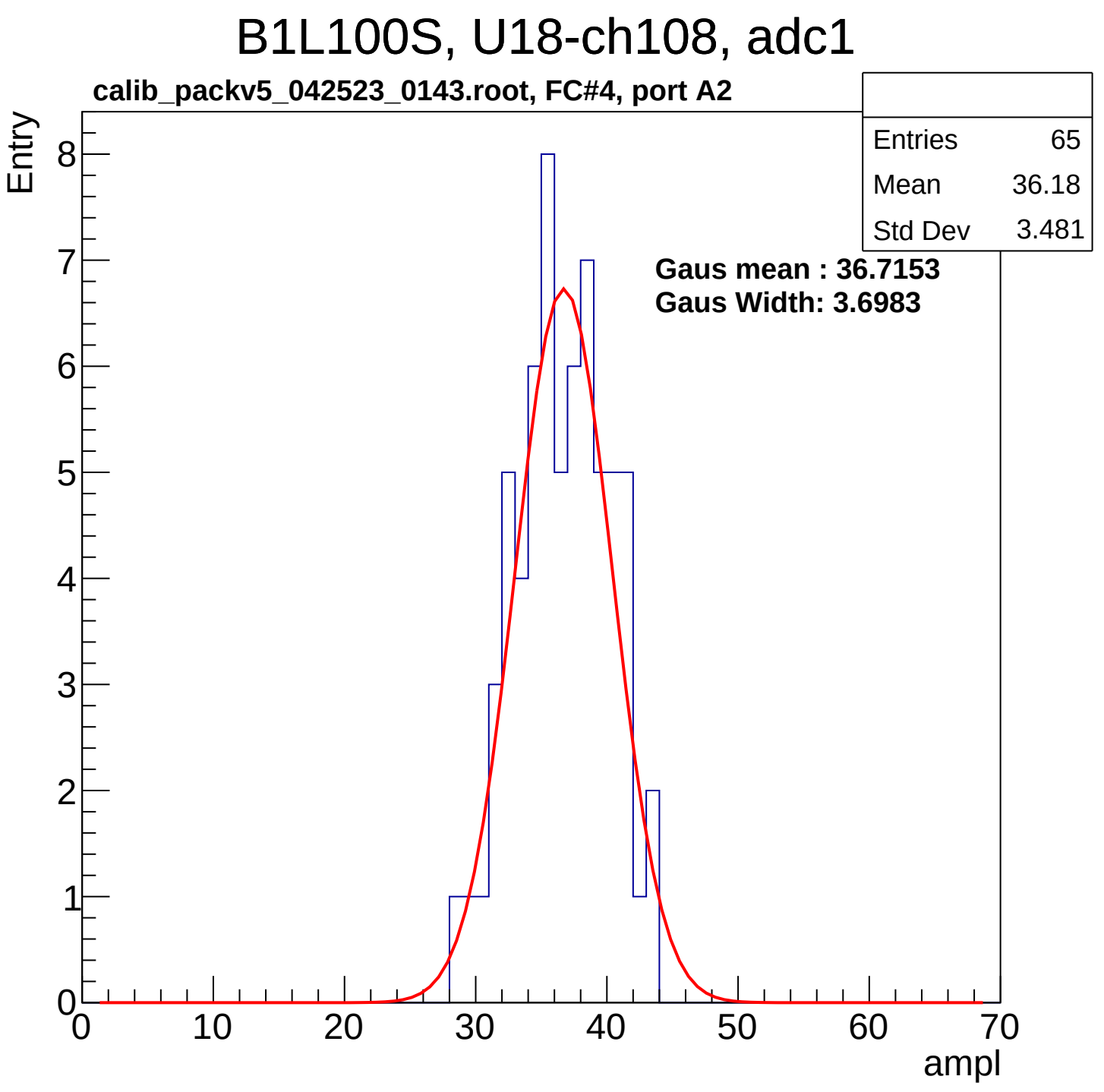

B1L100S, U18-ch107, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 55.41
Std Dev 3.918
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

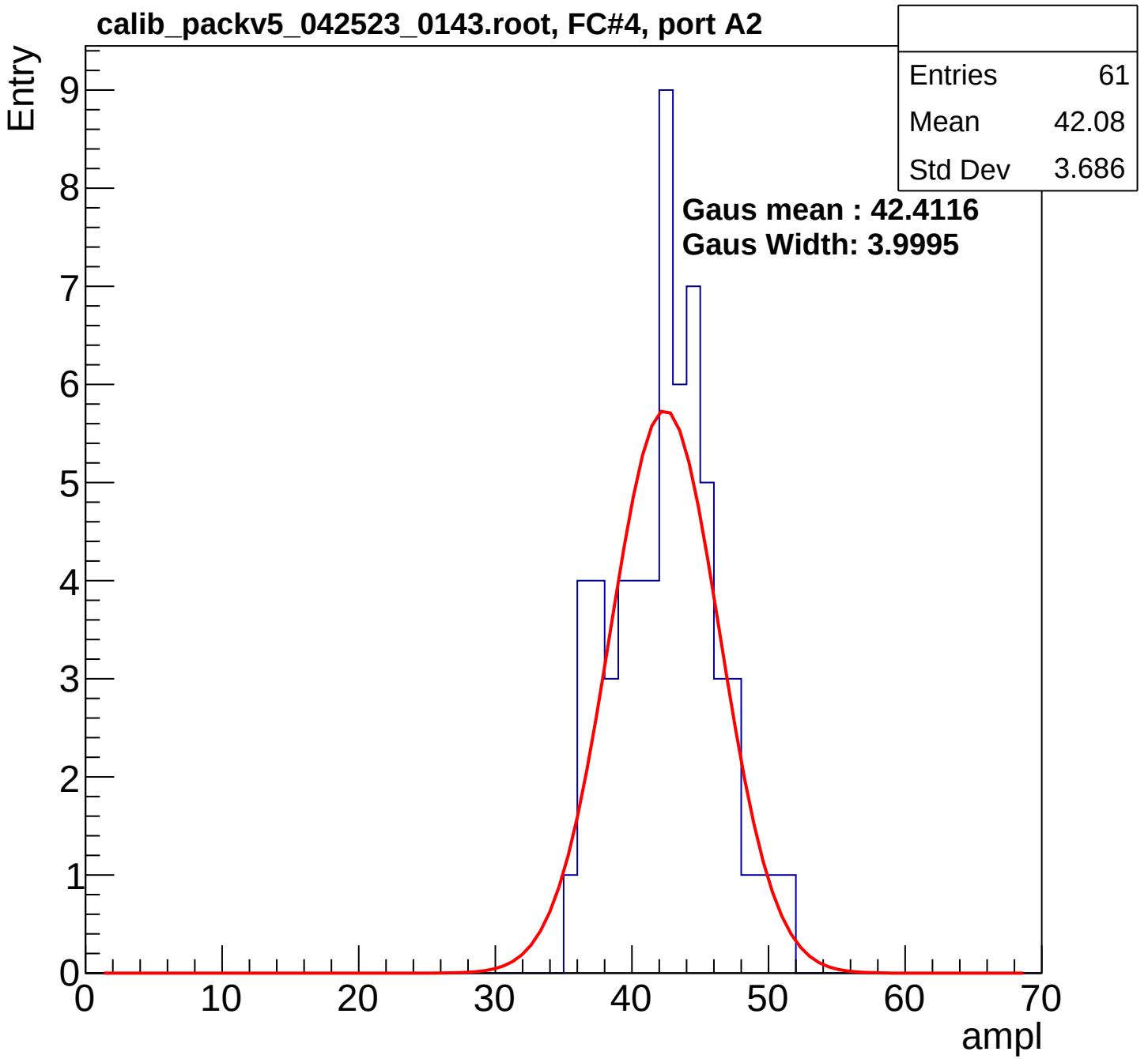

B1L100S, U18-ch107, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 58.76
Std Dev 9.039
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

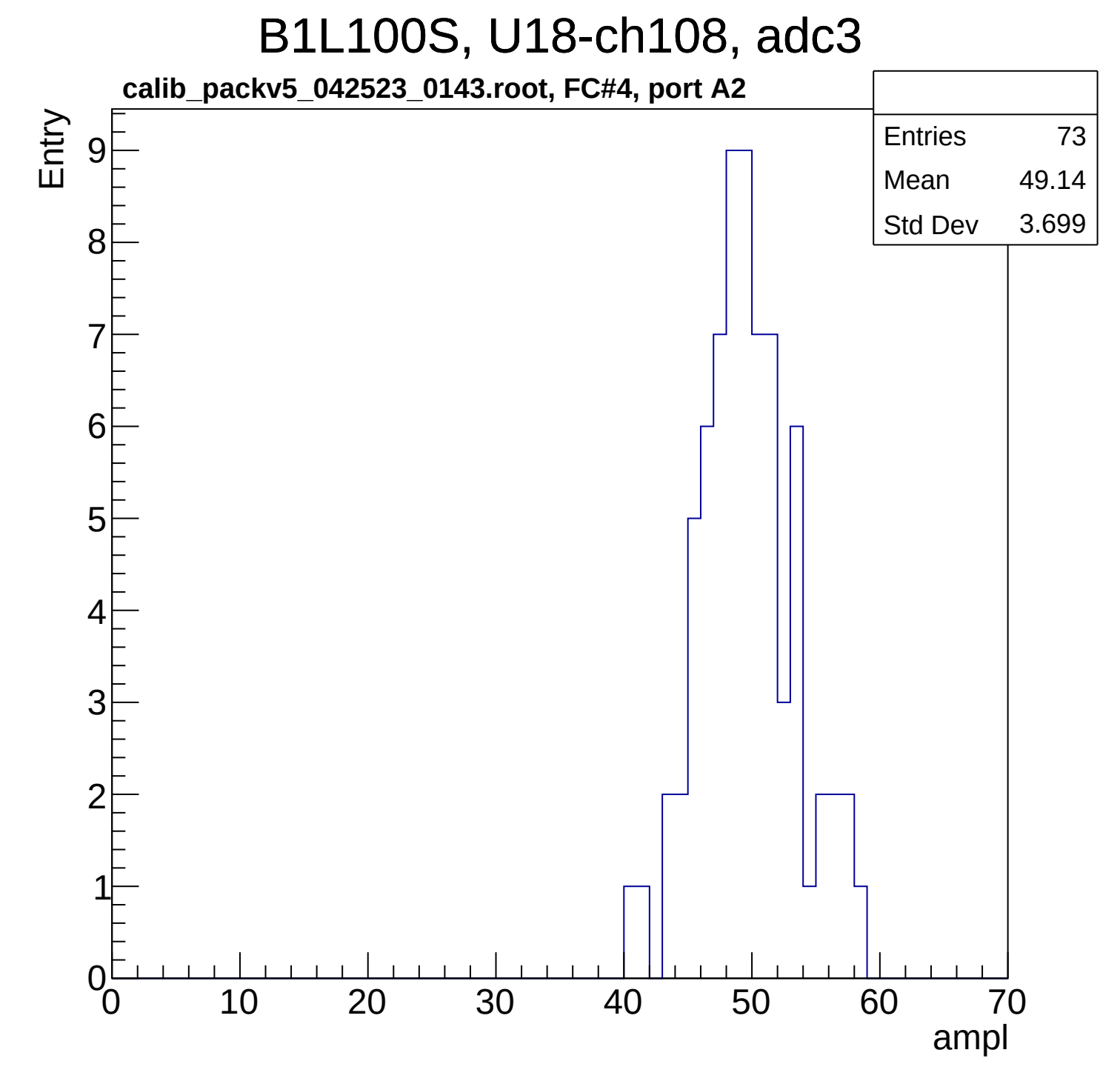

B1L100S, U18-ch107, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 62
Std Dev 1
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

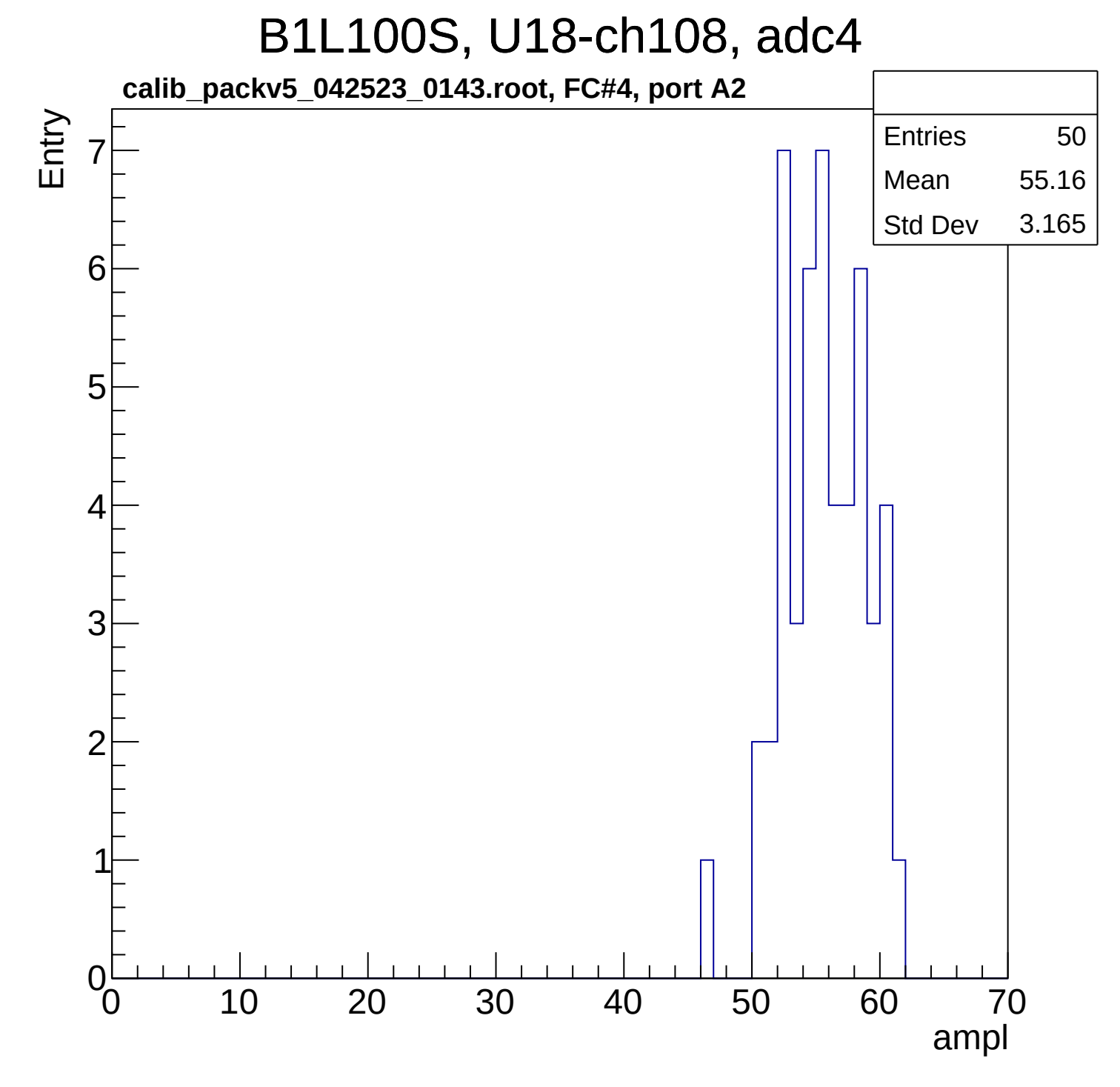

B1L100S, U18-ch107, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 6
Std Dev 8.485
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

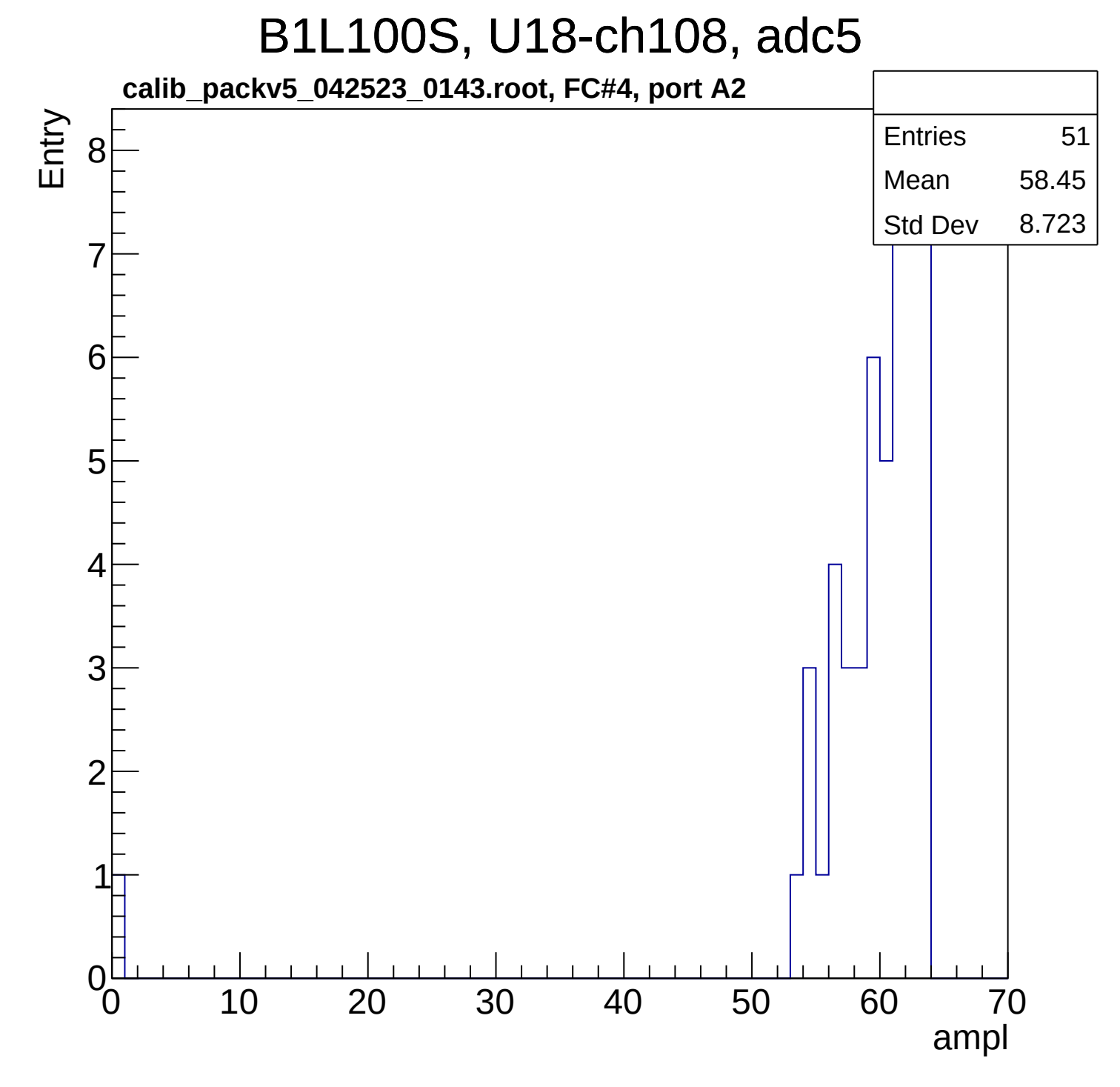

B1L100S, U18-ch108, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 28.97
Std Dev 3.971
Gaus mean : 29.1769
Gaus Width: 3.6149
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

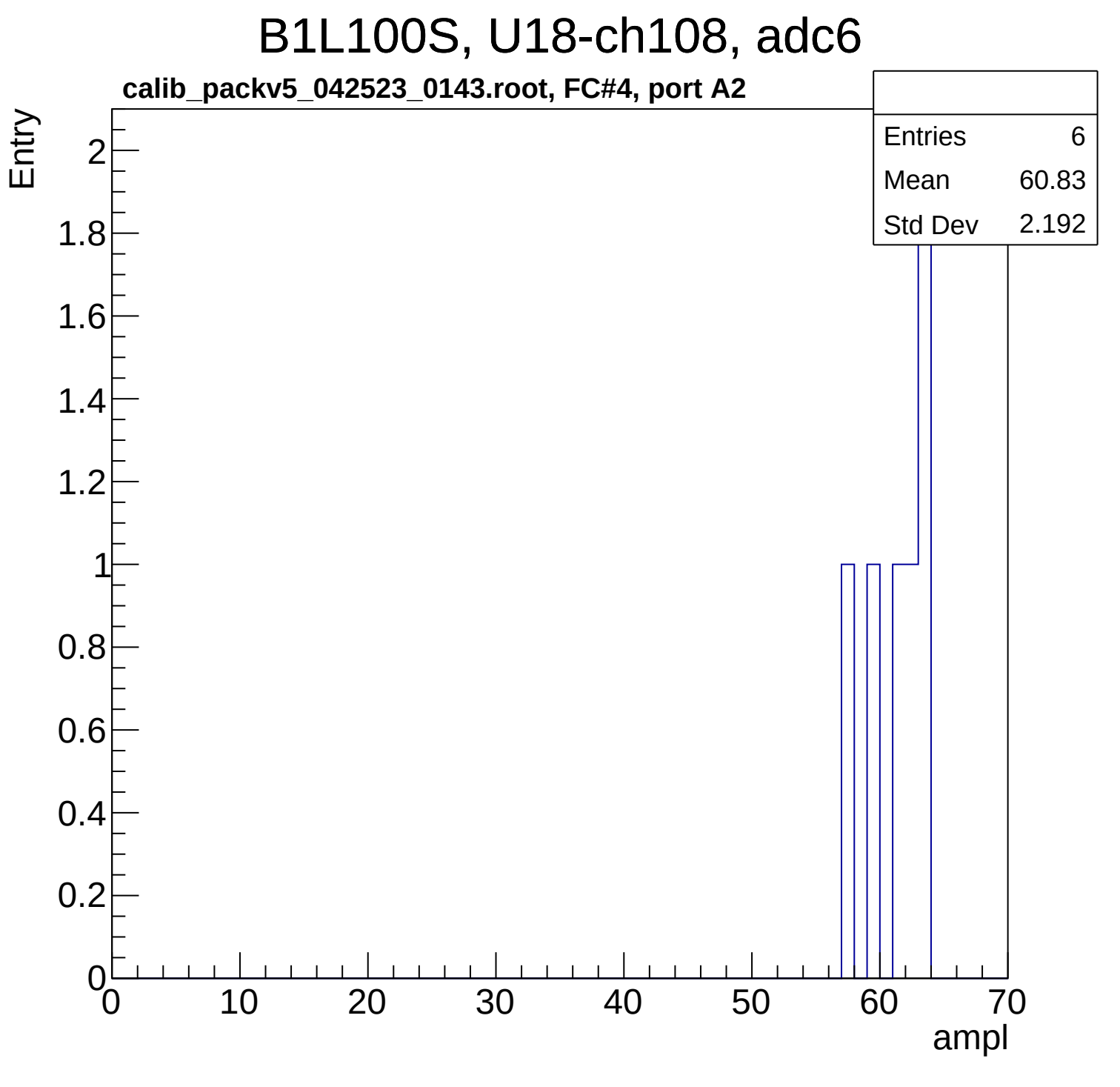

B1L100S, U18-ch108, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 36.18
Std Dev 3.481
Gaus mean : 36.7153
Gaus Width: 3.6983
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

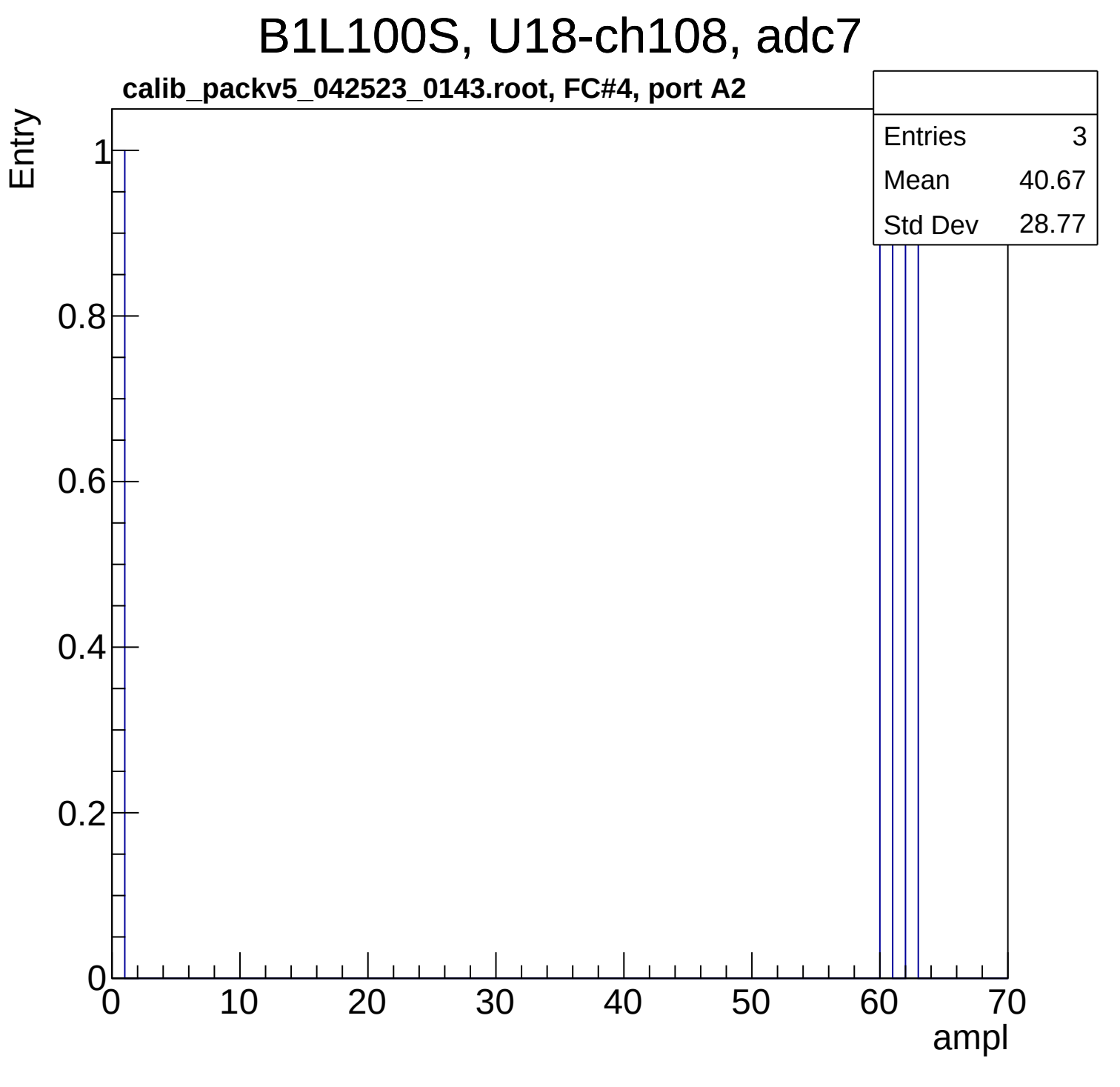

B1L100S, U18-ch108, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 42.08
Std Dev 3.686
Gaus mean : 42.4116
Gaus Width: 3.9995
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

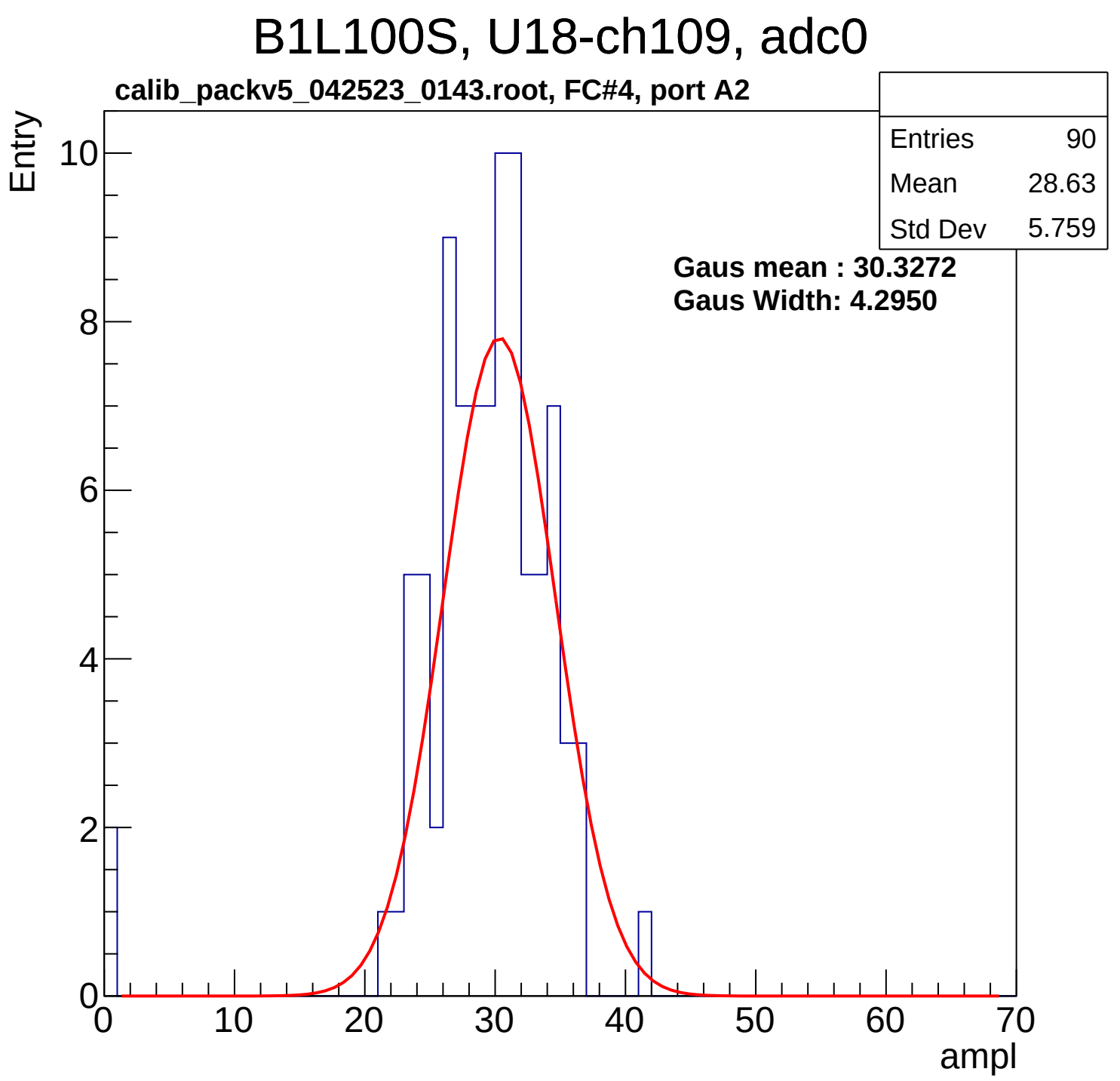

B1L100S, U18-ch108, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 49.14
Std Dev 3.699
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

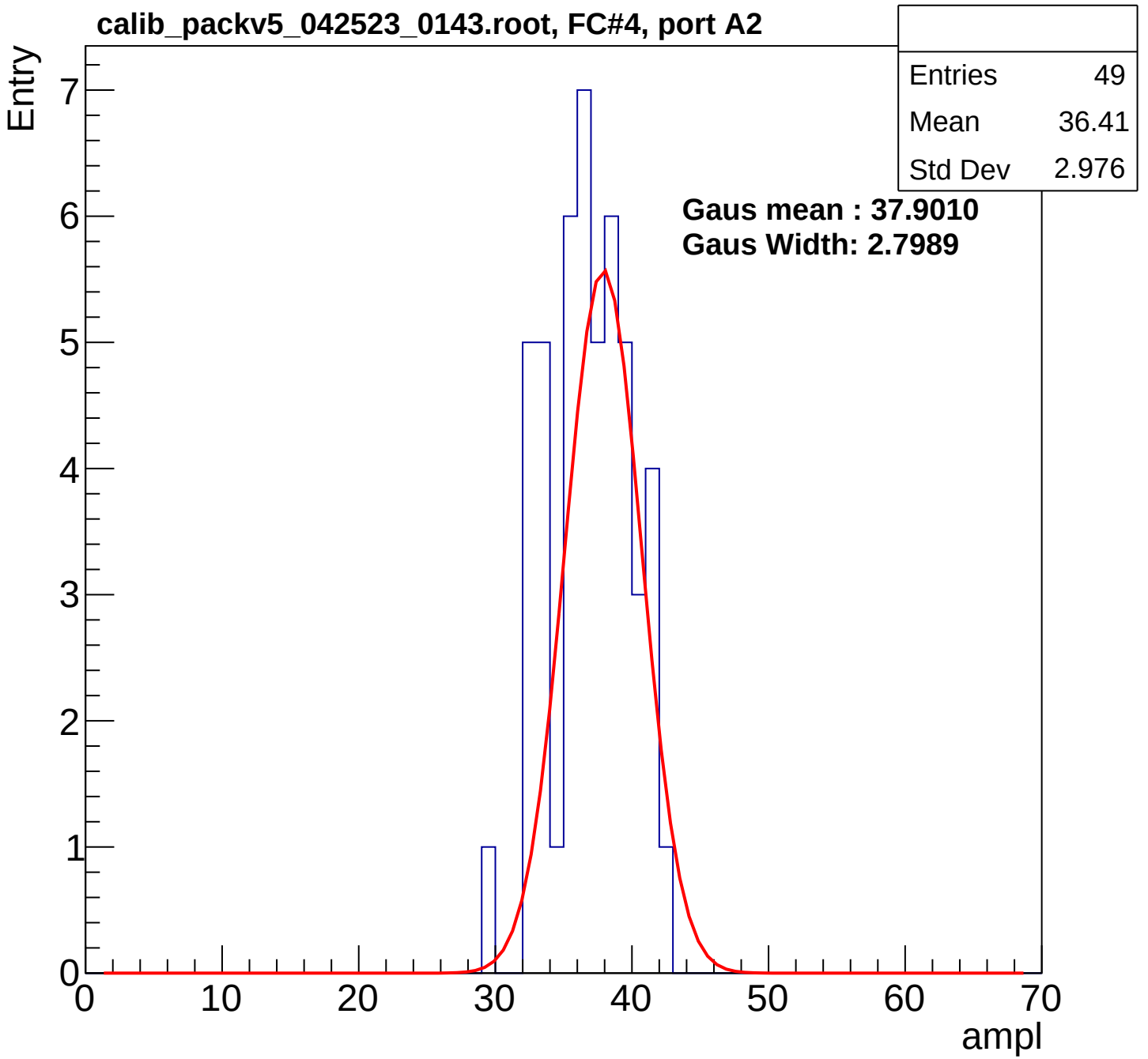

B1L100S, U18-ch108, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 55.16
Std Dev 3.165
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

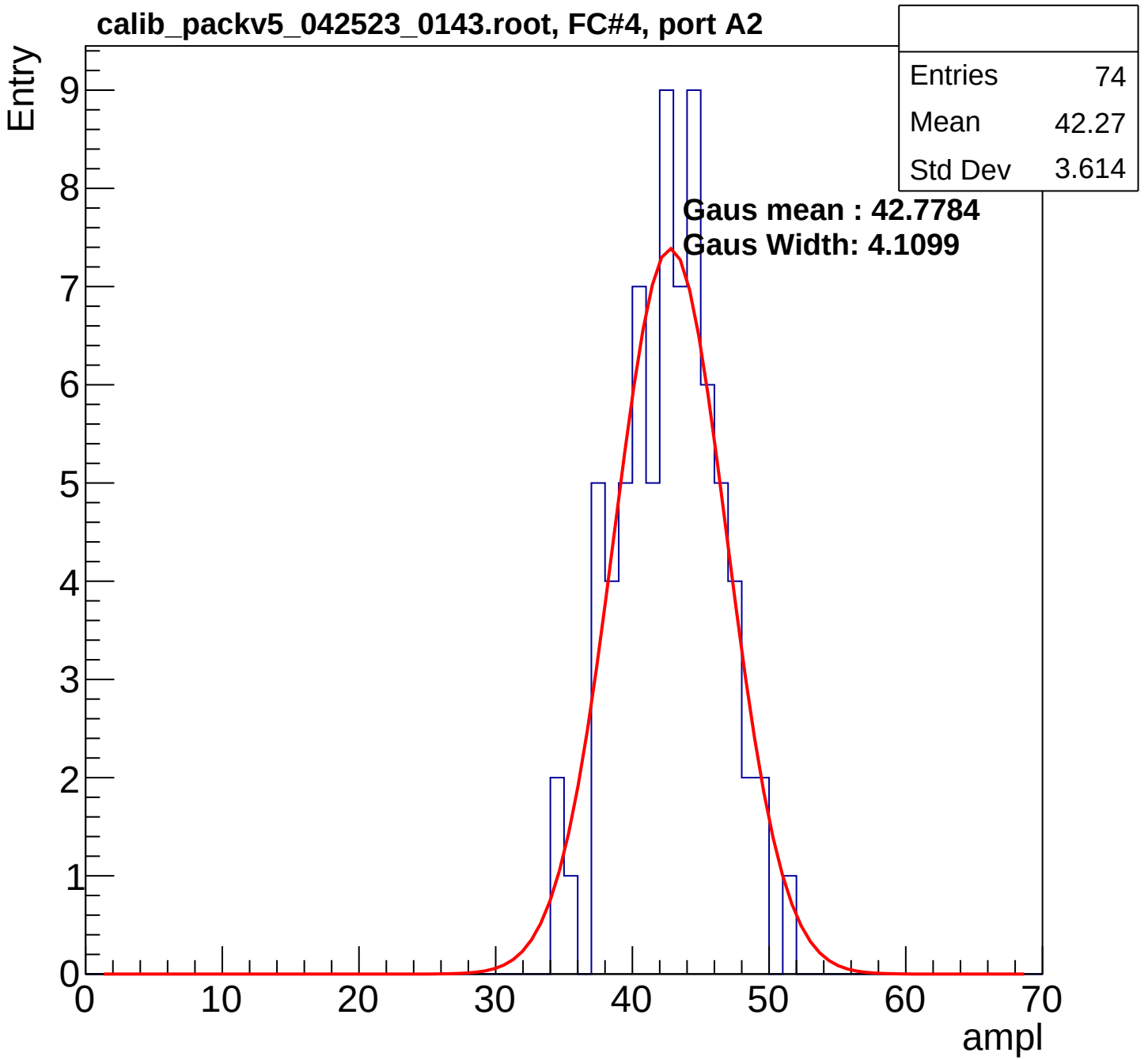

B1L100S, U18-ch108, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 58.45
Std Dev 8.723
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

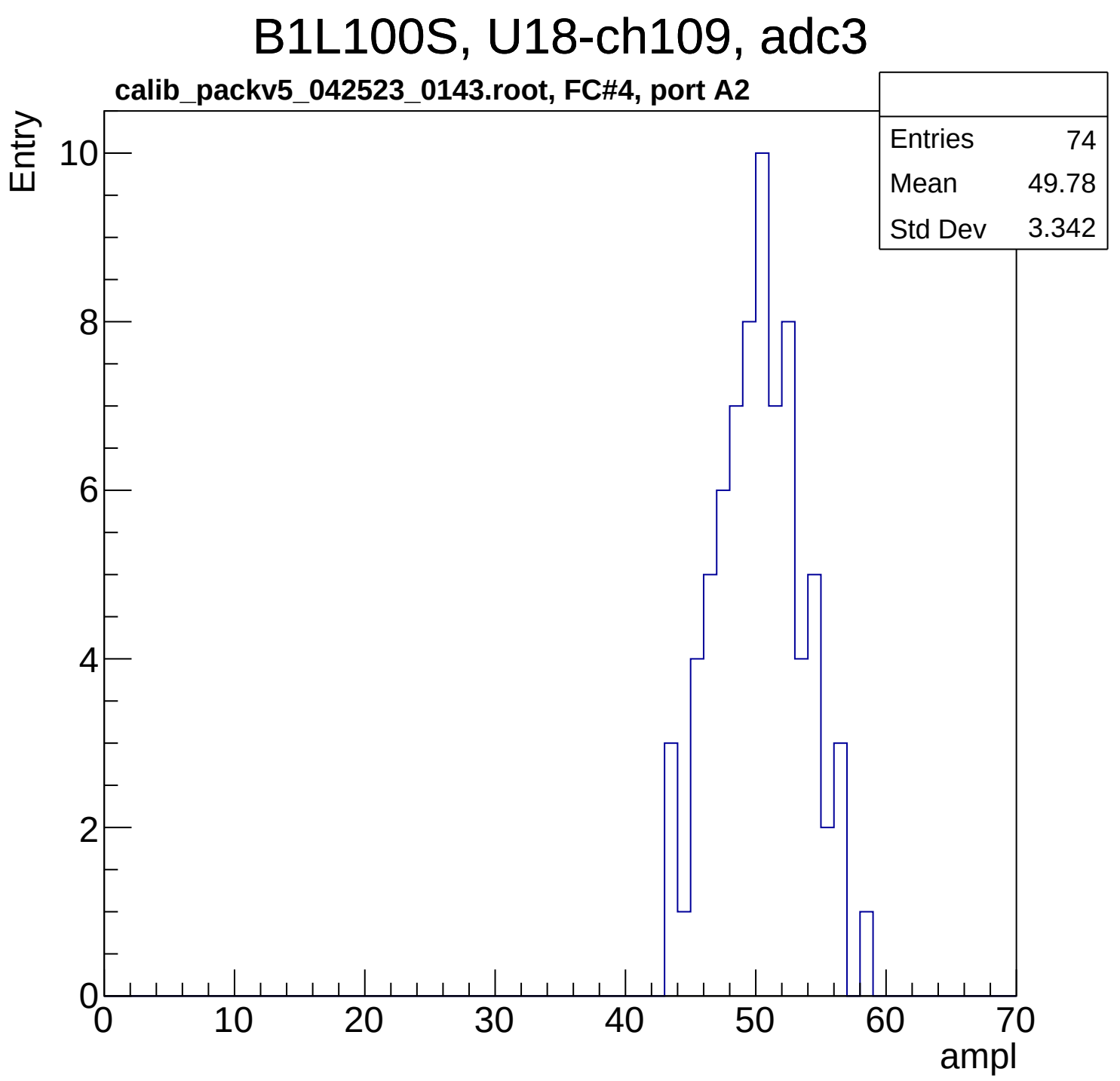

B1L100S, U18-ch108, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 60.83
Std Dev 2.192
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

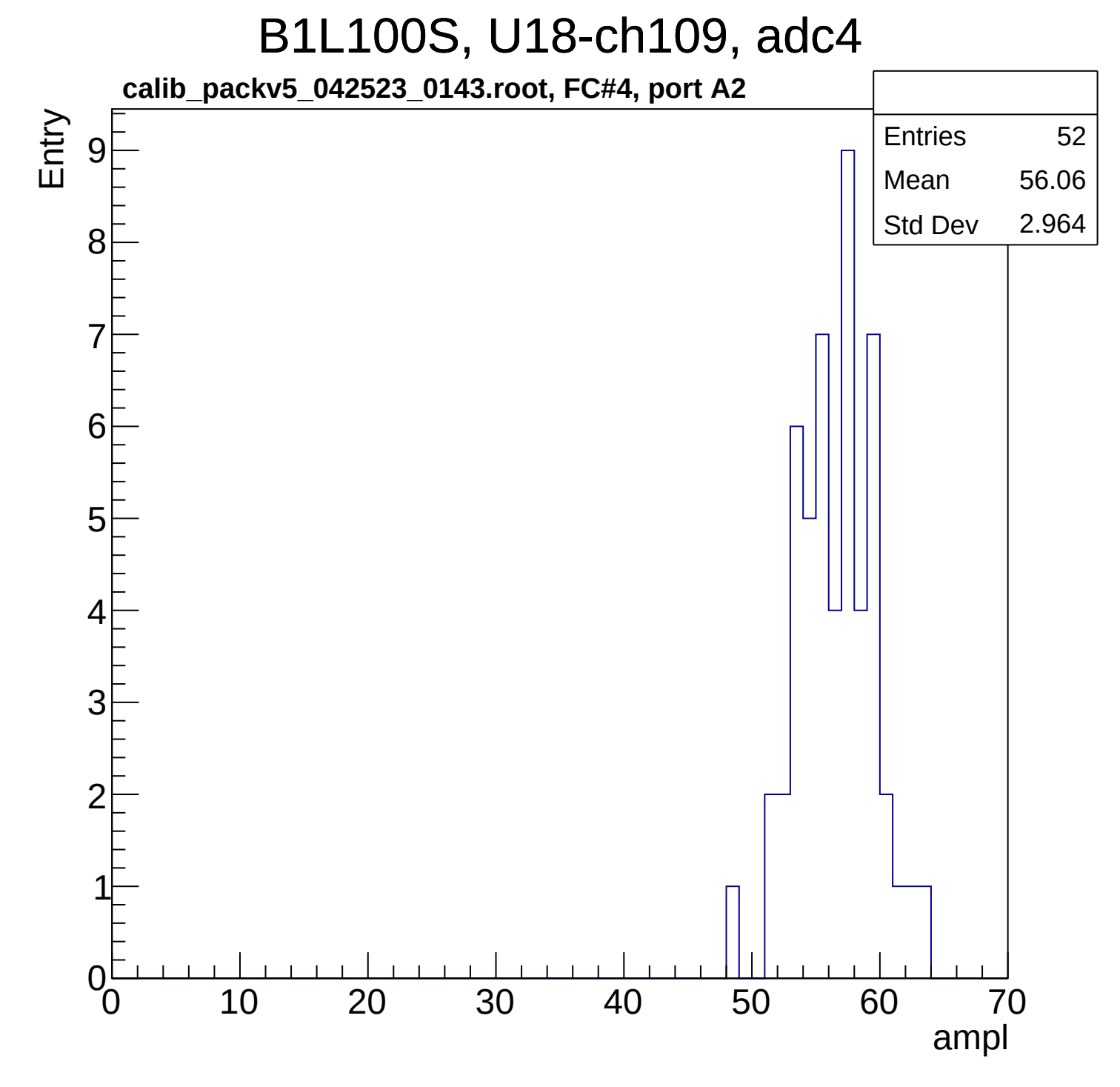

B1L100S, U18-ch108, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 40.67
Std Dev 28.77
Entry
ampl
0
0.2
0.4
0.6
0.8
1
0
10
20
30
40
50
60
70

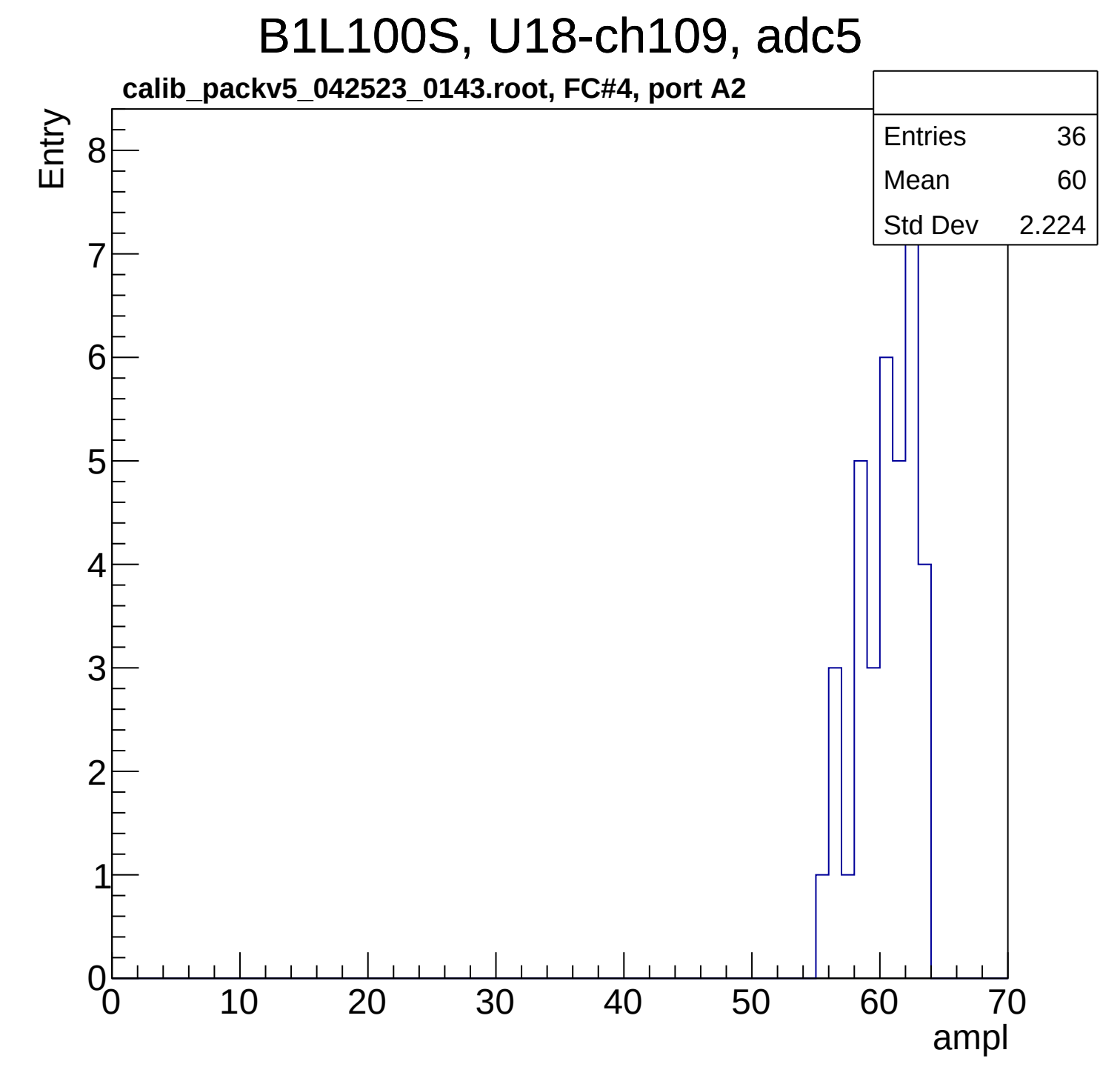

B1L100S, U18-ch109, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 90
Mean 28.63
Std Dev 5.759
Gaus mean : 30.3272
Gaus Width: 4.2950
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

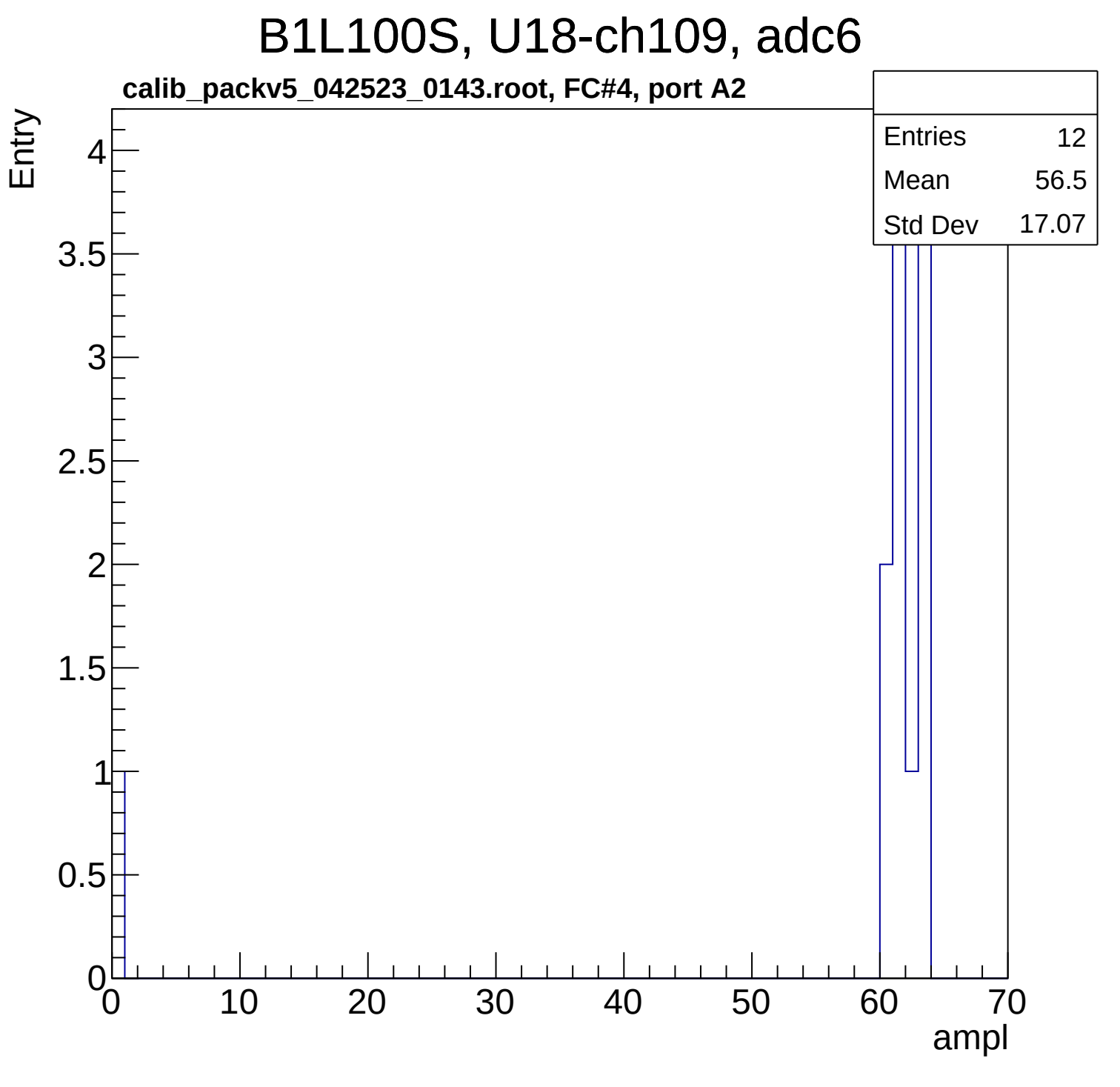

B1L100S, U18-ch109, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 36.41
Std Dev 2.976
Gaus mean : 37.9010
Gaus Width: 2.7989
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

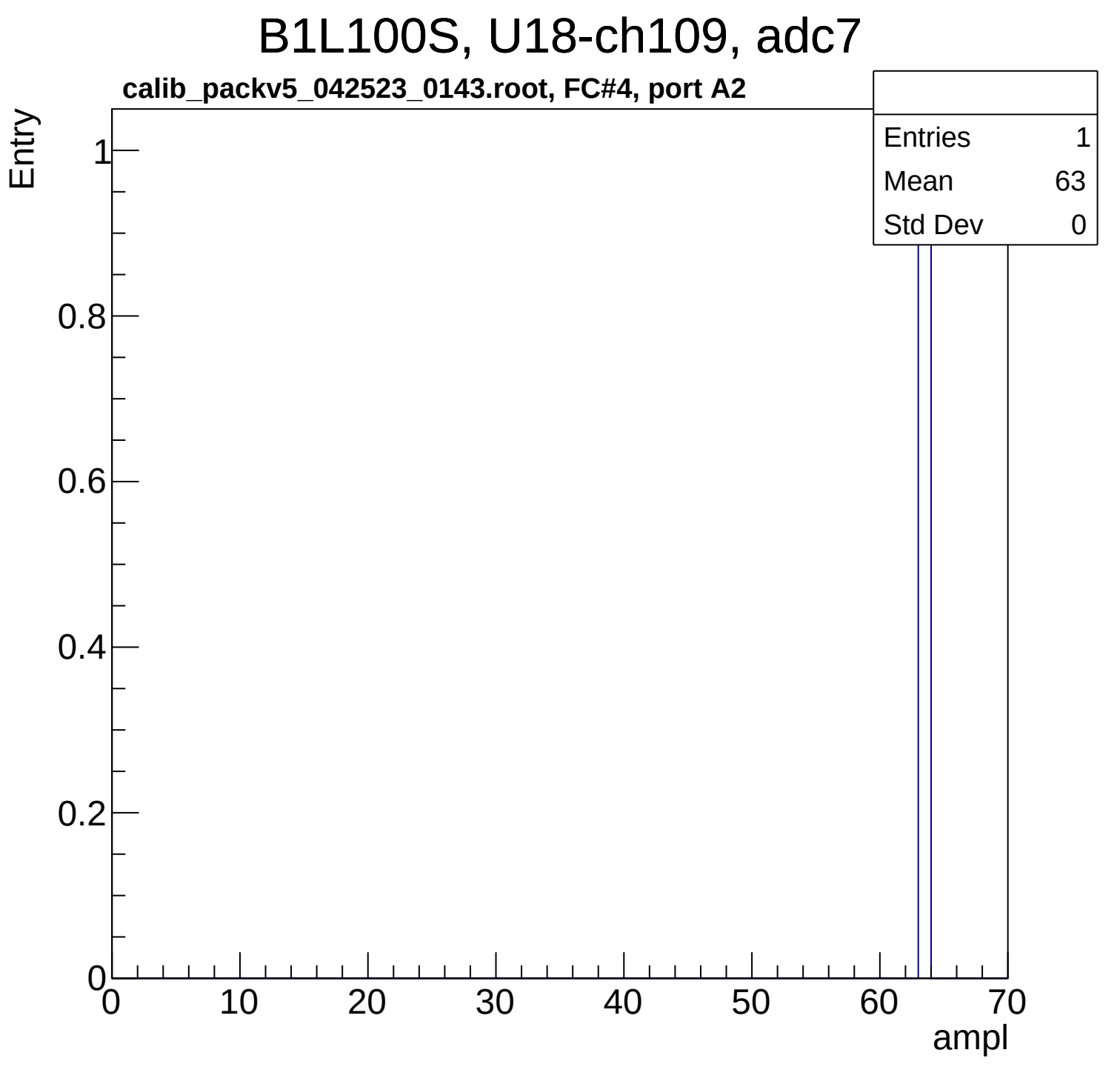

B1L100S, U18-ch109, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 42.27
Std Dev 3.614
Gaus mean : 42.7784
Gaus Width: 4.1099
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

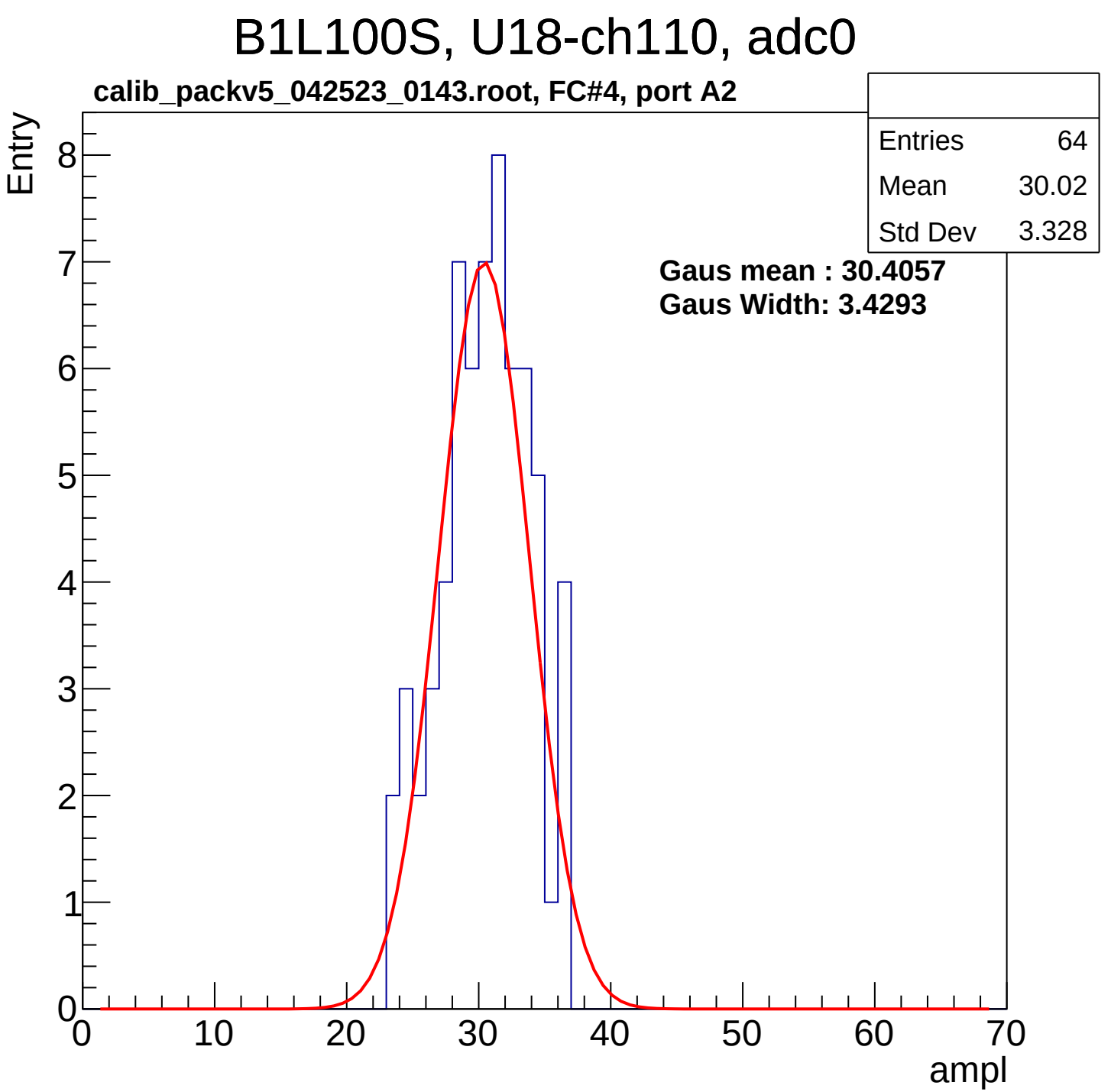

B1L100S, U18-ch109, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 49.78
Std Dev 3.342
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

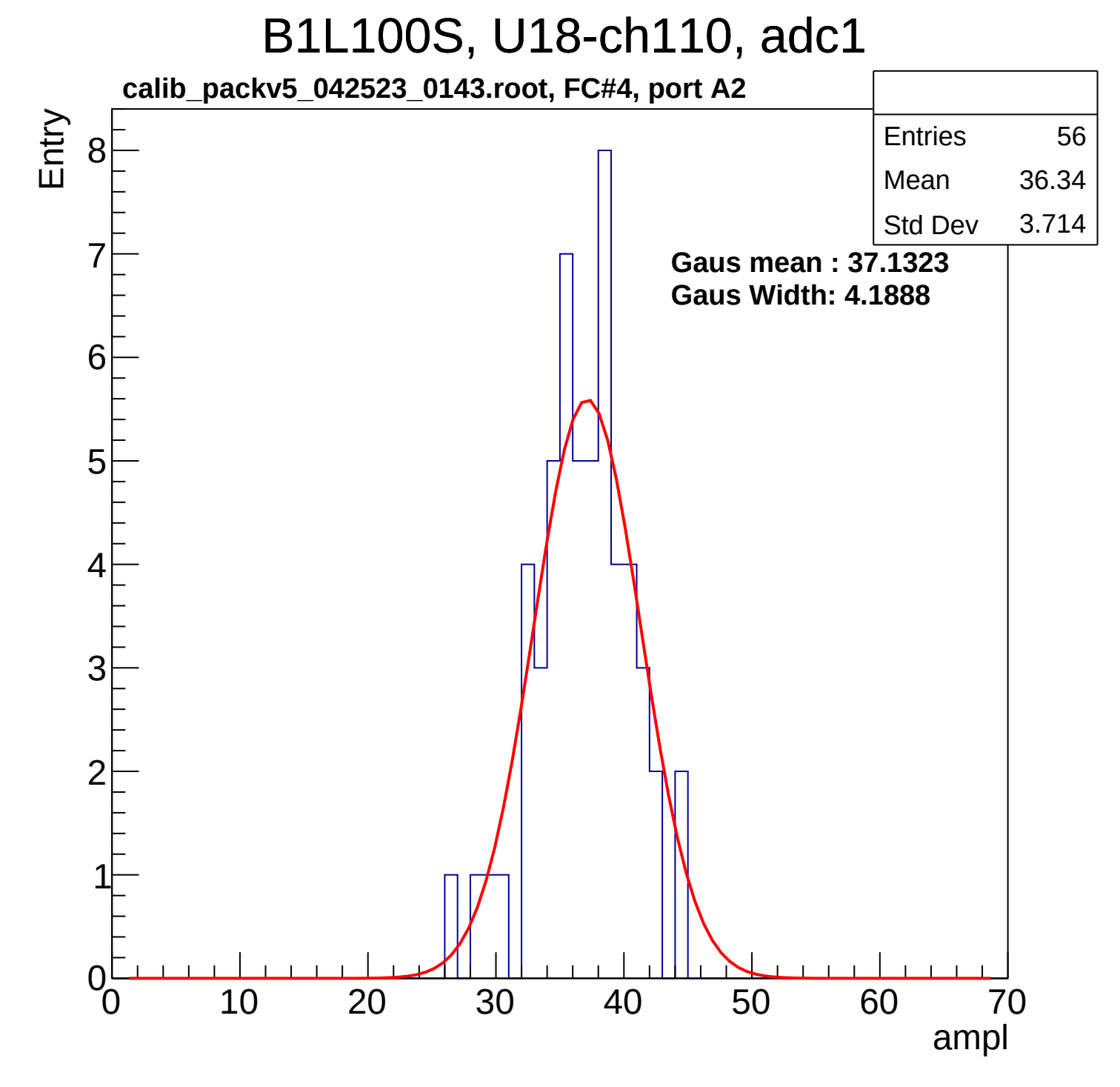

B1L100S, U18-ch109, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 56.06
Std Dev 2.964
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

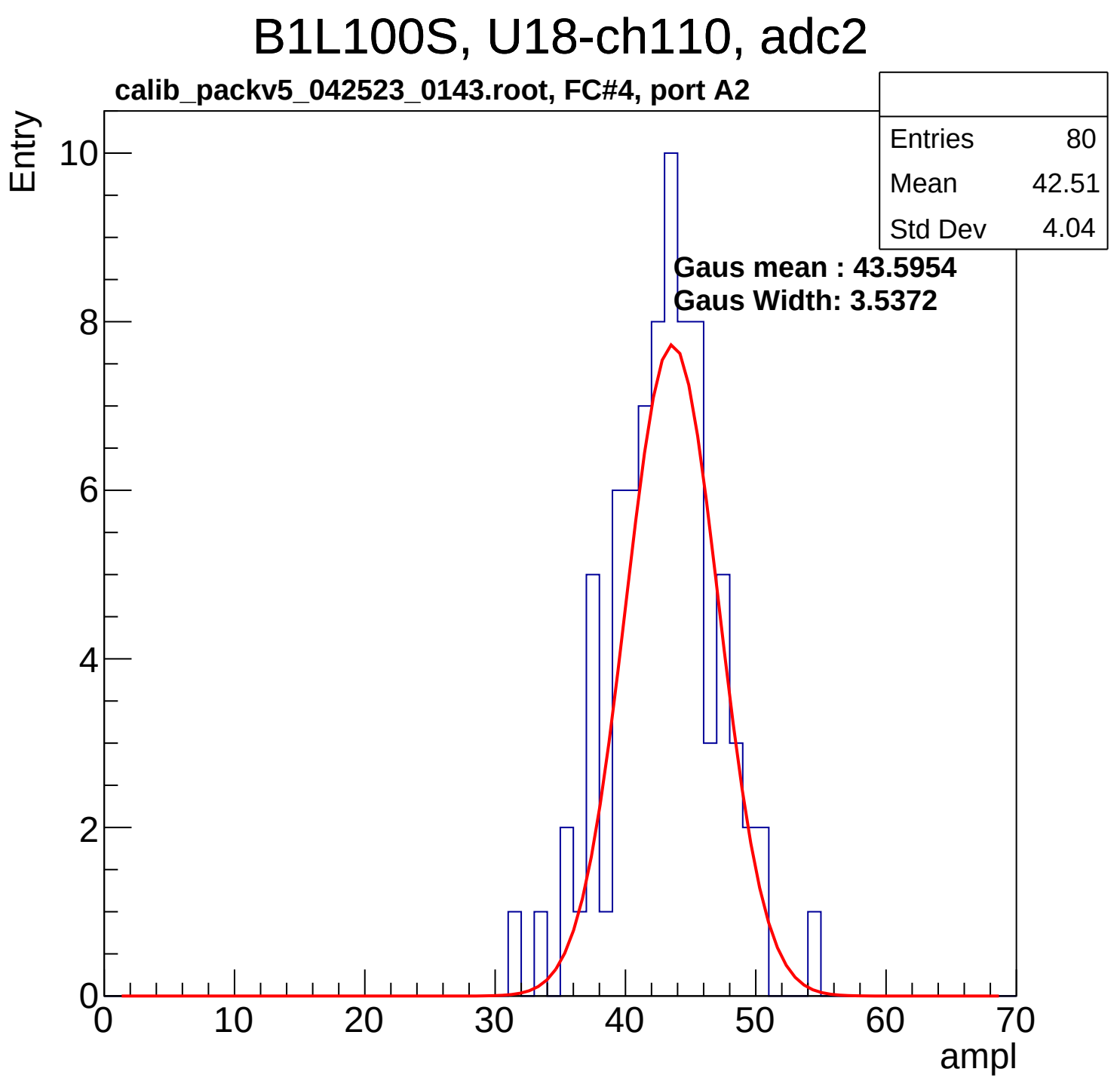

B1L100S, U18-ch109, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 36
Mean 60
Std Dev 2.224
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

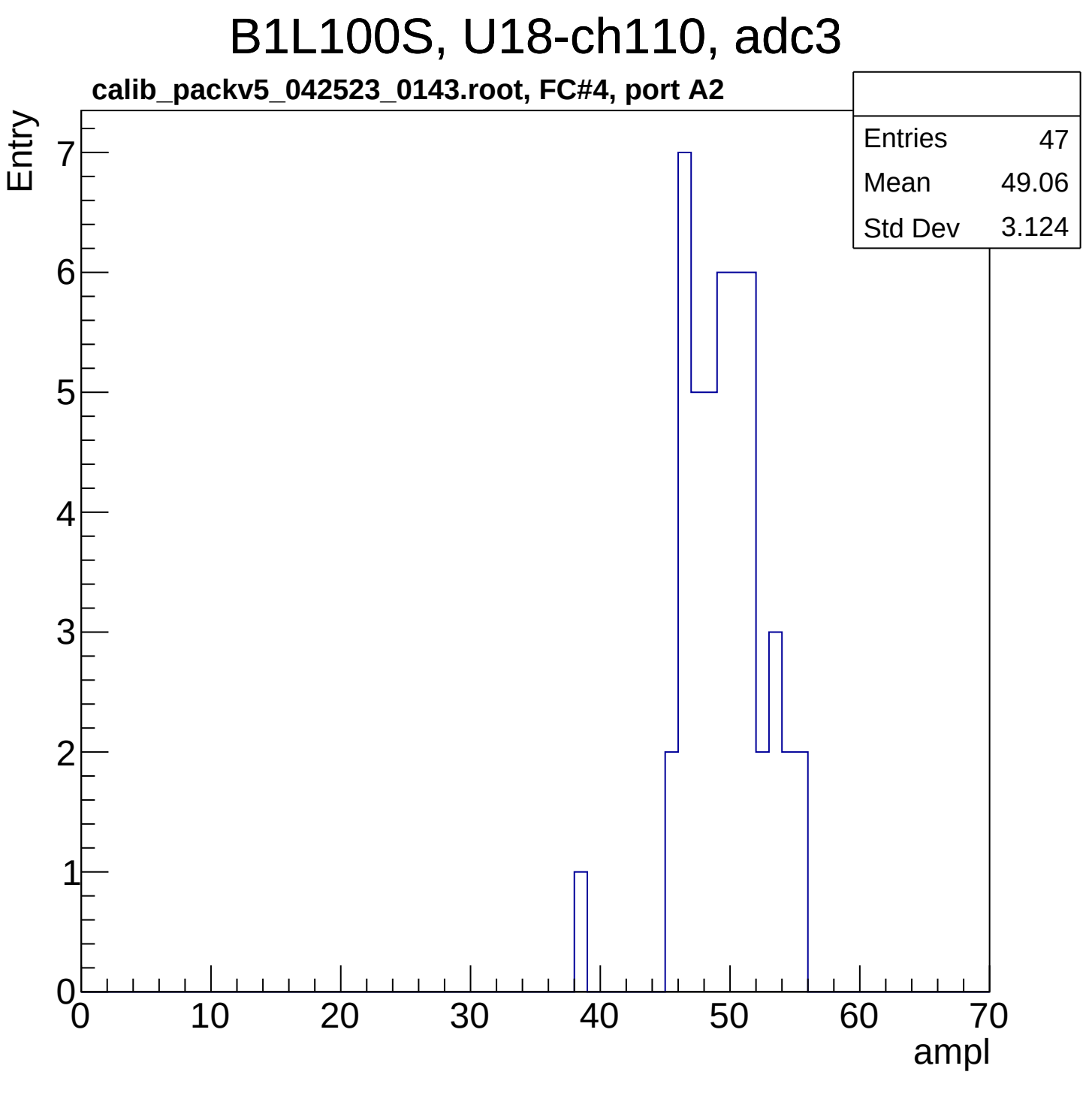

B1L100S, U18-ch109, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 12
Mean 56.5
Std Dev 17.07
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

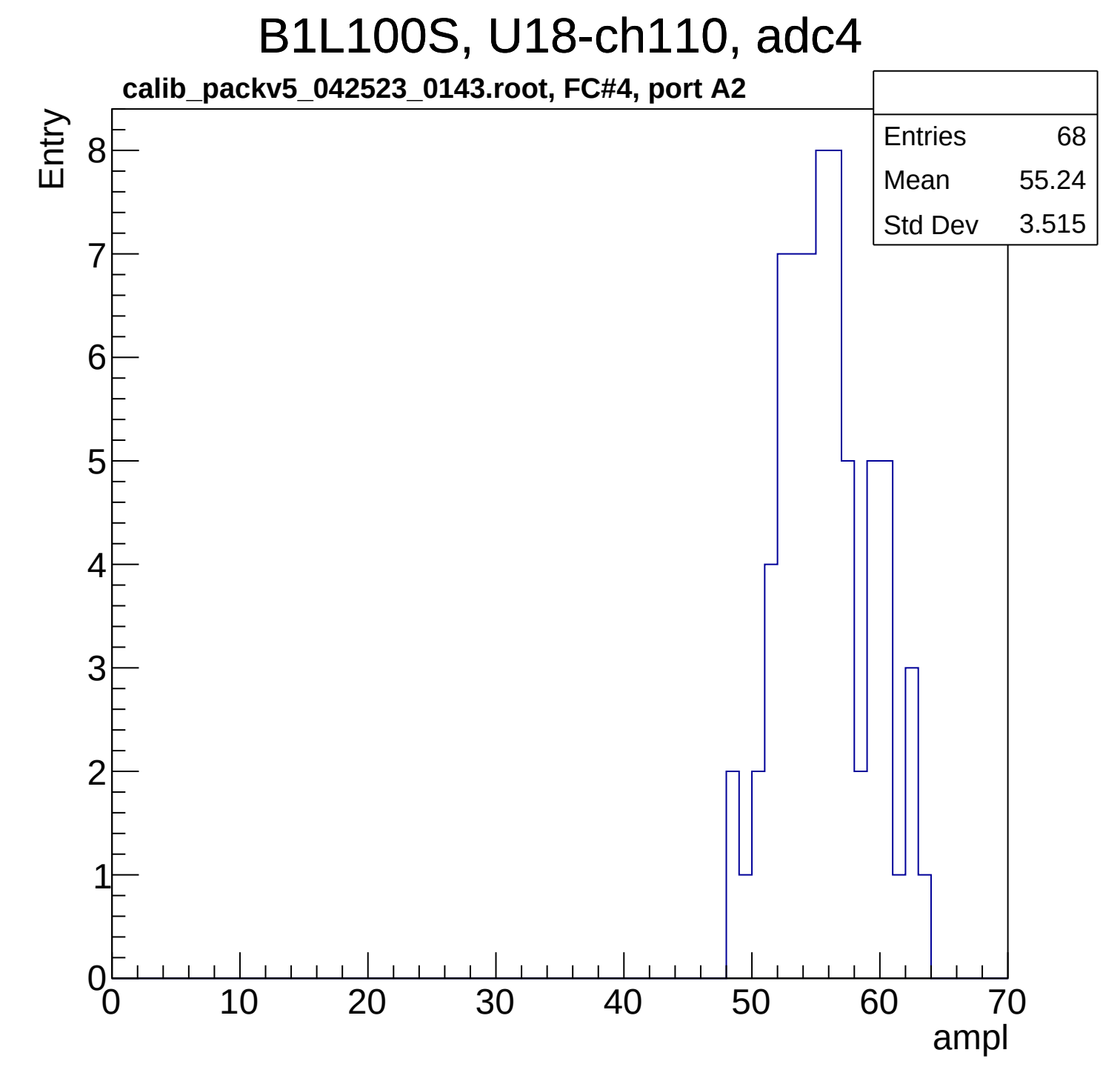

B1L100S, U18-ch109, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 63
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

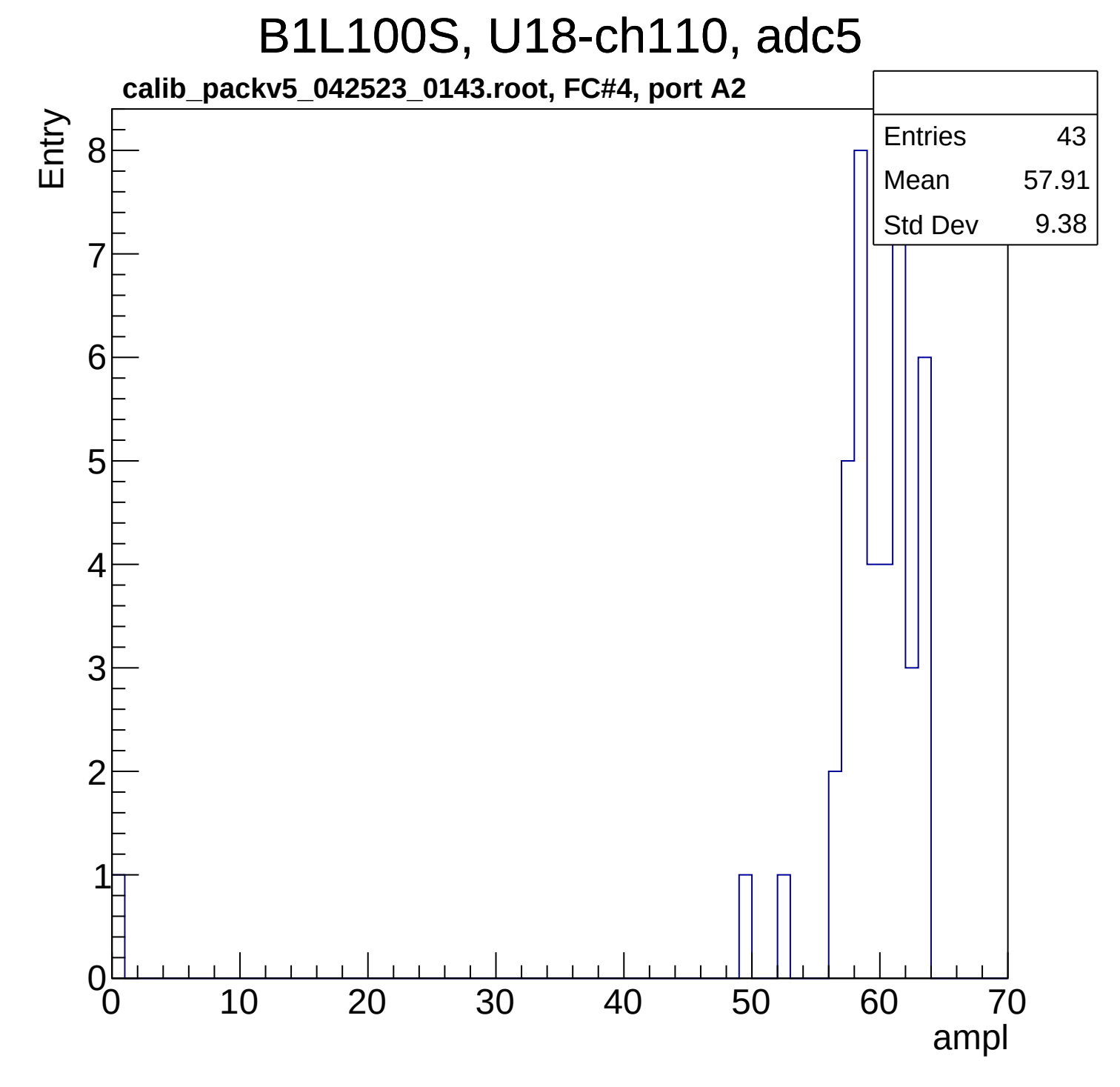

B1L100S, U18-ch110, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 30.02
Std Dev 3.328
Gaus mean : 30.4057
Gaus Width: 3.4293
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

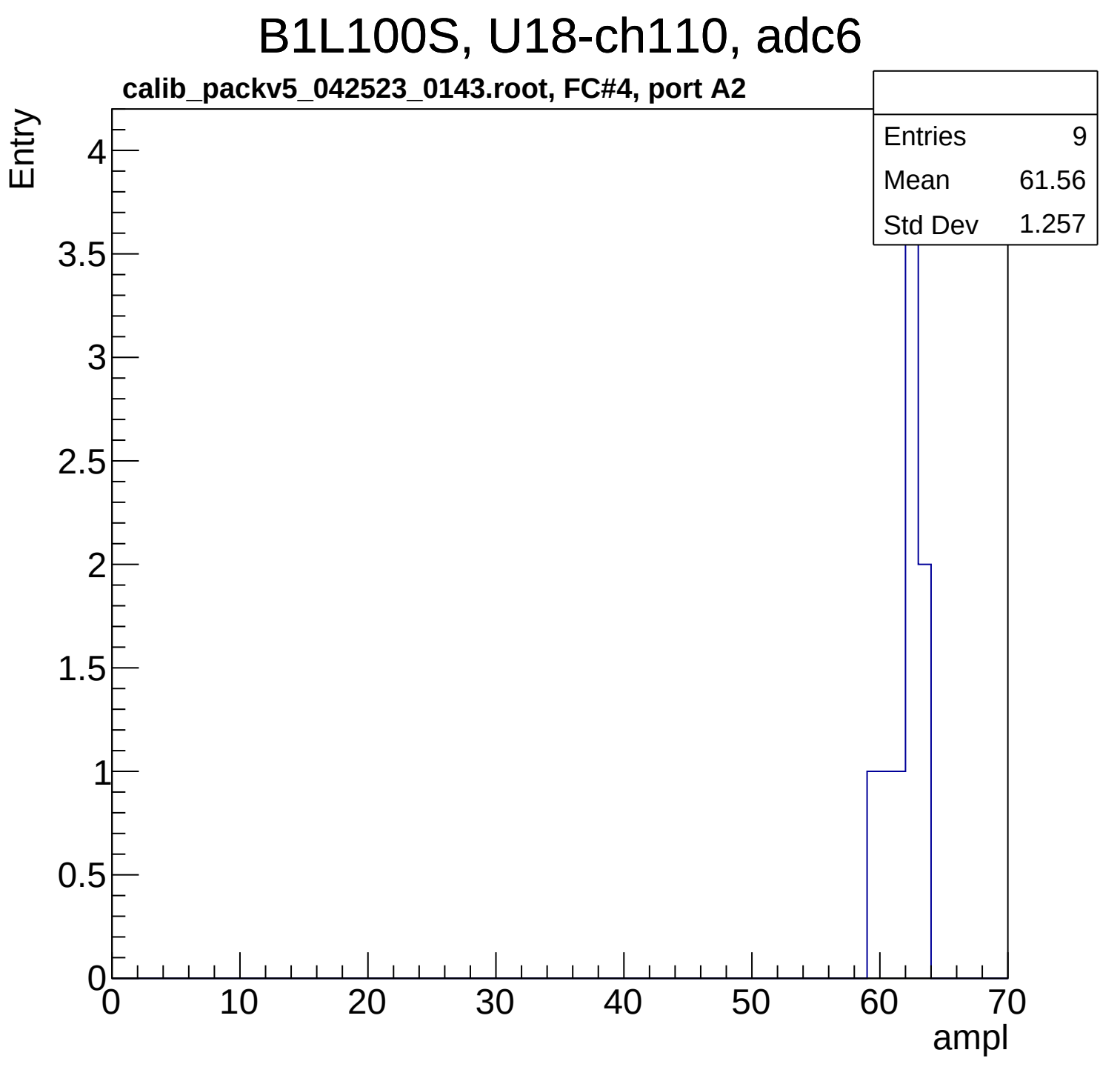

B1L100S, U18-ch110, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 36.34
Std Dev 3.714
Gaus mean : 37.1323
Gaus Width: 4.1888
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

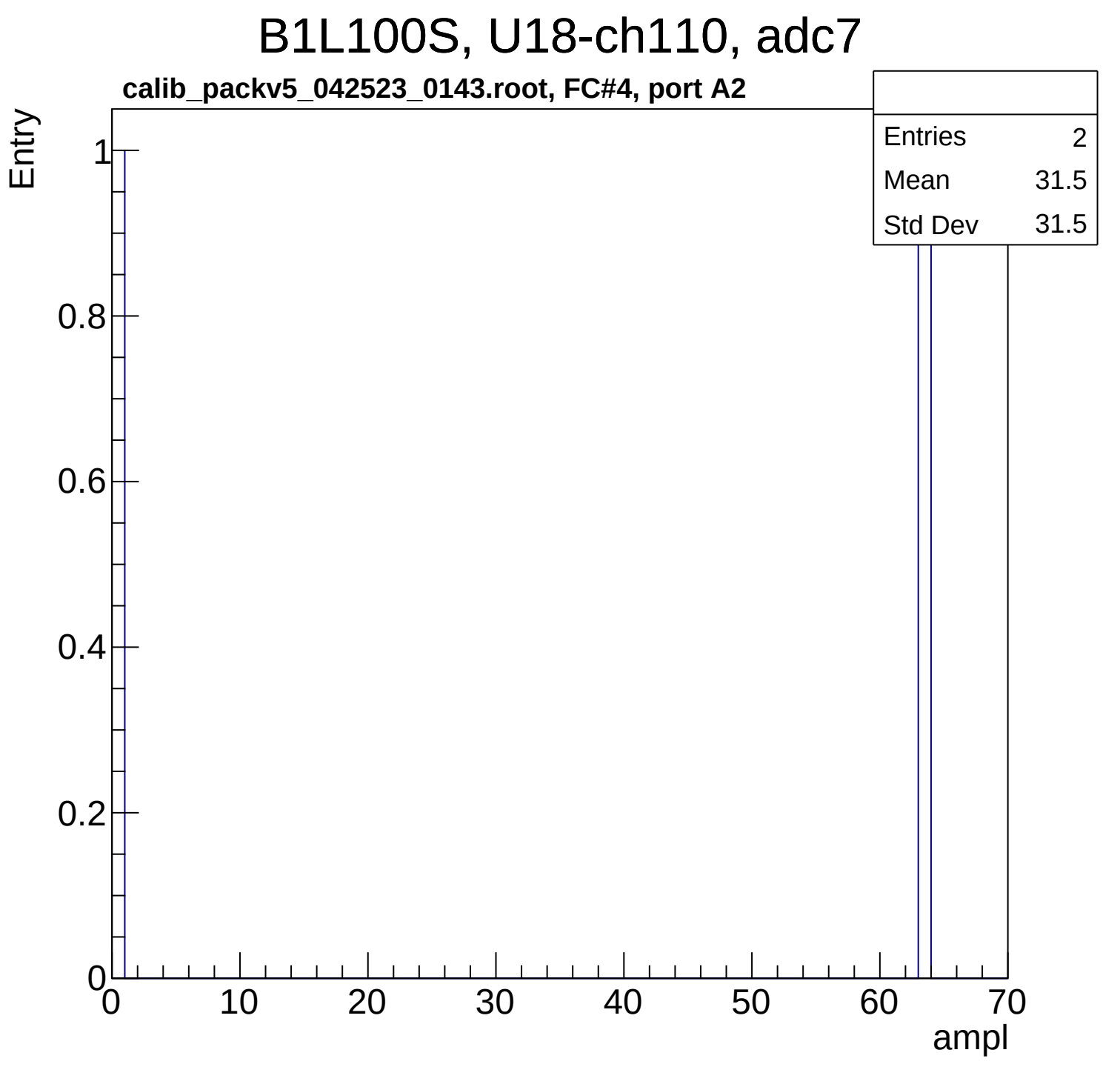

B1L100S, U18-ch110, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 42.51
Std Dev 4.04
Gaus mean : 43.5954
Gaus Width: 3.5372
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

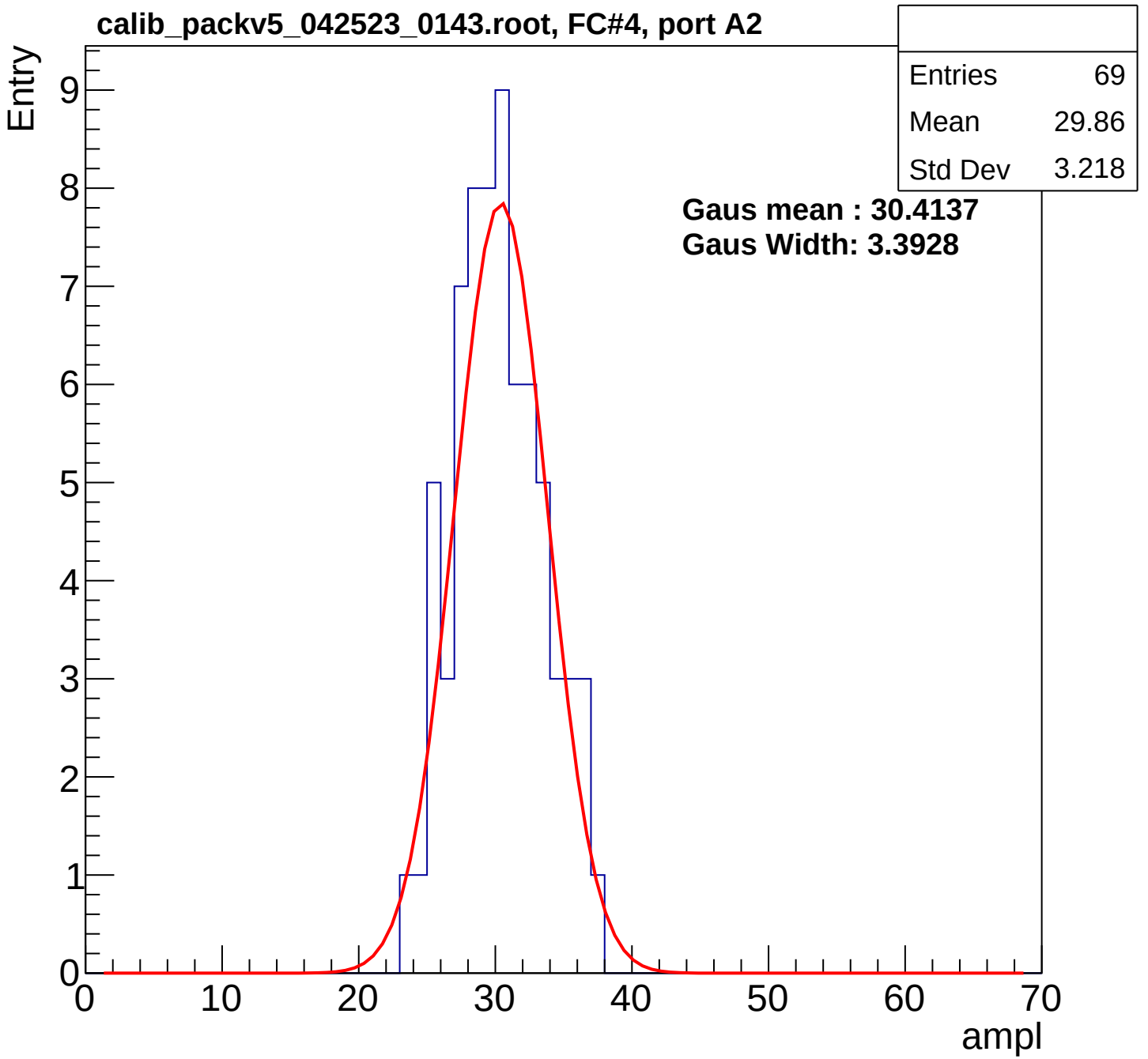

B1L100S, U18-ch110, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 49.06
Std Dev 3.124
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

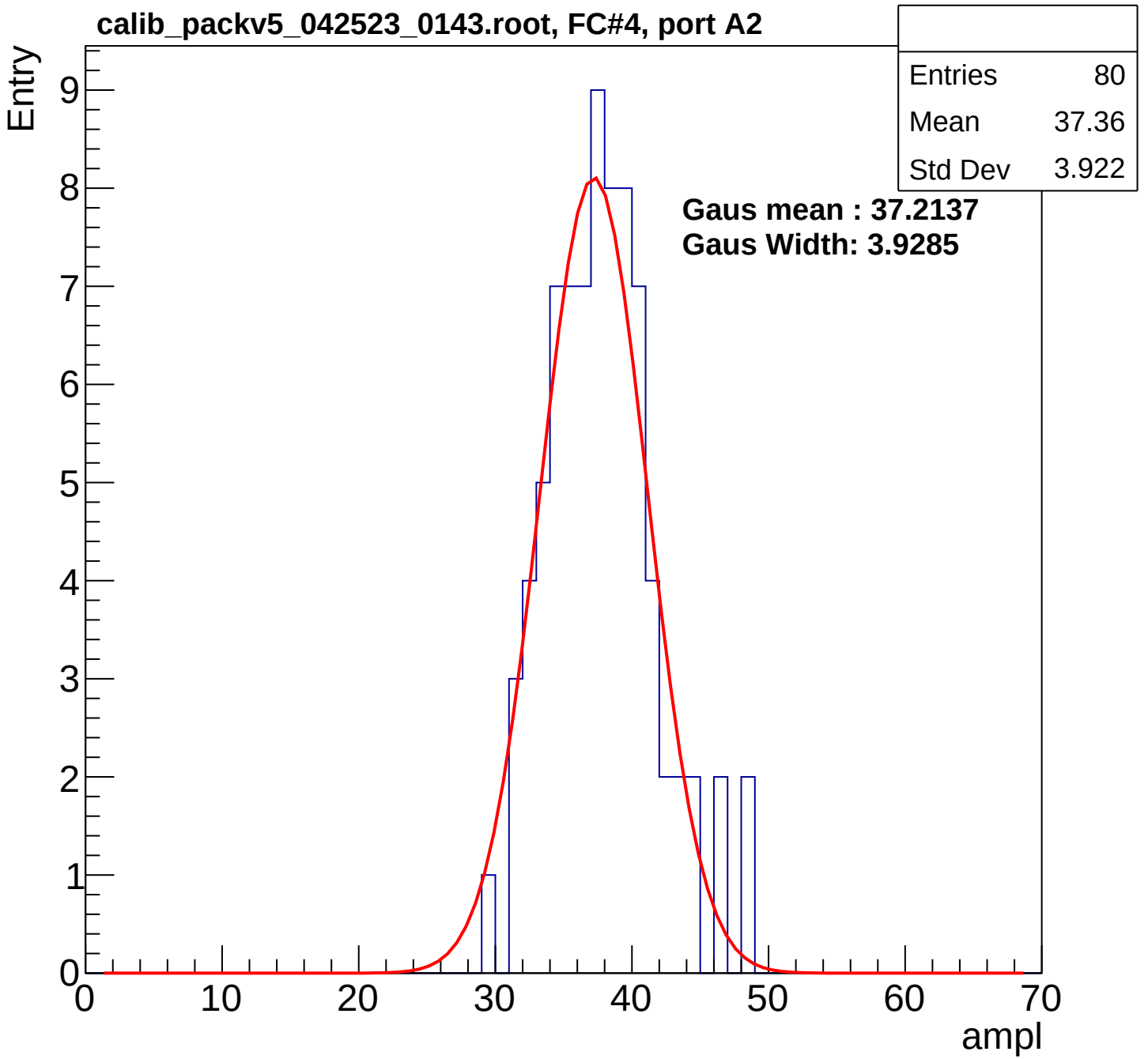

B1L100S, U18-ch110, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 68
Mean 55.24
Std Dev 3.515
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

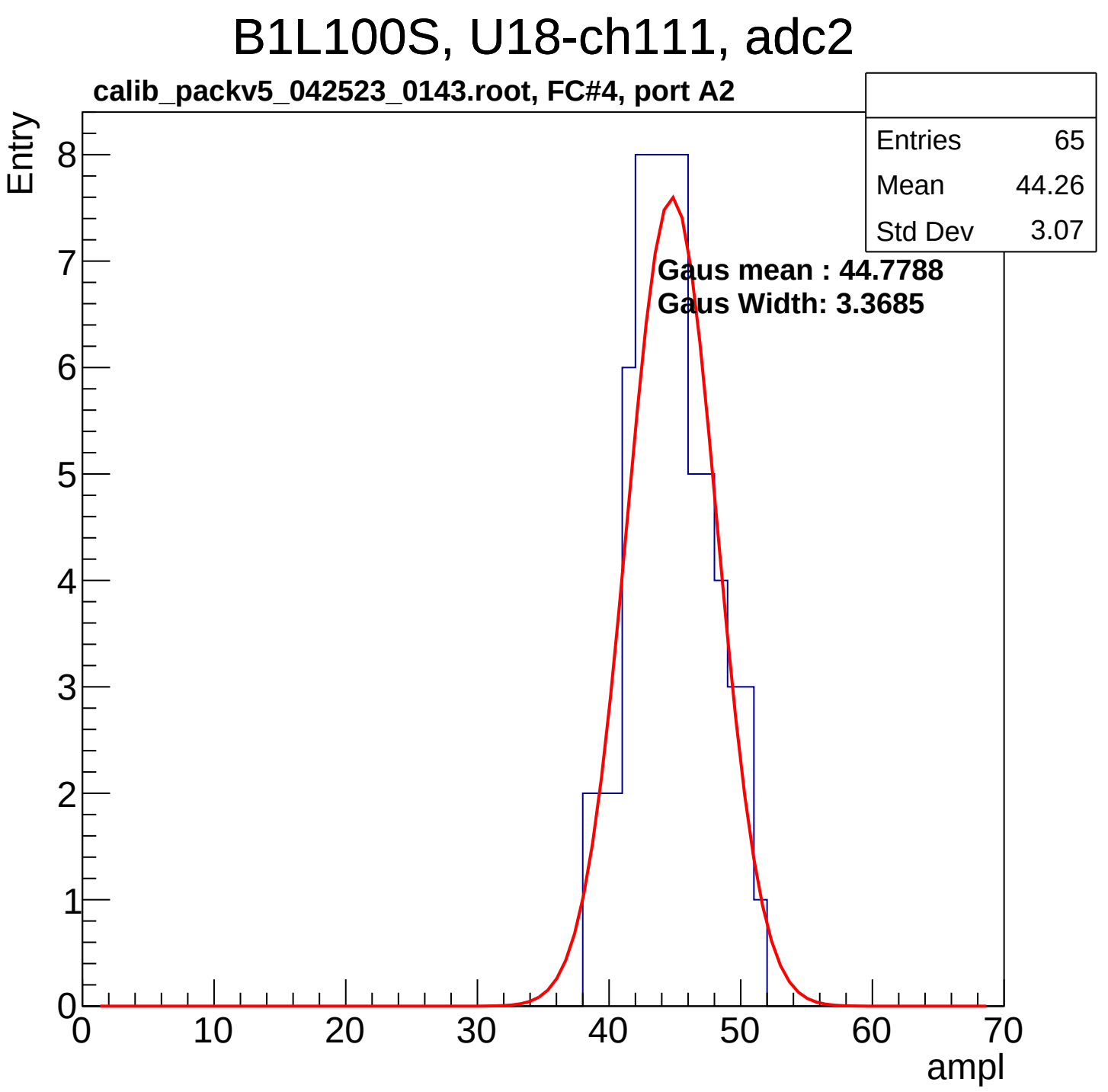

B1L100S, U18-ch110, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 57.91
Std Dev 9.38
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

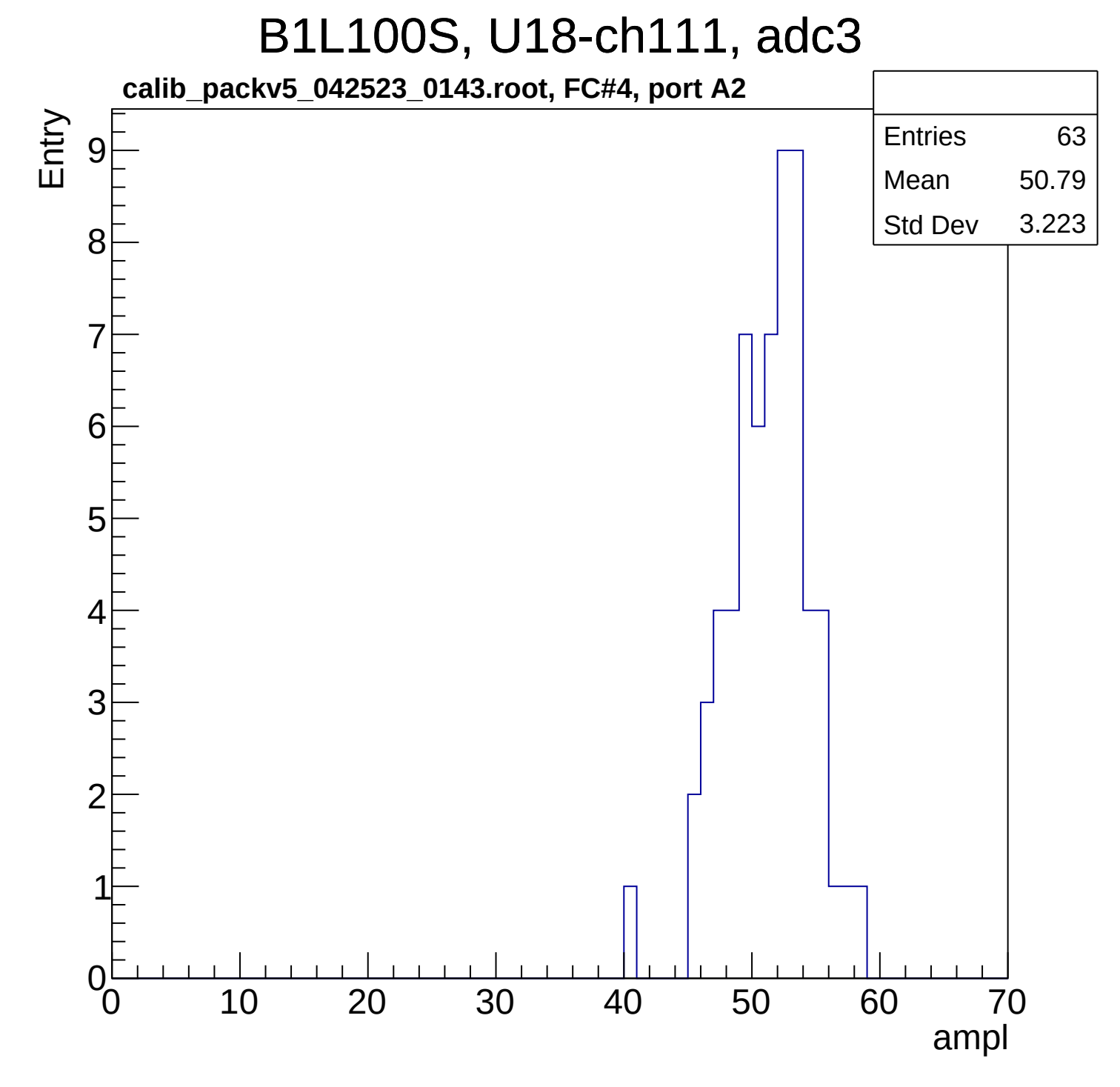

B1L100S, U18-ch110, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 61.56
Std Dev 1.257
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

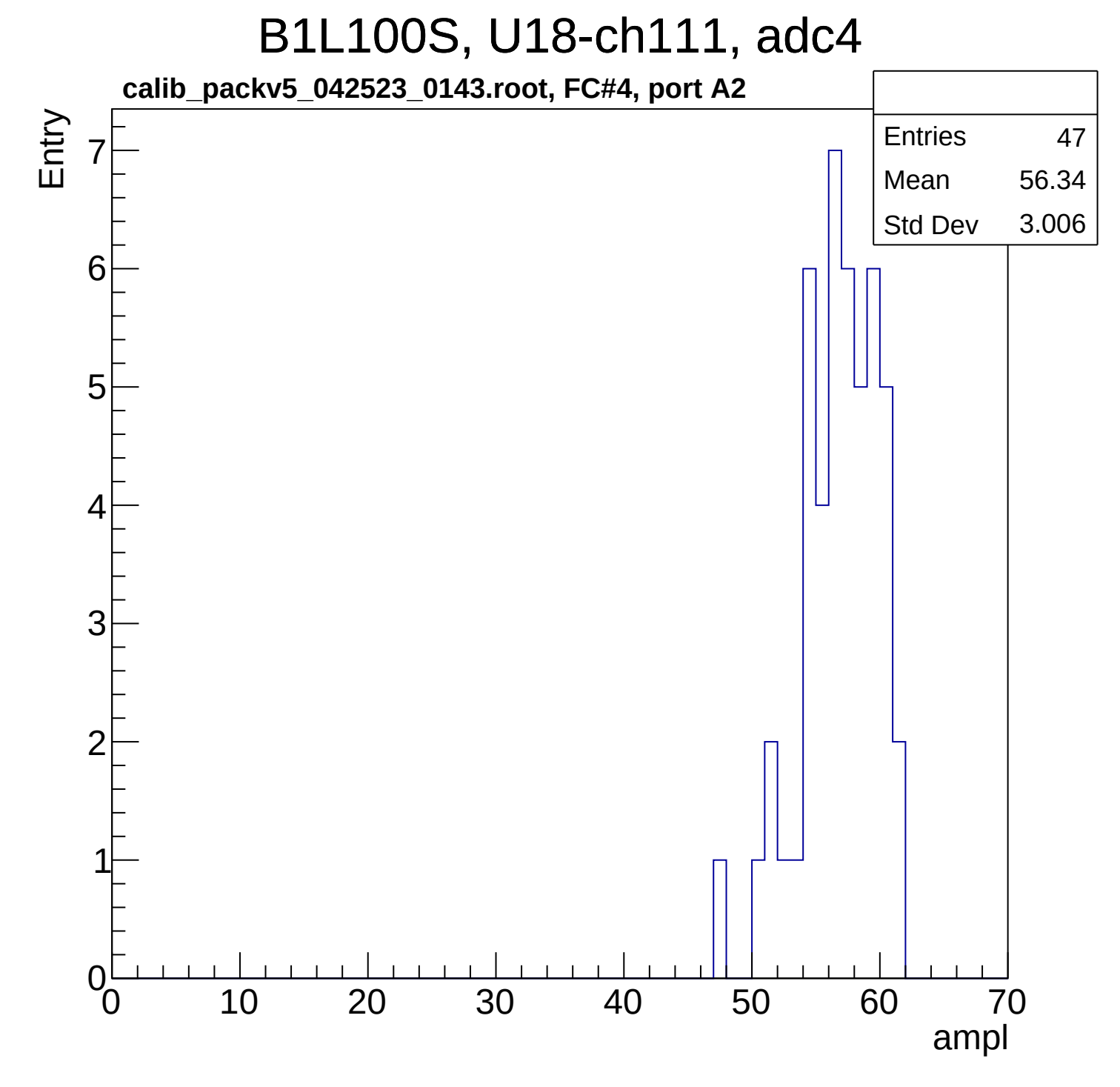

B1L100S, U18-ch110, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

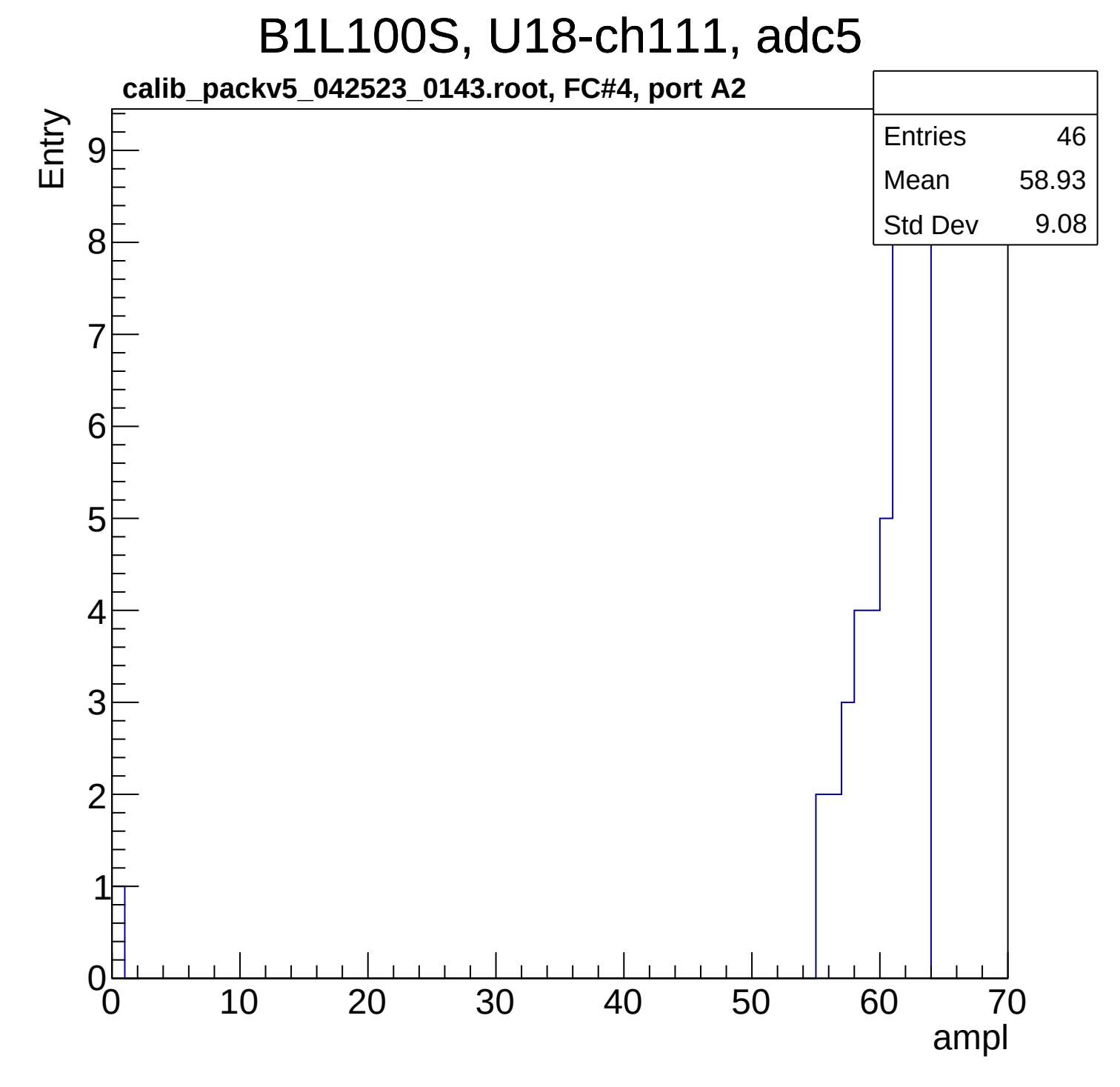

B1L100S, U18-ch111, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 29.86
Std Dev 3.218
Gaus mean : 30.4137
Gaus Width: 3.3928
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

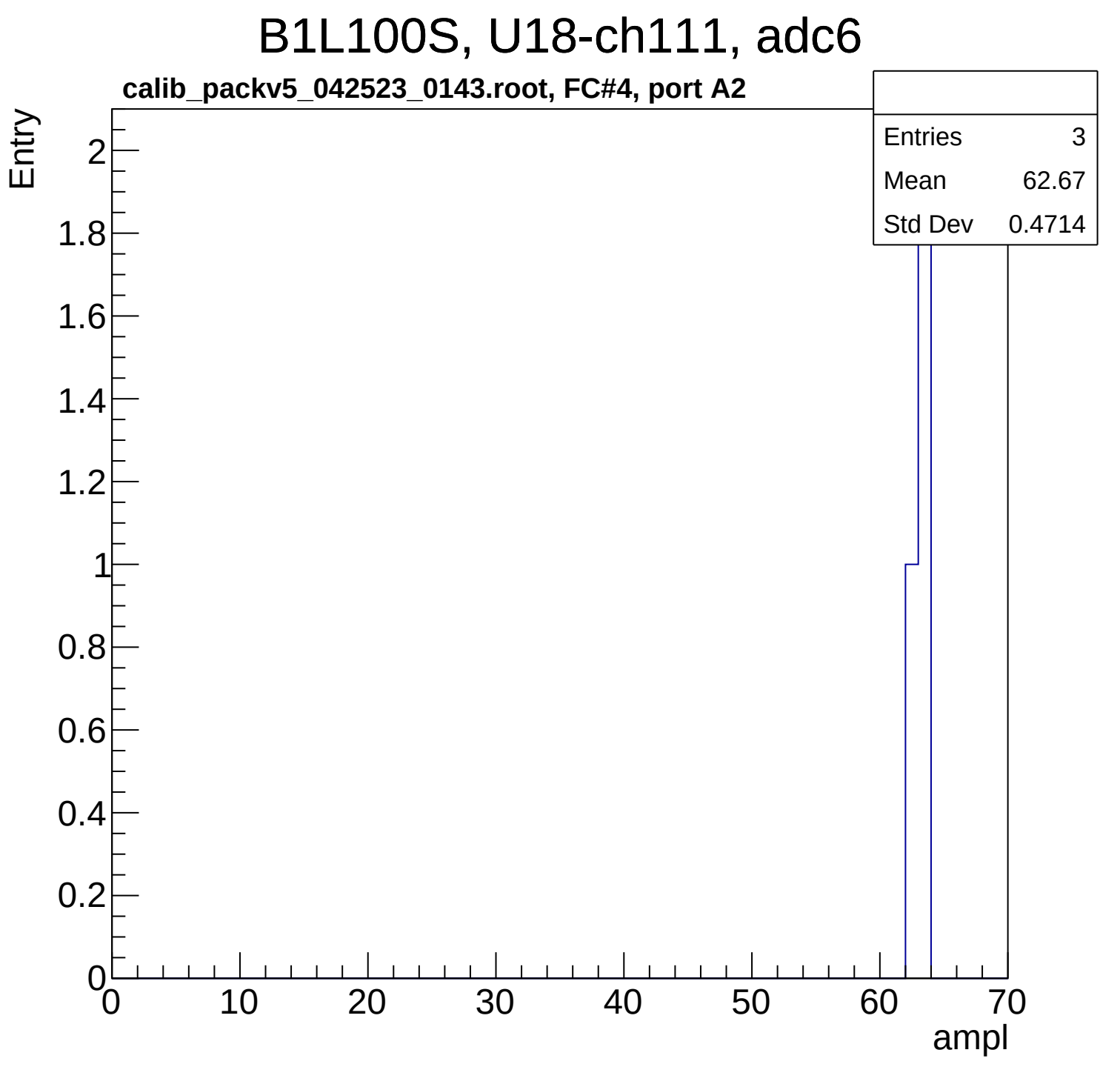

B1L100S, U18-ch111, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 80
Mean 37.36
Std Dev 3.922
Gaus mean : 37.2137
Gaus Width: 3.9285
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

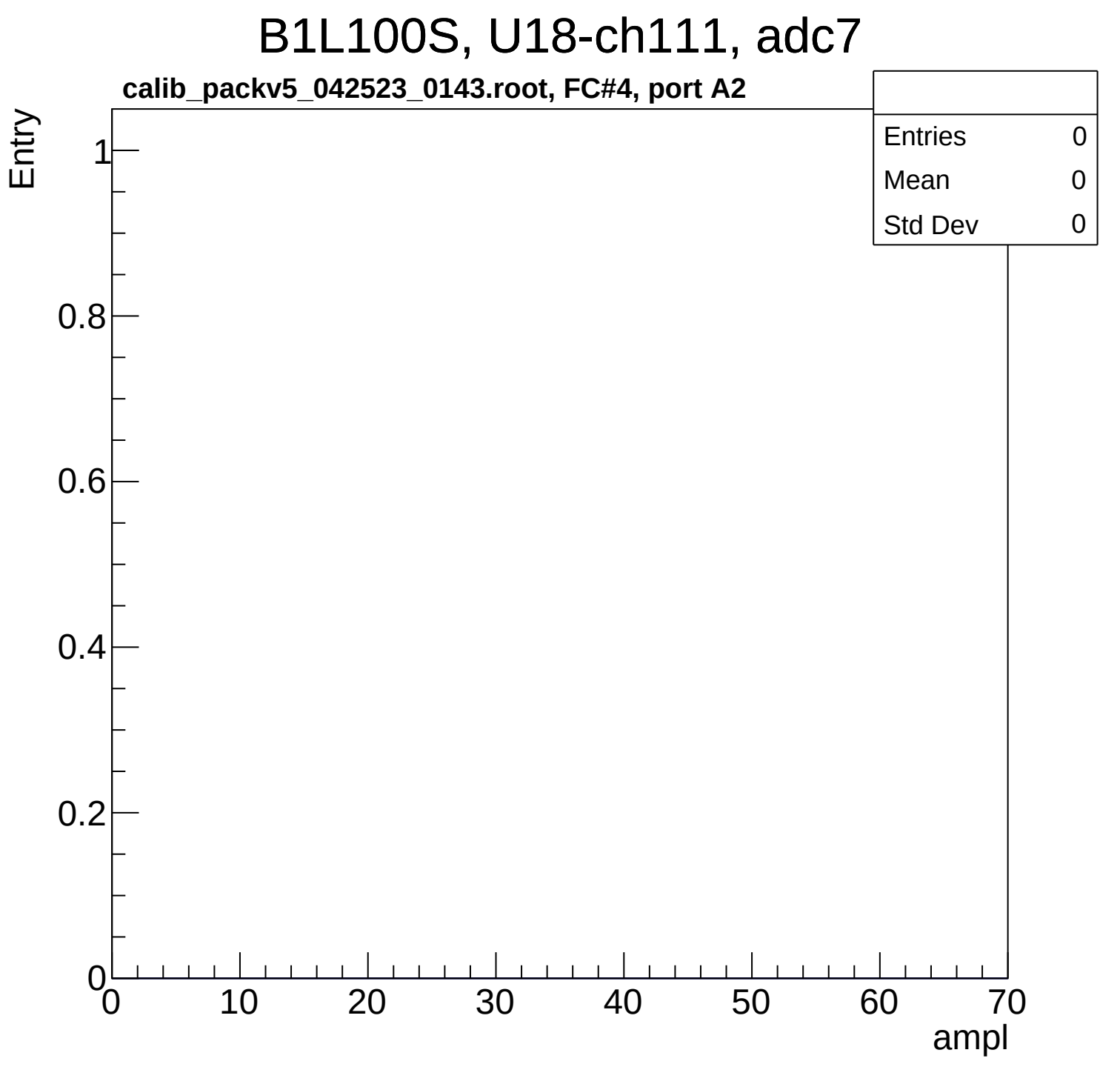

B1L100S, U18-ch111, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 65
Mean 44.26
Std Dev 3.07
Gaus mean : 44.7788
Gaus Width: 3.3685
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

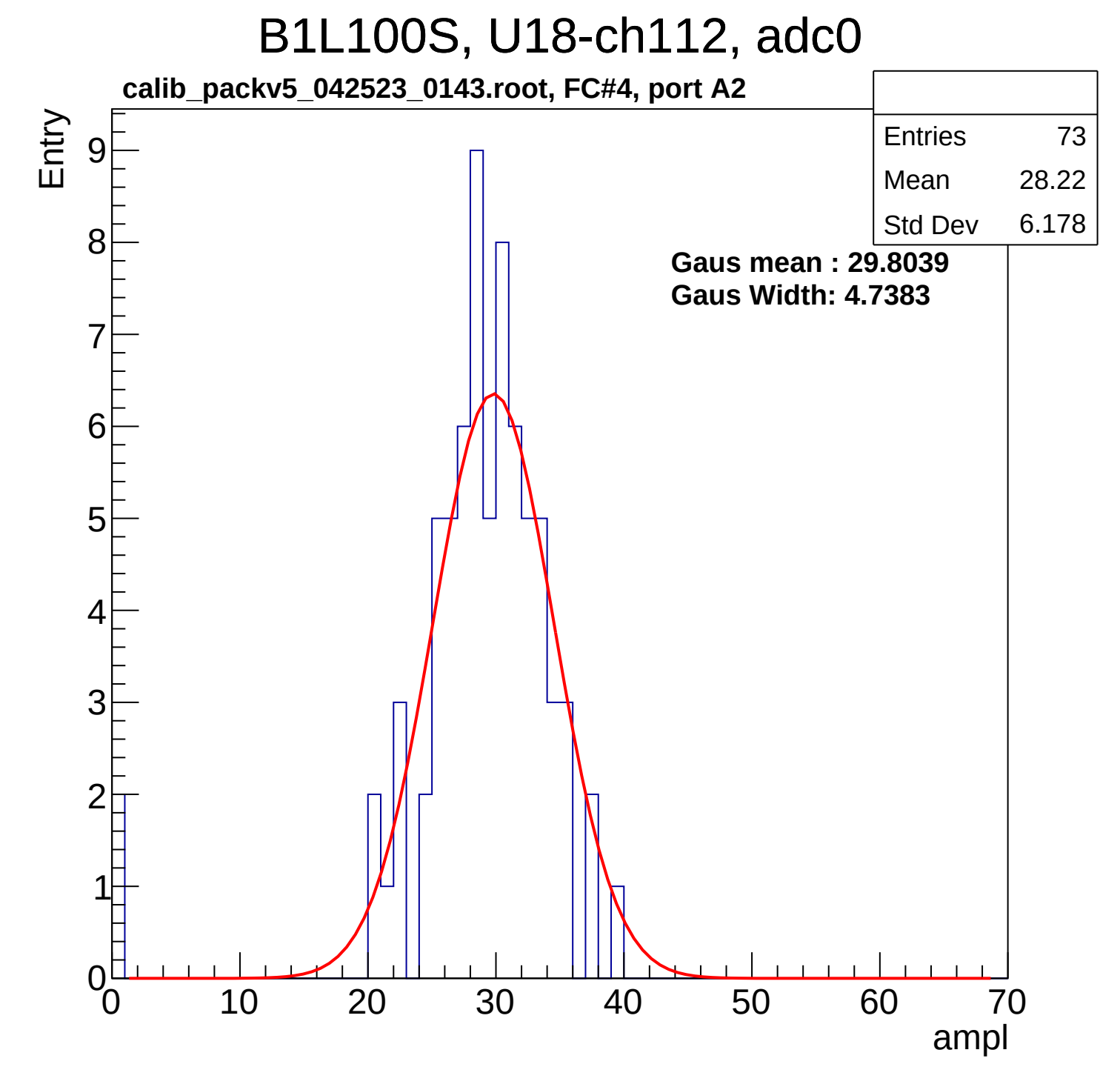

B1L100S, U18-ch111, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 50.79
Std Dev 3.223
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

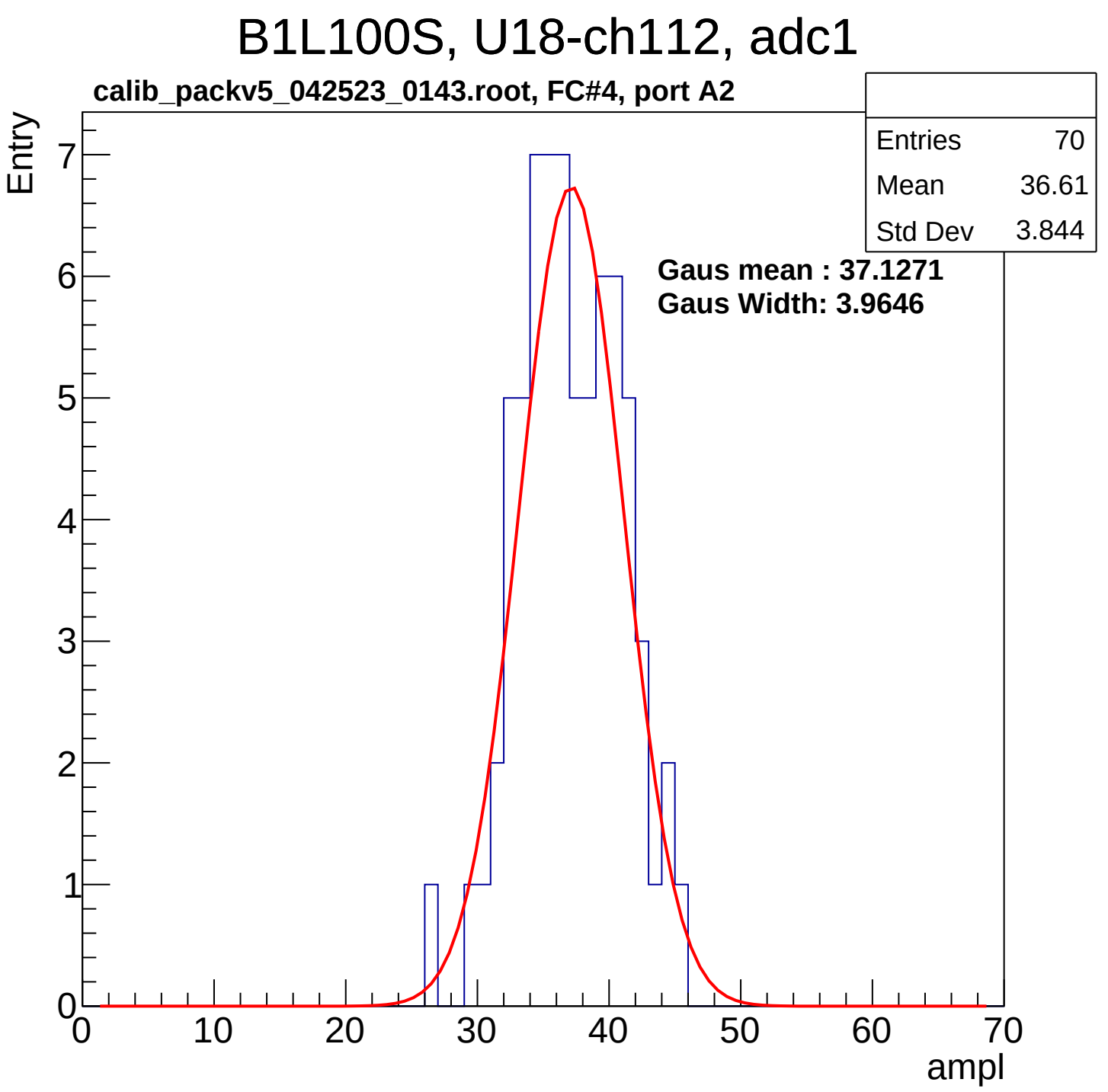

B1L100S, U18-ch111, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 56.34
Std Dev 3.006
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

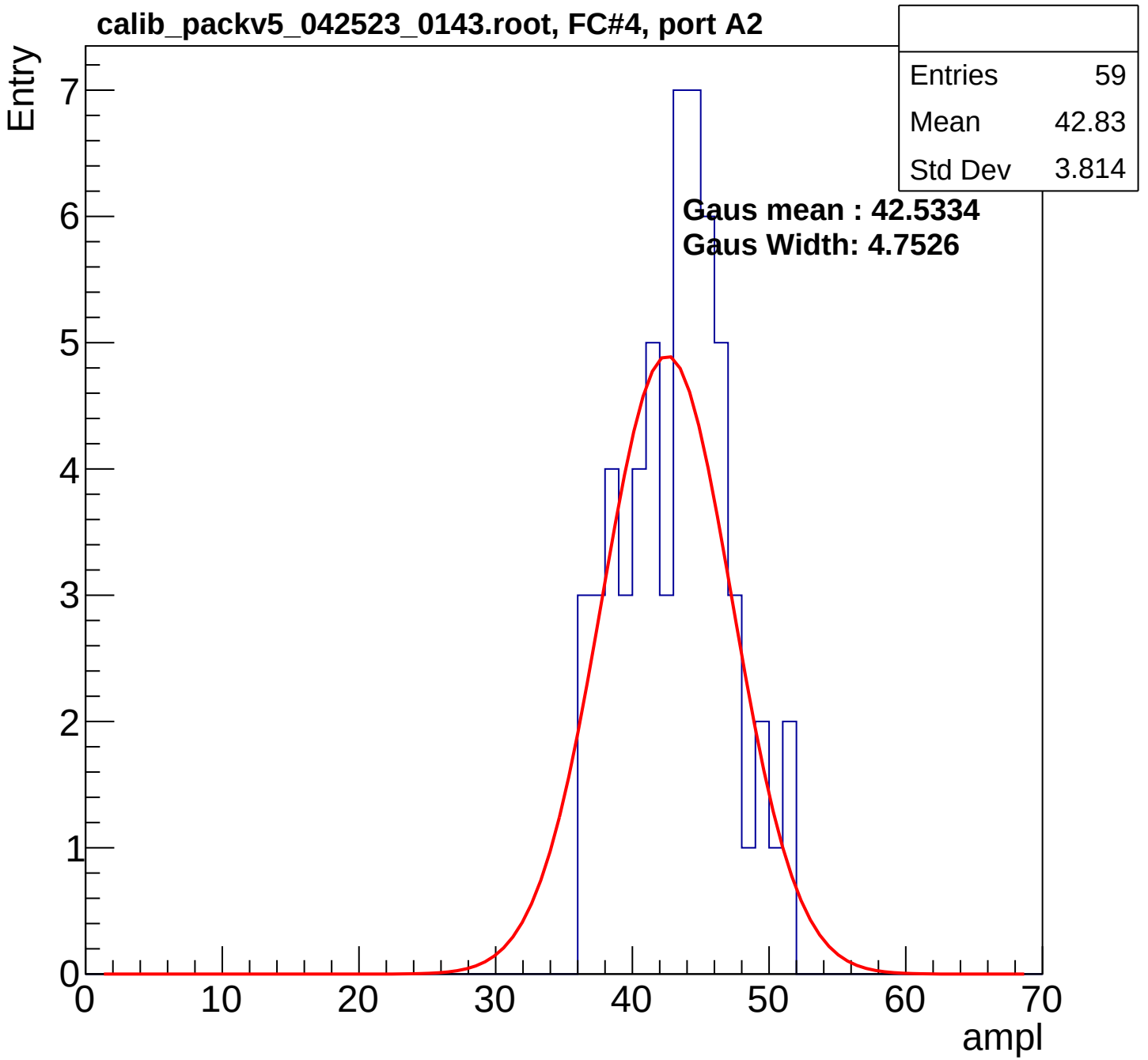

B1L100S, U18-ch111, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 46
Mean 58.93
Std Dev 9.08
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

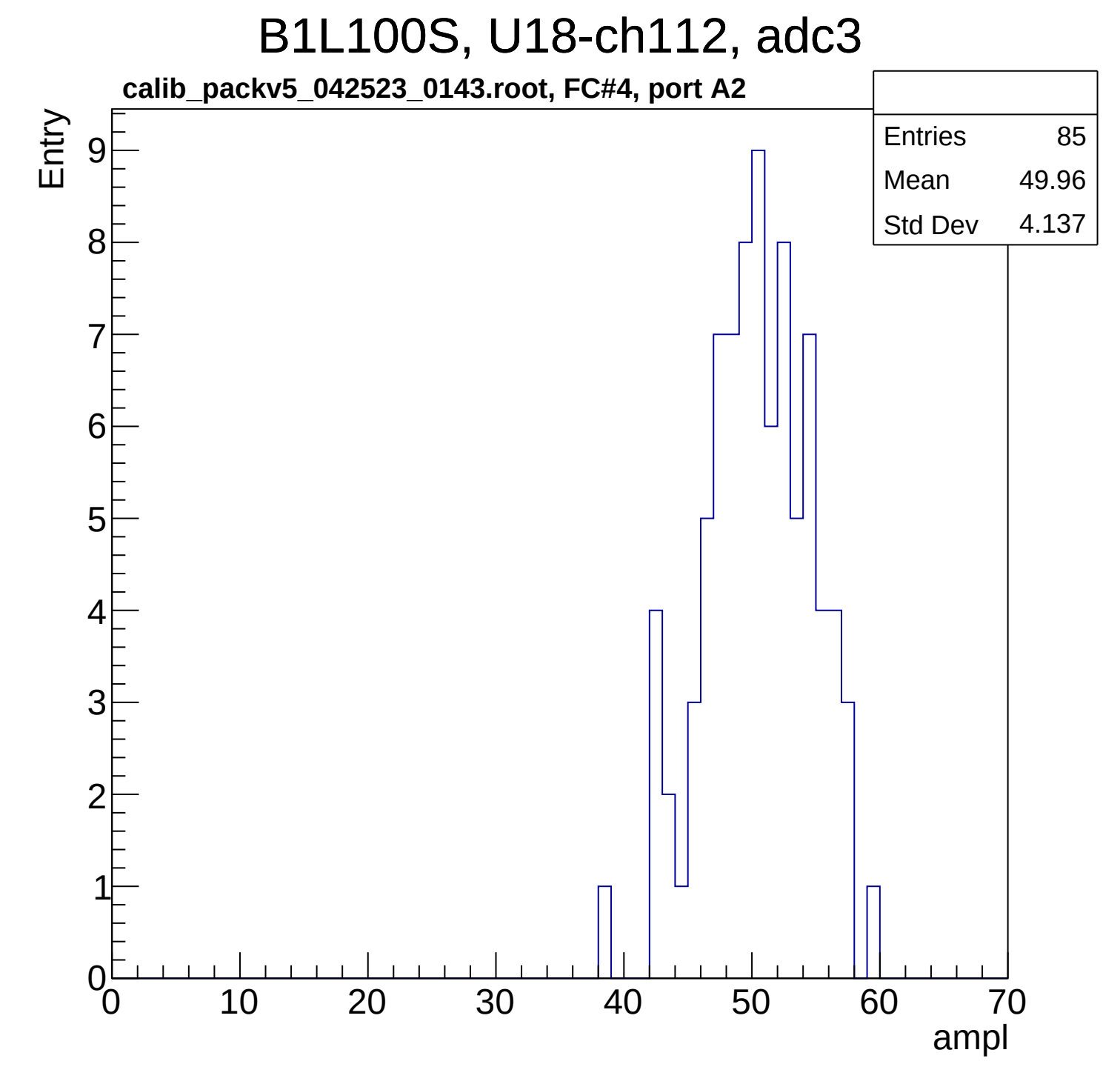

B1L100S, U18-ch111, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 62.67
Std Dev 0.4714
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

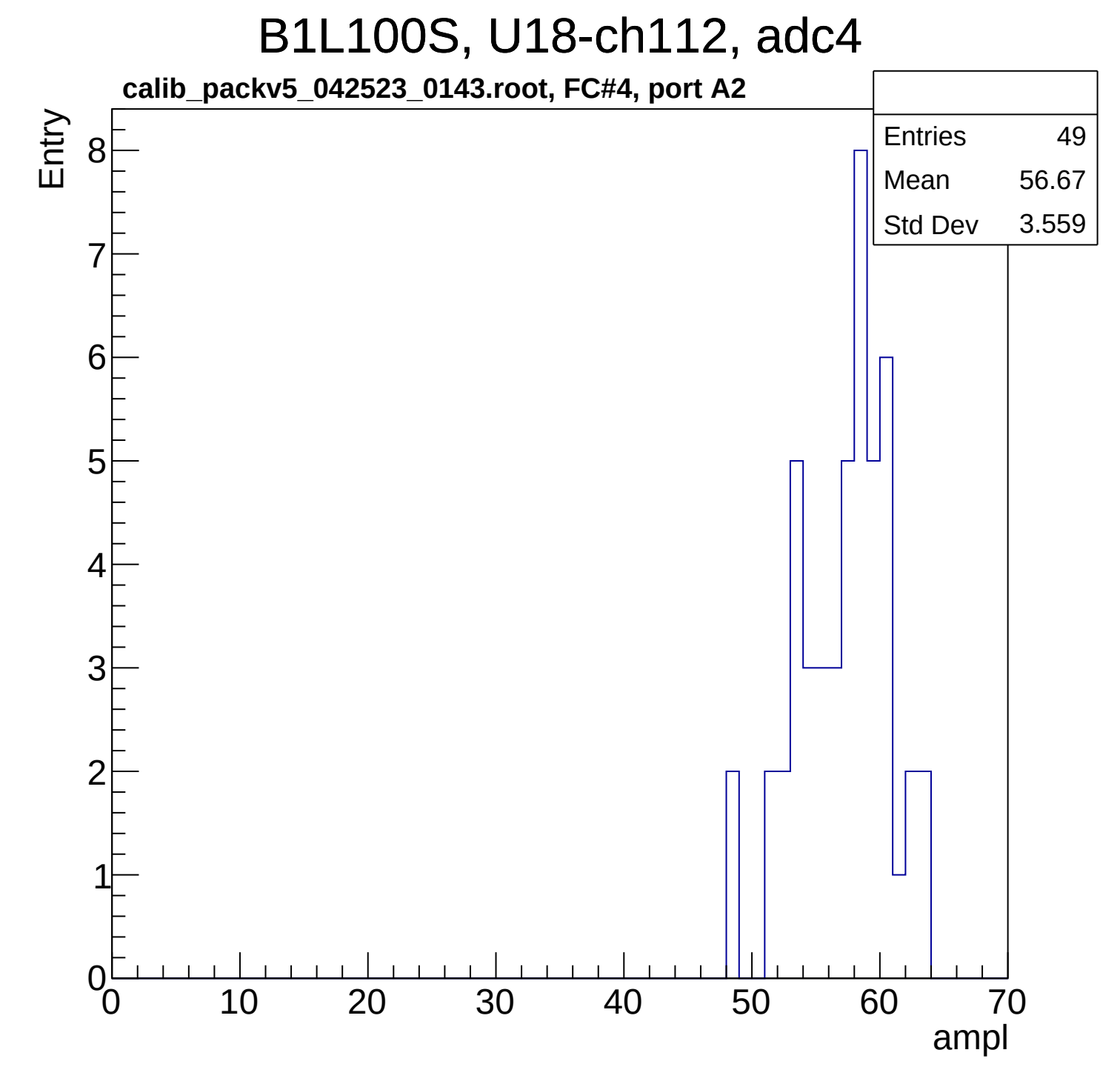

B1L100S, U18-ch111, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

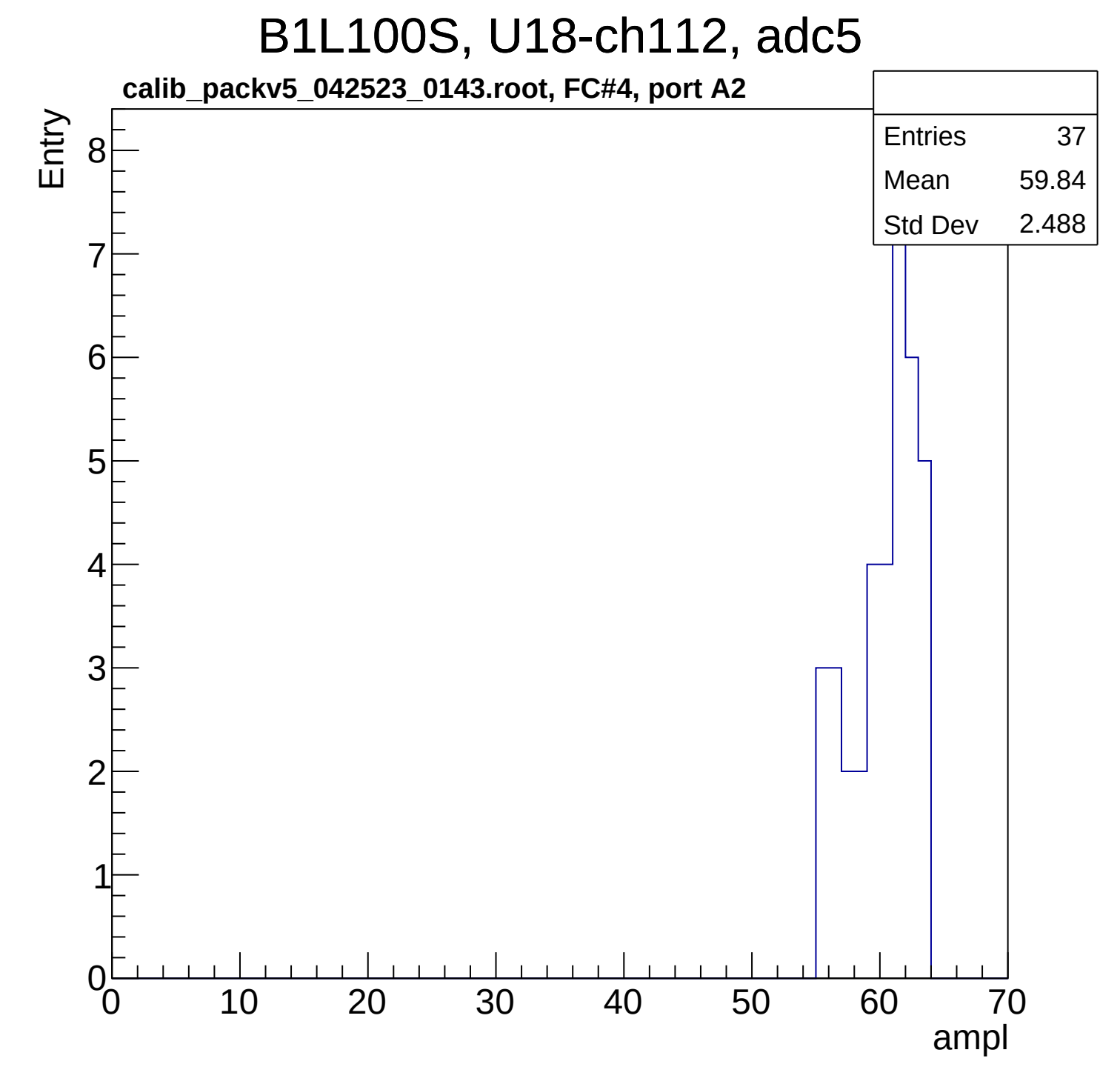

B1L100S, U18-ch112, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 28.22
Std Dev 6.178
Gaus mean : 29.8039
Gaus Width: 4.7383
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

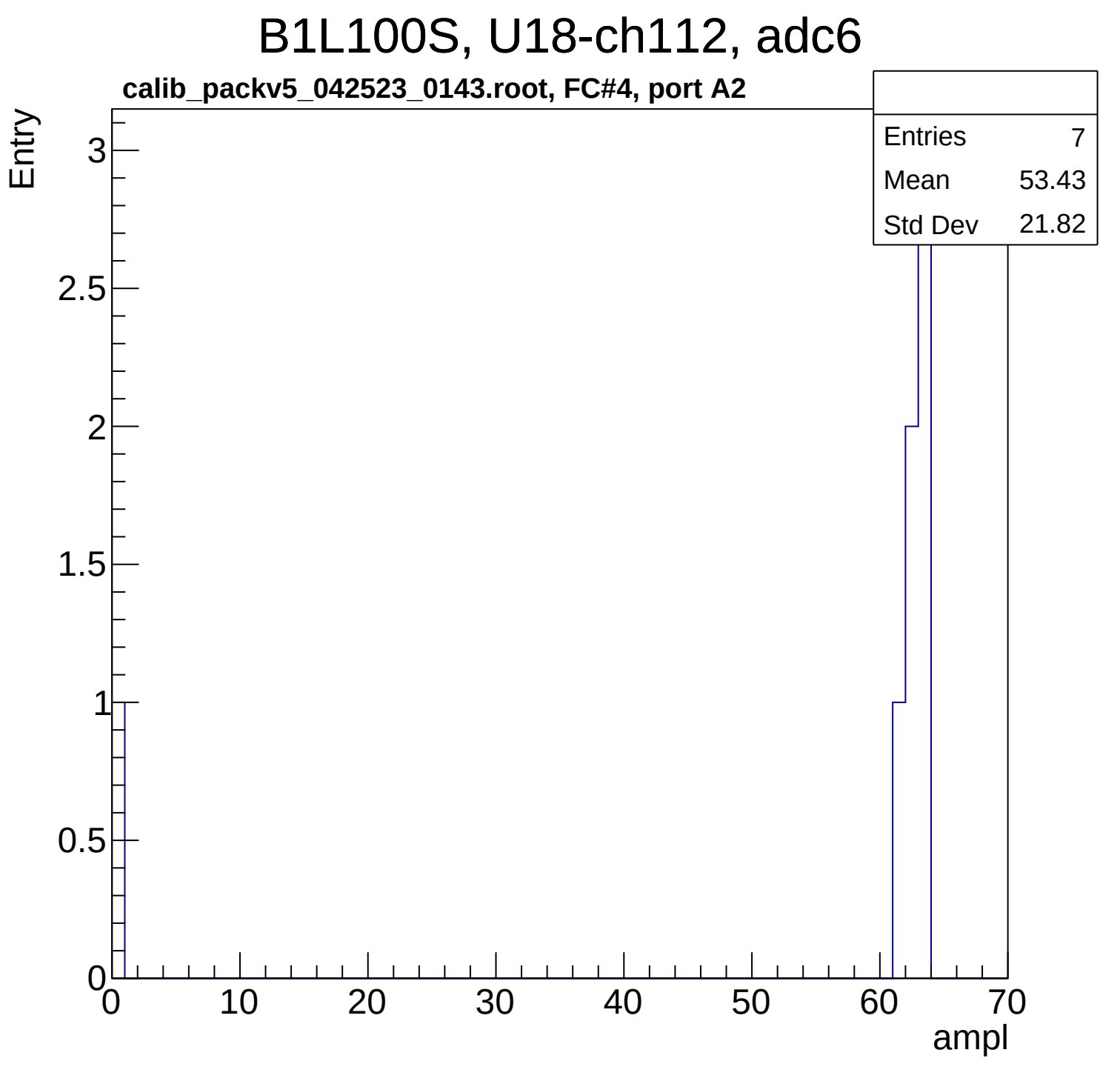

B1L100S, U18-ch112, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 36.61
Std Dev 3.844
Gaus mean : 37.1271
Gaus Width: 3.9646
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

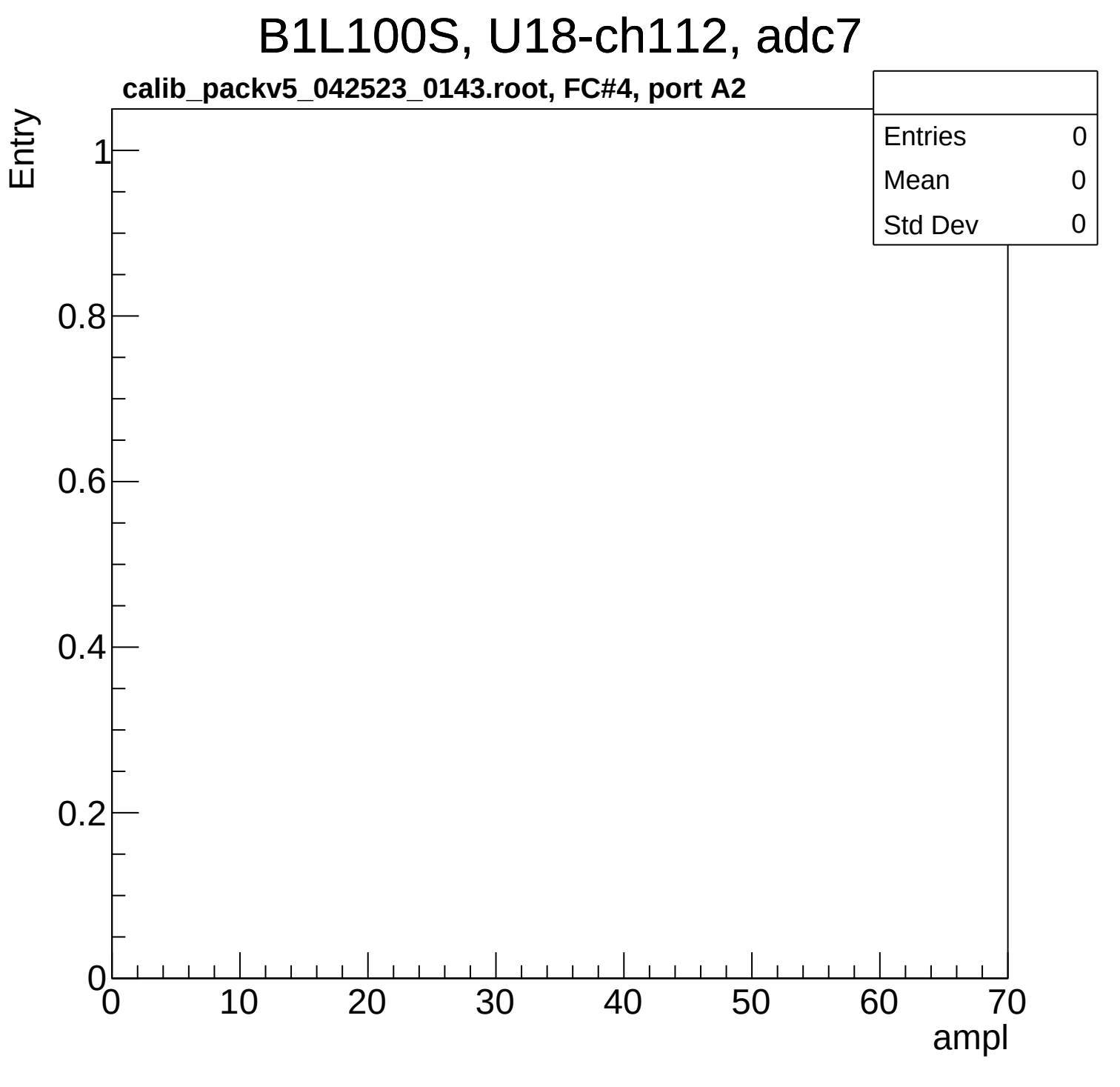

B1L100S, U18-ch112, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 42.83
Std Dev 3.814
Gaus mean : 42.5334
Gaus Width: 4.7526
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

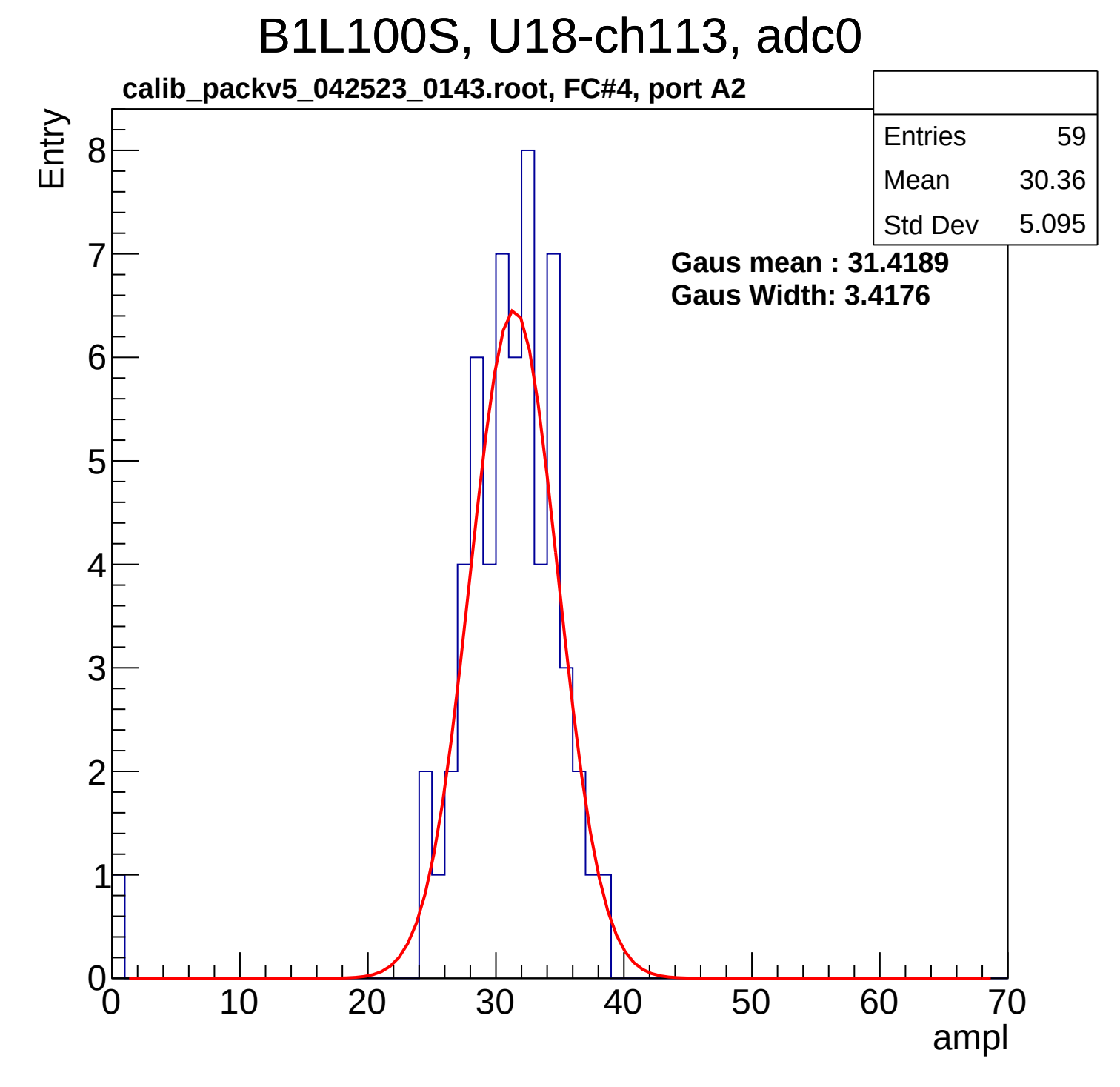

B1L100S, U18-ch112, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 85
Mean 49.96
Std Dev 4.137
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

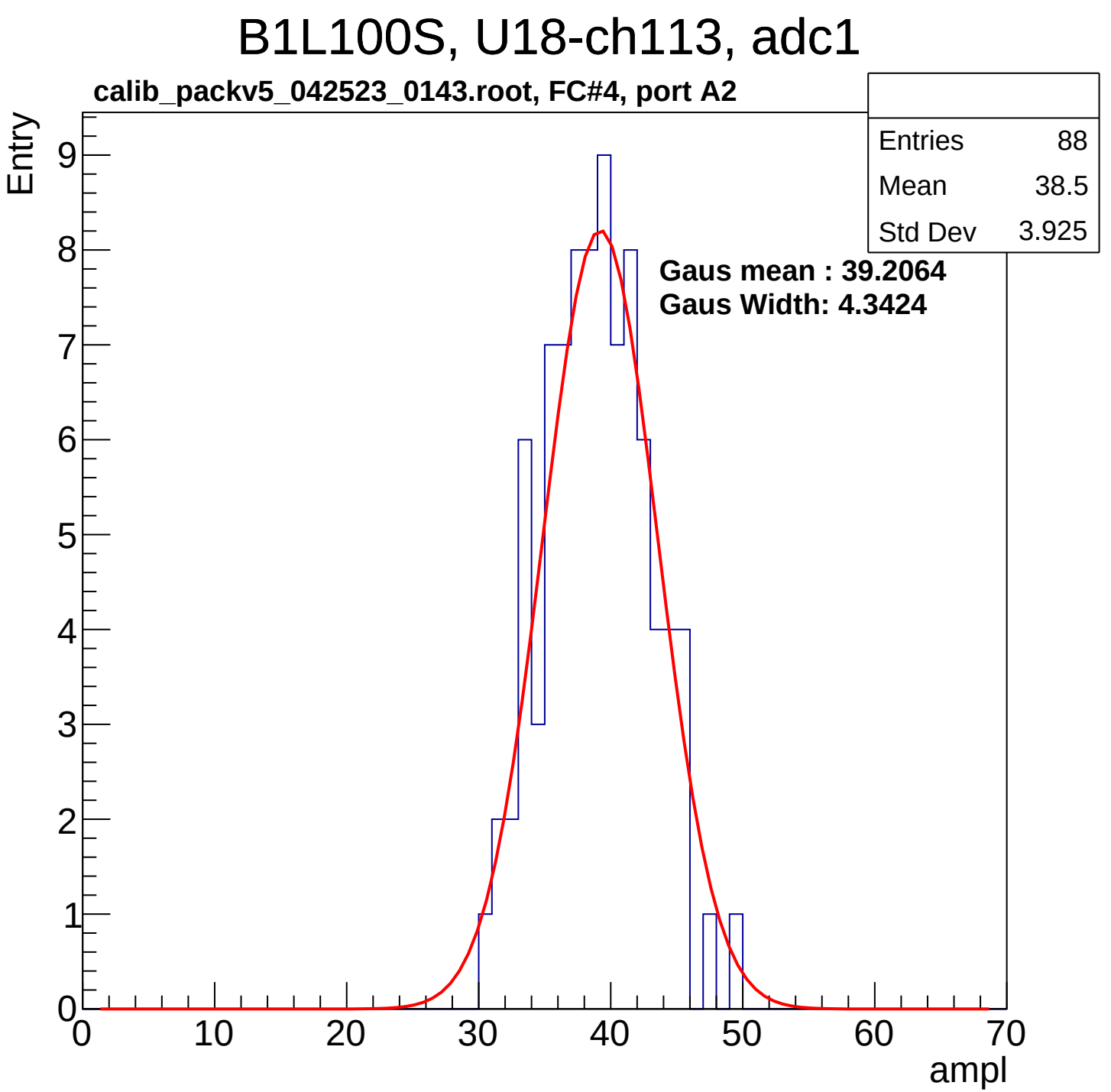

B1L100S, U18-ch112, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 49
Mean 56.67
Std Dev 3.559
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

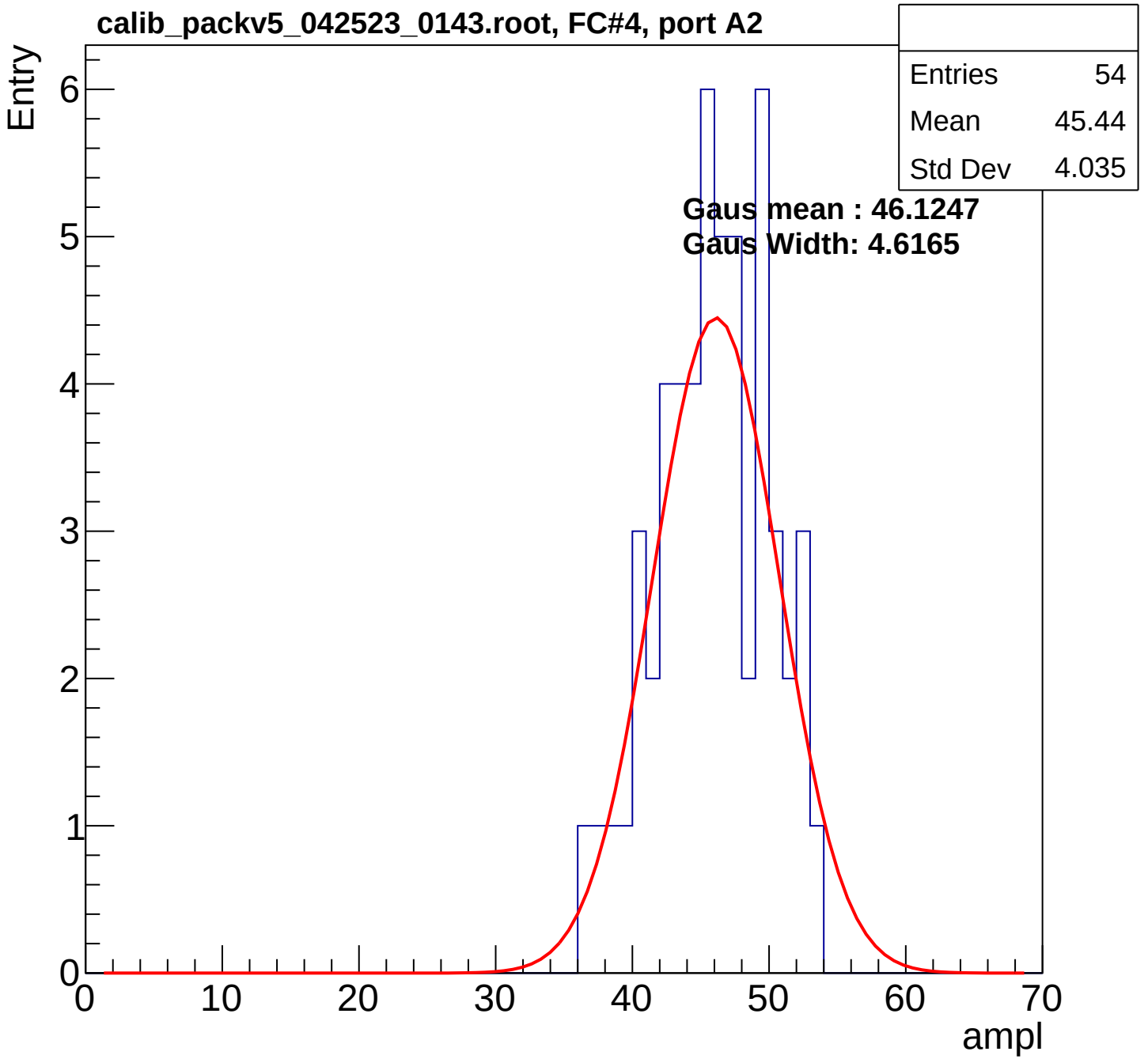

B1L100S, U18-ch112, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 37
Mean 59.84
Std Dev 2.488
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

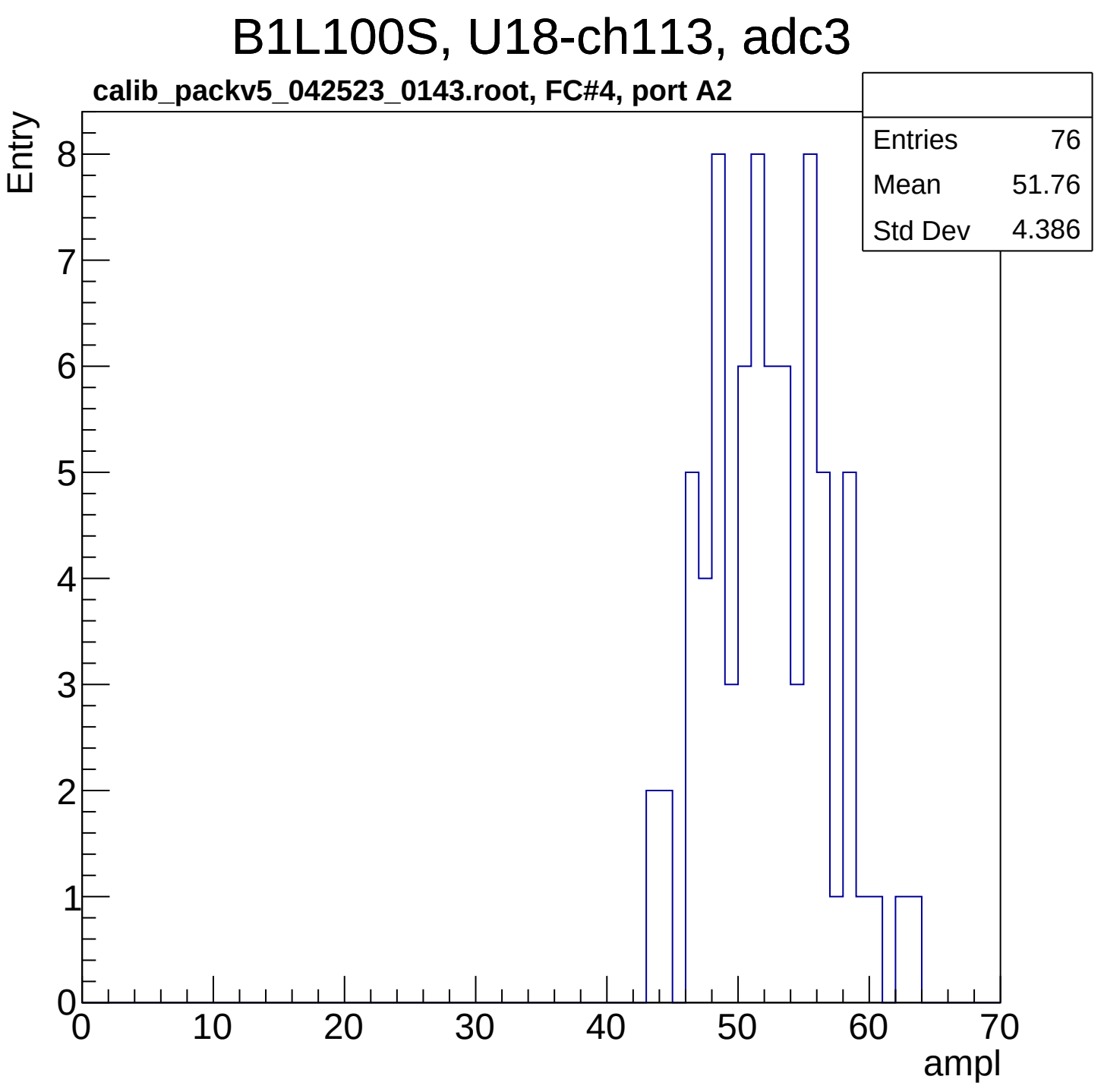

B1L100S, U18-ch112, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 53.43
Std Dev 21.82
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

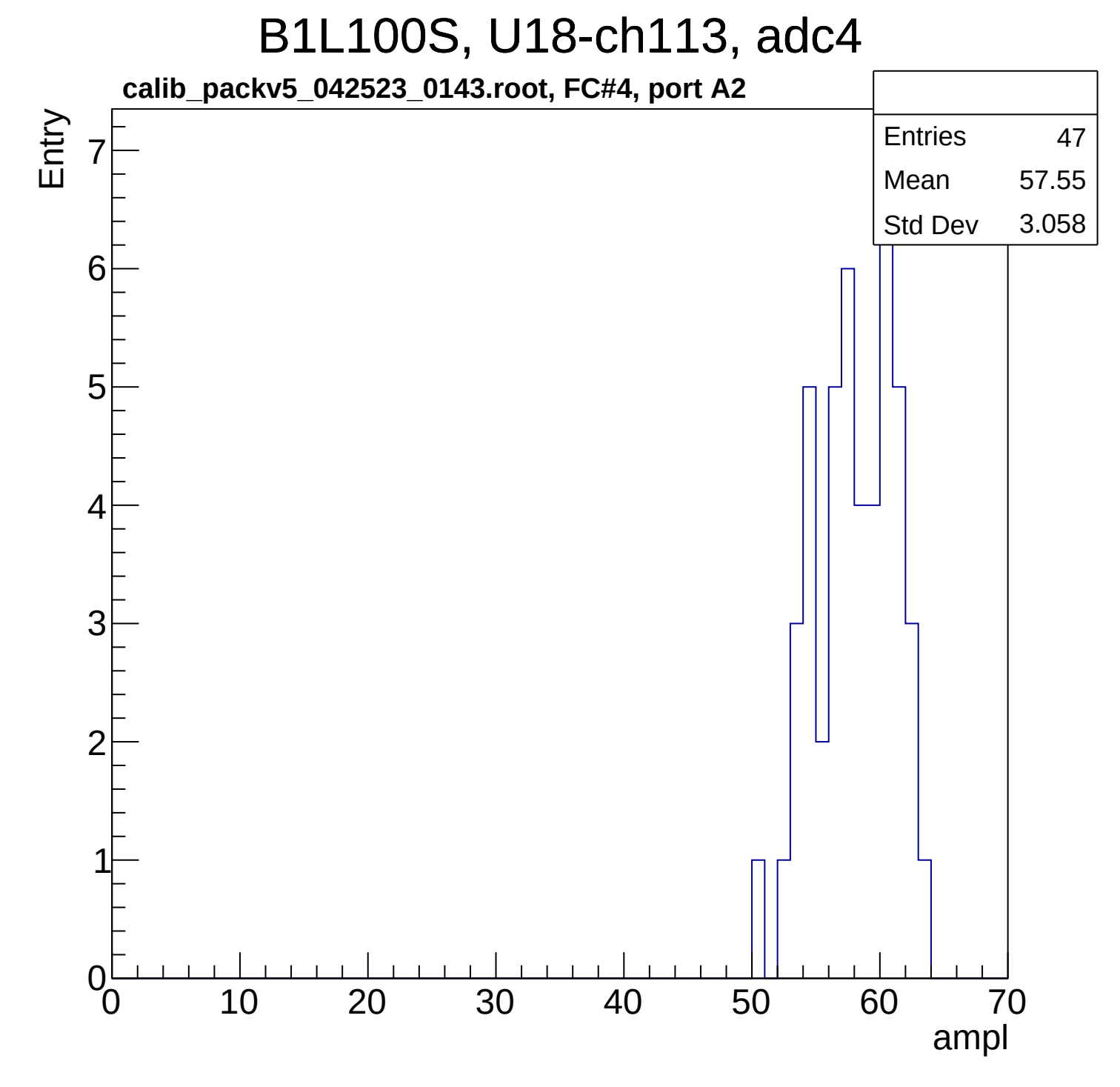

B1L100S, U18-ch112, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

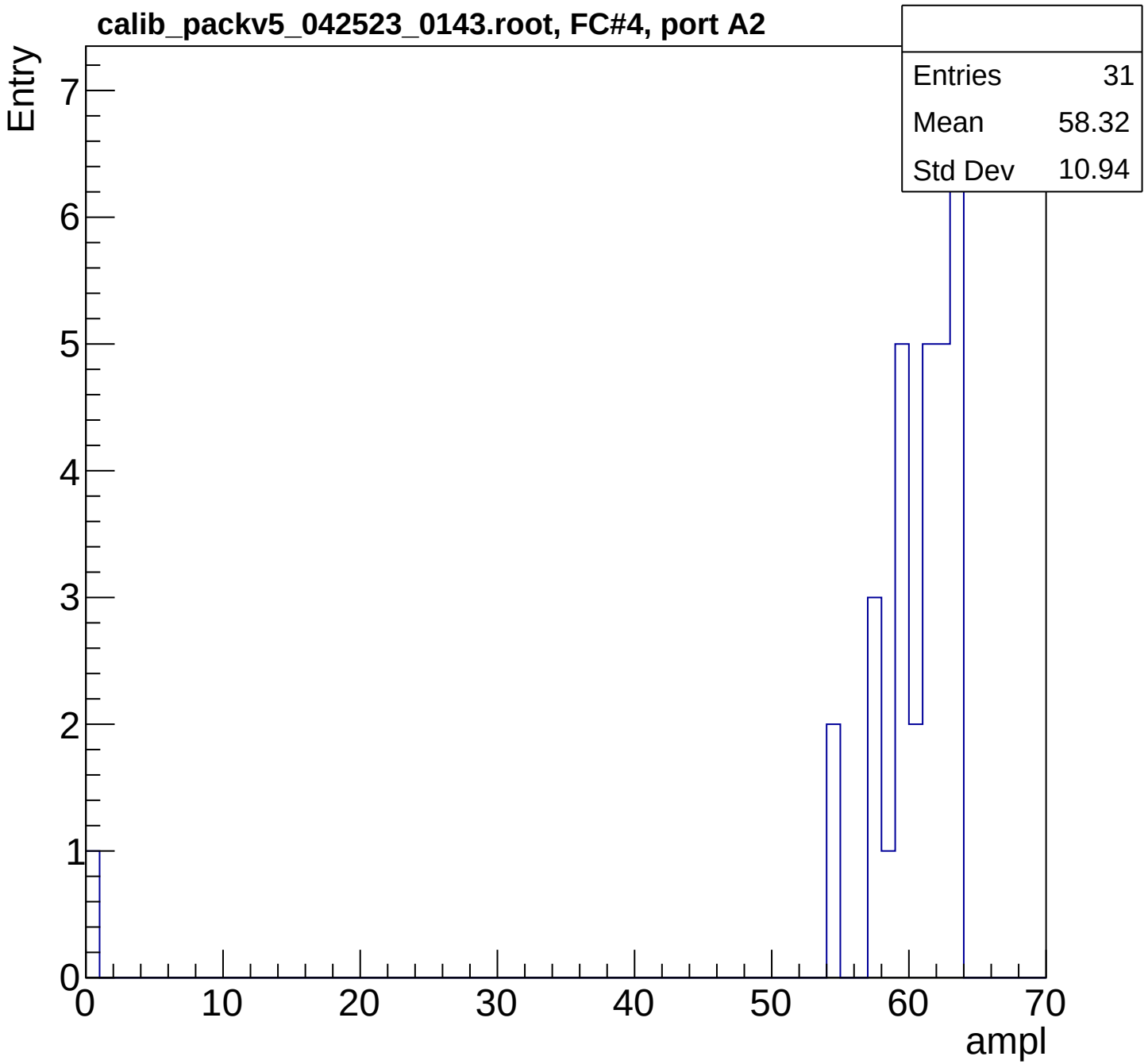

B1L100S, U18-ch113, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 30.36
Std Dev 5.095
Gaus mean : 31.4189
Gaus Width: 3.4176
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

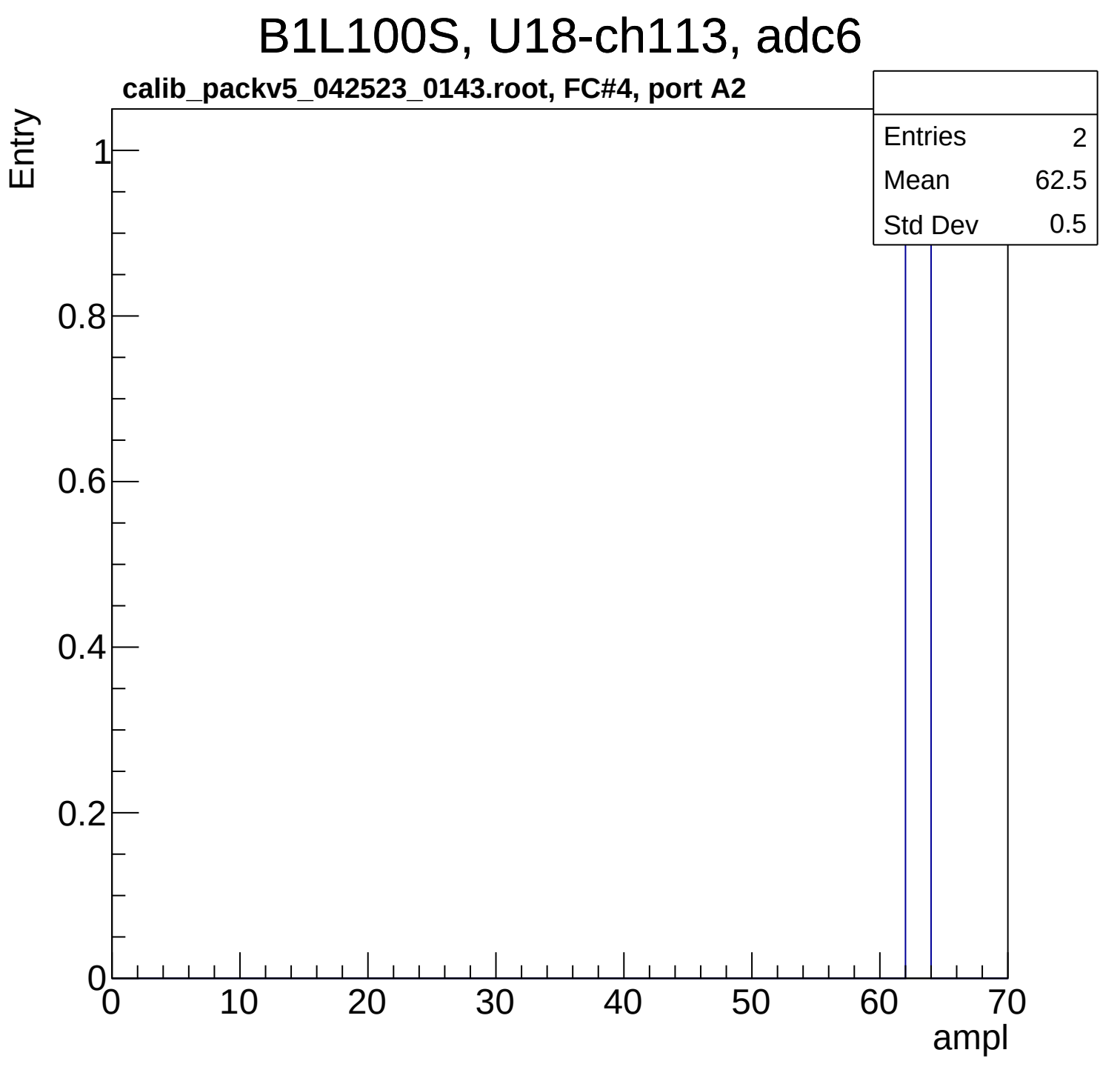

B1L100S, U18-ch113, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 88
Mean 38.5
Std Dev 3.925
Gaus mean : 39.2064
Gaus Width: 4.3424
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

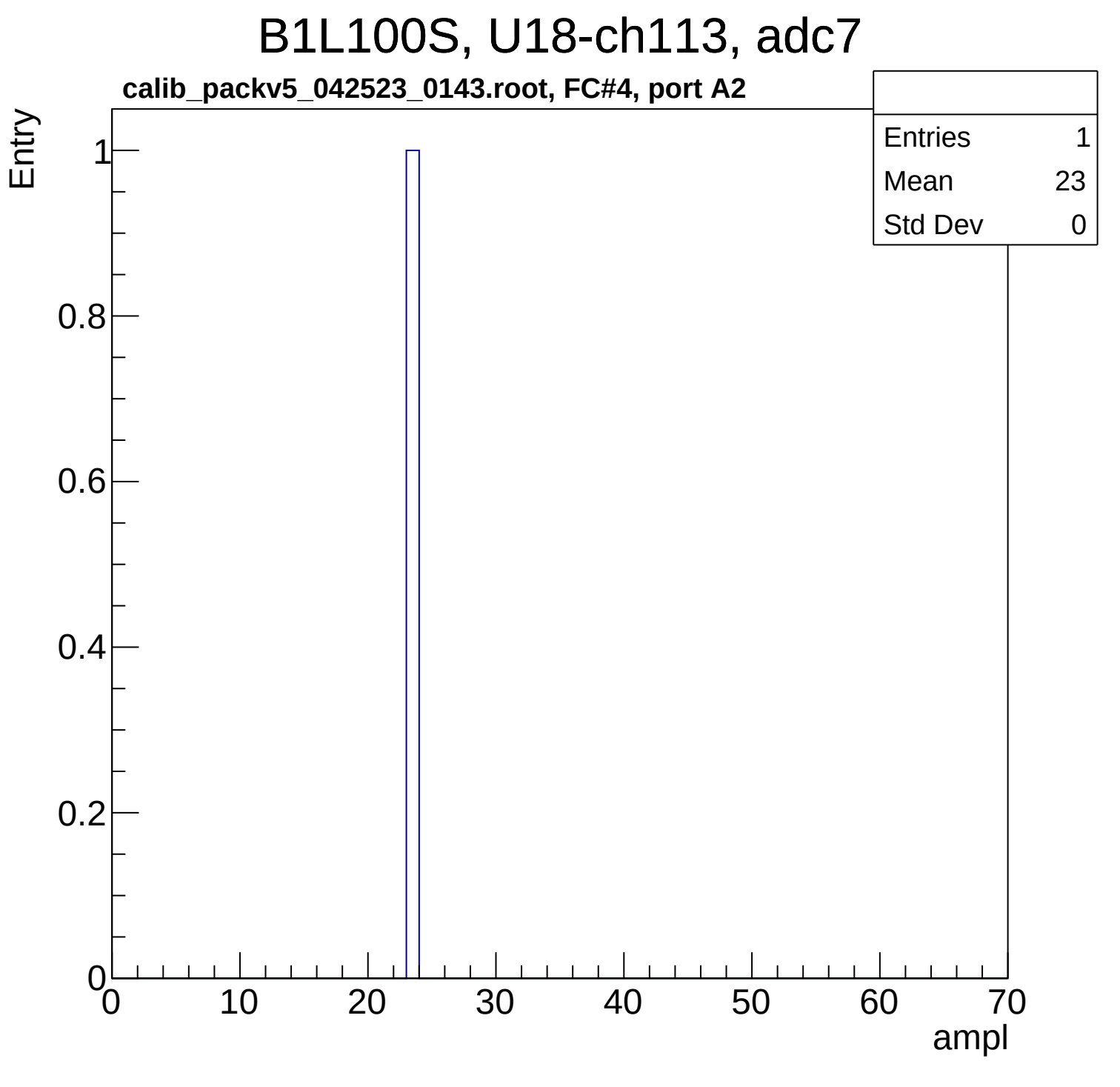

B1L100S, U18-ch113, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 45.44
Std Dev 4.035
Gaus mean : 46.1247
Gaus Width: 4.6165
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

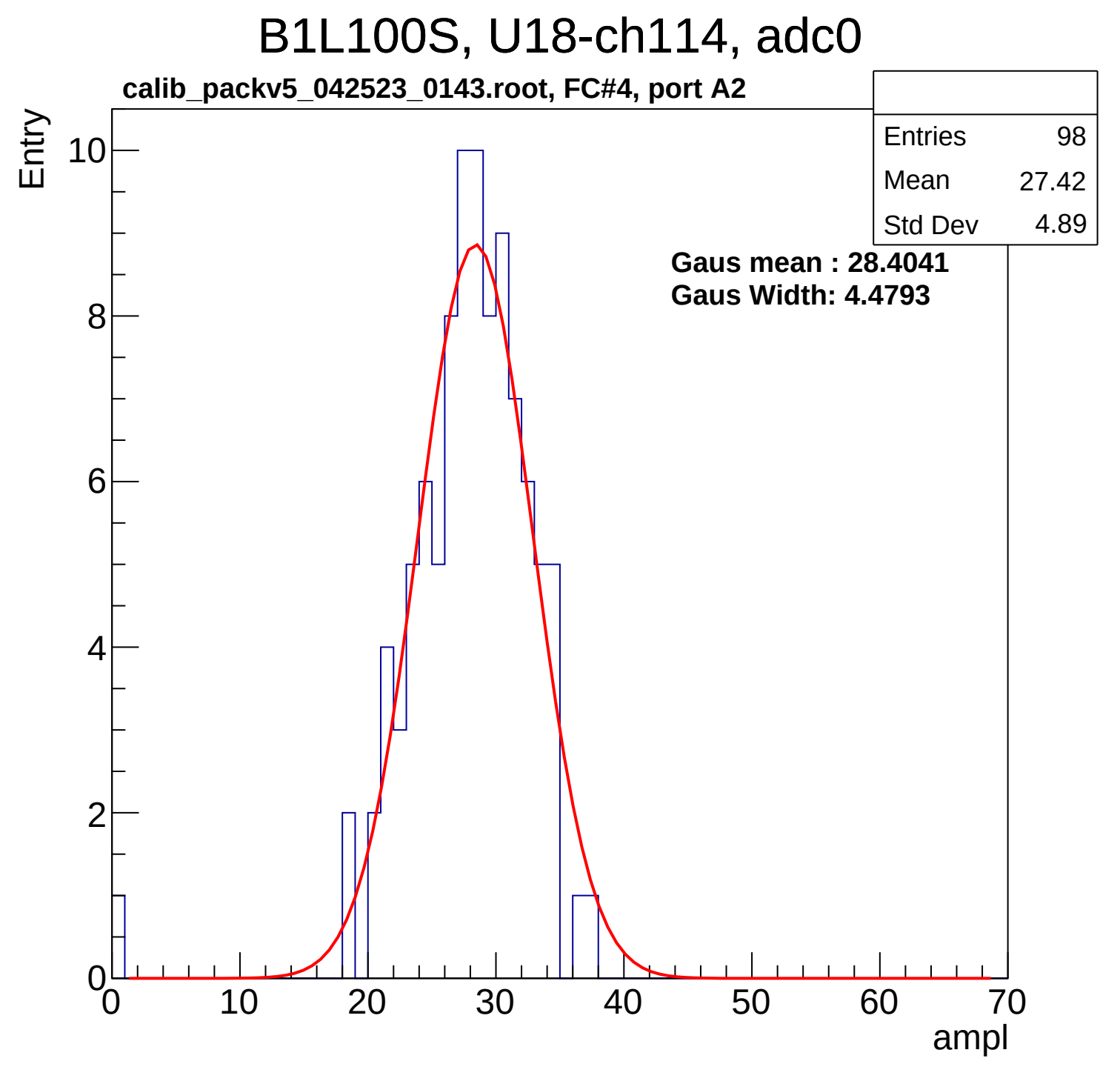

B1L100S, U18-ch113, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 51.76
Std Dev 4.386
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

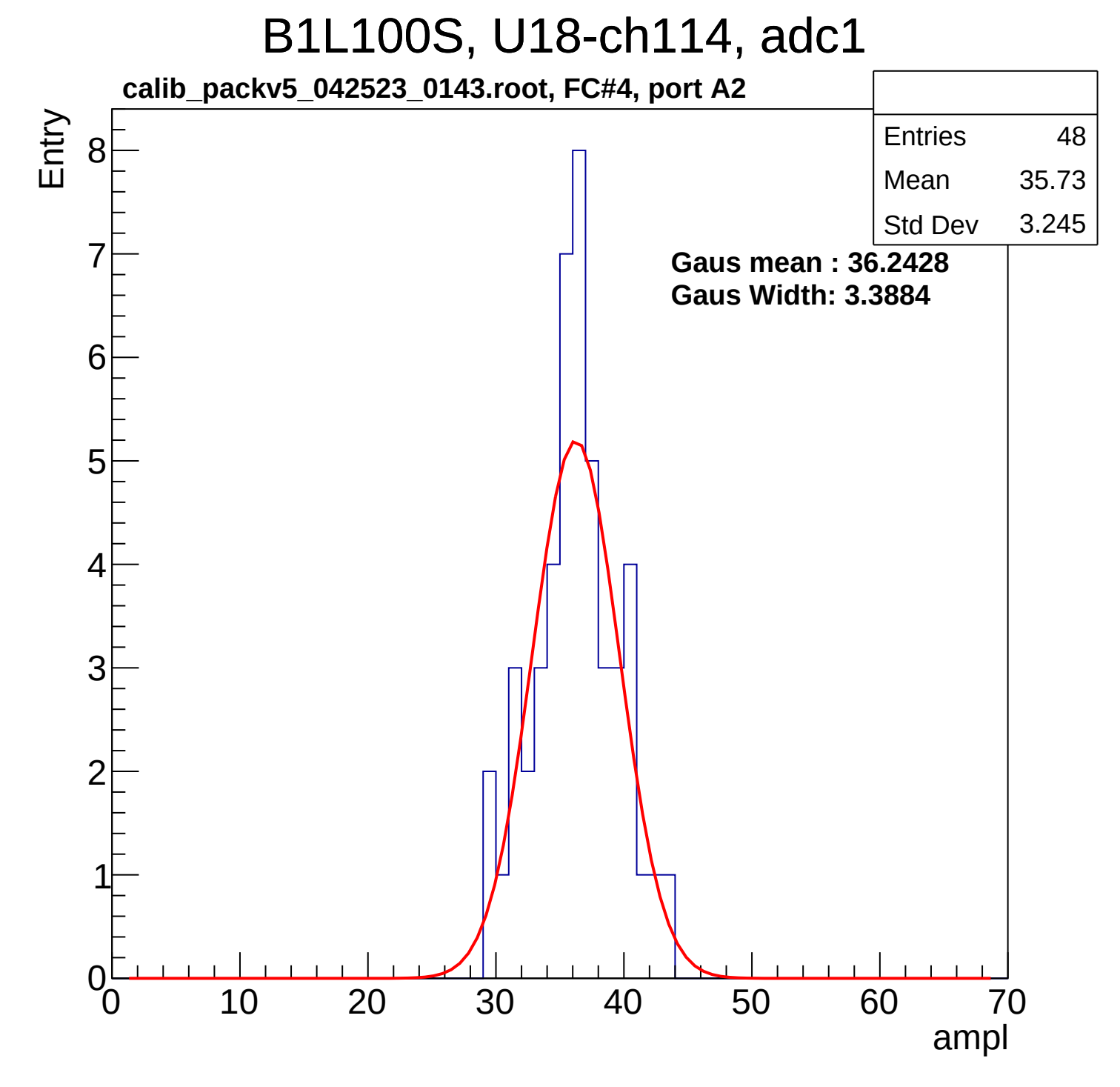

B1L100S, U18-ch113, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 57.55
Std Dev 3.058
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

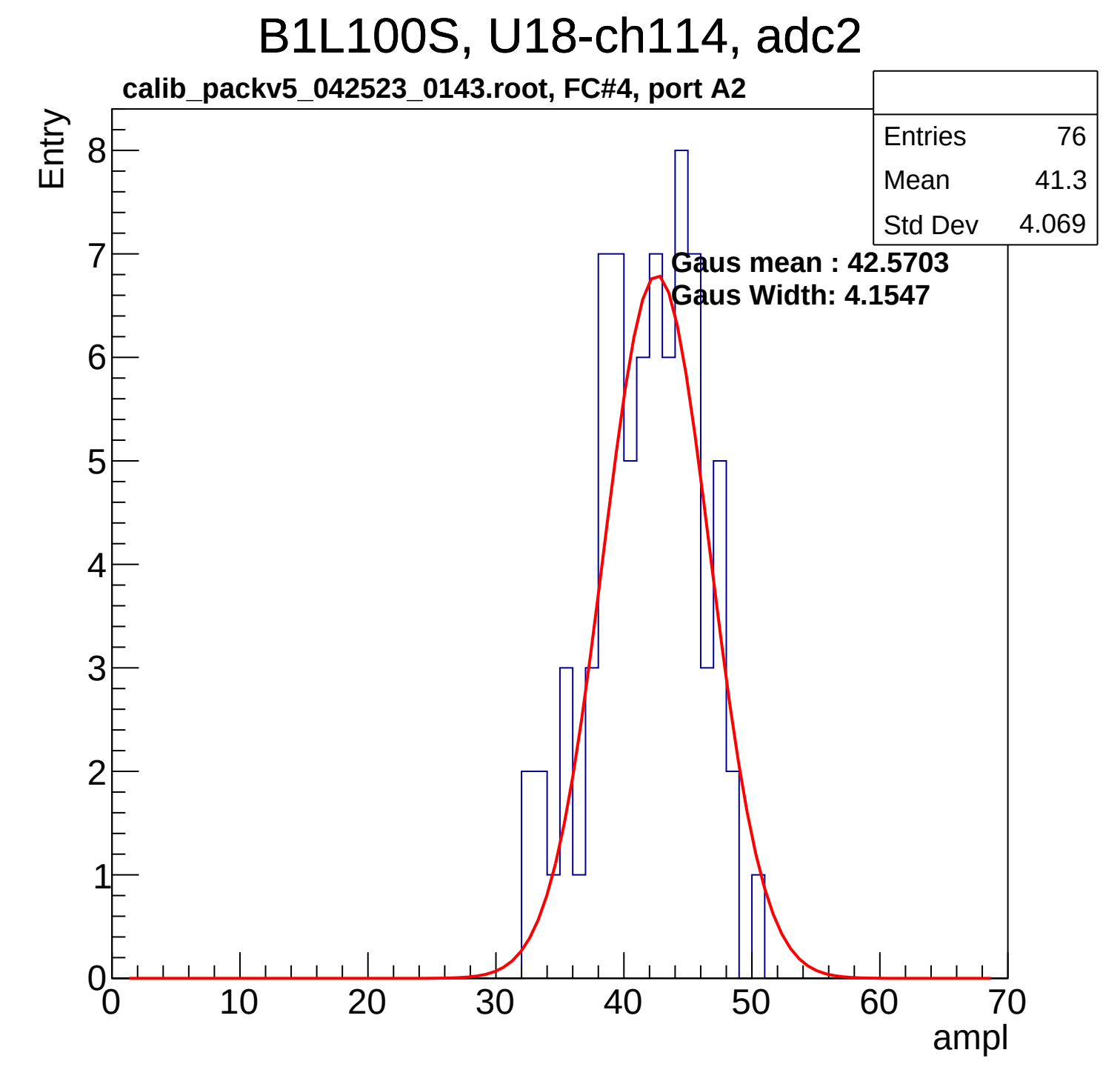

B1L100S, U18-ch113, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 31
Mean 58.32
Std Dev 10.94
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

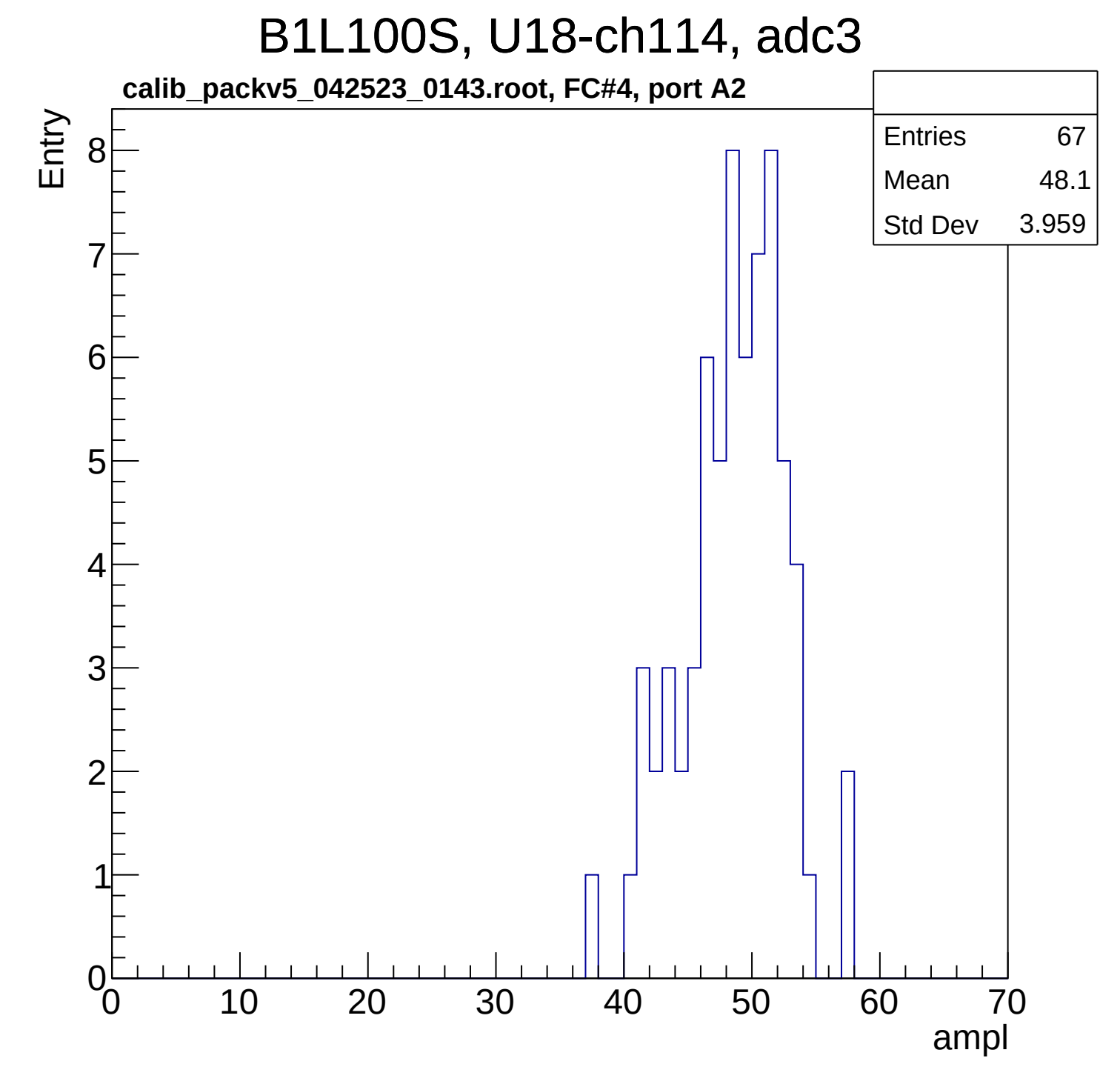

B1L100S, U18-ch113, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 62.5
Std Dev 0.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

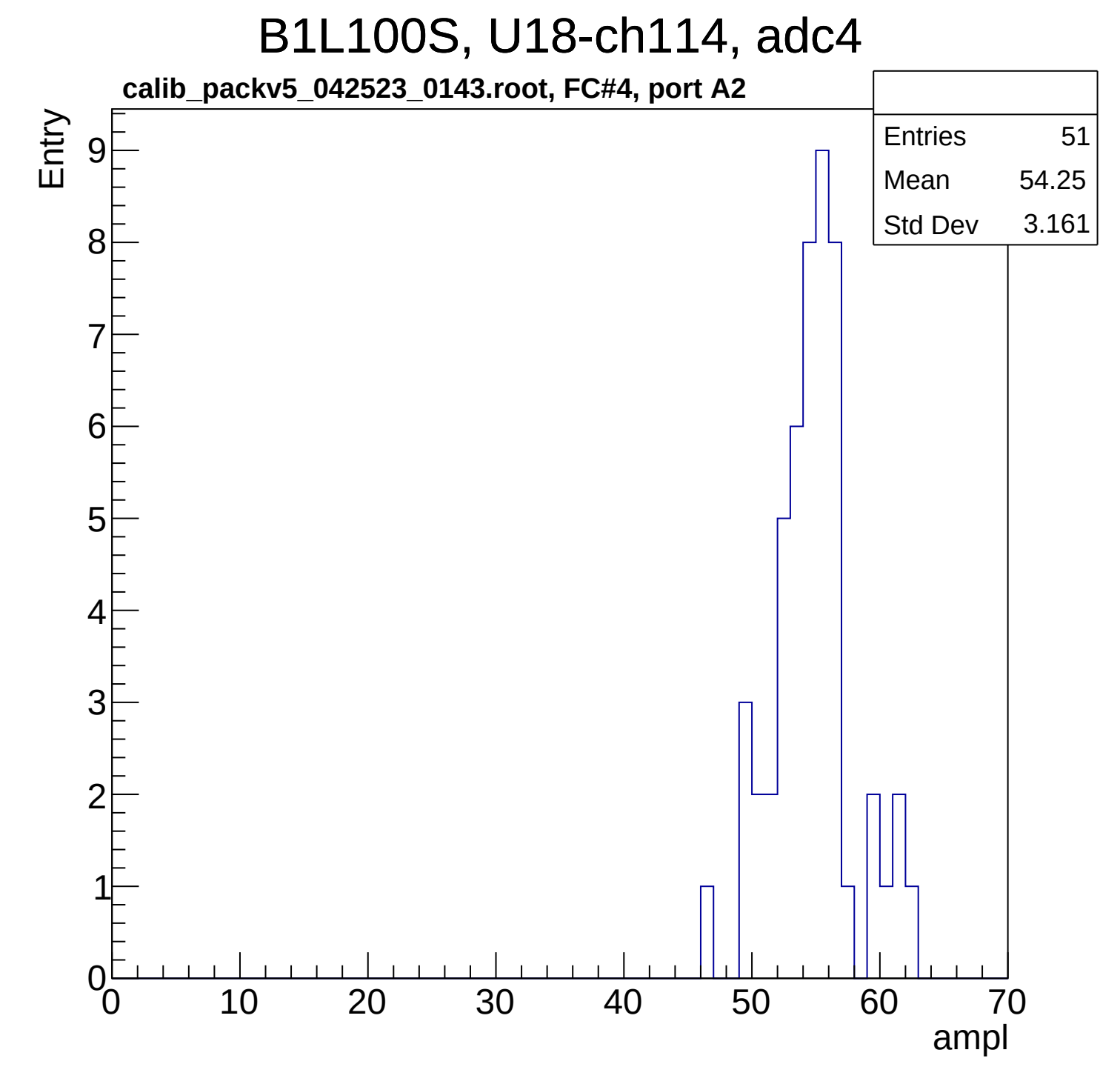

B1L100S, U18-ch113, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 23
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

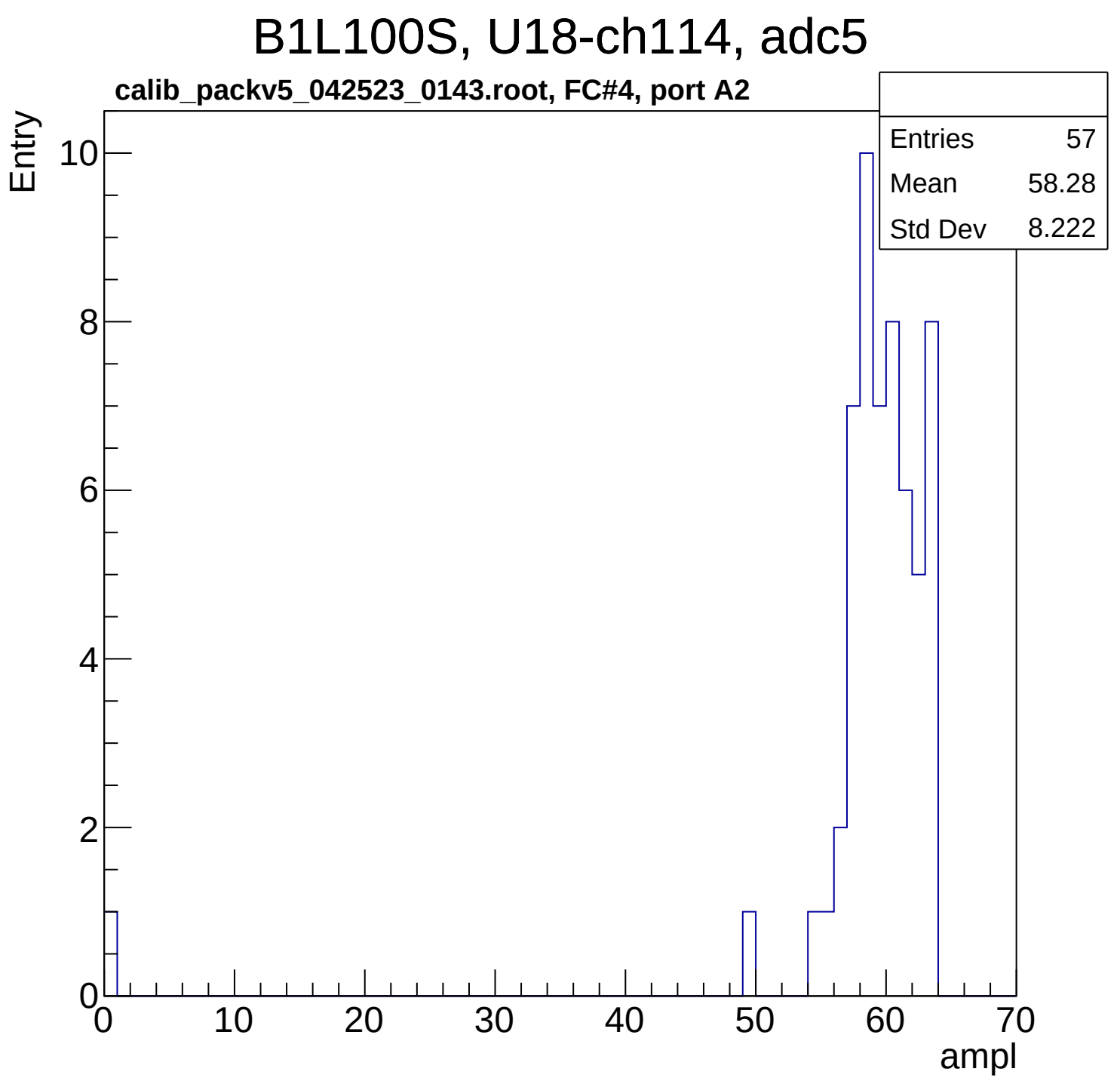

B1L100S, U18-ch114, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 98
Mean 27.42
Std Dev 4.89
Gaus mean : 28.4041
Gaus Width: 4.4793
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

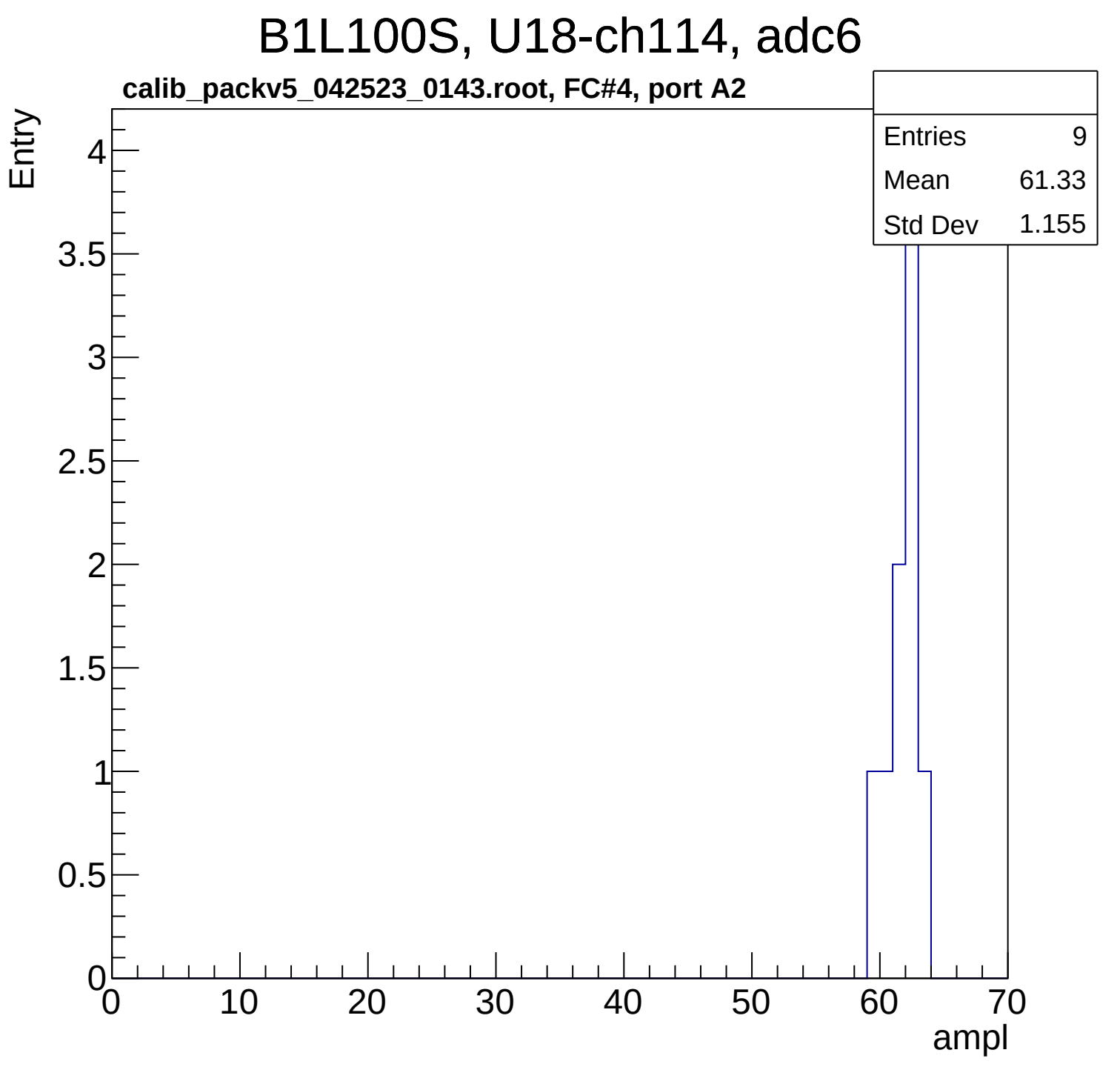

B1L100S, U18-ch114, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 35.73
Std Dev 3.245
Gaus mean : 36.2428
Gaus Width: 3.3884
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

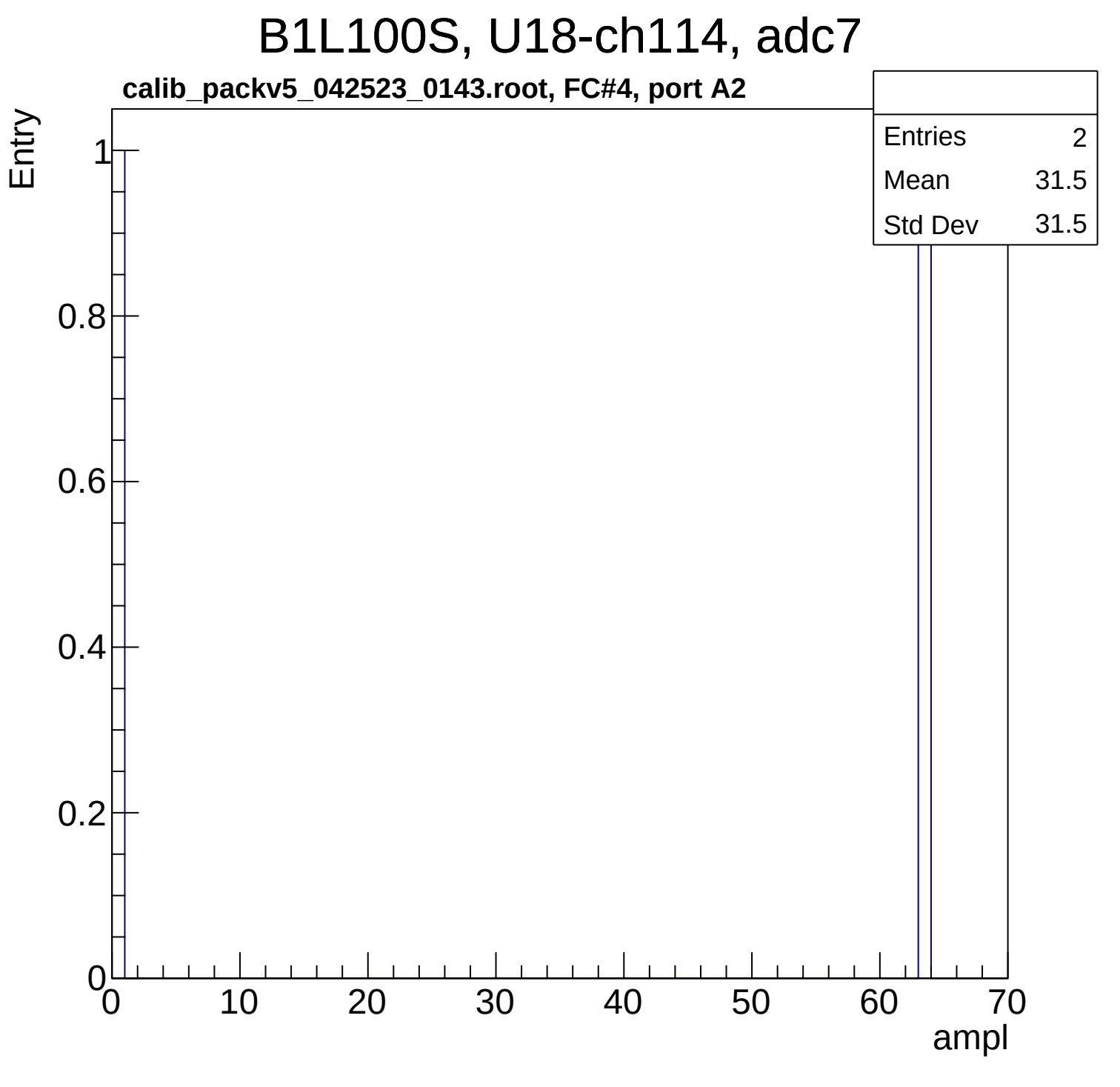

B1L100S, U18-ch114, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 76
Mean 41.3
Std Dev 4.069
Gaus mean : 42.5703
Gaus Width: 4.1547
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

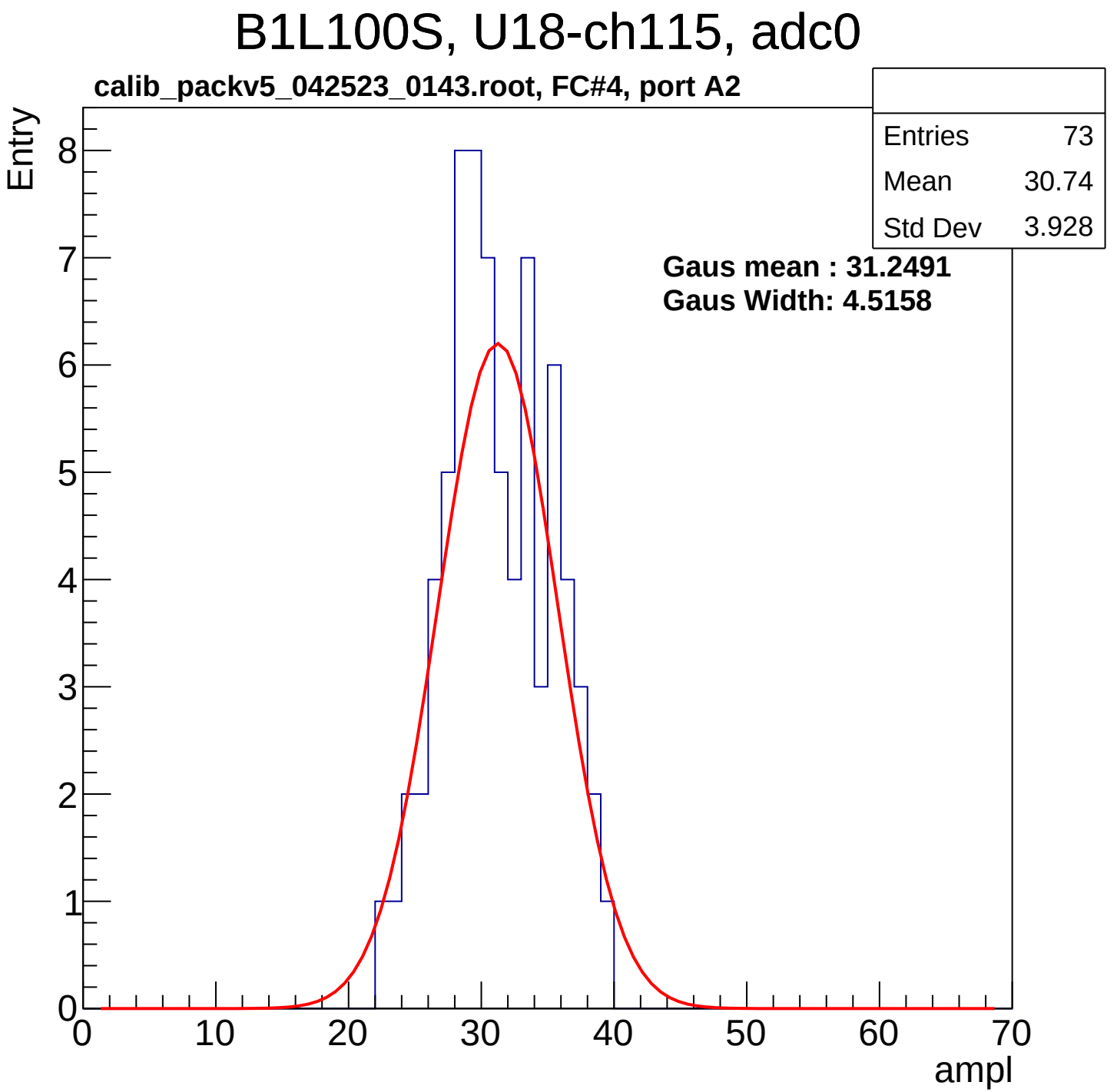

B1L100S, U18-ch114, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 48.1
Std Dev 3.959
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

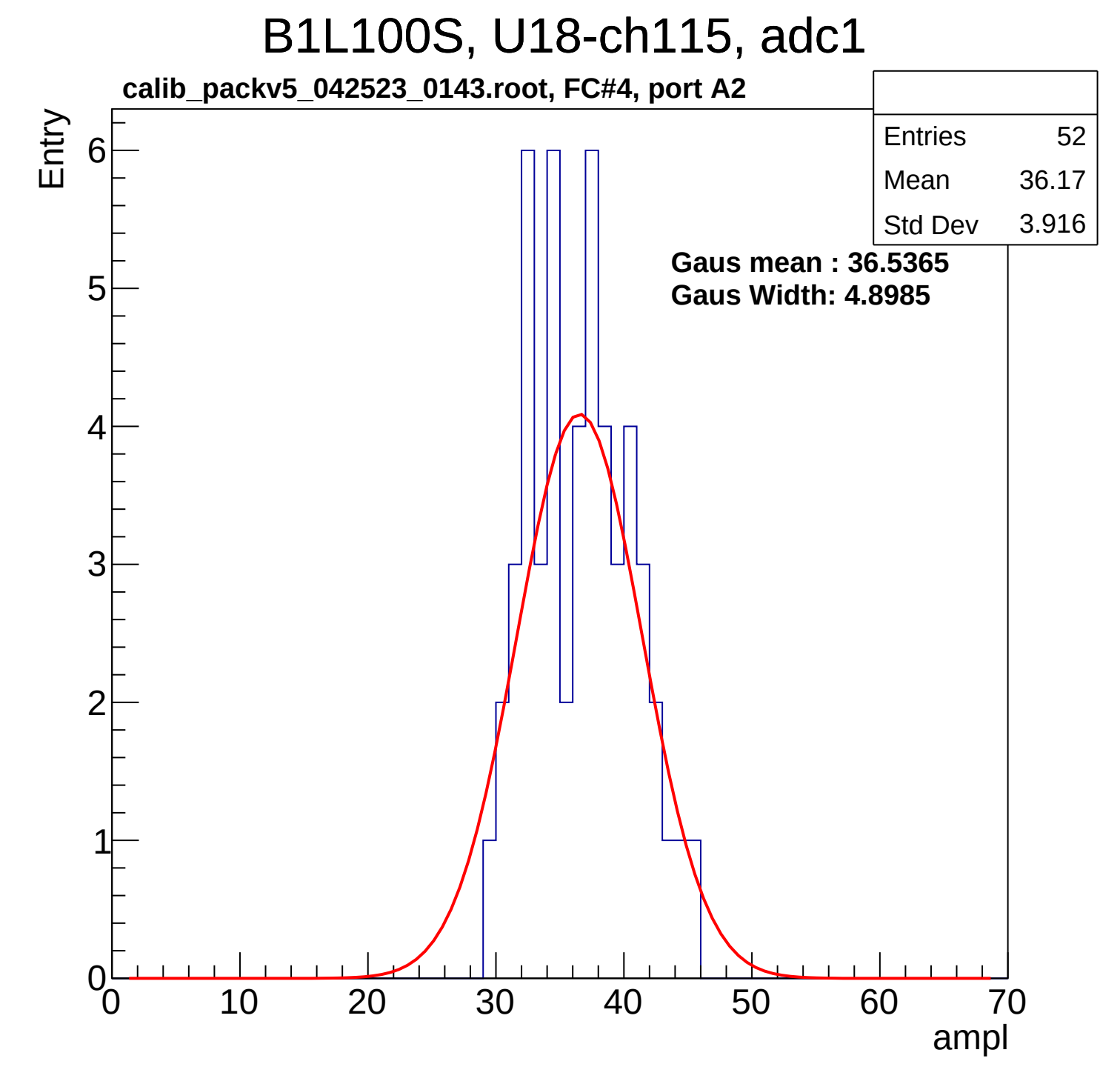

B1L100S, U18-ch114, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 51
Mean 54.25
Std Dev 3.161
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

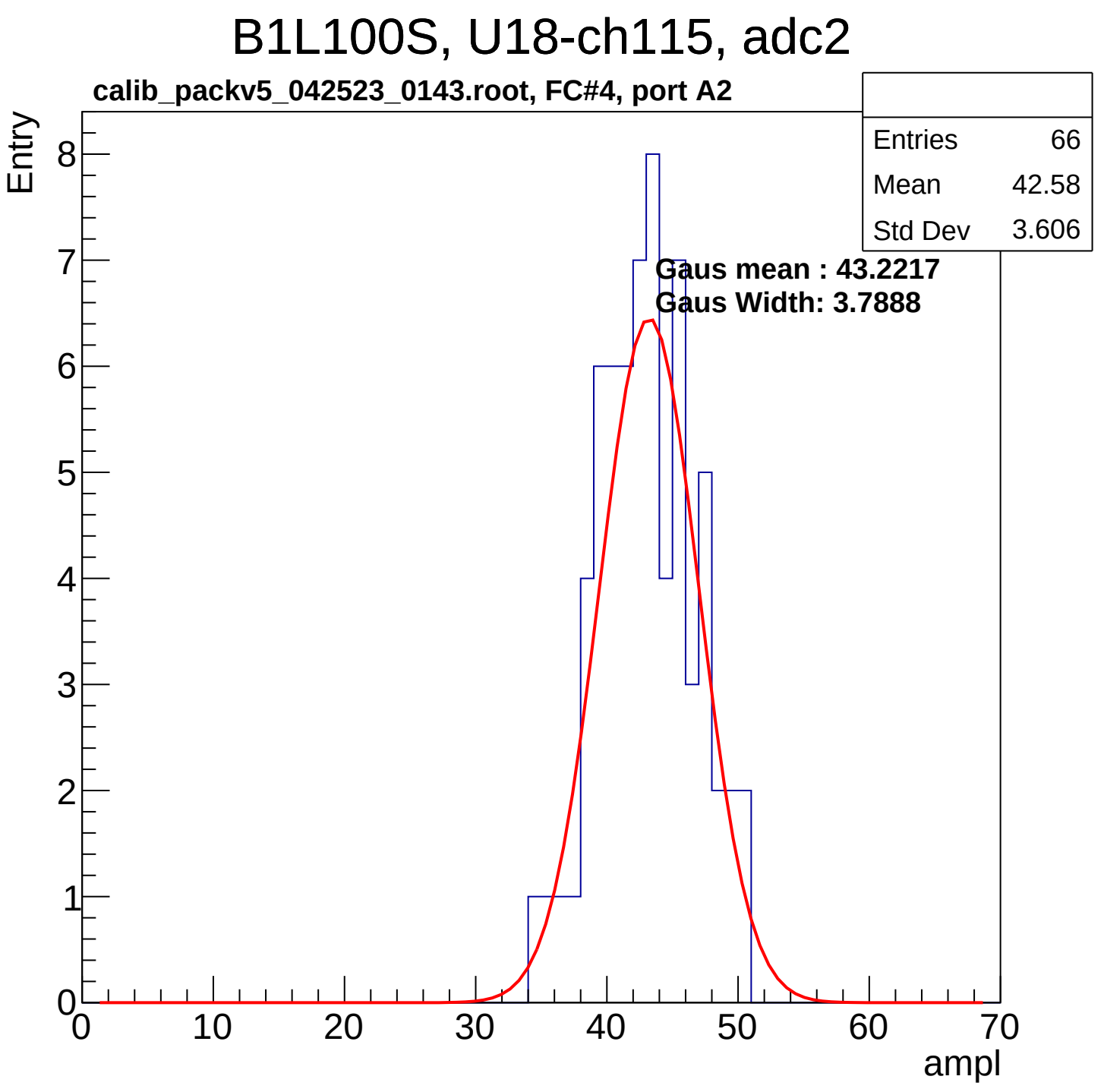

B1L100S, U18-ch114, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 57
Mean 58.28
Std Dev 8.222
Entry
0
2
4
6
8
10
0
10
20
30
40
50
60
70
ampl

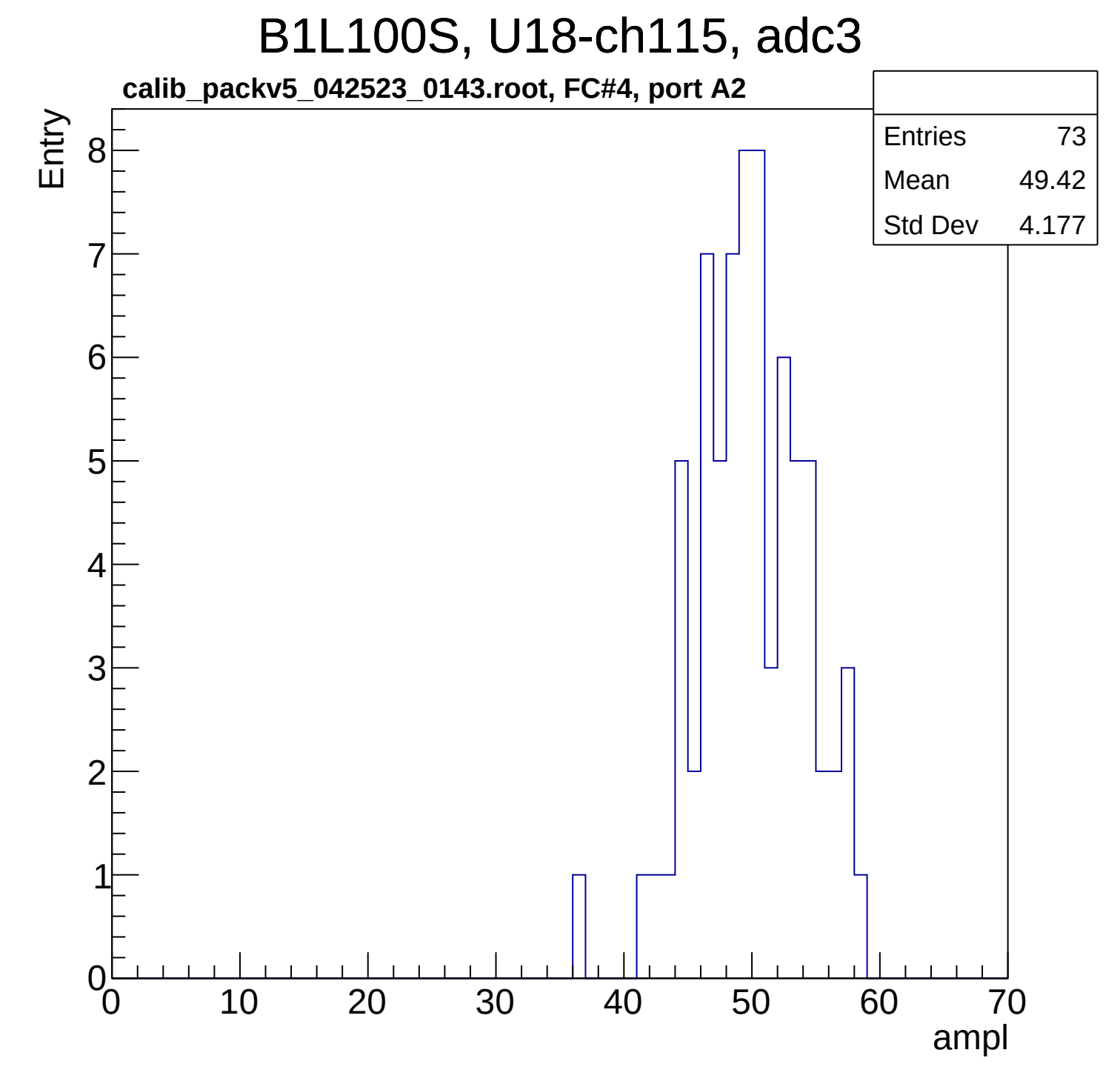

B1L100S, U18-ch114, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 9
Mean 61.33
Std Dev 1.155
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

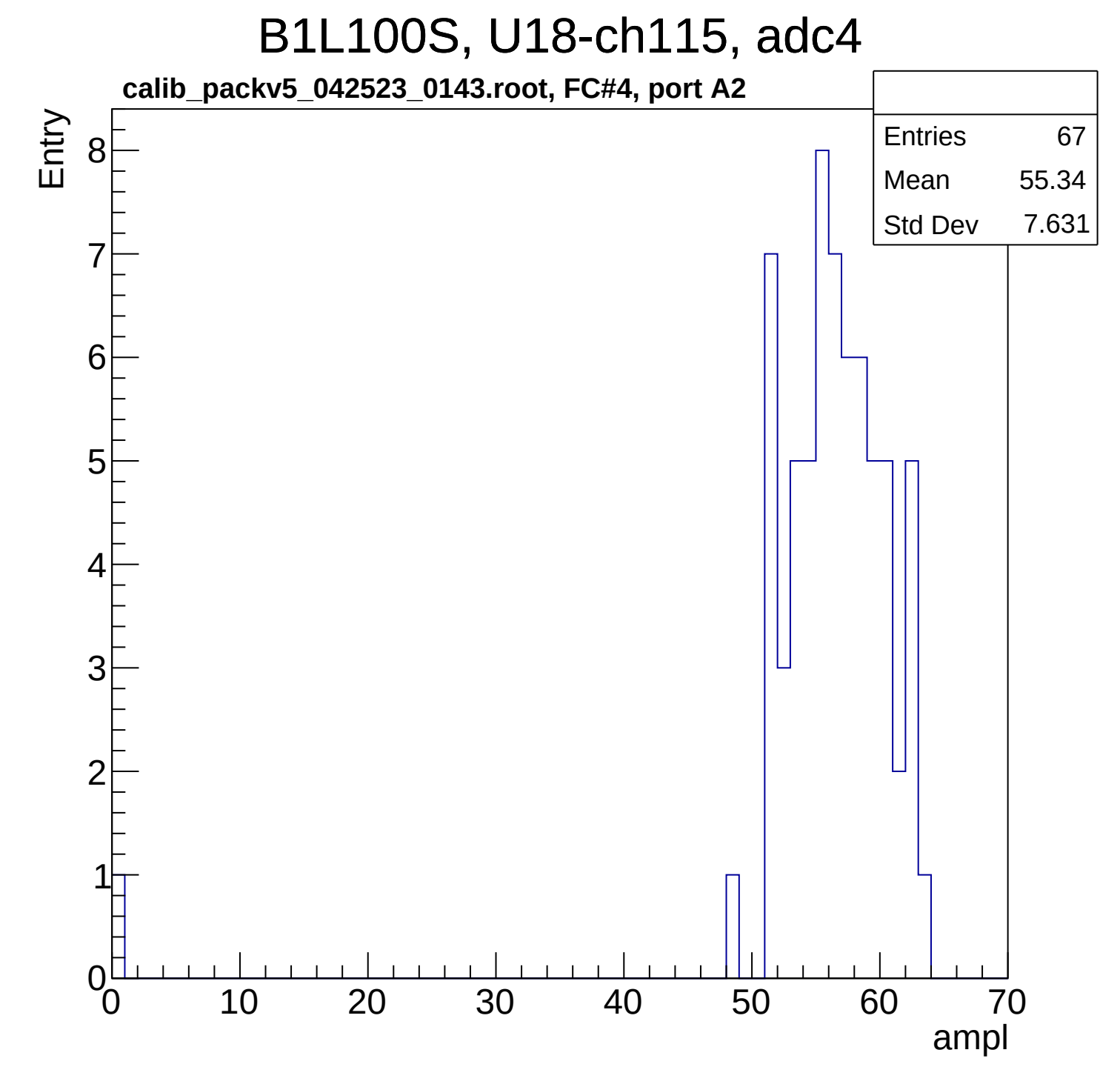

B1L100S, U18-ch114, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 31.5
Std Dev 31.5
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

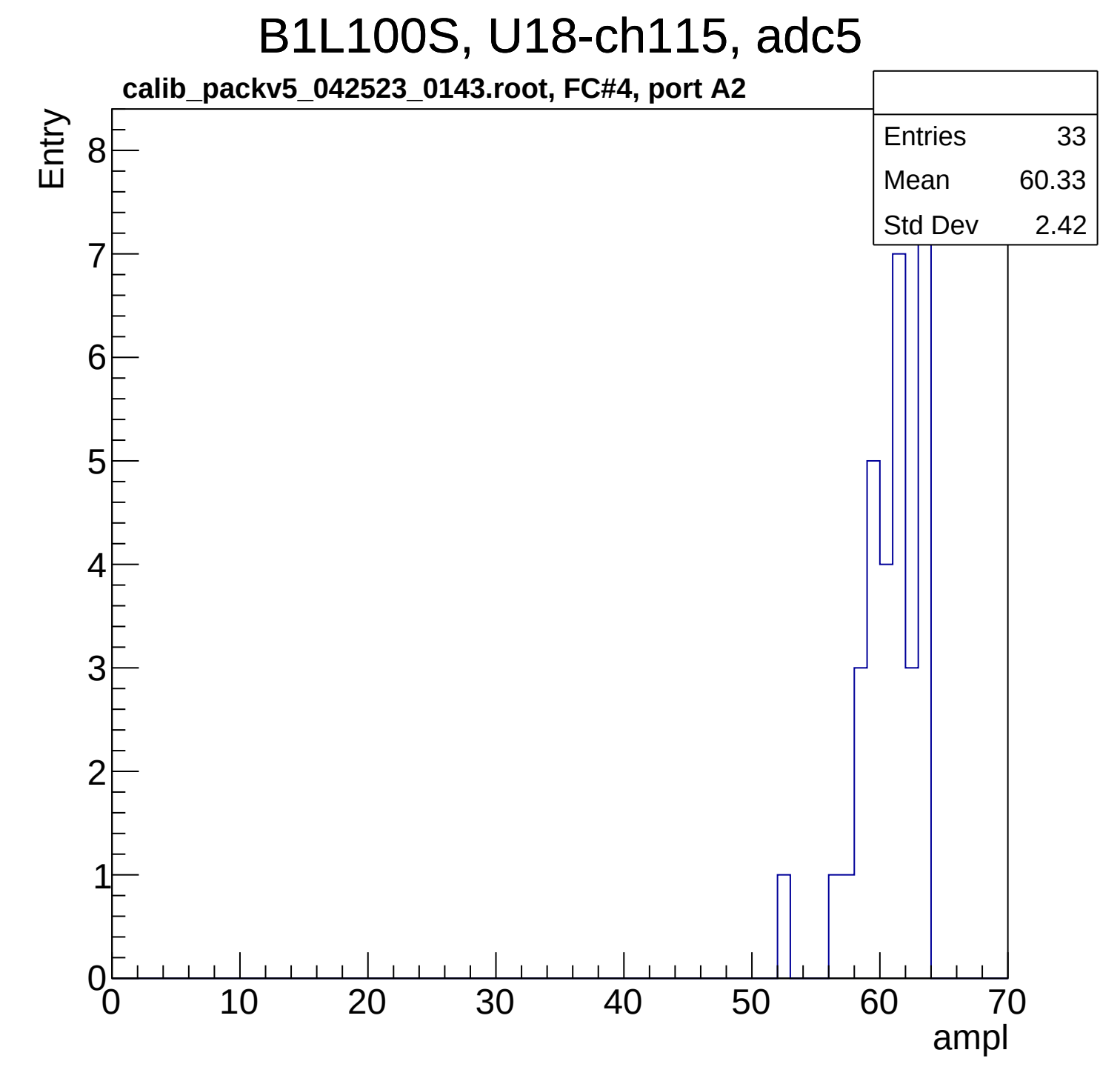

B1L100S, U18-ch115, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 30.74
Std Dev 3.928
Gaus mean : 31.2491
Gaus Width: 4.5158
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

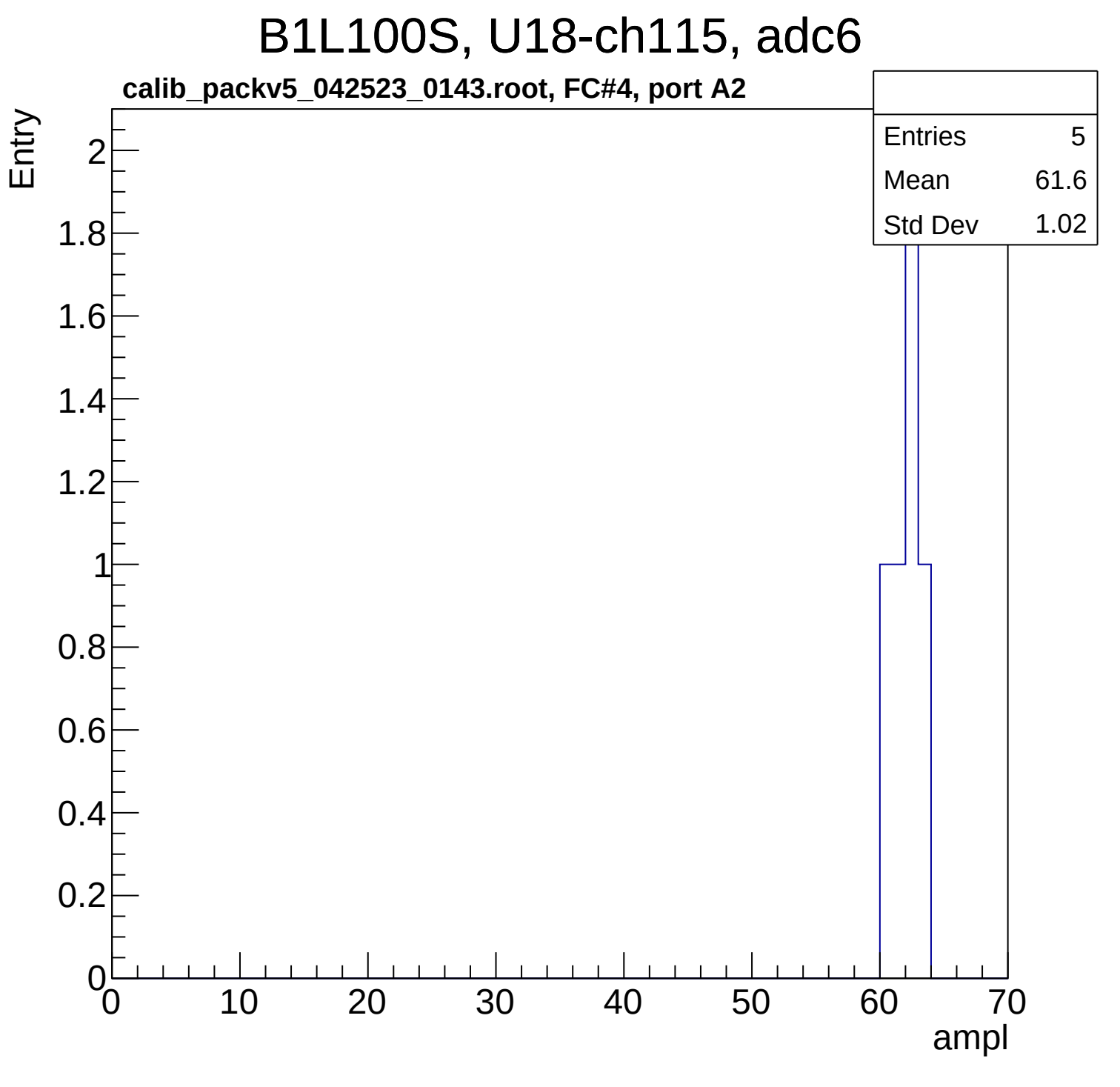

B1L100S, U18-ch115, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 52
Mean 36.17
Std Dev 3.916
Gaus mean : 36.5365
Gaus Width: 4.8985
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

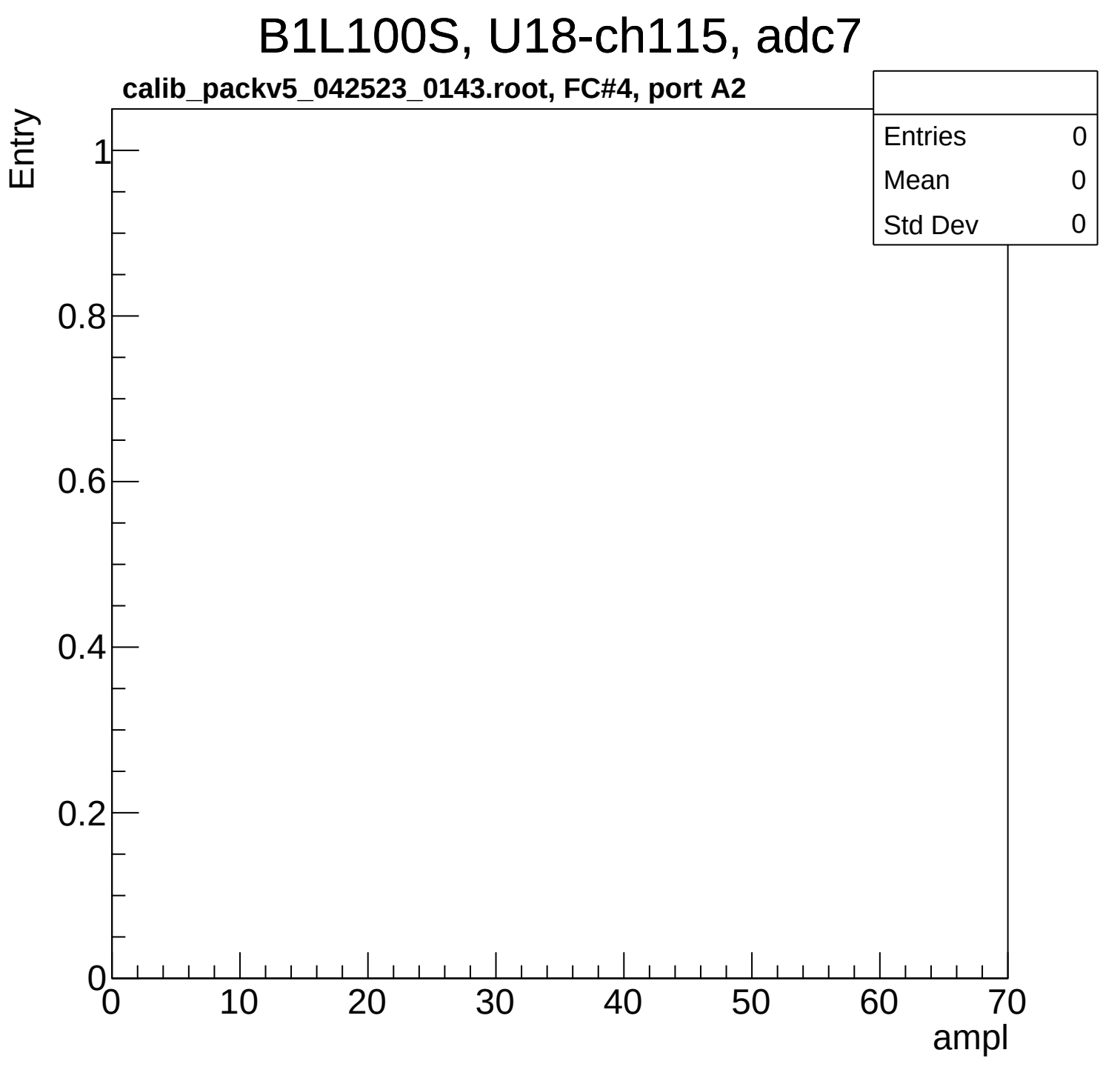

B1L100S, U18-ch115, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 66
Mean 42.58
Std Dev 3.606
Gaus mean : 43.2217
Gaus Width: 3.7888
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

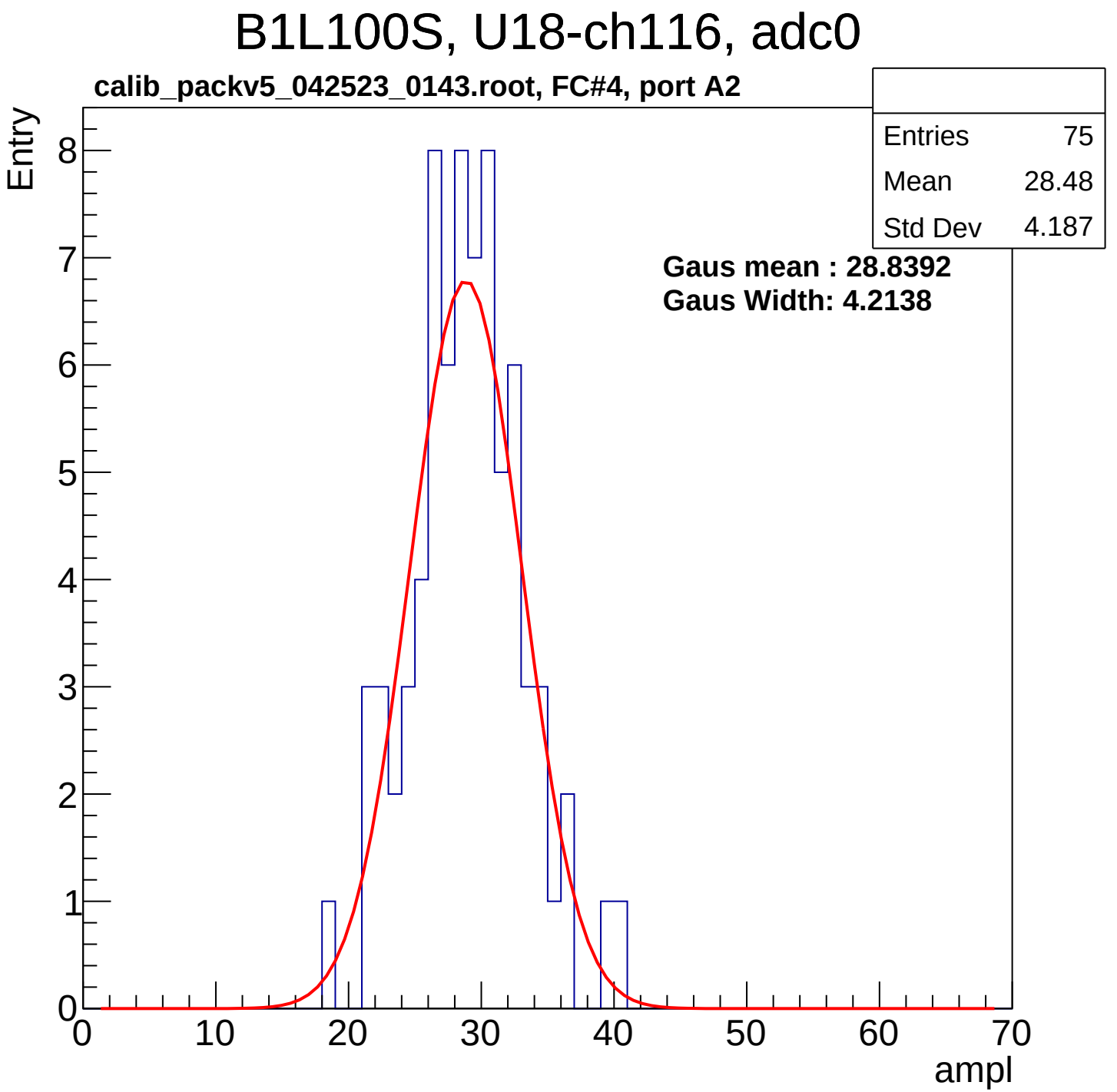

B1L100S, U18-ch115, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 49.42
Std Dev 4.177
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

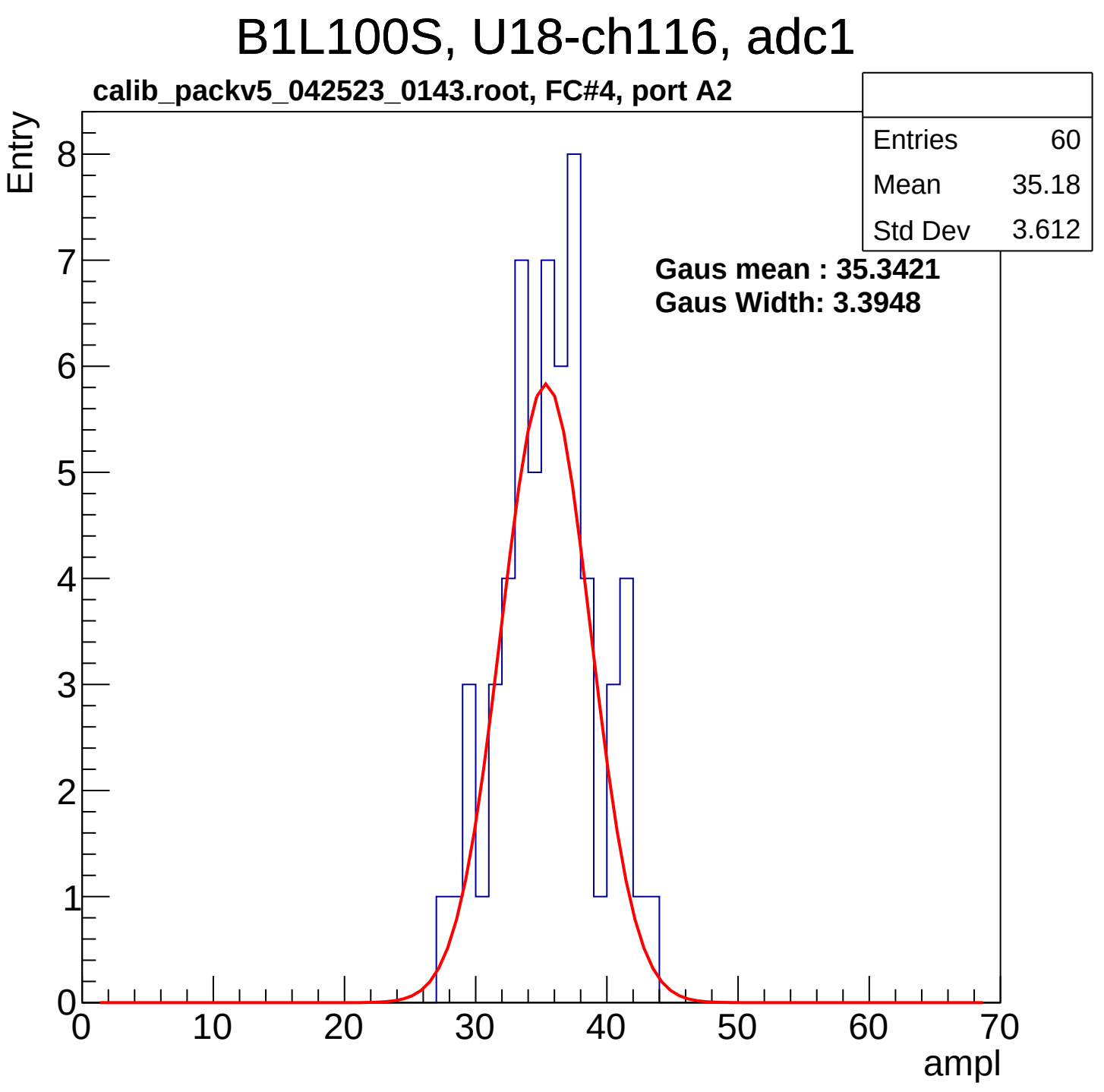

B1L100S, U18-ch115, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 55.34
Std Dev 7.631
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

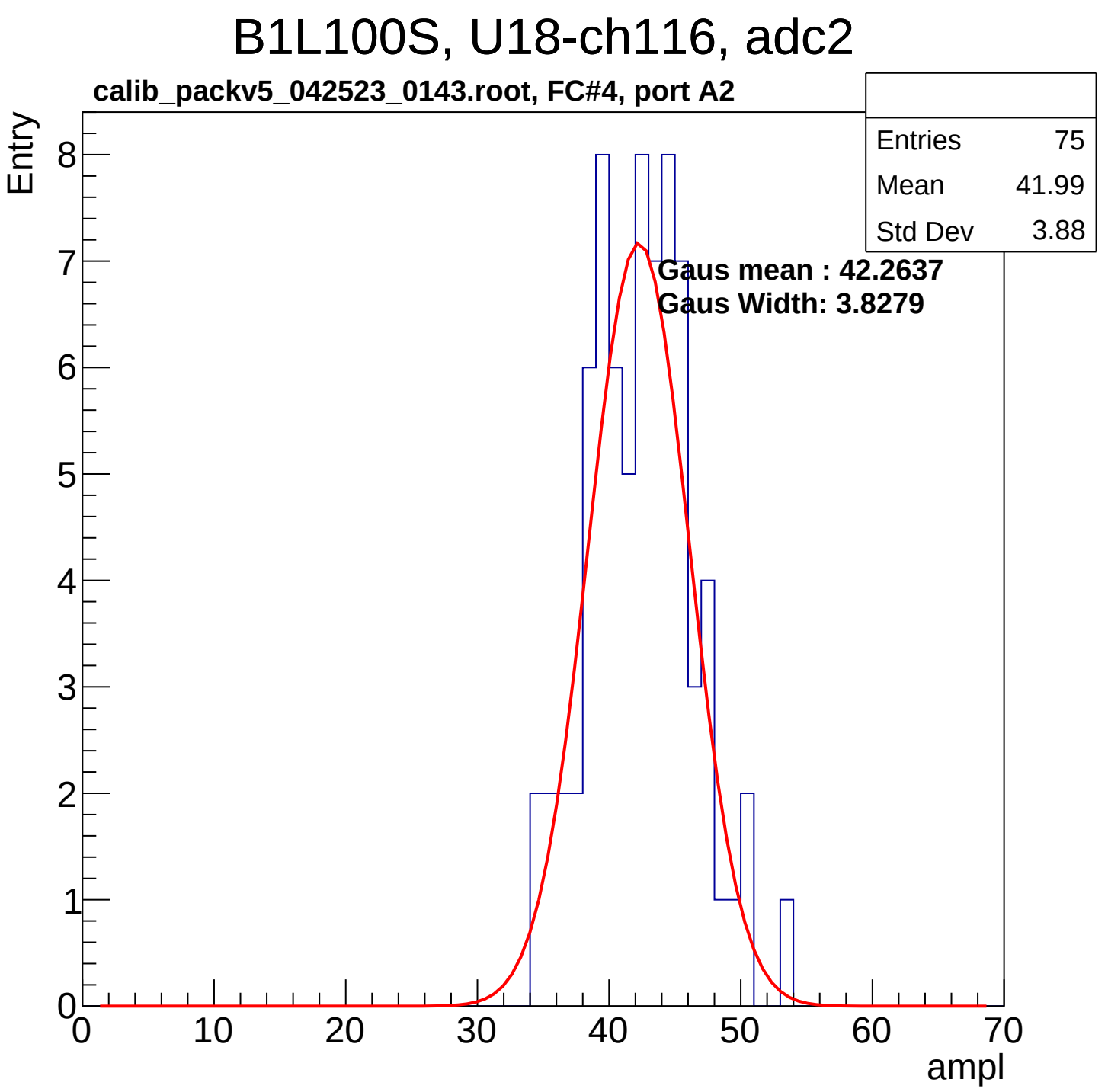

B1L100S, U18-ch115, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 33
Mean 60.33
Std Dev 2.42
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

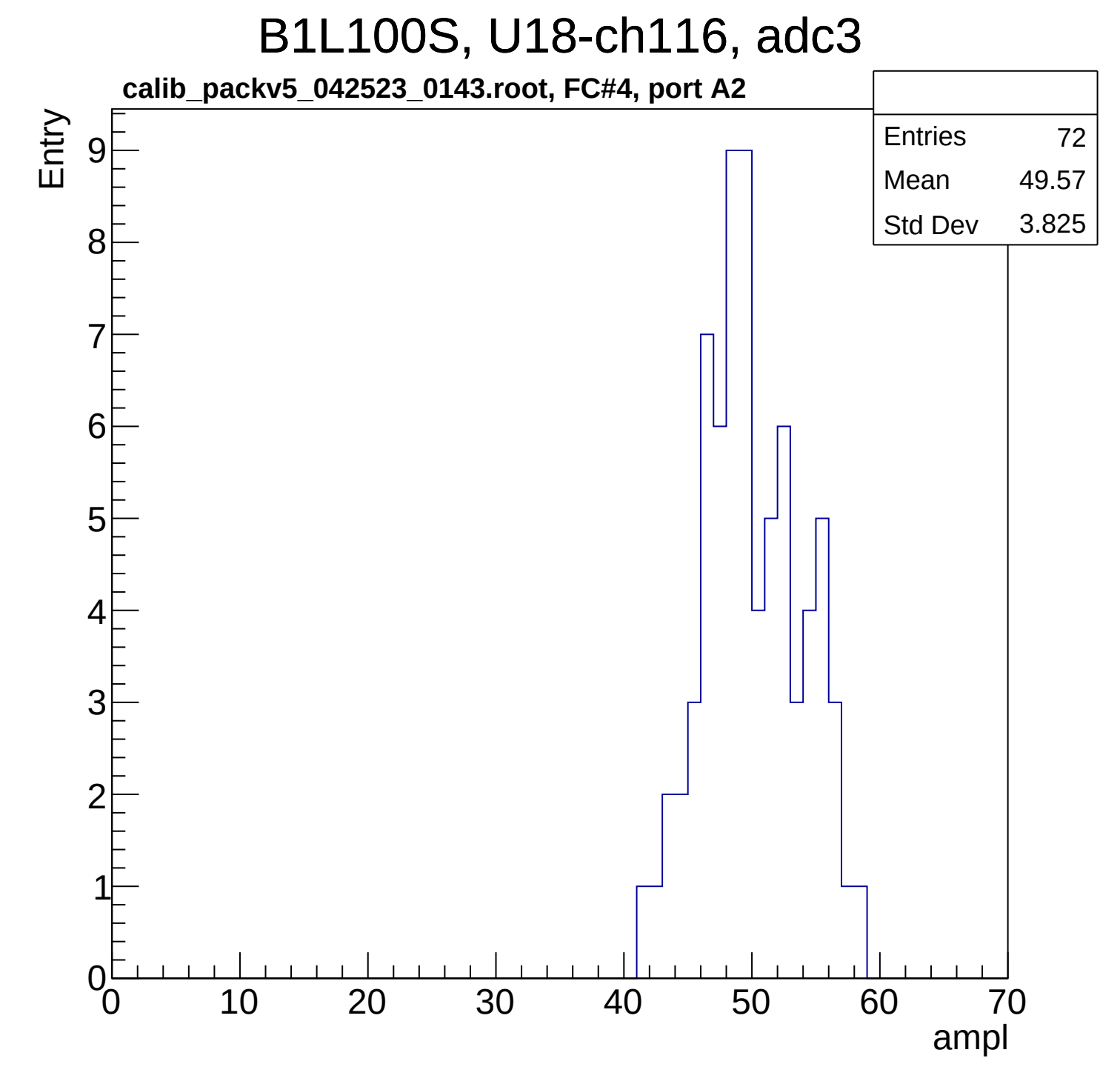

B1L100S, U18-ch115, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 5
Mean 61.6
Std Dev 1.02
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

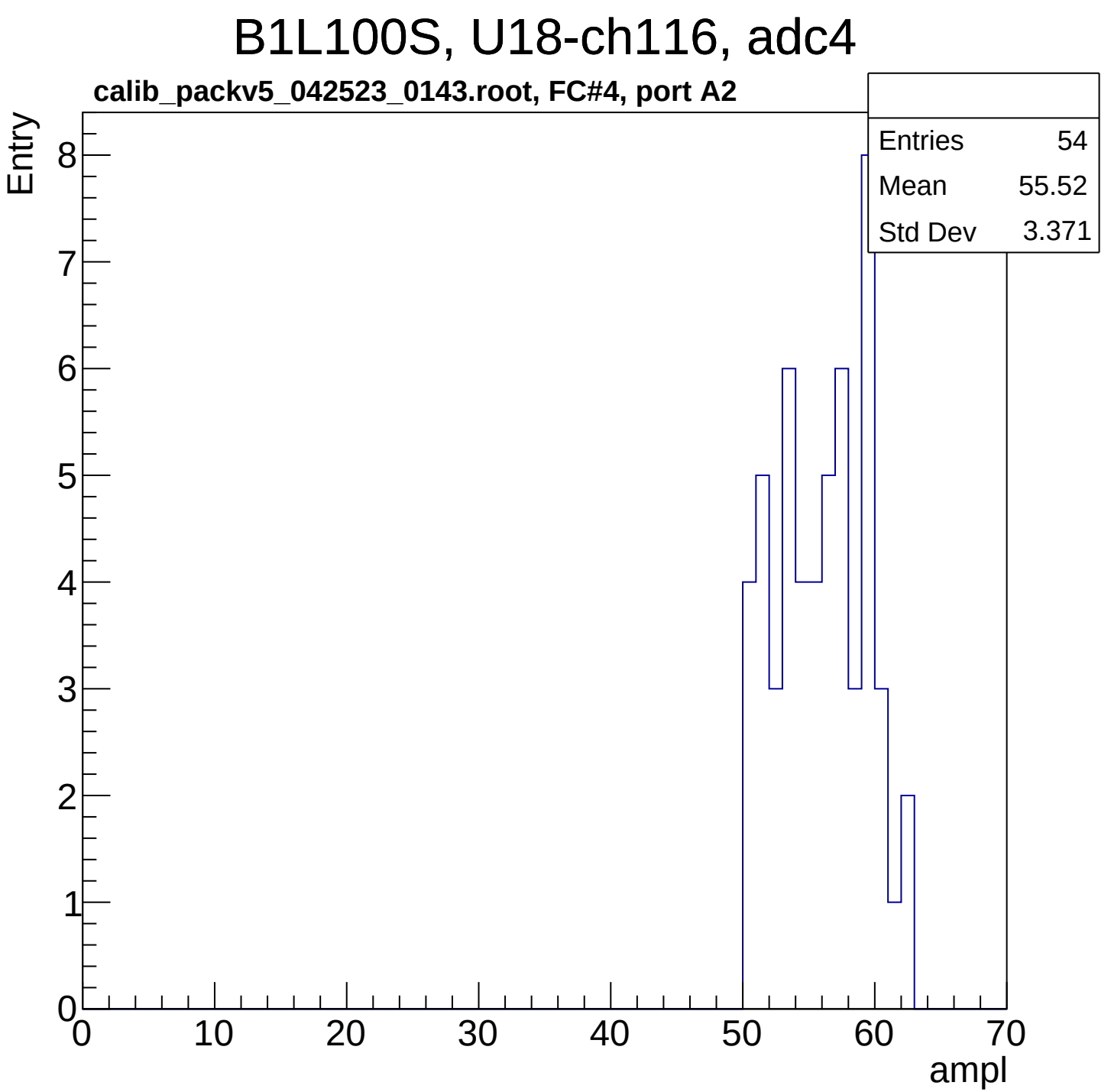

B1L100S, U18-ch115, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

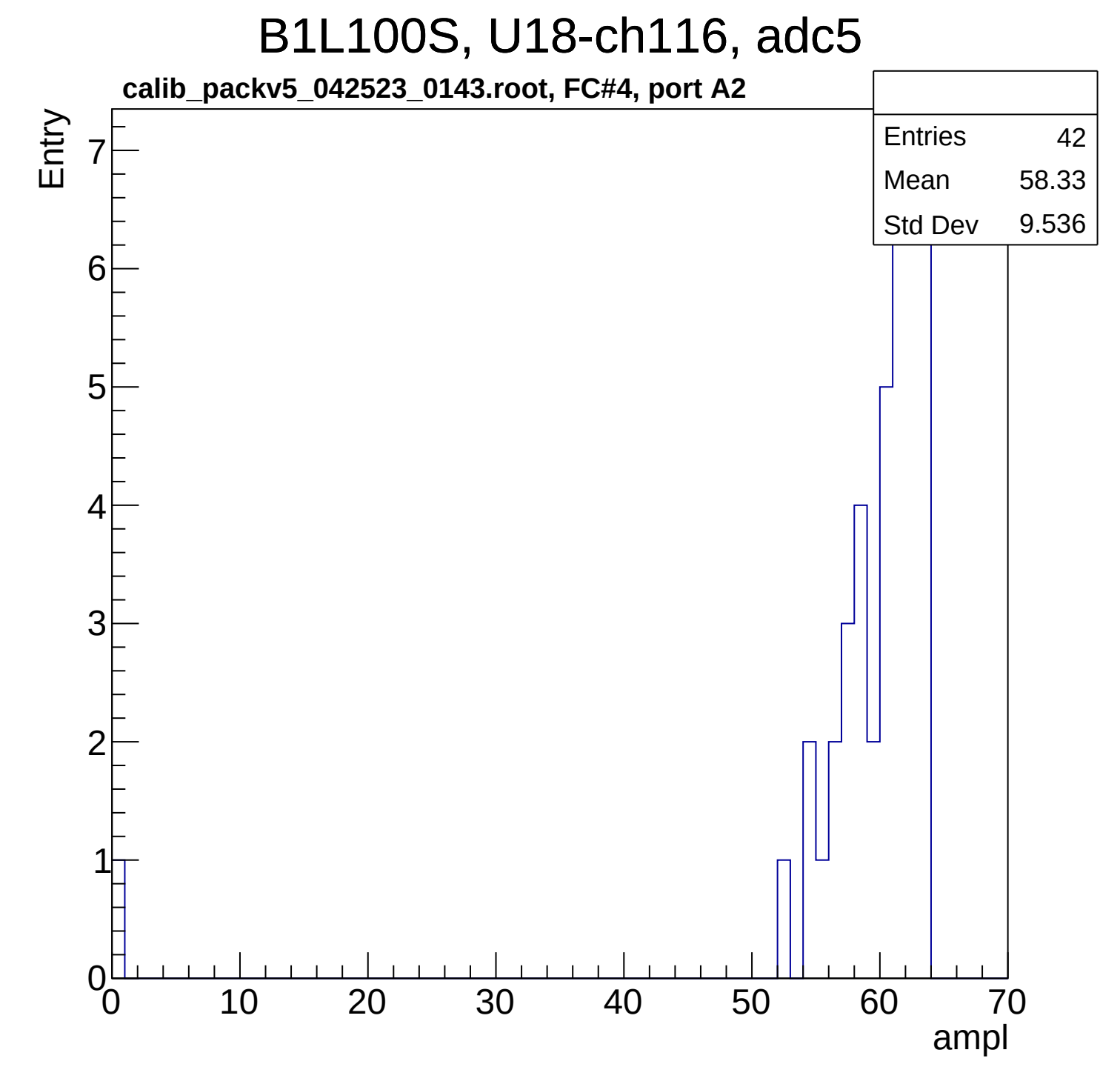

B1L100S, U18-ch116, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 28.48
Std Dev 4.187
Gaus mean : 28.8392
Gaus Width: 4.2138
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

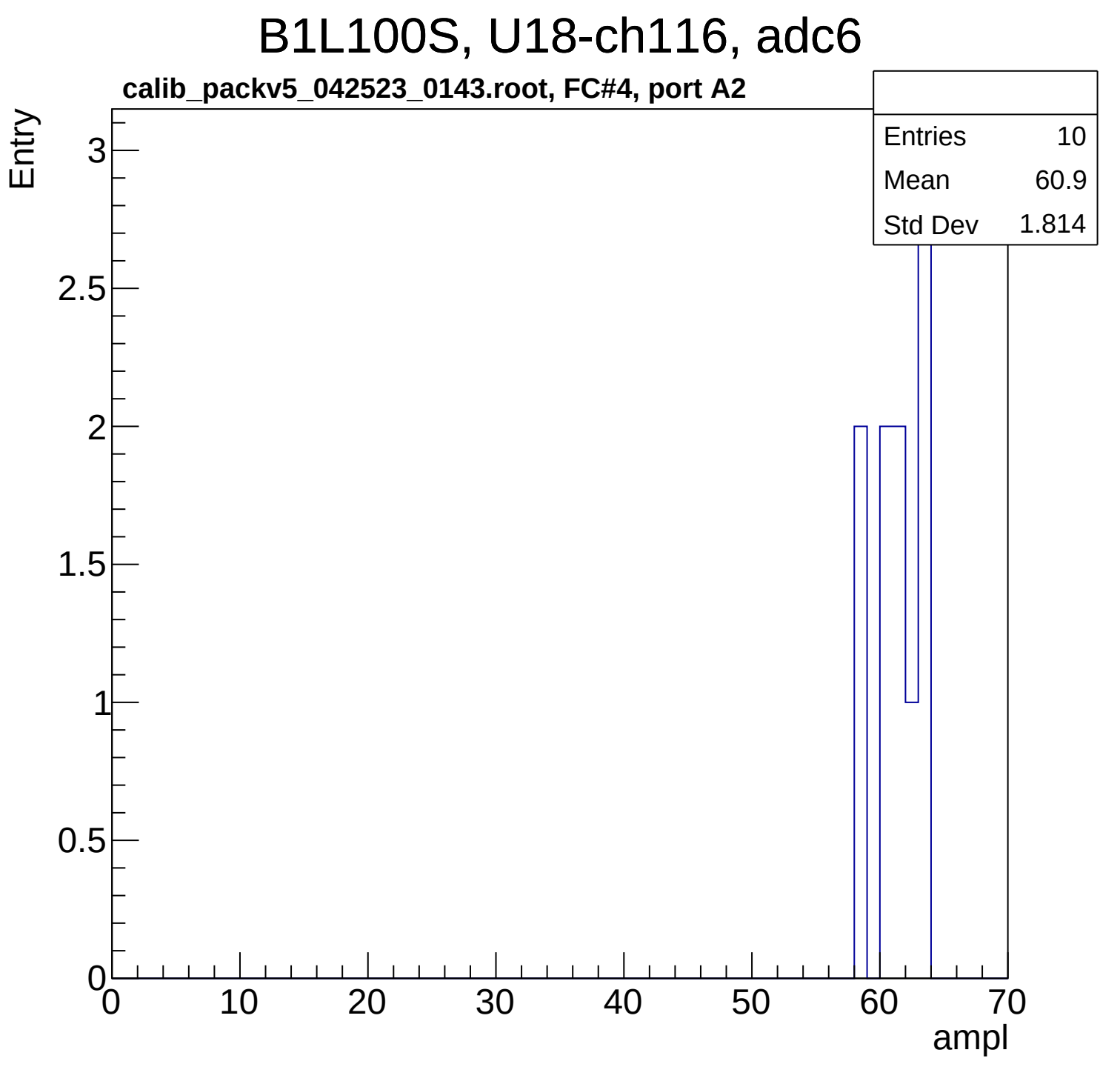

B1L100S, U18-ch116, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 35.18
Std Dev 3.612
Gaus mean : 35.3421
Gaus Width: 3.3948
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

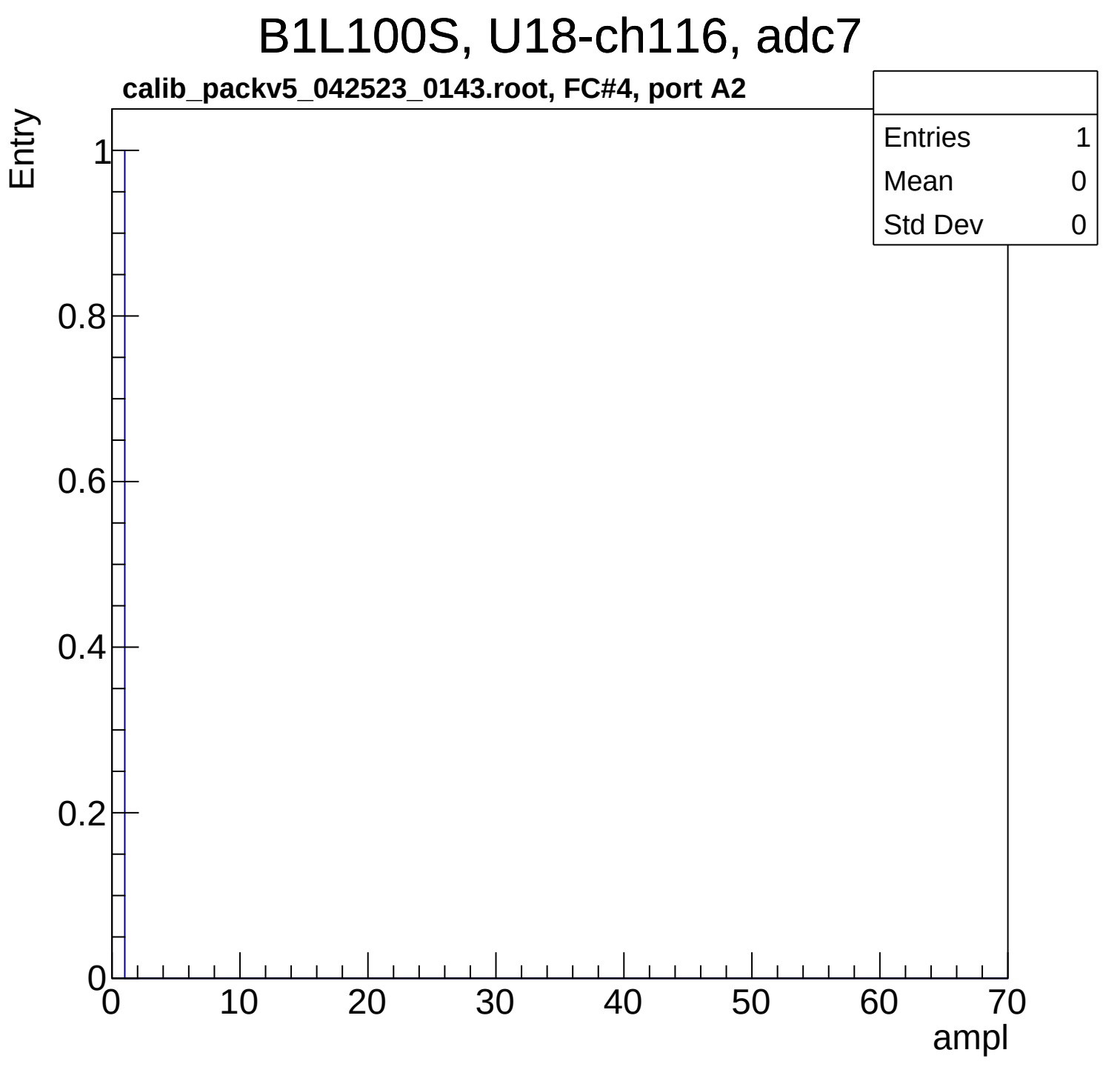

B1L100S, U18-ch116, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 41.99
Std Dev 3.88
Gaus mean : 42.2637
Gaus Width: 3.8279
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

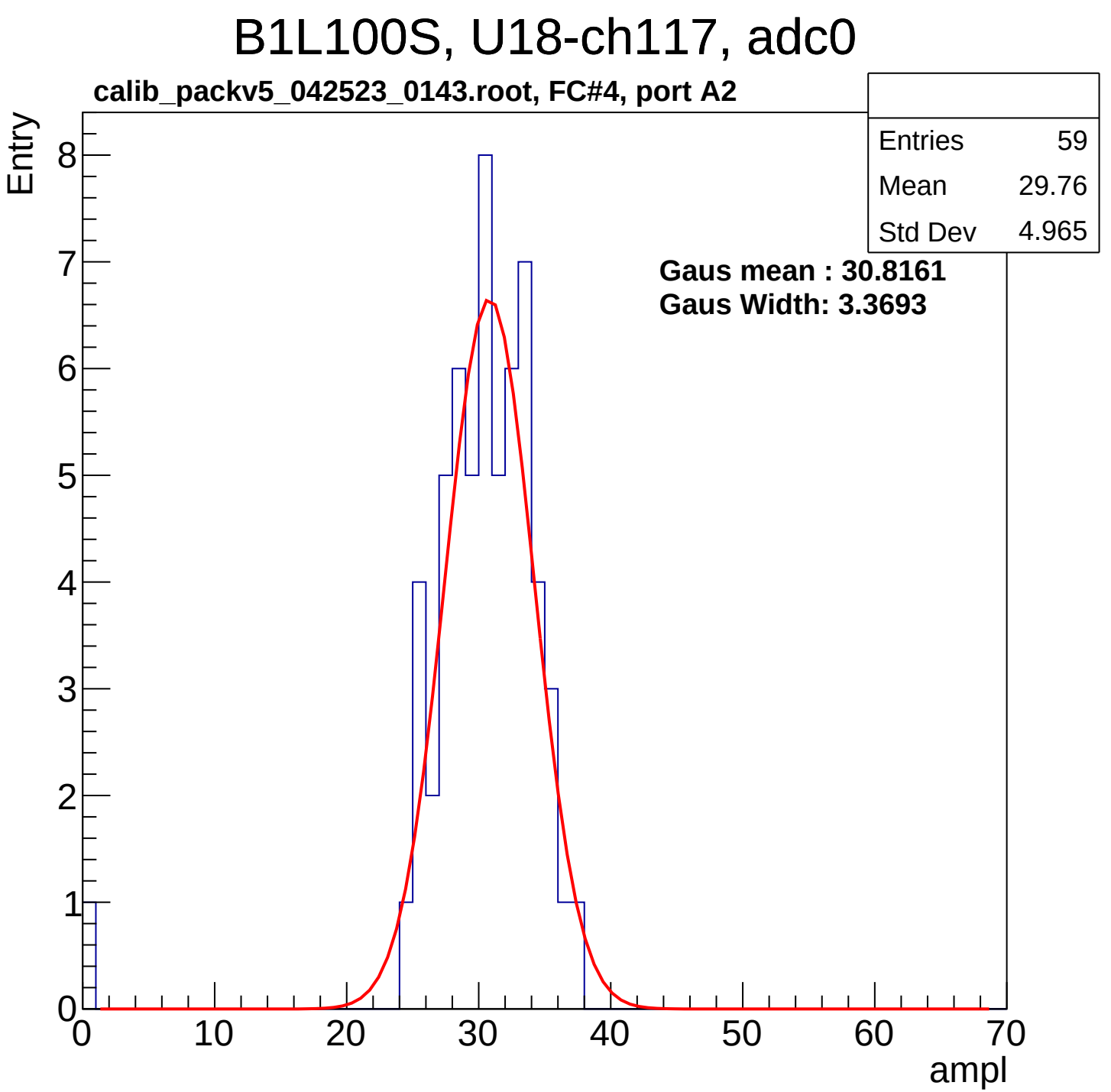

B1L100S, U18-ch116, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 72
Mean 49.57
Std Dev 3.825
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

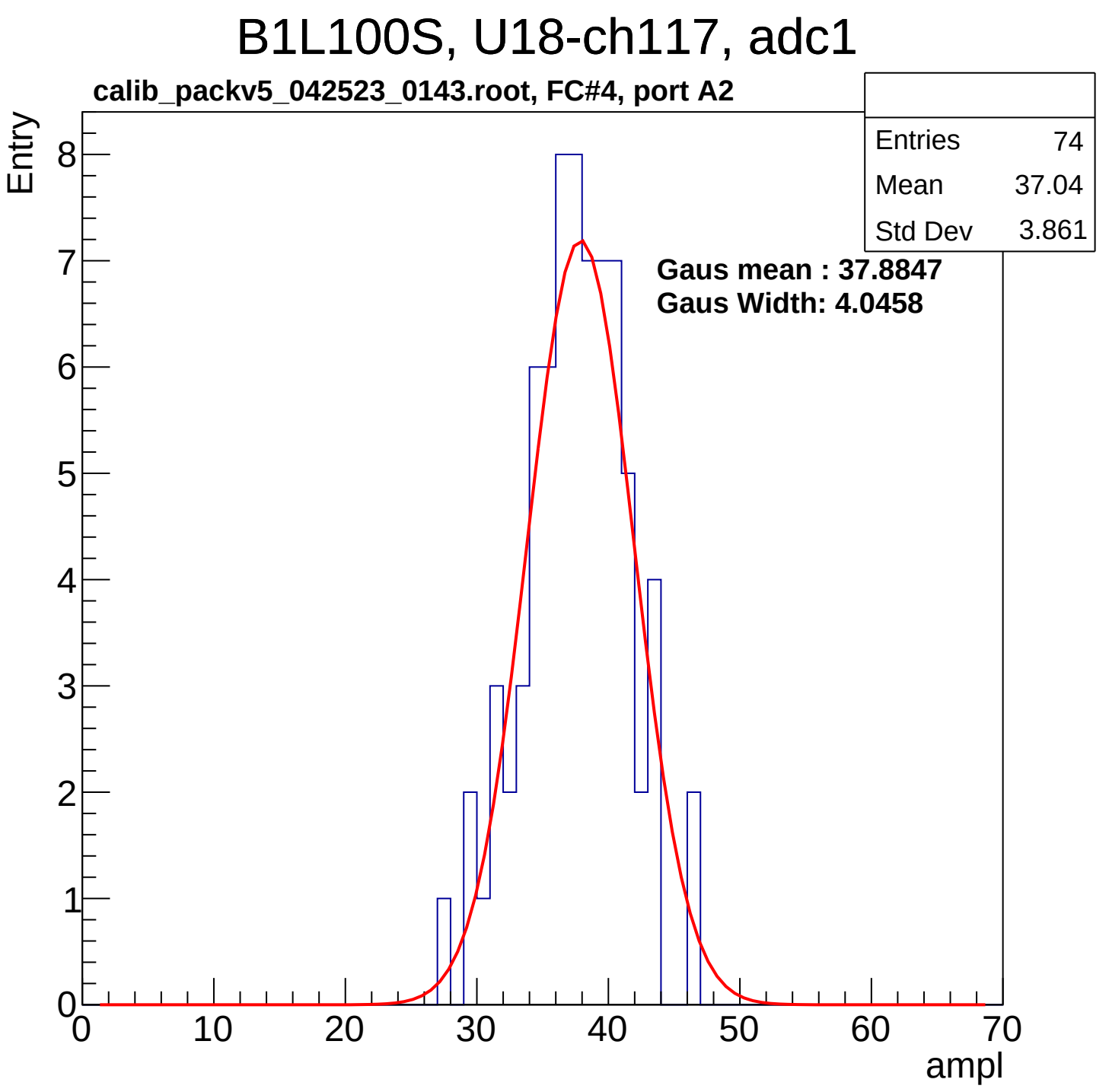

B1L100S, U18-ch116, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 54
Mean 55.52
Std Dev 3.371
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

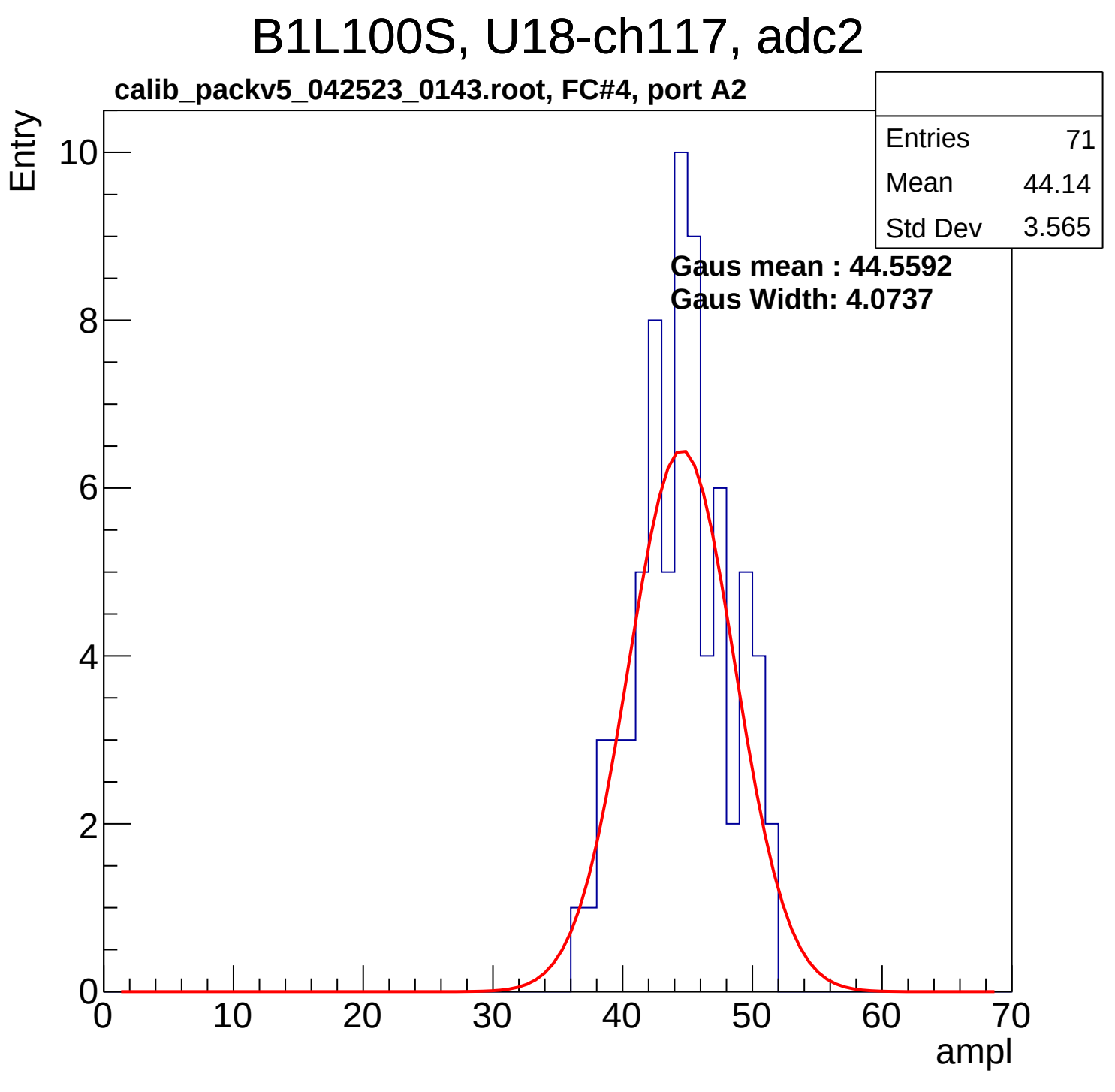

B1L100S, U18-ch116, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 42
Mean 58.33
Std Dev 9.536
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

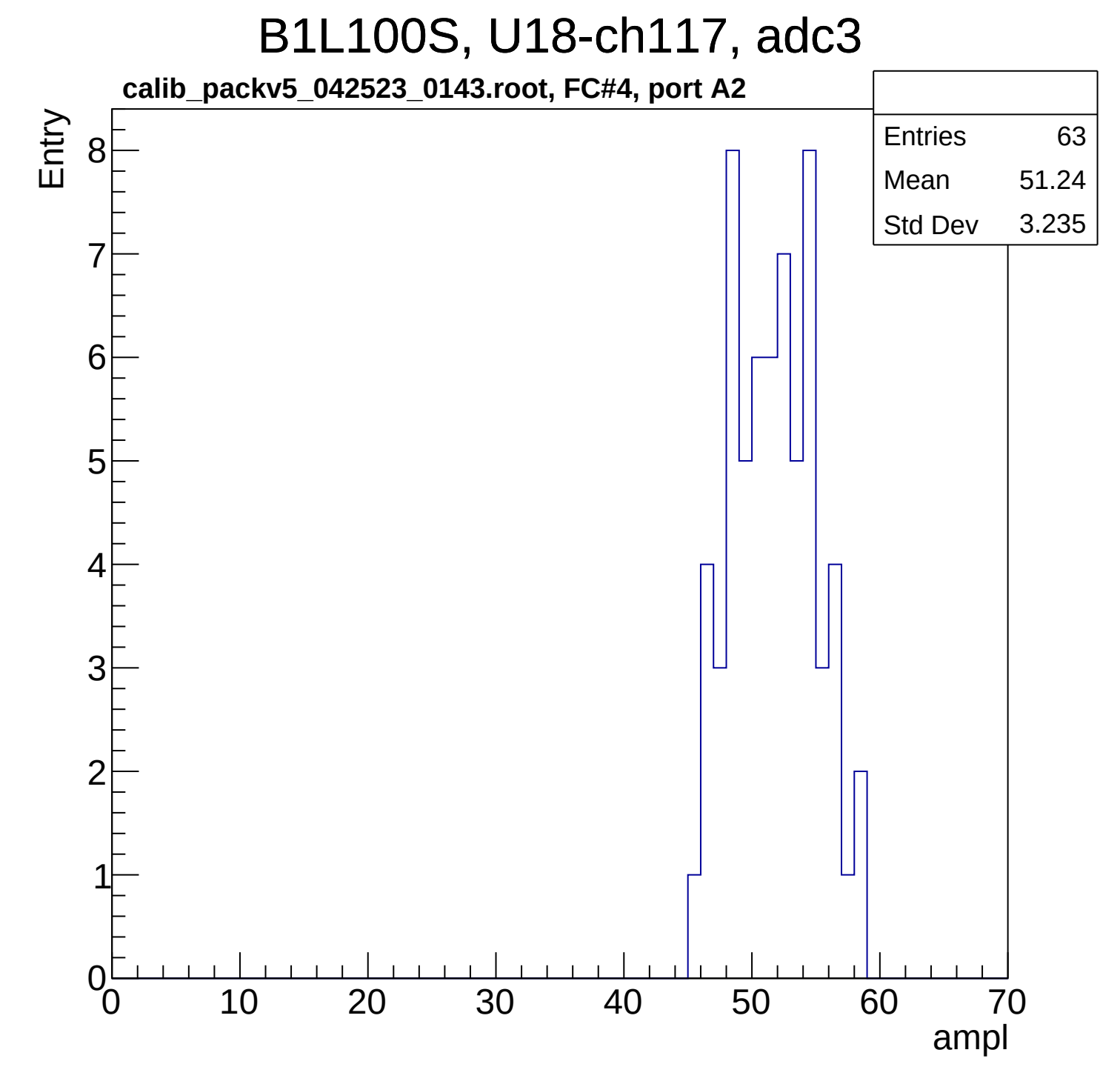

B1L100S, U18-ch116, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 60.9
Std Dev 1.814
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

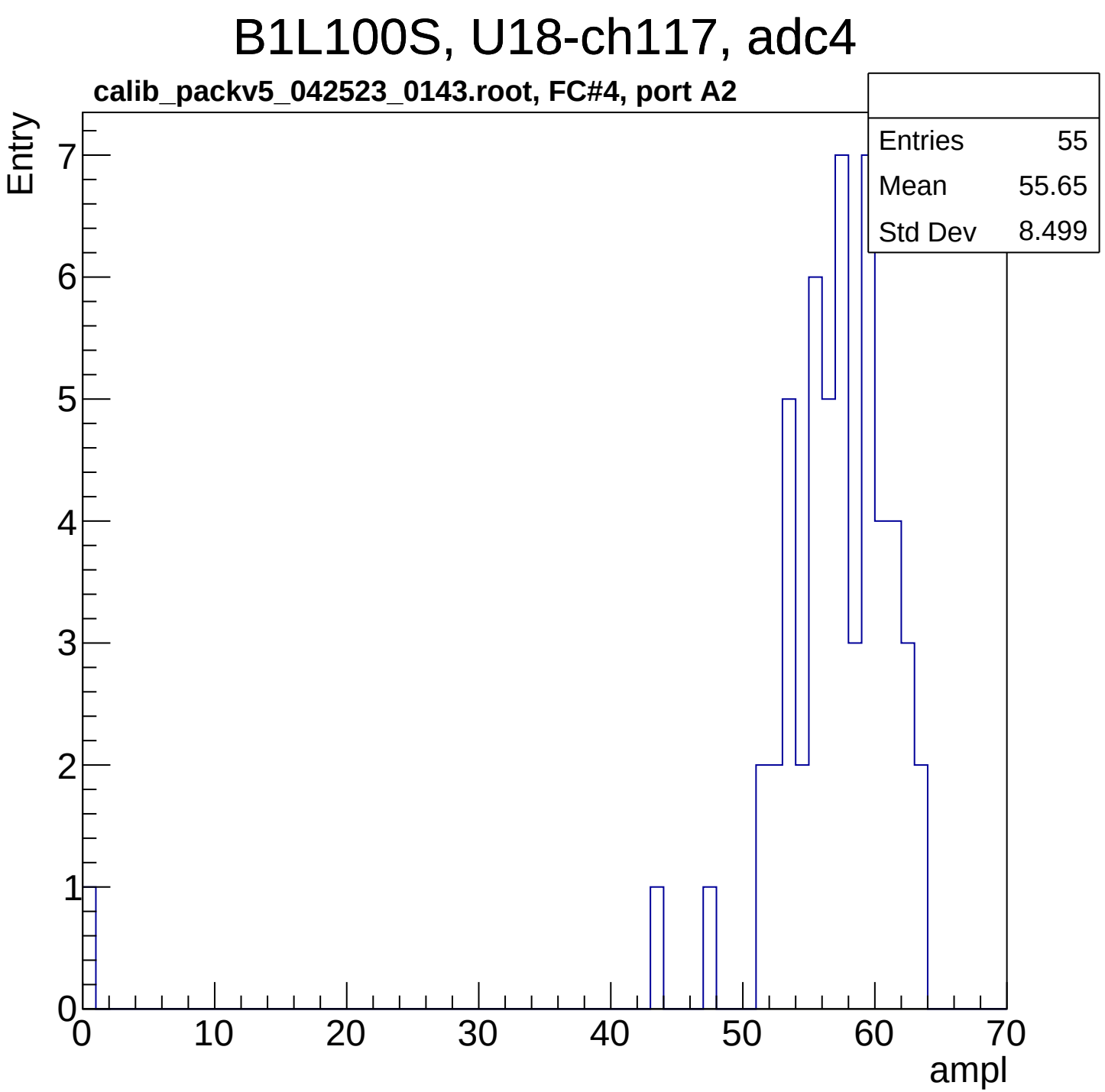

B1L100S, U18-ch116, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

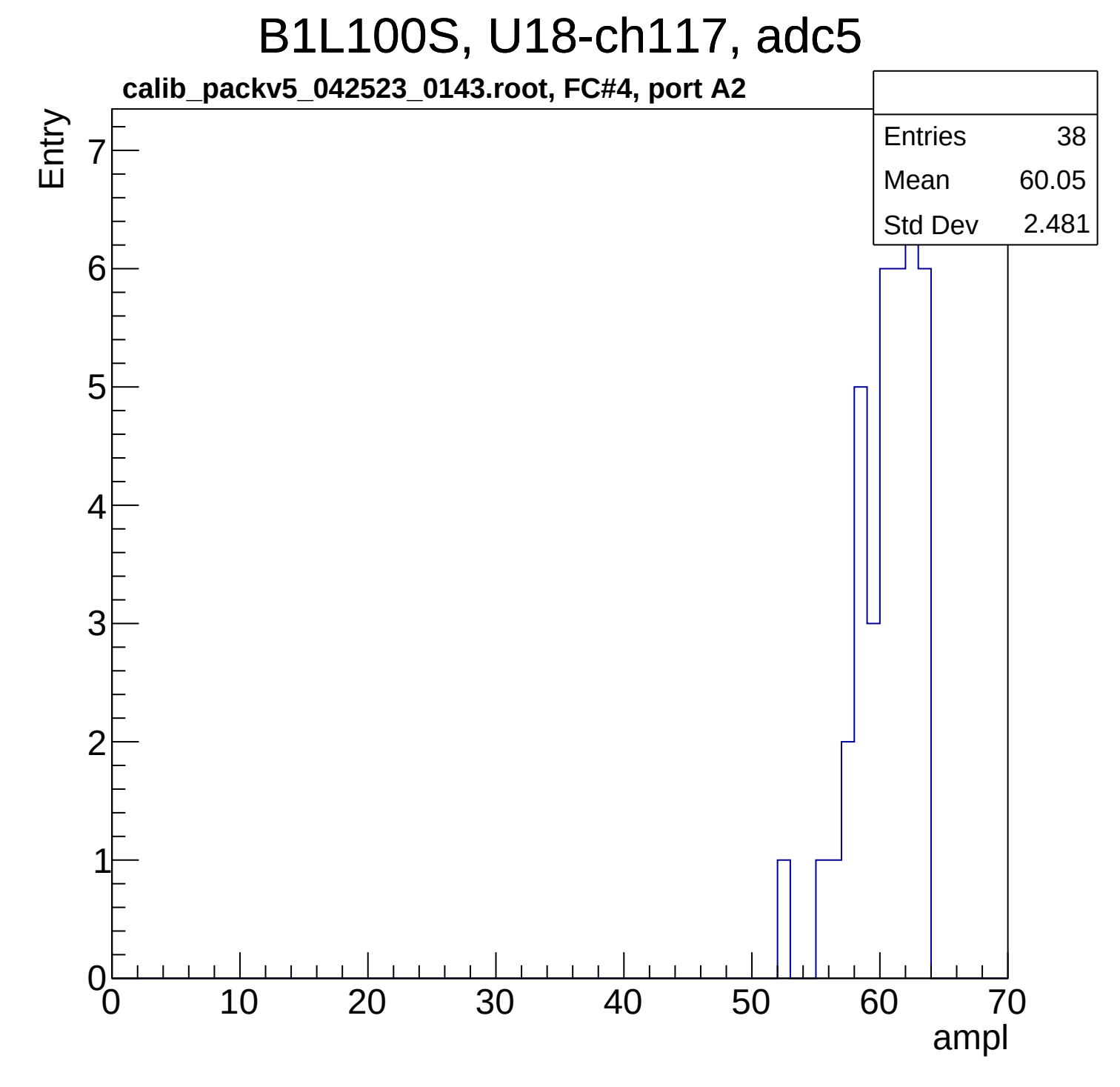

B1L100S, U18-ch117, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 29.76
Std Dev 4.965
Gaus mean : 30.8161
Gaus Width: 3.3693
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

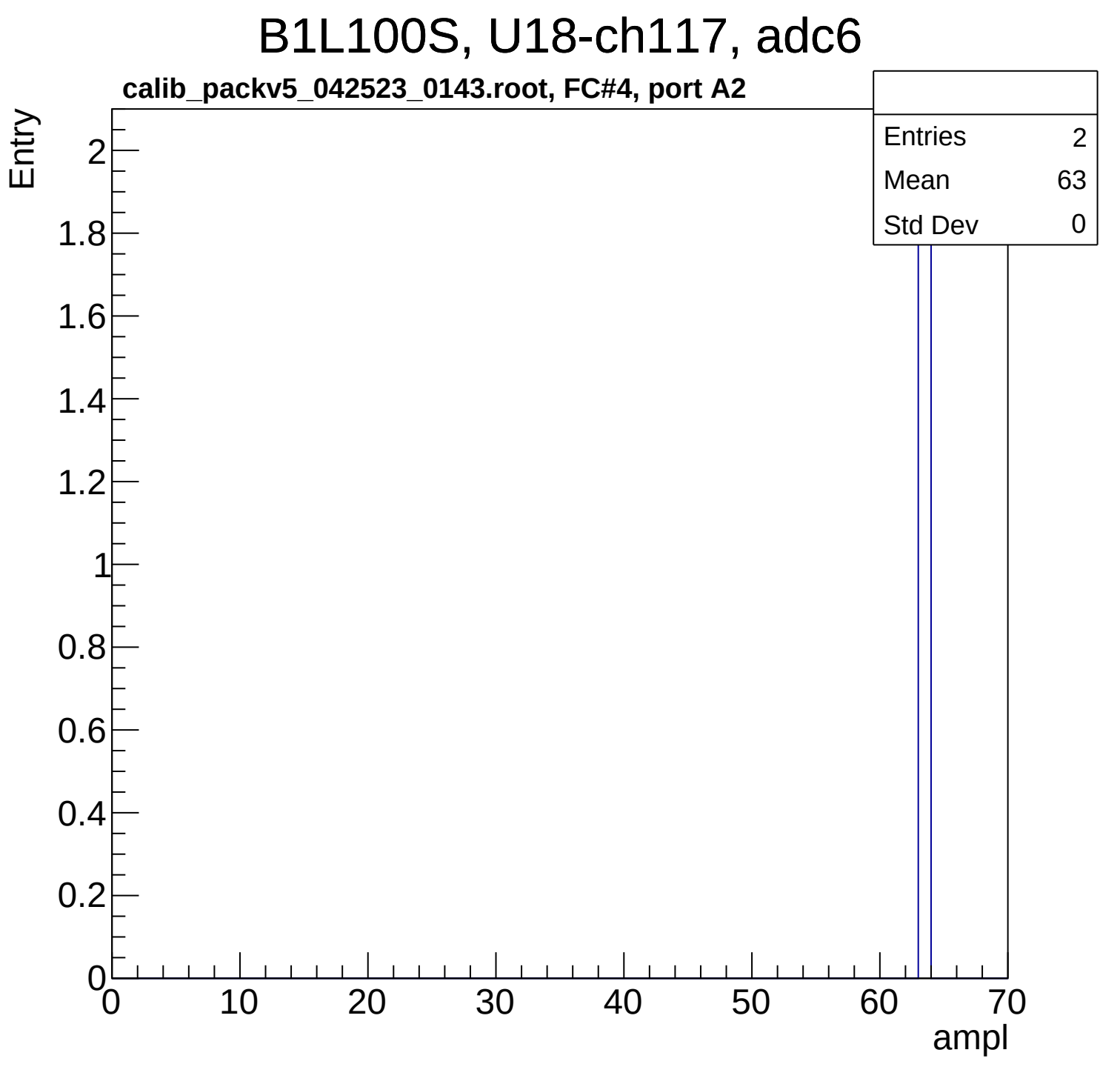

B1L100S, U18-ch117, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 37.04
Std Dev 3.861
Gaus mean : 37.8847
Gaus Width: 4.0458
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

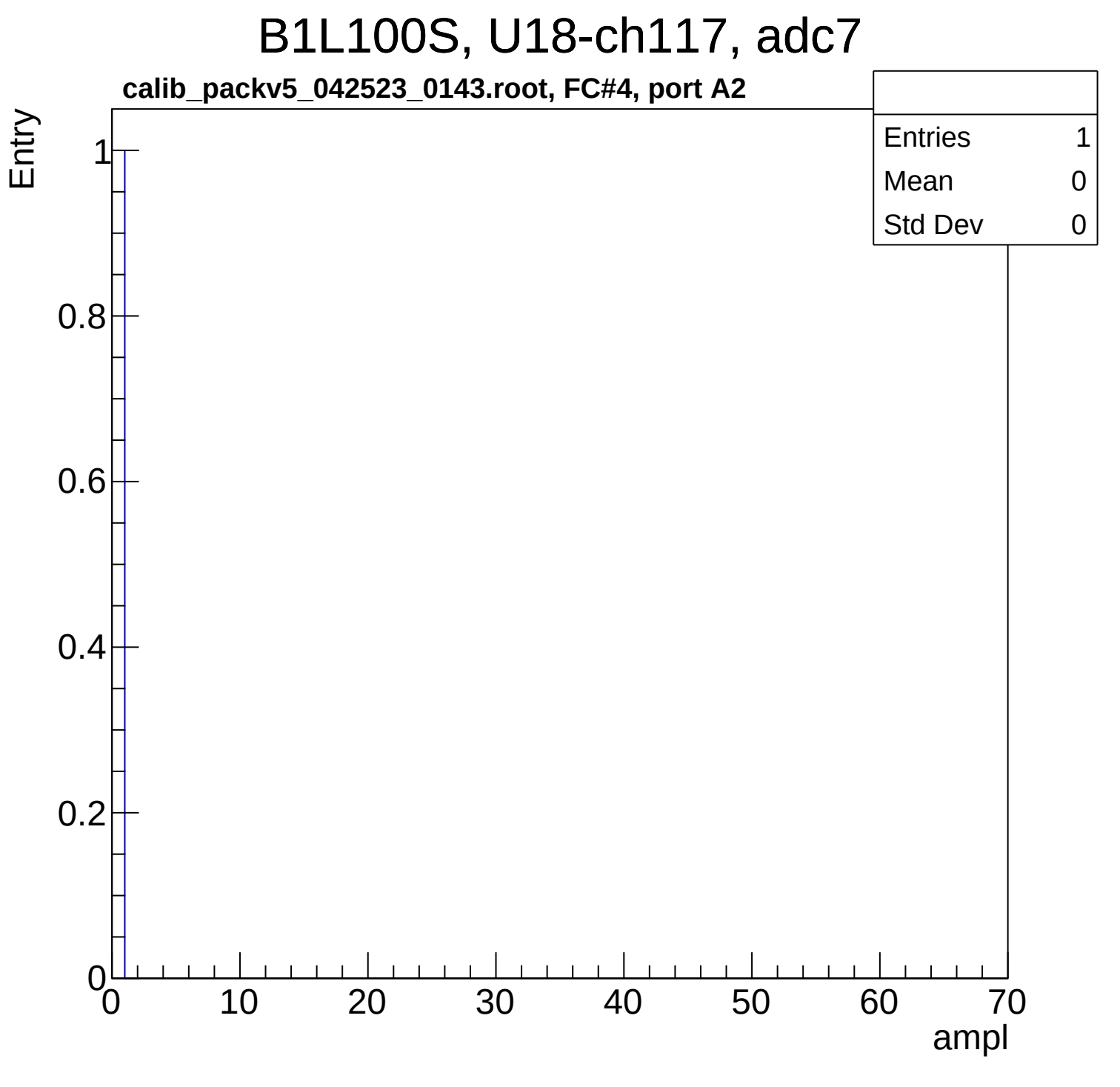

B1L100S, U18-ch117, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 71
Mean 44.14
Std Dev 3.565
Gaus mean : 44.5592
Gaus Width: 4.0737
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

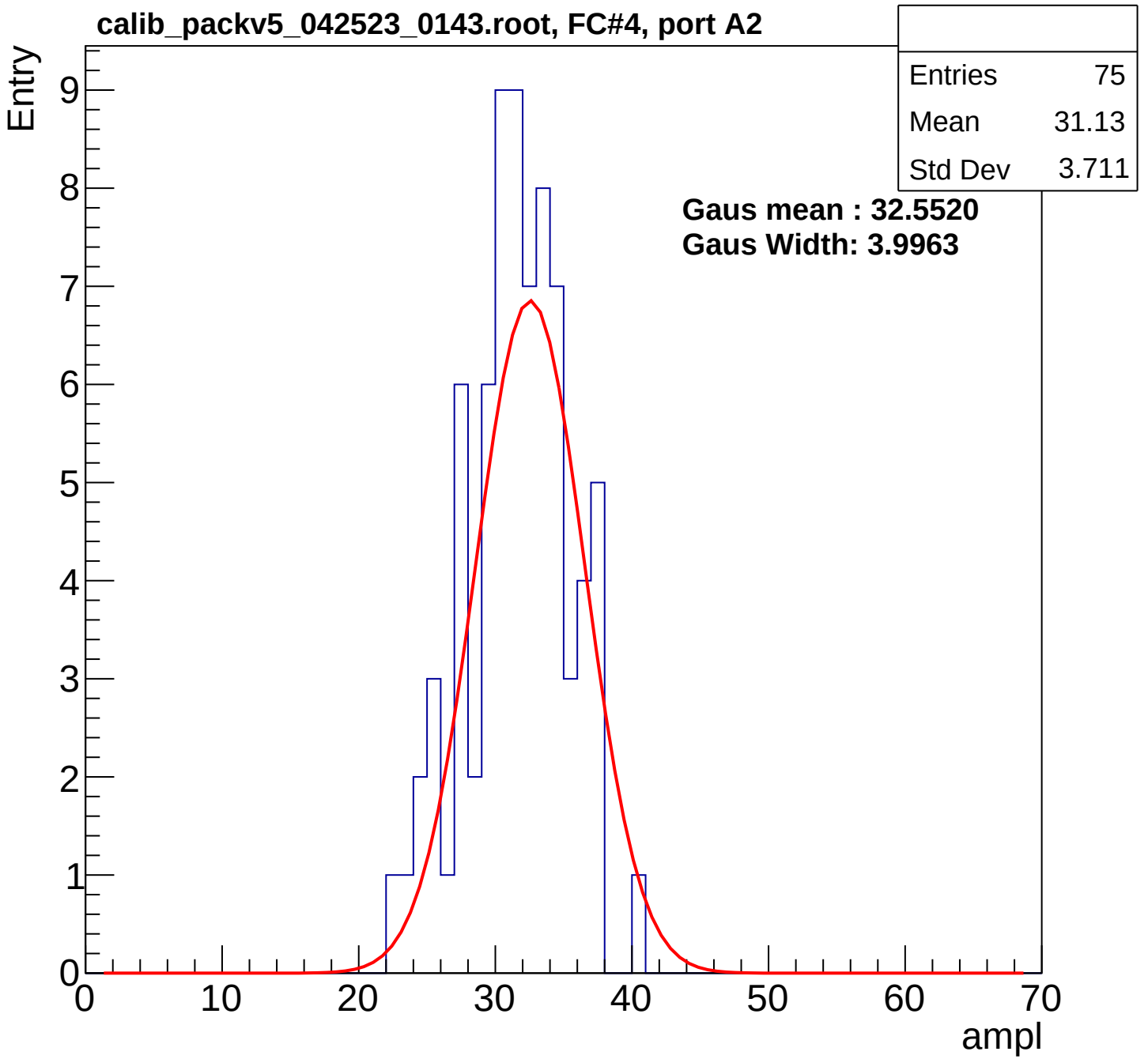

B1L100S, U18-ch117, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 51.24
Std Dev 3.235
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

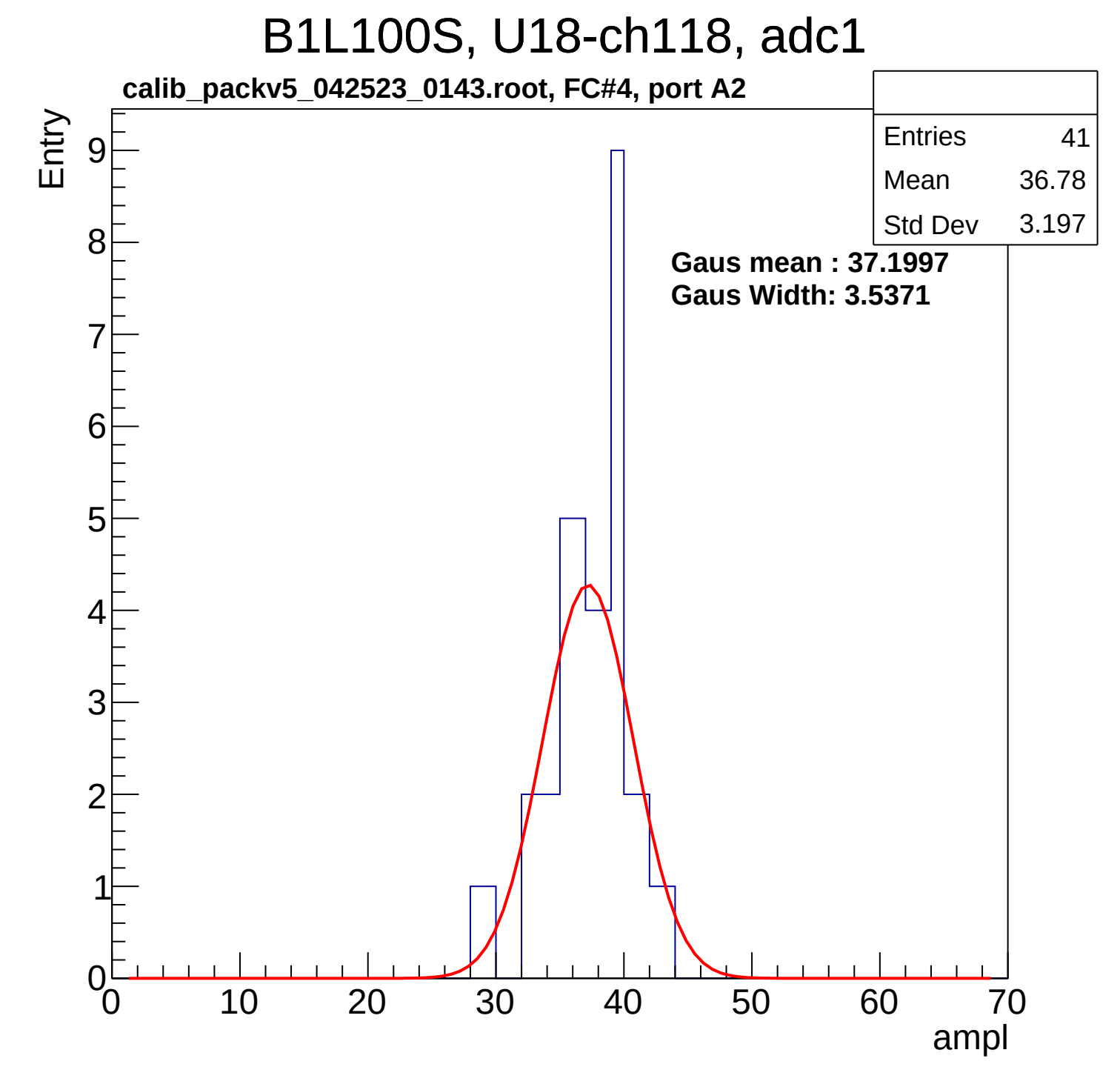

B1L100S, U18-ch117, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 55
Mean 55.65
Std Dev 8.499
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

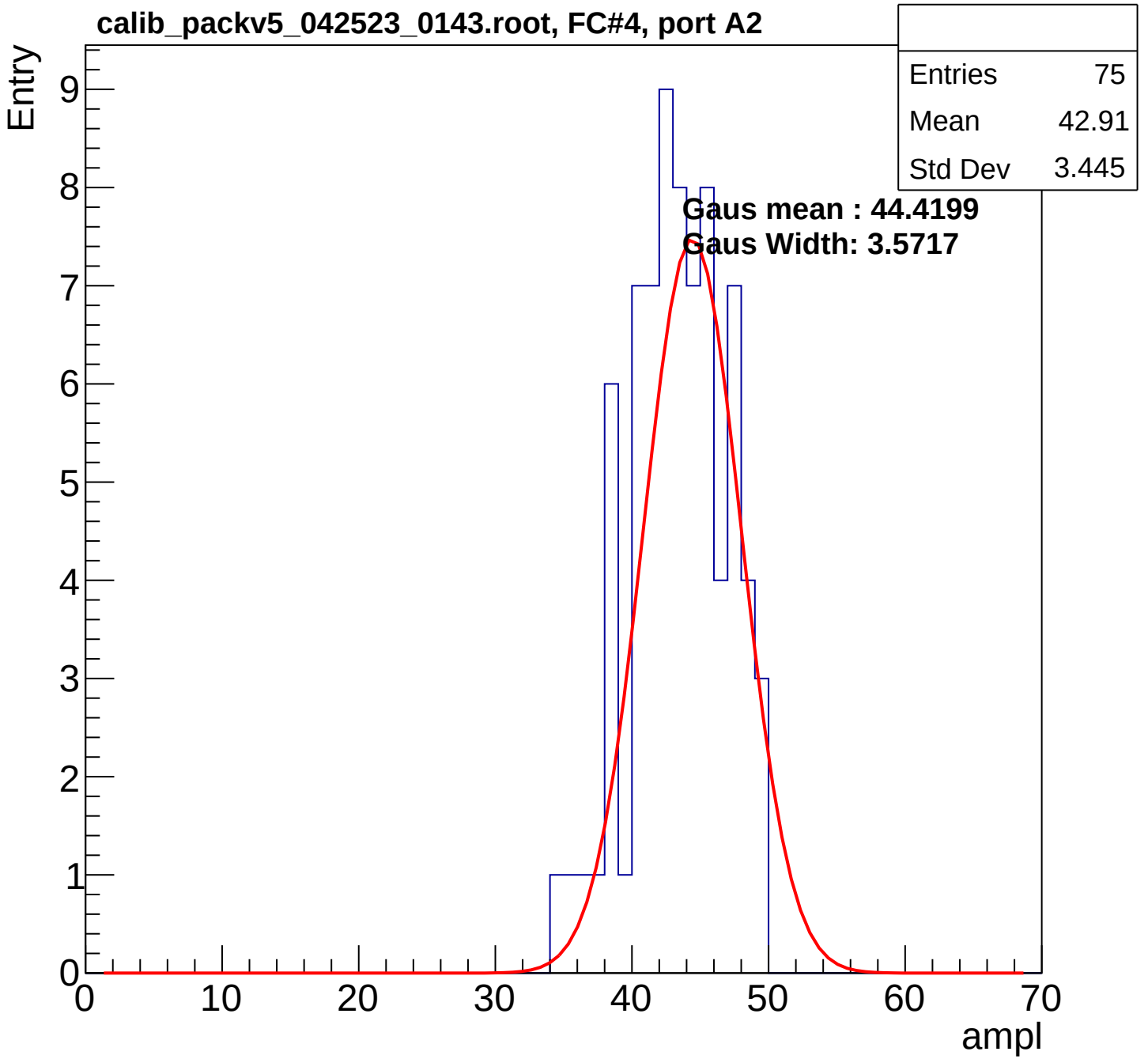

B1L100S, U18-ch117, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 38
Mean 60.05
Std Dev 2.481
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

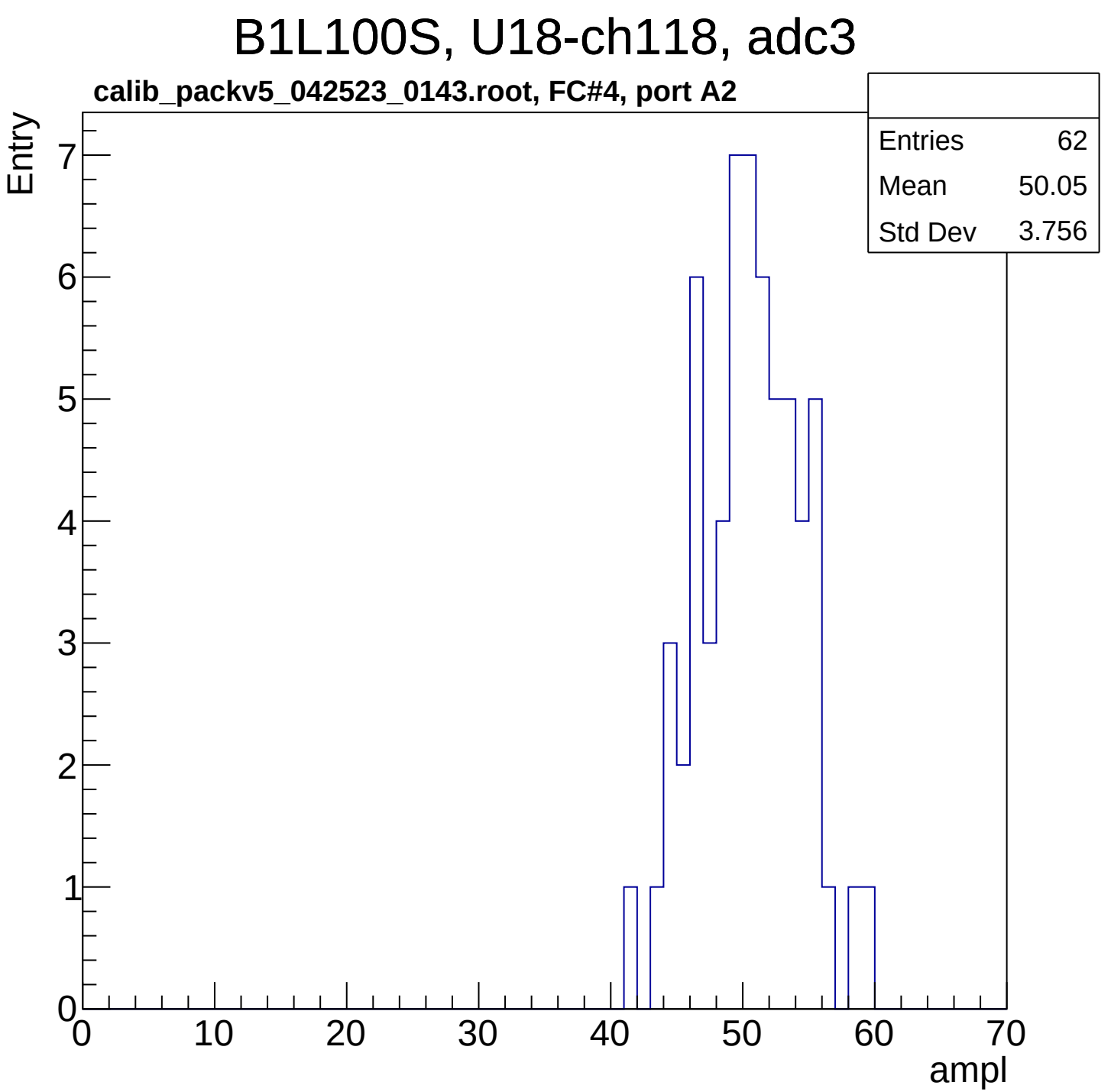

B1L100S, U18-ch117, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 63
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

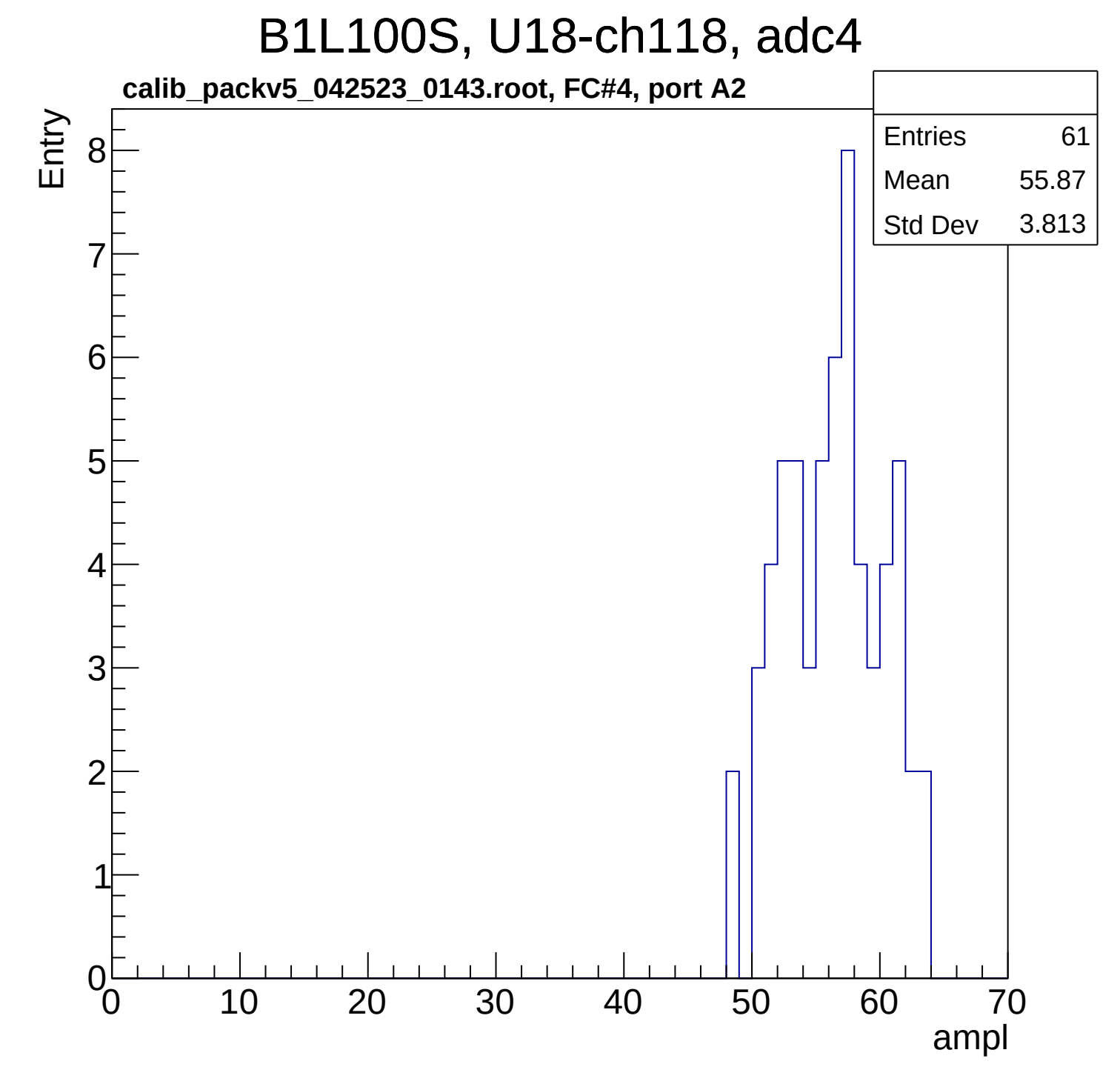

B1L100S, U18-ch117, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

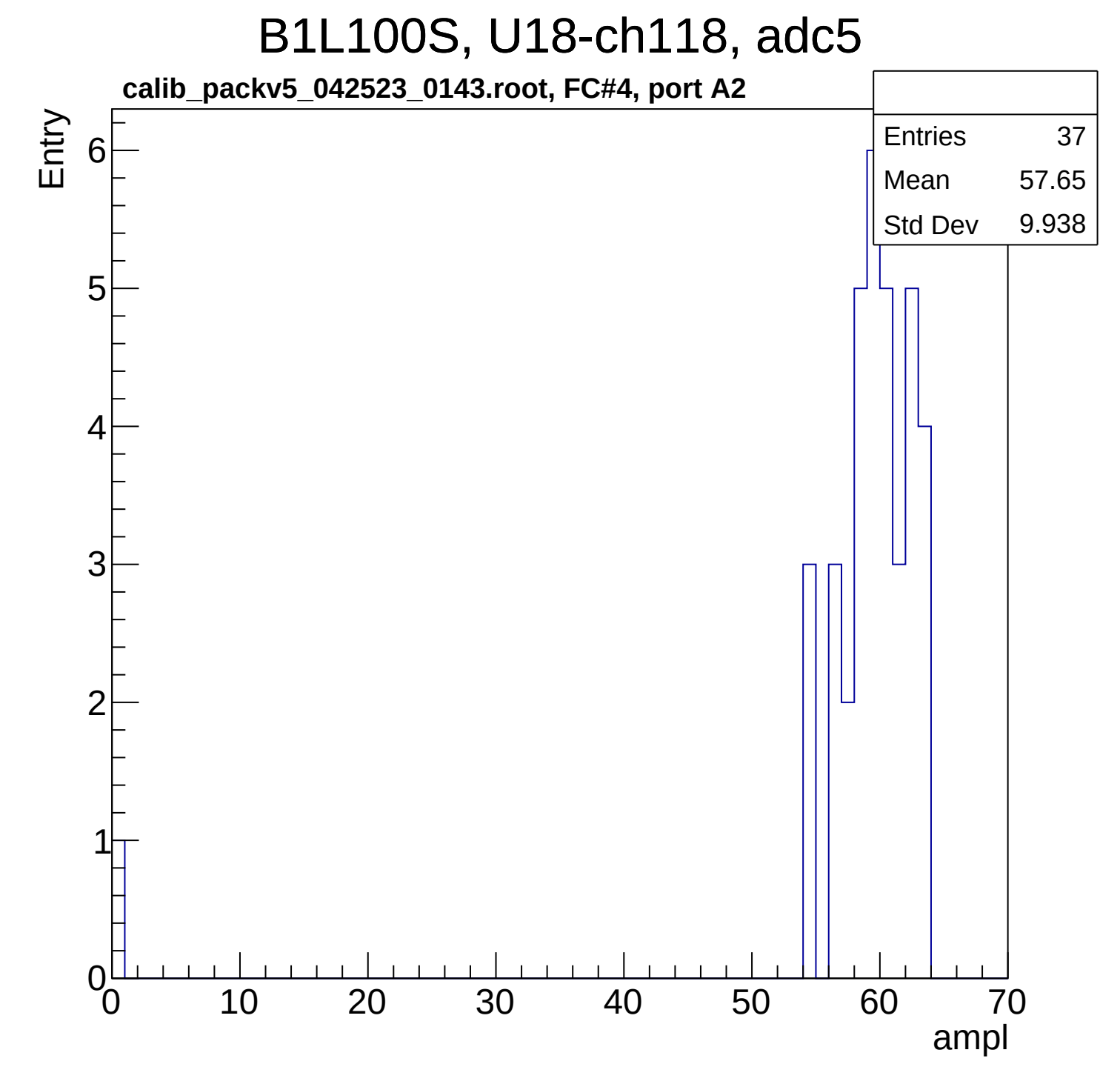

B1L100S, U18-ch118, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 31.13
Std Dev 3.711
Gaus mean : 32.5520
Gaus Width: 3.9963
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

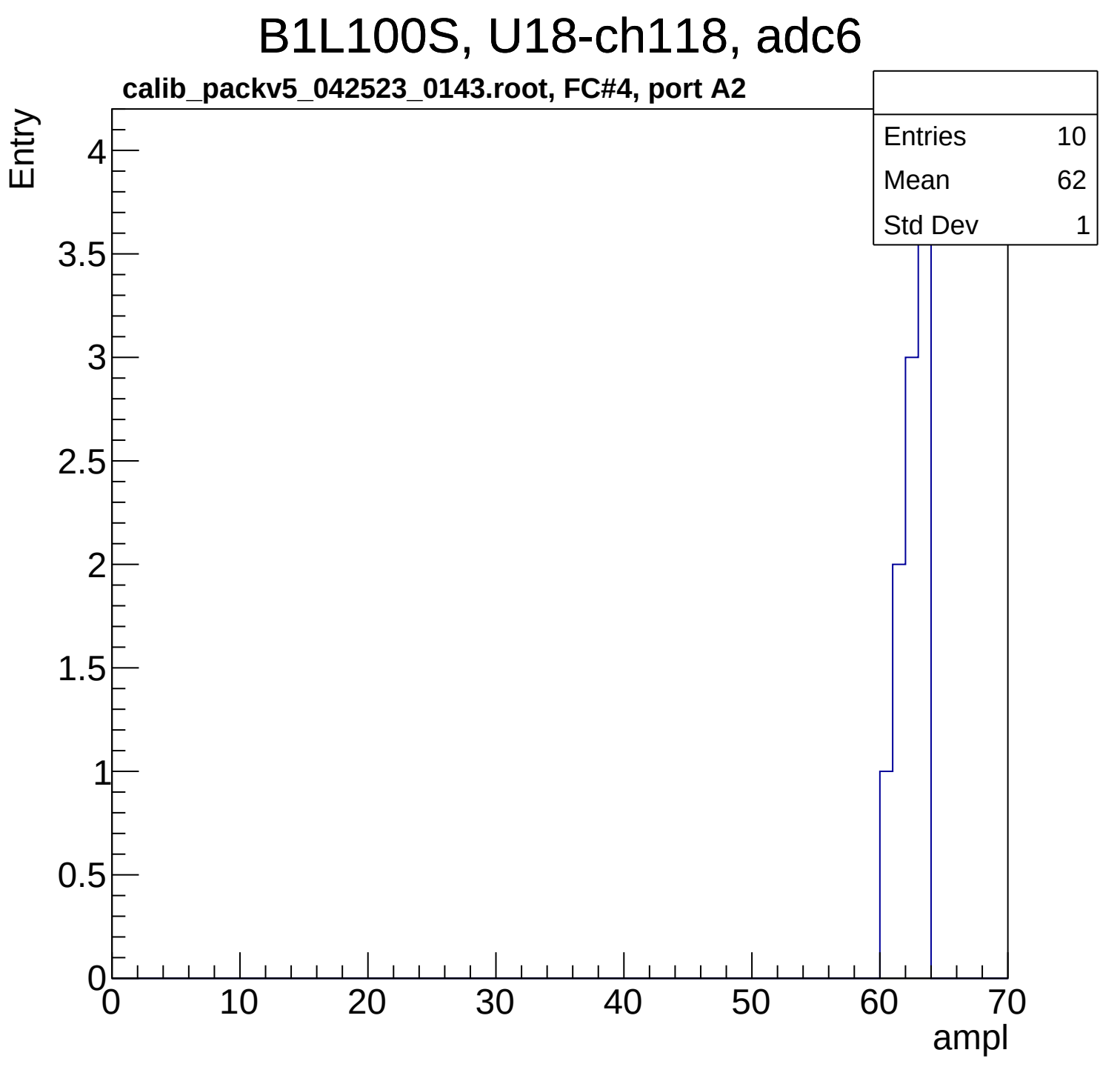

B1L100S, U18-ch118, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 41
Mean 36.78
Std Dev 3.197
Gaus mean : 37.1997
Gaus Width: 3.5371
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

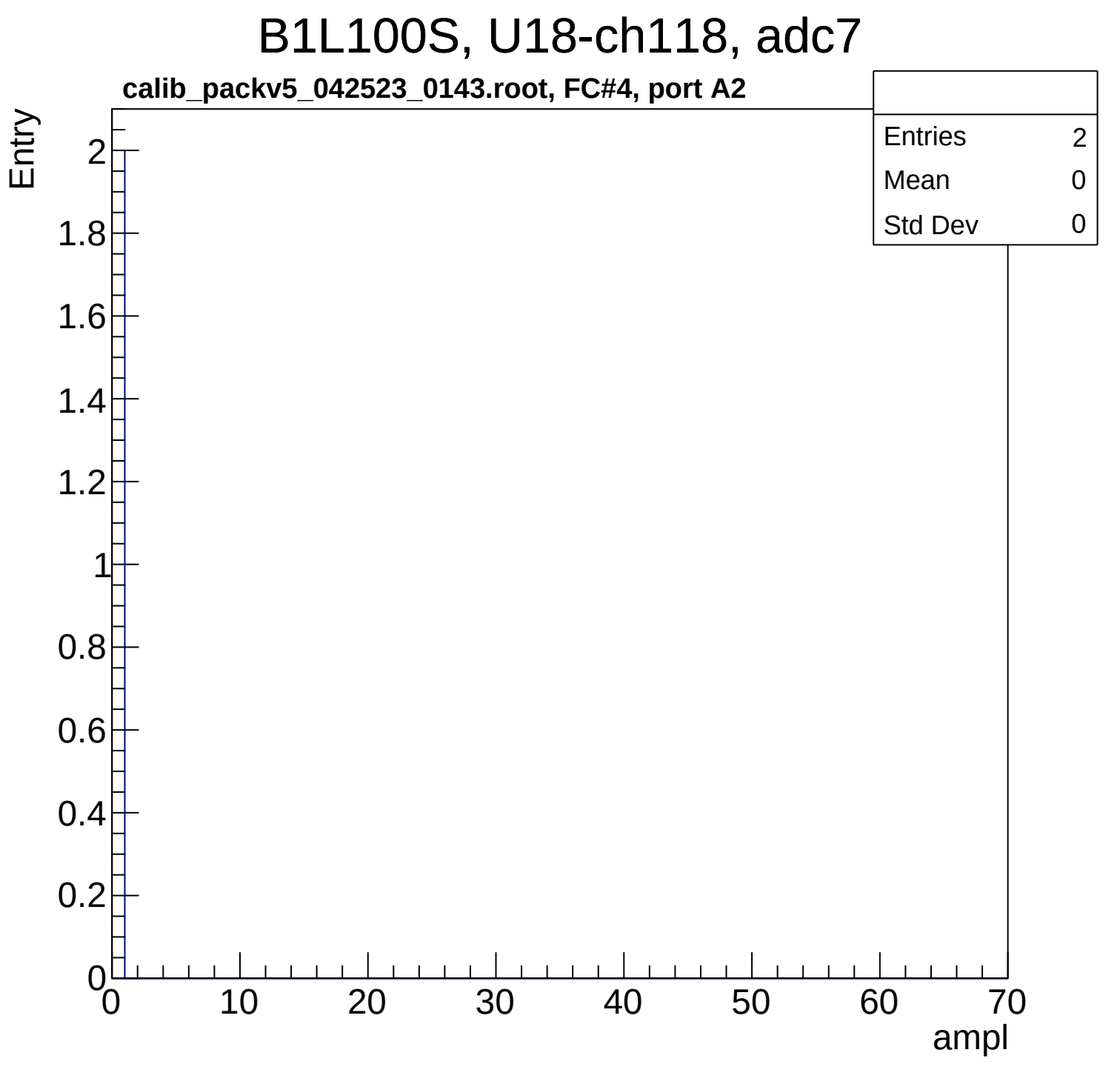

B1L100S, U18-ch118, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 42.91
Std Dev 3.445
Gaus mean : 44.4199
Gaus Width: 3.5717
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

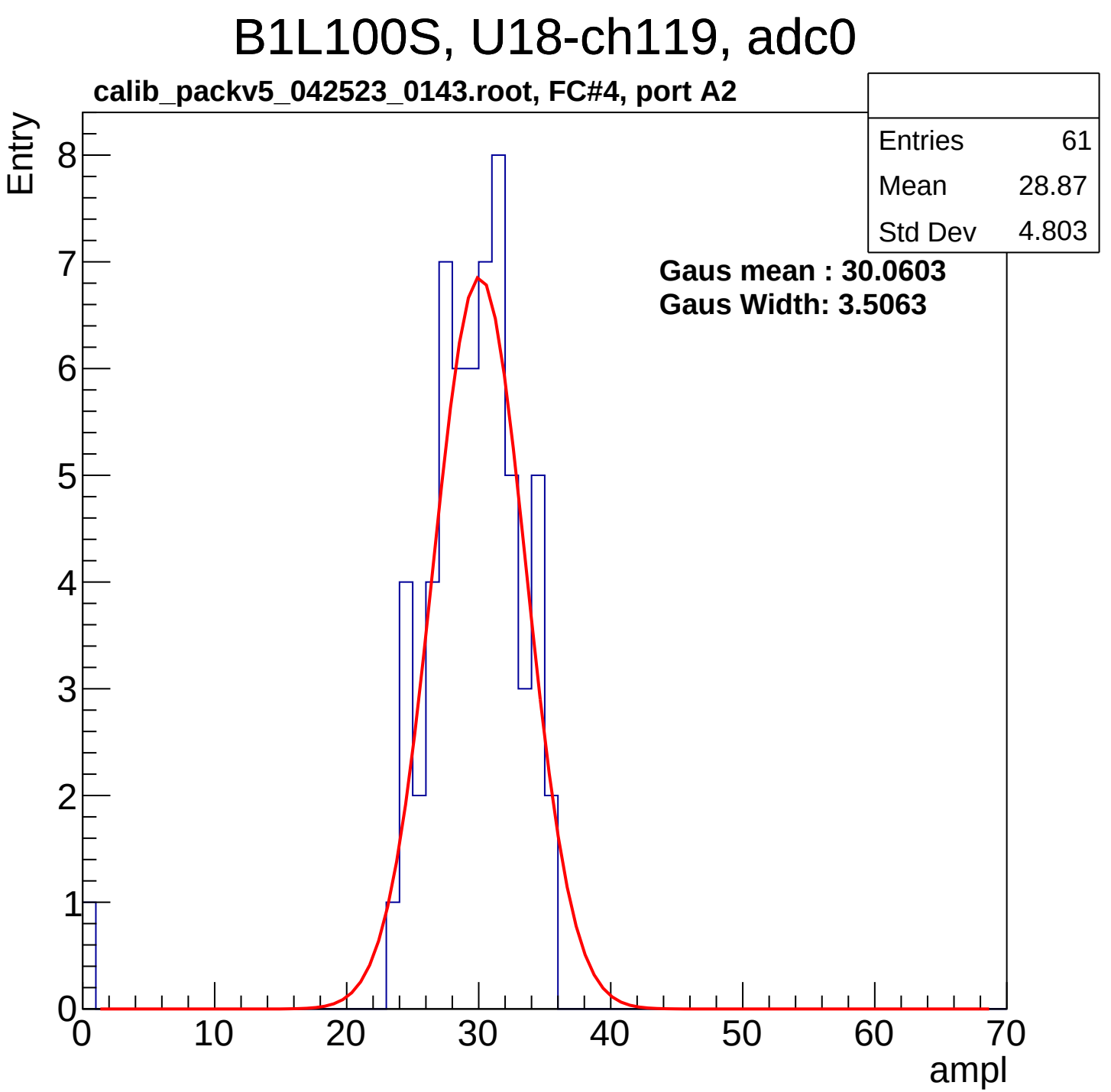

B1L100S, U18-ch118, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 50.05
Std Dev 3.756
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

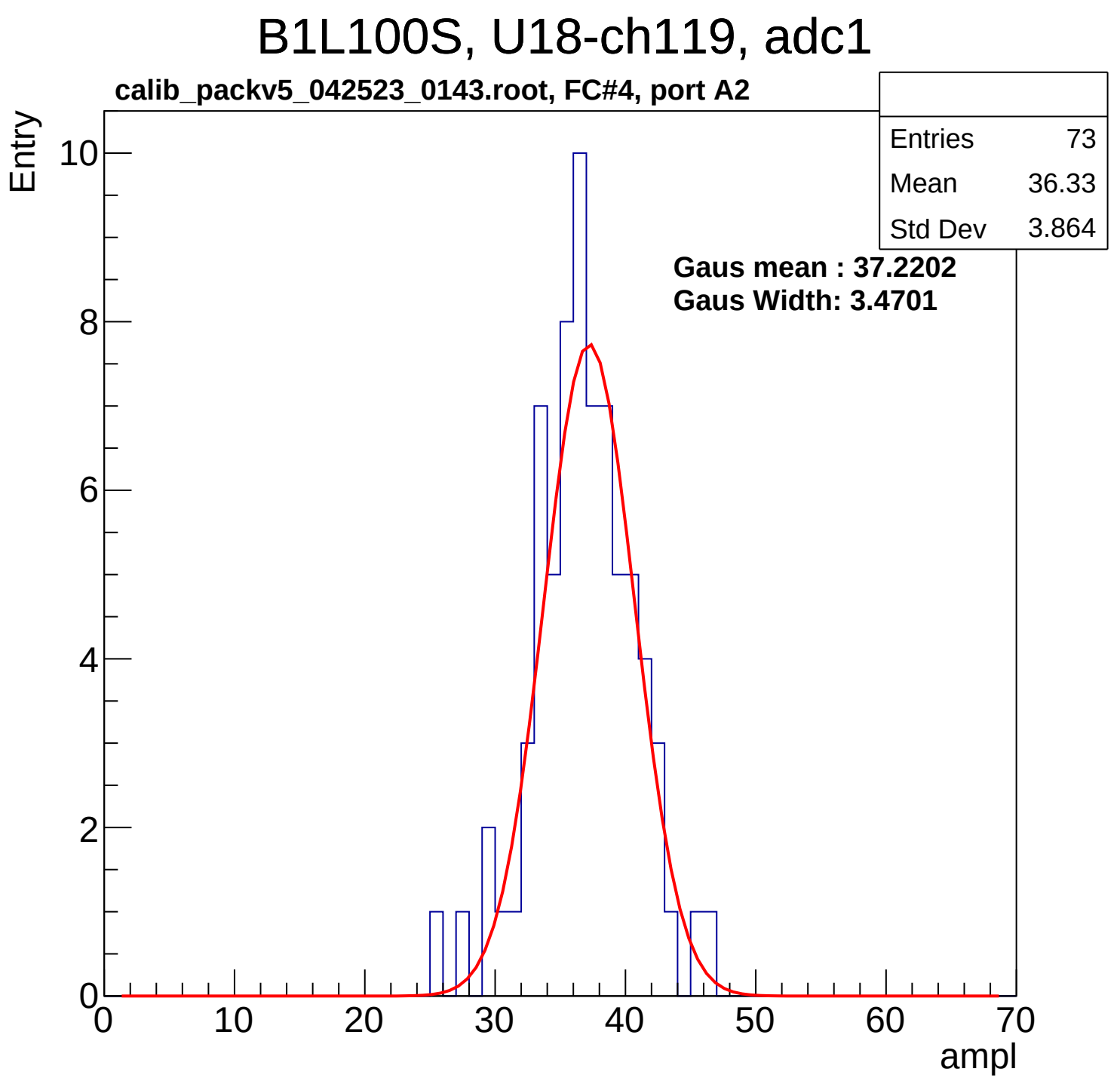

B1L100S, U18-ch118, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 55.87
Std Dev 3.813
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

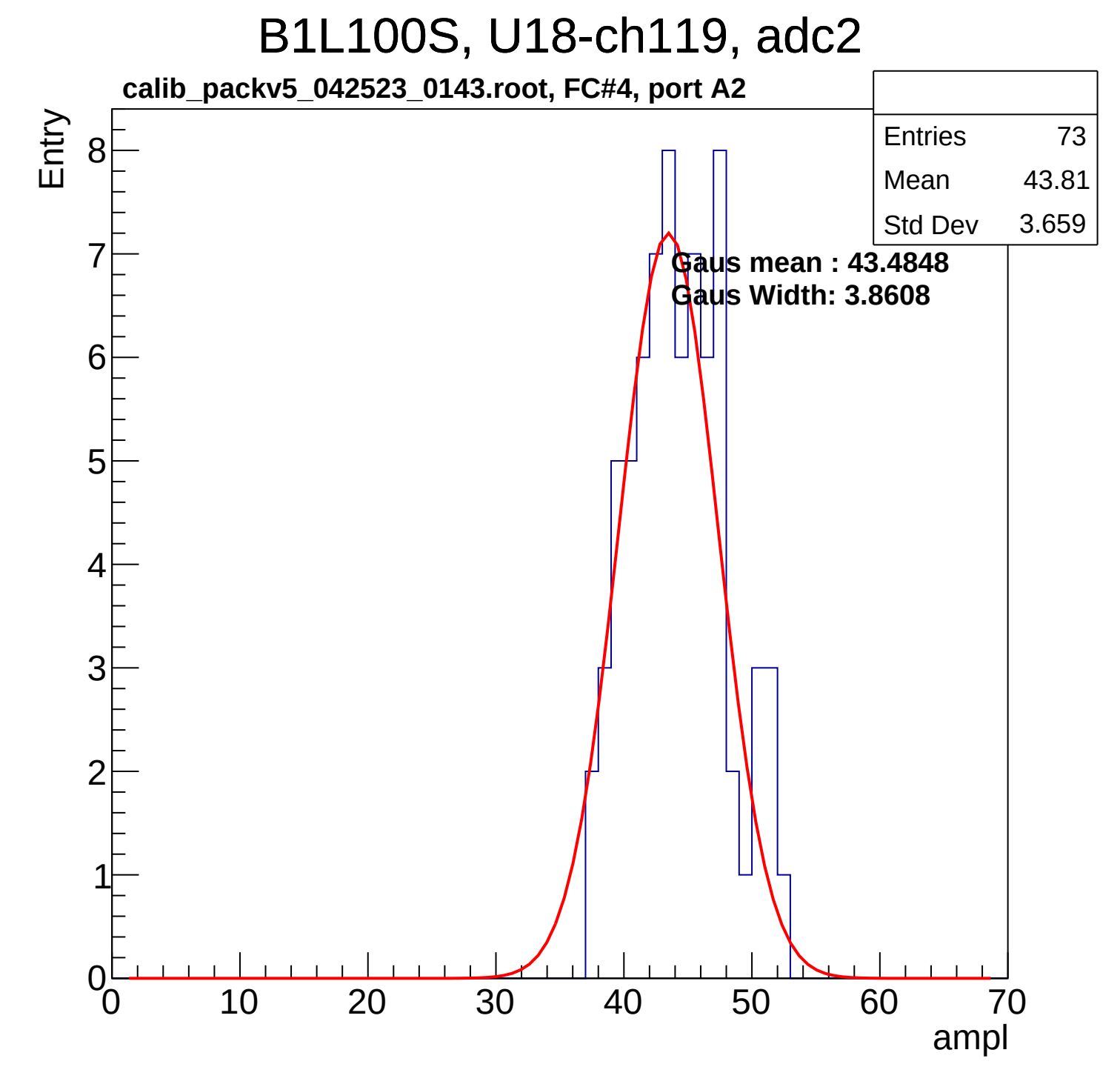

B1L100S, U18-ch118, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 37
Mean 57.65
Std Dev 9.938
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

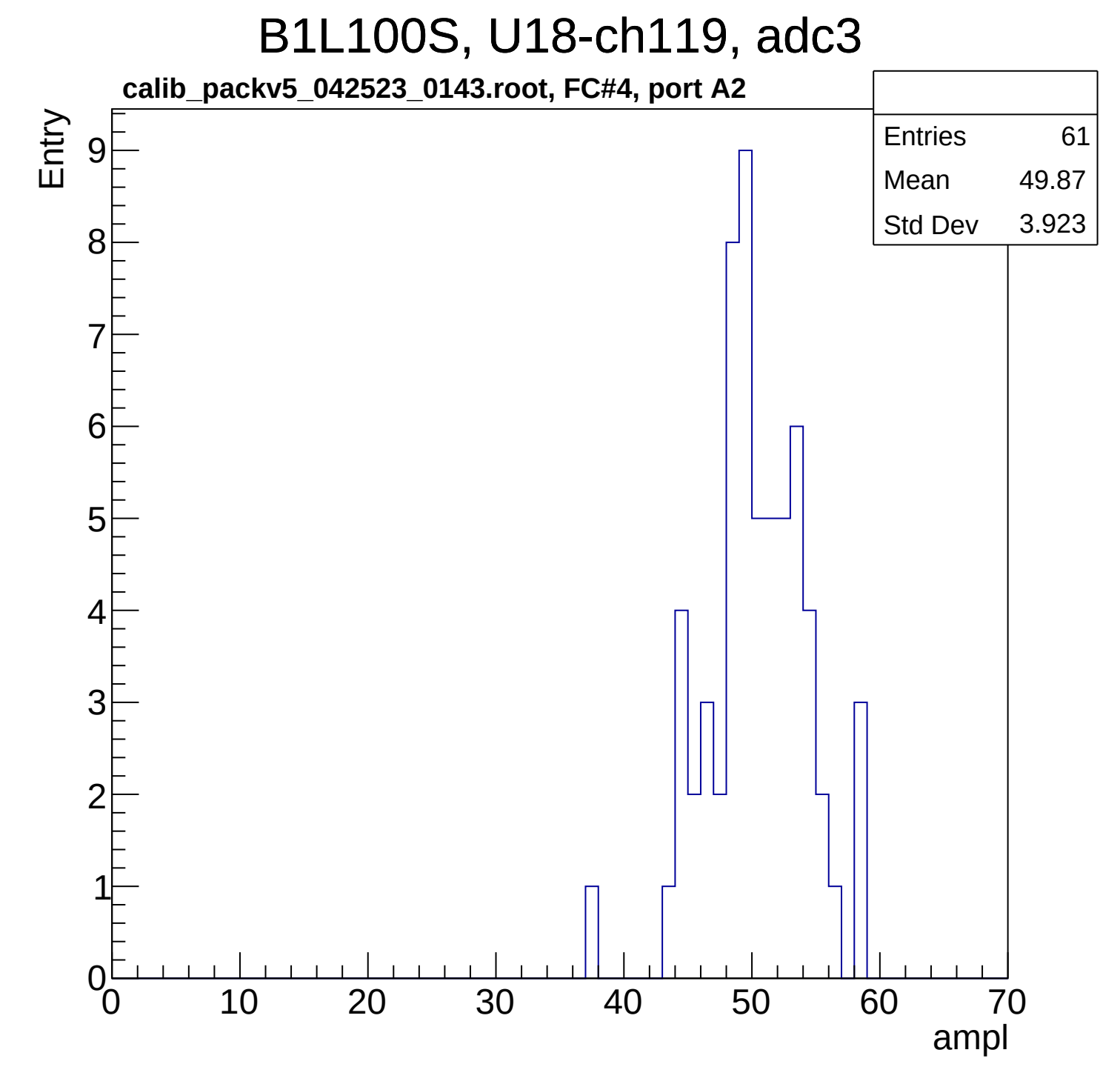

B1L100S, U18-ch118, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 62
Std Dev 1
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

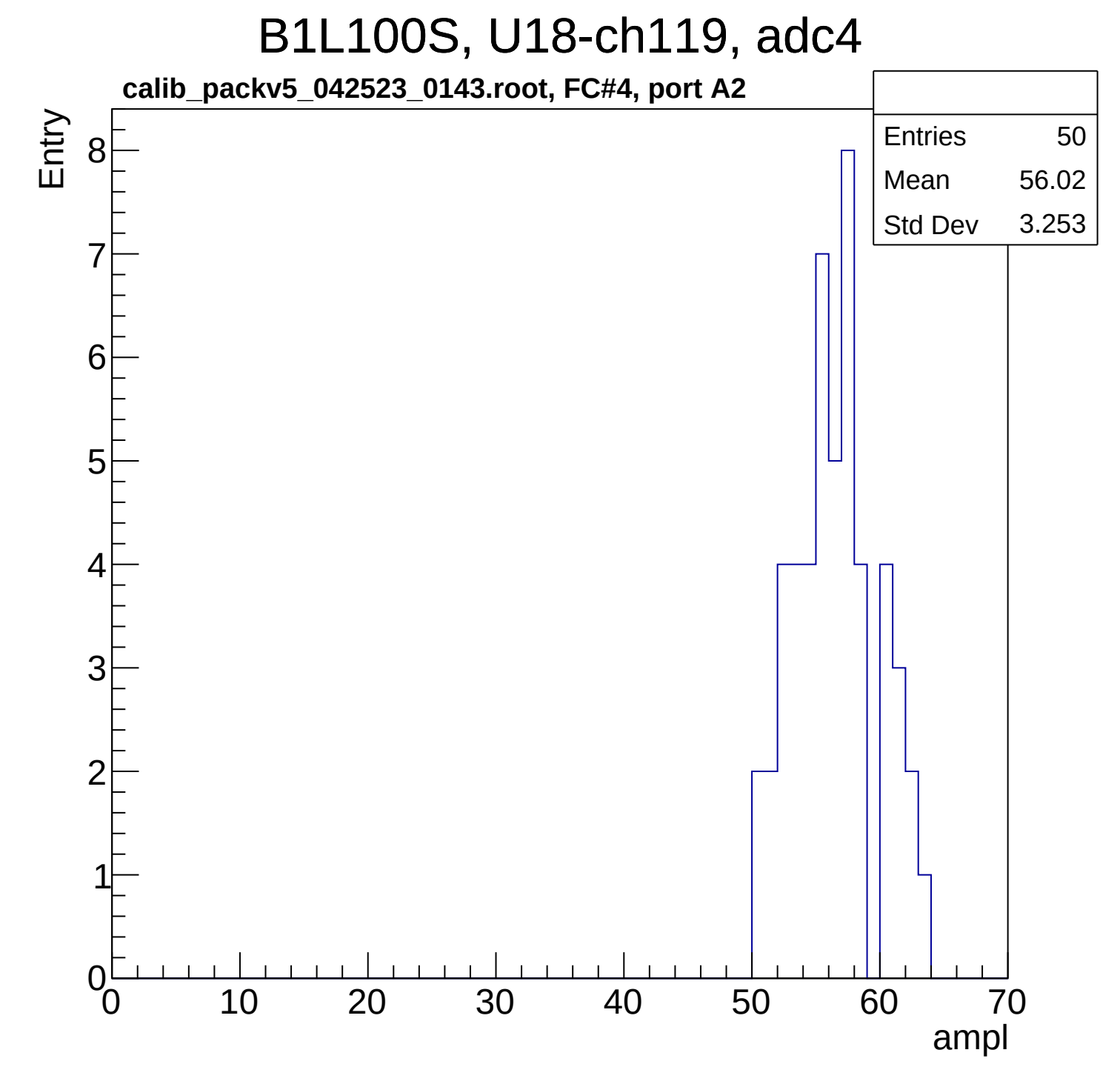

B1L100S, U18-ch118, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 2
Mean 0
Std Dev 0
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

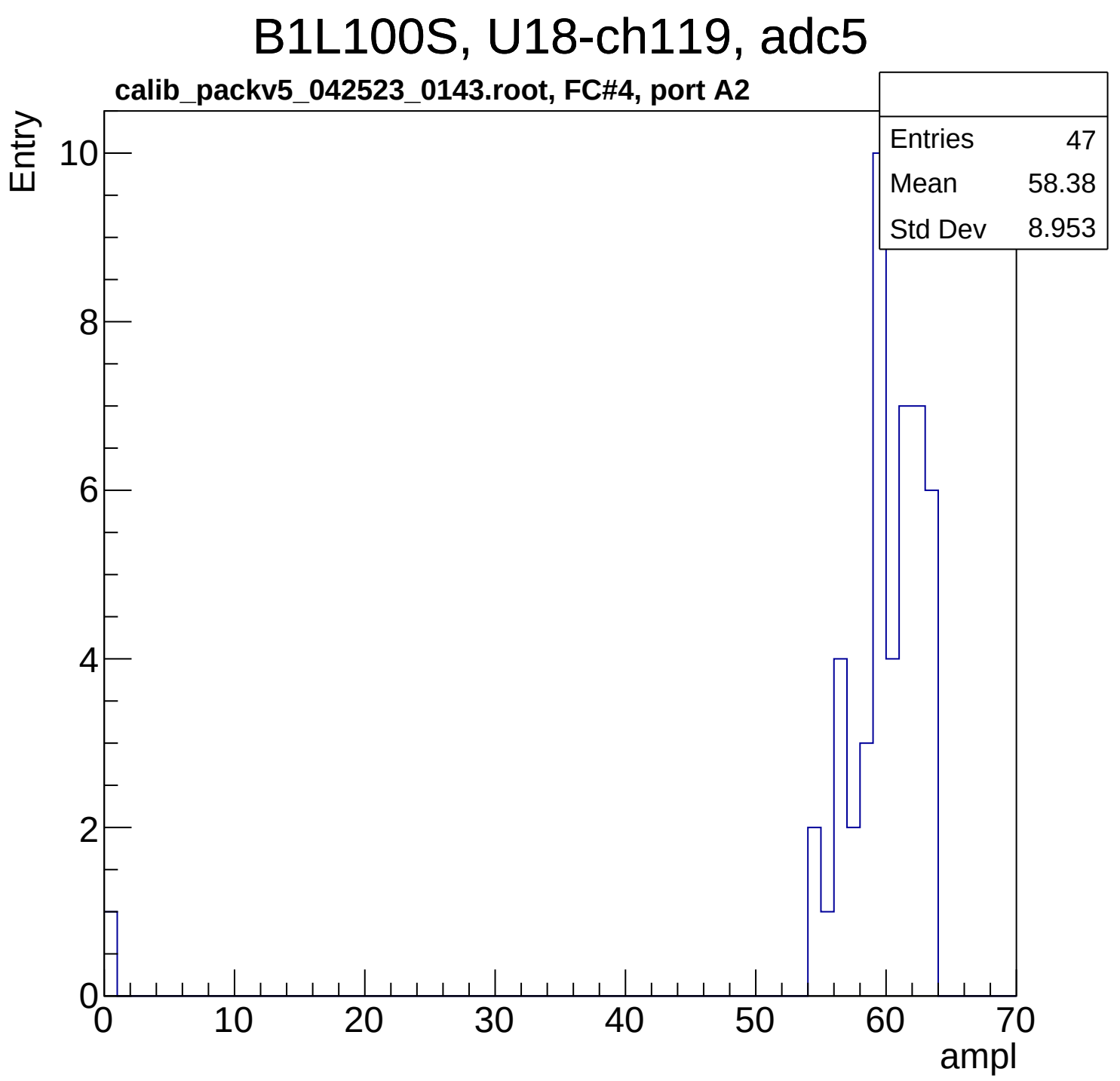

B1L100S, U18-ch119, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 28.87
Std Dev 4.803
Gaus mean : 30.0603
Gaus Width: 3.5063
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

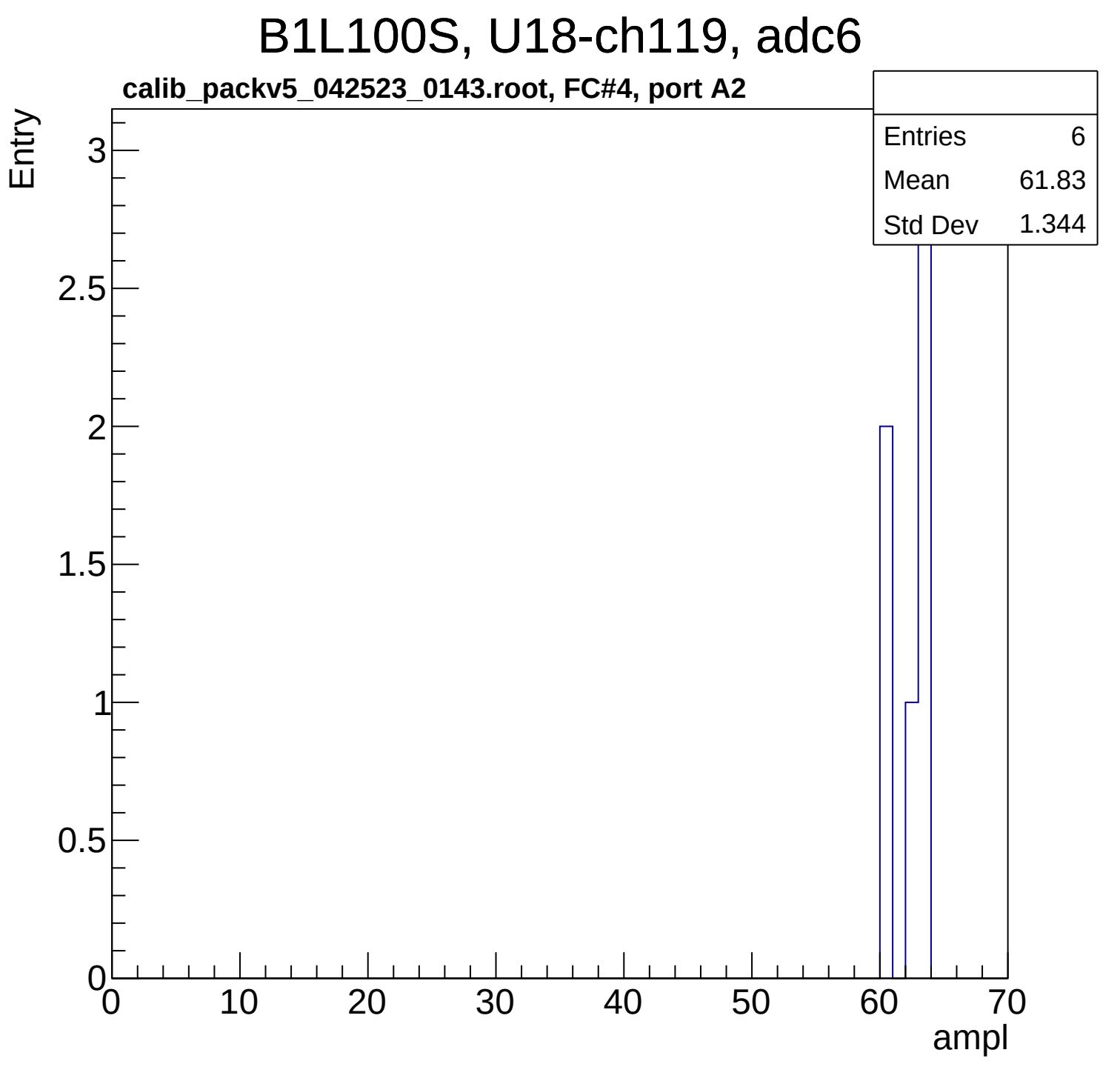

B1L100S, U18-ch119, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 36.33
Std Dev 3.864
Gaus mean : 37.2202
Gaus Width: 3.4701
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

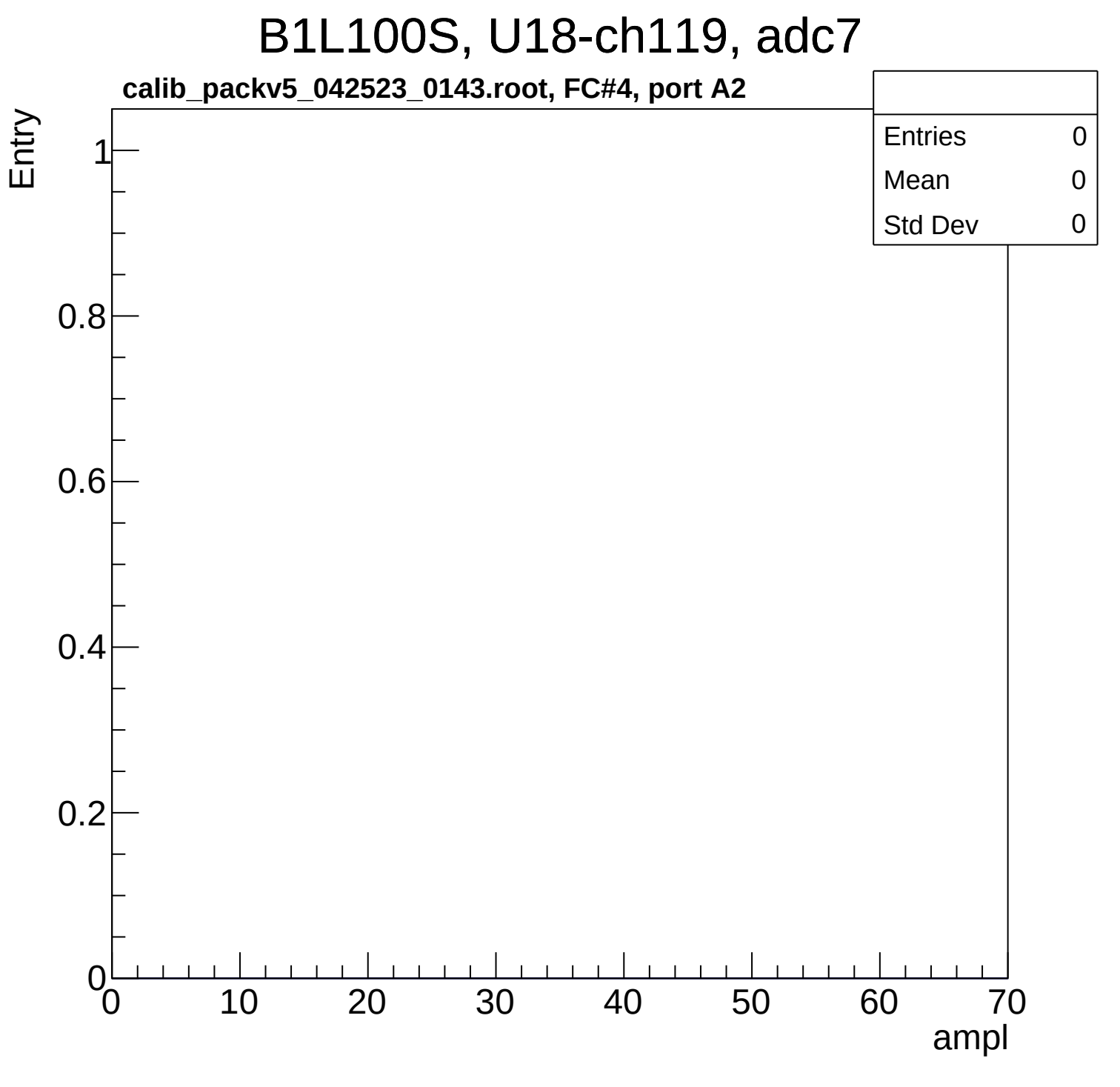

B1L100S, U18-ch119, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 43.81
Std Dev 3.659
Gaus mean : 43.4848
Gaus Width: 3.8608
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

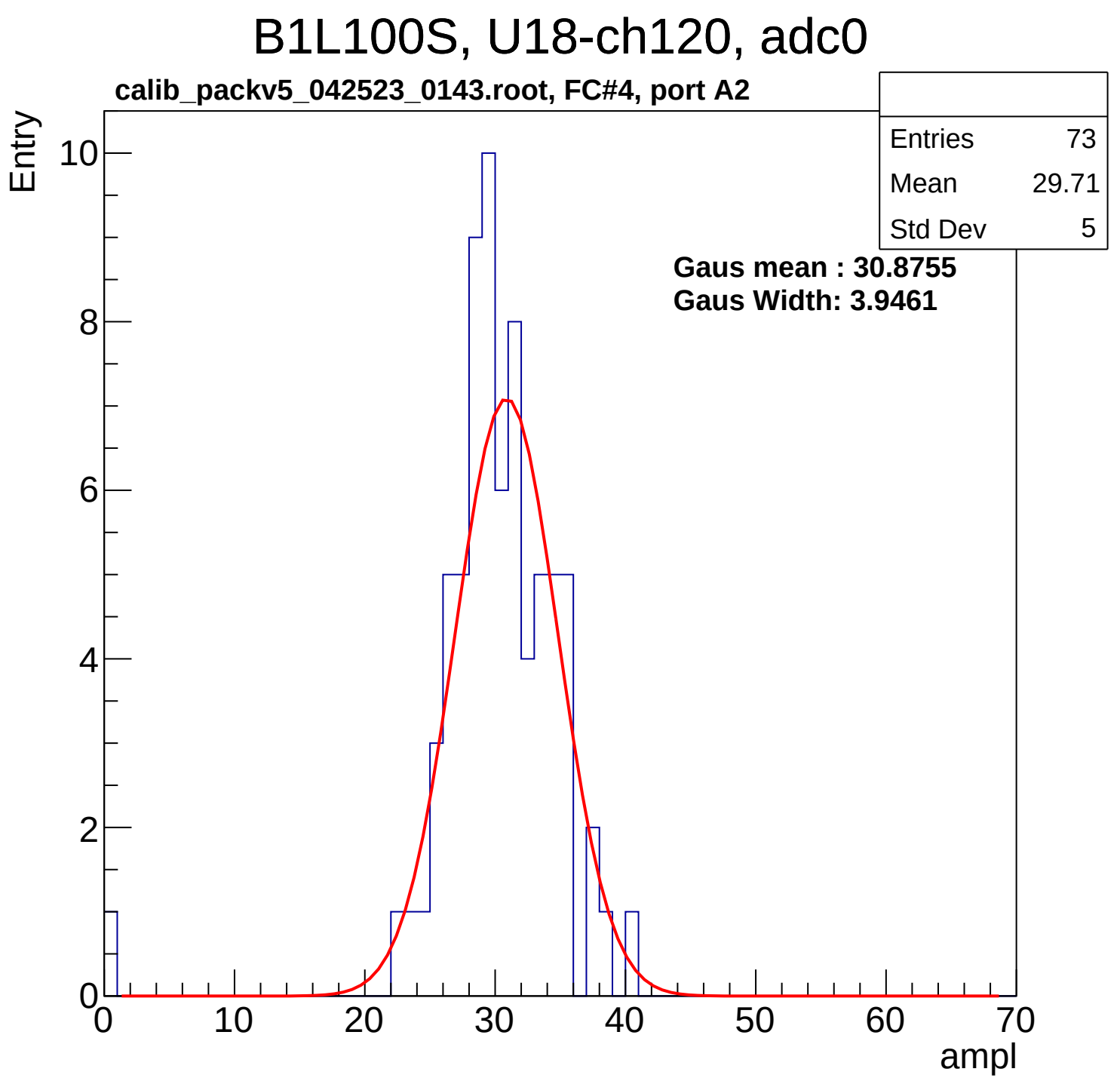

B1L100S, U18-ch119, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 49.87
Std Dev 3.923
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

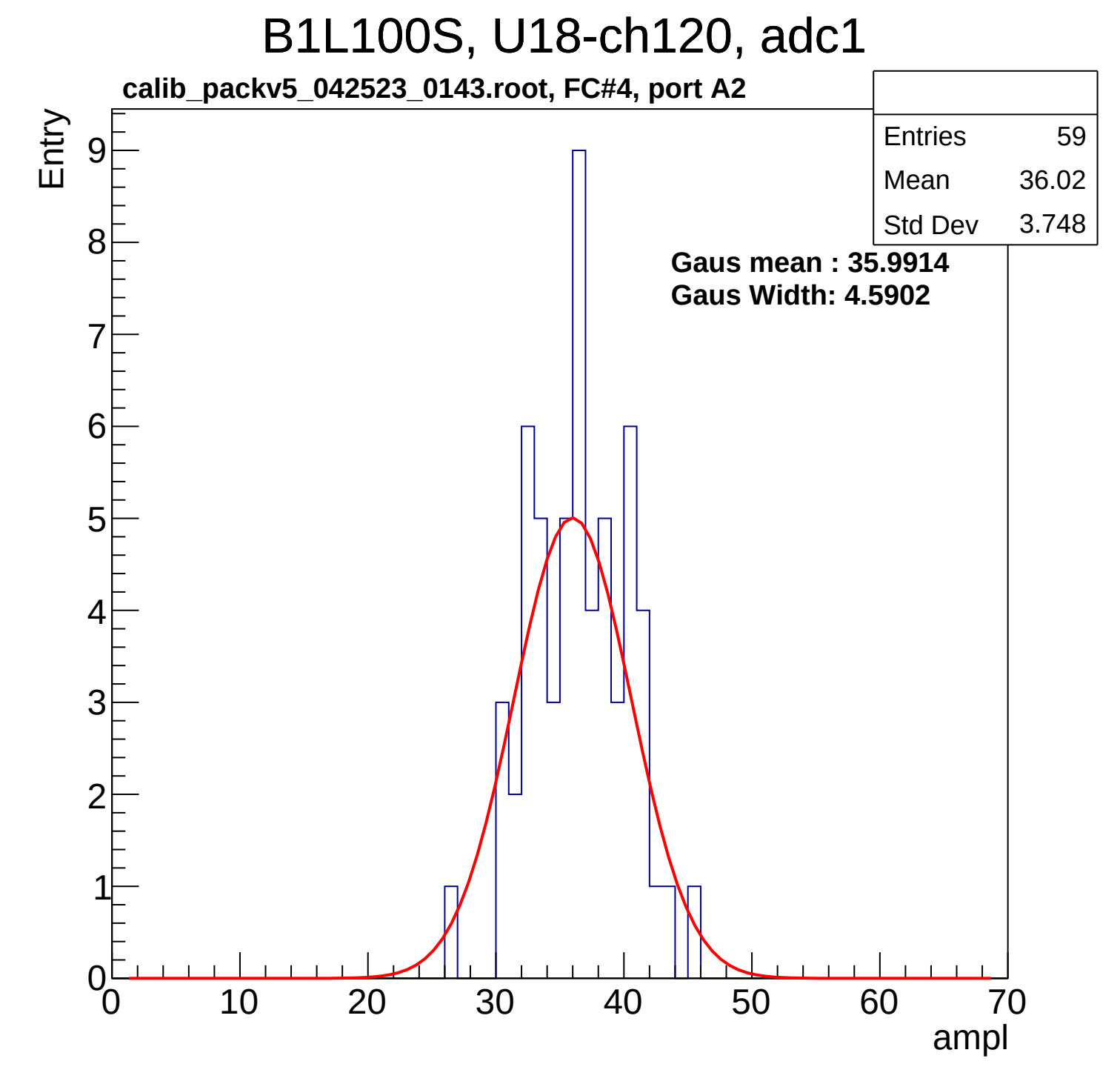

B1L100S, U18-ch119, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 56.02
Std Dev 3.253
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

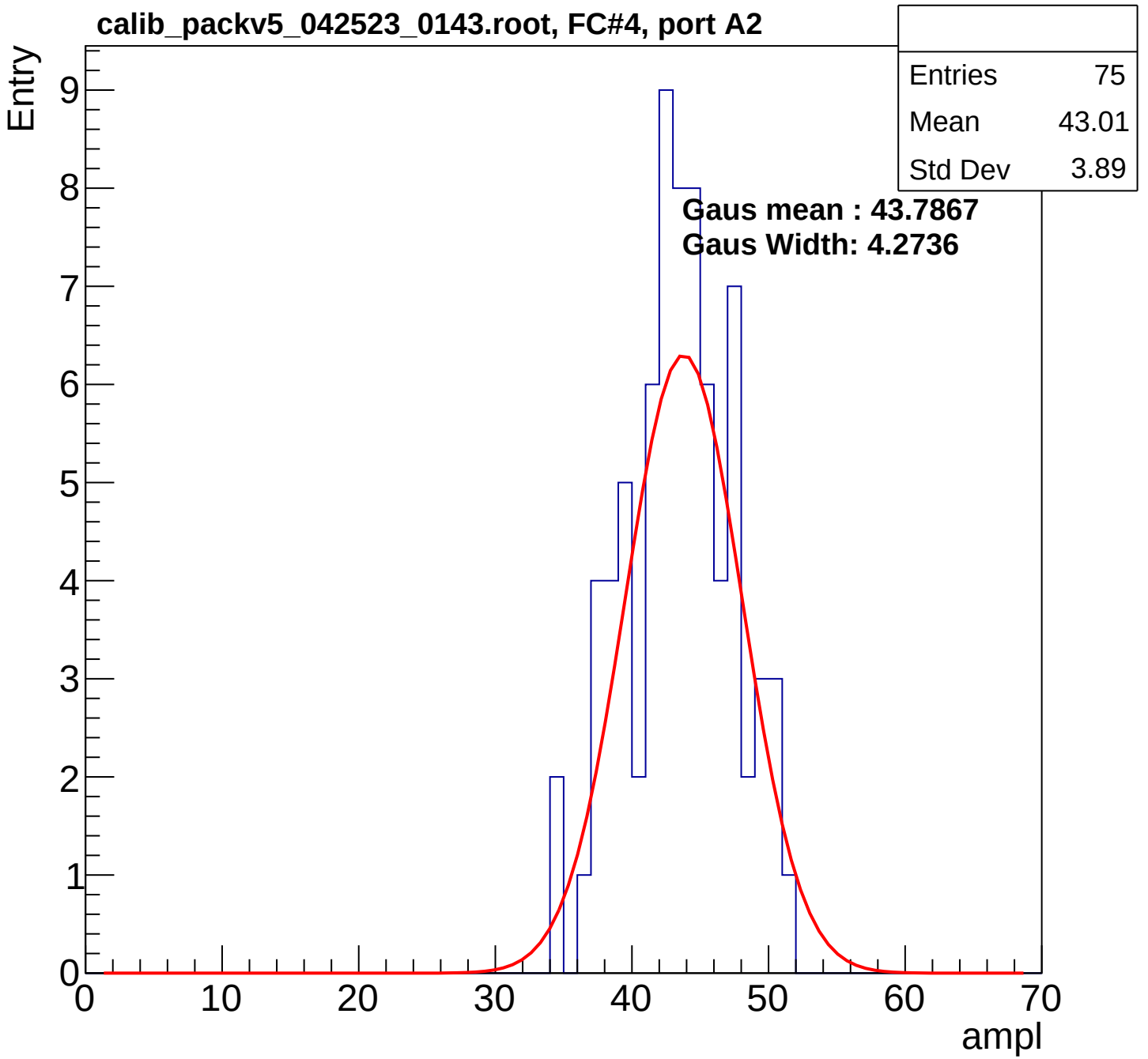

B1L100S, U18-ch119, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 58.38
Std Dev 8.953
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

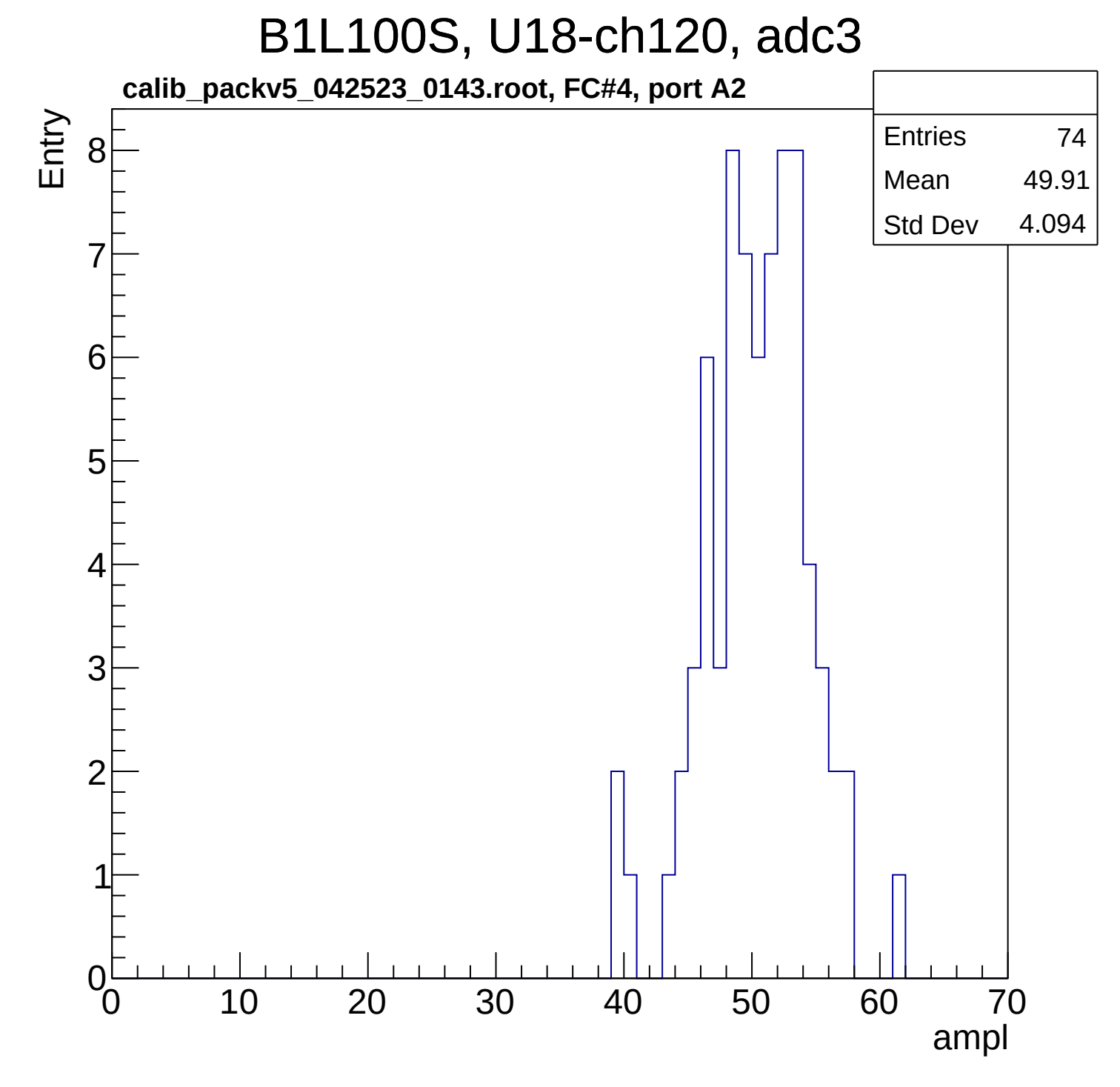

B1L100S, U18-ch119, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 61.83
Std Dev 1.344
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

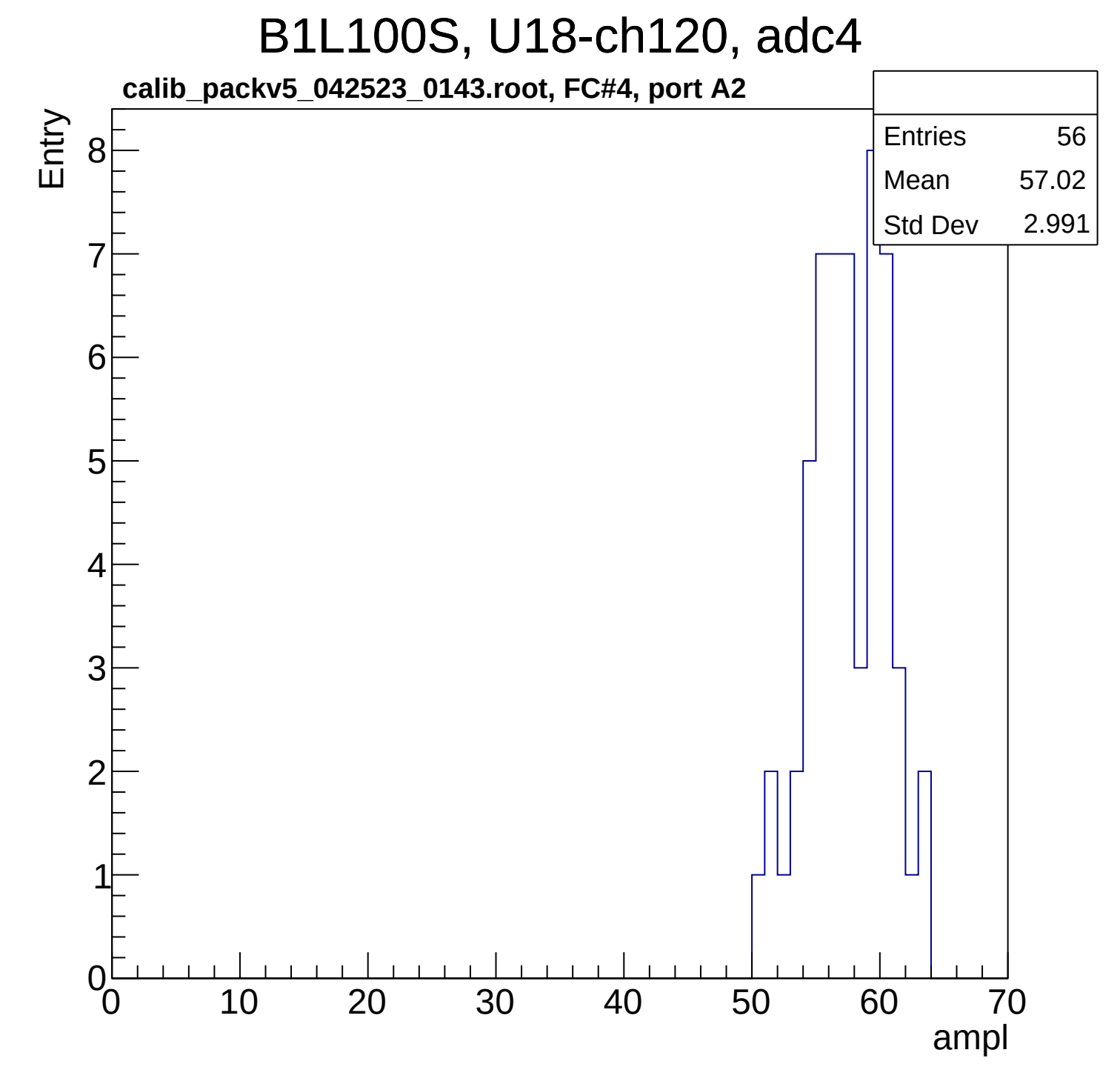

B1L100S, U18-ch119, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

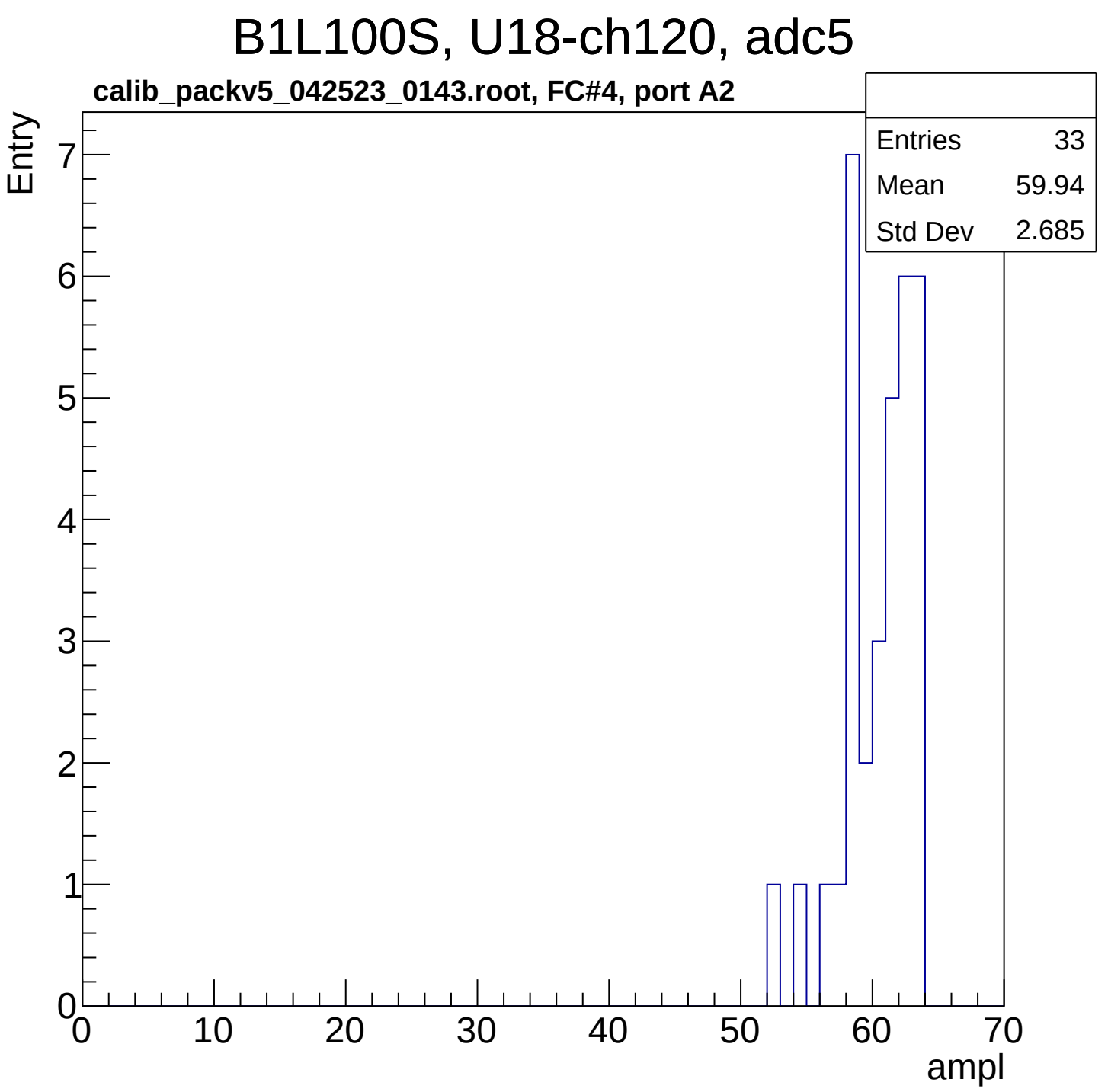

B1L100S, U18-ch120, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 29.71
Std Dev 5
Gaus mean : 30.8755
Gaus Width: 3.9461
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

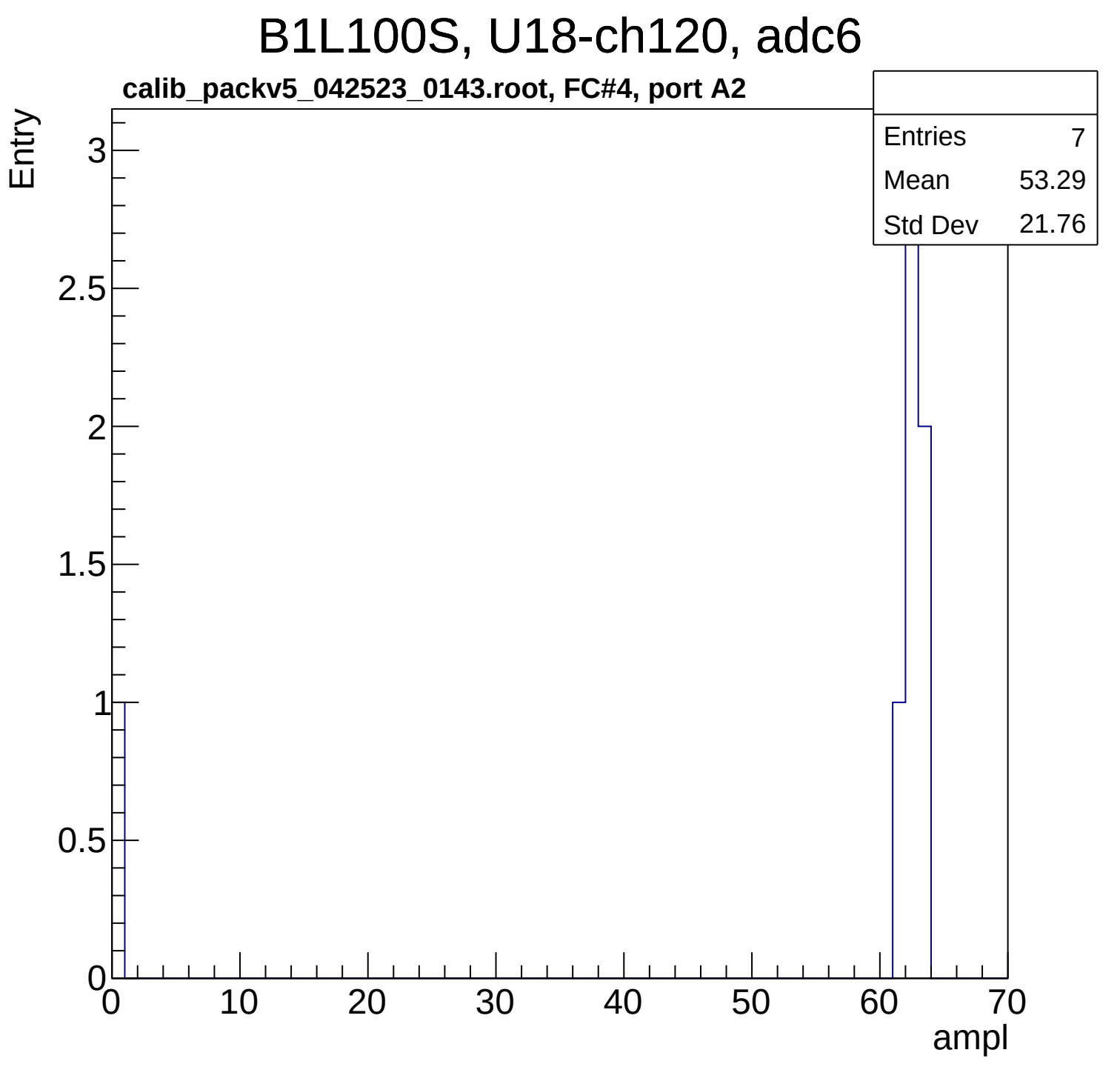

B1L100S, U18-ch120, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 36.02
Std Dev 3.748
Gaus mean : 35.9914
Gaus Width: 4.5902
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

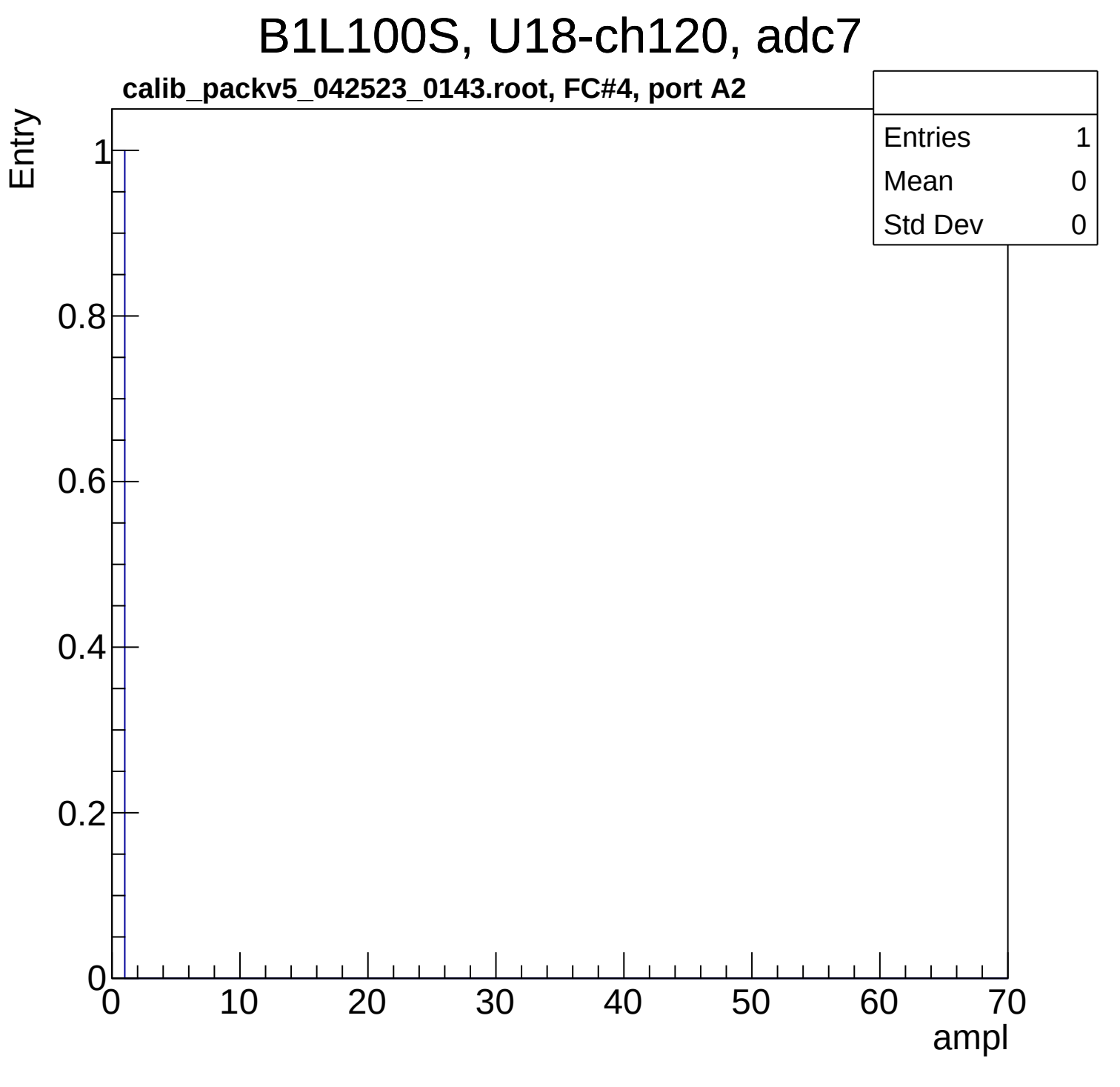

B1L100S, U18-ch120, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 75
Mean 43.01
Std Dev 3.89
Gaus mean : 43.7867
Gaus Width: 4.2736
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

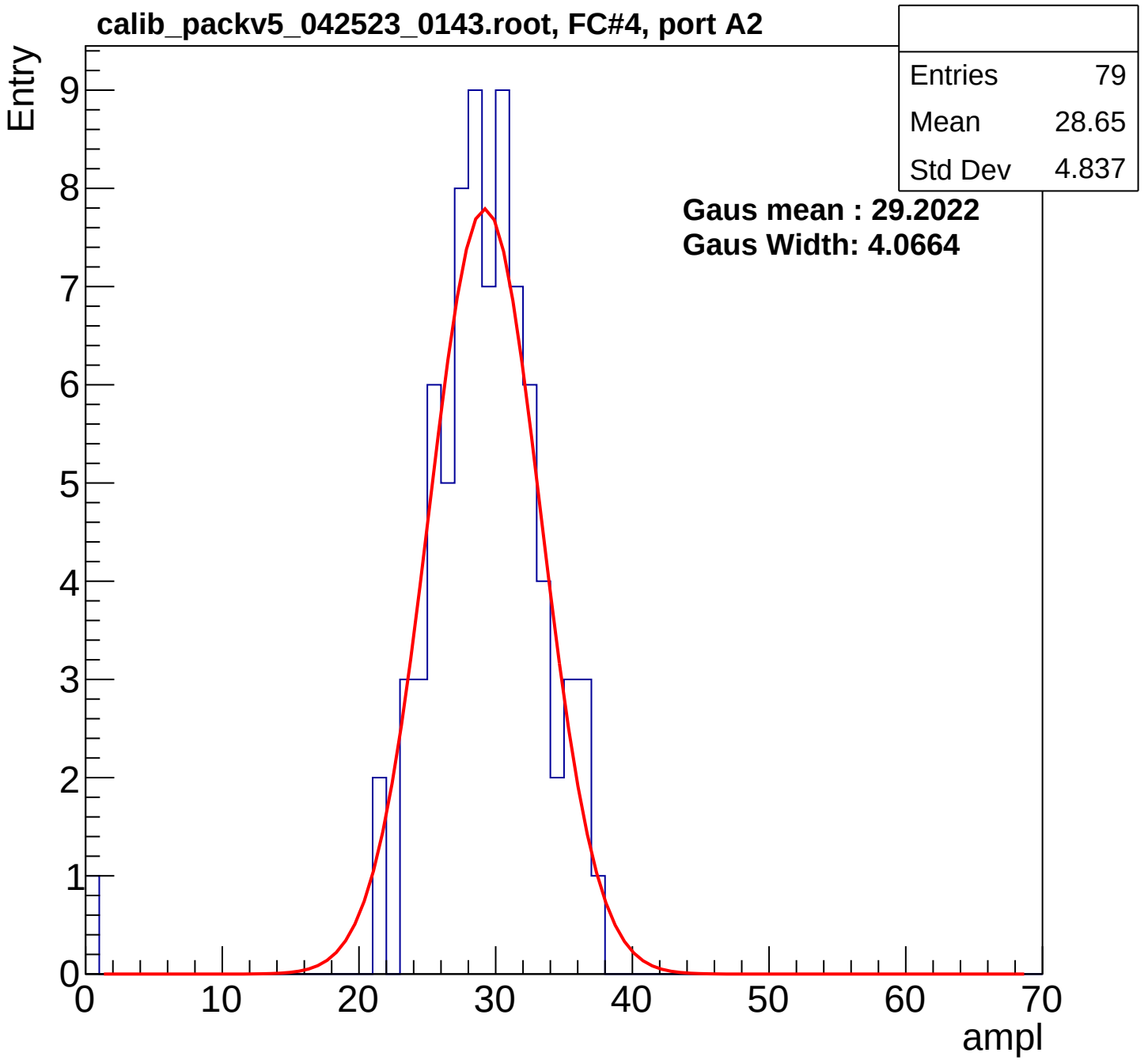

B1L100S, U18-ch120, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 74
Mean 49.91
Std Dev 4.094
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

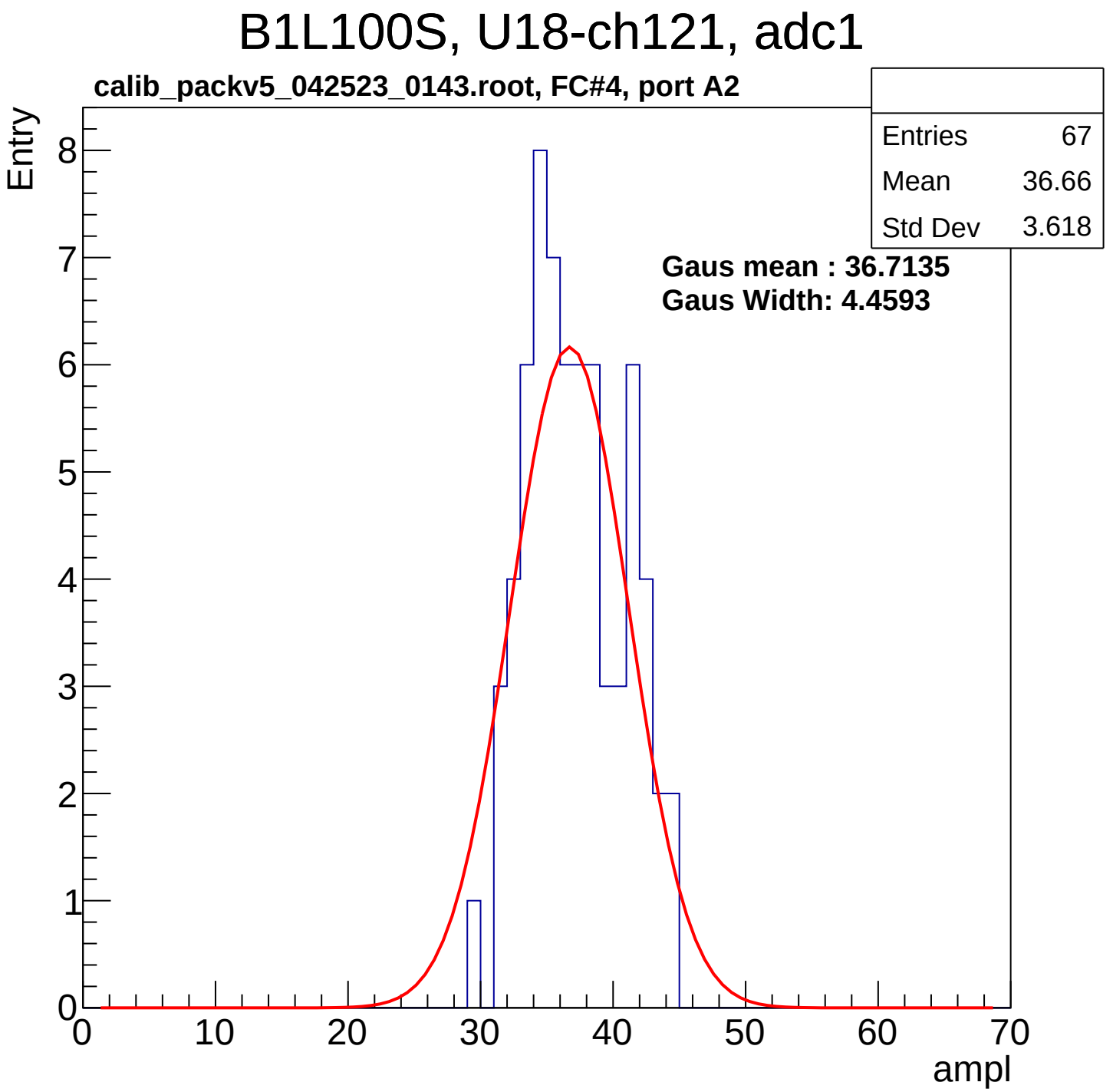

B1L100S, U18-ch120, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 57.02
Std Dev 2.991
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

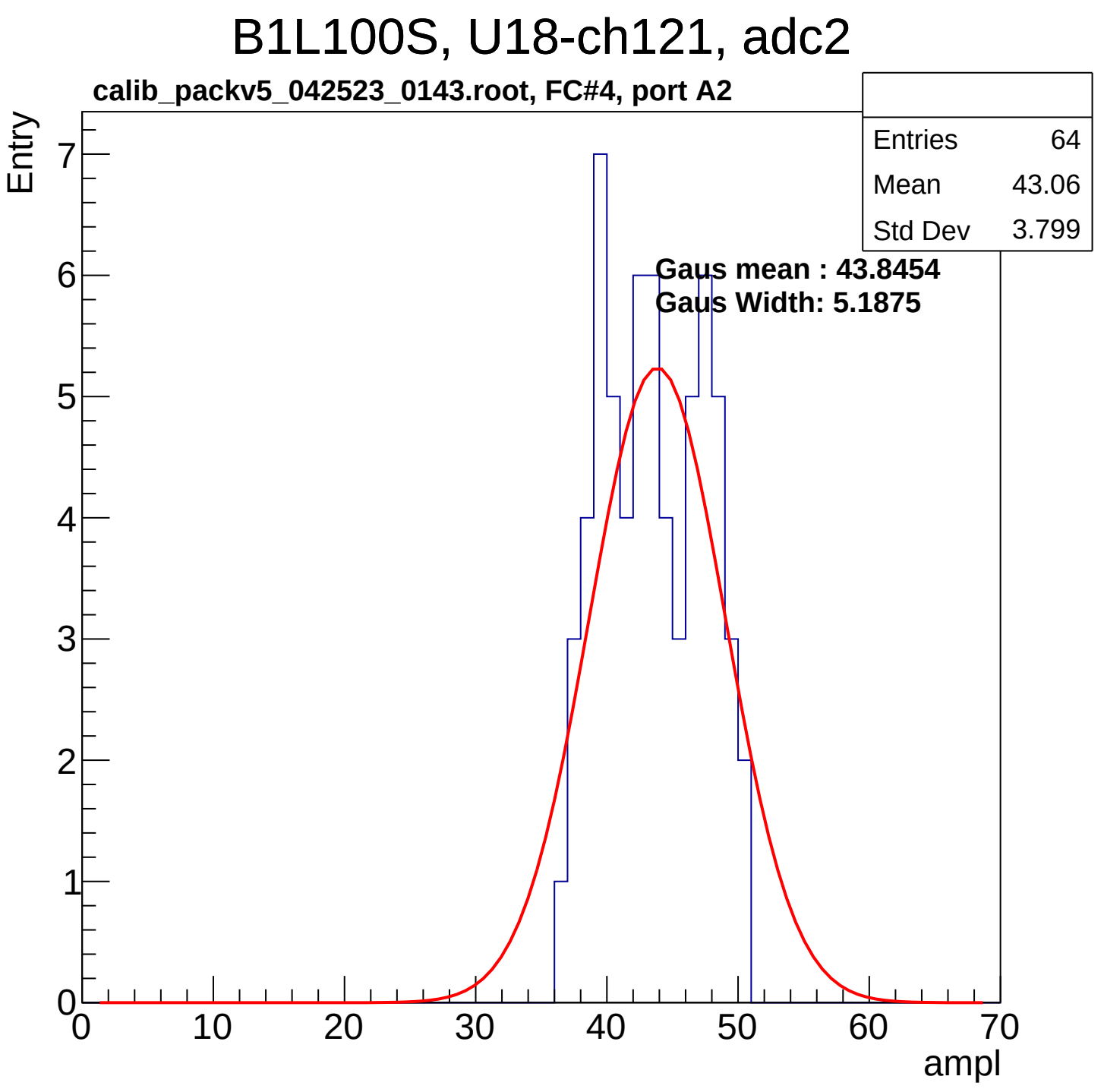

B1L100S, U18-ch120, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 33
Mean 59.94
Std Dev 2.685
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

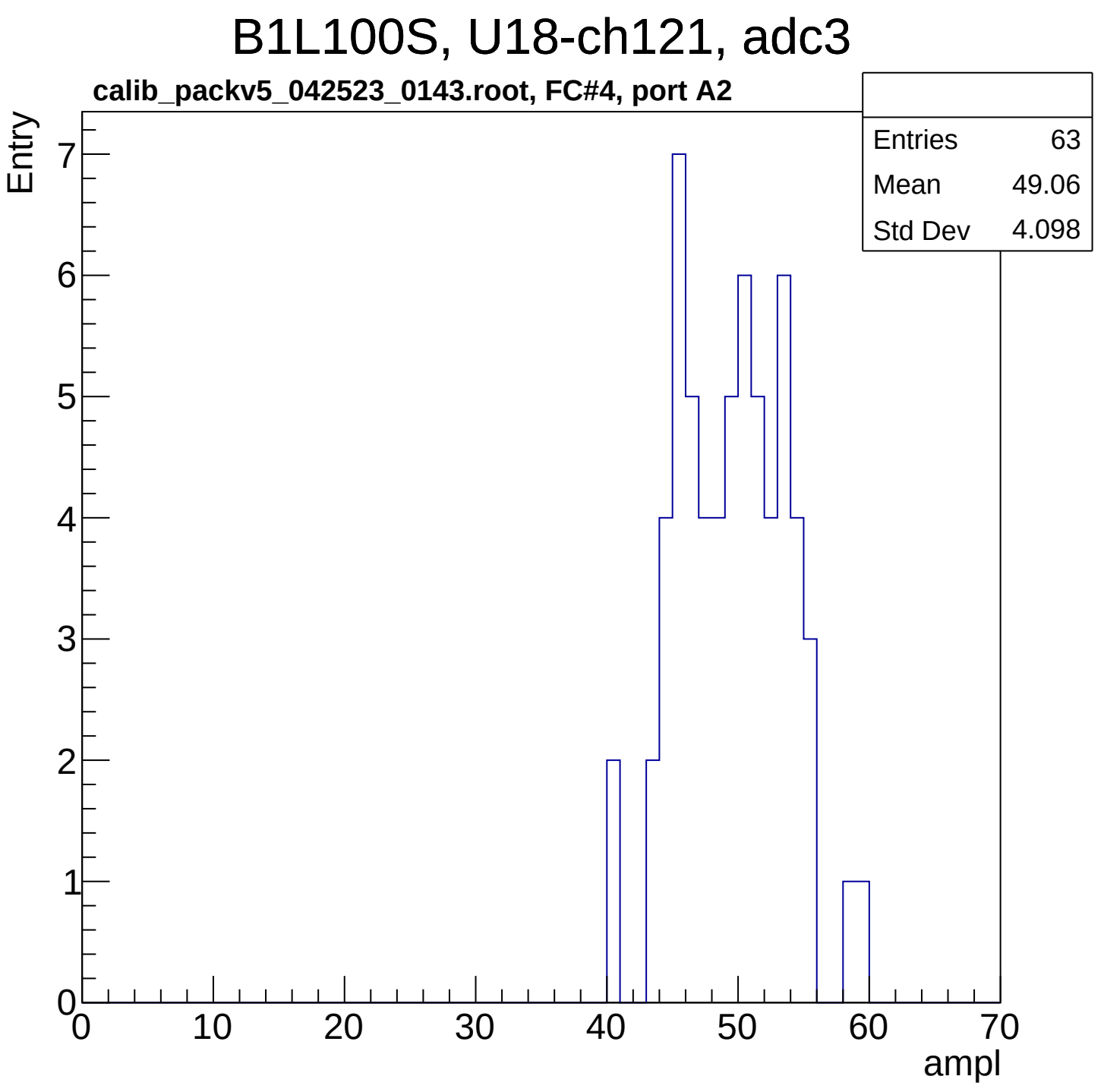

B1L100S, U18-ch120, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 53.29
Std Dev 21.76
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

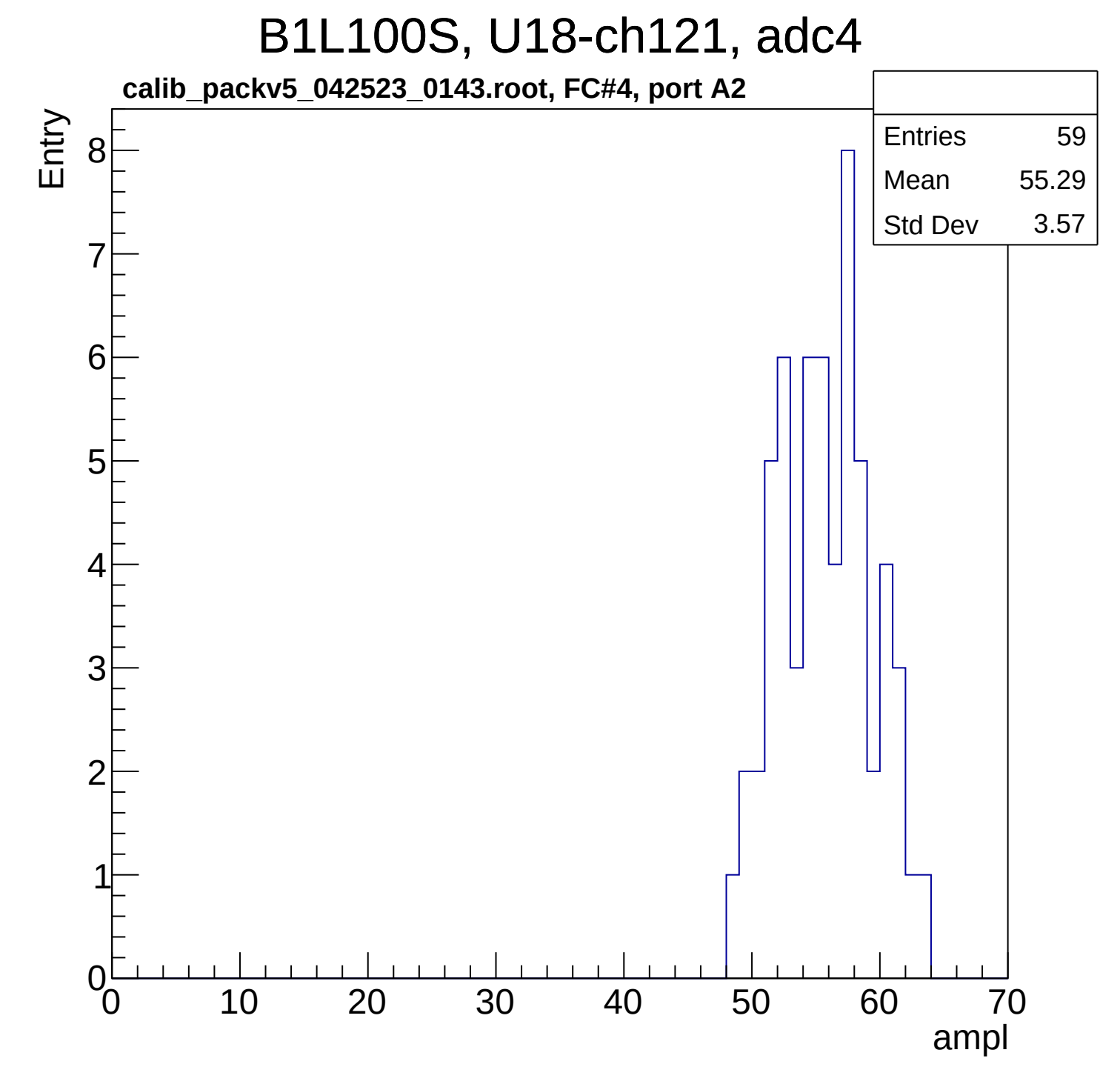

B1L100S, U18-ch120, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

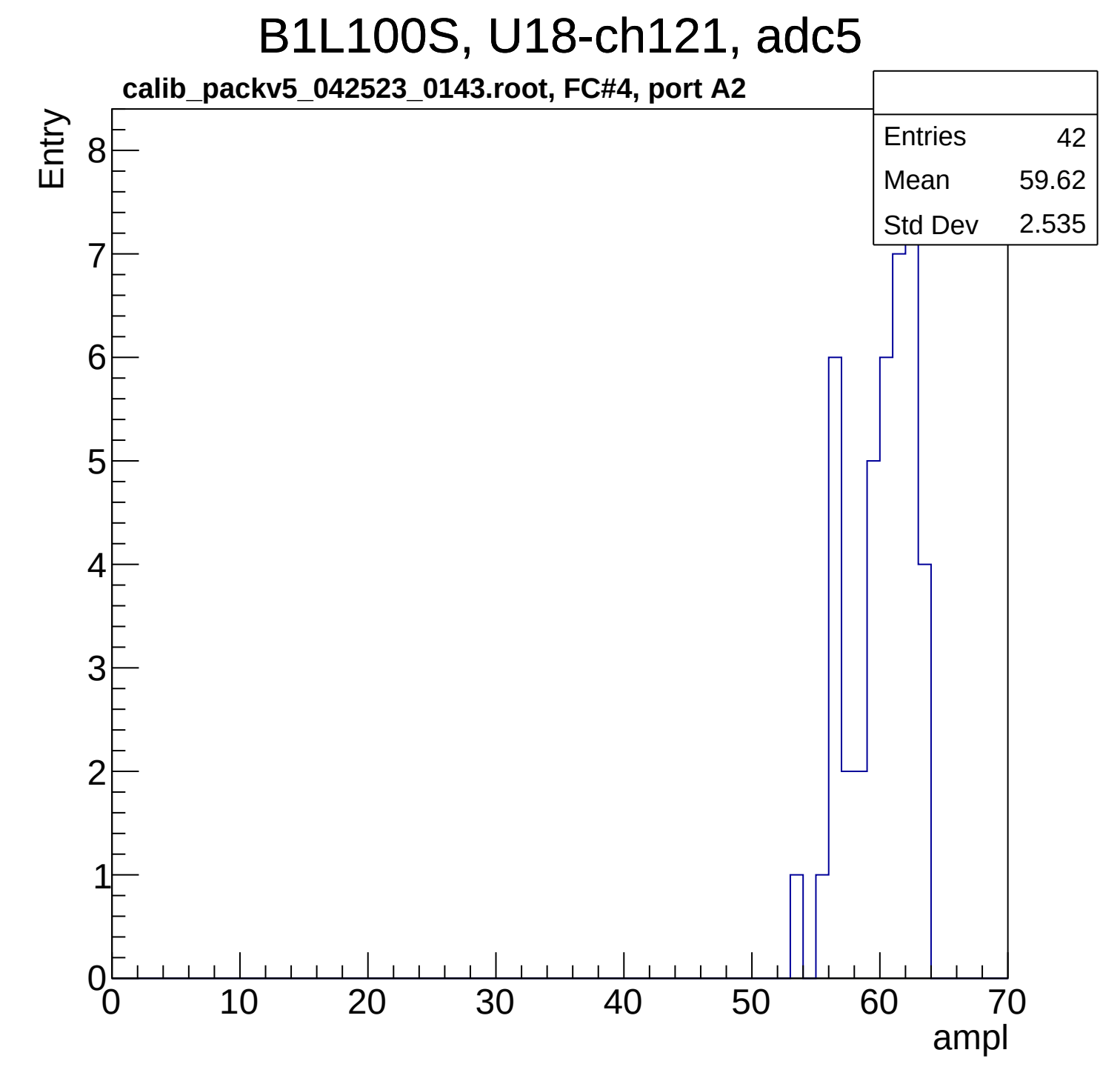

B1L100S, U18-ch121, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 79
Mean 28.65
Std Dev 4.837
Gaus mean : 29.2022
Gaus Width: 4.0664
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

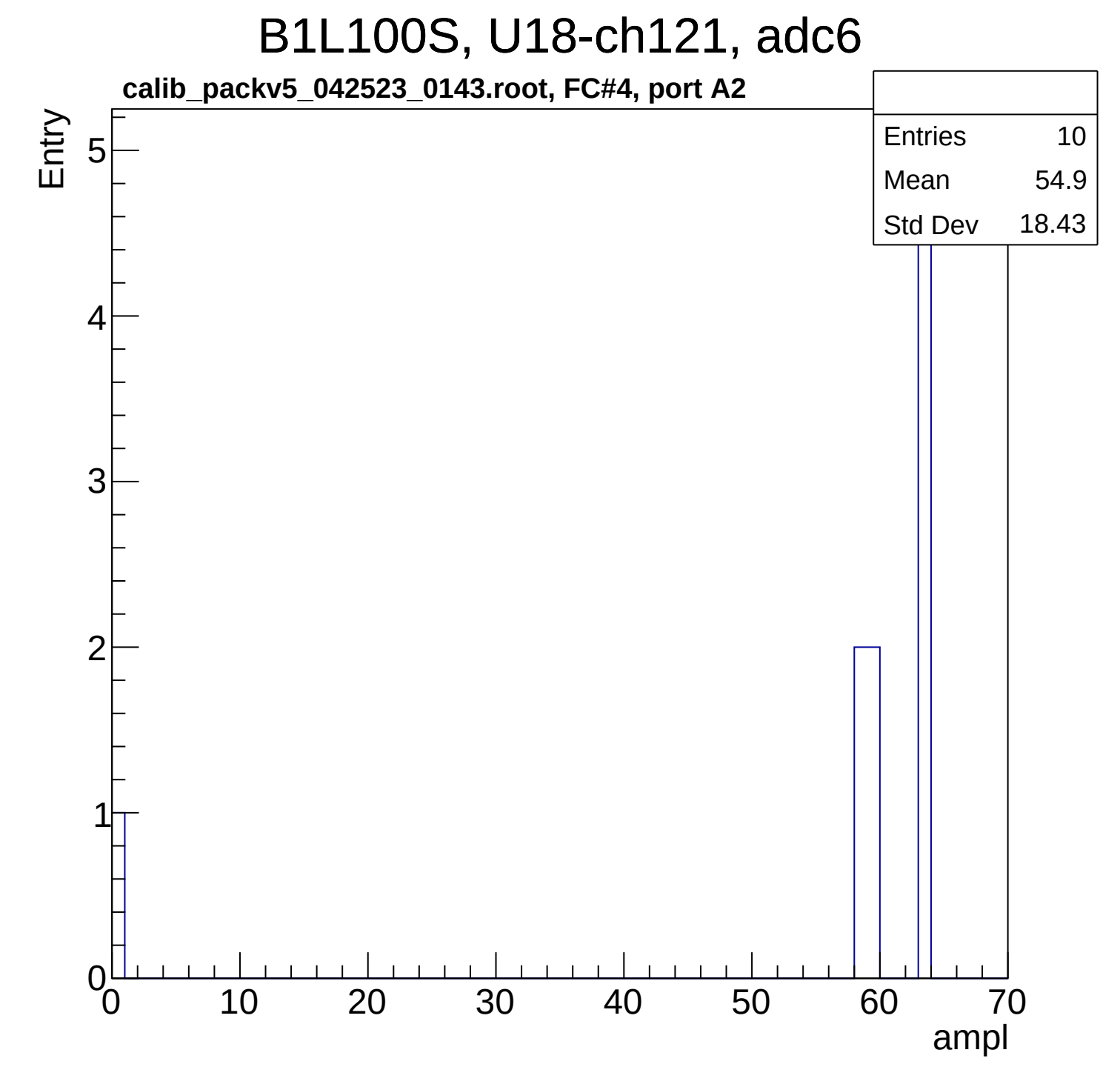

B1L100S, U18-ch121, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 67
Mean 36.66
Std Dev 3.618
Gaus mean : 36.7135
Gaus Width: 4.4593
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

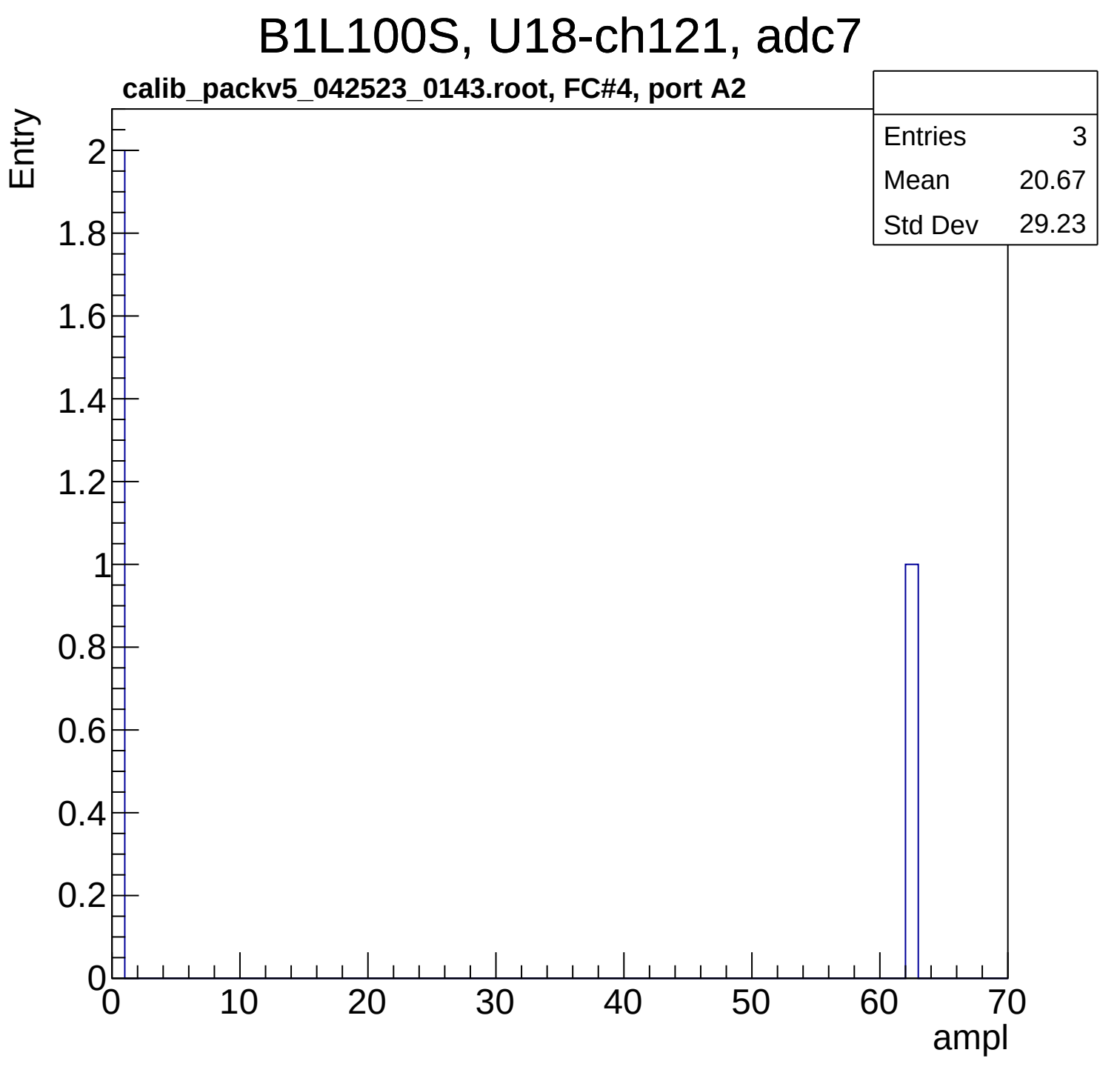

B1L100S, U18-ch121, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 64
Mean 43.06
Std Dev 3.799
Gaus mean : 43.8454
Gaus Width: 5.1875
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

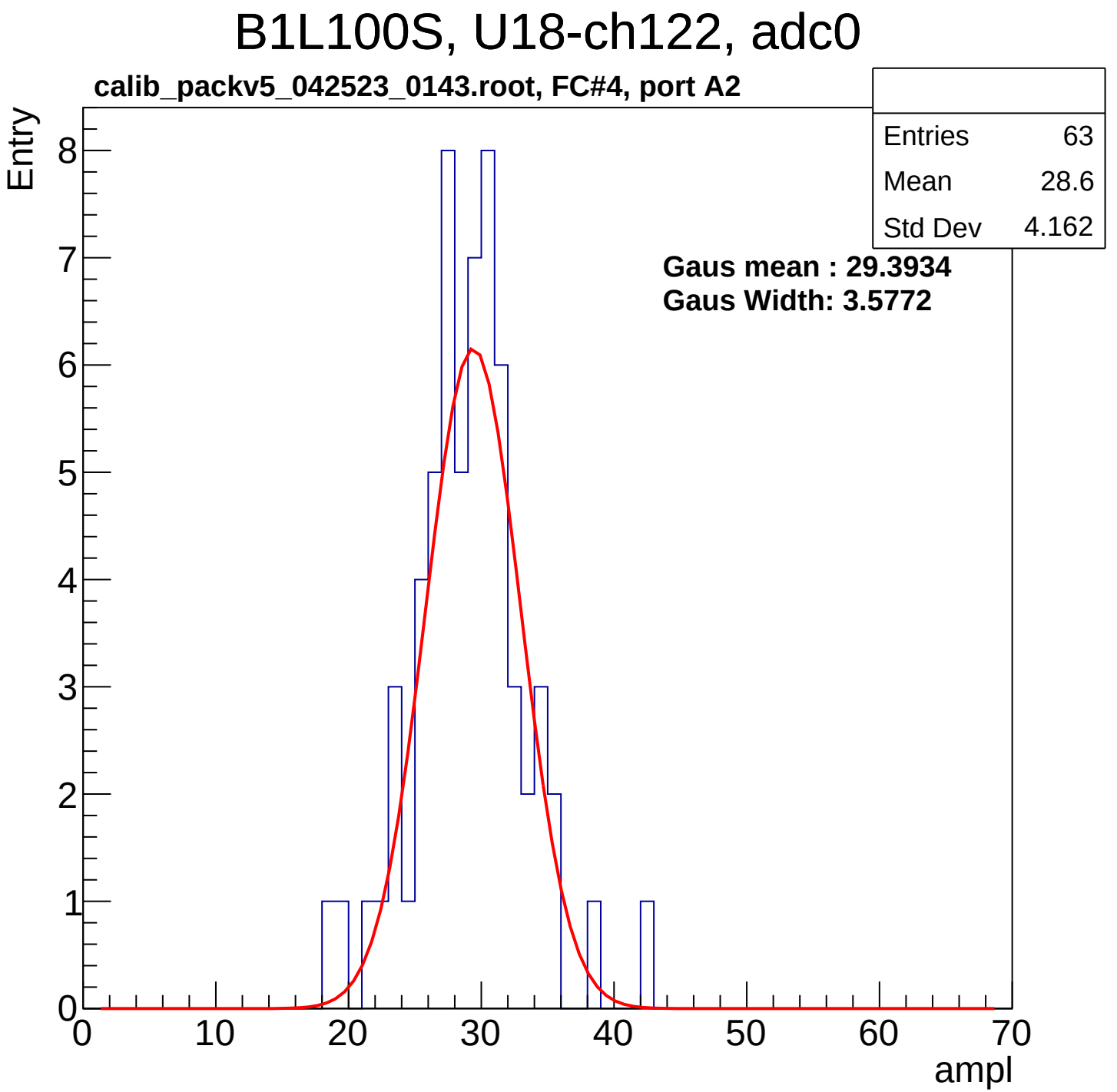

B1L100S, U18-ch121, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 49.06
Std Dev 4.098
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

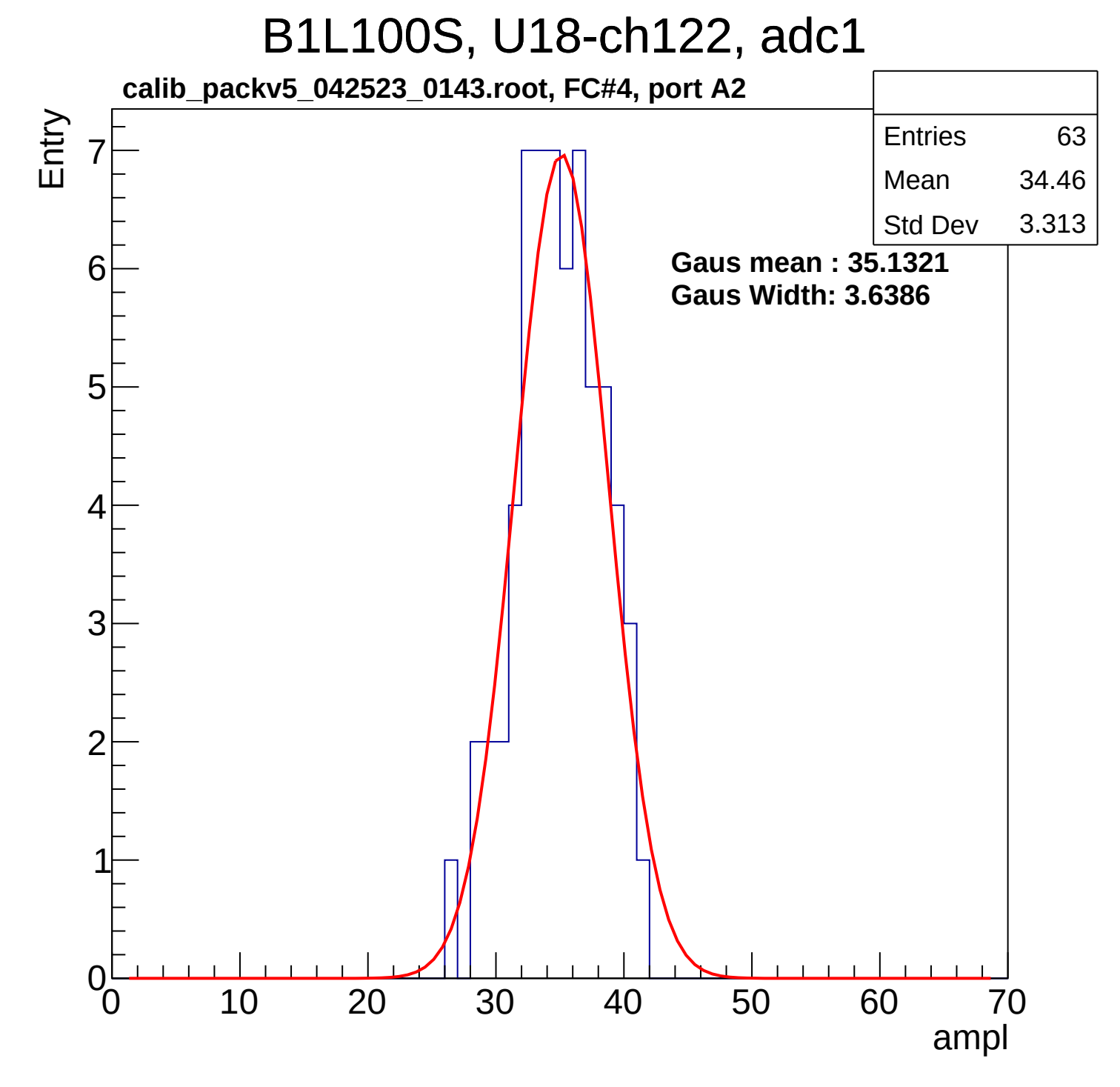

B1L100S, U18-ch121, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 55.29
Std Dev 3.57
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

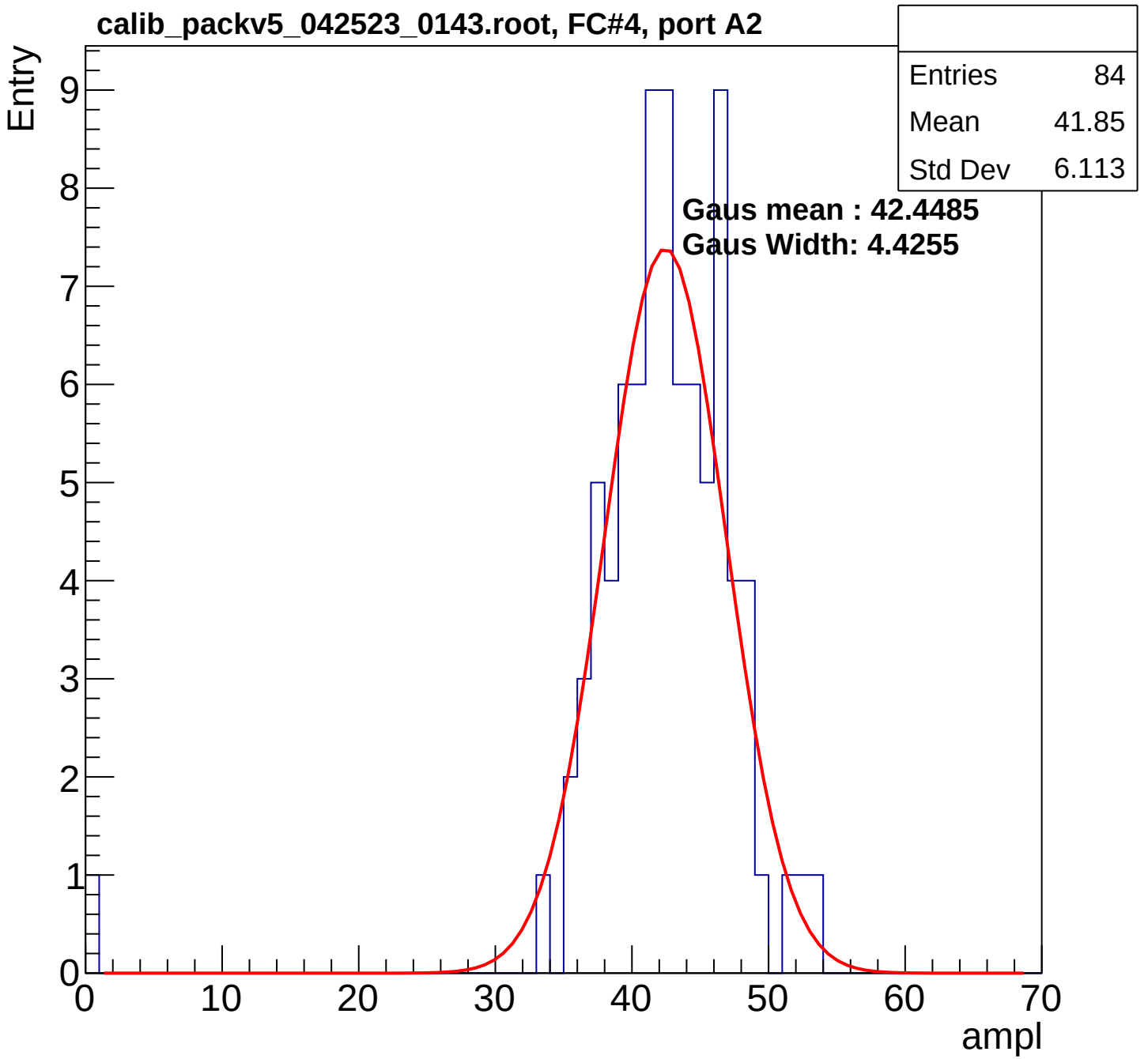

B1L100S, U18-ch121, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 42
Mean 59.62
Std Dev 2.535
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

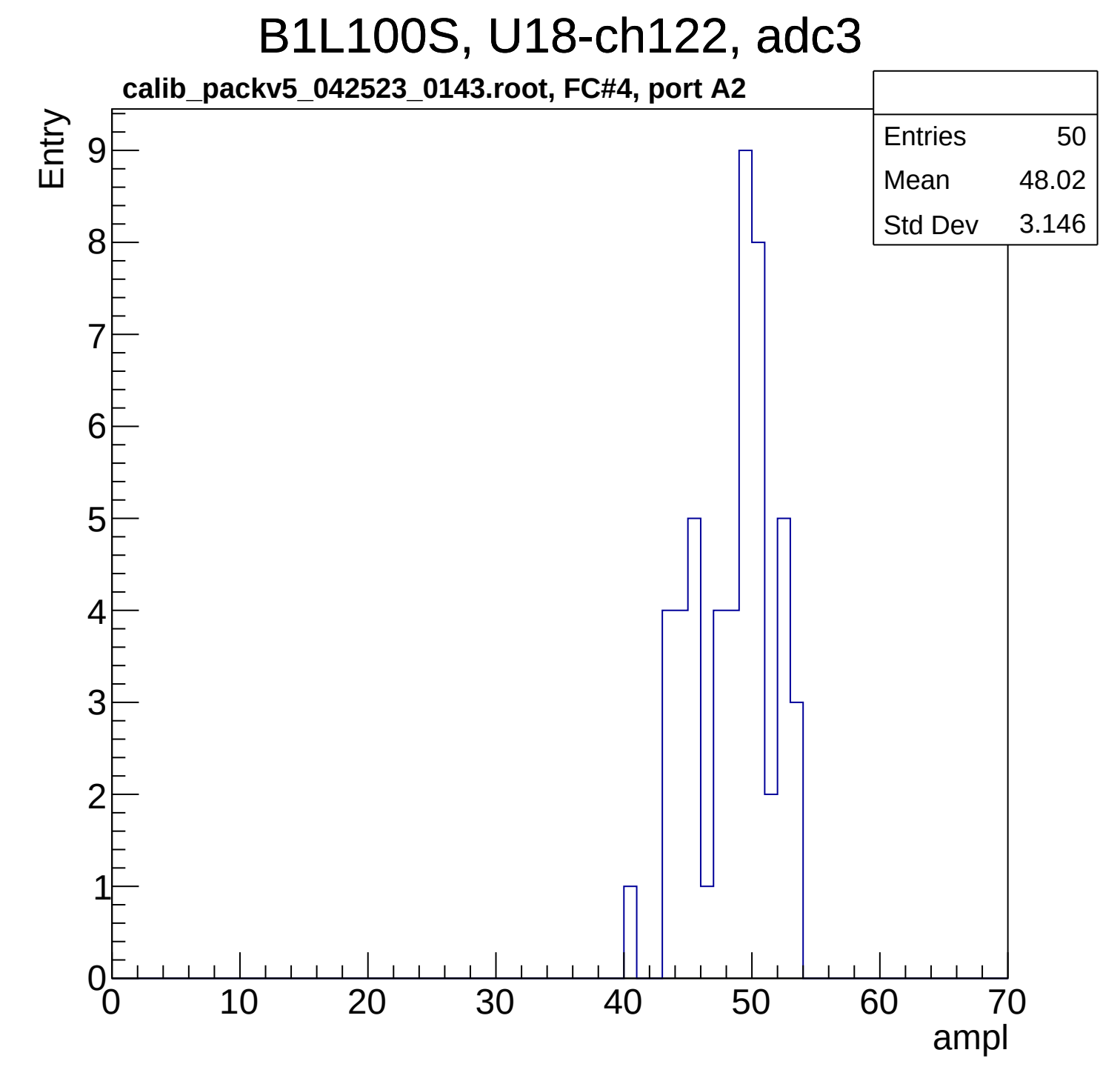

B1L100S, U18-ch121, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 54.9
Std Dev 18.43
Entry
0
1
2
3
4
5
0
10
20
30
40
50
60
70
ampl

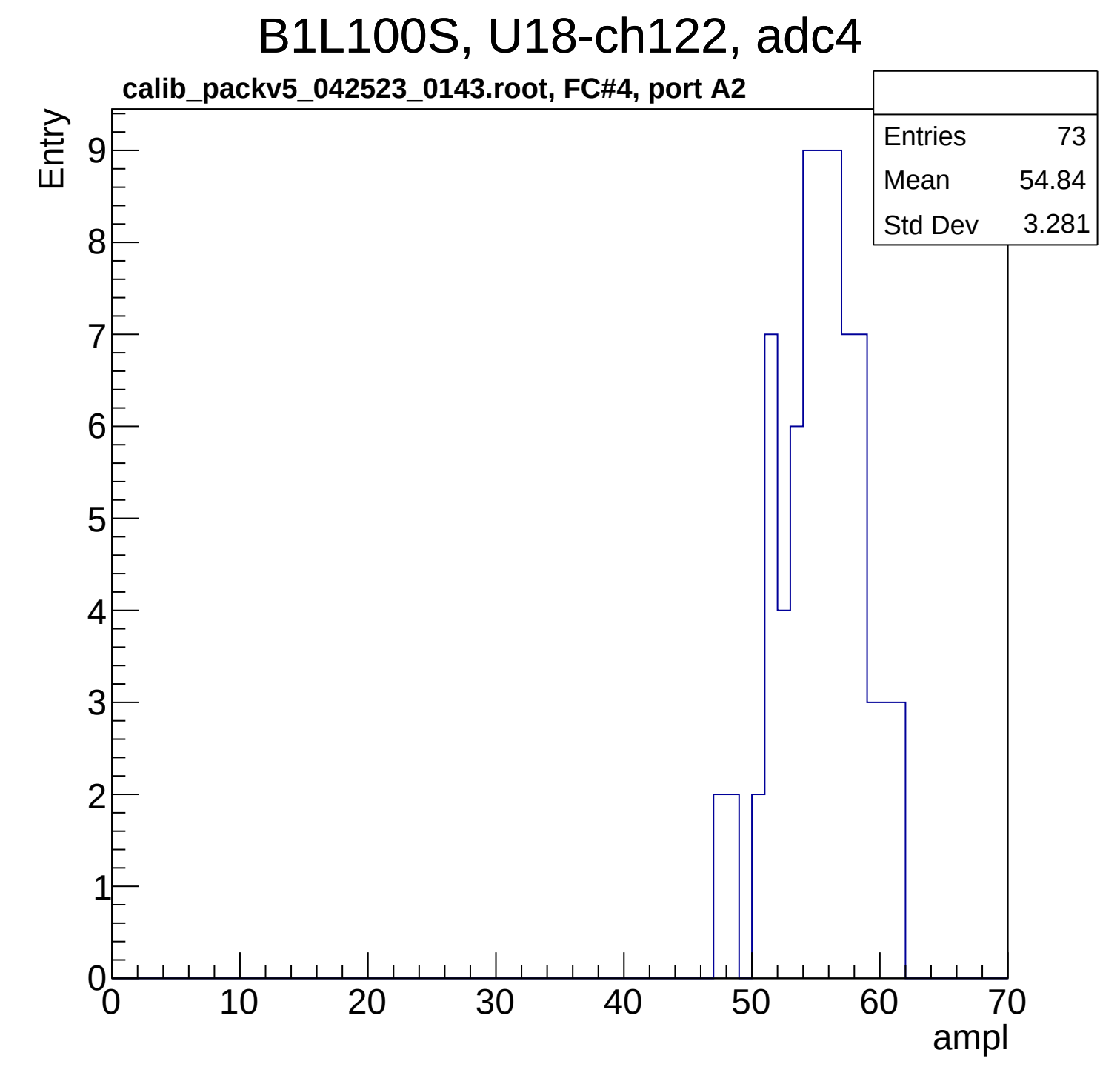

B1L100S, U18-ch121, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 3
Mean 20.67
Std Dev 29.23
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

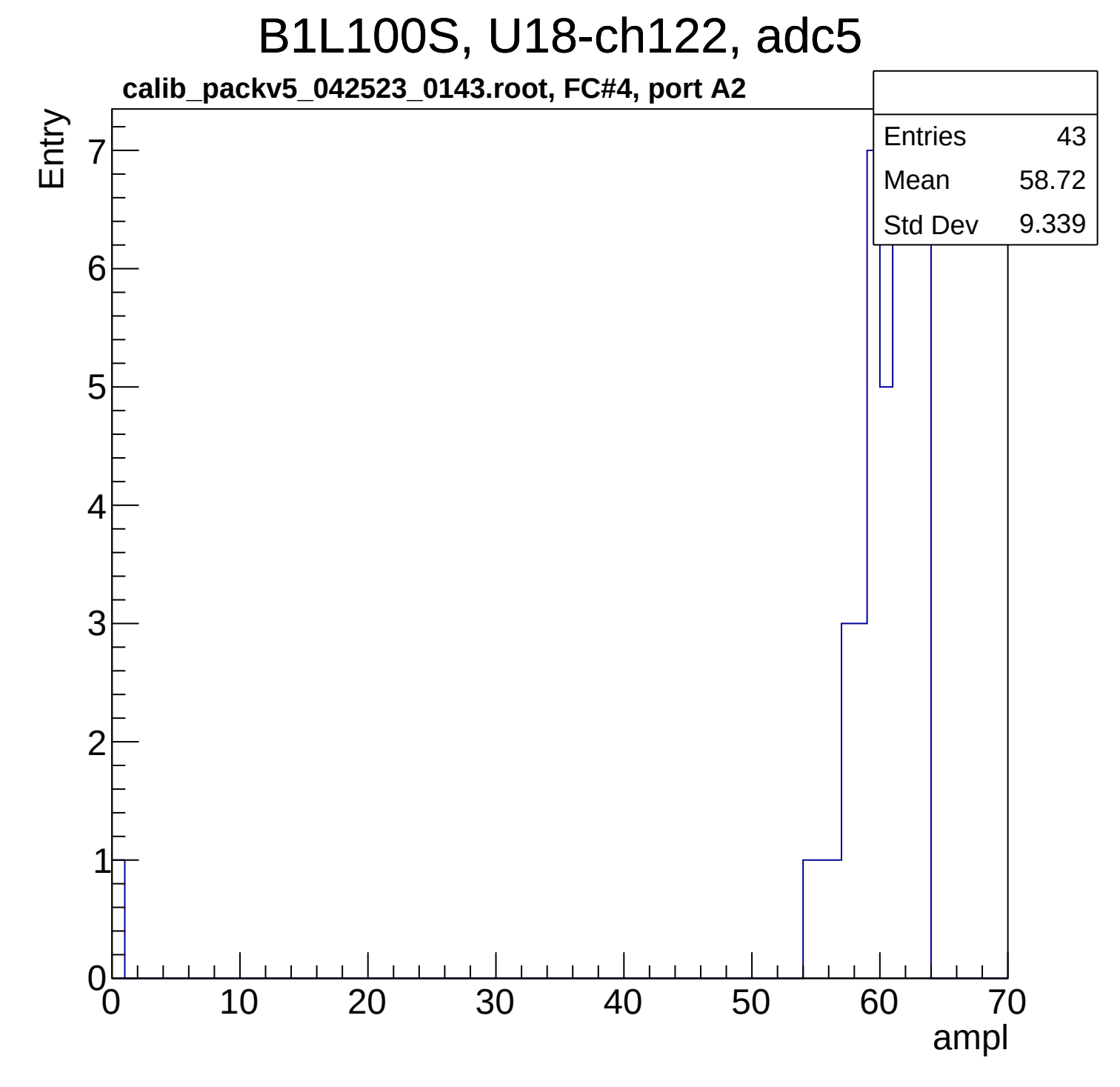

B1L100S, U18-ch122, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 28.6
Std Dev 4.162
Gaus mean : 29.3934
Gaus Width: 3.5772
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

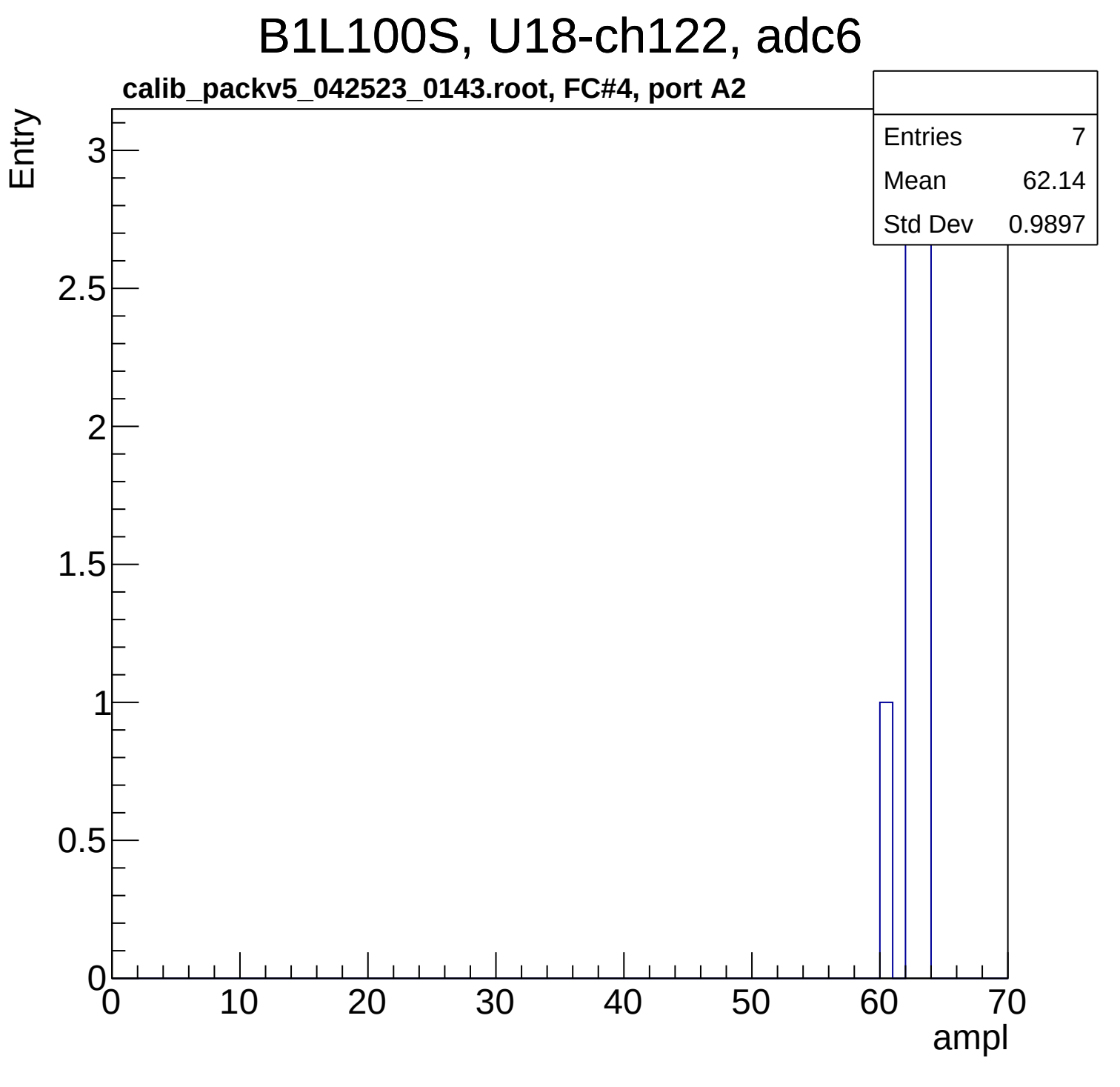

B1L100S, U18-ch122, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 34.46
Std Dev 3.313
Gaus mean : 35.1321
Gaus Width: 3.6386
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

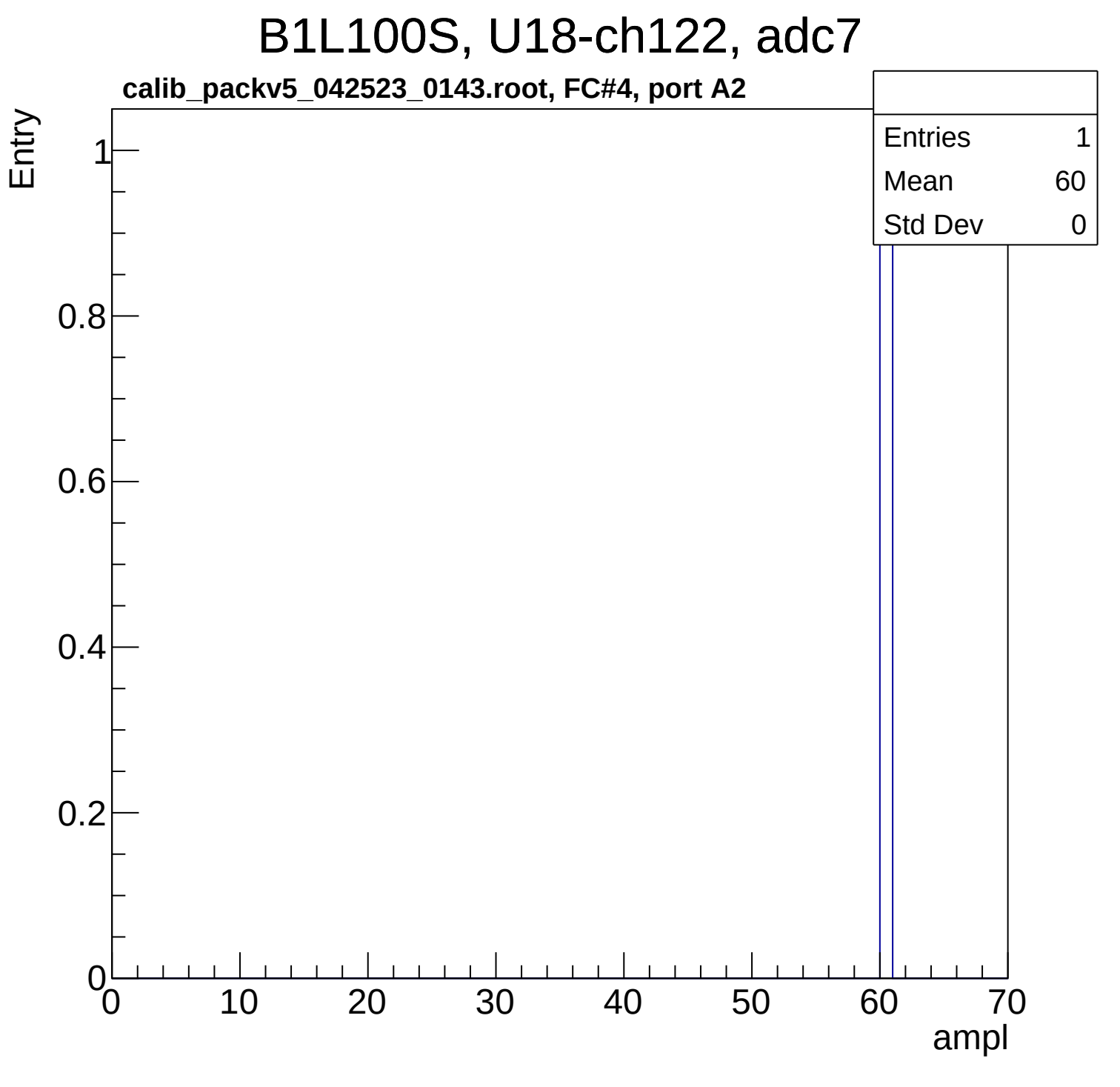

B1L100S, U18-ch122, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 84
Mean 41.85
Std Dev 6.113
Gaus mean : 42.4485
Gaus Width: 4.4255
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

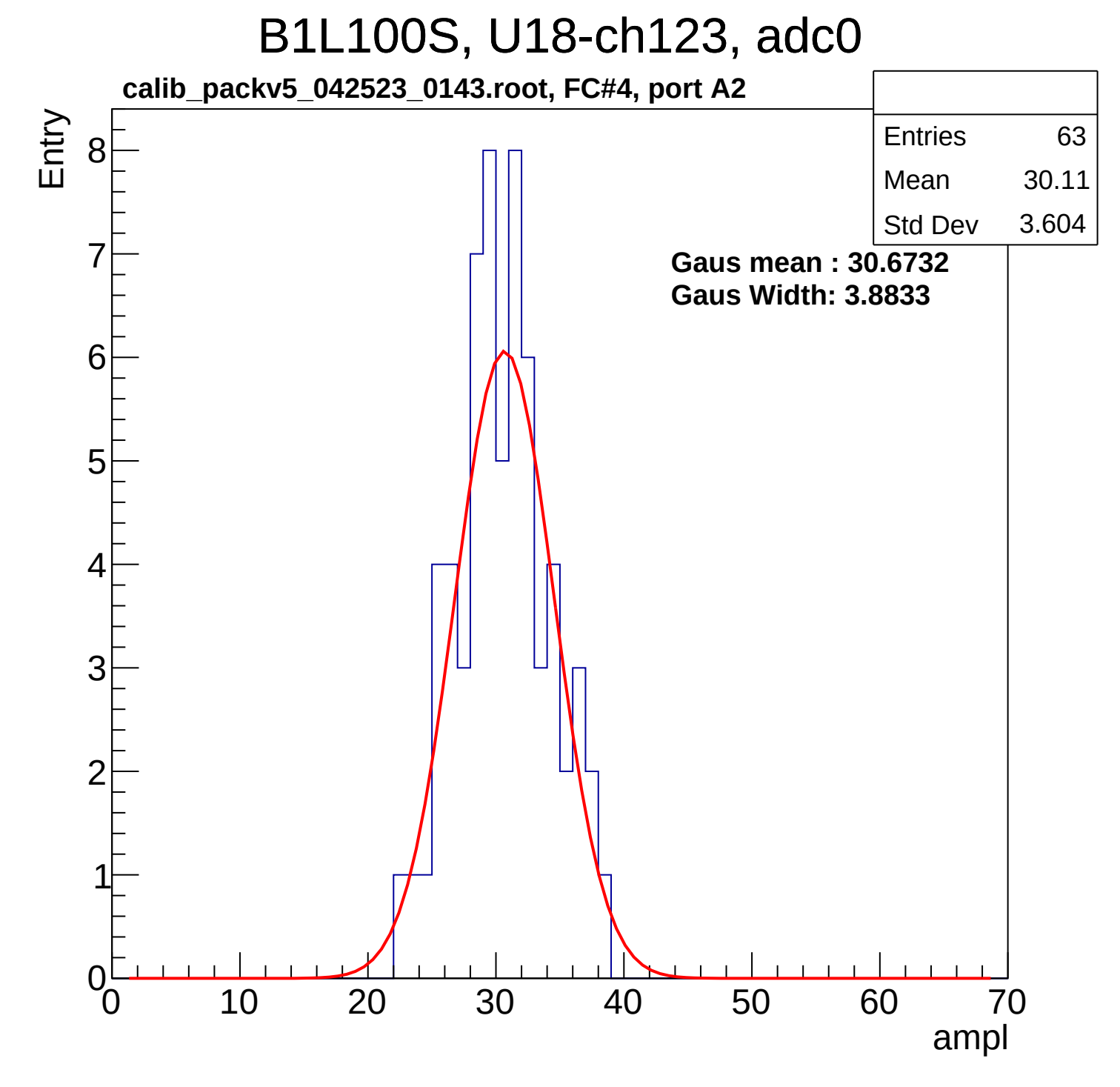

B1L100S, U18-ch122, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 48.02
Std Dev 3.146
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

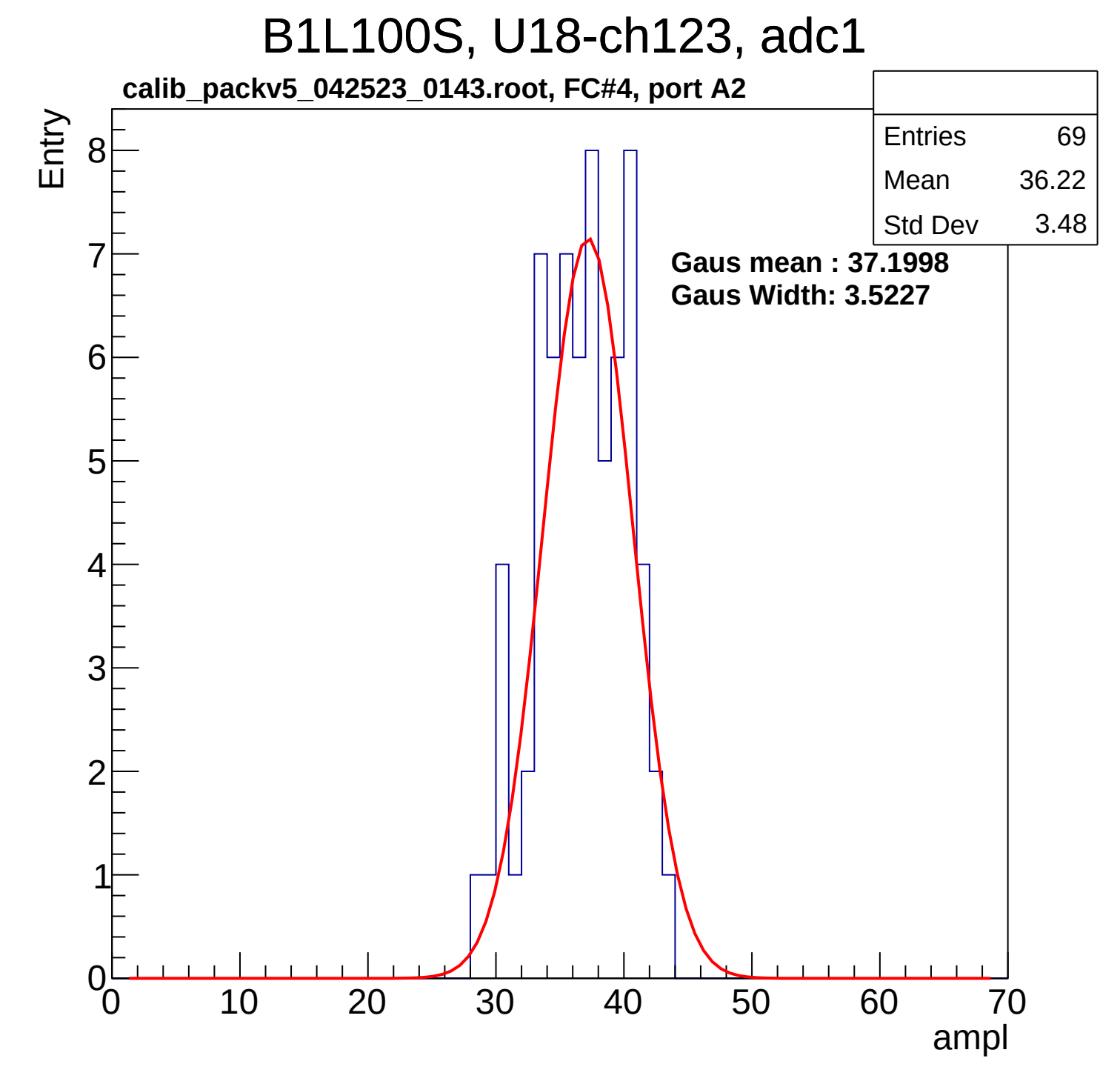

B1L100S, U18-ch122, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 73
Mean 54.84
Std Dev 3.281
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

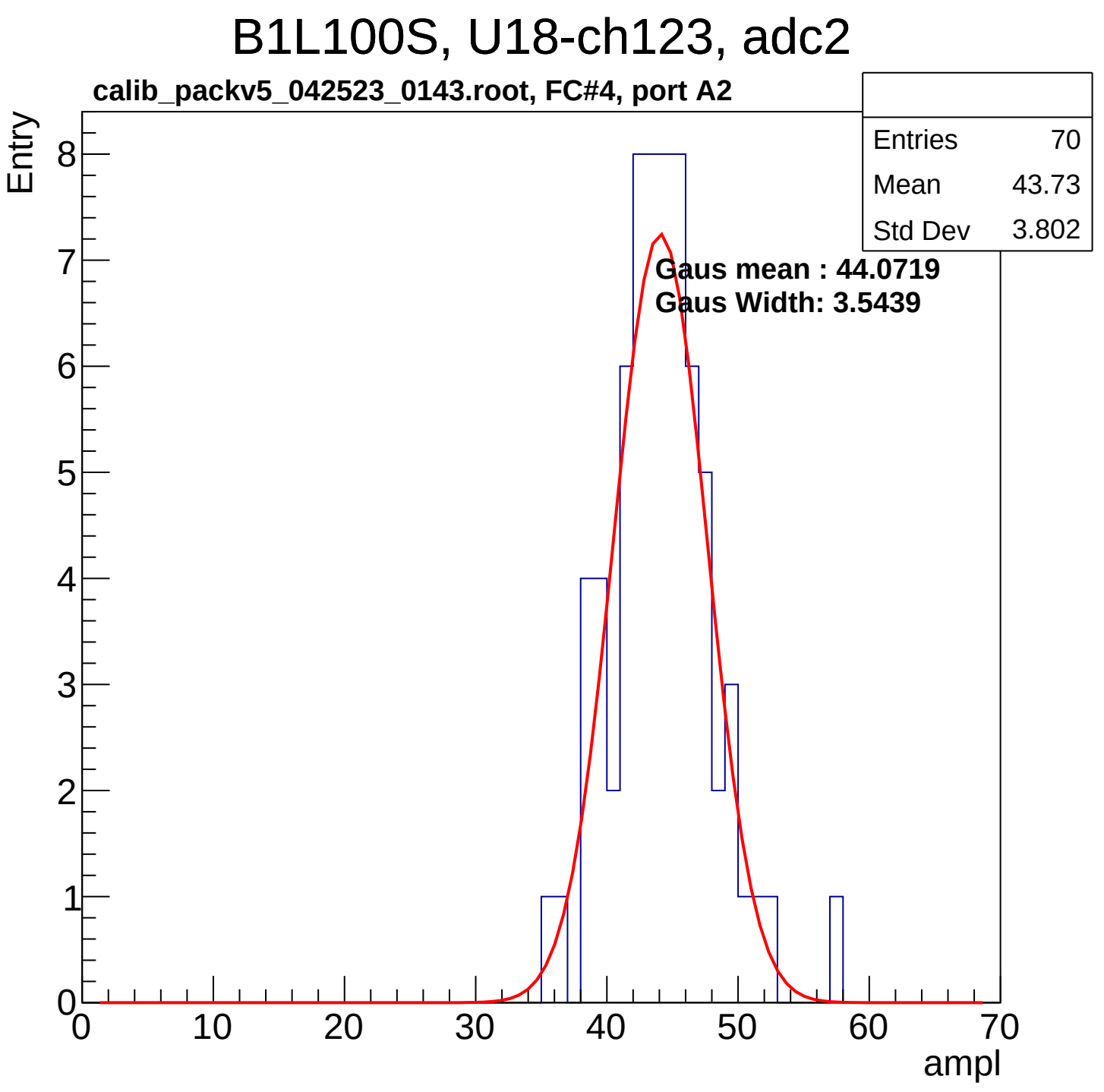

B1L100S, U18-ch122, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 58.72
Std Dev 9.339
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

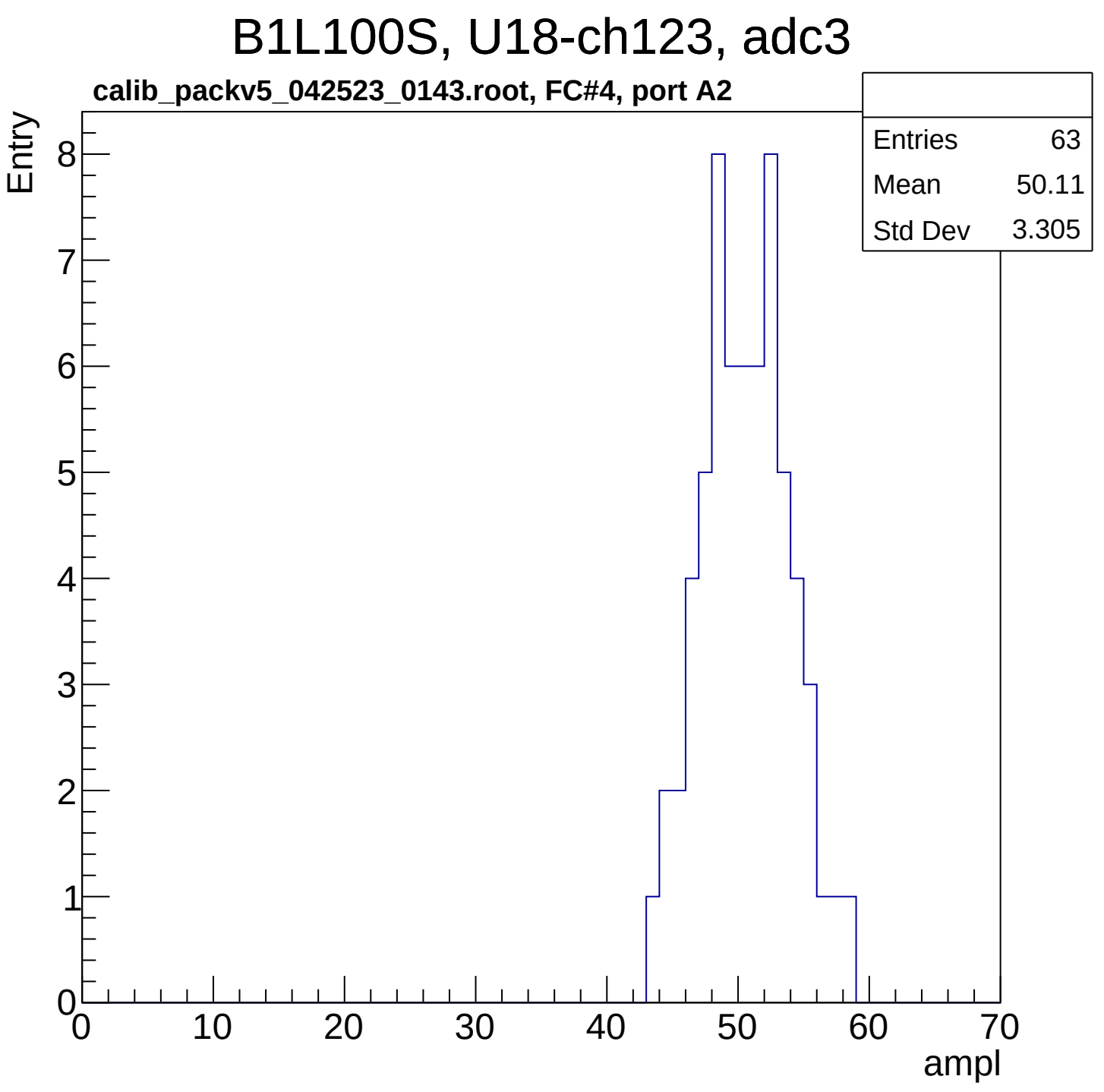

B1L100S, U18-ch122, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 7
Mean 62.14
Std Dev 0.9897
Entry
ampl
0
0.5
1
1.5
2
2.5
3
0
10
20
30
40
50
60
70

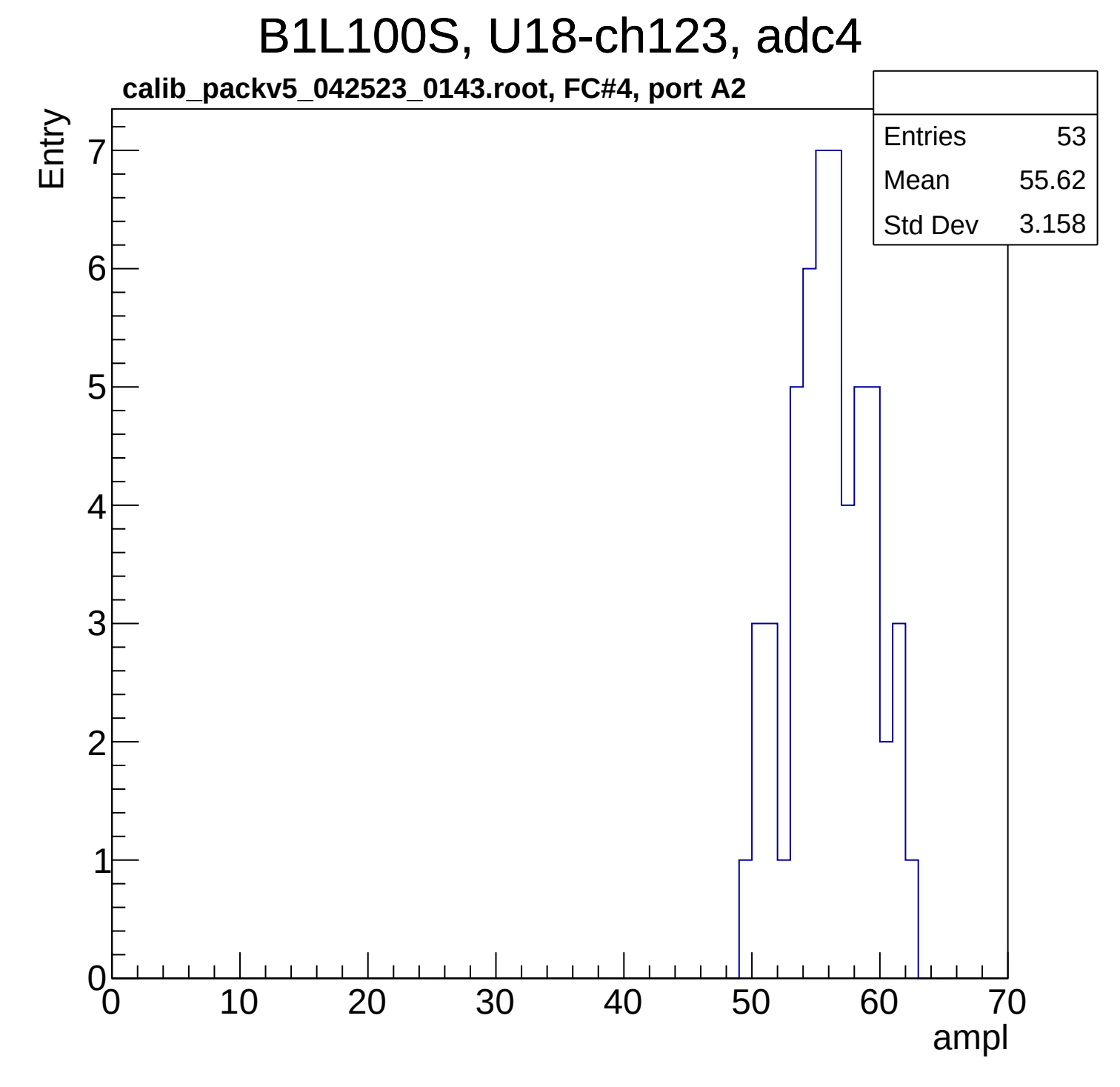

B1L100S, U18-ch122, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 60
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

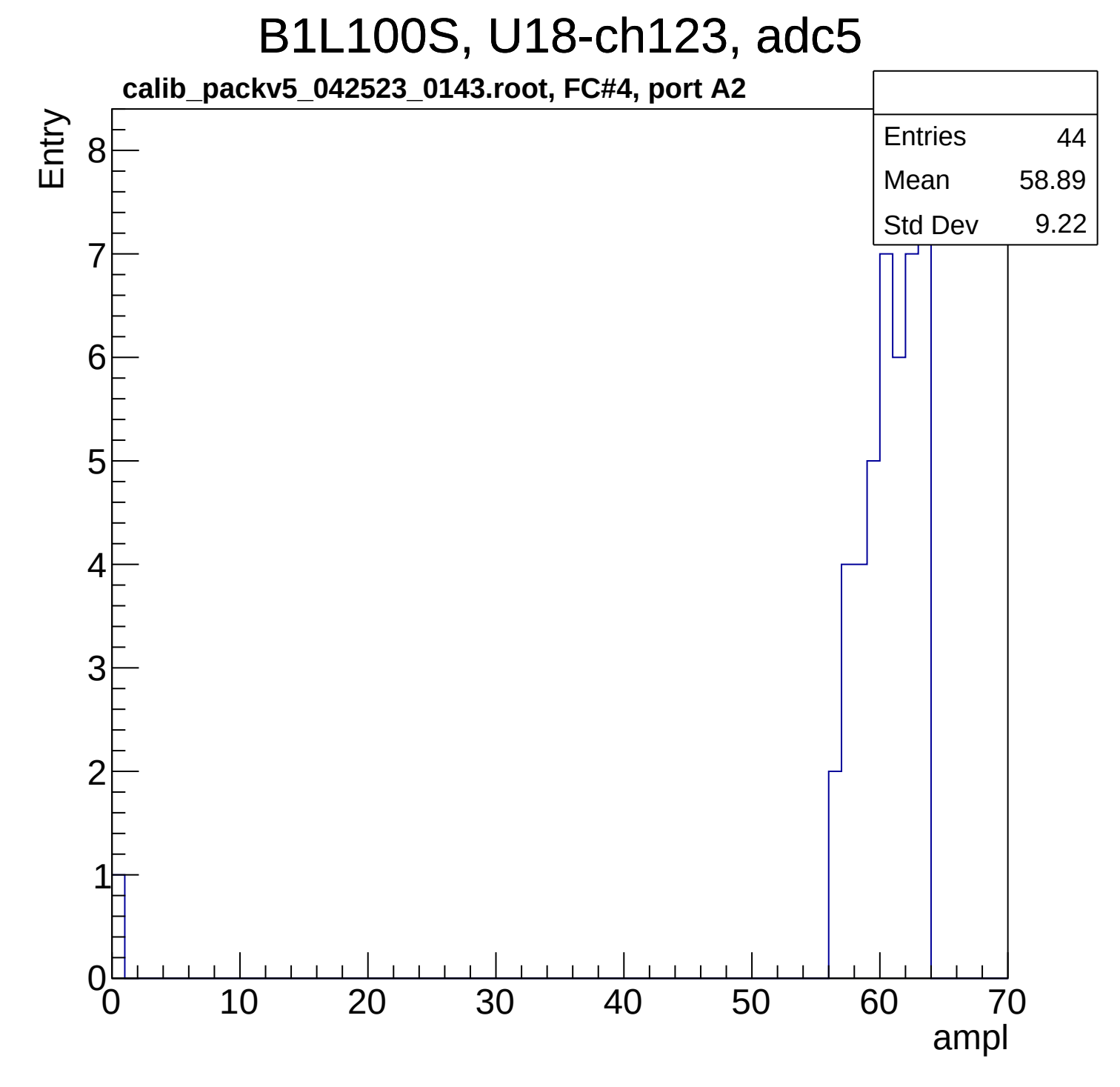

B1L100S, U18-ch123, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 30.11
Std Dev 3.604
Gaus mean : 30.6732
Gaus Width: 3.8833
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

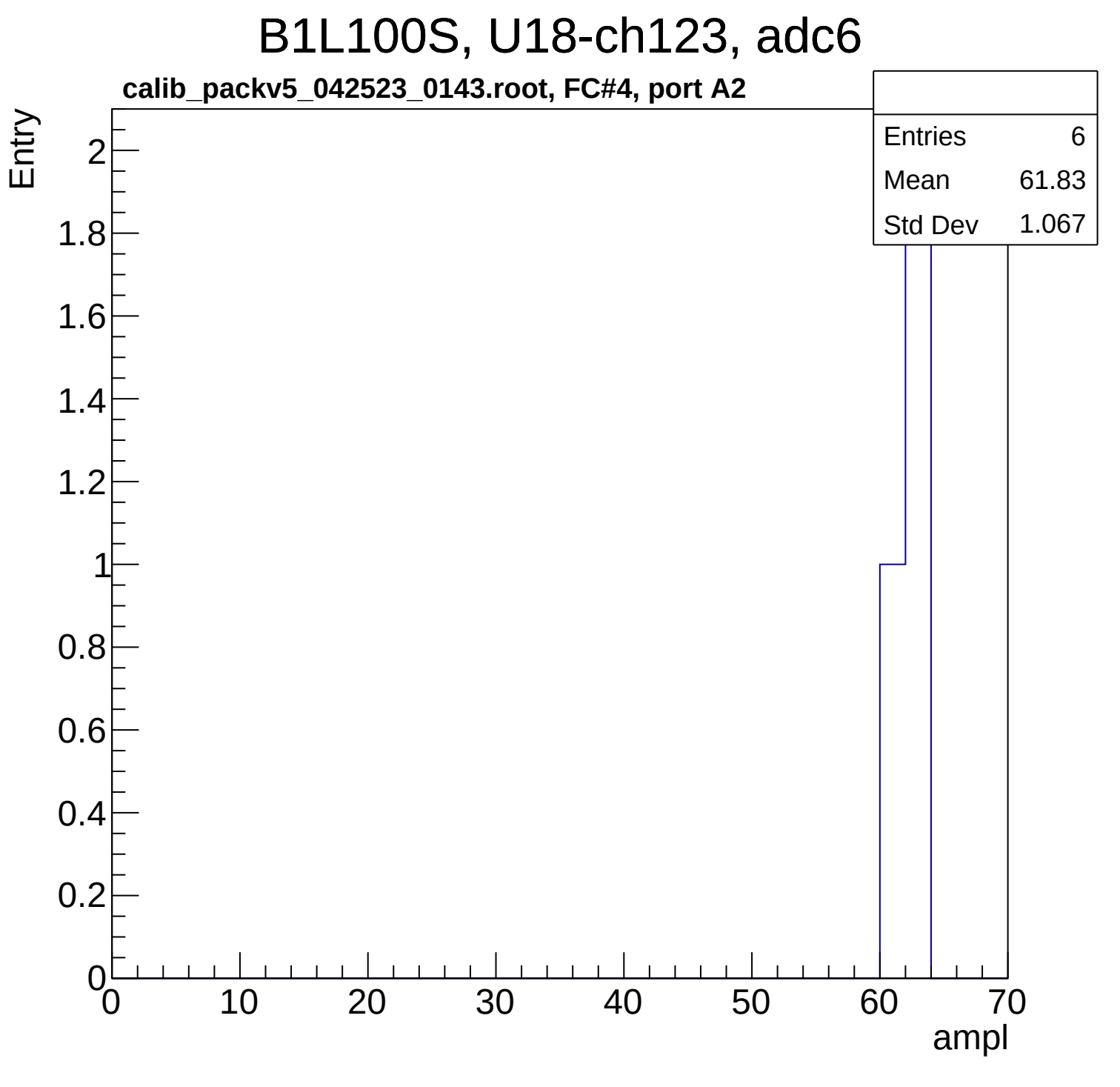

B1L100S, U18-ch123, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 69
Mean 36.22
Std Dev 3.48
Gaus mean : 37.1998
Gaus Width: 3.5227
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

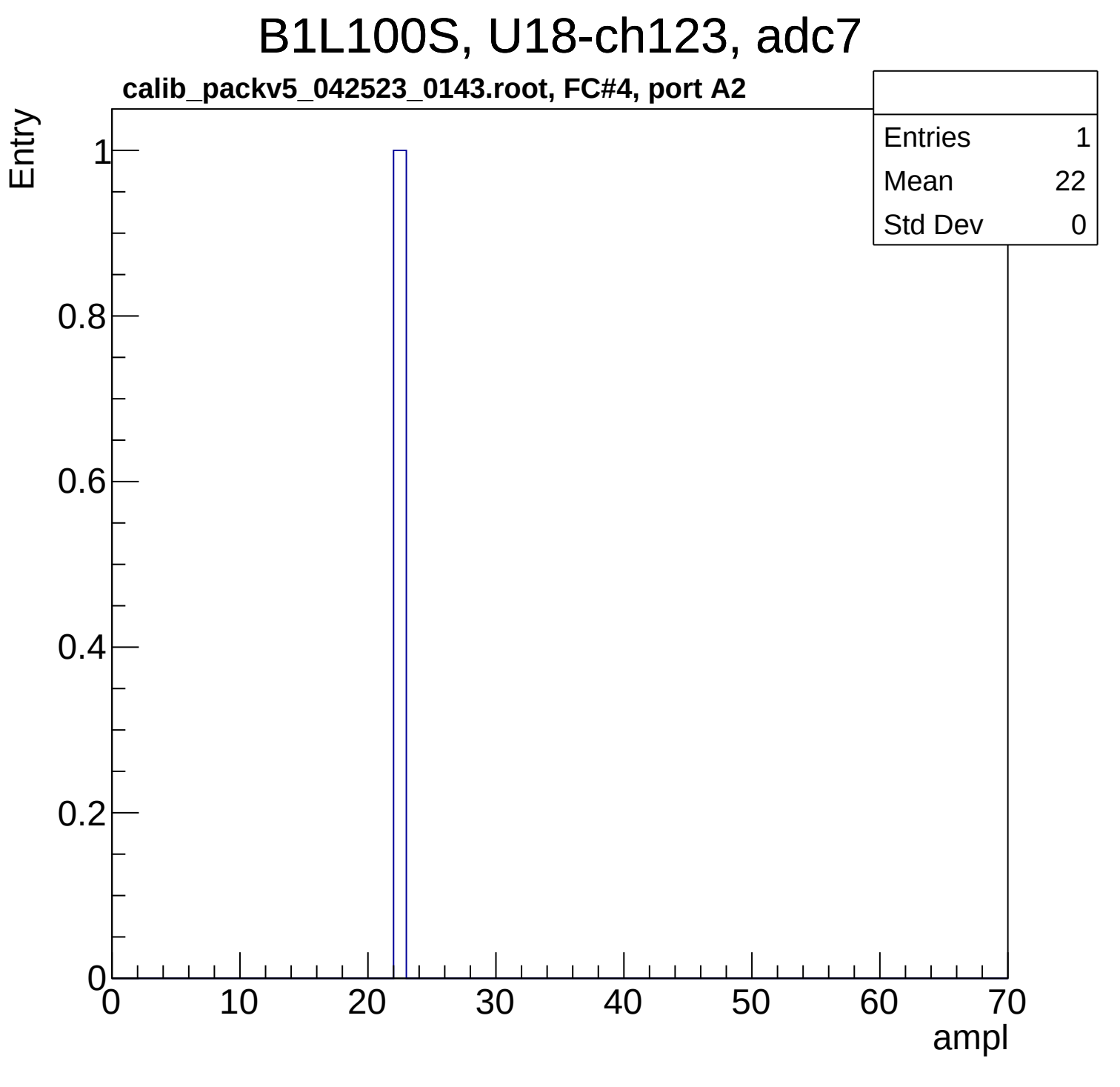

B1L100S, U18-ch123, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 70
Mean 43.73
Std Dev 3.802
Gaus mean : 44.0719
Gaus Width: 3.5439
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

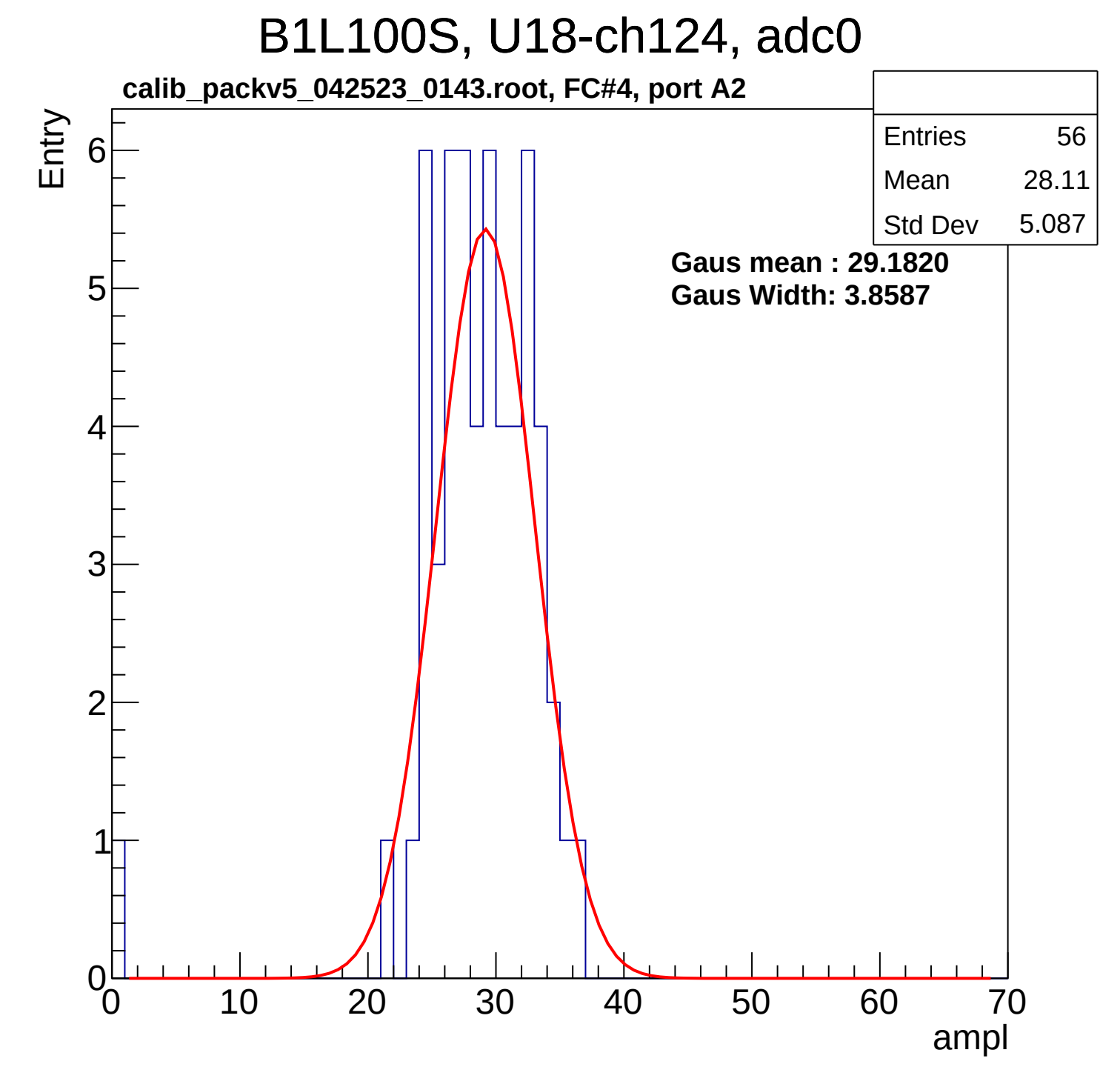

B1L100S, U18-ch123, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 50.11
Std Dev 3.305
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

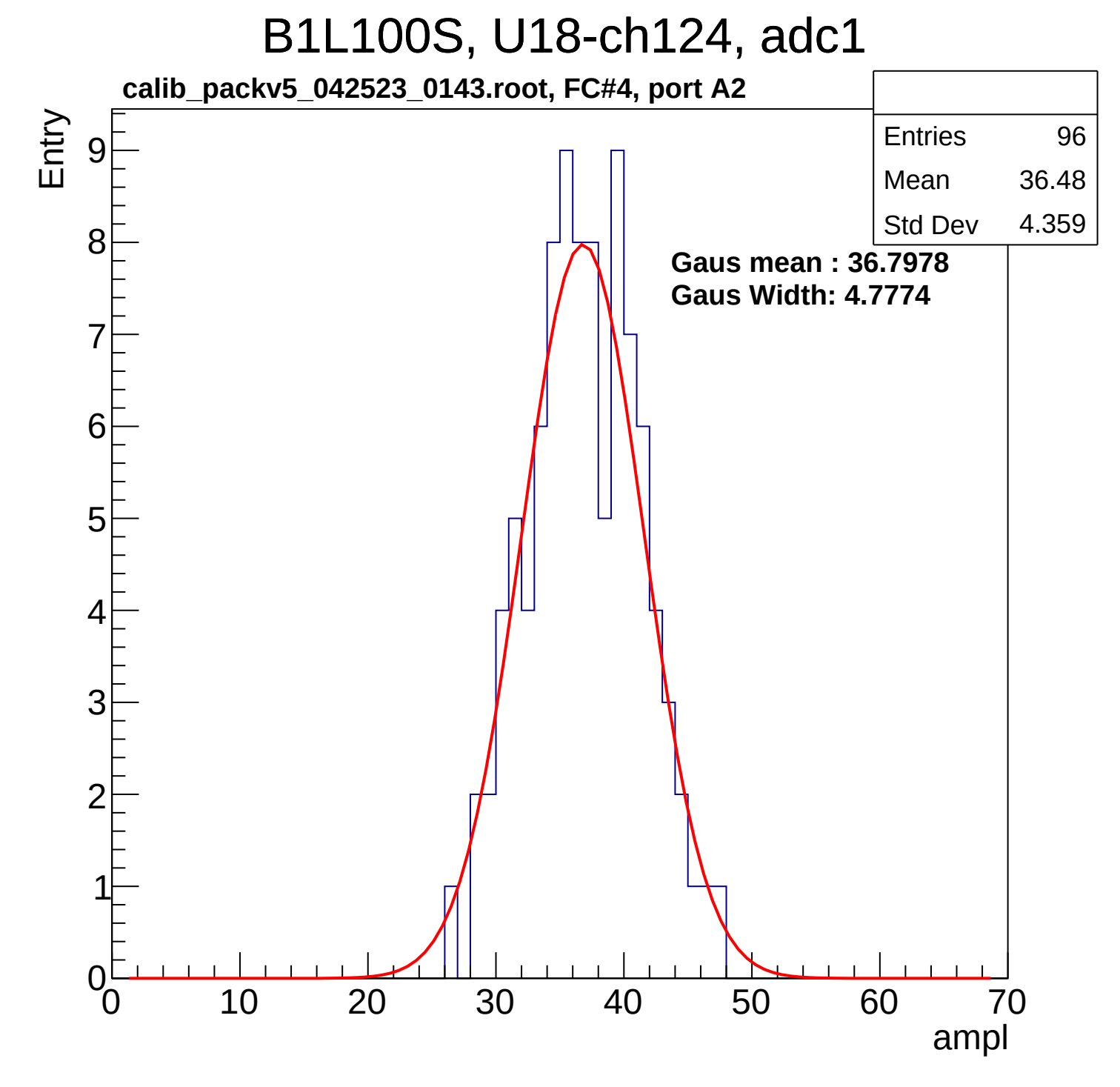

B1L100S, U18-ch123, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 53
Mean 55.62
Std Dev 3.158
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

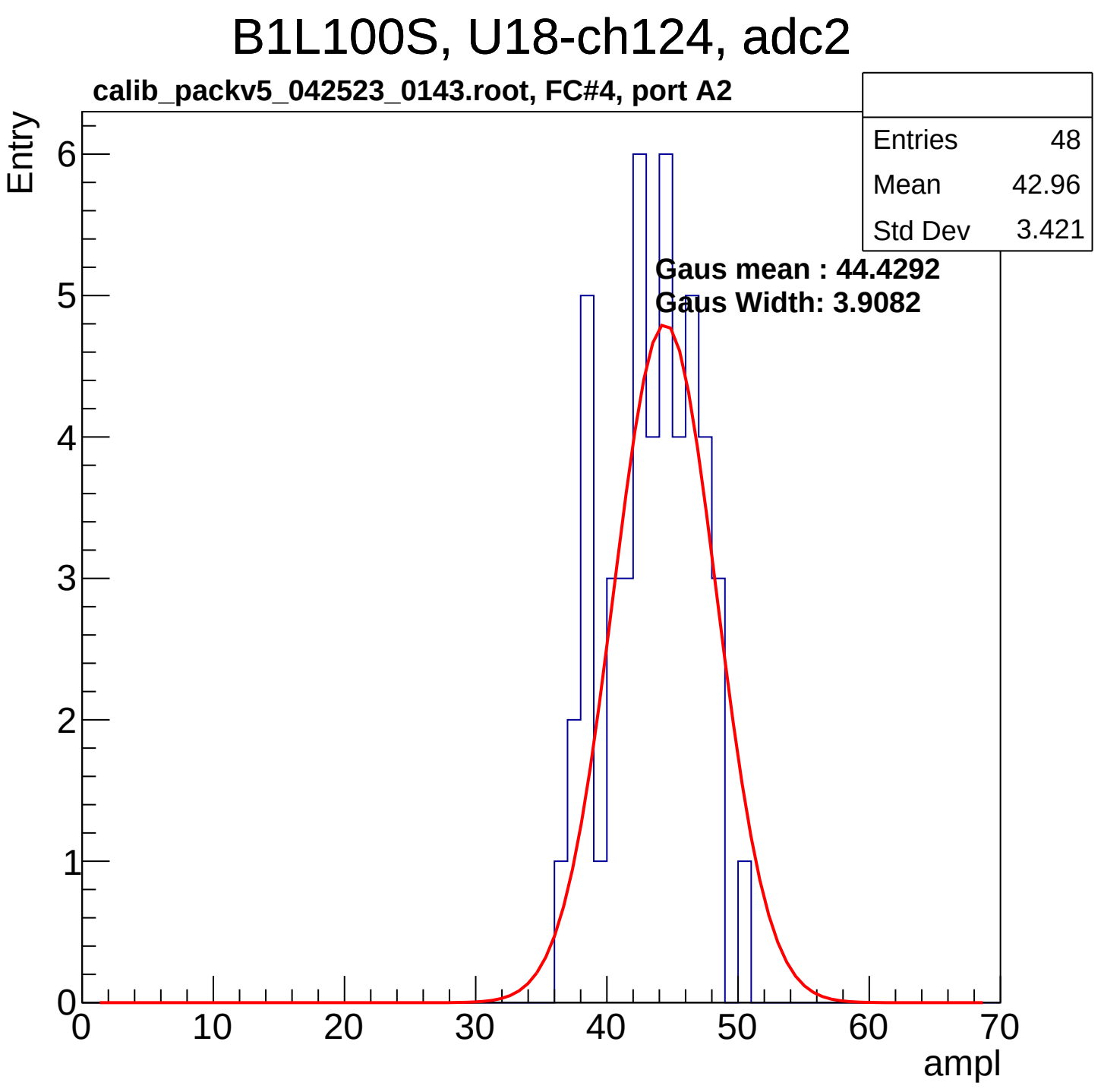

B1L100S, U18-ch123, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 44
Mean 58.89
Std Dev 9.22
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

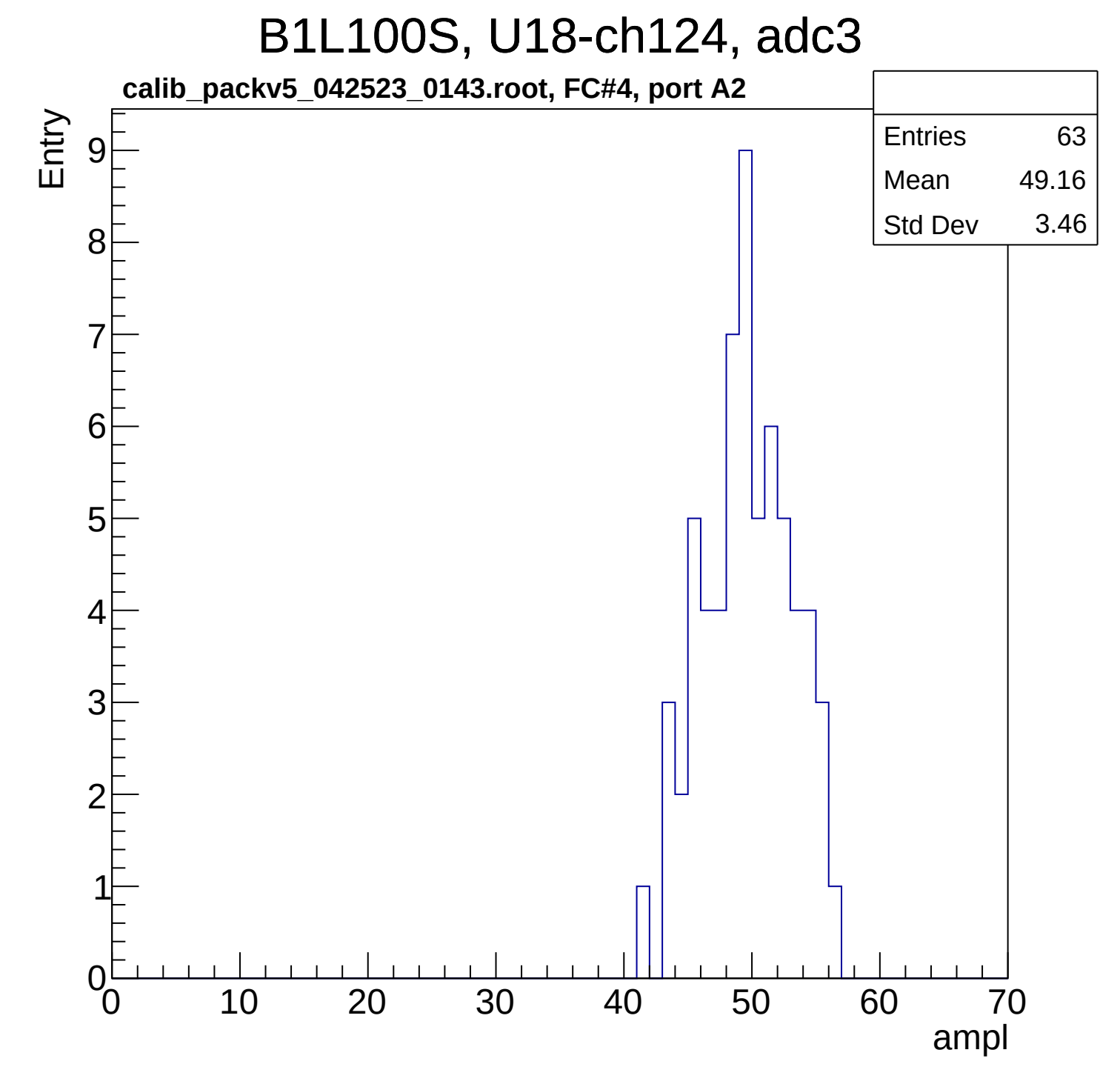

B1L100S, U18-ch123, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 61.83
Std Dev 1.067
Entry
ampl
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
10
20
30
40
50
60
70

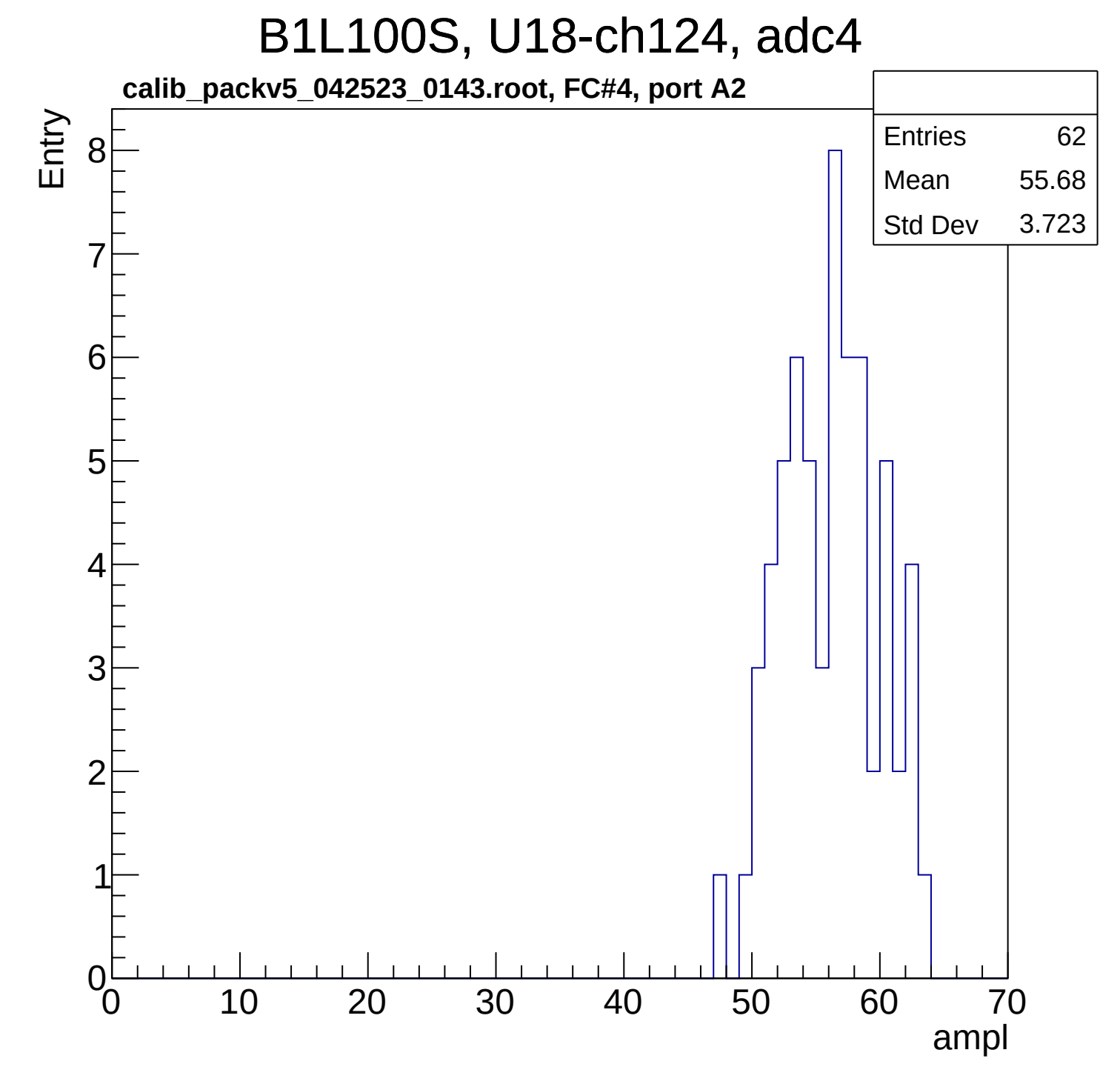

B1L100S, U18-ch123, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 22
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

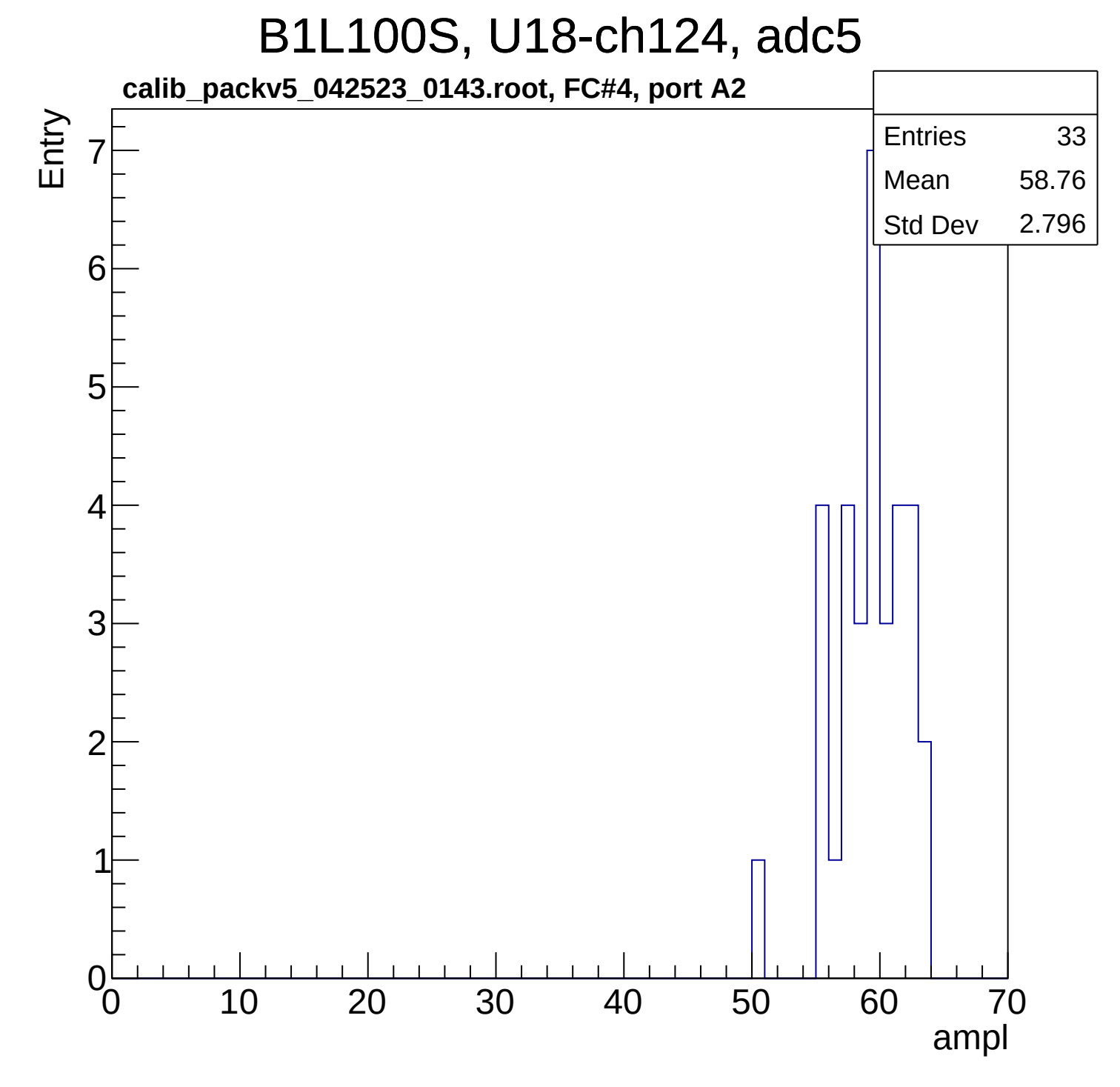

B1L100S, U18-ch124, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 56
Mean 28.11
Std Dev 5.087
Gaus mean : 29.1820
Gaus Width: 3.8587
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

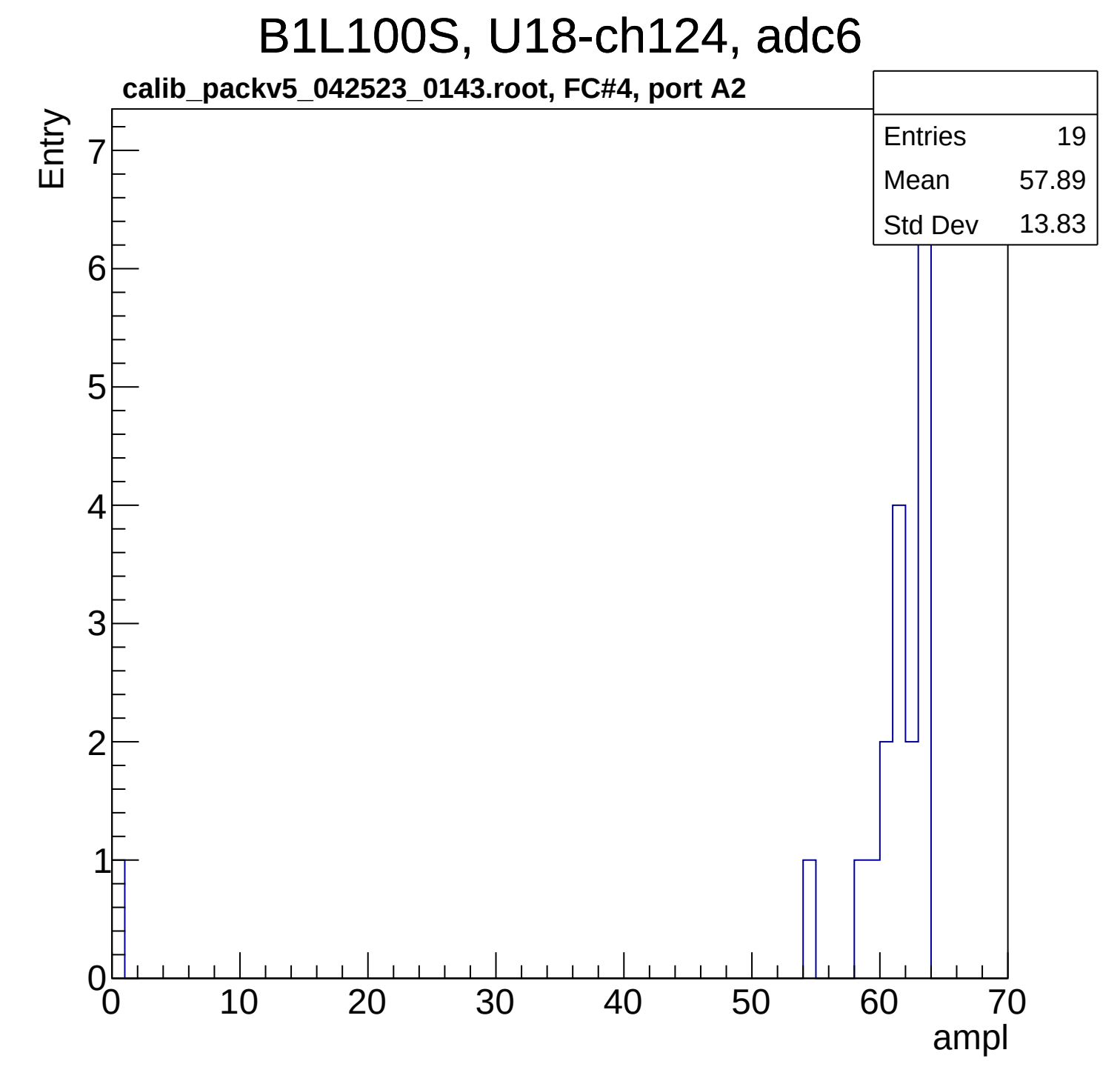

B1L100S, U18-ch124, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 96
Mean 36.48
Std Dev 4.359
Gaus mean : 36.7978
Gaus Width: 4.7774
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

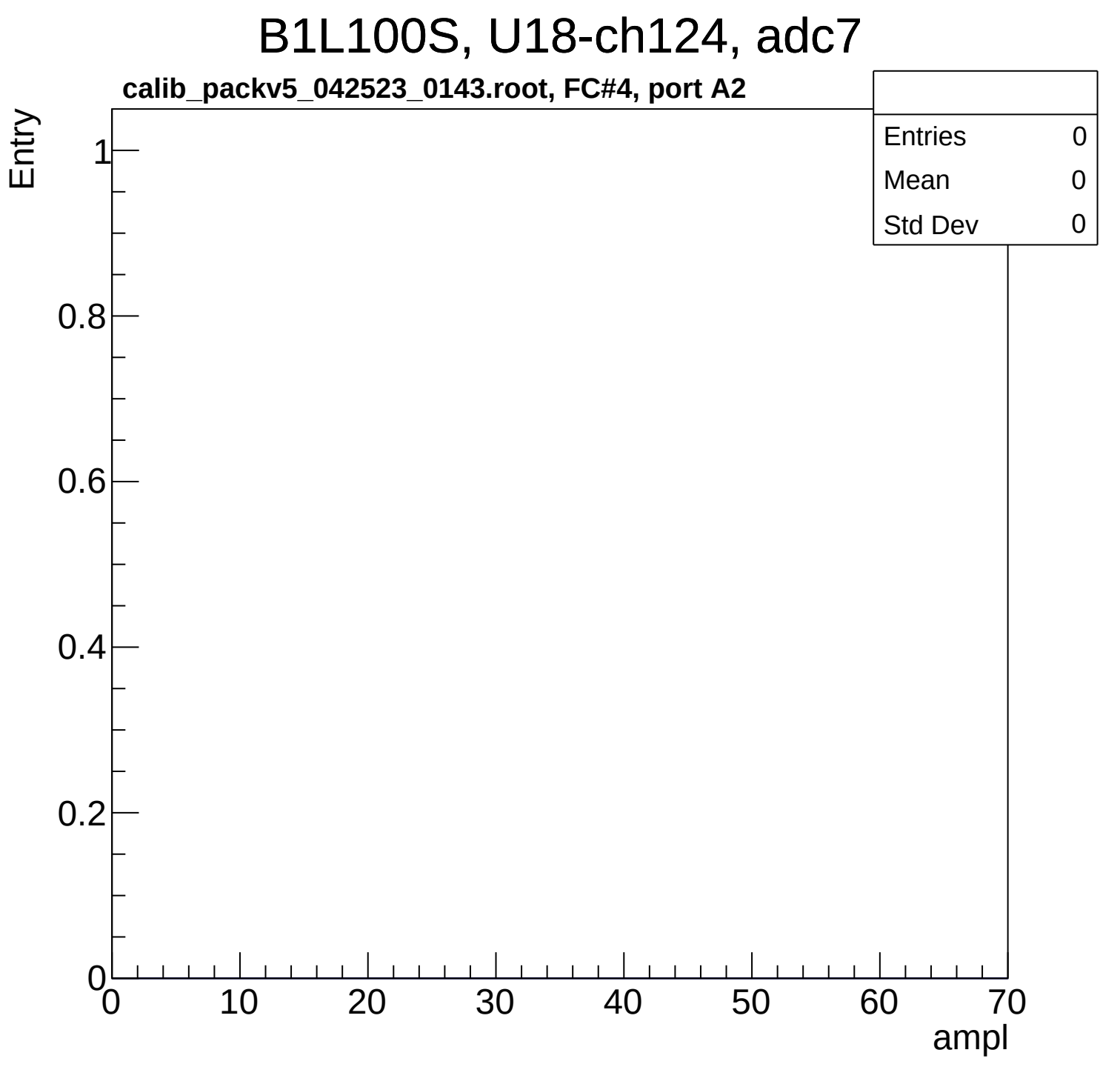

B1L100S, U18-ch124, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 48
Mean 42.96
Std Dev 3.421
Gaus mean : 44.4292
Gaus Width: 3.9082
Entry
ampl
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70

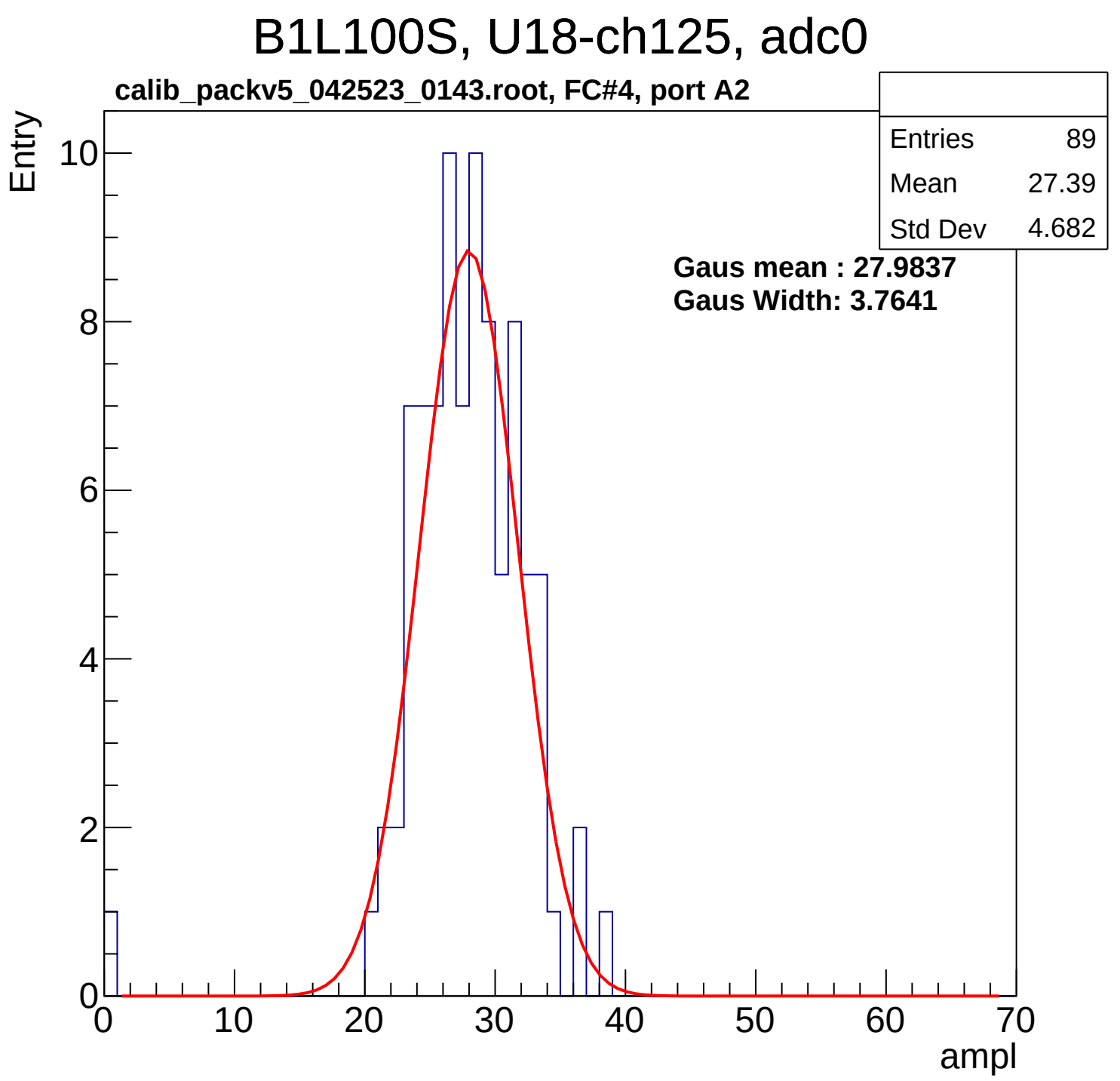

B1L100S, U18-ch124, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 49.16
Std Dev 3.46
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

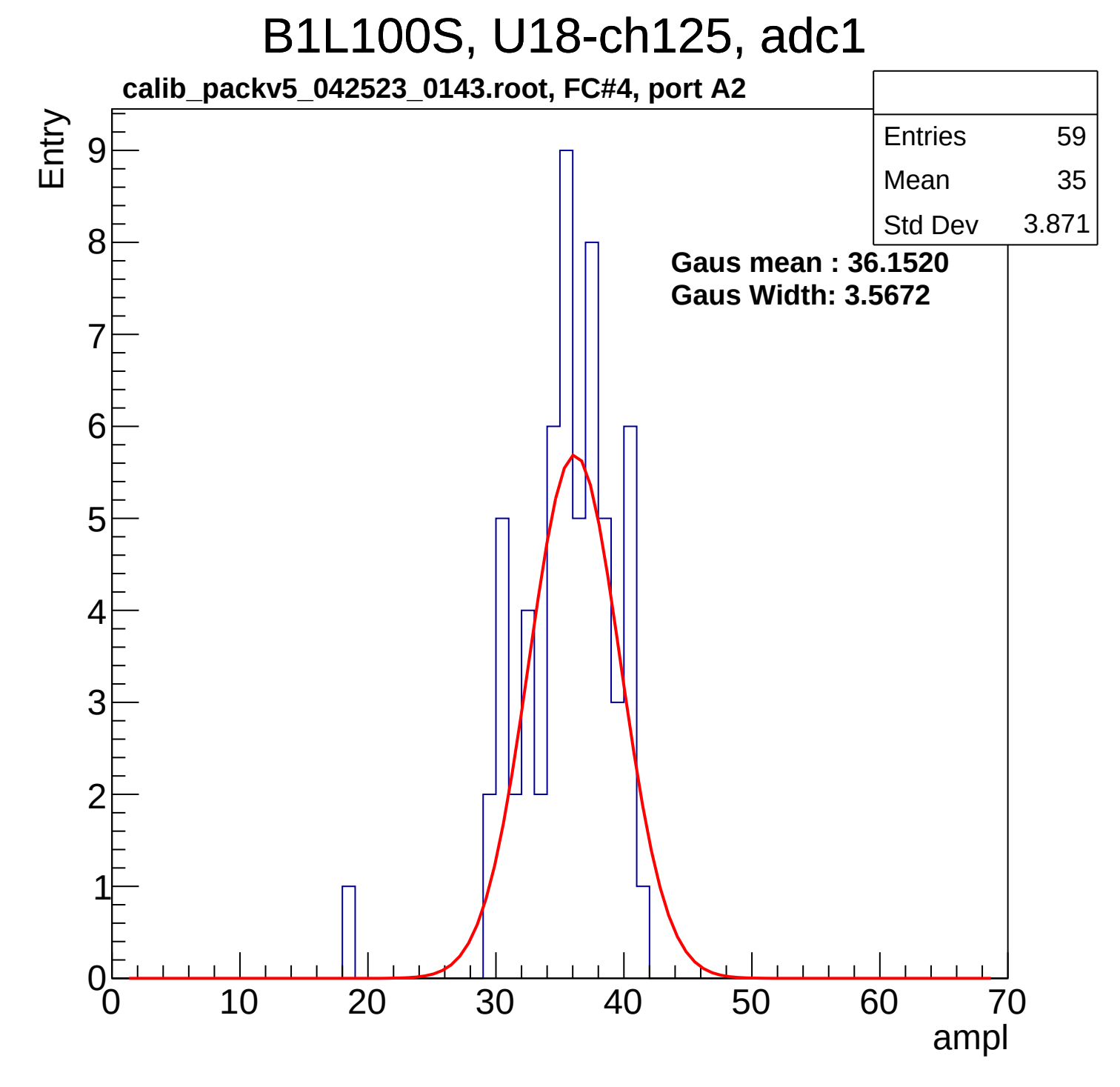

B1L100S, U18-ch124, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 55.68
Std Dev 3.723
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

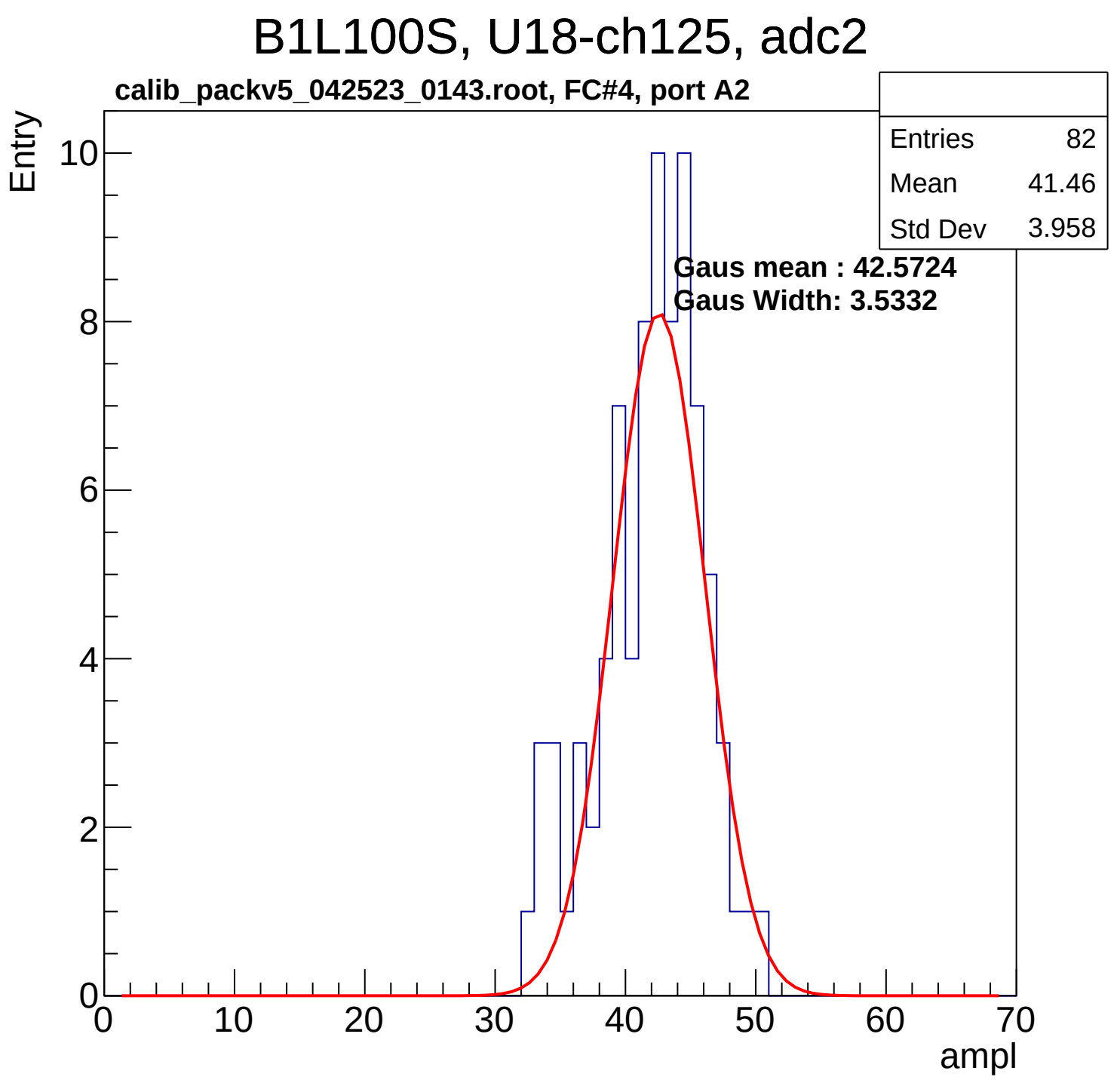

B1L100S, U18-ch124, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 33
Mean 58.76
Std Dev 2.796
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

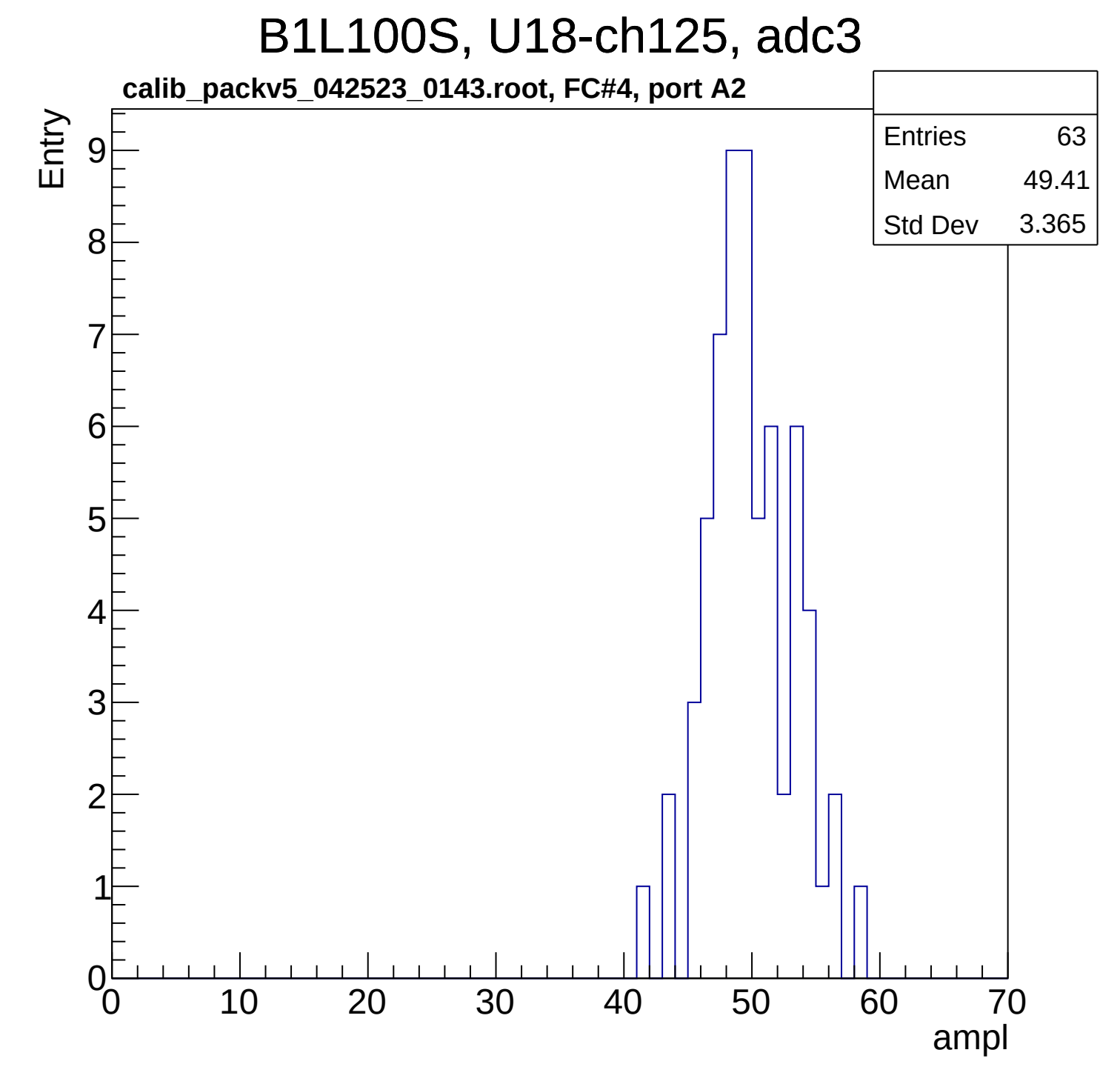

B1L100S, U18-ch124, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 19
Mean 57.89
Std Dev 13.83
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

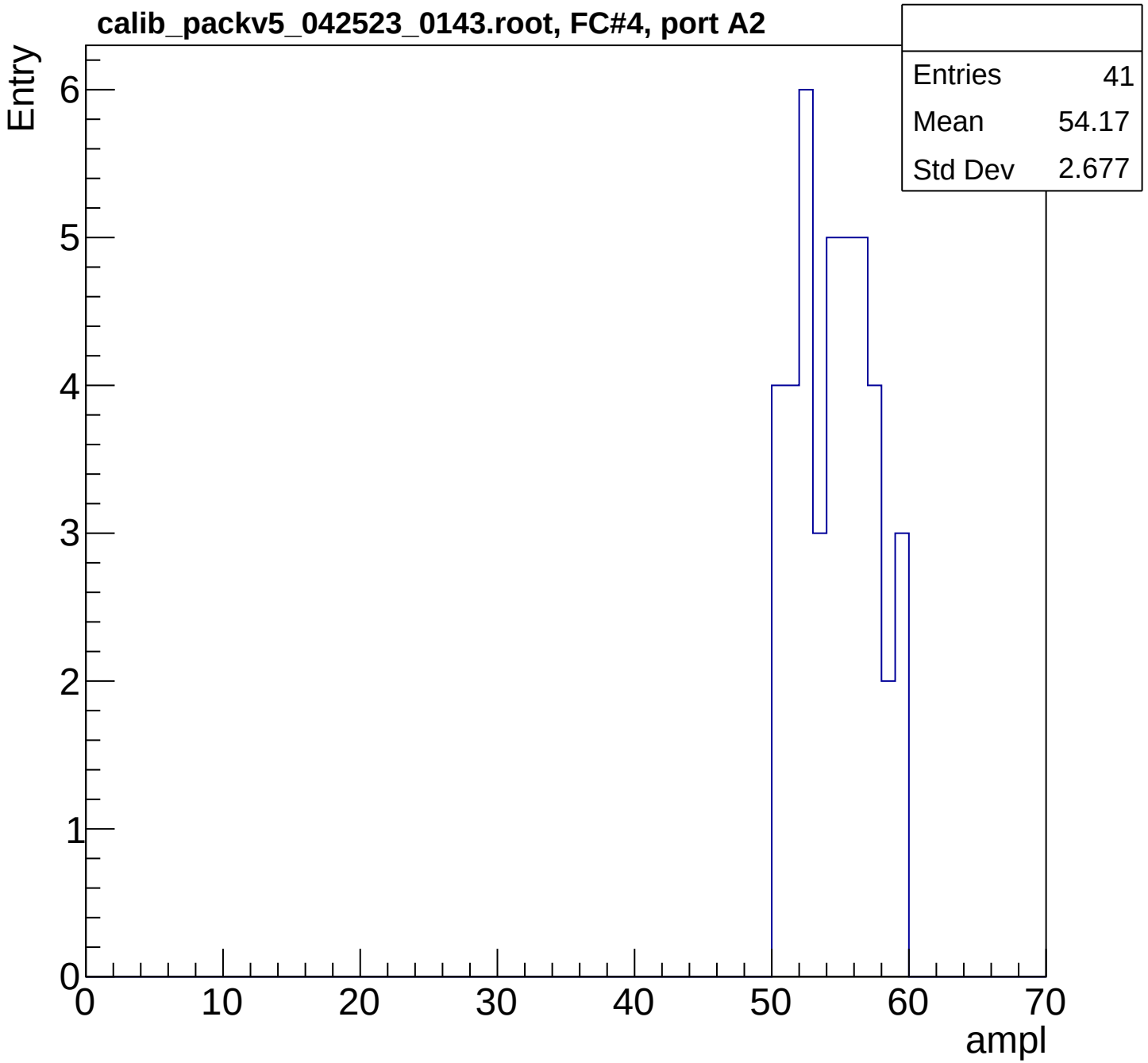

B1L100S, U18-ch124, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 0
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

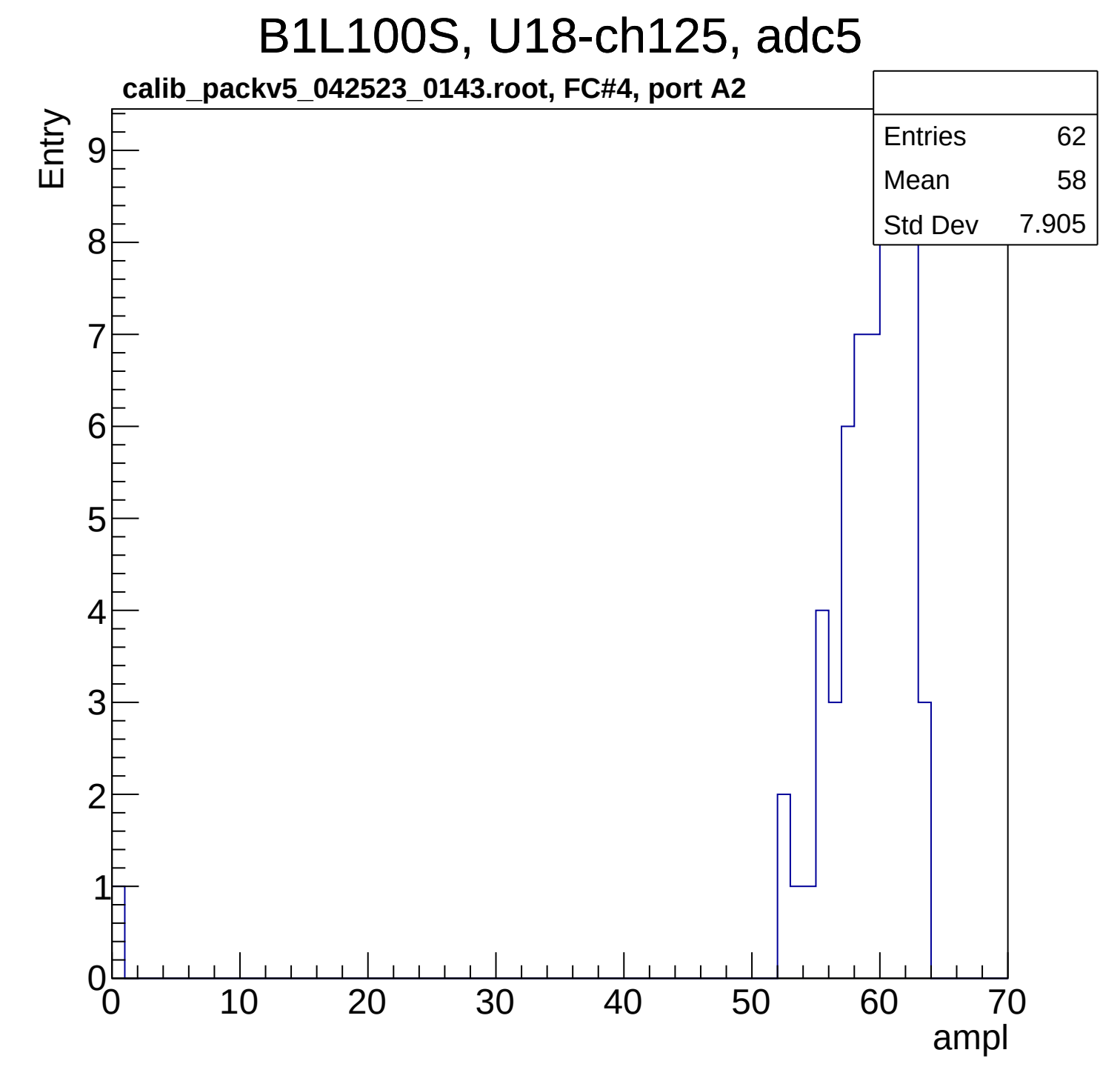

B1L100S, U18-ch125, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 89
Mean 27.39
Std Dev 4.682
Gaus mean : 27.9837
Gaus Width: 3.7641
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

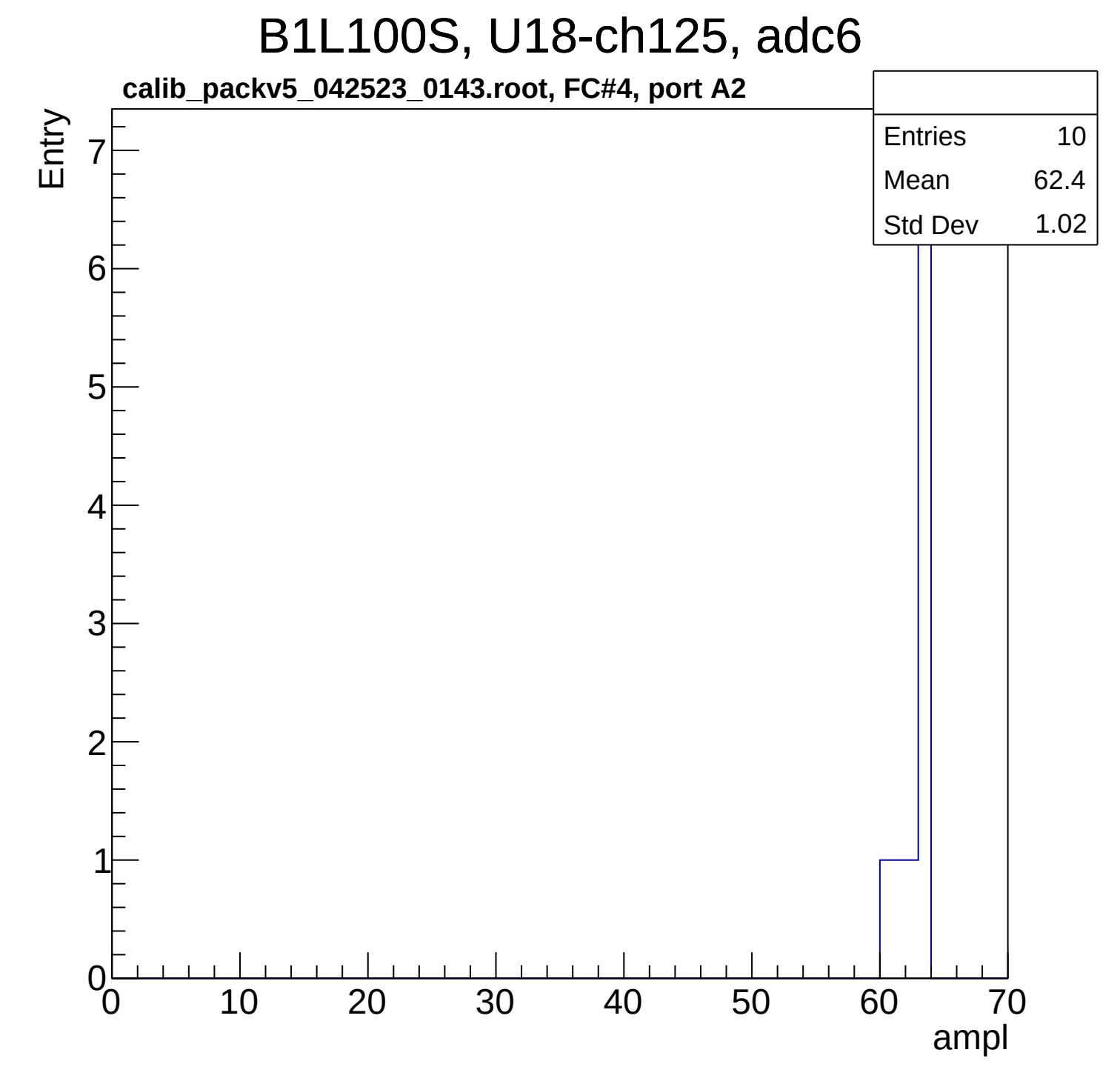

B1L100S, U18-ch125, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 59
Mean 35
Std Dev 3.871
Gaus mean : 36.1520
Gaus Width: 3.5672
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

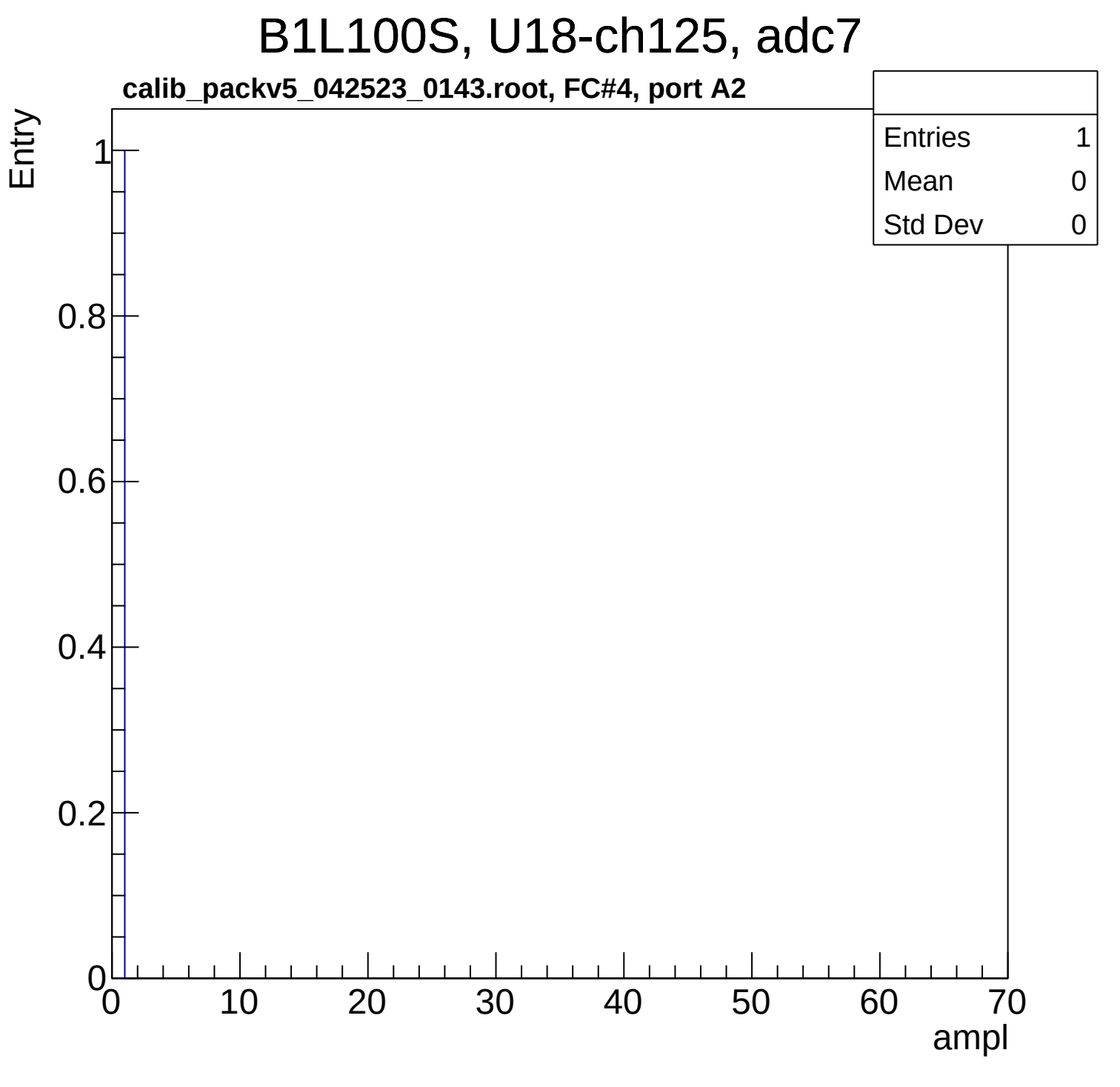

B1L100S, U18-ch125, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 41.46
Std Dev 3.958
Gaus mean : 42.5724
Gaus Width: 3.5332
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

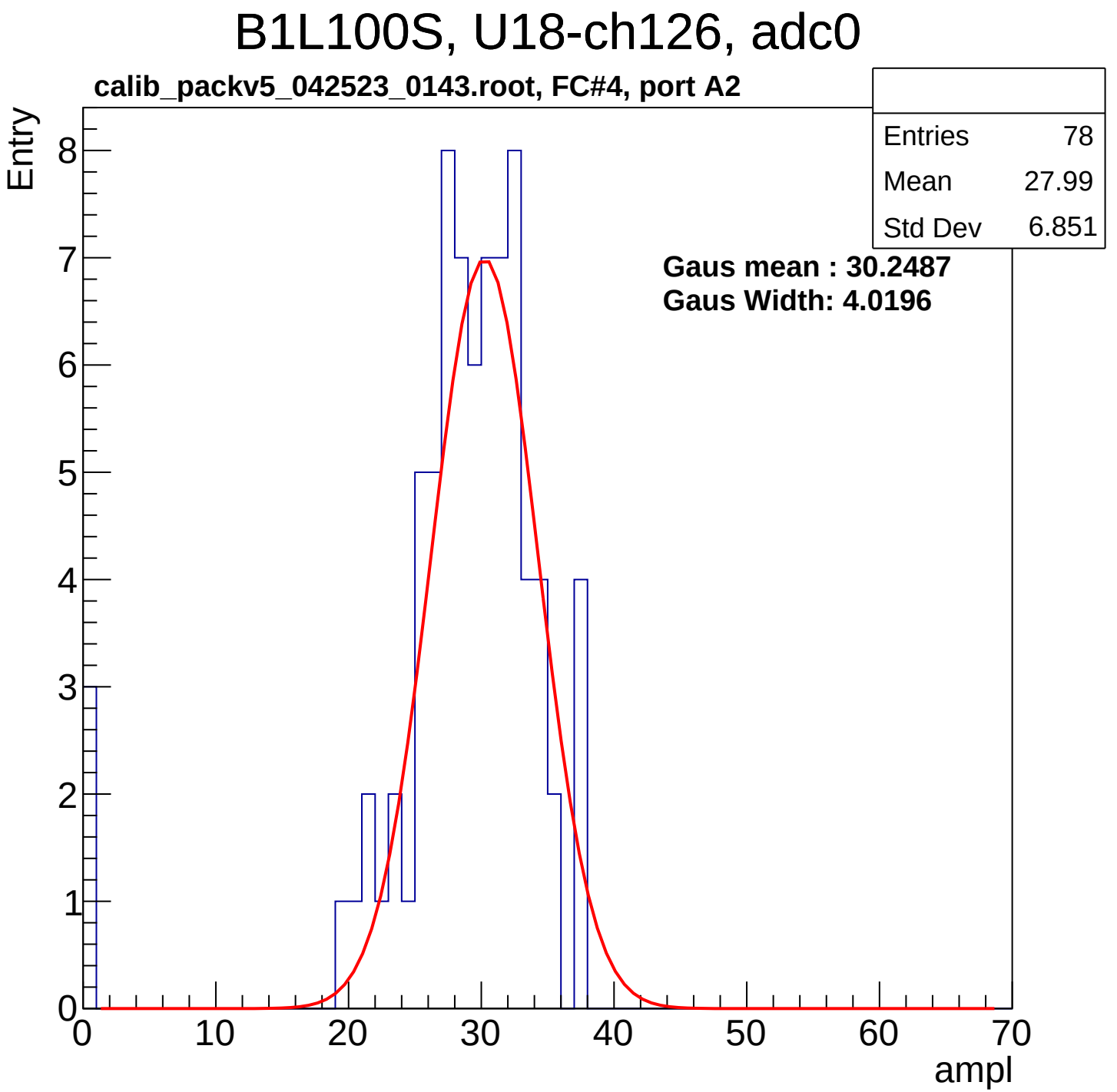

B1L100S, U18-ch125, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 49.41
Std Dev 3.365
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

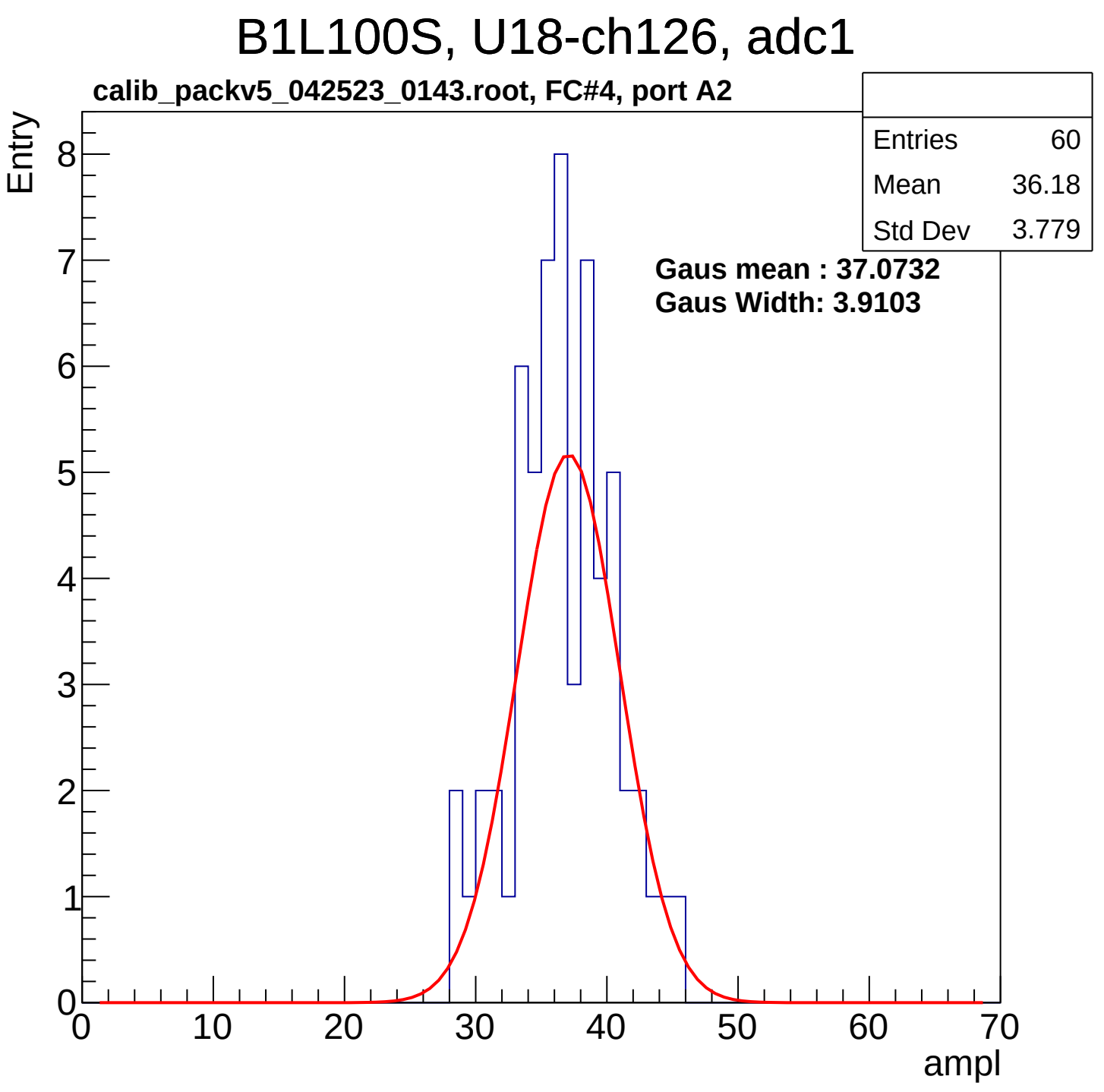

B1L100S, U18-ch125, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 41
Mean 54.17
Std Dev 2.677
Entry
0
1
2
3
4
5
6
0
10
20
30
40
50
60
70
ampl

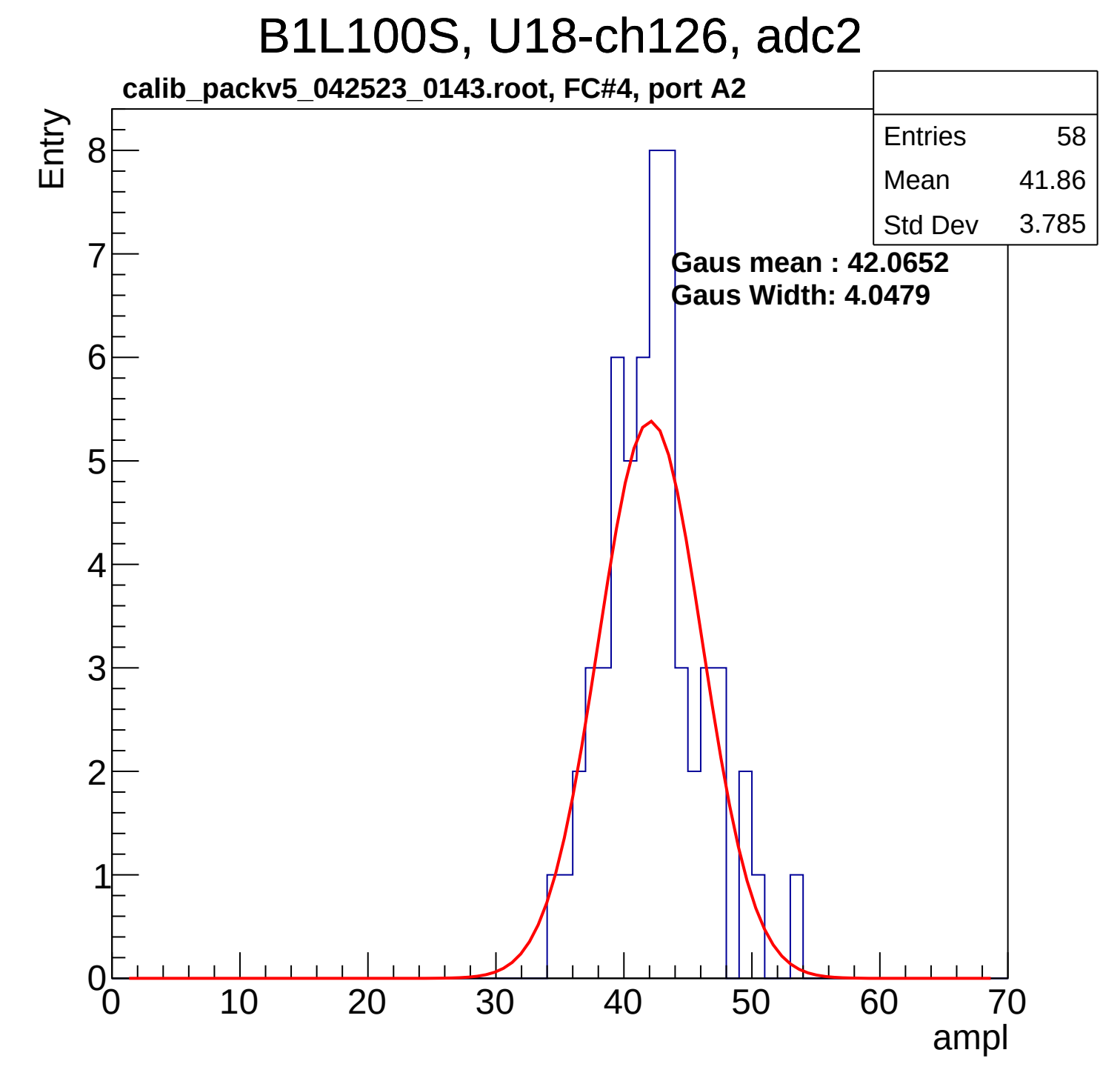

B1L100S, U18-ch125, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 62
Mean 58
Std Dev 7.905
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

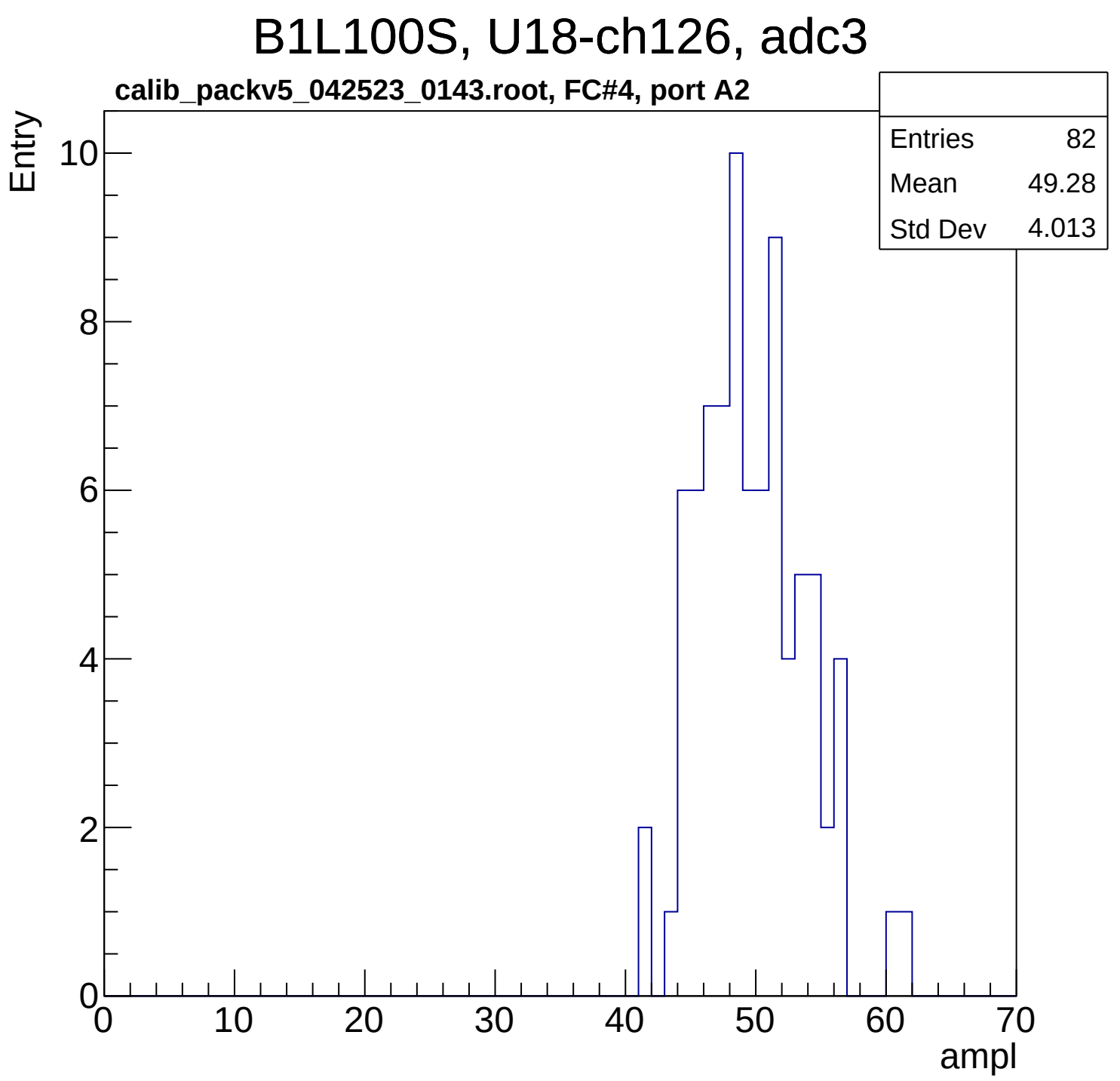

B1L100S, U18-ch125, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 62.4
Std Dev 1.02
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70

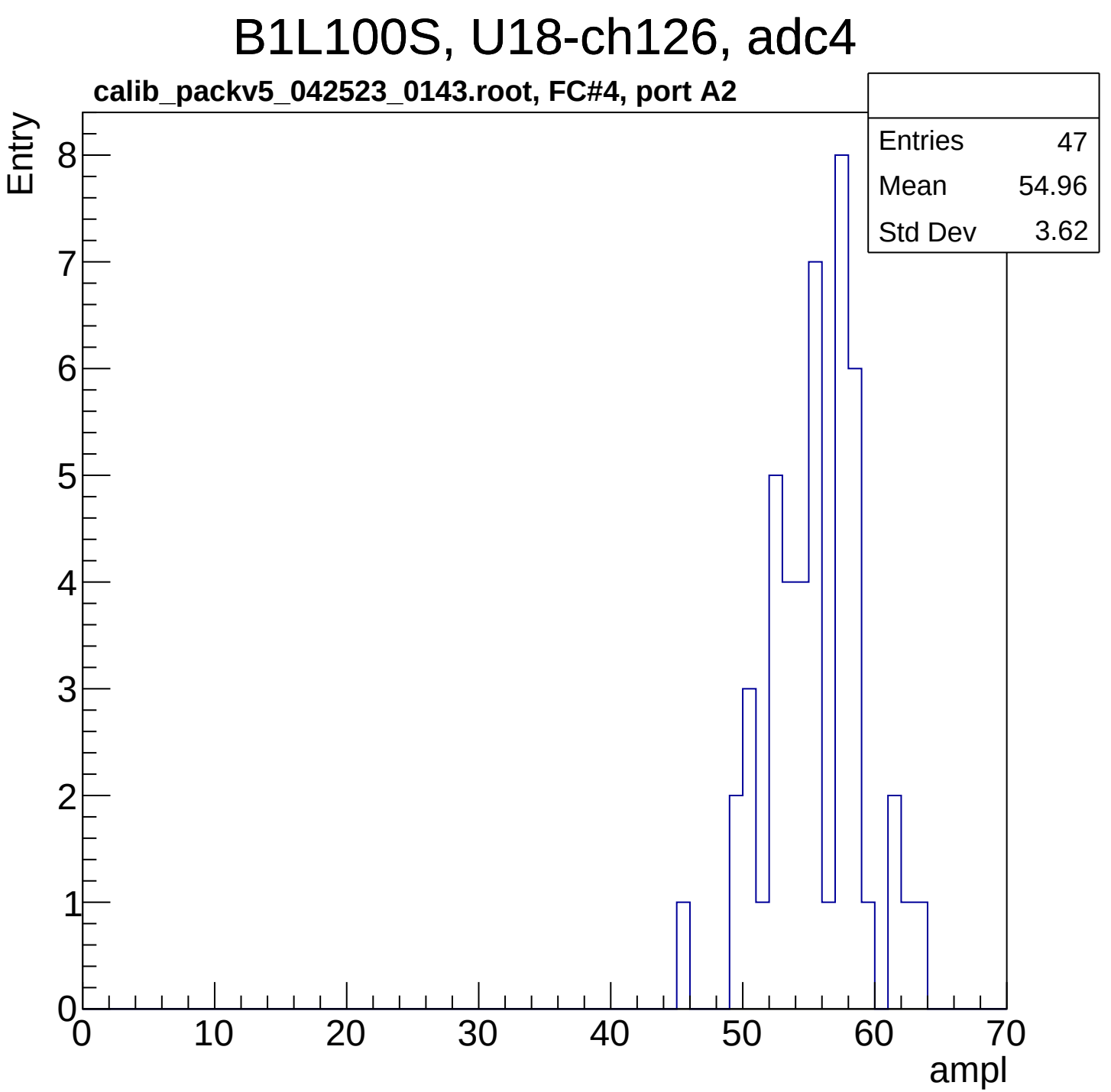

B1L100S, U18-ch125, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 0
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

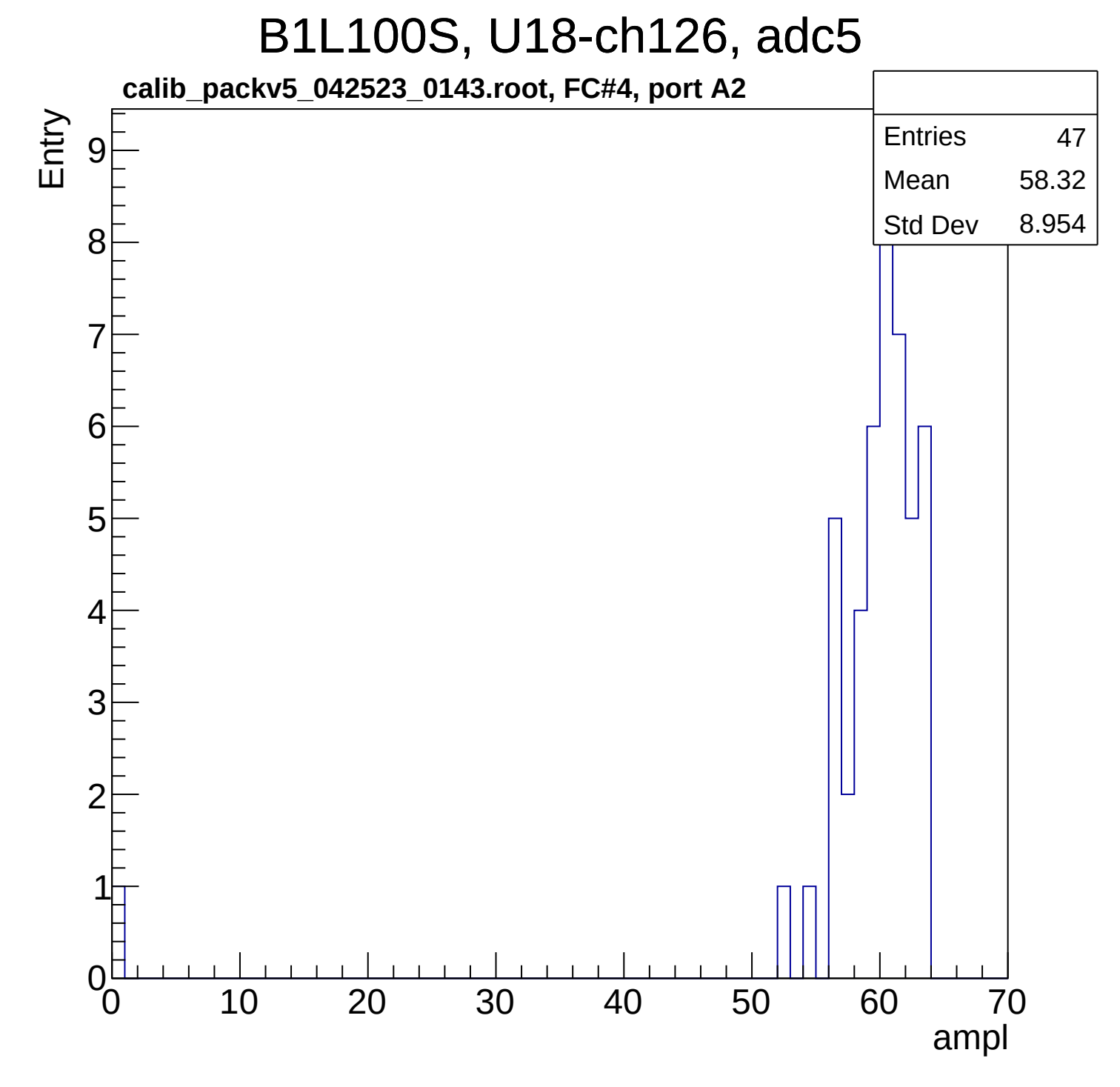

B1L100S, U18-ch126, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 78
Mean 27.99
Std Dev 6.851
Gaus mean : 30.2487
Gaus Width: 4.0196
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

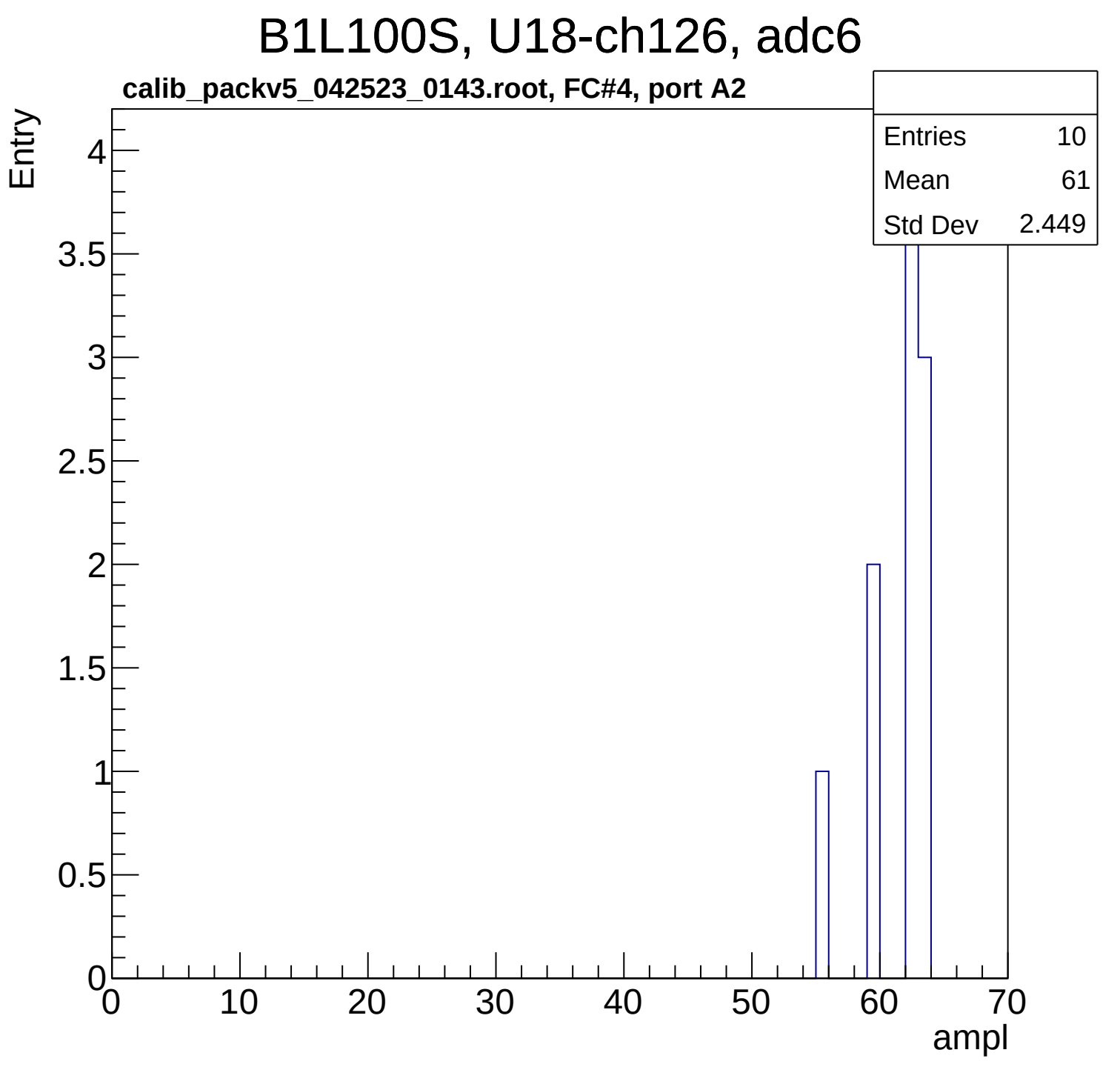

B1L100S, U18-ch126, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 60
Mean 36.18
Std Dev 3.779
Gaus mean : 37.0732
Gaus Width: 3.9103
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

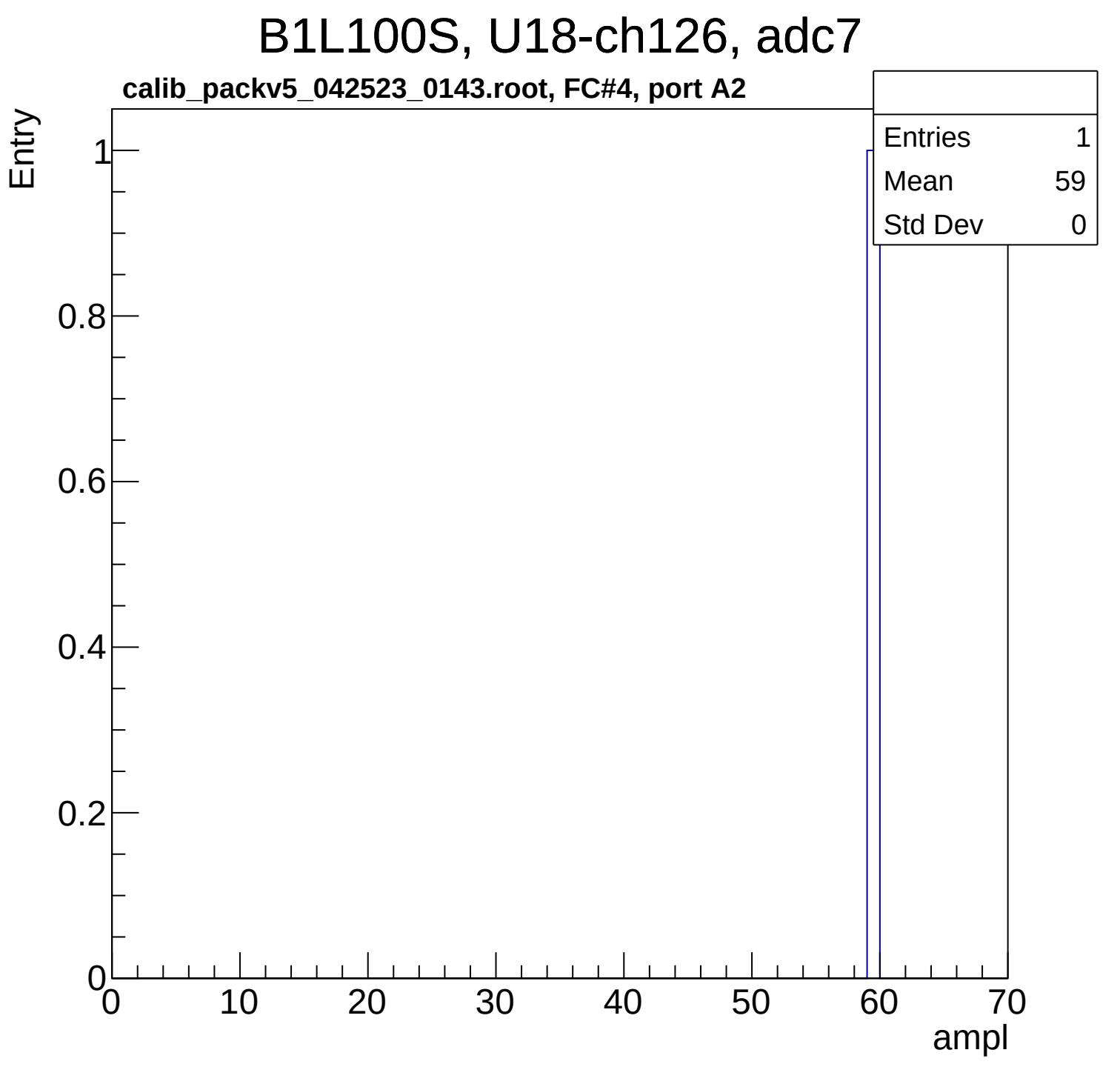

B1L100S, U18-ch126, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 58
Mean 41.86
Std Dev 3.785
Gaus mean : 42.0652
Gaus Width: 4.0479
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

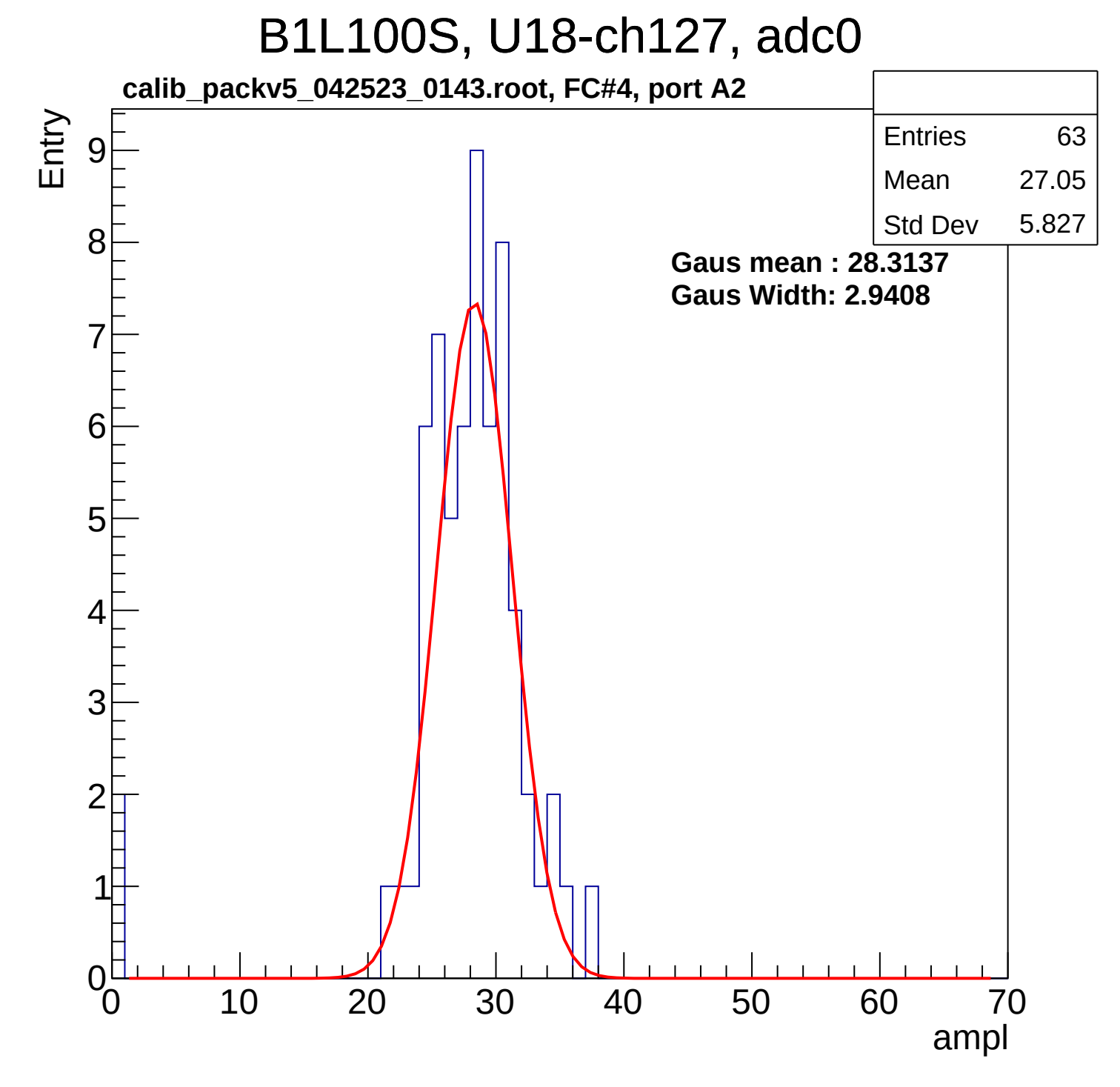

B1L100S, U18-ch126, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 49.28
Std Dev 4.013
Entry
ampl
0
2
4
6
8
10
0
10
20
30
40
50
60
70

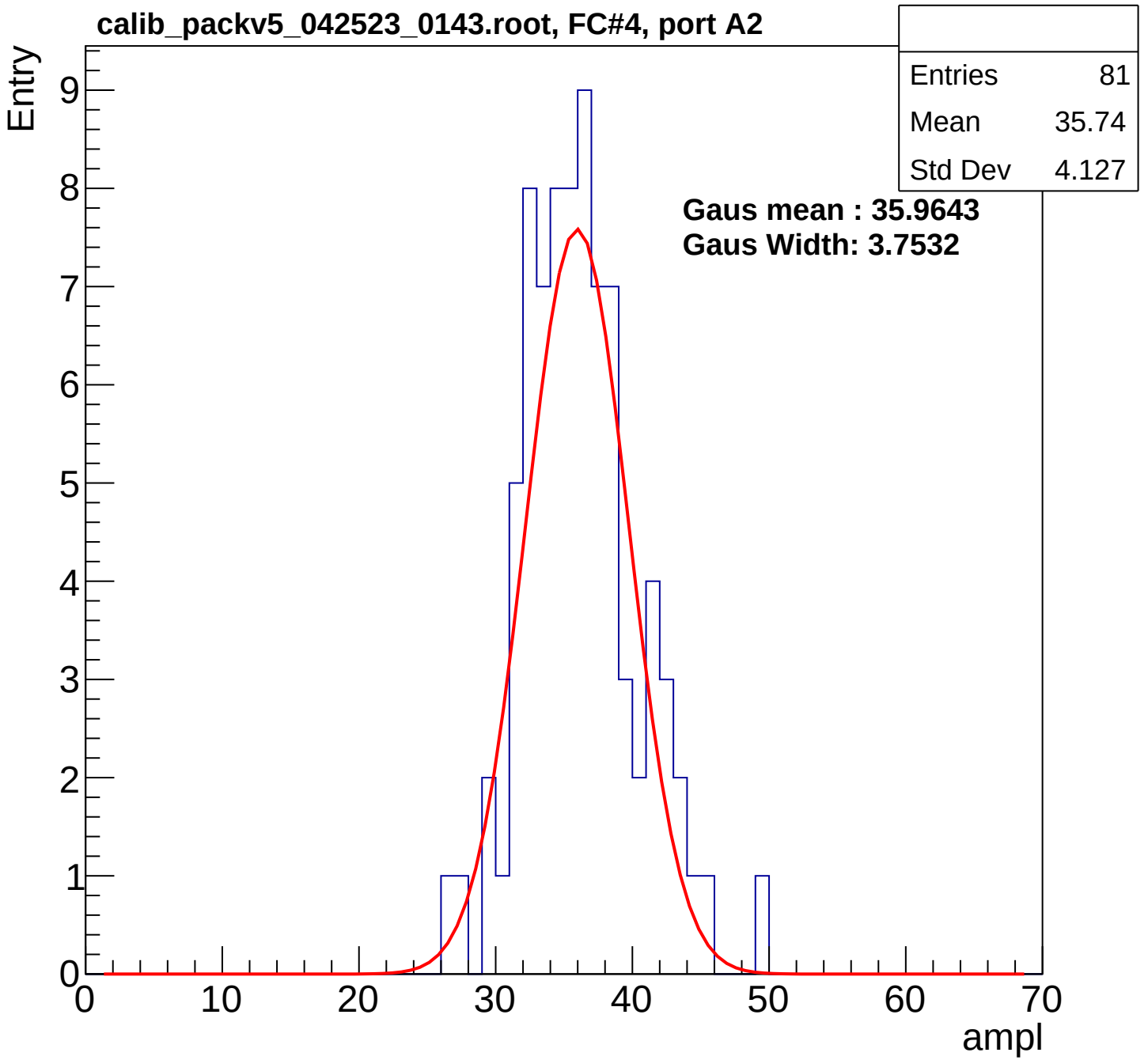

B1L100S, U18-ch126, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 54.96
Std Dev 3.62
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

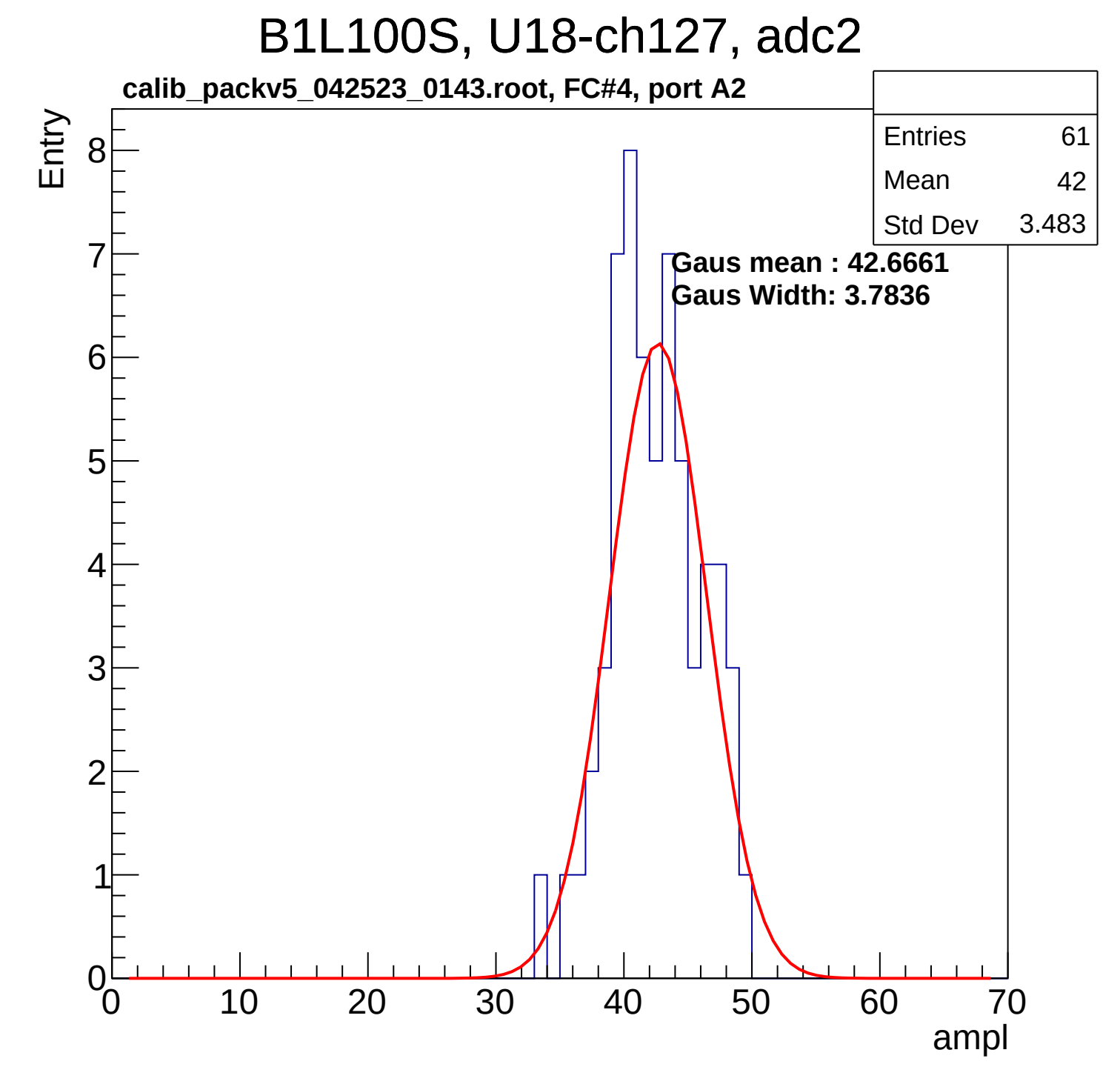

B1L100S, U18-ch126, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 47
Mean 58.32
Std Dev 8.954
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

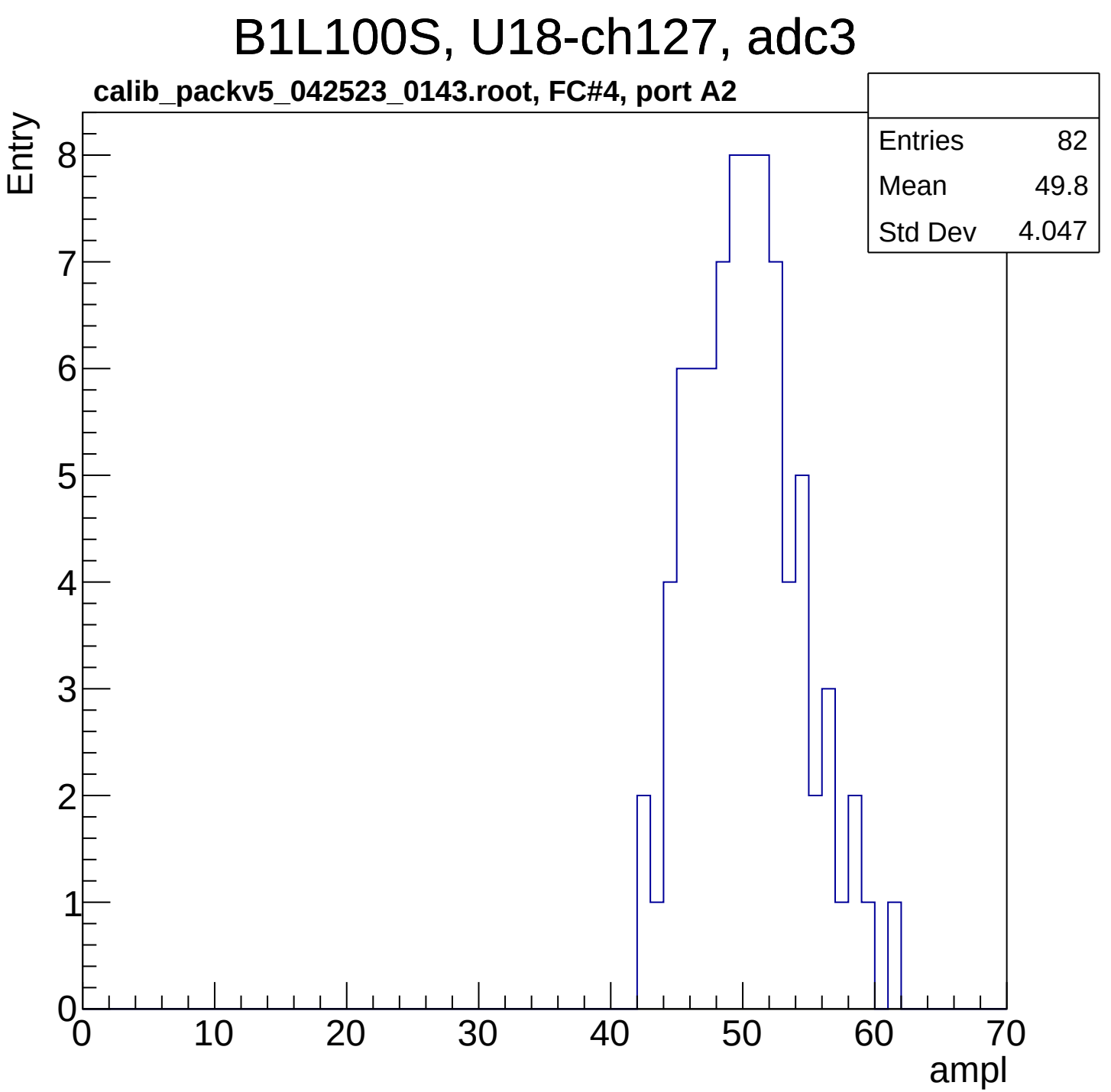

B1L100S, U18-ch126, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 10
Mean 61
Std Dev 2.449
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70

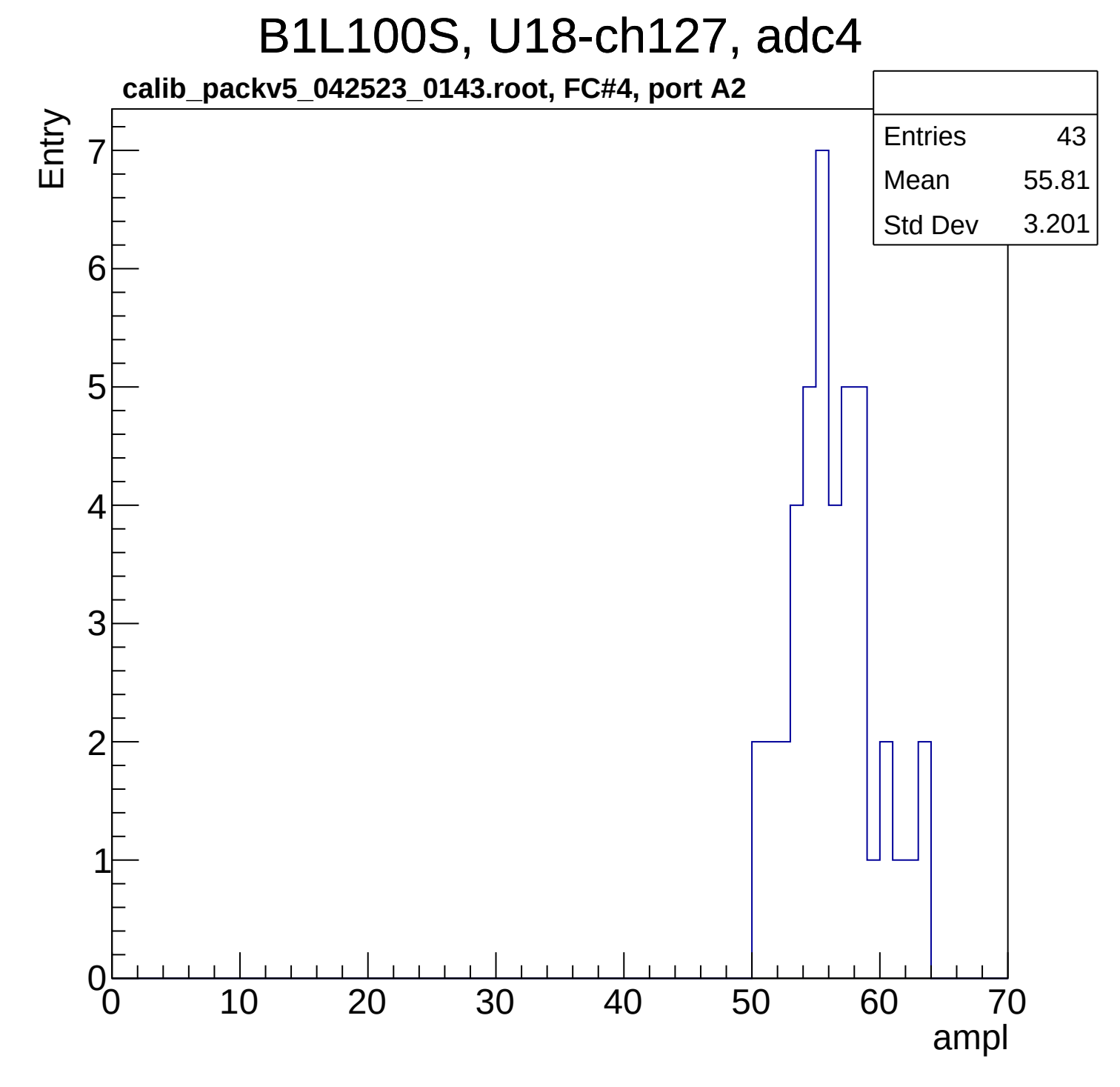

B1L100S, U18-ch126, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 59
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl

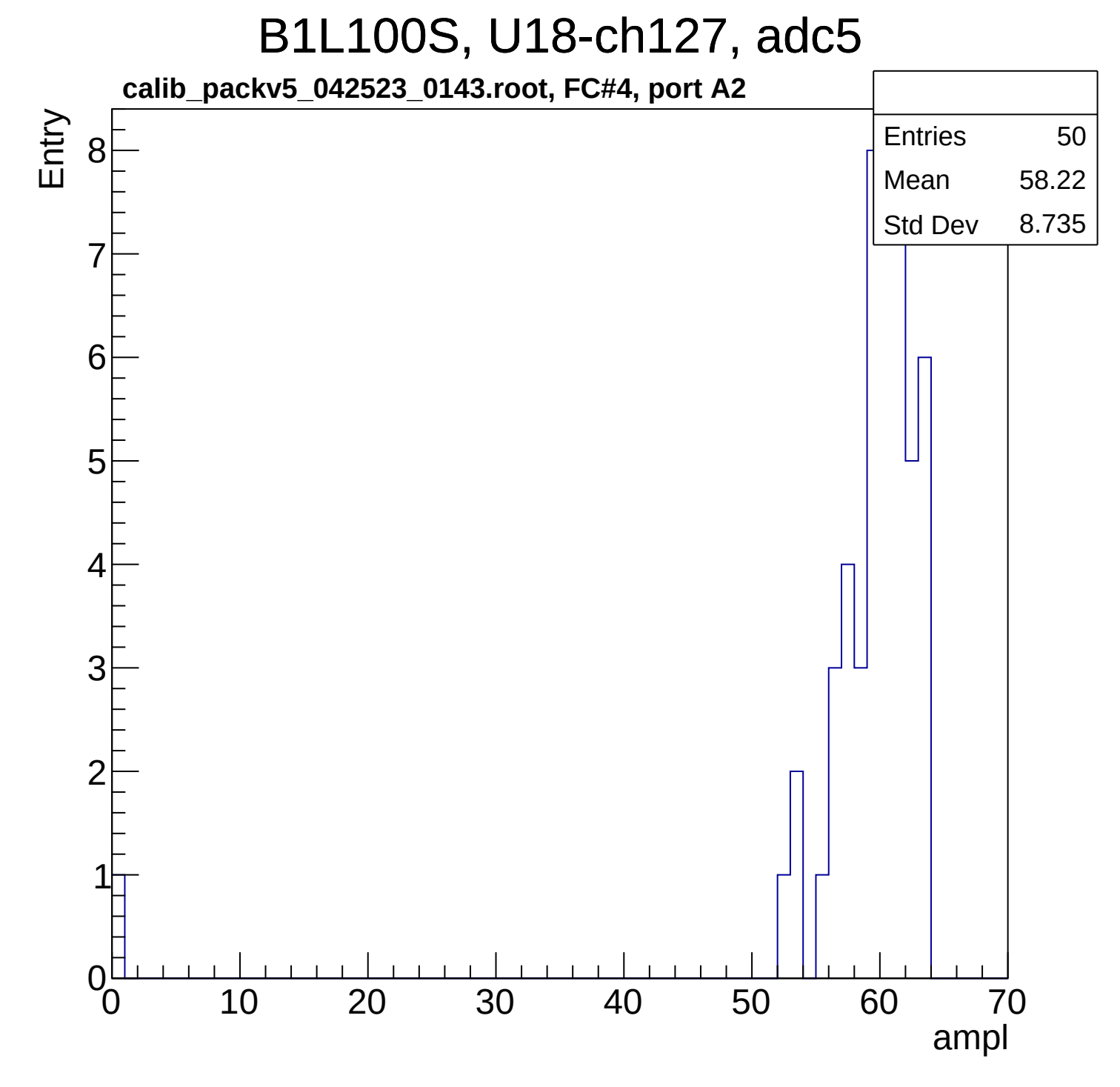

B1L100S, U18-ch127, adc0
calib_packv5_042523_0143.root, FC#4, port A2
Entries 63
Mean 27.05
Std Dev 5.827
Gaus mean : 28.3137
Gaus Width: 2.9408
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

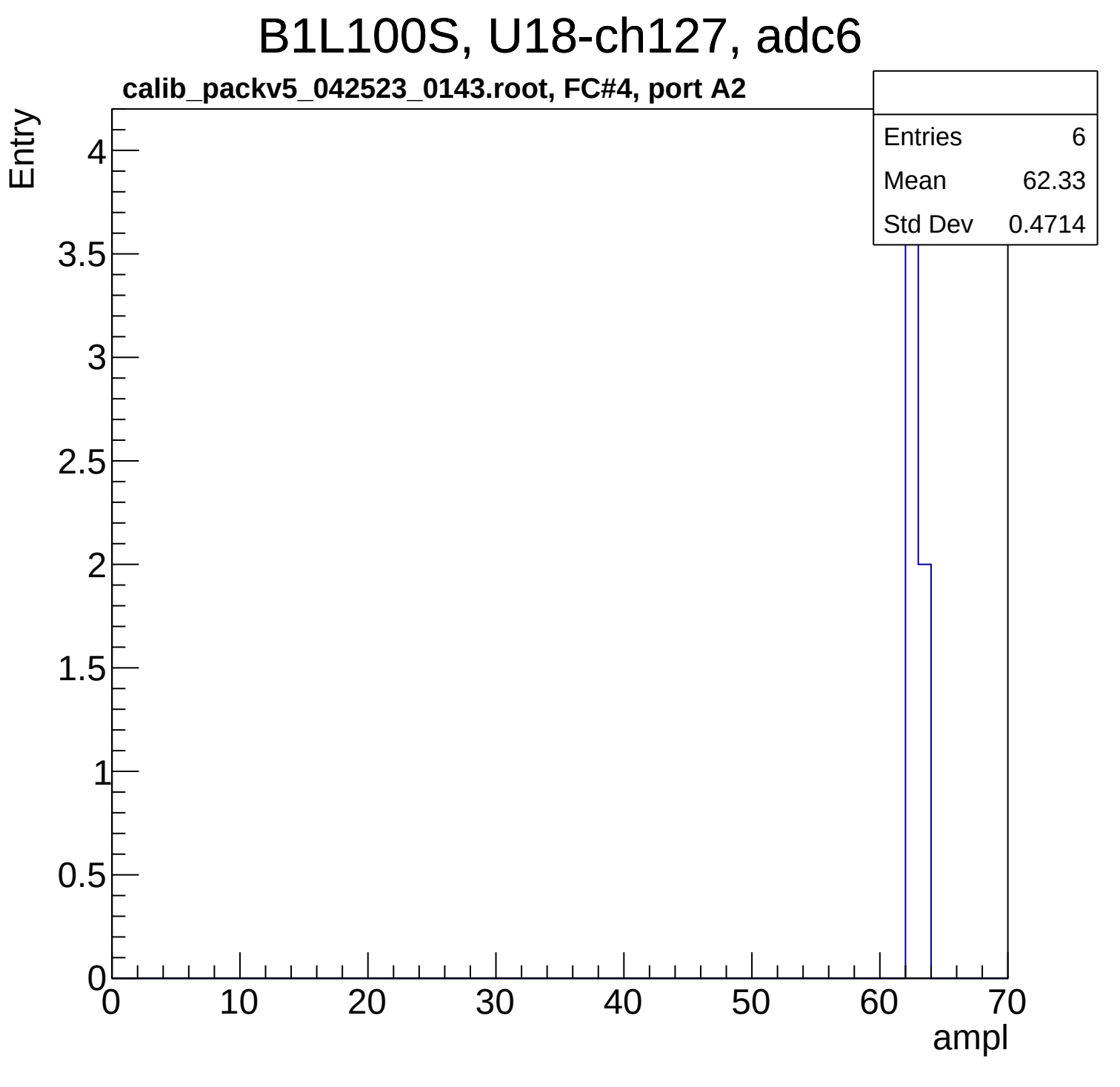

B1L100S, U18-ch127, adc1
calib_packv5_042523_0143.root, FC#4, port A2
Entries 81
Mean 35.74
Std Dev 4.127
Gaus mean : 35.9643
Gaus Width: 3.7532
Entry
ampl
0
1
2
3
4
5
6
7
8
9
0
10
20
30
40
50
60
70

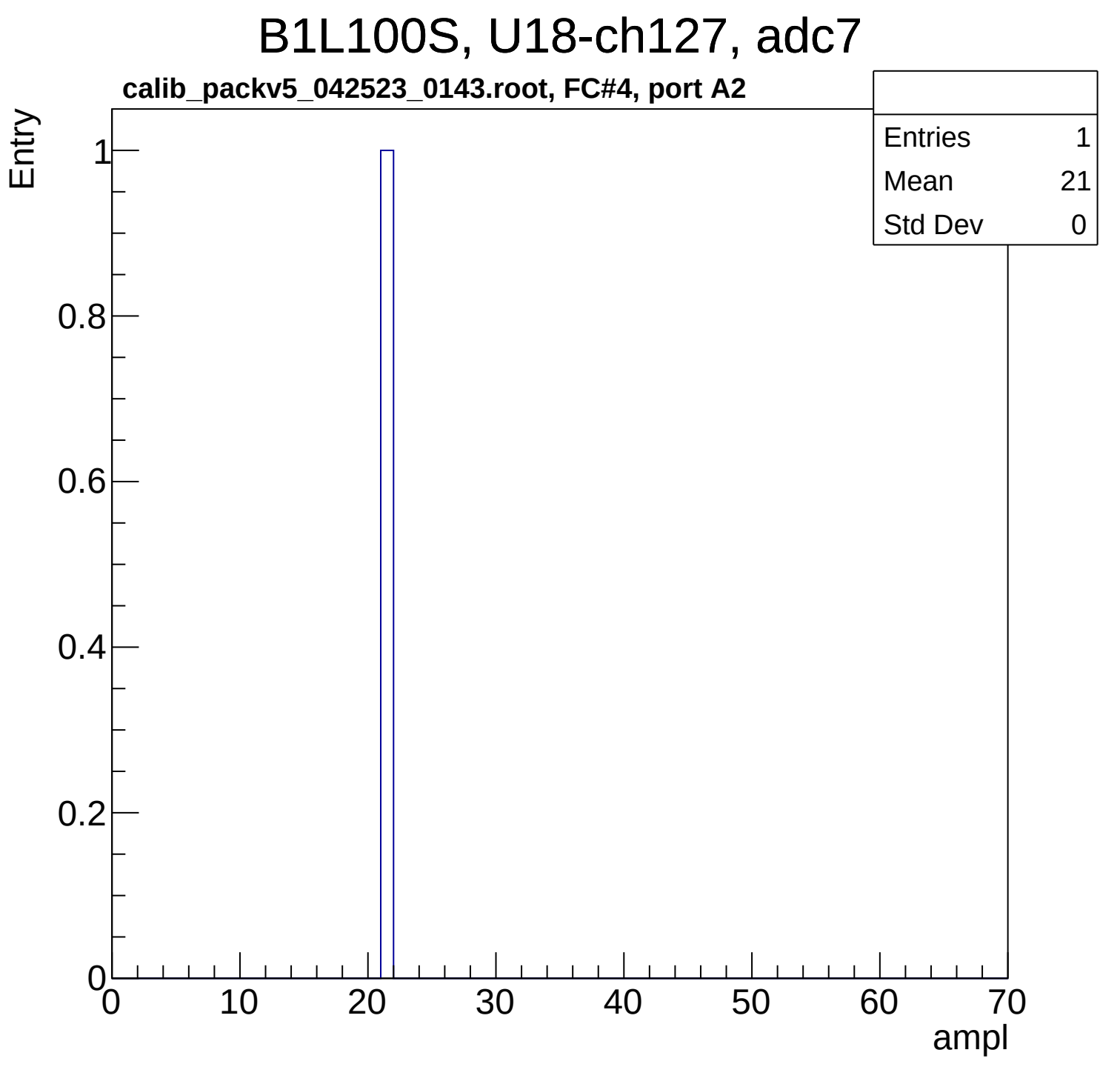

B1L100S, U18-ch127, adc2
calib_packv5_042523_0143.root, FC#4, port A2
Entries 61
Mean 42
Std Dev 3.483
Gaus mean : 42.6661
Gaus Width: 3.7836
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70

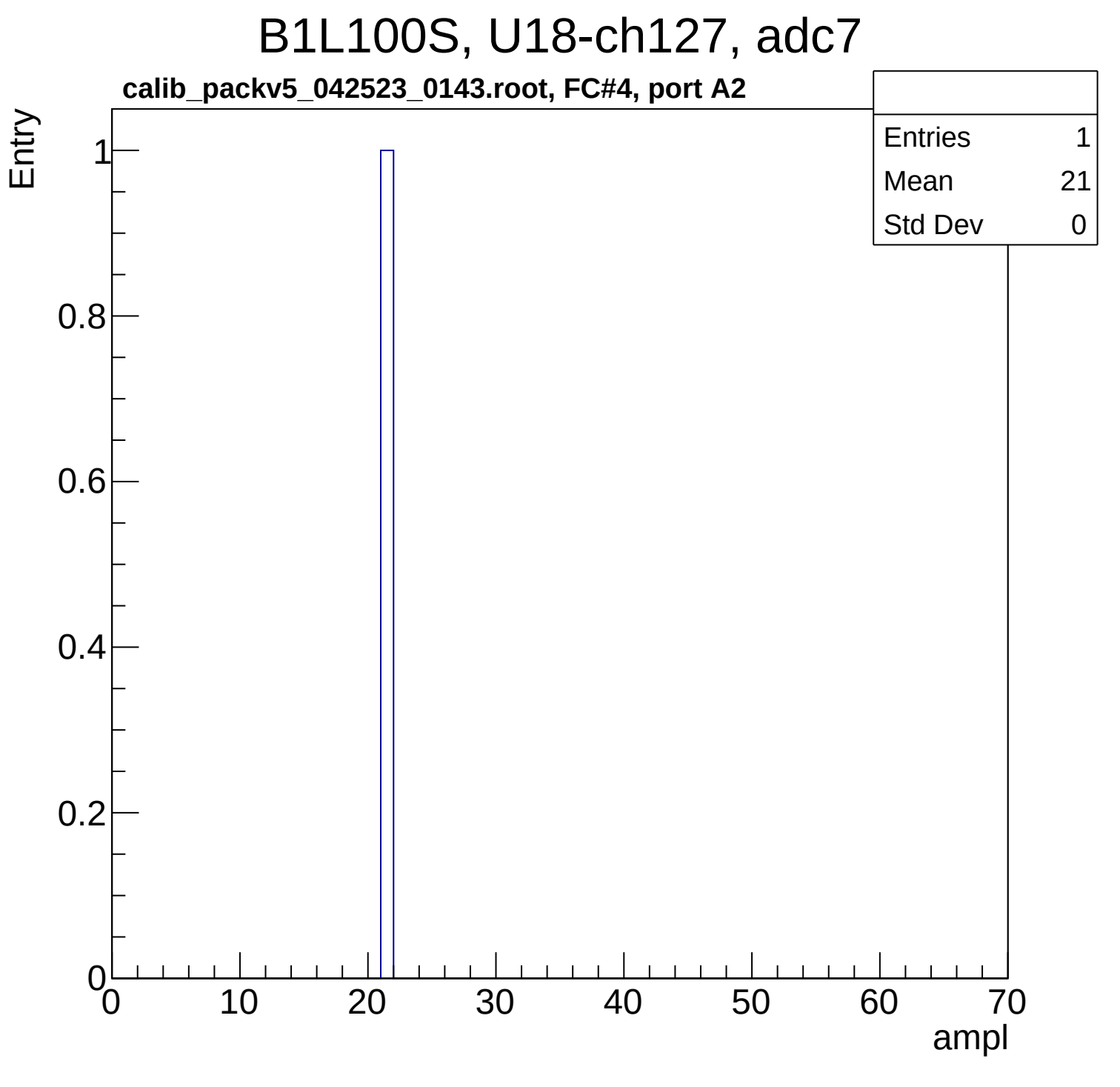

B1L100S, U18-ch127, adc3
calib_packv5_042523_0143.root, FC#4, port A2
Entries 82
Mean 49.8
Std Dev 4.047
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U18-ch127, adc4
calib_packv5_042523_0143.root, FC#4, port A2
Entries 43
Mean 55.81
Std Dev 3.201
Entry
ampl
0
1
2
3
4
5
6
7
0
10
20
30
40
50
60
70


B1L100S, U18-ch127, adc5
calib_packv5_042523_0143.root, FC#4, port A2
Entries 50
Mean 58.22
Std Dev 8.735
Entry
ampl
0
1
2
3
4
5
6
7
8
0
10
20
30
40
50
60
70


B1L100S, U18-ch127, adc6
calib_packv5_042523_0143.root, FC#4, port A2
Entries 6
Mean 62.33
Std Dev 0.4714
Entry
ampl
0
0.5
1
1.5
2
2.5
3
3.5
4
0
10
20
30
40
50
60
70


B1L100S, U18-ch127, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 21
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl


B1L100S, U18-ch127, adc7
calib_packv5_042523_0143.root, FC#4, port A2
Entries 1
Mean 21
Std Dev 0
Entry
1
0.8
0.6
0.4
0.2
0
0
10
20
30
40
50
60
70
ampl