



# B1L103S, U14-ch0

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	225
Mean	38.11
Std Dev	18.2

**Turn on : 24.5503**  
**Width : 4.289**  
**Height : 5.019**

Entry

25

20

15

10

5

0

0

10

20

30

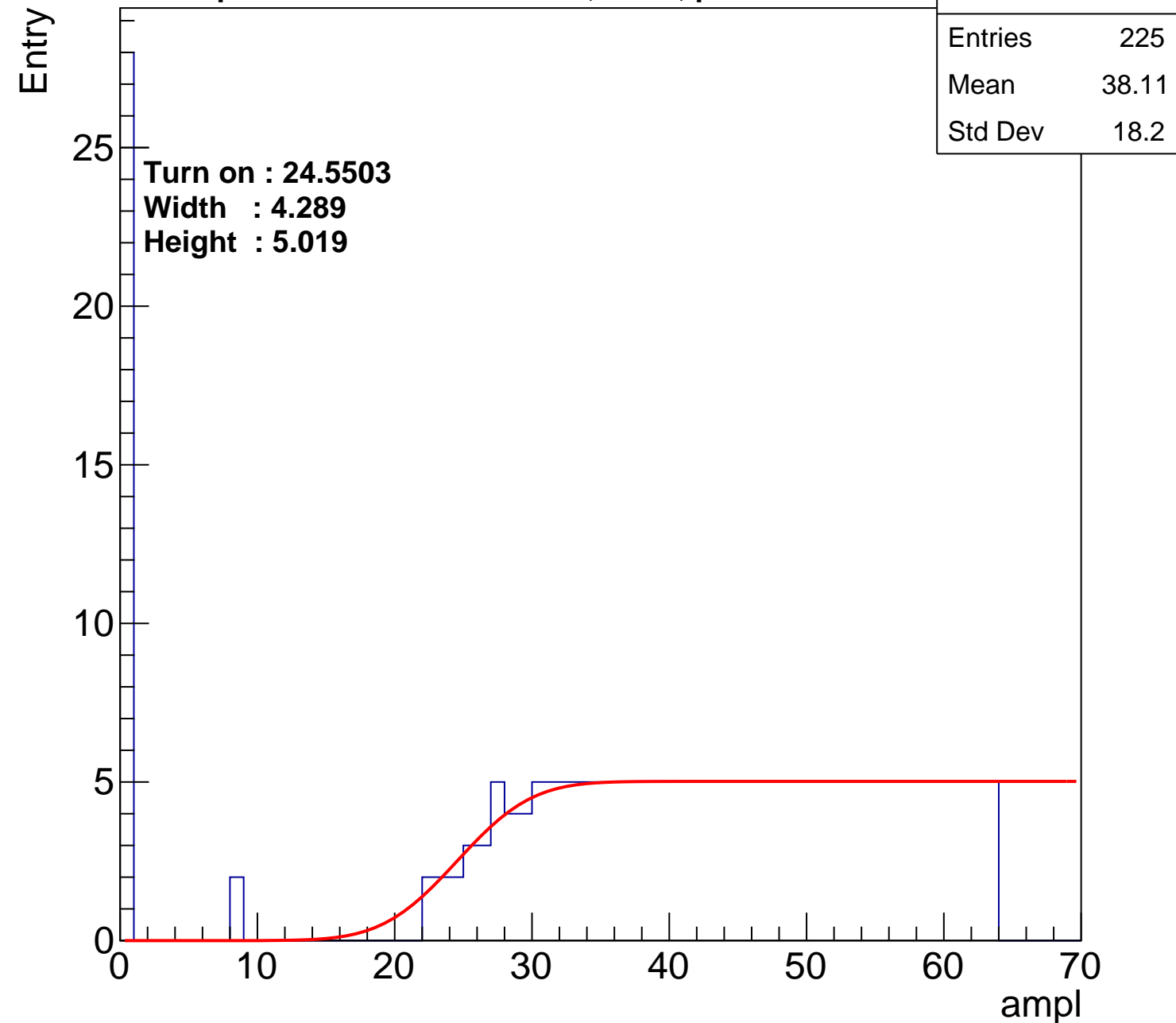
40

50

60

70

ampl



# B1L103S, U14-ch1

calib\_packv5\_041523\_1651.root, FC#0, port C2

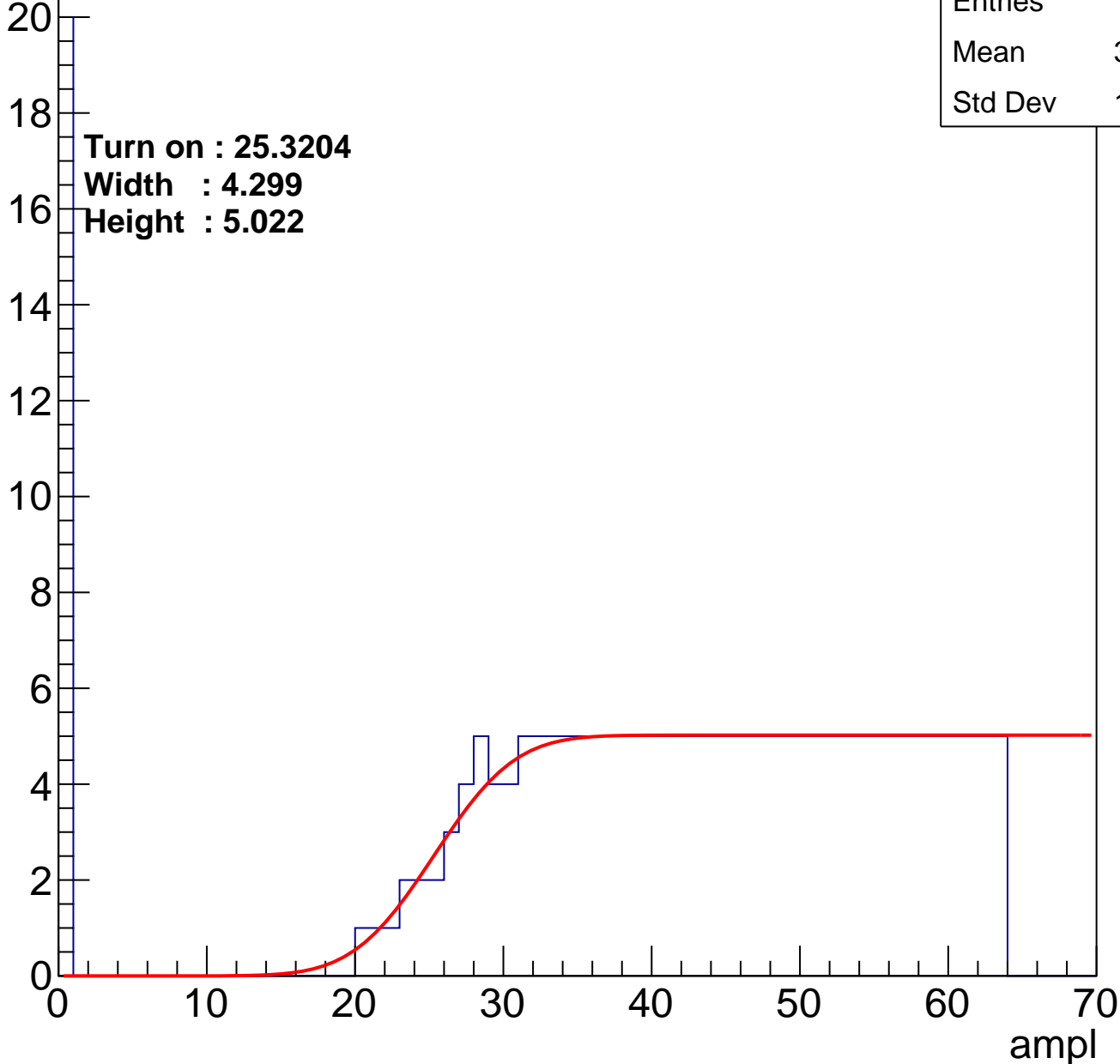
Entries	214
Mean	39.83
Std Dev	16.82

**Turn on : 25.3204**

**Width : 4.299**

**Height : 5.022**

Entry



# B1L103S, U14-ch2

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	220
Mean	38.75
Std Dev	17.81

**Turn on : 25.7108**

**Width : 4.097**

**Height : 5.030**

Entry

25

20

15

10

5

0

ampl

0

10

20

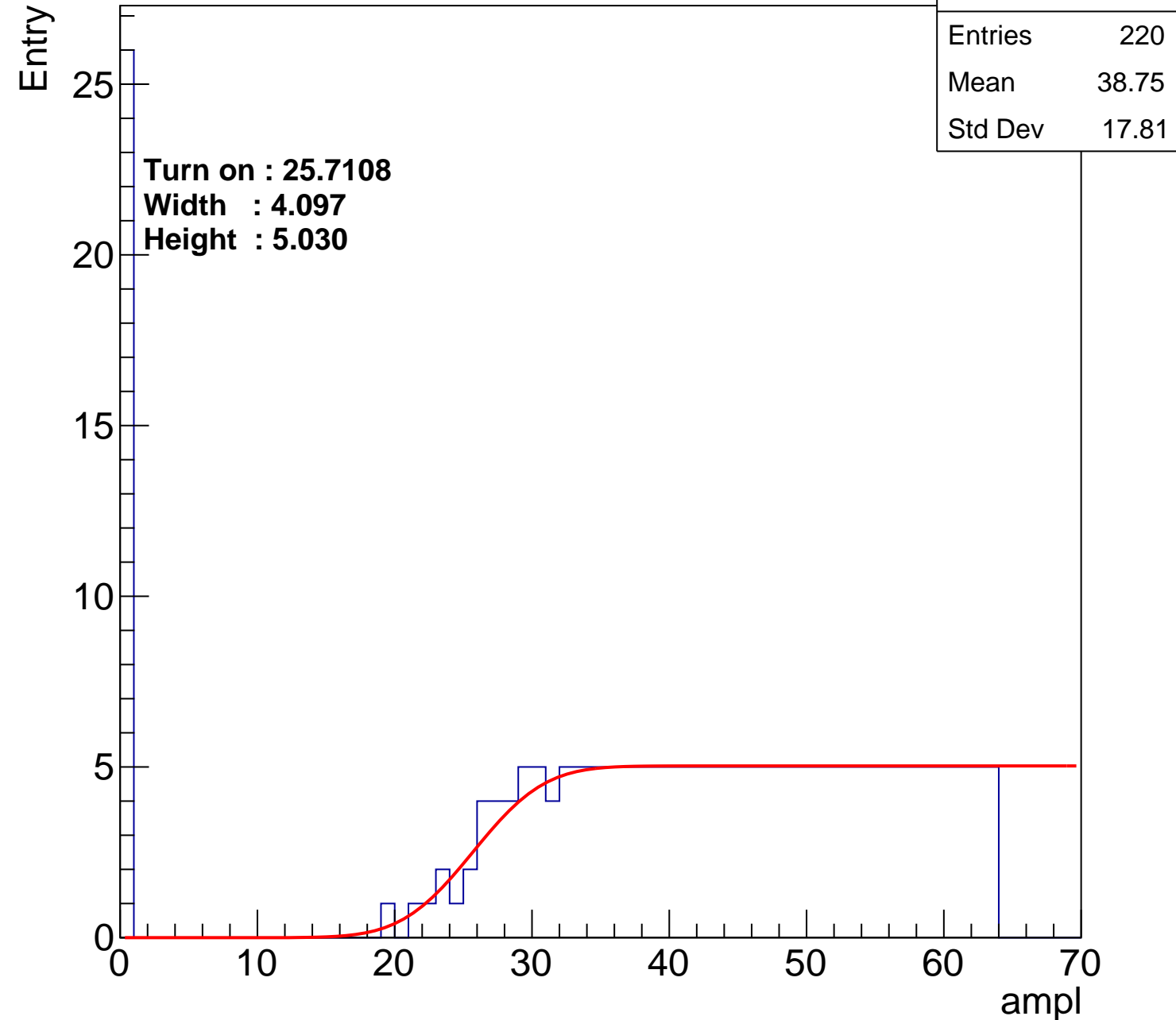
30

40

50

60

70



# B1L103S, U14-ch3

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	223
Mean	38.73
Std Dev	17.55

**Turn on : 24.9967**

**Width : 3.366**

**Height : 5.035**

Entry

25

20

15

10

5

0

0

10

20

30

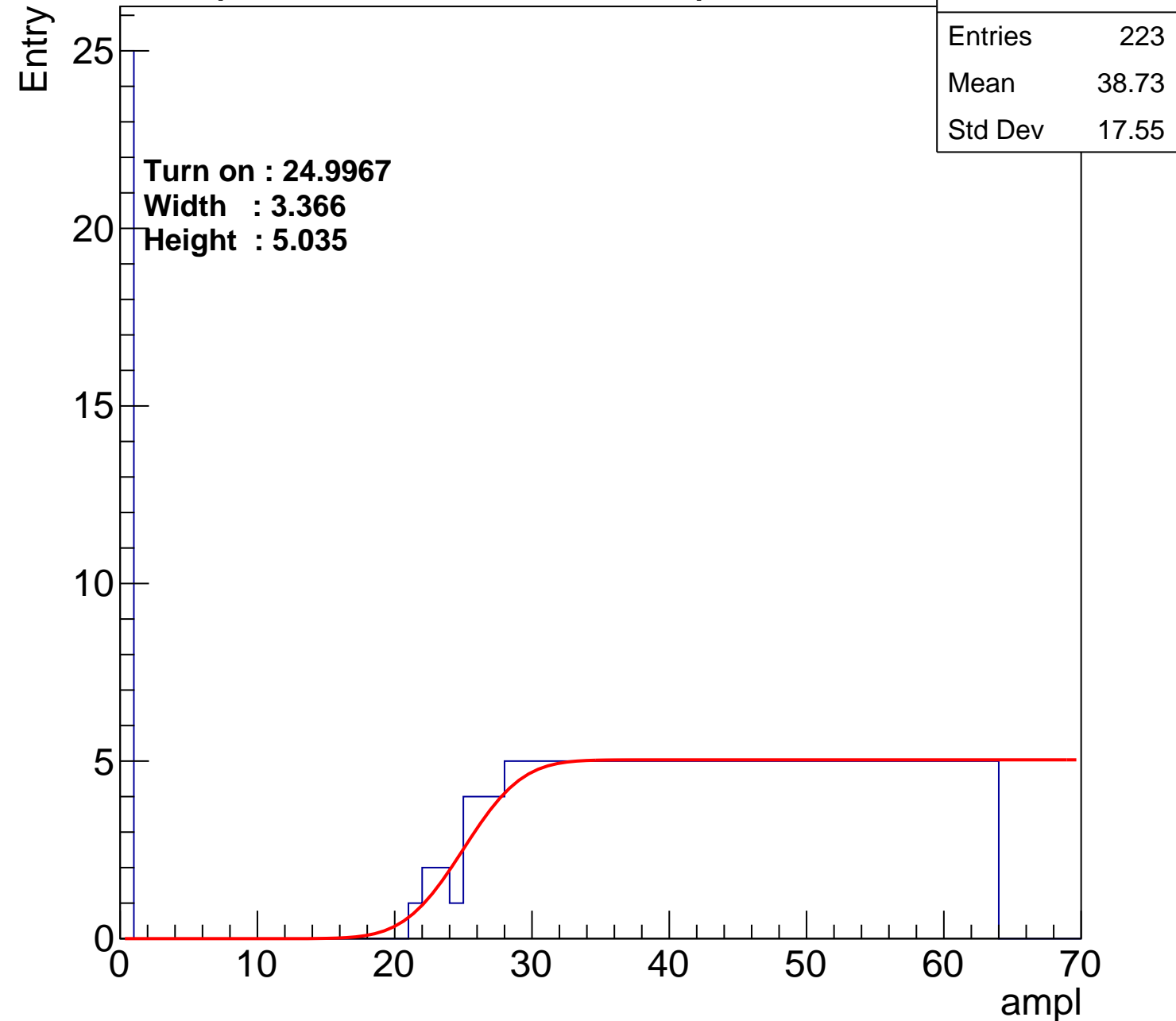
40

50

60

70

ampl



# B1L103S, U14-ch4

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	217
Mean	38.99
Std Dev	17.81

**Turn on : 25.9846**

**Width : 3.342**

**Height : 5.021**

Entry

25

20

15

10

5

0

ampl

0

10

20

30

40

50

60

70

# B1L103S, U14-ch5

calib\_packv5\_041523\_1651.root, FC#0, port C2

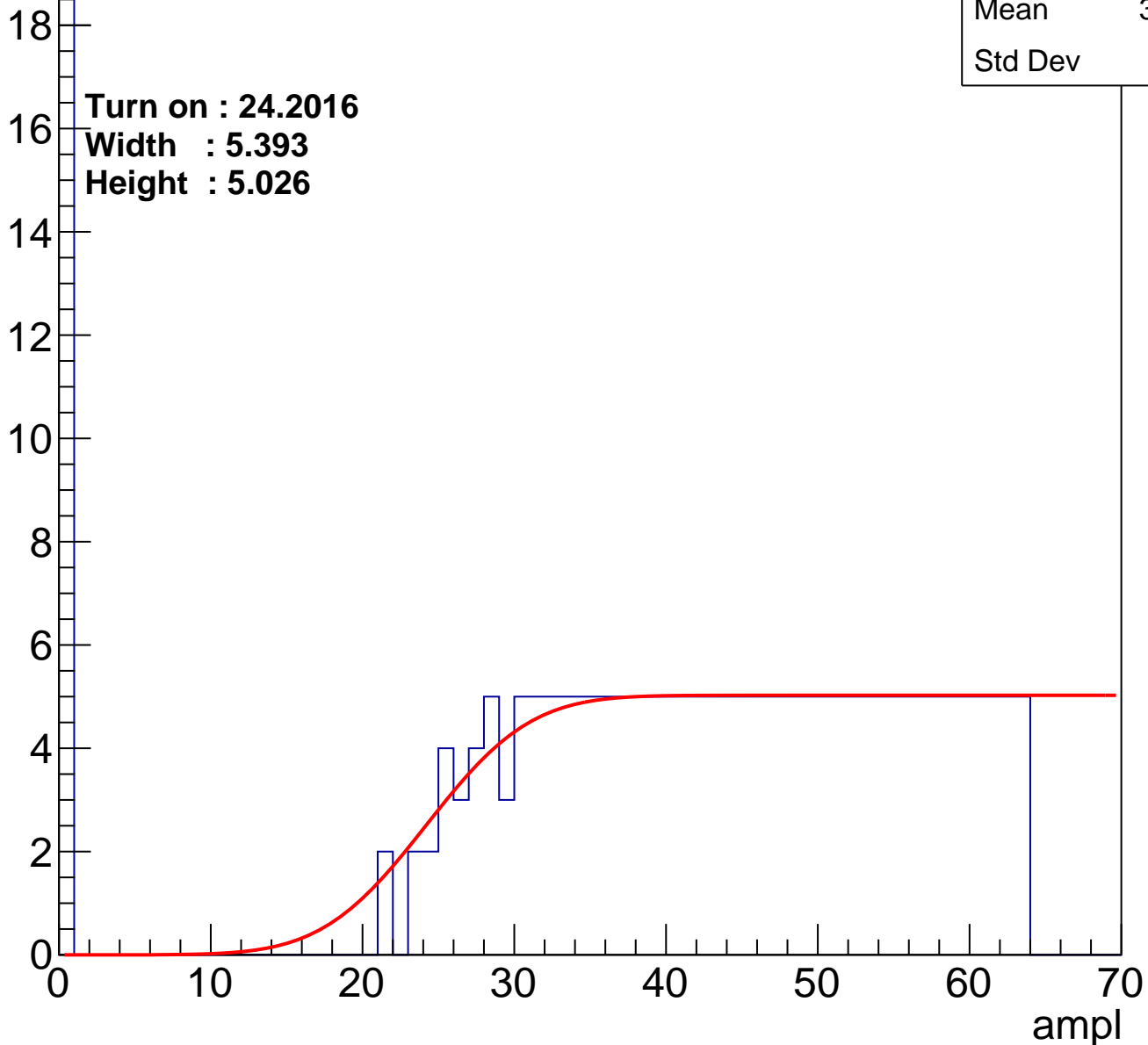
Entries	214
Mean	39.97
Std Dev	16.6

Turn on : 24.2016

Width : 5.393

Height : 5.026

Entry



# B1L103S, U14-ch6

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	217
Mean	38.81
Std Dev	18.11

**Turn on : 26.0677**  
**Width : 1.955**  
**Height : 4.999**

Entry

25

20

15

10

5

0

ampl

0

10

20

30

40

50

60

70



# B1L103S, U14-ch7

calib\_packv5\_041523\_1651.root, FC#0, port C2

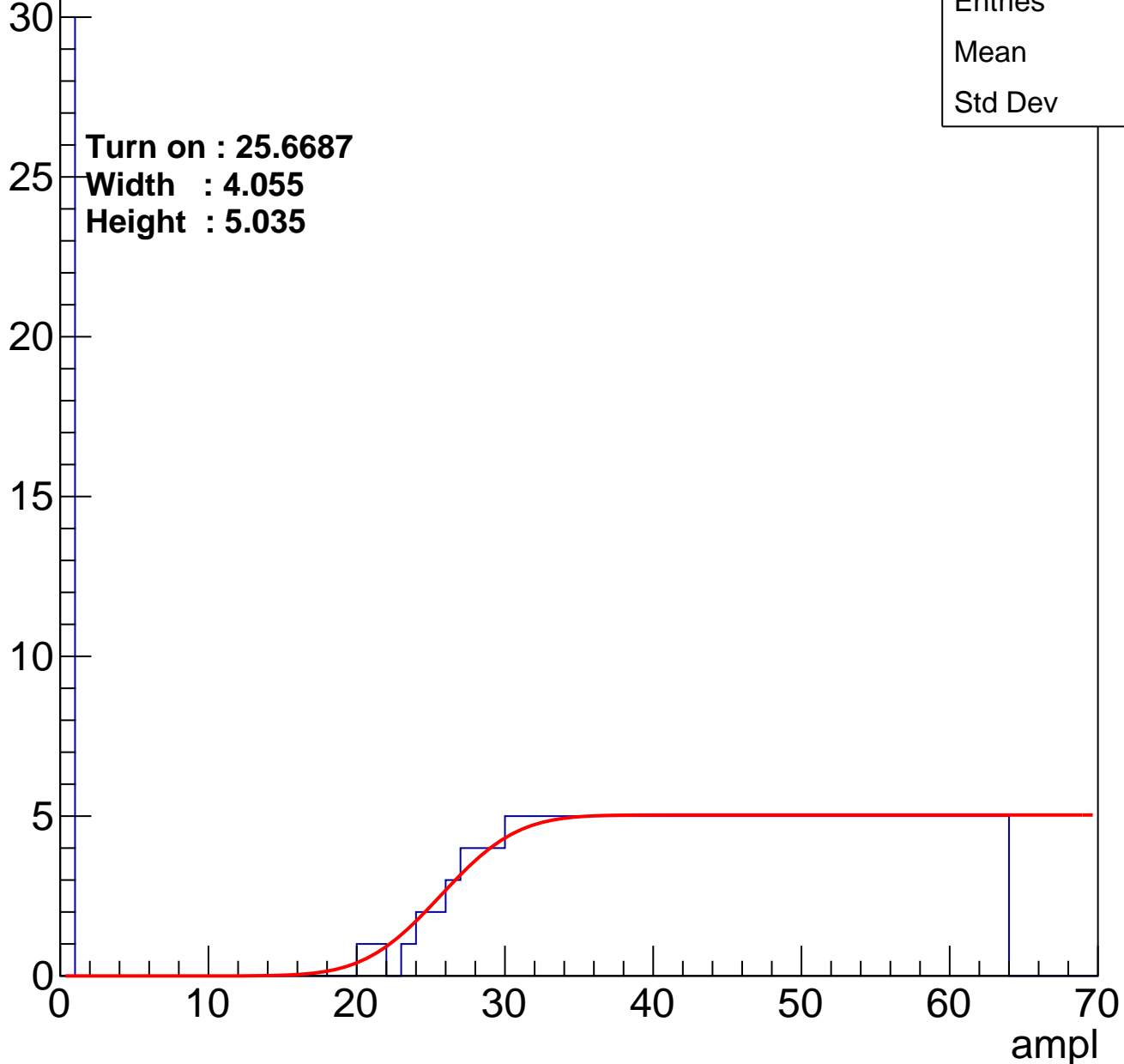
Entries	222
Mean	38.2
Std Dev	18.4

**Turn on : 25.6687**

**Width : 4.055**

**Height : 5.035**

Entry



# B1L103S, U14-ch8

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	220
Mean	38.79
Std Dev	17.78

**Turn on : 25.3442**

**Width : 3.393**

**Height : 5.016**

Entry

25

20

15

10

5

0

0

10

20

30

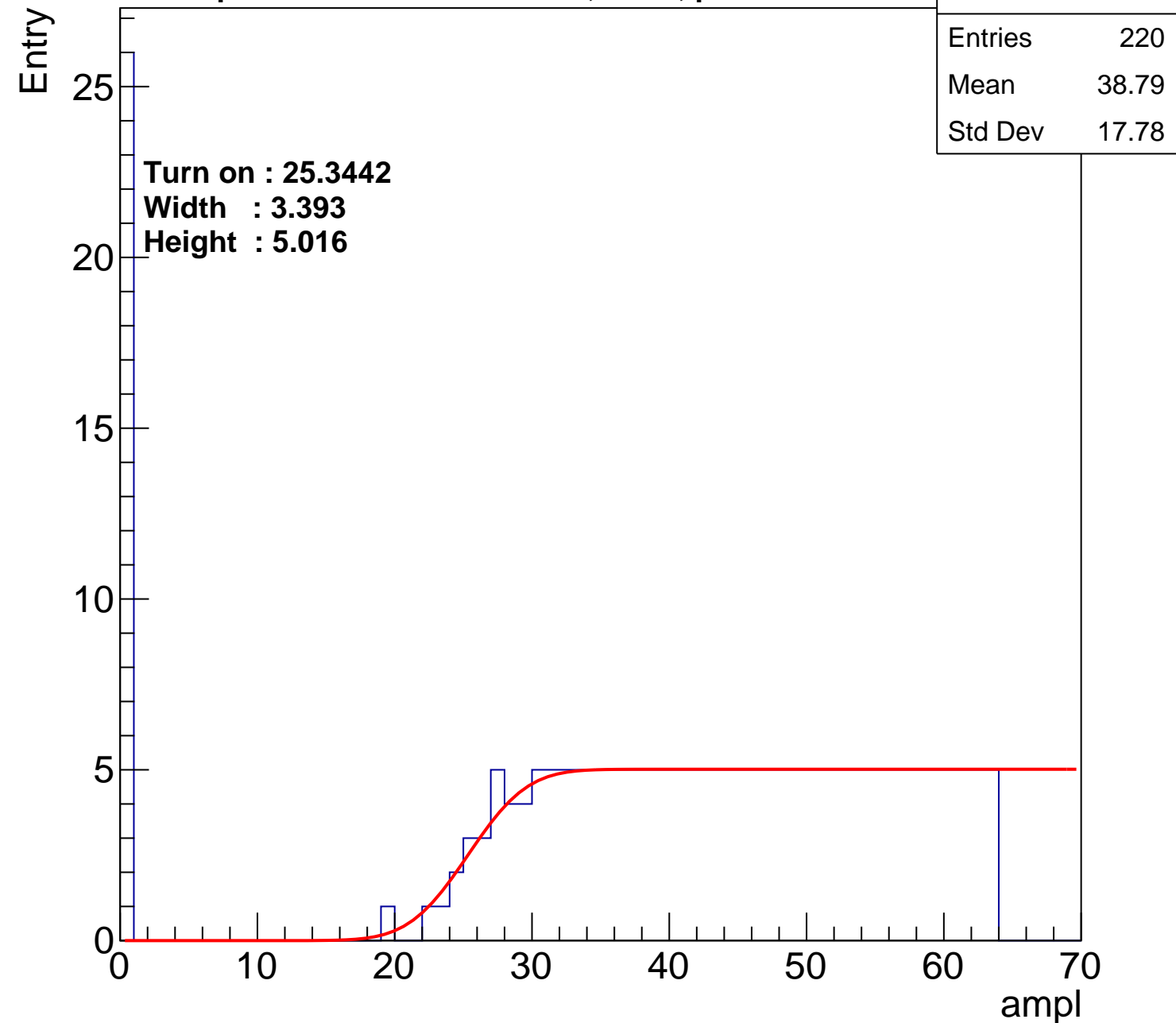
40

50

60

70

ampl



# B1L103S, U14-ch9

calib\_packv5\_041523\_1651.root, FC#0, port C2

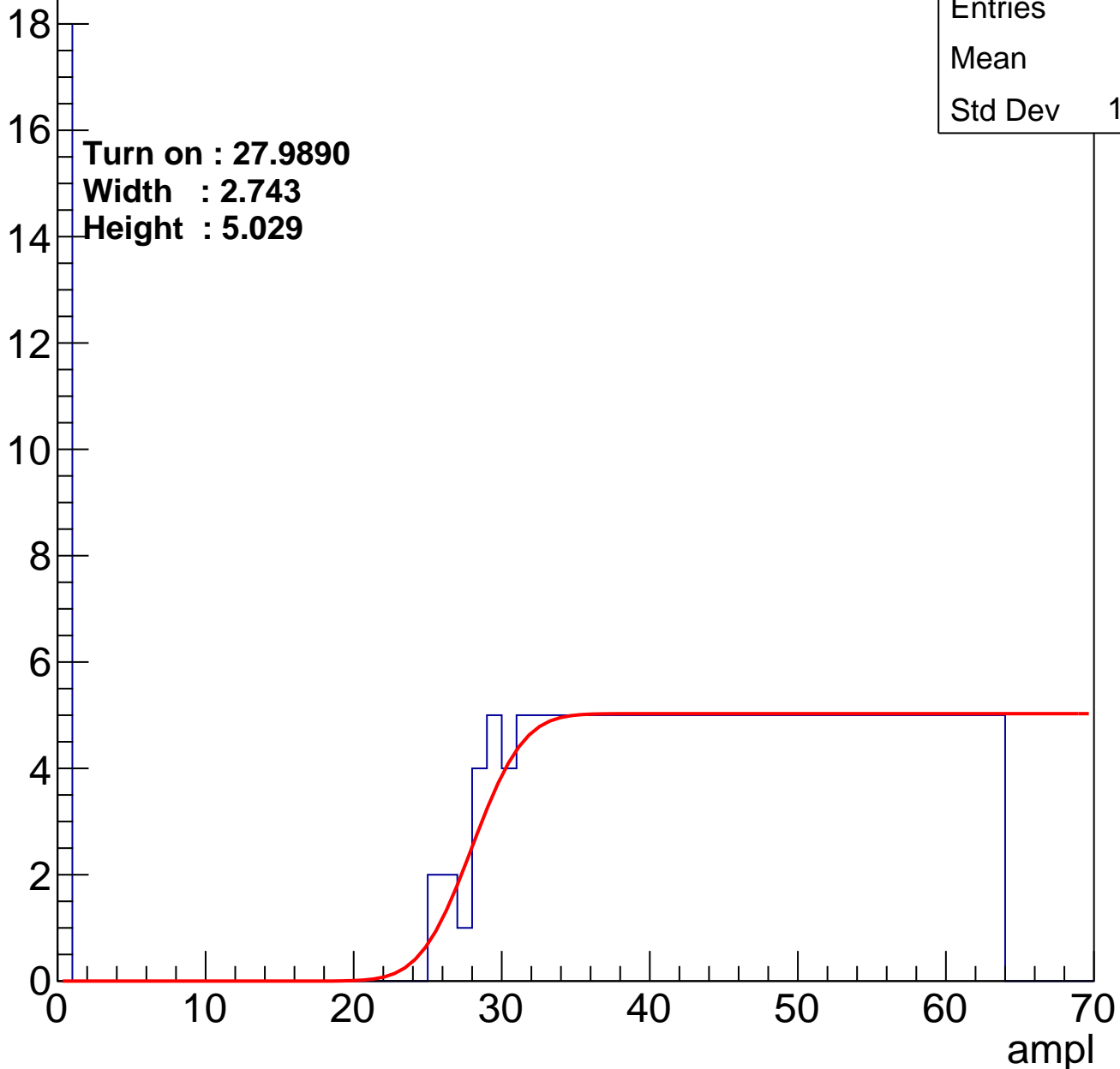
Entries	201
Mean	41.1
Std Dev	16.42

Turn on : 27.9890

Width : 2.743

Height : 5.029

Entry



# B1L103S, U14-ch10

calib\_packv5\_041523\_1651.root, FC#0, port C2

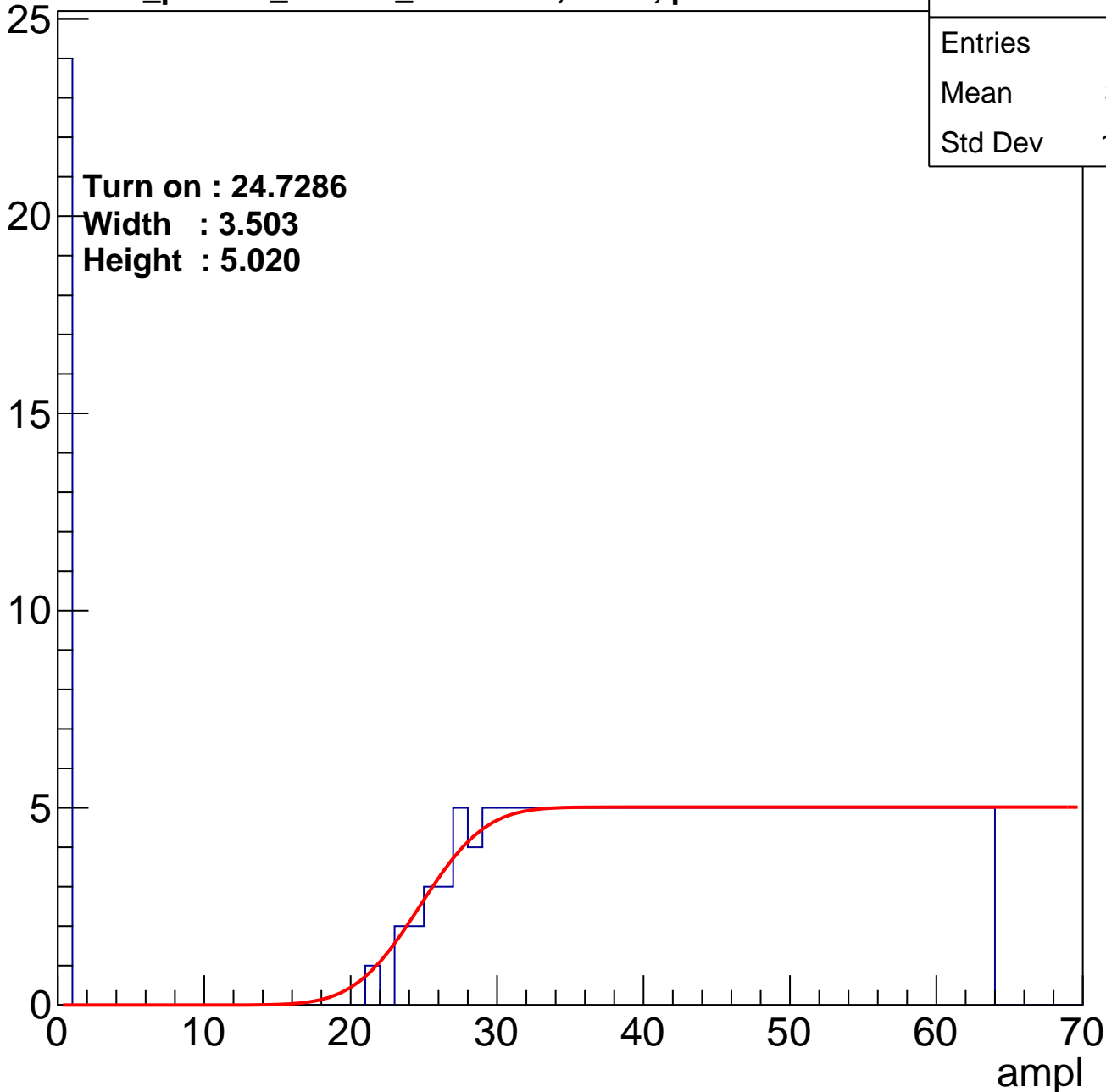
Entries	219
Mean	39.11
Std Dev	17.43

Turn on : 24.7286

Width : 3.503

Height : 5.020

Entry



# B1L103S, U14-ch11

calib\_packv5\_041523\_1651.root, FC#0, port C2

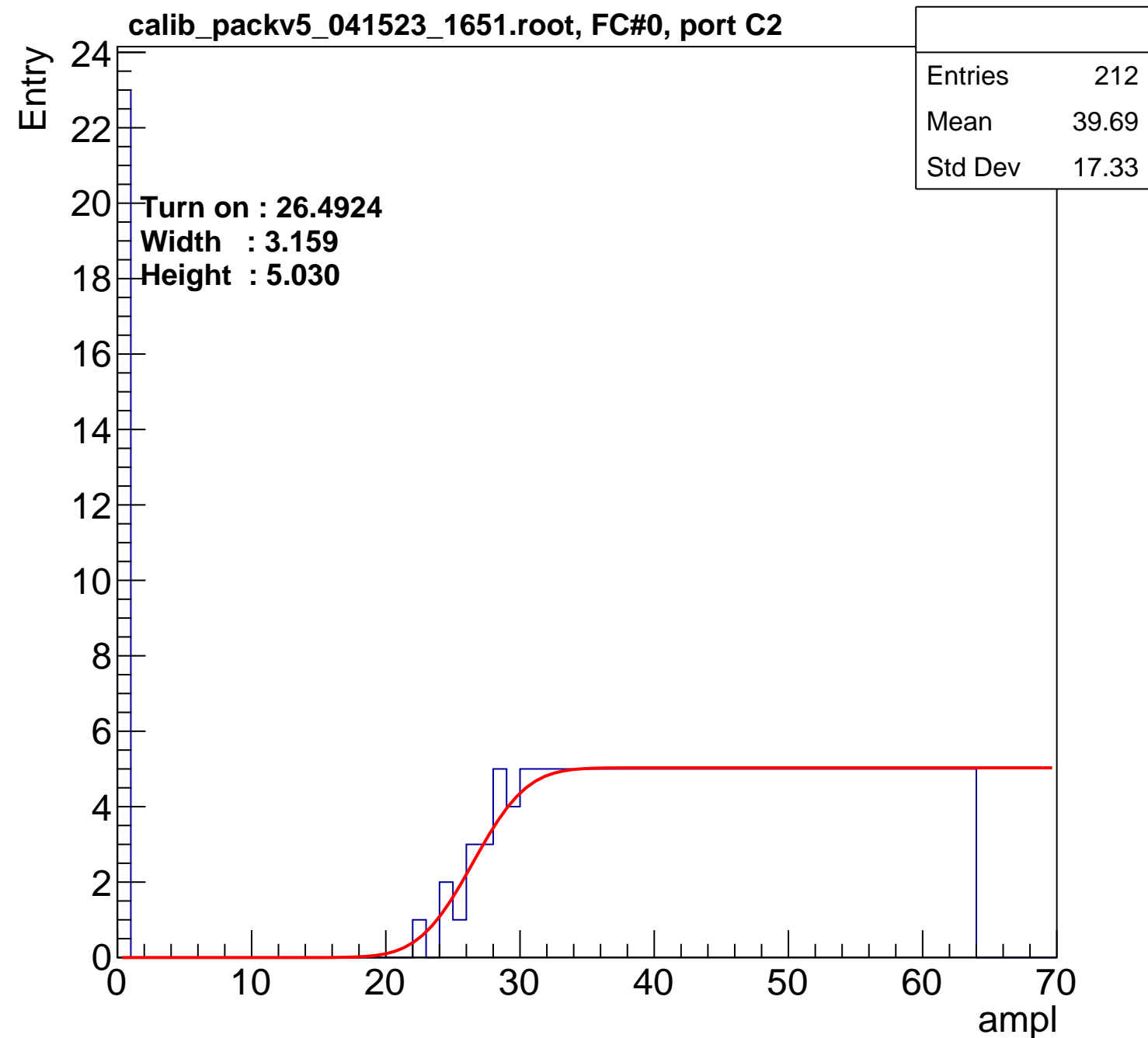
Entry

24  
22  
20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

Turn on : 26.4924  
Width : 3.159  
Height : 5.030

Entries	212
Mean	39.69
Std Dev	17.33

ampl



# B1L103S, U14-ch12

calib\_packv5\_041523\_1651.root, FC#0, port C2

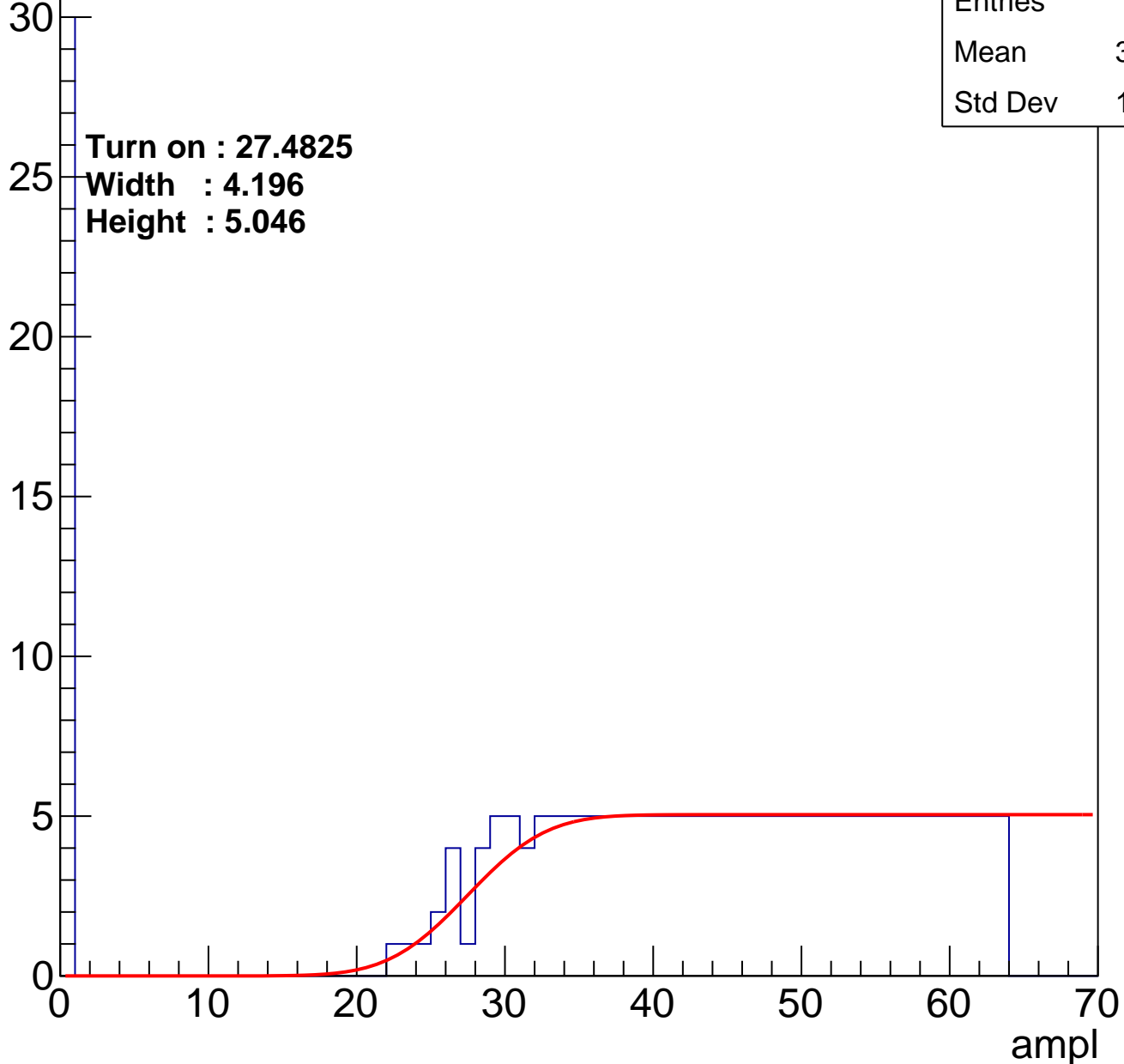
Entries	218
Mean	38.44
Std Dev	18.47

**Turn on : 27.4825**

**Width : 4.196**

**Height : 5.046**

Entry



# B1L103S, U14-ch13

calib\_packv5\_041523\_1651.root, FC#0, port C2

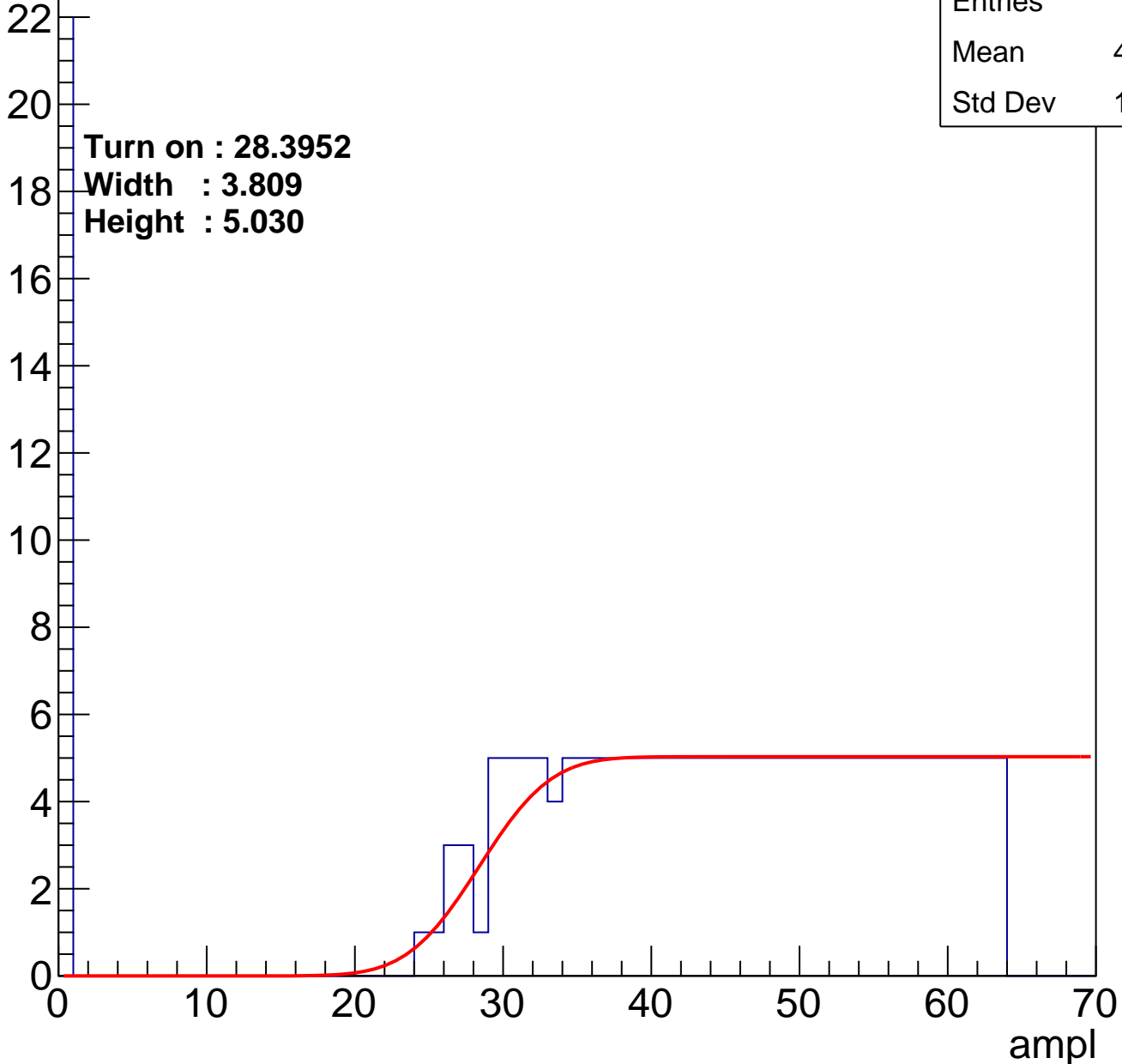
Entries	205
Mean	40.26
Std Dev	17.25

**Turn on : 28.3952**

**Width : 3.809**

**Height : 5.030**

Entry



# B1L103S, U14-ch14

calib\_packv5\_041523\_1651.root, FC#0, port C2

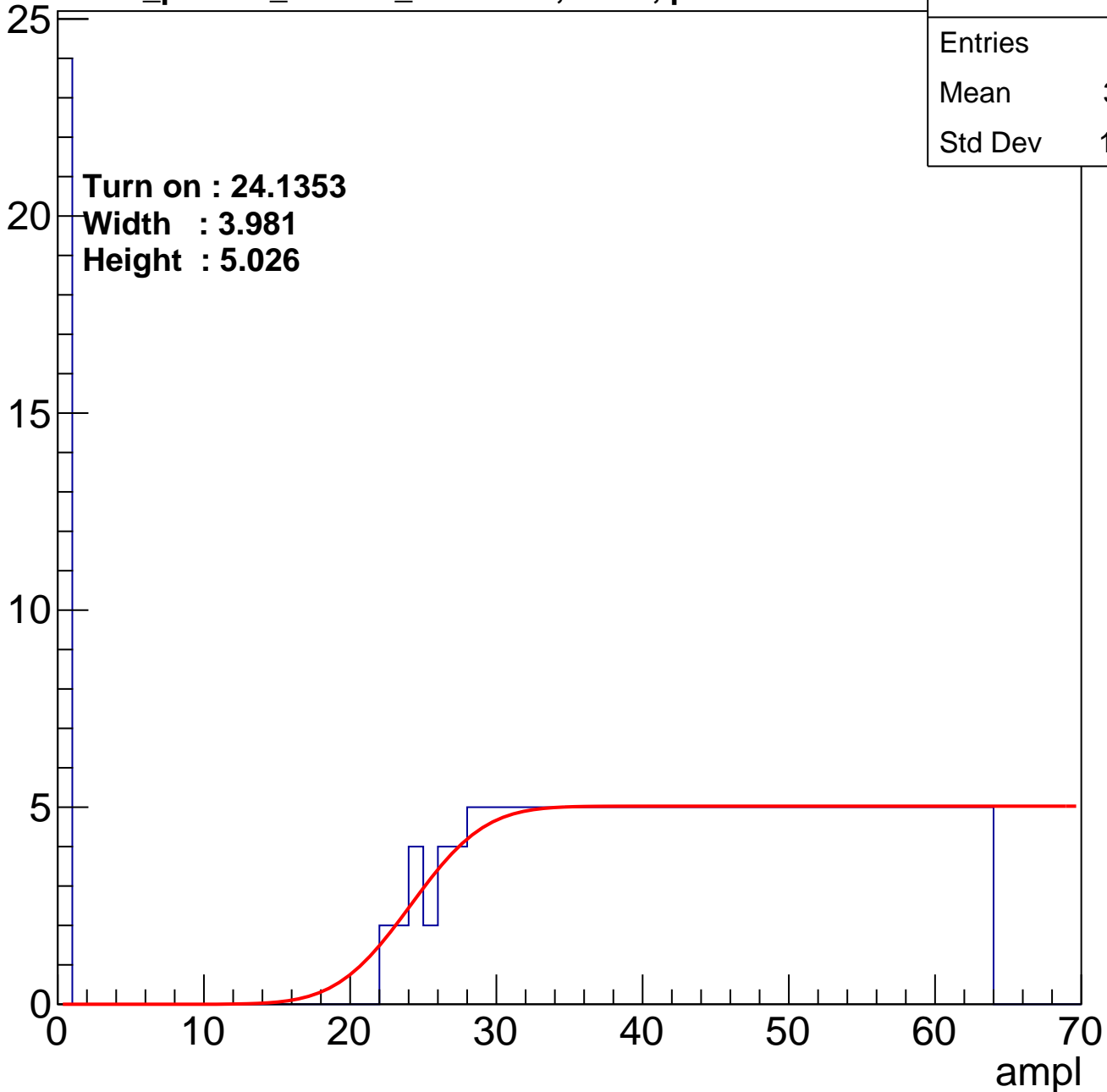
Entries	222
Mean	38.91
Std Dev	17.39

Turn on : 24.1353

Width : 3.981

Height : 5.026

Entry





# B1L103S, U14-ch15

calib\_packv5\_041523\_1651.root, FC#0, port C2

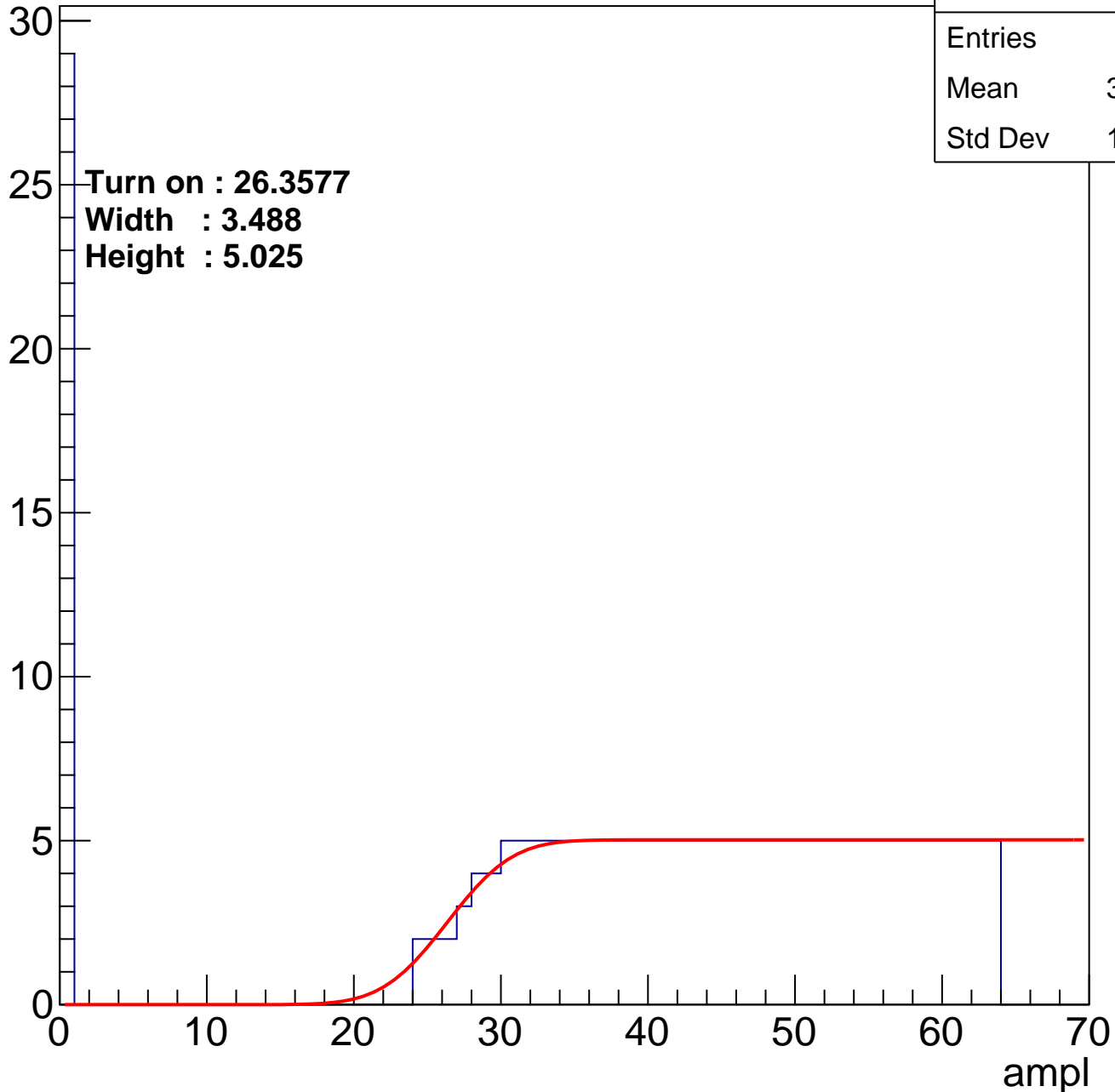
Entries	216
Mean	38.72
Std Dev	18.32

Turn on : 26.3577

Width : 3.488

Height : 5.025

Entry



# B1L103S, U14-ch16

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	224
Mean	38.61
Std Dev	17.69

**Turn on : 25.3404**

**Width : 3.962**

**Height : 5.079**

Entry

25

20

15

10

5

0

0

10

20

30

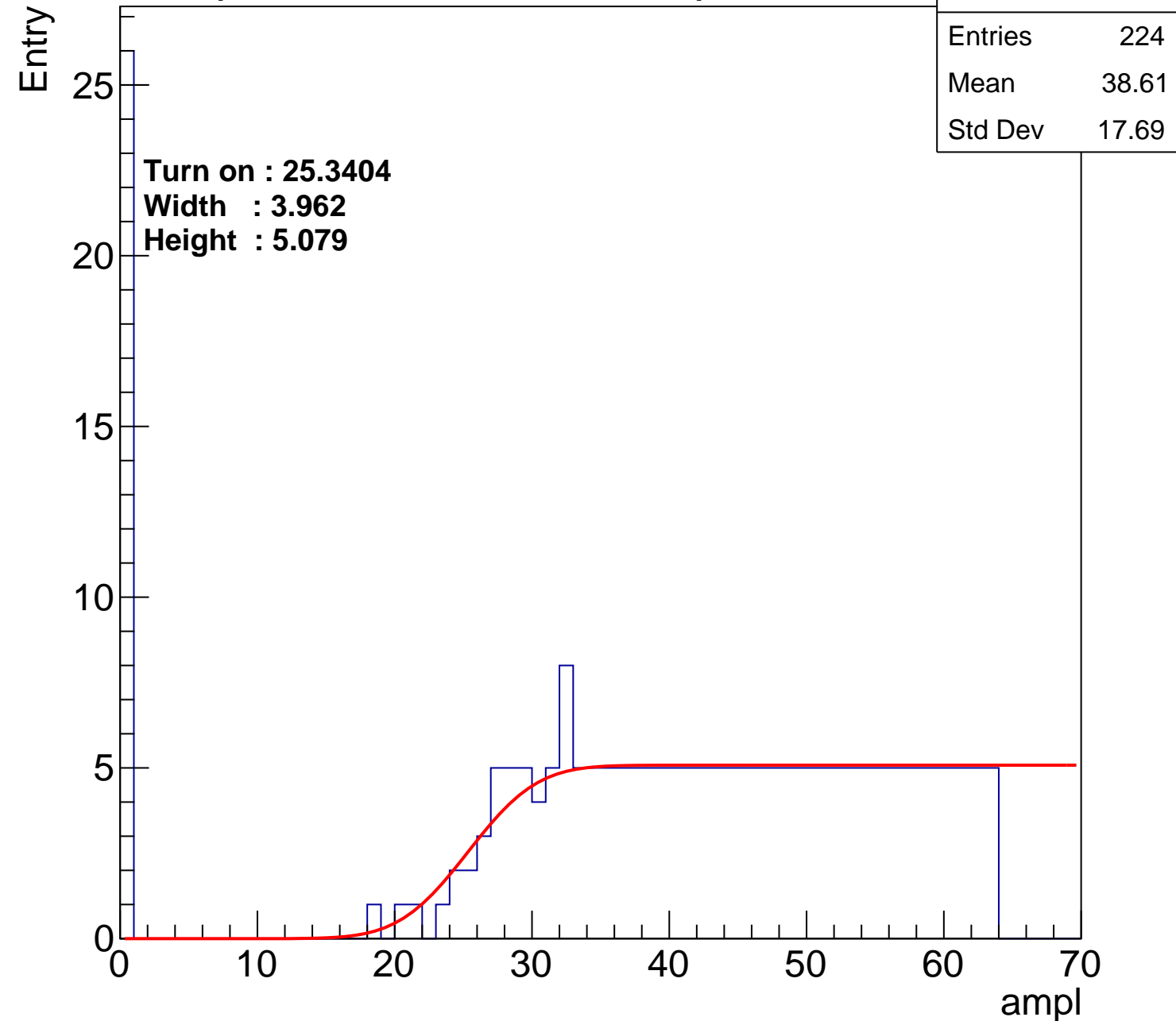
40

50

60

70

ampl



# B1L103S, U14-ch17

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	200
Mean	41.57
Std Dev	15.73

**Turn on : 27.0793**

**Width : 2.482**

**Height : 5.010**

Entry

14

12

10

8

6

4

2

0

0

10

20

30

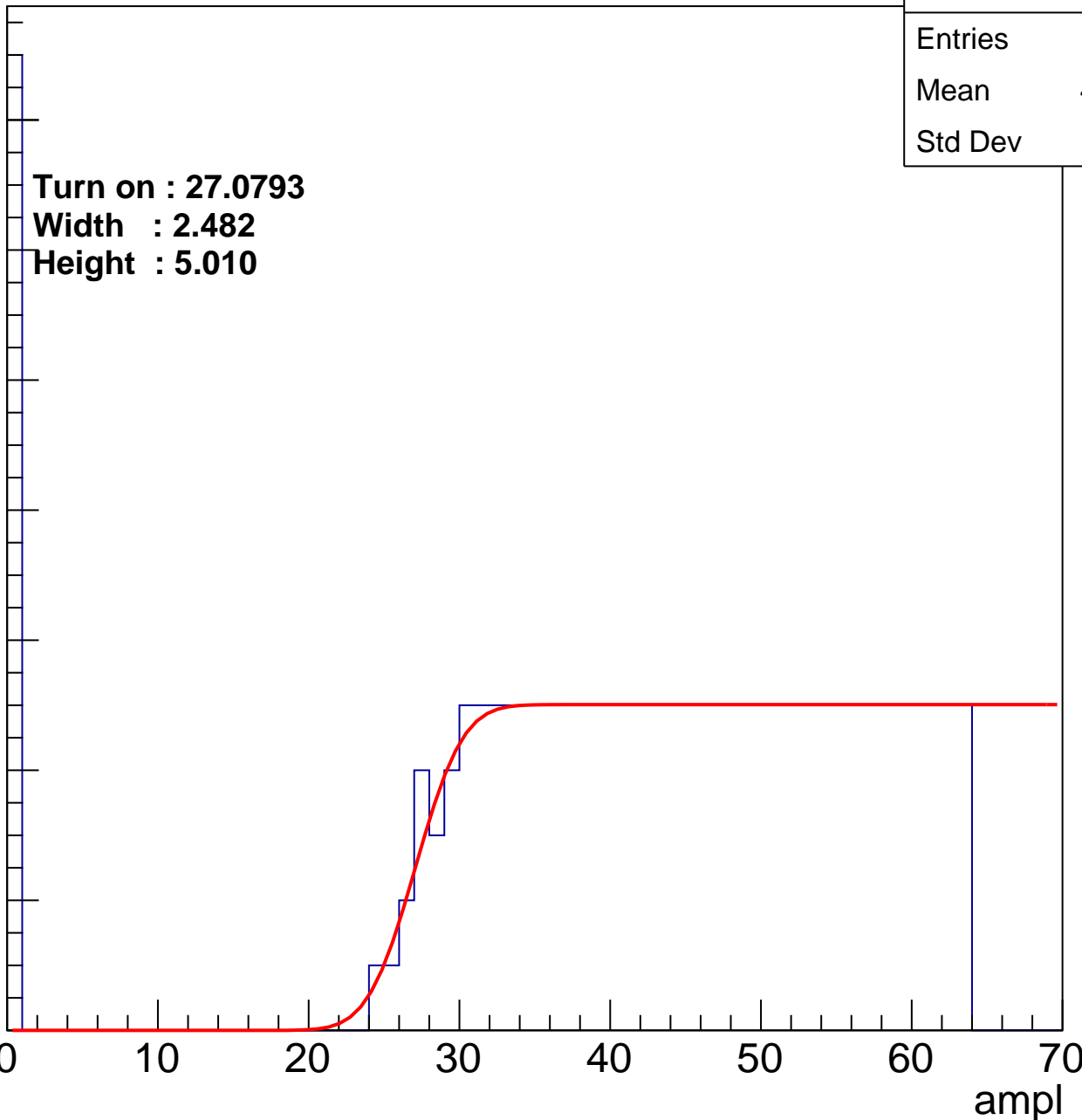
40

50

60

70

ampl



# B1L103S, U14-ch18

calib\_packv5\_041523\_1651.root, FC#0, port C2

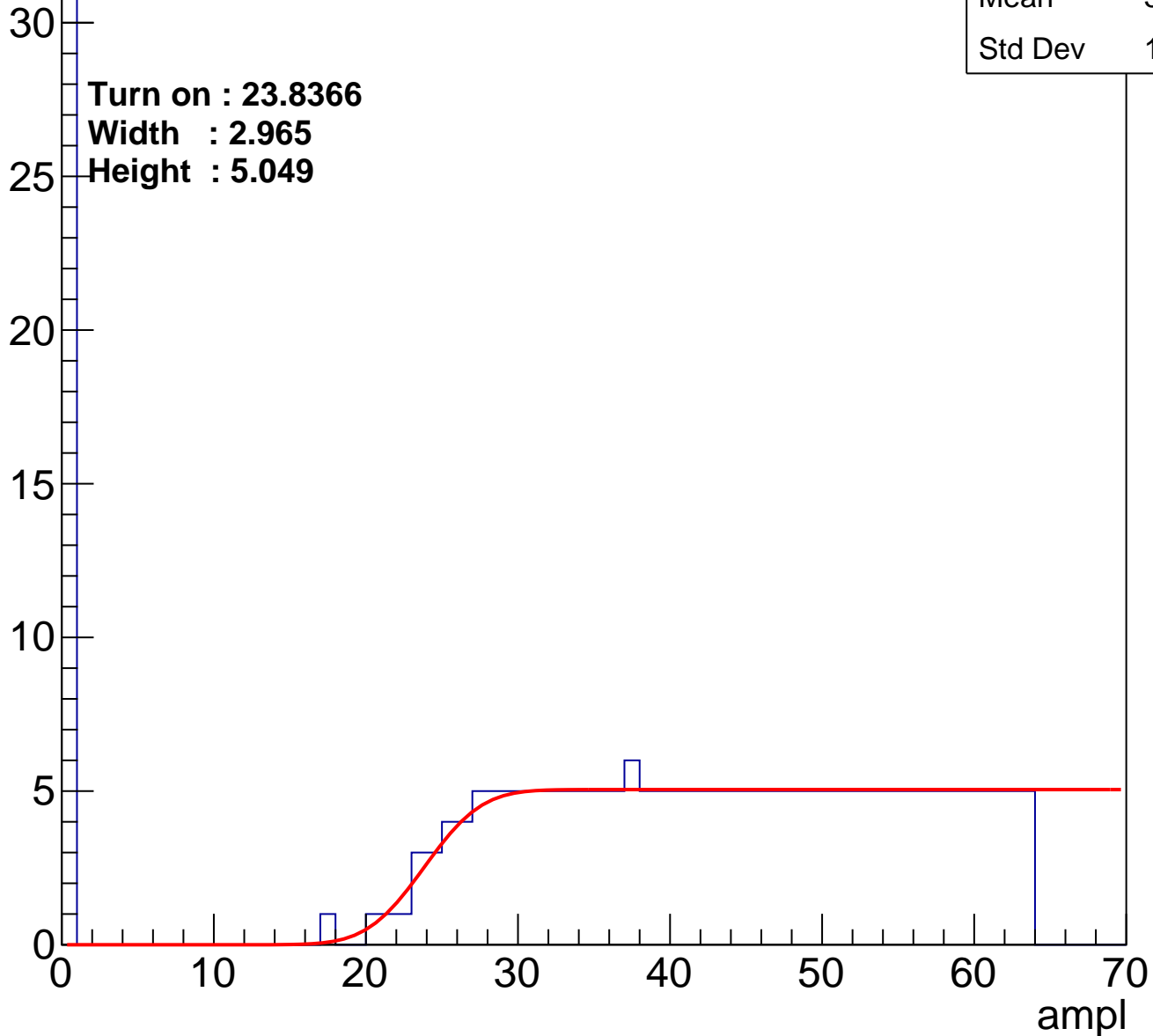
Entries	236
Mean	37.23
Std Dev	18.42

**Turn on : 23.8366**

**Width : 2.965**

**Height : 5.049**

Entry



# B1L103S, U14-ch19

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

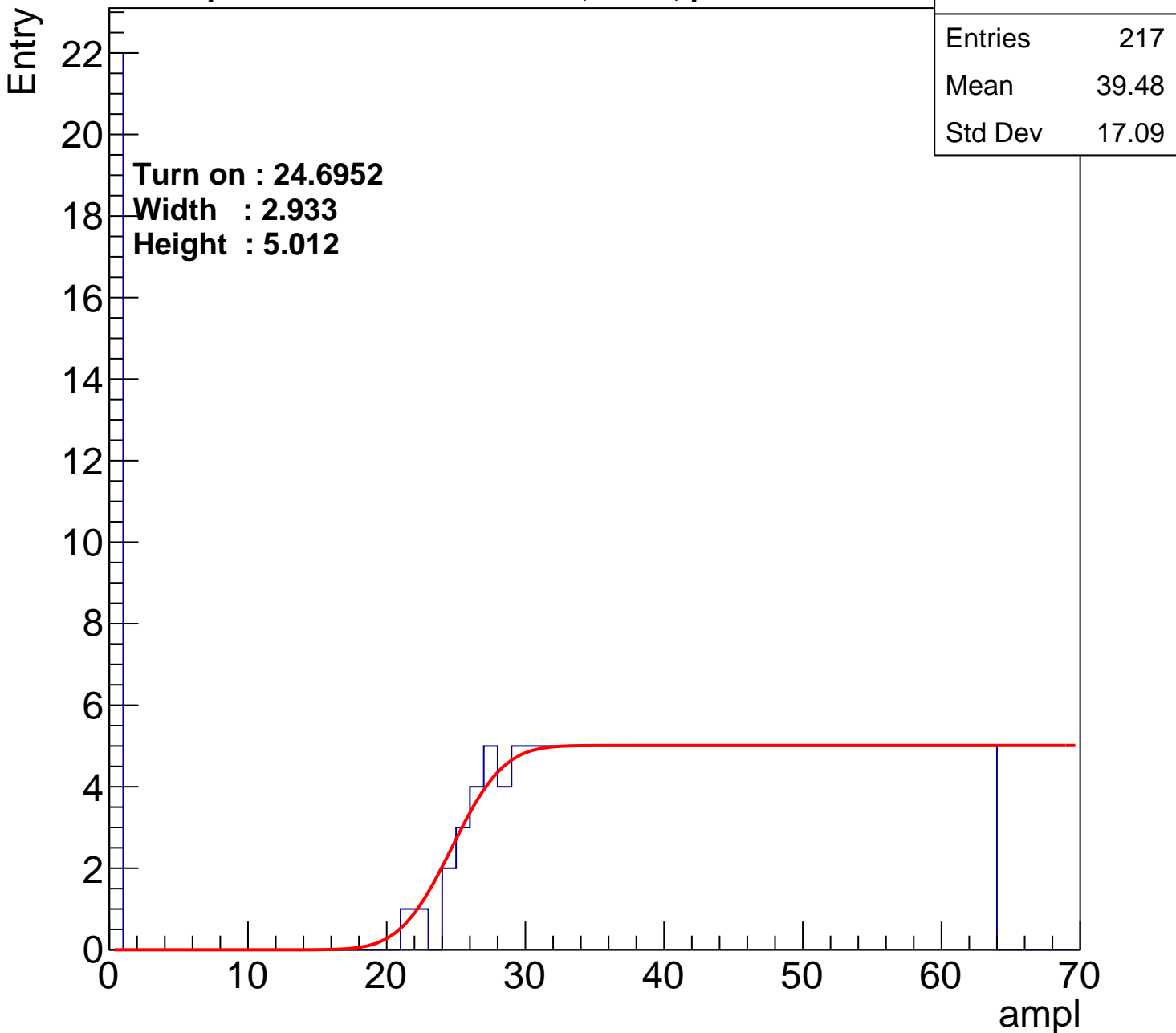
22  
20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 24.6952**  
**Width : 2.933**  
**Height : 5.012**

Entries	217
Mean	39.48
Std Dev	17.09

ampl

0 10 20 30 40 50 60 70



# B1L103S, U14-ch20

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	215
Mean	38.94
Std Dev	18.06

**Turn on : 26.9306**

**Width : 4.528**

**Height : 5.039**

Entry

25

20

15

10

5

0

0

10

20

30

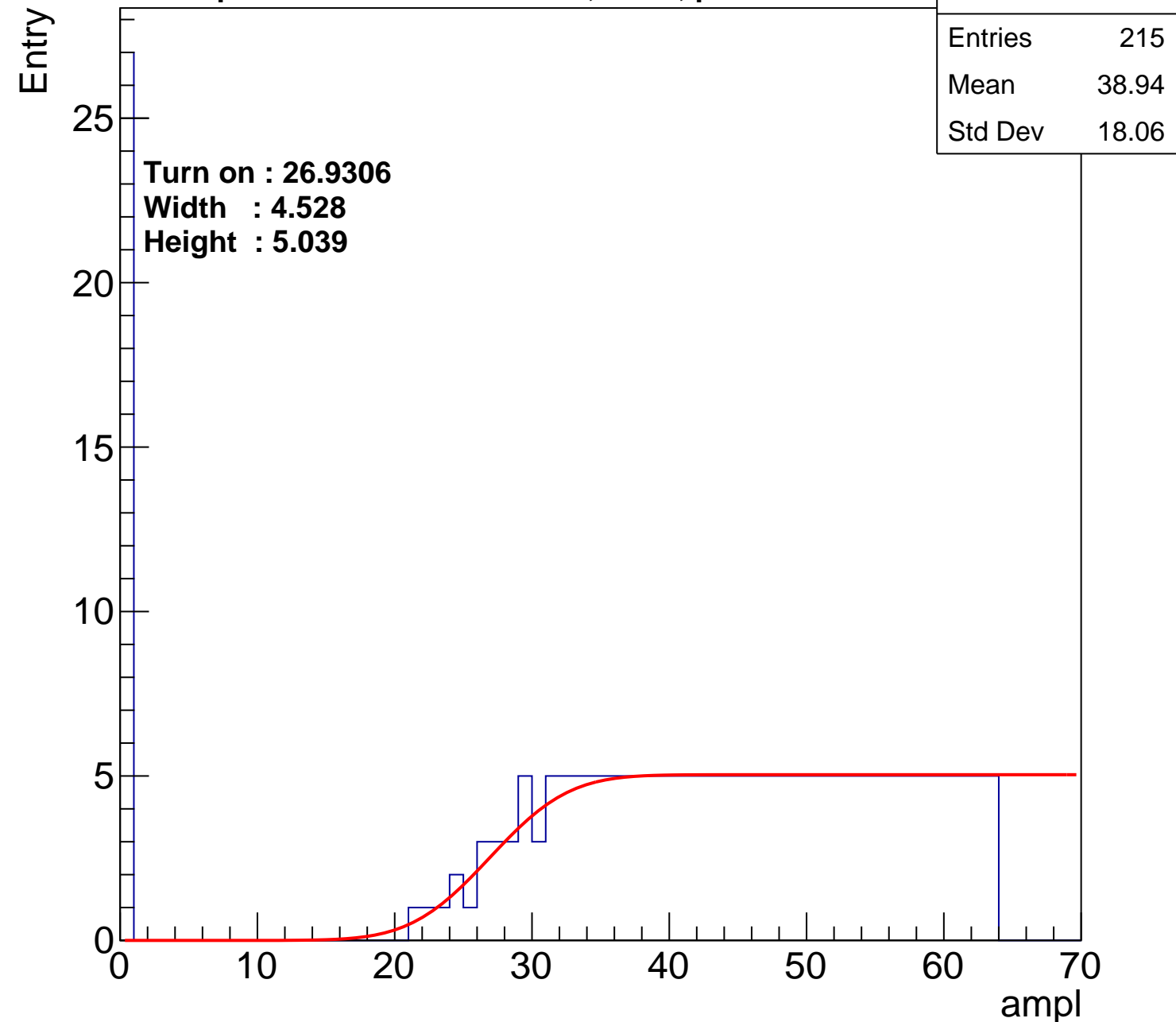
40

50

60

70

ampl



# B1L103S, U14-ch21

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	221
Mean	37.95
Std Dev	18.87

**Turn on : 26.9364**

**Width : 3.741**

**Height : 5.039**

Entry

30

25

20

15

10

5

0

0

10

20

30

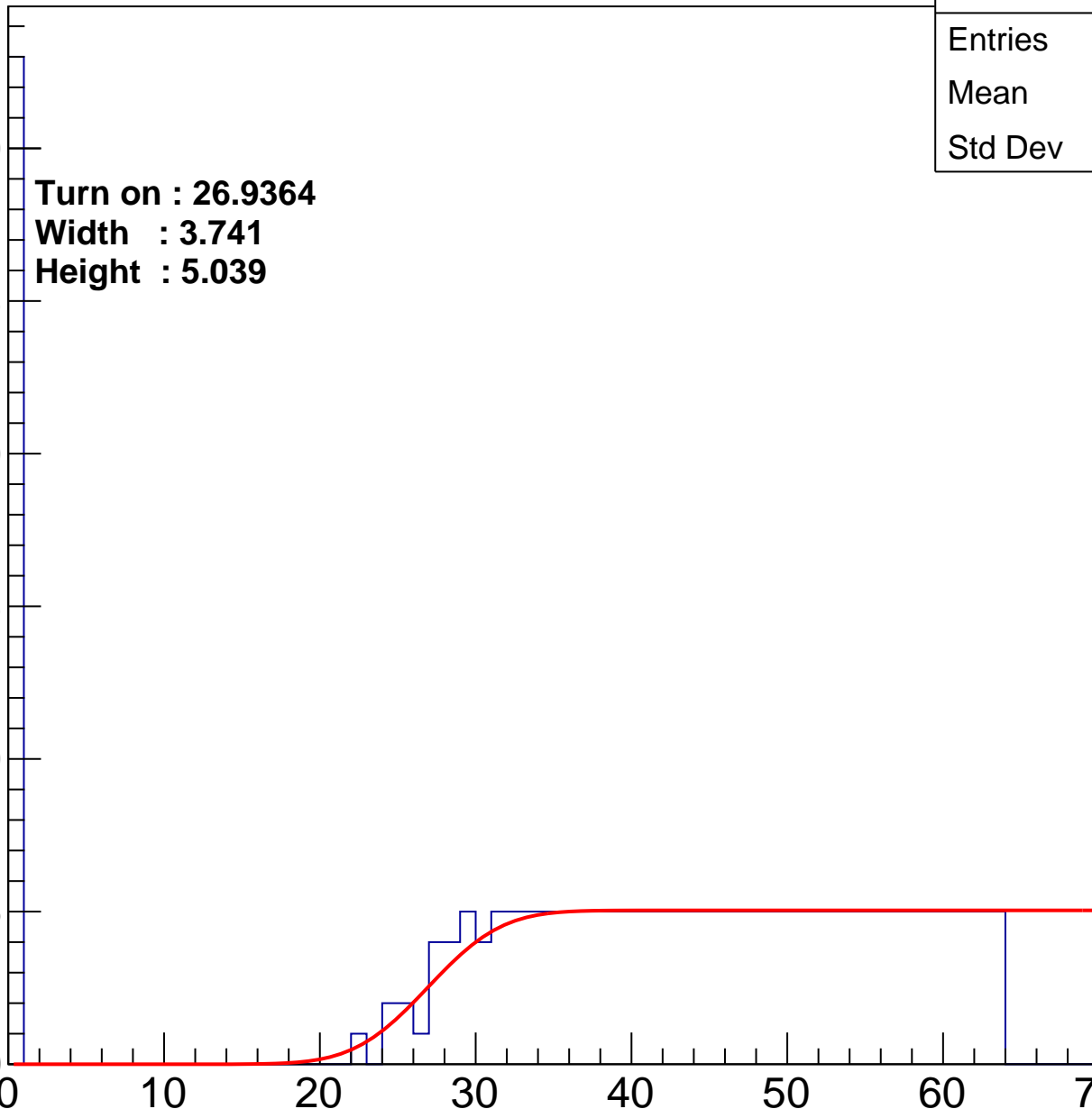
40

50

60

70

ampl



# B1L103S, U14-ch22

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	217
Mean	38.99
Std Dev	17.82

**Turn on : 25.9442**

**Width : 2.755**

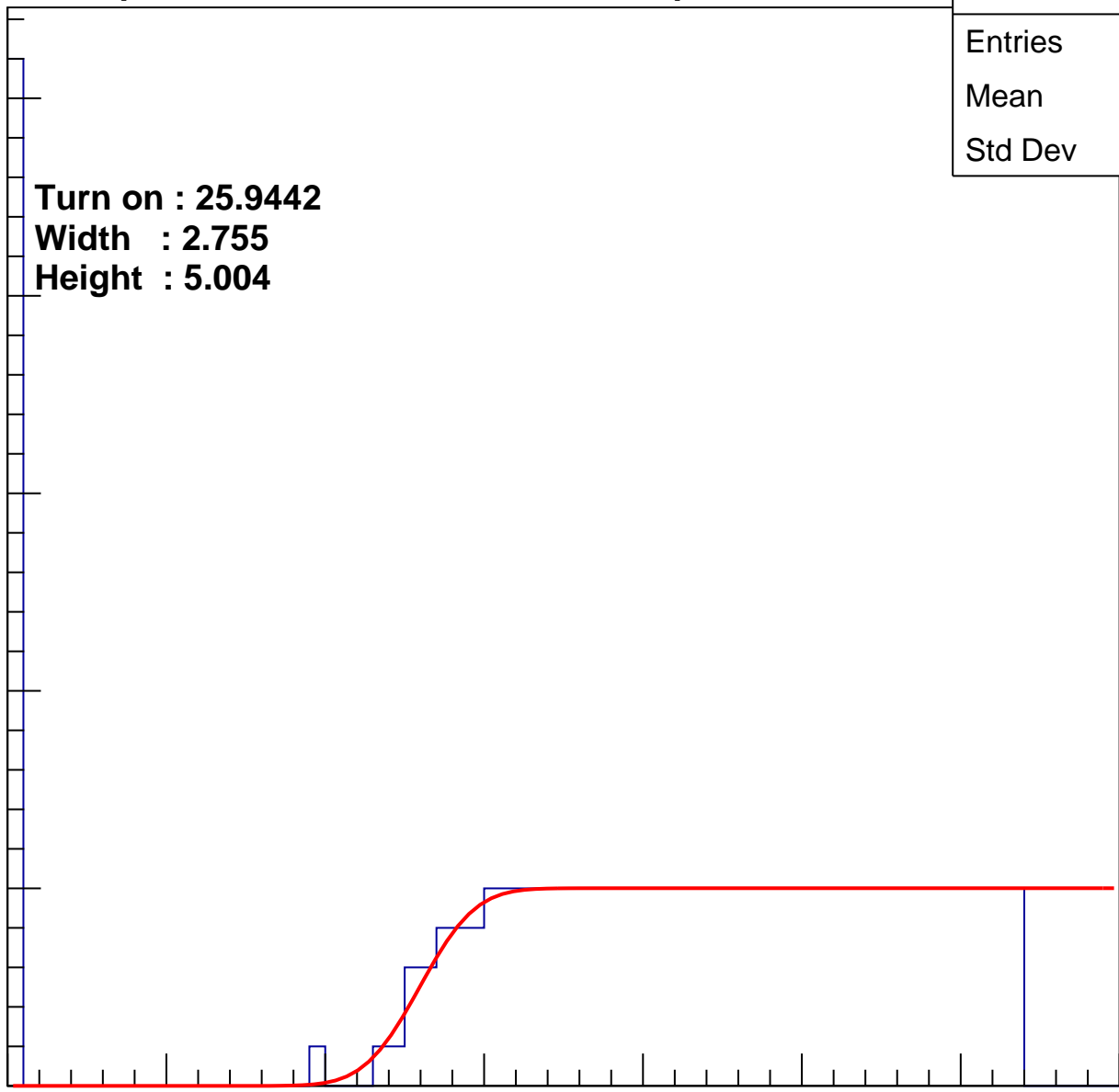
**Height : 5.004**

Entry

25  
20  
15  
10  
5  
0

0 10 20 30 40 50 60 70

ampl



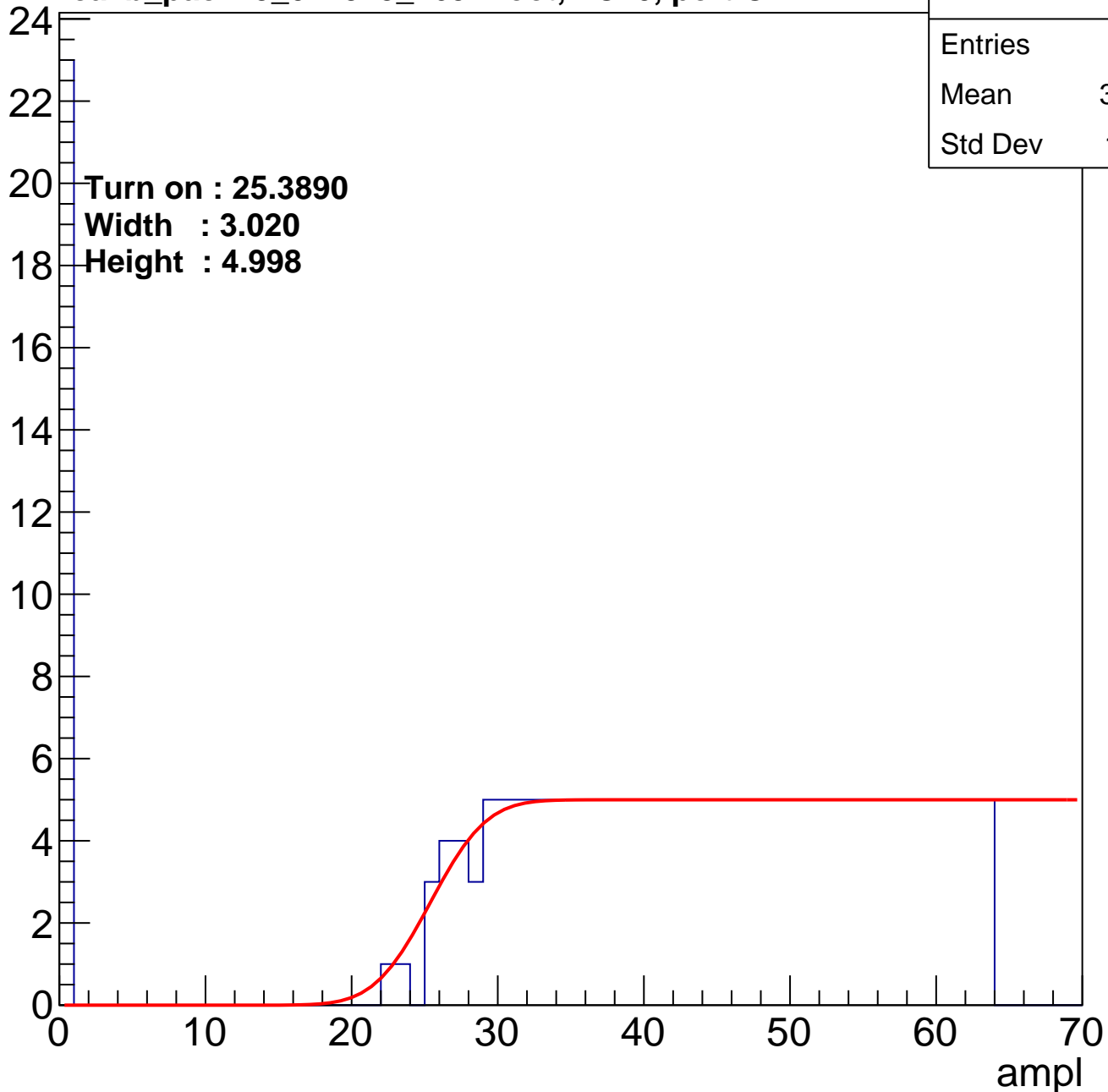


# B1L103S, U14-ch23

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	214
Mean	39.56
Std Dev	17.31

Entry



# B1L103S, U14-ch24

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	218
Mean	38.82
Std Dev	17.96

**Turn on : 25.8456**

**Width : 3.293**

**Height : 5.017**

Entry

25

20

15

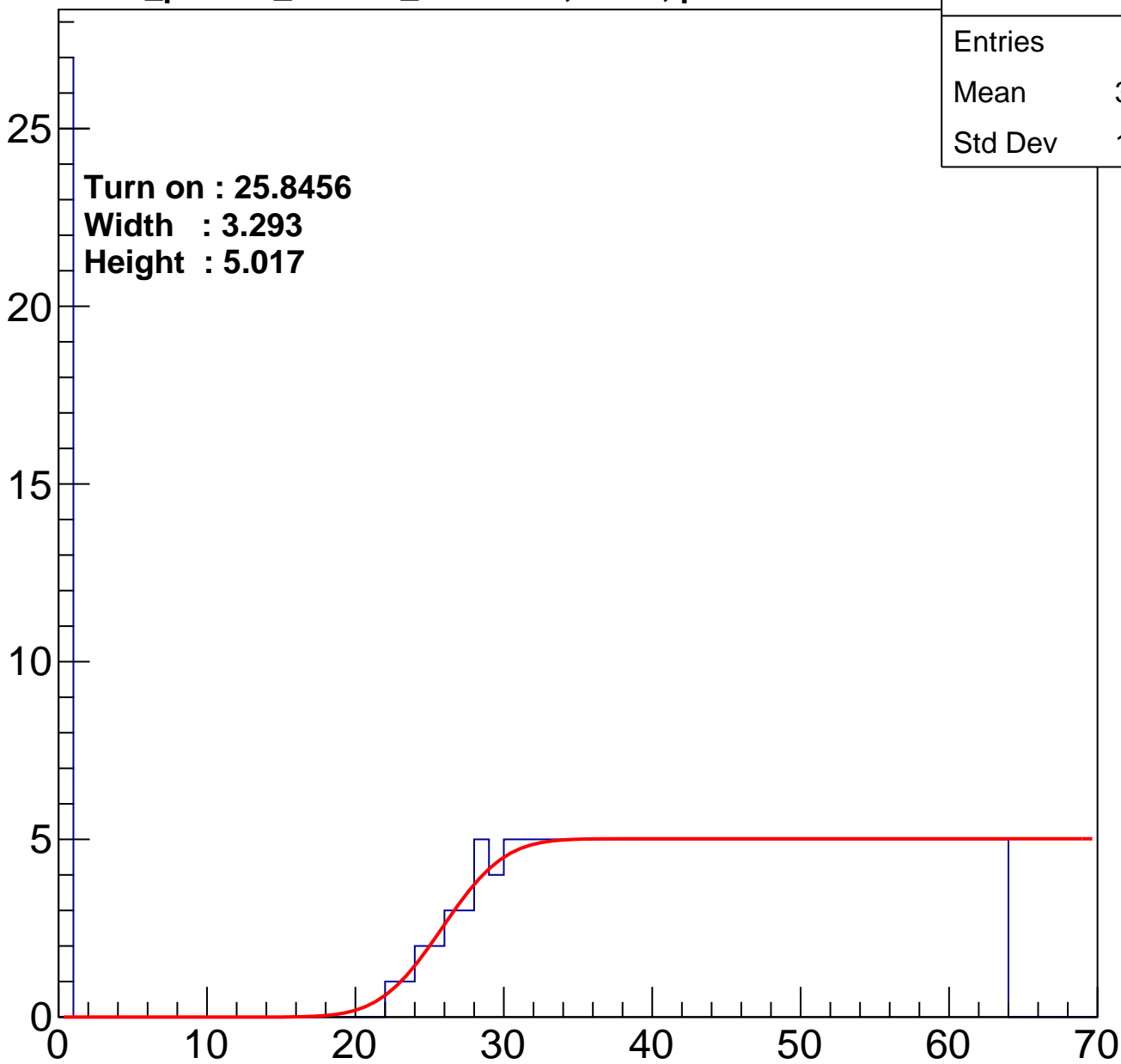
10

5

0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U14-ch25

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	210
Mean	39.4
Std Dev	17.97

**Turn on : 27.6974**

**Width : 2.334**

**Height : 5.004**

Entry

25

20

15

10

5

0

ampl

0

10

20

30

40

50

60

70

# B1L103S, U14-ch26

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	220
Mean	38.23
Std Dev	18.58

**Turn on : 26.3271**

**Width : 3.213**

**Height : 5.021**

Entry

30

25

20

15

10

5

0

0

10

20

30

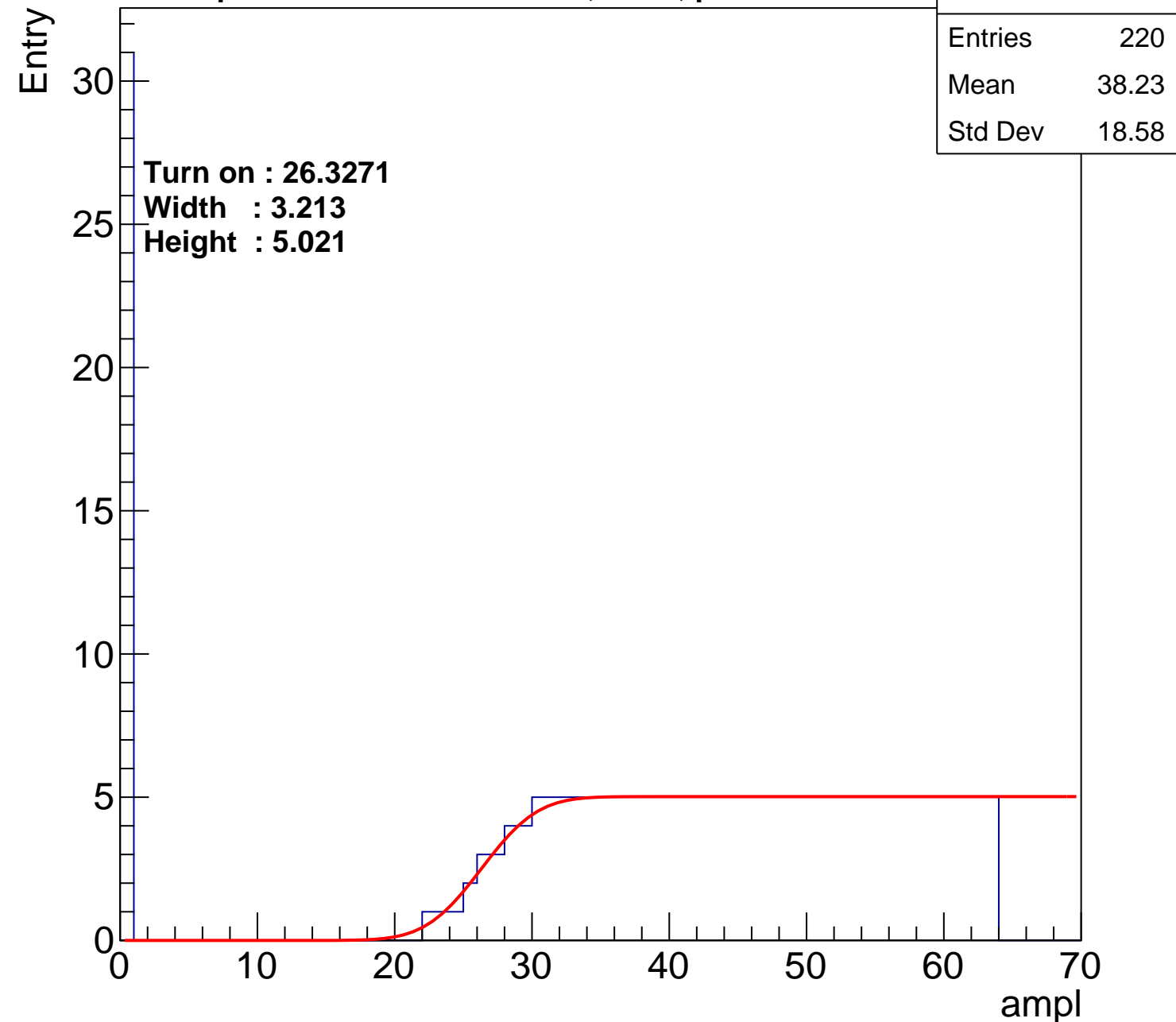
40

50

60

70

ampl



# B1L103S, U14-ch27

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	215
Mean	39.26
Std Dev	17.65

**Turn on : 25.9071**

**Width : 3.451**

**Height : 5.025**

Entry

25

20

15

10

5

0

0

10

20

30

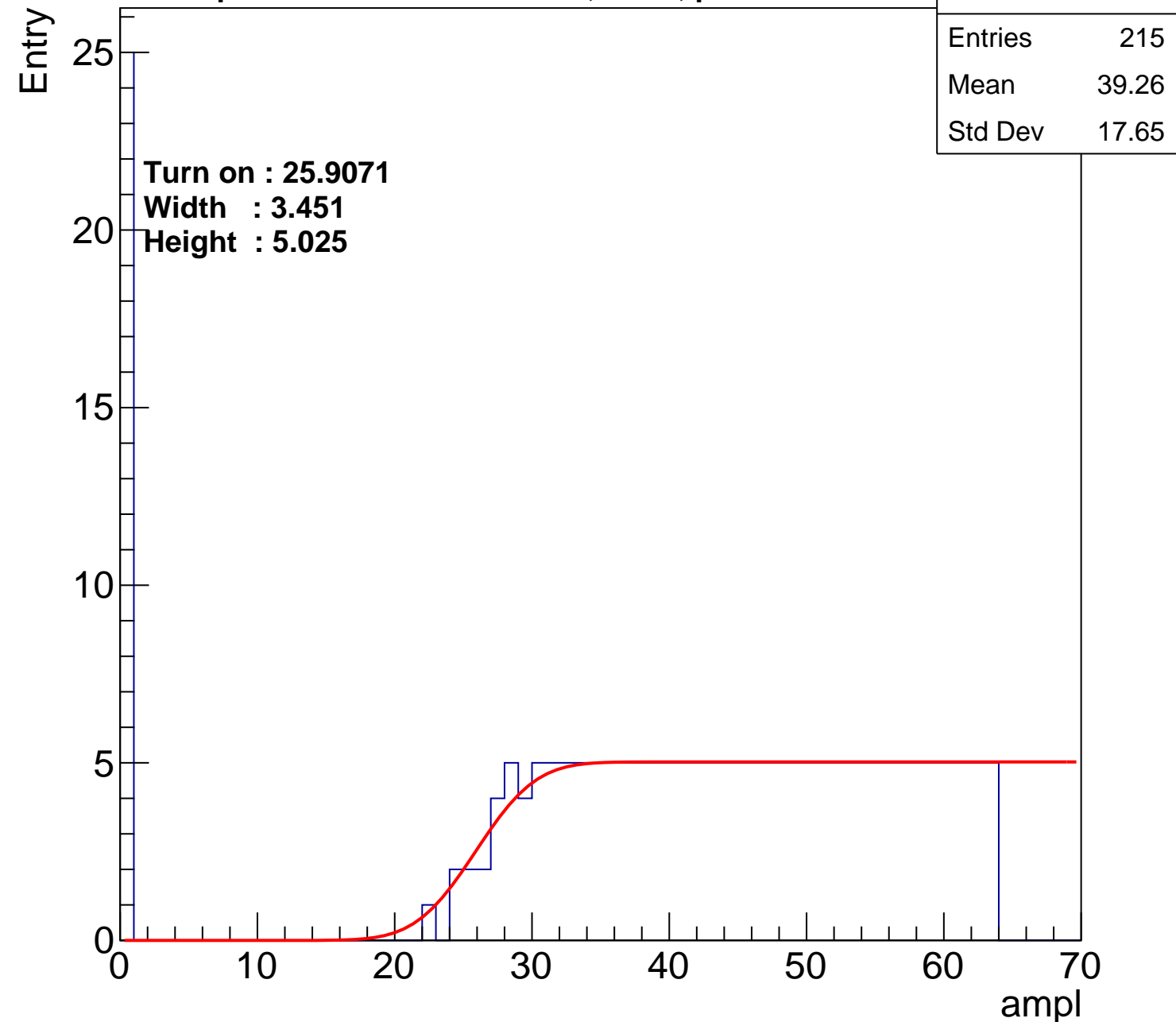
40

50

60

70

ampl



# B1L103S, U14-ch28

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	224
Mean	37.77
Std Dev	18.8

**Turn on : 26.0236**

**Width : 3.234**

**Height : 5.000**

Entry

30

25

20

15

10

5

0

0

10

20

30

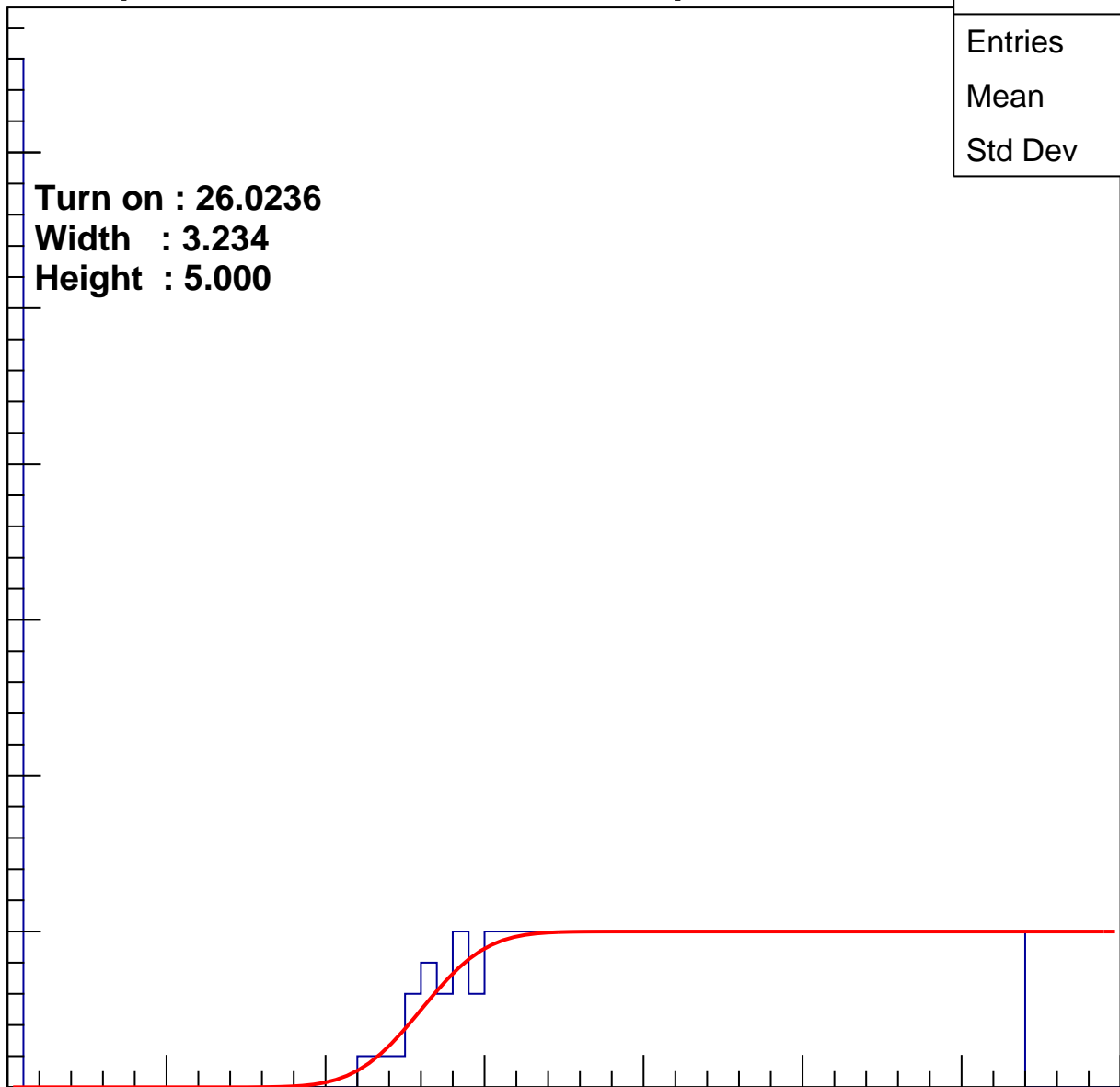
40

50

60

70

ampl



# B1L103S, U14-ch29

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	208
Mean	39.56
Std Dev	17.97

**Turn on : 28.2164**

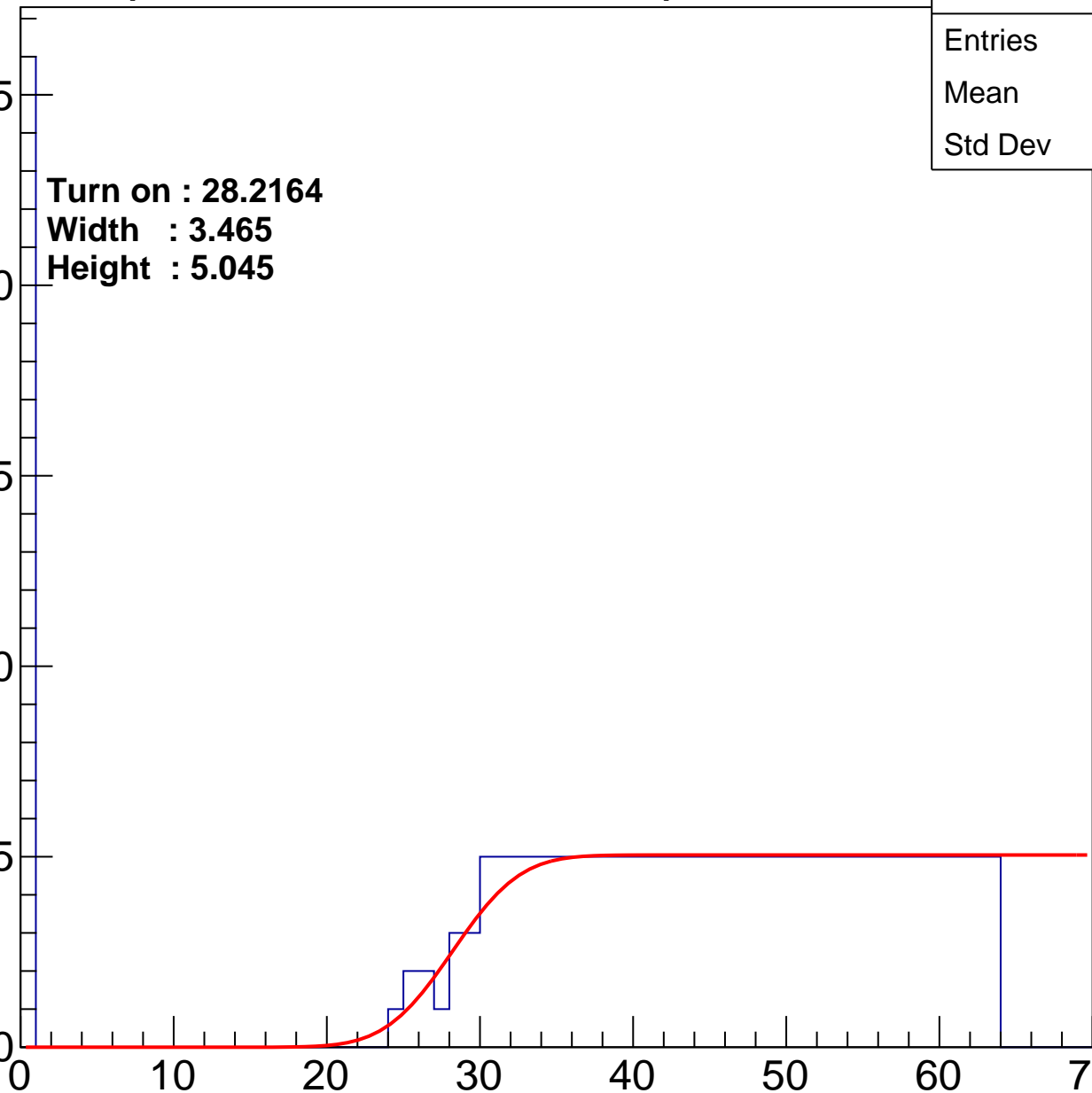
**Width : 3.465**

**Height : 5.045**

Entry

25  
20  
15  
10  
5  
0

ampl



# B1L103S, U14-ch30

calib\_packv5\_041523\_1651.root, FC#0, port C2

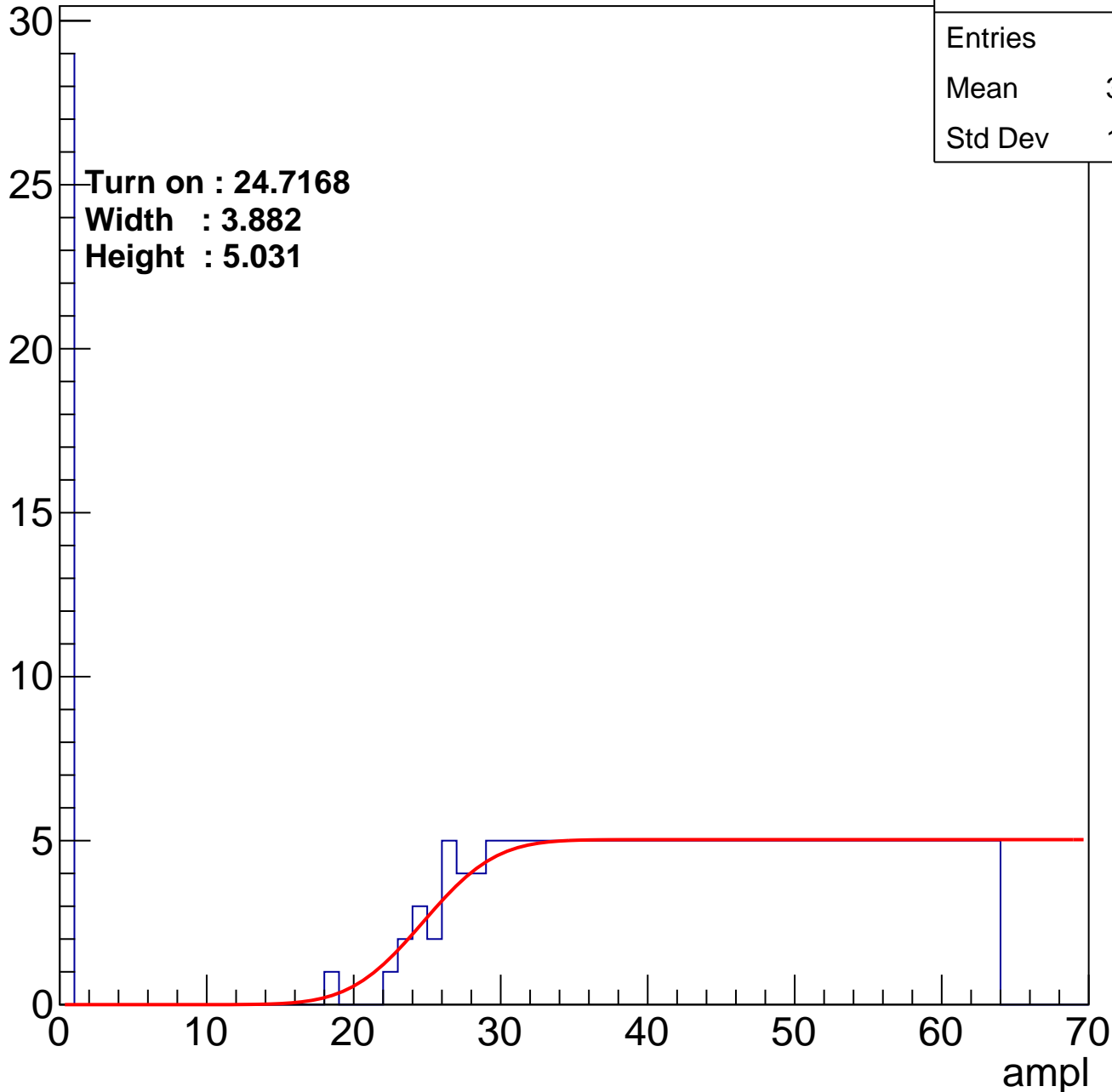
Entries	226
Mean	38.09
Std Dev	18.16

Turn on : 24.7168

Width : 3.882

Height : 5.031

Entry





# B1L103S, U14-ch31

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	220
Mean	37.99
Std Dev	18.9

**Turn on : 25.2953**

**Width : 4.277**

**Height : 5.035**

Entry

30

25

20

15

10

5

0

0

10

20

30

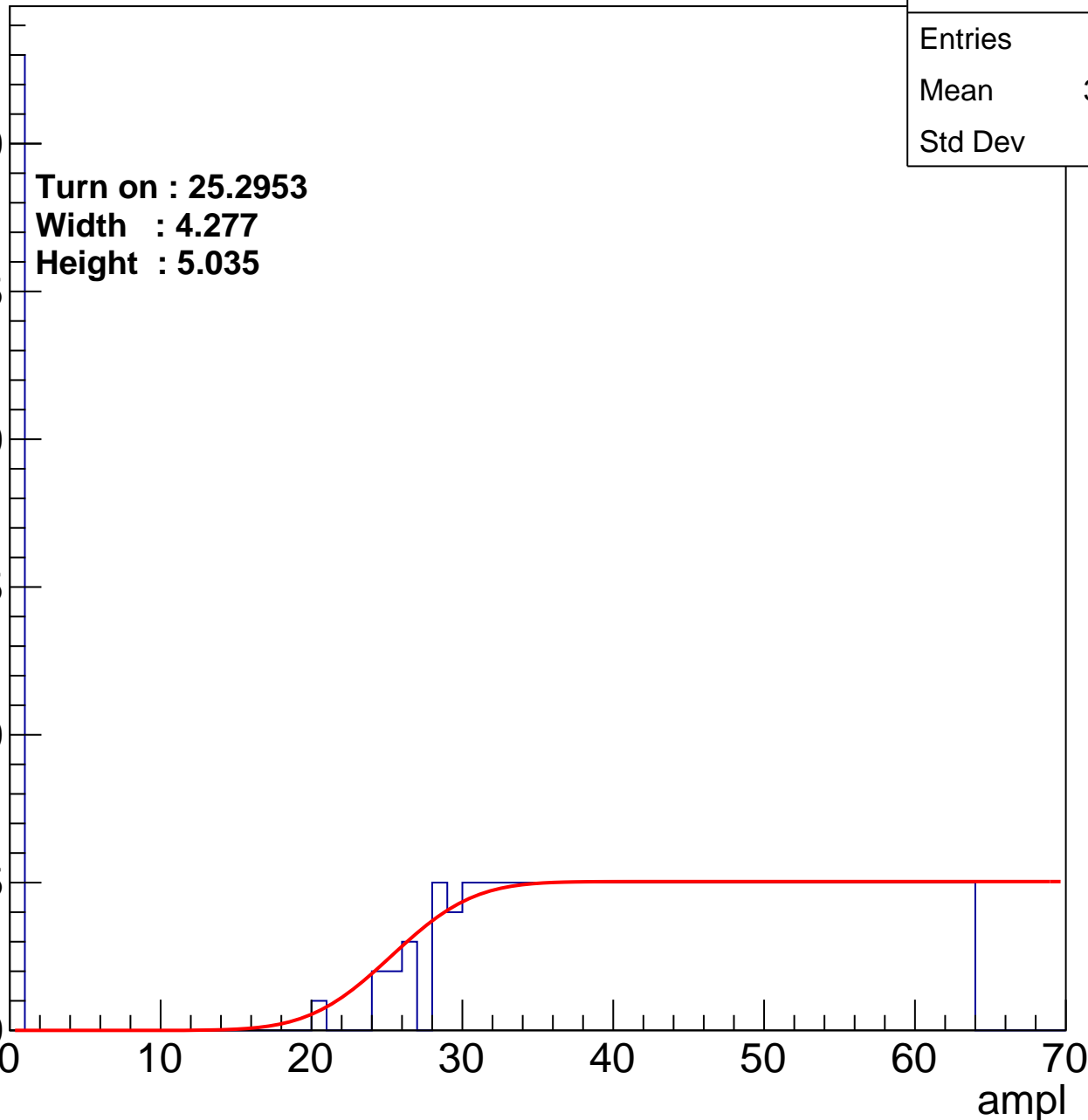
40

50

60

70

ampl



# B1L103S, U14-ch32

calib\_packv5\_041523\_1651.root, FC#0, port C2

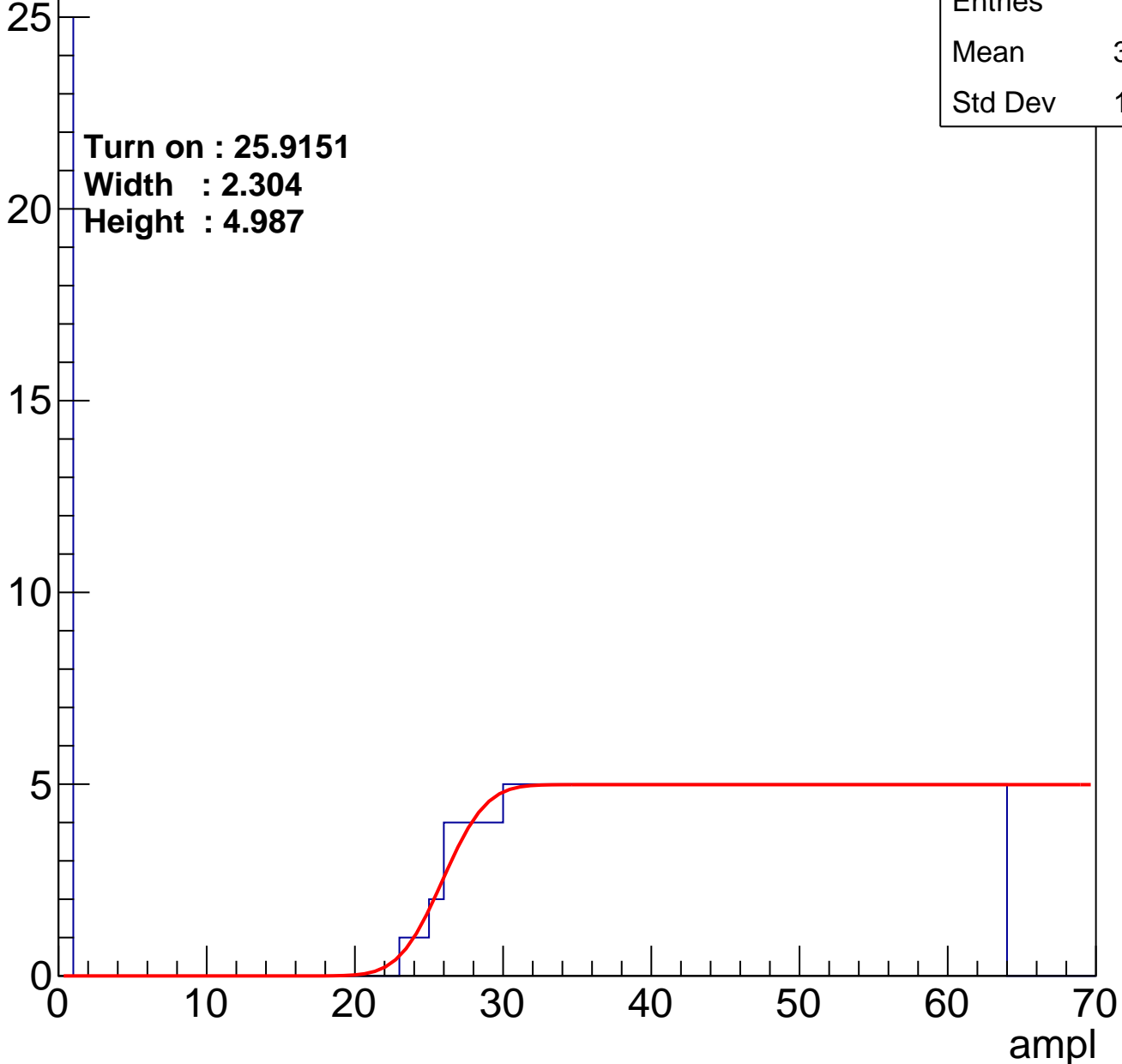
Entries	215
Mean	39.27
Std Dev	17.65

**Turn on : 25.9151**

**Width : 2.304**

**Height : 4.987**

Entry



# B1L103S, U14-ch33

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	215
Mean	39
Std Dev	18.02

**Turn on : 27.0351**

**Width : 3.652**

**Height : 5.050**

Entry

25

20

15

10

5

0

0

10

20

30

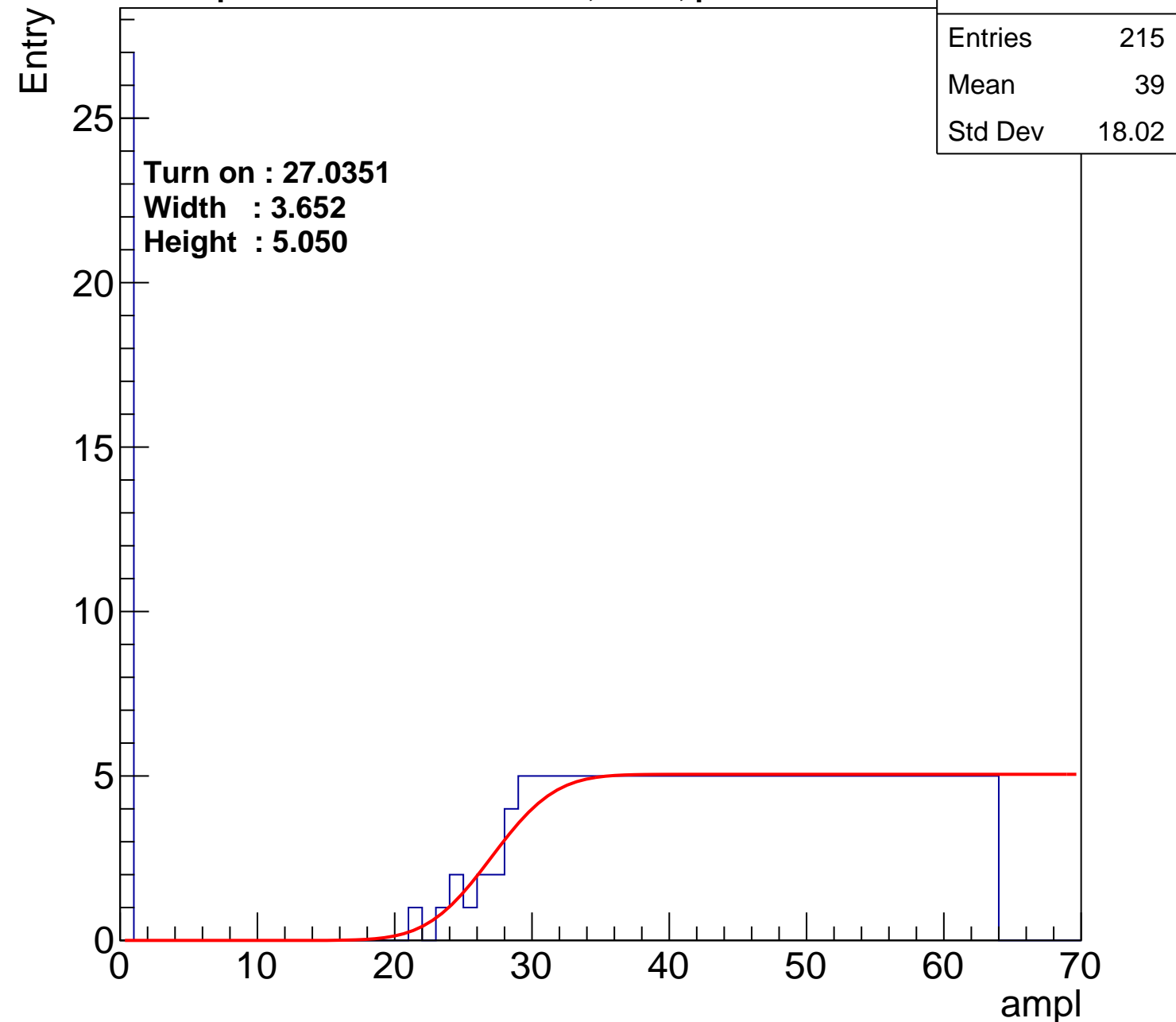
40

50

60

70

ampl



# B1L103S, U14-ch34

calib\_packv5\_041523\_1651.root, FC#0, port C2

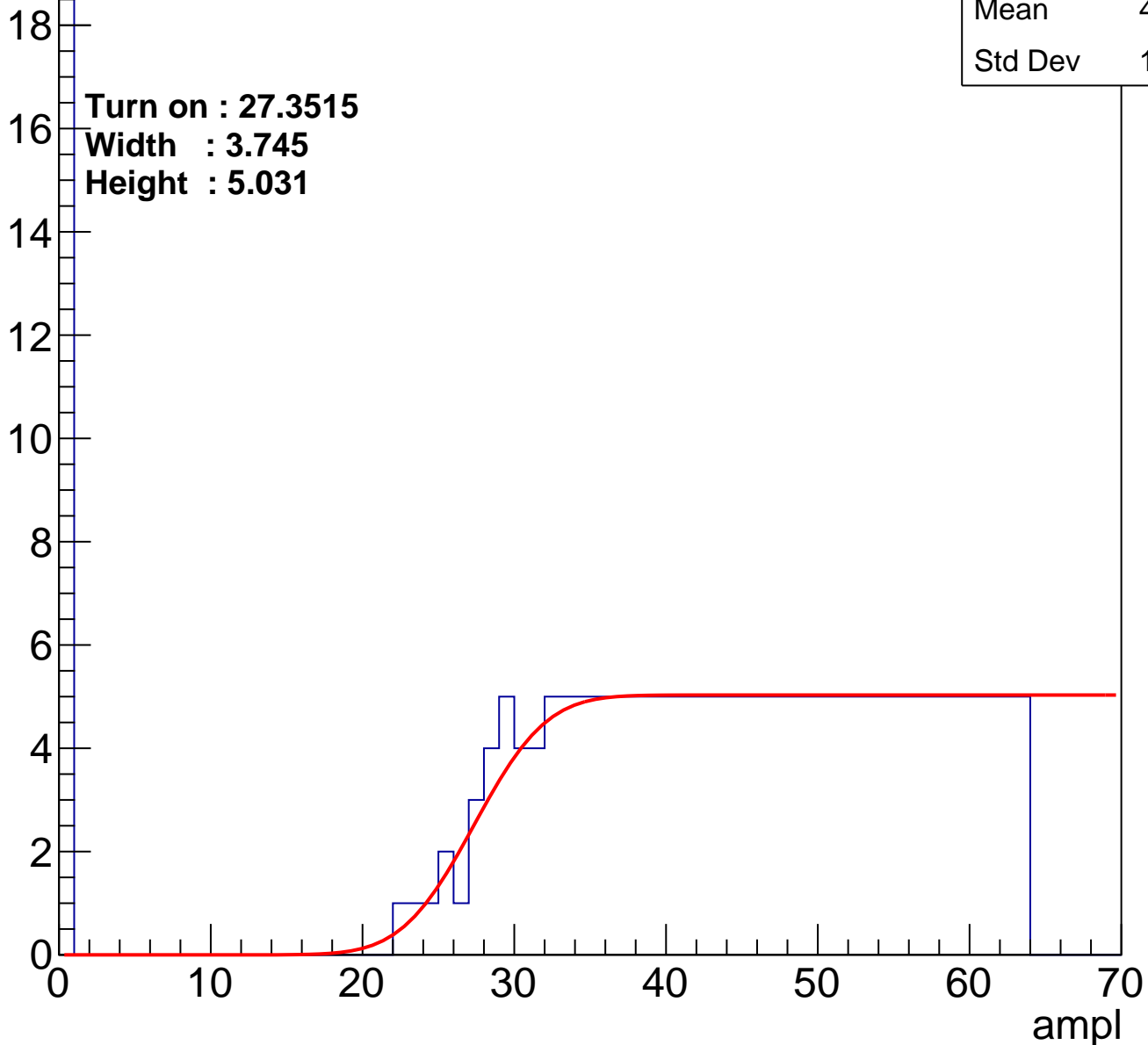
Entries	205
Mean	40.62
Std Dev	16.66

**Turn on : 27.3515**

**Width : 3.745**

**Height : 5.031**

Entry



# B1L103S, U14-ch35

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	219
Mean	38.73
Std Dev	17.96

**Turn on : 25.6081**

**Width : 3.491**

**Height : 5.003**

Entry

25

20

15

10

5

0

0

10

20

30

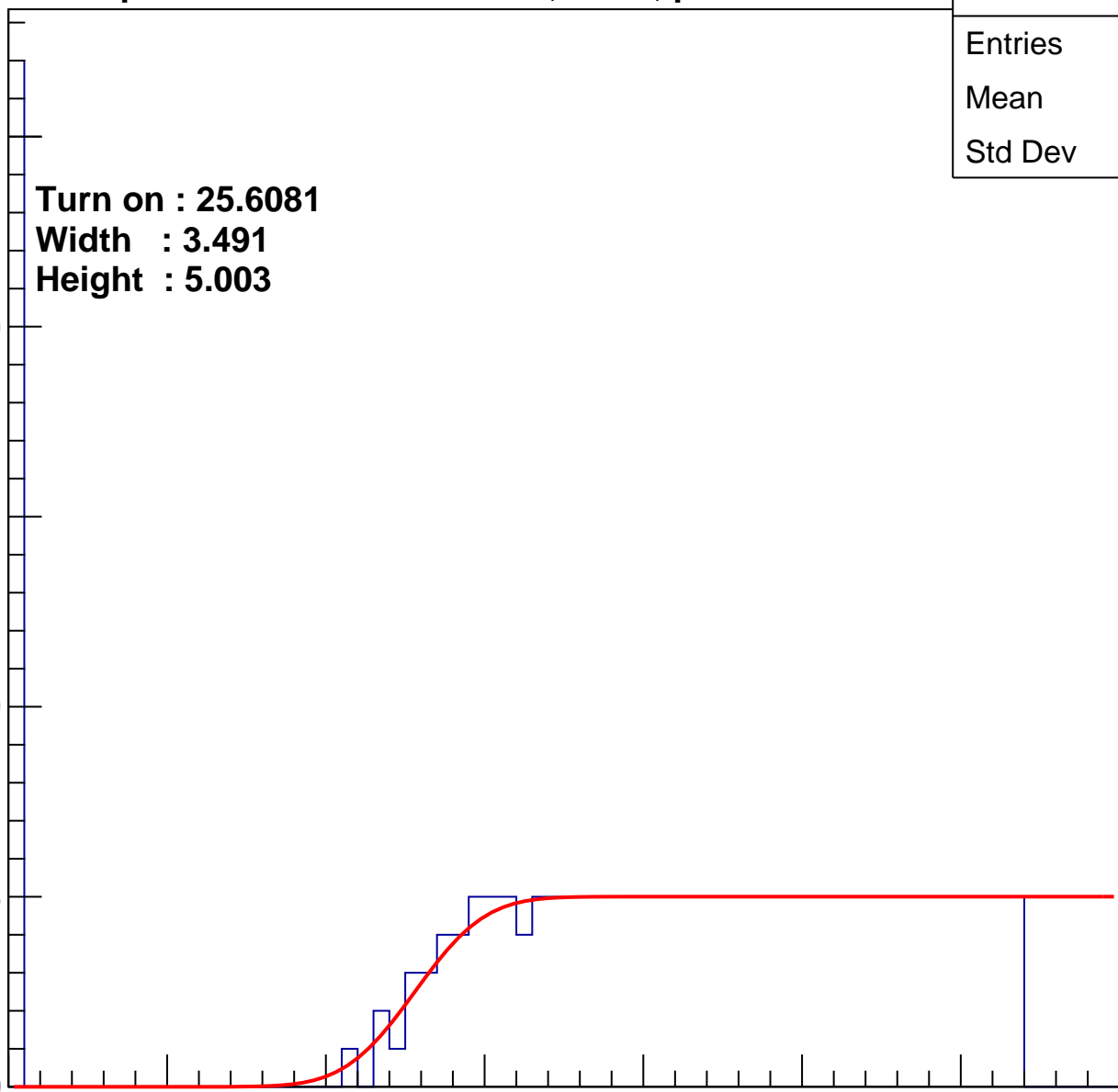
40

50

60

70

ampl



# B1L103S, U14-ch36

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	218
Mean	38.67
Std Dev	18.15

**Turn on : 26.6298**

**Width : 4.044**

**Height : 5.046**

Entry

25

20

15

10

5

0

0

10

20

30

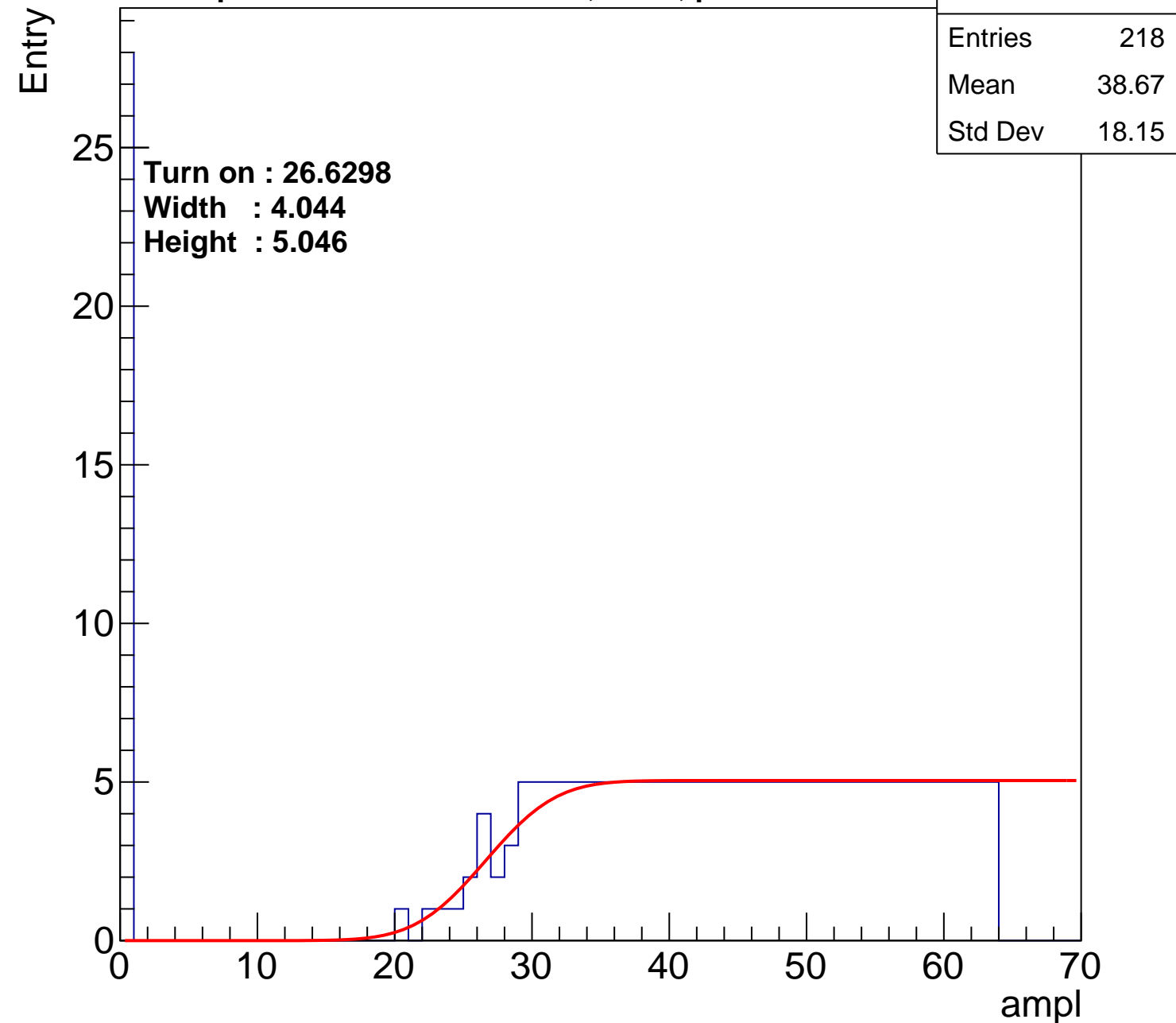
40

50

60

70

ampl



# B1L103S, U14-ch37

calib\_packv5\_041523\_1651.root, FC#0, port C2

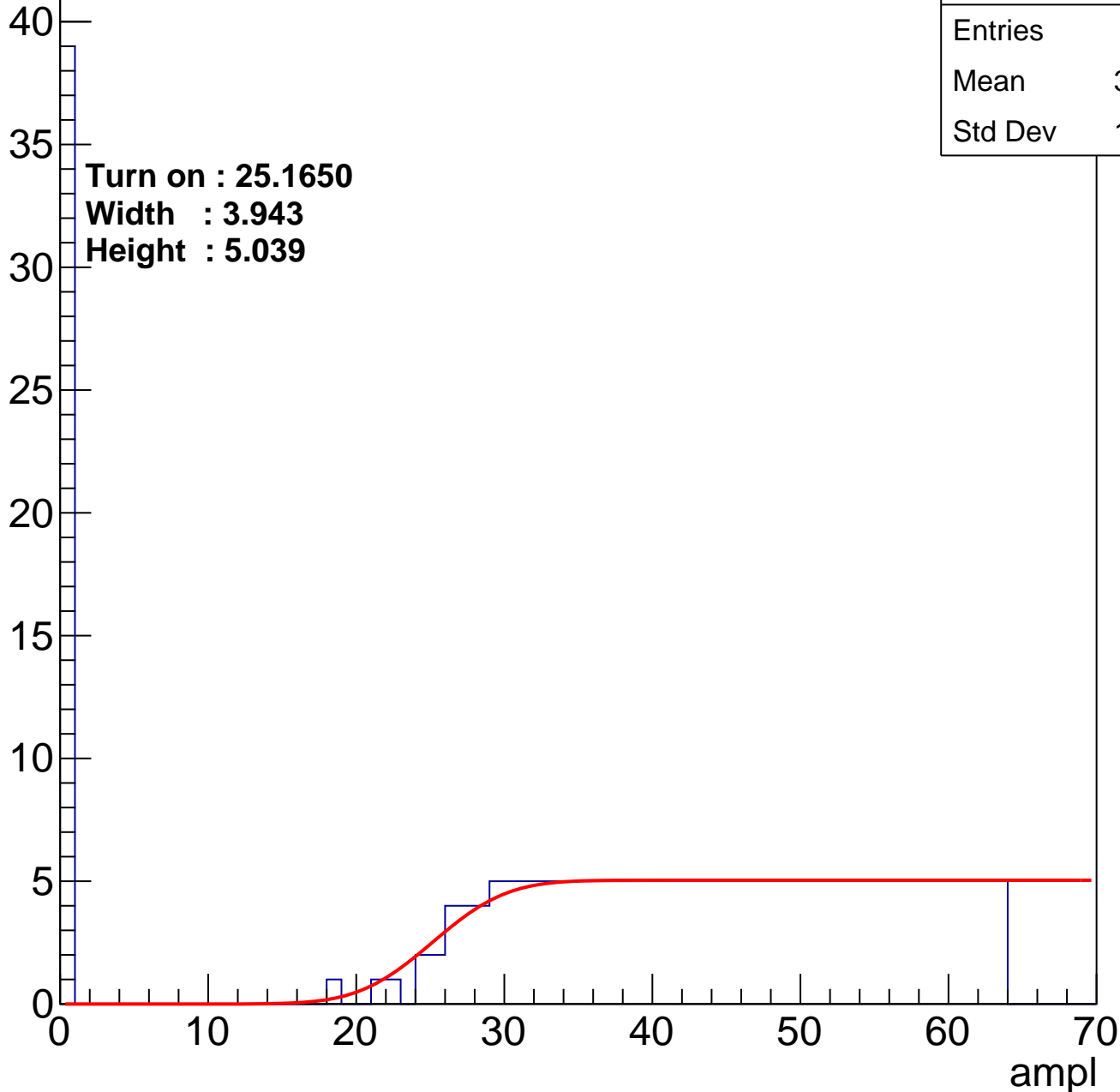
Entries	233
Mean	36.62
Std Dev	19.44

**Turn on : 25.1650**

**Width : 3.943**

**Height : 5.039**

Entry



# B1L103S, U14-ch38

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	223
Mean	39.26
Std Dev	16.71

**Turn on : 22.9316**

**Width : 1.779**

**Height : 4.940**

Entry

20  
18  
16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U14-ch39

calib\_packv5\_041523\_1651.root, FC#0, port C2

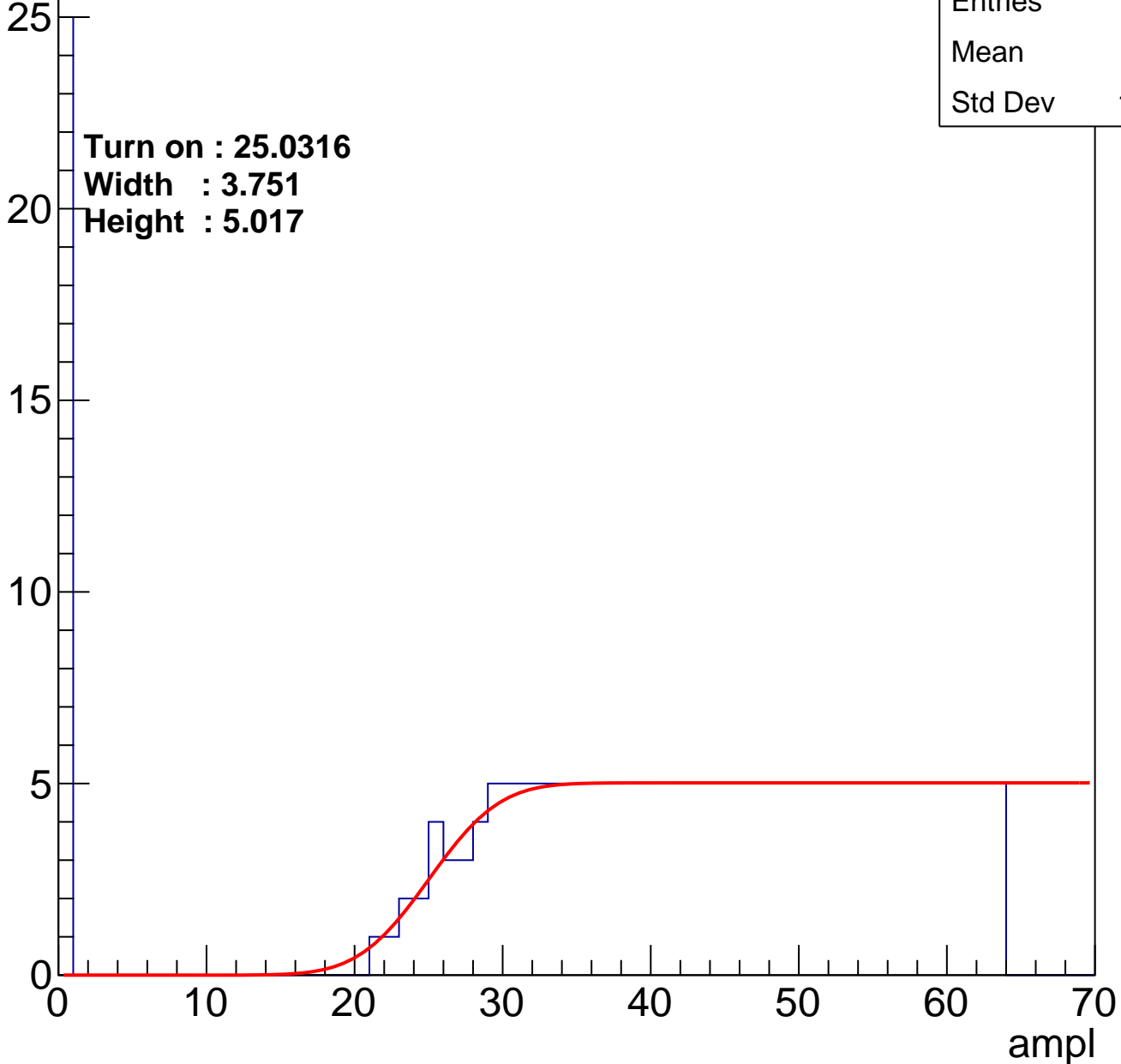
Entries	220
Mean	38.9
Std Dev	17.61

Turn on : 25.0316

Width : 3.751

Height : 5.017

Entry



# B1L103S, U14-ch40

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	221
Mean	38.83
Std Dev	17.77

**Turn on : 25.1515**

**Width : 3.307**

**Height : 5.007**

Entry

25

20

15

10

5

0

0

10

20

30

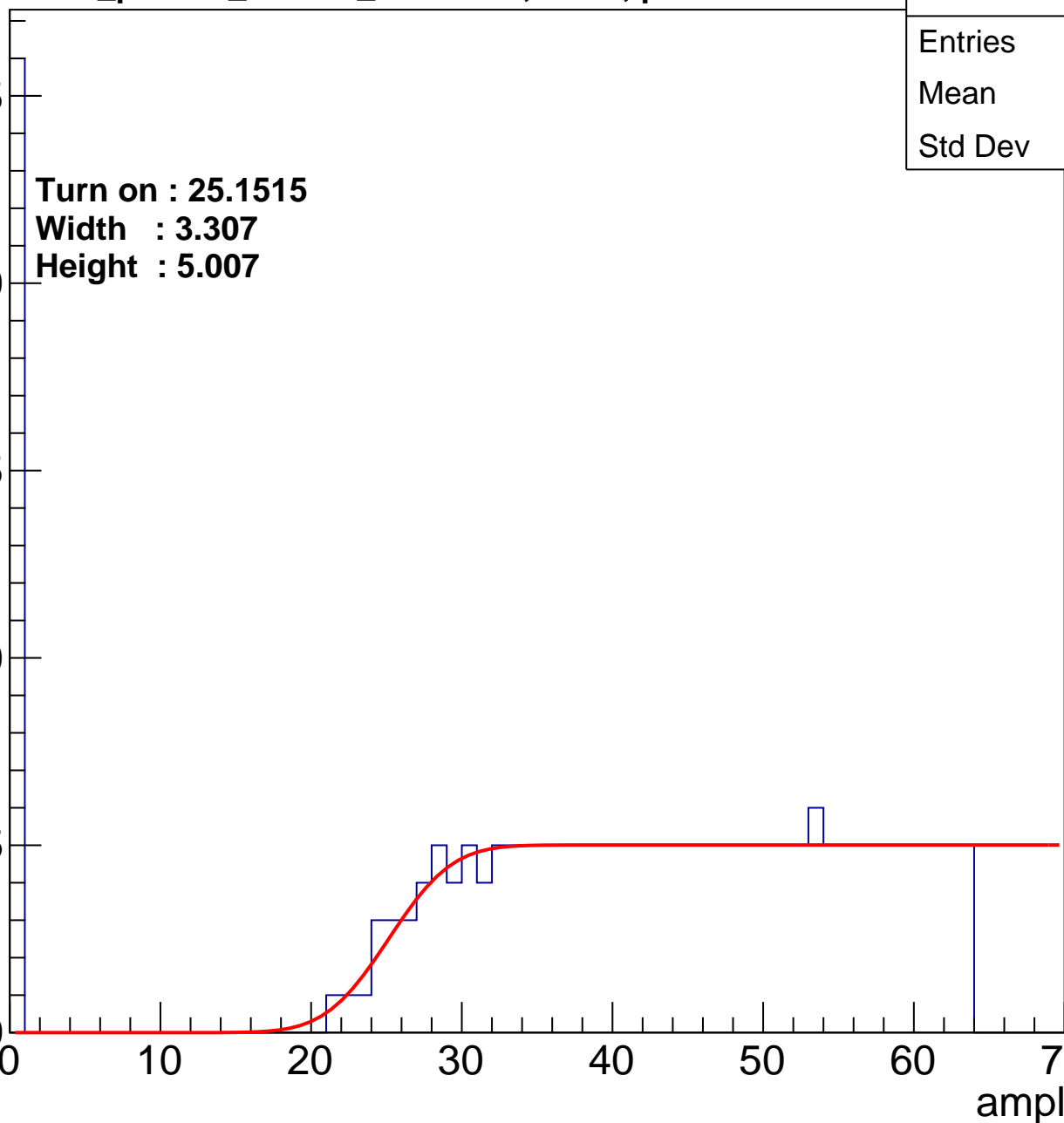
40

50

60

70

ampl



# B1L103S, U14-ch41

calib\_packv5\_041523\_1651.root, FC#0, port C2

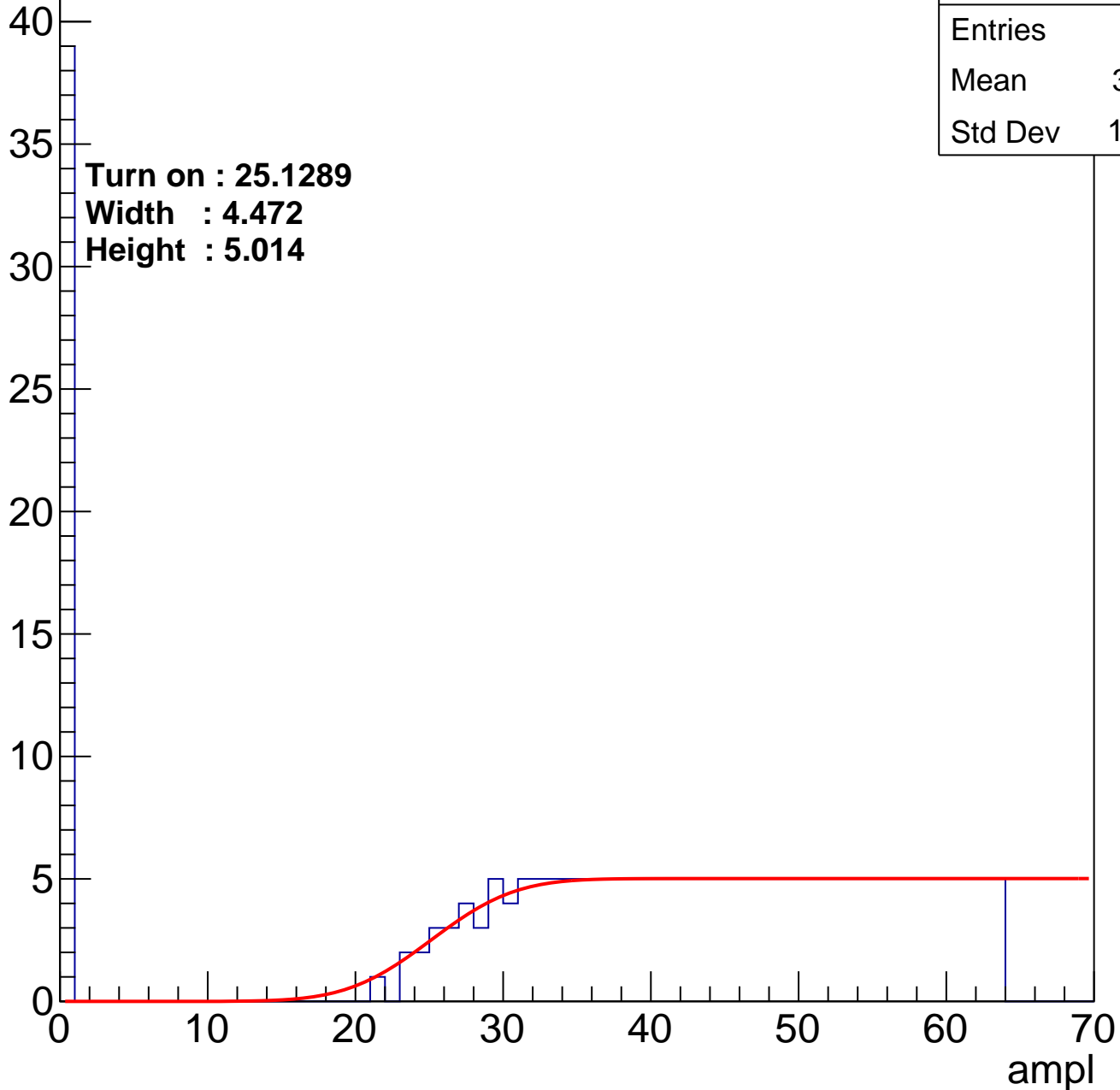
Entries	231
Mean	36.71
Std Dev	19.49

**Turn on : 25.1289**

**Width : 4.472**

**Height : 5.014**

Entry



# B1L103S, U14-ch42

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	218
Mean	38.8
Std Dev	17.98

**Turn on : 26.2056**

**Width : 3.453**

**Height : 5.034**

Entry

25

20

15

10

5

0

0

10

20

30

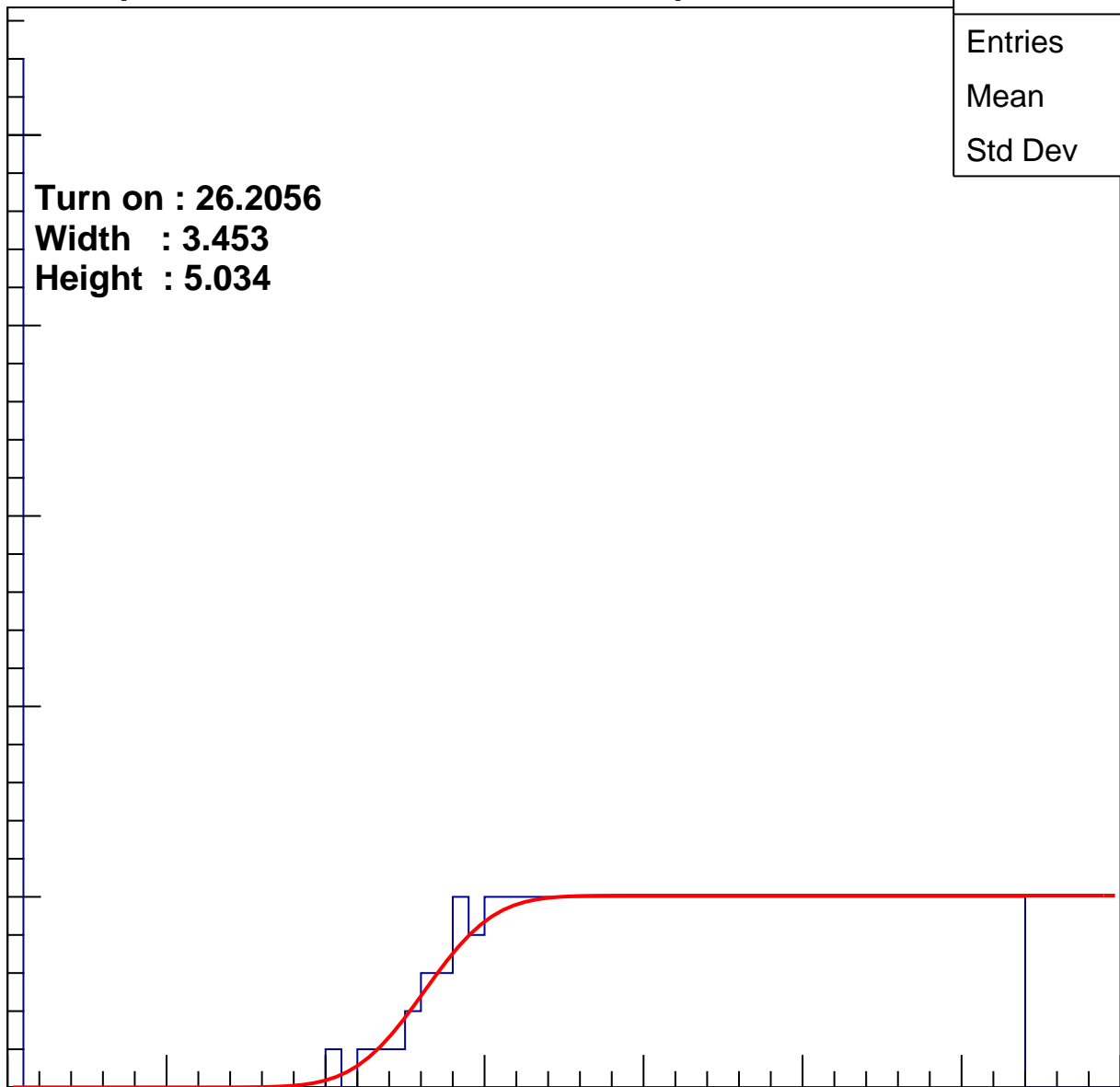
40

50

60

70

ampl



# B1L103S, U14-ch43

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	217
Mean	39.02
Std Dev	17.79

**Turn on : 25.7068**

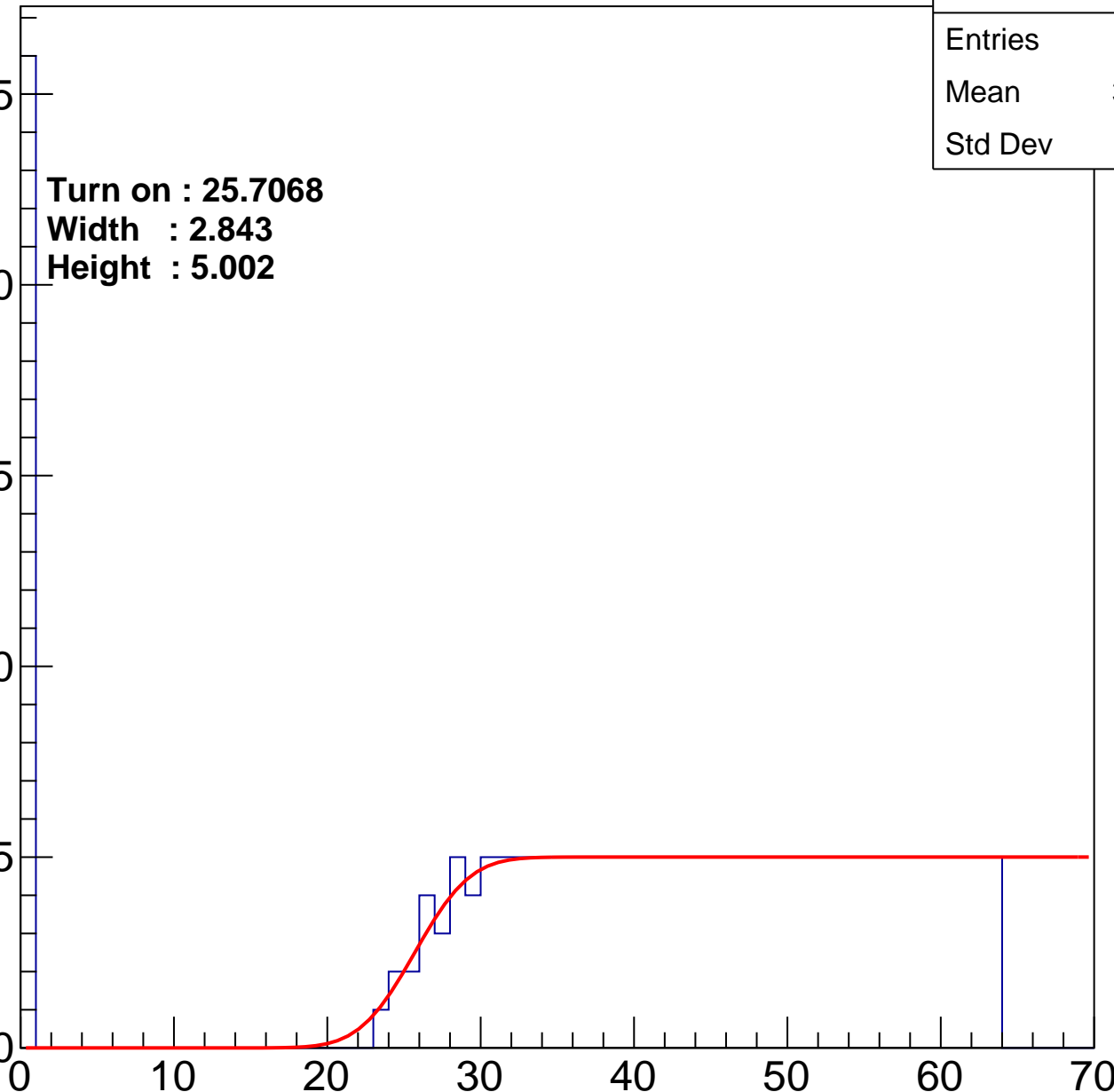
**Width : 2.843**

**Height : 5.002**

Entry

25  
20  
15  
10  
5  
0

ampl



# B1L103S, U14-ch44

calib\_packv5\_041523\_1651.root, FC#0, port C2

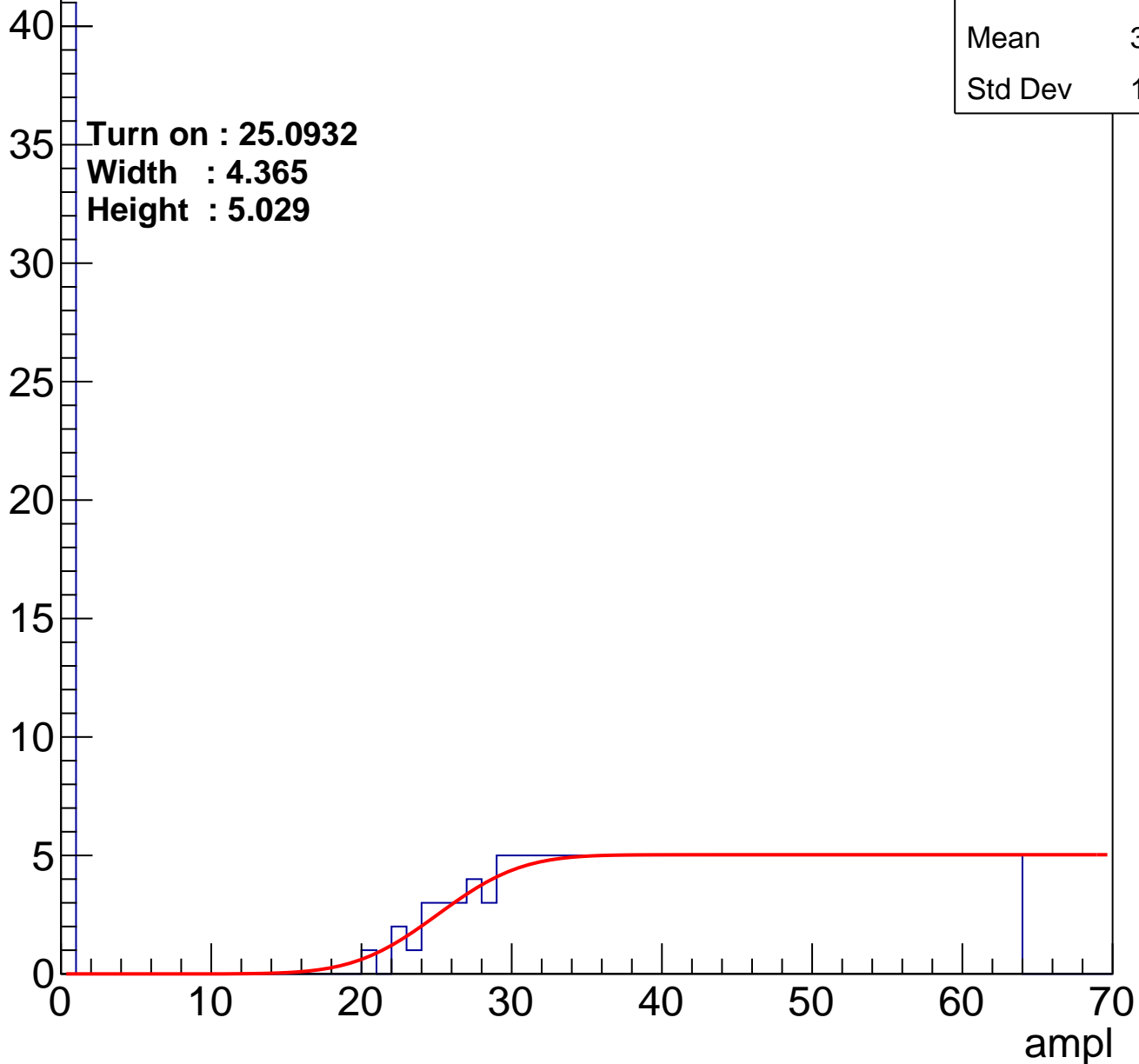
Entries	236
Mean	36.25
Std Dev	19.63

Turn on : 25.0932

Width : 4.365

Height : 5.029

Entry



# B1L103S, U14-ch45

calib\_packv5\_041523\_1651.root, FC#0, port C2

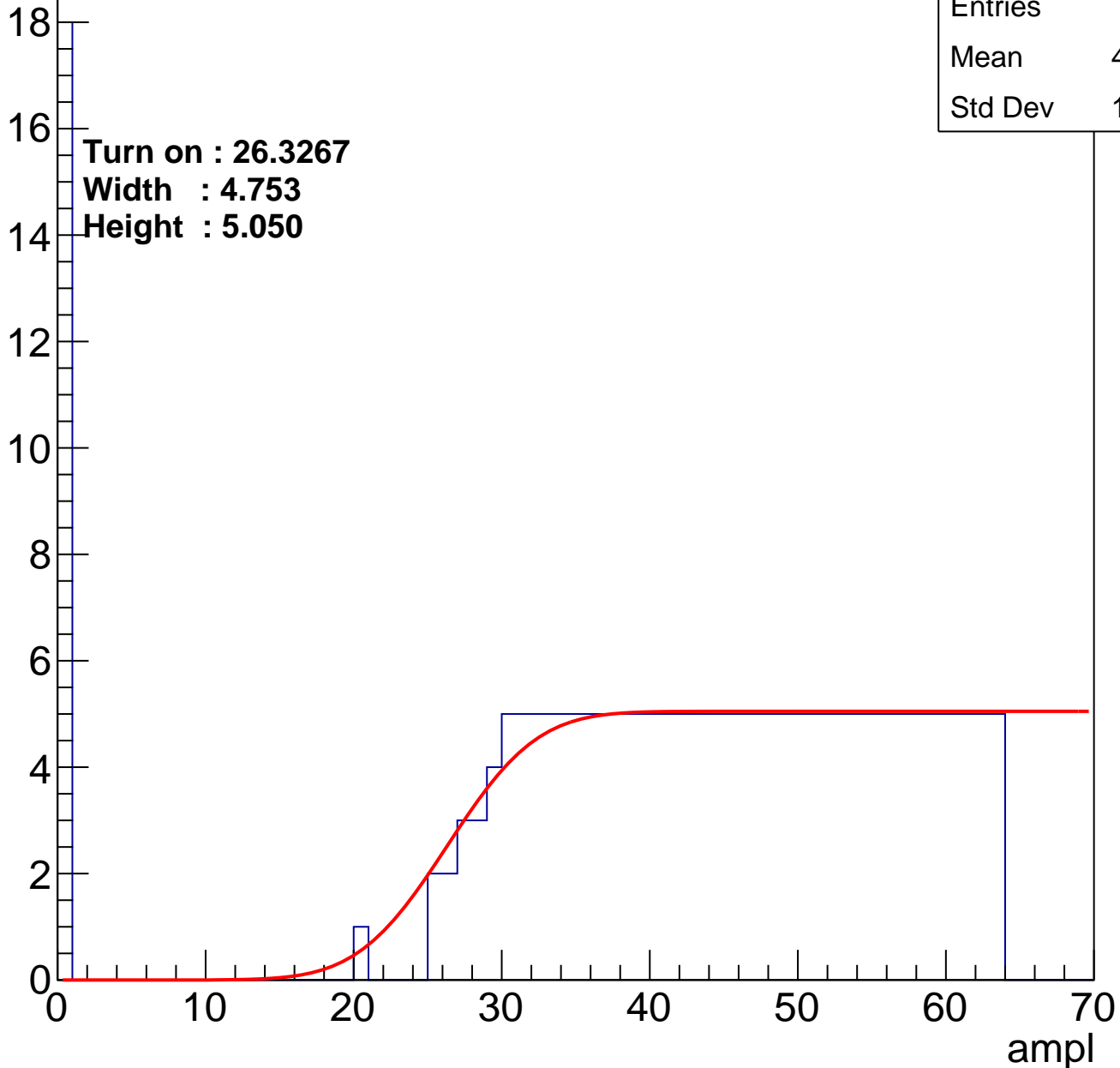
Entries	203
Mean	40.93
Std Dev	16.44

**Turn on : 26.3267**

**Width : 4.753**

**Height : 5.050**

Entry



# B1L103S, U14-ch46

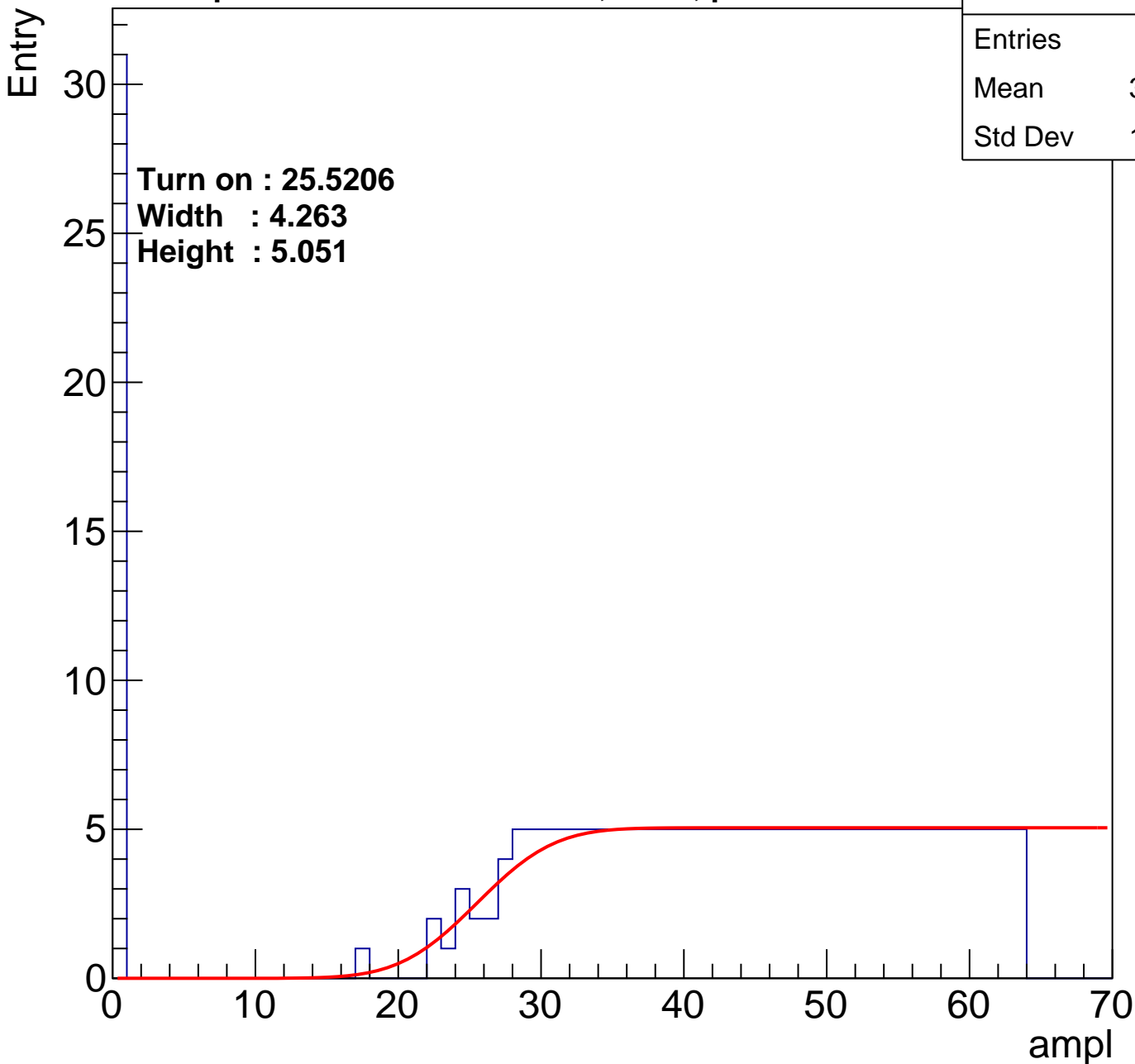
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	226
Mean	37.86
Std Dev	18.48

Turn on : 25.5206

Width : 4.263

Height : 5.051





# B1L103S, U14-ch47

calib\_packv5\_041523\_1651.root, FC#0, port C2

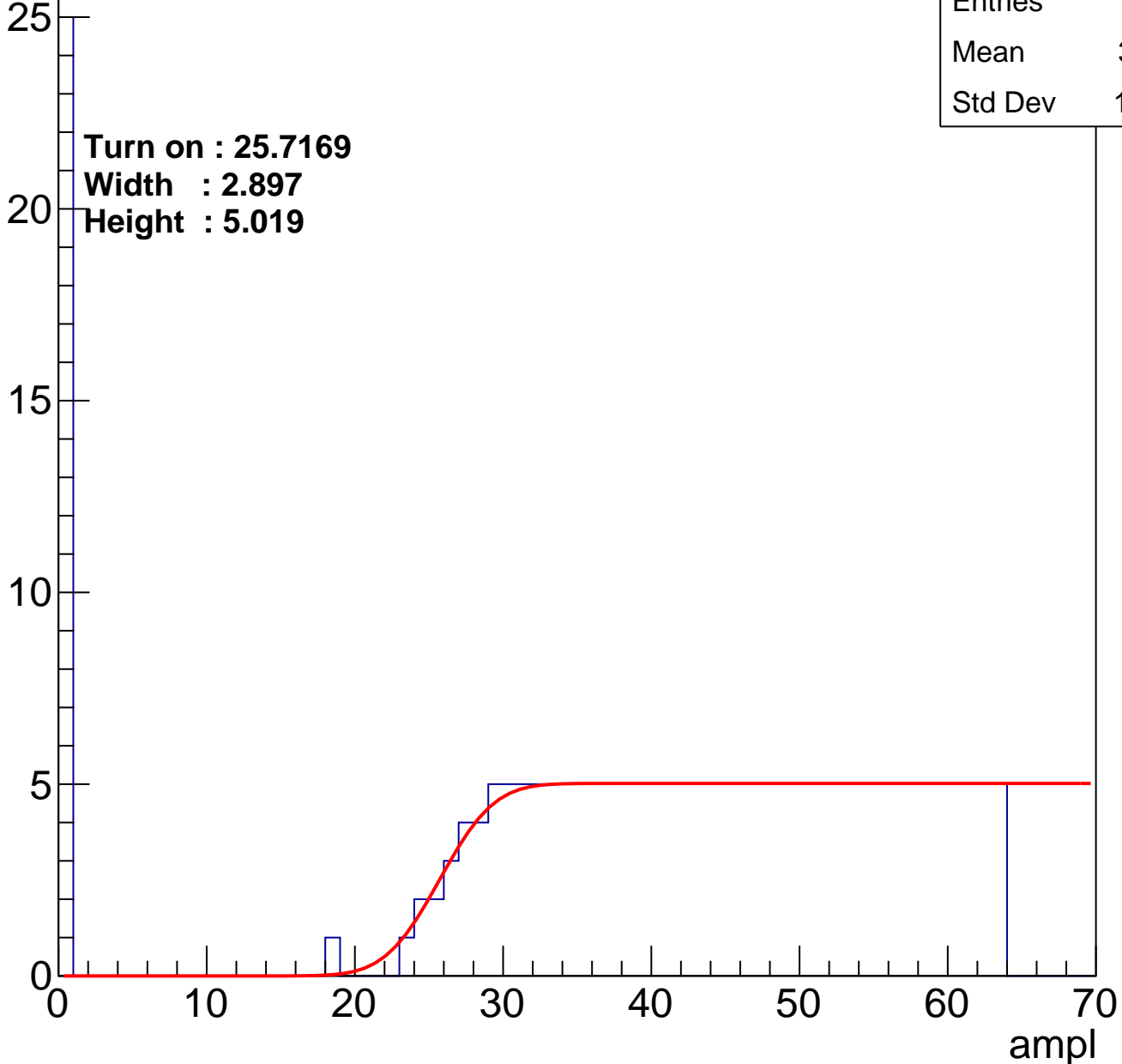
Entries	217
Mean	39.11
Std Dev	17.64

Turn on : 25.7169

Width : 2.897

Height : 5.019

Entry



# B1L103S, U14-ch48

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	219
Mean	38.84
Std Dev	17.81

**Turn on : 25.4524**

**Width : 4.458**

**Height : 5.040**

Entry

25

20

15

10

5

0

0

10

20

30

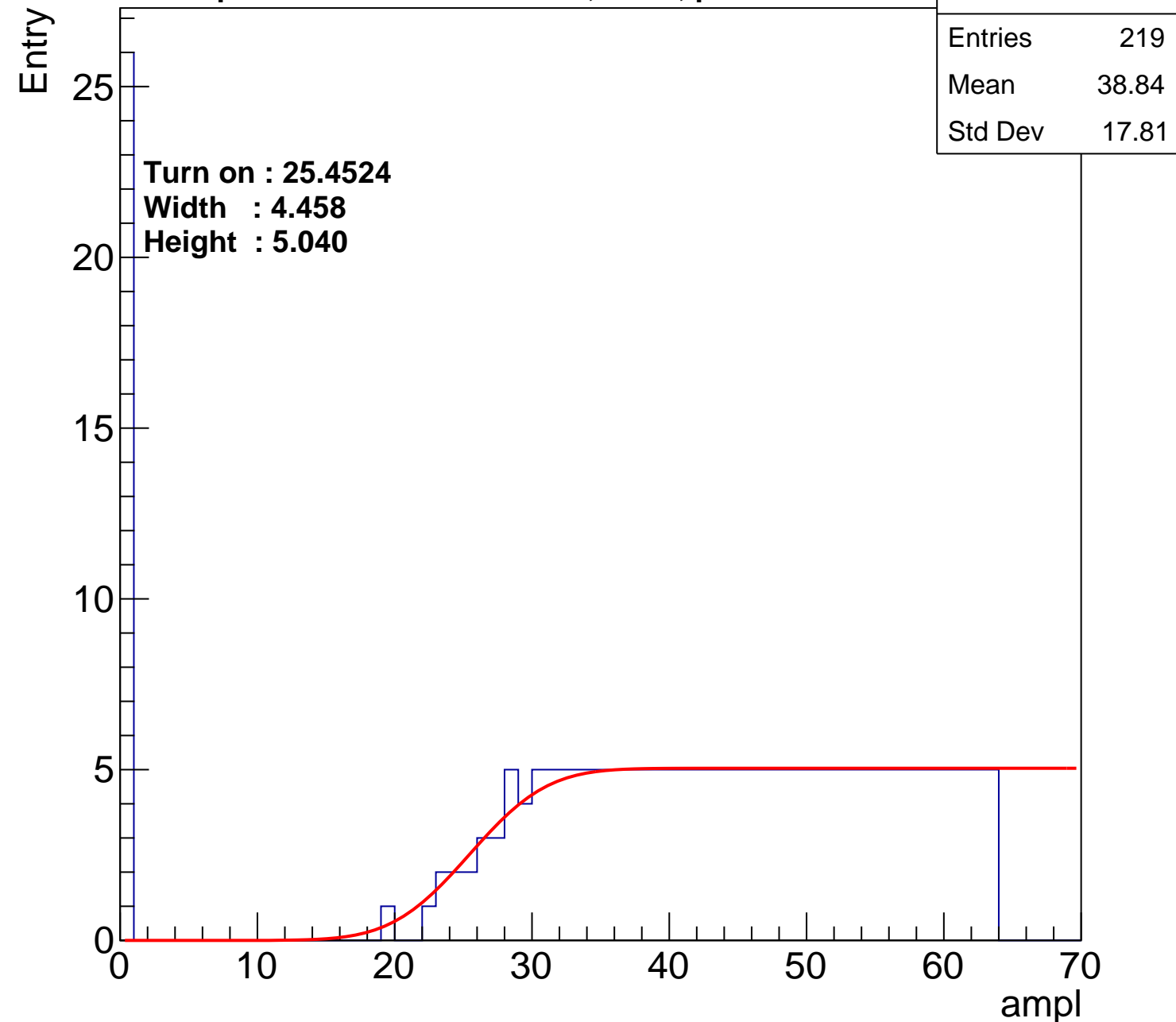
40

50

60

70

ampl



# B1L103S, U14-ch49

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	219
Mean	38.74
Std Dev	17.95

**Turn on : 25.7022**

**Width : 3.256**

**Height : 5.006**

Entry

25

20

15

10

5

0

0

10

20

30

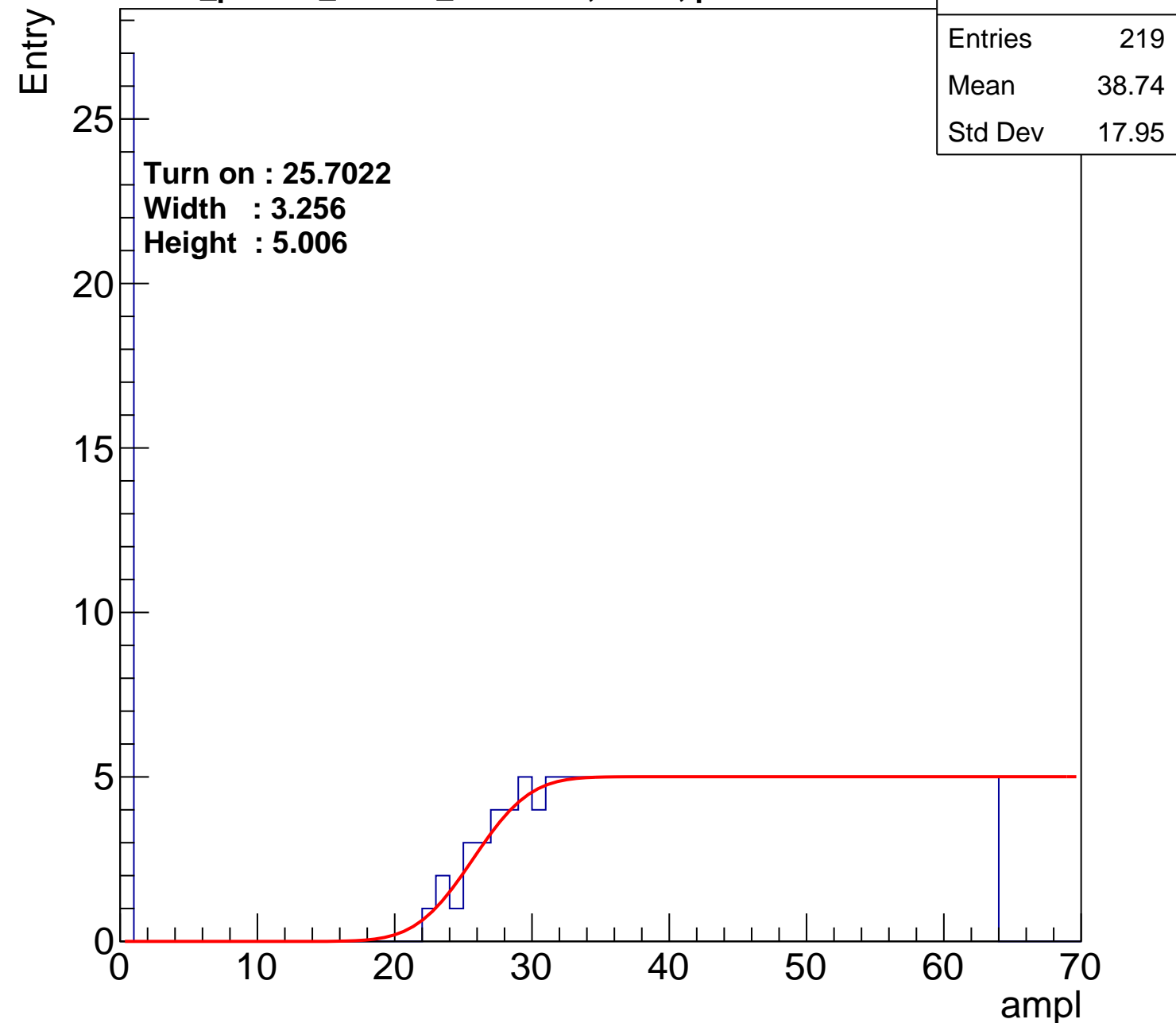
40

50

60

70

ampl



# B1L103S, U14-ch50

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	214
Mean	39.14
Std Dev	17.89

**Turn on : 26.7423**

**Width : 4.705**

**Height : 5.048**

Entry

25

20

15

10

5

0

0

10

20

30

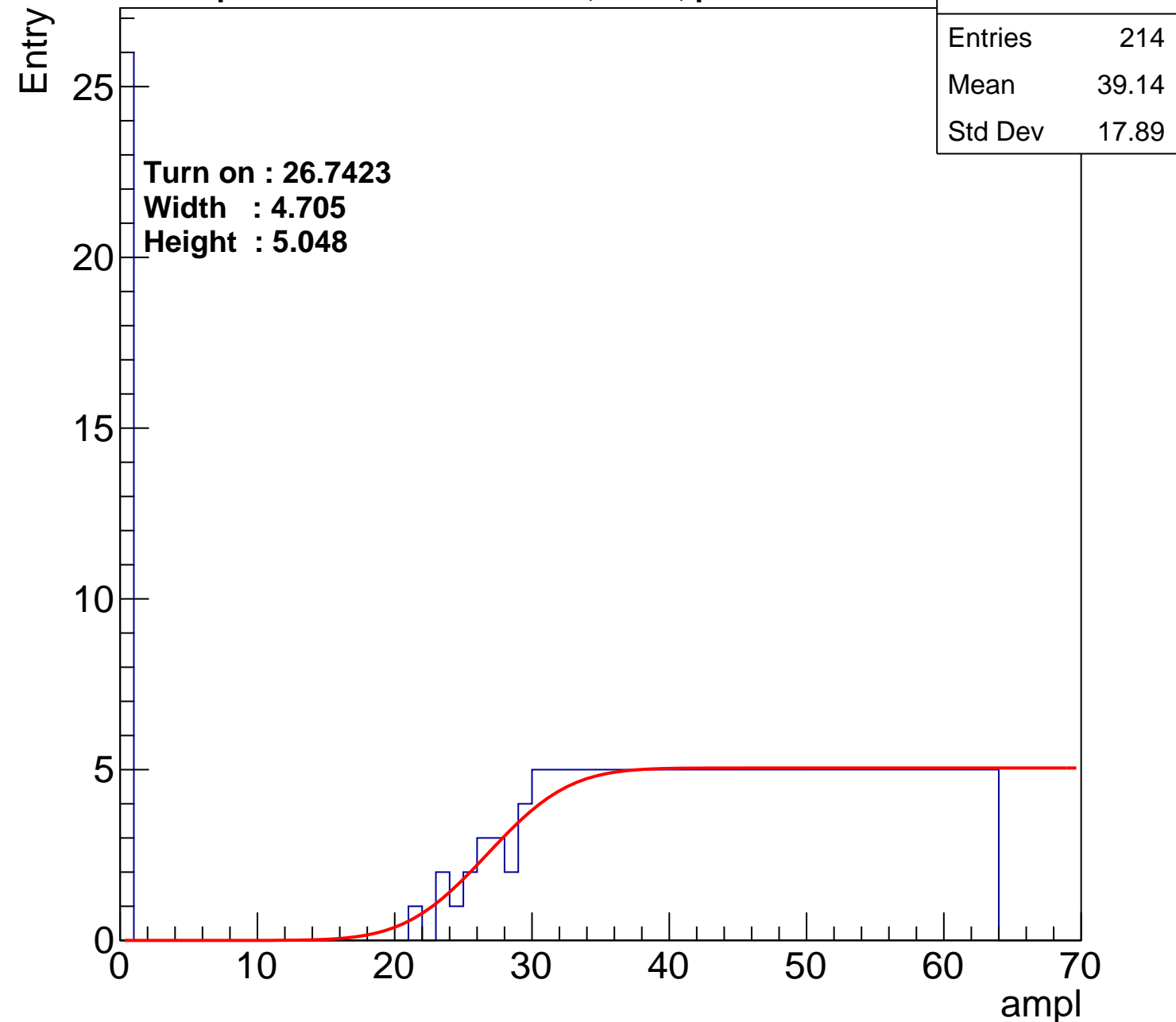
40

50

60

70

ampl



# B1L103S, U14-ch51

calib\_packv5\_041523\_1651.root, FC#0, port C2

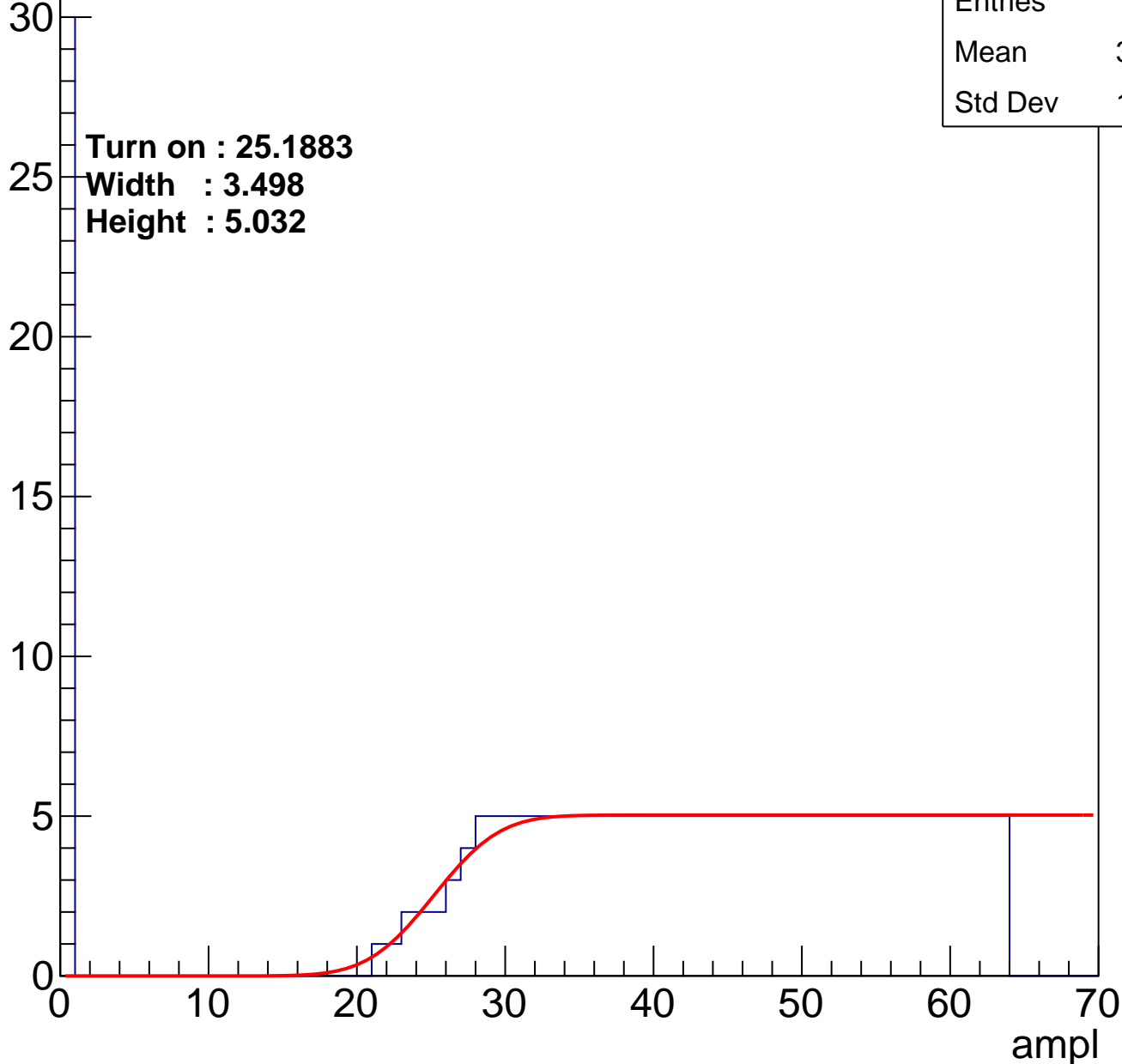
Entries	225
Mean	38.06
Std Dev	18.32

**Turn on : 25.1883**

**Width : 3.498**

**Height : 5.032**

Entry

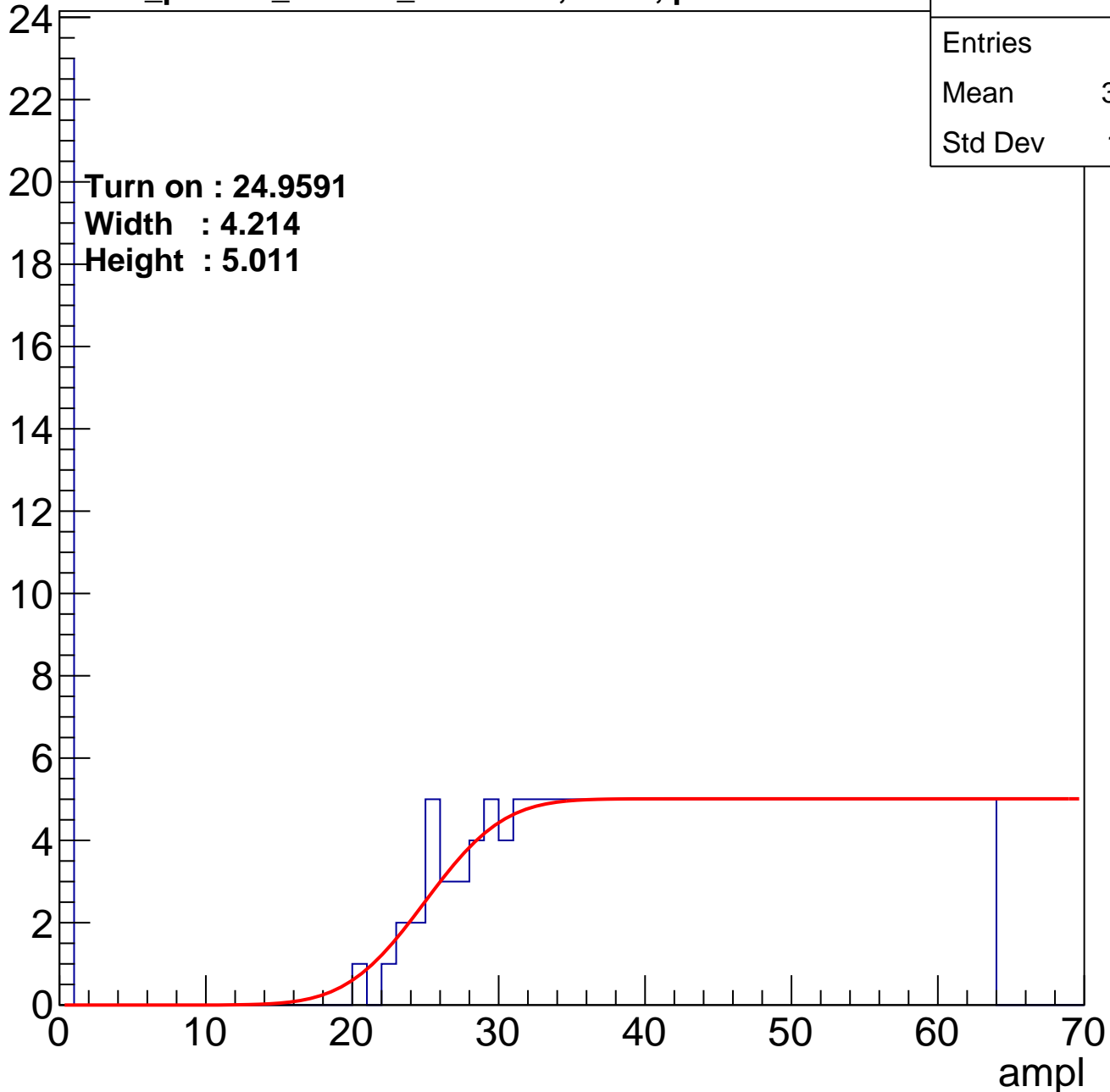


# B1L103S, U14-ch52

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	218
Mean	39.23
Std Dev	17.31

Entry



# B1L103S, U14-ch53

calib\_packv5\_041523\_1651.root, FC#0, port C2

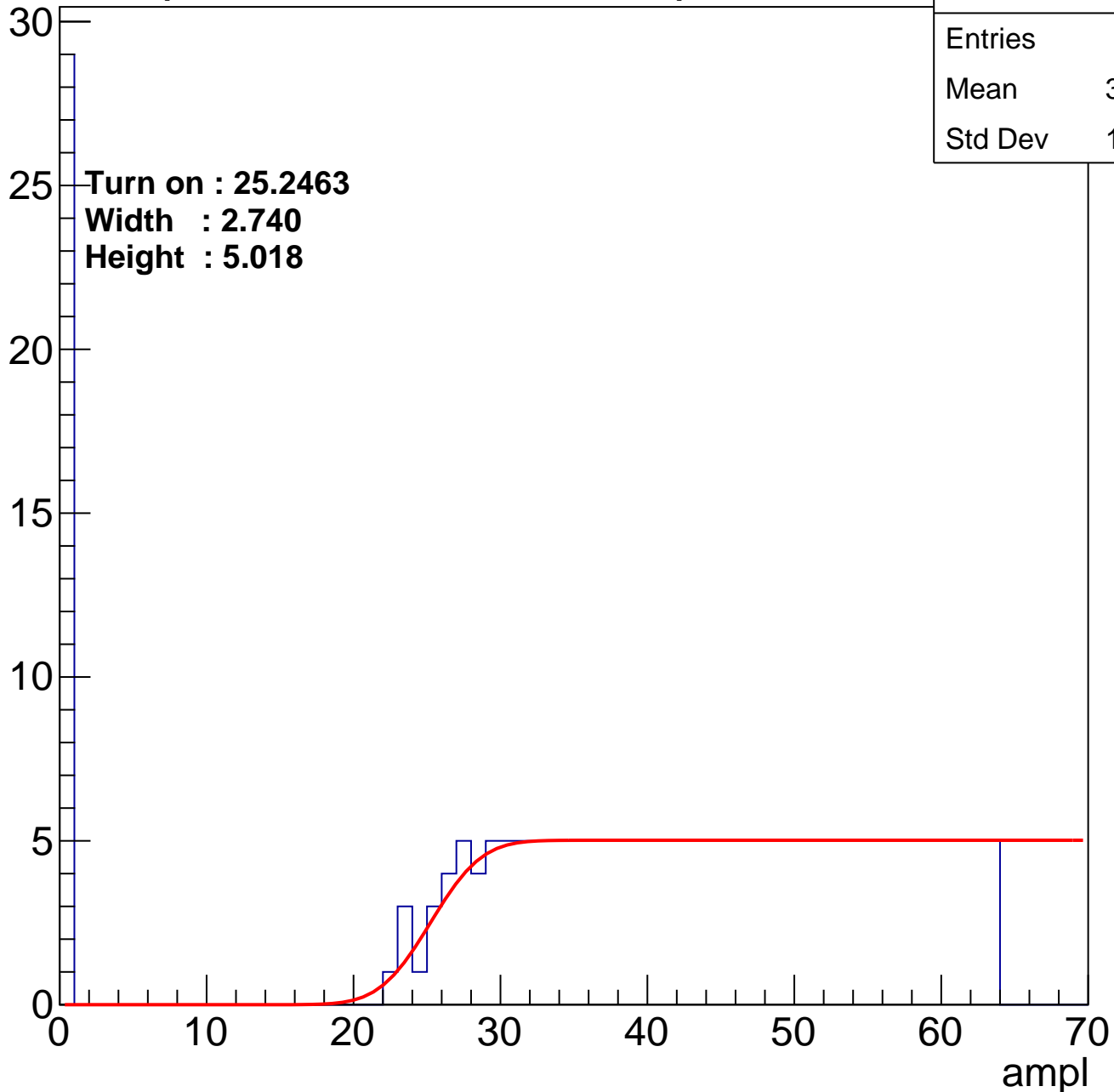
Entries	225
Mean	38.18
Std Dev	18.15

Turn on : 25.2463

Width : 2.740

Height : 5.018

Entry



# B1L103S, U14-ch54

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	217
Mean	38.82
Std Dev	18.03

**Turn on : 26.6269**

**Width : 4.824**

**Height : 5.059**

Entry

25

20

15

10

5

0

0

10

20

30

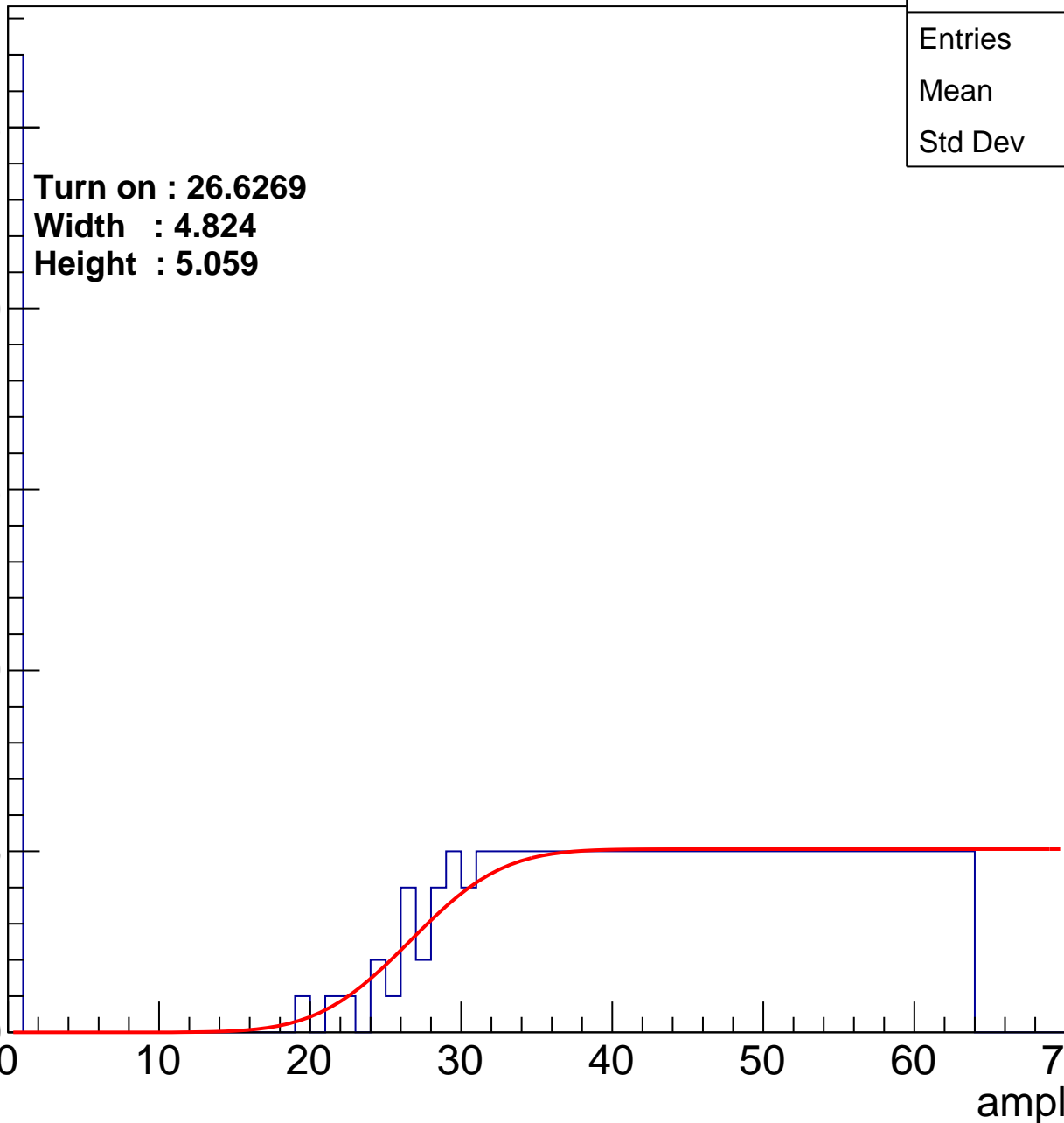
40

50

60

70

ampl



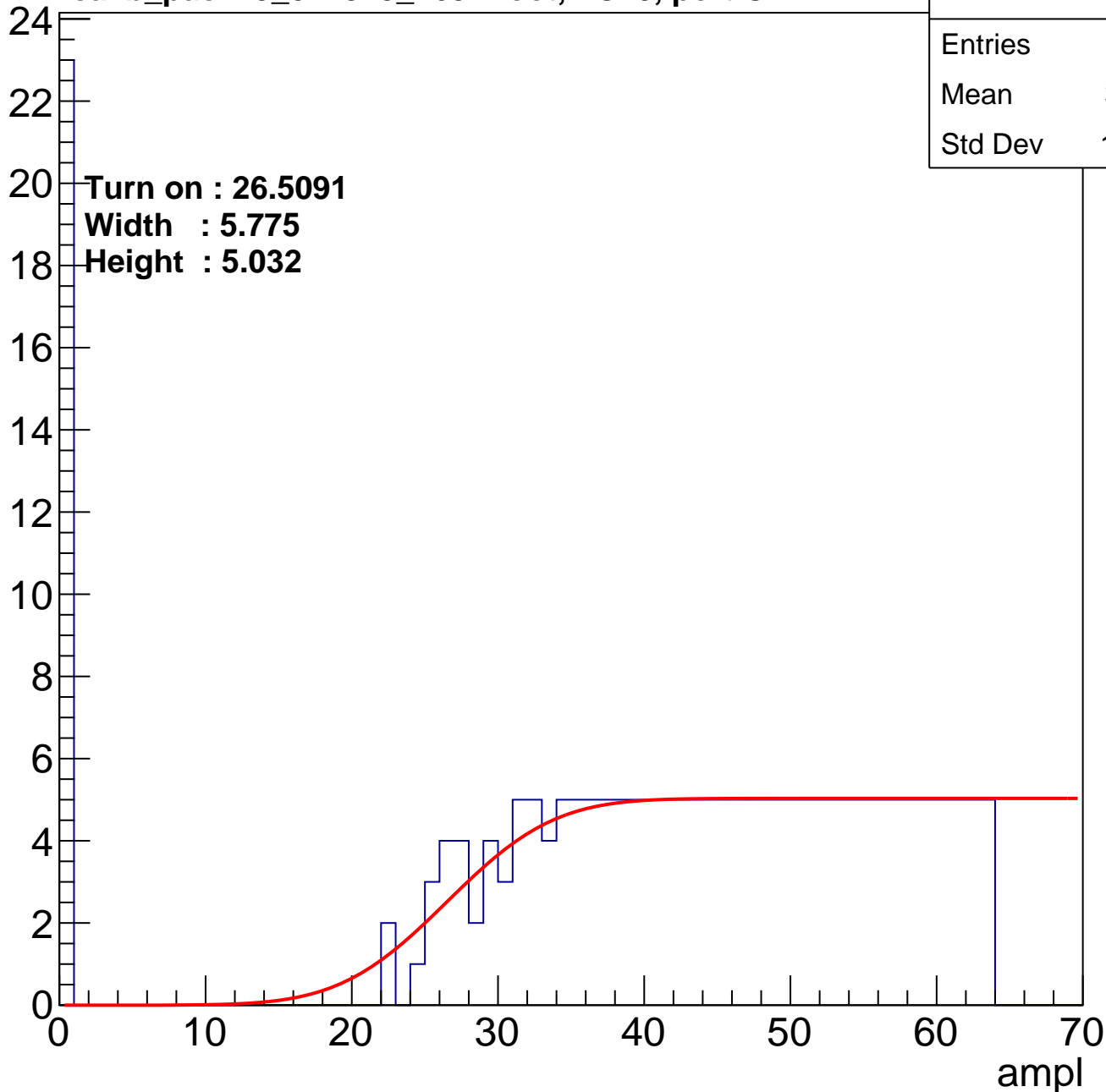


# B1L103S, U14-ch55

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	210
Mean	39.71
Std Dev	17.44

Entry



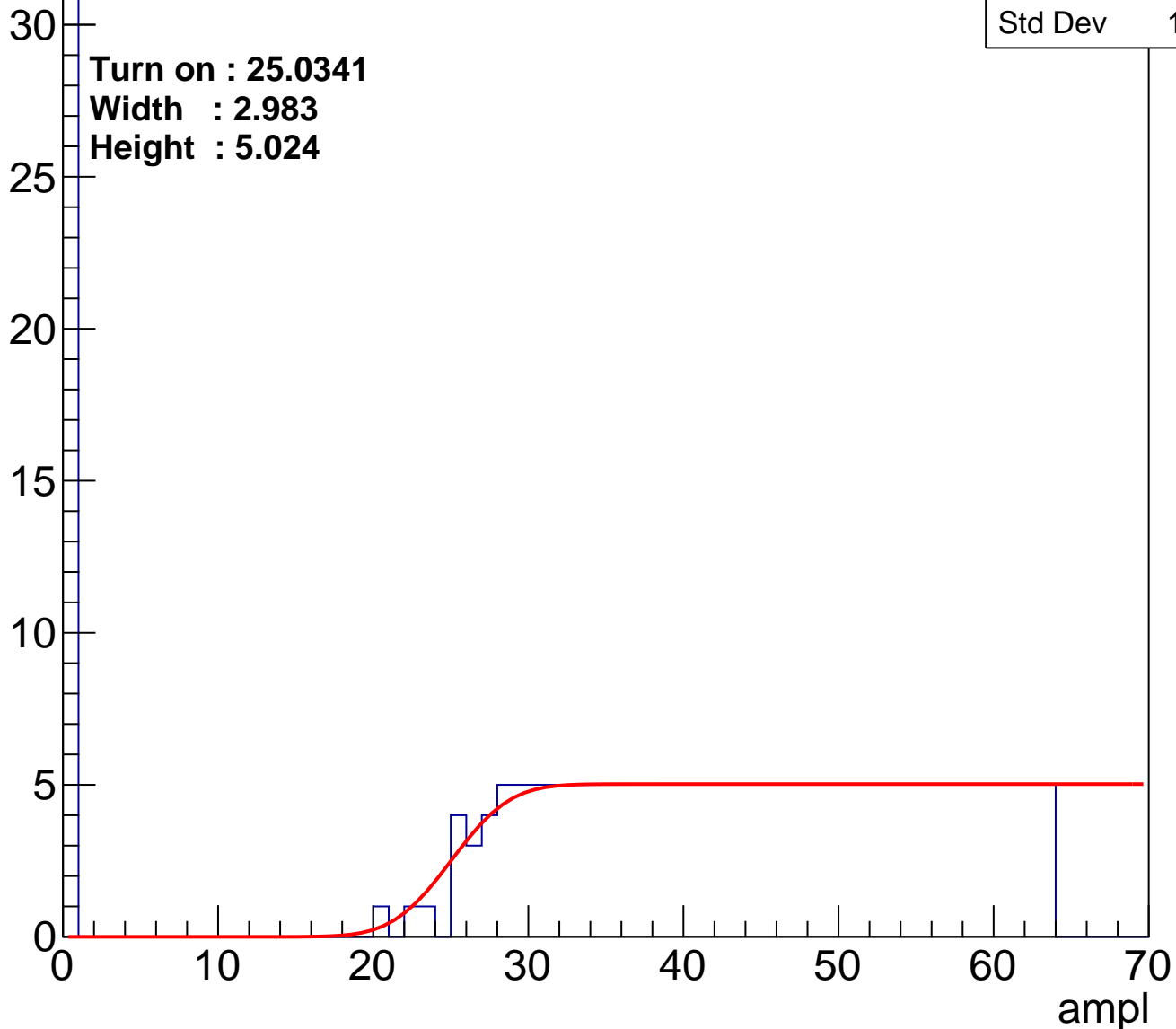
# B1L103S, U14-ch56

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	227
Mean	37.63
Std Dev	18.72

**Turn on : 25.0341**  
**Width : 2.983**  
**Height : 5.024**

Entry

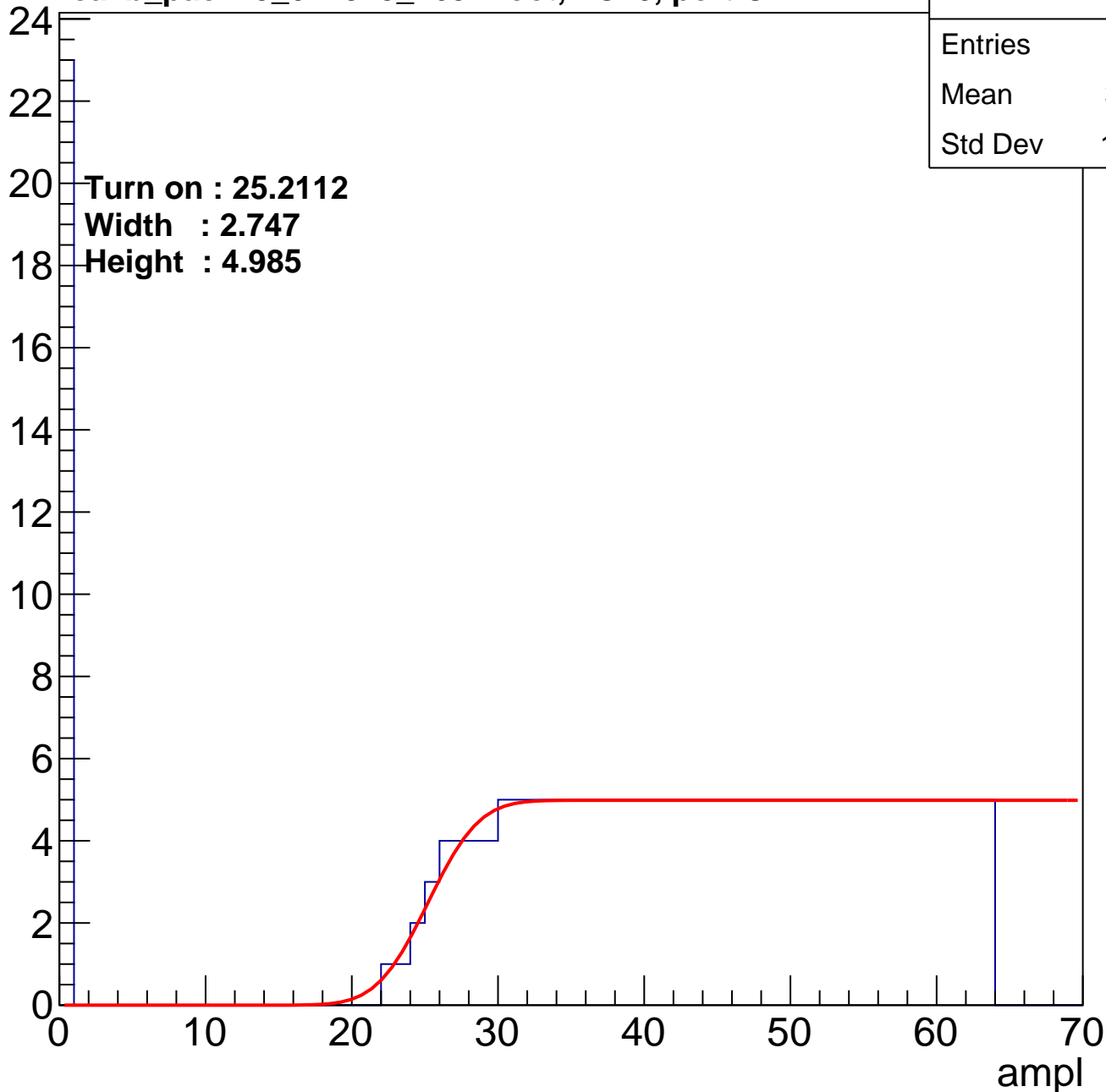


# B1L103S, U14-ch57

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	216
Mean	39.41
Std Dev	17.29

Entry



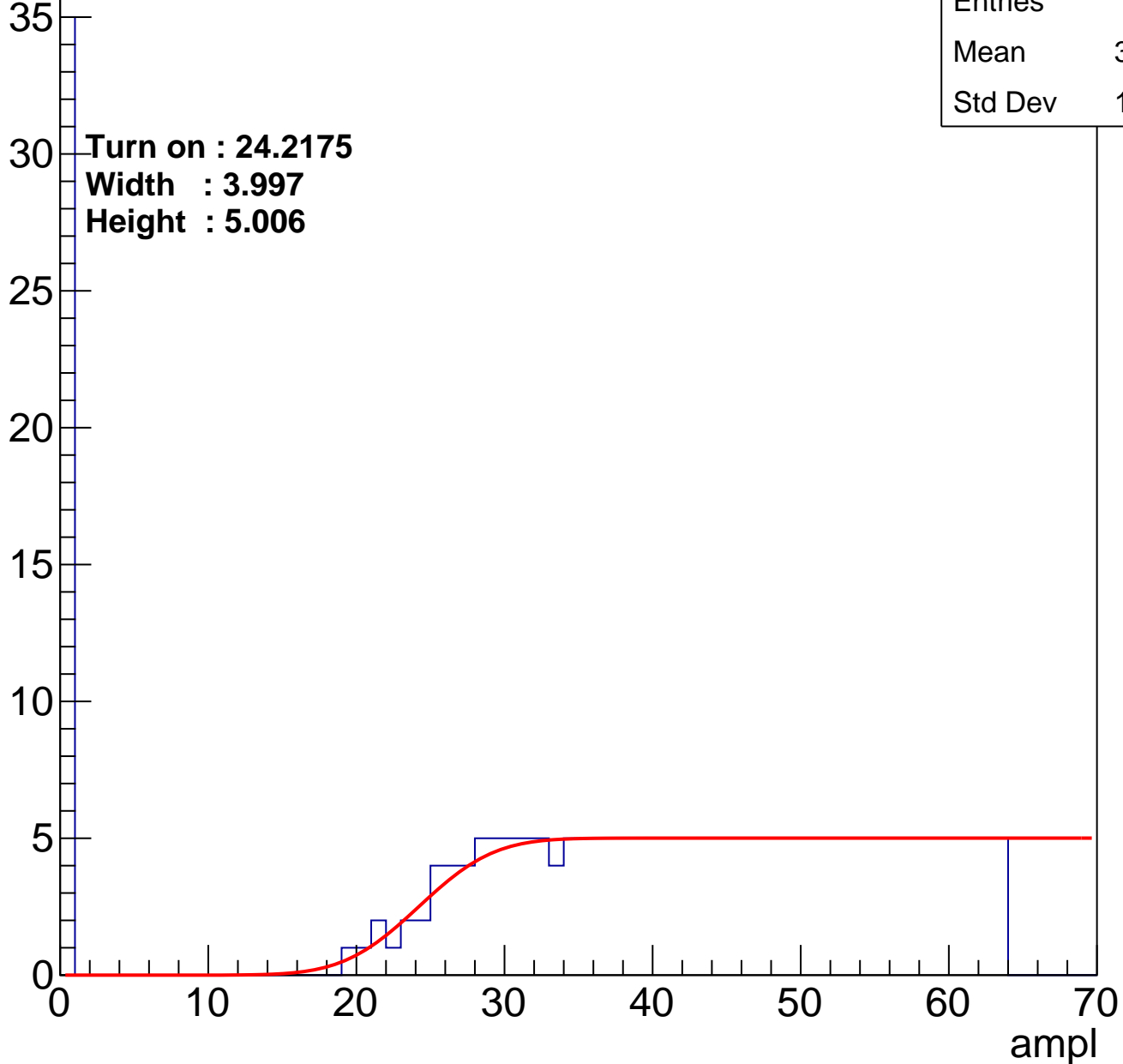
# B1L103S, U14-ch58

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	235
Mean	36.88
Std Dev	18.89

Turn on : 24.2175  
Width : 3.997  
Height : 5.006

Entry



# B1L103S, U14-ch59

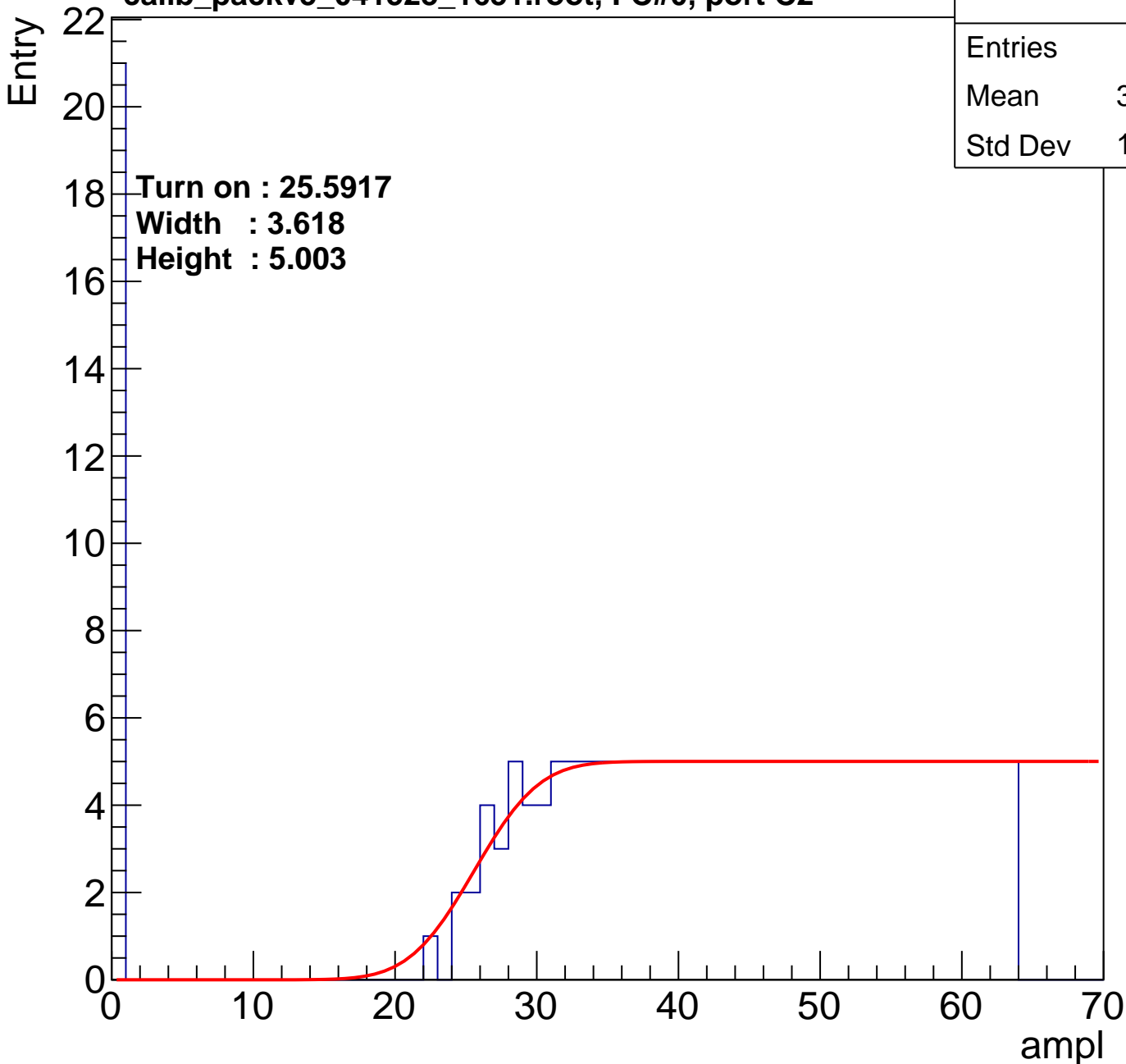
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	211
Mean	39.98
Std Dev	16.98

Turn on : 25.5917

Width : 3.618

Height : 5.003



# B1L103S, U14-ch60

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	220
Mean	38.5
Std Dev	18.16

**Turn on : 26.0363**  
**Width : 4.978**  
**Height : 5.057**

Entry

25

20

15

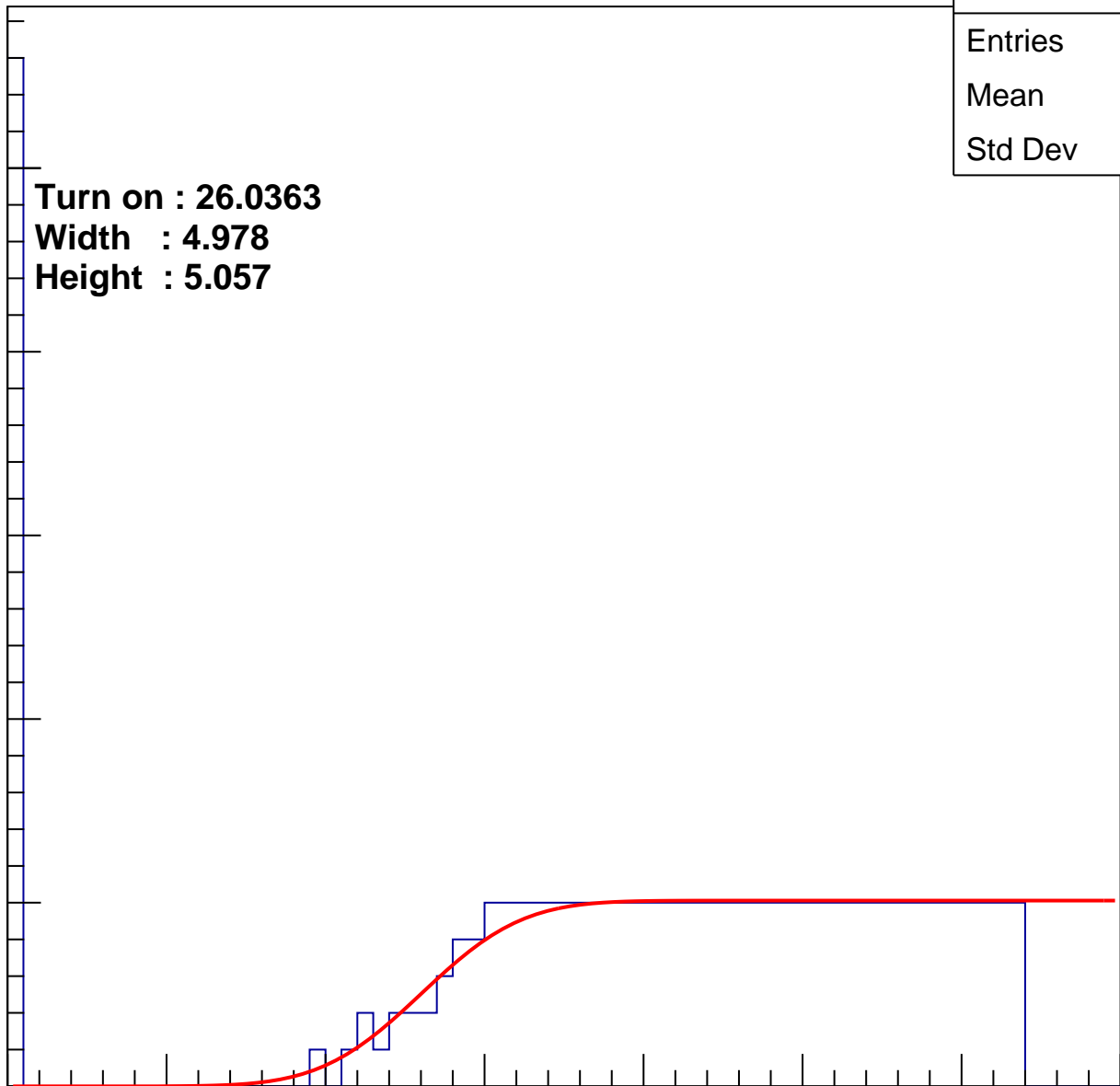
10

5

0

0 10 20 30 40 50 60 70

ampl



# B1L103S, U14-ch61

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entry

30

25

20

15

10

5

0

Turn on : 27.2112

Width : 4.067

Height : 5.043

Entries	218
Mean	38.2
Std Dev	18.8

ampl

0 10 20 30 40 50 60 70

# B1L103S, U14-ch62

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	218
Mean	38.9
Std Dev	17.82

**Turn on : 25.9028**

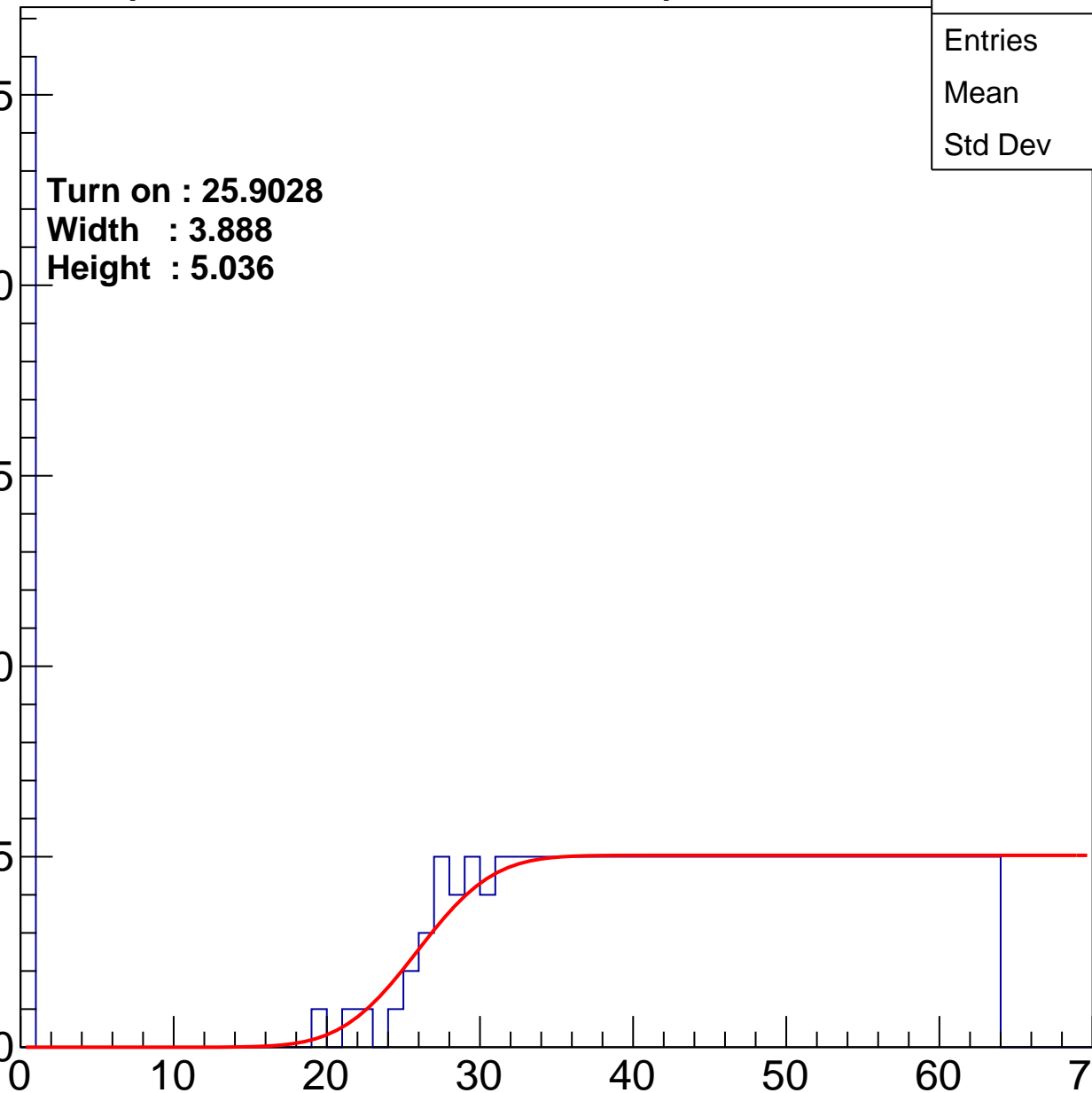
**Width : 3.888**

**Height : 5.036**

Entry

25  
20  
15  
10  
5  
0

ampl





# B1L103S, U14-ch63

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	229
Mean	37.44
Std Dev	18.73

**Turn on : 24.5286**

**Width : 5.195**

**Height : 5.034**

Entry

30

25

20

15

10

5

0

ampl

0

10

20

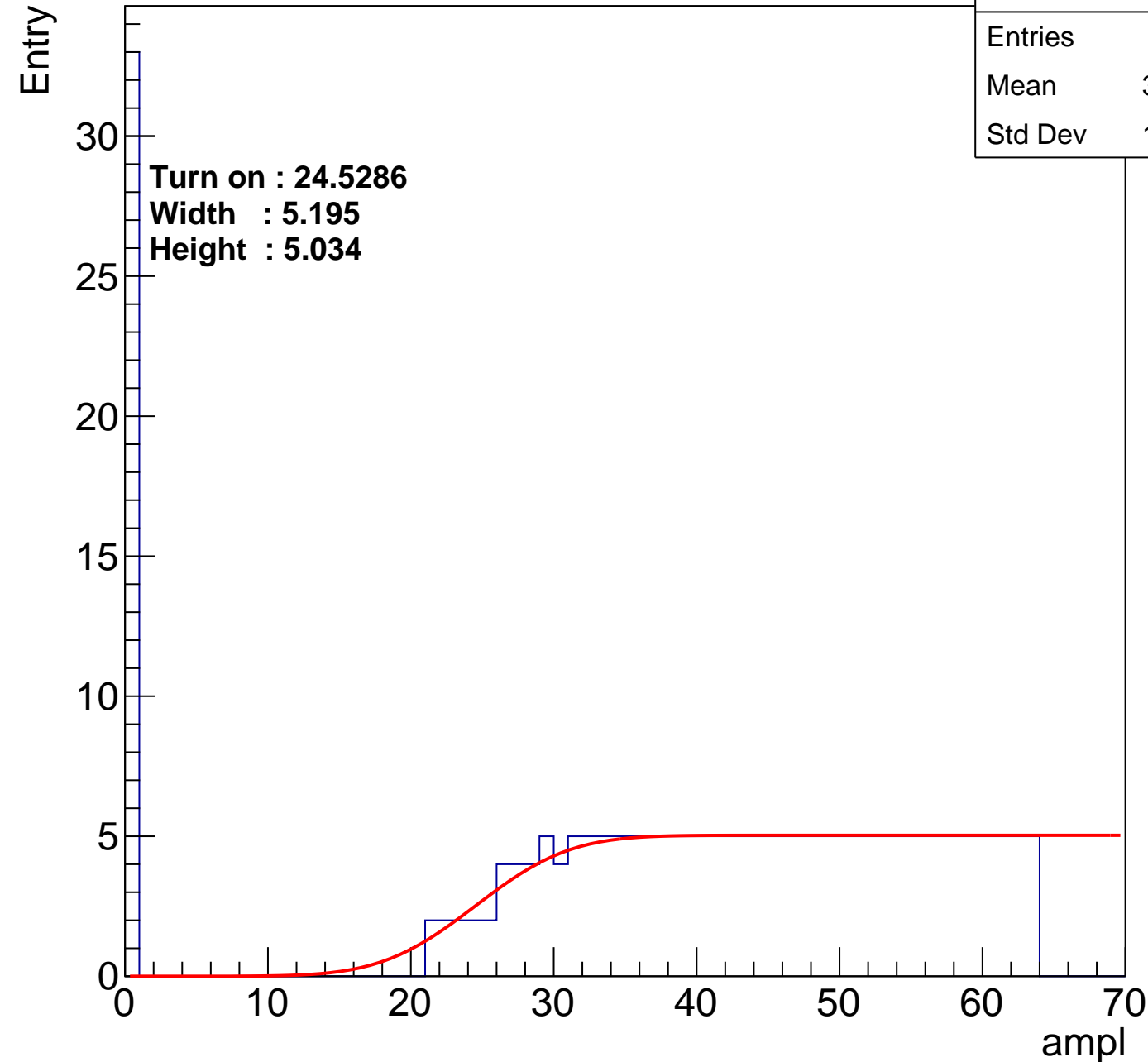
30

40

50

60

70

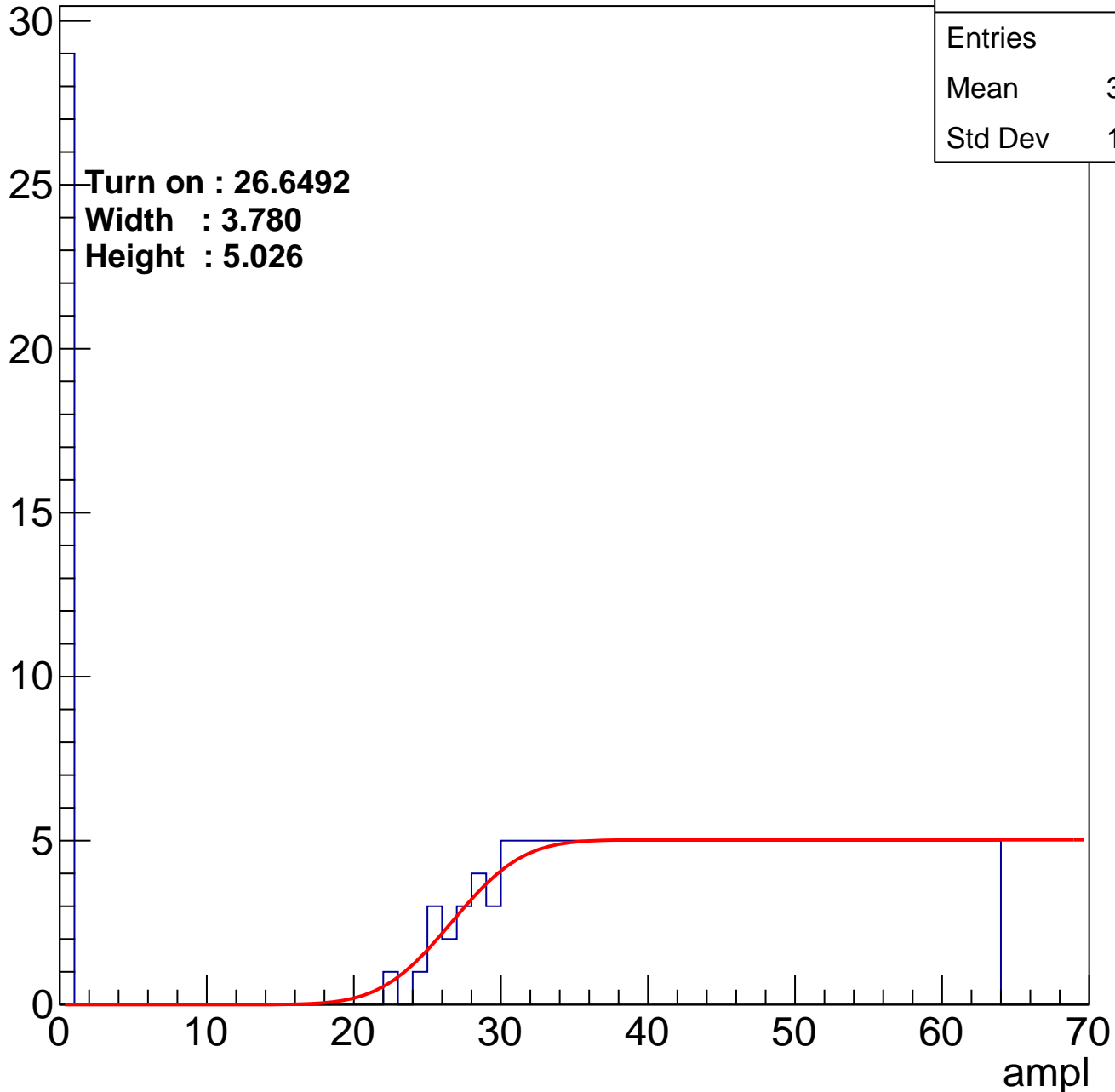


# B1L103S, U14-ch64

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	216
Mean	38.69
Std Dev	18.34

Entry



# B1L103S, U14-ch65

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	227
Mean	37.61
Std Dev	18.72

**Turn on : 24.1508**

**Width : 4.117**

**Height : 5.004**

Entry

30

25

20

15

10

5

0

ampl

0

10

20

30

40

50

60

70

# B1L103S, U14-ch66

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	226
Mean	37.63
Std Dev	18.77

**Turn on : 25.3813**

**Width : 3.935**

**Height : 5.017**

Entry

30

25

20

15

10

5

0

0

10

20

30

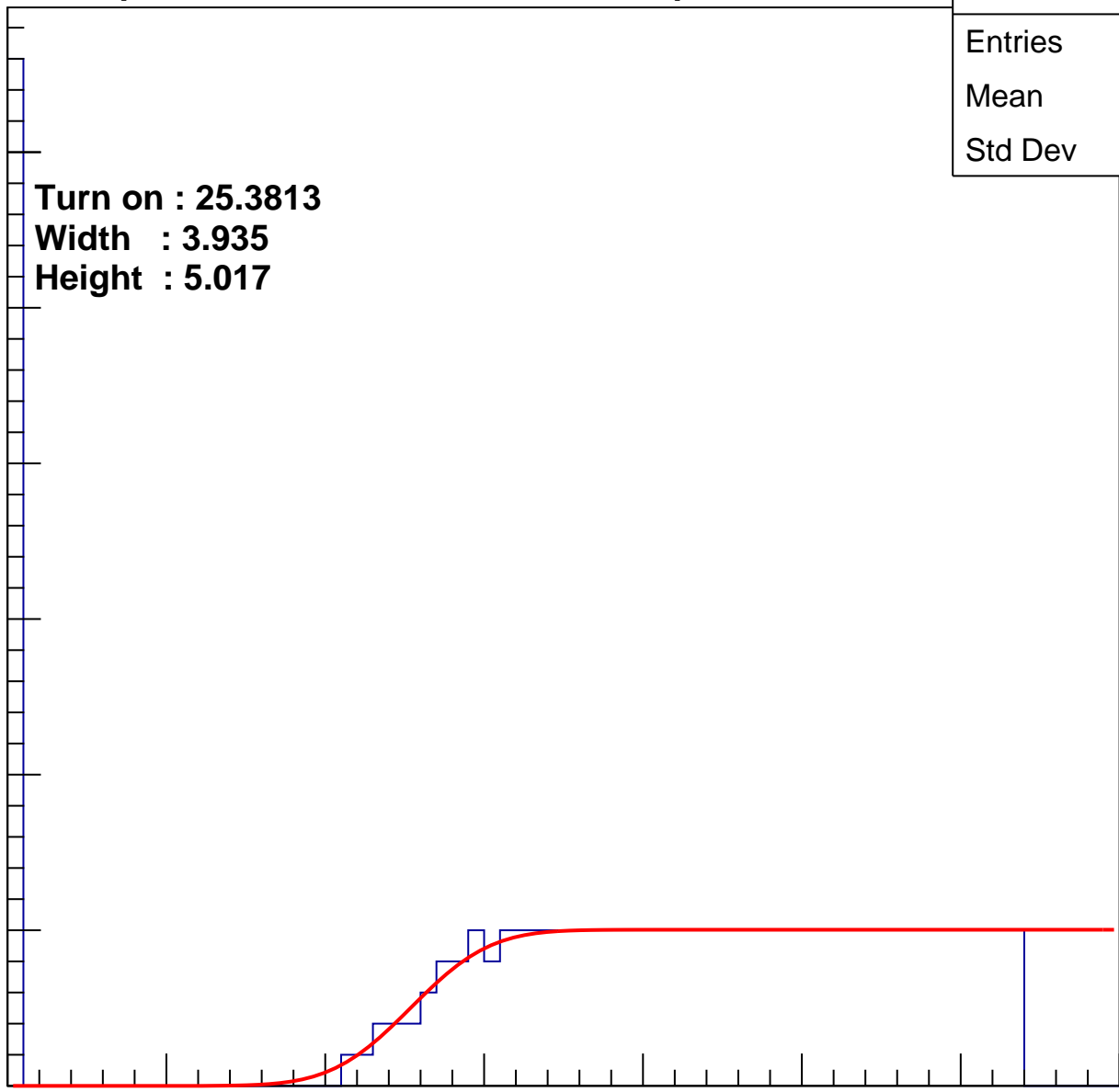
40

50

60

70

ampl



# B1L103S, U14-ch67

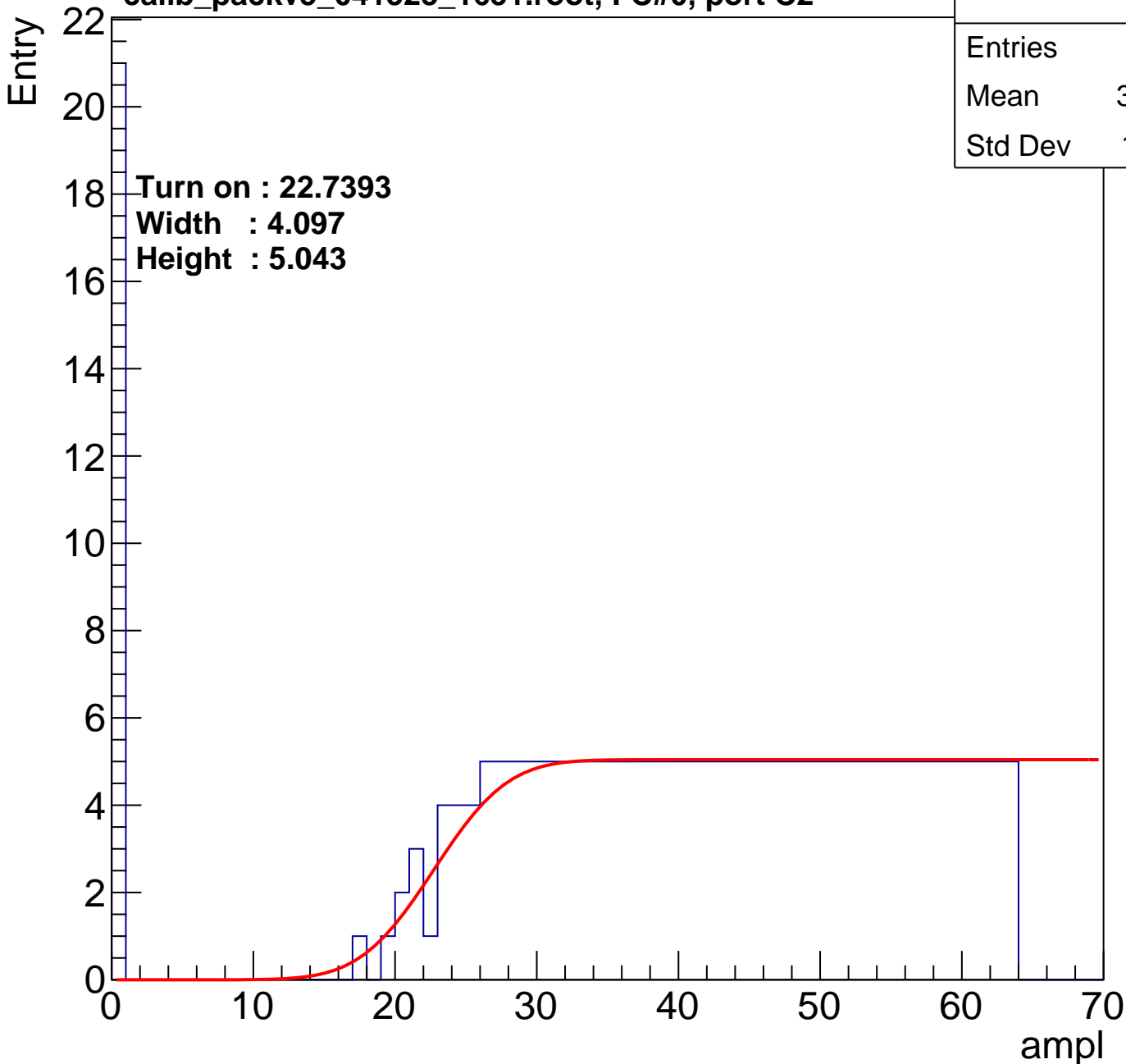
calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	231
Mean	38.55
Std Dev	16.91

Turn on : 22.7393

Width : 4.097

Height : 5.043



# B1L103S, U14-ch68

calib\_packv5\_041523\_1651.root, FC#0, port C2

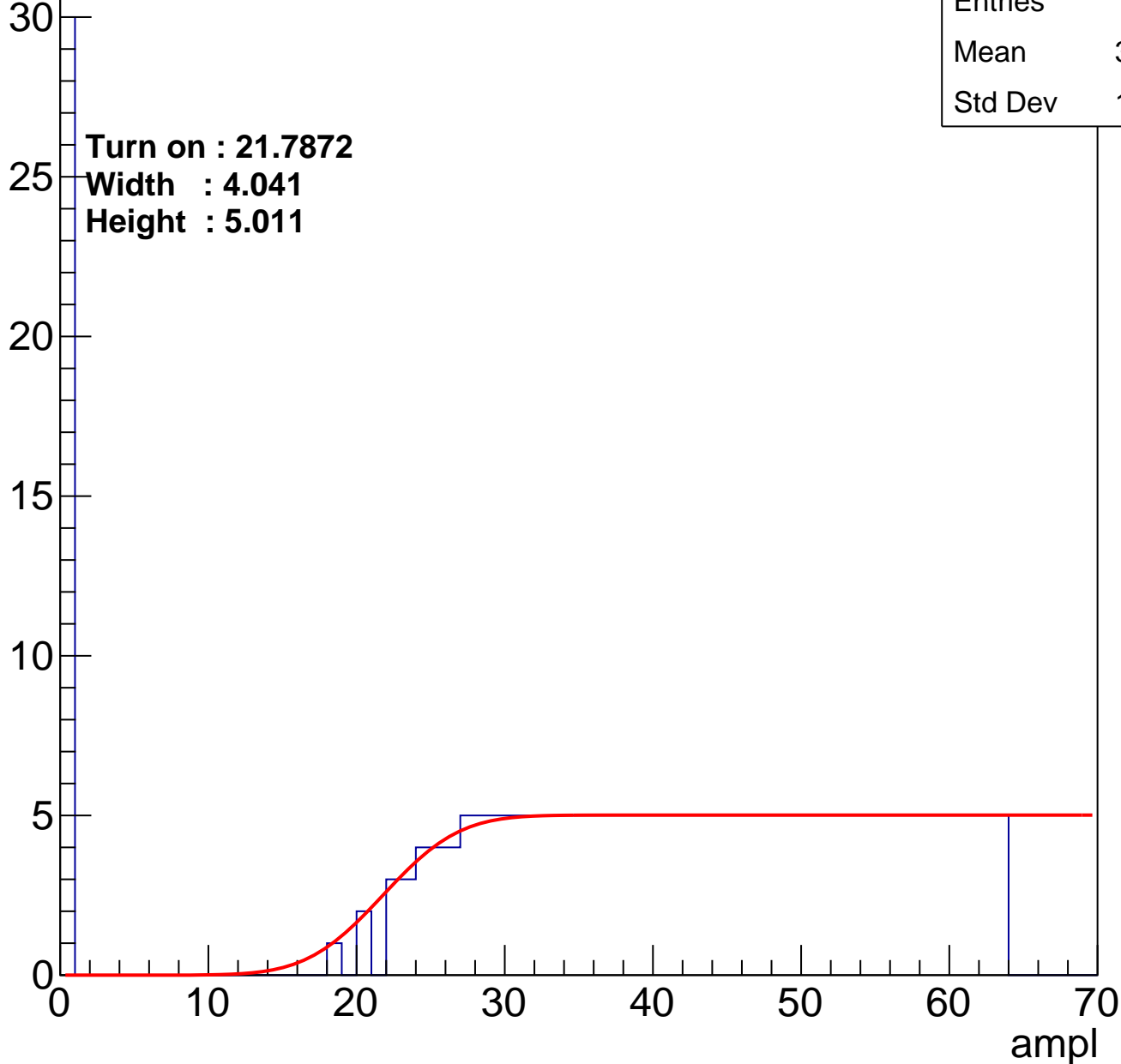
Entries	236
Mean	37.36
Std Dev	18.17

**Turn on : 21.7872**

**Width : 4.041**

**Height : 5.011**

Entry



# B1L103S, U14-ch69

calib\_packv5\_041523\_1651.root, FC#0, port C2

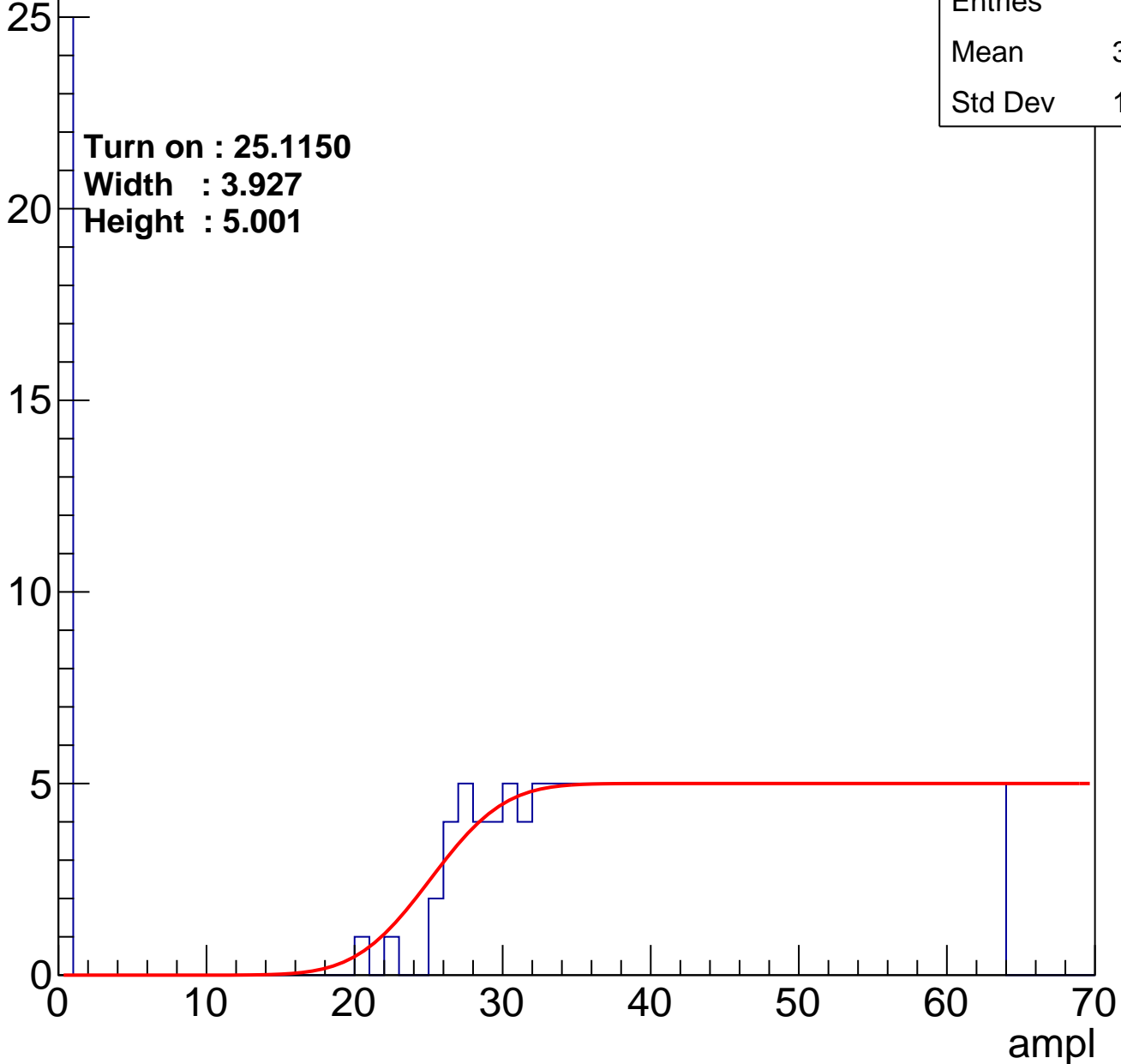
Entries	215
Mean	39.22
Std Dev	17.68

Turn on : 25.1150

Width : 3.927

Height : 5.001

Entry



# B1L103S, U14-ch70

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	226
Mean	38.4
Std Dev	17.71

**Turn on : 24.1367**

**Width : 3.130**

**Height : 5.020**

Entry

25

20

15

10

5

0

0

10

20

30

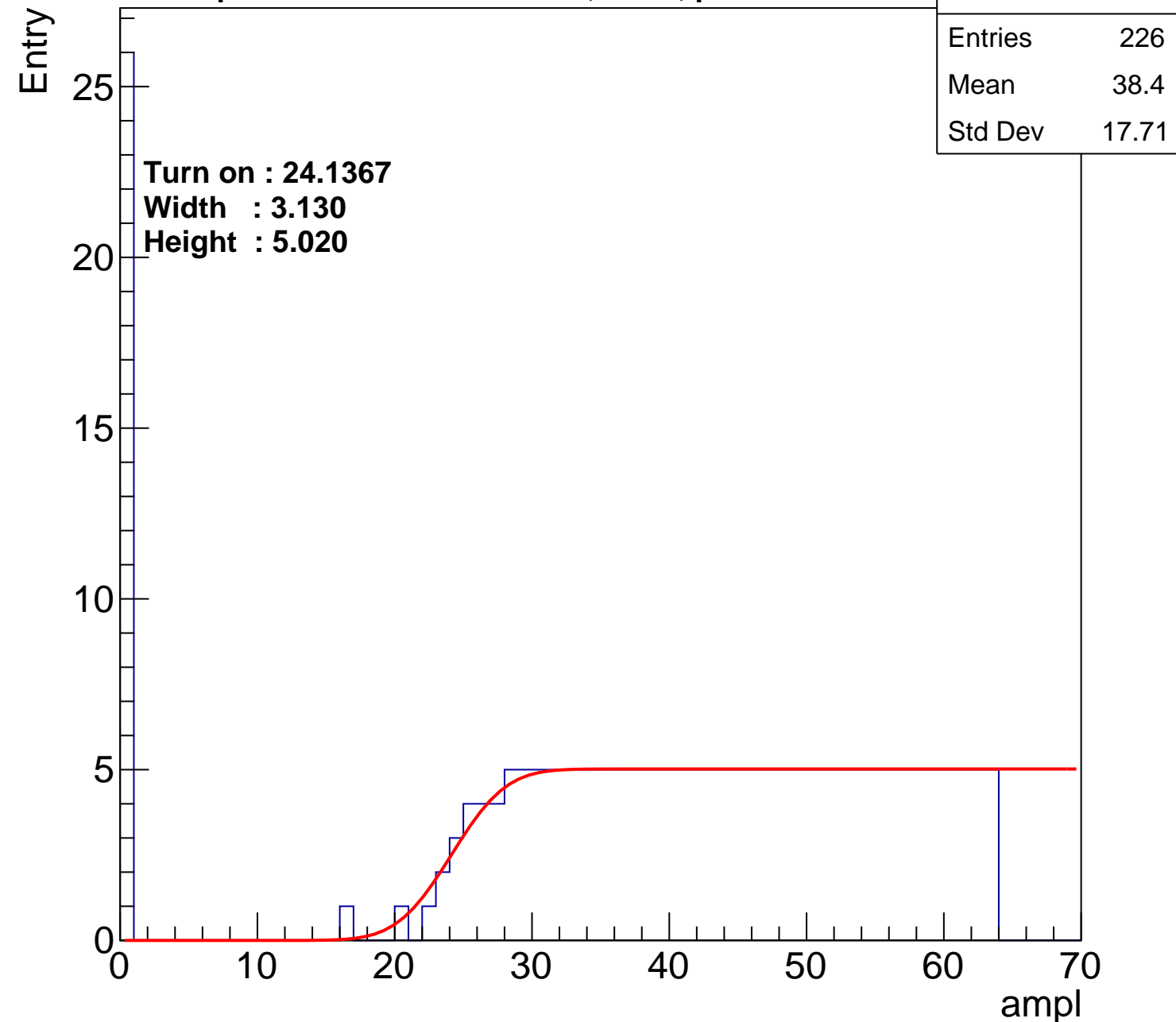
40

50

60

70

ampl





# B1L103S, U14-ch71

calib\_packv5\_041523\_1651.root, FC#0, port C2

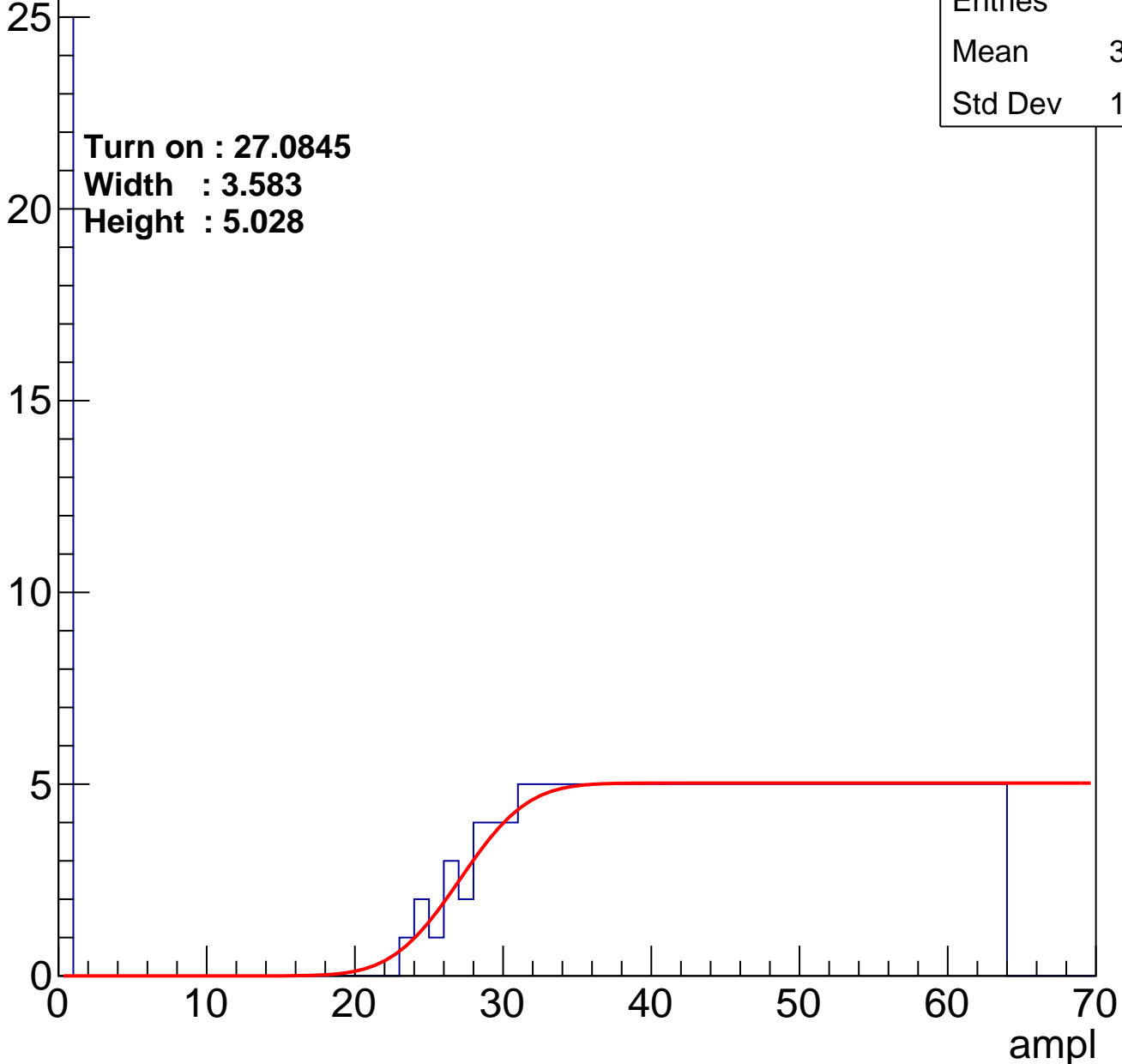
Entries	211
Mean	39.48
Std Dev	17.74

**Turn on : 27.0845**

**Width : 3.583**

**Height : 5.028**

Entry



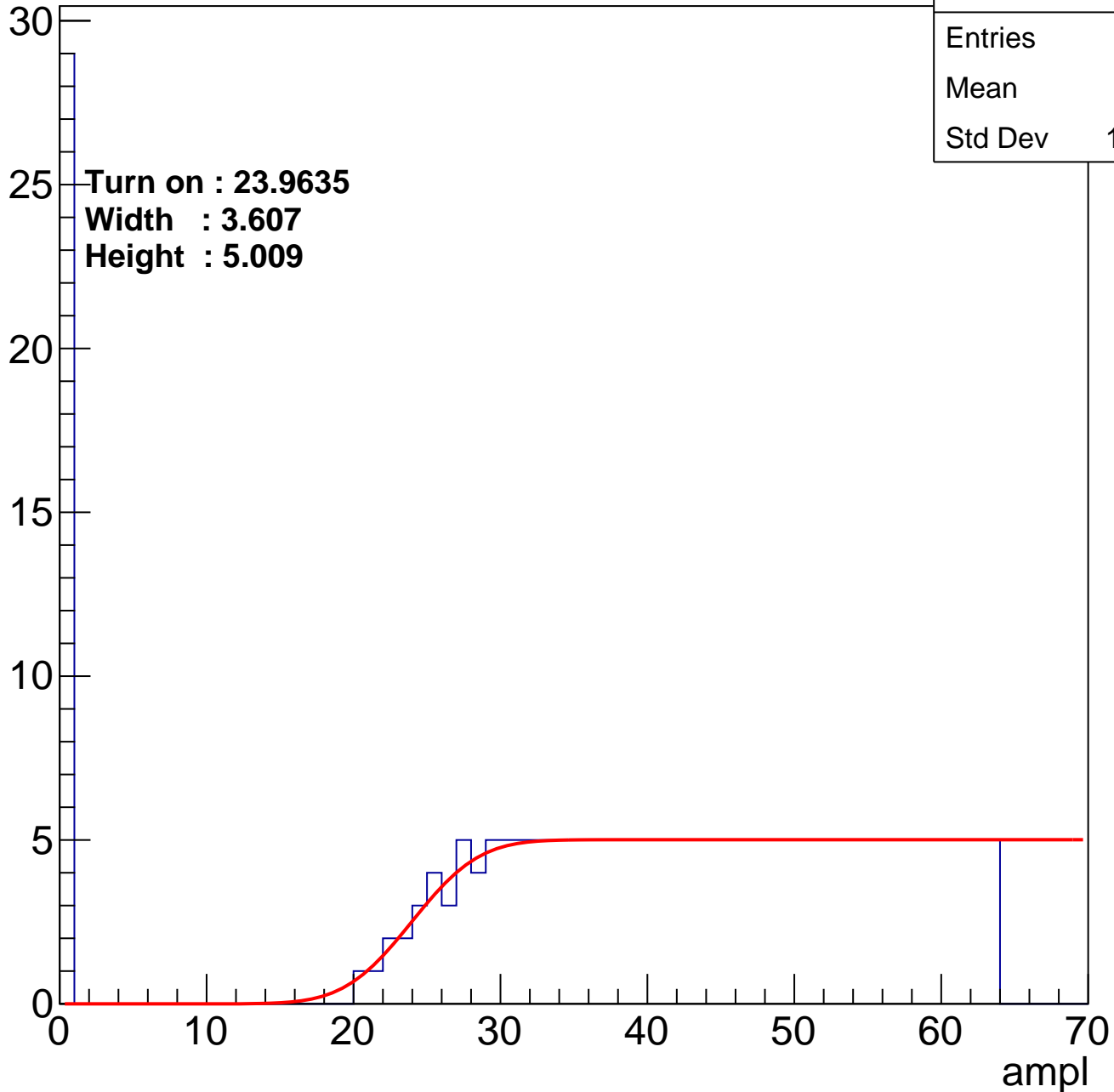
# B1L103S, U14-ch72

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	229
Mean	37.9
Std Dev	18.12

Turn on : 23.9635  
Width : 3.607  
Height : 5.009

Entry



# B1L103S, U14-ch73

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	223
Mean	38.49
Std Dev	17.9

**Turn on : 25.2121**

**Width : 3.416**

**Height : 5.037**

Entry

25

20

15

10

5

0

0

10

20

30

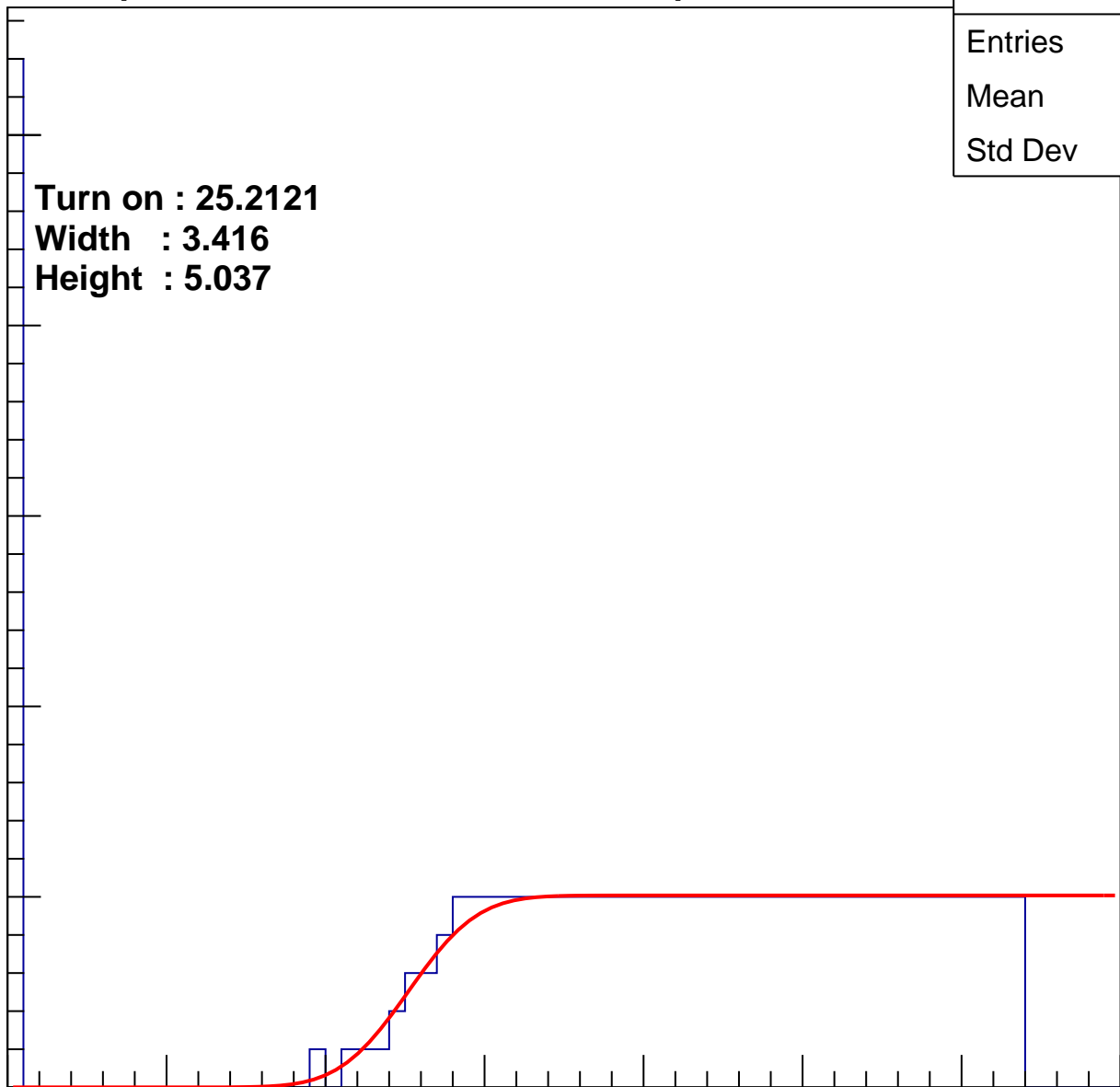
40

50

60

70

ampl



# B1L103S, U14-ch74

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	222
Mean	39.57
Std Dev	16.27

Turn on : 22.5165

Width : 4.702

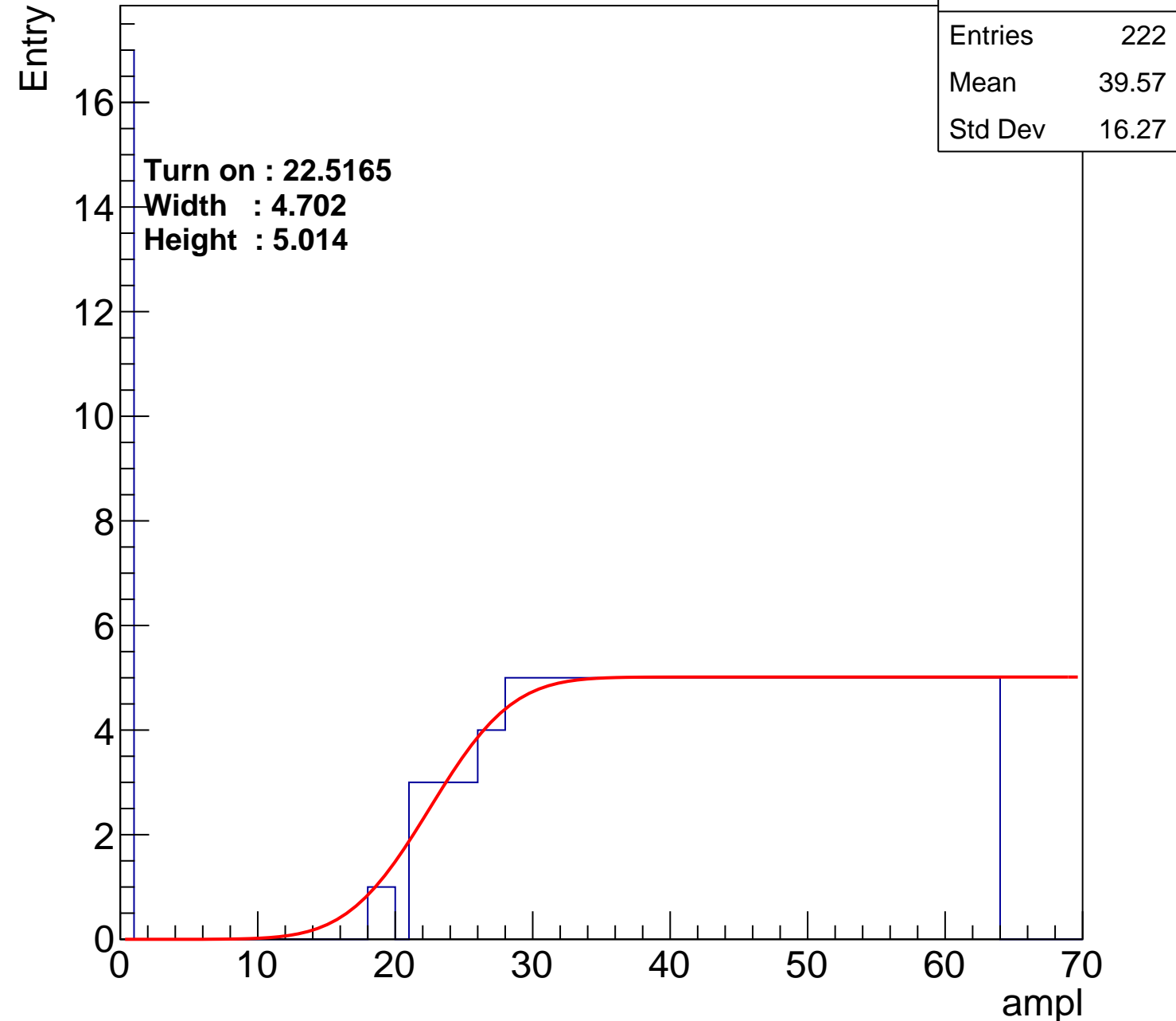
Height : 5.014

Entry

16  
14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B1L103S, U14-ch75

calib\_packv5\_041523\_1651.root, FC#0, port C2

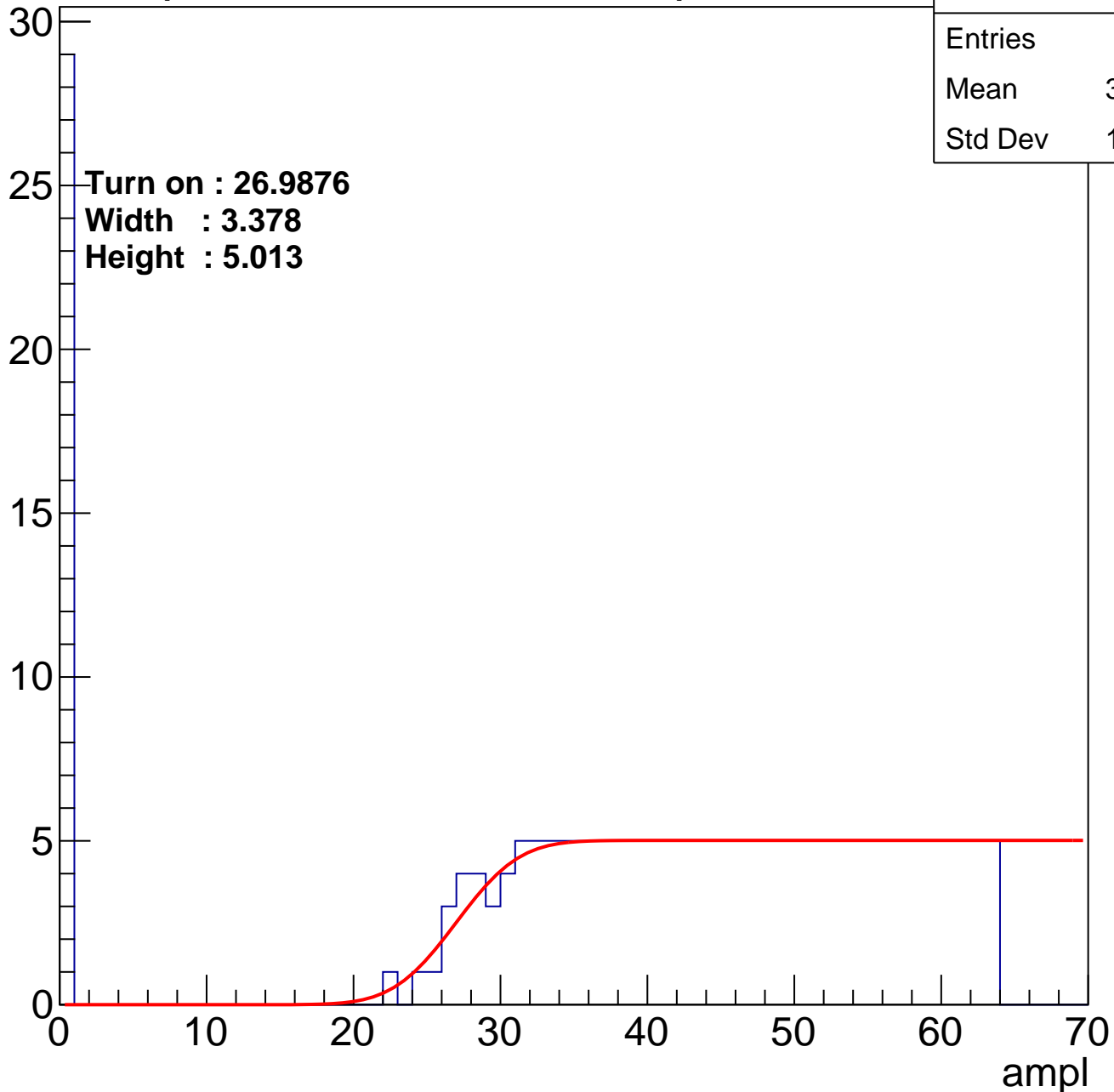
Entries	215
Mean	38.75
Std Dev	18.37

Turn on : 26.9876

Width : 3.378

Height : 5.013

Entry



# B1L103S, U14-ch76

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	232
Mean	37.59
Std Dev	18.24

**Turn on : 23.2337**

**Width : 4.182**

**Height : 5.006**

Entry

30

25

20

15

10

5

0

0

10

20

30

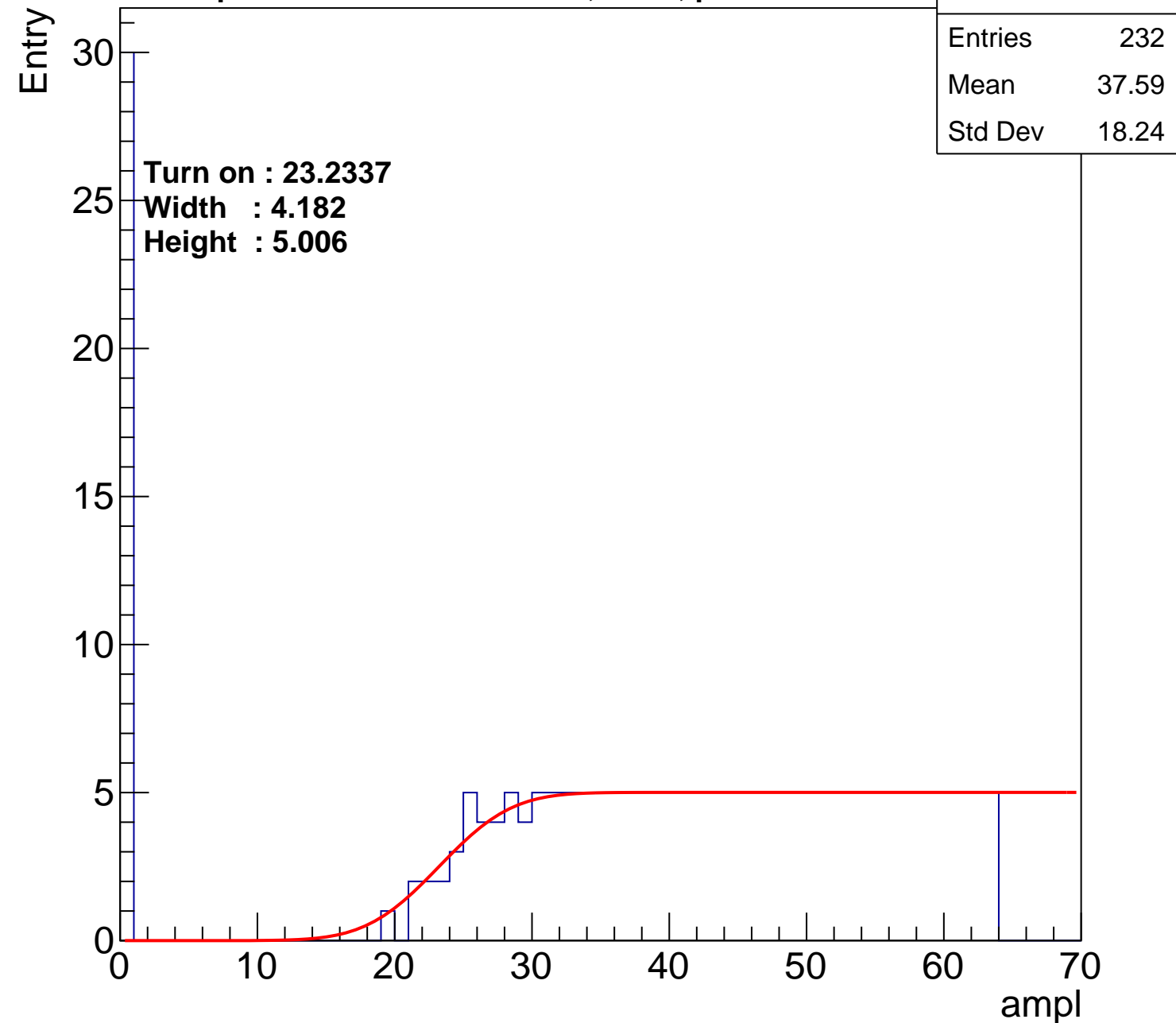
40

50

60

70

ampl



# B1L103S, U14-ch77

calib\_packv5\_041523\_1651.root, FC#0, port C2

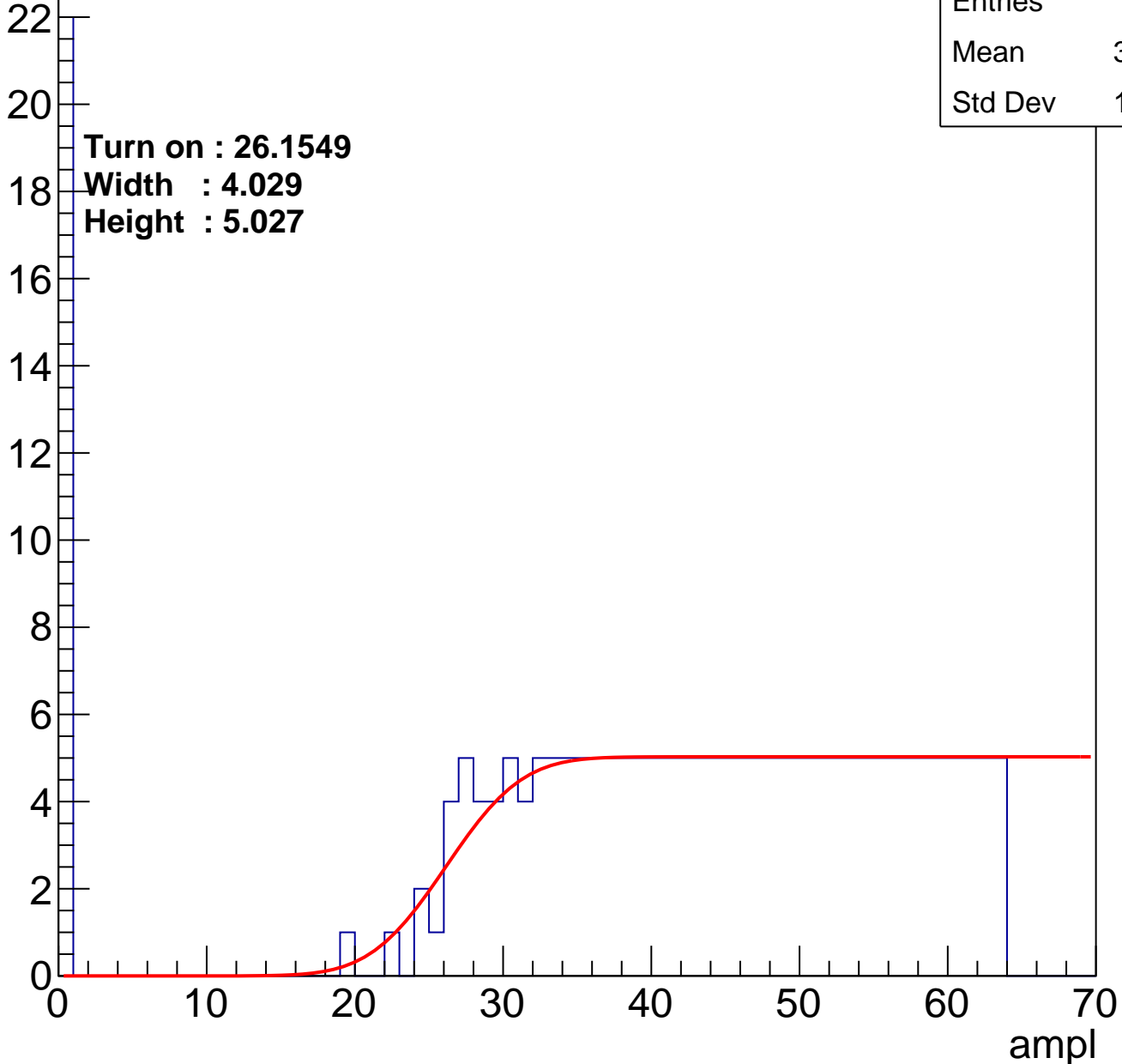
Entries	213
Mean	39.69
Std Dev	17.18

**Turn on : 26.1549**

**Width : 4.029**

**Height : 5.027**

Entry



# B1L103S, U14-ch78

calib\_packv5\_041523\_1651.root, FC#0, port C2

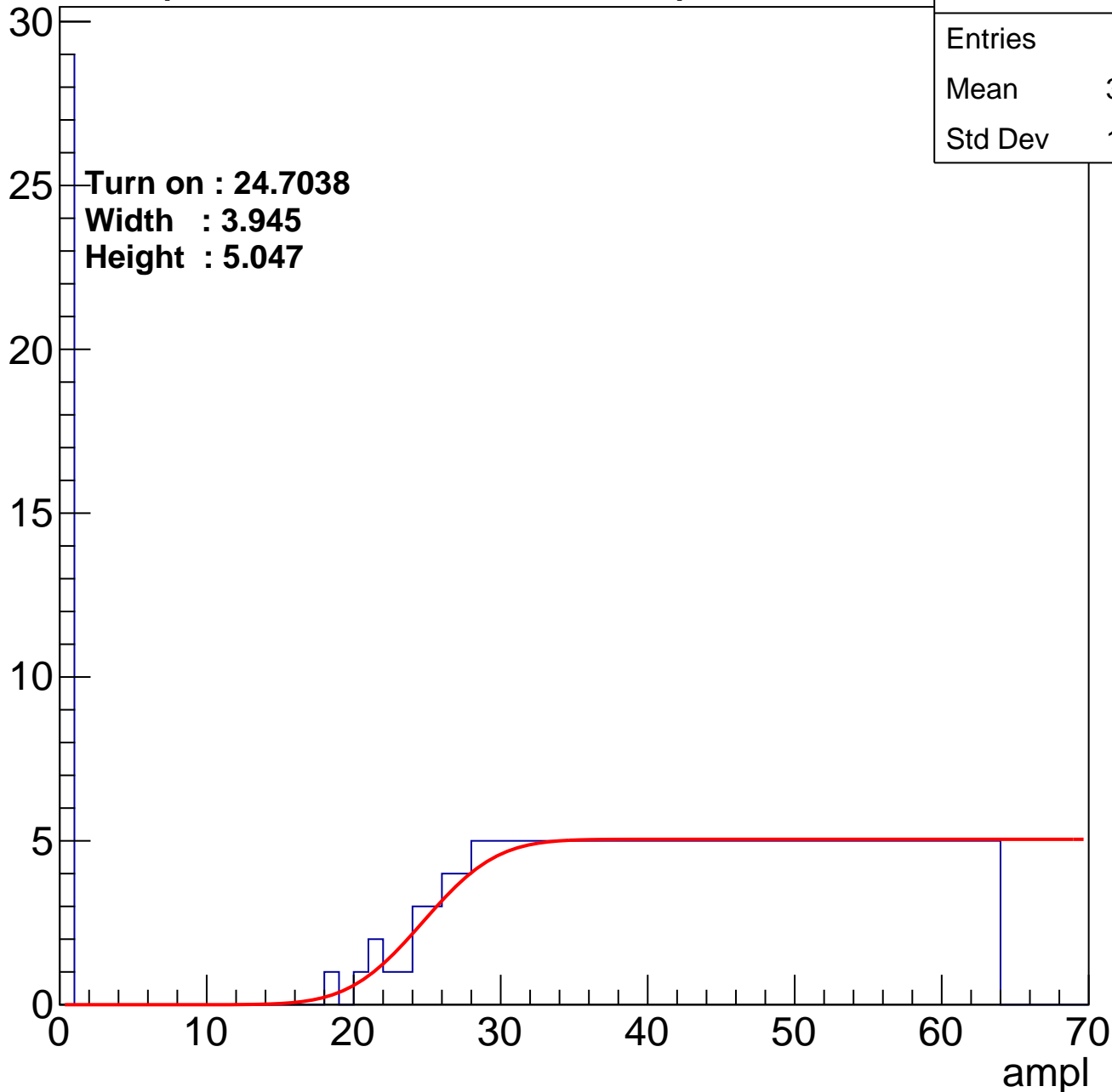
Entries	229
Mean	37.88
Std Dev	18.14

Turn on : 24.7038

Width : 3.945

Height : 5.047

Entry





# B1L103S, U14-ch79

calib\_packv5\_041523\_1651.root, FC#0, port C2

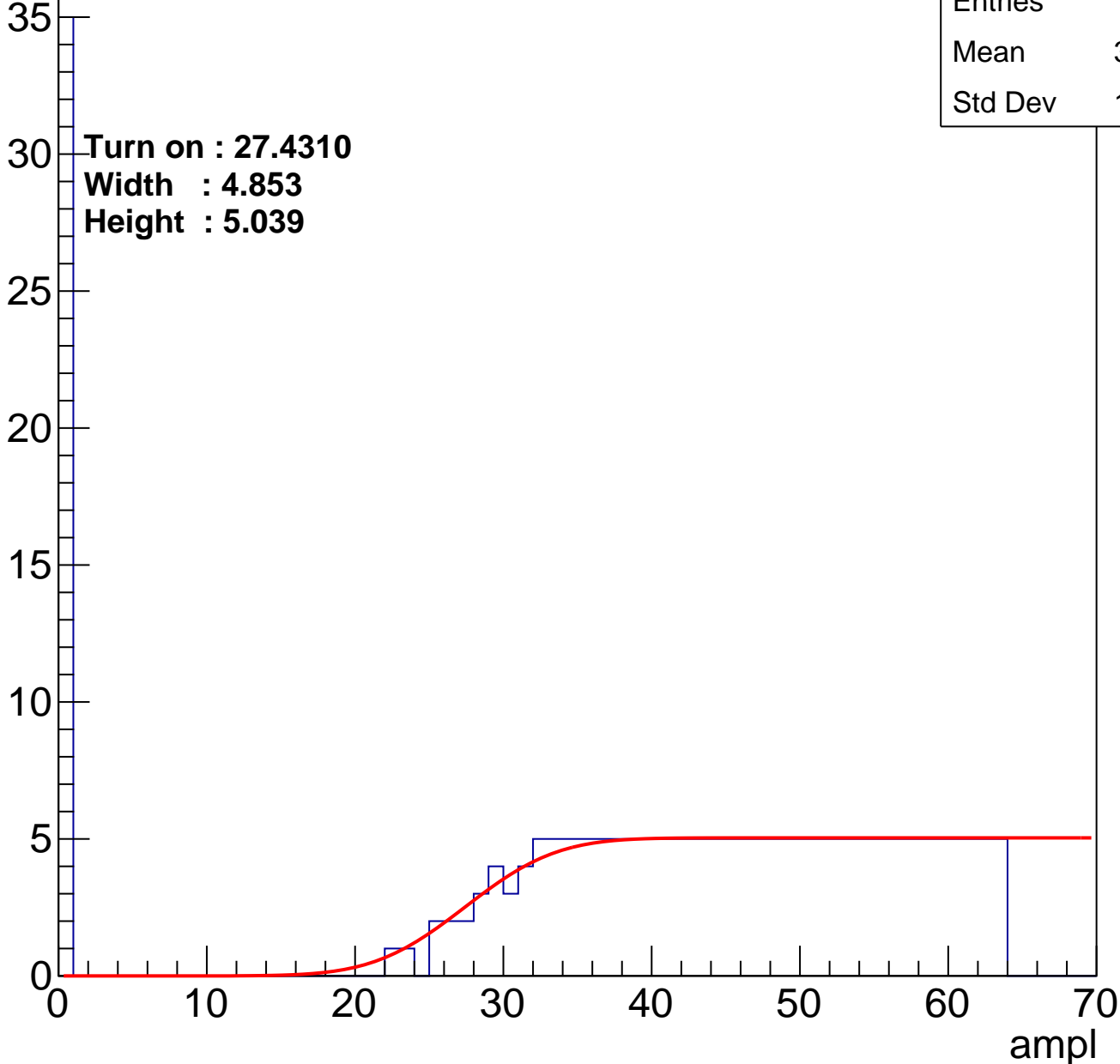
Entries	217
Mean	37.86
Std Dev	19.32

Turn on : 27.4310

Width : 4.853

Height : 5.039

Entry



# B1L103S, U14-ch80

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	220
Mean	38.81
Std Dev	17.76

**Turn on : 25.1382**

**Width : 2.934**

**Height : 4.991**

Entry

25

20

15

10

5

0

0

10

20

30

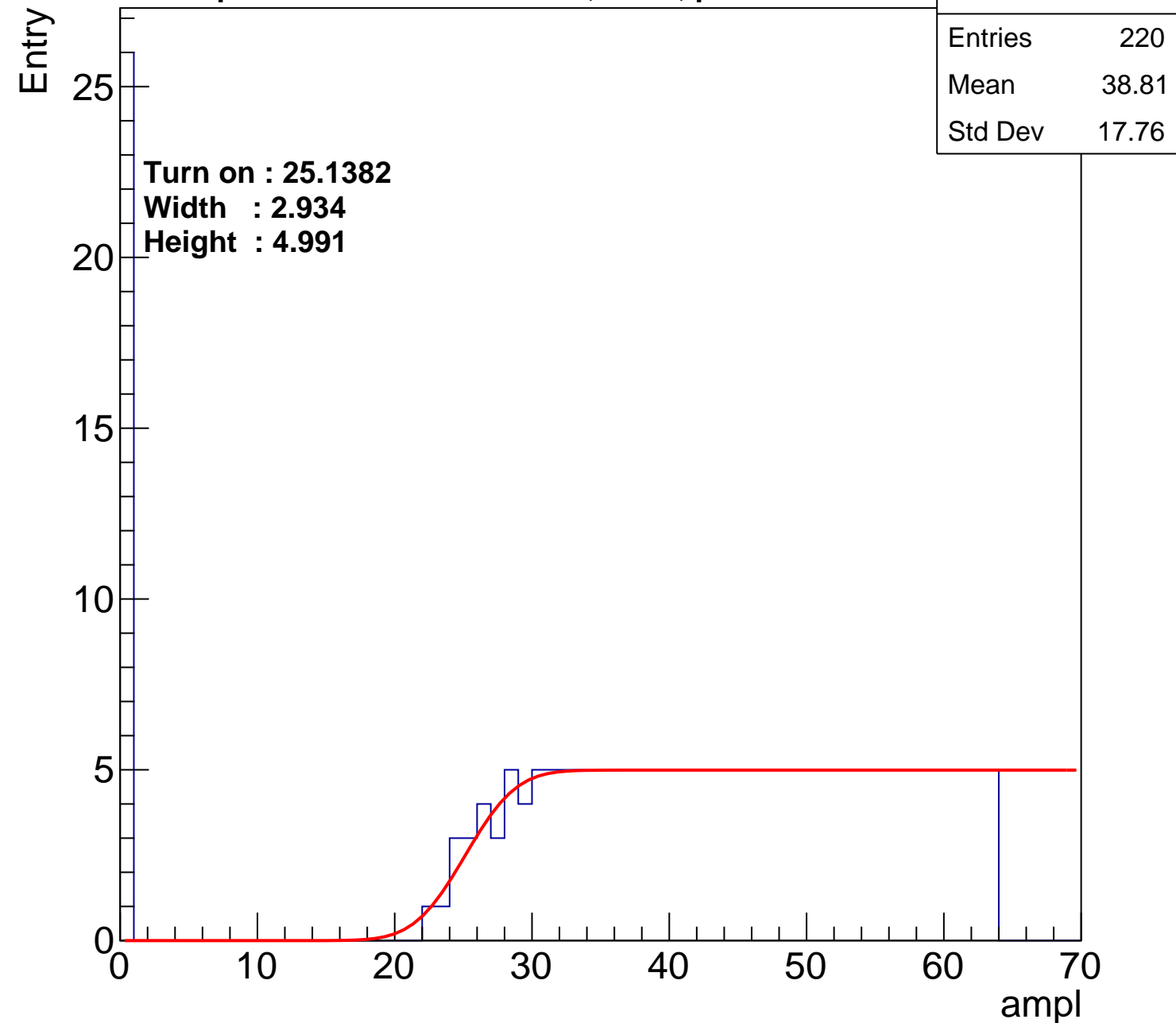
40

50

60

70

ampl



# B1L103S, U14-ch81

calib\_packv5\_041523\_1651.root, FC#0, port C2

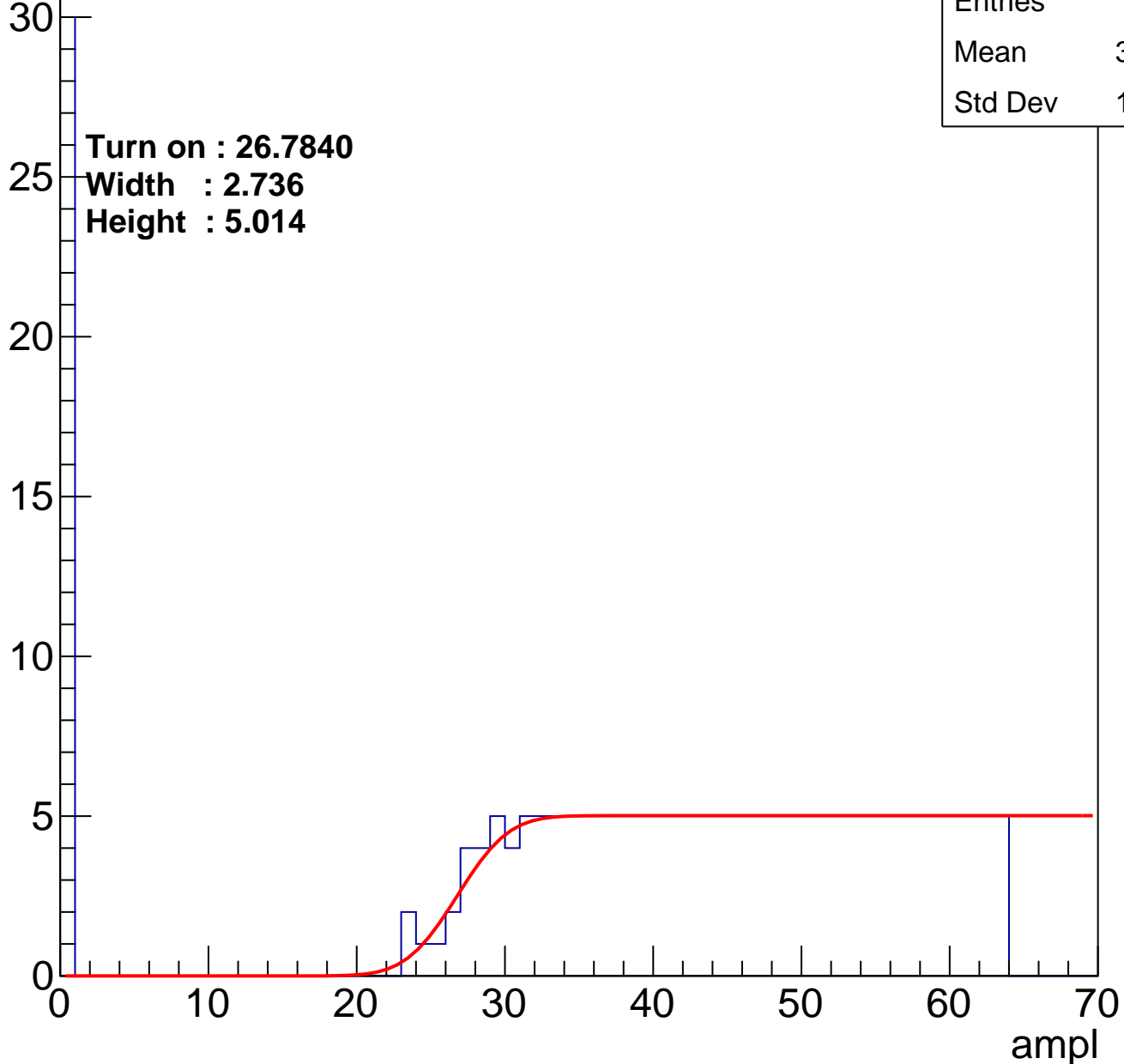
Entries	218
Mean	38.47
Std Dev	18.45

**Turn on : 26.7840**

**Width : 2.736**

**Height : 5.014**

Entry



# B1L103S, U14-ch82

calib\_packv5\_041523\_1651.root, FC#0, port C2

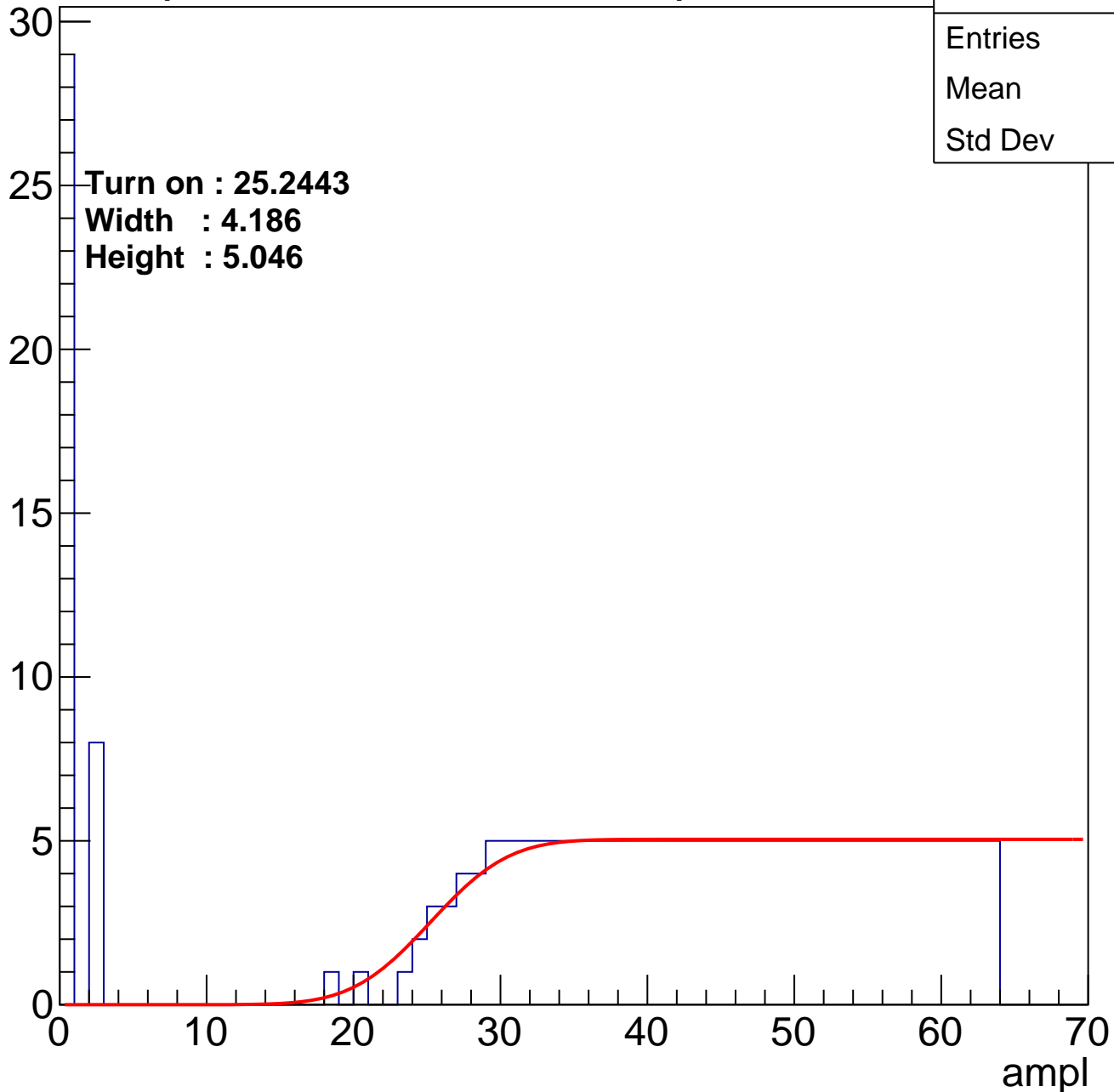
Entries	231
Mean	37
Std Dev	19.1

Turn on : 25.2443

Width : 4.186

Height : 5.046

Entry



# B1L103S, U14-ch83

calib\_packv5\_041523\_1651.root, FC#0, port C2

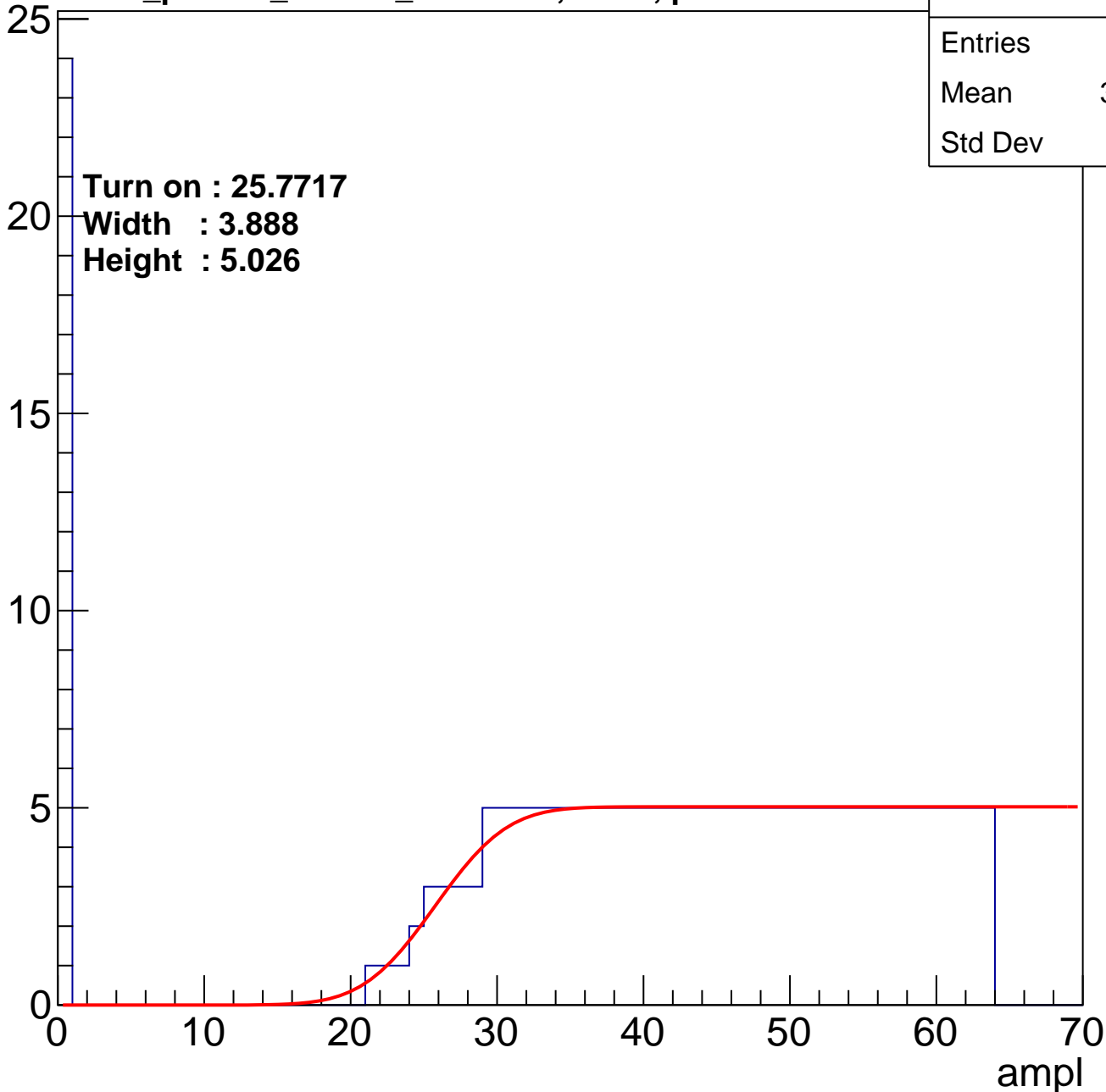
Entries	216
Mean	39.27
Std Dev	17.5

Turn on : 25.7717

Width : 3.888

Height : 5.026

Entry



# B1L103S, U14-ch84

calib\_packv5\_041523\_1651.root, FC#0, port C2

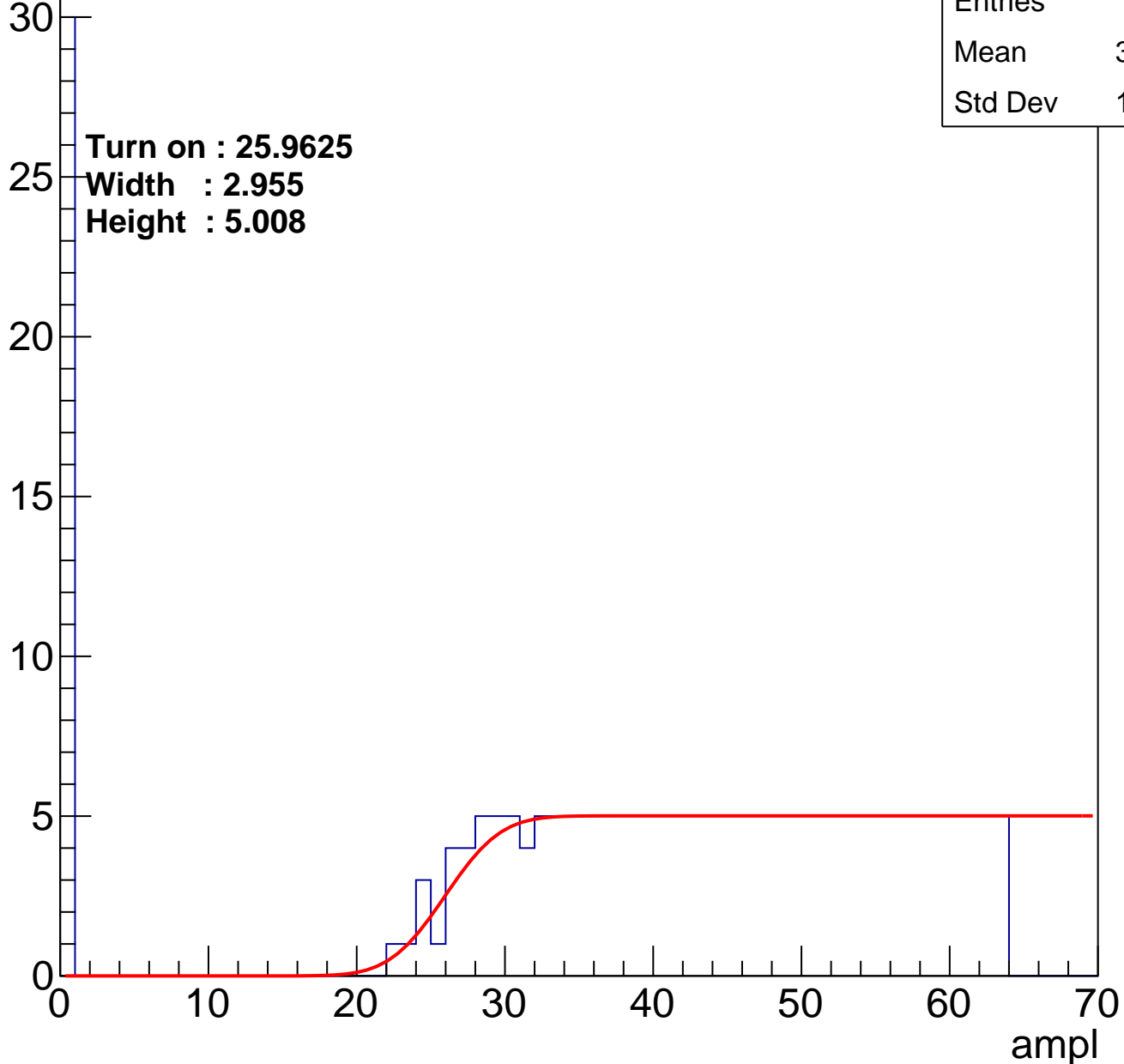
Entries	223
Mean	38.17
Std Dev	18.35

**Turn on : 25.9625**

**Width : 2.955**

**Height : 5.008**

Entry



# B1L103S, U14-ch85

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	213
Mean	39.19
Std Dev	17.92

**Turn on : 26.3502**

**Width : 4.527**

**Height : 5.020**

Entry

25

20

15

10

5

0

0

10

20

30

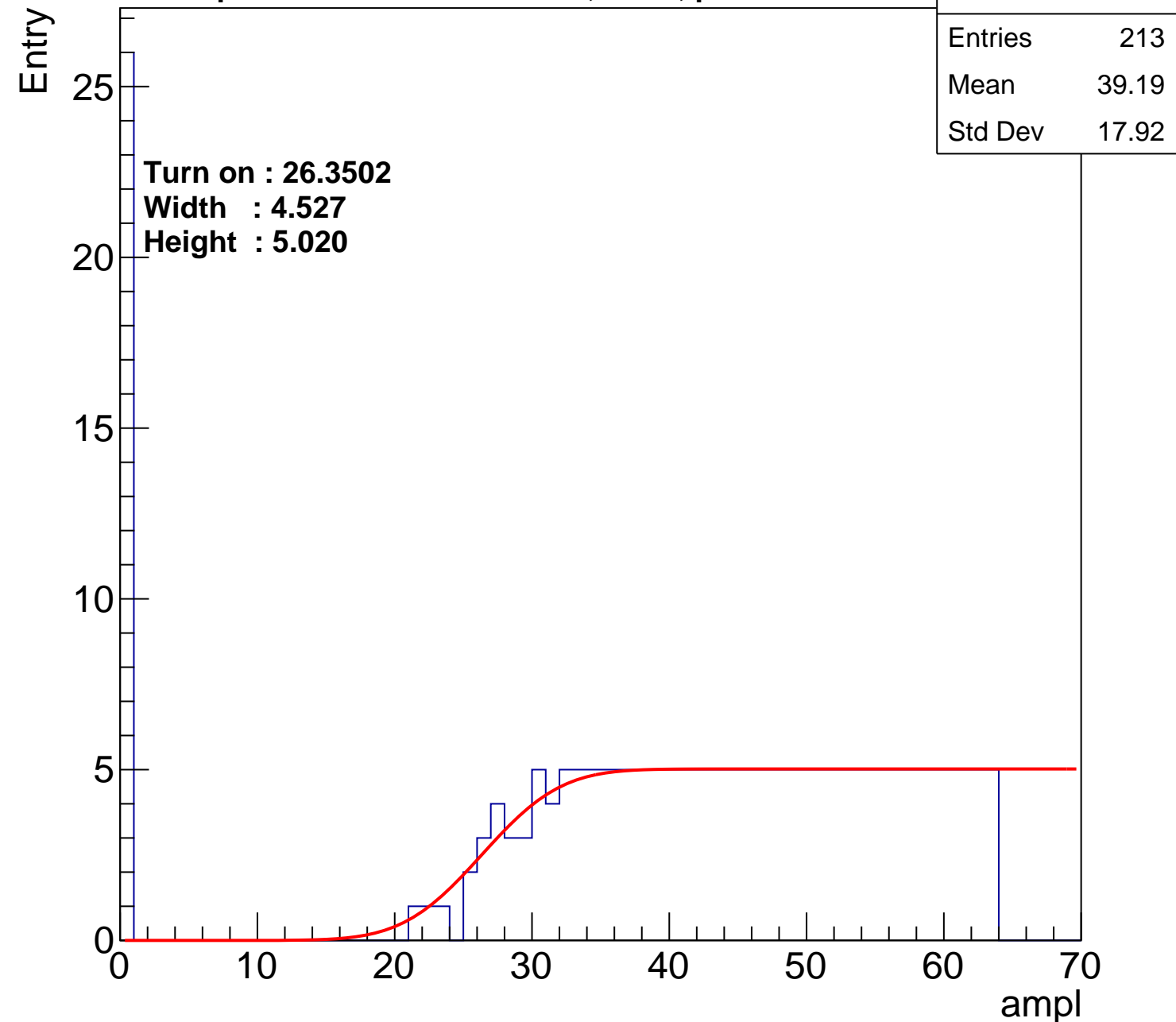
40

50

60

70

ampl



# B1L103S, U14-ch86

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	233
Mean	37.44
Std Dev	18.35

**Turn on : 23.1874**

**Width : 3.884**

**Height : 5.005**

Entry

30

25

20

15

10

5

0

0

10

20

30

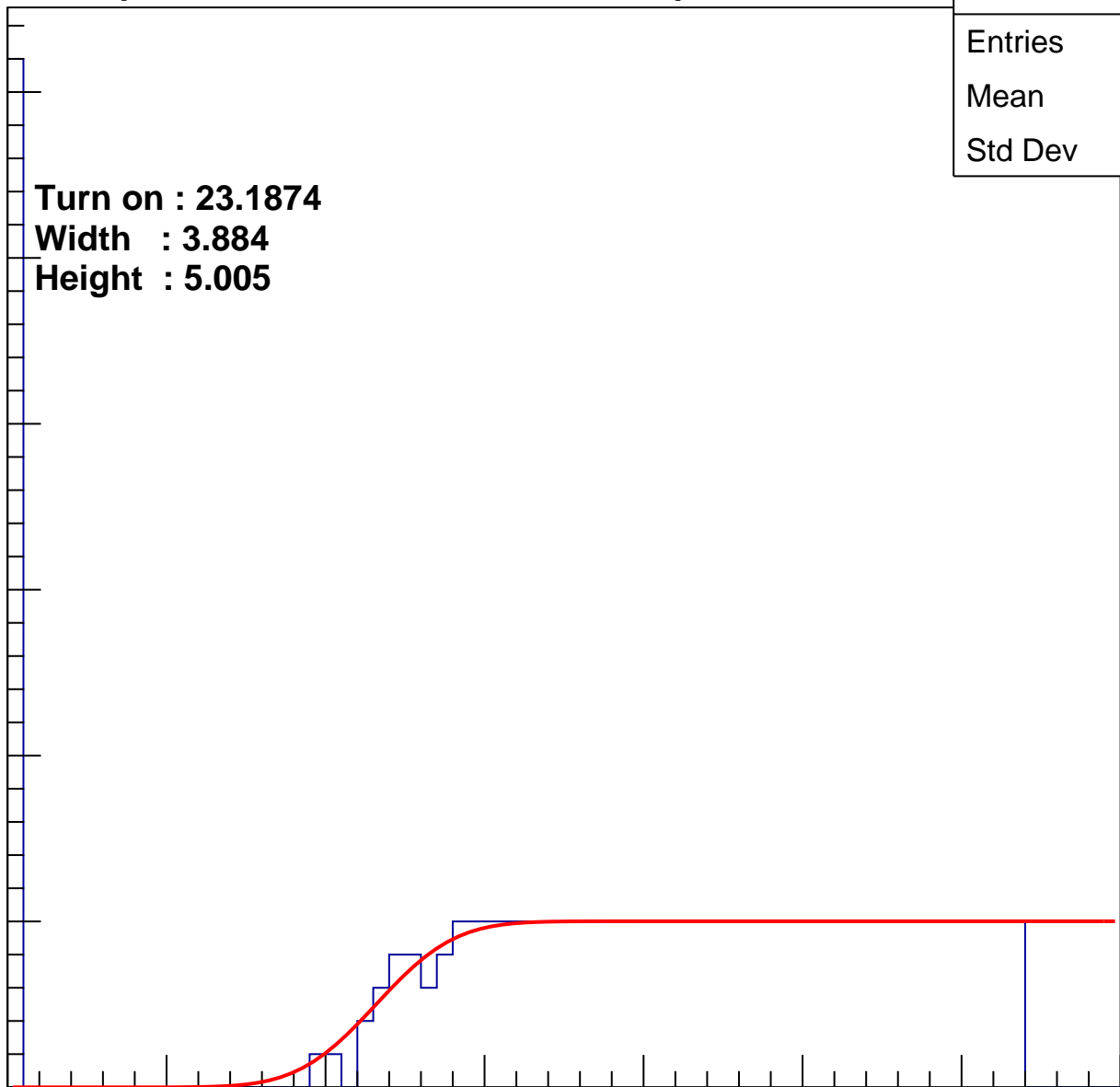
40

50

60

70

ampl





# B1L103S, U14-ch87

calib\_packv5\_041523\_1651.root, FC#0, port C2

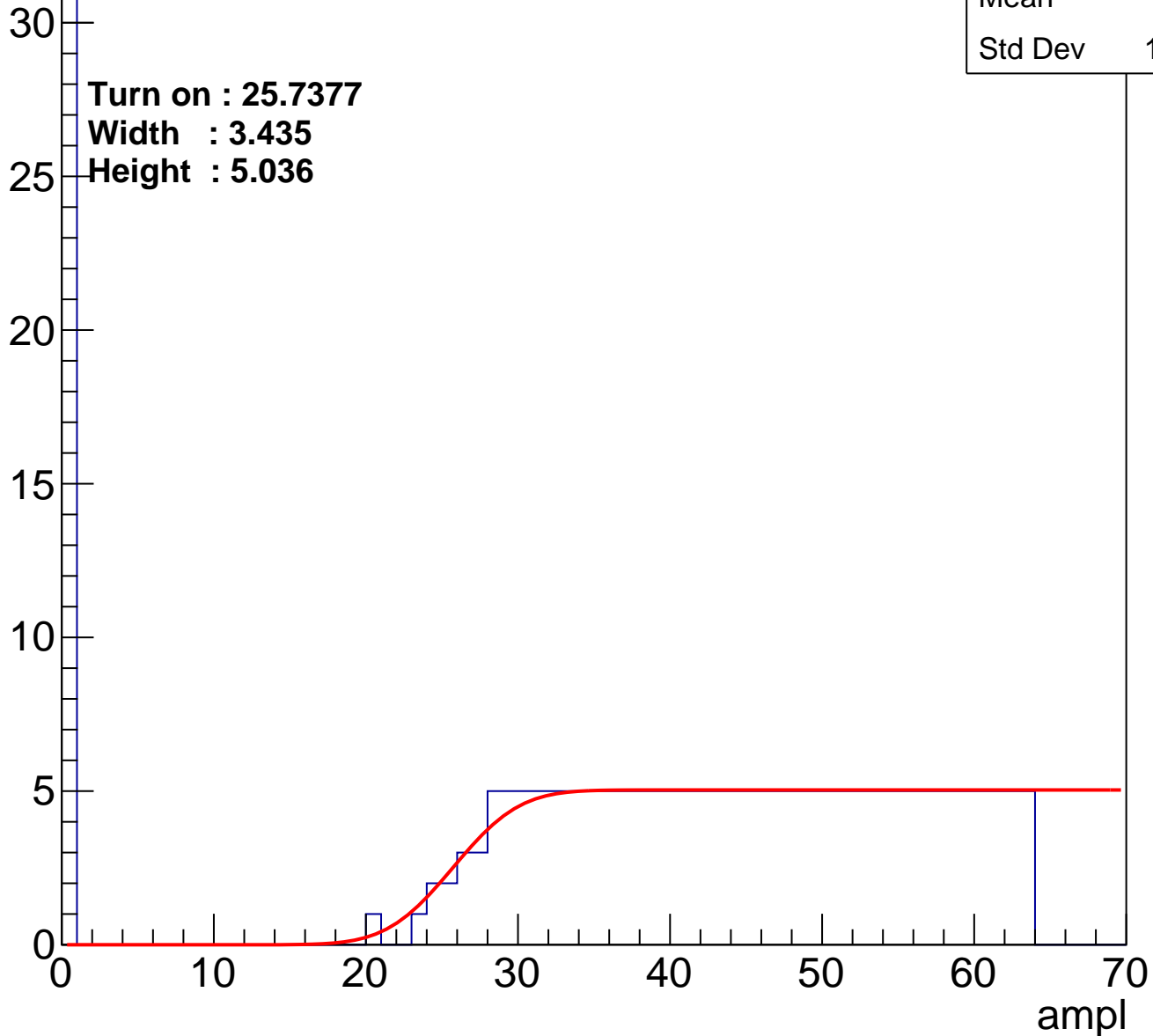
Entries	224
Mean	37.9
Std Dev	18.64

**Turn on : 25.7377**

**Width : 3.435**

**Height : 5.036**

Entry



# B1L103S, U14-ch88

calib\_packv5\_041523\_1651.root, FC#0, port C2

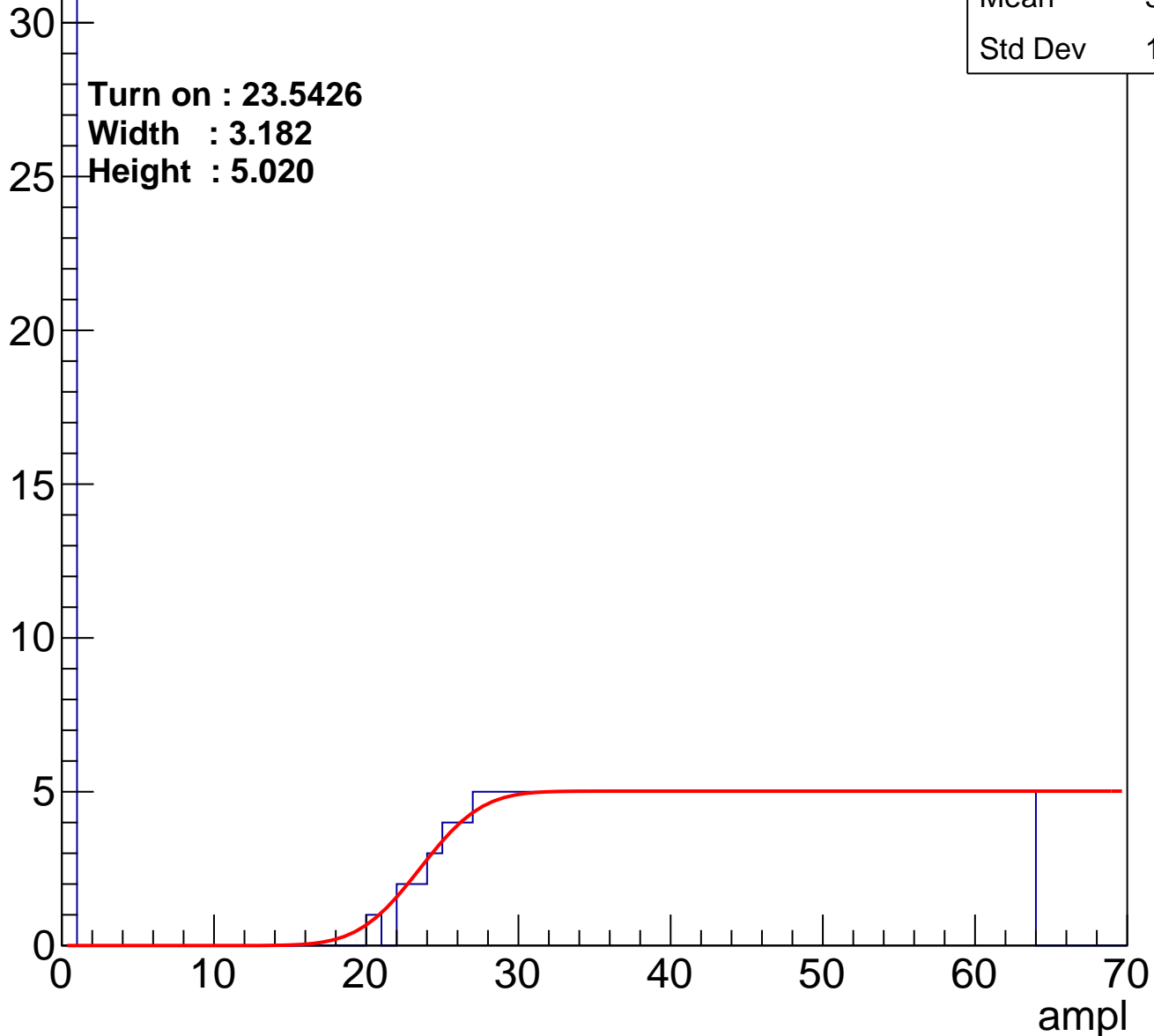
Entries	233
Mean	37.39
Std Dev	18.46

**Turn on : 23.5426**

**Width : 3.182**

**Height : 5.020**

Entry



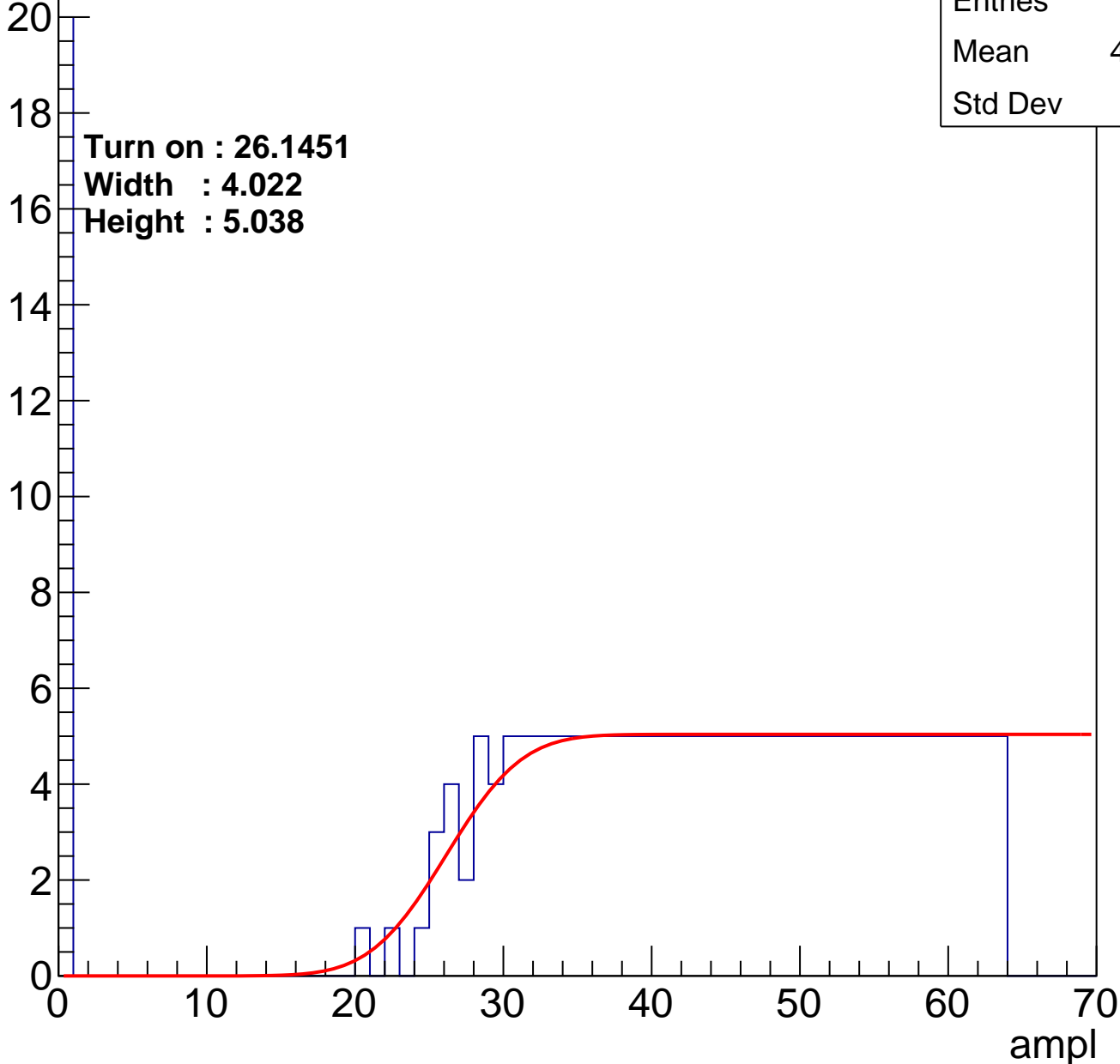
# B1L103S, U14-ch89

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	211
Mean	40.09
Std Dev	16.8

**Turn on : 26.1451**  
**Width : 4.022**  
**Height : 5.038**

Entry



# B1L103S, U14-ch90

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	225
Mean	38.59
Std Dev	17.54

**Turn on : 24.3313**

**Width : 3.142**

**Height : 5.024**

Entry

25

20

15

10

5

0

ampl

0

10

20

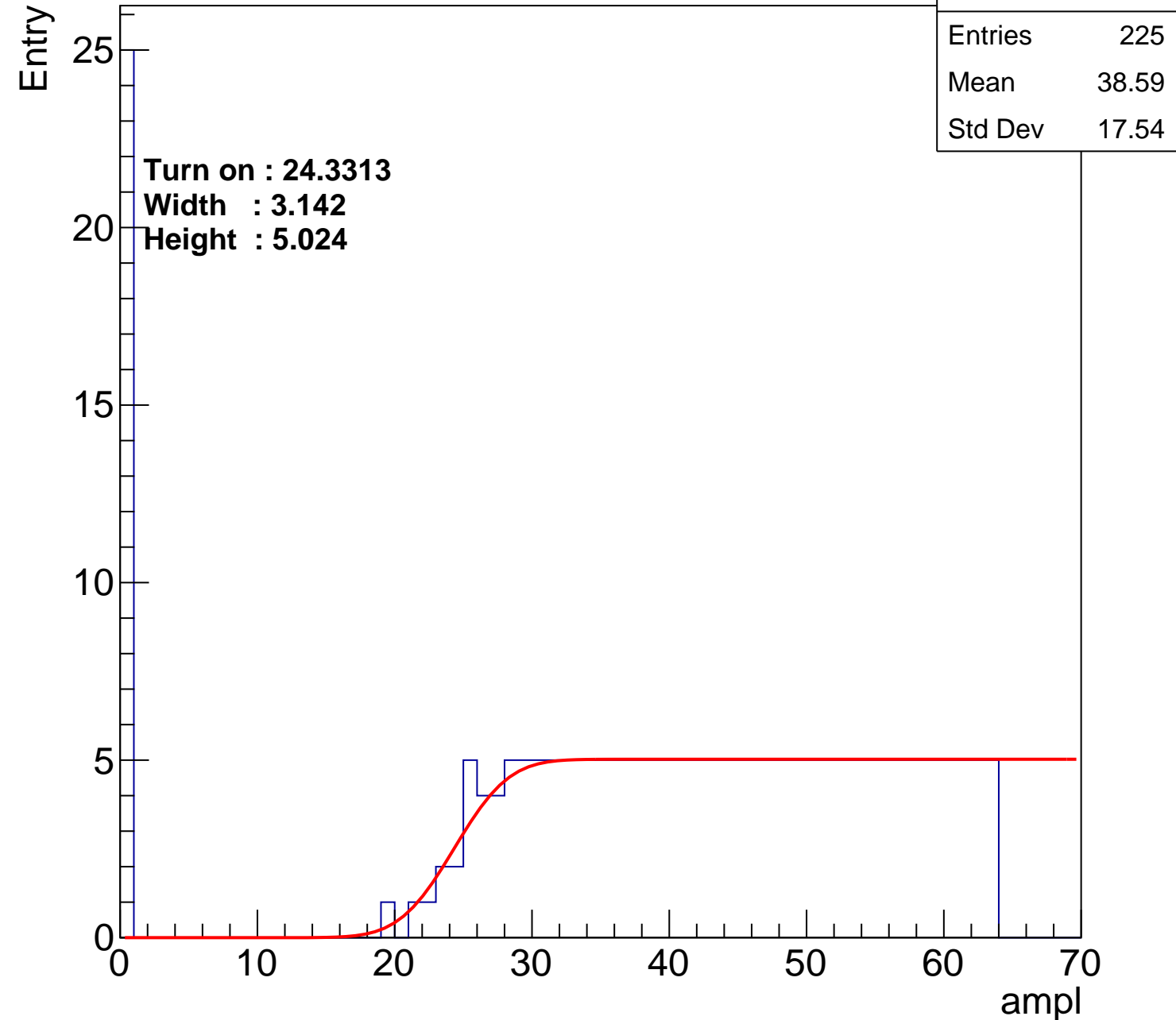
30

40

50

60

70



# B1L103S, U14-ch91

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	217
Mean	38.85
Std Dev	18

**Turn on : 26.3270**

**Width : 4.058**

**Height : 5.029**

Entry

25

20

15

10

5

0

0

10

20

30

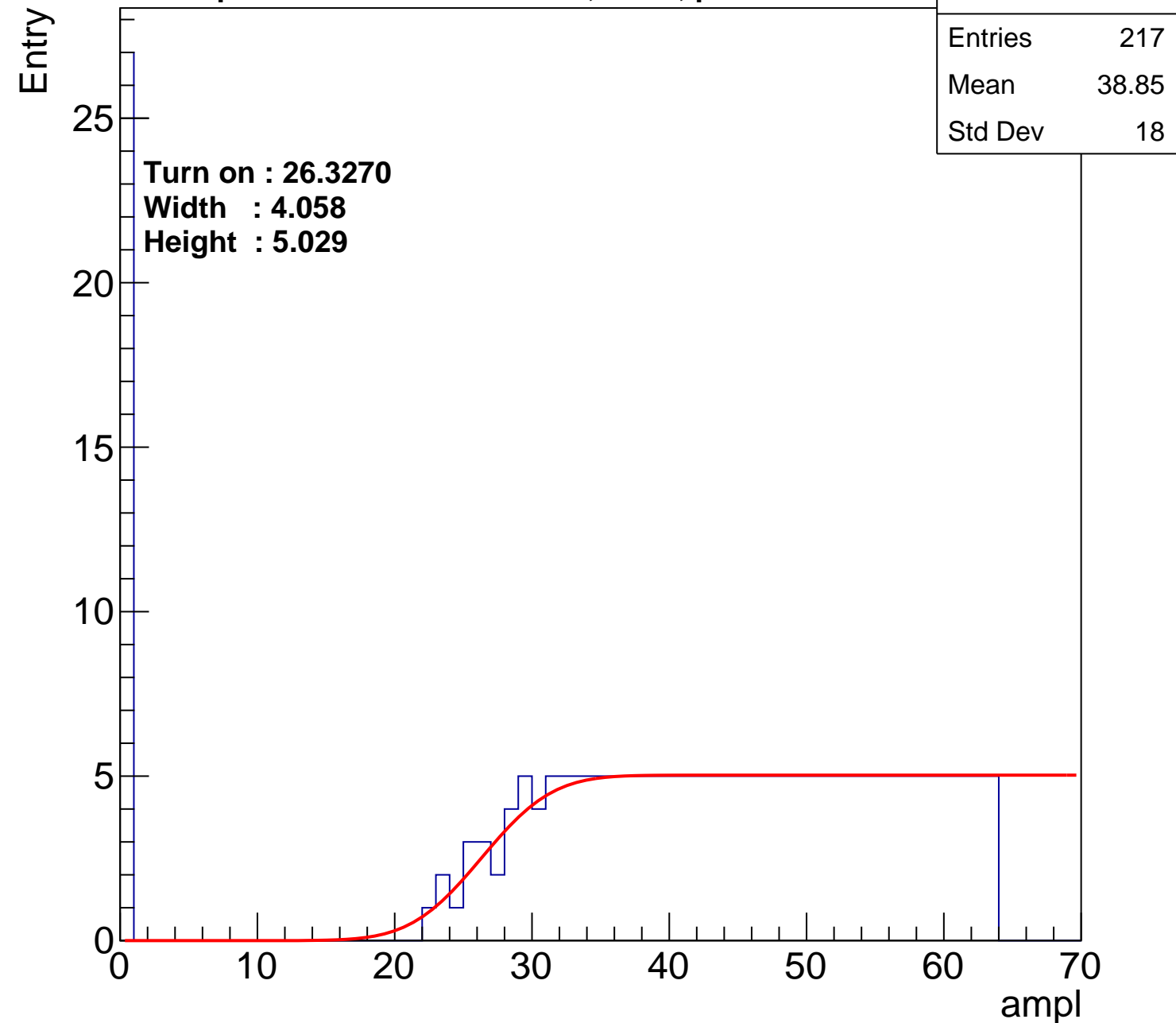
40

50

60

ampl

70



# B1L103S, U14-ch92

calib\_packv5\_041523\_1651.root, FC#0, port C2

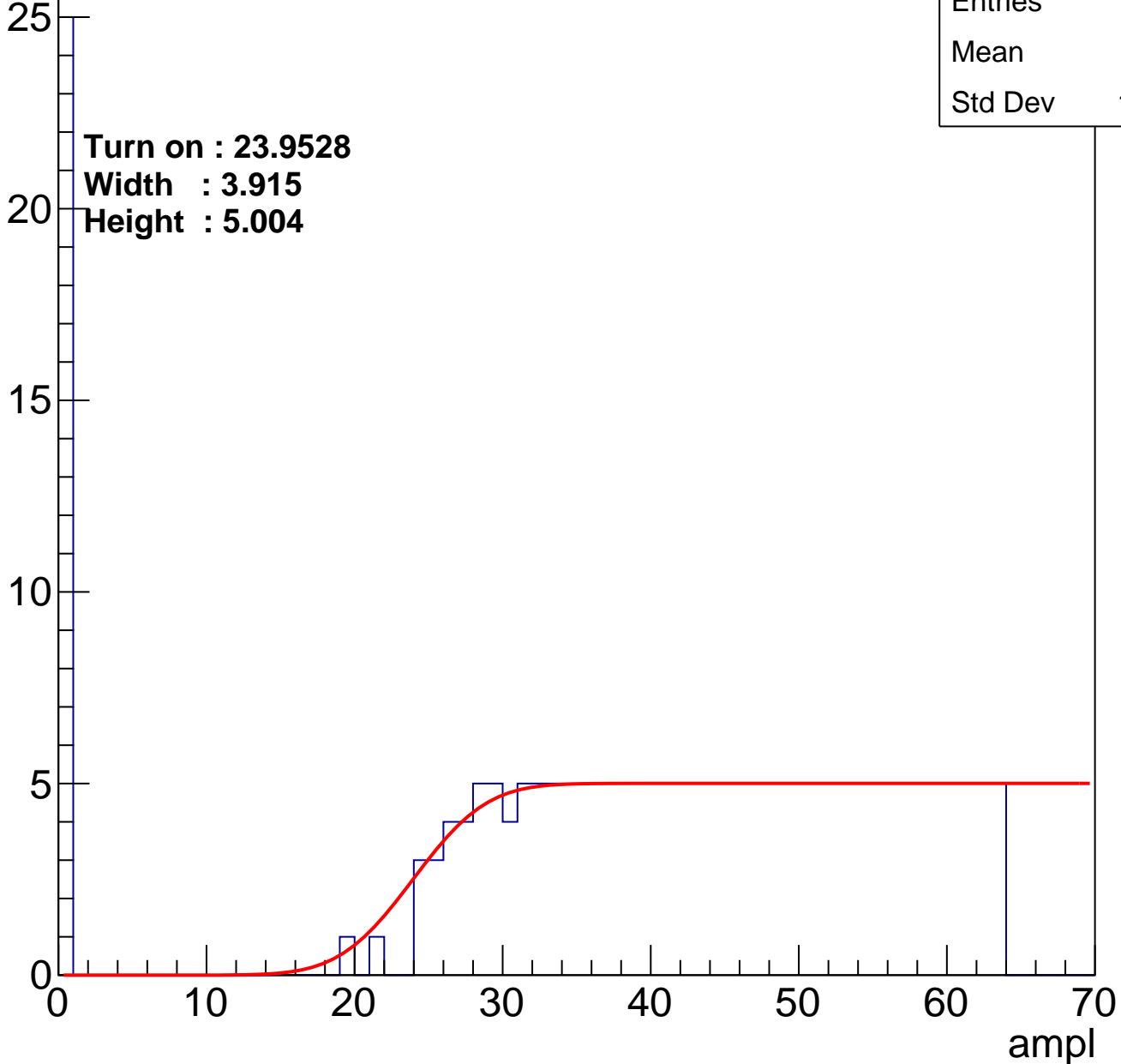
Entries	220
Mean	38.9
Std Dev	17.61

Turn on : 23.9528

Width : 3.915

Height : 5.004

Entry



# B1L103S, U14-ch93

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	225
Mean	38.33
Std Dev	17.89

**Turn on : 23.6026**

**Width : 4.960**

**Height : 5.021**

Entry

25

20

15

10

5

0

0

10

20

30

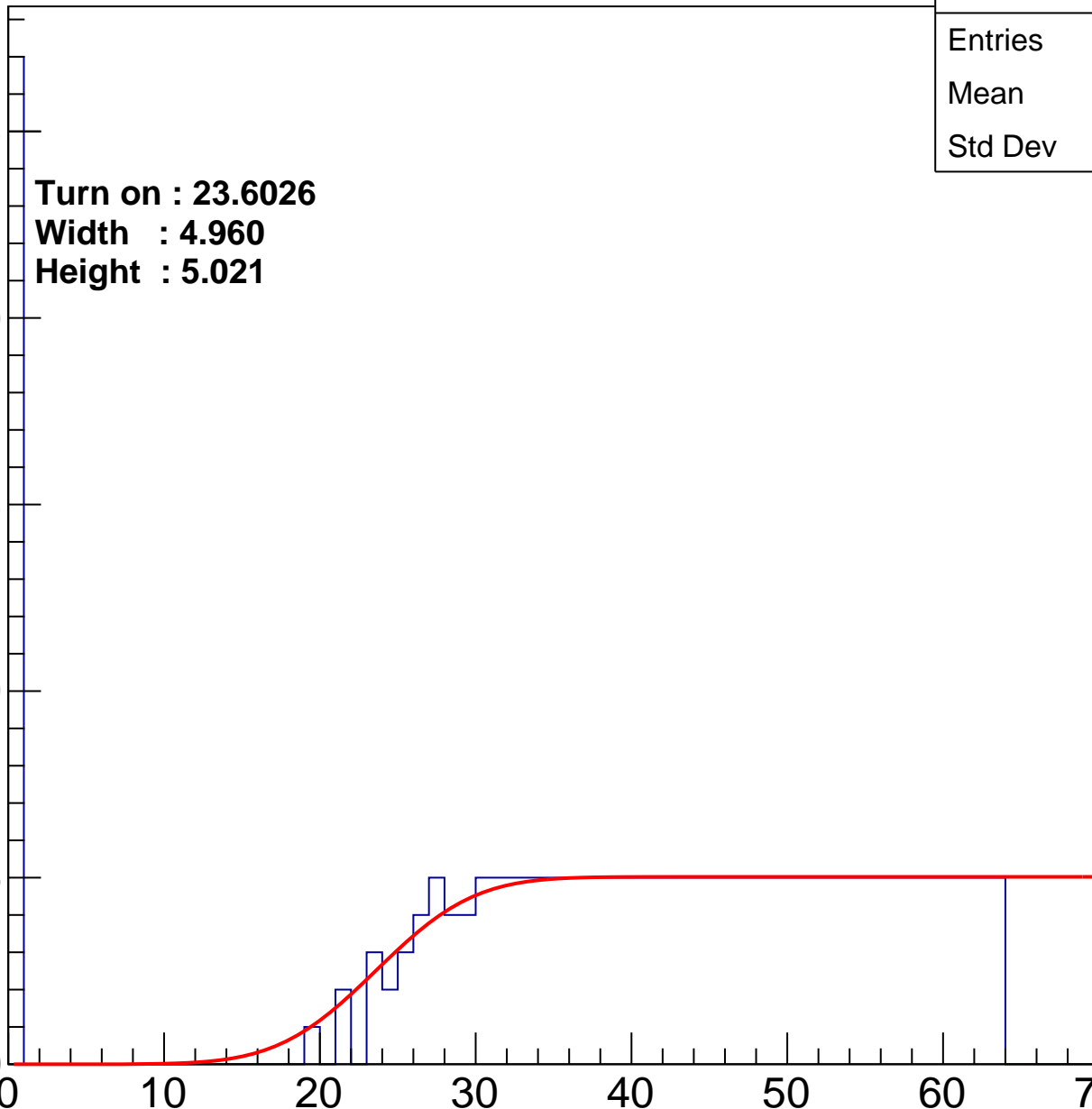
40

50

60

70

ampl



# B1L103S, U14-ch94

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	224
Mean	38.46
Std Dev	17.78

**Turn on : 24.0824**

**Width : 5.035**

**Height : 5.017**

Entry

25

20

15

10

5

0

0

10

20

30

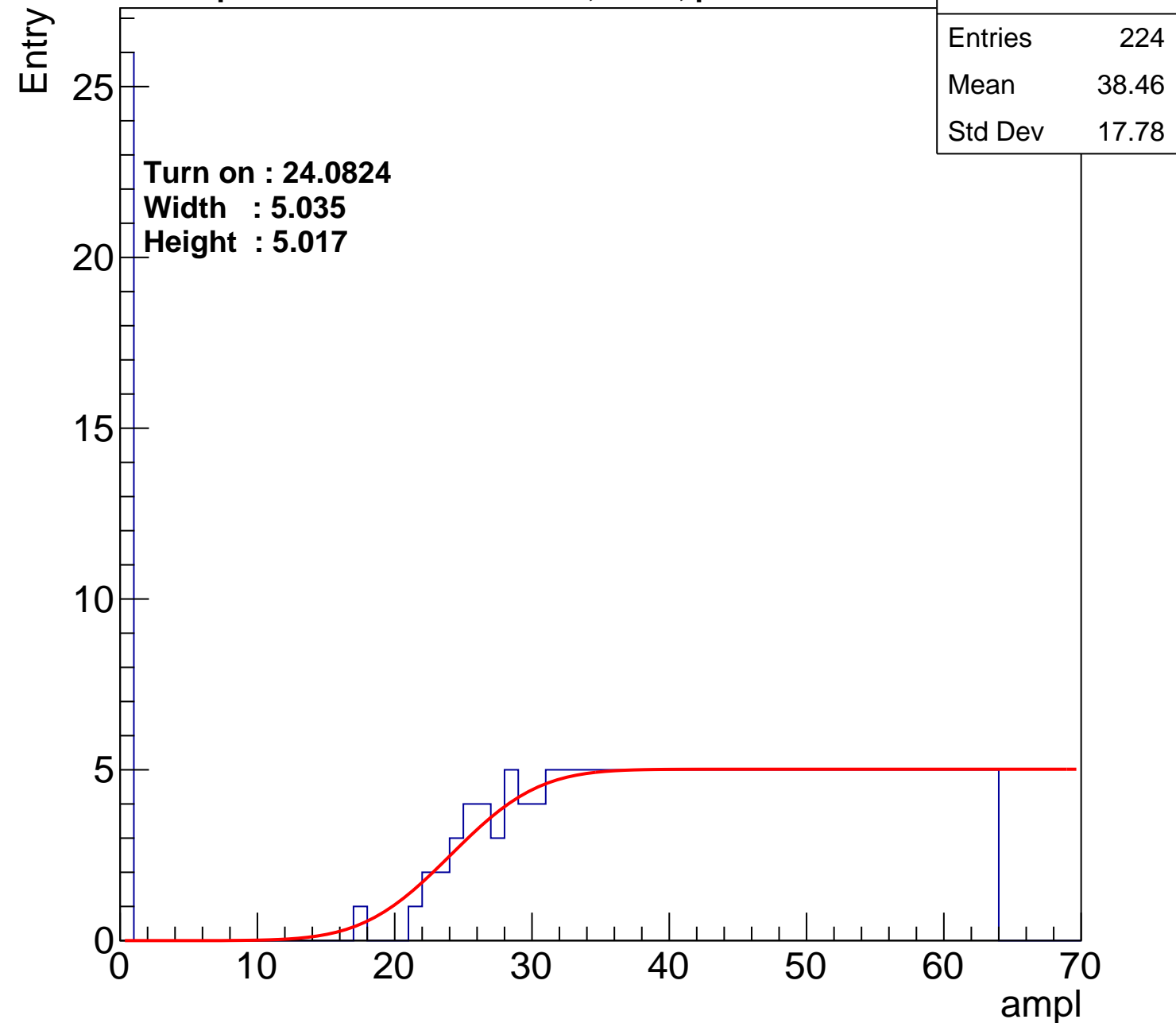
40

50

60

70

ampl





# B1L103S, U14-ch95

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	217
Mean	38.98
Std Dev	17.82

**Turn on : 25.8455**

**Width : 2.354**

**Height : 4.978**

Entry

25

20

15

10

5

0

0

10

20

30

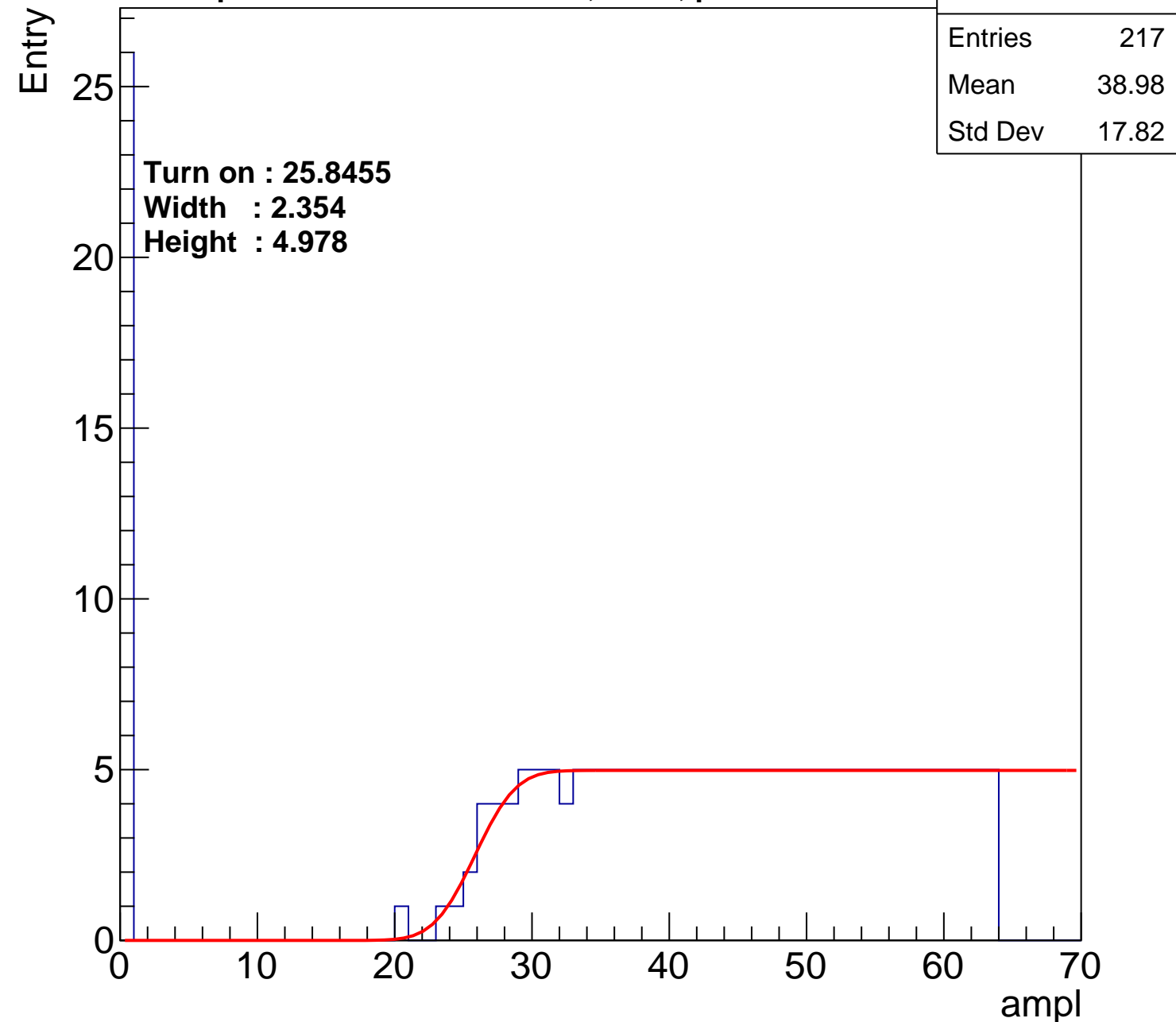
40

50

60

70

ampl



# B1L103S, U14-ch96

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	233
Mean	37.23
Std Dev	18.64

**Turn on : 24.4650**

**Width : 4.261**

**Height : 5.039**

Entry

30

25

20

15

10

5

0

ampl

0

10

20

30

40

50

60

70

# B1L103S, U14-ch97

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	234
Mean	36.67
Std Dev	19.28

Turn on : 25.1791

Width : 3.613

Height : 5.024

Entry

35

30

25

20

15

10

5

0

0

10

20

30

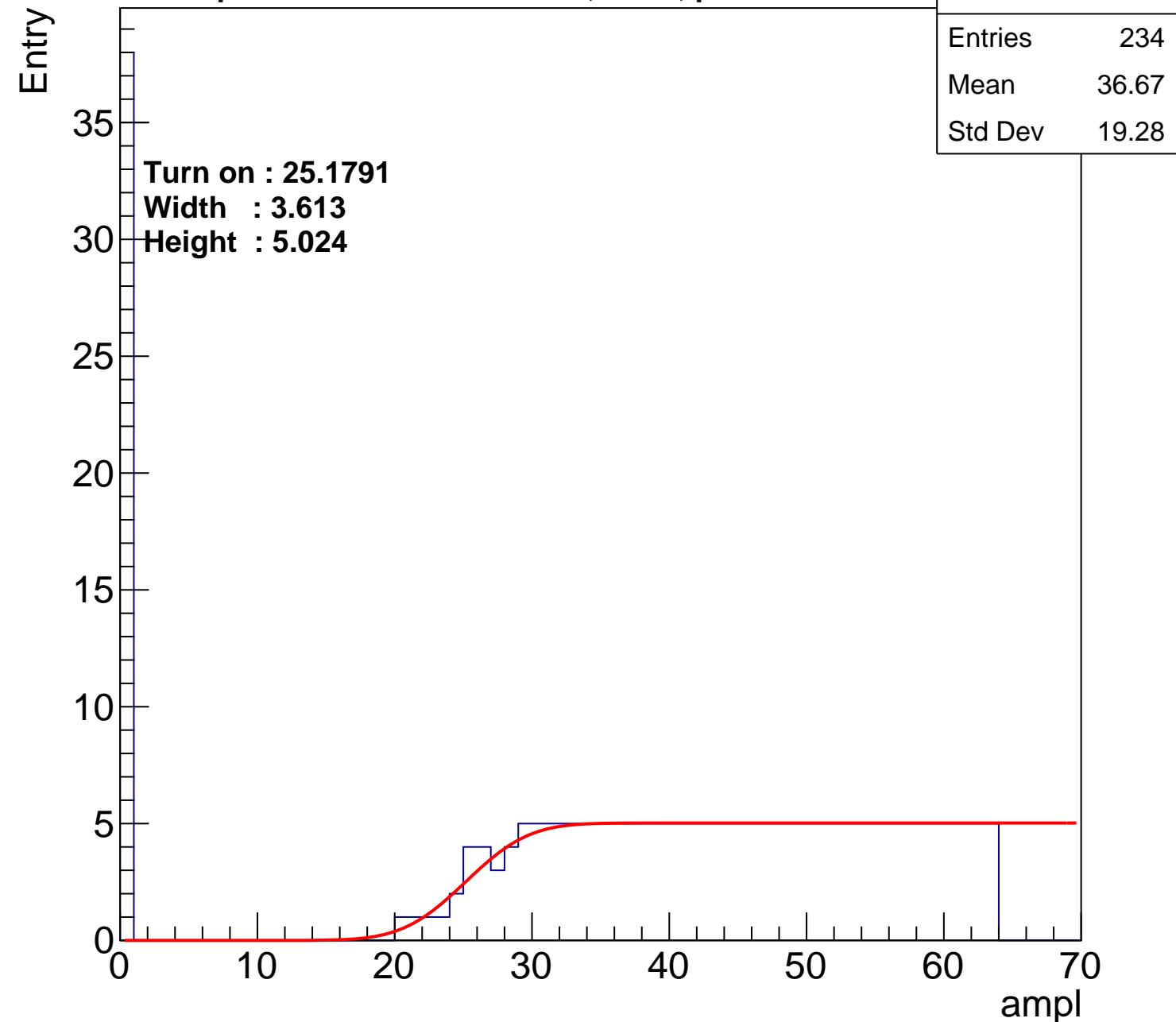
40

50

60

70

ampl



# B1L103S, U14-ch98

calib\_packv5\_041523\_1651.root, FC#0, port C2

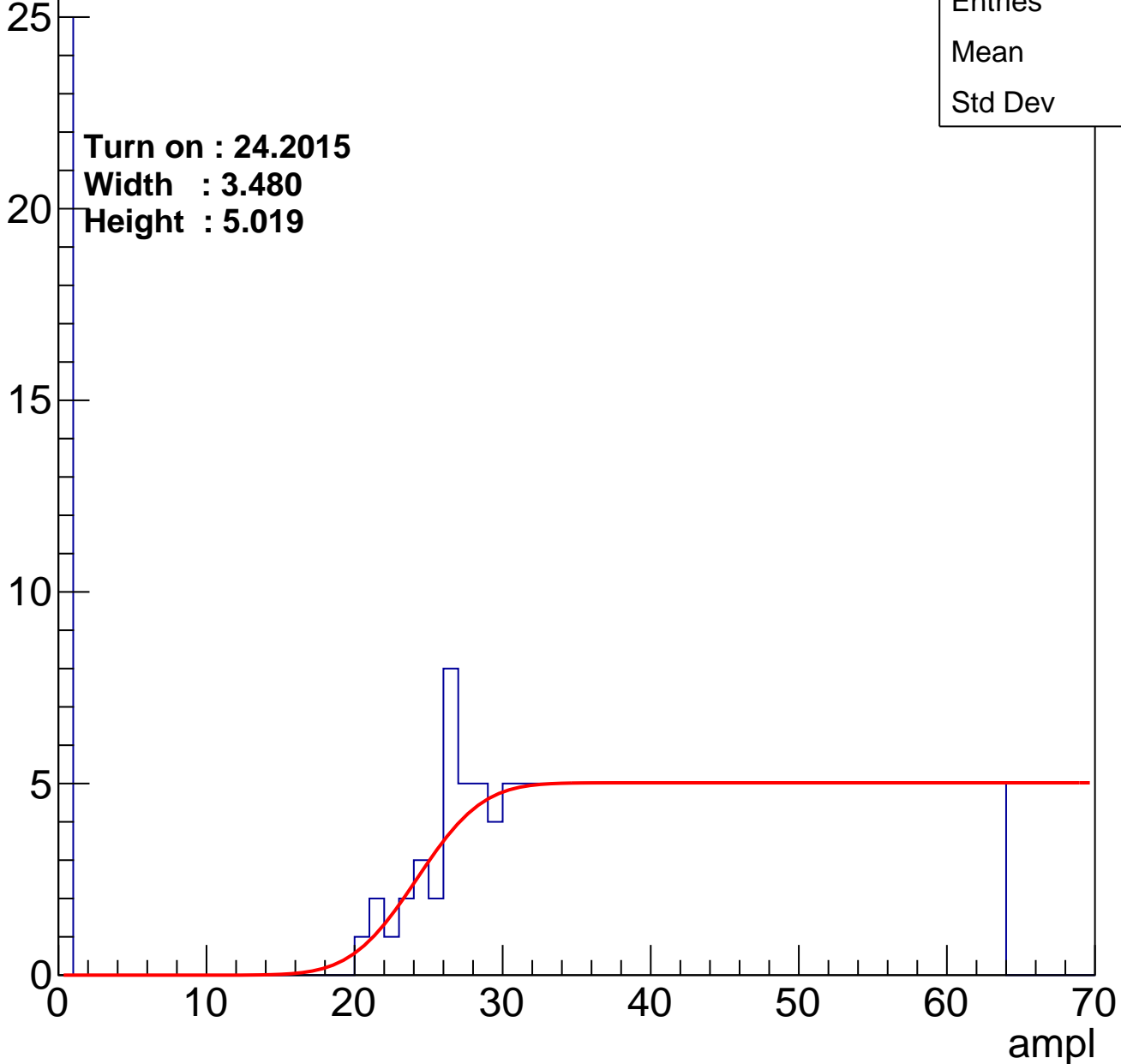
Entries	228
Mean	38.4
Std Dev	17.5

Turn on : 24.2015

Width : 3.480

Height : 5.019

Entry

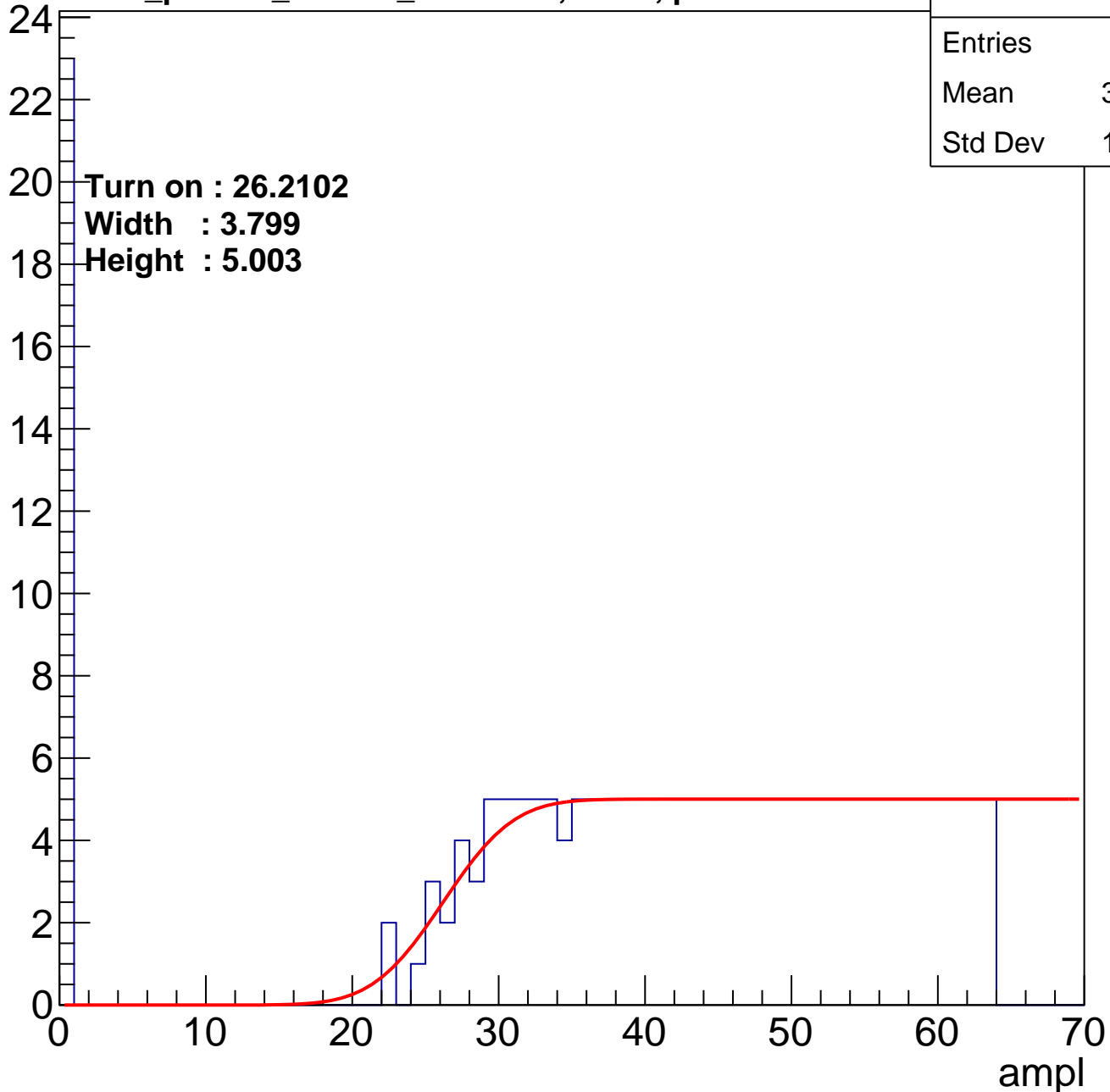


# B1L103S, U14-ch99

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	212
Mean	39.64
Std Dev	17.37

Entry



# B1L103S, U14-ch100

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	223
Mean	38.15
Std Dev	18.38

**Turn on : 25.7850**

**Width : 4.155**

**Height : 5.043**

Entry

30

25

20

15

10

5

0

0

10

20

30

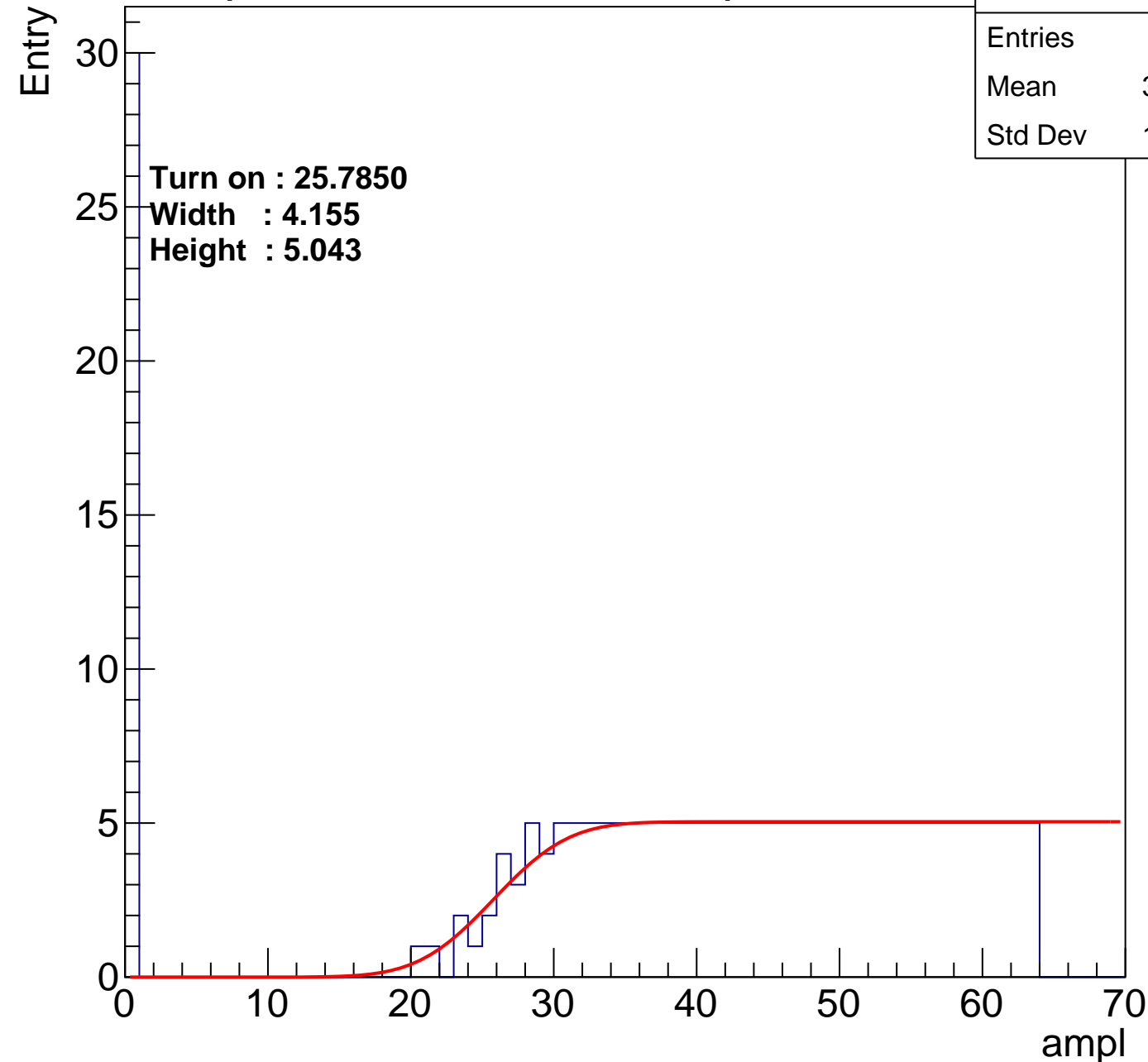
40

50

60

70

ampl



# B1L103S, U14-ch101

calib\_packv5\_041523\_1651.root, FC#0, port C2

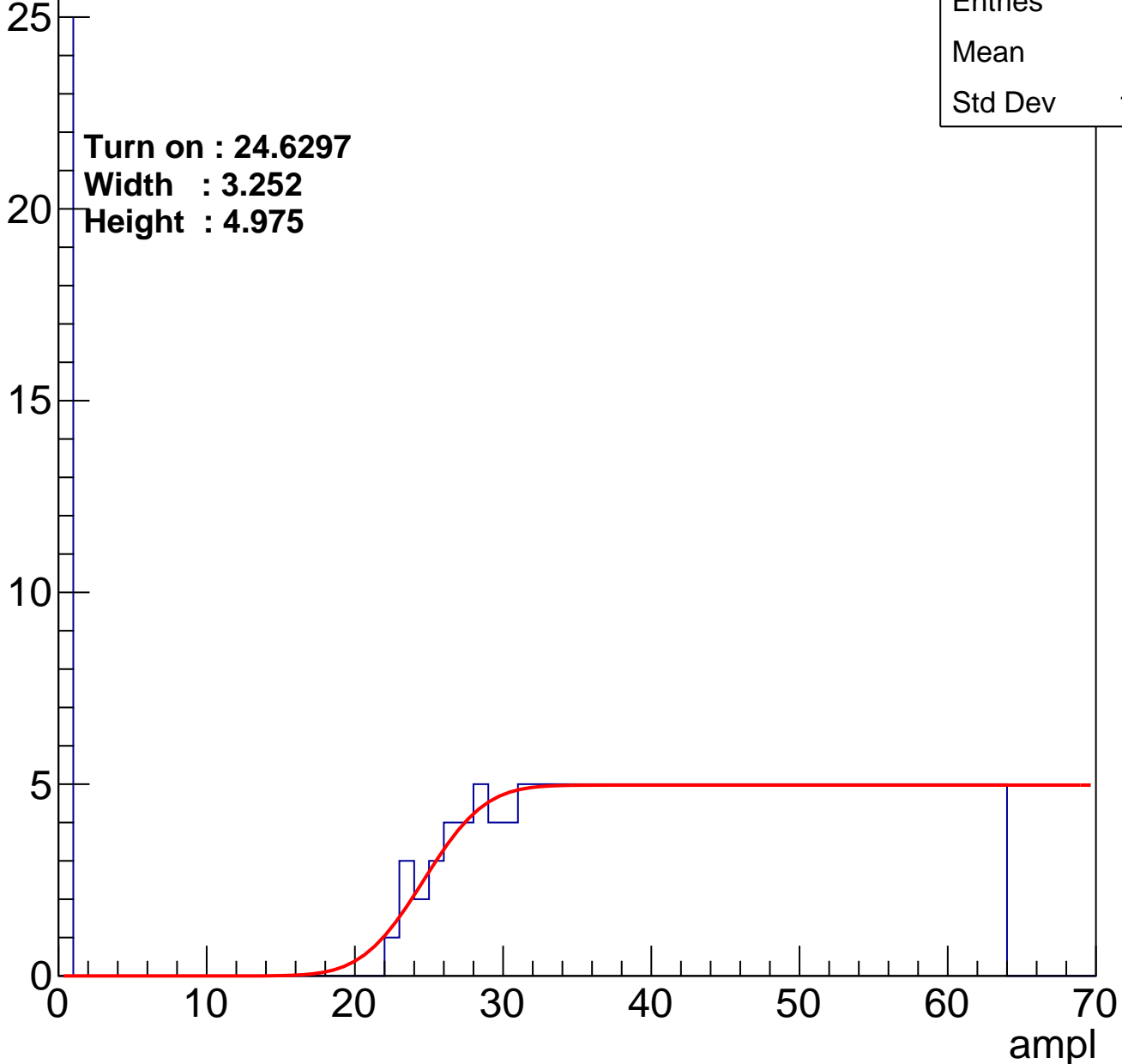
Entries	220
Mean	38.9
Std Dev	17.61

**Turn on : 24.6297**

**Width : 3.252**

**Height : 4.975**

Entry



# B1L103S, U14-ch102

calib\_packv5\_041523\_1651.root, FC#0, port C2

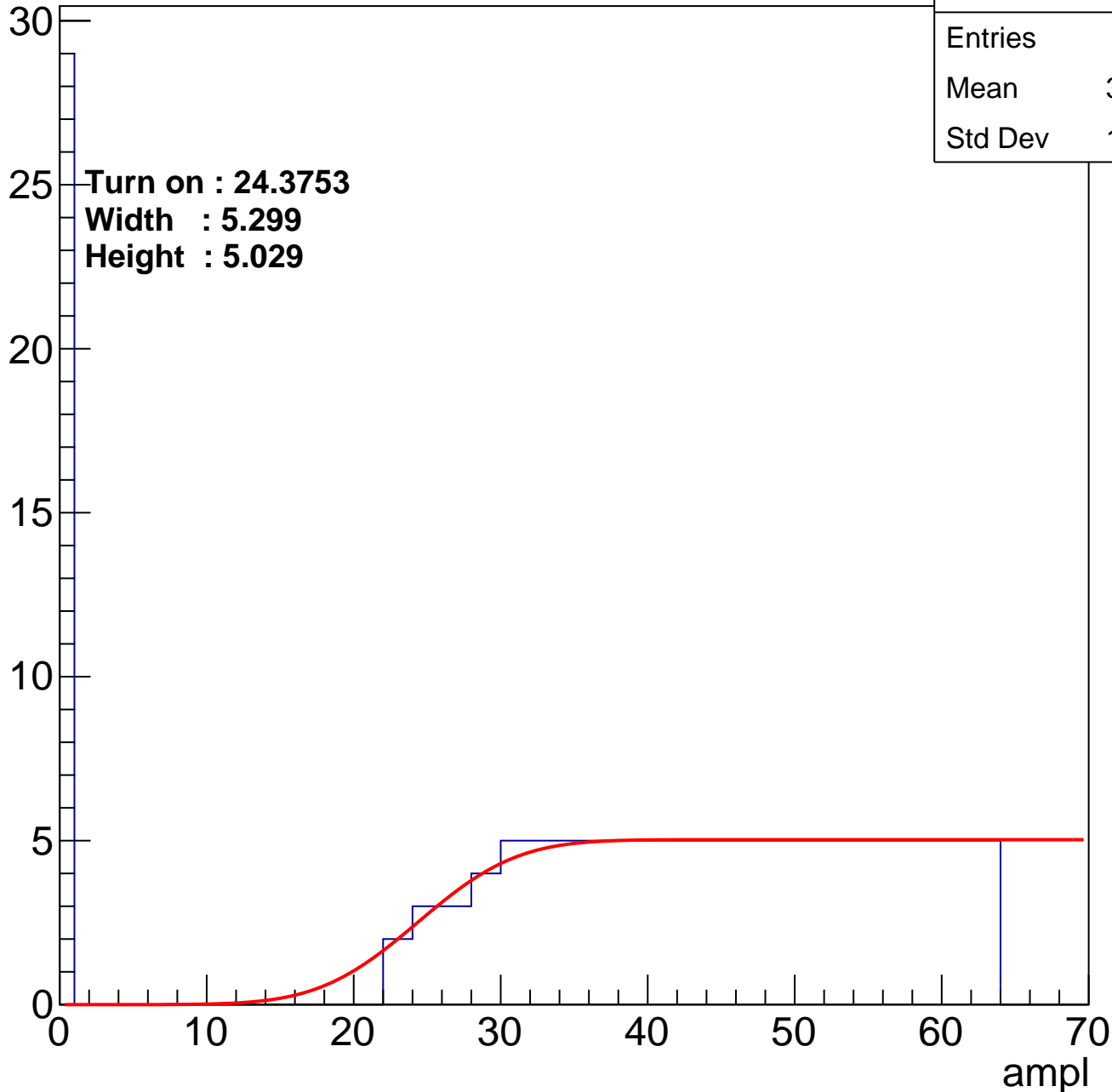
Entries	223
Mean	38.25
Std Dev	18.23

Turn on : 24.3753

Width : 5.299

Height : 5.029

Entry





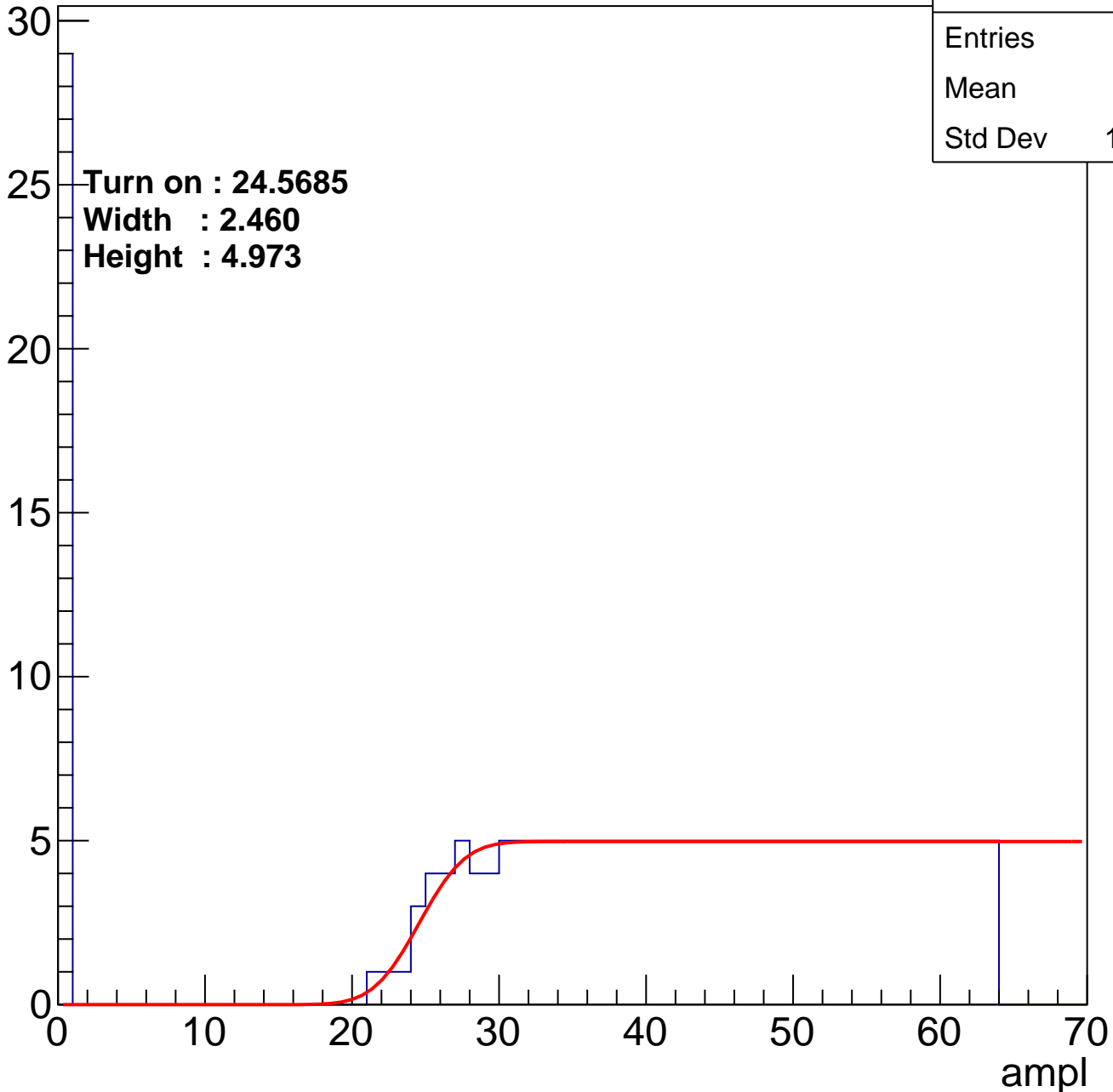
# B1L103S, U14-ch103

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	226
Mean	38.1
Std Dev	18.15

Turn on : 24.5685  
Width : 2.460  
Height : 4.973

Entry



# B1L103S, U14-ch104

calib\_packv5\_041523\_1651.root, FC#0, port C2

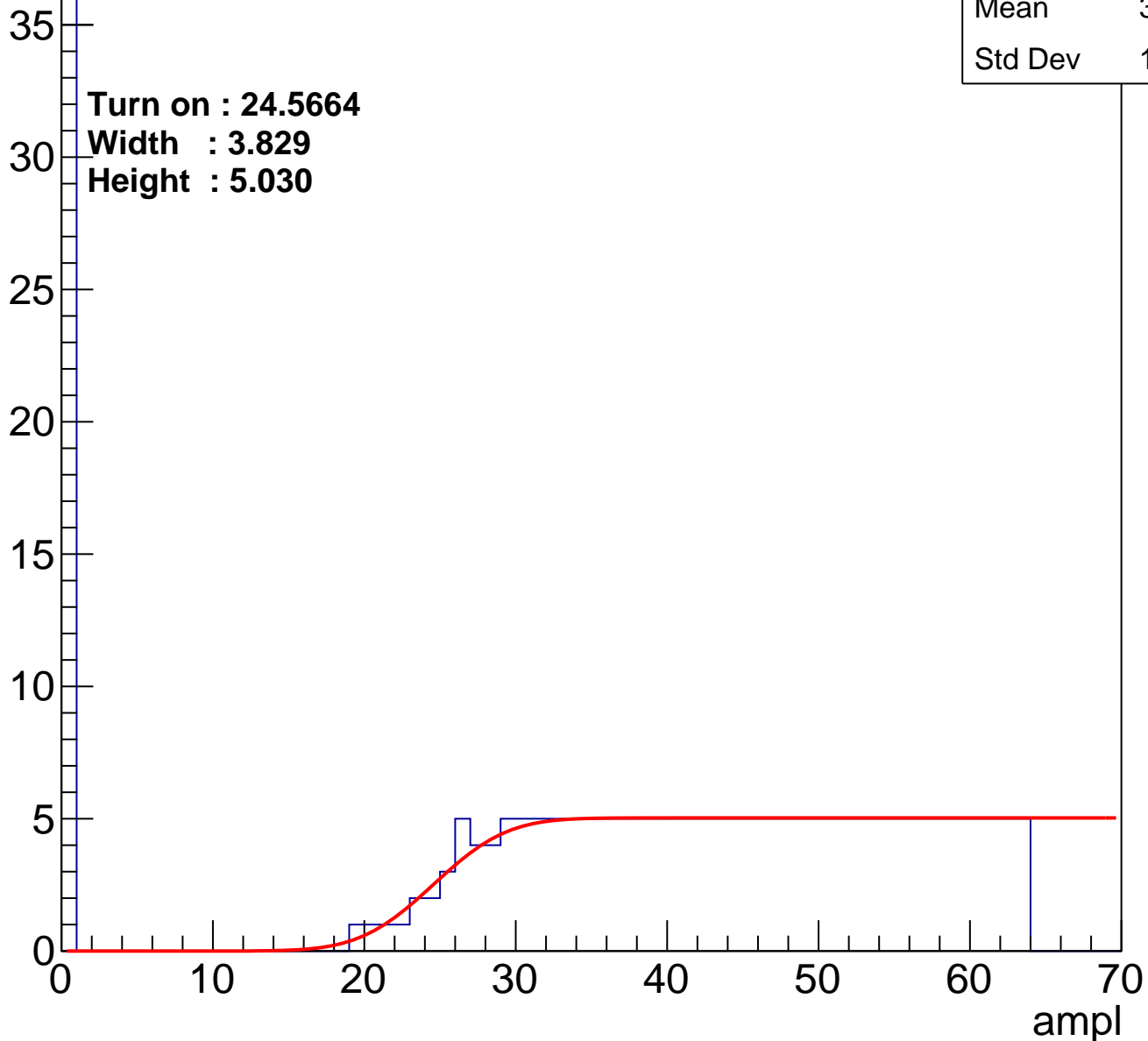
Entries	236
Mean	36.66
Std Dev	19.12

**Turn on : 24.5664**

**Width : 3.829**

**Height : 5.030**

Entry



# B1L103S, U14-ch105

calib\_packv5\_041523\_1651.root, FC#0, port C2

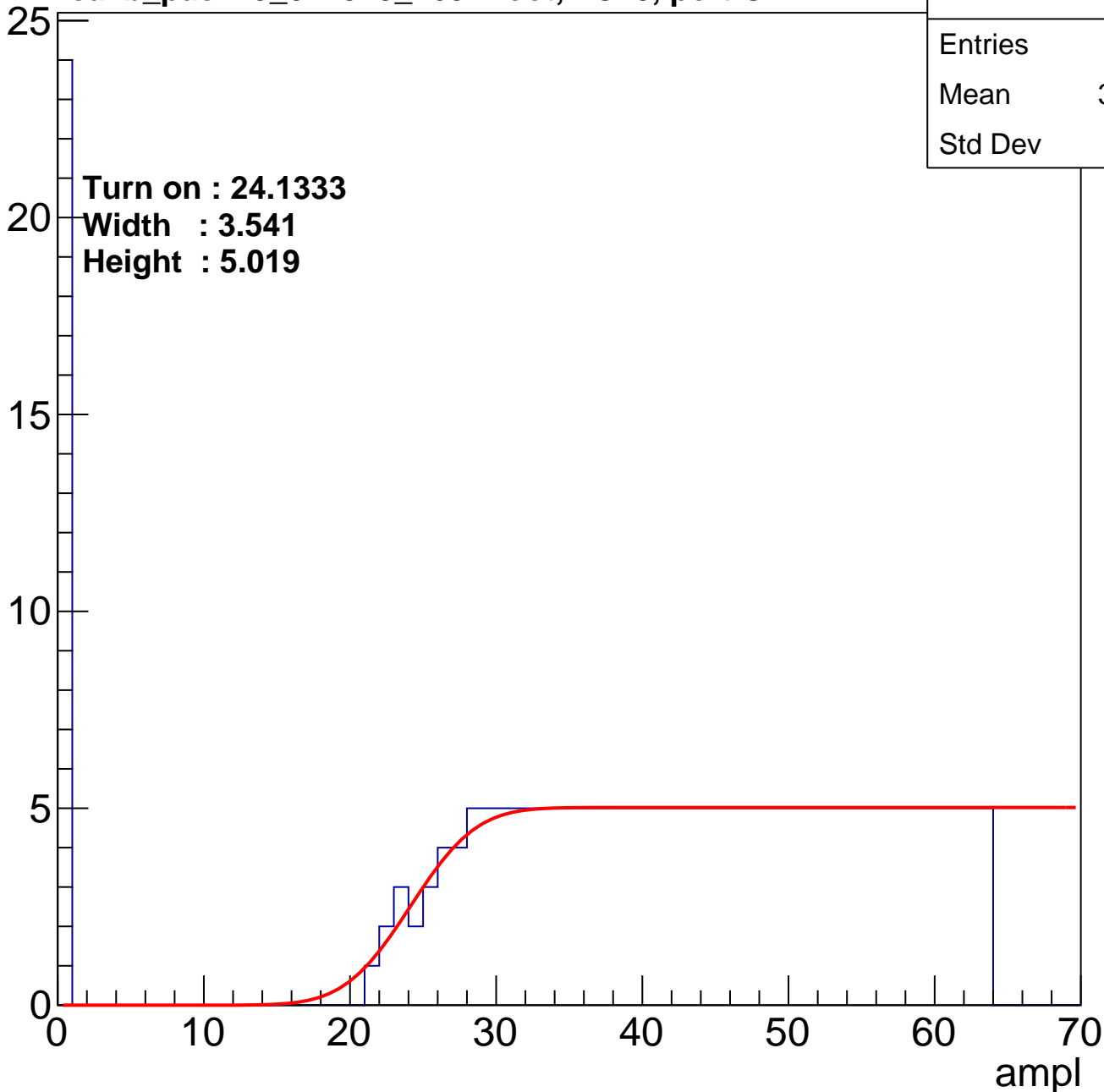
Entries	223
Mean	38.83
Std Dev	17.4

Turn on : 24.1333

Width : 3.541

Height : 5.019

Entry



# B1L103S, U14-ch106

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	229
Mean	38
Std Dev	17.97

**Turn on : 23.2999**  
**Width : 4.459**  
**Height : 5.012**

Entry

25

20

15

10

5

0

0

10

20

30

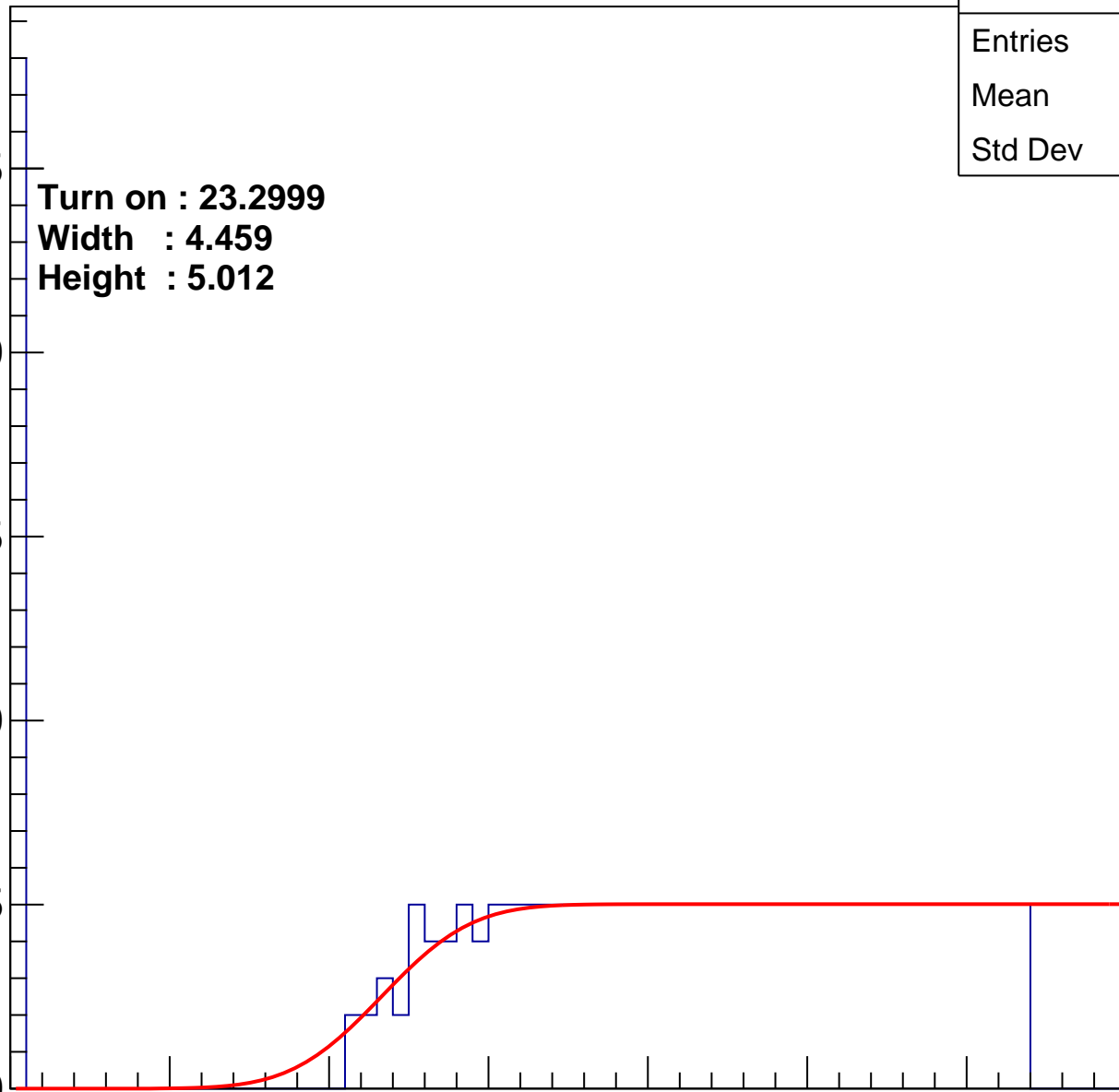
40

50

60

70

ampl



# B1L103S, U14-ch107

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	221
Mean	38.52
Std Dev	18.08

**Turn on : 25.8430**

**Width : 3.618**

**Height : 5.040**

Entry

25

20

15

10

5

0

0

10

20

30

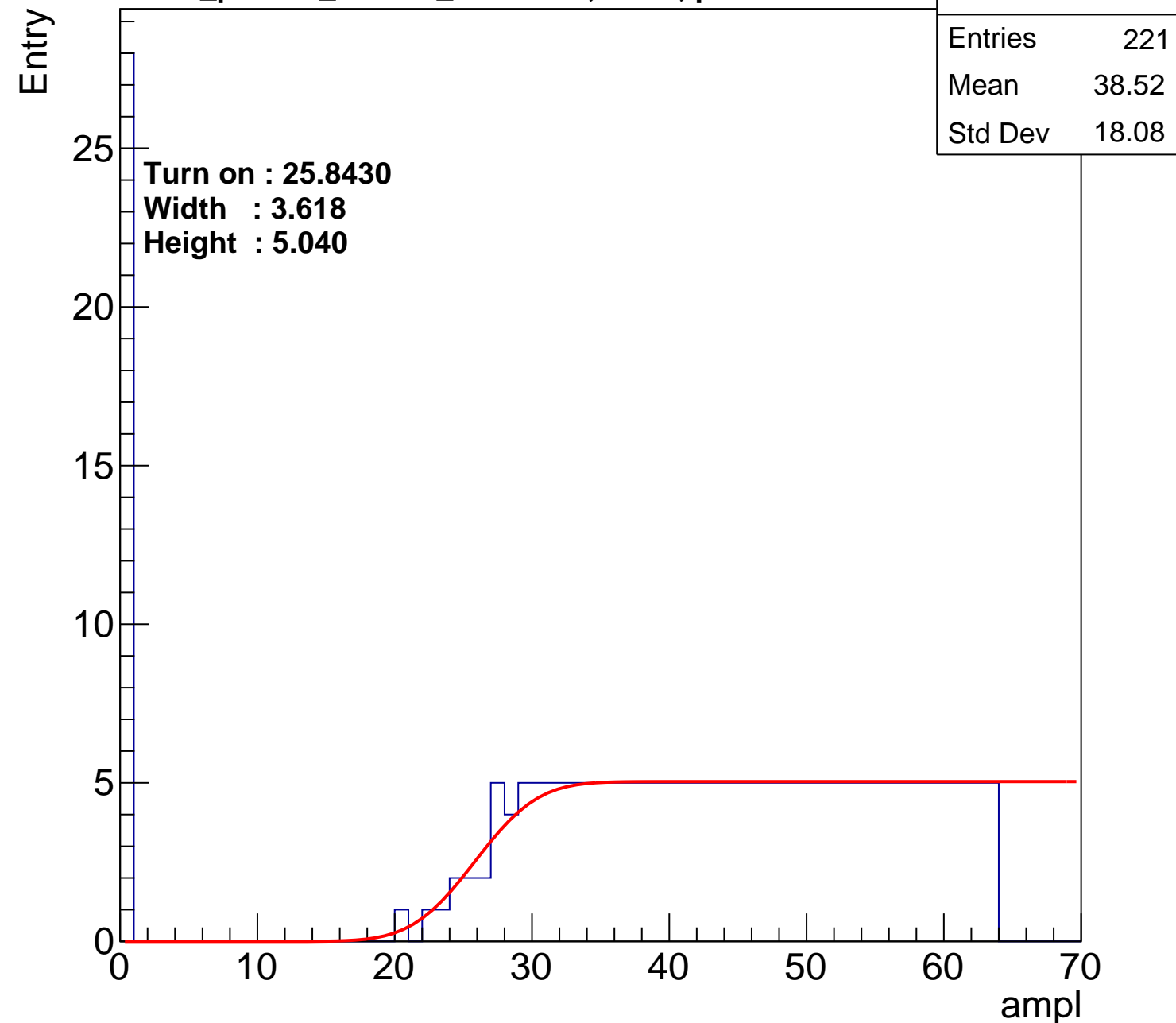
40

50

60

70

ampl



# B1L103S, U14-ch108

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	230
Mean	38.14
Std Dev	17.65

**Turn on : 22.8541**

**Width : 2.078**

**Height : 4.943**

Entry

25

20

15

10

5

0

0

10

20

30

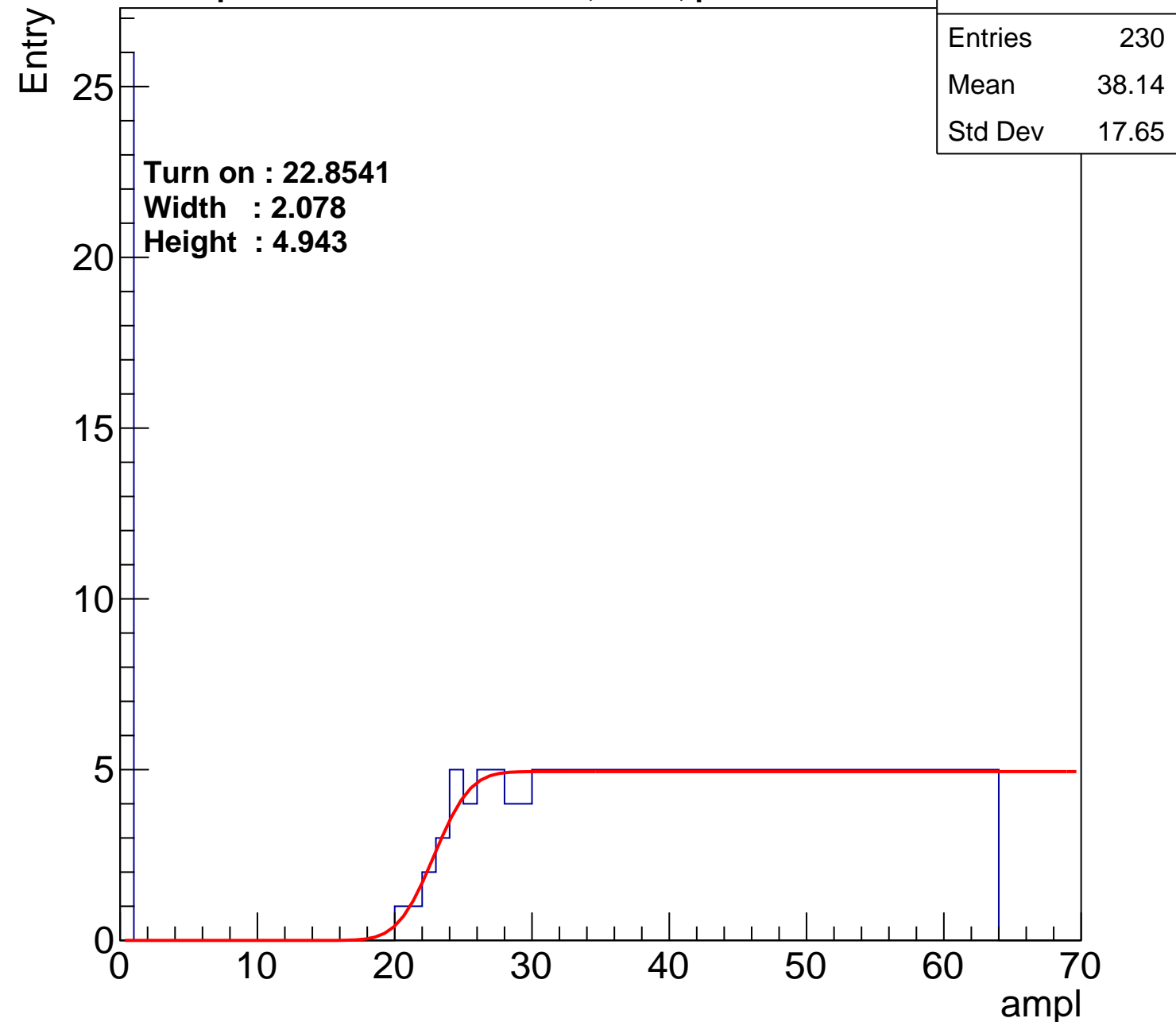
40

50

60

70

ampl



# B1L103S, U14-ch109

calib\_packv5\_041523\_1651.root, FC#0, port C2

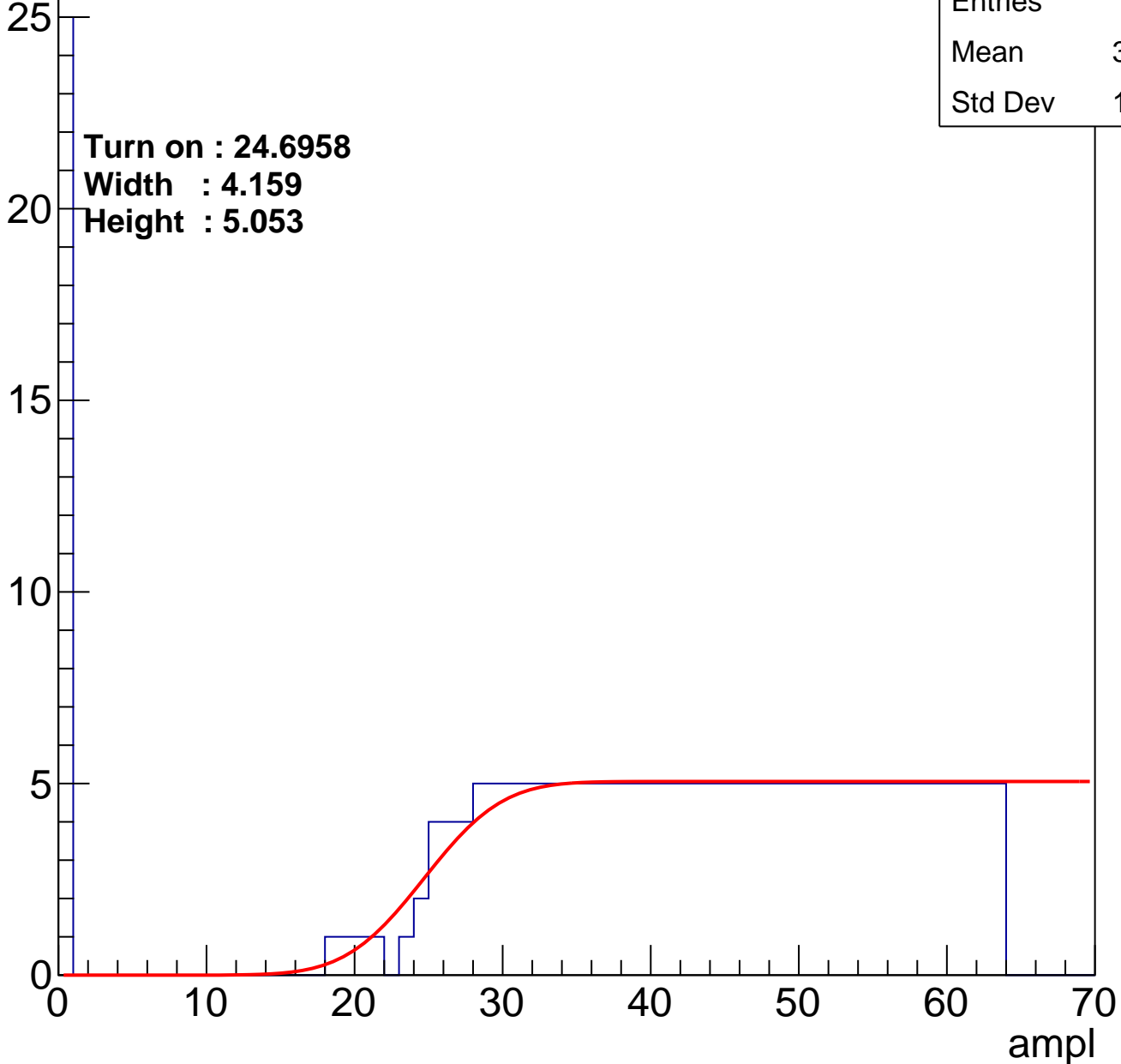
Entries	224
Mean	38.62
Std Dev	17.59

**Turn on : 24.6958**

**Width : 4.159**

**Height : 5.053**

Entry



# B1L103S, U14-ch110

calib\_packv5\_041523\_1651.root, FC#0, port C2

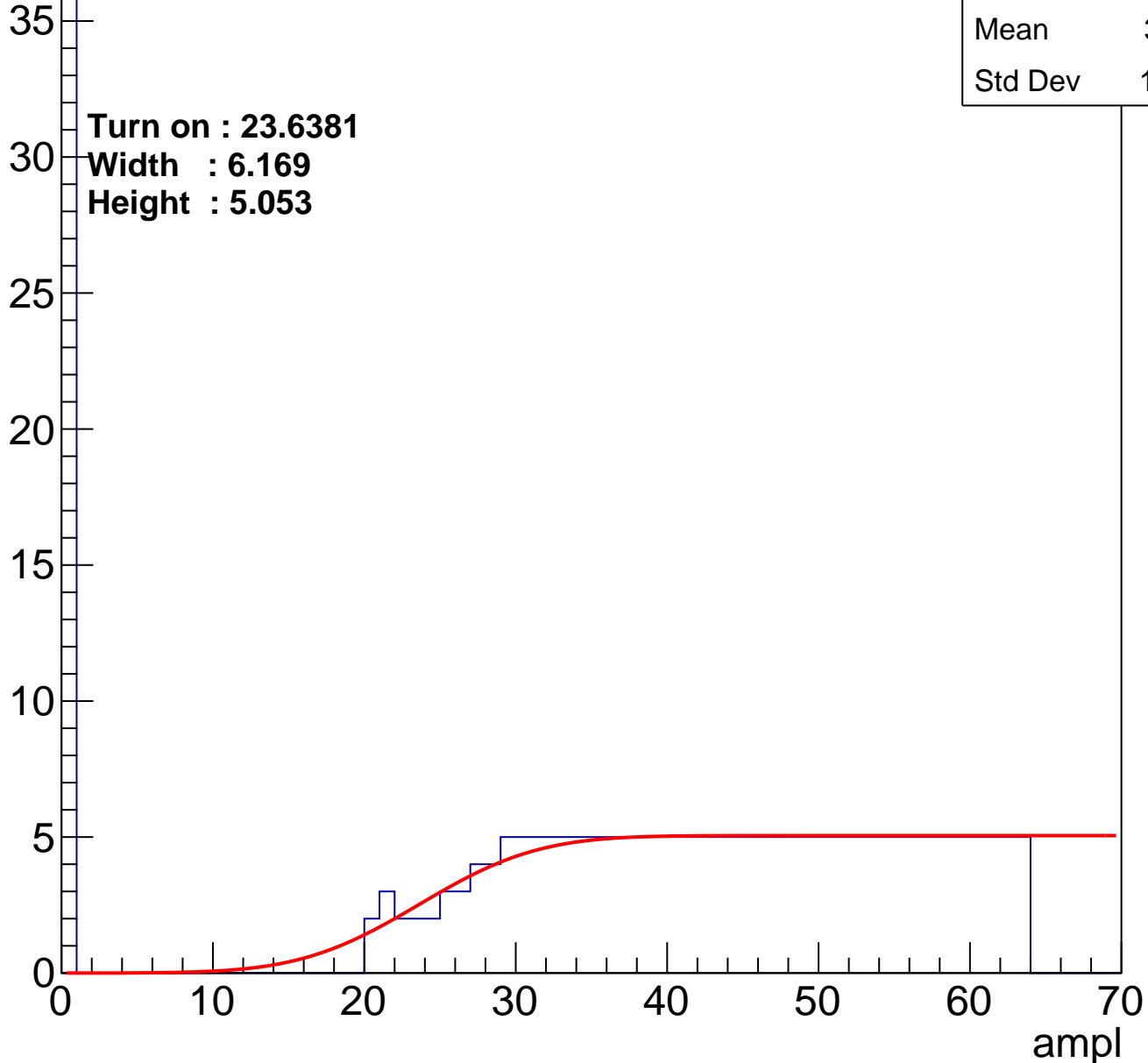
Entries	236
Mean	36.71
Std Dev	19.02

**Turn on : 23.6381**

**Width : 6.169**

**Height : 5.053**

Entry





# B1L103S, U14-ch111

calib\_packv5\_041523\_1651.root, FC#0, port C2

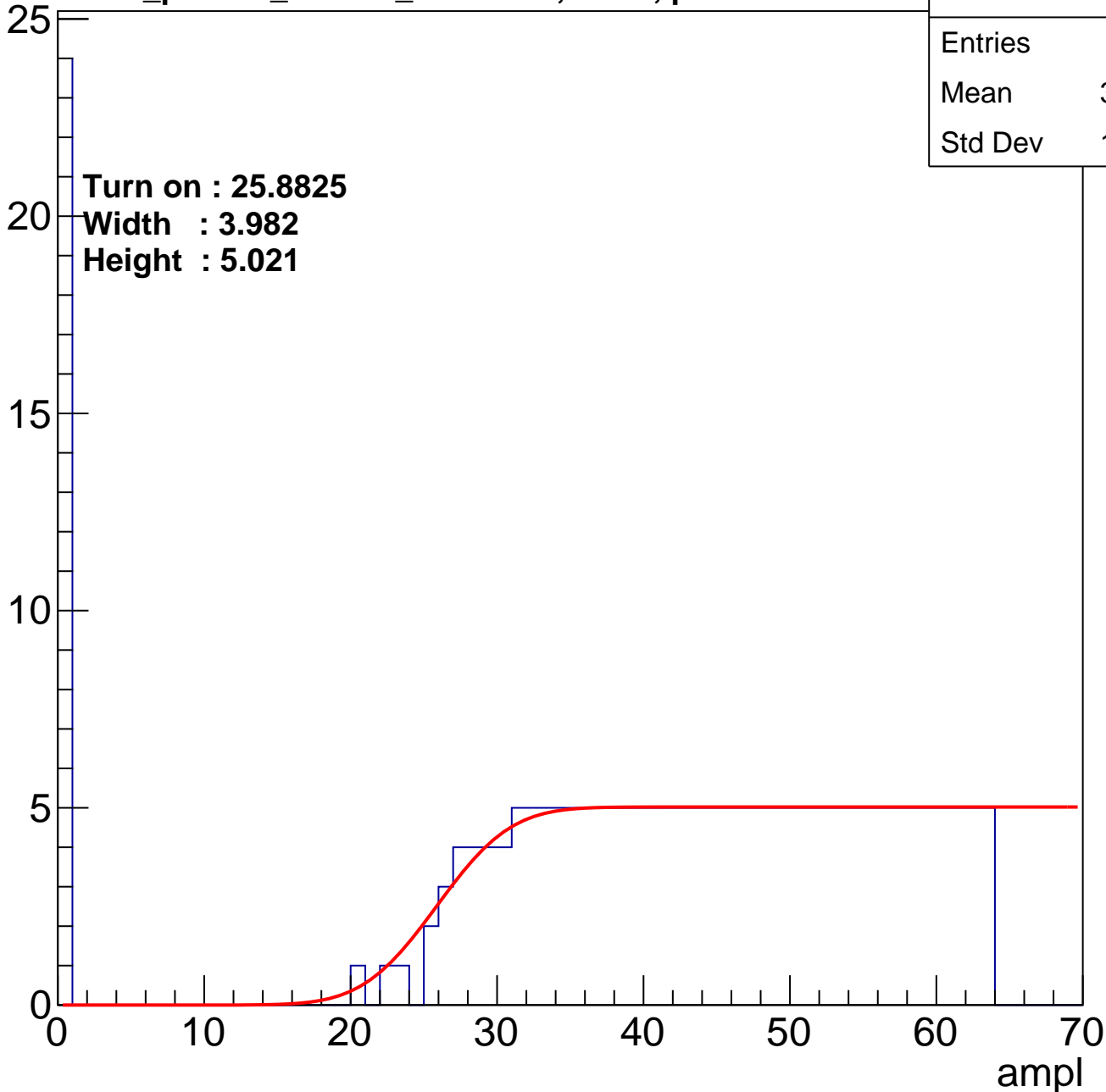
Entries	213
Mean	39.46
Std Dev	17.55

Turn on : 25.8825

Width : 3.982

Height : 5.021

Entry



# B1L103S, U14-ch112

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	227
Mean	38.37
Std Dev	17.89

**Turn on : 24.7522**

**Width : 4.135**

**Height : 5.060**

Entry

25

20

15

10

5

0

0

10

20

30

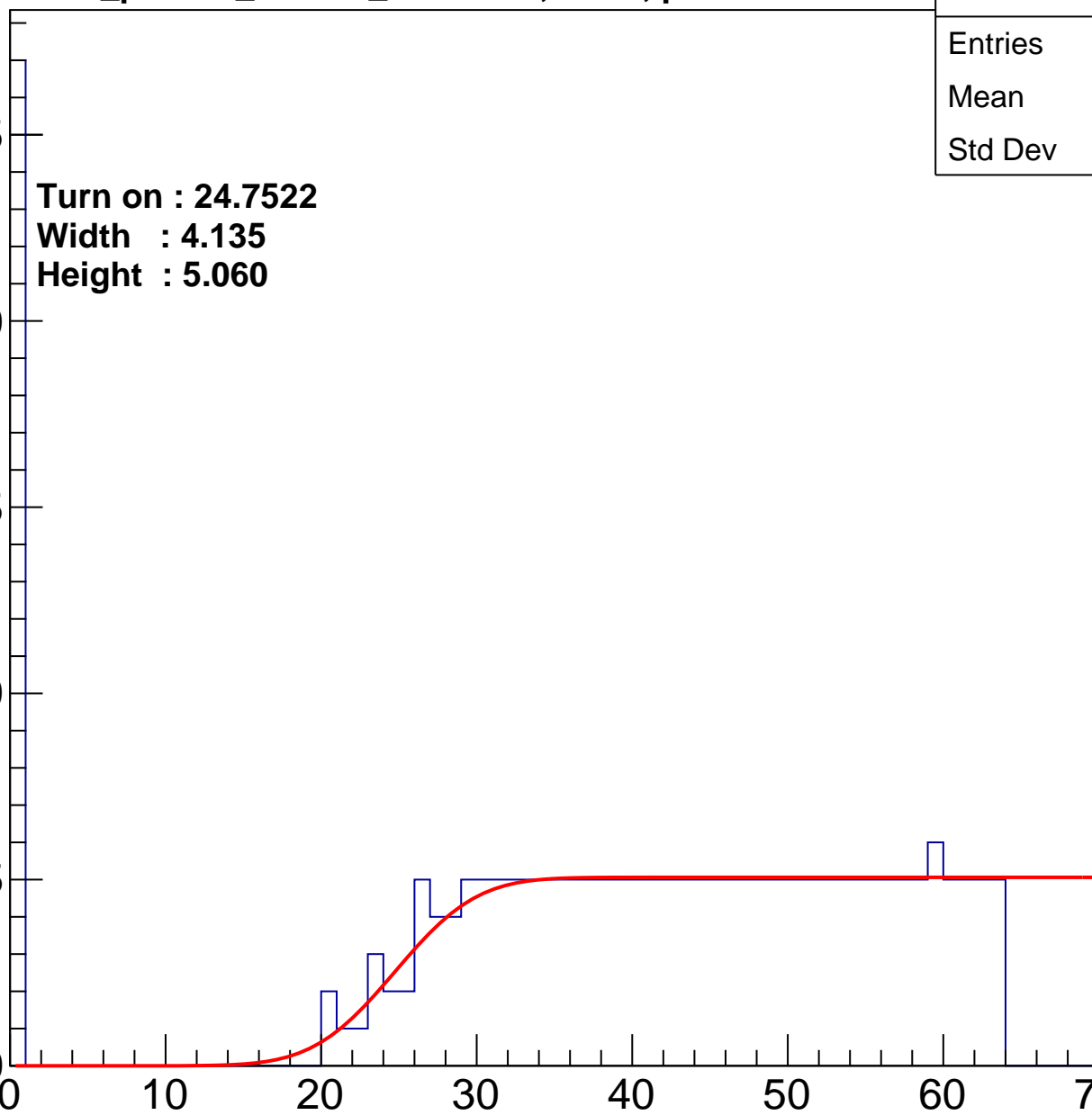
40

50

60

70

ampl



# B1L103S, U14-ch113

calib\_packv5\_041523\_1651.root, FC#0, port C2

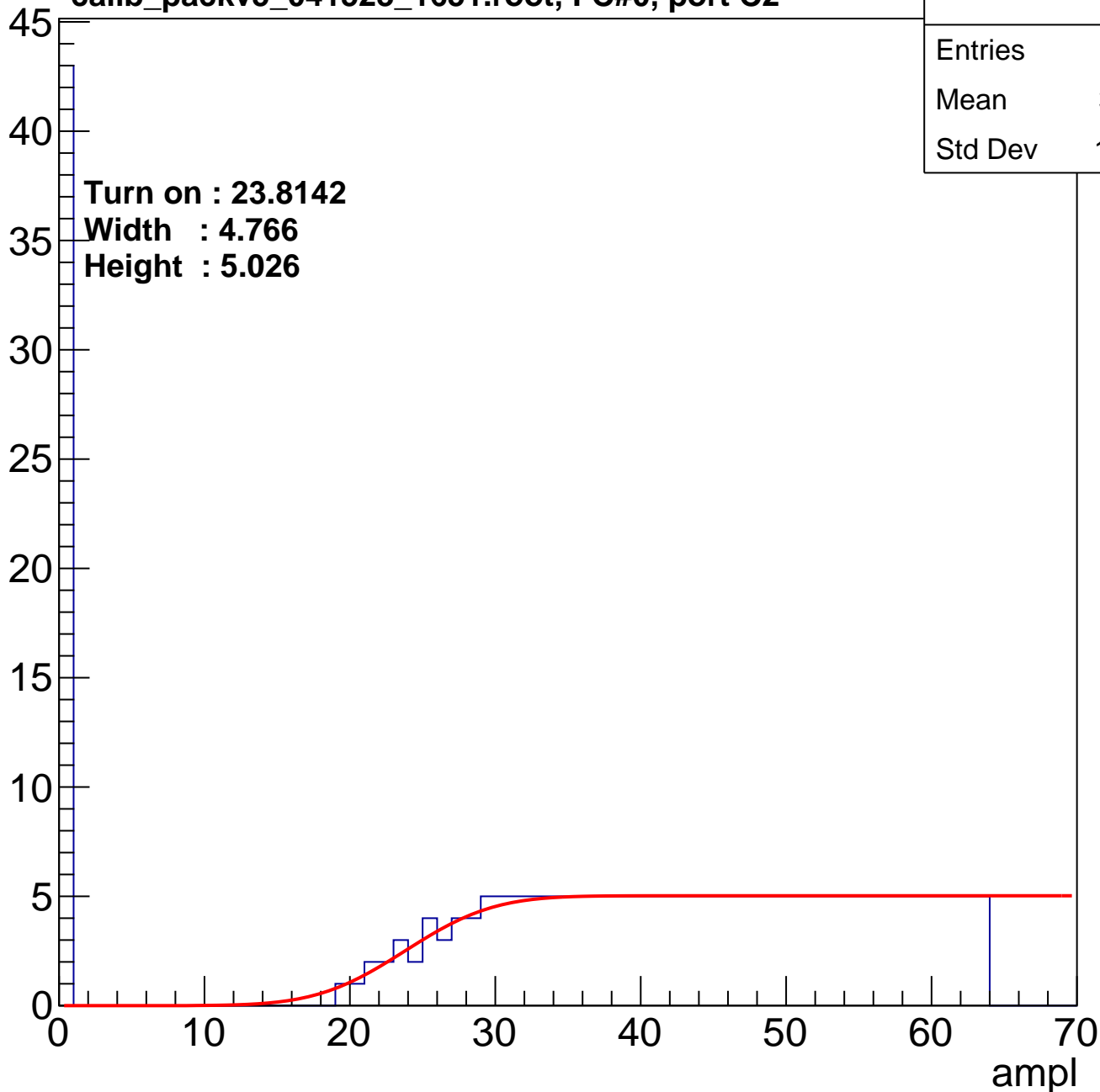
Entries	244
Mean	35.61
Std Dev	19.69

**Turn on : 23.8142**

**Width : 4.766**

**Height : 5.026**

Entry



# B1L103S, U14-ch114

calib\_packv5\_041523\_1651.root, FC#0, port C2

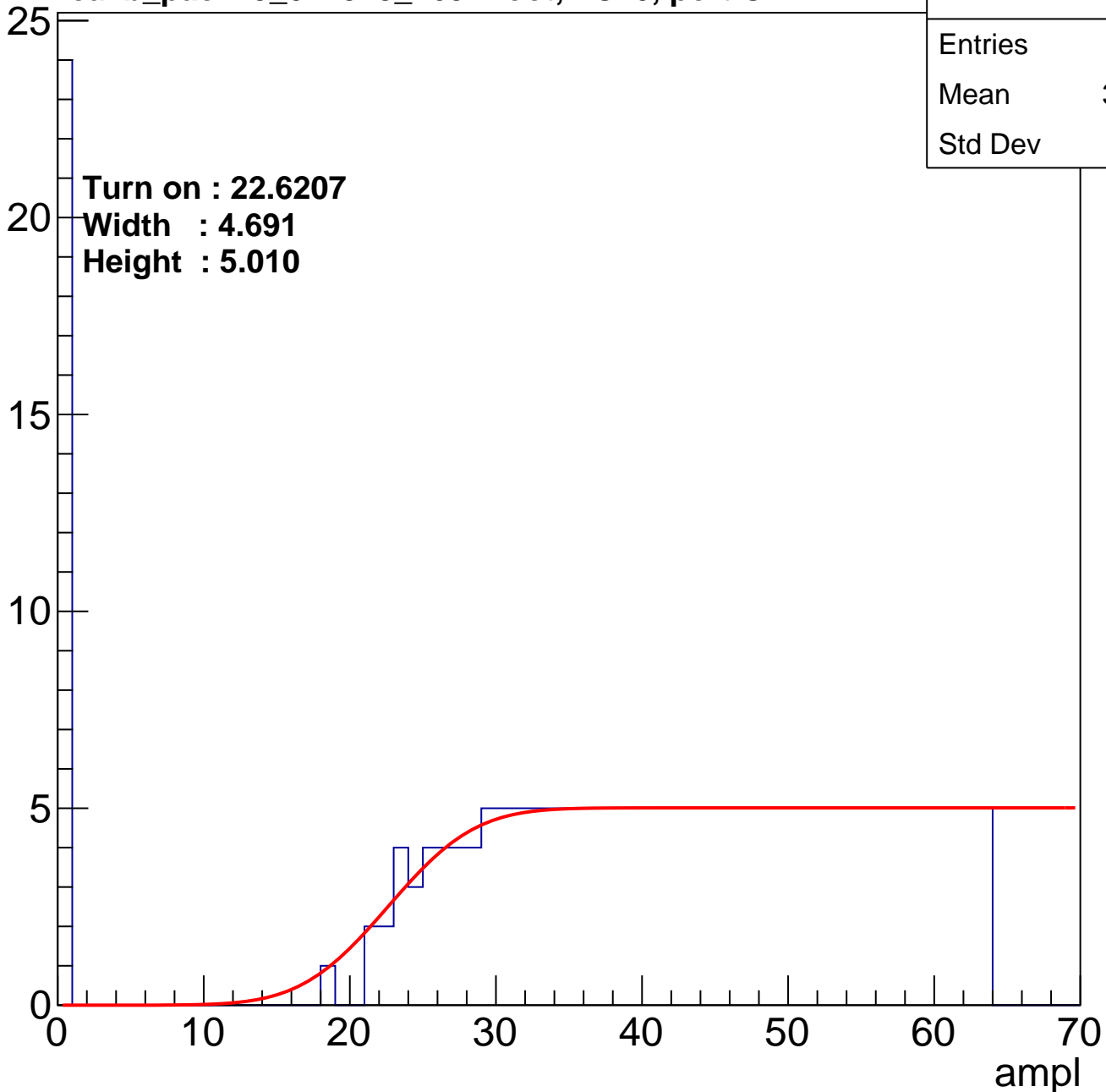
Entries	227
Mean	38.51
Std Dev	17.4

Turn on : 22.6207

Width : 4.691

Height : 5.010

Entry



# B1L103S, U14-ch115

calib\_packv5\_041523\_1651.root, FC#0, port C2

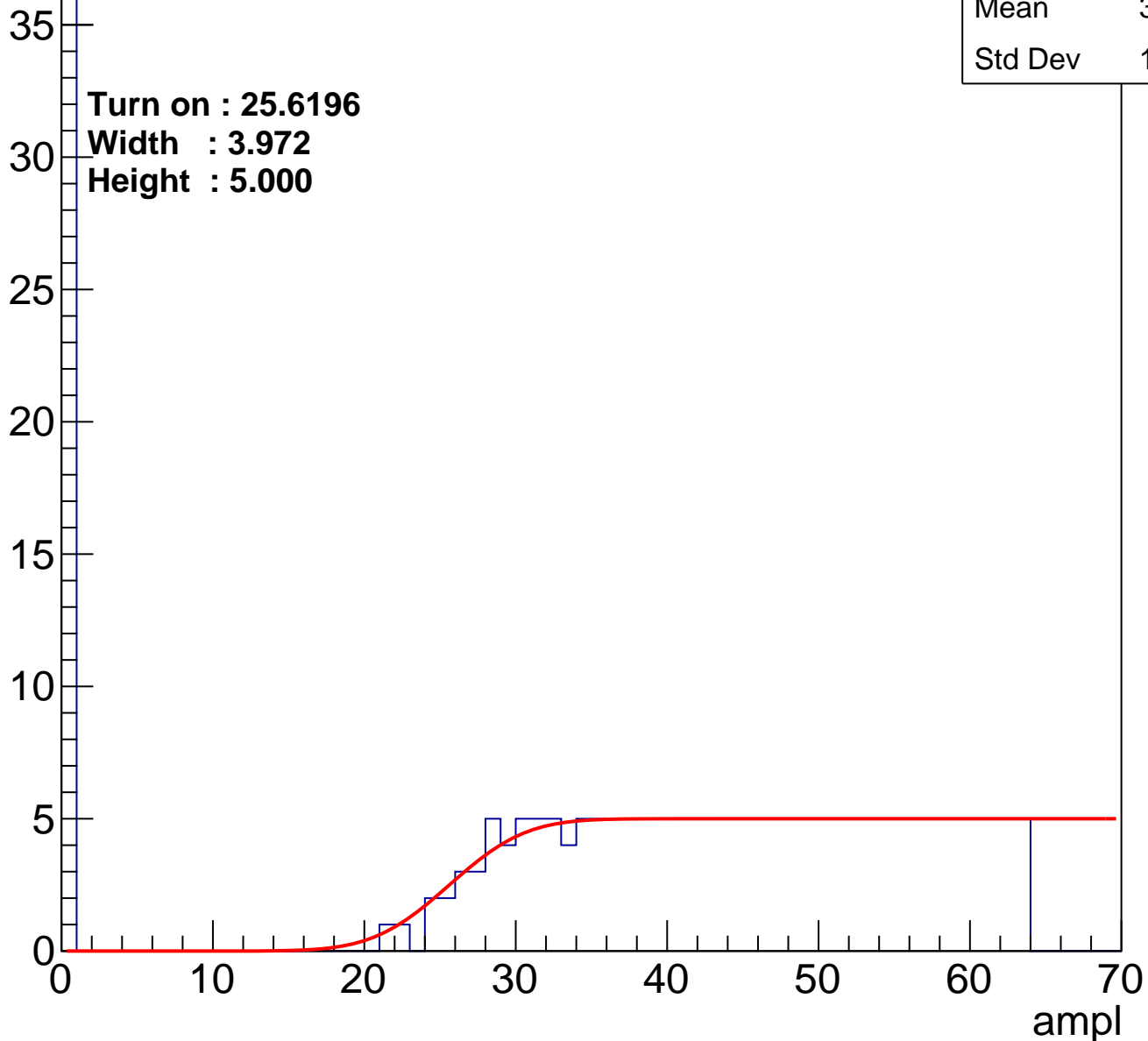
Entries	227
Mean	37.13
Std Dev	19.32

**Turn on : 25.6196**

**Width : 3.972**

**Height : 5.000**

Entry



# B1L103S, U14-ch116

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	228
Mean	37.78
Std Dev	18.41

**Turn on : 24.8199**

**Width : 2.787**

**Height : 5.021**

Entry

30

25

20

15

10

5

0

0

10

20

30

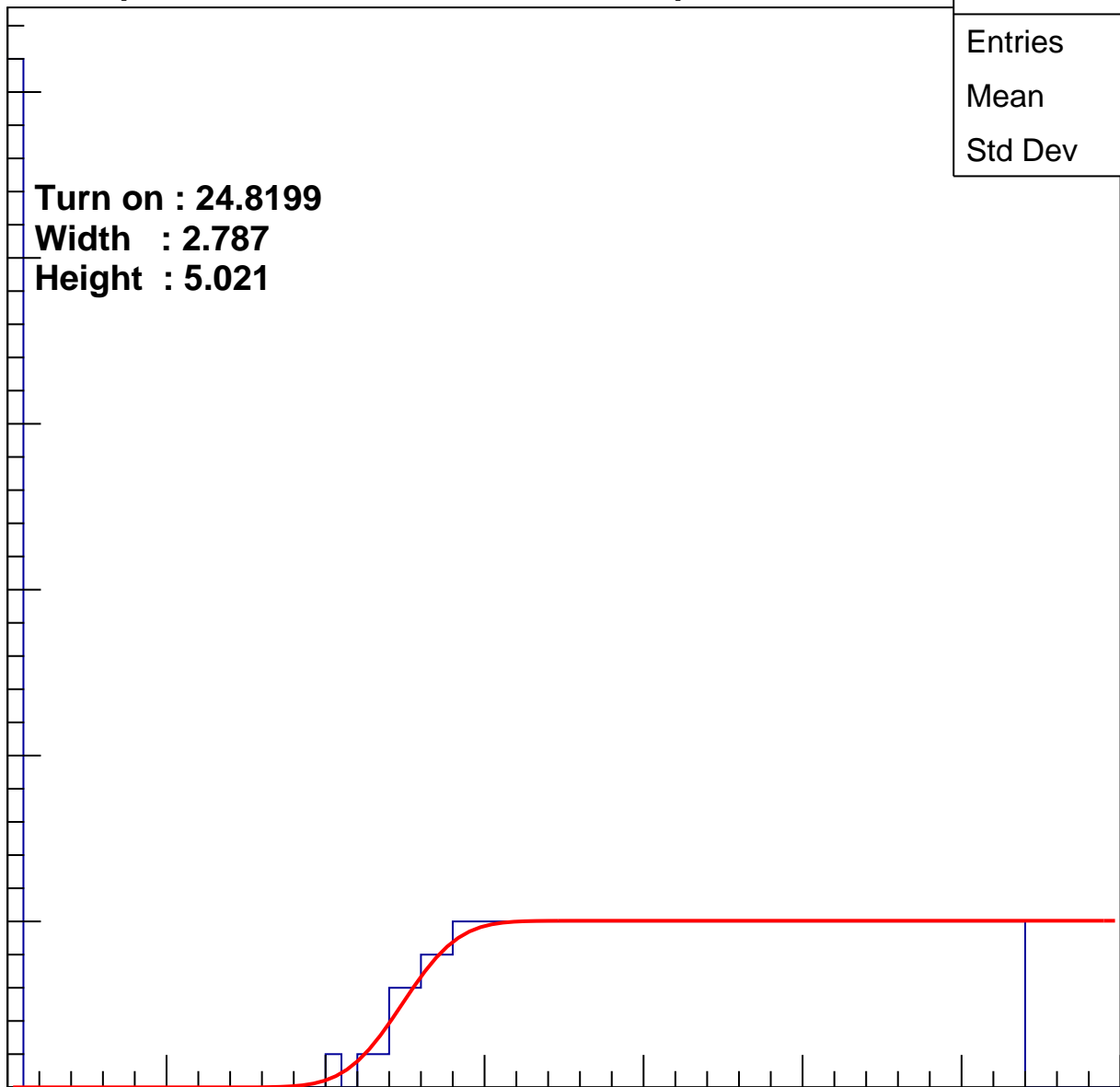
40

50

60

70

ampl



# B1L103S, U14-ch117

calib\_packv5\_041523\_1651.root, FC#0, port C2

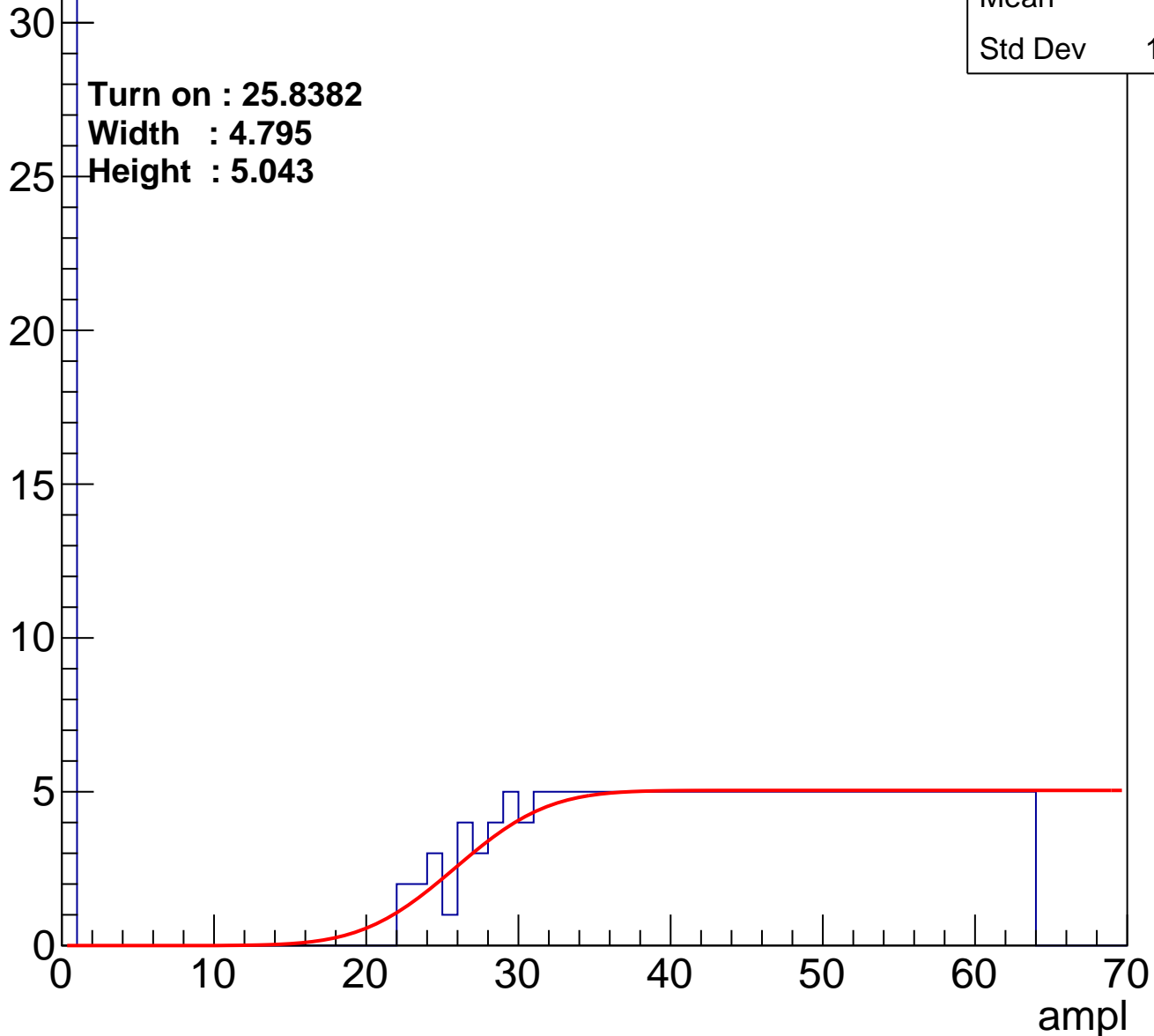
Entries	225
Mean	37.8
Std Dev	18.65

**Turn on : 25.8382**

**Width : 4.795**

**Height : 5.043**

Entry



# B1L103S, U14-ch118

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	240
Mean	36.89
Std Dev	18.41

**Turn on : 22.9163**

**Width : 3.763**

**Height : 5.023**

Entry

30

25

20

15

10

5

0

0

10

20

30

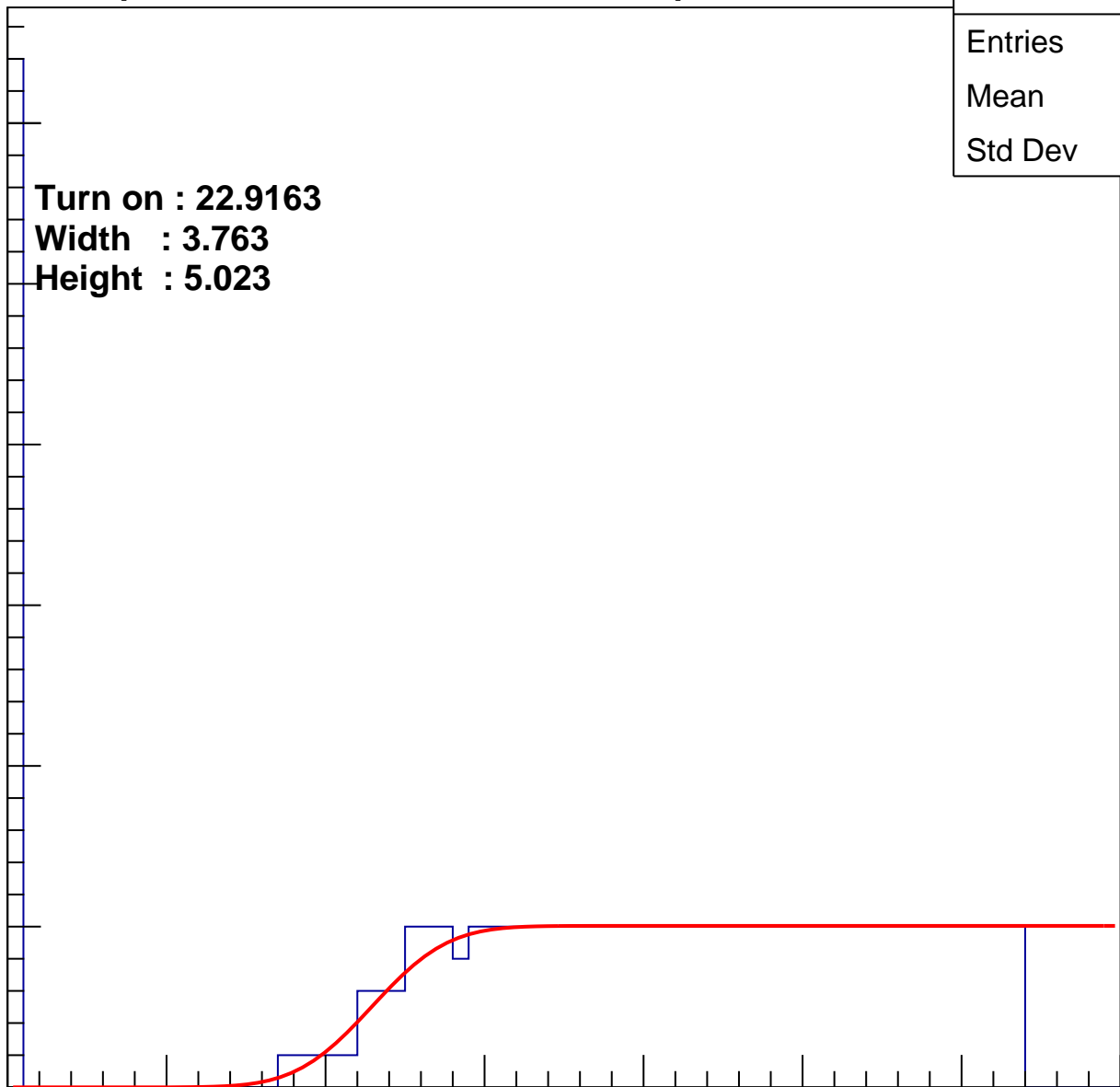
40

50

60

70

ampl





# B1L103S, U14-ch119

calib\_packv5\_041523\_1651.root, FC#0, port C2

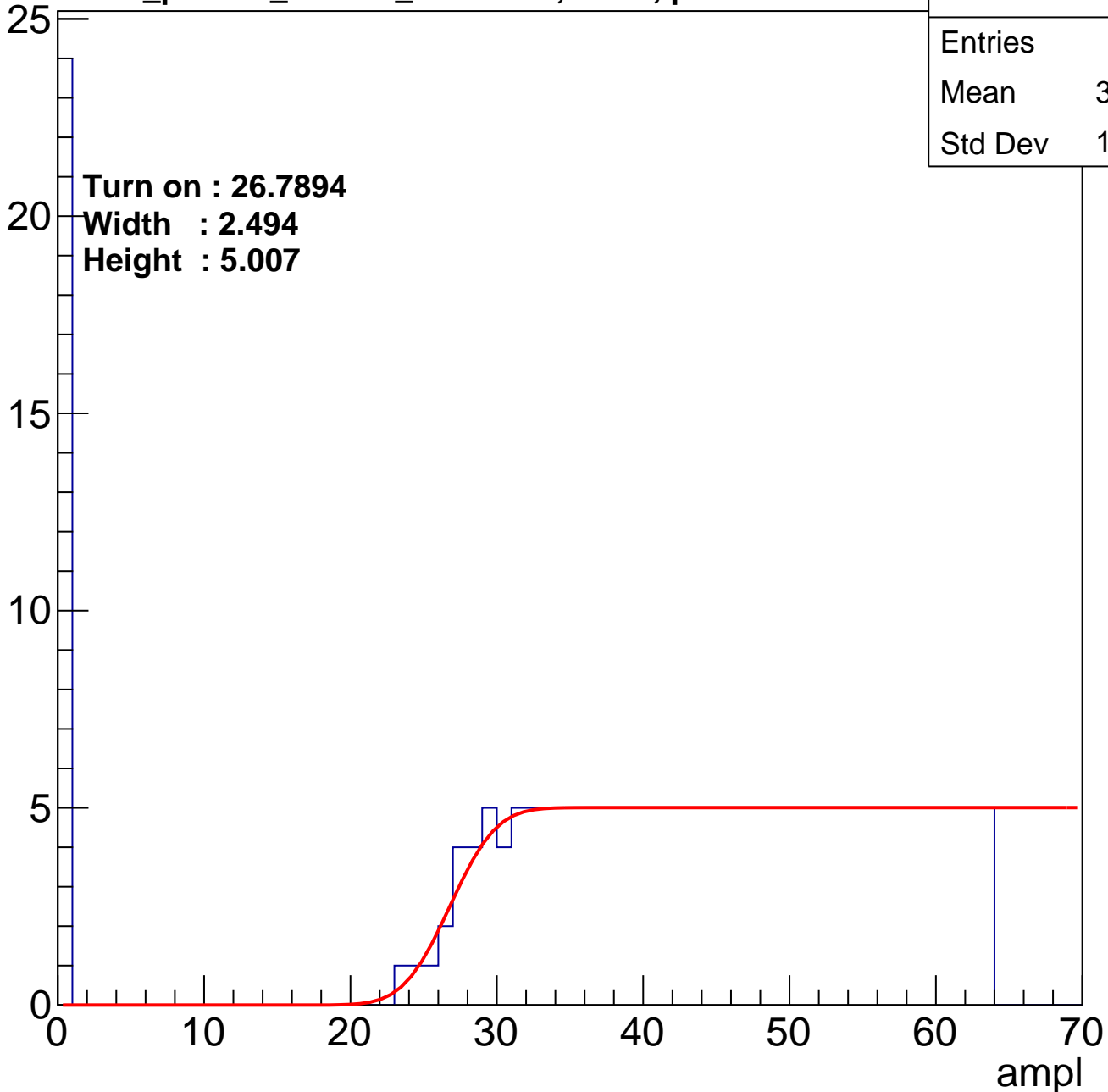
Entries	211
Mean	39.64
Std Dev	17.53

Turn on : 26.7894

Width : 2.494

Height : 5.007

Entry



# B1L103S, U14-ch120

calib\_packv5\_041523\_1651.root, FC#0, port C2

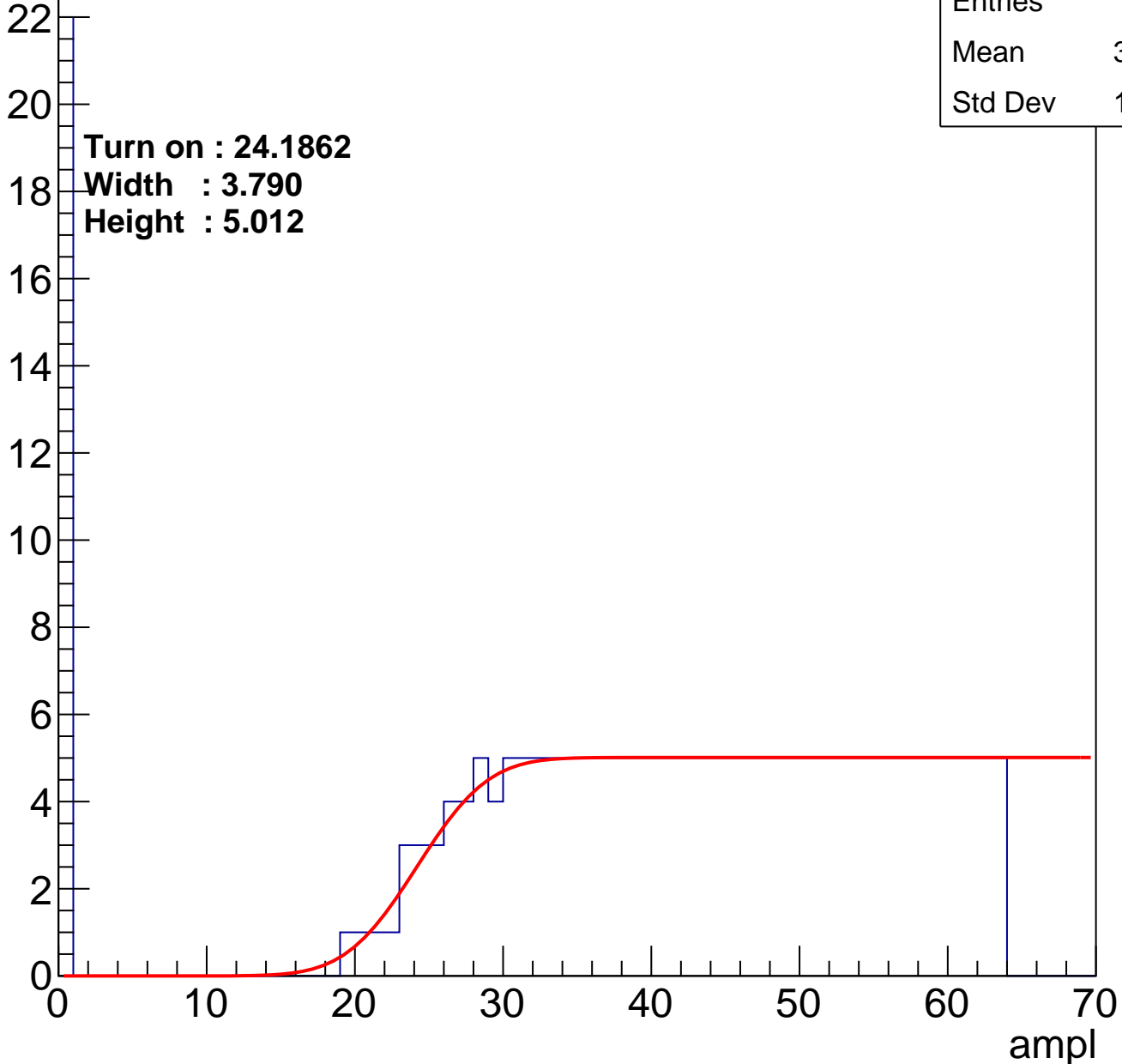
Entries	222
Mean	39.06
Std Dev	17.12

**Turn on : 24.1862**

**Width : 3.790**

**Height : 5.012**

Entry



# B1L103S, U14-ch121

calib\_packv5\_041523\_1651.root, FC#0, port C2

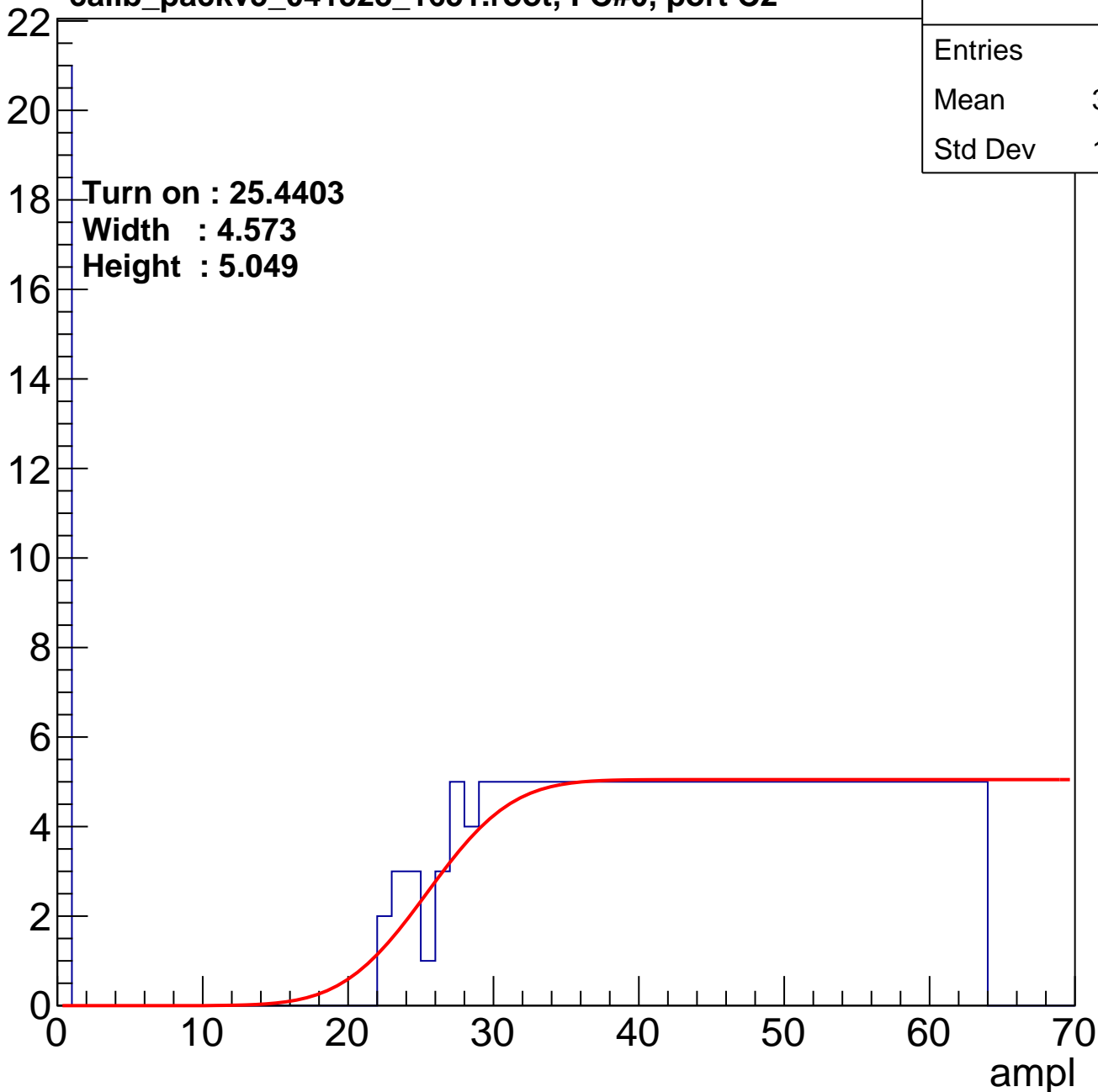
Entries	217
Mean	39.56
Std Dev	16.93

**Turn on : 25.4403**

**Width : 4.573**

**Height : 5.049**

Entry



# B1L103S, U14-ch122

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	215
Mean	38.45
Std Dev	18.87

**Turn on : 28.3242**

**Width : 4.579**

**Height : 5.093**

Entry

30

25

20

15

10

5

0

0

10

20

30

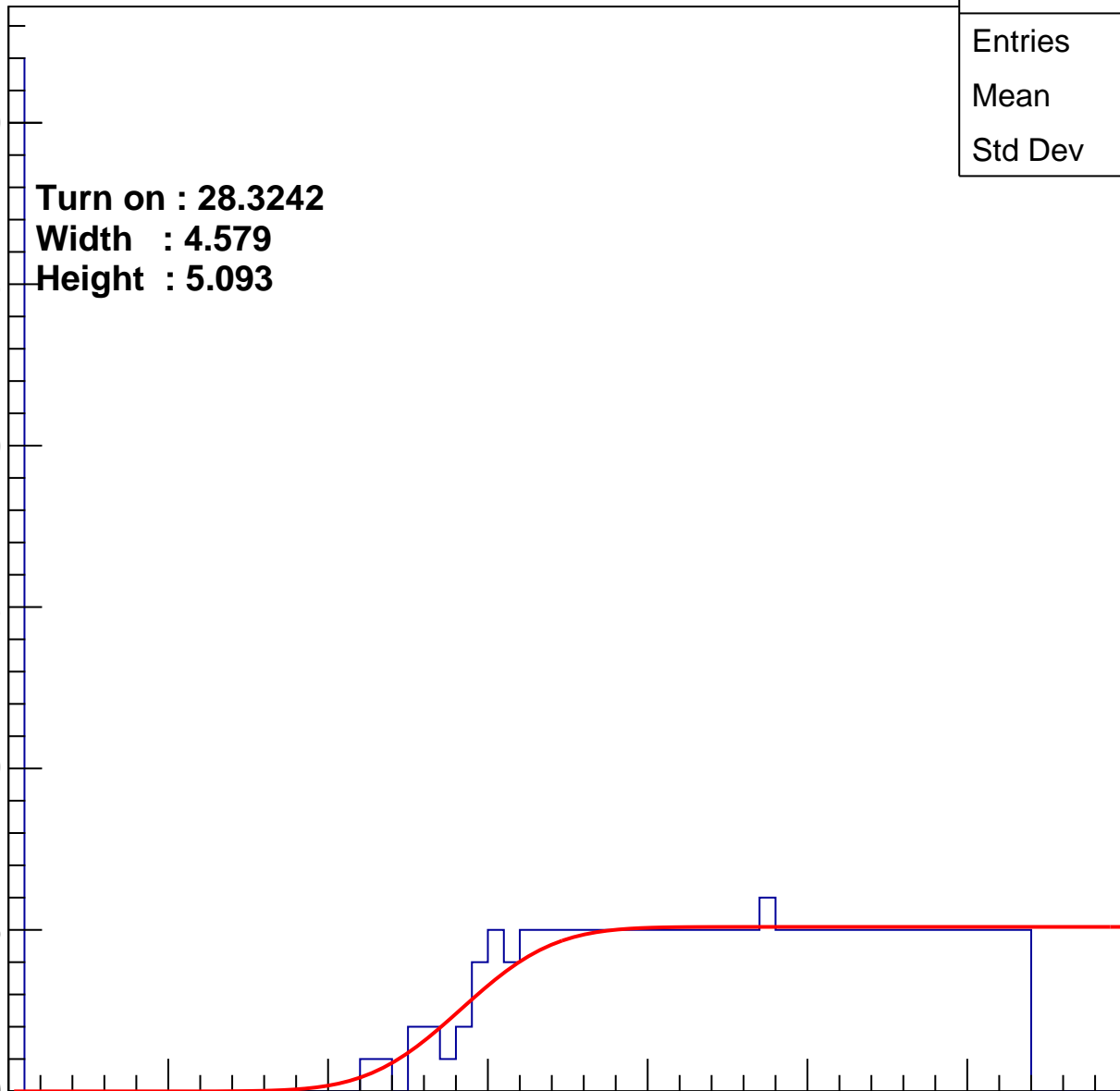
40

50

60

70

ampl



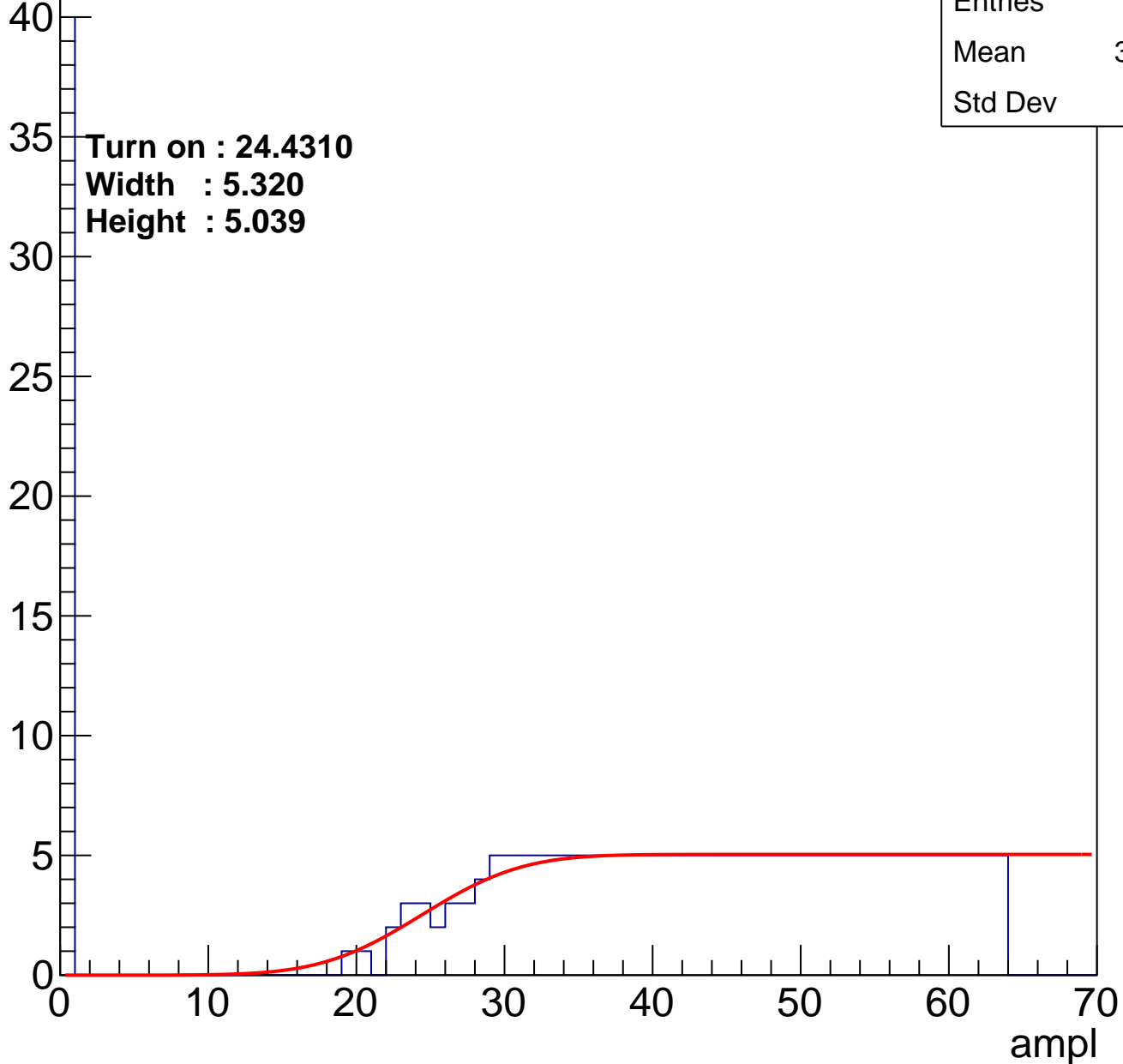
# B1L103S, U14-ch123

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	237
Mean	36.27
Std Dev	19.5

Turn on : 24.4310  
Width : 5.320  
Height : 5.039

Entry



# B1L103S, U14-ch124

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	239
Mean	36.39
Std Dev	19.18

**Turn on : 23.5743**

**Width : 4.756**

**Height : 5.032**

Entry

35

30

25

20

15

10

5

0

0

10

20

30

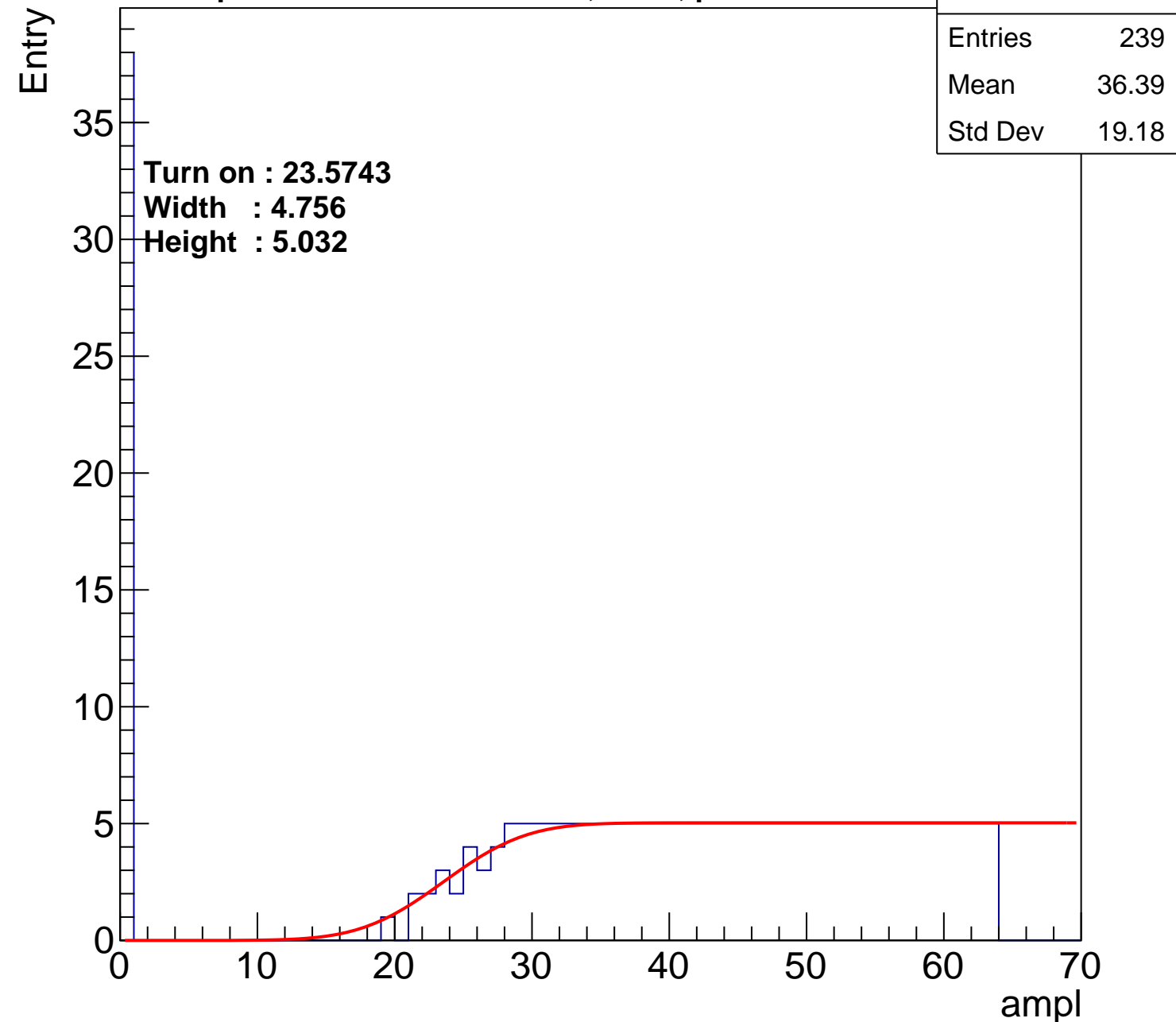
40

50

60

70

ampl



# B1L103S, U14-ch125

calib\_packv5\_041523\_1651.root, FC#0, port C2

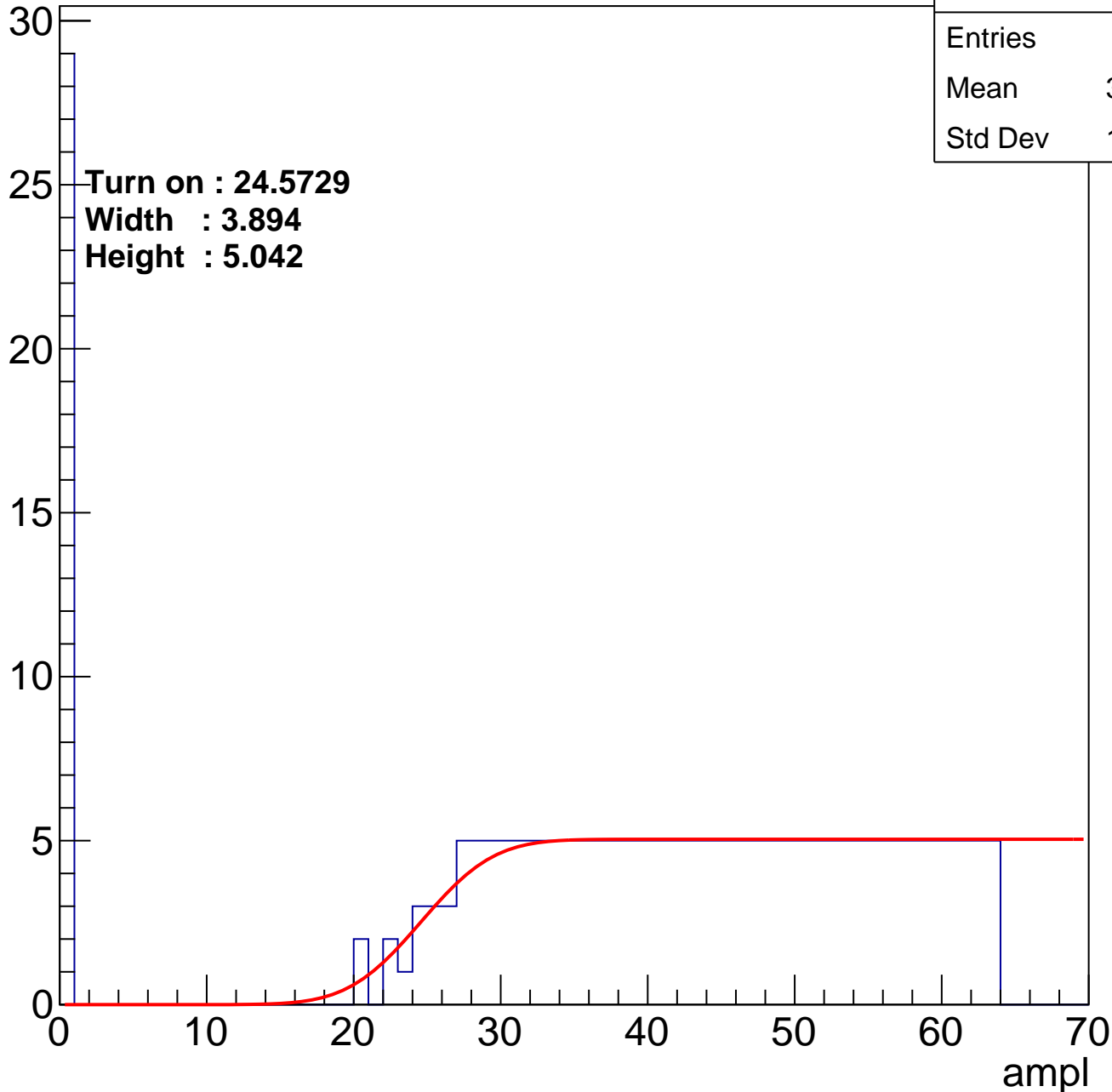
Entries	228
Mean	37.97
Std Dev	18.13

Turn on : 24.5729

Width : 3.894

Height : 5.042

Entry



# B1L103S, U14-ch126

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	237
Mean	36.76
Std Dev	18.86

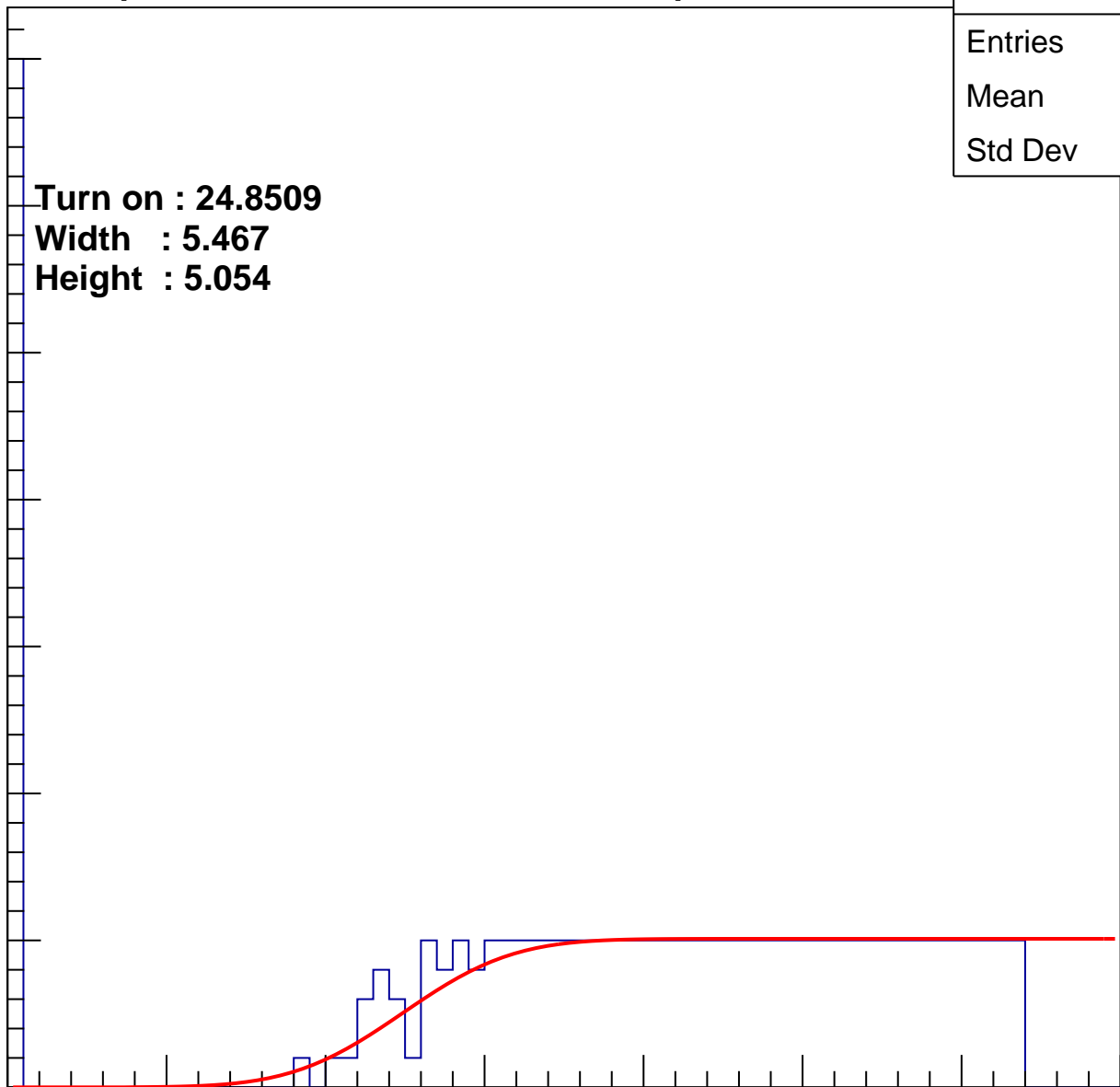
Entry

35  
30  
25  
20  
15  
10  
5  
0

Turn on : 24.8509  
Width : 5.467  
Height : 5.054

0 10 20 30 40 50 60 70

ampl



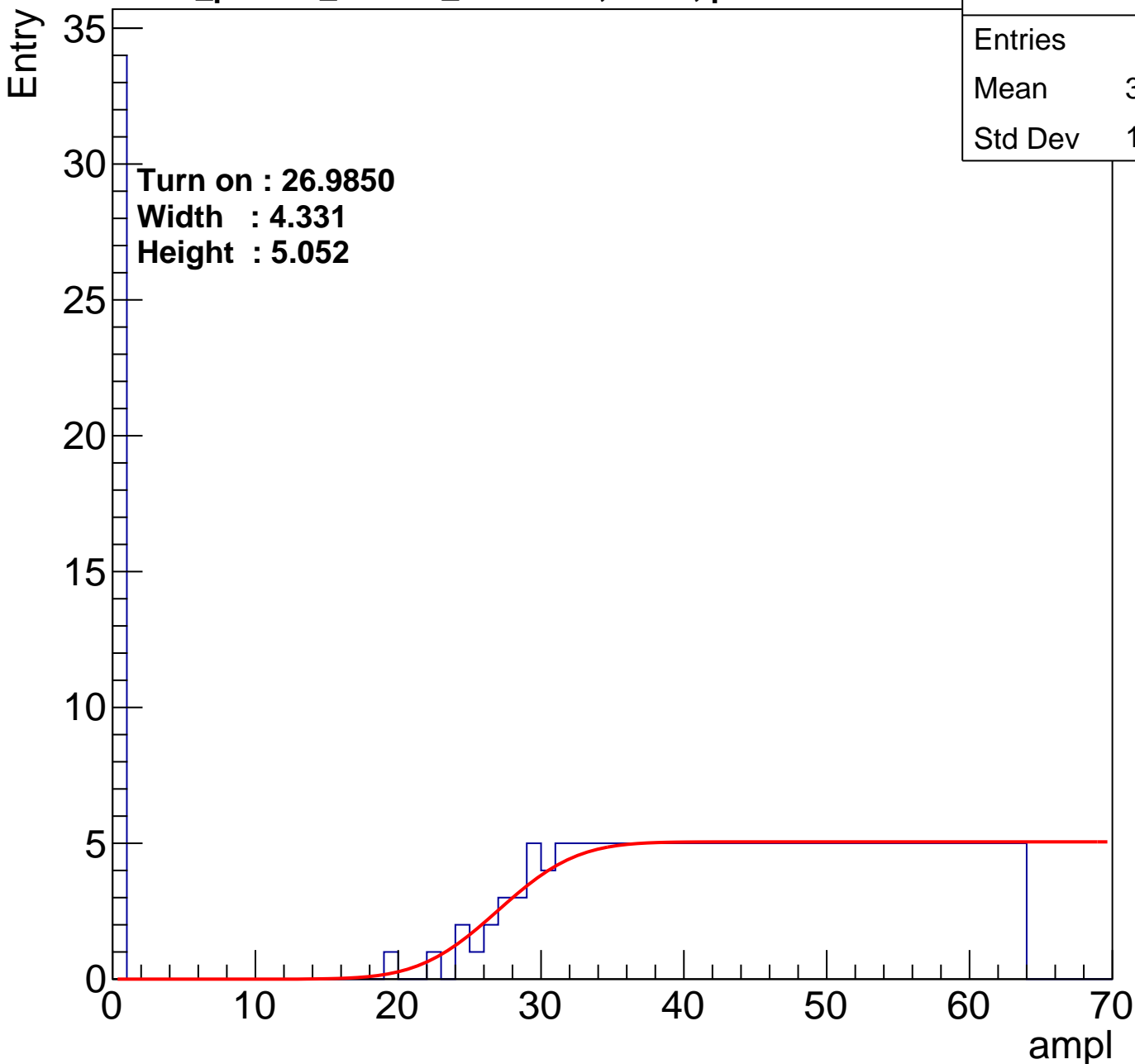


# B1L103S, U14-ch127

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	221
Mean	37.79
Std Dev	19.05

Turn on : 26.9850  
Width : 4.331  
Height : 5.052



# B1L103S, U14-ch127

calib\_packv5\_041523\_1651.root, FC#0, port C2

Entries	221
Mean	37.79
Std Dev	19.05

**Turn on : 26.9850**  
**Width : 4.331**  
**Height : 5.052**

