



# B0L000S, U1-ch0

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	363
Mean	45.18
Std Dev	10.87

Turn on : 28.0854

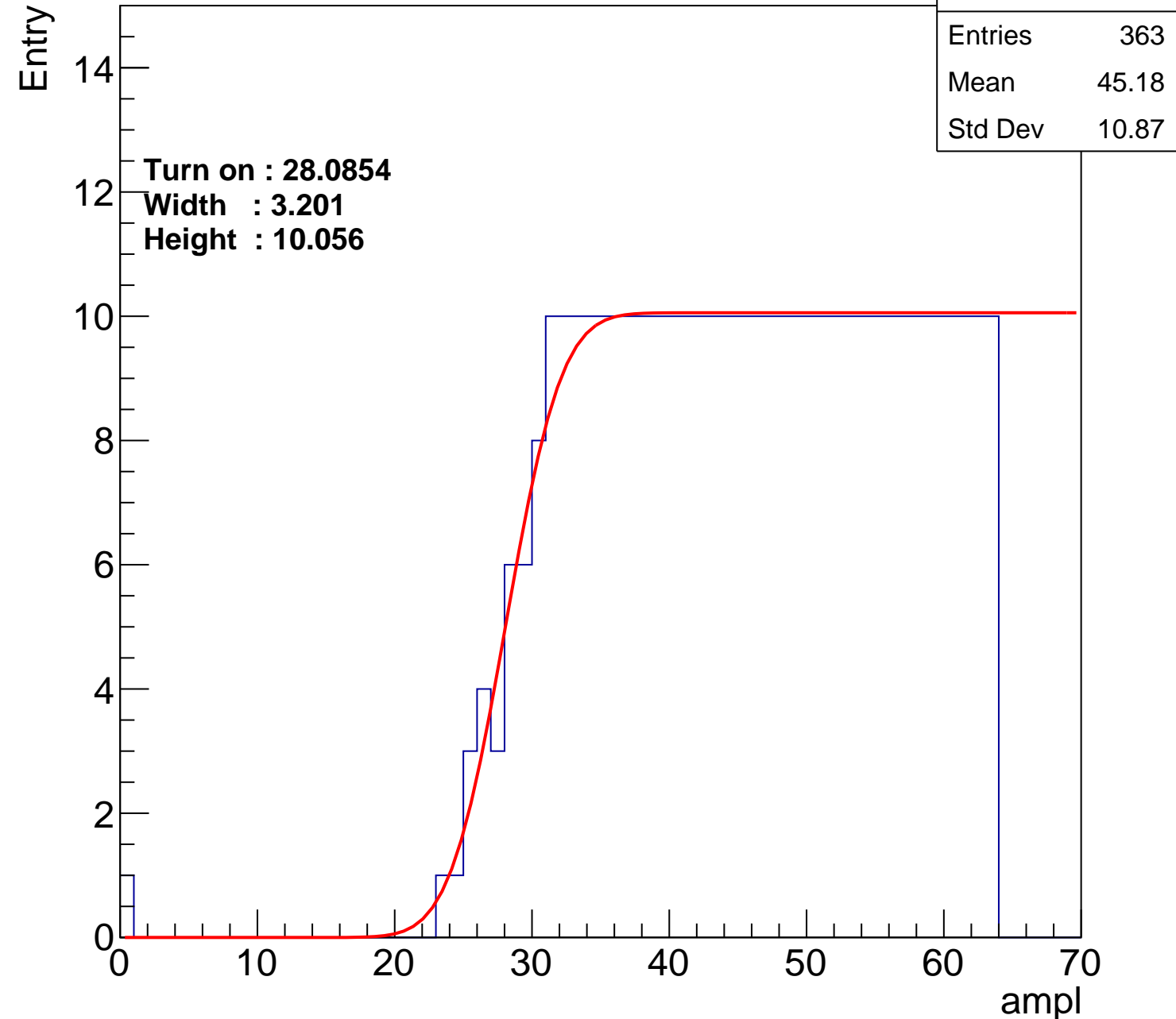
Width : 3.201

Height : 10.056

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch1

calib\_packv5\_042523\_0143.root, FC#5, port B1

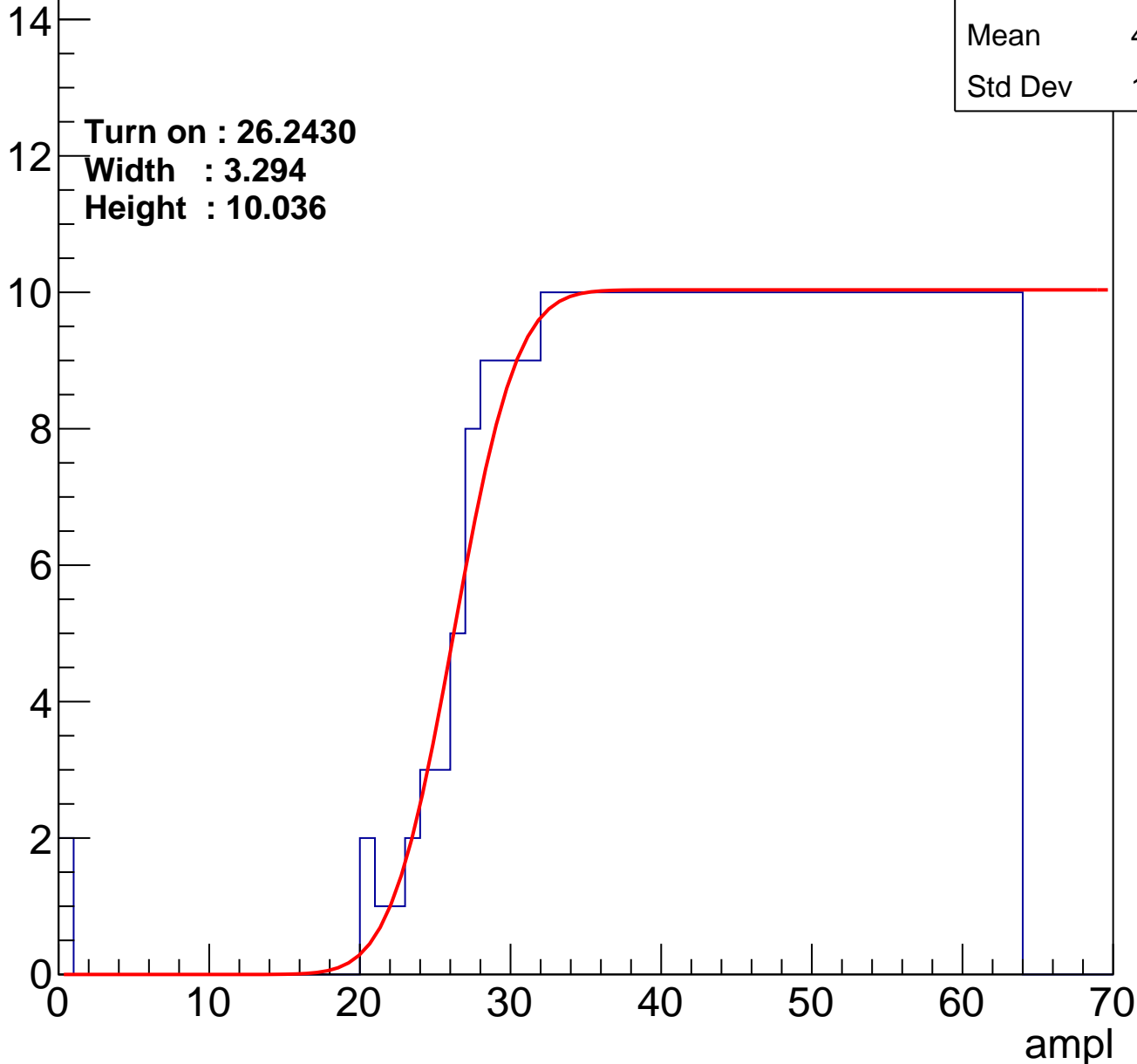
Entries	383
Mean	44.08
Std Dev	11.65

Turn on : 26.2430

Width : 3.294

Height : 10.036

Entry



# B0L000S, U1-ch2

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	382
Mean	44.19
Std Dev	11.52

Turn on : 26.1240

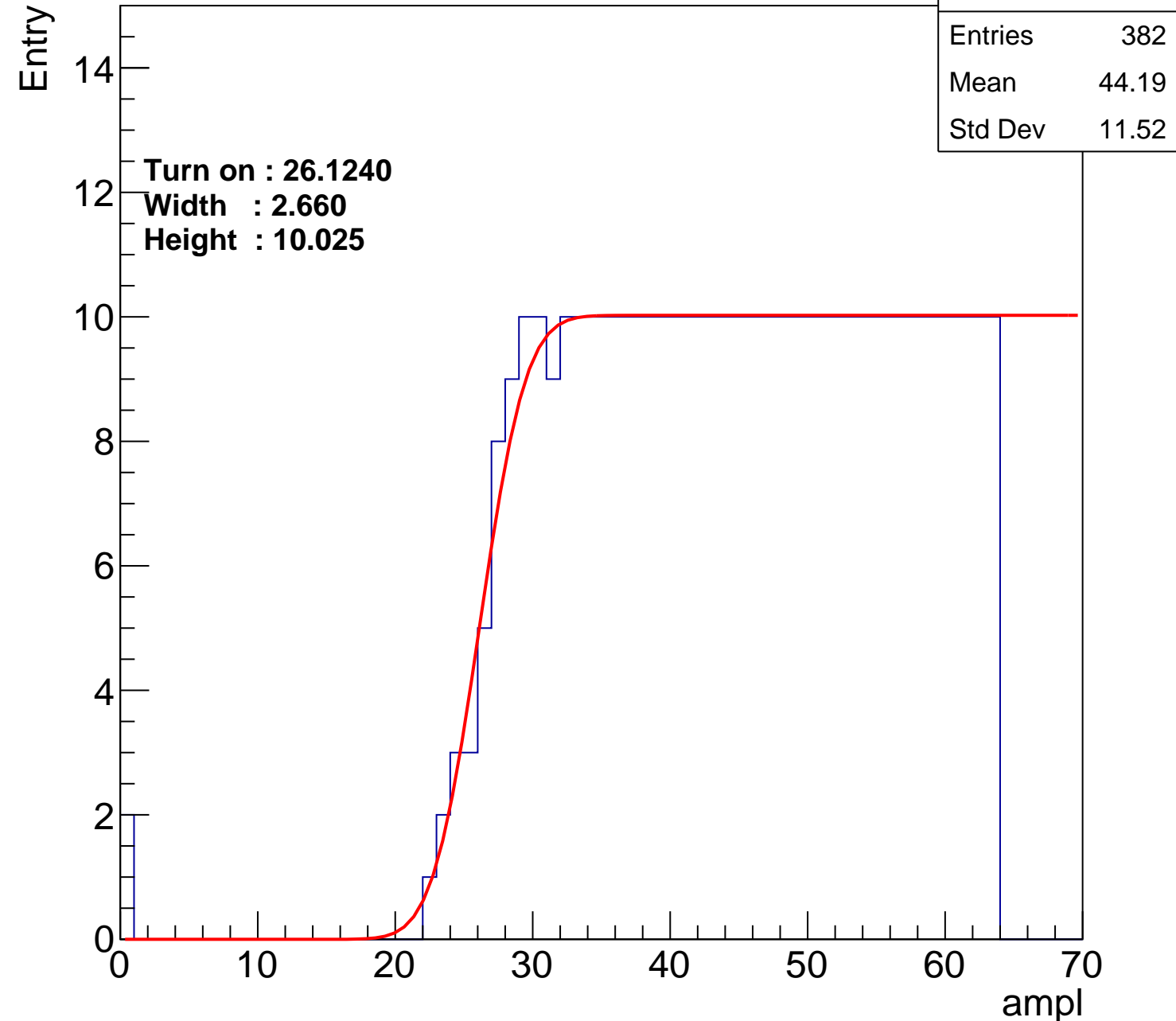
Width : 2.660

Height : 10.025

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch3

calib\_packv5\_042523\_0143.root, FC#5, port B1

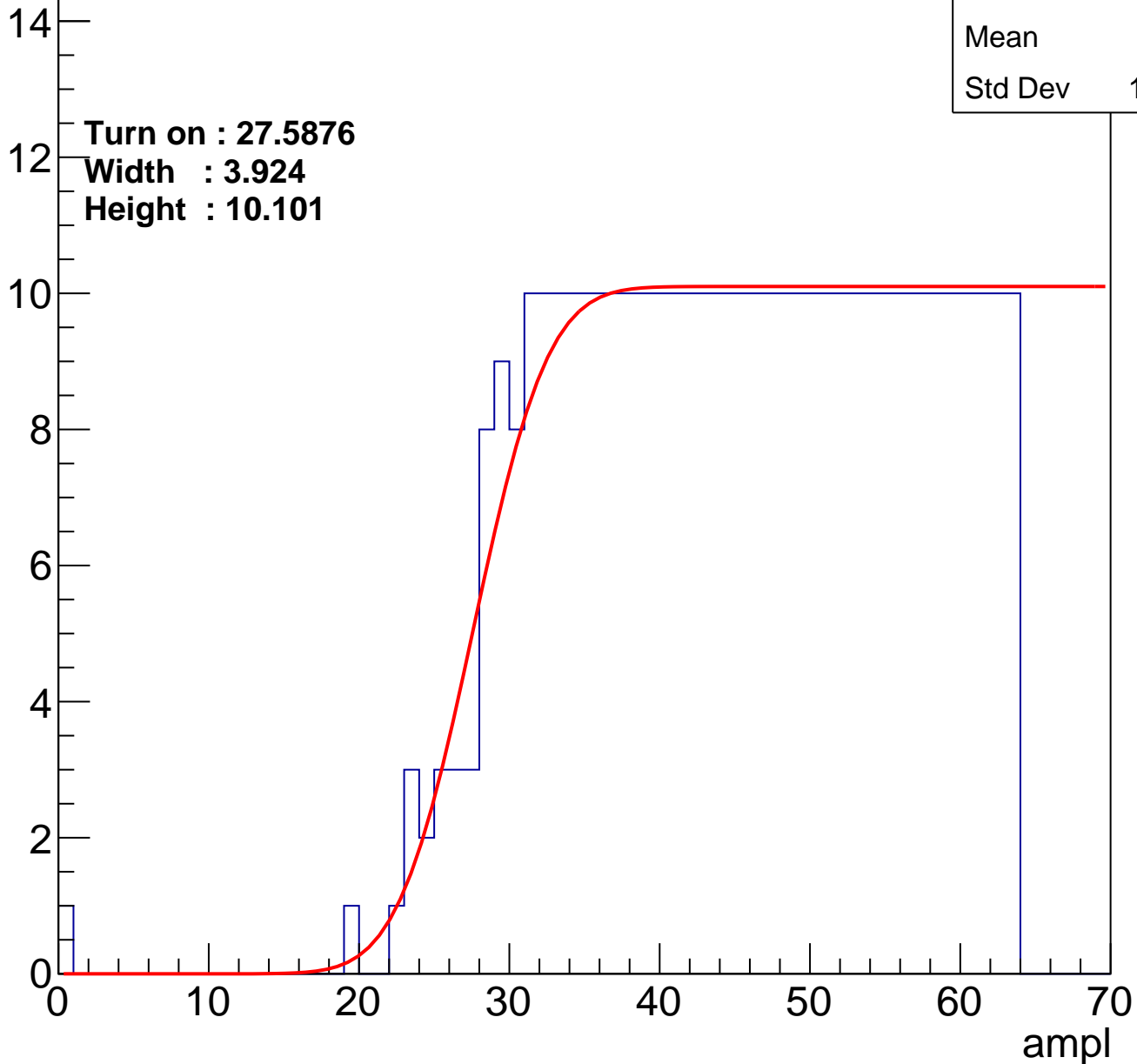
Entries	372
Mean	44.7
Std Dev	11.17

**Turn on : 27.5876**

**Width : 3.924**

**Height : 10.101**

Entry



# B0L000S, U1-ch4

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	372
Mean	44.65
Std Dev	11.32

**Turn on : 27.9973**

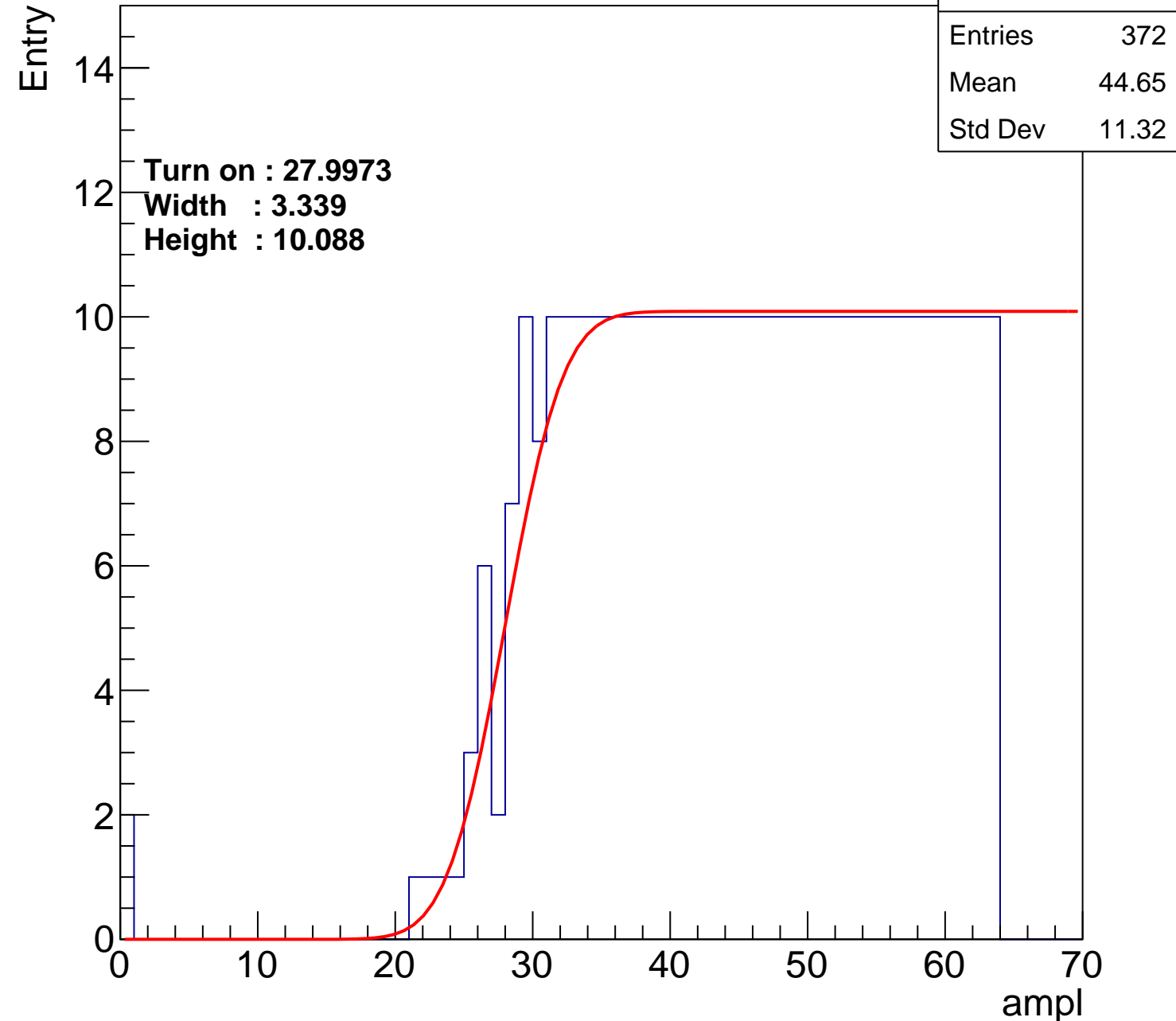
**Width : 3.339**

**Height : 10.088**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch5

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	378
Mean	44.22
Std Dev	11.84

**Turn on : 26.5749**

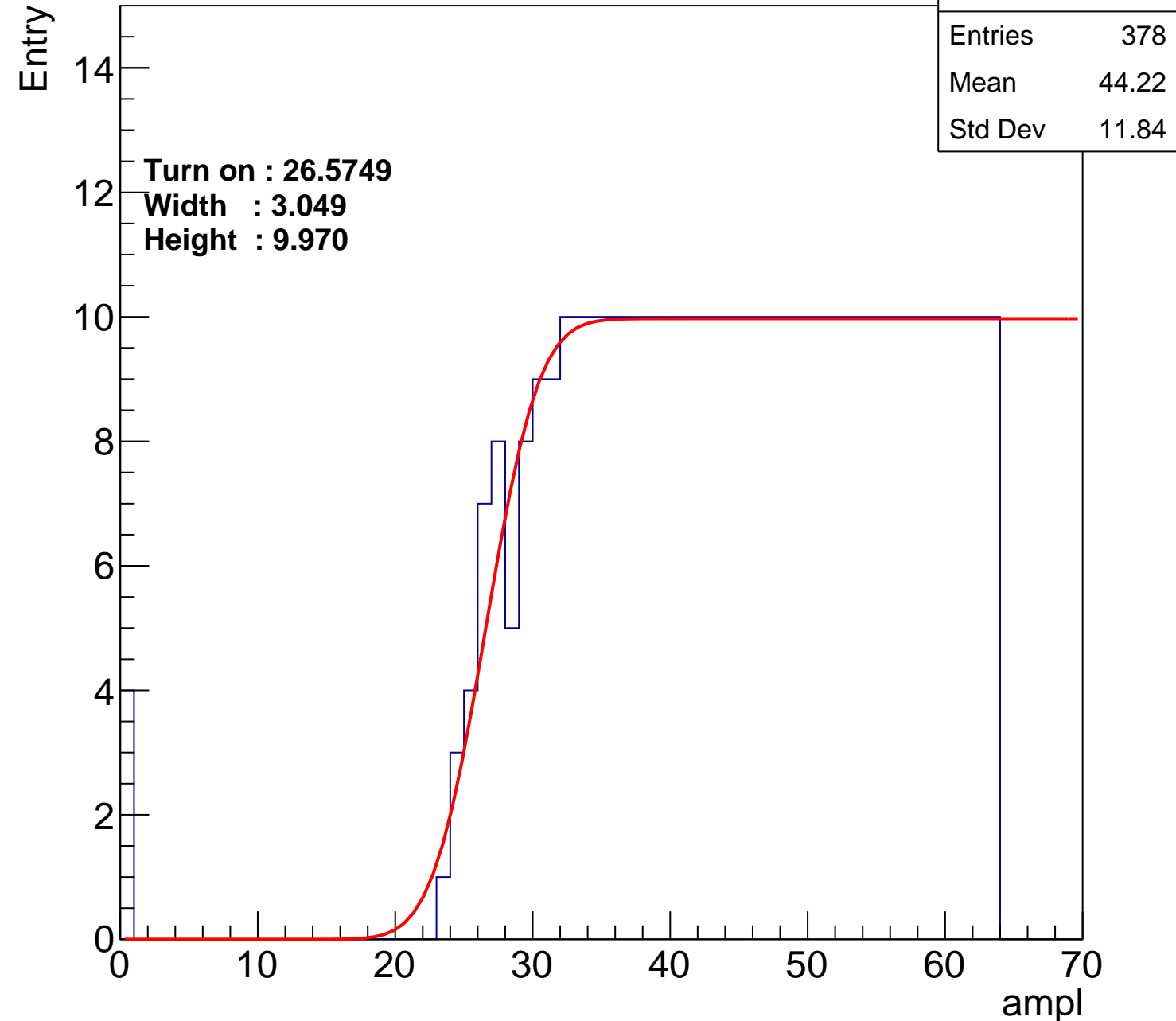
**Width : 3.049**

**Height : 9.970**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch6

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	373
Mean	44.6
Std Dev	11.34

Turn on : 27.1867

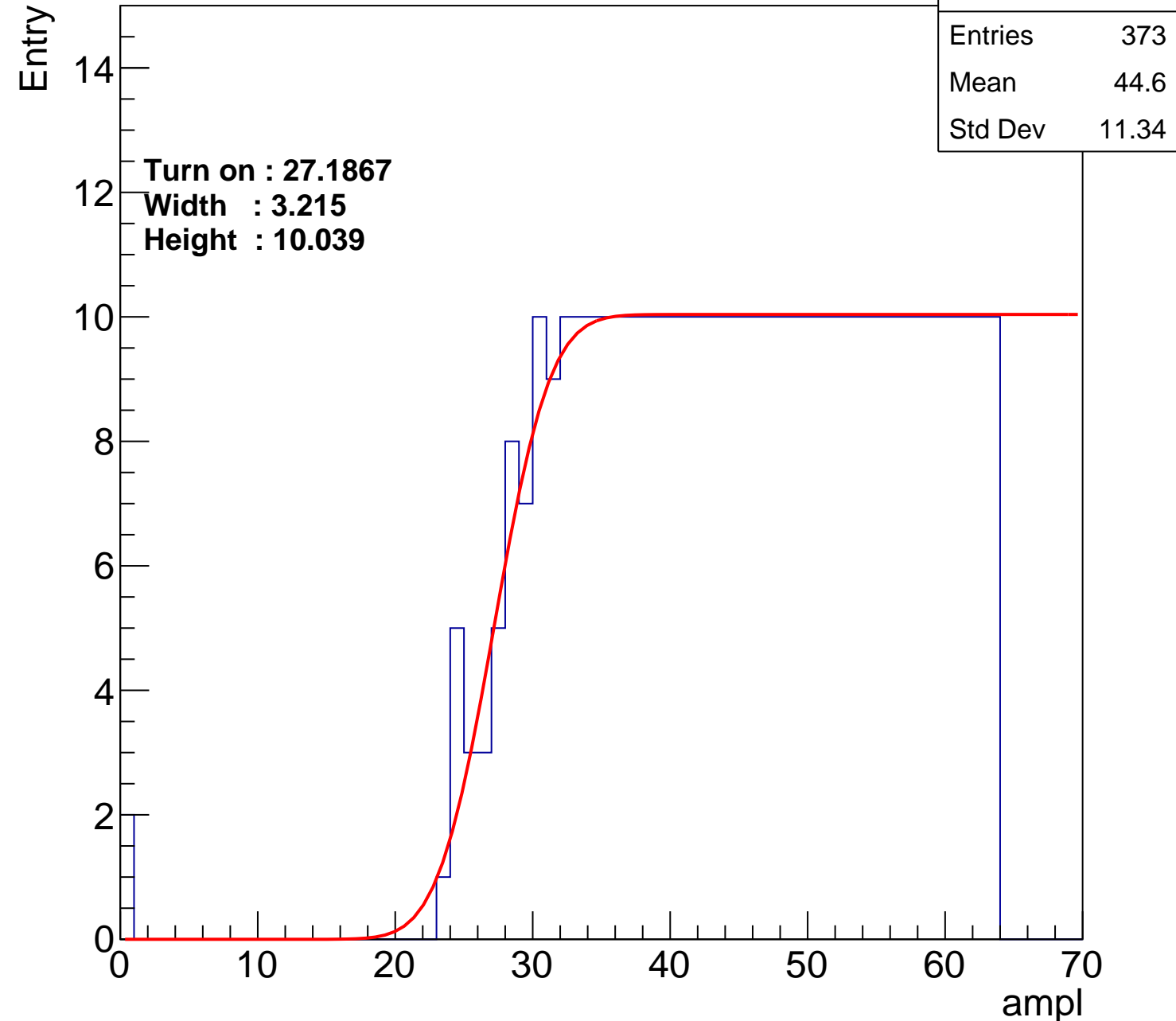
Width : 3.215

Height : 10.039

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L000S, U1-ch7

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	373
Mean	44.51
Std Dev	11.57

Turn on : 27.3697

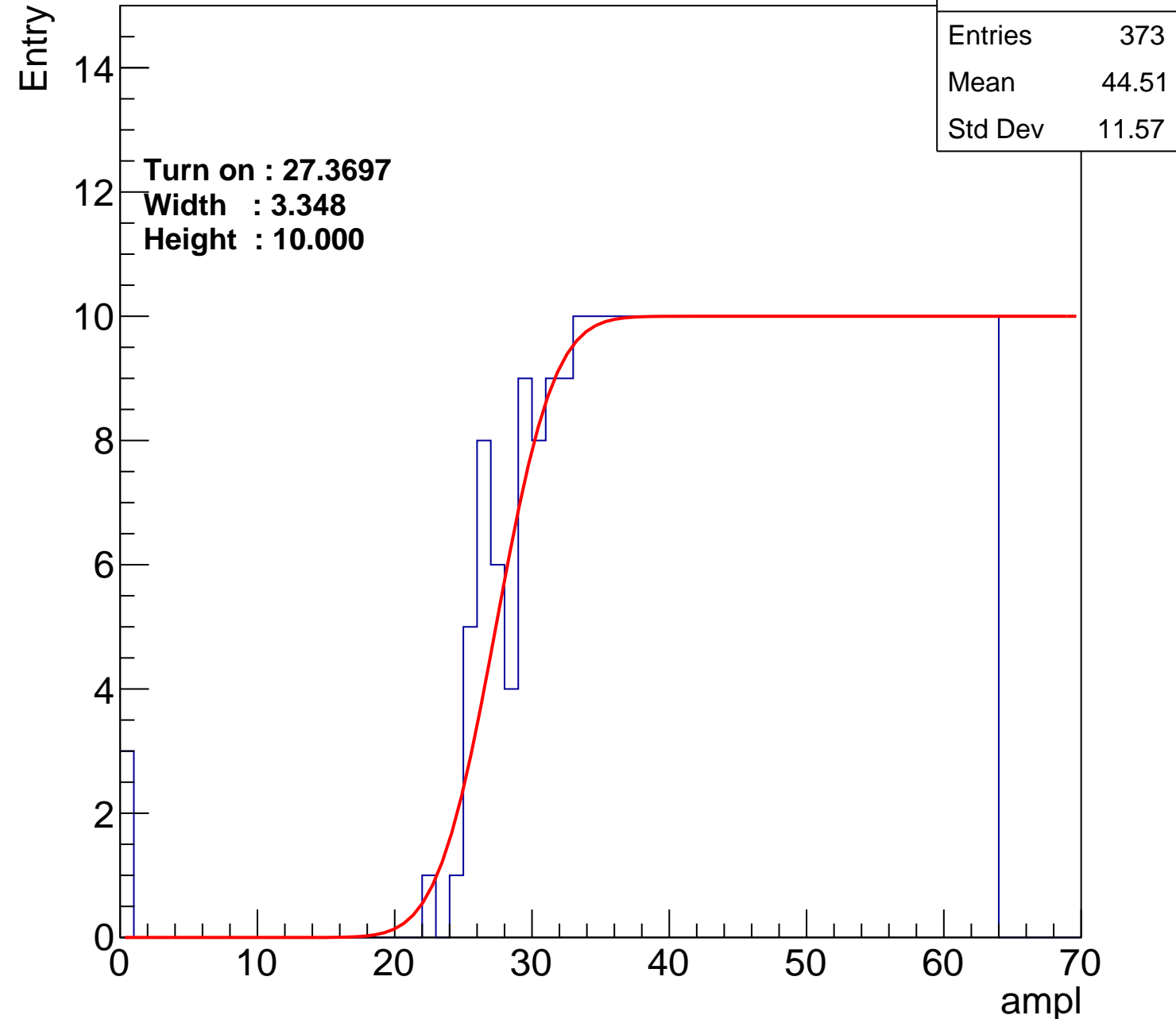
Width : 3.348

Height : 10.000

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch8

calib\_packv5\_042523\_0143.root, FC#5, port B1

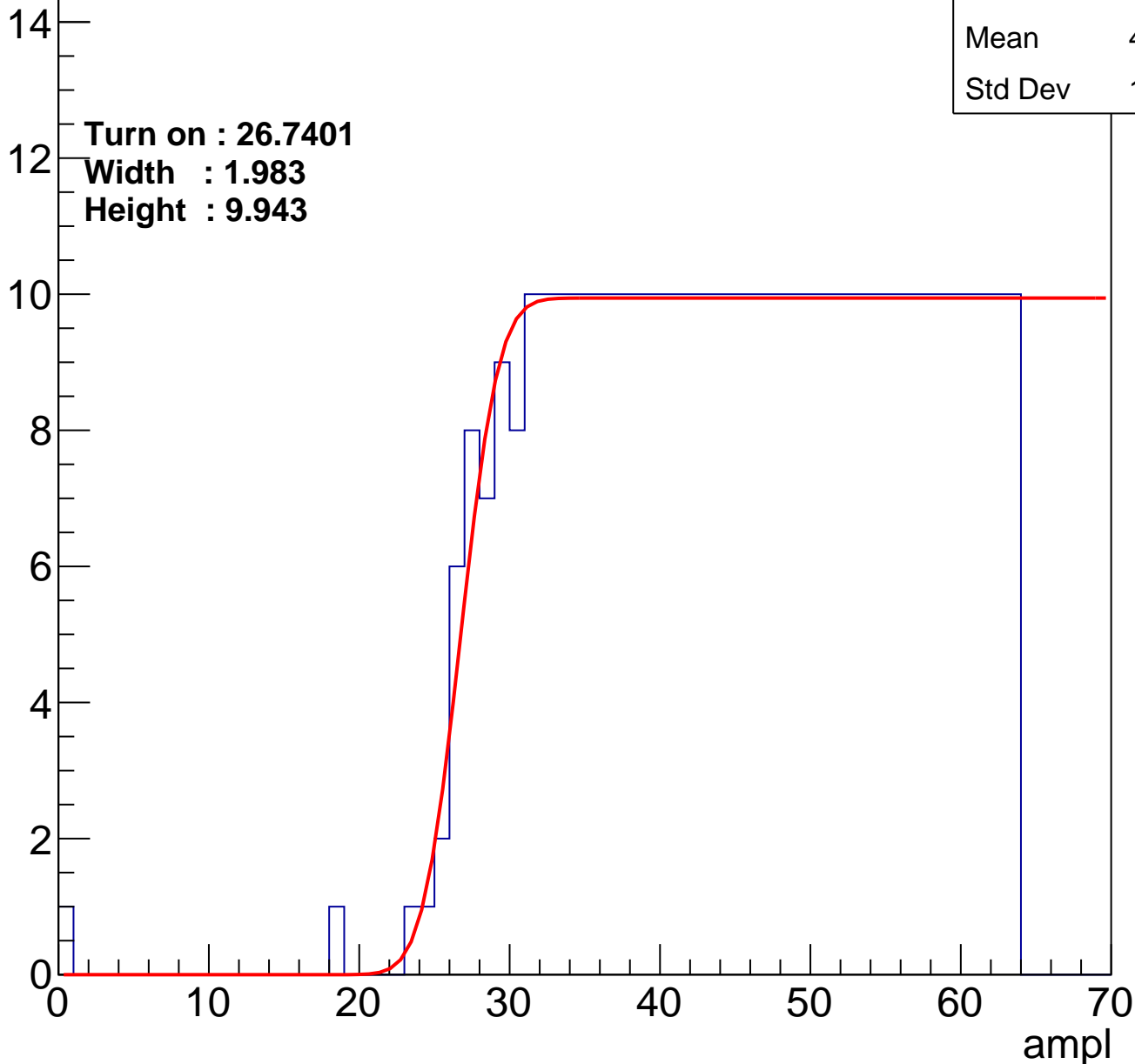
Entry

Entries	374
Mean	44.64
Std Dev	11.16

Turn on : 26.7401

Width : 1.983

Height : 9.943



# B0L000S, U1-ch9

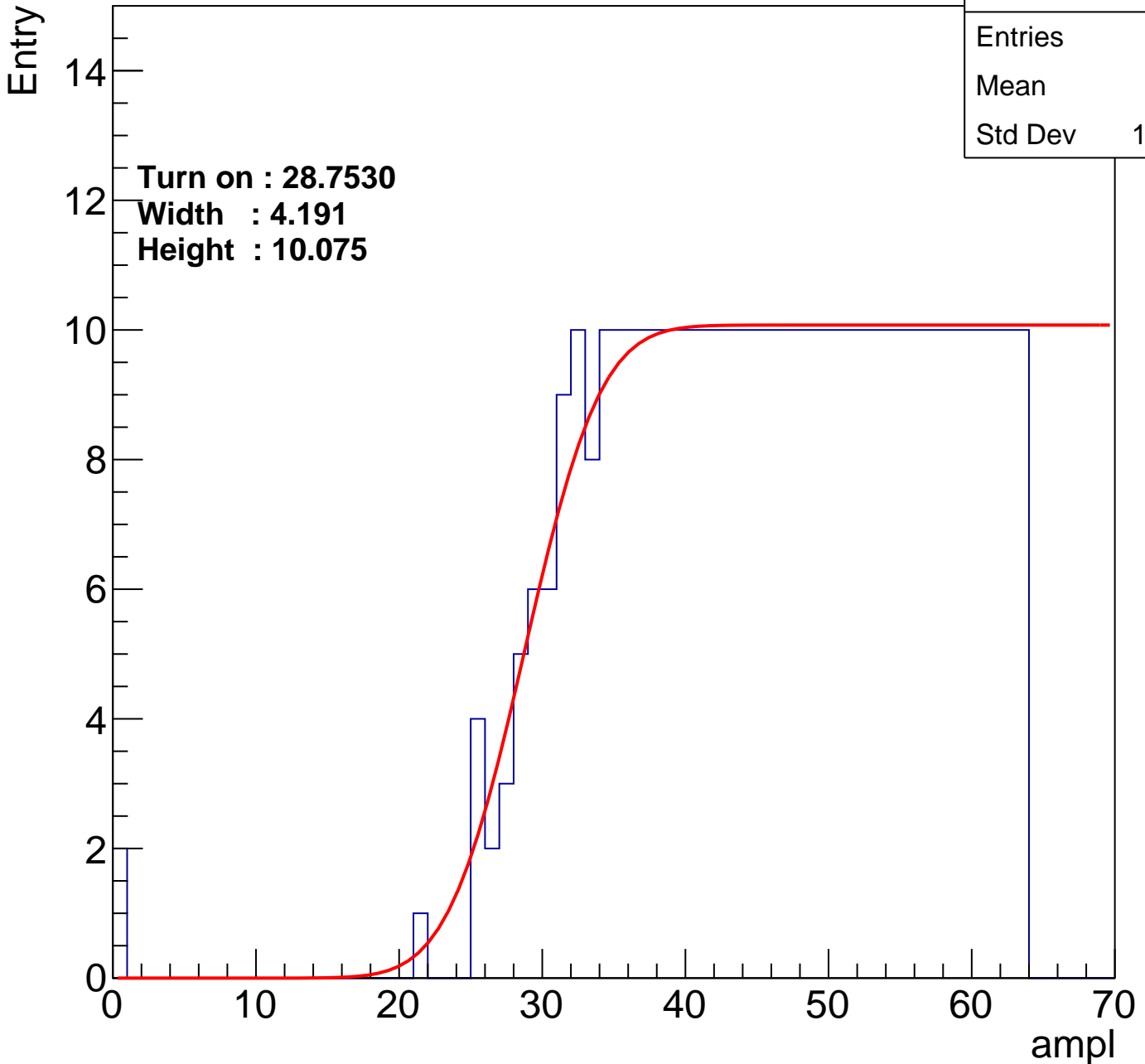
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	356
Mean	45.4
Std Dev	10.98

**Turn on : 28.7530**

**Width : 4.191**

**Height : 10.075**



# B0L000S, U1-ch10

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	374
Mean	44.59
Std Dev	11.32

**Turn on : 27.1517**

**Width : 2.931**

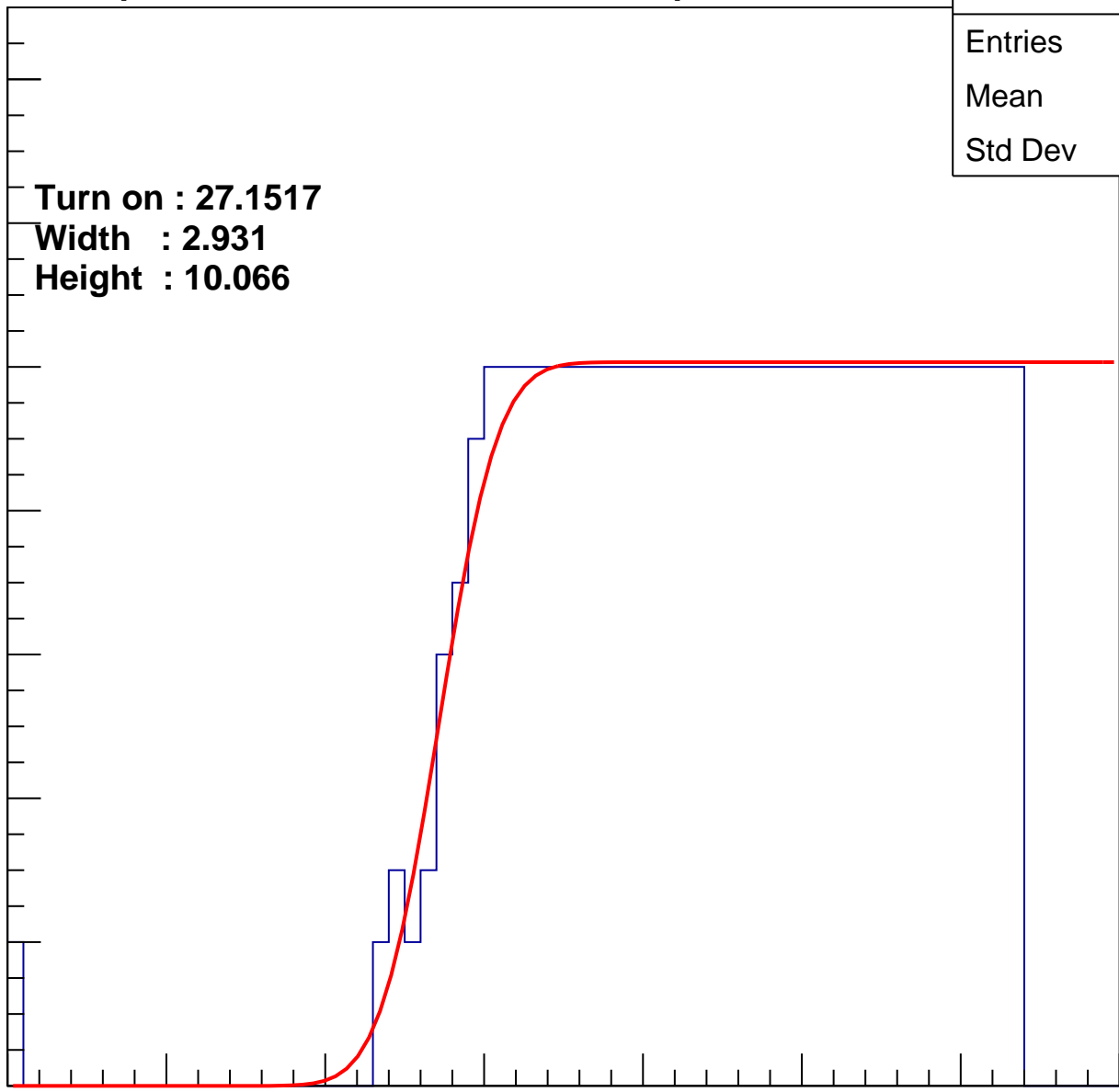
**Height : 10.066**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L000S, U1-ch11

calib\_packv5\_042523\_0143.root, FC#5, port B1

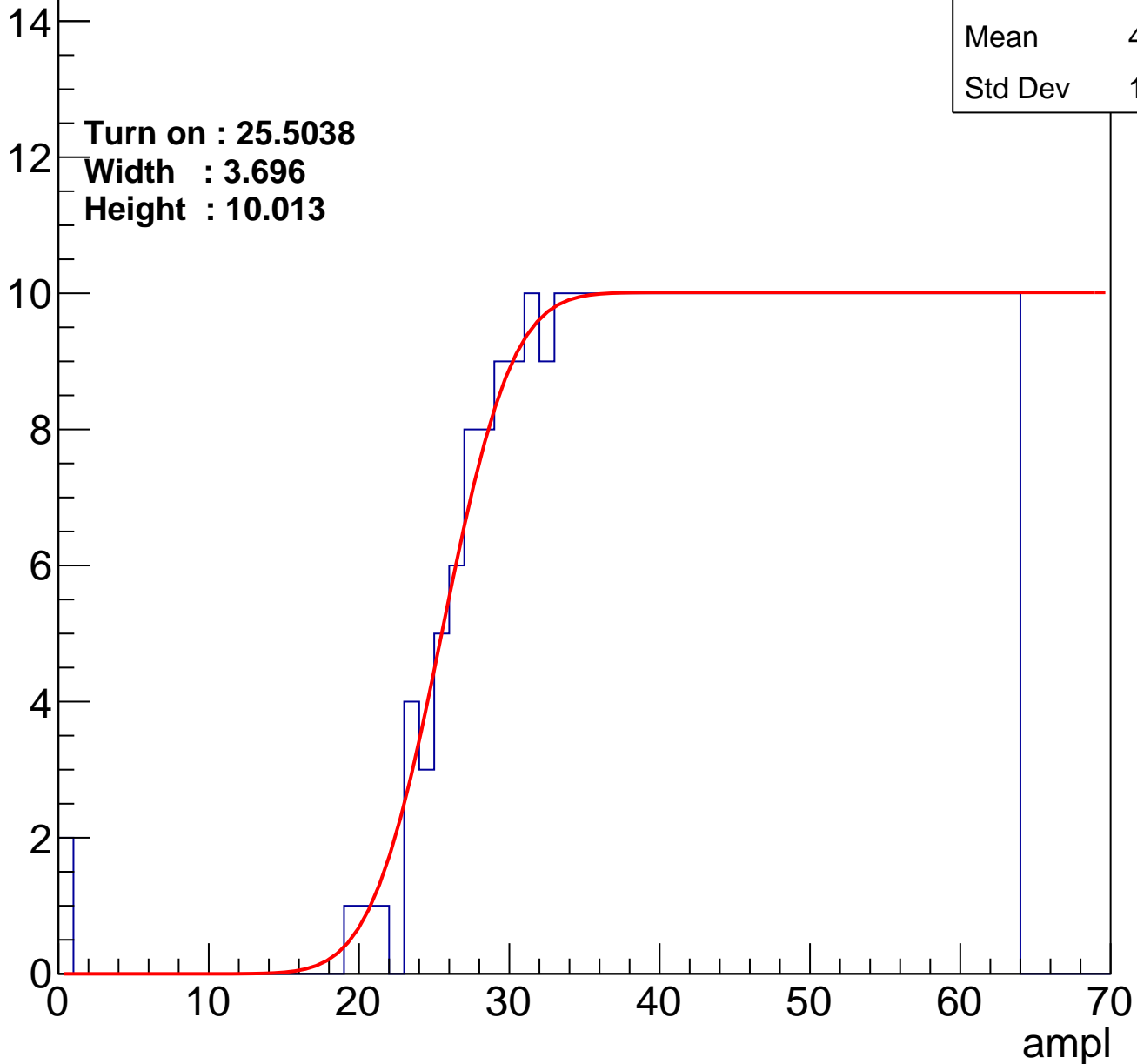
Entries	386
Mean	43.92
Std Dev	11.74

**Turn on : 25.5038**

**Width : 3.696**

**Height : 10.013**

Entry



# B0L000S, U1-ch12

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	385
Mean	43.99
Std Dev	11.75

Turn on : 25.5592

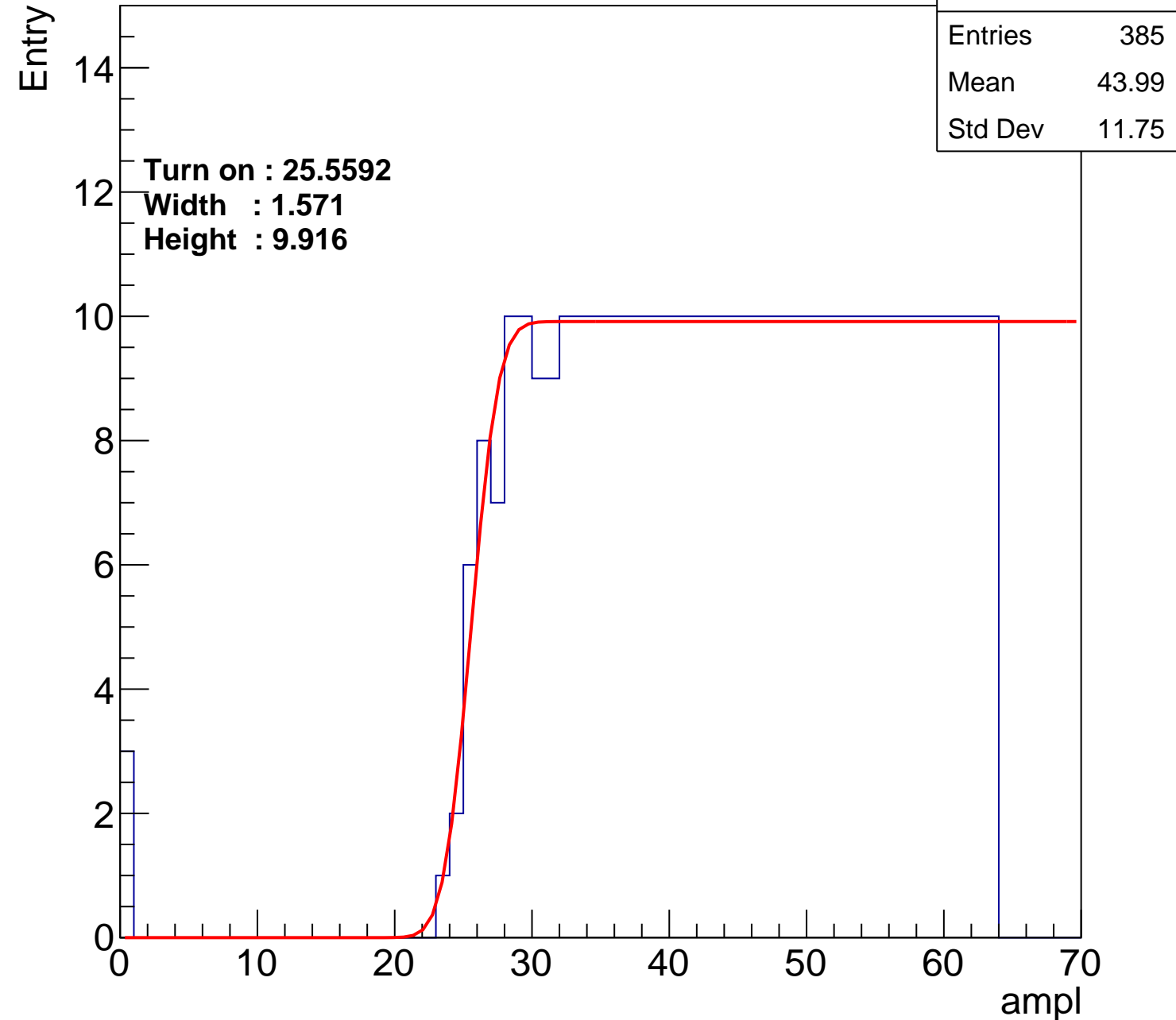
Width : 1.571

Height : 9.916

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch13

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	343
Mean	45.96
Std Dev	10.9

Turn on : 31.0182

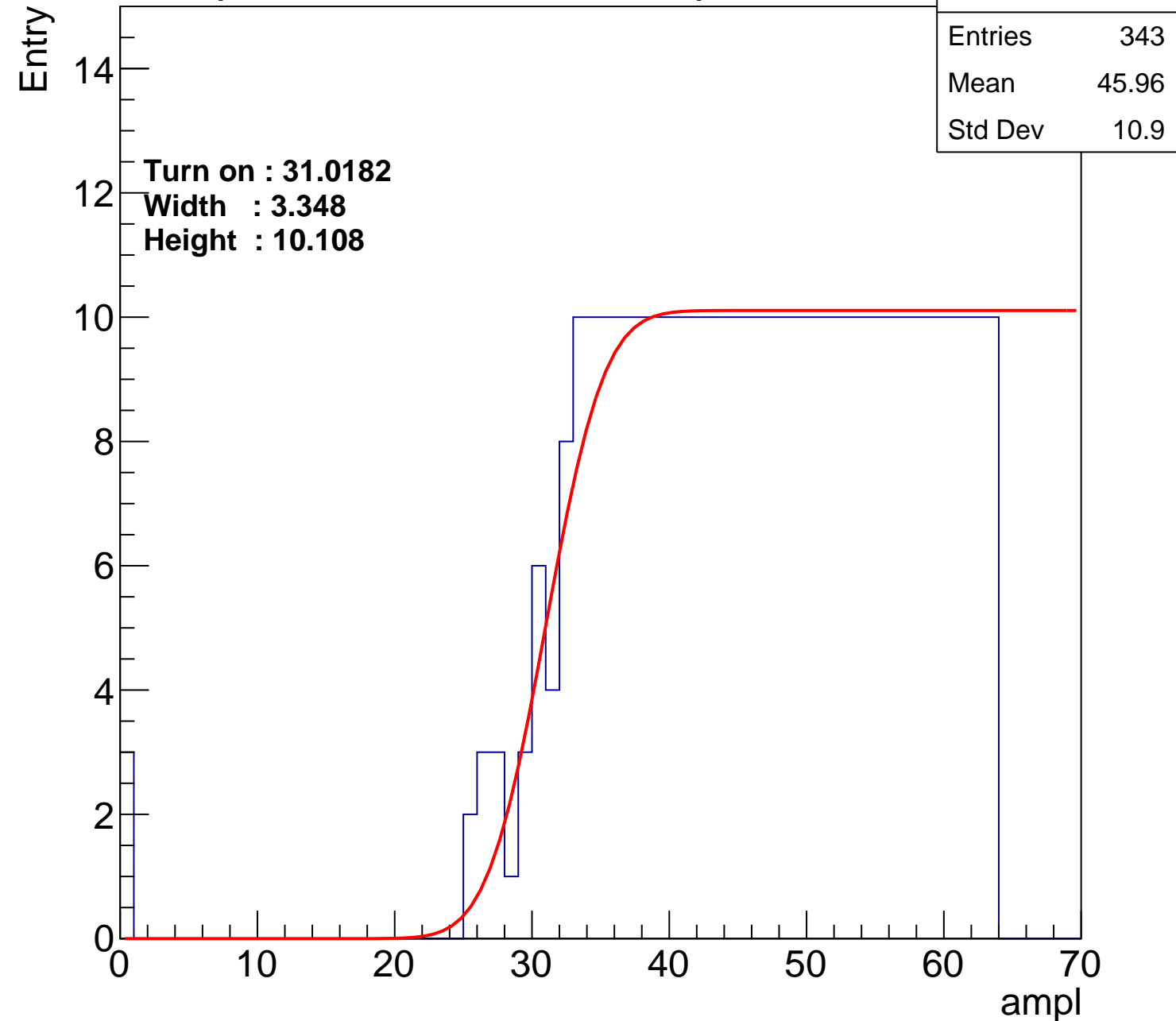
Width : 3.348

Height : 10.108

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch14

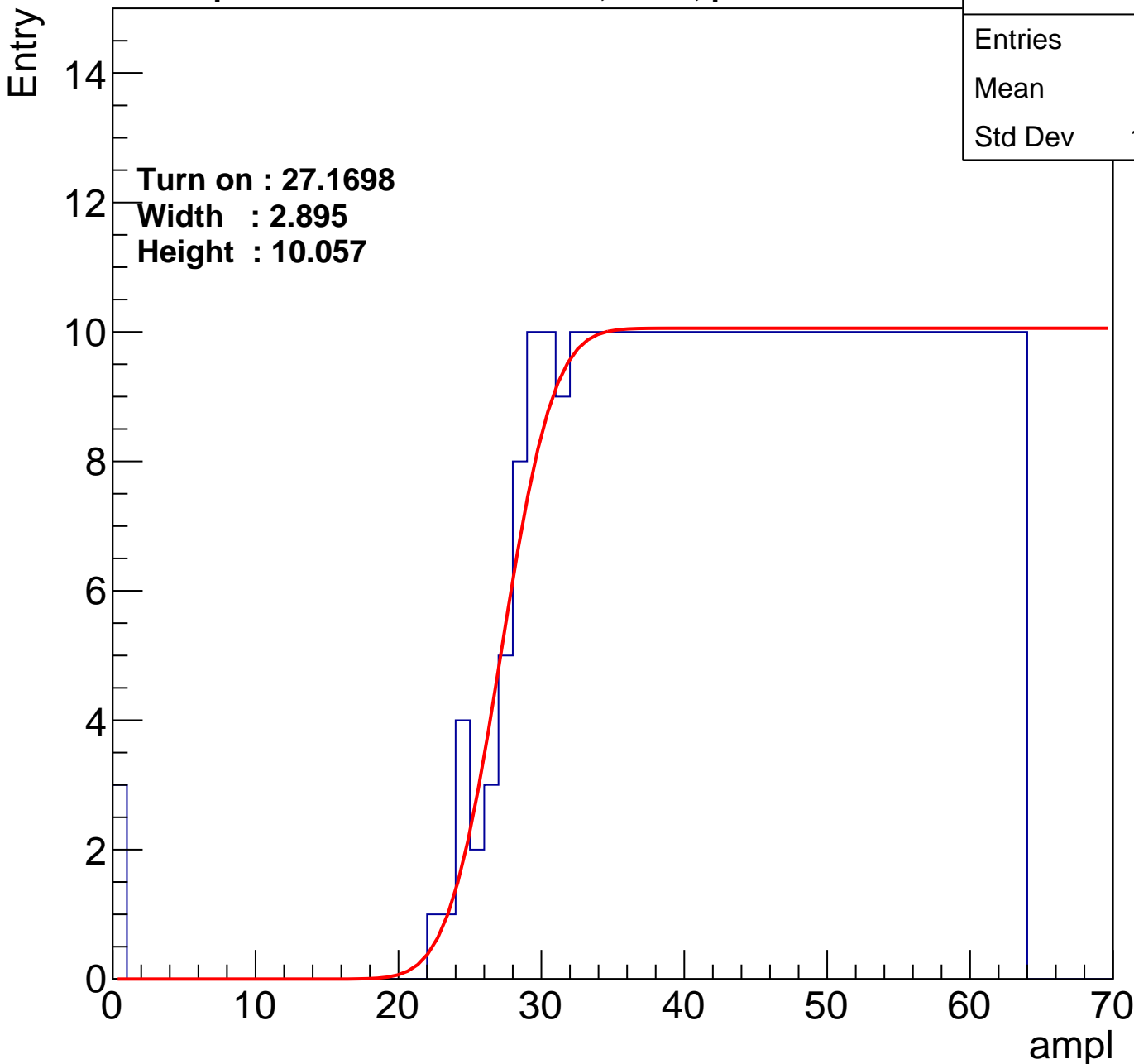
**calib\_packv5\_042523\_0143.root, FC#5, port B1**

Entries	376
Mean	44.41
Std Dev	11.58

**Turn on : 27.1698**

**Width : 2.895**

**Height : 10.057**





# B0L000S, U1-ch15

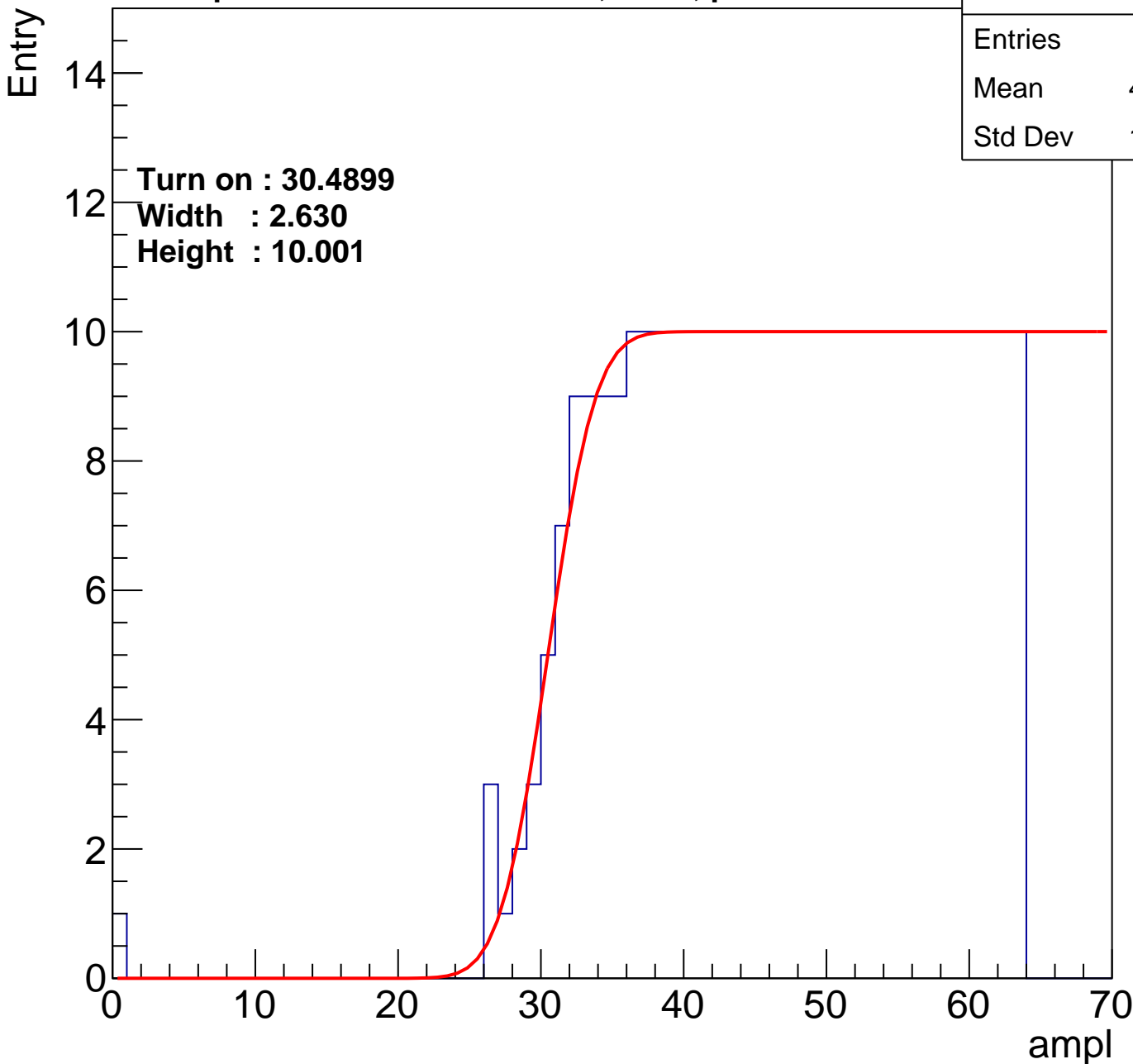
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	338
Mean	46.39
Std Dev	10.23

Turn on : 30.4899

Width : 2.630

Height : 10.001



# B0L000S, U1-ch16

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	363
Mean	45.15
Std Dev	10.9

**Turn on : 29.1114**

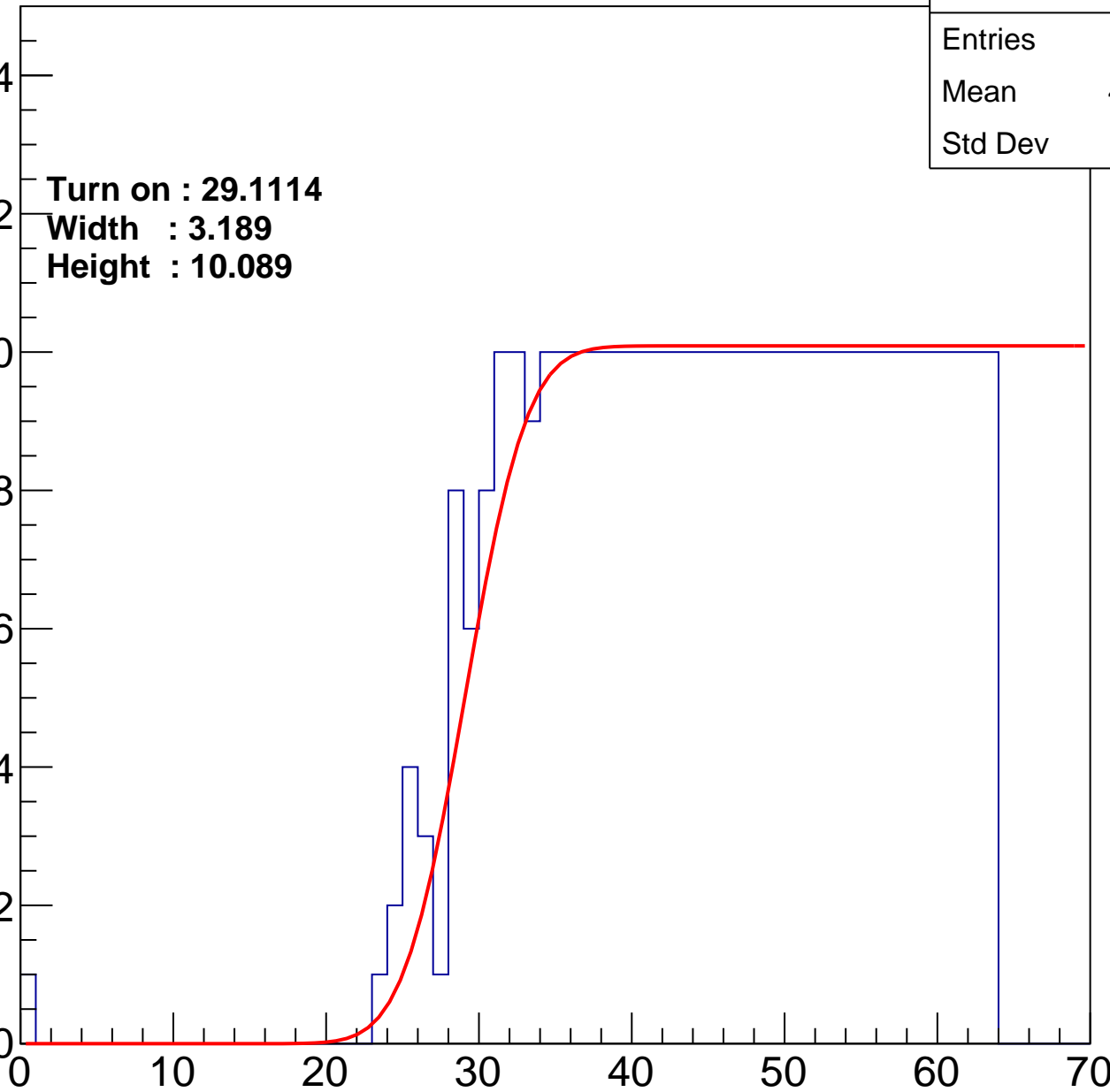
**Width : 3.189**

**Height : 10.089**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# BOL000S, U1-ch17

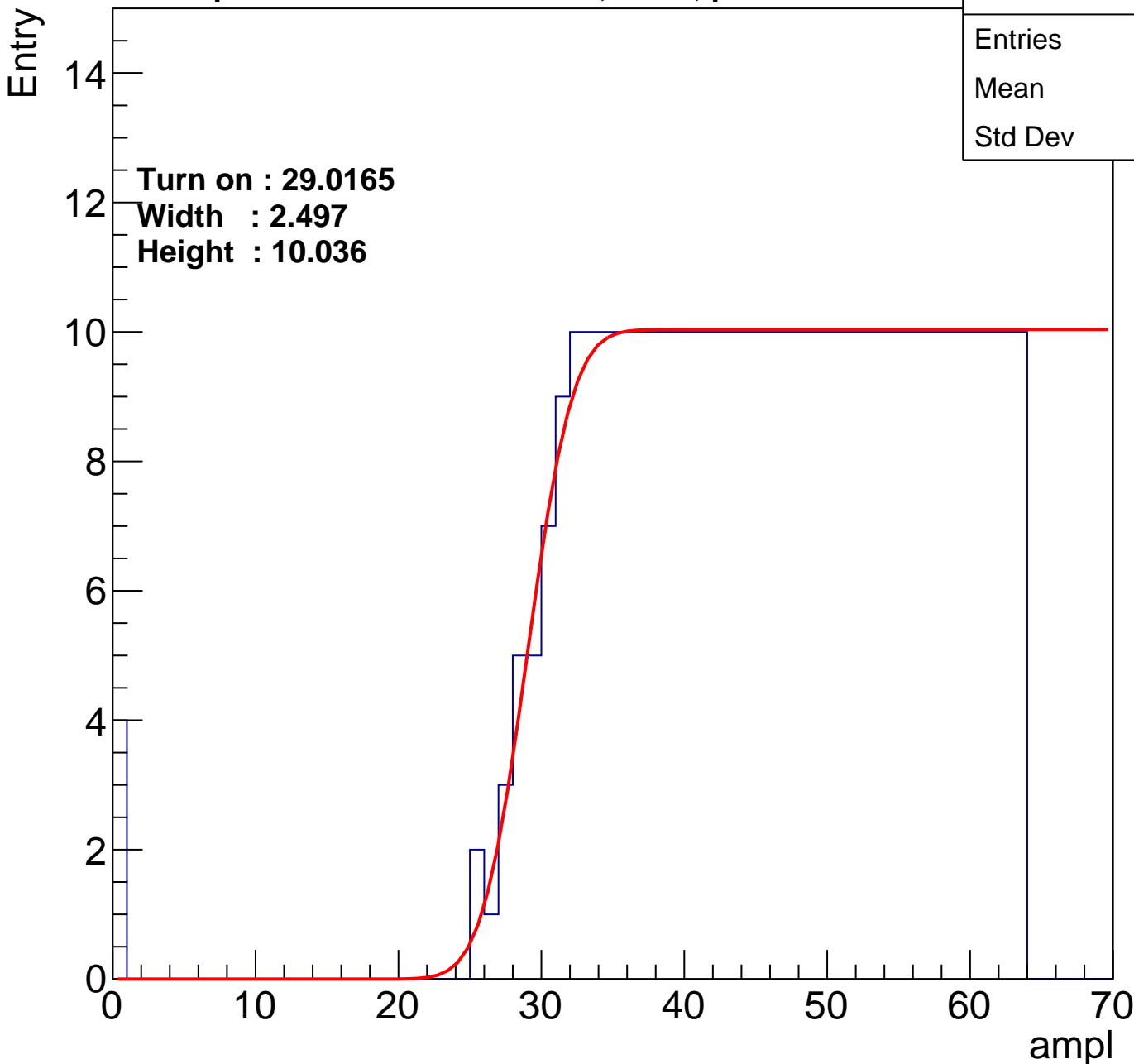
**calib\_packv5\_042523\_0143.root, FC#5, port B1**

**Turn on : 29.0165**

**Width : 2.497**

**Height : 10.036**

Entries	356
Mean	45.31
Std Dev	11.31



# B0L000S, U1-ch18

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	352
Mean	45.54
Std Dev	11.07

Turn on : 29.9634

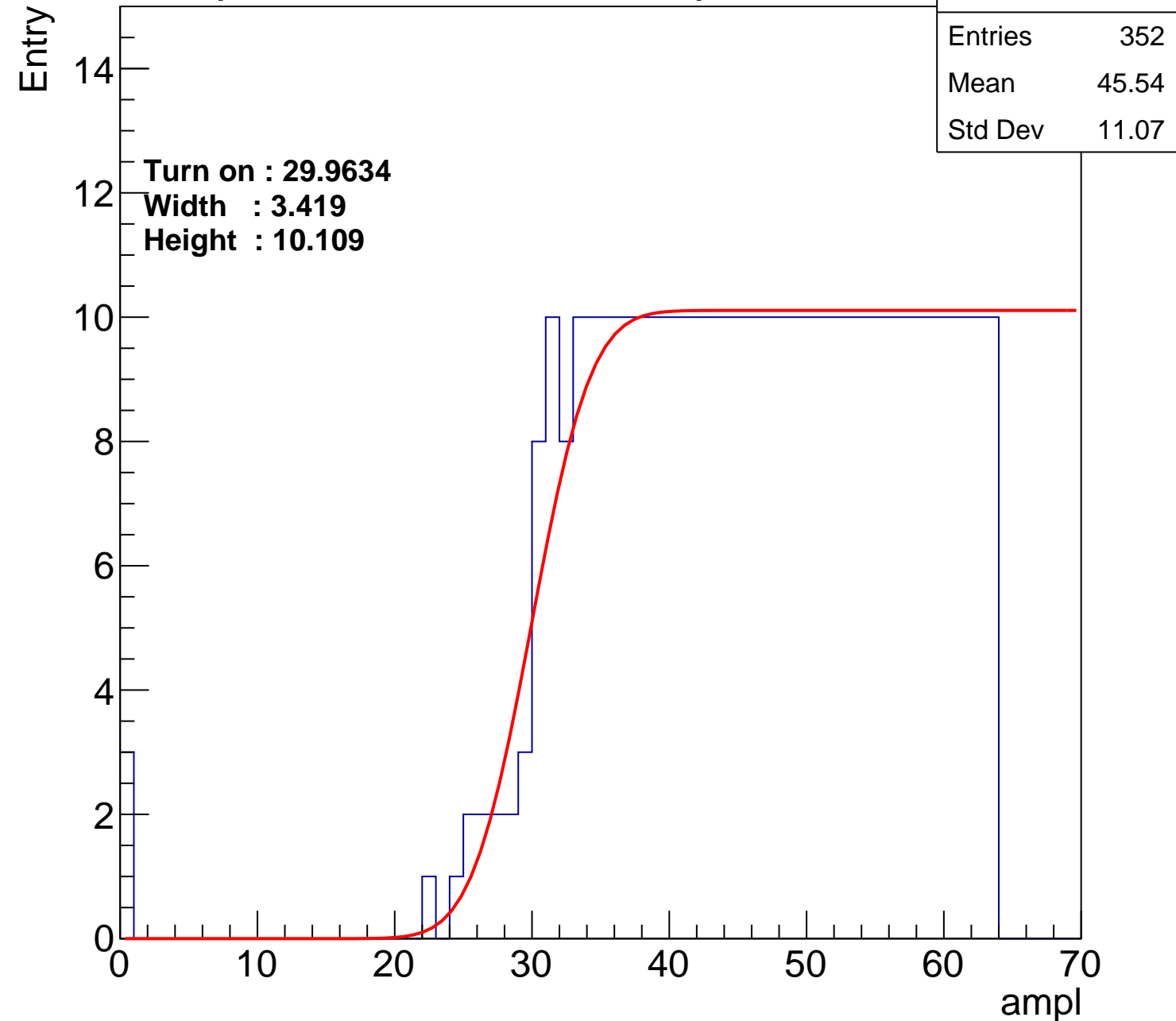
Width : 3.419

Height : 10.109

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch19

calib\_packv5\_042523\_0143.root, FC#5, port B1

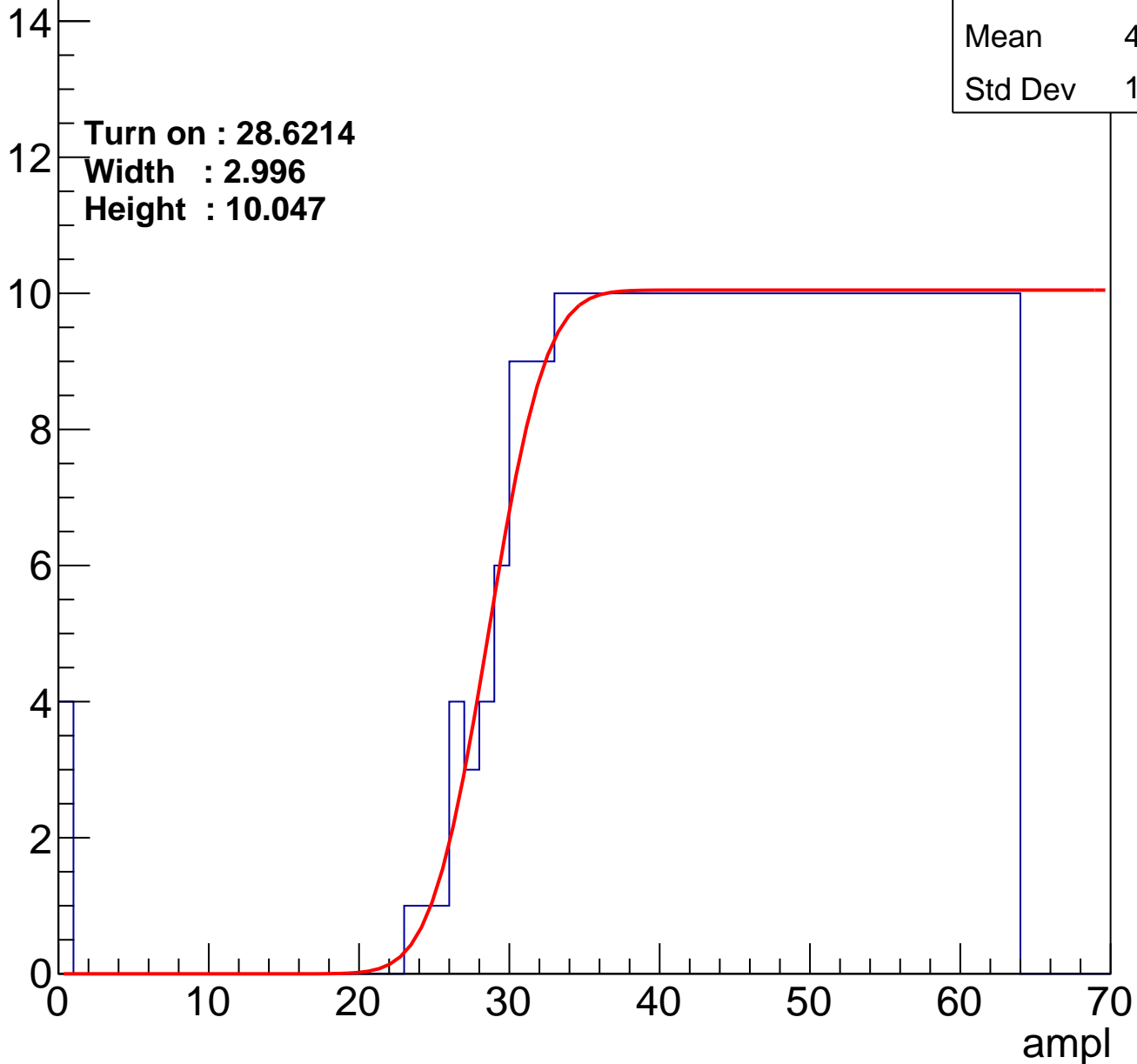
Entries	361
Mean	45.04
Std Dev	11.46

Turn on : 28.6214

Width : 2.996

Height : 10.047

Entry



# B0L000S, U1-ch20

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	364
Mean	45.01
Std Dev	11.26

**Turn on : 28.2273**

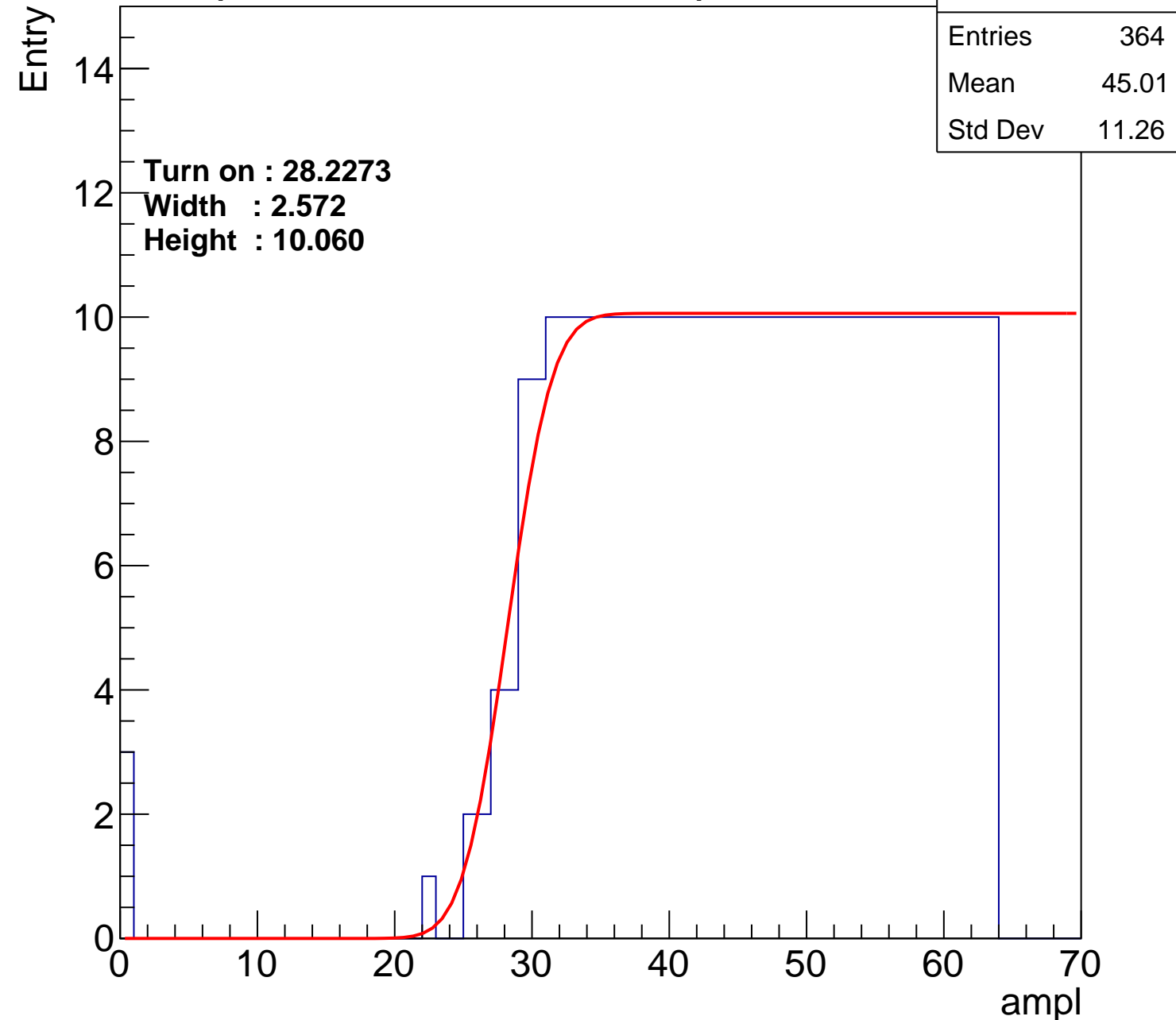
**Width : 2.572**

**Height : 10.060**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch21

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	383
Mean	44.15
Std Dev	11.53

Turn on : 25.7611

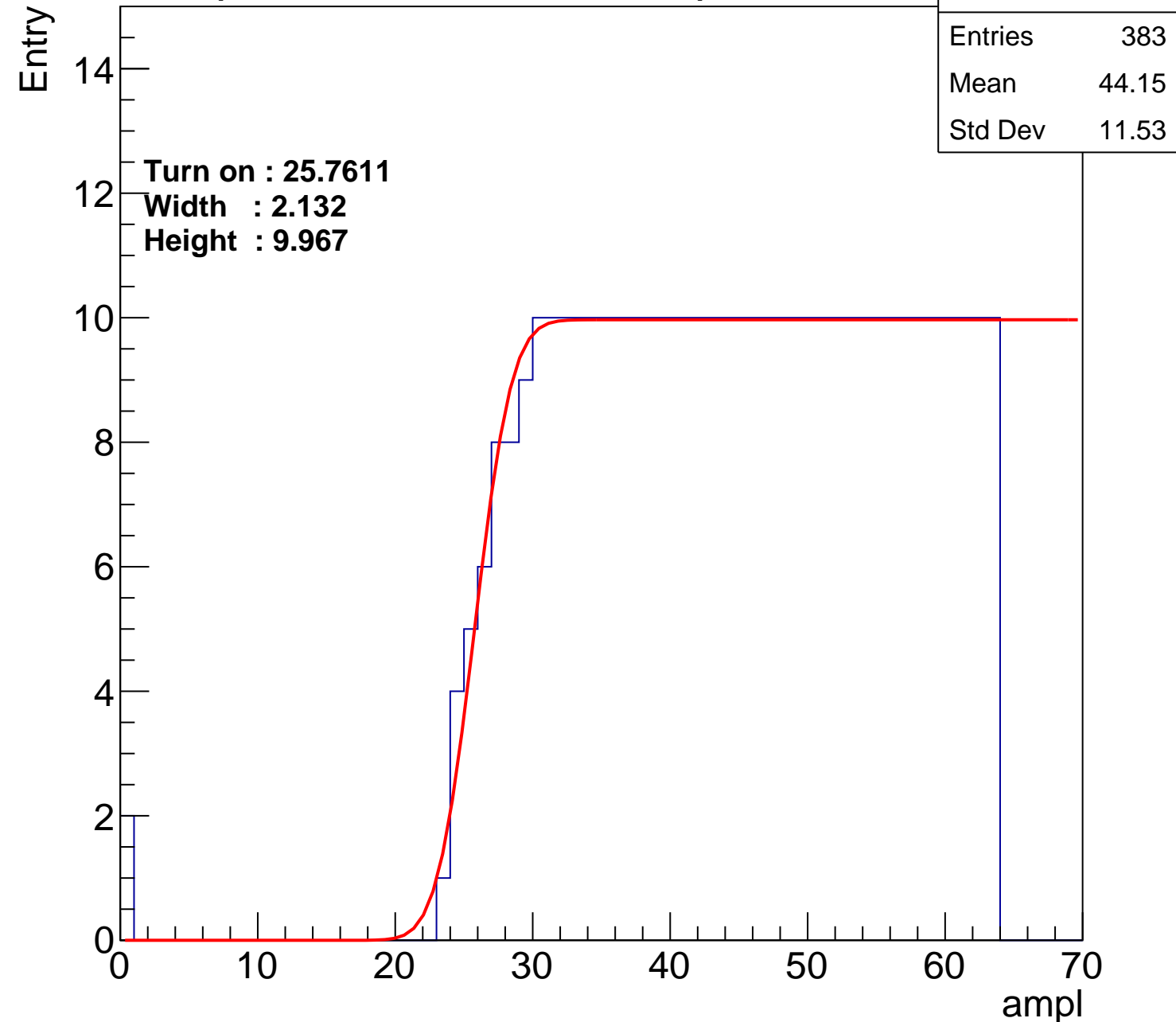
Width : 2.132

Height : 9.967

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch22

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	369
Mean	44.76
Std Dev	11.32

**Turn on : 27.5723**

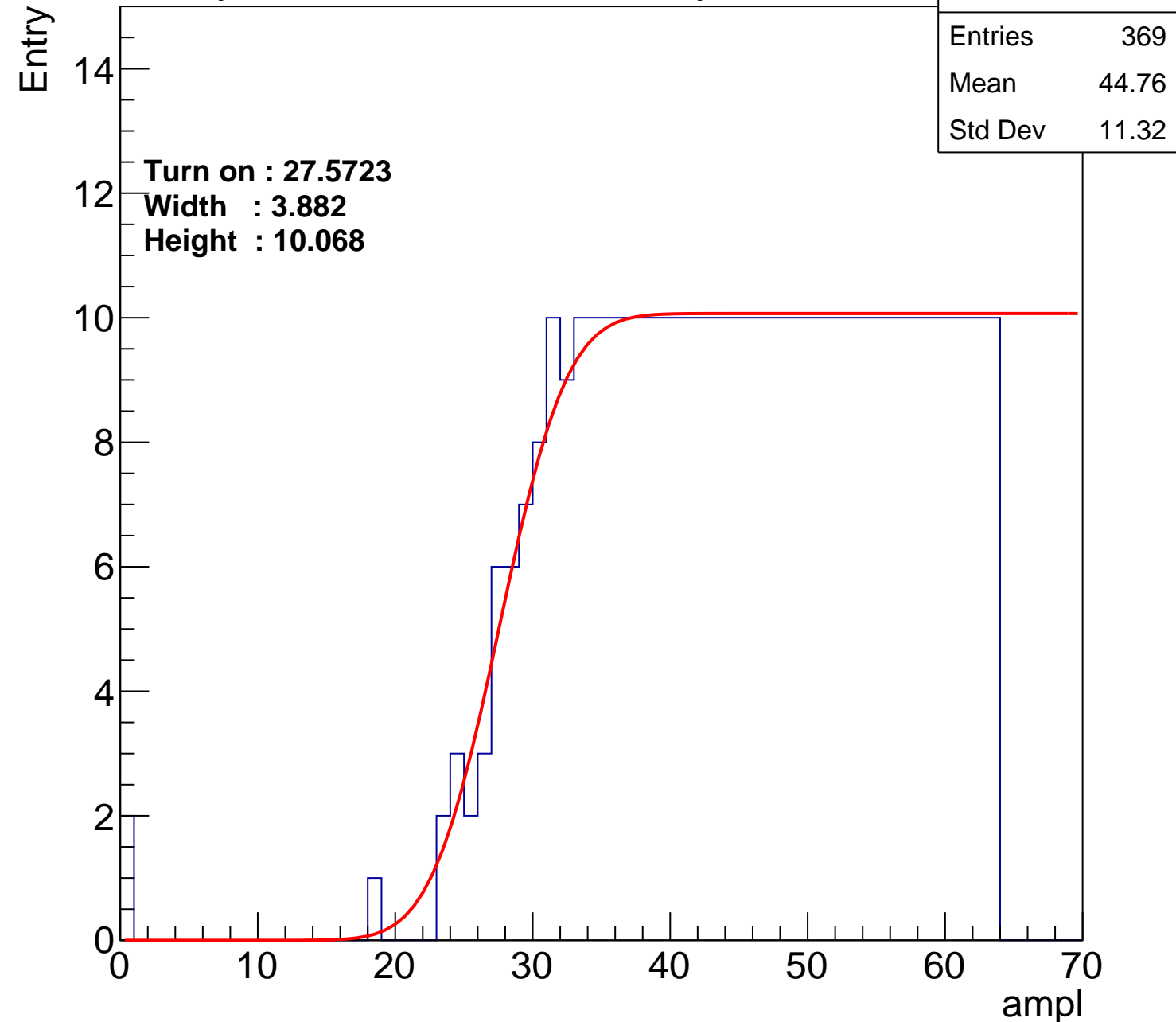
**Width : 3.882**

**Height : 10.068**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L000S, U1-ch23

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	361
Mean	44.89
Std Dev	11.78

**Turn on : 28.7304**

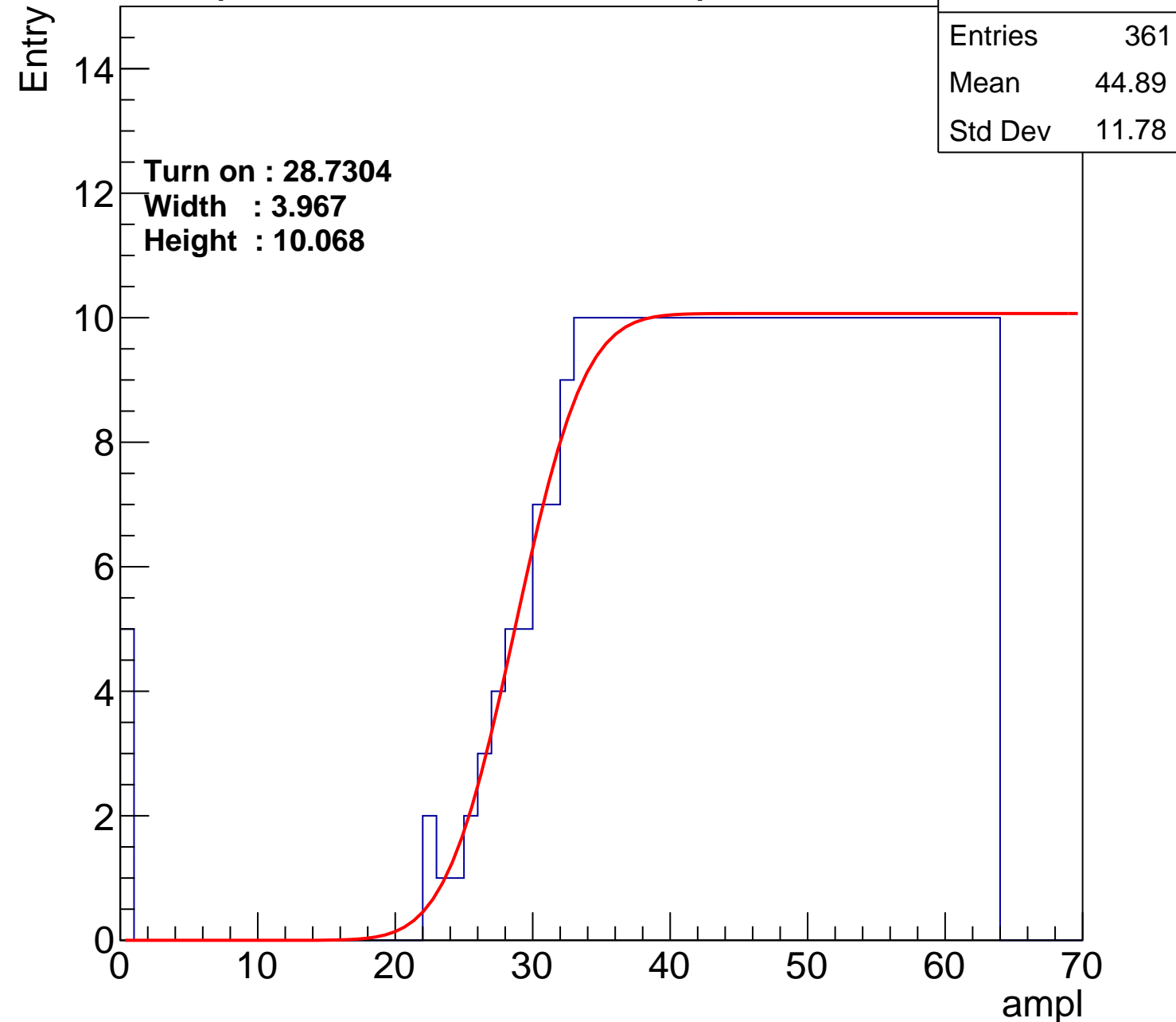
**Width : 3.967**

**Height : 10.068**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch24

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	378
Mean	44.21
Std Dev	11.85

Turn on : 27.2330

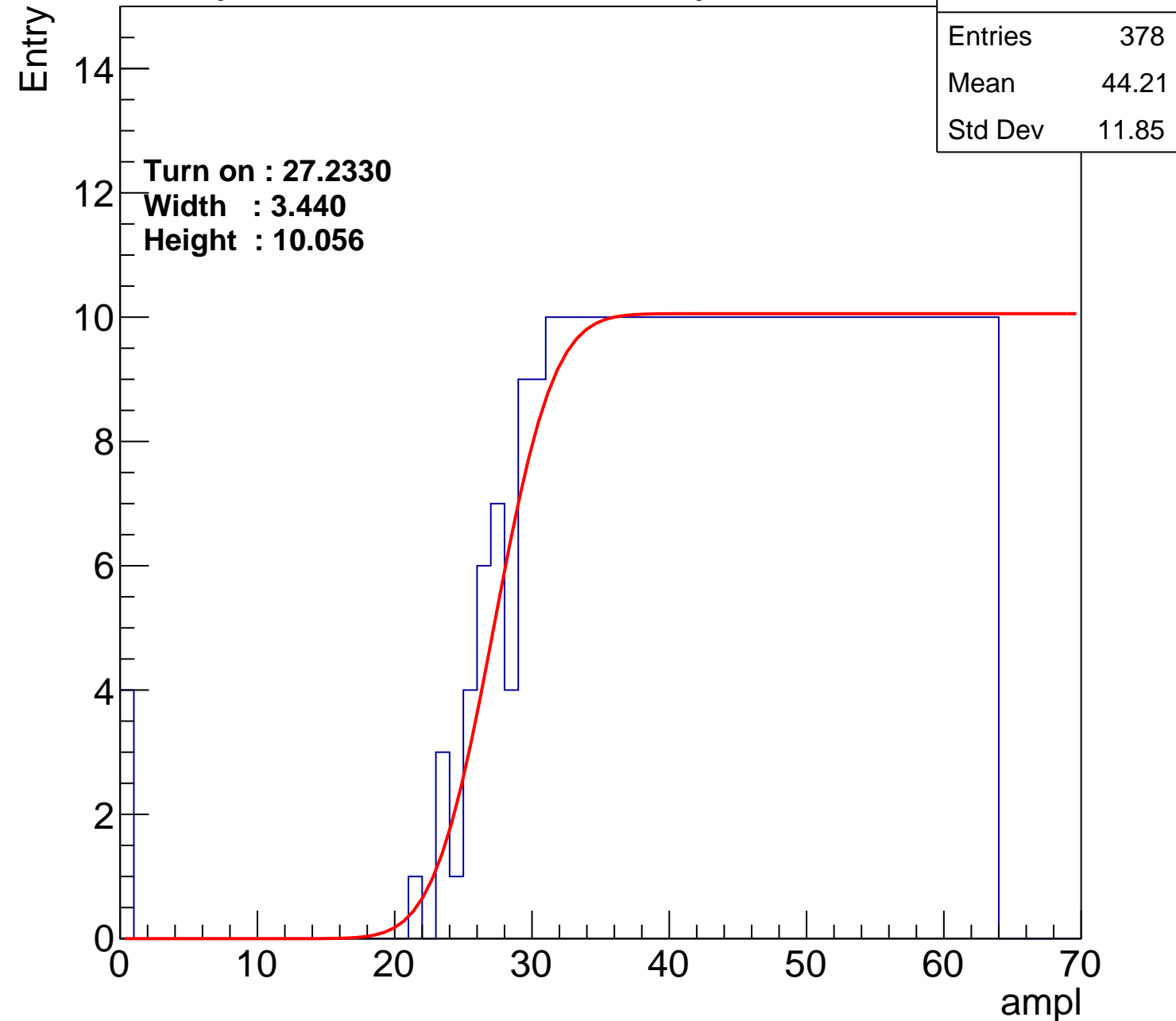
Width : 3.440

Height : 10.056

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch25

calib\_packv5\_042523\_0143.root, FC#5, port B1

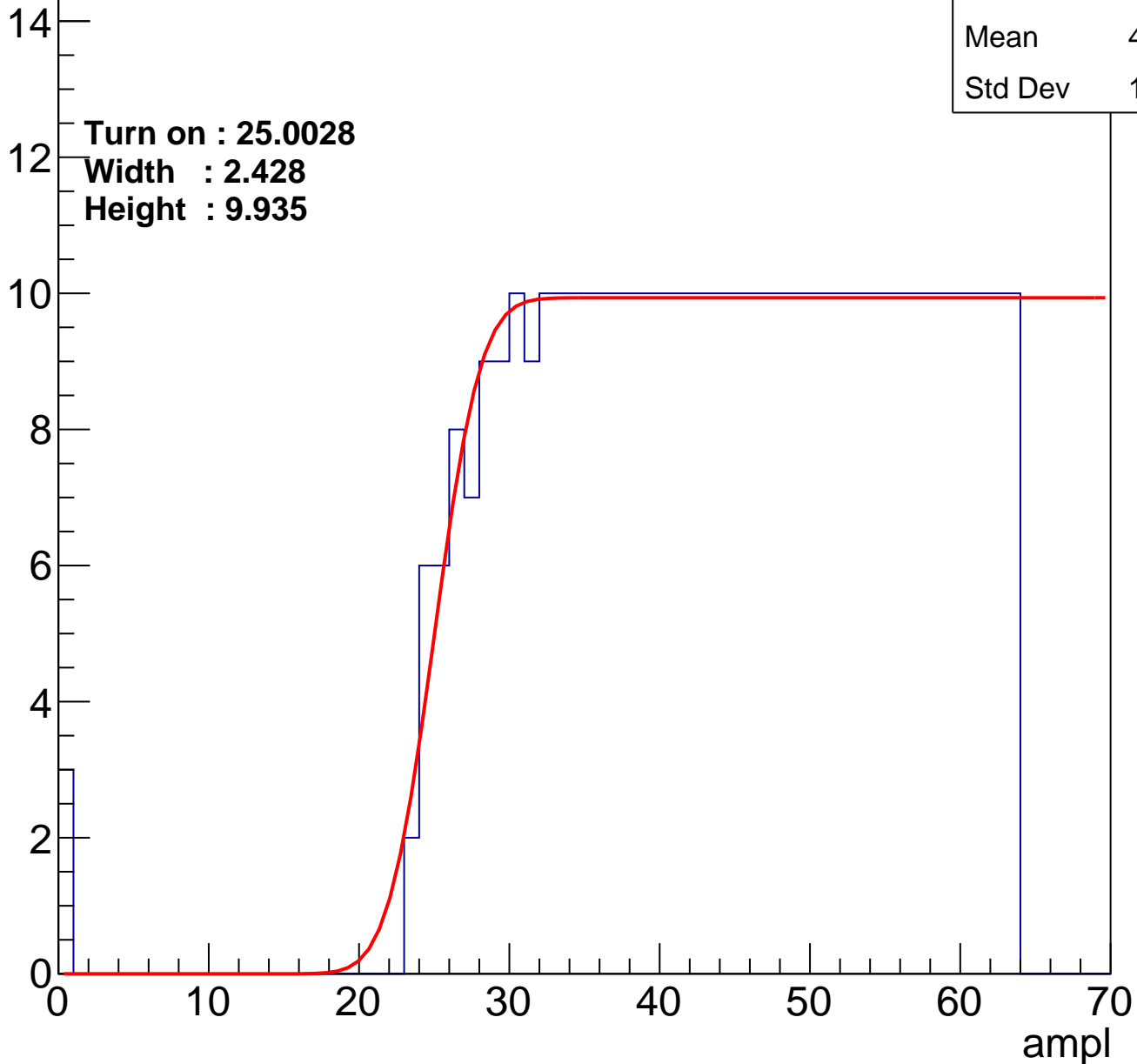
Entries	389
Mean	43.78
Std Dev	11.88

Turn on : 25.0028

Width : 2.428

Height : 9.935

Entry



# B0L000S, U1-ch26

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	372
Mean	44.48
Std Dev	11.74

Turn on : 27.5219

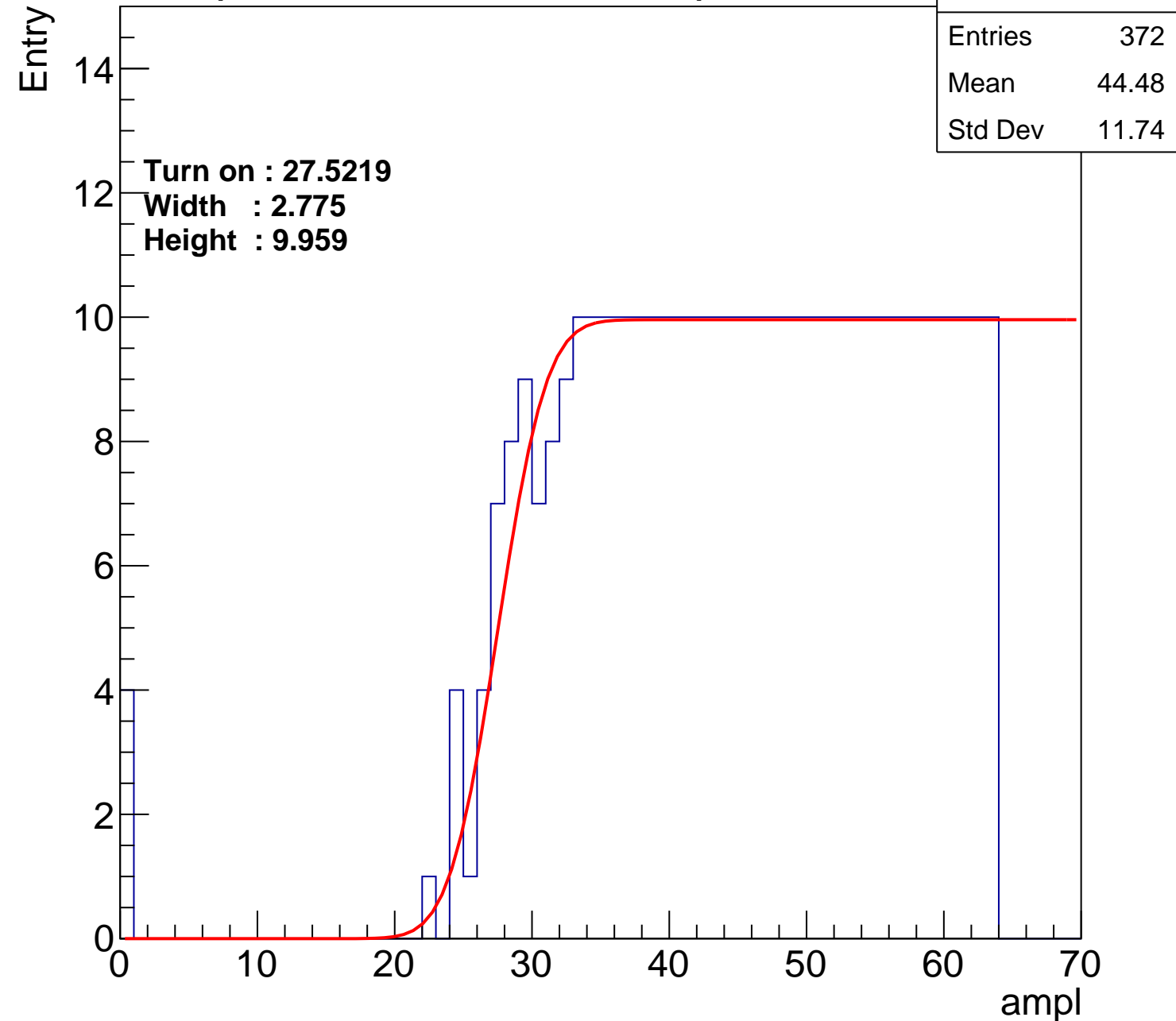
Width : 2.775

Height : 9.959

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch27

**calib\_packv5\_042523\_0143.root, FC#5, port B1**

Entries	371
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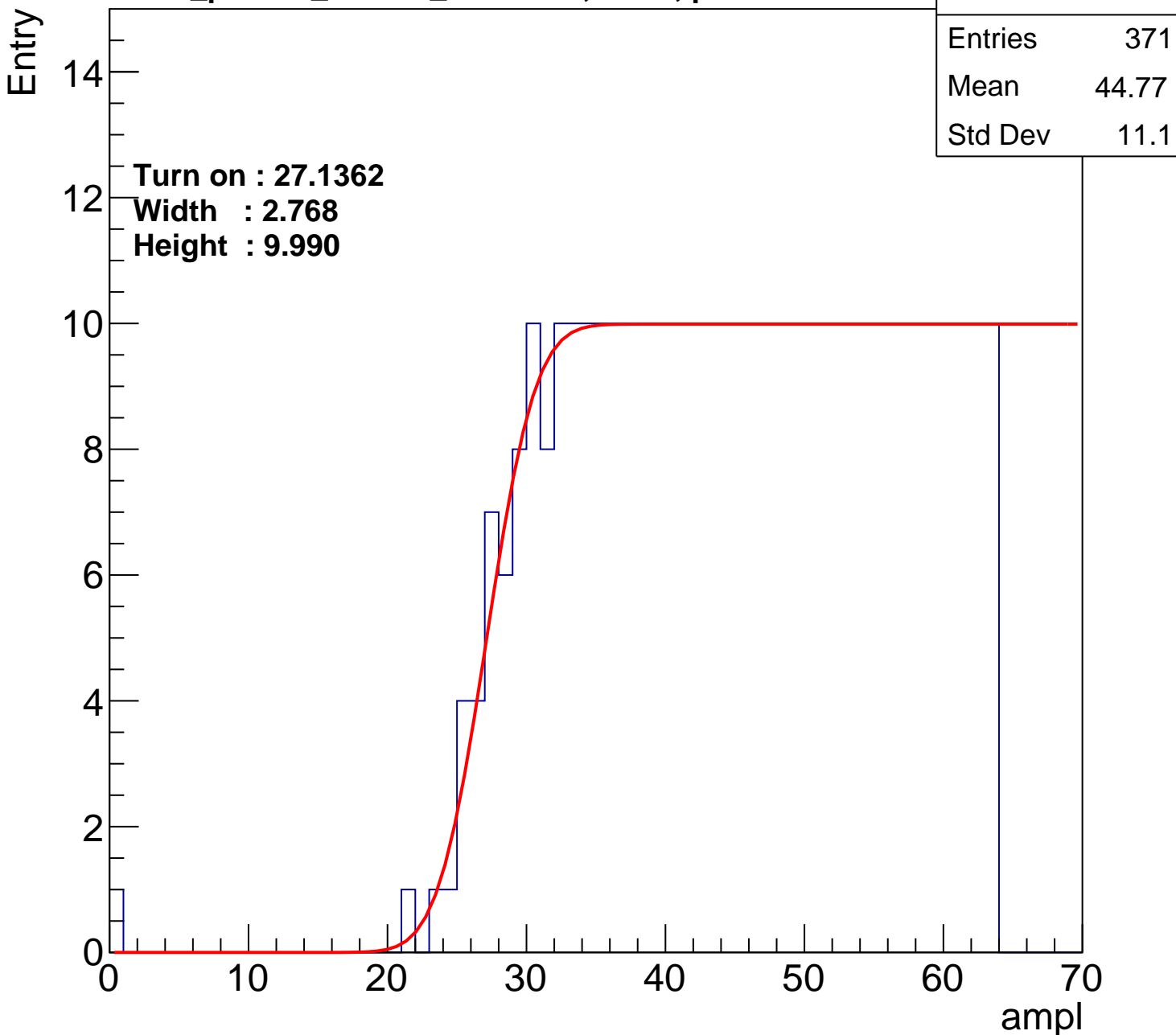
Mean	44.77
------	-------

Std Dev	11.1
---------	------

**Turn on : 27.1362**

**Width : 2.768**

**Height : 9.990**



# B0L000S, U1-ch28

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	365
Mean	44.91
Std Dev	11.37

**Turn on : 27.9192**

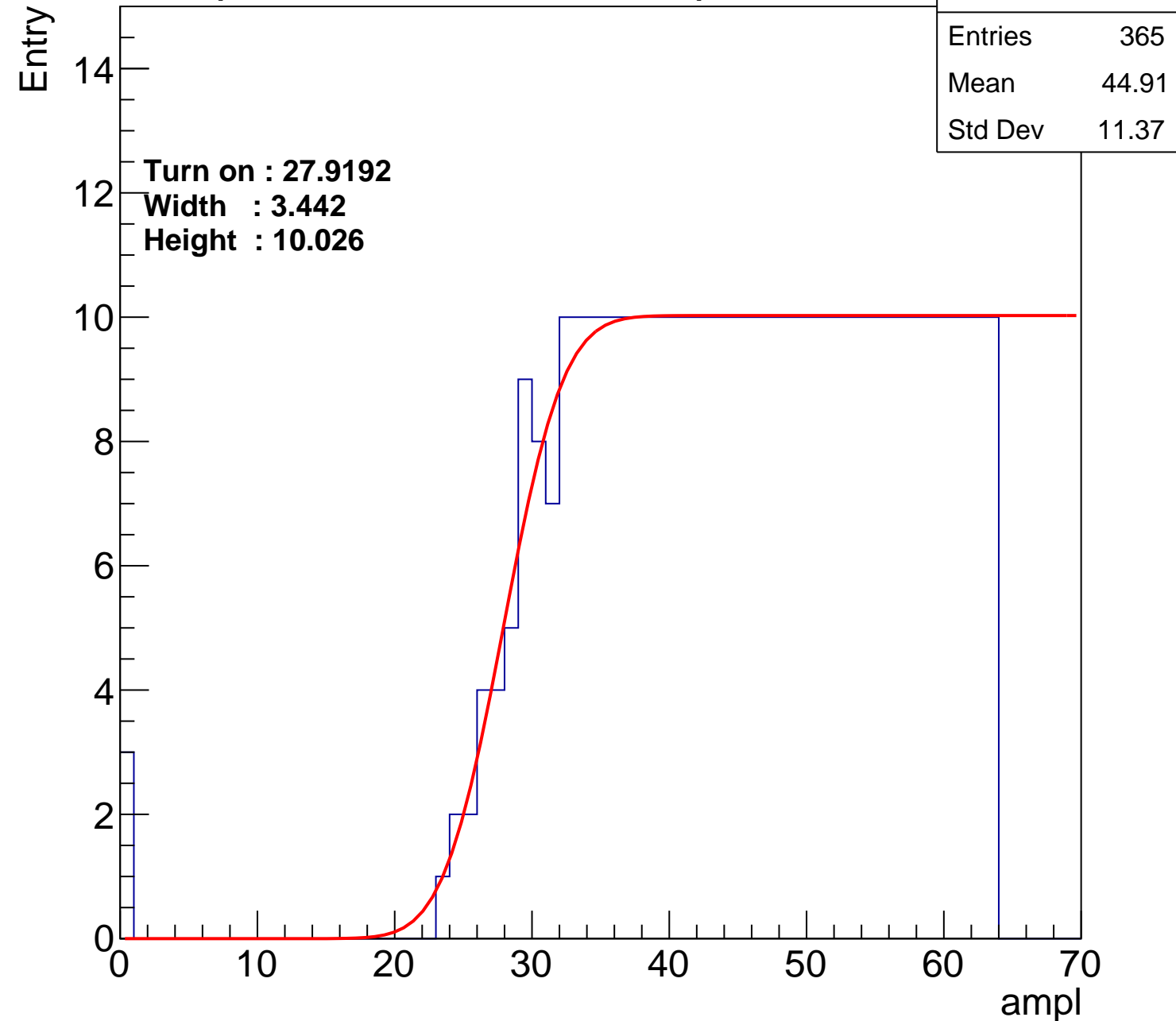
**Width : 3.442**

**Height : 10.026**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch29

calib\_packv5\_042523\_0143.root, FC#5, port B1

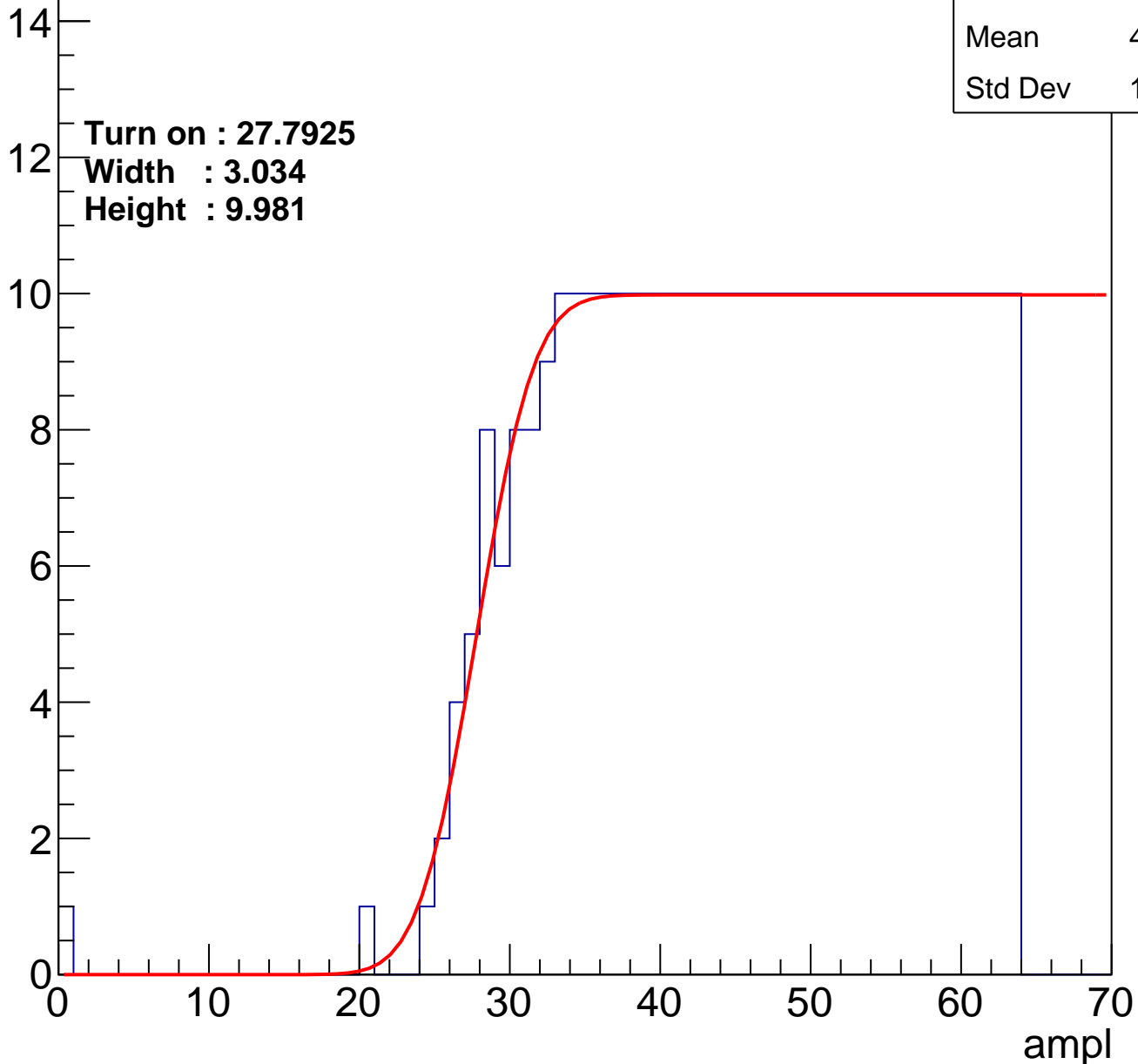
Entry

Entries	363
Mean	45.14
Std Dev	10.92

**Turn on : 27.7925**

**Width : 3.034**

**Height : 9.981**



# B0L000S, U1-ch30

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	366
Mean	44.79
Std Dev	11.59

Turn on : 28.4443

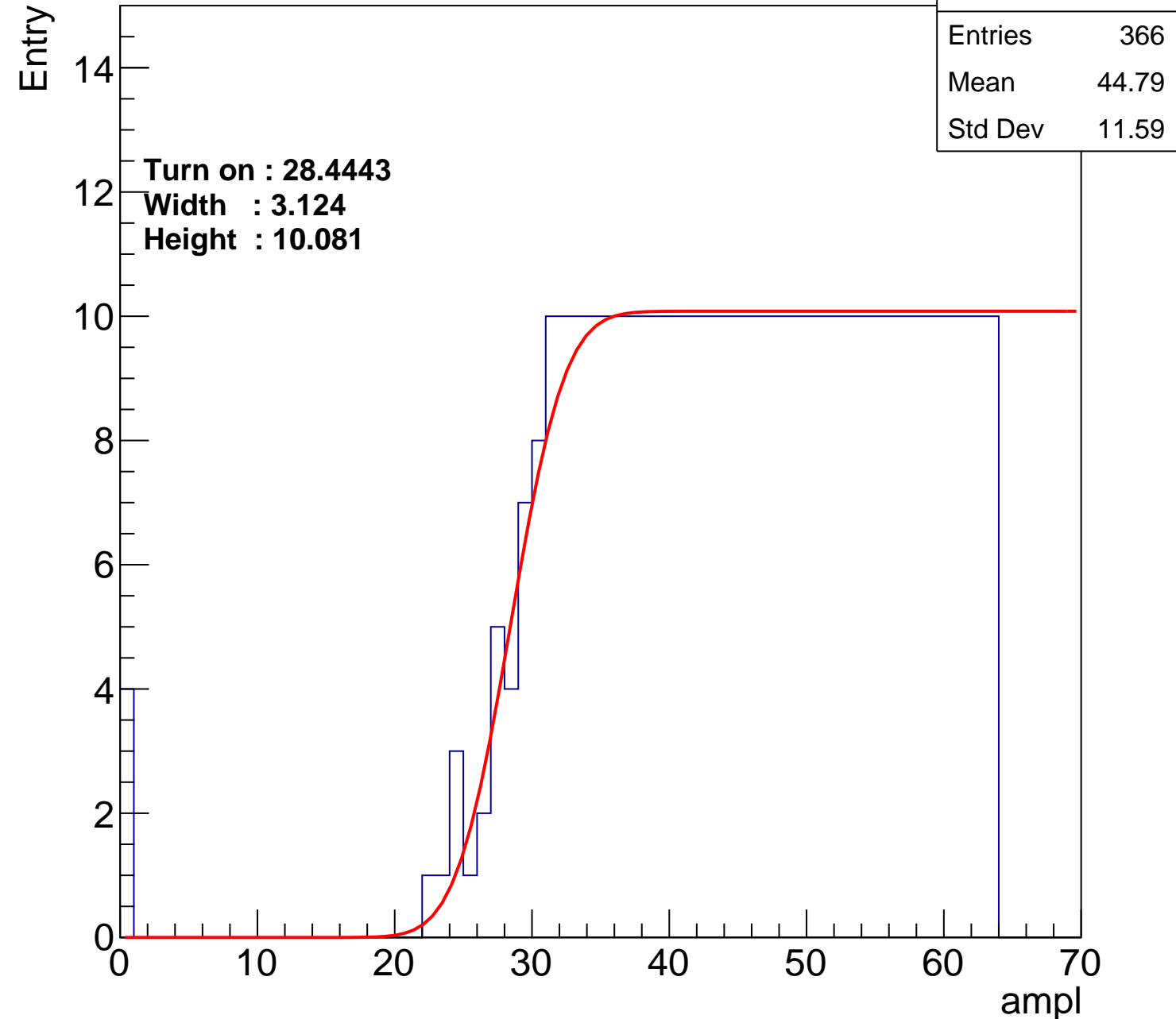
Width : 3.124

Height : 10.081

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L000S, U1-ch31

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	351
Mean	45.62
Std Dev	10.99

**Turn on : 29.1477**

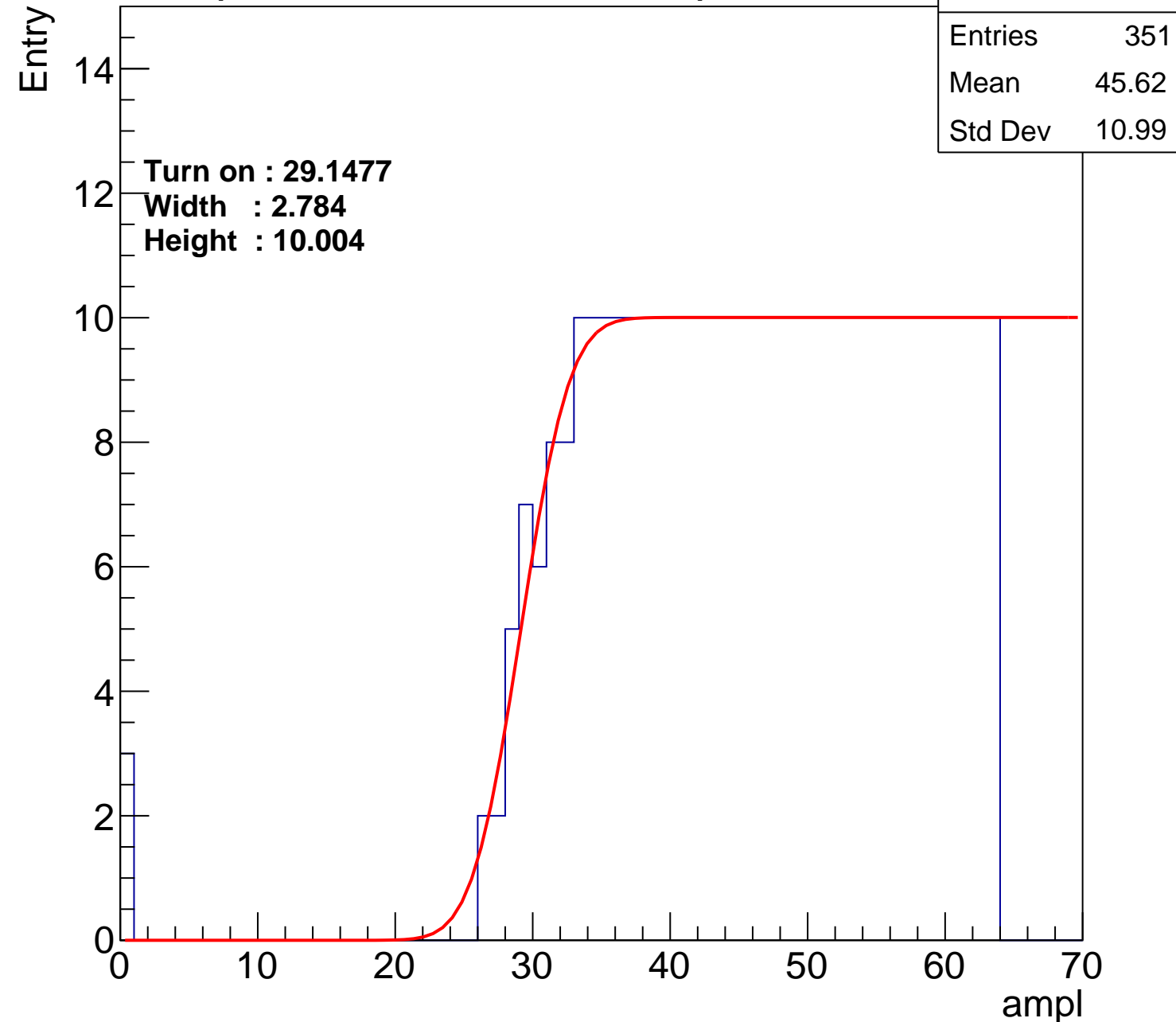
**Width : 2.784**

**Height : 10.004**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch32

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	394
Mean	43.57
Std Dev	11.89

Turn on : 25.1012

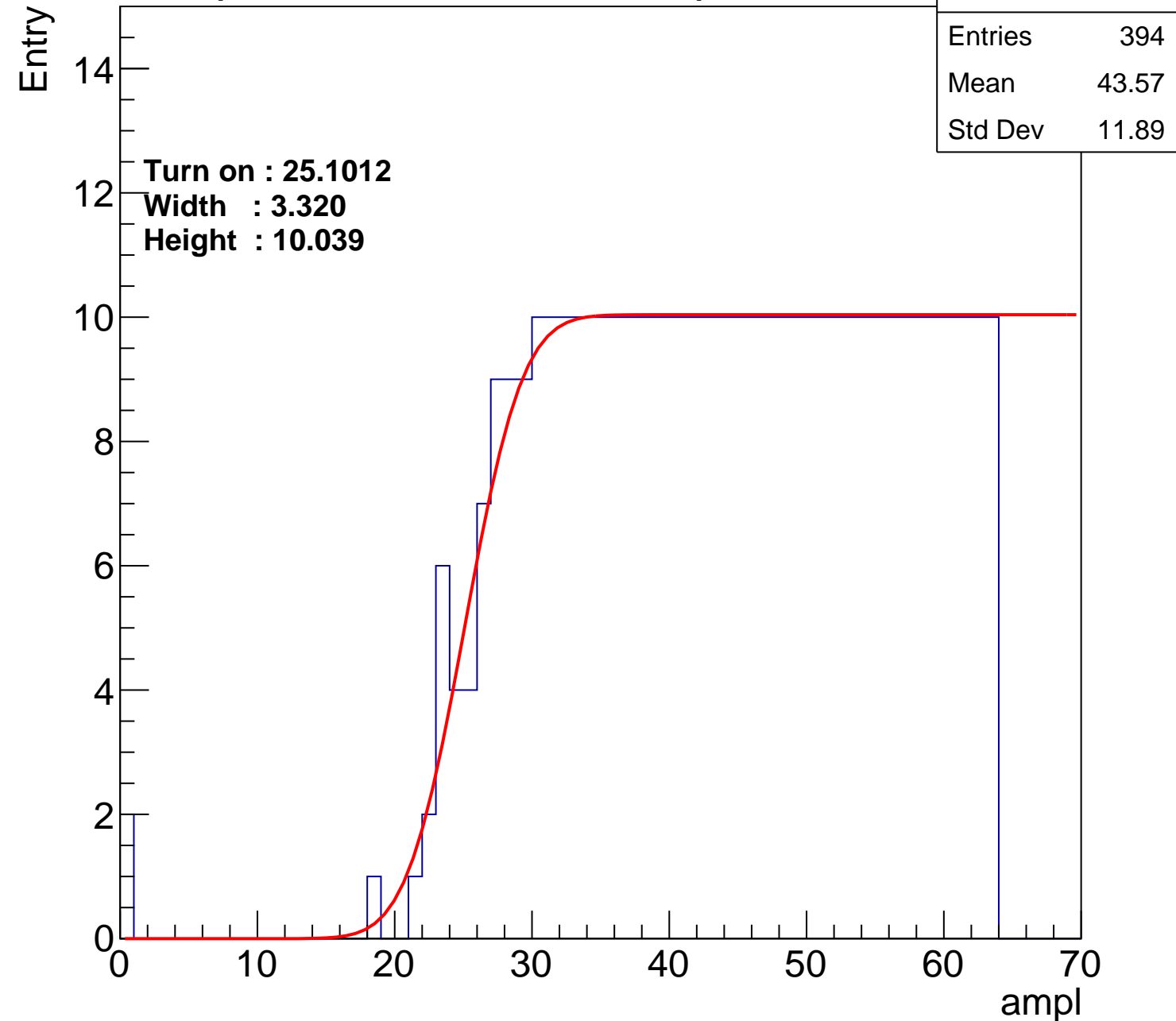
Width : 3.320

Height : 10.039

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch33

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	372
Mean	44.49
Std Dev	11.82

**Turn on : 27.2629**

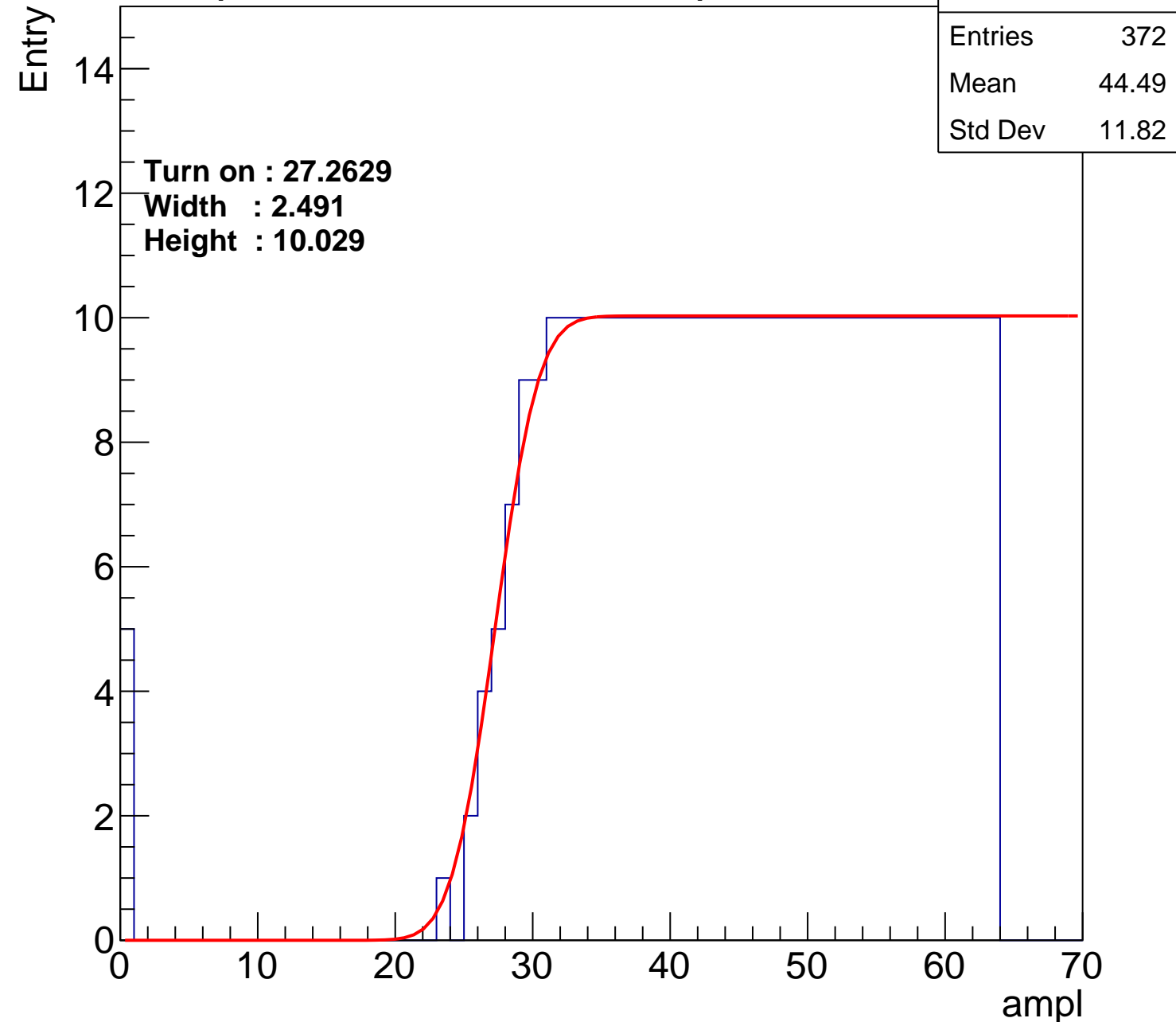
**Width : 2.491**

**Height : 10.029**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch34

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	365
Mean	44.83
Std Dev	11.58

**Turn on : 28.3768**

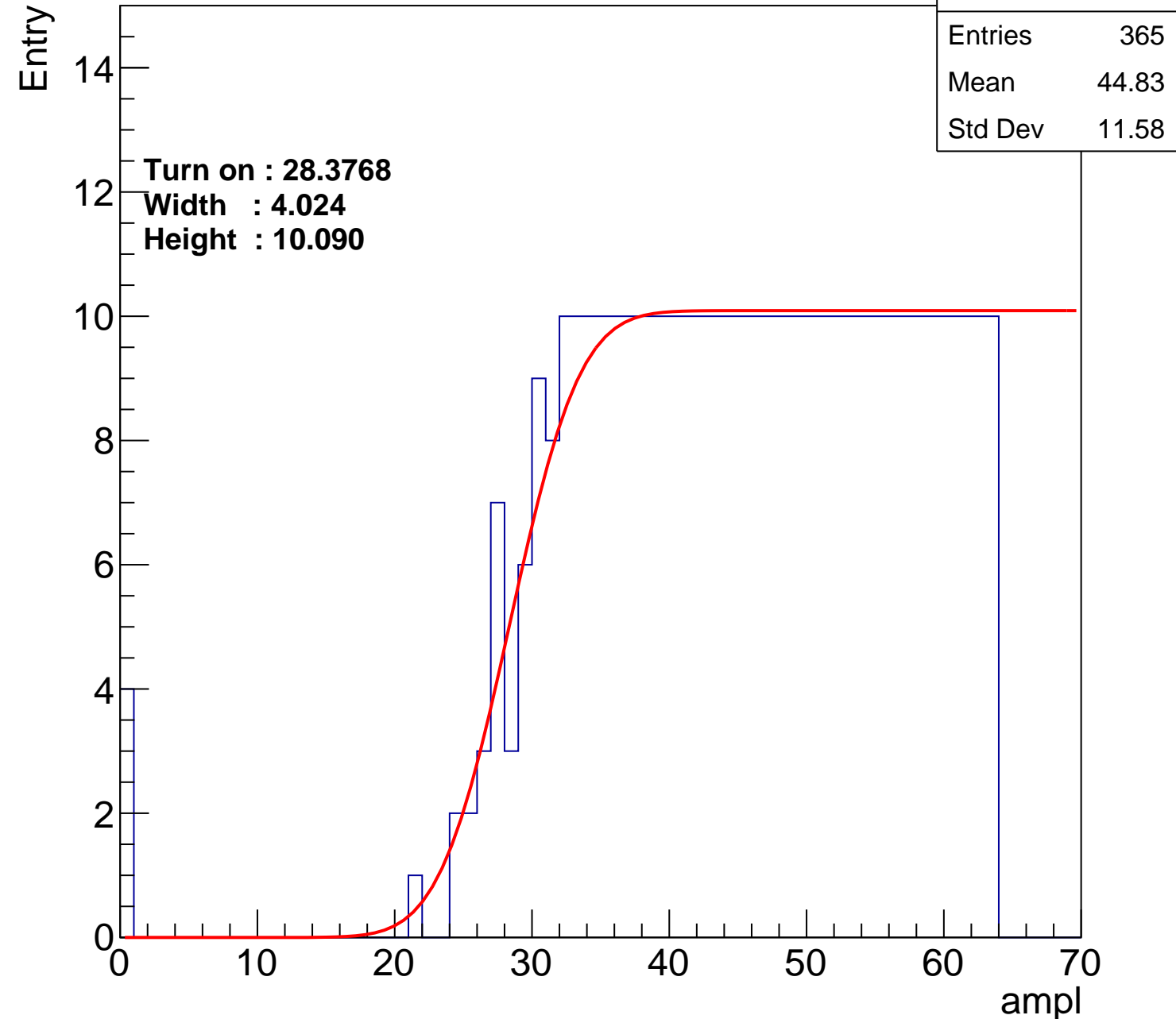
**Width : 4.024**

**Height : 10.090**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch35

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

18  
16  
14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 25.0000**  
**Width : 3.500**  
**Height : 0.000**

Entries	19
Mean	0
Std Dev	0

ampl

# B0L000S, U1-ch36

calib\_packv5\_042523\_0143.root, FC#5, port B1

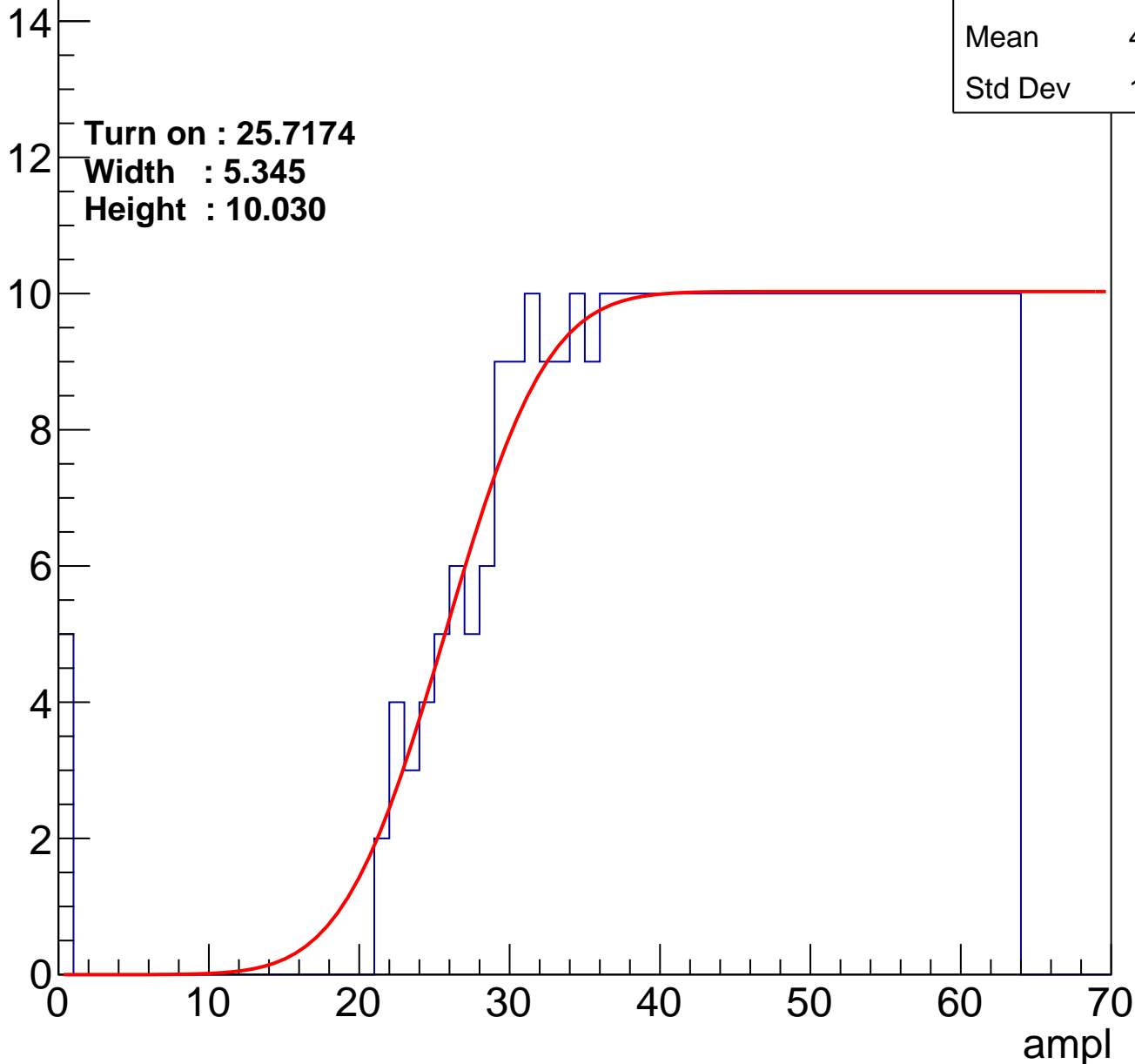
Entry

Entries	385
Mean	43.69
Std Dev	12.34

Turn on : 25.7174

Width : 5.345

Height : 10.030



# B0L000S, U1-ch37

calib\_packv5\_042523\_0143.root, FC#5, port B1

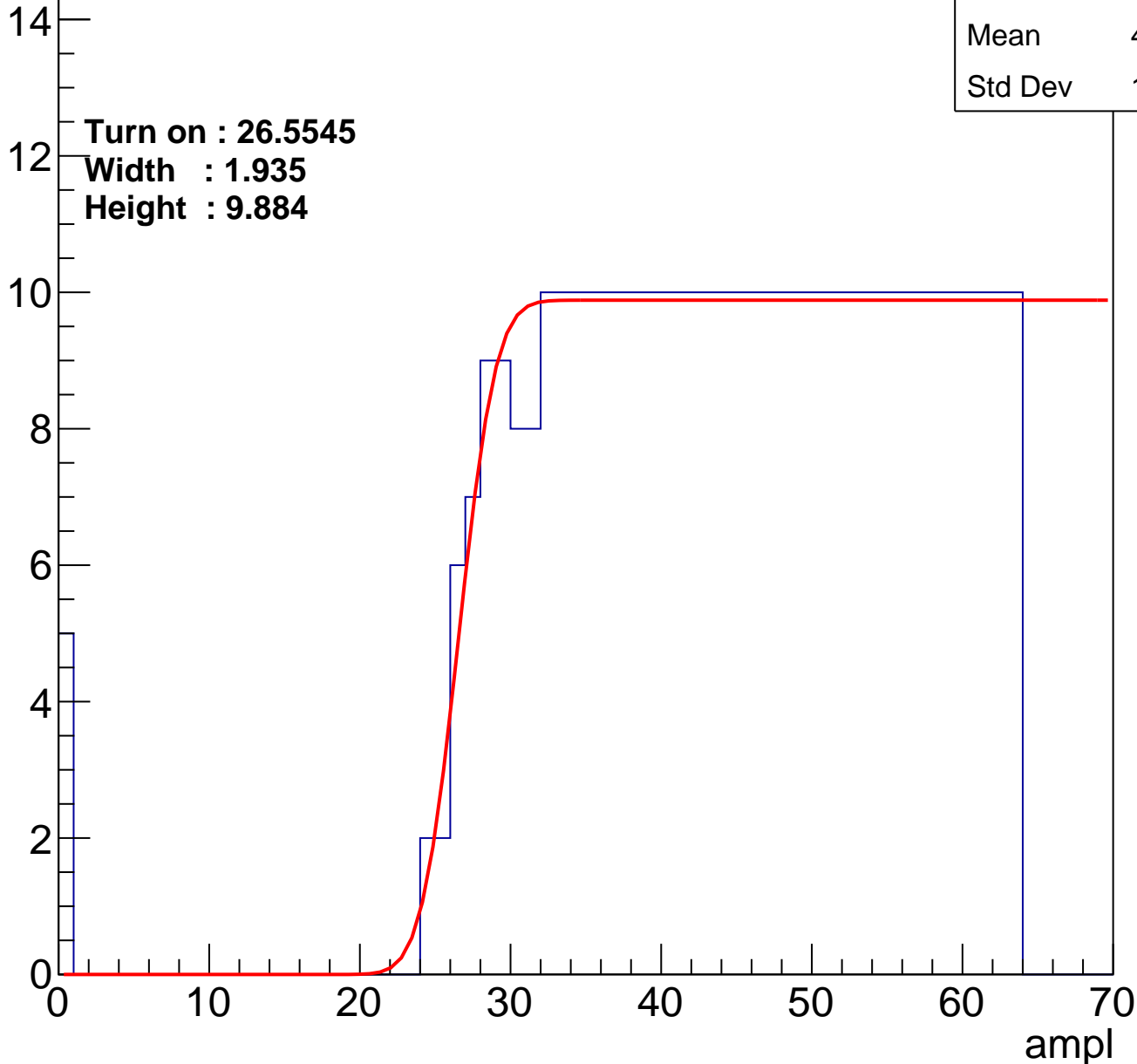
Entry

Entries	376
Mean	44.27
Std Dev	11.94

Turn on : 26.5545

Width : 1.935

Height : 9.884



# B0L000S, U1-ch38

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	380
Mean	44.36
Std Dev	11.28

Turn on : 26.2493

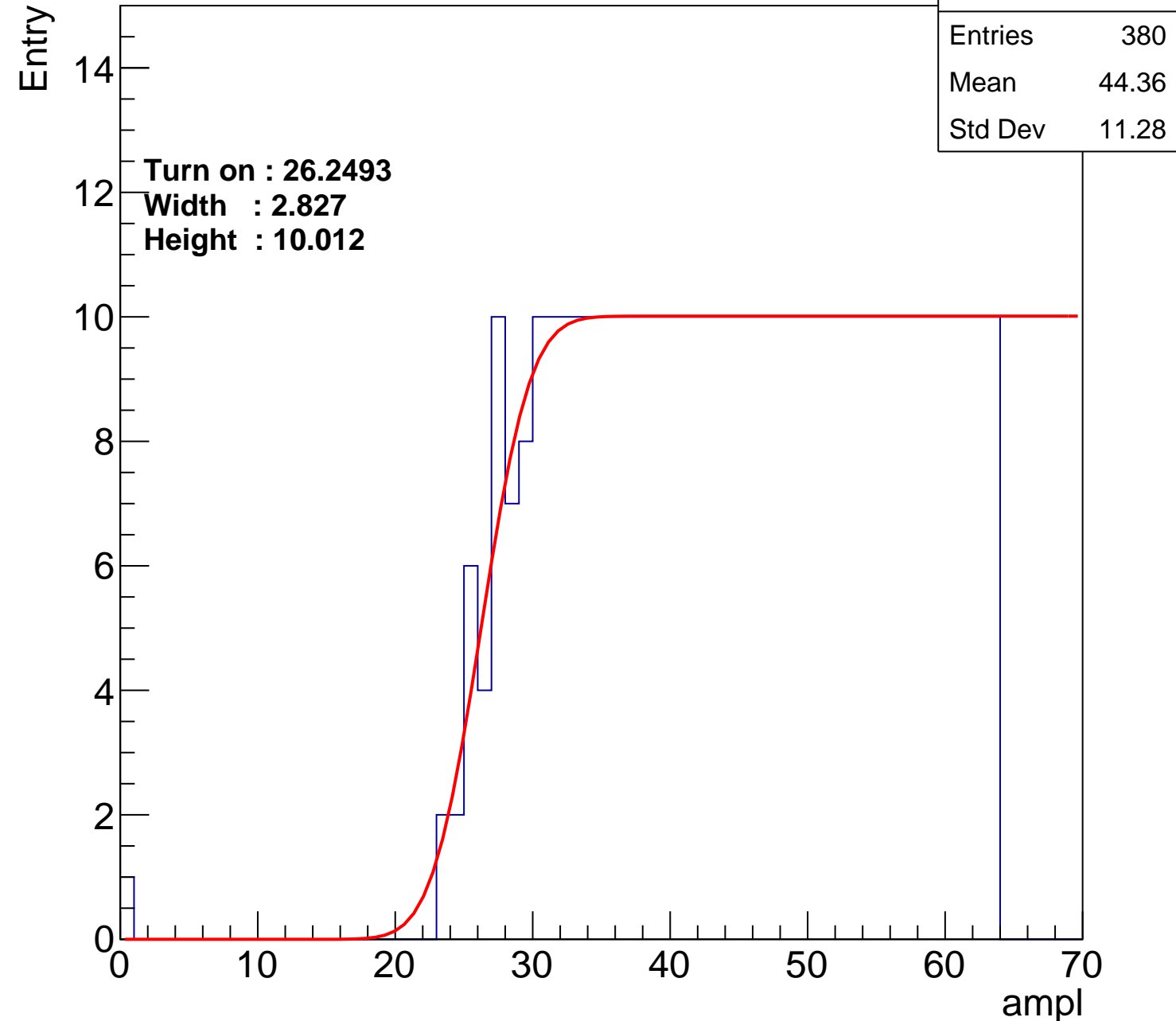
Width : 2.827

Height : 10.012

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L000S, U1-ch39

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	373
Mean	44.48
Std Dev	11.7

**Turn on : 26.9407**

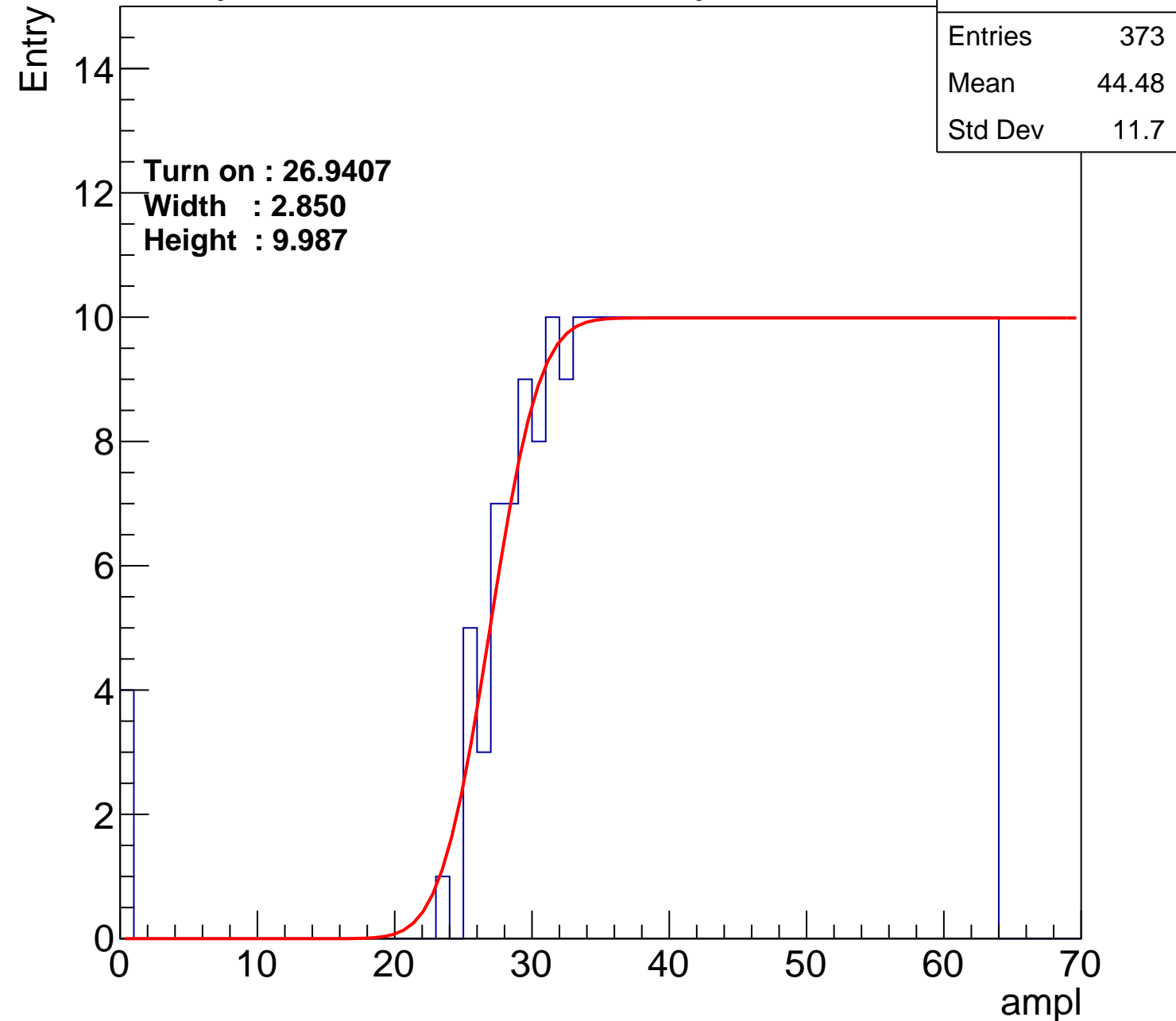
**Width : 2.850**

**Height : 9.987**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch40

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	360
Mean	45.23
Std Dev	11.04

**Turn on : 28.7276**

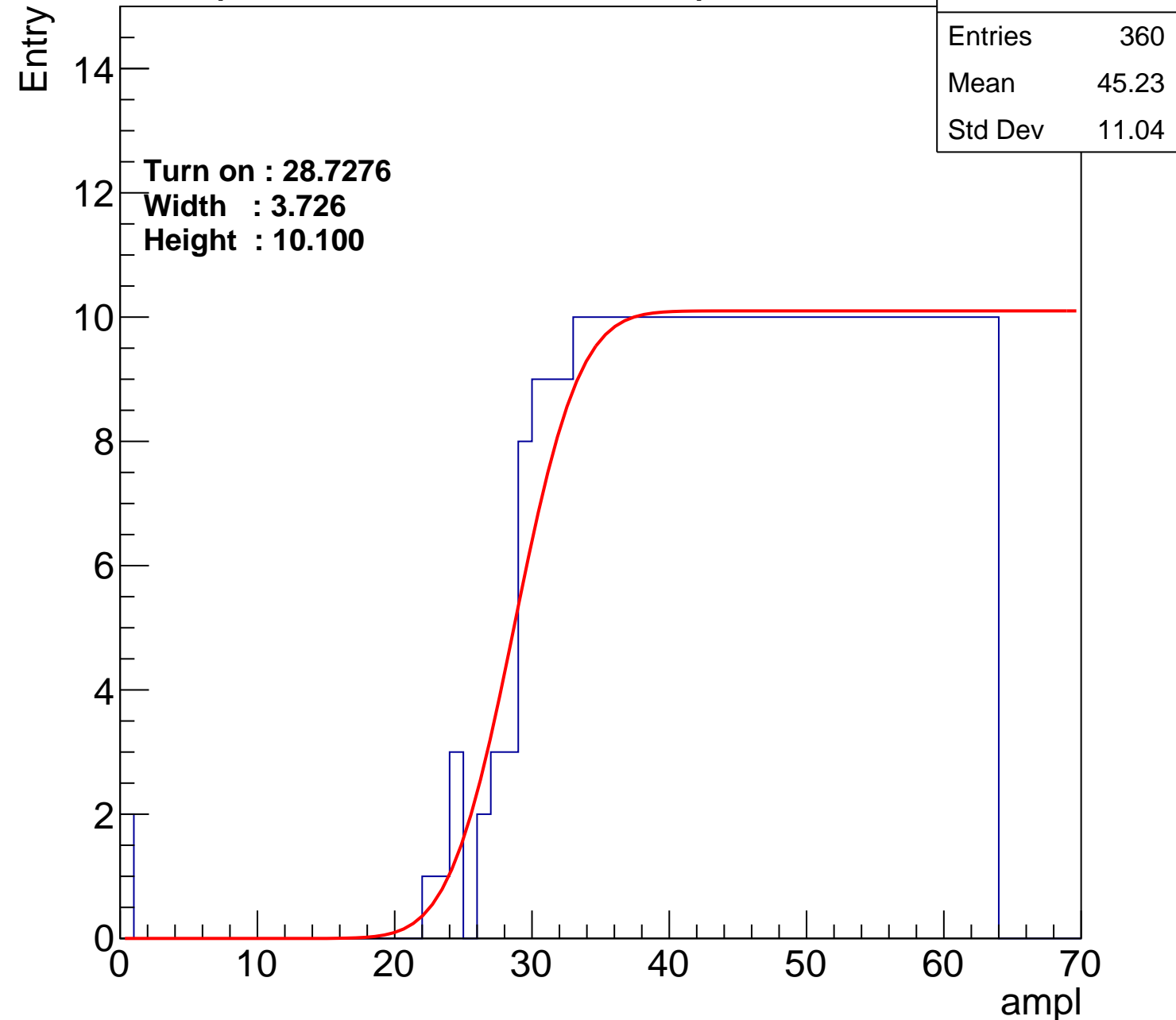
**Width : 3.726**

**Height : 10.100**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch41

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	364
Mean	45.07
Std Dev	10.99

**Turn on : 28.3222**

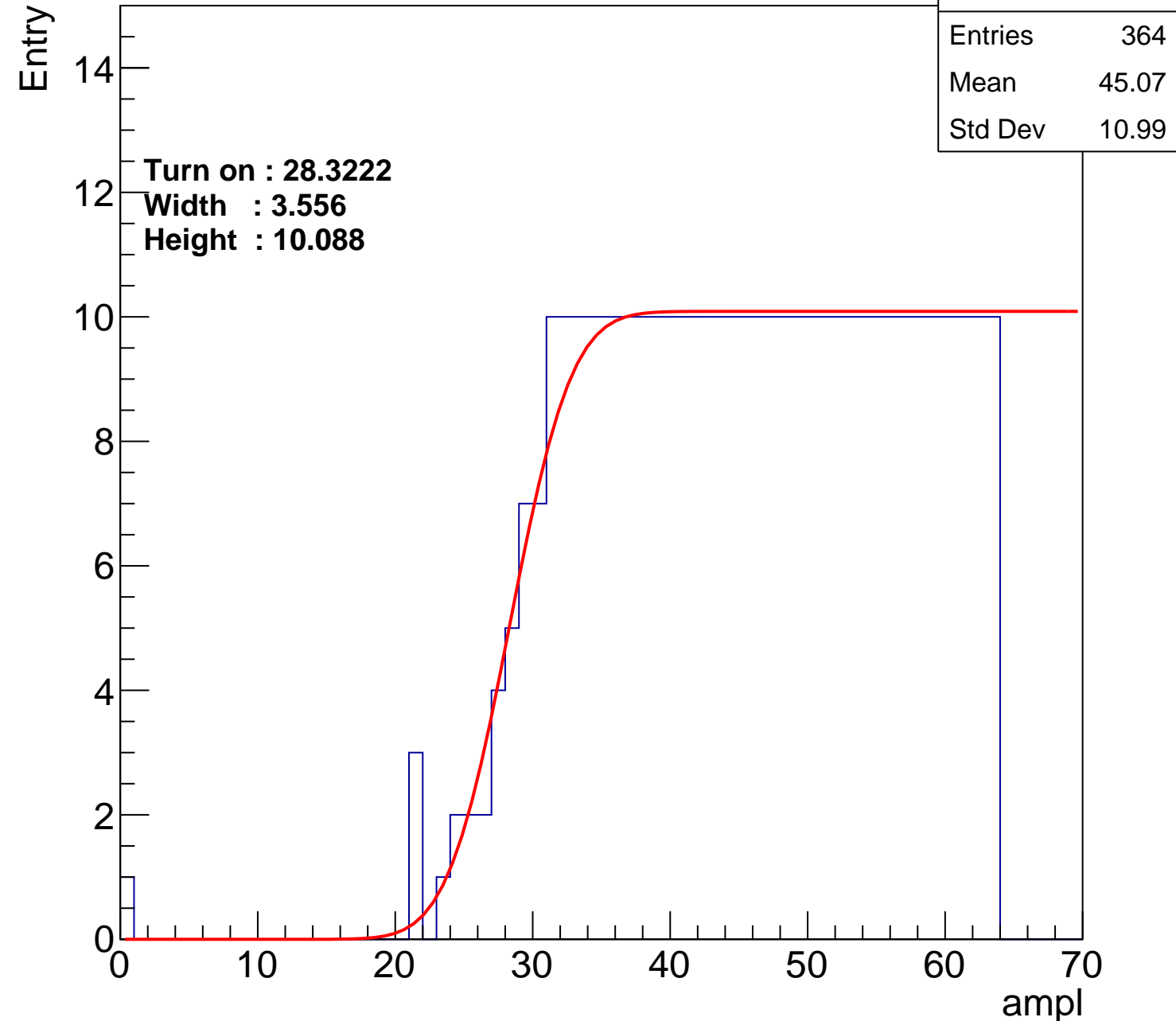
**Width : 3.556**

**Height : 10.088**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch42

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	392
Mean	43.59
Std Dev	12.08

**Turn on : 24.9269**

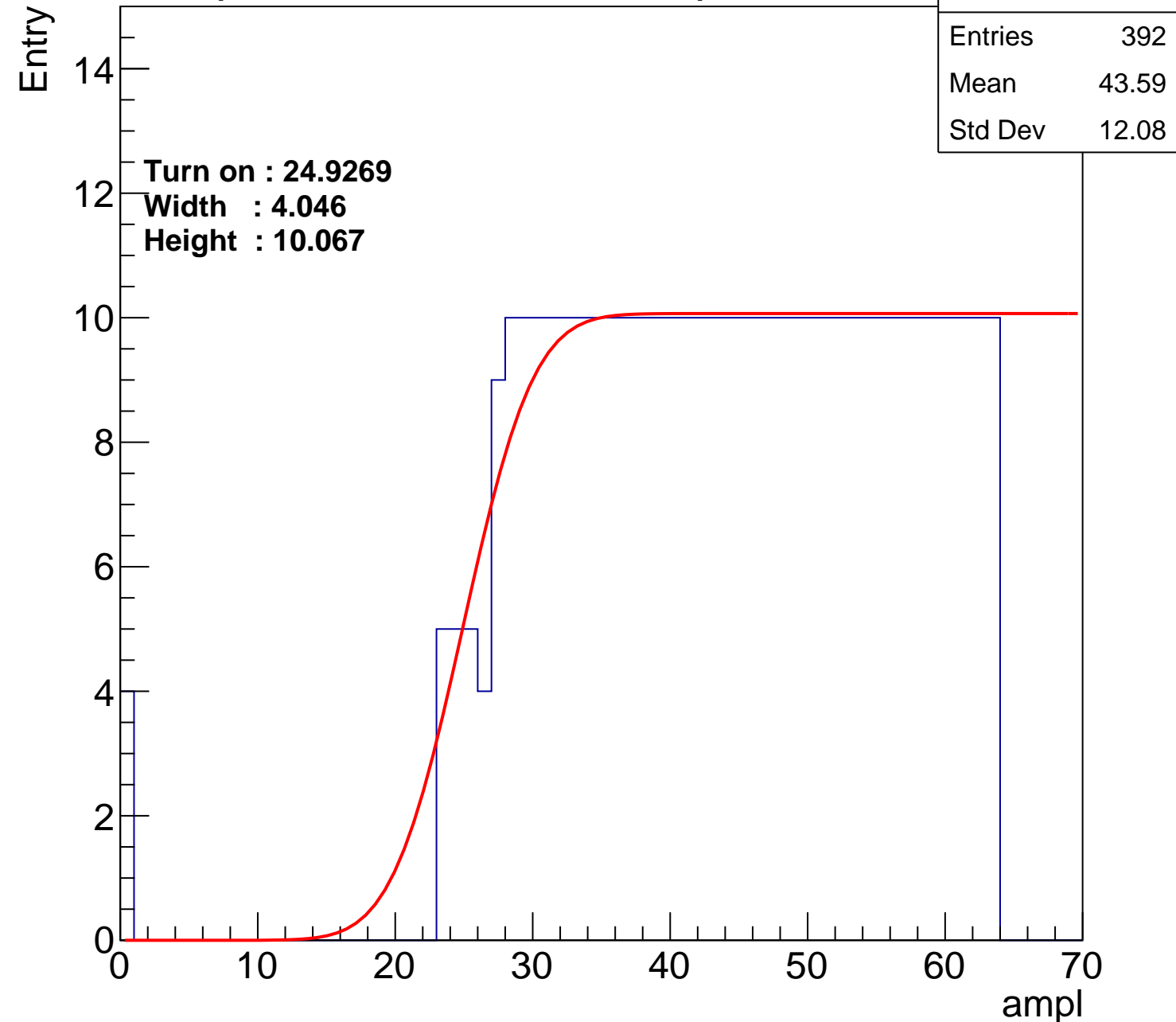
**Width : 4.046**

**Height : 10.067**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch43

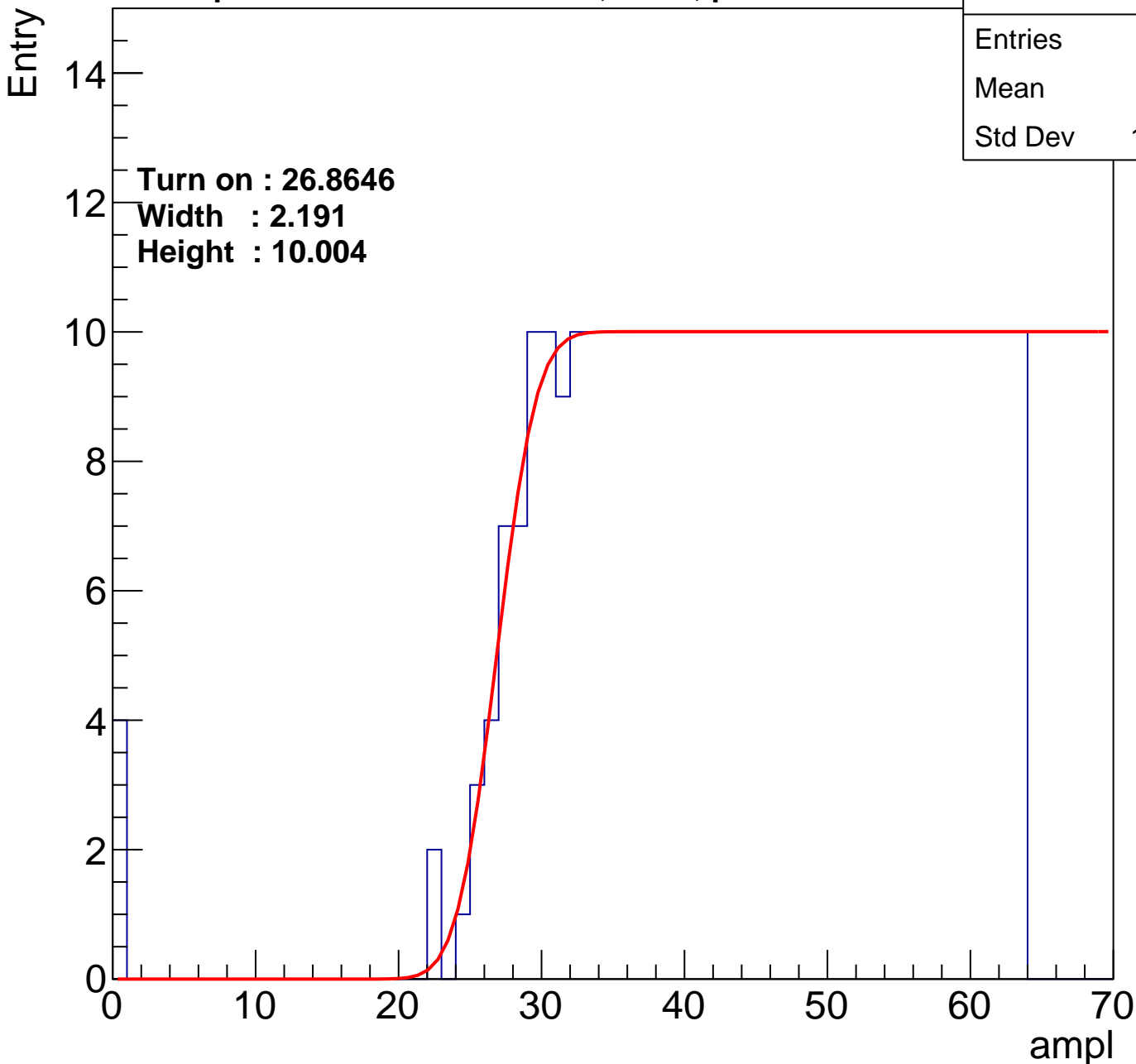
calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	377
Mean	44.3
Std Dev	11.77

Turn on : 26.8646

Width : 2.191

Height : 10.004



# B0L000S, U1-ch44

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	374
Mean	44.38
Std Dev	11.87

Turn on : 27.1815

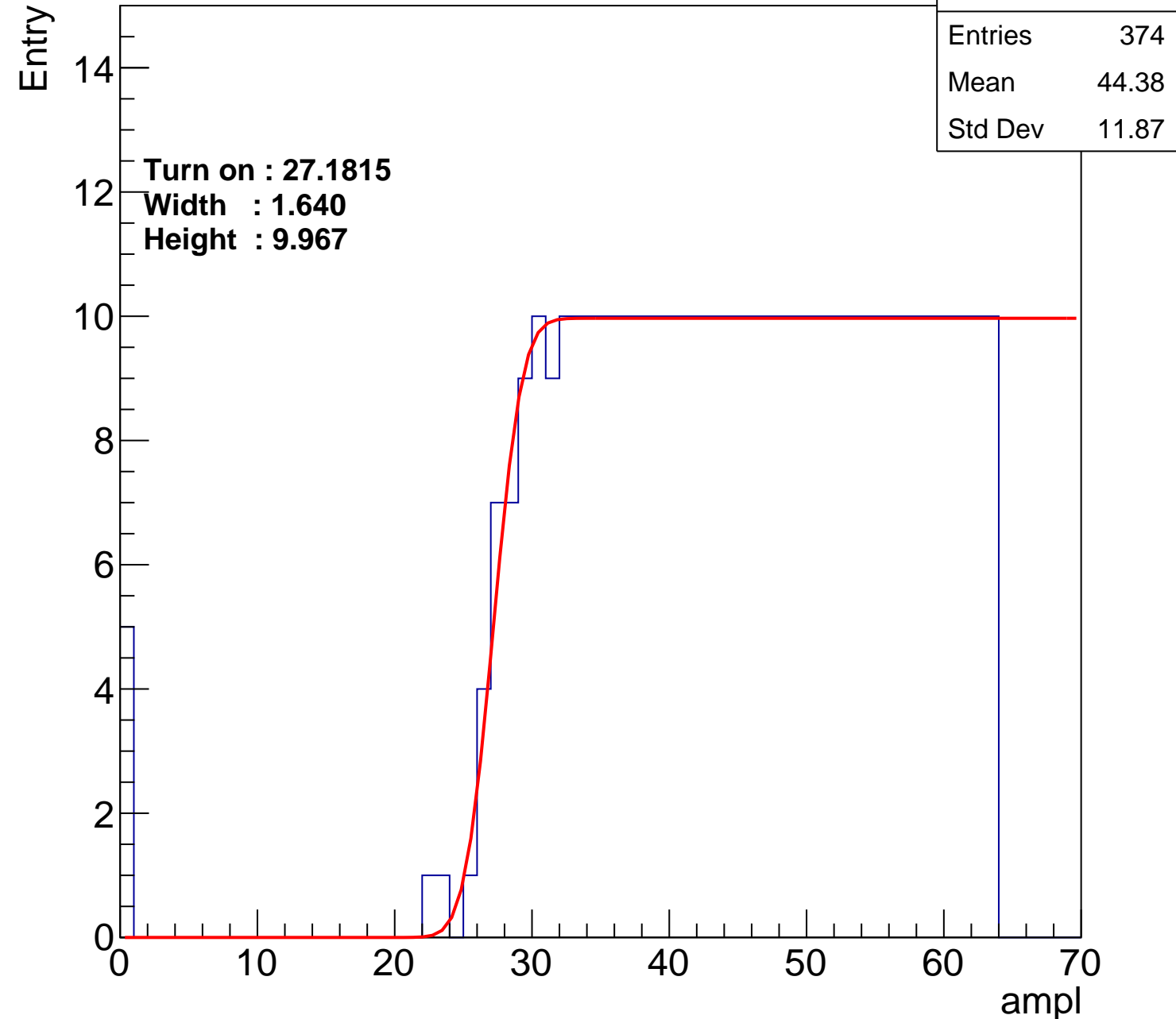
Width : 1.640

Height : 9.967

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch45

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	375
Mean	44.4
Std Dev	11.72

**Turn on : 26.8487**

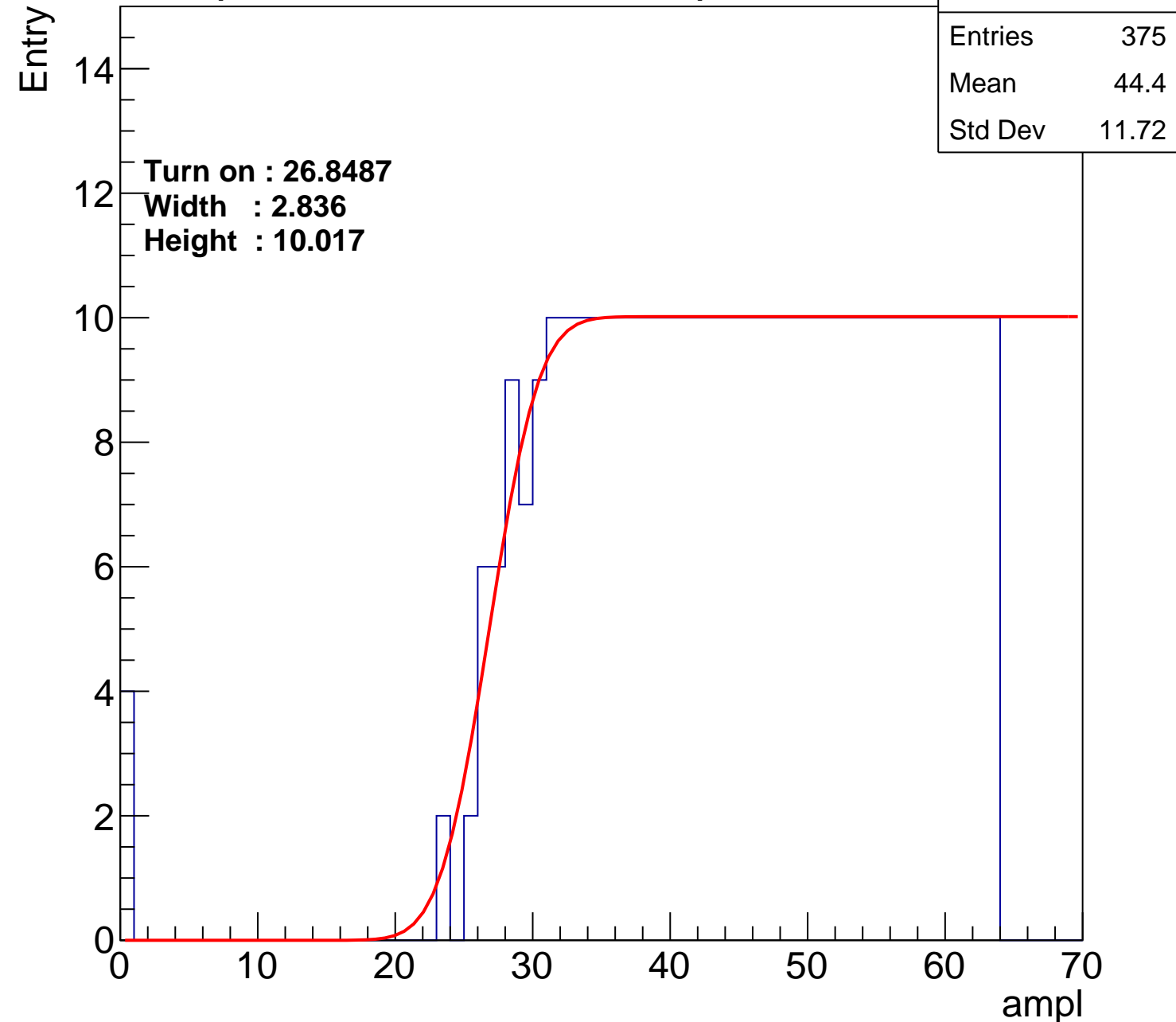
**Width : 2.836**

**Height : 10.017**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch46

calib\_packv5\_042523\_0143.root, FC#5, port B1

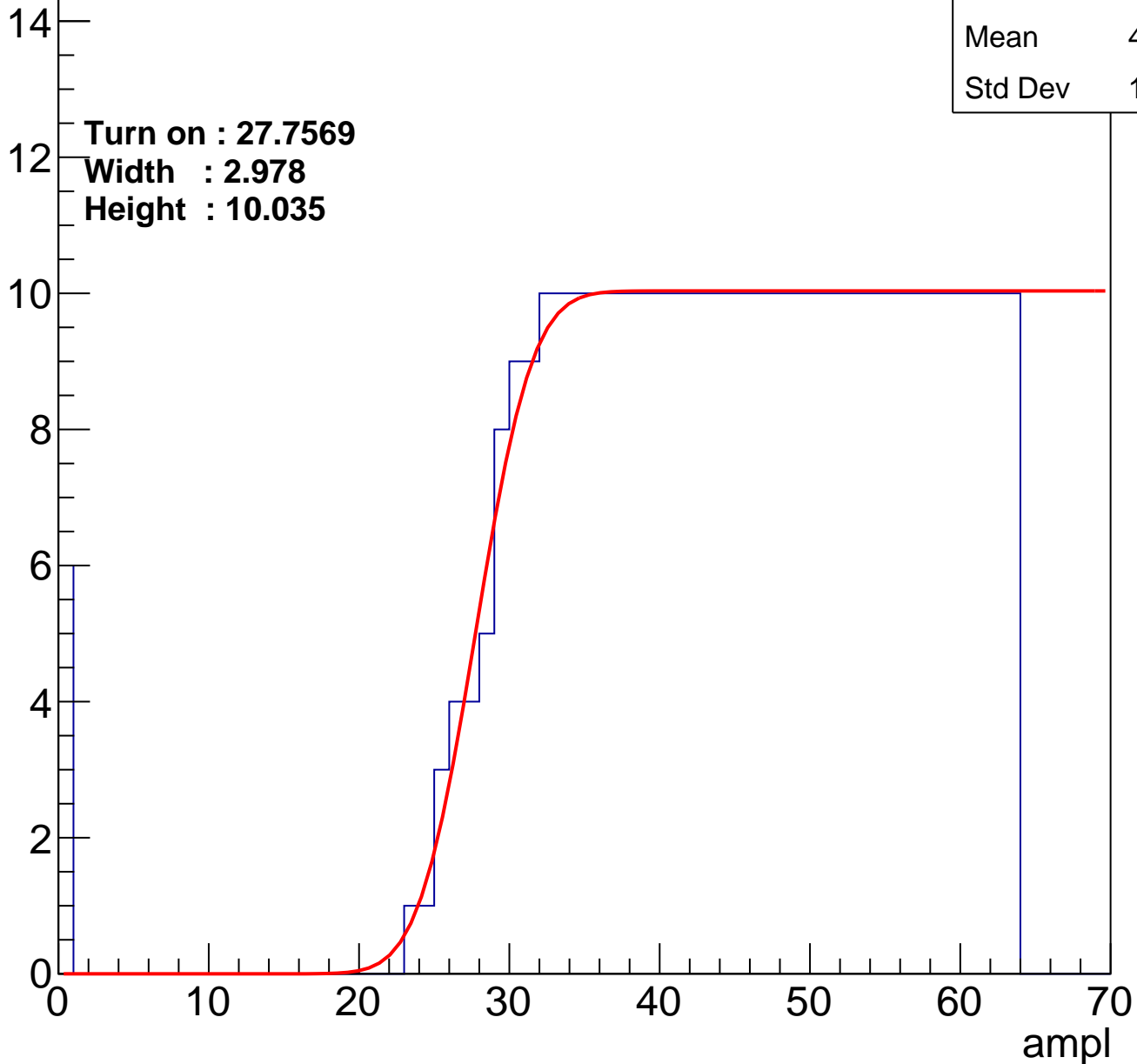
Entries	370
Mean	44.47
Std Dev	12.02

**Turn on : 27.7569**

**Width : 2.978**

**Height : 10.035**

Entry





# B0L000S, U1-ch47

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	382
Mean	44
Std Dev	11.96

**Turn on : 26.3538**

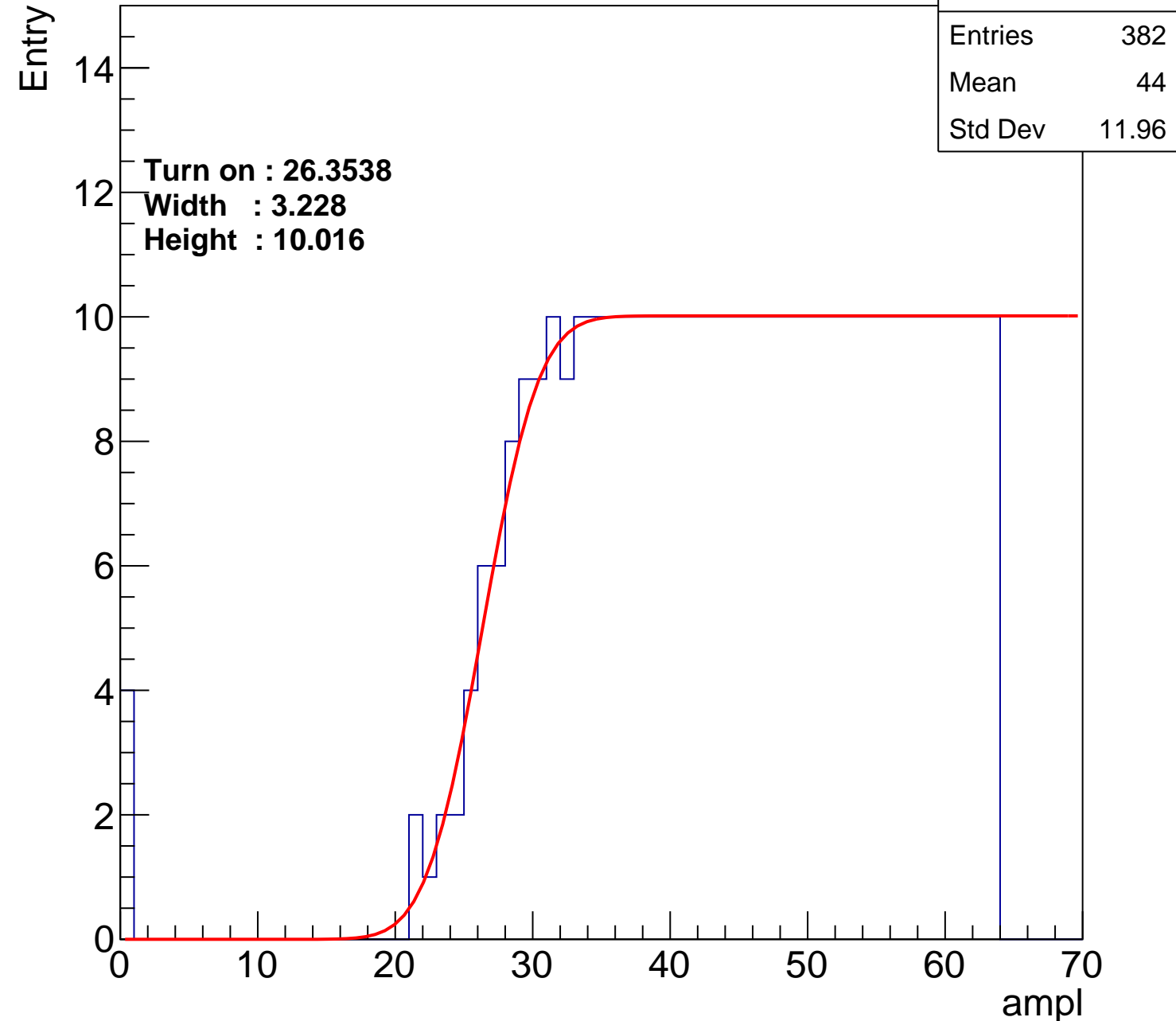
**Width : 3.228**

**Height : 10.016**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch48

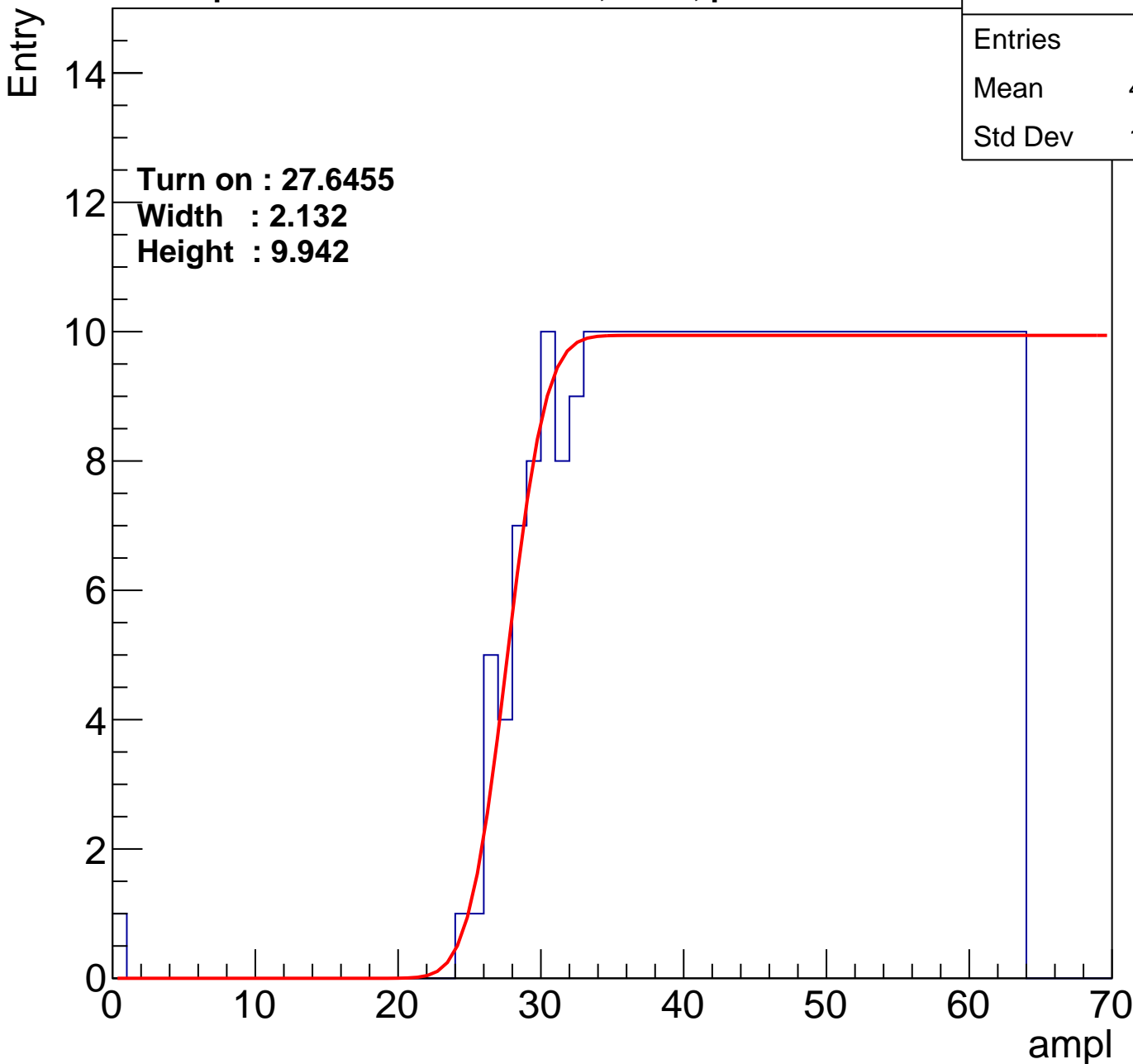
**calib\_packv5\_042523\_0143.root, FC#5, port B1**

Entries	364
Mean	45.14
Std Dev	10.86

**Turn on : 27.6455**

**Width : 2.132**

**Height : 9.942**



# B0L000S, U1-ch49

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	363
Mean	45.19
Std Dev	10.84

**Turn on : 28.2390**

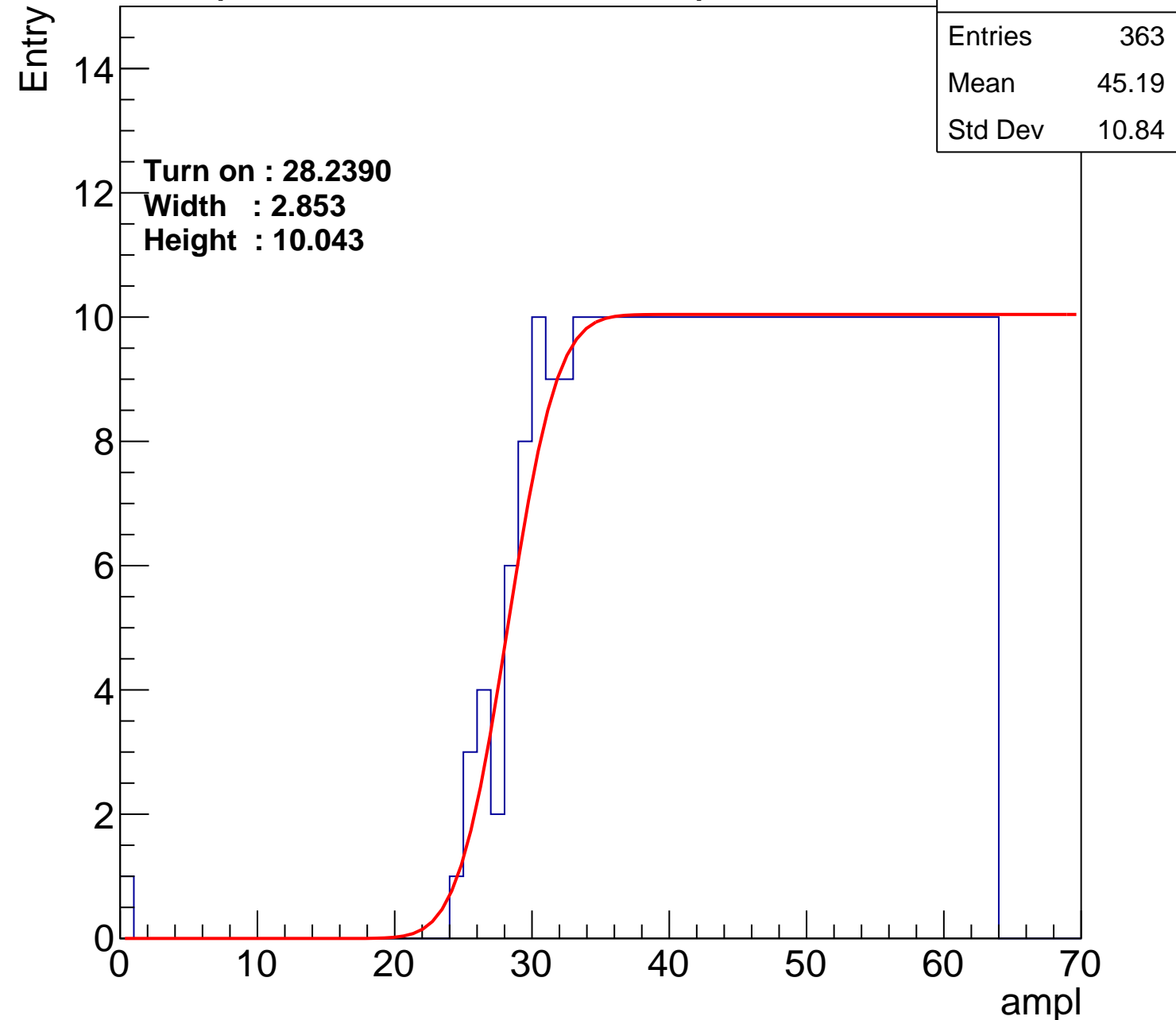
**Width : 2.853**

**Height : 10.043**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch50

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	359
Mean	45.17
Std Dev	11.27

**Turn on : 29.4545**

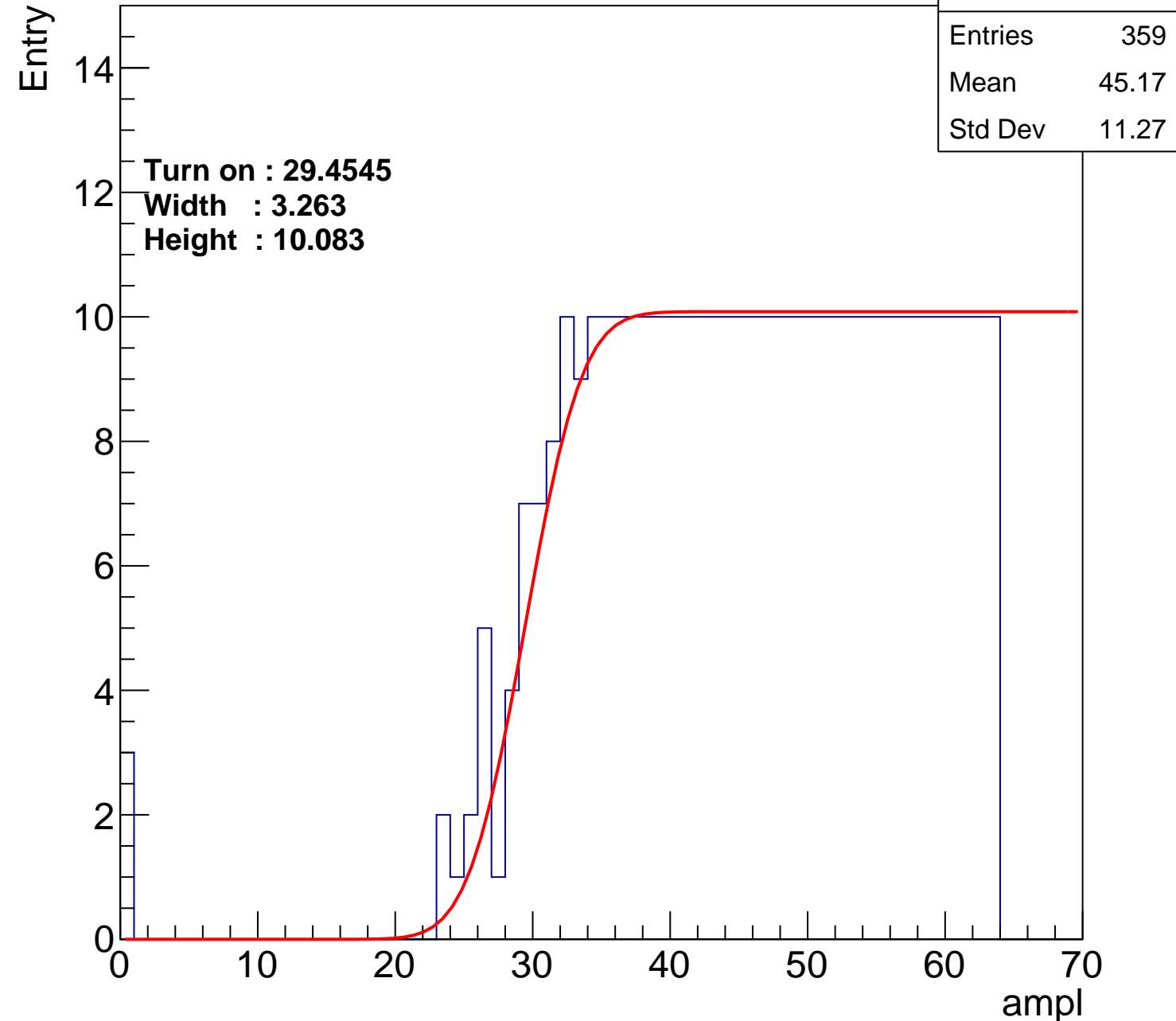
**Width : 3.263**

**Height : 10.083**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch51

calib\_packv5\_042523\_0143.root, FC#5, port B1

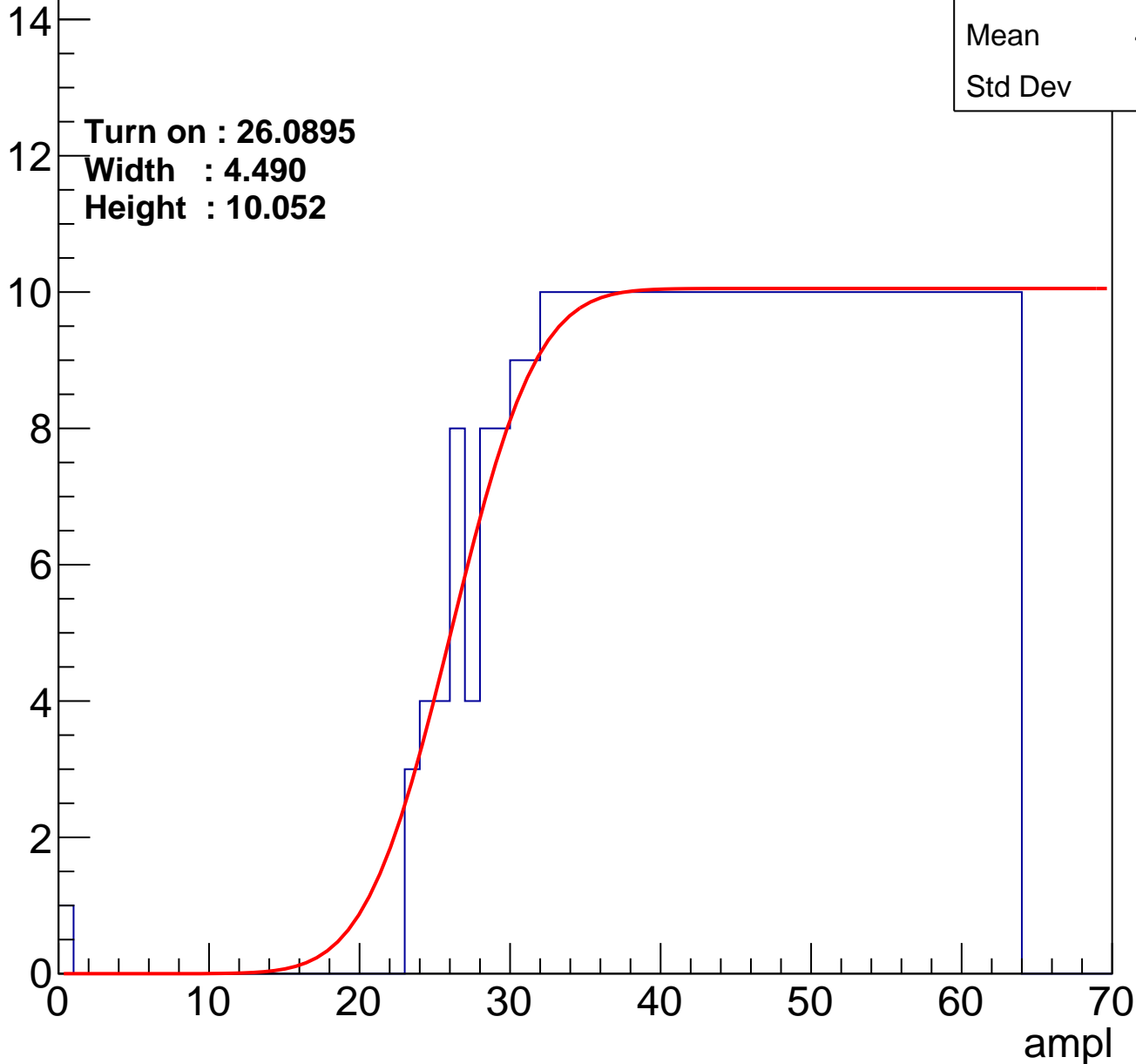
Entries	378
Mean	44.41
Std Dev	11.31

**Turn on : 26.0895**

**Width : 4.490**

**Height : 10.052**

Entry



# B0L000S, U1-ch52

calib\_packv5\_042523\_0143.root, FC#5, port B1

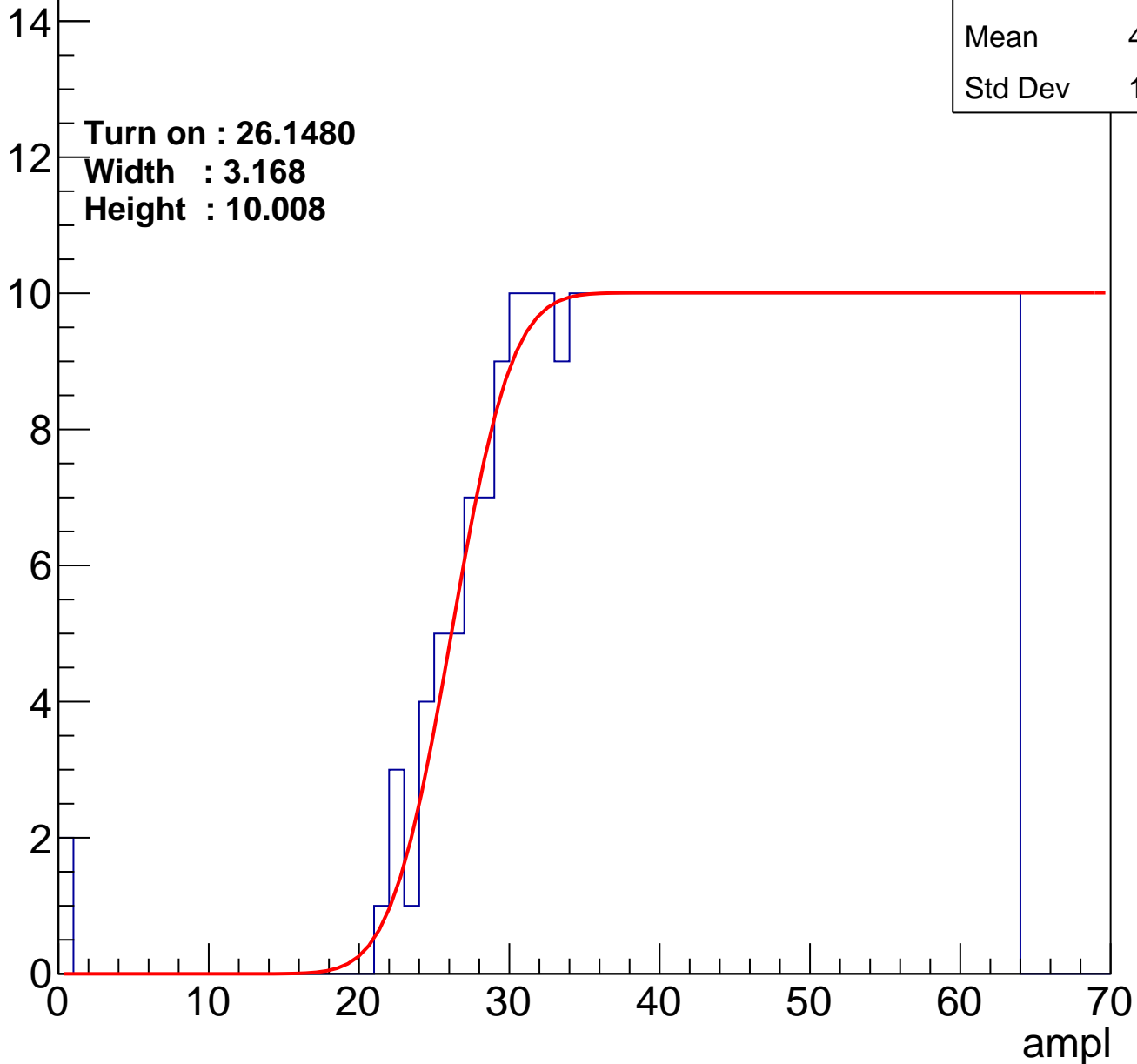
Entry

Entries	383
Mean	44.08
Std Dev	11.64

Turn on : 26.1480

Width : 3.168

Height : 10.008



# B0L000S, U1-ch53

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	386
Mean	44.05
Std Dev	11.46

**Turn on : 25.7830**

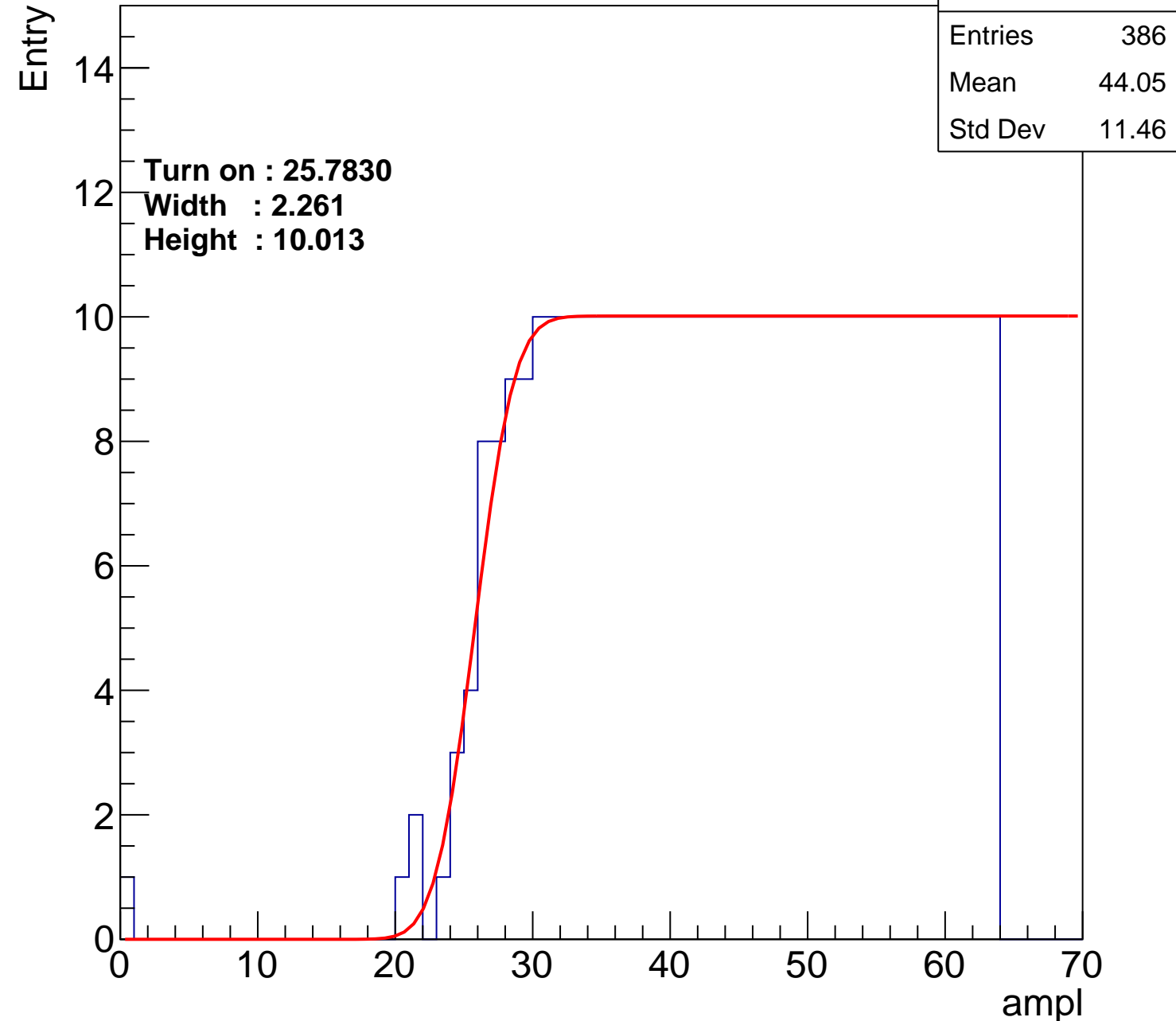
**Width : 2.261**

**Height : 10.013**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch54

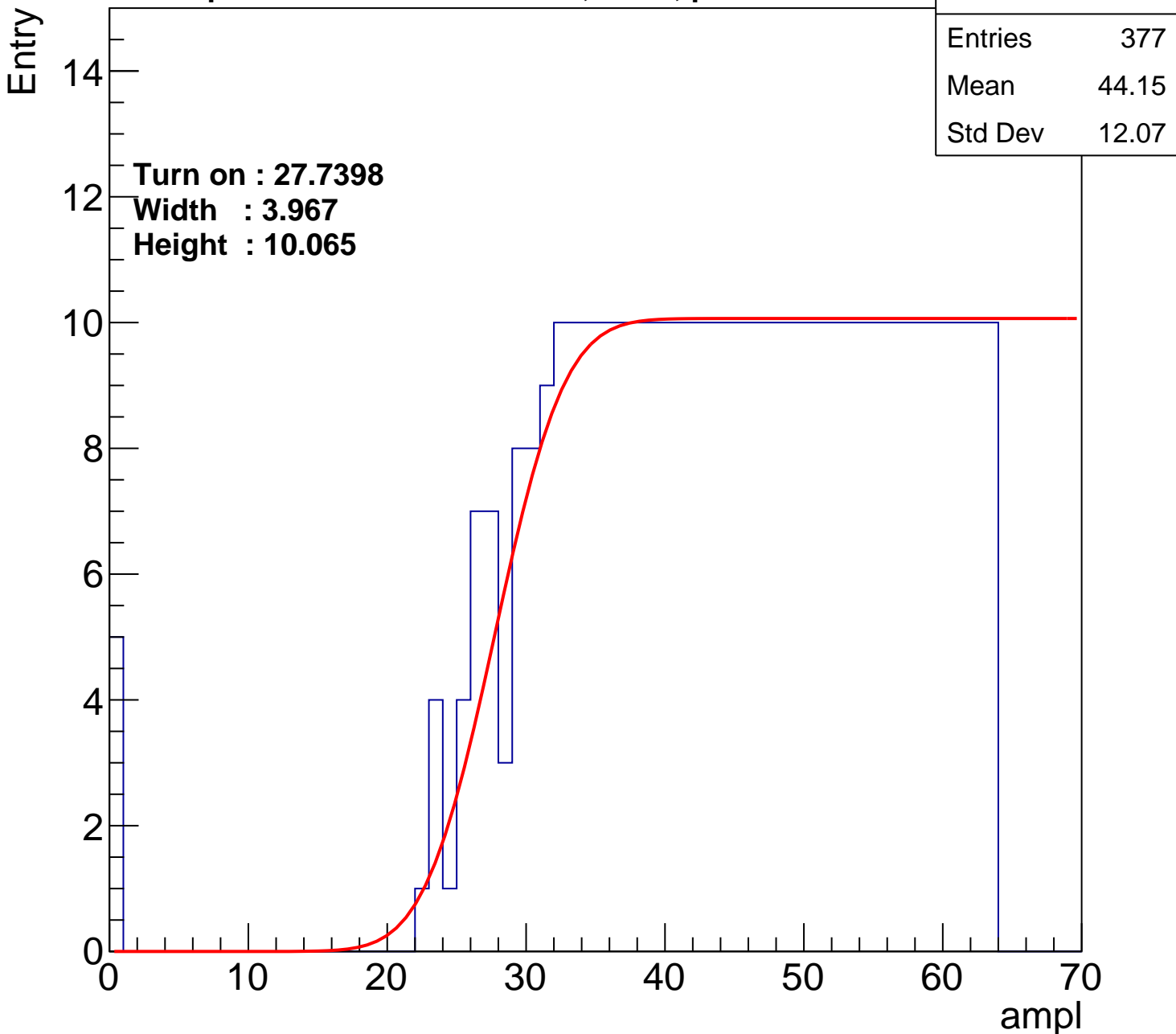
**calib\_packv5\_042523\_0143.root, FC#5, port B1**

Entries	377
Mean	44.15
Std Dev	12.07

**Turn on : 27.7398**

**Width : 3.967**

**Height : 10.065**





# B0L000S, U1-ch55

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	379
Mean	44.11
Std Dev	11.94

**Turn on : 26.5660**

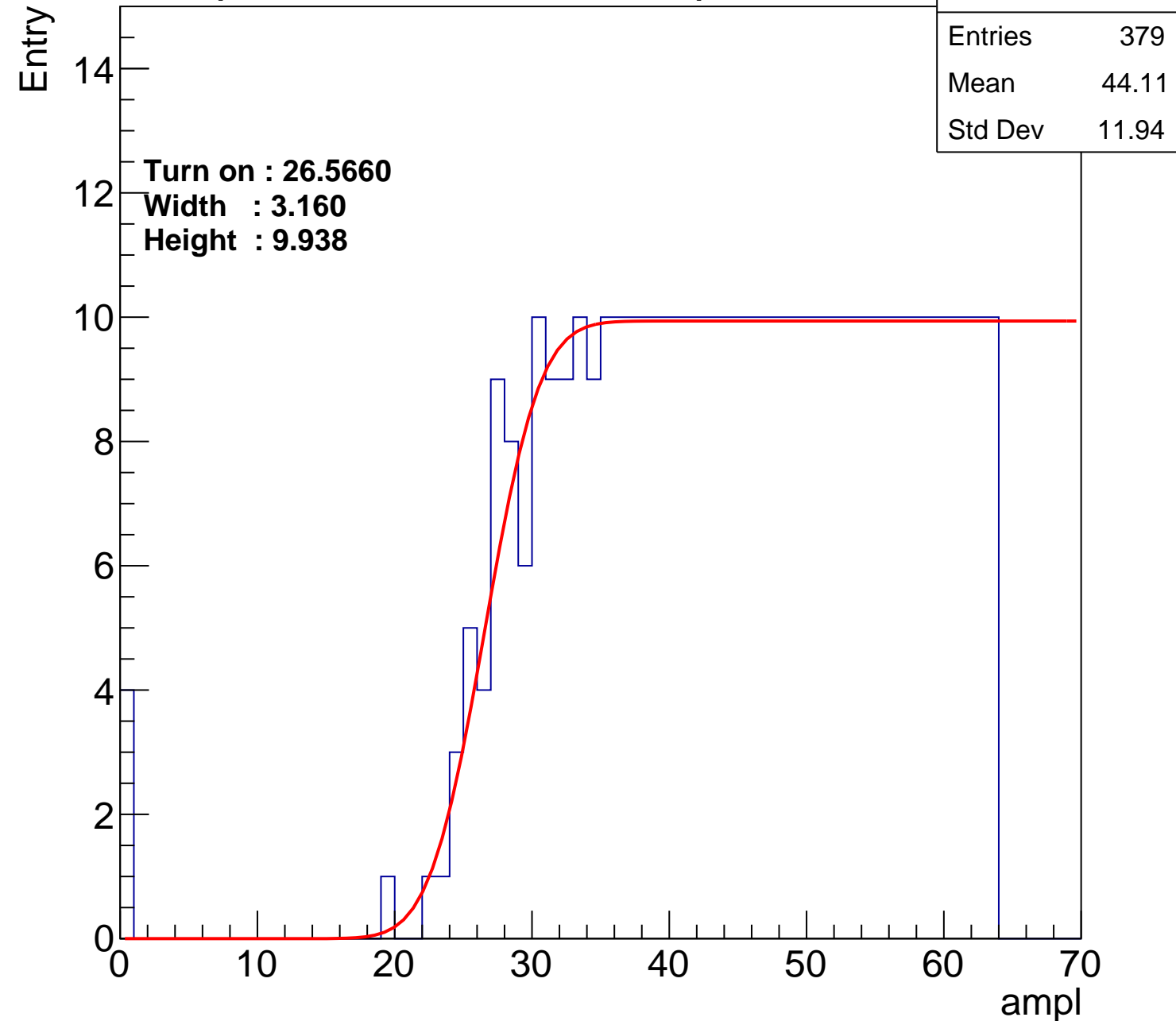
**Width : 3.160**

**Height : 9.938**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch56

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	359
Mean	45.34
Std Dev	10.92

Turn on : 28.6564

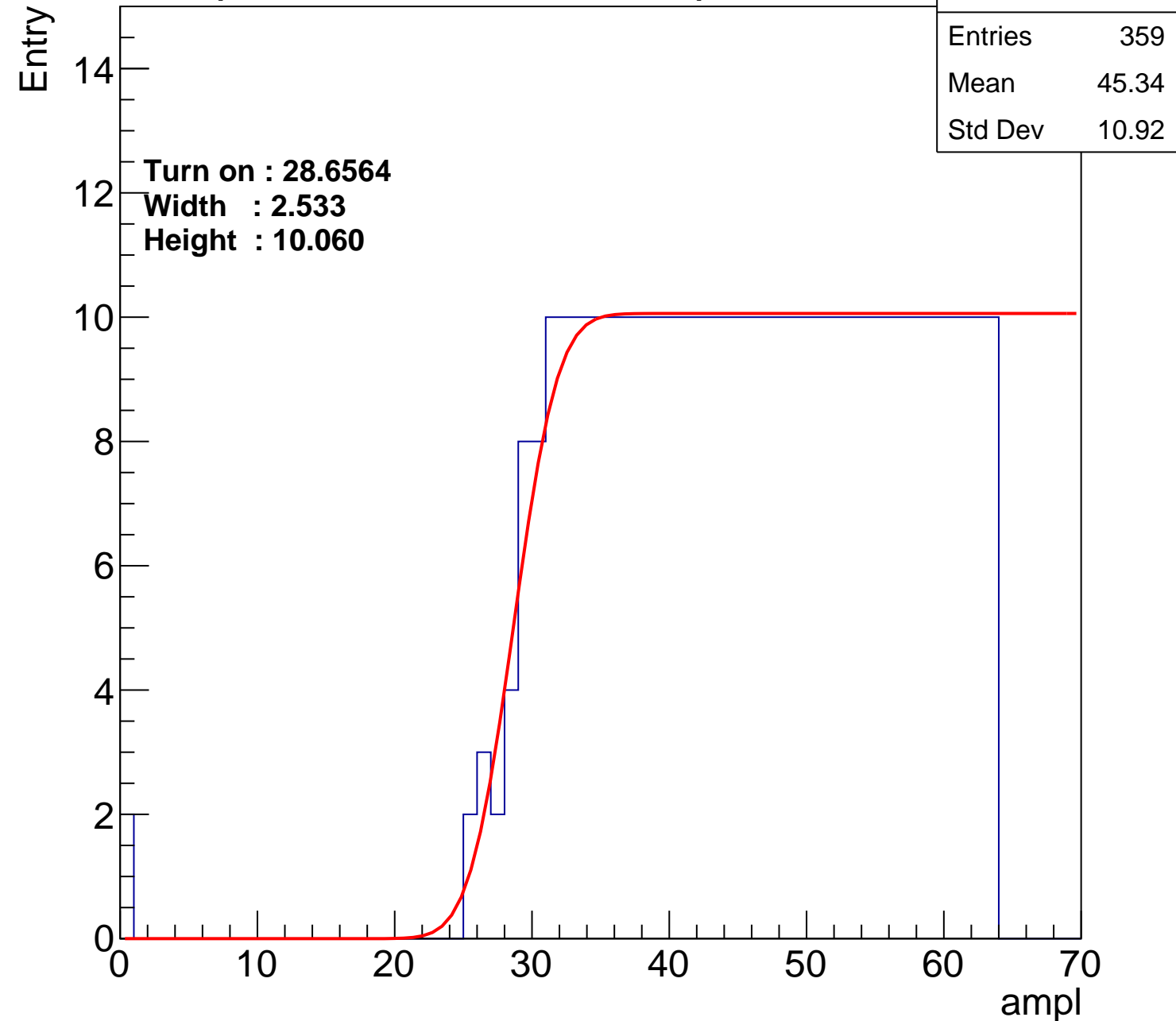
Width : 2.533

Height : 10.060

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch57

calib\_packv5\_042523\_0143.root, FC#5, port B1

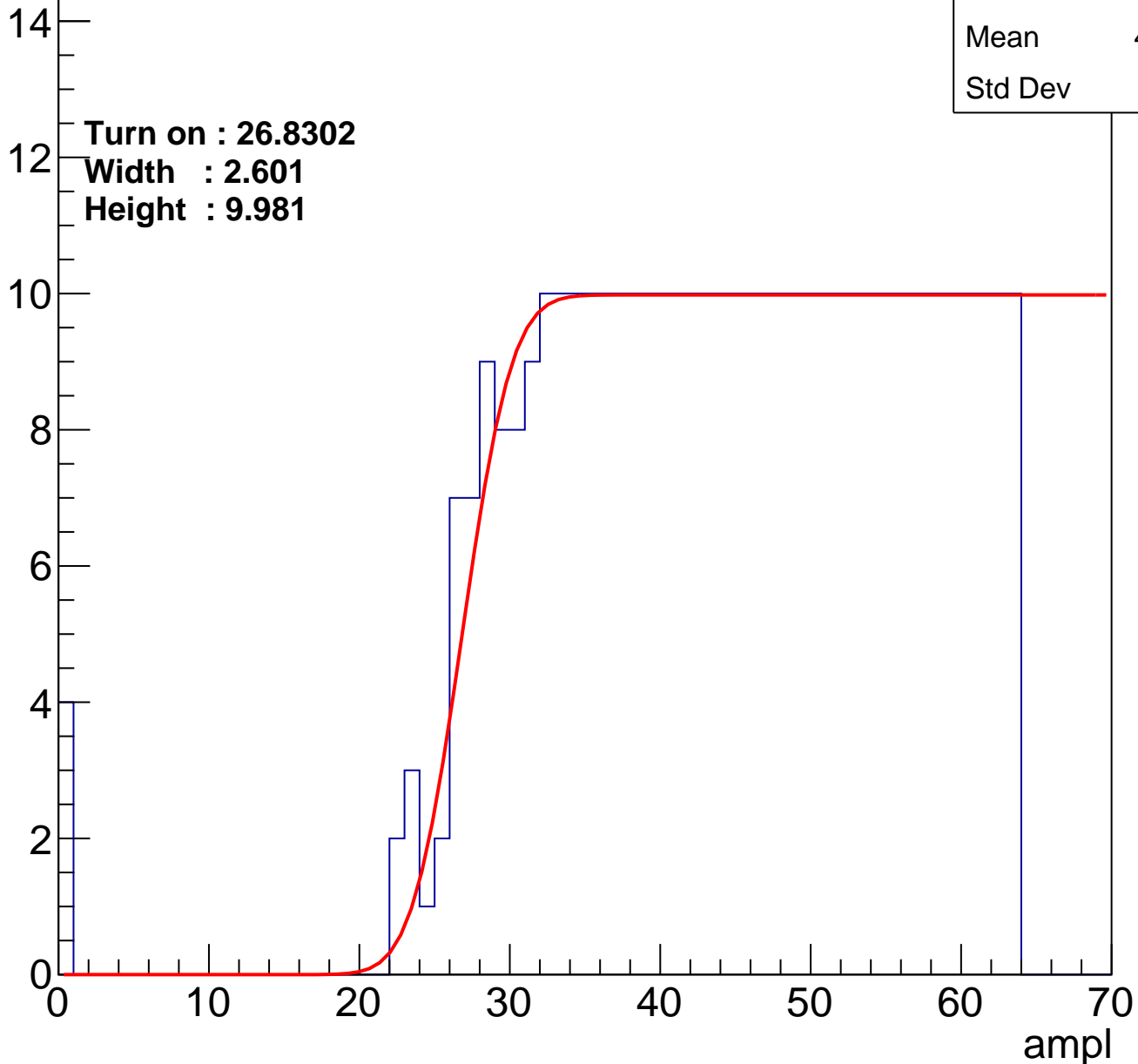
Entry

Entries	380
Mean	44.11
Std Dev	11.9

Turn on : 26.8302

Width : 2.601

Height : 9.981



# B0L000S, U1-ch58

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	372
Mean	44.64
Std Dev	11.33

**Turn on : 26.8941**

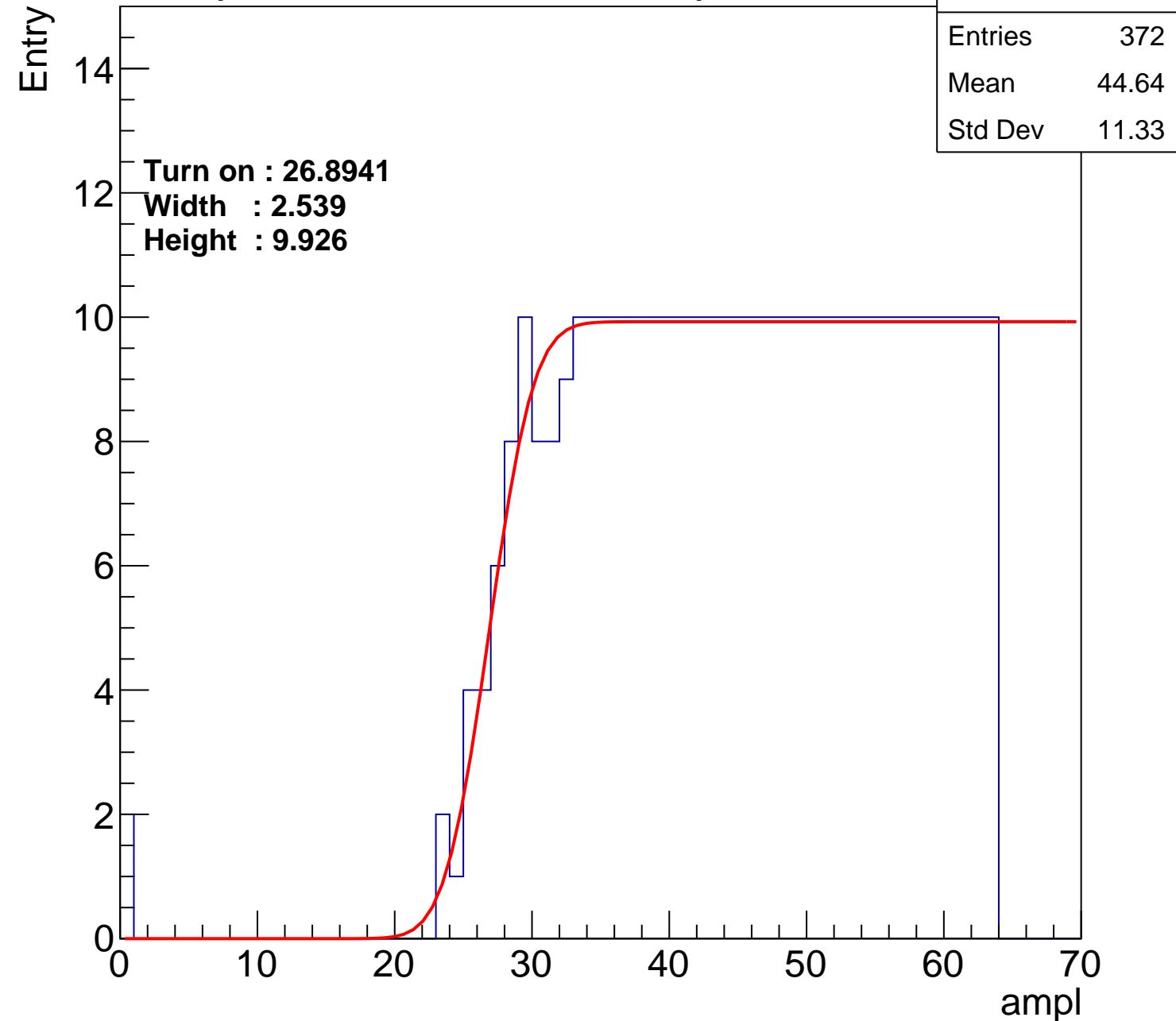
**Width : 2.539**

**Height : 9.926**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch59

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	378
Mean	43.99
Std Dev	12.4

Turn on : 26.6515

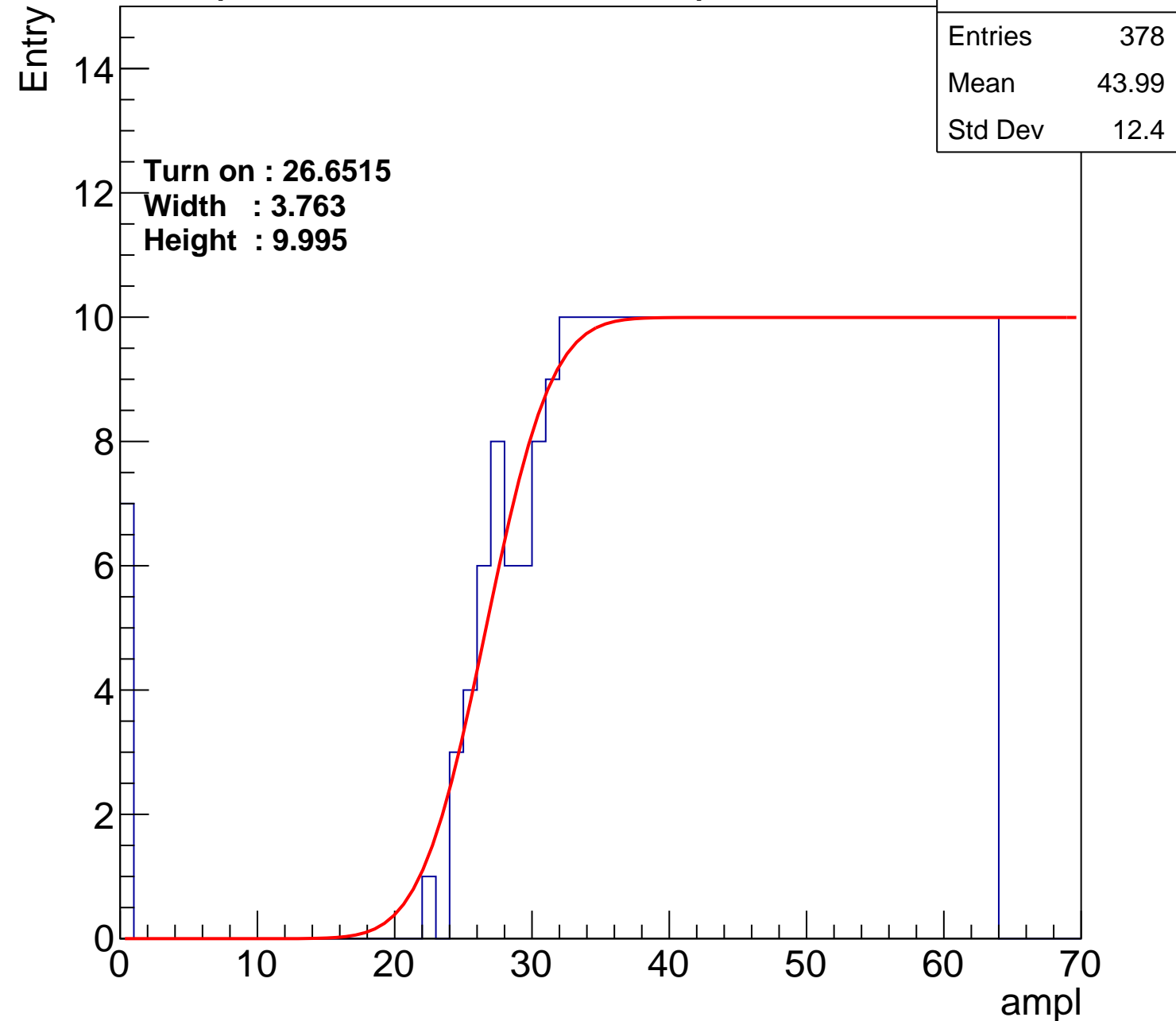
Width : 3.763

Height : 9.995

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch60

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	371
Mean	44.62
Std Dev	11.5

Turn on : 27.4172

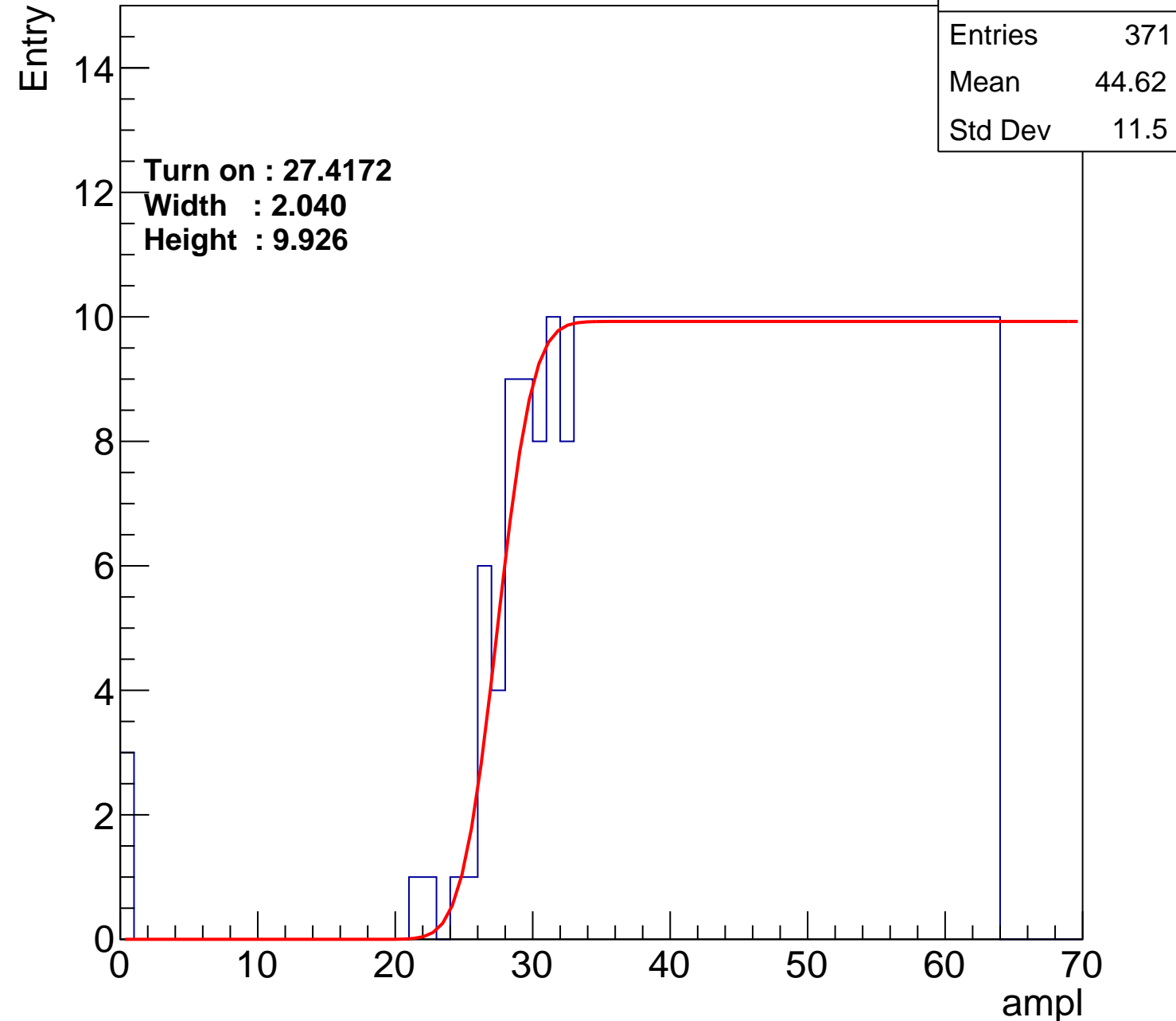
Width : 2.040

Height : 9.926

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch61

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	378
Mean	44.21
Std Dev	11.85

Turn on : 26.7652

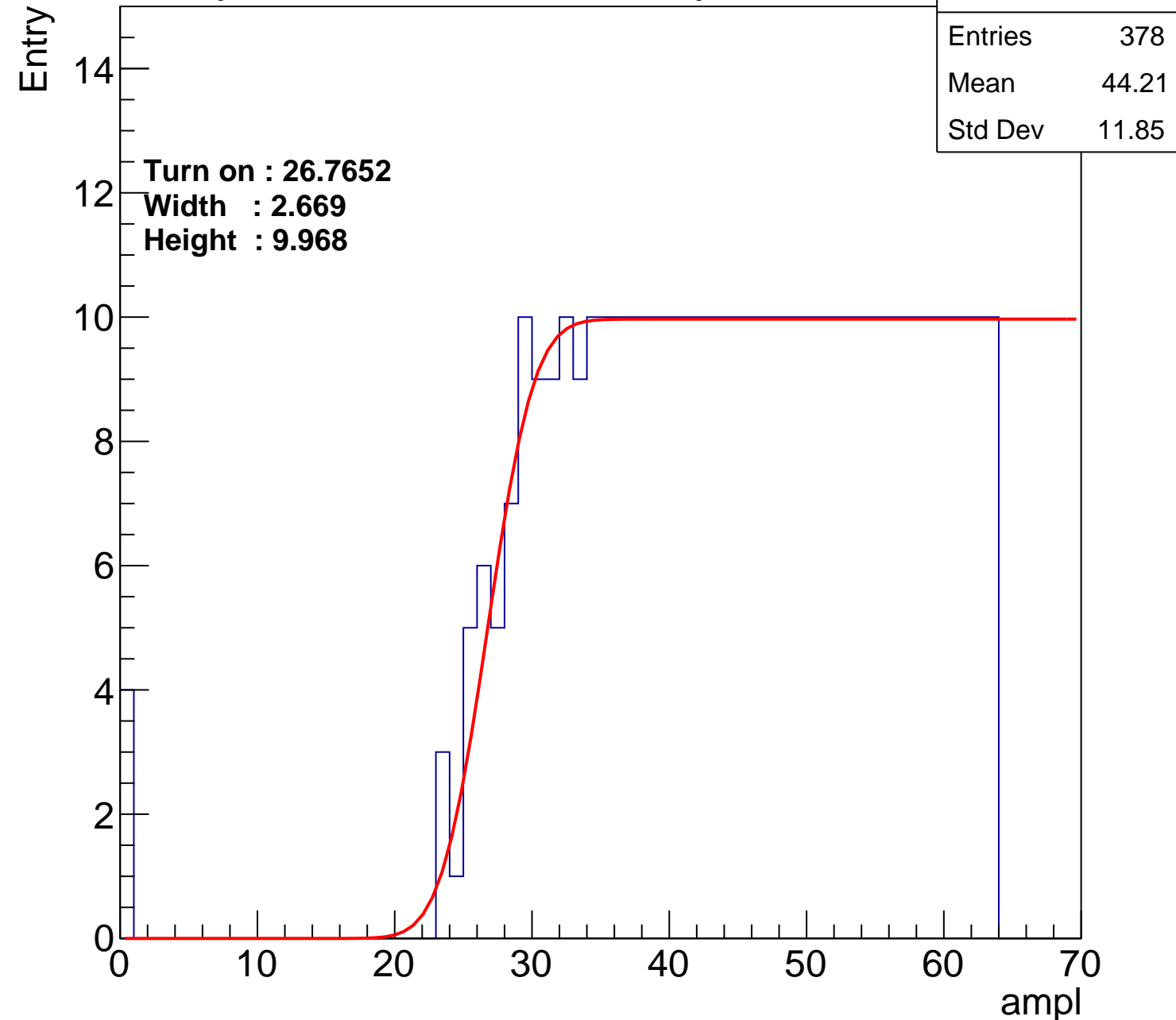
Width : 2.669

Height : 9.968

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch62

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	365
Mean	45.06
Std Dev	10.95

**Turn on : 27.9170**

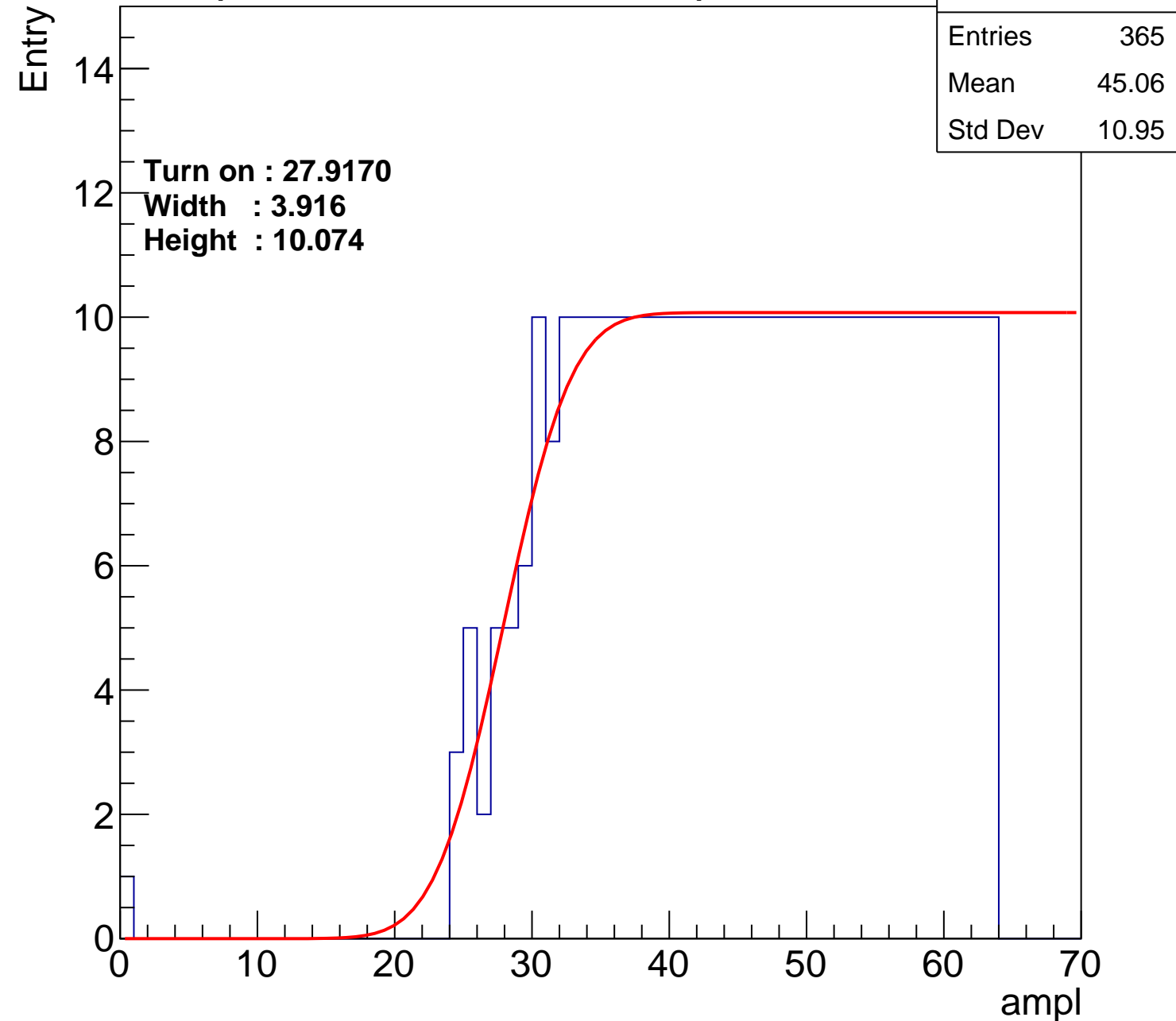
**Width : 3.916**

**Height : 10.074**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L000S, U1-ch63

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	374
Mean	44.59
Std Dev	11.23

**Turn on : 25.9433**

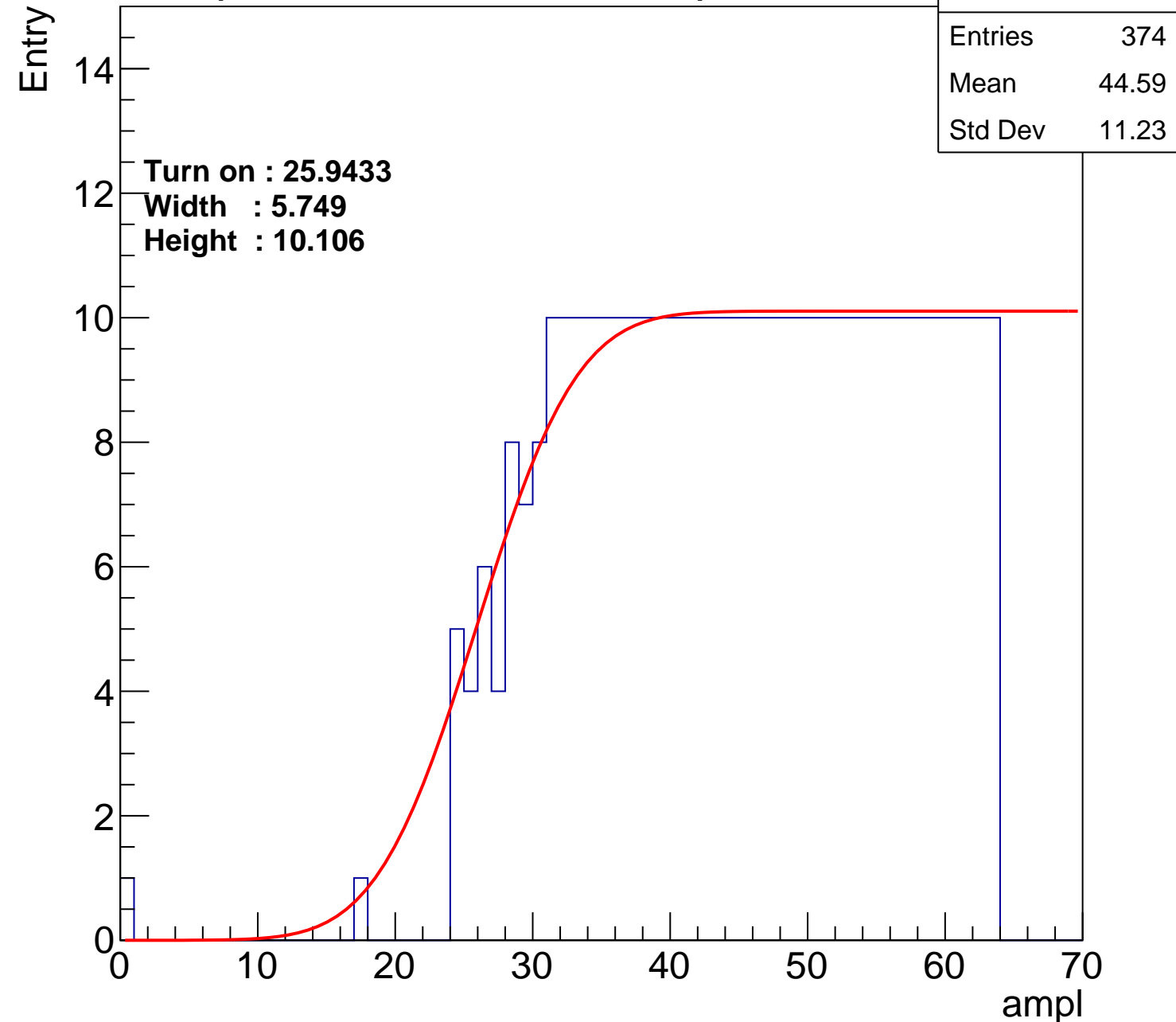
**Width : 5.749**

**Height : 10.106**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch64

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	390
Mean	43.75
Std Dev	11.74

Turn on : 25.3345

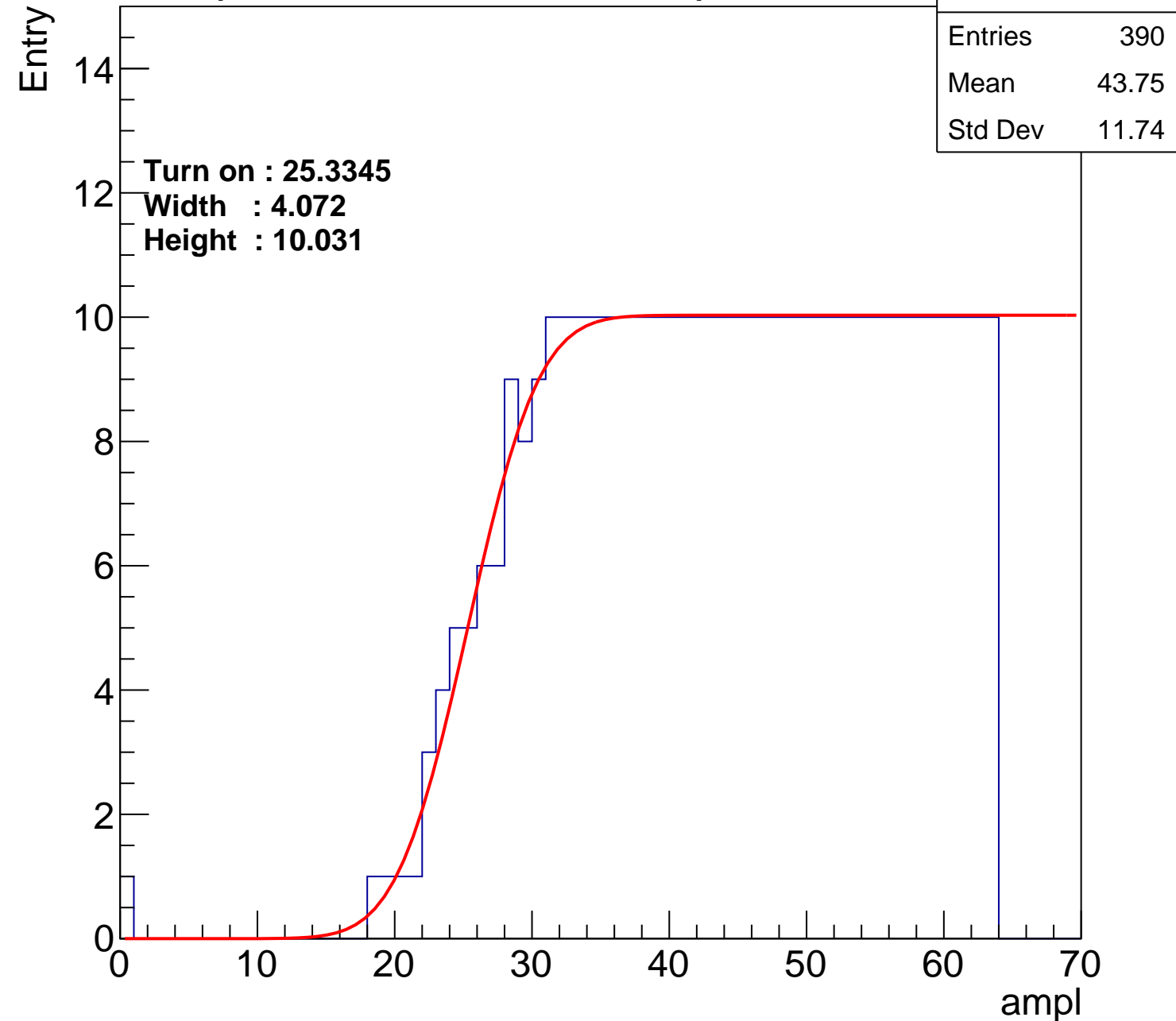
Width : 4.072

Height : 10.031

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch65

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	374
Mean	44.49
Std Dev	11.55

Turn on : 27.3297

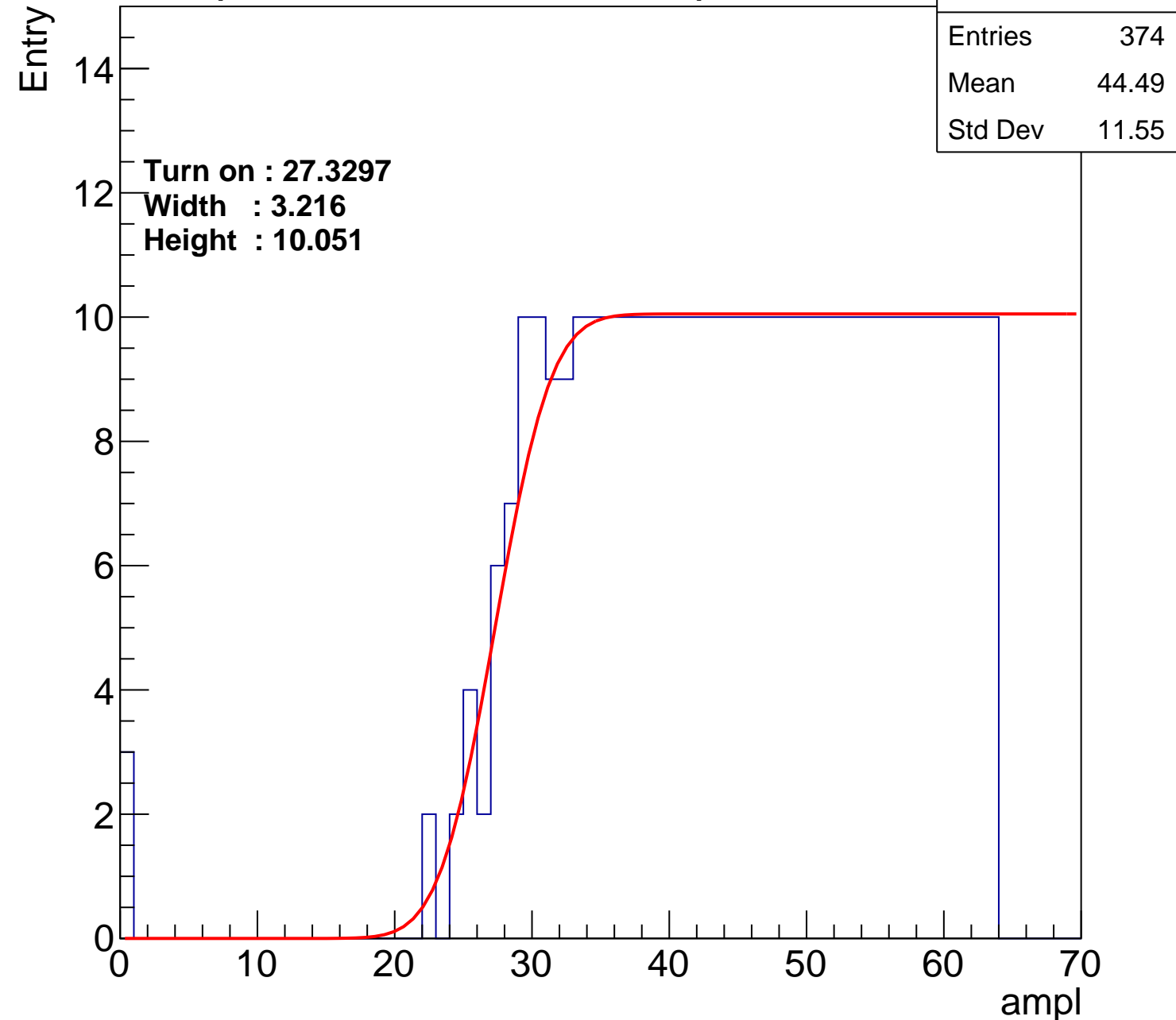
Width : 3.216

Height : 10.051

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch66

calib\_packv5\_042523\_0143.root, FC#5, port B1

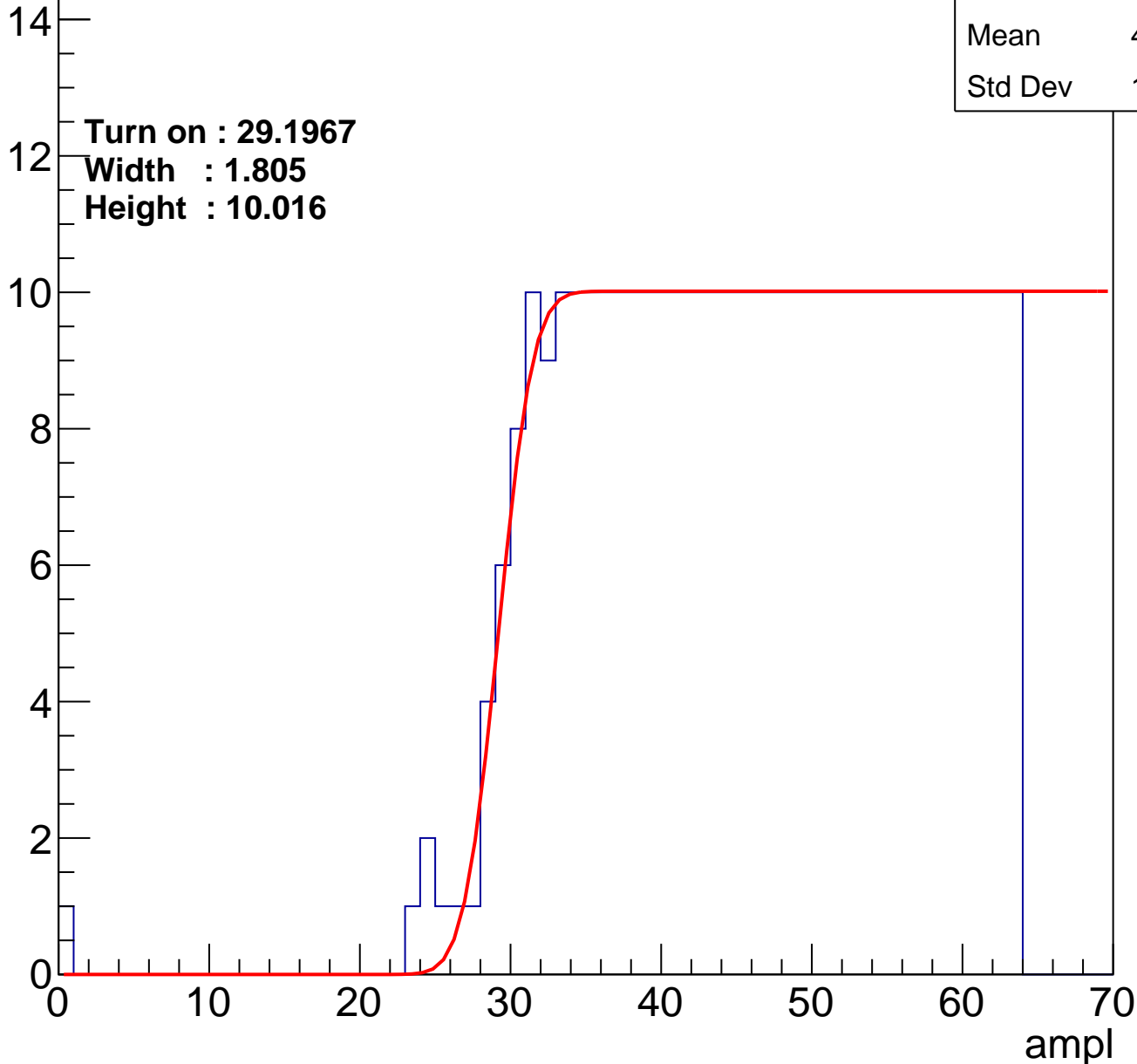
Entry

Entries	354
Mean	45.63
Std Dev	10.62

Turn on : 29.1967

Width : 1.805

Height : 10.016



# B0L000S, U1-ch67

calib\_packv5\_042523\_0143.root, FC#5, port B1

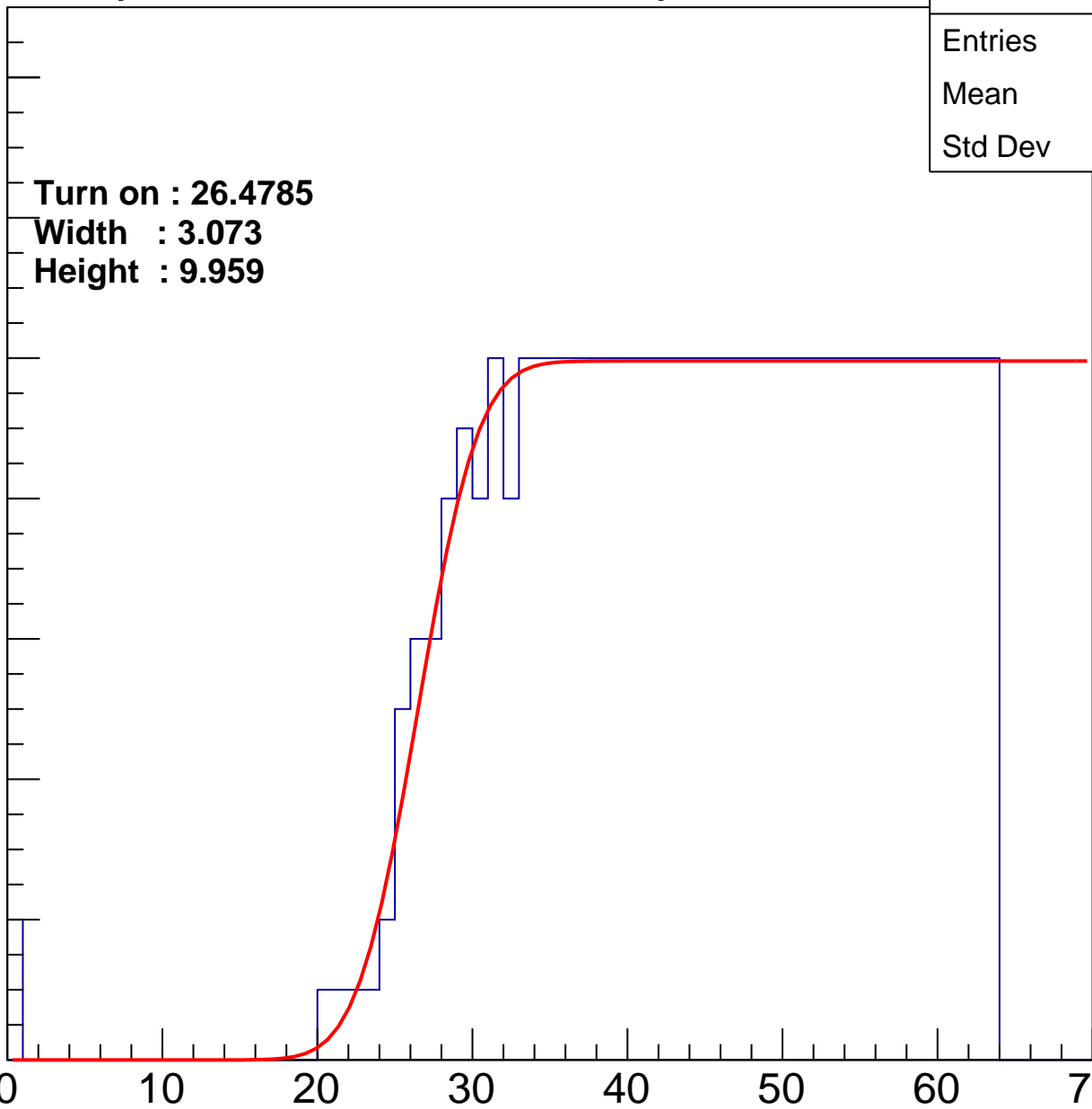
Entry

14  
12  
10  
8  
6  
4  
2  
0

**Turn on : 26.4785**  
**Width : 3.073**  
**Height : 9.959**

Entries	378
Mean	44.31
Std Dev	11.55

ampl



# B0L000S, U1-ch68

calib\_packv5\_042523\_0143.root, FC#5, port B1

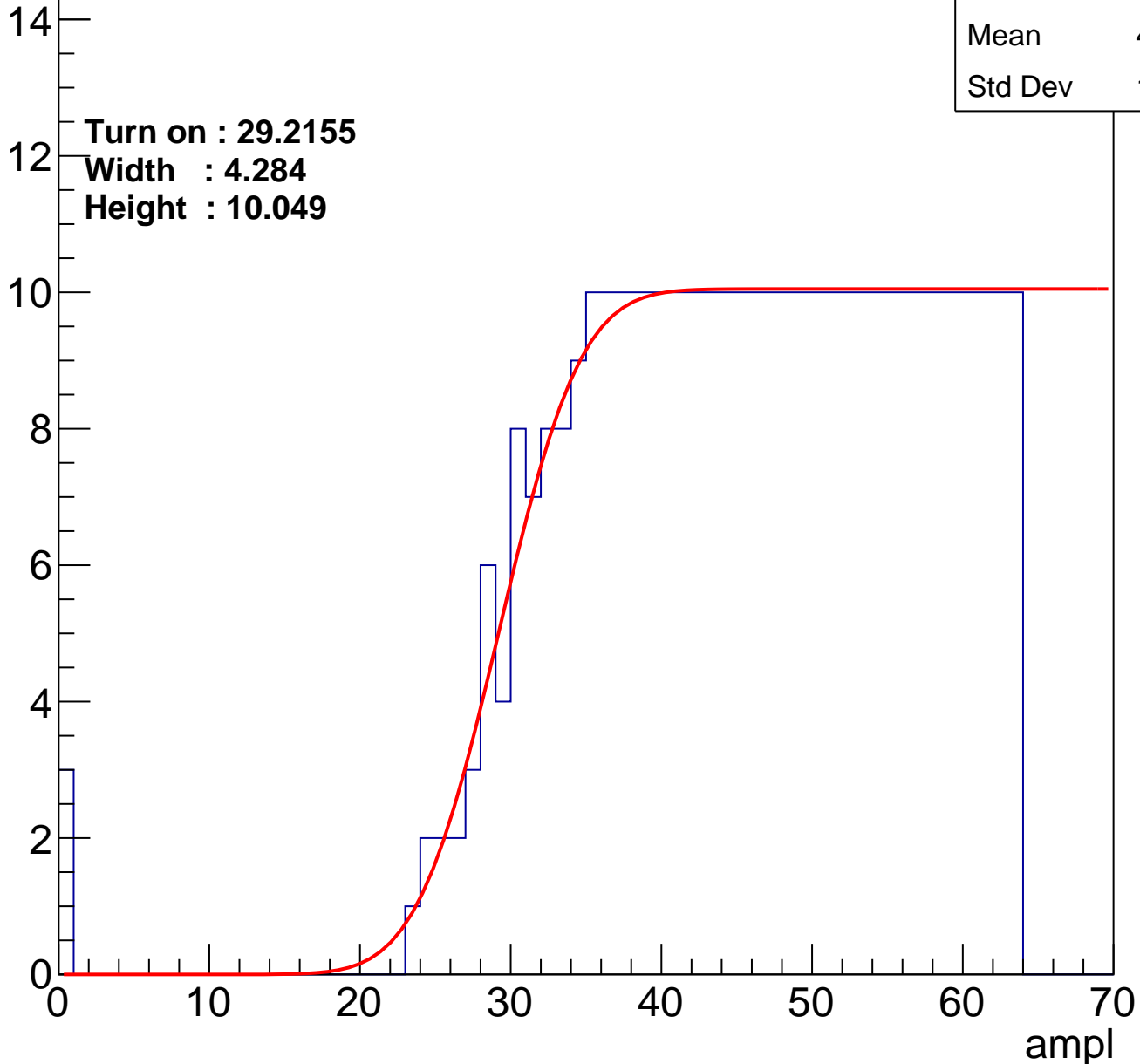
Entries	353
Mean	45.41
Std Dev	11.21

**Turn on : 29.2155**

**Width : 4.284**

**Height : 10.049**

Entry



# B0L000S, U1-ch69

calib\_packv5\_042523\_0143.root, FC#5, port B1

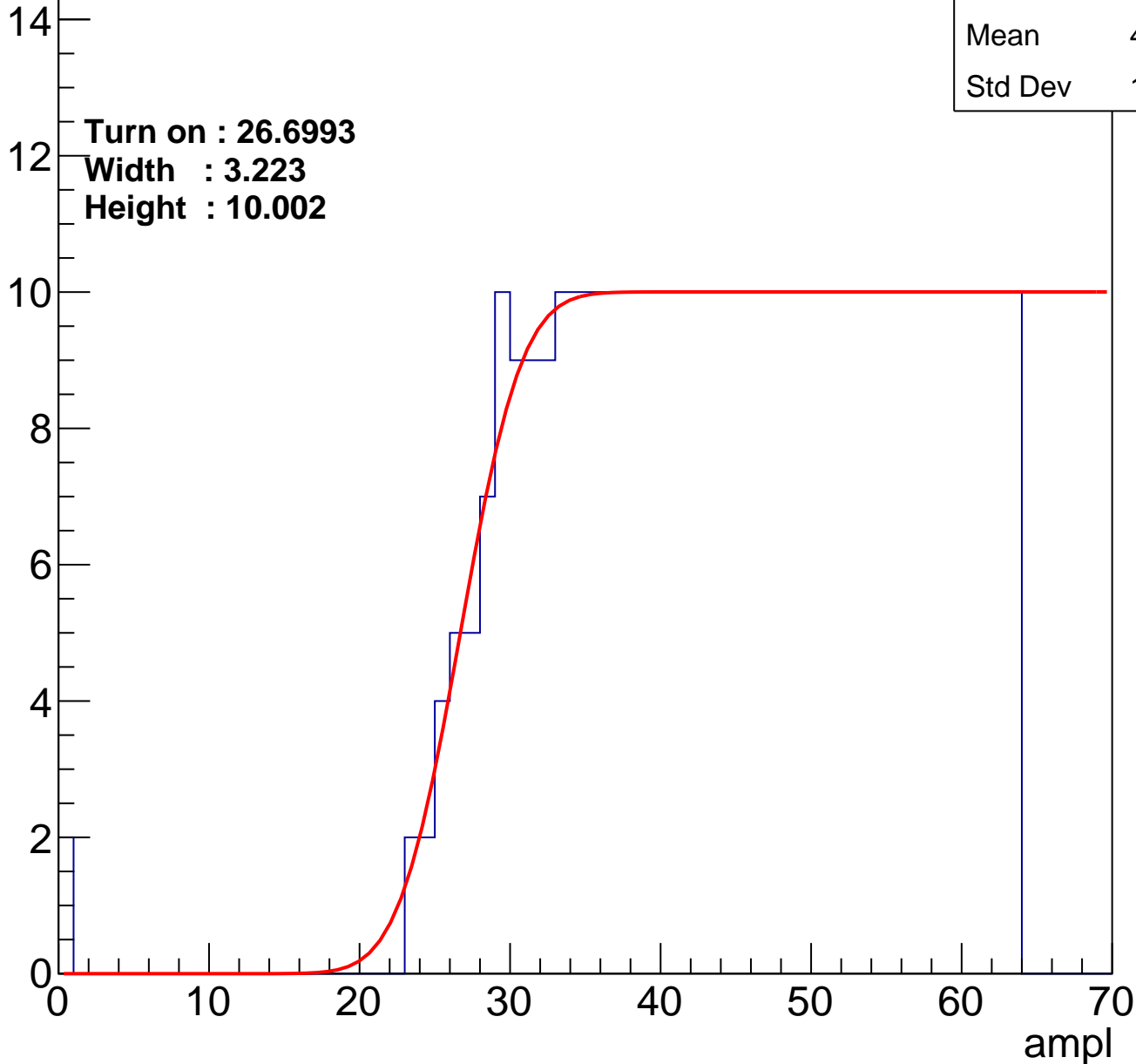
Entries	374
Mean	44.55
Std Dev	11.37

**Turn on : 26.6993**

**Width : 3.223**

**Height : 10.002**

Entry



# B0L000S, U1-ch70

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	371
Mean	44.69
Std Dev	11.31

**Turn on : 27.5378**

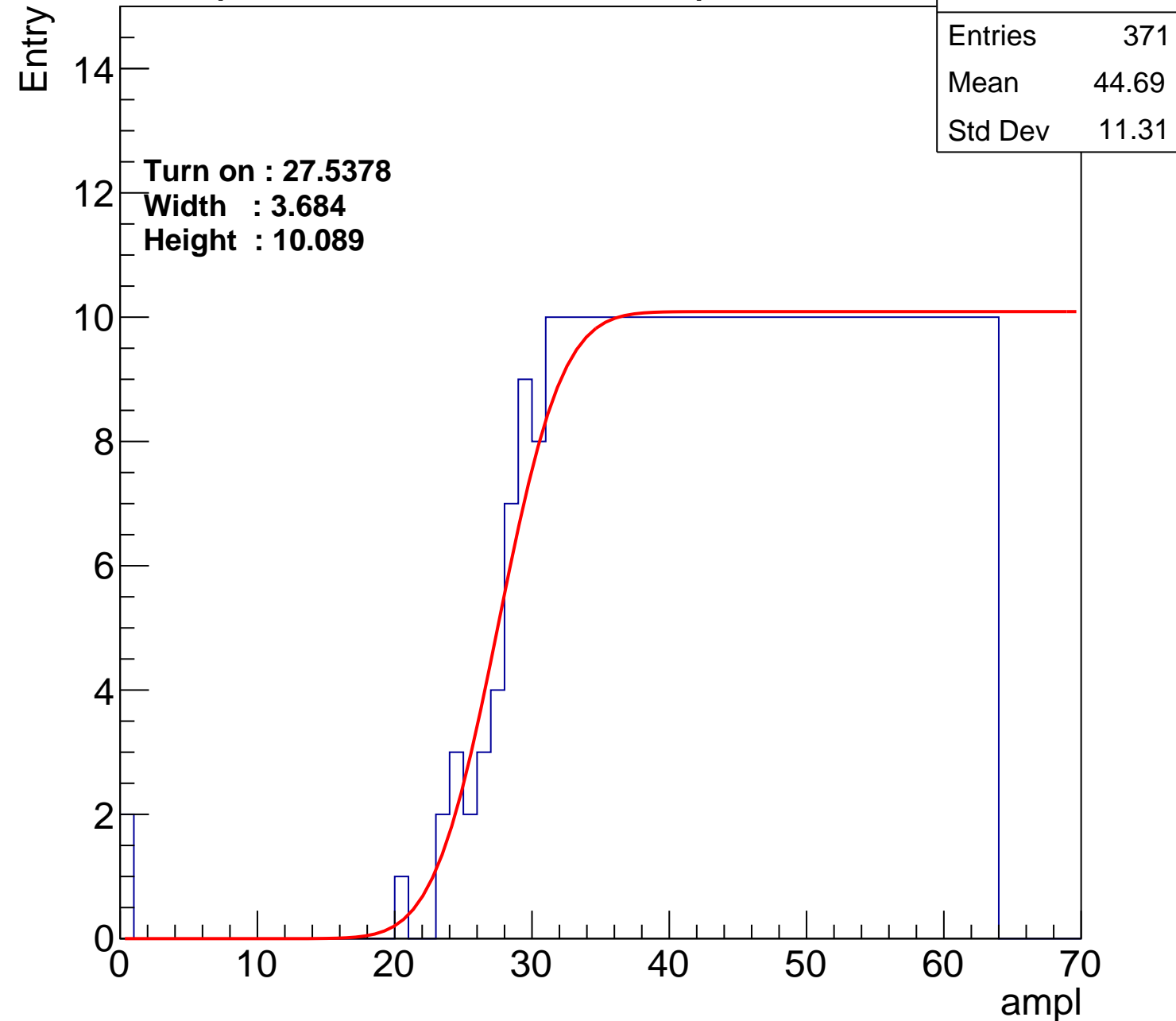
**Width : 3.684**

**Height : 10.089**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L000S, U1-ch71

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	376
Mean	44.28
Std Dev	11.85

Turn on : 27.2896

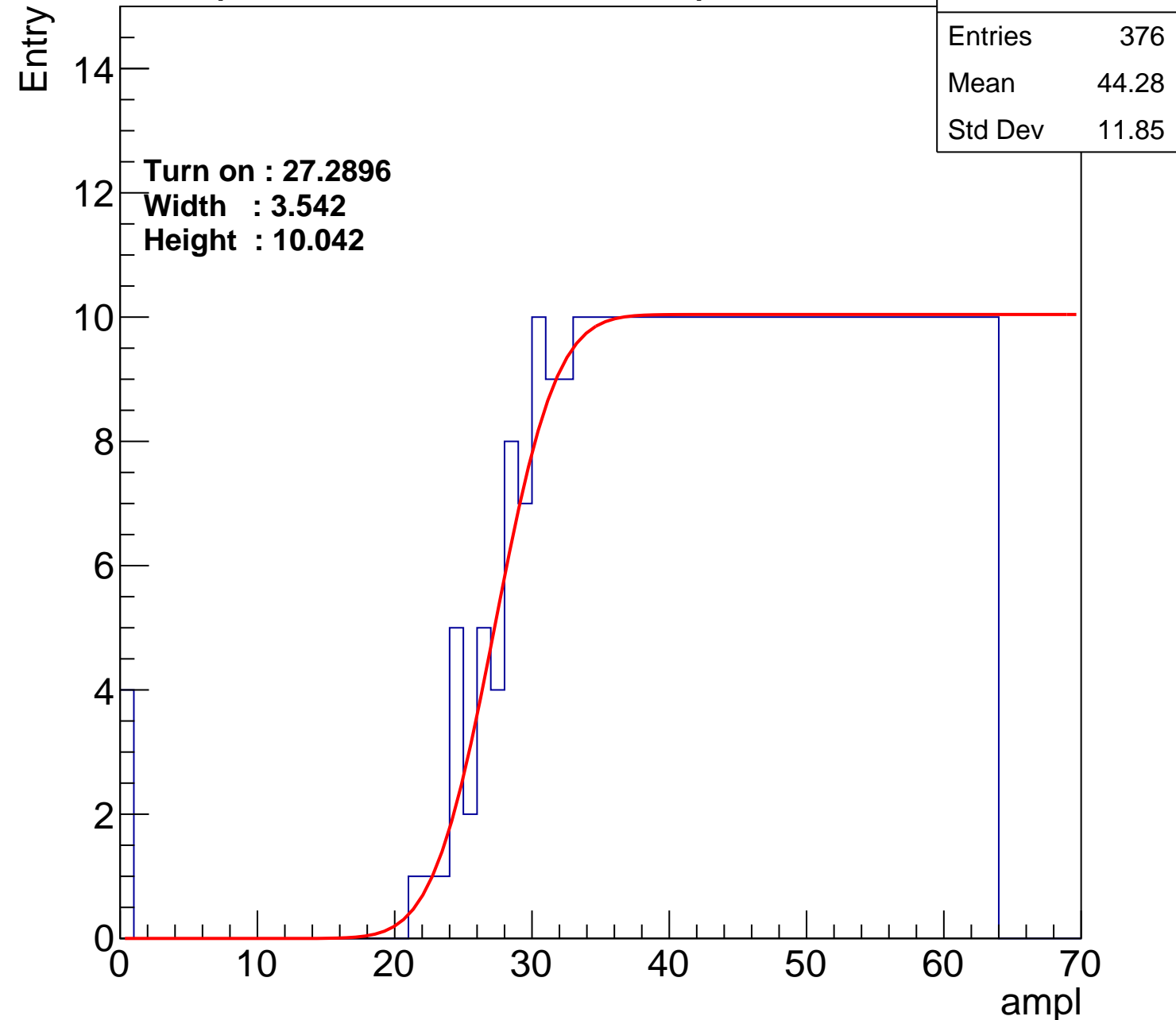
Width : 3.542

Height : 10.042

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch72

calib\_packv5\_042523\_0143.root, FC#5, port B1

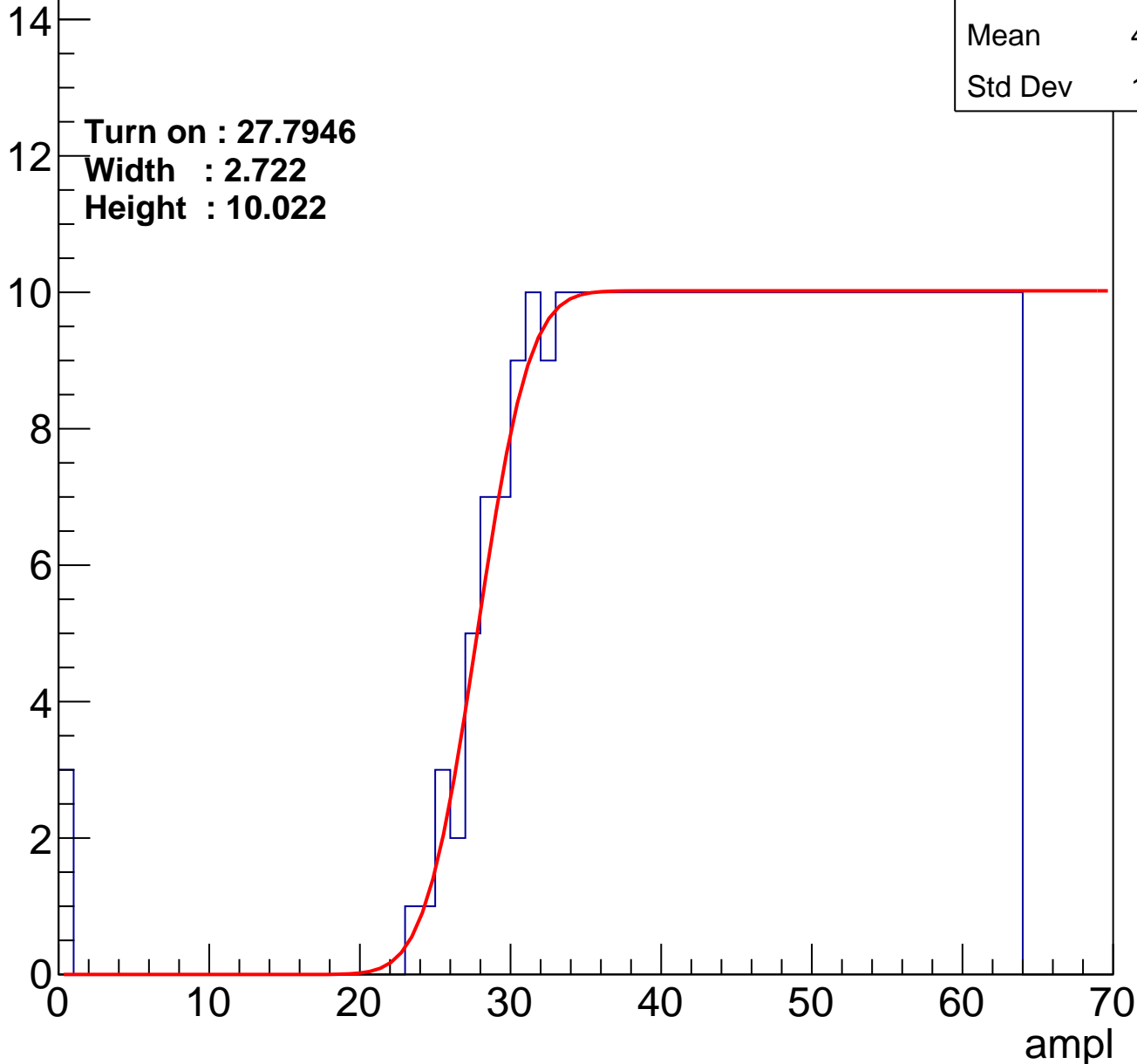
Entry

Entries	367
Mean	44.84
Std Dev	11.37

Turn on : 27.7946

Width : 2.722

Height : 10.022



# B0L000S, U1-ch73

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	364
Mean	44.83
Std Dev	11.71

Turn on : 28.2211

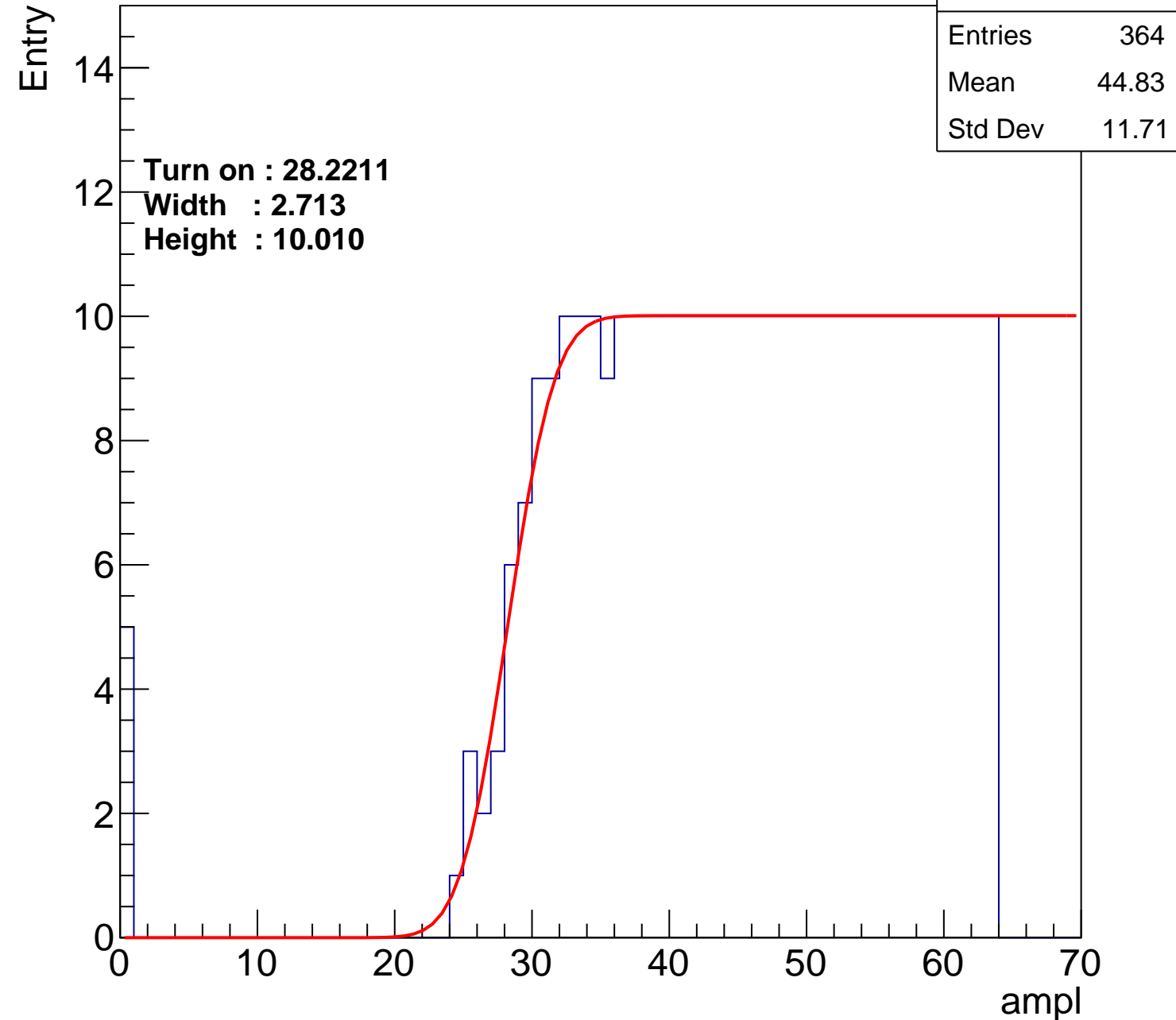
Width : 2.713

Height : 10.010

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch74

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	365
Mean	44.9
Std Dev	11.47

**Turn on : 28.2160**

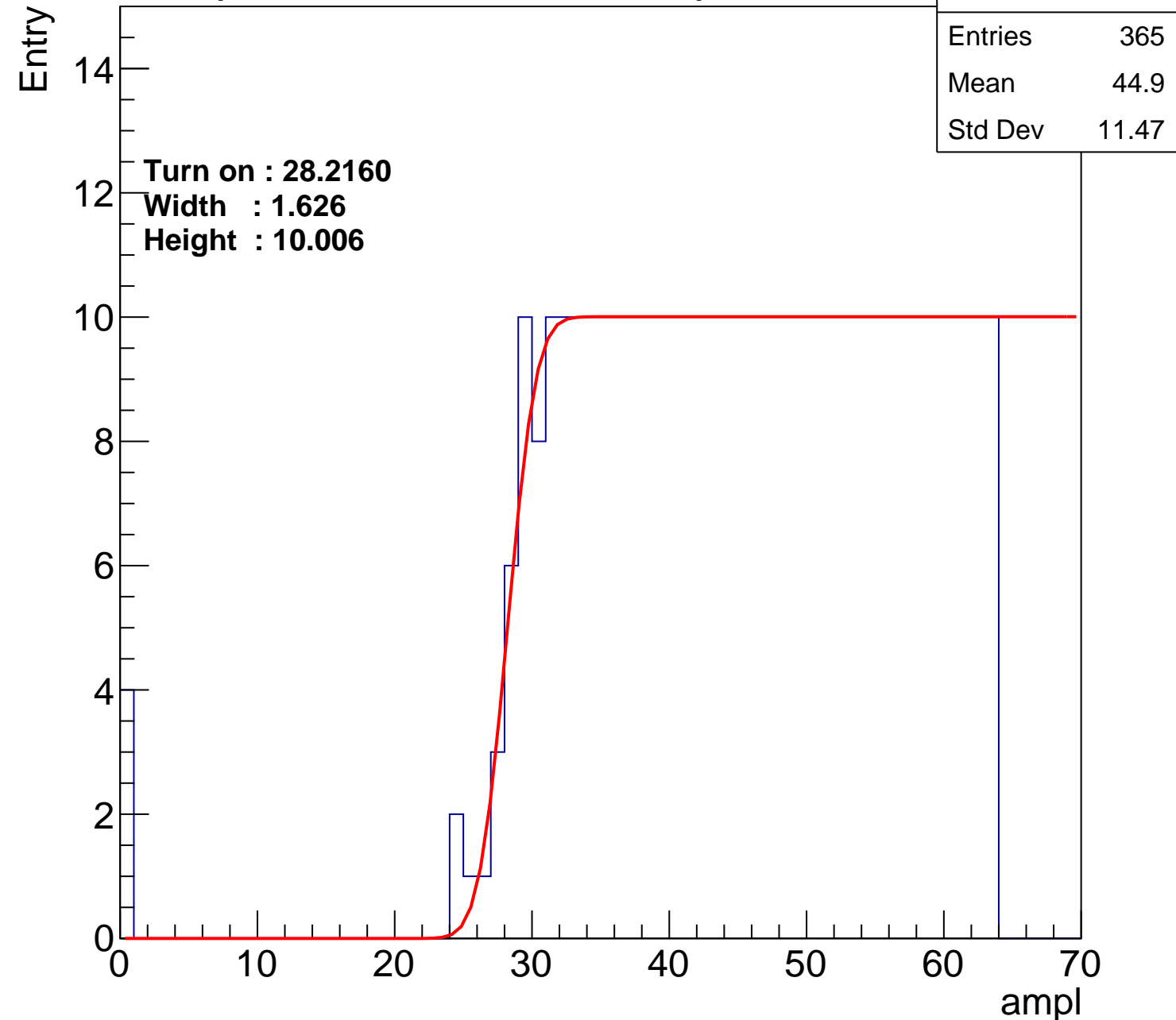
**Width : 1.626**

**Height : 10.006**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch75

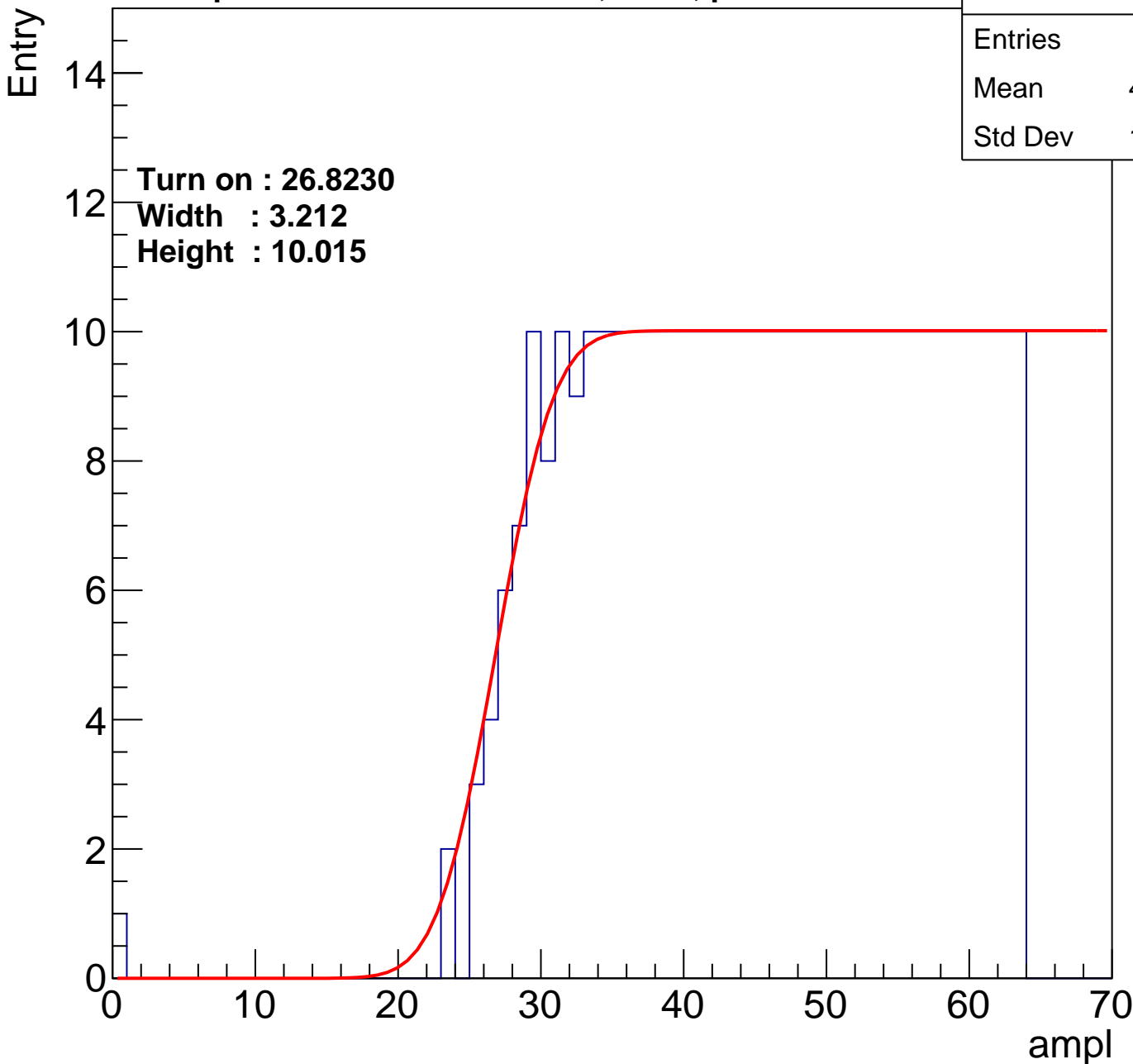
**calib\_packv5\_042523\_0143.root, FC#5, port B1**

Entries	370
Mean	44.84
Std Dev	11.03

**Turn on : 26.8230**

**Width : 3.212**

**Height : 10.015**



# B0L000S, U1-ch76

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	374
Mean	44.41
Std Dev	11.76

Turn on : 27.7350

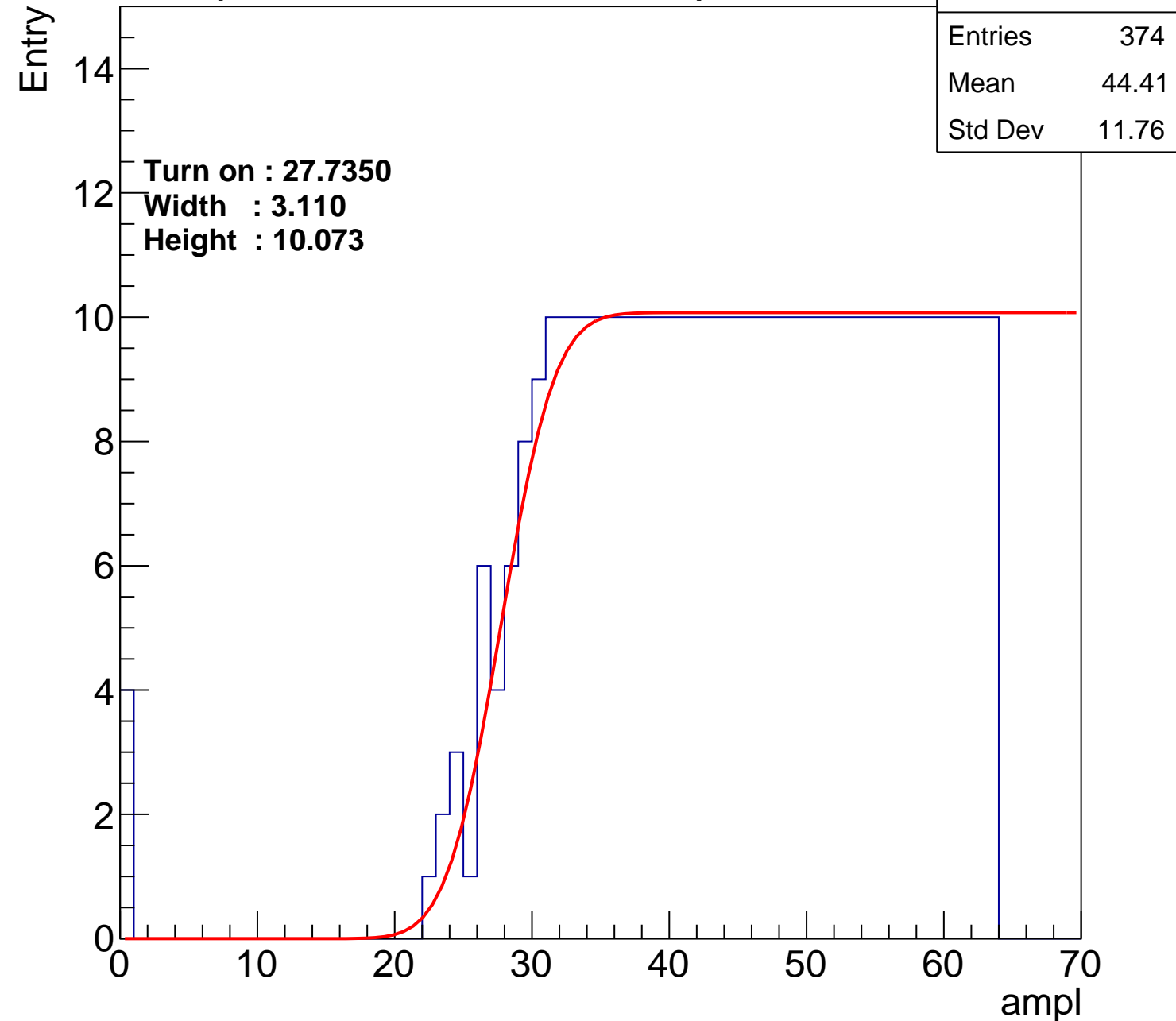
Width : 3.110

Height : 10.073

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch77

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	372
Mean	44.48
Std Dev	11.75

Turn on : 27.4608

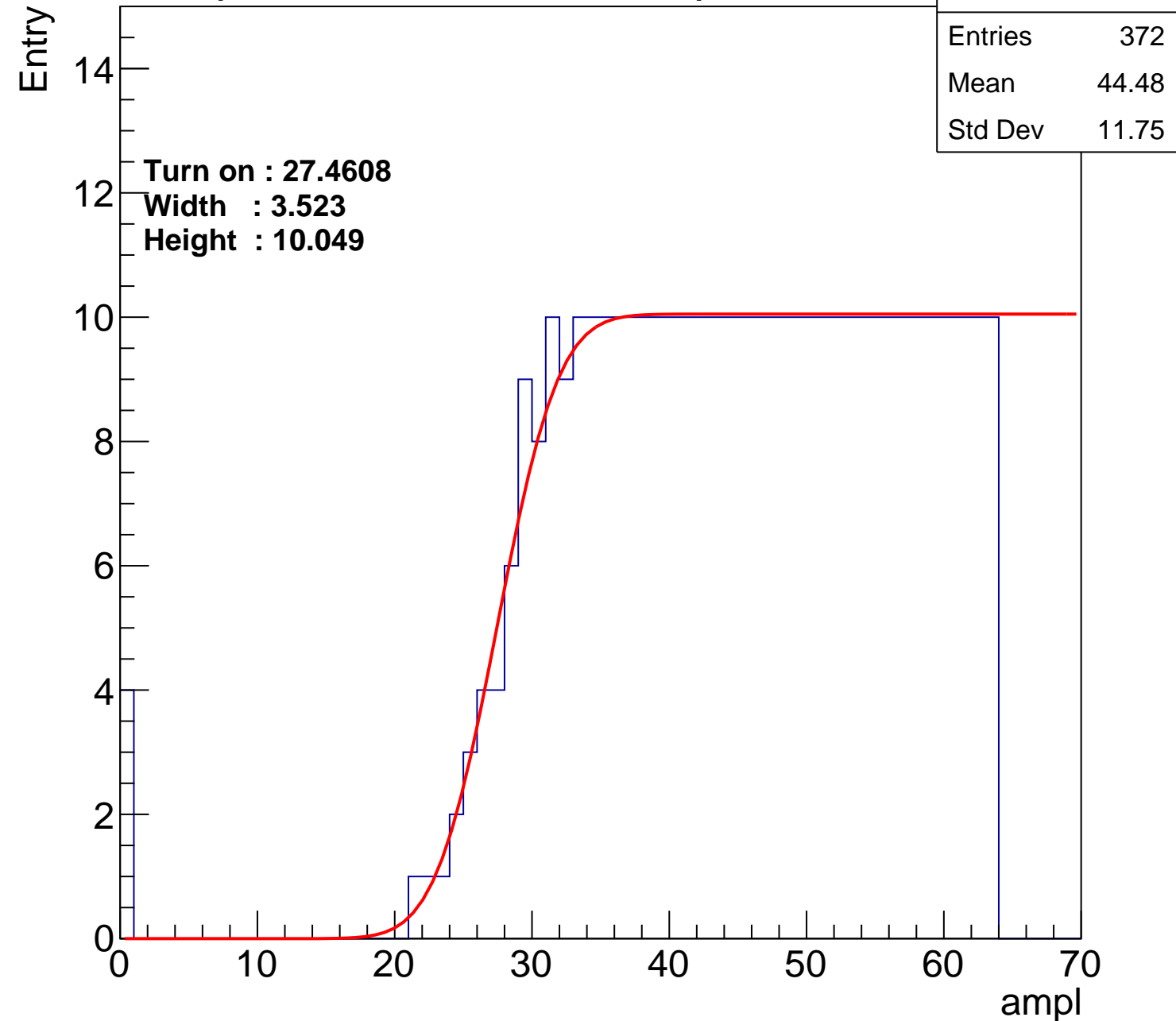
Width : 3.523

Height : 10.049

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch78

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	361
Mean	45.08
Std Dev	11.31

**Turn on : 28.2862**

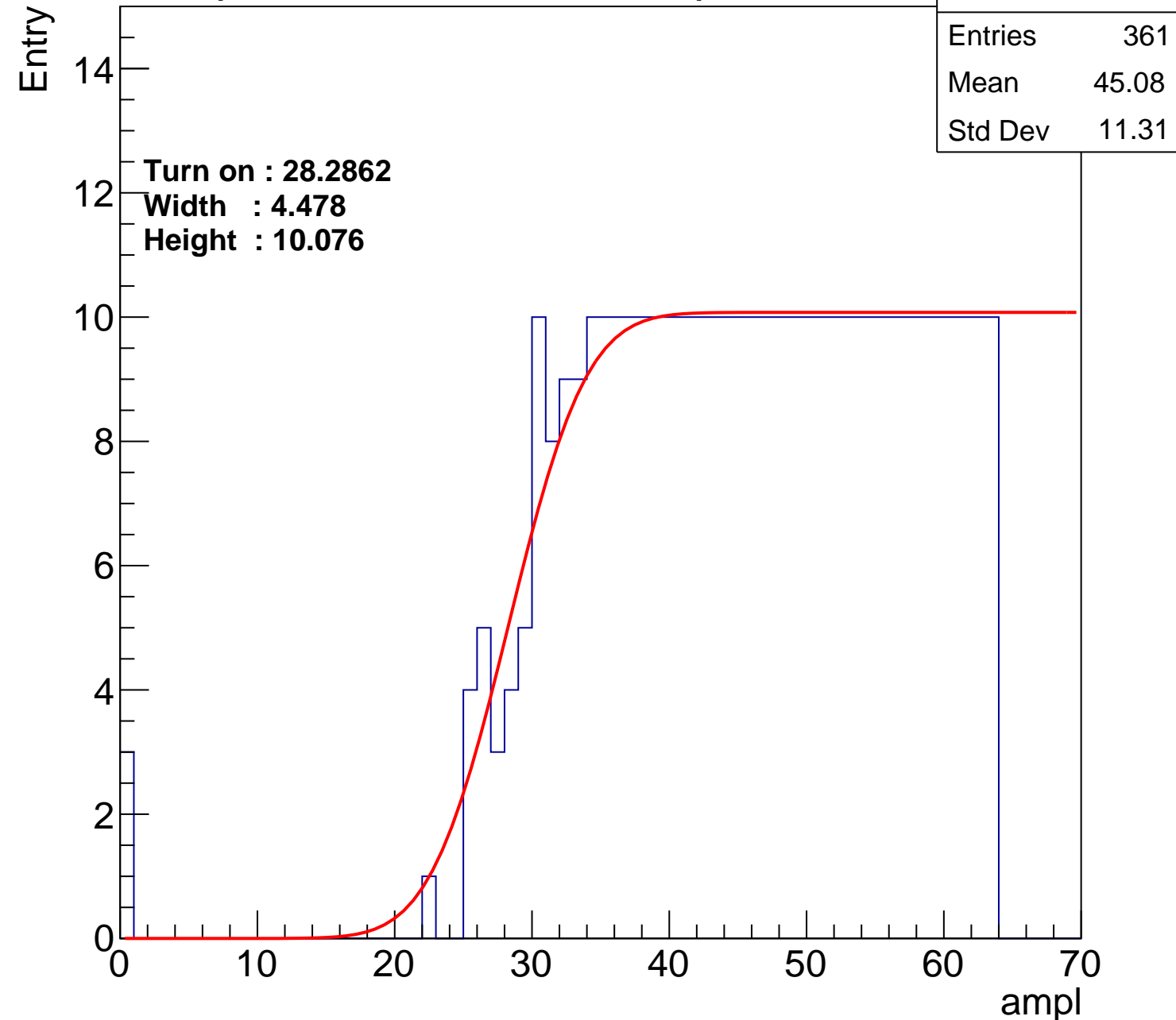
**Width : 4.478**

**Height : 10.076**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L000S, U1-ch79

calib\_packv5\_042523\_0143.root, FC#5, port B1

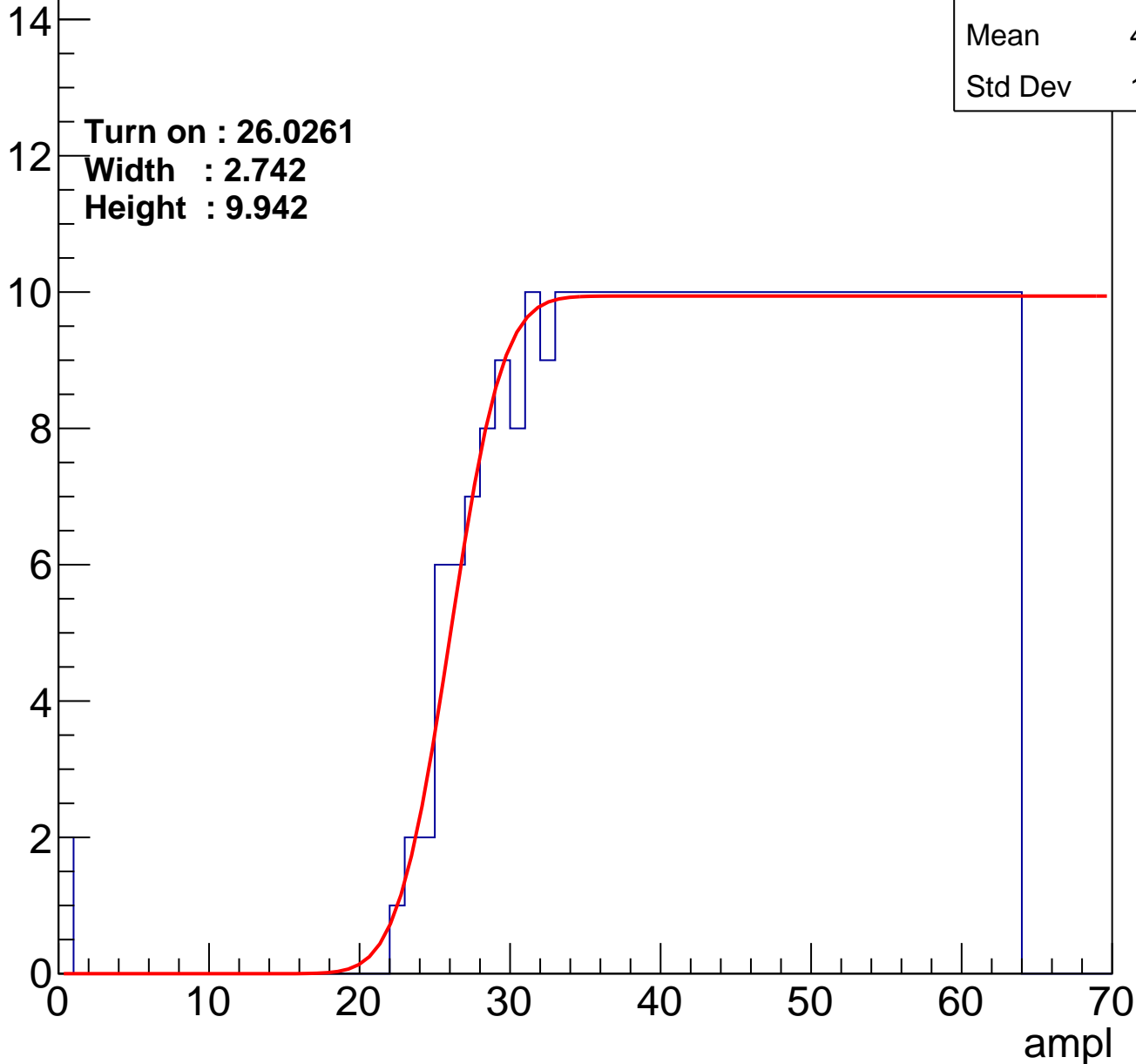
Entry

Entries	380
Mean	44.25
Std Dev	11.53

Turn on : 26.0261

Width : 2.742

Height : 9.942



# B0L000S, U1-ch80

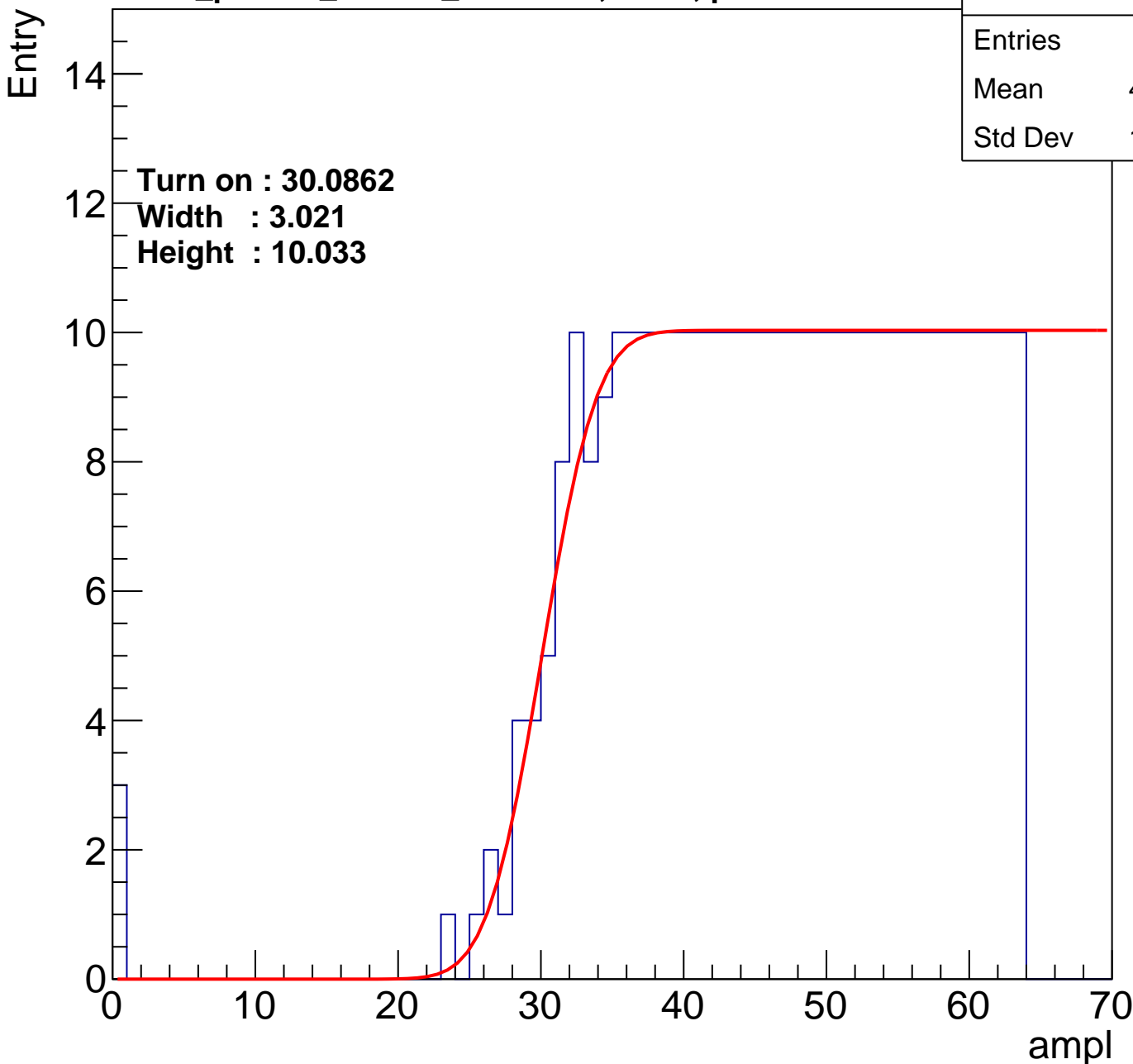
**calib\_packv5\_042523\_0143.root, FC#5, port B1**

Entries	346
Mean	45.82
Std Dev	10.95

**Turn on : 30.0862**

**Width : 3.021**

**Height : 10.033**



# B0L000S, U1-ch81

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	361
Mean	45.12
Std Dev	11.25

**Turn on : 28.5492**

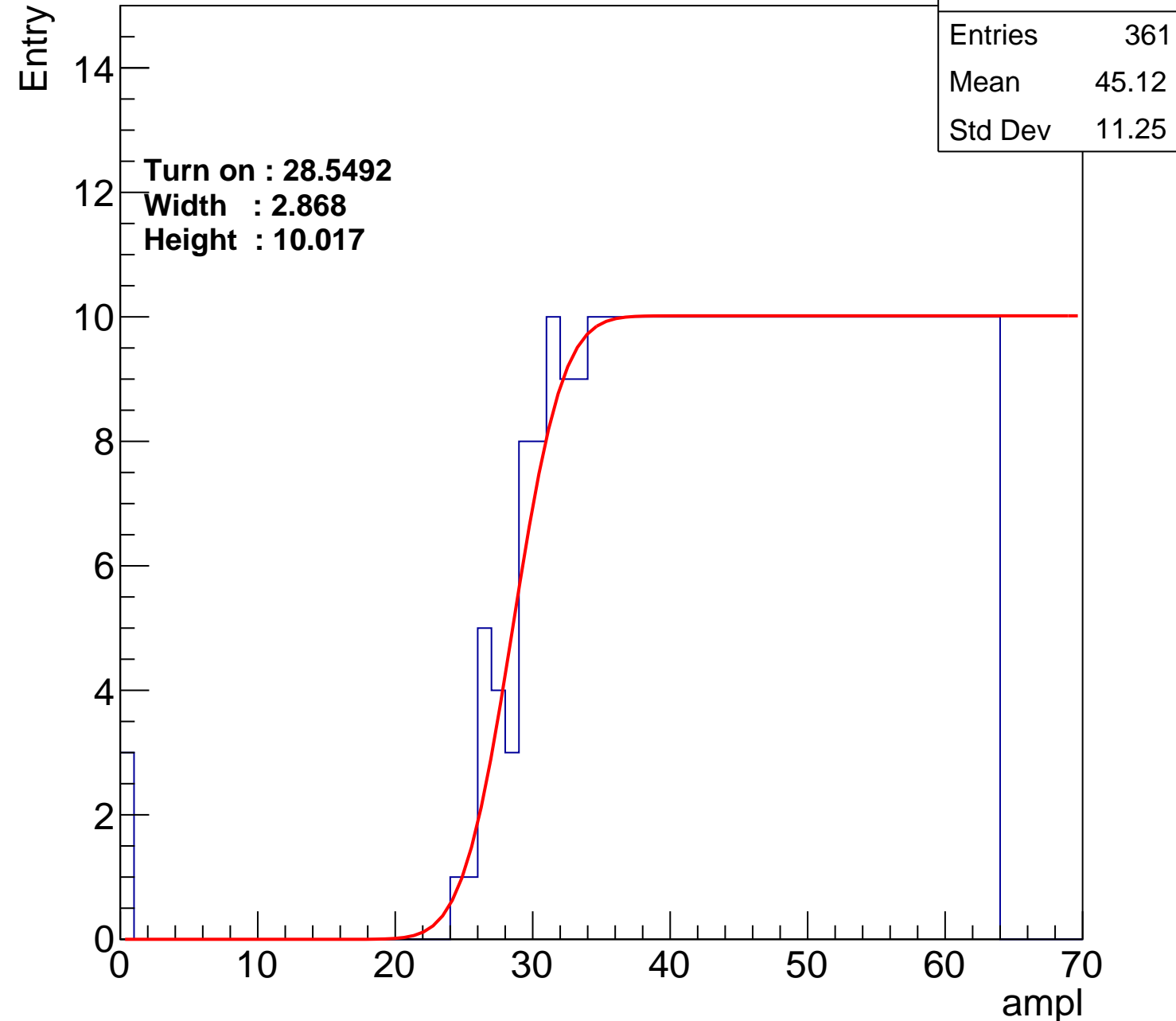
**Width : 2.868**

**Height : 10.017**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch82

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	367
Mean	44.79
Std Dev	11.45

Turn on : 27.8792

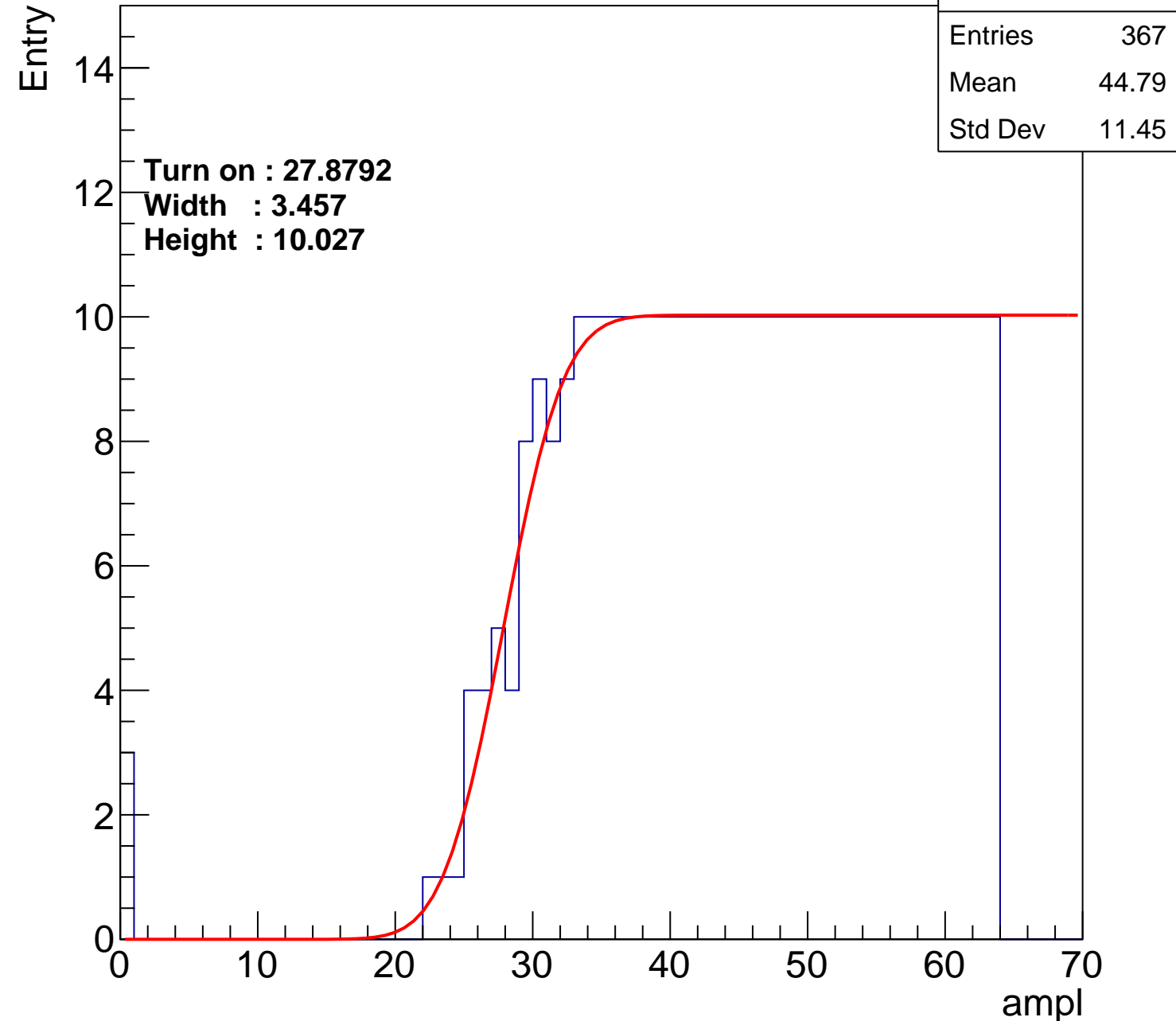
Width : 3.457

Height : 10.027

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch83

calib\_packv5\_042523\_0143.root, FC#5, port B1

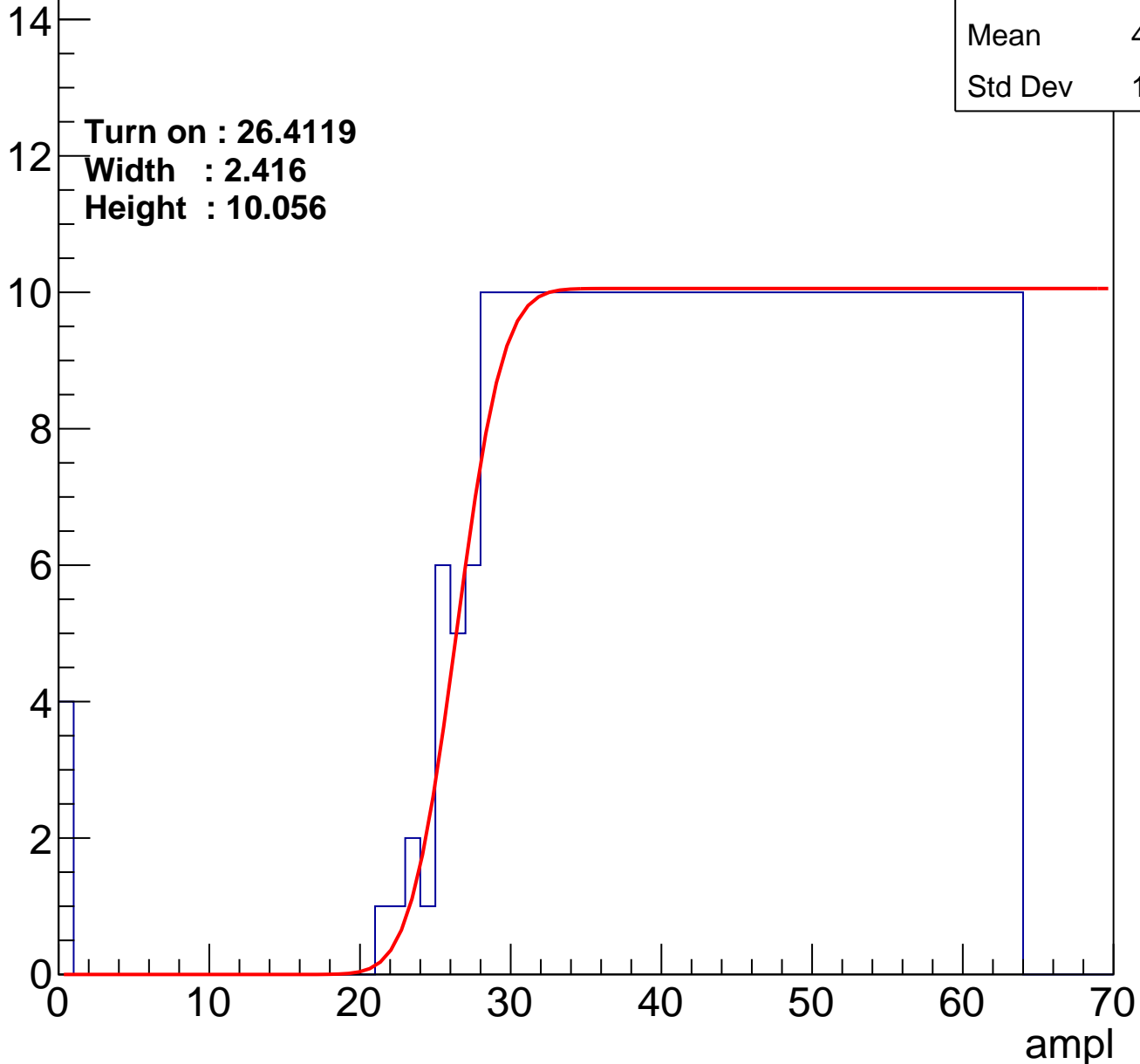
Entries	386
Mean	43.87
Std Dev	11.96

**Turn on : 26.4119**

**Width : 2.416**

**Height : 10.056**

Entry



# B0L000S, U1-ch84

calib\_packv5\_042523\_0143.root, FC#5, port B1

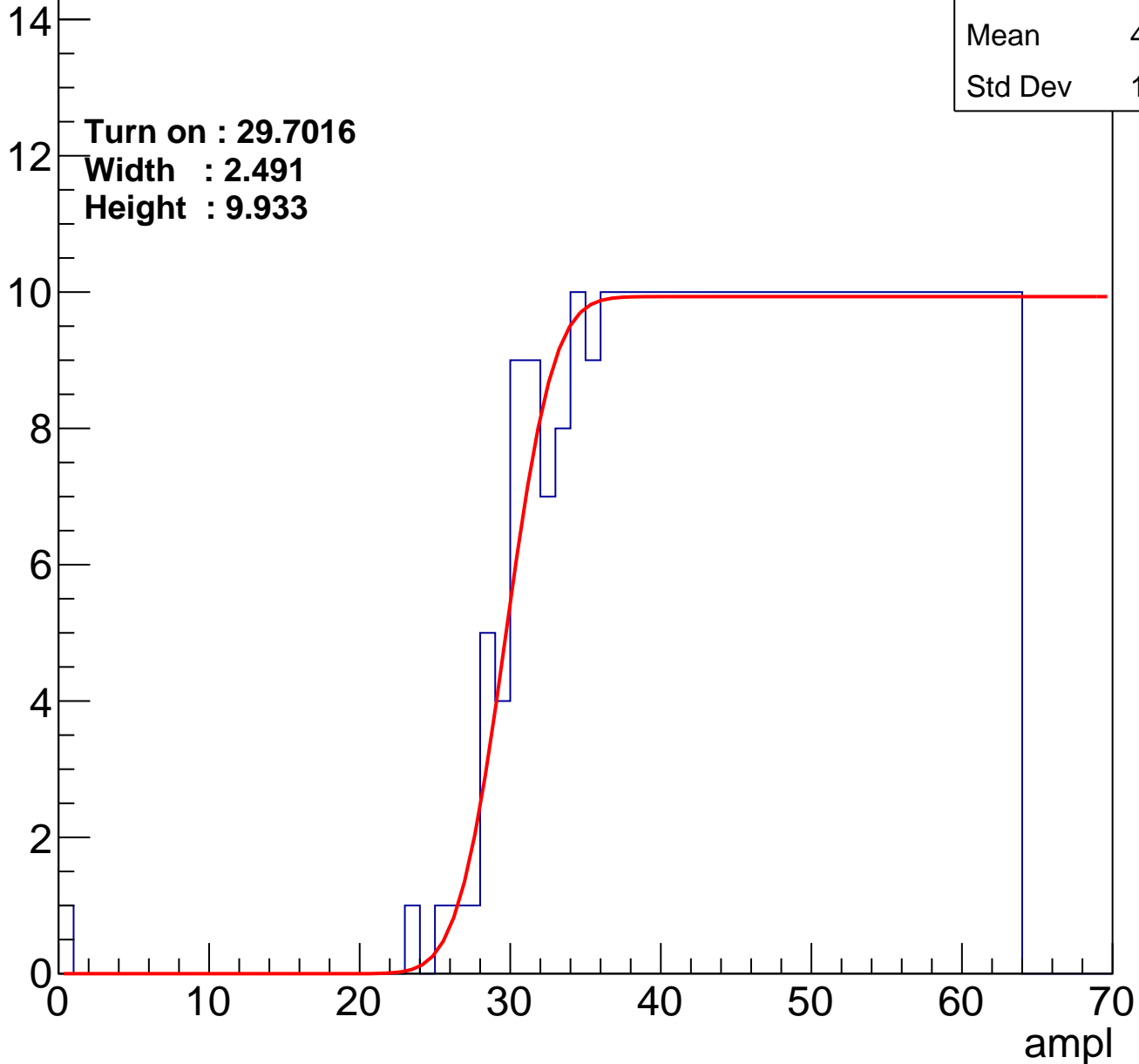
Entries	346
Mean	45.98
Std Dev	10.47

**Turn on : 29.7016**

**Width : 2.491**

**Height : 9.933**

Entry



# B0L000S, U1-ch85

calib\_packv5\_042523\_0143.root, FC#5, port B1

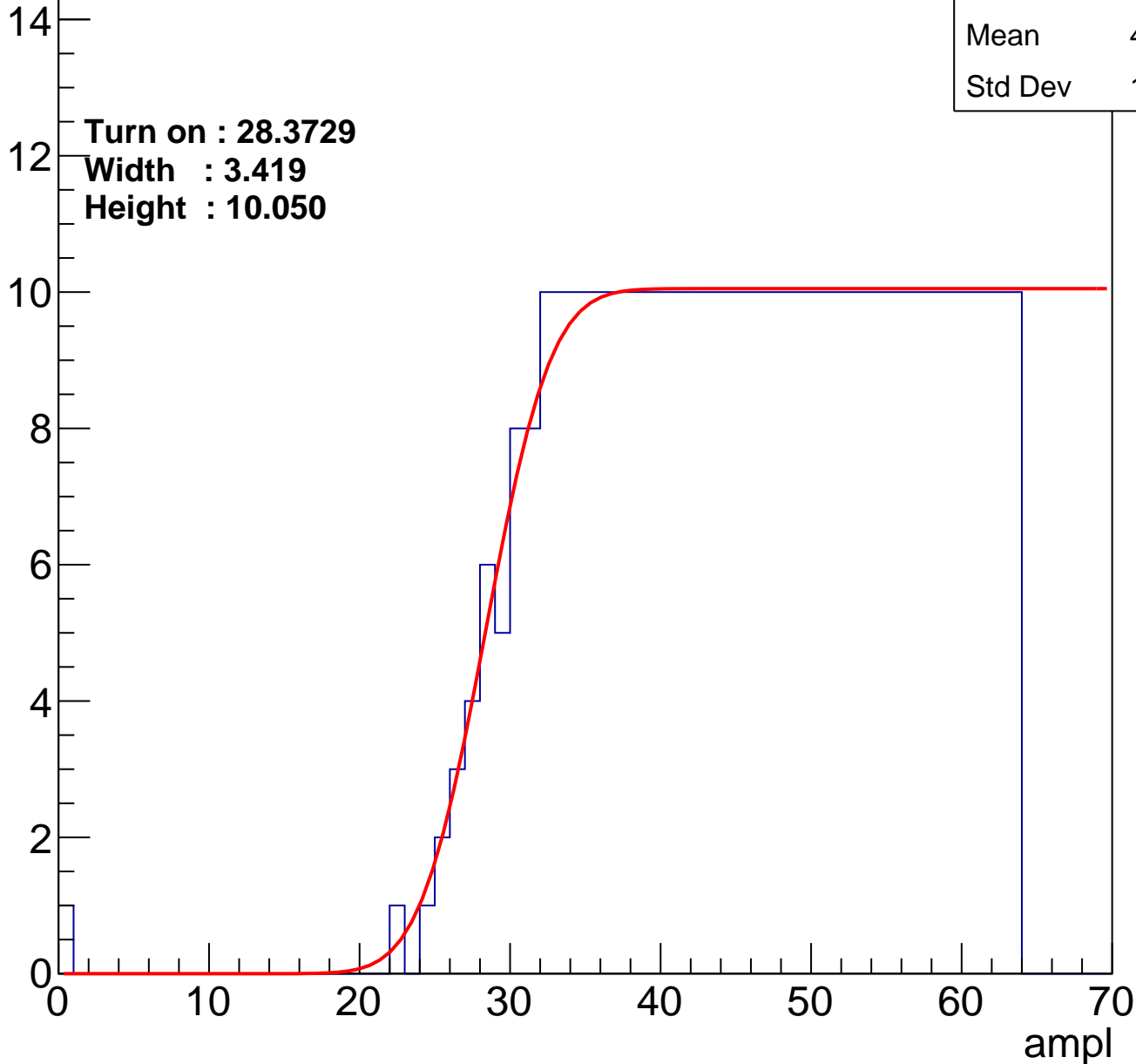
Entry

Entries	359
Mean	45.36
Std Dev	10.79

Turn on : 28.3729

Width : 3.419

Height : 10.050



# B0L000S, U1-ch86

calib\_packv5\_042523\_0143.root, FC#5, port B1

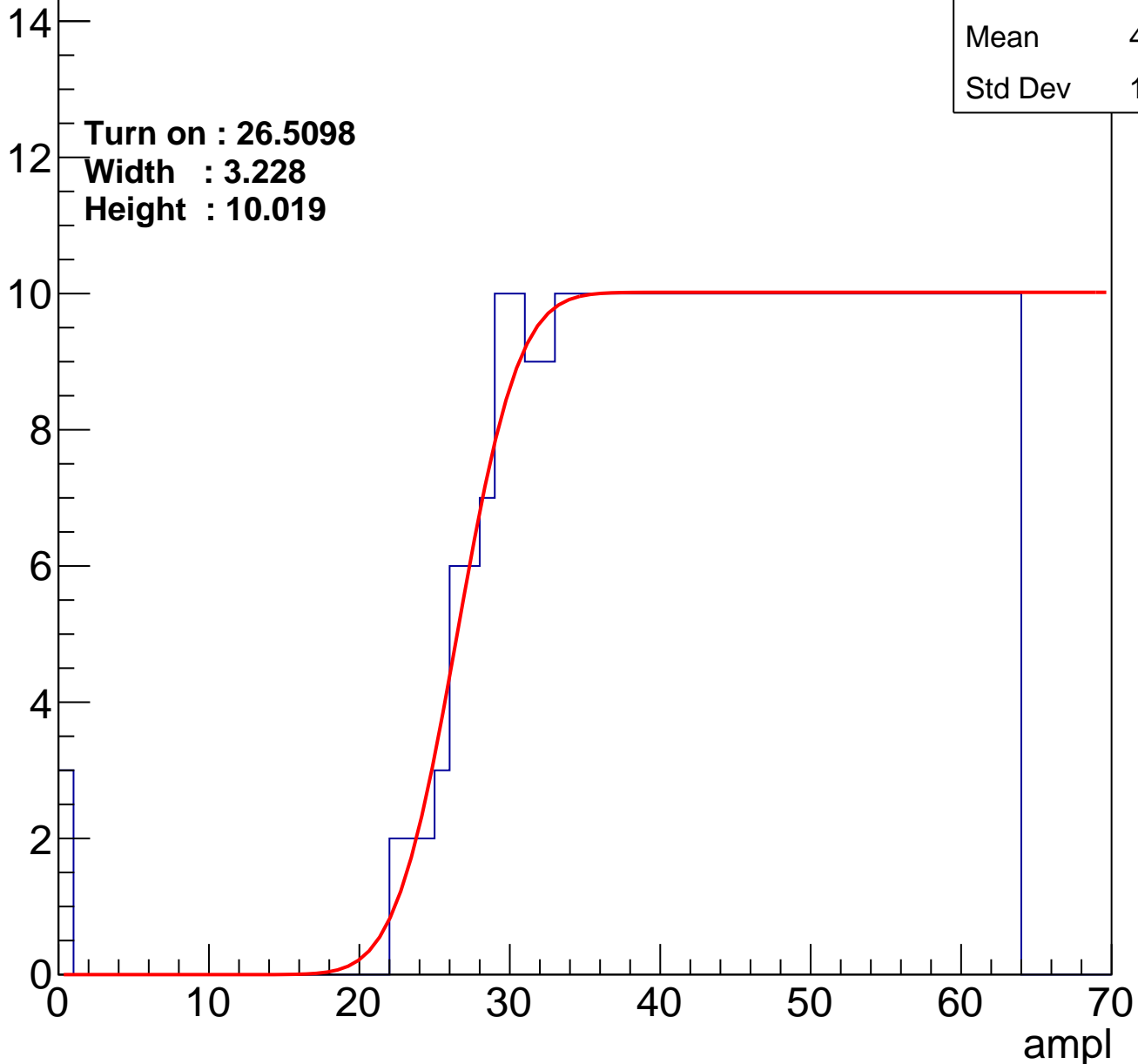
Entries	379
Mean	44.23
Std Dev	11.69

Turn on : 26.5098

Width : 3.228

Height : 10.019

Entry





# B0L000S, U1-ch87

calib\_packv5\_042523\_0143.root, FC#5, port B1

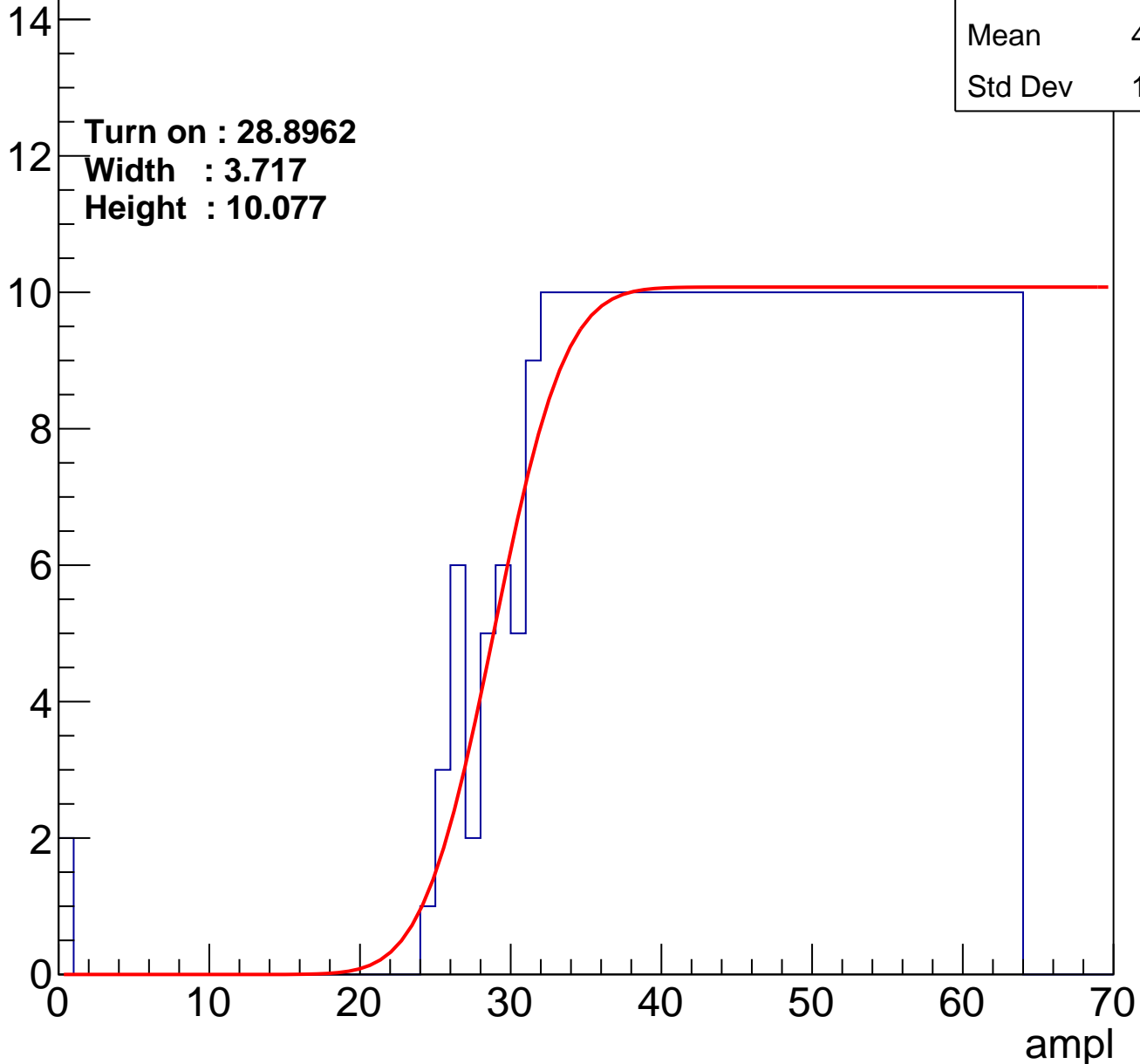
Entries	359
Mean	45.27
Std Dev	11.02

**Turn on : 28.8962**

**Width : 3.717**

**Height : 10.077**

Entry



# B0L000S, U1-ch88

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	362
Mean	45.09
Std Dev	11.24

Turn on : 28.9952

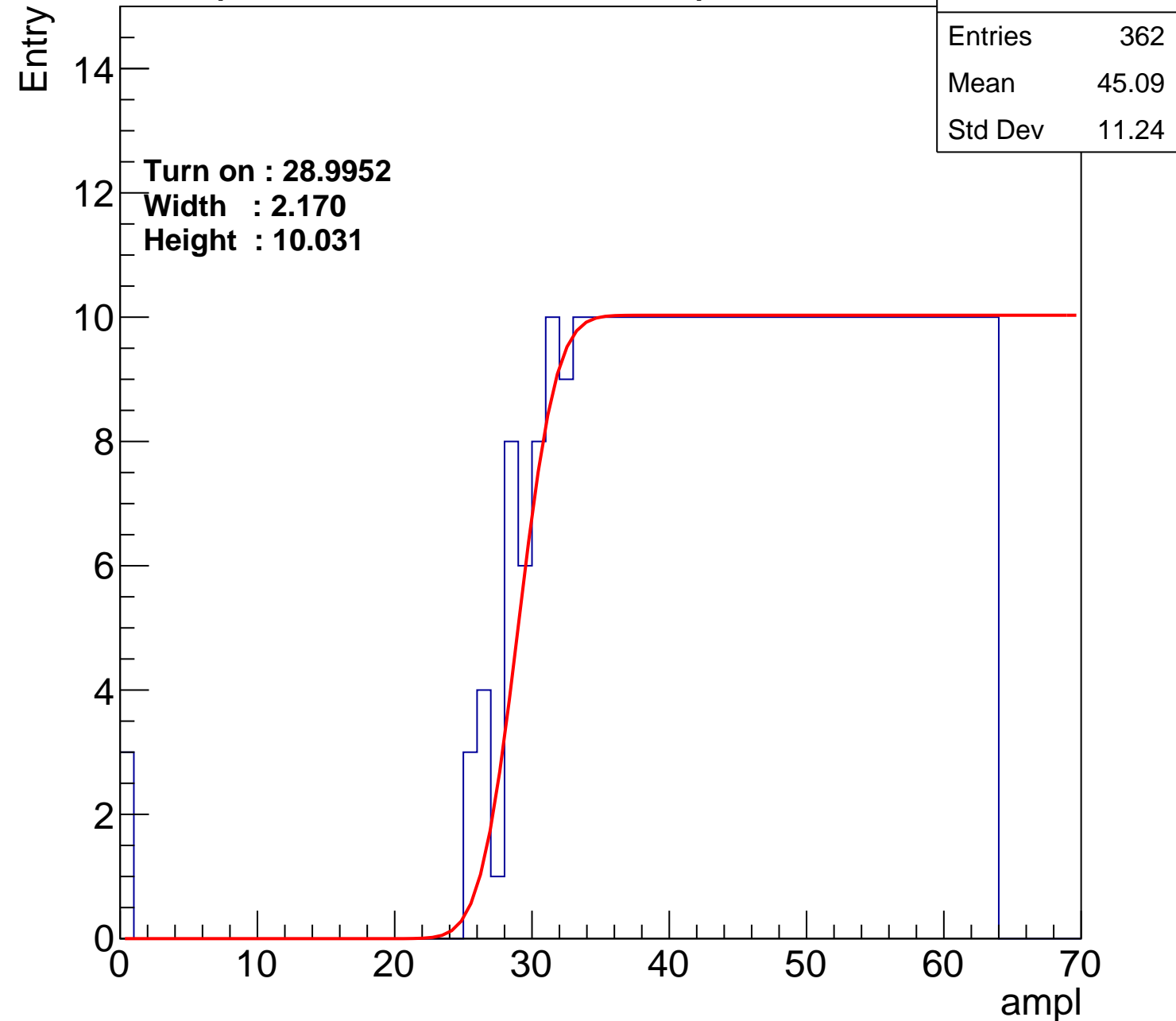
Width : 2.170

Height : 10.031

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch89

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	369
Mean	44.88
Std Dev	11.03

Turn on : 27.1752

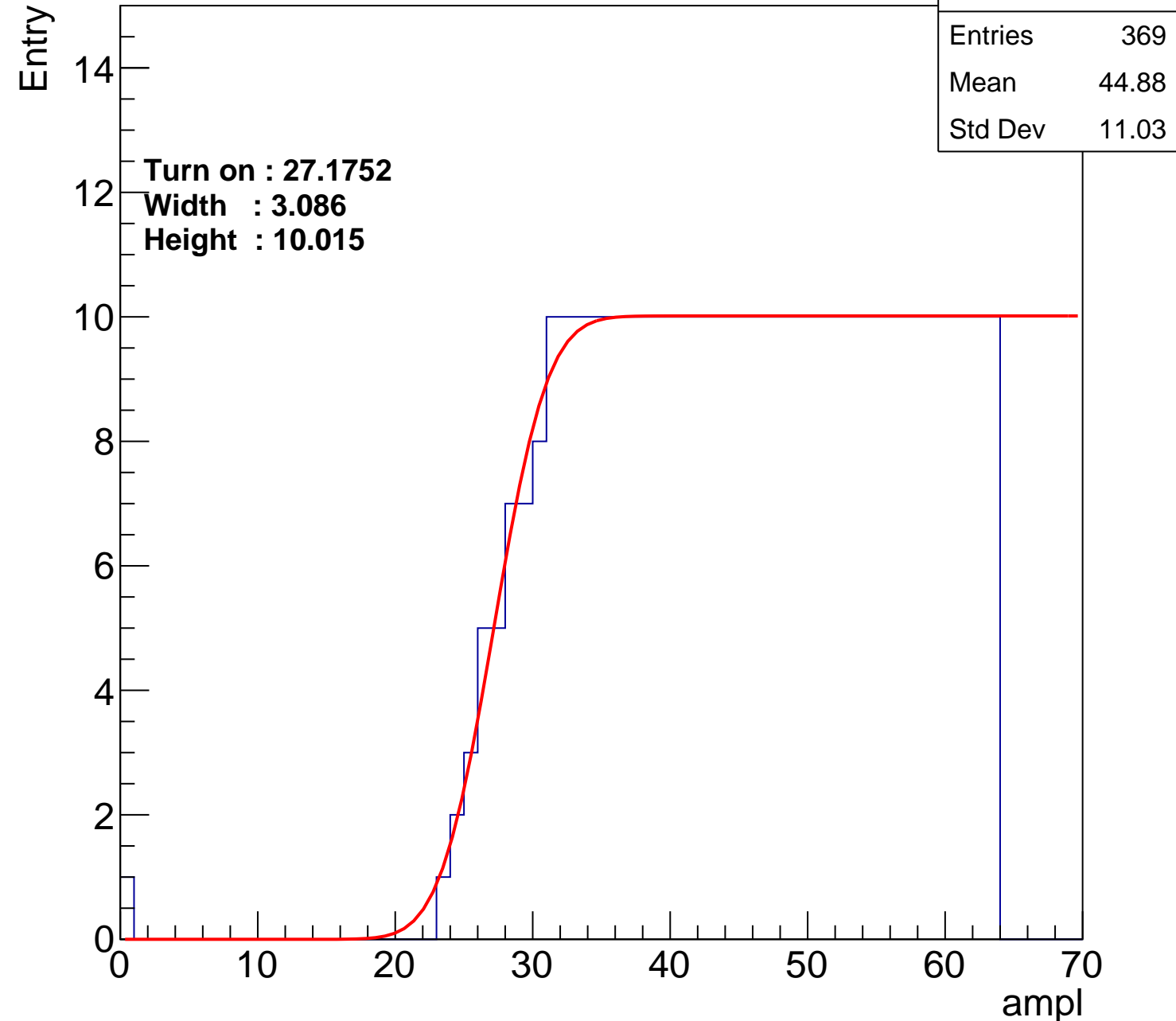
Width : 3.086

Height : 10.015

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch90

calib\_packv5\_042523\_0143.root, FC#5, port B1

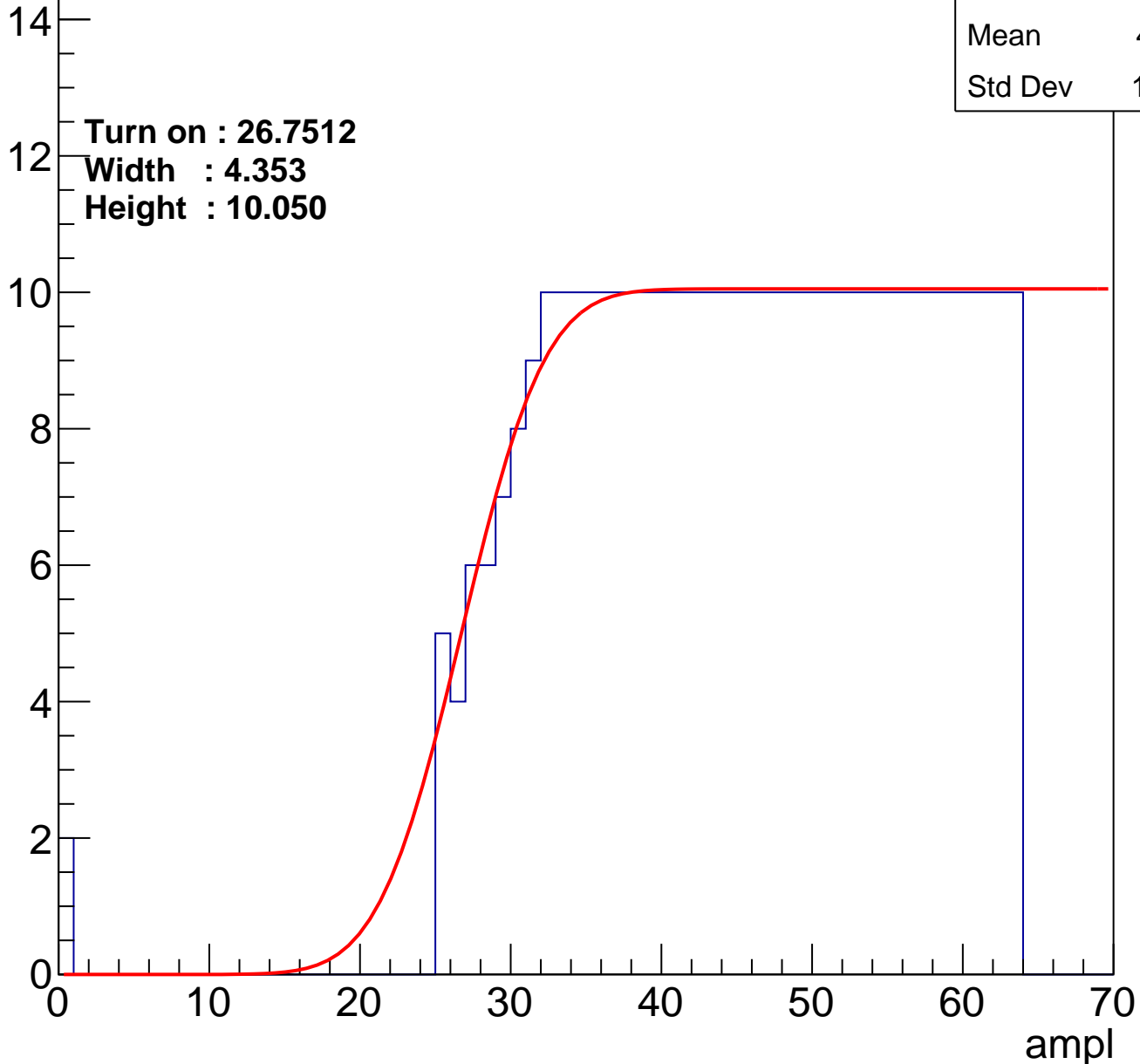
Entries	367
Mean	44.91
Std Dev	11.17

Turn on : 26.7512

Width : 4.353

Height : 10.050

Entry



# B0L000S, U1-ch91

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	397
Mean	43.32
Std Dev	12.25

**Turn on : 25.1383**

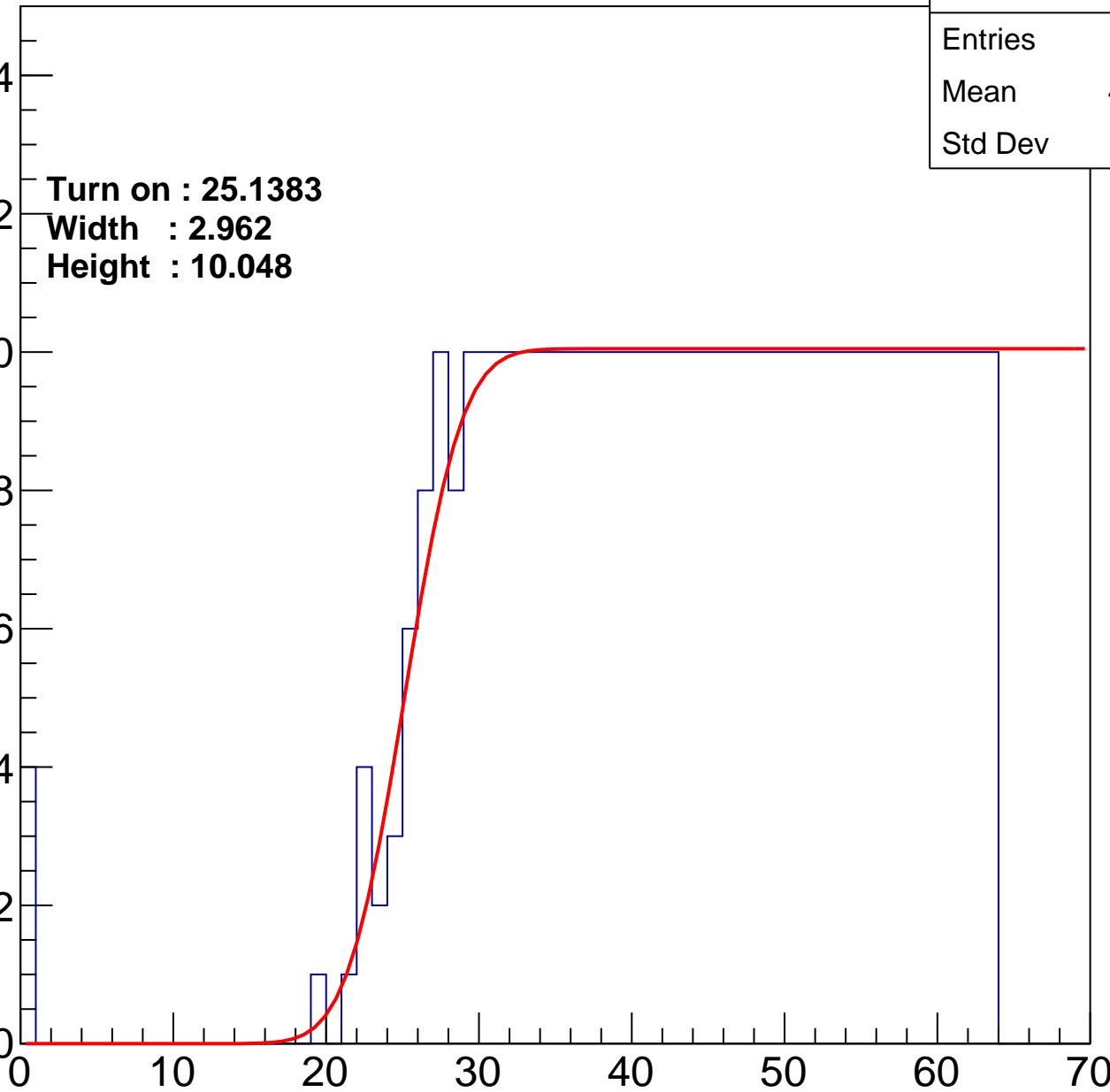
**Width : 2.962**

**Height : 10.048**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch92

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	383
Mean	44.2
Std Dev	11.38

**Turn on : 26.0457**

**Width : 2.741**

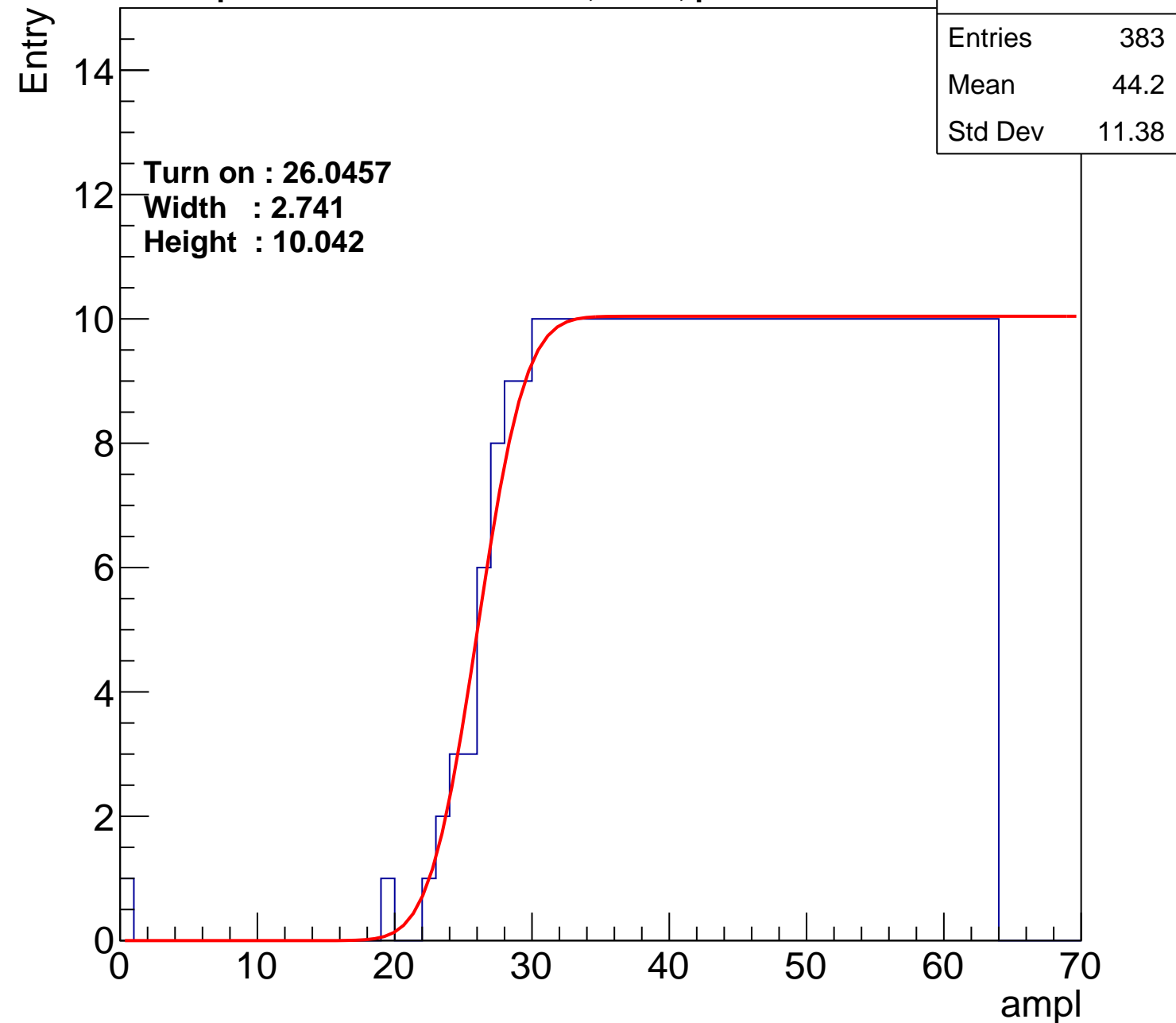
**Height : 10.042**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L000S, U1-ch93

calib\_packv5\_042523\_0143.root, FC#5, port B1

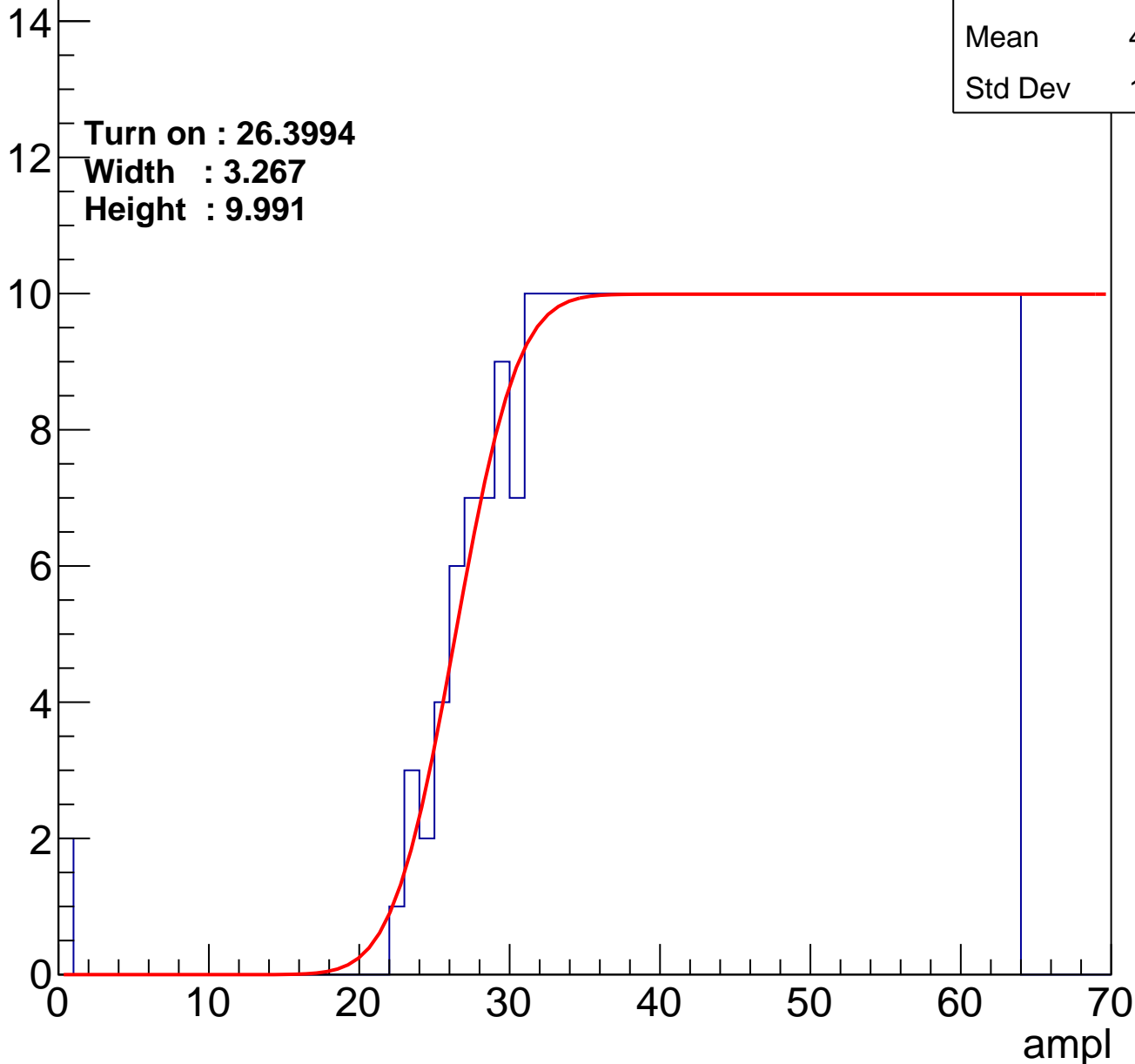
Entry

Entries	378
Mean	44.34
Std Dev	11.49

Turn on : 26.3994

Width : 3.267

Height : 9.991



# B0L000S, U1-ch94

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	372
Mean	44.64
Std Dev	11.33

Turn on : 27.0578

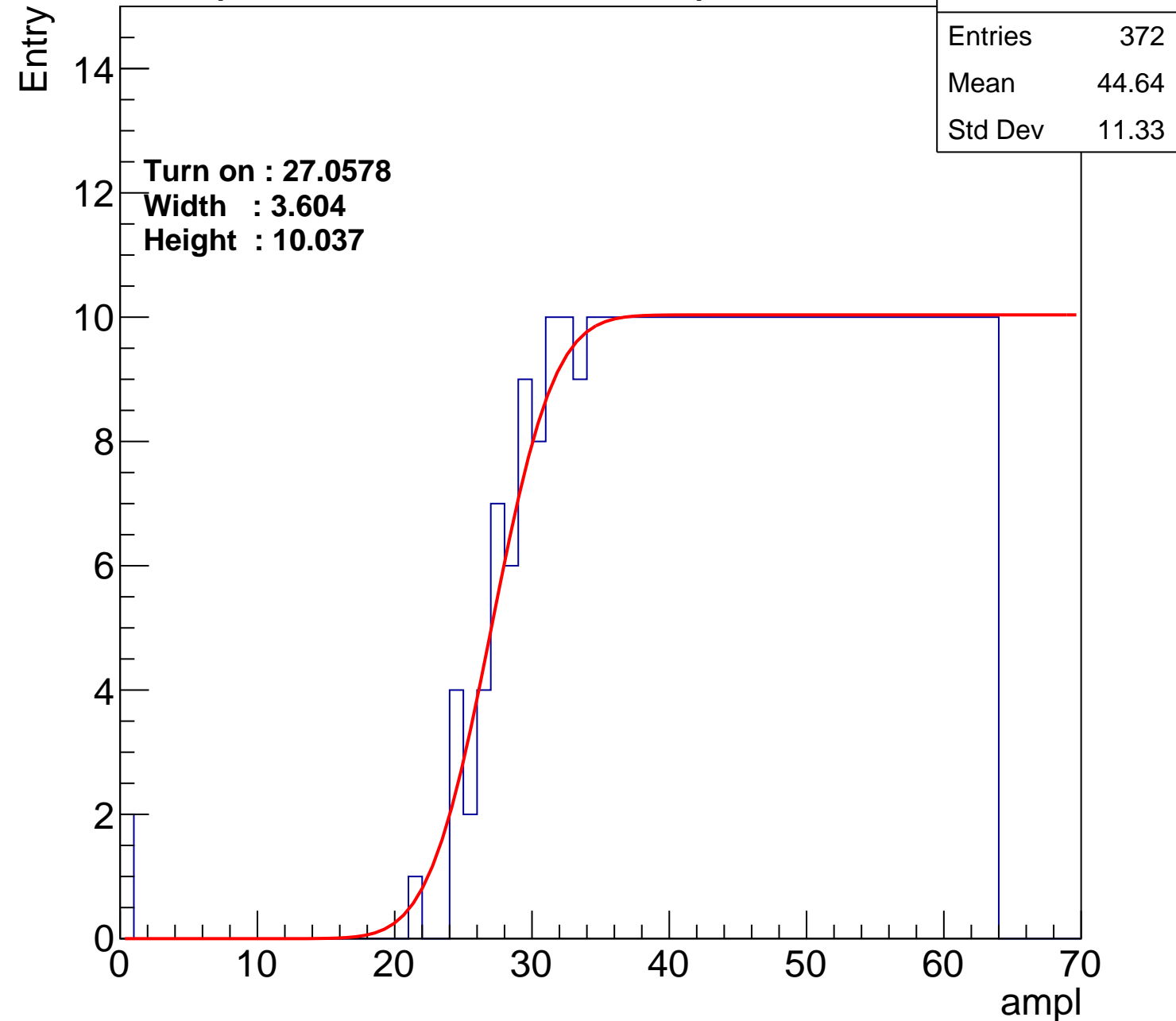
Width : 3.604

Height : 10.037

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L000S, U1-ch95

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	362
Mean	44.9
Std Dev	11.7

Turn on : 28.1711

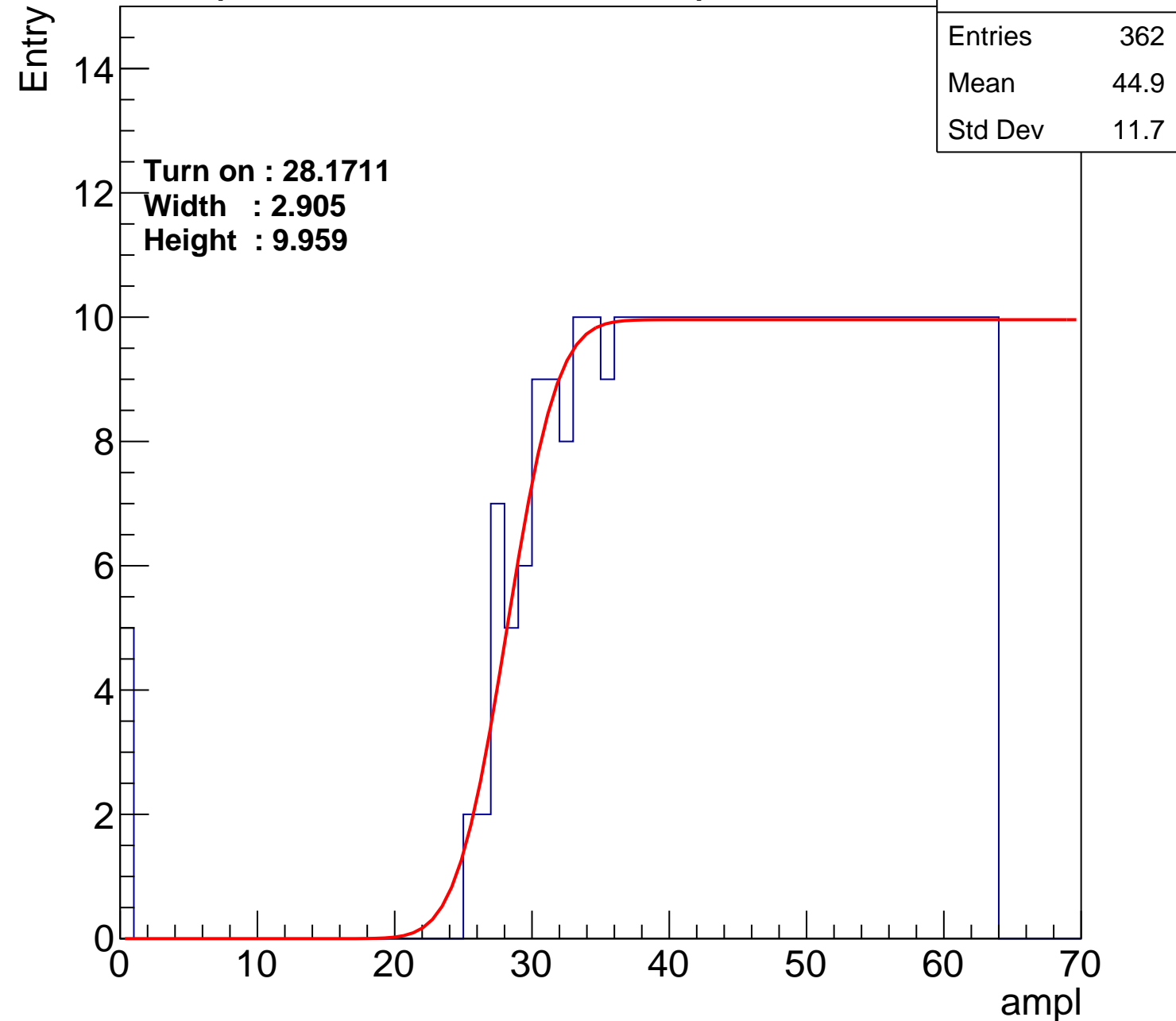
Width : 2.905

Height : 9.959

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch96

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	371
Mean	44.62
Std Dev	11.5

**Turn on : 28.1538**

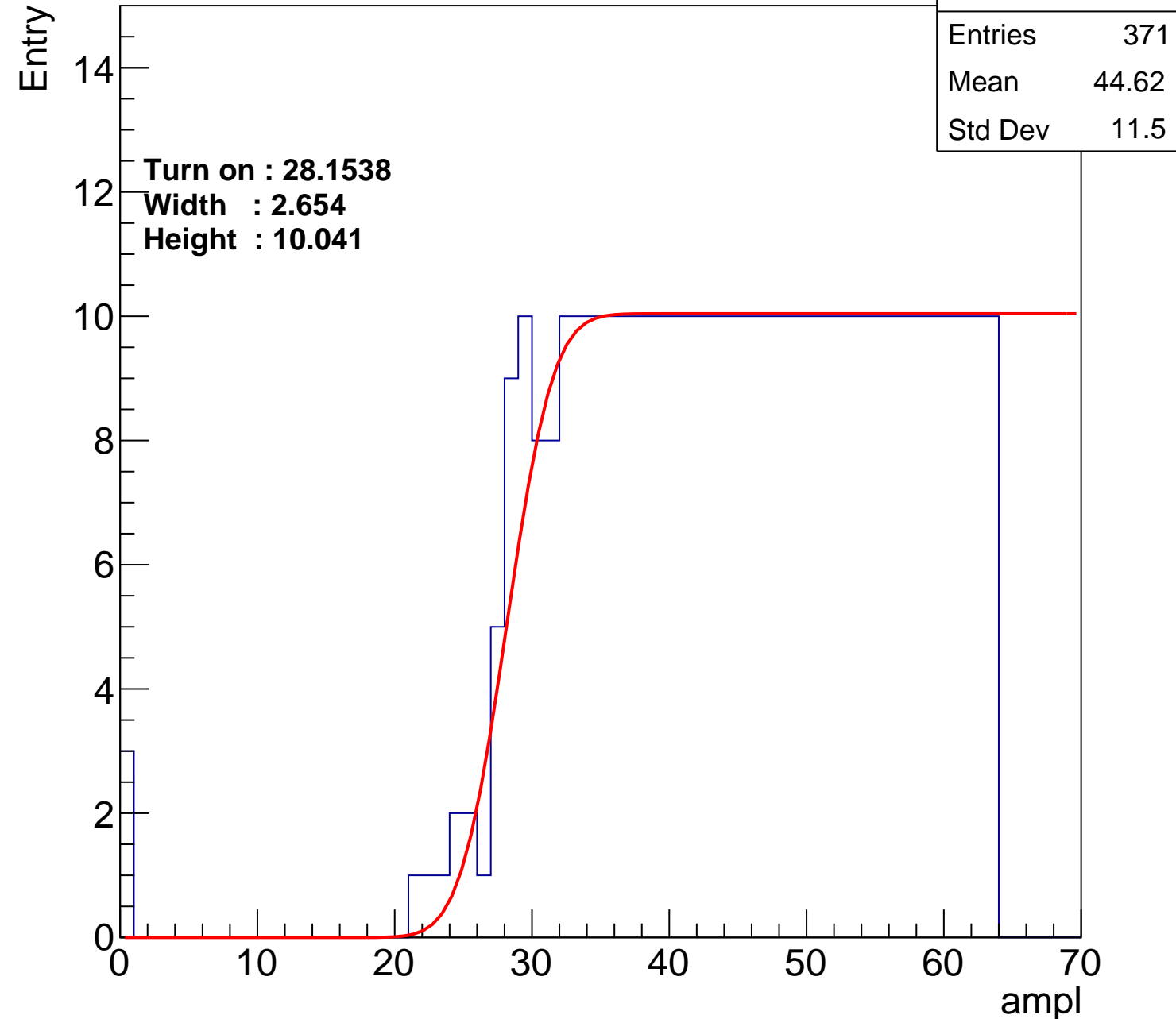
**Width : 2.654**

**Height : 10.041**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch97

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	397
Mean	43.29
Std Dev	12.29

Turn on : 24.8962

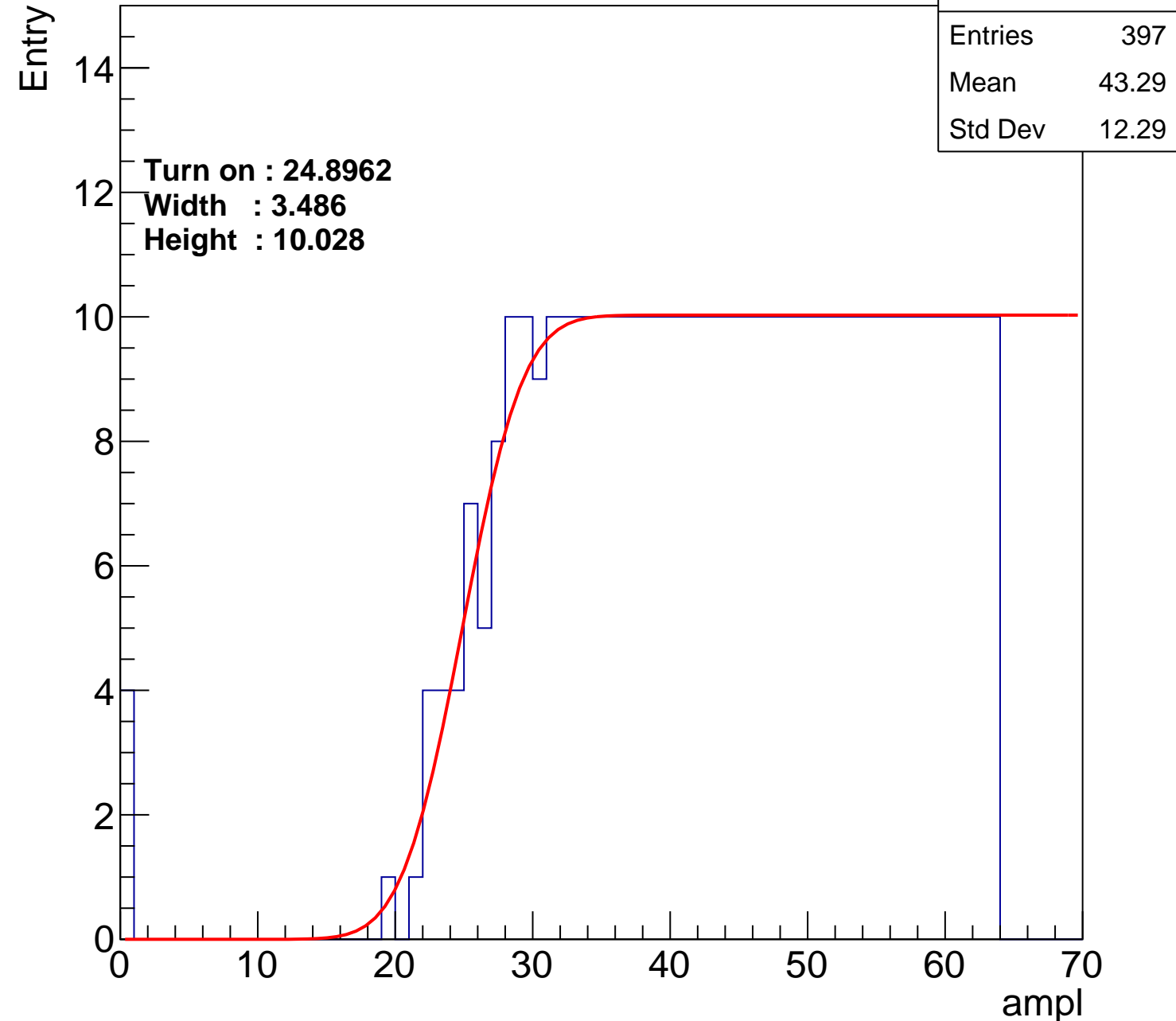
Width : 3.486

Height : 10.028

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



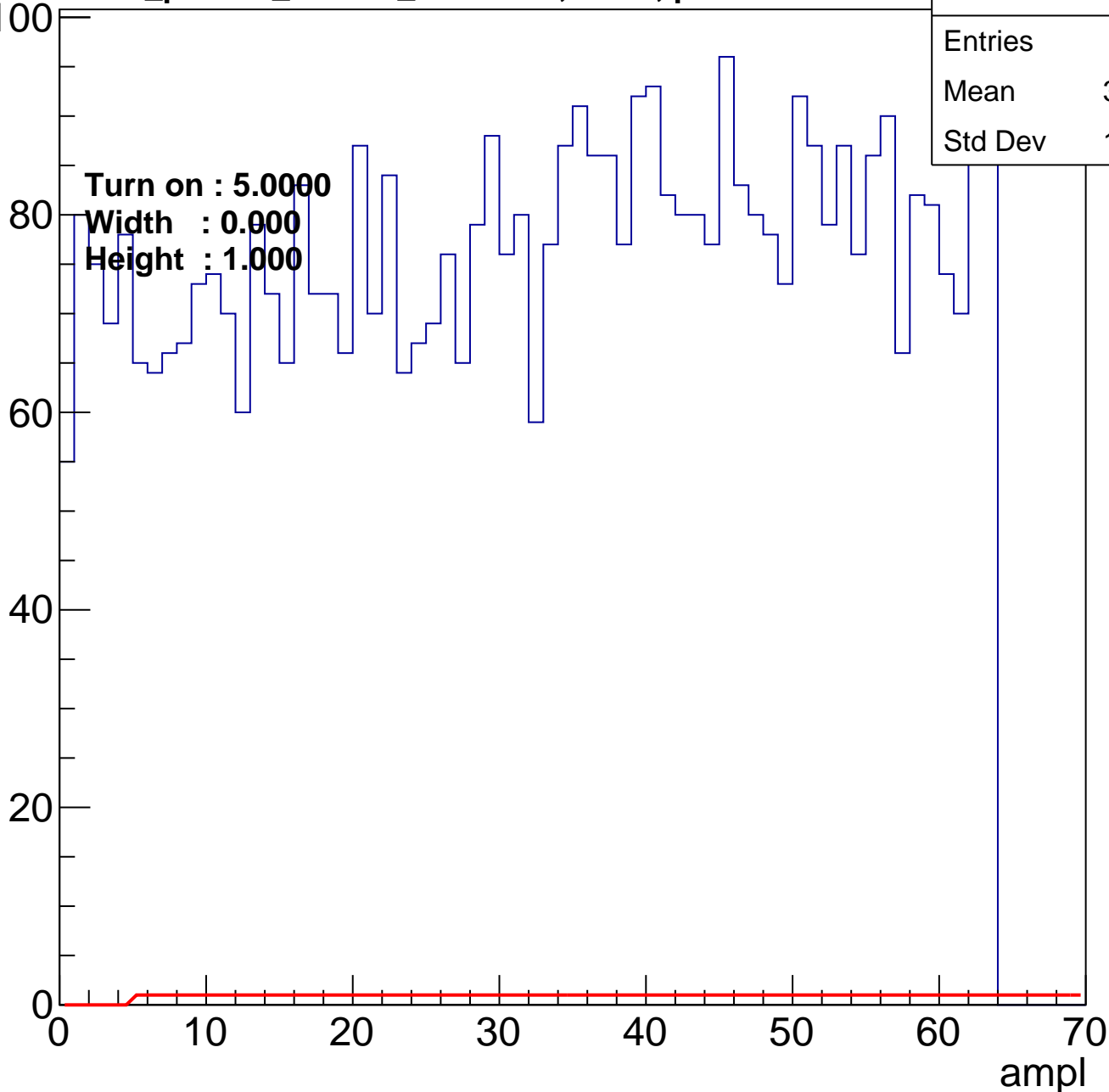
# B0L000S, U1-ch98

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entry

Entries	4934
Mean	32.66
Std Dev	18.27

Turn on : 5.0000  
Width : 0.000  
Height : 1.000



# B0L000S, U1-ch99

calib\_packv5\_042523\_0143.root, FC#5, port B1

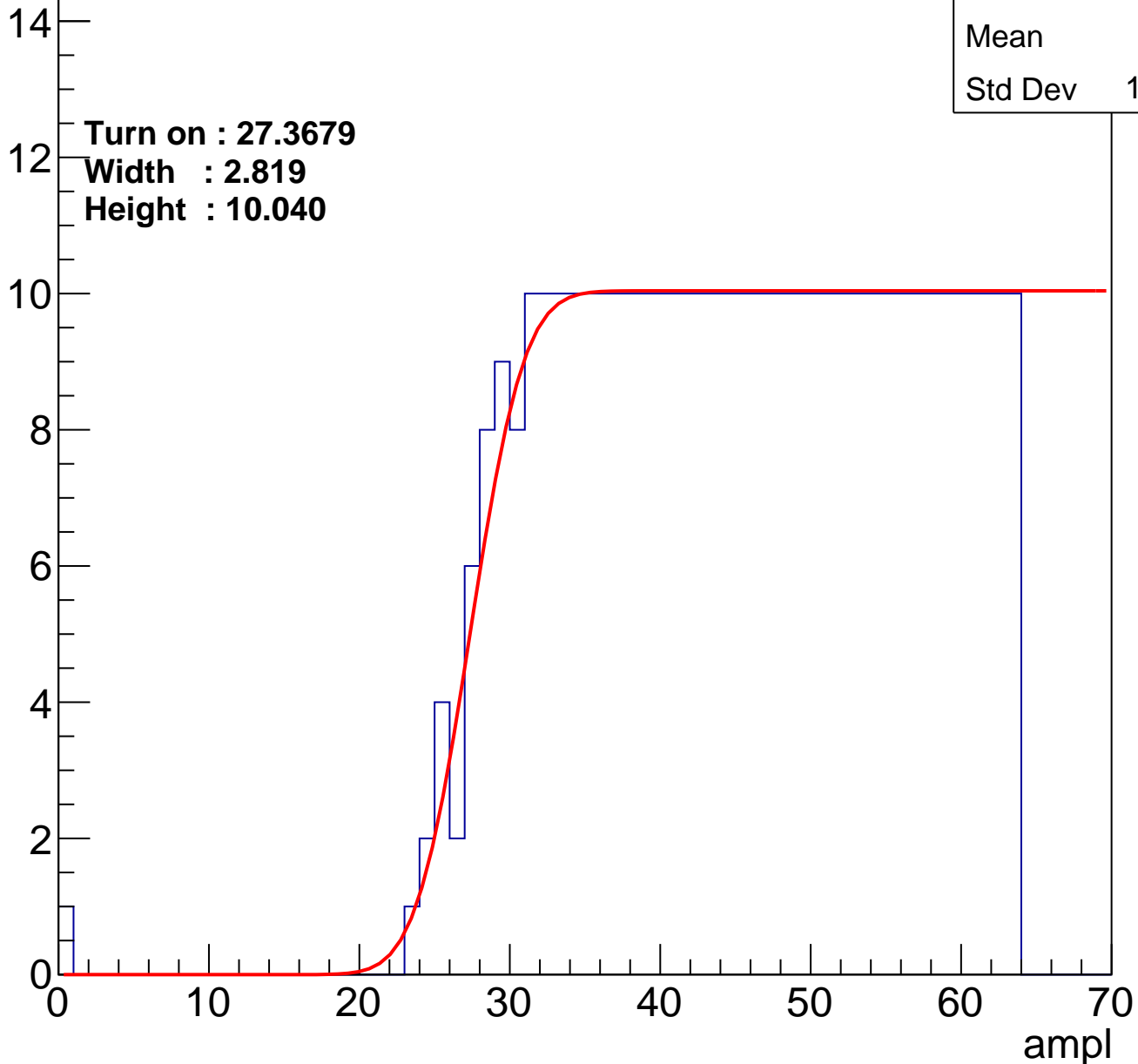
Entries	371
Mean	44.8
Std Dev	11.05

Turn on : 27.3679

Width : 2.819

Height : 10.040

Entry



# B0L000S, U1-ch100

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	376
Mean	44.34
Std Dev	11.77

**Turn on : 27.2088**

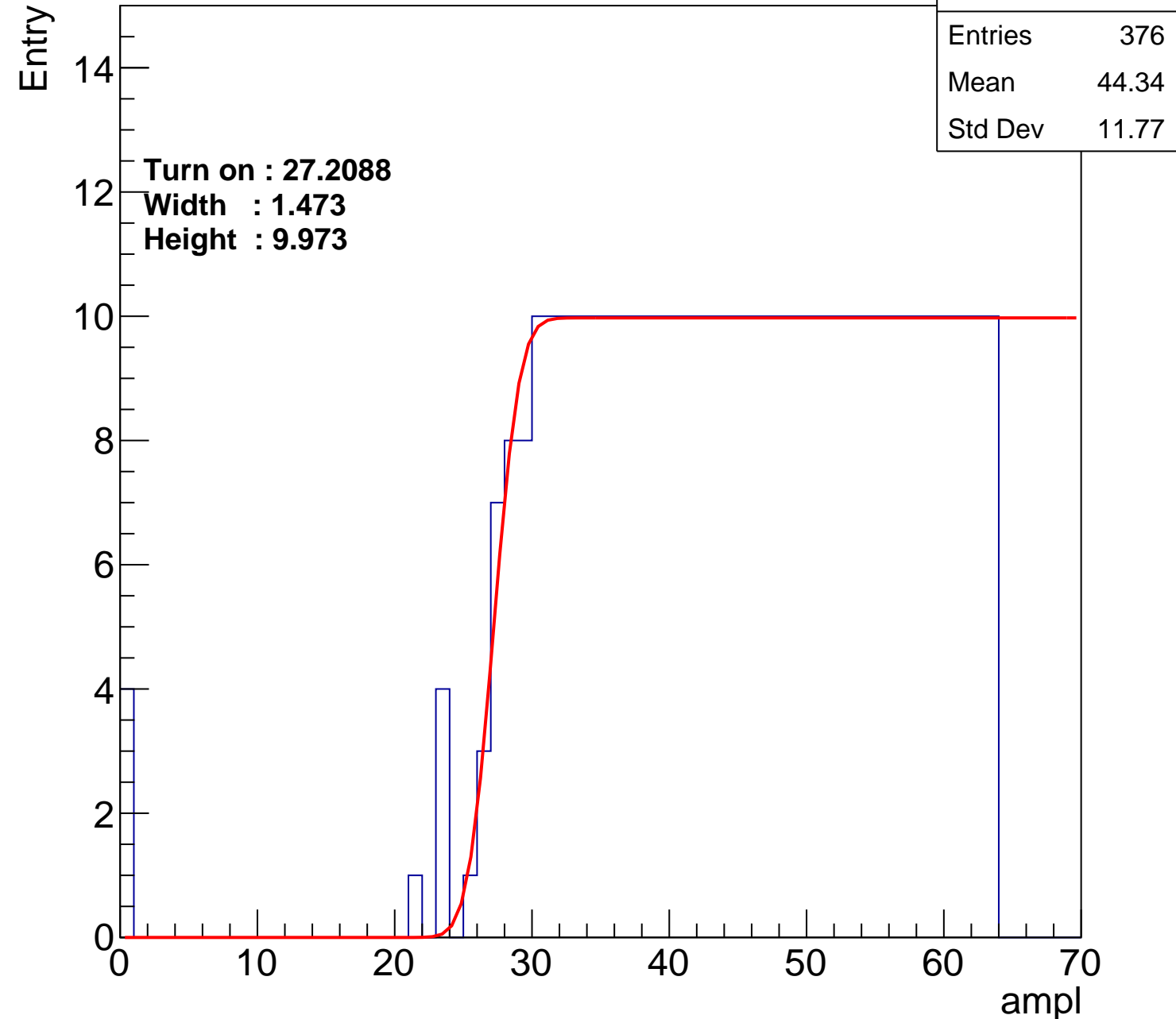
**Width : 1.473**

**Height : 9.973**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch101

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	369
Mean	44.86
Std Dev	11.05

Turn on : 27.4611

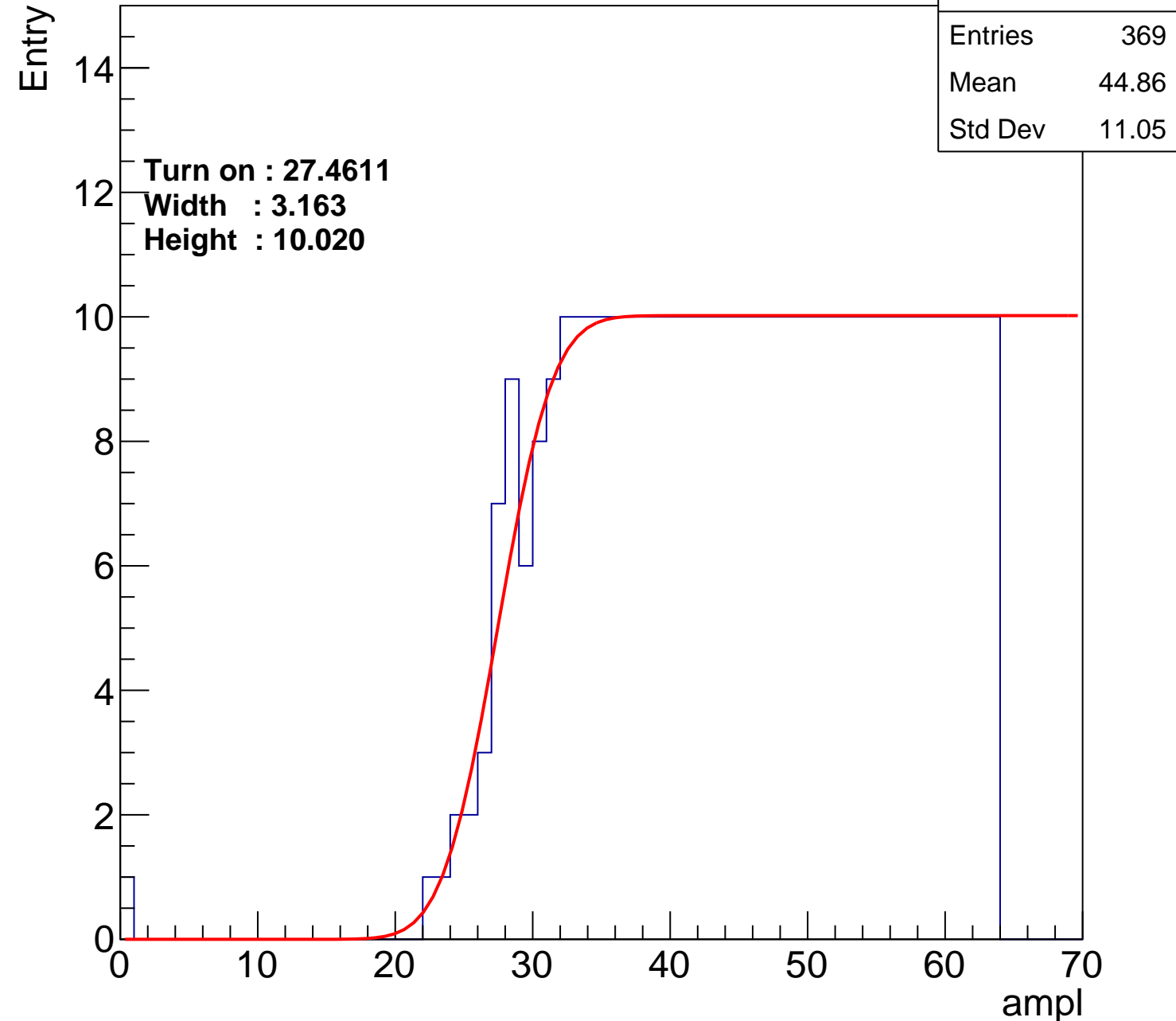
Width : 3.163

Height : 10.020

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch102

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	374
Mean	44.63
Std Dev	11.15

Turn on : 26.6871

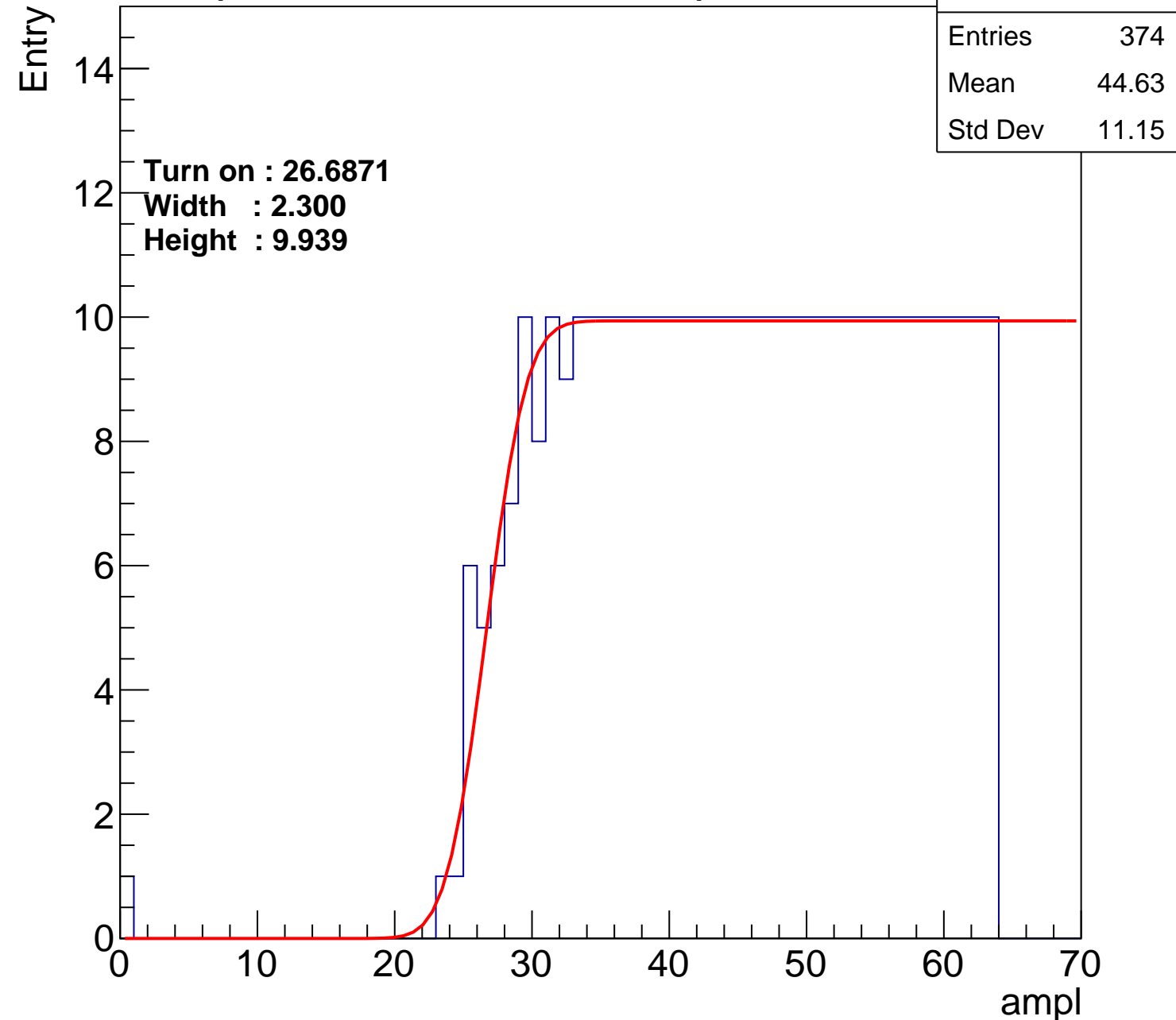
Width : 2.300

Height : 9.939

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L000S, U1-ch103

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	358
Mean	45.27
Std Dev	11.06

Turn on : 28.8472

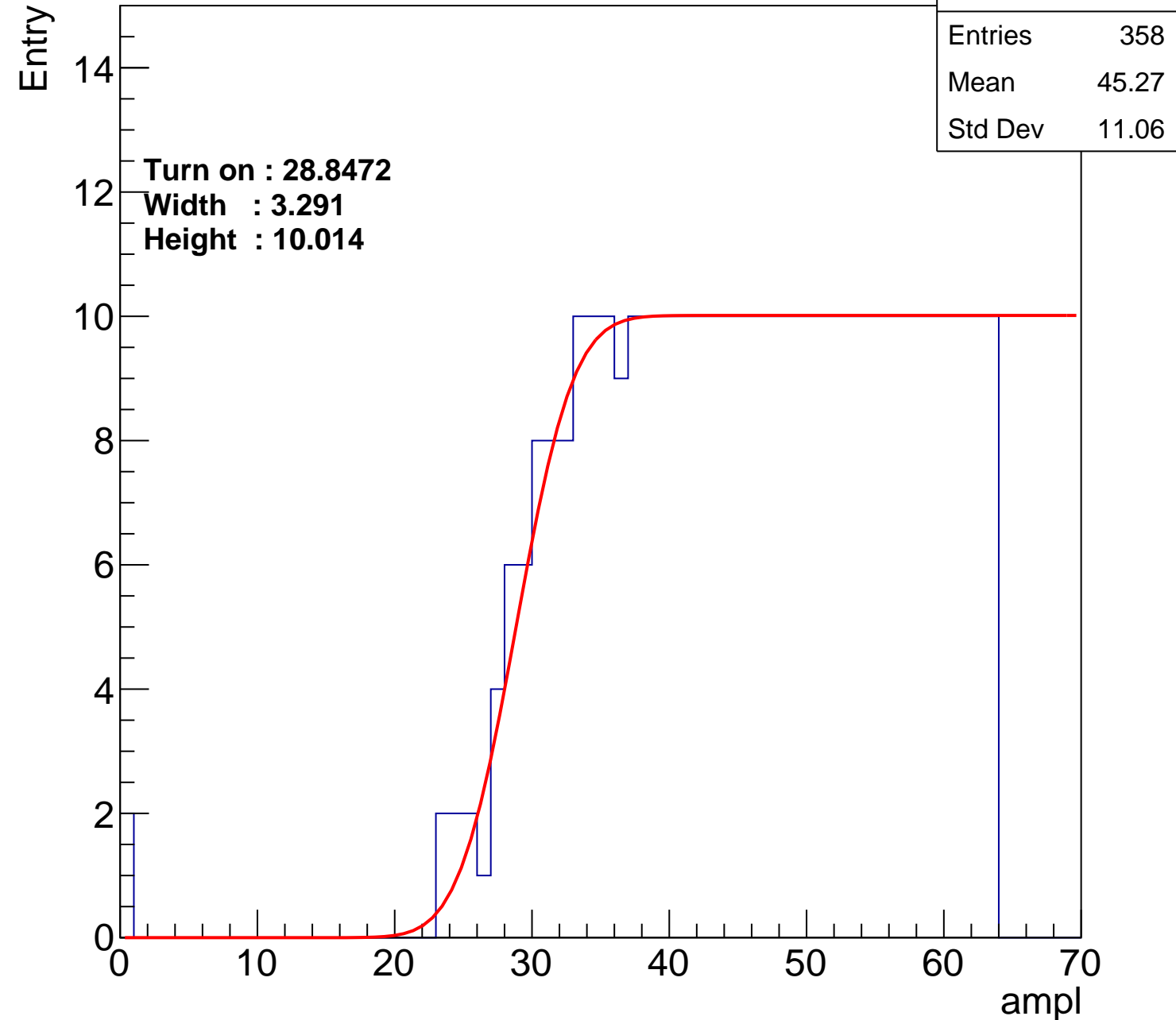
Width : 3.291

Height : 10.014

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch104

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	387
Mean	43.58
Std Dev	12.54

Turn on : 26.0320

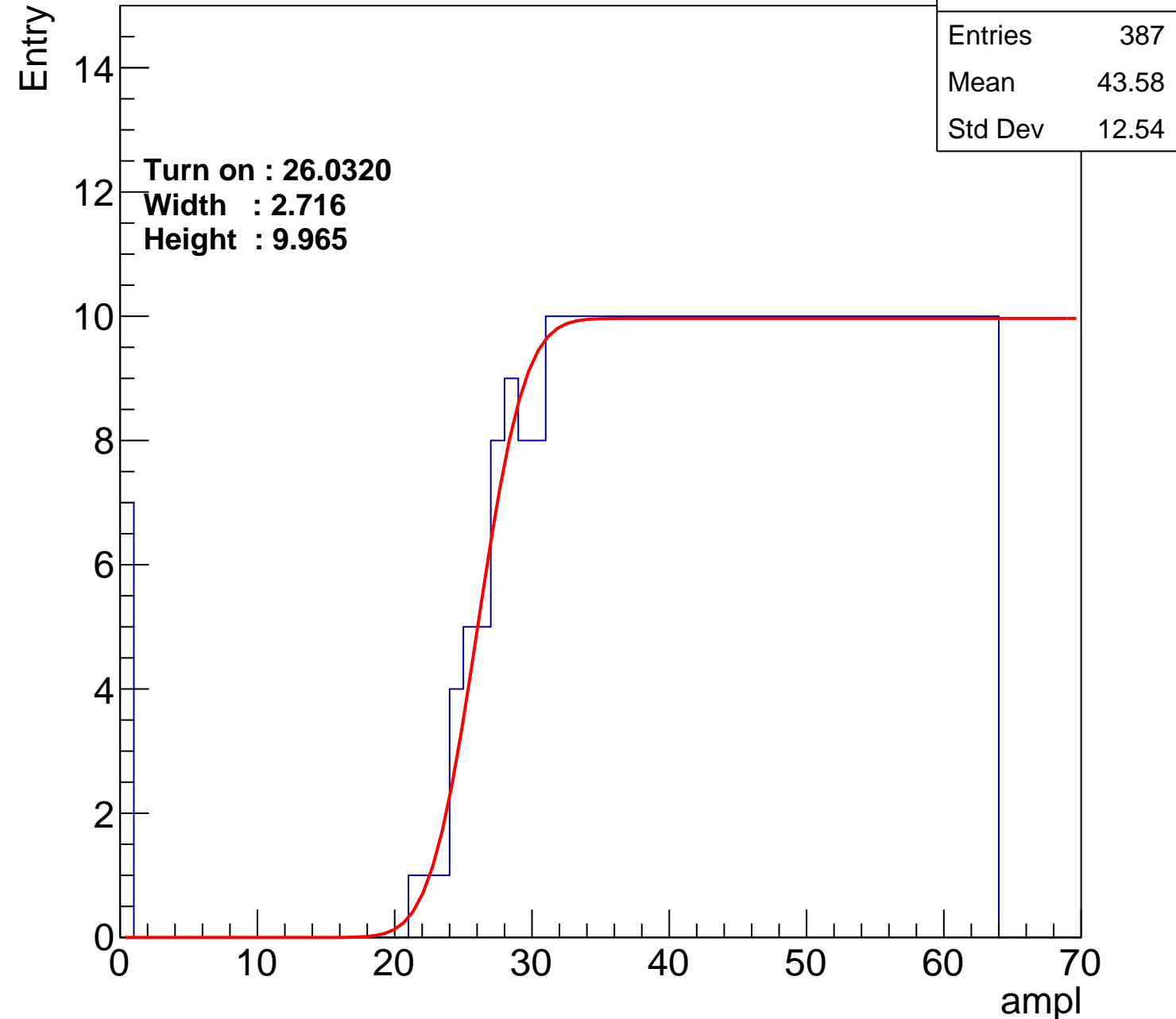
Width : 2.716

Height : 9.965

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch105

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	366
Mean	44.81
Std Dev	11.55

**Turn on : 27.7849**

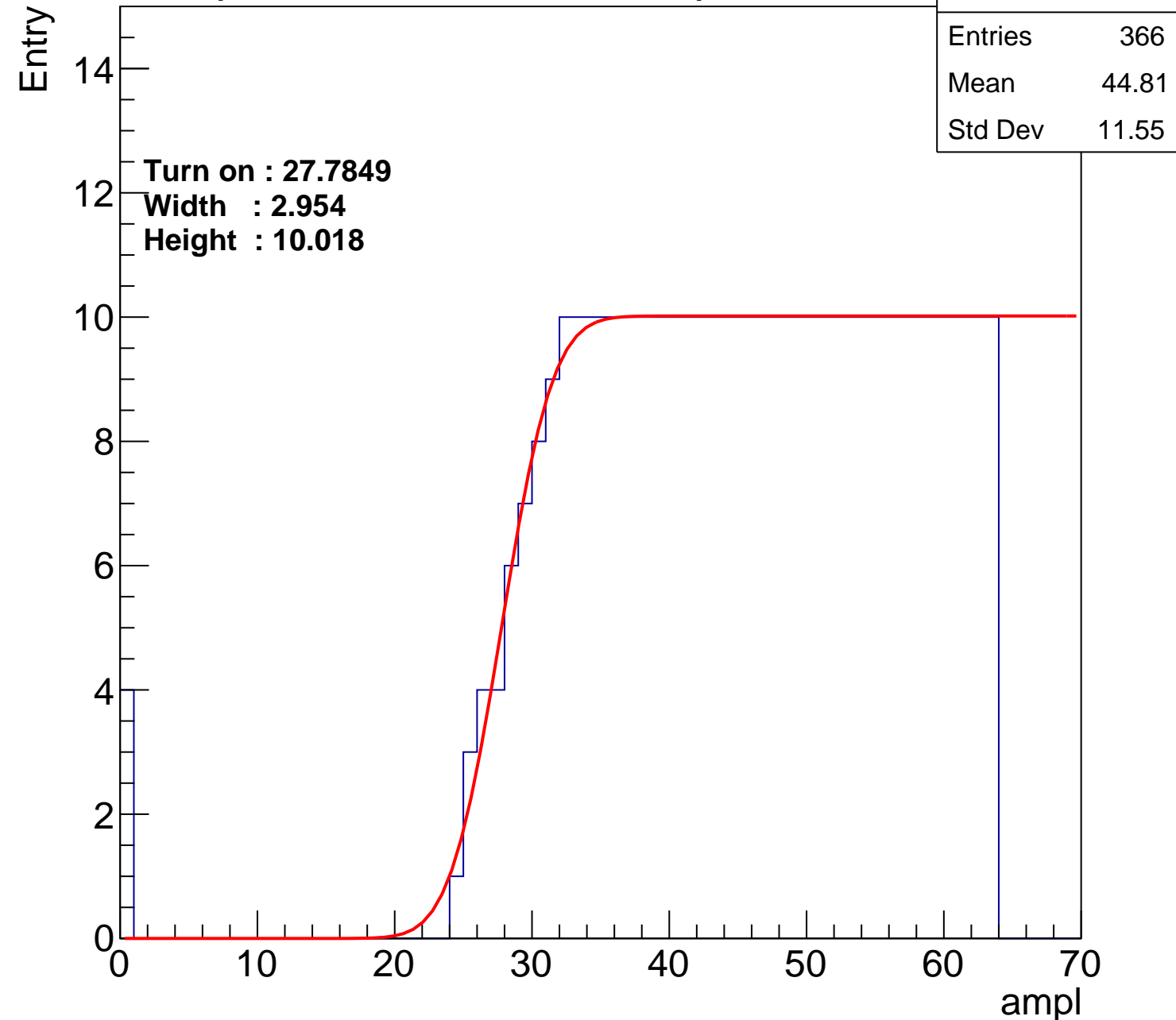
**Width : 2.954**

**Height : 10.018**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch106

calib\_packv5\_042523\_0143.root, FC#5, port B1

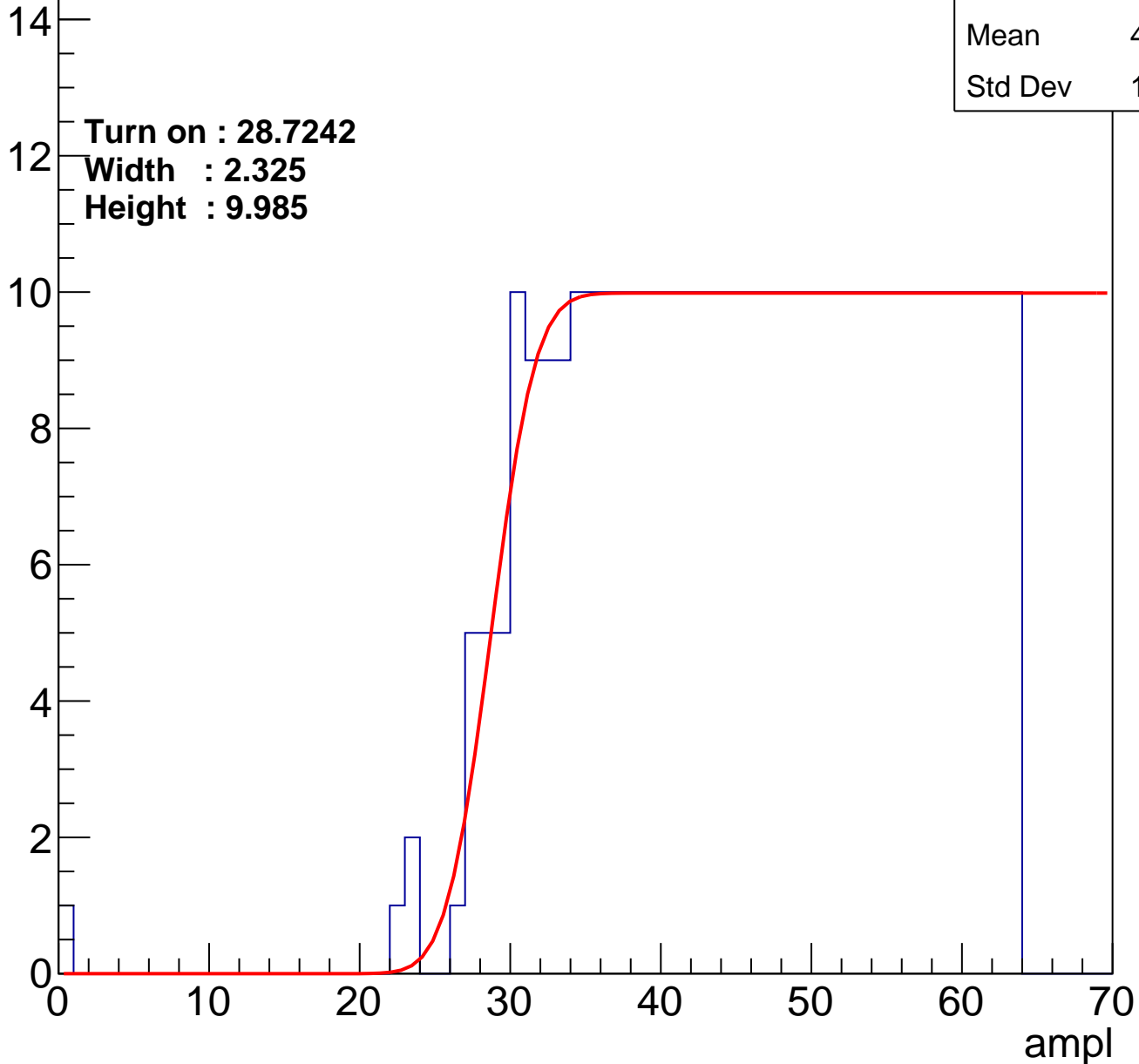
Entries	357
Mean	45.46
Std Dev	10.73

**Turn on : 28.7242**

**Width : 2.325**

**Height : 9.985**

Entry



# B0L000S, U1-ch107

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	365
Mean	44.87
Std Dev	11.42

Turn on : 27.9533

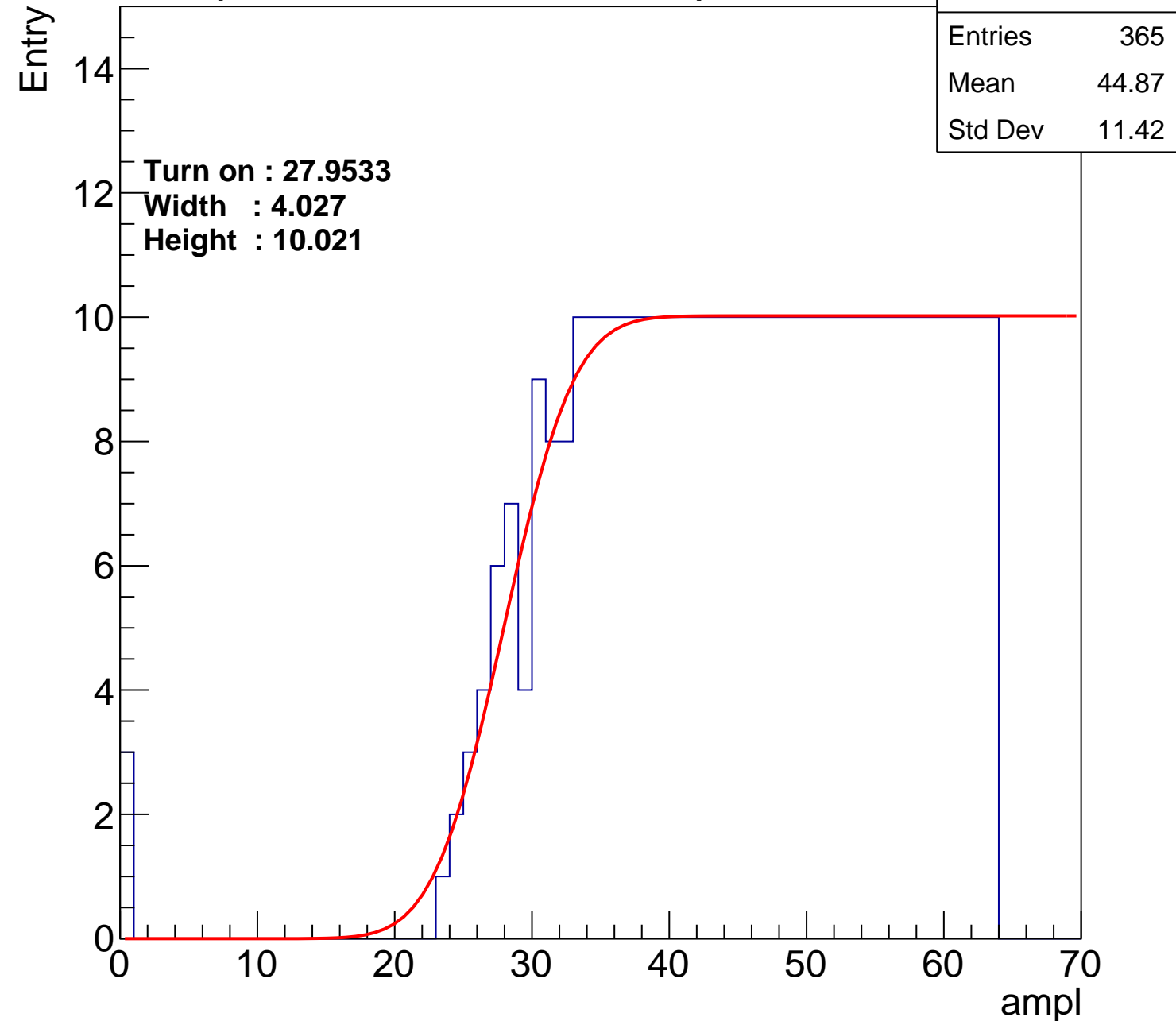
Width : 4.027

Height : 10.021

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch108

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	378
Mean	44.34
Std Dev	11.51

Turn on : 26.5793

Width : 3.558

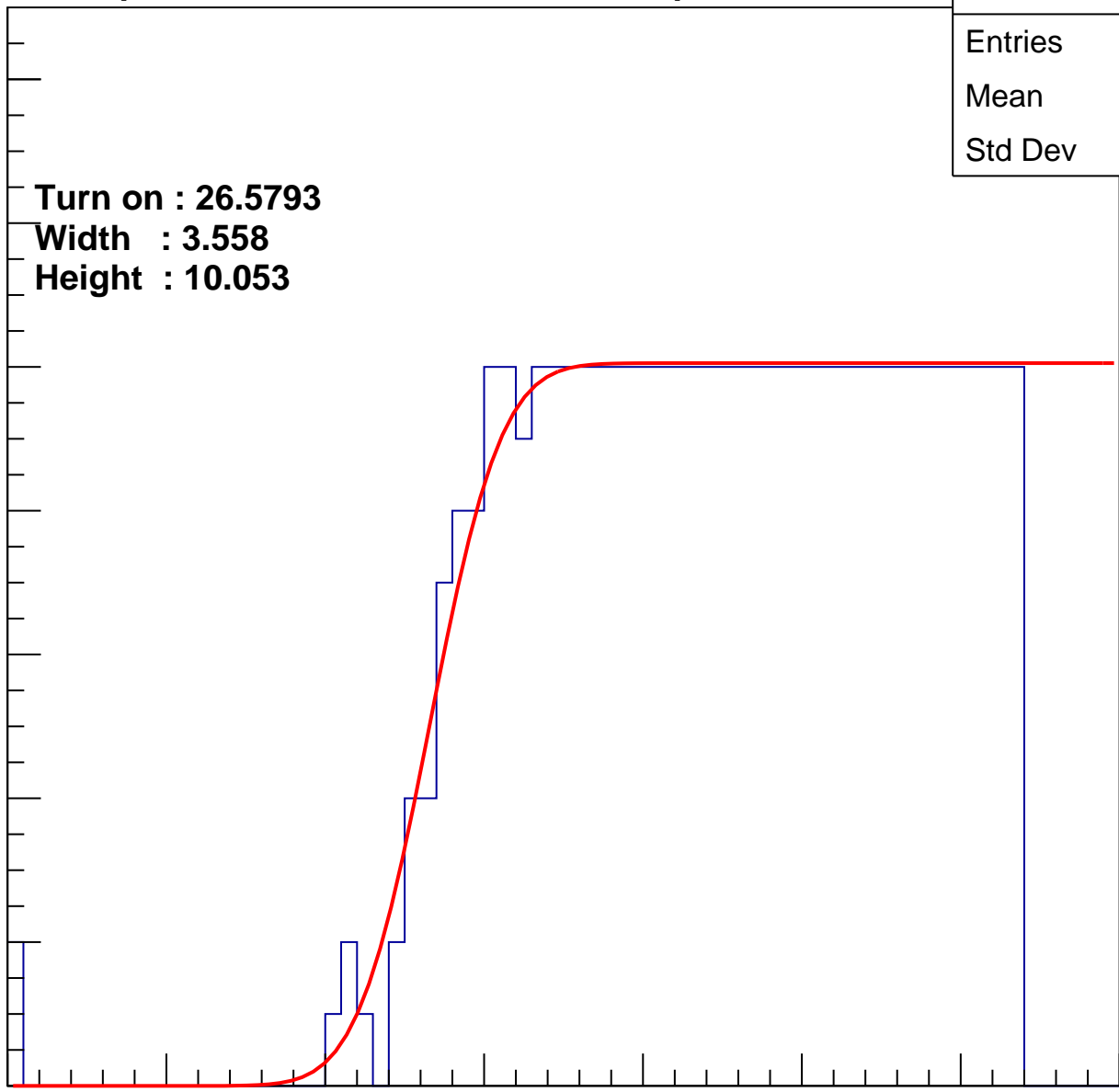
Height : 10.053

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

0 10 20 30 40 50 60 70



# B0L000S, U1-ch109

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	370
Mean	44.85
Std Dev	11.02

Turn on : 27.4938

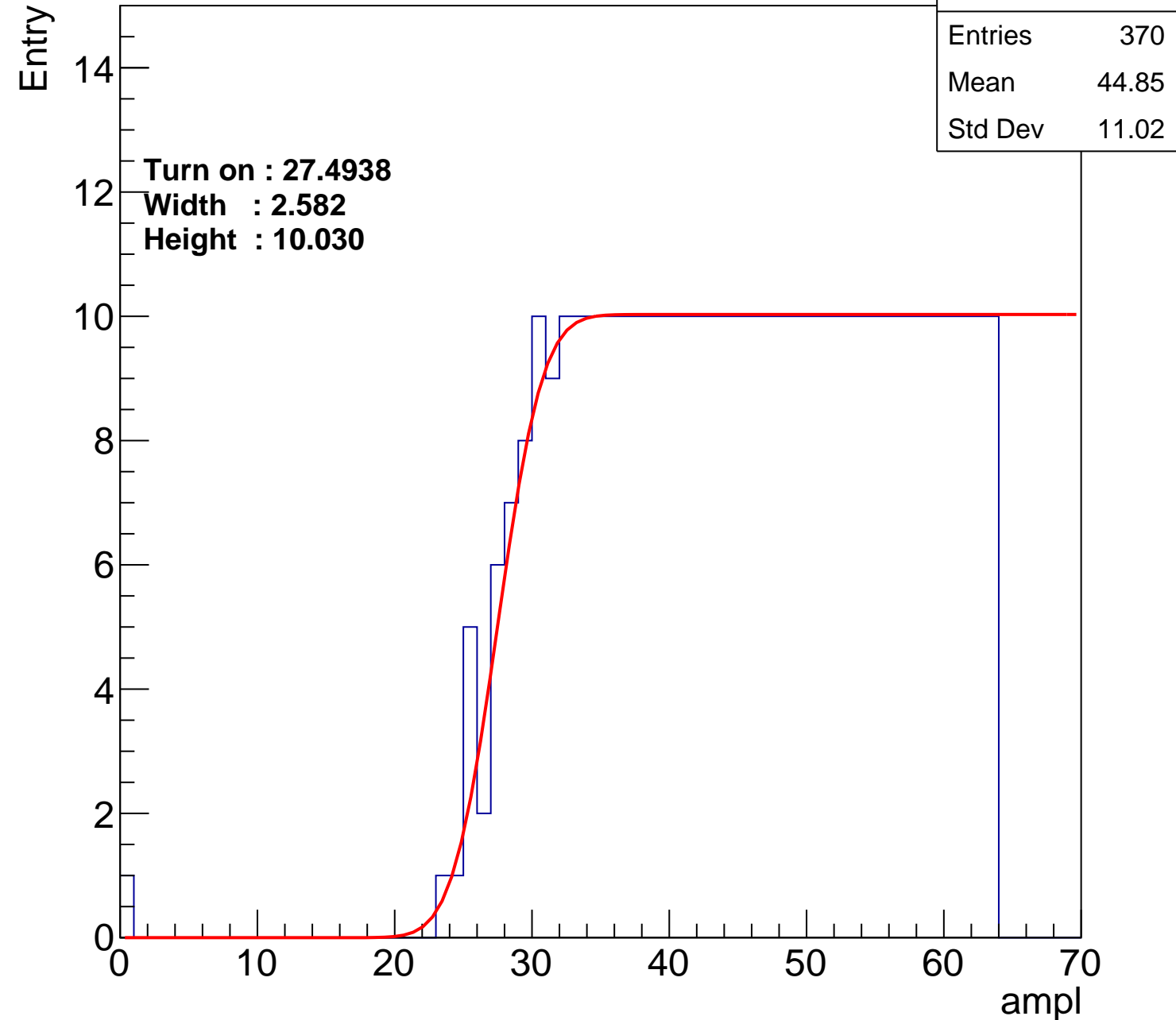
Width : 2.582

Height : 10.030

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch110

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	348
Mean	45.83
Std Dev	10.71

Turn on : 29.3814

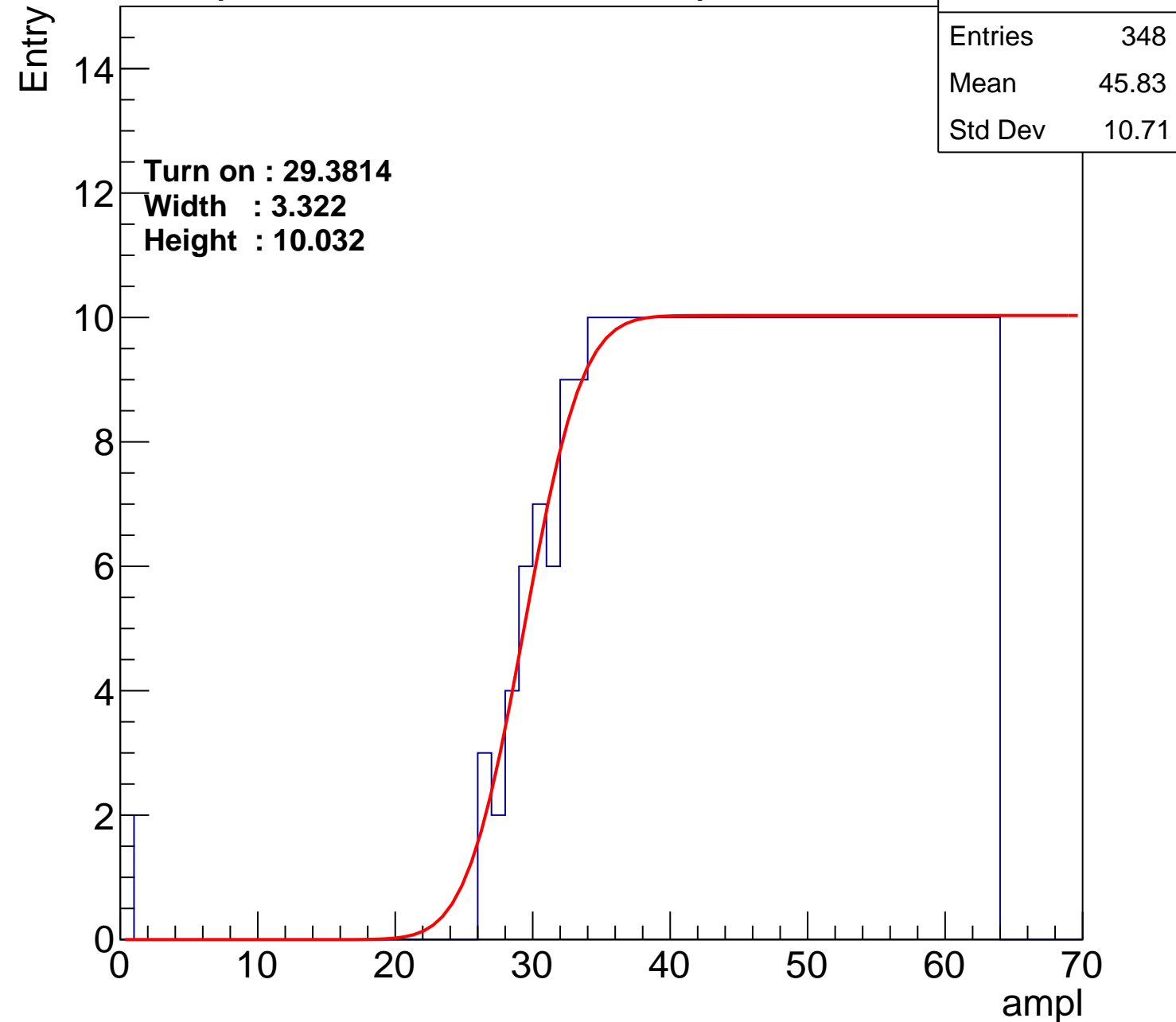
Width : 3.322

Height : 10.032

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L000S, U1-ch111

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	374
Mean	44.42
Std Dev	11.74

Turn on : 27.3509

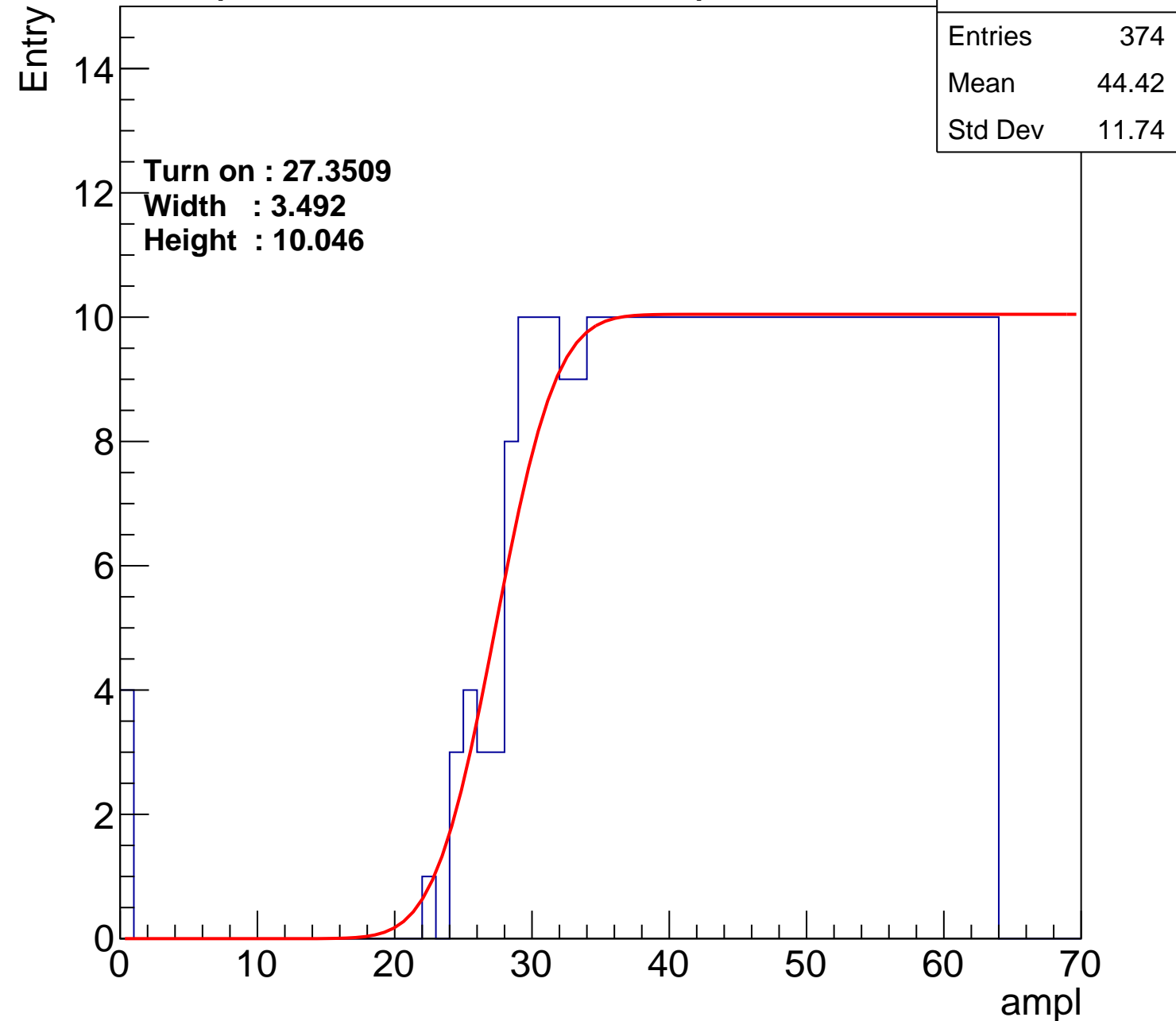
Width : 3.492

Height : 10.046

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch112

calib\_packv5\_042523\_0143.root, FC#5, port B1

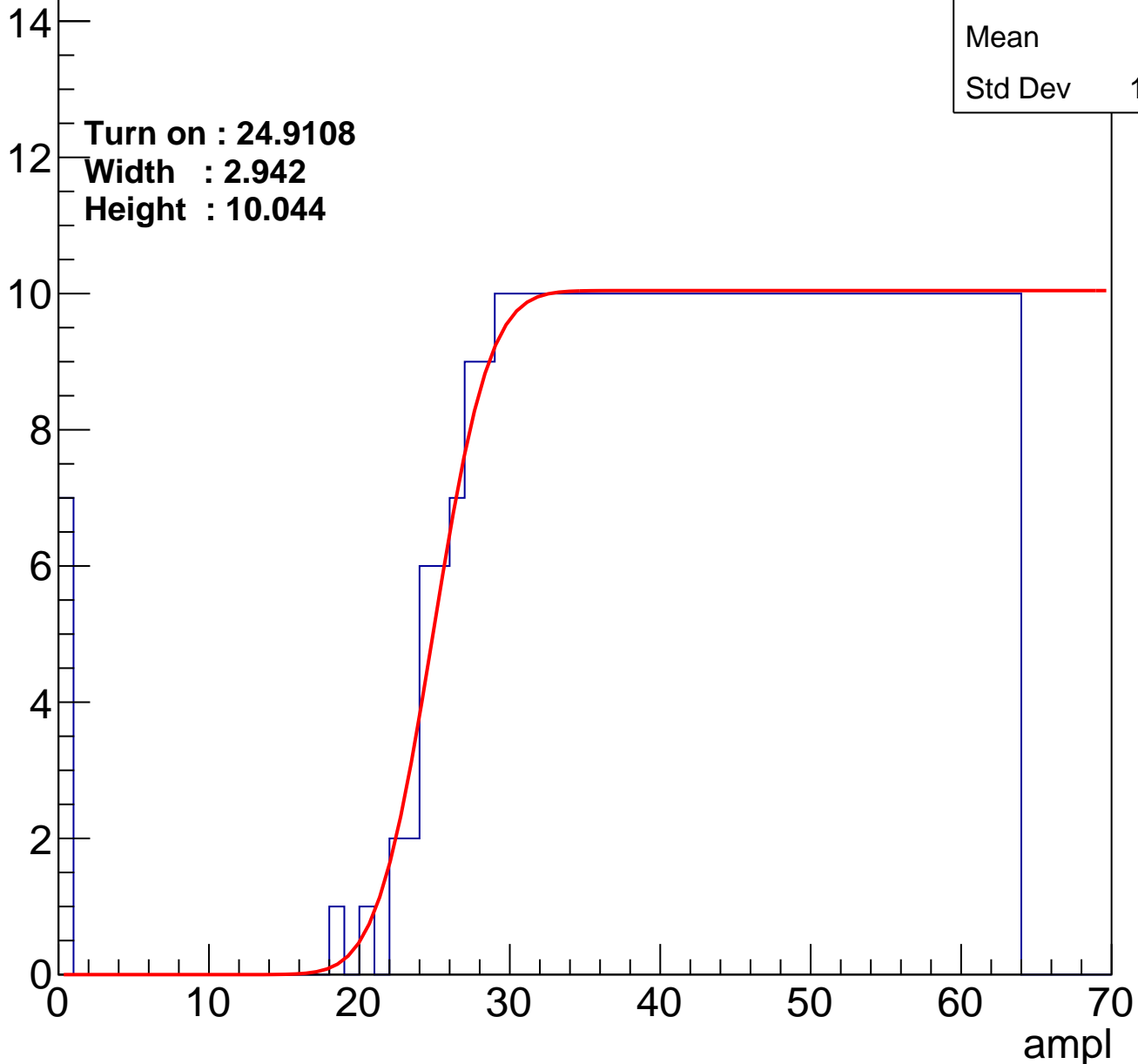
Entries	400
Mean	43
Std Dev	12.76

**Turn on : 24.9108**

**Width : 2.942**

**Height : 10.044**

Entry



# B0L000S, U1-ch113

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	376
Mean	44.3
Std Dev	11.82

Turn on : 26.9341

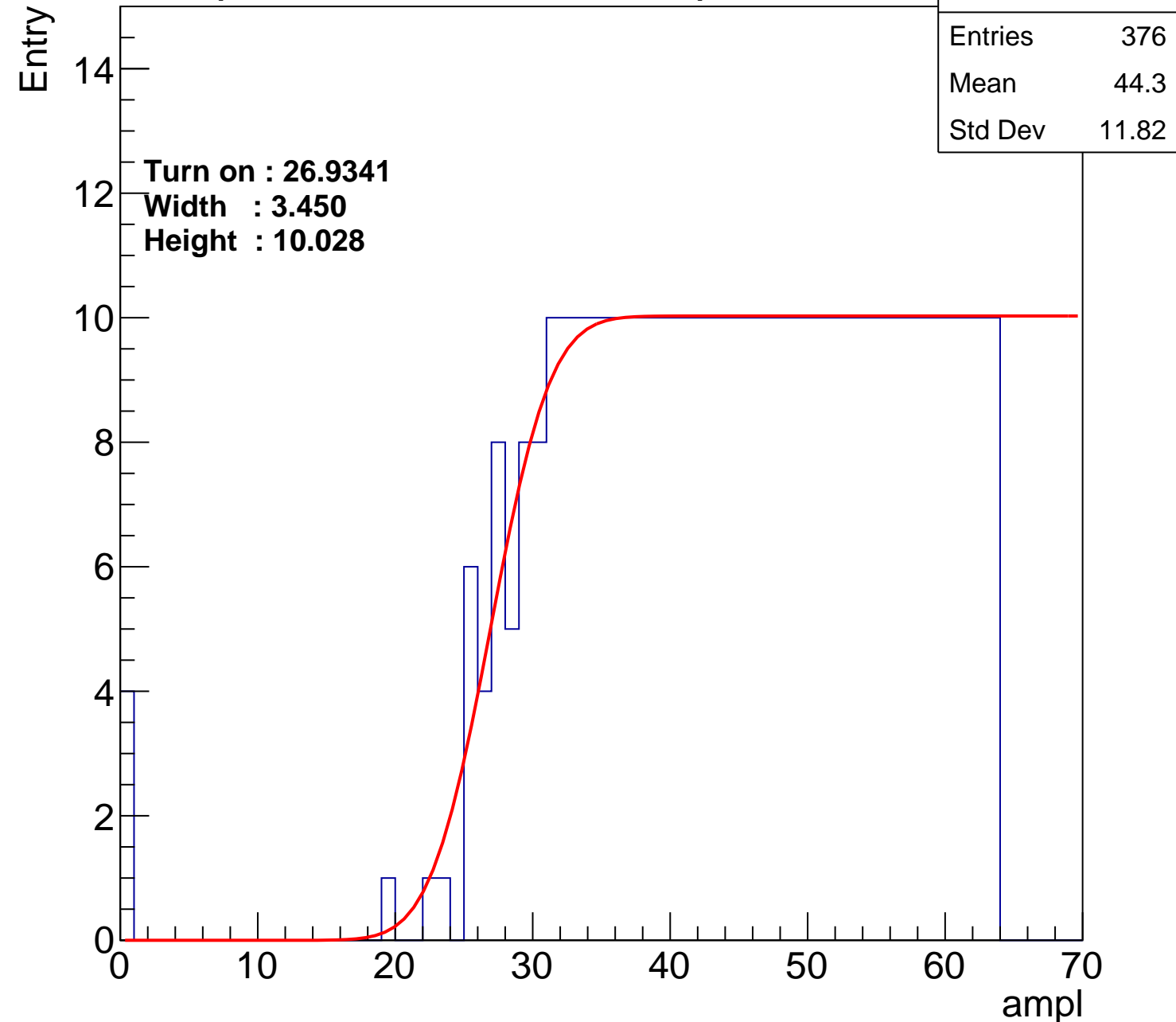
Width : 3.450

Height : 10.028

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch114

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	368
Mean	44.74
Std Dev	11.49

Turn on : 28.4966

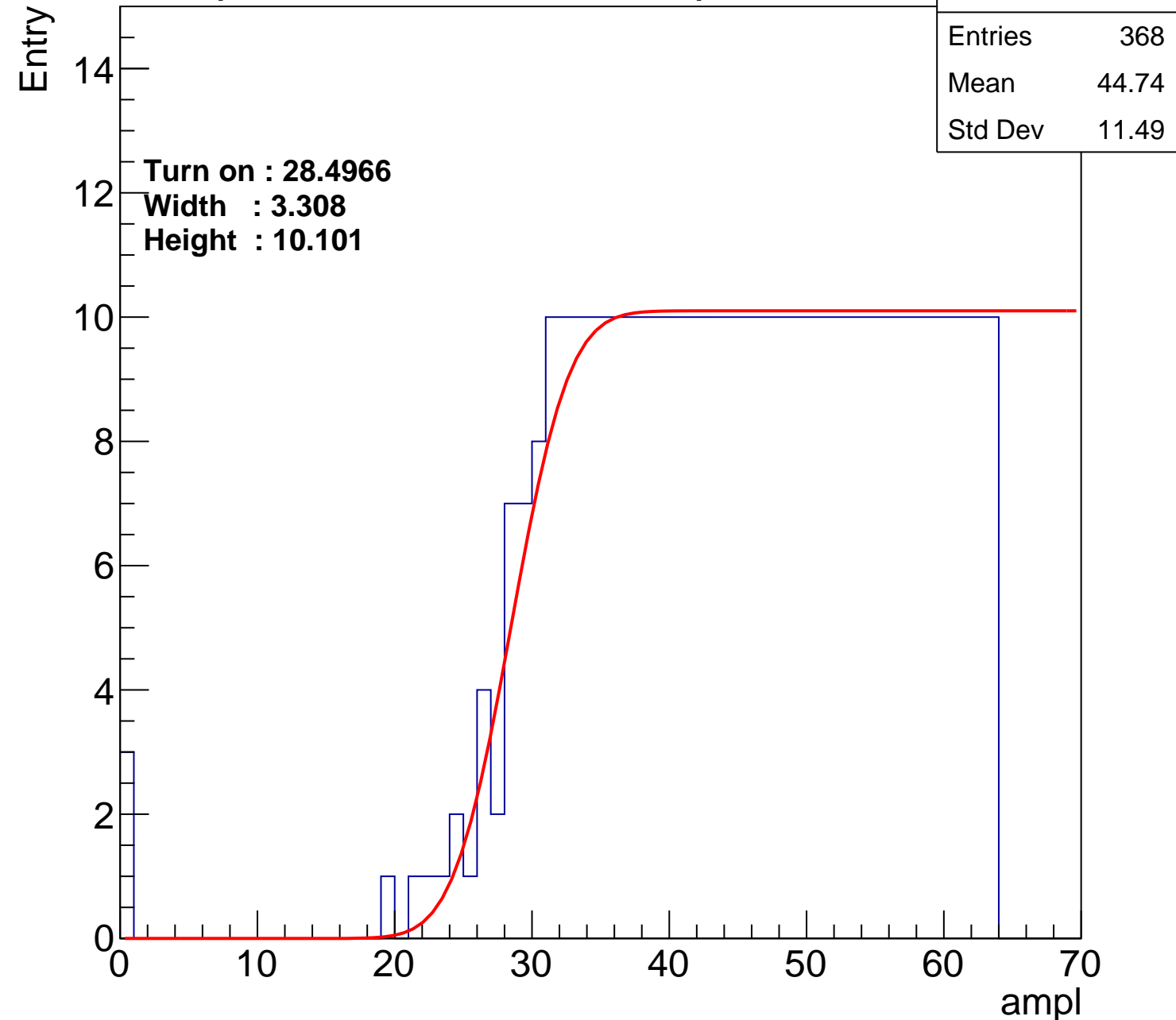
Width : 3.308

Height : 10.101

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch115

calib\_packv5\_042523\_0143.root, FC#5, port B1

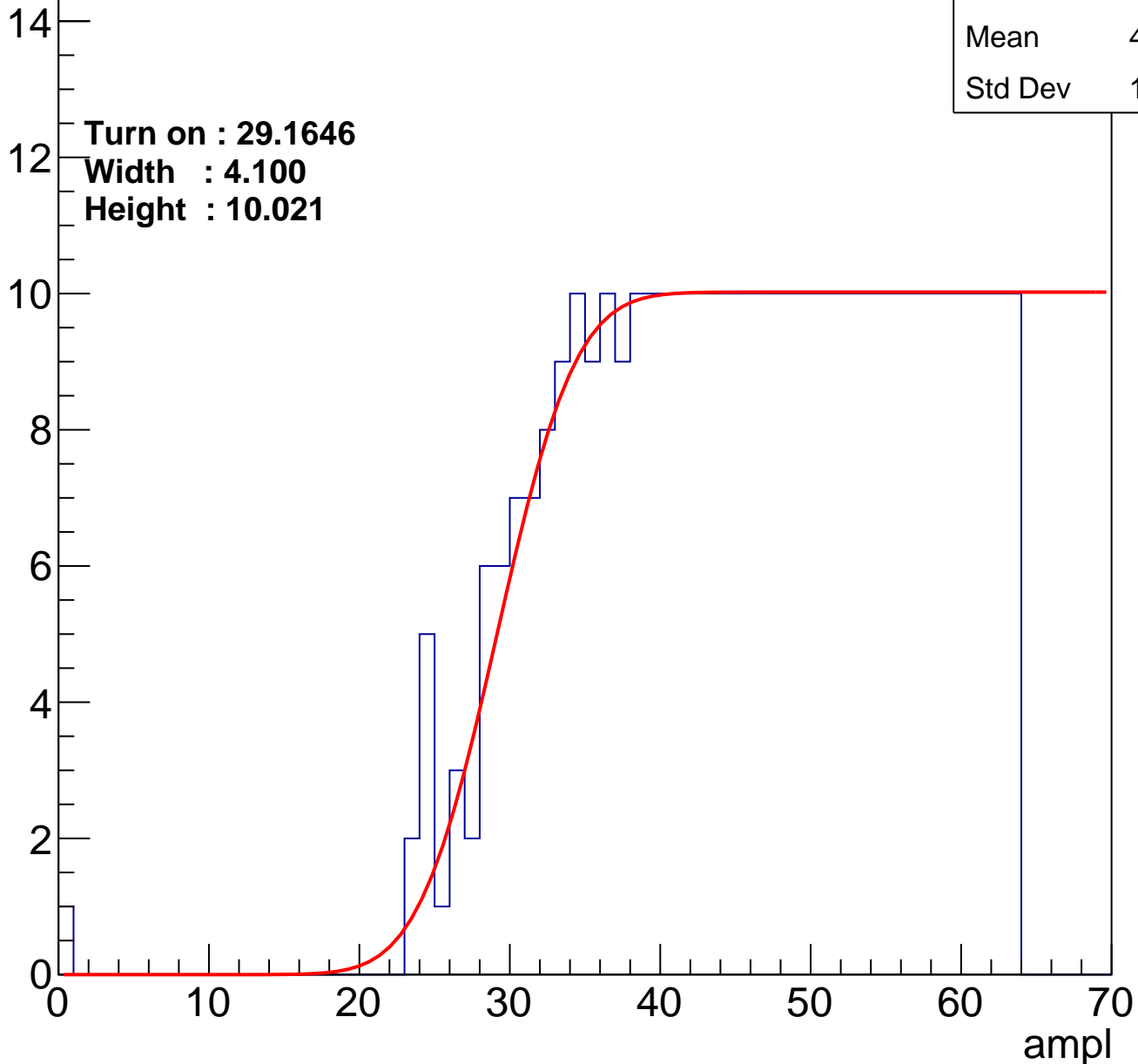
Entries	355
Mean	45.42
Std Dev	10.89

Turn on : 29.1646

Width : 4.100

Height : 10.021

Entry



# B0L000S, U1-ch116

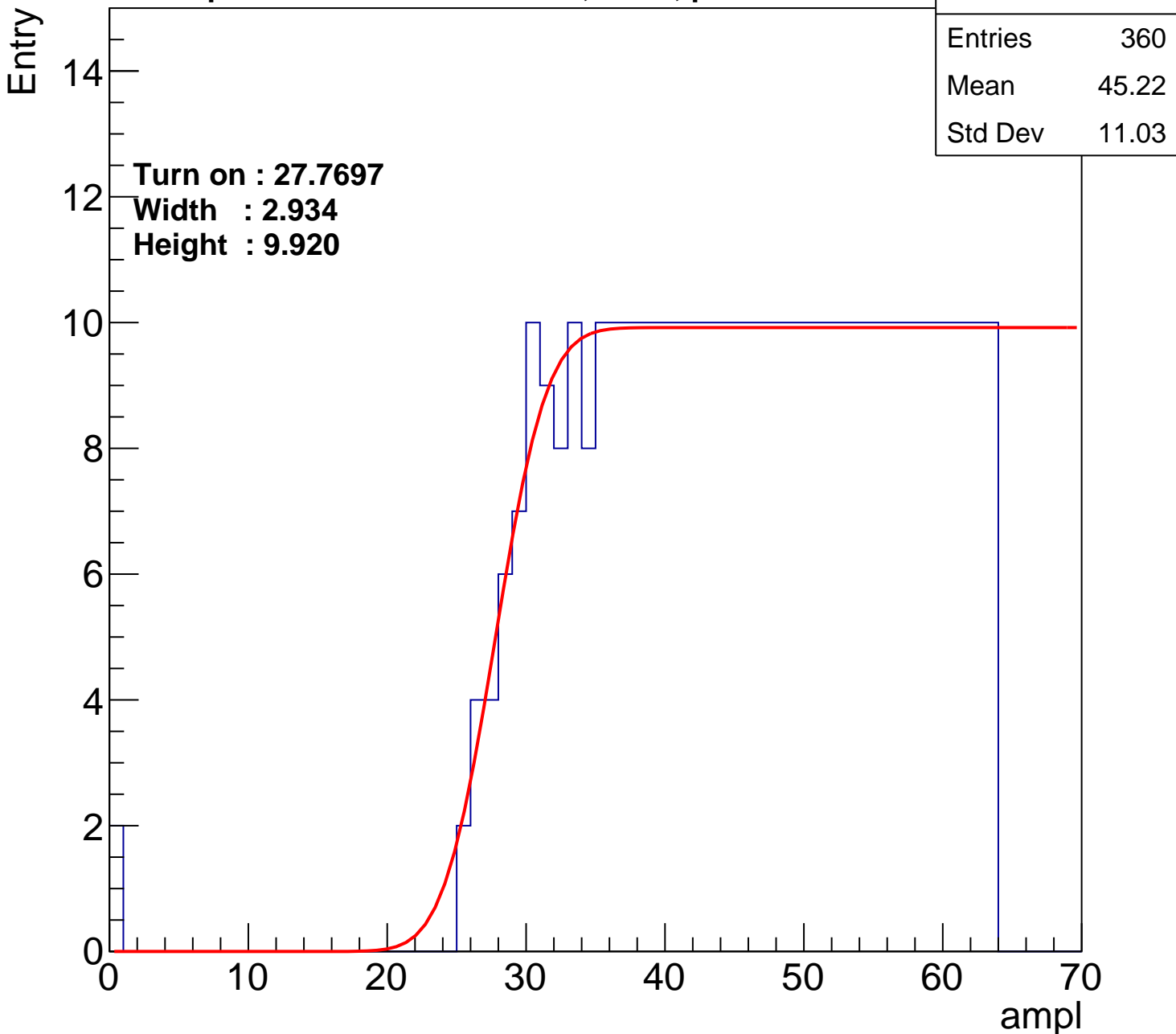
**calib\_packv5\_042523\_0143.root, FC#5, port B1**

Entries	360
Mean	45.22
Std Dev	11.03

**Turn on : 27.7697**

**Width : 2.934**

**Height : 9.920**



# B0L000S, U1-ch117

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	359
Mean	45.25
Std Dev	11.06

Turn on : 29.0934

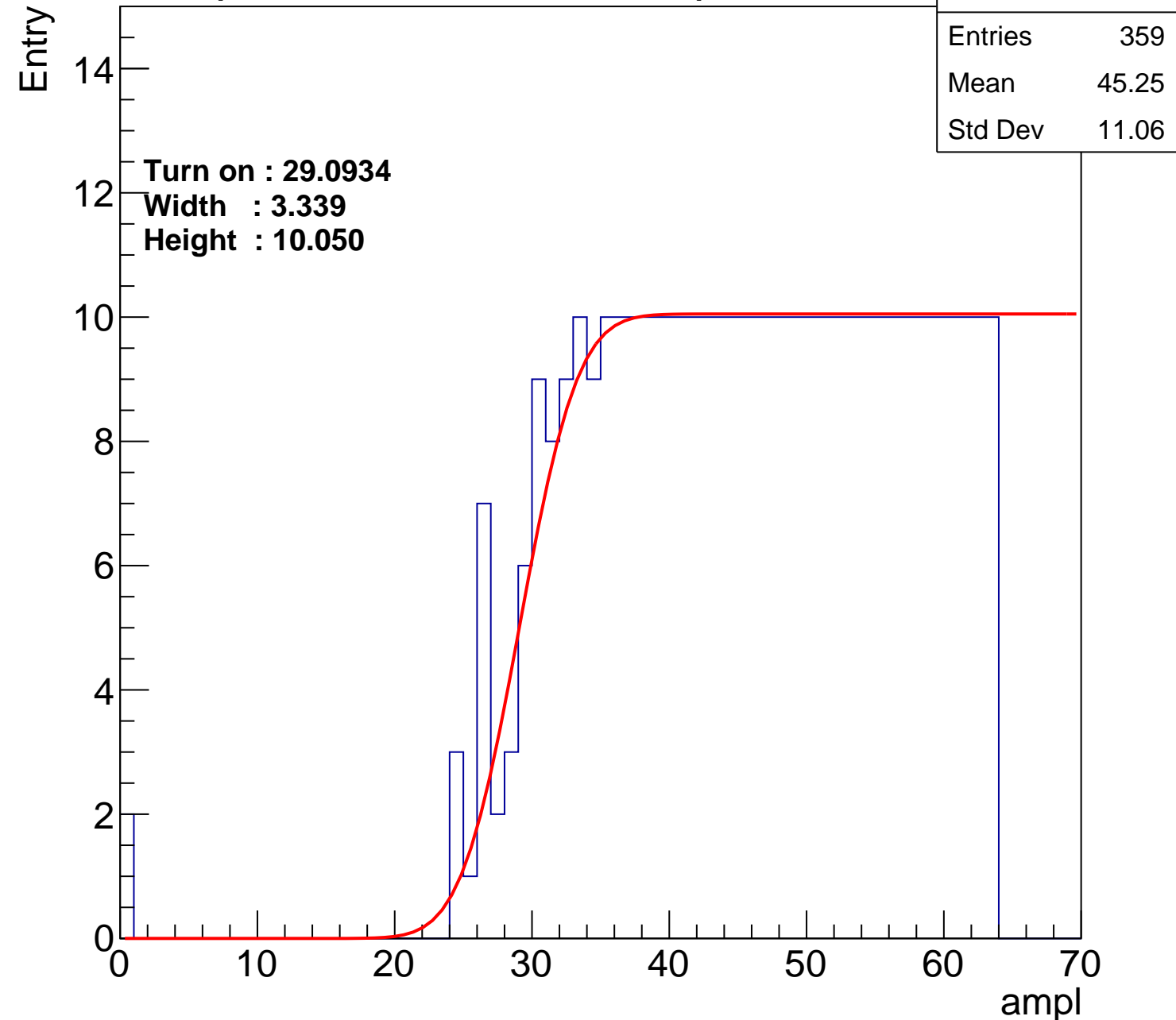
Width : 3.339

Height : 10.050

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch118

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	352
Mean	45.61
Std Dev	10.85

**Turn on : 29.1657**

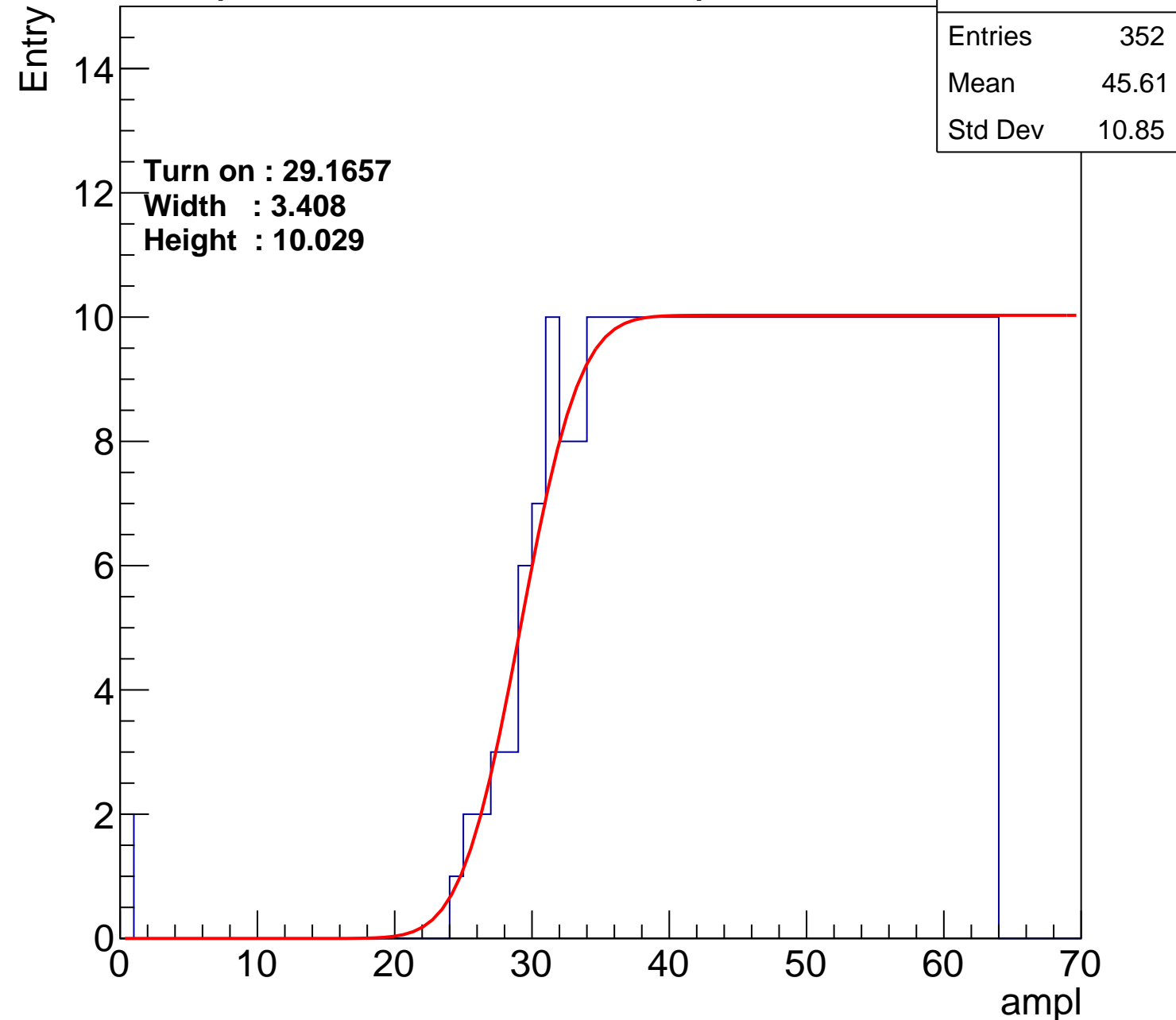
**Width : 3.408**

**Height : 10.029**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L000S, U1-ch119

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	363
Mean	44.84
Std Dev	11.75

**Turn on : 28.2098**

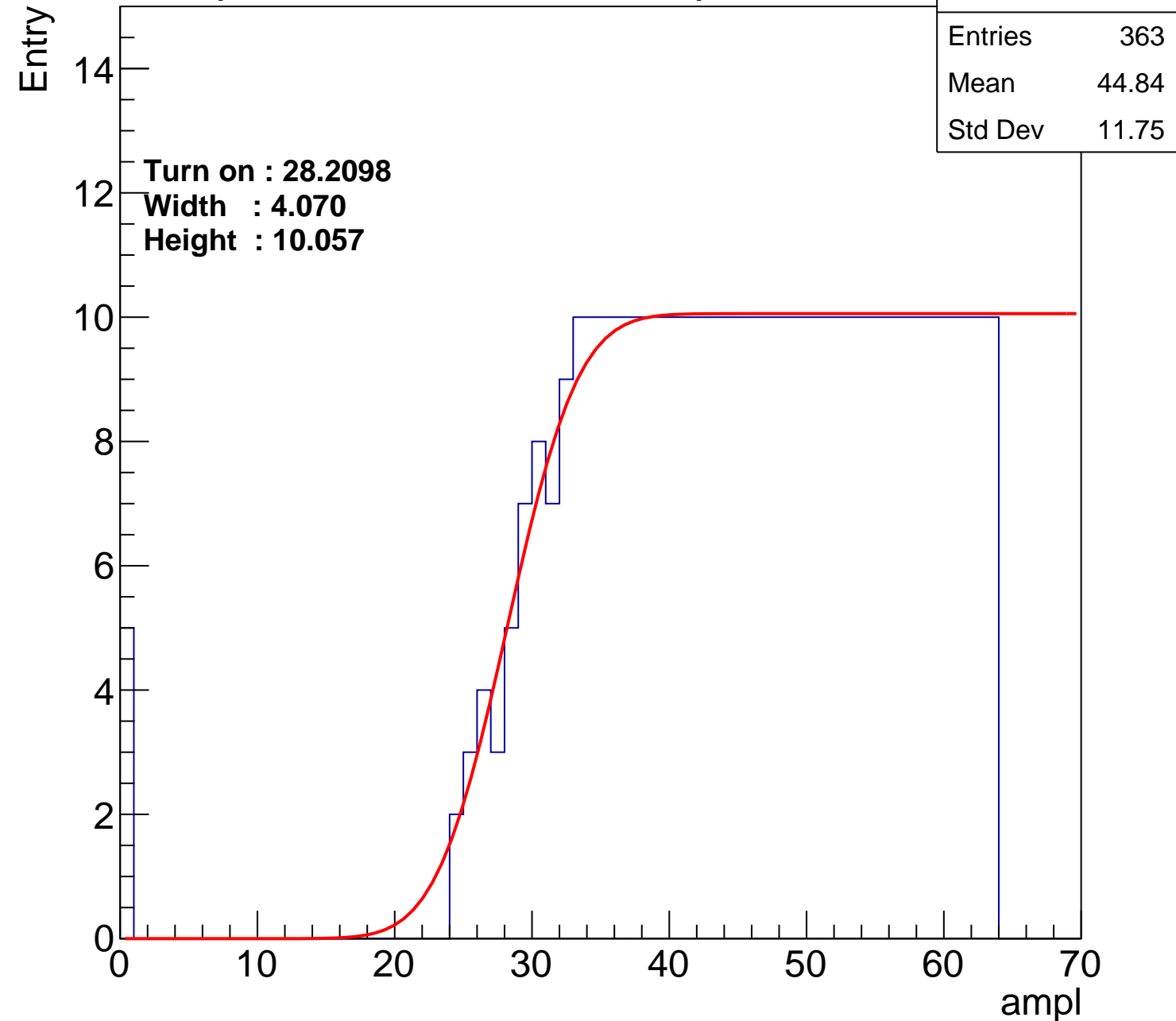
**Width : 4.070**

**Height : 10.057**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch120

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	351
Mean	45.55
Std Dev	11.11

Turn on : 30.0285

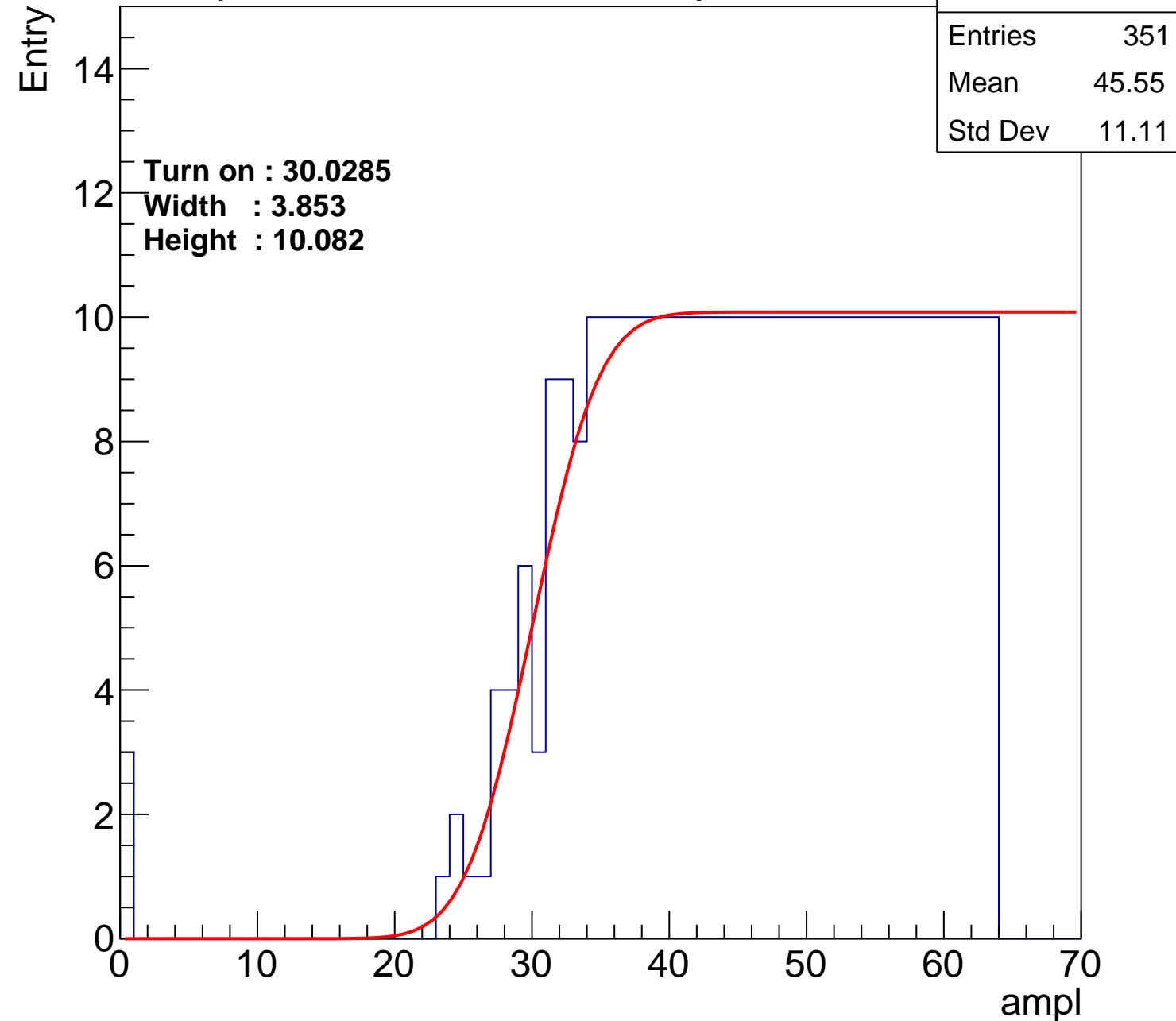
Width : 3.853

Height : 10.082

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch121

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	360
Mean	45.02
Std Dev	11.56

Turn on : 28.6640

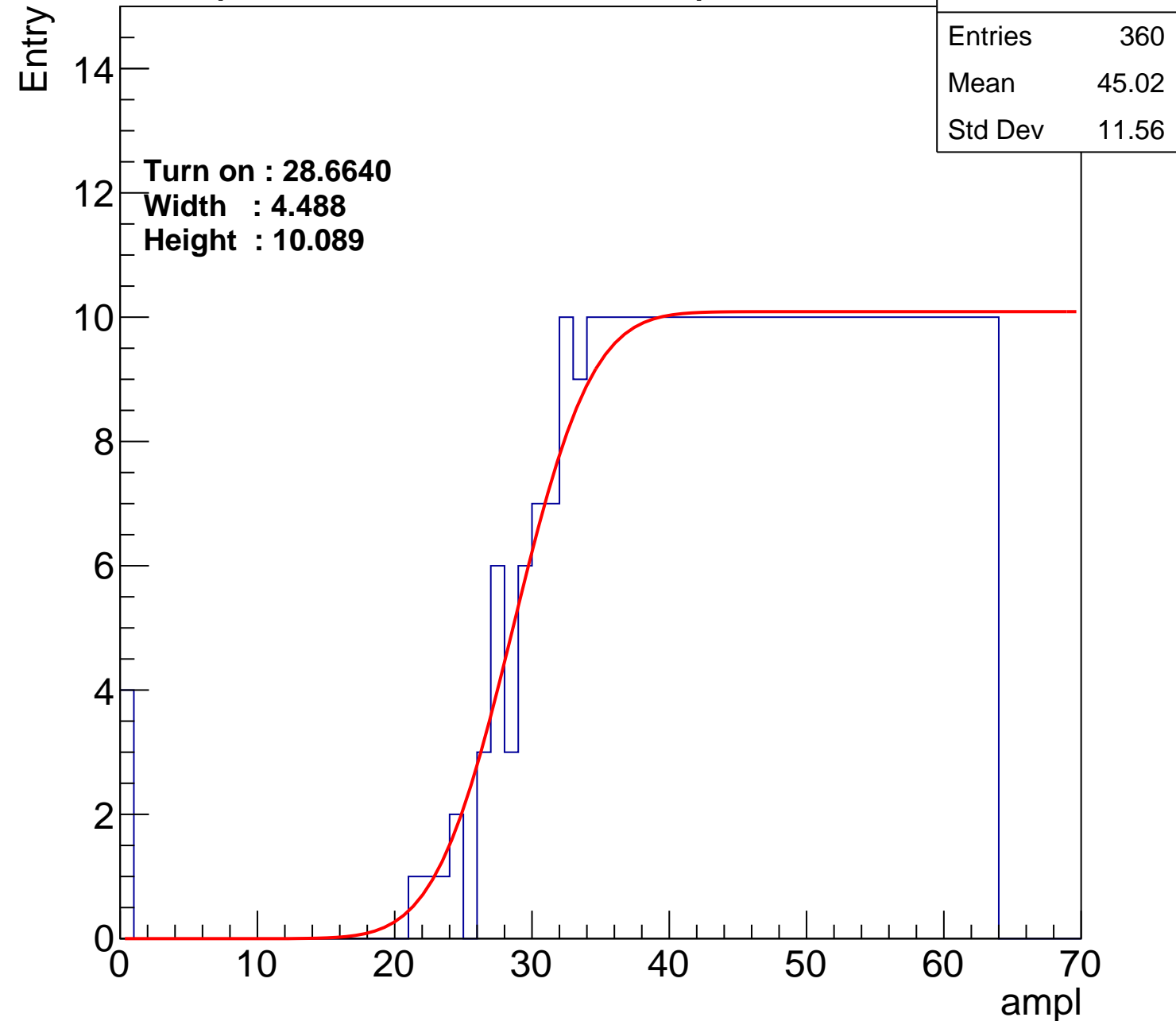
Width : 4.488

Height : 10.089

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch122

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	379
Mean	44.18
Std Dev	11.77

Turn on : 26.9886

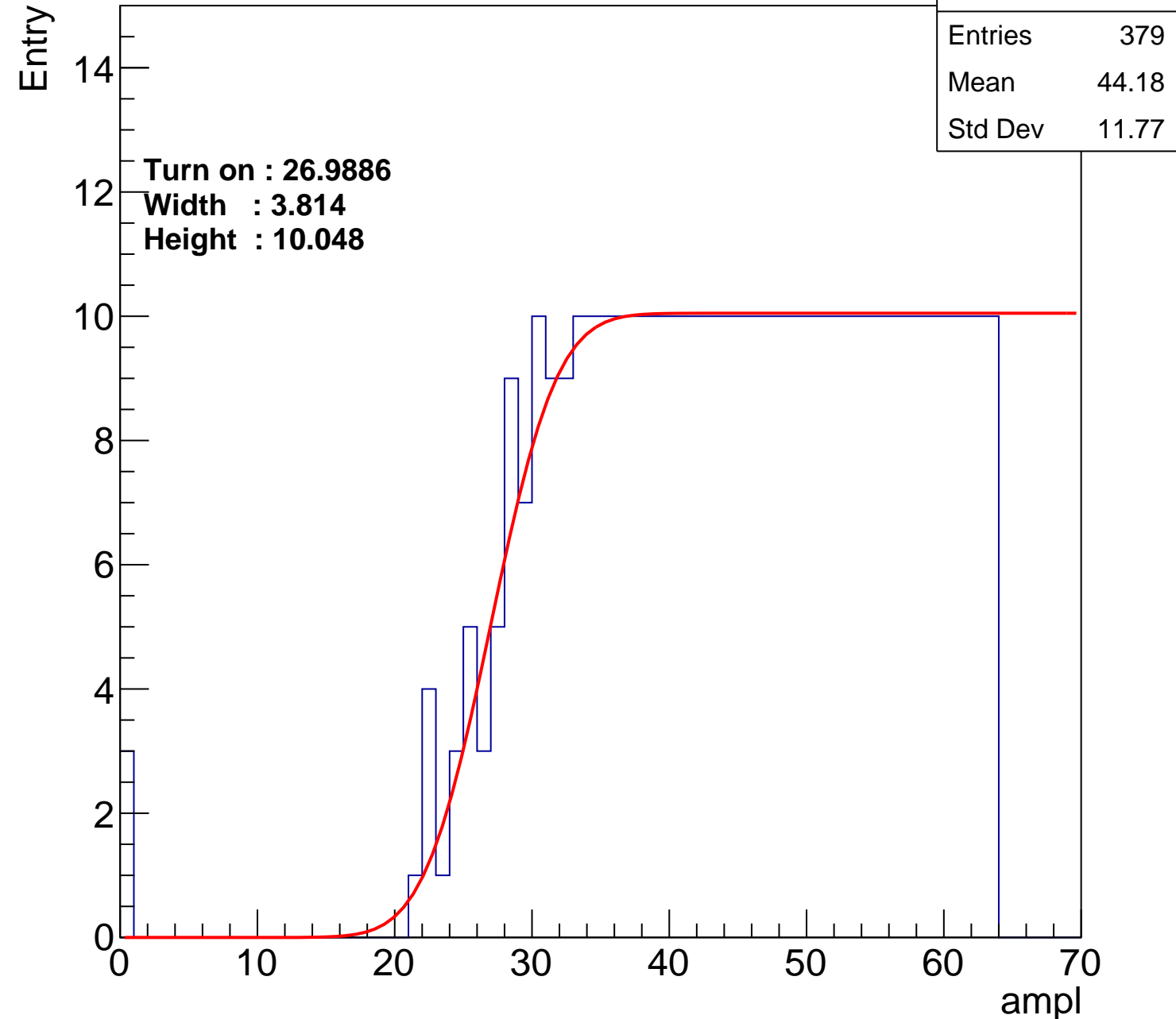
Width : 3.814

Height : 10.048

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch123

calib\_packv5\_042523\_0143.root, FC#5, port B1

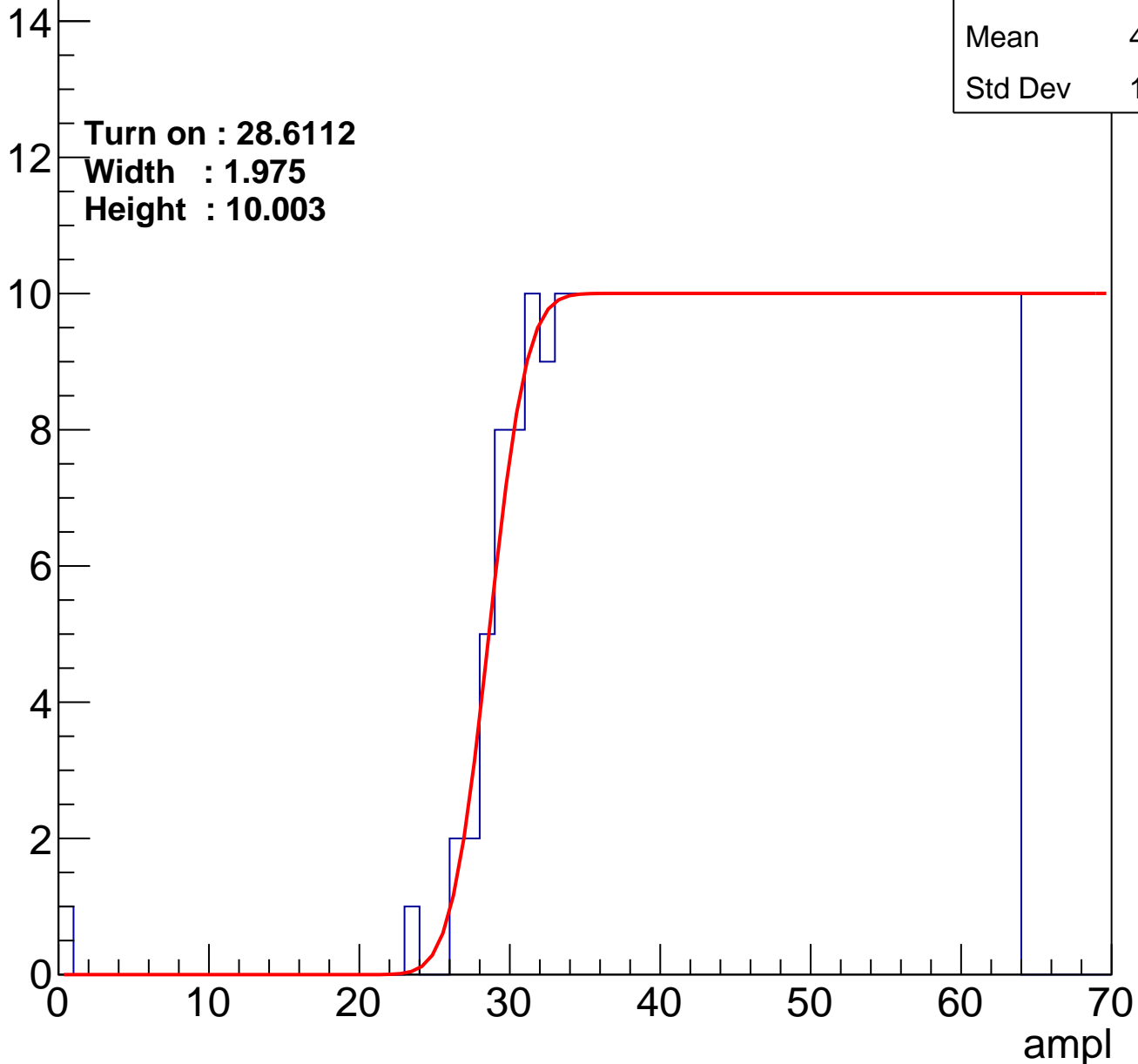
Entries	356
Mean	45.56
Std Dev	10.62

Turn on : 28.6112

Width : 1.975

Height : 10.003

Entry



# B0L000S, U1-ch124

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	383
Mean	43.99
Std Dev	11.85

Turn on : 26.1148

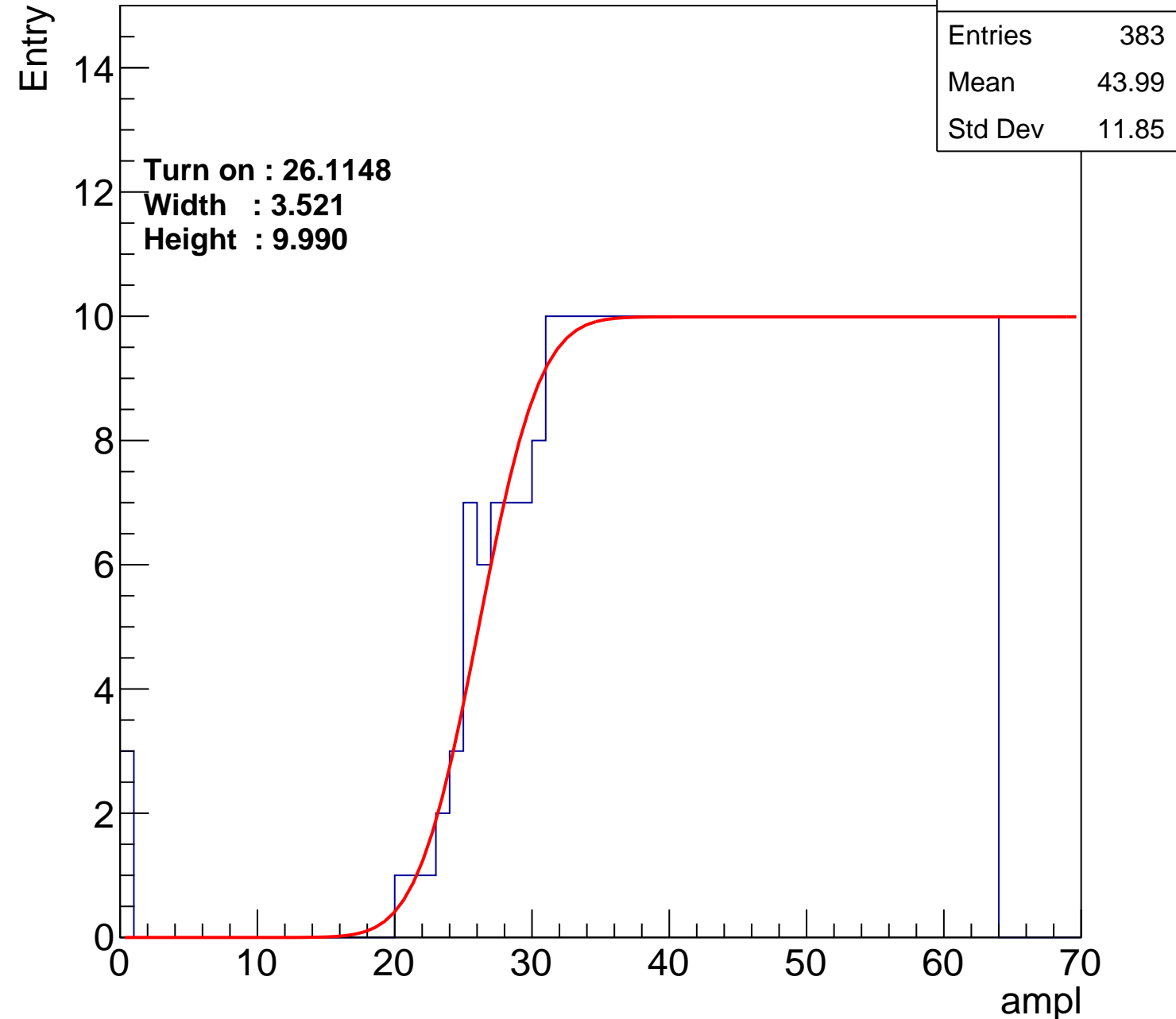
Width : 3.521

Height : 9.990

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch125

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	373
Mean	44.36
Std Dev	11.96

Turn on : 27.7527

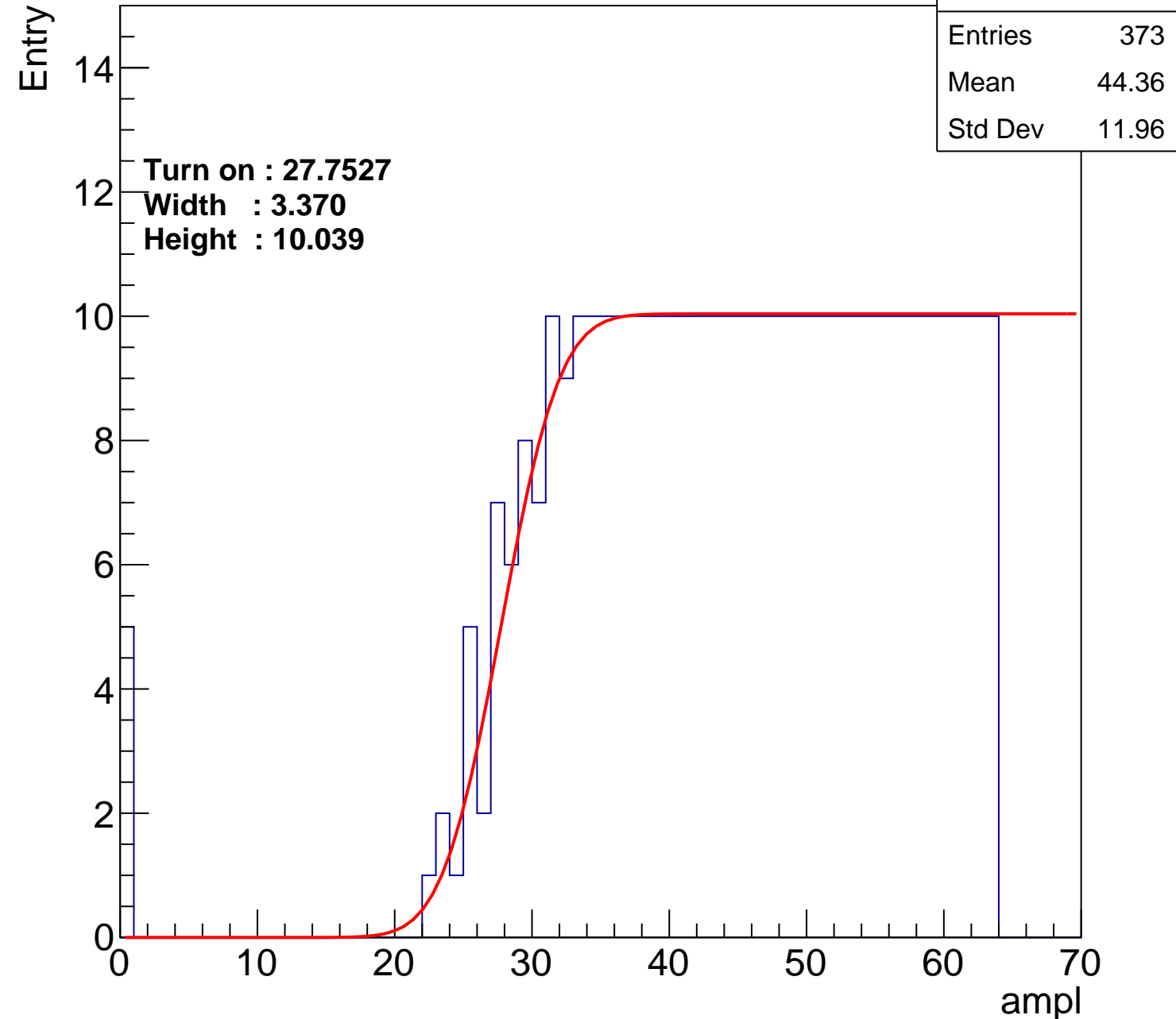
Width : 3.370

Height : 10.039

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch126

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	372
Mean	44.38
Std Dev	11.98

Turn on : 27.5704

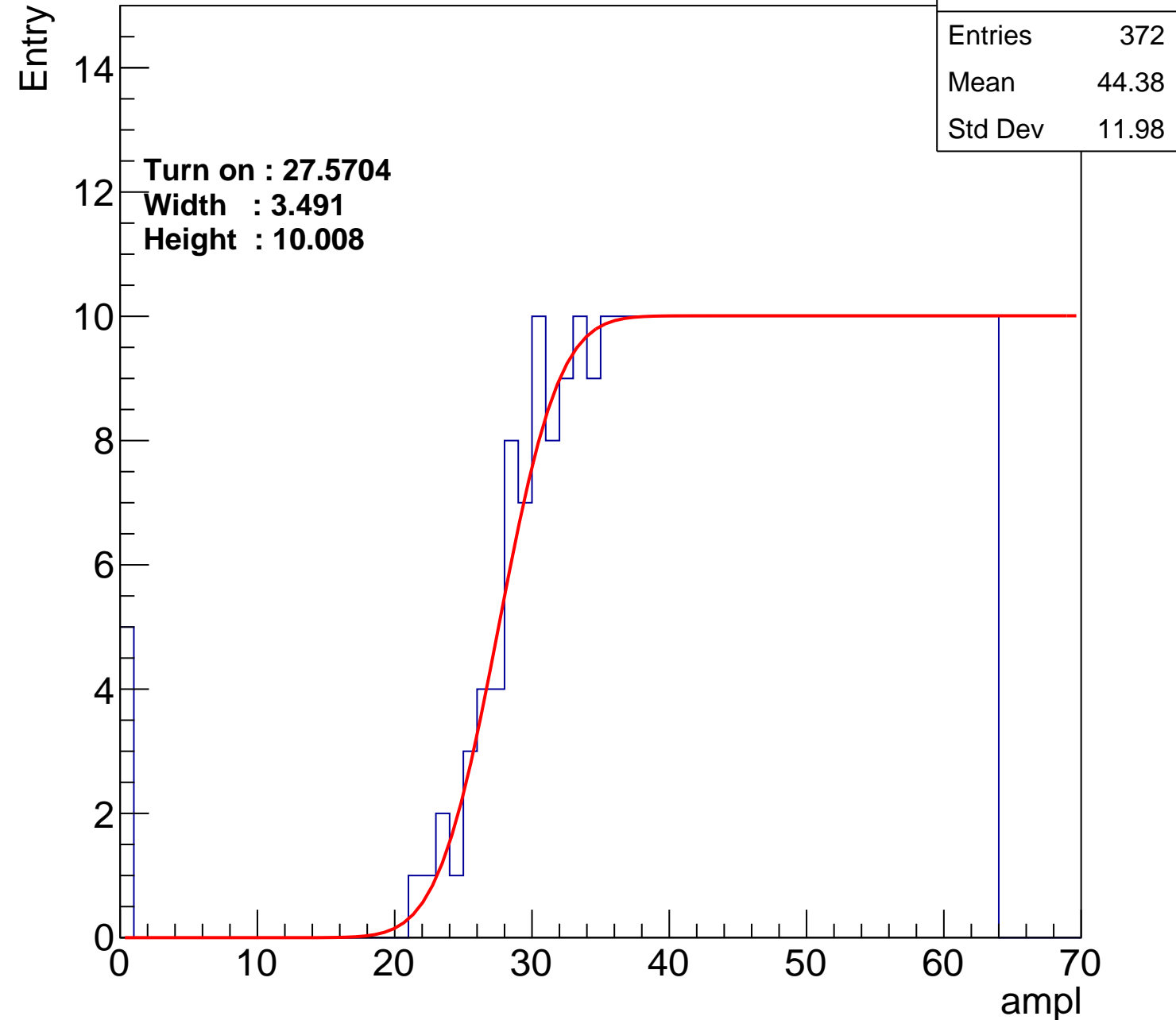
Width : 3.491

Height : 10.008

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl





# B0L000S, U1-ch127

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	357
Mean	45.18
Std Dev	11.47

**Turn on : 29.4768**

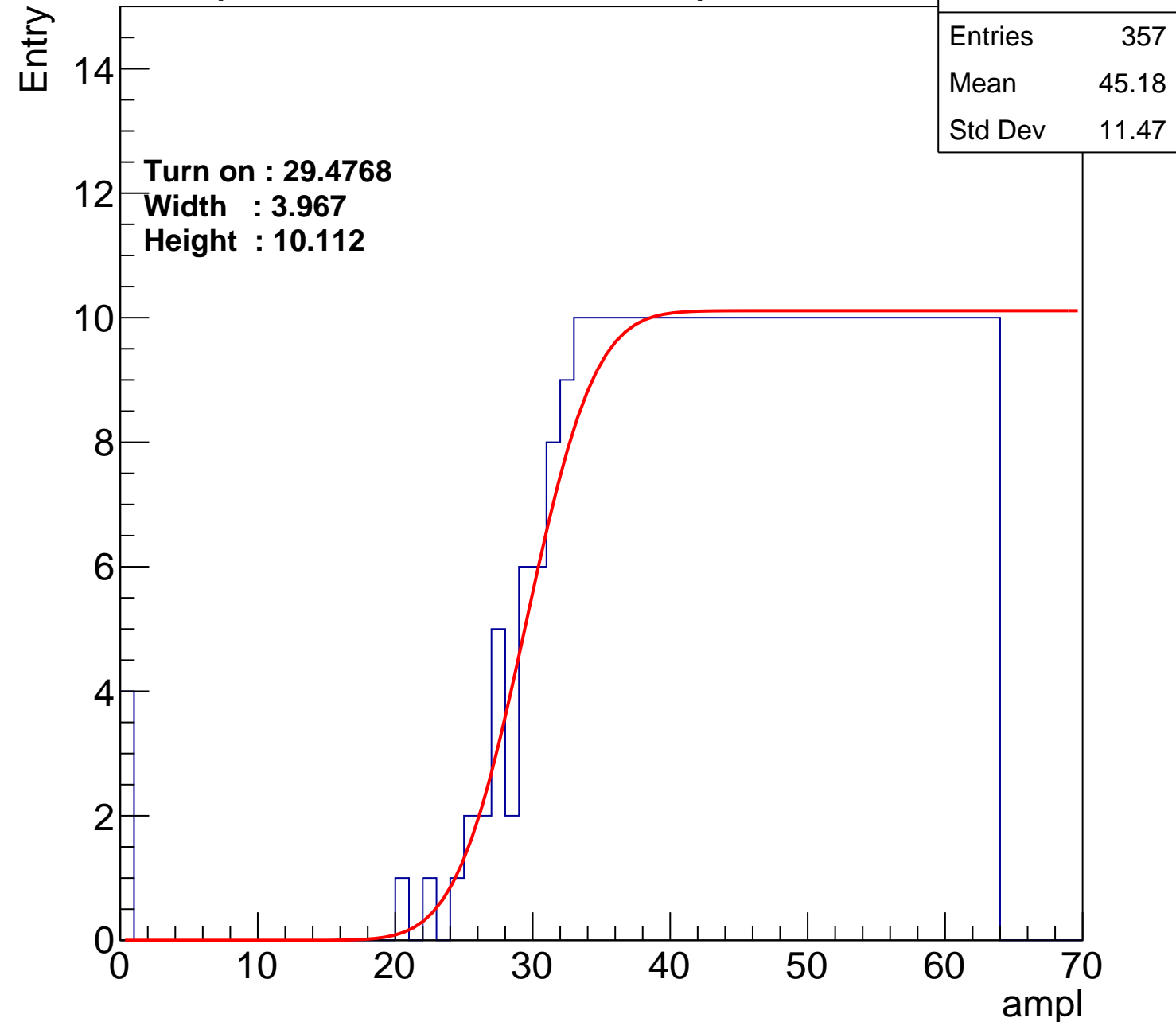
**Width : 3.967**

**Height : 10.112**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl



# B0L000S, U1-ch127

calib\_packv5\_042523\_0143.root, FC#5, port B1

Entries	357
Mean	45.18
Std Dev	11.47

**Turn on : 29.4768**

**Width : 3.967**

**Height : 10.112**

Entry

14  
12  
10  
8  
6  
4  
2  
0

ampl

