

B1L103S, U2-ch0

calib_packv5_042523_0143.root, FC#7, port C2

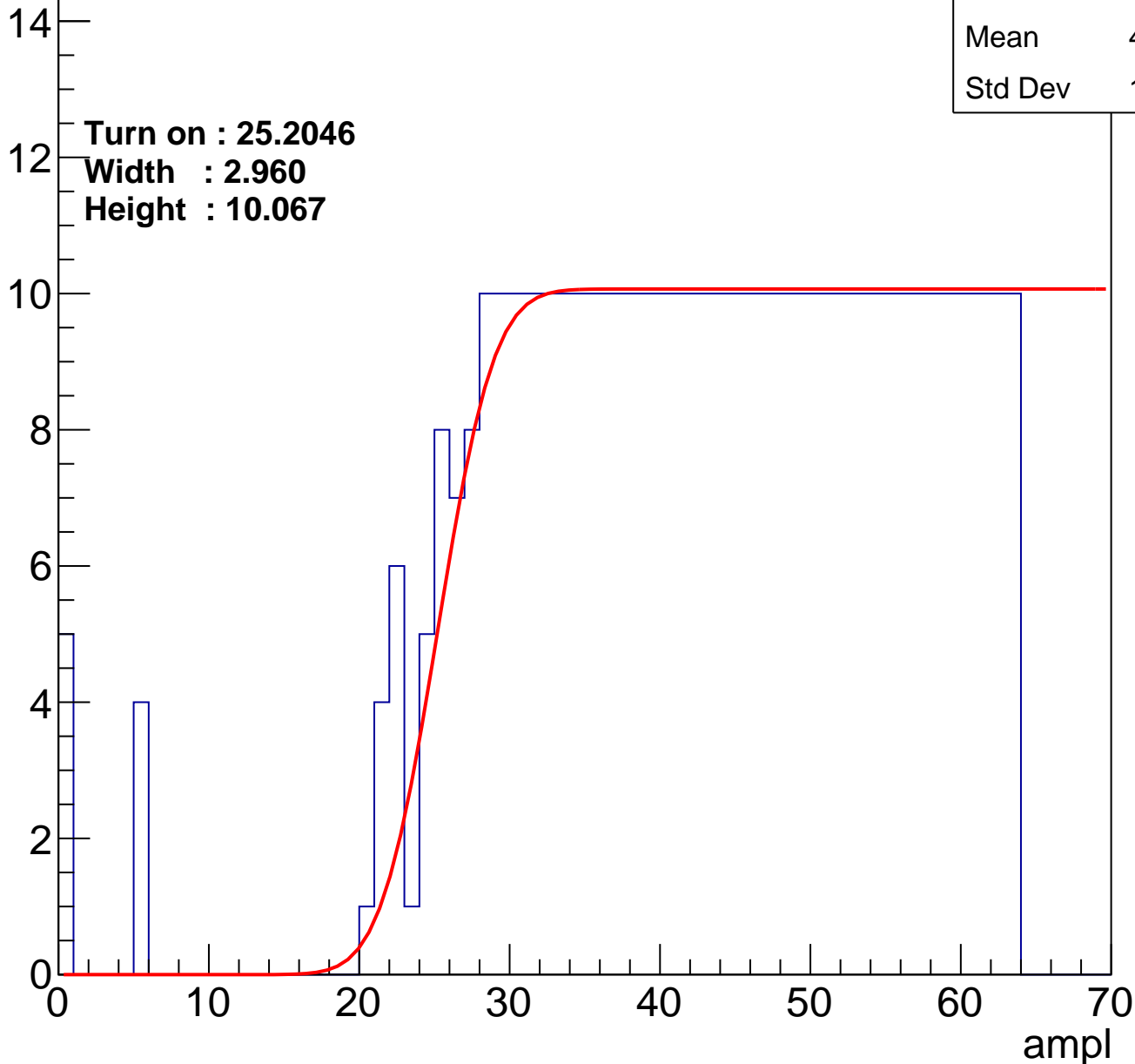
Entries	409
Mean	42.49
Std Dev	13.08

Turn on : 25.2046

Width : 2.960

Height : 10.067

Entry



B1L103S, U2-ch1

calib_packv5_042523_0143.root, FC#7, port C2

Entries	375
Mean	44.47
Std Dev	11.45

Turn on : 27.4315

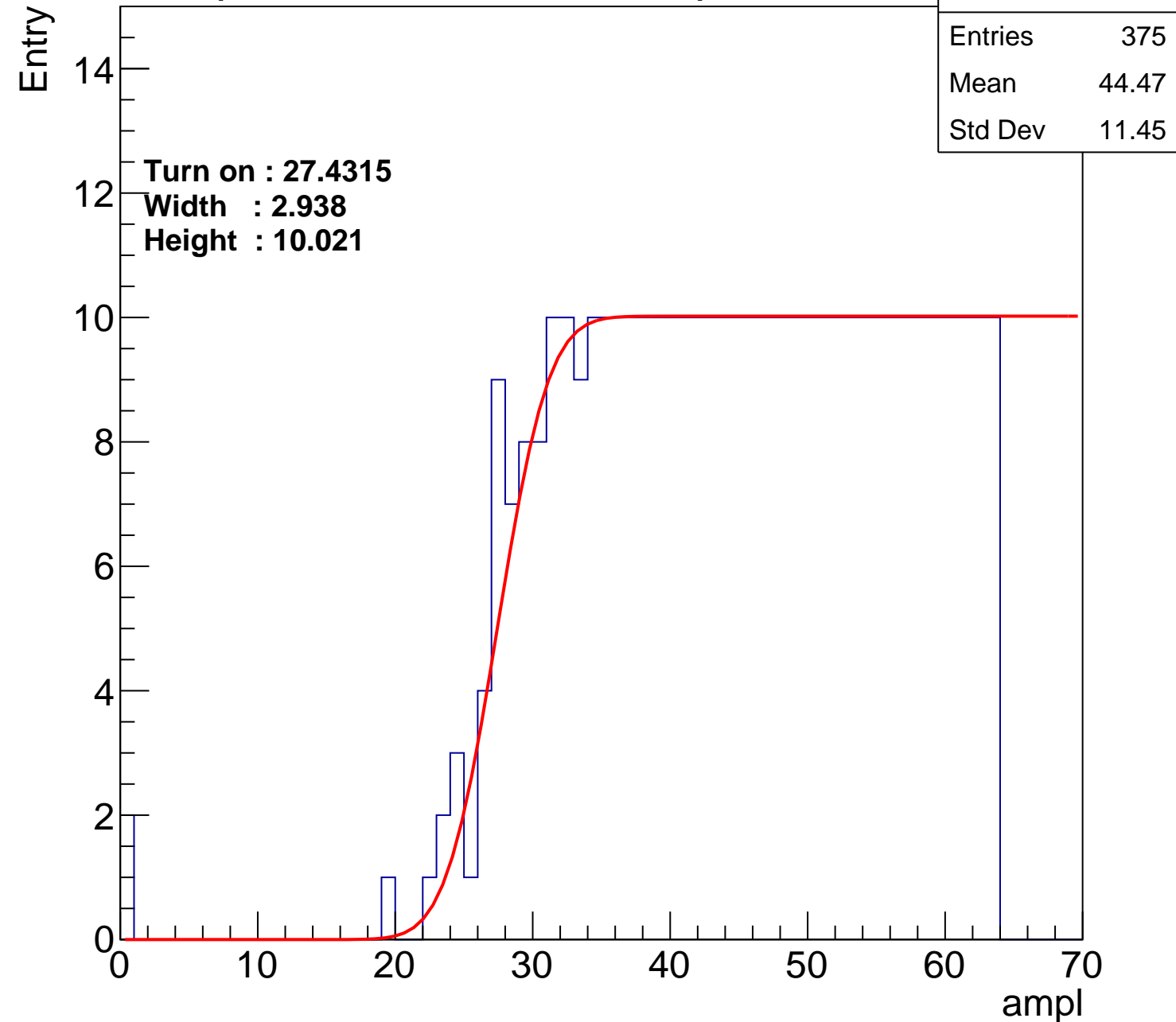
Width : 2.938

Height : 10.021

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch2

calib_packv5_042523_0143.root, FC#7, port C2

Entries	378
Mean	44.22
Std Dev	11.84

Turn on : 27.0794

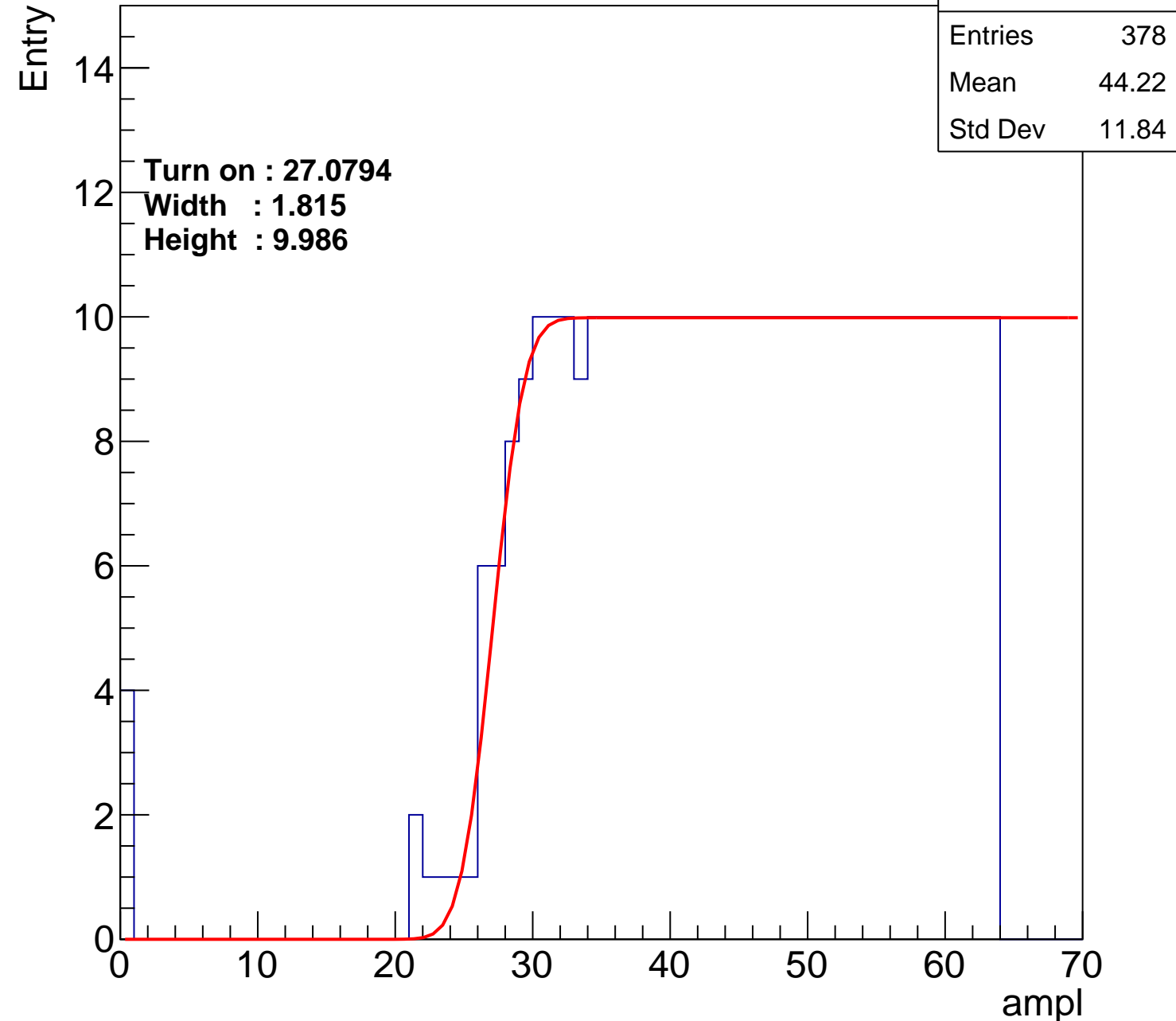
Width : 1.815

Height : 9.986

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch3

calib_packv5_042523_0143.root, FC#7, port C2

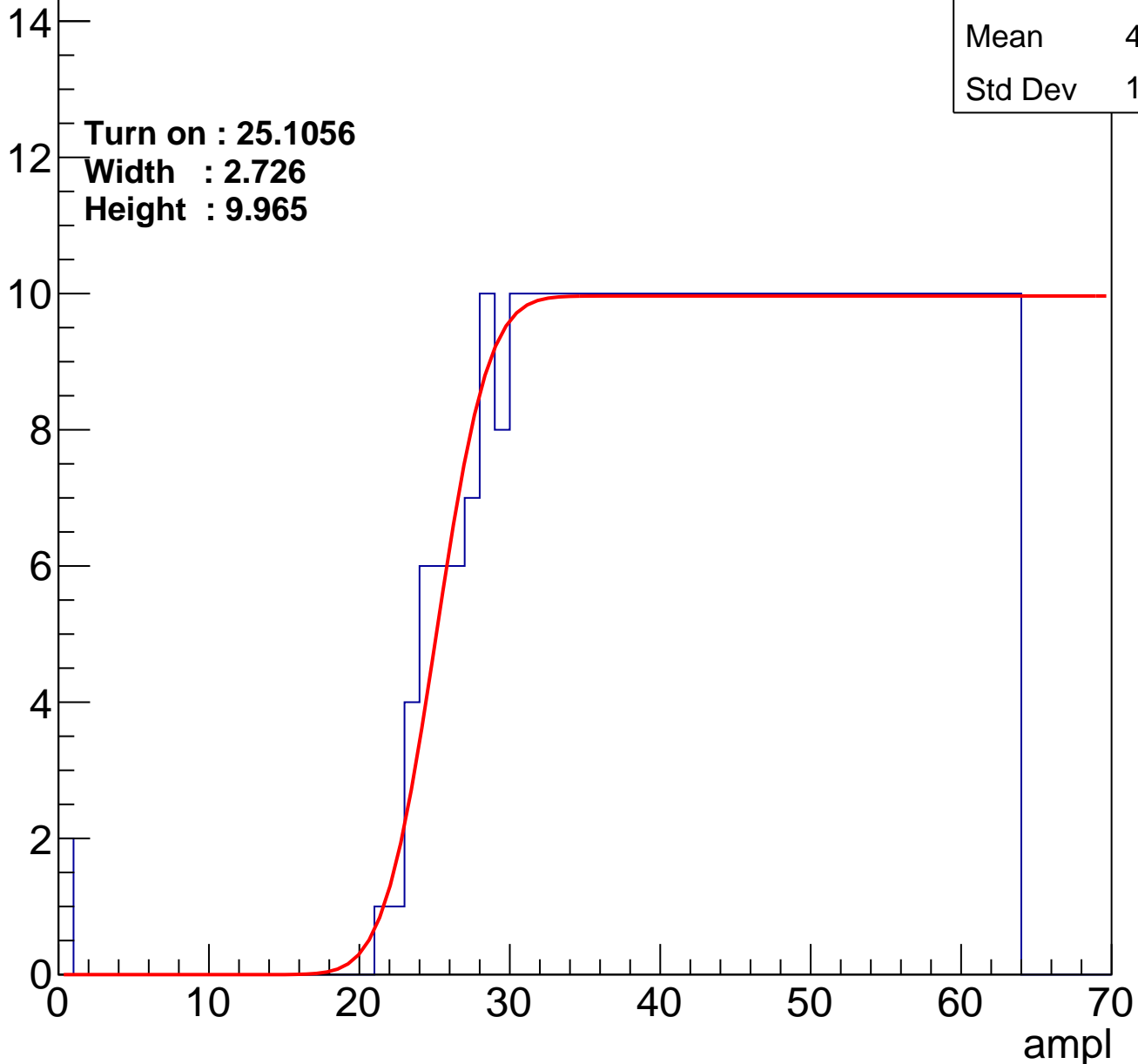
Entries	391
Mean	43.72
Std Dev	11.79

Turn on : 25.1056

Width : 2.726

Height : 9.965

Entry



B1L103S, U2-ch4

calib_packv5_042523_0143.root, FC#7, port C2

Entries	371
Mean	44.68
Std Dev	11.32

Turn on : 27.3137

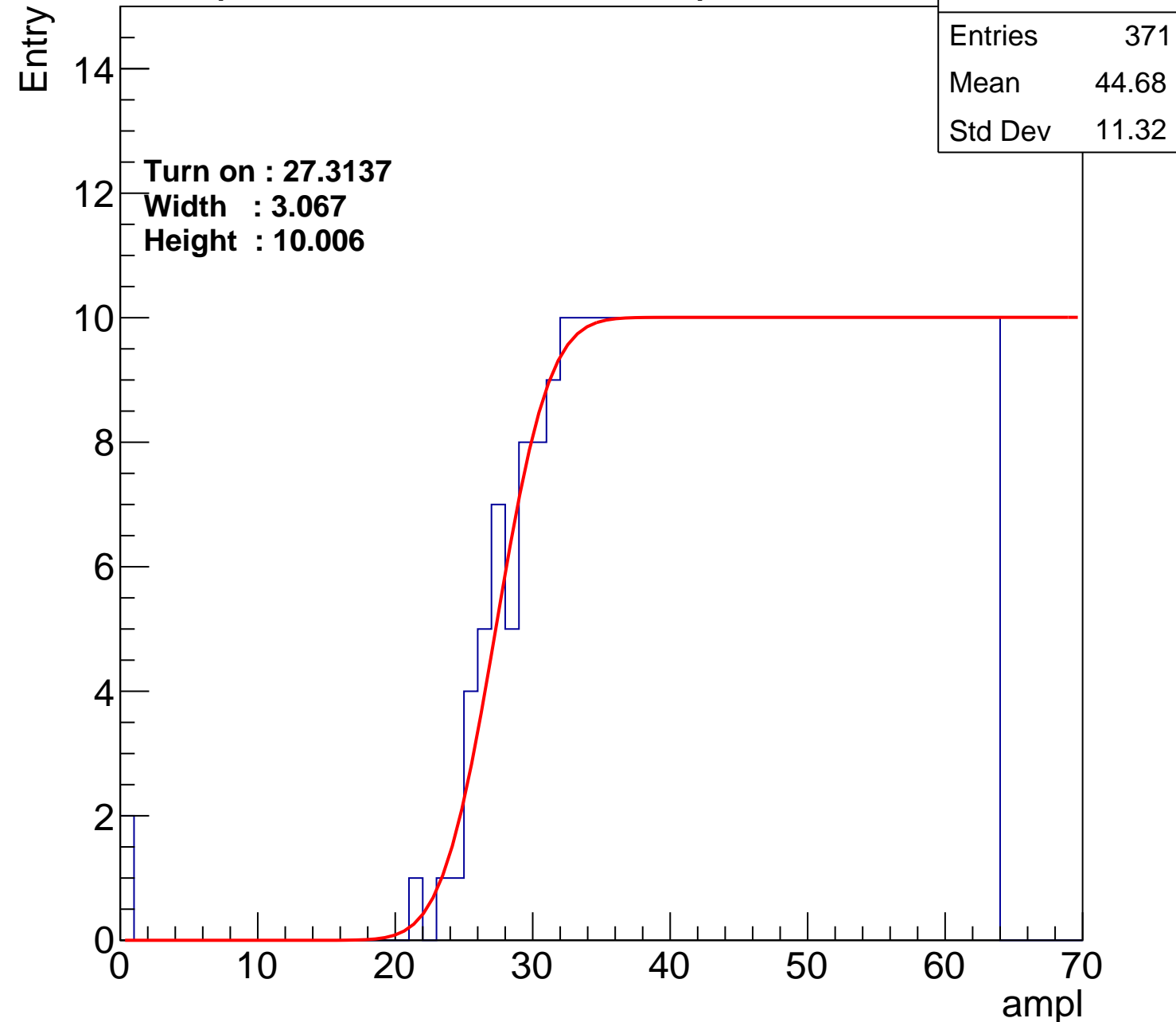
Width : 3.067

Height : 10.006

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch5

calib_packv5_042523_0143.root, FC#7, port C2

Entries	378
Mean	44.28
Std Dev	11.67

Turn on : 26.6872

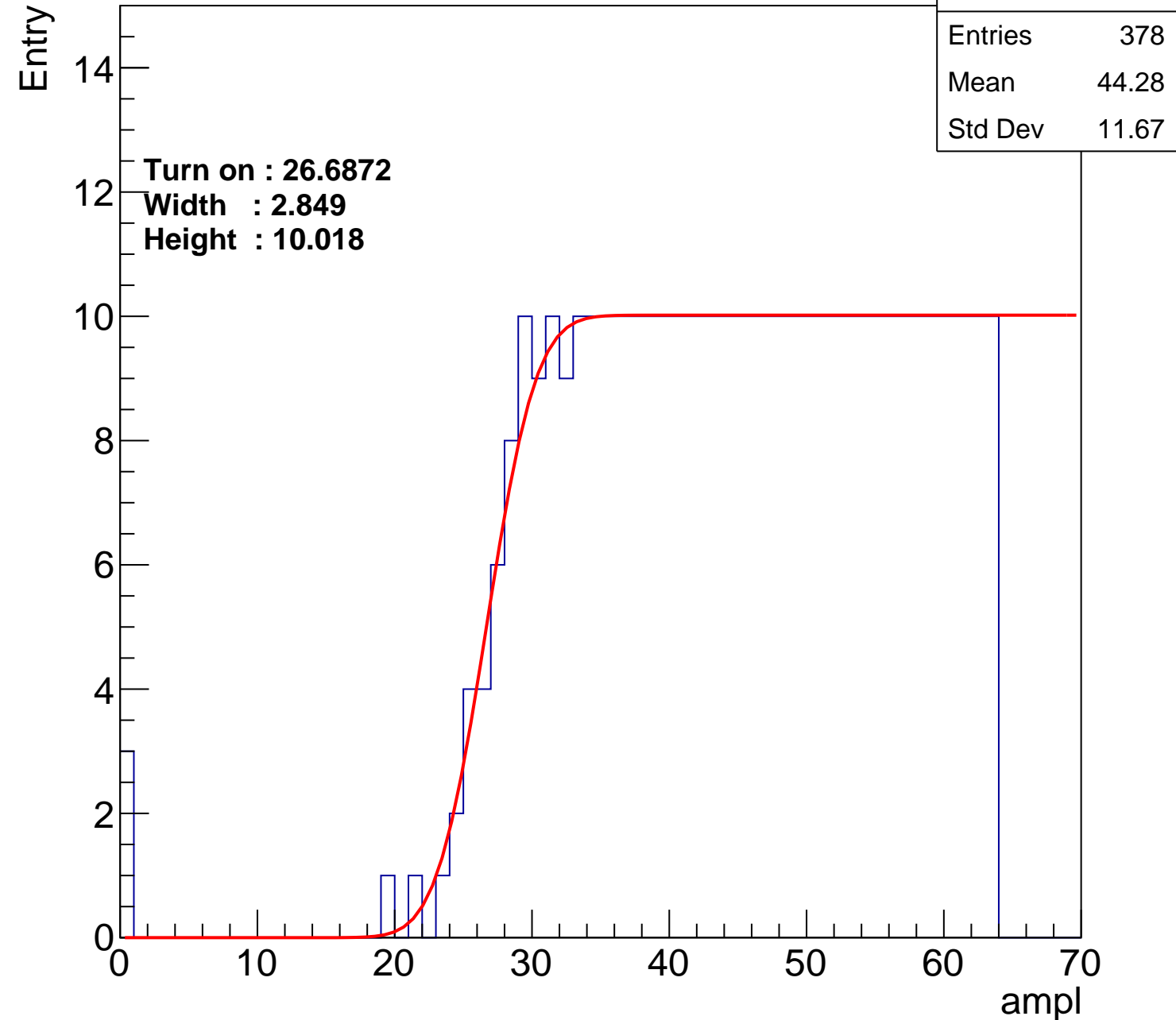
Width : 2.849

Height : 10.018

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch6

calib_packv5_042523_0143.root, FC#7, port C2

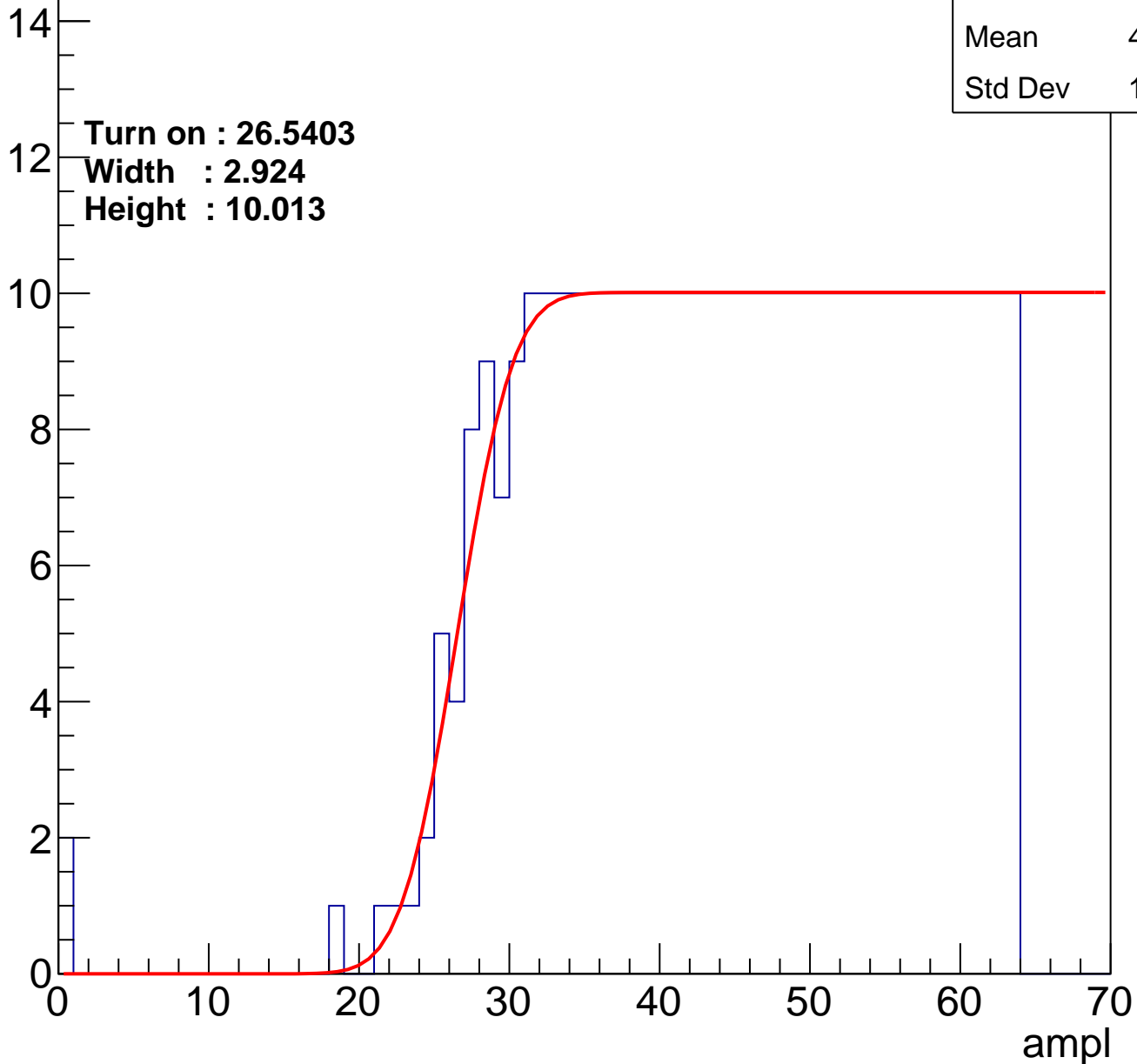
Entries	380
Mean	44.24
Std Dev	11.55

Turn on : 26.5403

Width : 2.924

Height : 10.013

Entry



B1L103S, U2-ch7

calib_packv5_042523_0143.root, FC#7, port C2

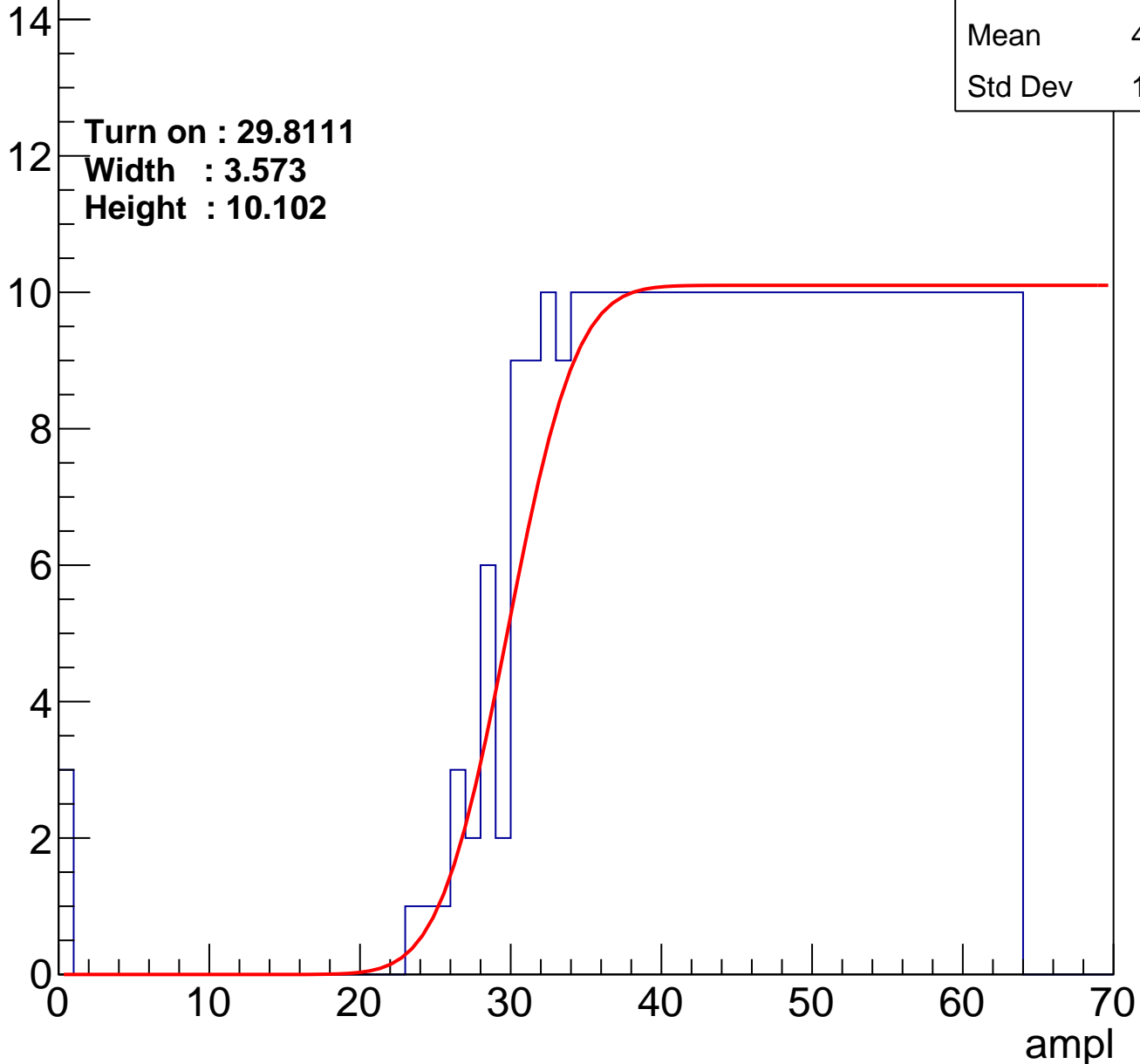
Entries	356
Mean	45.35
Std Dev	11.15

Turn on : 29.8111

Width : 3.573

Height : 10.102

Entry



B1L103S, U2-ch8

calib_packv5_042523_0143.root, FC#7, port C2

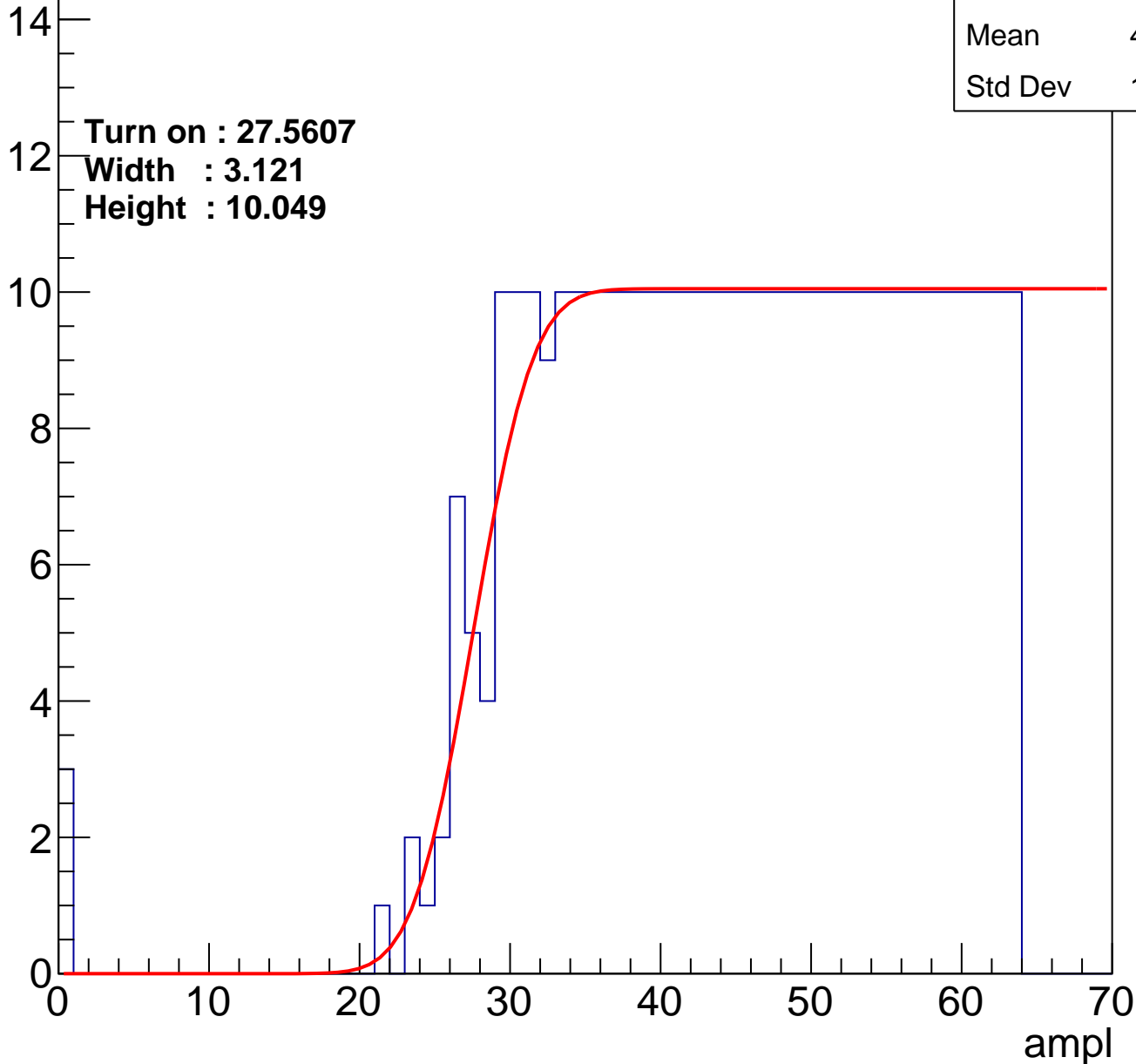
Entries	374
Mean	44.49
Std Dev	11.56

Turn on : 27.5607

Width : 3.121

Height : 10.049

Entry



B1L103S, U2-ch9

calib_packv5_042523_0143.root, FC#7, port C2

Entries	376
Mean	44.18
Std Dev	12.15

Turn on : 26.9475

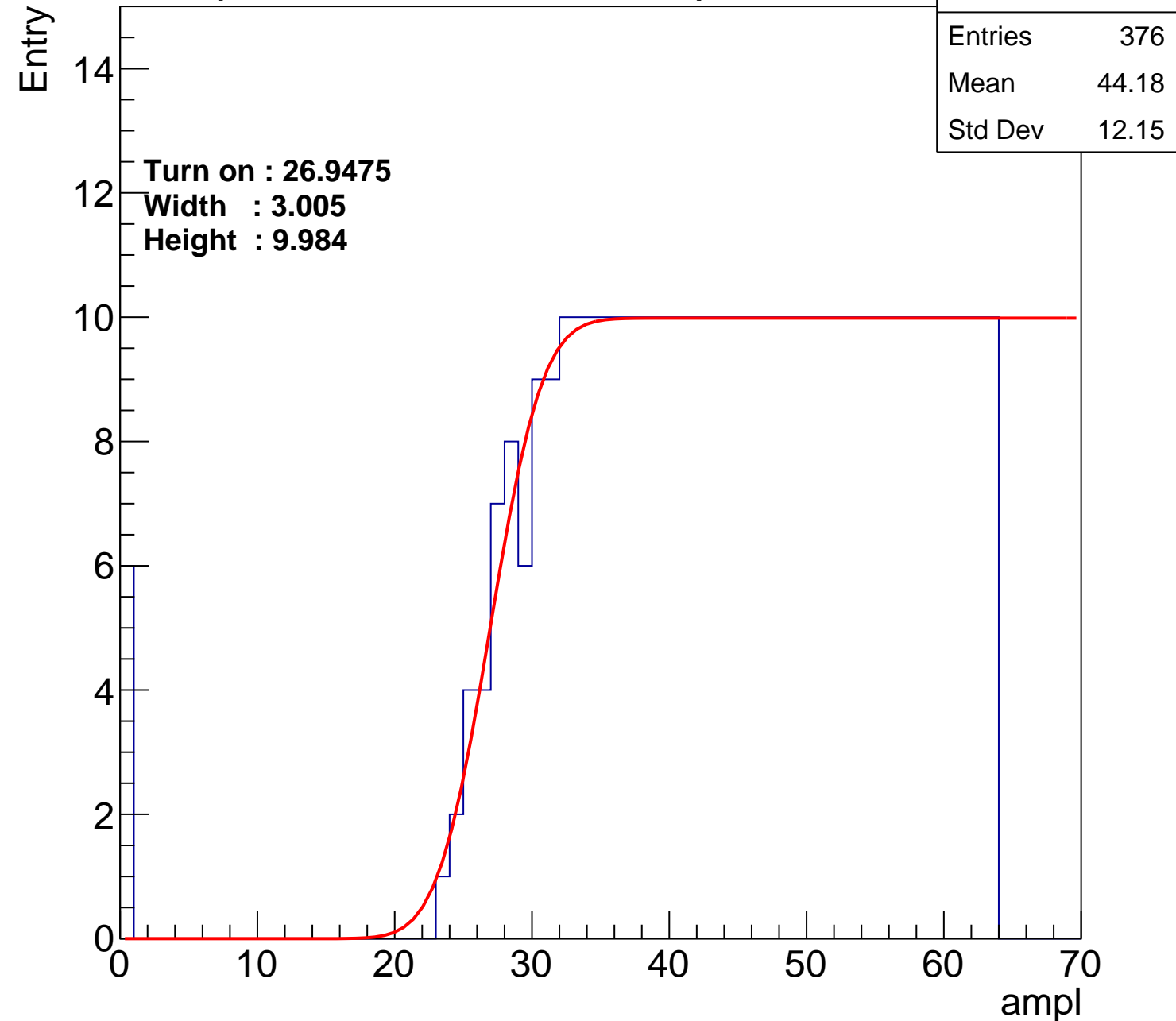
Width : 3.005

Height : 9.984

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch10

calib_packv5_042523_0143.root, FC#7, port C2

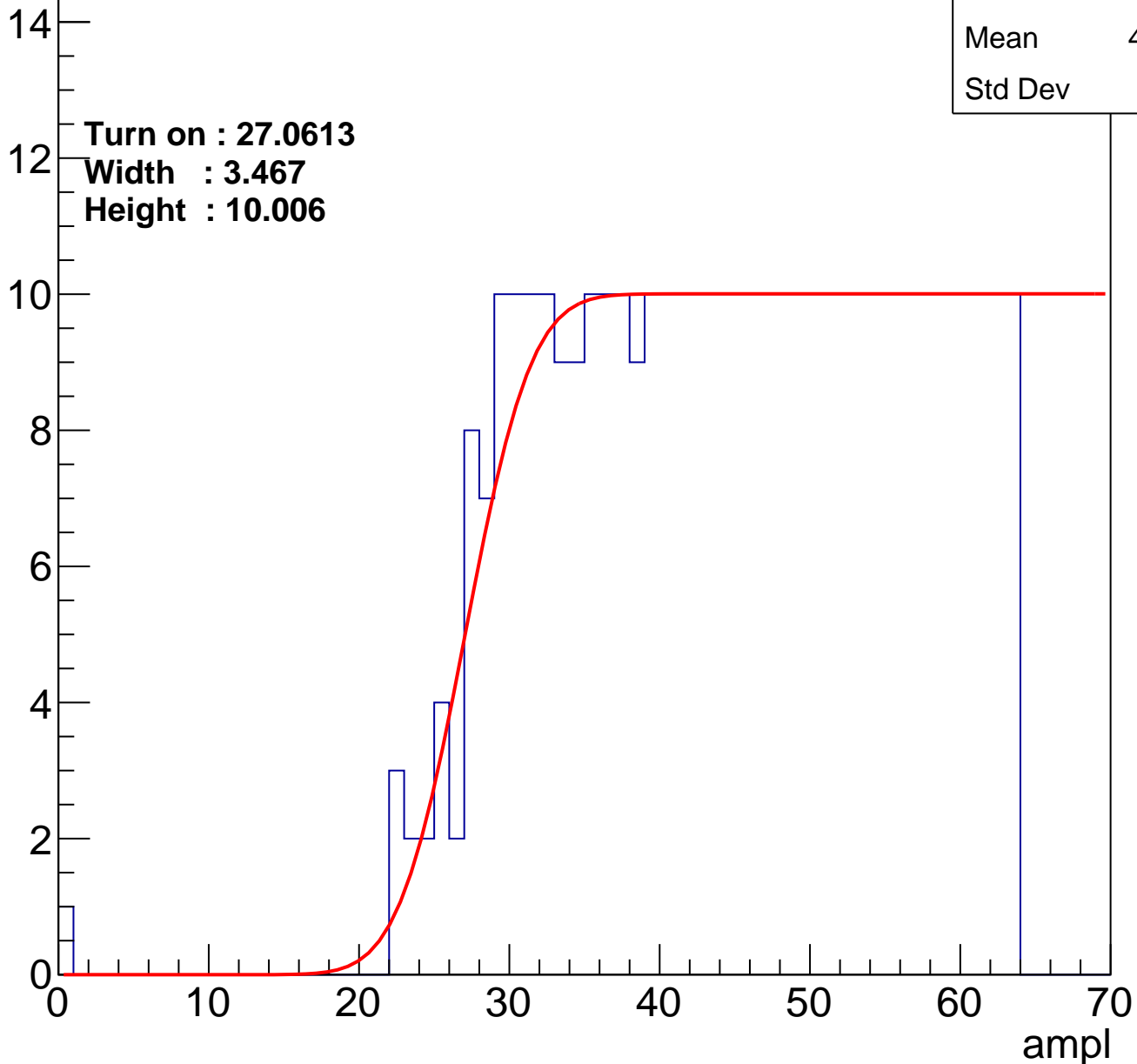
Entries	376
Mean	44.47
Std Dev	11.3

Turn on : 27.0613

Width : 3.467

Height : 10.006

Entry



B1L103S, U2-ch11

calib_packv5_042523_0143.root, FC#7, port C2

Entries	390
Mean	43.63
Std Dev	12.12

Turn on : 25.8680

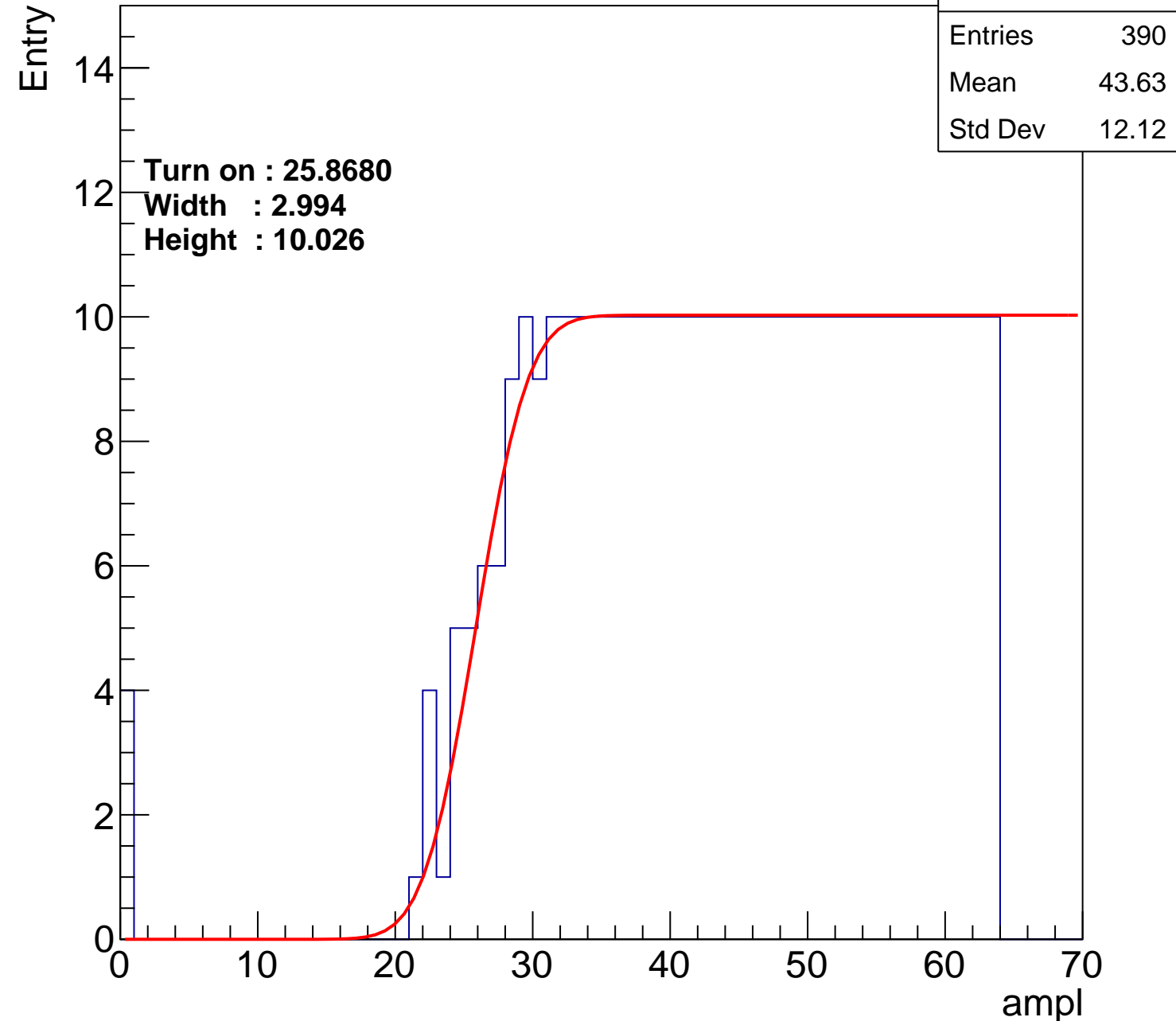
Width : 2.994

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch12

calib_packv5_042523_0143.root, FC#7, port C2

Entries	379
Mean	44.28
Std Dev	11.55

Turn on : 27.4447

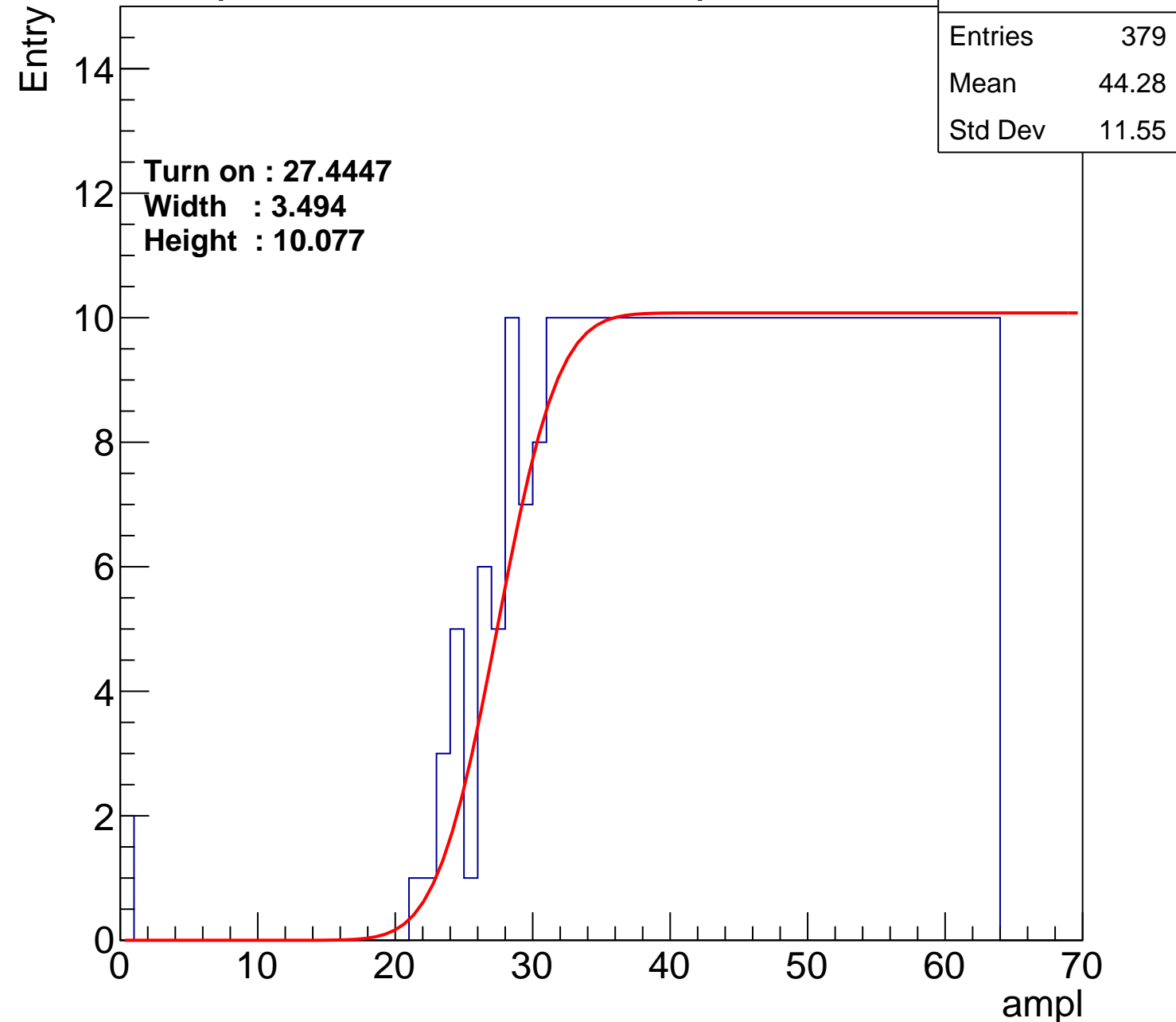
Width : 3.494

Height : 10.077

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch13

calib_packv5_042523_0143.root, FC#7, port C2

Entries	378
Mean	44.24
Std Dev	11.81

Turn on : 26.6431

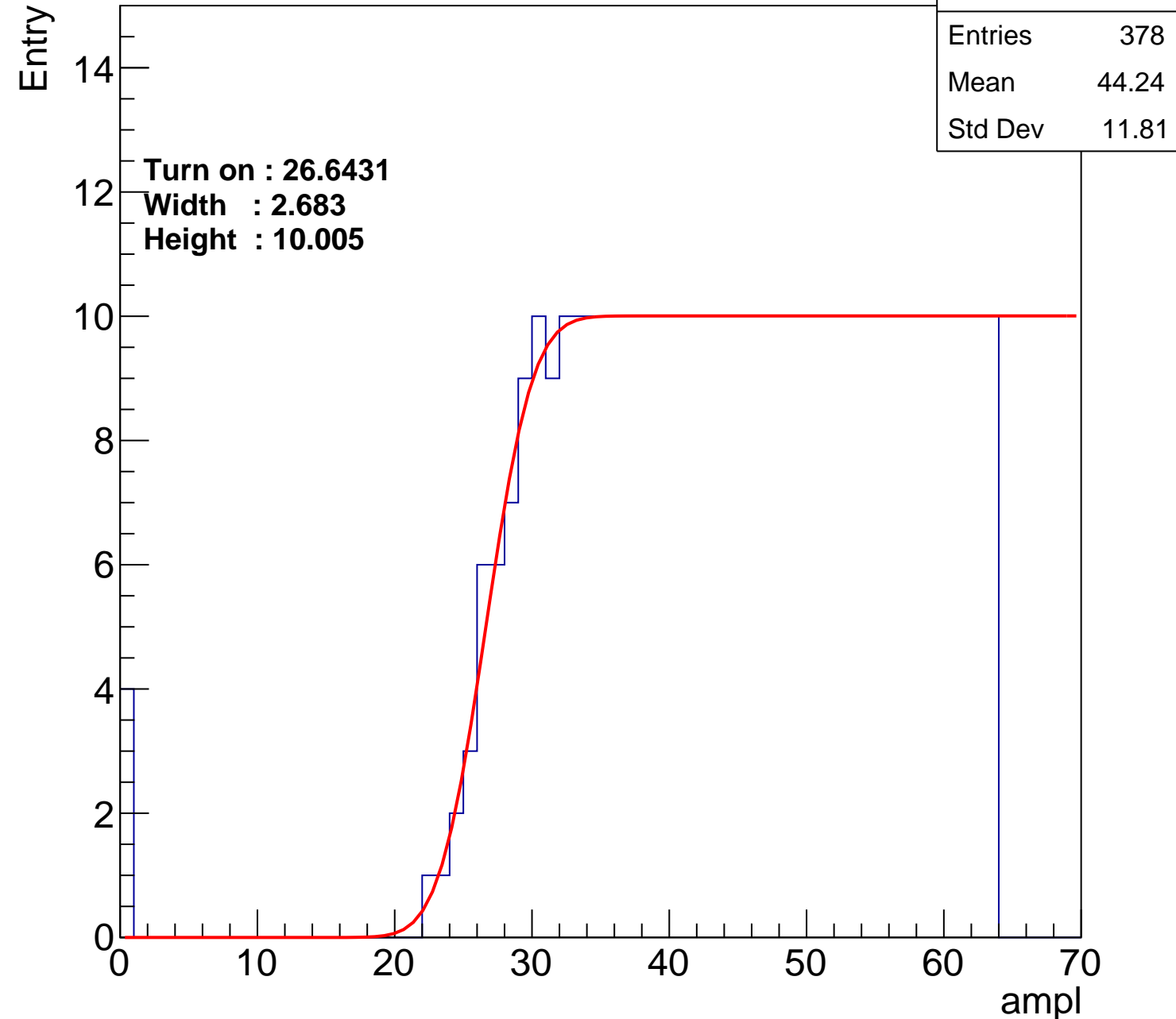
Width : 2.683

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch14

calib_packv5_042523_0143.root, FC#7, port C2

Entries	366
Mean	44.87
Std Dev	11.38

Turn on : 27.0326

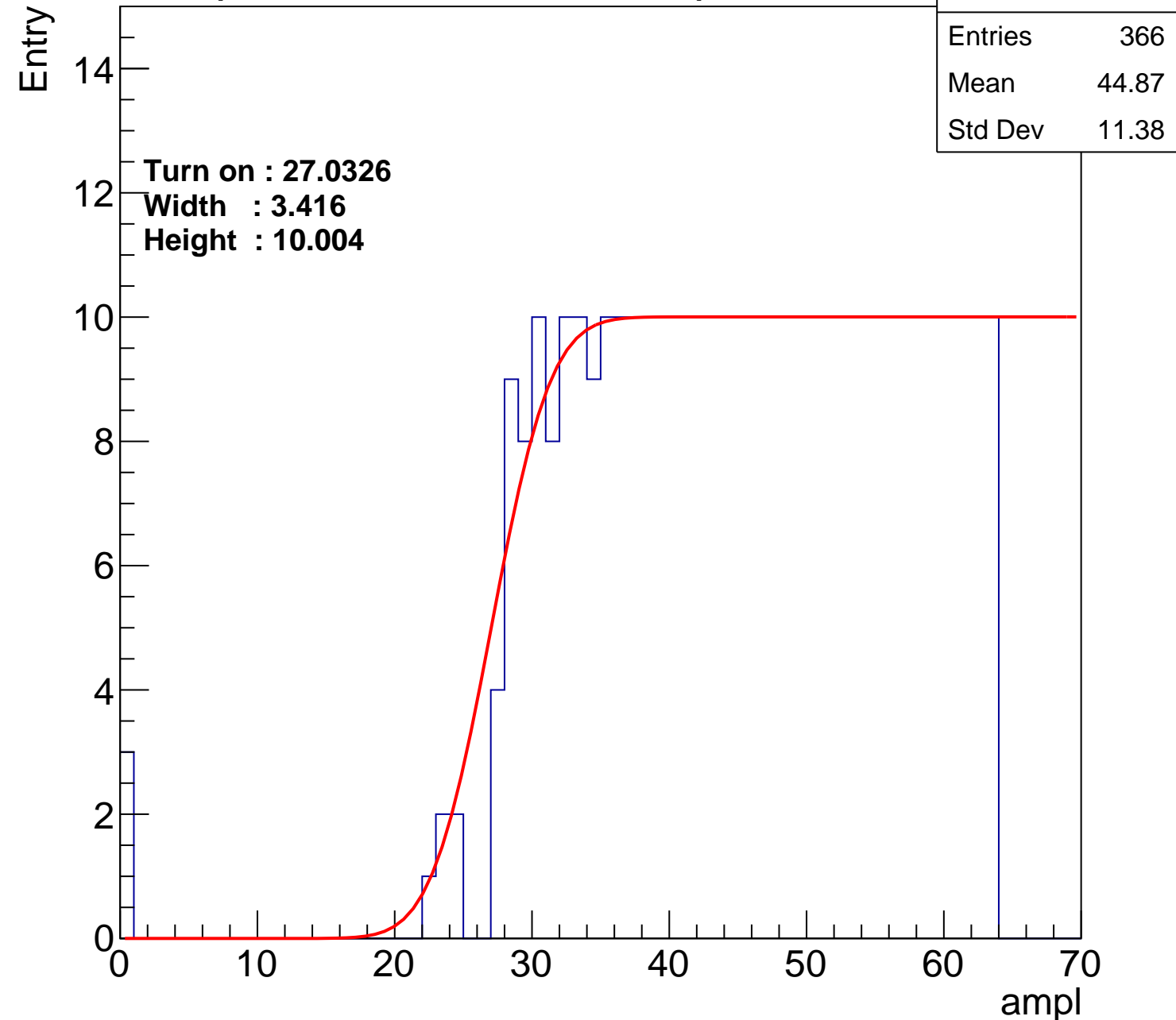
Width : 3.416

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch15

calib_packv5_042523_0143.root, FC#7, port C2

Entries	367
Mean	44.85
Std Dev	11.27

Turn on : 27.8233

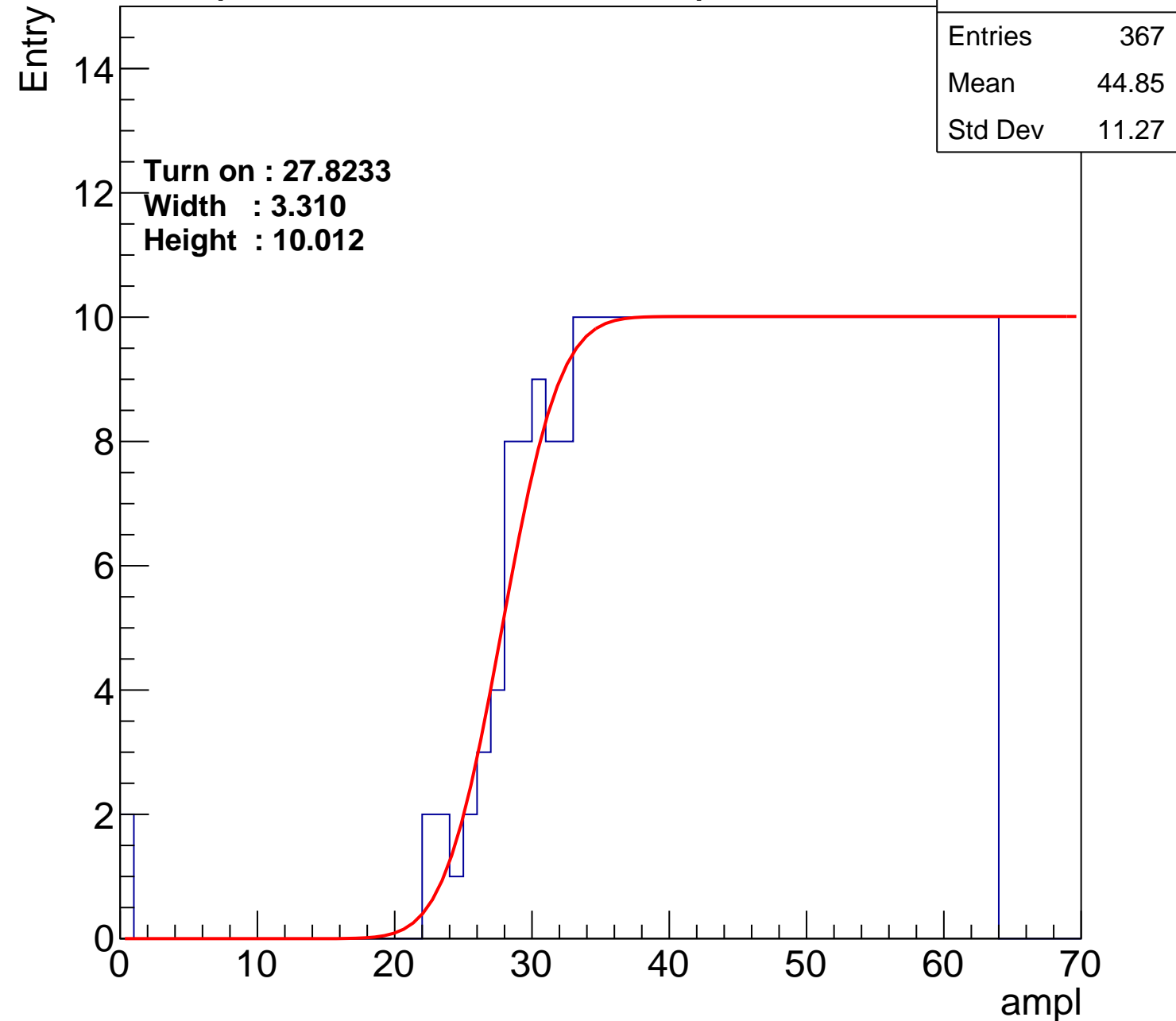
Width : 3.310

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch16

calib_packv5_042523_0143.root, FC#7, port C2

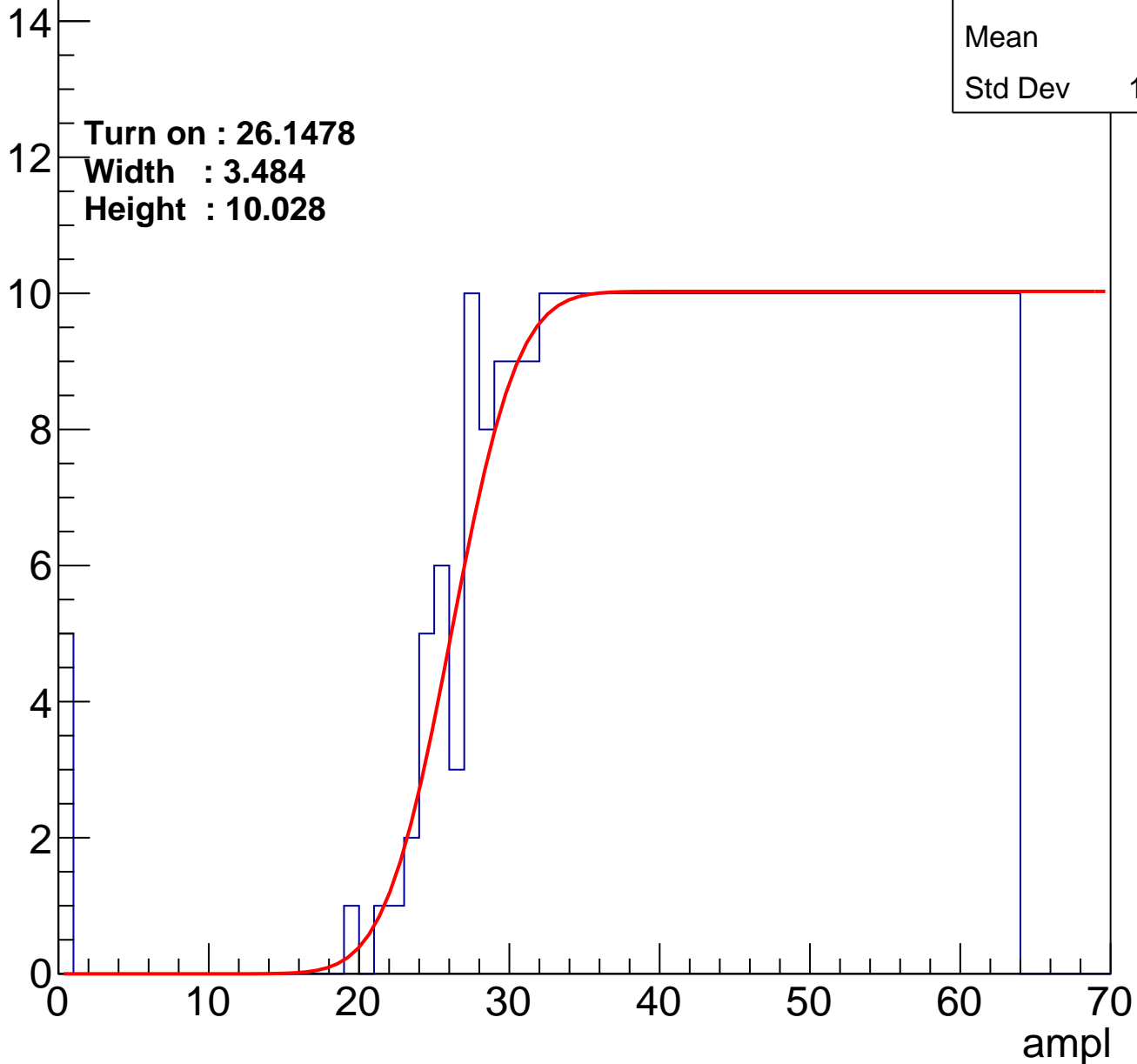
Entries	389
Mean	43.6
Std Dev	12.29

Turn on : 26.1478

Width : 3.484

Height : 10.028

Entry



B1L103S, U2-ch17

calib_packv5_042523_0143.root, FC#7, port C2

Entries	376
Mean	44.43
Std Dev	11.54

Turn on : 26.9100

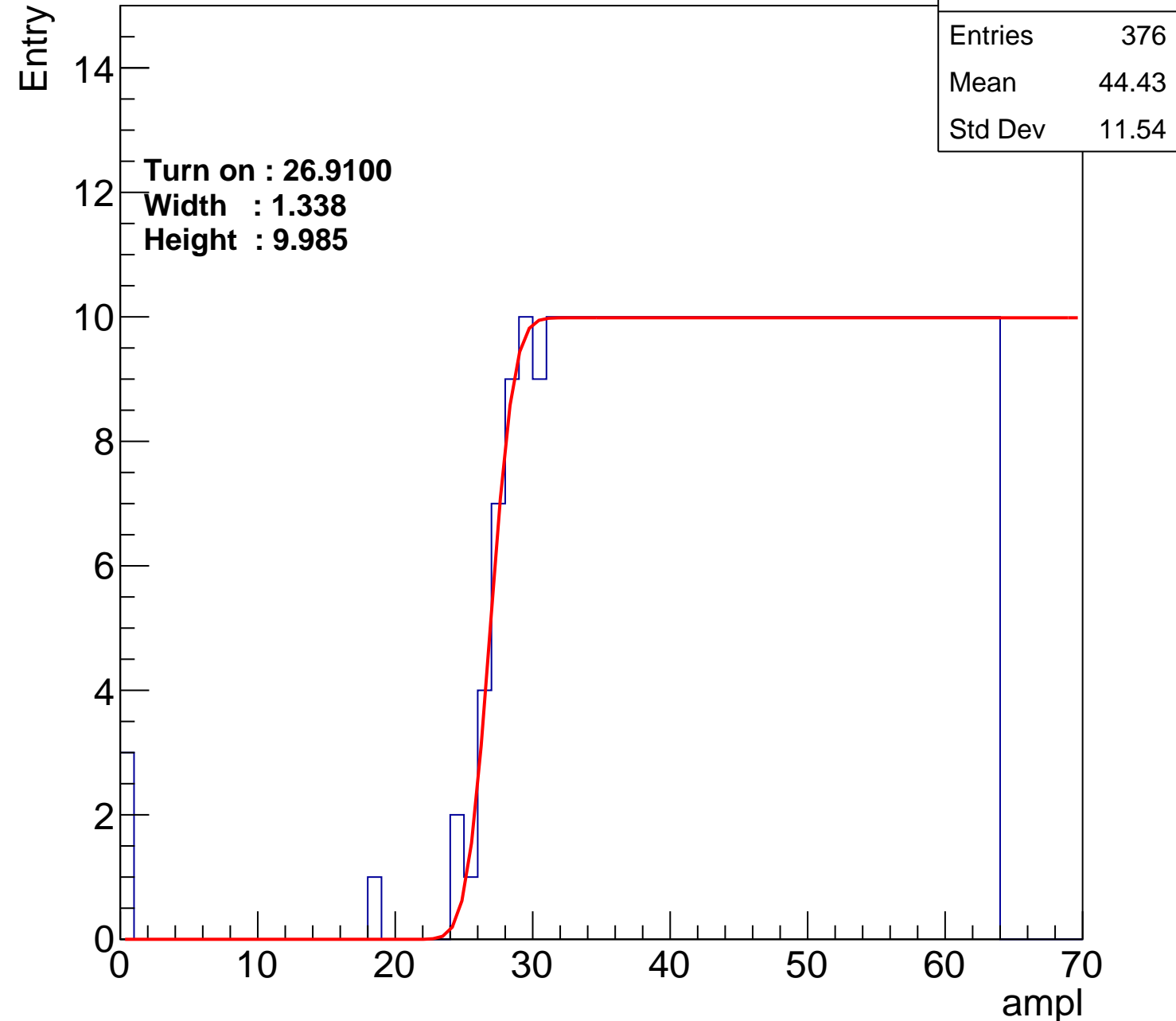
Width : 1.338

Height : 9.985

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch18

calib_packv5_042523_0143.root, FC#7, port C2

Entries	383
Mean	43.98
Std Dev	11.94

Turn on : 27.1593

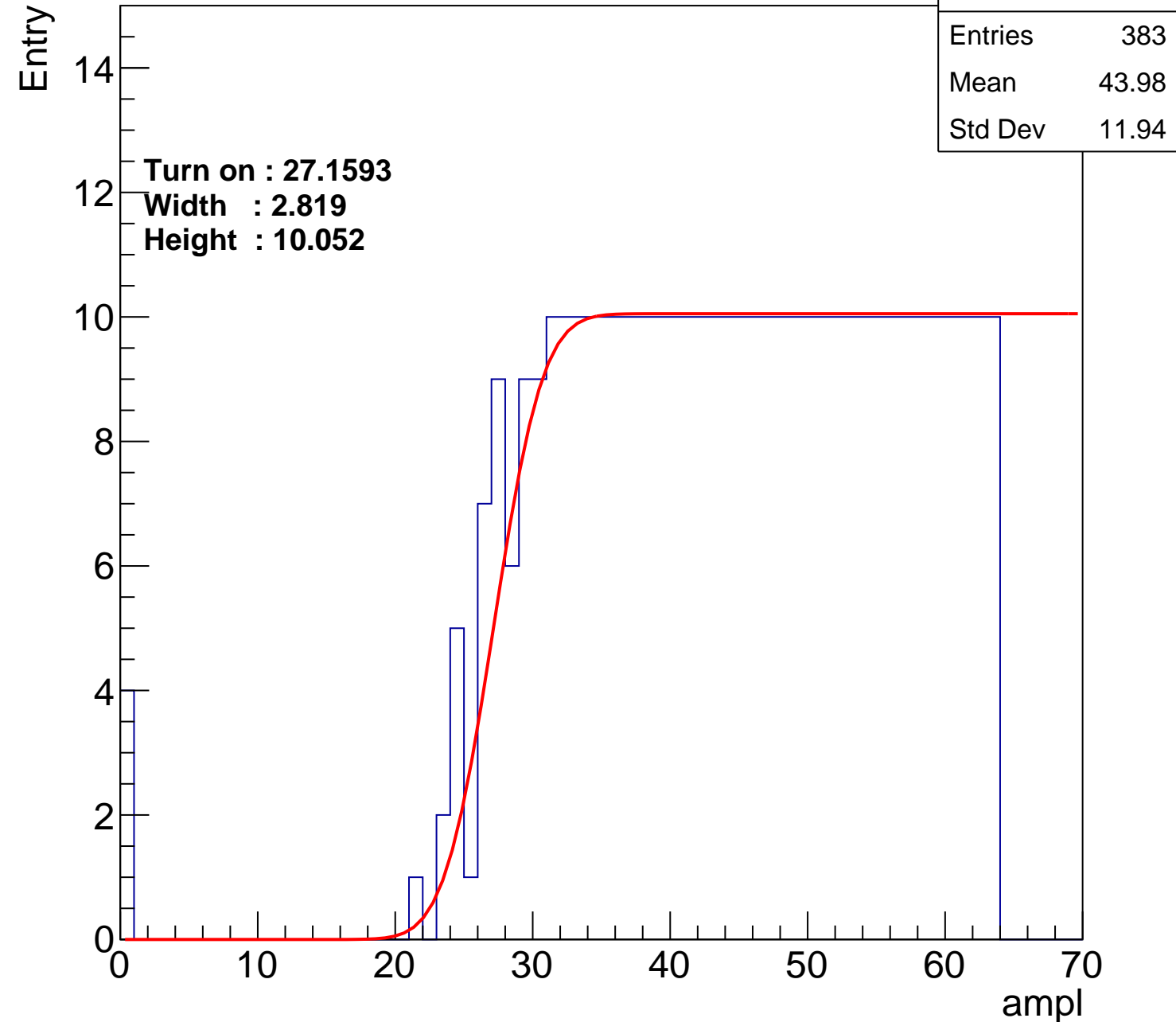
Width : 2.819

Height : 10.052

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch19

calib_packv5_042523_0143.root, FC#7, port C2

Entries	381
Mean	44.07
Std Dev	11.92

Turn on : 26.1678

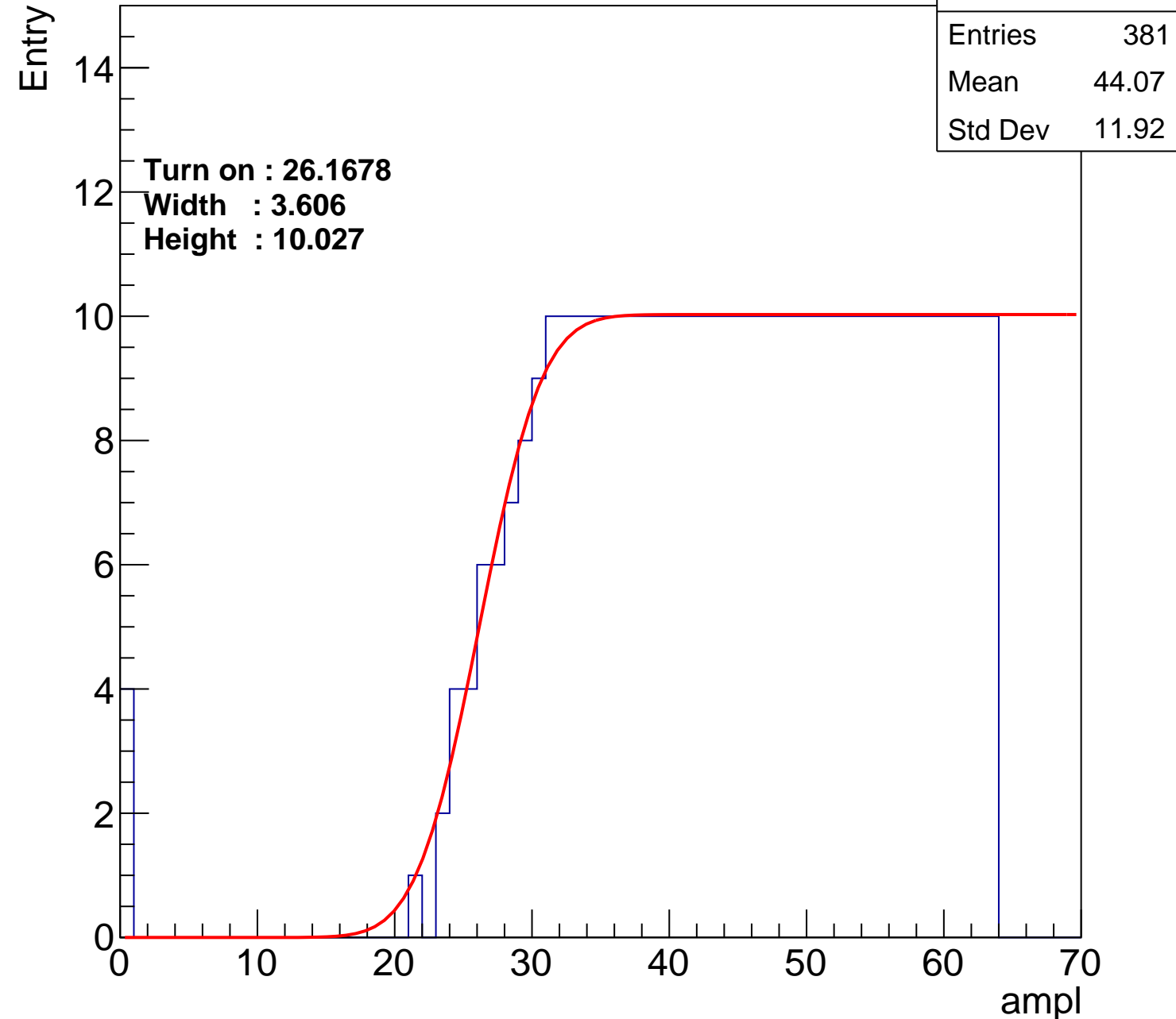
Width : 3.606

Height : 10.027

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch20

calib_packv5_042523_0143.root, FC#7, port C2

Entries	385
Mean	43.91
Std Dev	11.88

Turn on : 26.1175

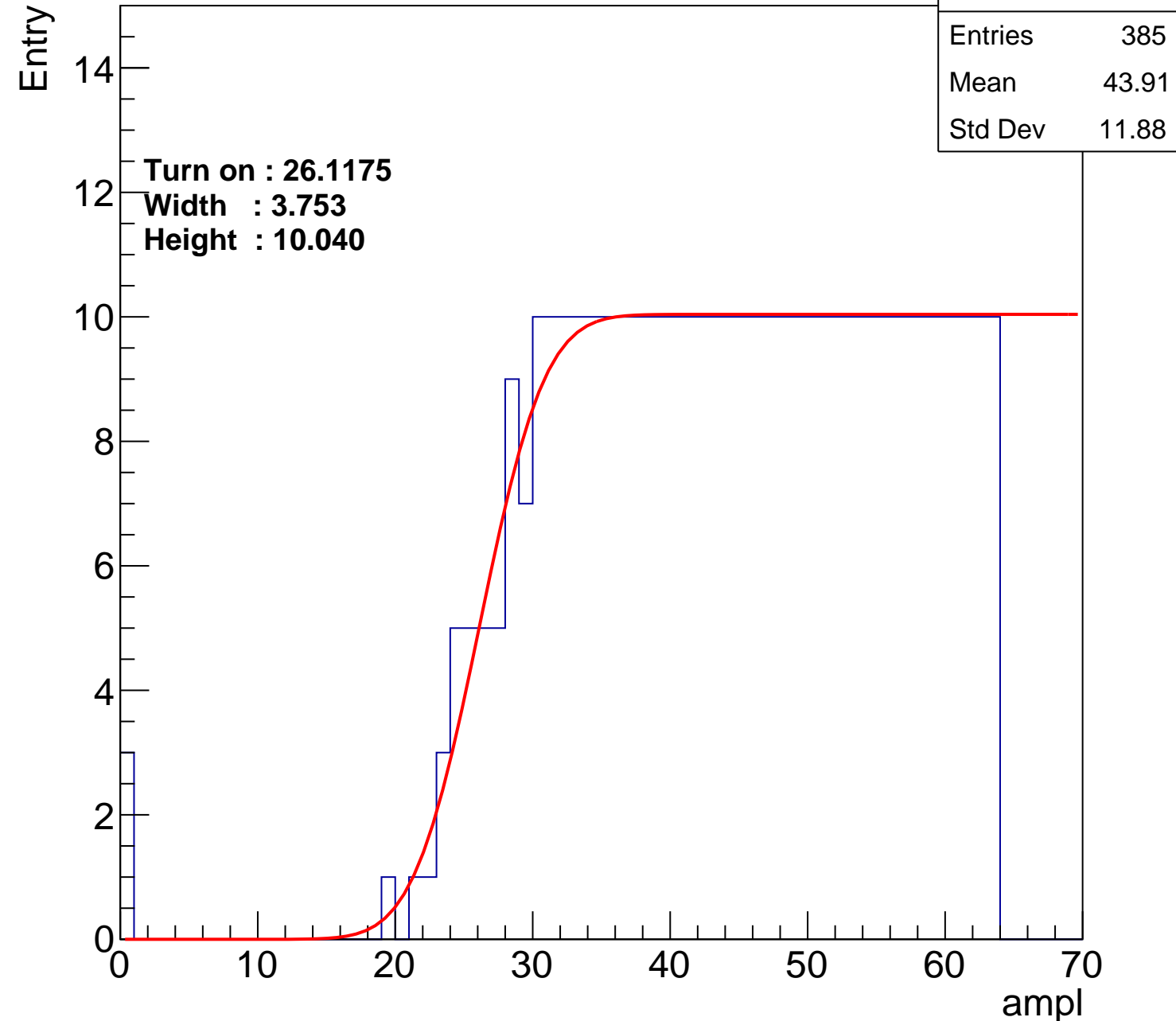
Width : 3.753

Height : 10.040

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch21

calib_packv5_042523_0143.root, FC#7, port C2

Entries	380
Mean	44.23
Std Dev	11.55

Turn on : 26.1842

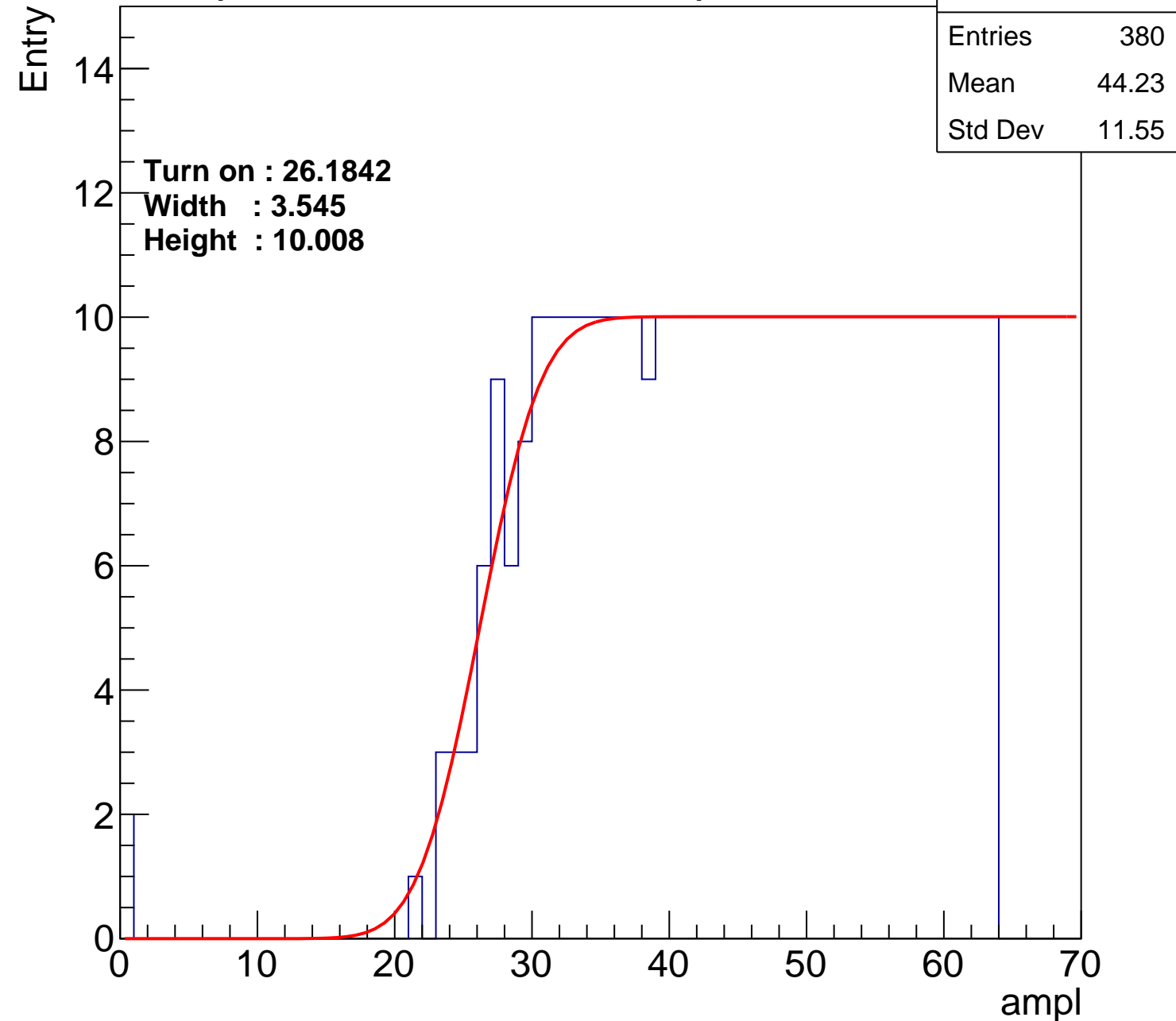
Width : 3.545

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch22

calib_packv5_042523_0143.root, FC#7, port C2

Entries	406
Mean	42.92
Std Dev	12.34

Turn on : 23.9680

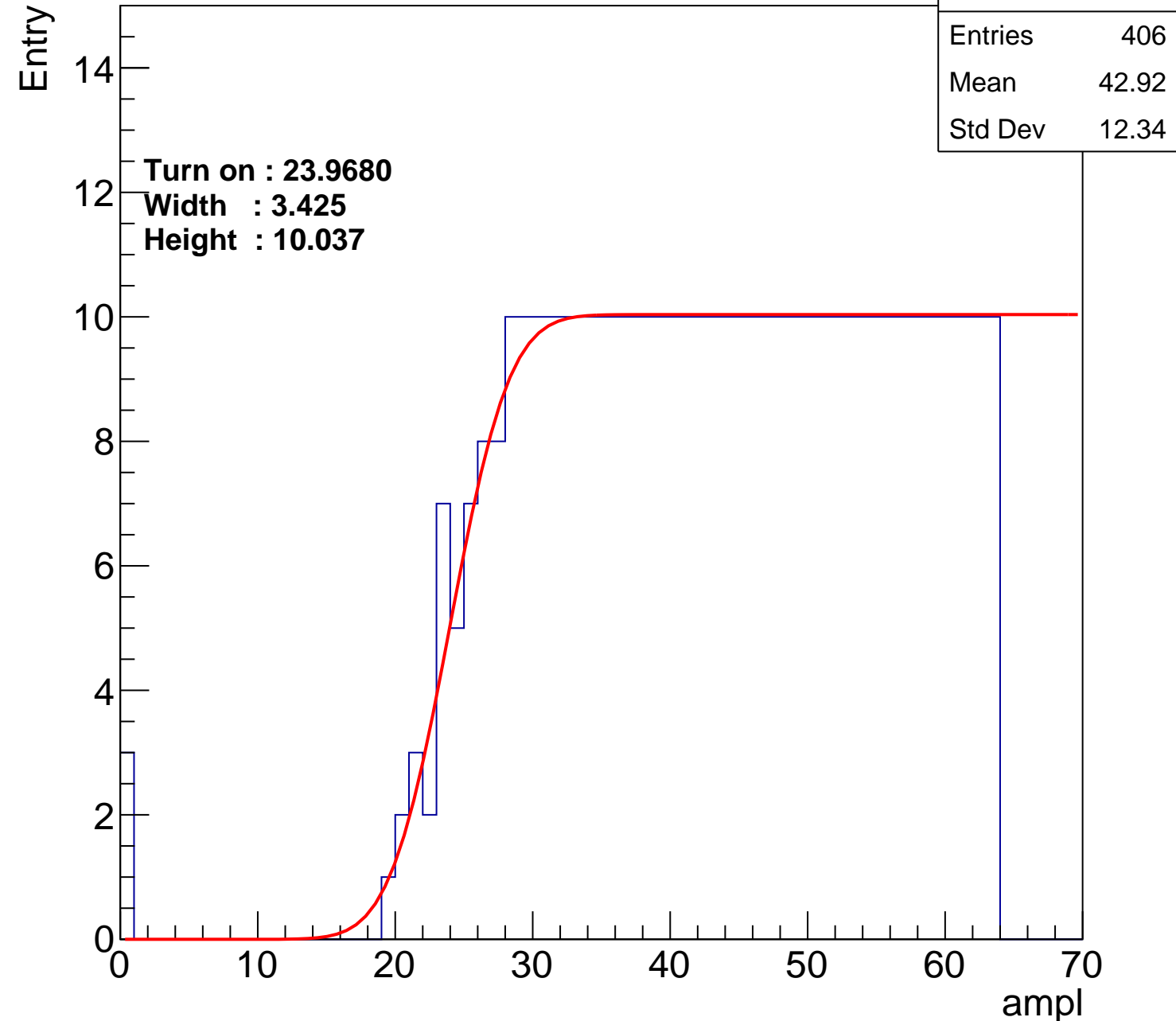
Width : 3.425

Height : 10.037

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch23

calib_packv5_042523_0143.root, FC#7, port C2

Entries	384
Mean	43.93
Std Dev	11.97

Turn on : 26.4488

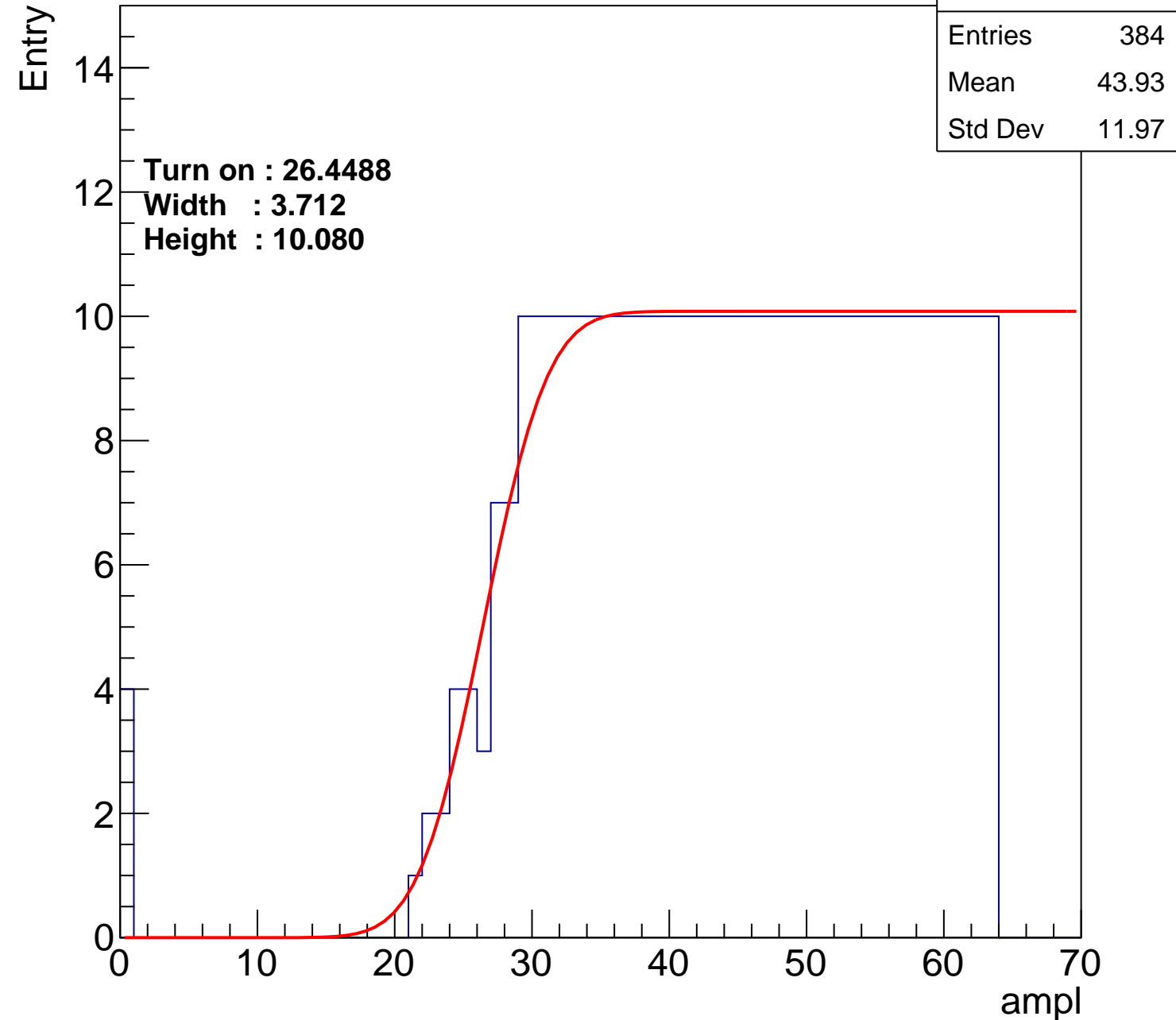
Width : 3.712

Height : 10.080

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch24

calib_packv5_042523_0143.root, FC#7, port C2

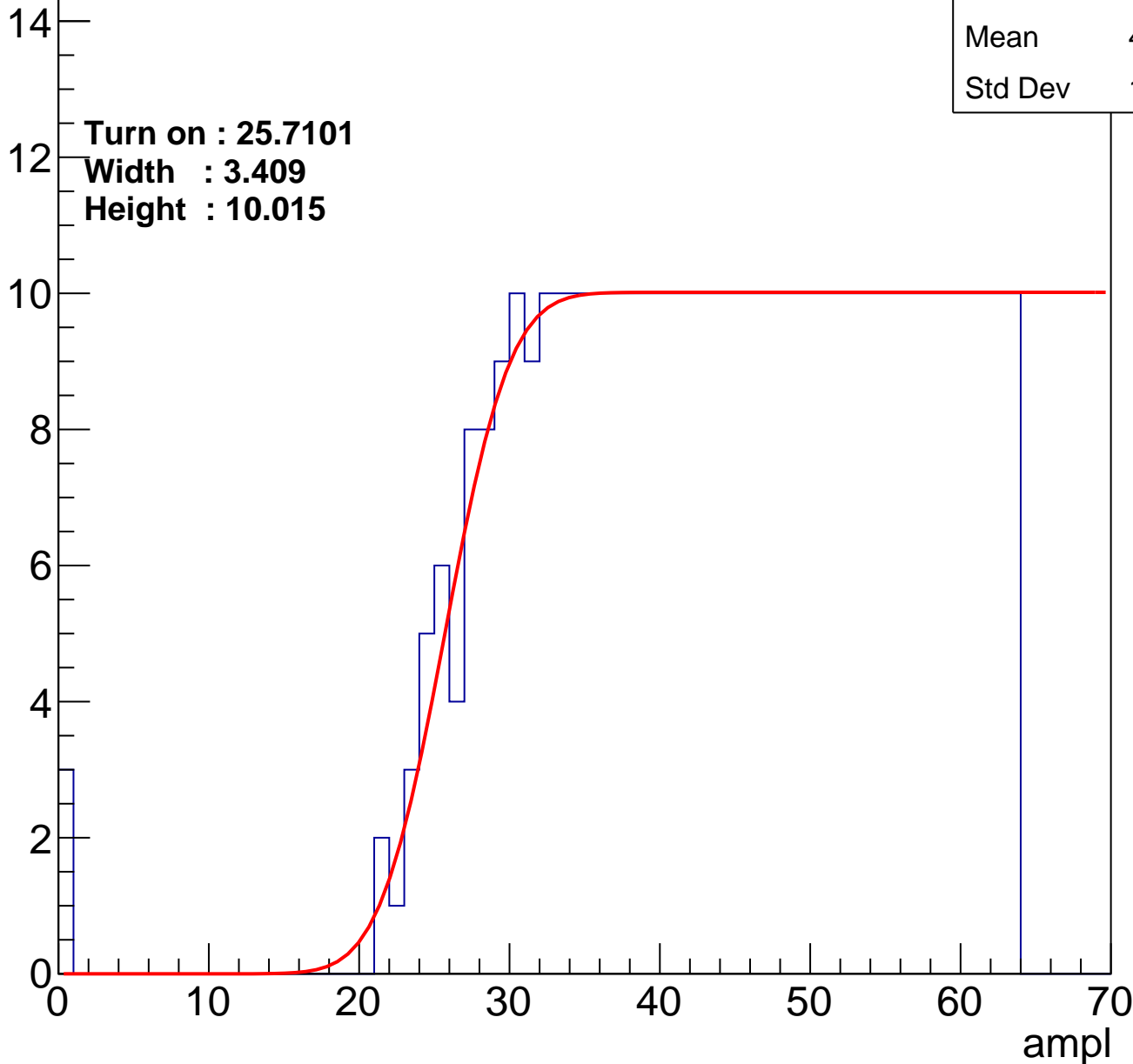
Entries	388
Mean	43.78
Std Dev	11.93

Turn on : 25.7101

Width : 3.409

Height : 10.015

Entry



B1L103S, U2-ch25

calib_packv5_042523_0143.root, FC#7, port C2

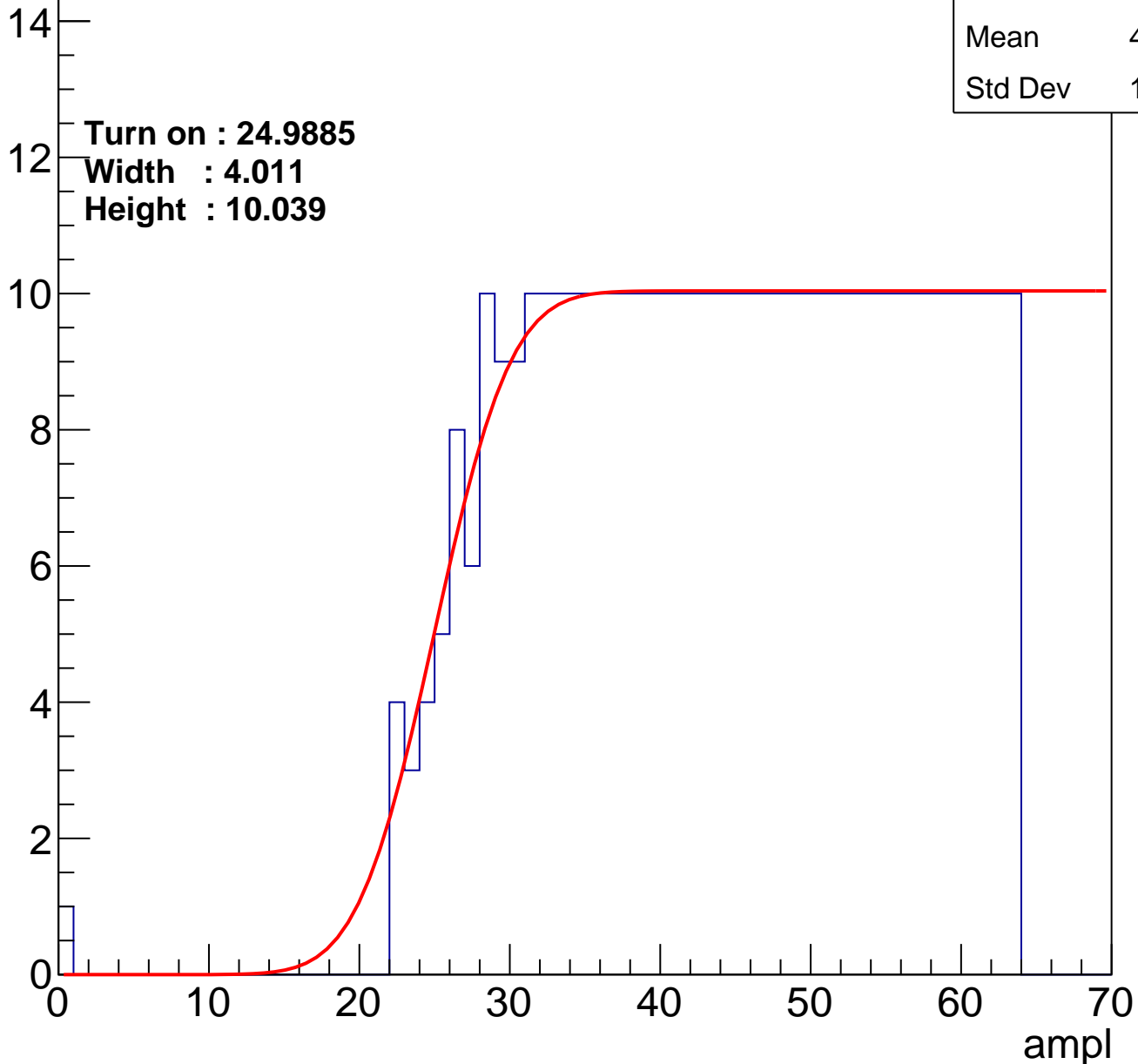
Entries	389
Mean	43.88
Std Dev	11.58

Turn on : 24.9885

Width : 4.011

Height : 10.039

Entry



B1L103S, U2-ch26

calib_packv5_042523_0143.root, FC#7, port C2

Entries	380
Mean	44.31
Std Dev	11.36

Turn on : 26.9923

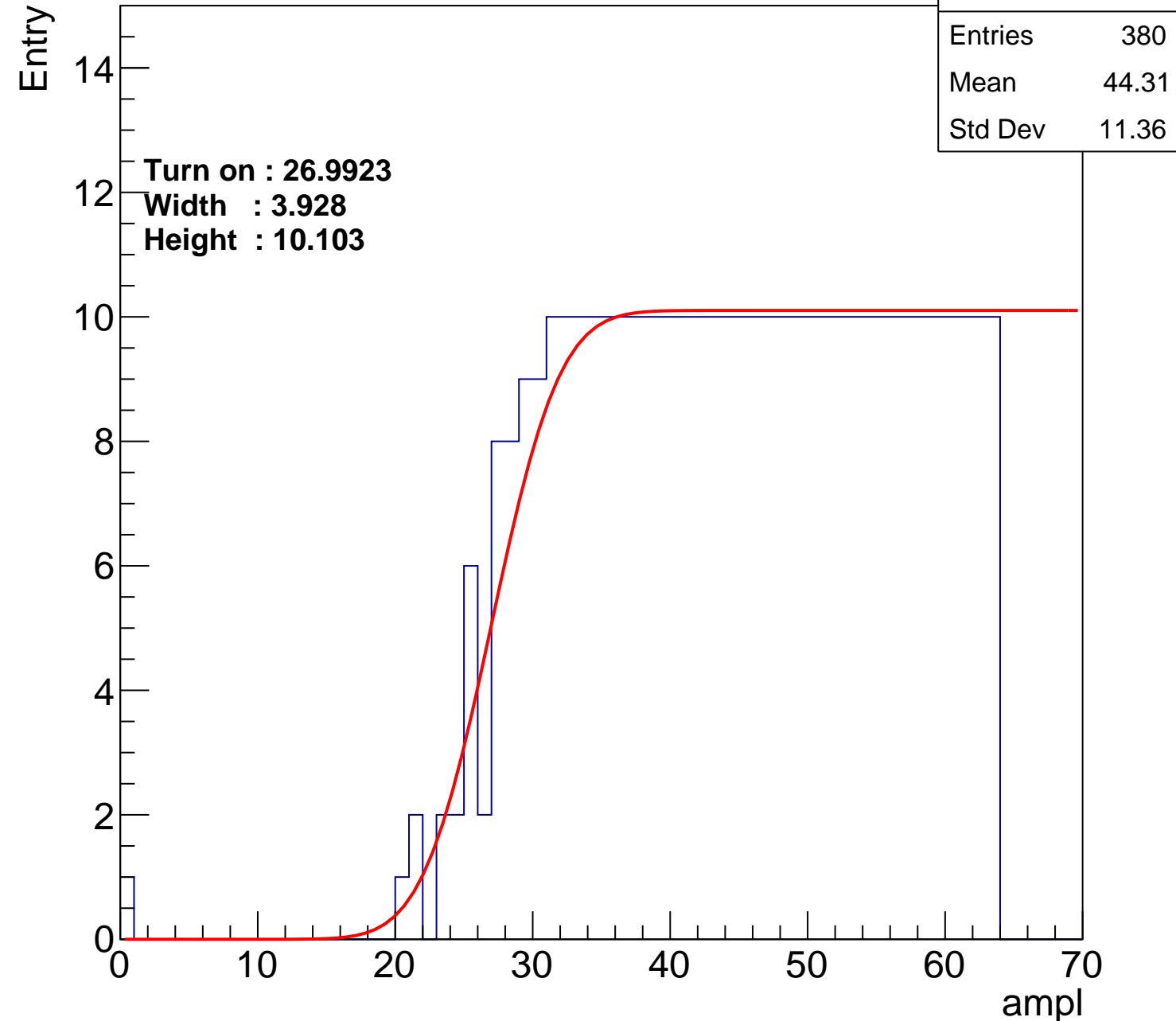
Width : 3.928

Height : 10.103

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch27

calib_packv5_042523_0143.root, FC#7, port C2

Entries	373
Mean	44.47
Std Dev	11.72

Turn on : 27.4325

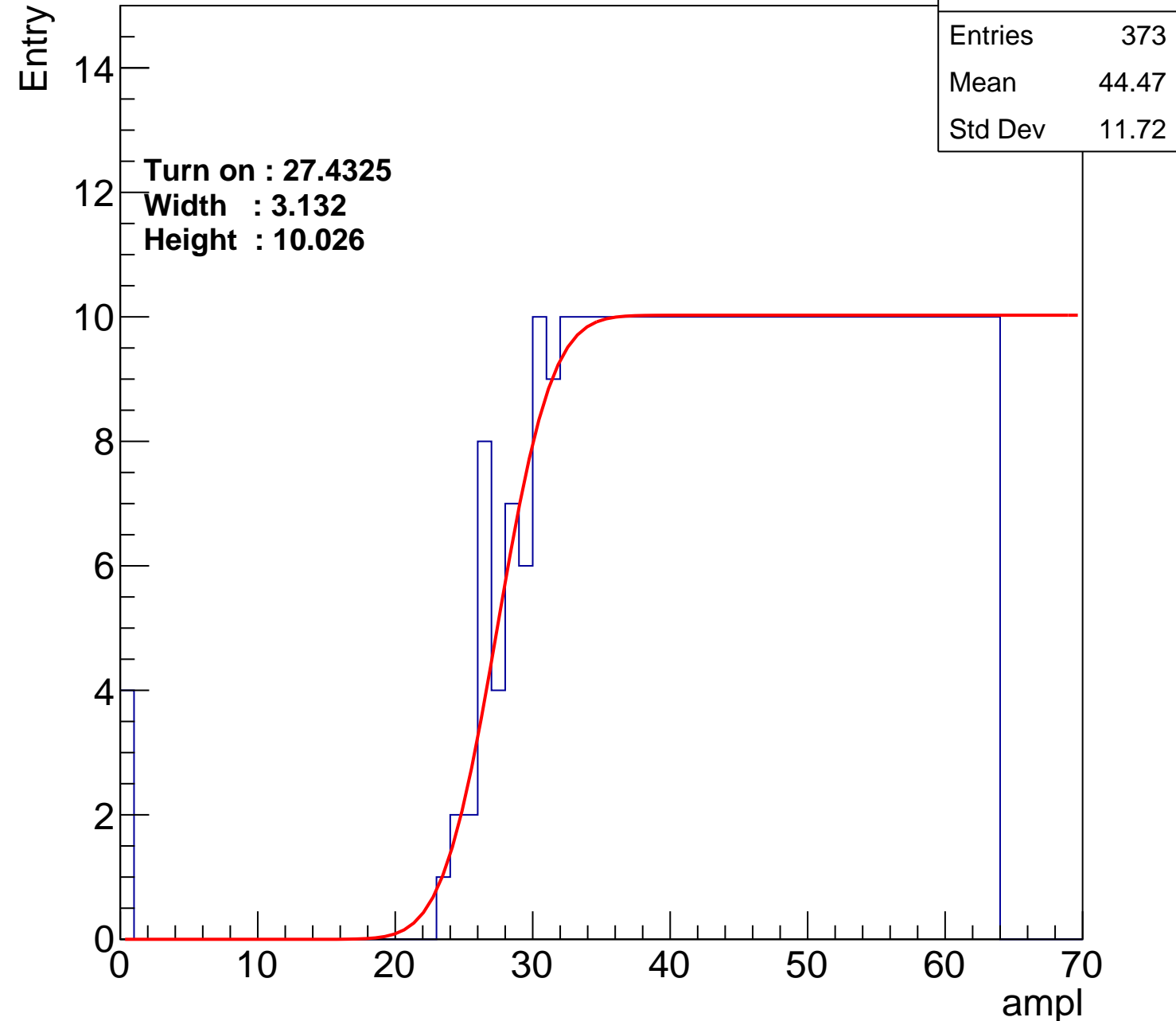
Width : 3.132

Height : 10.026

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch28

calib_packv5_042523_0143.root, FC#7, port C2

Entries	390
Mean	43.65
Std Dev	12.1

Turn on : 25.6656

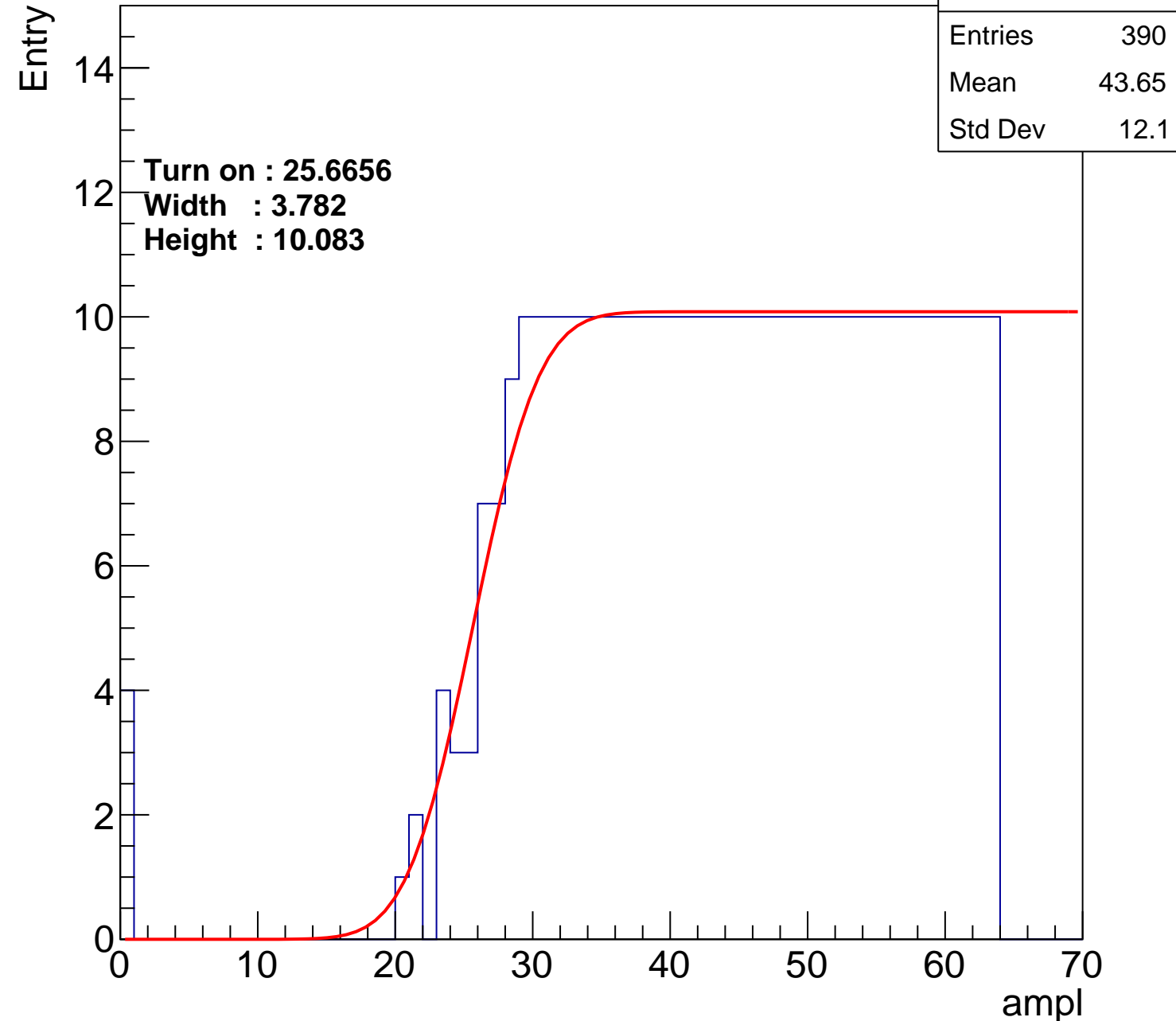
Width : 3.782

Height : 10.083

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch29

calib_packv5_042523_0143.root, FC#7, port C2

Entries	378
Mean	44.46
Std Dev	11.24

Turn on : 26.4965

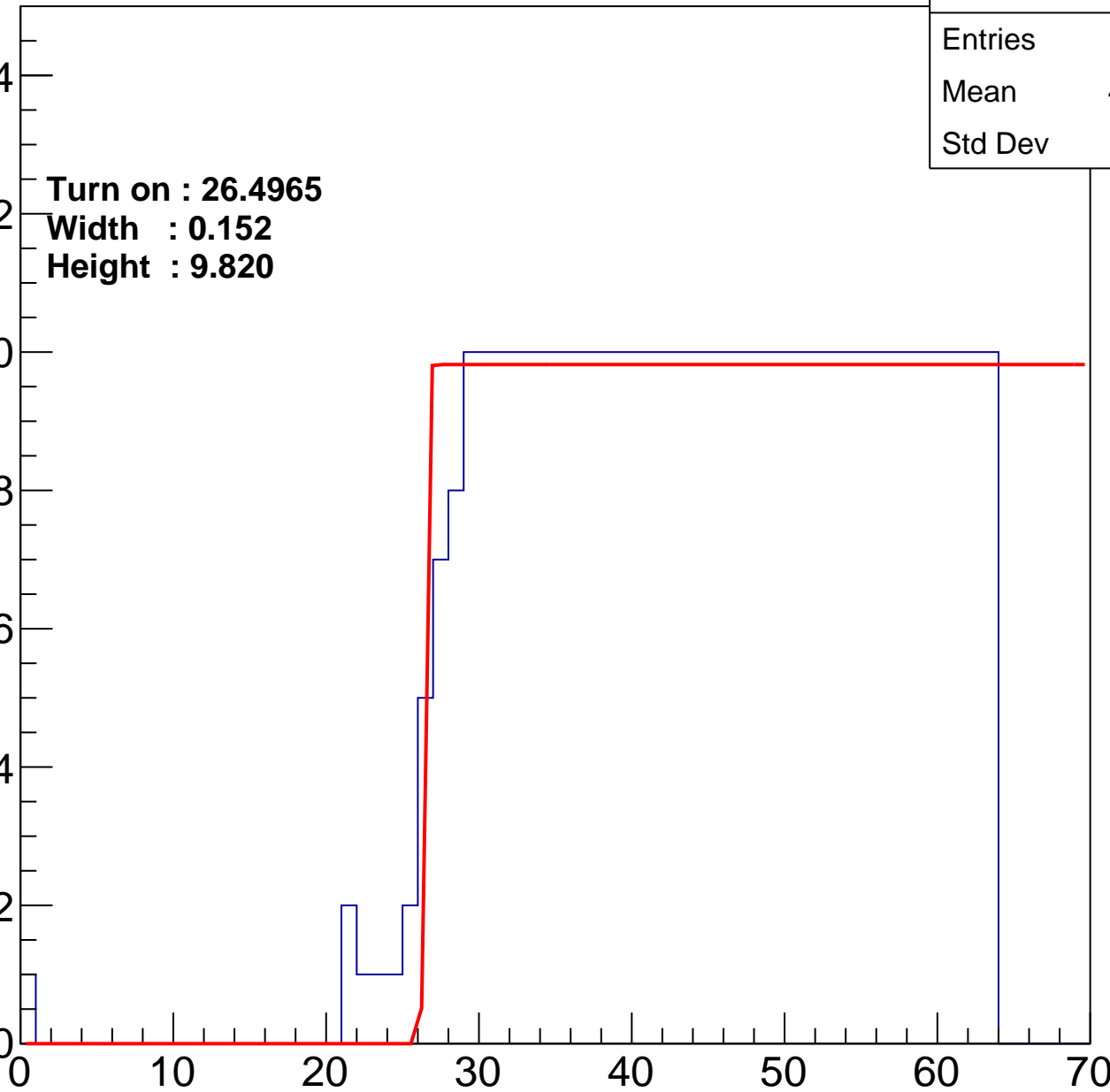
Width : 0.152

Height : 9.820

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch30

calib_packv5_042523_0143.root, FC#7, port C2

Entries	407
Mean	42.93
Std Dev	12.22

Turn on : 23.4404

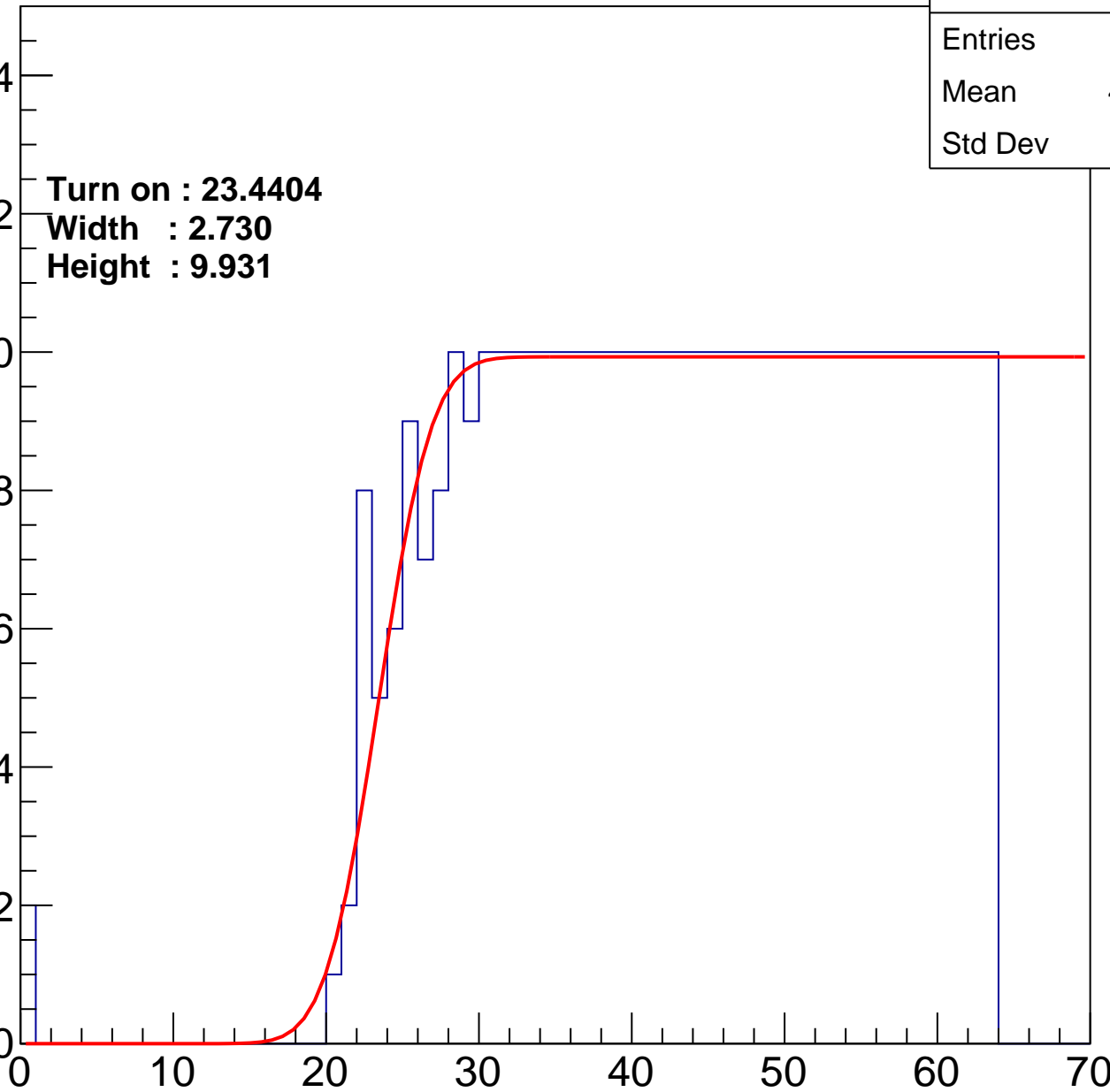
Width : 2.730

Height : 9.931

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch31

calib_packv5_042523_0143.root, FC#7, port C2

Entries	388
Mean	43.84
Std Dev	11.83

Turn on : 25.5114

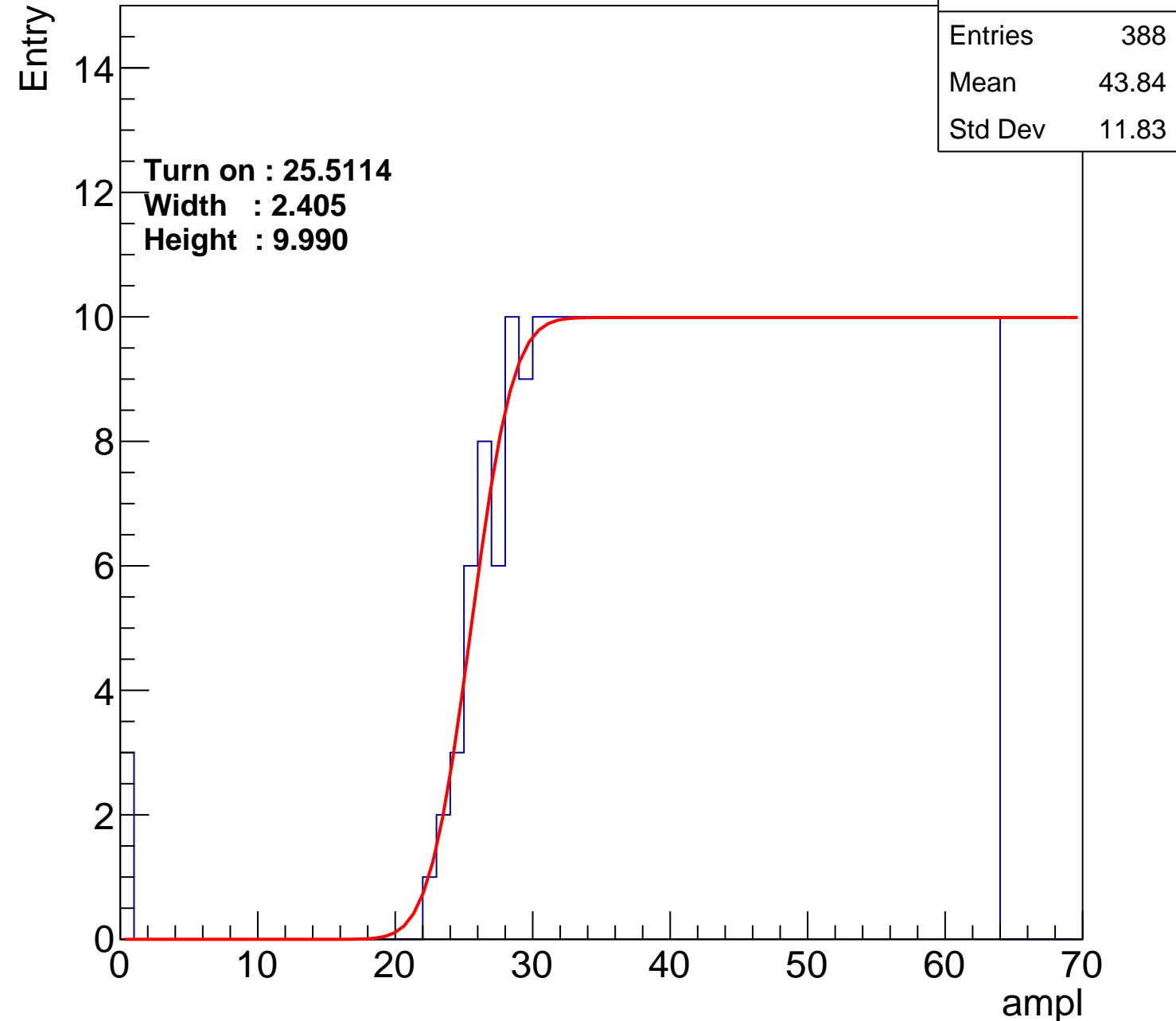
Width : 2.405

Height : 9.990

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch32

calib_packv5_042523_0143.root, FC#7, port C2

Entries	394
Mean	43.4
Std Dev	12.27

Turn on : 25.2647

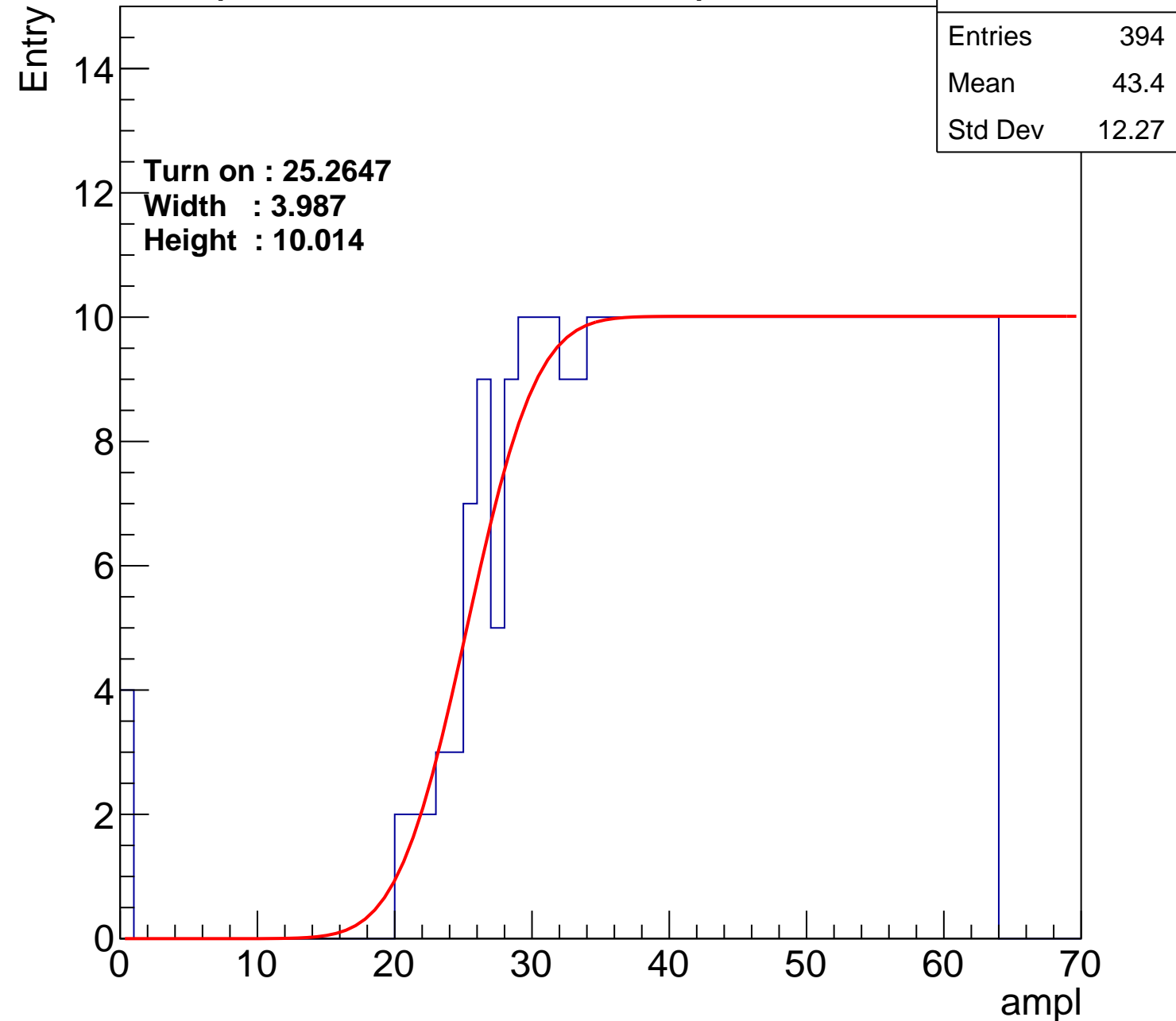
Width : 3.987

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch33

calib_packv5_042523_0143.root, FC#7, port C2

Entries	391
Mean	43.69
Std Dev	11.85

Turn on : 25.9145

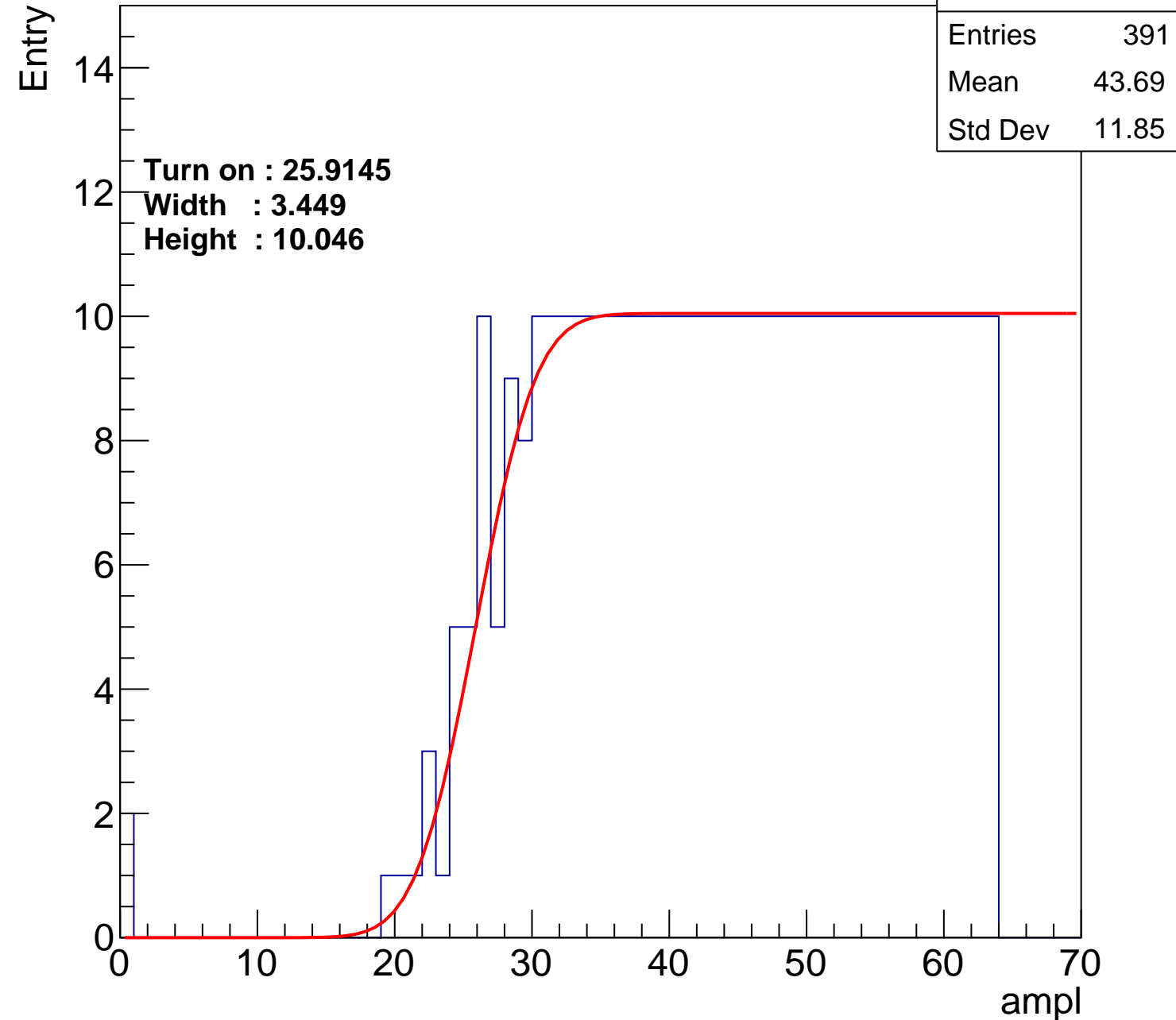
Width : 3.449

Height : 10.046

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch34

calib_packv5_042523_0143.root, FC#7, port C2

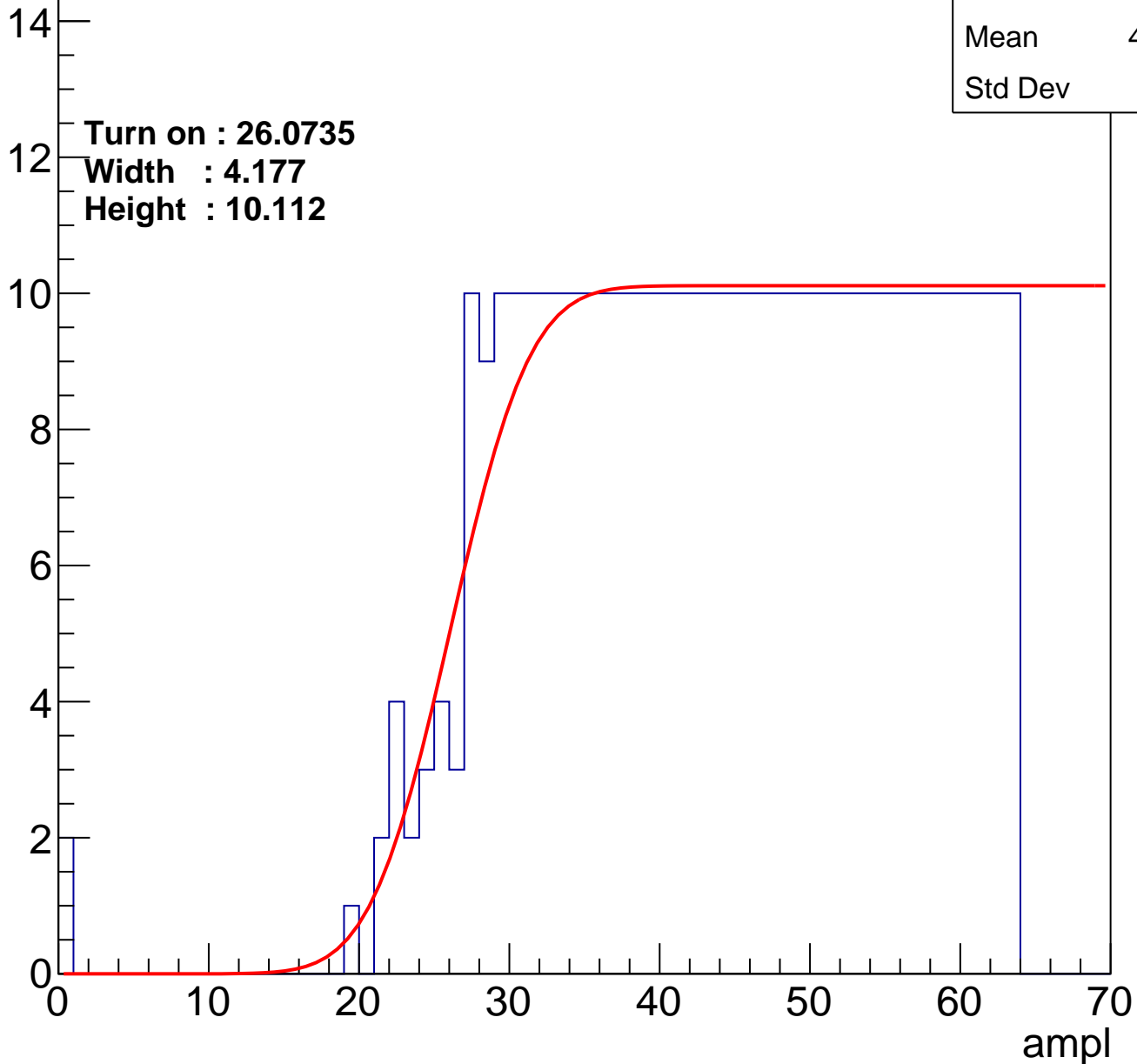
Entries	390
Mean	43.76
Std Dev	11.8

Turn on : 26.0735

Width : 4.177

Height : 10.112

Entry



B1L103S, U2-ch35

calib_packv5_042523_0143.root, FC#7, port C2

Entries	379
Mean	44.24
Std Dev	11.68

Turn on : 26.9015

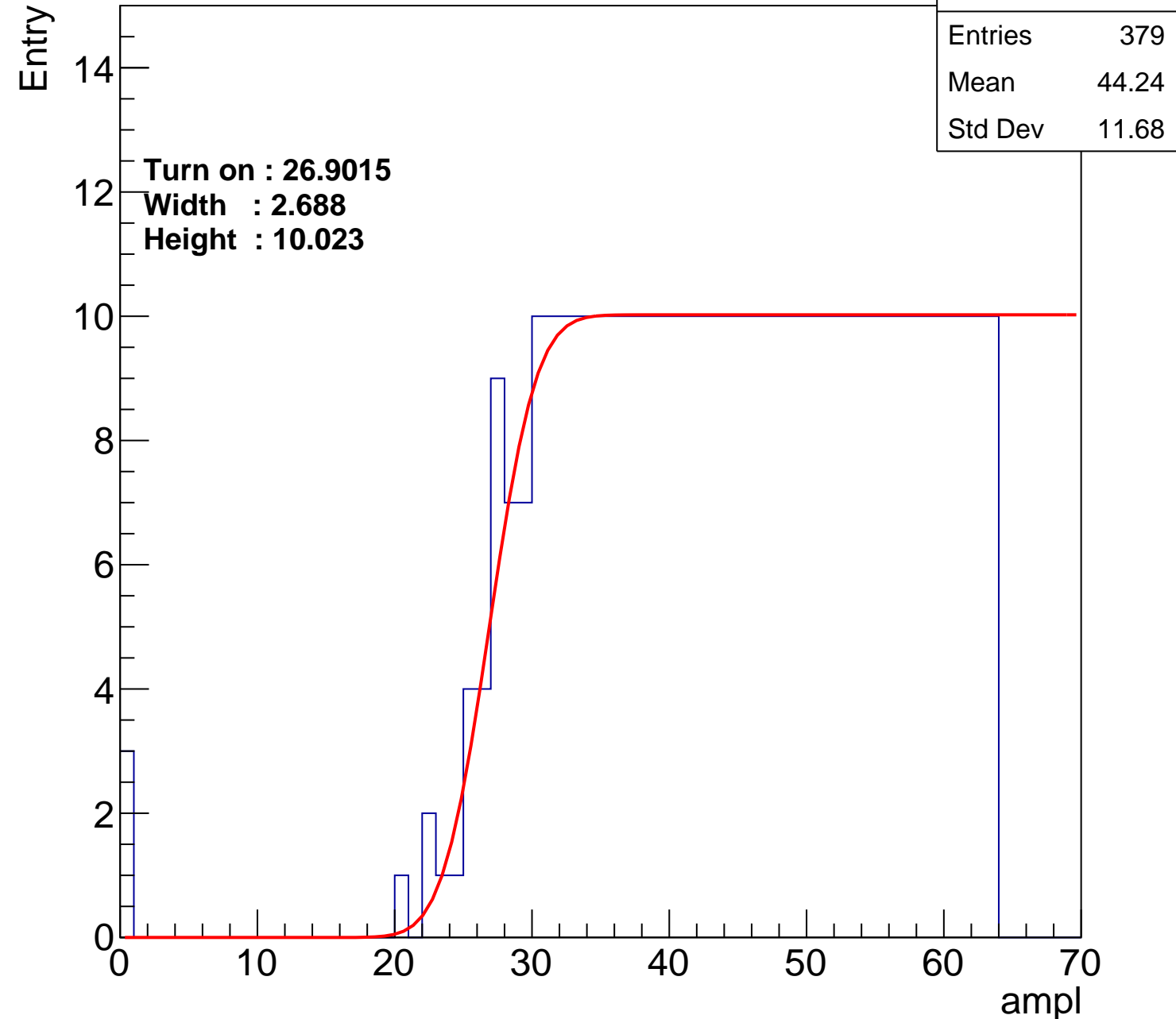
Width : 2.688

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch36

calib_packv5_042523_0143.root, FC#7, port C2

Entries	371
Mean	44.62
Std Dev	11.51

Turn on : 27.7029

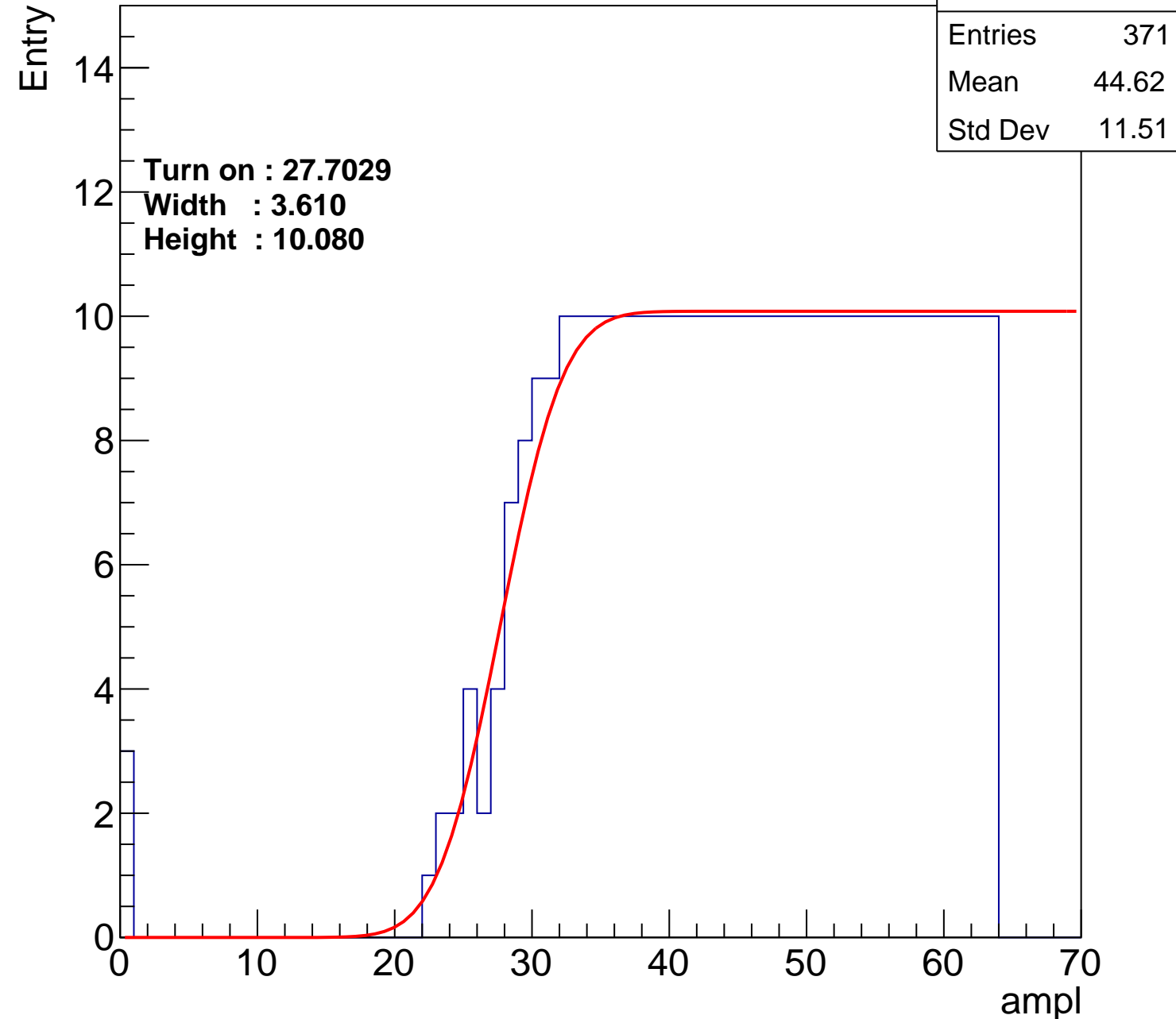
Width : 3.610

Height : 10.080

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch37

calib_packv5_042523_0143.root, FC#7, port C2

Entries	397
Mean	43.28
Std Dev	12.3

Turn on : 24.8918

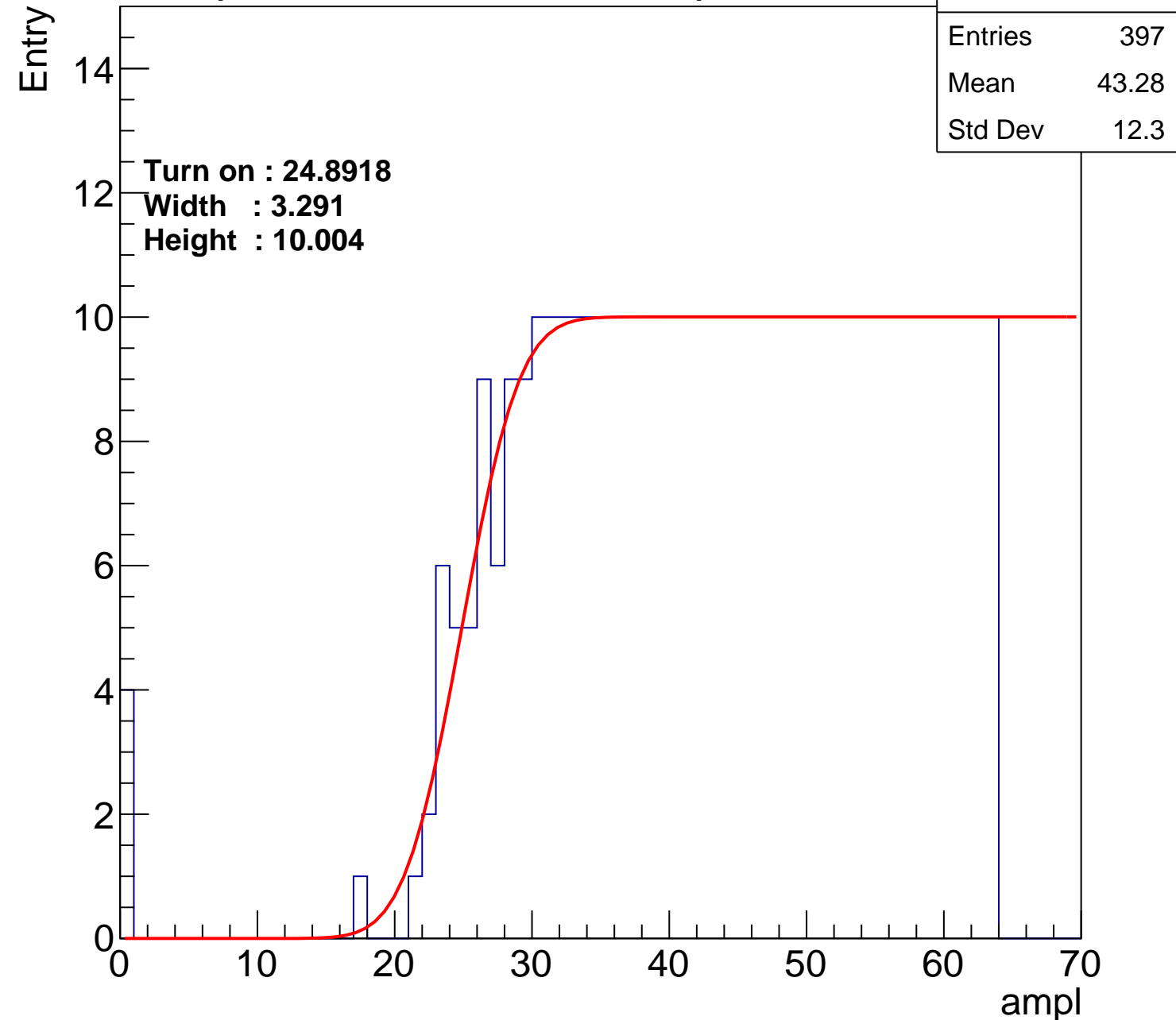
Width : 3.291

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch38

calib_packv5_042523_0143.root, FC#7, port C2

Entries	377
Mean	44.44
Std Dev	11.31

Turn on : 26.6689

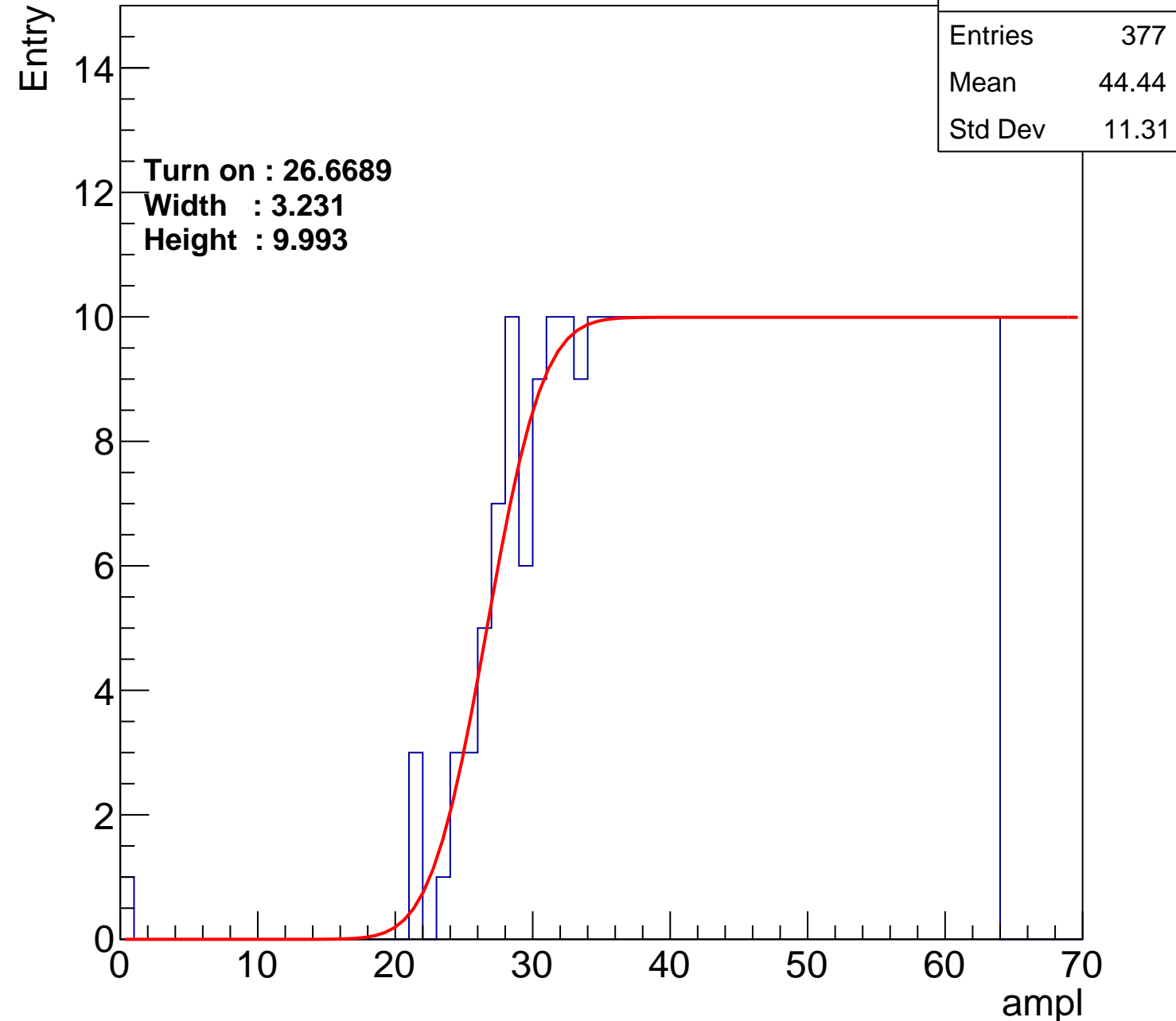
Width : 3.231

Height : 9.993

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch39

calib_packv5_042523_0143.root, FC#7, port C2

Entries	371
Mean	44.69
Std Dev	11.31

Turn on : 27.3898

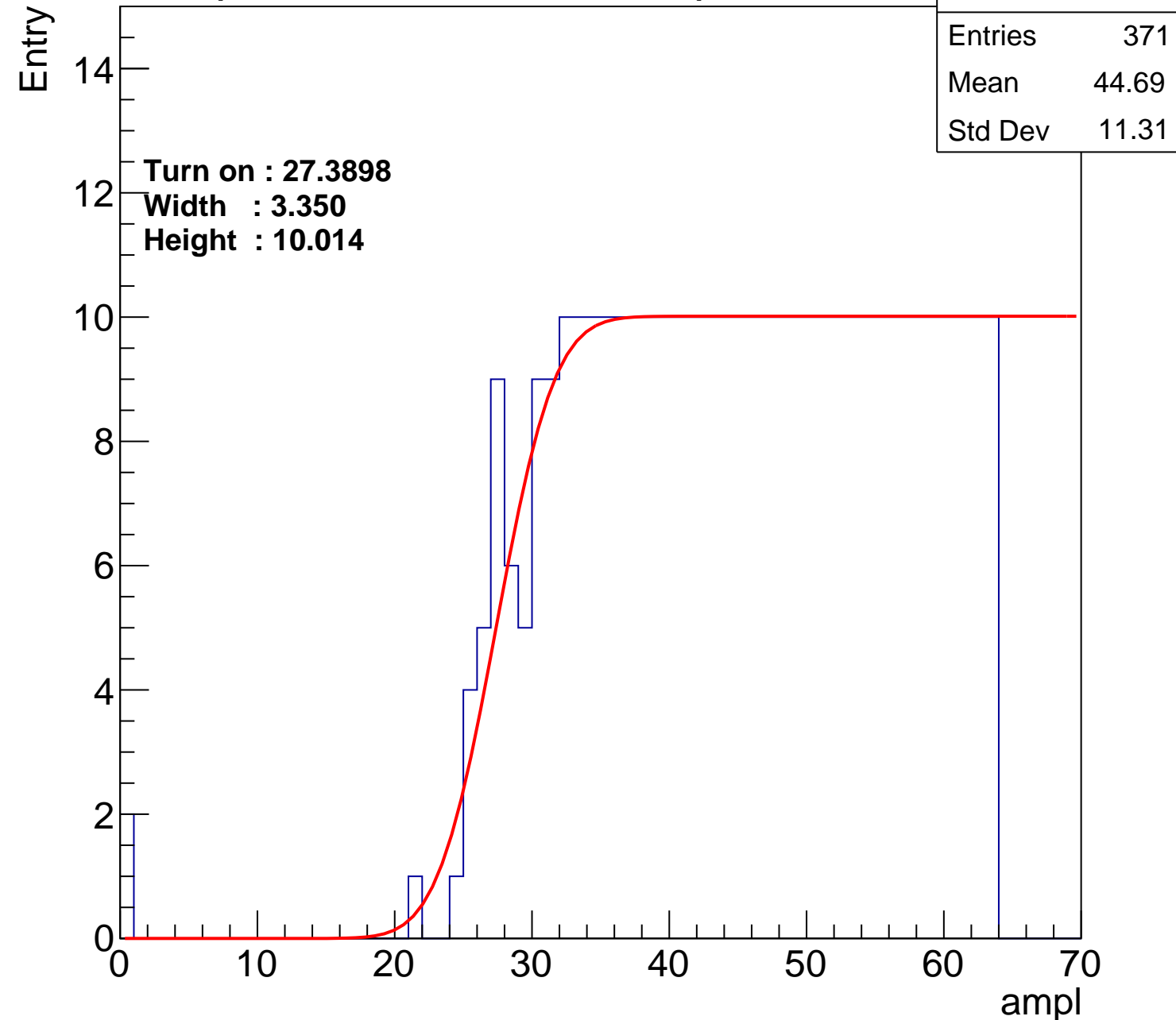
Width : 3.350

Height : 10.014

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch40

calib_packv5_042523_0143.root, FC#7, port C2

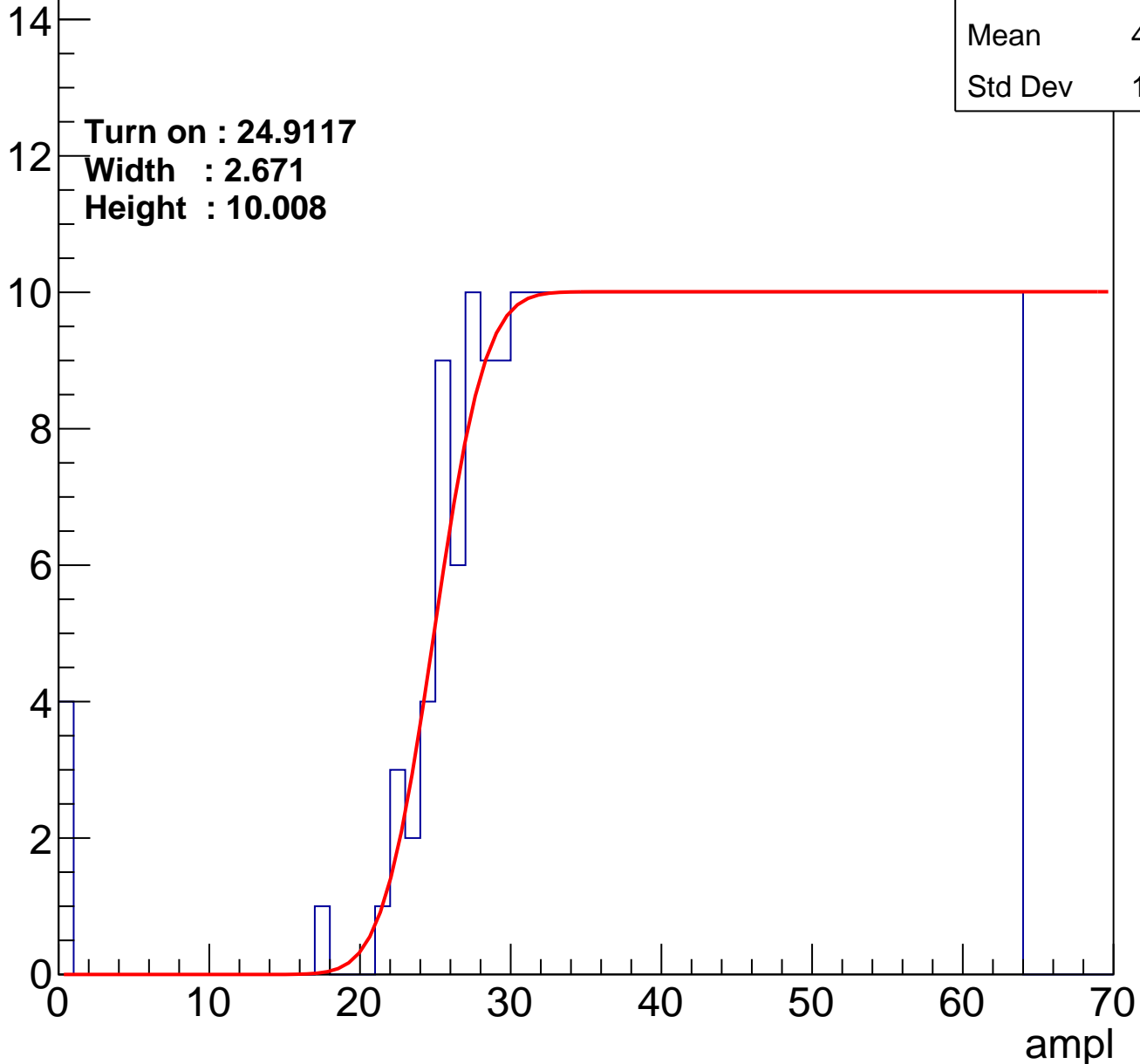
Entries	398
Mean	43.27
Std Dev	12.28

Turn on : 24.9117

Width : 2.671

Height : 10.008

Entry



B1L103S, U2-ch41

calib_packv5_042523_0143.root, FC#7, port C2

Entries	381
Mean	44.17
Std Dev	11.69

Turn on : 26.4745

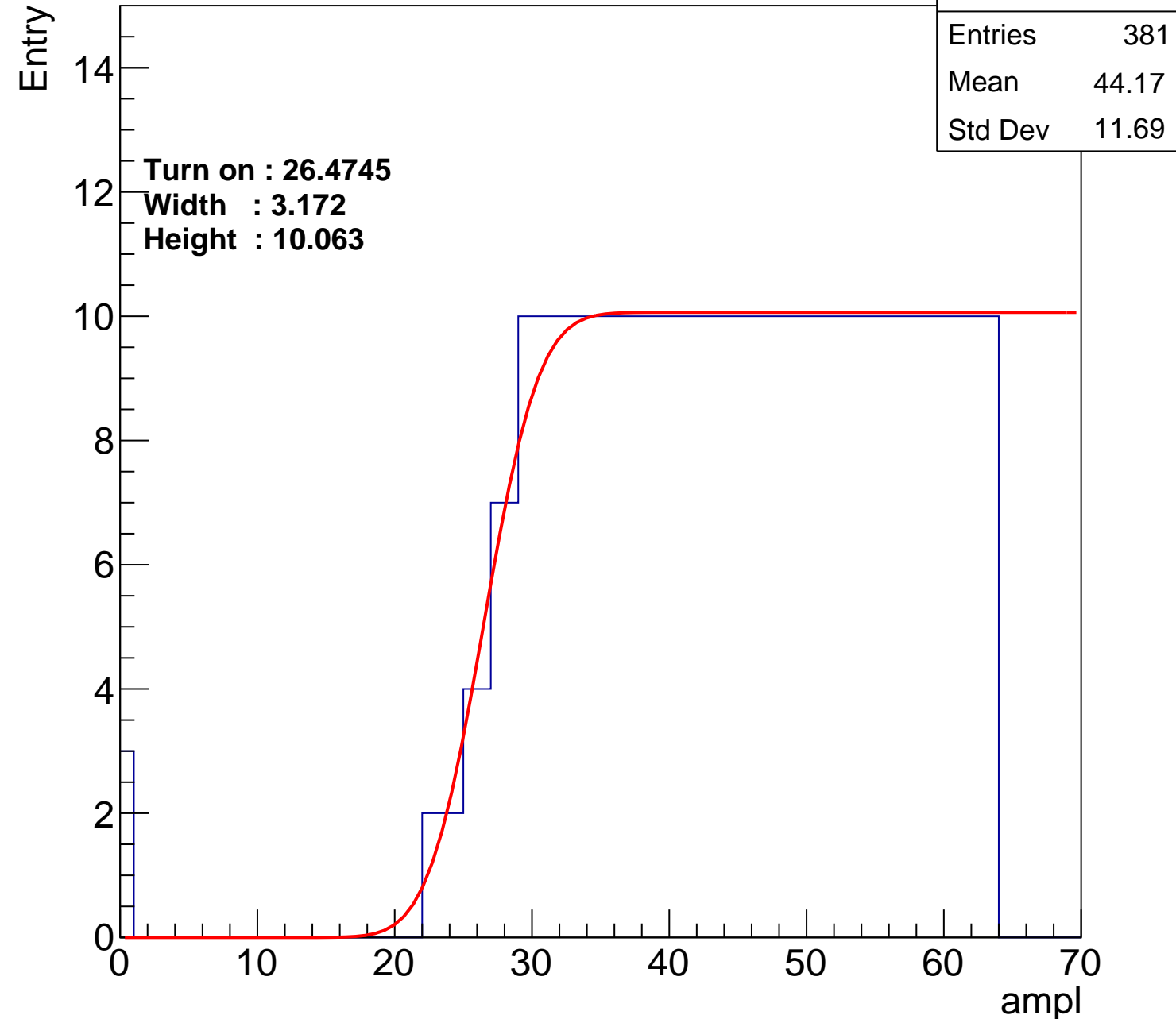
Width : 3.172

Height : 10.063

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch42

calib_packv5_042523_0143.root, FC#7, port C2

Entries	381
Mean	44.15
Std Dev	11.72

Turn on : 26.2623

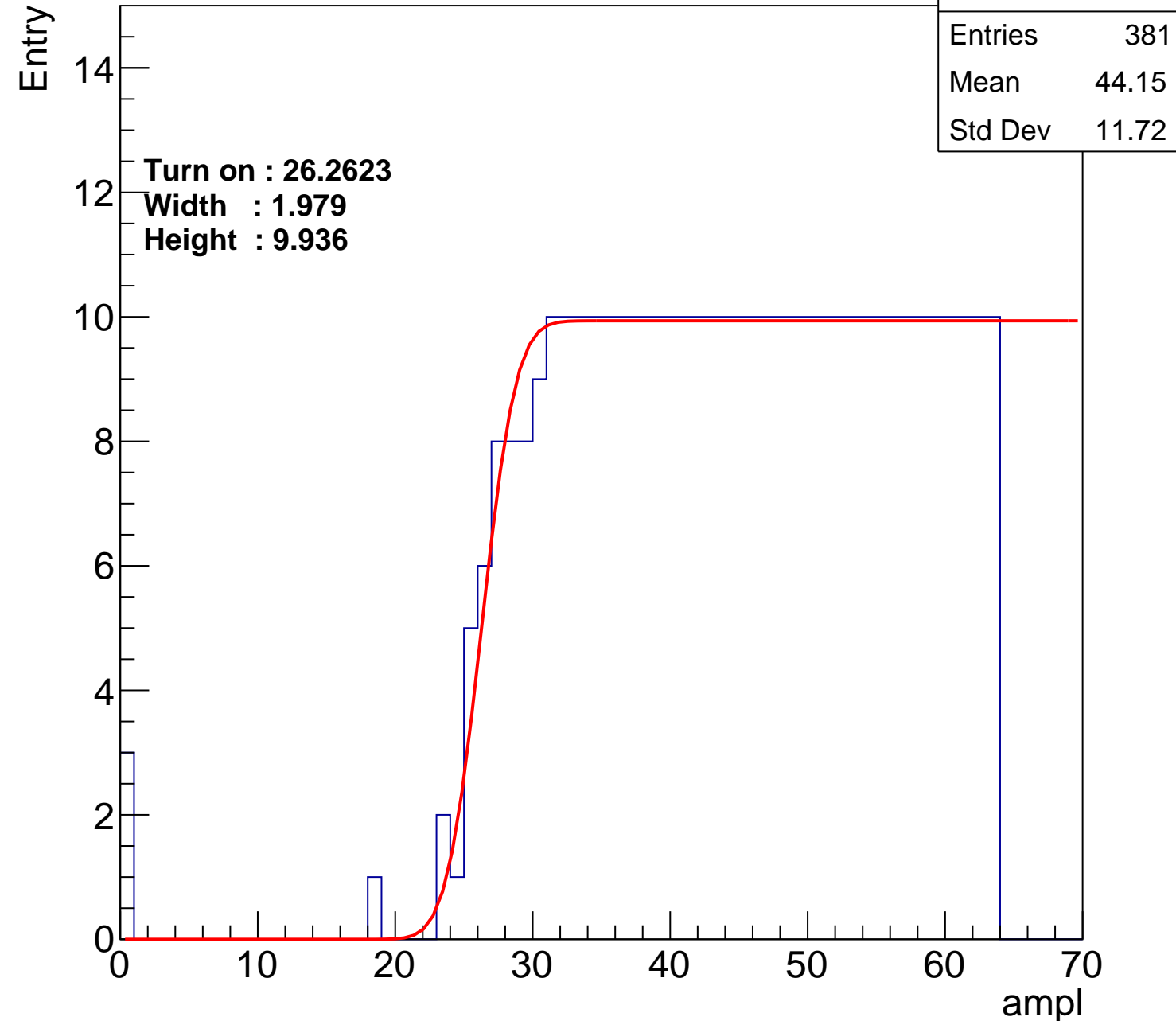
Width : 1.979

Height : 9.936

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch43

calib_packv5_042523_0143.root, FC#7, port C2

Entries	377
Mean	44.13
Std Dev	12.1

Turn on : 27.1792

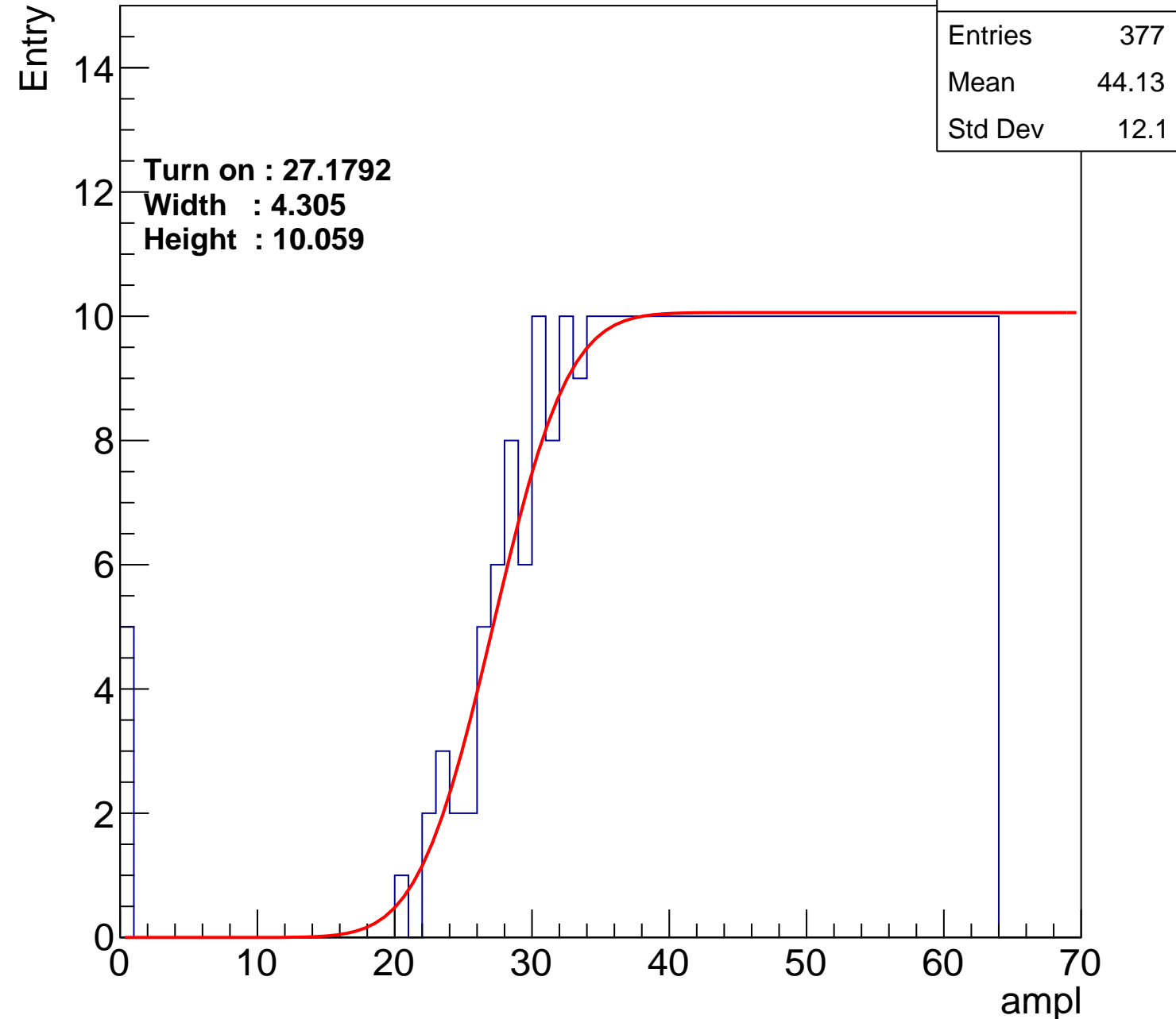
Width : 4.305

Height : 10.059

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch44

calib_packv5_042523_0143.root, FC#7, port C2

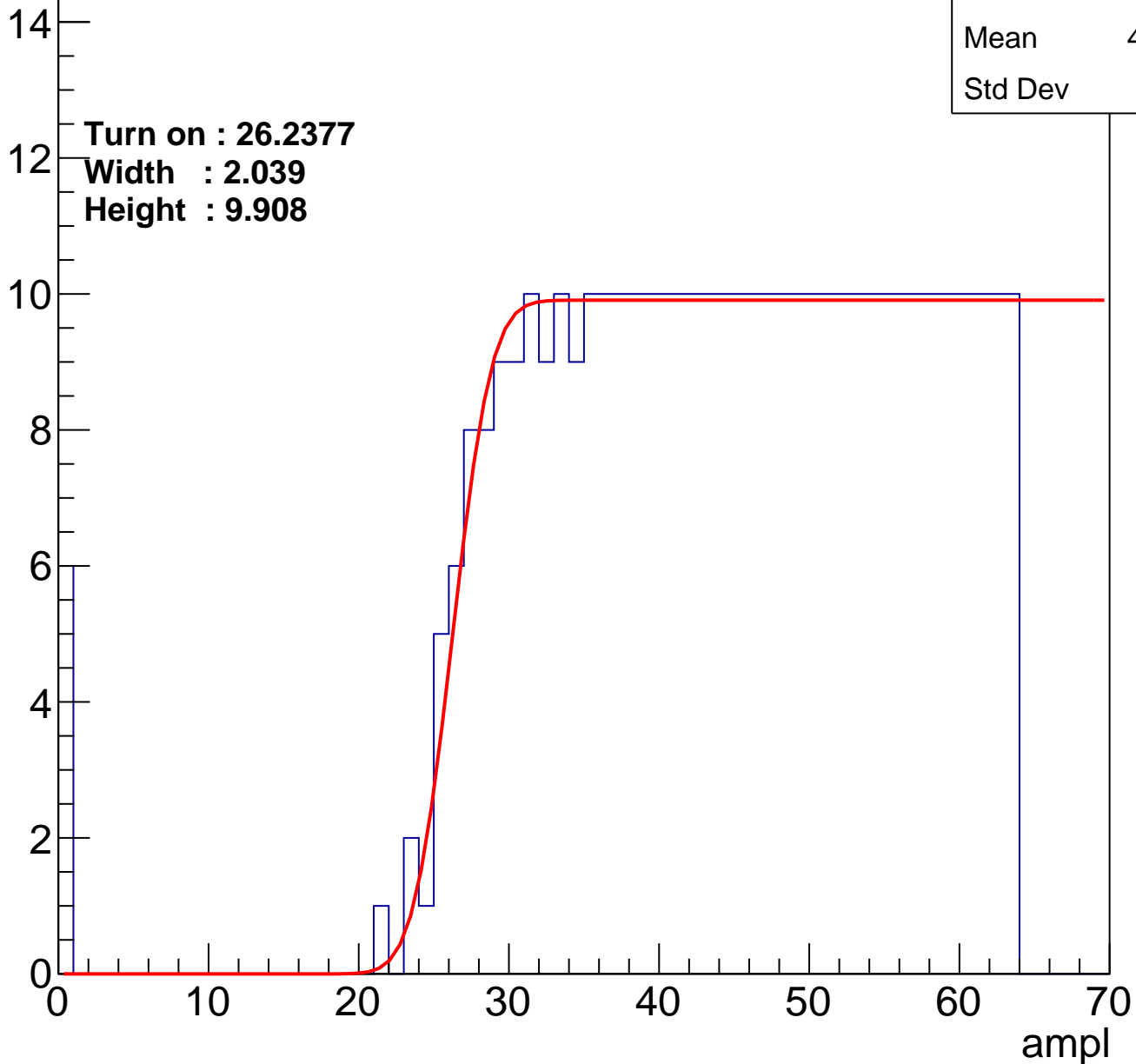
Entry

Entries	383
Mean	43.83
Std Dev	12.3

Turn on : 26.2377

Width : 2.039

Height : 9.908



B1L103S, U2-ch45

calib_packv5_042523_0143.root, FC#7, port C2

Entries	377
Mean	44.48
Std Dev	11.25

Turn on : 26.4957

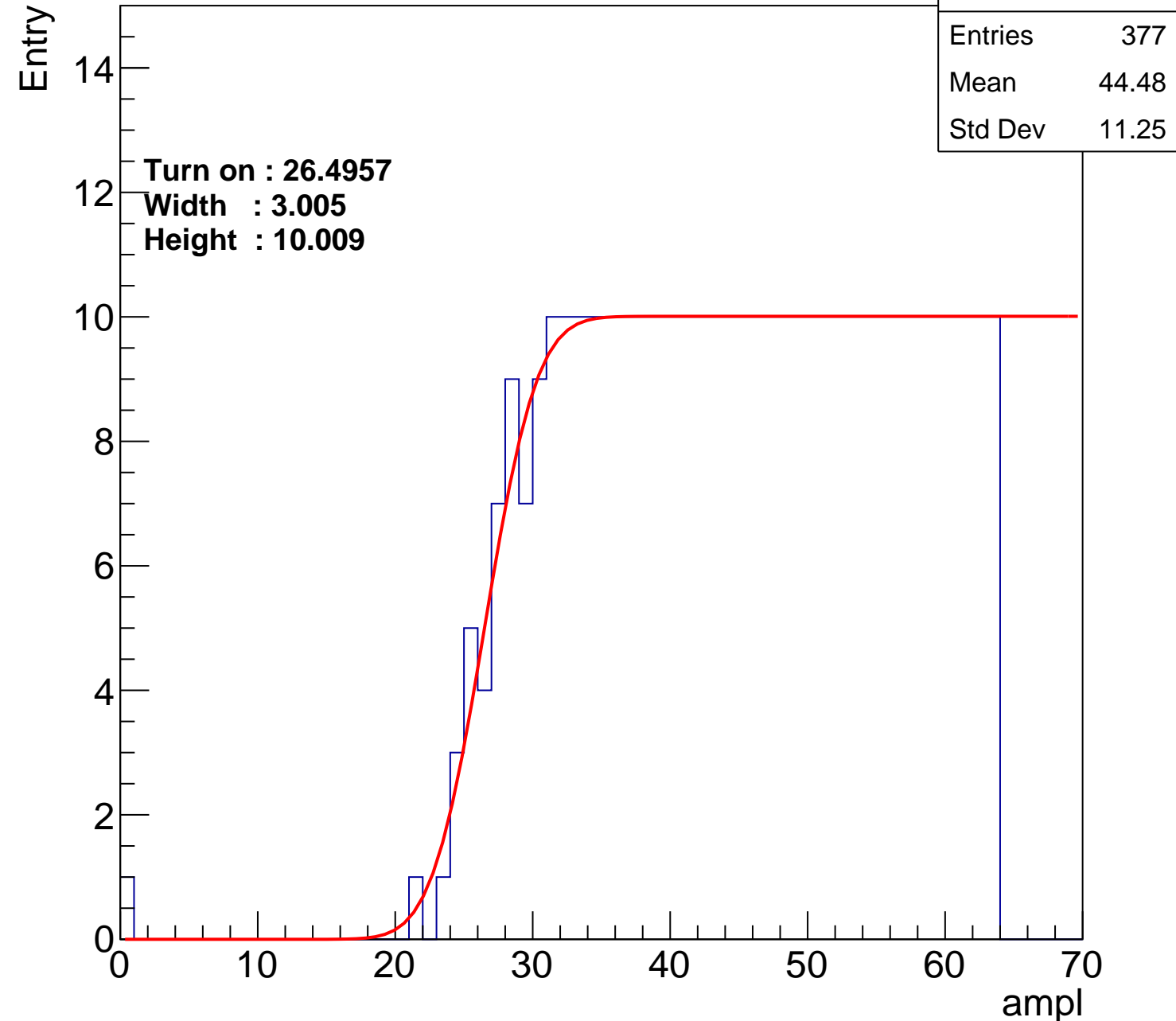
Width : 3.005

Height : 10.009

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch46

calib_packv5_042523_0143.root, FC#7, port C2

Entries	379
Mean	43.96
Std Dev	12.39

Turn on : 27.1114

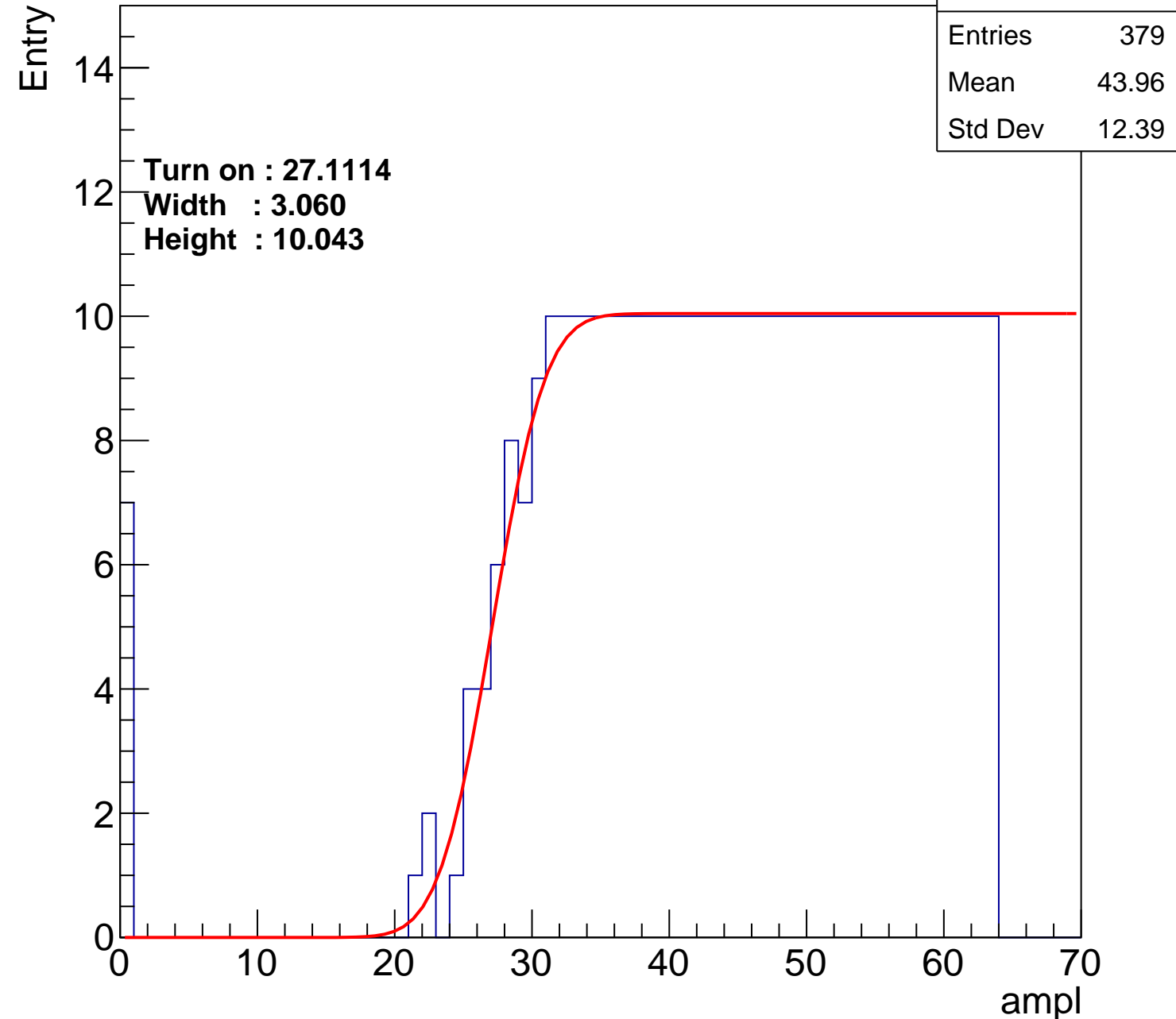
Width : 3.060

Height : 10.043

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch47

calib_packv5_042523_0143.root, FC#7, port C2

Entries	377
Mean	44.31
Std Dev	11.68

Turn on : 26.9615

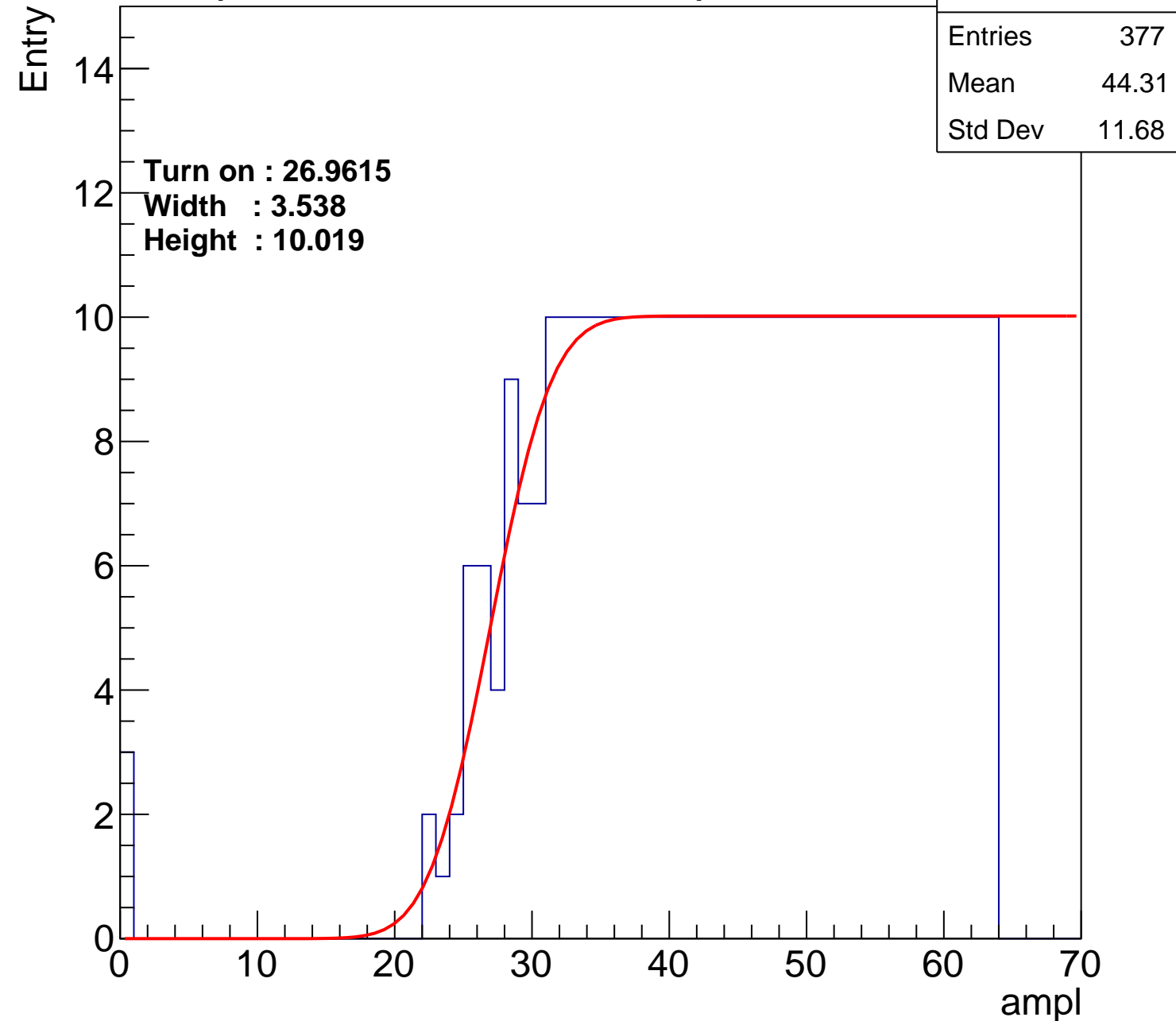
Width : 3.538

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch48

calib_packv5_042523_0143.root, FC#7, port C2

Entries	374
Mean	44.3
Std Dev	12

Turn on : 26.9512

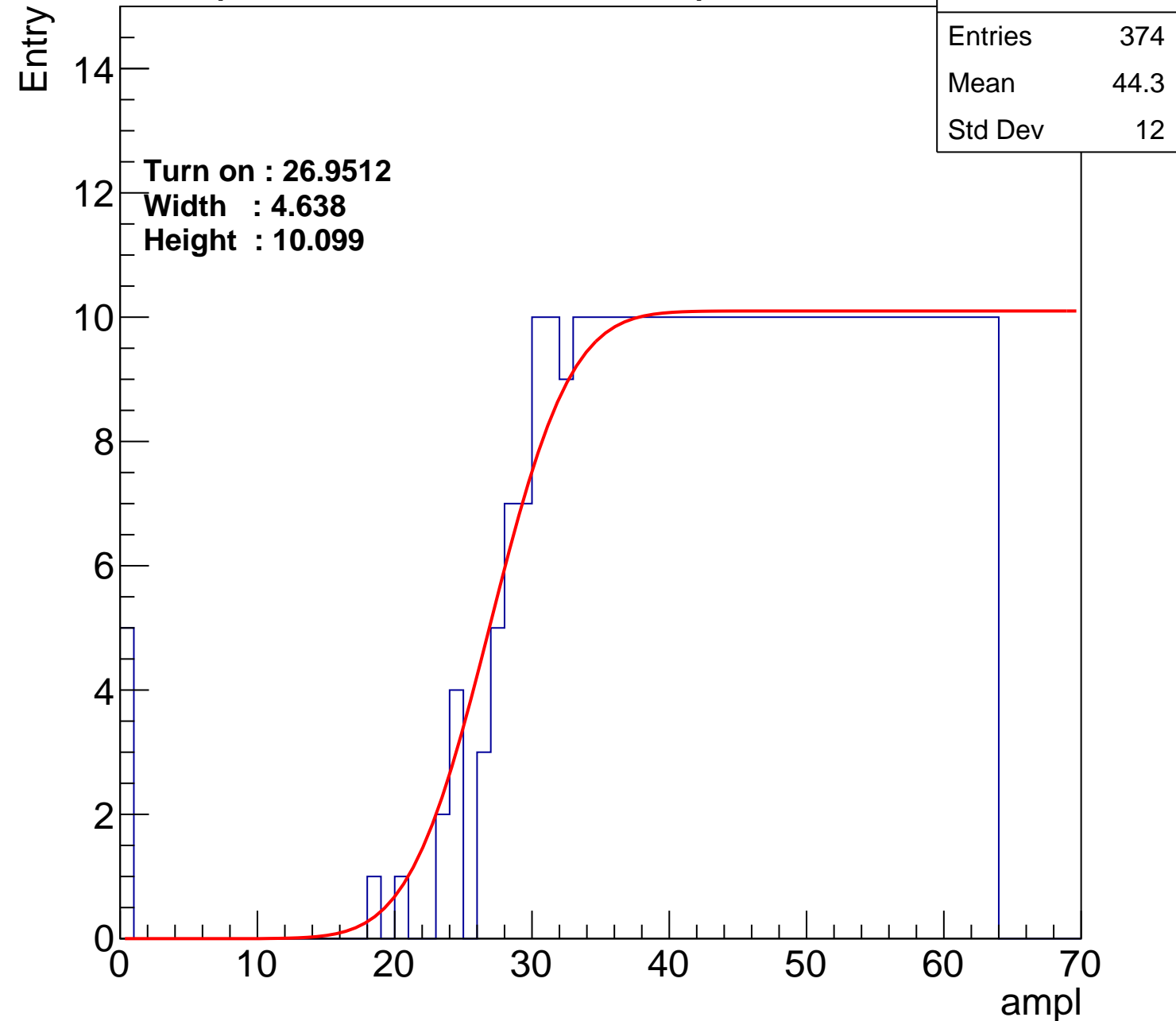
Width : 4.638

Height : 10.099

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch49

calib_packv5_042523_0143.root, FC#7, port C2

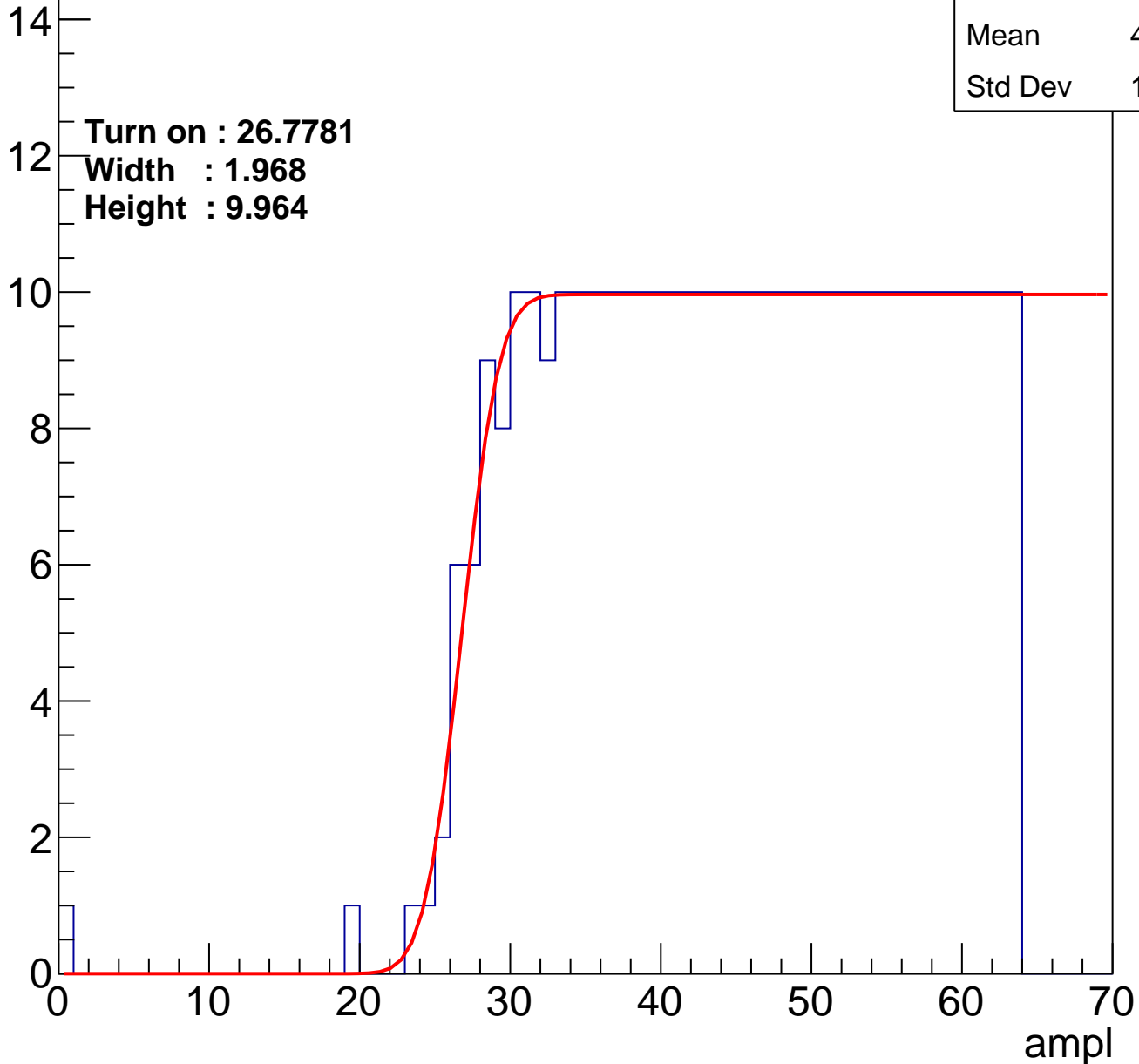
Entries	374
Mean	44.64
Std Dev	11.15

Turn on : 26.7781

Width : 1.968

Height : 9.964

Entry



B1L103S, U2-ch50

calib_packv5_042523_0143.root, FC#7, port C2

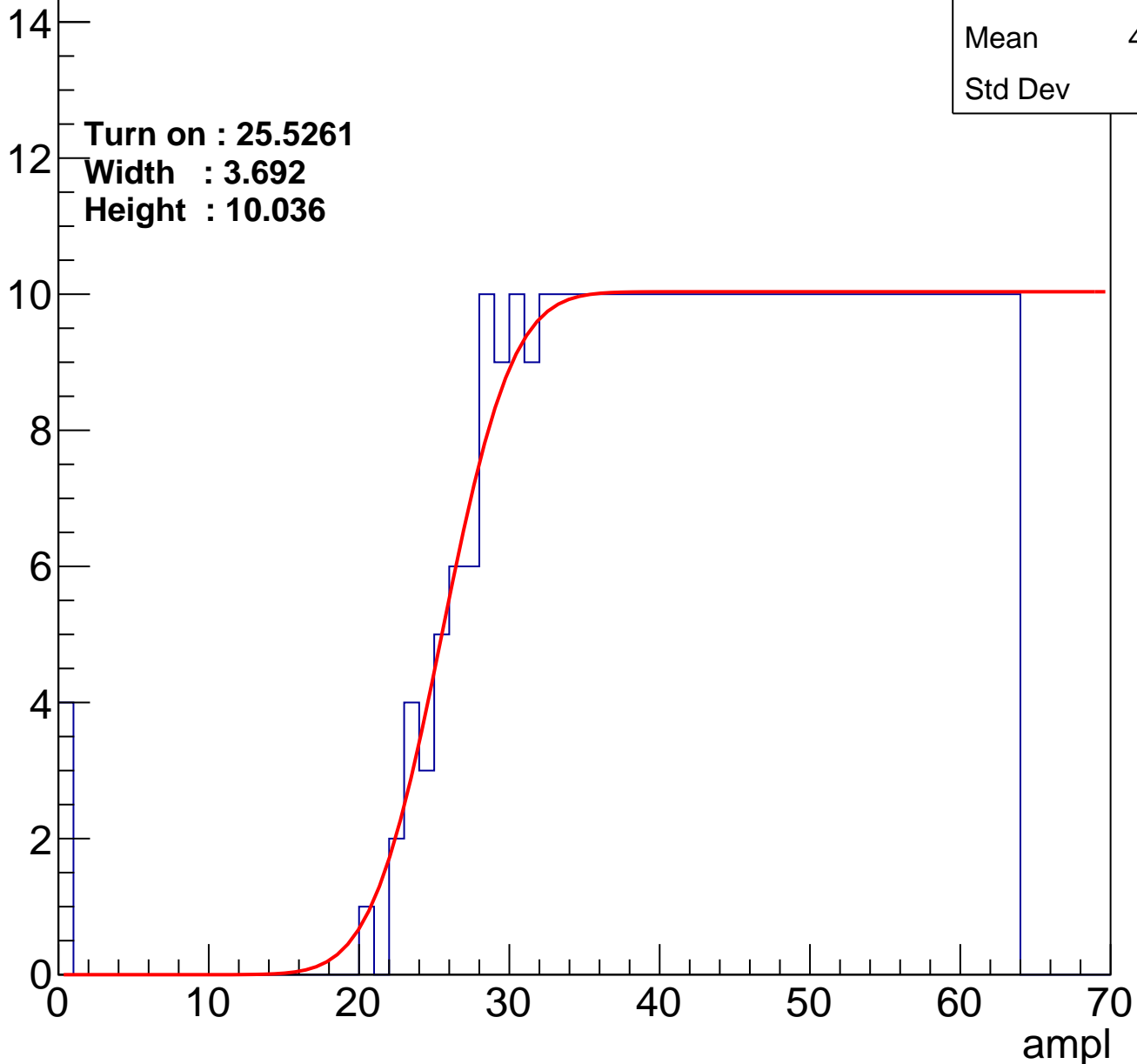
Entries	389
Mean	43.68
Std Dev	12.1

Turn on : 25.5261

Width : 3.692

Height : 10.036

Entry



B1L103S, U2-ch51

calib_packv5_042523_0143.root, FC#7, port C2

Entries	387
Mean	43.9
Std Dev	11.67

Turn on : 25.3463

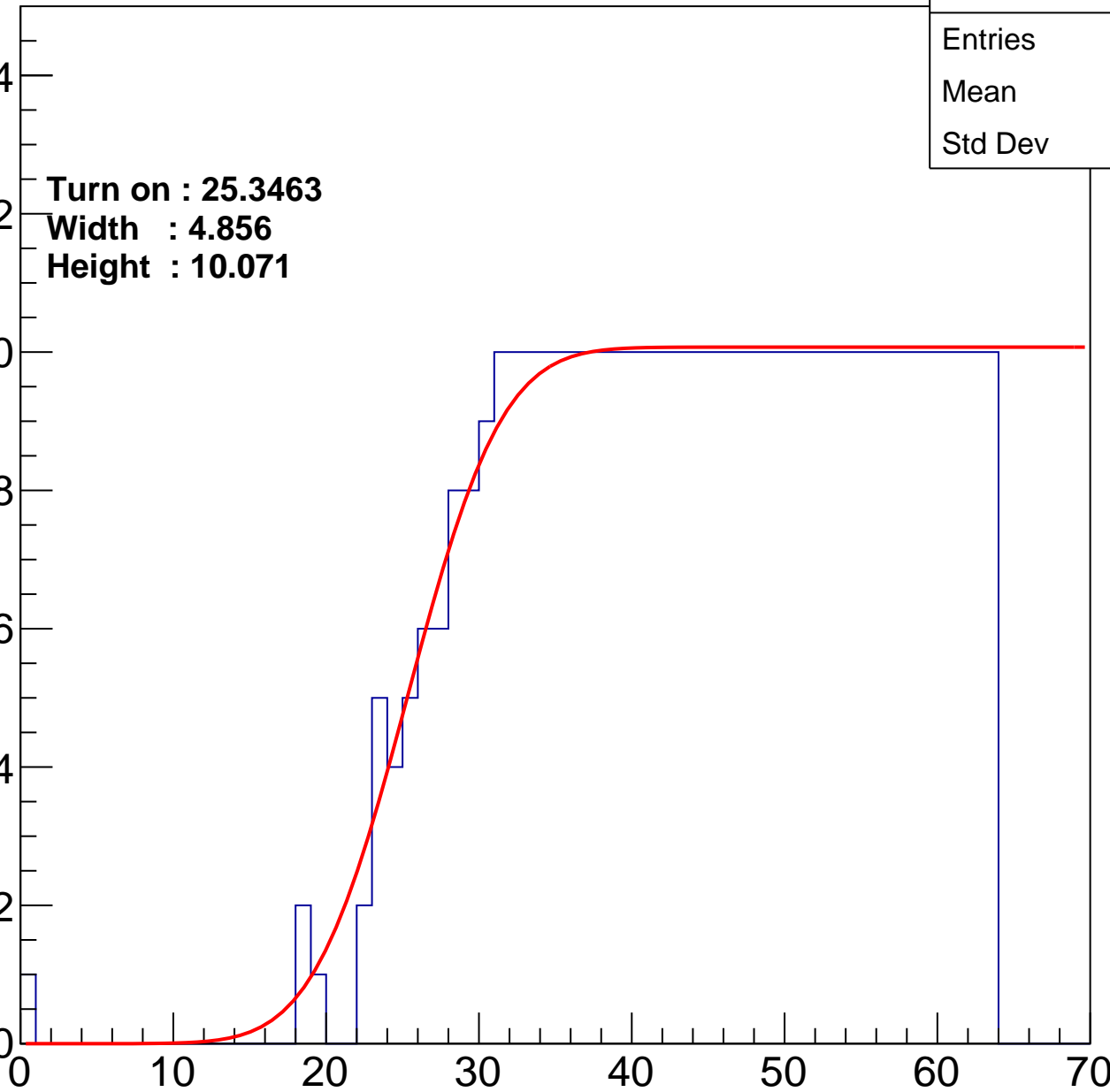
Width : 4.856

Height : 10.071

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch52

calib_packv5_042523_0143.root, FC#7, port C2

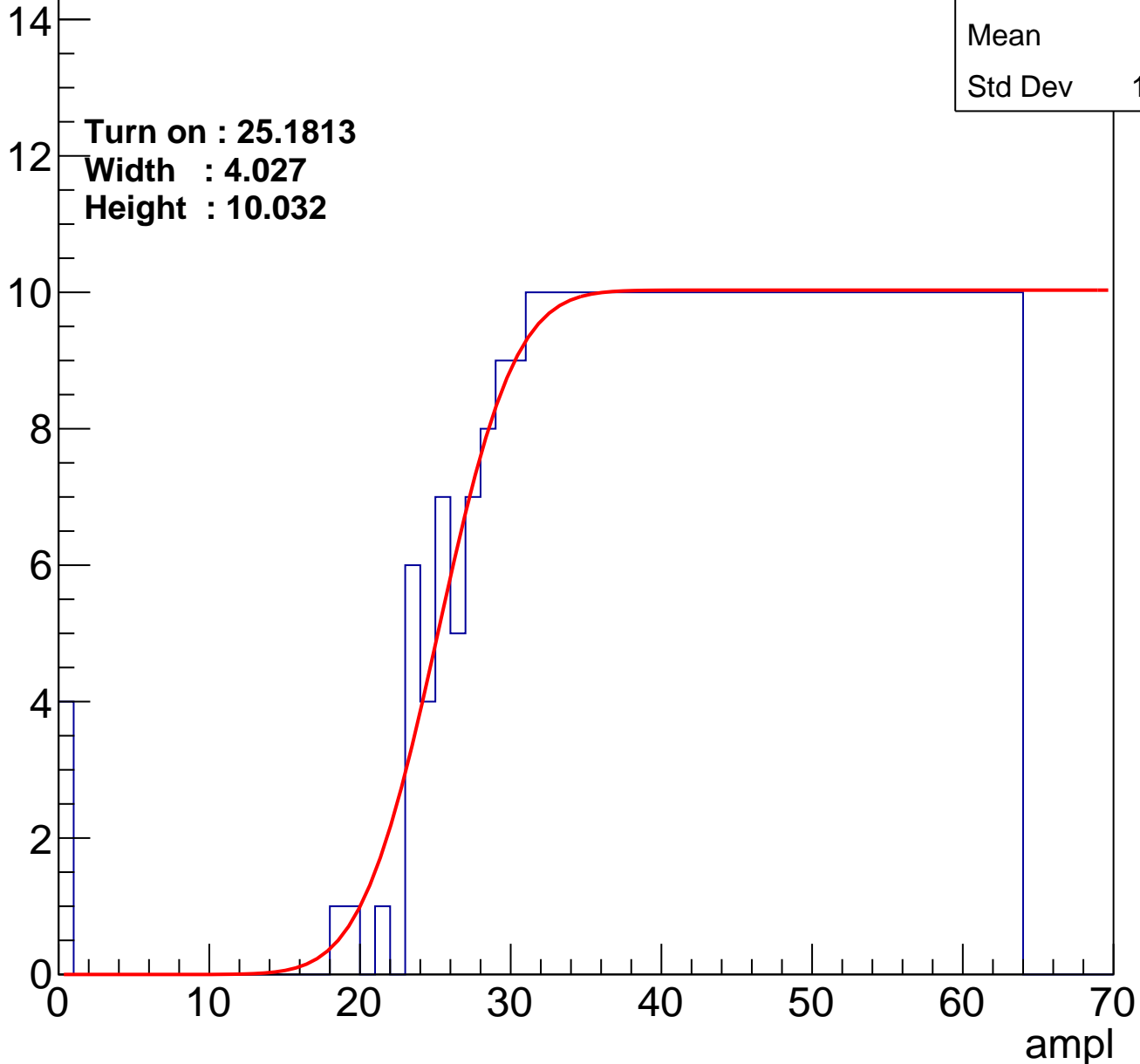
Entries	392
Mean	43.5
Std Dev	12.23

Turn on : 25.1813

Width : 4.027

Height : 10.032

Entry



B1L103S, U2-ch53

calib_packv5_042523_0143.root, FC#7, port C2

Entries	383
Mean	44.06
Std Dev	11.76

Turn on : 26.1131

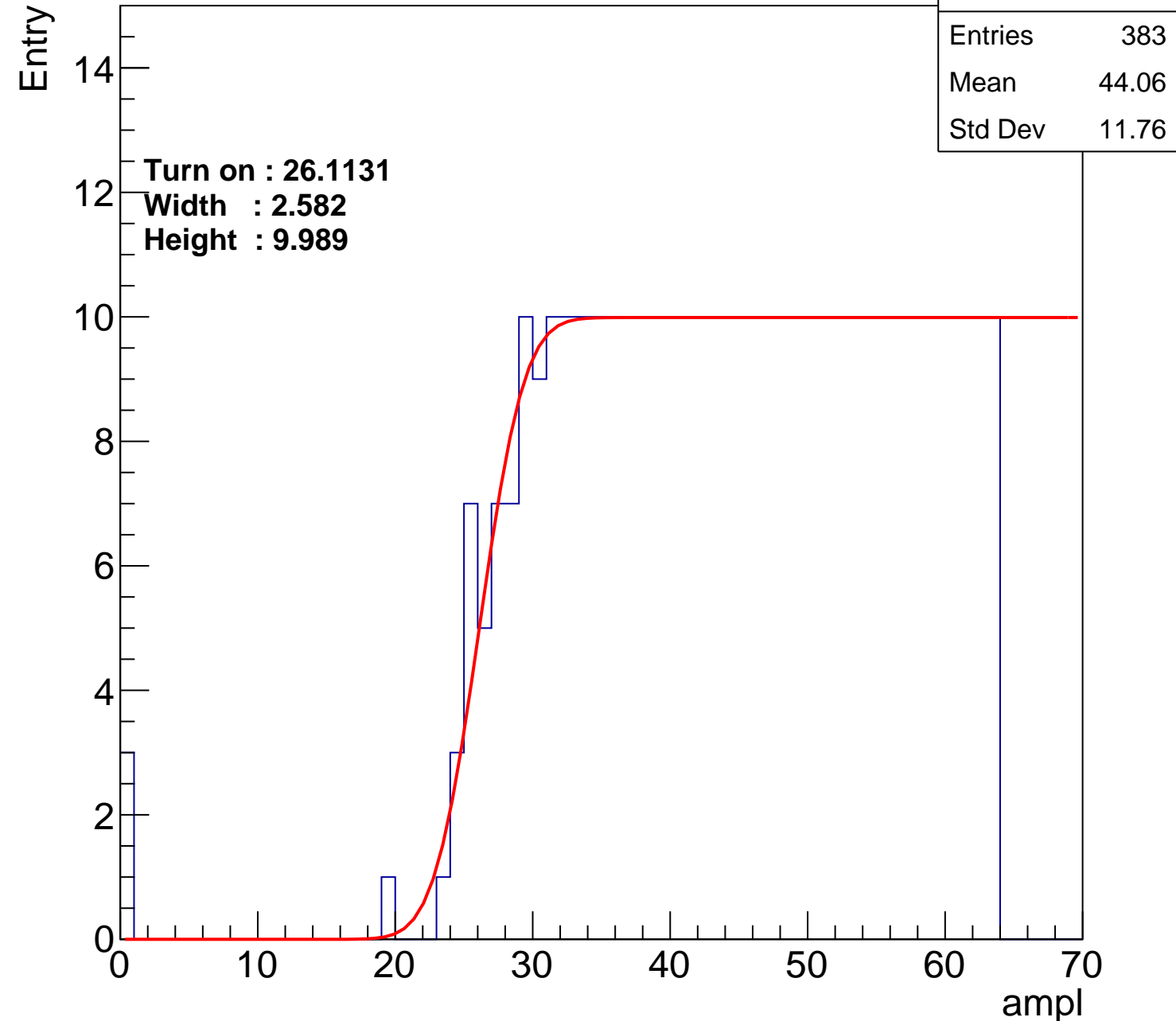
Width : 2.582

Height : 9.989

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch54

calib_packv5_042523_0143.root, FC#7, port C2

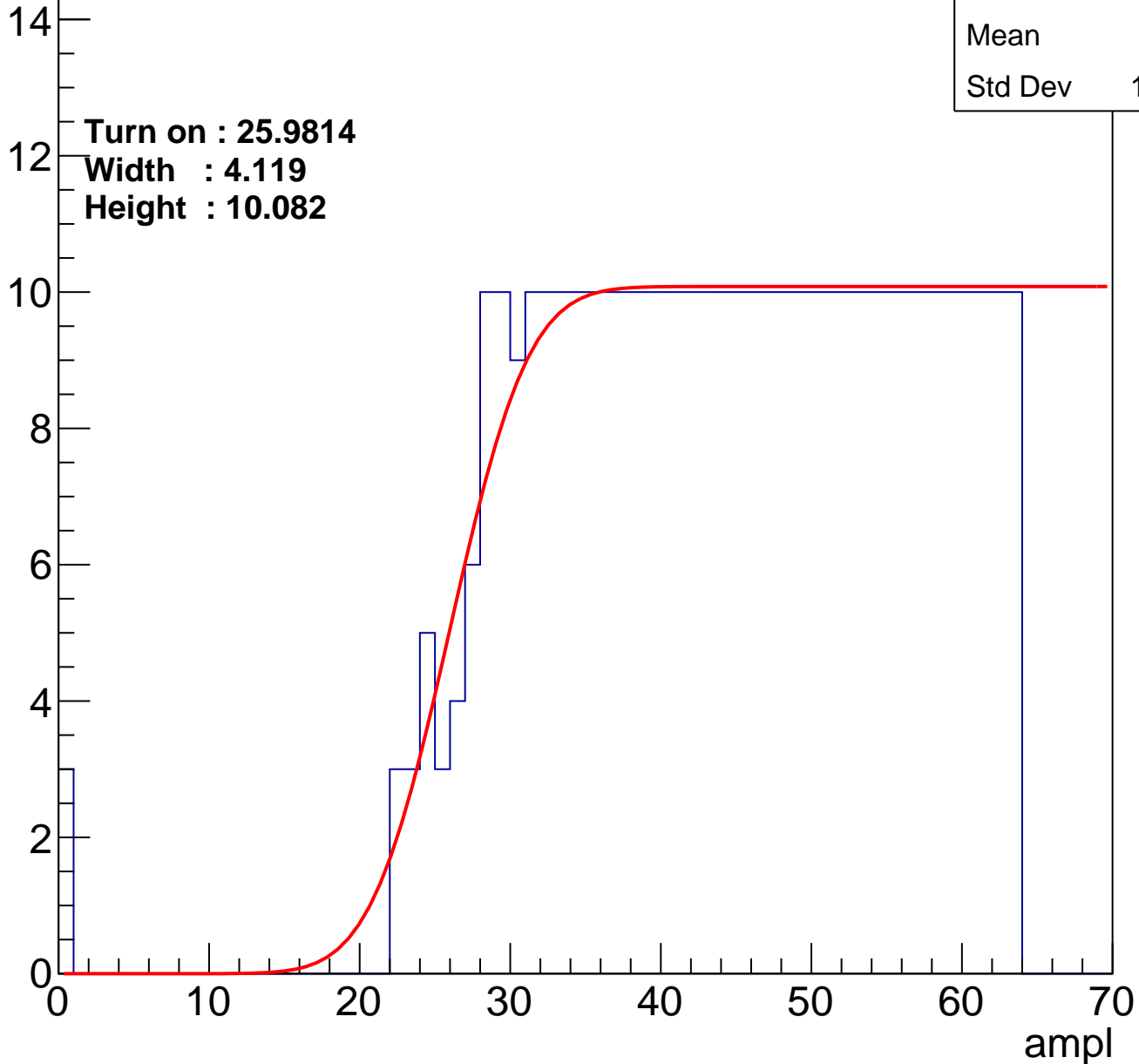
Entries	386
Mean	43.9
Std Dev	11.84

Turn on : 25.9814

Width : 4.119

Height : 10.082

Entry



B1L103S, U2-ch55

calib_packv5_042523_0143.root, FC#7, port C2

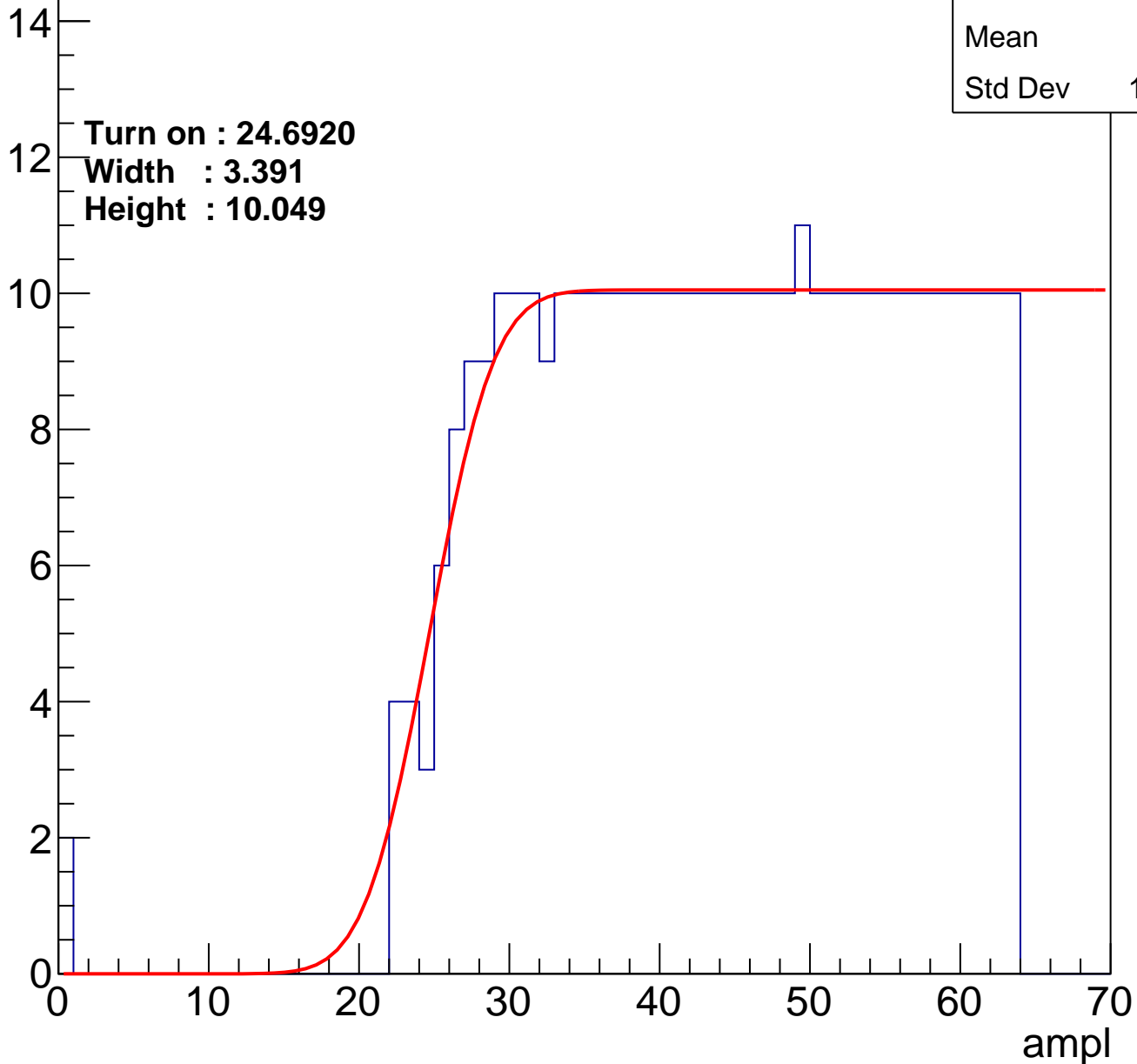
Entries	395
Mean	43.6
Std Dev	11.84

Turn on : 24.6920

Width : 3.391

Height : 10.049

Entry



B1L103S, U2-ch56

calib_packv5_042523_0143.root, FC#7, port C2

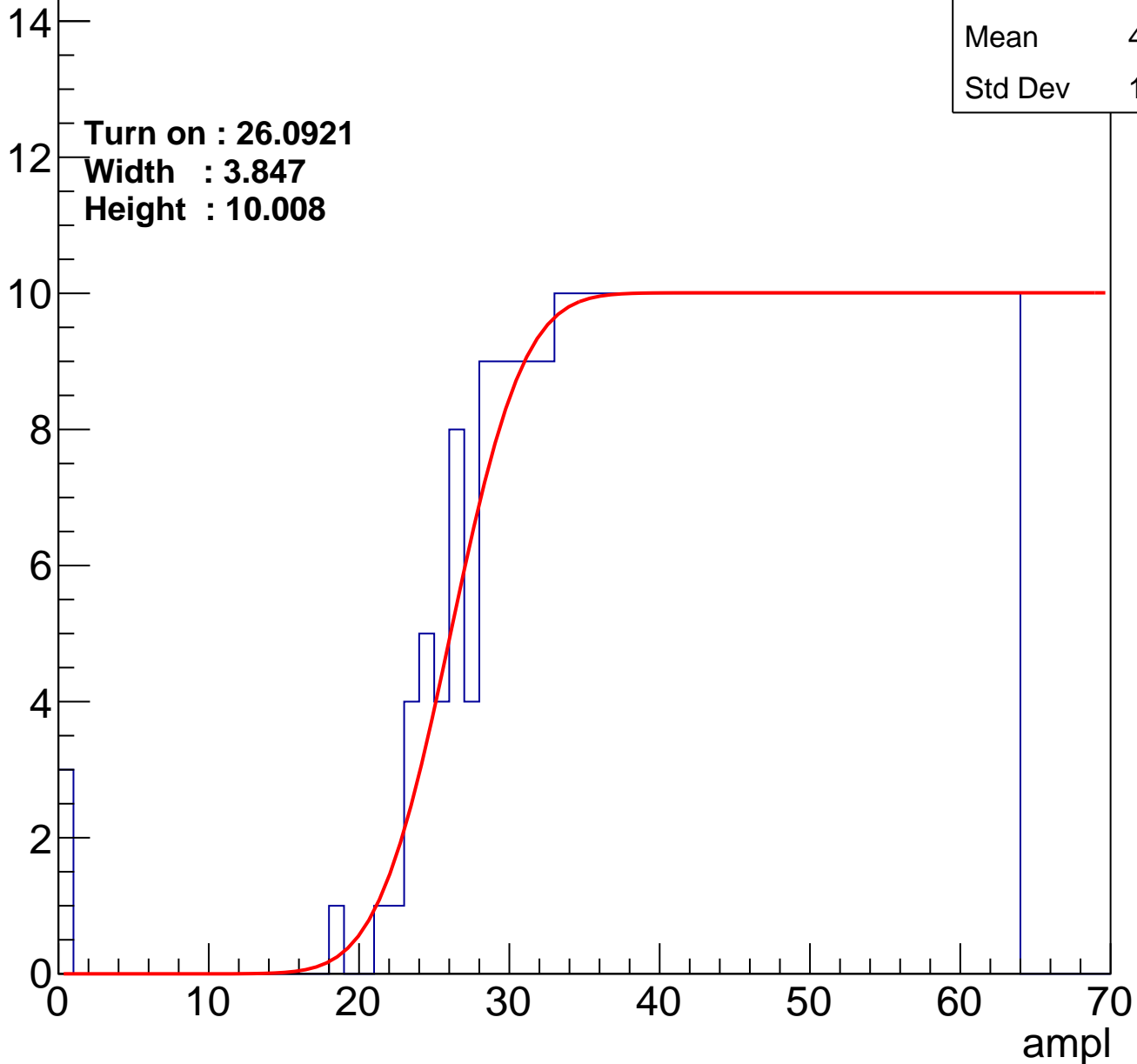
Entries	386
Mean	43.83
Std Dev	11.95

Turn on : 26.0921

Width : 3.847

Height : 10.008

Entry



B1L103S, U2-ch57

calib_packv5_042523_0143.root, FC#7, port C2

Entries	376
Mean	44.28
Std Dev	11.84

Turn on : 26.5344

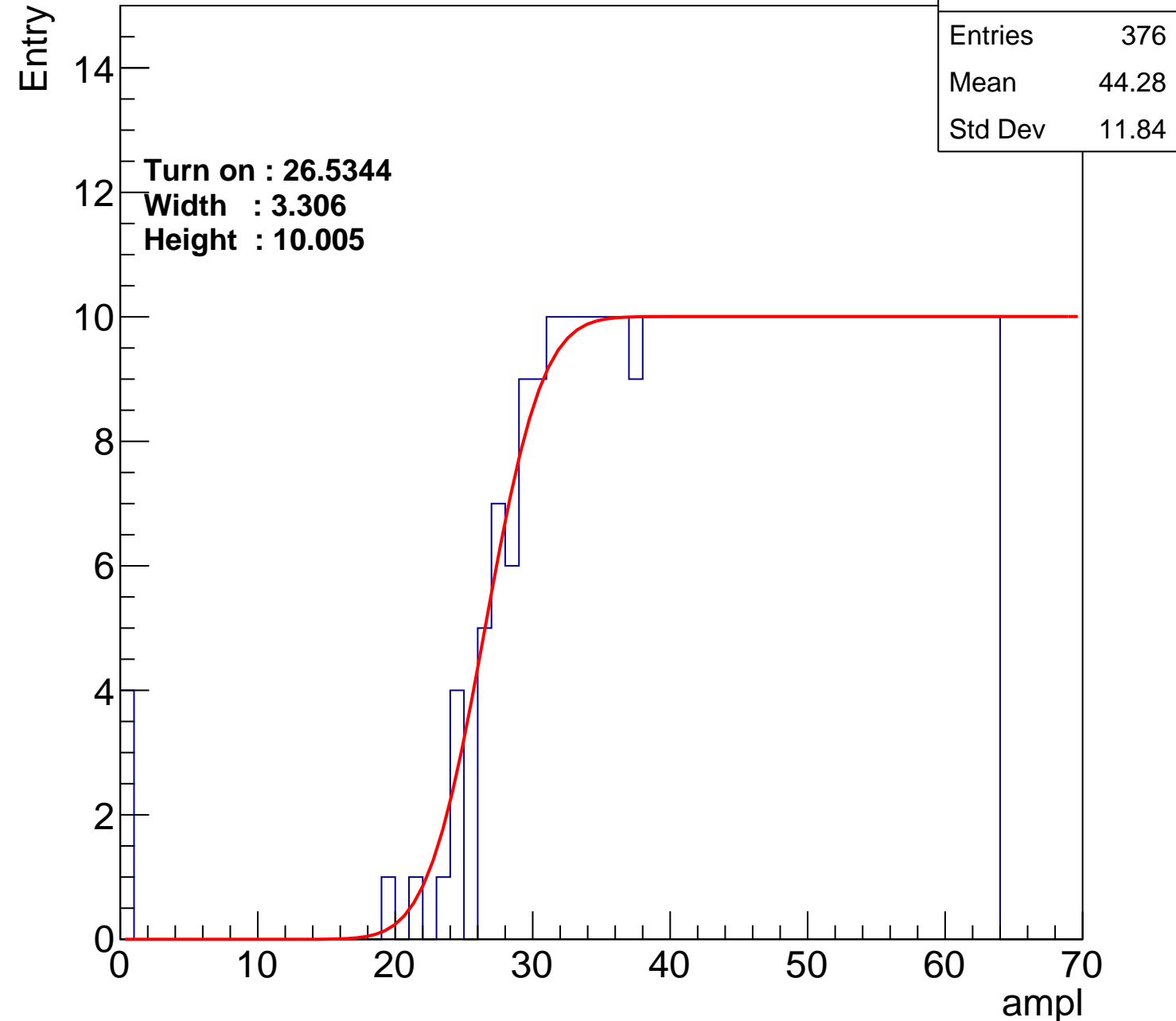
Width : 3.306

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch58

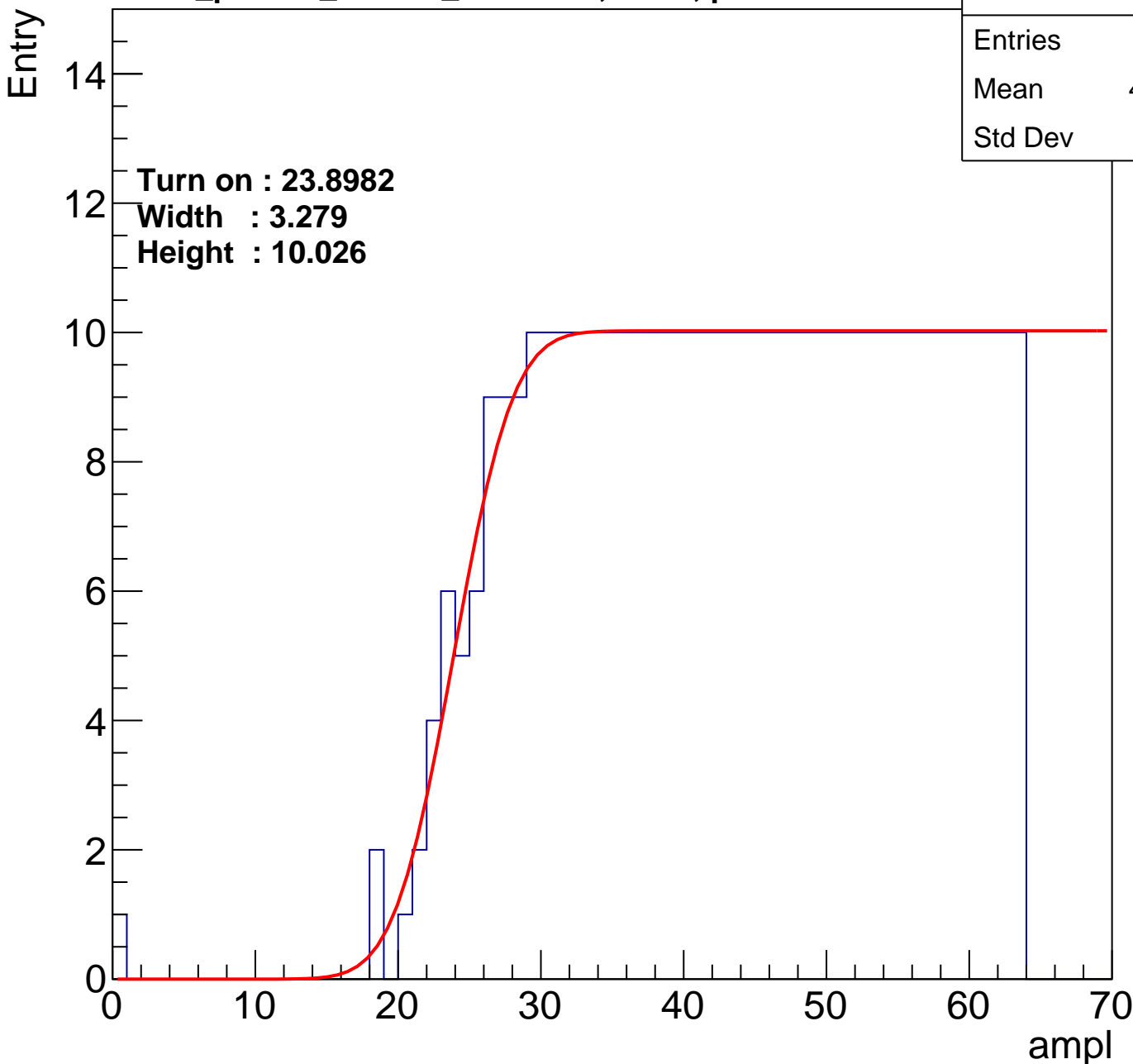
calib_packv5_042523_0143.root, FC#7, port C2

Entries	404
Mean	43.13
Std Dev	12.01

Turn on : 23.8982

Width : 3.279

Height : 10.026



B1L103S, U2-ch59

calib_packv5_042523_0143.root, FC#7, port C2

Entries	378
Mean	44.33
Std Dev	11.58

Turn on : 26.5981

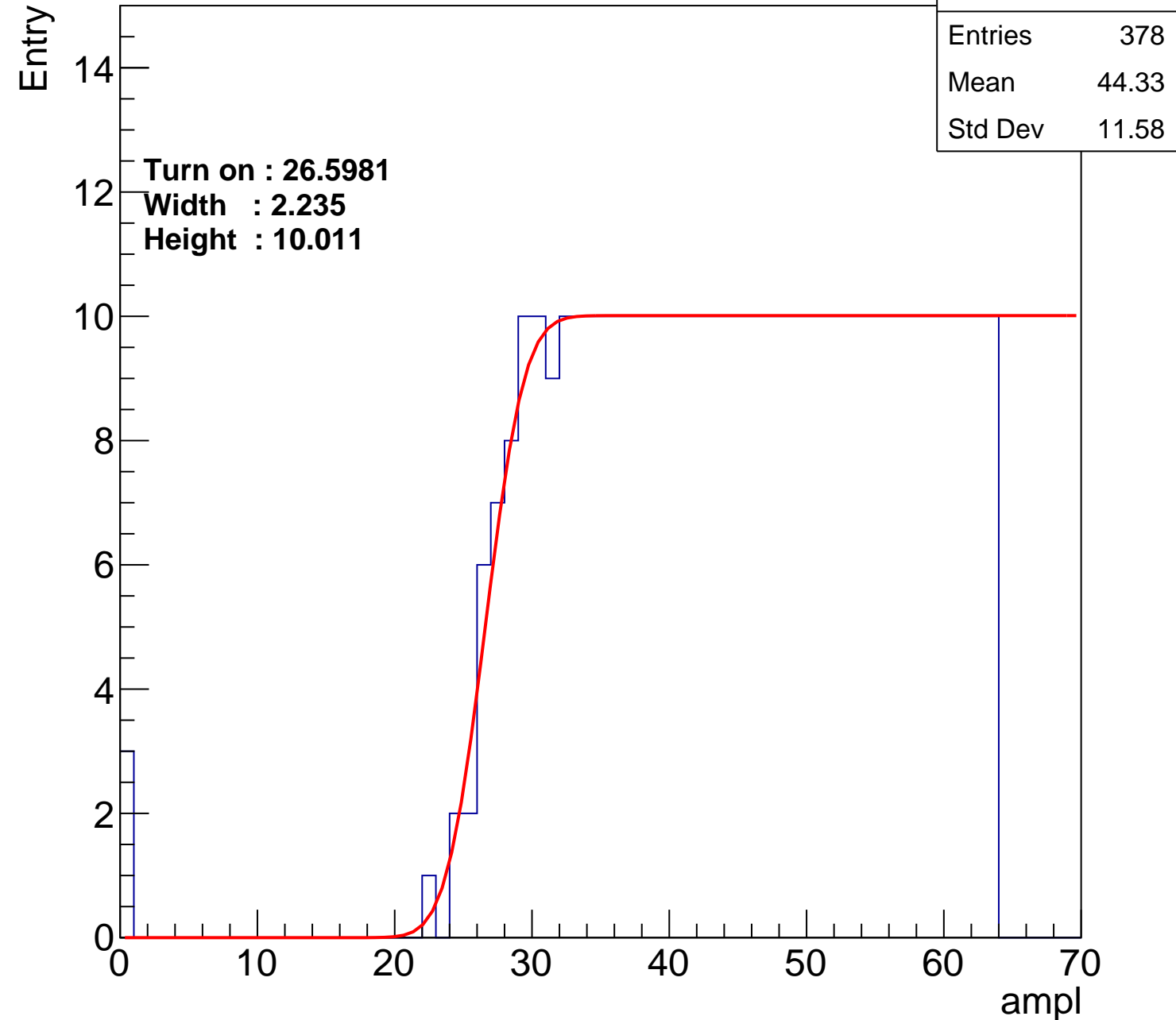
Width : 2.235

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch60

calib_packv5_042523_0143.root, FC#7, port C2

Entries	383
Mean	43.92
Std Dev	12.04

Turn on : 26.0615

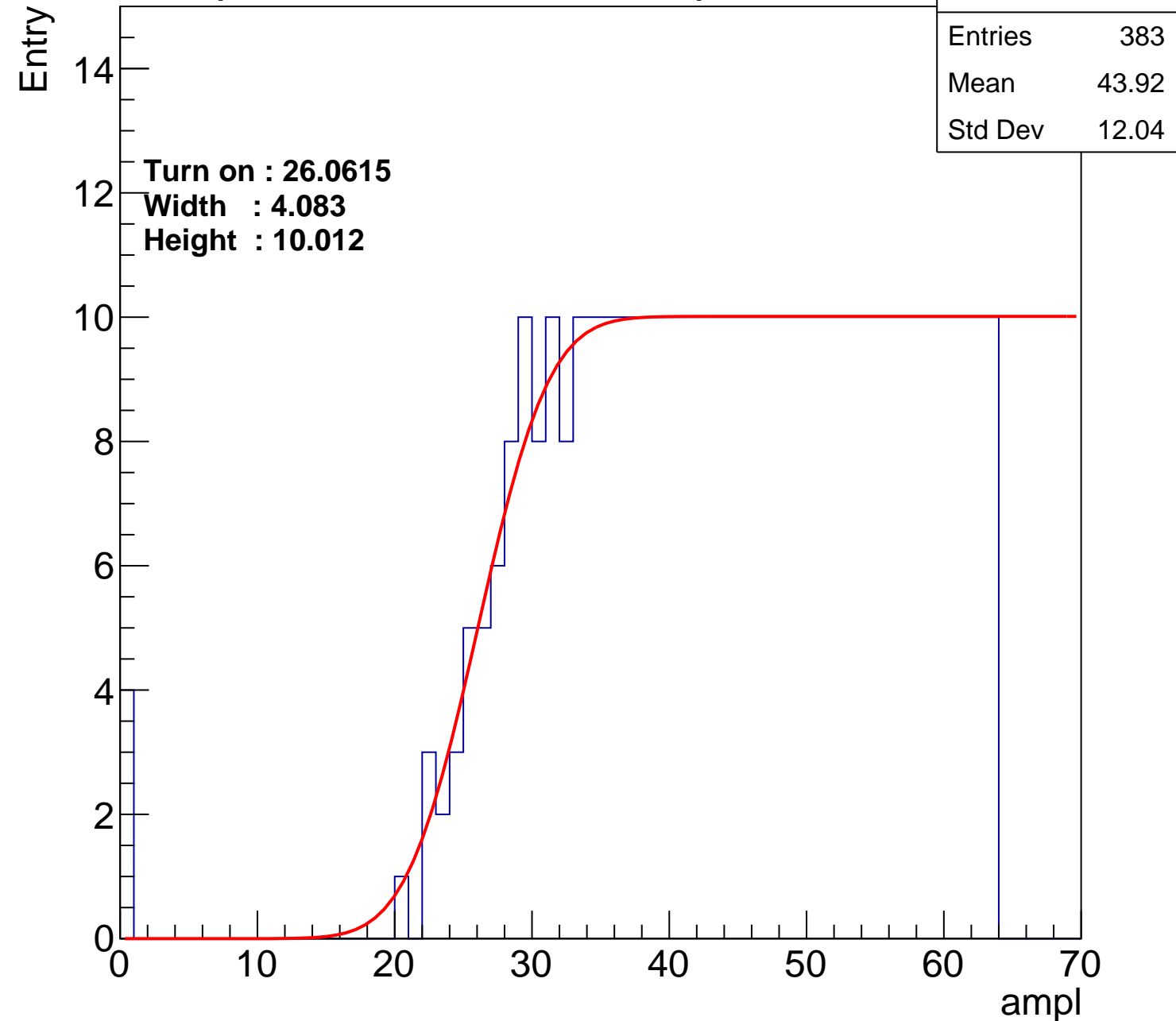
Width : 4.083

Height : 10.012

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch61

calib_packv5_042523_0143.root, FC#7, port C2

Entries	377
Mean	44.36
Std Dev	11.59

Turn on : 26.6724

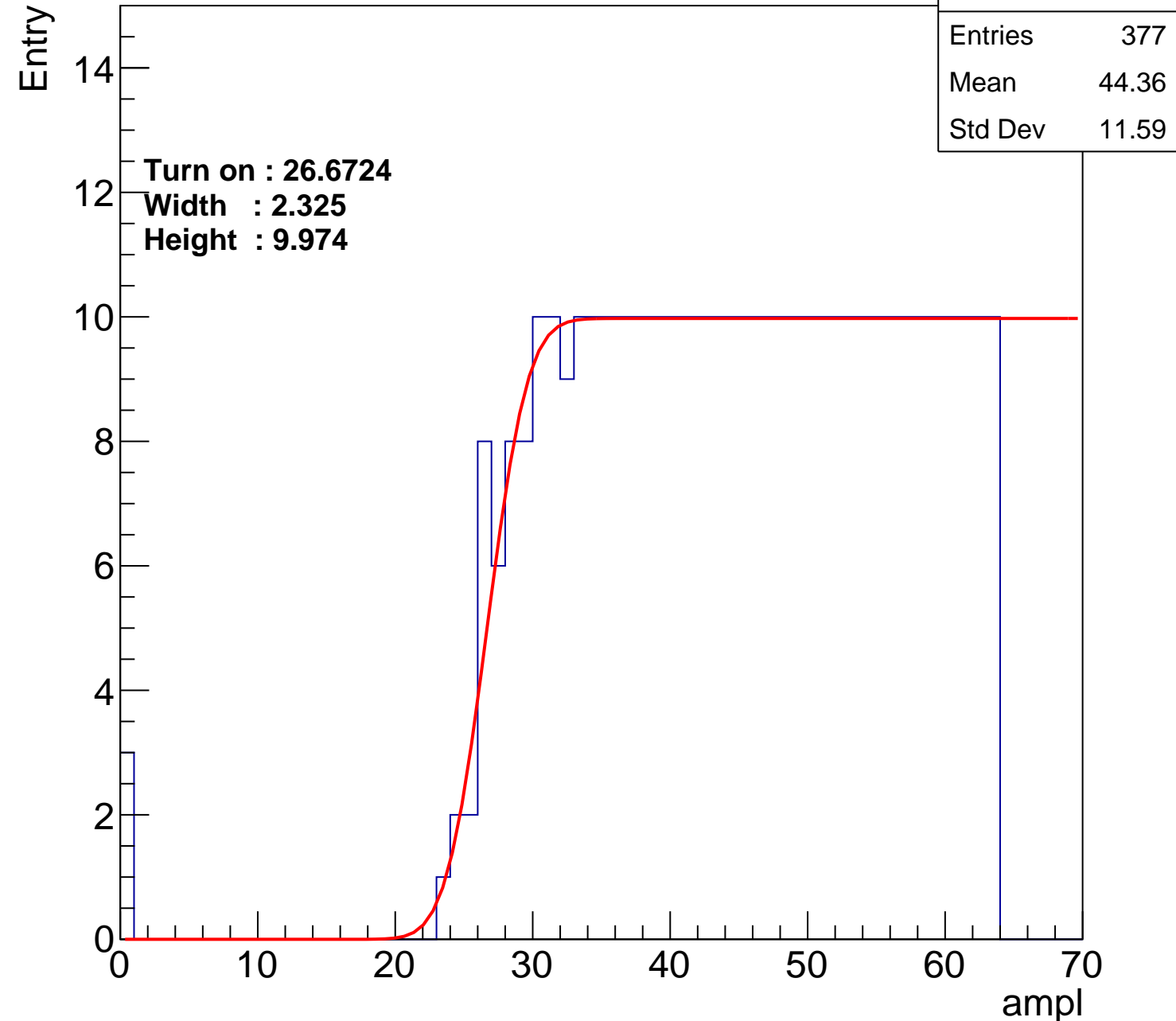
Width : 2.325

Height : 9.974

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch62

calib_packv5_042523_0143.root, FC#7, port C2

Entries	401
Mean	43.03
Std Dev	12.55

Turn on : 24.6379

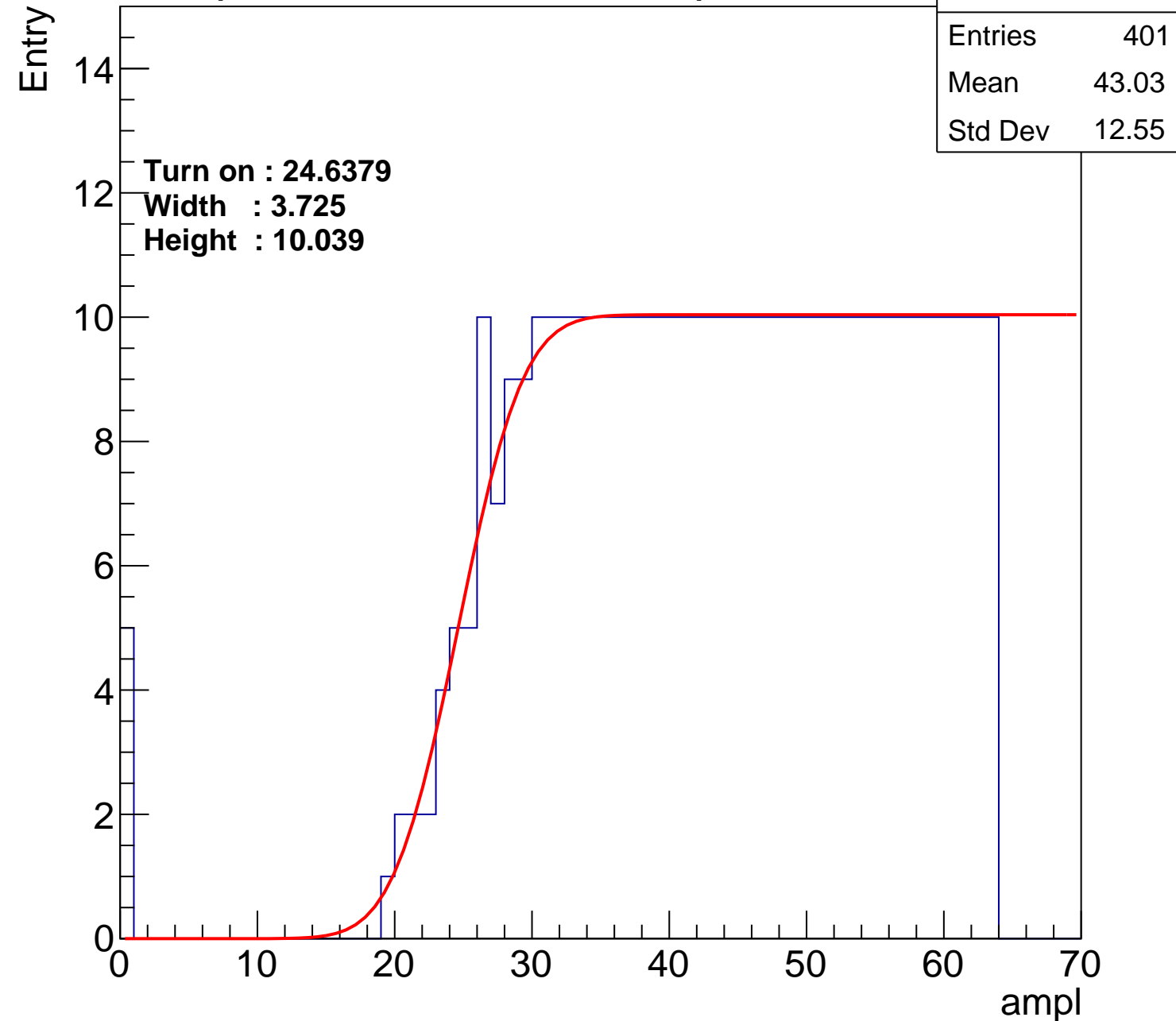
Width : 3.725

Height : 10.039

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch63

calib_packv5_042523_0143.root, FC#7, port C2

Entries	387
Mean	43.86
Std Dev	11.86

Turn on : 25.7193

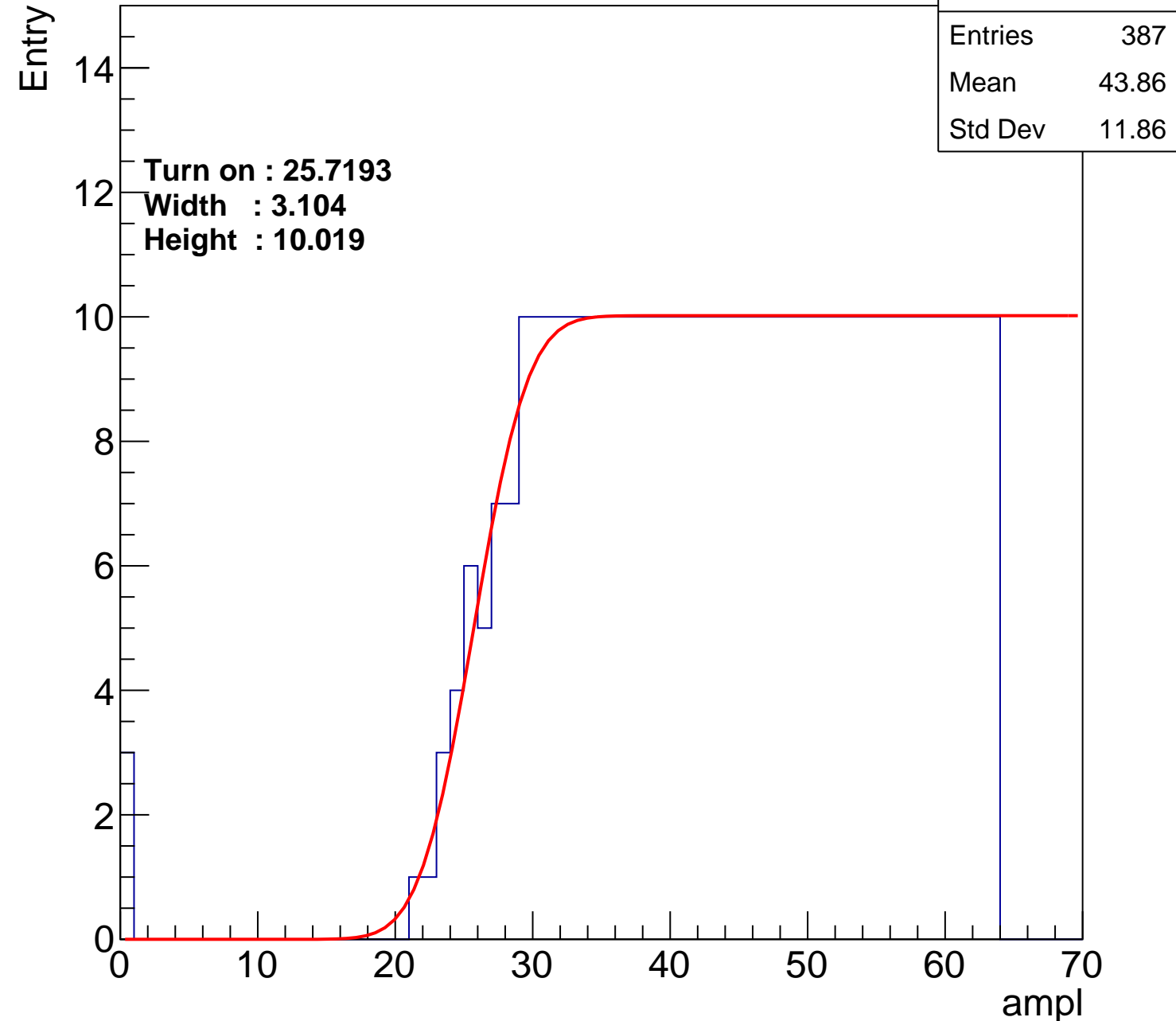
Width : 3.104

Height : 10.019

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch64

calib_packv5_042523_0143.root, FC#7, port C2

Entries	387
Mean	43.95
Std Dev	11.58

Turn on : 25.5105

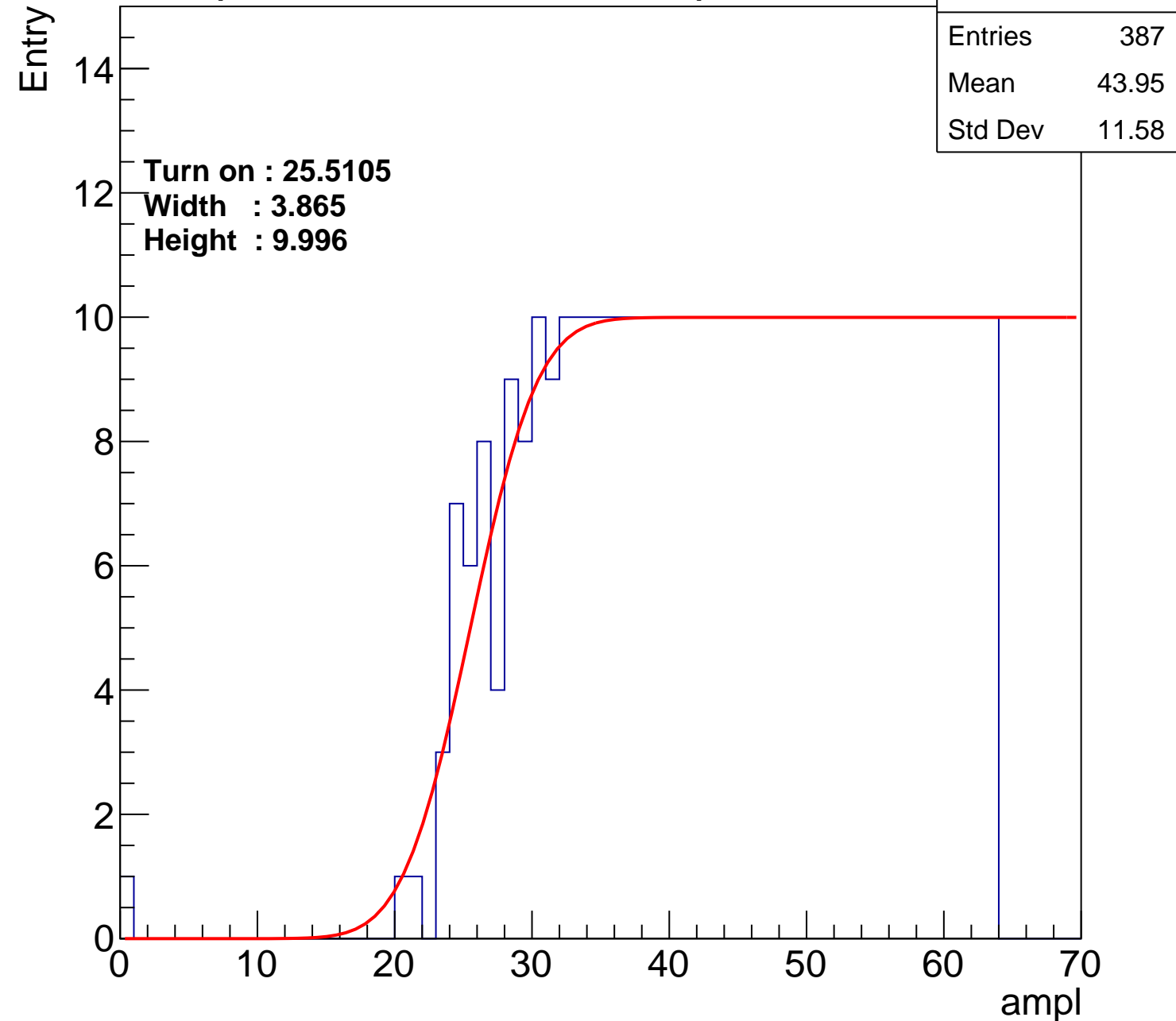
Width : 3.865

Height : 9.996

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch65

calib_packv5_042523_0143.root, FC#7, port C2

Entries	367
Mean	44.9
Std Dev	11.09

Turn on : 27.6923

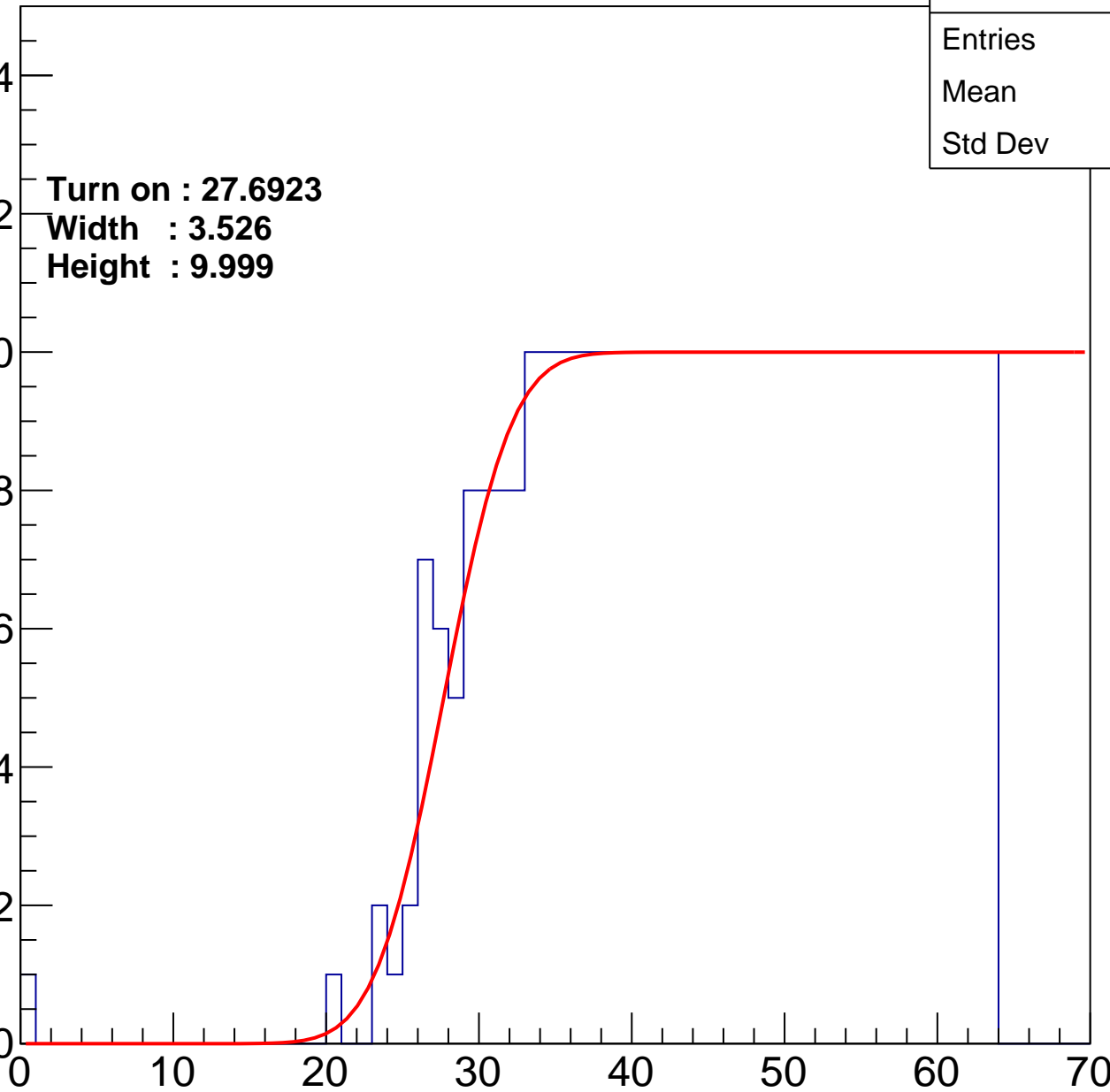
Width : 3.526

Height : 9.999

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch66

calib_packv5_042523_0143.root, FC#7, port C2

Entries	390
Mean	43.55
Std Dev	12.31

Turn on : 25.8179

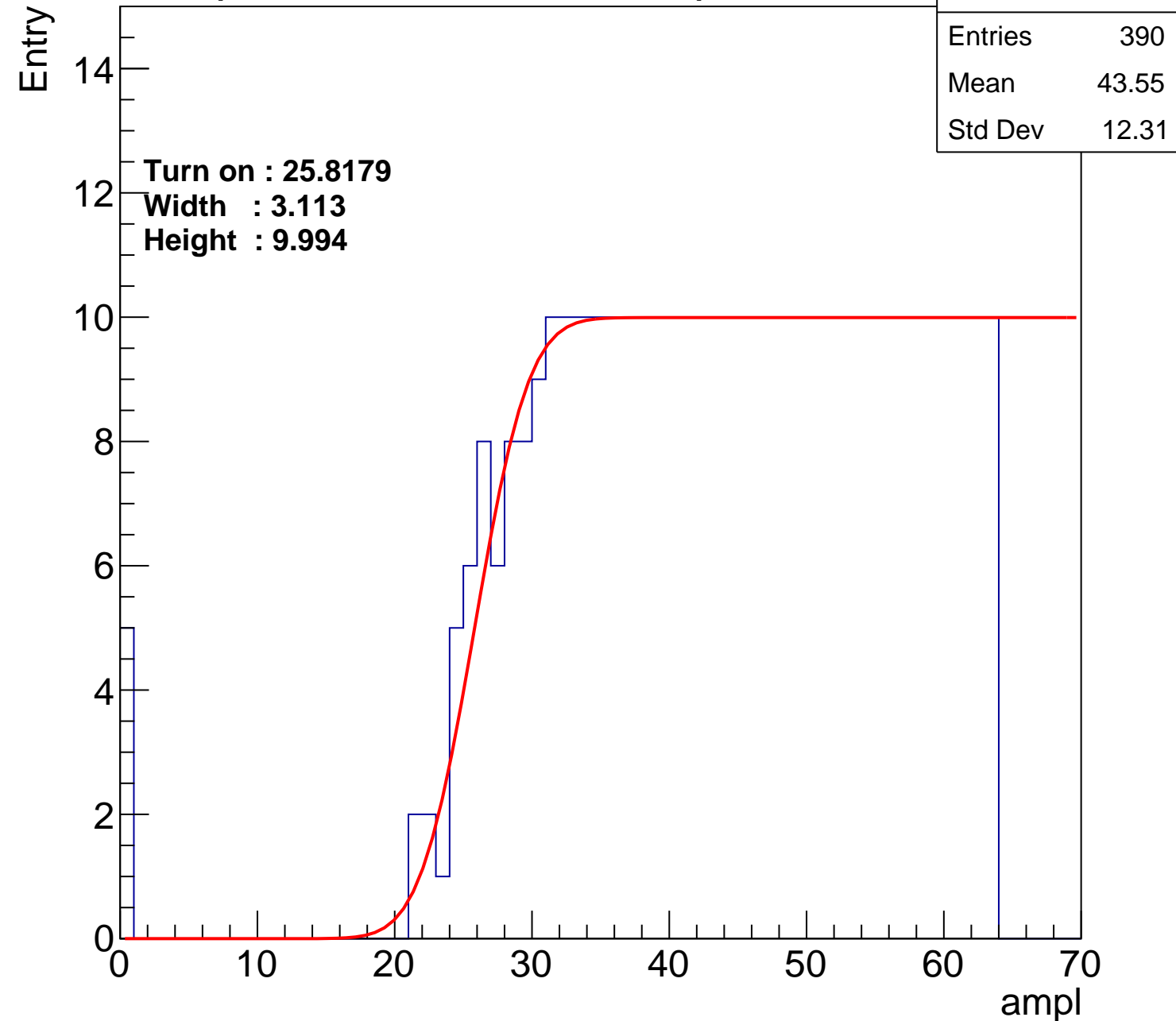
Width : 3.113

Height : 9.994

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch67

calib_packv5_042523_0143.root, FC#7, port C2

Entries	384
Mean	43.98
Std Dev	11.82

Turn on : 26.1793

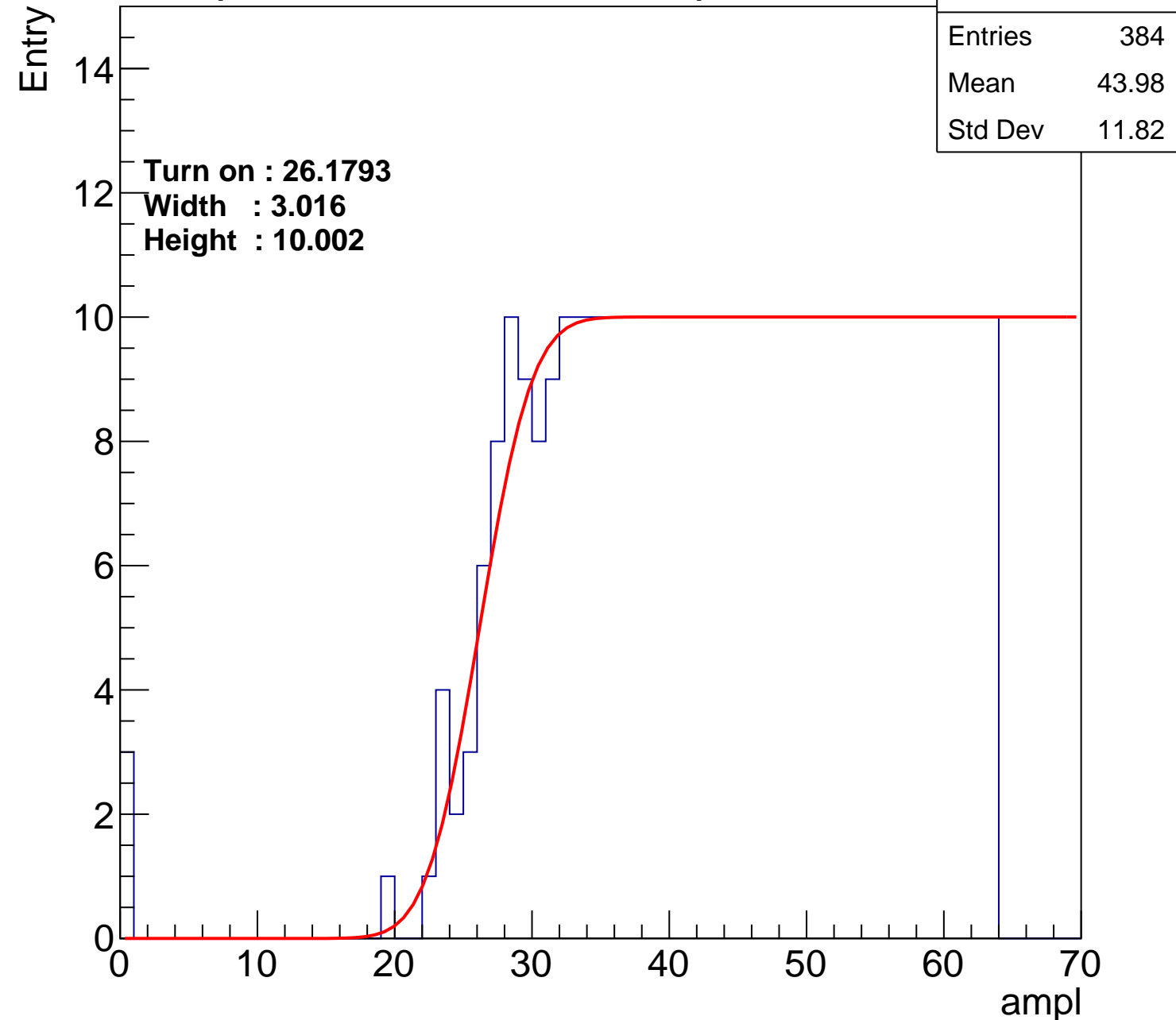
Width : 3.016

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch68

calib_packv5_042523_0143.root, FC#7, port C2

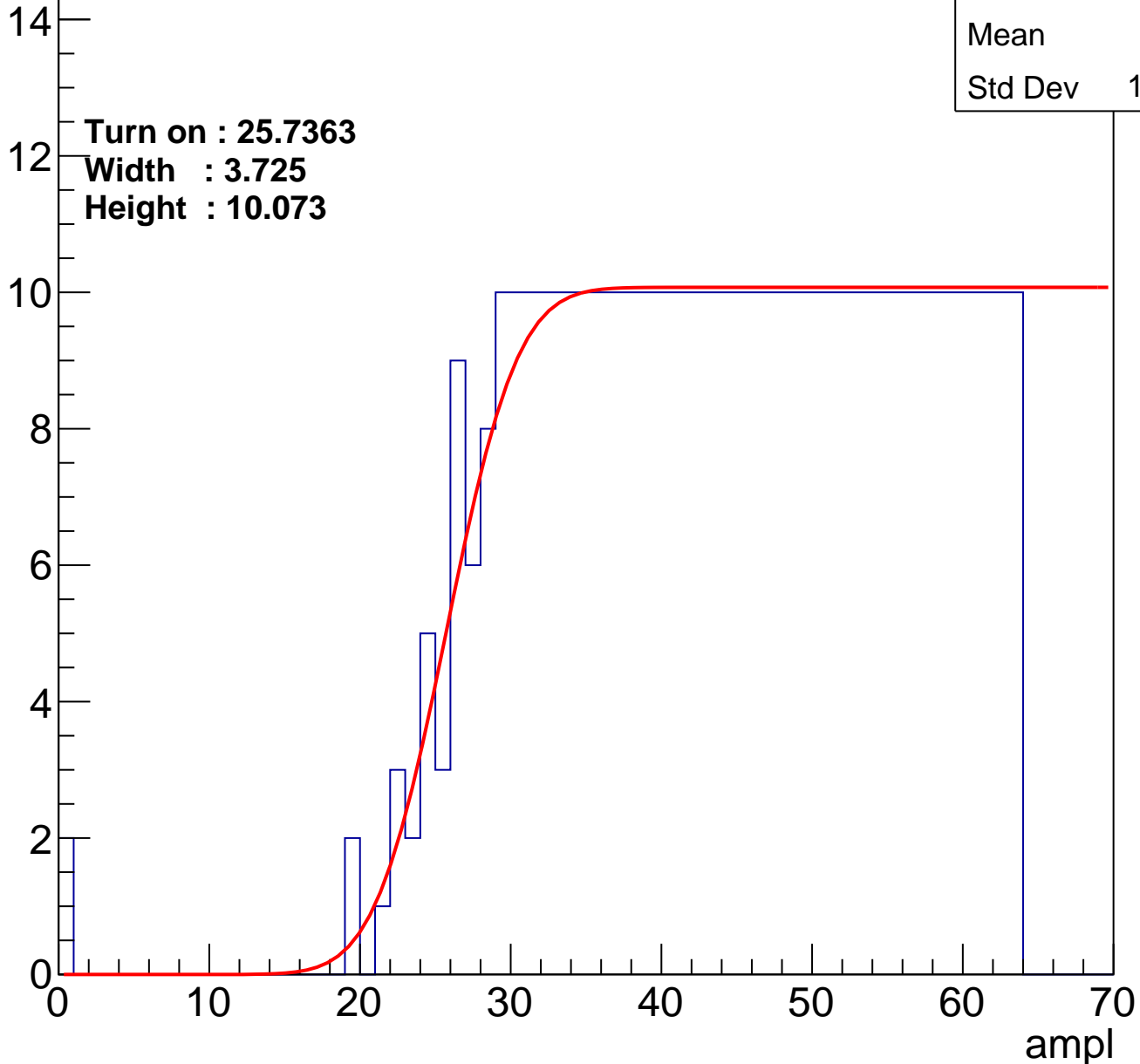
Entries	391
Mean	43.7
Std Dev	11.84

Turn on : 25.7363

Width : 3.725

Height : 10.073

Entry



B1L103S, U2-ch69

calib_packv5_042523_0143.root, FC#7, port C2

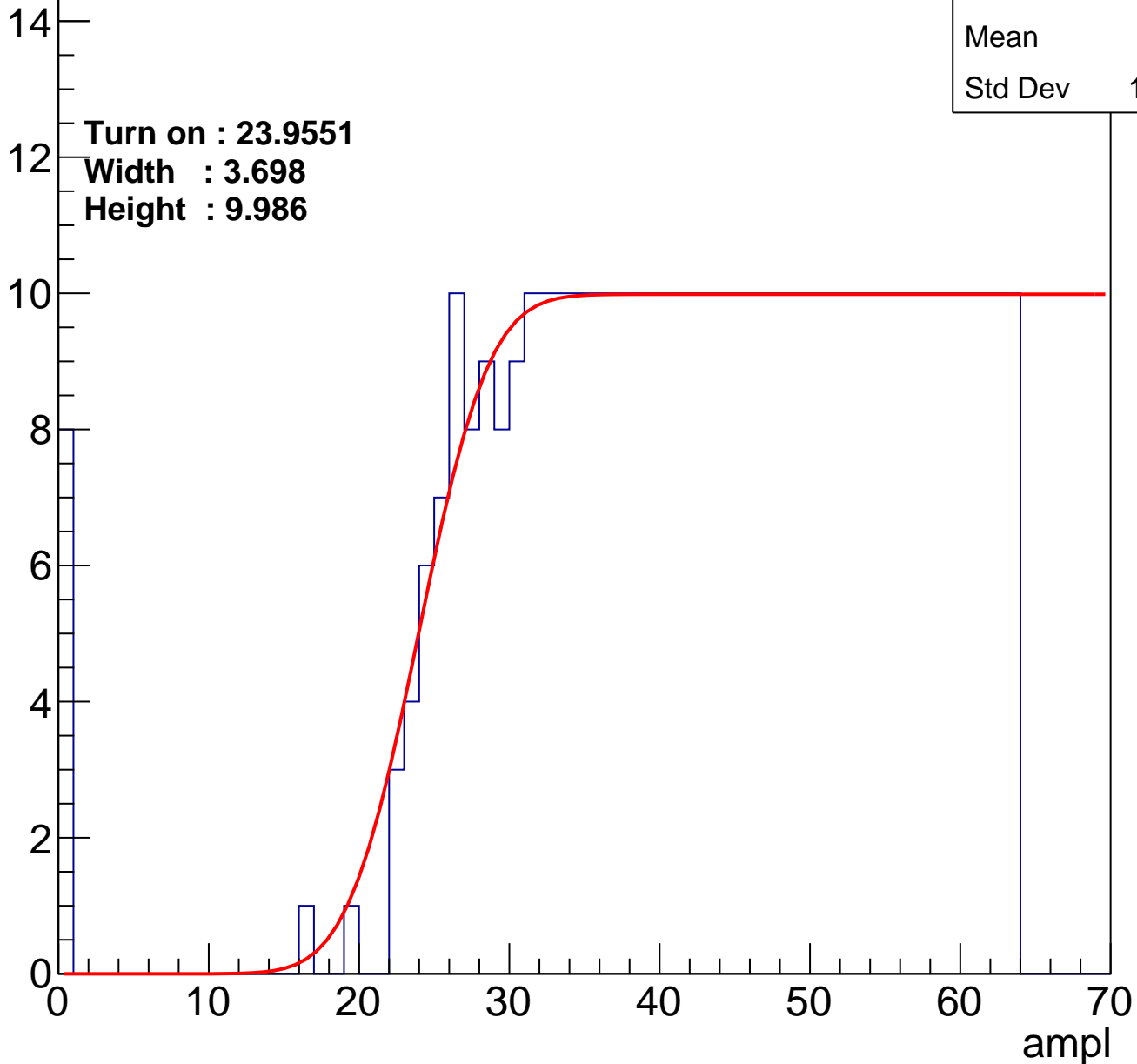
Entries	404
Mean	42.7
Std Dev	13.04

Turn on : 23.9551

Width : 3.698

Height : 9.986

Entry



B1L103S, U2-ch70

calib_packv5_042523_0143.root, FC#7, port C2

Entries	386
Mean	44
Std Dev	11.55

Turn on : 26.3450

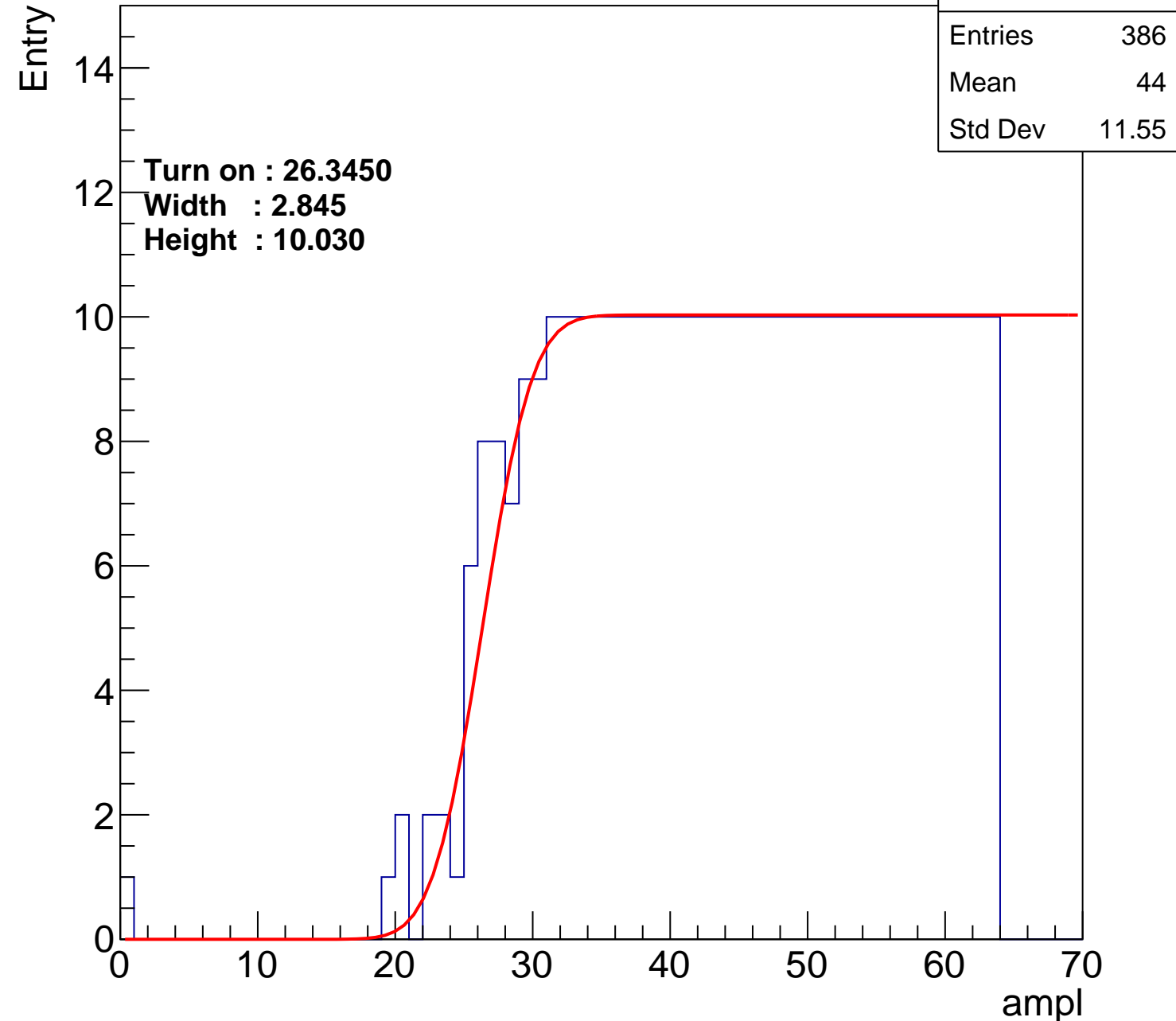
Width : 2.845

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch71

calib_packv5_042523_0143.root, FC#7, port C2

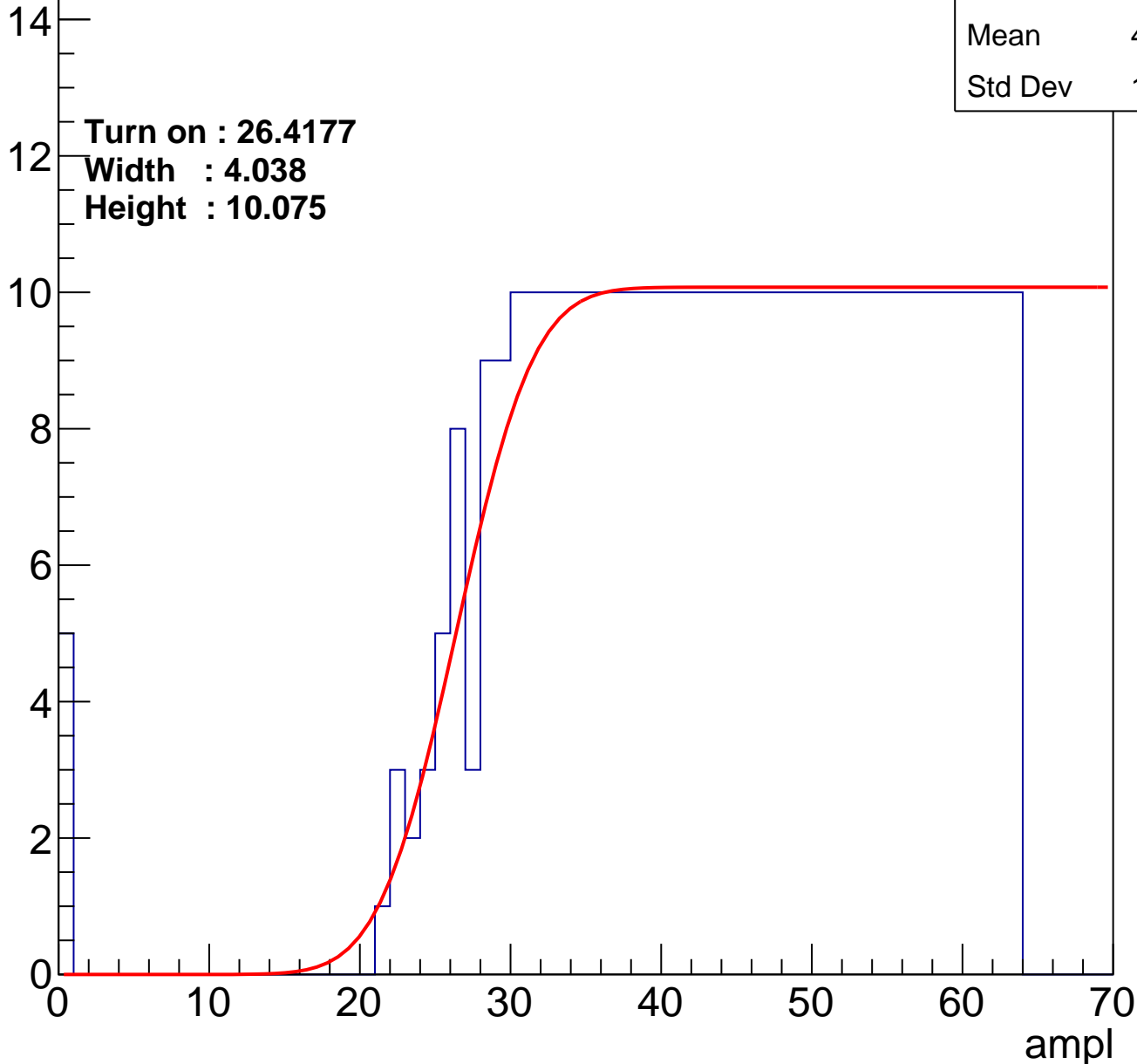
Entries	388
Mean	43.66
Std Dev	12.24

Turn on : 26.4177

Width : 4.038

Height : 10.075

Entry



B1L103S, U2-ch72

calib_packv5_042523_0143.root, FC#7, port C2

Entries	401
Mean	43.05
Std Dev	12.45

Turn on : 24.1806

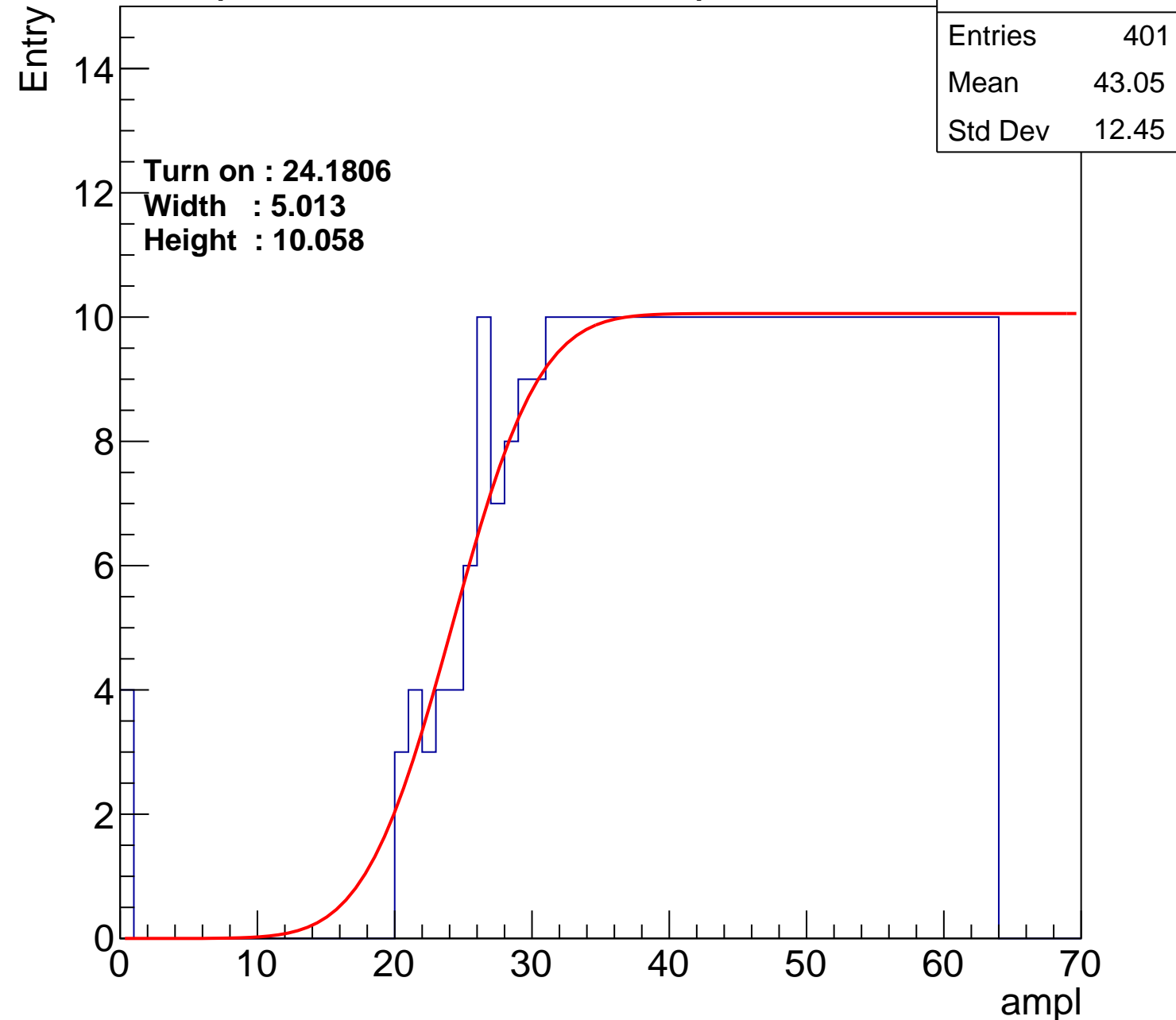
Width : 5.013

Height : 10.058

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch73

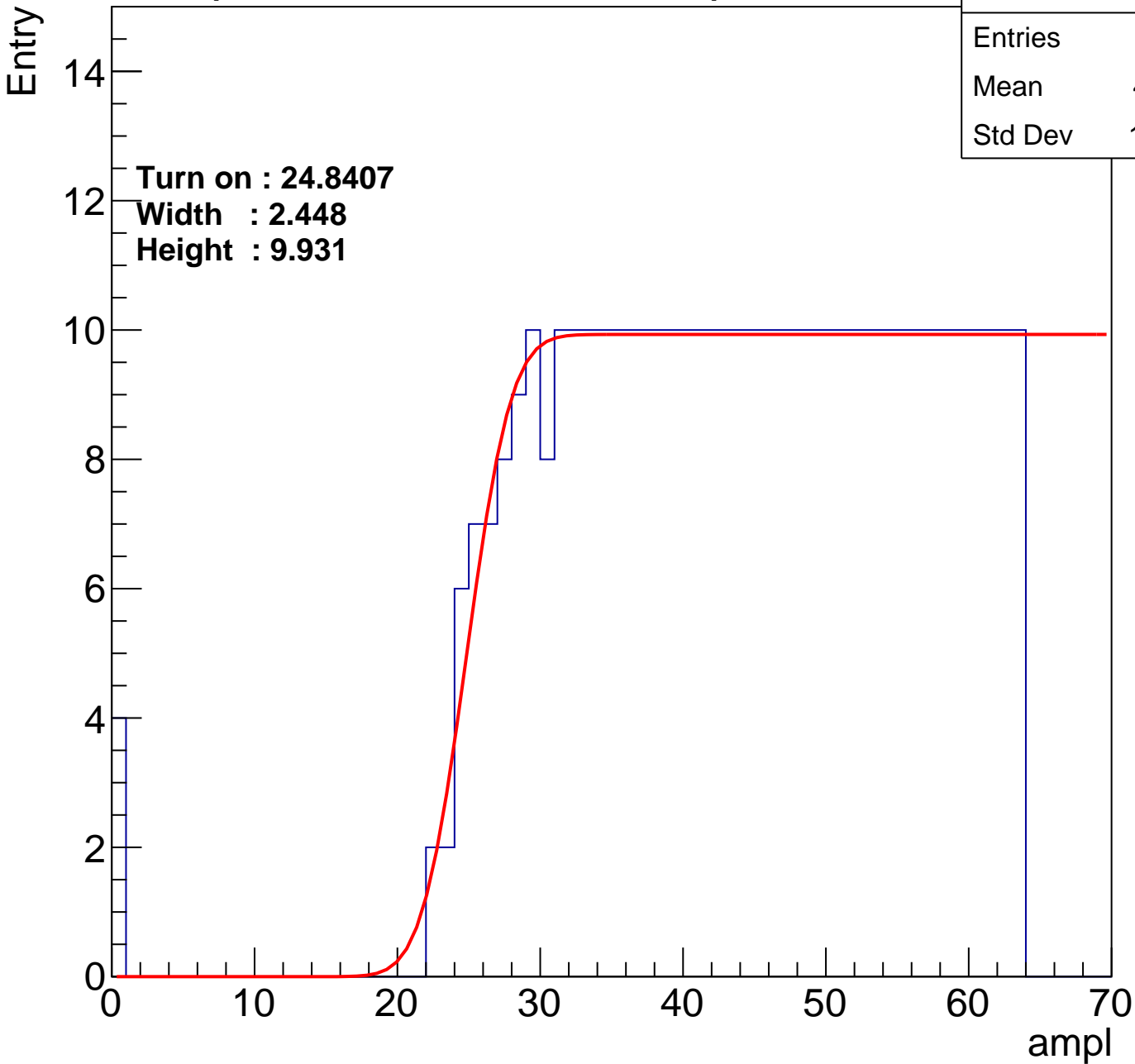
calib_packv5_042523_0143.root, FC#7, port C2

Turn on : 24.8407

Width : 2.448

Height : 9.931

Entries	393
Mean	43.51
Std Dev	12.15



B1L103S, U2-ch74

calib_packv5_042523_0143.root, FC#7, port C2

Entries	389
Mean	43.9
Std Dev	11.55

Turn on : 25.2568

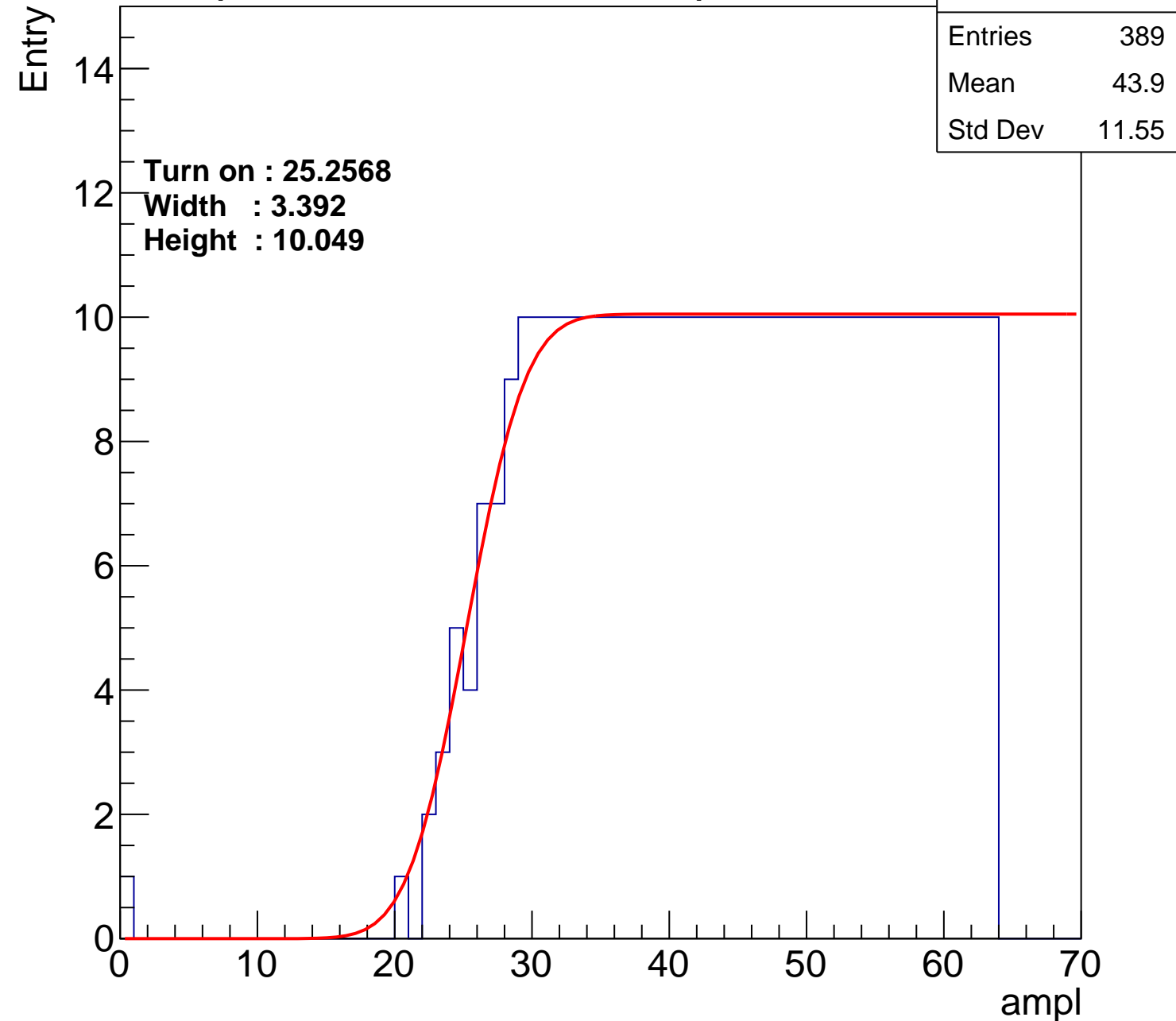
Width : 3.392

Height : 10.049

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch75

calib_packv5_042523_0143.root, FC#7, port C2

Entries	371
Mean	44.77
Std Dev	11.09

Turn on : 27.0792

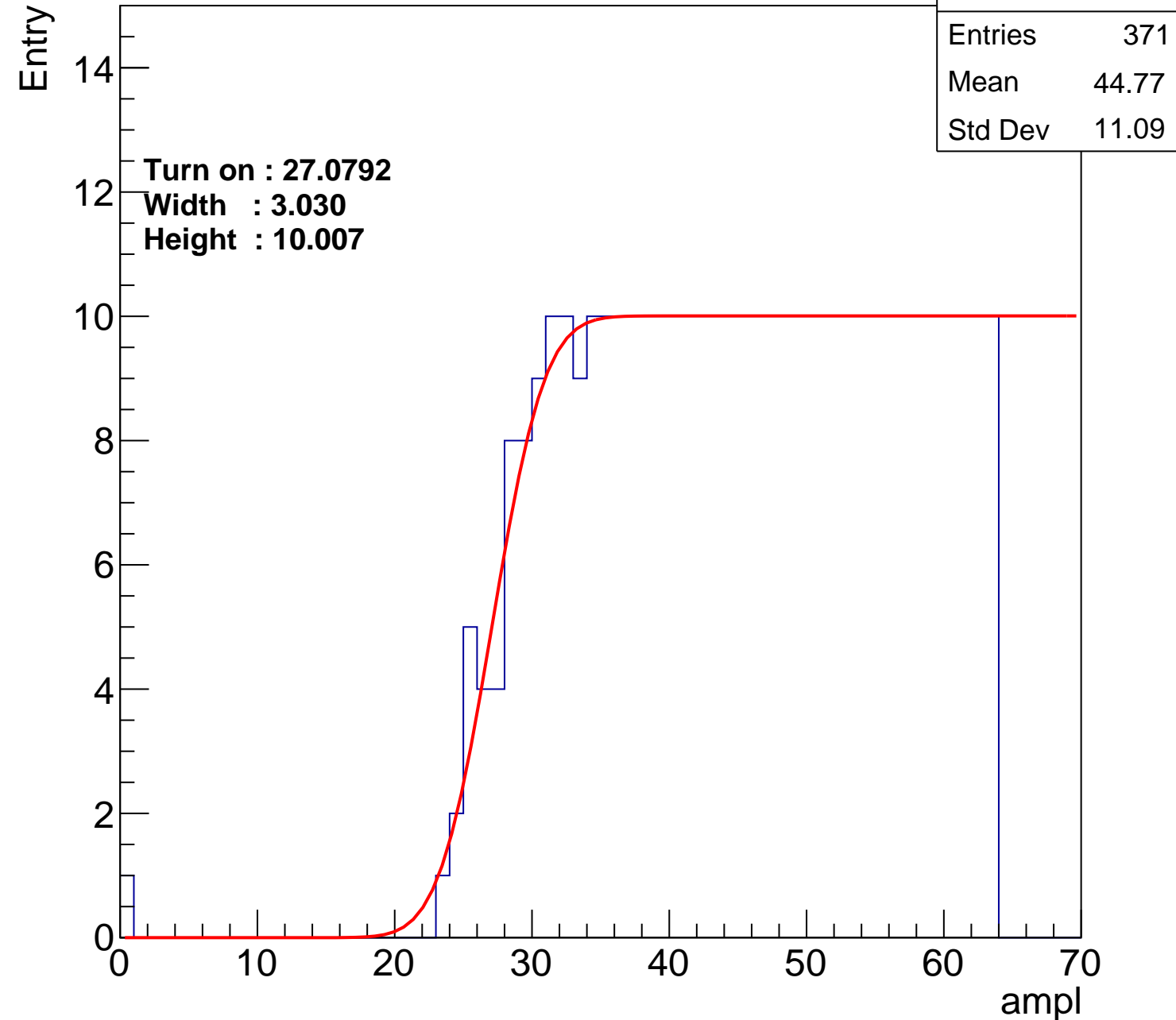
Width : 3.030

Height : 10.007

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch76

calib_packv5_042523_0143.root, FC#7, port C2

Entries	391
Mean	43.7
Std Dev	11.84

Turn on : 24.9815

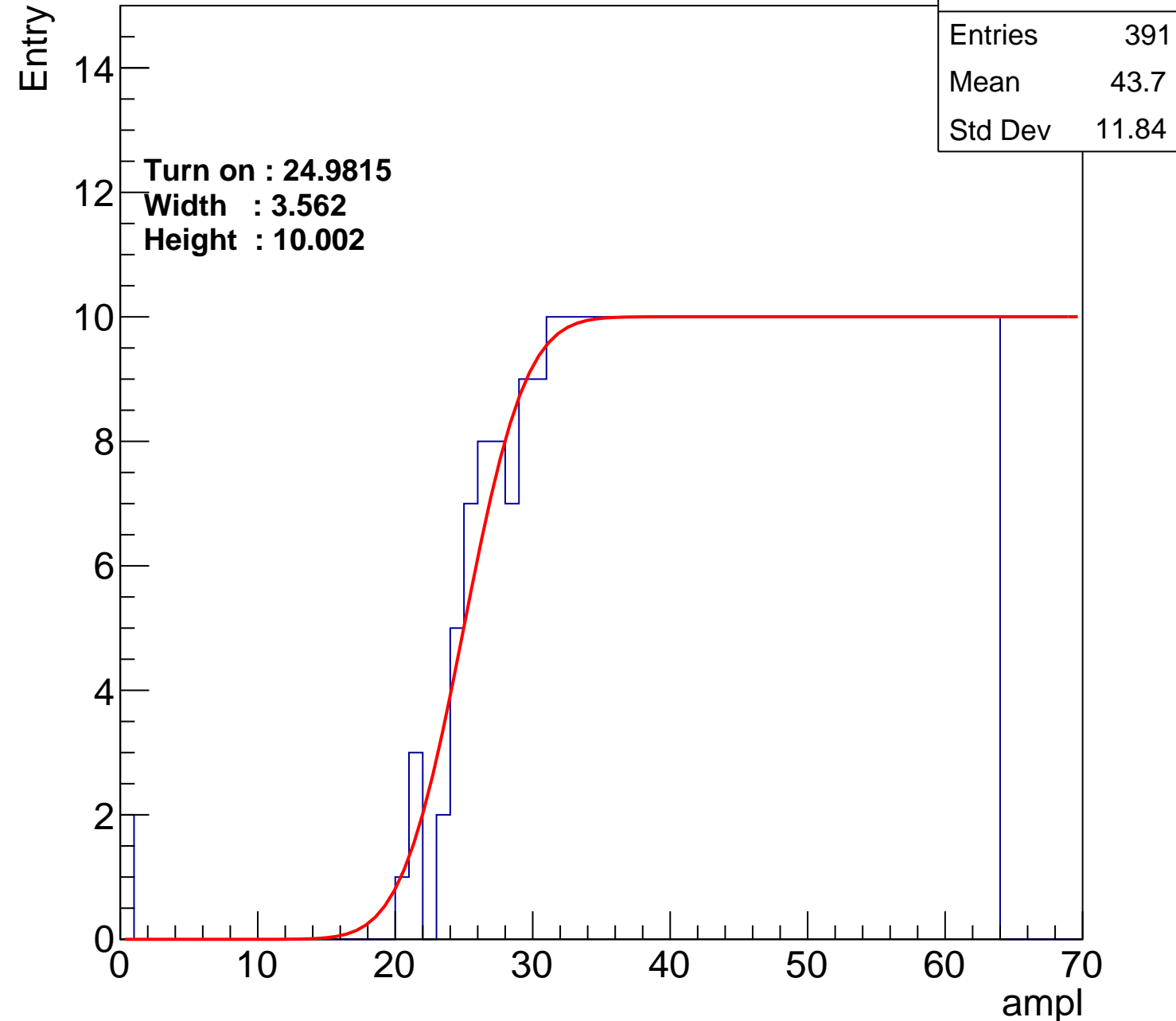
Width : 3.562

Height : 10.002

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch77

calib_packv5_042523_0143.root, FC#7, port C2

Entries	379
Mean	44.26
Std Dev	11.65

Turn on : 26.6933

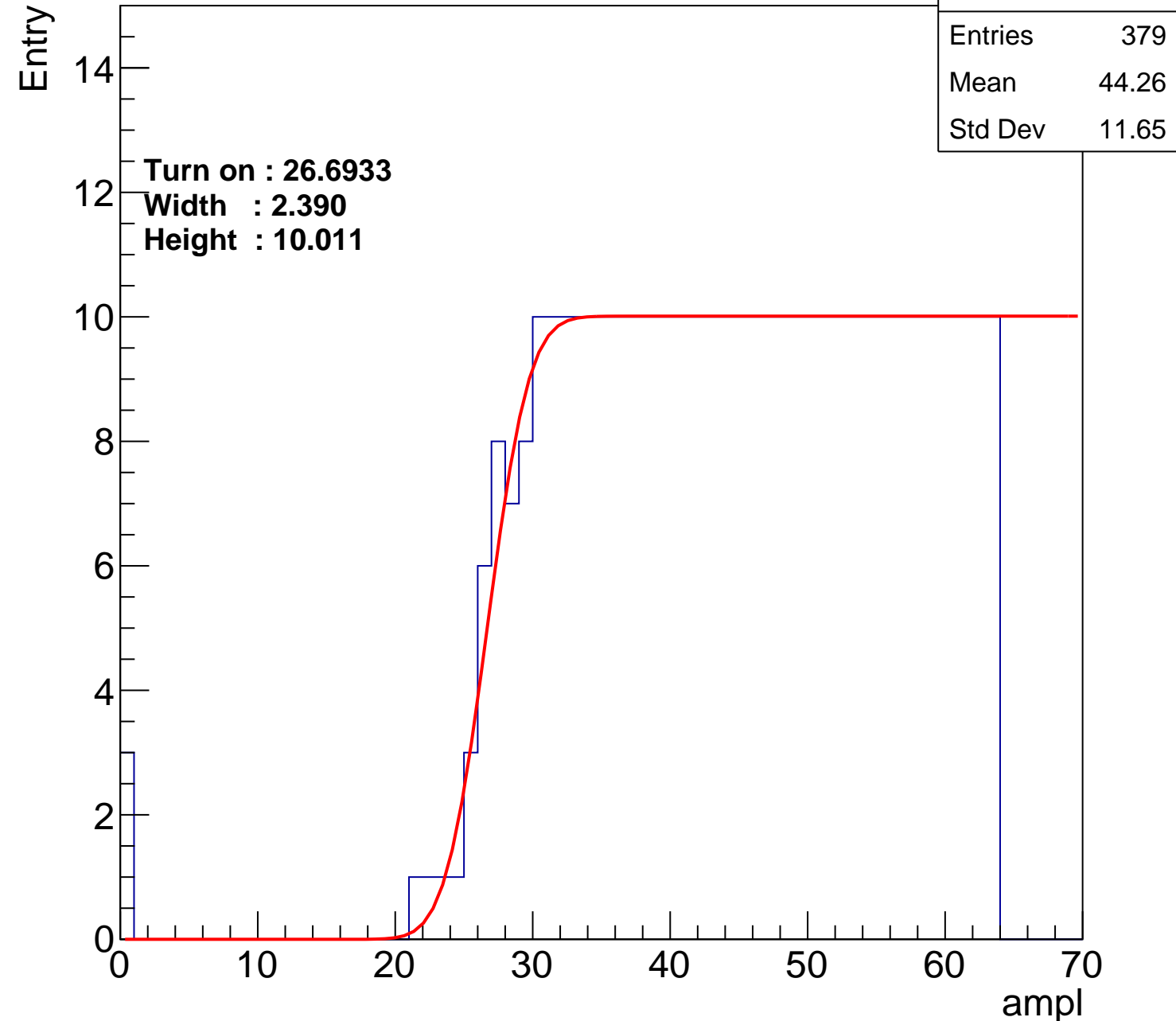
Width : 2.390

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch78

calib_packv5_042523_0143.root, FC#7, port C2

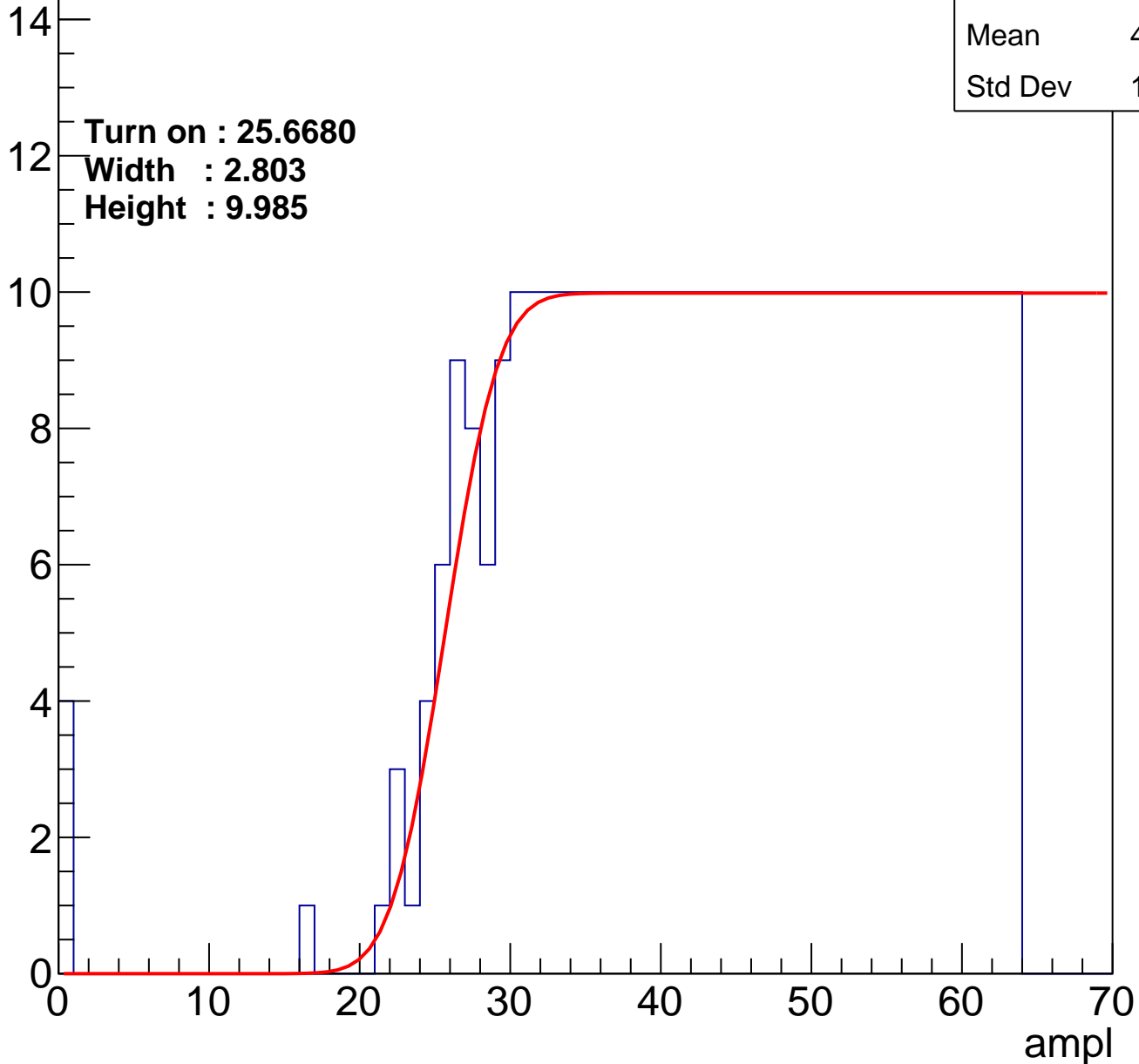
Entries	392
Mean	43.52
Std Dev	12.19

Turn on : 25.6680

Width : 2.803

Height : 9.985

Entry



B1L103S, U2-ch79

calib_packv5_042523_0143.root, FC#7, port C2

Entries	385
Mean	44.05
Std Dev	11.52

Turn on : 25.7486

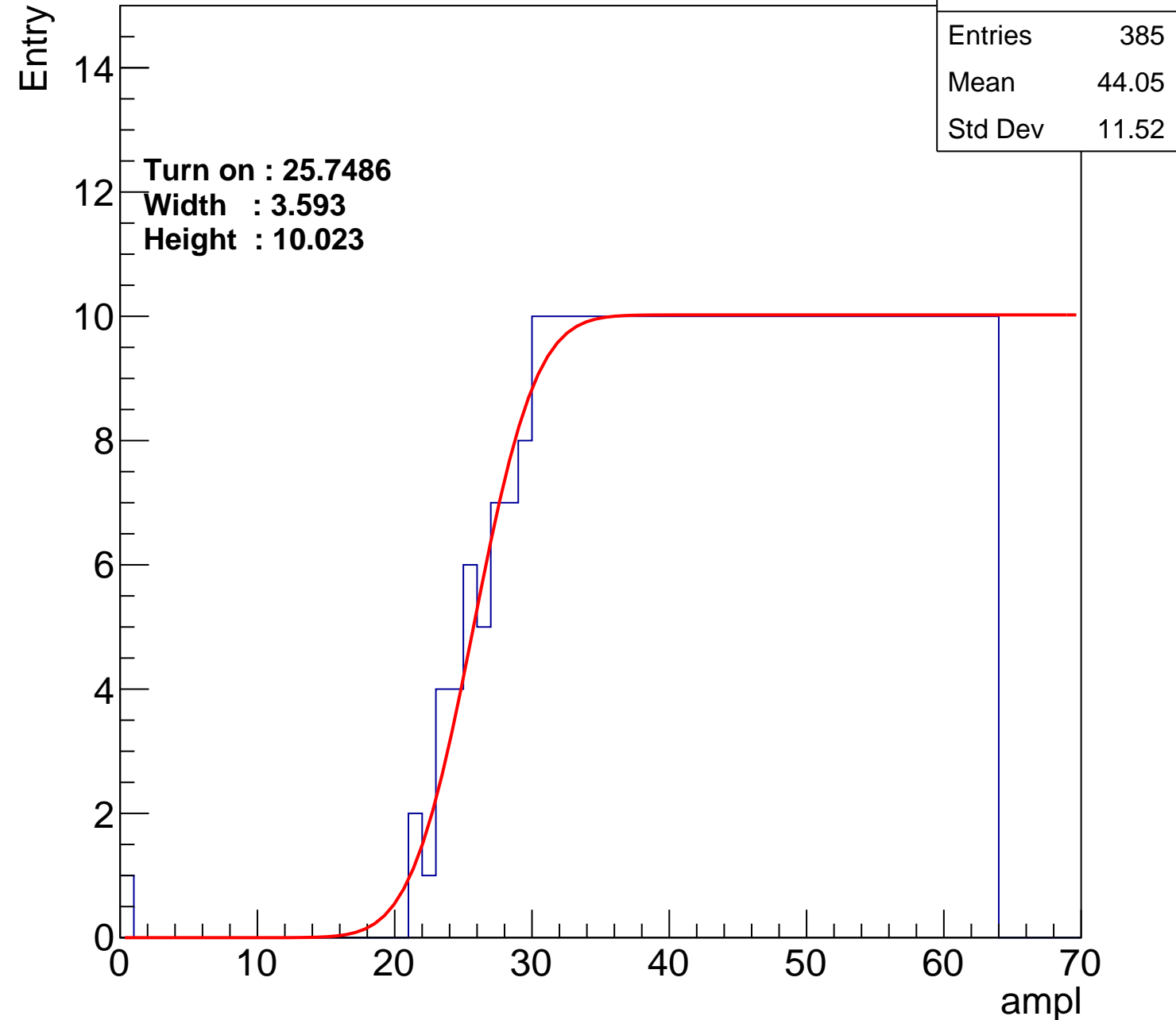
Width : 3.593

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch80

calib_packv5_042523_0143.root, FC#7, port C2

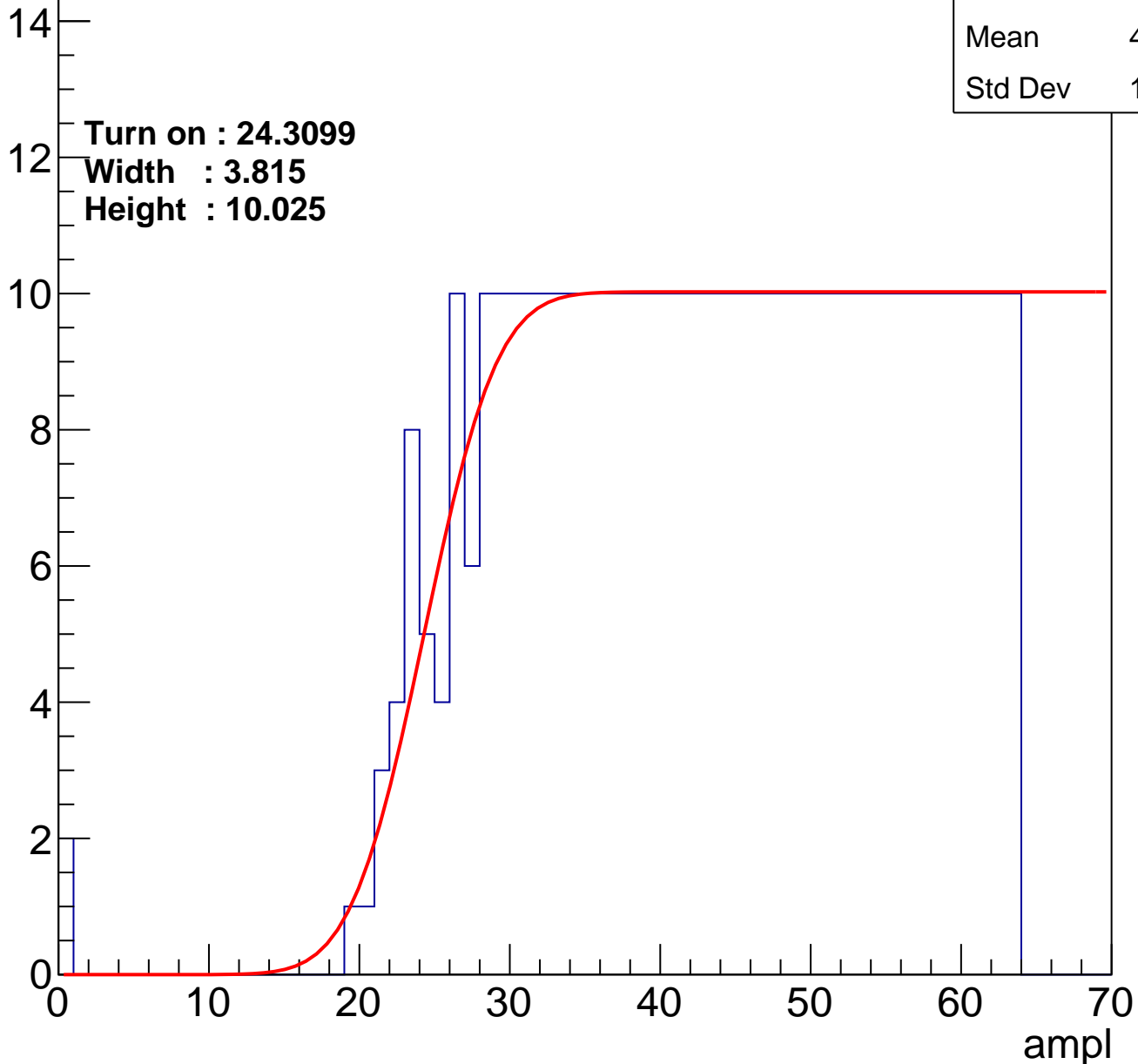
Entries	404
Mean	43.06
Std Dev	12.17

Turn on : 24.3099

Width : 3.815

Height : 10.025

Entry



B1L103S, U2-ch81

calib_packv5_042523_0143.root, FC#7, port C2

Entries	387
Mean	43.75
Std Dev	12.09

Turn on : 25.7904

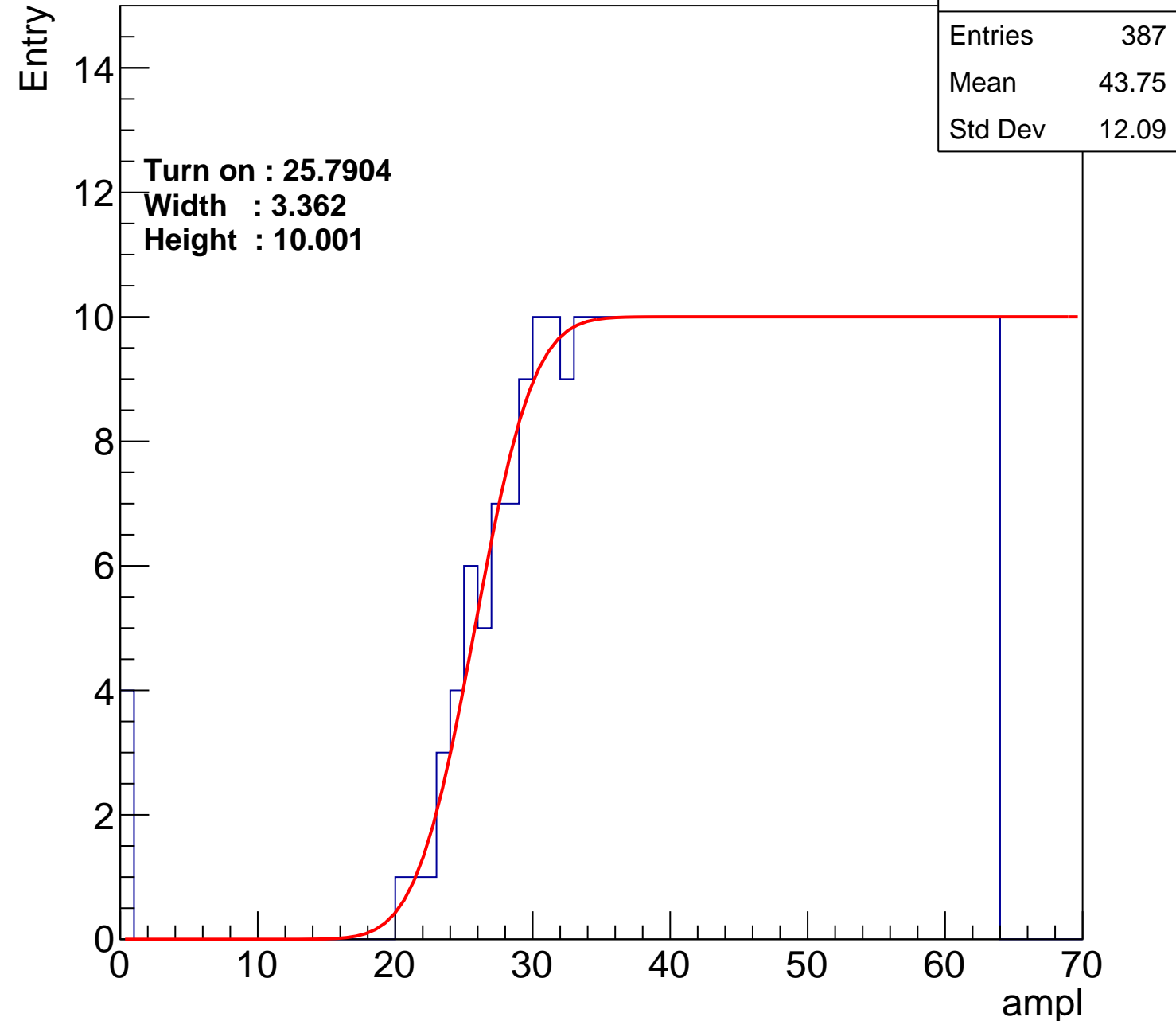
Width : 3.362

Height : 10.001

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch82

calib_packv5_042523_0143.root, FC#7, port C2

Entries	386
Mean	43.84
Std Dev	12

Turn on : 25.9444

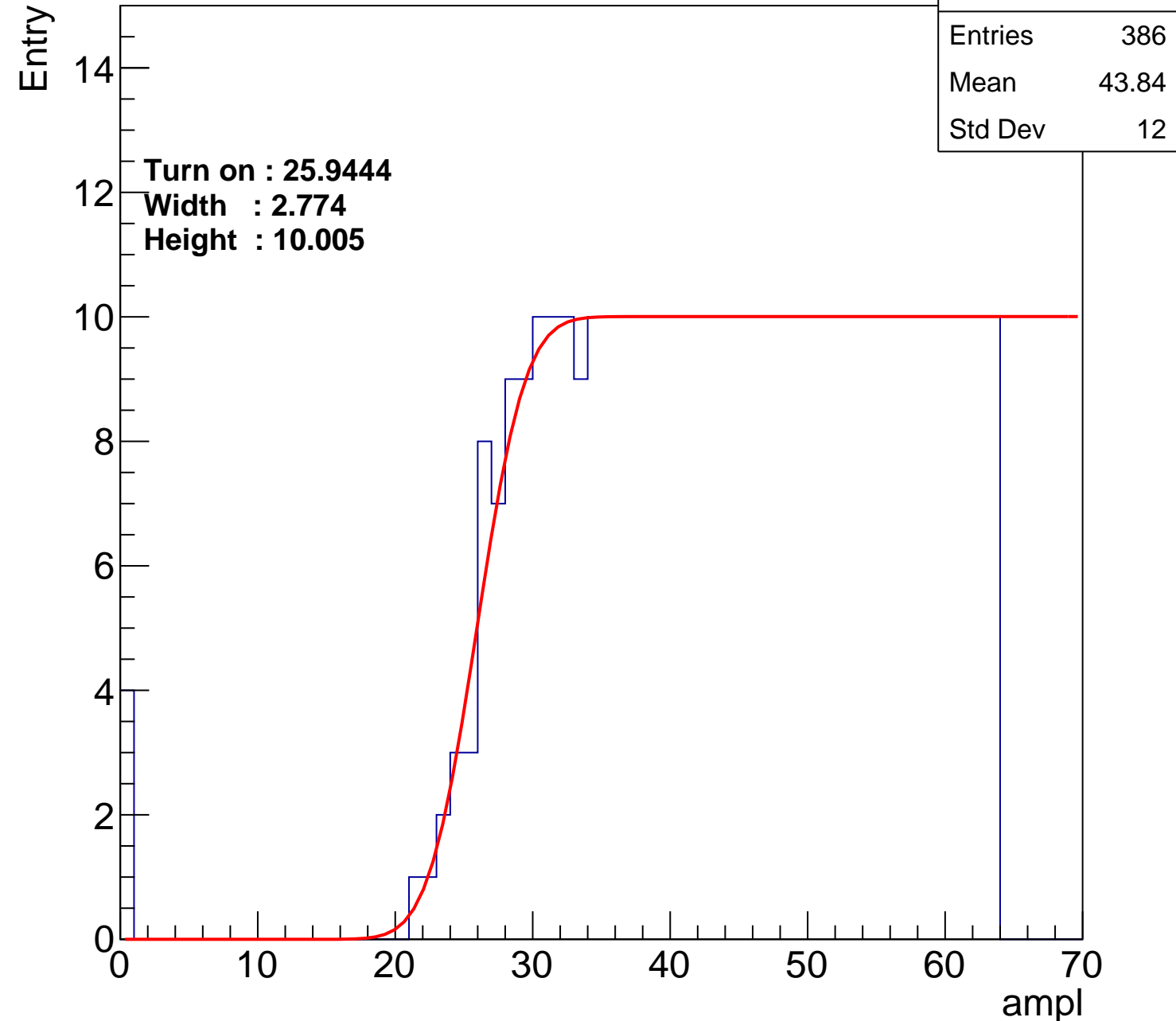
Width : 2.774

Height : 10.005

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch83

calib_packv5_042523_0143.root, FC#7, port C2

Entries	381
Mean	44.06
Std Dev	11.92

Turn on : 26.6629

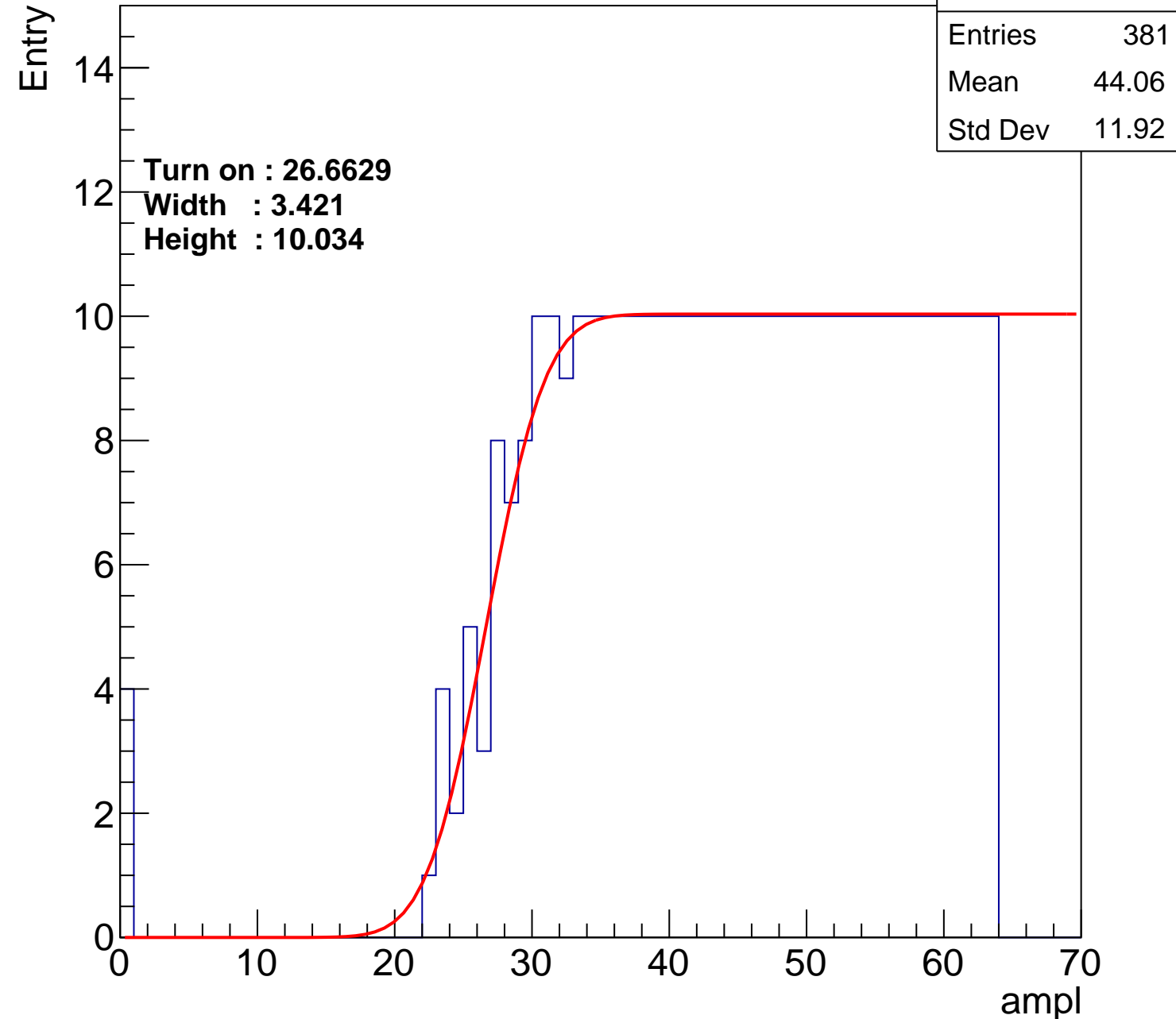
Width : 3.421

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch84

calib_packv5_042523_0143.root, FC#7, port C2

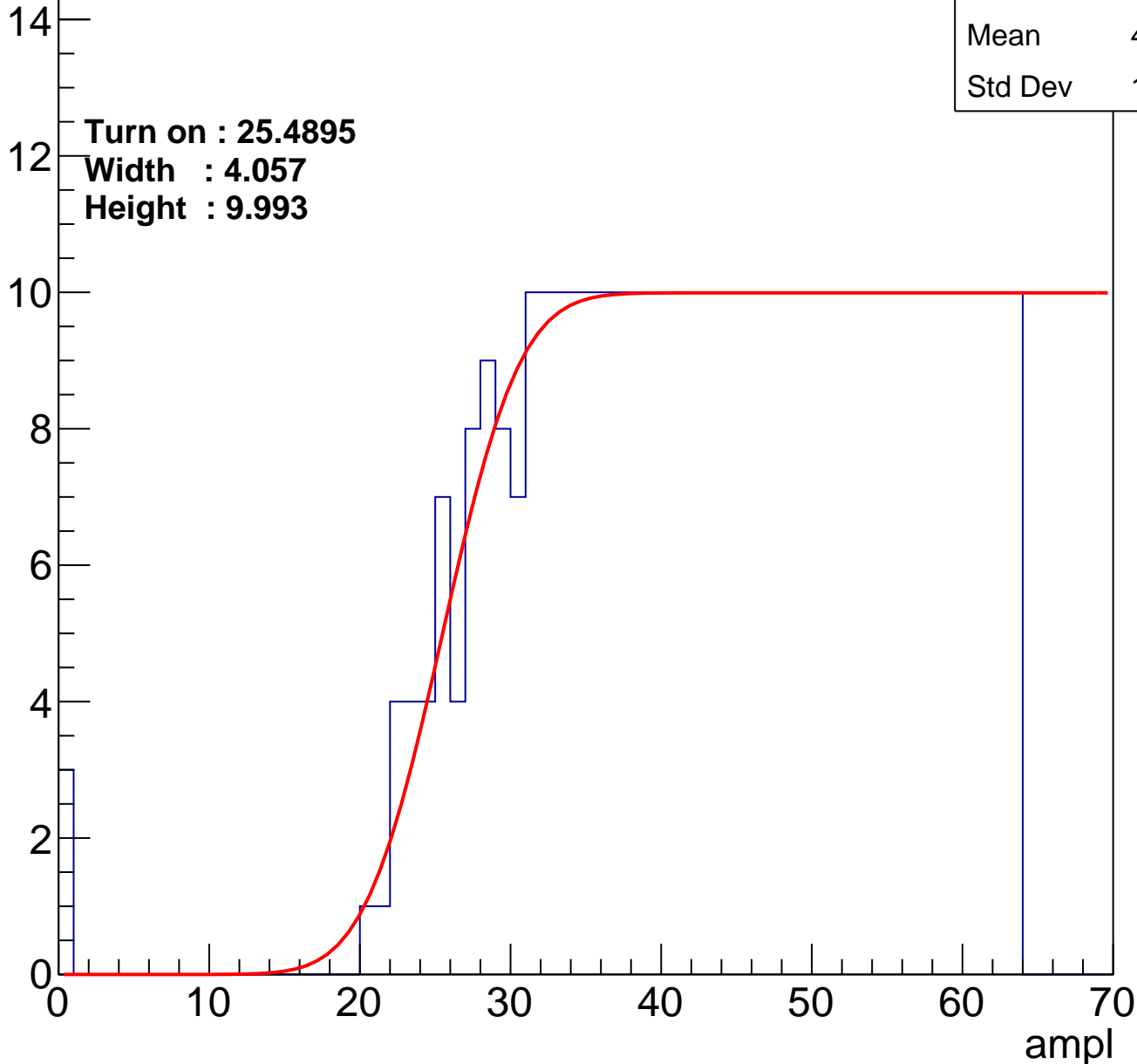
Entries	390
Mean	43.63
Std Dev	12.05

Turn on : 25.4895

Width : 4.057

Height : 9.993

Entry



B1L103S, U2-ch85

calib_packv5_042523_0143.root, FC#7, port C2

Entries	382
Mean	44.27
Std Dev	11.32

Turn on : 25.5842

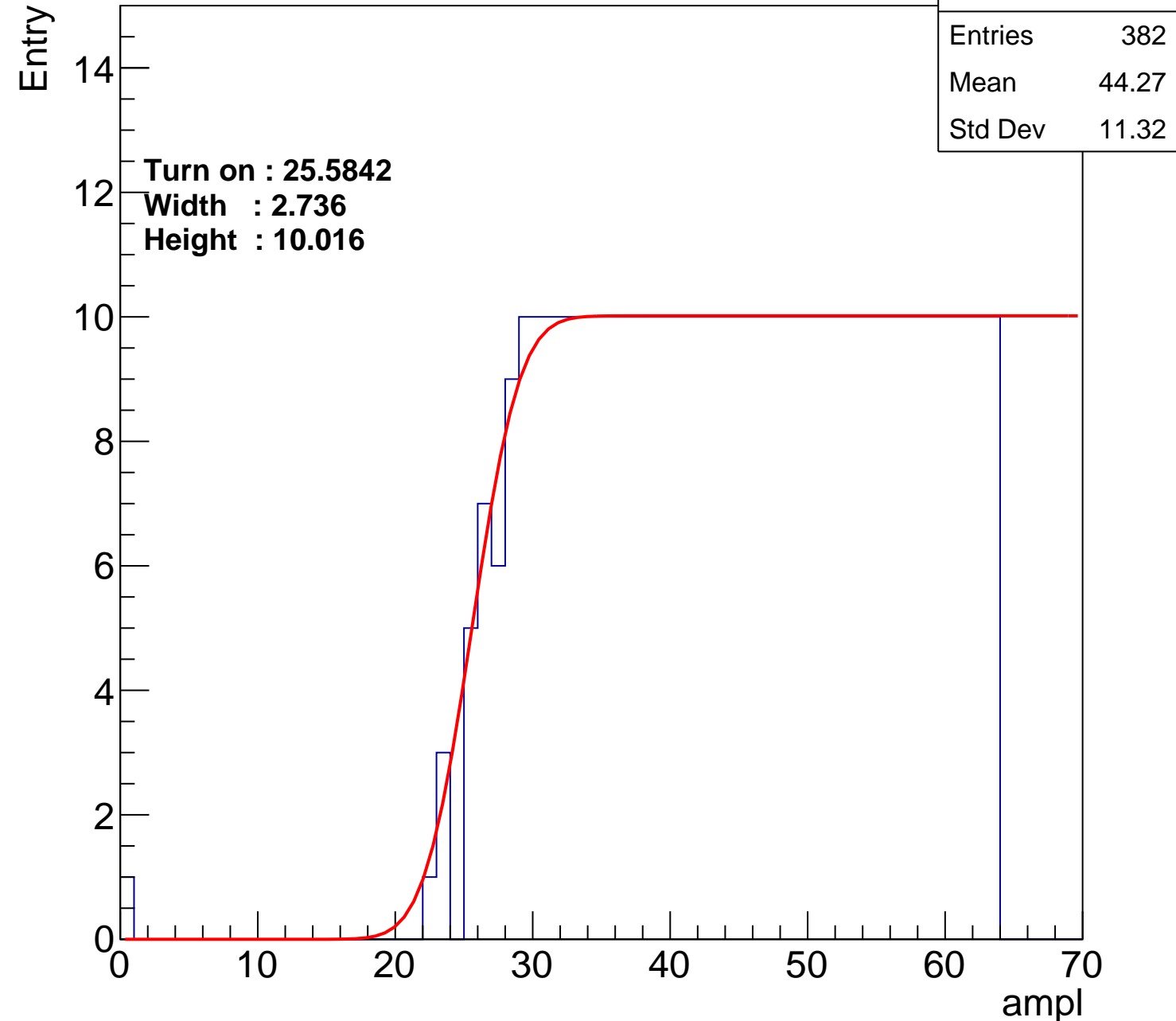
Width : 2.736

Height : 10.016

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch86

calib_packv5_042523_0143.root, FC#7, port C2

Entries	377
Mean	44.38
Std Dev	11.49

Turn on : 26.3119

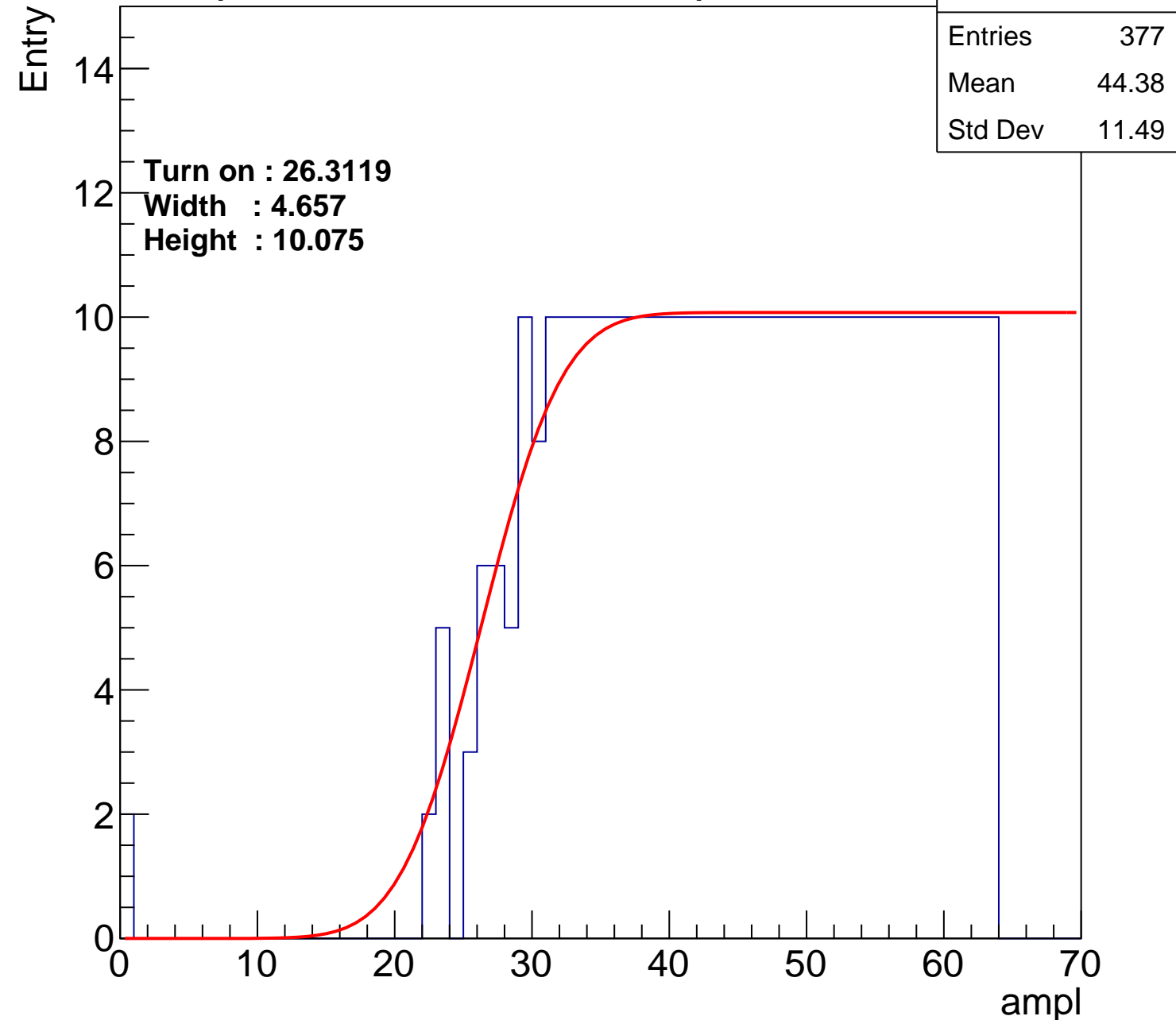
Width : 4.657

Height : 10.075

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch87

calib_packv5_042523_0143.root, FC#7, port C2

Entries	377
Mean	44.24
Std Dev	11.86

Turn on : 27.3491

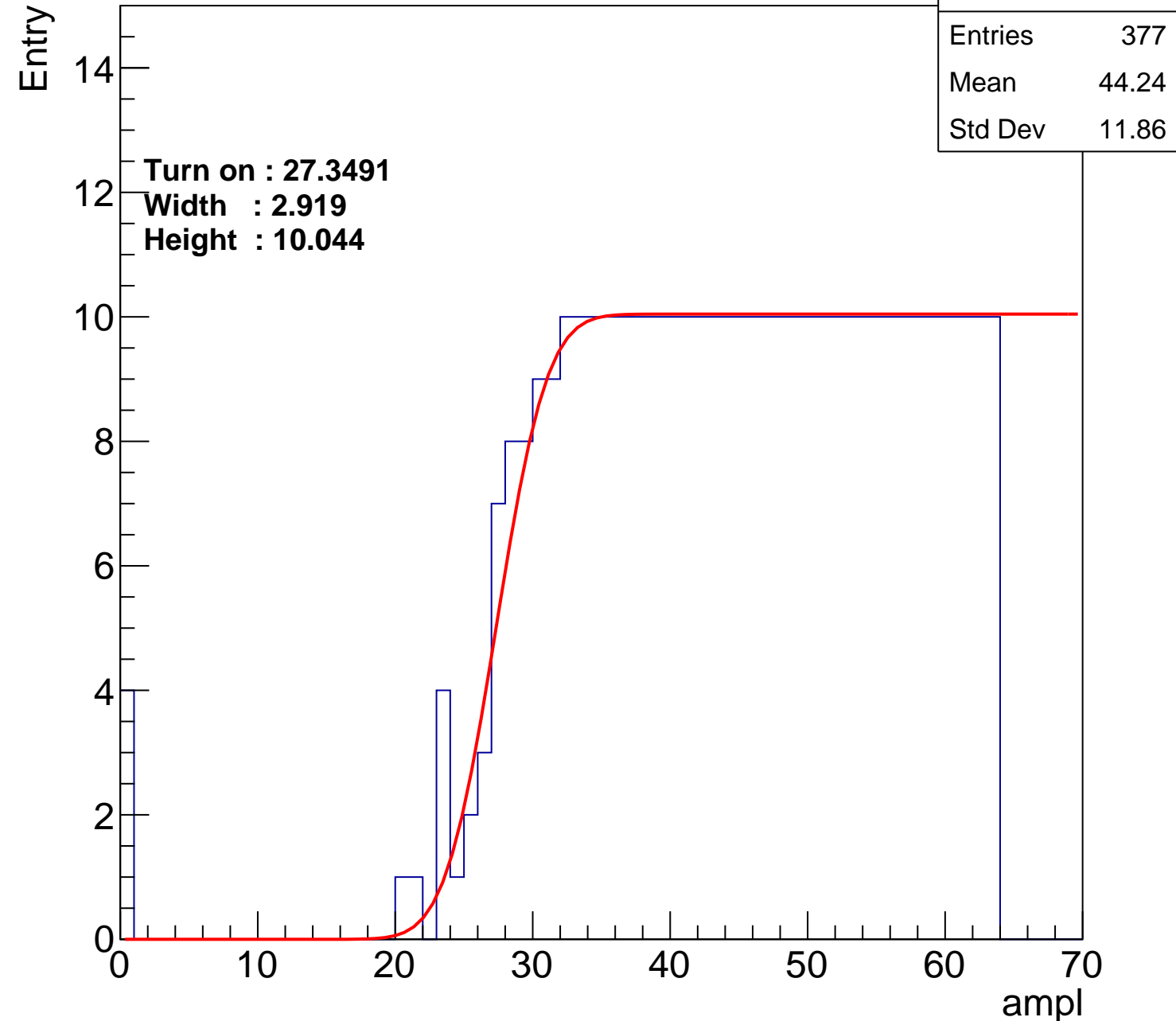
Width : 2.919

Height : 10.044

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch88

calib_packv5_042523_0143.root, FC#7, port C2

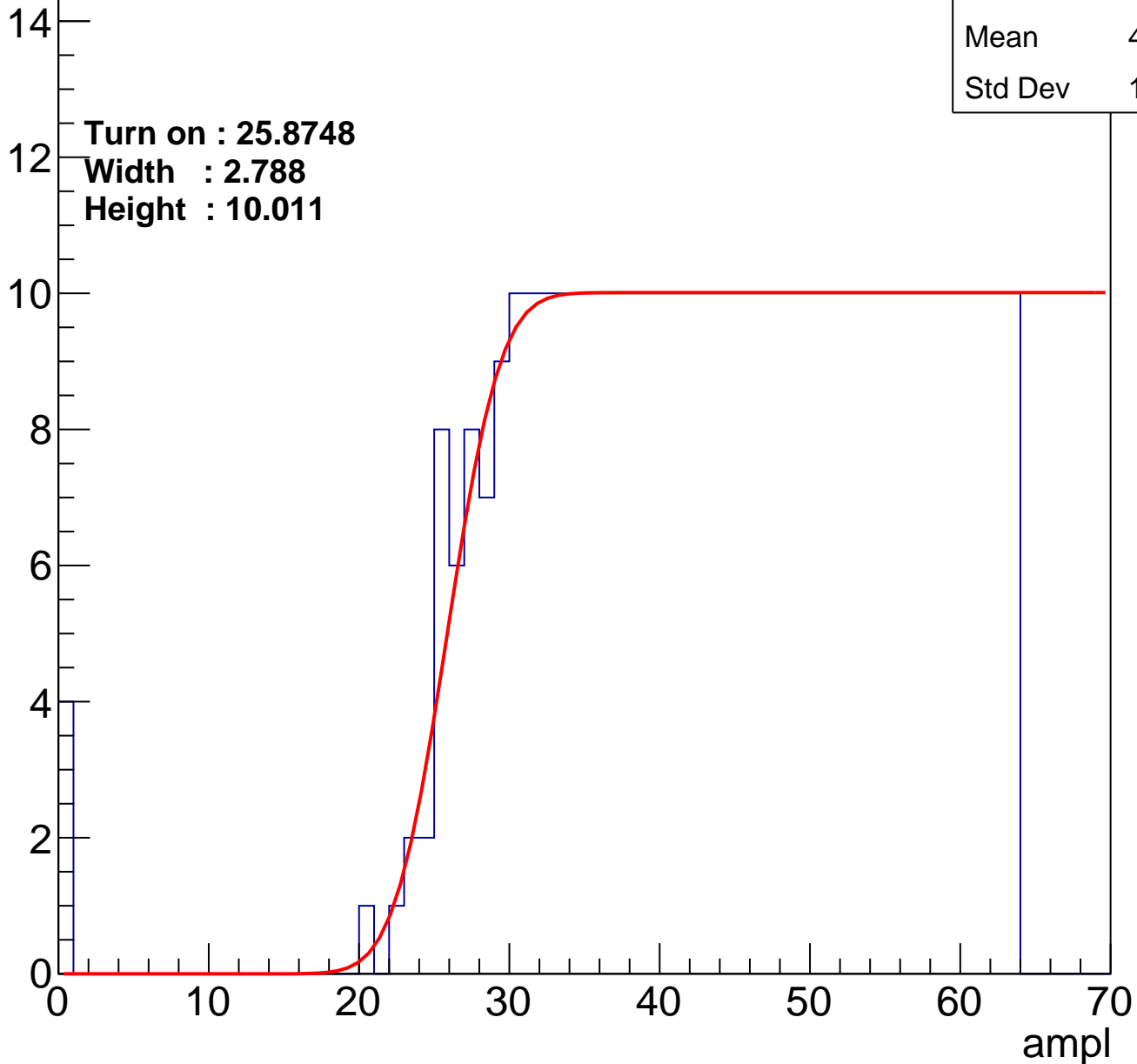
Entries	388
Mean	43.75
Std Dev	12.04

Turn on : 25.8748

Width : 2.788

Height : 10.011

Entry



B1L103S, U2-ch89

calib_packv5_042523_0143.root, FC#7, port C2

Entries	382
Mean	43.95
Std Dev	12.11

Turn on : 26.5590

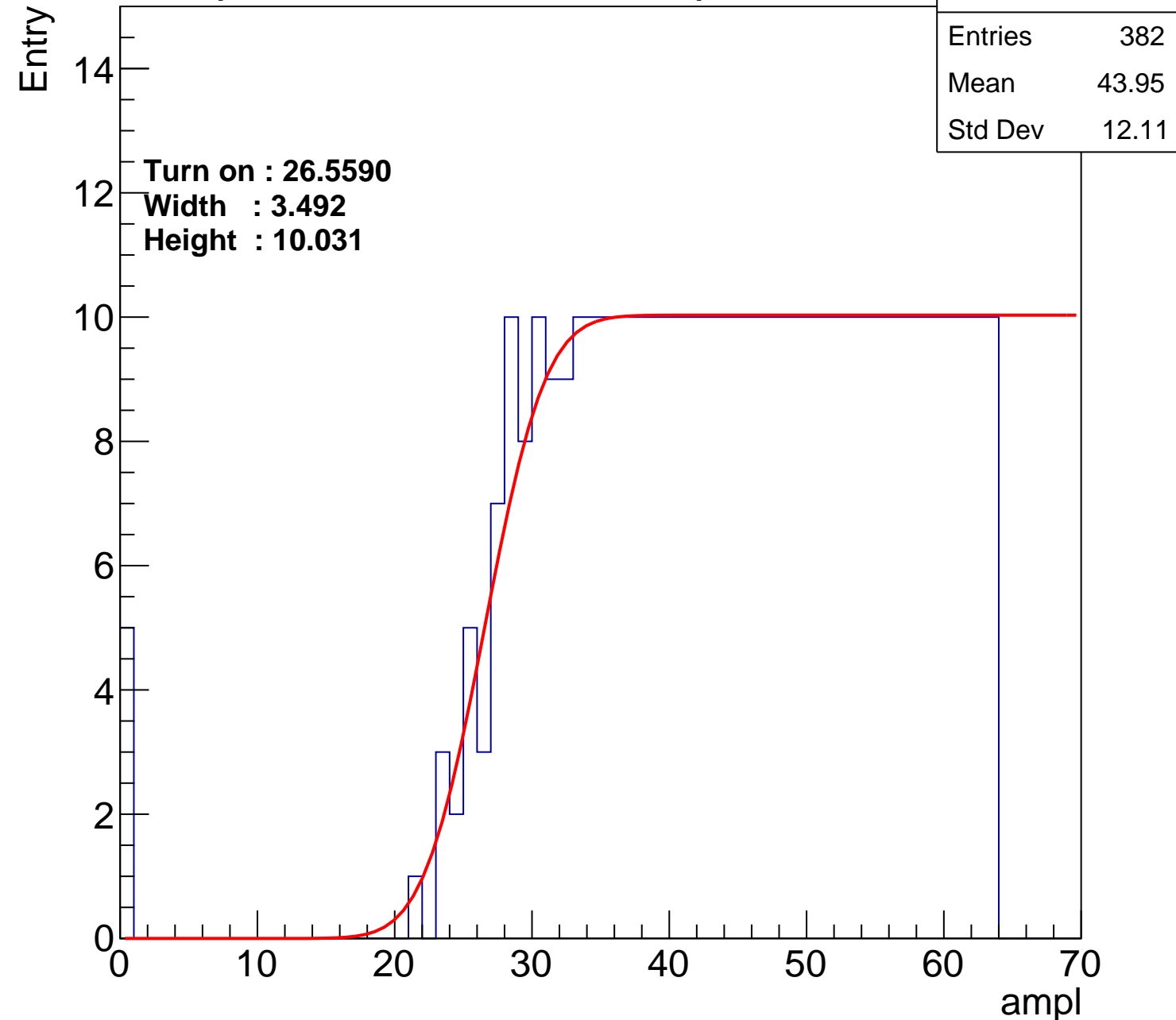
Width : 3.492

Height : 10.031

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch90

calib_packv5_042523_0143.root, FC#7, port C2

Entry

14

12

10

8

6

4

2

0

0

10

20

30

40

50

60

ampl

Turn on : 24.7917

Width : 2.313

Height : 9.973

Entries	395
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Mean	43.44
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Std Dev	12.16
---------	-------

B1L103S, U2-ch91

calib_packv5_042523_0143.root, FC#7, port C2

Entries	378
Mean	44.15
Std Dev	11.94

Turn on : 26.8822

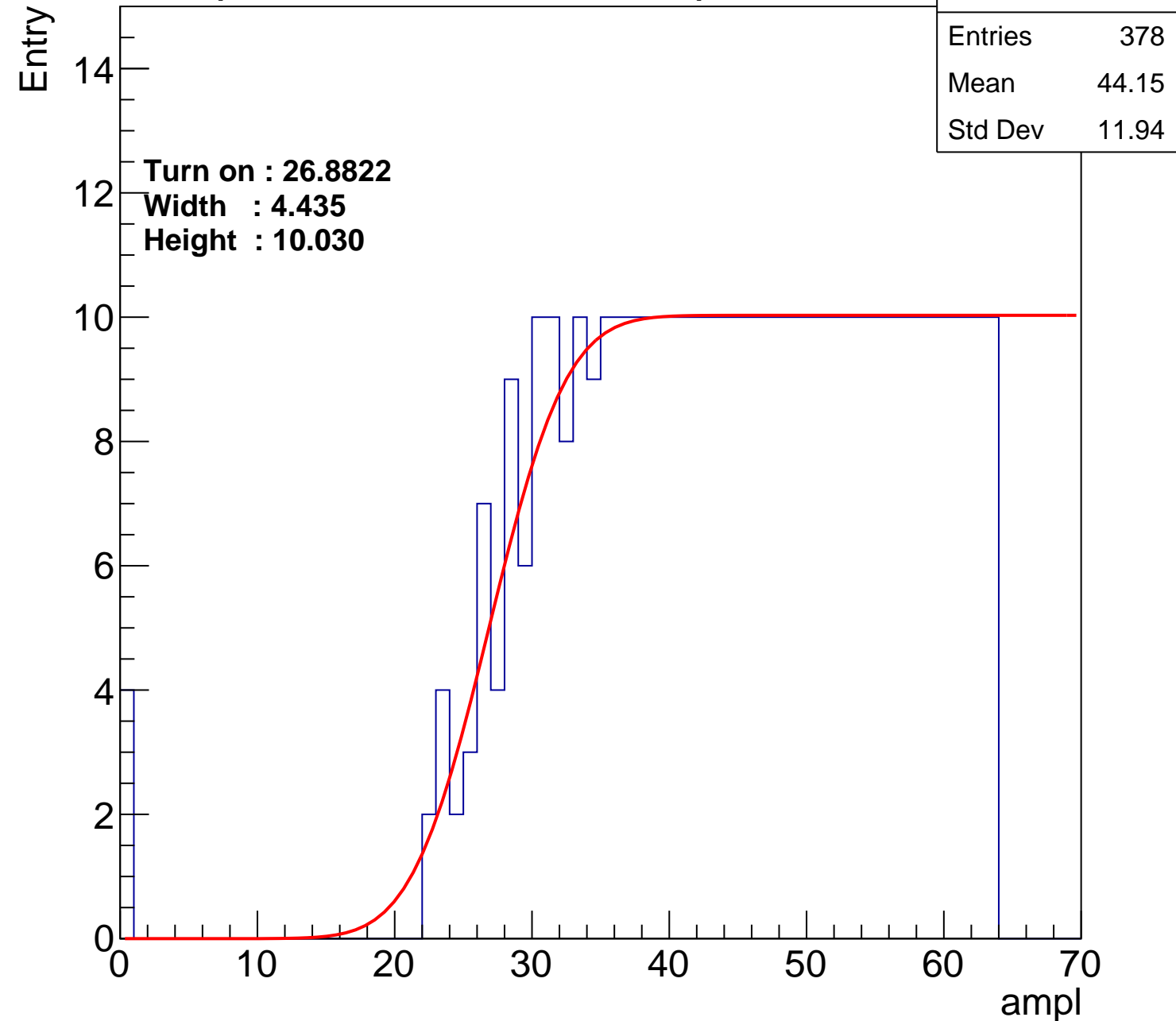
Width : 4.435

Height : 10.030

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch92

calib_packv5_042523_0143.root, FC#7, port C2

Entries	406
Mean	42.91
Std Dev	12.36

Turn on : 24.3308

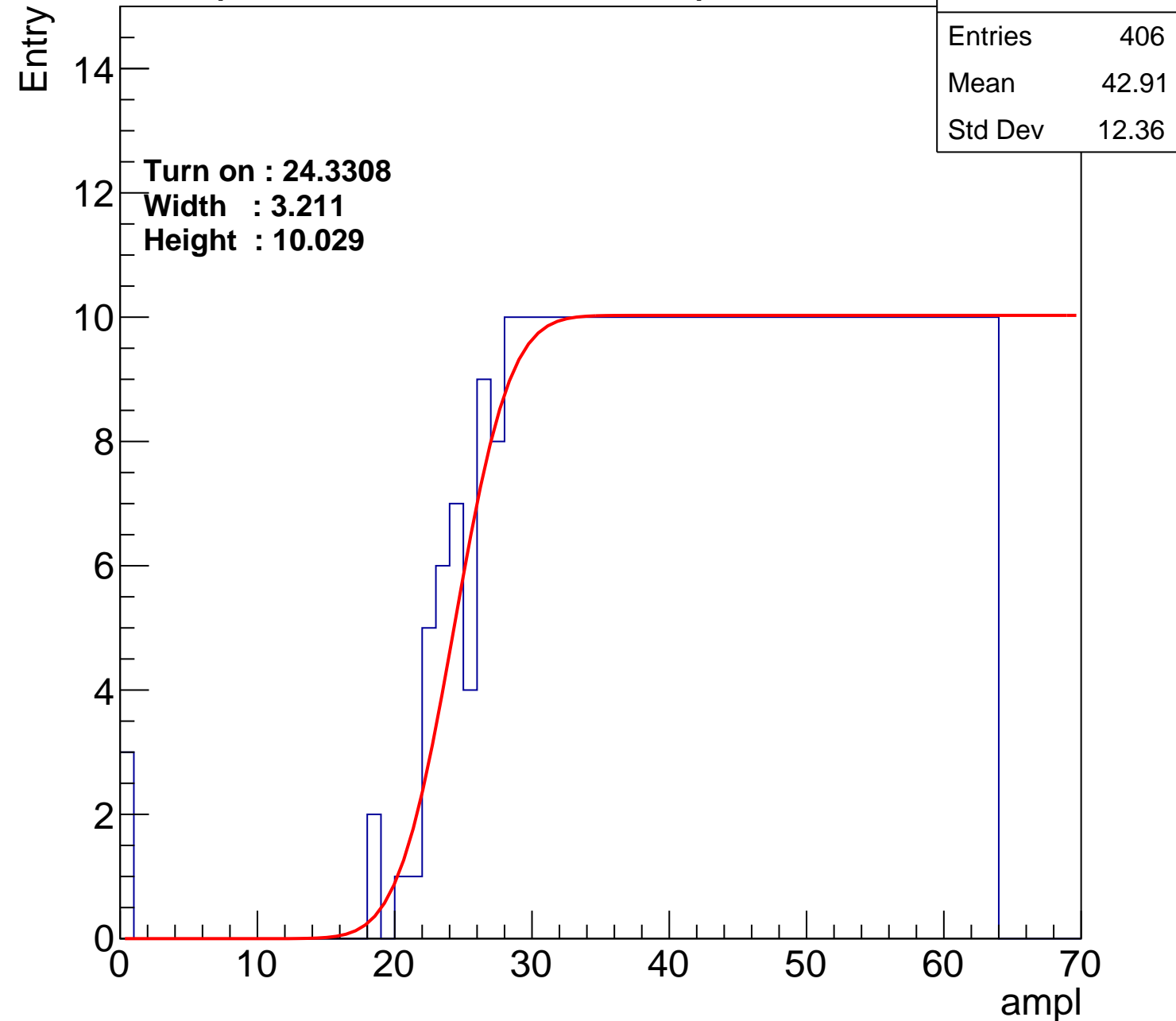
Width : 3.211

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch93

calib_packv5_042523_0143.root, FC#7, port C2

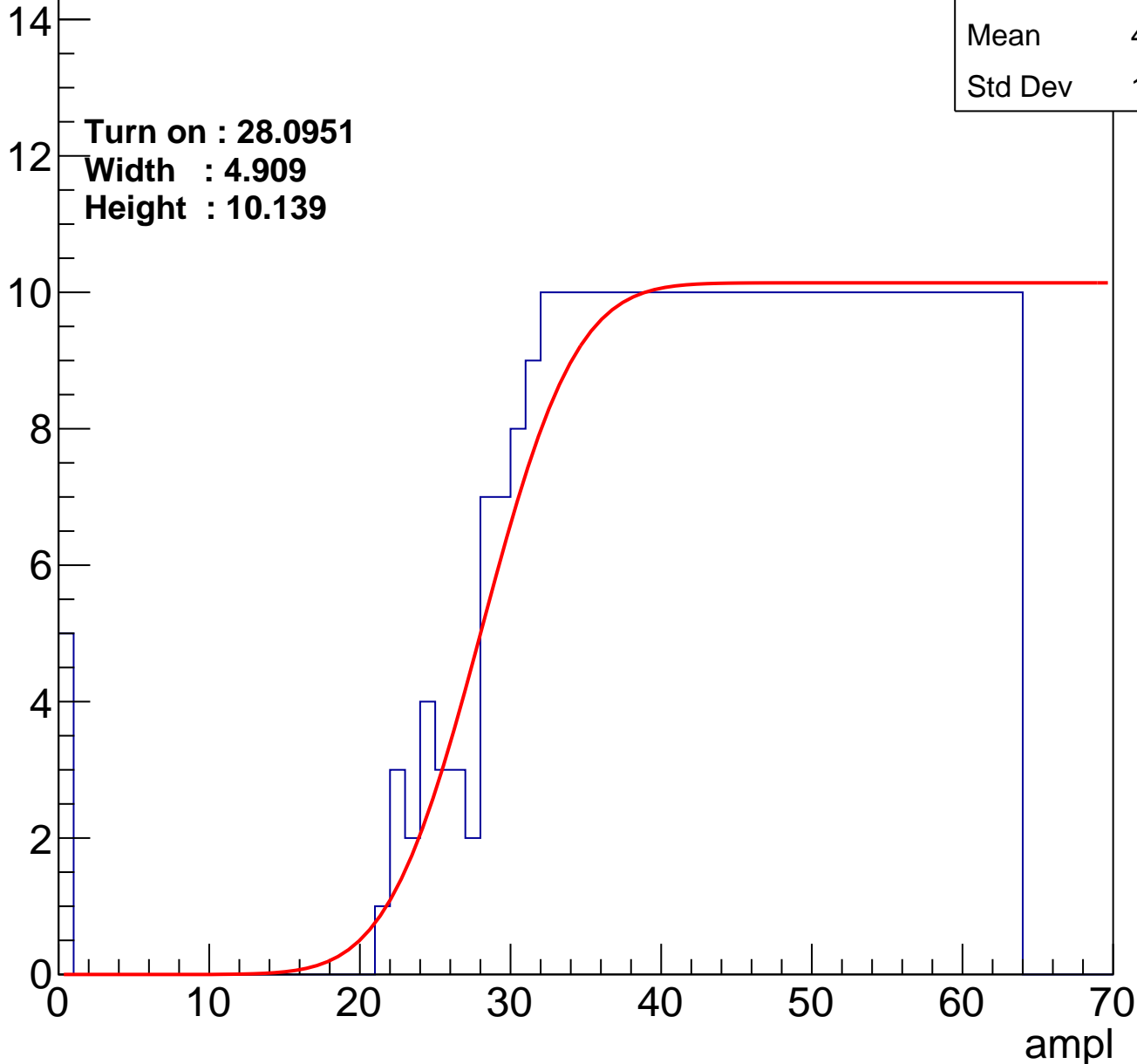
Entries	374
Mean	44.26
Std Dev	12.06

Turn on : 28.0951

Width : 4.909

Height : 10.139

Entry



B1L103S, U2-ch94

calib_packv5_042523_0143.root, FC#7, port C2

Entries	393
Mean	43.55
Std Dev	12.04

Turn on : 25.2748

Width : 4.056

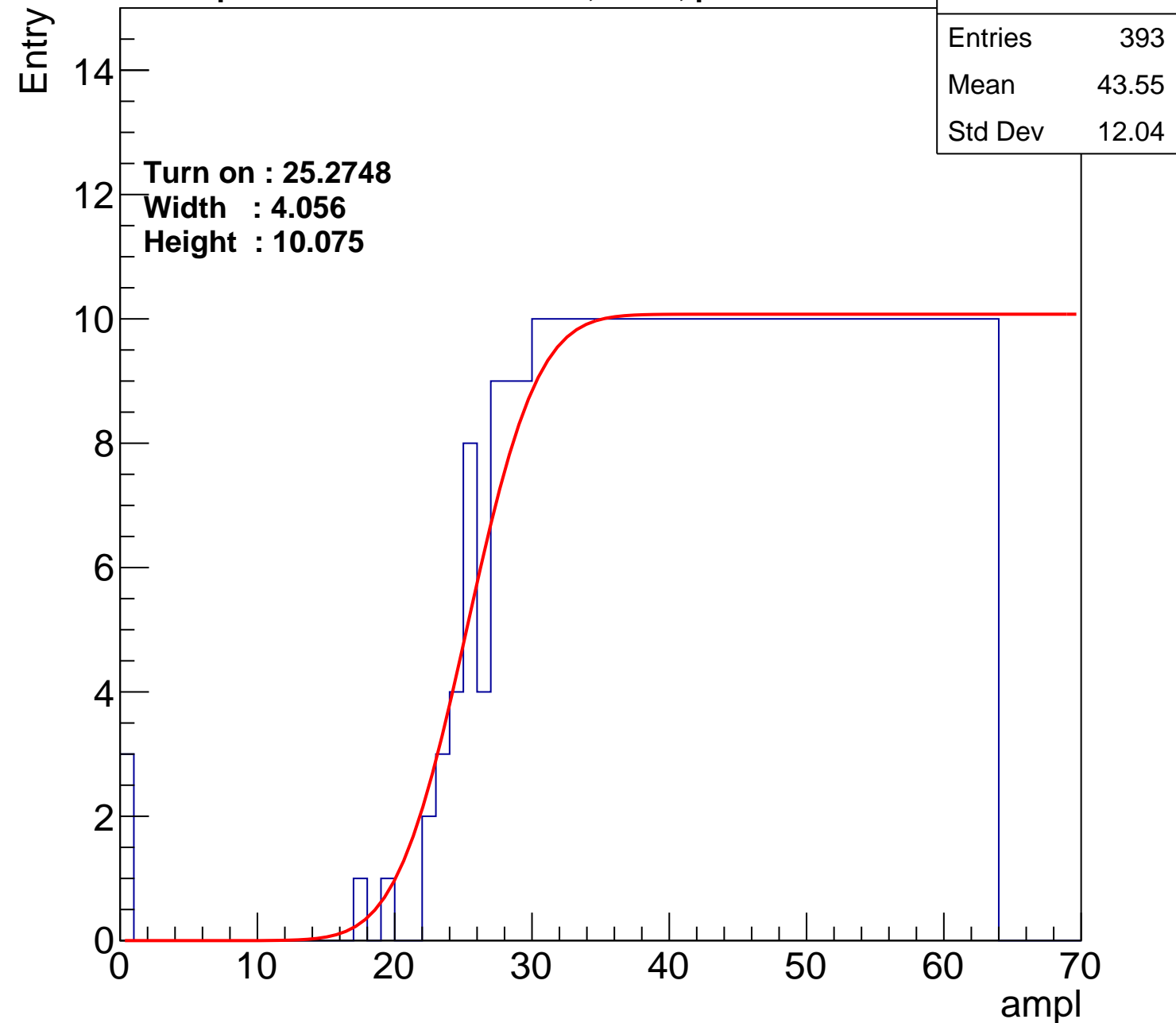
Height : 10.075

Entry

14
12
10
8
6
4
2
0

ampl

0 10 20 30 40 50 60 70



B1L103S, U2-ch95

calib_packv5_042523_0143.root, FC#7, port C2

Entries	380
Mean	44.09
Std Dev	11.92

Turn on : 26.2428

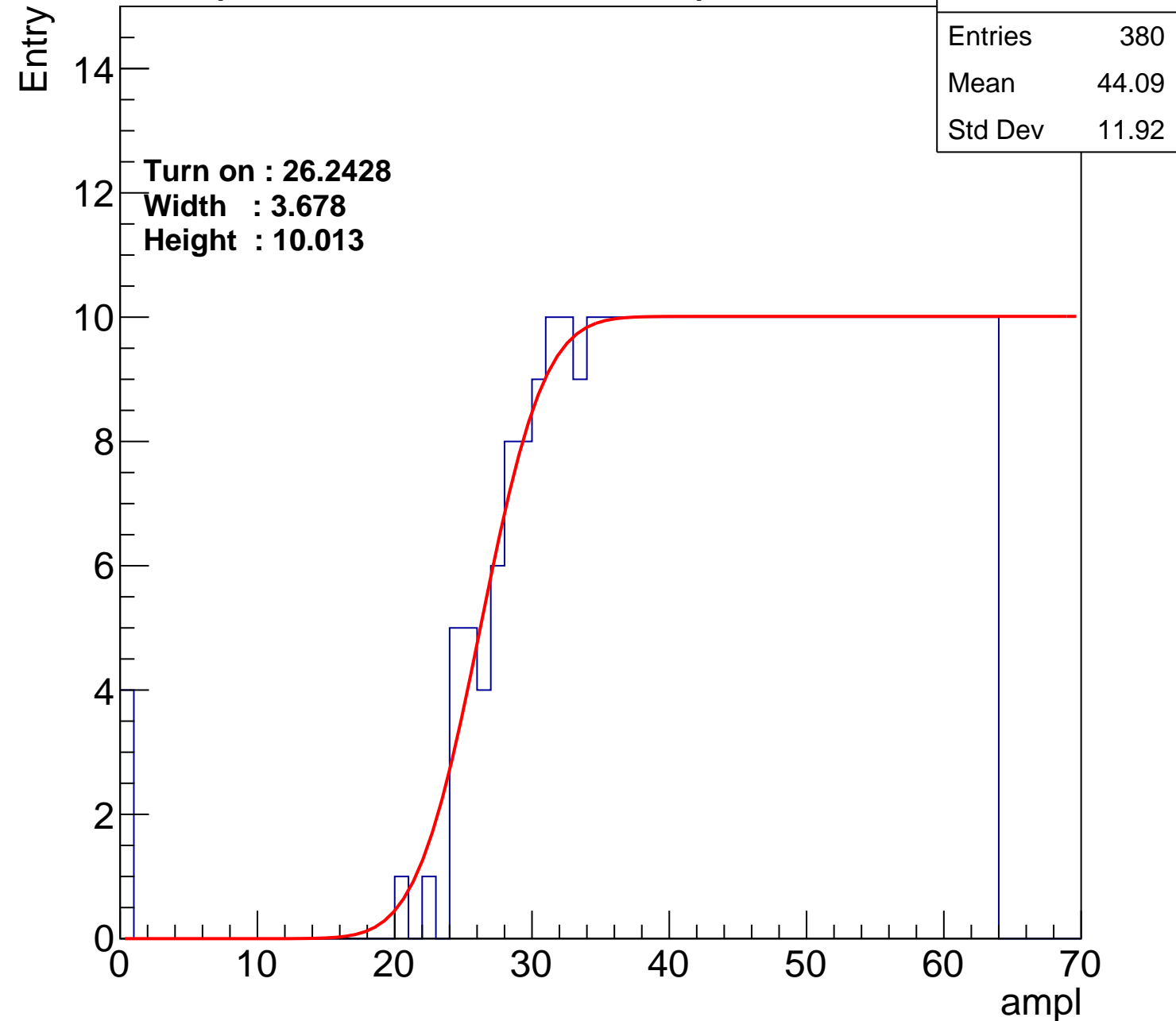
Width : 3.678

Height : 10.013

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch96

calib_packv5_042523_0143.root, FC#7, port C2

Entries	397
Mean	43.28
Std Dev	12.3

Turn on : 25.3628

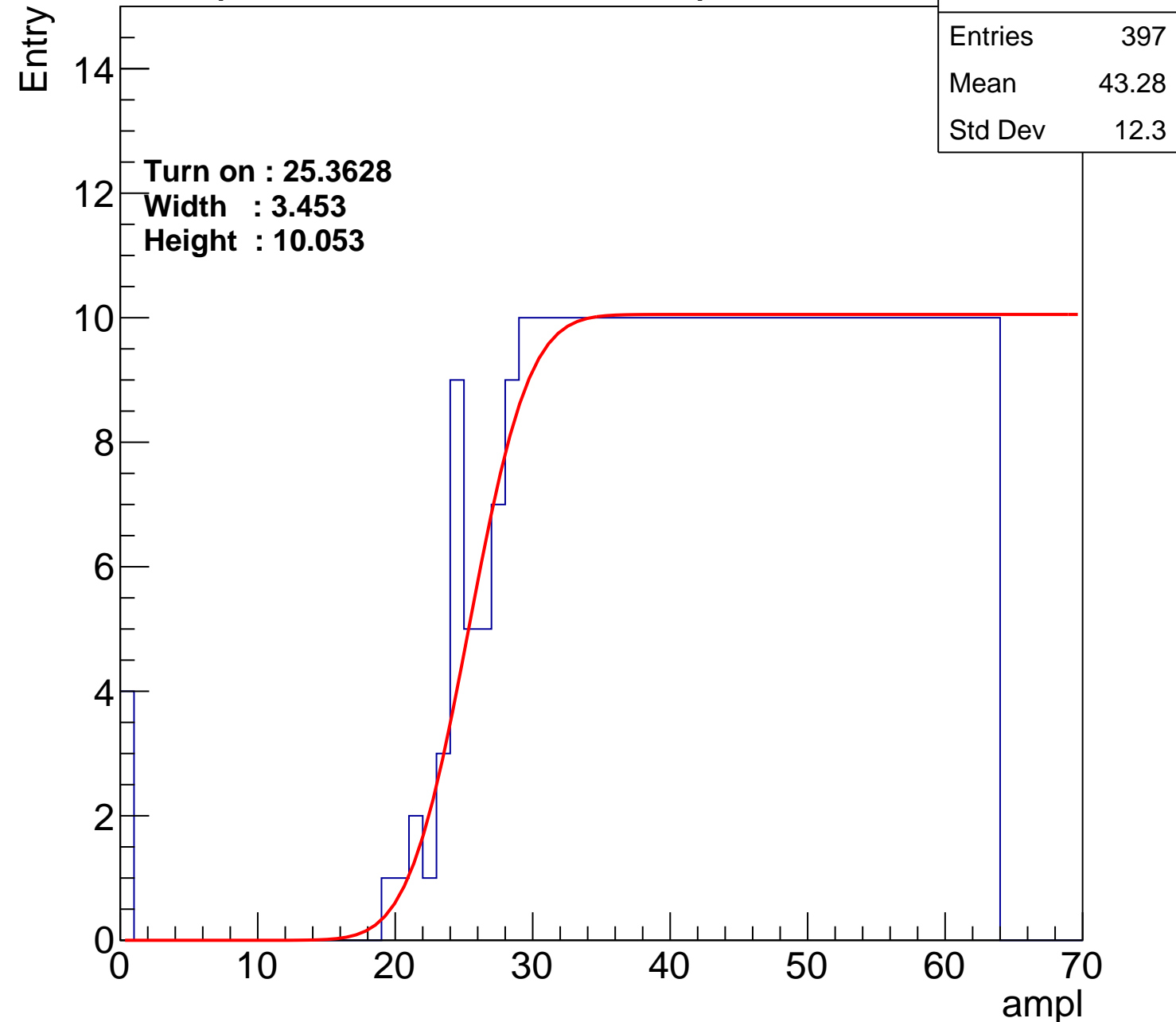
Width : 3.453

Height : 10.053

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch97

calib_packv5_042523_0143.root, FC#7, port C2

Entries	396
Mean	43.47
Std Dev	11.94

Turn on : 24.9773

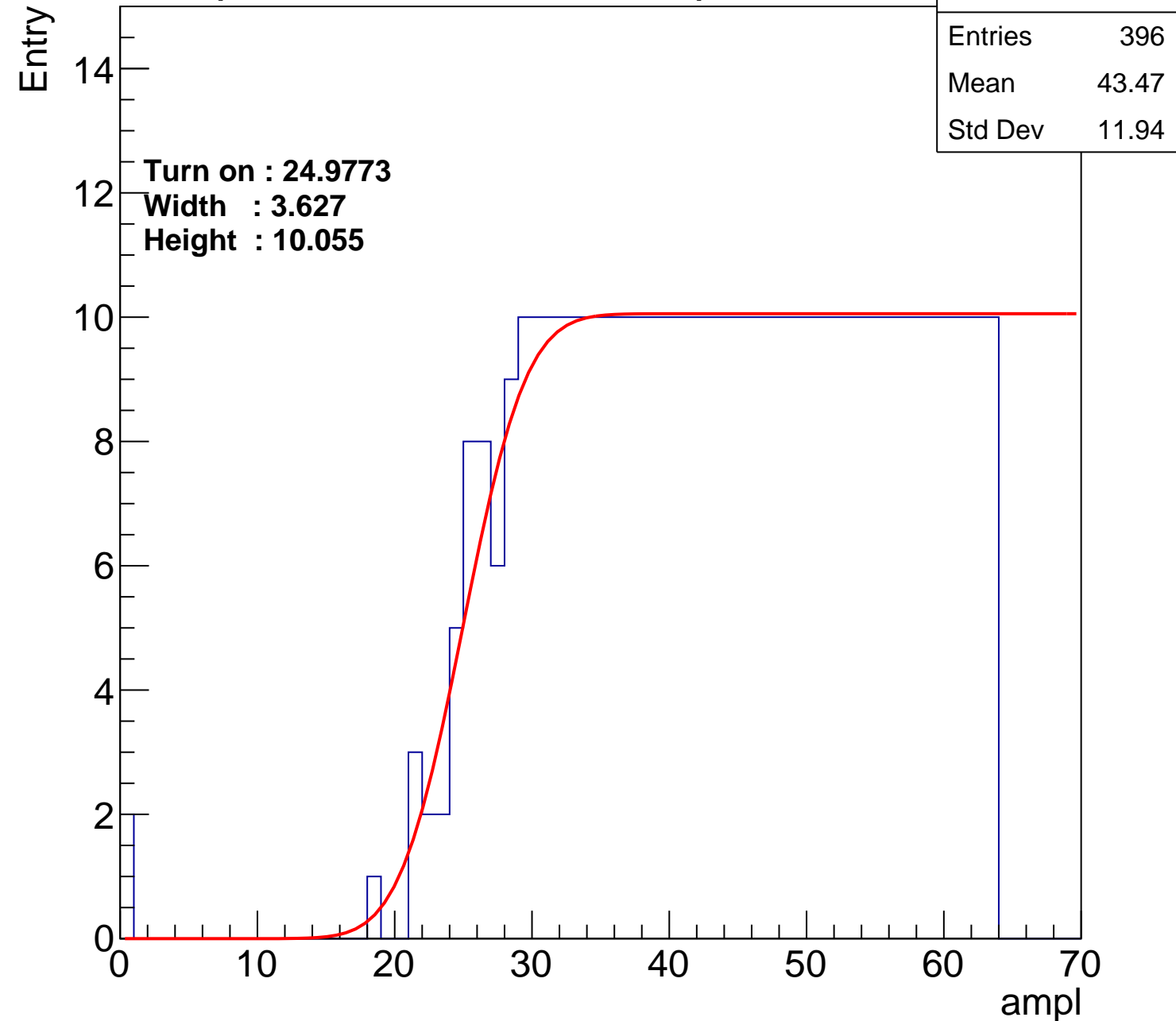
Width : 3.627

Height : 10.055

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch98

calib_packv5_042523_0143.root, FC#7, port C2

Entries	391
Mean	43.53
Std Dev	12.23

Turn on : 25.8951

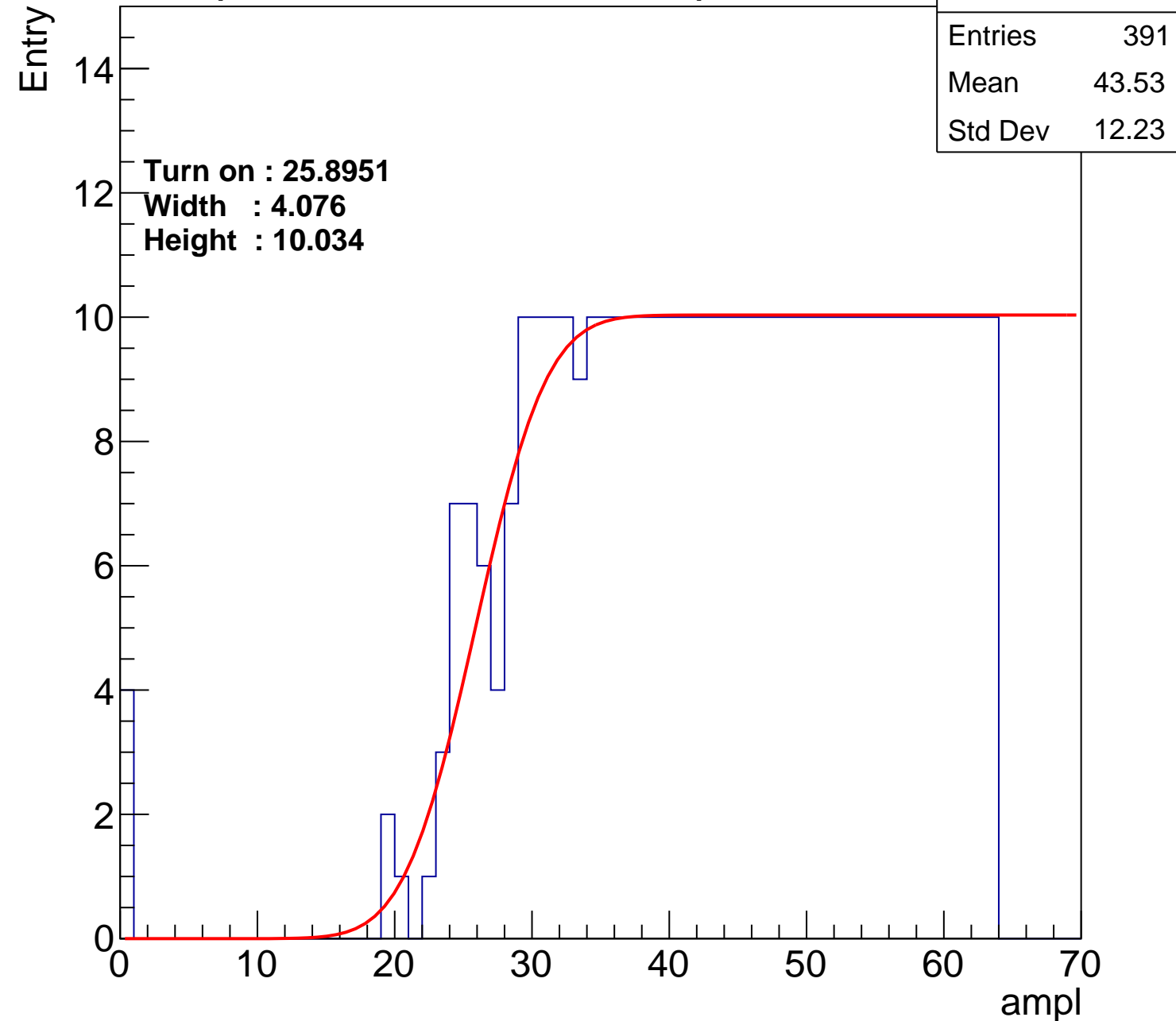
Width : 4.076

Height : 10.034

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch99

calib_packv5_042523_0143.root, FC#7, port C2

Entries	407
Mean	42.74
Std Dev	12.62

Turn on : 23.2613

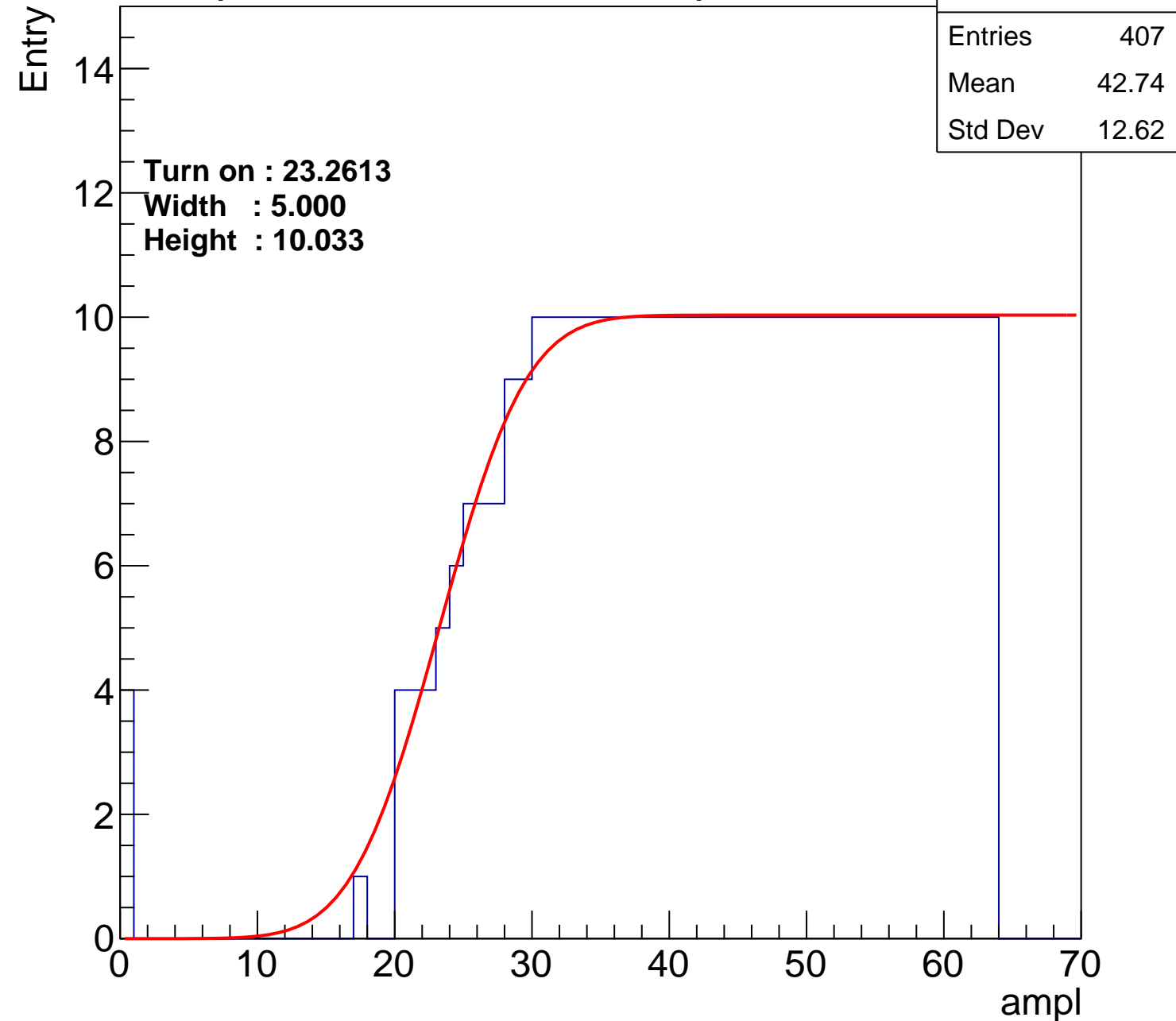
Width : 5.000

Height : 10.033

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch100

calib_packv5_042523_0143.root, FC#7, port C2

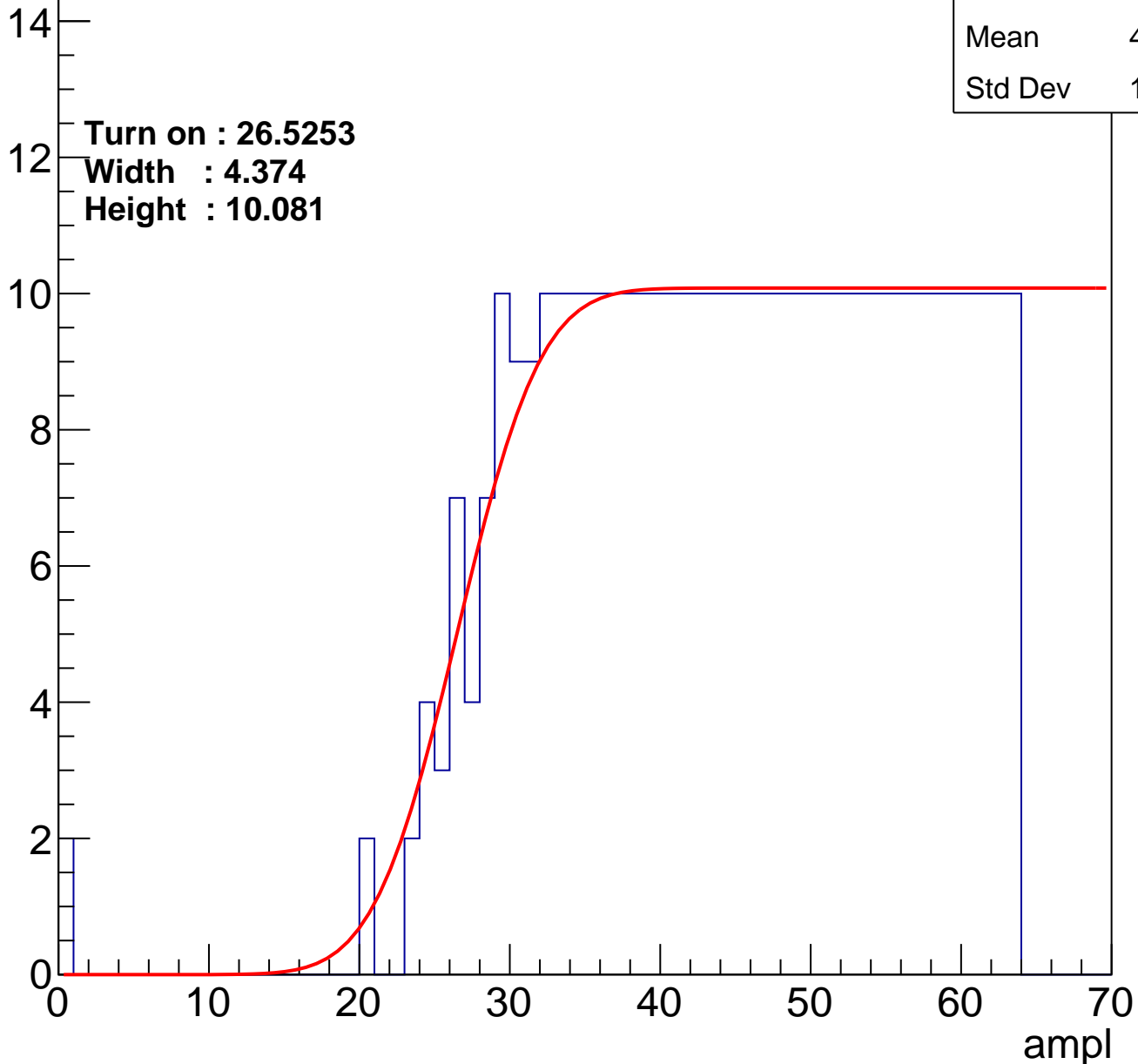
Entries	379
Mean	44.28
Std Dev	11.54

Turn on : 26.5253

Width : 4.374

Height : 10.081

Entry



B1L103S, U2-ch101

calib_packv5_042523_0143.root, FC#7, port C2

Entries	376
Mean	44.35
Std Dev	11.75

Turn on : 27.5034

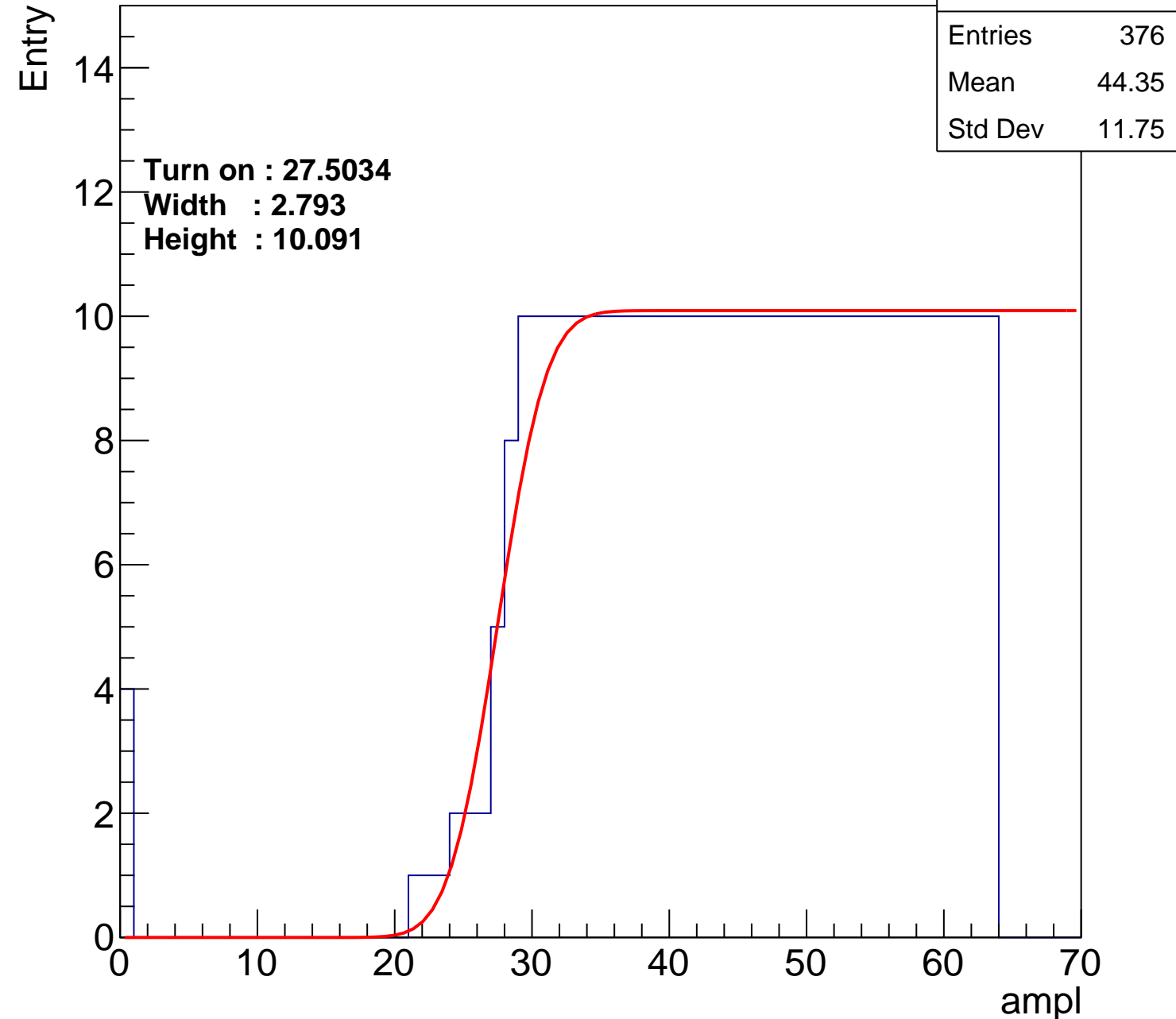
Width : 2.793

Height : 10.091

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch102

calib_packv5_042523_0143.root, FC#7, port C2

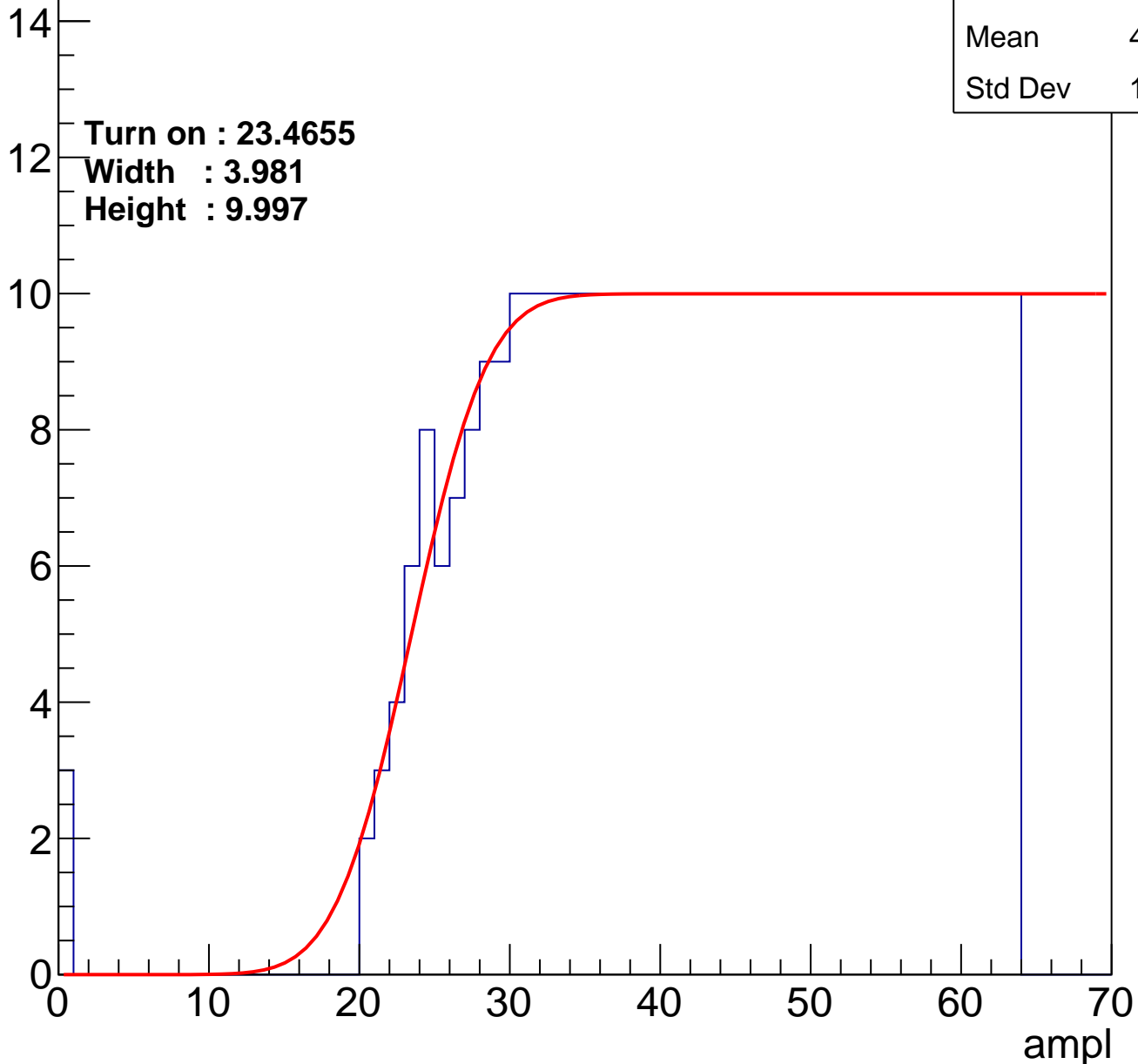
Entries	405
Mean	42.94
Std Dev	12.35

Turn on : 23.4655

Width : 3.981

Height : 9.997

Entry



B1L103S, U2-ch103

calib_packv5_042523_0143.root, FC#7, port C2

Entries	380
Mean	44.19
Std Dev	11.7

Turn on : 26.5285

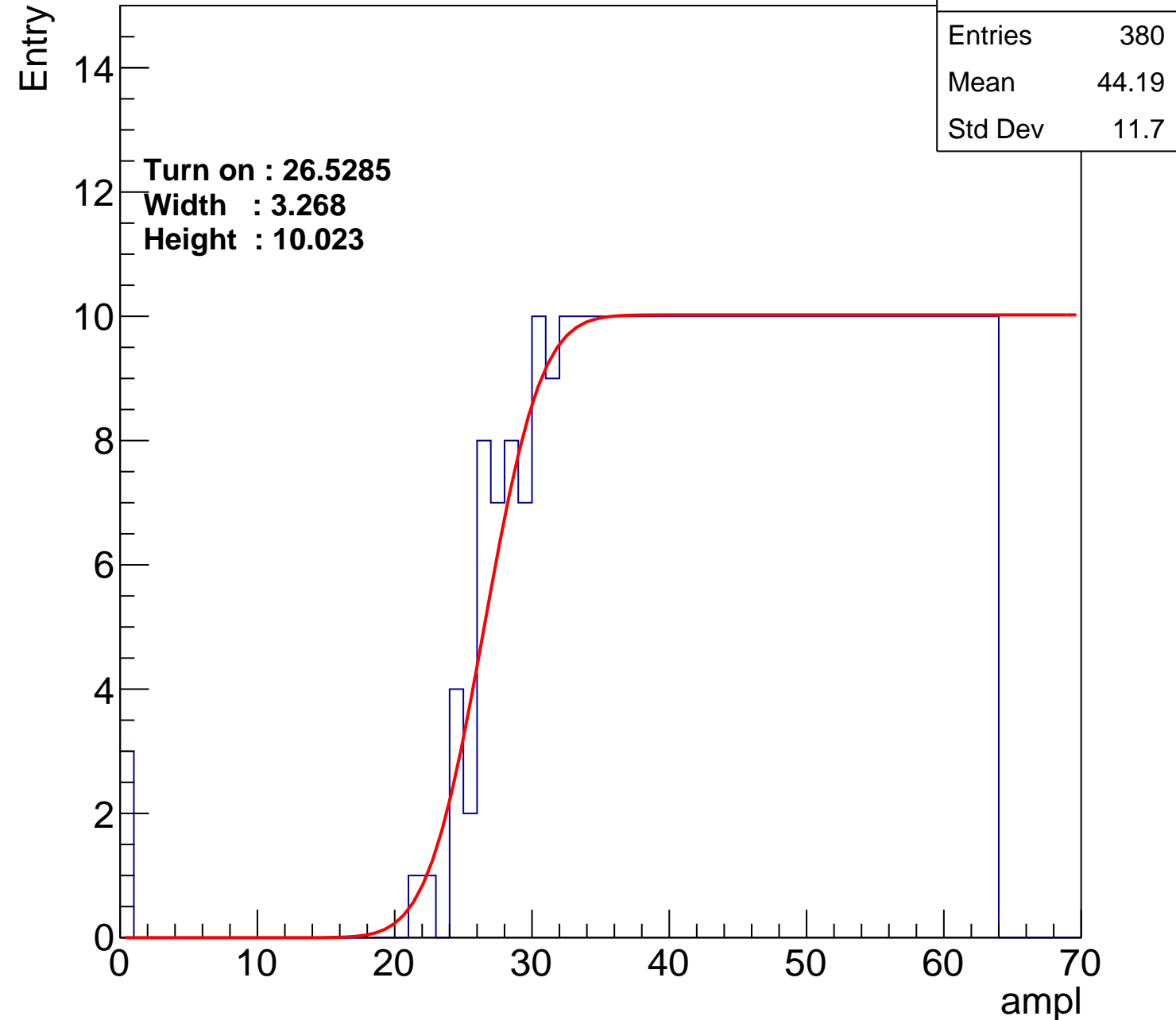
Width : 3.268

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch104

calib_packv5_042523_0143.root, FC#7, port C2

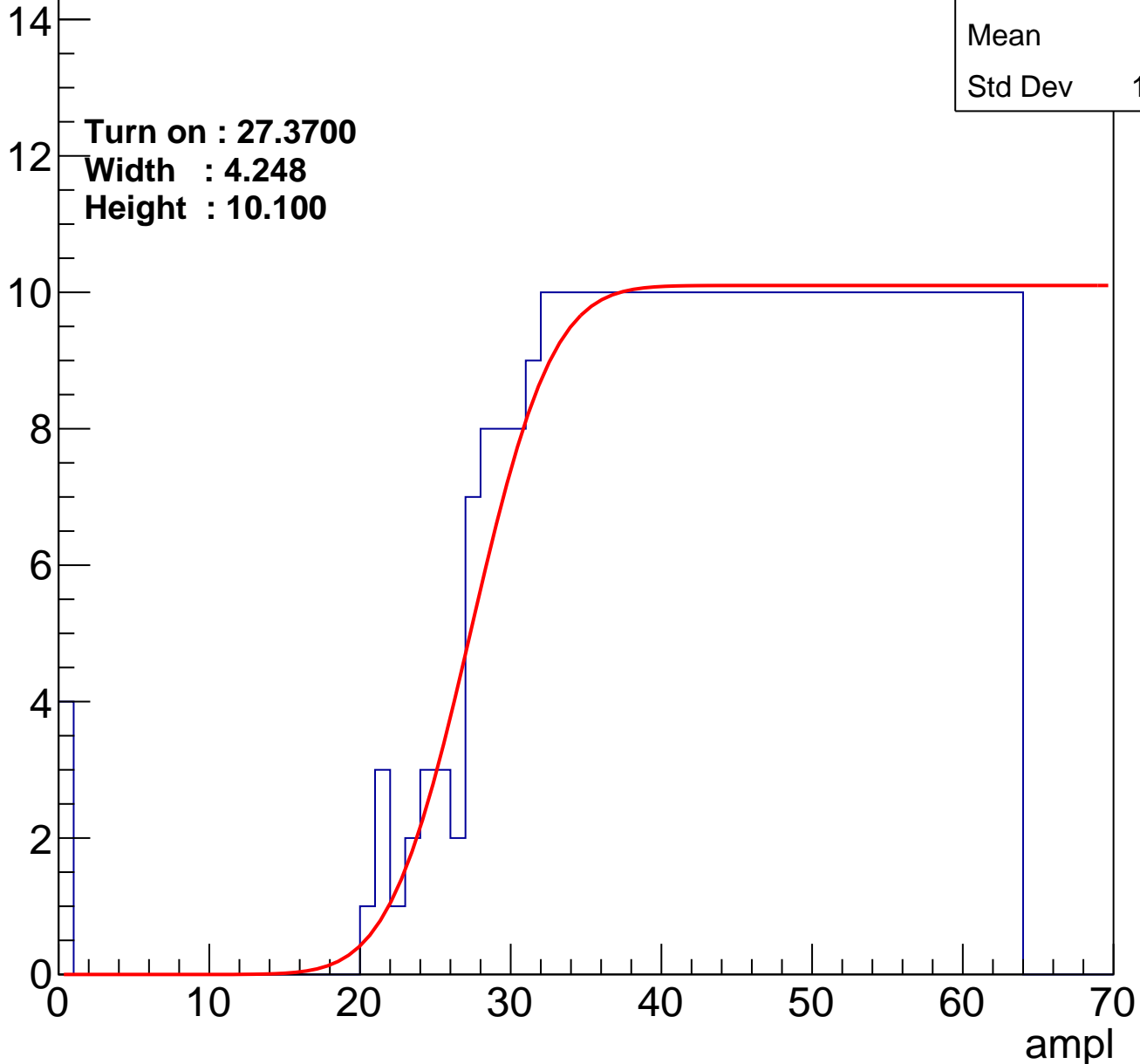
Entries	379
Mean	44.1
Std Dev	11.98

Turn on : 27.3700

Width : 4.248

Height : 10.100

Entry



B1L103S, U2-ch105

calib_packv5_042523_0143.root, FC#7, port C2

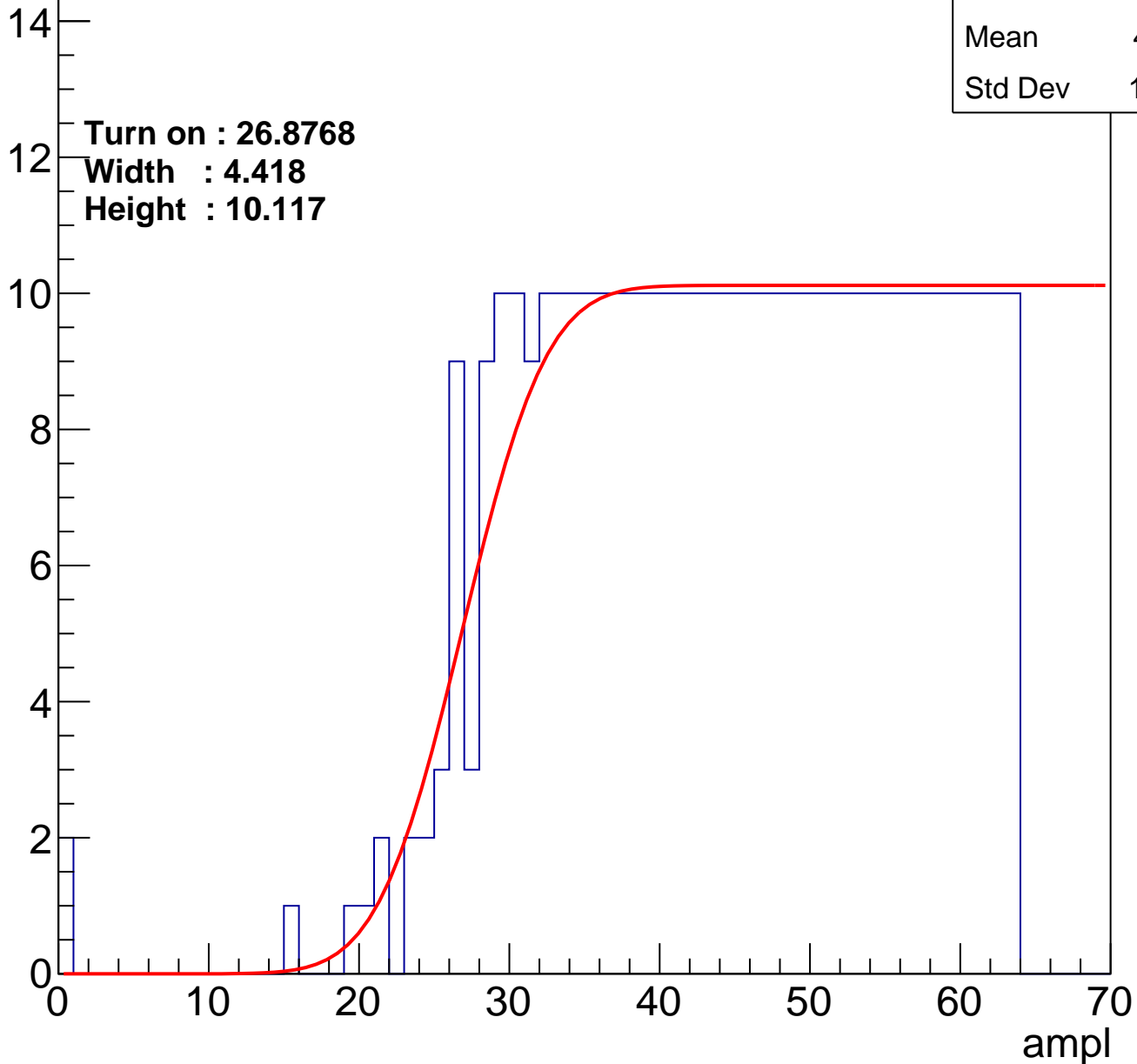
Entries	384
Mean	44.01
Std Dev	11.72

Turn on : 26.8768

Width : 4.418

Height : 10.117

Entry



B1L103S, U2-ch106

calib_packv5_042523_0143.root, FC#7, port C2

Entries	384
Mean	43.93
Std Dev	11.97

Turn on : 26.3734

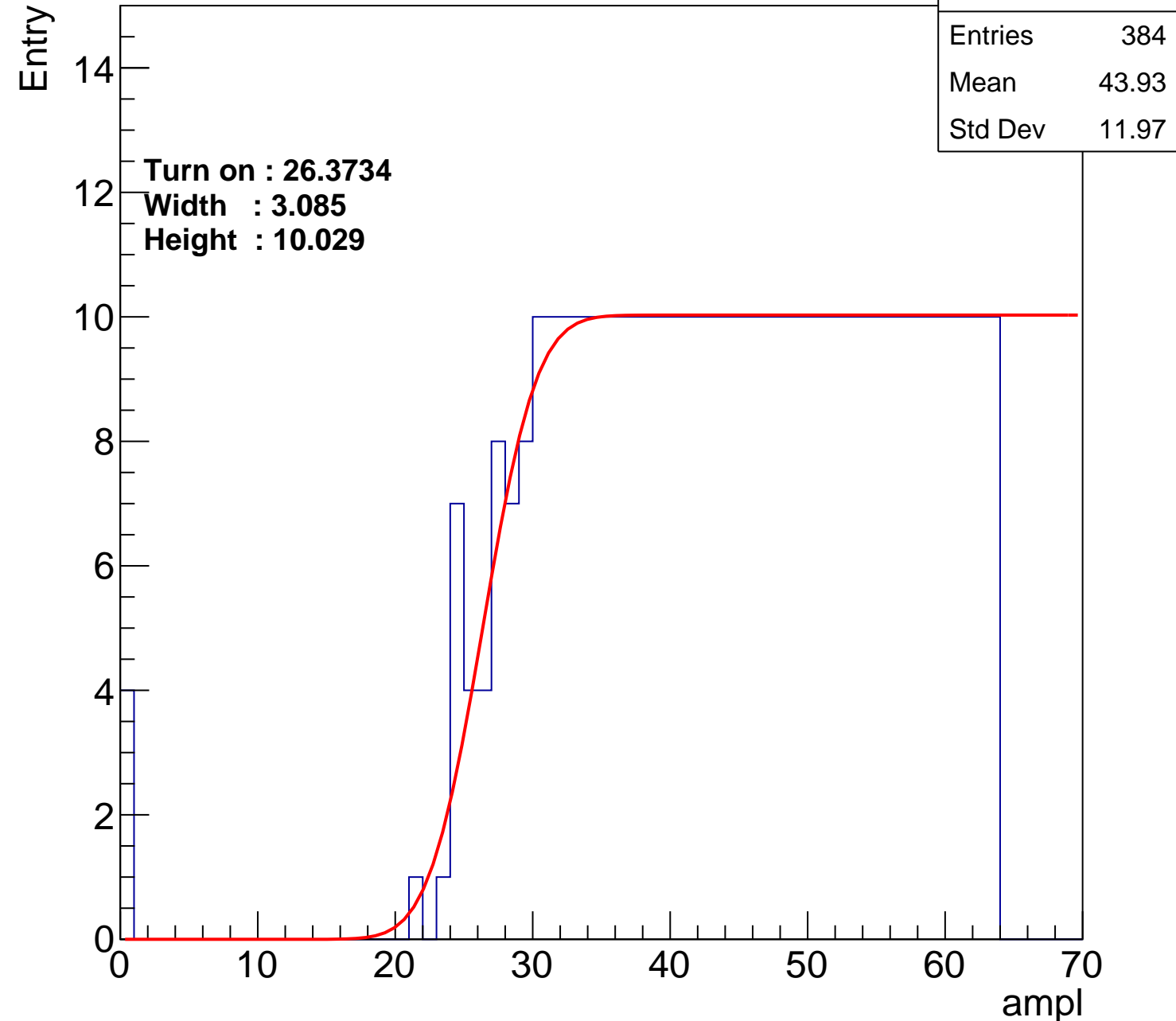
Width : 3.085

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch107

calib_packv5_042523_0143.root, FC#7, port C2

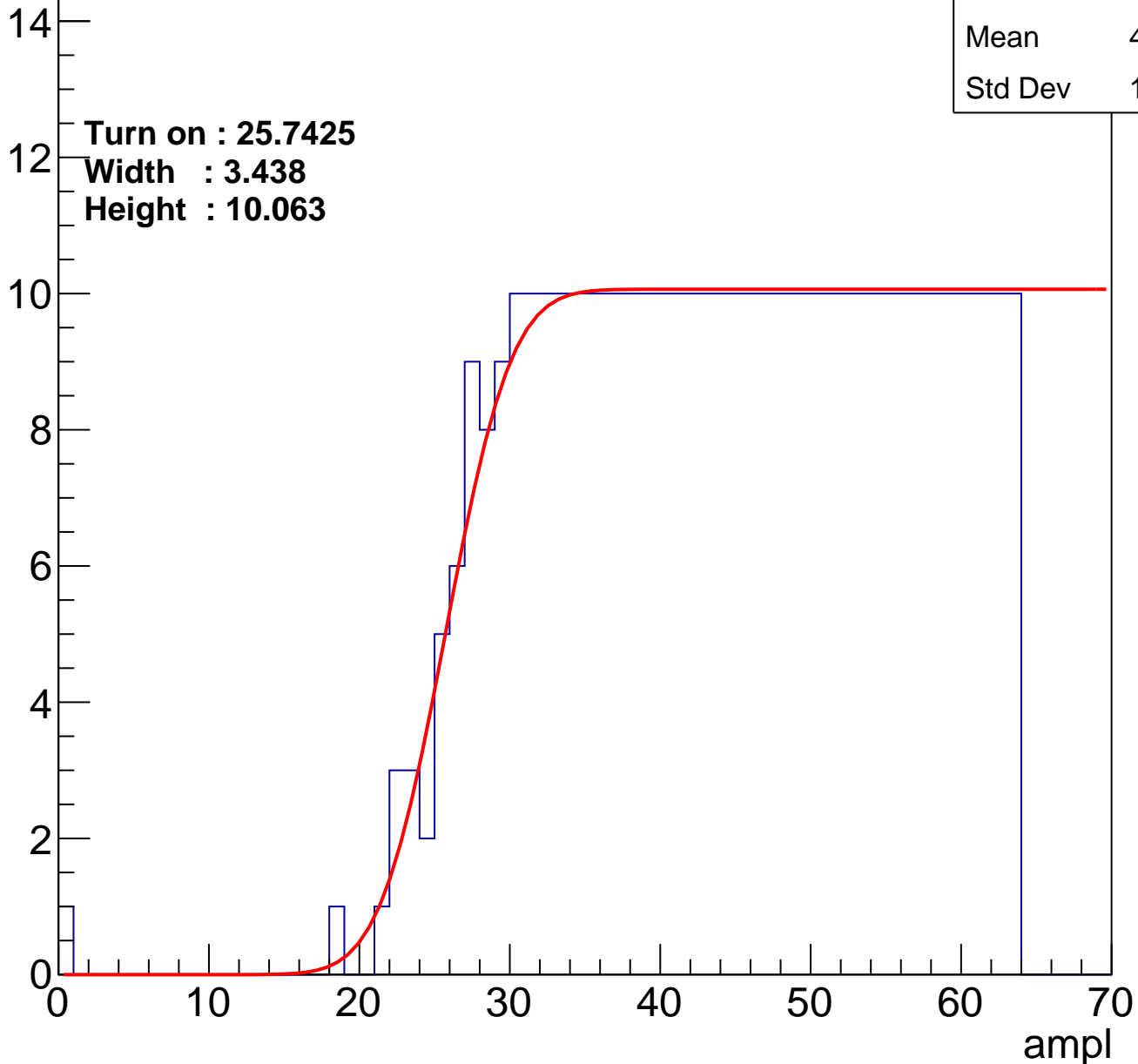
Entries	388
Mean	43.92
Std Dev	11.58

Turn on : 25.7425

Width : 3.438

Height : 10.063

Entry



B1L103S, U2-ch108

calib_packv5_042523_0143.root, FC#7, port C2

Entries	356
Mean	44.99
Std Dev	12.06

Turn on : 29.7350

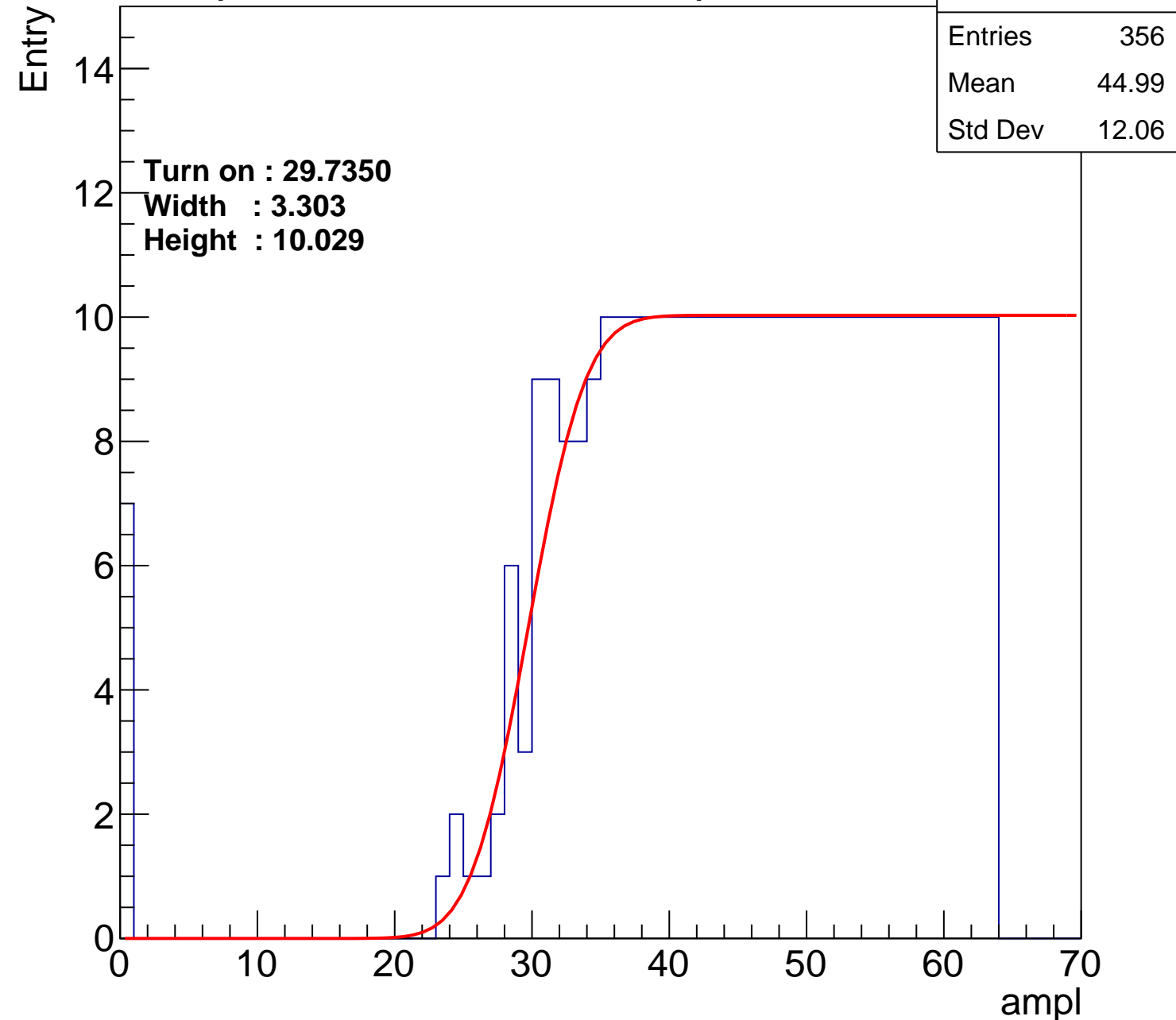
Width : 3.303

Height : 10.029

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch109

calib_packv5_042523_0143.root, FC#7, port C2

Entries	384
Mean	44.09
Std Dev	11.51

Turn on : 25.9676

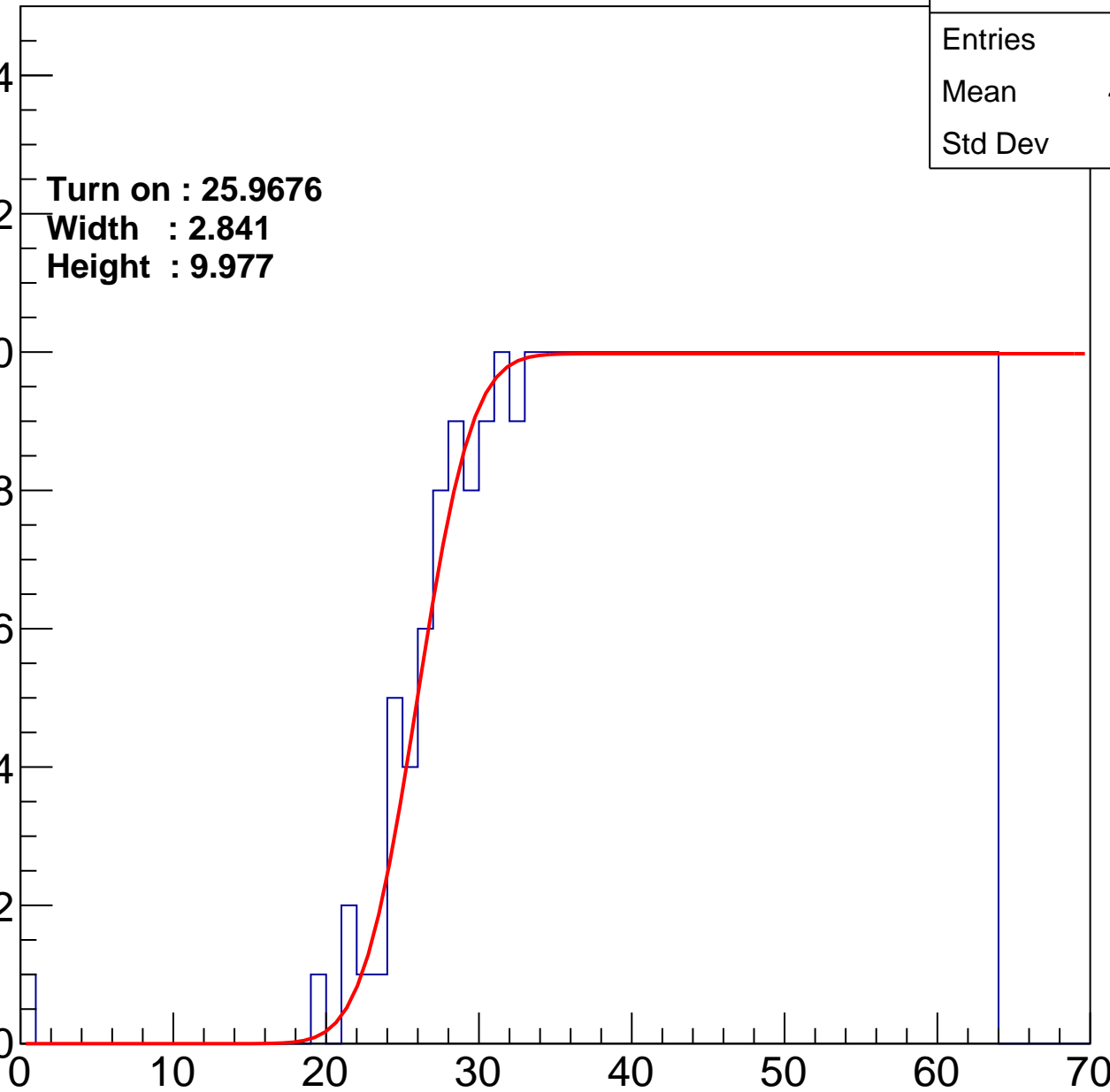
Width : 2.841

Height : 9.977

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch110

calib_packv5_042523_0143.root, FC#7, port C2

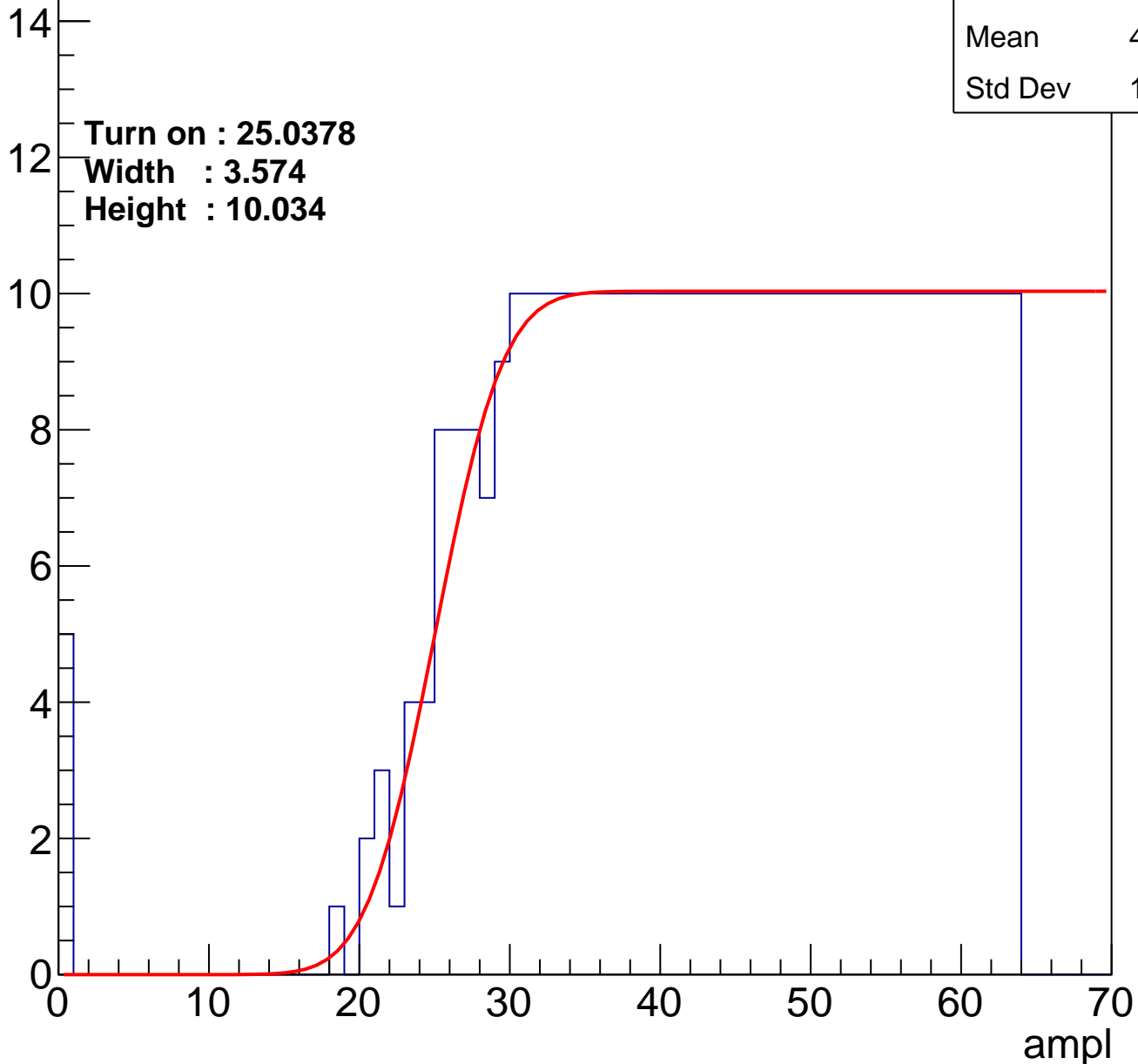
Entries	400
Mean	43.05
Std Dev	12.55

Turn on : 25.0378

Width : 3.574

Height : 10.034

Entry



B1L103S, U2-ch111

calib_packv5_042523_0143.root, FC#7, port C2

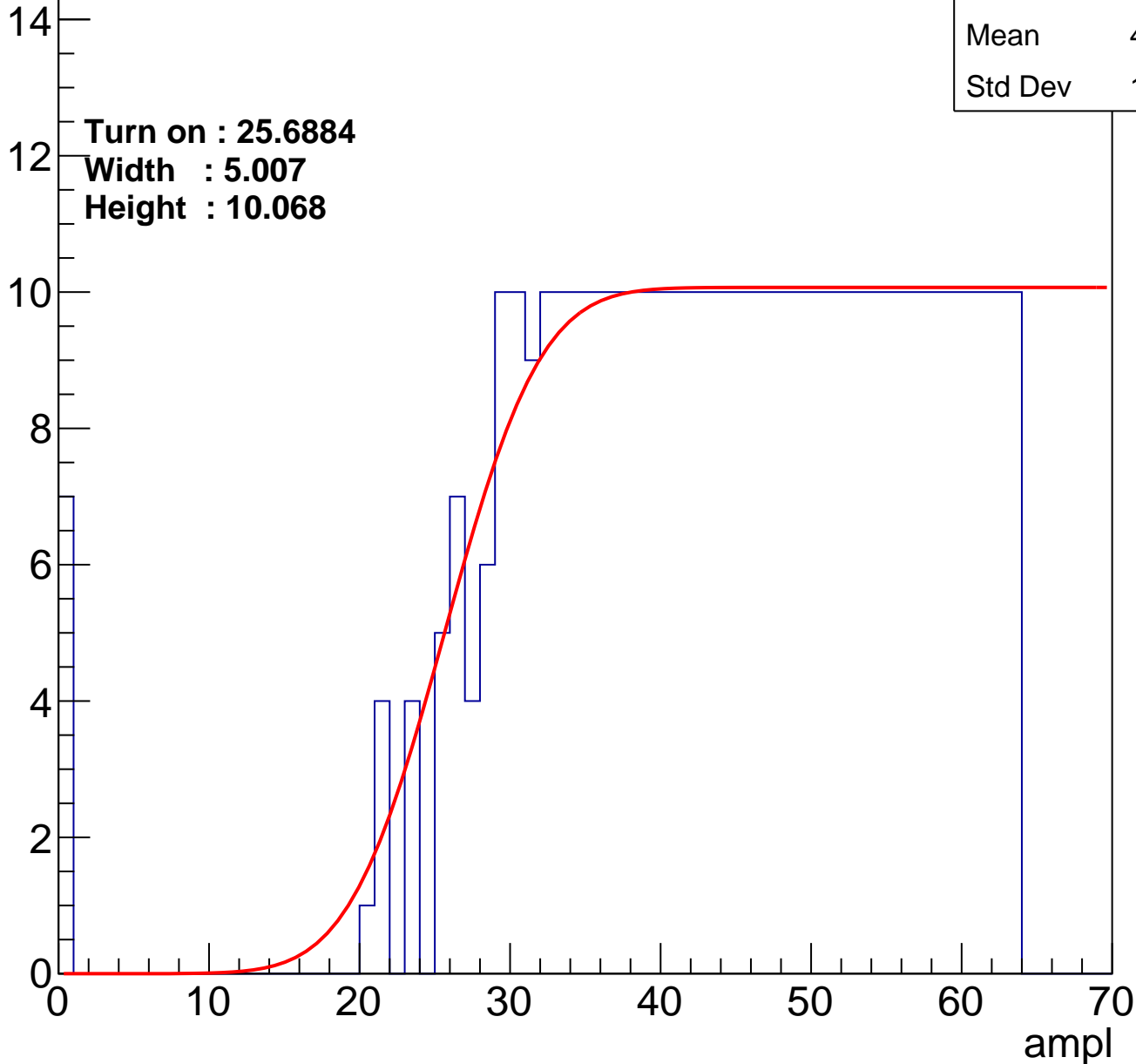
Entries	387
Mean	43.53
Std Dev	12.62

Turn on : 25.6884

Width : 5.007

Height : 10.068

Entry



B1L103S, U2-ch112

calib_packv5_042523_0143.root, FC#7, port C2

Entries	400
Mean	43.07
Std Dev	12.37

Turn on : 25.3549

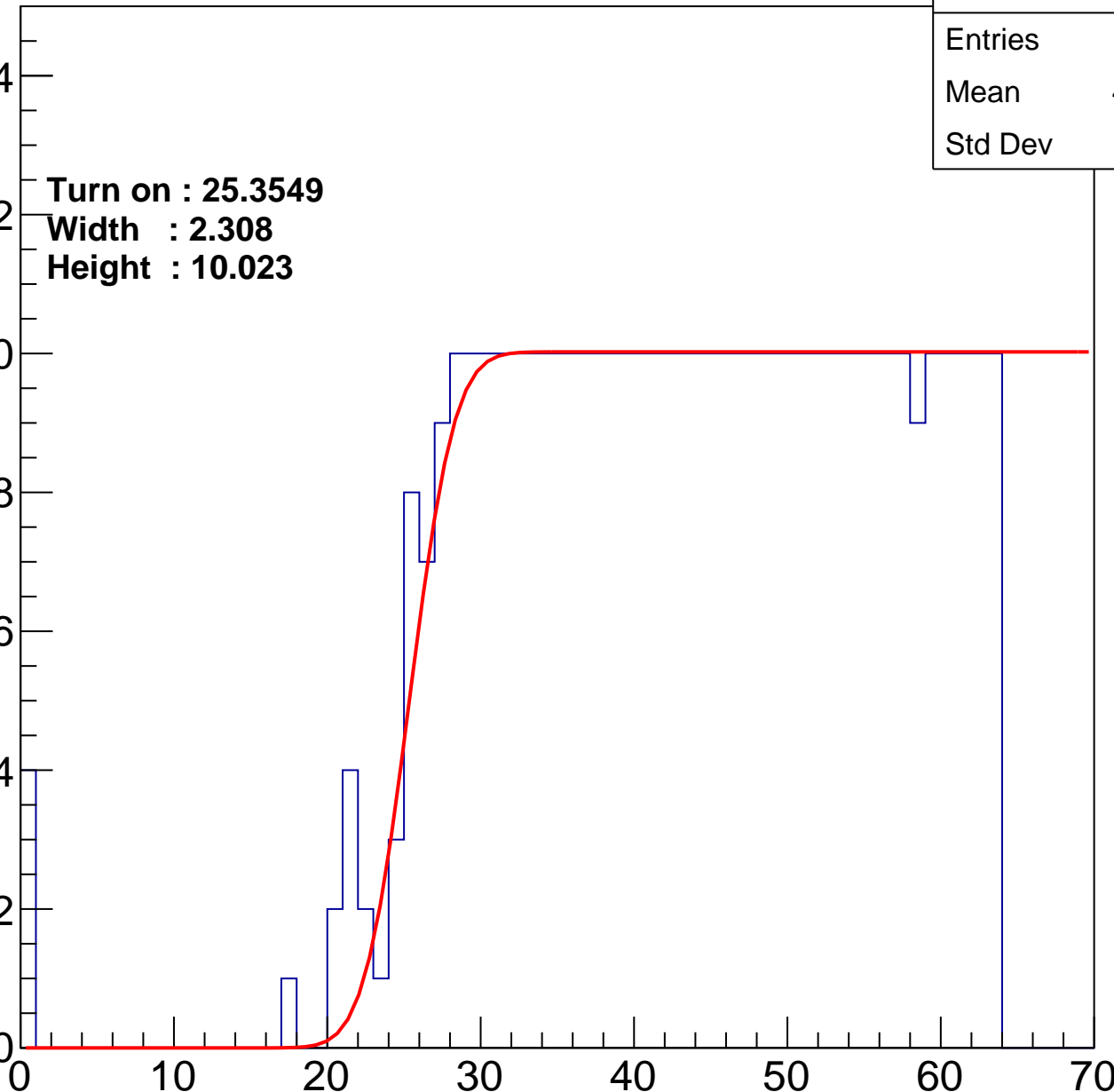
Width : 2.308

Height : 10.023

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch113

calib_packv5_042523_0143.root, FC#7, port C2

Entries	351
Mean	45.54
Std Dev	11.23

Turn on : 29.2948

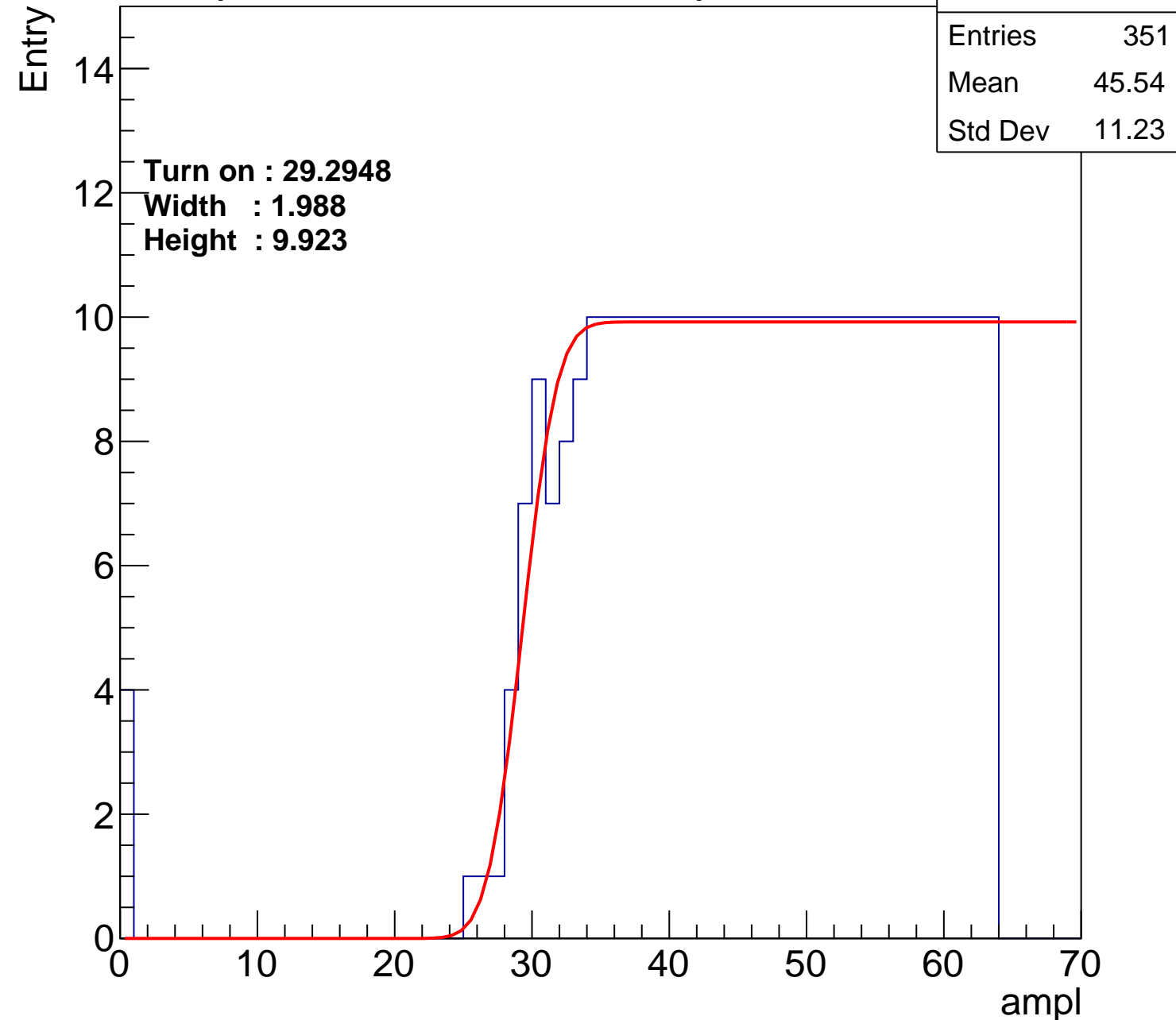
Width : 1.988

Height : 9.923

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch114

calib_packv5_042523_0143.root, FC#7, port C2

Entries	415
Mean	42.54
Std Dev	12.42

Turn on : 22.6004

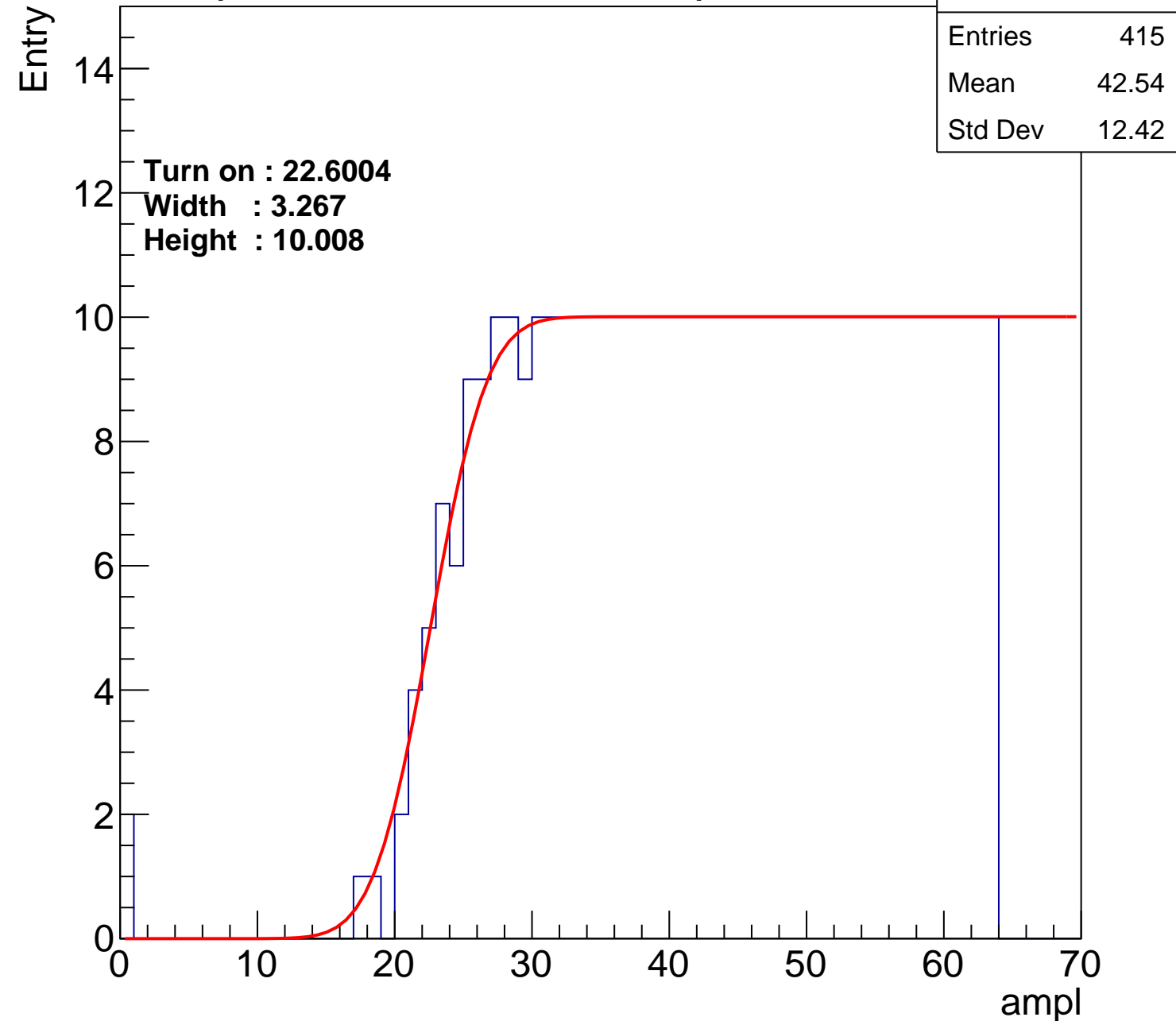
Width : 3.267

Height : 10.008

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch115

calib_packv5_042523_0143.root, FC#7, port C2

Entries	371
Mean	44.4
Std Dev	12.07

Turn on : 27.8485

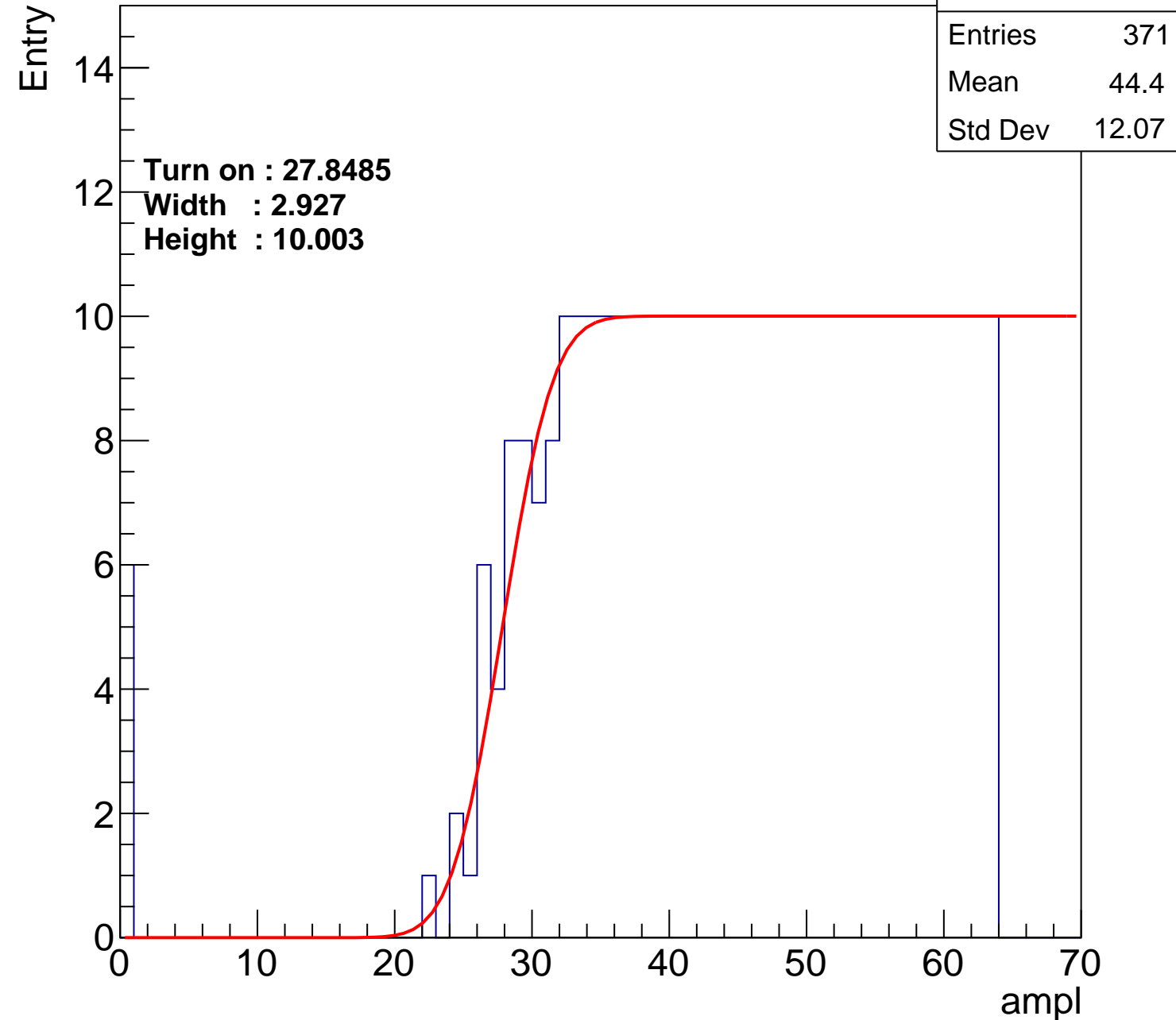
Width : 2.927

Height : 10.003

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch116

calib_packv5_042523_0143.root, FC#7, port C2

Entries	385
Mean	43.99
Std Dev	11.69

Turn on : 25.9068

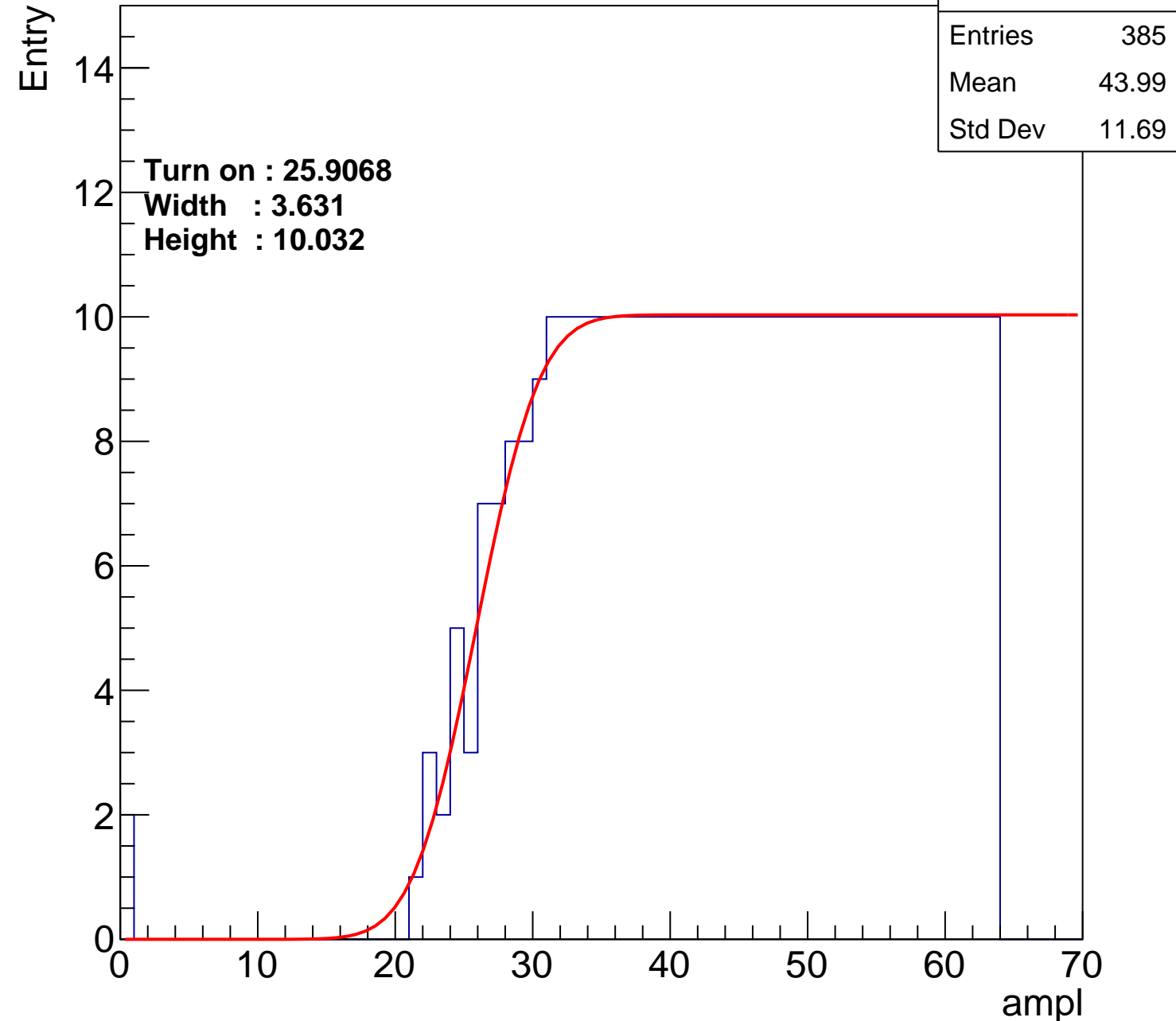
Width : 3.631

Height : 10.032

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch117

calib_packv5_042523_0143.root, FC#7, port C2

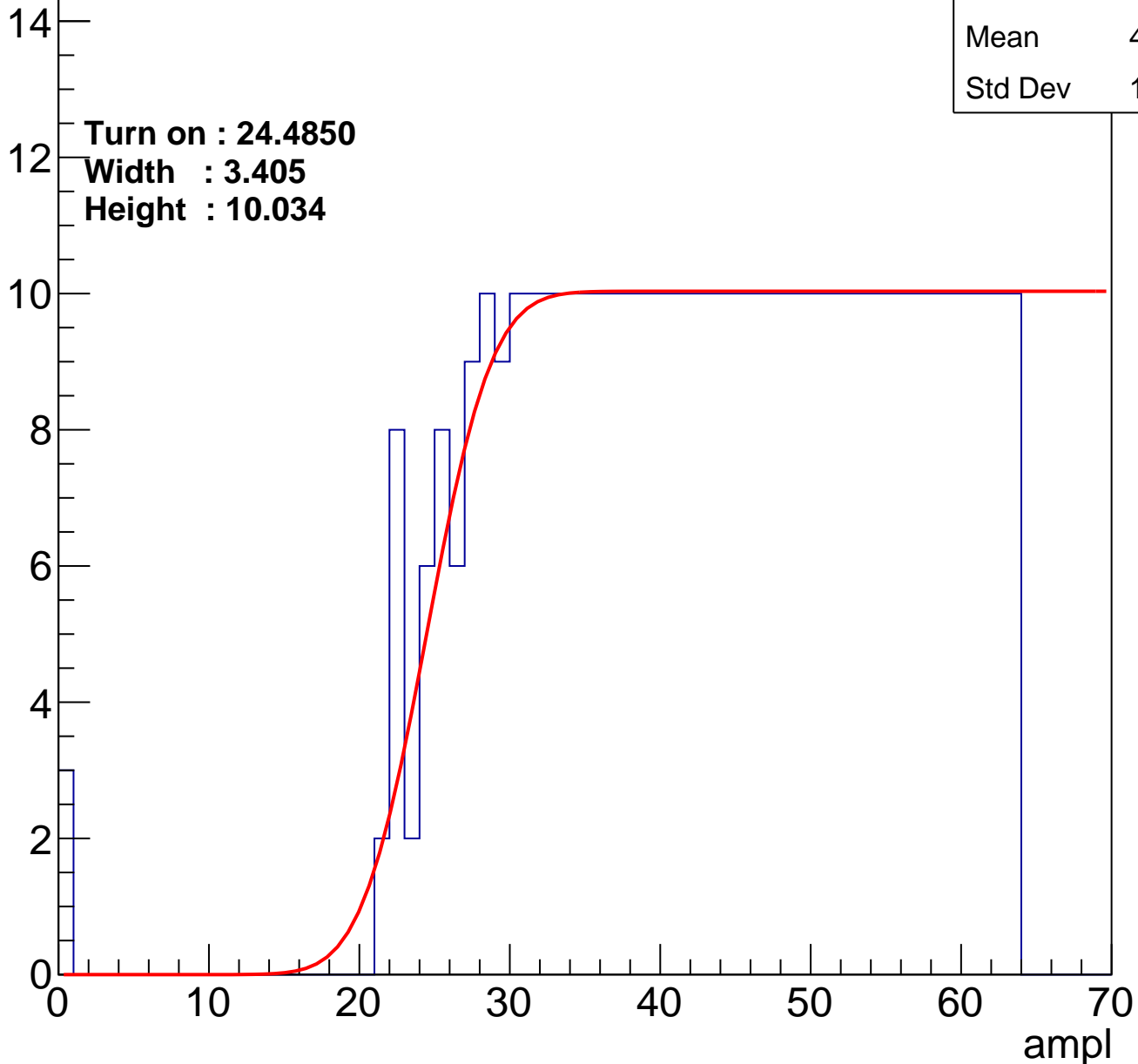
Entries	403
Mean	43.07
Std Dev	12.26

Turn on : 24.4850

Width : 3.405

Height : 10.034

Entry



B1L103S, U2-ch118

calib_packv5_042523_0143.root, FC#7, port C2

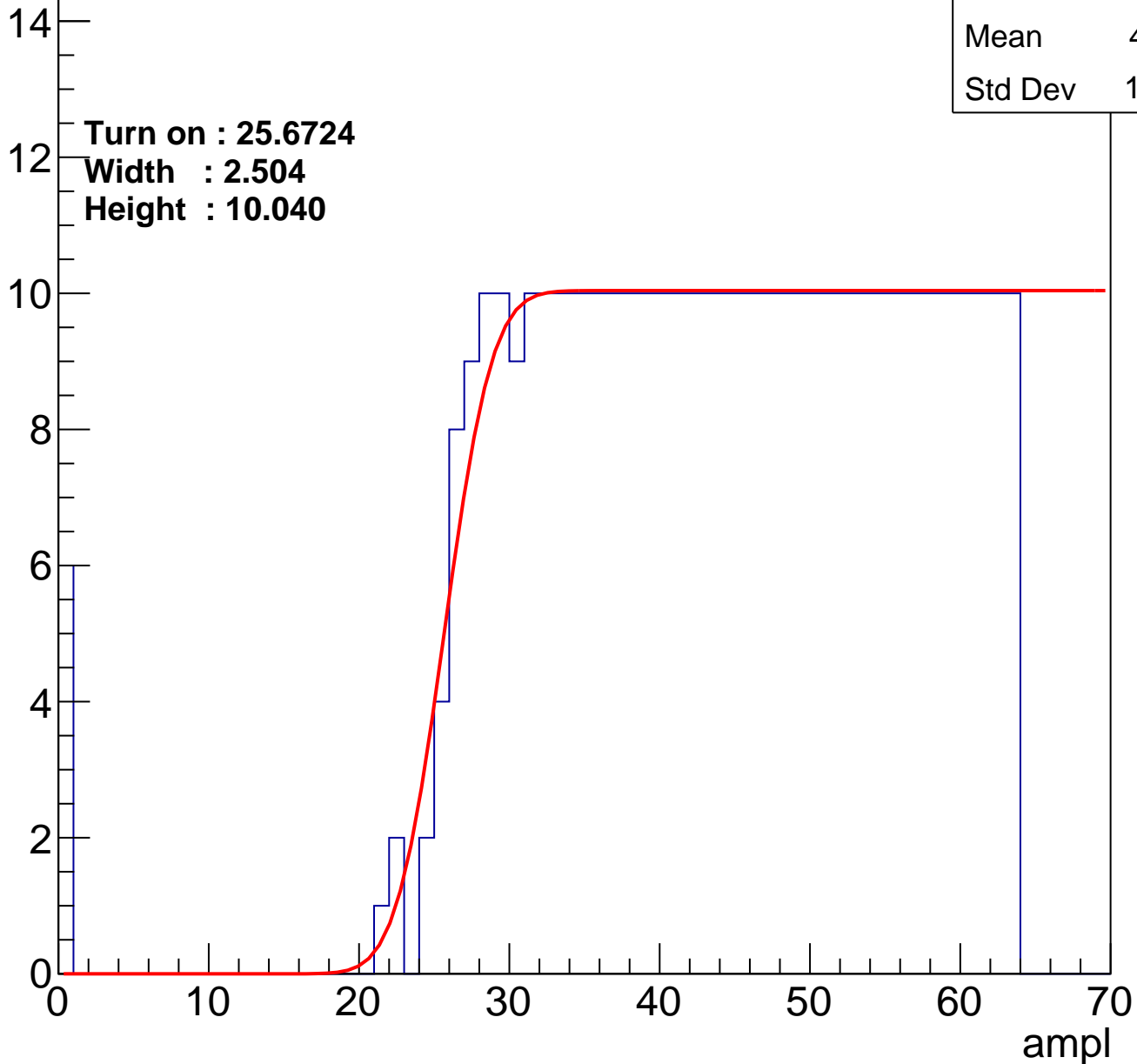
Entries	391
Mean	43.51
Std Dev	12.38

Turn on : 25.6724

Width : 2.504

Height : 10.040

Entry



B1L103S, U2-ch119

calib_packv5_042523_0143.root, FC#7, port C2

Entries	377
Mean	44.25
Std Dev	11.84

Turn on : 26.9505

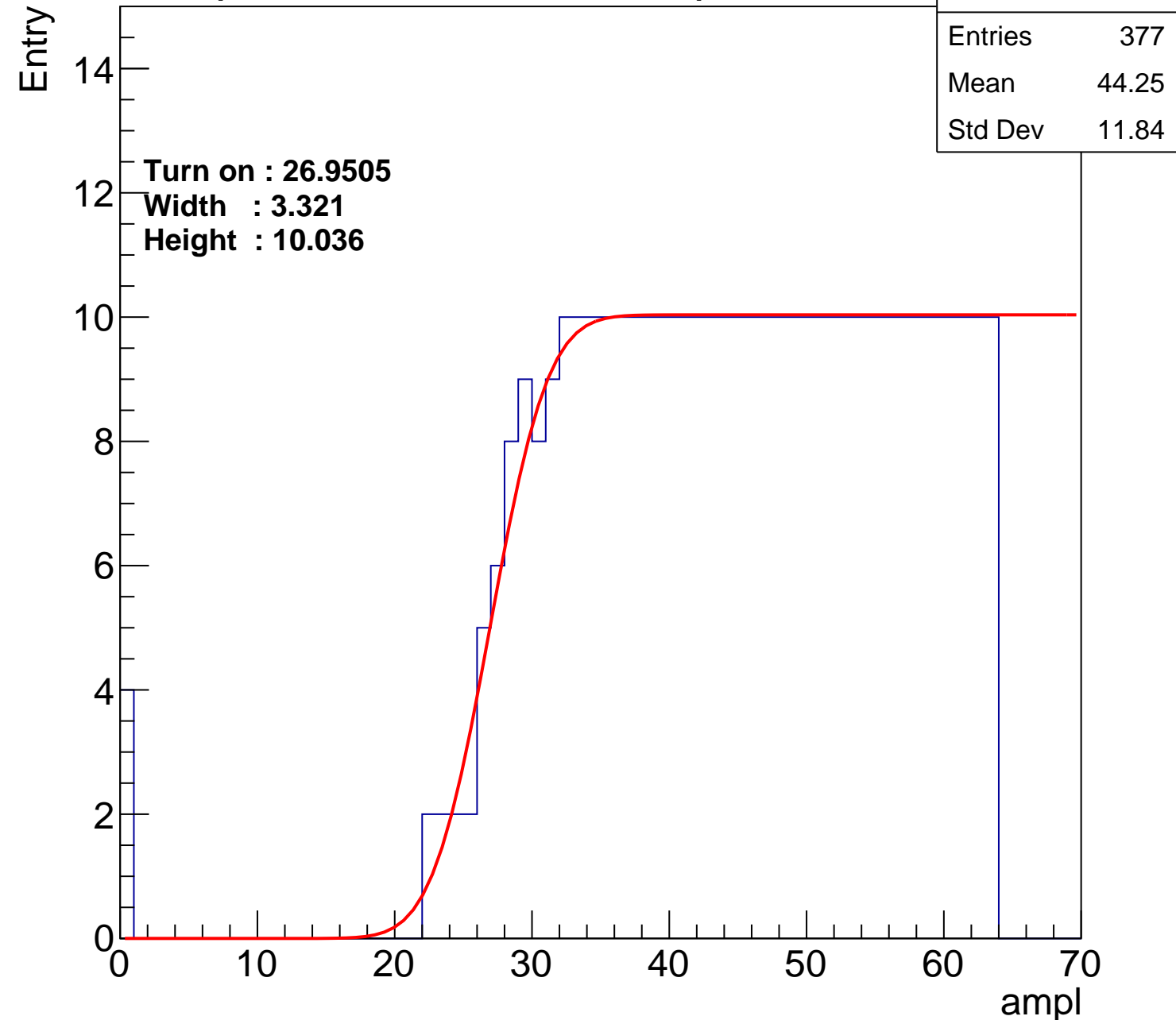
Width : 3.321

Height : 10.036

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch120

calib_packv5_042523_0143.root, FC#7, port C2

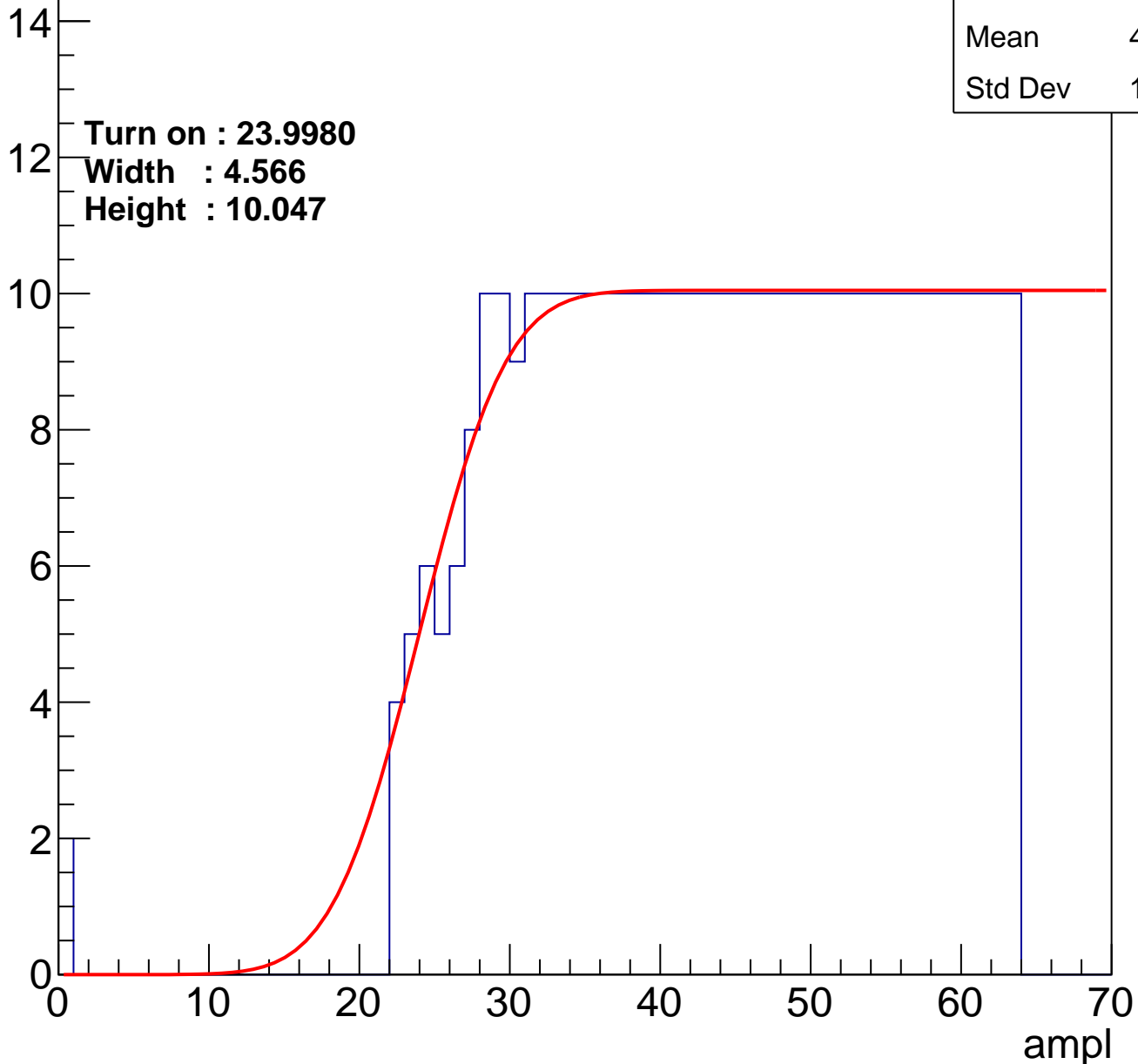
Entries	395
Mean	43.53
Std Dev	11.89

Turn on : 23.9980

Width : 4.566

Height : 10.047

Entry



B1L103S, U2-ch121

calib_packv5_042523_0143.root, FC#7, port C2

Entries	382
Mean	43.99
Std Dev	11.99

Turn on : 26.4644

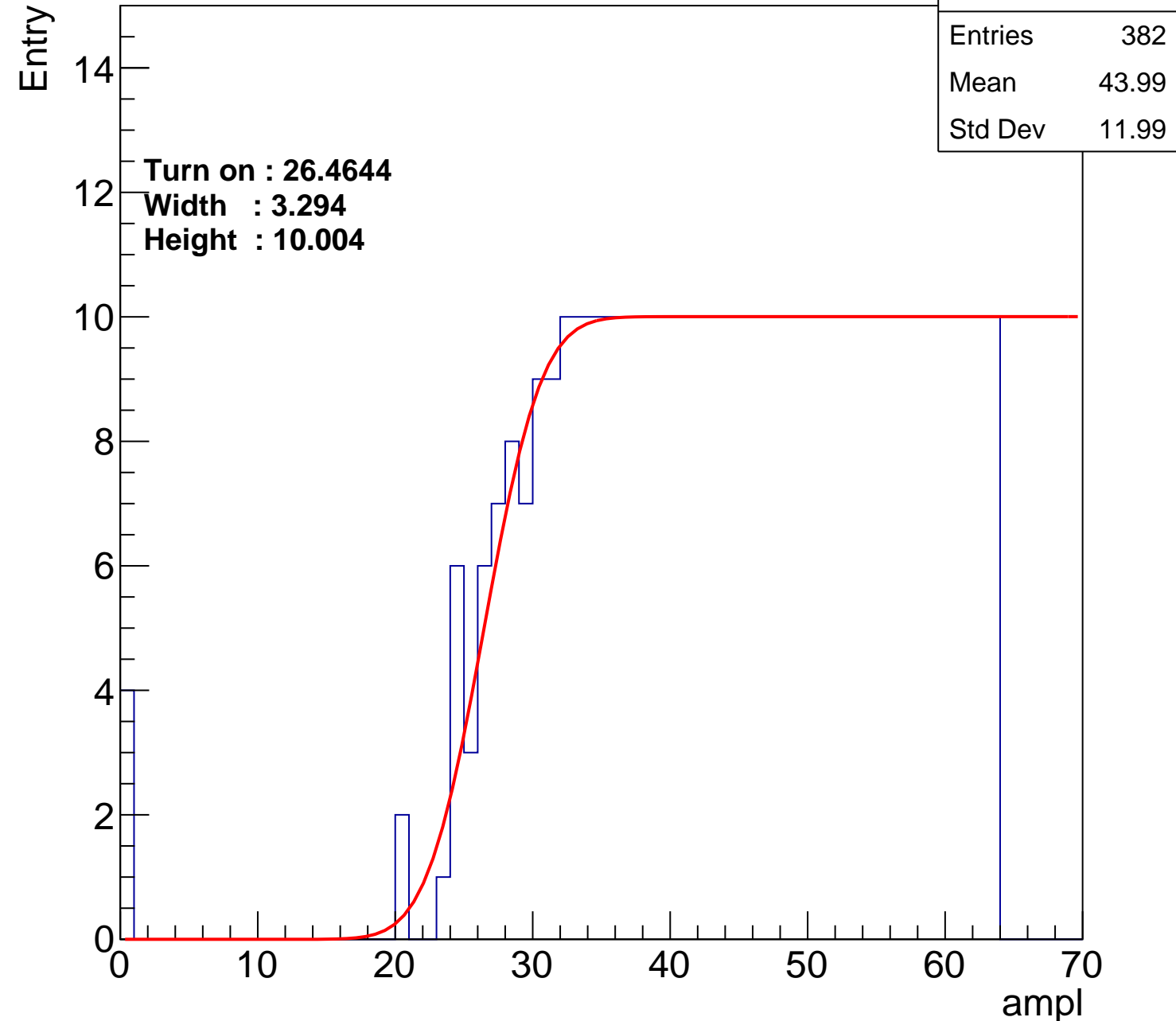
Width : 3.294

Height : 10.004

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch122

calib_packv5_042523_0143.root, FC#7, port C2

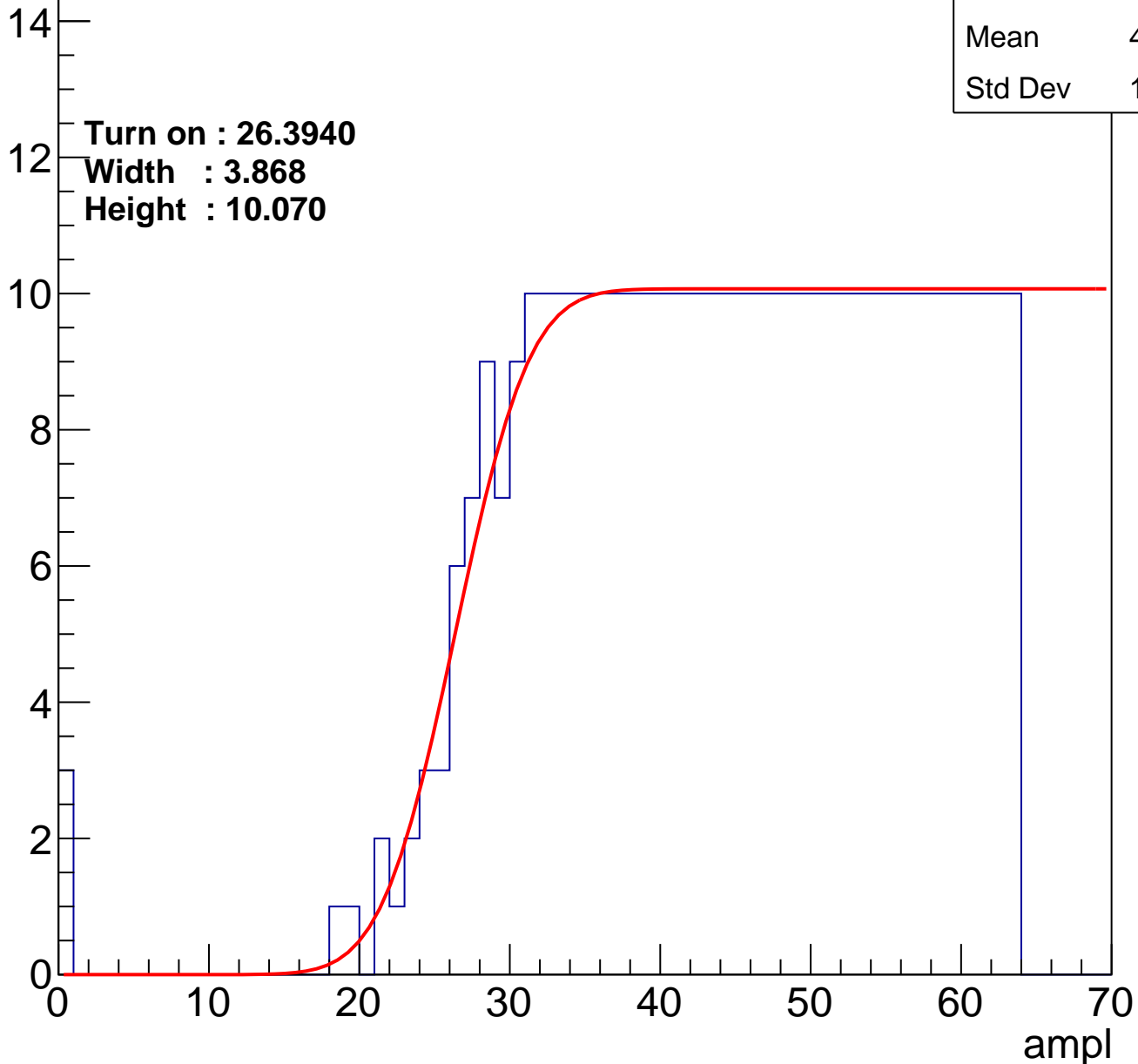
Entries	384
Mean	43.94
Std Dev	11.89

Turn on : 26.3940

Width : 3.868

Height : 10.070

Entry



B1L103S, U2-ch123

calib_packv5_042523_0143.root, FC#7, port C2

Entries	383
Mean	43.95
Std Dev	11.98

Turn on : 25.4848

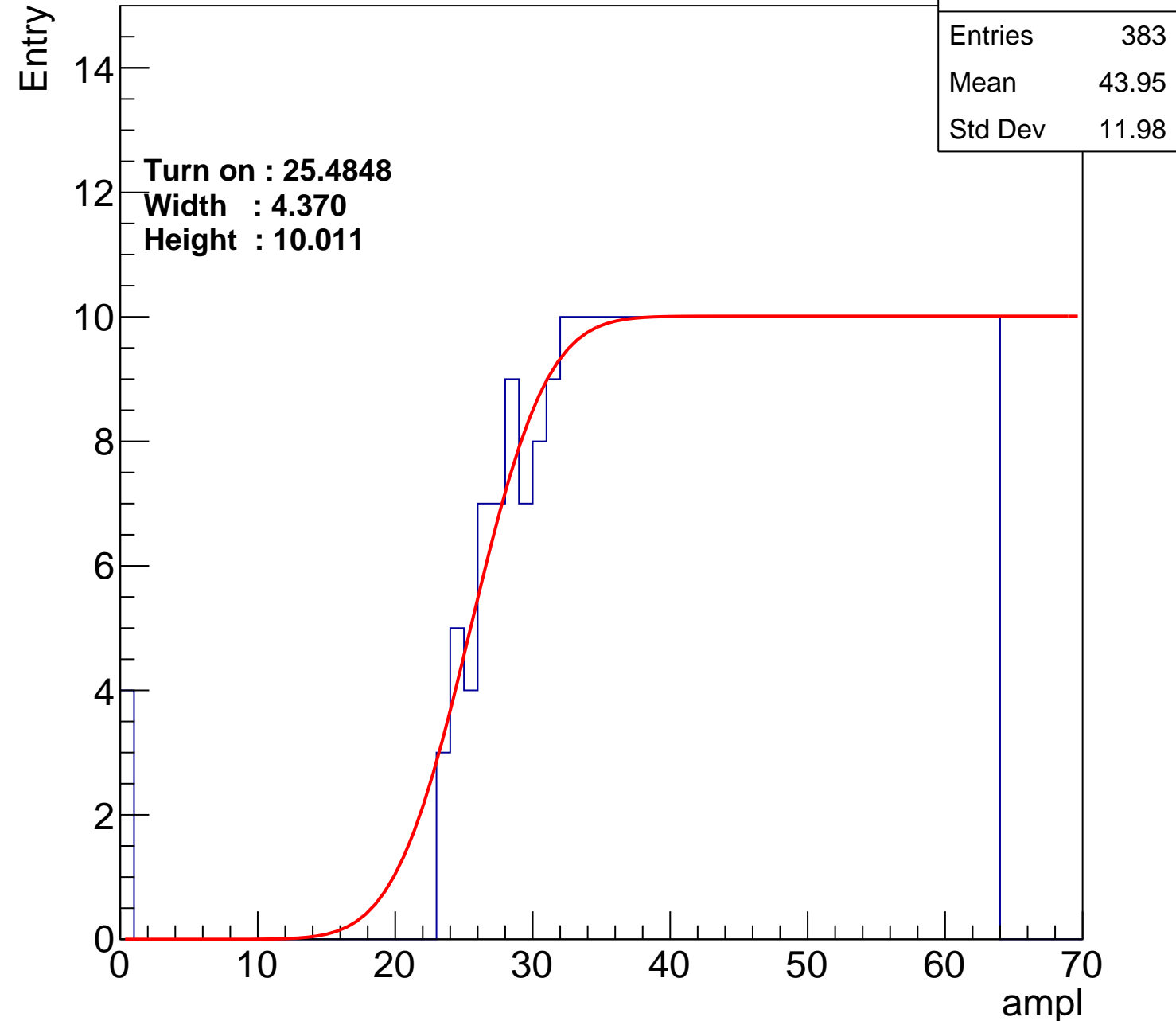
Width : 4.370

Height : 10.011

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch124

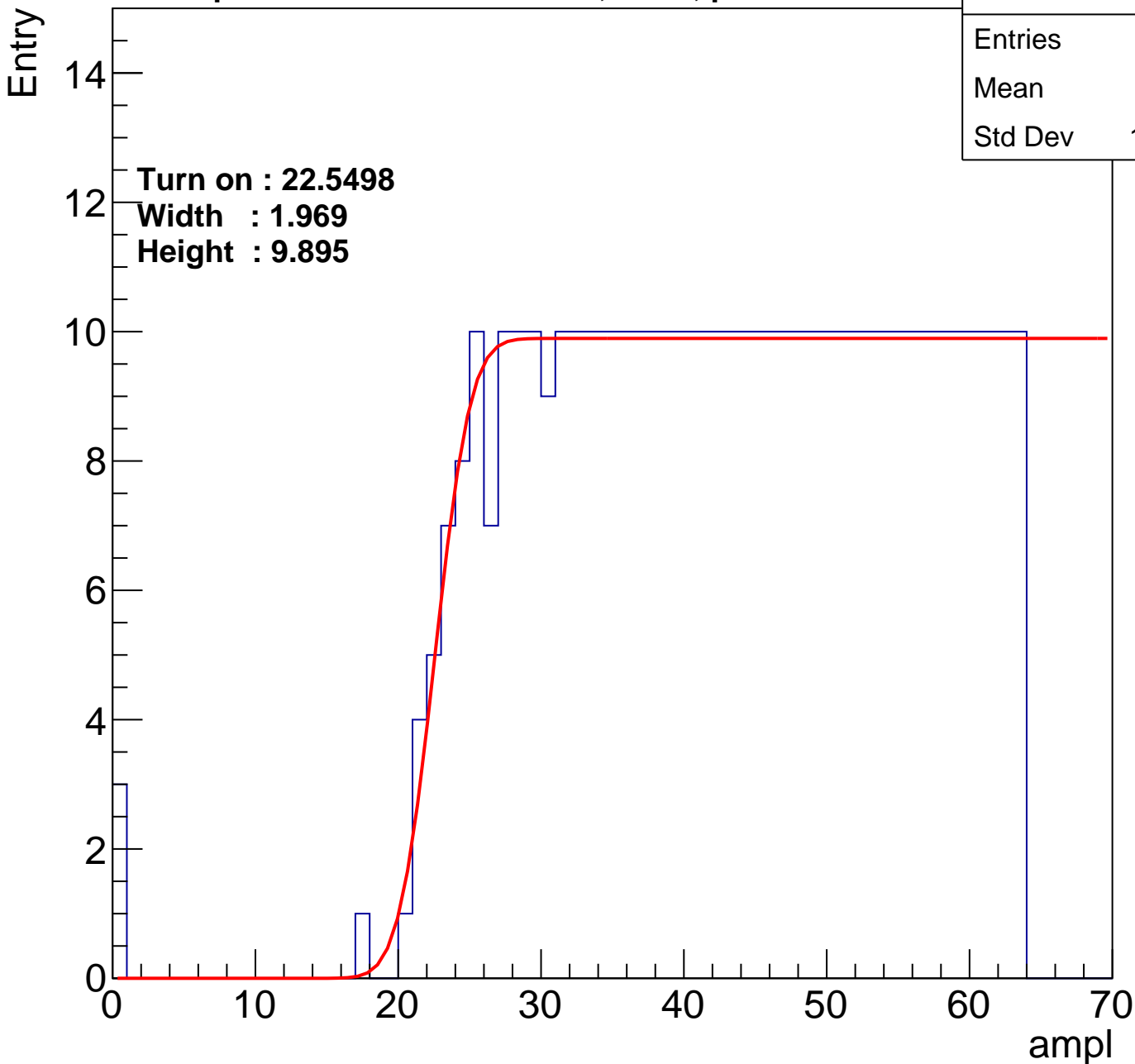
calib_packv5_042523_0143.root, FC#7, port C2

Entries	415
Mean	42.5
Std Dev	12.54

Turn on : 22.5498

Width : 1.969

Height : 9.895



B1L103S, U2-ch125

calib_packv5_042523_0143.root, FC#7, port C2

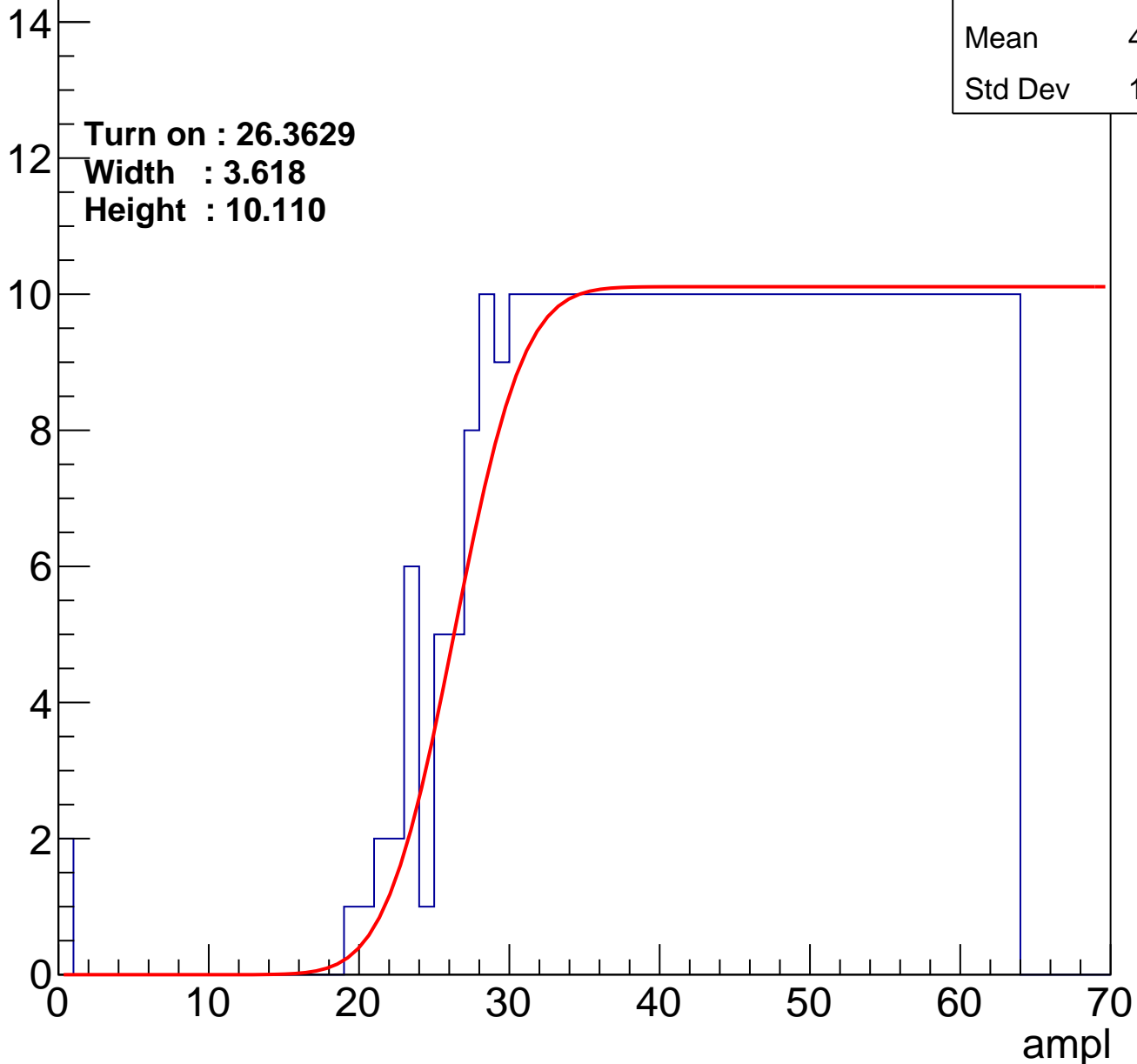
Entries	392
Mean	43.65
Std Dev	11.87

Turn on : 26.3629

Width : 3.618

Height : 10.110

Entry



B1L103S, U2-ch126

calib_packv5_042523_0143.root, FC#7, port C2

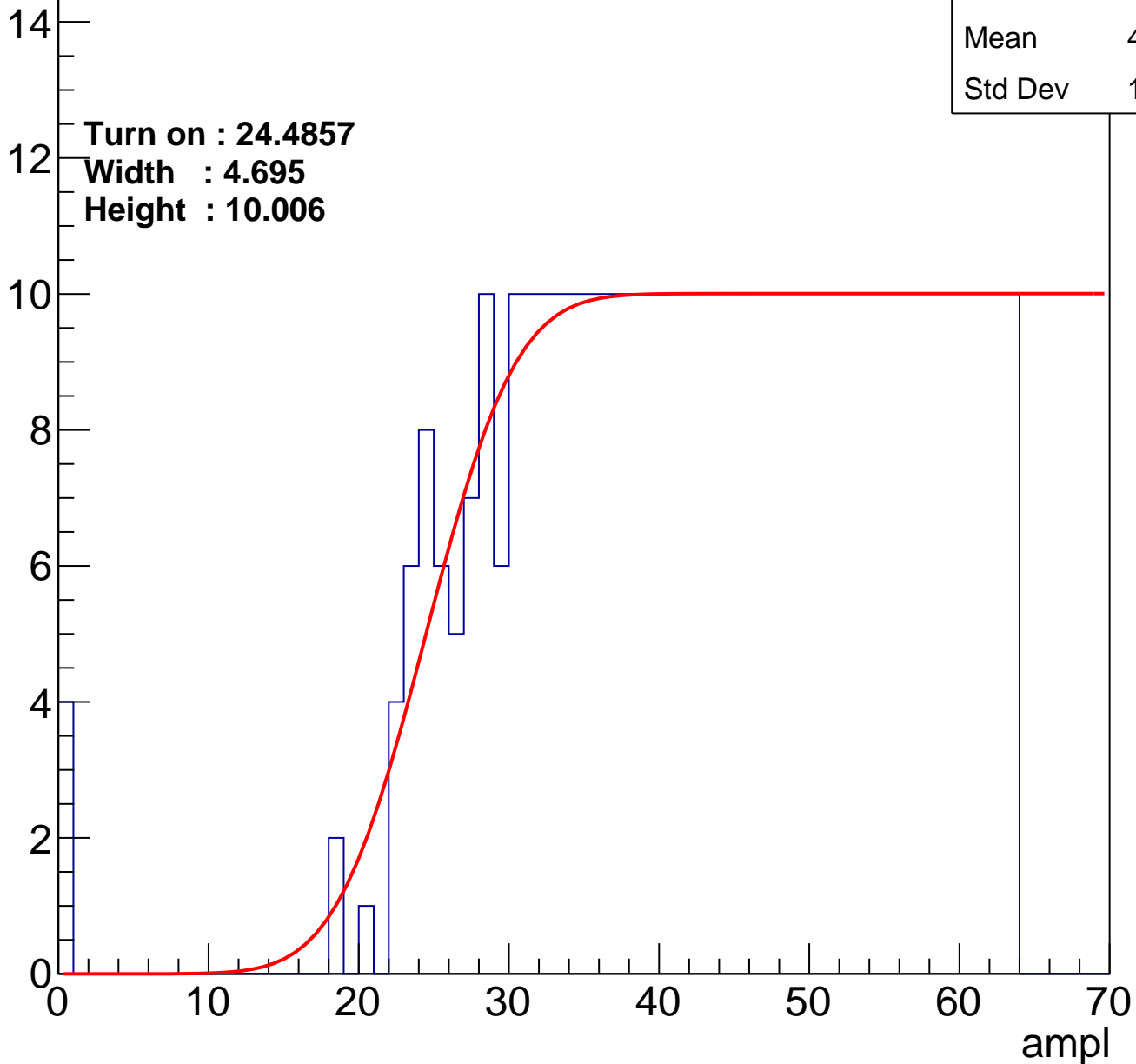
Entries	399
Mean	43.13
Std Dev	12.44

Turn on : 24.4857

Width : 4.695

Height : 10.006

Entry



B1L103S, U2-ch127

calib_packv5_042523_0143.root, FC#7, port C2

Entries	384
Mean	43.95
Std Dev	11.86

Turn on : 25.9917

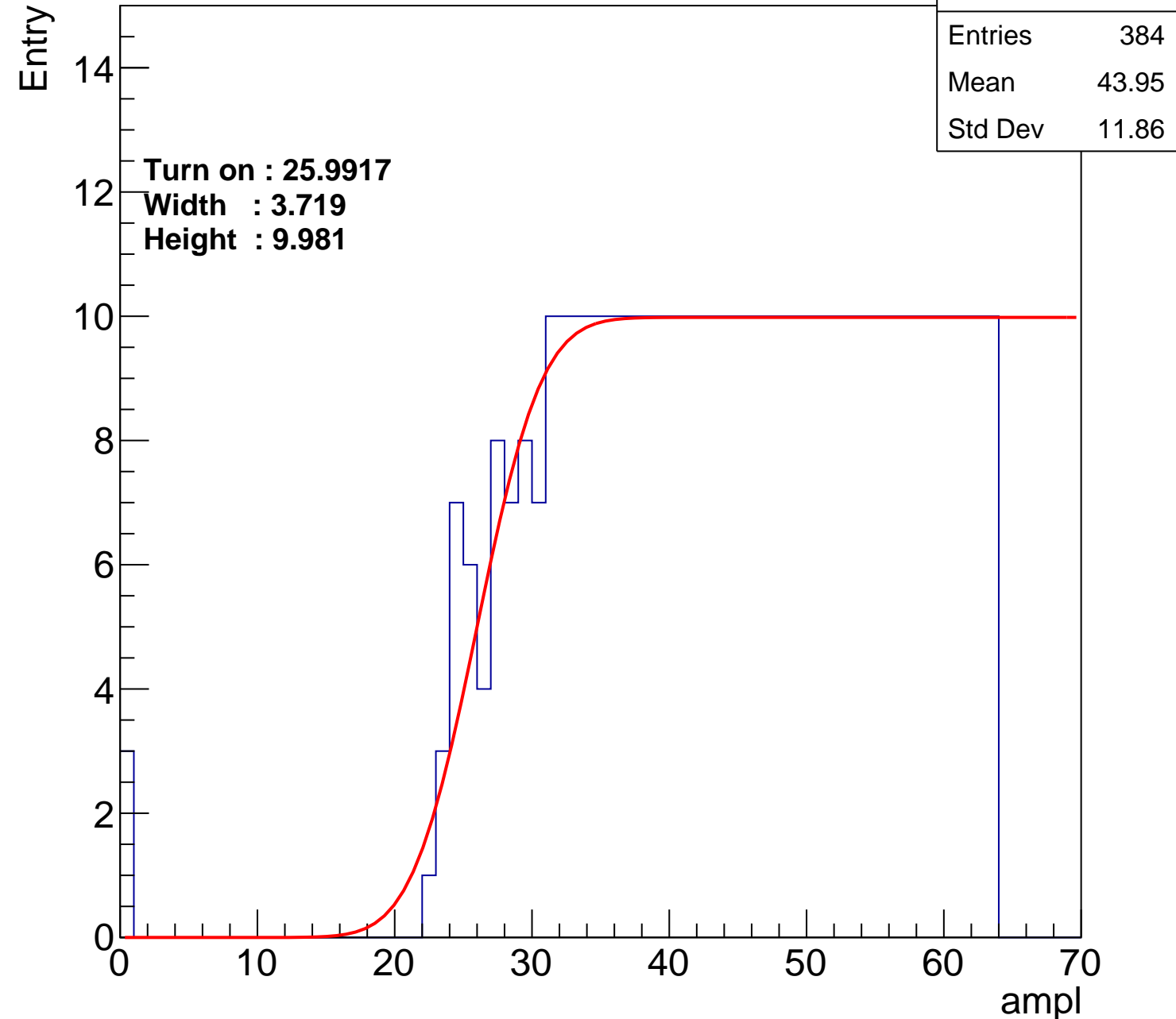
Width : 3.719

Height : 9.981

Entry

14
12
10
8
6
4
2
0

ampl



B1L103S, U2-ch127

calib_packv5_042523_0143.root, FC#7, port C2

Entries	384
Mean	43.95
Std Dev	11.86

Turn on : 25.9917

Width : 3.719

Height : 9.981

Entry

14
12
10
8
6
4
2
0

ampl

